ROCKWELL 1985 DATA BOOK

Semiconductor Products Division

Rockwell International

$10.00

1985 DATA BOOK

Rockwell International

Semiconductor Products Division

Order No. 1
January, 1985

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TABLE OF CONTENTS

TABLE OF CONTENTS (Continued)

ROCKWELL SEMICONDUCTORS CROSS-REFERENCE GUIDE

SYNERTEK	ROCKWELL
SY6502	R6502
SY6503	R6503
SY6504	R6504
SY6505	R6505
SY6506	R6506
SY6507	R6507
SY6512	R6512
SY6513	R6513
SY6514	R6514
SY6515	R6515
SY6520	R6520
SY6522	R6522
SY6530	R6530
SY6532	R6532
SY6545-1	R6545-1
SY6551	R6551

INTEL	ROCKWELL
8272	R6765

MOTOROLA	ROCKWELL
MC6820	R6520
(1)MC6821	R6520
(2)MC6845	R6545-1
(2)MC6845M	R6545-1
MC68000	R68000

(1) except application of (2) TTL loads
(2) ask customer for evaluation

MOS TECHNOLOGY	ROCKWELL
MPS6502	R6502
MPS6503	R6503
MPS6504	R6504
MPS6505	R6505
MPS6506	R6506
MPS6507	R6507
MPS6512	R6512
MPS6513	R6513
MPS6514	R6514
MPS6515	R6515
MPS6520	R6520
MPS6522	R6522
MPS6530	R6530
MPS6532	R6532

NCR	ROCKWELL
NCR6500/1E	R6500/1EC
NCR6500/1	R6500/1
NCR6500/11	R6500/11
NCR6500/12	R6500/12
NCR6500/13	R6500/13
NCR6500/11E	R6511Q
NCR6500/41	R6500/41
NCR6500/42	R6500/42
NCR6500/43	R6500/43
NCR6500/41E	R6541Q
NCR65C02	R65C02

GTE	ROCKWELL
G65SC02	R65C02
G65SC21	R65C21
G65SC51	R65C51
	R23C64

RICOH	ROCKWELL
RD5H64	R87C64

AMI	ROCKWELL
S2333	R2332
S2364	R2364
S23128	R23128
S6551	R6551

FUJITSU	ROCKWELL
MBM27C64	R87C64

AMD	ROCKWELL
AM2764	R87C64

RCA	ROCKWELL
CDP65564	R23C64

NEC	ROCKWELL
765	R6765

APPLICATION NOTE INDEX

Order No.	Title
R6500 Microprocessors and Peripherals	
223	R6502/R6532 Timer Interrupt Precautions
296	R6502 Interfacing Higher Speed R6502's to Lower Speed I/O & Memory
256	Printer Control with R6522 VIA (Versatile Interface Adapter)
226	R6531 ROM-RAM-I/O Counter (RRIOC)
227	R6531 Address Lines for Contiguous ROM
225	Generating Non-Standard Baud Rates with the R6551 ACIA (Asynchronous Communication Interface Adapter)
208	Low-Cost Crystal Oscillator for Clock Input Frequency Generator
231	Interfacing R6500 Microprocessors to a FDC (Floppy Disk Controller)
276	Crystal Considerations for R6500 Family Devices
287	Using R65XX Family Peripheral Devices with Z80 CPU
R6500/* Microcomputers	
239	Interfacing R6500/1 to SIDC (Serial Input Display Controller)
237	R6500/1 Microcomputer-Based Printer Controller
258	A Logical Tester for R6500/1 One-Chip Microcomputer
2163	A Dot Matrix Controller System Design Using the 10938/10939 Display Drivers and R6500/1EB Microcomputer
2162	A Low Cost Development Module for the R65F11/R65F12 FORTH Microcomputer
2178	Design Considerations for Conversion to Rockwell R6500/11 and R6501Q from Intel 8051/8031
2182	R6500/41 Based Stepper Motor Controller
Intelligent Display Controllers	
2163	A Dot Matrix Controller System Design Using the 10938/10939 Display Drivers and R6500/1EB Microcomputer
2175	Display Controller Designer Notes

Order No.	Title
Microcomputer Development Systems	
224	System 65 to AIM 65 Microcomputer Interface
240	User 65 Emulation with less than 512 Bytes of RAM
246	System 65 Bus Interface
2129	0S3.1 Monitor ROM & Macro Assembler/Linking Loader
2158	CMOS User 65 System 65 Development System
2166	R6500 Software Preparation System Development Configurations
Integral Modems	
607	R24 Modem Options
608	Quality of Received Data for R24 Modem
619	R24DC Interface to EIA RS-232-C
622	R24DC Interface to U.S. Switched Telephone Network
624	R24DC Modem Options
634	R24LL and R24DC Modem Control Signal To LED Interface
632	R24LL Modem Interface to EIA RS-232-C
635	R24LL Modem Options
617	4800/9600 BPS Modem Interfacing
637	Picture Plotter Data Transmission System
654	R96FAX Modem RAM Write Control
655	R96FAX Modem Recommended Receive Sequence for Group 2 Facsimile
656	R96FAX Modem Scrambled Ones Work-Around for R5300-18 and R5300-19
657	R96DP and R48DP Modems RAM Write Control
658	High Speed Modems Filter Characteristics

PART NO./DATA BOOK PAGE INDEX

PART NO./DATA BOOK PAGE INDEX (Continued)

PRODUCT INDEX

1

SECTION 1
R68000 MICROPROCESSOR AND PERIPHERALS

R68000 MICROPROCESSOR AND PERIPHERAL FAMILY
16-bit Speed and Data Capacity, Peripherals to Build Efficient Systems

Rockwell peripherals give a designer everything the 68000 family promises. They allow you to design functional systems utilizing all the speed and data handling potential of the 16-bit 68000 family.

First of these are the Rockwell designed 16-bit peripherals—multi-protocol communications controller, double density floppy disk controller, local area network controller—each a significant "first" that eliminates the "glue parts" between a CPU and peripherals.

Not to be ignored, however, is the very wide and complete family of 8-bit devices—processors, peripherals, memory, single-chip microcomputers—compatible with the R68000 family. All of the R6500 family of devices described in this Data Book are directly compatible with the R68000 bus. They often provide efficient, economical and very flexible ways of implementing system designs.

The Rockwell R68000 16-bit microprocessor (MPU) operates at clock speeds of 4, 6, 8, 10 or 12.5 MHz to match essentially any application.

The R68561 multi-protocol communications controller (MPCC) is the highest throughput communications device ever made commercially available. It operates up to 4 Mbits/sec and supports all major communication protocols. It's available to work with either 16-bit or 8-bit busses and can be adapted to function with essentially any of today's more common busses.

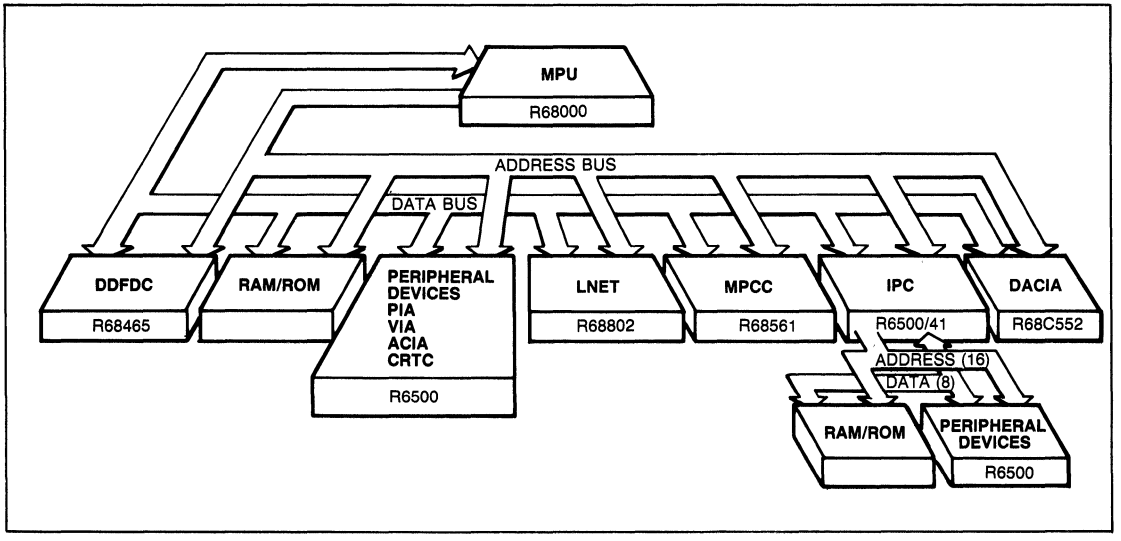
The R68465 double density floppy disk controller (DDFDC) is an intelligent device that can run up to four disk drives without the many support devices previously required.

The R68802* provides a flexible local area network (LNET) controller for the R68000. It supports both the IEEE 802.3 and Ethernet* standards based on the proven CSMA/CD technique together with network statistics.

The R68C552 provides an easily implemented, program controlled interface between 16-bit microprocessor-based systems and serial communication data sets and modems. This device is the first CMOS ACIA in the industry.

Rockwell lets you build efficient and economical 16-bit systems through families of 16-bit and 8-bit peripherals, all compatible. No other supplier offers you more.

**R68802 is a trademark of the Rockwell International Corp.*
**Ethernet is a trademark of the Xerox Corp.*



R68000/R6500 Peripheral Migration

Rockwell

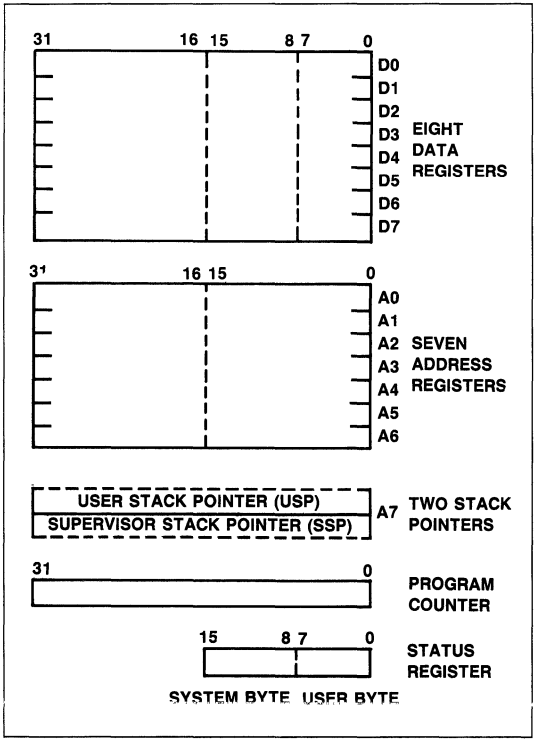
R68000
16-BIT MICROPROCESSING UNIT (MPU)

1

PRELIMINARY

DESCRIPTION

The R68000 microprocessor is designed for high performance where operational computation and versatility is required. The R68000 provides powerful mass-memory handling capability and architectural features designed to fit the broad range of 16-bit needs. The Rockwell family of 16-bit products also includes a wide range of peripherals that will allow complete system design and manufacture.



R68000 Registers

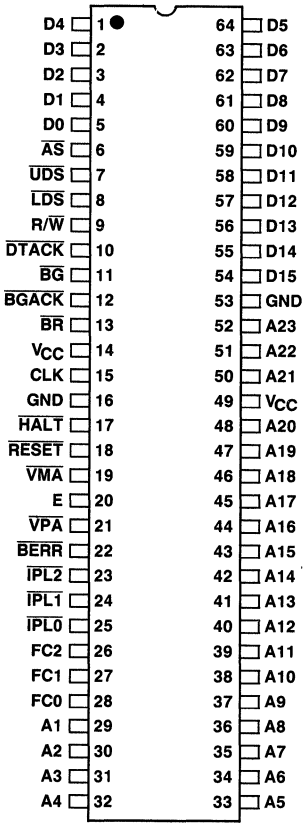
The R68000 offers seventeen 32-bit registers in addition to the 32-bit program counter and a 16-bit status register. The first eight registers (D0-D7) are used as data registers for byte (8-bit), word (16-bit), and long word (32-bit) data operations. The second set of seven registers (A0-A6) and the system stack pointer may be used as software stack pointers and base address registers. In addition, these registers may be used for word and long word address operations. All 17 registers may be used as index registers.

FEATURES

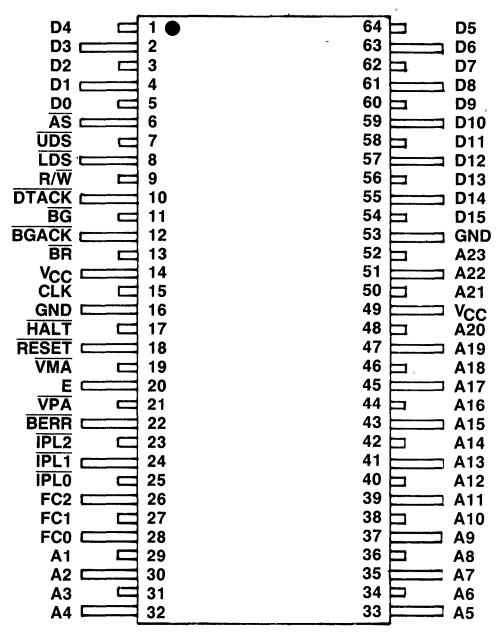
- 16M byte (8M word) Linear Addressing Range
- 14 Operand Addressing Modes
- 56 Powerful Instruction Types
- Instruction Set Supports Structured High-Level Languages
- Pipelining Instruction Execution
- 32-Bit Program Counter
- 16-Bit Data Bus
- 23-Line Address Bus
- 32-Bit Data and Address Registers Including:
  - — Eight General Purpose Data Registers
  - — Seven Address Registers
  - — Two Stack Pointers (User, Supervisory)
- All 17 Registers Can Be Index Registers
- Memory Mapped Peripheral Devices
- Vector Generated Exception Processing
- Seven Unique Autovectors for Interrupt Service Routines
- Trace Mode for Software Debugging
- Operations Occur on Five Main Data Types
  - — Bit
  - — BCD
  - — Byte
  - — Word
  - — Long Word
- Asynchronous and Synchronous Peripheral Interface Capability
- Many Peripheral Chips Available
  - — R68560 Multi-Protocol Communications Controller
  - — R68465 Double Density Floppy Disk Controller
  - — R68802 Local Network Controller
- Up to 12.5 MHz Input Clock
- +5 VDC Power Supply

Document No. 68650N01

Product Description Order No. 700
Rev. 5, October 1984



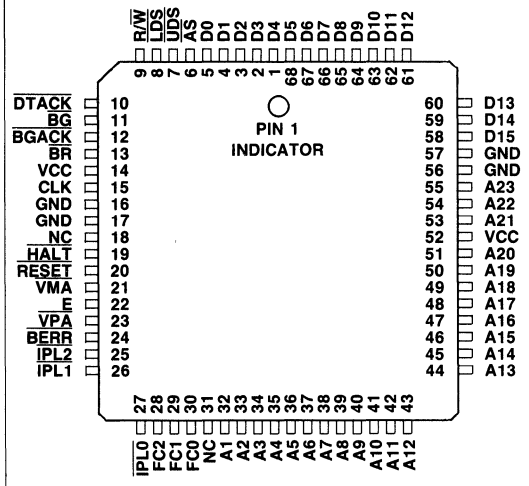
R68000C/P Pin Assignments—64-Pin DIP



R68000Q Pin Assignments—64-Pin QUIP

ORDERING INFORMATION

Part Number	Package Type	Frequency (MHz)	Temperature Range (°C)
R68000C4	Ceramic DIP	4	0 to +70
R68000C6	Ceramic DIP	6	0 to +70
R68000C8	Ceramic DIP	8	0 to +70
R68000C10	Ceramic DIP	10	0 to +70
R68000C12	Ceramic DIP	12.5	0 to +70
R68000J6	Plastic CC	6	0 to +55
R68000J8	Plastic CC	8	0 to +55
R68000J10	Plastic CC	10	0 to +55
R68000J12	Plastic CC	12.5	0 to +55
R68000P6	Plastic DIP	6	0 to +55
R68000P8	Plastic DIP	8	0 to +55
R68000P10	Plastic DIP	10	0 to +55
R68000P12	Plastic DIP	12.5	0 to +55
R68000Q6	Plastic QUIP	6	0 to +55
R68000Q8	Plastic QUIP	8	0 to +55
R68000Q10	Plastic QUIP	10	0 to +55
R68000Q12	Plastic QUIP	12.5	0 to +55



R68000J Pin Assignments—68-Pin PCC

SIGNAL DESCRIPTION

The following paragraphs briefly describe the input and output signals and also reference (if applicable) other paragraphs that contain more detail about the function being performed. Bus operation during the various machine cycles and operations is also discussed. The input and output signals can be functionally organized into the groups shown in Figure 1.

Note

The terms assertion and negation are used to avoid confusion when dealing with a mixture of "active-low" and "active-high" signals. The terms assert, or assertion, indicates that a signal is active, or true, independent of whether that voltage is low or high. The term negate, or negation, indicates that a signal is inactive or false.

ADDRESS BUS (A1 THROUGH A23). This 23-bit, unidirectional, three-state bus can address eight megawords of data. It provides the address for bus operation during all cycles except interrupt cycles. During interrupt cycles, address lines A1, A2, and A3 encode the interrupt level to be serviced while address lines A4 through A23 are all set high.

DATA BUS (D0 THROUGH D15). This 16-bit, bidirectional, three-state bus is the general purpose data path. It transfers and accepts data in either word or byte length. During an interrupt acknowledge cycle, an external device supplies the vector number on data lines D0-D7.

ASYNCHRONOUS BUS CONTROL. Asynchronous data transfers are handled using the following control signals: address strobe, read/write, upper and lower data strobes, and data transfer acknowlege. These signals are explained in the following paragraphs.

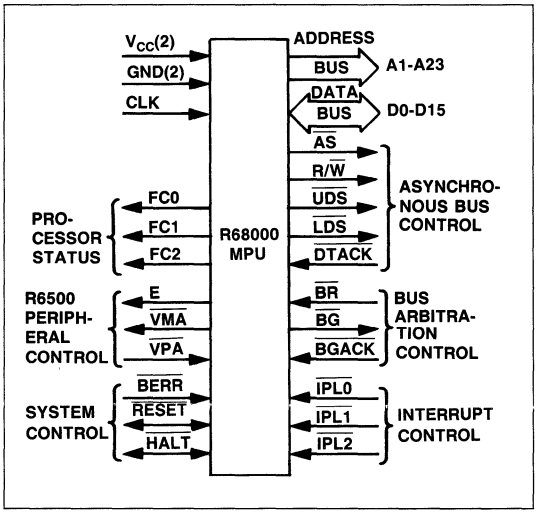


Figure 1. Input and Output Signals

Address Strobe (AS). The AS output indicates that there is a valid address on the address bus.

Read/Write (R/W). The R/W output defines the data bus transfer as a read or write cycle. The R/W signal also works in conjunction with the upper and lower data strobes as explained in the following paragraph.

Upper and Lower Data Strobes (UDS, LDS). The UDS and LDS outputs control the data on the data bus, as shown in Table 1. When the R/W line is high, the processor reads from the data bus as indicated. When the R/W line is low, the processor writes to the data bus as shown.

Data Transfer Acknowledge (DTACK). The DTACK input indicates that the data transfer is completed. When the processor recognizes DTACK during a read cycle, data is latched and the bus cycle terminated. When DTACK is recognized during a write cycle, the bus cycle terminates. Refer to **ASYNCHRONOUS VERSUS SYNCHRONOUS OPERATION.**

BUS ARBITRATION CONTROL. These three signals form a bus arbitration circuit to determine which device will be the bus master device.

Bus Request (BR). The BR input indicates to the processor that some other device desires to become the bus master. This input can be externally ORed with all other devices that could be bus masters.

Bus Grant (BG). The BG output indicates to all other potential bus master devices that the processor will release bus control at the end of the current bus cycle.

Bus Grant Acknowledge (BGACK). The BGACK input indicates that some other device has become the bus master. This signal cannot be asserted until the following four conditions are met:

1. a bus grant (BG) has been received,
2. address strobe (AS) is inactive which indicates that the processor is not using the bus

Table 1. Data Strobe Control of Data Bus

UDS	LDS	R/W	D8-D15	D0-D7
High	High	—	No valid data	No valid data
Low	Low	High	Valid data bits 8-15	Valid data bits 0-7
High	Low	High	No valid data	Valid data bits 0-7
Low	High	High	Valid data bits 8-15	No valid data
Low	Low	Low	Valid data bits 8-15	Valid data bits 0-7
High	Low	Low	Valid data bits 0-7*	Valid data bits 0-7
Low	High	Low	Valid data bits 8-15	Valid data bits 8-15*

*These conditions are a result of current implementation and may not appear on future devices.

3. data transfer acknowledge (DTACK) is inactive which indicates that neither memory nor peripherals are using the bus, and
4. bus grant acknowledge (BGACK) is inactive which indicates that no other device is still claiming bus mastership.

INTERRUPT CONTROL (IPL0, IPL1, IPL2). These input pins indicate the encoded priority level of the device requesting an interrupt. Level seven is the highest priority while level zero indicates that no interrupts are requested. Level seven cannot be masked. IPL0 is the least significant bit while IPL2 is the most significant bit. To insure an interrupt is recognized, the interrupt control lines (IPLX) must remain stable until the processor signals interrupt acknowledge (FC0, FC1, and FC2 all high).

SYSTEM CONTROL. The system control inputs either reset or halt the processor or indicate to the processor that bus errors have occurred. The three system control inputs are explained in the following paragraphs.

Bus Error (BERR). The BERR input informs the processor that a problem exists with the cycle currently being executed. Problems may be a result of:
1. nonresponding devices,
2. interrupt vector number acquisition failure,
3. illegal access request as determined by a memory management unit, or
4. other application dependent errors.

The Bus Error (BERR) signal interacts with the HALT signal to determine if exception processing should be performed or the current bus cycle should be retried.

Refer to BUS ERROR AND HALT OPERATION paragraph for additional information about the interaction of the bus error and halt signals.

Reset (RESET). This bidirectional signal line acts to reset (initiate a system initialization sequence) the processor and system in response to an external reset signal. An internally generated reset (result of a RESET instruction) resets all external devices while not affecting the internal state of the processor. A total system reset (processor and external devices) is the result of external HALT and RESET signals applied simultaneously. Refer to RESET OPERATION paragraph for additional information.

Halt (HALT). The bidirectional HALT line, when driven by an external device, will cause the processor to stop at the completion of the current bus cycle. Halting the processor using HALT causes all control signals to go inactive and all three-state lines to go to their high-impedance state. Refer to BUS ERROR AND HALT OPERATION paragraph for additional information about the interaction between the HALT and BERR signals.

When the processor has stopped executing instructions, such as in a double bus fault condition, the HALT line is driven by the processor to indicate to external devices that the processor has stopped. Refer to paragaph on Double Bus Faults.

R6500 PERIPHERAL CONTROL. These control signals are used to allow the interfacing of synchronous R6500 peripheral devices with the asynchronous R68000. These signals are explained in the following paragraphs.

Enable (E). The E output signal is the standard enable signal (Ø2 clock) common to all R6500 type peripheral devices. The period for this output is ten R68000 clock periods (six clocks low; four clocks high). Enable is generated by an internal ring counter which may come up in any state (i.e., at power on, it is impossible to guarantee phase relationship of E to CLK). E is a free-running clock and runs regardless of the state of the bus on the MPU.

Valid Peripheral Address (VPA). The VPA input indicates that the device or region addressed is a R6500 family device and that data transfer should be synchronized with the enable (E) signal. This input also indicates that the processor should use automatic vectoring for an interrupt. Refer to INTERFACE WITH R6500 PERIPHERALS.

Valid Memory Address (VMA). The VMA output indicates to R6500 peripheral devices that there is a valid address on the address bus and that the processor is synchronized to enable. This signal only responds to a valid peripheral address (VPA) input which indicates that the peripheral is a R6500 family device.

PROCESSOR STATUS (FC0, FC1, FC2). These function code outputs indicate the state (user or supervisor) and the cycle type currently being executed, as shown in Table 2. The information indicated by the function code outputs is valid whenever address strobe (AS) is active.

CLOCK (CLK). The clock input is a TTL-compatible signal that is internally buffered for development of the internal clocks needed by the processor. The clock input should not be gated off at any time and the clock signal must conform to minimum and maximum pulse width times.

SIGNAL SUMMARY. Table 3 summarizes all the signals discussed in the previous paragraphs.

Table 2. Function Code Outputs

FC2	FC1	FC0	Cycle Type
Low	Low	Low	(Undefined, Reserved)
Low	Low	High	User Data
Low	High	Low	User Program
Low	High	High	(Undefined, Reserved)
High	Low	Low	(Undefined, Reserved)
High	Low	High	Supervisor Data
High	High	Low	Supervisor Program
High	High	High	Interrupt Acknowledge

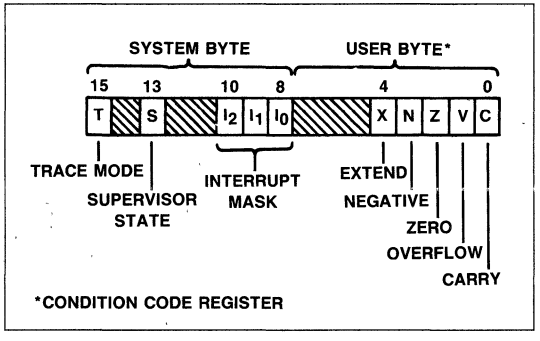
Table 3. Signal Summary

Signal Name	Mnemonic	Input/Output	Active State	Hi-Z	
				On $\overline{HALT}$	On $\overline{BGACK}$
Address Bus	A1-A23	Output	High	Yes	Yes
Data Bus	D0-D15	Input/Output	High	Yes	Yes
Address Strobe	$\overline{AS}$	Output	Low	No	Yes
Read/Write	R/$\overline{W}$	Output	Read-High Write-Low	No	Yes
Upper and Lower Data Strobes	$\overline{UDS}$, $\overline{LDS}$	Output	Low	No	Yes
Data Transfer Acknowledge	$\overline{DTACK}$	Input	Low	No	No
Bus Request	$\overline{BR}$	Input	Low	No	No
Bus Grant	$\overline{BG}$	Output	Low	No	No
Bus Grant Acknowledge	$\overline{BGACK}$	Input	Low	No	No
Interrupt Priority Level	$\overline{IPL0}$, $\overline{IPL1}$, $\overline{IPL2}$	Input	Low	No	No
Bus Error	$\overline{BERR}$	Input	Low	No	No
Reset	$\overline{RESET}$	Input/Output	Low	No*	No*
Halt	$\overline{HALT}$	Input/Output	Low	No*	No*
Enable	E	Output	High	No	No
Valid Memory Address	$\overline{VMA}$	Output	Low	No	Yes
Valid Peripheral Address	$\overline{VPA}$	Input	Low	No	No
Function Code Output	FC0, FC1, FC2	Output	High	No	Yes
Clock	CLK	Input	High	No	No
Power Input	V_{CC}	Input	—	—	—
Ground	GND	Input	—	—	—

*Open drain.

REGISTER DESCRIPTION AND DATA ORGANIZATION

STATUS REGISTER. The status register contains the eight level interrupt mask as well as the condition codes; extend (X), negative (N), zero (Z), overflow (V), and carry (C). Additional status bits indicate that the processor is in a trace (T) mode and/or in a supervisor (S) state.



Status Register

OPERAND SIZE

Operand sizes are defined as follows: a byte equals 8 bits, a word equals 16 bits, and a long word equals 32 bits. The operand size for each instruction is either explicitly encoded in the instruction or implicitly defined by the instruction operation. Implicit instructions support some subset of all three sizes.

DATA ORGANIZATION IN REGISTERS

The eight data registers support data operands of 1, 8, 16, or 32 bits. The seven address registers together with the active stack pointer support address operands of 32 bits.

DATA REGISTERS. Each data register is 32 bits wide. Byte operands occupy the low order 8 bits, word operands the low order 16 bits, and long word operands the entire 32 bits. The least significant bit is addressed as bit zero; the most significant bit is addressed as bit 31. When a data register is used as either a source or destination operand, only the appropriate low-order portion is changed; the remaining high order portion is neither used nor changed.

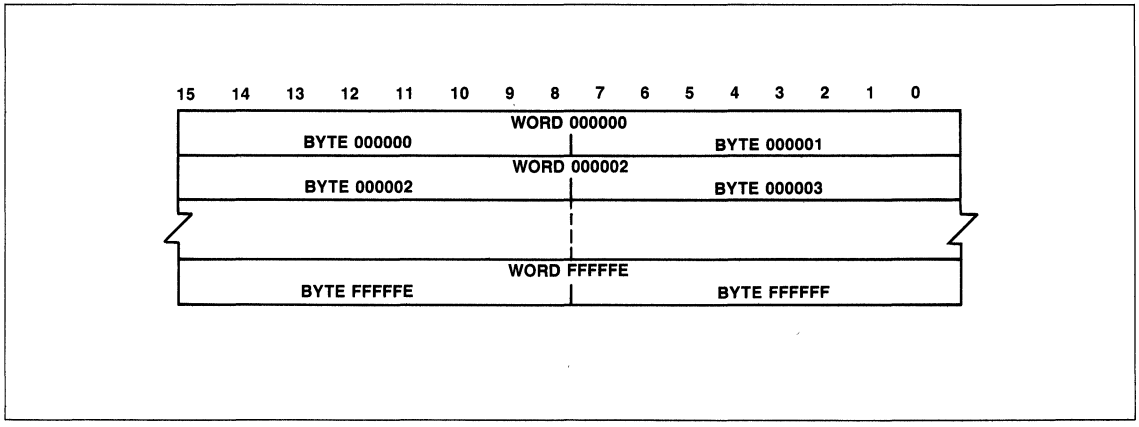


Figure 2. Word Organization In Memory

ADDRESS REGISTERS. Each address register and the stack pointer is 32 bits wide and holds a full 32-bit address. Address registers do not support byte sized operands. Therefore, when an address register is used as a source operand, either the low order word or the entire long word operand is used depending upon the operation size. When an address register is used as the destination operand, the entire register is affected regardless of the operation size. If the operation size is word, any other operands are sign extended to 32 bits before the operation is performed.

DATA ORGANIZATION IN MEMORY

Bytes are individually addressable with the high order byte having an even address the same as the word, as shown in Figure 2. The low order byte has an odd address that is one higher than the word address. Instructions and multi-byte data are accessed only on word (even byte) boundaries. If a long word datum is located at address n (n even), then the second word of that datum is located at address n + 2.

The data types supported by the R68000 are: bit data, integer data of 8, 16, or 32 bits, 32-bit addresses and binary coded decimal data. Each of these data types is put in memory, as shown in Figure 3. The numbers indicate the order in which data is accessed from the processor.

BUS OPERATION

The following paragraphs explain control signal and bus operation during data transfer operations, bus arbitration, bus error and halt conditions, and reset operation.

DATA TRANSFER OPERATIONS. Transfer of data between devices involves the following signals:

- Address Bus A1 through A23
- Data Bus D0 through D15
- Control Signals

The address and data buses are separate parallel buses which transfer data using an asynchronous bus structure. In all cycles, the bus master assumes responsibility for deskewing all signals it issues at both the start and end of a cycle. In addition, the bus master is responsible for deskewing the acknowledge and data signals from the slave device.

The following paragraphs explain the read, write, and read-modify-write cycles. The indivisible read-modify-write cycle is the method used by the R68000 for interlocked multiprocessor communications.

Read Cycle. During a read cycle, the processor receives data from memory or a peripheral device. The processor reads bytes of data in all cases, and for a word (or double word) operation, the processor reads both upper and lower bytes simultaneously by asserting both upper and lower data strobes. When the instruction specifies byte operation, the processor uses an internal AO bit to determine which byte to read and then issues the data strobe required for that byte. When the AO bit equals zero, the upper data strobe is issued, and when the AO bit equals one, the lower data strobe is issued. The processor correctly positions the received data internally.

A word read cycle flow chart is given in Figure 4. A byte read cycle flow chart is given in Figure 5. Read cycle timing is given in Figure 6. Figure 7 details word and byte read cycle operations.

Write Cycle. During a write cycle, the processor sends bytes of data to memory or a peripheral device. If the instruction specifies a word operation, the processor writes both bytes. When the instruction specifies a byte operation, the processor uses an internal AO bit to determine which byte to write and then issues the data strobe required for that byte. When the AO bit equals zero, the upper data strobe is issued and when the AO bit equals one, the lower data strobe is issued. A word write cycle flow chart is given in Figure 8. A byte write cycle flow chart is given in Figure 9. Write cycle timing is given in Figure 6. Figure 10 details word and byte write cycle operation.

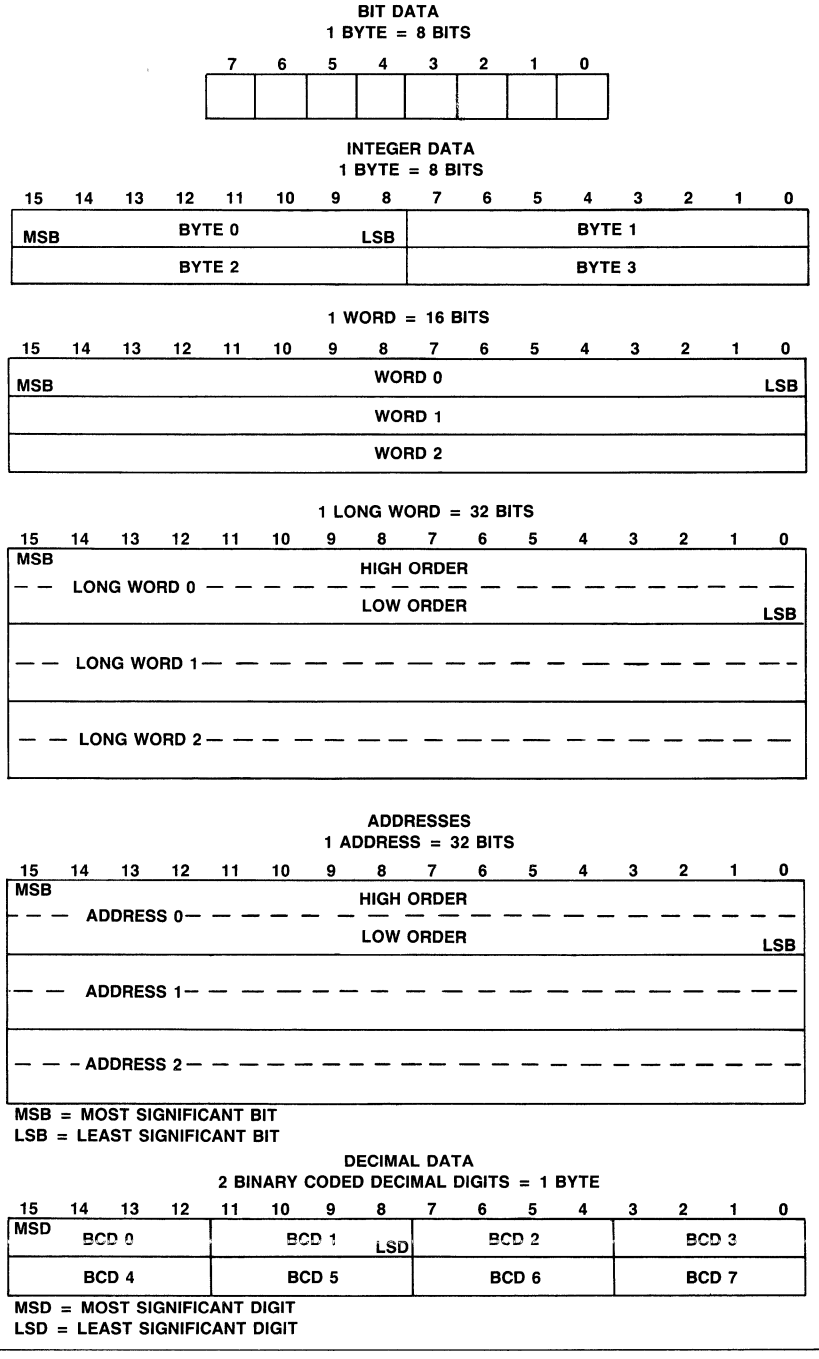


Figure 3. Data Organization In Memory

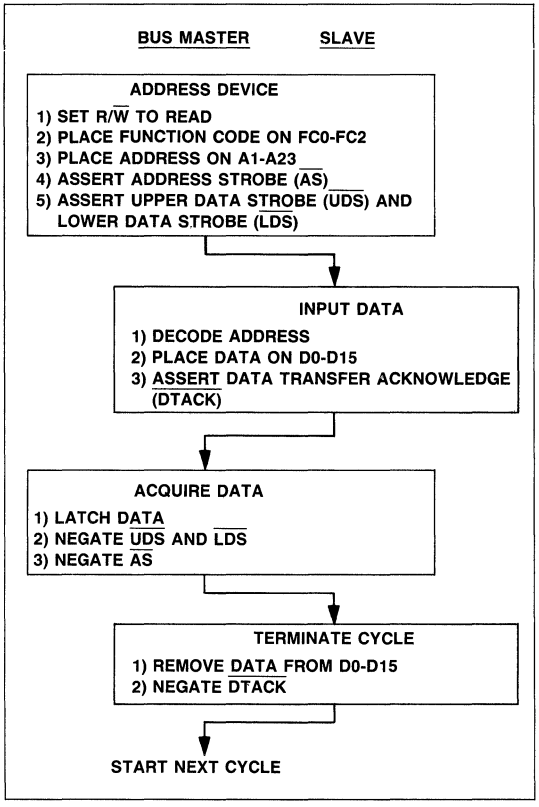


Figure 4. Word Read Cycle Flow Chart

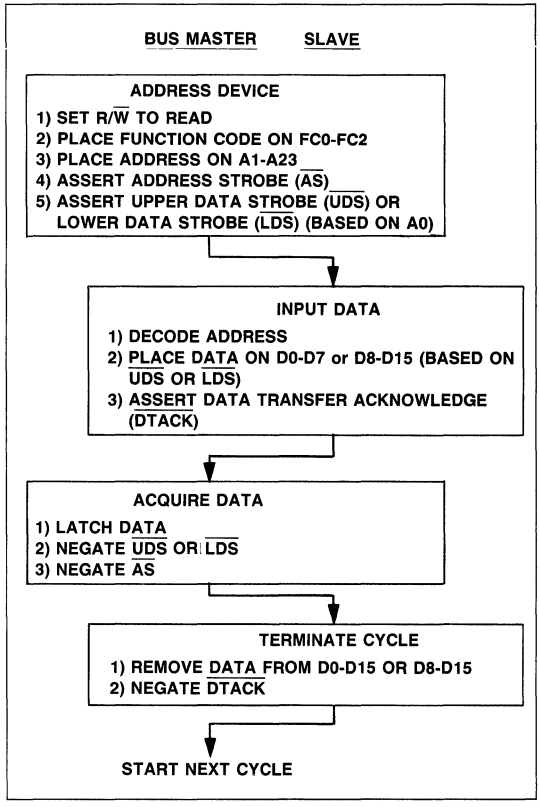


Figure 5. Byte Read Cycle Flow Chart

Read-Modify-Write Cycle. The read-modify-write cycle performs a read, modifies the data in the arithmetic-logic unit, and writes the data back to the same address. In the R68000 this cycle is indivisible in that the address strobe is asserted throughout the entire cycle. The test and set (TAS) instruction uses this cycle to provide meaningful communication between processors in a multiple processor environment. TAS is the only instruction that uses the read-modify-write cycles. Since the test and set instruction only operates on bytes, all read-modify-write cycles are byte operations. A read-modify-write cycle flow chart is given in Figure 11 and a timing diagram is given in Figure 12.

BUS ARBITRATION. Bus arbitration is a technique used by master-type devices to request, be granted, and knowledge bus mastership. In its simplest form, it consists of:

1. asserting a bus mastership request,
2. receiving a grant that the bus is available at the end of the current cycle, and
3. acknowledging that mastership has been assumed.

Figure 13 is a flow chart showing the detail involved in a request from a single device. Figure 14 is a timing diagram for the same operation. This technique allows processing of bus requests during data transfer cycles.

The timing diagram shows that the bus request is negated at the time that an acknowledge is asserted. This is true for a system consisting of the processor and one device capable of bus mastership. However, in systems having a number of devices capable of bus mastership, the bus request line from each device is ORed to the processor. In this system, it is easy to see that there could be more than one bus request being made. The timing diagram shows that the bus grant signals negate a few clock cycles after the transition of the acknowledge (BGACK) signal.

However, if the bus requests are still pending, the processor will assert another bus grant within a few clock cycles after negation. This additional assertion of bus grant allows external arbitration circuitry to select the next bus master before the current bus master has completed its requirements. The following paragraphs provide additional information about the three steps in the arbitration process.

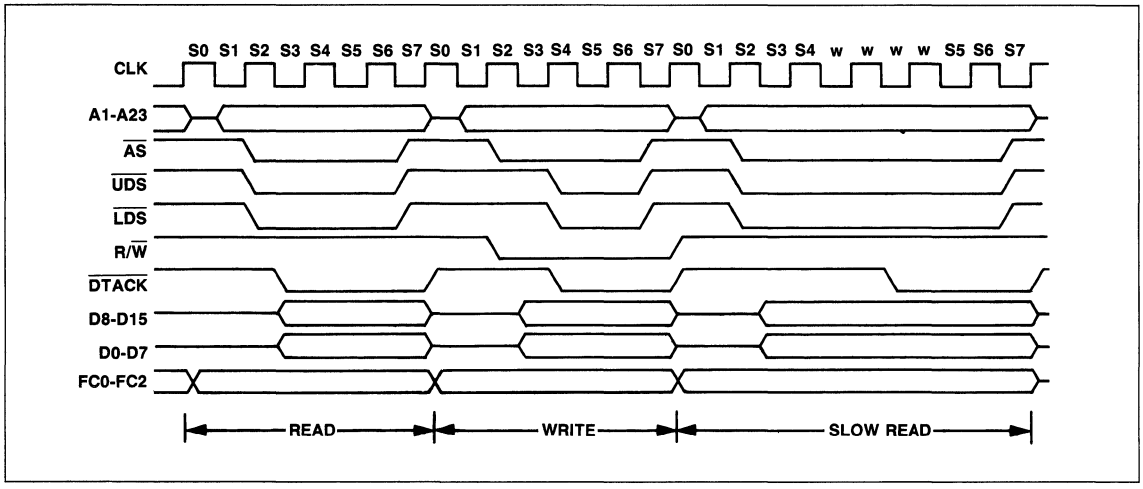


Figure 6. Read and Write Cycle Timing Diagram

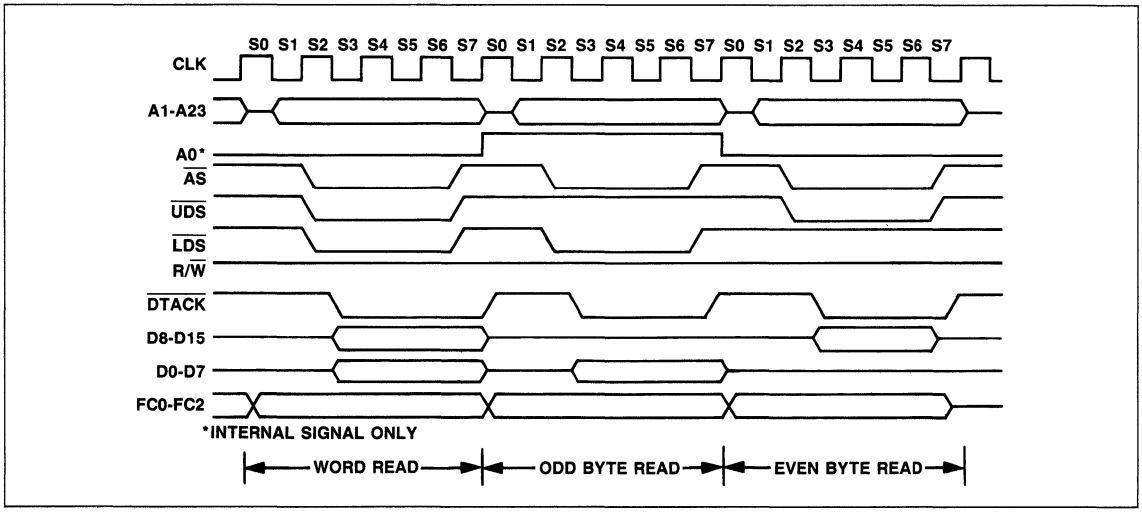


Figure 7. Word and Byte Read Cycle Timing Diagram

Requesting the Bus. External devices capable of becoming bus masters request the bus by asserting the bus request ($\overline{BR}$) signal. This ORed signal (although it need not be constructed from open collector devices) indicates to the processor that some external device requires control of the external bus. The processor, at a lower bus priority level than the external device, will relinquish the bus after it has completed the last bus cycle it has started. If no acknowledge is received before the bus request signal goes inactive, the processor will continue processing when it detects that the bus request is inactive. This allows ordinary processing to continue if the arbitration circuitry inadvertently responded to noise.

Receiving the Bus Grant. Normally the processor asserts bus grant ($\overline{BG}$) as soon as possible after internal synchronization. The only exception occurs when the processor has made an internal decision to execute the next bus cycle but has not progressed far enough into the cycle to have asserted the address strobe ($\overline{AS}$) signal. In this case, bus grant will not be asserted until one clock after address strobe is asserted to indicate to external devices that a bus cycle is being executed.

The bus grant signal may be routed through a daisy-chained network or through a specific priority-encoded network. The processor is not affected by the external method of arbitration as long as the protocol is obeyed.

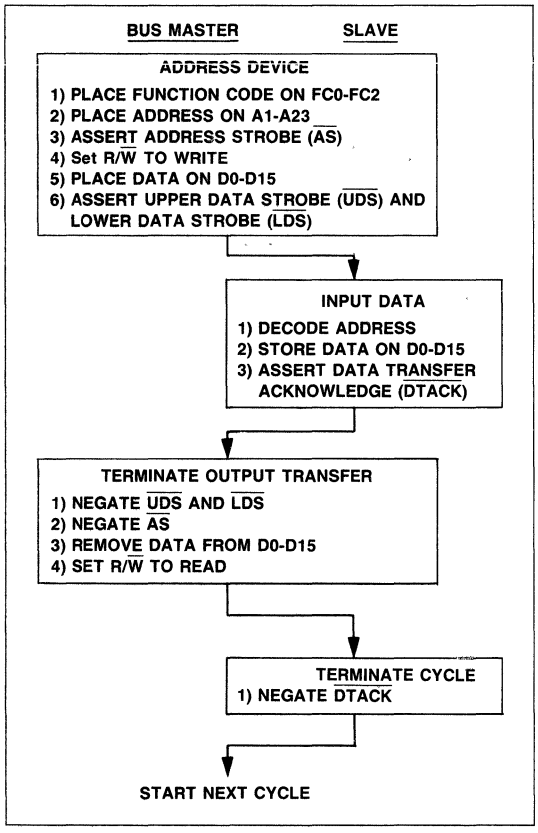


Figure 8. Word Write Cycle Flow Chart

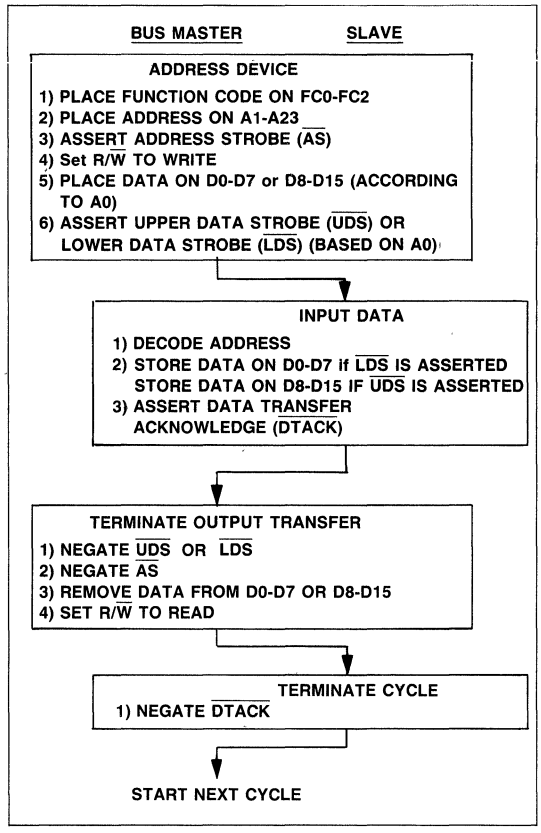


Figure 9. Byte Write Cycle Flow Chart

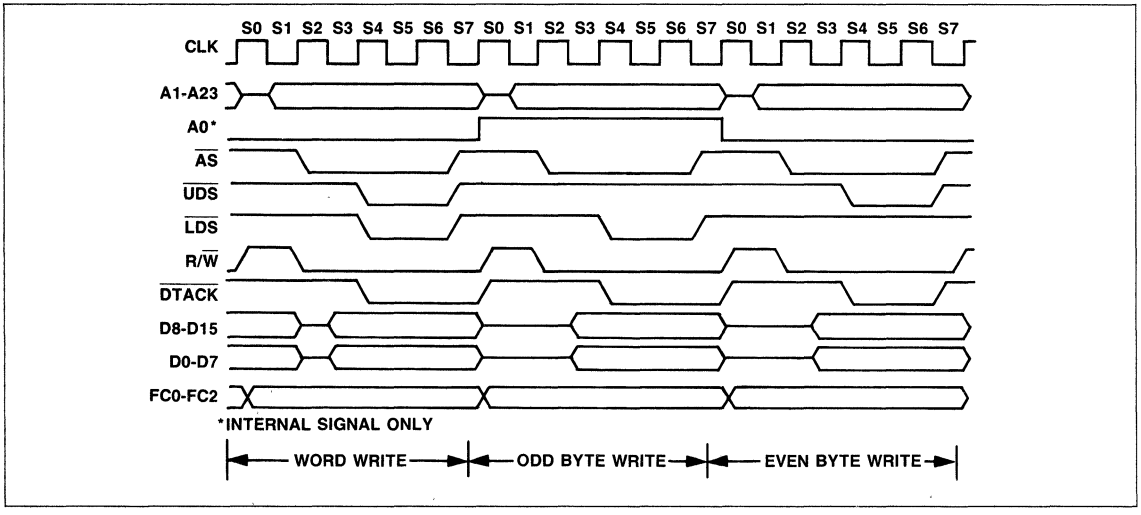


Figure 10. Word and Byte Write Cycle Timing Diagram

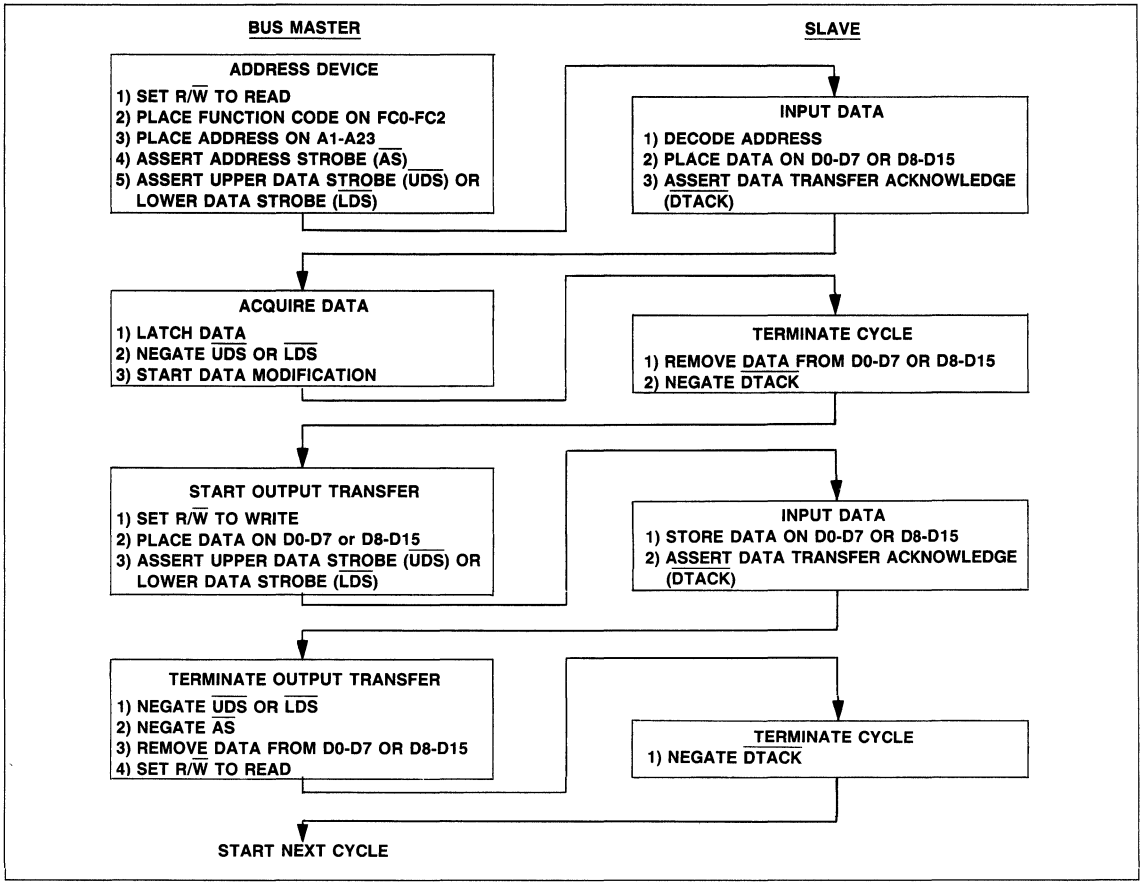


Figure 11. Read-Modify-Write Cycle Flow Chart

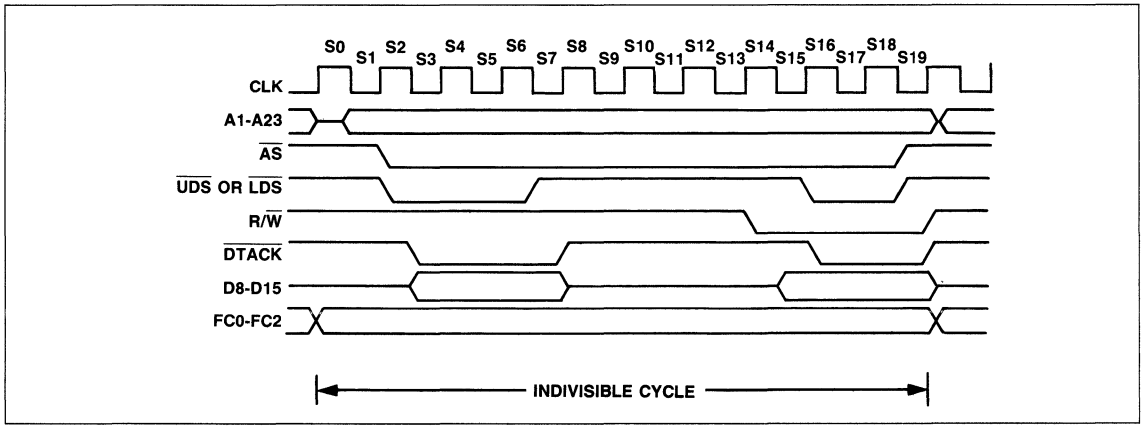


Figure 12. Read-Modify-Write Cycle Timing Diagram

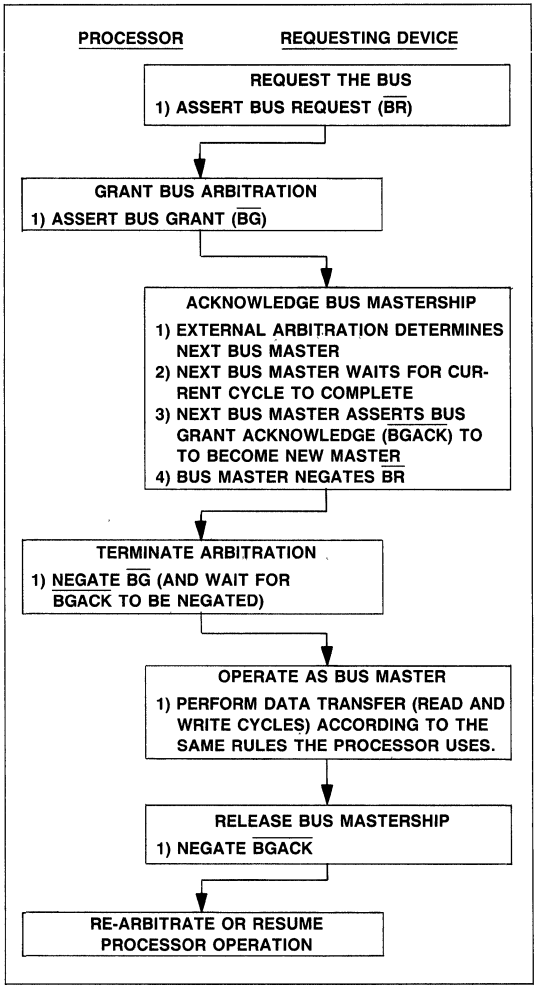


Figure 13. Bus Arbitration Cycle Flow Chart

Acknowledgment of Mastership. Upon receiving a bus grant ($\overline{BG}$), the requesting device waits until address strobe ($\overline{AS}$), data transfer acknowledge ($\overline{DTACK}$), and bus grant acknowledge ($\overline{BGACK}$) are negated before issuing its own $\overline{BGACK}$. The negation of the address strobe indicates that the previous master has completed its cycle, while the negation of bus grant acknowledge indicates that the previous master has released the bus. (If address strobe is asserted no device is allowed to "break into" a cycle.) The negation of data transfer acknowledge indicates the previous slave has terminated its connection to the previous master. In some applications data transfer acknowledge may not be required. In this case the devices would use the address strobe. When bus grant acknowledge is issued the device is bus master. Only after the bus cycle(s) is (are) completed should bus grant acknowledge be negated to terminate bus mastership.

The bus request from the granted device should be dropped after bus grant acknowledge is asserted. If a bus request is still pending, another bus grant will be asserted within a few clocks of the negation of bus grant. Refer to Bus Arbitration Control section. The processor does not perform any external bus cycles before it reasserts bus grant.

BUS ARBITRATION CONTROL. The bus arbitration control unit in the R68000 is implemented with a finite state machine. A state diagram of this machine is shown in Figure 15. All asynchronous signals to the R68000 are synchronized before being used internally. This synchronization is accomplished in a maximum of one cycle of the system clock, assuming that the asynchronous input setup time (#47) has been met (see Figure 16). The input signal is sampled on the falling edge of the clock and is valid internally after the next falling edge. If $\overline{BR}$ and $\overline{BGACK}$ meet the asynchronous set-up time tASI (#47), then tBGKBR (#37A) can be ignored. If $\overline{BR}$ and $\overline{BGACK}$ are asserted asynchronously with respect to the clock, $\overline{BGACK}$ has to be asserted before $\overline{BR}$ is negated.

As shown in Figure 15, input signals labeled R and A are internally synchronized on the bus request and bus grant acknowledge pins respectively. The bus grant output is labeled G and the internal three-state control signal T. If T is true, the address, data, and control buses are placed in a high-impedance state when $\overline{AS}$ is negated. All signals are shown in positive logic (active high) regardless of their true active voltage level.

State changes (valid outputs) occur on the next rising clock edge after the internal signal is valid.

A timing diagram of the bus arbitration sequence during a processor bus cycle is shown in Figure 17. The bus arbitration sequence while the bus is inactive (i.e., executing internal operations such as a multiply instruction) is shown in Figure 18.

If a bus request ($\overline{BR}$) is made at a time when the MPU has already begun a bus cycle but $\overline{AS}$ has not been asserted (bus state S0), $\overline{BG}$ will not be asserted on the next rising edge. Instead $\overline{BG}$ will be delayed until the second rising edge following its internal assertion. This sequence is shown in Figure 19.

BUS ERROR AND HALT OPERATION. In a bus architecture that requires a handshake from an external device, the possibility exists that the handshake might not occur. Since different systems will require a different maximum response time, a bus error input is provided.

External circuitry must be used to determine the duration between address strobe and data transfer acknowledge before issuing a bus error signal. When a bus error signal is received, the processor has two options: initiate a bus error exception sequence or try running the bus cycle again.

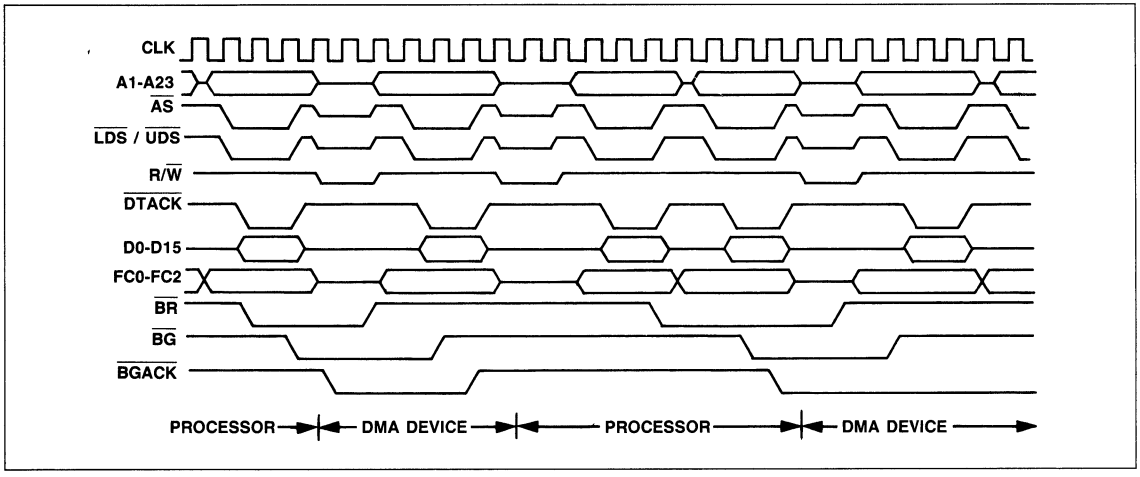
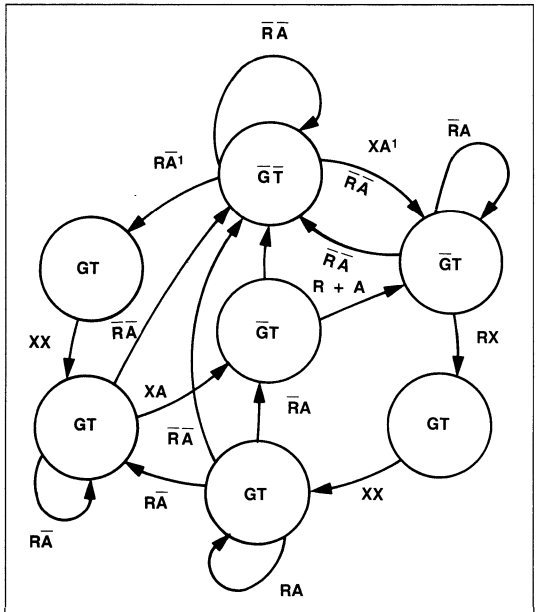


Figure 14. Bus Arbitration Cycle Timing Diagram



R = BUS REQUEST INTERNAL
A = BUS GRANT ACKNOWLEDGE INTERNAL
G = BUS GRANT
T = THREE-STATE CONTROL TO BUS CONTROL LOGIC[2]
X = DON'T CARE

1. STATE MACHINE WILL NOT CHANGE STATE IF BUS IS IN S0 OR S1. REFER TO BUS ARBITRATION CONTROL FOR ADDITIONAL INFORMATION.
2. THE ADDRESS BUS WILL BE PLACED IN THE HIGH IMPEDANCE STATE IF T IS ASSERTED AND AS NEGATED.

Figure 15. State Diagram of R68000 Bus Arbitration Unit

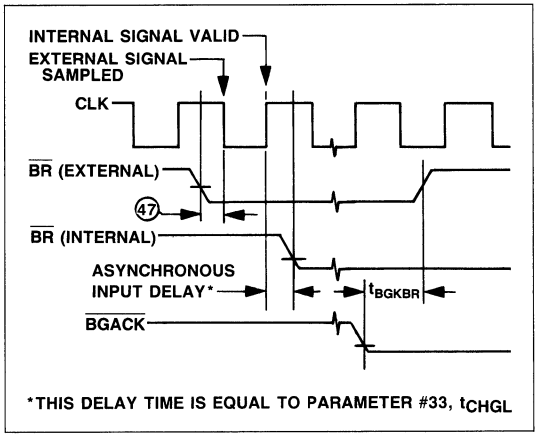


Figure 16. Timing Relationship of External Asynchronous Inputs to Internal Signals

Bus Error Operation. When BERR is asserted, the current bus cycle is terminated. If BERR is asserted before the falling edge of S2, AS will be negated in S7 in either a read or write cycle. As long as BERR remains asserted, the data and address buses will be in the high-impedance state. When BERR is negated, the processor will begin stacking for exception processing. Figure 20 is a timing diagram for the exception sequence. The sequence is composed of the following elements:

1. stacking the program counter and status register,
2. stacking the error information,
3. reading the bus error vector table entry, and
4. executing the bus error handler routine.

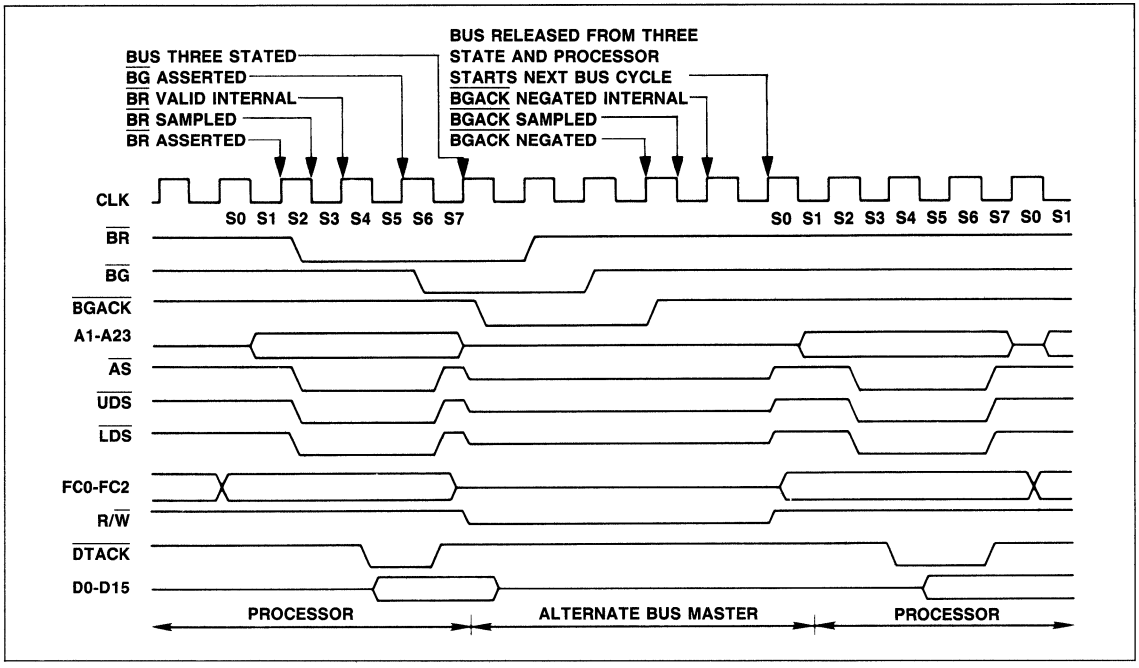


Figure 17. Bus Arbitration During Processor Bus Cycle

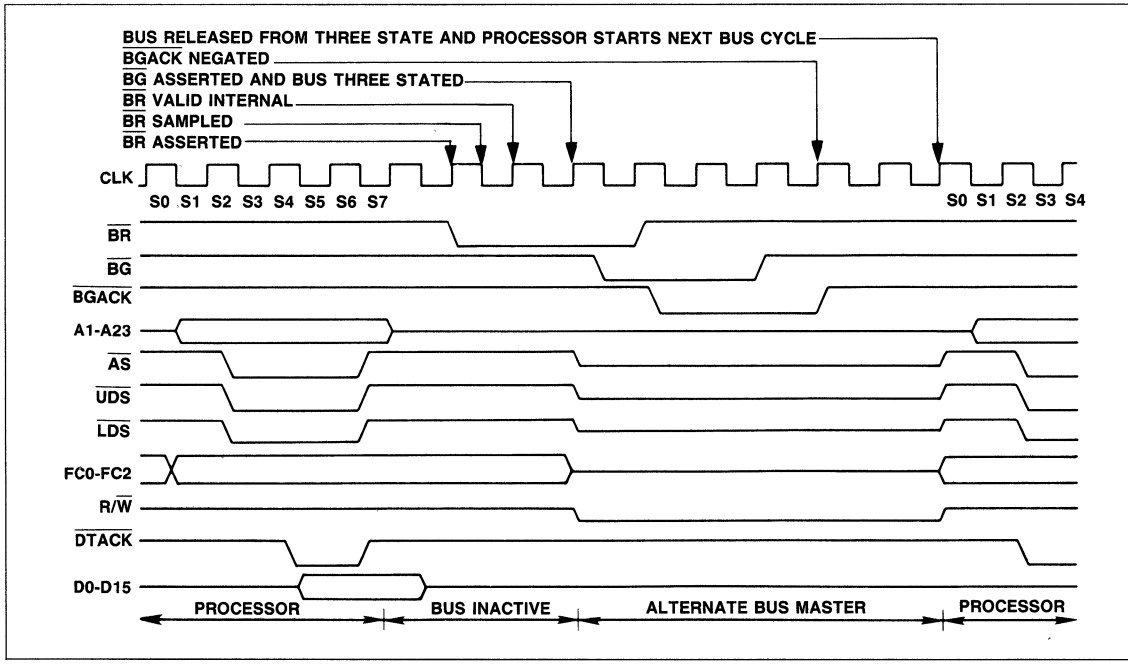


Figure 18. Bus Arbitration with Bus Inactive

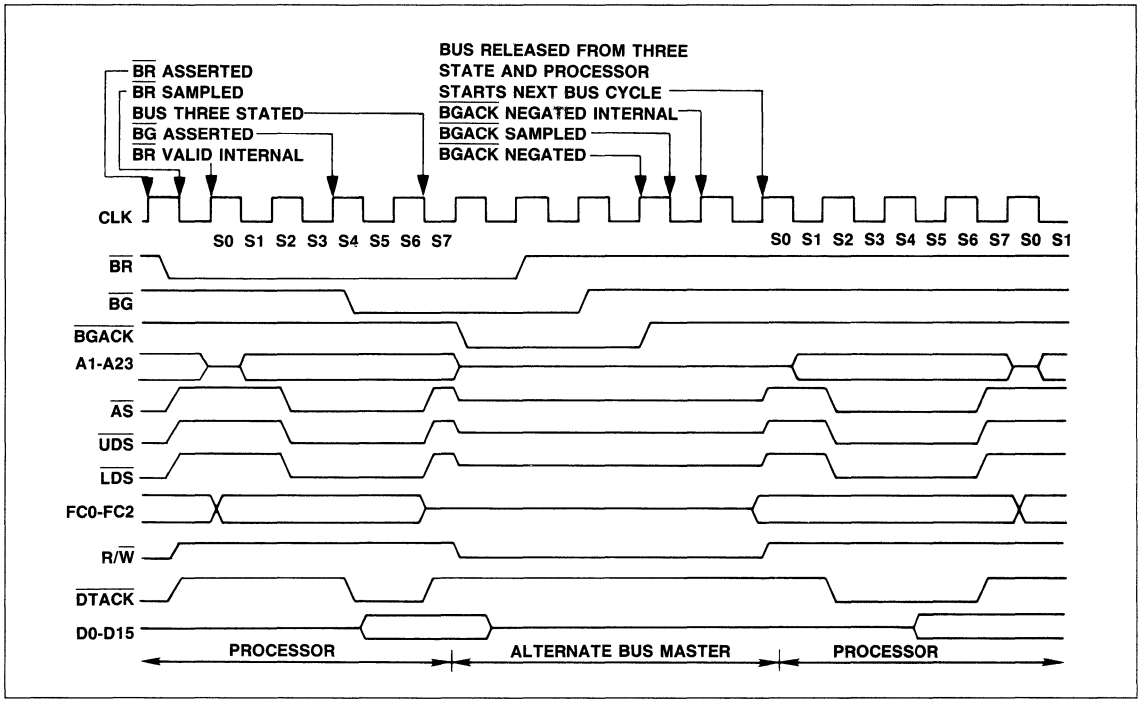


Figure 19. Bus Arbitration During Processor Bus Cycle Special Case

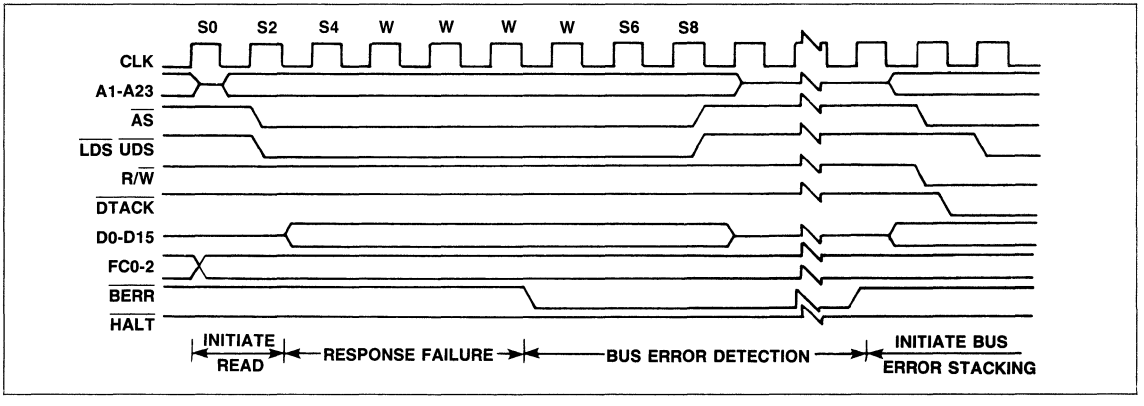


Figure 20. Bus Error Timing Diagram

The stacking of the program counter and the status register is identical to the interrupt sequence. Several additional items are stacked when a bus error occurs. These items are used to determine the nature of the error and correct it, if possible. The bus error vector is vector number two located at address $000008. The processor loads the new program counter from this location. A software bus error handler routine is then executed by the processor. Refer to EXCEPTION PROCESSING for additional information.

Re-Running the Bus Cycle. When, during a bus cycle, the processor receives a $\overline{BERR}$, and $\overline{HALT}$ is being driven by an external device, the processor enters the re-run sequence. Figure 21 is a timing diagram for re-running the bus cycle.

The processor terminates the bus cycle, then puts the address and data output lines in the high-impedance state. The processor remains "halted" and will not run another bus cycle until external logic negates $\overline{HALT}$. Then the processor will re-run the previous bus cycle using the same address, the same function codes, the same data (for a write operation), and the same controls. $\overline{BERR}$ should be negated at least one clock cycle before $\overline{HALT}$ is negated.

Note

The processor will not re-run a read-modify-write cycle. This restriction is made to guarantee that the entire cycle runs correctly and that the write operation of a Test-and-Set operation is performed without ever releasing $\overline{AS}$. If $\overline{BERR}$ and $\overline{HALT}$ are asserted during a read-modify-write bus cycle, a bus error operation results.

Halt Operation with No Bus Error. The $\overline{HALT}$ input signal to the R68000 performs a Halt/Run/Single-Step function in a similar fashion to the R6500 halt functions. When the $\overline{HALT}$ signal is constantly active the processor "halts" (does nothing) and when the $\overline{HALT}$ signal is constantly inactive the processor "runs" (does something).

The single-step mode, derived from correctly timed transitions on the $\overline{HALT}$ signal input, forces the processor to execute a single bus-cycle by entering the "run" mode until the processor starts a bus cycle then changing to the "halt" mode. Thus, the single-step mode allows the user to proceed through (and therefore debug) processor operations one bus cycle at a time.

Figure 22 details the timing required for correct single-step operations. Some care must be exercised to avoid harmful interactions between $\overline{BERR}$ and $\overline{HALT}$ when using the single cycle mode as a debugging tool. This is also true of interactions between the $\overline{HALT}$ and $\overline{RESET}$ lines since these can reset the machine.

When the processor completes a bus cycle after recognizing that $\overline{HALT}$ is active, most three-state signals are put in the high-impedance state. These include:

1. address lines, and
2. data lines.

This is required for correct performance of the re-run bus cycle operation.

Honoring the halt request has no effect on bus arbitration. Only the bus arbitration function removes the control signals from the bus.

Total debugging flexibility is derived from the software debugging package, the halt function, and the hardware trace capability. These processor capabilities allow the hardware debugger to trace single bus cycles or single instructions at a time.

Double Bus Faults. When a bus error exception occurs, the processor will attempt to stack several words containing information about the state of the machine. If a bus error exception occurs during the stacking operation, there have been two bus errors in a row, or a double bus fault. A double bus fault causes the processor to halt. Once a bus error exception has occurred, any bus error exception occurring before the execution of the next instruction constitutes a double bus fault.

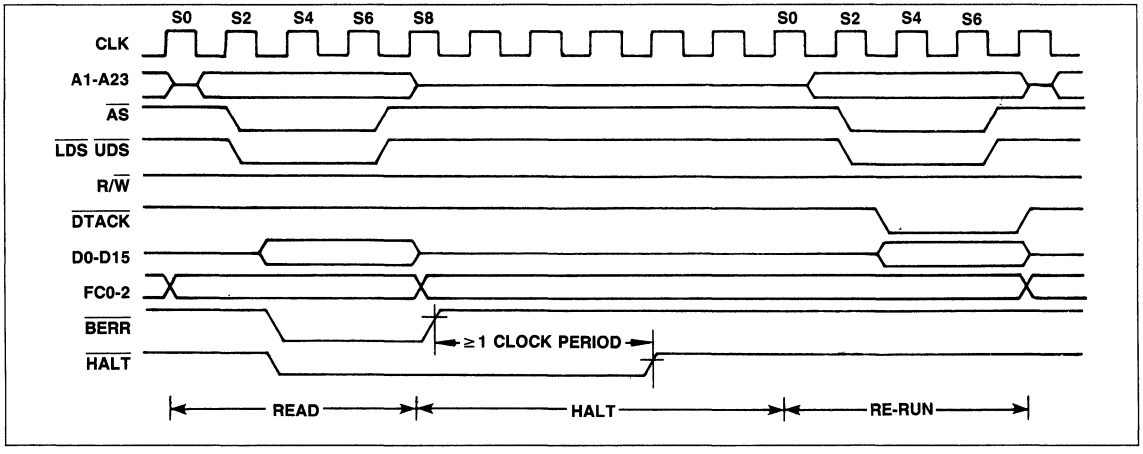


Figure 21. Re-Run Bus Cycle Timing Diagram

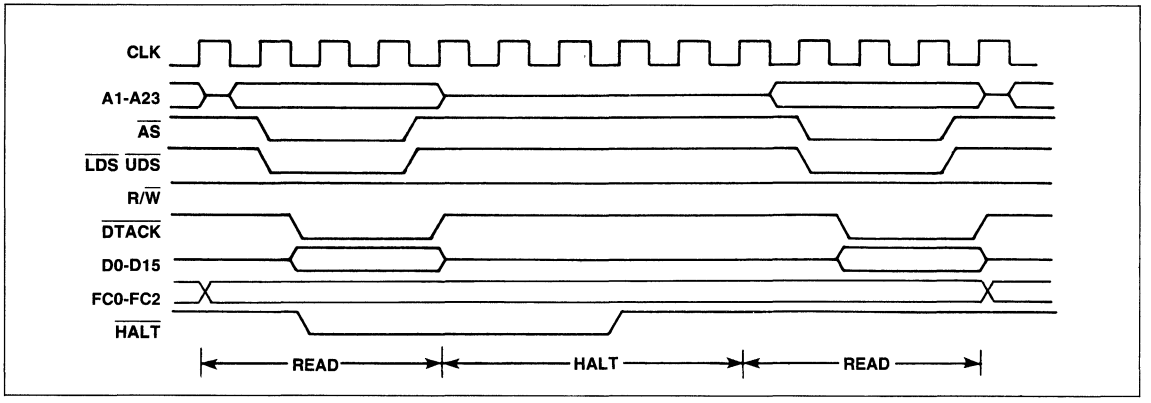


Figure 22. Halt Signal Timing Waveforms

Note that a bus cycle which is re-run does not constitute a bus error exception, and does not contribute to a double bus fault. This means that as long as the external hardware requests it, the processor will continue to re-run the same bus cycle.

The bus error ($\overline{BERR}$) pin also has an effect on processor operation after the processor receives an external reset input. The processor reads the vector table after a reset to determine the address to start program execution. If a bus error occurs while reading the vector table (or at any time before the first instruction is executed), the processor reacts as if a double bus fault has occurred and it halts. Only an external reset will start a halted processor.

RESET OPERATION. The reset signal is a bidirectional signal that allows either the processor or an external signal to reset the system. Figure 23 is a timing diagram for reset operations. Both $\overline{HALT}$ and $\overline{RESET}$ must be applied to ensure total reset of the processor.

When the $\overline{RESET}$ and $\overline{HALT}$ are driven by an external device the entire system, including the processor, is reset. The processor responds by reading the reset vector table entry (vector number zero, address $000000) and loads it into the supervisor stack pointer (SSP). Vector table entry number one at address $000004 is read next and loaded into the program counter. The processor initializes the status register to an interrupt level of seven, with no other register being affected.

Execution of the RESET instruction drives the reset pin low for 124 clock periods. In this case, the processor is trying to reset the rest of the system. The internal state of the processor, including the processor's internal registers and the status register, is unaffected by the execution of a RESET instruction. All external devices connected to the reset line will be reset at the completion of the RESET instruction.

Asserting $\overline{RESET}$ and $\overline{HALT}$ for 10 clock cycles will cause a processor reset, except when Vcc is initially applied to the processor. In this case, an external reset must be applied for 100 milliseconds.

THE RELATIONSHIP OF $\overline{DTACK}$, $\overline{BERR}$, AND $\overline{HALT}$

In order to properly control termination of a bus cycle for a re-run or a bus error condition, $\overline{DTACK}$, $\overline{BERR}$, and $\overline{HALT}$ should be asserted and negated on the rising edge of R68000 clock. This will assure that when two signals are asserted simultaneously, the required setup time (#47) for both of them will be met during the same bus state.

This, or some equivalent precaution, should be designed external to the R68000. Parameter #48 is intended to ensure this operation in a totally asynchronous system, and may be ignored if the above conditions are met.

The preferred bus cycle terminations may be summarized as follows (case numbers refer to Table 4):

Normal Termination: $\overline{DTACK}$ occurs first (case 1).

Halt Termination: $\overline{HALT}$ is asserted at same time, or precedes $\overline{DTACK}$ (no $\overline{BERR}$) cases 2 and 3.

Bus Error Termination: $\overline{BERR}$ is asserted in lieu of, at same time, or preceding $\overline{DTACK}$ (case 4); $\overline{BERR}$ negated at same time, or after $\overline{DTACK}$.

Re-Run Termination: $\overline{HALT}$ and $\overline{BERR}$ asserted in lieu of, at the same time, or before $\overline{DTACK}$ (cases 6 and 7); $\overline{HALT}$ must be negated at least one cycle after $\overline{BERR}$. (Case 5 indicates $\overline{BERR}$ may precede $\overline{HALT}$ which allows fully asynchronous assertion).

Table 4 details the resulting bus cycle termination under various combinations of control signal sequences. The negation of these same control signals under several conditions is shown in Table 5. ($\overline{DTACK}$ is assumed to be negated normally in all cases; for best results, both $\overline{DTACK}$ and $\overline{BERR}$ should be negated when address strobe is negated).

Example A: A system uses a watch-dog timer to terminate accesses to unpopulated address space. The timer asserts $\overline{DTACK}$ and $\overline{BERR}$ simultaneously after timeout (case 4).

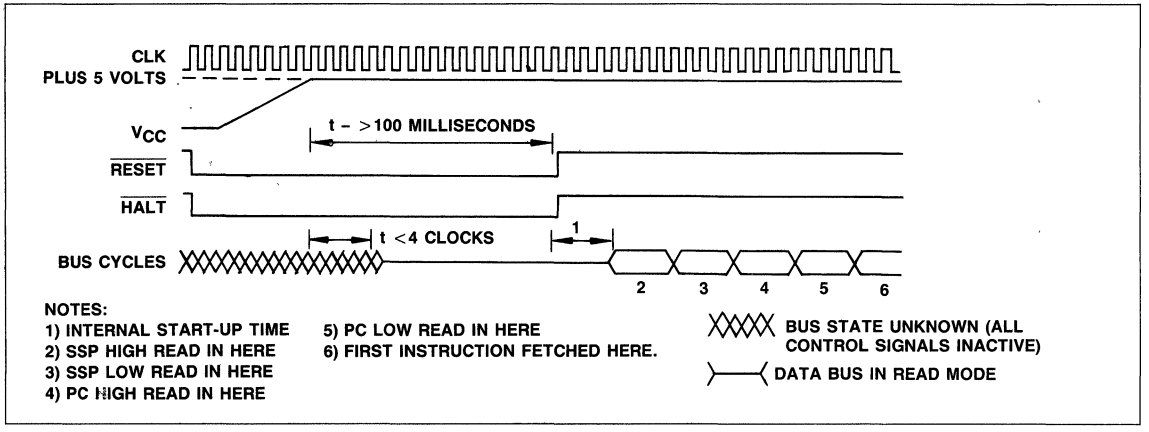


Figure 23. Reset Operation Timing Diagram

Example B: A system uses error detection on RAM contents. Designer may (a) delay DTACK until data verified, and return BERR and HALT simultaneously to re-run error cycle (case 6), or if valid, return DTACK (case 1); (b) delay DTACK until data verified and return BERR at same time as DTACK if data in error (case 4).

ASYNCHRONOUS VERSUS SYNCHRONOUS OPERATION

Asynchronous Operation

To achieve clock frequency independence at a system level, the R68000 can be used in an asynchronous manner. This entails using only the bus handshake lines (AS, UDS, LDS, DTACK, BERR, HALT, and VPA) to control the data transfer. Using this method, AS signals the start of a bus cycle and the data strobes are used as a condition for valid data on a write cycle. The slave device (memory or peripheral) then responds by placing the requested data on the data bus for a read cycle or latching data on a write cycle and asserting the data transfer acknowledge signal (DTACK) to terminate the bus cycle. If no slave reponds or the access is invalid, external control logic asserts the BERR, or BERR and HALT, signal to abort or rerun the bus cycle.

The DTACK signal is allowed to be asserted before the data from a slave device is valid on a read cycle. The length of time that DTACK may precede data is given as parameter #31 (See Figure 45) and it must be met in any asynchronous system to insure that valid data is latched into the processor. Notice that there is no maximum time specified from the assertion of AS to the assertion of DTACK. This is because the MPU will insert wait cycles of one clock period each until DTACK is recognized.

The BERR signal is allowed to be asserted after the DTACK signal is asserted. BERR must be asserted within the time given as parameter #48 after DTACK is asserted in any asynchronous system to insure proper operation. If this maximum delay time is violated, the processor may exhibit erratic behavior.

Synchronous Operation

To allow for those systems which use the system clock as a signal to generate DTACK and other asynchronous inputs, the asynchronous inputs setup time is given as parameter #47. If this setup is met on an input, such as DTACK, the processor is guaranteed to recognize that signal on the next falling edge of the system clock. However, the converse is not true—if the input signal does not meet the setup time it is not guaranteed not to be recognized. In addition, if DTACK is recognized on a falling edge, valid data will be latched into the processor (on a read cycle) on the next falling edge provided that the data meets the setup time given as parameter #27. Given this, parameter #31 may be ignored. Note that if DTACK is asserted, with the required setup time, before the falling edge of S4, no wait states will be incurred and the bus cycle will run at its maximum speed of four clock periods.

In order to assure proper operation in a synchronous system when BERR is asserted after DTACK, the following conditions must be met. Within one clock cycle after DTACK was recognized, BERR must meet the setup time parameter #27A prior to the falling edge of the next clock. The setup time is critical to proper operation, and the R68000 may exhibit erratic behavior if it is violated.

Note

During an active bus cycle, VPA and BERR are sampled on every falling edge of the clock starting with S0. DTACK is sampled on every falling edge of the clock starting with S4 and data is latched on the falling edge of S6 during a read. The bus cycle will then be terminated in S7 except when BERR is asserted in the absence of DTACK, in which case it will terminate one clock cycle later in S9.

Table 4. $\overline{\text{DTACK}}$, $\overline{\text{BERR}}$, $\overline{\text{HALT}}$ Assertion Results

Case No.	Control Signal	Asserted on Rising Edge of State		Result
		N	N + 2	
1	$\overline{\text{DTACK}}$ $\overline{\text{BERR}}$ $\overline{\text{HALT}}$	A NA NA	S X X	Normal cycle terminate and continue.
2	$\overline{\text{DTACK}}$ $\overline{\text{BERR}}$ $\overline{\text{HALT}}$	A NA A	S X S	Normal cycle terminate and halt Continue when $\overline{\text{HALT}}$ removed.
3	$\overline{\text{DTACK}}$ $\overline{\text{BERR}}$ $\overline{\text{HALT}}$	NA NA A	A NA S	Normal cycle terminate and halt Continue when $\overline{\text{HALT}}$ removed
4	$\overline{\text{DTACK}}$ $\overline{\text{BERR}}$ $\overline{\text{HALT}}$	X A NA	X S NA	Terminate and take bus error trap
5	$\overline{\text{DTACK}}$ $\overline{\text{BERR}}$ $\overline{\text{HALT}}$	NA A NA	X S A	Terminate and re-run
6	$\overline{\text{DTACK}}$ $\overline{\text{BERR}}$ $\overline{\text{HALT}}$	X A A	X S S	Terminate and re-run when $\overline{\text{HALT}}$ removed
7	$\overline{\text{DTACK}}$ $\overline{\text{BERR}}$ $\overline{\text{HALT}}$	NA NA A	X A S	Terminate and re-run when $\overline{\text{HALT}}$ removed

Legend.
N — the number of the current even bus state (e g., S4, S6, etc.)
A — signal is asserted in this bus state
NA — signal is not asserted in this state
X — don't care
S — signal was asserted in previous state and remains asserted in this state

Table 5. $\overline{\text{BERR}}$ AND $\overline{\text{HALT}}$ Negation Results

Conditions of Termination in Table 4-4	Control Signal	Negated on Rising Edge of State			Results — Next Cycle
		N		N + 2	
Bus Error	$\overline{\text{BERR}}$ $\overline{\text{HALT}}$	● ●	or or	● ●	Takes bus error trap.
Re-run	$\overline{\text{BERR}}$ $\overline{\text{HALT}}$	● ●	or	●	Illegal sequence; usually traps to vector number 0
Re-run	$\overline{\text{BERR}}$ $\overline{\text{HALT}}$	●		●	Re-runs the bus cycle.
Normal	$\overline{\text{BERR}}$ $\overline{\text{HALT}}$	● ●	or	●	May lengthen next cycle.
Normal	$\overline{\text{BERR}}$ $\overline{\text{HALT}}$	●	or	● none	If next cycle is started it will be terminated as a bus error.

● = Signal is negated in this bus state

PROCESSING STATES

The following paragraphs describe the actions of the R68000 which are outside the normal processing associated with the execution of instructions. The functions of the bits in the supervisor portion of the status register are covered: the supervisor/user bit, the trace enable bit, and the processor interrupt priority mask. The sequence of memory references and actions taken by the processor on exception conditions are detailed.

The R68000 is always in one of three processing states: normal, exception, or halted. The normal processing state associated with instruction execution; the memory references are to fetch instructions and operands, and to store results. A special case of the normal state is the stopped state which the processor enters when a STOP instruction is executed. In this state, no further references are made.

The exception processing state is associated with interrupts, trap instructions, tracing and other exceptional conditions. The exception may be internally generated by an instruction or by an unusual condition arising during the execution of an instruction. Externally, exception processing can be forced by an interrupt, by a bus error, or by a reset. Exception processing is designed to provide an efficient context switch so that the processor may handle unusual conditions.

The halted processing state is an indication of a catastrophic hardware failure. For example, if during the exception processing of a bus error another bus error occurs, the processor assumes that the system is unusable and halts. Only an external reset can restart a halted processor. Note that a processor in the stopped state is not in the halted state, nor vice versa.

PRIVILEGE STATES

The processor operates in one of two states of privilege: the "user" state or the "supervisor" state. The privilege state determines legal operations. It is used to choose between the supervisor stack pointer and the user stack pointer in instruction references, and by the external memory management device to control and translate accesses.

The privilege state is a mechanism for providing security in a computer system by allowing most programs to execute in user state. In this state, the accesses are controlled, and the effects on other parts of the system are limited. Programs should access only their own code and data areas, and ought to be restricted from accessing information.

The operating system which executes in the supervisor state, has access to all resources and performs the overhead tasks for the user state programs.

SUPERVISOR STATE. The supervisor state is the higher state of privilege. For instruction execution, the supervisor state is determined by asserting (high) the S-bit of the status register. All instructions can be executed in the supervisor state. The bus cycles generated by instructions executed in the supervisor state are classified as supervisor references. While the processor is in the supervisor privilege state, those instructions which use either the system stack pointer implicitly or address register seven explicitly access the supervisor stack pointer.

All exception processing is done in the supervisor state, regardless of the setting of the S-bit. The bus cycles generated during exception processing are classified as supervisor references. All stacking operations during exception processing use the supervisor stack pointer.

USER STATE. The user state is the lower state of privilege. For instruction execution, the user state is determined by negating (low) the S-bit of the status register.

Most instructions execute the same in user state as in the supervisor state. However, some instructions which have important system effects are made privileged. User programs are not permitted to execute the STOP instruction, or the RESET instruction. To ensure that a user program cannot enter the supervisor state except in a controlled manner, the instructions which modify the whole state register are priviled. To aid in debugging programs which are to be used as operating systems, the move to user stack pointer (MOVE to USP) and move from user stack pointer (MOVE from USP) instructions are also privileged.

The bus cycles generated by an instruction executed in user state are classified as user state references. This allows an external memory management device to translate the address and to control access to protected portions of the address space. While the processor is in user privilege state, those instructions which use either the system stack pointer implicitly or address register seven explicitly, access the user stack pointer.

PRIVILEGE STATE CHANGES. Once the processor is in the user state and executing instructions, only exception processing can change the privilege state. During exception processing, the current setting of the S-bit of the status register is saved and the S-bit is asserted, putting the processing in the supervisor state. Therefore, when instruction execution resumes to process the exception, the processor is in the supervisor privilege state.

REFERENCE CLASSIFICATION. When the processor makes a reference, it classifies the kind of reference being made by using the encoding on the three function code output lines. This allows external translation of addresses, control of access, and differentiation of special processor states, such as interrupt acknowledge. Table 6 lists the classification of references.

Table 6. Reference Classification

Function Code Output			
FC2	FC1	FC0	Reference Class
0	0	0	(Unassigned)
0	0	1	User Data
0	1	0	User Program
0	1	1	(Unassigned)
1	0	0	(Unassigned)
1	0	1	Supervisor Data
1	1	0	Supervisor Program
1	1	1	Interrupt Acknowledge

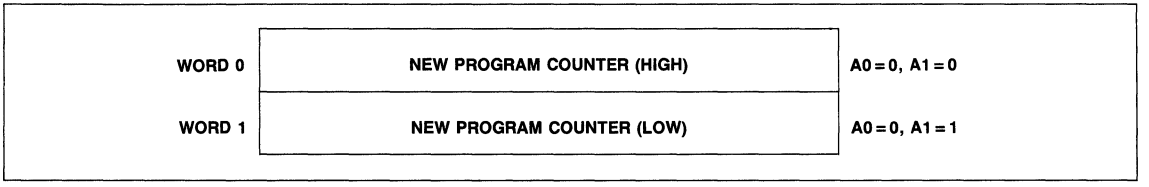


Figure 24. Exception Vector Format

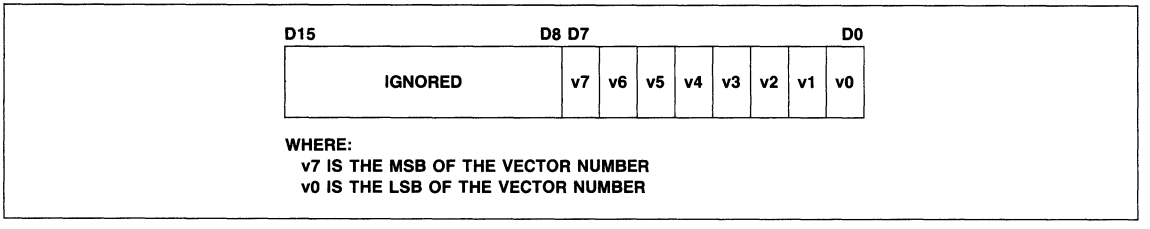


Figure 25. Peripheral Vector Number Format

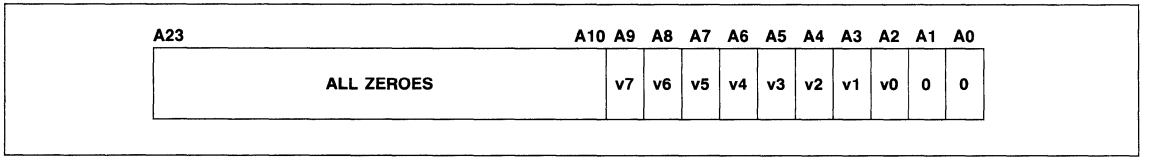


Figure 26. Address Translated From 8-Bit Vector Number

EXCEPTION PROCESSING

Before discussing the details of interrupts, traps, and tracing, a general description of exception processing is in order. The processing of an exception occurs in four steps, with variations for different exception causes. During the first step, a temporary copy of the status register is made, and the status register is set for exception processing. In the second step the exception vector is determined, and the third step is the saving of the current processor contents. In the fourth step a new context is obtained, and the processor switches to instruction processing.

EXCEPTION VECTORS. Exception vectors are memory locations from which the processor fetches the address of a routine which will handle that exception. All exception vectors are two words in length (Figure 24), except for the reset vector, which is four words. All exception vectors lie in the supervisor data space, except for the reset vector which is in the supervisor program space. A vector number is an eight-bit number which, when multipled by four, gives the address of an exception vector. Vector numbers are generated internally or externally, depending on the cause of the exception. In the case of interrupts, during the interrupt acknowledge bus cycle, a peripheral provides an 8-bit vector number (Figure 25) to the processor on data bus lines D0 through D7. The processor translates the vector number into a full 24-bit address, as shown in Figure 26. The memory layout for exception vectors is given in Table 7.

As shown in Table 7, the memory layout is 512 words long (1024 bytes). It starts at address 0 and proceeds through address 1023. This provides 255 unique vectors; some of these are reserved for TRAPS and other system functions. Of the 255, there are 192 reserved for user interrupt vectors. However, there is no protection on the first 64 entries, so user interrupt vectors may overlap at the discretion of the systems designer.

KINDS OF EXCEPTIONS. Exceptions can be generated either internally or externally. Externally generated exceptions include interrupts ($\overline{IRQ}$), bus error ($\overline{BERR}$), and reset ($\overline{RESET}$) requests. Interrupts are requests from peripheral devices for processor action while $\overline{BERR}$ and $\overline{RESET}$ inputs are used for access control and processor restart. Internally generated exceptions come from instructions, from address errors, or from tracing. The trap (TRAP), trap on overflow (TRAPV), check register against bounds (CHK) and divide (DIV) instructions can all generate exceptions as part of their instruction execution. In addition, illegal instructions, word fetches from odd addresses and privilege violations cause exceptions. Tracing behaves like a very high priority, internally generated interrupt after each instruction execution.

EXCEPTION PROCESSING SEQUENCE. Exception processing occurs in four identifiable steps. In the first step, an internal copy is made of the status register. After the copy is made, the S-bit is asserted, putting the processor into the supervisor privilege state. Also, the T-bit is negated which will allow the exception handler to execute unhindered by tracing. For the reset and interrupt exceptions, the interrupt priority mask is also updated.

Table 7. Exception Vector Assignment

Vector Number(s)	Address			Assignment
	Dec	Hex	Space	
0	0	000	SP	Reset: Initial SSP
—	4	004	SP	Reset: Initial PC
2	8	008	SD	Bus Error
3	12	00C	SD	Address Error
4	16	010	SD	Illegal Instruction
5	20	014	SD	Zero Divide
6	24	018	SD	CHK Instruction
7	28	01C	SD	TRAPV Instruction
8	32	020	SD	Privilege Violation
9	36	024	SD	Trace
10	40	028	SD	Line 1010 Emulator
11	44	02C	SD	Line 1111 Emulator
12*	48	030	SD	(Unassigned, reserved)
13*	52	034	SD	(Unassigned, reserved)
14*	56	038	SD	(Unassigned, reserved)
15	60	03C	SD	Uninitialized Interrupt Vector
16-23*	64	04C	SD	(Unassigned, reserved)
	95	05F		—
24	96	060	SD	Spurious Interrupt
25	100	064	SD	Level 1 Interrupt Autovector
26	104	068	SD	Level 2 Interrupt Autovector
27	108	06C	SD	Level 3 Interrupt Autovector
28	112	070	SD	Level 4 Interrupt Autovector
29	116	074	SD	Level 5 Interrupt Autovector
30	120	078	SD	Level 6 Interrupt Autovector
31	124	07C	SD	Level 7 Interrupt Autovector
32-47	128	080	SD	TRAP Instruction Vectors
	191	0BF		—
48-63*	192	0C0	SD	(Unassigned, reserved)
	255	0FF		—
64-255	256	100	SD	User Interrupt Vectors
	1023	3FF		—

*Vector numbers 12, 13, 14, 16 through 23, and 48 through 63 are reserved for future enhancements. No user peripheral devices should be assigned these numbers

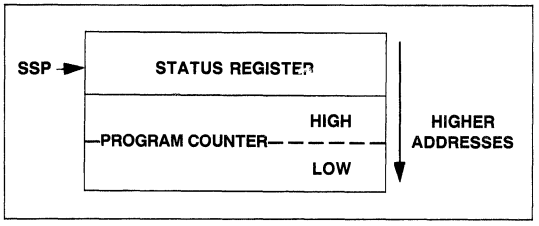


Figure 27. Exception Stack Order (Groups 1 and 2)

In the second step, the vector number of the exception is determined. For interrupts, the vector number is obtained by a processor fetch, classified as an interrupt acknowledge. For all other exceptions, internal logic provides the vector number. This vector number is then used to generate the address of the exception vector.

The third step is to save the current processor status except for the reset exception. The current program counter value and the saved copy of the status register are stacked using the supervisor stack pointer as shown in Figure 27. The program counter value stacked usually points to the next unexecuted instruction; however, for bus error and address error, the value stacked for the program counter is unpredictable, and may be incremented from the address of the instruction which caused the error. Additional information defining the current context is stacked for the bus error and address error exceptions.

The last step is the same for all exceptions. The new program counter value is fetched from the exception vector. The processor then resumes instruction execution. The instruction at the address given in the exception vector is fetched, and normal instruction decoding and execution is started.

MULTIPLE EXCEPTIONS. These paragraphs describe the processing which occurs when multiple exceptions arise simultaneously. Exceptions can be grouped according to their occurrence and priority. The Group 0 exceptions are reset, bus error, and address error. These exceptions cause the instruction currently being executed to be aborted, and the exception processing to commence within two clock cycles. The Group 1 exceptions are trace and interrupt, as well as the privilege violations and illegal instructions. These exceptions allow the current instruction to execute to completion, but preempt the execution of the next instruction by forcing exception processing to occur (privilege violations and illegal instructions are detected when they are the next instruction to be executed). The Group 2 exceptions occur as part of the normal processing of instructions. The TRAP, TRAPV, CHK, and zero divide exceptions are in this group. For these exceptions, the normal execution of an instruction may lead to exception processing.

Group 0 exceptions have highest priority, while Group 2 exceptions have lowest priority. Within Group 0, reset has highest priority, followed by address error and then bus error. Within Group 1, trace has priority over external interrupts, which in turn takes priority over illegal instruction and privilege violation. Since only one instruction can be executed at a time, there is no priority relation within Group 2.

Table 8. Exception Grouping and Priority

Group	Exception	Processing
0	Reset Address Error Bus Error	Exception processing begins within two clock cycles.
1	Trace Interrupt Illegal Instruction Privilege Violation	Exception processing begins before the next instruction.
2	TRAP, TRAPV, CHK, Zero Divide	Exception processing is started by normal instruction execution

The priority relation between two exceptions determines which is taken first if the conditions for both arise simultaneously. Therefore, if a bus error occurs during a TRAP instruction, the bus error takes precedence, and the TRAP instruction processing is aborted. In another example, if an interrupt request occurs during the execution of an instruction while the T-bit is asserted, the trace exception has priority, and is processed first. Before instruction processing resumes, however, the interrupt exception is also processed, and instruction processing commences finally in the interrupt handler routine. Table 8 gives a summary of exception grouping and priority.

EXCEPTION PROCESSING DETAILED DISCUSSION

Exceptions have a number of sources, and each exception has a unique processing sequence. The following paragraphs detail the sources of exceptions, how each arises, and how each is processed.

RESET. The reset input provides the highest exception level. The processing of the reset signal is designed for system initiation, and recovery from catastrophic failure. Any processing in progress at the time of the reset is aborted and cannot be recovered. The processor is forced into the supervisor state and the trace state is forced off. The processor interrupt priority mask is set at level seven. The vector number is internally generated to reference the reset exception vector at location 0 in the supervisor program space. Because no assumptions can be made about the validity of register contents, in particular the supervisor stack pointer, neither the program counter nor the status register is saved. The address contained in the first two words of the reset exception vector is fetched as the initial supervisor stack pointer, and the address in the last two words of the reset exception vector is fetched as the initial program counter. Finally, instruction execution is started at the address in the program counter. The powerup/restart code should be pointed to by the initial program counter.

The RESET instruction does not cause loading of the reset vector, but does assert the reset line to reset external devices. This allows the software to reset the system to a known state and then continue processing with the next instruction.

INTERRUPTS. Seven levels of interrupt priorities are provided. Devices may be chained externally within interrupt priority levels, allowing an unlimited number of peripheral devices to interrupt the processor. Interrupt priority levels are numbered from one to seven, level seven being the highest priority. The status register contains a three-bit mask which indicates the current processor priority. Interrupts are inhibited for all priority levels less than or equal to the current processor priority.

An interrupt request is made to the processor by encoding the interrupt request level on the interrupt request lines; a zero indicates no interrupt request. Interrupt requests arriving at the processor do not face immediate exception processing, but are made pending. Pending interrupts are detected between instruction executions. If the priority of the pending interrupt is lower than or equal to the current processor priority, execution continues with the next instruction and the interrupt exception processing is postponed. (The recognition of level seven is slightly different, as explained in a following paragraph.)

If the priority of the pending interrupt is greater than the current processor priority, the exception processing sequence is started. First a copy of the status register is saved, and the privilege state is set to supervisor, then tracing is suppressed, and the processor priority level is set to the level of the interrupt being acknowledged. The processor fetches the vector number from the interrupting device, classifying the reference as an interrupt acknowledge and displaying the level number of the interrupt being acknowledged on the address bus. If external logic requests an automatic vectoring, the processor internally generates a vector number which is determined by the interrupt level number. If external logic indicates a bus error, the interrupt is taken to be spurious, and the generated vector number references the spurious interrupt vector. The processor then proceeds with the usual exception processing, saving the program counter and status register on the supervisor stack. The saved value of the program counter is the address of the instruction which would have been executed had the interrupt not been present. The content of the interrupt vector whose vector number was previously obtained is fetched and loaded into the program counter, and normal instruction execution commences in the interrupt handling routine. A flow chart for the interrupt acknowledge sequence is given in Figure 28, a timing diagram is given in Figure 29, and the interrupt exception timing sequence is shown in Figure 30.

Priority level seven is a special case. Level seven interrupts cannot be inhibited by the interrupt priority mask, thus providing a "non-maskable interrupt" capability. An interrupt is generated each time the interrupt request level changes from some lower level to level seven. Note that a level seven interrupt may still be caused by the level comparison if the request level is a seven and the processor priority is set to a lower level by an instruction.

UNINITIALIZED INTERRUPT. An interrupting device asserts $\overline{\text{VPA}}$ or provides an interrupt vector during an interrupt acknowledge cycle to the R68000. If the vector register has not been initialized, the responding R68000 Family peripheral will provide vector 15, the uninitialized interrupt vector. This provides a uniform way to recover from a programming error.

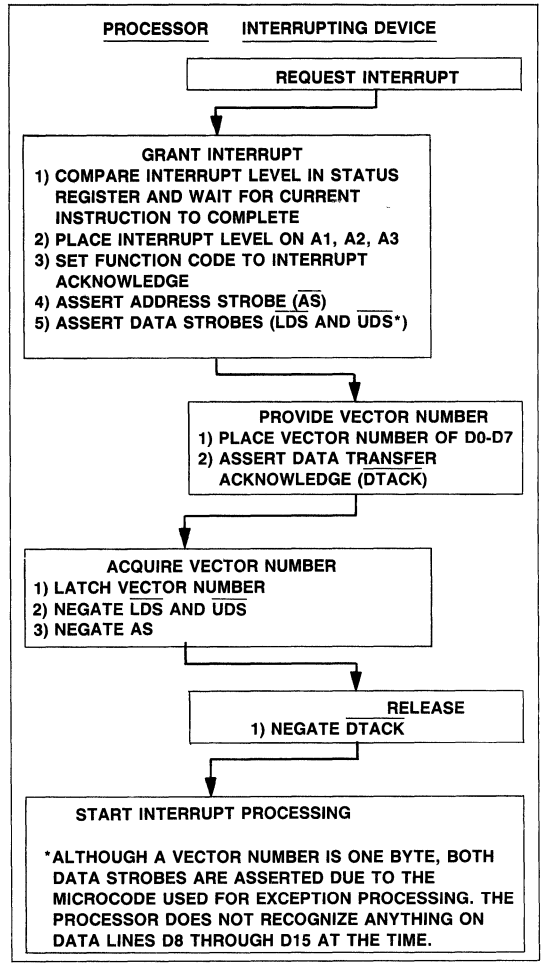


Figure 28. Interrupt Acknowledge Sequence Flow Chart

SPURIOUS INTERRUPT. If during the interrupt acknowledge cycle no device responds by asserting $\overline{\text{DTACK}}$ or $\overline{\text{VPA}}$, the bus error line should be asserted to terminate the vector acquisition. The processor separates the processing of this error from bus error by fetching the spurious interrupt vector instead of the bus error vector. The processor then proceeds with the usual exception processing.

INSTRUCTION TRAPS. Traps are exceptions caused by instructions. They arise either from processor recognition of abnormal conditions during instruction execution, or from use of instructions whose normal behavior is trapping.

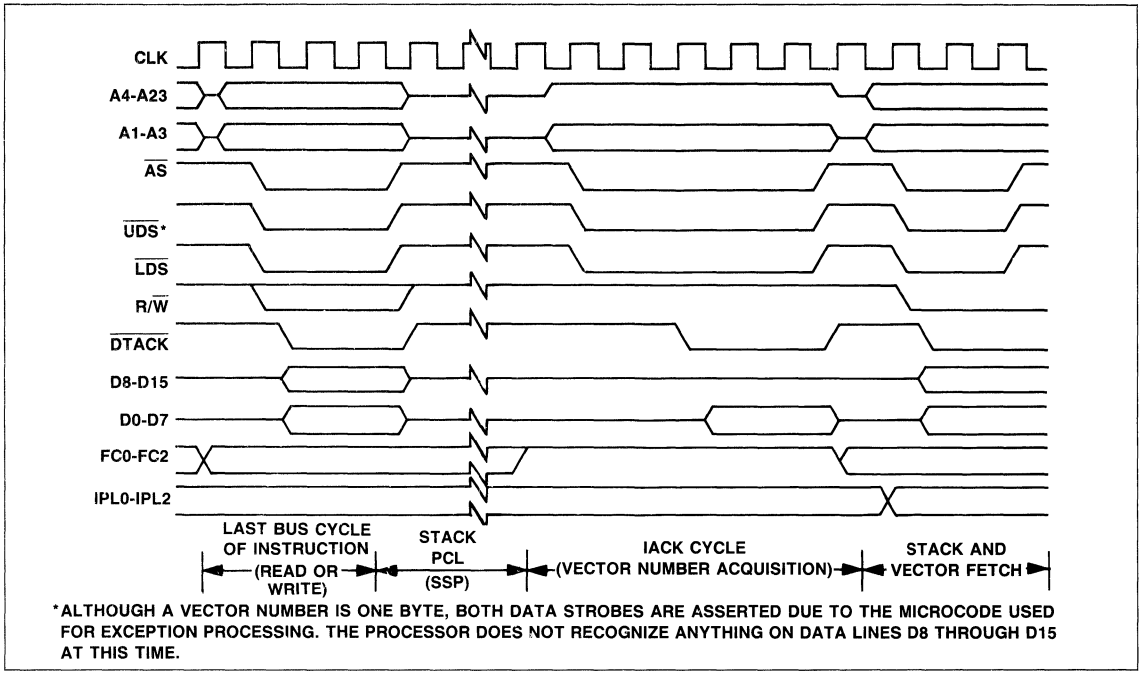


Figure 29. Interrupt Acknowledge Sequence Timing Diagram

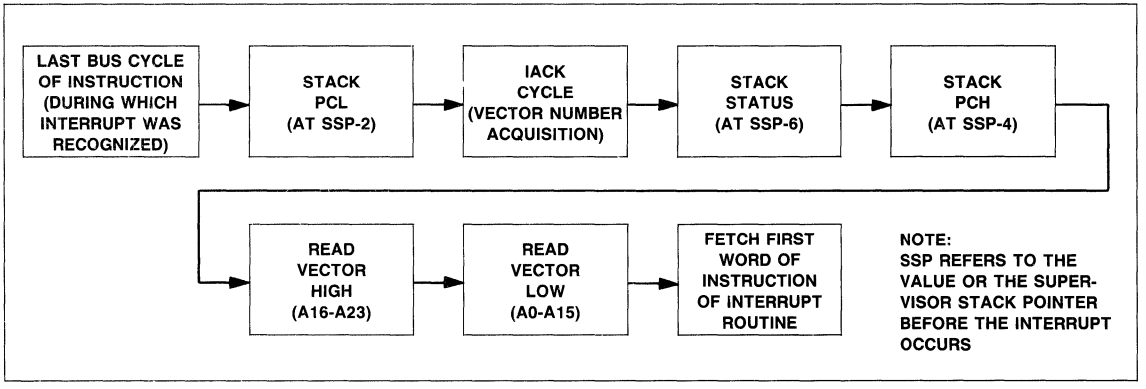


Figure 30. Interrupt Exception Timing Sequence

Some instructions are used specifically to generate traps. The TRAP instruction always forces an exception, and is useful for implementing system calls for user programs. The TRAPV and CHK instructions force an exception if the user program detects a runtime error, which may be an arithmetic overflow or a subscript out of bounds.

The signed divide (DIVS) and unsigned divide (DIVU) instructions will force an exception if a division operation is attempted with a divisor of zero.

ILLEGAL AND UNIMPLEMENTED INSTRUCTIONS. Illegal instruction refers to any of the word bit patterns which are not the bit pattern of the first word of a legal instruction. During instruction execution, if such an instruction is fetched, an illegal instruction exception occurs. Rockwell reserves the right to define instructions whose opcodes may be any of the illegal instructions. Three bit patterns will always force an illegal instruction trap on all R68000 Family compatible microprocessors. They are: $4AFA, $4AFB, and $4AFC. Two of the patterns, $4AFA and $4AFB, are reserved for Rockwell system products. The third pattern, $4AFC, is reserved for customer use.

Word patterns with bits 15 through 12 equaling 1010 or 1111 are distinguished as unimplemented instructions and separate exception vectors are given to these patterns to permit efficient emulation. This facility allows the operating system to detect program errors, or to emulate unimplemented instructions in software.

PRIVILEGE VIOLATIONS. In order to provide system security, various instructions are privileged. An attempt to execute one of the privileged instructions while in the user state will cause an exception. The privileged instructions are:

STOP	AND Immediate to SR
RESET	EOR Immediate to SR
RTE	OR Immediate to SR
MOVE USP	MOVE to SR

TRACING. To aid in program development, the R68000 includes a facility to allow instruction by instruction tracing. In the trace state, after each instruction is executed an exeception is forced, allowing a debugging program to monitor the execution of the program under test.

The trace facility uses the T-bit in the supervisor portion of the status register. If the T-bit is negated (off), tracing is disabled, and instruction execution proceeds from instruction to instruction as normal. If the T-bit is asserted (on) at the beginning of the execution of an instruction, a trace exception will be generated after the execution of that instruction is completed. If the instruction is not executed, either because an interrupt is taken, or the instruction is illegal or privileged, the trace exception does not occur. The trace exception also does not occur if the instruction is aborted by a reset, bus error, or address error exception. If the instruction is indeed executed and an interrupt is pending on completion, the trace exception is processed before the interrupt exception. If, during the execution of the instruction, an exception is forced by that instruction, the forced exception is processed before the trace exception.

As an extreme illustration of the above rules, consider the arrival of an interrupt during the execution of a TRAP instruction while tracing is enabled. First the trap exception is processed, then the trace exception, and finally the interrupt exception. Instruction execution resumes in the interrupt handler routine.

BUS ERROR. Bus error exceptions occur when the external logic requests that a bus error be processed by an exception. The current bus cycle which the processor is making is then aborted. Whether the processor was doing instruction or exception processing, that processing is terminated, and the processor immediately begins exception processing.

Exception processing for bus error follows the usual sequence of steps. The status register is copied, the supervisor state is entered, and the trace state is turned off. The vector number is generated to refer to the bus error vector. Since the processor was not between instructions when the bus error exception request was made, the context of the processor is more detailed. To save more of this context, additional information is saved on the supervisor stack. The program counter and the copy of the status register are of course saved. The value saved for the program counter is advanced by some amount, two to ten bytes beyond the address of the first word of the instruction which made the reference causing the bus error. If the bus error occurred during the fetch of the next instruction, the saved program counter has a value in the vicinity of the current instruction, even if the current instruction is a branch, a jump, or a return instruction. Besides the usual information, the processor saves its internal copy of the first word of the instruction being processed, and the address which was being accessed by the aborted bus cycle. Specific information about the access is also saved: whether it was a read or a write, whether the processor was processing an instruction or not, and the classification displayed on the function code outputs when the bus error occurred. The processor is processing an instruction if in the normal state or processing a Group 2 exception; the processor is not processing an instruction when processing a Group 0 or a Group 1 exception. Figure 31 illustates how the information is organized on the supervisor stack. Although this information is not sufficient to effect full recovery from the bus error, it does allow software diagnosis. Finally, the processor commences instruction processing at the address contained in the vector. It is the responsibility of the error handler routine to clean up the stack and determine where to continue execution.

If a bus error occurs during the exception processing for a bus error, address error, or reset, the processor is halted, and all processing ceases. This simplifies the detection of catastrophic system failure, since the processor removes itself from the system rather than destroy all memory contents. Only the $\overline{\text{RESET}}$ pin can restart a halted processor.

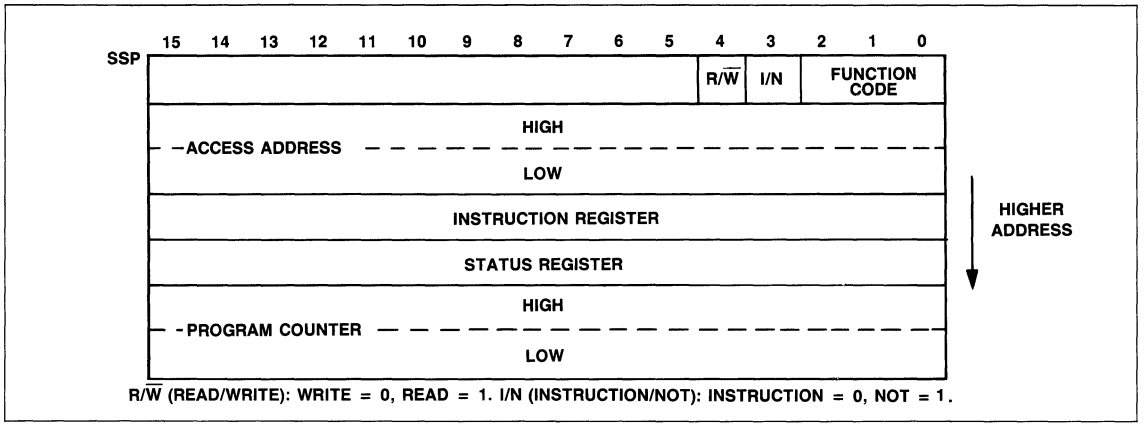


Figure 31. Supervisor Stack Order (Group 0)

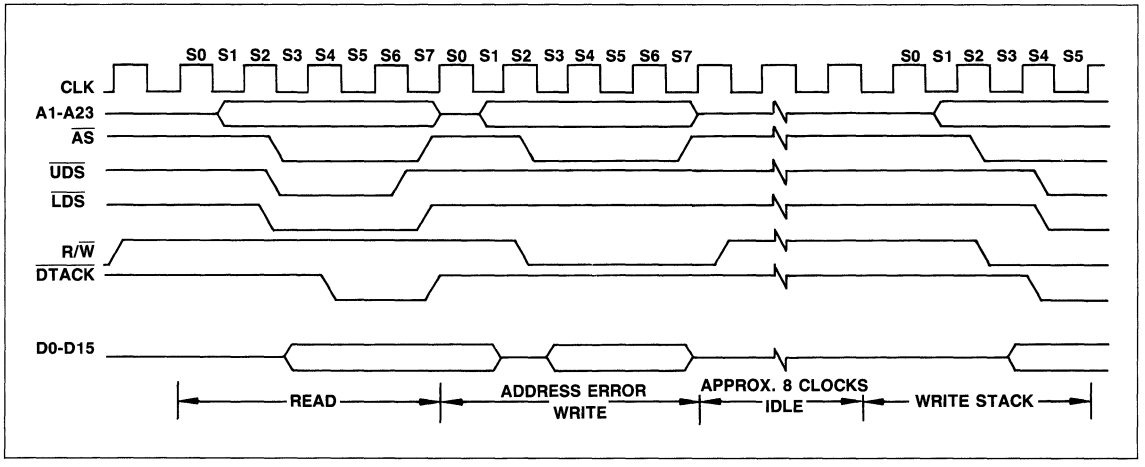


Figure 32. Address Error Timing

ADDRESS ERROR. Address error exceptions occur when the processor attempts to access a word or a long word operand or an instruction at an odd address. The effect is much like an internally generated bus error, so that the bus cycle is aborted, and the processor ceases whatever processing it is currently doing and begins exception processing. After exception processing commences, the sequence is the same as that for bus error including the information that is stacked, except that the vector number refers to the address error vector instead. Likewise, if an address error occurs during the exception processing for a bus error, address error, or reset, the processor is halted. As shown in Figure 32, an address error will execute a short bus cycle followed by an exception processing.

INTERFACE WITH R6500 PERIPHERALS

Rockwell's line of R6500 peripherals are directly compatible with the R68000. Some of these devices that are particularly useful are:

R6520 Peripheral Interface Adapter (PIA)
R6522 Versatile Interface Adapter (VIA)
R6545 CRT Controller (CRTC)
R6551 Asynchronous Communication Interface Adapter (ACIA)

To interface the synchronous R6500 peripherals with the asynchronous R68000, the processor modifies its bus cycle to meet the R6500 cycle requirements whenever an R6500 device address is detected. This is possible since both processors use memory mapped I/O. Figure 33 is a flow chart of the interface operation between the processor and R6500 devices. 6800 peripherals are also compatible with the R68000 processor.

DATA TRANSFER OPERATION

Three signals on the processor provide the R6500 interface. They are: enable (E), valid memory address ($\overline{VMA}$), and valid Peripheral address ($\overline{VPA}$). Enable corresponds to the E or Ø2 signal in existing R6500 systems. The bus frequency is one tenth of the incoming R68000 clock frequency. The timing of E allows 1 MHz peripherals to be used with an 8 MHz R68000. Enable has a 60/40 duty cycle; that is, it is low for six input clocks and high for four input clocks. This duty cycle allows the processor to do successive $\overline{VPA}$ accesses on successive E pulses.

Figures 34 and 35 give a general R6500 to R68000 interface timing, while Figures 36 and 37 detail the specific timing parameters involved in the interface. At state zero (S0) in the cycle, the address bus is in the high-impedance state. A function code is asserted on the function code output lines. One-half clock later, in state 1, the address bus is released from the high-impedance state.

During state 2, the address strobe ($\overline{AS}$) is asserted to indicate that there is a valid address on the address bus. If the bus cycle is a read cycle, the upper and/or lower data strobes are also asserted in state 2. If the bus cycle is a write cycle, the read/write (R/$\overline{W}$) signal is switched to a low (write) during state 2. One-half clock later, in state 3, the write data is placed on the data bus, and in state 4 the data strobes are issued to indicate valid data on the data bus. The processor now inserts wait states until it recognizes the assertion of $\overline{VPA}$.

The $\overline{VPA}$ input signals the processor that the address on the bus is the address of an R6500 device (or an area reserved for R6500 devices) and that the bus should conform to the Ø2 transfer characteristics of the R6500 bus. Valid peripheral address ($\overline{VPA}$) is derived by decoding the address bus, conditioned by address strobe ($\overline{AS}$). Chip select for the R6500 peripherals should be derived by decoding the address bus conditioned by $\overline{VMA}$.

After the recognition of $\overline{VPA}$, the processor assures that the Enable (E) is low, by waiting if necessary, and subsequently asserts $\overline{VMA}$. Valid memory address is then used as part of the chip select equation of the peripheral. This ensures that the R6500 peripherals are selected and deselected at the correct time. The peripheral now runs its cycle during the high portion of the E signal. Figures 34 and 35 depict the best and worst case R6500 cycle timing. This cycle length is dependent strictly upon when $\overline{VPA}$ is asserted in relationship the E clock.

If we assume that external circuitry asserts $\overline{VPA}$ as soon as possible after the assertion of $\overline{AS}$, then $\overline{VPA}$ will be recognized as being asserted on the falling edge of S4. In this case, no "extra" wait cycles will be inserted prior to the recognition of $\overline{VPA}$ assertion and only the wait cycles inserted to synchronize with the E clock will determine the total length of the cycle. In any case, the synchronization delay will be some integral number of clock cycles within the following two extremes:

1. Best Case—$\overline{VPA}$ is recognized as being asserted on the falling edge three clock cycles before E rises (or three clock cycles after E falls).
2. Worst Case—$\overline{VPA}$ is recognized as being asserted on the falling edge two clock cycles before E rises (or four clock cycles after E falls).

Near the end of a read cycle, the processor latches the peripheral's data in state 6. For all cycles, the processor negates the address and data strobes one half clock cycle later in state 7, and the Enable signal goes low at this time. Another half clock later, the address bus is put in the high-impedance state. Upon write cycle completion, the data bus is put in the high-impedance state and the read/write signal is switched high. The peripheral logic must remove $\overline{VPA}$ within one clock after address strobe is negated.

$\overline{DTACK}$ should not be asserted while $\overline{VPA}$ is asserted. Note that the R68000 $\overline{VMA}$ is active low. This allows the processor to put its buses in the high-impedance state on DMA requests without inadvertently selecting peripherals.

INTERRUPT OPERATION

During an interrupt acknowledge cycle while the processor is fetching the vector, if $\overline{VPA}$ is asserted, the R68000 will assert $\overline{VMA}$ and complete a normal R6500 read cycle as shown in Figure 38. The processor will then use an internally generated vector, called an autovector, that is a function of the interrupt being served. The seven autovectors are vector numbers 25 through 31 (decimal).

Autovectors operate in the same fashion (but are not restricted to) the R6500 interrupt sequence. The basic difference is that there are six normal interrupt vectors and one NMI type vector. As with both the R6500 and the R68000's normal vectored interrupt, the interrupt service routine can be located anywhere in the address space. This is due to the fact that while the vector numbers are fixed, the contents of the vector table entries are assigned by the user.

Since $\overline{VMA}$ is asserted during autovectoring, the R6500 peripheral address decoding should prevent unintended accesses.

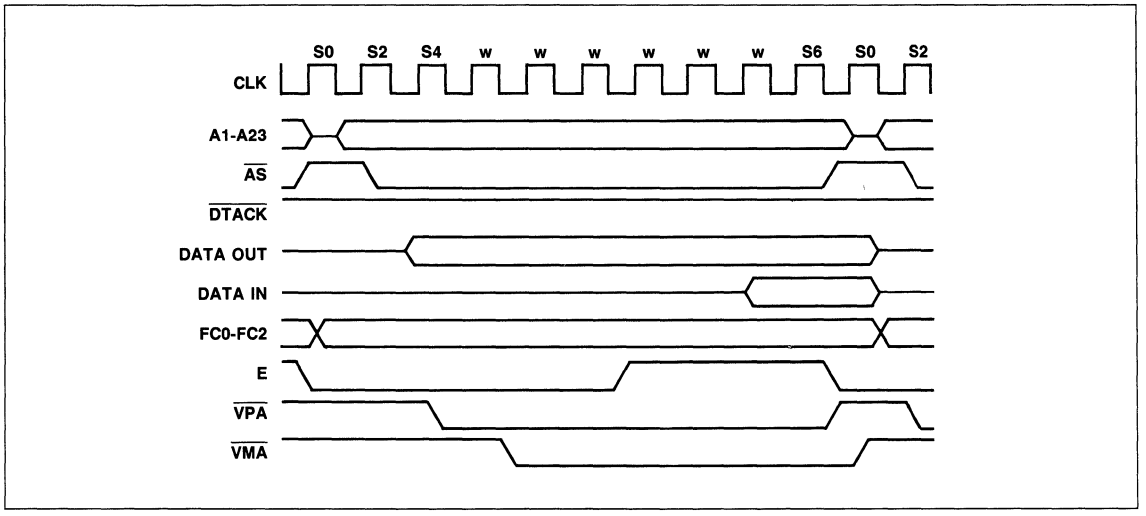


Figure 34. R68000 to R6500 Peripheral Timing—Best Case

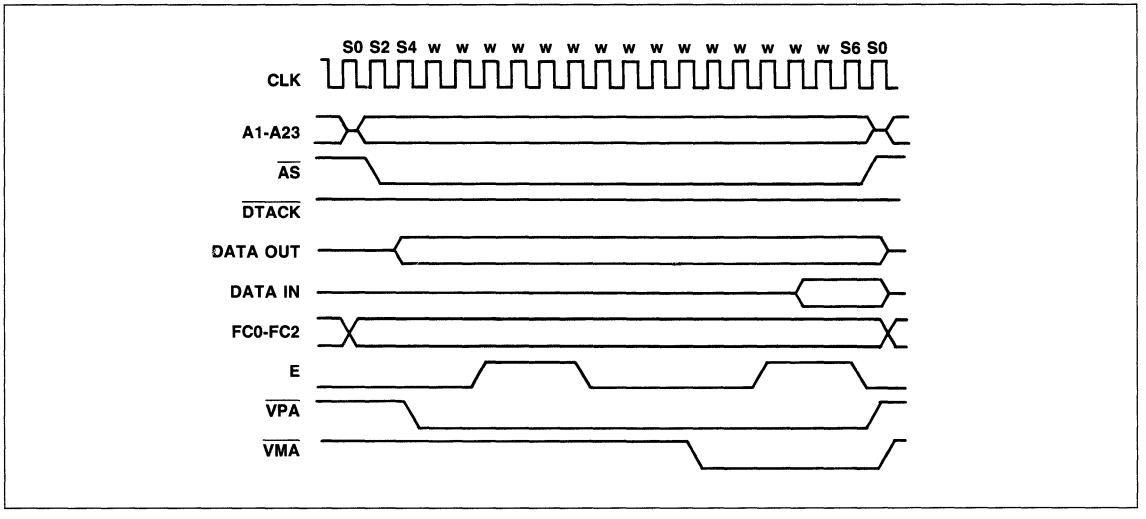
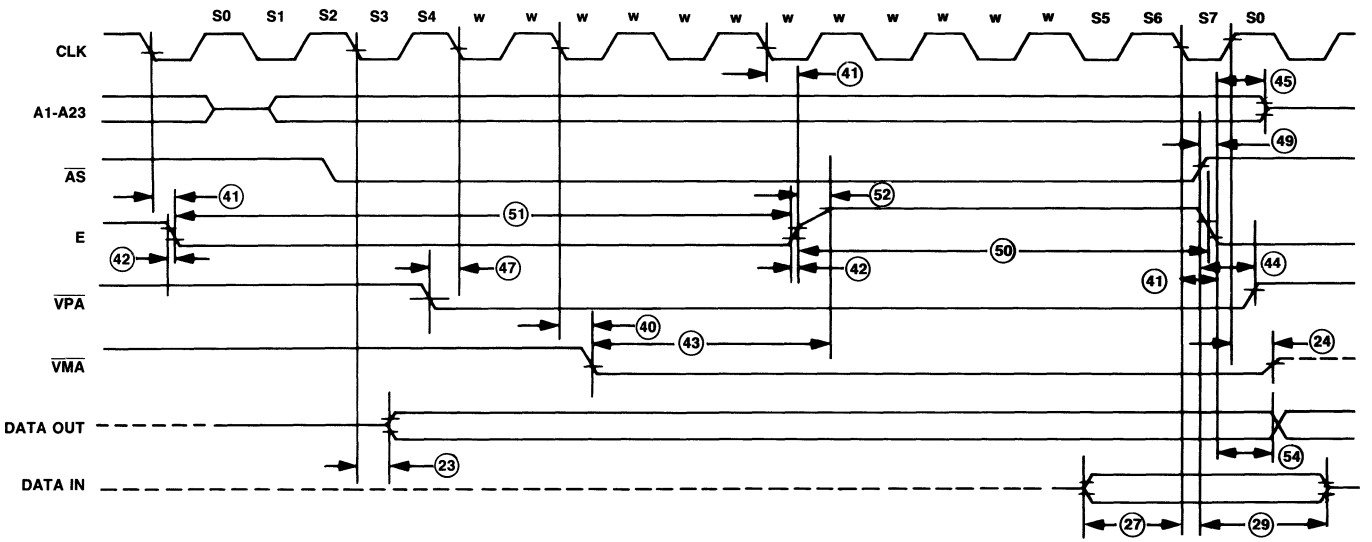


Figure 35. R68000 to R6500 Peripheral Timing—Worst Case



NOTES:
THIS FIGURE REPRESENTS THE BEST CASE R6500 TIMING WHERE $\overline{VPA}$ FALLS BEFORE THE THIRD SYSTEM CLOCK CYCLE AFTER THE FALLING EDGE OF E.

THIS TIMING DIAGRAM IS INCLUDED FOR THOSE WHO WISH TO DESIGN THEIR OWN CIRCUIT TO GENERATE $\overline{VMA}$ IT SHOWS THE BEST CASE POSSIBLY ATTAINABLE.

Figure 36. R6500 Timing—Best Case

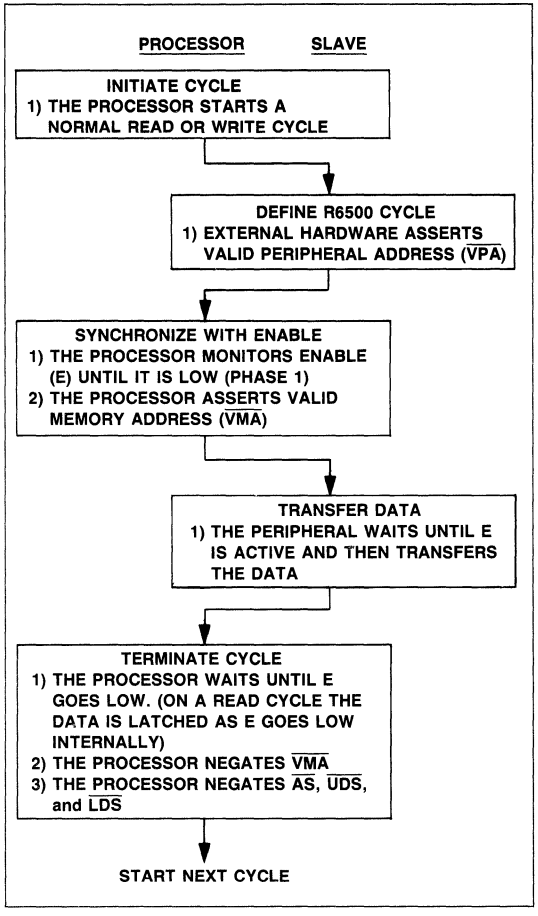


Figure 33. R6500 Interfacing Flow Chart

DATA TYPES AND ADDRESSING MODES

Five basic data types are supported. These data types are:

- Bits
- BCD Digits (4-bits)
- Bytes (8-bits)
- Word (16-bits)
- Long Words (32-bits)

In addition, operations on other data types such as memory addresses, status word data, etc., are provided for in the instruction set.

The 14 addressing modes, shown in Table 9, include six basic types:

- Register Direct
- Register Indirect
- Absolute
- Program Counter Relative
- Implied
- Immediate

Included in the register indirect addressing modes is the capability to do postincrementing, predecrementing, offsetting and indexing. Program counter relative mode can also be modified via indexing and offsetting.

Table 9. Addressing Modes

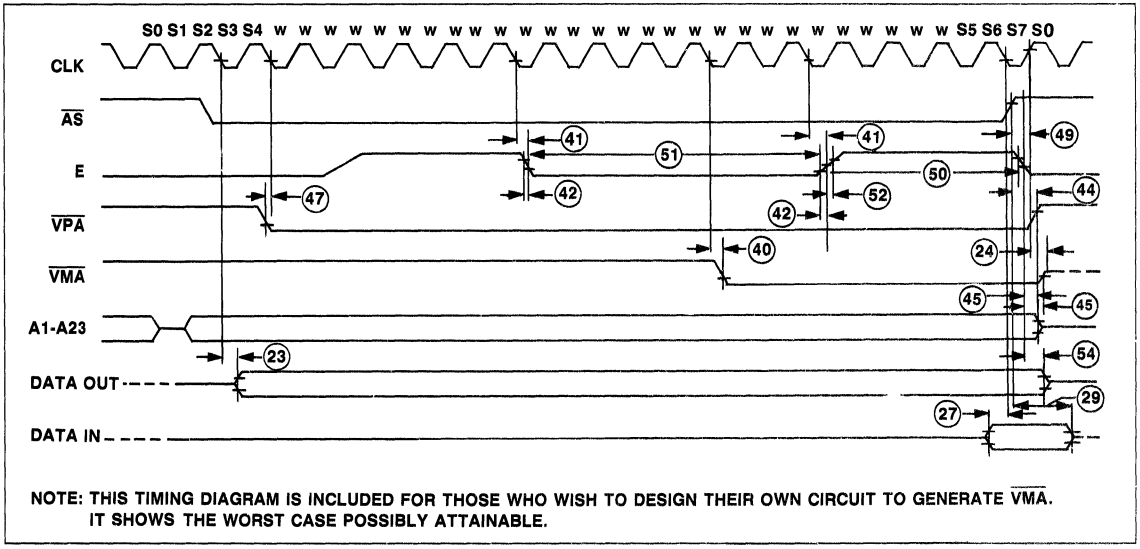
Mode	Generation
Register Direct Addressing	
Data Register Direct	EA = Dn
Address Register Direct	EA = An
Absolute Data Addressing	
Absolute Short	EA = (Next Word)
Absolute Long	EA = (Next Two Words)
Program Counter Relative Addressing	
Relative with Offset	EA = (PC) + d_{16}
Relative with Index and Offset	EA = (PC) + (Xn) + d_8
Register Indirect Addressing	
Register Indirect	EA = (An)
Postincrement Register Indirect	EA = (An), An ← An + N
Predecrement Register Indirect	An ← An – N, EA = (An)
Register Indirect with Offset	EA = (An) + d_{16}
Indexed Register Indirect with Offset	EA = (An) + (Xn) + d_8
Immediate Data Addressing	
Immediate	DATA = Next Word(s)
Quick Immediate	Inherent Data
Implied Addressing	
Implied Register	EA = SR, USP, SP, PC

NOTES:

EA = Effective Address
An = Address Register
Dn = Data Register
Xn = Address or Data Register used as Index Register
SR = Status Register
PC = Program Counter
( ) = Contents of
d_8 = Eight-bit Offset (displacement)
d_{16} = Sixteen-bit Offset (displacement)
N = 1 for Byte, 2 for Words and 4 for Long Word. If An is the stack pointer and the operand size is byte, N = 2 to keep the stack pointer on a word boundry.
← = Replaces

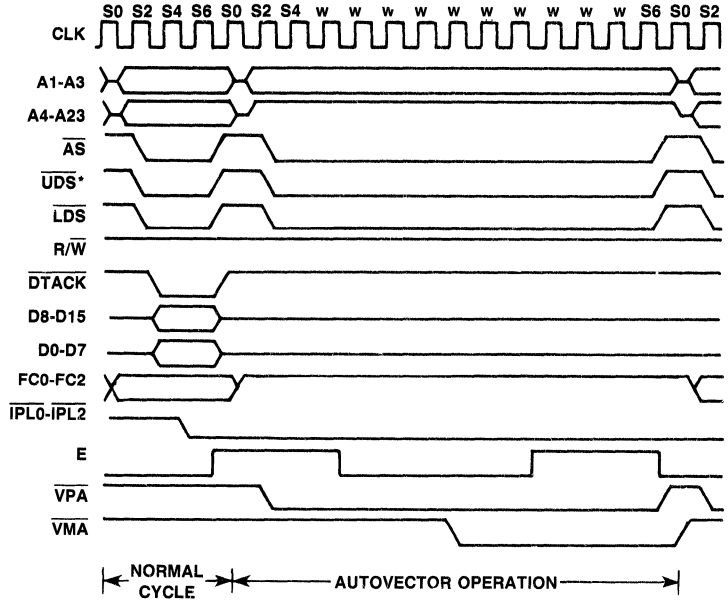
INSTRUCTION SET OVERVIEW

The R68000 instruction set is shown in Table 10. Some additional instructions are variations, or subsets, of these and they appear in Table 11. Special emphasis has been given to the instruction set's support of structured high-level languages to facilitate ease of programming. Each instruction, with few exceptions, operates on bytes, words, and long words and most instructions can use any of the 14 addressing modes. Combining instruction types, data types, and addressing modes, over 1000 useful instructions are provided. These instructions include signed and unsigned multiply and divide, "quick" arithmetic operations. BCD arithmetic and expanded operations (through traps).



NOTE: THIS TIMING DIAGRAM IS INCLUDED FOR THOSE WHO WISH TO DESIGN THEIR OWN CIRCUIT TO GENERATE VMA. IT SHOWS THE WORST CASE POSSIBLY ATTAINABLE.

Figure 37. RC68000 to R6500 Peripheral Timing Diagram — Worst Case



*ALTHOUGH A VECTOR NUMBER IS ONE BYTE, BOTH DATA STROBES ARE ASSERTED DUE TO THE MICROCODE USED FOR EXCEPTION PROCESSING. THE PROCESSOR DOES NOT RECOGNIZE ANYTHING ON DATA LINES D8 THROUGH D15 AT THIS TIME.

Figure 38. Autovector Operation Timing Diagram

Table 10. Instruction Set Summary

Mnemonic	Description	Mnemonic	Description	Mnemonic	Description
ADBC	Add Decimal with Extend	EOR	Exclusive Or	PEA	Push Effective Address
ADD	Add	EXG	Exchange Registers		
AND	Logical And	EXT	Sign Extend	RESET	Reset External Devices
ASL	Arithmetic Shift Left			ROL	Rotate Left without Extend
ASR	Arithmetic Shift Right	JMP	Jump	ROR	Rotate Right without Extend
		JSR	Jump to Subroutine	ROXL	Rotate Left with Extend
B_{CC}	Branch Conditionally			ROXR	Rotate Right with Extend
BCHG	Bit Test and Change	LEA	Load Effective Address	RTE	Return from Exception
BCLR	Bit Test and Clear	LINK	Link Stack	RTR	Return and Restore
BRA	Branch Always	LSL	Logical Shift Left	RTS	Return from Subroutine
BSET	Bit Test and Set	LSR	Logical Shift Right		
BSR	Branch to Subroutine			SBCD	Subtract Decimal with Extend
BTST	Bit Test	MOVE	Move	S_{CC}	Set Conditional
		MULS	Signed Multiply	STOP	Stop
CHK	Check Register Against Bounds	MULU	Unsigned Multiply	SUB	Subtract
				SWAP	Swap Data Register Halves
CLR	Clear Operand	NBCD	Negate Decimal with Extend		
CMP	Compare	NEG	Negate	TAS	Test and Set Operand
		NOP	No Operation	TRAP	Trap
DB_{CC}	Test Condition, Decrement and Branch	NOT	One's Complement	TRAPV	Trap on Overflow
				TST	Test
DIVS	Signed Divide	OR	Logical Or		
DIVU	Unsigned Divide			UNLK	Unlink

Table 11. Variations of Instruction Types

Instruction Type	Variation	Description	Instruction Type	Variation	Description
ADD	**ADD**	Add	**MOVE**	**MOVE**	Move
	ADDA	Add Address		MOVEA	Move Address
	ADDQ	Add Quick		MOVEM	Move Multiple Registers
	ADDI	Add Immediate		MOVEP	Move Peripheral Data
	ADDX	Add with Extend		MOVEQ	Move Quick
				MOVE from SR	Move from Status Register
AND	**AND**	Logical And		MOVE to SR	Move to Status Register
	ANDI	And Immediate		MOVE to CCR	Move to Condition Codes
	ANDI to CCR	And Immediate to Condition Codes		MOVE USP	Move User Stack Pointer
	ANDI to SR	And Immediate to Status Register	**NEG**	**NEG**	Negate
				NEGX	Negate with Extend
CMP	**CMP**	Compare	**OR**	**OR**	Logical Or
	CMPA	Compare Address		ORI	Or Immediate
	CMPM	Compare Memory		ORI to CCR	Or Immediate to Condition Codes
	CMPI	Compare Immediate		ORI to SR	Or Immediate to Status Register
EOR	**EOR**	Exclusive Or	**SUB**	**SUB**	Subtract
	EORI	Exclusive Or Immediate		SUBA	Subtract Address
	EORI to CCR	Exclusive Or Immediate to Condition Codes		SUBI	Subtract Immediate
				SUBQ	Subtract Quick
	EORI to SR	Exclusive Or Immediate to Status Register		SUBX	Subtract with Extend

The following paragraphs contain an overview of the form and structure of the R68000 instruction set. The instructions form a set of tools that include all the machine functions to perform the following operations:

Data Movement
Integer Arithmetic
Logical
Shift and Rotate
Bit Manipulation
Binary Coded Decimal
Program Control
System Control

The complete range of instruction capabilities combined with the flexible addressing modes described previously provide a very flexible base for program development.

ADDRESSING

Instructions for the R68000 contain two kinds of information: the type of function to be performed, and the location of the operand(s) on which to perform that function. The methods used to locate (address) the operand(s) are explained in the following paragraphs.

Instructions specify an operand location in one of three ways:

Register Specification — the number of the register is given in the register field of the instruction.

Effective Address — use of the different effective address modes.

Implicit Reference — the definition of certain instructions implies the use of specific registers.

DATA MOVEMENT OPERATIONS

The move (MOVE) instruction provides a means for data acquisition (transfer and storage). The move instruction and the effective addressing modes allow both address and data manipulation. Data move instructions allow byte, word, and long word operands to be transferred from memory to memory, memory to register, register to memory, and register to register. Address move instructions allow word and long word operand transfers and ensure that only legal address manipulations are executed. In addition to the general move instruction there are several special data movement instructions: move multiple registers (MOVEM), move peripheral data (MOVEP), exchange registers (EXG), load effective address (LEA), push effective address (PEA), link stack (LINK), unlink stack (UNLK), and move quick (MOVEQ). Table 12 summarizes the data movement operations.

INTEGER ARITHMETIC OPERATIONS

The arithmetic operators include the four basic operations of add (ADD), subtract (SUB), multiply (MUL), and divide (DIV) as well as arithmetic compare (CMP), clear (CLR), and negate (NEG). The add and subtract instructions are available for both address and data operations, and with data operations accepting all operand sizes. Address operations are limited to legal address size operands (16 or 32 bits). Data, address, and memory compare operations are also available. The clear and negate instructions may be used on all sizes of data operands.

The multiply and divide operations are available for signed and unsigned operands using word multiply to produce a long word product, and a long word dividend with word divisor to produce a word quotient with a word remainder.

Multiprecision and mixed size arithmetic can be accomplished using a set of extended instructions. These instructions are: add extended (ADDX), subtract extended (SUBX), sign extend (EXT), and negate binary with extend (NEGX).

A text operand (TST) instruction that sets the condition codes as a result of a compare of the operand with zero is available. Test and set (TAS) is a synchronization instruction useful in multiprocessor systems. Table 13 summrizes the integer arithmetic operations.

Table 12. Data Movement Operations

Instruction	Operand Size	Operation
EXG	32	Rx↔Ry
LEA	32	EA→ An
LINK	—	An →–(SP) SP →An SP + displacement →SP
MOVE	8, 16, 32	s →d
MOVEM	16, 32	(EA) →An, Dn An, Dn →EA
MOVEP	16, 32	(EA) →Dn Dn →(EA)
MOVEQ	8	#xxx →Dn
PEA	32	EA →–(SP)
SWAP	32	Dn[31.16]↔Dn[15:0]
UNLK	—	An →Sp (SP) + →An

NOTES:
s = source –( ) = indirect with predecrement
d = destination ( )+ = indirect with postdecrement
[ ] = bit number # = immediate data

INSTRUCTION FORMAT

Instructions, as shown in Figure 39, vary from one to five words in length. The first word of the instruction, called the operation word, specifies the length of the instruction and the operation to be performed. The remaining words further specify the operands. These words are either immediate operands or extensions to the effective address mode specified in the operation word.

Table 13. Integer Arithmetic Operations

Instruction	Operand Size	Operation
ADD	8, 16, 32	Dn + (EA) → Dn
		(EA) + Dn → (EA)
		(EA) + #xxx → (EA)
	16, 32	An + (EA) → An
ADDX	8, 16, 32	Dx + Dy + X → Dx
	16, 32	−(Ax) + −(Ay) + X → (Ax)
CLR	8, 16, 32	0 → EA
CMP	8, 16, 32	Dn − (EA)
		(EA) − #xxx
		(Ax)+ − (Ay)−
	16, 32	An − (EA)
DIVS	32 ÷ 16	Dn ÷ (EA) → Dn
DIVU	32 ÷ 16	Dn ÷ (EA) → Dn
EXT	8 → 16	$(Dn)_8 \rightarrow Dn_{16}$
	16 → 32	$(Dn)_{16} \rightarrow Dn_{32}$
MULS	16 × 16 → 32	Dn × (EA) → Dn
MULU	16 × 16 → 32	Dn × (EA) → Dn
NEG	8, 16, 32	0 − (EA) → (EA)
NEGX	8, 16, 32	0 − (EA) − X → (EA)
SUB	8, 16, 32	Dn − (EA) → Dn
		(EA) − Dn → (EA)
		(EA) − #xxx → (EA)
	16, 32	An − (EA) → An
SUBX	8, 16, 32	Dx − Dy − X → Dx
		−(Ax) − −(Ay) − X → (Ax)
TAS	8	[EA] − 0, 1 → EA[7]
TST	8, 16, 32	(EA) − 0

NOTES:
[ ] = bit number
−( ) = indirect with predecrement
( )+ = indirect with postdecrement
= immediate data

PROGRAM/DATA REFERENCES

The R68000 separates memory references into two classes: program references, and data references. Program references reference that section of memory that contains the program being executed. Data references refer to that section of memory that contains data. Operand reads are from the data space, except in the case of the program counter relative addressing mode. All operand writes are to the data space.

REGISTER SPECIFICATION

The register field within an instruction specifies the register to be used. Other fields within the instruction specify whether the register selected is an address or data register and how the register is to be used.

EFFECTIVE ADDRESS

Most instructions specify the location of an operand by using the effective address field in the operation word. For example, Figure 40 shows the general format of the single effective address instruction operation word. The effective address is composed of two 3-bit fields: the mode field, and the register field. The value in the mode field selects the different address modes. The register field contains the number of a register.

The effective address field may require additional information to fully specify the operand. This additional information, called the effective address extension, is contained in the following word or words and is considered part of the instruction, as shown in Figure 39. The effective address modes are grouped into three categories: register direct, memory addressing, and special.

REGISTER DIRECT MODES. These effective addressing modes specify that the operand is in one of the 16 multifunction registers.

Data Register Direct. The operand is in the data register specified by the effective address register field.

Address Register Direct. The operand is in the address register specified by the effective address register field.

MEMORY ADDRESS MODES. These effective addressing modes specify that the operand is in memory and provide the specific address of that operand.

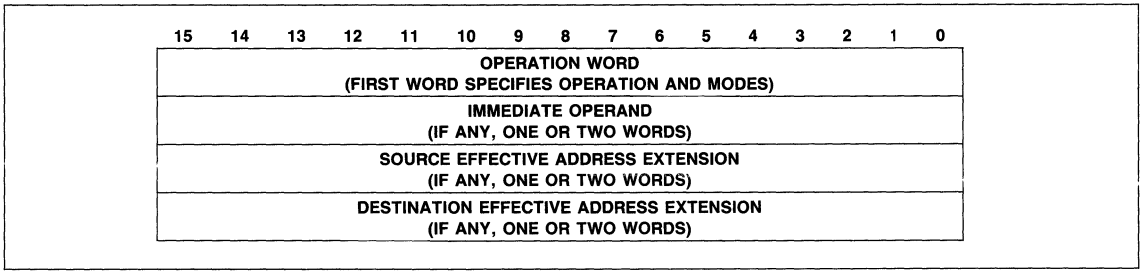


Figure 39. Instruction Format

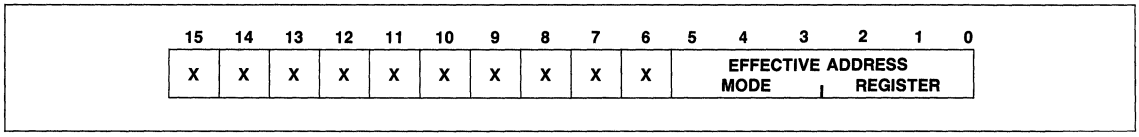


Figure 40. Single-Effective-Address Instruction Operation Word General Format

Address Register Indirect. The address of the operand is in the address register specified by the register field. The reference is classified as a data reference with the exception of the jump and jump to subroutine instructions.

Address Register Indirect With Postincrement. The address of the operand is in the address register specified by the register field. After the operand address is used, it is incremented by one, two or four depending upon whether the size of the operand is byte, word, or long word. If the address register is the stack pointer and the operand size is byte, the address is incremented by two rather than one to keep the stack pointer on a word boundary. The reference classifies as a data reference.

Address Register Indirect With Predecrement. The address of the operand is in the address register specified by the register field. Before the operand address is used, it is decremented by one, two, or four depending upon whether the operand size is byte, word, or long word. If the address register is the stack pointer and the operand size is byte, the address is decremented by two rather than one to keep the stack pointer on a word boundary. The reference is classified as a data reference.

Address Register Indirect with Displacement. This address mode requires one word of extension. The address of the operand is the sum of the address in the address register and the sign-extended 16-bit displacement integer in the extension word. The reference classifies as a data reference with the exception of the jump to subroutine instructions.

Address Register Indirect With Index. This address mode requires one word of extension. The address of the operand sums the addresses in the address register, the sign-extended displacement integer in the low order eight bits of the extension word, and the contents of the index register. The reference is classified as a data reference with the exception of the jump and jump to subroutine instructions.

SPECIAL ADDRESS MODE. The special address modes use the effective address register field to specify the special addressing mode instead of a register number.

Absolute Short Address. This address mode requires one word of extension. The address of the operand is the extension word. The 16-bit address is sign extended before it is used. The reference classifies as a data reference with the exception of the jump and jump to subroutine instructions.

Absolute Long Address. This address mode requires two words of extension. The address of the operand is developed by the concatenation of the extension words. The high-order part of the address is the first extension word; the low-order part of the address is the second extension word. The reference classifies as a data reference with the exception of the jump and jump to subroutine instructions.

Program Counter With Displacement. This address mode requires one word of extension. The address of the operand sums the addresses in the program counter and the sign-extended 16-bit displacement integer in the extension word. The value in the program counter is the address of the extension word. The reference classifies as a program reference.

Program Counter With Index. This address mode requires one word of extension. This address sums the addresses in the program counter, the sign-extended displacement integer in the lower eight bits of the extension word, and the contents of the index register. The value in the program counter is the address of the extension word. This reference classifies as a program reference.

Immediate Data. This address mode requires either one or two words of extension depending on the size of the operation.

Byte Operation	— operand is low order byte of extension word
Word Operation	— operand is extension word
Long Word Operation	— operand is in the two extension words, high-order 16 bits are in the first extension word, low-order 16 bits are in the second extension word.

IMPLICIT REFERENCE

Some instructions make implicit reference to the program counter (PC), the system stack pointer (SP), the supervisor stack pointer (SSP), the user stack pointer (USP), or the status register (SR).

A selected set of instructions may reference the status register by means of the effective address field. These are:

ANDI to CCR
ANDI to SR
EORI to CCR
EORI to SR
MOVE to CCR
MOVE to SR
MOVE from SR
ORI to CCR
ORI to SR

EFFECTIVE ADDRESS ENCODING SUMMARY

Table 14 summarizes the effective addressing modes discussed in the previous paragraphs.

Table 14. Effective Address Encoding Summary

Addressing Mode	Mode	Register
Data Register Direct	000	register number
Address Register Direct	001	register number
Address Register Indirect	010	register number
Address Register Indirect with Postincrement	011	register number
Address Register Indirect with Predecrement	100	register number
Address Register Indirect with Displacement	101	register number
Address Register Indirect with Index	110	register number
Absolute Short	111	000
Absolute Long	111	001
Program Counter with Displacement	111	010
Program Counter with Index	111	011
Immediate	111	100

SYSTEM STACK. The system stack is used implicitly by many instructions; user stacks and queues may be created and maintained through the addressing modes. Address register seven (A7) is the system stack pointer (SP). The system stack pointer is either the supervisor stack pointer (SSP) or the user stack pointer (USP), depending on the state of the S-bit in the status register. If the S-bit indicates supervisor state (High), SSP is the active system stack pointer, and the USP cannot be referenced as an address register. If the S-bit indicates user state (Low), the USP is the active system stack pointer, and the SSP cannot be referenced. Each system stack fills from high memory to low memory.

LOGICAL OPERATIONS

Logical operation instructions AND, OR, EOR, and NOT are available for all sizes of integer data operands. A similar set of immediate instructions (ANDI, ORI, and EORI) provide these logical operations with all sizes of immediate data. Table 15 summarizes the logical operations.

SHIFT AND ROTATE OPERATIONS

Shift operations in both directions are provided by arithmetic instructions ASR and ASL and logical shift instructions LSR and LSL. The rotate instructions (with and without extend) available are ROXR, ROXL, ROR, and ROL. All shift and rotate operations can be performed in either registers or memory. Register shifts and rotates support all operand sizes and allow a shift count specified in a data register.

Table 15. Logical Operations

Instruction	Operand Size	Operation
AND	8, 16, 32	DnΛ(EA) →Dn (EA)ΛDn →(EA) (EA)Λ#xxx →(EA)
OR	8, 16, 32	Dn ν (EA) →Dn (EA) ν Dn →(EA) (EA) ν #xxx →(EA)
EOR	8, 16, 32	(EA) ⊕ Dy →(EA) (EA) ⊕ #xxx →(EA)
NOT	8, 16, 32	~ (EA) →(EA)

NOTES:
~ = invert
# = immediate data
Λ = logical AND
ν = logical OR
⊕ = logical exclusive OR

Memory shifts and rotates are for word operands only and allow only single-bit shifts or rotates.

Table 16 summarizes the shift and rotate operations.

BIT MANIPULATION OPERATIONS

The following instructions provide bit manipulation operations: bit test (BTST), bit test and set (BSET), bit test and clear (BCLR), and bit test and change (BCHG). Table 17 is a summary of the bit manipulation operations. (Bit 2 of the status register is Z.)

Table 16. Shift and Rotate Operations

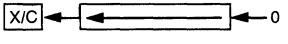
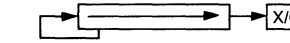
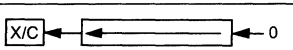
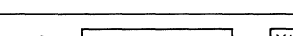
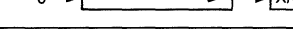
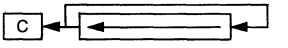
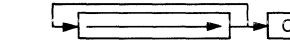
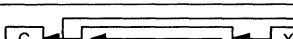
Instruction	Operand Size	Operation
ASL	8, 16, 32	
ASR	8, 16, 32	
LSL	8, 16, 32	
LSR	8, 16, 32	
ROL	8, 16, 32	
ROR	8, 16, 32	
ROXL	8, 16, 32	
ROXR	8, 16, 32	

Table 17. Bit Manipulation Operations

Instruction	Operand Size	Operation
BTST	8, 32	~ bit of (EA) →Z
BSET	8, 32	~ bit of (EA) →Z 1 →bit of EA
BCLR	8, 32	~ bit of (EA) →Z 0 →bit of EA
BCHG	8, 32	~ bit of (EA) →Z ~ bit of (EA) →bit of EA
NOTE: ~ = invert		

BINARY CODED DECIMAL OPERATIONS

The following instructions accomplish multiprecision arithmetic operations on binary coded decimal numbers: add decimal with extend (ABCD), subtract decimal with extend (SBCD), and negate decimal with extend (NBCD). Table 18 summarizes the binary coded decimal operations.

PROGRAM CONTROL OPERATIONS

Program control operations implementation requires a series of conditional and unconditional branch instructions and return instructions. These instructions are summarized in Table 19.

The conditional instructions provide setting and branching for the following conditions:

CC — carry clear
CS — carry set
EQ — equal
F — never true
GE — greater or equal
GT — greater than
HI — high
LE — less or equal
LS — low or same
LT — less than
MI — minus
NE — not equal
PL — plus
T — always true
VC — no overflow
VS — overflow

Table 18. Binary Coded Decimal Operations

Instruction	Operand Size	Operation
ABCD	8	$Dx_{10} + Dy_{10} + X \rightarrow Dx$ $-(Ax)_{10} + -(Ay)_{10} + x \rightarrow (Ax)$
SBCD	8	$Dx_{10} - Dy_{10} - X \rightarrow Dx$ $-(Ax)_{10} - -(Ay)_{10} - X \rightarrow (Ax)$
NBCD	8	$0 - (EA)_{10} - X \rightarrow (EA)$
NOTE: -( ) = indirect with predecrement		

Table 19. Program Control Operations

Instruction	Operation
Conditional	
B_{CC}	Branch conditionally (14 conditions) 8- and 16-bit displacement
DB_{CC}	Test condition, decrement, branch 16-bit displacement
S_{CC}	Set byte conditionally (16 conditions)
Unconditional	
BRA	Branch always 8- and 16-bit displacement
BSR	Branch to subroutine 8- and 16-bit displacement
JMP	Jump
JSR	Jump to subroutine
Returns	
RTR	Return and restore condition codes
RTS	Return from subroutine

SYSTEM CONTROL OPERATIONS

System control operations are accomplished by using privileged instructions, trap generating instructions, and instructions that use or modify the status register. These instructions are summarized in Table 20.

INSTRUCTION SET

The following paragraphs provide information about the addressing categories and instruction set of the R68000.

ADDRESSING CATEGORIES

Effective address modes may be categorized by the ways in which they may be used. The following classifications will be used in the instructions definitions.

Data — If an effective address mode may be used to refer to data operands, it is considered a data addressing effective address mode.

Memory — If an effective address mode may be used to refer to memory operands, it is considered a memory addressing effective address mode.

Alterable — If an effective address mode may be used to refer to alterable (writeable) operands, it is considered an alterable addressing effective address mode.

Control — If an effective address mode may be used to refer to memory operands without an associated size, it is considered control addressing effective address mode.

Table 21 shows the various categories to which each of the effective address modes belong. Table 22 is the instruction set summary.

Table 20. System Control Operations

Instruction	Operation
Privileged	
ANDI to SR	Logical AND to Status Register
EORI to SR	Logical EOR to Status Register
MOVE EA to SR	Load New Status Register
MOVE USP	Move User Stack Pointer
ORI to SR	Logical OR to Status Register
RESET	Reset External Devices
RTE	Return from Exception
STOP	Stop Program Execution
Trap Generating	
CHK	Check Data Register Against Upper Bounds
TRAP	Trap
TRAPV	Trap on Overflow
Status Register	
ANDI to CCR	Logical AND to Condition Codes
EORI to CCR	Logical EOR to Condition Codes
MOVE EA to CCR	Load New Condition Codes
MOVE SR to EA	Store Status Register
ORI to CCR	Logical OR to Condition Codes

The status register addressing mode is not permitted unless it is explicitly mentioned as a legal addressing mode.

These categories may be combined, so that additional, more restrictive, classifications may be defined. For example, the instruction descriptions use such classifications as alterable memory or data alterable. The former refers to those addressing modes which are both alterable and memory addresses, and the latter refers to addressing modes which are both data and alterable.

INSTRUCTION PREFETCH

The R68000 uses a two-word tightly-coupled instruction prefetch mechanism to enhance performance. This mechanism is described in terms of the microcode operations involved. If the execution of an instruction is defined to begin when the microroutine for that instruction is entered, some features of the prefetch mechanism can be described.

1) When execution of an instruction begins, the operation word and the word following have already been fetched. The operation word is in the instruction decoder.
2) In the case of multi-word instructions, as each additional word of the instruction is used internally, a fetch is made to the instruction stream to replace it.
3) The last fetch from the instruction stream is made when the operation word is discarded and decoding is started on the next instruction.
4) If the instruction is a single-word instruction causing a branch, the second word is not used. But because this word is fetched by the preceding instruction, it is impossible to avoid this superfluous fetch.
5) In the case of an interrupt or trace exception, both words are not used.
6) The program counter usually points to the last word fetched from the instruction stream.

INSTRUCTION EXECUTION TIMES

The following paragraphs contain listings of the instruction execution times in terms of external clock (CLK) periods. In this timing data, it is assumed that both memory read and write cycle times are four clock periods. Any wait states caused by a longer memory cycle must be added to the total instruction time. The number of bus read and write cycles for each instruction is enclosed in parenthesis following the execution periods and is shown as (r/w) where r is the number of read cycles and w is the number of write cycles.

Table 21. Effective Addressing Mode Categories

Effective Address Modes	Mode	Register	Addressing Categories			
			Data	Memory	Control	Alterable
Dn	000	Register Number	X	—	—	X
An	001	Register Number	—	—	—	X
(An)	010	Register Number	X	X	X	X
(An)+	011	Register Number	X	X	—	X
−(An)	100	Register Number	X	X	—	X
d(An)	101	Register Number	X	X	X	X
d(An, ix)	110	Register Number	X	X	X	X
xxx.W	111	000	X	X	X	X
xxx.L	111	001	X	X	X	X
d(PC)	111	010	X	X	X	—
d(PC, ix)	111	011	X	X	X	—
#xxx	111	X	X	X	—	—

Table 22. Instruction Set

Mnemonic	Description	Operation	Condition Codes				
			X	N	Z	V	C
ABCD	Add Decimal with Extend	(Destination)$_{10}$ + (Source)$_{10}$ + X → Destination	*	U	*	U	*
ADD	Add Binary	(Destination) + (Source) → Destination	*	*	*	*	*
ADDA	Add Address	(Destination) + (Source) → Destination	—	—	—	—	—
ADDI	Add Immediate	(Destination) + Immediate Data → Destination	*	*	*	*	*
ADDQ	Add Quick	(Destination) + Immediate Data → Destination	*	*	*	*	*
ADDX	Add Extended	(Destination) + (Source) + X → Destination	*	*	*	*	*
AND	AND Logical	(Destination) Λ (Source) → Destination	—	*	*	0	0
ANDI	AND Immediate	(Destination) Λ Immediate Data → Destination	—	*	*	0	0
ANDI to CCR	AND Immediate to Condition Codes	(Source) Λ CCR → CCR	*	*	*	*	*
ANDI to SR	AND Immediate to Status Register	(Source) Λ SR → SR	*	*	*	*	*
ASL, ASR	Arithmetic Shift	(Destination) Shifted by <count> → Destination	*	*	*	*	*
B$_{CC}$	Branch Conditionally	If $_{CC}$ then PC + d → PC	—	—	—	—	—
BCHG	Test a Bit and Change	~ (<bit number>) OF Destination → Z ~ (<bit number>) OF Destination → <bit number> OF Destination	—	—	*	—	—
BCLR	Test a Bit and Clear	~ (<bit number>) OF Destination → Z 0 → <bit number> → OF Destination	—	—	*	—	—
BRA	Branch Always	PC + d → PC	—	—	—	—	—
BSET	Test a Bit and Set	~ (<bit number>) OF Destination → Z 1 → <bit number> OF Destination	—	—	*	—	—
BSR	Branch to Subroutine	PC → (SP); PC + d → PC	—	—	—	—	—
BTST	Test a Bit	~ (<bit number>) OF Destination → Z	—	—	*	—	—
CHK	Check Register Against Bounds	If Dn <0 or Dn> (<ea>) then TRAP	—	*	U	U	U
CLR	Clear and Operand	0 → Destination	—	0	1	0	0
CMP	Compare	(Destination) – (Source)	—	*	*	*	*
CMPA	Compare Address	(Destination) – (Source)	—	*	*	*	*
CMPI	Compare Immediate	(Destination) – Immediate Data	—	*	*	*	*
CMPM	Compare Memory	(Destination) – (Source)	—	*	*	*	*
DB$_{CC}$	Test Condition, Decrement and Branch	If ~ $_{CC}$ then Dn – 1 → Dn; if Dn ≠ – 1 then PC + d → PC	—	—	—	—	—
DIVS	Signed Divide	(Destination)/(Source) → Destination	—	*	*	*	0
DIVU	Unsigned Divide	(Destination)/(Source) → Destination	—	*	*	*	0
EOR	Exclusive OR Logical	(Destination) ⊕ (Source) → Destination	—	*	*	0	0
EORI	Exclusive OR Immediate	(Destination) ⊕ Immediate Data → Destination	—	*	*	0	0
EORI to CCR	Exclusive OR Immediate to Condition Codes	(Source) ⊕ CCR → CCR	*	*	*	*	*

NOTES:

Λ = logical AND
ν = logical OR
⊕ = logical exclusive OR
~ = logical complement

* = affected
— = unaffected
0 = cleared
1 = set
U = undefined

Table 22. Instruction Set (Continued)

Mnemonic	Description	Operation	Condition Codes				
			X	N	Z	V	C
EORI to SR	Exclusive OR Immediate to Status Register	(Source) ⊕ SR → SR	*	*	*	*	*
EXG	Exchange Register	Rx ↔ Ry	—	—	—	—	—
EXT	Sign Extend	(Destination) Sign-Extended → Destination	—	*	*	0	0
JMP	Jump	Destination → PC	—	—	—	—	—
JSR	Jump to Subroutine	PC → −(SP); Destination → PC	—	—	—	—	—
LEA	Load Effective Address	<ea> → An	—	—	—	—	—
LINK	Link and Allocate	An → (SP); SP → An; SP + Displacement → SP	—	—	—	—	—
LSL, LSR	Logical Shift	(Destination) Shifted by <count> → Destination	*	*	*	0	*
MOVE	Move Data from Source to Destination	(Source) → Destination	—	*	*	0	0
MOVE to CCR	Move to Condition Code	(Source) → CCR	*	*	*	*	*
MOVE to SR	Move to the Status Register	(Source) → SR	*	*	*	*	*
MOVE from SR	Move from the Status Register	SR → Destination	—	—	—	—	—
MOVE USP	Move User Stack Pointer	USP → An; An → USP	—	—	—	—	—
MOVEA	Move Address	(Source) → Destination	—	—	—	—	—
MOVEM	Move Multiple Registers	Register → Destination (Source) → Registers	—	—	—	—	—
MOVEP	Move Peripheral Data	(Source) → Destination	—	—	—	—	—
MOVEQ	Move Quick	Immediate Data → Destination	—	*	*	0	0
MULS	Signed Multiply	(Destination)X(Source) → Destination	—	*	*	0	0
MULU	Unsigned Multiply	(Destination)X(Source) → Destination	—	*	*	0	0
NBCD	Negate Decimal with Extend	0 − (Destination)$_{10}$ − X → Destination	*	U	*	U	*
NEG	Negate	0 − (Destination) → Destination	*	*	*	*	*
NEGX	Negate with Extend	0 − (Destination) − X → Destination	*	*	*	*	*
NOP	No Operation	—	—	—	—	—	—
NOT	Logical Complement	~ (Destination) → Destination	—	*	*	0	0
OR	Inclusive OR Logical	(Destination) ∨ (Source) → Destination	—	*	*	0	0
ORI	Inclusive OR Immediate	(Destination) ∨ Immediate Data → Destination	—	*	*	0	0
ORI to CCR	Inclusive OR Immediate to Condition Codes	(Source) ∨ CCR → CCR	*	*	*	*	*
ORI to SR	Inclusive OR Immediate to Status Register	(Source) ∨ SR → SR	*	*	*	*	*
PEA	Push Effective Address	<ea> → − (SP)	—	—	—	—	—
RESET	Reset External Device	—	—	—	—	—	—
ROL, ROR	Rotate (Without Extend)	(Destination) Rotated by <count> → Destination	—	*	*	0	*

NOTES:

Λ = logical AND
∨ = logical OR
⊕ = logical exclusive OR
~ = logical complement

* = affected
— = unaffected
0 = cleared
1 = set
U = undefined

Table 22. Instruction Set (Continued)

Mnemonic	Description	Operation	Condition Codes				
			X	N	Z	V	C
ROXL, ROXR	Rotate with Extend	(Destination) Rotated by <count> →Destination	*	*	*	0	*
RTE	Return from Exception	(SP) + →SR; (SP) + →PC	*	*	*	*	*
RTR	Return and Restore Condition Codes	(SP) + →CC; (SP) + →PC	*	*	*	*	*
RTS	Return from Subroutine	(SP) + →PC	—	—	—	—	—
SBCD	Subtract Decimal with Extend	$(Destination)_{10}$ − $(Source)_{10}$ − X →Destination	*	U	*	U	*
Scc	Set According to Condition	If cc then 1's →Destination else 0's →Destination	—	—	—	—	—
STOP	Load Status Register and Stop	Immediate Data →SR; STOP	*	*	*	*	*
SUB	Subtract Binary	(Destination) − (Source) →Destination	*	*	*	*	*
SUBA	Subtract Address	(Destination) − (Source) →Destination	—	—	—	—	—
SUBI	Subtract Immediate	(Destination) − Immediate Data →Destination	*	*	*	*	*
SUBQ	Subtract Quick	(Destination) − Immediate Data →Destination	*	*	*	*	*
SUBX	Subtract with Extend	(Destination) − (Source) − X →Destination	*	*	*	*	*
SWAP	Swap Register Halves	Register [31:16]↔Register [15:0]	—	*	*	0	0
TAS	Test and Set an Operand	(Destination) Tested →CC; 1 →[7] OF Destination	—	*	*	0	0
TRAP	Trap	PC →− (SSP); SR →− (SSP); (Vector) →PC	—	—	—	—	—
TRAPV	Trap on Overflow	If ν then TRAP	—	—	—	—	—
TST	Test and Operand	(Destination) Tested →CC	—	*	*	0	0
UNLK	Unlink	An →SP; (SP) + →An	—	—	—	—	—

NOTES:

[ ]	= bit number	*	= affected
Λ	= logical AND	—	= unaffected
ν	= logical OR	0	= cleared
$\oplus$	= logical exclusive OR	1	= set
~	= logical complement	U	= undefined

Note

The number of periods includes instruction fetch and all applicable operand fetches and stores.

EFFECTIVE ADDRESS OPERAND CALCULATION TIMING

Table 23 lists the number of clock periods required to compute an instruction's effective address. It includes fetching of any extension words, the address computation, and fetching of the memory operand. The number of bus read and write cycles is shown in parenthesis as (r/w). Note there are no write cycles involved in processing the effective address.

MOVE INSTRUCTION CLOCK PERIODS

Tables 24 and 25 indicate the number of clock periods for the move instruction. This data includes instruction fetch, operand reads, and operand writes. The number of bus read and write cycles is shown in parenthesis as (r/w).

STANDARD INSTRUCTION CLOCK PERIODS

The number of clock periods shown in Table 26 delineate the time required to perform the operations, store the results, and read the next instruction. The number of bus read and write cycles is shown in parenthesis as (r/w). The number of clock periods and the number of read and write cycles must be added respectively to those of the effective address calculation where indicated.

In Table 26, the headings have the following meanings: An = address register operand, Dn = data register operand, ea = an operand specified by an effective address, and M = memory effective address operand.

IMMEDIATE INSTRUCTION CLOCK PERIODS

The number of clock periods shown in Table 27 includes the time to fetch immediate operands, perform the operations, store the results, and read the next operation. The number of bus read and write cycles is shown in parenthesis as (r/w). The number

Table 23. Effective Address Calculation Timing

Addressing Mode		Byte, Word	Long
	Register		
Dn	Data Register Direct	0(0/0)	0(0/0)
An	Address Register Direct	0(0/0)	0(0/0)
	Memory		
(An)	Address Register Indirect	4(1/0)	8(2/0)
(An)+	Address Register Indirect with Postincrement	4(1/0)	8(2/0)
−(An)	Address Register Indirect with Predecrement	6(1/0)	10(2/0)
d(An)	Address Register Indirect with Displacement	8(2/0)	12(3/0)
d(An, ix)*	Address Register Indirect with Index	10(2/0)	14(3/0)
xxx.W	Absolute Short	8(2/0)	12(3/0)
xxx.L	Absolute Long	12(3/0)	16(4/0)
d(PC)	Program Counter with Displacement	8(2/0)	12(3/0)
d(PC, ix)*	Program Counter with Index	10(2/0)	14(3/0)
#xxx	Immediate	4(1/0)	8(2/0)

*The size of the index register (ix) does not affect execution time.

Table 24. Move Byte and Word Instruction Clock Periods

	Destination								
Source	**Dn**	**An**	**(An)**	**(An)+**	**−(An)**	**d(An)**	**d(An, ix)***	**xxx.W**	**xxx.L**
Dn	4(1/0)	4(1/0)	8(1/1)	8(1/1)	8(1/1)	12(2/1)	14(2/1)	12(2/1)	16(3/1)
An	4(1/0)	4(1/0)	8(1/1)	8(1/1)	8(1/1)	12(2/1)	14(2/1)	12(2/1)	16(3/1)
(An)	8(2/0)	8(2/0)	12(2/1)	12(2/1)	12(2/1)	16(3/1)	18(3/1)	16(3/1)	20(4/1)
(An)+	8(2/0)	8(2/0)	12(2/1)	12(2/1)	12(2/1)	16(3/1)	18(3/1)	16(3/1)	20(4/1)
−(An)	10(2/0)	10(2/0)	14(2/1)	14(2/1)	14(2/1)	18(3/1)	20(3/1)	18(3/1)	22(4/1)
d(An)	12(3/0)	12(3/0)	16(3/1)	16(3/1)	16(3/1)	20(4/1)	22(4/1)	20(4/1)	24(5/1)
d(An, ix)*	14(3/0)	14(3/0)	18(3/1)	18(3/1)	18(3/1)	22(4/1)	24(4/1)	22(4/1)	26(5/1)
xxx.W	12(3/0)	12(3/0)	16(3/1)	16(3/1)	16(3/1)	20(4/1)	22(4/1)	20(4/1)	24(5/1)
xxx.L	16(4/0)	16(4/0)	20(4/1)	20(4/1)	20(4/1)	24(5/1)	26(5/1)	24(5/1)	28(6/1)
d(PC)	12(3/0)	12(3/0)	16(3/1)	16(3/1)	16(3/1)	20(4/1)	22(4/1)	20(4/1)	24(5/1)
d(PC, ix)*	14(3/0)	14(3/0)	18(3/1)	18(3/1)	18(3/1)	22(4/1)	24(4/1)	22(4/1)	26(5/1)
#xxx	8(2/0)	8(2/0)	12(2/1)	12(2/1)	12(2/1)	16(3/1)	18(3/1)	16(3/1)	20(4/1)

*The size of the index register (ix) does not affect execution time

of clock periods and the number of read and write cycles must be added respectively to those of the effective adress calculation where indicated.

In Table 27, the headings have the following meanings: # = immediate operand, Dn = data register operand, An = address register operand, M = memory operand, and SR = status register.

SINGLE OPERAND INSTRUCTION CLOCK PERIODS

Table 28 indicates the number of clock periods for the single operand instructions. The number of bus read and write cycles is shown in parenthesis as (r/w). The number of clock periods and the number of read and write cycles must be added respectively to those of the effective address calculation where indicated.

Table 25. Move Long Instruction Clock Periods

Source	Destination								
	Dn	An	(An)	(An)+	−(An)	d(An)	d(An, ix)*	xxx.W	xxx.L
Dn	4(1/0)	4(1/0)	12(1/2)	12(1/2)	12(1/2)	16(2/2)	18(2/2)	16(2/2)	20(3/2)
An	4(1/0)	4(1/0)	12(1/2)	12(1/2)	12(1/2)	16(2/2)	18(2/2)	16(2/2)	20(3/2)
(An)	12(3/0)	12(3/0)	20(3/2)	20(3/2)	20(3/2)	24(4/2)	26(4/2)	24(4/2)	28(5/2)
(An)+	12(3/0)	12(3/0)	20(3/2)	20(3/2)	20(3/2)	24(4/2)	26(4/2)	24(4/2)	28(5/2)
−(An)	14(3/0)	14(3/0)	22(3/2)	22(3/2)	22(3/2)	26(4/2)	28(4/2)	26(4/2)	30(5/2)
d(An)	16(4/0)	16(4/0)	24(4/2)	24(4/2)	24(4/2)	28(5/2)	30(5/2)	28(5/2)	32(6/2)
d(An, ix)*	18(4/0)	18(4/0)	26(4/2)	26(4/2)	26(4/2)	30(5/2)	32(5/2)	30(5/2)	34(6/2)
xxx.W	16(4/0)	16(4/0)	24(4/2)	24(4/2)	24(4/2)	28(5/2)	30(5/2)	28(5/2)	32(6/2)
xxx.L	20(5/0)	20(5/0)	28(5/2)	28(5/2)	28(5/2)	32(6/2)	34(6/2)	32(6/2)	36(7/2)
d(PC)	16(4/0)	16(4/0)	24(4/2)	24(4/2)	24(4/2)	28(5/2)	30(5/2)	28(5/2)	32(5/2)
d(PC, ix)*	18(4/0)	18(4/0)	26(4/2)	26(4/2)	26(4/2)	30(5/2)	32(5/2)	30(5/2)	34(6/2)
#xxx	12(3/0)	12(3/0)	20(3/2)	20(3/2)	20(3/2)	24(4/2)	26(4/2)	24(4/2)	28(5/2)

*The size of the index register (ix) does not affect execution time.

Table 26. Standard Instruction Clock Periods

Instruction	Size	op<ea>, An†	op<ea>, Dn	op Dn, <M>
ADD	Byte, Word	8(1/0)+	4(1/0)+	8(1/1)+
	Long	6(1/0)+**	6(1/0)+**	12(1/2)+
AND	Byte, Word	—	4(1/0)+	8(1/1)+
	Long	—	6(1/0)+**	12(1/2)+
CMP	Byte, Word	6(1/0)+	4(1/0)+	—
	Long	6(1/0)+	6(1/0)+	—
DIVS	—	—	158(1/0)+*	—
DIVU	—	—	140(1/0)+*	—
EOR	Byte, Word	—	4(1/0)***	8(1/1)+
	Long	—	8(1/0)***	12(1/2)+
MULS	—	—	70(1/0)+*	—
MULU	—	—	70(1/0)+*	—
OR	Byte, Word	—	4(1/0)+	8(1/1)+
	Long	—	6(1/0)+**	12(1/2)+
SUB	Byte, Word	8(1/0)+	4(1/0)+	8(1/1)+
	Long	6(1/0)+**	6(1/0)+**	12(1/2)+

NOTES:
+ add effective address calculation time
† word or long only
* indicates maximum value
** The base time of six clock periods is increased to eight if the effective address mode is register direct or immediate (effective address time should also be added).
*** Only available effective address mode is data register direct
DIVS, DIVU The divide algorithm used by the R68000 provides less than 10% difference between the best and worst case timings.
MULS, MULU The multiply algorithm requires 38 + 2n clocks where n is defined as:
MULU: n = the number of ones in each <ea>
MULU: n = concatanate the <ea> with a zero as the LSB; n is the resultant number of 10 or 01 patterns in the 17-bit source; i.e., worst case happens when the source is $5555.

Table 27. Immediate Instruction Clock Periods

Instruction	Size	op #, Dn	op #, An	op #, M
ADDI	Byte, Word	8(2/0)	—	12(2/1) +
	Long	16(3/0)	—	20(3/2) +
ADDQ	Byte, Word	4(1/0)	8(1/0)*	8(1/1) +
	Long	8(1/0)	8(1/0)	12(1/2) +
ANDI	Byte, Word	8(2/0)	—	12(2/1) +
	Long	16(3/0)	—	20(3/1) +
CMPI	Byte, Word	8(2/0)	—	8(2/0) +
	Long	14(3/0)	—	12(3/0) +
EORI	Byte, Word	8(2/0)	—	12(2/1) +
	Long	16(3/0)	—	20(3/2) +
MOVEQ	Long	4(1/0)	—	—
ORI	Byte, Word	8(2/0)	—	12(2/1) +
	Long	16(3/0)	—	20(3/2) +
SUBI	Byte, Word	8(2/0)	—	12(2/1) +
	Long	16(3/0)	—	20(3/2) +
SUBQ	Byte, Word	4(1/0)	8(1/0)*	8(1/1) +
	Long	8(1/0)	8(1/0)	12(1/2) +

\+ add effective address calculation time
* word only

Table 28. Single Operand Instruction Clock Periods

Instruction	Size	Register	Memory
CLR	Byte, Word	4(1/0)	8(1/1) +
	Long	6(1/0)	12(1/2) +
NBCD	Byte	6(1/0)	8(1/1) +
NEG	Byte, Word	4(1/0)	8(1/1) +
	Long	6(1/0)	12(1/2) +
NEGX	Byte, Word	4(1/0)	8(1/1) +
	Long	6(1/0)	12(1/2) +
NOT	Byte, Word	4(1/0)	8(1/1) +
	Long	6(1/0)	12(1/2) +
Scc	Byte, False	4(1/0)	8(1/1) +
	Byte, True	6(1/0)	8(1/1) +
TAS	Byte	4(1/0)	10(1/1) +
TST	Byte, Word	4(1/0)	4(1/0) +
	Long	4(1/0)	4(1/0) +

\+ add effective address calculation time

SHIFT/ROTATE INSTRUCTION CLOCK PERIODS

Table 29 delineates the number of clock periods for the shift and rotate instructions. The number of bus read and write cycles is shown in parenthesis as: (r/w). The number of clock periods and the number of read and write cycles must be added respectively to those of the effective address calculation where indicated.

BIT MANIPULATION INSTRUCTION CLOCK PERIODS

Table 30 indicates the number of clock periods required for the bit manipulation instructions. The number of bus read and write cycles is shown in parenthesis as: (r/w). The number of clock periods and the number of read and write cycles must be added respectively to those of the effective address calculation where indicated.

CONDITIONAL INSTRUCTION CLOCK PERIODS

Table 31 delineates the number of clock periods required for the conditional instructions. The number of bus read and write cycles is indicated in parenthesis as: (r/w). The number of clock periods and the number of read and write cycles must be added respectively to those of the effective address calculation where indicated.

JMP, JSR, LEA, PWA, MOVEM INSTRUCTION CLOCK PERIODS

Table 32 indicates the number of clock periods required for the jump, jump to subroutine, load effective address, push effective address, and move multiple registers instructions. The number of bus read and write cycles is shown in parenthesis as: (r/w).

Table 29. Shift/Rotate Instruction Clock Periods

Instruction	Size	Register	Memory
ASR, ASL	Byte, Word	**6** + **2n**(1/0)	**8**(1/1) +
	Long	**8** + **2n**(1/0)	—
LSR, LSL	Byte, Word	**6** + **2n**(1/0)	**8**(1/1) +
	Long	**8** + **2n**(1/0)	—
ROR, ROL	Byte, Word	**6** + **2n**(1/0)	**8**(1/1) +
	Long	**8** + **2n**(1/0)	—
ROXR, ROXL	Byte, Word	**6** + **2n**(1/0)	**8**(1/1) +
	Long	**8** + **2n**(1/0)	—

+ add effective address calculation time
n is shift or rotate count

Table 30. Bit Manipulation Instruction Clock Periods

Instruction	Size	Dynamic		Static	
		Register	Memory	Register	Memory
BCHG	Byte	—	**8**(1/1) +	—	**12**(2/1) +
	Long	**8**(1/0)*	—	**12**(2/0)*	—
BCLR	Byte	—	**8**(1/1) +	—	**12**(2/1) +
	Long	**10**(1/0)*	—	**14**(2/0)*	—
BSET	Byte	—	**8**(1/1) +	—	**12**(2/1) +
	Long	**8**(1/0)*	—	**12**(2/0)*	—
BTST	Byte	—	**4**(1/0) +	—	**8**(2/0) +
	Long	**6**(1/0)	—	**10**(2/0)	—

+ add effective address calculation time
* indicates maximum value

Table 31. Conditional Instruction Clock Periods

Instruction	Displacement	Branch Taken	Branch Not Taken
B_{CC}	Byte	10(2/0)	8(1/0)
	Word	10(2/0)	12(2/0)
BRA	Byte	10(2/0)	—
	Word	10(2/0)	—
BSR	Byte	18(2/2)	—
	Word	18(2/2)	—
DB_{CC}	CC true	—	12(2/0)
	CC false	10(2/0)	14(3/0)

Table 32. JMP, JSR, LEA, PEA, MOVEM INSTRUCTION CLOCK PERIODS

Instr	Size	(An)	(An)+	−(An)	d(An)	d(An, ix)* +	xxx.W	xxx.L	d(PC)	d(PC, ix)*
JMP	—	8(2/0)	—	—	10(2/0)	14(3/0)	10(2/0)	12(3/0)	10(2/0)	14(3/0)
JSR	—	16(2/2)	—	—	18(2/2)	22(2/2)	18(2/2)	20(3/2)	18(2/2)	22(2/2)
LEA	—	4(1/0)	—	—	8(2/0)	12(2/0)	8(2/0)	12(3/0)	8(2/0)	12(2/0)
PEA	—	12(1/2)	—	—	16(2/2)	20(2/2)	16(2/2)	20(3/2)	16(2/2)	20(2/2)
MOVEM M → R	Word	12 + 4n (3 + n/0)	12 + 4n (3 + n/0)	—	16 + 4n (4 + n/0)	18 + 4n (4 + n/0)	16 + 4n (4 + n/0)	20 + 4n (5 + n/0)	16 + 4n (4 + n/0)	18 + 4n (4 + n/0)
	Long	12 + 8n (3 + 2n/0)	12 + 8n (3 + 2n/0)	—	16 + 8n (4 + 2n/0)	18 + 8n (4 + 2n/0)	16 + 8n (4 + 2n/0)	20 + 8n (5 + 2n/0)	16 + 8n (4 + 2n/0)	18 + 8n (4 + 2n/0)
MOVEM R → M	Word	8 + 4n (2/n)	—	8 + 4n (2/n)	12 + 4n (3/n)	14 + 4n (3/n)	12 + 4n (3/n)	16 + 4n (4/n)	— —	— —
	Long	8 + 8n (2/2n)	— —	8 + 8n (2/2n)	12 + 8n (3/2n)	14 + 8n (3/2n)	12 + 8n (3/2n)	16 + 8n (4/2n)	— —	— —

n is the number of registers to move
* The size of the index register (ix) does not affect the instruction's execution time

MULTI-PRECISION INSTRUCTION CLOCK PERIODS

Table 33 delineates the number of clock periods for the multi-precision instructions. The number of clock periods includes the time to fetch both operands, perform the operations, store the results, and read the next instructions. The number of read and write cycles is shown in parenthesis as: (r/w).

In Table 33, the headings have the following meanings: Dn = data register operand and M = memory operand.

Table 33. Multi-Precision Instruction Clock Periods

Instruction	Size	op Dn, Dn	op M, M
ADDX	Byte, Word	4(1/0)	18(3/1)
	Long	8(1/0)	30(5/2)
CMPM	Byte, Word	—	12(3/0)
	Long		20(5/0)
SUBX	Byte, Word	4(1/0)	18(3/1)
	Long	8(1/0)	30(5/2)
ABCD	Byte	6(1/0)	18(3/1)
SBCD	Byte	6(1/0)	18(3/1)

MISCELLANEOUS INSTRUCTION CLOCK PERIODS

Table 34 and 35 indicate the number of clock periods for the following miscellaneous instructions. The number of bus read and write cycles is shown in parenthesis as: (r/w). The number of clock periods plus the number of read and write cycles must be added to those of the effective address calculation where indicated.

EXCEPTION PROCESSING CLOCK PERIODS

Table 36 delineates the number of clock periods for exception processing. The number of clock periods includes the time for all stacking, the vector fetch, and the fetch of the first instruction of the handler routine. The number of bus read and write cycles is shown in parenthesis as (r/w)

Table 34. Miscellaneous Instruction Clock Periods

Instruction	Size	Register	Memory	Instruction	Size	Register	Memory
ANDI to CCR	Byte	**20**(3/0)	—	LINK	—	**16**(2/2)	—
ANDI to SR	Word	**20**(3/0)	—	MOVE from USP	—	**4**(1/0)	—
CHK	—	**10**(1/0) +	—	MOVE to USP	—	**4**(1/0)	—
EORI to CCR	Byte	**20**(3/0)	—	NOP	—	**4**(1/0)	—
EORI to SR	Word	**20**(3/0)	—	RESET	—	**132**(1/0)	—
ORI to CCR	Byte	**20**(3/0)	—	RTE	—	**20**(5/0)	—
ORI to SR	Word	**20**(3/0)	—	RTR	—	**20**(5/0)	—
MOVE from SR	—	**6**(1/0)	**8**(1/1) +	RTS	—	**16**(4/0)	—
MOVE to CCR	—	**12**(2/0)	**12**(2/0) +	STOP	—	**4**(0/0)	—
MOVE to SR	—	**12**(2/0)	**12**(2/0) +	SWAP	—	**4**(1/0)	—
EXG	—	**6**(1/0)	—	TRAPV	—	**4**(1/0)	—
EXT	Word	**4**(1/0)	—	UNLK	—	**12**(3/0)	—
	Long	**4**(1/0)	—				
+ add effective address calculation time							

Table 35. Move Peripheral Instruction Execution Times

Instruction	Size	Register→Memory	Memory→Register
MOVEP	Word	**16**(2/2)	**16**(4/0)
	Long	**24**(2/4)	**24**(6/0)

Table 36. Exception Processing Clock Periods

Exception	Periods
Address Error	**50**(4/7)
Bus Error	**50**(4/7)
CHK Instruction	**44**(5/4) +
Divide by Zero	**42**(5/4)
Illegal Instruction	**34**(4/3)
Interrupt	**44**(5/3)*
Privilege Violation	**34**(4/3)
$\overline{\text{RESET}}$**	**40**(6/0)
Trace	**34**(4/3)
TRAP Instruction	**38**(4/4)
TRAPV Instruction	**34**(4/3)

+ add effective address calculation time
* The interrupt acknowledge cycle is assumed to take four clock periods
** Indicates the time from when $\overline{\text{RESET}}$ and $\overline{\text{HALT}}$ are first sampled as negated to when instruction execution starts

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to +7.0	V
Input Voltage	V_{IN}	−0.3 to +7.0	V
Operating Temperature Range	T_A	T_L to T_H 0 to 70	°C
Storage Temperature	T_{STG}	−56 to 150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Thermal Resistance 64-Pin Ceramic 64-Pin Plastic Dip	θ_{JA}	 30 55 ±5	 °C/W °C/W

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{CC}.

POWER CONSIDERATIONS

The average chip-junction temperature, T_J, in °C can be obtained from:

$$T_J = T_A + (P_D \cdot \theta_{JA}) \quad (1)$$

Where:

$T_A \equiv$ Ambient Temperature, °C

$\theta_{JA} \equiv$ Package Thermal Resistance, Junction-to-Ambient, °C/W

$P_D \equiv P_{INT} + P_{I/O}$

$P_{INT} \equiv I_{CC} \cdot V_{CC}$, Watts—Chip Internal Power

$P_{I/O} \equiv$ Power Dissipation on Input and Output Pins—User Determined

For most applications $P_{I/O} \ll P_{INT}$ and can be neglected.

An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = K - (T_J + 273°C) \quad (2)$$

Solving equations 1 and 2 for K gives:

$$K = P_D \cdot (T_A + 273°C) + \theta_{JA} \cdot P_D^2 \quad (3)$$

Where K is a constant pertaining to the particular part. K can be determined from equation 3 by measuring P_D (at equilibrium) for a known T_A. Using this value of K the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A.

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0 Vdc ±5%, V_{SS} = 0 Vdc, T_A = T_L to T_H °C. See Figures 41, 42, and 43.

Characteristic	Symbol	Min	Max	Unit	Test Conditions
Input High Voltage	V_{IH}	2.0	V_{CC}	V	
Input Low Voltage	V_{IL}	V_{SS} − 0.3	0.8	V	
Input Leakage Current $\overline{BERR}$, $\overline{BGACK}$, $\overline{BR}$, $\overline{DTACK}$, CLK, $\overline{IPL0}$-$\overline{IPL2}$ $\overline{VPA}$, $\overline{HALT}$, $\overline{RESET}$	I_{IN}	 — —	 2.5 20	 μA μA	 V_{IN} = 5.25 V_{CC} = OV
Three-State (Off State) Input Current AS, A1–A23, D0–D15, FC0–FC2, $\overline{LDS}$, R/$\overline{W}$, $\overline{UDS}$, $\overline{VMA}$	I_{TSI}	—	20	μA	V_{IN} = 0.4V to 2.4V V_{CC} = 5.25V
Output High Voltage E* E, $\overline{AS}$, A1–A23, $\overline{BG}$, D0–D15, FC0–FC2, $\overline{LDS}$, R/$\overline{W}$, $\overline{UDS}$, $\overline{VMA}$	V_{OH}	 V_{CC} − 0.75 2.4	 — —	 V V	 V_{CC} = 4.75V I_{OH} = −400 μA
Output Low Voltage $\overline{HALT}$ $\overline{BG}$, FC0–FC2, A1–A23 $\overline{RESET}$ $\overline{AS}$, D0–D15, $\overline{LDS}$, R/$\overline{W}$ $\overline{UDS}$, $\overline{VMA}$	V_{OL}	 — — — —	 0.6 0.5 0.5 0.5	 V V V V	 V_{CC} = 4.75V (I_{OL} = 1.6 mA) (I_{OL} = 3.2 mA) (I_{OL} = 5.0 mA) (I_{OL} = 5.3 mA)
Power Dissipation	P_D***	—	1.5	W	
Input Capacitance	C_{IN}	—	20.0	pF	V_{CC} = 5.0V, V_{IN} = OV f = 1 MHz, T_A = 25°C

*With external pullup resistor of 1.1 kΩ

**Capacitance is periodically sampled rather than 100% tested.

***During normal operation instantaneous V_{CC} current requirements may be as high as 1.5A

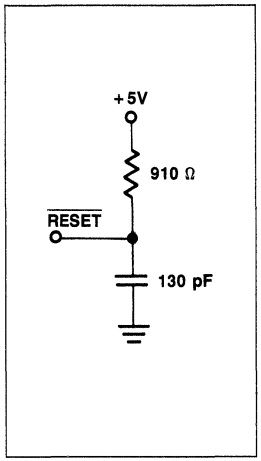


Figure 41. $\overline{\text{RESET}}$ Test Load

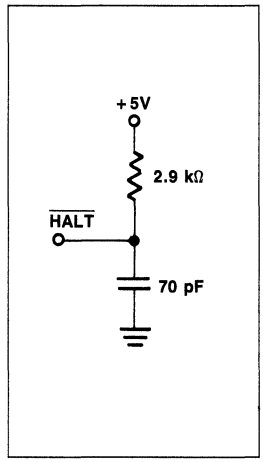


Figure 42. $\overline{\text{HALT}}$ Test Load

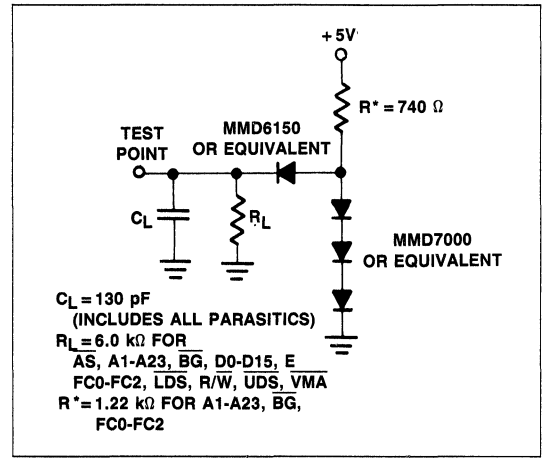


Figure 43. Test Loads

CLOCK TIMING (See Figure 44)

Characteristic	Symbol	4 MHz		6 MHz		8 MHz		10 MHz		12.5 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Frequency of Operation	F	2.0	4.0	2.0	6.0	2.0	8.0	2.0	10.0	4.0	12.5	MHz
Cycle Time	t_{cyc}	250	500	167	500	125	500	100	500	80	250	ns
Clock Pulse Width	t_{CL} t_{CH}	115 115	250 250	75 75	250 250	55 55	250 250	45 45	250 250	35 35	125 125	ns
Rise and Fall Times	t_{Cr} t_{Cf}	— —	10 10	— —	10 10	— —	10 10	— —	10 10	— —	5 5	ns

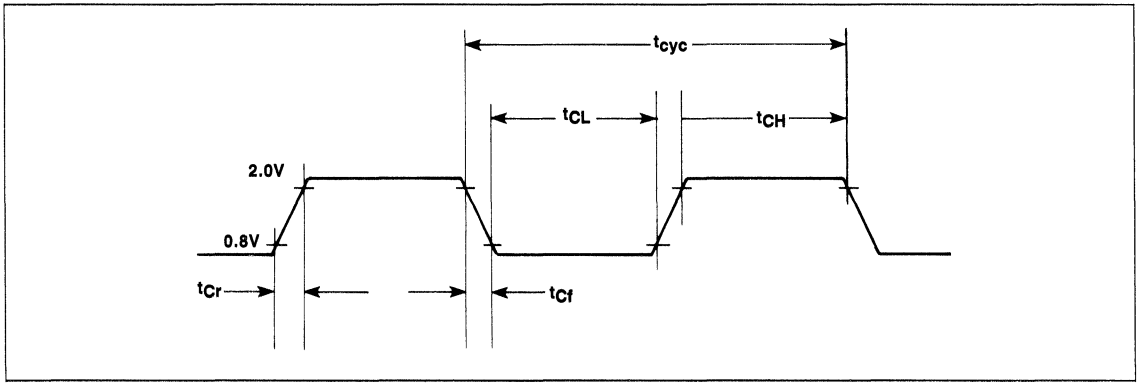


Figure 44. Input Clock Waveform

AC ELECTRICAL SPECIFICATIONS — READ AND WRITE CYCLES

(V_{CC} = 5.0 Vdc ±5%, V_{SS} = 0 Vdc; T_A = T_L to T_H, see Figures 45 and 46)

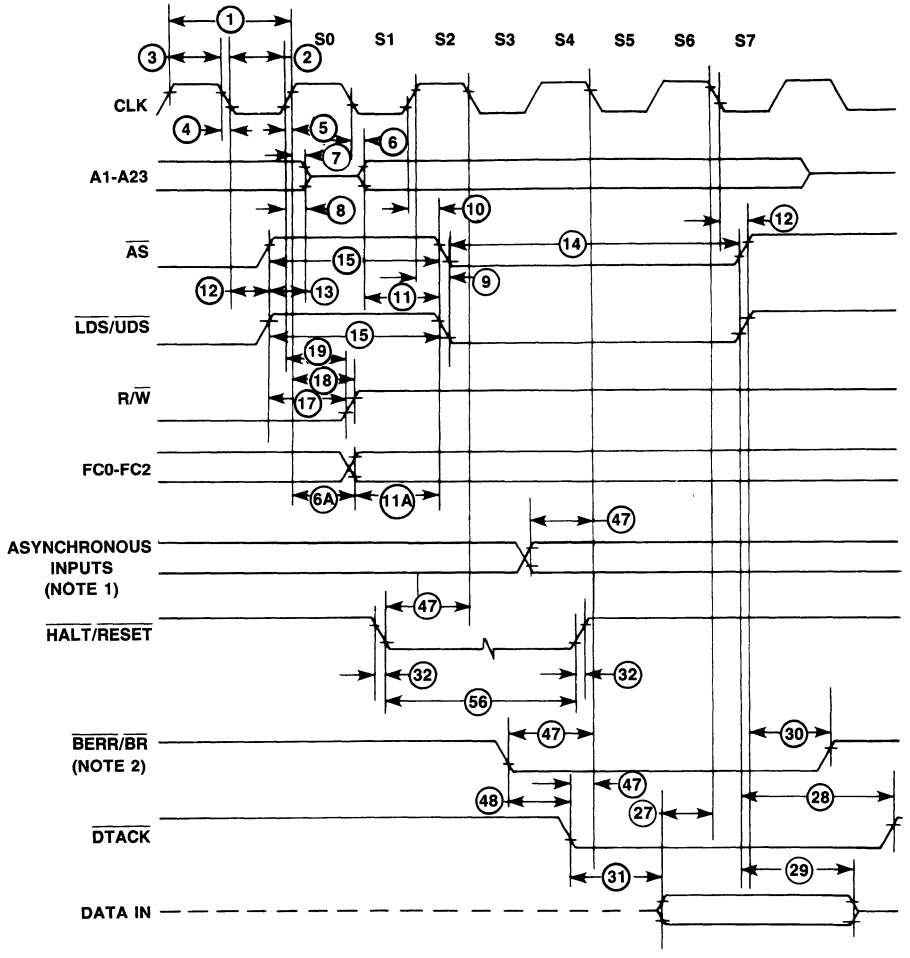
Num.	Characteristic	Symbol	4 MHz		6 MHz		8 MHz		10 MHz		12.5 MHz		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
1	Clock Period	t_{cyc}	250	500	167	500	125	500	100	500	80	250	ns
2	Clock Width Low	t_{CL}	115	250	75	250	55	250	45	250	35	125	ns
3	Clock Width High	t_{CH}	115	250	75	250	55	250	45	250	35	125	ns
4	Clock Fall Time	t_{Cf}	—	10	—	10	—	10	—	10	—	5	ns
5	Clock Rise Time	t_{Cr}	—	10	—	10	—	10	—	10	—	5	ns
6	Clock Low to Address	t_{CLAV}	—	90	—	80	—	70	—	60	—	55	ns
6A	Clock High to FC Valid	t_{CHFCV}	—	90	—	80	—	70	—	60	—	55	ns
7	Clock High to Address Data High Impedance (Maximum)	t_{CHAZx}	—	120	—	100	—	80	—	70	—	60	ns
8	Clock High to Address/FC Invalid (Minimum)	t_{CHAZn}	0	—	0	—	0	—	0	—	0	—	ns
9[1]	Clock High to $\overline{AS}$, $\overline{DS}$ Low (Maximum)	t_{CHSLx}	—	80	—	70	—	60	—	55	—	55	ns
10	Clock High to $\overline{AS}$, $\overline{DS}$ Low (Minimum)	t_{CHSLn}	0	—	0	—	0	—	0	—	0	—	ns
11[2]	Address to $\overline{AS}$, $\overline{DS}$ (Read) Low/$\overline{AS}$ Write	t_{AVSL}	55	—	35	—	30	—	20	—	0	—	ns
11A[2]	FC Valid to $\overline{AS}$, $\overline{DS}$ (Read) Low/$\overline{AS}$ Write	t_{FCVSL}	80	—	70	—	60	—	50	—	40	—	ns
12[1]	Clock Low to $\overline{AS}$, $\overline{DS}$ High	t_{CLSH}	—	90	—	80	—	70	—	55	—	50	ns
13[2]	$\overline{AS}$, $\overline{DS}$ High to Address/FC Invalid	t_{SHAZ}	60	—	40	—	30	—	20	—	10	—	ns
14[2]	$\overline{AS}$, $\overline{DS}$ Width Low (Read)/$\overline{AS}$ Write	t_{SL}	535	—	337	—	240	—	195	—	160	—	ns
14A[2]	$\overline{DS}$ Width Low (Write)	t_{DWPW}	285	—	170	—	115	—	95	—	80	—	ns
15[2]	$\overline{AS}$, $\overline{DS}$ Width High	t_{SH}	285	—	180	—	150	—	105	—	65	—	ns
16	Clock High to $\overline{AS}$, $\overline{DS}$ High	t_{CHSZ}	—	120	—	100	—	80	—	70	—	60	ns
17[2]	$\overline{AS}$, $\overline{DS}$ High to R/$\overline{W}$ High	t_{SHRH}	60	—	50	—	40	—	20	—	10	—	ns
18[1]	Clock High to R/$\overline{W}$ High (Maximum)	t_{CHRHx}	—	90	—	80	—	70	—	60	—	60	ns
19	Clock High to R/$\overline{W}$ High (Minimum)	t_{CHRHn}	0	—	0	—	0	—	0	—	0	—	ns
20[1]	Clock High to R/$\overline{W}$ Low	t_{CHRL}	—	90	—	80	—	70	—	60	—	60	ns
20A[6]	$\overline{AS}$ Low to R/$\overline{W}$ Valid	t_{ASRV}	—	20	—	20	—	20	—	20	—	20	ns
21[2]	Address Valid to R/$\overline{W}$ Low	t_{AVRL}	45	—	25	—	20	—	0	—	0	—	ns
21A[2]	FC Valid to R/$\overline{W}$ Low	t_{FCVRL}	80	—	70	—	60	—	50	—	30	—	ns
22[2]	R/$\overline{W}$ Low to $\overline{DS}$ Low (Write)	t_{RLSL}	200	—	140	—	80	—	50	—	30	—	ns
23	Clock Low to Data Out Valid	t_{CLDO}	—	90	—	80	—	70	—	55	—	55	ns
24	Clock High to R/$\overline{W}$, $\overline{VMA}$ High Impedance	t_{CHRZ}	—	120	—	100	—	80	—	70	—	60	ns
25[2]	$\overline{DS}$ High to Data Out Invalid	t_{SHDO}	60	—	40	—	30	—	20	—	15	—	ns
26[2]	Data Out Valid to $\overline{DS}$ Low (Write)	t_{DOSL}	55	—	35	—	30	—	20	—	15	—	ns
27[5]	Data In to Clock Low (Setup Time)	t_{DICL}	30	—	25	—	15	—	10	—	10	—	ns
27A	Late $\overline{BERR}$ Low to Clock Low (Setup Time)	t_{BELCL}	45	—	45	—	45	—	45	—	45	—	ns
28[2]	$\overline{AS}$, $\overline{DS}$ High to $\overline{DTACK}$ High	t_{SHDAH}	0	490	0	325	0	245	0	190	0	150	ns

AC ELECTRICAL SPECIFICATIONS — READ AND WRITE CYCLES (CONTINUED)

Num.	Characteristic	Symbol	4 MHz		6 MHz		8 MHz		10 MHz		12.5 MHz		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
29	$\overline{DS}$ High to Data Invalid (Hold Time)	t_{SHDI}	0	—	0	—	0	—	0	—	0	—	ns
30	$\overline{AS}$, $\overline{DS}$ High to $\overline{BERR}$ High	t_{SHBEH}	0	—	0	—	0	—	0	—	0	—	ns
31[2]	$\overline{DTACK}$ Low to Data In (Setup Time)	t_{DALDI}	—	180	—	120	—	90	—	65	—	50	ns
32	$\overline{HALT}$ and $\overline{RESET}$ Input Transition Time	$t_{RHr,f}$	0	200	0	200	0	200	0	200	0	200	ns
33	Clock High to $\overline{BG}$ Low	t_{CHGL}	—	90	—	80	—	70	—	60	—	50	ns
34	Clock High to $\overline{BG}$ High	t_{CHGH}	—	90	—	80	—	70	—	60	—	50	ns
35	$\overline{BR}$ Low to $\overline{BG}$ Low	t_{BRLGL}	1.5	3.5	1.5	3.5	1.5	3.5	1.5	3.5	1.5	3.5	Clk Per.
36	$\overline{BR}$ High to $\overline{BG}$ High	t_{BRHGH}	1.5	3.5	1.5	3.5	1.5	3.5	1.5	3.5	1.5	3.5	Clk. Per.
37	$\overline{BGACK}$ Low to $\overline{BG}$ High	t_{GALGH}	1 5	3.0	1.5	3.0	1 5	3 0	1 5	3.0	1 5	3 0	Clk. Per.
37A	$\overline{BGACK}$ Low to $\overline{BR}$ High (to Prevent Rearbitration)	t_{BGKBR}	30	—	25	—	20	—	20	—	20	—	ns
38	$\overline{BG}$ Low to Bus High Impedance (with $\overline{AS}$ High)	t_{GLZ}	—	120	—	100	—	80	—	70	—	60	ns
39	$\overline{BG}$ Width High	t_{GH}	1 5	—	1 5	—	1 5	—	1 5	—	1.5	—	Clk. Per.
40	Clock Low to $\overline{VMA}$ Low	t_{CLVML}	—	90	—	80	—	70	—	70	—	70	ns
41	Clock Low to E Transition	t_{CLC}	—	100	—	85	—	70	—	55	—	45	ns
42	E Output Rise and Fall Time	$t_{Er,f}$	—	25	—	25	—	25	—	25	—	25	ns
43	$\overline{VMA}$ Low to E High	t_{VMLEH}	325	—	240	—	200	—	150	—	90	—	ns
44	$\overline{AS}$, $\overline{DS}$ High to $\overline{VPA}$ High	t_{SHVPH}	0	240	0	160	0	120	0	90	0	70	ns
45	E Low to Address/$\overline{VMA}$/FC Invalid	t_{ELAI}	55	—	35	—	30	—	10	—	10	—	ns
46	$\overline{BGACK}$ Width	t_{BGL}	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	Clk. Per
47[5]	Asynchronous Input Setup Time	t_{ASI}	30	—	25	—	20	—	20	—	20	—	ns
48[3]	$\overline{BERR}$ Low to $\overline{DTACK}$ Low	t_{BELDAL}	30	—	25	—	20	—	20	—	20	—	ns
49	E Low to $\overline{AS}$, $\overline{DS}$ Invalid	t_{ELSI}	−80	—	−80	—	−80	—	−80	—	−80	—	ns
50	E Width High	t_{EH}	900	—	600	—	450	—	350	—	280	—	ns
51	E Width Low	t_{EL}	1400	—	900	—	700	—	550	—	440	—	ns
52	E Extended Rise Time	t_{CIEHX}	—	80	—	80	—	80	—	80	—	80	ns
53	Data Hold from Clock High	t_{CHDO}	0	—	0	—	0	—	0	—	0	—	ns
54	Data Hold from E Low (Write)	t_{ELDOZ}	60	—	40	—	30	—	20	—	15	—	ns
55	R/$\overline{W}$ to Data Bus Impedance Change	t_{RLDO}	55	—	35	—	30	—	20	—	10	—	ns
56[4]	$\overline{HALT}$/$\overline{RESET}$ Pulse Width	t_{HRPW}	10	—	10	—	10	—	10	—	10	—	Clk. Per.

Notes:

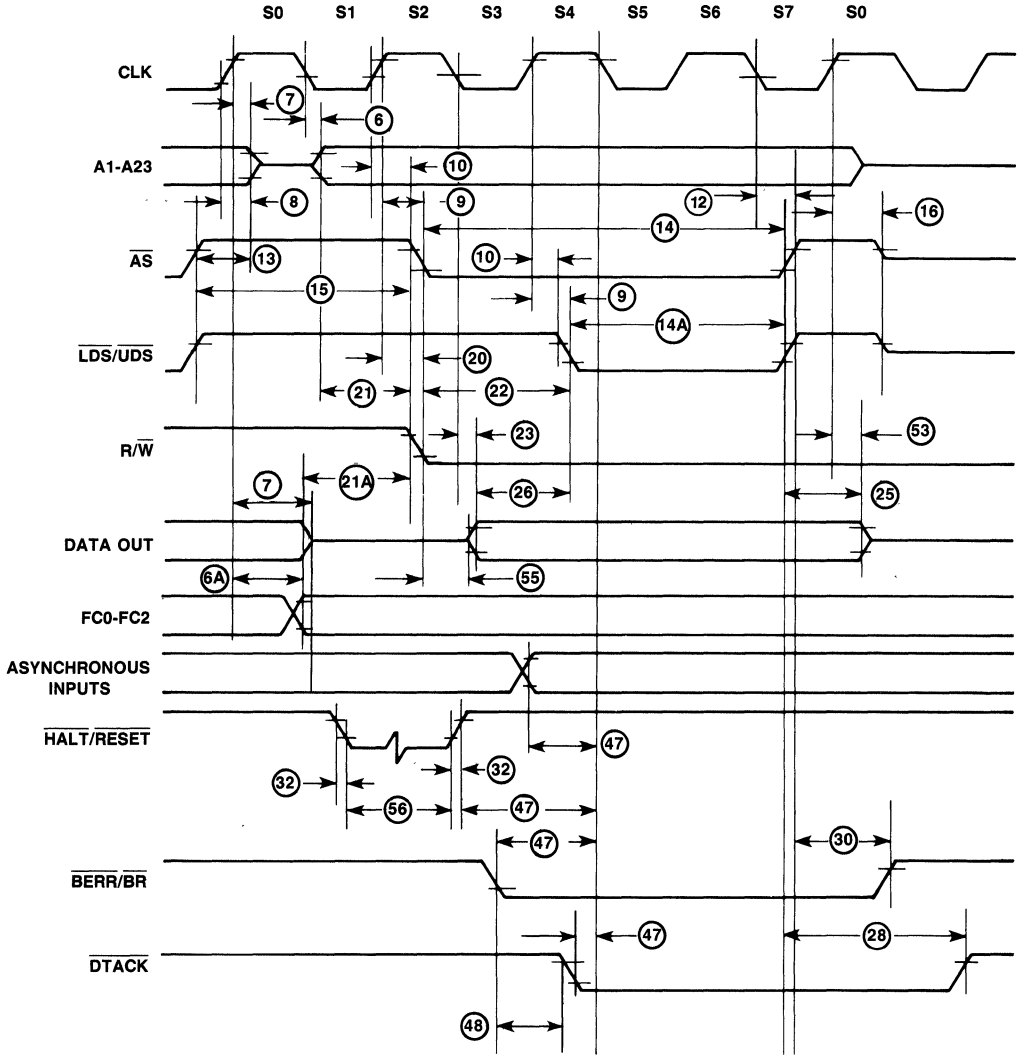
1. For a loading capacitance of less than or equal to 50 picofarads, subtract 5 nanoseconds from the value given in these columns.
2. Actual value depends on clock period.
3. If #47 is satisfied for both $\overline{DTACK}$ and $\overline{BERR}$, #48 may be 0 nanoseconds.
4. For power up, the MPU must be held in $\overline{RESET}$ state for 100 ms to stabilize all on-chip circuitry. After the system is powered up, #56 refers to the minimum pulse width required to reset the system.
5. If the asynchronous setup time (#47) requirements are satisfied the $\overline{DTACK}$ low-to-data setup time (#31) requirement can be ignored. The data must only satisfy the data-in clock-low setup time (#27) for the following cycle.
6. When $\overline{AS}$ and R/$\overline{W}$ are equally loaded (±20%), subtract 10 nanoseconds from the value given in these columns.



NOTES:

1. SETUP TIME FOR THE ASYNCHRONOUS INPUTS BGACK, IPL0-IPL2, AND VPA GUARANTEES THEIR RECOGNITION AT THE NEXT FALLING EDGE OF THE CLOCK.
2. BR NEEDS FALL AT THIS TIME ONLY IN ORDER TO INSURE BEING RECOGNIZED AT THE END OF THIS BUS CYCLE.
3. TIMING MEASUREMENTS ARE REFERENCED TO AND FROM A LOW VOLTAGE OF 0.8 VOLTS AND A HIGH VOLTAGE OF 2.0 VOLTS, UNLESS OTHERWISE NOTED.

Figure 45. Read Cycle Timing



NOTES:
1. BECAUSE OF LOADING VARIATIONS, R/$\overline{W}$ MAY BE VALID AFTER $\overline{AS}$ EVEN THOUGH BOTH ARE INITIATED BY THE RISING EDGE OF S2 (SPECIFICATION 20A).
2. TIMING MEASUREMENTS ARE REFERENCED TO AND FROM A LOW VOLTAGE OF 0.8 VOLTS AND A HIGH VOLTAGE OF 2.0 VOLTS, UNLESS OTHERWISE NOTED.

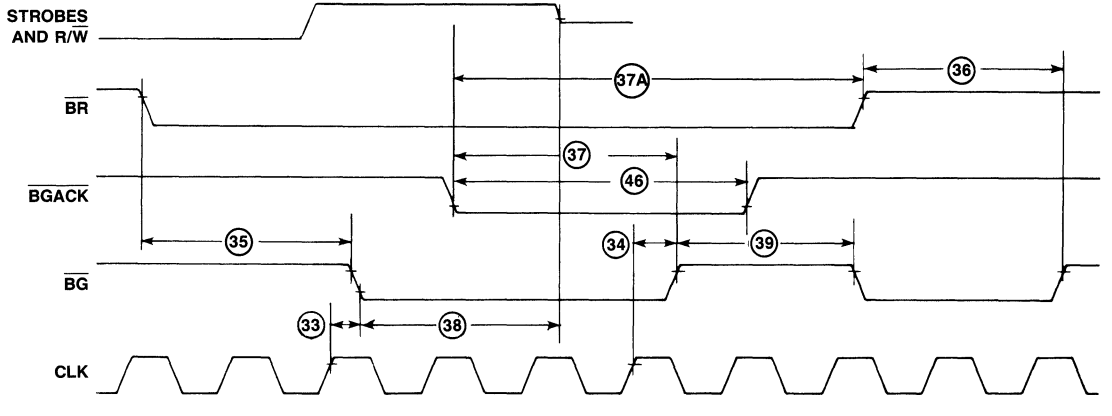
Figure 46. Write Cycle Timing

AC ELECTRICAL SPECIFICATIONS — BUS ARBITRATION

(V_{CC} = 5.0 Vdc ±5%, V_{SS} = 0 Vdc, T_A = 0° to 70°C. See Figure 47.)

Num.	Characteristic	Symbol	4 MHz		6 MHz		8 MHz		10 MHz		12.5 MHz		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
33	Clock High to $\overline{BG}$ Low	t_{CHGL}	—	90	—	80	—	70	—	60	—	50	ns
34	Clock High to $\overline{BG}$ High	t_{CHGH}	—	90	—	80	—	70	—	60	—	50	ns
35	$\overline{BR}$ Low to $\overline{BG}$ Low	t_{BRLGL}	1.5	3.5	1 5	3.5	1.5	3 5	1.5	3 5	1 5	3.5	Clk. Per
36	$\overline{BR}$ High to $\overline{BG}$ High	t_{BRHGH}	1 5	3 5	1.5	3 5	1.5	3 5	1 5	3 5	1 5	3.5	Clk Per
37	$\overline{BGACK}$ Low to $\overline{BG}$ High	t_{GALGH}	1.5	3.0	1 5	3 0	1 5	3.0	1 5	3 0	1.5	3 0	Clk Per
37A	$\overline{BGACK}$ Low to $\overline{BR}$ High (to Prevent Rearbitration)	t_{BGKBR}	30	—	25	—	20	—	20	—	20	—	ns
38	$\overline{BG}$ Low to Bus High Impedance (with $\overline{AS}$ High)	t_{GLZ}	—	120	—	100	—	80	—	70	—	60	ns
39	$\overline{BG}$ Width High	t_{GH}	1 5	—	1 5	—	1.5	—	1 5	—	1 5	—	Clk Per
46	$\overline{BGACK}$ Width	t_{BGL}	1.5	—	1.5	—	1 5	—	1 5	—	1.5	—	Clk. Per

THESE WAVEFORMS SHOULD ONLY BE REFERENCED IN REGARD TO THE EDGE-TO-EDGE MEASUREMENT OF THE TIMING SPECIFICATIONS. THEY ARE NOT INTENDED AS A FUNCTIONAL DESCRIPTION OF THE INPUT AND OUTPUT SIGNALS. REFER TO OTHER FUNCTIONAL DESCRIPTIONS AND THEIR RELATED DIAGRAMS FOR DEVICE OPERATION.

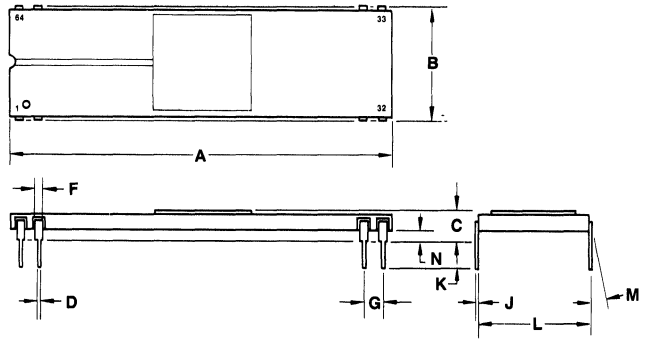


NOTES:

1. **SETUP TIME FOR THE ASYNCHRONOUS INPUTS $\overline{BERR}$, $\overline{BGACK}$, $\overline{BR}$, $\overline{DTACK}$, $\overline{IPL0}$-$\overline{IPL2}$, AND $\overline{VPA}$ GUARANTEES THEIR RECOGNITION AT THE NEXT FALLING EDGE OF THE CLOCK.**
2. **WAVEFORM MEASUREMENTS FOR ALL INPUTS AND OUTPUTS ARE SPECIFIED AT: LOGIC HIGH = 2.0 VOLTS, LOGIC LOW = 0.8 VOLTS**

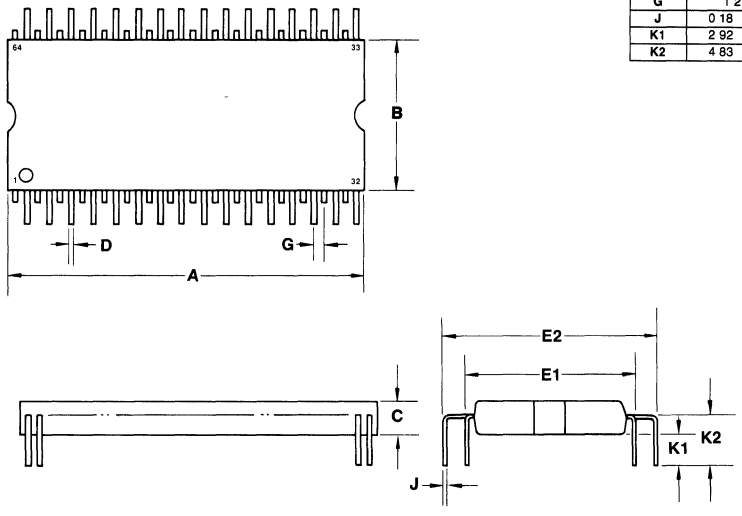
Figure 47. AC ELECTRICAL Waveforms — Bus Arbitration

64-PIN CERAMIC DUAL IN-LINE PACKAGE (DIP)



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	80.52	82.04	3.170	3.230
B	22.25	22 96	0.876	0 904
C	3 05	4 32	0 120	0 170
D	0 38	0 53	0 015	0 021
F	0 76	1 40	0 030	0 055
G	2.54 BSC		0.100 BSC	
J	0.20	0.33	0.008	0.013
K	2 54	4.19	0.100	0 165
L	22 61	23.11	0.890	0 910
M	—	10°	—	10°
N	1 02	1 52	0 040	0.060

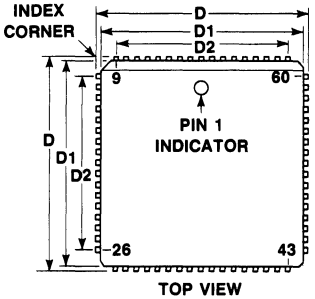
64-PIN PLASTIC QUAD IN-LINE PACKAGE (QUIP)



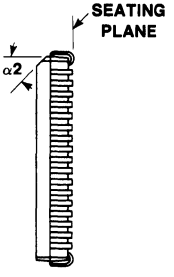
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	41 10	41.61	1 618	1 638
B	17.02	17 23	0.670	0 690
C	3 56	4.58	0 140	0 180
D	0.48	0 56	0 018	0 022
E1	19 05 BSC		0 750 BSC	
E2	23.50 BSC		0 925 BSC	
G	1 27 BSC		0 050 BSC	
J	0 18	0 33	0 007	0 013
K1	2 92	3 18	0 115	0 125
K2	4 83	5 34	0 190	0 210

PACKAGE DIMENSIONS

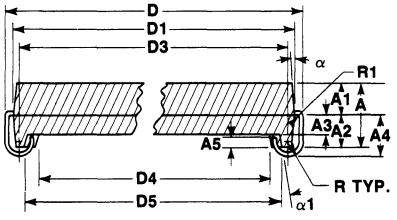
68-PIN PLASTIC CHIP CARRIER (PCC)



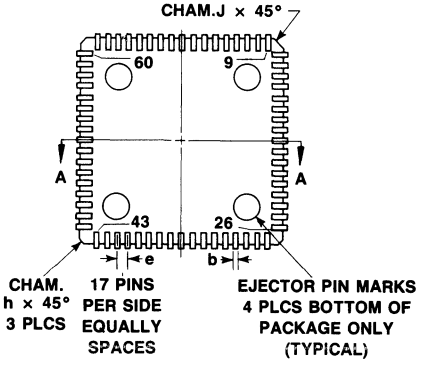
TOP VIEW



SIDE VIEW



SECTION A-A
TYP FOR BOTH AXIS (EXCEPT FOR BEVELED EDGE)



BOTTOM VIEW

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	3 683	3 785	145	149
A1	1 829	1 930	072	076
A2	1 803	1 905	071	075
A3	1 372	1 473	054	058
A4	2 311	2 464	091	097
A5	0 203	0 305	008	012
b	0 457 TYP		018 TYP	
D	25 02	25 27	985	995
D1	24 00	24 26	945	955
D2	20 19	20 45	795	805
D3	23 24	23 50	915	925
D4	20 96	21 21	825	835
D5	22 23	22 48	875	885
e	1 27 BSC		050 BSC	
h	1 143 TYP		045 TYP	
J	0 254 TYP		010 TYP	
α	4° TYP		4° TYP	
α1	10° TYP		10° TYP	
α2	45° TYP		45° TYP	
R	0 889 TYP		035 TYP	
R1	0 254 TYP		010 TYP	

Rockwell

R68265, R68465 DOUBLE-DENSITY FLOPPY DISK CONTROLLER (DDFDC)

PRELIMINARY

DESCRIPTION

The R68465 Double-Density Floppy Disk Controller (DDFDC) interfaces up to four floppy disk drives to a 68000/68008 microprocessor-based system. The DDFDC simplifies the system design by minimizing both the number of external hardware components and software steps needed to implement the floppy disk drive (FDD) interface. Control signals supplied by the DDFDC reduce the number of components required in external phase locked loop and write precompensation circuitry. Memory-mapped registers containing commands, status and data simplify the software interface. Built-in functions reduce the software overhead needed to control the FDD interface. The DDFDC supports both the IBM 3740 Single-Density (FM) and IBM System 34 Double-Density (MFM) formats.

The R68265 interfaces to the 3½″ Sony Micro Floppy disk drive as well as 5¼″ and 8″ drives. The R68265 writes in the 3½″ Sony compatible format and can also read from disks formatted in IBM compatible format. Any combination of up to four 3½″, 5¼″ and 8″ drives can be interfaced to and controlled by the R68265. The R68265 is pin-compatible with, and electrically identical to, the R68465.

The DDFDC interfaces directly to the 68000/68008 asynchronous microprocessor bus and operates with 8-bit byte length data transferred on the bus. The DDFDC will operate in either DMA or non-DMA mode. In DMA mode, the MPU need only load the command into the DDFDC and all data transfers occur under DMA control. The R68265/R68465 is directly compatible with the MC68440 Dual Direct Memory Access Controller (DDMAC). In non-DMA mode, the DDFDC generates an interrupt to the MPU indicating that a byte of data is available.

Controller commands, command or device status, and data are transferred between the DDFDC and the MPU via six internal registers. The Main Status Register (MSR) stores the DDFDC status information while four additional status registers provide result information to the MPU following each controller command. The Data Register (DR) stores actual disk data, parameters, controller commands and FDD status information for use by the MPU.

The DDFDC executes 15 separate multi-byte commands:

Read Data	Specify
Write Data	Format a Track
Read Deleted Data	Scan Equal
Write Deleted Data	Scan High or Equal
Read a Track	Scan Low or Equal
Read ID	Sense Interrupt Status
Seek	Sense Drive Status
Recalibrate (Restore to Track 0)	

FEATURES

- Address mark detection circuitry
- Software control of
  —Track stepping rate
  —Head load time
  —Head unload time
- Writes in:
  —IBM compatible (single- and double-density format (R68465)
  —Sony compatible (EMCA) format (R68265)
- Reads
  —IBM compatible format (R68265 and R68465)
  —Sony compatible format (R68265)
- Programmable data record lengths: 128, 256, 512, 1024, 2048, 4096 or 8192 bytes/sector
- Multi-sector and multi-track transfer capability
- Controls up to four floppy disk drives
- Data scan capability—will scan a single sector or an entire track of data fields, comparing on a byte-by-byte basis data in the processor's memory with data read from the disk
- Data transfers in DMA or non-DMA mode
- Parallel seek operations on up to four drives
- Directly compatible with 68000 16-bit and 68008 8-bit asynchronous microprocessor bus
- Single phase 8 MHz clock
- Single +5 volt power supply

ORDERING INFORMATION

Part Number	CLK Frequency	Temperature Range
R68265 —		
R68465 —	8 MHz	0°C to 70°C
Package: C = Ceramic P = Plastic		

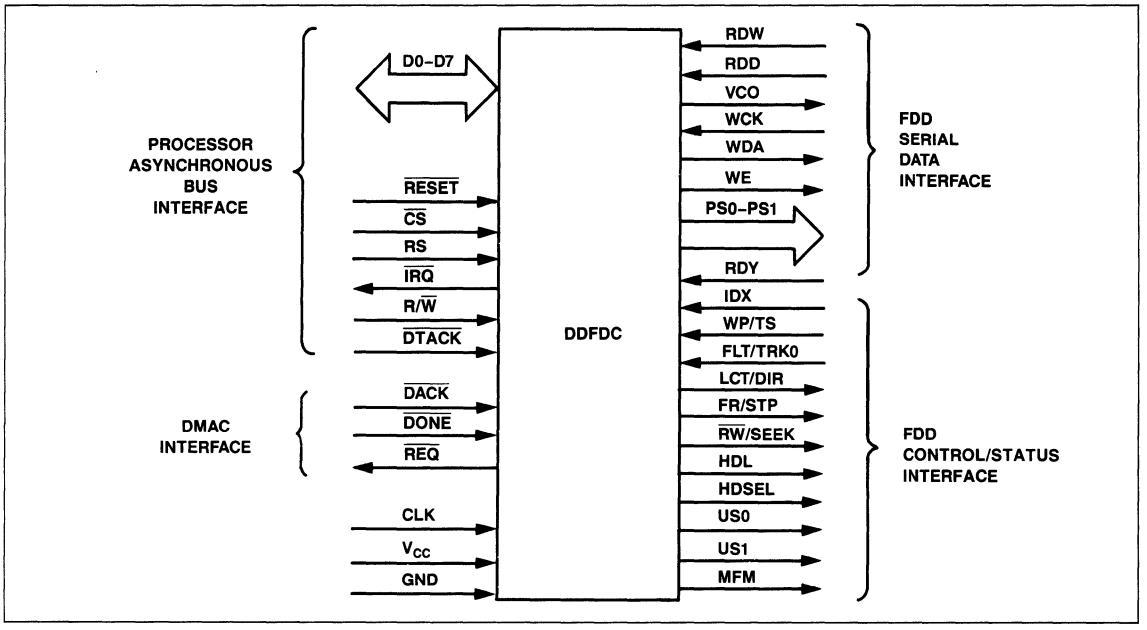


Figure 1. DDFDC Input and Output Signals

PIN DESCRIPTION

Throughout this document signals are presented using the terms active and inactive, or asserted and negated, independent of whether the signal is active in the high-voltage state or low-voltage state. (The active state of each logic pin is described below.) Active low signals are denoted by a superscript bar. For example, R/$\overline{W}$ indicates read is active high and a write is active low.

BUS INTERFACE

D0–D7—Data Lines. The bidirectional data lines transfer data between the DDFDC and the 8-bit data bus.

CLK—CLOCK. The clock is a TTL compatible 8 MHz square wave signal.

$\overline{\text{RESET}}$—RESET. This active low input places the DDFDC in the idle state and resets the output lines to the floppy disk drives to the low state. $\overline{\text{RESET}}$ does not affect the Step Rate Time (SRT), Head Unload Time (HUT) or Head Load Time (HLT) set by a specify command. If RDY goes high while $\overline{\text{RESET}}$ is low, the DDFDC will assert $\overline{\text{IRQ}}$ within 1.024 ms. This interrupt can be cleared by issuing a Sense Interrupt Status command.

$\overline{\text{CS}}$—Chip Select. The DDFDC is selected when the $\overline{\text{CS}}$ input is low.

RS—Data/Status Register Select. This input selects the Data or Status Register for reading from or writing to. When RS = high, the Data Register is selected and the state of R/$\overline{W}$ determines whether it is a read (R/$\overline{W}$ = high) or a write (R/$\overline{W}$ = low) operation. when RS = low, the Status Register is selected. This register may only be read (R/$\overline{W}$ = high); the state R$\overline{W}$ = low is invalid when the Status Register is selected.

$\overline{\text{IRQ}}$—Interrupt Request. This active low output is the interrupt request generated by the DDFDC to the MPU. $\overline{\text{IRQ}}$ is asserted upon completion of some DDFDC commands and before a data byte is transferred between the DDFDC and the data bus (in the Non-DMA mode).

R/$\overline{W}$—Read/Write. This input defines the data bus transfer as a read or write cycle. When high (read), the data transfer is from the DDFDC to the data bus. When low (write), the data transfer is from the data bus to the DDFDC.

$\overline{\text{DTACK}}$—Data Transfer Acknowledge. This signal is the asynchronous handshake line for information transfer on the 68000 system bus. It is generated by the DDFDC as an acknowledge to the $\overline{\text{CS}}$ signal in an asynchronous transfer. A low output indicates that valid data is on the bus (read cycle) or that data has been written (write cycle). Except when being asserted, this signal is normally in the high impedance state.

The output characteristics of $\overline{DTACK}$ are the same as other system interface signals with allowances for an external pull-up resistor such that the output is driven to the high level first and then to the high impedance state.

DIRECT MEMORY ACCESS CONTROLLER (DMAC) INTERFACE

$\overline{DACK}$—DMA Acknowledge. The DMA transfer acknowledge signal is a TTL compatible input generated by the DMA controller (DMAC) controlling the DDFDC. The DMA cycle is active when $\overline{DACK}$ is low and the DDFDC is performing a DMA transfer.

$\overline{REQ}$—Data DMA Request. The transfer request signal is a TTL compatible output generated by the DDFDC to request a data transfer operation under control of the DMAC (in the DMA mode). The request is active when $\overline{REQ}$ = low. The signal is reset inactive when DMA Acknowledge ($\overline{DACK}$) is asserted (low).

$\overline{DONE}$—DMA Transfer Complete. This input signal is issued to the DDFDC when the DMA transfer for a channel is complete. The signal is active low concurrent with the $\overline{DACK}$ input when the DMA operation is complete as a result of that transfer.

FDD SERIAL DATA INTERFACE

RDD—Read Data. Read Data input from the floppy disk drive (FDD) containing clock and data bits.

RDW—Read Data Window. Data Window input generated by the Phase Locked Loop (PLL) and used to sample data from the FDD.

VCO—Voltage Controlled Oscillator Sync. This output signal inhibits the VCO in the PLL circuit when low and enables the VCO in the PLL circuit when high. This inhibits RDD and RDW from being generated until valid data is detected from the FDD.

WCK—Write Clock. This input clock determines the Write Data rate to the FDD. The data rate is 500 KHz in the FM mode (MFM = low) and 1 MHz in the MFM mode (MFM = high). The pulse width is 250 ns (typical) in both modes.

WDA—Write Data. Serial write data output to the FDD containing both clock and data bits.

WE—Write Enable. This output signal enables the Write Data into the FDD when high.

PS0–PS1—Preshift. These outputs are encoded to convey write compensation status during the MFM mode to determine early, late or normal times as follows:

Write Precompensation Status	Preshift Outputs	
	PS0	PS1
Normal	0	0
Late	0	1
Early	1	0
Invalid	1	1

0 = Low, 1 = High

FDD CONTROL/STATUS INTERFACE

RDY—Ready. An active high input signal indicates the FDD is ready to send data to, or receive data from, the DDFDC.

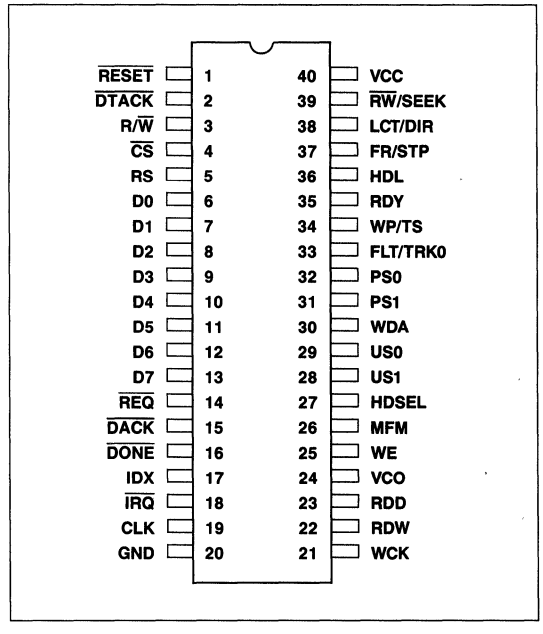
IDX—Index. An active high input signal from the FDD indicates the index hole is under the index sensor. Index is used to synchronize DDFDC timing.

$\overline{RW}$/SEEK—Read Write/Seek. Mode selection signal to the FDD which controls the multiplexer from the multiplexed signals. When $\overline{RW}$/SEEK is low, the Read/Write mode is commanded; when $\overline{RW}$/SEEK is high, the Seek mode is commanded.

$\overline{RW}$/SEEK	Mode	Active FDD Interface Signals
Low	Read/Write	WP, FLT, LCT, FR
High	Seek	TS, TRK0, DIR, STP

WP/TS—Write Protect/Two Side. An active high multiplexed input signal from the FDD. In the Read/Write mode, WP/TS high indicates the media is write-protected. In the Seek mode, WP/TS high indicates the media is two-sided.

FLT/TRK0—Fault/Track Zero. An active high multiplexed input from the FDD. In the Read/Write mode ($\overline{RW}$/SEEK = low), FLT/TRK0 high indicates an FDD fault. In the Seek mode, FLT/TRK0 high indicates that the read/write head is positioned over track zero.



Pin Diagram

LCT/DIR—Low Current/Direction. A multiplexed output to the FDD. In the Read/Write mode, LCT/DIR is low when the read/write head is to be positioned over the inner tracks and the LCT/DIR is high when the head is to be positioned over the outer tracks. In the Seek mode, LCT/DIR controls the head direction. When LCT/DIR is high, the head steps to the outside of the disk; when LCT/DIR is low, the head steps to the inside of the disk.

FR/STP—Fault Reset/Step. A multiplexed output to the FDD. In the Read/Write mode, FR/STP high resets the fault indicator in the FDD. An FR pulse is issued at the beginning of each read or write command prior to issuing HDL. In the Seek mode, FR/STP provides the step pulses to move the read/write head to another track in the direction indicated by the LCT/DIR signal.

HDL—Head Load. An active high output to notify the FDD that the read/write head should be loaded (placed in contact with the media). A low level indicates the head should be unloaded.

HD—Head Select. An output to the FDD to select the proper read/write head. Head One is selected when HD = high and Head Zero is selected when HD = low.

US0-US1—Unit Select. Output signals for floppy disk drive selection as follows:

Unit Select		Floppy Disk Drive Select
US0	US1	
0	0	0
0	1	1
1	0	2
1	1	3
0 = Low, 1 = High		

MFM—MFM Mode. Output signal to the FDD to indicate MFM or FM mode. Selects the MFM mode when MFM = high and the FM mode when MFM = low.

VCC—Power. +5V dc.

GND—Ground (V_{ss}).

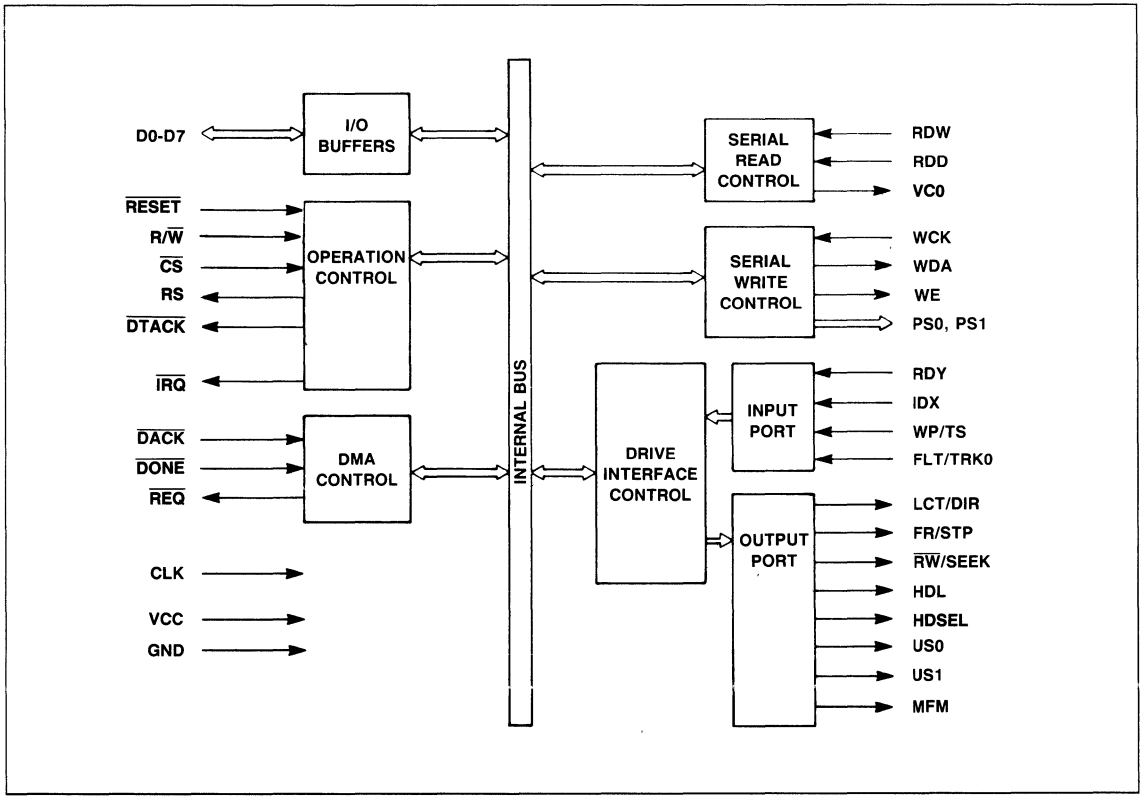


Figure 2. R68265/R68465 DDFDC Block Diagram

DDFDC REGISTERS

The DDFDC contains six registers which may be accessed by the processor or DMA controller via the system (i.e., microprocessor) bus: a Main Status Register, a Data Register, and four Result Status Registers. The 8-bit Main Status Register (MSR) contains the status information of the DDFDC, and may be accessed at any time. The 8-bit Data Register, consisting of several registers in a stack with only one register presented to the data bus at a time, stores data, commands, parameters and FDD status information. Bytes of data are read out of, or written into, the Data Register in order to initiate a command or to obtain the results of a command execution.

The read-only Main Status Register facilitates the transfer of data between the system and the DDFDC. The other Status Registers (ST0, ST1, ST2 and ST3) are only available during the result phase, and may be read only after completing a command. The particular command which has been executed determines how many of the Status Registers will be read.

The relationship between the status/data registers and the R/$\overline{W}$ and RS signals is shown below.

RS	R/$\overline{W}$	Function
0	0	Read Main Status Register
0	0	Illegal
1	1	Read from Data Register
1	0	Write into Data Register
0 = Low, 1 = High		

Table 1 shows each of the status registers used by the DDFDC and each bit assignment within the individual registers. Table 2 defines the symbols used throughout the command definitions. Each register bit symbol is defined in the register definition that follows Table 2.

REGISTER DEFINITIONS

Main Status Register (MSR)

7	6	5	4	3	2	1	0
RQM	DIO	EXM	CB	D3B	D2B	D1B	D0B

The Main Status Register (MSR) contains the status information of the DDFDC, and must be read by the processor before each byte is written to, or read from, the Data Register during the command or result phase. MSR reads are not required during the execution phase. The Data Input/Output (DIO) and Request for Master (RQM) bits in the MSR indicate when data is ready and in which direction data will be transferred on the data bus. The maximum time between the last R/$\overline{W}$ during command or result phases and the DIO and RQM getting set or reset is 12 μs. For this reason, every time the MSR is read the processor should wait 12 μs. The maximum time from the end of the last read in the result phase to when bit 4 (DDFDC Busy) goes low is also 12 μs.

The DIO and RQM timing chart is shown in Figure 3.

MSR
7 RQM —Request for Master.
0 Data Register is not ready.
1 Data Register is ready.

MSR
6 DIO —Data Input/Output.
0 Data transfer is from system to the Data Register.
1 Data transfer is from Data Register to the system.

MSR
5 EXM —Execution Mode. (Non-DMA mode only).
0 Execution phase ended, result phase begun.
1 Execution phase started.

MSR
4 CB —Controller (DDFDC) Busy.
0 DDFDC is not busy, will accept a command.
1 DDFDC is busy, will not accept a command.

MSR
3 D3B —Floppy Disk Drive (FDD) 3 Busy.
0 FDD 3 is not busy, DDFDC will accept read or write command.
1 FDD 3 is busy, DDFDC will not accept read or write command.

MSR
2 D2B —FDD 2 Busy.
0 FDD 2 is not busy, DDFDC will accept read or write command.
1 FDD 2 is busy, DDFDC will not accept read or write command.

MSR
1 D1B —FDD 1 Busy.
0 FDD 1 is not busy, DDFDC will accept read or write command.
1 FDD 1 is busy, DDFDC will not accept read or write command.

MSR
0 D0B —FDD 0 Busy.
0 FDD 0 is not busy, DDFDC will accept read or write command.
1 FDD 0 is busy, DDFDC will not accept read or write command.

Status Register 0 (ST0)

7	6	5	4	3	2	1	0
IC		SE	EC	NR	HD	US	
						US1	US0

The Status Register 0 (ST0) as well as the other status registers (ST1-ST3), are available only during the result phase, and may be read only after completing a command. The particular command executed determines which status registers are used and may be read.

Table 1. DDFDC Status Register Bit Assignments

	Bit Number							
	7	6	5	4	3	2	1	0
Main Status Register (MSR)	RQM	DIO	EXM	CB	D3B	D2B	D1B	D0B
Status Register 0 (ST0)	IC		SE	EC	NR	HD	US	
							US1	US0
Status Register 1 (ST1)	EN	0	DE	OR	0	ND	NW	MA
Status Register 2 (ST2)	0	CM	DD	WT	SH	SN	BT	MD
Status Register 3 (ST3)	FLT	WP	RDY	TRK0	TS	HD	US1	US0

Table 2. Command Symbol Description

Symbol	Name	Description
D	Data	The data pattern which is going to be written into a sector.
D0-D7	Data Bus	8-bit data bus, where D0 is the least significant data line and D7 is the most significant data line.
DTL	Data Length	When N is defined as 00, DTL is the number of data bytes to read from or write into the sector.
EOT	End of Track	The final sector number on a track. During read or write operation, the DDFDC stops data transfer after reading from or writing to the sector equal to EOT.
GPL	Gap Length	The length of Gap 3. During read/write commands this value determines the number of bytes that the VCO will stay low after two CRC bytes. During the Format a Track command it determines the size of Gap 3.
H	Head Address	Head number 0 or 1, as specified in ID field.
HD (H)	Head	A selected head number 0 or 1 which controls the polarity of pin 27. (H = HD in all command words).
HLT	Head Load Time	The head load time in the FDD (2 to 254 ms in 2 ms increments).
HUT	Head Unload Time	The head unload time after a read or write operation has occurred (16 to 240 ms in 16 ms increments).
MF	FM or MFM Mode	When MF = 0, FM mode is selected; and when MF = 1, MFM mode is selected.
MT	Multi-Track	When MT = 1, a multi-track operation is to be performed. After finishing a read/write operation on side 0, the DDFDC will automatically start searching for sector 1 on side 1.
N	Bytes/Sector	The number of data bytes written in a sector.
ND	Non-DMA Mode	When ND = 1, operation is in the Non-DMA mode; when ND = 0, operation is in the DMA mode.
NTN	New Track Number	A new track number, which will be reached as a result of the Seek command. Desired head position.
PTN	Present Track Number	The track number at the completion of Sense Interrupt Status command. Present head position.
R	Record (Sector)	The sector number to be read or written.
RS	Register Select	Controls selection of Main Status Register (RS = low) or Data Register (RS = high).
R/W	Read/Write	Either read (R) or write (W) signal
ST	Sectors/Track	The number of sectors per track.
SK	Skip	Skip Deleted Data Address Mark.
SRT	Step Rate Time	The stepping rate for the FDD (1 to 16 ms in 1 ms increments). Stepping rate applies to all drives (F = 1 ms, E = 2 ms, etc.)
ST0 ST1 ST2 ST3	Status 0 Status 1 Status 2 Status 3	Four registers which store the status information after a command has been executed. This information is available during the result phase after command execution. These registers should not be confused with the Main Status Register (selected by RS = low). ST0-ST3 may be read only after a command has been executed and contain information relevant to that particular command.
STP	Sector Test Process	During a Scan command, if STP = 01, the data in contiguous sectors is compared byte by byte with data sent from the processor (or DMA controller); and if STP = 02, then alternate sectors are read and compared.
T	Track Number	The current/selected track number of the medium (0–255).
US0,US1	Unit Select	A selected drive number (0-3).

ST0
7 6 IC —Interrupt Code.
0 0 Normal Termination (NT). Command was properly executed and completed.
0 1 Abnormal Termination (AT). Command execution was started, but was not successfully completed.
1 0 Invalid Command (IC). Received command was invalid.
1 1 Abnormal Termination (AT). The Ready (RDY) signal from the FDD changed state during command execution.

ST0
5 SE —Seek End.
0 Seek command is not completed.
1 Seek command completed by DDFDC.

ST0
4 EC —Equipment Check.
0 No error.
1 Either a fault signal is received from the FDD or the track 0 signal failed to occur after 256 step pulses (Recalibrate Command).

ST0
3 NR —Not Ready.
0 FDD is ready.
1 FDD is not ready at issue of read or write command. If a read or write command is issued to side 1 of a single-sided drive, this bit is also set.

ST0
2 HD —Head Address. (At Interrupt).
0 Head Select 0.
1 Head Select 1.

ST0
1 0 US —Unit Selected. (At Interrupt).
0 0 FDD 0 selected.
0 1 FDD 1 selected.
1 0 FDD 2 selected.
1 1 FDD 3 selected.

Status Register 1 (ST1)

7	6	5	4	3	2	1	0
EN	0	DE	OR	0	ND	NW	MA

ST1
7 EN —End of Track.
0 No error.
1 DDFDC attempted to access a sector beyond the last sector of a track.

ST1
6 —Not Used. Always Zero.

ST1
5 DE —Data Error.
0 No error.
1 DDFDC detected a CRC error in ID field or the Data field.

ST1
4 OR —Overrun.
0 No error.
1 DDFDC was not serviced by the system during data transfers, within a predetermined time interval.

ST1
3 —Not Used. Always Zero.

ST1
2 ND —No Data.
0 No error.
1 3 possible errors.

1. DDFDC cannot find sector specified in the Internal Data Register (IDR) during execution of Read Data, Write Deleted Data or Scan commands.
2. DDFDC cannot read ID field without an error during Read ID command.
3. DDFDC cannot find starting sector during execution of Read a Track command.

ST1
1 NW —Not Writable.
0 No error.
1 DDFDC detected a write protect signal from FDD during execution of Write Data, Write Deleted Data or Format a Track commands.

ST1
0 MA —Missing Address Mark.
0 No error.
1 2 possible errors.

1. DDFDC cannot detect the ID Address Mark after encountering the index hole twice.
2. DDFDC cannot detect the Data Address Mark or Deleted Data Address Mark. The MD (Missing Address Mark in Data field) of Status Register 2 is also set.

Status Register 2 (ST2)

7	6	5	4	3	2	1	0
0	CM	DD	WT	SH	SN	BT	MD

ST2
7 —Not Used. Always Zero.

ST2
6 CM —Control Mark.
0 No error.
1 DDFDC encountered a sector which contained a Deleted Data Address Mark during execution of a Read Data, Read a Track, or Scan command, or the DDFDC encountered a sector which contained a Data Address Mark during execution of a Read Deleted Data command.

ST2
5 DD —Data Error in Data Field.
0 No error.
1 DDFDC detected a CRC error in the Data field.

ST2
4 WT —Wrong Track.
0 No error.
1 Contents of T on the disk is different from that stored in IDR. Bit is related to ND (Bit 2) of Status Register 1.

ST2
3 SH —Scan Equal Hit.
0 No "equal" condition during a scan command.
1 "Equal" condition satisfied during a scan command.

ST2
2 SN —Scan Not Satisfied.
0 No error.
1 DDFDC cannot find a sector on the track which meets the scan command condition.

ST2
1 BT —Bad Track.
0 No error.
1 Contents of T on the disk is different from that stored in the IDR and T = FF. Bit is related to ND (Bit 2) of Status Register 1.

ST2
0 MD —Missing Address Mark in Data Field.
0 No error.
1 DDFDC cannot find a Data Address Mark or Deleted Data Address Mark during a data read from the disk.

Status Register 3 (ST3)

7	6	5	4	3	2	1	0
FLT	WP	RDY	TRK0	TS	HD	US1	US0

Status Register 3 (ST3) holds the results of the Sense Drive Status command.

ST3
7 FLT —Fault.
0 Fault (FLT) signal from the FDD is low.
1 Fault (FLT) signal from the FDD is high.

ST3
6 WP —Write Protect.
0 Write Protect (WP) signal from the FDD is low.
1 Write Protect (WP) signal from the FDD is high.

ST3
5 RDY —Ready.
0 Ready (RDY) signal from the FDD is low.
1 Ready (RDY) signal from the FDD is high.

ST3
4 TRK0 —Track 0.
0 Track 0 (TRK0) signal from the FDD is low.
1 Track 0 (TRK0) signal is from the FDD is high.

ST3
3 TS —Two Side.
0 Two Side (TS) signal from the FDD is low.
1 Two Side (TS) signal from the FDD is high.

ST3
2 HD —Head Select.
0 Head Select (HD) signal to the FDD is low.
1 Head Select (HD) signal to the FDD is high.

ST3
1 US1 —Unit Select 1.
0 Unit Select 1 (US1) signal to the FDD is low.
1 Unit Select 1 (US1) signal to the FDD is high.

ST3
0 US0 —Unit Select 0.
0 Unit Select 0 (US0) signal to the FDD is low.
1 Unit Select 0 (US1) signal to the FDD is high.

COMMAND SEQUENCE

The DDFDC is capable of performing 15 different commands. Each command is initiated by a multi-byte transfer of data from the system. After command execution, the result of the command may be a multi-byte transfer of data back to the system. Because of this multi-byte transfer of information between the DDFDC and the system, each command consists of three phases:

Command Phase—The DDFDC receives all information required to perform a particular operation from the system.

Execution Phase—The DDFDC performs the instructed operation.

Result Phase—After completion of the operation, status and other housekeeping information are made available to the system.

The bytes of data sent to the DDFDC to form a command, and read out of the DDFDC in the result phase, must occur in the order shown for each command sequence. That is, the command Code byte must be sent first followed by the other bytes in the specified sequence. All command bytes must be written and all result bytes must be read in each phase. After the last byte of data in the command phase is received by the DDFDC, the execution phase starts. Similarly, when the last byte of data is read out in the Result Phase, the command is ended and the DDFDC is ready to accept a new command. A command can be terminated by asserting the $\overline{\text{DONE}}$ signal to the DDFDC. This ensures that the processor can always get the DDFDC's attention even if the command in process hangs up in an abnormal manner.

COMMAND DESCRIPTION

READ DATA

A command set of nine bytes places the DDFDC into the Read Data mode. After the Read Data command has been received the DDFDC loads the head (if it is unloaded), waits the specified Head Settling Time (defined in the Specify command), then begins reading ID Address Marks and ID fields from the disk. When the current sector number (R) stored in the ID Register (IDR) matches the sector number read from the disk, the DDFDC transfers data from the disk Data field to the data bus.

After completion of the read operation from the current sector, the DDFDC increments the Sector Number (R) by one, and the data from the next sector is read and output to the data bus. This continuous read function is called a "Multi-Sector Read Operation." The Read Command terminates after reading the last data byte from sector R when R = EOT. ST0 bits 7 and 6 are set to 0 and 1, respectively, and ST1 bit 7 (EN) is set to a 1.

The Read Data command can also be terminated by a low $\overline{\text{DONE}}$ signal. $\overline{\text{DONE}}$ should be issued at the same time that the $\overline{\text{DACK}}$ for the last byte of data is sent. Upon receipt of TC, the DDFDC stops outputting data to the data bus, but continues to read data from the current sector, checks CRC (Cyclic Redundancy Count) bytes, and then at the end of that sector terminates the Read Data command and sets bits 7 and 6 in ST0 to 0. The amount of data which can be handled with a single command to the DDFDC depends upon MT (Multi-Track), MF (MFM/FM), and N (Number of Bytes/Sector) values. Table 3 shows the transfer capacity.

The multi-track function (MT) allows the DDFDC to read data from both sides of the disk. For a particular track, data is transferred starting at sector 1, side 0 and completed at sector L, side 1 (sector L = last sector on the side). This function pertains to only one track (the same track) on each side of the disk.

When N = 0 in command byte 6 (FM mode), the Data Length (DTL) in command byte 9 defines the data length that the DDFDC must treat as a sector. If DTL is smaller than the actual data length in a sector, the data beyond the DTL is not sent to the data bus. The DDFDC reads (internally) the complete sector, performs the CRC check, and depending upon the manner of command termination, may perform a multi-sector Read operation. When N is non-zero (MFM mode), DTL has no meaning and should be set to FF.

At the completion of the Read Data command, the head is not unloaded until the Head Unload Time (HUT) interval defined in the Specify command has elapsed. The head settling time may be avoided between subsequent reads if the processor issues another command before the head unloads. This time savings is considerable when disk contents are copied from one drive to another.

If the DDFDC detects the Index Hole twice in succession without finding the right sector (indicated in R), then the DDFDC sets the No Data (ND) flag in Status Register 1 (ST1) to a 1, sets Status Register 0 (ST0) bits 7 and 6 to 0 and 1, respectively, and terminates the Read Data command.

After reading the ID and Data fields in each sector, the DDFDC checks the CRC bytes. If a read error is detected (incorrect CRC in ID field), the DDFDC sets the Data Error (DE) flag in ST1 to a 1, sets the Data Error in Data Field (DD) flag in ST2 to a 1 if a CRC error occurs in the Data field, sets bits 7 and 6 in ST0 to 0 and 1, respectively, and terminates the command.

If the DDFDC reads a **Deleted Data Address Mark** from the disk, and the Skip Deleted Data Address Mark bit in the first command byte is not set (SK = 0), then the DDFDC reads all the data in the sector, sets the Control Mark (CM) flag in ST2 to a 1, and terminates the command. If SK = 1, the DDFDC skips the sector with the **Deleted Data Address Mark** and reads the next sector. The CRC bits in the deleted data field are not checked when SK = 1.

Table 3. DDFDC Transfer Capacity

Multi-Track (MT)	MFM/FM (MF)	Bytes/Sector (N)	Maximum Transfer Capacity (Bytes/Sector) (Number of Sectors)	Final Sector Read from Disk
0	0	00	(128) (26) = 3,328	26 at Side 0
0	1	01	(256) (26) = 6,656	or 26 at Side 1
1	0	00	(128) (52) = 6,656	26 at Side 1
1	1	01	(256) (52) = 13,312	
0	0	01	(256) (15) = 3,840	15 at Side 0
0	1	02	(512) (15) = 7,680	or 15 at Side 1
1	0	01	(256) (30) = 7,680	15 at Side 1
1	1	02	(512) (30) = 15,360	
0	0	02	(512) (8) = 4,096	8 at Side 0
0	1	03	(1024) (8) = 8,192	or 8 at Side 1
1	0	02	(512) (16) = 8,192	8 at Side 1
1	1	03	(1024) (16) = 16,384	

During disk data transfers from the DDFDC to the system, the DDFDC must be serviced by the system within 27 μs in the FM mode, and within 13 μs in the MFM mode, otherwise the DDFDC sets the Over Run (OR) flag in ST1 to a 1, sets bits 7 and 6 in ST0 to 0 and 1, respectively, and terminates the command.

If the processor terminates a read (or write) operation in the DDFDC, then the ID information in the result phase is dependent upon the state of the MT bit in the first command byte and the End of Track (EOT) byte. Table 4 shows the values for Track Number (T), Head Number (H), Sector Number (R), and Number of Data Bytes/Sector (N), when the processor terminates the command.

Command Phase:

R/W	BYTE	7	6	5	4	3	2	1	0
W	1	MT	MF	SK	0	0	1	1	0
	2	X	X	X	X	X	HD	US1	US0
	3	Track Number (T)							
	4	Head Number (H)							
	5	Sector Number (R)							
	6	Number of Data Bytes per Sector (N)							
	7	End of Track (EOT)							
	8	Gap Length (GPL)							
	9	Data Length (DTL)							

Result Phase:

R	1	Status Register 0 (ST0)
	2	Status Register 1 (ST1)
	3	Status Register 2 (ST2)
	4	Track Number (T)
	5	Head Number (H)
	6	Sector Number (R)
	7	Number of Data Bytes per Sector (N)

WRITE DATA

A command set of nine bytes places the DDFDC in the Write Data mode. After the Write Data command has been received the DDFDC loads the head (if it is unloaded), waits the specified Head Settling Time (defined in the Specify command), then begins reading ID fields from the disk. When the four bytes (T, H, R, N) loaded during the command match the four bytes of the ID field from the disk, the DDFDC transfers data from the data bus to the disk Data field.

After writing data into the current sector, the DDFDC increments the sector number (R) by one, and writes into the Data field in the next sector. The DDFDC continues this multi-sector write operation until the last byte is written to sector R when R = EOT. ST0 bits 7 and 6 are set to 0 and 1, respectively, and ST1 bit 7 (EN) is set to a 1.

The command can also be terminated by a low on $\overline{\text{DONE}}$. If $\overline{\text{DONE}}$ is sent to the DDFDC while writing into the current sector, then the remainder of the Data field is filled with 00 (zeros). In this case, ST0 bits 7 and 6 are set to 0 and the command is terminated.

The DDFDC reads the ID field of each sector and checks the CRC bytes. If the DDFDC detects a read error (incorrect CRC) in one of the ID fields, it terminates the Write Data command, sets the DE flag in ST1 to a 1, and sets bits 7 and 6 in ST0 to 0 and 1, respectively.

The Write Data command operates in much the same manner as the Read Data command. Refer to the Read Data command for the handling of the following items:

- Transfer Capacity
- End of Track (EN) flag
- No Data (ND) flag
- Head Unload Time (HUT) interval
- ID information when the processor terminates command (see Table 4)
- Definition of Data Length (DTL) when N = 0 and when N ≠ 0

Table 4. DDFDC Command Termination Values

Command Phase ID		Final Sector Transferred to/from Data Bus	Result Phase ID			
Multi-Track (MT)	Head Number (HD)		Track Number (T)	Head Number (H)	Sector Number (R)	No. of Data Bytes (N)
0	0	Less than EOT	NC	NC	R + 1	NC
	0	Equal to EOT	T + 1	NC	01	NC
	1	Less than EOT	NC	NC	R + 1	NC
	1	Equal to EOT	T + 1	NC	01	NC
1	0	Less than EOT	NC	NC	R + 1	NC
	0	Equal to EOT	NC	LSB	01	NC
	1	Less than EOT	NC	NC	R + 1	NC
	1	Equal to EOT	T + 1	LSB	01	NC

Notes:
1. NC (No Change): The same value as the one at the beginning of command execution.
2. LSB (Least Significant Bit): The least significant bit of H is complemented.

In the Write Data mode, data transfers from the data bus to the DDFDC must occur within 27 μs in the FM mode, and within 13 μs in the MFM mode. If the time interval between data transfers is longer than this, then the DDFDC terminates the Write Data command, sets the Over Run (OR) flag in ST1 to a 1, and sets bits 7 and 6 in ST0 to 0 and 1, respectively.

Command Phase:

R/W	BYTE	7	6	5	4	3	2	1	0
W	1	MT	MF	0	0	0	1	0	1
	2	X	X	X	X	X	HD	US1	US0
	3	Track Number (T)							
	4	Head Number (H)							
	5	Sector Number (R)							
	6	Number of Data Bytes per Sector (N)							
	7	End of Track (EOT)							
	8	Gap Length (GPL)							
	9	Data Length (DTL)							

Result Phase:

R	1	Status Register 0 (ST0)
	2	Status Register 1 (ST1)
	3	Status Register 2 (ST2)
	4	Track Number (T)
	5	Head Number (H)
	6	Sector Number (R)
	7	Number of Data Bytes per Sector (N)

WRITE DELETED DATA

The Write Deleted Data command is the same as the Write Data command except a Deleted Data Address Mark is written at the beginning of the Data field instead of the normal Data Address Mark.

Command Phase:

R/W	BYTE	7	6	5	4	3	2	1	0
W	1	MT	MF	0	0	1	0	0	1
	2	X	X	X	X	X	HD	US1	US0
	3	Track Number (T)							
	4	Head Number (H)							
	5	Sector Number (R)							
	6	Number of Data Bytes per Sector (N)							
	7	End of Track (EOT)							
	8	Gap Length (GPL)							
	9	Data Length (DTL)							

Result Phase:

R	1	Status Register 0 (ST0)
	2	Status Register 1 (ST1)
	3	Status Register 2 (ST2)
	4	Track Number (T)
	5	Head Number (H)
	6	Sector Number (R)
	7	Number of Data Bytes per Sector(N)

READ DELETED DATA

The Read Deleted Data command is the same as the Read Data command except that if SK = 0 when the DDFDC detects a **Data Address Mark** at the beginning of a Data field, it reads all the data in the sector and sets the CM flag in ST2 to a 1, and then terminates the command. If SK = 1, then the DDFDC skips the sector with the **Data Address Mark** and reads the next sector.

Command Phase:

R/W	BYTE	7	6	5	4	3	2	1	0
W	1	MT	MF	SK	0	1	1	0	0
	2	X	X	X	X	X	HD	US1	US0
	3	Track Number (T)							
	4	Head Number (H)							
	5	Sector Number (R)							
	6	Number of Data Bytes per Sector (N)							
	7	End of Track (EOT)							
	8	Gap Length (GPL)							
	9	Data Length (DTL)							

Result Phase:

R	1	Status Register 0 (ST0)
	2	Status Register 1 (ST1)
	3	Status Register 2 (ST2)
	4	Track Number (T)
	5	Head Number (H)
	6	Sector Number (R)
	7	Number of Data Bytes per Sector (N)

READ A TRACK

The Read a Track command is similar to the Read Data command except that this is a continuous read operation where all Data fields from each of the sectors on a track are read and transferred to the data bus. Immediately after encountering the Index Hole, the DDFDC starts reading the Data fields as continuous blocks of data. This command terminates when the number of sectors read is equal to EOT. Multi-track operations are not allowed with this command.

If the DDFDC finds an error in the ID or Data CRC check bytes, it continues to read data from the track. The DDFDC compares the ID information read from each sector with the value stored in the IDR, and sets the ND flag in ST1 to a 1 if there is no match.

If the DDFDC does not find an ID Address Mark on the disk after it encounters the Index Hole for the second time it terminates the command, sets the Missing Address Mark (MA) flag in ST1 to a 1, and sets bits 7 and 6 of ST0 to 0 and 1, respectively.

Command Phase:

R/W	BYTE	7	6	5	4	3	2	1	0
W	1	0	MF	SK	0	0	0	1	0
	2	X	X	X	X	X	HD	US1	US0
	3	Track Number (T)							
	4	Head Number (H)							
	5	Sector Number (R)							
	6	Number of Data Bytes per Sector (N)							
	7	End of Track (EOT)							
	8	Gap Length (GPL)							
	9	Data Length (DTL)							

Result Phase:

R	1	Status Register 0 (ST0)
	2	Status Register 1 (ST1)
	3	Status Register 2 (ST2)
	4	Track Number (T)
	5	Head Number (H)
	6	Sector Number (R)
	7	Number of Data Bytes per Sector (N)

READ ID

The two-byte Read ID command returns the present position of the read/write head. The DDFDC obtains the value from the first ID field it is able to read, sets bits 7 and 6 in ST0 to 0 and terminates the command.

If no proper ID Address Mark is found on the disk before the Index Hole is encountered for the second time then the Missing Address Mark (MA) flag in ST1 is set to a 1, and if no data is found then the ND flag to a 1 is also set in ST1. Bits 7 and 6 in ST0 are set to 0 and 1, respectively and the command is terminated.

During this command there is no data transfer between DDFDC and the data bus except during the result phase.

Command Phase:

R/W	BYTE	7	6	5	4	3	2	1	0
W	1	0	MF	0	0	1	0	1	0
	2	X	X	X	X	X	HD	US1	US0

Result Phase:

R	1	Status Register 0 (ST0)
	2	Status Register 1 (ST1)
	3	Status Register 2 (ST2)
	4	Track Number (T)
	5	Head Number (H)
	6	Sector Number (R)
	7	Number of Data Bytes per Sector (N)

FORMAT A TRACK

The six-byte Format a Track command formats an entire track. After the Index Hole is detected, data is written on the disk: Gaps, Address Marks, ID fields and Data fields; all are recorded in either the double-density IBM System 34 format (MF = 1) or the single-density IBM 3740 format (MF = 0). The particular format written is also controlled by the values of Number of Bytes/Sector (N), Sectors/Track (ST), Gap Length (GPL) and Data Pattern (D) which are supplied by the processor during the command phase. The Data field is filled with the data pattern stored in D.

The ID field for each sector is supplied by the processor in response to four data requests per sector issued by the DDFDC. The type of data request depends upon the Non-DMA flag (ND) in the Specify command. In the DMA mode (ND = 0), the DDFDC asserts the DMA Request (DRQ) output four times per sector. In the Non-DMA mode (ND = 1), the DDFDC asserts Interrupt Request ($\overline{IRQ}$) output four times per sector.

The processor must write one data byte in response to each request, sending (in the consecutive order) the Track Number (T), Head Number (H), Sector Number (R) and Number of Bytes/Sector (N). This allows the disk to be formatted with non-sequential sector numbers, if desired.

The processor must send new values for T, H, R, and N to the DDFDC for each sector on the track. For sequential formatting R is incremented by one after each sector is formatted, thus, R contains the total numbers of sectors formatted when it is read during the result phase. This incrementing and formatting continues for the whole track until the DDFDC, upon encountering the Index Hole for the second time, terminates the command and sets bits 7 and 6 in ST0 to 0.

If the Fault (FLT) signal is high from the FDD at the end of a write operation, the DDFDC sets the Equipment Check (EC) flag in ST0 to a 1, sets bits 7 and 6 of ST0 to 0 and 1, respectively, and terminates the command. Also, a low (RDY) signal at the beginning of a command execution phase causes bits 7 and 6 of ST0 to be set to 0 and 1, respectively.

Table 5 shows the relationship between N, ST, and GPL for various disk and sector sizes.

Table 5. Standard Floppy Disk Sector Size Relationship

Disk Size	Mode	Sector Size Bytes/Sector	No. of Data Bytes/Sector (N)	No. of Sectors/Track (ST)	Gap Length (GPL)[4]		Remarks
					Read/Write Command[1]	Format Command[2]	
8″	FM	128	00	1A	07	1B	
		256	01	0F	0E	2A	
		512	02	08	1B	3A	
		1024	03	04	47	8A	
		2048	04	02	C8	FF-	
		4096	05	01	C8	FF	
	MFM[3]	256	01	1A	0E	36	
		512	02	0F	1B	54	
		1024	03	08	35	74	
		2048	04	04	99	FF	
		4096	05	02	C8	FF	
		8192	06	01	C8	FF	
5¼″	FM	128	00	12	07	09	
		128	00	10	10	19	
		256	01	08	18	30	
		512	02	04	46	87	
		1024	03	02	C8	FF	
		2048	04	01	C8	FF	
	MFM[3]	256	01	12	0A	0C	
		256	01	10	20	32	
		512	02	08	2A	50	
		1024	03	04	80	F0	
		2048	04	02	C8	FF	
		4096	05	01	C8	FF	
3½″	FM	128	00	0F	07	1B	
		256	01	09	0E	2A	
		512	02	05	1B	3A	
	MFM[3]	256	01	0F	0E	36	
		512	02	09	1B	54	
		1024	03	05	35	74	

Notes:
1. Suggested values of GPL in Read or Write commands to avoid overlapping between Data field and ID field of contiguous sections.
2. Suggested values of GPL in Format a Track command.
3. In MFM mode the DDFDC cannot perform a read/write/format operation with 128 bytes/sector (N = 00).
4. Values of ST and GPL are in hexadecimal.

Command Phase:

R/W	BYTE	7	6	5	4	3	2	1	0
W	1	0	MF	0	0	1	1	0	1
	2	X	X	X	X	X	HD	US1	US0
	3	Number of Bytes per Sector (N)							
	4	Sectors per Track (ST)							
	5	Gap Length (GPL)							
	6	Data Pattern (D)							

Result Phase:

R	1	Status Register 0 (ST0)
	2	Status Register 1 (ST1)
	3	Status Register 2 (ST2)
	4	Track Number (T)*
	5	Head Number (H)*
	6	Sector Number (R)*
	7	Number of Data Bytes per Sector (N)*

* The ID information has no meaning in this command.

SCAN COMMANDS

The scan commands compare data read from the disk to data supplied from the data bus. The DDFDC compares the data, and looks for a sector of data which meets the conditions of $D_{FDD} = D_{BUS}$, $D_{FDD} \leq D_{BUS}$, or $D_{FDD} \geq D_{BUS}$ (D = the data pattern in hexadecimal). A magnitude comparison is performed (FF = largest number, 00 = smallest number). The hexadecimal byte of FF either from the bus or from FDD can be used as a mask byte because it always meets the condition of the compare. After a whole sector of data is compared, if the conditions are not met, the sector number is incremented (R + STP → R), and the scan operation is continued. The scan operation continues until one of the following events occur: the conditions for scan are met (equal, low or equal, or high or equal), the last sector on the track is reached (EOT), or TC is received.

If conditions for scan are met, the DDFDC sets the Scan Hit (SH) flag in ST2 to a 1, and terminates the command. If the conditions for scan are not met between the starting sector (as specified by R) and the last sector on the track (EOT), then the DDFDC sets the Scan Not Satisfied (SN) flag in ST2 to a 1, and terminates the command. The receipt of TC from the processor or DMA controller during the scan operation will cause the DDFDC to complete the comparison of the particular byte which is in process, and then to terminate the command. Table 6 shows the status of bits SH and SN under various conditions of scan.

Table 6. Scan Status Codes

Command	Status Register 2		Comments
	Bit 2 = SN	Bit 3 = SH	
Scan Equal	0	1	$D_{FDD} = D_{BUS}$
	1	0	$D_{FDD} \neq D_{BUS}$
Scan Low or Equal	0	1	$D_{FDD} = D_{BUS}$
	0	0	$D_{FDD} < D_{BUS}$
	1	0	$D_{FDD} > D_{BUS}$
Scan High or Equal	0	1	$D_{FDD} = D_{BUS}$
	0	0	$D_{FDD} > D_{BUS}$
	1	0	$D_{FDD} < D_{BUS}$

If SK = 0 and the DDFDC encounters a Deleted Data Address Mark on one of the sectors, it regards that sector as the last sector of the track, sets the Control Mark (CM) bit in ST2 to a 1 and terminates the command. If SK = 1, the DDFDC skips the sector with the Deleted Data Address Mark, sets the CM flag to a 1 in order to show that a Deleted Sector has been encountered, and reads the next sector.

When either the STP sectors are read (contiguous sectors = 01, or alternate sectors = 02) or MT (Multi-Track) is set, **the last sector on the track must be read.** For example, if STP = 02, MT = 0, the sectors are numbered sequentially 1 through 26, and the scan command starts reading at sector 21. Sectors 21, 23, and 25 are read, then the next sector (26) is skipped and the Index Hole is encountered before the EOT value of 26 can be read. This results in an abnormal termination of the command. If the EOT had been set at 25 or the scanning started at sector 20, then the scan command would be completed in a normal manner.

During a scan command data is supplied from the data bus for comparison against the data read from the disk. In order to avoid having the Over Run (OR) flag set in ST1, data must be available from the data bus in less than 27 μs (FM mode) or 13 μs (MFM mode). If an OR occurs, the DDFDC terminates the command and sets bits 7 and 6 of ST0 to 0 and 1, respectively.

The following tables specify the command bytes and describe the result bytes for the three scan commands.

SCAN EQUAL

Command Phase:

R/W	BYTE	7	6	5	4	3	2	1	0
W	1	MT	MF	SK	1	0	0	0	1
	2	X	X	X	X	X	HD	US1	US0
	3	Track Number (T)							
	4	Head Number (H)							
	5	Sector Number (R)							
	6	Number of Data Bytes per Sector (N)							
	7	End of Track (EOT)							
	8	Gap Length (GPL)							
	9	Sector Test Process (STP)							

Result Phase:

R		
	1	Status Register 0 (ST0)
	2	Status Register 1 (ST1)
	3	Status Register 2 (ST2)
	4	Track Number (T)
	5	Head Number (H)
	6	Sector Number (R)
	7	Number of Data Bytes per Sector (N)

SCAN LOW OR EQUAL

Command Phase:

R/W	BYTE	7	6	5	4	3	2	1	0
W	1	MT	MF	SK	1	1	0	0	1
	2	X	X	X	X	X	HD	US1	US0
	3	Track Number (T)							
	4	Head Number (H)							
	5	Sector Number (R)							
	6	Number of Data Bytes per Sector (N)							
	7	End of Track (EOT)							
	8	Gap Length (GPL)							
	9	Sector Test Process (STP)							

Result Phase:

R		
	1	Status Register 0 (ST0)
	2	Status Register 1 (ST1)
	3	Status Register 2 (ST2)
	4	Track Number (T)
	5	Head Number (H)
	6	Sector Number (R)
	7	Number of Data Bytes per Sector (N)

SCAN HIGH OR EQUAL

Command Phase:

R/W	BYTE	7	6	5	4	3	2	1	0
W	1	MT	MF	SK	1	1	1	0	1
	2	X	X	X	X	X	HD	US1	US0
	3	Track Number (T)							
	4	Head Number (H)							
	5	Sector Number (R)							
	6	Number of Data Bytes per Sector (N)							
	7	End of Track (EOT)							
	8	Gap Length (GPL)							
	9	Sector Test Process (STP)							

Result Phase:

R	1	Status Register 0 (ST0)
	2	Status Register 1 (ST1)
	3	Status Register 2 (ST2)
	4	Track Number (T)
	5	Head Number (H)
	6	Sector Number (R)
	7	Number of Data Bytes per Sector (N)

SEEK

The three-byte Seek command steps the FDD read/write head from track to track. The DDFDC has four independent Present Track Registers for each drive. They are cleared only by the Recalibrate command. The DDFDC compares the Present Track Number (PTN) which is the current head position with the New Track Number (NTN), and if there is a difference, performs the following operation:

If PTN < NTN: Sets the direction output (LCT/DIR) high and issues step pulses (FR/STP) to the FDD to cause the read/write head to step in.

If PTN > NTN: Sets the direction output (LCT/DIR) low and issues step pulses to the FDD to cause the read/write head to step out.

The rate at which step pulses are issued is controlled by the Step Rate Time (SRT) in the Specify command. After each step pulse is issued, NTN is compared against PTN. When NTN = PTN, then the Seek End (SE) flag in ST0 is set to a 1, bits 7 and 6 in ST0 are set to 0, and the command is terminated. At this point DDFDC asserts $\overline{IRQ}$.

The FDD Busy flag (bit 0-3) in the Main Status Register (MSR) corresponding to the FDD performing the Seek operation is set to a 1.

After command termination, all FDD Busy bits set are cleared by the Sense Interrupt Status command.

During the command phase of the Seek operation the DDFDC sets the Controller Busy (CB) flag in the MSR to 1; but during the execution phase the CB flag is set to 0 to indicate DDFDC non-busy. While the DDFDC is in the non-busy state, another Seek command may be issued, and in this manner parallel seek operations may be performed on all drives at once.

No command other than Seek will be accepted while the DDFDC is sending step pulses to any FDD. If a different command type is attempted, the DDFDC will set bits 7 and 6 in ST0 to a 1 and 0, respectively, to indicate an invalid command.

If the FDD is in a not ready state at the beginning of the command execution phase or during the seek operation, then the DDFDC sets the Not Ready (NR) flag in ST0 to a 1, sets ST0 bits 7 and 6 to 0 and 1, respectively, and terminates the command.

If the time to write the three bytes of the Seek command exceeds 150 μs, the time between the first two step pulses may be shorter than the Step Rate Time (SRT) defined by the Specify command by as much as 1 ms.

Command Phase:

R/W	BYTE	7	6	5	4	3	2	1	0
W	1	0	0	0	0	1	1	1	1
	2	X	X	X	X	X	0	US1	US0
	3	New Track Number (NTN)							

Result Phase: None.

RECALIBRATE

This two-byte command retracts the FDD read/write head to the Track 0 position. The DDFDC clears the contents of the PTN counters, and checks the status of the Track 0 signal from the FDD. As long as the Track 0 signal (TRK0) is low, the direction signal (LCT/DIR) output remains low and step pulses are issued on FR/STP. When TRK0 goes high the DDFDC sets the Seek End (SE) flag in ST0 to a 1 and terminates the command. If the TRK0 is still low after 256 step pulses have been issued, the DDFDC sets Seek End (SE) and Equipment Check (EC) flags in ST0 to 1s, sets bits 7 and 6 of ST0 to 0 and 1, respectively, and terminates the command.

The ability to do overlap Recalibrate commands to multiple FDDs and the loss of the RDY signal, as described in the Seek command, also applies to the Recalibrate command.

Command Phase:

R/W	BYTE	7	6	5	4	3	2	1	0
W	1	0	0	0	0	0	1	1	1
	2	X	X	X	X	X	0	US1	US0

Result Phase: None.

SENSE INTERRUPT STATUS

Interrupt request ($\overline{IRQ}$) is asserted by the DDFDC when any of the following conditions occur:

1. Upon entering the result phase of:
   a. Read Data command
   b. Read a Track command
   c. Read ID command
   d. Read Deleted Data command
   e. Write Data command
   f. Format a Track command
   g. Write Deleted Data command
   h. Scan commands
2. Ready (RDY) line from the FDD changes state
3. Seek or Recalibrate command termination
4. During execution phase in the Non-DMA mode

$\overline{IRQ}$ caused by reasons 1 and 4 above occur during normal command operations and are easily discernible by the processor. During an execution phase in Non-DMA mode, bit 5 in the MSR is set to 1. Upon entering result phase this bit is set to 0. Reasons 1 and 4 do not require the Sense Interrupt Status command. The interrupt is cleared by reading or writing data to DDFDC. Interrupts caused by reasons 2 and 3 are identified with the aid of the Sense Interrupt Status command. This command resets $\overline{IRQ}$ and sets/resets bits 5, 6, and 7 of ST0 to identify the cause of the interrupt. Table 7 defines the seek and interrupt codes.

The Sense Interrupt Status command is used in conjunction with the Seek and Recalibrate commands which have no result phase. When the disk drive has reached the desired head position the DDFDC asserts interrupt output. The host CPU must thenissue a Sense Interrupt Status command to determine the actual cause of the interrupt, which could be Seek End or a change in ready status from one of the drives (see example in Figure 3).

Issuing a Sense Interrupt Status command without an interrupt pending is treated as an invalid command.

Table 7. ST0 Seek and Interrupt Code Definition for Sense Interrupt Status

Status Register 0 (ST0) Bits			
Interrupt Code (IC)		Seek End (SE)	Cause
7	6	5	
1	1	0	RDY line changed state, either polarity
0	0	1	Normal termination of Seek or Recalibrate command
0	1	1	Abnormal termination of Seek or Recalibrate command

Command Phase:

R/W	BYTE	7	6	5	4	3	2	1	0
W	1	0	0	0	0	1	0	0	0

Result Phase:

R	1	Status Register 0 (ST0)
	2	Present Track Number (PTN)

SPECIFY

The three-byte Specify command sets the initial values for each of the three internal timers. The Head Unload Time (HUT) defines the time from the end of the execution phase of one of the read/write commands to the head unload state. This timer is programmable from 16 to 240 ms in increments of 16 ms (1 = 16 ms, 2 = 32 ms,. . .F = 240 ms).

The Step Rate Time (SRT) defines the time interval between adjacent step pulses. This timer is programmable from 1 to 16 ms in increments of 1 ms (F = 1 ms, E = 2 ms, D = 3 ms,. . . 0 = 16 ms).

The Head Load Time (HLT) defines the time between the Head Load (HDL) signal going high and the start of the read/write operation. This timer is programmable from 2 to 254 ms in increments of 2 ms (01 = 2 ms, 02 = 4 ms, 03 = 6 ms,. . . 7F = 254 ms).

The time intervals are a direct function of the clock (CLK on pin 19). Times indicated above are for an 8 MHz clock. If the clock is reduced to 4 MHz (mini-floppy application) then all time intervals are increased by a factor of two.

The choice of DMA or Non-DMA operation is made by the Non-DMA mode (ND) bit. When this bit = 1 the Non-DMA mode is selected, and when ND = 0 the DMA mode is selected.

Command Phase:

R/W	BYTE	7	6	5	4	3	2	1	0
W	1	0	0	0	0	0	0	1	1
	2	SRT				HUT			
	3	HLT							ND

SRT — Step Rate Time
HUT — Head Unload Time
HLT — Head Load Time
ND — Non-DMA mode

Result Phase: None.

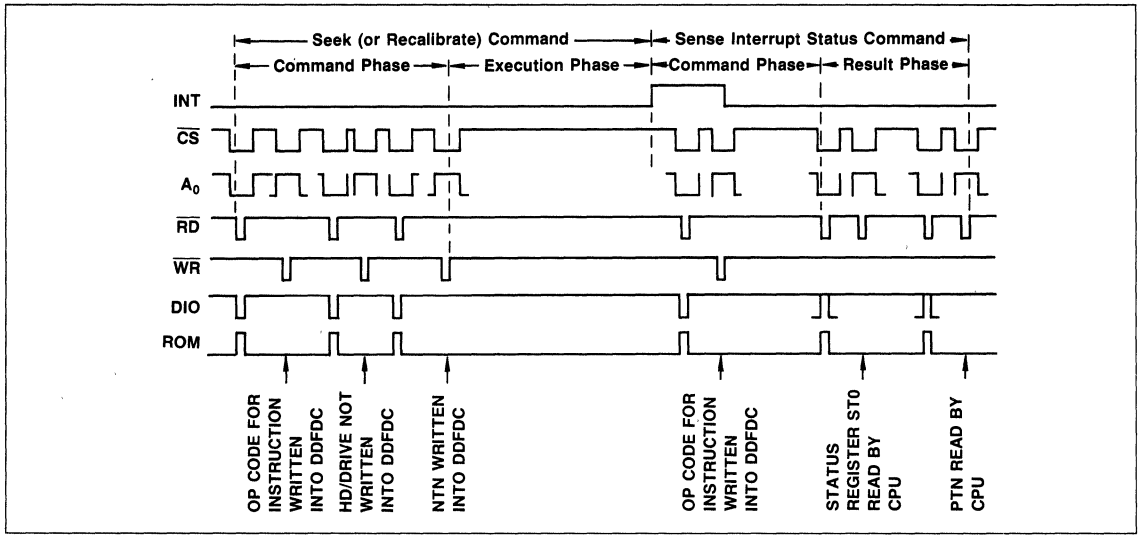


Figure 3. Sense Interrupt Status

SENSE DRIVE STATUS

This two-byte command obtains and reports the status of the FDDs. Status Register 3 (ST3) is returned in the result phase and contains the drive status.

Command Phase:

R/W	BYTE	7	6	5	4	3	2	1	0
W	1	0	0	0	0	0	1	0	0
	2	X	X	X	X	X	HD	US1	US0

Result Phase:

R	1	Status Register 3 (ST3)

INVALID COMMAND

If an invalid command (i.e., a command not previously defined) is received by the DDFDC, then the DDFDC terminates the command after setting bits 7 and 6 of ST0 to 1 and 0, respectively. The DDFDC does not generate an interrupt during this condition. Bits 6 and 7 (DIO and RQM) in the MSR are both set to a 1 indicating to the processor that the DDFDC is in the result phase and that ST0 must be read. A hex 80 in ST0 indicates an invalid command was received.

A Sense Interrupt Status command must be sent after a Seek or Recalibrate interrupt, otherwise the DDFDC considers the next command to be an invalid command.

In some applications the user may wish to use this command as a No-Op command, to place the DDFDC in a standby or no operation state.

Command Phase:

R/W	BYTE	7	6	5	4	3	2	1	0
W	1	Invalid Codes							

Result Phase:

R	1	Status Register 0 (ST0) = 80

PROCESSOR INTERFACE

During the command or result phases, the Main Status Register (MSR) must be read by the processor before each byte of information is transferred to, or from, the DDFDC Data Register. After each byte of data is written to, or read from, the Data Register, the processor should wait 12 μs before reading the MSR. Bits 6 and 7 in the MSR must be a 0 and 1, respectively, before each command byte can be written to the DDFDC. During the result phase, bits 6 and 7 of the MSR must both be 1s prior to reading each byte from the Data Register onto the data bus. Note that this status reading of bits 6 and 7 of the MSR before each byte transfer to and from the DDFDC is required in only the command and result phases and not during the execution phase.

During the result phase all bytes shown in the result phase must be read by the processor. The Read Data command, for example, has seven bytes of data in the result phase. All seven Bytes must be read to successfully complete the Read Data command. The DDFDC will not accept a new command until all seven bytes have been read. Other commands may require fewer bytes to be read during the result phase.

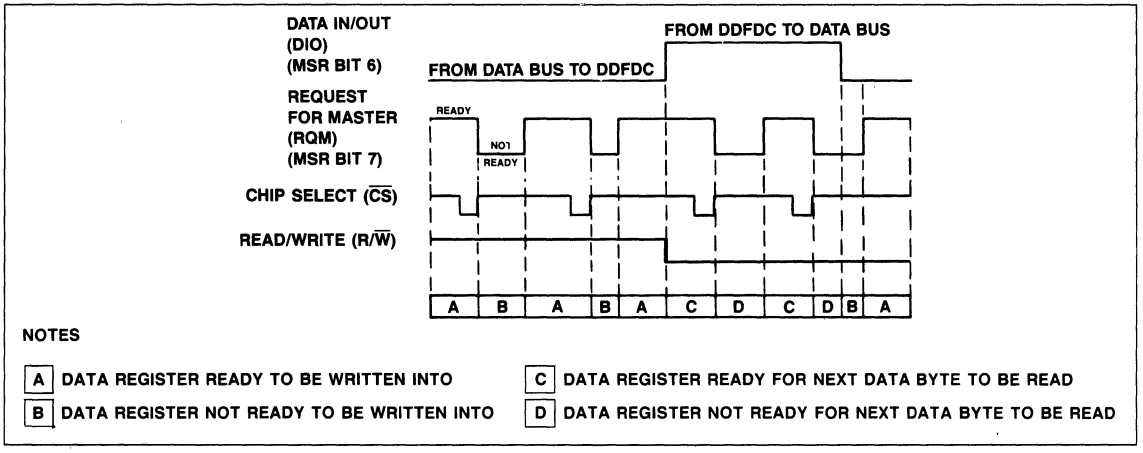


Figure 4. DDFDC and System Data Transfer Timing

INTERRUPT REQUEST MODE

During the execution phase, the MSR need not be read. The receipt of each data byte from the FDD is indicated by $\overline{IRQ}$ low on pin 18. When the DDFDC is in Non-DMA mode, $\overline{IRQ}$ is asserted during the execution phase. When the DDFDC is in the DMA mode, $\overline{IRQ}$ is asserted at the result phase. The $\overline{IRQ}$ signal is reset by a read (R/$\overline{W}$ high) or write (R/$\overline{W}$ low) of data to the DDFDC. A further explanation of the $\overline{IRQ}$ signal is described in the Sense Interrupt Status command on page 16. If the system cannot handle interrupts fast enough (within 13 μs for MFM mode or 27 μs for FM mode), it should poll bit 7 (RQM) in the MSR. In this case, RQM in the MSR functions as an Interrupt Request ($\overline{IRQ}$). If the RQM bit is not set, the Over Run (OR) flag in ST1 will be set to a 1 and bits 7 and 6 of ST0 will be set to a 0 and 1, respectively.

DMA MODE

When the DDFDC is in the DMA mode (ND = 0 in the third command byte of the Specify command), DRQ (DMA Request) is asserted during the execution phase (rather than $\overline{IRQ}$) to request the transfer of a data byte between the data bus and the DDFDC.

During a read command, the DDFDC asserts $\overline{REQ}$ as each byte of data is available to be read. The DMA controller responds to this request with both $\overline{DACK}$ low (DMA Acknowledge) and R/$\overline{W}$ high (read). When DACK goes low the DMA Request is reset ($\overline{REQ}$ high). After the execution phase has been completed ($\overline{DONE}$ low or the EOT sector is read), $\overline{IRQ}$ is asserted to indicate the beginning of the result phase. When the first byte of data is read during the result phase, $\overline{IRQ}$ is reset high.

During a write command, the DDFDC asserts $\overline{REQ}$ as each byte of data is required. The DMA controller responds to this request with $\overline{DACK}$ low (DMA Acknowledge) and R/$\overline{W}$ low (write). When $\overline{DACK}$ goes low the DMA Request is reset ($\overline{REQ}$ high). After the execution phase has been completed ($\overline{DONE}$ low or the EOT sector is written), $\overline{IRQ}$ is asserted. This signals the beginning of the result phase. When the first byte of data is read during the result phase, the $\overline{IRQ}$ is reset high.

FDD POLLING

After the Specify command has been received by the DDFDC, the Unit Select lines (US0 and US1) begin the polling mode. Between commands (and between step pulses in the Seek Command) the DDFDC polls all the FDD's looking for a change in the RDY line from any of the drives. If the RDY line changes state (usually due to the door opening or closing) then the DDFDC asserts $\overline{IRQ}$. When Status Register 0 (ST0) is read (after Sense Interrupt Status command is issued), Not Ready (NR = 1) will be indicated. The polling of the RDY line by the DDFDC occurs continuously between commands, thus notifying the processor which drives are on- or off-line. Each drive is polled every 1.024 ms except during read/write commands.

R68465 (FM MODE)

FIELD	GAP 4a	SYNC	IAM	GAP 1	SYNC	IDAM	CYL	HD	SEC	NO	CRC	GAP 2	SYNC	DATA AM	DATA		GAP 3	GAP 4b
NO. OF BYTES	40×	6×		26×	6×							11×	6×		①	CRC	①	
DATA	FF	00	FC	FF	00	FE						FF	00	FB OR F8				

INDEX ⎍ ⊢——— REPEAT N TIMES ———⊣

R68265 (FM MODE)

FIELD	GAP 1	SYNC	IDAM	CYL	HD	SEC	NO	CRC	GAP 2	SYNC	DATA AM	DATA		GAP 3	GAP 4
NO OF BYTES	16×	6×							11×	6×		①	CRC	①	
DATA	FF	00	FC						FF	00	FB OR F8				

INDEX ⎍ ⊢——— REPEAT N TIMES ———⊣

R68465 (MFM MODE)

GAP 4a	SYNC	IAM		GAP 1	SYNC	IDAM		CYL	HD	SEC	NO	CRC	GAP 2	SYNC	DATA AM		DATA		GAP 3	GAP 4b
80×	12×	3×		50×	12×	3×							22×	12×	3×	FB	①	CRC	①	
4E	00	C2	FC	4E	00	A1	FE						4E	00	A1	F8				

INDEX ⎍ ⊢——— REPEAT N TIMES ———⊣

R68265 (MFM MODE)

FIELD	GAP 1	SYNC	IDAM		CYL	HD	SEC	NO	CRC	GAP 2	SYNC	DATA AM		DATA		GAP 3	GAP 4
NO. OF BYTES	32×	12×	3×							22x	12×	3×	FB	①	CRC	①	
DATA	4E	00	A1	FE						4E	00	A1	F8				

INDEX ⎍ ⊢——— REPEAT N TIMES ———⊣

Figure 5. DDFDC Formats

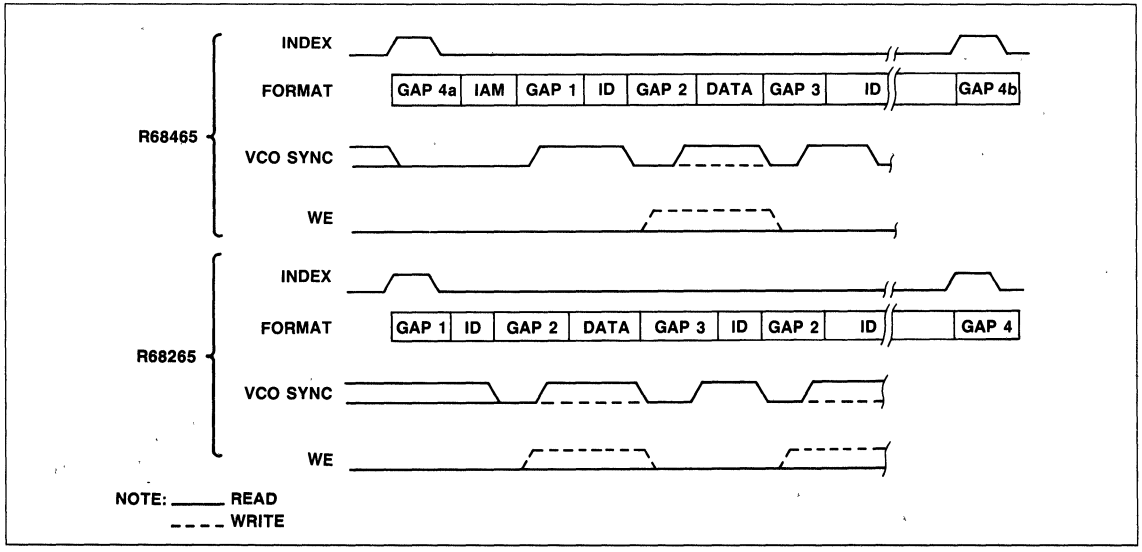
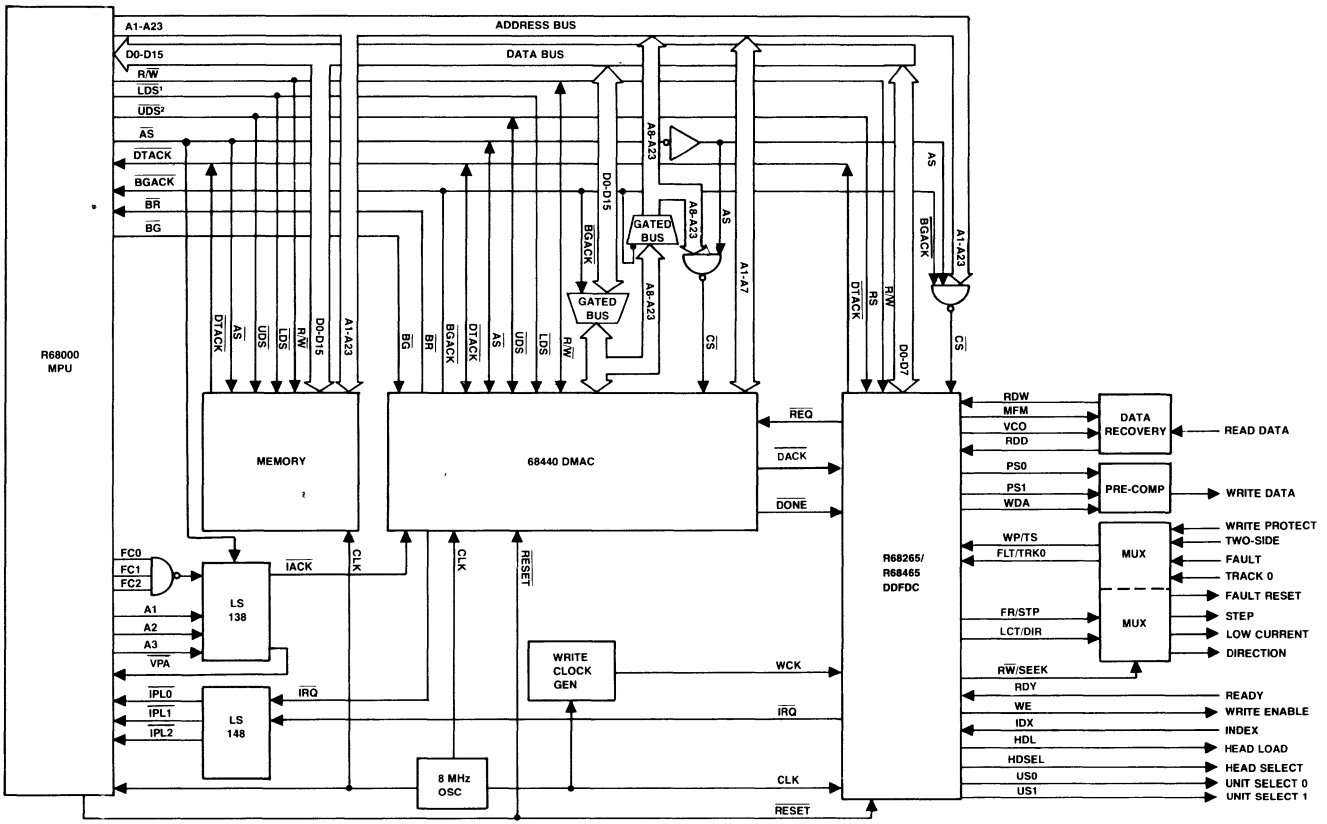


Figure 6. DDFDC Formats



[1] Signal not used in interface to 68008 MPU.
[2] UDS changed to DS when interfaced to 68008 MPU.

Figure 7. R68265/R68465 DDFDC Interface to R68000

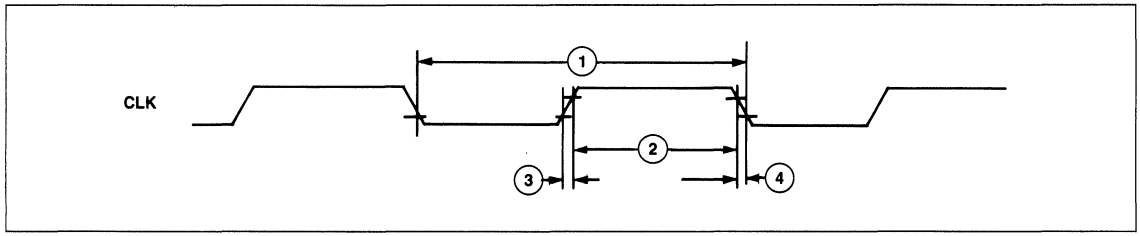


Figure 8. Clock Timing

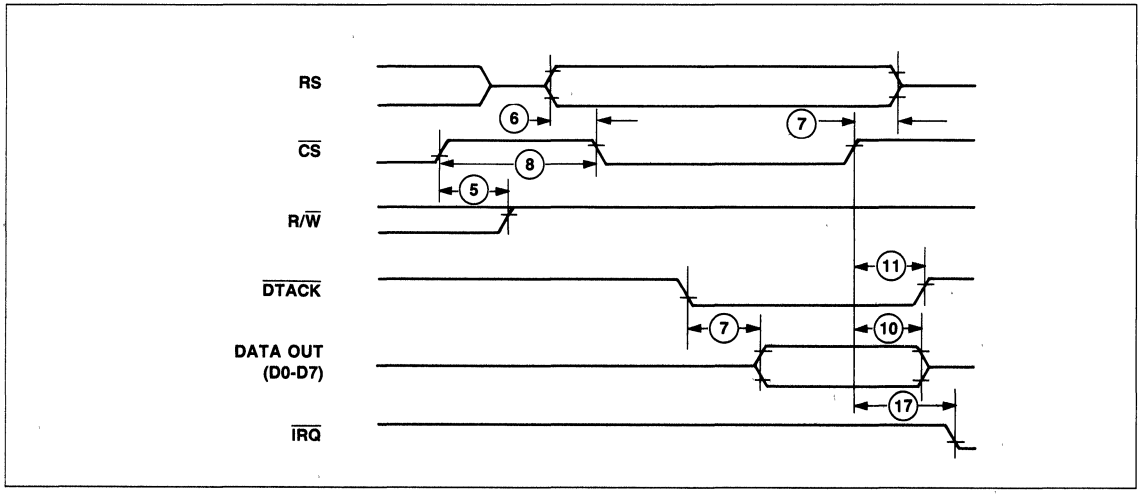


Figure 9. DDFDC Read Cycle Timing

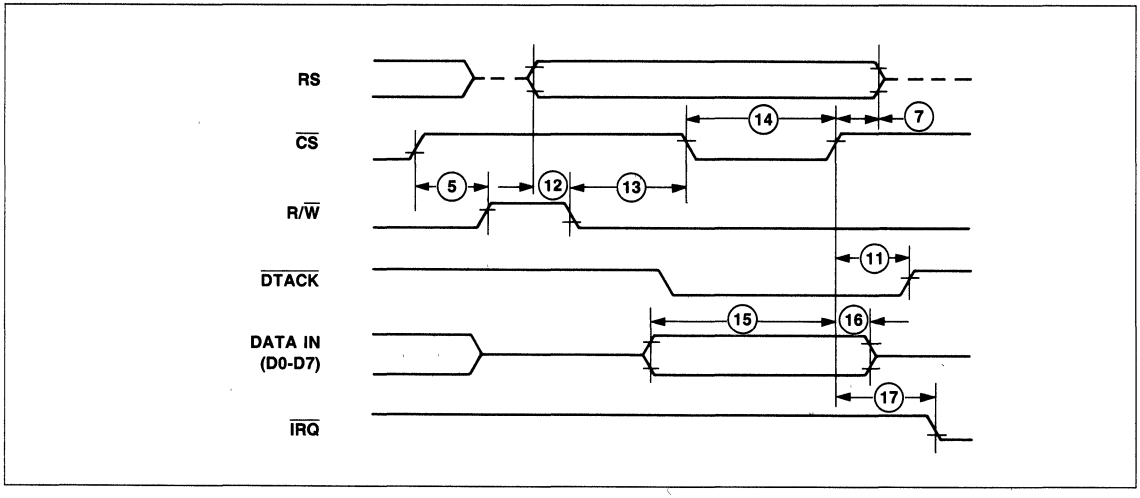


Figure 10. DDFDC Write Cycle Timing

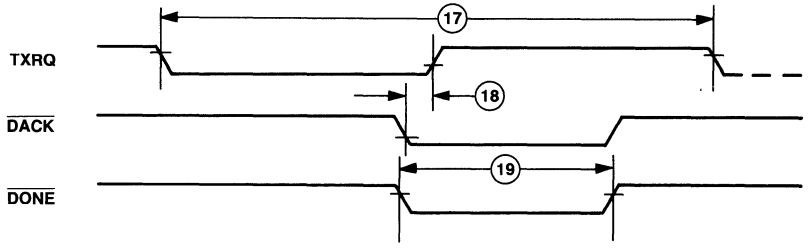


Figure 11. DMA Operation Timing

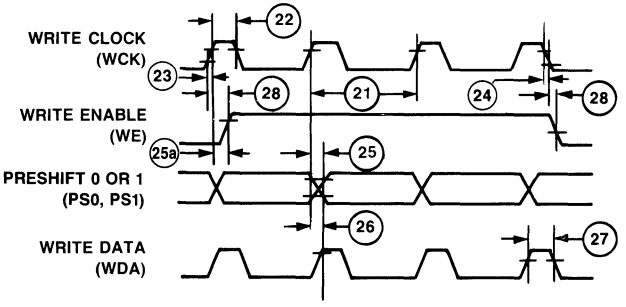
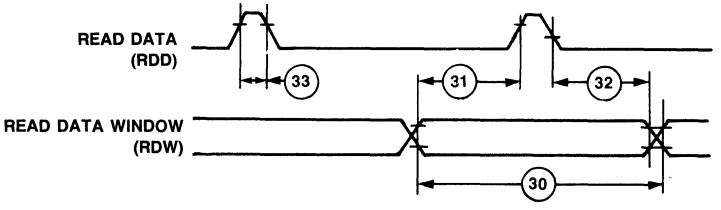


Figure 12. FDD Write Operation Timing



NOTE:
EITHER POLARITY DATA WINDOW IS VALID

Figure 13. FDD Read Operation Timing

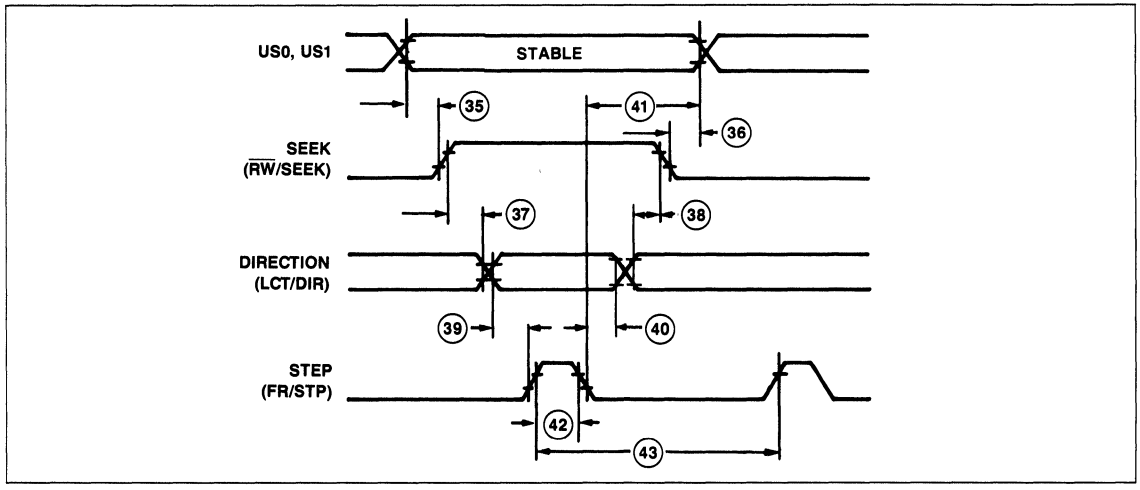


Figure 14. Seek Operation Timing

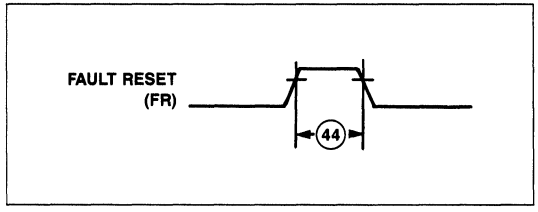


Figure 15. Fault Reset Timing

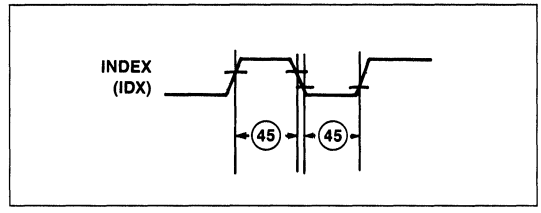


Figure 16. Index Timing

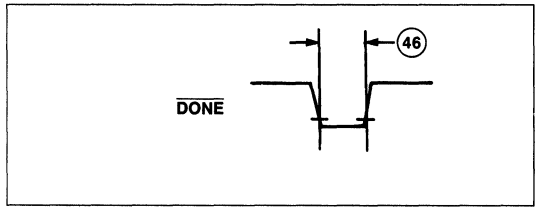


Figure 17. Terminal Count Timing

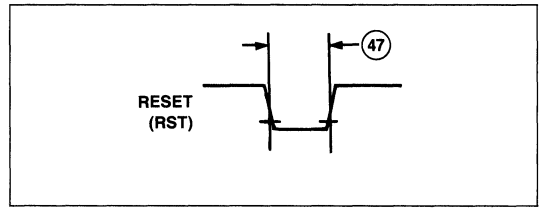
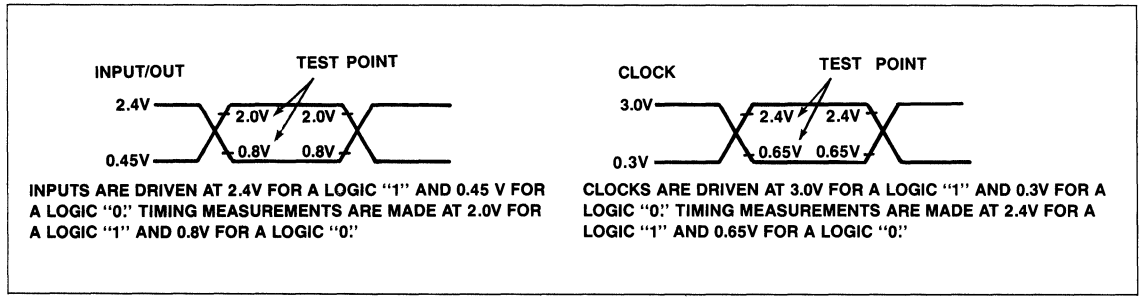


Figure 18. Reset Timing



INPUTS ARE DRIVEN AT 2.4V FOR A LOGIC "1" AND 0.45 V FOR A LOGIC "0." TIMING MEASUREMENTS ARE MADE AT 2.0V FOR A LOGIC "1" AND 0.8V FOR A LOGIC "0."

CLOCKS ARE DRIVEN AT 3.0V FOR A LOGIC "1" AND 0.3V FOR A LOGIC "0." TIMING MEASUREMENTS ARE MADE AT 2.4V FOR A LOGIC "1" AND 0.65V FOR A LOGIC "0."

Figure 19. AC Timing Measurement Conditions

AC CHARACTERISTICS

(V_{CC} = 5.0 Vdc ±5%, V_{SS} = 0 Vdc, T_A = 0°C to 70°C)

Ref. Fig.	No.	Characteristic		Symbol	Alt. Sym.	Min.	Typ.	Max.	Unit	Test Conditions
5	1	Clock Period	(8″ or 3-1/2″ FDD)	t_{CY}	ϕ_{CY}	120	125	500	ns	CLK = 8 MHz
			(5-1/4″ FDD)			—	250	—	ns	CLK = 4 MHz
	2	Clock High			t_{CA}	ϕ_0	40	—	—	ns	CLK = 8 MHz
	3	Clock Rise Time			t_{CLCH}	ϕ_r	—	—	20	ns	
	4	Clock Fall Time			t_{CHCL}	ϕ_f	—	—	20	ns	
6 and 7	5	$\overline{CS}$ High to R/$\overline{W}$ High			t_{SHRH}	t_{SR}	40	—	—	ns	
	6	Address Valid to $\overline{CS}$ Low			t_{AVSL}	t_{RA}	0	—	—	ns	
	7	$\overline{CS}$ High to Address Invalid			t_{SHAX}	t_{AH}	0	—	—	ns	
	8	$\overline{CS}$ High			t_{SHSL}	t_{SH}	150	—	—	ns	
	9	$\overline{DTACK}$ Low to Data Valid			t_{DLDV}	t_{RD}	—	—	90	ns	C_L = 100 pF
	10	$\overline{CS}$ High to Output High Z			t_{SHDZ}	t_{DF}	20	—	—	ns	
	11	$\overline{CS}$ High to $\overline{DTACK}$ High			t_{SHDH}	t_{DTK}	—	—	120	ns	
	12	Address Valid to R/$\overline{W}$ Low			t_{AVRL}	t_{WS}	20	—	—	ns	
	13	R/$\overline{W}$ Low to $\overline{CS}$ Low			t_{RLSL}	t_{WH}	80	—	—	ns	
	14	$\overline{CS}$ Low Pulse Width			t_{SLSH}	t_{SL}	250	—	—	ns	
	15	Data Valid to $\overline{CS}$ High			t_{DVSH}	t_{DSU}	150	—	—	ns	
	16	$\overline{CS}$ High to Data Invalid			t_{SHDZ}	t_{DHW}	5	—	—	ns	
8	17	$\overline{IRQ}$ Delay from $\overline{CS}$ High			t_{ILSH}	t_{IRQ}	—	—	500	μs	CLK = 8 MHz
	18	TXRQ Cycle Period			t_{TQCY}	t_{TCY}	13	—	—	ns	
	19	$\overline{ACK}$ Low to TXRQ Low			t_{AKTH}	t_{ACK}	—	—	200	t_{CY}	
	19a	TXRQ High to $\overline{ACK}$ Low (Delay)			t_{QHAL}	t_{MA}	200	—	—	ns	t_{CY} = 125 ns
	20	$\overline{DONE}$ Low Width			t_{NLNH}	t_{DONE}	1	—	—	ns	CLK = 8 MHz
9	21	WCK Cycle Time	(8″ or 3-1/2″ FDD)		t_{KCY}	t_{CY}	—	2	—	μs	MFM = 0
							—	1	—	μs	MFM = 1
			(5-1/4″ FDD)				—	4	—	μs	MFM = 0
							—	2	—	μs	MFM = 1
	22	WCK High Width			t_{KHKL}	t_0	80	250	350	ns	
	23	WCK Rise Time			t_{KLKH}	t_r	—	—	20	ns	
	24	WCK Fall Time			t_{KHKL}	t_f	—	—	20	ns	
	25	WCK High to PS0, PS1 Valid (Delay)			t_{KHPV}	t_{CP}	20	—	100	ns	
	25a	WCK High to WE High (Delay)			t_{DHEN}	t_{CWE}	20	—	100	ns	
	26	PS0, PS1 Valid to WDA High (Delay)			t_{PVDH}	t_{CD}	20	—	—	ns	
	27	WDA High Width			t_{DHDL}	t_{WDD}	t_{WCH} – 50	—	100	ns	
	28	WE High to WCK High or WE Low to WCK Low			t_{EHKH}	t_{WE}	20	—	100	ns	
10	30	RDW Cycle Time	(8″ or 3-1/2″ FDD)		t_{WCY}	t_{WCY}	—	2	—	μs	MFM = 0
							—	1	—	μs	MRM = 1
			(5-1/4″ FDD)				—	4	—	μs	MFM = 0
							—	2	—	μs	MFM = 1
	31	RDW Valid to RDD High (Setup)			t_{WVRH}	t_{WRD}	15	—	—	ns	
	32	RDD Low to RDW Invalid (Hold)			t_{RLWI}	t_{RDW}	15	—	—	ns	
	33	RDD High Width			t_{RHRL}	t_{RDD}	40	—	—	ns	
11	35	US0, US1 Valid to SEEK High (Setup)			t_{UVSH}	t_{US}	12	—	—	μs	
	36	SEEK Low to US0, US1 Invalid (Hold)			t_{SLUI}	t_{SU}	15	—	—	μs	
	37	SEEK High to DIR Valid (Setup)			t_{SHDV}	t_{SD}	7	—	—	μs	
	38	DIR Invalid to SEEK Low (Hold)			t_{DXSL}	t_{DS}	30	—	—	μs	CLK = 8 MHz
	39	DIR Valid to STP High (Setup)			t_{DVTH}	t_{DST}	1	—	—	μs	
	40	STP Low to DIR Invalid (Hold)			t_{TLDX}	t_{STD}	24	—	—	μs	
	41	STP Low to US0, US1 Invalid (Hold)			t_{TLUX}	t_{STU}	5	—	—	μs	
	42	STP High Width			t_{THTL}	t_{STP}	6	7	8	μs	
	43	STP Cycle Time			t_{TCY}	t_{SC}	33[3]	—	note 1	μs	
12	44	FR High Width			t_{FHFL}	t_{FR}	8	—	10	μs	
13	45	IDX High Width			t_{IHIL}	t_{IDX}	10	—	—	t_{CY}	
14	46	$\overline{DONE}$ Low Width			t_{THTL}	t_{TC}	1	—	—	t_{CY}	
15	47	$\overline{RESET}$ Low Width			t_{RHRL}	t_{RST}	14	—	—	t_{CY}	

Notes:

1. t_{SC} = 33 μs min. is for different drive units. In the case of the same unit, t_{SC} can be ranged from 1 ms to 16 ms with 8 MHz clock period, and 2 ms to 32 ms with 4 MHz clock, under software control.

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to +7.0	V
Input Voltage	V_{IN}	−0.3 to +7.0	V
Output Voltage	V_{OUT}	−0.3 to +7.0	V
Operating Temperature Range	T_A	0 to +70	C°
Storage Temperature Range	T_{STG}	−55 to +150	C°

***NOTE:** Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in other sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING CONDITIONS

Parameter	Range
V_{CC} Power Supply	5.0V ±5%
Operating Temperature	0°C to 70°C

DC CHARACTERISTICS

(V_{CC} = 5.0 Vdc ±5%, V_{SS} = 0 Vdc, T_A = 0°C to 70°C, unless otherwise noted)

Parameter	Symbol	Min	Max	Unit	Test Conditions
Input Low Voltage Logic CLK and WCK	V_{IL}	 −0.5 −0.5	 0.8 0.65	V	
Input High Voltage Logic CLK and WCK	V_{IH}	 2.0 2.4	 V_{CC} + 0.5 V_{CC} + 0.5	V	
Output Low Voltage	V_{OL}		0.45	V	V_{CC} = 4.75V, I_{OL} = 2.0 mA
Output High Voltage	V_{OH}	2.4	V_{CC}	V	V_{CC} = 4.75V, I_{OH} = −200 μA
V_{CC} Supply Current	I_{CC}		150	mA	V_{CC} = 4.75V
Input Load Current All Inputs	I_{IL}		10 −10	μA μA	V_{IN} = V_{CC} V_{IN} = 0V
High Level Output Leakage Current	I_{LOH}		10	μA	V_{CC} = 0V to 5.25V, V_{SS} = 0V V_{OUT} = V_{CC}
Low Level Output Leakage Current	I_{LOL}		−10	μA	V_{CC} = 0V to 5.25V, V_{SS} = 0V V_{OUT} = +0.45V
Internal Power Dissipation	P_{INT}	—	1.0	W	T_A = 25°C

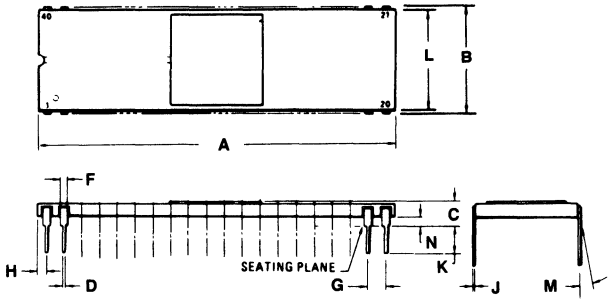
CAPACITANCE

(T_A = 25°C; f_c = 1 MHz; V_{CC} = 0V)

Parameter	Symbol	Max Limit	Unit
Clock Input	$C_{IN(C)}$	20	pF
Input	C_{IN}	10	pF
Output	C_{OUT}	20	pF
Note: All pins except pin under test tied to ground.			

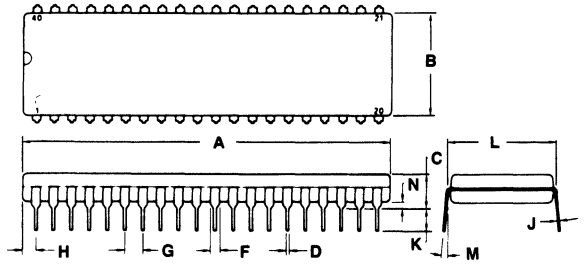
PACKAGE DIMENSIONS

40-PIN CERAMIC DIP



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	50.29	51.31	1.980	2.020
B	14.86	15.62	0.585	0.615
C	2.54	4.19	0.100	0.165
D	0.38	−0.53	0.015	0.021
F	0.76	1.40	0.030	0.055
G	2.54 BSC		0.100 BSC	
H	0.76	1.78	0.030	0.070
J	0.20	0.33	0.008	0.013
K	2.54	4.19	0.100	0.165
L	14.60	15.37	0.575	0.605
M	0°	10°	0°	10°
N	0.51	1.52	0.020	0.060

40-PIN PLASTIC DIP



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	51.28	52.32	2.040	2.060
B	13.72	14.22	0.540	0.560
C	3.55	5.08	0.140	0.200
D	0.36	0.51	0.014	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.30	0.008	0.012
K	3.05	3.56	0.120	0.140
L	15.24 BSC		0.600 BSC	
M	7°	10°	7°	10°
N	0.51	1.02	0.020	0.040

Rockwell

R68560, R68561 MULTI-PROTOCOL COMMUNICATIONS CONTROLLER (MPCC)

PRELIMINARY

DESCRIPTION

The R68560, R68561 Multi-Protocol Communications Controller (MPCC) interfaces a single serial communications channel to a 68008/68000 microcomputer-based system using either asynchronous or synchronous protocol. High speed bit rate, automatic formatting, low overhead programming, eight character buffering, two channel DMA interface and three separate interrupt vector numbers optimize MPCC performance to take full advantage of the 68008/68000 processing capabilities and asynchronous bus structure.

In synchronous operation, the MPCC supports bit-oriented protocols (BOP), such as SDLC/HDLC, and character-oriented protocols (COP), such as IBM Bisync (BSC) in either ASCII or EBCDIC coding. Formatting, synchronizing, validation and error detection is performed automatically in accordance with protocol requirements and selected options. Asynchronous (ASYNC) and isochronous (ISOC) modes are also supported. In addition, modem interface handshake signals are available for general use.

Control, status and data are transferred between the MPCC and the microcomputer bus via 22 directly addressable registers and a DMA interface. Two first-in first-out (FIFO) registers, addressable through separate receiver and transmitter data registers, each buffer up to eight characters at a time to allow more MPU processing time to service data received or to be transmitted and to maximize bus throughput, especially during DMA operation. The two-channel Direct Memory Access (DMA) interface operates with the MC68440/MC68450 DMA Controllers. Three prioritized interrupt vector numbers separately support receiver, transmitter and modem interface operation.

An on-chip oscillator drives the internal baud rate generator (BRG) and an external clock output with an 8 MHz input crystal or clock frequency. The BRG, in conjunction with two selectable prescalers and 16-bit programmable divisor, provides a data bit rate of DC to 4 MHz.

The 48-pin R68561 supports word-length (16-bit) operation when connected to the 68000 16-bit asynchronous bus, as well as byte-length (8-bit) operation when connected to the 68008 8-bit bus. The 40-pin R68560 supports byte-length operation on the 68008 bus.

FEATURES

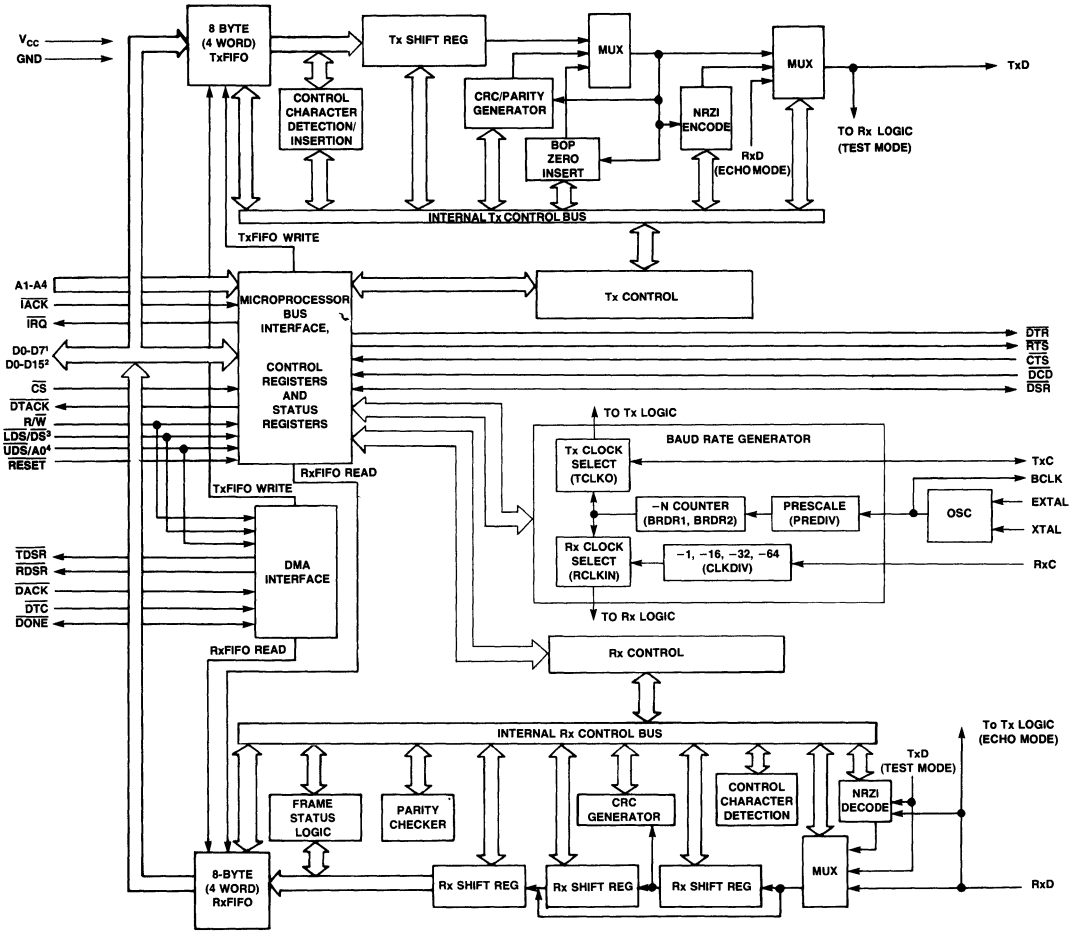
- Full duplex synchronous/asynchronous receiver and transmitter
- Fully implements IBM Binary Synchronous Communications (BSC) in two coding formats: ASCII and EBCDIC
- Supports other synchronous character-oriented protocols (COP), such as six-bit BSC, X3.28, ISO IS1745, ECMA-16, etc.
- Supports synchronous bit-oriented protocols (BOP), such as SDLC, HDLC, X.25, etc.
- Asynchronous and isochronous modes
- Modem handshake interface
- High speed serial data rate (DC to 4 MHz)
- Internal oscillator and Baud Rate Generator (BRG) with programmable data rate
- Crystal or TTL level clock input and buffered clock output (8 MHz)
- Direct interface to 68008/68000 asynchronous bus
- Eight-character receiver and transmitter buffer registers
- 22 directly addressable registers for flexible option selection, complete status reporting, and data transfer
- Three separate programmable interrupt vector numbers for receiver, transmitter and serial interface
- Maskable interrupt conditions for receiver, transmitter and serial interface
- Programmable microprocessor bus data transfer: polled, interrupt and two-channel DMA transfer compatible with MC68440/MC68450
- Clock control register for receiver clock divisor and receiver and transmitter clock routing
- Selectable full/half duplex, autoecho and local loop-back modes
- Selectable parity (enable, odd, even) and CRC (control field enable, CRC-16, CCITT V.41, VRC/LRC)

ORDERING INFORMATION

Part Number	Frequency	Temperature Range
R6856 _ _	4 MHz	0°C to 70°C

Package: C = Ceramic
P = Plastic

Number of pins: 0 = 40
1 = 48



NOTES:
1. R68560 ONLY.
2. R68561 ONLY.
3. $\overline{\text{UDS}}$ ON R68561 A0 ON R68560
4. $\overline{\text{LDS}}$ ON R68561 $\overline{\text{DS}}$ ON R68560

Figure 1. MPCC Block Diagram

PIN DESCRIPTION

Throughout the document, signals are presented using the terms active and inactive or asserted and negated independent of whether the signal is active in the high-voltage state or low-voltage state. (The active state of each logic pin is described below.) Active low signals are denoted by a superscript bar. R/$\overline{W}$ indicates a write is active low and a read active high.

Note: The R68561 interface is described for word mode operation only and the R68560 interface is described for byte mode operation only.

A1 – A4—Address Lines. A1 – A4 are active high inputs used in conjunction with the $\overline{CS}$ input to access the internal registers. The address map for these registers is shown in Table 1.

D0 – D15—Data Lines. The bidirectional data lines transfer data between the MPCC and the MPU, memory or other peripheral device. D0 – D15 are used when connected to the 16-bit 68000 bus and operating in the MPCC word mode. D0 – D7 are used when connected to the 16-bit 68000 bus or the 8-bit 68008 bus and operating in the MPCC byte mode. The data bus is three-stated when $\overline{CS}$ is inactive. (See exceptions in DMA mode.)

$\overline{CS}$—Chip Select. $\overline{CS}$ low selects the MPCC for programmed transfers with the host. The MPCC is deselected when the $\overline{CS}$ input is inactive in non-DMA mode. $\overline{CS}$ must be decoded from the address bus and gated with address strobe ($\overline{AS}$).

R/$\overline{W}$—Read/Write. R/$\overline{W}$ controls the direction of data flow through the bidirectional data bus by indicating that the current bus cycle is a read (high) or write (low) cycle.

$\overline{DTACK}$—Data Transfer Acknowledge. $\overline{DTACK}$ is an active low output that signals the completion of the bus cycle. During read or interrupt acknowledge cycles, $\overline{DTACK}$ is asserted by the MPCC after data has been provided on the data bus; during write cycles it is asserted after data has been accepted at the data bus. $\overline{DTACK}$ is driven high after assertion prior to being tri-stated. A holding resistor is required to maintain $\overline{DTACK}$ high between bus cycles.

$\overline{DS}$—Data Strobe (R68560). During a write (R/$\overline{W}$ low), the $\overline{DS}$ positive transition latches data on data bus lines D0 – D7 into the MPCC. During a read (R/$\overline{W}$ high), $\overline{DS}$ low enables data from the MPCC to data bus lines D0 – D7.

$\overline{LDS}$—Lower Data Strobe (R68561). During a write (R/$\overline{W}$ low), the positive transition latches data on the data bus lines D0 – D7 (and on D8 – D15 if $\overline{UDS}$ is low) into the MPCC. During a read (R/$\overline{W}$ high), $\overline{LDS}$ low enables data from the MPCC to D0 – D7 (and to D8 – D15 if $\overline{UDS}$ is low).

A0—Address Line A0 (R68560). When interfacing to an 8-bit data bus system such as the 68008, address line A0 is used to access an internal register. A0 = 0 defines an even register and A0 = 1 defines an odd register. See Table 1b.

$\overline{UDS}$—Upper Data Strobe (R68561). When interfacing to a 16-bit data bus system such as the 68000, a low on control bus signal $\overline{UDS}$ enables access to the upper data byte on D8 – D15. A high on $\overline{UDS}$ disables access to D8 – D15. Data is latched and enabled in conjunction with $\overline{LDS}$.

$\overline{IRQ}$—Interrupt Request. The active low $\overline{IRQ}$ output requests interrupt service by the MPU. $\overline{IRQ}$ is driven high after assertion prior to being tri-stated.

$\overline{IACK}$—Interrupt Acknowledge. The active low $\overline{IACK}$ input indicates that the current bus cycle is an interrupt acknowledge cycle. When $\overline{IACK}$ is asserted the MPCC places an interrupt vector on the lower byte (D0 – D7) of the data bus.

$\overline{TDSR}$—Transmitter Data Service Request. When Transmitter DMA mode is active, the low $\overline{TDSR}$ output requests DMA service.

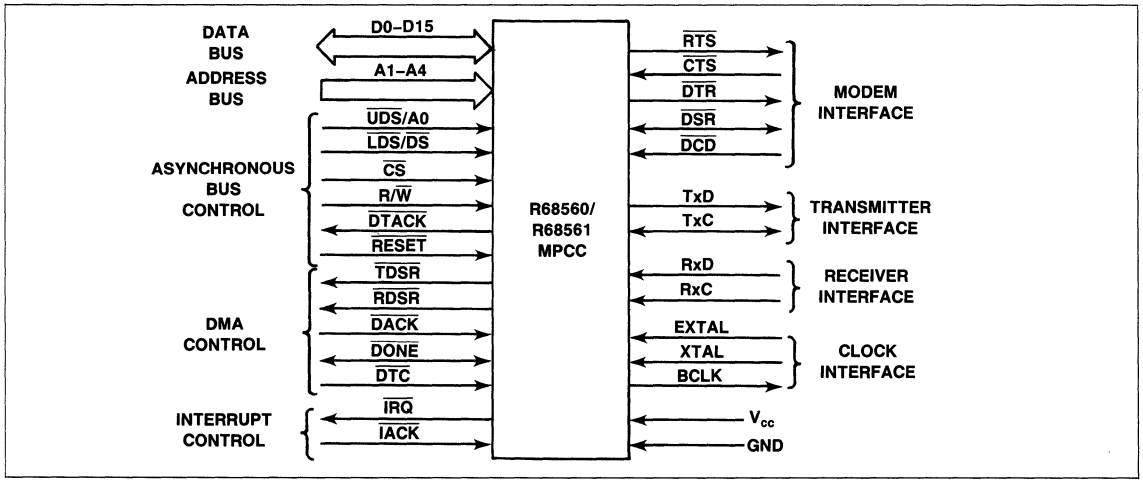


Figure 2. MPCC Input and Output Signals

$\overline{RDSR}$—Receiver Data Service Request. When receiver DMA mode is active, the low $\overline{RDSR}$ output requests DMA service.

$\overline{DACK}$—DMA Acknowledge. The $\overline{DACK}$ low input indicates that the data bus has been acquired by the DMAC and that the requested bus cycle is beginning.

$\overline{DTC}$—Data Transfer Complete. The $\overline{DTC}$ low input indicates that a DMA data transfer is complete. $\overline{DTC}$ in response to a $\overline{RDSR}$ indicates that the data has been successfully stored in memory. $\overline{DTC}$ in response to a $\overline{TDSR}$ indicates that the data is present on the data bus for strobing into the MPCC. $\overline{DTC}$ is used in conjunction with R/$\overline{W}$ to increment the TxFIFO or RxFIFO pointer.

$\overline{DONE}$—Done. $\overline{DONE}$ is a bidirectional active low signal. The $\overline{DONE}$ signal is asserted by the DMAC when the DMA transfer count is exhausted and there is no more data to be transferred, or asserted by the MPCC when the status byte following the last character of a frame (block) is being transferred in response to a $\overline{RDSR}$. The $\overline{DONE}$ signal asserted by the DMAC in response to a $\overline{TDSR}$ will be stored to track with the data byte (lower byte for word transfer) through the TxFIFO.

$\overline{RESET}$—Reset. $\overline{RESET}$ is an active low, high impedance input that initializes all MPCC functions. $\overline{RESET}$ must be asserted for at least 500 ns to initialize the MPCC.

$\overline{DTR}$—Data Terminal Ready. The $\overline{DTR}$ active low output is general purpose in nature, and is controlled by the DTRLVL bit in the Serial Interface Control Register (SICR).

$\overline{RTS}$—Request to Send. The $\overline{RTS}$ active low output is general purpose in nature, and is controlled by the RTSLVL bit in the SICR.

$\overline{CTS}$—Clear to Send. The $\overline{CTS}$ active low input positive transition and level are reported in the CTST and CTSLVL bits in the Serial Interface Status Register (SISR), respectively.

$\overline{DSR}$—Data Set Ready. The $\overline{DSR}$ active low input negative transition and level are reported in the DSRT and DSRLVL bits in the SISR, respectively. $\overline{DSR}$ is also an output for RSYN.

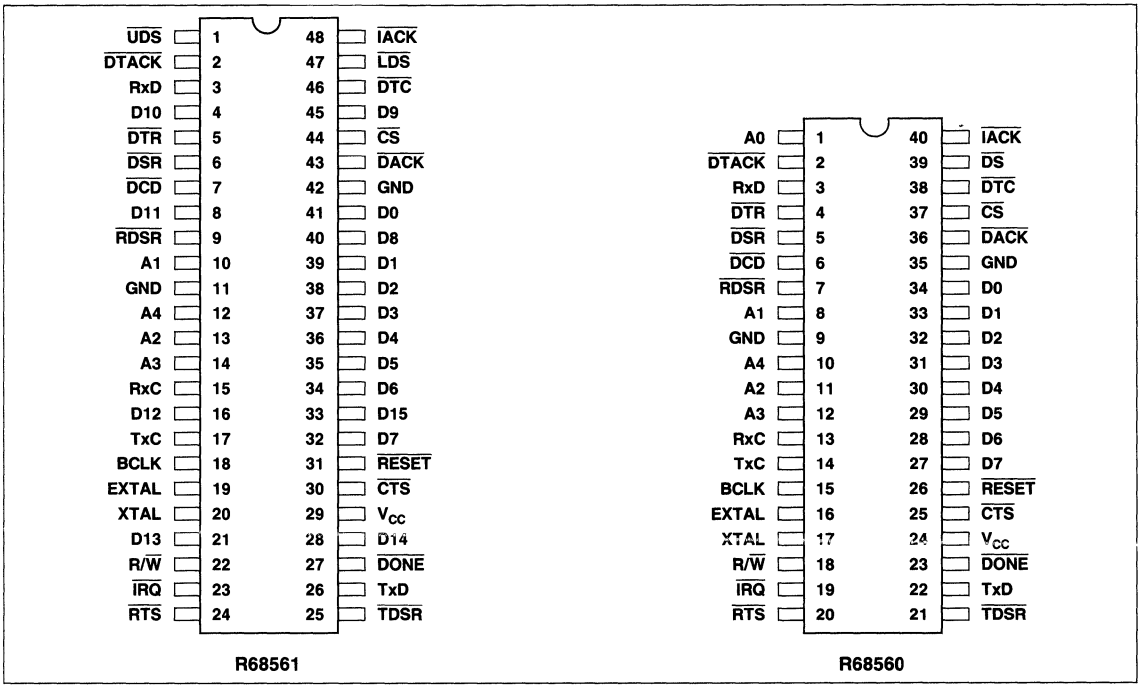
$\overline{DCD}$—Data Carrier Detect. The $\overline{DCD}$ active low input positive transition and level are reported in the DCDT and DCDLVL bits in the the SISR, respectively.

TxD—Transmitted Data. The MPCC transmits serial data on the TxD output. The TxD output changes on the negative going edge of TxC.

RxD—Received Data. The MPCC receives serial data on the RxD input. The RxD input is shifted into the receiver with the negative going edge of RxC.

TxC—Transmitter Clock. TxC can be programmed to be an input or an output. When TxC is selected to be an input, the transmitter clock must be provided externally. When TxC is programmed to be an output, a clock is generated by the MPCC's internal baud rate generator. The low-to-high transition of the clock signal nominally indicates the center of a serial data present on the TxD output.

RxC—Receiver Clock. RxC provides the MPCC receiver with received data timing information.



Pin Configuration

EXTAL—Crystal/External Clock Input.
XTAL Crystal Return. EXTAL and XTAL connect an 8 MHz external crystal to the MPCC internal oscillator. The pin EXTAL may also be used as a TTL level input to supply a DC to 8 MHz reference timing from an external clock source. XTAL must be tied to ground when applying an external clock to the EXTAL input.

BCLK—Buffered Clock. BCLK is the internal oscillator buffered output available to other MPCC devices eliminating the need for additional crystals.

Vcc—Power. 5V ±5%.

GND—Ground. Ground (V_{SS}).

MPCC REGISTERS

Twenty-two registers control and monitor the MPCC operation. The registers and their addresses are identified in Table 1a (R68561 operation in word mode) and in Table 1b (R68560 operation in byte mode). When the R68561 is operated in the word mode, two registers are read or written at a time starting at an even boundary. When the R68560 is operated in the byte mode, each register is explicitly addressed based on A0.

Table 2 summarizes the MPCC register bit assignments and their access. A read from an unassigned location results in a read from a "null register." A null register returns all ones for data and results in a normal bus cycle. Unused bits of a defined register are read as zeros unless otherwise noted.

Table 1a. R68561 Accessible Registers (Word Mode)

Register(s)		R/W	Addr (Hex.)	Address Lines A4 A3 A2 A1
15 8	7 0			
Receiver Control Register (RCR)	Receiver Status Register (RSR)	R/W	00	0 0 0 0
Receiver Data Register (RDR)—16 bits[1]		R	02	0 0 0 1
Receiver Interrupt Enable Register (RIER)	Receiver Interrupt Vector Number Register (RIVNR)	R/W	04	0 0 1 0
Transmitter Control Register (TCR)	Transmitter Status Register (TSR)	R/W	08	0 1 0 0
Transmitter Data Register (TDR)—16 bits[2]		W	0A	0 1 0 1
Transmitter Interrupt Enable Register (TIER)	Transmitter Interrupt Vector Number Register (TIVNR)	R/W	0C	0 1 1 0
Serial Interface Control Register (SICR)	Serial Interface Status Register (SISR)	R/W	10	1 0 0 0
Reserved[3]	Reserved[3]	R/W	12	1 0 0 1
Serial Interrupt Enable Register (SIER)	Serial Interrupt Vector Number Register (SIVNR)	R/W	14	1 0 1 0
Protocol Select Register 2 (PSR2)	Protocol Select Register (PSR1)	R/W	18	1 1 0 0
Address Register 2 (AR2)	Address Register 1 (AR1)	R/W	1A	1 1 0 1
Band Rate Divider Register 2 (BRDR2)	Baud Rate Divider Register 1 (BRDR1)	R/W	1C	1 1 1 0
Error Control Register (ECR)	Clock Control Register (CCR)	R/W	1E	1 1 1 1

Notes:
1. Accessible register of the four word RxFIFO. The data is not initialized, however, $\overline{RES}$ resets the RxFIFO pointer to the start of the first word.
2. Accessible register of the four word TxFIFO. The data is not initialized, however, $\overline{RES}$ resets the TxFIFO pointer to the start of the first word.
3. Reserved registers may contain random bit values.

Table 1b. R68560 Accessible Registers (Byte Mode)

Register(s)	R/W	Addr (Hex.)	Address Lines A4	A3	A2	A1	A0
7 0							
Receiver Status Register (RSR)	R/W	00	0	0	0	0	0
Receiver Control Register (RCR)	R/W	01	0	0	0	0	1
Receiver Data Register (RDR)—8 bits[1]	R	02	0	0	0	1	0
Reserved[3]		03	0	0	0	1	1
Receiver Interrupt Vector Number Register (RIVNR)	R/W	04	0	0	1	0	0
Receiver Interrupt Enable Register (RIER)	R/W	05	0	0	1	0	1
Transmitter Status Register (TSR)	R/W	08	0	1	0	0	0
Transmitter Control Register (TCR)	R/W	09	0	1	0	0	1
Transmitter Data Register (TDR)[2]—8 bits	W	0A	0	1	0	1	0
Reserved[3]		0B	0	1	0	1	1
Transmitter Interrupt Vector Number Register (TIVNR)	R/W	0C	0	1	1	0	0
Transmitter Interrupt Enable Register (TIER)	R/W	0D	0	1	1	0	1
Serial Interface Status Register (SISR)	R/W	10	1	0	0	0	0
Serial Interface Control Register (SICR)	R/W	11	1	0	0	0	1
Reserved[3]		12	1	0	0	1	0
Reserved[3]		13	1	0	0	1	1
Serial Interrupt Vector Number Register (SIVNR)	R/W	14	1	0	1	0	0
Serial Interrupt Enable Register (SIER)	R/W	15	1	0	1	0	1
Protocol Select Register 1 (PSR1)	R/W	18	1	1	0	0	0
Protocol Select Register 2 (PSR2)	R/W	19	1	1	0	0	1
Address Register 1 (AR1)	R/W	1A	1	1	0	1	0
Address Register 2 (AR2)	R/W	1B	1	1	0	1	1
Baud Rate Divider Register 1 (BRDR1)	R/W	1C	1	1	1	0	0
Baud Rate Divider Register 2 (BRDR2)	R/W	1D	1	1	1	0	1
Clock Control Register (CCR)	R/W	1E	1	1	1	1	0
Error Control Register (ECR)	R/W	1F	1	1	1	1	1

Notes:
1. Accessible register of the eight byte RxFIFO. The data is not initialized, however, $\overline{RES}$ resets the RxFIFO pointer to the start of the first byte.
2. Accessible register of the eight byte TxFIFO. The data is not initialized, however, $\overline{RES}$ resets the TxFIFO pointer to the start of the first byte.
3. Reserved registers may contain random bit values.

Table 2. MPCC Register Bit Assignments

R/W Access	Bit Number 7	6	5	4	3	2	1	0	Reset[1] Value	
R/W	RDA	EOF	0	C/PERR	FRERR	ROVRN	RA/B	RIDLE	00	Receiver Status Register (RSR)
R/W	0	RDSREN	DONEEN	RSYNEN	STRSYN	0	RABTEN	RRES	01	Receiver Control Register (RCR)
R	RECEIVED DATA (RxFIFO)[2]								— —	Receiver Data Register (RDR)
R/W	RECEIVER INTERRUPT VECTOR NUMBER (RIVN)								0F	Receiver Interrupt Vector Number Register (RIVNR)
R/W	RDA IE	EOF IE	0	C/PERR IE	FRERR IE	ROVRN IE	RA/B IE	0	00	Receiver Interrupt Enable Register (RIER)
R/W	TDRA	TFC	0	0	0	TUNRN	TFERR	0	80	Transmitter Status Register (TSR)
R/W	TEN	TDSREN	TICS	THW	TLAST	TSYN	TABT	TRES	01	Transmitter Control Register (TCR)
W	TRANSMITTED DATA (TxFIFO)[2]								— —	Transmitter Data Register (TDR)
R/W	TRANSMITTER INTERRUPT VECTOR NUMBER (TIVN)								0F	Transmitter Interrupt Vector Number Register (TIVNR)
R/W	TDRA IE	TFC IE	0	0	0	TUNRN IE	TFERR IE	0	00	Transmitter Interrupt Enable Register (TIER)
R/W	CTST	DSRT	DCDT	CTSLVL	DSRLVL	DCDLVL	0	0	00	Serial Interface Status Register (SISR)
R/W	RTSLVL	DTRLVL	0	0	0	ECHO	TEST	0	00	Serial Interface Control Register (SICR)
	RANDOM BIT VALUES									(reserved)
	RANDOM BIT VALUES									(reserved)
R/W	SERIAL INTERRUPT VECTOR NUMBER (SIVN)								0F	Serial Interrupt Vector Number Register (SIVNR)
R/W	CTS IE	DSR IE	DCD IE	0	0	0	0	0	00	Serial Interrupt Enable Register (SIER)
R/W	0	0	0	0	0	0	CTLEX	ADDEX	00	Protocol Select Register 1 (PSR1)
R/W	WD/BYT	STOP BIT SEL SB2	SB1	CHAR LEN SEL CL2	CL1	PROTOCOL SEL PS3	PS2	PS1	00	Protocol Select Register 2 (PSR2)
R/W	BOP ADDRESS/BSC & COP PAD								00	Address Register 1 (AR1)
R/W	BOP ADDRESS/BSC & COP SYN								00	Address Register 2 (AR2)
R/W	BAUD RATE DIVIDER (LSH)								01	Baud Rate Divider Register 1 (BRDR1)
R/W	BAUD RATE DIVIDER (MSH)								00	Baud Rate Divider Register 2 (BRDR2)
R/W	0	0	0	PSCDIV	TCLKO	RCLKIN	CLK SEL CK2	CK1	00	Clock Control Register (CCR)
R/W	PAREN	ODDPAR	0	0	CFCRC	CRCPRE	CRC SEL CR2	CR1	04	Error Control Register (ECR)

Notes:
1. RESET = Register contents upon power up or $\overline{\text{RESET}}$.
2. 16-bits for R68561 (word mode); 8-bits for R68560 (byte mode).

REGISTER DEFINITIONS

RECEIVER REGISTERS

Receiver Status Register (RSR)

7	6	5	4	3	2	1	0
RDA	EOF	0	C/PERR	FRERR	ROVRN	RA/B	RIDLE

Reset Value = $00

The Receiver Status Register (RSR) contains the status of the receiver including error conditions. Status bits are cleared by writing a 1 into respective positions, by writing a 1 into the RCR RRES bit or by $\overline{\text{RESET}}$. If an EOF, C/PERR, or FRERR is set in the RSR, the data reflecting the error (the first byte or word in the RxFIFO) must be read prior to resetting the corresponding status bit in the RSR. The $\overline{\text{IRQ}}$ output is asserted if any of the conditions reported by the status bits occur and the corresponding interrupt enable bit in the RIER is set.

The RSR format is the same as the frame status format (see below) except as noted.

RSR
7 RDA —Receiver Data Available. (RSR only).
0 The RxFIFO is empty (i.e., no received data is available).
1 Received data is available in the RxFIFO and can be read via the RDR.

RSR
6 EOF —End of Frame.
0 No end of frame or block detected.
1 End of frame or block detected (BOP and BSC).

RSR
5 RHW —Receive Half Word. (Frame Status only)*
0 The last word of the frame contains data on the upper half (D8 – D15) and frame status on the lower half (D0 – D7) of the data bus.
1 The lower half of the data bus (D0 – D7) contains the frame status but the upper half (D8 – D15) is blank or invalid.

RSR
4 C/PERR —CRC/Parity Error.
0 No CRC or parity error detected.
1 CRC error detected (BOP, BSC), Parity error detected (ASYNC, ISOC and COP).

RSR
3 FRERR —Frame Error.
0 No frame error detected.
1 Short Frame or a closing FLAG detected off boundary (BOP), Frame error (ASYNC, ISOC) or receiver overrun.

RSR
2 ROVRN —Receiver Overrun.
0 No receiver overrun detected.
1 Receiver overrun detected. Indicates that receiver data was attempted to be transferred into the RxFIFO when it was full, resulting in loss of received data. The data that is already in RxFIFO are not affected and may be read by the processor.

RSR
1 RA/B —Receiver Abort/Break.
0 Normal Operation.
1 ABORT detected after an opening flag (BOP), ENQ detected in a block of text data (BSC), or BREAK ended (ASYNC).

RSR
0 RIDLE —Receiver Idle. (RSR only).
0 Receiver not idle.
1 15 or more consecutive "1's" have been received and the receiver is in an inactive idle state.

*Frame Status (RSR)

7	6	5	4	3	2	1	0
0	EOF	RHW	C/PERR	FRERR	ROVRN	RA/B	0

For the BSC and BOP protocols which have defined message blocks or frames, a "frame status" byte will be loaded into the RxFIFO following the last data byte of each block. The frame status contains all the status contained within the RSR with the exception of RDA and RIDLE. But, in addition to the RSR contents, the frame status byte has a RHW status in bit 5 which indicates either an even or odd boundary (applicable to word mode only).

If the MPCC is in word mode and the last data byte was on an even byte boundary (i.e., there was an even number of bytes in the message), a blank byte will be loaded into the RxFIFO prior to loading the frame status byte in order to force the "frame status" byte and the next frame to be on an even boundary. When RHW = 0, the last word of the frame contains data on the upper half and status on the lower half of the data bus. If RHW = 1, the lower half of the bus contains status but the upper half is a blank or invalid byte.

In the byte mode, the status byte will always immediately follow the last data byte of the block/frame (see Figure 3). The EOF status in the RSR is then set when the byte/word containing the frame status is the next byte/word to be read from the RxFIFO.

In the receiver DMA mode, when the EOF status in the RSR is set, DONE is asserted to the DMAC. Thus the last byte accessed by the DMAC is always a status byte, which the processor may read to check the validity of entire frame.

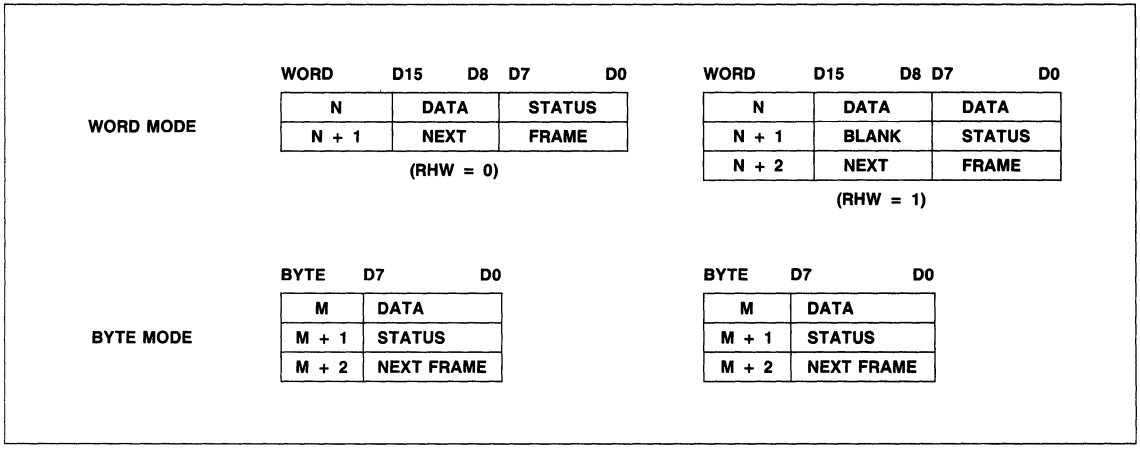


Figure 3. BSC/BOP Block/Frame Status Location

Receiver Control Register (RCR)

7	6	5	4	3	2	1	0
—	RDSREN	DONEEN	RSYNEN	STRSYN	0	RABEN	RRES

Reset value = $01

The Receiver Control Register (RCR) selects receiver control options.

RCR
7 —Not used.

RCR
6 **RDSREN —Receiver Data Service Request Enable.**
0 Disable receiver DMA mode.
1 Enable receiver DMA mode.

RCR
5 **DONEEN —$\overline{\text{DONE}}$ Output Enable.**
0 Disable $\overline{\text{DONE}}$ output.
1 Enable $\overline{\text{DONE}}$ output. (When the receiver is in the DMA mode, i.e., RDSREN = 1).

RCR
4 **RSYNEN —RSYNEN Output Enable.** Selects the DSR signal input or the RSYN SYNC signal output on the $\overline{\text{DSR}}$ pin.
0 Input DSR on $\overline{\text{DSR}}$.
1 Output RSYN on $\overline{\text{DSR}}$.

RCR
3 **STRSYN —Strip SYN Character (COP only).**
0 Do not strip SYN character.
1 Strip SYN character.

RCR
2 **MUST BE ZERO**
0

RCR
1 **RABTEN —Receiver Abort Enable (BOP only).**
0 Do not abort frame upon error detection.
1 Abort frame upon RxFIFO overrun (ROVRN bit = 1 in the RSR) or CFCRC error detection (C/PERR bit = 1 in the RSR). If either error occurs, the MPCC ignores the remainder of the current frame and searches for the beginning of the next frame.

RCR
0 **RRES —Receiver Reset Command.**
0 Enable normal receiver operation.
1 Reset receiver. Resets the receiver section including the RxFIFO and the RSR (but not the RCR). RRES is set by $\overline{\text{RESET}}$ or by writing a 1 into this bit for one write cycle and is cleared by writing a 0 into this bit. RRES requires clearing after $\overline{\text{RESET}}$.

Receiver Data Register (RDR)

R68561 (Word Mode)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSB			Byte 1			LSB		MSB			Byte 0			LSB	

R68560 (Byte Mode)

7	6	5	4	3	2	1	0
MSB			Byte 0			LSB	

The receiver has an 8-byte (or 4-word) First In First Out (FIFO) register file (RxFIFO) where received data are stored before being transferred to the bus. The received data is transferred out of the RxFIFO via the RDR in 8-bit bytes or 16-bit words depending on the WD/BYT bit setting in PSR2. When the RxFIFO has a data byte/word ready to be transferred, the RDA status bit in the RSR is set to 1.

Receiver Interrupt Vector Number Register (RIVNR)

7	6	5	4	3	2	1	0
Receiver Interrupt Vector Number (RIVN)							

Reset value = $0F

If a receiver interrupt condition occurs (as reported by status bits in the RSR that correspond to interrupt enable bits in the RIER) and the corresponding bit is set in the RIER, $\overline{IRQ}$ output is asserted to request MPU receiver interrupt service. When the $\overline{IACK}$ input is asserted from the bus, the Receiver Interrupt Vector Number (RIVN) from the Receiver Interrupt Vector Number Register (RIVNR) is placed on the data bus.

Receiver Interrupt Enable Register (RIER)

7	6	5	4	3	2	1	0
RDA IE	EOF IE	0	C/PERR IE	FRERR IE	ROVRN IE	RA/B IE	0

Reset value = $00

The Receiver Interrupt Enable Register (RIER) contains interrupt enable bits for the Receiver Status Register (RSR). When enabled, the $\overline{IRQ}$ output is asserted when the corresponding condition is detected and reported in the RSR.

RIER
7 RDA IE —Receiver Data Available Interrupt Enable.
0 Disable RDA Interrupt.
1 Enable RDA Interrupt.

RIER
6 EOF IE —End of Frame Interrupt Enable.
0 Disable EOF Interrupt.
1 Enable EOF Interrupt.

RIER
5 —Not used.

RIER
4 C/PERR IE —CRC/Parity Error Interrupt Enable.
0 Disable C/PERR Interrupt.
1 Enable C/PERR Interrupt.

RIER
3 FRERR IE —Frame Error Interrupt Enable.
0 Disable FRERR Interrupt.
1 Enable FRERR Interrupt.

RIER
2 ROVRN IE —Receiver Overrun Interrupt Enable.
0 Disable ROVRN Interrupt.
1 Enable ROVRN Interrupt.

RIER
1 RA/B IE —Receiver Abort/Break Interrupt Enable.
0 Disable RA/B Interrupt.
1 Enable RA/B Interrupt.

RIER
0 —Not used.

TRANSMITTER REGISTERS

Transmitter Status Register (TSR)

7	6	5	4	3	2	1	0
TDRA	TFC	0	0	0	TUNRN	TFERR	0

Reset value = $80

The Transmitter Status Register (TSR) contains the transmitter status including error conditions. The transmitter status bits are cleared by writing a 1 into their respective positions, by writing a 1 into the TCR TRES bit, or by $\overline{RESET}$. The $\overline{IRQ}$ output is asserted if any of the conditions reported by the status bits occur and the corresponding interrupt enable bit in the TIER is set.

TSR
7 TDRA —Transmitter Data Register Available.
0 The TxFIFO is full.
1 The TxFIFO is not full (i.e., available) and data to transmit can be loaded via the TDR.

TSR
6 TFC —Transmitted Frame Complete. (BOP, BSC and COP only).
0 Frame not complete.
1 Closing FLAG or ABORT character has been transmitted (BOP), Trailing PAD has been transmitted (BSC), or the last character of a frame or block as defined by TLAST (TCR bit 3) has been transmitted (COP).

TSR
5-3 —Not used.

TSR
2 TUNRN —Transmitter Underrun (BOP, BSC and COP only). A transmitter underrun occurs when the transmitter runs out of data during a transmission. For BOP, the underrun condition is treated as an abort. For BSC and COP, SYN characters are transmitted until more data is available in the TxFIFO.
0 No transmitter underrun occurred.
1 Transmitter underrun occurred.

TSR
1 TFERR —Transmit Frame Error (BOP only).
0 No frame error has occurred.
1 No control field was present (short frame).

Transmitter Control Register (TCR)

7	6	5	4	3	2	1	0
TEN	TDSREN	TICS	THW	TLAST	TSYN	TABT	TRES

Reset value = $01

The Transmitter Control Register (TCR) selects transmitter control function.

TCR
7 TEN —Transmitter Enable.
0 Disable transmitter. TxD output is idled. The TxFIFO may be loaded while the transmitter is disabled.
1 Enable transmitter.

TCR

6 **TDSREN —Transmitter Data Service Request Enable.**

0 Disable transmitter DMA mode.

1 Enable transmitter DMA mode.

TCR

5 **TICS —Transmitter Idle Character Select.** Selects the idle character to be transmitted when the transmitter is in an active idle mode (transmitter enabled or disabled).

0 Mark Idle (TxD output is held high).

1 Content of AR2 (BSC and COP), BREAK condition (ASYNC and ISOC), or FLAG character (BOP).

TCR

4 **THW —Transmit Half Word.** (R68561, word mode only). This bit is used when the frame or block ends on an odd boundary in conjunction with the TLAST bit and indicates that the last word in the TxFIFO contains valid data in the upper byte only. This bit must always be 0 in byte mode (R68560).

0 Transmit full word (16 bits) from the TxFIFO.

1 Transmit upper byte (8 bits) from the TxFIFO.

TCR

3 **TLAST —Transmit Last Character** (BOP, BSC and COP only).

0 The next character is not the last character in a frame or block.

1 The next character to be written into the TDR is the last character of the message. The TLAST bit automatically returns to a 0 when the associated word/byte is written to the TxFIFO. If the transmitter DMA mode is enabled, TLAST is set to a 1 by $\overline{DONE}$ from the DMAC. In this case the character written into the TDR in the current cycle is the last character.

TCR

2 **TSYN —Transmit SYN** (BSC and COP only).

0 Do not transmit SYN characters.

1 Transmit SYN characters. Causes a pair of SYN characters to be transmitted immediately following the current character. If BSC transparent mode is active, a DLE SYN sequence is transmitted. The TSYN bit automatically returns to a 0 when the SYN character is loaded into the Transmitter Shift Register.

TCR

1 **TABT —Transmit ABORT** (BOP only).

0 Enable normal transmitter operation.

1 Causes an abort by sending eight consecutive 1's. A data word/byte must be loaded into the TxFIFO after setting this bit in order to complete the command. The TABT bit clears automatically when the subsequent data word/byte is loaded into the TxFIFO.

TCR

0 **TRES —Transmitter Reset Command.**

0 Enable normal transmitter operation.

1 Reset transmitter. Clears the transmitter section including the TxFIFO and the TSR (but not the TCR). The TxD output is held in "Mark" condition. TRES is set by $\overline{RESET}$ or by writing a 1 into this bit for one write cycle and is cleared by writing a 0 into this bit. TRES requires clearing after $\overline{RESET}$.

Transmit Data Register (TDR)

R68561 (Word Mode)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSB			Byte 1			LSB		MSB			Byte 0			LSB	

R68560 (Byte Mode)

7	6	5	4	3	2	1	0
MSB			Byte 0			LSB	

The transmitter has an 8-byte (or 4-word) FIFO register file (TxFIFO). Data to be transmitted is transferred from the bus into the TxFIFO via the TDR in 8-bit bytes or 16-bit words depending on the WD/BYT bit setting in PSR2. The TDRA status bit in the TSR is set to 1 when the TxFIFO is ready to accept another data word/byte.

Transmitter Interrupt Vector Number Register (TIVNR)

7	6	5	4	3	2	1	0
Transmitter Interrupt Vector Number (TIVN)							

Reset value = $0F

If a transmitter interrupt condition occurs (as reported by status bits in the TSR that correspond to interrupt enable bits in the TIER) and the corresponding bit in the TIER is set, the $\overline{IRQ}$ output is asserted to request MPU transmitter interrupt service. When the $\overline{IACK}$ input is asserted from the bus, the Transmitter Interrupt Vector Number (TIVN) from the Transmitter Interrupt Vector Number Register (TIVNR) is placed on the data bus.

Transmitter Interrupt Enable Register (TIER)

7	6	5	4	3	2	1	0
TDRA IE	TFC IE	0	0	0	TUNRN IE	TFERR IE	—

Reset value = $00

The Transmitter Interrupt Enable Register (TIER) contains interrupt enable bits for the Transmitter Status Register. When enabled, the $\overline{IRQ}$ output is asserted when the corresponding condition is detected and reported in the TSR.

TIER

7 **TDRA IE —Transmitter Data Register (TDR) Available Interrupt Enable.**

0 Disable TDRA Interrupt.

1 Enable TDRA Interrupt.

TIER
6 TFC IE —Transmit Frame Complete (TFC) Interrupt Enable.
0 Disable TFC Interrupt.
1 Enable TFC Interrupt.

TIER
5-3 —Not used.

TIER
2 TUNRN IE —Transmitter Underrun (TUNRN) Interrupt Enable.
0 Disable TUNRN Interrupt.
1 Enable TUNRN Interrupt.

TIER
1 TFERR IE —Transmit Frame Error (TFERR) Interrupt Enable.
0 Disable TFERR Interrupt.
1 Enable TFERR Interrupt.

TIER
0 —Not used.

SERIAL INTERFACE REGISTERS

Serial Interface Status Register (SISR)

7	6	5	4	3	2	1	0
CTST	DSRT	DCDT	CTSLVL	DSRLVL	DCDLVL	0	0

Reset value = $00

The Serial Interface Status Register (SISR) contains the serial interface status information. The transition status bits (CTST, DSRT and DCDT) are cleared by writing a 1 into their respective positions, or by $\overline{\text{RESET}}$. The level status bits (CTSLVL, DSRLVL and DCDLVL) reflect the state of their respective inputs and cannot be cleared internally. The $\overline{\text{IRQ}}$ output is asserted if any of the conditions reported by the transition status bits occur and the corresponding interrupt enable bit in the SIER is set.

SISR
7 CTST —Clear to Send Transition Status.
1 $\overline{\text{CTS}}$ has transitioned positive (from active to inactive). (TRES must be zero).
0 $\overline{\text{CTS}}$ has not transitioned positive.

SISR
6 DSRT —Data Set Ready Transition Status.
1 $\overline{\text{DSR}}$ has transitioned negative (from inactive to active).
0 $\overline{\text{DSR}}$ has not transitioned negative.

SISR
5 DCDT —Data Carrier Detect Transition Status.
1 $\overline{\text{DCD}}$ has transitioned positive (from active to inactive).
0 $\overline{\text{DCD}}$ has not transitioned positive.

SISR
4 CTSLVL —Clear to Send Level.
0 $\overline{\text{CTS}}$ input level is negated (high).
1 $\overline{\text{CTS}}$ input level is asserted (low).

SISR
3 DSRLVL —Data Set Ready Level.
0 $\overline{\text{DSR}}$ input level is negated (high).
1 $\overline{\text{DSR}}$ input level is asserted (low).

SISR
2 DCDLVL —Data Carrier Detect Level.
0 $\overline{\text{DCD}}$ input level is negated (high).
1 $\overline{\text{DCD}}$ input level is asserted (low).

SISR
1-0 —Not used.

Serial Interface Control Register (SICR)

7	6	5	4	3	2	1	0
RTSLVL	DTRLVL	0	0	0	ECHO	TEST	0

Reset value = $00

The Serial Interface Control Register (SICR) controls various serial interface signals and test functions.

SICR
7 RTSLVL —Request to Send Level.
0 Negate $\overline{\text{RTS}}$ output (high).
1 Assert $\overline{\text{RTS}}$ output (low).

NOTE

In BOP, BSC, or COP, when the RTSLVL bit is cleared in the middle of data transmission, the $\overline{\text{RTS}}$ output remains asserted until the end of the current frame or block has been transmitted. In ASYNC or ISOC, the $\overline{\text{RTS}}$ output is negated when the TxFIFO is empty. If the transmitter is idling when the RTSLVL bit is reset, the $\overline{\text{RTS}}$ output is negated within two bit times.

SICR
6 DTRLVL —Data Terminal Ready Level.
0 Negate $\overline{\text{DTR}}$ output (high).
1 Assert $\overline{\text{DTR}}$ output (low).

SICR
5-3 —Not used. These bits are initialized to 0 by $\overline{\text{RESET}}$ and must not be set to 1.

SICR
2 ECHO —Echo Mode Enable.
0 Disable Echo mode (enable normal operation).
1 Enable Echo mode. Received data (RxD) is routed back through the transmitter to TxD. The contents of the TxFIFO is undisturbed. This mode may be used for remote test purposes.

SICR
1 TEST —Self-test Enable.
0 Disable self-test (enable normal operation).
1 Enable self-test. The transmitted data (TxD) and clock (TxC) are routed back through to the receiver through RxD and RxC, respectively ($\overline{\text{DCD}}$ and $\overline{\text{CTS}}$ are ignored). This "loopback" self-test may be used for all protocols. RxC is external regardless of the state of CCR bit 2. CCR bit 3 must be a 1.

SICR

0 MUST BE ZERO
0

Serial Interrupt Vector Number Register (SIVNR)

7	6	5	4	3	2	1	0
Serial Interrupt Vector Number (SIVN)							

Reset value = $0F

If a serial interface interrupt condition occurs (as reported by status bits in the SISR that correspond to interrupt enable bits in the SIER) and the corresponding bit in the SIER is set, the $\overline{IRQ}$ output is asserted to request MPU serial interface interrupt service. When the $\overline{IACK}$ input is asserted from the bus, the Serial Interrupt Vector Number (SIVN) from the Serial Interrupt Vector Number Register (SIVNR) is placed on the data bus.

Serial Interrupt Enable Register (SIER)

7	6	5	4	3	2	1	0
CTS IE	DSR IE	DCD IE	0	0	0	0	0

Reset value = $00

The Serial Interrupt Enable Register (SIER) contains interrupt enable bits for the Serial Interface Status Register. When an interrupt enable bit is set, the $\overline{IRQ}$ output is asserted when the corresponding condition occurs as reported in the SISR.

SIER

7 CTS IE —Clear to Send (CTS) Interrupt Enable.
0 Disable CTS Interrupt.
1 Enable CTS Interrupt.

SIER

6 DSR IE —Data Set Ready (DSR) Interrupt Enable.
0 Disable DSR Interrupt.
1 Enable DSR Interrupt.

SIER

5 DCD IE —Data Carrier Detect (DCD) Interrupt Enable.
0 Disable DCD Interrupt.
1 Enable DCD Interrupt.

SIER

4-0 —Not used.

GLOBAL REGISTERS

The global registers contain command information applying to different modes of operation and protocols. After changing global register data, TRES in the TCR and RRES in the RCR should be set then cleared prior to performing normal mode processing.

Protocol Select Register 1 (PSR1)

7	6	5	4	3	2	1	0
0	0	0	0	0	0	CTLEX	ADDEX

Reset value = $00

Protocol Select Register 1 (PSR1) selects BOP protocol related options.

PSR1

7-2 —Not used.

PSR1

1 CTLEX —Control Field Extend (BOP only).
0 Select 8-bit control field.
1 Select 16-bit control field.

PSR1

0 ADDEX —Address Extend (BOP only).
0 Disable address extension. All eight bits of the address byte are utilized for addressing.
1 Enable address extension. When bit 0 in the address byte is a 0 the address field is extended by one byte. An exception to the address field extension occurs when the first address byte is all 0's (null address).

Protocol Select Register 2 (PSR2)

7	6	5	4	3	2	1	0
WD/BYT	STOP BIT SEL		CHAR LEN SEL		PROTOCOL SEL		
	SB2	SB1	CL2	CL1	PS3	PS2	PS1

Reset value = $00

Protocol Select Register 2 (PSR2) selects protocols, character size, the number of stop bits, and word/byte mode.

PSR2

7 WD/BYT —Data Bus Word/Byte Mode.
0 Select byte mode. Selects the number of data bits to be transferred from the RxFIFO and the registers to the data bus and to be transferred from the data bus to the TxFIFO and the registers. The MPCC is initialized by $\overline{RESET}$ to the byte mode.
1 Select word mode. For operation with the 16-bit bus, select the word mode by sending $80 on D7 – D0 to address $19 prior to transferring subsequent data between the MPCC and the data bus.

PSR2

6-5 STOP BIT SEL —Number of Stop Bits Select. Selects the number of stop bits transmitted at the end of the data bins in ASYNC and ISOC modes.

6 SB2	5 SB1	No. of Stop Bits ASYNC	No. of Stop Bits ISOC
0	0	1	1
0	1	1-1/2	2
1	0	2	2

PSR2

4-3 **CHAR LEN SEL —Character Length Select.** Selects the character length except in BOP and BSC where the character length is always eight bits. Parity is not included in the character length.

4 CL2	3 CL1	Character Length
0	0	5 bits
0	1	6 bits
1	0	7 bits
1	1	8 bits

PSR2

2-0 **PROTOCOL SEL—Protocol Select.** Selects protocol and defines the protocol dependent control bits.

2 PS3	1 PS2	0 PS1	Protocol
0	0	0	BOP (Primary)
0	0	1	BOP (Secondary)
0	1	0	Reserved
0	1	1	COP
1	0	0	BSC EBCDIC
1	0	1	BSC ASCII
1	1	0	ASYNC
1	1	1	ISOC

Address Register 1 (AR1)

7	6	5	4	3	2	1	0
BOP ADDRESS/BSC & COP PAD							

Reset value = $00

Address Register 2 (AR2)

7	6	5	4	3	2	1	0
BSC & COP SYN							

Reset value = $00

The protocol selected in PSR2 (BOP, BSC and COP only) determines the function of the two 8-bit Address Registers (AR1 and AR2). As a secondary station in BOP, the contents of AR1 is used for address matching. In BSC and COP, AR1 and AR2 contain programmable leading PAD and programmable SYN characters, respectively.

Address Register (AR) Contents

Protocol Selected	AR1	AR2
BOP (Primary)	X	X
BOP (Secondary)	Address	X
BSC EBCDIC	Leading PAD	SYN
BSC ASCII	Leading PAD	SYN
COP	Leading PAD	SYN
*X = Not used		

Baud Rate Divider Register 1 (BRDR1)

7	6	5	4	3	2	1	0
BAUD RATE DIVIDER (LSH)							

Reset value = $01

Baud Rate Divider Register 2 (BRDR2)

7	6	5	4	3	2	1	0
BAUD RATE DIVIDER (MSH)							

Reset value = $00

The two 8-bit Baud Rate Divider Registers (BRDR1 and BRDR2) hold the divisor of the Baud Rate Divider circuit. BRDR1 contains the least significant half (LSH) and BRDR2 contains the most significant half (MSH), With an 8.064 MHz EXTAL input, standard bit rates can be selected using the combination of Prescaler Divider (in the CCR) and Baud Rate Divider values shown in Table 3. For isochronous or synchronous protocols, the Baud Rate Divider value must be multiplied by two for the same Prescaler Divider value.

The Baud Rate Divider (BRD) value can be computed for other crystal frequency, prescaler divider and desired baud rate values as follows:

$$BRD = \frac{\text{Crystal Frequency}}{\text{(Prescaler Divider) (Baud Rate) (K)}}$$

where: K = 1 for isochronous or synchronous
2 for asynchronous

Clock Control Register (CCR)

7	6	5	4	3	2	1	0
0	0	0	PSCDIV	TCLKO	RCLKIN	CLK SEL	
						CK2	CK1

Reset value = $00

The CCR selects various clock options.

CCR

7-5 **—Not used.**

CCR

4 **PSCDIV —Prescaler Divider.** The Prescaler Divider network reduces the external/oscillator frequency to a value for use by the internal Baud Rate Generator.

0 Divide by 2.
1 Divide by 3.

CCR

3 **TCLKO —Transmitter Clock Output Select.**

0 Select TxC to be an input.
1 Select TxC to be an output. (1X clock)

Table 3. Standard Baud Selection (8.064 MHz Crystal)

Desired Baud Rate (Bit Rate)	Prescaler Divider		Baud Rate Divider					
			Asynchronous			Isochronous and Synchronous		
				Hexadecimal Value			Hexadecimal Value	
	Decimal Value	PSCDIV (0 to 1)	Decimal Value	BRDR2 (MSH)	BRDR1 (LSH)	Decimal Value	BRDR2 (MSH)	BRDR1 (LSH)
50	3	1	26,880	69	00	53,760	D2	00
75	2	0	26,880	69	00	53,760	D2	00
110	3	1	12,218	2F	BA	24,436	5F	74
135	2	0	14,933	3A	55	29,866	74	AA
150	3	1	8,960	23	00	17,920	46	00
300	2	0	6,720	1A	40	13,440	34	80
1200	3	1	1,120	04	60	2,240	08	C0
1800	2	0	1,120	04	60	2,240	08	C0
2400	2	0	840	03	48	1,680	06	90
3600	2	0	560	02	30	1,120	04	60
4800	3	1	280	01	18	560	02	30
7200	2	0	280	01	18	560	02	30
9600	3	1	140	00	8C	280	01	18
19200	3	1	70	00	46	140	00	8C
38400	3	1	35	00	23	70	00	46

CCR

2 RCLKIN —Receiver Clock Internal Select (ASYNC only).

0 Select External RxC.

1 Select Internal RxC.

CCR

1-0 CLK DIV —External Receiver Clock Divider. Selects the divider of the external RxC to determine the receiver data rate.

CK2	CK1	Divider
0	0	1 (ISOC)
0	1	16
1	0	32
1	1	64

Error Control Register (ECR)

7	6	5	4	3	2	1	0
PAREN	ODDPAR	—	—	CFCRC	CRCPRE	CRCSEL	
						CR2	CR1

Reset value = $04

The Error Control Register (ECR) selects the error detection method used by the MPCC.

ECR

7 PAREN —Parity Enable. (ASYNC, ISOC and COP only).

0 Disable parity generation/checking.

1 Enable parity generation/checking.

ECR

6 ODDPAR —Odd/Even Parity Select (Effective only when PAREN = 1).

0 Generate/check even parity.

1 Generate/check odd parity.

ECR

5-4 —Not used.

ECR

3 CFCRC —Control Field CRC Enable.

0 Disable control field CRC. Enables an intermediate CRC remainder to be appended after the address/control field in transmitted BOP frames and checked in received frames. The CRC generator is reset after control field CRC calculation.

ECR

2 CRCPRE —CRC Generator Preset Select.

0 Preset CRC Generator to 0.

1 Preset CRC Generator to 1 and transmit the 1's complement of the resulting remainder.

ECR

1-0 CRCSEL —CRC Polynomial Select. Selects one of the RC polynominals.

1 CR2	0 CR1	Polynominal
0	0	$x^{16}+x^{12}+x^5+1$ (CCITT V.41)
0	1	$x^{16}+x^{15}+x^2+1$ (CRC-16)
1	0	x^8+1 (VRC/LRC)*
1	1	Not used.

*VRC: Odd-parity check is performed on each character including the LRC character.

INPUT/OUTPUT FUNCTIONS

MPU INTERFACE

Transfer of data between the MPCC and the system bus involves the following signals:

	R68561	R68560
Address Lines	A1–A4	A0–A4
Data Lines	D0–D15	D0–D7
Read/Write	R/$\overline{W}$	R/$\overline{W}$
Data Transfer Acknowledge	$\overline{DTACK}$	$\overline{DTACK}$
Chip Select	$\overline{CS}$	$\overline{CS}$
Data Strobes	$\overline{UDS}$ and $\overline{LDS}$	$\overline{DS}$

Figures 10 and 11 show typical interface connections.

Read/Write Operation

The R/$\overline{W}$ input controls the direction of data flow on the data bus. $\overline{CS}$ (Chip Select) enables the MPCC for access to the internal registers and other operations. When $\overline{CS}$ is asserted, the data I/O buffer acts as an output driver during a read operation and as an input buffer during a write operation. $\overline{CS}$ must be decoded from the address bus and gated with address strobe ($\overline{AS}$).

When the R68561 is connected to the 16-bit bus for operation in the word mode (WD/BYT = 1 in the PSR2), address lines A1–A4 select the internal register(s) (the 8-bit control/status registers are accesed two at a time and the 16-bit data registers are accessed on even address boundaries). When the MPCC is selected ($\overline{CS}$ low) during a read (R/$\overline{W}$ high), 16 bits of register data are placed on the data bus when the data strobes ($\overline{LDS}$ and $\overline{UDS}$) are asserted. $\overline{LDS}$ strobes the eight data bits from the even numbered registers to the lower data bus lines (D0–D7) and $\overline{UDS}$ strobes the eight data bits from the odd numbered registers to the upper data bus lines (D8–D15). The MPCC asserts Data Transfer Acknowledge ($\overline{DTACK}$ prior to placing data on the data bus. Conversely, when the MPCC is selected ($\overline{CS}$ low) during a write (R/$\overline{W}$ low) $\overline{LDS}$ and $\overline{UDS}$ strobe data from the D0 – D7 and D8–D15 data bus lines into the addressed even and odd numbered registers, respectively, and the MPCC asserts $\overline{DTACK}$. $\overline{DTACK}$ is negated when $\overline{CS}$ is negated. Figures 12 and 13 show the read and write timing relationships.

When the R68560 is connected to the 8-bit bus for operation in the byte mode (WD/BYT = 0 in the PSR2), address lines A0–A4 select one internal 8-bit register. When the MPCC is selected ($\overline{CS}$ low) during a read (R/$\overline{W}$ high), eight bits of register data are placed on data bus lines D0–D7 when the data strobe ($\overline{DS}$) is asserted. When the MPCC is selected ($\overline{CS}$ low) for a write (R/$\overline{W}$ low), $\overline{DS}$ strobes data from the D0–D7 data lines into the selected register.

DMA INTERFACE

The MPCC is capable of providing DMA data transfers up to 2 Mbytes per second when used with the MC68440 or MC68450 DMAC in the single address mode. Based on 4 Mb/s serial data rate and 5 bits/character, the maximum DMA required transfer rate is 800 Kbytes per second.

The MPCC has separate DMA enable bits for the transmitter and receiver, each of which requires a DMA channel. Both the transmitter and receiver data are implicitly addressed (TDR or RDR) therefore addressing of the data register is not required before data may be transferred. Communication between the MPCC and the DMAC is accomplished by a two-signal request/acknowledge handshake. Since the MPCC has only one acknowledge input ($\overline{DACK}$) for its two DMA request lines, an external OR function must be provided to combine the two DMA acknowledge signals. The MPCC uses the R/$\overline{W}$ input to distinguish between the Transmitter Data Service Request ($\overline{TDSR}$ acknowledge and the Receiver Data Service Request ($\overline{RDSR}$) acknowledge.

Receiver DMA Mode

The receiver DMA mode is enabled when the RDSREN bit in the RCR is set to 1. When data is available in the RxFIFO, Receiver Data Service Request ($\overline{RDSR}$) is asserted for one receiver clock period (BOP and BSC) to initiate the MPCC to memory DMA transfer. For asynchronous operation, $\overline{RDSR}$ is asserted for 2–3 periods of the system clock depending on prescale factor. The next $\overline{RDSR}$ cycle may be initiated as soon as the current $\overline{RDSR}$ cycle is completed (i.e., a full sequence of $\overline{DACK}$, $\overline{DS}$, and $\overline{DTC}$).

In response to $\overline{RDSR}$ assertion, the DMAC sets the R/$\overline{W}$ line to write, asserts the memory address, address strobe, and DMA acknowledge. The MPCC outputs data from the RxFIFO to the data bus and the DMAC asserts the data strobes. The memory latches the data and asserts $\overline{DTACK}$ to complete the data transfer. The DMAC asserts $\overline{DTC}$ to indicate to the MPCC that data transfer is complete. Figure 13 shows the timing relationships for the receiver DMA mode.

$\overline{RDSR}$ is inhibited when either RDSREN is reset to 0 or RRES is set to 1 (both in the RCR), or when $\overline{RESET}$ is asserted.

Transmitter DMA Mode

The transmitter DMA mode is enabled when the TDSREN bit in the TCR is set to 1. When the TxFIFO is available, Transmitter Data Service Request ($\overline{TDSR}$) is asserted for one transmitter clock period to initiate the memory to MPCC DMA transfer. For asynchronous operation, $\overline{TDSR}$ is asserted for a period of one-half the transmitter baud rate. The next $\overline{TDSR}$ cycle may be initiated as soon as the current $\overline{TDSR}$ cycle is completed.

In the transmitter DMA mode, the TxFIFO Is implicitly addressed. That is, when the transfer is from memory to the TxFIFO, only the memory is addressed. In response to $\overline{TDSR}$ assertion, the DMAC sets the R/$\overline{W}$ line to read, asserts the memory address, the address strobe, the data strobes and DMA acknowledge. The memory places data on the data bus and asserts $\overline{DTACK}$. Data is valid at this time and will remain valid until the data strobes are negated. The DMAC asserts $\overline{DTC}$ to indicate to the MPCC that data is available. The MPCC loads the data into the TxFIFO on the negation (rising edge) of $\overline{DS}$ and the transfer is complete. A timing diagram for the transmitter DMA Mode is shown in Figure 15.

$\overline{TDSR}$ is inhibited when either TDSREN is reset to 0 or TRES is set to 1 (both in the TCR), or when $\overline{RESET}$ is asserted.

$\overline{DONE}$ Signal

When the DMA transfer count is exhausted in transmitter DMA mode, the DMAC asserts $\overline{DONE}$ which sets the TLAST bit in the TCR to indicate that the last word/byte has been transferred. In the receiver DMA mode, $\overline{DONE}$ is asserted by the MPCC coincident with $\overline{DACK}$ when the last character of the frame/block is being transferred from the RxFIFO to the data bus if the DONEEN bit is set to a 1 in the RCR.

CAUTION

$\overline{DONE}$ is reasserted with each occurrence of $\overline{DACK}$ until EOF is cleared in the RSR.

INTERRUPTS

If an interrupt generating status occurs and the interrupt is enabled, the MPCC asserts the $\overline{IRQ}$ output. Upon receiving $\overline{IACK}$ for the pending interrupt request, the MPCC places an interrupt vector on D0–D7 data bus and asserts $\overline{DTACK}$.

The MPCC has three vector registers: Receiver Interrupt Vector Number Register (RIVNR), Transmitter Interrupt Vector Number Register (TIVNR), and Serial Interrupt Vector Number Register (SIVNR). The receiver interrupt has higher priority over the transmitter interrupt, and the transmitter interrupt has priority over the serial interface interrupt. For example, if a pending interrupt request has been generated simultaneously by the receiver and the transmitter, the Receiver Interrupt Vector Number (RIVN) is placed on D0–D7 when acknowledged by the MPU. Upon completion of the first interrupt request cycle (which clears the receiver interrupt), $\overline{IRQ}$ will remain low to start the transmitter interrupt cycle. $\overline{IRQ}$ is negated by clearing all bits set in a status register that could have caused the interrupt.

CAUTION

A higher priority interrupt occurring while $\overline{IACK}$ is low during transfer of a lower priority interrupt vector to the MPU will cause the lower priority interrupt vector on the data bus to be invalid if there are any 1's in the higher priority interrupt vector in the same bit positions as any 0's in the lower priority interrupt vector. To prevent this problem from occurring, ensure that the higher priority interrupt vectors contain 1's only in bit positions where there are 1's in the lower priority interrupt vectors, e.g.:

Vector	Vector Value (Hex)	Vector Value (Binary)
Receiver Interrupt Vector Number (RIVN)	44	01000100
Transmitter Interrupt Vector Number (TIVN)	4C	01001100
Serial Interrupt Vector Number (SIVN)	5C	01011100

A timing diagram for the interrupt acknowledge sequence is shown in Figure 15.

SERIAL INTERFACE

The MPCC is a high speed, high performance device supporting the more popular bit and character oriented data protocols. The lower speed asynchronous (ASYNC) and isochronous (ISOCH) modes are also supported. An on-chip clock oscillator and baud rate generator provide an output data clock at a frequency of DC to 4 MHz. The clock can also be used in the ASYNC mode to provide a receive clock for the incoming data. The serial interface consists of the following signals:

$\overline{RTS}$ (Request to Send) Output

The $\overline{RTS}$ output to the DCE is controlled by the RTSLVL bit in the SICR in conjunction with the state of the transmitter section. When the RTSLVL bit is set to 1, the $\overline{RTS}$ output is asserted. When the RTSLVL bit is reset to 0, the $\overline{RTS}$ output remains asserted until the TxFIFO becomes empty or the end of the message (or frame), complete with CRC code if any, has been transmitted. $\overline{RTS}$ also is negated when the RTSLVL bit is reset during transmitter idle, or when the $\overline{RESET}$ input is asserted.

$\overline{CTS}$ (Clear to Send) Input

The $\overline{CTS}$ input signal is normally generated by the DCE to indicate whether or not the data set is ready to receive data. The CTST bit in the SISR reflects the transition status of the $\overline{CTS}$ input while the CTSLVL bit in the SISR reflects the current level. A positive transition on the $\overline{CTS}$ pin asserts $\overline{IRQ}$ if the CTS IE bit in the SIER is set. The $\overline{CTS}$ input in an inactive state disables the start of transmission of each frame.

$\overline{DCD}$ (Data Carrier Detect) Input

The $\overline{DCD}$ input signal is normally generated by the DCE and indicates that the DCE is receiving a data carrier signal suitable for demodulation. The DCDT bit in the SISR reports the transition status of the $\overline{DCD}$ input while the DCDLVL bit in the SISR contains the current level. A positive transition on the $\overline{DCD}$ pin asserts the $\overline{IRQ}$ output if the DCD IE bit in the SIER is set. A negated $\overline{DCD}$ input disables the start of the receiver but does not stop the operation of an incoming message already in progress.

$\overline{DSR}$ (Data Set Ready) Input/RSYN Output

The DSRT input from the DCE indicates the status of the local set. The DSRT bit in the SISR contains the transition status of the $\overline{DSR}$ input while the DSRLVL bit in the SISR reports the current level. A negative transition on the $\overline{DSR}$ pin asserts the $\overline{IRQ}$ output if the DSR IE bit in the SIER is set.

When the RSYN bit in the RCR is set to 1, the frame synchronization signal (RSYN) in the receiver is output on the $\overline{DSR}$ pin. In this mode, $\overline{DSR}$ output low indicates detection of SYN in BSC or COP, or an address match in BOP.

$\overline{DTR}$ (Data Terminal Ready) Output

The $\overline{DTR}$ output is general purpose in nature and can be used to control switching of the DCE. The $\overline{DTR}$ output is controlled by the DTRLVL bit in the SICR.

TxC (Transmitter Clock) Input/Output

The transmitter clock (TxC) may be programmed to be input or an output. When the TCLKO control bit in the CCR is set to a 1, the TxC pin becomes an output and provides the DCE with a clock whose frequency is determined by the internal baud rate generator. When the TCLKO control bit is reset, TxC is an input and the transmitter shift timing must be provided externally. The TxD output changes state on the negative-going edge of the transmitter clock. In the asynchronous mode when TCLKO = 0 in the CCR, the TxC input frequency must be two times the desired baud rate.

TxD (Transmitted Data) Output

The serial data transmitted from the MPCC is coded in NRZ or NRZI (zero complement) data format as selected by the NRZI control bit in the SICR.

RxC (Receiver Clock) Input

The receiver latches data on the negative transition of the RxC.

RxD (Received Data) Input

The serial data received by the MPCC can be coded in NRZ or NRZI data format. The MPCC will decode the received data in accordance with the NRZI control bit setting in the SICR.

Serial Interface Timing

The timing for the serial interface clock and data lines is shown in Figure 18. The MPCC supports high speed synchronous operation. As shown, the TxD output changes with the negative-going edge of TxC and the received data on RxD is latched on the negative edge of RxC. This assures high speed two-way operation between two MPCCs connected as shown in Figure 17.

For low speed operation between the MPCC and a modem or RS-232C Data Communications Equipment (DCE), an inverter can be used in the TxC output lines as shown in Figure 17. RS-232 and RS-423 (covering serial data interface up to 100K baud) require that data be centered ±25% about the negative-going edge of the RxC. This criteria is met for frequencies up to 1.25 MHz using the inverter. Use of the inverter also allows MPCC to MPCC operation up to 2.17 MHz.

SERIAL COMMUNICATION MODES AND PROTOCOLS

ASYNCHRONOUS AND ISOCHRONOUS MODES

Asynchronous and isochronous data are transferred in frames. Each frame consists of a start bit, 5 to 8 data bits plus optional even or odd parity, and 1, 1½, or 2 stop bits. The data character is transmitted with the least significant bit (LSB) first. The data line is normally held high (MARK) between frames, however, a BREAK (minimum of one frame length for which the line is held low) is used for control purposes. Figure 4 illustrates the frame format supported by the MPCC.

Asynchronous Receive

In the asynchronous (ASYNC) mode, data received on RxD occurs in three phases: (1) detection of the start bit and bit synchronization, (2) character assembly and optional parity check, and (3) stop bit detection. The receiver bit stream may be synchronized by the internal baud rate generator clock or by an external clock on RxC. When RCLKIN in the CCR is set to 0, an external clock with a frequency of 16, 32, or 64 times the data rate establishes the data bit midpoint and maintains bit synchronization. The character assembly process does not start if the start bit is less than one-half bit time. Framing and parity errors are detected and buffered along with the character on which errors

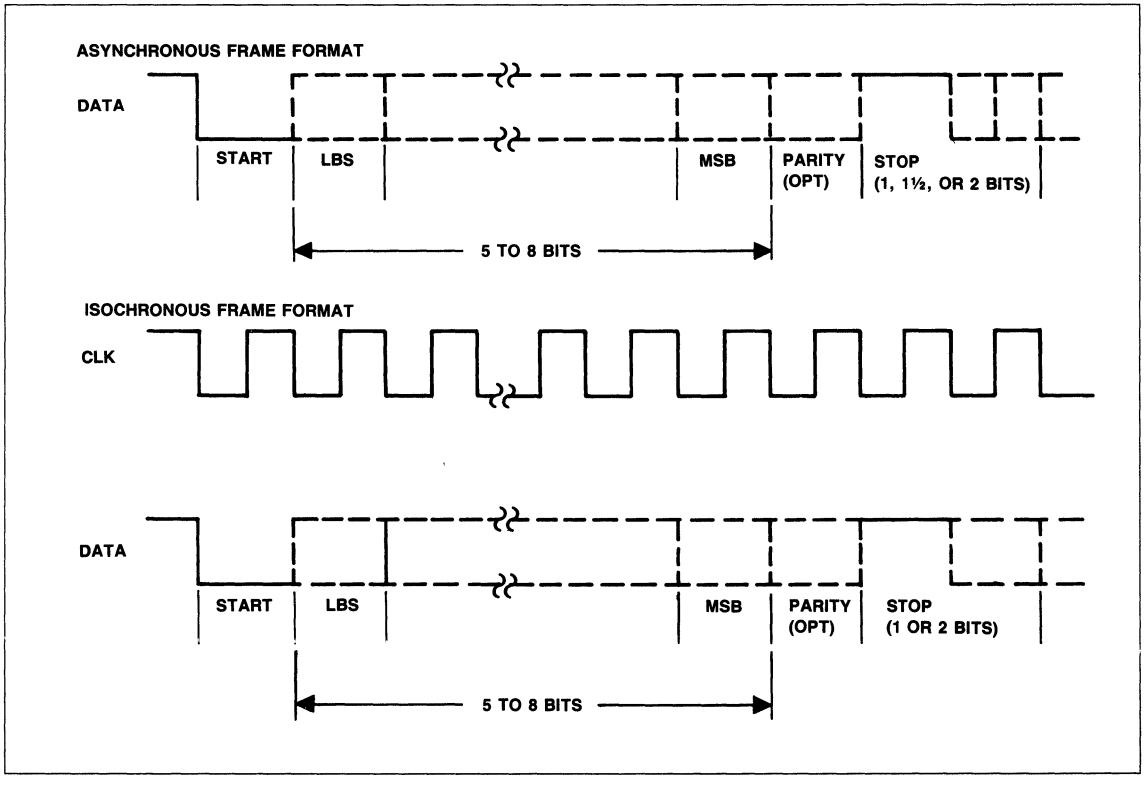


Figure 4. Asynchronous and Isochronous Frame Format

bit is less than one-half bit time. Framing and parity errors are detected and buffered along with the character on which errors occurred. They are passed on to the RxFIFO and set appropriate status bits in the RSR when the character with an error reaches the last RxFIFO register where it is ready to be transferred onto the data bus via the RDR.

Isochronous Receive

In the isochronous (ISOC) mode, a 1 times clock on RxC is required with the data on RxD and the serial data bit is latched on the falling edge of each clock pulse. The requirement for the detection of a valid start bit, or the beginning of a break, is satisfied by the detection of a high-to-low transition on the serial data input line. Error detection and status indication are the same as the asynchronous mode.

Asynchronous and Isochronous Transmit

In asynchronous and isochronous transmit modes, output data transmission on TxD begins with the start bit. This is followed by the data character which is transmitted LSB first. If parity generation is enabled, the parity bit is transmitted after the MSB of the character.

SYNCHRONOUS MODES

In synchronous modes, a one-times clock is provided along with the data. Serial output data is shifted out and input data is latched on the falling edge of the clock.

BIT ORIENTED PROTOCOLS (BOP)

In bit oriented protocols (BOP), messages (data) are transmitted and received in frames. Each frame contains an opening flag, address field, control field, frame check sequence, and a closing flag. A frame may also contain an information field. (See Figure 5).

The opening flag is a special character whose bit pattern is 01111110. It marks the frame boundaries and is the interframe fill character. The address field of a frame contains the address of the secondary station which is receiving or responding to a command. The address field may be one or more bytes long. The address field can be extended by setting the ADDEX bit to a 1 in PSR1. In this case, the address field will be extended until the occurrence of an address byte with a 1 in bit 0. The first byte of the address field is automatically checked when the MPCC is programmed to be a secondary station in BOP. An automatic check for global (11111111) or null (00000000) address is also made. The control field of one or two bytes is transparent to the MPCC and sent directly to the host without interpretation.

The optional information field consists of 8-bit characters. Cyclic redundancy checking is used for error detection and the CRC remainder resulting from the calculation is transmitted as the frame check sequence field. For BOP, the polynomial $X^{16} + X^{12} + X^5 + 1$ (CRC-CCITT) should be used, i.e., selected in the CRC SEL bits in the ECR. The registers representing the CRC-CCITT polynomial are generally preset to all 1s, and the 1s complement of the resulting remainder is transmitted. (See X.25 Recommendation.)

Zero insertion/deletion is employed to prevent valid frame data from being confused with the special characters. A 0 is inserted by the transmitter after every fifth consecutive 1 in the data stream. These inserted zeros are removed by the receiver to restore the data to its original form. The inserted zeros are not included in the CRC calculation.

The end of the frame is determined by the detection of the closing Flag special character which is the same is the opening Flag.

With the control options offered by the MPCC, commonly used bit oriented protocols such as SDLC, HDLC and X.25 standards can be supported. Figure 6 compares the requirements of these options.

BOP Receiver Operation

In BOP, the receiver starts assembling characters and accumulating CRC immediately after the detection of a Flag. The receiver also continues to search for additional Flag, or Abort, characters on a bit-by-bit basis. Zero deletion is implemented in the Receiver Shift Register after the Flag detection logic and before the CRC circuitry. The receiver recognizes the shared flag (the closing flag for one frame serves as the opening flag for the next frame) and the shared zero (the ending 0 of a closing flag serves as the beginning 0 of an opening flag forming the pattern "011111101111110."

Character assembly and CRC accumulation are stopped when a closing Flag or Abort is detected. The CRC accumulation includes all the characters between the opening Flag and the closing Flag. The contents of the CRC register are checked at the close of a frame and the C/PERR bit in the RSR is updated. The FCS and the Flag are not passed on to the RxFIFO.

FLAG 01111110	ADDRESS 1 OR N BYTES	CONTROL 1 OR 2 BYTES	INFORMATION N BYTES (OPTIONAL)	FCS 2 BYTES	FLAG 01111110

Figure 5. Bit Oriented Protocol (BOP) Frame Format

IBM SDLC FRAME FORMAT

FLAG 01111110	ADDRESS 1 BYTE	CONTROL 1 BYTE	INFORMATION N BYTES	FCS 2 BYTES	FLAG 01111110

ADCCP/HDLC FRAME FORMAT

FLAG 01111110	ADDRESS N BYTES	CONTROL 1 OR 2 BYTES	INFORMATION N BYTES	FCS 2 BYTES	FLAG 01111110

Figure 6. Implemented Bit Oriented Protocols

If the Flag is a closing flag, checks for short frame (no control field) and CRC error conditions are made and the appropriate status is updated. When an Abort (seven 1s) is detected, the remaining frame is discarded and the RA/B bit is set in the RSR. When a link idle (15 or more consecutive 1s) is detected, the RIDLE status bit is set in the RSR. The zeros that have been inserted to distinguish data from special characters are detected and deleted from the data stream before characters are assembled. The MPCC programmed as a secondary station provides automatic address matching of the first byte. If there is no address match, the receiver (secondary station) ignores the remainder of the frame by searching for the Flag. If there is a match, the address bytes are transferred to the RxFIFO as they are assembled.

For the control field, one or two bytes are assembled and passed on to the RxFIFO depending on the state of the extended control field bit.

If the CFCRC bit in the ECR is set to 1, an intermediate CRC check will be made after the address and control field. The Frame Check Sequence is still calculated over the remainder of the frame.

BOP Transmitter Operation

In BOP, the TxFIFO can be preloaded through the TDR while the transmitter is disabled (TEN = 0 in the TCR). When the transmitter is enabled (TEN = 1 in the TCR), the leading Flag is automatically sent prior to transmitting data from the TxFIFO. The TDRA bit is set to 1 in the TSR as long as TxFIFO is not full. If an underrun occurs, the TUNRN bit in the TSR is set to a 1 and an Abort (11111111) is transmitted followed by continuous Flags or marks until a new sequence is initiated.

The TLAST bit in the TCR must be set prior to loading the last character of the message to signal the transmitter to append the two-byte Frame Check Sequence (FCS) following the last character. If the transmitter DMA mode is selected (the TDSREN bit set to 1 in the TCR) the TLAST bit is set by the $\overline{\text{DONE}}$ signal from the DMAC.

A message may be terminated at any time by setting the TABT bit in the TCR to 1. This causes the transmitter to send an Abort character followed by the remainder of the current frame data in the TxFIFO.

The serial data from the Transmitter Shift Register is continuously monitored for five consecutive 1s, and a 0 is inserted in the data stream each time this condition occurs (excluding Flag and Abort characters).

CRC accumulation begins with the first non-Flag character and includes all subsequent characters. The CRC remainder is transmitted as the FCS following the last data character. If the CTLCRC bit in the ECR is set to 1, an intermediate CRC remainder is appended after the Address and Control field. The final Frame Check Sequence is calculated over the balance of the frame.

BISYNC (BSC)

The structure of messages utilizing the IBM Binary Synchronous Communications (BSC) protocol, commonly called Bisync, is shown in Figure 7. The MPCC can process both transparent and nontransparent messages using either the EBCDIC or the ASCII codes. The CRC-16 polynomial should be selected by setting the appropriate CRCSEL bits in the ECR for both transparent and non-transparent EBCDIC and for transparent ASCII coded messages. VRC/LRC should be selected for non-transparent ASCII coded messages. BSC messages are formatted using defined data-link control characters. Data-link control characters generated and recognized by the MPCC are listed in Table 4.

A heading is a block of data starting with an SOH and containing one or more characters that are used for message control (e.g., message identification, routing, and priority). The SOH initiates the block-check-character (BCC) accumulation, but is not included in the accumulation. The heading is terminated by STX when it is part of a block containing both heading and text. A block containing only a heading is terminated with an ITB or an ETB followed by the BCC. Only the first SOH or STX in a transmission block following a line turnaround causes the BCC to reset. All succeeding STX or SOH characters are included in the BCC. This permits the entire transmission (excluding the first SOH or STX) to be block-checked.

The text data is transmitted in complete units called messages, which are initiated by STX and concluded with ETX. A message can be subdivided into smaller blocks for ease in processing and more efficient error control. Each block starts with STX and ends with ETB (except for the last block of a message, which ends with ETX). A single transmission can contain any number of blocks (ending with ETB) or messages (ending with ETX). An EOT following the last ETX block indicates a normal end of transmission. Message blocking without line turnaround can be accomplished by using ITB (see the Additional Data Link Capabilities section, IBM GA 27-3004-2).

Table 4. BSC Control Sequences—Inclusion in CRC Accumulation

ASCII			EBCDIC		
Command	**Byte 1**	**Byte 2**	**Command**	**Byte 1**	**Byte 2**
SYN	16*	—	SYN	32*	—
SOH	01	—	SOH	01	—
STX	02	—	STX	02	—
ETB	17	—	EOB (ETB)	26	—
ETX	03	—	ETX	03	—
ENQ	05	—	ENQ	2D	—
DLE	10	—	DLE	10	—
ITB	1F	—	ITB	1F	—
EOT	04	—	EOT	37	—
ACK N*	10	30-37	ACK 0	10	70
NAK	15	—	ACK 1	10	61
WACK	10	3B	NAK	3D	—
RVI	10	3C	WACK	10	6B
			RVI	10	7C

Note: *Programmable

Two modes of data transfers are used in BSC. In non-transparent mode, data link control characters may not appear as text data. In transparent mode, each control character is preceded by a data link escape (DLE) character to differentiate it from the text data. Table 5 indicates which control characters are excluded in the CRC generation. All characters not shown in the table are included in the CRC generation. Figure 8 shows various formats for Control/Response Blocks and Heading and Text Blocks.

Table 5. BSC Control Sequences — Inclusion in CRC Accumulation

Character of Sequence	Included in CRC Accumulation	
	Yes	No
TSYN	—	DLESYN
TSOH	—	DLESOH
TSTX*	—	DLESTX
TETB	ETB	DLE
TETX	ETX	DLE
TDLE	(DLE)DLE	DLE(DLE)

*If not preceded within the same block by transparent heading information.

LEADING PAD 1 BYTE (AR1)	SYN 1 BYTE (AR2)	SYN 1 BYTE (AR2)	BODY	BCC	TRAILING PAD 11111111

Figure 7. BSC Block Format

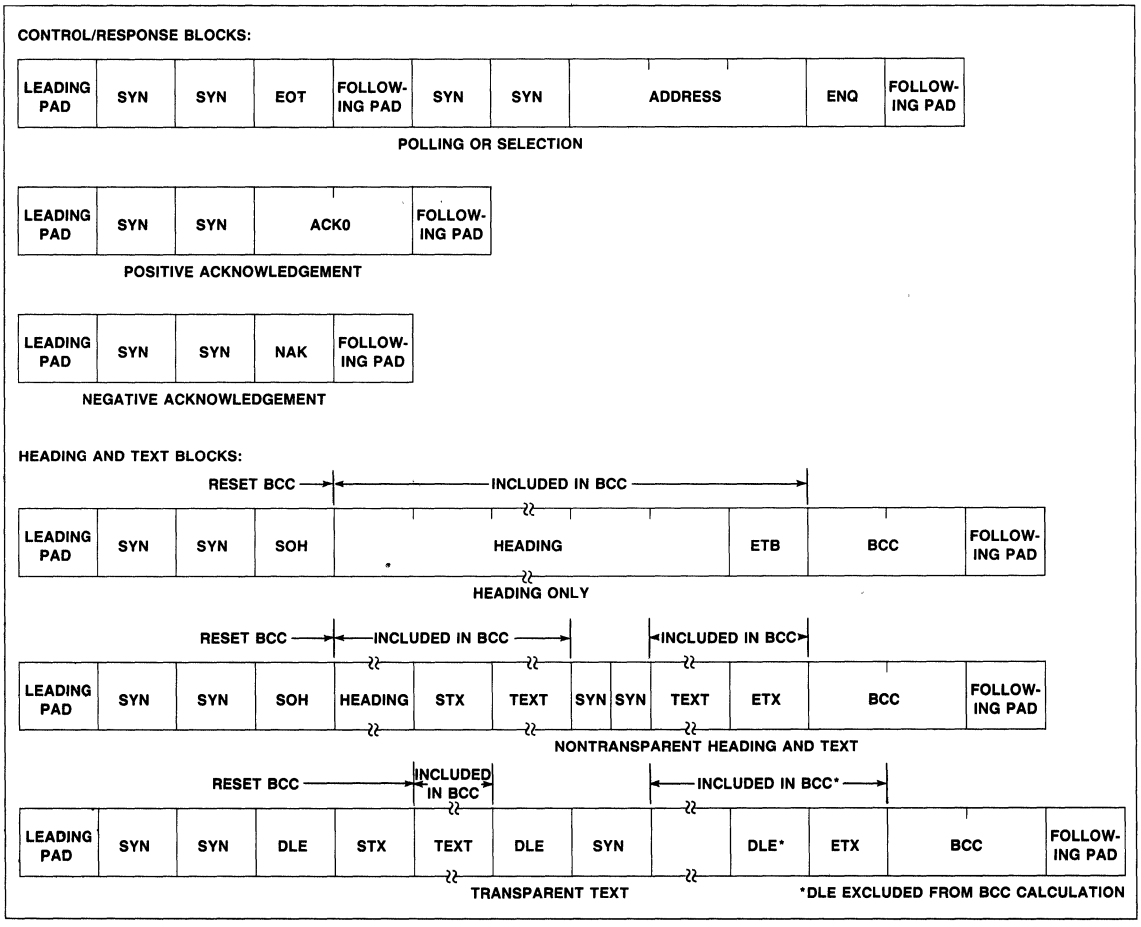


Figure 8. BSC Message Format Examples

BSC Receiver Operation

Character length defaults to eight bits in BSC mode. When ASCII is selected, the eighth bit is used for parity provided that VRC/LRC polynomial is selected. Character assembly starts after the receipt of two consecutive SYN characters. Serial data bits are shifted through the Receiver Shift Register into the Serial-to-Parallel Register and transferred to the RxFIFO. The RDA status bit in the RSR is set to 1 each time data is transferred to the RxFIFO. The SYN character pairs in non-transparent mode and DLE-SYN pairs in transparent mode are discarded.

The receiver starts each block in the non-transparent mode. It switches to transparent mode if a block begins with a DLE-SOH or DLE-STX pair. The receiver remains in transparent mode until a DLE-ITB, DLE-ETB, DLE-ETX or DLE-ENQ pair is received. BCC accumulation begins after an opening SOH, STX, or DLE-STX. SYN characters in non-transparent mode or DLE-SYN pairs in transparent mode are excluded from the BCC accumulation. The first DLE of a DLE-DLE sequence is not included in the BCC accumulation and is discarded. The BCC is checked after receipt of an ITB, ETB, or ETX in non-transparent mode or DLE-ITB, DLE-ETB, DLE-ETX in transparent mode. If a CRC error is detected, the C/PERR and EOF bits in the RSR are set to 1. If no error is detected only the EOF bit is set. If the closing character was an ITB, BCC accumulation and character assembly starts again on the first character following the BCC.

BSC Transmitter Operation

BSC transmission begins with the sending of an opening pad (PAD) and two sync (SYN) characters. These characters are programmable and stored in AR1(PAD) and AR2(SYN). SOH or STX initiates the block-check-character (BCC) accumulation. An initial SOH or STX is not included in the BCC accumulation. Should an underrun condition occur, the content of AR2 (normally SYN character) is transmitted until new characters become available. The message is terminated by the transmission of the BCC followed by a closing pad when an ETB, ITB, or ETX is fetched from the TxFIFO. The closing PAD is generated by the MPCC.

In transparent mode, the BCC accumulation is initiated by DLE-STX and is terminated by the sequences DLE-ETX, DLE-ETB, or DLE-ITB. See Table 5 for character sequence and inclusion in CRC accumulation. If an underrun occurs, DLE-SYN characters will be transmitted until new characters are available in the TxFIFO. ETC, ETX, ITB, or ENQ with a TLAST tag is treated as a control character and the MPCC automatically inserts a DLE immediately preceding these characters. DLE-ETB, DLE-ETX, DLE-ITB, or DLE-ENQ terminates a block of transparent text, and returns the data link to normal mode. BCC generation is not used for messages beginning with characters other than SOH, STX, DLE-SOH, or DLE-STX. On all message types, if the TSYN bit is set to 1 in the TCR, a SYN-SYN (DLE-SYN sequence on transparent messages) sequence is transmitted before the next character is fetched from the TxFIFO.

CHARACTER ORIENTED PROTOCOLS

The character oriented protocol (COP) option uses the format shown in Figure 9. It may be used for various character oriented protocols with 5-8 bit character sizes and optional parity checking. The input data is checked on a bit-by-bit basis for a pair of consecutive SYN characters to establish character synchronization. These SYN characters are discarded after detection. The PAD and SYN characters may be 5-8 bits long and are user programmable as stored in AR1 and AR2, respectively.

If parity checking is enabled the characters assembled after character sync are checked for parity errors. If STRSYN is set in the RCR, all SYN characters detected within the message will be discarded and will not be passed on to the RxFIFO. If STRSYN is reset, SYNs detected within the message will be treated as data.

DMA CONSIDERATIONS

When the R68561, in the word mode, is used with a DMAC, high throughput of bit-oriented protocols is achieved. However, problems can arise when trying to DMA byte-oriented data in the word mode.

BOP and BSC have well-defined message boundaries and the MPCC can detect the end of message, determine if there is an odd (single) byte at the end of a message, and so inform the host MPU by setting the Received Half Word (RHW) bit in the Frame Status byte.

In byte-oriented protocols (such as ASYNC and COP) there is no defined message length. In the word mode, received bytes are grouped in pairs. In the byte mode, each byte is available through the RxFIFO as it is received. Thus, the MPCC in the word mode has no way of knowing when an odd (single) byte has been received at an end of a transmission to be passed onto the host MPU.

For transmission of data by the MPCC in the word mode, the MPCC provides a Transmit Half Word (THW) bit in the Transmit Control Register. When set, this bit informs the MPCC that the last word in the TxFIFO (marked by setting the TLAST bit with $\overline{\text{DONE}}$) contains only the upper byte as valid data. However, the current available DMACs have no method to inform the MPCC that the last word of the message contains a single byte and MPU intervention is unrealistic.

Therefore, for bit-oriented protocols, the R68561 in the word mode can be efficiently used with a DMAC. To handle byte-oriented protocols with DMAC, an R68561 in the byte mode or the R68560 (byte mode only) should be used.

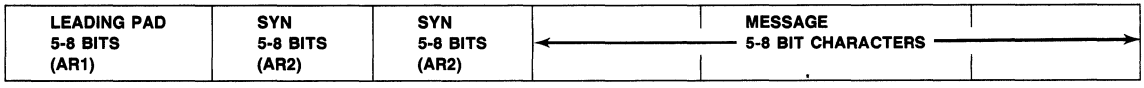


Figure 9. Character Oriented Protocol Format

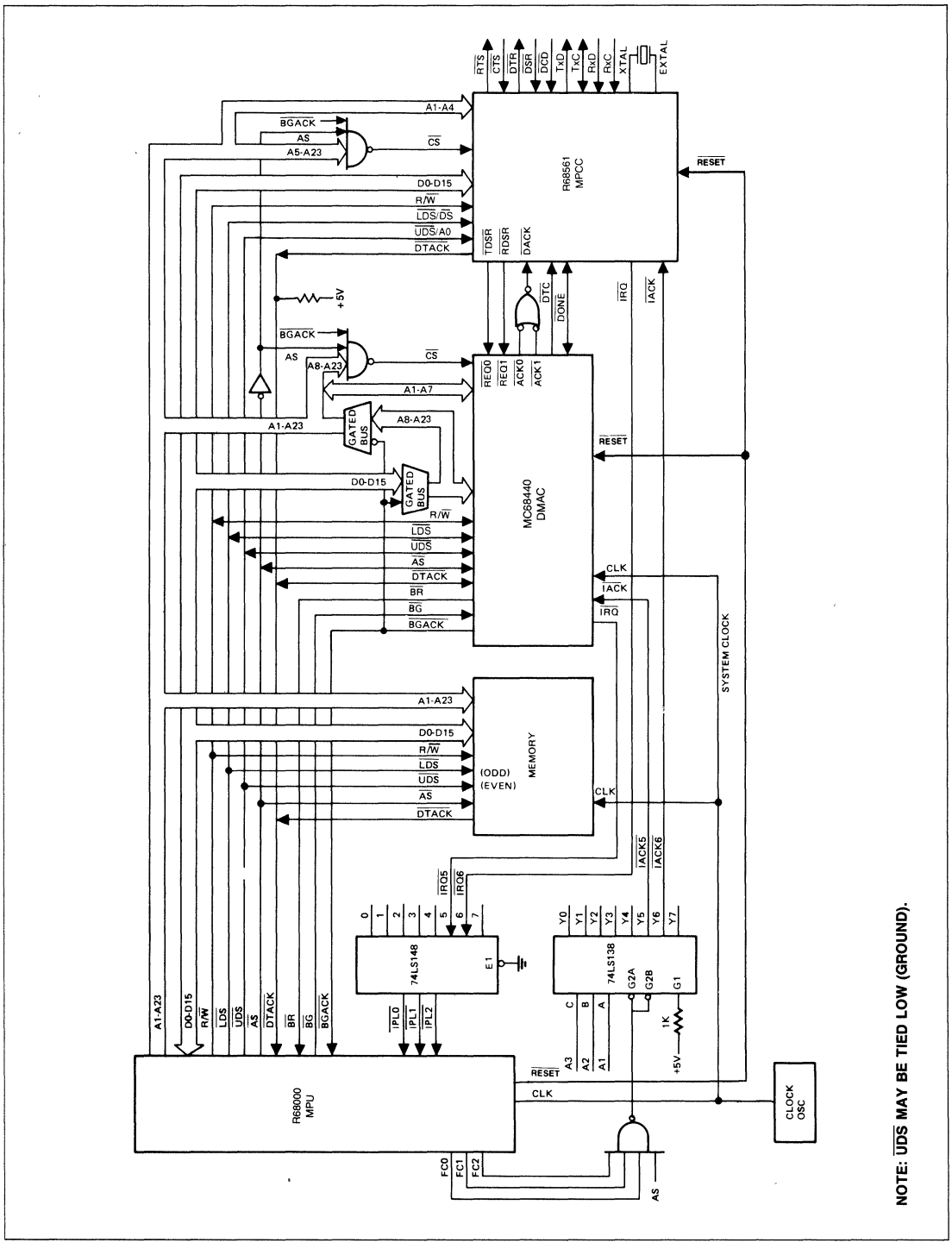


Figure 10. Typical Interface to 68000-Based System

NOTE: $\overline{UDS}$ MAY BE TIED LOW (GROUND).

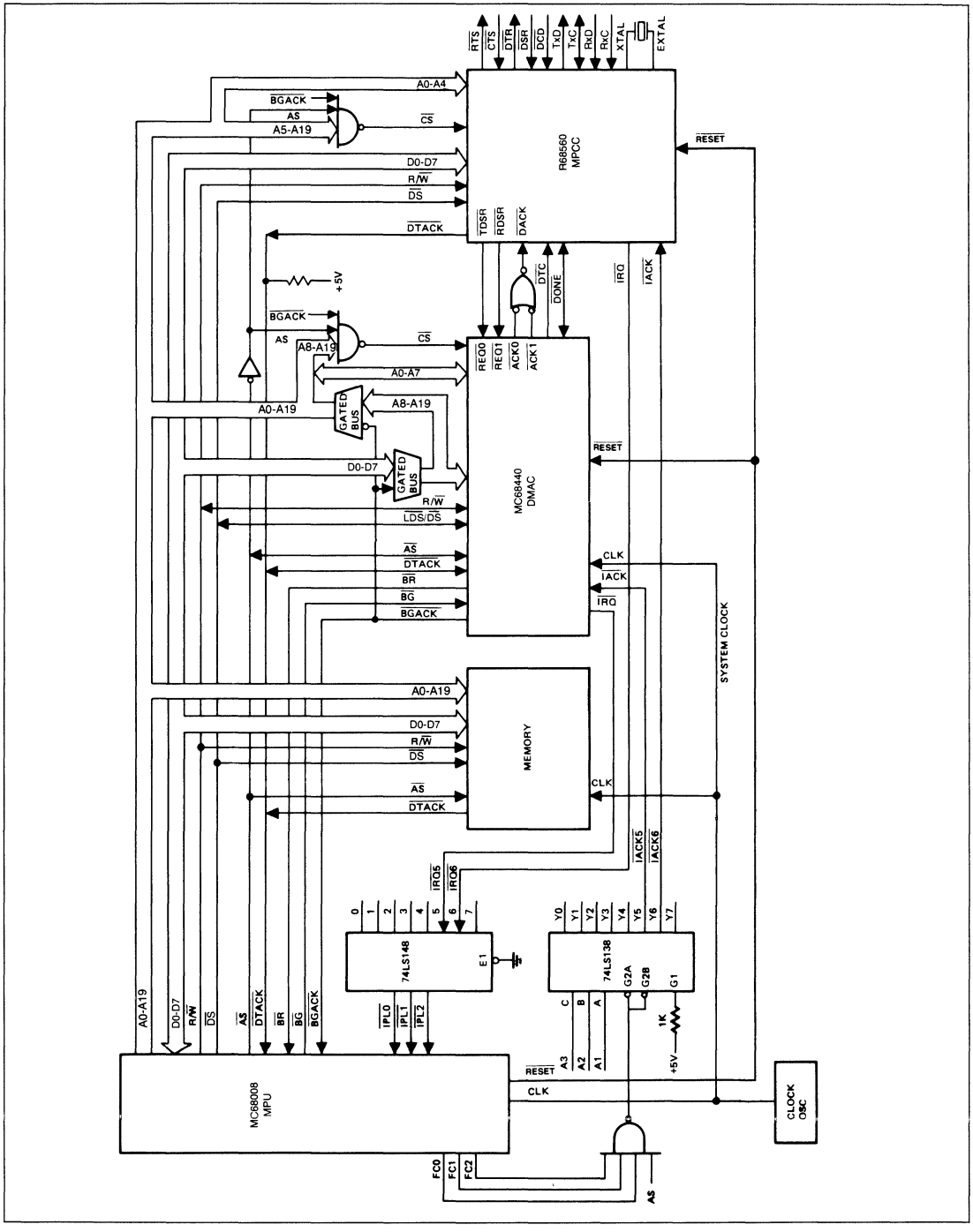
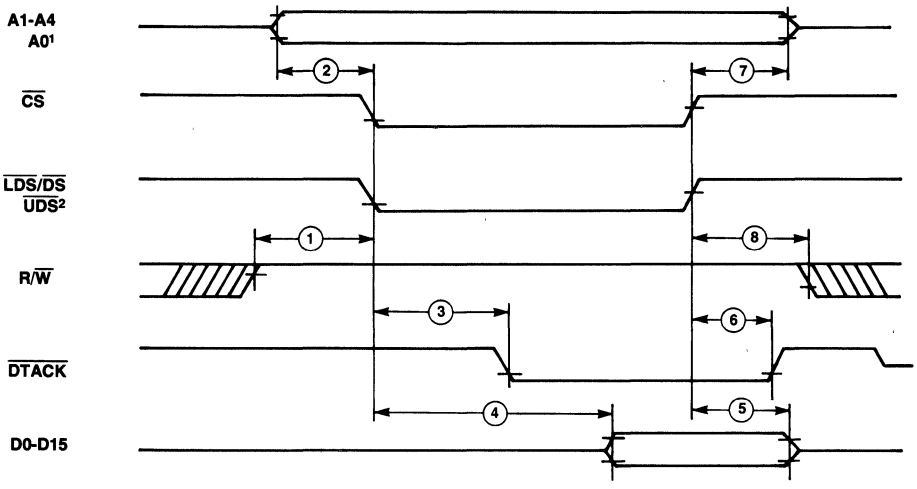
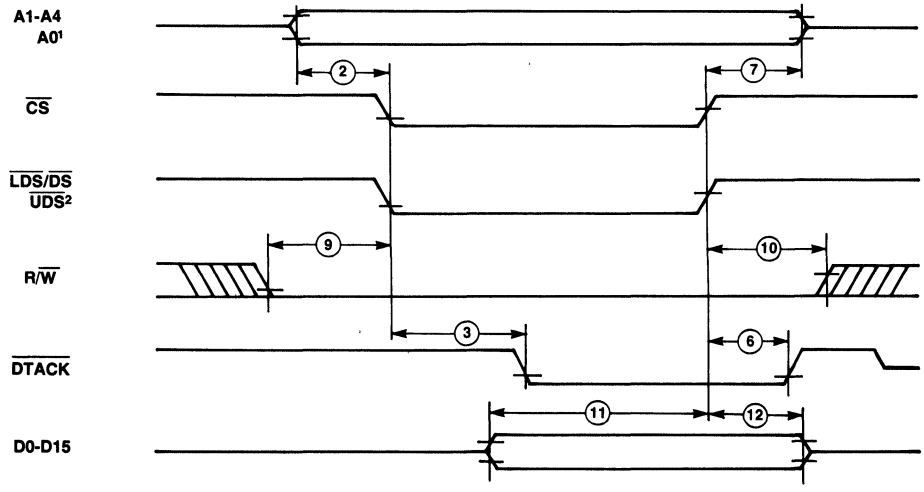


Figure 11. Typical Interface to 68008-Based System



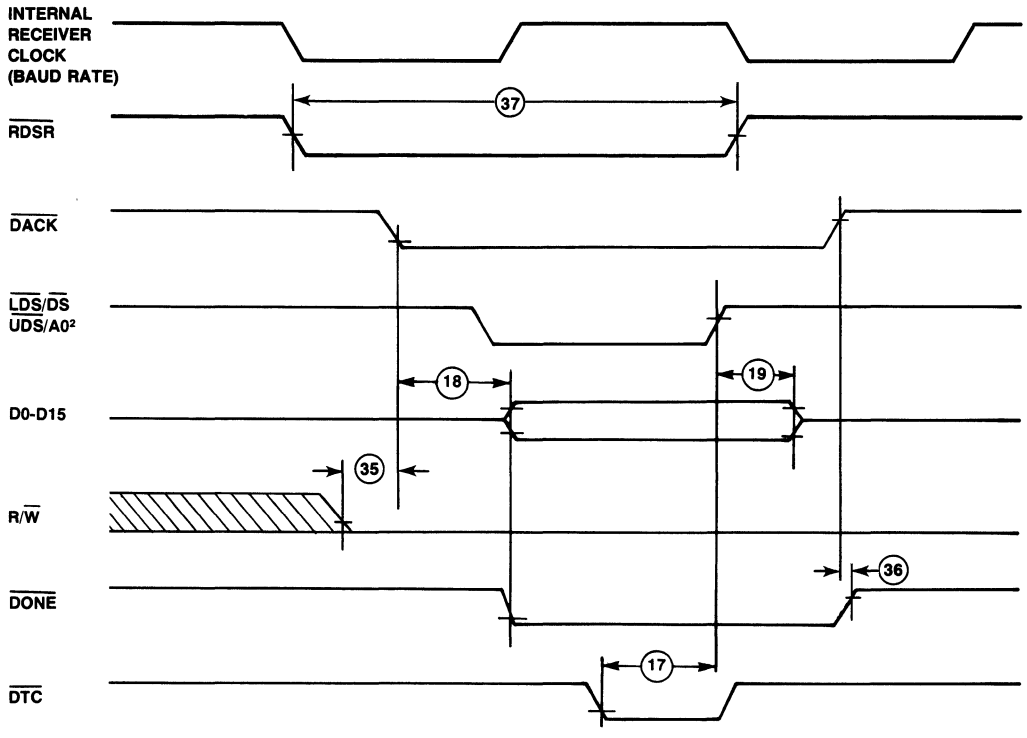
NOTES:
1. BYTE MODE WHEN CONNECTED TO A0 ON 68008 BUS.
2. WORD MODE WHEN CONNECTED TO $\overline{UDS}$ ON 68000 BUS.
3. TIMING MEASUREMENTS ARE REFERENCED TO AND FROM A LOW VOLTAGE OF 0.8 VOLTS AND A HIGH VOLTAGE OF 2.0 VOLTS, UNLESS OTHERWISE NOTED.

Figure 12. MPCC Read Cycle Timing



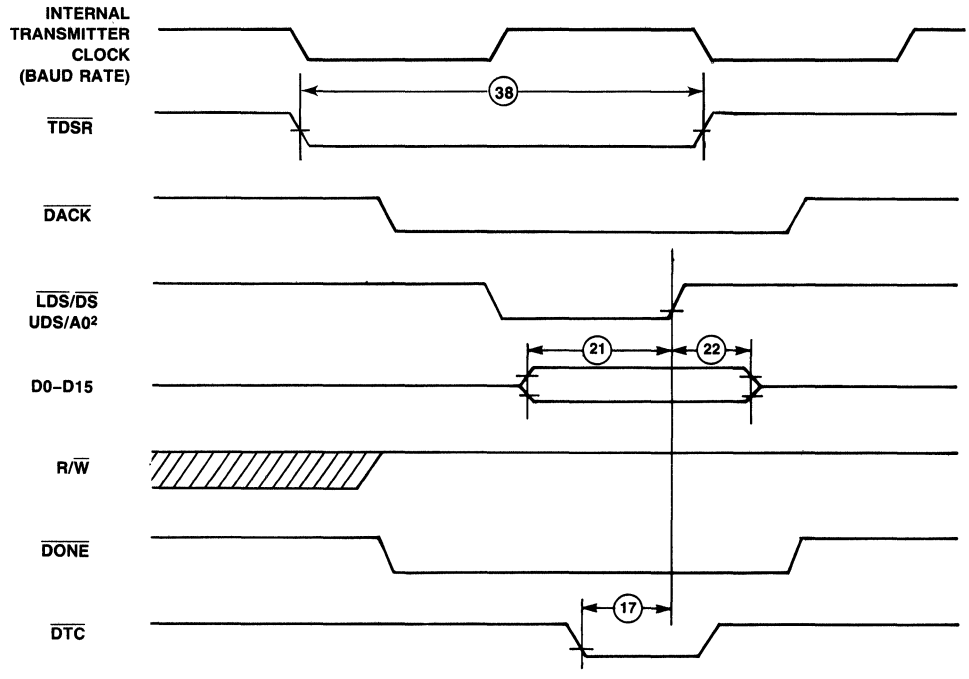
NOTES:
1. BYTE MODE WHEN CONNECTED TO A0 ON 68008 BUS.
2. WORD MODE WHEN CONNECTED TO $\overline{UDS}$ ON 68000 BUS.
3. TIMING MEASUREMENTS ARE REFERENCED TO AND FROM A LOW VOLTAGE OF 0.8 VOLTS AND A HIGH VOLTAGE OF 2.0 VOLTS, UNLESS OTHERWISE NOTED.

Figure 13. MPCC Write Cycle Timing



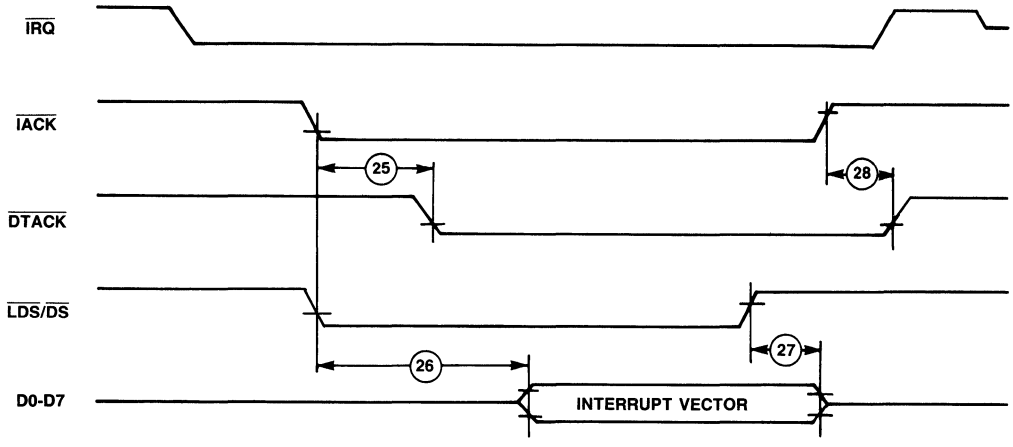
NOTES:
1. TIMING MEASUREMENTS ARE REFERENCED TO AND FROM A LOW VOLTAGE OF 0.8 VOLTS AND A HIGH VOLTAGE OF 2.0 VOLTS UNLESS OTHERWISE NOTED.
2. WORD MODE ONLY.

Figure 14. MPCC to Memory DMA Transfer Cycle Timing (Receiver DMA Mode)



NOTES:
1. TIMING MEASUREMENTS ARE REFERENCED TO AND FROM A LOW VOLTAGE OF 0.8 VOLTS AND A HIGH VOLTAGE OF 2.0 VOLTS UNLESS OTHERWISE NOTED.
2. WORD MODE ONLY.

Figure 15. Memory to MPCC DMA Transfer Cycle Timing (Transmitter DMA Mode)



NOTES:
1. TIMING MEASUREMENTS ARE REFERENCED TO AND FROM A LOW VOLTAGE OF 0.8 VOLTS AND A HIGH VOLTAGE OF 2.0 VOLTS, UNLESS OTHERWISE NOTED.
2. IRQ IS NEGATED WHEN ALL BITS IN STATUS REGISTERS THAT COULD HAVE CAUSED THE INTERRUPT ARE CLEARED.

Figure 16. Interrupt Request Cycle Timing

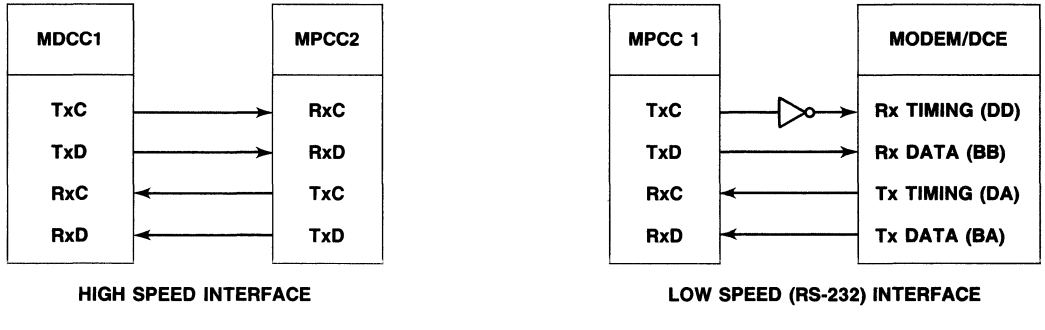


Figure 17. Serial Interface

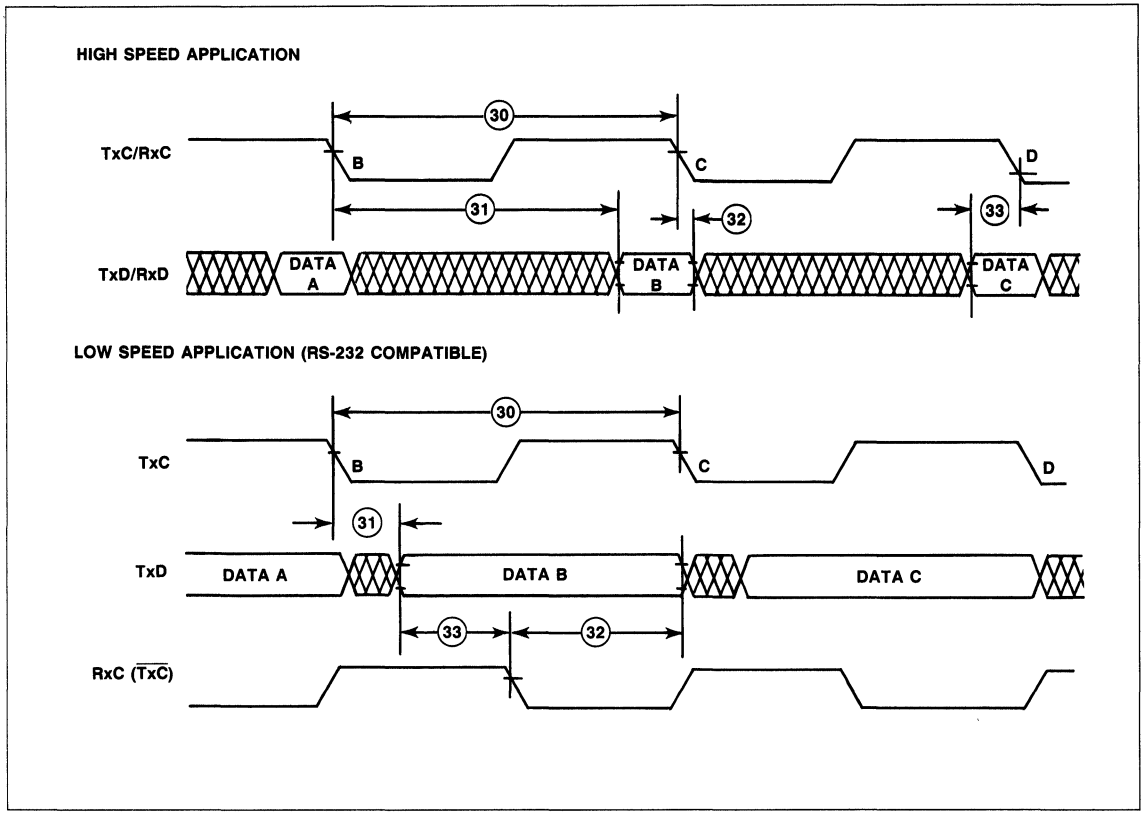


Figure 18. Serial Interface Timing

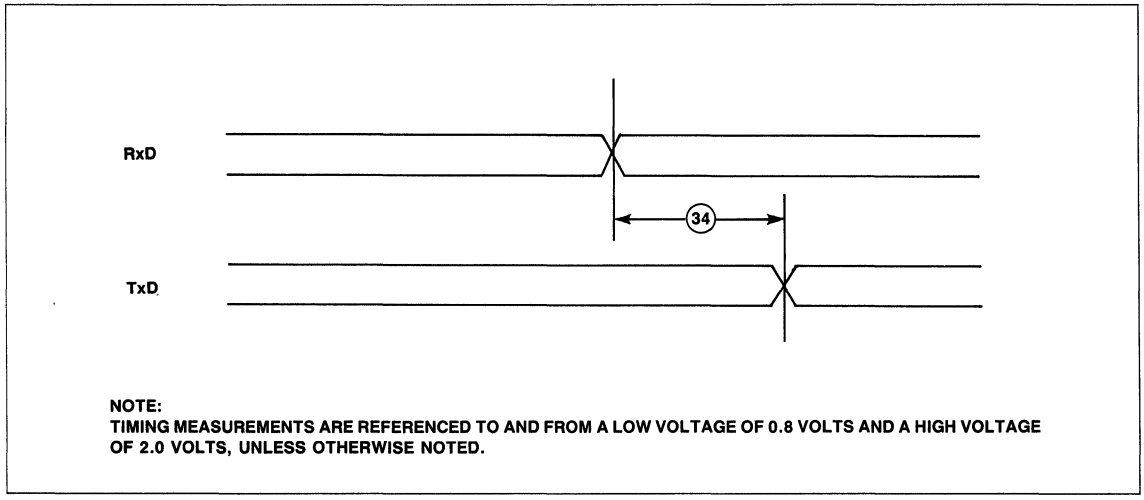


Figure 19. Serial Interface Echo Mode Timing

AC CHARACTERISTICS

(V_{CC} = 5.0 Vdc ±5%, V_{SS} = 0 Vdc, T_A = 0°C to 70°C)

Number	Parameter	Symbol	Min	Max	Unit
1	R/$\overline{W}$ High to $\overline{CS}$, $\overline{DS}$ Low	t_{RHSL}	0	—	ns
2	Address Valid to CS, $\overline{DS}$ Low	t_{AVSL}	30	—	ns
3[1]	$\overline{CS}$ Low to $\overline{DTACK}$ Low	t_{CLDAL}	0	60	ns
4[1]	$\overline{CS}$, $\overline{DS}$ Low to Data Valid	t_{SLDV}	0	140	ns
5	$\overline{CS}$, $\overline{DS}$ High to Data Invalid	t_{SHDXR}	10	150	ns
6	$\overline{CS}$, $\overline{DS}$ High to $\overline{DTACK}$ High	t_{SHDAT}	0	40	ns
7	$\overline{CS}$, $\overline{DS}$ High to Address Invalid	t_{SHAI}	20	—	ns
8	$\overline{CS}$, $\overline{DS}$ High to R/$\overline{W}$ Low	t_{SHRL}	20	—	ns
9	R/$\overline{W}$ Low to $\overline{CS}$, $\overline{DS}$ Low	t_{RLSL}	0	—	ns
10	$\overline{CS}$ High, $\overline{DS}$ High to R/$\overline{W}$ High	t_{SHRH}	20	—	ns
11	Data Valid to $\overline{CS}$, $\overline{DS}$ High	t_{DVSH}	60	—	ns
12	$\overline{CS}$, $\overline{DS}$ High to Data Invalid	t_{SHDXW}	0	—	ns
17	$\overline{DTC}$ Low to $\overline{DS}$ High	t_{CLSH}	60	—	ns
18	$\overline{DACK}$ Low to Data Valid, $\overline{DONE}$ Low	t_{ALDV}	0	140	ns
19	$\overline{DS}$ High to Data Invalid	t_{SHDXDR}	10	150	ns
21	Data Valid to $\overline{DS}$ High	t_{DVSH}	60	—	ns
22	$\overline{DS}$ High to Data Invalid	t_{SHDXDW}	0	—	ns
25	$\overline{IACK}$ Low to $\overline{DTACK}$ Low	t_{IALAL}	0	40	ns
26	$\overline{IACK}$, $\overline{DS}$ Low to Data Valid	t_{IALDV}	0	140	ns
27	$\overline{DS}$ High to Data Invalid	t_{ISHDI}	10	150	ns
28	$\overline{IACK}$ High to $\overline{DTACK}$ High	t_{IAHDAT}	0	40	ns
30	RxC and TxC Period	t_{CP}	248	—	ns
31	TxC Low to TxD Delay	t_{TCLTD}	0	200	ns
32	RxC Low to RxD Transition (Hold)	t_{RCLRD}	0	—	ns
33	RxD Transition to RxC Low (Setup)	t_{RDRCL}	30	—	ns
34	RxD to TxD Delay (Echo Mode)	t_{RDTD}	—	200	ns
35	R/$\overline{W}$ Low to $\overline{DTACK}$ Low (Setup)	t_{RLAL}	0	—	ns
36	$\overline{DACK}$ High to $\overline{DONE}$ High	t_{AHDH}	0	—	ns
37[2, 3]	$\overline{RDSR}$ Pulse Width	t_{RPW}	1	—	clock period
38[2, 4]	$\overline{TDSR}$ Pulse Width	t_{TPW}	1	—	clock period

Notes:

1. For read cycle timing, the MPCC asserts $\overline{DTACK}$ within the MPU S4 clock low setup time requirement and establishes valid data (Data In) within the MPU S6 clock low setup time requirement.
2. For synchronous protocols, this is one full serial clock period of RxC for $\overline{RDSR}$ and TxC for $\overline{TDSR}$.
3. For asynchronous protocols, $\overline{RDSR}$ is asserted for two system clock periods for a prescale factor of 2 and for three system clock periods for a prescale factor of 3.
4. For asynchronous protocols, $\overline{TDSR}$ is asserted for a period of one-half the baud rate.

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to +7.0	V
Input Voltage	V_{IN}	−0.3 to +7.0	V
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature	T_{STG}	−55 to +150	°C

***NOTE:** Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in other sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL CHARACTERISTICS

Parameter	Symbol	Value	Rating
Thermal Resistance	θ_{JA}		°C/W
Ceramic		50	
Plastic		68	

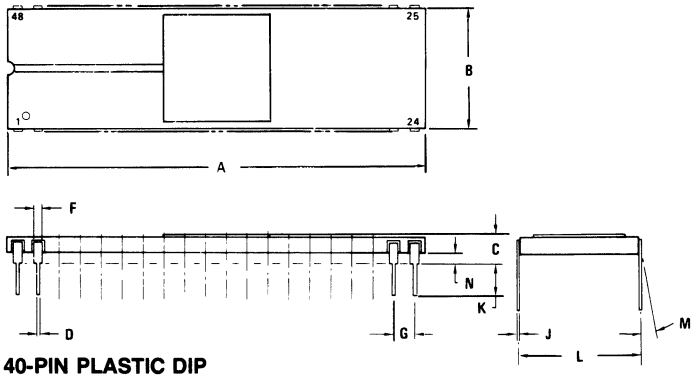
DC CHARACTERISTICS

(V_{CC} = 5.0 Vdc ±5%, V_{SS} = 0 Vdc, T_A = 0°C to 70°C unless otherwise noted)

Parameter	Symbol	Min	Max	Unit	Test Conditions
Input High Voltage All Inputs	V_{IH}	2.0	V_{CC}	V	
Input Low Voltage All Inputs	V_{IL}	−0 3	+0 8	V	
Input Leakage Current R/$\overline{W}$, $\overline{RESET}$, $\overline{CS}$	I_{IN}	—	10.0	μA	V_{IN} = 0 to 5.25V V_{CC} = 5 25V
Three-State (Off State) Input Current $\overline{IRQ}$, $\overline{DTACK}$, D0-D15	T_{TSI}	—	10.0	μA	V_{IN} = 0.4 to 2.4V V_{CC} = 5 25V
Output High Voltage $\overline{RDSR}$, $\overline{TDSR}$, $\overline{IRQ}$, $\overline{DTACK}$, D0-D15, $\overline{DSR}$, $\overline{DTR}$, $\overline{RTS}$, TxD, TxC	V_{OH}	V_{SS} + 2.4	—	V	V_{CC} = 4 75V I_{LOAD} = −400μA C_{LOAD} = 130 pF
BCLK	V_{OH}	V_{SS} + 2 4	—	V	V_{CC} = 4 75V I_{LOAD} = 0 C_{LOAD} = 30 pF
Output Low Voltage $\overline{RDSR}$, $\overline{TDSR}$, $\overline{IRQ}$, $\overline{DTACK}$ D0-D15, $\overline{DSR}$, $\overline{DTR}$, $\overline{RTS}$, TxD, TxC, BCLK,	V_{OL}	—	0.5	V	V_{CC} = 4.75V I_{LOAD} = 3.2 mA
$\overline{DONE}$					V_{CC} = 4 75V I_{LOAD} = 8.8 mA
Internal Power Dissipation	P_{INT}	—	1	W	T_A = 25°C
Input Capacitance	C_{IN}	—	13	pF	V_{IN} = 0V T_A = 25°C f = 1 MHz

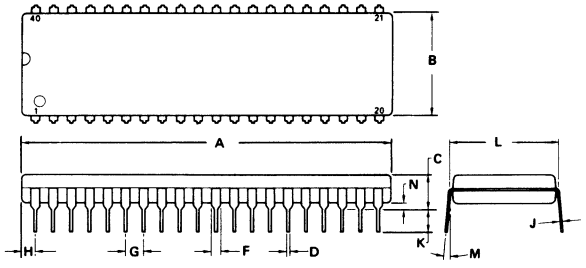
PACKAGE DIMENSIONS

48-PIN CERAMIC DIP



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	60 35	61 57	2 376	2 424
B	14 63	15 34	0 576	0 604
C	3 05	4 32	0 120	0 160
D	0 381	0 533	0 015	0 021
F	0 762	1 397	0 030	0 055
G	2 54 BSC		0 100 BSC	
J	0 203	0 330	0 008	0 013
K	2 54	4 19	0 100	0 165
L	14 99	15 65	0 590	0 616
M	0°	10°	0°	10°
N	1 016	1 524	0 040	0 606

40-PIN PLASTIC DIP



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	51 28	52 32	2 040	2 060
B	13 72	14 22	0 540	0 560
C	3 55	5 08	0 140	0 200
D	0 36	0 51	0 014	0 020
F	1 02	1 52	0 040	0 060
G	2 54 BSC		0 100 BSC	
H	1 65	2 16	0 065	0 085
J	0 20	0 30	0 008	0 012
K	3 05	3 56	0 120	0 140
L	15 24 BSC		0 600 BSC	
M	7°	10°	7°	10°
N	0 51	1 02	0 020	0 040

Rockwell

R68802
LOCAL NETWORK CONTROLLER (LNET)

PRELIMINARY

DESCRIPTION

The R68802* Local Network Controller (LNET) implements the IEEE 802.3 CSMA/CD Access Method local network standard. More generally, it is designed to support a variety of local network designs with varying performance requirements.

The basic function of the LNET is to execute the CSMA/CD algorithm, perform parallel-to-serial and serial-to-parallel conversions of the 10M bps packet data stream, and assemble and disassemble the packet format. In addition, the LNET provides the necessary asynchronous handshake signals to the 68000 family processors, the required DMA interfaces, and the proper interface to the Manchester Interface (MI) component(s) used to connect the LNET to an IEEE 802.3 defined Media Attachment Unit (MAU).

The controller can interface data terminal equipment to local networks with differing performance requirements. At the high end, the R68802 meets the IEEE 802.3 10M bps specification and supports the implementation of ISO layers one and two. For low cost networks, the controller can be run at greatly reduced data rates and inexpensive system components (drivers, cables, etc.) may be selected.

The LNET controller implements a protocol known as Carrier Sense Multiple Access with Collision Detection (CSMA/CD), which allows multiple Data Terminal Equipment to share the same communication medium without the need for a central arbiter of medium utilization.

Ethernet nodes needing to transmit wait exactly 9.6 μs before transmitting data to provide recovery time for other controllers and the cable itself. If a collision with another station is detected, the transmission is aborted and a jam signal transmitted to alert other nodes. Following a jam, the station waits a random amount of time based on a Binary Exponential Back-off algorithm before retransmitting. Repeated collisions result in repeated retries and an increase in the randomly selected time interval to improve trafficking.

ORDERING INFORMATION

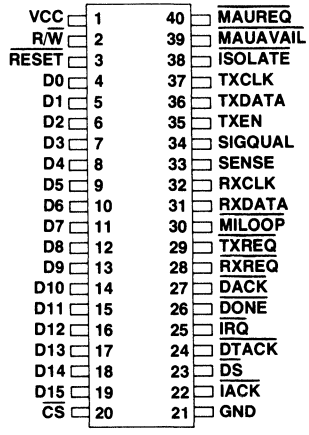
Part Number
R68802_ Temperature Range: 0°C to 70°C
Package:
C = Ceramic
P = Plastic

FEATURES

- Serial data rates as high as 10M bps
- Compatible with a variety of 8- or 16-bit processors and DMA controllers
- Meets the IEEE 802.3 (as well as Ethernet*) specifications for local networks
- Interfaces to SEEQ 8002 Manchester Code Converter (MCC)
- Programmable interframe wait times for smaller topologies and lower data rates
- CSMA/CD algorithm:
  - —Wait before transmit
  - —Jam on collision
  - —Binary exponential backoff
- Programmable 2- or 6-byte address recognition
- Supports three modes of node self-test
- Programmable disable on reception
- 32-bit CRC generation and reception
- Broadband applications
- TTL compatible I/O
- 40-pin DIP
- Single 5V power supply

R68802 is a trademark of the Rockwell International Corporation

Ethernet is a trademark of the Xerox Corporation



R68802 Pin Assignments

Document No. 68650N07

Product Description Order No. 706
Rev. 2 January 1984

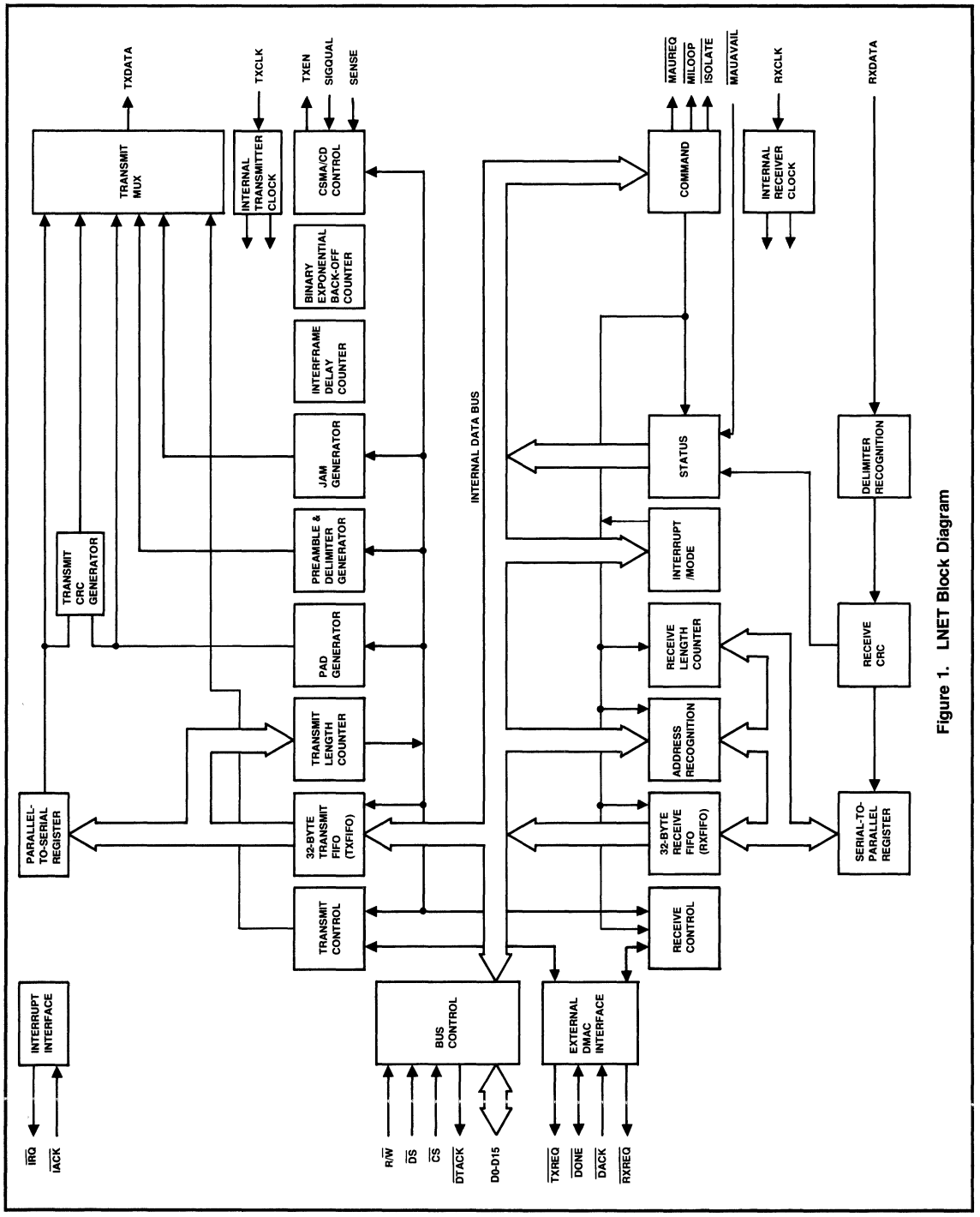


Figure 1. LNET Block Diagram

PIN DESCRIPTION

Throughout the document, signals are presented using the terms active and inactive or asserted and negated independent of whether the signal is active in the high-voltage state or low-voltage state. (The active state of each logic pin is described below.) Active low signals are denoted by a superscript bar. R/$\overline{W}$ indicates a write is active low and a read active high.

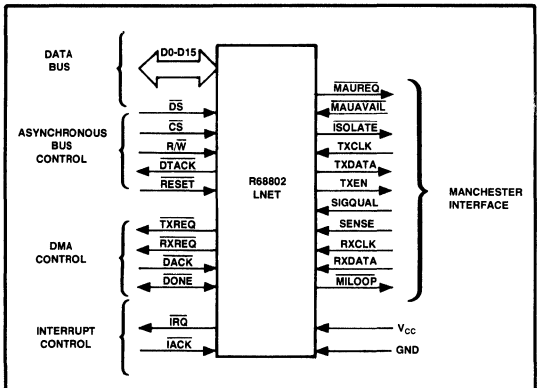


Figure 2. LNET Input and Output Signals

D0-D15—Data Lines. The bidirectional data lines transfer data between the LNET and the MPU, memory or other peripheral device. D0-D15 are used when connected to the 16-bit 68000 bus and operating in the word mode. D0-D7 are used when connected to the 16-bit 68000 bus or the 8-bit 68008 bus and operating in the byte mode. The data bus is tri-stated when $\overline{CS}$ is inactive. (See exceptions in DMA mode.)

$\overline{CS}$—Chip Select. $\overline{CS}$ low selects the LNET for programmed transfers with the host. The LNET is deselected when the $\overline{CS}$ input is inactive in non-DMA mode. $\overline{CS}$ must be decoded from the address bus and gated with address strobe ($\overline{AS}$).

R/$\overline{W}$—Read/Write. R/$\overline{W}$ controls the direction of data flow through the bidirectional data bus by indicating that the current bus cycle is a read (high) or write (low) cycle.

$\overline{DTACK}$—Data Transfer Acknowledge. $\overline{DTACK}$ is an active low output that signals the completion of the bus cycle. During read or interrupt acknowledge cycles, $\overline{DTACK}$ is asserted by the LNET after data has been provided on the data bus; during write cycles it is asserted after data has been accepted at the data bus. A pull up resistor is required to maintain $\overline{DTACK}$ high between bus cycles.

$\overline{DS}$—Data Strobe. During a write (R/$\overline{W}$ low), the $\overline{DS}$ positive transition latches data from the external data bus lines into the LNET. During a read (R/$\overline{W}$ high), $\overline{DS}$ low enables data from the LNET onto data bus lines.

$\overline{IRQ}$—Interrupt Request. The active low $\overline{IRQ}$ output requests interrupt service by the MPU.

$\overline{IACK}$—Interrupt Acknowledge. The active low $\overline{IACK}$ input indicates that the current bus cycle is an interrupt acknowledge cycle. When $\overline{IACK}$ is asserted the LNET places an interrupt vector on the lower byte (D0-D7) of the data bus.

$\overline{DACK}$—DMA Acknowledge. The $\overline{DACK}$ low input indicates that the data bus has been acquired by the DMAC and that the requested bus cycle is beginning.

$\overline{DONE}$—Done. $\overline{DONE}$ is a bidirectional active low signal. The $\overline{DONE}$ signal is asserted by the DMAC when the DMA transfer count is exhausted and there is no more data to be transferred, or is asserted by the LNET when either the last byte of receive data is transferred or a collision is detected during a transmission.

$\overline{RESET}$—Reset. The active low, high impedance $\overline{RESET}$ input initializes all LNET functions. $\overline{RESET}$ must be asserted for at least 500 TXCLKs to initialize the LNET.

$\overline{RXREQ}$—Receive DMA Request. When receive data becomes available in the RXFIFO, $\overline{RXREQ}$ output is asserted and held low for 16 (single address burst mode) DMAC cycles (16 sequential $\overline{DACK}$ pulses) or until the end of the receive block. When the last data byte of the receive block is transferred, $\overline{DONE}$ is asserted by the LNET with the last $\overline{DACK}$ strobe and the negation of $\overline{RXREQ}$.

$\overline{TXREQ}$—Transmit DMA Request. When the Transmitter Enable bit is set in Command Register 1, $\overline{TXREQ}$ output is asserted and held low for 16 (single address burst mode) DMAC cycles (16 sequential $\overline{DACK}$ pulses) or until the end of the transmit data block as signaled by the DMAC's assertion of $\overline{DONE}$.

$\overline{MILOOP}$—MI Loopback. With an active $\overline{MILOOP}$ output, the MI shunts its LNET data-in path to its LNET data-out path, effectively routing the LNET TXDATA output into the LNET RXDATA input.

RXDATA—Receive Data. The LNET receives serial data via the RXDATA input. The RXDATA input is shifted into the receiver on the positive going edge of RXCLK.

RXCLK—Receive Clock. The free-running Receive Clock provides the LNET with received data timing information. The positive (low-to-high) clock transition enables an RXDATA bit into the LNET.

SENSE—Carrier Sense. The active high SENSE input indicates the presence of data on the RXDATA serial input line.

SIGQUAL—Signal Quality. The assertion of the active high SIGQUAL input by the MI indicates an error condition on the medium. During the transmission mode the LNET interprets this as a collision.

TXEN—Transmit Enable. The active high TXEN output indicates to the MI that data is present on the TXDATA output.

TXDATA—Transmit Data. The LNET transmits serial data on the TXDATA line. The TXDATA output changes on the positive going edge of TXCLK.

TXCLK—Transmit Clock. The Transmit Clock input is a free-running clock supplied by the MI that provides both a system clock and a means of shifting out serial data bit on the TXDATA output line.

$\overline{\text{ISOLATE}}$—Isolate MAU. The active low $\overline{\text{ISOLATE}}$ output is asserted when the Isolate bit in Command Register 1 is set to 1 to isolate the MAU from the medium. As long as $\overline{\text{ISOLATE}}$ is low, the MAU is unable to transmit or receive on the medium.

$\overline{\text{MAUAVAIL}}$—MAU Available. When the active low $\overline{\text{MAUAVAIL}}$ input is asserted, the transmission algorithm can proceed.

$\overline{\text{MAUREQ}}$—MAU Request. The active low $\overline{\text{MAUREQ}}$ output is asserted prior to transmission if $\overline{\text{MAUAVAIL}}$ is not asserted.

V_{CC}—Power. 5 V ± 5%.

GND—Ground. Ground.

LNET REGISTERS

The LNET contains three groups of registers accessible from the MPU bus which initialize the LNET, control and monitor LNET operation, and transfer data between the LNET and the MPU bus. These register groups, specific registers within each group, and the size, access and mode of each register are listed in Table 1.

All registers, except the Mode Register, may be accessed either in the word or byte mode, depending on the MPU data bus length (8-bit or 16-bit) and the Word/Byte mode selected in bit 4 of the Mode Register during initialization. In the word mode, two registers are read or written during one cycle with the least significant byte (D0-D7) accessed first.

INITIALIZATION REGISTERS

The initialization registers contain command information to configure the LNET for normal operation. The registers are the one-byte Mode Register (MR), the one-byte Interrupt Vector Number Register (IVNR) and the two- or six-byte Station Address Register (SAR). These registers must be loaded upon $\overline{\text{RESET}}$ (either caused by power up or initiated during normal operation) or upon setting of the $\overline{\text{RESET}}$ bit in Command Register 1. Any of these conditions reset the LNET by clearing the Mode Register, Station Address Register, Command Registers and Status Registers. The Interrupt Vector Number Register is auto-initialized to its default value of $0F.

All initialization registers must be written to by the MPU instruction sequence immediately after a reset in the manner decribed below even if no data is changed in a register. The number of bytes written depends upon the number of bytes in the Station Address as selected in bit 4 of the Mode Register.

After the proper number of write cycles have been completed, the LNET Initialized bit in Status Register 1 is set and further MPU writes to the LNET will address only Command Register 1 or Command Register 2. All MPU reads of the LNET after initialization is complete will access only Status Register 1 or Status Register 2.

Initialization Procedure for 16-Bit MPU Bus

Write cycle 1—write the Mode byte on the lower byte of the data bus D0-D7. The upper byte is not used and can contain any data.

Write cycle 2—write the Interrupt Vector Number on the lower byte of the data bus D0-D7. The upper byte is not used and can contain any data.

Write cycle 3 or write cycles 3 through 5—write the one- or three-word Station Address (depending on the Station Address Size loaded into the Mode Register), least significant words first.

Table 1. LNET MPU Bus Accessible Registers

Register Group	Register Name	Size (No. Bytes)	Access	Reset Value	Mode
Initialization Registers	Mode Register (MR)	1	$\overline{CS}$ = L, R/$\overline{W}$ = L (write one byte[1])	$00	MPU Write
	Interrupt Vector Number Register (IVNR)	1	$\overline{CS}$ = L, R/$\overline{W}$ = L (write one byte[2])	$0F	
	Station Address Register (SAR)	2 or 6	$\overline{CS}$ = L, R/$\overline{W}$ = L (write 1 or 3 sequential words or 2 or 6 sequential bytes)	$00	
Operating Registers	Command Register 1 (CR1) Command Register 2 (CR2)	1 1	$\overline{CS}$ = L, R/$\overline{W}$ = L	$00	MPU Write
	Status Register 1 (SR1) Status Register 2 (SR2)	1 1	$\overline{CS}$ = L, R/$\overline{W}$ = H	$00	MPU Read
Data Buffers	Transmit FIFO Register File (TXFIFO)	32	$\overline{TXREQ}$ = L	$XX	DMA Write
	Receive FIFO Register File (RXFIFO)	32	$\overline{RXREQ}$ = L	$XX	DMA Read

Notes:
1. Second byte of word ignored.
2. Second byte in word mode ignored.

Initialization Procedure for 8-Bit MPU Bus

Write cycle 1—write the Mode byte on the data bus.

Write cycle 2—write the Interrupt Vector Number on the data bus.

Write cycles 3 through 4 or 3 through 8—write the two- or six-byte Station Address (depending on the Station Address Size loaded into the Mode Register), least significant bytes first.

Mode Register (MR)

7 6 5	4	3	2	1	0
IFWT	BYTE	INTCOL	DISRX	NOLC	SAS

The Mode Register sets conditions during initialization for use during normal operations. It must be the first byte written during initialization. All mode bits are active high, i.e., = 1. All bits are cleared upon RESET or setting the RESET bit to 1 in Command Register 1.

MR IFWT —Interframe Wait Time

7-5	No. of TXCLKs
000	16
001	32
010	48
011	64
100	80
101	96
110	112
111	128

MR
4 BYTE —Data Bus Byte Mode
0 Select word mode (for use with 16-bit MPU bus).
1 Select byte mode (for use with 8-bit MPU bus).

MR
3 INTCOL —Interrupt on Collision
0 Assert only DONE on collision.
1 Assert IRQ and DONE on collision.

MR
2 DISRX —Disable Receiver
0 Enable receiver after each packet reception.
1 Disable receiver after each packet reception.

MR
1 NOLC —No Length Count
0 Use length count in packet format.
1 Do not use length count in packet format.

MR
0 SAS —Station Address Size
0 6-byte station address.
1 2-byte station address.

Interrupt Vector Number Register (IVNR)

7	6	5	4	3	2	1	0
Interrupt Vector Number (IVN)							

If an interrupt condition occurs (as reported by bits in Status Register 1 and Status Register 2), IRQ is asserted to request MPU interrupt service. Upon IACK input assertion, the Interrupt Vector Number (IVN) from the Interrupt Vector Number Register (IVNR) is placed on the data bus (D0-D7). The IVN must be the second byte initialized during LNET initialization. The IVN is set to $0F upon RESET or setting the RESET bit to 1 in Command Register 1.

Station Address Register (SAR)

7	6	5	4	3	2	1	0
Station Address							

The Station Address Register holds the Station Address for the Receiver Address Recognition circuitry. The Station Address bytes must be written to the LNET following the Interrupt Vector Number during the initialization sequence. Either two or six bytes must be written, least significant bytes first, depending on the Station Address Size loaded into the Mode Register.

OPERATING REGISTERS

The command or status registers are addressed during an MPU write or read, respectively, after initialization is complete as indicated by the LNET Initialized bit in Status Register 1. In word mode, both command registers are written during one write cycle. Command Register 1 occupies the lower byte of the word. Likewise, while reading the status registers in word mode, Status Register 1 occupies the lower byte of the word.

COMMAND REGISTERS

Command Register 1 (CR1)

Command Register 1 controls the operation of the LNET. All command bits are active high (i.e., = 1).

7	6	5	4	3	2	1	0
RESET	ENRX	RECALL	NOISOL	MILOOP	INLOOP	ODDND	ENMAU

CR1
7 RESET —Reset
0 Enable LNET operation.
1 Reset LNET.

Note: The RESET bit is automatically cleared to 0 upon the completion of the reset sequence. This bit is unaffected by the RESET pin level.

CR1
6 ENRX —Enable Receiver after Packet Reception
0 Disable receiver after packet reception.
1 Enable receiver after packet reception. This bit must be set after each packet is received to enable reception of the next packet only if bit 2 in the Mode Register is set at initialization. Reception of the packet clears this bit.

Note: This bit is not used if bit 2 in the Mode Register is not set at intitialization.

CR1
5 RECALL—Receive All Packets
0 Receive only addressed packets. The address must correspond to the Station Address loaded into the Station Address Register upon initialization.
1 Receive all packets (regardless of address).

CR1
4 NOISOL —No Isolate
0 Assert $\overline{\text{ISOLATE}}$ to the MI to request that the MAU isolate itself from the medium.
1 Negate $\overline{\text{ISOLATE}}$ to the MI to request that the MAU connect itself to the medium.

CR1
3 MILOOP—Manchester Interface Loopback Test
0 Negate $\overline{\text{MILOOP}}$ to command MI normal operation.
1 Assert $\overline{\text{MILOOP}}$ to command MI loopback operation.

CR1
2 INLOOP—Internal LNET Loopback Test
0 Enable LNET normal operation.
1 Enable LNET internal loopback operation.

CR1
1 ODDNO —Odd Number of Bytes
0 Transmit even number of bytes in a block.
1 Transmit odd number of bytes in a block.

CR1
0 ENMAU —Enable $\overline{\text{MAUREQ}}$
0 Negate $\overline{\text{MAUREQ}}$.
1 Assert $\overline{\text{MAUREQ}}$.

Command Register 2 (CR2)

7	6	5	4	3	2	1	0
Reserved for future use							

This register not presently in use. When programming, $00 should be written to CR2 to assure future software compatibility. In byte mode, $00 must be written to this register following the Command Register 1 write cycle.

STATUS REGISTERS

The two interrupt driven status registers report the status of the LNET receiver and transmitter operations. Status registers cannot be polled, they can *only* be read upon interrupt service by the MPU. Status is reported in either discrete or encoded bits. All discrete (or non-encoded) status bits are active high (i.e., = 1).

A change in any of these status bits causes IRQ to be asserted (except as noted). Reading of the status registers resets the individual bit or encoded field that caused the IRQ assertion and negates IRQ (except as noted). In the byte mode, both status registers must be read in consecutive read cycles.

Status Register 1 (SR1)

7	6 5 4	3	2 1 0
HRTBT	TXSTAT	ODD	RXSTAT

SR1
7 HRTBT —Heartbeat Absent
0 Heartbeat present.
1 Heartbeat absent (part of the transmission algorithm is to listen for the heartbeat before posting transmit status. Set concurrent with the transmitter status field.). The Heartbeat test checks the collision detection circuitry by listening for a "ping" within seven TXCLKs after the end of a transmission).

SR1
6-4 TXSTAT —Transmitter Status
000 Transmitter idle.
001 Transmit successful.
010 Collision (Assertion of SIGQUAL within the first 512 bit times causes $\overline{\text{DONE}}$, or $\overline{\text{DONE}}$ and $\overline{\text{IRQ}}$, to be asserted depending on the state of MR bit 3).
011 Signal Quality error (SIGQUAL asserted after the first 512 bit times).
100 Transmit retry count exceeded.
101 Transmit buffer underflow during transmission (indicates the TXFIFO emptied between the 16th data byte delivered for transmission and the assertion of $\overline{\text{DONE}}$).
110 Transmit in progress (indicates the real time activity of the TXDATA pin. This state does not set the $\overline{\text{IRQ}}$ bit in SR2 nor cause $\overline{\text{IRQ}}$ to be asserted. This bit pattern is not reset to the transmitter idle pattern upon reading SR1.
111 $\overline{\text{MAUAVAIL}}$ changed state during transmission.

SR1
3 ODD —Odd Number of Receive Bytes
0 Even number of bytes in the receive packet.
1 Odd number of bytes in the receive packet.

SR1
2-0 RXSTAT —Receiver Status
000 Receiver idle.
001 Receive successful.
010 Minimum packet size error.
011 Receive buffer overflow.
100 Frame terminated on a non-byte boundary error.
101 Frame Check Sequence (FCS) error.
110 Receive in progress (indicates a valid address has been recognized and $\overline{\text{DONE}}$ has not been asserted. This state does not set the IRQ bit in SR2 nor cause $\overline{\text{IRQ}}$ to be asserted. This bit pattern is not reset to the receiver idle pattern upon reading SR1.
111 Reserved

Status Register 2 (SR2)

7	6	5	4	3	2	1	0
IRQ	0	INIT	MAUAVAIL	COLCNT			

SR2
7 IRQ —Interrupt Request
0 An interrupt condition has not occurred and $\overline{IRQ}$ has not been asserted.
1 An interrupt condition has occurred and $\overline{IRQ}$ has been asserted.

Note: This bit is cleared when SR2 is read and there is no pending interrupt condition.

SR2
6 —Not used
0 Always reads zero.

SR2
5 INIT —LNET Initialized
0 LNET initialization not complete.
1 LNET initialization complete (set after the last station address byte has been written).

Note: This bit is cleared upon $\overline{RESET}$ or RESET bit set in Command Register 1.

SR2
4 MAUAVAIL—MAU Available
0 MAU is not available.
1 MAU is available.

Note: This bit is not cleared when SR2 is read.

SR2
3-0 COLCNT—Collision Count
0000 Zero
.
.
.
1111 Fifteen

Note: Reset to zero when the enable $\overline{MAUREQ}$ bit is set in CR1. If Mode Register bit 3 is negated the changing count does not generate IRQ interrupts.

TRANSMIT DATA BUFFER (TXFIFO)

The Transmit data buffer is a 32-byte FIFO register file (TXFIFO) which can be loaded only by DMA service. One half of the TXFIFO loads data for transmission via the DMAC; the other half holds data currently being transmitted out serially on TXDATA. When the transmitting half is empty it becomes the loading half and the current loading buffer becomes the transmitting half. If the transmitting buffer empties before the loading buffer is fully loaded, $\overline{IRQ}$ is asserted and the transmitter buffer underflow bit pattern (101) is set in Status Register 1.

The time required to load half the transmitter buffer under DMAC control must be less than the time it takes to serialize out the transmitting half on TXDATA. From the assertion of $\overline{TXREQ}$ to the end of the 16th DMAC bus cycle, no more than 128 TXCLKs can elapse.

RECEIVE DATA BUFFER (RXFIFO)

The Receive data buffer is a 32-byte FIFO register file (RXFIFO) which can be read only during DMA service. One half of the RXFIFO is a receiving buffer for the data from the Serial-to-Parallel Register; the other half is a reading buffer for the data ready to be transferred to the MPU bus. As soon as the receiving buffer is full, these two halves switched roles. If the receiving buffer is fully loaded before the reading buffer is empty, $\overline{IRQ}$ is asserted and the receive buffer overflow bit pattern (011) is set in Status Register 1.

The time it takes to unload the reading buffer under DMAC control must be less than the time it takes to load the receiving buffer from RXDATA. The loading time is 128 RXCLKs.

INPUT/OUTPUT FUNCTIONS

In addition to being directly compatible with the 68000 and the 68008 MPU's, the LNET supports DMA transfers when used with the 68440, 68450, AMZ9516, or AMZ8016 DMA controller. The LNET also provides the necessary synchronous signals for interfacing to the Manchester Interface device.

MPU INTERFACE

Transfer of data between the LNET and the system bus involves the following signals: Data Bus D0 through D15 and control singals consisting of R/$\overline{W}$, $\overline{DTACK}$, $\overline{CS}$, $\overline{IACK}$, and $\overline{DS}$.

16-Bit MPU Interface

When connecting the LNET to the 16-bit 68000 MPU data bus, the LNET $\overline{DS}$ input is connected to the bus $\overline{LDS}$ line and the LNET D0-D15 data lines are connected to the bus D0-D15 data lines (see Figure 4).

Bit 4 in the Mode Register, left in its default value of 0 during initialization, selects the word mode. In the word mode, a read of both status registers performed with one word read cycle transfers Status Register 1 on D0-D7 and Status Register 2 on D8-D15. A write to the command registers is also accomplished in one cycle which transfers Command Register 1 on D0-D7 and Command Register 2 on D8-D15.

8-Bit MPU Interface

When connecting the LNET to the 8-bit 68008 MPU data bus, the $\overline{DS}$ input is connected to the bus $\overline{DS}$ line and the LNET D0-D7 data lines are connected to the bus D0-D7 data lines (see Figure 5).

Bit 4 of the Mode Register set to 1 during initialization selects byte mode. In the byte mode, reading of the status registers is performed with two consecutive byte read cycles to enable first Status Register 1 and then Status Register 2 onto D0-D7. Writing to the command registers also requires two consecutive byte write cycles with Command Register 1 transferred first followed by Command Register 2.

Read/Write Operation

The R/$\overline{W}$ input controls the direction of data flow on the data bus. $\overline{CS}$ (Chip Select) enables the LNET for access to the internal registers and other operations. When $\overline{CS}$ is asserted the data I/O buffer acts as an output driver during a read operation, and as an input buffer during a write operation. $\overline{CS}$ must be decoded from the address bus and gated with address strobe ($\overline{AS}$).

If the LNET is selected ($\overline{CS}$ = low) for a read (R/$\overline{W}$ = high), data is placed on the data bus from the status register when the $\overline{DS}$ is asserted. The LNET asserts Data Transfer Acknowledge ($\overline{DTACK}$) concurrent with the output data.

If the LNET is selected ($\overline{CS}$ = low) for a write (R/$\overline{W}$ = low), $\overline{DS}$ strobes data into the selected register and the LNET asserts $\overline{DTACK}$ immediately after $\overline{DS}$ is asserted.

DMA INTERFACE

During receiving or transmitting data from the MPU bus, the LNET asserts a receive or transmit request ($\overline{RXREQ}$ or $\overline{TXREQ}$) to the DMAC. A DMA acknowledge ($\overline{DACK}$) signal is asserted in response to $\overline{RXREQ}$ or $\overline{TXREQ}$ when the DMAC is ready to service the request. Both receive request and transmit request share the same $\overline{DACK}$ pin; therefore, in the case of DMAC devices with a $\overline{DACK}$ for each channel, they must be ORed together externally.

Transmit DMA Request

In servicing the $\overline{TXREQ}$, the DMAC writes to the TXFIFO a byte or a word at a time. The TXFIFO input pointer (TIP) is advanced and data latches on the rising edge of $\overline{DS}$.

Receive DMA Request

In servicing the $\overline{RXREQ}$, the DMAC reads from the RXFIFO a byte or word at a time. Data is enabled out on the falling edge of $\overline{DACK}$ and the RXFIFO output pointer (ROP) is advanced on the rising edge of $\overline{DACK}$. The data lines are tri-stated following the rising edge of $\overline{DACK}$.

$\overline{DONE}$

$\overline{DONE}$ is a bidirectional signal line to or from the DMAC. With the AMZ8016 and the AMZ9516, $\overline{DONE}$ auto-initializes the DMAC back to the start of the packet when a collision occurs during transmission. With the 68440, the $\overline{DONE}$ output is routed to the 68440's PCL input after gating with $\overline{TXREQ}$ line. For the 68450 it is necessary for the MPU to reinitialize the DMAC on collision.

INTERRUPTS

The $\overline{IRQ}$ output asserts when there is status information available after the completion of a transmit or receive transaction. The MPU grants the interrupt by asserting an interrupt acknowledge ($\overline{IACK}$) signal and reads the interrupt vector when the LNET asserts data transfer acknowledge ($\overline{DTACK}$). The subsequent negation of $\overline{IACK}$ and $\overline{IRQ}$ preceed MPU interrupt processing.

MANCHESTER INTERFACE (MI) SIGNALS

The abbreviation MI refers to the Manchester Interface component(s) necessary to interface the LNET to an IEEE 802.3 specified Media Access Unit (MAU).

SENSE (Sense Carrier) Input

The MI asserts SENSE when it has detected a change in Carrier Sense from no carrier present to carrier present. SENSE stays active as long as carrier is present and is negated when the carrier disappears.

$\overline{ISOLATE}$ (Isolate Message Request) Output

The LNET asserts $\overline{ISOLATE}$ to direct the MI to send an Isolate message to the MAU. When $\overline{ISOLATE}$ is negated, the MI sends a Normal message to the MAU unless the LNET requires that the MAU request message be sent to permit data output.

$\overline{MAUREQ}$ (MAU Request) Output

The LNET asserts $\overline{MAUREQ}$ when CR 1 bit 0 is active. $\overline{MAUREQ}$ stays active and a MAU request message is sent until the end of a packet transmission.

$\overline{MAUAVAIL}$ (MAU Available) Input

The MI asserts $\overline{MAUAVAIL}$ when an MAU available message from the MAU is received. $\overline{MAUAVAIL}$ is negated when an MAU not available message is received from the MAU.

SIGQUAL (Signal Quality) Input

SIGQUAL is asserted by MI when a Signal Quality Error Message is received from the MAU.

TXEN (Transmission Enable) Output

The LNET starts a transmission by asserting TXEN and outputs serial data on TXDATA which is Manchester encoded by the MI. TXEN is active until the end of the transmission.

RXCLK (Receive Clock) Input

RXCLK shifts receive data into the LNET and is free running at 10 MHz, or slower.

TXCLK (Transmitter Clock) Input

The TXCLK is a free running 10 MHz, or slower, clock used to clock data into the MI and perform operations in the transmitter.

$\overline{MILOOP}$ (MI Loopback) Output

The $\overline{MILOOP}$ output signals the MI component(s) that the current data is a test frame and it is to be "looped back" to the LNET instead of being sent to the MAU.

LNET FUNCTIONAL DESCRIPTION

The LNET transmits and receives serial data on an IEEE 802.3 CSMA/CD Access Method defined communications medium and transfers parallel data to and from a host system under program or DMA control according to the IEEE 802.3 data link specification.

Frame Format

Serial data transfers synchronously between the LNET and the MI within the frame structure for data communications using local area network media access control (MAC) procedures. Each MAC frame, or packet, consists of eight fields: Preamble, Start Field Delimiter (SFD), Destination Address, Source Address, Length Count, Data, Pad and Frame Check Sequence (FSC). Figure 3 illustrates the frame format.

The Preamble consists of seven bytes of alternating 1's and 0's, i.e., 1010 . . . 1010.

The Start Field Delimiter (SFD) consists of one byte of bit pattern 10101011 immediately following the Preamble pattern which indicates the start of a valid frame.

The Destination and Source Addresses are either two or six bytes in length. Addresses may be any one of the following three types: Station Address, Logical Group, or Broadcast. Logical Group and Broadcast Addresses are identified by a 1 in the first bit position received. The first bit of a Station Address is 0.

The Length Count field is two bytes in length and specifies the Data field length (in an Ethernet application this field is the Type field and the Length Count field in the Mode Register must be initialized appropriately).

The Data field can have a variable number of bytes. If the Data field is less than 46 bytes (in a six-byte address mode), or less than 54 (in a two-byte address mode), pad bytes are added to the frame on transmission to bring the overall packet size up to the minimum size of 72 bytes. The maximum Data field length must be programmed into the DMAC operating with the LNET.

The Frame Check Sequence (FCS) field is four bytes in length.

Frame Reception

The Receiver consists of the following sections: Delimiter Recognition, Receive CRC, Serial-to-Parallel Register, Receive Length Counter, Address Recognition, and a 32-byte FIFO register file (RXFIFO). These registers are all driven or loaded by RXCLK or a derivative.

In the absence of serial input data from the network bus, the SENSE input from the MI is inactive. The Receive Clock (RXCLK) is free running and the Receiver front end is idling.

The assertion of SENSE defines the beginning of a frame. The rising edge of RXCLK enables SENSE and concurrently the first Preamble bit on RXDATA to the LNET. The falling edge of RXCLK shifts the first bit of the Preamble into the Delimiter Recognition logic and SENSE into the SENSE Detection logic. Delimiter Recognition is deferred for eight RXCLKS after the assertion of SENSE, to give the MI unit time to synchronize on the Preamble.

If sequential zeros are detected during the time the LNET is searching for the double ones delimiter, the packet's reception is aborted.

The Preamble bits are shifted through the Delimiter Recognition logic without result. As the last bit of the Delimiter is shifted in, an internal signal is asserted.

The data is then routed to the Receive CRC and the Serial-to-Parallel Register. The Byte Alignment and Odd/Even byte monitor is initialized, and a Byte Counter is started.

At the appropriate byte count, the first byte of Destination Address is converted to parallel data, and compared with the first byte of Station Address and loaded into the RXFIFO.

The RXFIFO Input Pointer (RIP) is then advanced by one. The next byte(s) of destination and source addresses are loaded in the same manner. As the two length count bytes are sent to the RXFIFO they are also loaded into the Length Counter. If this field is non-zero it is decremented on each succeeding byte of the packet.

The remainder of the first 16 bytes of the packet are loaded into the RXFIFO (unless the Length Counter reaches its terminal count or the packet terminates).

With 16 bytes buffered, the RXFIFO is half full. $\overline{\text{RXREQ}}$ is now asserted, the receiving half of the buffer becomes the reading half, and the first 16 bytes of receive data are unloaded by advancing the RXFIFO Output Pointer (ROP) as a function of the DMAC's $\overline{\text{DACK}}$ and $\overline{\text{DS}}$ signals. Meanwhile the empty, receiving half, of the RXFIFO continues to fill.

As the 32nd byte of received data is loaded, $\overline{\text{RXREQ}}$ is asserted again and RIP proceeds to the just emptied reading buffer while DMA bus cycles unload the new reading buffer.

The RXFIFO continues to load and unload in this manner throughout the duration of the packet's Data field.

The position of RIP indicates when to load the Length Counter from the data stream, when to check for a valid address, when to assert or negate $\overline{\text{RXREQ}}$ and to flag an overrun of the receive DMA service.

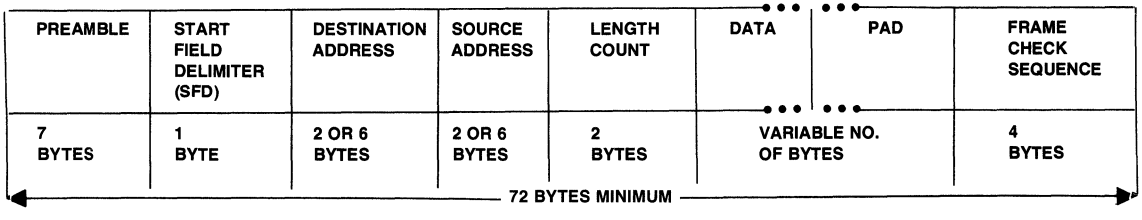


Figure 3. MAC Frame Format

The two-byte Length Counter is located either four or twelve bytes (depending on the address mode) after Valid Delimiter. The Length Counter is decremented every eight RXCLKs. When the Length Counter equals zero, indicating the end of the Data field, RIP is disabled and RXREQ asserts long enough to unload the last bytes.

In the case of a normal termination of the packet, after the last bytes are unloaded, the LNET asserts $\overline{DONE}$ concurrent with the last $\overline{DACK}$ strobe and negates $\overline{RXREQ}$. The CRC Register continues to calculate over the Pad and Frame Check Sequence fields and the Byte Alignment Checker continues to run until packet end. The state of the Odd/Even byte checker is latched at the time of the Length Counter's terminal count.

The end of the packet is recognized as follows. The last FCS bit shifts in as RXCLK goes low in the normal manner. Two RXCLKs later the negated value of SENSE shifts in. At the next rising edge of RXCLK the CRC syndrom is compared and the result is posted to Status Register 1 and $\overline{IRQ}$ is asserted.

If, during the course of a reception, the Data byte count held by the system exceeds the maximum number (1500 bytes for Ethernet), a maximum frame size error is flagged by $\overline{DONE}$ from the DMAC. The LNET responds by negating $\overline{RXREQ}$ and clearing the status registers without generating an $\overline{IRQ}$.

Frame Transmission

The Transmitter consists of the following: Parallel-to-Serial Register, Transmit Length Counter, 32-byte Transmitter FIFO register file (TXFIFO), Transmit CRC Generator, Preamble and Delimiter Generator, Jam Generator, Interframe Delay Counter, and the Binary Exponential Back-Off Counter. These sections are all driven by TXCLK or a derivation.

Frame transmission commences with a MPU write to Command Register 1 setting the Enable $\overline{MAUREQ}$ bit. The LNET responds by asserting Transmit DMA Request ($\overline{TXREQ}$). Under DMA control, 16 bytes are loaded from the MPU bus into the TXFIFO by advancing the TXFIFO Input Pointer (TIP) as a function of $\overline{DACK}$ and DS. The LNET then negates $\overline{TXREQ}$ until the first byte of this data has been serialized out.

While the first 16 bytes are being loaded into the TXFIFO, the LNET is monitoring the SENSE input Upon SENSE negation the Transmitter waits 96 TXCLKS (strict IEEE 802.3 or Ethernet application, otherwise the delay follows whatever is programmed into Mode Register bits 5-7) and then serializes out the first byte of data on TXDATA if the TXFIFO is half full (if it is not half full yet, the LNET returns to monitoring SENSE). If SENSE is active the LNET waits until it is negated and then starts the Interframe Delay Counter.

At the terminal count of the Interframe Delay Counter the first preamble bits are shifted out under TXCLK control and the transmitter begins to monitor the SIGQUAL input. At the same time $\overline{TXREQ}$ is asserted again and another 16-byte data burst is transferred into the empty half of the TXFIFO.

As the TXFIFO Output Pointer (TOP) advances to the first byte of the most recently filled half of the buffer, $\overline{TXREQ}$ is again asserted to reload the half just emptied.

Upon the assertion of the $\overline{DONE}$ input by the DMAC (at the time of the last byte or word transfer), the transmitter finishes serializing the last bytes out, zeros the TXFIFO Input Pointer (TIP) and serializes the contents of the CRC Register out on TXDATA.

If SIGQUAL is asserted by the MI *during* the first 512 TXCLKS, the LNET assumes there has been a collision between its own transmission and that of another node in the network. The response of the LNET at its MI interface is to abort the frame transmission after appending a Jam signal consisting of 48 alternating zeros and ones to it. The Jam signal is sent whenever the LNET has successfully contended for the medium and then has been interrupted in its transmission during the collision window.

DMA TRANSFER MODES

The response of the LNET at its MPU/DMAC interface to a collision is programmable to one of two modes in the Mode Register at initialization.

This allows for the LNET to be used with DMACs of differing capabilities. Specifically, some DMACs need to be reinitialized by the MPU if they are to restart a block transfer that has been aborted by a peripheral's assertion of a $\overline{DONE}$ and an $\overline{IRQ}$. Others are capable of automatically re-starting a block by themselves if a $\overline{DONE}$ is detected during a transfer.

Mode One: Assert $\overline{IRQ}$ plus $\overline{DONE}$ On Collision.

Assertion of SIGQUAL *during* the first 512 TXCLKS after transmission begins sets the collision code (010) in the encoded Transmitter Status field in Status Register 1 and increments the Collision Count field in Status Register 2 by one. Next, $\overline{IRQ}$ is asserted, and the Interrupt Vector Number from the Interrupt Vector Number Register is output on the data bus when $\overline{IACK}$ is asserted.

The MPU processes the interrupt by reading the status registers to determine the cause of the interrupt and to clear the interrupt. The MPU then reinitializes the DMAC and reloads the first 16 bytes of the aborted data packet into the TXFIFO. Meanwhile the LNET is sending the Jam signal followed by a delay interval determined by the Binary Exponential Back-off Counter. At the end of this time interval the LNET begins to transmit the preamble and delimiter again if the TXFIFO has been reloaded with the first 16 bytes of the packet. If the TXFIFO has not been reloaded by the time the Jam signal and the back-off delay interval are over, the LNET will wait for data.

Mode Two: Assert only $\overline{DONE}$ On Collision.

Upon the assertion of SIGQUAL *during* the first 512 TXCLKs, the LNET zeros the TIP, asserts $\overline{DONE}$ to the DMAC concurrent with the next $\overline{DACK}$ signal, increments the retry count and remains in the transmit mode ($\overline{TXREQ}$ asserted, etc.), the Jam is sent, and the Back-off delay is observed. In the meantime, 16 bytes of data are loaded into the TXFIFO by the DMAC. The packet is then transmitted as before.

If the MI asserts SIGQUAL *after* the first 512 TXCLKs, $\overline{IRQ}$ is asserted and the Transmitter Status field in Status Register 2 is set to 011.

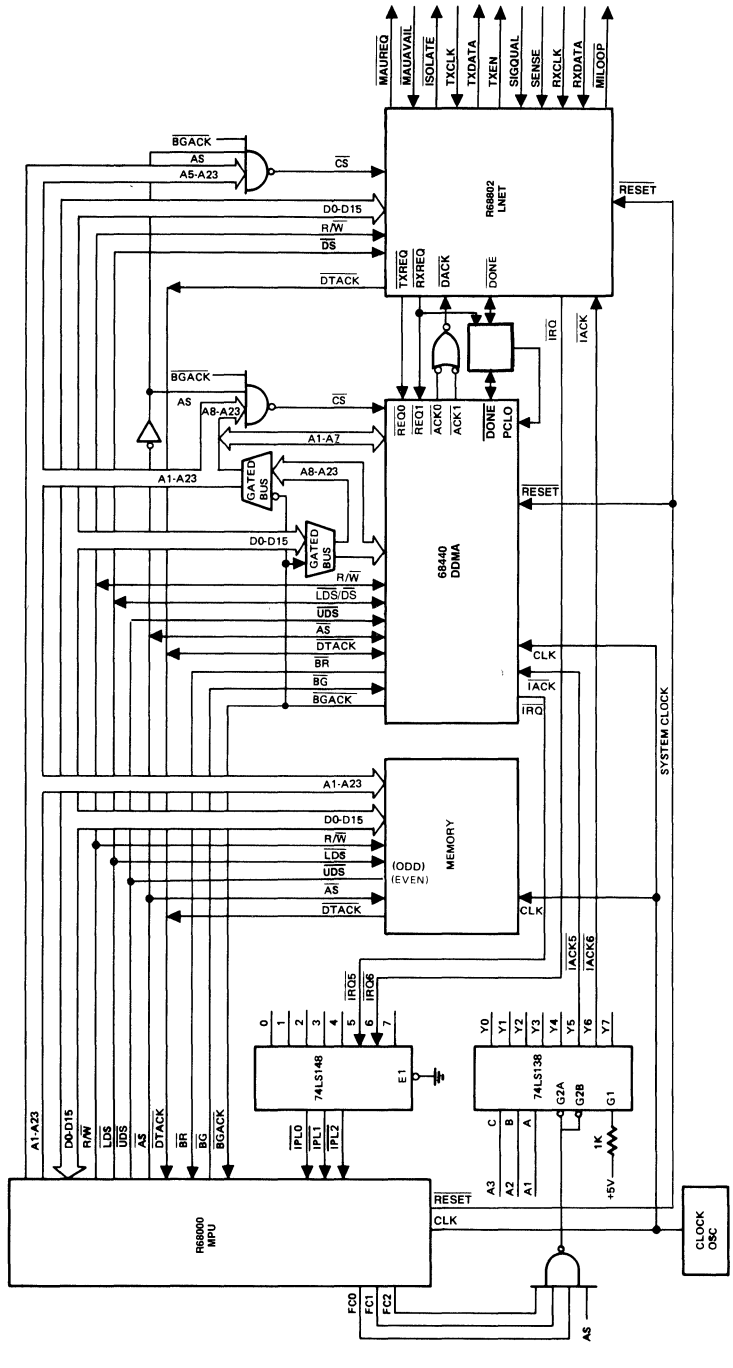


Figure 4. Typical Interface to 68000-Based System

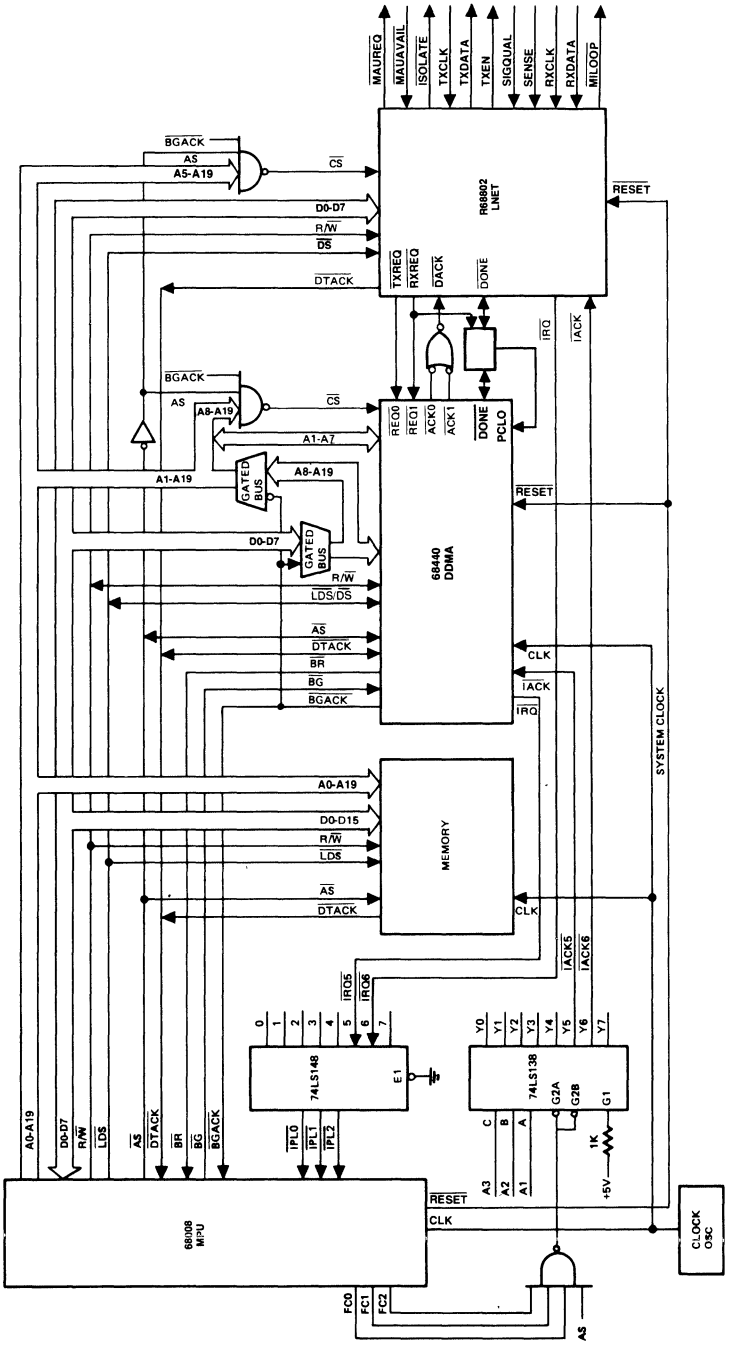
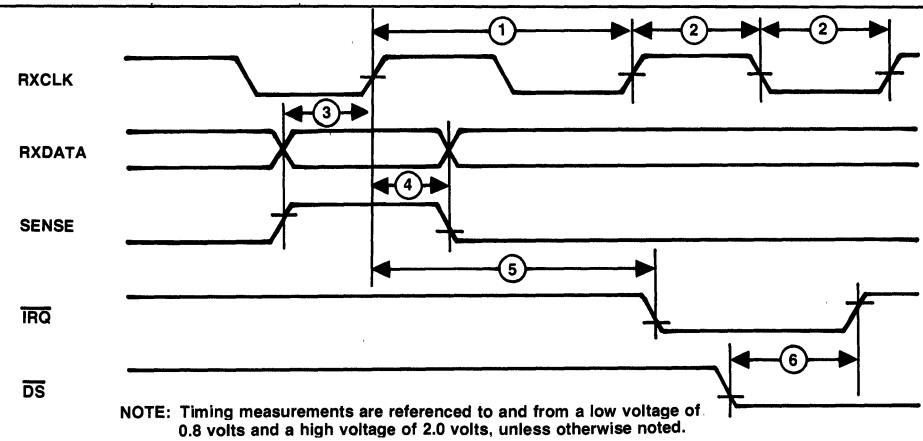
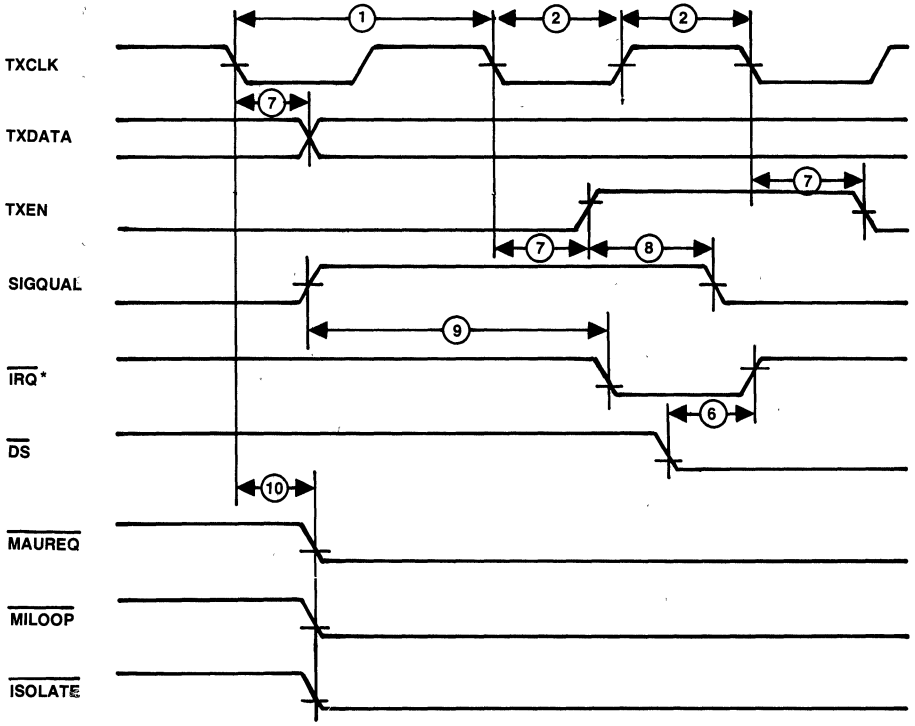


Figure 5. Typical Interface to 68008-Based System



NOTE: Timing measurements are referenced to and from a low voltage of 0.8 volts and a high voltage of 2.0 volts, unless otherwise noted.

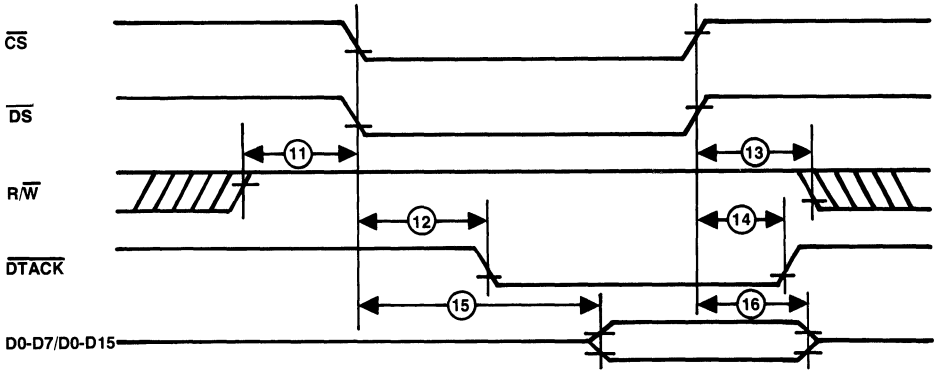
Figure 6. Manchester Interface Serial Receiver Timing



NOTE: Timing measurements are referenced to and from a low voltage of 0.8 volts and a high voltage of 2.0 volts, unless otherwise noted.

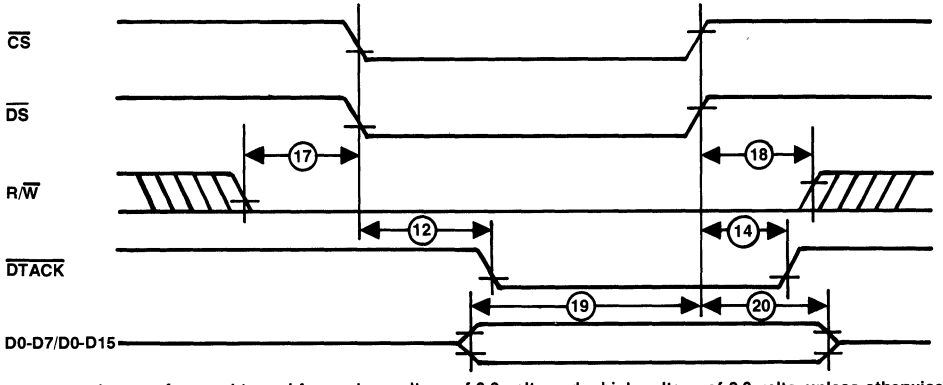
*$\overline{IRQ}$ assertion on collision not required—Bit 3 of the mode register (MR) determines whether or not $\overline{IRQ}$ asserts on collision.

Figure 7. Manchester Interface Serial Transmitter Timing



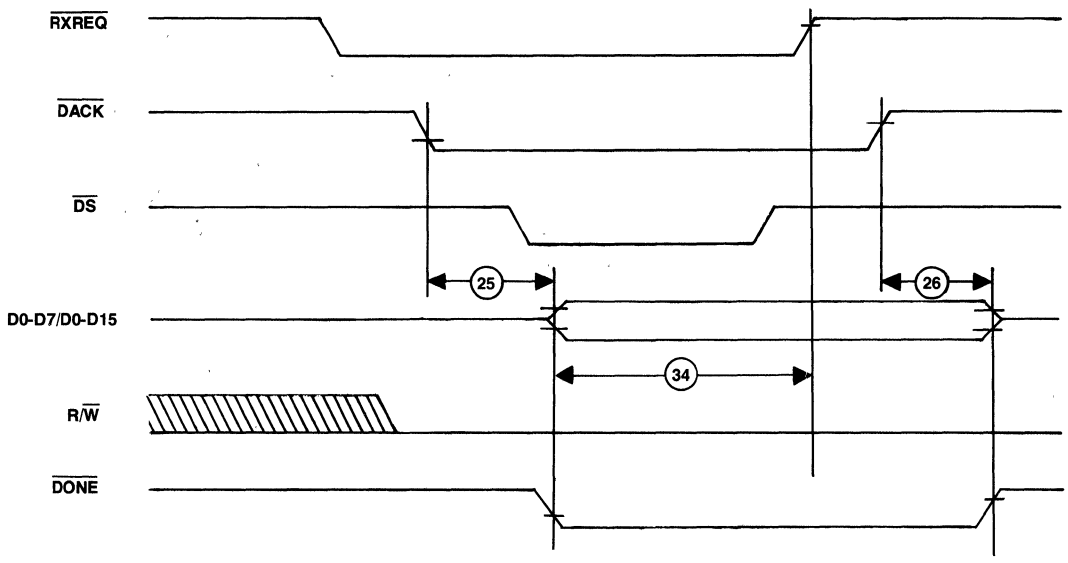
NOTE:
Timing measurements are referenced to and from a low voltage of 0.8 volts and a high voltage of 2.0 volts, unless otherwise noted.

Figure 8. LNET Read Cycle Timing



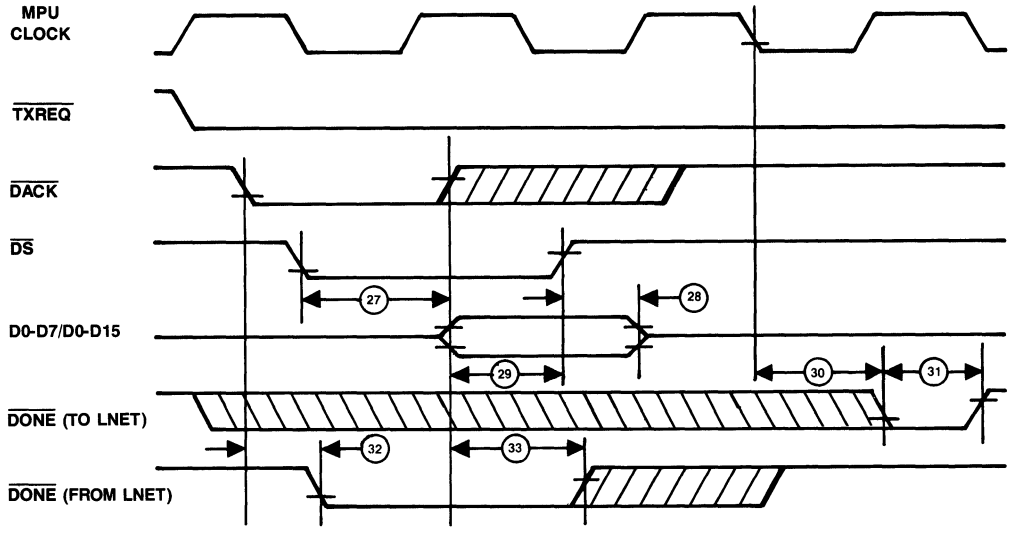
NOTE:
Timing measurements are referenced to and from a low voltage of 0.8 volts and a high voltage of 2.0 volts, unless otherwise noted.

Figure 9. LNET Write Cycle Timing



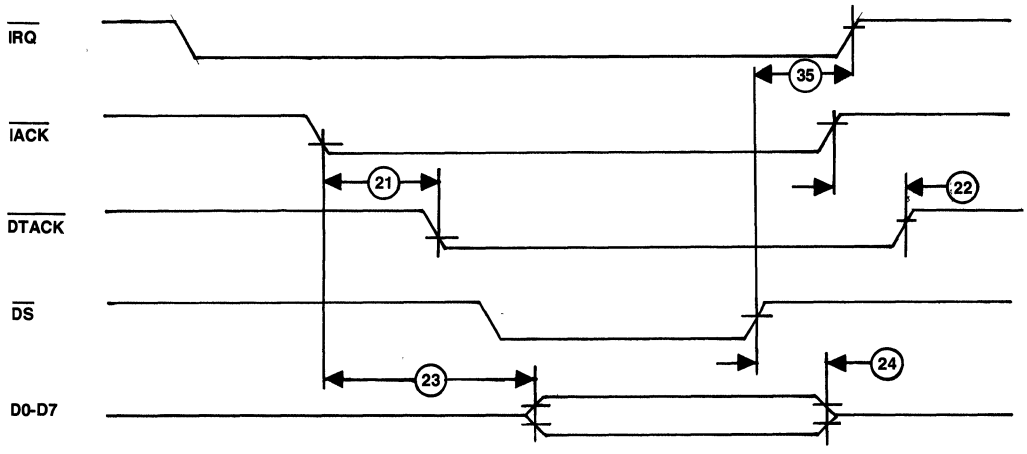
NOTES: 1. Timing measurements are referenced to and from a low voltage of 0.8 volts and a high voltage of 2.0 volts, unless otherwise noted.
2. Word mode only.

Figure 10. LNET to Memory DMA Transfer Cycle Timing



NOTES: 1. Timing measurements are referenced to and from a low voltage of 0.8 volts and a high voltage of 2.0 volts, unless otherwise noted.
2. Word mode only.

Figure 11. Memory to LNET DMA Transfer Cycle Timing



NOTE: Timing measurements are referenced to and from a low voltage of 0.8 volts and a high voltage of 2.0 volts, unless otherwise noted.

Figure 12. Interrupt Request Cycle Timing

SPECIFICATIONS

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0Vdc ± 5%, V_S = 0Vdc, T_A = 0 to 70°C)

Number	Characteristic	Symbol	Min	Typ	Max	Unit
1	Clock Period	t_{CP}	90		1000	ns
2	Receive Clock Pulse Width	t_{CFR}	45		—	ns
3	Receive Data/Sense Setup	t_{RXS}	30		—	ns
4	RXDATA, Sense Hold Time	t_{RXH}	20		—	ns
5	$\overline{IRQ}$ Delay from RXCLK	t_{RID}	0		80	ns
6	$\overline{DS}$ to $\overline{IRQ}$ Clear (Status Read)	t_{DID}	50		—	ns
7	TXDATA/TXEN Delay (C_L = 35pF)	t_{TXD}	20		60	ns
8	SIGQUAL Hold Time	t_{CPH}	0		—	ns
9	$\overline{IRQ}$ Delay from SIGQUAL Edge (Optional)*	t_{ISD}	0			ns
10	MAU/MI Control Output Delay	t_{MOD}	0		80	ns
11	R/$\overline{W}$ High to $\overline{CS}$, $\overline{DS}$ Low	t_{RHSL}	0		—	ns
12	$\overline{CS}$ Low to $\overline{DTACK}$ Low	t_{CLDAL}	20	40	80	ns
13	$\overline{CS}$, $\overline{DS}$ High to R/$\overline{W}$ Low	t_{SHRL}	20		—	ns
14	$\overline{CS}$ High to $\overline{DTACK}$ Tristate	t_{SHDAT}	20	40	80	ns
15	$\overline{CS}$, $\overline{DS}$ Low to Data Valid	t_{SLDV}	0		140	ns
16	$\overline{CS}$, $\overline{DS}$ High to Data Invalid	t_{SHDI}	10		150	ns
17	R/$\overline{W}$ Low to $\overline{CS}$, $\overline{DS}$ Low	t_{RLSL}	0		—	ns
18	$\overline{CS}$, $\overline{DS}$ High to R/$\overline{W}$ High	t_{SHRH}	20		—	ns
19	Data Valid to $\overline{CS}$, $\overline{DS}$ High	t_{DVSH}	100		—	ns
20	$\overline{CS}$, $\overline{DS}$ High to Data Invalid	t_{SHDI}	10		—	ns
21	$\overline{IACK}$ Low to $\overline{DTACK}$ Low	t_{IALAL}	20	40	80	ns
22	$\overline{IACK}$ High to $\overline{DTACK}$ Tristate	t_{IAHDAT}	20	40	80	ns
23	$\overline{IACK}$ Low to Data Valid	t_{IALDV}	0		140	ns
24	$\overline{DS}$ High to Data Invalid	t_{ISHDI}	10		50	ns
25	$\overline{DACK}$ Low to $\overline{DONE}$/Data Valid	t_{DLDV}	0		50	ns
26	$\overline{DTACK}$ High to $\overline{DONE}$ Invalid/Data	t_{DHDV}	0		40	ns
27	$\overline{DS}$ Low to $\overline{DACK}$ High	t_{DLDH}	0		50	ns
28	$\overline{DS}$ High to Data Invalid	t_{SHDI}	0		40	ns
29	Data Invalid to $\overline{DS}$ High	t_{DVSH}	65		—	ns
30	Clock Low to $\overline{DONE}$ (to LNET) Low	t_{CLDL}	0		100	ns
31	External $\overline{DONE}$ Pulse Width	t_{EDPW}	70		250	ns
32	$\overline{DACK}$ Low to Internal $\overline{DONE}$ Low Delay	t_{DLID}			80	ns
33	$\overline{DACK}$ High to Internal $\overline{DONE}$ High Delay	t_{DHID}			80	ns
34	$\overline{DONE}$ Low to $\overline{RXREQ}$ High	t_{DLRXH}		2		RXCLK
35	$\overline{DS}$ High to $\overline{IRQ}$ High	t_{DSHIH}		2		RXCLK

Note:
* $\overline{IRQ}$ assertion on collision dependent on bit 3 of mode register (MR).

MAXIMUM RATINGS

Characteristics	Symbol	Value
Supply Voltage	V_{CC}	−0.3 to +7.0V
Input Voltage	V_{IN}	−0.3 to +7.0V
Operating Temperatures	T_A	0 to 70°C
Storage Temperatures	T_{STG}	−55 to +150°C

Note:
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, normal precautions should be taken to avoid application of any voltage higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{CC}).

THERMAL CHARACTERISTICS

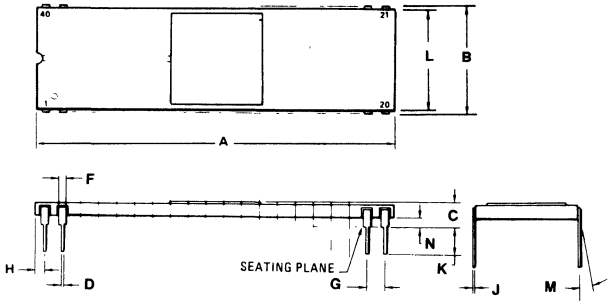
Characteristics	Symbol	Value	Rating
Thermal Resistance	θ_{JA}		
Ceramic		50	°C/W
Plastic		68	°C/W

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0Vdc ± 5%, V_{SS} = 0Vdc, T_A = 0 to 70°C unless otherwise noted)

Characteristics	Symbol	Min	Max	Unit	Test Conditions
Input High Voltage	V_{IH}	+2.0	V_{CC}	V	
Input Low Voltage	V_{IL}	−0.3	+0.8	V	
Input Leakage Current R/W, RESET, CS	I_{IN}	—	10	μA	V_{IN} = 0 to 5.25V V_{CC} = 0V
Input Leakage Current for Three-State (Off) DTACK, D0-D15	I_{TSI}	—	10	μA	V_{IN} = 0.4 to 2.4V V_{CC} = 0V
Output High Voltage	V_{OH}		—		V_{CC} = 4.75V
RXREQ, TXREQ, DTACK,		+2.4	—	V	I_{LOAD} = −400 μA, C_{LOAD} = 130 pF
D0-D15, MILOOP, MAUREQ, ISOLATE		+2.4	—	V	I_{LOAD} = −400 μA, C_{LOAD} = 32 pF
TXEN, TXDATA		+2.4	—	V	I_{LOAD} = 0, C_{LOAD} = 30 pF
Output Low Voltage	V_{OL}				V_{CC} = 4.75V
RXREQ, TXREQ, TXEN, TXDATA, DTACK, D0-D15 MILOOP, MAUREQ, ISOLATE		—	0.5	V	I_{LOAD} = 3.2 mA
IRQ, DONE		—	0.5	V	I_{LOAD} = 8.8 mA
Power Dissipation	P_{INT}	—	1.0	W	T_A = 25°C
Input Capacitance	C_{IN}	—	13	pF	V_{CC} = 5.0V V_{IN} = 0V f = 1 MHz T_A = 25°C

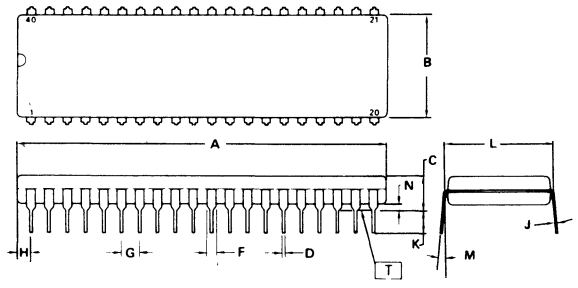
PACKAGE DIMENSIONS

40-PIN CERAMIC DIP



DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	50 29	51 31	1 980	2.020
B	14 86	15 62	0 585	0 615
C	2 54	4 19	0 100	0.165
D	0 38	0 53	0 015	0 021
F	0 76	1 40	0 030	0 055
G	2 54 BSC		0 100 BSC	
H	0 76	1 78	0 030	0 070
J	0 20	0.33	0 008	0 013
K	2 54	4 19	0 100	0 165
L	14 60	15 37	0 575	0 605
M	0°	10°	0°	10°
N	0 51	1 52	0 020	0 060

40-PIN PLASTIC DIP



DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	51 28	52 32	2 040	2 060
B	13 72	14 22	0 540	0 560
C	3 55	5 08	0 140	0 200
D	0 36	0 51	0 014	0 020
F	1 02	1 52	0 040	0 060
G	2 54 BSC		0 100 BSC	
H	1 65	2.16	0 065	0 085
J	0 20	0 30	0 008	0 012
K	3 05	3 56	0 120	0 140
L	15 24 BSC		0 600 BSC	
M	7°	10°	7°	10°
N	0 51	1 02	0 020	0 040

Rockwell

R68C552
DUAL ASYNCHRONOUS COMMUNICATIONS INTERFACE ADAPTER (DACIA)

PRELIMINARY

DESCRIPTION

The Rockwell CMOS R68C552 Dual Asynchronous Communications Interface Adapter (DACIA) provides an easily implemented, program controlled interface between 16-bit microprocessor-based systems and serial communication data sets and modems.

The DACIA has an internal baud rate generator. This feature eliminates the need for multiple component support circuits, a crystal being the only other part required. The Transmitter baud rate can be selected under program control to be either 1 of 15 different rates from 50 to 38,400 baud, or at 1/16 times an external clock rate. The Receiver baud rate may be selected under program control to be either the Transmitter rate, or at 1/16 times the external clock rate. The DACIA is programmable for word lengths of 5, 6, 7 or 8 bits; even, odd, or no parity; and 1 or 2 stop bits.

The DACIA is designed for maximum programmed control from the microprocessor (MPU) to simplify hardware implementation. Dual sets of registers allow independent control and monitoring of each channel. The DACIA also provides a unique, programmable Automatic Address Recognition mode for use in a multi-drop environment.

The Control Register and Status Register permit the MPU to easily select the R68C552's operating modes and determine operational status.

The Interrupt Enable Registers (IER) and Interrupt Status Registers (ISR) allow the MPU to control and monitor the interrupt capabilities of the DACIA.

The Control and Format Register (CFR) permits selection of baud rates, word lengths, parity and stop bits as well as control of DTR and RTS output signals.

The Status Register (SR) gives the MPU access to the state of the modem control lines, framing error, transmitter underrun and break conditions.

The Compare Data Registers (CDR) hold the data value to be used in the compare mode.

The IRQ Vector Register (IVR) holds the interrupt vector for use in the interrupt acknowledge state, or commands a Transmit Break and provides for parity/address recognition during Automatic Address Recognition mode.

ORDERING INFORMATION

Part Number:
R68C552

Package:
C = Ceramic
P = Plastic

FEATURES

- Low power CMOS N-well silicon gate technology
- Two independent full duplex channels with buffered receivers and transmitters.
- Data set/modem control functions
- Internal baud rate generator with 15 programmable baud rates (50 to 38,400)
- Program-selectable internally or externally controlled receiver rate
- Programmable word lengths, number of stop bits, and parity bit generation and detection
- Programmable interrupt control
- Programmable control of edge detect for DCD, DSR, DTR, RTS, and CTS
- Program-selectable serial echo mode for each channel
- Automatic Address Recognition mode for multi-drop operations
- 5.0 Vdc ±5% supply requirements
- 40-pin plastic or ceramic DIP
- Full TTL or CMOS input/output compatibility
- Compatible with R68000 microprocessor family

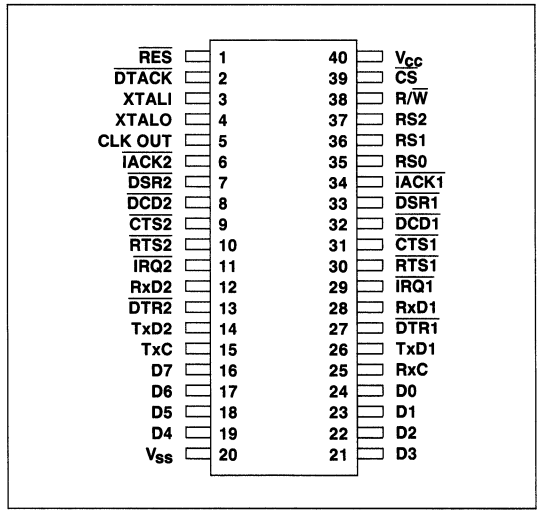


Figure 1. R68C552 Pin Configuration

INTERFACE SIGNALS

Figure 2 shows the DACIA interface signals associated with the microprocessor and the modem.

DATA BUS (D0-D7)

The D0-D7 pins are eight data lines that transfer data between the microprocessor (MPU) and the DACIA. These lines are bidirectional and are normally high-impedance except during READ cycle when the DACIA is selected.

REGISTER SELECTS (RS0, RS1, RS2)

The three register select lines are normally connected to the processor address lines to allow the MPU to select the various internal registers. Table 1 shows the internal register select coding and identifies the abbreviations (ABBR) used throughout the text for each register. Table 2 summarizes the control and status registers and shows each bit allocation.

READ/WRITE (R/$\overline{W}$)

The R/$\overline{W}$ input, generated by the microprocessor, controls the direction of data transfer. A high on the R/$\overline{W}$ line indicates a read cycle, while a low indicates a write cycle.

CHIP SELECT ($\overline{CS}$)

The chip select input is normally connected to the processor address lines either directly or through decoders. The DACIA latches address and R/$\overline{W}$ inputs on the falling edge of $\overline{CS}$ and latches the data bus inputs on the rising edge of $\overline{CS}$.

RESET ($\overline{RES}$)

During system initialization a low level on the $\overline{RES}$ input causes a RESET to occur. At this time the IER's are set to $80, the $\overline{DTR}$ and $\overline{RTS}$ lines go to the high state, the RDR register is cleared, the IVR is set to $0F, the compare mode is disabled, and the $\overline{CTS}$, $\overline{DCD}$, $\overline{DSR}$ flags are cleared. No other bits are affected.

TRANSMIT DATA (TXD1, TXD2)

The TxD outputs transfer serial non-return to zero (NRZ) data to the data communications equipment (DCE). The data is transferred, LSB first, at a rate determined by the baud rate generator.

RECEIVE DATA (RXD1, RXD2)

The RxD inputs transfer serial NRZ data into the DACIA from the DCE, LSB first. The receiver baud rate is determined by the baud rate generator.

CLEAR TO SEND ($\overline{CTS1}$, $\overline{CTS2}$)

The $\overline{CTS}$ control line inputs allow handshaking by the transmitter. When $\overline{CTS}$ is low, the data is transmitted continuously. When $\overline{CTS}$ is high, the Transmit Data Register empty bit in the ISR is not set. The word presently in the Transmit Shift Register is sent normally. Any active transition on the $\overline{CTS}$ lines sets the $\overline{CTS}$ bit in the appropriate ISR. The $\overline{CTS}$ status bit in the SR reflects the current high or low state of $\overline{CTS}$.

DATA CARRIER DETECT ($\overline{DCD1}$, $\overline{DCD2}$)

These two lines may be used as general purpose inputs. An active transition sets the $\overline{DCD}$ bit in the ISR. The $\overline{DCD}$ bit in the SR reflects the current state of the $\overline{DCD}$ line.

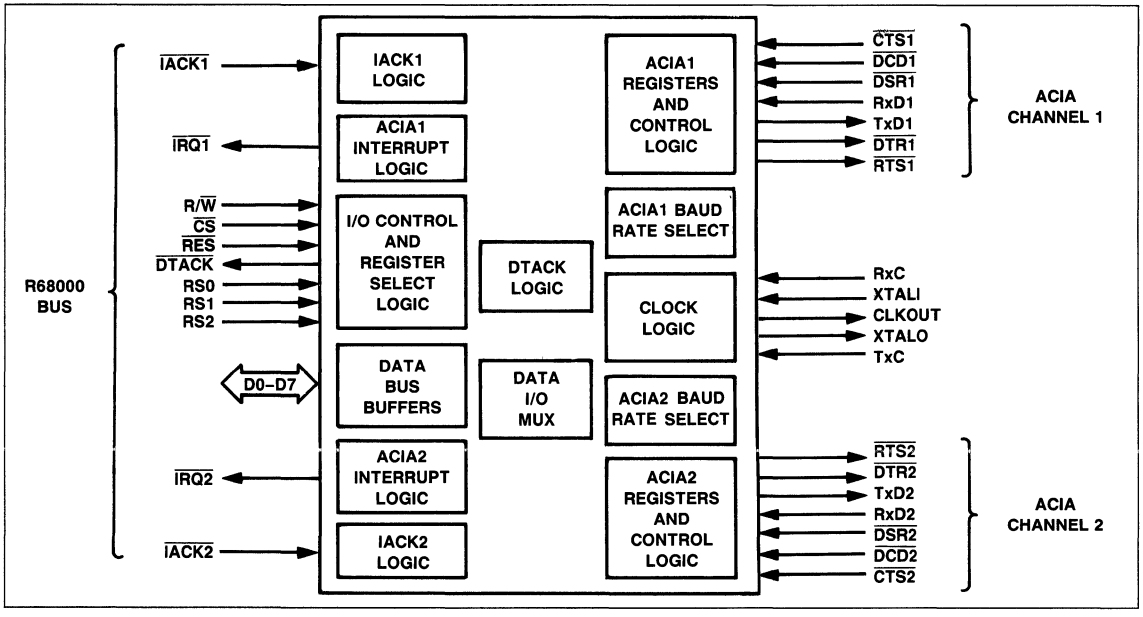


Figure 2. DACIA Interface Signals

DATA SET READY ($\overline{DSR1}$, $\overline{DSR2}$)

These two lines may be used as general purpose inputs. An active transition sets the $\overline{DSR}$ bit in the ISR. The $\overline{DSR}$ bit in the SR reflects the current state of the $\overline{DSR}$ line.

REQUEST TO SEND ($\overline{RTS1}$, $\overline{RTS2}$)

These two lines may be used as general purpose outputs. They are set high upon reset. Their state may be programmed by setting the appropriate bits in the CFR high or low. The state of the $\overline{RTS}$ line is reflected by the $\overline{RTS}$ bit in the SR.

DATA TERMINAL READY ($\overline{DTR1}$, $\overline{DTR2}$)

These two lines may be used as general purpose outputs. They are set high upon reset. Their state may be programmed by setting the appropriate bits in the CFR high or low. The state of the $\overline{DTR}$ line is reflected by the $\overline{DTR}$ bit in the SR.

INTERRUPT REQUEST ($\overline{IRQ1}$, $\overline{IRQ2}$)

The $\overline{IRQ}$ lines are open-drain outputs from the interrupt control logic. $\overline{IRQ1}$ is associated with ACIA1 and $\overline{IRQ2}$ is associated with ACIA2. These lines are normally high but go low when one of the flags in the ISR is set, provided that its corresponding enable bit is set in the IER.

CLOCK CIRCUIT

The internal clock oscillator supplies the time base for the baud rate generator. The oscillator can be driven by a crystal or an external clock, or it can be disabled, in which case the time base for the baud rate is generated by the Receiver External Clock (RxC) and Transmitter External Clock (TxC) input pins. Figure 3 shows the three possible clock configurations.

CRYSTAL (XTALI, XTALO)

These pins are normally connected to an external 3.6864 MHz crystal used as the time base for the baud rate generator. As an alternative, the XTALI pin may be driven with an externally generated clock in which case the XTALO pin must float.

RECEIVER CLOCK (RxC)

This pin is the Receiver 16x clock input when the baud rate generator is programmed for External Clock. Figure 15 shows timing considerations for RxC.

TRANSMITTER CLOCK (TxC)

This pin is the transmitter 16x clock input when the baud rate generator is programmed for External Clock. Figure 16 shwos timing considerations for TxC.

Note

When RxC and TxC are used for external clock input, XTALI must be tied to ground (Vss) and XTALO must be left open (floating).

CLOCK OUT (CLK OUT)

This output is a buffered output from the 3.6864 MHz crystal oscillator. It may be used to drive the XTALI input of another DACIA. This allows multiple DACIA chips to be used in a system with only one crystal needed. CLK OUT is in phase with XTALI.

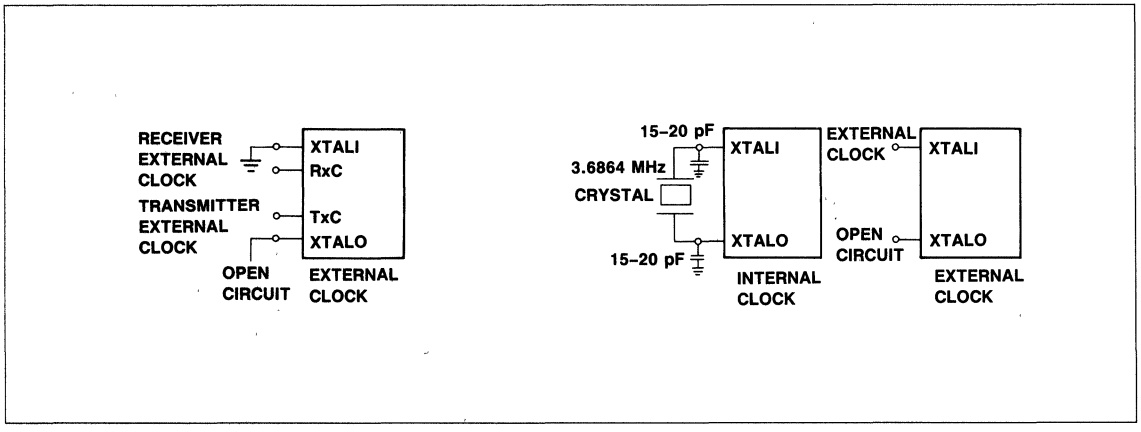


Figure 3. DACIA Clock Generation

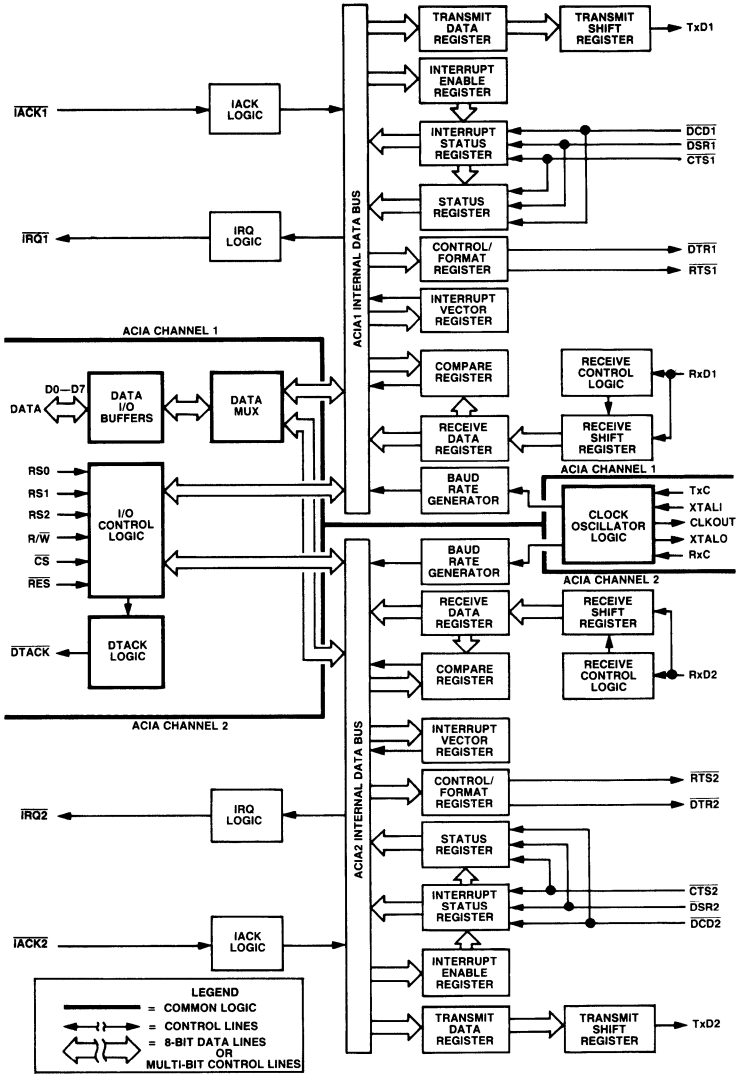


Figure 4. DACIA Block Diagram

FUNCTIONAL DESCRIPTION

Figure 4 is a block diagram of the DACIA which consists of two asynchronous communications interface adapters with common microprocessor interface control logic and data bus buffers. The individual functional elements of the DACIA are described in the following paragraphs.

DATA BUS BUFFER

The Data Bus Buffer is a bidirectional interface between the system data lines and the internal data bus. When R/$\overline{W}$ is high and $\overline{CS}$ is low, the Data Bus Buffer passes data from the internal data bus to the system data lines. When R/$\overline{W}$ is high, $\overline{CS}$ is high, and either $\overline{IACK}$ line is low, the IRQ vector is passed to the system data bus. When R/$\overline{W}$ is low and $\overline{CS}$ is low, data is brought into the DACIA from the system data bus. The following table summarizes the Data Bus Buffer states.

Data Bus Buffer Summary

Control Signals				Data Bus Buffer State
R/$\overline{W}$	$\overline{CS}$	$\overline{IACK1}$	$\overline{IACK2}$	
L	L	L	L	ILLEGAL MODE — TRI STATE
L	L	L	H	ILLEGAL MODE — TRI STATE
L	L	H	L	ILLEGAL MODE — TRI STATE
L	L	H	H	WRITE MODE — TRI STATE
L	H	L	L	ILLEGAL MODE — TRI STATE
L	H	L	H	ILLEGAL MODE — TRI STATE
L	H	H	L	ILLEGAL MODE — TRI STATE
L	H	H	H	TRI STATE
H	L	L	L	ILLEGAL MODE — OUTPUT $0F
H	L	L	H	ILLEGAL MODE — OUTPUT $0F
H	L	H	L	ILLEGAL MODE — OUTPUT $0F
H	L	H	H	READ MODE — OUTPUT DATA
H	H	L	L	ILLEGAL MODE — OUTPUT $0F
H	H	L	H	OUTPUT IRQ VECTOR 1
H	H	H	L	OUTPUT IRQ VECTOR 2
H	H	H	H	TRI STATE

TRANSMIT AND RECEIVE DATA REGISTERS

These registers are used as temporary data storage for the DACIA Transmit and Receive circuits. The Transmit Data Register is characterized as follows:

- Bit 0 is the leading bit to be transmitted.
- Unused data bits are the high-order bits and are "don't care" for transmission.
- Write-Only Register.

The Receive Data Register is characterized in a similar fashion as follows:

- Bit 0 is the leading bit received.
- Unused data bits are the high order bits and are "0" for the receiver.
- Parity bits are not contained in the Receive Data Register, but are stripped off after being used for external parity checking. Parity and all unused high-order bits are "0".
- Read-Only Register

Figure 5 shows an example of a single transmitted or received data word. In this example, the data word is formatted with 8 data bits, parity, and two stop bits. Figure 5 also shows a single character transmitted or received in Address Recognition mode. In this example, the address or data word is 8 bits, there is no parity bit, and there are two stop bits. The 10th bit, (normal parity bit) is an address/data indicator bit. A 1 means the 8 bits are an address that will be compared with the address stored in the Compare Data Register. A 0 means the 8 bits are data.

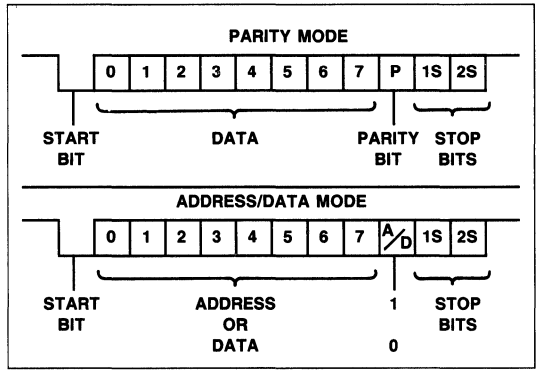


Figure 5. Typical Data Word

INTERRUPT LOGIC

The interrupt logic causes the $\overline{IRQ}$ lines ($\overline{IRQ1}$ or $\overline{IRQ2}$) to go low when conditions are met that require the attention of the MPU. There are two registers (the Interrupt Enable Register and the Interrupt Status Register) involved in the control of interrupts in the DACIA. Corresponding bits in both registers must be set to cause an $\overline{IRQ}$.

INTERRUPT ENABLE REGISTER (IER)

The Interrupt Enable Register (IER) is a write-only register that allows each of the possible IRQ sources to be enabled, or disabled, individually without affecting any of the other interrupt enable bits in the register. IRQ sources are enabled by writing to the IER with bit 7 set to a 1 and every bit set to a 1 that corresponds to the IRQ source to be enabled. IRQ sources are disabled by writing to the IER with bit 7 set to a 0 and every bit set to a 1 that corresponds to the IRQ source to be disabled. Any bit (except bit 7) to which a 0 is written is unaffected and remains in its original state. As an example, writing $7F to the IER will disable all IRQ source bits, but writing $FF to the IER will enable all IRQ source bits. A hardware reset ($\overline{RES}$) clears all IRQ source bits to the 0 state. Bit assignments for the IER are as follows:

7	6	5	4	3	2	1	0
CLEAR/ SET BITS	TDR EMPTY IE	$\overline{CTS}$ IE	$\overline{DCD}$ IE	$\overline{DSR}$ IE	PARITY ERROR IE	FRM OVR BRK CPR IE	RDR FULL IE

Table 1. DACIA Register Selection

HEX	REGISTER SELECT LINES			CONTROL & FORMAT REGISTER BITS		REG	REGISTER ACCESS	
							WRITE	READ
00	L	L	L	—	—	IER1 ISR1	INTERRUPT ENABLE REGISTER 1	INTERRUPT STATUS REGISTER 1
01	L	L	H	0	—	CFR1 SR1	CONTROL REGISTER 1	STATUS REGISTER 1
				1	—	CFR1	FORMAT REGISTER 1	INVALID
02	L	H	L	—	0	CDR1	COMPARE DATA REGISTER 1	INVALID
				—	1	IVR1	IRQ VECTOR 1	INVALID
03	L	H	H	—	—	TDR1 RDR1	TRANSMIT DATA REGISTER 1	RECEIVE DATA REGISTER 1
04	H	L	L	—	—	IER2 ISR2	INTERRUPT ENABLE REGISTER 2	INTERRUPT STATUS REGISTER 2
05	H	L	H	0	—	CFR2 SR2	CONTROL REGISTER 2	STATUS REGISTER 2
				1	—	CFR2	FORMAT REGISTER 2	INVALID
06	H	H	L	—	0	CDR2	COMPARE DATA REGISTER 2	INVALID
				—	1	IVR2	IRQ VECTOR 2	INVALID
07	H	H	H	—	—	TDR2 RDR2	TRANSMIT DATA REGISTER 2	RECEIVE DATA REGISTER 2

Table 2. Control and Status Registers Format Summary

REGISTER BIT NUMBERS								REGISTER	$\overline{RES}$
7	6	5	4	3	2	1	0		
CLEAR/SET BITS	TDR EMPTY IE	$\overline{CTS}$ IE	$\overline{DCD}$ IE	$\overline{DSR}$ IE	PARITY ERROR IE	FRM, OVR BRK, CPR IE	RDR FULL IE	INTERRUPT ENABLE REGISTERS	$80
ANY BIT SET	TDR EMPTY	$\overline{CTS}$ TRANS	$\overline{DCD}$ TRANS	$\overline{DSR}$ TRANS	PARITY ERROR	FRM, OVR BRK, CPR	RDR FULL	INTERRUPT STATUS REGISTERS	—
FRAMING ERROR	TRANS UNDR	$\overline{CTS}$ STATUS	$\overline{DCD}$ STATUS	$\overline{DSR}$ STATUS	REC BREAK	$\overline{DTR}$ STATUS	$\overline{RTS}$ STATUS	STATUS REGISTERS	—
0	IVR/CDR REG	NO. STOP BITS	ECHO	BAUD RATE SELECTION				CONTROL REGISTERS AND FORMAT REGISTERS	—
1	NUMBER OF DATA BITS		PARITY SELECTION		PARITY ENABLE	$\overline{DTR}$ CONTROL	$\overline{RTS}$ CONTROL		
COMPARE BITS (ADDRESS RECOGNITION)								COMPARE DATA REGISTER	—
IRQ VECTOR ADDRESS						IRQ SOURCE		IA MODE INTERRUPT VECTOR REGISTER T/R MODE	$0F
NOT USED						TRANS BRK	PAR/ ADDR		

INTERRUPT STATUS REGISTER (ISR)

The Interrupt Status Register (ISR) is a read-only register that identifies the current status condition for each DACIA internal IRQ source. Bits 6 through 0 of the ISR are set to a 1 whenever the corresponding IRQ source condition has occurred in the DACIA. Bit 7 identifies if any of the IRQ source status bits have been set in the ISR.

7	6	5	4	3	2	1	0
ANY BIT SET	TDR EMPTY	$\overline{\text{CTS}}$ TRANS	$\overline{\text{DCD}}$ TRANS	$\overline{\text{DSR}}$ TRANS	PARITY ERROR	FRM OVR BRK CPR	RDR FULL

Bit 7 **Any Bit Set**
1 Any bit (6 through 0) has been set to a 1
0 No bits have been set to a 1

Bit 6 **Transmit Data Register Empty (TDR EMPTY)**
1 Transmit Data Register has been transferred to the shift register
0 New data has been written to the Transmit Data Register

Bit 5 **Transition On $\overline{\text{CTS}}$ Line ($\overline{\text{CTS}}$ TRANS)**
1 A positive or negative transition has occurred on $\overline{\text{CTS}}$
0 No transition has occurred on $\overline{\text{CTS}}$, or ISR has been read

Bit 4 **Transition On $\overline{\text{DCD}}$ Line ($\overline{\text{DCD}}$ TRANS)**
1 A positive or negative transition has occurred on $\overline{\text{DCD}}$
0 No transition has occurred on $\overline{\text{DCD}}$, or ISR has been read

Bit 3 **Transition On $\overline{\text{DSR}}$ Line ($\overline{\text{DSR}}$ TRANS)**
1 A positive or negative transition has occurred on $\overline{\text{DSR}}$
0 No transition has occurred on $\overline{\text{DSR}}$, or ISR has been read

Bit 2 **Parity Error**
1 A parity error has occurred in received data
0 No parity error has occurred, or the Receive Data Register (RDR) has been read

Bit 1 **Frame Error, Overrun or Break (FRM, OVR, BRK, CPR)**
1 A framing error, receive overrun, or receive break has occurred or, in Compare Mode
0 No error, overrun, break has occurred or RDR has been read, or not in Compare Mode

Bit 0 **Receive Data Register Full (RDR FULL)**
1 Shift register data has been transferred to Receive Data Register
0 Receive Data Register has been read

INTERRUPT VECTOR REGISTER (IVR)

The DACIA has two Interrupt Vector Registers which are write-only registers. By storing the appropriate vector address number in bits 7 through 2 of the IVR, the DACIA will place the vector on the data bus when requested by the $\overline{\text{IACK}}$ signal. In this mode, bits 1 and 0 identify the source of the IRQ.

Note: In order for the IVR Vector Address to be placed on the bus, bit 6 of the Control/Format Register (CFR1, CFR2) must be a 1.

During the Transmit Receive mode, bits 7 through 2 are not used and are treated as "don't care" bits. In this mode, bits 1 and 0 are used for Transmit Break and Parity/Address recognition.

Writing a 1 to bit 1 of the IVR causes a continuous Break to be transmitted by the ACIA associated with the register. Writing a 0 to this bit allows normal transmission to resume. Writing a 1 to bit 0 of the IVR commands the value of the Parity bit to be sent to the Parity Error bit (bit 2 of the ISR). Writing a 0 to this bit allows normal Parity Error recognition to be in force. When an $\overline{\text{RES}}$ is received by the DACIA, both of these bits are reset to 0. The bits format for the IVR are as follows:

7	6	5	4	3	2	1	0
IRQ VECTOR ADDRESS						IRQ SOURCE	
NOT USED						TRANS BRK	PAR/ ADDR

Interrupt Acknowledge Mode (IA Mode)

Bits 7-2 **IRQ Vector Address**

Bit 1 **IRQ Source Channel**
1 ACIA1 selected
0 ACIA2 selected

Bit 0 **IRQ Source**
1 Other IRQ (CTS, DCD, DSR, Parity, Break, OV)
0 Transmit or Receive IRQ

Transmit/Receive Mode (T/R Mode)

Bits 7-2 **Not used (don't care)**

Bit 1 **Transmit Break (TRANS BRK)**
1 Transmit continuous Break until disabled
0 Resume normal transmission

Bit 0 **Parity/Address Recognition (PAR/ADDR)**
1 Send value of parity to ISR bit 2 (Address Recognition mode)
0 Return to normal Parity Error recognition mode

COMPARE DATA REGISTER

The Compare Data Register (CDR) is a write-only register which can be accessed when CFR bit 6 = 0. By writing a value into the CDR, the DACIA is put in the compare mode. In this mode, setting of the RDRF bit is inhibited and the FRM/OVR/BRK/CPR bit (bit 1) of the ISR is set until a character is received which matches the value in the CDR. The next character is then received and the RDRF bit is set. The receiver will now operate normally until the CDR is again loaded.

STATUS REGISTER (SR)

The Status Register (SR) is a read-only register that provides I/O status and error condition information. The SR is normally read after an IRQ has occurred to determine the exact cause of the interrupt condition.

7	6	5	4	3	2	1	0
FRAMING ERROR	TRANS UNDR	$\overline{CTS}$ STATUS	$\overline{DCD}$ STATUS	$\overline{DSR}$ STATUS	REC BREAK	$\overline{DTR}$ STATUS	$\overline{RTS}$ STATUS

Bit 7 **Framing Error**
1 A framing error occurred in receive data
0 No framing error occurred, or the RDR was read

Bit 6 **Transmitter Underrun (TRANS UNDR)**
1 Transmit shift register is empty and TDRE bits in IER and ISR are set
0 A write to the TDR has occurred

Bit 5 **$\overline{CTS}$ Status**
1 $\overline{CTS}$ line high
0 $\overline{CTS}$ line low

Bit 4 **$\overline{DCD}$ Status**
1 $\overline{DCD}$ line high
0 $\overline{DCD}$ line low

Bit 3 **$\overline{DSR}$ Status**
1 $\overline{DSR}$ line high
0 $\overline{DSR}$ line low

Bit 2 **REC Break**
1 A Receive Break has occurred
0 No Receive Break occurred, or RDR, was read

Bit 1 **$\overline{DTR}$ Status**
1 $\overline{DTR}$ line high
0 $\overline{DTR}$ line low

Bit 0 **$\overline{RTS}$ Status**
1 $\overline{RTS}$ line high
0 $\overline{RTS}$ line low

CONTROL AND FORMAT REGISTER (CFR)

The Control and Format Register (CFR) is a dual-function, write-only register which allows control of word length, baud rate, control line outputs, parity, echo mode, and compare/IVR access. When the CFR is written to with bit 7 = 0, the CFR functions as a Control Register. When the CFR is written to with bit 7 = 1, the CFR operates as a Formal Register.

Control Register (CFR Addressed with Bit 7 = 0)

7	6	5	4	3 2 1 0
0	IVR/CDR	NO. STOP BITS	ECHO	BAUD RATE SELECTION

Bit 6 **IVR/CDR**
1 Access the IRQ Vector Register (IVR)
0 Access the Compare Data Register (CDR)

Bit 5 **Number of Stop Bits**
1 Two stop bits
0 One stop bit

Bit 4 **Echo Selection (ECHO)**
1 Echo activated
0 Echo deactivated

Bits 3-0 **Baud Rate Selection**

3	2	1	0	Baud Rate
0	0	0	0	50
0	0	0	1	109.2
0	0	1	0	134.58
0	0	1	1	150
0	1	0	0	300
0	1	0	1	600
0	1	1	0	1200
0	1	1	1	1800
1	0	0	0	2400
1	0	0	1	3600
1	0	1	0	4800
1	0	1	1	7200
1	1	0	0	9600
1	1	0	1	19200
1	1	1	0	38400
1	1	1	1	External TxC and RxC Clocks

Format Register (CFR Addressed with Bit 7 = 1)

7	6 5	4 3	2	1	0
1	NUMBER OF DATA BITS	PARITY SELECTION	PARITY ENABLE	$\overline{DTR}$ CONTROL	$\overline{RTS}$ CONTROL

Bits 6-5 **Number of Data Bits Per Channel**

6	5	No. Bits
0	0	5
0	1	6
1	0	7
1	1	8

Bits 4-3 **Parity Mode Selection**

4	3	Selects
0	0	Odd Parity
0	1	Even Parity
1	0	Mark Parity
1	1	Space Parity

Bit 2 **Parity Enable**
1 Parity as specified by bits 4-3
0 No Parity

Bit 1 **$\overline{DTR}$ Control**
1 $\overline{DTR}$ high
0 $\overline{DTR}$ low

Bit 0 **$\overline{RTS}$ Control**
1 $\overline{RTS}$ high
0 $\overline{RTS}$ low

OPERATION

The ten modes (or conditions) of operation of the DACIA are:

- Continuous Data Transmit
- Continuous Data Receive
- Transmit Underrun Condition
- Effects of CTS on Transmitter
- Effects of Overrun on Receive
- Echo Mode Timing
- Framing Error
- Transmit Break Character
- Receive Break Character
- Automatic Address Mode

CONTINUOUS DATA TRANSMIT

In the normal operating mode, the TDRE bit in the ISR signals the MPU that the DACIA is ready to accept the next data word. An $\overline{IRQ}$ occurs if the corresponding TDRE IRQ enable bit is set in the IER. The TDRE bit is set at the beginning of the start bit. When the MPU writes a word to the TDR the TDRE bit is cleared. In order to maintain continuous transmission the TDR must be loaded before the stop bit(s) are ended. Figure 6 shows the relationship between $\overline{IRQ}$ and TxD for the Continuous Data Transmit mode.

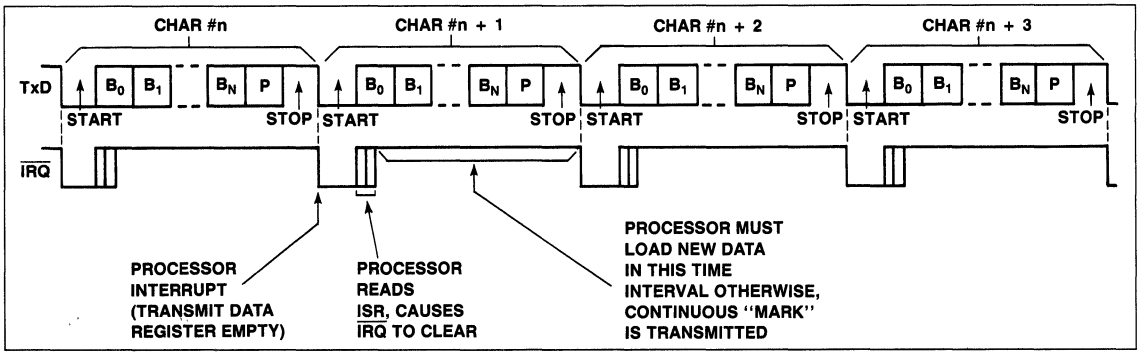


Figure 6. Continuous Data Transmit

CONTINUOUS DATA RECEIVE

Similar to the continuous data transmit mode, the normal receive mode sets the RDRF bit in the ISR when the DACIA has received a full data word. This occurs at about the 9/16 point through the stop bit. The processor must read the RDR before the next stop bit, or an overrun error occurs. Figure 7 shows the relationship between $\overline{IRQ}$ and RxD for the continuous Data Receive mode.

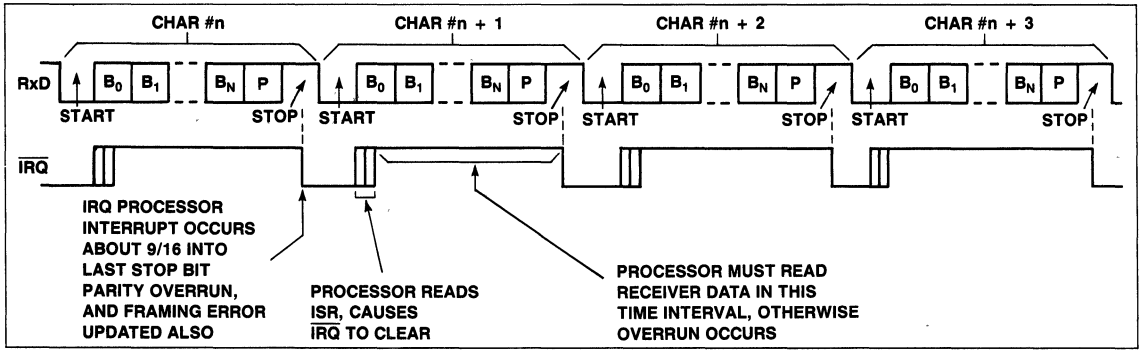


Figure 7. Continuous Data Receive

TRANSMIT UNDERRUN CONDITION

If the MPU is unable to load the TDR before the last stop bit is sent, the TxD line goes to the MARK condition and the underrun flag is set. This condition persists until the TDR is loaded with a new word. Figure 8 shows the relation between $\overline{IRQ}$ and TxD for the Transmit Underrun Condition.

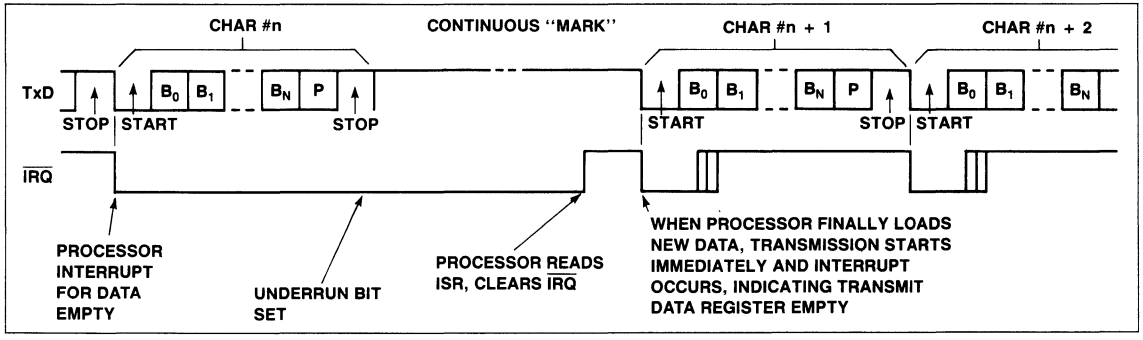


Figure 8. Transmit Underrun Condition Relationship

EFFECTS OF $\overline{CTS}$ ON TRANSMITTER

The $\overline{CTS}$ control line controls the transmission of data or the handshaking of data to a "busy" device (such as a printer). When the $\overline{CTS}$ line is low, the transmitter operates normally. Any transition on this line sets the $\overline{CTS}$ bit in the ISR. A high condition inhibits the TDRE bit in the ISR from becoming set. The word currently in the shift register continues to be sent but any word in the TDR is held until $\overline{CTS}$ goes low. At the high-to-low transition the $\overline{CTS}$ bit in the ISR is again set. Figure 9 shows the relationship of $\overline{IRQ}$, TxD, and $\overline{CTS}$ for the effects of $\overline{CTS}$ on the transmitter.

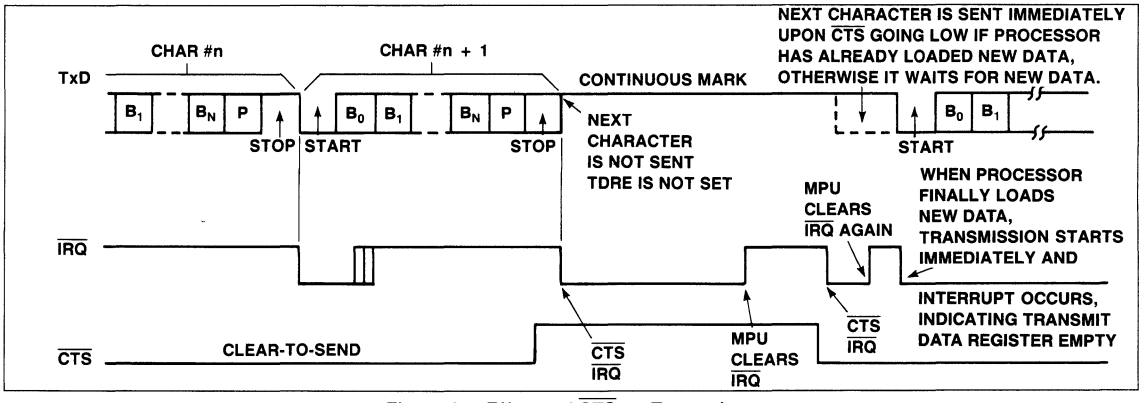


Figure 9. Effects of $\overline{CTS}$ on Transmitter

EFFECTS OF OVERRUN ON RECEIVER

If the processor does not read the RDR before the stop bit of the next word, an overrun error occurs, the overrun bit is set in the ISR, and the new data word is not transferred to the RDR. The RDR contains the last word not read by the MPU and all following data is lost. The receiver will return to normal operation when the RDR is read. Figure 10 shows the relation of $\overline{IRQ}$ and RxD for the effects of overrun on the receiver.

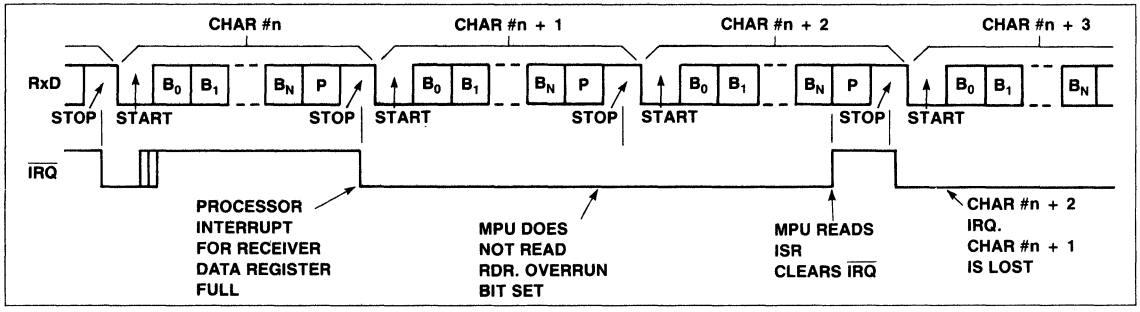


Figure 10. Effects of Overrun on Receiver

ECHO MODE TIMING

In the Echo Mode, the TxD line re-transmits the data received on the RxD line, delayed by 1/2 of a bit time. An internal underrun mode must occur before Echo Mode will start transmitting. In normal transmit mode if TDRE occurs (indicating end of data) an underflow flag would be set and continuous Mark transmitted. If Echo is initiated, the underflow flag will not be set at end of data and continuous Mark will not be transmitted. Figure 11 shows the relationship of RxD and TxD for Echo Mode.

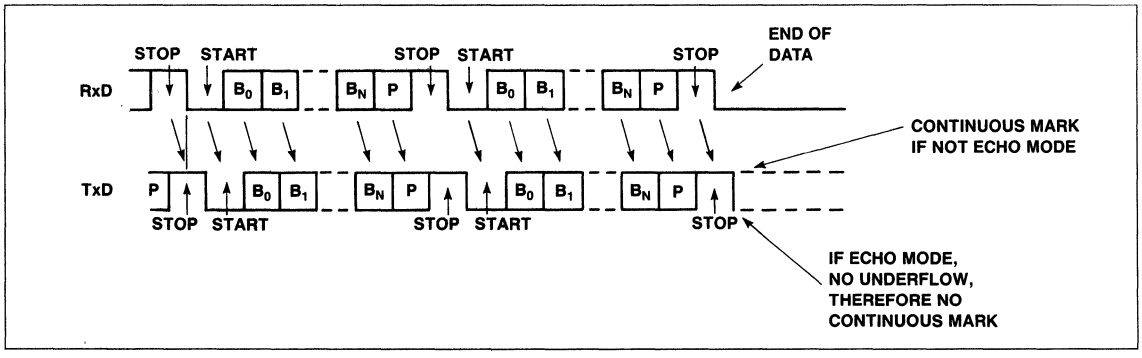


Figure 11. Echo Mode Timing

FRAMING ERROR

Framing error is caused by the absence of stop bit(s) on received data. The framing error bit is set when the RDRF bit is set. Subsequent data words are tested separately, so the status bit always reflects the last data word received. Figure 12 shows the relationship of $\overline{IRQ}$ and RxD when a framing error occurs.

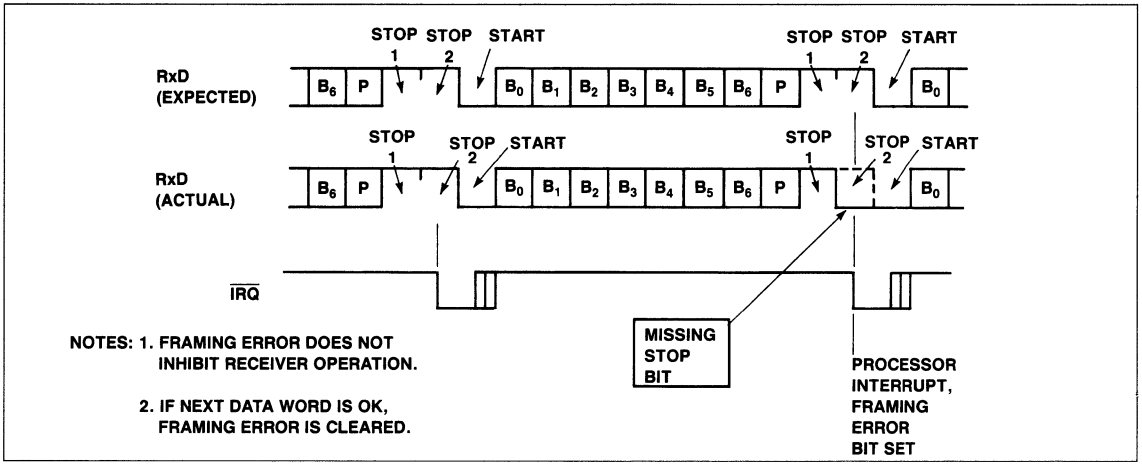


Figure 12. Framing Error

TRANSMIT BREAK CHARACTER

A Break may be transmitted by storing a value of $00 in the IER. After storing zero in the IER the Break is transmitted immediately. Care should be exercised so that a character in transmission is not disturbed inadvertently. The Break level lasts until other than $00 is stored in the IER at which time a stop bit is sent and transmission may resume. At least one full word time of Break will be sent regardless of the length of time between starting and stopping the Break character. Figure 13 shows the relationship of $\overline{IRQ}$ and TxD for a Transmit Break character.

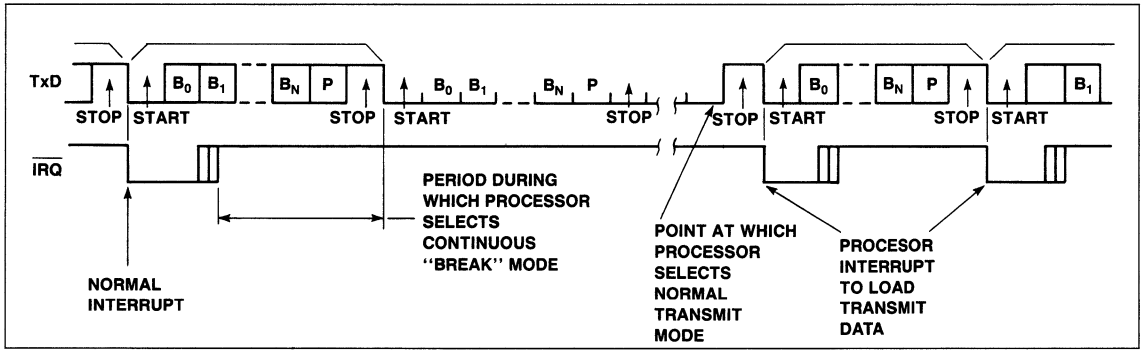


Figure 13. Transmit Break Character

Table 4. Divisor Selection

Control Register Bits				Divisor Selected For The Internal Counter	Baud Rate Generated With 3.6864 MHz Crystal	Baud Rate Generated With a Crystal of Frequency (f)
3	2	1	0			
0	0	0	0	73,728	$(3.6864 \times 10^6)/73,728 = 50$	f/73,728
0	0	0	1	33,538	$(3.6864 \times 10^6)/33,538 = 109.92$	f/33,538
0	0	1	0	27,408	$(3.6864 \times 10^6)/27,408 = 134.58$	f/27,408
0	0	1	1	24,576	$(3.6864 \times 10^6)/24,576 = 150$	f/24,576
0	1	0	0	12,288	$(3.6864 \times 10^6)/12,288 = 300$	f/12,288
0	1	0	1	6,144	$(3.6864 \times 10^6)/6,144 = 600$	f/6,144
0	1	1	0	3,072	$(3.6864 \times 10^6)/3,072 = 1,200$	f/3,072
0	1	1	1	2,048	$(3.6864 \times 10^6)/2,048 = 1,800$	f/2,048
1	0	0	0	1,536	$(3.6864 \times 10^6)/1,536 = 2,400$	f/1,536
1	0	0	1	1,024	$(3.6864 \times 10^6)/1,024 = 3,600$	f/1,024
1	0	1	0	768	$(3.6864 \times 10^6)/768 = 4,800$	f/768
1	0	1	1	512	$(3.6864 \times 10^6)/512 = 7,200$	f/512
1	1	0	0	384	$(3.6864 \times 10^6)/384 = 9,600$	f/384
1	1	0	1	192	$(3.6864 \times 10^6)/192 = 19,200$	f/192
1	1	1	0	96	$(3.6864 \times 10^6)/96 = 38,400$	f/96
1	1	1	1	16	TxC/16 = Baud Rate or RxC/16 = Baud Rate	

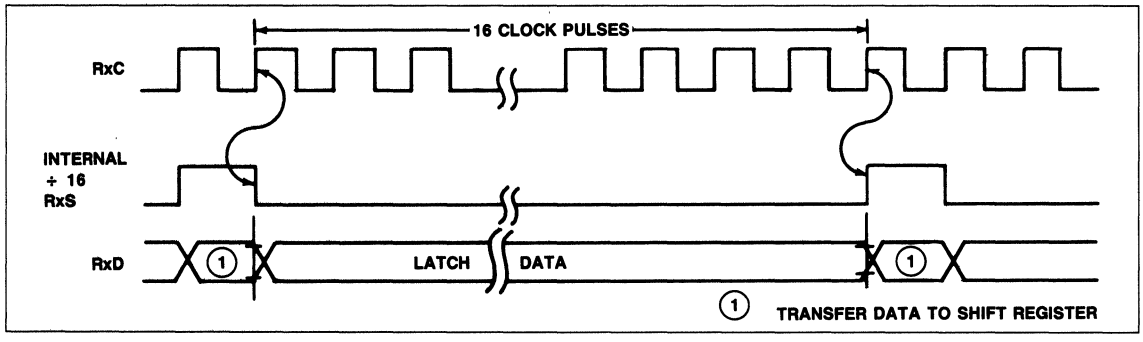


Figure 15. DACIA External Clock Timing — Receive Data

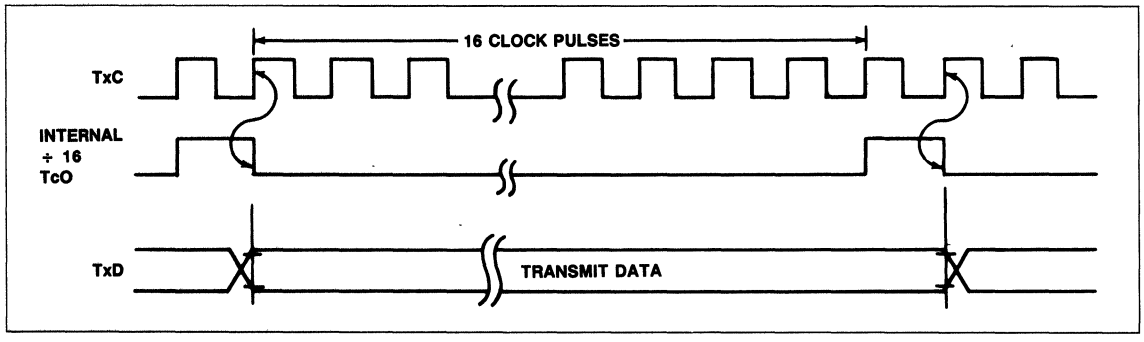


Figure 16. DACIA External Clock Timing — Transmit Data

RECEIVE BREAK CHARACTER

In the event that a Break character is received by the receiver, the Break bit is set. The receiver does not set the RDRF bit and remains in this state until a stop bit is received. At this time the next character is to be received normally. Figure 14 shows the relationship of $\overline{IRQ}$ and RxD for a Receive Break Character.

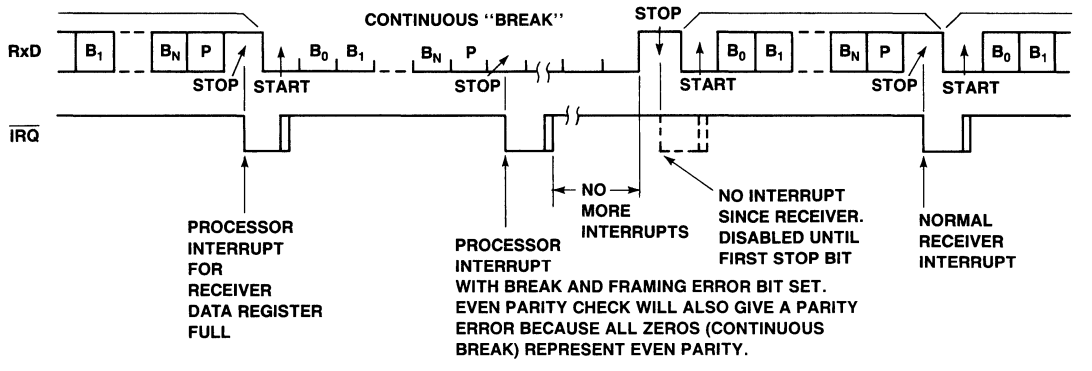


Figure 14. Receive Break Character

AUTOMATIC ADDRESS RECOGNITION

The DACIA offers a unique solution to the standard problem associated with multi-drop environment UARTs and communication interface controllers. In the standard configuration used by other devices, the slave CPU must be constantly interrupted to analyze incoming characters on the communications net to determine if an address word is present and if so, does that address match the address assigned to the slave UART. This CPU interrupt scheme can become intolerable in very large multi-drop networks because every slave on the communications net must "wake-up" it's CPU for every character sent down the network by the master. The end results is that the CPUs on the communications net are constantly being interrupted for the mundane task of address recognition.

To avoid this constant CPU interrupt problem, the DACIA has been designed to do address comparison and recognition internally without the need for CPU intervention. Therefore, the slave CPU is not interrupted until the DACIA has determined that the character sent over the communications net by the master was an address and the address matched the address stored in the DACIA Compare Register. At this point the DACIA interrupts the CPU, goes out of Compare Mode, and receives the string of characters being transmitted by the master, (i.e., the data characters). When all data has been received by the slave, it's CPU must again write the slave address into the DACIA Compare Register which automatically puts it back into the Compare Mode, waiting for another address character.

GENERATION OF NON-STANDARD BAUD RATES

Divisors

The internal counter/divider circuit selects the appropriate divisor for the crystal frequency by means of bits 0-3 of the CFR Control Register, as shown in Table 4.

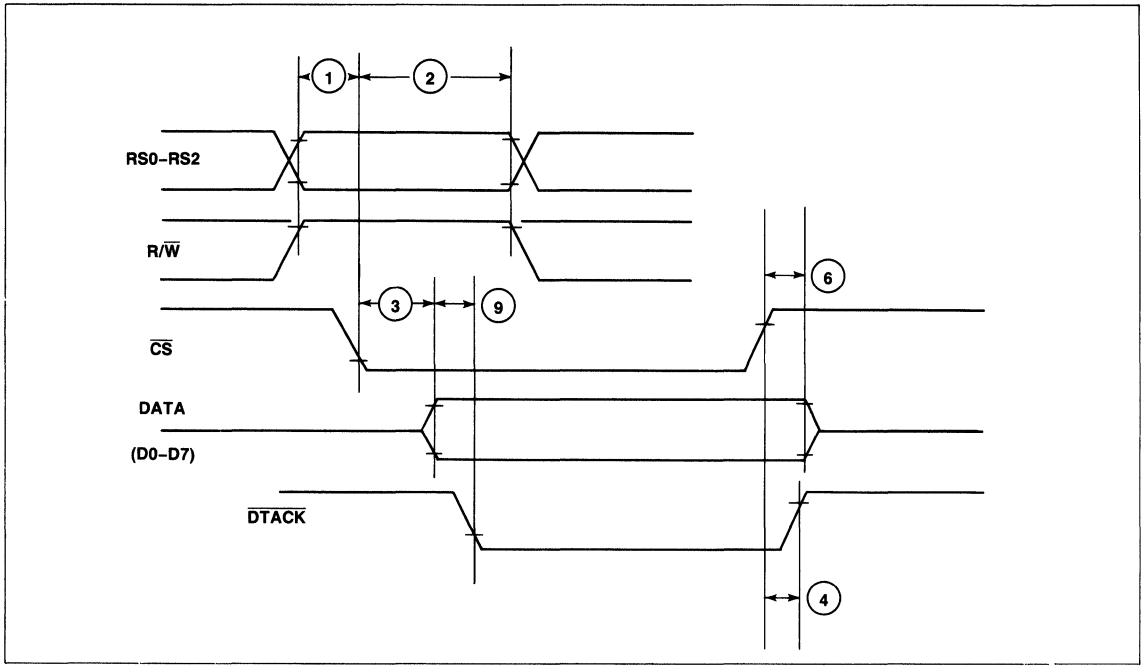
Generating Other Baud Rates

By using a different crystal, other baud rates may be generated.

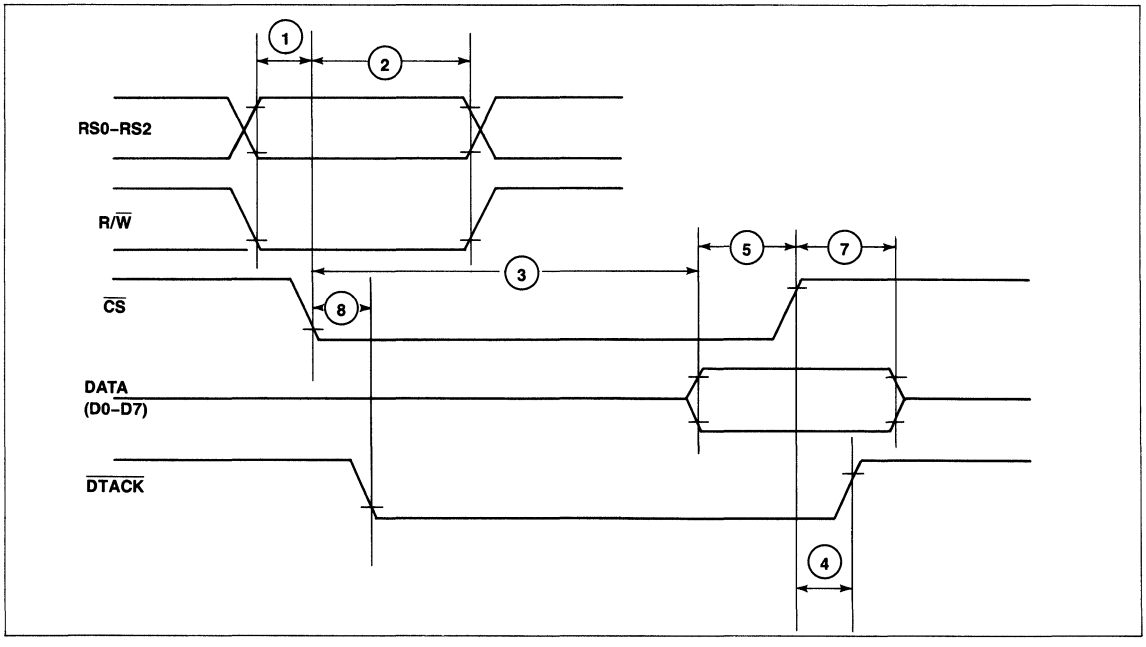
These can be determined by:

$$\text{Baud Rate} = \frac{\text{Crystal Frequency}}{\text{Divisor}}$$

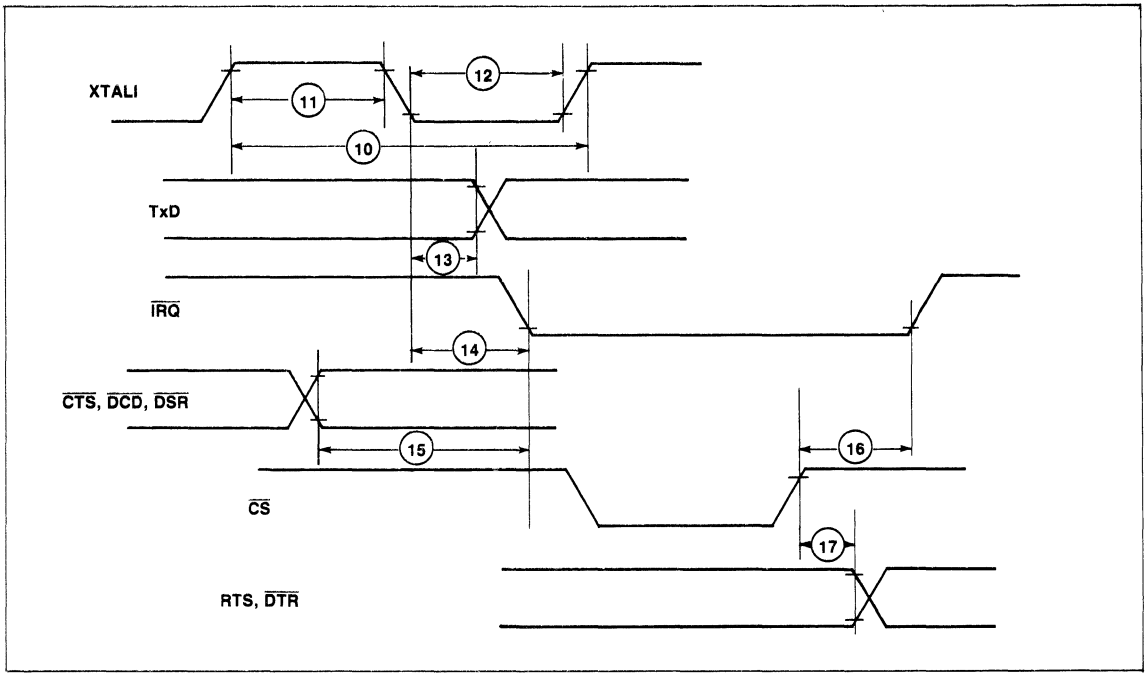
Furthermore, it is possible to drive the DACIA with an off-chip oscillator to achieve other baud rates. In this case, XTALI (pin 3) must be the clock input and XTALO (pin 4) must be a nonconnect.



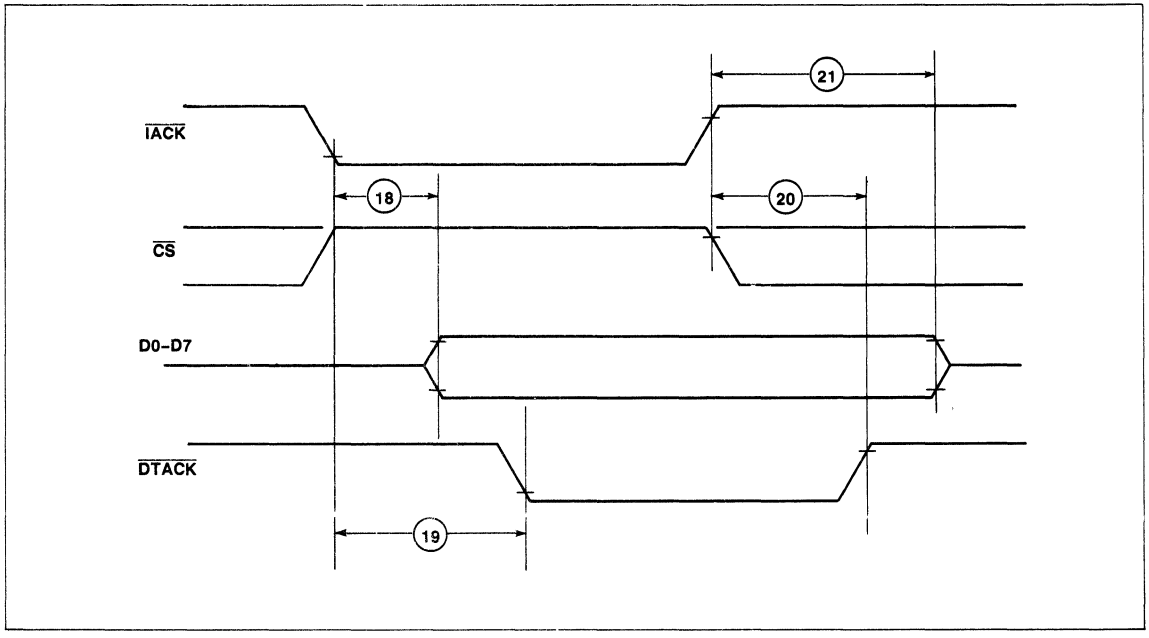
DACIA Read Cycle Timing



DACIA Write Cycle Timing



DACIA Transmit/Receiver Timing



DACIA Interrupt Acknowledge Timing

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to +7.0	Vdc
Input Voltage	V_{IN}	−0.3 to V_{CC} +0.3	Vdc
Output Voltage	V_{OUT}	−0.3 to V_{CC} +0.3	Vdc
Operating Temperature Commercial Industrial	T_A	 0 to +70 −40 to +85	°C
Storage Temperature	T_{STG}	−55 to +150	°C

***NOTE:** Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in other sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING CONDITIONS

Parameter	Symbol	Value
Supply Voltage	V_{CC}	5V ± 5%
Temperature Range Commercial Industrial	T_A	 0 to 70°C −40°C to +85°C

DC CHARACTERISTICS

(V_{CC} = 5.0 V ±5%, V_{SS} = 0, T_A = T_L to T_H, unless otherwise noted)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input High Voltage Except XTALI and XTALO XTALI and XTALO	V_{IH}	 +2.0 +2.4	 — —	 V_{CC} + 0.3 V_{CC} + 0.3	V	
Input Low Voltage Except XTALI and XTALO XTALI and XTALO	V_{IL}	 −0.3 −0.3	 — —	 +0.8 +0.4	V	
Input Leakage Current R/W, RES, RS0, RS1, RS2, RxD, CTS, DCD, DSR, RxC, TxC, CS, IACK	I_{IN}	—	10	50	μA	V_{IN} = 0V to 5.0V V_{CC} = 5.25V
Input Leakage Current for Three-State Off D0–D7	I_{TSI}	 —	 ±2	 10	μA	V_{IN} = 0.4V to 2.4V V_{CC} = 5.25V
Output High Voltage D0–D7, TxD, CLK OUT, RTS, DTR	V_{OH}	+2.4 1.5	— —	— —	V	V_{CC} = 4.75V I_{LOAD} = −100 μA
Output Low Voltage D0–D7, TxD, CLK OUT, RTS', DTR	V_{OL}	—	—	+0.4	V	V_{CC} = 4.75V I_{LOAD} = 1.6 mA
Output Leakage Current (Off State) IRQ, DTACK	I_{OFF}	 —	 ±2	 ±10	μA	V_{CC} = 5.25V V_{OUT} = 0 to 2.4V
Power Dissipation	P_D	—	—	10	mW/MHz	
Input Capacitance Except XTALI and XTALO XTALI and XTALO	C_{IN}	 — —	 — —	 5 10	 pF pF	V_{CC} = 5.0V V_{IN} = 0V f = 2 MHz T_A = 25°C
Output Capacitance	C_{OUT}	—		10	pF	

Notes:
1. All units are direct current (dc) except for capacitance.
2. Negative sign indicates outward current flow, positive indicates inward flow.
3. Typical values are shown for V_{CC} = 5.0V and T_A = 25°C.

SPECIFICATIONS

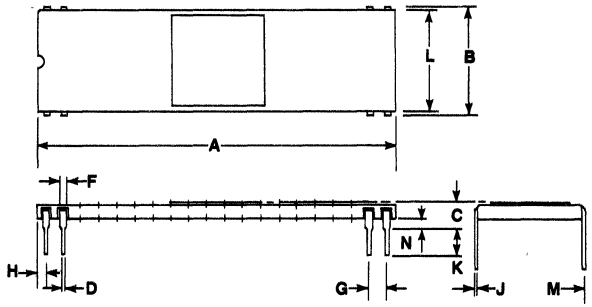
AC CHARACTERISTICS

(V_{CC} = 5 Vdc ± 5%, V_{SS} = 0 Vdc, T_A = T_L to T_H, unless otherwise noted)

Number	Characteristic	Symbol	Min.	Max.	Unit
READ/WRITE TIMING					
1	R/$\overline{W}$, RS0–RS2 Valid to $\overline{CS}$ Low (Setup)	t_{RVCL}	0	—	ns
2	$\overline{CS}$ Low to R/$\overline{W}$, RS0–RS2 Read (Hold Time)	t_{CLRV}	65	—	ns
3	$\overline{CS}$ Low to Data Valid	t_{CLDV}	—	100	ns
4	$\overline{CS}$ High to $\overline{DTACK}$ High	t_{CHTH}	0	40	ns
5	Data Valid to $\overline{CS}$ High	t_{DVCH}	20	—	ns
6	$\overline{CS}$ High to Data Invalid (Read)	t_{CHDZ}	10	30	ns
7	$\overline{CS}$ High to Data Invalid (Write)	t_{CHDZ}	0	40	ns
8	$\overline{CS}$ Low to $\overline{DTACK}$ Low (Write)	t_{CLTL}	0	—	ns
9	Data Valid to $\overline{DTACK}$ Low (Read)	t_{DVTL}	0	—	ns
TRANSMIT/RECEIVE TIMING					
10	Transmit/Receive Clock Rate	t_{CY}	250	—	ns
11	Transmit/Receive Clock High	t_{CH}	100	—	ns
12	Transmit/Receive Clock Low	t_{LL}	100	—	ns
13	XTALI to TxD Propagation Delay	t_{CLTD}	—	250	ns
14	XTALI to $\overline{IRQ}$ Propagation Delay	t_{CLID}	—	250	ns
15	$\overline{CTS}$, $\overline{DCD}$, $\overline{DSR}$ Valid to $\overline{IRQ}$ Low	t_{SVIL}	—	150	ns
16	$\overline{IRQ}$ Propagation Delay (Clear)	t_{IRQC}	—	150	ns
17	$\overline{RTS}$, $\overline{DTR}$ Propagation Delay	t_{RDPD}	—	150	ns
INTERRUPT ACKNOWLEDGE TIMING					
18	$\overline{IACK}$ Low to Data Valid	t_{ILDV}	—	100	ns
19	$\overline{IACK}$ Low to $\overline{DTACK}$ Low	t_{ILTL}	0	—	ns
20	$\overline{IACK}$ High to $\overline{DTACK}$ High	t_{IHTH}	0	—	ns
21	$\overline{IACK}$ High to Data Invalid	t_{IHDZ}	10	30	ns

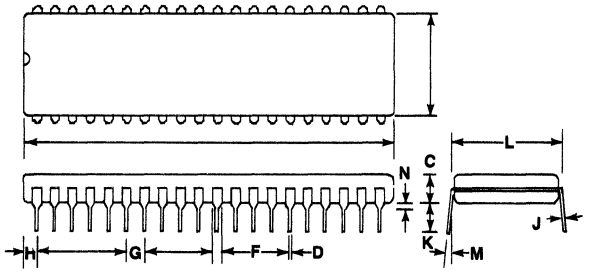
PACKAGE DIMENSIONS

40-PIN CERAMIC DIP



DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	50.29	51.31	1.980	2.020
B	14.86	15.62	0.585	0.615
C	2.54	4.19	0.100	0.165
D	0.38	0.53	0.015	0.021
F	0.76	1.40	0.030	0.055
G	2.54 BSC		0.100 BSC	
H	0.76	1.78	0.030	0.070
J	0.20	0.33	0.008	0.013
K	2.54	4.19	0.100	0.165
L	14.60	15.37	0.575	0.605
M	0°	10°	0°	10°
N	0.51	1.52	0.020	0.060

40-PIN PLASTIC DIP



DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	51.28	52.32	2.040	2.060
V	13.72	14.22	0.540	0.560
C	3.55	5.08	0.140	0.200
D	0.36	0.51	0.014	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.30	0.008	0.012
K	3.05	3.56	0.120	0.140
L	15.24 BSC		0.600 BSC	
M	7°	10°	7°	10°
N	0.51	1.02	0.020	0.040

SECTION 2
8-BIT MICROPROCESSORS AND PERIPHERALS

2

R6500 MICROPROCESSOR AND PERIPHERAL FAMILY
Fastest Executing, Largest Selling 8-Bit Family Now Also In CMOS

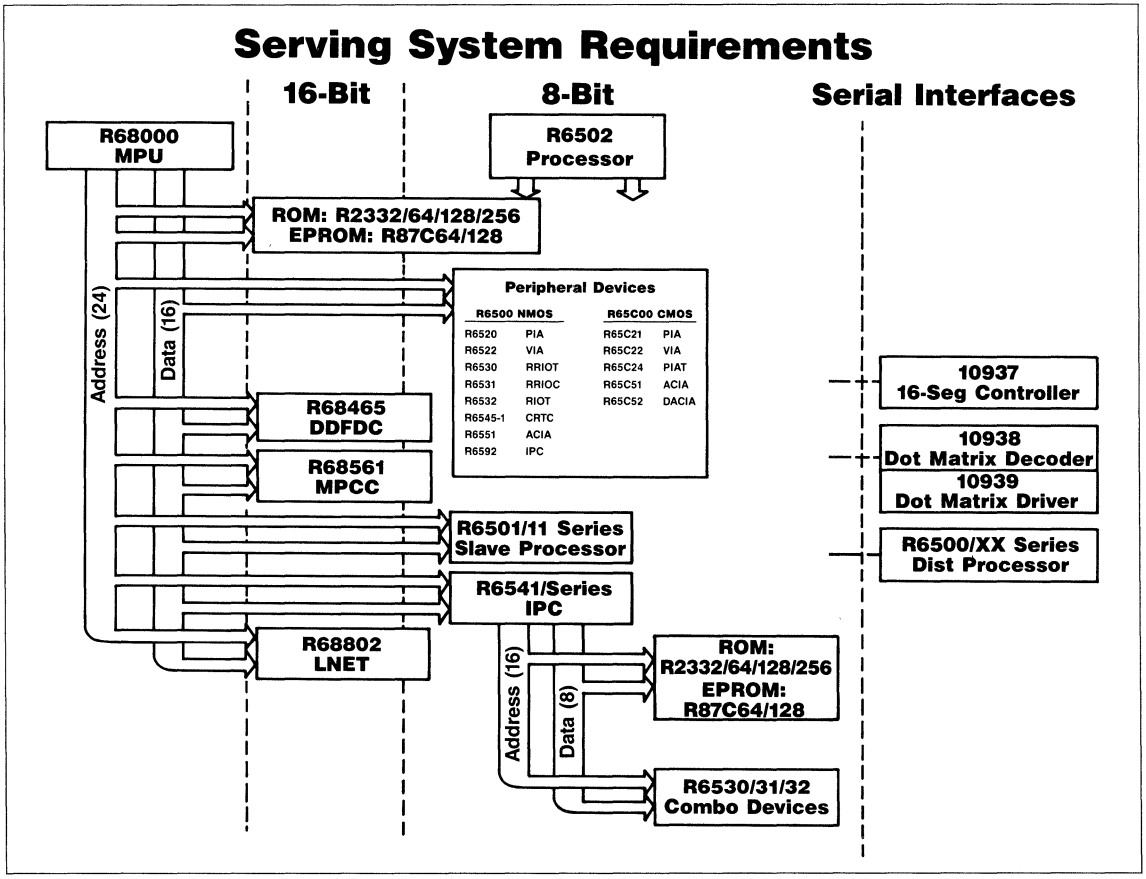
There is no microprocessor family easier to implement than the R6500. It's the fastest instruction executing 8-bit family. It's software compatible with a family of single-chip microcomputers and available in NMOS and CMOS versions. It has a wide variety of CPUs and peripheral controllers and versatile memory-I/O-timer combinations.

In the 8-bit range, nothing gives higher performance than this third generation microprocessor family. Pipeline architecture provides much faster instruction execution (1μsec). Thirteen address modes provide the most efficient ways of addressing memory. R6500 peripherals are system oriented, designed to implement systems with minimum chips.

And now, it's available in CMOS, for even higher speed, low power applications—the R65C00 family. It's now possible to move complete product and system designs directly into CMOS, being downward software compatible with the NMOS R6500 family.

Because of its inherent characteristics, the advanced Rockwell CMOS provides low power consumption, high noise immunity and high speed operation. Its 2 MHz CPU dissipates only 40 mW (compared to 700-800 mW in NMOS) and requires only 10 μA standby current. Instructions can be executed in only 500 nanoseconds. Instruction memory requirements are 20% less due to added bit manipulation features. And, there are even more advantages.

The entire 8-bit R6500 family is upward compatible with the 16-bit R68000 bus, software compatible to the R6500/* single-chip microcomputers and are the building blocks for for a wide range of system applications. There's no wonder it's one of the world's largest selling families of microprocessors.



Rockwell

R650X and R651X MICROPROCESSORS (CPU)

DESCRIPTION

The 8-bit R6500 microprocessor devices are produced with N-channel, silicon gate technology. Its performance speeds are enhanced by advanced system architecture. This innovative architecture results in smaller chips—the semiconductor threshold is cost-effectivity. System cost-effectivity is further enhanced by providing a family of 10 software-compatible microprocessor (CPU) devices, described in this document. Rockwell also provides single chip microcomputers, memory and peripheral devices—as well as low-cost design aids and documentation.

Ten CPU devices are available. All are software-compatible. They provide options of addressable memory, interrupt input, on-chip clock oscillators and drivers. All are bus-compatible with earlier generation microprocessors like the M6800 devices.

The R650X and R651X family includes six microprocessors with on-board clock oscillators and drivers and four microprocessors driven by external clocks. The on-chip clock versions are aimed at high performance, low cost applications where single phase inputs, crystal or RC inputs provide the time base. The external clock versions are geared for multiprocessor system applications where maximum timing control is mandatory. All R6500 microprocessors are also available in a variety of packaging (ceramic and plastic), operating frequency (1 MHz, 2 MHz and 3 MHz) and temperature (commercial and industrial) versions.

ORDERING INFORMATION

Part Number: R65XX___

- Temperature Range (T_L to T_H):
  - No letter = 0°C to +70°C
  - E = −40°C to +85°C
- Package
  - C = Ceramic
  - P = Plastic
- Frequency Range:
  - No letter = 1 MHz
  - A = 2 MHz
  - B = 3 MHz
- Model Designator*
  - XX = 02, 03, 04, 15

FEATURES

- N-channel, silicon gate, depletion load technology
- 8-bit parallel processing
- 56 instructions
- Decimal and binary arithmetic
- Thirteen addressing modes
- True indexing capability
- Programmable stack pointer
- Variable length stack
- Interrupt request
- Non-maskable interrupt
- Use with any type of speed memory
- 8-bit bidirectional data bus
- Addressable memory range of up to 64K bytes
- "Ready" input
- Direct Memory Access capability
- Bus compatible with M6800
- 1 MHz, 2 MHz, and 3 MHz versions
- Choice of external or on-chip clocks
- On-chip clock options
  - —External single clock input
  - —Crystal time base input
- Commercial and industrial temperature versions
- Pipeline architecture
- Single +5V supply

R6500 CPU FAMILY MEMBERS

Microprocessors with Internal Two Phase Clock Generator

Model	No. Pins	Addressable Memory
R6502	40	64K Bytes
R6503	28	4K Bytes
R6504	28	8K Bytes
R6505	28	4K Bytes
R6506	28	4K Bytes
R6507	28	8K Bytes

Microprocessors with External Two Phase Clock Input

Model	No. Pins	Addressable Memory
R6512	40	64K Bytes
R6513	28	4K Bytes
R6514	28	8K Bytes
R6515	28	4K Bytes

INTERFACE SIGNAL DESCRIPTIONS

CLOCKS (Ø1, Ø2)

The R651X requires a two phase non-overlapping clock that runs at the V_{CC} voltage level. The R650X clocks are supplied with an internal clock generator. The frequency of these clocks is externally controlled.

ADDRESS BUS (A0-A15, R6502)

The address line outputs access data in memory device locations or cells, access data in I/O device registers and/or effect logical operations in I/O or controller devices depending on system design. The addressing range is determined by the number of address lines available on the particular CPU device. The R6502 and R6512 can address 64K bytes with a 16-bit address bus (A0-A15); the R6504, R6507, and the R6514 can address 8K bytes with a 13-bit address bus (A0-A12); and the R6503, R6505, R6506, R6513, and R6515 can address 4K bytes with a 12-bit address bus (A0-A11). These outputs are TTL-compatible and are capable of driving one standard TTL load and 130 pF.

DATA BUS (D0-D7)

The data lines (D0-D7) form an 8-bit bidirectional data bus which transfers data between the CPU and memory or peripheral devices. The outputs are tri-state buffers capable of driving one standard TTL load and 130 pF.

DATA BUS ENABLE (DBE, R6512 ONLY)

The TTL-compatible DBE input allows external control of the tri-state data output buffers and will enable the microprocessor bus driver when in the high state. In normal operation DBE is driven by the phase two (Ø2) clock, thus allowing data output from microprocessor only during Ø2. During the read cycle, the data bus drivers are internally disabled, becoming essentially an open circuit. To disable data bus drivers externally, DBE should be held low.

READY (RDY)

The Ready input signal allows the user to halt or single cycle the microprocessor on all cycles except write cycles. A negative transition to the low state during or coincident with phase one (Ø1) will halt the microprocessor with the output address lines reflecting the current address being fetched. If Ready is low during a write cycle, it is ignored until the following read operation. This condition will remain through a subsequent phase two (Ø2) in which the Ready signal is low. This feature allows microprocessor interfacing with the low speed PROMs as well as Direct Memory Access (DMA).

INTERRUPT REQUEST ($\overline{IRQ}$)

The TTL level active-low $\overline{IRQ}$ input requests that an interrupt sequence begin within the microprocessor. The microprocessor will complete the current instruction being executed before recognizing the request. At that time, the interrupt mask bit in the Processor Status Register will be examined. If the interrupt mask flag is not set, the microprocessor will begin an interrupt sequence. The Program Counter and Processor Status Register are stored in the stack. The microprocessor will then set the interrupt mask flag high so that no further interrupts can occur. At the end of this cycle, the program counter low will be loaded from address FFFE, and program counter high from location FFFF, therefore transferring program control to the memory vector located at these addresses. The RDY signal must be in the high state for any interrupt to be recognized. A 3KΩ external resistor should be used for proper wire-OR operation.

NON-MASKABLE INTERRUPT ($\overline{NMI}$)

A negative going edge on the $\overline{NMI}$ input requests that a non-maskable interrupt sequence be generated within the microprocessor.

$\overline{NMI}$ is an unconditional interrupt. Following completion of the current instruction, the sequence of operations defined for $\overline{IRQ}$ will be performed, regardless of the state interrupt mask flag. The vector address loaded into the program counter, low and high, are locations FFFA and FFFB respectively, thereby transferring program control to the memory vector located at these addresses. The instructions loaded at these locations cause the microprocessor to branch to a non-maskable interrupt routine in memory.

$\overline{NMI}$ also requires an external 3KΩ register to V_{CC} for proper wire-OR operations.

Inputs $\overline{IRQ}$ and $\overline{NMI}$ are hardware interrupts lines that are sampled during Ø2 (phase 2) and will begin the appropriate interrupt routine on the Ø1 (phase 1) following the completion of the current instruction.

SET OVERFLOW FLAG ($\overline{SO}$)

A negative going edge on the $\overline{SO}$ input sets the overflow bit in the Processor Status Register. This signal is sampled on the trailing edge of Ø1 and must be externally synchronized.

SYNC

The SYNC output line identifies those cycles in which the microprocessor is doing an OP CODE fetch. The SYNC line goes high during Ø1 of an OP CODE fetch and stays high for the remainder of that cycle. If the RDY line is pulled low during the Ø1 clock pulse in which SYNC went high, the processor will stop in its current state and will remain in the state until the RDY line goes high. In this manner, the SYNC signal can be used to control RDY to cause single instruction execution.

RESET ($\overline{RES}$)

The active low $\overline{RES}$ resets, or starts, the microprocessor from a power down or restart condition. During the time that this line is held low, writing to or from the microprocessor is inhibited. When a positive edge is detected on the input, the microprocessor will immediately begin the reset sequence.

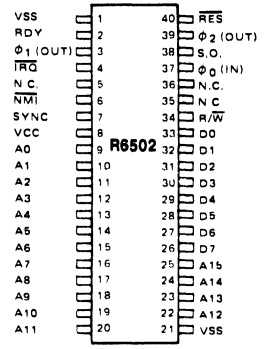
After a system initialization time of six clock cycles, the mask interrupt flag is set and the microprocessor loads the program counter from the memory vector locations FFFC and FFFD. This is the start location for program control.

After V_{CC} reaches 4.75 volts in a power up routine, reset must be held low for at least two clock cycles. At this time the R/$\overline{W}$ and SYNC signals become valid.

2

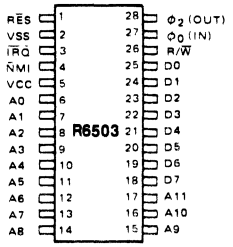
R6502 FEATURES

- 64K addressable bytes of memory (A0-A15)
- $\overline{IRQ}$ interrupt
- On-chip clock
  TTL-level single phase input
  RC time base input
  crystal time base input
- SYNC signal
  (can be used for single instruction execution)
- RDY signal
  (can be used to halt or single cycle execution)
- Two phase output clock for timing of support chips
- $\overline{NMI}$ interrupt
- 40-pin DIP



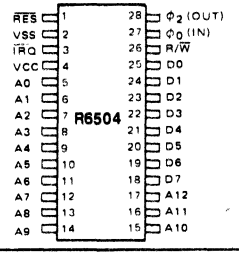
R6503 FEATURES

- 4K addressable bytes of memory (A0-A11)
- On-chip clock
- $\overline{IRQ}$ interrupt
- $\overline{NMI}$ interrupt
- 8-bit bidirectional data bus
- 28-pin DIP



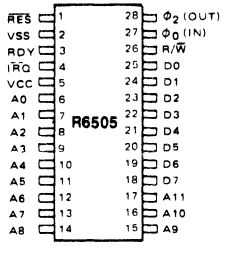
R6504 FEATURES

- 8K addressable bytes of memory (A0-A12)
- On-chip clock
- $\overline{IRQ}$ interrupt
- 8-bit bidirectional data bus
- 28-pin DIP



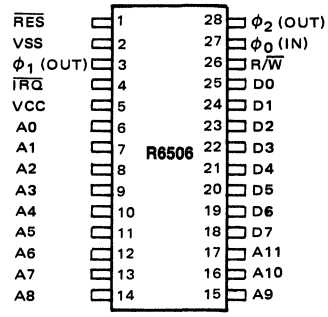
R6505 FEATURES

- 4K addressable bytes of memory (A0-A11)
- On-chip clock
- $\overline{IRQ}$ interrupt
- RDY signal
- 8-bit bidirectional data bus
- 28-pin DIP



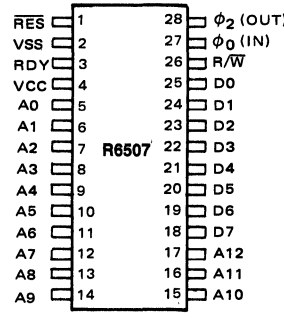
R6506 FEATURES

- 4K addressable bytes of memory (A0-A11)
- On-chip clock
- $\overline{IRQ}$ interrupt
- Two phase output clock for timing of support chips
- 8-bit bidirectional data bus
- 28-pin DIP



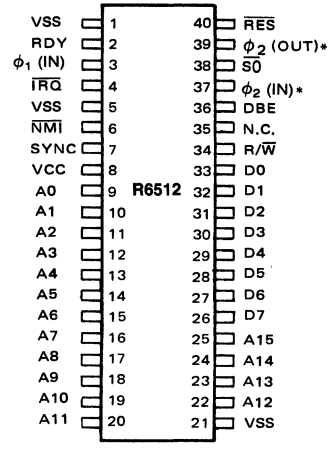
R6507 FEATURES

- 8K addressable bytes of memory (A0-A12)
- On-chip clock
- RDY signal
- 8-bit bidirectional data bus
- 28-pin DIP



R6512 FEATURES

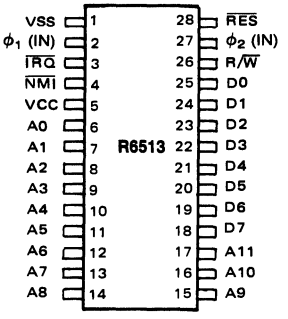
- 64K addressable bytes of memory (A0-A15)
- $\overline{IRQ}$ interrupt
- $\overline{NMI}$ interrupt
- RDY signal
- 8-bit bidirectional data bus
- SYNC signal
- Two phase clock input
- Data Bus Enable
- 40-pin DIP



*Pins 37 and 39 are connected internally

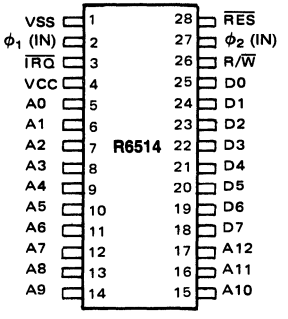
R6513 FEATURES

- 4K addressable bytes of memory (A0-A11)
- Two phase clock input
- $\overline{IRQ}$ interrupt
- $\overline{NMI}$ interrupt
- 8-bit bidirectional data bus
- 28-pin DIP



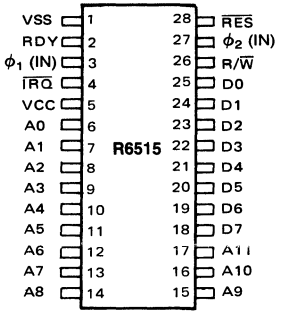
R6514 FEATURES

- 8K addressable bytes of memory (A0-A12)
- Two phase clock input
- $\overline{IRQ}$ interrupt
- 8-bit bidirectional data bus



R6515 FEATURES

- 4K addressable bytes of memory (A0-A11)
- Two phase clock input
- $\overline{IRQ}$ interrupt
- RDY signal
- 8-bit bidirectional data bus



FUNCTIONAL DESCRIPTION

The internal organization of all R6500 CPUs is identical except for some variations in clock interface, the number of address output lines, and some unique input/output lines between versions.

CLOCK GENERATOR

The clock generator develops all internal clock signals, and (where applicable) external clock signals, associated with the device. It is the clock generator that drives the timing control unit and the external timing for slave mode operations.

TIMING CONTROL

The timing control unit keeps track of the instruction cycle being monitored. The unit is set to zero each time an instruction fetch is executed and is advanced at the beginning of each phase one clock pulse for as many cycles as is required to complete the instruction. Each data transfer which takes place between the registers depends upon decoding the contents of both the instruction register and the timing control unit.

PROGRAM COUNTER

The 16-bit program counter provides the addresses which step the microprocessor through sequential instructions in a program.

Each time the microprocessor fetches an instruction from program memory, the lower byte of the program counter (PCL) is placed on the low-order bits of the address bus and the higher byte of the program counter (PCH) is placed on the high-order 8 bits. The counter is incremented each time an instruction or data is fetched from program memory.

INSTRUCTION REGISTER AND DECODE

Instructions fetched from memory are gated onto the internal data bus. These instructions are latched into the instuction register, then decoded, along with timing and interrupt signals, to generate control signals for the various registers.

ARITHMETIC AND LOGIC UNIT (ALU)

All arithmetic and logic operations take place in the ALU including incrementing and decrementing internal registers (except the program counter). The ALU has no internal memory and is used only to perform logical and transient numerical operations.

ACCUMULATOR

The accumulator is a general purpose 8-bit register that stores the results of most arithmetic and logic operations, and in addition, the accumulator usually contains one of the two data words used in these operations.

INDEX REGISTERS

There are two 8-bit index registers (X and Y), which may be used to count program steps or to provide an index value to be used in generating an effective address.

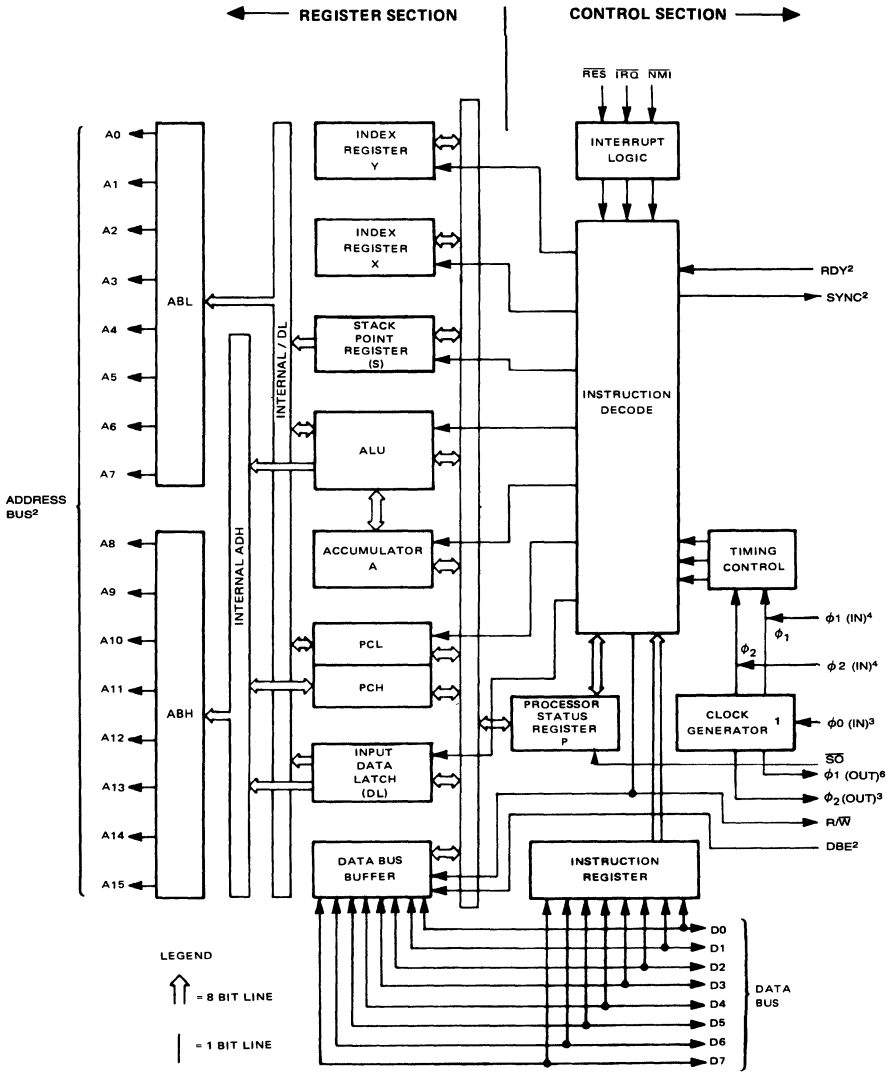
When executing an instruction which specifies indexed addressing, the CPU fetches the op code and the base address, and modifies the address by adding the index register to it prior to performing the desired operation. Pre- or post-indexing of indirect addresses is possible (see addressing modes).

STACK POINTER

The stack pointer is an 8-bit register used to control the addressing of the variable-length stack on page one. The stack pointer is automatically incremented and decremented under control of the microprocessor to perform stack manipulations under direction of either the program or interrupts ($\overline{NMI}$) and $\overline{IRQ}$). The stack allows simple implementation of nested subroutines and multiple level interrupts. The stack pointer should be initialized before any interrupts or stack operations occur.

PROCESSOR STATUS REGISTER

The 8-bit processor status register contains seven status flags. Some of the flags are controlled by the program, others may be controlled both by the program and the CPU.



NOTE

1. **CLOCK GENERATOR IS NOT INCLUDED ON R6512, R6513, R6514 AND R6515.**
2. **ADDRESSING CAPABILITY AND CONTROL OPTIONS VARY WITH EACH OF THE CPUs.**
3. **R6502, R6503, R6504, R6505, R6506 AND R6507.**
4. **R6512, R6513, R6514 AND R6515.**
5. **R6512 ONLY.**
6. **R6502 ONLY.**

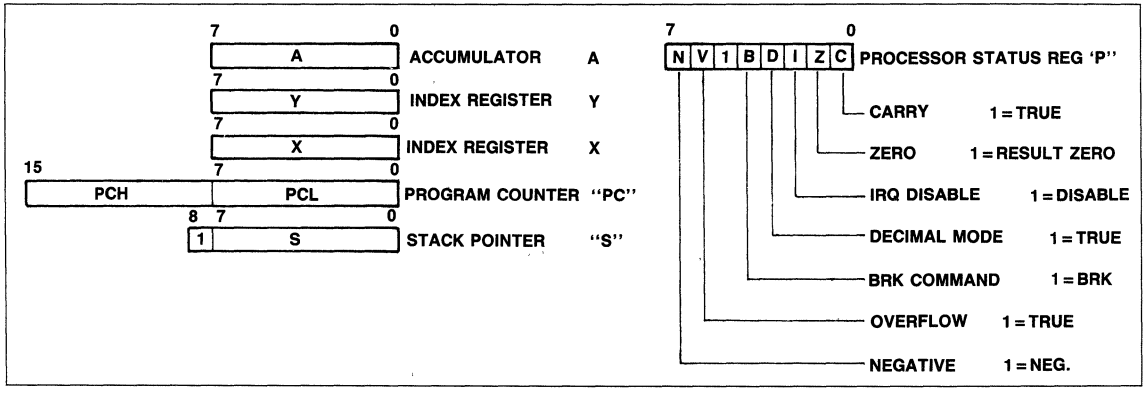
R650X and R651X Internal Architecture

INSTRUCTION SET

The R6500 CPU has 56 instruction types which are enhanced by up to 13 addressing modes for each instruction. The accumulator, index registers, Program Counter, Stack Pointer and Processor Status Register are illustrated below.

Alphabetic Listing of Instruction Set

Mnemonic	Function	Mnemonic	Function
ADC	Add Memory to Accumulator with Carry	JMP	Jump to New Location
AND	"AND" Memory with Accumulator	JSR	Jump to New Location Saving Return Address
ASL	Shift Left One Bit (Memory or Accumulator)		
		LDA	Load Accumulator with Memory
BCC	Branch on Carry Clear	LDX	Load Index X with Memory
BCS	Branch on Carry Set	LDY	Load Index Y with Memory
BEQ	Branch on Result Zero	LSR	Shift One Bit Right (Memory or Accumulator)
BIT	Test Bits in Memory with Accumulator		
BMI	Branch on Result Minus	NOP	No Operation
BNE	Branch on Result not Zero		
BPL	Branch on Result Plus	ORA	"OR" Memory with Accumulator
BRK	Force Break		
BVC	Branch on Overflow Clear	PHA	Push Accumulator on Stack
BVS	Branch on Overflow Set	PHP	Push Processor Status on Stack
		PLA	Pull Accumulator from Stack
CLC	Clear Carry Flag	PLP	Pull Processor Status from Stack
CLD	Clear Decimal Mode		
CLI	Clear Interrupt Disable Bit	ROL	Rotate One Bit Left (Memory or Accumulator)
CLV	Clear Overflow Flag	ROR	Rotate One Bit Right (Memory or Accumulator)
CMP	Compare Memory and Accumulator	RTI	Return from Interrupt
CPX	Compare Memory and Index X	RTS	Return from Subroutine
CPY	Compare Memory and Index Y		
		SBC	Subtract Memory from Accumulator with Borrow
DEC	Decrement Memory by One	SEC	Set Carry Flag
DEX	Decrement Index X by One	SED	Set Decimal Mode
DEY	Decrement Index Y by One	SEI	Set Interrupt Disable Status
		STA	Store Accumulator in Memory
EOR	"Exclusive-OR" Memory with Accumulator	STX	Store Index X in Memory
		STY	Store Index Y in Memory
INC	Increment Memory by One		
INX	Increment Index X by One	TAX	Transfer Accumulator to Index X
INY	Increment Index Y by One	TAY	Transfer Accumulator to Index Y
		TSX	Transfer Stack Pointer to Index X
		TXA	Transfer Index X to Accumulator
		TXS	Transfer Index X to Stack Register
		TYA	Transfer Index Y to Accumulator



Programming Model

ADDRESSING MODES

The R6500 CPU family has 13 addressing modes. In the following discussion of these addressing modes, a bracketed expression follows the title of the mode. This expression is the term used in the Instruction Set Op Code Matrix table (later in this product description) to make it easier to identify the actual addressing mode used by the instruction.

ACCUMULATOR ADDRESSING [Accum]—This form of addressing is represented with a one byte instruction, implying an operation on the accumulator.

IMMEDIATE ADDRESSING [IMM]—In immediate addressing, the second byte of the instruction contains the operand, with no further memory addressing required.

ABSOLUTE ADDRESSING [Absolute]—In absolute addressing, the second byte of the instruction specifies the eight low order bits of the effective address while the third byte specifies the eight high order bits Thus, the absolute addressing mode allows access to the entire 64K bytes of addressable memory.

ZERO PAGE ADDRESSING [ZP]—The zero page instructions allow for shorter code and execution times by fetching only the second byte of the instruction and assuming a zero high address byte. Careful use of the zero page can result in significant increase in code efficiency.

INDEXED ZERO PAGE ADDRESSING [ZP, X or Y]—(X, Y indexing)—This form of addressing is used with the index register and is referred to as "Zero Page, X" or "Zero Page, Y". The effective address is calculated by adding the second byte to the contents of the index register Since this is a form of "Zero Page" addressing, the content of the second byte references a location in page zero. Additionally, due to the "Zero Page" addressing nature of this mode, no carry is added to the high order eight bits of memory and crossing of page boundaries does not occur.

INDEXED ABSOLUTE ADDRESSING [ABS, X or Y]—(X, Y indexing)—This form of addressing is used in conjunction with X and Y index register and is referred to as "Absolute, X" and "Absolute, Y". The effective address is formed by adding the contents of X or Y to the address contained in the second and third bytes of the instruction. This mode allows the index register to contain the index or count value and the instruction to contain the base address. This type of indexing allows any location referencing and the index to modify multiple fields, resulting in reduced coding and execution time.

IMPLIED ADDRESSING [Implied]—In the implied addressing mode, the address containing the operand is implicitly stated in the operation code of the instruction.

RELATIVE ADDRESSING [Relative]—Relative addressing is used only with branch instructions and establishes a destination for the conditional branch.

The second byte of the instruction becomes the operand which is an "Offset" added to the contents of the lower eight bits of the program counter when the counter is set at the next instruction. The range of the offset is −128 to +127 bytes from the next instruction

INDEXED INDIRECT ADDRESSING [(IND, X)]—In indexed indirect addressing (referred to as (Indirect, X)), the second byte of the instruction is added to the contents of the X index register, discarding the carry The result of this addition points to a memory location on page zero whose contents are the low order eight bits of the effective address. The next memory location in page zero contains the high order eight bits of the effective address. Both memory locations specifying the high and low order bytes of the effective address must be in page zero.

INDIRECT INDEXED ADDRESSING [(IND), Y]—In indirect indexed addressing (referred to as (Indirect), Y), the second byte of the instruction points to a memory location in page zero. The contents of this memory location are added to the contents of the Y index register, the result being the low order eight bits of the effective address. The carry from this addition is added to the contents of the next page zero memory location, the result being the high order eight bits of the effective address.

ABSOLUTE INDIRECT [Indirect]—The second byte of the instruction contains the low order eight bits of a memory location. The high order eight bits of that memory location are contained in the third byte of the instruction The contents of the fully specified memory location are the low order byte of the effective address. The next memory location contains the high order byte of the effective address which is loaded into the sixteen bits of the program counter. (JMP (IND) only)

INSTRUCTION SET OP CODE MATRIX

The following matrix shows the Op Codes associated with the R6500 family of CPU devices. The matrix identifies the hexadecimal code, the mnemonic code, the addressing mode, the number of instruction bytes, and the number of machine cycles associated with each Op Code. Also, refer to the instruction set summary for additional information on these Op Codes.

MSD \ LSD	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	MSD
0	BRK Implied 1 7	ORA (IND, X) 2 6				ORA ZP 2 3	ASL ZP 2 5		PHP Implied 1 3	ORA IMM 2 2	ASL Accum 1 2			ORA ABS 3 4	ASL ABS 3 6		0
1	BPL Relative 2 2**	ORA (IND), Y 2 5*				ORA ZP, X 2 4	ASL ZP, X 2 6		CLC Implied 1 2	ORA ABS, Y 3 4*				ORA ABS, X 3 4*	ASL ABS, X 3 7		1
2	JSR Absolute 3 6	AND (IND, X) 2 6			BIT ZP 2 3	AND ZP 2 3	ROL ZP 2 5		PLP Implied 1 4	AND IMM 2 2	ROL Accum 1 2		BIT ABS 3 4	AND ABS 3 4	ROL ABS 3 6		2
3	BMI Relative 2 2**	AND (IND), Y 2 5*				AND ZP, X 2 4	ROL ZP, X 2 6		SEC Implied 1 2	AND ABS, Y 3 4*				AND ABS, X 3 4*	ROL ABS, X 3 7		3
4	RTI Implied 1 6	EOR (IND, X) 2 6				EOR ZP 2 3	LSR ZP 2 5		PHA Implied 1 3	EOR IMM 2 2	LSR Accum 1 2		JMP ABS 3 3	EOR ABS 3 4	LSR ABS 3 6		4
5	BVC Relative 2 2**	EOR (IND), Y 2 5*				EOR ZP, X 2 4	LSR ZP, X 2 6		CLI Implied 1 2	EOR ABS, Y 3 4*				EOR ABS, X 3 4*	LSR ABS, X 3 7		5
6	RTS Implied 1 6	ADC (IND, X) 2 6				ADC ZP 2 3	ROR ZP 2 5		PLA Implied 1 4	ADC IMM 2 2	ROR Accum 1 2		JMP Indirect 3 5	ADC ABS 3 4	ROR ABS 3 6		6
7	BVS Relative 2 2**	ADC (IND), Y 2 5*				ADC ZP, X 2 4	ROR ZP, X 2 6		SEI Implied 1 2	ADC ABS, Y 3 4*				ADC ABS, X 3 4*	ROR ABS, X 3 7		7
8		STA (IND, X) 2 6			STY ZP 2 3	STA ZP 2 3	STX ZP 2 3		DEY Implied 1 2		TXA Implied 1 2		STY ABS 3 4	STA ABS 3 4	STX ABS 3 4		8
9	BCC Relative 2 2**	STA (IND), Y 2 6			STY ZP, X 2 4	STA ZP, X 2 4	STX ZP, Y 2 4		TYA Implied 1 2	STA ABS, Y 3 5	TXS Implied 1 2			STA ABS, X 3 5			9
A	LDY IMM 2 2	LDA (IND, X) 2 6	LDX IMM 2 2		LDY ZP 2 3	LDA ZP 2 3	LDX ZP 2 3		TAY Implied 1 2	LDA IMM 2 2	TAX Implied 1 2		LDY ABS 3 4	LDA ABS 3 4	LDX ABS 3 4		A
B	BCS Relative 2 2**	LDA (IND), Y 2 5*			LDY ZP, X 2 4	LDA ZP, X 2 4	LDX ZP, Y 2 4		CLV Implied 1 2	LDA ABS, Y 3 4*	TSX Implied 1 2		LDY ABS, X 3 4*	LDA ABS, X 3 4*	LDX ABS, Y 3 4*		B
C	CPY IMM 2 2	CMP (IND, X) 2 6			CPY ZP 2 3	CMP ZP 2 3	DEC ZP 2 5		INY Implied 1 2	CMP IMM 2 2	DEX Implied 1 2		CPY ABS 3 4	CMP ABS 3 4	DEC ABS 3 6		C
D	BNE Relative 2 2**	CMP (IND), Y 2 5*				CMP ZP, X 2 4	DEC ZP, X 2 6		CLD Implied 1 2	CMP ABS, Y 3 4*				CMP ABS, X 3 4*	DEC ABS, X 3 7		D
E	CPX IMM 2 2	SBC (IND, X) 2 6			CPX ZP 2 3	SBC ZP 2 3	INC ZP 2 5		INX Implied 1 2	SBC IMM 2 2	NOP Implied 1 2		CPX ABS 3 4	SBC ABS 3 4	INC ABS 3 6		E
F	BEQ Relative 2 2**	SBC (IND), Y 2 5*				SBC ZP, X 2 4	INC ZP, X 2 6		SED Implied 1 2	SBC ABS, Y 3 4*				SBC ABS, X 3 4*	INC ABS, X 3 7		F
MSD \ LSD	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	MSD

0

0 | BRK
Implied
1 7 | —OP Code
—Addressing Mode
—Instruction Bytes; Machine Cycles

*Add 1 to N if page boundary is crossed.
**Add 1 to N if branch occurs to same page, add 2 to N if branch occurs to different page

INSTRUCTION SET SUMMARY

INSTRUCTIONS		IMMEDIATE			ABSOLUTE			ZERO PAGE			ACCUM			IMPLIED			(IND, X)			(IND), Y			Z PAGE, X			ABS, X			ABS, Y			RELATIVE			INDIRECT			Z PAGE, Y			PROCESSOR STATUS CODES	
																																							7 6 5 4 3 2 1 0	
MNEMONIC	OPERATION	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	N V • B D I Z C	MNEMONIC
ADC	A + M + C → A (4) (1)	69	2	2	6D	4	3	65	3	2							61	6	2	71	5	2	75	4	2	7D	4	3	79	4	3										N V • • • • Z C	ADC
AND	A ∧ M → A (1)	29	2	2	2D	4	3	25	3	2							21	6	2	31	5	2	35	4	2	3D	4	3	39	4	3										N • • • • • Z •	AND
ASL	C ← [7 6 5 4 3 2 1 0] ← 0				0E	6	3	06	5	2	0A	2	1										16	6	2	1E	7	3													N • • • • • Z C	ASL
BCC	BRANCH ON C = 0 (2)																															90	2	2							• • • • • • • •	BCC
BCS	BRANCH ON C = 1 (2)																															B0	2	2							• • • • • • • •	BCS
BEQ	BRANCH ON Z = 1 (2)																															F0	2	2							• • • • • • • •	BEQ
BIT	A ∧ M				2C	4	3	24	3	2																															M_7 M_6 • • • • Z •	BIT
BMI	BRANCH ON N = 1 (2)																															30	2	2							• • • • • • • •	BMI
BNE	BRANCH ON Z = 0 (2)																															D0	2	2							• • • • • • • •	BNE
BPL	BRANCH ON N = 0 (2)																															10	2	2							• • • • • • • •	BPL
BRK	BREAK													00	7	1																									• • • 1 • 1 • •	BRK
BVC	BRANCH ON V = 0 (2)																															50	2	2							• • • • • • • •	BVC
BVS	BRANCH ON V = 1 (2)																															70	2	2							• • • • • • • •	BVS
CLC	0 → C													18	2	1																									• • • • • • • 0	CLC
CLD	0 → D													D8	2	1																									• • • • 0 • • •	CLD
CLI	0 → I													58	2	1																									• • • • • 0 • •	CLI
CLV	0 → V													B8	2	1																									• 0 • • • • • •	CLV
CMP	A - M	C9	2	2	CD	4	3	C5	3	2							C1	6	2	D1	5	2	D5	4	2	DD	4	3	D9	4	3										N • • • • • Z C	CMP
CPX	X - M	E0	2	2	EC	4	3	E4	3	2																															N • • • • • Z C	CPX
CPY	Y - M	C0	2	2	CC	4	3	C4	3	2																															N • • • • • Z C	CPY
DEC	M - 1 → M				CE	6	3	C6	5	2													D6	6	2	DE	7	3													N • • • • • Z •	DEC
DEX	X - 1 → X													CA	2	1																									N • • • • • Z •	DEX
DEY	Y - 1 → Y													88	2	1																									N • • • • • Z •	DEY
EOR	A ⊻ M → A (1)	49	2	2	4D	4	3	45	3	2							41	6	2	51	5	2	55	4	2	5D	4	3	59	4	3										N • • • • • Z •	EOR
INC	M + 1 → M				EE	6	3	E6	5	2													F6	6	2	FE	7	3													N • • • • • Z •	INC
INX	X + 1 → X													E8	2	1																									N • • • • • Z •	INX
INY	Y + 1 → Y													C8	2	1																									N • • • • • Z •	INY
JMP	JUMP TO NEW LOC				4C	3	3																												6C	5	3				• • • • • • • •	JMP
JSR	JUMP SUB				20	6	3																																			• • • • • • • •	JSR
LDA	M → A (1)	A9	2	2	AD	4	3	A5	3	2							A1	6	2	B1	5	2	B5	4	2	BD	4	3	B9	4	3										N • • • • • Z •	LDA
LDX	M → X (1)	A2	2	2	AE	4	3	A6	3	2																			BE	4	3							B6	4	2	N • • • • • Z •	LDX
LDY	M → Y (1)	A0	2	2	AC	4	3	A4	3	2													B4	4	2	BC	4	3													N • • • • • Z •	LDY
LSR	0 → [7 6 5 4 3 2 1 0] → C				4E	6	3	46	5	2	4A	2	1										56	6	2	5E	7	3													0 • • • • • Z C	LSR
NOP	NO OPERATION													EA	2	1																									• • • • • • • •	NOP
ORA	A ∨ M → A	09	2	2	0D	4	3	05	3	2							01	6	2	11	5	2	15	4	2	1D	4	3	19	4	3										N • • • • • Z •	ORA
PHA	A → M_S S - 1 → S													48	3	1																									• • • • • • • •	PHA
PHP	P → M_S S - 1 → S													08	3	1																									• • • • • • • •	PHP
PLA	S + 1 → S M_S → A													68	4	1																									N • • • • • Z •	PLA
PLP	S + 1 → S M_S → P													28	4	1																									(RESTORED)	PLP
ROL	[7 6 5 4 3 2 1 0] ← [C] ←				2E	6	3	26	5	2	2A	2	1										36	6	2	3E	7	3													N • • • • • Z C	ROL
ROR	→ [C] → [7 6 5 4 3 2 1 0]				6E	6	3	66	5	2	6A	2	1										76	6	2	7E	7	3													N • • • • • Z C	ROR
RTI	RTRN INT													40	6	1																									(RESTORED)	RTI
RTS	RTRN SUB													60	6	1																									• • • • • • • •	RTS
SBC	A - M - $\overline{C}$ → A (1)	E9	2	2	ED	4	3	E5	3	2							E1	6	2	F1	5	2	F5	4	2	FD	4	3	F9	4	3										N V • • • • Z (3)	SBC
SEC	1 → C													38	2	1																									• • • • • • • 1	SEC
SED	1 → D													F8	2	1																									• • • • 1 • • •	SED
SEI	1 → I													78	2	1																									• • • • • 1 • •	SEI
STA	A → M				8D	4	3	85	3	2							81	6	2	91	6	2	95	4	2	9D	5	3	99	5	3										• • • • • • • •	STA
STX	X → M				8E	4	3	86	3	2																													96	4	2	• • • • • • • •	STX
STY	Y → M				8C	4	3	84	3	2													94	4	2																• • • • • • • •	STY
TAX	A → X													AA	2	1																									N • • • • • Z •	TAX
TAY	A → Y													A8	2	1																									N • • • • • Z •	TAY
TSX	S → X													BA	2	1																									N • • • • • Z •	TSX
TXA	X → A													8A	2	1																									N • • • • • Z •	TXA
TXS	X → S													9A	2	1																									• • • • • • • •	TXS
TYA	Y → A													98	2	1																									N • • • • • Z •	TYA

(1) ADD 1 TO N IF PAGE BOUNDARY IS CROSSED

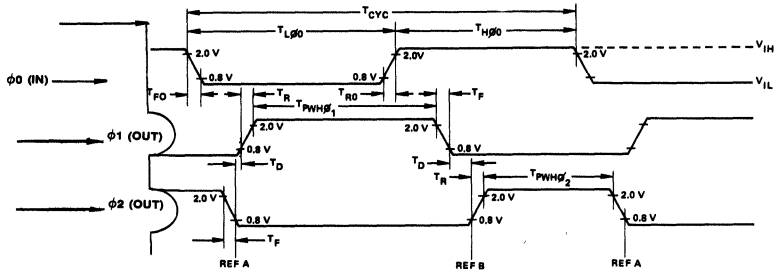
(2) ADD 1 TO N IF BRANCH OCCURS TO SAME PAGE
ADD 2 TO N IF BRANCH OCCURS TO DIFFERENT PAGE

(3) CARRY NOT - BORROW

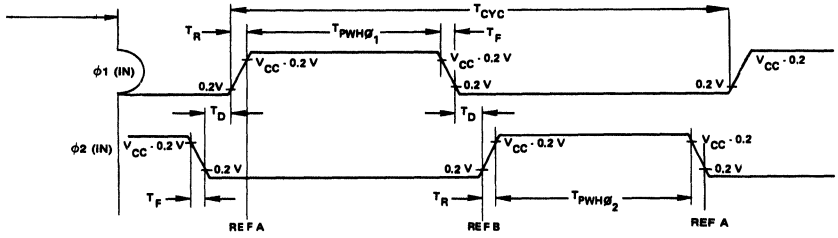
(4) IF IN DECIMAL MODE Z FLAG IS INVALID
ACCUMULATOR MUST BE CHECKED FOR ZERO RESULT

X	INDEX X	+	ADD
Y	INDEX Y	-	SUBTRACT
A	ACCUMULATOR	∧	AND
M	MEMORY PER EFFECTIVE ADDRESS	∨	OR
M_S	MEMORY PER STACK POINTER	⊻	EXCLUSIVE OR
M	MEMORY BIT 7		
M_6	MEMORY BIT 6		
n	NO CYCLES		
#	NO BYTES		

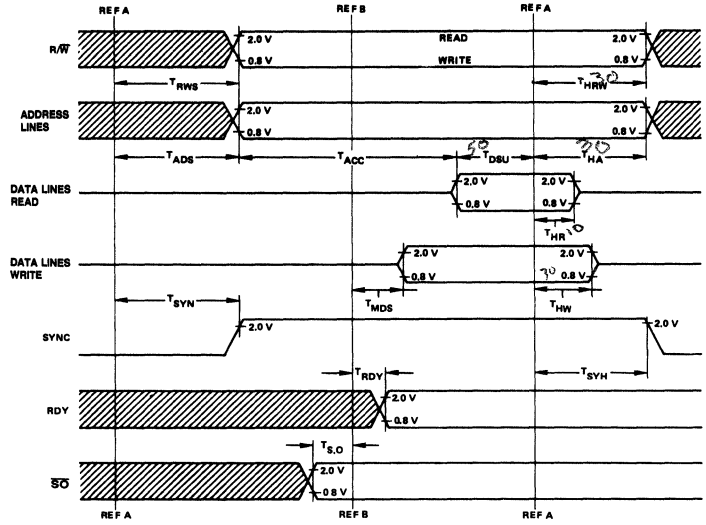
R650X CLOCK TIMING



R651X CLOCK TIMING



R65XX READ WRITE TIMING

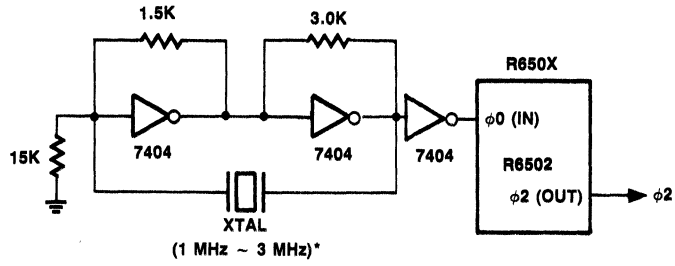


AC CHARACTERISTICS

Characteristic	Symbol	R65XX (1 MHz) Min	R65XX (1 MHz) Max	R65XXA (2 MHz) Min	R65XXA (2 MHz) Max	R65XXB (3 MHz) Min	R65XXB (3 MHz) Max	Unit
R650X CLOCK TIMING								
Clock Cycle Time	T_{CYC}	1.0	10	0.5	10	0.33	10	µs
Ø0 (IN) Low Pulse Width	$T_{L\emptyset0}$	480	—	240	—	160	—	ns
Ø0 (IN) High Pulse Width	$T_{H\emptyset0}$	460	—	240	—	160	—	ns
Ø0 (IN) Rise and Fall Time[1, 2]	T_{R0}, T_{F0}	—	10	—	10	—	10	ns
Ø1 (OUT) High Pulse Width	$T_{PWH\emptyset1}$	460	—	235	—	155	—	ns
Ø2 (OUT) High Pulse Width	$T_{PWH\emptyset2}$	460	—	240	—	160	—	ns
Delay Between Ø1 (OUT) and Ø2 (OUT)	T_D	0	—	0	—	0	—	ns
Ø1 (OUT), Ø2 (OUT) Rise and Fall Time[1, 2]	T_R, T_F	—	25	—	25	—	15	ns
R651X CLOCK TIMING								
Clock Cycle Time	T_{CYC}	1.0	10	0.5	10	0.33	10	µs
Ø1 (IN) High Pulse Width	T_{PWH01}	430	—	215	—	150	—	ns
Ø2 (IN) High Pulse Width	T_{PWH02}	470	—	235	—	160	—	ns
Delay Between Ø1 and Ø2	T_D	0	—	0	—	0	—	ns
Ø1 (IN), Ø2 (IN) Rise and Fall Time[1, 3]	T_R, T_F	—	25	—	20	—	15	ns
R65XX READ/WRITE TIMING								
R/$\overline{W}$ Setup Time	T_{RWS}	—	225	—	140	—	110	ns
R/$\overline{W}$ Hold Time	T_{HRW}	30	—	30	—	15	—	ns
Address Setup Time	T_{ADS}	—	225	—	140	—	110	ns
Address Hold Time	T_{HA}	30	—	30	—	15	—	ns
Read Access Time	T_{ACC}	—	650	—	310	—	170	ns
Read Data Setup Time	T_{DSU}	100	—	50	—	50	—	ns
Read Data Hold Time	T_{HR}	10	—	10	—	10	—	ns
Write Data Setup Time	T_{MDS}	—	175	—	100	—	85	ns
Write Data Hold Time	T_{HW}	30	—	30	—	15	—	ns
SYNC Hold Time	T_{SYH}	30	—	30	—	15	—	ns
RDY Setup Time	T_{RDY}	100	—	50	—	35	—	ns
$\overline{SO}$ Setup Time	T_{S0}	100	—	50	—	35	—	ns
SYNC Setup Time	T_{SYN}	—	225	—	140	—	110	ns

Notes:
1. Loads: All output except clocks = 1 TTL + 130 pF. Clock outputs = 1 TTL + 30 pF.
2. Measured between 0.8 and 2.0 points on waveform load.
3. Measured between 10% and 90% points on waveforms.
4. *RDY must never switch states within R_{RDY} to end of Ø2.

EXAMPLE OF TIME BASE GENERATION FOR R6502



*CRYSTAL: CTS KNIGHTS MP SERIES, OR EQUIVALENT

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to +7.0	Vdc
Input Voltage	V_{IN}	−0.3 to +7.0	Vdc
Operating Temperature Range Commercial Industrial	T_A	 −40 to +85	°C
Storage Temperature	T_{STG}	−55 to +150	°C

***NOTE:** Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the other sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2

OPERATING CONDITIONS

Parameter	Symbol	Value
Supply Voltage	V_{CC}	5V ±5%
Temperature Range Commercial Industrial	T_A	 0°C to +70°C −40°C to +85°C

DC CHARACTERISTICS

(V_{CC} = 5.0V ±5%, V_{SS} = 0, T_A = T_L to T_H, unless otherwise noted)

Parameter	Symbol	Min.	Typ.[5]	Max.	Unit[1]	Test Conditions
Input High Voltage Logic, Ø0 (IN) Ø1 (IN), Ø2 (IN)	V_{IH}	 2.0 V_{CC} −0.3	 — —	 V_{CC} V_{CC} + 0.25	V	
Input Low Voltage Logic, Ø0 (IN) Ø1 (IN), Ø2 (IN)	V_{IL}	 −0.3 −0.3	 — —	 0.8 0.4	V	
Input Leakage Current Logic (Excl. RDY, S.O.) Ø1 (IN), Ø2 (IN) Ø0 (IN)	I_{IN}	 — — —	 — — —	 2.5 100 10	μA	V_{IN} = 0V to 5.25V V_{CC} = 0V
Input Leakage Current for Three State Off D0-D7	I_{TSI}	 —	 —	 10	μA	V_{IN} = 0.4V to 2.4V V_{CC} = 5.25V
Output High Voltage SYNC, D0-D7, A0-A15, R/$\overline{W}$, Ø1 (OUT), Ø2 (OUT)	V_{OH}	 +2.4	 —	 —	V	I_{LOAD} = −100 μA V_{CC} = 4.75V
Output Low Voltage SYNC, D0-D7, A0-A15, R/$\overline{W}$, Ø1 (OUT), Ø2 (OUT)	V_{OL}			 +0.4	V	I_{LOAD} = 1.6 mA V_{CC} = 4.75V
Power Dissipation 1 and 2 MHz 3 MHz	P_D	 — —	 450 500	 700 800	mW	
Capacitance Logic D0-D7 A0-A15, R/$\overline{W}$, SYNC Ø0 (IN) Ø1 (IN) Ø2 (IN)	C C_{IN} C_{OUT} $C_{Ø0(IN)}$ $C_{Ø1}$ $C_{Ø2}$	 — — — — — —	 — — — — 30 50	 10 15 12 15 50 80	pF	V_{CC} = 5.0V V_{IN} = 0V f = 1 MHz T_A = 25°C

Notes:
1. All units are direct current (dc) except for capacitance.
2. Negative sign indicates outward current flow, positive indicates inward flow.
3. $\overline{IRQ}$ and $\overline{NMI}$ require 3K pull-up resistor.
4. Ø1 (IN) and Ø2 (IN) apply to R6512, 13, 14, and 15; Ø0 (IN) applies to R6502, 03, 04, 05, 06 and 07.
5. Typical values shown for V_{CC} = 5.0V and T_A = 25°C.

Rockwell

R6501Q AND R6511Q ONE-CHIP MICROPROCESSOR

INTRODUCTION

The Rockwell R6501Q and R6511Q are extended, high performance 8-bit NMOS-3, single chip microprocessors, and are compatible with all members of the R6500 family.

The devices contain an enhanced R6502 CPU, an internal clock oscillator, 192 bytes of Random Access Memory, and versatile interface circuitry. The interface circuitry includes two 16-bit programmable timer/counters, 32 bidirectional input/output lines (including four edge sensitive lines and input latching on one 8-bit port), a full-duplex serial I/O channel, ten interrupts and bus expandability. A full 16-bit address bus and 8-bit data bus provide accessing to 65K bytes of external memory.

The devices come in a 64-pin Quad Inline package (QUIP).

The devices may be used as a CPU-RAM-I/O counter device in multichip systems or as an emulator for the R6500/11 family of microcomputers. They provide all R6500/11 interface lines, plus the address bus, data bus and control lines to interface with external memory.

SYSTEMS DEVELOPMENT

Rockwell supports development of the devices with the Rockwell Design Center System and the R6500/* Personality Set: Complete in-circuit emulation with the Personality Set allows total systems test and evaluation.

This data sheet is for the reader familiar with the R6502 CPU hardware and programming capabilities. For additional information see the R6501Q Product Description, (Document Order Number 2145) or the R6511Q Product Description, (Document Order Number 2133).

ORDERING INFORMATION

Part Number	Package Type	Frequency Option	Temp. Range
R6501Q	Plastic (QUIP)	1 MHz	0°C to 70°C
R6501AQ	Plastic (QUIP)	2 MHz	0°C to 70°C
R6511Q	Plastic (QUIP)	1 MHz	0°C to 70°C
R6511AQ	Plastic (QUIP)	2 MHz	0°C to 70°C

FEATURES

- Enhanced R6502 CPU
  - —Four new bit manipulation instructions
    - Set Memory Bit (SMB)
    - Reset Memory Bit (RMB)
    - Branch on Bit Set (BBS)
    - Branch on Bit Reset (BBR)
  - —Decimal and binary arithmetic modes
  - —13 Addressing modes
  - —True indexing
- 192-byte static RAM
- 32 bidirectional, TTL-compatible I/O lines (four ports)
- One 8-bit port may be tri-stated under software control
- One 8-bit port may have latched inputs under software control
- Two 16-bit programmable counter/timers, with 3 latches
  - —Pulse width measurement
  - —Pulse generation (1 symmetrical, 1 asymmetrical)
  - —Interval timer
  - —Event counter
  - —Retriggerable interval timer
- Serial Port — Full Duplex, Buffered UART
  - —Receiver Wake Up and Transmitter End of Transmission Features
  - —Programmable Standard Asynchronous Baud Rates from 50 to 125K bits/sec at 2 MHz

    Satisfies SMPTE 422 Broadcast Standard (8 Data, Parity, 1 Stop) at 38.4K bits/sec
  - —Programmable 5-8 bit Character Lengths, with or without parity
  - —Receiver Error Detection for Framing, Parity, and Overrun
  - —Synchronous Shift Register alternate mode (250KC at 2 MHz)
- Ten interrupts
  - —Four edge-sensitive lines; two positive, two negative
  - —Two counter underflows
  - —Serial data receiver buffer full
  - —Serial data transmitter buffer empty
  - —Non-maskable
  - —Reset
- Full data and address pins for 65K bytes of external memory
- Flexible clock circuitry
  - —2 MHz or 1 MHz internal operation
  - —Internal clock with external XTAL at four times internal frequency (R6501Q) or two times internal frequency (R6511Q)
  - —External clock input divided by one or four (R6501Q) or one or two (R6511Q)
- 68% of the instructions have execution times less than 2 μs at 2 MHz
- NMOS-3 silicon gate, depletion load technology
- Single +5V power supply
- 12 mW stand-by power for 32 bytes of the 192-byte RAM
- 64-pin QUIP
- R6501Q has pullup resistors on PA, PB, and PC
  R6511Q has no pullup resistors

FUNCTIONAL DESCRIPTION

CENTRAL PROCESSING UNIT (CPU)

The internal CPU of the device is a standard R6502 configuration with the standard R6502 instructions plus 4 new bit manipulation instructions. These new bit manipulator instructions form an enhanced R6502 instruction set and improve memory utilization efficiency and performance.

Set Memory Bit (SMB #,ADDR.)

This instruction sets to "1" one bit of the 8-bit data field specified by the zero page address (memory or I/O port). The first byte of the instruction specifies the SMB operation and which one of 8 bits to be set. The second byte of the instruction designates the address (0-225) of the byte or I/O port to be operated upon.

Reset Memory Bit (RMB #,ADDR.)

This instruction is the same operation and format as the SMB instruction except a reset to "0" of the bit results.

Branch on Bit Set Relative (BBS #,ADDR.,DEST)

This instruction tests one of 8 bits designated by a 3-bit immediate field within the first byte of the instruction. The second byte is used to designate the location of the byte or I/O port to be tested within the zero page address range. The third byte of the instruction is used to specify the 8-bit relative address to which the instruction branches if the bit tested is a "1". If the bit tested is not set, the next sequential instruction is executed.

Branch on Bit Reset Relative (BBR #,ADDR.,DEST)

This instruction is the same operation and format as the BBS instruction except that a branch takes place if the bit tested is a "0".

Random Access Memory (RAM)

The RAM consists of 192 by 8 bits of read/write memory with an assigned page zero address of 0040 through 00FF. The devices provide a separate power pin (V_{RR}) which may be used for standby power. In the event of the loss of V_{CC} power, the lowest 32 bytes of RAM data will be retained if standby power is supplied to the V_{RR} pin.

Clock Oscillator

The clock oscillator provides the basic timing signals. A reference frequency can be generated with the on board oscillator (with external crystal) or an external reference source can be driven into the XTLI pin. If the XTLO pin is left floating, the reference frequency is internally divided by four (R6501Q) or two (R6511Q) to obtain the internal clock. The internal clock is then available as an output at the Ø2 pin. The XTLI pin may be used as an undivided clock input by connecting XTLO to V_{SS}, in which case the internal division circuitry is bypassed and the device operates at the reference frequency.

Parallel Input/Output Ports

The devices have 32 I/O lines grouped into four 8-bit ports (PA, PB, PC, PD). Ports A through C may be used either for input or output individually, or in groups of any combination. The R6501Q has pullup resistors on PA, PB and PC. The R6511Q has no pullup resistors. Port D may be used as all inputs or all outputs. It has active pull-ups.

Port A (PA) can be programmed as a standard parallel 8-bit I/O port or under software control as serial I/O lines, counter I/O lines, positive (2) and negative (2) edge detects, or an input data strobe for the Port B (PB) input latch.

Port B (PB) can be programmed as an I/O port with latched input enabled or disabled.

Port C (PC) can be programmed as an I/O port, as an abbreviated bus, as a multiplexed bus, or as part of the full address mode. In the full address mode pins PC6 and PC7 serve as addresses A13 and A14, respectively; PC0–PC5 are I/O pins.

Port D (PD) functions as an I/O port, an 8-bit tri-state data bus, or as a multiplexed address/data bus.

Serial Input/Output Channel — UART

The devices provide a full duplex serial I/O channel with programmable bit rates covering all standard baud rates from 50 to 125K bits/sec including the SMPTE 422 standard at 38.4K bits/sec. Character lengths of 5 to 8 bits, with or without parity are programmable. A full complement of flags provides for Receiver Wake Up; Receiver Buffer Full; Receiver Error Conditions detecting Framing, Parity, and Overrun errors; Transmitter End of Transmission and Transmitter Buffer Empty. In addition, a synchronous shift register mode to 250 KC at 2 MHz is available.

Wake-Up Feature

In a multi-distributed microcomputer application, a destination address is usually included at the beginning of the message. The Wake-Up Feature allows non-selected CPUs to ignore the remainder of the message until the beginning of the next message by setting the Wake-Up bit.

Counter/Latch Logic

The devices contain two 16-bit counters (Counter A and Counter B) and three 16-bit latches associated with the counters. Counter A has one 16-bit latch and Counter B has two 16-bit latches. Each counter can be independently programmed to operate in one of four modes:

Counter A	Counter B
• Pulse width measurement	• Retriggerable Interval Counter
• Pulse Generation	• Assymmetrical Pulse Generation
• Interval Timer	• Interval Timer
• Event Counter	• Event Counter

Mode Control Register (MCR)

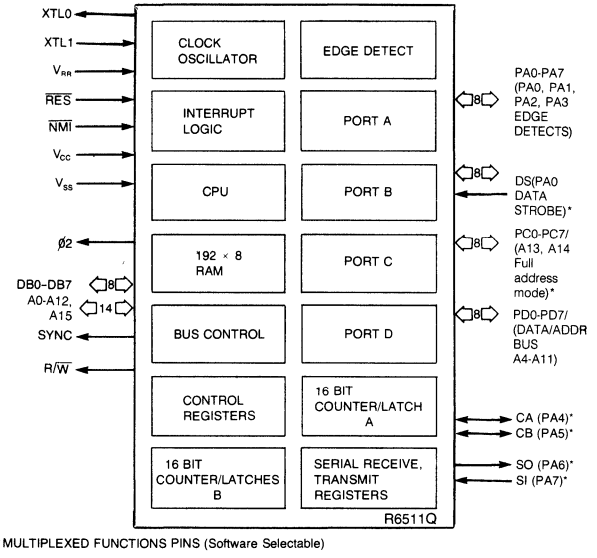
The Mode Control Register contains control bits for the multifunction I/O ports and mode select bits for Counter A and Counter B.

Ports C and D Operation Modes

There are four operating modes available in ports C and D, software programmable via the Mode Control Register. The full address mode allows access to a full 65K bytes of external storage. In this mode PC6 and PC7 are automaticallyu used for A13 and A14. In the Input/Output mode the four ports are all used for I/O. In the abbreviated and multiplexed modes some port pins set up for addressing 64 or 16,384 bytes of external memory.

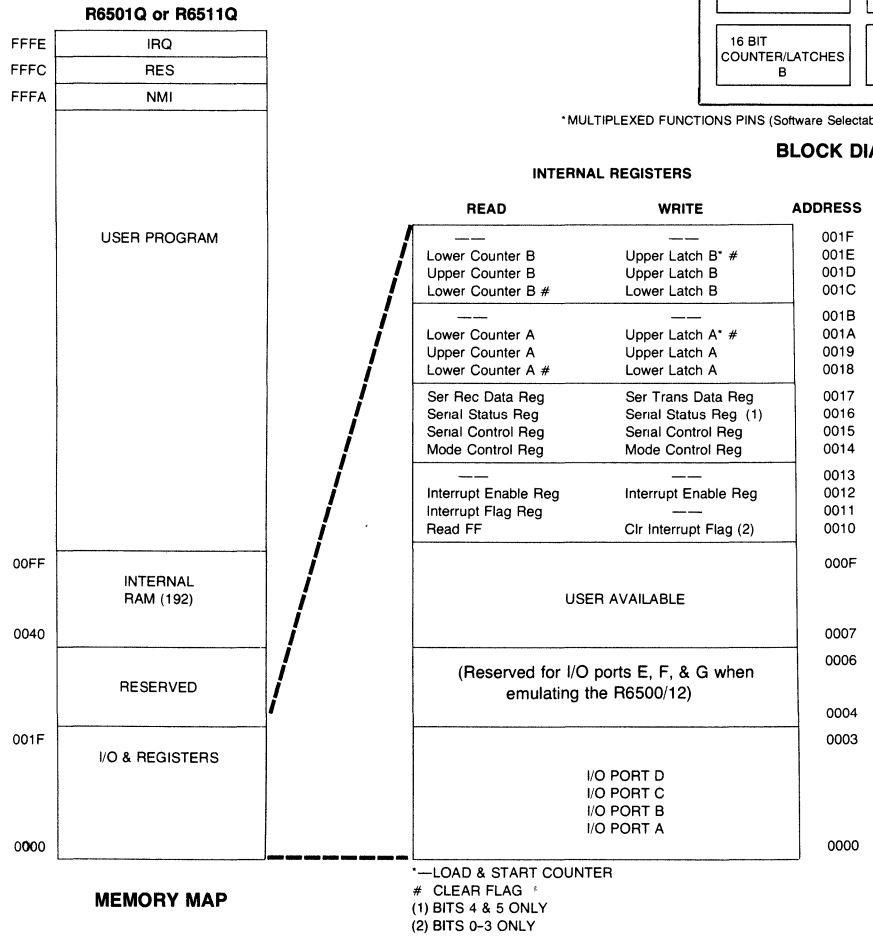
Interrupt Flag Register (IFR) and Interrupt Enable Register (IER)

The devices include an Interrupt Flat Register and an Interrupt Enable Register which flags and controls I/O and counter status.



*MULTIPLEXED FUNCTIONS PINS (Software Selectable)

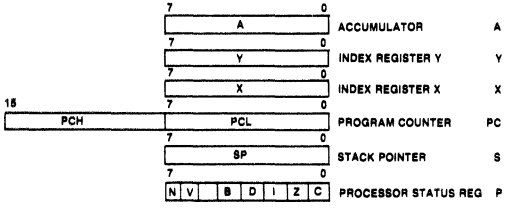
BLOCK DIAGRAM



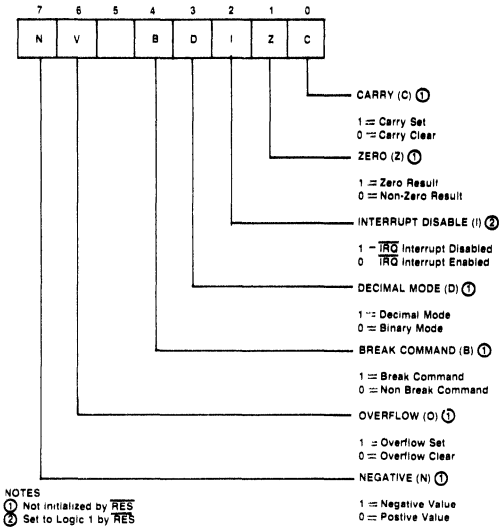
*—LOAD & START COUNTER
CLEAR FLAG
(1) BITS 4 & 5 ONLY
(2) BITS 0-3 ONLY

MEMORY MAP

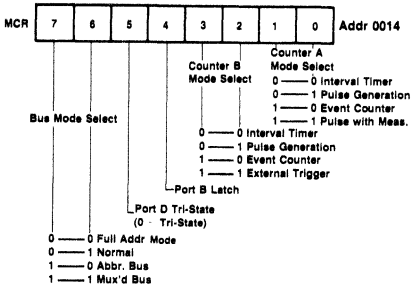
KEY REGISTER SUMMARY



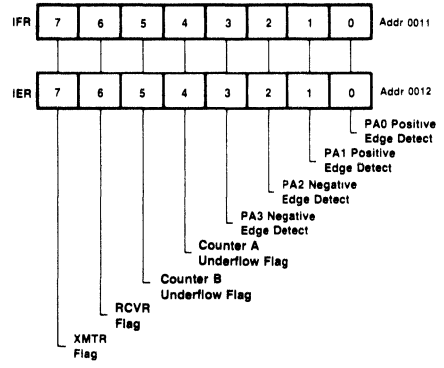
CPU Registers



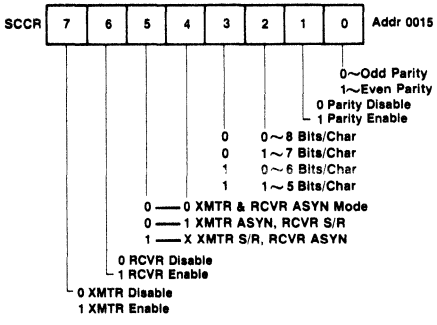
Processor Status Register



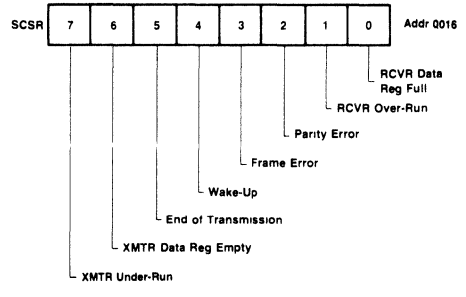
Mode Control Register



Interrupt Enable and Flag Registers



Serial Communications Control Register



Serial Communications Status Register

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC} & V_{RR}	−0.3 to +7.0	Vdc
Input Voltage	V_{IN}	−0.3 to +7.0	Vdc
Operating Temperature Commercial	T	0 to +70	°C
Storage Temperature Range	T_{STG}	−55 to +150	°C

***NOTE:** Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in other sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

(V_{CC} = 5V ±5% V_{SS} = 0)

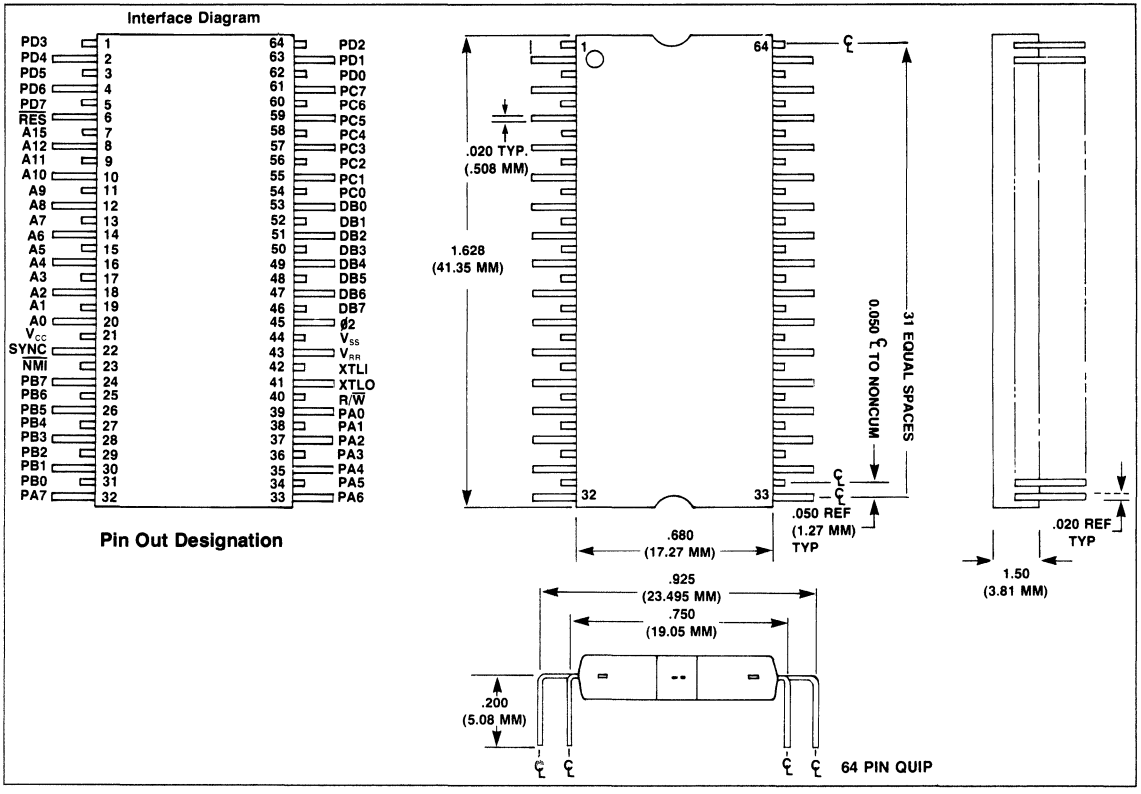
Parameter	Symbol	Min	Typ	Max	Unit
Power Dissipation (Outputs High) Commercial at 25°C	P_D	—	—	1200	mW
RAM Standby Voltage (Retention Mode)	V_{RR}	3.0	—	V_{CC}	Vdc
RAM Standby Current (Retention Mode) Commercial at 25°C	I_{RR}	—	4	—	mAdc
Input High Voltage Except XTLI	V_{IH}	+2.0	—	V_{CC}	Vdc
Input High Voltage (XTLI)	V_{IH}	+4.0	—	V_{CC}	Vdc
Input Low Voltage	V_{IL}	−0.3	—	+0.8	Vdc
Input Leakage Current ($\overline{RES}$, $\overline{NMI}$) V_{IN} = 0 to 5.0 Vdc	I_{IN}	—	—	±10	μAdc
Input Low Current (V_{IL} = 0.4 Vdc)	I_{IL}	—	−1.0	−1.6	mAdc
Output High Voltage Except XTLO (I_{LOAD} = −100 μAdc)	V_{OH}	+2.4	—	V_{CC}	Vdc
Output Low Voltage (I_{LOAD} = 1.5 mAdc)	V_{OL}	—	—	+0.4	Vdc
Input Capacitance (V_{IN} −0, T_A = 25°C, f = 1.0 MHz) XTL1, XTLO All Others	C_{IN}	— —	— —	50 10	pF
I/O Port Pull-Up Resistance PA0–PA7, PB0–PB7, PC0–PC7 R6501Q only	R_L	3.0	6.0	11.5	KΩ
Note: Negative sign indicates outward current flow, positive indicates inward flow.					

AC CHARACTERISTICS

(V_{CC} = 5V ±6% V_{SS} = 0

Parameter	Symbol	1 MHz		2 MHz		Unit
		Min	Max	Min	Max	
XTLI Input Clock Cycle Time	T_{CYC}	1.0	10.0	0.500	10.0	μsec
Internal Write to Peripheral Data Valid (TTL)	T_{POW}	1.0		0.5		μsec
Peripheral Data Setup Time	T_{PDSU}	500		500		nsec
Count and Edge Detect Pulse Width	T_{PW}	1.0		0.5		μsec

PACKAGE DIMENSIONS



Rockwell

R6520
PERIPHERAL INTERFACE ADAPTER (PIA)

DESCRIPTION

The R6520 Peripheral Interface Adapter (PIA) is designed to solve a broad range of peripheral control problems in the implementation of microcomputer systems. This device allows a very effective trade-off between software and hardware by providing significant capability and flexibility in a low cost chip. When coupled with the power and speed of the R6500, R6500* or R65C00 family of microprocessors, the R6520 allows implementation of very complex systems at a minimum overall cost.

Control of peripheral devices is handled primarily through two 8-bit bidirectional ports. Each of these lines can be programmed to act as either an input or an output. In addition, four peripheral control/interrupt input lines are provided. These lines can be used to interrupt the processor or to "handshake" data between the processor and a peripheral device.

FEATURES

- Direct replacement for MC6820 PIA
- Two 8-bit bidirectional I/O ports with individual data direction control
- Automatic "Handshake" control of data transfers
- Two interrupts (one for each port) with program control
- Commercial and industrial temperature range versions
- 40-pin plastic and ceramic versions
- 5 volt ±5% supply requirements
- Compatible with the R6500, R6500/* and R65C00 family of microprocessors
- 1 and 2 MHz versions

ORDERING INFORMATION

Part Number
R6520 ___

- Temperature Range (T_L to T_H):
  - Blank = 0°C to +70°C
  - E = −40°C to +85°C
- Package:
  - C = Ceramic
  - P = Plastic
- Frequency Range:
  - No letter = 1 MHz
  - A = 2 MHz

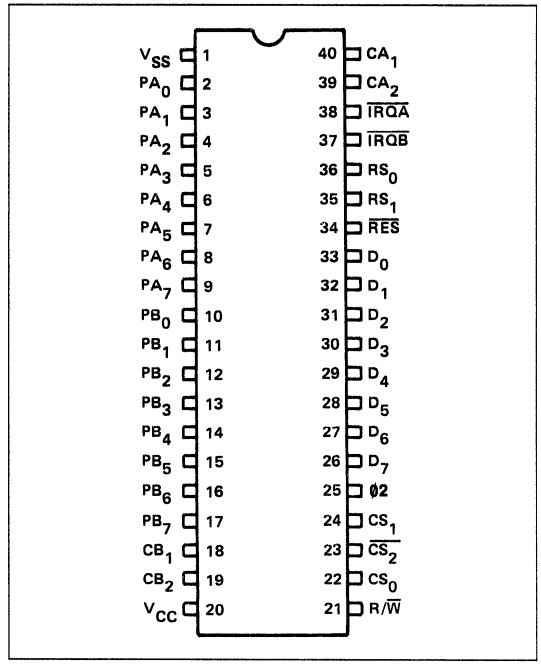


Figure 1. R6520 Pin Configuration

FUNCTIONAL DESCRIPTION

The R6520 PIA is organized into two independent sections referred to as the A Side and the B Side. Each section consists of a Control Register (CRA, CRB), Data Direction Register (DDRA, DDRB), Output Register (ORA, OBR), Interrupt Status Control (ISCA, ISCB), and the buffers necessary to drive the Peripheral Interface buses. Data Bus Buffers (DBB) interface data from the two sections to the data bus, while the Data Input Register (DIR) interfaces data from the DBB to the PIA registers. Chip Select and R/$\overline{W}$ control circuitry interface to the processor bus control lines. Figure 2 is a block diagram of the R6520 PIA.

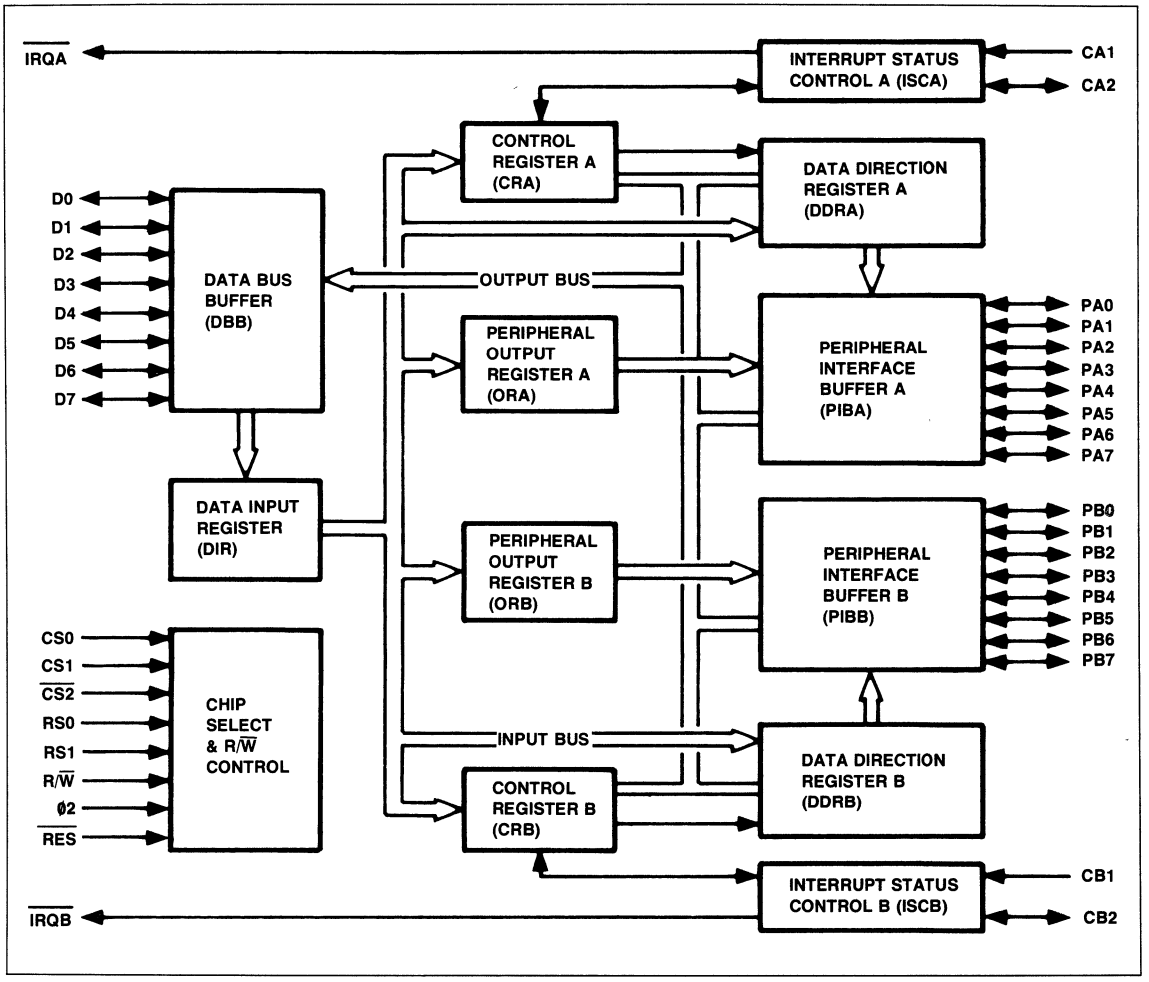


Figure 2. R6520 PIA Block Diagram

DATA INPUT REGISTER (DIR)

When the microprocessor writes data into the PIA, the data which appears on the data bus during the Ø2 clock pulse is latched into the Data Input Register (DIR). The data is then transferred into one of six internal registers of the PIA after the trailing edge of the Ø2 clock. This assures that the data on the peripheral output lines will make smooth transitions from high to low (or from low to high) and the voltage will remain stable except when it is going to the opposite polarity.

CONTROL REGISTERS (CRA and CRB)

Table 1 illustrates the bit designation and functions in the two control registers. The control registers allow the microprocessor to control the operation of the Interrupt Control inputs (CA1, CA2, CB1, CB2), and Peripheral Control outputs (CA2, CB2). Bit 2 in each register controls the addressing of the Data Direction Registers (DDRA, DDRB) and the Output Registers (ORA, ORB). In addition, two bits (bit 6 and 7) in each control register indicate the status of the Interrupt Input lines (CA1, CA2, CB1, CB2). These Interrupt Status bits (IRQA1, IRQA2 or IRQB1, IRQB2) are normally interrogated by the microprocessor during the $\overline{IRQ}$ interrupt service routine to determine the source of the interrupt.

DATA DIRECTION REGISTERS (DDRA, DDRB)

The Data Direction Registers (DDRA, DDRB) allow the processor to program each line in the 8-bit Peripheral I/O port to be either an input or an output. Each bit in DDRA controls the corresponding line in the Peripheral A port and each bit in DDRB controls the corresponding line in the Peripheral B port. Writing a "0" in a bit position in the Data Direction Register causes the corresponding Peripheral I/O line to act as an input; a "1" causes it to act as an output.

Bit 2 (DDRA, DDRB) in each Control Register (CRA and CRB) controls the accessing to the Data Direction Register or the Peripheral interface. If bit 2 is a "1," a Peripheral Output register (ORA, ORB) is selected, and if bit 2 is a "0," a Data Direction Register (DDRA, DDRB) is selected. The Data Direction Register Access Control bit, together with the Register Select lines (RS0, RS1) selects the various internal registers as shown in Table 2.

In order to write data into DDRA, ORA, DDRB, or ORB registers, bit 2 in the proper Control Register must first be set. The desired register may then be accessed with the address determined by the address interconnect technique used.

PERIPHERAL OUTPUT REGISTERS (ORA, ORB)

The Peripheral Output Registers (ORA, ORB) store the output data from the Data Bus Buffers (DBB) which appears on the Peripheral I/O port. If a line on the Peripheral A Port is programmed as an output by the DDRA, writing a 0 into the corresponding bit in the ORA causes that line to go low (<0.4 V); writing a 1 causes the line to go high. The lines of the Peripheral B port are controlled by ORB in the same manner.

INTERRUPT STATUS CONTROL (ISCA, ISCB)

The four interrupt/peripheral control lines (CA1, CA2, CB1, CB2) are controlled by the Interrupt Status Control logic (A, B). This logic interprets the contents of the corresponding Control Register and detects active transitions on the interrupt inputs.

PERIPHERAL I/O PORTS (PA0-PA7, PB0-PB7)

The Peripheral A and Peripheral B I/O ports allow the microprocessor to interface to the input lines on the peripheral device by writing data into the Peripheral Output Register. They also allow the processor to interface with the peripheral device output lines by reading the data on the Peripheral Port input lines directly onto the data bus and into the internal registers of the processor.

Each of the Peripheral I/O lines can be programmed to act as an input or an output. This is accomplished by setting a 1 in the corresponding bit in the Data Direction Register for those lines which are to act as outputs. A 0 in a bit of the Data Direction Register causes the corresponding Peripheral I/O lines to act as an input.

The buffers which drive the Peripheral A I/O lines contain "passive" pull-up devices. These pull-up devices are resistive in nature and therefore allow the output voltage to go to VCC for a logic 1. The switches can sink a full 3.2 mA, making these buffers capable of driving two standard TTL loads.

In the input mode, the pull-up devices are still connected to the I/O pin and still supply current to this pin. For this reason, these lines also represent two standard TTL loads in the input mode.

The Peripheral B I/O port duplicates many of the functions of the Peripheral A port. The process of programming these lines to act as an input or an output is similar to the Peripheral A port, as is the effect of reading or writing this port. However, there are several characteristics of the buffers driving these lines which affect their use in peripheral interfacing.

Table 1. Control Registers Bit Designations

	7	6	5	4	3	2	1	0
CRA	IRQA1	IRQA2	CA2 Control			DDRA Access	CA1 Control	
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CRB	IRQB1	IRQB2	CB2 Control			DDRB Access	CB1 Control	

The Peripheral B I/O port buffers are push-pull devices i.e., the pull-up devices are switched OFF in the 0 state and ON for a logic 1. Since these pull-ups are active devices, the logic 1 voltage will not go higher than +2.4V.

Another difference between the PA0-PA7 lines and the PB0 through PB7 lines is that they have three-state capability which allows them to enter a high impedance state when programmed to be used as input lines. In addition, data on these lines will be read properly, when programmed as output lines, even if the data signals fall below 2.0 volts for a "high" state or are above 0.8 volts for a "low" state. When programmed as output, each line can drive at least a two TTL load and may also be used as a source of up to 1 milliampere at 1.5 volts to directly drive the base of a transistor switch, such as a Darlington pair.

Because these outputs are designed to drive transistors directly, the output data is read directly from the Peripheral Output Register for those lines programmed to act as inputs.

The final characteristic is the high-impedance input state which is a function of the Peripheral B push-pull buffers When the Peripheral B I/O lines are programmed to act as inputs, the output buffer enters the high impedance state.

DATA BUS BUFFERS (DBB)

The Data Bus Buffers are 8-bit bidirectional buffers used for data exchange, on the D0-D7 Data Bus, between the microprocessor and the PIA. These buffers are tri-state and are capable of driving a two TTL load (when operating in an output mode) and represent a one TTL load to the microprocessor (when operating in an input mode).

INTERFACE SIGNALS

The PIA interfaces to the R6500, R6500/* or the R65C00 microprocessor family with a reset line, a ø2 clock line, a read/write line, two interrupt request lines, two register select lines, three chip select lines, and an 8-bit bidirectional data bus.

The PIA interfaces to the peripheral devices with four interrupt/control lines and two 8-bit bidirectional data buses.

Figure 1 (on the front page) shows the pin assignments for these interface signals and Figure 3 shows the interface relationship of these signal as they pertain to the CPU and the peripheral devices.

CHIP SELECT (CS0, CS1, $\overline{CS2}$)

The PIA is selected when CS0 and CS1 are high and $\overline{CS2}$ is low. These three chip select lines are normally connected to the processor address lines either directly or through external decoder circuits. When the PIA is selected, data will be transferred between the data lines and PIA registers, and/or peripheral interface lines as determined by the R/$\overline{W}$, RS0, and RS1 lines and the contents of Control Registers A and B.

RESET SIGNAL ($\overline{RES}$)

The Reset ($\overline{RES}$) input initializes the R65C21 PIA. A low signal on the $\overline{RES}$ input causes all internal registers to be cleared.

CLOCK SIGNAL (ø2)

The Phase 2 Clock Signal (ø2) is the system clock that triggers all data transfers between the CPU and the PIA. ø2 is generated by the CPU and is therefore the synchronizing signal between the CPU and the PIA.

READ/WRITE SIGNAL (R/$\overline{W}$)

Read/Write (R/$\overline{W}$) controls the direction of data transfers between the PIA and the data lines associated with the CPU and the peripheral devices. A high on the R/$\overline{W}$ line permits the peripheral devices to transfer data to the CPU from the PIA. A low on the R/$\overline{W}$ line allows data to be transfered from the CPU to the peripheral devices from the PIA

REGISTER SELECT (RS0, RS1)

The two Register Select lines (RS0, RS1), in conjunction with the Control Registes (CRA, CRB) DAta Direction Register access bits (see Table 1, bit 2) select the various R6520 registers to be accessed by the CPU, RS0 and RS1 are normally connected to the microprocessor (CPU) address output lines. Through control of these lines, the CPU can write directly into the Control

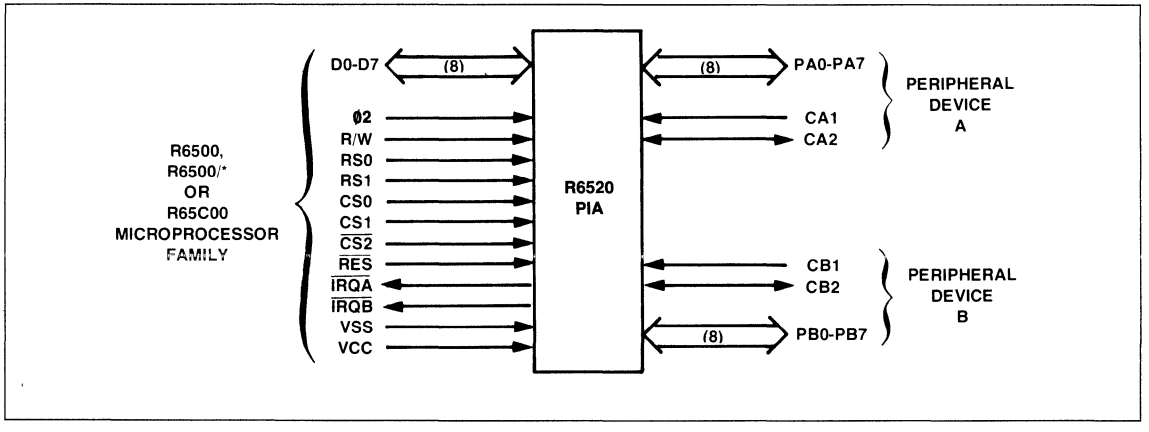


Figure 3. Interface Signals Relationship

Registers (CRA, CRB) the Data Direction Registers (DDRA, DDRB) and the Peripheral Output Registers (ORA, ORB). In addition, the processor may directly read the contents of the Control Registers and the Data Direction Registers. Accessing the Peripheral Output Register for the purpose of reading data back into the processor operates differently on the ORA and the ORB registers and therefore are shown separately in Table 2.

Table 2. ORA and ORB Register Addressing

Register Address (Hex)	Register Select Lines		Data Direction Control		Register Operation	
	RS1	RS0	CRA (Bit 2)	CRB (Bit 2)	R/$\overline{W}$=H	R/$\overline{W}$=L
0	L	L	1	—	Read PIBA	Write ORA
0	L	L	0	—	Read DDRA	Write DDRA
1	L	H	—	—	Read CRA	Write CRA
2	H	L	—	1	Read PIBB	Write ORB
2	H	L	—	0	Read DDRB	Write DDRB
3	H	H	—	—	Read CRB	Write CRB

INTERRUPT REQUEST LINES ($\overline{IRQA}$, $\overline{IRQB}$)

The active low Interrupt Request lines ($\overline{IRQA}$ and $\overline{IRQB}$) act to interrupt the microprocessor either directly or through external interrupt priority circuitry. These lines are open drain and are capable of sinking 1.6 milliamps from an external source. This permits all interrupt request lines to be tied together in a wired-OR configuration. The A and B in the titles of these lines correspond to the peripheral port A and the peripheral port B so that each interrupt request line services one peripheral data port.

Each Interrupt Request line has two interrupt flag bits which can cause the Interrupt Request line to go low. These flags are bits 6 and 7 in the two Control Registers (CRA, CRB). These flags act as the link between the peripheral interrupt signals and the microprocessor interrupt inputs. Each flag has a corresponding interrupt disable bit which allows the processor to enable or disable the interrupt from each of the four interrupt inputs (CA1, CA2, CB1, CB2). The four interrupt flags are set (enabled) by active transitions of the signal on the interrupt input (CA1, CA2, CB1, CB2).

CRA bit 7 (IRQA1) is always set by an active transition of the CA1 interrupt input signal. However, $\overline{IRQA}$ can be disabled by setting bit 0 in CRA to a 0. Likewise, CRA bit 6 (IRQA2) can be set by an active transition of the CA2 interrupt input signal and $\overline{IRQA}$ can be disabled by setting bit 3 in CRA to a 0.

Both bit 6 and bit 7 in CRA are reset by a "Read Peripheral Output Register A" operation. This is defined as an operation in which the read/write, proper data direction register and register select signals are provided to allow the processor to read the Peripheral A I/O port. A summary of $\overline{IRQA}$ control is shown in Table 3.

Control of $\overline{IRQB}$ is performed in exactly the same manner as that described above for $\overline{IRQA}$. Bit 7 in CRB (IRQB1) is set by an active transition on CB1 and $\overline{IRQB}$ from this flag is controlled by CRB bit 0. Likewise, bit 6 (IRQB2) in CRB is set by an active transition on CB2, and $\overline{IRQB}$ from this flag is controlled by CRB bit 3.

Also, both bit 6 and bit 7 of CRB are reset by a "Read Peripheral B Output Register" operation. A summary of $\overline{IRQB}$ control is shown in Table 3.

Table 3. $\overline{IRQA}$ and $\overline{IRQB}$ Control Summary

Control Register Bits	Action
CRA-7=1 and CRA-0=1	$\overline{IRQA}$ goes low (Active)
CRA-6=1 and CRA-3=1	$\overline{IRQA}$ goes low (Active)
CRB-7=1 and CRB-0=1	$\overline{IRQB}$ goes low (Active)
CRB-6=1 and CRB-3=1	$\overline{IRQB}$ goes low (Active)

Note:

The flags act as the link between the peripheral interrupt signals and the processor interrupt inputs The interrupt disable bits allow the processor to control the interrupt function

INTERRUPT INPUT/PERIPHERAL CONTROL LINES (CA1, CA2, CB1, CB2)

The four interrupt input/peripheral control lines provide a number of special peripheral control functions These lines greatly enhance the power of the two general purpose interface ports (PA0-PA7, PB0-PB7). Figure 4 summarizes the operation of these control lines.

CA1 is an interrupt input only. An active transition of the signal on this input will set bit 7 of the Control Register A to a logic 1 The active transition can be programmed by setting a "0" in bit 1 of the CRA if the interrupt flag (bit 7 of CRA) is to be set on a negative transition of the CA1 signal or a "1" if it is to be set on a positive transition.

Note:

A negative transition is defined as a transition from a high to a low, and a positive transition is defined as a transition from a low to a high voltage.

CA2 can act as a totally independent interrupt or as a peripheral control output. As an input (CRA, bit 5 = 0) it acts to set the interrupt flag, bit 6 of CRA, to a logic 1 on the active transition selected by bit 4 of CRA.

These control register bits and interrupt inputs serve the same basic function as that described above for CA1. The input signal sets the interrupt flag which serves as the link between the peripheral device and the processor interrupt structure. The interrupt disable bit allows the processor to exercise control over the system interrupt.

In the output mode (CRA, bit 5 = 1), CA2 can operate independently to generate a simple pulse each time the microprocessor reads the data on the Peripheral A I/O port. This mode is selected by setting CRA, bit 4 to a 0 and CRA, bit 3 to a 1. This pulse output can be used to control the counters, shift registers, etc., which make sequential data available on the Peripheral input lines.

CONTROL REGISTER A (CRA)

CA2 INPUT MODE (BIT 5 = 0)

7	6	5	4	3	2	1	0
IRQA1 FLAG	IRQA2 FLAG	CA2 INPUT MODE SELECT (=0)	IRQA2 POSITIVE TRANSITION	$\overline{\text{IRQA}}$ ENABLE FOR IRQA2	ORA SELECT	IRQA1 POSITIVE TRANSITION	$\overline{\text{IRQA}}$ ENABLE FOR IRQA1
			IRQA/IRQA2 CONTROL			$\overline{\text{IRQA}}$/IRQA1 CONTROL	

CA2 OUTPUT MODE (BIT 5 = 1)

7	6	5	4	3	2	1	0
IRQA1 FLAG	0	CA2 OUTPUT MODE SELECT (=1)	CA2 OUTPUT CONTROL	CA2 RESTORE CONTROL	ORA SELECT	IRQA1 POSITIVE TRANSITION	$\overline{\text{IRQA}}$ ENABLE FOR IRQA1
			CA2 CONTROL			$\overline{\text{IRQA}}$/IRQA1 CONTROL	

CA2 INPUT OR OUTPUT MODE (BIT 5 = 0 or 1)

Bit 7 IRQA1 FLAG
- 1 A transition has occurred on CA1 that satisfies the bit 1 IRQA1 transition polarity criteria This bit is cleared by a read of Output Register A or by $\overline{\text{RES}}$
- 0 No transition has occurred on CA1 that satisfies the bit 1 IRQA1 transition polarity criteria

Bit 2 OUTPUT REGISTER A SELECT
- 1 Select Output Register A
- 0 Select Data Direction Register A

Bit 1 IRQA1 POSITIVE TRANSITION
- 1 Set IRQA1 Flag (bit 7) on a positive (low-to-high) transition of CA1
- 0 Set IRQA1 Flag (bit 7) on a negative (high-to-low) transition of CA1

Bit 0 $\overline{\text{IRQA}}$ ENABLE FOR IRQA1
- 1 Enable assertion of $\overline{\text{IRQA}}$ when IRQA1 Flag (bit 7) is set
- 0 Disable assertion of $\overline{\text{IRQA}}$ when IRQA1 Flag (bit 7) is set

CA2 INPUT MODE (BIT 5 = 0)

Bit 6 IRQA2 FLAG
- 1 A transition has occurred on CA2 that satisfies the bit 4 IRQA2 transition polarity criteria This flag is cleared by a read of Output Register A or by $\overline{\text{RES}}$
- 0 No transition has occurred on CA2 that satisfies the bit 4 IRQA2 transition polarity criteria

Bit 5 CA2 MODE SELECT
- 0 Select CA2 Input Mode

Bit 4 IRQA2 POSITIVE TRANSITION
- 1 Set IRQA2 Flag (bit 6) on a positive (low-to-high) transition of CA2
- 0 Set IRQA2 Flag (bit 6) on a negative (high-to-low) transition of CA2

Bit 3 $\overline{\text{IRQA}}$ ENABLE FOR IRQA2
- 1 Enable assertion of $\overline{\text{IRQA}}$ when IRQA2 Flag (bit 6) is set
- 0 Disable assertion of $\overline{\text{IRQA}}$ when IRQA2 Flag (bit 6) is set.

CA2 OUTPUT MODE (BIT 5 = 1)

Bit 6 NOT USED
- 0 Always zero

Bit 5 CA2 MODE SELECT
- 1 Select CA2 Output Mode

Bit 4 CA2 OUTPUT CONTROL
- 1 CA2 goes low when a zero is written into CRA bit 3 CA2 goes high when a one is written into CRA bit 3
- 0 CA2 goes low on the first negative (high-to-low) Ø2 clock transition following a read of Output Register A CA2 returns high as specified by bit 3.

Bit 3 CA2 READ STROBE RESTORE CONTROL (4 = 0)
- 1 CA2 returns high on the next Ø2 clock negative transition following a read of Output Register A.
- 0 CA2 returns high on the next active CA1 transition following a read of Output Register A as specified by bit 1.

Figure 4. Control Line Operations Summary (1 of 2)

CONTROL REGISTER B (CRB)

CB2 INPUT MODE (BIT 5 = 0)

7	6	5	4	3	2	1	0
IRQB1 FLAG	IRQB2 FLAG	CB2 INPUT MODE SELECT (=0)	IRQB2 POSITIVE TRANSITION	$\overline{\text{IRQB}}$ ENABLE FOR IRQB2	ORB SELECT	IRQB1 POSITIVE TRANSITION	$\overline{\text{IRQB}}$ ENABLE FOR IRQB1
			$\overline{\text{IRQB}}$/IRQB2 CONTROL			$\overline{\text{IRQB}}$/IRQB1 CONTROL	

CB2 OUTPUT MODE (BIT 5 = 1)

7	6	5	4	3	2	1	0
IRQB1 FLAG	0	CB2 OUTPUT MODE SELECT (=1)	CB2 OUTPUT CONTROL	CB2 RESTORE CONTROL	ORB SELECT	IRQB1 POSITIVE TRANSITION	$\overline{\text{IRQB}}$ ENABLE FOR IRQB1
			CB2 CONTROL			$\overline{\text{IRQB}}$/IRQB1 CONTROL	

CB2 INPUT OR OUTPUT MODE (BIT 5 = 0 or 1)

Bit 7 IRQB1 FLAG
- 1 A transition has occurred on CB1 that satisfies the bit 1 IRQB1 transition polarity criteria. This bit is cleared by a read of Output Register B or by $\overline{\text{RES}}$.
- 0 No transition has occurred on CB1 that satisfies the bit 1 IRQB1 transition polarity criteria.

Bit 2 OUTPUT REGISTER B SELECT
- 1 Select Output Register B.
- 0 Select Data Direction Register B.

Bit 1 IRQB1 POSITIVE TRANSITION
- 1 Set IRQB1 Flag (bit 7) on a positive (low-to-high) transition of CB1.
- 0 Set IRQB1 Flag (bit 7) on a negative (high-to-low) transition of CB1.

Bit 0 $\overline{\text{IRQB}}$ ENABLE FOR IRQB1
- 1 Enable assertion of $\overline{\text{IRQB}}$ when IRQB1 Flag (bit 7) is set.
- 0 Disable assertion of $\overline{\text{IRQB}}$ when IRQB1 Flag (bit 7) is set.

CB2 INPUT MODE (BIT 5 = 0)

Bit 6 IRQB2 FLAG
- 1 A transition has occurred on CB2 that satisfies the bit 4 IRQB2 transition polarity criteria. This flag is cleared by a read of Output Register B or by $\overline{\text{RES}}$.
- 0 No transition has occurred on CB2 that satisfies the bit 4 IRQB2 transition polarity criteria.

Bit 5 CB2 MODE SELECT
- 0 Select CB2 Input Mode.

Bit 4 IRQB2 POSITIVE TRANSITION
- 1 Set IRQB2 Flag (bit 6) on a positive (low-to-high) transition of CB2.
- 0 Set IRQB2 Flag (bit 6) on a negative (high-to-low) transition of CB2.

Bit 3 $\overline{\text{IRQB}}$ ENABLE FOR IRQB2
- 1 Enable assertion of $\overline{\text{IRQB}}$ when IRQB2 Flag (bit 6) is set.
- 0 Disable assertion of $\overline{\text{IRQB}}$ when IRQB2 Flag (bit 6) is set.

CB2 OUTPUT MODE (BIT 5 = 1)

Bit 6 NOT USED
- 0 Always zero.

Bit 5 CB2 MODE SELECT
- 1 Select CB2 Output Mode.

Bit 4 CB2 OUTPUT CONTROL
- 1 CB2 goes low when a zero is written into CRB bit 3 CB2 goes high when a one is written into CRB bit 3.
- 0 CB2 goes low on the first negative (high-to-low) Ø2 clock transition following a write to Output Register B. CB2 returns high as specified by bit 3.

Bit 3 CB2 WRITE STROBE RESTORE CONTROL (BIT 4 = 0)
- 1 CB2 returns high on the next Ø2 clock negative transition following a write to Output Register B.
- 0 CB2 returns high on the next active CB1 transition following a write to Output Register B as specified by bit 1.

Figure 4. Control Line Operations Summary (2 of 2)

A second output mode allows CA2 to be used in conjunction with CA1 to "handshake" between the processor and the peripheral device. On the A side, this technique allows positive control of data transfers from the peripheral device into the microprocessor. The CA1 input signals the processor that data is available by interrupting the processor. The processor reads the data and sets CA2 low. This signals the peripheral device that it can make new data available.

The final output mode can be selected by setting bit 4 of CRA to a 1. In this mode, CA2 is a simple peripheral control output which can be set high or low by setting bit 3 or CRA to a 1 or a 0 respectively.

CB1 operates as an interrupt input only in the same manner as CA1. Bit 7 of CRB is set by the active transition selected by bit 0 of CRB. Likewise, the CB2 input mode operates exactly the same as the CA2 input modes. The CB2 output modes, CRB bit 5 = 1, differ somewhat from those of CA2. The pulse output occurs when the processor writes data into the Peripheral B Output Register. Also, the "handshaking" operates on data transfers from the processor into the peripheral device.

READING THE PERIPHERAL A I/O PORT

Performing a Read operation with RS1 = 0, RS0 = 0 and the Data Direction Register Access Control bit (CRA-2) = 1, directly transfers the data on the Peripheral A I/O lines to the data bus. In this situation, the data bus will contain both the input and output data. The processor must be programmed to recognize and interpret only those bits which are important to the particular peripheral operation being performed.

Since the processor always reads the Peripheral A I/O port pins instead of the actual Peripheral Output Register (ORA), it is possible for the data read by the processor to differ from the contents of the Peripheral Output Register for an output line. This is true when the I/O pin is not allowed to go to a full +2.4V DC when the Peripheral Output register contains a logic 1. In this case, the processor will read a 0 from the Peripheral A pin, even though the corresponding bit in the Peripheral Output register is a 1.

READING THE PERIPHERAL B I/O PORT

Reading the Peripheral B I/O port yields a combination of input and output data in a manner similar to the Peripheral A port. However, data is read directly from the Peripheral B Output Register (ORB) for those lines programmed to act as outputs. It is therefore possible to load down the Peripheral B Output lines without causing incorrect data to be transferred back to the processor on a Read operation.

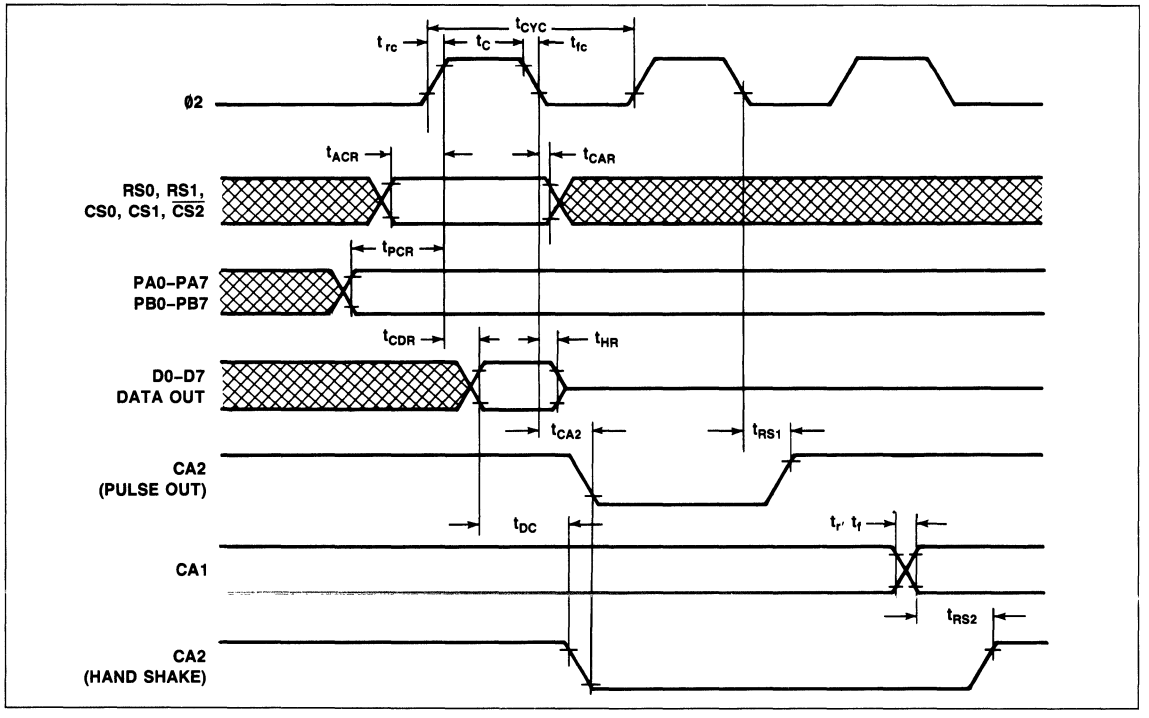


Figure 5. Read Timing Waveforms

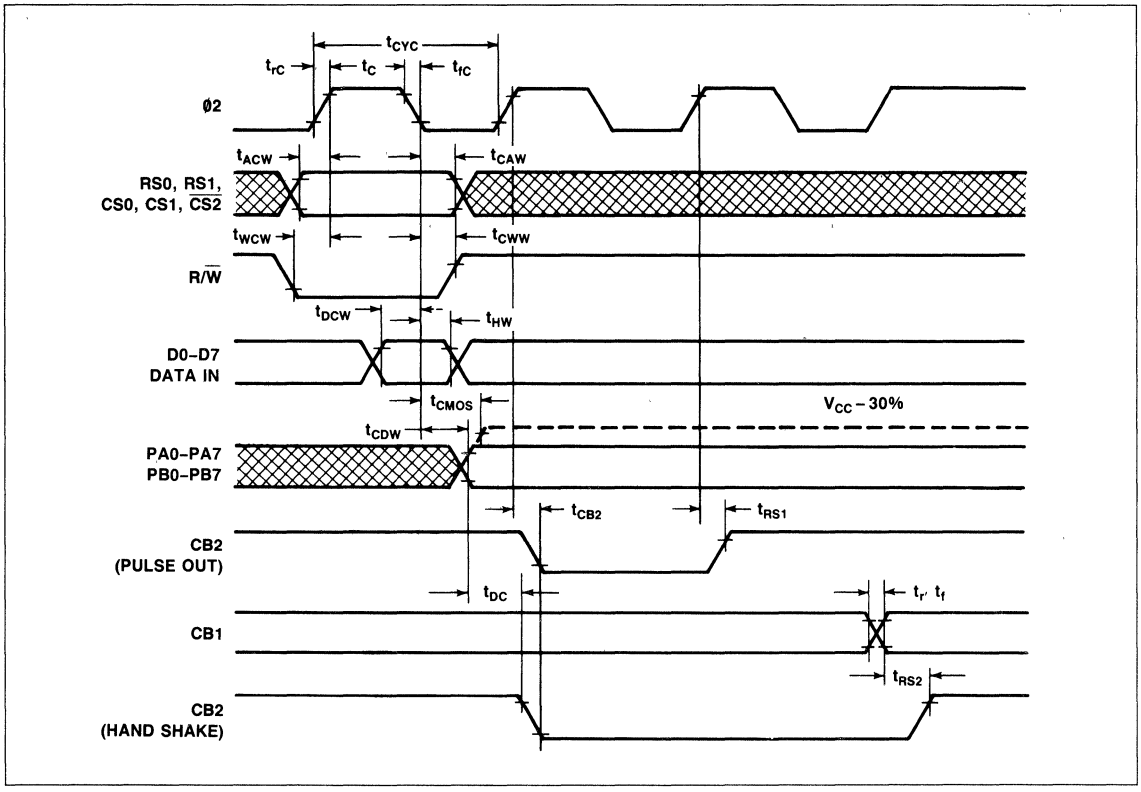


Figure 6. Write Timing Waveforms

BUS TIMING CHARACTERISTICS

Parameter	Symbol	1 MHz		2 MHz		Unit
		Min.	Max.	Min.	Max.	
Ø2 Cycle	t_{CYC}	1.0	—	0.5	—	μs
Ø2 Pulse Width	t_C	470	25	235	25	ns
Ø2 Rise and Fall Time	t_{rc}, t_{fc}	—	25	—	15	ns

READ TIMING

Address Set-Up Time	t_{ACR}	150	—	90	—	ns
Address Hold Time	t_{CAR}	0	—	0	—	ns
Peripheral Data Set-Up Time	t_{PCR}	300	—	150	—	ns
Data Bus Delay Time	t_{CDR}	—	395	—	190	ns
Data Bus Hold Time	t_{HR}	10	—	10	—	ns

WRITE TIMING

Address Set-Up Time	t_{ACW}	180	—	90	—	ns
Address Hold Time	t_{CAW}	0	—	0	—	ns
R/$\overline{W}$ Set-Up Time	t_{WCW}	130	—	65	—	ns
R/$\overline{W}$ Hold Time	t_{CWW}	50	—	25	—	ns
Data Bus Set-Up Time	t_{DCW}	300	—	150	—	ns
Data Bus Hold Time	t_{HW}	10	—	10	—	ns
Peripheral Data Delay Time	t_{CPW}	—	1.0	—	0.5	μs
Peripheral Data Delay Time to CMOS Level	t_{CMOS}	—	2.0	—	1.0	μs

PERIPHERAL INTERFACE TIMING

Peripheral Data Set-Up	t_{PCR}	300	—	150	—	ns
Ø2 Low to CA2 Low Delay	t_{CA2}	—	1.0	—	0.5	μs
Ø2 Low to CA2 High Delay	t_{RS1}	—	1.0	—	0.5	μs
CA1 Active to CA2 High Delay	t_{RS2}	—	2.0	—	1.0	μs
Ø2 High to CB2 Low Delay	t_{CB2}	—	1.0	—	0.5	μs
Peripheral Data Valid to CB2 Low Delay	t_{DC}	0	1.5	0	0.75	μs
Ø2 High to CB2 High Delay	t_{RS1}	—	1.0	—	0 5	μs
CB1 Active to CB2 High Delay	t_{RS2}	—	2.0	—	1.0	μs
CA1, CA2, CB1 and CB2 Input Rise and Fall Time	t_r, t_f	—	1.0	—	1.0	μs

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to +7.0	Vdc
Input Voltage	V_{IN}	−0.3 to $+V_{CC}$	Vdc
Operating Temperature Range Commercial Industrial	T_A	T_L T_H 0 to +70 −40 to +85	°C
Storage Temperature	T_{STG}	−55 to +150	°C

***NOTE:** Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the other sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING CONDITIONS

Parameter	Symbol	Value
Supply Voltage	V_{CC}	5V ±5%
Temperature Range Commercial Industrial	T_A	 0°C to 70°C −40°C to +85°C

DC CHARACTERISTICS

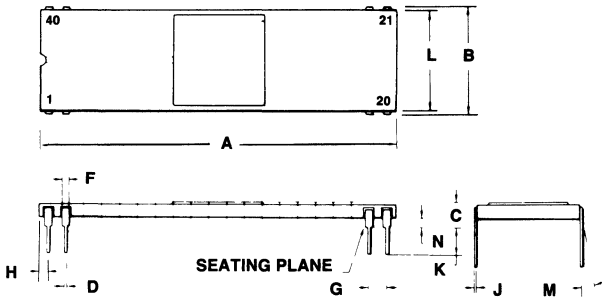
(V_{CC} = 5.0V ±5%, V_{SS} = 0, T_A = T_L to T_H, unless otherwise noted)

Parameter	Symbol	Min.	Typ.[3]	Max.	Unit[1]	Test Conditions
Input High Voltage	V_{IH}	+2.0	—	V_{CC}	V	
Input Low Voltage	V_{IL}	−0.3	—	+0.8	V	
Input Leakage Current R/W, RES, RS0, RS1, CS0, CS1, CS2, CA1, CB1, ø2	I_{IN}	—	±1	±2.5	µA	V_{IN} = 0V to 5.25V V_{CC} = 0V
Output Leakage Current for Three-State Off D0–D7, PB0–PB7, CB2	I_{TSI}	—	±2	±10	µA	V_{IN} = 0.4V to 2.4V V_{CC} = 5.25V
Input High Current PA0–PA7, CA2	I_{IH}	−100	−250	—	µA	V_{IH} = 2.4V
Input Low Current PA0–PA7, CA2	I_{IL}	—	−1	−1.6	mA	V_{IL} = 0.4V
Output High Voltage All outputs PB0–PB7, CB2 (Darlington Drive)	V_{OH}	 2.4 1.5	 — —	 — —	 V V	V_{CC} = 4.75V I_{LOAD} = −100µA I_{LOAD} = −1.0 mA
Output Low Voltage	V_{OL}	—	—	+0.4	V	V_{CC} = 4.75V I_{LOAD} = 1.6 mA
Output High Current (Sourcing) Logic PB0–PB7, CB2 (Darlington Drive)	I_{OH}	 −100 −1.0	 −1000 −2.5	 — −10	 µA mA	 V_{OH} = 2.4V V_{OH} = 1.5V
Output Low Current (Sinking)	I_{OL}	1.6	—	—	mA	V_{OL} = 0.4V
Output Leakage Current (Off State) IRQA, IRQB	I_{OFF}	—	1	±10	µA	V_{OH} = 2.4V V_{CC} = 5.25V
Power Dissipation	P_D		200	500	mW	
Input Capacitance D0–D7, PA0–PA7, PB0–PB7, CA2, CB2 R/W, RES, RS0, RS1, CS0, CS1, CS2 CA1, CB1, ø2	C_{IN}	 — — —	 — — —	 10 7.0 20	pF	V_{CC} = 5.0V V_{IN} = 0V f = 2 MHz T_A = 25°C
Output Capacitance	C_{OUT}	—	—	10	pF	

Notes:
1. All units are direct current (dc) except for capacitance.
2. Negative sign indicates outward current flow, positive indicates inward flow.
3. Typical values are shown for V_{CC} = 5.0V and T_A = 25°C.

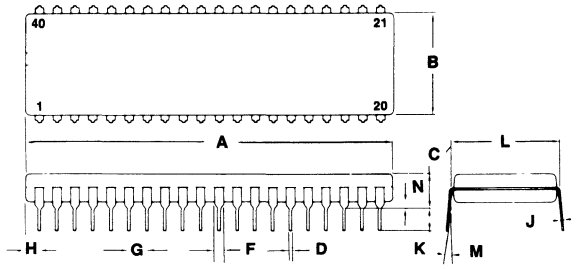
PACKAGE DIMENSIONS

40-PIN CERAMIC DIP



DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	50 29	51 31	1 980	2 020
B	14 86	15 62	0 585	0 615
C	2 54	4 19	0 100	0 165
D	0 38	0 53	0 015	0 021
F	0 76	1 40	0 030	0 055
G	2 54 BSC		0 100 BSC	
H	0 76	1 78	0 030	0 070
J	0 20	0 33	0 008	0 013
K	2 54	4 19	0 100	0 165
L	14 60	15 37	0 575	0 605
M	0	10°	0	10
N	0 51	1 52	0 020	0 060

40-PIN PLASTIC DIP



DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	51 28	52 32	2 040	2 060
B	13 72	14 22	0 540	0 560
C	3 55	5 08	0 140	0 200
D	0 36	0 51	0 014	0 020
F	1 02	1 52	0 040	0 060
G	2 54 BSC		0 100 BSC	
H	1 65	2 16	0 065	0 085
J	0 20	0 30	0 008	0 012
K	3 05	3 56	0 120	0 140
L	15 24 BSC		0 600 BSC	
M	7	10	7	10
N	0 51	1 02	0 020	0 040

Rockwell

R6522
VERSATILE INTERFACE ADAPTER (VIA)

DESCRIPTION

The R6522 Versatile Interface Adapter (VIA) is a very flexible I/O control device. In addition, this device contains a pair of very powerful 16-bit interval timers, a serial-to-parallel/parallel-to serial shift register and input data latching on the peripheral ports. Expanded handshaking capability allows control of bidirectional data transfers between VIA's in multiple processor systems.

Control of peripheral devices is handled primarily through two 8-bit bidirectional ports. Each line can be programmed as either an input or an output. Several peripheral I/O lines can be controlled directly from the interval timers for generating programmable frequency square waves or for counting externally generated pulses. To facilitate control of the many powerful features of this chip, an interrupt flag register, an interrupt enable register and a pair of function control registers are provided.

FEATURES

- Two 8-bit bidirectional I/O ports
- Two 16-bit programmable timer/counters
- Serial data port
- TTL compatible
- CMOS compatible peripheral control lines
- Expanded "handshake" capability allows positive control of data transfers between processor and peripheral devices.
- Latched output and input registers
- 1 MHz and 2 MHz operation
- Single +5V power supply

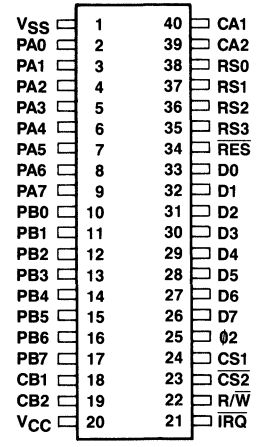
ORDERING INFORMATION

Part Number:
R6522

Temperature Range
Blank = 0°C to +70°C
R = −40°C to +85°C

Package
C = Ceramic
P = Plastic

Frequency
No Letter = 1 MHz
A = 2 MHz



R6522 Pin Configuration

INTERFACE SIGNALS

RESET ($\overline{RES}$)

A low reset ($\overline{RES}$) input clears all R6522 internal registers to logic 0 (except T1 and T2 latches and counters and the Shift Register). This places all peripheral interface lines in the input state, disables the timers, shift register, etc. and disables interrupting from the chip.

INPUT CLOCK (PHASE 2)

The input clock is the system $\phi 2$ clock and triggers all data transfers between processor bus and the R6522

READ/WRITE (R/$\overline{W}$)

The direction of the data transfers between the R6522 and the system processor is controlled by the R/$\overline{W}$ line in conjunction with the CS1 and $\overline{CS2}$ inputs. When R/$\overline{W}$ is low, (write operation) and the R6522 is selected, data is transferred from the processor bus into the selected R6522 register. When R/$\overline{W}$ is high, (read operation) and the R6522 is selected, data is transferred from the selected R6422 register to the processor bus.

DATA BUS (D0-D7)

The eight bidirectional data bus lines transfer data between the R6522 and the system processor bus. During read cycles, the contents of the selected R6522 register are placed on the data bus lines. During write cycles, these lines are high-impedance inputs and data is transferred from the processor bus into the selected register. When the R6522 is not selected, the data bus lines are high-impedance.

CHIP SELECTS (CS1, $\overline{CS2}$)

The two chip select inputs are normally connected to processor address lines either directly or through decoding. The selected R6522 register is accessed when CS1 is high and $\overline{CS2}$ is low.

REGISTER SELECTS (RS0-RS3)

The coding of the four Register Select inputs select one of the 16 internal registers of the R6522, as shown in Table 1.

INTERRUPT REQUEST ($\overline{IRQ}$)

The Interrupt Request output goes low whenever an internal interrupt flag is set and the corresponding interrupt enable bit is a logic 1. This output is open-drain to allow the interrupt request signal to be wire-OR'ed with other equivalent signals in the system.

PERIPHERAL PORT A (PA0-PA7)

Port A consists of eight lines which can be individuallly programmed to act as inputs or outputs under control of Data Direction Register A. The polarity of output pins is controlled by an Output Register and input data may be latched into an internal register under control of the CA1 line. All of these modes of operation are controlled by the system processor through the internal control registers. These lines represent one standard TTL load in the input mode and will drive one standard TTL load in the output mode. Figure 2 illustrates the output circuit.

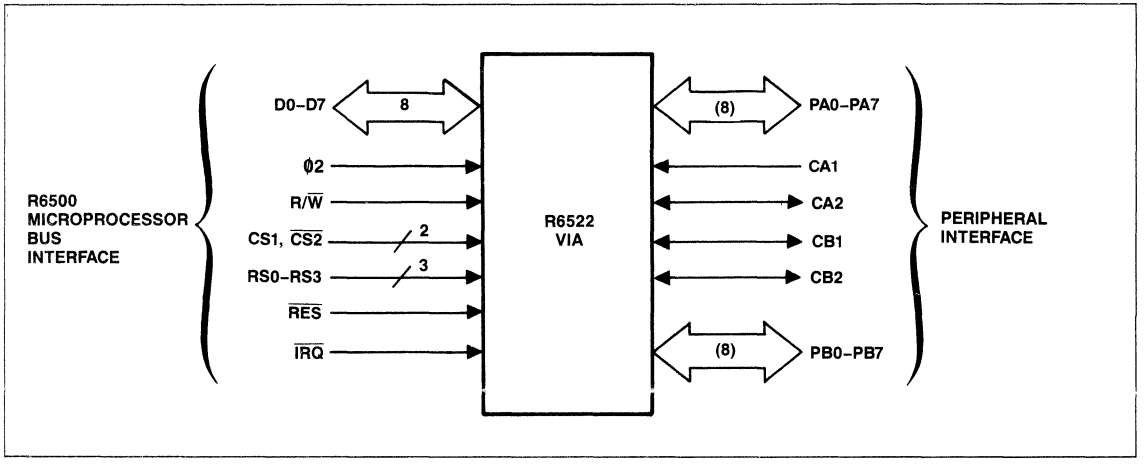


Figure 1. R6522 VIA Interface Signals

PORT A CONTROL LINES (CA1, CA2)

The two Port A control lines act as interrupt inputs or as handshake outputs. Each line controls an internal interrupt flag with a corresponding interrupt enable bit. In addition, CA1 controls the latching of data on Port A input lines. CA1 is a high-impedance input only while CA2 represents one standard TTL load in the input mode. CA2 will drive one standard TTL load in the output mode.

PORT B (PB0–PB7)

Peripheral Port B consists of eight bidirectional lines which are controlled by an output register and a data direction register in much the same manner as the Port A. In addition, the polarity of the PB7 output signal can be controlled by one of the interval timers while the second timer can be programmed to count pulses on the PB6 pin. Port B lines represent one standard TTL load in the input mode and will drive one standard TTL load in the output mode. In addition, they are capable of sourcing 1.0 mA at 1.5 Vdc in the output mode to allow the outputs to directly drive Darlington transistor circuits. Figure 3 is the circuit schematic.

PORT B CONTROL LINES (CB1, CB2)

The Port B control lines act as interrupt inputs or as handshake outputs. As with CA1 and CA2, each line controls an interrupt flag with a corresponding interrupt enable bit. In addition, these lines act as a serial port under control of the Shift Register. These lines represent one standard TTL load in the input mode and will drive one standard TTL load in the output mode. CB2 *can* also drive a Darlington transistor circuit; however, CB1 *cannot*.

Table 1. R6522 Register Addressing

Register Number	RS Coding				Register Desig.	Register/Description	
	RS3	RS2	RS1	RS0		Write (R/$\overline{W}$ = L)	Read (R/$\overline{W}$ = H)
0	0	0	0	0	ORB/IRB	Output Register B	Input Register B
1	0	0	0	1	ORA/IRA	Output Register A	Input Register A
2	0	0	1	0	DDRB	Data Direction Register B	
3	0	0	1	1	DDRA	Data Direction Register A	
4	0	1	0	0	T1C-L	T1 Low-Order Latches	T1 Low-Order Counter
5	0	1	0	1	T1C-H	T1 High-Order Counter	
6	0	1	1	0	T1L-L	T1 Low-Order Latches	
7	0	1	1	1	T1L-H	T1 High-Order Latches	
8	1	0	0	0	T2C-L	T2 Low-Order Latches	T2 Low-Order Counter
9	1	0	0	1	T2C-H	T2 High-Order Counter	
10	1	0	1	0	SR	Shift Register	
11	1	0	1	1	ACR	Auxiliary Control Register	
12	1	1	0	0	PCR	Peripheral Control Register	
13	1	1	0	1	IFR	Interrupt Flag Register	
14	1	1	1	0	IER	Interrupt Enable Register	
15	1	1	1	1	ORA/IRA	Output Register A*	Input Register A*

NOTE: *Same as Register 1 except no handshake.

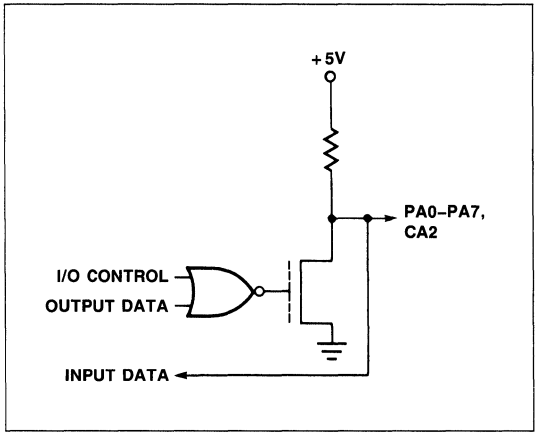


Figure 2. Port A Output Circuit

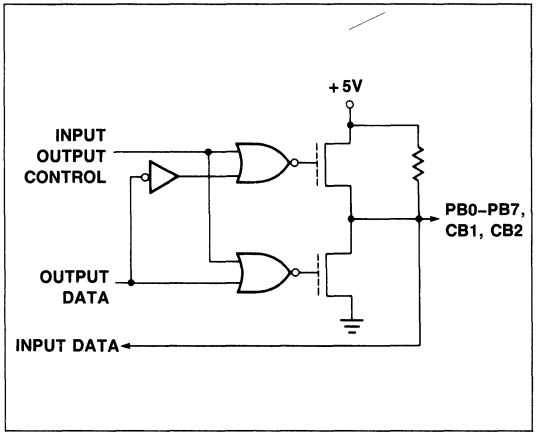


Figure 3. Port B Output Circuit

FUNCTIONAL DESCRIPTION

The internal organization of the R6522 VIA is illustrated in Figure 4.

PORT A AND PORT B OPERATION

The R6522 VIA has two 8-bit bidirectional I/O ports (Port A and Port B) and each port has two associated control lines.

Each 8-bit peripheral port has a Data Direction Register (DDRA, DDRB) for specifying whether the peripheral pins are to act as inputs or outputs. A 0 in a bit of the Data Direction Register causes the corresponding peripheral pin to act as an input. A 1 causes the pin to act as an output.

Each peripheral pin is also controlled by a bit in the Output Register (ORA, ORB) and the Input Register (IRA, IRB). When the pin is programmed as an output, the voltage on the pin is controlled by the corresponding bit of the Output Register. A 1 in the Output Register causes the output to go high, and a "0" causes the output to go low. Data may be written into Output Register bits corresponding to pins which are programmed as inputs. In this case, however, the output signal is unaffected.

Reading a peripheral port causes the contents of the Input Register (IRA, IRB) to be transferred onto the Data Bus. With input latching disabled, IRA will always reflect the levels on the PA pins. With input latching enabled, IRA will reflect the levels on the PA pins at the time the latching occurred (via CA1).

The IRB register operates similar to the IRA register. However, for pins programmed as outputs there is a difference. When reading IRA, the *level on the pin* determines whether a 0 or a 1 is sensed. When reading IRB, however, the bit stored in the *output register,* ORB, is the bit sensed. Thus, for outputs which have large loading effects and which pull an output "1" down or which pull an output "0" up, reading IRA may result in reading a "0" when a "1" was actually programmed, and reading a "1" when a "0" was programmed. Reading IRB, on the other hand, will read the "1" or "0" level actually programmed, no matter what the loading on the pin.

Figures 5 through 8 illustrate the formats of the port registers. In addition, the input latching modes are selected by the Auxiliary Control Register (Figure 14).

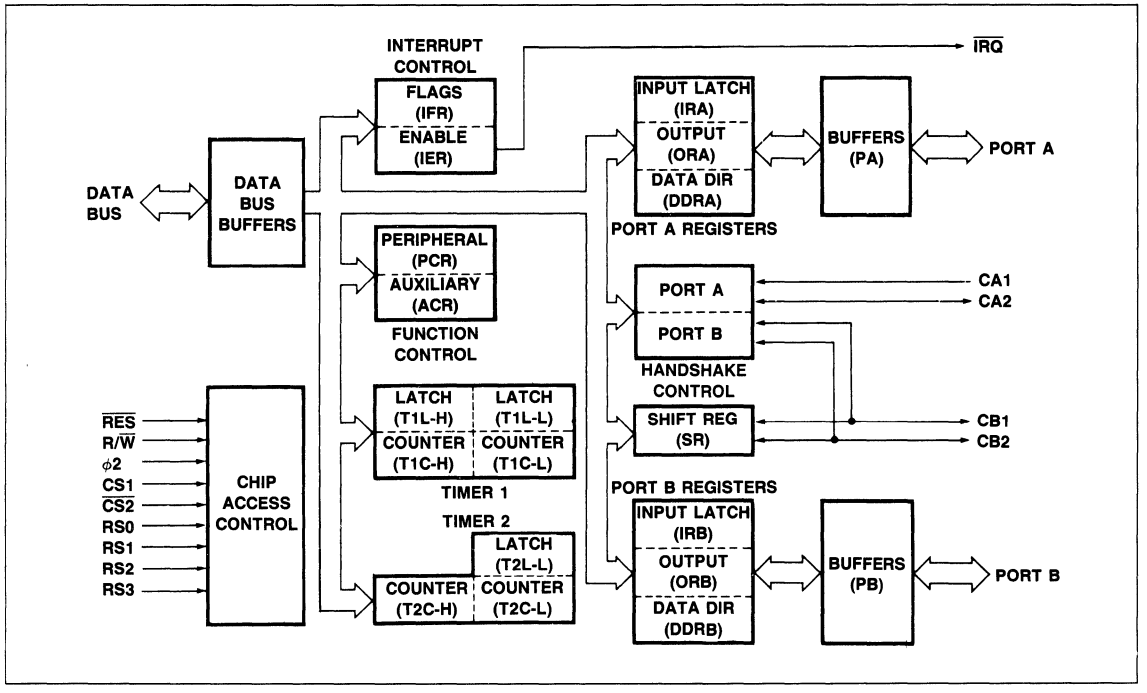


Figure 4. R6522 VIA Block Diagram

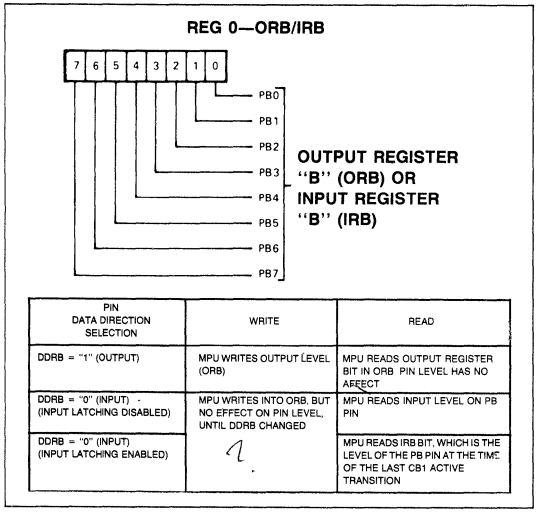
HANDSHAKE CONTROL OF DATA TRANSFERS

The R6522 allows positive control of data transfers between the system processor and peripheral devices through the operation of "handshake" lines. Port A lines (CA1, CA2) handshake data on both a read and a write operation while the Port B lines (CB1, CB2) handshake on a write operation only.

Read Handshake

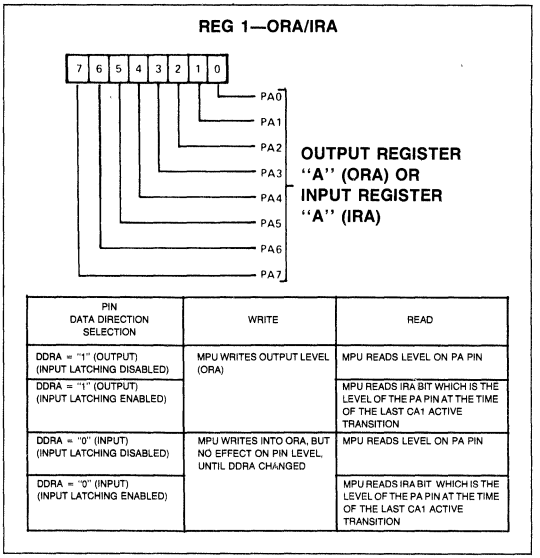
Positive control of data transfers from peripheral devices into the system processor can be accomplished very effectively using Read Handshaking. In this case, the peripheral device must generate the equivalent of a "Data Ready" signal to the processor signifying that valid data is present on the peripheral port. This signal normally interrupts the processor, which then reads the data, causing generation of a "Data Taken" signal. The peripheral device responds by making new data available. This process continues until the data transfer is complete.

In the R6522, automatic "Read" Handshaking is possible on the Peripheral A port only. The CA1 interrupt input pin accepts the "Data Ready" signal and CA2 generates the "Data Taken" signal. The "Data Ready" signal will set an internal flag which may interrupt the processor or which may be polled under program control. The "Data Taken" signal can either be a pulse or a level which is set low by the system processor and is cleared by the "Data Ready" signal. These options are shown in Figure 9 which illustrates the normal Read Handshake sequence.



PIN DATA DIRECTION SELECTION	WRITE	READ
DDRB = "1" (OUTPUT)	MPU WRITES OUTPUT LEVEL (ORB)	MPU READS OUTPUT REGISTER BIT IN ORB. PIN LEVEL HAS NO AFFECT
DDRB = "0" (INPUT) (INPUT LATCHING DISABLED)	MPU WRITES INTO ORB, BUT NO EFFECT ON PIN LEVEL, UNTIL DDRB CHANGED	MPU READS INPUT LEVEL ON PB PIN
DDRB = "0" (INPUT) (INPUT LATCHING ENABLED)		MPU READS IRB BIT, WHICH IS THE LEVEL OF THE PB PIN AT THE TIME OF THE LAST CB1 ACTIVE TRANSITION

Figure 5. Output Register B (ORB), Input Register B (IRB)



PIN DATA DIRECTION SELECTION	WRITE	READ
DDRA = "1" (OUTPUT) (INPUT LATCHING DISABLED)	MPU WRITES OUTPUT LEVEL (ORA)	MPU READS LEVEL ON PA PIN
DDRA = "1" (OUTPUT) (INPUT LATCHING ENABLED)		MPU READS IRA BIT WHICH IS THE LEVEL OF THE PA PIN AT THE TIME OF THE LAST CA1 ACTIVE TRANSITION
DDRA = "0" (INPUT) (INPUT LATCHING DISABLED)	MPU WRITES INTO ORA, BUT NO EFFECT ON PIN LEVEL, UNTIL DDRA CHANGED	MPU READS LEVEL ON PA PIN
DDRA = "0" (INPUT) (INPUT LATCHING ENABLED)		MPU READS IRA BIT WHICH IS THE LEVEL OF THE PA PIN AT THE TIME OF THE LAST CA1 ACTIVE TRANSITION

Figure 6. Output Register A (ORA), Input Register A (IRA)

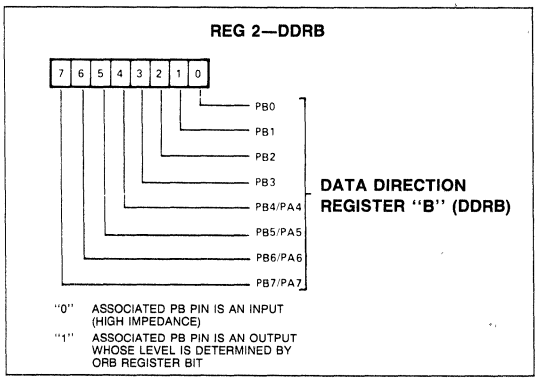


Figure 7. Data Direction Register B (DDRB)

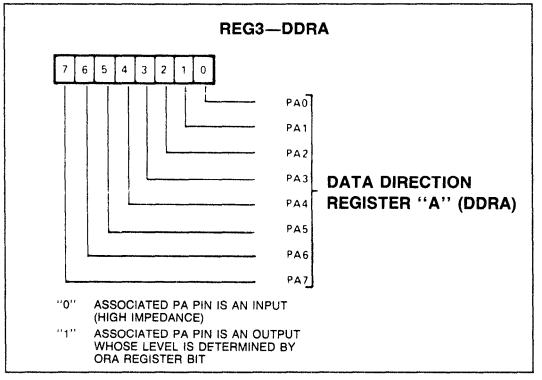


Figure 8. Data Direction Register A (DDRA)

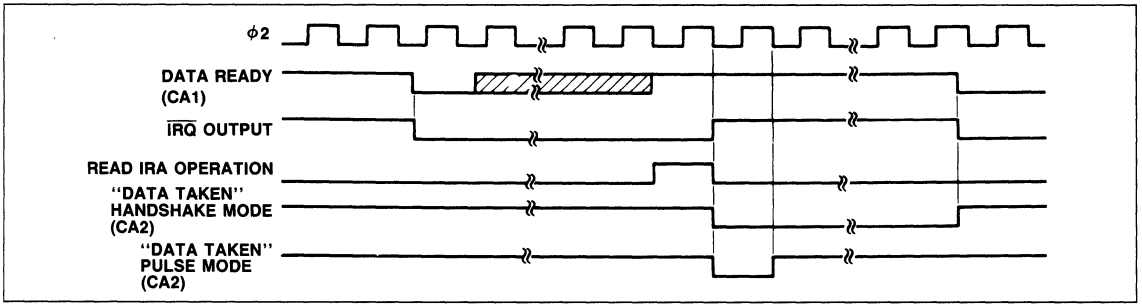


Figure 9. Read Handshake Timing (Port A Only)

Write Handshake

The sequence of operations which allows handshaking data from the system processor to a peripheral device is very similar to that described for Read Handshaking. However, for Write Handshaking, the R6522 generates the "Data Ready" signal and the peripheral device must respond with the "Data Taken" signal. This can be accomplished on both the PA port and the PB port on the R6522. CA2 or CB2 act as a "Data Ready" output in either the handshake mode or pulse mode and CA1 or CB1 accept the "Data Taken" signal from the peripheral device, setting the interrupt flag and clearing the "Data Ready" output. This sequence is shown in Figure 10.

Selection of operating modes for CA1, CA2, CB1, and CB2 is accomplished by the Peripheral Control Register (Figure 11).

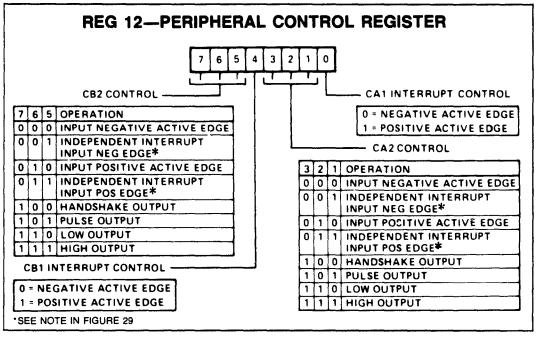


Figure 11. Peripheral Control Register (PCR)

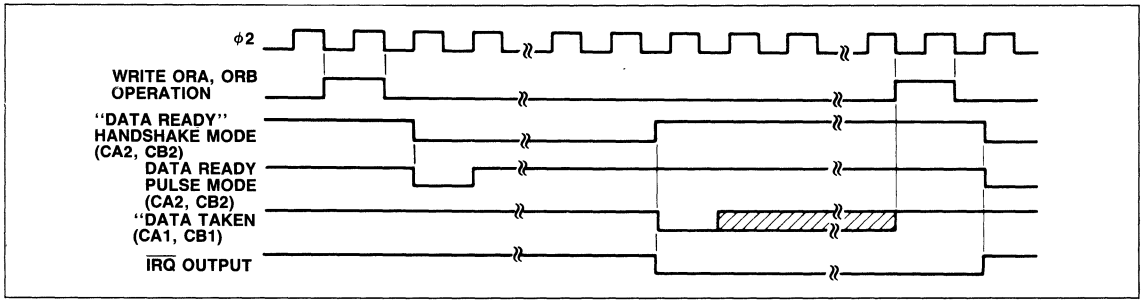


Figure 10. Write Handshake Timing

COUNTER/TIMERS

There are two independent 16-bit counter/timers (called Timer 1 and Timer 2) in the R6522. Each timer is controlled by writing bits into the Auxiliary Control Register (ACR) to select the mode of operation (Figure 14.

Timer 1 Operation

Interval Timer T1 consists of two 8-bit latches (Figure 12) and a 16-bit counter (Figure 13). The latches store data which is to be loaded into the counter. After loading, the counter decrements at Ø2 clock rate. Upon reaching zero, an interrupt flag is set, and $\overline{IRQ}$ goes low if the T1 interrupt is enabled. Timer 1 then disables any further interrupts, automatically transers the contents of the latches into the counter and continues to decrement. In addition, the timer may be programmed to invert the output signal on peripheral pin PB7 each time it "times-out." Each of these modes is discussed separaely below.

Note that the processor does not write directly into the low-order counter (T1C-L). Instead, this half of the counter is loaded automatically from the low order latch (T1L-L) when the processor writes into the high order counter (T1C-H). In fact, it may not be necessary to write to the low order counter in some applications since the timing operation is triggered by writing to the high order latch.

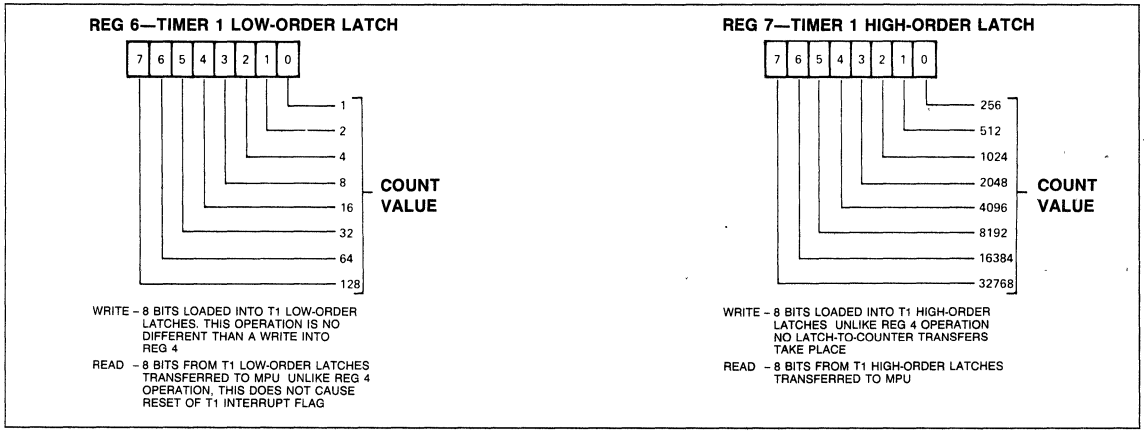


Figure 12. Timer 1 (T1) Latch Registers

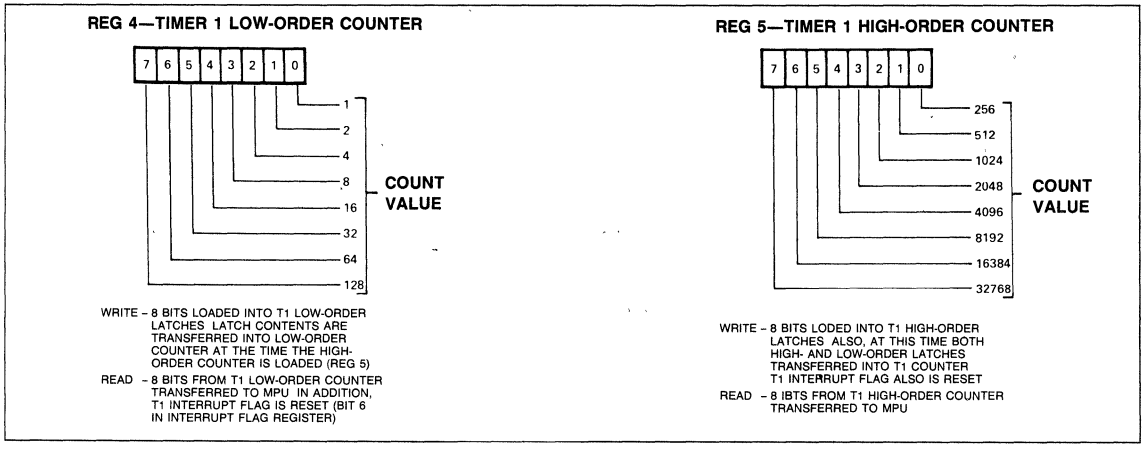


Figure 13. Timer 1 (T1) Counter Registers

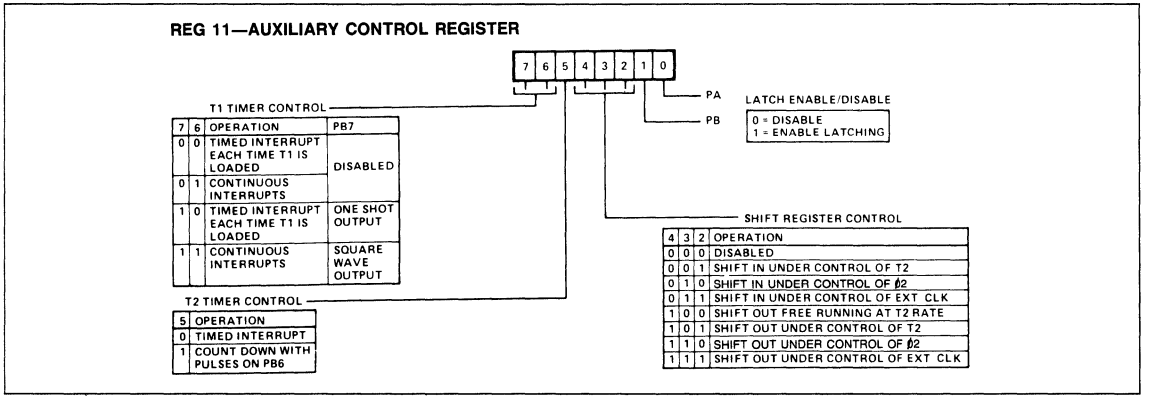


Figure 14. Auxiliary Control Register (ACR)

Timer 1 One-Shot Mode

The Timer 1 one-shor mode generates a single interrupt for each timer load operation. As with any interval timer, the delay between the "write T1C-H" operation and generation of the processor interrupt is a direct function of the data loaded into the timing counter. In addition to generating a single interrupt, Timer 1 can be programmed to produce a single negative pulse on the PB7 peripheral pin. With the output enabled (ACR7 = 1) a "write T1C-H" operation will cause PB7 to go low. PB7 will return high when Timer 1 times out. The result is a single programmable width pulse.

Timing for the R6522 interval timer one-shot modes is shown in Figure 15.

In the one-shot mode, writing into the T1L-H has no effect on the operation of Timer 1. However, it will be necessary to assure that the low order latch contains the proper data before initiating the count-down with a "write T1C-H" operation. When the processor writes into the high order counter (T1C-H), the T1 interrupt flag will be cleared, the contents of the low order latch will be transferred into the low order counter, and the timer will begin to decrement at system clock rate. If the PB7 output is enabled, this signal will go low on the Ø2 following the write operation. When the counter reaches zero, the T1 interrupt flag will be set, the $\overline{IRQ}$ pin will go low (interrupt enabled), and the signal on PB7 will go high. At this time the counter will continue to decrement at system clock rate. This allows the system processor to read the contents of the counter to determine the time since interrupt. However, the T1 interrupt flag cannot be set again unless it has been cleared as described in this specification.

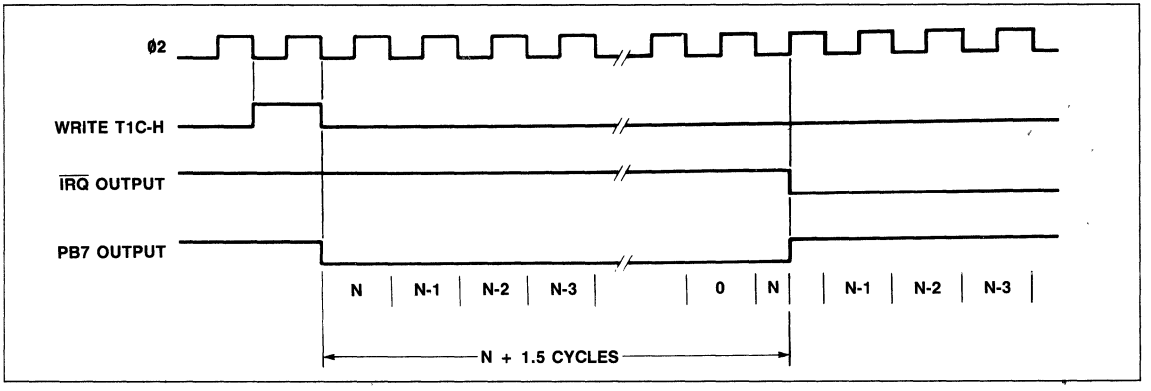


Figure 15. Timer 1 One-Shot Mode Timing

Timer 1 Free-Run Mode

The most important advantage associated with the latches in T1 is the ability to produce a continuous series of evenly spaced interrupts and the ability toproduce a square wave on PB7 whose frequency is not affected by variations in the processor interrupt response time This is accomplished in the "free-running" mode.

In the free-running mode, the interrupt flag is set and the signal on PB7 is inverted each time the counter reaches zero, at which time the timer automatically transfers the contents of the latch into the counter (16 bits) and continues to decrement from there. The interrupt flag can be cleared by writing T1C-H, by reading T1C-L, or by writing directly into the flag as described later. However, it is not necessary to rewrite the timer to enable setting the interrupt flag on the next time-out.

All interval timers in the R6522 are "re-triggerable." Rewriting the counter will always re-initialize the time-out period. In fact, the time-out can be prevented completely if the processor continues to rewrite the timer before it reaches zero. Timer 1 will operate in this manner if the processor writes into the high order counter (T1C-H). However, by loading the latches only, the processor can access the timer during each down-counting operation without affecting the time-out in process. Instead, the data loaded into the latches will determine the length of the next time-out period. This capability is particularly valuable in the free-running mode with the output enabled. In this mode, the signal on PB7 is inverted and the interrupt flag is set with each time-out. By responding to the interrupts with new data for the latches, the processor can determine the period of the next half cycle during each half cycle of the output signal on PB7. In this manner, very complex waveforms can be generated.

A precaution to take in the use of PB7 as the timer output concerns the Data Direction Register contents for PB7. *Both* DDRB bit 7 and ACR bit 7 must be 1 for PB7 to function as the timer output. If one is 1 and the other is 0, then PB7 functions as a normal output pin, controlled by ORB bit 7.

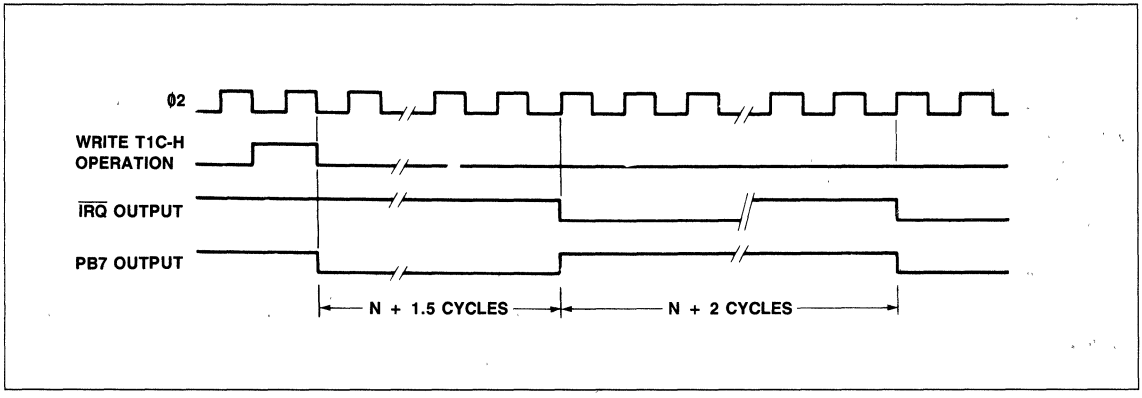


Figure 16. Timer 1 Free-Run Mode Timing

Timer 2 Operation

Timer 2 operates as an interval timer (in the "one-slot" mode only), or as a counter for counting negative pulses on the PB6 peripheral pin. A single control bit in the Auxiliary Control Register selects between these two modes. This timer is comprised of a "write-only" lower-order latch (T2L-L), a "read-only" low-order counter (T2C-L) and a read/write high order counter (T2C-H). The counter registers act as a 16-bit counter which decrements at Ø2 rate. Figure 17 illustrates the T2 Latch/Counter Registers.

Timer 2 One-Shot Mode

As an interval timer, T2 operates in the "one-shot" mode similar to Time 1. In this mode, T2 provides a single interrupt for each "write T2C-H" operation. After timing out, the counter will continue to decrement. However, setting of the interrupt flag is disabled after initial time-out so that it will not be set by the counter decrementing again through zero. The processor must rewrite T2C-H to enable setting of the interrupt flag. The interrupt flag is cleared by reading T2C-L or by writing T2C-H. Timing for this operation is shown in Figure 18.

Timer 2 Pulse Counting Mode

In the pulse counting mode, T2 counts a predetermined number of negative-going pulses on PB6. This is accomplished by first loading a number into T2. Writing into T2C-H clears the interrupt flag and allows the counter to decrement each time a pulse is applied to PB6. The interrupt flag is set when T2 counts down past zero. The counter will then continue to decrement with each pulse on PB6. However, it is necessary to rewrite T2C-H to allow the interrupt flag to set on a subsequent time-out. Timing for this mode is shown in Figure 19. The pulse must be low on the leading edge of Ø2.

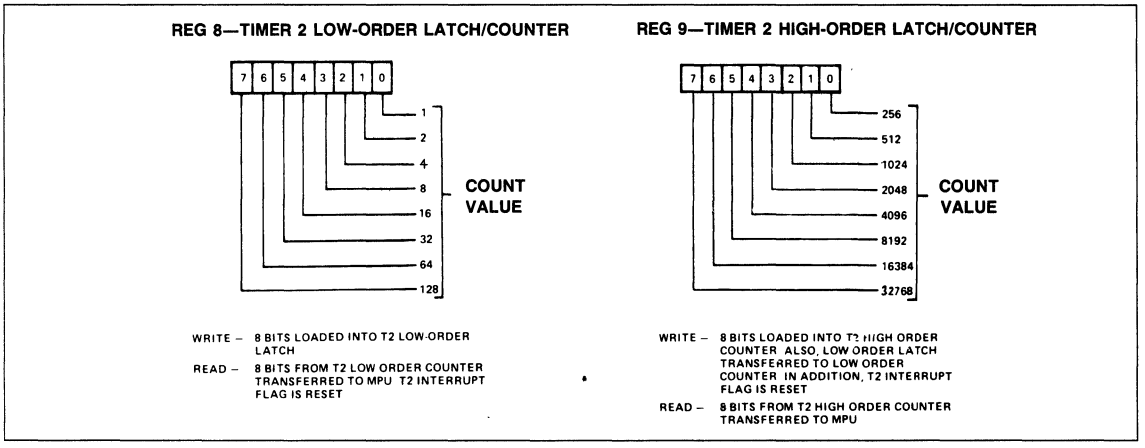


Figure 17. Timer 2 (T2) Latch/Counter Registers

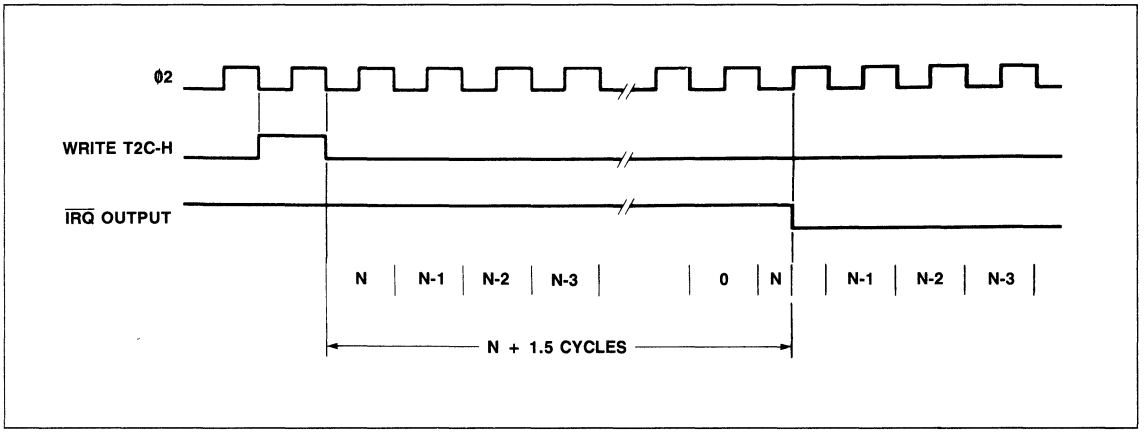


Figure 18. Timer 2 One-Shot Mode Timing

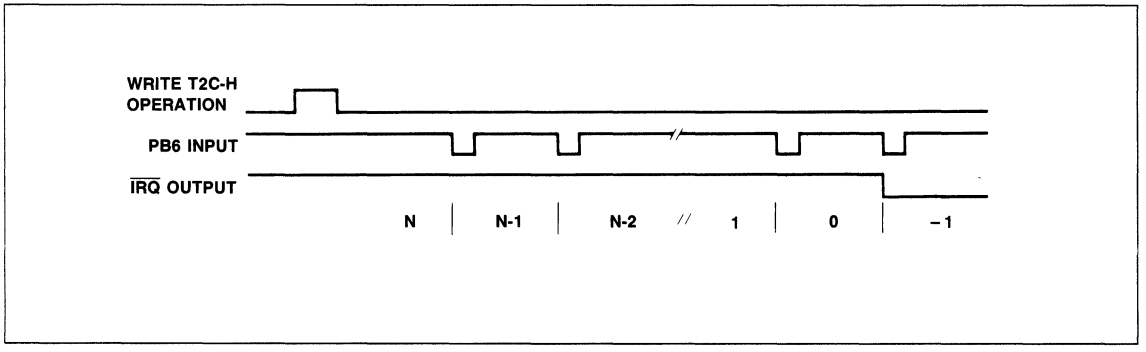


Figure 19. Timer 2 Pulse Counting Mode

SHIFT REGISTER OPERATION

The Shift Register (SR) performs serial data transfers into and out of the CB2 pin under control of an internal modulo-8 counter. Shift pulses can be applied to the CB1 pin from an external source or, with the proper mode selection, shift pulses generated internally will appear on the CB1 pin for controlling external devices.

The control bits which select the various shift register operating modes are located in the Auxiliary Control Register. Figure 20 illustrates the configuration of the SR data bits and Figure 21 shows the SR control bits of the ACR.

SR Mode 0 — Disabled

Mode 0 disables the Shift Register. In this mode the microprocessor can write or read the SR and the SR will shift on each CB1 positive edge shifting in the value on CB2. In this mode the SR interrupt Flag is disabled (held to a logic 0).

SR Mode 1 — Shift In Under Control of T2

In mode 1, the shifting rate is controlled by the low order 8 bits of T2 (Figure 22). Shift pulses are generated on the CB1 pin to control shifting in external devices. The time between transitions of this output clock is a function of the system clock period and the contents of the low order T2 latch (N).

The shifting operation is triggered by the read or write of the SR if the SR flag is set in the IFR. Otherwise the first shift will occur at the next time-out of T2 after a read or write of the SR. Data is shifted first into the low order bit of SR and is then shifted into the next higher order bit of the shift register on the negative-going edge of each clock pulse. The input data should change before the positive-going edge of the CB1 clock pulse. This data is shifted into the shift register during the Ø2 clock cycle following the positive-going edge of the CB1 clock pulse. After 8 CB1 clock pulses, the shift register interrupt flag will set and $\overline{IRQ}$ will go low.

SR Mode 2 — Shift In Under Ø2 Control

In mode 2, the shift rate is a direct function of the system clock frequency (Figure 23). CB1 becomes an output which generates shift pulses for controlling external devices. Timer 2 operates as an independent interval timer and has no effect on SR. The shifting operation is triggered by reading or writing the Shift Register. Data is shifted, first into bit 0 and is then shifted into the next higher order bit of the shift register on the trailing edge of each ϕ2 clock pulse. After 8 clock pulses, the shift register interrupt flag will be set, and the output clock pulses on CB1 will stop.

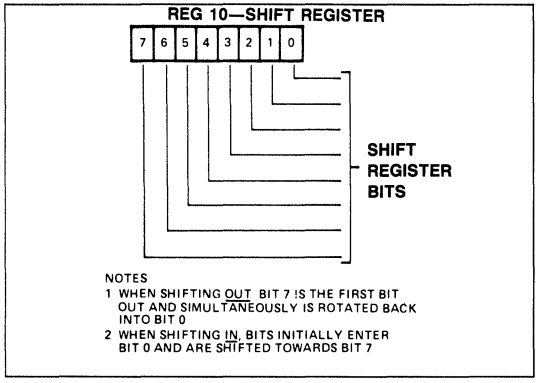
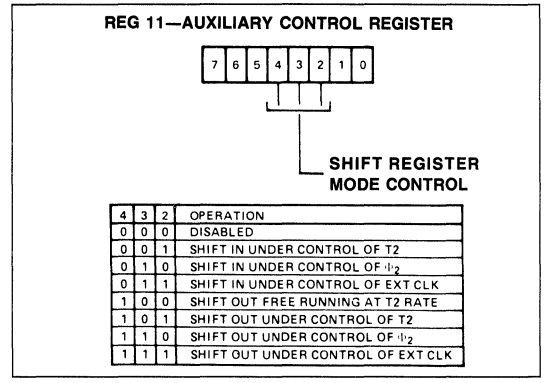


Figure 20. Shift Registers



4	3	2	OPERATION
0	0	0	DISABLED
0	0	1	SHIFT IN UNDER CONTROL OF T2
0	1	0	SHIFT IN UNDER CONTROL OF Φ_2
0	1	1	SHIFT IN UNDER CONTROL OF EXT CLK
1	0	0	SHIFT OUT FREE RUNNING AT T2 RATE
1	0	1	SHIFT OUT UNDER CONTROL OF T2
1	1	0	SHIFT OUT UNDER CONTROL OF Φ_2
1	1	1	SHIFT OUT UNDER CONTROL OF EXT CLK

Figure 21. Shift Register Modes

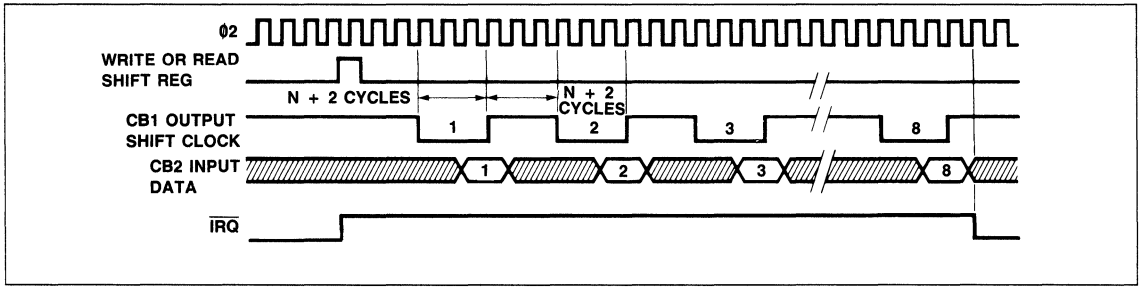


Figure 22. SR Mode 1 — Shift In Under T2 Control

SR Mode 3 — Shift In Under CB1 Control

In mode 3, external pin CB1 becomes an input (Figure 24). This allows an external device to load the shift register at its own pace. The shift register counter will interrupt the processor each time 8 bits have been shifted in. The shift register stops after 8 counts and must be reset to start again. Reading or writing the Shift Register resets the Interrrupt Flag and initializes the SR counter to count another 8 pulses.

Note that the data is shifted during the first system clock cycle following the posiive going edge of the CB1 shift pulse. For this reason, data must be held stable during the first full cycle following CB1 going high.

SR Mode 4 — Shift Out Under T2 Control (Free-Run)

Mode 4 is very similar to mode 5 in which the shifting rate is set by T2. However, in mode 4 the SR counter does not stop the shifting operation (Figure 25). Since the Shift Register bit 7 (SR7) is recirculated back into bit 0, the 8 bits loaded into the shift register will be clocked onto CB2 repetitively. In this mode the shift register counter is disabled.

SR Mode 5 — Shift Out Under T2 Control

In mode 5, the shift rate is controlled by T2 (as in mode 4). The shifting operation is triggerd by the read or write of the SR if the SR flag is set in the IFR (Figure 26). Otherwise the first shift will occur at the next time-out of T2 after a read or write of the SR. However, with each read or write of the shift register the SR Counter is reset and 8 bits are shifted onto CB2. At the same time, 8 shift pulses are generated on CB1 to control shifting in external devices. After the 8 shift pulses, the shifting is disabled, the SR Interrupt Flag is set and CB2 remains at the last data level.

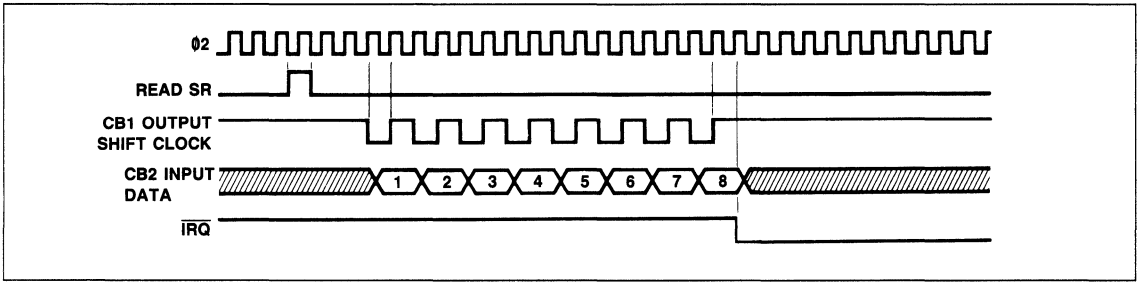


Figure 23. SR Mode 2 — Shift In Center Ø2 Control

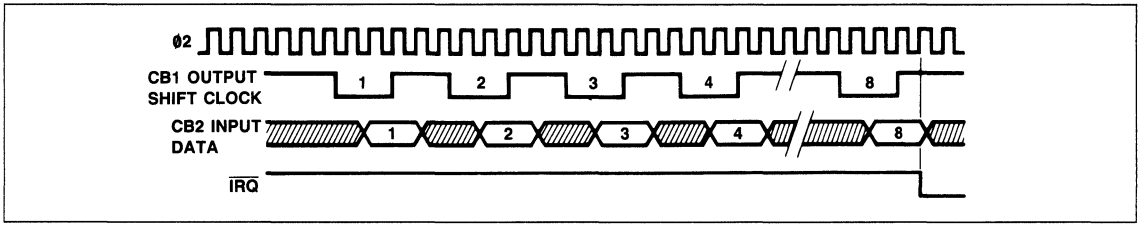


Figure 24. SR Mode 3 — Shift In Under CB1 Control

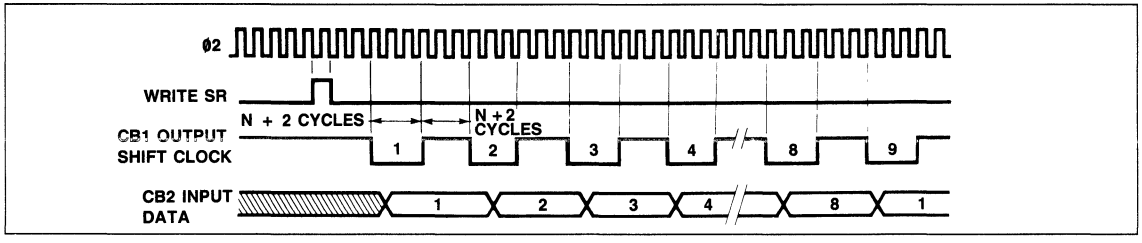


Figure 25. SR Mode 4 — Shift Our Under T2 Control (Free-Run)

SR Mode 6 — Shift OUt Under Ø2 Control

In mode 6, the shift rate is controlled by the Ø2 system clock (Figure 27).

SR Mode 7 — Shift Out Under CB1 Control

In mode 7, shifting is controlled by pulses applied to the CB1 pin by an external device (Figure 28). The SR counter sets the SR Interrupt Flag each time it counts 8 pulses but it does not disable the shifting function. Each time the microprocessor writes or reads the shift register, the SR Interrupt Flag is reset and the SR counter is initialized to begin counting the next 8 shift pulses on pin CB1. After 8 shift pulses, the Interrupt Flag is set. The microprocessor can then load the shift register with teh next byte of data.

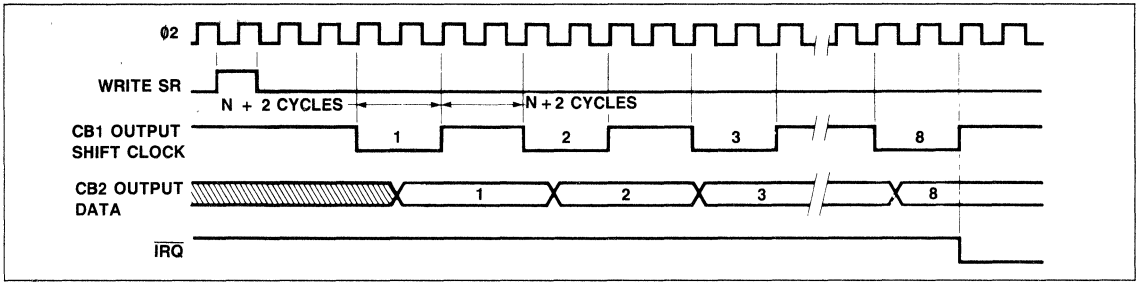


Figure 26. SR Mode 5 — Shift Out Under T2 Control

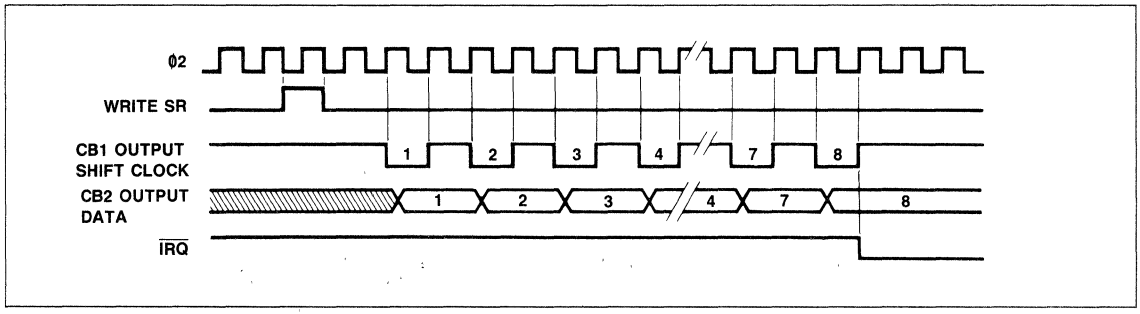


Figure 27. SR Mode 6 — Shift Out Under Ø2 Control

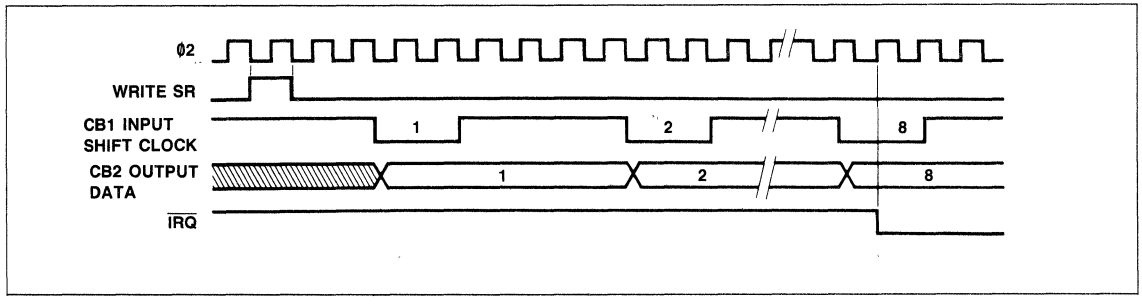


Figure 28. SR Mode 7 — Shift Out Under CB1 Control

Interrupt Operation

Controlling interrupts within the R6522 involves three principal operations. These are flagging the interrupts, enabling interrupts and signaling to the processor that an active interrupt exists within the chip. Interrupt flags are set in the Interrupt Flag Register (IFR) by conditions detected within the R6522 or on inputs to the R6522. These flags normally remain set until the interrupt has been serviced. To determine the source of an interrupt, the microprocessor must examine these flags in order, from highest to lowest priority.

Associated with each interrupt flag is an interrupt enable bit in the Interrupt Enable Register (IER). This can be set or cleared by the processor to enable interrupting the processor from the corresponding interrupt flag. If an interrupt flag is set to a logic 1 by an interrupting condition, and the corresponding interrupt enable bit is set to a 1, the Interrupt Request Output ($\overline{IRQ}$) will go low. $\overline{IRQ}$ is an "open-collector" output which can be "wire-OR'ed" with other devices in the system to interrupt the processor.

Interrupt Flag Register (IFR)

In the R6522, all the interrupt flags are contained in one register, i.e., the IFR (Figure 29). In addition, bit 7 of this register will be read as a logic 1 when an interrupt exists within the chip. This allows very convenient polling of several devices within a system to locate the source of an interrupt.

The Interrupt Flag Register (IRF) may be read directly by the processor. In addition, individual flag bits may be cleared by writing a "1" into the appropriate bit of the IFR. When the proper chip select and register signals are appplied to the chip, the contents of this register are placed on the data bus. Bit 7 indicates the status of the $\overline{IRQ}$ output. This bit corresponds to the logic function: $\overline{IRQ}$ = IFR6 × IER6 + IFR5 × IER5 + IFR4 × IER4 + IFR3 × IER3 + IFR2 × IER2 + IFR1 × IER1 + IFR0 × IER0.

Note:

× = logic AND, + = Logic OR.

The IFR bit 7 is not a flag. Therefore, this bit is not directly cleared by writing a logic 1 into it. It can only be cleared by clearing all the flags in the register or by disabling all the active interrupts as discussed in the next section.

Interrupt Enable Register (IER)

For each interrupt flag in IFR, there is a corresponding bit in the Interrupt Enable Register (IER) (Figure 30). Individual bits in the IER can be set or cleared to facilitate controlling individual interrupts without affecting others. This is accomplished by writing to the (IER) after bit 7 set or cleared to, in turn, set or clear selected enable bits. If bit 7 of the data placed on the system data bus during this write operation is a 0, each 1 in bits 6 through 0 clears the corresponding bit in the Interrupt Enable Register. For each zero in bits 6 through 0, the corresponding bit is unaffected.

Selected bits in the IER can be set by writing to the IER with bit 7 in the data word set to a 1. In this case, each 1 in bits 6 through 0 will set the corresponding bit. For each zero, the corresponding bit will be unaffected. This individual control of the setting and clearing operations allows very convenient control of the interrupts during system operation.

In addition to setting and clearing IER bits, the contents of this register can be read at any time. Bit 7 will be read as a logic 1, however.

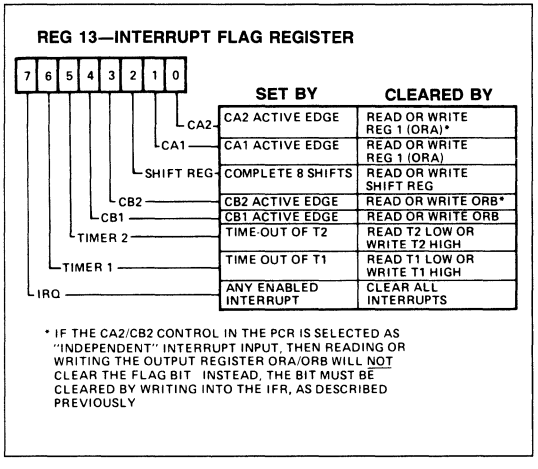


Figure 29. Interrupt Flag Register (IFR)

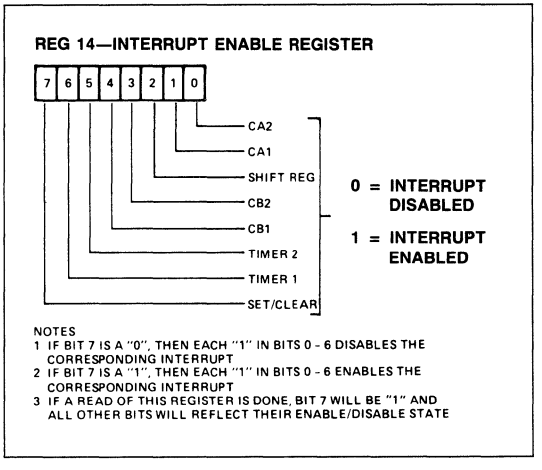


Figure 30. Interrupt Enable Register (IER)

PERIPHERAL INTERFACE CHARACTERISTICS

Symbol	Characteristic	Min.	Max.	Unit	Figure
t_r, t_f	Rise and Fall Time for CA1, CB1, CA2 and CB2 Input Signals	—	1 0	μs	—
t_{CA2}	Delay Time, Clock Negative Transition to CA2 Negative Transition (read handshake or pulse mode)	—	1.0	μs	31a, 31b
t_{RS1}	Delay Time, Clock Negative Transition to CA2 Positive Transition (pulse mode)	—	1.0	μs	31a
t_{RS2}	Delay Time, CA1 Active Transition to CA2 Positive Transition (handshake mode)	—	2.0	μs	31b
t_{WHS}	Delay Time, Clock Positive Transition to CA2 or CB2 Negative Transition (write handshake)	0.05	1.0	μs	31c, 31d
t_{DS}	Delay Time, Peripheral Data Valid to CB2 Negative Transition	0 20	1.5	μs	31c, 31d
t_{RS3}	Delay Time, Clock Positive Transition to CA2 or CB2 Positive Transition (pulse mode)	—	1.0	μs	31c
t_{RS4}	Delay Time, CA1 or CB1 Active Transition to CA2 or CB2 Positive Transition (handshake mode)	—	2.0	μs	31d
t_{21}	Delay Time Required from CA2 Output to CA1 Active Transition (handshake mode)	400	—	ns	31d
t_{IL}	Setup Time, Peripheral Data Valid to CA1 or CB1 Active Transition (input latching)	300	—	ns	31e
t_{AL}	CA1, CB1 Setup Prior to Transition to Arm Latch	300	—	ns	31e
t_{PDH}	Peripheral Data Hold After CA1, CB1 Transition	150	—	ns	31e
t_{SR1}	Shift-Out Delay Time — Time from ϕ_2 Falling Edge to CB2 Data Out	—	300	ns	31f
t_{SR2}	Shift-In Setup Time — Time from CB2 Data In to ϕ_2 Rising Edge	300	—	ns	31g
t_{SR3}	External Shift Clock (CB1) Setup Time Relative to ϕ_2 Trailing Edge	100	T_{CY}	ns	31g
t_{IPW}	Pulse Width — PB6 Input Pulse	2 × T_{CY}	—		31i
t_{ICW}	Pulse Width — CB1 Input Clock	2 × T_{CY}	—		31h
t_{IPS}	Pulse Spacing — PB6 Input Pulse	2 × T_{CY}	—		31ı
t_{ICS}	Pulse Spacing — CB1 Input Pulse	2 × T_{CY}	—		31h

PERIPHERAL INTERFACE WAVEFORMS

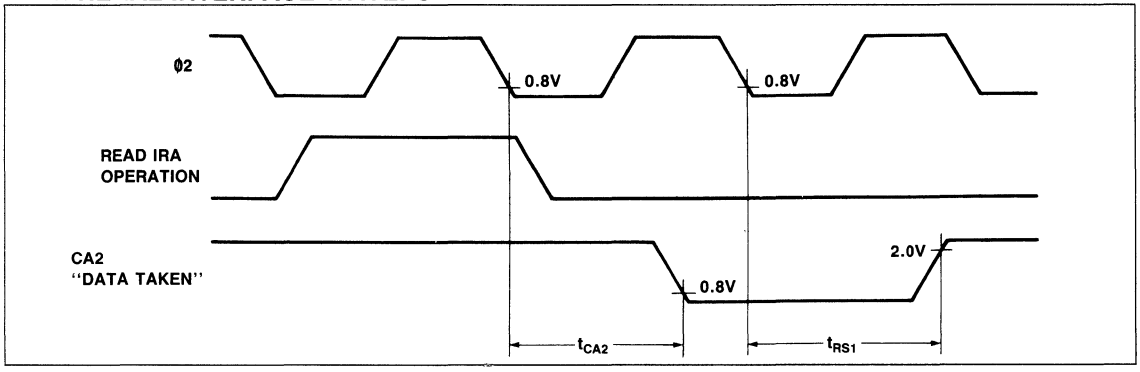


Figure 31a. CA2 Timing for Read Handshake, Pulse Mode

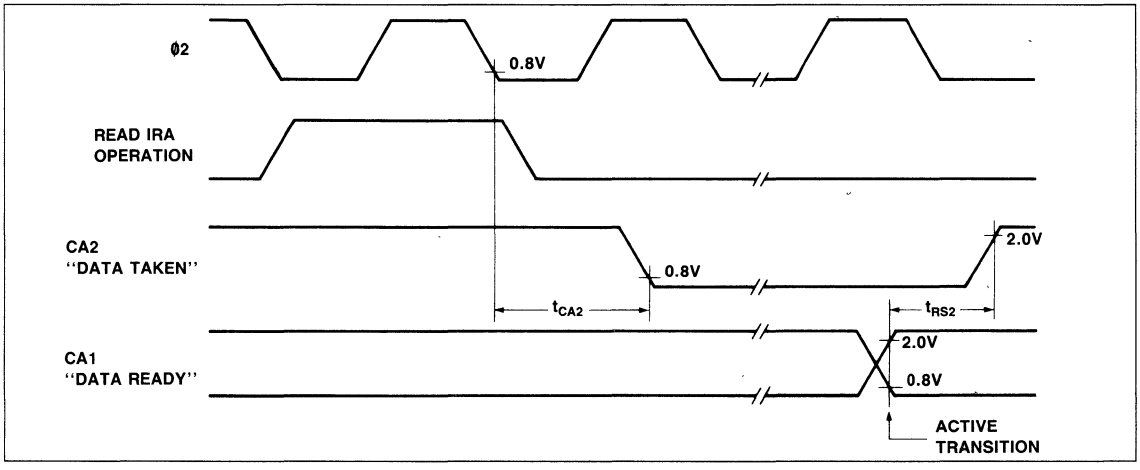


Figure 31b. CA2 Timing for Read Handshake, Handshake Mode

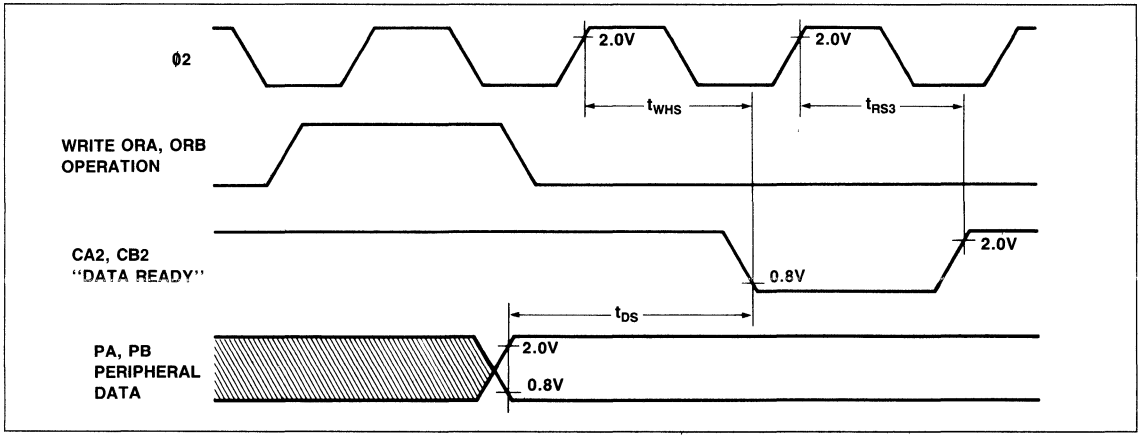


Figure 31c. CA2, CB2 Timing for Write Handshake, Pulse Mode

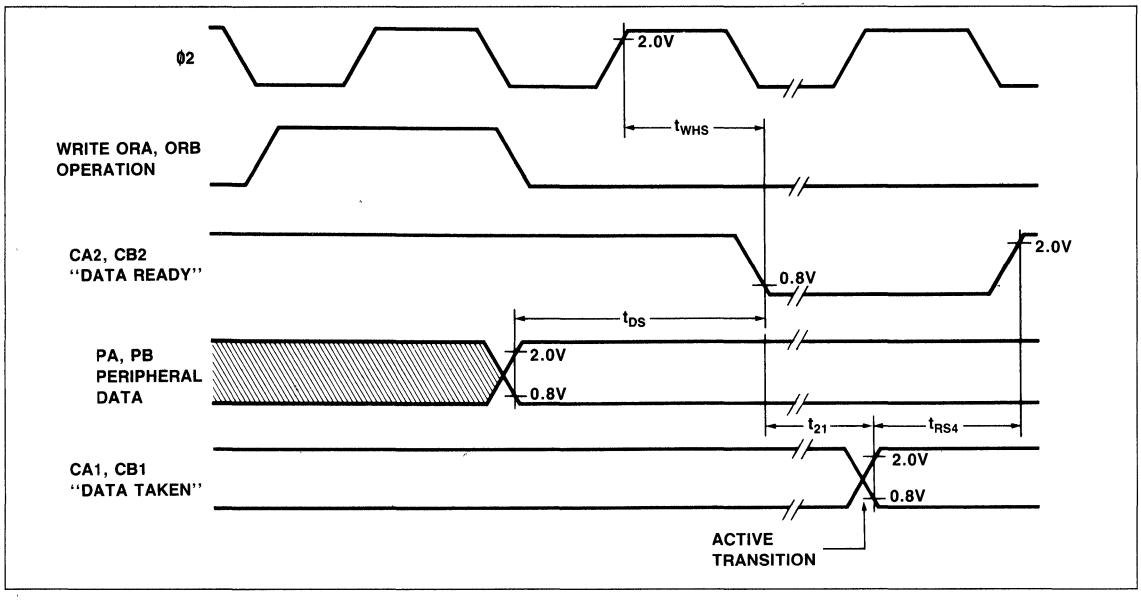


Figure 31d. CA2, CB2 Timing for Write Handshake, Handshake Mode

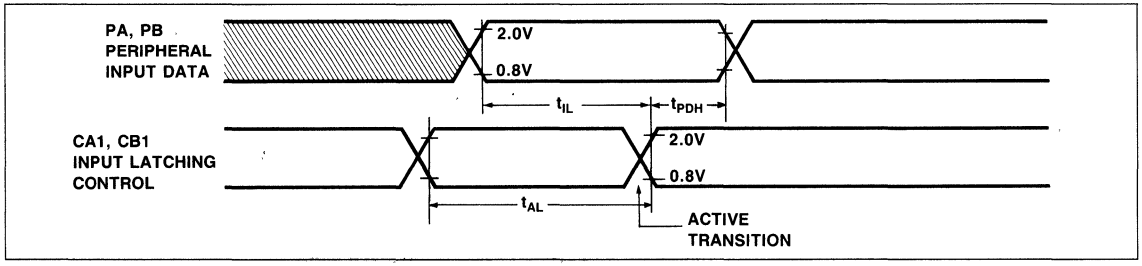


Figure 31e. Peripheral Data Input Latching Timing

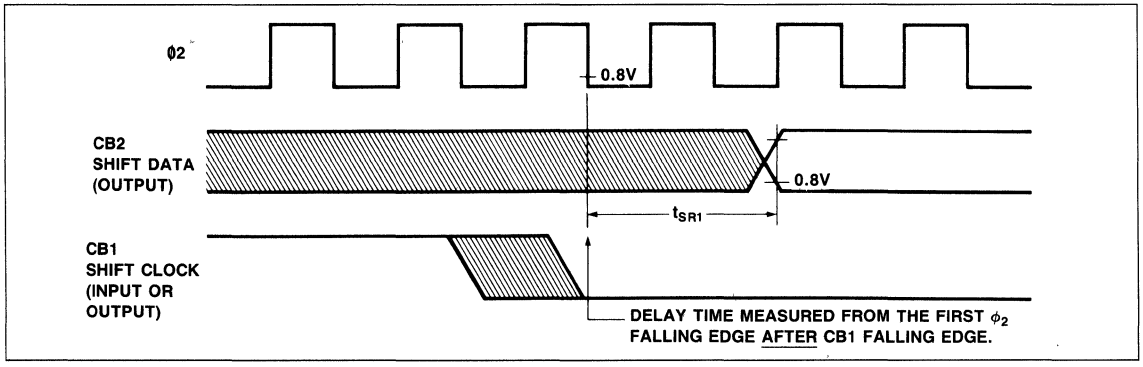


Figure 31f. Timing for Shift Out with Internal or External Shift Clocking

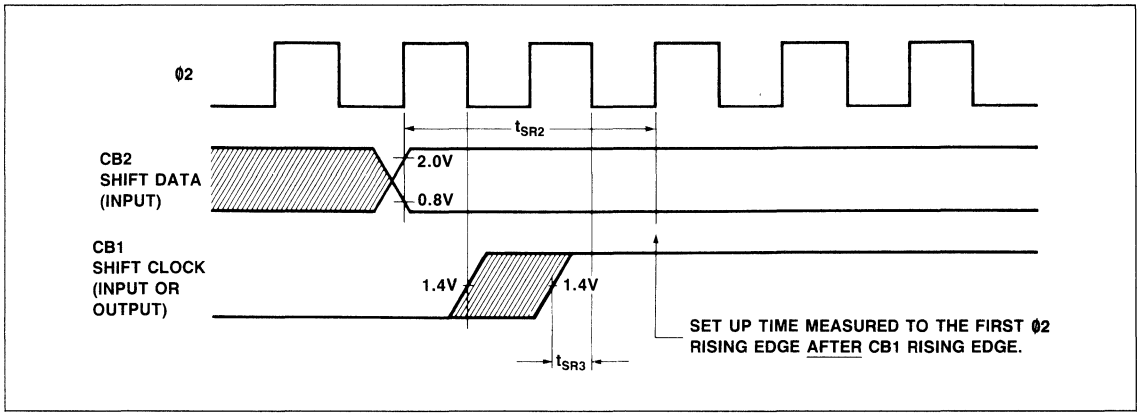


Figure 31g. Timing for Shift in with Internal or External Shift Clocking

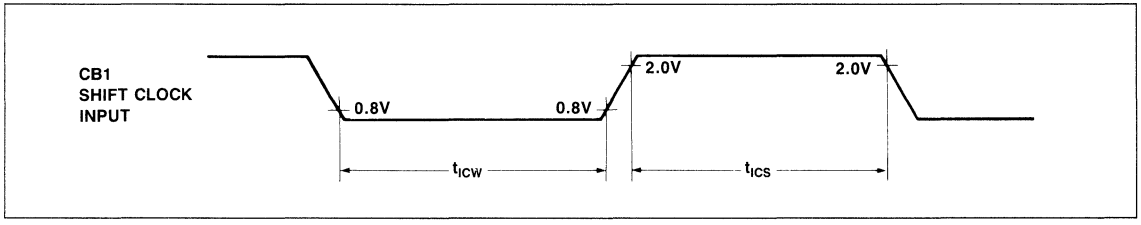


Figure 31h. External Shift Clock Timing

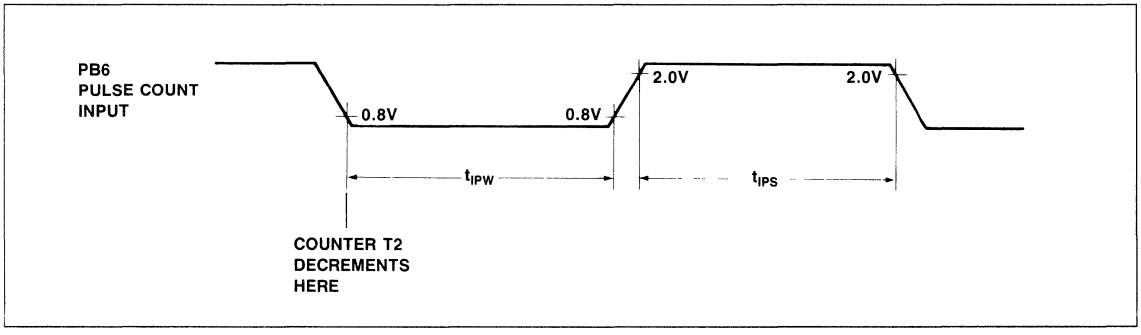
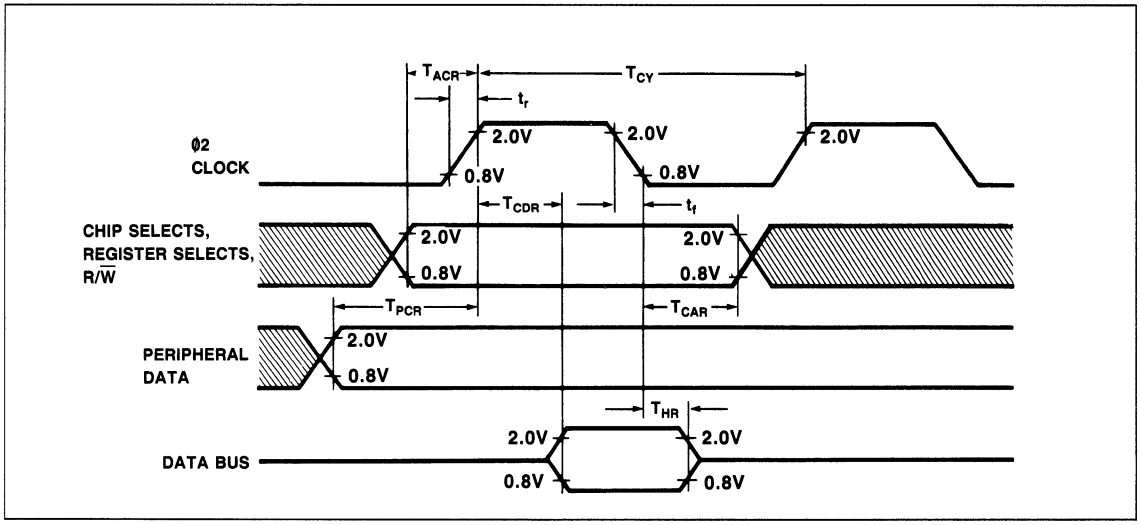


Figure 31i. Pulse Count Input Timing

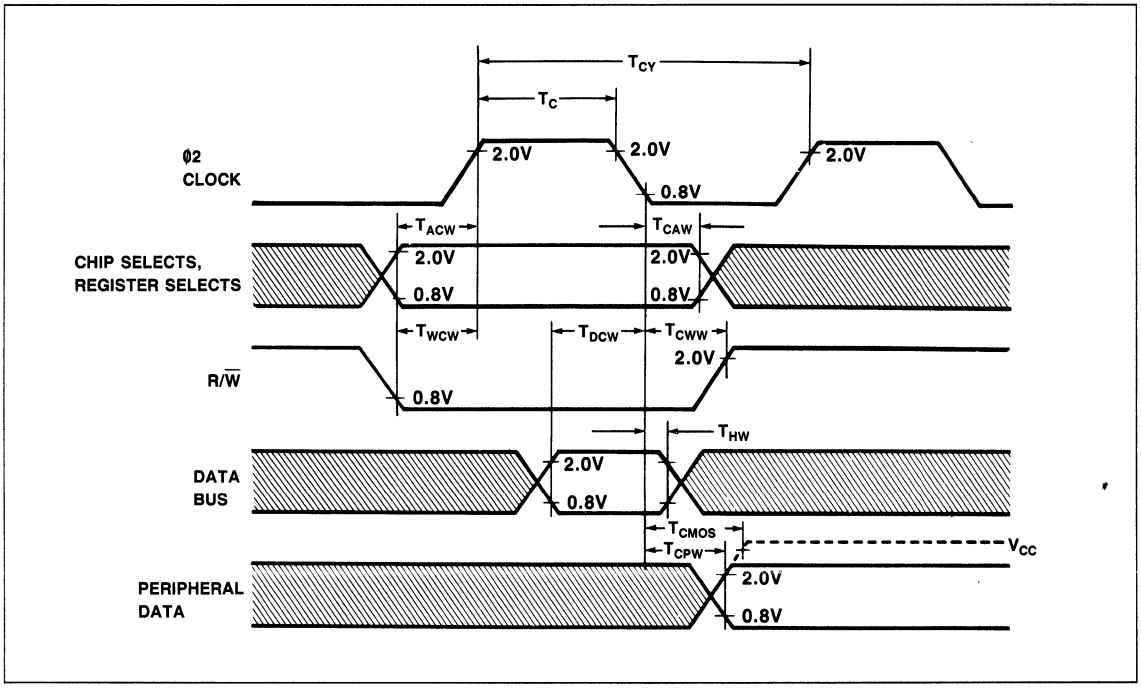
BUS TIMING CHARACTERISTICS

Parameter	Symbol	R6522 (1 MHz)		R6522A (2 MHz)		Unit
		Min.	Max.	Min.	Max.	
READ TIMING						
Cycle Time	T_{CY}	1	10	0.5	10	μs
Address Set-Up Time	T_{ACR}	180	—	90	—	ns
Address Hold Time	T_{CAR}	0	—	0	—	ns
Peripheral Data Set-Up Time	T_{PCR}	300	—	150	—	ns
Data Bus Delay Time	T_{CDR}	—	365	—	190	ns
Data Bus Hold Time	T_{HR}	10	—	10	—	ns
WRITE TIMING						
Cycle Time	T_{CY}	1	10	0.50	10	μs
Ø2 Pulse Width	T_C	470	—	235	—	ns
Address Set-Up Time	T_{ACW}	180	—	90	—	ns
Address Hold Time	T_{CAW}	0	—	0	—	ns
R/$\overline{W}$ Set-Up Time	T_{WCW}	180	—	90	—	ns
R/$\overline{W}$ Hold Time	T_{CWW}	0	—	0	—	ns
Data Bus Set-Up Time	T_{DCW}	200	—	90	—	ns
Data Bus Hold Time	T_{HW}	10	—	10	—	ns
Peripheral Data Delay Time	T_{CPW}	—	1.0	—	0.5	μs
Peripheral Data Delay Time to CMOS Levels	T_{CMOS}	—	2.0	—	1.0	μs
Note: t_R and t_F = 10 to 30 ns.						

BUS TIMING WAVEFORMS



Read Timing Waveforms



Write Timing Waveforms

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to +7.0	Vdc
Input Voltage	V_{IN}	−0.3 to +7.0	Vdc
Operating Temperature Commercial Industrial	T_A	 0 to +70 −40 to +85	 °C °C
Storage Temperature	T_{STG}	−55 to +150	°C

***NOTE:** Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the other sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING CONDITIONS

Parameter	Symbol	Value
Supply Voltage	V_{CC}	5V ±5%
Temperature Range Commercial	T_A	 0°C to 70°C

DC CHARACTERISTICS

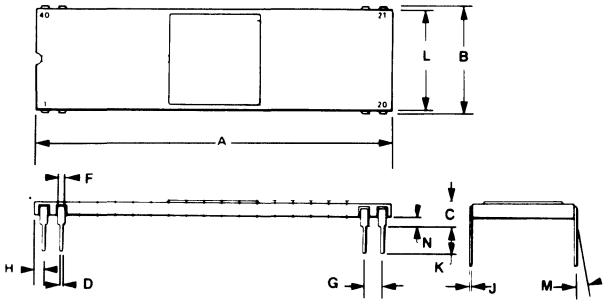
(V_{CC} = 5.0 Vdc ±5%, V_{SS} = 0, T_A = T_L to T_H, unless otherwise noted)

Parameter	Symbol	Min.	Typ.[3]	Max.	Unit	Test Conditions
Input High Voltage	V_{IH}	2.4	—	V_{CC}	V	
Input Low Voltage	V_{IL}	−0.3	—	0.4	V	
Input Leakage Current R/$\overline{W}$, $\overline{RES}$, RS0, RS1, RS2, RS3, CS1, $\overline{CS2}$, CA1, Ø2	I_{IN}	—	±1	±2.5	μA	V_{IN} = 0V to 5.25V V_{CC} = 0V
Input Leakage Current for Three-State Off D0-D07	I_{TSI}	—	±2	±10	μA	V_{IN} = 0.4V to 2.4V V_{CC} = 5.25V
Input High Current PA0-PA7, CA2, PB0-PB7, CB1, CBS	I_{IH}	−100	−200	—	μA	V_{IN} = 2.4V V_{CC} = 5.25V
Input Low Current PA0-PA7, CA2, PB0-PB7, CB1, CB2	I_{IL}	—	−0.9	−1.8	mA	V_{IL} = 0.4V V_{CC} = 5.25V
Output High Voltage All outputs PB0-PB7, CB2 (Darlington Drive)	V_{OH}	 2.4 1.5	 — —	 — —	 V V	V_{CC} = 4.75V I_{LOAD} = −100 μA I_{LOAD} = −1.0 mA
Output Low Voltage	V_{OL}	—	—	0.4	V	V_{CC} = 4.75V I_{LOAD} = 1.6 mA
Output High Current (Sourcing) Logic PB0-PB7, CB2 (Darlington Drive)	I_{OH}	 −100 −1.0	 −1000 −2.5	 — −10	 μA mA	 V_{OH} = 2.4V V_{OH} = 1.5V
Output Low Current (Sinking)	I_{OL}	1.6	—	—	mA	V_{OL} = 0.4V
Output Leakage Current (Off State) $\overline{IRQ}$	I_{OFF}	—	4	±10	μA	V_{OH} = 2.4V V_{CC} = 5.25V
Power Dissipation	P_D	—	450	700	mW	
Input Capacitance R/$\overline{W}$, $\overline{RES}$, RS0, RS1, RS2, RS3, CS1, $\overline{CS2}$, D0-D7, PA0-PA7, CA1, CA2, PB0-PB7 CB1, CB2 Ø2 Input	C_{IN}	 — — —	 — — —	 7 10 20	 pF pF pF	V_{CC} = 5.0V V_{IN} = 0V f = 1 MHz T_A = 25°C
Output Capacitance	C_{OUT}	—	—	10	pF	

Notes:
1. All units are direct current (DC) except for capacitance.
2. Negative sign indicates outward current flow, positive indicates inward flow.
3. Typical values shown for V_{CC} = 5.0V and T_A = 25°C.

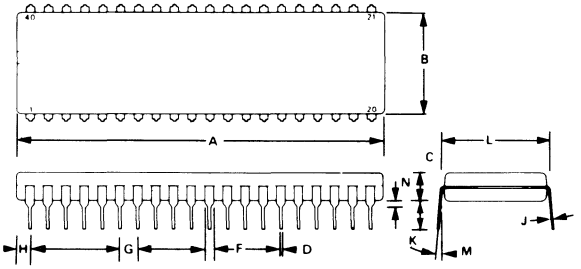
PACKAGE DIMENSIONS

40-PIN CERAMIC DIP



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	50 29	51 31	1 980	2 020
B	14 86	15 62	0 585	0 615
C	2 54	4 19	0 100	0 165
D	0 38	0 53	0 015	0 021
F	0 76	1 40	0 030	0 055
G	2 54 BSC		0 100 BSC	
H	0 76	1 78	0 030	0 070
J	0 20	0 33	0 008	0 013
K	2 54	4 19	0 100	0 165
L	14 60	15 37	0 575	0 605
M	0°	10°	0°	10°
N	0 51	1 52	0 020	0 060

40-PIN PLASTIC DIP



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	51 28	52 32	2 040	2 060
B	13 72	14 22	0 540	0 560
C	3 55	5 08	0 140	0 200
D	0 36	0 51	0 014	0 020
F	1 02	1 52	0 040	0 060
G	2 54 BSC		0 100 BSC	
H	1 65	2 16	0 065	0 085
J	0 20	0 30	0 008	0 012
K	3 05	3 56	0 120	0 140
L	15 24 BSC		0 600 BSC	
M	7°	10°	7°	10°
N	0 51	1 02	0 020	0 040

Rockwell

R6530
ROM-RAM-I/O-TIMER (RRIOT)

DESCRIPTION

The R6530 ROM-RAM-I/O-Timer (RRIOT) combines read only memory, random access memory, parallel I/O data ports, and timer functions into a single peripheral device which operates in conjunction with any CPU in the R6500 microprocessor family. The R6530 allows two chip solutions in a variety of production applications. It is comprised of a mask programmable 1024 × 8 ROM, a 64 × 8 static RAM, two software controlled 8-bit bidirectional data ports allowing direct interfacing between the microprocessor unit and peripheral devices, and a software programmable interval timer with interrupt, capable of timing in various intervals from 1 to 262,144 clock periods.

FEATURES

- 1024 × 8 mask programmable ROM
- 64 × 8 static RAM
- Two 8-bit bidirectional data ports for interface to peripherals
- Two programmable data direction registers
- Programmable interval timer
- Programmable interval timer interrupt
- TTL & CMOS compatible peripheral lines
- Peripheral pins with direct transistor drive capability
- 8-bit directional data bus for direct communication with the microprocessor
- High impedance three-state data bus
- Allows up to 7K contiguous bytes of ROM with no external decoding

ORDERING INFORMATION

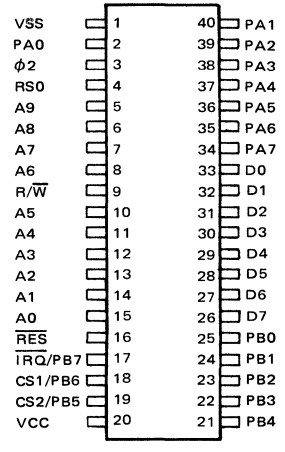
Part Number: R6530_

Package:
- C = Ceramic DIP
- P = Plastic DIP

Temperature Range:
- 0°C to 70°C

Frequency:
- 1 MHz

Note: A custom part number will be assigned by Rockwell. ROM codes should be submitted using ROM Code Order Form, Order No. 2137.



R6530 Pin Configuration

INTERFACE SIGNALS

RESET ($\overline{RES}$)

During system initialization, a $\overline{RES}$ input causes zeroing of all four I/O registers. This in turn causes all I/O buses to act as inputs thus protecting external components from possible damage and erroneous data while the system is being configured under software control. The Data Bus Buffers are put into an off state during Reset. Interrupt capability is disabled with the $\overline{RES}$ signal. The $\overline{RES}$ signal must be held low for at least one clock period when reset is required.

READ/WRITE (R/$\overline{W}$)

The R/$\overline{W}$ input is supplied by the microprocessor and controls the transfer of data between the R6530 and the microprocessor via the data bus. A high on the R/$\overline{W}$ pin reads (with proper addressing) data from the R6530 onto the data bus. A low on the R/$\overline{W}$ pin writes (with proper addressing) data from the data bus into R6530.

PHASE 2 CLOCK (Ø2)

The Phase 2 clock (Ø2) input is the system clock generated by the CPU that triggers all data transfers between the data bus and the R6530.

INTERRUPT REQUEST ($\overline{IRQ}$)

The $\overline{IRQ}$ pin is an interrupt pin from the interval timer. This same pin, if not used as an interrupt, can be used as a peripheral I/O pin (PB7). When used as an interrupt, the pin should be set up as an input by the Data Direction Register. The pin will be normally high with a low indicating an interrupt from the R6530. An external pull-up device is not required; however, if collector-OR'd with other devices, the internal pullup may be omitted with a mask option.

DATA BUS (D0–D7)

The R6530 has eight bidirectional data pins (D0–D7). These pins connect to the system's data lines and allow transfer of data to and from the microprocessor The output buffers remain in the off state except when selected for a Read operation.

ADDRESS LINES (A0–A9)

There are 10 address pins (A0–A9). In addition, there is the ROM Select pin (RS0). Further, pins PB5 and PB6 are mask programmable, and can be used either individually or together as chip selects. When used as peripheral data pins they cannot be used as chip selects.

ROM SELECT (RS0)

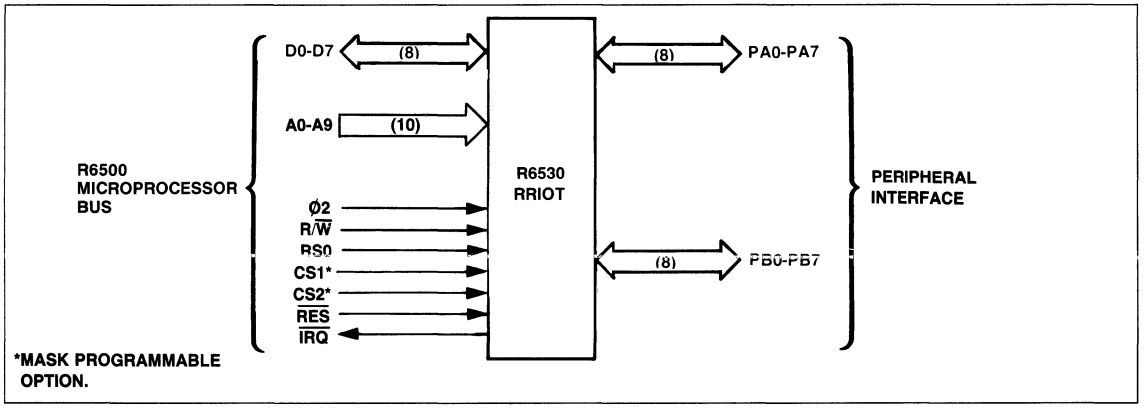
RS0 serves as an additional address input line. When RS0 is high, internal ROM is selected; when RS0 is low, internal ROM is not selected.

PERIPHERAL DATA PORTS

The R6530 has 16 pins available for peripheral I/O operations. Each pin is individually software programmable to act as either an input or an output. The 16 pins are divided into two 8-bit ports, PA0–PA7 and PB0–PB7. PB5, PB6 and PB7 also have other uses which are discussed in later sections. The pins are set up as an input by writing a "0" into the corresponding bit of the Data Direction Register. A "1" into the Data Direction Register causes its corresponding bit to be an output. When in the input mode, the Peripheral Data Buffers are in the "1" state and the internal pull-up device acts as less than one TTL load to the peripheral data lines. On a Read operation, the microprocessor unit reads the peripheral pin. When the peripheral device gets information from the R6530 it receives data stored in the Output Register. The microprocessor will read correct information if the peripheral lines are greater than 2.0 volts (for a "1") or less than 0.8 volts (for a "0") as the peripheral pins are all TTL compatible.

CHIP SELECT (CS0, CS1)

Pins 18 and 19 are individually selectable at mask time as either chip selects CS1 and CS2, respectively, or port B functions PB6 and PB5, respectively.



Interface Signals

INTERNAL ORGANIZATION

The R6530 is divided into four basic sections: RAM, ROM, I/O and Timer. The RAM and ROM interface directly with the microprocessor through the system data bus and address lines. The I/O section consists of two 8-bit halves. Each half contains a Data Direction Register (DDR) and an Output Register.

ROM—1K BYTE (8K BITS)

The 1K byte ROM is in a 1024 × 8 configuration. Address lines A0–A9, as well as RS0 are needed to address the entire ROM. With the addition of CS1 and CS2, seven R6530's may be addressed, giving 7168 × 8 bits of contiguous ROM.

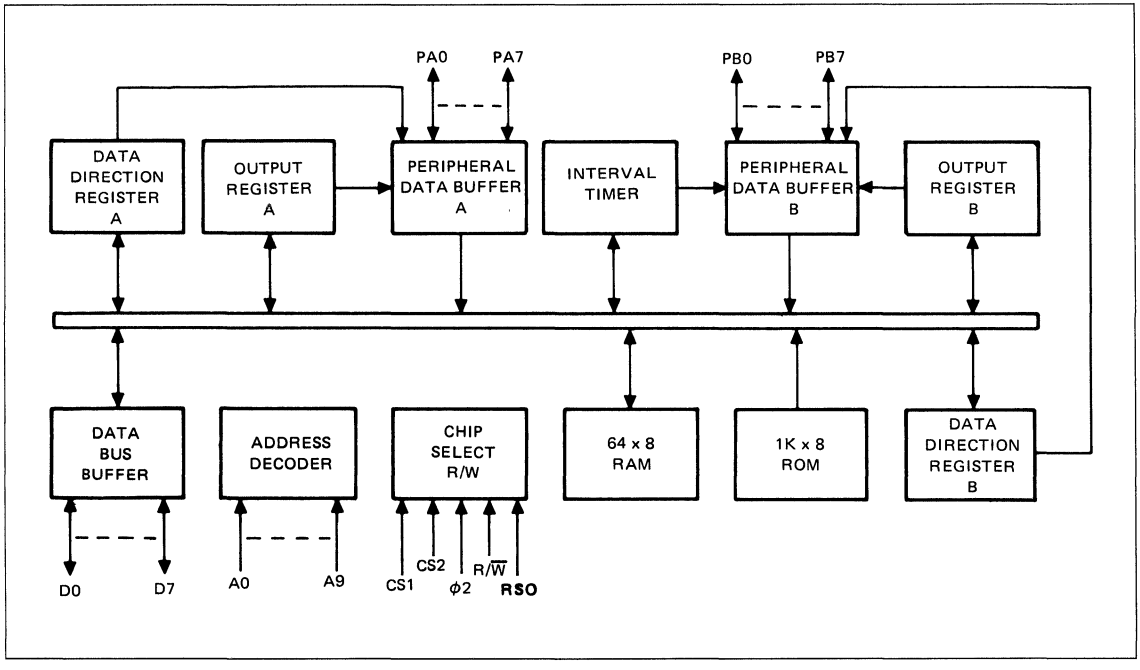
RAM—64 BYTES (512 BITS)

A 64 × 8 static RAM is contained on the R6530. It is addressed by A0–A5 (Byte Select), RS0, A6, A7, A8, A9 and, depending on the number of chips in the system, CS1 and CS2.

INTERNAL PERIPHERAL REGISTERS

There are four internal registers, two data direction registers and two output registers. The two data direction registers (A side and B side) control the direction of the data into and out of the peripheral pins. A "1" written into the Data Direction Register sets up the corresponding peripheral buffer pin as an output. Therefore, anything then written into the Output Register will appear on that corresponding peripheral pin. A "0" written into the DDR inhibits the output buffer from transmitting data from the Output Register. For example, a "1" loaded into Data Direction Register A, position 3, sets up peripheral pin PA3 as an output. If a "0" had been loaded, PA3 would be configured as an input and remain in the high state. The two Data Output Registers are used to latch data from the Data Bus during a Write operation until the peripheral device can read the data supplied by the microprocessor.

During a Read operation the microprocessor is reading the peripheral data pins. For the peripheral data pins which are programmed as outputs the microprocessor will read the corresponding data bits of the Output Register. The only way the Output Register data can be changed is by a microprocessor Write operation. The Output Register is not affected by a Read of the data on the peripheral pins.



R6530 Block Diagram

INTERVAL TIMER

The Timer section of the R6530 contains three basic parts: prescale divide down register, programmable 8-bit register and interrupt logic.

The interval timer can be programmed to count up to 256 time intervals. Each time interval can be either 1T, 8T, 64T or 1024T increments, where T is the system clock period. When a full count is reached, an interrupt flag is set to a logic "1". After the interrupt flag is set the internal clock begins counting down to a maximum of −225T. Thus, after the interrupt flag is set, a Read of the timer will tell how long since the flag was set up to a maximum of 255T.

The 8 bit system Data Bus is used to transfer data to and from the Interval Timer. If a count of 52 time intervals were to be counted, the pattern 0 0 1 1 0 1 0 0 would be put on the Data Bus and written into the Interval Timer Register.

At the same time that data is being written to the Interval Timer, the counting interval (1, 8, 64, or 1024T) is decoded from address lines A0 and A1. During a Read or Write operation address line A3 controls the interrupt capability of PB7, i.e., A3 = 1 enables $\overline{IRQ}$ on PB7, A3 = 0 disables $\overline{IRQ}$ on PB7. When PB7 is to be used as an interrupt flag with the interval timer it should be programmed as an input. If PB7 is enabled by A3 and an interrupt occurs PB7 will go low. When the timer is read prior to the interrupt flag being set, the number of time intervals remaining will be read, i.e., 51, 50, 49, etc.

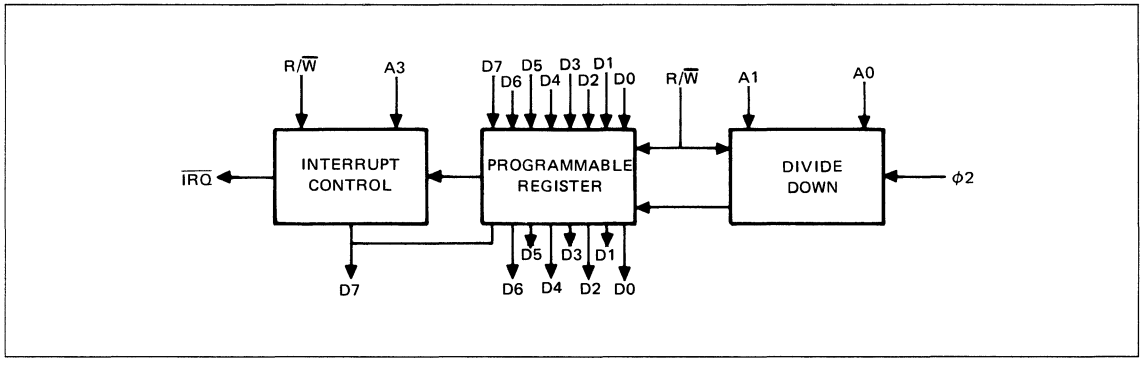
When the timer has counted down to 0 0 0 0 0 0 0 0 on the next count time an interrupt will occur and the counter will read 1 1 1 1 1 1 1 1. After interrupt, the Timer Register decrements at a divide by "1" rate of the system clock. If after interrupt, the timer is read and a value of 1 1 1 0 0 1 0 0 is read, the time since interrupt is 27T. The value read is in one's complement.

Value read = 1 1 1 0 0 1 0 0
Complement = 0 0 0 1 1 0 1 1 = 27

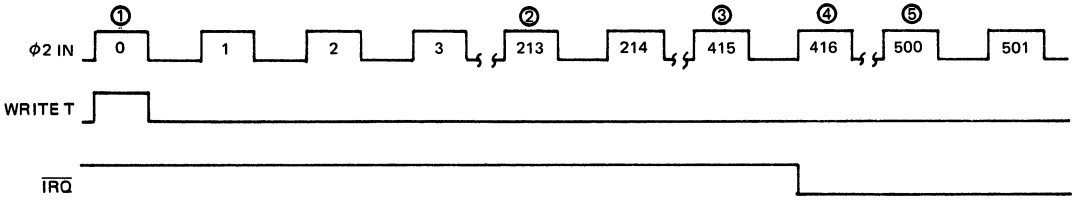
Thus, to arrive at the total elapsed time, merely do a one's complement and add to the original time written into the timer. Again, assume time written as 0 0 1 1 0 1 0 0 (=52). With a divide by 8, total time to interrupt is (52 × 8) + 1 = 417T. Total elapsed time would be 417T + 27T = 444T, assuming the value read after interrupt was 1 1 1 0 0 1 0 0.

After the interrupt, whenever the timer is written or read the interrupt is reset. However, the reading of the timer at the same time the interrupt occurs will not reset the interrupt flag. When the interrupt flag is read on D7 all other D outputs (D0 through D6) go to "0".

When reading the timer after an interrupt, A3 should be low so as to disable the $\overline{IRQ}$ pin. This is done so as to avoid future interrupts until after another Write timer operation.



Basic Elements of Interval Timer



① Data written into interval timer is: 0 0 1 1 0 1 0 0 = 52_{10}

② Data in Interval timer is: 0 0 0 1 1 0 0 1 = 25_{10}

$$52 - \frac{213}{8} - 1 = 52 - 26 - 1 = 25$$

③ Data in Interval timer is: 0 0 0 0 0 0 0 0 = 0_{10}

$$52 - \frac{415}{8} - 1 = 52 - 51 - 1 = 0$$

④ Interrupt has occurred at Ø2 pulse #416
Data in Interval timer is: 1 1 1 1 1 1 1 1

⑤ Data in Interval timer is: 1 0 1 0 1 1 0 0
two's complement is: 0 1 0 1 0 0 1 1 = 83_{10}
$83 + (52 \times 8) + 1 = 500_{10}$

R6530 Timer Example

ADDRESSING

Addressing of the R6530 offers many variations to the user for greater flexibility. The user may configure his system with RAM in lower memory, ROM in higher memory, and I/O registers with interval timers between the extremes. There are 10 address lines (A0–A9). In addition, there is the possibility of 3 additional address lines to be used as chip-selects and to distinguish between ROM, RAM, I/O and interval timer. Two of the additional lines are chip-selects 1 and 2 (CS1 and CS2). The chip-select pins can also be PB5 and PB6. Whether the pins are used as chip-selects or peripheral I/O pins is a mask option and must be specified when ordering the part. Both pins act independently of each other in that either or both pins may be designated as a chip-select. The third additional address line is RS0. The R6502 and R6530 in a 2-chip system would use RS0 to distinguish between ROM and non-ROM sections of the R6530. With the addressing pins available, a total of 7K contiguous ROM may be addressed with no external decode. Following is an example of a 1-chip and a 7-chip R6530 Addressing Scheme.

ONE-CHIP ADDRESSING

A 1-chip system decode is illustrated in the R6530 One-Chip Address Encoding Diagram.

SEVEN-CHIP ADDRESSING

In the seven-chip system, the objective would be to have 7K bytes of contiguous ROM, with RAM in low order memory. The 7K of ROM could be placed between addresses 65,535 and 1024. For this case, assume A13, A14 and A15 are all 1 when addressing ROM, and 0 when addressing RAM or I/O. This would place the 7K ROM between addresses 65,535 and 58,367. The two pins designated as chip-select, or I/O, would be masked programmed as chip-select pins. Pin RS0 would be connected to address line A10. Pins CS1 and CS2 would be connected to address lines A11 and A12 respectively. See table 1.

The two examples shown would allow addressing of the ROM and RAM; however, once the I/O or timer has been addressed, further decoding is necessary to select which of the I/O registers are desired, as well as the coding of the interval timer.

I/O REGISTER—TIMER ADDRESSING

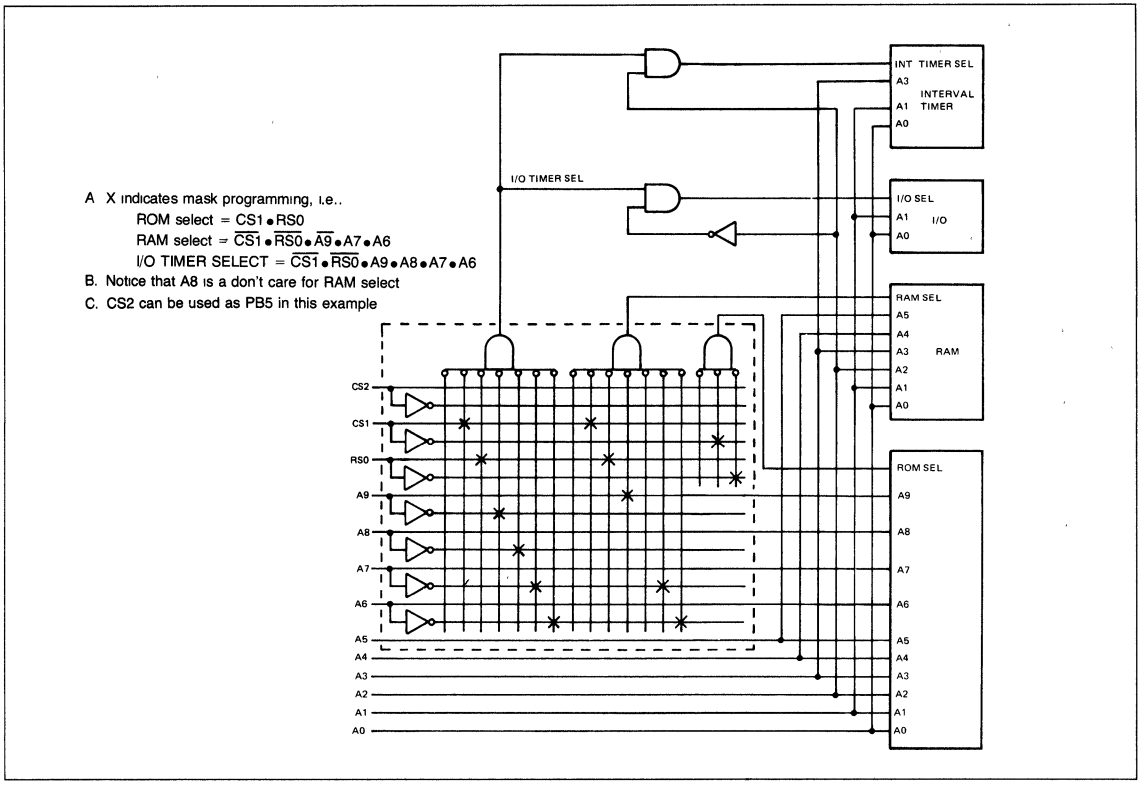
Table 2, Addressing Decode for I/O Register and Timer, illustrates the address decoding for the internal elements and timer programming. Address lines A2 distinguishes I/O registers from the timer. When A2 is high and I/O timer select is high, the I/O registers are addressed. Once the I/O registers are addressed, address lines A1 and A0 decode the desired register.

When the timer is selected A1 and A0 decode the divide by matrix. In addition, Address A3 is used to enable the interrupt flag to PB7.

Table 1. R6530 Seven-Chip Addressing Scheme

		Address, Chip Select and Register Select Lines						
Device	Function	CS2 A12	CS1 All	RS0 A10	A9	A8	A7	A6
R6530 #1	ROM Select	0	0	1	X	X	X	X
	RAM Select	0	0	0	0	0	0	0
	I/O Timer	0	0	0	1	0	0	0
R6530 #2	ROM Select	0	1	0	X	X	X	X
	RAM Select	0	0	0	0	0	0	1
	I/O Timer	0	0	0	1	0	0	1
R6530 #3	ROM Select	0	1	1	X	X	X	X
	RAM Select	0	0	0	0	0	1	0
	I/O Timer	0	0	0	1	0	1	0
R6530 #4	ROM Select	1	0	0	X	X	X	X
	RAM Select	0	0	0	0	0	1	1
	I/O Timer	0	0	0	1	0	1	1
R6530 #5*	ROM Select	1	0	1	X	X	X	X
	RAM Select	0	0	0	0	1	0	0
	I/O Timer	0	0	0	1	1	0	0
R6530 #6	ROM Select	1	1	0	X	X	X	X
	RAM Select	0	0	0	0	1	0	1
	I/O Timer	0	0	0	1	1	0	1
R6530 #7	ROM Select	1	1	1	X	X	X	X
	RAM Select	0	0	0	0	1	1	0
	I/O Timer	0	0	0	1	1	1	0

Note: * RAM select for R6530 #5 would read = $\overline{A12} \bullet \overline{A11} \bullet \overline{A10} \bullet \overline{A9} \bullet A8 \bullet \overline{A7} \bullet \overline{A6}$



R6530 One-Chip Address Encoding Diagram

Table 2. Addressing Decode for I/O Register and Timer

Function	Addressing Decode							
	ROM Select	RAM Select	I/O Timer Select	R/$\overline{W}$	A3	A2	A1	A0
Read ROM	1	0	0	1	X	X	X	X
Write RAM	0	1	0	0	X	X	X	X
Read RAM	0	1	0	1	X	X	X	X
Write DDRA	0	0	1	0	X	0	0	1
Read DDRA	0	0	1	1	X	0	0	1
Write DDRB	0	0	1	0	X	0	1	1
Read DDRB	0	0	1	1	X	0	1	1
Write Per Reg. A	0	0	1	0	X	0	0	0
Read Per. Reg. A	0	0	1	1	X	0	0	0
Write Per. Reg. B	0	0	1	0	X	0	1	0
Read Per. Reg. B	0	0	1	1	X	0	1	0
Write Timer								
−1T	0	0	1	0	*	1	0	0
−8T	0	0	1	0	*	1	0	1
−64T	0	0	1	0	*	1	1	0
−1024T	0	0	1	0	*	1	1	1
Read Timer	0	0	1	1	*	1	X	0
Read Interrupt Flag	0	0	1	1	X	1	X	1

Notes: *A3 = 1 Enables $\overline{IRQ}$ to PB7
A3 = 0 Disables $\overline{IRQ}$ to PB7

TIMING CHARACTERISTICS

Read Timing

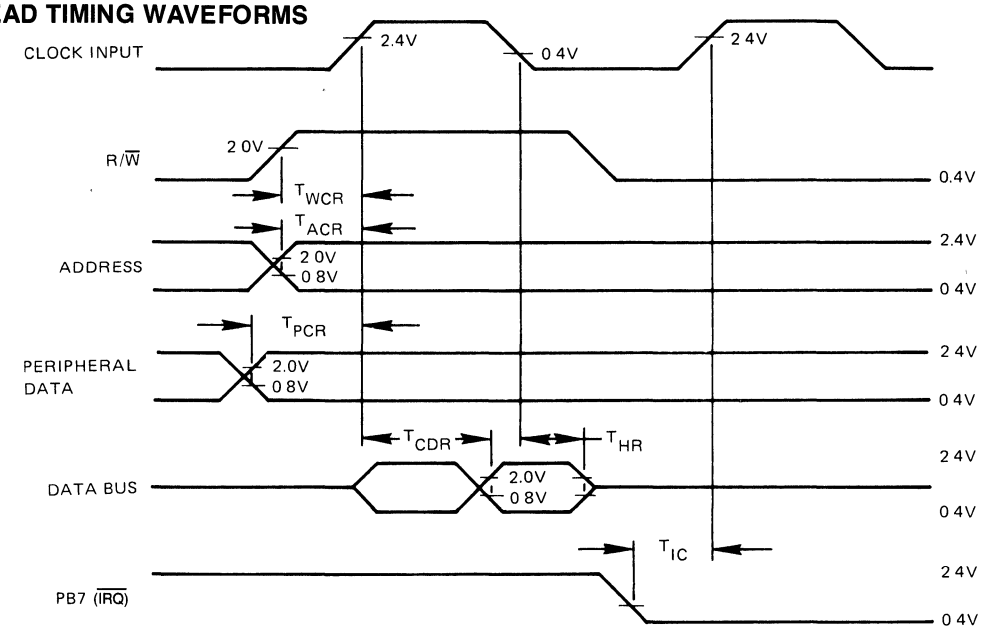
Characteristic	Symbol	Min	Max	Unit
R/$\overline{W}$ valid before positive transition of clock	T_{WCR}	180	—	ns
Address valid before positive transition of clock	T_{ACR}	180	—	ns
Peripheral data valid before positive transition of clock	T_{PCR}	300	—	ns
Data Bus valid after positive transition of clock	T_{CDR}	—	395	ns
Data Bus Hold Time	T_{HR}	10	—	ns
$\overline{IRQ}$ (Interval Timer Interrupt) valid before positive transition of clock	T_{IC}	200	—	ns

Note: Loading = 30 pF + 1 TTL load for PA0–PA7, PB0–PB7
= 130 pF + 1 TTL load for D0–D7

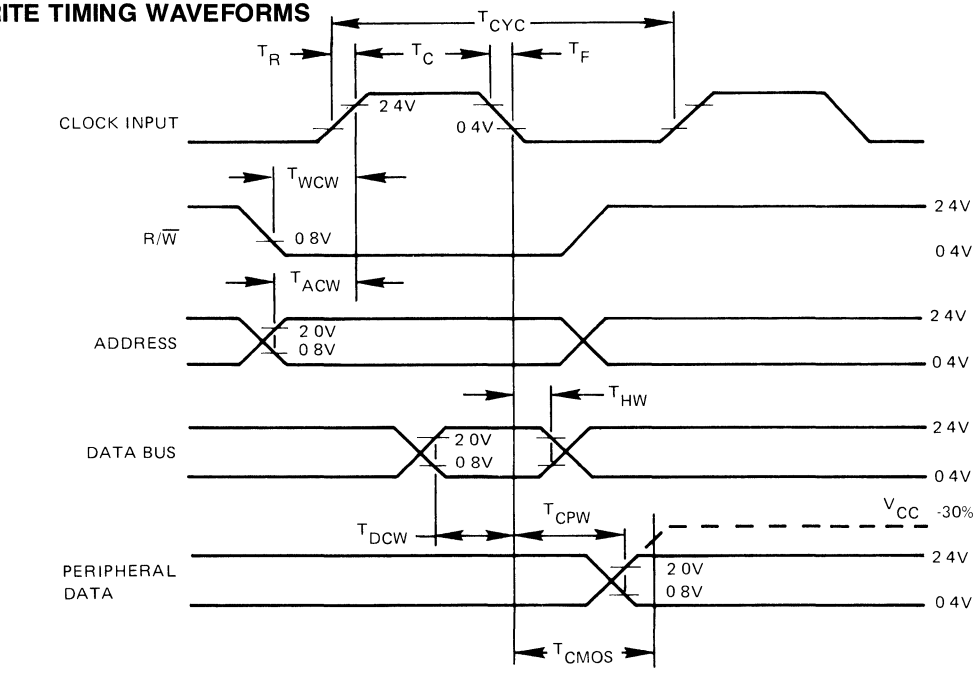
Write Timing

Characteristic	Symbol	Min	Max	Unit
Clock Period	T_{CYC}	1	10	μS
Rise & Fall Times	T_R, T_F	—	25	ns
Clock Pulse Width	T_C	470	—	ns
R/$\overline{W}$ valid before positive transition of clock	T_{WCW}	180	—	ns
Address valid before positive transition of clock	T_{ACW}	180	—	ns
Data Bus valid before negative transition of clock	T_{DCW}	300	—	ns
Data Bus Hold Time	T_{HW}	10	—	ns
Peripheral data valid after negative transition of clock	T_{CPW}	—	1	μS
Peripheral data valid after negative transition of clock driving CMOS (Level = VCC − 30%)	T_{CMOS}	—	2	μS

READ TIMING WAVEFORMS



WRITE TIMING WAVEFORMS



MAXIMUM RATINGS*

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to +7.0	V
Input/Output Voltage	V_{IN}	−0.3 to +7.0	V
Operating Temperature	T_A	0 to 70	°C
Storage Temperature	T_{STG}	−55 to +150	°C

*Note: All inputs contain protection circuitry to prevent damage due to high static charges. Care should be taken to prevent unnecessary application of voltage outside the specification range.

2

DC CHARACTERISTICS

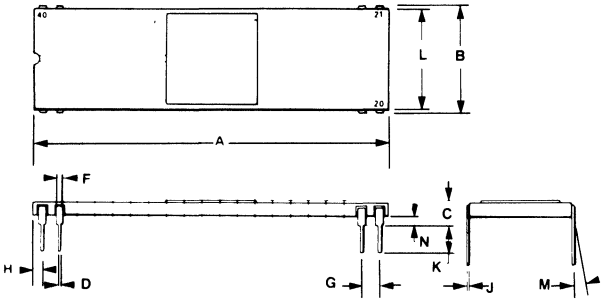
(V_{CC} = 5.0V ± 5%, V_{SS} = 0V, 0°C to 70°C, unless otherwise noted)

Characteristic	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Input High Voltage	V_{IH}	+2.4		V_{CC}	V	
Input Low Voltage	V_{IL}	−0.3		+0.4	V	
Input Leakage Current A0-A9, RS0, R/$\overline{W}$, $\overline{RES}$, 02, PB6(3), PB5(3)	I_{IN}		1.0	2.5	μA	V_{IN} = 0 to +5.0V V_{CC} = 0
Input Leakage Current for Three State Off D0-D7	I_{TSI}		±1.0	±10	μA	V_{IN} = 0.4V to 2.4V V_{CC} = 5.25V
Input High Current PA0-PA7, PB0-PB7	I_{IH}	−100	−300		μA	V_{IN} = 2.4V
Input Low Current; PA0-PA7 PB0-PB7	I_{IL}		−1.0	−1.6	mA	V_{IN} = 0.4V
Output High Voltage PA0-PA7, PB0-PB7 (TTL drive), D0-D7 PB0-PB7, (other drive, e.g., Darlington)	V_{OH}	 +2.4 +1.5			V	V_{CC} = 4.25V I_{LOAD} = −100 μA I_{LOAD} = 3.0 mA
Output Low Voltage	V_{OL}			+0 4	V	V_{CC} = 4.25V I_{LOAD} = 1.6 mA
Output High Current (Sourcing) PA0-PA7, PB0-PB7 (TTL drive), D0-D7 PB0-PB7 (other drive)	I_{OH}	 −100 −3 0	 −1000 −5.0		 μA mA	V_{OH} = 2.4V V_{OH} = 1 5V
Output Low Current (Sinking) PA0-PA7, PB0-PB7	I_{OL}	1.6			mA	V_{OL} = 0.4V
Power Dissipation	P_D		500	1000	mW	
Input Capacitance ø2 Logic	 C_{CLK} C_{IN}			 30 10	 pF pF	 V_{IN} = 0, f = 1 MHz T_A = 25°C
Output Capacitance	C_{OUT}					

Note: 1. All units are direct current (DC).
2. Negative sign indicates outward current flow, positive indicates inward flow.
3. When programmed as address pins.

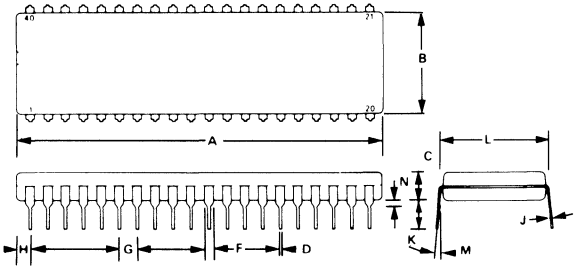
PACKAGE DIMENSIONS

40-PIN CERAMIC DIP



DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	50 29	51 31	1 980	2 020
B	14 86	15 62	0 585	0 615
C	2 54	4 19	0 100	0 165
D	0 38	0 53	0 015	0 021
F	0 76	1 40	0 030	0 055
G	2 54 BSC		0 100 BSC	
H	0 76	1 78	0 030	0 070
J	0 20	0 33	0 008	0 013
K	2 54	4 19	0 100	0 165
L	14 60	15 37	0 575	0 605
M	0°	10°	0°	10°
N	0 51	1 52	0 020	0 060

40-PIN PLASTIC DIP



DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	51 28	52 32	2 040	2 060
B	13 72	14 22	0 540	0 560
C	3 55	5 08	0 140	0 200
D	0 36	0 51	0 014	0 020
F	1 02	1 52	0 040	0 060
G	2 54 BSC		0 100 BSC	
H	1 65	2 16	0 065	0 085
J	0 20	0 30	0 008	0 012
K	3 05	3 56	0 120	0 140
L	15 24 BSC		0 600 BSC	
M	7°	10°	7°	10
N	0 51	1 02	0 020	0 040

Rockwell

R6531
ROM-RAM-I/O COUNTER (RRIOC)

DESCRIPTION

The R6531 ROM-RAM-I/O-Counter (RRIOC) integrates read-only memory, random access memory, various I/O data port configurations and timer functions into a single peripheral device which operates in conjunction with any CPU in the R6500 microprocessor family. The R6531 provides innovative system designers with a two-chip solution to a wide range of applications. It can also be combined in a variety of multi-chip system configurations with other R6531's, ROMs, RAMs and other I/O devices.

There are two R6531 versions: a 40-pin dual-in-line package; another with expanded I/O in a compact 52-pin quad-in-line package. Both versions contain a 2048 × 8 mask-programmable ROM, a 128 × 8 static RAM, a software programmable multi-mode counter, an 8-bit serial data channel, and 15 bidirectional data lines (two ports) with a handshake control mode and four interrupt inputs. The 52-pin version has an 8-bit output port and a 4-bit input port for a total of 27 I/O lines. Several mask options are available to provide a RAM standby power pin and chip selects for multi-chip systems.

Prototyping circuits are available in both the 40- and 52-pin packages, and in 1- and 2-MHz versions. They are offered as part numbers R6531-098 and R6531-098A for the 40-pin part, and as part numbers R6531-099 and R6531-099A for the 52-pin part.

ORDERING INFORMATION

Part Number:
R6531

Temperature Range: (T_L-T_h)
- Blank = 0° to +70°C
- E = −40°C to +85°C

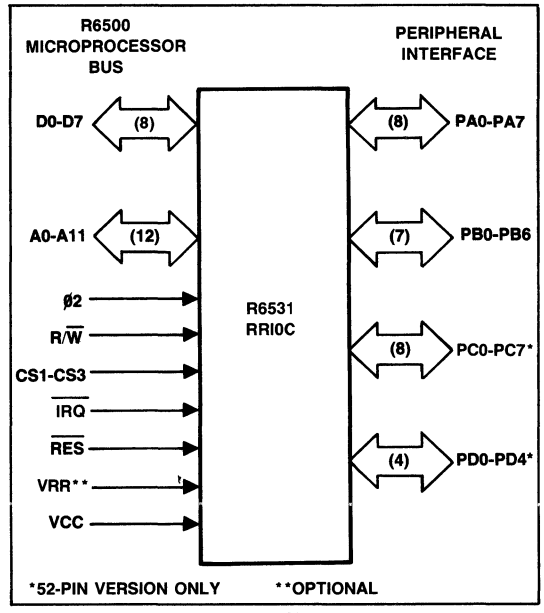
Package:
- C = 40-Pin DIP, Ceramic
- P = 40-Pin DIP, Plastic
- Q = 52-Pin QUIP, Plastic

Frequency Range:
- No letters = 1 MHz
- A = 2 MHz

NOTE: Contact your local Rockwell representative for availability.

FEATURES

- 2048 × 8 mask programmable ROM
- 128 × 8 static RAM
- 16-bit multi-mode counter/latch
  - — internal timer (one shot or free-running)
  - — pulse generator (one-shot or free-running)
  - — event counter
  - — external trigger
- 8-bit serial channel
- TTL compatible I/O, drive one TTL load
- 15 bidirectional I/O lines (2 ports — 40-pin package)
- Expansion 8-bit output port and 4-bit input port (52-pin package)
- I/O handshake control
- Four edge sensitive interrupt inputs
- 1 MHz or 2 MHz operation
- ROM-less versions available for prototyping
- Single +5V power supply



Interface Signals

INTERFACE SIGNALS

RESET ($\overline{RES}$)

This active low signal initializes the R6531. It clears all internal registers (except the counter and serial registers) to logic zero. This action places all bidirectional I/O lines in the input state and the Port C outputs in the high state. The timer, shift register, and interrupts are disabled. The $\overline{RES}$ signal must be low for at least four clock periods when reset is required.

ADDRESS BUS (A0–A11) AND CHIP SELECTS (CS1–CS3)

Memory and register selection is accomplished using the 12 address lines and, in multiple device systems, also using one or more of the three Chip Select mask options. When PB4, PB5, or PD2 are chosen as chip selects, they cannot be used as peripheral I/O pins.

DATA BUS (D0–D7)

The R6531 has eight data bus lines, which allow data to be transferred to or from the microprocessor. The output buffers remain in the off-state except when the R6531 is selected for a read operation.

READ/WRITE (R/$\overline{W}$)

The R/$\overline{W}$ input controls the transfer of data to and from the microprocessor and the R6531. A high on the R/$\overline{W}$ pin allows the processor to read (with proper addressing) the data supplied by the R6531. A low on the R/$\overline{W}$ pin allows a write (with proper addressing) to the R6531.

PHASE 2 CLOCK (ϕ2)

The Phase 2 Clock (ϕ2) input is the system clock that triggers all data transfers between the data bus and the R6531.

PERIPHERAL DATA PORTS (PA0–PA7, PB0–PB6, PC0–PC7, PD0–PD3)

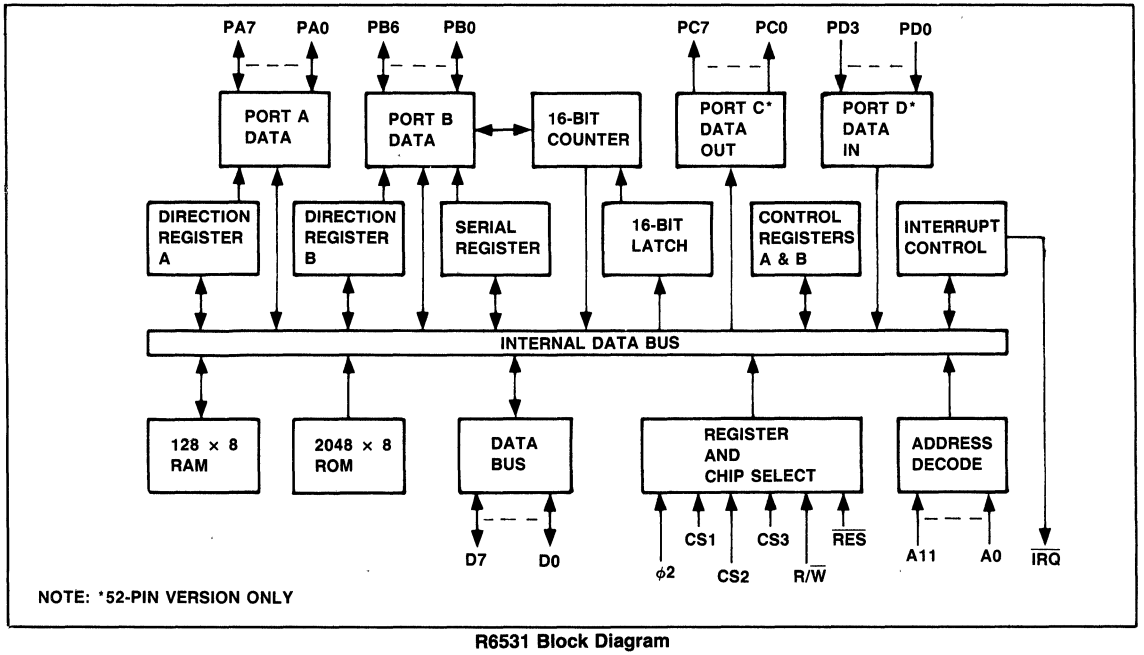
Both versions of the R6531 have 15 pins available for peripheral I/O operations. Each pin is software programmable to act as an input or an output. The pins are grouped into an 8-bit port, PA0-PA7, and a 7-bit port, PB0-PB6. The lines of the PB port may serve other functions. Ports PA and PB have associated data direction registers.

The expanded I/O of the 52-pin version provides an 8-bit output only part, PC0-PC7, and a 4-bit input only port PD0-PD3. PD2 and PD3 may be assigned other functions as described later.

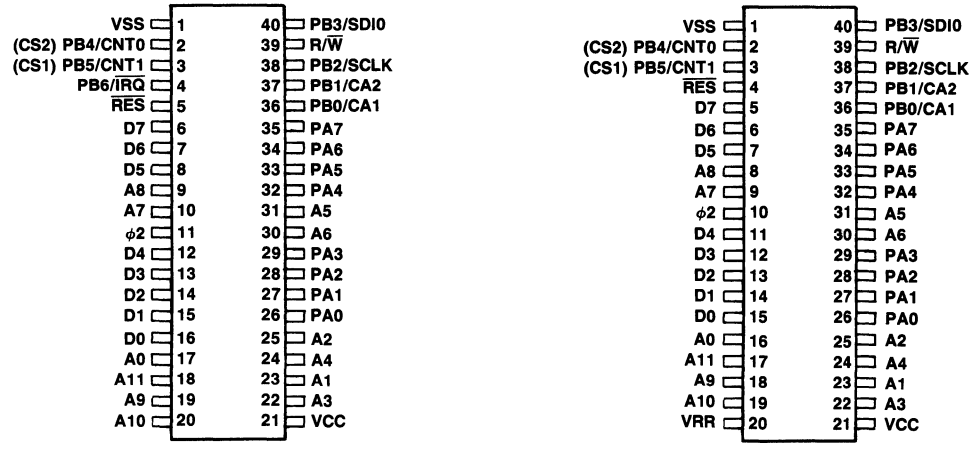
The outputs are push/pull type drivers capable of driving a single TTL load. When inputs are selected the drivers float. If PB6 is programmed as the $\overline{IRQ}$ request output, the line is driven low and requires an external pull-up, thus allowing the wire OR-ing of $\overline{IRQ}$ from other devices.

RAM RETENTION VOLTAGE (VRR)

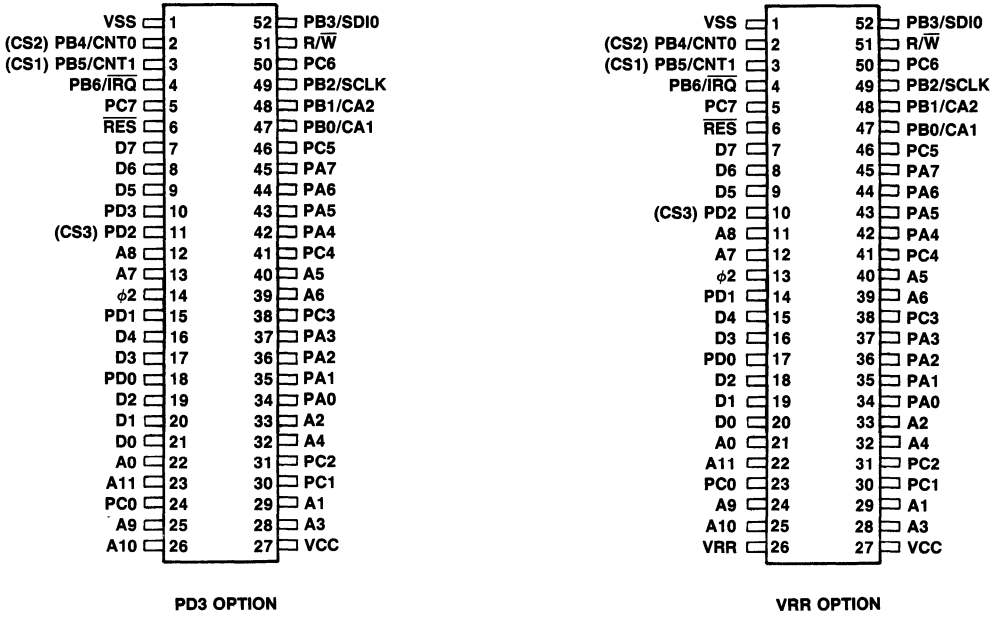
A separate pin for a power supply for the read/write memory is available as a mask option. This allows the retention of RAM data by using a battery back-up for the RAM only. Pin PB6 in the 40-pin version or PD3 in the 52-pin version is mask programmable as the VRR pin. Address line A10 must be held in the logic state which deselects RAM (user-defined) in order to protect the RAM data when VCC falls below the specified level or is turned off.



R6531 Block Diagram



R6531 40-Pin DIP Configurations



R6531Q 52-Pin QUIP Configurations

INTERNAL ORGANIZATION

The R6531 is divided into three basic functions: ROM, RAM, and I/O. The selection of any one of these three is accomplished by issuing the appropriate address information on the address bus when the chip is selected

ROM—2K BYTES (16K BITS)

The 16K ROM is a 2048 × 8 bit configuration. An address on lines A0-A10 uniquely selects one byte of ROM. Additionally, address line A11 and the chip selects are required to select the ROM function on a given chip. In a system with multiple R6531's, the CS1, CS2, and CS3 mask options allow up to seven devices with 14K bytes of ROM without the need for external decoding.

RAM—128 BYTES (1024 BITS)

The 128 × 8 static RAM of a given R6531 is addressed by lines A0-A6. Additionally, address lines A7-A11 and chip selects CS1, CS2, and CS3 provide selection of the RAM section of the device as well as the device itself when additional RAM devices or R6531's are in the system.

INPUT/OUTPUT

The input/output section is comprised of the data ports, direction registers, counter and associated latches, control registers, and interrupt registers. These I/O functions are all accessible by the R6502 CPU's instruction set using address bits A0-A3 for the specific function of the device. Address bits A4-A11 and CS1, CS2, and CS3 additionally may be decoded to select a given R6531 device in a multichip system.

Control Registers

Two control registers allow software selection of various I/O functions. The Peripheral Control Register (PCR) is primarily associated with Port B functions and the Auxiliary Control Register (ACR) is associated with the counter and serial data functions which also affect Port B.

ADDRESSING

Addressing of the R6531 offers many variations to the user for system configuration flexibility. Combination with other R6531 ROMs, RAMs or I/O devices is possible without need for external address decoding. Each of the three basic functions on the device has its own decode mask for unique selection.

The specific address ranges and chip selects are defined by the user and are dependent on the number of chips in the system. The programmed options to be fixed by masking are shown in Table 1.

Table 1. R6531 Addressing

R6531 Function	Chip Selects			Address Inputs (A0-A11)											
	CS3	CS2	CS1	11	10	9	8	7	6	5	4	3	2	1	0
ROM	X	X	X	X	2K ROM Decode										
RAM	Y	Y	Y	Y	Y	Y	Y	Y	128 RAM Decode						
I/O	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	I/O Decode		

The X, Y, and Z bits may be selected as high, low or no effect.

The chip select pins are also discrete I/O pins PB5, PB4, and PD2. The pins are independent of each other in that any one may be used as a chip select. The user specifies as mask options which pins are to be used as I/O and which as chip selects.

40-PIN PROTOTYPING CIRCUIT

Prototyping circuits R6531-098 (1 MHz) and R6531-098A (2 MHz) are packaged in a 40-pin dual in-line package that has the same pinouts as the 40-pin R6531 with PB6 option. In this prototyping circuit, the ROM is disabled and there is no VRR option. Access codes for this prototyping circuit are shown in Table 2.

Table 2. R6531-098 Addressing

R6531-098 Function	Chip Selects		Address Inputs (A0 - A11)											
	CS2	CS1	11	10	9	8	7	6	5	4	3	2	1	0
RAM	N	N	L	L	L	N	L	128 RAM Decode						
I/O	N	N	L	H	H	H	L	L	L	L	I/O Decode			

N means No Effect, H means High and L means Low.

52-PIN PROTOTYPING CIRCUIT

Prototyping circuits R6531-099 (1 MHz) and R6531-099A (2 MHz) are packaged in the 52-point quad in-line package, with VRR option. PD2 is used as a chip select (CS3), and PB4 and PB5 are available as I/O lines. Access codes for the prototyping circuit are shown in Table 3.

Table 3. R6531-099 Addressing

R6531-099 Function	Chip Selects			Address Inputs (A0-A11)											
	CS3	CS2	CS1	11	10	9	8	7	6	5	4	3	2	1	0
ROM	H	N	N	H	2K ROM Decode										
RAM	L	N	N	L	L	L	N	L	128 RAM Decode						
I/O	L	N	N	L	H	H	H	L	L	L	L	I/O Decode			

The 128 words or RAM have been mapped into the first half of both Page 0 and Page 1, to accommodate zero page addressing and stack operations. The full I/O capabilities described for the R6531 are available in the prototyping circuit, except that I/O lines PD2 and PD3 are dedicated to the VRR and CS3 mask options.

REGISTERS

REGISTER SELECTION

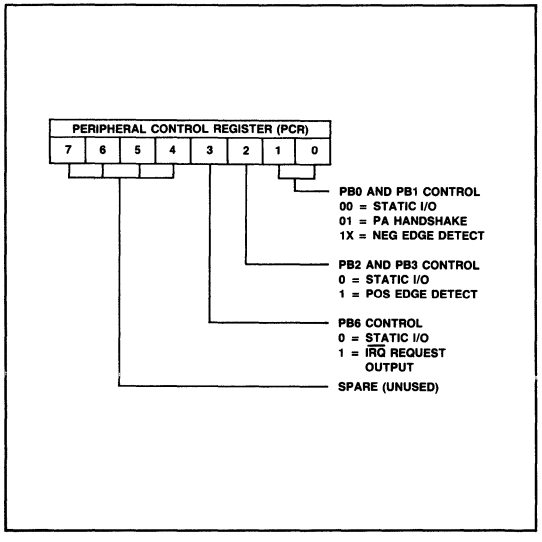
The register selection and/or general operation performed by the 15 R6531 addresses in conjunction with the R/$\overline{W}$ state is shown in Table 4.

Table 4. Register Selection

Hex Addr	Address Line				Operation	
	A3	A2	A1	A0	R/$\overline{W}$ = High	R/$\overline{W}$ = Low
0	L	L	L	L	Read Port A Data	Write Port A Data
1	L	L	L	H	Read Port B Data	Write Port B Data
2	L	L	H	L	—	Write Port C Data
3	L	L	H	H	—	Write Port D Data
4	L	H	L	L	Read Lower Counter	Write Lower Latch
5	L	H	L	H	Read Upper Counter	Write Upper Latch and Download
6	L	H	H	L	—	Write Lower Latch
7	L	H	H	H	—	Write Upper Latch
8	H	L	L	L	Read Serial Data Register	Write Serial Data Register
9	H	L	L	H	Read Interrupt Flag Register	Write Interrupt Flag Register
A	H	L	H	L	Read Interrupt Enable Register	Write Interrupt Enable Register
B	H	L	H	H	Read Auxiliary Control Register	Write Auxiliary Control Register
C	H	H	L	L	Read Peripheral Control Register	Write Peripheral Control Register
D	H	H	L	H	—	Write Port A Data Direction Register
E	H	H	H	L	—	Write Port B Data Direction Register

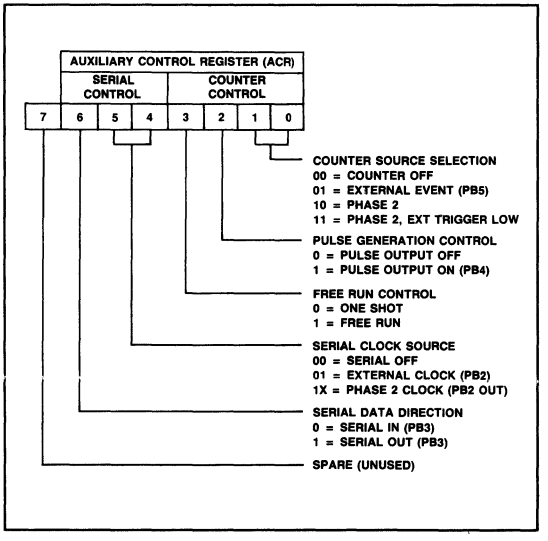
Peripheral Control Register (PCR)

Some Port B operating options are software selectable by writing control bits to the Peripheral Control Register (PCR).



Auxiliary Control Register (ACR)

Operating Modes for the Timer/Counter, PB2/PB3 Serial input/output and PB4 pulse output are selected by writing bits to the Auxiliary Control Register (ACR).



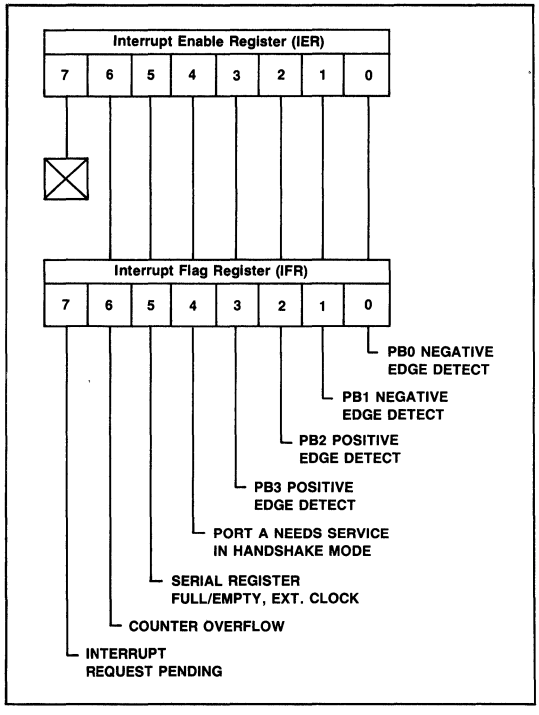
Interrupt Enable and Flag Registers

Two registers are provided for interrupt control. Corresponding bits in the enable and flag registers are logically ANDed to set the Interrupt Request Pending flag. If the pending flag is set and PB6 is selected as an $\overline{IRQ}$ Request Output, then PB6 will be set low to request the R6502 CPU to service $\overline{IRQ}$.

The interrupt enable bits are set or reset by writing into the Interrupt Enable Register. The interrupt flag bits IFR0-IFR6 can be cleared directly by writing a byte to the flag register which has 1's in those bit positions to be cleared.

IFR4 and IFR5 may also be cleared by reading or writing the Port A or Serial Data Registers respectively. IFR6 may also be cleared by reading the lower counter with I/O address hex 4 writing the upper latch with I/O addresses hex 5 or 7.

These registers and their bit assignments are illustrated.



PERIPHERAL DATA PORTS

Each line of the 8-bit data Port A may be individually selected as an input or output. Associated with the port is Data Direction Register — Port A (DDRA). Each line of the 7-bit date Port B may be individually selected as an input or an output. This port also has a Data Direction Register (DDRB). The two data direction registers (A and B) control the direction of the data into and out of the peripheral pins. A "1" written into the Data Direction Register sets up the corresponding peripheral pin as an output. Therefore, anything written into the data register will appear on that corresponding peripheral pin. A "0" written into the DDR inhibits the output buffer from transmitting data from the data register. For example, a "1" loaded into DDRA, position 3, sets up peripheral pin PA3 as an output. If a "0" had been loaded, PA3 would be configured as an input and would be in a float state.

Note that when lines in the PB port are used alternately as control lines for other on-chip functions, Direction Register B must also be loaded to set up the proper direction — the Control Registers have no effect on data direction.

The 8-bit Port C is an output only port. The 4-bit data Port D is an input only port.

For those lines being used as outputs, the data registers are used to latch data from the Data Bus during a Write operation so the peripheral device can read the data supplied by the microprocessor.

For the lines being used as inputs, the microprocessor is reading the peripheral data pins. For the peripheral data pins which are programmed as outputs the microprocessor will read the corresponding data bits of the Output data.

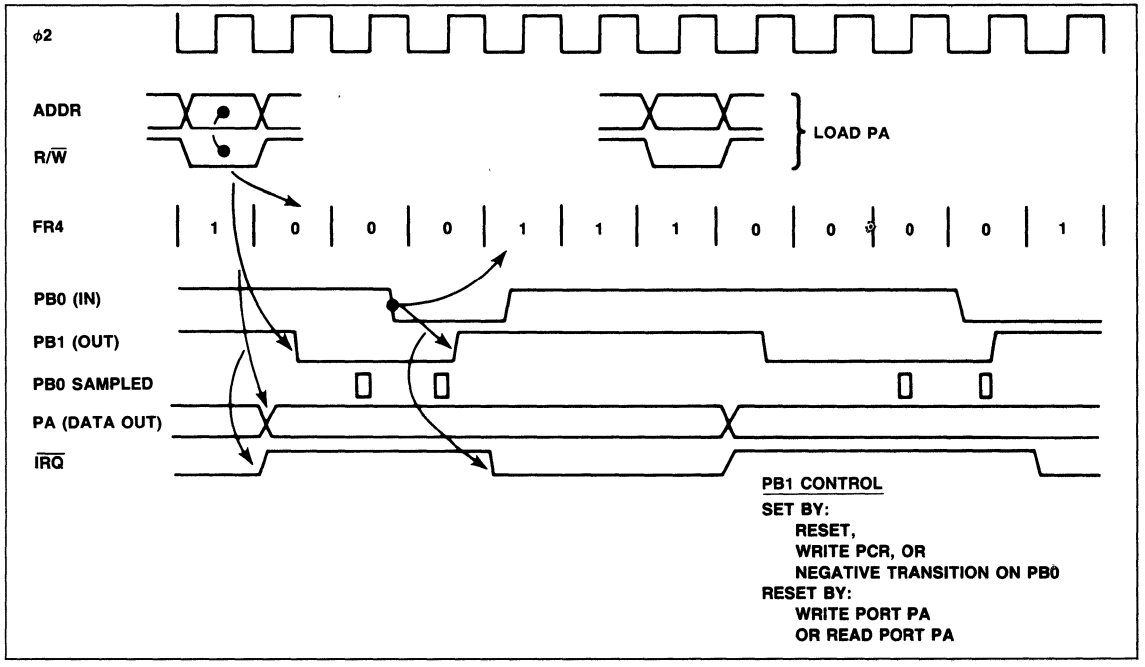
EDGE DETECT LOGIC

Operating in parallel with the I/O operation of PB0-PB3 is edge detect logic that is enabled by Peripheral Control Register bits 1 and 2. PCR1 enables logic that upon detection of a negative edge on PB0 or PB1 will set a corresponding flag in the Interrupt Flag Register. PCR2 enables logic that upon detection of a positive edge on PB2 or PB3 will set corresponding flags in the Interrupt Flag Register. If corresponding bits are set in the Interrupt Enable Register, then the Interrupt Request Pending flag will be set.

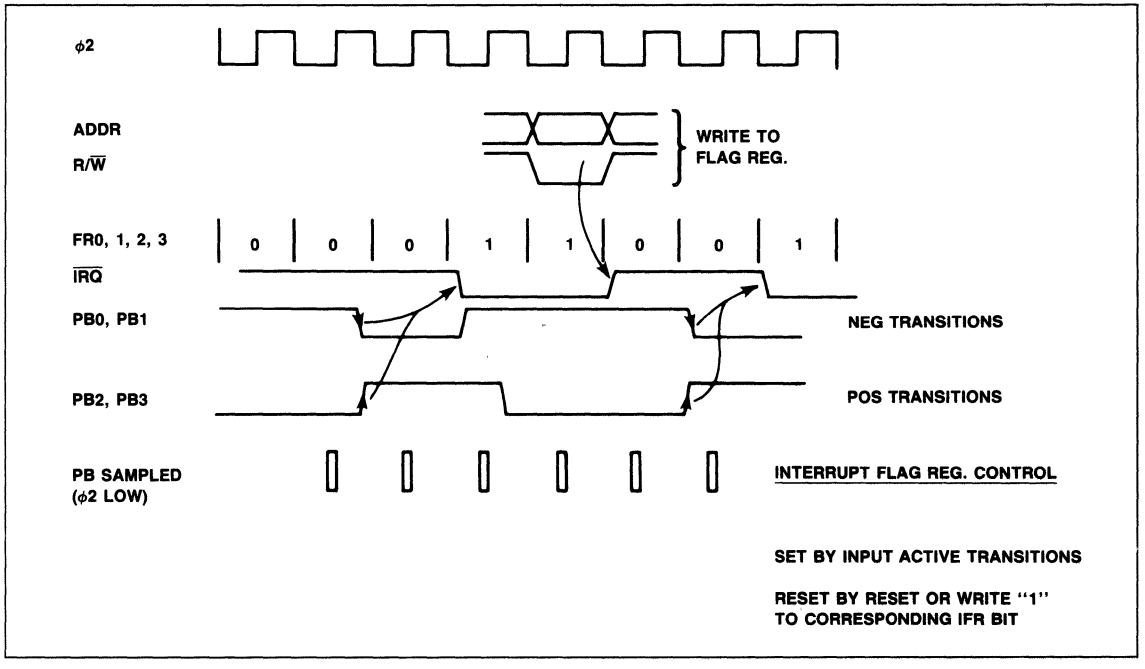
HANDSHAKE OPERATIONS

PB0 and PB1 may be used as handshake control lines for date transmissions over Port PA; see PCR definition. PB0 is a control input, PB1 is a control output. PB1 switches low on a read or write to Port PA, and switches high in response to a negative transition on PB0.

IFR4 in the Flag Register is set by a negative transition on PB0, and cleared by a Read or Write to Port PA; see Handshake Timing Diagram for timing details.



R6531 Timing for Handshake Mode



R6531 Timing for Interrupt Mode

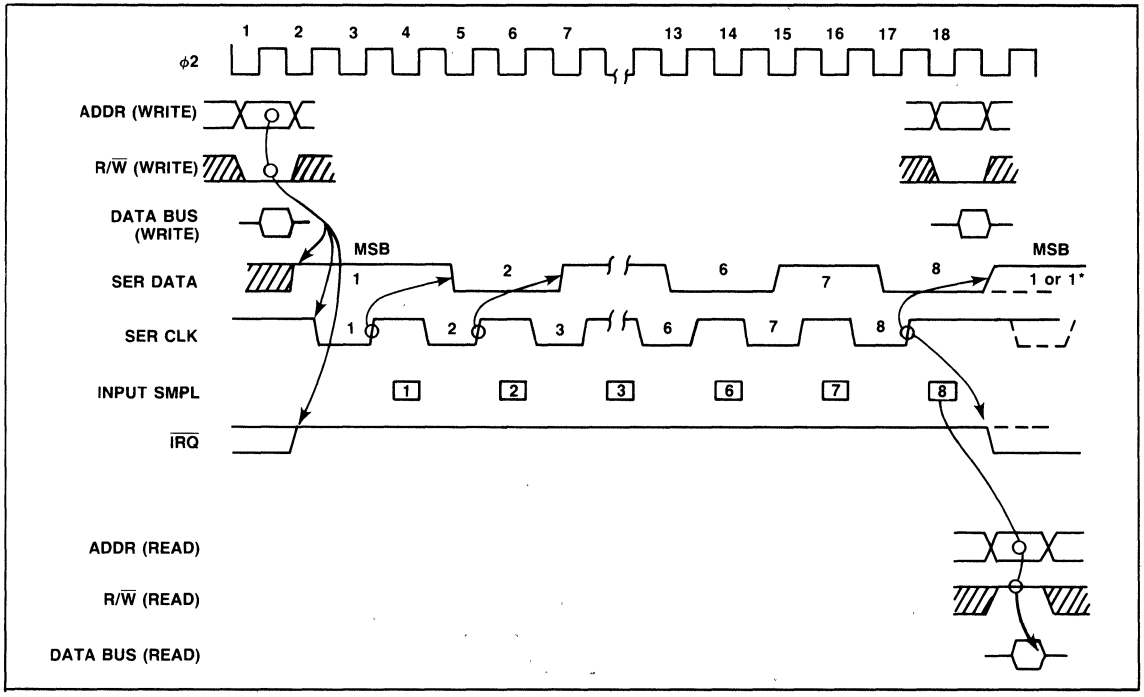
SERIAL DATA CHANNEL

The R6531 has an 8-bit serial channel. PB2 and PB3 are software selectable as the serial clock (SCLK) and serial data (SDI0) lines respectively.

The software sets Auxiliary Control Register bits 4 and 5 to enable the serial channel and to specify the source of the shift clock. Selection of the internal clock will shift data at one half the system $\phi 2$ clock rate. If the external clock is used, data may be shifted at any rate up to one half the system $\phi 2$ clock rate. In the external clock mode, the counter may be operated in the free run pulse generation mode using the CNTO line externally connected to the SCLK line to provide the desired shift rate.

Auxiliary Control Register bit 6 sets the serial data direction. Data are shifted in or out, most significant bit first, under control of the shift clock.

In the external clock mode, the completion of eight shifts of the serial register will set bit 5 of the interrupt flag register. If the corresponding bit of the Interrupt Enable Register is also set an Interrupt Request Pending flag will be set.



R6531 Serial I/O Timing

COUNTER/TIMER

The R6531 contains a multi-mode 16-bit counter/timer with an associated 16-bit latch whose modes are software selectable by setting appropriate bits in the Auxiliary Control Register. The latch holds the counter preset value and all 16 bits download to the counter simultaneously upon command (I/O address hex 5) of the software or automatically in free run modes upon overflow of the counter. The counter is a decrementing counter and causes the setting of a flag in the Interrupt Flag Register when it overflows. This interrupt flag, bit 6, is logically ANDed with a corresponding counter overflow interrupt enabled bit to set the Interrupt Request Pending flag. The Auxiliary Control Register is used to set four basic modes which specify the source of the count information, and to select two mode modifiers that apply equally to the three active modes.

Mode 0 —Counter Off

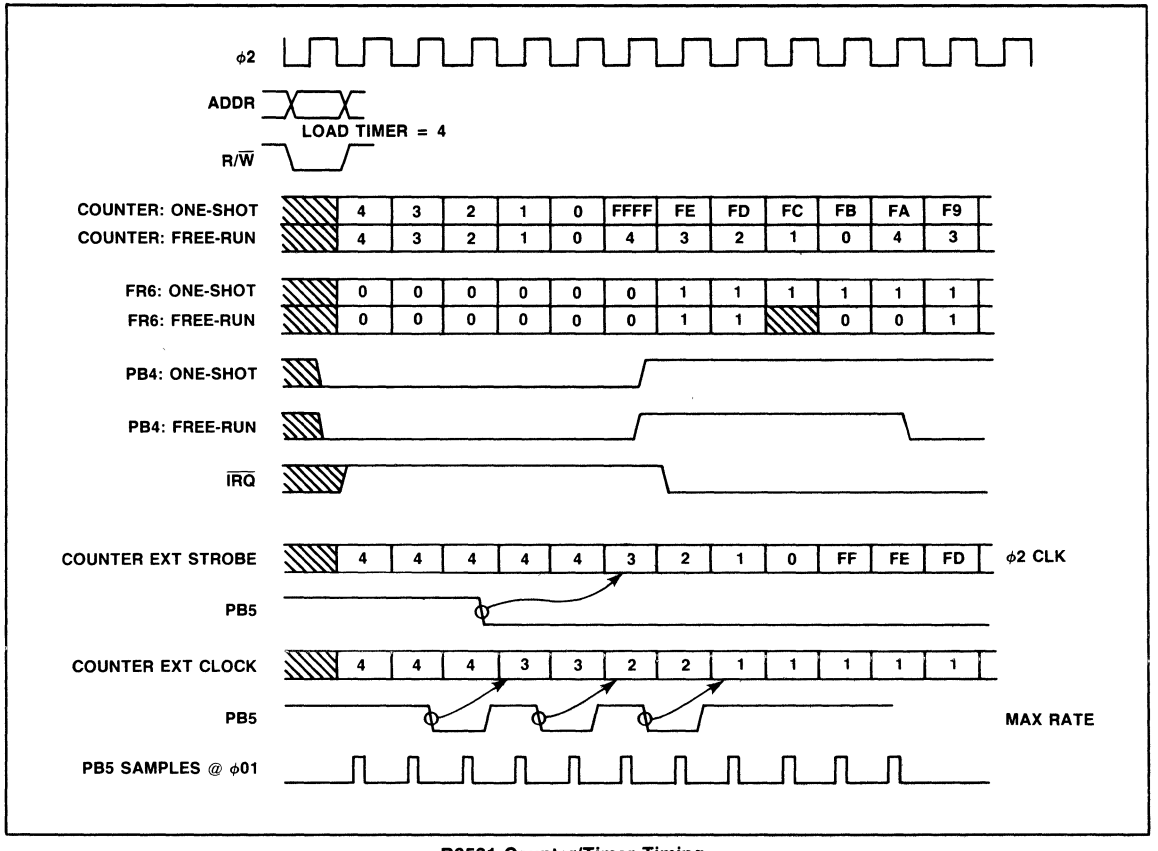
Mode 1 —Event Counter — counts external event inputs (negative transitions) at PB5

Mode 2 —Interval Timer — counts Ø2 system clock pulses.

Mode 3 —External Trigger — counts Ø2 system clock pulses starting with a negative transition on PB5.

Mode Modifier A —Pulse Generation Control — causes the output level on PB4 to switch low each time the counter is loaded using I/O address hex. 5. At counter overflow, PB4 switches high. If in the free run mode, PB4 continues to toggle at each subsequent counter overflow; otherwise there are no further transitions until the counter is reactivated by the software.

Mode Modifier B —Free-Run Control — causes the full 16-bit latch to be downloaded to the counter, continues to count, and sets the counter overflow flag bit every time the counter overflows. Otherwise the counter is a one shot mode in which the counter overflow flag is set one time only until the counter is reactivated by the software.



R6531 Counter/Timer Timing

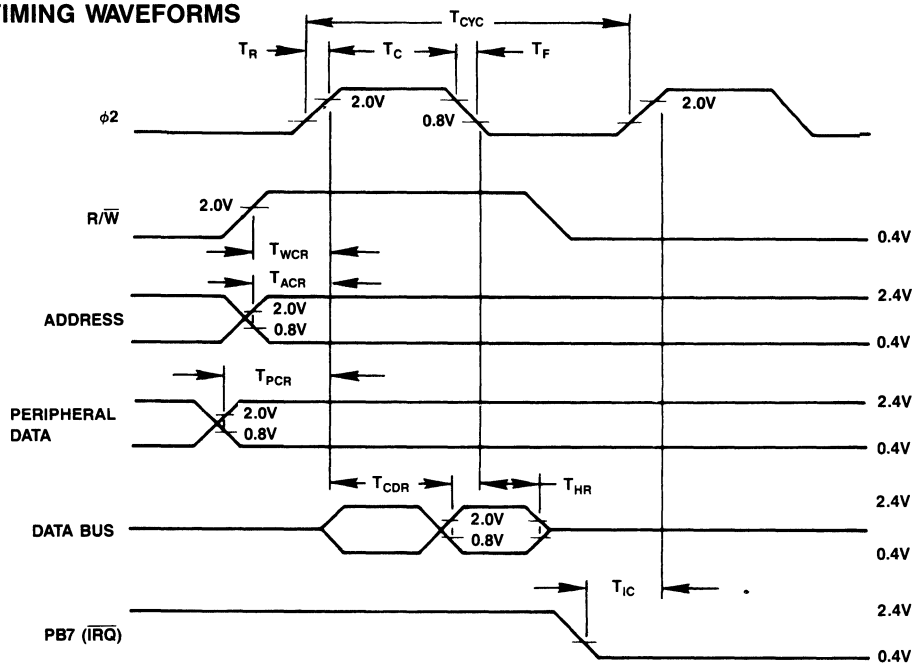
BUS TIMING CHARACTERISTICS

Characteristic	Symbol	R6531 (1 MHz) Min	R6531 (1 MHz) Max	R6531A (2 MHz) Min	R6531A (2 MHz) Max	Unit
Clock Period	T_{CYC}	1.0	10	0.5	10	µs
Clock Pulse Width	T_C	470	—	235	—	ns
Rise & Fall Times	T_R, T_F	—	25	—	15	ns
READ TIMING						
R/$\overline{W}$ valid before positive transition of clock	T_{WCR}	180	—	120	—	ns
Address valid before positive transition of clock	T_{ACR}	180	—	120	—	ns
Peripheral data valid before positive transition of clock	T_{PCR}	270	—	135	—	ns
Data Bus valid after positive transition of clock	T_{CDR}	—	350	—	180	ns
Data Bus Hold Time	T_{HR}	10	—	10	—	ns
$\overline{IRQ}$ valid after negative transition of clock	T_{IC}	—	900	—	450	ns
WRITE TIMING						
R/$\overline{W}$ valid before positive transition of clock	T_{WCW}	180	—	120	—	ns
Address valid before positive transition of clock	T_{ACW}	180	—	120	—	ns
Data Bus valid before negative transition of clock	T_{DCW}	270	—	135	—	ns
Data Bus Hold Time	T_{HW}	10	—	10	—	ns
Peripheral data valid after negative transition of clock	T_{CPW}	—	900	—	450	ns

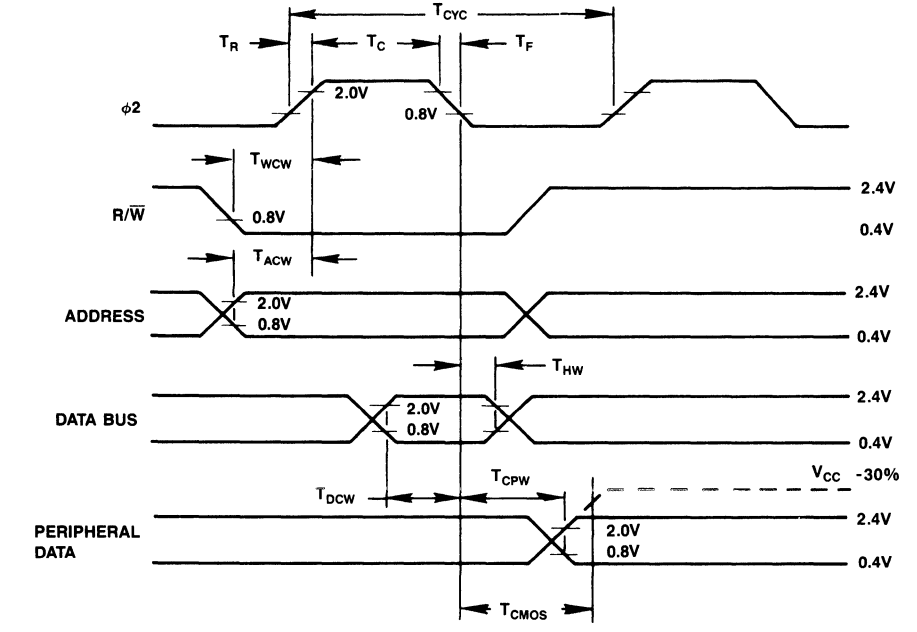
NOTES:

Load = 100 pF + 1 TTL for PA0-PA7, PB0-PB6, and PC0-PC7.
= 100 pF + 1 TTL for D0-D7 (R6531A).
= 130 pF + 1 TTL for D0-D7 (R6531).

READ TIMING WAVEFORMS



WRITE TIMING WAVEFORMS



MAXIMUM RATINGS*

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to 7.0	Vdc
Input Voltage	V_{in}	−0.3 to +7.0	Vdc
Operating Temperature Range Commercial Industrial	T_A	 0 to +70 −40 to +85	 °C °C
Storage Temperature Range	T_{stg}	−55 to +150	°C

*__Note:__ This device contains circuitry to protect the inputs against damage due to high static voltages, however, normal precautions should be taken to avoid application of any voltage higher than maximum rated voltages to this circuit.

DC CHARACTERISTICS

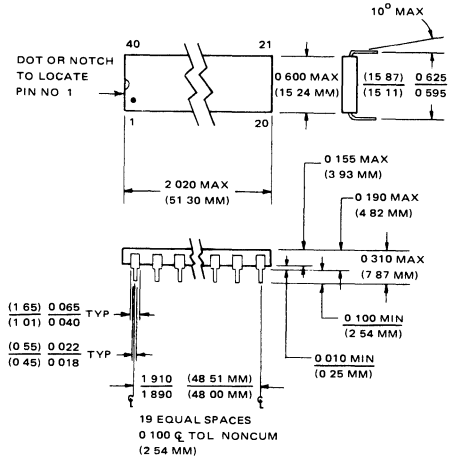
(V_{CC} 5.0V ±10%, V_{CC} = 5.0V ±5% A, V_{SS} = 0, T_A = T_L to T_H, unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit(1)	Test Conditions
Input High Voltage	V_{IH}	2.0	V_{CC}	V	
Input Low Voltage	V_{IL}	−0.3	+0.8	V	
Input Leakage Current A0–A11, CS1–CS3, R/$\overline{W}$, $\overline{RES}$, ϕ2, PD0–PD3	I_{IN}	—	2.5	μA	V_{IN} = 0V to 5.0V V_{CC} = 0V
Leakage Current for Three-State Off (Three State) D0–D7, PA0–PA7, PB0–PB6	I_{TSI}	—	±10	μA	V_{IN} = 0.4V to 2.4V V_{CC} = 5.0V
Input High Current PA0–PA7, PB0–PB6, PD0–PD3	I_{IH}	−100	—	μA	V_{IN} = 2.4V
Input Low Current PA0–PA7, PB0–PB6, PD0–PD3	I_{IL}	1.6	—	mA	V_{IN} = 0.4V
Output High Voltage D0–D7, PA0–PA7, PB0–PB6, PC0–PC7	V_{OH}	+2.4	—	V	V_{CC} = 4.75V I_{LOAD} = −200 μA
Output Low Voltage D0–D7, PA0–PA7, PB0–PB6, PC0–PC7	V_{OL}		+0.4	V	V_{CC} = 4.75V I_{LOAD} = 2.5 mA
Output High Current (Sourcing), PA0–PA7, PB0–PB6, PC0–PC7	I_{OH}	−200	—	μA	V_{OH} = 2.4V
Output Low Current (Sinking) PA0–PA7, PB0–PB7, PC0–PC7	I_{OL}	2.1	—	mA	V_{OL} = 0.4V
Input Capacitance ϕ2 Logic	 C_{Clk} C_{IN}		 20 10	 pF pF	V_{CC} = 5.0V, V_{IN} = 0V, f = 1 MHz,
Output Capacitance	C_{OUT}		10	pF	T_A = 25°C
Power Dissipation	P_D		1.0	W	

NOTES:
1 All units are direct current (DC)
2 Negative sign indicates current flow, positive indicates inward flow

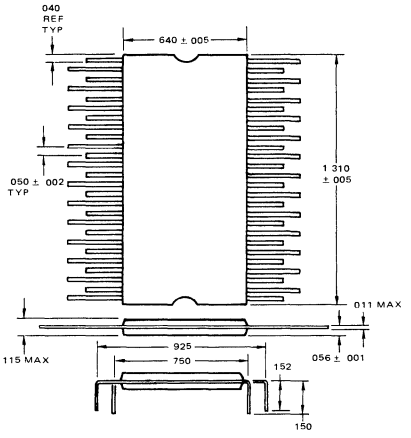
PACKAGE DIMENSIONS

40-PIN DIP



NOTE Pin No 1 is in lower left corner when symbolization is in normal orientation

52-PIN PLASTIC QUIP



Rockwell

R6532
RAM-I/O-TIMER (RIOT)

DESCRIPTION

The R6532 RAM-I/O-Timer (RIOT) integrates random access memory (RAM), parallel I/O data ports and timer functions into a single peripheral device which operates in conjunction with any CPU in the R6500 microprocessor family. It is comprised of a 128 × 8 static RAM, two software-controlled, 8-bit bidirectional data ports allowing direct interfacing between the microcomputer and peripheral devices, a software programmable interval timer with interrupt, capable of timing in various intervals from 1 to 262,144 clock periods, and a programmable edge-detect circuit.

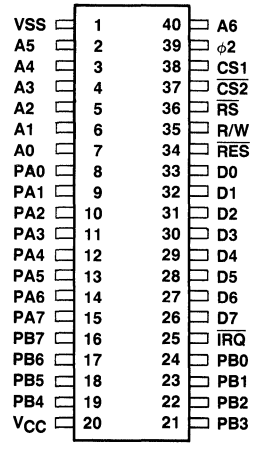
FEATURES

- 128 × 8 static RAM
- Two 8 bit bidirectional data ports
- Programmable interval timer with interrupt capability
- TTL & CMOS compatible peripheral lines
- One port has direct transistor drive capability
- Programmable edge-sensitive interrupt input
- 8 bit bidirectional data bus
- 6500/6800 bus compatible
- 1 MHz and 2 MHz parts available
- Single +5V power supply

ORDERING INFORMATION

Part Number: R6532 _ _ _

- Temperature Range:
  - Blank = 0°C to +70°C
  - E = −40°C to +85°C
- Package:
  - C = Ceramic DIP
  - P = Plastic DIP
- Frequency:
  - No Letter = 1 MHz
  - A = 2 MHz



R6532 Pin Configuration

INTERFACE SIGNALS

RESET ($\overline{RES}$)

During system initialization, a low $\overline{RES}$ input causes a zeroing of all four I/O registers. This in turn causes all I/O buses to act as inputs thus protecting external components from possible damage and erroneous data while the system is being configured under software control. The Data Bus Buffers are put into an OFF-STATE during Reset. Interrupt capability is disabled with the $\overline{RES}$ signal. The $\overline{RES}$ signal must be held low for at least two clock periods when reset is required.

READ/WRITE (R/$\overline{W}$)

The R/$\overline{W}$ signal is supplied by the microprocessor and controls the transfer of data to and from the R6532. A high on the R/$\overline{W}$ pin allows the processor to read (with proper addressing) the data supplied by the R6532. A low on the R/$\overline{W}$ pin allows a write (with proper addressing) to the R6532.

INTERRUPT REQUEST ($\overline{IRQ}$)

The $\overline{IRQ}$ pin is an interrupt pin from the interrupt control logic. The pin will be normally high with a low indicating an interrupt from the R6532. An external 3K pull-up resistor is required. The $\overline{IRQ}$ pin may be activated by a transition on PA7 or timeout of the interval timer.

DATA BUS (D0–D7)

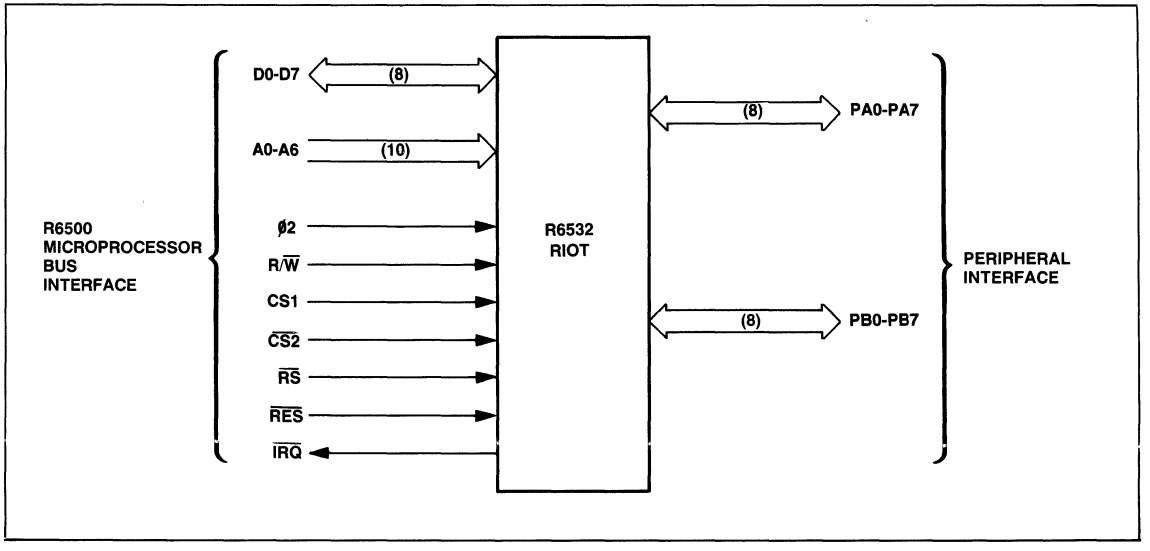
The R6532 has eight bidirectional data pins (D0–D7). These pins connect to the system's data lines and transfer data between the R6532 and the microprocessor data bus. The output buffers remain off, or tri-stated, except when the R6532 is selected for a Read operation.

ADDRESS LINES (A0–A6)

There are seven address pins (A0–A6). In addition, there is the $\overline{RAM\ SELECT}$ ($\overline{RS}$) pin. The pins A0–A6 and $\overline{RS}$ are always used as addressing pins. There are two additional pins which are used as CHIP SELECTS. They are pins CS1 and $\overline{CS2}$. Tables 1 and 2 identify the functions selected and registers addressed depending upon the address line and $\overline{RS}$ inputs in conjunction with the R/$\overline{W}$ level.

I/O PORTS (PA0–PA7, PB0–PB7)

The R6532 has 16 pins available for peripheral I/O operations. Each pin is individually software programmable to act as either an input or an output. The 16 pins are divided into two 8-bit ports, PA0–PA7 and PB0–PB7. (PA7 also has another use which is discussed later.) Each is set up as an input by writing a "0" into the corresponding bit of the data direction register. A "1" written into the data direction register causes its corresponding bit to be an output. When in the input mode, the peripheral output buffers are in the "1" state and the internal pull-up device acts as less than one TTL load to the peripheral data lines. On a Read operation, the microprocessor reads the peripheral pin. When the peripheral device gets information from the R6532 it receives data stored in the data register. The microprocessor reads valid pin information if the peripheral lines are greater than 2.0 volts for a "1" and less than 0.8 volt for a "0" as the peripheral pins are all TTL compatible. Pins PB0–PB7 are also capable of sourcing 3 ma at 1.5V, thus making them capable of Darlington drive.



RIOT Interface Signals

Table 1. Address Decoding

Operation	$\overline{RS}$	R/$\overline{W}$	A4	A3	A2	A1	A0
Write RAM	0	0	—	—	—	—	—
Read RAM	0	1	—	—	—	—	—
Write Output Reg A	1	0	—	—	0	0	0
Read Output Reg A	1	1	—	—	0	0	0
Write DDRA	1	0	—	—	0	0	1
Read DDRA	1	1	—	—	0	0	1
Write Output Reg B	1	0	—	—	0	1	0
Read Output Reg B	1	1	—	—	0	1	0
Write DDRB	1	0	—	—	0	1	1
Read DDRB	1	1	—	—	0	1	1
Write Timer							
−1T	1	0	1	(a)	1	0	0
−8T	1	0	1	(a)	1	0	1
−64T	1	0	1	(a)	1	1	0
−1024T	1	0	1	(a)	1	1	1
Read Timer	1	1	—	(a)	1	—	0
Read Interrupt Flag	1	1	—	—	1	—	1
Write Edge Detect Control	1	0	0	—	1	(b)	(c)

Notes:
— = Don't Care, "1" = High level (≥2.4V), "0" = Low level (≤0.4V)

(a) A3 = 0 to disable interrupt from timer to $\overline{IRQ}$
A3 = 1 to enable interrupt from timer to $\overline{IRQ}$

(b) A1 = 0 to disable interrupt from PA7 to $\overline{IRQ}$
A1 = 1 to enable interrupt from PA7 to $\overline{IRQ}$

(c) A0 = 0 for negative edge-detect
A0 = 1 for positive edge-detect

Table 2. Register Addressing

Start Address +	Register/Function	Start Address +	Register/Function
$0	DRA ('A' side data register)	$7	Write edge-detect control (positive edge-detece, enable interrupt)
$1	DDRA ('A' side data direction register)		
$2	DRB ('B' side data register)	$C	Read timer (enable interrupt)
$3	DDRB ('B' side data direction register)	$14	Write timer (divide by 1, disable interrupt)
$4	Read timer (disable interrupt)	$15	Write timer (divide by 8, disable interrupt)
$4	Write edge-detect control (negative edge-detect, disable interrupt)	$16	Write timer (divide by 64, disable interrupt)
		$17	Write timer (divide by 1024, disable interrupt)
$5	Read interrupt flag register (bit 7 = timer, bit 6 = PA7 edge-detect) Clear PA7 flag	$1C	Write timer (divide by 1, enable interrupt)
		$1D	Write timer (divide by 8, enable interrupt)
$5	Write edge-detect control (positive edge-detect, disable interrupt)	$1E	Write timer (divide by 64, enable interrupt)
		$1F	Write timer (divide by 1024, enable interrupt)
$6	Write edge-detect control (negative edge-detect, enable interrupt)		

INTERNAL ORGANIZATION

The R6532 is divided into four basic sections, RAM, I/O, Timer, and Interrupt Control. The RAM interfaces directly with the microprocessor through the system data bus and address lines. The I/O section consists of two 8-bit halves Each half contains a Data Direction Register (DDR) and a Data Register (DR).

RAM—128 BYTES (1024 BITS)

The 128 × 8 Read/Write Memory acts as a conventional static RAM and can be accessed from the microprocessor by selecting the chip (CS1 = high, $\overline{CS2}$ = low) and by setting $\overline{RS}$ low. Address lines A0 through A6 then select the desired byte of storage.

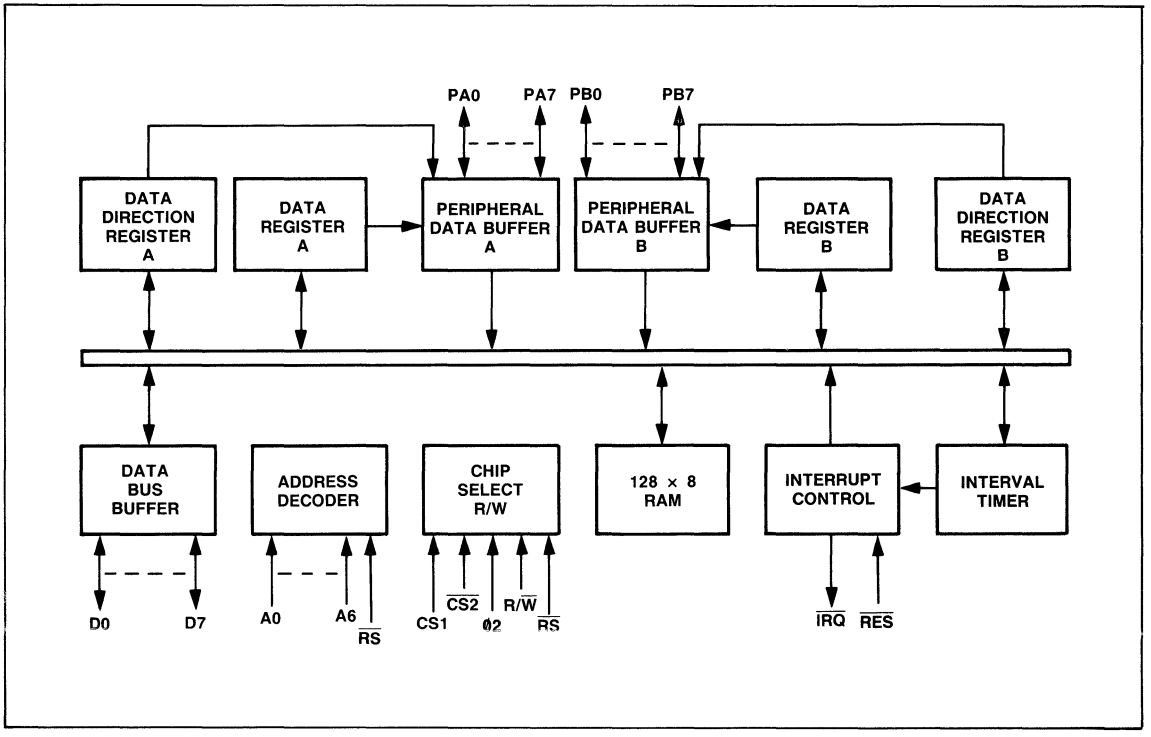
I/O PORTS AND REGISTERS

The I/O Ports consist of eight lines which can be individually programmed to act as either an input or an output A logic zero in a bit of the Port A Data Direction Register (DDRA) causes the corresponding line of Port A to act as an input. A logic one causes the corresponding Port A line to act as an output. The voltage on any line programmed to be an output is determined by the corresponding bit in the Port A Data Register (DRA).

Data is read directly from the data pins during any read operation. For any output pin, the data transferred into the processor will be the same as that contained in the Data Register if the voltage on the pin is allowed to go to 2.4V for a logic one. Note that for input lines, the processor can write into the corresponding bit of the Data Register. This will not affect the polarity on the pin until the corresponding bit of DDRA is set to a logic one to allow the I/O line to act as an output.

The operation of the Port B is exactly the same as the normal I/O operation of the Port A. Each of the eight lines can each be programmed to act as either an input or as an output by placing a 0 or a 1 into the Port B Data Direction register (DDRB). In the output mode, the voltage on a peripheral pin is controlled by the Port B Data Register (DRB).

The primary difference between Port A and the Port B is in the operation of the output buffers which drive these pins. The Port B output buffers are push-pull devices which are capable of sourcing 3 ma at 1.5V This allows these pins to directly drive transistor switches. To assure that the microprocessor will read proper data on a "Read Port B" operation, logic in the R6532 allows the microprocessor to read the Output Register instead of reading the peripheral pin as on Port A.



R6532 Block Diagram

EDGE DETECTING WITH PA7

In addition to acting as a peripheral I/O line, the PA7 line can be used as an edge-detecting input. In this mode, an active transition sets the internal interrupt flag (bit 6 of the Interrupt Flag register). Setting the interrupt flag causes $\overline{IRQ}$ output to go low if the PA7 interrupt has been enabled.

Control of the PA7 edge detecting mode is accomplished by writing to one of four addresses. In this operation, A0 controls the polarity of the active transition and A1 acts to enable or disable interrupting of the processor. The data which is placed on the Data Bus during this operation is discarded and has no effect on the control of PA7.

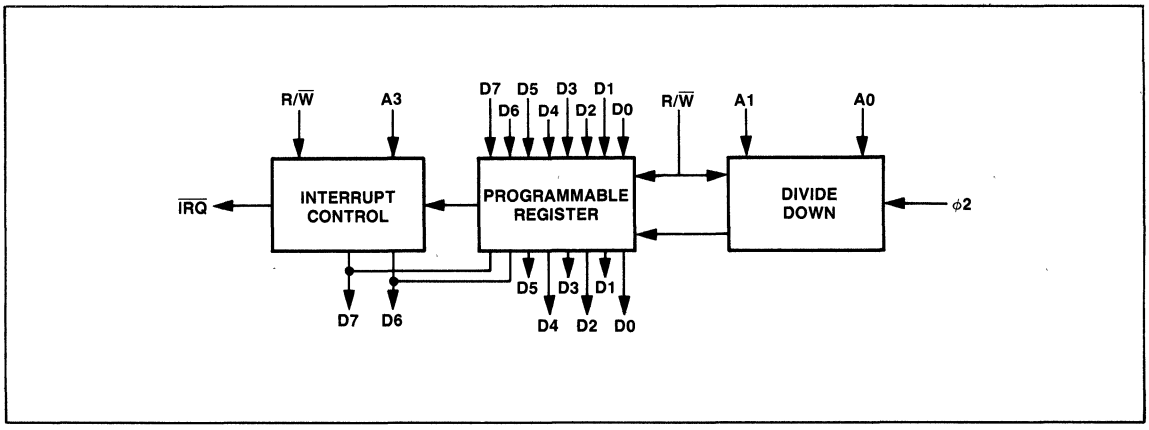
The PA7 interrupt flag is set on an active transition, even if the pin is being used as a normal input or as a peripheral control output. The flag is also set by an active transition if the PA7 interrupt is disabled. The reset signal ($\overline{RES}$) disables the PA7 interrupt and enables negative (high-to-low) edge detection on PA7. The PA7 edge detect logic can be set to detect either a positive or negative transition and to either enable or disable interrupt ($\overline{IRQ}$) generation upon detection.

During system initialization, the interrupt flag may inadvertently be set by an unexpected transition on the PA7. It is therefore recommended that the interrupt flag be cleared *before* enabling interrupting from PA7. To clear PA7 interrupt flag, simply read the interrupt Flag Register.

INTERVAL TIMER

The Timer section of the R6532 contains three basic parts: preliminary divide down register, programmable 8-bit register and interrupt logic.

The Timer can be programmed to count up to 255 time intervals. Each time interval can be either 1T, 8T, 64T or 1024T increments, where T is the system clock period. When a full count is reached, an interrupt flag is set to logic "1". After the interrupt flag is set the internal clock begins counting down at the system clock rate to a maximum of −255T. Thus, after the interrupt flag is set, a Read of the timer will tell how long since the flag was set up to a maximum of 255T.



Basic Elements of Interval Timer

INTERVAL TIMER EXAMPLE

The 8-bit microprocessor data bus transfers data to and from the Timer. If a count of 52 time intervals were to be counted, the pattern 0 0 1 1 0 1 0 0 would be put on the data bus and written into the divide by 1 Timer register.

At the same time that data is being written to the Timer, the counting intervals of 1, 8, 64, 1024T are decoded from address lines A0 and A1. During a Read or Write operation address line A3 controls the interrupt capability of PB7, i.e., A3 = 1 enables $\overline{IRQ}$, A3 = 0 disables $\overline{IRQ}$. When the timer is read prior to the interrupt flag being set, the number of time intervals remaining will be read, i.e., 51, 50, 49, etc.

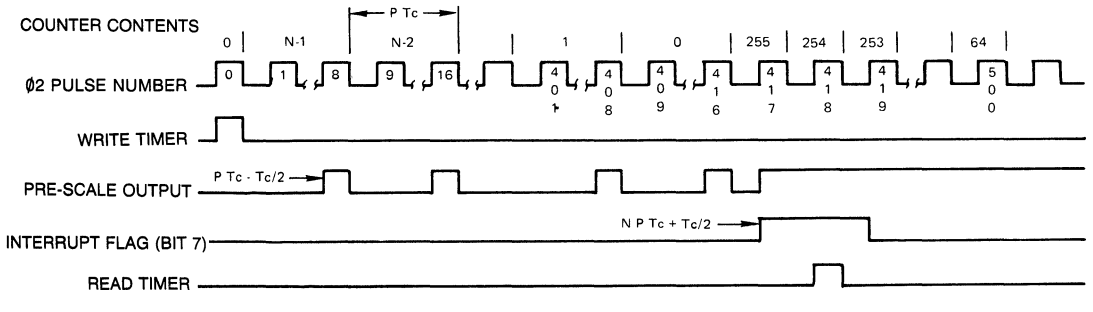
When the Timer has counted through 0 0 0 0 0 0 0 0 on the next count time an interrupt will occur and the counter will read 1 1 1 1 1 1 1 1. After the interrupt flag is set, the timer register decrements at a divide by "1" rate of the system clock. If the timer is read after the interrupt flag is set and a value of 1 1 1 0 0 1 0 0 is read, the time since interrupt is 27T. The value read is in two's complement, but remember that interrupt occurred on count number one. Therefore, we must subtract 1.

Value read	= 1 1 1 0 0 1 0 0	
Complement	= 0 0 0 1 1 0 1 1	
ADD 1	= 0 0 0 1 1 1 0 0 =	28 Equals two's complement of register
SUB 1	= 0 0 0 1 1 0 1 1 =	27

Thus, to arrive at the *total* elapsed time, merely do a two's complement add to the original time written into the timer. Again, assume time written as 0 0 1 1 0 1 0 0 (=52). With a divide by 8, total time to interrupt is (52 × 8) + 1 = 417T. Total elapsed time would be 416T + 27T = 443T, assuming the value read after interrupt was 1 1 1 0 0 1 0 0.

The interrupt flag will be reset whenever the Timer is accessed by a read or a write. However, the reading of the timer at the same time the interrupt occurs will not reset the interrupt flag. When the interrupt flags are read (D7 for the timer, D6 for the edge detect) data bus lines D0–D5 go to 0.

When reading the timer after an interrupt, A3 should be low so as to disable the $\overline{IRQ}$ pin. This is done so as to avoid future interrupts until after another Write timer operation.

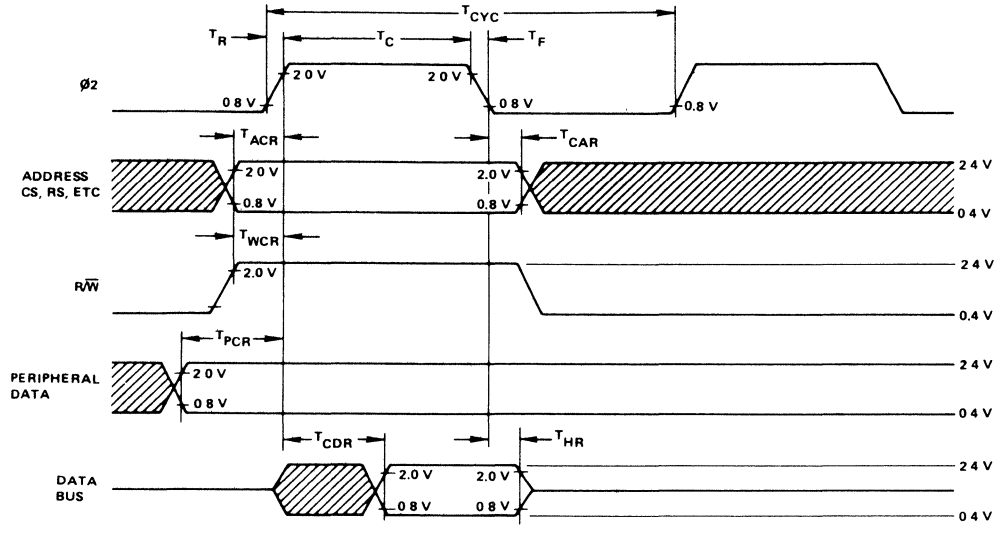


Notes:
Assume 52 Loaded into Timer with a divide by 8.
The Counter Contents and the Clock Pulse Numbers will coincide.
Prescale, P = 8.
Cycle Time, T_C = 1 μsec (for 1 MHz)
Count, N = 52

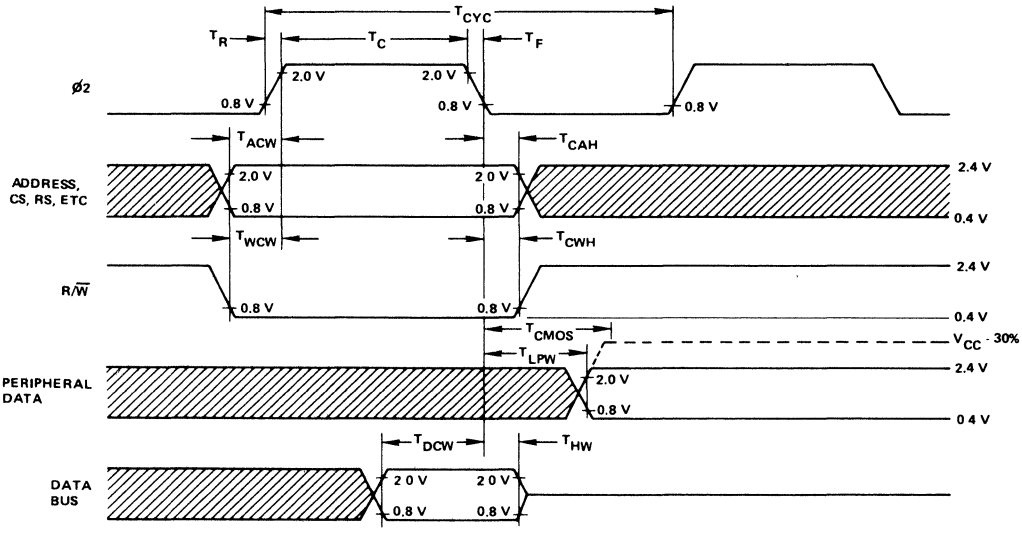
Interval Time Example Waveforms

BUS AND PERIPHERAL TIMING WAVEFORMS

READ TIMING



WRITE TIMING



AC CHARACTERISTICS

Characteristic	Symbol	R6532 (1 MHz) Min	R6532 (1 MHz) Max	R6532A (2 MHz) Min	R6532A (2 MHz) Max	Unit
Clock Cycle Time	T_{CYC}	1	10	0.5	10	μs
Clock Pulse Width	T_C	470	—	240	—	ns
Rise & Fall Times	T_R, T_F	—	25	—	15	ns

READ TIMING

Address Set Up Time	T_{ACR}	180	—	90	—	ns
Address Hold Time	T_{CAR}	0	—	0	—	ns
R/$\overline{W}$ Set Up Time	T_{WCR}	180	—	90	—	ns
Data Bus Delay Time	T_{CDR}	—	395	—	190	ns
Data Bus Hold Time	T_{HR}	10	—	10	—	ns
Peripheral Data Set Up Time	T_{PCR}	300	—	150	—	ns

WRITE TIMING

Ø2 Cycle Time	T_{CYC}	1	10	0.5	10	μs
Ø2 Pulse Width	T_C	470	—	240	—	ns
Address Set Up Time	T_{ACW}	180	—	90	—	ns
Address Hold Time	T_{CAH}	0	—	0	—	ns
R/$\overline{W}$ Set Up Time	T_{WCW}	180	—	90	—	ns
R/$\overline{W}$ Hold Time	T_{CWH}	0	—	0	—	ns
Data Bus Set-Up Time	T_{DCW}	200	—	90	—	ns
Data Bus Hold Time	T_{HW}	10	—	10	—	ns
Peripheral Data Delay Time	T_{CPW}	—	1	—	0.5	μs
Peripheral Data Delay Time CMOS	T_{CMOS}	—	2	—	1	μs

MAXIMUM RATINGS*

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to +7.0	Vdc
Input Voltage	V_{IN}	−0.3 to +7.0	Vdc
Operating Temperature Commercial Industrial	T_A	 0 to +70 −40 to +85	 °C °C
Storage Temperature	T_{STG}	−55 to +150	°C

***NOTE:** Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the other sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

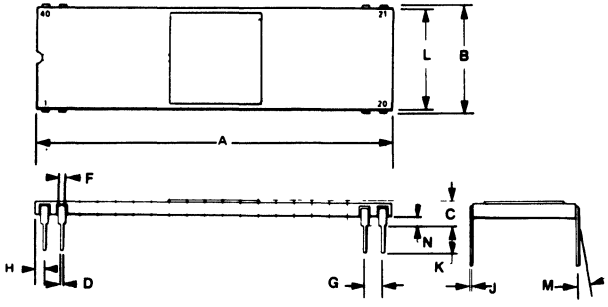
(V_{CC} = 5.0 ±5%, T_A = T_L to T_H unless otherwise noted)

Parameter	Symbol	Min	Max	Unit(1)	Test Conditions
Input High Voltage	V_{IH}	2.4	V_{CC}	V	
Input Low Voltage	V_{IL}	0	0.4	V	
Input Leakage Current: A0-A6, RS, R/$\overline{W}$, $\overline{RES}$, Ø2, CS1,$\overline{CS2}$	I_{IN}	—	2.5	µA	V_{IN} = 0V to 5.0V V_{CC} = 0V
Input Leakage Current for Three-State Off D0-D7	I_{TSI}	—	±10	µA	V_{IN} = 0.4V to 2.4V
Input High Current PA0-PA7, PB0-PB7	I_{IH}	−100	—	µA	V_{IH} = 2.4V
Input Low Current PA0-PA7, PB0-PB7	I_{IL}	—	−1 6	mA	V_{IN} = 0.4V
Output High Voltage PA0-PA7, PB0-PB7 (TTL drive), D0-D7 PB0-PB7 (other than TTL drive, e.g., Darlington)	V_{OH}	 2.4 1.5	 — —	V	V_{CC} = 4.75V I_{LOAD} = −100 µA I_{LOAD} = 3 mA
Output Low Voltage D0-D7	V_{OL}	 —	 0.4	V	V_{CC} = 4.75V I_{LOAD} = 1.6 mA
Output High Current (Sourcing) PA0-PA7, PB0-PB7 (TTL drive), D0-D7 PB0-PB7 (other drive, e.g., Darlington)	I_{OH}	 −100 −3.0	 —	 µA mA	 V_{OH} = 2.4V V_{OH} = 1.5V
Output Low Current (Sinking) PA0-PA7, PB0-PB7	I_{OL}	1.6	—	mA	V_{OL} = 0.4V
Input Capacitance Ø2 Other	 C_{CLK} C_{IN}	 — —	 30 10	 pF pF	V_{CC} = 5.0V V_{IN} = 0V f = 1 MHz T_A = 25°C
Other Capacitance	C_{OUT}	—	10	pF	
Power Dissipation	P_D	—	1000	mW	T_A = 0°C

Notes:
1. All units are direct current (DC).
2. Negative sign indicates outward current flow, positive indicates inward flow.

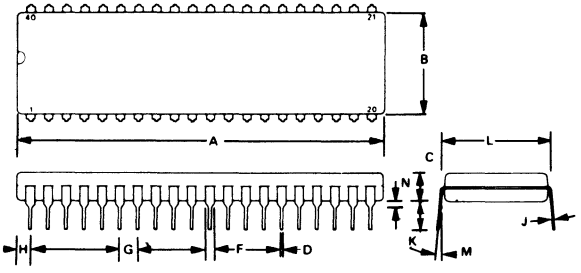
PACKAGE DIMENSIONS

40-PIN CERAMIC DIP



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	50.29	51.31	1 980	2 020
B	14.86	15.62	0.585	0.615
C	2.54	4.19	0 100	0.165
D	0 38	0 53	0.015	0.021
F	0 76	1 40	0.030	0 055
G	2 54 BSC		0 100 BSC	
H	0 76	1 78	0 030	0 070
J	0 20	0 33	0 008	0 013
K	2 54	4 19	0.100	0 165
L	14 60	15 37	0 575	0 605
M	0°	10°	0°	10°
N	0 51	1 52	0 020	0 060

40-PIN PLASTIC DIP



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	51 28	52 32	2 040	2 060
B	13 72	14 22	0 540	0 560
C	3 55	5 08	0 140	0 200
D	0 36	0 51	0 014	0 020
F	1 02	1 52	0 040	0 060
G	2 54 BSC		0 100 BSC	
H	1 65	2 16	0 065	0 085
J	0 20	0 30	0 008	0 012
K	3 05	3 56	0 120	0 140
L	15 24 BSC		0 600 BSC	
M	7°	10°	7°	10°
N	0 51	1 02	0 020	0 040

Rockwell

R6541Q, R6500/41, R6500/42 & R6500/43 ONE-CHIP INTELLIGENT PERIPHERAL CONTROLLER

INTRODUCTION

The Rockwell R6541Q, R6500/41, R6500/42 and R6500/43 One-Chip Intelligent Peripheral Controllers (IPC) are general purpose, programmable interface I/O devices designed for use with a variety of 8-bit and 16-bit microprocessor systems.

NOTE

This document describes four Intelligent Peripheral Controller devices. In the text, the terms IPC or device will be used when describing all parts. The few differences will be described in the text using the terms R6541Q, R6500/41, R6500/42, or R6500/43.

The one-chip R6500/41 IPC has an enhanced R6502 CPU, 1.5K by 8-bit ROM, 64 by 8-bit RAM, three I/O ports with multiplexed special functions, and a multi-function timer all contained within a 40 pin package.

For systems requiring additional I/O ports, the device is also available in a 64-pin QUIP version, R6500/42, that provides three additional 8-bit ports.

Another 64 pin QUIP version, R6500/43, is functionally equivalent to the R6500/41 except 4K addresses and a data bus are provided on pins, and the ROM size is optionally 256 or 0 bytes.

The R6541Q, also a 64 pin QUIP version, is functionally identical to the R6500/43 except it has no options. The part has no ROM and no port pull-up resistors. It can be used as an IPC microprocessor or as an emulator for the family.

In all versions, special interface registers allow these IPC devices to function as peripheral controllers for the 6500, 6800, Z80, 8080, and other 8-bit or 16-bit host microcomputer systems. The innovative architecture and the demonstrated high performance of the R6502 CPU, as well as the instruction simplicity results in system cost-effectiveness and a wide range of computational power. These features make the device a leading candidate for IPC computer applications.

FEATURES

- Directly compatible with 6500, 6800, 8080, and Z80 bus families
- Asynchronous Host interface that allows independent clock operation
- Input, Output and Status Registers for CPU/Host data transfers
- Interrupt or polled data interchange with Host
- Enhanced 6502 CPU
  - —Four new bit manipulation instructions:
    - Set Memory Bit (SMB)
    - Reset Memory Bit (RMB)
    - Branch on Bit Set (BBS)
    - Branch on Bit Reset (BBR)
  - —Decimal and binary arithmetic modes
  - —13 addressing modes
  - —True indexing
- 1.5K, 256 or zero bytes mask-programmable ROM
- 64-byte static RAM
- 47 TTL-compatible I/O lines (R6500/42)
- 23 TTL-compatible I/O lines (all others)
- A 16-bit programmable counter/timer, with latch
  - —Pulse width measurement
  - —Pulse generation
  - —Interval timer
  - —Event counter
- Seven interrupts
  - —Two edge-sensitive lines: one positive, one negative
  - —Reset
  - —Counter
  - —Host data received
  - —Output Data Register full
  - —Input Data Register empty
- Multiplexed bus expandable to 4K bytes of external memory
- Unmultiplexed bus for Peripheral I/O expansion
- 68% of the instructions are executed in less than 2μs at 2 MHz
- NMOS-3 silicon gate, depletion load technology
- Single +5V power supply
- 40-pin DIP (R6500/41)
- 64-pin QUIP (all others)

Document No. 29000D95

Data Sheet Order No. D95
Rev. 1, February 1983

Rockwell supports development of the R6500/41, R6500/42, and R6500/43 with the System 65 Microcomputer development System and the R6500/* Family of Personality Modules. Complete in-circuit emulation with the R6500/* Family of Personality Modules allows total system test and evaluation.

This document is for the reader familiar with the R6502 CPU hardware and programming capabilities. A detailed description of the R6502 CPU hardware is included in the R6500 Microcomputer System Hardware Manual (Order Number 201). A description of the instruction capabilities of the R6502 CPU is contained in the R6500 Microcomputer System Programming Manual (Order Number 202).

Additional information on the devices can be obtained from the R6500/41 and R6500/42 Product Description (Order Number 2135) and the R6500/43 and R6541Q Product Description (Order Number 2136).

MASK OPTIONS

The R6500/41 provides for internal pull-up resistors on PA and PC ports as a mask option. This option is available for port groups only, not for individual port lines.

The R6500/42 has provision for pull-up resistors on PA, PC, PF, and PG ports as a mask option. This option is available for port groups only, not for individual port lines.

The R6500/43 allows for 256 Bytes of ROM or no ROM, the Reset vector at FFFC or 0FFC, and pull-up resistors on PA and PC ports as independent mask options. The port resistor options are available for port groups only, not for individual port lines.

The R6541Q has no options. It is configured with no ROM, Reset vector at FFFC, and no pull-up resistors.

FUNCTIONAL DESCRIPTION

The internal CPU or the device is a standard R6502 configuration with the standard R6502 instructions, plus four new bit manipulation instructions. These new bit manipulator instructions form an enhanced R6502 instruction set and improve memory utilization efficiency and performance.

Set Memory Bit (SMB #,ADDR.)

This instruction sets to "1" one bit of the 8-bit data field specified by the zero page address (memory or I/O port). The first byte of the instruction specifies the SMB operation and which one of the eight bits to set. The second byte of the instruction designates the address (0-255) of the byte or the I/O port to be operated on.

Reset Memory Bit (RMB #,ADDR.)

This instruction has the same operation and format as the SMB instruction except that a reset to "0" results.

Branch on Bit Set Relative (BBS #,ADDR.,DEST)

This instruction tests one of the eight bits designated by a 3-bit immediate field within the first byte of the instruction. The second byte designates the location of the byte or I/O port to be tested within the zero page address range. The third byte of the instruction specifies the 8-bit relative address that the instruction will branch to if the tested bit is a "1". If the bit tested is not set, the next sequential instruction is executed.

Branch on Bit Reset Relative (BBR #,ADDR.,DEST)

This instruction has the same operation and format as the BBS instruction except that a branch occurs if the bit tested is a "0".

Read Only Memory (ROM)

The ROM consists of 1536 bytes of mask programmable memory with an address space from FA00 to FFFF for the R6500/41 and R6500/42. The R6500/43 has an optional 256 bytes of ROM at address space 0F00 to 0FFF. The R6541Q has no ROM.

Random Access Memory (RAM)

The RAM consists of 64 bytes of read/write memory with an assigned page zero address of 0040 through 007F.

System Clock

The device functions with an external clock. It is fully asynchronous in reference to the Host computer timing. The device clock frequency equals the external clock frequency. It is also made available for any external device synchronization at pin Ø2.

Parallel Input/Output Ports

All of the devices except the R6500/42 have 23 I/O lines grouped into three ports (PA, PB, PC). Ports A and C may be used either for input or output individually or in groups of any combination. Port B may be used as all inputs or all outputs.

Port A (PA)

Port A can be programmed as a standard parallel 8-bit I/O port or, under software control, as a counter I/O line or positive and negative edge detects.

Port B (PB)

Port B can be programmed as an I/O port.

Port C (PC)

Port C has seven pins and can be programmed as an I/O port.

Ports E, F, and G (PE, PF, & PG) R6500/42 only

The R6500/42 has all of the above ports A, B, and C, plus three extra ports (PE, PF, PG). Port E is outputs only. Ports F and G are bidirectional in any combination.

Host Computer Interface

The device will work with a variety of Host Computers. The HOST interface consists of a chip select, one address line, two control lines, and an 8-bit 3-state data bus. Internal logic (controlled by MCR4) configures the address and two control lines to either a 6500 or 8080 operational methodology. The interface is completely asynchronous and will work with a Host Computer up to a 5 MHz bus transfer rate. The device clock input frequency need not be the same as the Host's. A mode control register is set to match the interface to that of the Host device as follows:

The device has an 8-bit Input Data Register (IDR) and an 8-bit Output Data Register (ODR). The IDR serves as a temporary storage for commands and data from the Host to the device.

The ODR serves as a temporary storage for data from the device to the Host.

A Host Status Flag Register facilitates a software protocol that permits independent and uninterrupted flow of data asynchronously between the Host Computer and the device.

The Host Status Flag Register contains eight flag bits that can be read at any time by either the Host or the device.

Counter/Latch Logic

The device contains a 16-bit counter and a 16-bit latch associated with it. The counter can be independently programmed to operate in one of four modes:

Counter

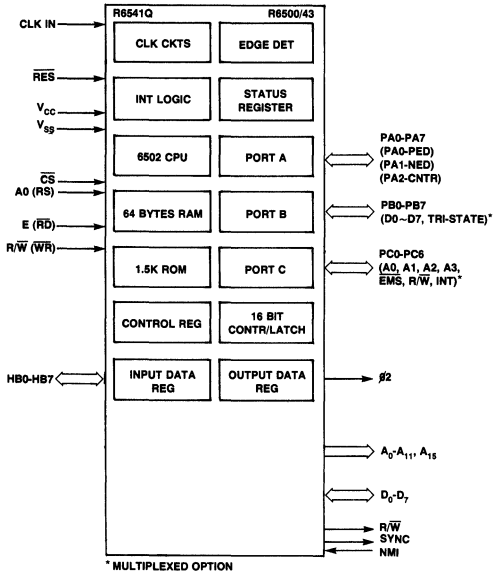
- Pulse width measurement
- Pulse Generation
- Interval Timer
- Event Counter

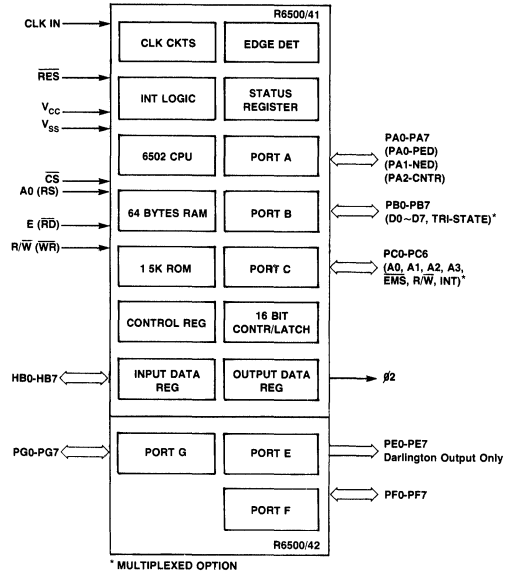
Mode Control Register (MCR)

The Mode Control Register contains control bits for the multifunction I/O ports, mode select bits for the Counter, and a selection bit for the type of Host interface.

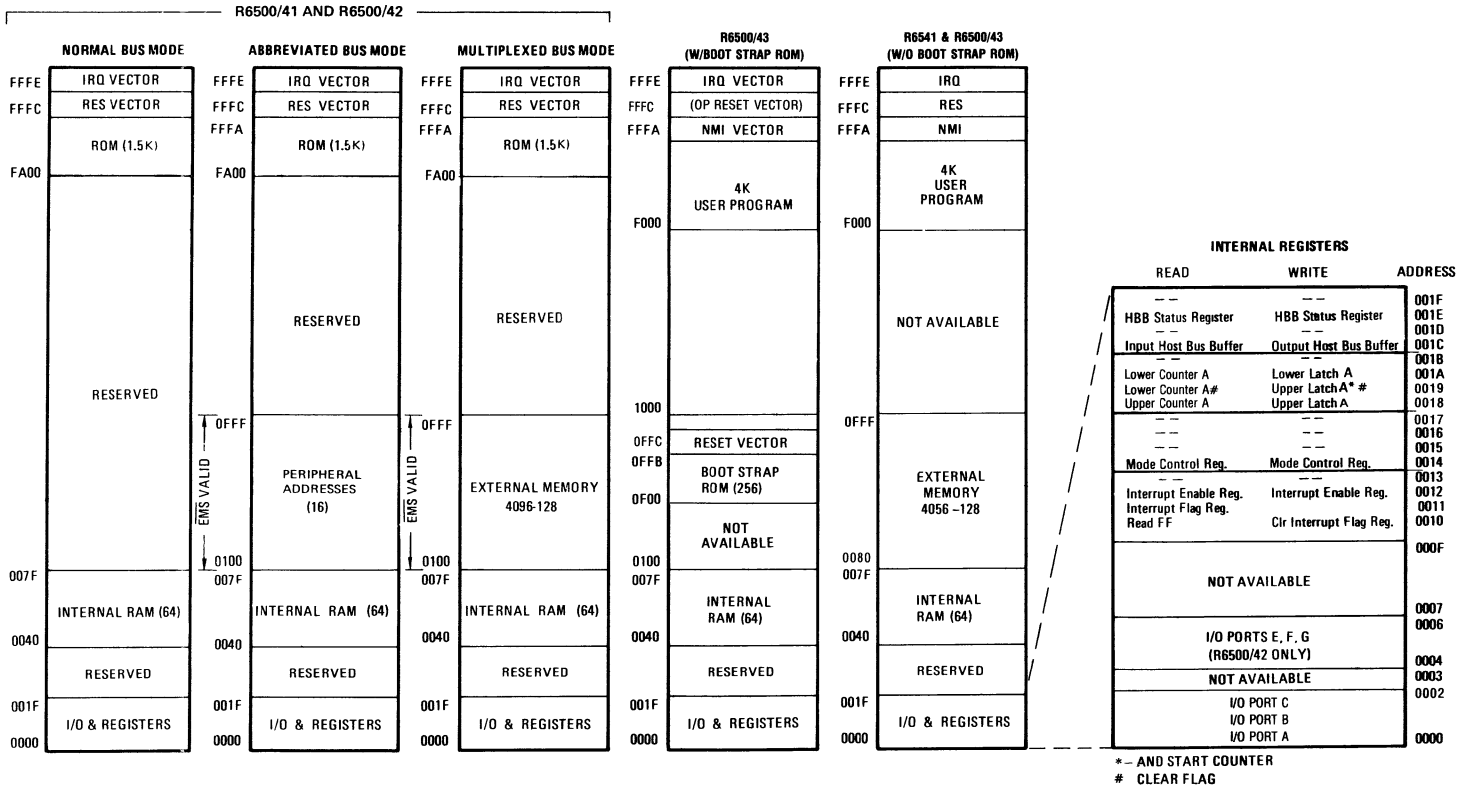
Interrupt Flag Register (IFR) and Interrupt Enable Register (IER)

The device includes an Interrupt Flag Register and an Interrupt Enable Register which flags and controls I/O and counter status.



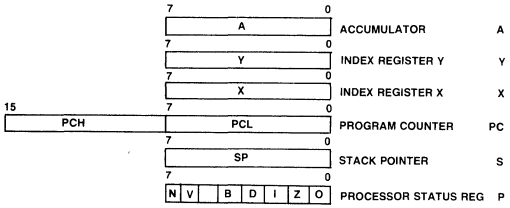


MEMORY MAP

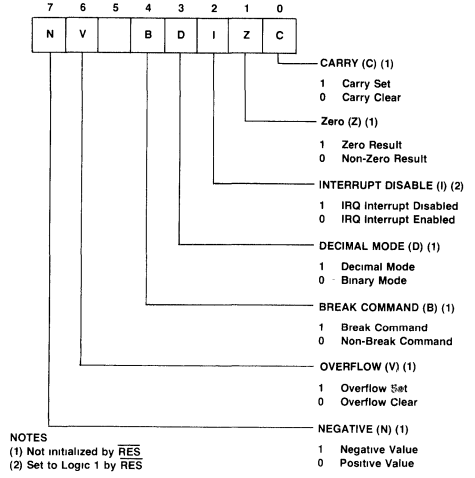

R6500/41 AND R6500/42
NORMAL BUS MODE
ABBREVIATED BUS MODE
MULTIPLEXED BUS MODE
R6500/43 (W/BOOT STRAP ROM)
R6541 & R6500/43 (W/O BOOT STRAP ROM)
FFFE
FFFC
FFFA
FA00
0FFF
0100
007F
0040
001F
0000
F000
1000
0FFC
0FFB
0F00
0080
IRQ VECTOR
RES VECTOR
ROM (1.5K)
RESERVED
EMS VALID
INTERNAL RAM (64)
I/O & REGISTERS
PERIPHERAL ADDRESSES (16)
EXTERNAL MEMORY 4096-128
(OP RESET VECTOR)
NMI VECTOR
4K USER PROGRAM
RESET VECTOR
BOOT STRAP ROM (256)
NOT AVAILABLE
IRQ
RES
NMI
EXTERNAL MEMORY 4056 –128
INTERNAL REGISTERS
READ
WRITE
ADDRESS
HBB Status Register
Input Host Bus Buffer
Output Host Bus Buffer
Lower Counter A
Lower Counter A#
Upper Counter A
Lower Latch A
Upper Latch A* #
Upper Latch A
Mode Control Reg.
Interrupt Enable Reg.
Interrupt Flag Reg.
Read FF
Clr Interrupt Flag Reg.
I/O PORTS E, F, G (R6500/42 ONLY)
I/O PORT C
I/O PORT B
I/O PORT A
*– AND START COUNTER
CLEAR FLAG

KEY REGISTER SUMMARY

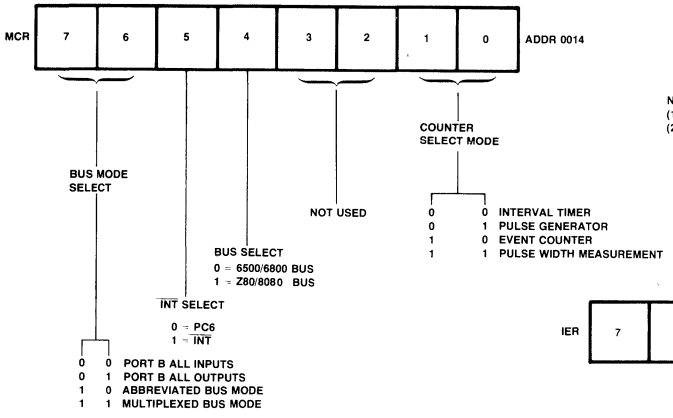
CPU Registers



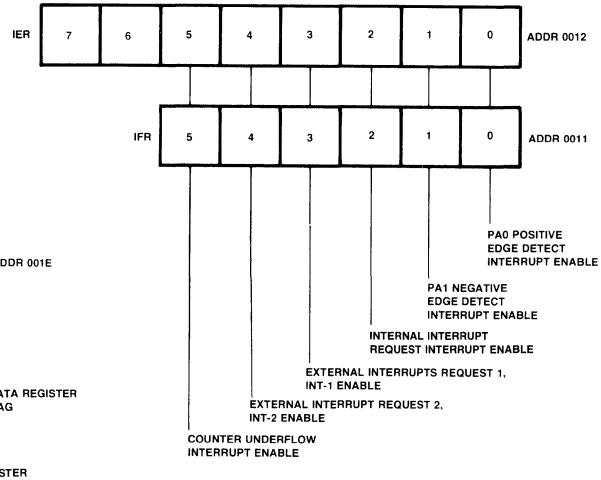
Processor Status Register



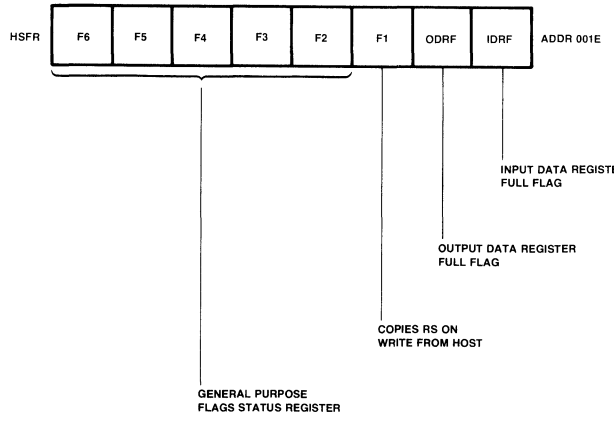
Mode Control Register



Interrupt Enable and Flag Registers



Host Status Flag Register



Host Addressing Matrix

RS (A_0)	READ	WRITE
1	HOST STATUS FLAG	COMMAND INPUT
0	DATA REG INPUT	DATA REG OUTPUT

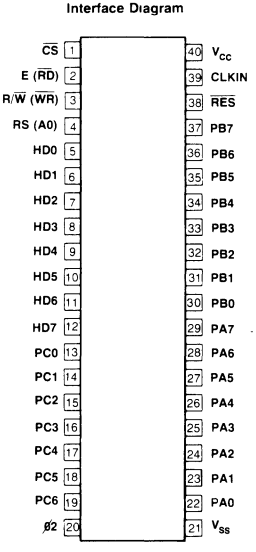


FIGURE 2-2. R6500/41 Pin Out Designation (40 PIN DIP)

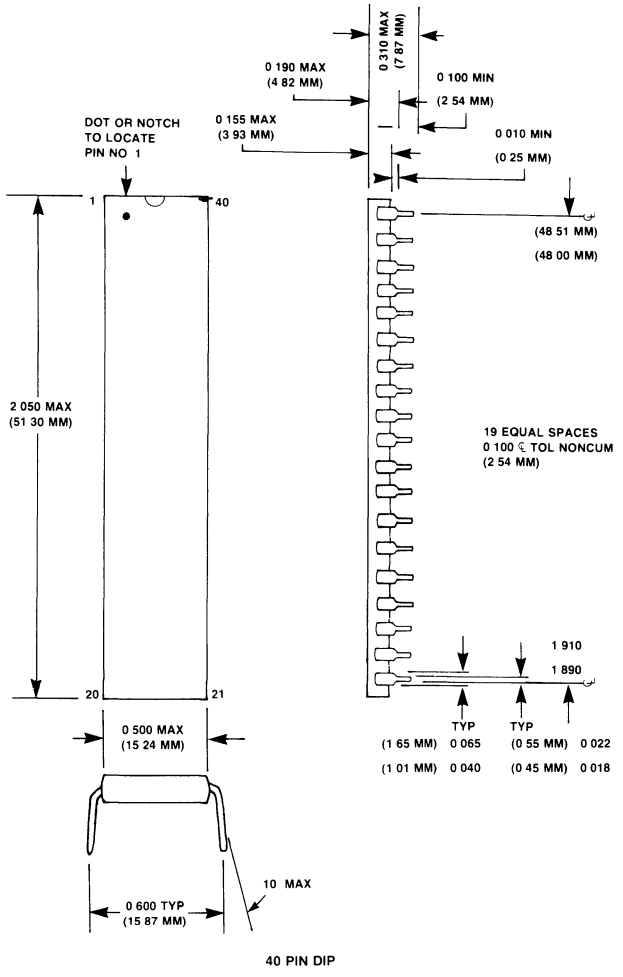


FIGURE 2-3. R6500/41 Dimensional Outline

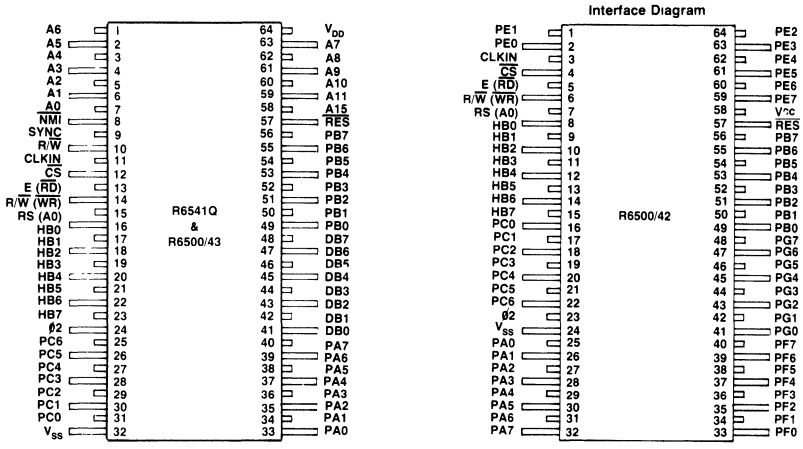


FIGURE 2-4. R6541Q, R6500/42 & R6500/43 Pin Out Designations (64 PIN QUIP)

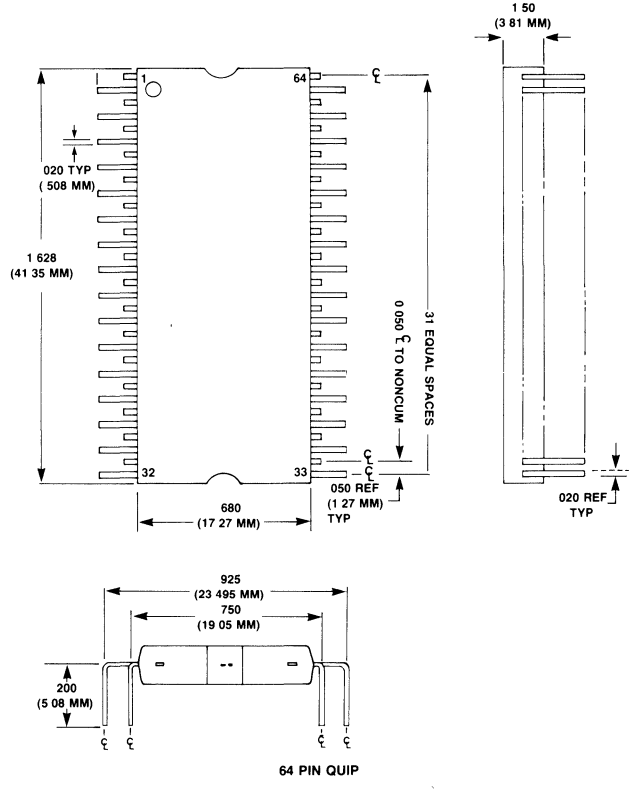


FIGURE 2-5. 64 PIN QUIP Dimensional Outline

ELECTRICAL SPECIFICATIONS

Maximum Ratings

RATING	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	-0.3 to +7.0	Vdc
Input Voltage	V_{in}	-0.3 to +7.0	Vdc
Operating Temperature Range, Commercial	T	0 to +70	°C
Storage Temperature Range	T_{stg}	65 to 150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages, however it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this circuit

D.C. Characteristics (V_{CC} = 5V ± 5%, V_{SS} = 0)

CHARACTERISTIC	SYMBOL	MIN	TYP	MAX	UNITS
Power Dissipation (Outputs High) Commercial 0°C to +70 C	P_D	—	500	—	mW
Input High Voltage (Normal Operating Levels)	V_{IH}	+2.0	—	V_{CC}	Vdc
Input Low Voltage (Normal Operating Levels)	V_{IL}	0.3	—	0.8	Vdc
Input Leakage Current V_{in} = 0 to 5.25 Vdc	I_{IN}	10.0		10.0	μAdc
Input Low Current (V_{IL} = 0.4 Vdc)	I_{IL}		1.0	1.6	mAdc
Output High Voltage (V_{CC} = min, I_{Load} = -100 μAdc)	V_{OH}	2.4	—	V_{CC}	Vdc
Output High Voltage (V_{CC} = min)	V_{CMOS}	V_{CC} -30%	—	V_{CC}	Vdc
Output Low Voltage (V_{CC} = min, I_{Load} = 1.6 mAdc)	V_{OL}	—	—	0.4	Vdc
Output High Current (Sourcing) (V_{OH} = 2.4 Vdc)	I_{OH}	100	—	—	μAdc
Output Low Current (Sinking) (V_{OL} = 0.4 Vdc)	I_{OL}	1.6	—	—	mAdc
Darlington Current Drive, PE* (V_{OH} = 1.5 Vdc)	I_{OH}	1.0	—	—	mAdc
Output Low Current, PE* (V_{OL} = 0.4 Vdc)	I_{OL}	1.6	—	—	mAdc
Input Capacitance (V_{in} = 0, T_A = 25°C, f = 1.0 MHz) PA, PB, PC, PF*, PG*	C_{in}	—	—	10	pF
Output Capacitance (V_{in} = 0, T_A = 25°C, f = 1.0 MHz)	C_{OUT}	—	—	10	pF
I/O Port Resistance PA0-PA7, PC0-PC6 PF0-PF7, PG0-PG7	R_i	3.0	6.0	11.5	KΩ

NOTE: Negative sign indicates outward current flow, positive indicates inward flow V_{CC} = 5V ± 5% *R6500/42 only

Rockwell

R6545
CRT CONTROLLER (CRTC)

DESCRIPTION

The R6545 CRT Controller (CRTC) interfaces an 8-bit microprocessor to CRT raster scan video displays, and adds an advanced CRT controller to the established and expanding line of R6500, R6500/* and R65C00 microprocessor, microcomputer and peripheral device products.

The R6545 provides refresh memory addresses and character generator row addresses which allow up to 16K characters with 32 scan lines per character to be addressed. A major advantage of the R6545 is that the refresh memory may be addressed in either straight binary or by row/column.

Other functions in the R6545 include an internal cursor register which generates a cursor output when its contents are equal to the current refresh address. Programmable cursor start and end registers allow a cursor of up to the full character scan in height to be placed on any scan lines of the character. Variable cursor display blink rates are provided. A light pen strobe input allows capture of the current refresh address in an internal light pen register. The refresh address lines are configured to provide direct dynamic memory refresh.

All timing for the video refresh memory signals is derived from the character clock input. Shift register, latch, and multiplex control signals (when needed) are provided by external high-speed timing. The mode control register allows noninterlaced video display modes at 50 or 60 Hz refresh rate. The internal status register may be used to monitor the R6545 operation. The $\overline{RES}$ input allows the CRTC-generated field rate to be dynamically-synchronized with line frequency jitter.

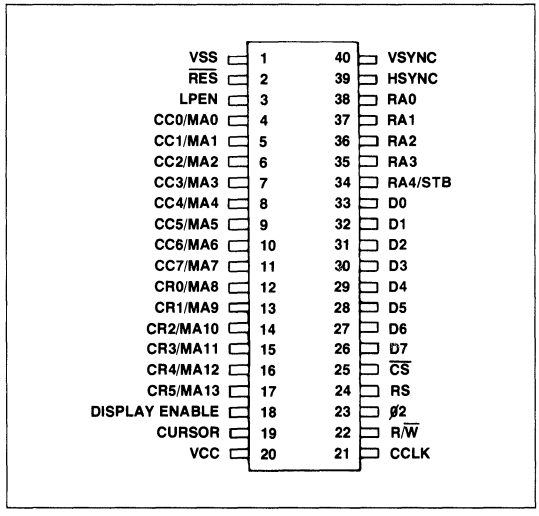
FEATURES

- Compatible with 8-bit microprocessors
- 3.7 MHz character clock operation
- Refresh RAM may be configured in row/column or straight binary addressing
- Alphanumeric and limited graphics capability
- Up and down scrolling by page, line, or character
- Programmable vertical sync width
- Fully programmable display (rows, columns, character matrix)
- Video display RAM may be configured as part of microprocessor memory field or independently slaved to R6545 (Transparent Addressing)
- Interlaced or non-interlaced scan
- 50/60 Hz operation
- Fully programmable cursor
- Light pen register
- Addresses refresh RAM to 16K characters
- No external DMA required
- Internal status register
- 40-pin ceramic or plastic DIP
- Pin-compatible with MC6845R
- Single +5 ±5% volt power supply

ORDERING INFORMATION

Part Number: R6545___

- Operating Temperature (T_L to T_H)
  - No letter = 0°C to 70°C
  - E = −40°C to 85°C
- Package
  - P = Plastic
  - C = Ceramic
- Operating Frequency
  - No Letter = 1 MHz
  - A = 2 MHz



R6545 Pin Configuration

INTERFACE SIGNAL DESCRIPTION

Figure 1 illustrates the interface between the CPU, the R6545, and the video circuitry. Figure 2 shows typical timing waveforms at the video interface.

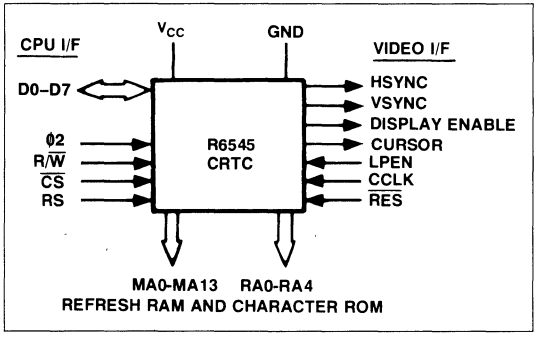


Figure 1. R6545 Interface Diagram

CPU INTERFACE

Ø2 (Phase 2 Clock)

The Phase 2 (Ø2) input clock triggers all data transfers between the system processor (CPU) and the R6545. Since there is no maximum limit to the allowable Ø2 clock time, it is not necessary for it to be a continuous clock. This capability permits the R6545 to be easily interfaced to non-6500 compatible microprocessors.

R/$\overline{W}$ (Read/Write)

The R/$\overline{W}$ input signal generated by the processor controls the direction of data transfers. A high on the R/$\overline{W}$ pin allows the processor to read the data supplied by the R6545, a low on the R/$\overline{W}$ pin allows data on data lines D0–D7 to be written into the R6545.

$\overline{CS}$ (Chip Select)

The Chip Select input is normally connected to the processor address bus either directly or through a decoder. The R6545 is selected when $\overline{CS}$ is low.

RS (Register Select)

The Register Select input allows access to internal registers. A low on this pin permits writing (R/$\overline{W}$ = low) into the Address Register and reading (R/$\overline{W}$ = high) from the Status Register. The contents of the Address Register is the identity of the register accessed when RS is high.

D0–D7 (Data Bus)

The eight data lines (D0–D7) transfer data between the processor and the R6545. These lines are bidirectional and are normally high-impedance except during read cycles when the chip is selected (CS = low).

VIDEO INTERFACE

HSYNC (Horizontal Sync)

The HSYNC active-high output signal determines the start of the horizontal raster line. It may drive a CRT monitor directly or may be used for composite video generation. HSYNC time position and width are fully programmable.

VSYNC (Vertical Sync)

The VSYNC active-high output signal determines the start of the vertical frame. Like HSYNC, VSYNC may drive a CRT monitor or composite video generation circuits. VSYNC time position and width are both programmable.

DISPLAY ENABLE (Display Enable)

The DISPLAY ENABLE active-high output signal indicates when the R6545 is generating active display information. The number of horizontal display characters per row and the number of vertical display rows are both fully programmable and together generate the DISPLAY ENABLE signal. DISPLAY ENABLE delays one character time by setting bit 4 of R8 to a 1.

CURSOR (Cursor Coincidence)

The CURSOR active-high output signal indicates when the scan coincides with the programmed cursor position. The cursor position is programmable to any character in the address field. Furthermore, within the character, the cursor may be programmed to be any block of scan lines, since the start scan line and the end scan line are both programmable. The cursor position may be delayed by one character time by setting Bit 5 of R8 to a 1.

LPEN (Light Pen Strobe)

The LPEN edge-sensitive input signal loads the internal Light Pen Register with the contents of the Refresh Scan Counter at the time the active edge occurs. The low-to-high transition activates LPEN.

CCLK (Clock)

The CCLK character timing clock input signal is the time base for all internal count/control functions.

$\overline{RES}$

The $\overline{RES}$ active-low input signal initializes all internal scan counter circuits. When $\overline{RES}$ is low, all internal counters stop and clear, all scan and video outputs go low and control registers are unaffected. $\overline{RES}$ must stay low for at least one CCLK period. All scan timing initiates when $\overline{RES}$ goes high. In this way, $\overline{RES}$ can synchronize display frame timing with line frequency. $\overline{RES}$ may also synchronize multiple CRTC's in horizontal and/or vertical split screen operation.

REFRESH RAM AND CHARACTER ROM INTERFACE

MA0–MA13 (Refresh RAM Address Lines)

These 14 active-high output signals address the refresh RAM for character storage and display operations. The starting scan address is fully programmable and the ending scan address is determined by the total number of characters displayed, which is also programmable, in terms of characters/line and lines/frame.

There are two selectable address modes for MA0–MA13:

In the straight binary mode (R8, Mode Control, bit 2 = 0), characters are stored in successive memory locations. Thus, the software design must translate row and column character coordinates into sequentially-numbered addresses for Refresh memory operations.

In the row/column mode (R8, Mode Control, bit 2 = 1), MA0–MA7 become column addresses CC0–CC7 and MA8–MA13 become row addresses CR0–CR5. In this case, the software manipulates characters in terms of row and column locations, but additional address compression circuits are needed to convert the CC0–CC7 and CR0–CR5 addresses into a memory-efficient binary address scheme.

RA0–RA4 (Raster Address Lines)

These five active-high output signals select each raster scan within an individual character row. The number of raster scan lines is programmable and determines the character height, including spaces between character rows.

The high-order line, RA4, is unique in that it can also function as a strobe output pin when the R6545 is programmed to operate in the "Transparent Address Mode." In this case the strobe is an active-high output and is true at the time the Refresh RAM update address gates on to the address lines, MA0–MA13. In this way, updates and readouts of the Refresh RAM can be made under control of the R6545 with only a small amount of external circuitry.

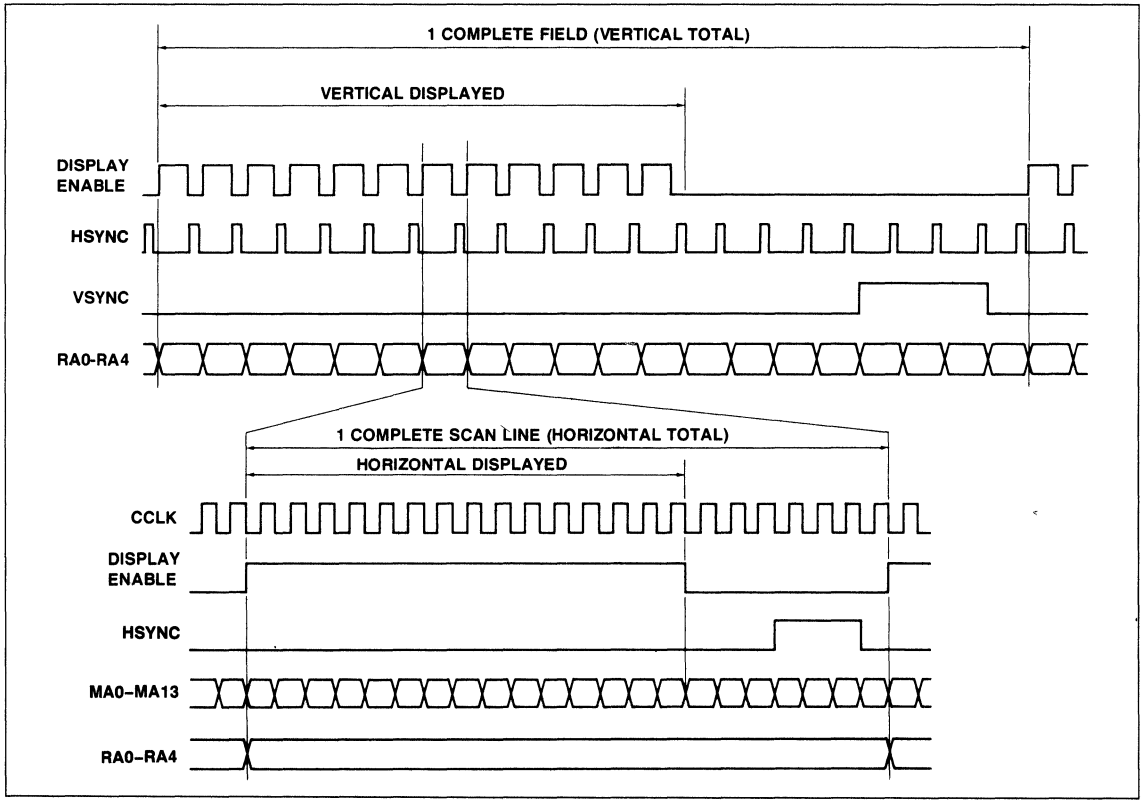


Figure 2. Vertical and Horizontal Timing

INTERNAL REGISTER DESCRIPTION

Table 1 summarizes the internal registers and indicates their address selection and read/write capabilities.

ADDRESS REGISTER

7	6	5	4	3	2	1	0
—	—	—	A_4	A_3	A_2	A_1	A_0

This 5-bit write-only register is used as a "pointer" to direct CRTC/CPU data transfers within the CRTC. It contains the number of the desired register (0–31). When RS is low, this register may be loaded; when RS is high, the selected register is the one whose identity is stored in this address register.

STATUS REGISTER (SR)

7	6	5	4	3	2	1	0
UR	LRF	VRT	—	—	—	—	—

This 3-bit register contains the status of the CRTC.

SR 7 — UR —Update Ready

0 Register R31 has been either read or written by the CPU.

1 An update strobe has occurred.

SR 6 — LRF —LPEN Register Full

0 Register R16 or R17 has been read by the CPU.

1 LPEN strobe has been received.

SR 5 — VRF —Vertical Re-Trace

0 Scan is not currently in the vertical re-trace time.

1 Scan currently in its vertical re-trace time. Note that this bit actually goes to a 1 when vertical re-trace starts, but goes to a 0 five character clock times before vertical re-trace ends to ensure that critical timings for refresh RAM operations are avoided.

SR 4–0 —Not used.

2

Table 1. Internal Register Summary

$\overline{CS}$	RS	Address Reg. 4	3	2	1	0	Reg. No.	Register Name	Stored Info.	RD	WR	Register Bit 7	6	5	4	3	2	1	0
1	—	—	—	—	—	—	—												
0	0	—	—	—	—	—	—	Address Reg	Reg No		√				A_4	A_3	A_2	A_1	A_0
0	0	—	—	—	—	—	—	Status Reg		√		U	L	V					
0	1	0	0	0	0	0	R0	Horiz Total	# Charac −1		√	●	●	●	●	●	●	●	●
0	1	0	0	0	0	1	R1	Horiz Displayed	# Charac		√	●	●	●	●	●	●	●	●
0	1	0	0	0	1	0	R2	Horiz Sync Position	# Charac		√	●	●	●	●	●	●	●	●
0	1	0	0	0	1	1	R3	VSYNC, HSYNC Widths	# Scan Lines and # Char Times		√	V_3	V_2	V_1	V_0	H_3	H_2	H_1	H_0
0	1	0	0	1	0	0	R4	Vert Total	# Charac Row −1		√		●	●	●	●	●	●	●
0	1	0	0	1	0	1	R5	Vert Total Adjust	# Scan Lines		√				‡	●	●	●	●
0	1	0	0	1	1	0	R6	Vert Displayed	# Charac Rows		√		●	●	●	●	●	●	●
0	1	0	0	1	1	1	R7	Vert Sync Position	# Charac Rows		√		●	●	●	●	●	●	●
0	1	0	1	0	0	0	R8	Mode Control			√	U_1	U_0	C	D	T	RC	I_1	I_0
0	1	0	1	0	0	1	R9	Scan Lines	# Scan Lines −1		√				●	●	●	●	●
0	1	0	1	0	1	0	R10	Cursor Start	Scan Line No		√		B_1	B_0	●	●	●	●	●
0	1	0	1	0	1	1	R11	Cursor End	Scan Line No		√				●	●	●	●	●
0	1	0	1	1	0	0	R12	Display Start Addr (H)			√				●	●	●	●	●
0	1	0	1	1	0	1	R13	Display Start Addr (L)			√	●	●	●	●	●	●	●	●
0	1	0	1	1	1	0	R14	Cursor Position (H)		√	√				●	●	●	●	●
0	1	0	1	1	1	1	R15	Cursor Position (L)		√	√	●	●	●	●	●	●	●	●
0	1	1	0	0	0	0	R16	Light Pen Reg (H)		√					●	●	●	●	●
0	1	1	0	0	0	1	R17	Light Pen Reg (L)		√		●	●	●	●	●	●	●	●
0	1	1	0	0	1	0	R18	Update Address Reg (H)			√				●	●	●	●	●
0	1	1	0	0	1	1	R19	Update Address Reg (L)			√	●	●	●	●	●	●	●	●
0	1	1	1	1	1	1	R31	Dummy Location											

Notes: ● Designates used bit in register

Designates unused bit in register Reading this bit is always 0, except for R31, which does not drive the data bus at all, and for $\overline{CS}$ = 1 which operates likewise

R0—HORIZONTAL TOTAL CHARACTERS

7	6	5	4	3	2	1	0
NUMBER OF CHARACTERS – 1							

This 8-bit write-only register contains the total of displayed and non-displayed characters, minus one, per horizontal line. This register determines the frequency of HSYNC.

R1—HORIZONTAL DISPLAYED CHARACTERS

7	6	5	4	3	2	1	0
NUMBER OF CHARACTERS							

This 8-bit write-only register contains the number of displayed characters per horizontal line.

R2—HORIZONTAL SYNC POSITION

7	6	5	4	3	2	1	0
HORIZONTAL SYNC POSITION							

This 8-bit write-only register contains the position of HSYNC on the horizontal line, in terms of the character location number on the line. The position of the HSYNC determines the left to right location of the displayed text on the video screen. In this way, the side margins are adjusted.

R3—HORIZONTAL AND VERTICAL SYNC WIDTHS

7	6	5	4	3	2	1	0
V_3	V_2	V_1	V_0	H_3	H_2	H_1	H_0

This 8-bit write-only register contains the widths of both HSYNC and VSYNC, as follows:

HVSW
7–4 VSYNC Pulse Width
The width of the vertical sync pulse (VSYNC) in the number of scan lines. When bits 4–7 are all 0, VSYNC is 16 scan lines wide.

HVSW
3–0 HSYNC Pulse Width
The width of the horizontal sync pulse (HSYNC) in the number of character clock times (CCLK).

Control of these parameters allows the R6545 to interface with a variety of CRT monitors, since the HSYNC and VSNYC timing signals may be accommodated without the use of external one shot timing.

R4—VERTICAL TOTAL ROWS

7	6	5	4	3	2	1	0
—	NO. OF CHAR. ROWS – 1						

The 7-bit Vertical Total Register contains the total number of character rows in a frame, minus one. This register, along with R5, determines the overall frame rate, which should be close to the line frequency to ensure flicker-free appearance. If the frame time is adjusted to be longer than the period of the line frequency, then $\overline{RES}$ may provide absolute synchronism.

R5—VERTICAL TOTAL LINE ADJUST

7	6	5	4	3	2	1	0
—	—	—	SCAN LINES				

The 5-bit write-only Vertical Total Line Adjust Register (R5) contains the number of additional scan lines needed to complete an entire frame scan and is intended as a fine adjustment for the video frame time.

R6—VERTICAL DISPLAYED ROWS

7	6	5	4	3	2	1	0
—	DISPLAYED CHAR. ROWS						

This 7-bit write-only register contains the number of displayed character rows in each frame. This determines the vertical size of the displayed text.

R7—VERTICAL SYNC POSITION

7	6	5	4	3	2	1	0
—	VERTICAL POSITION						

This 7-bit write-only register selects the character row time at which the vertical SYNC pulse is desired to occur and, thus, positions the displayed text in the vertical direction.

R8—MODE CONTROL (MC)

7	6	5	4	3	2	1	0
UM(T)	US(T)	CSK	DES	RRA	RAD	—	0

This 8-bit write-only register selects the operating modes of the R6545, as follows:

MC
7 UM(T)—Update/Read Mode (Transparent Mode)
0 Update occurs during horizontal and vertical blanking times with update strobe.
1 Update interleaves during Ø2 portion of cycle.

MC
6 US(T) —Update Strobe (Transparent Mode)
0 Pin 34 functions as memory address.
1 Pin 34 functions as update strobe.

MC
5 CSK —Cursor Skew
0 No delay.
1 Delays Cursor one character time.

MC
4 DES —Display Enable Skew
0 No delay.
1 Display Enable delays one character time.

MC 3	RRA —Refresh RAM Access
0	Shared memory access
1	Transparent memory access

MC 2	RAD —Refresh RAM Addressing Mode
0	Straight binary addressing
1	Row/column addressing

MC1–MC0 IMC —Interlace Mode Control

MC 1	MC 0	Operation
X	0	Non-interlace
0	1	Interlace SYNC raster scan
1	1	Interlace SYNC and video raster scan

R9—ROW SCAN LINES

7	6	5	4	3	2	1	0
—	—	—	SCAN LINES −1				

This 5-bit write-only register contains the number of scan lines, minus one, per character row, including spacing.

R10—CURSOR START LINE

7	6	5	4	3	2	1	0
—	B_1	B_0	START SCAN LINE				

R11—CURSOR END LINE

7	6	5	4	3	2	1	0
—	—	—	END SCAN LINE				

These 5-bit write-only registers select the starting and ending scan lines for the cursor. In addition, bits 5 and 6 of R10 are used to select the cursor blink mode, as follows:

B_1	B_0	Cursor Operating Mode
0	0	Display Cursor Continuously
0	1	Blank Cursor
1	0	Blink cursor at 1/16 Field Rate
1	1	Blink Cursor at 1/32 Field Rate

A one character wide cursor can be controlled by storing values into the Cursor Start Line (R10) and Cursor End Line (R11) registers and into the Cursor Position Address High (R14) and Cursor Position Low (R15) registers.

R12—DISPLAY START ADDRESS HIGH

7	6	5	4	3	2	1	0
—	—	DISPLAY START ADDRESS HIGH					

R13—DISPLAY START ADDRESS LOW

7	6	5	4	3	2	1	0
DISPLAY START ADDRESS LOW							

These registers together form a 14-bit register whose contents is the memory address of the first character of the displayed scan (the character on the top left of the video display, as in Figure 1). Subsequent memory addresses are generated by the R6545 as a result of CCLK input pulses. Scrolling of the display is accomplished by changing R12 and R13 to the memory address associated with the first character of the desired line of text to be displayed first. Entire pages of text may be scrolled or changed as well via R12 and R13.

R14—CURSOR POSITION HIGH

7	6	5	4	3	2	1	0
—	—	CURSOR POSITION HIGH					

R15—CURSOR POSITION LOW

7	6	5	4	3	2	1	0
CURSOR POSITION LOW							

These registers together form a 14-bit register whose contents is the memory address of the current cursor position. When the video display scan counter (MA lines) matches the contents of this register, and when the scan line counter (RA lines) falls within the bounds set by R10 and R11, then the CURSOR output becomes active. Bit 5 of the Mode Control Register (R8) may be used to delay the CURSOR output by a full CCLK time to accommodate slow access memories.

A cursor of up to 32 characters in height can be displayed on and between the scan lines as loaded into the Cursor Start Line (R10) and Cursor End Line (R11) Registers.

The cursor is positioned on the screen by loading the Cursor Position Address High (R14) and Cursor Position Address Low (R15) registers with the desired refresh RAM address. The cursor can be positioned in any of the 16K character positions. Hardware paging and data scrolling is thus allowed without loss of cursor position. Figure 3 is an example of the display cursor scan line.

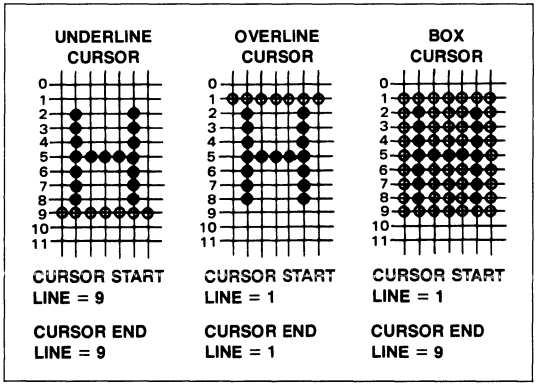


Figure 3. Cursor Display Scan Line Control Examples

R16—LIGHT PEN HIGH

7	6	5	4	3	2	1	0
—	—	LPEN HIGH					

R17—LIGHT PEN LOW

7	6	5	4	3	2	1	0
LPEN LOW							

These registers together form a 14-bit register whose contents is the light pen strobe position, in terms of the video display address at which the strobe occurred. When the LPEN input changes from low to high, then, on the next negative-going edge of CCLK, the contents of the internal scan counter is stored in registers R16 and R17.

R18—UPDATE ADDRESS HIGH

7	6	5	4	3	2	1	0
—	—	UPDATE ADDRESS HIGH					

R19—UPDATE ADDRESS LOW

7	6	5	4	3	2	1	0
UPDATE ADDRESS LOW							

These registers together comprise a 14-bit register whose contents is the memory address at which the next read or update will occur (for transparent address mode, only). Whenever a read/update occurs, the update location automatically increments to allow for fast updates or readouts of consecutive character locations. This is described elsewhere in this document. The section on REFRESH RAM ADDRESSING describes this more fully.

R31—DUMMY LOCATION

7	6	5	4	3	2	1	0
—	—	—	—	—	—	—	—

This register does not store any data, but is required to detect when transparent addressing updates occur. This is necessary to increment the Update Address Register and to set the Update Ready bit in the status register.

REGISTER FORMATS

Register pairs R12/R13, R14/R15, R16/R17, and R18/R19 are formatted in one of two ways:

(1) Straight binary, if register R8, bit 2 = 0
(2) Row/Column, if register R8, bit 2 = 1. In this case the low byte is the Character Column and the high byte is the Character Row.

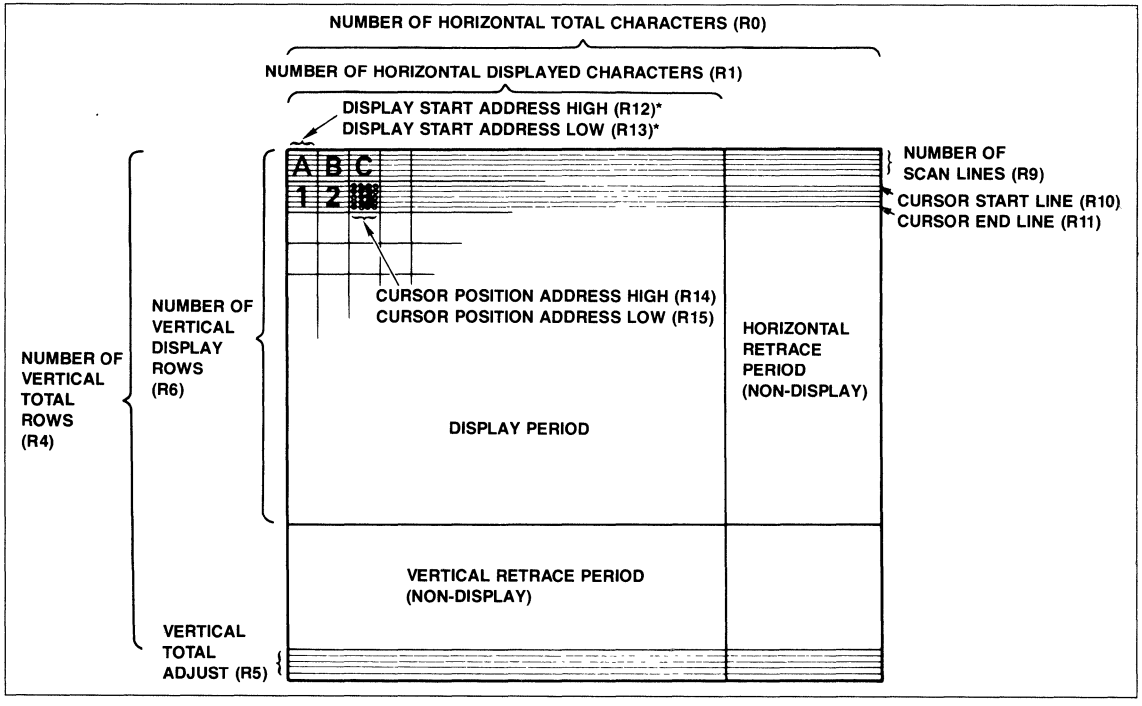


Figure 4. Video Display Format

DESCRIPTION OF OPERATION

VIDEO DISPLAY

Figure 4 indicates the relationship of the various program registers in the R6545 and the resulant video display.

Non-displayed areas of the Video Display are for horizontal and vertical retrace functions of the CRT monitor. The horizontal and vertical sync signals, HSYNC and VSYNC, are programmed to occur during these intervals and trigger the retrace in the CRT monitor. The pulse widths are constrained by the monitor requirements. The time position of the pulses may be adjusted to vary the display margins (left, right, top, and bottom).

REFRESH RAM ADDRESSING

There are two modes of addressing for the video display memory:

Shared Memory Mode (R8, BIT 3 = 0)

In this mode, the Refresh RAM address lines (MA0–MA13) directly reflect the contents of the internal refresh scan character counter. Multiplex control, to permit addressing and selection of the RAM by both the CPU and the CRTC, must be provided external to the CRTC. In the Row/Column address mode, lines MA0–MA7 become character column addresses (CC0–CC7) and MA8–MA13 become character row addresses (CR0–CR5). Figure 5 illustrates the system configuration.

Transparent Memory Addressing

For this mode, the display RAM is not directly accessible by the CPU, but is controlled entirely by the R6545. All CPU accesses are made via the R6545 and a small amount of external circuits. Figure 6 shows the system configuration for this approach.

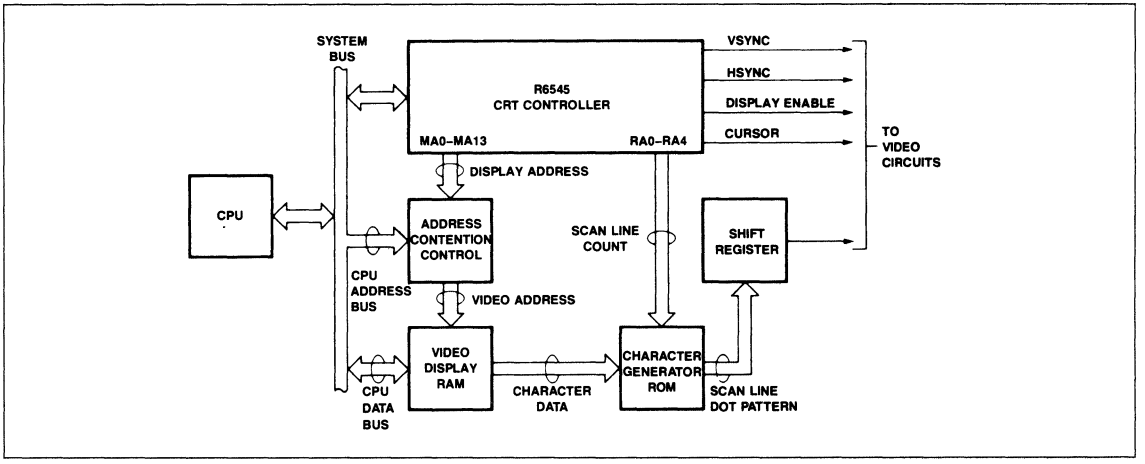


Figure 5. Shared Memory System Configuration

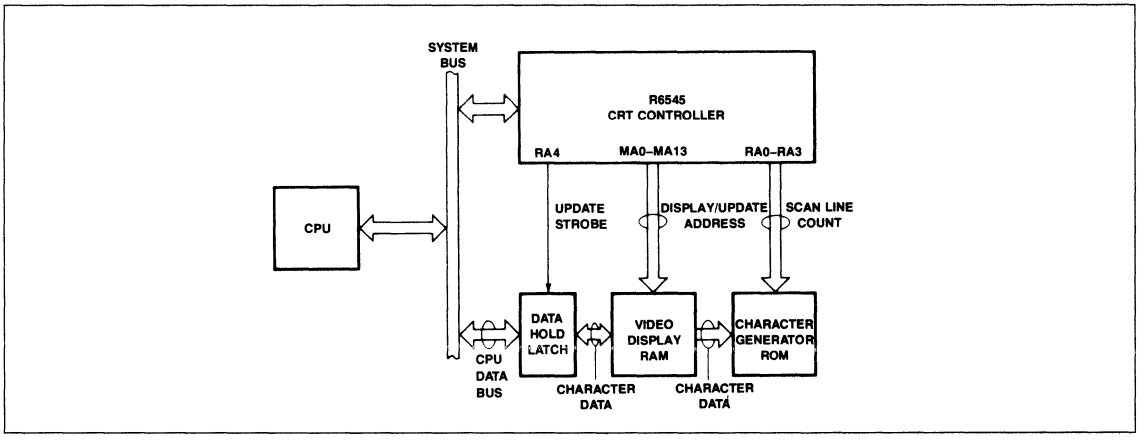


Figure 6. Transparent Memory Addressing System Configuration (Data Hold Latch Needed for Horizontal/Vertical Blanking Updates, Only).

ADDRESSING MODES

Figure 7 illustrates the address sequence for both modes of the Refresh RAM address.

Row/Column

In this mode, the CRTC address lines (MA0–MA13) generates as 8 column (MA0–MA7) and 6 row (MA8–MA13) addresses. Extra hardware is needed to compress this addressing into a straight binary sequence in order to conserve memory in the refresh RAM (register R8, bit 2 is a 1).

Binary

In this mode, the CRTC address lines are straight binary and no compression circuits are needed. However, software complexity increases since the CRT characters cannot be stored in terms of their row and column locations, but must be sequential (register R8, bit 2 is a 0).

USE OF DYNAMIC RAM FOR REFRESH MEMORY

The R6545 permits use of dynamic RAMS as storage devices for the Refresh RAM by continuing to increment memory addresses in the non-display intervals of the scan. This is a viable technique, since the Display Enable signal controls the actual video display blanking. Figure 7 illustrates Refresh RAM addressing for both row/column and binary addressing for 80 columns and 24 rows with 10 non-displayed columns and 10 non-displayed rows.

Note that the straight-binary mode has the advantage that all display memory addresses are stored in a continuous memory block, starting with address 0 and ending at 1919. The disadvantage with this method is that, if it is desired to change a displayed character location, the row and column identity of the location must be converted to its binary address before the memory may be written. The row/column mode, on the other hand, does not need to undergo this conversion. However, memory is not used as efficiently, since the memory addresses are not continuous, gaps exist. This requires that the system be equipped with more memory than actually used and this extra memory is wasted. Alternatively, address compression logic may be employed to translate the row/column format into a continuous address block.

The user selects whichever mode is best for the given application. The trade-offs between the modes are software versus hardware. Straight-binary mode minimizes hardware requirements and row/column minimizes software requirements.

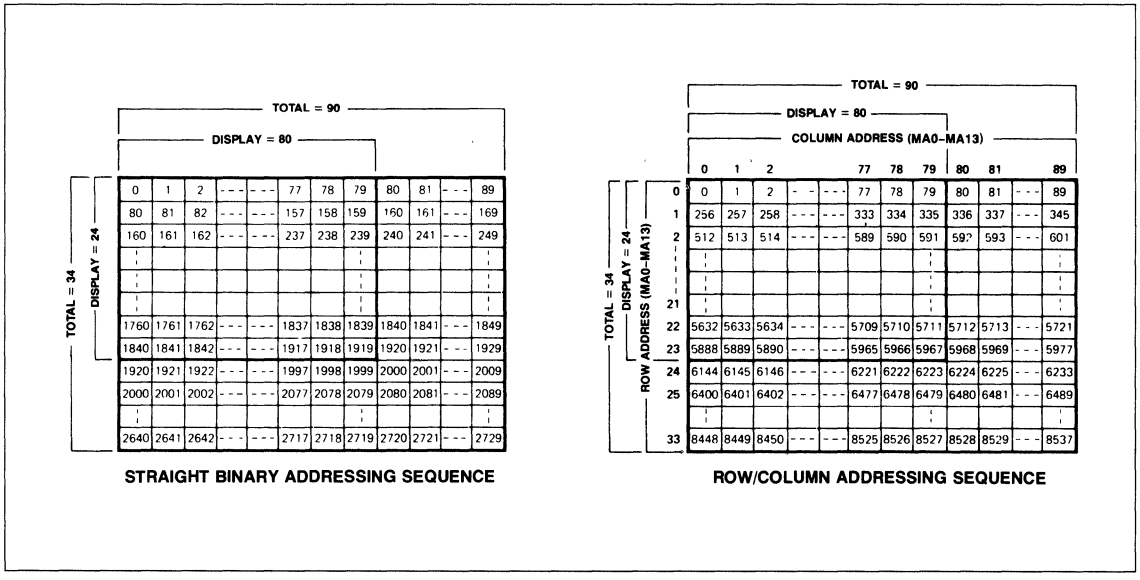


Figure 7. Display Address Sequences (with Start Address = 0) for 80 x 24 Example

MEMORY CONTENTION SCHEMES FOR SHARED MEMORY ADDRESSING

From the diagram of Figure 5, it is clear that both the R6545 and the system CPU must address the video display memory. The R6545 repetitively fetches character information to generate the video signals in order to keep the screen display active. The CPU occasionally accesses the memory to change the displayed information or to read out current data characters. Three ways of resolving this dual-contention requirement are apparent:

- **CPU Priority**

  In this technique, the address lines to the video display memory are normally driven by the R6545 unless the CPU needs access, in which case the CPU addresses immediately override those from the R6545 giving the CPU immediate access.

- **ϕ1 and ϕ2 Memory Interleaving**

  This method permits both the R6545 and the CPU access to the video display memory by time-sharing via the system ϕ1 and ϕ2 clocks. During the ϕ1 portion of each cycle (the time when ϕ2 is low), the R6545 address outputs are gated to the video display memory. In the ϕ2 time, the CPU address lines are switched in. In this way, both the R6545 and the CPU have unimpeded access to the memory. Figure 8 illustrates the timings.

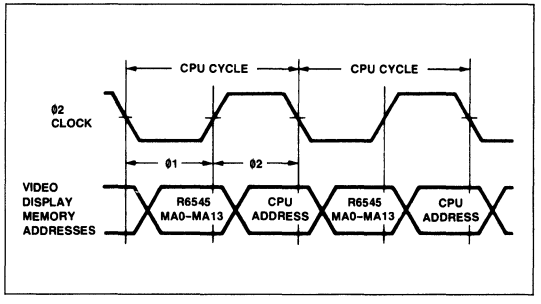


Figure 8. ϕ1 and ϕ2 Interleaving

- **Vertical Blanking**

  With this approach, the address circuitry is identical to the case for CPU Priority updates. The only difference is that the Vertical Retrace status bit (bit 5 of the Status Register) is used by the CPU so that access to the video display memory is only made during vertical blanking time (when bit 5 is a 1). In this way, no visible screen perturbations result. See Figure 10 for details.

TRANSPARENT MEMORY ADDRESSING

In this mode of operation, the video display memory address lines are not switched by contention circuits, but are generated by the R6545. In effect, the contention is handled by the R6545. As a result, the schemes for accomplishing CPU memory access are different:

- **ϕ1 and ϕ2 Interleaving**

  This mode is similar to the Interleave mode used with shared memory. In this case, however, the ϕ2 address is generated from the Update Address Register (R18 and R19) in the R6545. Thus, the CPU must first load the address to be accessed into R18/R19 and then this address is always gated onto the MA lines during ϕ2. Figure 9 shows the timing.

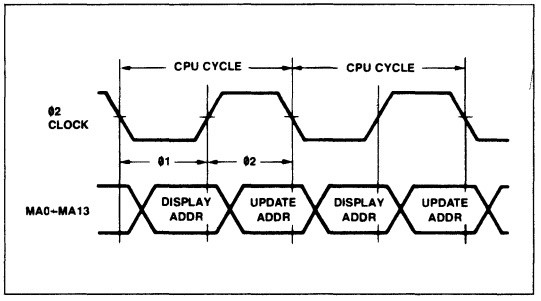


Figure 9. ϕ1 and ϕ2 Transparent Interleaving

- **Horizontal/Vertical Blanking**

  In this mode, the CPU loads the Update Address, but is only gated onto the MA lines during horizontal or vertical blank times, so memory accesses do not interfere with the display appearance. To signal when the update address is on the MA lines, an update strobe (STB) is provided as an alternate function of pin 34. Data hold latches are necessary to temporarily retain the character to be stored until the retrace time occurs. In this way, the system CPU is not halted waiting for the blanking time to arrive. Figure 11 illustrates the address and strobe timing for this mode.

CURSOR AND DISPLAY ENABLE SKEW CONTROL

Bits 4 and 5 of the Mode Control register (R8) are used to delay the Display Enable and Cursor outputs, respectively. Figure 12 illustrates the effect of the delays.

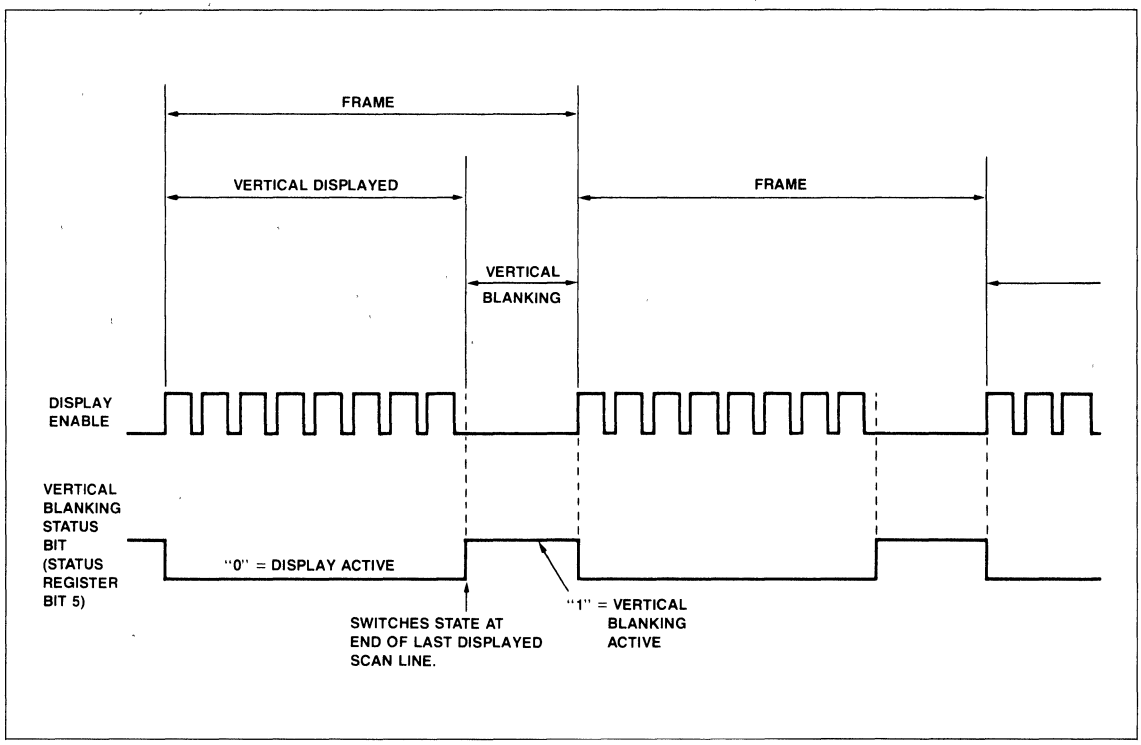


Figure 10. Operation of Vertical Blanking Status Bit

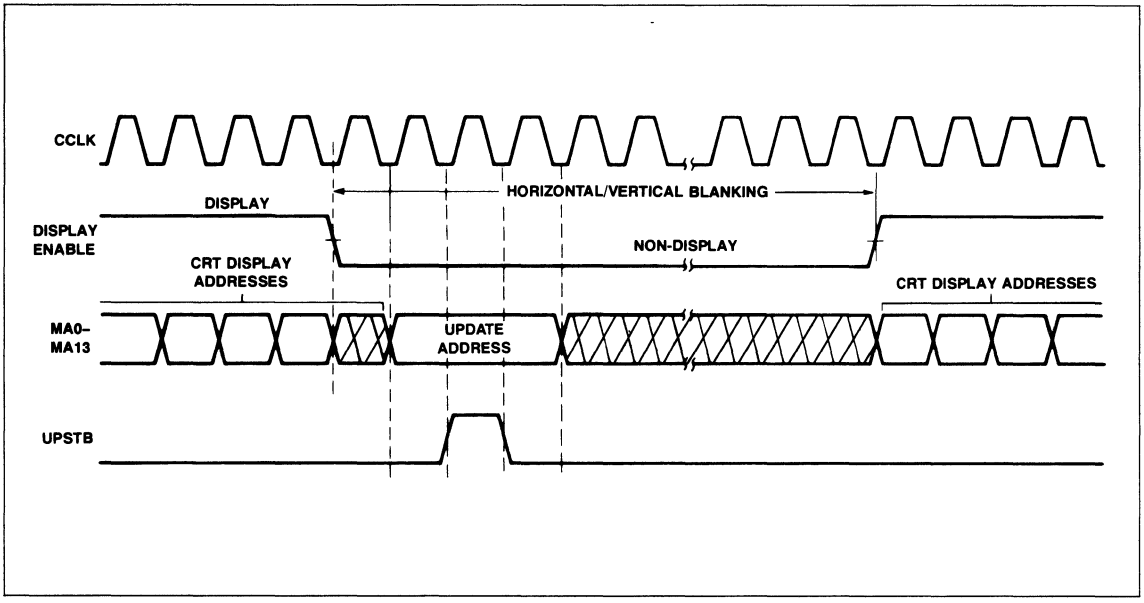


Figure 11. Retrace Update Timing

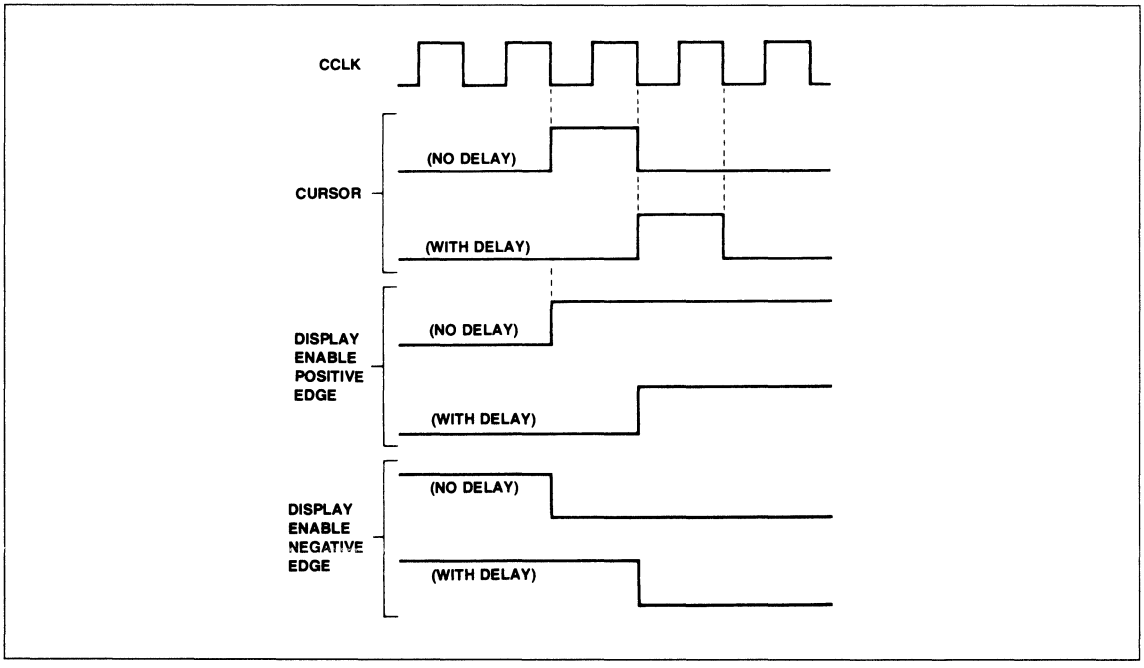


Figure 12. Cursor and Display Enable Skew

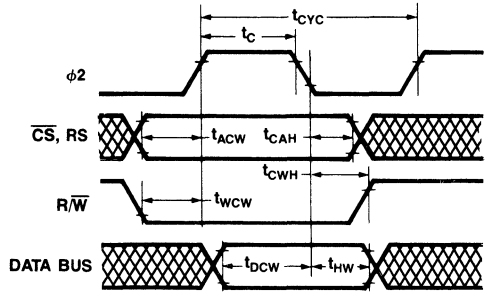
WRITE TIMING CHARACTERISTICS (V_{CC} = 5.0V ± 5%, T_A = T_L to T_H, unless otherwise noted)

Symbol	Characteristic	R6545		R6545A		Unit
		Min.	Max.	Min.	Max.	
t_{CYC}	Cycle Time	1.0	—	0 5	—	μs
t_C	ϕ2 Pulse Width	440	—	200	—	ns
t_{ACW}	Address Set-Up Time	80	—	40	—	ns
t_{CAH}	Address Hold Time	0	—	0	—	ns
t_{WCW}	R/$\overline{W}$ Set-Up Time	80	—	40	—	ns
t_{CWH}	R/$\overline{W}$ Hold Time	0	—	0	—	ns
t_{DCW}	Data Bus Set-Up Time	165	—	60	—	ns
t_{HW}	Data Bus Hold Time	10	—	10	—	ns
(t_R and t_F = 10 to 30 ns)						

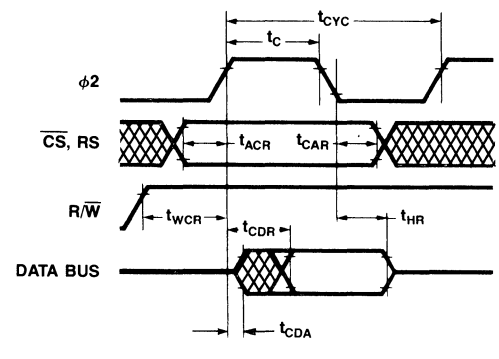
READ TIMING CHARACTERISTICS (V_{CC} = 5.0V ± 5%, T_A = T_L to T_H, unless otherwise noted)

Symbol	Characteristic	R6545		R6545A		Unit
		Min.	Max.	Min.	Max.	
t_{CYC}	Cycle Time	1.0	—	0 5	—	μs
t_C	ϕ2 Pulse Width	440	—	200	—	ns
t_{ACR}	Address Set-Up Time	80	—	40	—	ns
t_{CAR}	Address Hold Time	0	—	0	—	ns
t_{WCR}	R/$\overline{W}$ Set-Up Time	80	—	40	—	ns
t_{CDR}	Read Access Time (Valid Data)	—	290	—	150	ns
t_{HR}	Read Hold Time	10	—	10	—	ns
t_{CDA}	Data Bus Active Time (Invalid Data)	40	—	40	—	ns
(t_R and t_F = 10 to 30 ns)						

WRITE TIMING WAVEFORMS



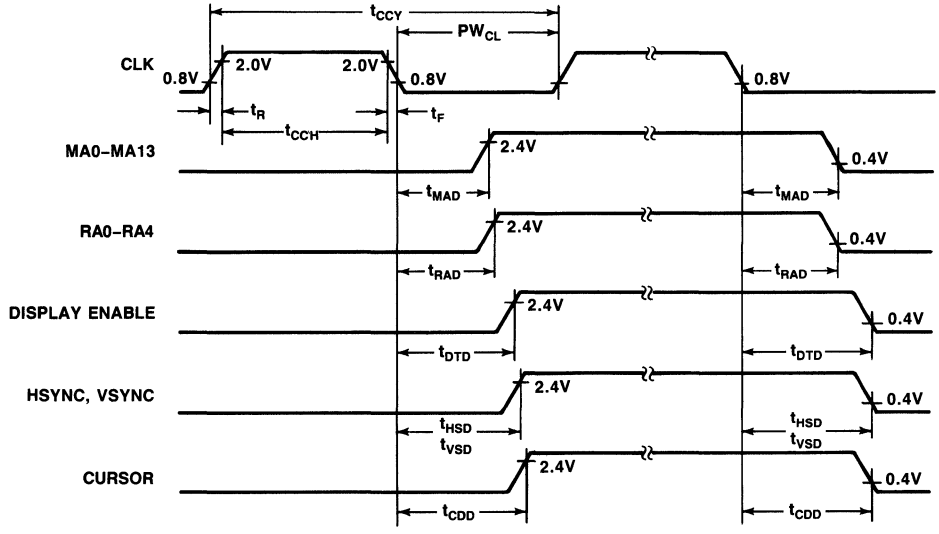
READ TIMING WAVEFORMS



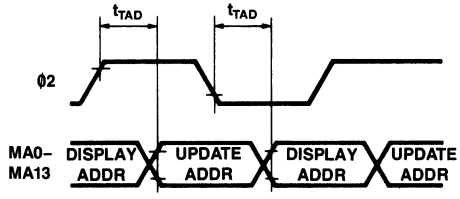
MEMORY AND VIDEO INTERFACE CHARACTERISTICS

(V_{CC} = 5.0V ± 5%, T_A = T_L to T_H, unless otherwise noted)

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{CCH}	Minimum Clock Pulse Width, High	130			ns
t_{CCV}	Clock Frequency			3.7	MHz
t_R, t_F	Rise and Fall Time for Clock Input			20	ns
t_{MAD}	Memory Address Delay Time		100	160	ns
t_{RAD}	Raster Address Delay Time		100	160	ns
t_{DTD}	Display Timing Delay Time		160	300	ns
t_{HSD}	Horizontal Sync Delay Time		160	300	ns
t_{VSD}	Vertical Sync Delay Time		160	300	ns
t_{CDD}	Cursor Display Timing Delay Time		160	300	ns



TRANSPARENT ADDRESSING WAVEFORMS (Ø1/Ø2 INTERLEAVING)

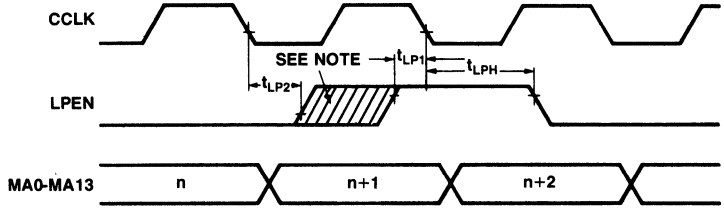


LIGHT PEN STROBE TIMING CHARACTERISTICS

Symbol	Characteristic	R6545		R6545A		Unit
		Min.	Max.	Min.	Max.	
t_{LPH}	LPEN Hold Time	100	—	100	—	ns
t_{LP1}	LPEN Setup Time	120	—	120	—	ns
t_{LP2}	CCLK to LPEN Delay	0	—	0	—	ns

Note: t_R, t_F = 20 ns (max)

LIGHT PEN STROBE TIMING WAVEFORMS



NOTE: "Safe" time position for LPEN positive edge to cause address n+2 to load into Light Pen Register.
t_{LP2} and t_{LP1} are time positions causing uncertain results.

CRTC Register Comparison

REGISTER	SY6545R	SY6845	MC6845R HD6845R	HD6845S	R6545-1 SY6545-1	R6545 SY6545E
NON-INTERLACE						
R0 HORIZONTAL TOT	TOT-1	TOT-1	TOT-1	TOT-1	TOT-1	TOT-1
R1 HORIZONAL DISP	ACTUAL	ACTUAL	ACTUAL	ACTUAL	ACTUAL	ACTUAL
R2 HORIZONTAL SYNC	ACTUAL	ACTUAL	ACTUAL	ACTUAL	ACTUAL	ACTUAL
R3 HORIZ AND VERT SYNC WIDTH	HORIZONTAL	HORIZONTAL	HORIZONTAL	HORIZONTAL AND VERTICAL	HORIZONTAL AND VERTICAL	HORIZONTAL AND VERTICAL
R4 VERTICAL TOT	TOT-1	TOT-1	TOT-1	TOT-1	TOT-1	TOT-1
R5 VERTICAL TOT ADJ	ANY VALUE	ANY VALUE	ANY VALUE	ANY VALUE	ANY VALUE EXCEPT R5 = R9H•X	ANY VALUE
R6 VERTICAL DISP	ANY VALUE <R4	ANY VALUE <R4	ANY VALUE <R4	ANY VALUE <R4	ANY VALUE <R4	ANY VALUE <R4
R7 VERTICAL SYNC POS	ACTUAL	ACTUAL	ACTUAL	ACTUAL	ACTUAL	ACTUAL
R8 MODE REG BITS 0 and 1	INTERLACE MODE SELECT	INTERLACE MODE SELECT	INTERLACE MODE SELECT	INTERLACE MODE SELECT	INTERLACE MODE SELECT	INTERLACE MODE SELECT
BITS 2	—	—	—	—	ROW/COLUMN OR STRAIGHT BINARY ADDRESSING	ROW/COLUMN OR STRAIGHT BINARY ADDRESSING
BITS 3	—	—	—	—	SHARED OR TRANSPARENT ADDR	SHARED OR TRANSPARENT ADDR
BITS 4	—	—	—	DISPEN SKEW	DISPEN SKEW	DISPEN SKEW
BITS 5	—	—	—	DISPEN SKEW	CURSOR SKEW	CURSOR SKEW
BITS 6	—	—	—	CURSOR SKEW	RA4/UPSTB	RA4/UPSTB
BITS 7	—	—	—	CURSOR SKEW	TRANSPARENT MODE SELECT	TRANSPARENT MODE SELECT
R9 SCAN LINES	TOT-1	TOT-1	TOT-1	TOT-1	TOT-1	TOT-1
R10 CURSOR START	ACTUAL	ACTUAL	ACTUAL	ACTUAL	ACTUAL	ACTUAL
R11 CURSOR END	ACTUAL	ACTUAL	ACTUAL	ACTUAL	ACTUAL	ACTUAL
R12/R13 DISP ADDR	WRITE ONLY	WRITE ONLY	WRITE ONLY	READ/WRITE	WRITE ONLY	WRITE ONLY
R14/R15 CURSOR POS	READ/WRITE	READ/WRITE	WRITE ONLY	READ/WRITE	READ/WRITE	READ/WRITE
R16/R17 LPEN REG	READ ONLY	READ ONLY	READ ONLY	READ ONLY	READ ONLY	READ ONLY
R18/R19 UPDATE ADDR REG	N/A	N/A	N/A	N/A	TRANSPARENT MODE ONLY	TRANSPARENT MODE ONLY
R31 DUMMY REG	N/A	N/A	N/A	N/A	TRANSPARENT MODE ONLY	TRANSPARENT MODE ONLY
STATUS REG	YES	NO	NO	NO	YES	YES
INTERLACE SYNC						
R0	TOT-1 = ODD OR EVEN	TOT-1 = ODD OR EVEN	TOT-1 = ODD	TOT-1 = ODD	TOT-1 = ODD	TOT-1 = ODD OR EVEN
INTERLACE SYNC AND VIDEO						
R4 VERTICAL	TOT-1	TOT-1	TOT-1	TOT-2	TOT/2-1	TOT-1
R6 VERT DISP	TOT	TOT	TOT/2	TOT	TOT/2	TOT
R7 VERT SYNC	ACTUAL	ACTUAL	ACTUAL	ACTUAL	ACTUAL/2	ACTUAL
R10 CURSOR START R11 CURSOR END	ODD/EVEN ODD/EVEN	ODD/EVEN ODD/EVEN	BOTH ODD OR BOTH EVEN	ODD/EVEN ODD/EVEN	ODD/EVEN ODD/EVEN	ODD/EVEN ODD/EVEN
CCLK	3 7 MHz	2.5 MHz	2 5 MHz	3.7 MHz	2.5 MHz	3.7 MHz

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to +7.0	Vdc
Input Voltage	V_{IN}	−0.3 to +7.0	Vdc
Operating Temperature Range Commercial Industrial	T_A	 0 to +70 −40 to +85	°C
Storage Temperature	T_{STG}	−55 to +150	°C

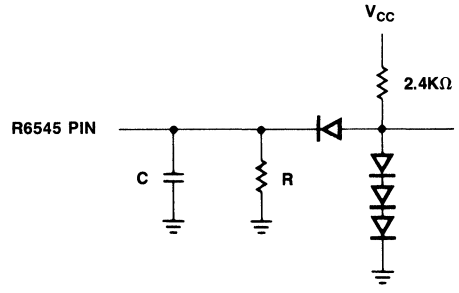
***NOTE:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

(V_{CC} = 5.0V ±5%, T_A = T_L to T_H, unless otherwise noted)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Input High Voltage	V_{IH}	2 0		V_{CC}	Vdc
Input Low Voltage	V_{IL}	−0.3		0.8	Vdc
Input Leakage (Ø2, R/$\overline{W}$, $\overline{RES}$, $\overline{CS}$, RS, LPEN, CCLK)	I_{IN}	—		2.25	μAdc
Three-State Input Leakage (D0–D7) (V_{IN} = 0.4 to 2 4V)	I_{TSI}	—		± 10.0	μAdc
Output High Voltage I_{LOAD} = 205 μAdc (D0–D7) I_{LOAD} = 100 μAdc (all others)	V_{OH}	2.4		—	Vdc
Output Low Voltage I_{LOAD} = 1.6 mAdc	V_{OL}	—		0.4	Vdc
Power Dissipation (V_{CC} = 5.25V)	P_D	—	260	525	mW
Input Capacitance Ø2, R/$\overline{W}$, $\overline{RES}$, $\overline{CS}$, RS, LPEN, CCLK D0–D7	C_{IN}	 — —		10.0 12.5	pF pF
Output Capacitance	C_{OUT}	—		10.0	pF

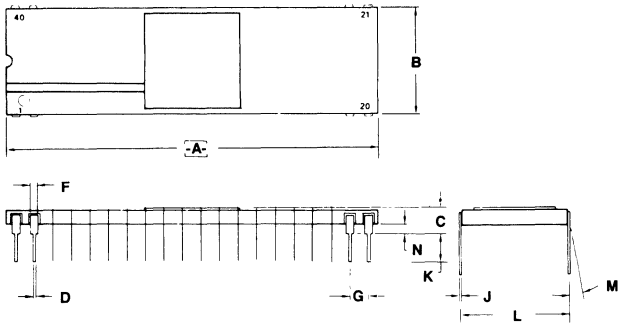
TEST LOAD



R = 11KΩ FOR D0-D7
= 24KΩ FOR ALL OTHER OUTPUTS
C = 130 pF TOTAL FOR D0-D7
= 30 pF ALL OTHER OUTPUTS

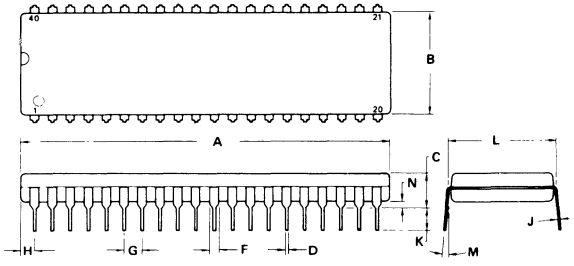
PACKAGE DIMENSIONS

40-PIN CERAMIC DIP



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	50 29	51 56	1 980	2 030
B	14 73	15 49	0 580	0 610
C	1 78	3 05	0 070	0 120
D	0 38	0 58	0 015	0 023
F	1 02	1 65	0 040	0 065
G	2 29	2 80	0 090	0 110
J	0 20	0 38	0 008	0 015
K	3 18	3 81	0 125	0 150
L	14 99	16 51	0 590	0 650
M	0°	10°	0°	10°
N	0 58	1 78	0 020	0 070

40-PIN PLASTIC DIP



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	51 28	52 32	2 040	2 060
B	13 72	14 22	0 540	0 560
C	3 55	5 08	0 140	0 200
D	0 36	0 51	0 014	0 020
F	1 02	1 52	0 040	0 060
G	2 54 BSC		0 100 BSC	
H	1 65	2 16	0 065	0 085
J	0 20	0 30	0 008	0 012
K	3 05	3 56	0 120	0 140
L	15 24 BSC		0 600 BSC	
M	7°	10°	7°	10°
N	0 51	1 02	0 020	0 040

Rockwell

R6545-1
CRT CONTROLLER (CRTC)

DESCRIPTION

The R6545-1 CRT Controller (CRTC) interfaces an 8-bit microprocessor to CRT raster scan video displays, and adds an advanced CRT controller to the established and expanding line of R6500, R6500/* and R65C00 microprocessor, microcomputer and peripheral device products.

The R6545-1 provides refresh memory addresses and character generator row addresses which allow up to 16K characters with 32 scan lines per character to be addressed. A major advantage of the R6545-1 is that the refresh memory may be addressed in either straight binary or by row/column.

Other functions in the R6545-1 include an internal cursor register which generates a cursor output when its contents are equal to the current refresh address. Programmable cursor start and end registers allow a cursor of up to the full character scan in height to be placed on any scan lines of the character. Variable cursor display blink rates are provided. A light pen strobe input allows capture of the current refresh address in an internal light pen register. The refresh address lines are configured to provide direct dynamic memory refresh.

All timing for the video refresh memory signals is derived from the character clock input. Shift register, latch, and multiplex control signals (when needed) are provided by external high-speed timing. The mode control register allows noninterlaced video display modes at 50 or 60 Hz refresh rate. The internal status register may be used to monitor the R6545-1 operation. The $\overline{RES}$ input allows the CRTC-generated field rate to be dynamically-synchronized with line frequency jitter.

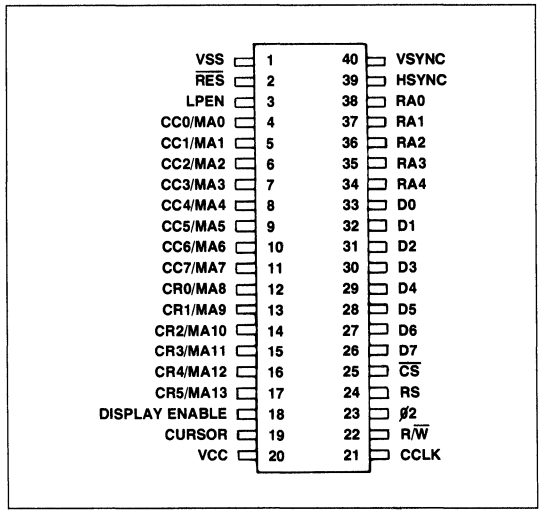
ORDERING INFORMATION

Part Number: R6545-1___

- Operating Temperature (T_L to T_H)
  - No letter = 0°C to 70°C
  - E = −40°C to 85°C
- Package
  - P = Plastic
  - C = Ceramic
- Operating Frequency
  - No Letter = 1 MHz
  - A = 2 MHz

FEATURES

- Compatible with 8-bit microprocessors
- Up to 2.5 MHz character clock operation
- Refresh RAM may be configured in row/column or straight binary addressing
- Alphanumeric and limited graphics capability
- Up and down scrolling by page, line, or character
- Programmable vertical sync width
- Fully programmable display (rows, columns, character matrix)
- Video display RAM may be configured as part of microprocessor memory field or independently slaved to R6545-1 (Transparent Addressing)
- Non-interlaced scan
- 50/60 Hz operation
- Fully programmable cursor
- Light pen register
- Addresses refresh RAM to 16K characters
- No external DMA required
- Internal status register
- 40-pin ceramic or plastic DIP
- Pin-compatible with MC6845
- Single +5 ±5% volt power supply



R6545-1 Pin Configuration

INTERFACE SIGNAL DESCRIPTION

Figure 1 illustrates the interface between the CPU, the R6545-1, and the video circuitry. Figure 2 shows typical timing waveforms at the video interface.

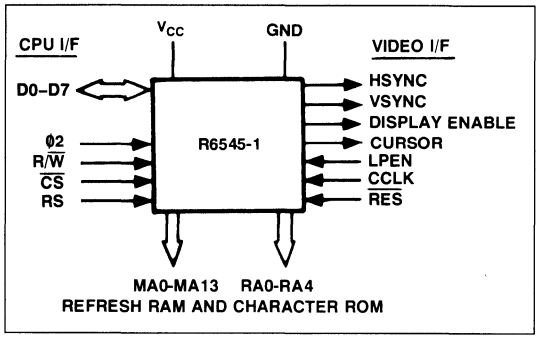


Figure 1. R6545-1 Interface Diagram

CPU INTERFACE

Ø2 (Phase 2 Clock)

The Phase 2 (Ø2) input clock triggers all data transfers between the system processor (CPU) and the R6545-1. Since there is no maximum limit to the allowable Ø2 clock time, it is not necessary for it to be a continuous clock. This capability permits the R6545-1 to be easily interfaced to non-6500 compatible microprocessors.

R/$\overline{W}$ (Read/Write)

The R/$\overline{W}$ input signal generated by the processor controls the direction of data transfers. A high on the R/$\overline{W}$ pin allows the processor to read the data supplied by the R6545-1, a low on the R/$\overline{W}$ pin allows data on data lines D0-D7 to be written into the R6545-1.

$\overline{CS}$ (Chip Select)

The Chip Select input is normally connected to the processor address bus either directly or through a decoder. The R6545-1 is selected when $\overline{CS}$ is low.

RS (Register Select)

The Register Select input allows access to internal registers. A low on this pin permits writing (R/$\overline{W}$ = low) into the Address Register and reading (R/$\overline{W}$ = high) from the Status Register. The contents of the Address Register is the identity of the register accessed when RS is high.

D0–D7 (Data Bus)

The eight data lines (D0–D7) transfer data between the processor and the R6545-1. These lines are bidirectional and are normally high-impedance except during read cycles when the chip is selected ($\overline{CS}$ = low).

VIDEO INTERFACE

HSYNC (Horizontal Sync)

The HSYNC active-high output signal determines the start of the horizontal raster line. It may drive a CRT monitor directly or may be used for composite video generation. HSYNC time position and width are fully programmable.

VSYNC (Vertical Sync)

The VSYNC active-high output signal determines the start of the vertical frame. Like HSYNC, VSYNC may drive a CRT monitor or composite video generation circuits. VSYNC time position and width are both programmable.

DISPLAY ENABLE (Display Enable)

The DISPLAY ENABLE active-high output signal indicates when the R6545-1 is generating active display information. The number of horizontal display characters per row and the number of vertical display rows are both fully programmable and together generate the DISPLAY ENABLE signal. DISPLAY ENABLE delays one character time by setting bit 4 of R8 to a 1.

CURSOR (Cursor Coincidence)

The CURSOR active-high output signal indicates when the scan coincides with the programmed cursor position. The cursor position is programmable to any character in the address field. Furthermore, within the character, the cursor may be programmed to be any block of scan lines, since the start scan line and the end scan line are both programmable. The cursor position may be delayed by one character time by setting Bit 5 of R8 to a 1.

LPEN (Light Pen Strobe)

The LPEN edge-sensitive input signal loads the internal Light Pen Register with the contents of the Refresh Scan Counter at the time the active edge occurs. The low-to-high transition activates LPEN.

CCLK (Clock)

The CCLK character timing clock input signal is the time base for all internal count/control functions.

$\overline{RES}$

The $\overline{RES}$ active-low input signal initializes all internal scan counter circuits. When $\overline{RES}$ is low, all internal counters stop and clear, all scan and video outputs go low and control registers are unaffected. $\overline{RES}$ must stay low for at least one CCLK period. All scan timing initiates when $\overline{RES}$ goes high. In this way, $\overline{RES}$ can synchronize display frame timing with line frequency. $\overline{RES}$ may also synchronize multiple CRTC's in horizontal and/or vertical split screen operation.

REFRESH RAM AND CHARACTER ROM INTERFACE

MA0–MA13 (Refresh RAM Address Lines)

These 14 active-high output signals address the refresh RAM for character storage and display operations. The starting scan address is fully programmable and the ending scan address is determined by the total number of characters displayed, which is also programmable, in terms of characters/line and lines/frame.

There are two selectable address modes for MA0–MA13:

In the straight binary mode (R8, Mode Control, bit 2 = 0), characters are stored in successive memory locations. Thus, the software design must translate row and column character coordinates into sequentially-numbered addresses for Refresh memory operations.

In the row/column mode (R8, Mode Control, bit 2 = 1), MA0–MA7 become column addresses CC0–CC7 and MA8–MA13 become row addresses CR0–CR5. In this case, the software manipulates characters in terms of row and column locations, but additional address compression circuits are needed to convert the CC0–CC7 and CR0–CR5 addresses into a memory-efficient binary address scheme.

RA0–RA4 (Raster Address Lines)

These five active-high output signals select each raster scan within an individual character row. The number of raster scan lines is programmable and determines the character height, including spaces between character rows.

The high-order line, RA4, is unique in that it can also function as a strobe output pin when the R6545-1 is programmed to operate in the "Transparent Address Mode." In this case the strobe is an active-high output and is true at the time the Refresh RAM update address gates on to the address lines, MA0–MA13. In this way, updates and readouts of the Refresh RAM can be made under control of the R6545-1 with only a small amount of external circuitry.

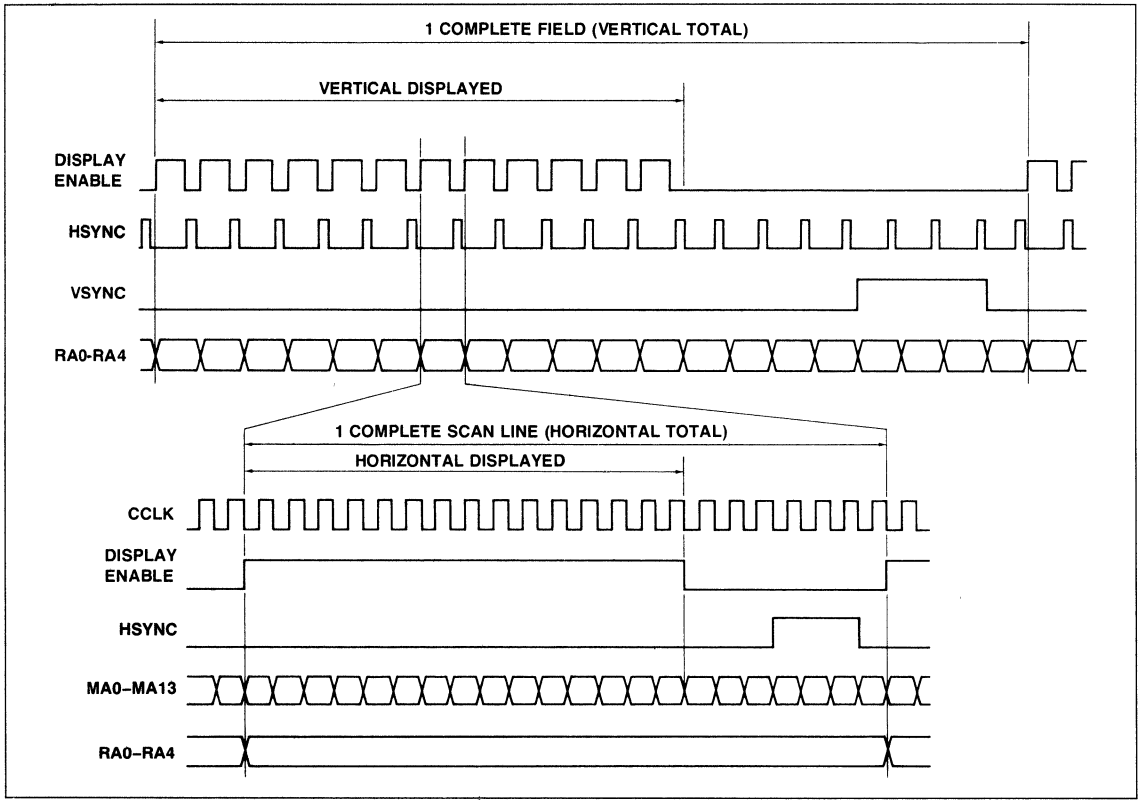


Figure 2. Vertical and Horizontal Timing

INTERNAL REGISTER DESCRIPTION

Table 1 summarizes the internal registers and indicates their address selection and read/write capabilities.

ADDRESS REGISTER

7	6	5	4	3	2	1	0
—	—	—	A_4	A_3	A_2	A_1	A_0

This 5-bit write-only register is used as a "pointer" to direct CRTC/CPU data transfers within the CRTC. It contains the number of the desired register (0–31). When RS is low, this register may be loaded; when RS is high, the selected register is the one whose identity is stored in this address register.

STATUS REGISTER (SR)

7	6	5	4	3	2	1	0
UR	LRF	VRT	—	—	—	—	—

This 3-bit register contains the status of the CRTC.

SR 7 — UR —Update Ready

0 Register R31 has been either read or written by the CPU.

1 An update strobe has occurred.

SR 6 — LRF —LPEN Register Full

0 Register R16 or R17 has been read by the CPU.

1 LPEN strobe has been received.

SR 5 — VRF —Vertical Re-Trace

0 Scan is not currently in the vertical re-trace time.

1 Scan currently in its vertical re-trace time. Note that this bit actually goes to a 1 when vertical re-trace starts, but goes to a 0 five character clock times before vertical re-trace ends to ensure that critical timings for refresh RAM operations are avoided.

SR 4–0 —Not used.

2

Table 1. Internal Register Summary

$\overline{CS}$	RS	Address Reg. 4	3	2	1	0	Reg. No.	Register Name	Stored Info.	RD	WR	Register Bit 7	6	5	4	3	2	1	0
1	—	—	—	—	—	—	—												
0	0	—	—	—	—	—	—	Address Reg	Reg No		√				A_4	A_3	A_2	A_1	A_0
0	0	—	—	—	—	—	—	Status Reg		√		U	L	V					
0	1	0	0	0	0	0	R0	Horiz Total	# Charac −1		√	•	•	•	•	•	•	•	•
0	1	0	0	0	0	1	R1	Horiz. Displayed	# Charac		√	•	•	•	•	•	•	•	•
0	1	0	0	0	1	0	R2	Horiz Sync Position	# Charac		√	•	•	•	•	•	•	•	•
0	1	0	0	0	1	1	R3	VSYNC, HSYNC Widths	# Scan Lines and # Char Times		√	V_3	V_2	V_1	V_0	H_3	H_2	H_1	H_0
0	1	0	0	1	0	0	R4	Vert Total	# Charac Row −1		√		•	•	•	•	•	•	•
0	1	0	0	1	0	1	R5	Vert Total Adjust	# Scan Lines		√			÷	•	•	•	•	•
0	1	0	0	1	1	0	R6	Vert Displayed	# Charac Rows		√		•	•	•	•	•	•	•
0	1	0	0	1	1	1	R7	Vert Sync Position	# Charac Rows		√		•	•	•	•	•	•	•
0	1	0	1	0	0	0	R8	Mode Control			√	U_1	U_0	C	D	T	RC		0
0	1	0	1	0	0	1	R9	Scan Lines	# Scan Lines −1		√				•	•	•	•	•
0	1	0	1	0	1	0	R10	Cursor Start	Scan Line No		√		B_1	B_0	•	•	•	•	•
0	1	0	1	0	1	1	R11	Cursor End	Scan Line No		√				•	•	•	•	•
0	1	0	1	1	0	0	R12	Display Start Addr (H)			√			•	•	•	•	•	•
0	1	0	1	1	0	1	R13	Display Start Addr (L)			√	•	•	•	•	•	•	•	•
0	1	0	1	1	1	0	R14	Cursor Position (H)		√	√			•	•	•	•	•	•
0	1	0	1	1	1	1	R15	Cursor Position (L)		√	√	•	•	•	•	•	•	•	•
0	1	1	0	0	0	0	R16	Light Pen Reg (H)		√				•	•	•	•	•	•
0	1	1	0	0	0	1	R17	Light Pen Reg (L)		√		•	•	•	•	•	•	•	•
0	1	1	0	0	1	0	R18	Update Address Reg (H)			√			•	•	•	•	•	•
0	1	1	0	0	1	1	R19	Update Address Reg (L)			√	•	•	•	•	•	•	•	•
0	1	1	1	1	1	1	R31	Dummy Location											

Notes: • Designates used bit in register

Designates unused bit in register Reading this bit is always 0, except for R31, which does not drive the data bus at all, and for $\overline{CS}$ = 1 which operates likewise

R0—HORIZONTAL TOTAL CHARACTERS

7	6	5	4	3	2	1	0
NUMBER OF CHARACTERS −1							

This 8-bit write-only register contains the total of displayed and non-displayed characters, minus one, per horizontal line. This register determines the frequency of HSYNC.

R1—HORIZONTAL DISPLAYED CHARACTERS

7	6	5	4	3	2	1	0
NUMBER OF CHARACTERS							

This 8-bit write-only register contains the number of displayed characters per horizontal line.

R2—HORIZONTAL SYNC POSITION

7	6	5	4	3	2	1	0
HORIZONTAL SYNC POSITION							

This 8-bit write-only register contains the position of HSYNC on the horizontal line, in terms of the character location number on the line. The position of the HSYNC determines the left to right location of the displayed text on the video screen. In this way, the side margins are adjusted.

R3—HORIZONTAL AND VERTICAL SYNC WIDTHS

7	6	5	4	3	2	1	0
V_3	V_2	V_1	V_0	H_3	H_2	H_1	H_0

This 8-bit write-only register contains the widths of both HSYNC and VSYNC, as follows:

HVSW
7-4 **VSYNC Pulse Width**
The width of the vertical sync pulse (VSYNC) in the number of scan lines. When bits 4-7 are all 0, VSYNC is 16 scan lines wide.

HVSW
3-0 **HSYNC Pulse Width**
The width of the horizontal sync pulse (HSYNC) in the number of character clock times (CCLK).

Control of these parameters allows the R6545-1 to interface with a variety of CRT monitors, since the HSYNC and VSYNC timing signals may be accommodated without the use of external one shot timing.

R4—VERTICAL TOTAL ROWS

7	6	5	4	3	2	1	0
—	NO. OF CHAR. ROWS −1						

The 7-bit Vertical Total Register contains the total number of character rows in a frame, minus one. This register, along with R5, determines the overall frame rate, which should be close to the line frequency to ensure flicker-free appearance. If the frame time is adjusted to be longer than the period of the line frequency, then $\overline{RES}$ may provide absolute synchronism.

R5—VERTICAL TOTAL LINE ADJUST

7	6	5	4	3	2	1	0
—	—	—	SCAN LINES				

The 5-bit write-only Vertical Total Line Adjust Register (R5) contains the number of additional scan lines needed to complete an entire frame scan and is intended as a fine adjustment for the video frame time.

R6—VERTICAL DISPLAYED ROWS

7	6	5	4	3	2	1	0
—	DISPLAYED CHAR. ROWS						

This 7-bit write-only register contains the number of displayed character rows in each frame. This determines the vertical size of the displayed text.

R7—VERTICAL SYNC POSITION

7	6	5	4	3	2	1	0
—	VERTICAL POSITION						

This 7-bit write-only register selects the character row time at which the vertical SYNC pulse is desired to occur and, thus, positions the displayed text in the vertical direction.

R8—MODE CONTROL (MC)

7	6	5	4	3	2	1	0
UM(T)	US(T)	CSK	DES	RRA	RAD	—	0

This 8-bit write-only register selects the operating modes of the R6545-1, as follows:

MC
7 **UM(T) —Update/Read Mode (Transparent Mode)**
0 Update occurs during horizontal and vertical blanking times with update strobe.
1 Update interleaves during Ø2 portion of cycle.

MC
6 **US(T) —Update Strobe (Transparent Mode)**
0 Pin 34 functions as memory address.
1 Pin 34 functions as update strobe.

MC
5 **CSK —Cursor Skew**
0 No delay
1 Delays Cursor one character time.

MC
4 **DES —Display Enable Skew**
0 No delay
1 Display Enable delays one character time.

MC 3 RRA —Refresh RAM Access
0 Shared memory access
1 Transparent memory access

MC 2 RAD —Refresh RAM Addressing Mode
0 Straight binary addressing
1 Row/column addressing

MC 1 —Not Used—don't care

MC 0 —Not Used—must be a 0.

R9—ROW SCAN LINES

7	6	5	4	3	2	1	0
—	—	—	SCAN LINES −1				

This 5-bit write-only register contains the number of scan lines, minus one, per character row, including spacing.

R10—CURSOR START LINE

7	6	5	4	3	2	1	0
—	B_1	B_0	START SCAN LINE				

R11—CURSOR END LINE

7	6	5	4	3	2	1	0
—	—	—	END SCAN LINE				

These 5-bit write-only registers select the starting and ending scan lines for the cursor. In addition, bits 5 and 6 of R10 are used to select the cursor blink mode, as follows:

B_1	B_0	Cursor Operating Mode
0	0	Display Cursor Continuously
0	1	Blank Cursor
1	0	Blink Cursor at 1/16 Field Rate
1	1	Blink Cursor at 1/32 Field Rate

A one character wide cursor can be controlled by storing values into the Cursor Start Line (R10) and Cursor End Line (R11) registers and into the Cursor Position Address High (R14) and Cursor Position Low (R15) registers.

R12—DISPLAY START ADDRESS HIGH

7	6	5	4	3	2	1	0
—	—	DISPLAY START ADDRESS HIGH					

R13—DISPLAY START ADDRESS LOW

7	6	5	4	3	2	1	0
DISPLAY START ADDRESS LOW							

These registers together form a 14-bit register whose contents is the memory address of the first character of the displayed scan (the character on the top left of the video display, as in Figure 1). Subsequent memory addresses are generated by the R6545-1 as a result of CCLK input pulses. Scrolling of the display is accomplished by changing R12 and R13 to the memory address associated with the first character of the desired line of text to be displayed first. Entire pages of text may be scrolled or changed as well via R12 and R13.

R14—CURSOR POSITION HIGH

7	6	5	4	3	2	1	0
—	—	CURSOR POSITION HIGH					

R15—CURSOR POSITION LOW

7	6	5	4	3	2	1	0
CURSOR POSITION LOW							

These registers together form a 14-bit register whose contents is the memory address of the current cursor position. When the video display scan counter (MA lines) matches the contents of this register, and when the scan line counter (RA lines) falls within the bounds set by R10 and R11, then the CURSOR output becomes active. Bit 5 of the Mode Control Register (R8) may be used to delay the CURSOR output by a full CCLK time to accommodate slow access memories.

A cursor of up to 32 characters in height can be displayed on and between the scan lines as loaded into the Cursor Start Line (R10) and Cursor End Line (R11) Registers.

The cursor is positioned on the screen by loading the Cursor Position Address High (R14) and Cursor Position Address Low (R15) registers with the desired refresh RAM address. The cursor can be positioned in any of the 16K character positions. Hardware paging and data scrolling is thus allowed without loss of cursor position. Figure 3 is an example of the display cursor scan line.

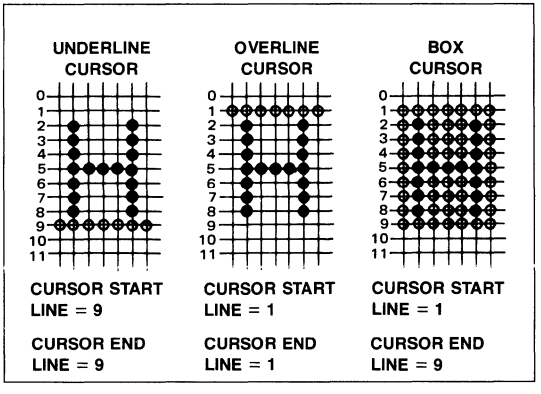


Figure 3. Cursor Display Scan Line Control Examples

R16—LIGHT PEN HIGH

7	6	5	4	3	2	1	0
—	—	LPEN HIGH					

R17—LIGHT PEN LOW

7	6	5	4	3	2	1	0
LPEN LOW							

These registers together form a 14-bit register whose contents is the light pen strobe position, in terms of the video display address at which the strobe occurred. When the LPEN input changes from low to high, then, on the next negative-going edge of CCLK, the contents of the internal scan counter is stored in registers R16 and R17.

R18—UPDATE ADDRESS HIGH

7	6	5	4	3	2	1	0
—	—	UPDATE ADDRESS HIGH					

R19—UPDATE ADDRESS LOW

7	6	5	4	3	2	1	0
UPDATE ADDRESS LOW							

These registers together comprise a 14-bit register whose contents is the memory address at which the next read or update will occur (for transparent address mode, only). Whenever a read/update occurs, the update location automatically increments to allow for fast updates or readouts of consecutive character locations. This is described elsewhere in this document. The section on REFRESH RAM ADDRESSING describes this more fully.

R31—DUMMY LOCATION

7	6	5	4	3	2	1	0
—	—	—	—	—	—	—	—

This register does not store any data, but is required to detect when transparent addressing updates occur. This is necessary to increment the Update Address Register and to set the Update Ready bit in the status register.

REGISTER FORMATS

Register pairs R12/R13, R14/R15, R16/R17, and R18/R19 are formatted in one of two ways:

(1) Straight binary, if register R8, bit 2 = 0
(2) Row/Column, if register R8, bit 2 = 1. In this case the low byte is the Character Column and the high byte is the Character Row.

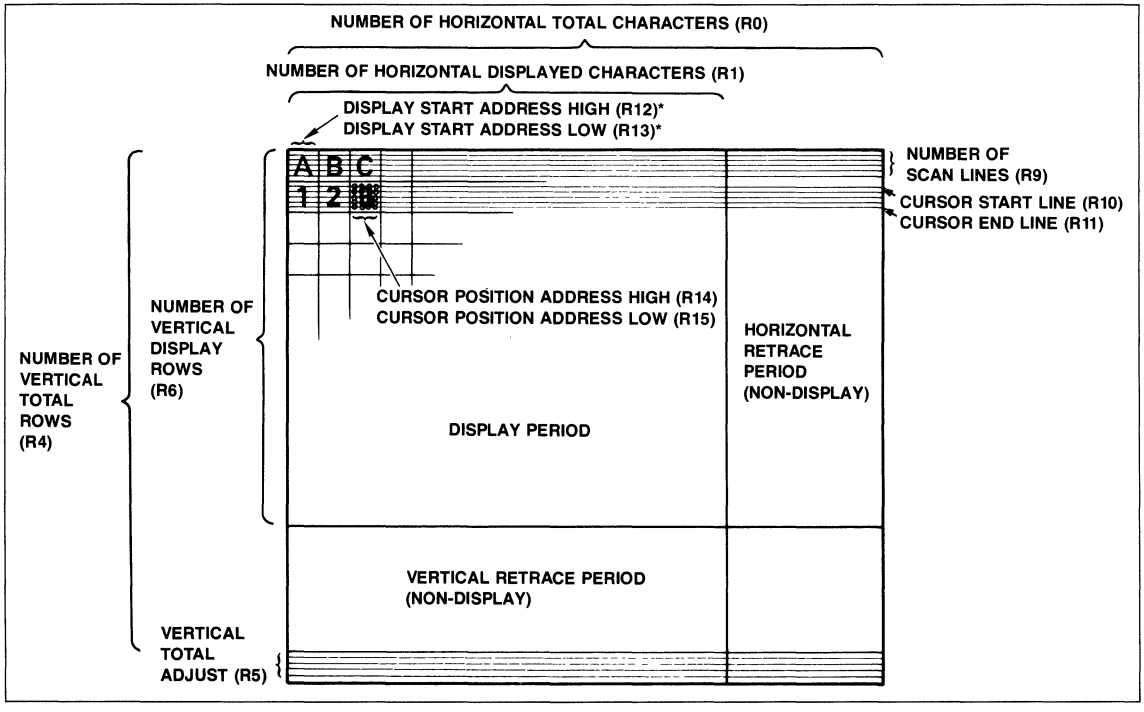


Figure 4. Video Display Format

DESCRIPTION OF OPERATION

VIDEO DISPLAY

Figure 4 indicates the relationship of the various program registers in the R6545-1 and the resultant video display.

Non-displayed areas of the Video Display are for horizontal and vertical retrace functions of the CRT monitor. The horizontal and vertical sync signals, HSYNC and VSYNC, are programmed to occur during these intervals and trigger the retrace in the CRT monitor. The pulse widths are constrained by the monitor requirements. The time position of the pulses may be adjusted to vary the display margins (left, right, top, and bottom).

REFRESH RAM ADDRESSING

There are two modes of addressing for the video display memory.

Shared Memory Mode (R8, BIT 3 = 0)

In this mode, the Refresh RAM address lines (MA0-MA13) directly reflect the contents of the internal refresh scan character counter. Multiplex control, to permit addressing and selection of the RAM by both the CPU and the CRTC, must be provided external to the CRTC. In the Row/Column address mode, lines MA0-MA7 become character column addresses (CC0-CC7) and MA8-MA13 become character row addresses (CR0-CR5). Figure 5 illustrates the system configuration.

Transparent Memory Addressing

For this mode, the display RAM is not directly accessible by the CPU, but is controlled entirely by the R6545-1. All CPU accesses are made via the R6545-1 and a small amount of external circuits. Figure 6 shows the system configuration for this approach.

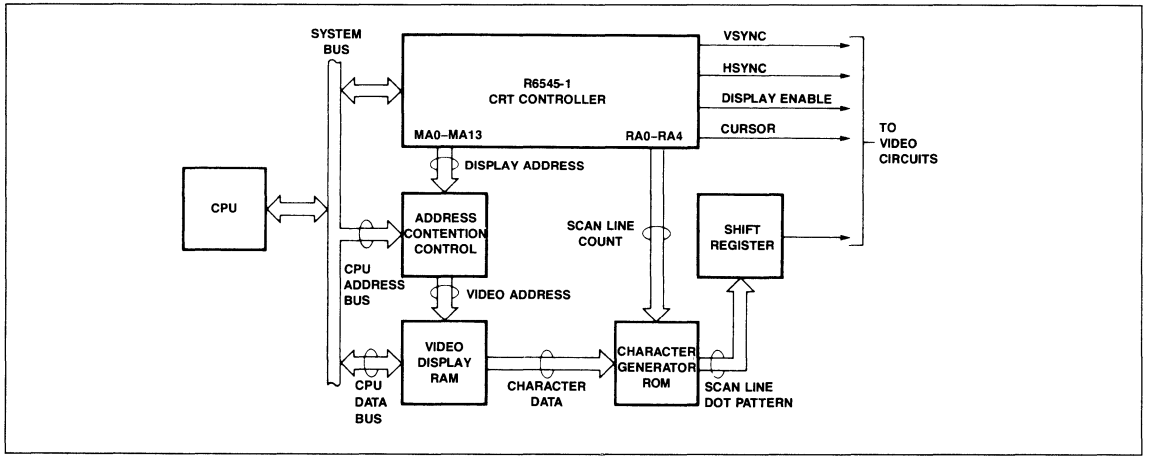


Figure 5. Shared Memory System Configuration

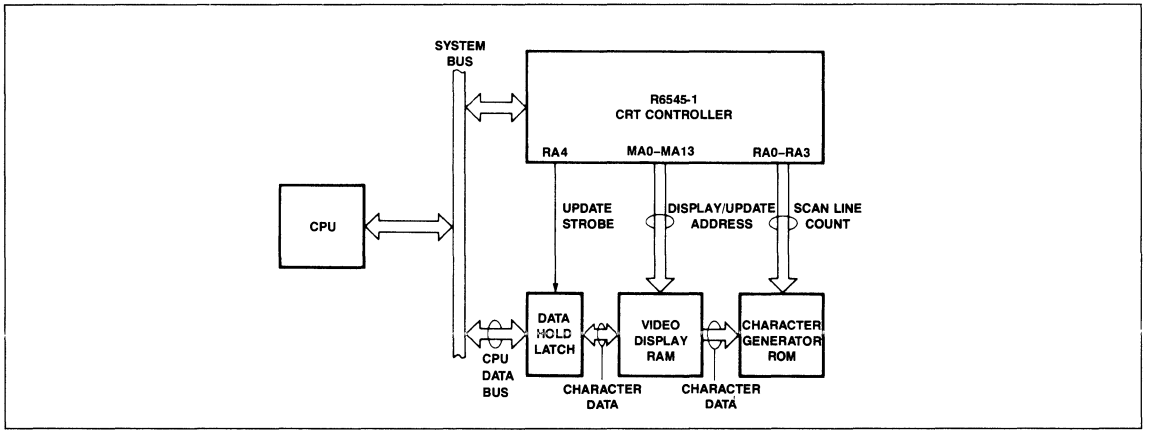


Figure 6. Transparent Memory Addressing System Configuration (Data Hold Latch Needed for Horizontal/Vertical Blanking Updates, Only).

ADDRESSING MODES

Figure 7 illustrates the address sequence for both modes of the Refresh RAM address.

Row/Column

In this mode, the CRTC address lines (MA0-MA13) generate as 8 column (MA0-MA7) and 6 row (MA8-MA13) addresses. Extra hardware is needed to compress this addressing into a straight binary sequence in order to conserve memory in the refresh RAM (register R8, bit 2 is a 1).

Binary

In this mode, the CRTC address lines are straight binary and no compression circuits are needed. However, software complexity increases since the CRT characters cannot be stored in terms of their row and column locations, but must be sequential (register R8, bit 2 is a 0).

USE OF DYNAMIC RAM FOR REFRESH MEMORY

The R6545-1 permits use of dynamic RAMS as storage devices for the Refresh RAM by continuing to increment memory addresses in the non-display intervals of the scan. This is a viable technique, since the Display Enable signal controls the actual video display blanking. Figure 7 illustrates Refresh RAM addressing for both row/column and binary addressing for 80 columns and 24 rows with 10 non-displayed columns and 10 non-displayed rows.

Note that the straight-binary mode has the advantage that all display memory addresses are stored in a continuous memory block, starting with address 0 and ending at 1919. The disadvantage with this method is that, if it is desired to change a displayed character location, the row and column identity of the location must be converted to its binary address before the memory may be written. The row/column mode, on the other hand, does not need to undergo this conversion. However, memory is not used as efficiently, since the memory addresses are not continuous, gaps exist. This requires that the system be equipped with more memory than actually used and this extra memory is wasted. Alternatively, address compression logic may be employed to translate the row/column format into a continuous address block.

The user selects whichever mode is best for the given application. The trade-offs between the modes are software versus hardware. Straight-binary mode minimizes hardware requirements and row/column minimizes software requirements.

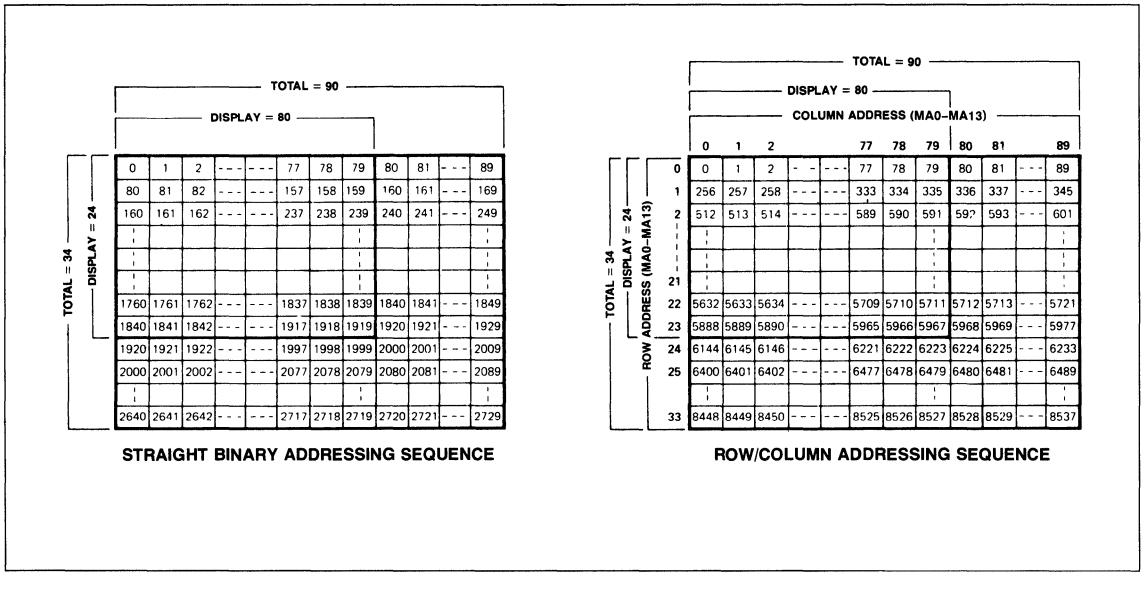


Figure 7. Display Address Sequences (with Start Address = 0) for 80 x 24 Example

MEMORY CONTENTION SCHEMES FOR SHARED MEMORY ADDRESSING

From the diagram of Figure 5, it is clear that both the R6545-1 and the system CPU must address the video display memory. The R6545-1 repetitively fetches character information to generate the video signals in order to keep the screen display active. The CPU occasionally accesses the memory to change the displayed information or to read out current data characters. Three ways of resolving this dual-contention requirement are apparent:

- **CPU Priority**

  In this technique, the address lines to the video display memory are normally driven by the R6545-1 unless the CPU needs access, in which case the CPU addresses immediately override those from the R6545-1 giving the CPU immediate access.

- **Ø1 and Ø2 Memory Interleaving**

  This method permits both the R6545-1 and the CPU access to the video display memory by time-sharing via the system Ø1 and Ø2 clocks. During the Ø1 portion of each cycle (the time when Ø2 is low), the R6545-1 address outputs are gated to the video display memory. In the Ø2 time, the CPU address lines are switched in. In this way, both the R6545-1 and the CPU have unimpeded access to the memory. Figure 8 illustrates the timings.

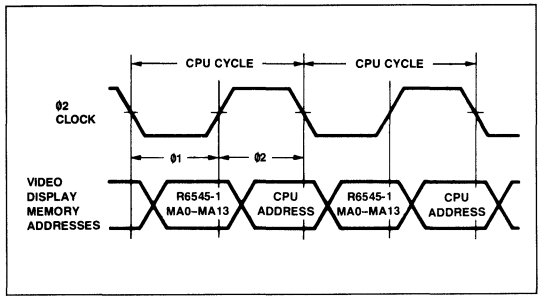


Figure 8. Ø1 and Ø2 Interleaving

- **Vertical Blanking**

  With this approach, the address circuitry is identical to the case for CPU Priority updates. The only difference is that the Vertical Retrace status bit (bit 5 of the Status Register) is used by the CPU so that access to the video display memory is only made during vertical blanking time (when bit 5 is a 1). In this way, no visible screen perturbations result. See Figure 10 for details.

TRANSPARENT MEMORY ADDRESSING

In this mode of operation, the video display memory address lines are not switched by contention circuits, but are generated by the R6545-1. In effect, the contention is handled by the R6545-1. As a result, the schemes for accomplishing CPU memory access are different:

- **Ø1 and Ø2 Interleaving**

  This mode is similar to the Interleave mode used with shared memory. In this case, however, the Ø2 address is generated from the Update Address Register (R18 and R19) in the R6545-1. Thus, the CPU must first load the address to be accessed into R18/R19 and then this address is always gated onto the MA lines during Ø2. Figure 9 shows the timing.

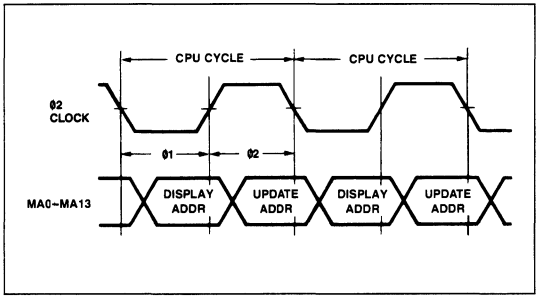


Figure 9. Ø1 and Ø2 Transparent Interleaving

- **Horizontal/Vertical Blanking**

  In this mode, the CPU loads the Update Address, but is only gated onto the MA lines during horizontal or vertical blank times, so memory accesses do not interfere with the display appearance. To signal when the update address is on the MA lines, an update strobe (STB) is provided as an alternate function of pin 34. Data hold latches are necessary to temporarily retain the character to be stored until the retrace time occurs. In this way, the system CPU is not halted waiting for the blanking time to arrive. Figure 11 illustrates the address and strobe timing for this mode.

CURSOR AND DISPLAY ENABLE SKEW CONTROL

Bits 4 and 5 of the Mode Control register (R8) are used to delay the Display Enable and Cursor outputs, respectively. Figure 12 illustrates the effect of the delays.

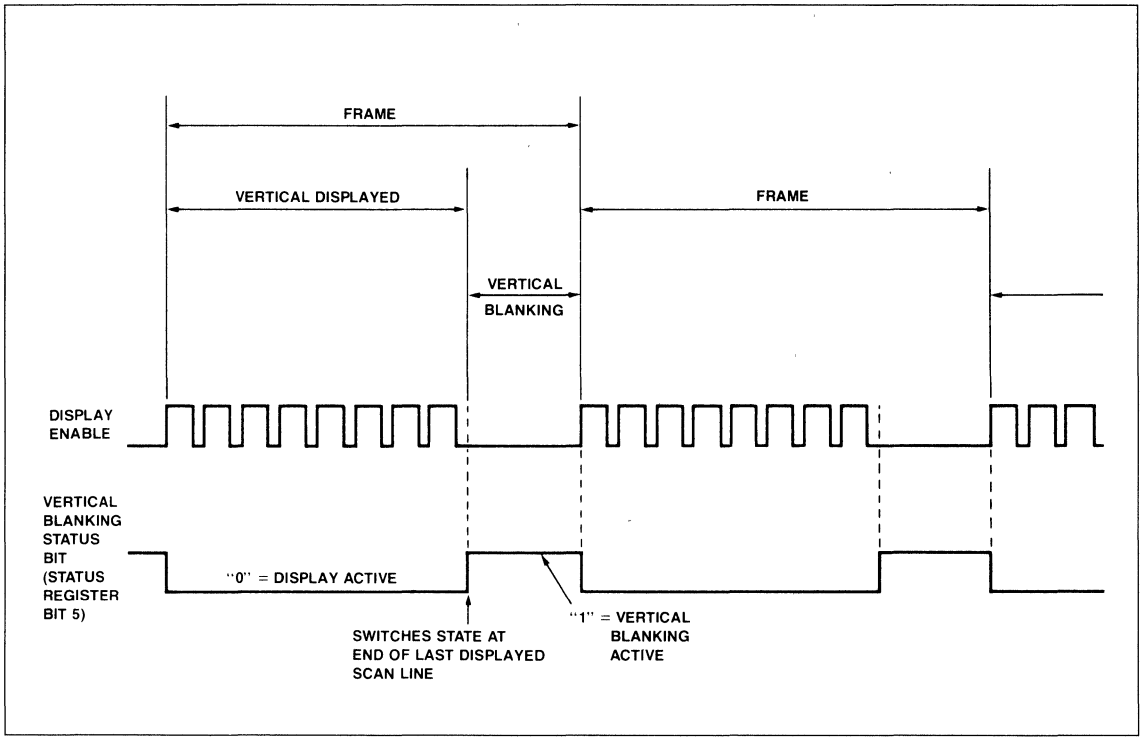


Figure 10. Operation of Vertical Blanking Status Bit

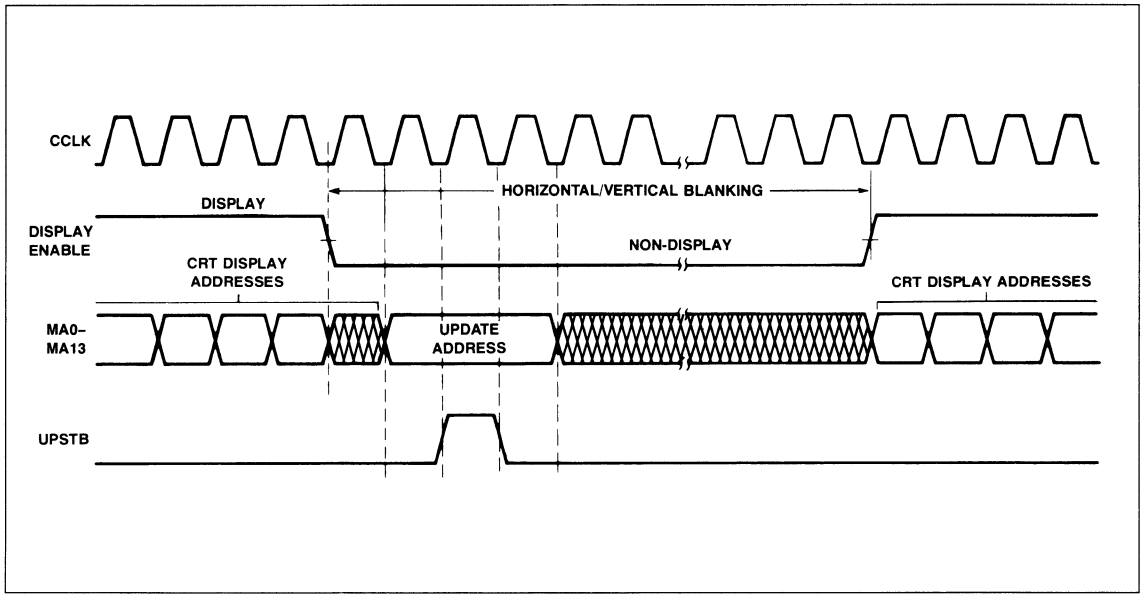


Figure 11. Retrace Update Timing

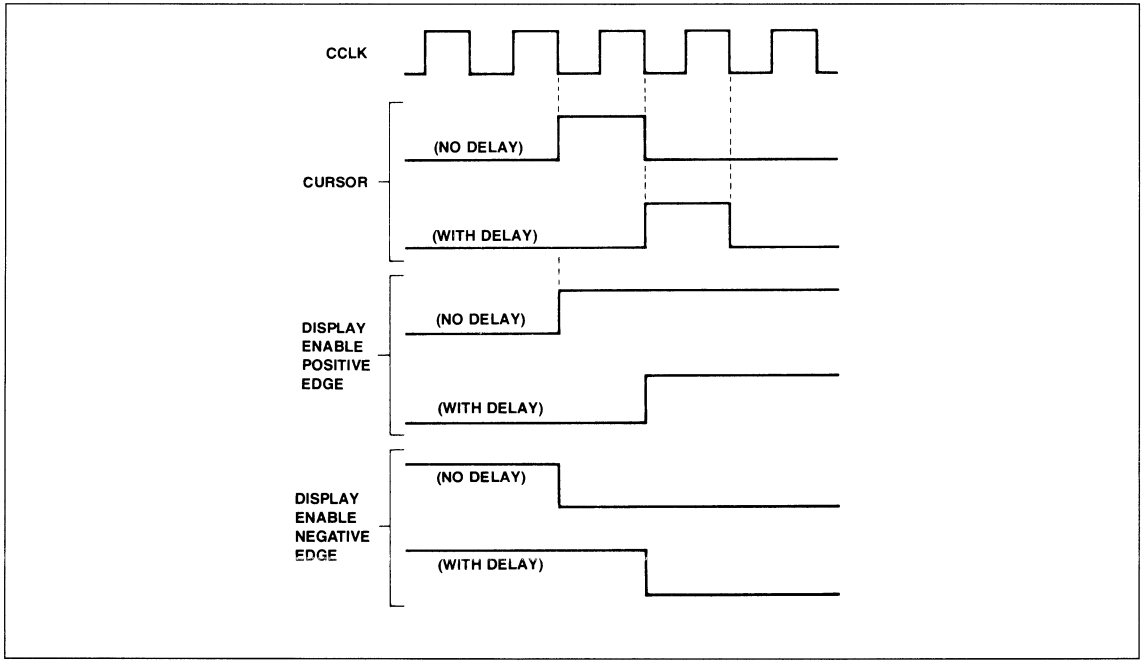


Figure 12. Cursor and Display Enable Skew

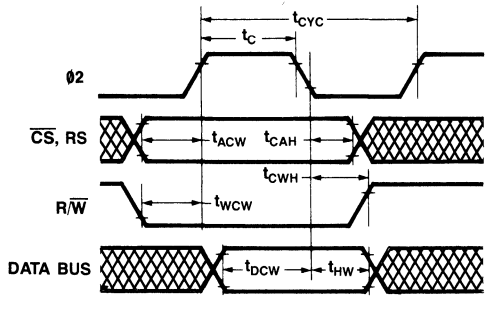
WRITE TIMING CHARACTERISTICS (V_{CC} = 5.0V ± 5%, T_A = T_L to T_H, unless otherwise noted)

Symbol	Characteristic	R6545-1		R6545A-1		Unit
		Min.	Max.	Min.	Max.	
t_{CYC}	Cycle Time	1.0	—	0.5	—	μs
t_C	Ø2 Pulse Width	440	—	200	—	ns
t_{ACW}	Address Set-Up Time	180	—	90	—	ns
t_{CAH}	Address Hold Time	0	—	0	—	ns
t_{WCW}	R/$\overline{W}$ Set-Up Time	180	—	90	—	ns
t_{CWH}	R/$\overline{W}$ Hold Time	0	—	0	—	ns
t_{DCW}	Data Bus Set-Up Time	265	—	100	—	ns
t_{HW}	Data Bus Hold Time	10	—	10	—	ns
(t_R and t_F = 10 to 30 ns)						

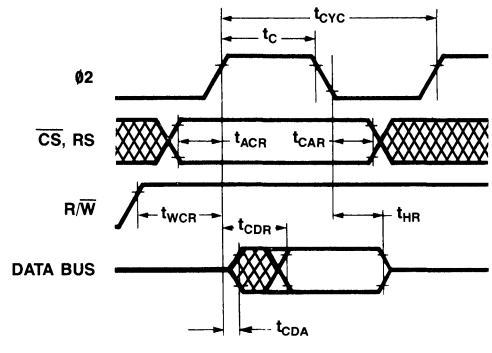
READ TIMING CHARACTERISTICS (V_{CC} = 5.0V ± 5%, T_A = T_L to T_H, unless otherwise noted)

Symbol	Characteristic	R6545-1		R6545A-1		Unit
		Min.	Max.	Min.	Max.	
t_{CYC}	Cycle Time	1.0	—	0 5	—	μs
t_C	Ø2 Pulse Width	440	—	200	—	ns
t_{ACR}	Address Set-Up Time	180	—	90	—	ns
t_{CAR}	Address Hold Time	0	—	0	—	ns
t_{WCR}	R/$\overline{W}$ Set-Up Time	180	—	90	—	ns
t_{CDR}	Read Access Time (Valid Data)	—	340	—	150	ns
t_{HR}	Read Hold Time	10	—	10	—	ns
t_{CDA}	Data Bus Active Time (Invalid Data)	40	—	40	—	ns
(t_R and t_F = 10 to 30 ns)						

WRITE TIMING WAVEFORMS



READ TIMING WAVEFORMS



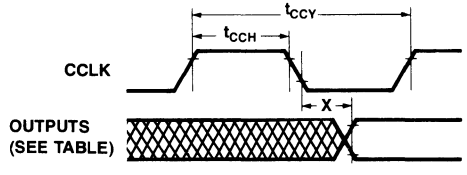
MEMORY AND VIDEO INTERFACE CHARACTERISTICS

(V_{CC} = 5.0V ± 5%, T_A = T_L to T_H, unless otherwise noted)

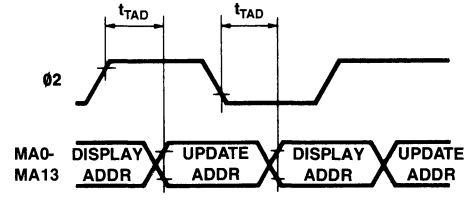
Symbol	Characteristic	R6545-1 Min.	R6545-1 Max.	R6545A-1 Min.	R6545A-1 Max.	Unit
t_{CCY}	Character Clock Cycle Time	0.40	—	0 40	—	μs
t_{CCH}	Character Clock Pulse Width	200	—	200	—	ns
(X)t_{MAD}	MA0–MA13 Propagation Delay	—	300	—	300	ns
(X)t_{RAD}	RA0–RA4 Propagation Delay	—	300	—	300	ns
(X)t_{DTD}	DISPLAY ENABLE Propagation Delay	—	450	—	450	ns
(X)t_{HSD}	HSYNC Propagation Delay	—	450	—	450	ns
(X)t_{VSD}	VSYNC Propagation Delay	—	450	—	450	ns
(X)t_{CDD}	CURSOR Propagation Delay	—	450	—	450	ns
t_{TAD}	MA0–MA13 Switching Delay	—	200	—	200	ns

Note: t_R, t_F = 20 ns (max).

SYSTEM TIMING WAVEFORMS



TRANSPARENT ADDRESSING WAVEFORMS (Ø1/Ø2 INTERLEAVING)

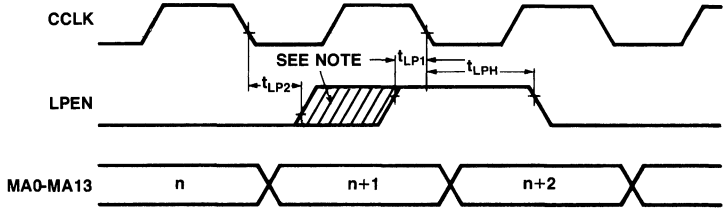


LIGHT PEN STROBE TIMING CHARACTERISTICS

Symbol	Characteristic	R6545-1 Min.	R6545-1 Max.	R6545A-1 Min.	R6545A-1 Max.	Unit
t_{LPH}	LPEN Hold Time	150	—	150	—	ns
t_{LP1}	LPEN Setup Time	20	—	20	—	ns
t_{LP2}	CCLK to LPEN Delay	0	—	0	—	ns

Note: t_R, t_F = 20 ns (max)

LIGHT PEN STROBE TIMING WAVEFORMS



NOTE: "Safe" time position for LPEN positive edge to cause address n+2 to load into Light Pen Register. t_{LP2} and t_{LP1} are time positions causing uncertain results.

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to +7.0	Vdc
Input Voltage	V_{IN}	−0.3 to +7.0	Vdc
Operating Temperature Range Commercial Industrial	T_A	 0 to +70 −40 to +85	°C
Storage Temperature	T_{STG}	−55 to +150	°C

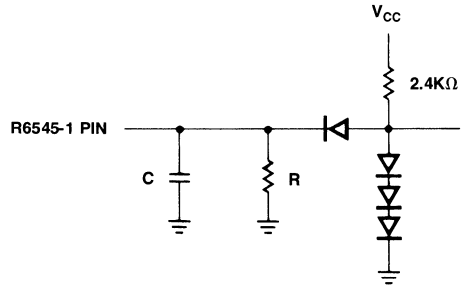
***NOTE:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

(V_{CC} = 5.0V ±5%, T_A = T_L to T_H, unless otherwise noted)

Parameter	Symbol	Min.	Max.	Unit
Input High Voltage	V_{IH}	2.4	V_{CC}	Vdc
Input Low Voltage	V_{IL}	−0.3	0.4	Vdc
Input Leakage (Ø2, R/$\overline{W}$, $\overline{RES}$, $\overline{CS}$, RS, LPEN, CCLK)	I_{IN}	—	2.25	μAdc
Three-State Input Leakage (D0–D7) (V_{IN} = 0.4 to 2.4V)	I_{TSI}	—	±10.0	μAdc
Output High Voltage I_{LOAD} = 205 μAdc (D0–D7) I_{LOAD} = 100 μAdc (all others)	V_{OH}	2 4	—	Vdc
Output Low Voltage I_{LOAD} = 1 6 mAdc	V_{OL}	—	0.4	Vdc
Power Dissipation	P_D	—	900	mW
Input Capacitance Ø2, R/$\overline{W}$, $\overline{RES}$, $\overline{CS}$, RS, LPEN, CCLK D0–D7	C_{IN}	 — —	10.0 12 5	pF pF
Output Capacitance	C_{OUT}	—	10 0	pF

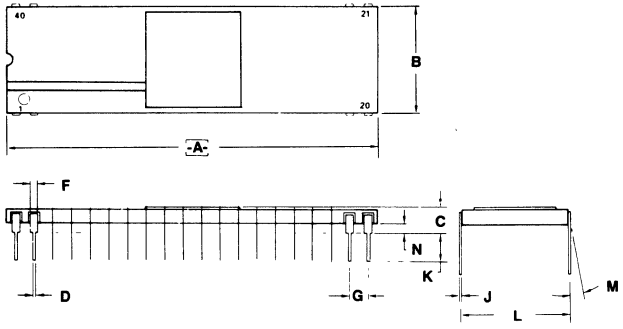
TEST LOAD



R = 11KΩ FOR D0-D7
= 24KΩ FOR ALL OTHER OUTPUTS
C = 130 pF TOTAL FOR D0-D7
= 30 pF ALL OTHER OUTPUTS

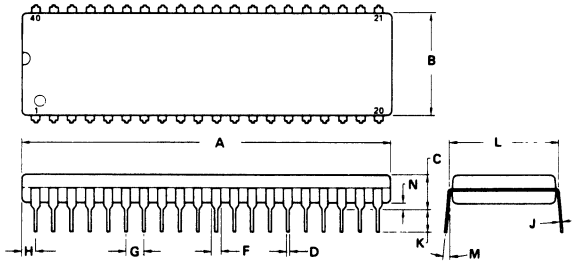
PACKAGE DIMENSIONS

40-PIN CERAMIC DIP



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	50 29	51 56	1 980	2 030
B	14 73	15 49	0 580	0 610
C	1 78	3 05	0 070	0 120
D	0 38	0 58	0 015	0 023
F	1 02	1 65	0 010	0 065
G	2 29	2 80	0 090	0 110
J	0 20	0 38	0 008	0 015
K	3 18	3 81	0 125	0 150
L	14 99	16 51	0 590	0 650
M	0°	10°	0°	10°
N	0 58	1 78	0 020	0 070

40-PIN PLASTIC DIP



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	51 28	52 32	2 040	2 060
B	13 72	14 22	0 540	0 560
C	3 55	5 08	0 140	0 200
D	0 36	0 51	0 014	0 020
F	1 02	1 52	0 040	0 060
G	2 54 BSC		0 100 BSC	
H	1 65	2 16	0 065	0 085
J	0 20	0 30	0 008	0 012
K	3 05	3 56	0 120	0 140
L	15 24 BSC		0 600 BSC	
M	7°	10°	7°	10°
N	0 51	1 02	0 020	0 040

R6549
COLOR VIDEO DISPLAY GENERATOR (CVDG)

PRELIMINARY

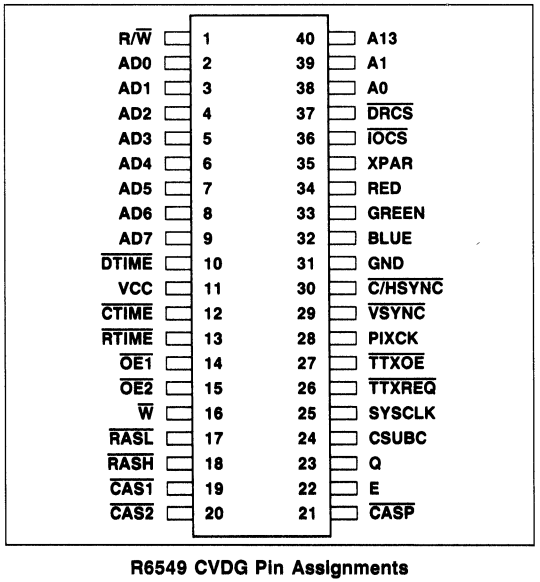
DESCRIPTION

The Rockwell R6549 Color Video Display Generator (CVDG) integrates video raster control; color lookup table (LUT) update and access; color generation and display refresh; teletext data DMA addressing, data routing and handshake; dynamic RAM (DRAM) control and refresh; and MPU/CVDG/DMA access to DRAM into a single device. Internal horizontal and vertical state machines generate video synchronization signals and control access of video color data from DRAM. A 16-entry color lookup table (LUT) supports 4-bit encoded color levels for red, green and blue (RGB) colors allowing 4096 color combinations to be generated. Each color code is converted to a 16-level analog signal by a dedicated DAC, combined with a blanking signal, and output in sync with a pixel clock.

Control registers allow MPU selection of CVDG operating mode and options while data registers allow MPU update of LUT data, current drawing pointer (CDP) graphics, Y scroll pointer and teletext pointer. The data registers can also be monitored by the MPU as can mode and raster scan status.

The R6549 is the first display generator to be designed exclusively in support of North American Presentation Level Protocol Syntax (NAPLPS) videotex (VTX) and teletext (TTX).

Replacing over 30 conventional MSI/LSI devices, the R6549 simplifies system design and layout, reduces printed circuit size, and minimizes required support circuits to speed system prototyping and greatly reduce both development and production costs.



R6549 CVDG Pin Assignments

FEATURES

- High performance video generator
  - 2:1 or 1:1 interlace
  - Analog red, green, blue (RGB) outputs
  - 16 levels per color plus blanking
  - 4096 color combinations
  - RS-170 sync and color subcarrier generation
  - 16 entry color look-up table (LUT)
  - RS-170 composite sync output with equalization and serration pulses
  - Internal/external video synchronization
  - Color subcarrier generation with line, field and pixel phase lock
  - Compatible with MC1377 color encoder
- Videotex (VTX)/Teletext (TTX) graphics
  - 256 x 210 x 4 bit-mapped video image buffer
  - Programmable border color
  - Transparent video overlay signal
  - Fast X CDP and Y CDP nibble or byte graphics I/O
  - NAPLPS X – Y origin with smooth Y vertical scroll
  - Fast horizontal drawing support with X auto increment byte write
- Dynamic RAM interface
  - Direct 48k-byte DRAM support, with auto inherent refresh for interfacing to six 16k x 4 DRAMS (4416-150 ns)
  - Supports three methods of DRAM access:
    - Video refresh 26.9k-byte DRAM—port or address mapped
    - Teletext/program 5.9k-byte DRAM—port or address mapped
    - Optional program 16k-byte DRAM extension—address mapped
  - Interleaving of MPU and CVDG DRAM access for uninterrupted read/write memory access without memory contention
  - On-chip refresh timing and control
- MPU Interface
  - Direct timing and cycle stealing for 1.4 MHz 68A09E MPU
  - Direct interface to R6512 CPU
- Teletext support
  - DMA interface and handshake to external NABTS teletext prefix processor
  - 5.72 Mbps effective data rate
  - 8k-byte teletext buffer DRAM interface

ORDERING INFORMATION

Part Number	Temperature Range
R6549	0°C to 70°C

Package: P = Plastic

Document No. 29651N86

Product Description Order No. 2183
September 1984

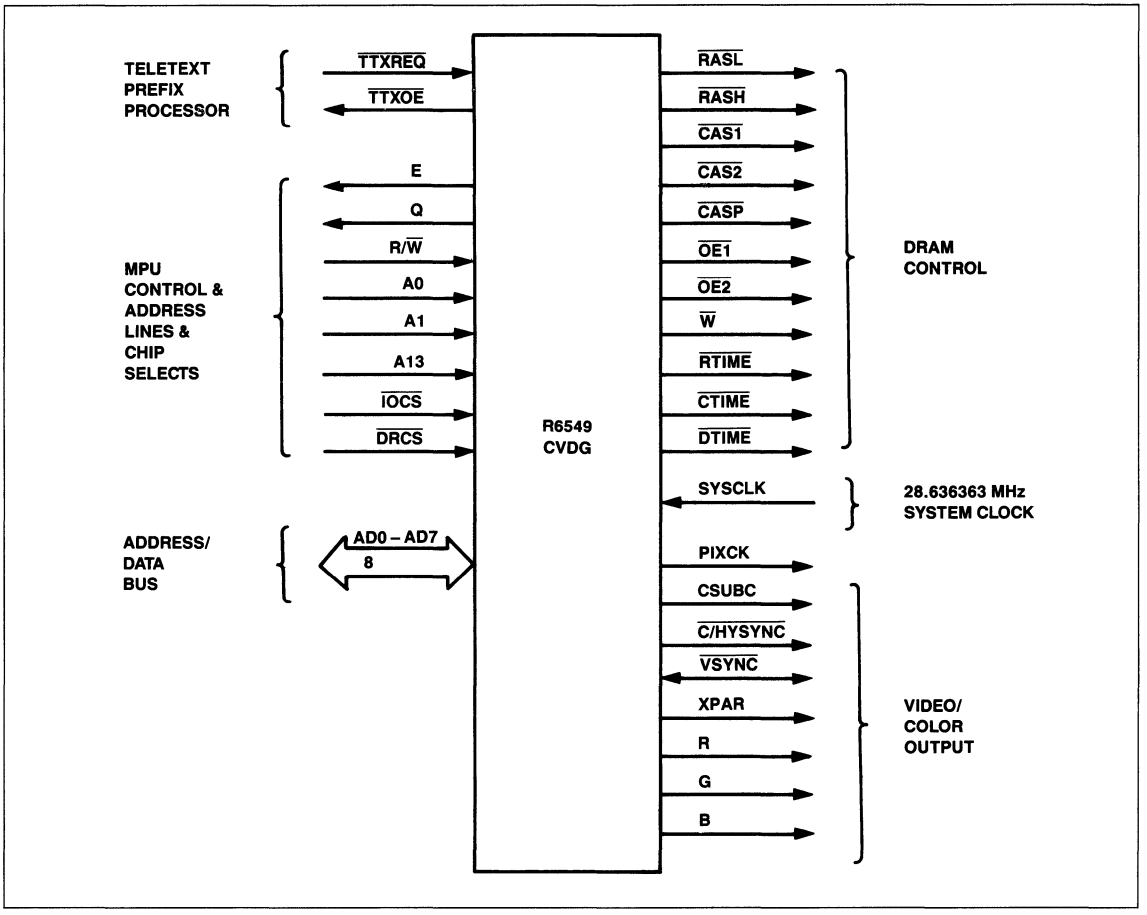


Figure 1. R6549 CVDG Interface Signals

PIN DESCRIPTION

Throughout this document signals are described logically using the terms active (or asserted) representing the true state, or inactive (or negated) representing the false state, regardless of whether the signal is active at a high or low voltage level.

The R6549 CVDG signals can be categorized into several different functional interfaces: MPU control and address bus, address/data (A/D) bus, DRAM control, color video output, teletext prefix processor and system clock input. Figure 1 identifies the signals within each group.

DMAC INTERFACE

$\overline{\text{TTXREQ}}$—Teletext DMA Request. An asynchronous falling edge-triggered request for direct memory access (DMA) transfer of data from a teletext prefix processor connected to the address/data (A/D) bus to DRAM. This TTL compatible input causes the CVDG to stop generating the E and Q clocks for one A/D bus cycle, output a 13-bit address (A0 – A12) to the DRAM during the processor portion of the A/D bus cycle, assert the $\overline{\text{TTXOE}}$ signal, and assert the $\overline{\text{W}}$ output to enable writing the data into DRAM.

$\overline{\text{TTXOE}}$—Teletext DMA Output Enable. An active LOW TTL compatible output pulse asserted within one A/D bus cycle after $\overline{\text{TTXREQ}}$ is asserted to acknowledge $\overline{\text{TTXREQ}}$ receipt and to enable data transfer from the teletext prefix processor onto the A/D bus (AD0 – AD7).

MPU CONTROL AND ADDRESS BUS

E—E Clock. A TTL compatible 1.43 MHz output clock that synchronizes data transfers over the MPU bus. This output drives the E clock input to the 6809E MPU. The E clock has special V_{OH} and V_{OL} output levels, V_{CC} – 0.5V and V_{SS} + 0.3V, respectively.

Q—Q Clock. A TTL compatible 1.43 MHz output clock that leads the E clock output for use by the 6809E.

R/$\overline{W}$—Read/Write. The TTL compatible Read/Write input controls the direction of data transfer between the MPU and the CVDG (HIGH = read from the CVDG; LOW = write to the CVDG). The R/$\overline{W}$ line should be connected to external data bus transceivers to also control the data direction between the MPU bus and the A/D bus.

A0, A1—MPU Address Line A0 and A1 Inputs. When $\overline{IOCS}$ is active, the encoded A0 and A1 inputs select the register in the CVDG to be accessed during a read or write operation (see Table 1). An exception is when A0 and A1 are both high during Mode 0, in which case DRAM is CDP accessed directly by the MPU at addresses generated by the CVDG.

When $\overline{DRCS}$ is active and program DRAM is selected (P = 1 in the DRAM Page Register), A0 is passed through the CVDG to drive the AD6 output during DRAM column address generation in the processor portion of the A/D bus cycle (see MPU DRAM Access Description).

A13—MPU Address Line A13 Input. When $\overline{DRCS}$ is active, A13 input HIGH causes program DRAM to be accessed ($\overline{CASP}$ asserted) during the processor portion of the A/D bus cycle independent of the P bit value in the DRAM Page Register. When program DRAM is selected in the DRAM Page Register (P = 1) or when A13 = 1, A13 is passed through the CVDG to drive the AD5 output during DRAM column address generation in the processor portion of the A/D bus cycle (see MPU DRAM Access Description).

$\overline{IOCS}$—I/O Chip Select. The active LOW, TTL compatible, $\overline{IOCS}$ input selects CVDG I/O port operation. The CVDG internal registers addressed by the A0 and A1 inputs are accessed as enabled by the mode selected in the Mode Register. Data direction is controlled by the R/$\overline{W}$ input as appropriate for each register and mode.

Table 1. CVDG Register Select Logic ($\overline{IOCS}$ =LOW)

A1	A0	Mode[1]	Read (R/$\overline{W}$ =H)	Write (R/$\overline{W}$ =L)
L	L	—	Status Register	Mode Register
L	H	0	X CDP Register	X CDP Register
H	L	0	Y CDP Register	Y CDP Register
H	H	0	DRAM[2]	DRAM[2]
H	H	1	—	LUT Address Register
H	H	2	LUT[3]	LUT Data Register
H	H	3	—	Switch Register
H	H	4	—	Y Scroll Register
H	L	5	TTX Pointer Register	TTX Pointer Register
H	H	6	—	DRAM Page Register

Notes:
1. The mode is selected in Mode Register.
2. DRAM is accessed directly by the MPU at DRAM addresses determined by the CVDG X CDP and Y CDP register contents
3. The LUT is accessed as enabled and addressed in the LUT Address Register.

$\overline{DRCS}$—DRAM Chip Select. $\overline{DRCS}$ is a TTL compatible, active LOW, input that enables MPU access to the DRAM. $\overline{CTIME}$, $\overline{RTIME}$ and $\overline{DTIME}$ outputs are asserted by the CVDG at the proper times to enable external buffers which drive the MPU generated address onto the A/D bus and drive data between the MPU bus data lines and the A/D bus in the direction controlled by R/$\overline{W}$ (HIGH = read from DRAM; LOW = write to DRAM). Note that $\overline{DRCS}$ configurations are advanced and optional for many configurations.

ADDRESS/DATA BUS

AD0 – AD7—Address/Data Lines. Eight TTL compatible, bidirectional, multiplexed address/data lines (AD0 – AD7) interface the CVDG directly to the video/program DRAM, through external buffers to the MPU address bus (A1 – A12), and through external transceivers to the MPU data bus (D0 – D7). These lines transfer both address and data between the DRAM and the CVDG and between the MPU bus and the CVDG/DRAM during one 698 ns A/D bus cycle.

$\overline{RASL}$, $\overline{RASH}$—Row Address Strobe Low and High. TTL compatible outputs strobe the upper eight bits of the address on A/D bus lines AD0–AD7 into DRAM (as DRAM addresses A6–A13) on the falling edge. $\overline{RASL}$ strobes the address into the DRAM containing the lower four data bits (D0–D3) and $\overline{RASH}$ strobes the address into the DRAM containing the upper four data bits (D4–D7).

$\overline{CAS1}$, $\overline{CAS2}$, $\overline{CASP}$—Column Address Strobes 1, 2 and P. The TTL compatible CAS outputs strobe the six lower bits of the address on A/D bus lines (AD1–AD6) into DRAM (as DRAM addresses A0–A5) on the falling edge. $\overline{CAS1}$ and $\overline{CAS2}$ connect to the video DRAM containing the LUT addresses. Four 4-bit LUT addresses packed into two bytes are accessed during the video portion of each A/D bus cycle. $\overline{CAS1}$ strobes the DRAM containing the LUT addresses for the first two pixel positions while $\overline{CAS2}$ strobes the DRAM devices containing the LUT addresses for the second two pixel positions. $\overline{CASP}$ connects to the program DRAM containing the program instructions/data.

$\overline{OE1}$, $\overline{OE2}$—DRAM Output Enable. These active LOW, TTL compatible, outputs enable DRAM device data output lines during a read. $\overline{OE1}$ connects to the two video DRAM devices containing byte 1 (LUT addresses for pixels 1 and 2) and is asserted first during a video refresh cycle. $\overline{OE2}$ connects to the two DRAM devices containing byte 2 (LUT addresses for pixels 3 and 4) and is asserted following $\overline{OE1}$. $\overline{OE2}$ is also connected to the program DRAM devices and enables their data outputs during the processor portion of the A/D bus cycle.

$\overline{W}$—DRAM Write Enable. The TTL compatible, active LOW, $\overline{W}$ output strobes data from the A/D bus into DRAM during a write in the processor portion of the A/D bus cycle. $\overline{W}$ is held HIGH during a read from DRAM.

$\overline{RTIME}$—Row Address Time. The active LOW, TTL compatible, $\overline{RTIME}$ output enables DRAM row address lines from the MPU onto the A/D bus through external buffers when $\overline{DRCS}$ is active. (Required for $\overline{DRCS}$ configurations only.)

$\overline{CTIME}$—Column Address Time. The active LOW, TTL compatible, $\overline{CTIME}$ output enables DRAM column address lines from the MPU onto the A/D bus through external buffers when $\overline{DRCS}$ is active. (Required for $\overline{DRCS}$ configurations only.)

$\overline{\text{DTIME}}$—Data Time. The active LOW, TTL compatible, $\overline{\text{DTIME}}$ output enables data transfer between the MPU data bus and the A/D bus through external transceivers when $\overline{\text{DRCS}}$ or $\overline{\text{IOCS}}$ is active.

SYSTEM CLOCK

SYSCLK—System Clock. A clock input with a duty cycle of 40/60 to 50/50. The clock frequency should be 28.63636 MHz ±80 Hz for proper operation of the colorburst frequency. This input clock may be stopped in either state for up to 1 μs to allow for external digital phase lock techniques.

VIDEO/COLOR OUTPUTS

CSUBC—Color Subcarrier Clock Output. A TTL compatible 3.579545 MHz ± 10% color subcarrier clock. The clock rate complies with the North American Color Burst Clock Output Standard. The rate is the SYSCLK divided by eight and is phase keyed to the horizontal sync ($\overline{\text{HSYNC}}$) output on $\overline{\text{C/HSYNC}}$ (as either a component of $\overline{\text{CSYNC}}$ or pure $\overline{\text{HSYNC}}$). Vertical blanking interval (VBI) color gating by $\overline{\text{VSYNC}}$ must be done externally (since some modems require an uninterrupted 3.579 MHz clock).

When the color outputs are connected to an MC1377 color encoder, the CSUBC output can be connected to the MC1377 CLK input, typically through a 500 pF capacitor/150 μH inductor filter network.

$\overline{\text{C/HSYNC}}$—Composite/Horizontal Sync Output. Either a composite sync ($\overline{\text{CSYNC}}$) or a horizontal sync ($\overline{\text{HSYNC}}$) output at TTL levels, asserted "tips down", is selected by the External Sync (EXT) bit in the Switch Register.

In internal sync (EXT = 0), an RS-170 composite sync with full serration and equalization is output in either 2:1 or 1:1 interlace as selected by the 2:1 Interlace Select (S21) bit in the Switch Register (S21 = 1 for 2:1; S21 = 0 for 1:1).

In external sync (EXT = 1), a pure $\overline{\text{HSYNC}}$ is output in either normal or early timing as selected by the Normal Horizontal Sync (NHS) bit in the Switch Register. In normal timing (NHS = 1), a 15.7 kHz signal is output; in advance timing (NHS = 0), a 15.9 kHz stop clock signal is output.

When the color outputs are connected to an MC1377 color encoder, the $\overline{\text{C/HSYNC}}$ output can be connected directly to the MC1377 SYNC input pin.

$\overline{\text{VSYNC}}$—Vertical Sync Input/Output. A TTL compatible vertical sync ($\overline{\text{VSYNC}}$) input or output signal depending on the state of the External Sync (EXT) bit in the Switch Register (see Mode 3). $\overline{\text{VSYNC}}$ is an externally generated input at power up or when EXT = 1. $\overline{\text{VSYNC}}$ is an internally generated output when EXT = 0.

The $\overline{\text{VSYNC}}$ output can be used to disable the color subcarrier at the chroma modulator during VBI. Videotex decoders can also use $\overline{\text{VSYNC}}$ to interrupt the MPU at a 60 Hz rate for blink, task and timekeeping operations.

PIXCLK—Pixel Clock Output. A 5.7272 MHz pixel output clock running synchronously with the RGB color outputs.

R, G, B—Red, Green and Blue Color Outputs. Three separate color analog output voltages. Each output provides a 1.0 Vpp video signal at high impedance with a 1.8 Vdc offset. Each color level is controlled by a 4-bit color code accessed from the LUT for each pixel position. A digital-to-analog converter (DAC) converts the 4-bit code to one of 16 output voltage levels (black level = 1.875 Vdc; white level = 2.800 Vdc). The three outputs allow 4096 color level combinations. A composite blanking signal (1.800 Vdc) is included in each output.

The output signals include high frequency clock components which may require low pass filtering in some applications. The outputs can be connected to the R IN, G IN, and B IN inputs to a MC1377 color encoder through 15 μF (typical) AC coupling capacitors.

The color outputs, through external buffers, can also drive 75 ohm loads, e.g., the inputs to an RGB color monitor/TV.

XPAR—Transparent Output. A TTL compatible, active HIGH, output controlled by one bit in a 4-bit code (three bits are don't care) in the LUT. A LUT value of 1XXX in DRAM asserts XPAR (HIGH); LUT value of 0XXX in DRAM negates XPAR (LOW). This output can be used to indicate which video source to select. When XPAR output is HIGH, external video signals should be selected to display background video; when XPAR output is LOW, CVDG outputs should be selected to display graphics. The XPAR output is always HIGH during composite blanking to pass external vertical blanking interval (VBI) signals, external sync, color burst, etc.

POWER/GROUND

VCC—Primary Power. 5.0 Vdc.

VSS—Ground. Power and signal ground.

FUNCTIONAL DESCRIPTION

The R6549 CVDG operation is controlled by three free-running synchronous state machines with the following cycle rates:

Address/Data (A/D) Bus Cycle	698 ns/cycle (1.43 MHz)
Horizontal Raster Line Cycle	63.5 μs/cycle (15.74 kHz)*
Vertical Raster Frame Cycle	33.3 ms/cycle (30 Hz)

The CVDG also includes timing shift registers and sample flip-flops to generate internal and external timing signals; programmed logic arrays (PLAs) to perform I/O decoding, generate DRAM control signals and determine state machine outputs; registers to hold command/status and data; an internal 16-bit row/column bus in display X-Y coordinates; internal input and output 8-bit data busses; and input/output buffers to isolate internal circuits from external interfaces and to drive outputs. Figure 2 illustrates the main CVDG components.

*A 15.9 kHz stop-clock early sync is selectable.

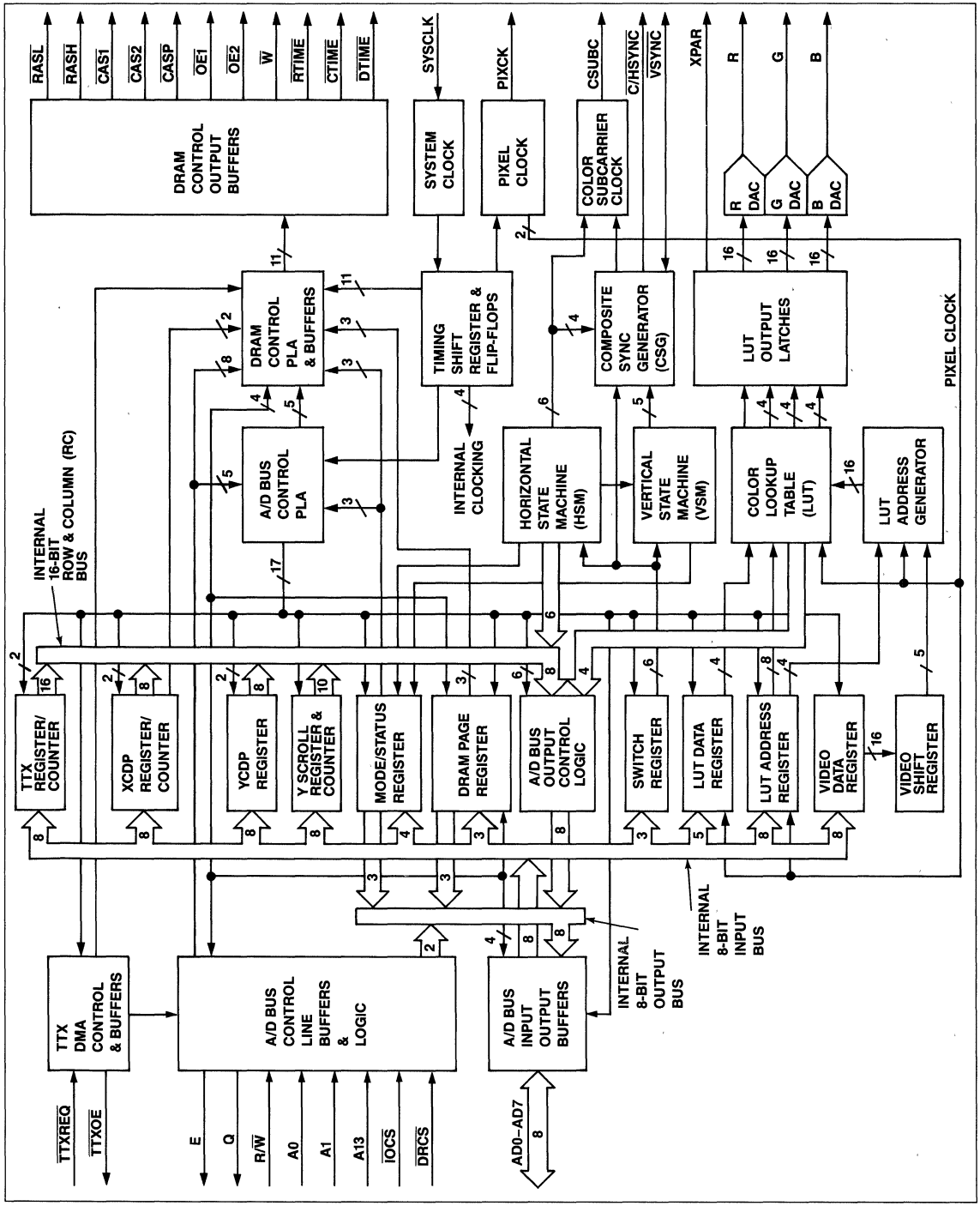


Figure 2. R6549 CVDG Block Diagram

SYSTEM TIMING

System Clock

Internal and output timing signals are derived from the 28.636363 MHz crystal frequency on the SYSCLK input pin. A two-phase non-overlapping 14.318181 MHz (SYSCLK/2) clock is generated to sequence high speed data transfer within the CVDG.

Timing Shift Register

The Timing Shift Register generates internal timing pulses as internal timing references at frequencies from 14.318 MHz down to 13.98 kHz. Flip-flops sample the various timing pulses to generate derivative timing reference signals for use by other CVDG circuits.

A two-phase non-overlapping 1.431818 MHz (SYSCLK/20) clock is generated for low speed sequencing within the CVDG and is also the external microprocessor bus and A/D bus timing reference. One phase of the 1.43 MHz clock drives the E clock output pin. A quadrature 1.431818 MHz clock leading the E clock is output on the Q output pin.

Pixel Clock

A 5.72 MHz pixel clock is output on the PIXCK output pin. Four pixel output clocks occur each 698 ns (one clock pulse coincident with each of the red, green and blue color level outputs and the transparent bit output for each pixel location).

VIDEO RASTER CONTROL

Horizontal Raster Line Cycle

An internal horizontal state machine (HSM) controls the horizontal raster line cycle. The HSM is incremented at the E clock rate, nominally every 698 ns. When normal horizontal sync timing is selected in the Switch Register (NHS = 1), 91 horizontal counts (HS0 – HS90), or states, comprise the 63.56 μs line raster. When early horizontal sync timing is selected (NHS = 0), typically to support external synchronization, 90 horizontal counts (HS0 – HS89) provide a 62.86 μs line raster. The first 64 counts clock the 256 displayed pixels (at four pixels per count). Figure 3 illustrates the horizontal and vertical raster count reference.

The HSM generates the horizontal raster timing pulses for internal logic and/or external output. These signals are the horizontal sync ($\overline{\text{HSYNC}}$), horizontal border and blanking, horizontal blanking, serration and equalization timing pulses.

The horizontal border and blanking pulse identifies the time that a border color is output (see LUT Data Register description) outside of the 256 pixel locations except during actual horizontal blanking. This signal is reported in bit 6 ($\overline{\text{HB}}$) of the Status Register.

An increment vertical count signal is also generated to increment the vertical state machine.

Vertical Raster Frame Cycle

An internal vertical state machine (VSM) controls the 33.3 ms vertical raster frame cycle. The VSM is incremented twice each horizontal raster line cycle. The VSM count (VS0 – VS523 or VS0 – VS524), or state, supports two frames per 30 ms vertical raster cycle. The upper count depends on the interlace mode (S21) switch position selected in the Switch Register. When 2:1 interlace mode is selected (S21 = 1), the upper VSM count supports a 262½ line frame. When 1:1 interlace is selected (S21 = 0), the upper VSM count supports a 262 line frame.

A VSM clear sign is normally generated when the VSM upper count is reached to restart the VSM at 0; however, when external sync is selected (EXT = 1) the VSM clear signal is generated from the external sync signal input on the $\overline{\text{VSYNC}}$ pin. Internal vertical state timing signals are generated for internal logic and/or external output. These signals include vertical sync ($\overline{\text{VSYNC}}$), vertical border and blanking, vertical blanking, and equalization enable pulses and the load Y scroll pointer time.

An internal vertical sync pulse, a vertical blanking pulse, and an equalization pulse are generated for combining with the $\overline{\text{HSYNC}}$ serration and equalization pulses when internal sync is selected (EXT = 0) to output composite sync on the $\overline{\text{C/HSYNC}}$ pin.

The vertical blanking pulse is also buffered and output on the $\overline{\text{VSYNC}}$ pin when internal sync is selected in the Switch Register (EXT = 0).

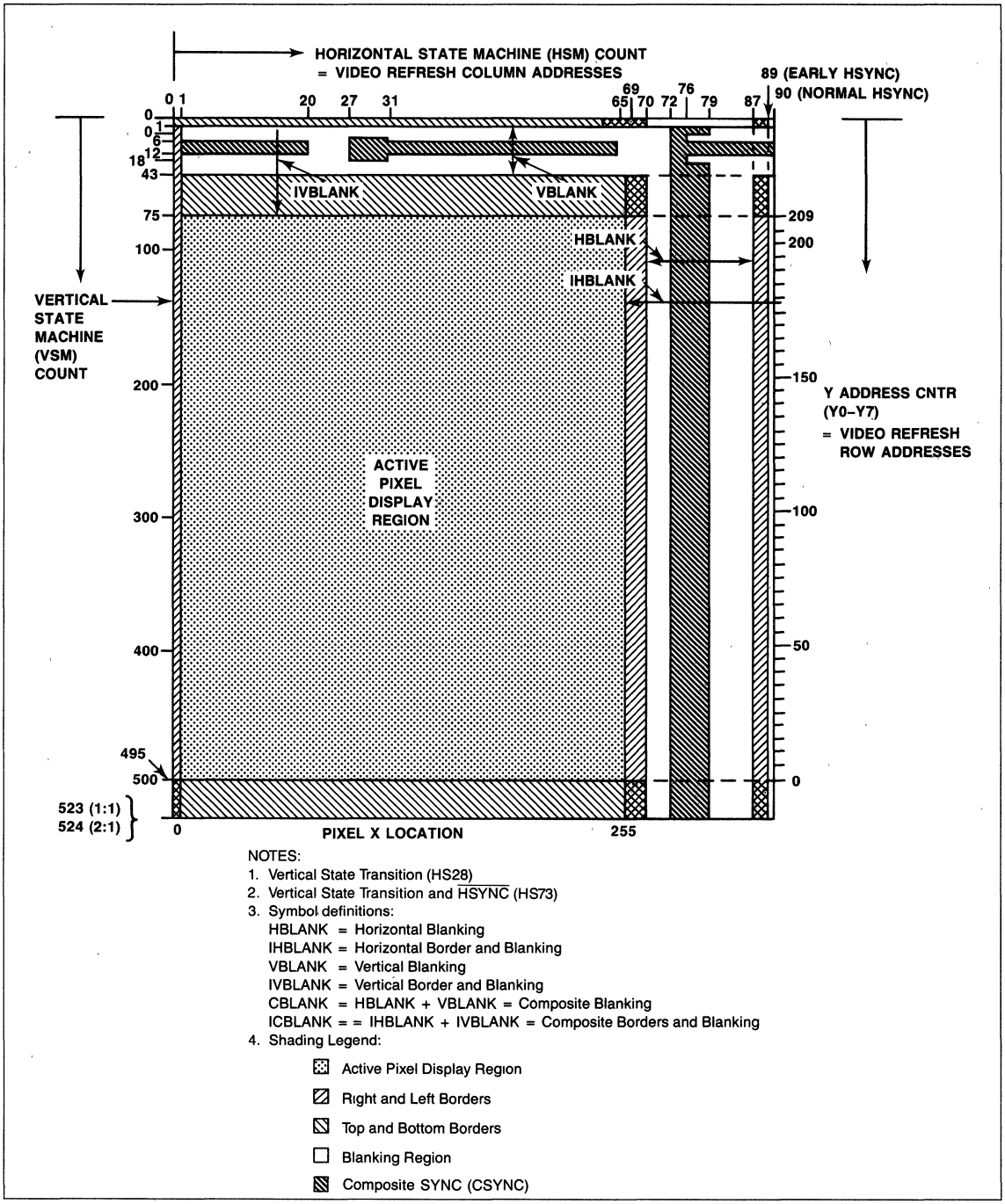
The internal vertical border and blanking pulse is generated and reported in bit 7 ($\overline{\text{VB}}$) of the Status Register. The pulse width is 3.302 ms for 2:1 interlace (S21 = 1) or 3.333 ms for 1:1 interlace (S21 = 0). This duration identifies the time the border color determined from the LUT Data Register is output, except during actual vertical blanking.

An internal load Y offset pointer signal is generated and routed to the Y Scroll Counter to cause the Y offset to load during the non-visible portion of the display raster.

Composite Sync and Color Subcarrier Clock Generation

$\overline{\text{HSYNC}}$ is output in one of two forms on the $\overline{\text{C/HSYNC}}$ pin depending upon the EXT bit state in the Switch Register. If internal sync is selected (EXT = 0), $\overline{\text{HSYNC}}$ is combined with horizontal blanking serration, equalization and vertical sync ($\overline{\text{VSYNC}}$) pulses to output as composite sync ($\overline{\text{CSYNC}}$). If external sync is selected (EXT = 1), the $\overline{\text{HSYNC}}$ signal is output on $\overline{\text{C/HSYNC}}$.

A 3.58 MHz color subcarrier clock (SYSCLK/8 and phase keyed to horizontal sync) is generated from composite sync and horizontal sync signals then is output on the CSUBC pin.



NOTES:
1. Vertical State Transition (HS28)
2. Vertical State Transition and $\overline{\text{HSYNC}}$ (HS73)
3. Symbol definitions:
   HBLANK = Horizontal Blanking
   IHBLANK = Horizontal Border and Blanking
   VBLANK = Vertical Blanking
   IVBLANK = Vertical Border and Blanking
   CBLANK = HBLANK + VBLANK = Composite Blanking
   ICBLANK = = IHBLANK + IVBLANK = Composite Borders and Blanking
4. Shading Legend:
   - Active Pixel Display Region
   - Right and Left Borders
   - Top and Bottom Borders
   - Blanking Region
   - Composite SYNC (CSYNC)

Figure 3. CVDG Video Raster Count Reference

ADDRESS/DATA BUS CONTROL

The Address/Data Bus state machine controls the operation of the 698 ns A/D bus cycle. The A/D bus cycle contains a 2-byte video data access cycle and a 1-byte I/O data access cycle (Figure 4). The addresses and data transferred on the A/D bus depend on the phase of the A/D bus cycle (i.e., the E clock level) and the type of operation in the I/O data access cycle. Table 2 identifies the source of the addresses for each type of DRAM access.

Video Data Access Cycle

The video data access cycle (also referred to as the video portion of the A/D bus cycle) occurs during the first half of the A/D bus cycle (when the E clock is LOW). Two bytes of video data (containing four LUT addresses corresponding to four pixel locations on the display) are read each cycle from DRAM at the DRAM address generated by the CVDG. The DRAM address is generated corresponding to the first of four pixel column locations in the horizontal raster and the pixel row location in the vertical raster. The video column (X) address of 0 to 64 is controlled by the horizontal state machine. The video row (Y) address of 209 to 0 is controlled by the Y Address Counter, which is in turn controlled by the vertical state machine and the Y Scroll Register. The two data bytes are loaded into the CVDG Video Data Register for subsequent serialization and LUT access (see the Pixel Color Generation description).

Up to 48k-bytes of Dynamic RAM (DRAM) can be connected to the A/D bus to store video data (LUT addresses) for video refresh, program instructions/data and received teletext data. The DRAM is segmented into six 8k-byte blocks with page selection of one block at a time during access (Figure 5). Four pages are required for video refresh (V00 – V11); three pages (V00, V01 and V10) hold video data exclusively, and one page (V11) holds video and program/teletext data. Two other pages hold program data. During the video data access cycle, and some modes of the I/O data access cycle, paging is handled automatically by the CVDG. The A13 and A0 input lines and the P, V1 and V0 bits in the CVDG DRAM Page Register select the page for MPU DRAM access during the I/O data access cycle (see MPU DRAM Access description).

I/O Data Access Cycle

The I/O data access cycle (also referred to as the processor portion of the A/D bus cycle) occurs during the second half of the A/D bus cycle (when E clock is HIGH). A/D bus address source and data source/destination depends upon CVDG chip select ($\overline{IOCS}$ and $\overline{DRCS}$) and Teletext Request ($\overline{TTXREQ}$) input levels, the selected CVDG mode, and the register select (A0 and A1) input levels. Refer to the description of each I/O access cycle function for details.

A/D Bus Control Line Buffers and Logic

The A/D Bus Control Line Buffers and Logic condition input and output A/D Bus control signals. Six input signals (R/$\overline{W}$, A0, A1, A13, $\overline{IOCS}$ and $\overline{DRCS}$) are buffered and routed to the DRAM Control PLA.

The E and Q output clocks are suppressed during a teletext DMA transfer. When $\overline{TTXREQ}$ input goes LOW, the Q and E clock outputs are held LOW to disable the clocks for one MPU bus cycle. In addition, the increment TTX address count goes HIGH to increment the modulo 32 TTX Counter. When $\overline{TTXREQ}$ goes HIGH at the completion of the DMA data transfer, the E and Q output clocks are enabled, the $\overline{TTXOE}$ output is negated (reset HIGH), and the increment TTX address count signal is reset.

Internal reset and initialization signals are generated when both $\overline{IOCS}$ and $\overline{DRCS}$ inputs are LOW for test purposes.

A/D Bus Control PLA

The A/D Bus Control PLA decodes CVDG and A/D Bus operation commands from buffered A/D bus control input signals and encoded mode bits in the Mode Register. Outputs from the PLA are buffered and routed to other circuits in the CVDG as internal enable signals.

A/D Bus Input/Output Buffers

The A/D Bus Input/Output Buffers isolate the internal CVDG data bus lines from the external A/D bus lines (AD0 – AD7). Input buffers continuously copy AD0 – AD7 onto the internal input data bus. Output buffers drive the states of the internal output data bus lines onto AD0 – AD7 when enabled by a CVDG output function and clocked by the 14.3 MHz internal clock. Two of these output buffers drive AD5 and AD6 during MPU DRAM access ($\overline{DRCS}$ = L) with the DRAM page signals, i.e., V0 and V1, respectively, or A13 and A0 inputs, respectively, depending on the state of the A13 input and the P bit in the DRAM Page Register.

A/D Bus Output Control Logic

The A/D Bus Output Control Logic drives data onto the internal output bus from the internal row and column bus lines, from the LUT, and from other internal CVDG circuits when enabled by outputs from the A/D Bus Control PLA.

DRAM Control PLA and Buffers

The DRAM Control PLA and Buffers generate and drive control and timing output signals to the DRAM; the row, column and data time output control signals for use by external line buffers and data line transceivers; and internal signals to control input/output data direction and to enable the internal row and column bus.

Timing pulses from the Timing Shift Registers; control signals from the Mode and Page registers, A/D Bus Control Buffers and Logic, and A/D Bus Control PLA; and control signals generated and derived from other sections of the CVDG are input to the PLA.

Output control states from the PLA are buffered and routed to external DRAM control signal pins ($\overline{RASL}$, $\overline{RASH}$, $\overline{CAS1}$, $\overline{CAS2}$, $\overline{CASP}$, $\overline{OE1}$, $\overline{OE2}$, and $\overline{W}$) and to external A/D bus control signal pins ($\overline{CTIME}$, $\overline{RTIME}$ and $\overline{DTIME}$). Other output signals are inverted and routed to internal logic.

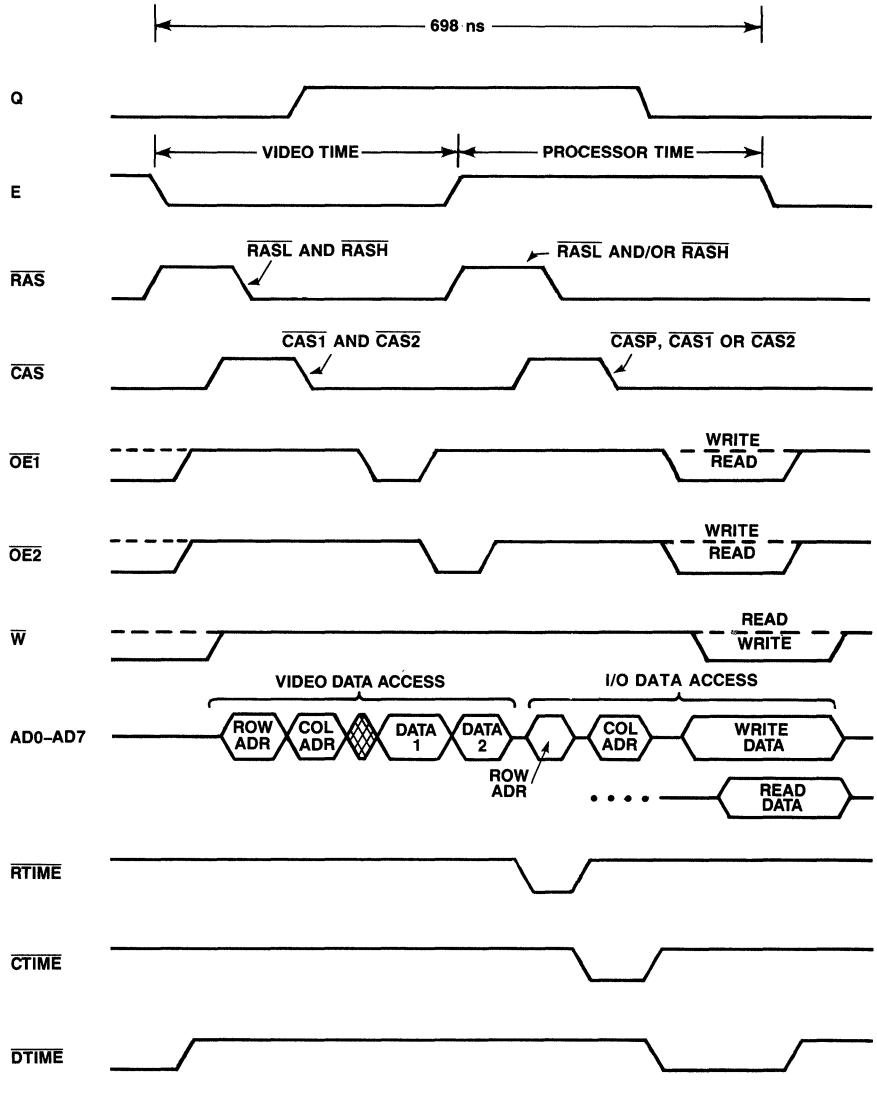


Figure 4. DRAM Address/Data (A/D) Bus Cycle

Table 2. Address/Data Bus Address Sources

DRAM Row/Column	—	CA5	CA4	CA3	CA2	CA1	CA0	—	RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0
CVDG Display Row/Column Bus	C7	C6	C5	C4	C3	C2	C1	C0	R7	R6	R5	R4	R3	R2	R1	R0
A/D Bus	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
Video Cycle[1]	0	V7	V6	V5	V4	V3	V2	0	V1	V0	H6	H5	H4	H3	H2	H1
Processor Cycle CDP Graphics[2] ($\overline{IOCS}$ = L, Mode 0)	X1[3]	Y7	Y6	Y5	Y4	Y3	Y2	X0[4]	Y1	Y0	X7	X6	X5	X4	X3	X2
MPU Video DRAM Access[5] ($\overline{DRCS}$ = L, P = 0)	A0[6]	V1[7]	V0[2]	A12	A11	A10	A9	0	A8	A7	A6	A5	A4	A3	A2	A1
MPU Program DRAM Access[8] ($\overline{DRCS}$ = L, P = 1)	0	A0[9]	A13[9]	A12	A11	A10	A9	0	A8	A7	A6	A5	A4	A3	A2	A1
Teletext DMA Access[10] ($\overline{TTXREQ}$ = L)	T0	1[11]	1[11]	T12	T11	T10	T9	0	T8	T7	T6	T5	T4	T3	T2	T1

Notes:

1. Video Cycle:
   H1 – H6 = HSM Output = 0 to 64 (= 0 to 255 pixel LUT addresses @ 4 addresses per access);
   V0 – V7 = Y Scroll Counter Output = 209 to 0
2. CDP Graphics:
   X0 – X7 = X CDP Register/Counter contents = 0 to 255;
   Y0 – Y7 = Y CDP Register contents = 0 to 255 (0 to 209 for displayable data)
3. X1 controls the $\overline{CAS1}$ and $\overline{CAS2}$ outputs:
   0 = Assert $\overline{CAS1}$
   1 = Assert $\overline{CAS2}$
4. X0 controls the $\overline{RASL}$ and $\overline{RASH}$ outputs:
   0 = Assert $\overline{RASL}$
   1 = Assert $\overline{RASH}$
5. MPU Video DRAM Access: A0 – A12 = MPU Address = 0 to 4096.
6. A0 input controls the $\overline{CAS1}$ and $\overline{CAS2}$ outputs:
   L = Assert $\overline{CAS1}$
   H = Assert $\overline{CAS2}$
7. V0 and V1 bits in the DRAM Page Register control assertion of AD6 and AD5 outputs, respectively:
   0 = Negate output
   1 = Assert output
8. MPU Program DRAM Access: A0 – A13 = MPU Address = 0 to 8192
9. A0 and A13 inputs control the AD6 and AD5 outputs, respectively:
   L = Negate output
   H = Assert output
10. Teletext Access:
    T1 – T4 = Modulo 32 counter incremented by each DMA byte transfer
    T5 – T12 = Teletext Pointer Register contents incremented by T1 – T4 overflow
11. AD6 and AD5 asserted to select program DRAM.

DRAM Page Register				Addr (Hex)	Addr (Dec)	Memory Page	Memory Function
A13	P	V1	V0				
				1FFF	8191		
1	1	X	X			Program 1 (A13 = 1)	PROGRAM
				0	0		
				1FFF	8191		
0	1	X	X			Program 0 (A13 = 0)	
				0	0		
				1FFF	8191		PROGRAM/ TELETEXT
0	0	1	1			Video 3 (V11)	
				0900	2304		
				08FF	2303	0,209 | 1,209	Note 2
				0	0		
				1FFF	8191		
0	0	1	0			Video 2 (V10)	
				0	0		
				1FFF	8191		VIDEO[1] DATA
0	0	0	1			Video 1 (V01)	
				0	0		
				1FFF	8191		
0	0	0	0			Video 0 (V00)	
				0	0	254,0 | 255,0	Note 2

Notes:

1. 26,880 bytes of video memory are required to support video refresh, i.e., to supply 53,760 4-bit LUT addresses in support of the 210 x 256 pixel display area. With 32,768 bytes supplied in four 4416 DRAM devices, 5888 bytes are available for general program/TTX message use in the upper part of video memory page 3 (V11).
2. Nibbles shown correspond to beginning and ending data for 210 x 256 pixel display area in X(column), Y(row) coordinates.

Figure 5. DRAM Memory Map

PIXEL COLOR GENERATION

LUT Address Generation

The 16-bit Video Data Register latches the four LUT addresses contained in the two data bytes acquired during the video data access cycle. Two 4-bit color lookup table (LUT) addresses are packed into each byte. The Video Shift Register serializes the four LUT addresses and transfers them one byte at a time to the LUT Address Generator. The LUT Address Generator latches the 4-bit coded LUT addresses from the Video Shift Register, converts the coded address to 16 binary signals and latches the binary address (0 – 15) for routing to the LUT.

LUT Operation

The color look-up table (LUT) is a 16 × 13 bit memory holding 16 entries of R, G and B color codes and corresponding transparent state (see Table 3). Each entry holds three 4-bit encoded color levels (0000 = lowest voltage level, 1111 = highest voltage level) and a 1-bit transparent state (0 = off, 1 = on). For each pixel location the three color level codes (R, G and B) are sampled from the LUT, latched and routed through three separate digital-to-analog converters. The transparent bit corresponding to each pixel location is also accessed from the LUT, latched, buffered and output on the $\overline{\text{XPAR}}$ pin.

Digital-To-Analog Conversion (DACs)

The 4-bit color code for each color (R, G and B) at a pixel position is converted to a corresponding analog voltage through a 16-level digital-to-analog converter (DAC). Four lines from the four color code lines and their four complements are decoded to one of 16 levels, sampled and latched. The latched outputs are in turn connected to the color output pin (R, G and B) through a voltage divider ladder network.

Table 3. LUT Structure

LUT ADDR (HEX)	LUT FORMAT																
	XPAR[1]				GREEN[2]				BLUE[2]				RED[2]				
	3	2	1	0	3	2	1	0	3	2	1	0	3	2	1	0	
F																	
E																	
D																	
C	0				0	0	0	0	0	1	0	0	0	1	1	1	Example 1[3]
B																	
A		NO															
9	1	ACTUAL			1	0	0	0	1	1	0	0	1	1	1	1	Example 2[4]
8		DATA															
7																	
6																	
5																	
4																	
3																	
2																	
1																	
0																	

Notes:

1. XPAR is a single bit in the LUT, the format shown corresponds to the LUT Data Register format:
   0XXX = XPAR output LOW
   1XXX = XPAR output HIGH

2. Color Data Level:
   0000 = lowest output voltage = 1.875 Vdc
   1111 = highest output voltage = 2.800 Vdc

3. Example 1—LUT Address C Data
   XPAR output = LOW
   G output = 1.875 + 0 (0.0617) = 1.875 Vdc
   B output = 1.875 + 4 (0.0617) = 2.122 Vdc
   R output = 1.875 + 7 (0.0617) = 2.307 Vdc

4. Example 2—LUT Address 9 Data·
   XPAR output = HIGH
   G output = 1 875 + 8 (0.0617) = 2.369 Vdc
   B output = 1.875 + 12 (0.0617) = 2.615 Vdc
   R output = 1.875 + 15 (0.0617) = 2.800 Vdc

I/O DATA ACCESS CYCLE FUNCTIONS

The I/O access cycle operates in one of five ways:

1. CVDG Mode/Status Register Access (enabled by $\overline{IOCS}$ LOW)
2. CVDG Graphics Access (enabled by $\overline{IOCS}$ LOW)
3. CVDG Parameter I/O Access (enabled by $\overline{IOCS}$ LOW)
4. MPU DRAM I/O Access (enabled by $\overline{DRCS}$ LOW)
5. Teletext Byte DMA (enabled by $\overline{TTXREQ}$ LOW)

The basic type of I/O access cycle is determined by the chip select ($\overline{IOCS}$ or $\overline{DRCS}$) and Teletext Request ($\overline{TTXREQ}$) inputs. When neither of the chip select inputs are LOW, nor has a TTX DMA transfer been initiated by $\overline{TTXREQ}$ LOW, the I/O access cycle is idle with no data transfer occurring during the processor portion of the A/D bus cycle.

When $\overline{IOCS}$ is LOW, the register address inputs (A0 and A1) and the mode selected in the CVDG Mode Register define the specific CVDG I/O operation, i.e., Mode/Status Register Access, CVDG Graphics Access (Mode 0), or one of the six CVDG Parameter Access modes (Modes 1–6). Table 4 shows the CVDG registers accessible during the I/O access cycle and the bit assignments. When A1 and A0 are both HIGH, the register bits are defined with reference to a pseudo Data Register (DR). The actual internal CVDG register accessed depends on the selected mode (see Table 4). The bits are defined in the following text.

CVDG Mode/Status Register Access

When $\overline{IOCS}$ is LOW and the register address is zero (A0 and A1 inputs are both LOW), the Mode Register (MR) or the Status Register (SR) is accessed depending upon the R/$\overline{W}$ input level. When R/$\overline{W}$ is LOW, the Mode Register is written; when R/$\overline{W}$ is HIGH, the Status Register is read.

Table 4. CVDG Register Summary

Internal CVDG Register	Mode	Register Select Lines		R/W[4]	Register Bit No.								Reset[3]
		A1	A0		7	6	5	4	3	2	1	0	
Mode Register	—	0	0	W	—	—	—	—	S	M2	M1	M0	0F
Status Register	—	0	0	R	$\overline{VB}$	$\overline{HB}$	M2	M1	M0	P	V1	V0	——
X CDP Register	0	0	1	R/W	X7	X6	X5	X4	X3	X2	X1	X0	00
Y CDP Register	0	1	0	R/W	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0	00
DRAM[1]	0	1	1	R/W	P3	P2	P1	P0	Q3	Q2	Q1	Q0	——
LUT Address Register	1	1	1	W	XPE	RE	GE	BE	A3	A2	A1	A0	00
LUT[2]	2	1	1	R	—	—	—	—	D3	D2	D1	D0	——
LUT Data Register	2	1	1	W	—	—	—	—	D3	D2	D1	D0	——
Switch Register	3	1	1	W	NHS	S21	EXT	LS	TST	—	—	—	F8
Y Scroll Register	4	1	1	W	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0	00
TTX Pointer Register	5	1	0	R/W	A12	A11	A10	A9	A8	A7	A6	A5	00
DRAM Page Register	6	1	1	W	—	—	—	—	—	P	V1	V0	07

Notes:
1. The DRAM is directly accessed and not the CVDG.
2. Data is transferred from the LUT onto the A/D bus without going through the LUT Data Register.
3. Reset state upon power up.
4. R/W = Read/write (R = read only; W = write only; R/W = read or write).

Mode Register

The write-only Mode Register selects the CVDG mode for next read from, or write to, the CVDG. In addition, the Mode Register contains a submode flag applicable only to Mode 0. The Mode Register may be written at any time regardless of the current CVDG mode. The mode and submode bits are initialized to ones upon power up.

				Bit Position							
Register	A1	A0	R/W	7	6	5	4	3	2	1	0
Mode	0	0	W	—	—	—	—	S	M2	M1	M0

MR7–MR4 Not used (no effect)

MR3 CDP Submode Flag (S) — (Mode 0 only—see Mode 0 description)

0 Enable CDP Nibble Submode. Allows read/write of a single 4-bit pixel nibble in a byte.

1 Enable CDP Byte Submode. Allows read/write of two 4-bit pixel nibbles in a byte with automatic increment of the X CDP for faster storage of LUT addresses in DRAM.

MR2–MR0			CVDG Mode (M2–M0)
(M2)	(M1)	(M0)	
0	0	0	Mode 0 — Port CDP Graphics
0	0	1	Mode 1 — LUT Address
0	1	0	Mode 2 — LUT Data
0	1	1	Mode 3 — Switch Register
1	0	0	Mode 4 — Y Scroll Offset Register
1	0	1	Mode 5 — Teletext DMA Pointer
1	1	0	Mode 6 — Set DRAM Page
1	1	1	Not used — no effect

Note that the mode must be written into the Mode Register before the desired mode can be executed.

Status Register

The read-only Status Register reports the selected CVDG mode, the selected DRAM page and the status of the horizontal and vertical raster blanking signals. The Status Register may be read at anytime regardless of the CVDG mode.

The horizontal blanking ($\overline{HB}$) and vertical blanking ($\overline{VB}$) signals report the state of the video raster at the time of access. The states of these two signals can be used for 15 kHz poll-driven timing, vertical blanking interval (VBI) identification, LUT loading, etc. These blanking times reflect the non-pixel display time including the time actual horizontal and vertical blanking signals are generated (for inclusion in composite sync output).

				Bit Position							
Register	A1	A0	R/W	7	6	5	4	3	2	1	0
Status	0	0	R	$\overline{VB}$	$\overline{HB}$	M2	M1	M0	P	V1	V0

SR7 Vertical Blanking ($\overline{VB}$)

0 Vertical blanking is asserted.

1 Vertical blanking is not asserted.

SR6 Horizontal Blanking ($\overline{HB}$)

0 Horizontal blanking is asserted.

1 Horizontal blanking is not asserted.

SR5–SR3 Mode Selected (M2–M0)

Reports the current CVDG mode as selected in bits 2–0 of the Mode Register.

SR5 (M2)	SR4 (M1)	SR3 (M0)	
0	0	0	Mode 0 — Port CDP Graphics
0	0	1	Mode 1 — LUT Address
0	1	0	Mode 2 — LUT Data
0	1	1	Mode 3 — Switch Register
1	0	0	Mode 4 — Y Scroll Offset Register
1	0	1	Mode 5 — Teletext DMA Pointer
1	1	0	Mode 6 — DRAM Page
1	1	1	Not used — no effect

SR2–SR0 DRAM Page Selected (P, V1, V0)

Reports the current DRAM Page selected in bits 2–0 of the Page Register (see Mode 6 — Write DRAM Page). P is the program RAM page indicator. V0 and V1 are the video page indicators.

SR2 (P)	SR1 (V1)	SR0 (V0)	Selected DRAM Page
0	0	0	Video Page 0: 8k-byte video RAM
0	0	1	Video Page 1: 8k-byte video RAM
0	1	0	Video Page 2: 8k-byte video RAM
0	1	1	Video Page 3: 2.3k-byte video RAM; 5.9k-byte program RAM
1	0	0	Program Page: 16k-byte optional program RAM accessed via $\overline{DRCS}$ (additionally paged by A13 and A0 inputs)

Mode 0 — Port CDP Graphics

When $\overline{IOCS}$ is LOW and Mode 0 is selected in the Mode Register, the Port Current Drawing Pointer (CDP) Mode is active. In this mode display column and row addresses can be written to the CVDG Current Drawing Pointer (CDP) X and Y registers, respectively, and pixel data accessed in DRAM. This mode is primarily used to update LUT addresses (i.e., the CDPs) in the video pages of DRAM. These LUT addresses are the video data read from the DRAM by the CVDG during the video portion of the A/D bus cycle.

This mode can be used to write or read data in any of the four 8k-byte video pages of DRAM defined by the V0 and V1 bits in the CVDG DRAM Page Register. The first three pages (V00, V01 and V10) are used exclusively for video data. 2304 bytes (addresses 0–8FF) of the fourth page (V11) are used for video data while the rest of the DRAM can be used for program or teletext message storage.

In mode 0, the MPU writes the address of the data in display coordinates into the CVDG X CDP and Y CDP registers. The X CDP contains the pixel position in the horizontal axis (i.e., the display column number) and varies from 0 to 255 (hex FF). Each pixel data nibble corresponds to a location (0 to 15) in the color look-up table (LUT) from which the corresponding R, G and B color levels and transparent bit data are retrieved for color generation. The Y CDP contains the pixel position in the vertical axis (i.e., the display row number) and varies from 0 to 255 (hex FF). Only values of 0 to 209 are used by the CVDG during the video portion of the A/D bus cycle to access video data. Y addresses 210–255 identify DRAM address on video DRAM page V11 that can contain non-displayable data, i.e., program or teletext data.

The registers accessible (besides in Mode and Status registers) in this mode are:

				Bit Position							
Register	A1	A0	R/W	7	6	5	4	3	2	1	0
X CDP	0	1	R/W	X7	X6	X5	X4	X3	X2	X1	X0
Y CDP	1	0	R/W	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0
DRAM*	1	1	R/W	P3	P2	P1	P0	Q3	Q2	Q1	Q0
*Not CVDG Access											

The X CDP Register is accessed at register address 1 (A1 = 0 and A0 = 1) and the Y CDP Register is accessed at register address 2 (A1 = 1 and A0 = 0). When register address 3 (A1 = 1 and A0 = 1) is detected, the CVDG generates DRAM row and column addresses corresponding to the display coordinates loaded in the X CDP and Y CDP registers. Data is then written from the A/D bus to the DRAM (R/$\overline{W}$ = low) or read from the DRAM to the A/D bus (R/$\overline{W}$ = high).

There are two submodes in Mode 0 that allow accessing of DRAM data at either the nibble (4-bit) or byte (8-bit) level. The submode is selected by the S bit (bit 3) in the Mode Register:

S = 0 CDP Nibble Submode
S = 1 CDP Byte Submode

CDP Nibble Submode

The CDP Nibble Submode (S = 0) reads or writes DRAM data one nibble at a time. Eight bits of data corresponding to two 4-bit LUT addresses (P3–P0 and Q3–Q0) are on the A/D data bus, but only one nibble is read or written during each access.

When writing the data, the Q nibble should contain the same pixel data as the P nibble. Only one of the nibble values is strobed into DRAM according to the X0 value in the X CDP Register which enables the $\overline{RASL}$ or $\overline{RASH}$ signal to DRAM during the write. If X0 = 0, the Q nibble (data bits 3–0) is written into the DRAM (row address strobed by $\overline{RASL}$); if X0 = 1, the P nibble (data bits 7–4) is written into the DRAM (row address strobed by $\overline{RASH}$).

When reading the data, only one nibble is read depending on the state of X0 in the X CDP. If X0 = 0, the Q nibble is read (row address strobed by $\overline{RASL}$); if X0 = 1, the P nibble is read (row address strobed by $\overline{RASH}$).

Reading or writing the data in this submode has no effect on the X CDP or Y CDP register values.

CDP Byte Access Submode

The CDP Byte Submode (S = 1) reads or writes two 4-bit LUT addresses at a time (in one byte) with an automatic increment of the X CDP value in the X CDP Register during write. Each write of the DRAM data writes the eight data bits on AD0–AD7 into DRAM and increments the X CDP by two upon the completion of the write cycle. (The new X CDP count can be read from the X CDP Register at any time.) As writing of the data continues, the X CDP value eventually wraps around to zero and continues incrementing. The Y CDP Register value must be incremented by writing a new Y CDP value. The automatic increment of X CDP value allows fast horizontal drawing for filling of polygon and rectangle type shapes (i.e., no intervening X CDP update is required). Note that the filled boundaries must be addressed by the horizontal line software since the X0 value has no effect in this submode.

This feature is useful for fast non-modulo 210 Y scrolling with quick reads/writes interleaved by old/new Y address updates. Note that when S = 1 in the Mode Register, the X0 value has no effect (the P nibble corresponds to X0 = 1 and the Q nibble corresponds to X0 = 0).

Reading of the DRAM data in this submode does not effect the X CDP count.

CVDG PARAMETER I/O ACCESS

Six CVDG Parameter Access modes allow the MPU to load control parameters into CVDG internal registers. Two of the modes also allow the MPU to read the parameter values from registers. The exact mode and access is controlled by the selected mode in the Mode Register and the register select input lines (A1 and A0).

Mode 1 — LUT Address

In Mode 1, data written to register address 3 (A1 = 1 and A0 = 1) is loaded into the LUT Address Register. Four bits control LUT write and read and the other four bits contain the actual LUT address. Bits 7–4 (XPE, RE, GE and BE) enable writing into, or reading from, corresponding sections of the LUT (i.e., XPAR, R, G and B) during Mode 2 access. Bits 3–0 in the register contain the LUT address (0–15) accessed during Mode 2.

				Bit Position							
Register	A1	A0	R/W	7	6	5	4	3	2	1	0
LUT Address	1	1	W	XPE	RE	GE	BE	A3	A2	A1	A0

DR7 Transparent Enable (XPE)

0 Disable XPAR write or read
1 Enable XPAR write or read

DR6 Red Enable (RE)

0 Disable R write or read
1 Enable R write or read

DR5 Green Enable (GE)

0 Disable G write or read
1 Enable G write or read

DR4 Blue Enable (BE)

0 Disable B write or read
1 Enable B write or read

DR3–DR0 LUT Address (A3–A0)

DR3 (A3)	DR2 (A2)	DR1 (A1)	DR0 (A0)	
0	0	0	0	LUT address 0
0	0	0	1	LUT address 1
	.		.	
1	1	1	1	LUT address 15

The LUT address in the LUT Address Register, rather than the LUT addresses read from DRAM, is also used to lookup the color level code in the LUT during the active display time (border and/or pixel) in two circumstances:

1. Outside the 256 × 210 graphics area, i.e., to generate the border color. Note that programs loading the LUT during the vertical blanking interval (VBI) must restore the address of the border color in the LUT into the LUT Address Register prior to unblanking.
2. Within the 256 × 210 graphics area when the LS bit = 0 in the Switch Register.

Mode 2 — LUT Data

In Mode 2, LUT data (i.e., color levels and transparent state) written to, or read from, register address 3 (A1 = 1, A0 = 1) is loaded into, or read from the LUT at the LUT address contained in the LUT Address Register. Only the section (R, G, B and/or XPAR codes) of the LUT entry enabled by bits 7–4 in the LUT Address Register are accessed. Normally only one enable bit at a time is set to a 1. During a write, data will be written into each LUT section enabled. During a read, ambiguous data will be accessed if more than one enable bit is set.

The transparent state (XPAR) is only one bit (D3). The other three data bits (D2–D0) are don't care.

During a write, the data on the A/D bus is written into the CVDG LUT Data Register. The LUT Address Generator latches the 4-bit LUT address from the LUT Data Register rather than from the Video Shift Register. The LUT Address Generator then generates the 16-bit binary address for routing to the LUT. The LUT is loaded in a similar manner as described for pixel color generation.

During a read, data is transferred from the LUT directly to the A/D bus without going through the LUT Data Register. XPAR is not availabe for readback.

				Bit Position							
Register	A1	A0	R/W	7	6	5	4	3	2	1	0
LUT Data*	1	1	R/W	—	—	—	—	D3	D2	D1	D0

*During a read, data is transferred directly from LUT to A/D bus without going through LUT Data Register.

DR7–DR4 Not used (no effect)

DR3–DR0 Color Level Code or Transparent Bit State

D3	D2	D1	D0	R, G or B Color Output Level
0	0	0	0	Color output level 0
0	0	0	1	Color output level 1
	.			.
	.			.
1	1	1		Color output level 15

D3	D2	D1	D0	XPAR Output Level
0	X	X	X	XPAR output LOW
1	X	X	X	XPAR output HIGH (X = no effect)

Mode 3 — Switch Register

In Mode 3, switch position data (represented by bit states) written to register address 3 (A1 = 1, A0 = 1) is loaded into the CVDG Switch Register. Three bits control video raster operation, one bit controls the LUT address access source, and one bit enables the CVDG test mode. All five bits are set to a 1 by power up.

				Bit Position							
Register	A1	A0	R/W	7	6	5	4	3	2	1	0
Switch	1	1	W	NHS	S21	EXT	LS	TST	—	—	—

DR7 Normal Horizontal Sync (NHS) Select

0 Early 15.9 kHz ($\overline{\text{HSYNC}}$) Output
1 Normal 15.7 kHz $\overline{\text{HSYNC}}$ Output

DR6 2:1 Interlace Select (S21)

0 1:1 interlace
1 2:1 interlace

DR5 External Sync Select (EXT)

0 Internal sync output on $\overline{\text{VSYNC}}$ ($\overline{\text{C/HSYNC}}$ output enabled.
1 External sync input on $\overline{\text{VSYNC}}$ ($\overline{\text{C/HSYNC}}$ output disabled)

DR4 LUT Address Select (LS)

0 Select the LUT Address Register as the LUT address source
1 Select Video Shift Register data as LUT address source

DR3 Test Mode Select (TST)

0 Normal mode; Vertical state machine (VSM) and Y address counter (YAC) run at normal rate
1 Test mode; VSM and YAC run at 1.413 MHz (used for factory test only)

Mode 4 — Y Scroll Register

In Mode 4, a Y scroll offset value written to register address 3 (A1 = 1, A0 = 1) is loaded into the Y Scroll Register. The Y scroll offset may vary from 0 to 209 (decimal). The value written defines the first horizontal row to be displayed at the top of the 256 x 210 graphics image area.

Register	A1	A0	R/W	Bit Position 7	6	5	4	3	2	1	0
Y Scroll	1	1	W	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0

DR7–DR0 Y Scroll Offset

0000000 Offset = 0
0000001 Offset = 1
. .
. .
. .
11010001 Offset = 209 (maximum allowed)

Mode 5 — Teletext DMA Pointer

In Mode 5, an 8-bit Teletext pointer written to register address 2 (A1 = 1, A0 = 0) is loaded into the TTX Pointer Register and Counter. The pointer, consisting of address bits A12–A5 specifies the starting address on a 32-byte boundary for the DMA transfer of teletext data into video page 3 of DRAM. During a teletext DMA data transfer, the Modulo 32 Teletext Counter is incremented by one upon each DMA byte transfer. The TTX Pointer Register is incremented by one every 32 bytes. The value of the Teletext Pointer can be read at any time in Mode 5.

Register	A1	A0	R/W	Bit Position 7	6	5	4	3	2	1	0
Teletext Pointer	1	0	R/W	A12	A11	A10	A9	A8	A7	A6	A5

The status of the P, V1 and V0 in the Mode/Status Register are unchanged during a Teletext DMA data transfer.

Mode 6 — Set DRAM Page

In Mode 6, data written to register address 3 (A1 = 1, A0 = 1) is loaded into the DRAM Page Register. The data contains a 3-bit DRAM page select code and five unused bits (don't care). These DRAM page select bits specify the 8k-byte DRAM page accessed during a MPU DRAM access ($\overline{DRCS}$ = low) when A13 input is LOW. The DRAM page bits can be read from the Status Register at any time.

Register	A1	A0	R/W	Bit Position 7	6	5	4	3	2	1	0
DRAM Page	1	1	W	—	—	—	—	—	P	V1	V0

DR7–DR3 Not Used (no effect)

DR2–DR0 Selected DRAM Page

DR2 (P)	DR1 (V1)	DR0 (V0)	
0	0	0	Video Page 0: 8k-byte video RAM
0	0	1	Video Page 1: 8k-byte video RAM
0	1	0	Video Page 2: 8k-byte video RAM
0	1	1	Video Page 3: 2.3k-byte video RAM; 5.9k-byte program RAM
1	0	0	Program Page 0: 16k-byte optional program RAM accessed via $\overline{DRCS}$ (additionally paged by A13 and A0 inputs)

MPU DRAM I/O ACCESS

When $\overline{DRCS}$ is LOW, the MPU directly accesses the DRAM in an address map manner. The MPU generates the DRAM row and column addresses (except for two column address lines which are driven by the CVDG). The CVDG drives the AD5 and AD6 lines during DRAM column address time and also outputs control signals ($\overline{RTIME}$, $\overline{CTIME}$ and $\overline{DTIME}$) to enable external A/D bus buffers. MPU address line A1–A8 are enabled onto A/D bus lines AD0–AD7, respectively, by $\overline{RTIME}$ to drive the DRAM row address. MPU address line A9–A12 are enabled onto A/D bus lines AD1–AD4, respectively, by $\overline{CTIME}$ to drive the DRAM column address. The CVDG drives AD5 and AD6 with one of two sets of signals during $\overline{CTIME}$. External bidirectional data line buffers are enabled by $\overline{DTIME}$ in the direction controlled by the MPU R/$\overline{W}$ output to transfer data between the MPU data bus lines D0–D7 and A/D bus lines AD0–AD7.

A13 input high causes program DRAM to be accessed during the processor portion of the A/D bus independent of the P bit value in the DRAM Page Register. $\overline{CASP}$ is asserted in response to the A13 HIGH to strobe the column address lines into program DRAM.

When A13 input is LOW, the section of DRAM accessed depends on the P bit value in the DRAM Page Register and the A0 input. If P = 0, video DRAM is accessed; $\overline{CAS1}$ is generated when A0 is LOW and $\overline{CAS2}$ is generated when A0 is HIGH. If P = 1, program DRAM is accessed since $\overline{CASP}$ is generated instead of $\overline{CAS1}$ or $\overline{CAS2}$ to strobe the DRAM column address.

The AD5 and AD6 outputs are driven by the CVDG during DRAM column address generation in the processor portion of the A/D bus cycle as controlled by the P bit in the DRAM Page Register. If video DRAM is selected (P = 0), the V0 and V1 bits in the DRAM Page Register are output on AD5 and AD6, respectively. If program DRAM is selected (P = 1), the A0 and A13 inputs are output on AD5 and AD6, respectively.

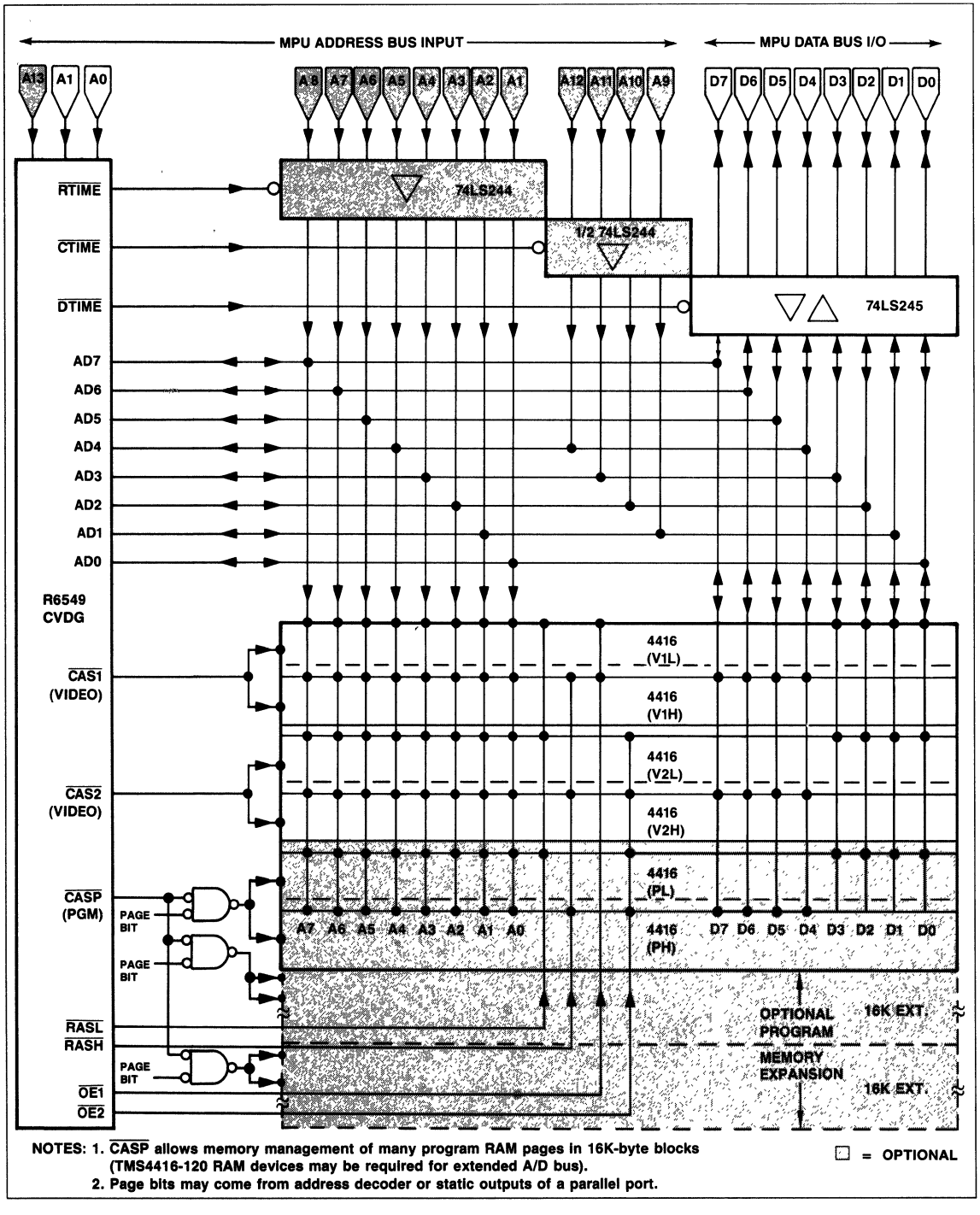
Note that the DRAM requires assertion of all three control signals for a valid access (i.e., $\overline{RAS}$, $\overline{CAS}$ and $\overline{OE}$ for a read and $\overline{RAS}$, $\overline{CAS}$ and $\overline{W}$ for a write). The CVDG sometimes outputs one or two of these signals but not all three control signals in "no access" situations.

TELETEXT DMA I/O ACCESS

Teletext data can be DMA transferred from a teletext prefix processor connected to the A/D bus to DRAM locations addressed by the CVDG. A 13-bit TTX Latch/Counter determines the DRAM address. The upper 8-bits of the TTX Counter is a latch. The value of the latch is defined by the TTX Pointer Register which can be loaded in Mode 5 by writing to register address 2 (A1 = 1 and A0 = 0). The TTX Pointer Register value therefore defines the TTX DMA starting address on a 32-byte boundary. The lower 5-bits of the TTX Latch/Counter is a modulo 32 counter. This counter increments by one after each TTX byte transfer. When the counter overflows (i.e., from 31 to 0) the upper count is incremented by one to increment the total address. The address is reset to zero during horizontal blanking. The upper count may be read from the TTX Pointer Register at any time in Mode 5.

TTX DMA transfer is initiated by asserting $\overline{\text{TTXREQ}}$ to the CVDG. The CVDG asserts TTX Output Enable ($\overline{\text{TTXOE}}$) to acknowledge $\overline{\text{TTXREQ}}$ receipt, suspends outputting the E and Q clocks for one cycle, outputs the 13-bit DRAM address and asserts DRAM Write Enable ($\overline{\text{W}}$) to enable writing into DRAM.

Note that DMA must be used only when the horizontal sync is genlocked to the external teletext raster.



NOTES: 1. $\overline{\text{CASP}}$ allows memory management of many program RAM pages in 16K-byte blocks (TMS4416-120 RAM devices may be required for extended A/D bus).
2. Page bits may come from address decoder or static outputs of a parallel port.

□ = OPTIONAL

Figure 6. CVDG Connection to A/D Bus and DRAM

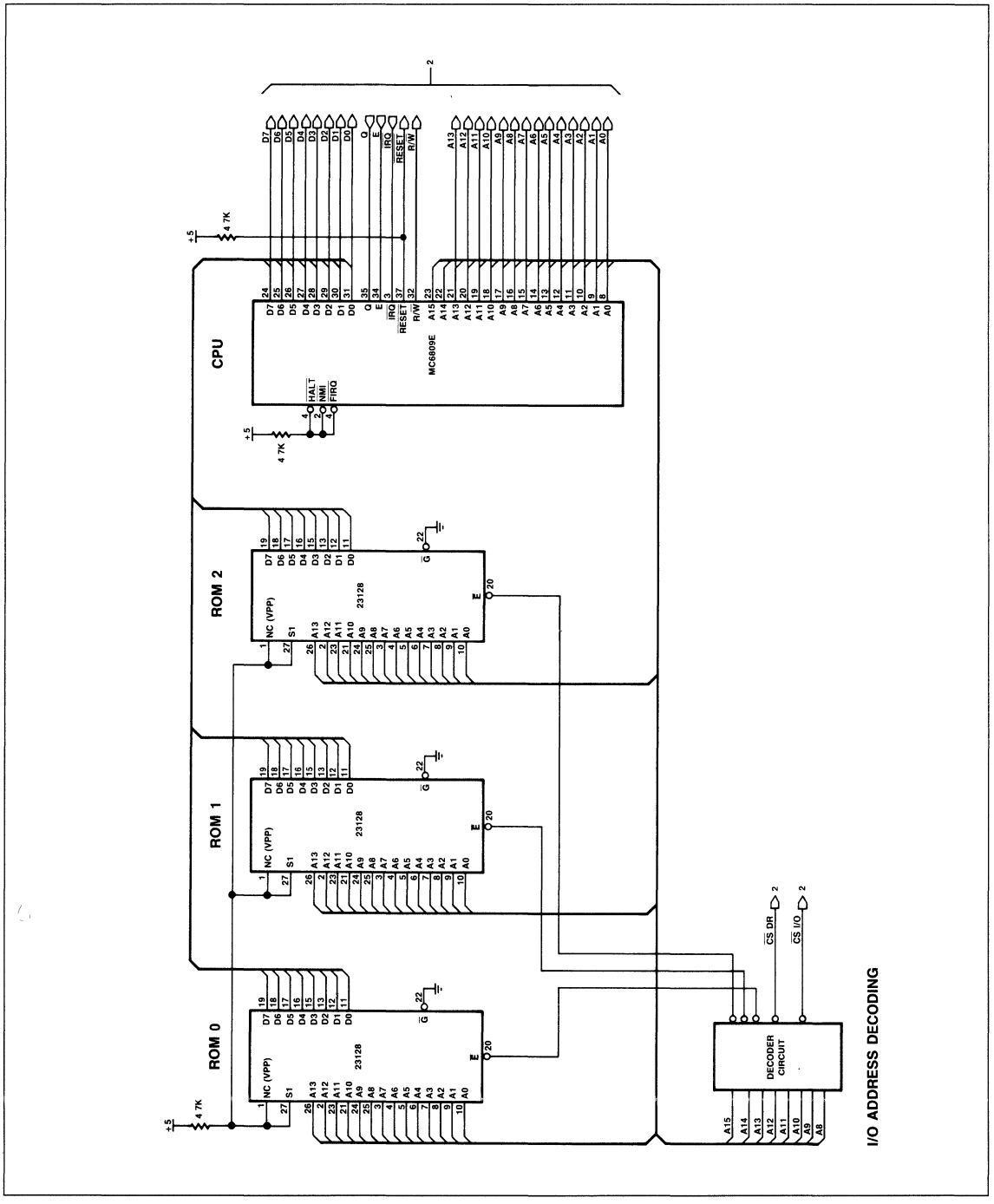


Figure 7. CVDG Application Schematic (Typical) (Sheet 1 of 2)

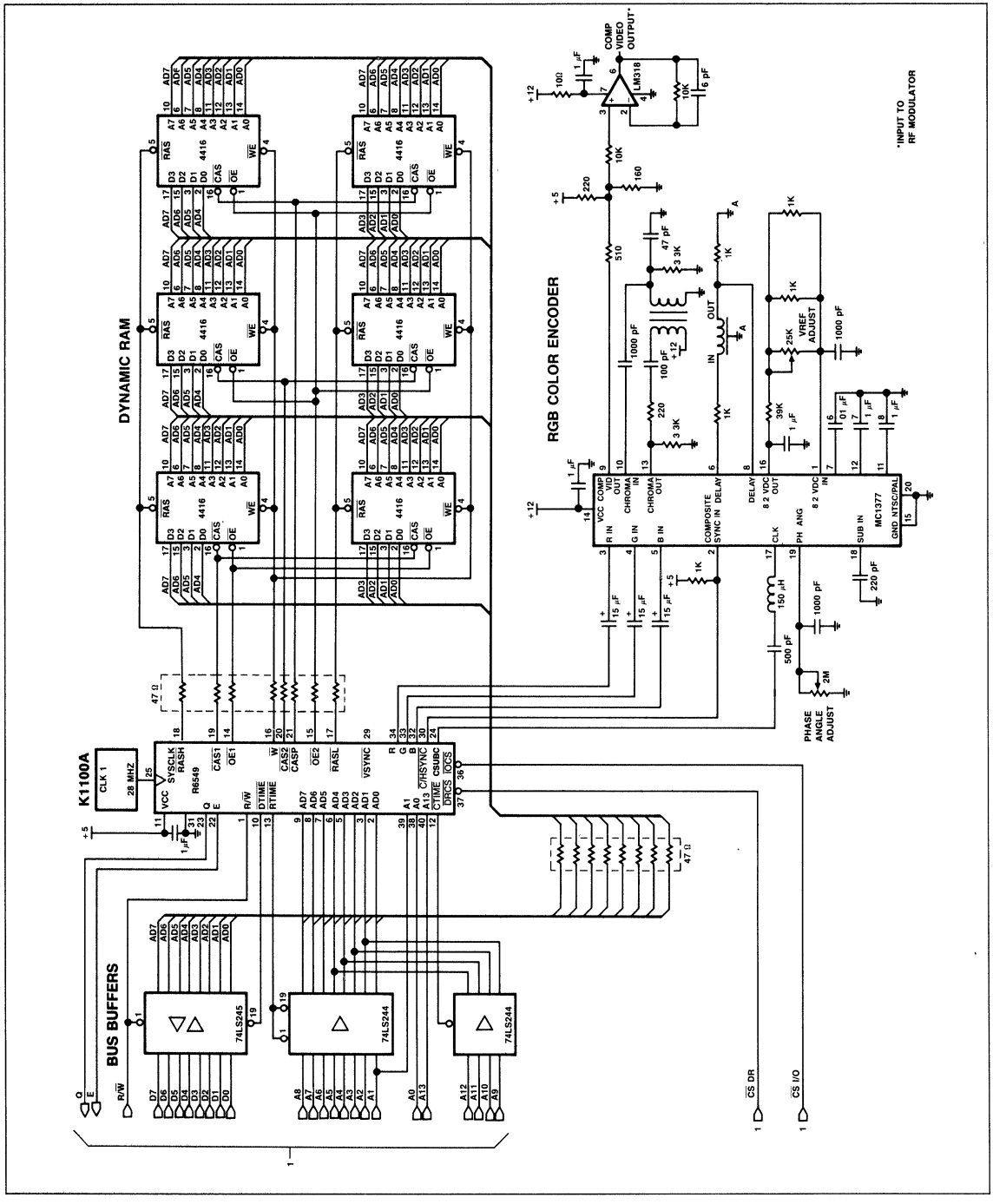


Figure 7. CVDG Application Schematic (Typical) (Sheet 2 of 2)

AC CHARACTERISTICS

(V_{CC} = 5.0V ±5%, V_{SS} = 0)

MPU CLOCK AND CONTROL LINE TIMING

Ref. Fig. 8 No.	Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
1	t_{ECYC}	E Cycle Time	700	698		ns	1
2	t_r, t_f	E and Q Rise and Fall		25		ns	
3	t_{ELEH}	E Low to E High		350		ns	
4	t_{EHEL}	E High to E Low		350		ns	
5	t_{ELQH}	E Low to Q Rising		175		ns	
6	t_{QHEH}	Q High to E Rising		175		ns	
7	t_{EHQL}	E High to Q Falling		175		ns	
8	t_{QLEL}	Q Low to E Falling		175		ns	
9	t_{SLEH}	Chip Select Low to E Rising (Setup)		70		ns	
10	t_{SHEH}	Chip Select High to E Rising (Hold)		0		ns	
11	t_{EHQV}	E High to Data Valid (Read)			240	ns	
12	t_{ELQZ}	E Low to Output High Z (Read)		10		ns	
13	t_{DVEL}	Data Valid to E Falling (Write)	100			ns	
14	t_{ELDZ}	E Falling to Data Invalid (Write)		30		ns	

Note:
1. Based on 28.636363 MHz SYSCLK input.

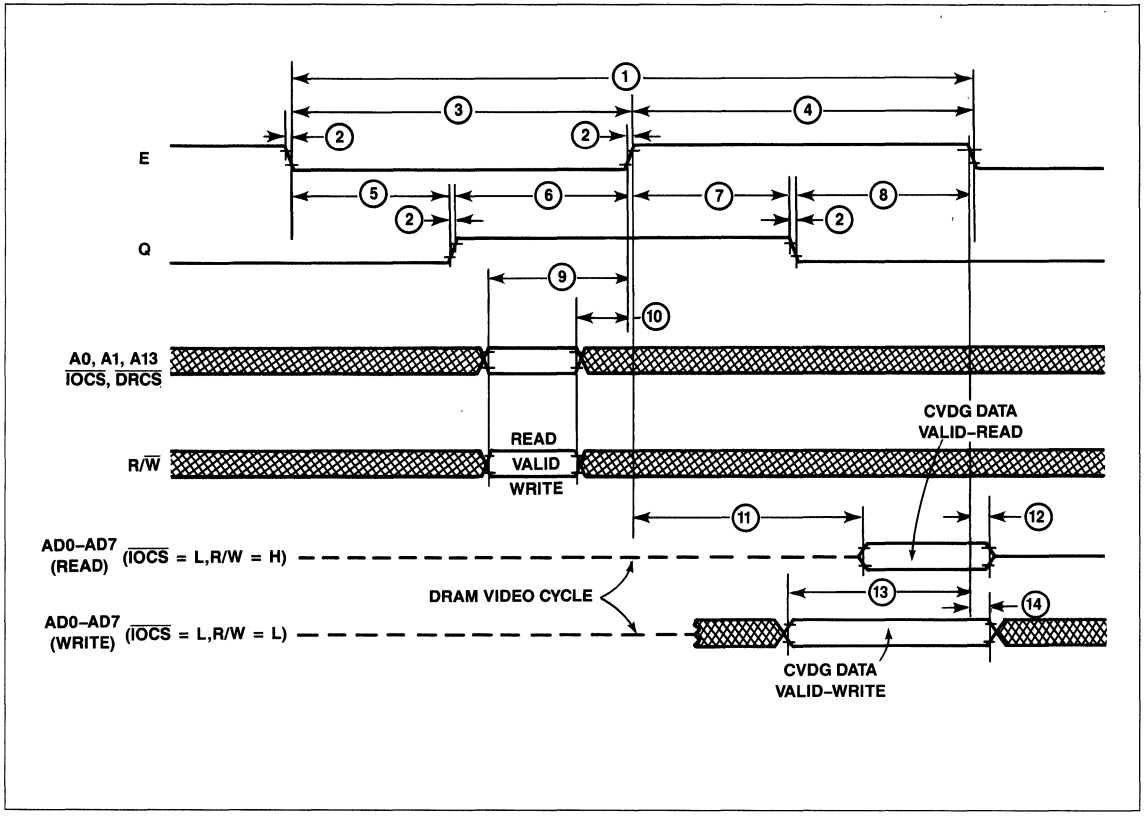


Figure 8. CVDG-MPU A/D Bus Timing Waveforms

DRAM TIMING — VIDEO ACCESS CYCLE

Ref. Fig. 9 No.	Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
1	t_{RLRTL}	$\overline{RAS}$ Low to $\overline{RTIME}$ Low (Delay)		315		ns	
2	t_{RTLRTH}	$\overline{RTIME}$ Low to $\overline{RTIME}$ High		70		ns	
3	t_{RLCTL}	$\overline{RAS}$ Low to $\overline{CTIME}$ Low (Delay)		35		ns	
4	t_{CTLCTH}	$\overline{CTIME}$ Low to $\overline{CTIME}$ High		87		ns	
5	t_{RLDTL}	$\overline{RAS}$ Low to $\overline{DTIME}$ Low (Delay)		122		ns	
6	t_{DTLDTH}	$\overline{DTIME}$ Low to $\overline{DTIME}$ High		157		ns	
7	t_{RC}	RAM Read/Write Cycle		350		ns	
8	t_{RP}	$\overline{RAS}$ High Width		105		ns	
9	t_{RAS}	$\overline{RAS}$ Low Width		245		ns	
10	t_{RCD}	$\overline{RAS}$ Low to $\overline{CAS}$ Low (Delay)		70		ns	
11	t_{CAS}	$\overline{CAS}$ Low Width		245		ns	
12	t_{CSH}	$\overline{RAS}$ Low to $\overline{CAS}$ Rising (Delay)		315		ns	
13	t_{RSH}	$\overline{CAS}$ Low to $\overline{RAS}$ Rising (Delay)		175		ns	
14	t_{CPN}	$\overline{CAS}$ High Width		105		ns	
15	t_{CRP}	$\overline{CAS}$ High to $\overline{RAS}$ Falling (Delay)		35		ns	
16	t_t	$\overline{RAS}$ and $\overline{CAS}$ Transition Times		5		ns	
17	t_{RCS}	Read Command Setup		105		ns	
18	t_{ASR}	Row Address Setup		35		ns	
19	t_{RAH}	Row Address Hold		35		ns	
20	t_{ASC}	Column Address Setup		35		ns	
21	t_{CAH}	Column Address Hold		70		ns	
22	t_{AR}	$\overline{RAS}$ Low to Column Hold		140		ns	
23	t_{RAC}	$\overline{RAS}$ Low to Data Valid (Setup)			150	ns	
24	t_{CAC}	$\overline{CAS}$ Low to Data Valid (Setup)			80	ns	
25	t_{RLG1L}	$\overline{RAS}$ Low to $\overline{OE1}$ Low (Delay)		140		ns	
26	t_{GLGHr}	$\overline{OE}$ Low to $\overline{OE}$ High		70		ns	
27	t_{OEA}	$\overline{OE}$ Low to Data Valid (Setup)	0		40	ns	
28	t_{OEZ}	$\overline{OE}$ High to Output High Z (Hold)	0		35	ns	
29	t_{RLG2L}	$\overline{RAS}$ Low to $\overline{OE2}$ Low (Delay)		210		ns	

DRAM TIMING — MPU DRAM ACCESS CYCLE

Ref. Fig. 9 No.	Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
30	t_{RRH}	Read Command Hold After $\overline{RAS}$ High		280		ns	
31	t_{RCH}	Read Command Hold After $\overline{CAS}$ High		210		ns	
33	t_{GLGH}	$\overline{OE1}$, $\overline{OE2}$ Low to $\overline{OE1}$, $\overline{OE2}$ High		140		ns	
36	t_{DS}	Data Setup		12		ns	
37	t_{WP}	$\overline{W}$ Low to $\overline{W}$ High		140		ns	
38	t_{DH}	Data Hold After $\overline{W}$ Low		70		ns	
39	t_{DHC}	Data Hold After $\overline{CAS}$ Low		175		ns	
40	t_{DHR}	Data Hold After $\overline{RAS}$ Low		245		ns	
41	t_{WCR}	Write Command Hold After $\overline{RAS}$ Low		315		ns	
42	t_{WCH}	Write Command Hold After $\overline{CASP}$ Low		245		ns	
43	t_{RWL}	Write Command Setup before $\overline{RAS}$ Rising		70		ns	
44	t_{CWL}	Write Command Setup before $\overline{CAS}$ Rising		140		ns	

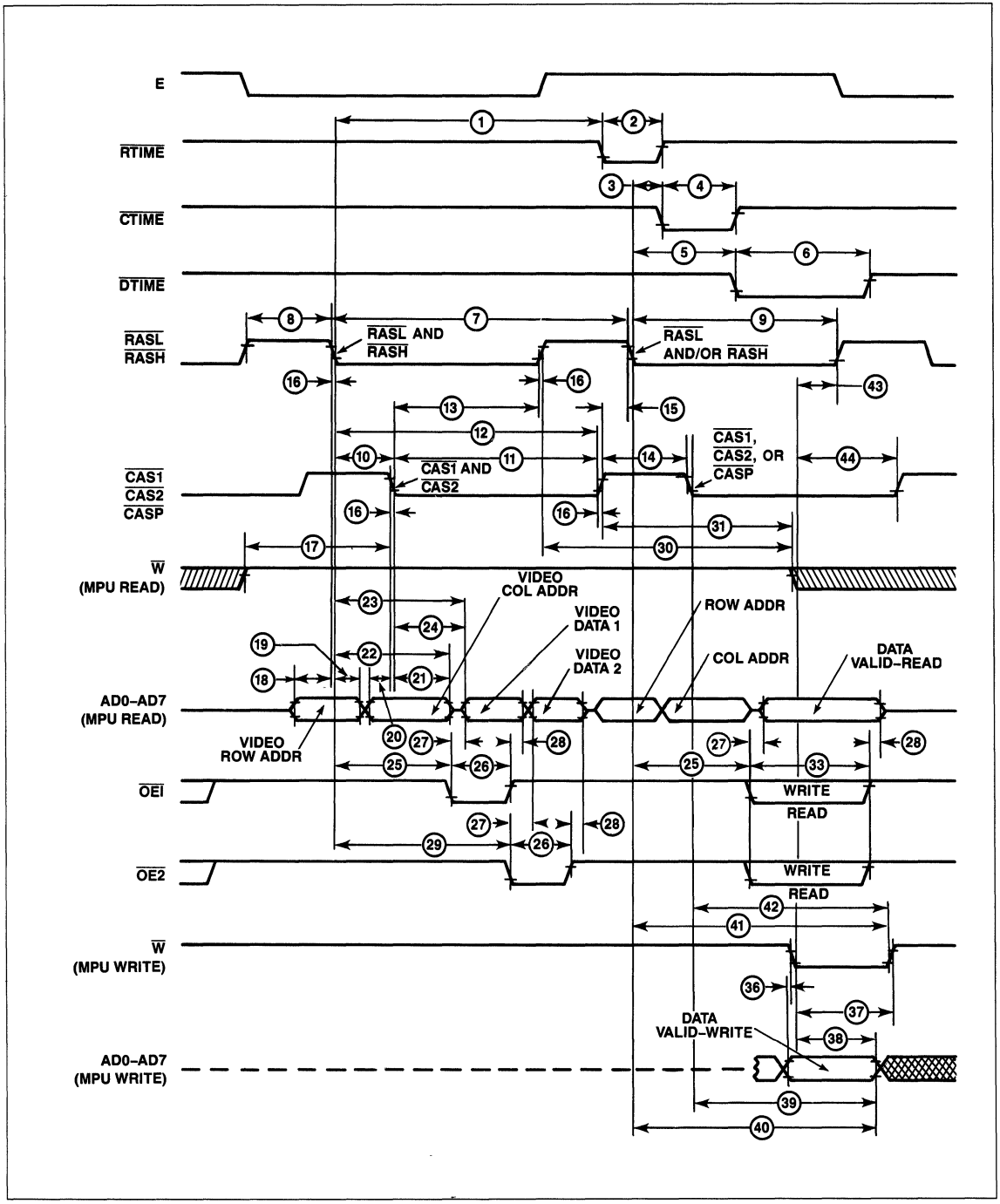


Figure 9. CVDG-DRAM A/D Bus Timing Waveforms

TELETEXT DMA CYCLE TIMING

Ref. Fig. 10 No.	Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
1	t_{RLEL}	$\overline{TTXREQ}$ Low to E Low (Setup)		80		ns	
2	t_{ELRH}	E Low to $\overline{TTXREQ}$ High (Hold)		10		ns	
3	t_{ELGL}	E Low to $\overline{TTXOE}$ Low		595		ns	
4	t_{GLGH}	$\overline{TTXOE}$ Low to $\overline{TTXOE}$ High		140		ns	

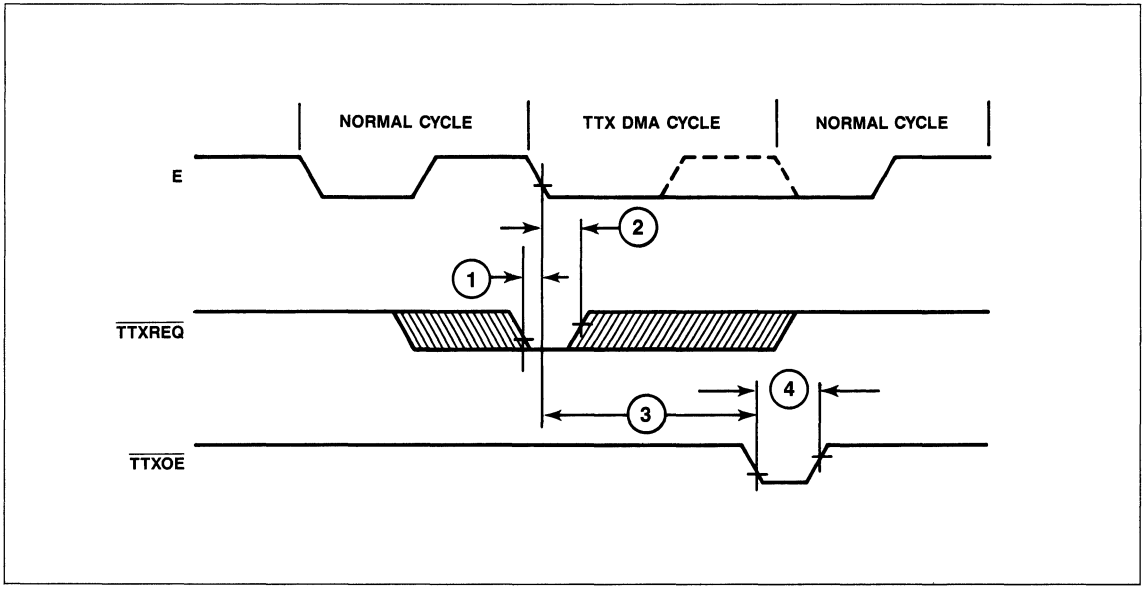


Figure 10. Teletext Prefix Processor — CVDG Timing Waveforms

HORIZONTAL VIDEO TIMING

Ref. Fig. 11 No.	Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
1		H Sync to Setup	9.3	9.4	9.5	μs	1
2		H Front Porch	1.4	1.5	1.6	μs	1
3		H Sync to XPAR	—	10.16	—	μs	2
4		XPAR Front Porch	—	2.79	—	μs	2
5		H Sync to Border 1	—	8.38	—	μs	2
6		H Sync to Graphics	—	12.57	—	μs	2
7		H Sync to Border 2	—	57.27	—	μs	2
8		Border Front Porch	—	2.79	—	μs	2
9		H Sync Tip	—	4.81	—	μs	2
10		H Period (Normal)	—	63.556	—	μs	2
11		H Period (Early)	—	62.857	—	μs	2

Notes: 1. RS-170A Specification (shown for reference only).
2 ±0.1μs, based on 28.636363 MHz SYSCLK input.

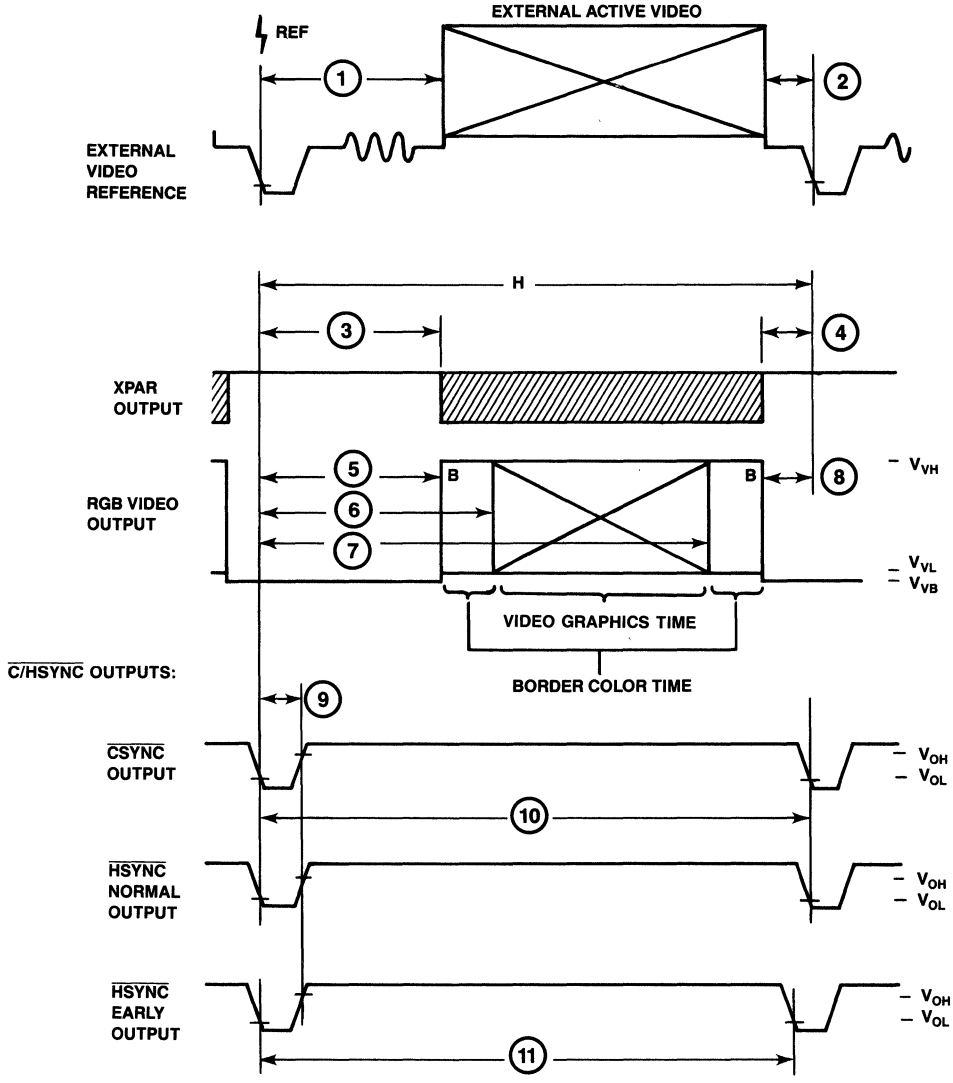


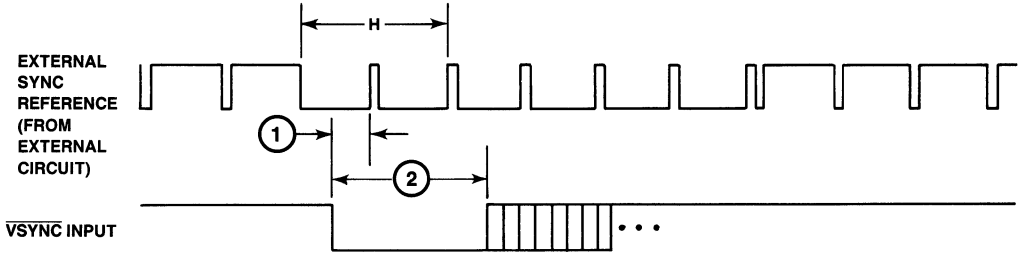
Figure 11. Horizontal Video Output Timing Waveforms

Vertical Cycle Timing

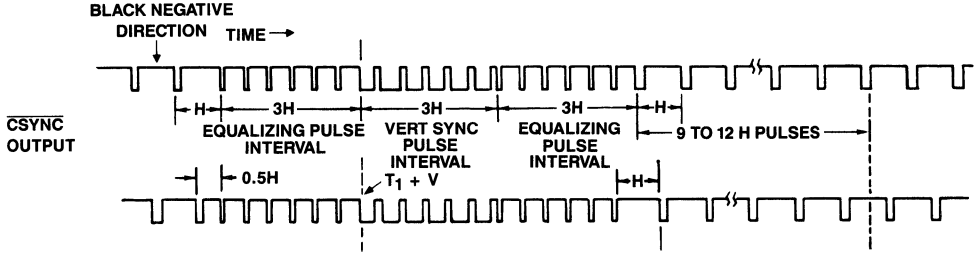
Ref. Fig. 12 No.	Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
1	V_{SU}	$\overline{VSYNC}$ Low Input to First Serration Setup	20	—	—	ns	3
2	V_H	$\overline{VSYNC}$ Low Input Pulse Duration	63.5	—	—	μs	3
—		$\overline{VSYNC}$ Low Output Pulse Duration (Burst Blank)	19	—	—	H	1
—		V Blank Duration	52	—	—	H	1
—		V Unblank to Graphics Duration (Top Border)	21	—	—	H	1
—		Graphics to V Blank Duration (Bottom Border)	31	—	—	H	1, 2

Notes: 1. H = $\overline{HSYNC}$ pulse width (63.5 μs)
2. 2 1 interlace mode
3. Shown for reference only—not an R6549 requirement

2



a. Vertical Synchronization



b. RS-170A Composite Sync VBI Timing Specifications

Figure 12. Vertical Cycle Waveforms—2:1 Interlace

TELETEXT DMA CYCLE TIMING

Ref. Fig. 13 No.	Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
1	t_{ELPL}	E Low to PIXCK High		0		ns	
2	t_{PHPL}	PIXCK High to PIXCK Low		70		ns	
3	t_{PLPH}	PIXCK Low to PIXCK High		105		ns	
4	t_{PCYC}	PIXCK Cycle		175		ns	

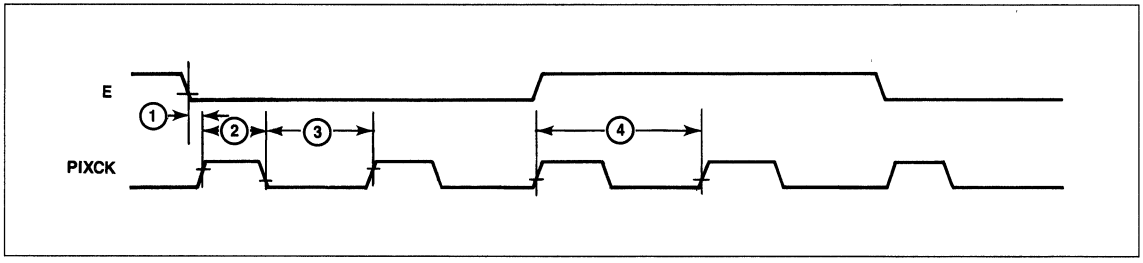


Figure 13. Video Output Waveforms

DC CHARACTERISTICS

(V_{CC} = 5.0V ±5%, V_{SS} = 0V, T_A = 0°C to 70°C, unless otherwise noted)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Input High Voltage					V	
SYSCLK	V_{IHC}	V_{CC} - 0.75	—	V_{CC}		
IOCS, DRCS, TTXREQ, A0, A1, A13, R/W, VSYNC, AD0-AD7	V_{IH}	V_{SS} + 2.0	—	V_{CC}		
Input Low Voltage					V	
SYSCLK	V_{ILC}	V_{SS} - 0.3	—	V_{SS} + 0.4		
IOCS, DRCS, TTXREQ, A0, A1, A13, R/W VSYNC, AD0-AD7	V_{IL}	V_{SS} - 0.3	—	V_{SS} + 0.8		
Input Leakage Current	I_{IL}	—	—	±10	μA	V_{IN} = 0V to 5.25V V_{CC} = 0
Output High Voltage	V_{OH}				V	V_{CC} = 4.75V
E		V_{CC} - 0.75	—	—		I_{OH} = -0.14 mA Note 1
Q, RTIME, CTIME, DTIME, RASL, RASH, W CAS1, CAS2, CASP, OE1, OE2, TTXOE, C/HSYNC, VSYNC, CSUBC, PIXCK, XPAR		V_{SS} + 2.4	—	—		I_{OH} = -80 μA Note 2
AD0-AD7		V_{SS} + 2.4	—	—		I_{OH} = -170 μA Note 3
Output Low Voltage	V_{OL}				V	V_{CC} = 4.75V
E		—	—	V_{SS} + 0.4		I_{OL} = 1.7 mA Note 1
Q, RTIME, CTIME, DTIME, RASL, RASH, W, CAS1, CAS2, CASP, OE1, OE2, TTXOE, C/HSYNC, VSYNC, CSUBC, PIXCK, XPAR		—	—	V_{SS} + 0.4		I_{OL} = 1.6 mA Note 2
AD0-AD7		—	—	V_{SS} + 0.4		I_{OL} = 3.0 mA Note 3
Output Leakage Current (Off-State) AD0-AD7	I_{OFF}	—	—	±20	μA	V_{IN} = 0 to 5.25V
Output High Voltage R, G, B	V_{VH}	—	+2.800	—	V	C_L = 30 pF R_L = 10K Ohms t_r/t_f = 50 ns
Output Low Voltage R, G, B	V_{VL}	—	+1.875	—	V	
Output Blanking Voltage R, G, B	V_{VB}	—	+1.800	—	V	
Input Capacitance[4]	C_{IN}				pF	V_{CC} = 5.0V, chip
SYSCLK		—	—	10		deselected, pin
IOCS, DRCS, TTXREQ, A0, A1, A13, R/W, VSYNC, AD0-AD7		—	—	5		Under test at 0V, T_A = 25°C, f = 0.986 MHz (SYSCLK = 28.6363 MHz)

Notes:
1. Output Load: 1 TTL gate; C_L = 140 pF
2. Output Load: 1 TTL gate; C_L = 100 pF
3. Output Load: 6 DRAM, 2 LS244 buffers and 1 LS245 transceiver; C_L = 180 pF
4. This parameter is periodically sampled and is not 100% tested.

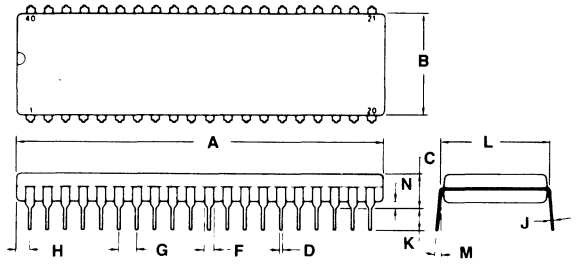
ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to +7.0	V
Input Voltages	V_{IN}	−0.3 to +7.0	V
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{STG}	−55 to +150	°C

***NOTE:** Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the other sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PACKAGE DIMENSIONS

40-PIN PLASTIC DIP



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	51.28	52.32	2.040	2 060
B	13.72	14.22	0.540	0 560
C	3.55	5.08	0.140	0 200
D	0.36	0 51	0.014	0.020
F	1.02	1 52	0 040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2 16	0.065	0.085
J	0.20	0.30	0.008	0.012
K	3 05	3.56	0.120	0.140
L	15 24 BSC		0.600 BSC	
M	7°	10°	7°	10°
N	0.51	1.02	0.020	0 040

Rockwell

R6551
ASYNCHRONOUS COMMUNICATIONS INTERFACE ADAPTER (ACIA)

DESCRIPTION

The Rockwell R6551 Asynchronous Communications Interface Adapter (ACIA) provides an easily implemented, program controlled interface between 8-bit microprocessor-based systems and serial communication data sets and modems.

The ACIA has an internal baud rate generator. This feature eliminates the need for multiple component support circuits, a crystal being the only other part required. The Transmitter baud rate can be selected under program control to be either 1 of 15 different rates from 50 to 19,200 baud, or at $^1/_{16}$ times an external clock rate. The Receiver baud rate may be selected under program control to be either the Transmitter rate, or at $^1/_{16}$ times the external clock rate. The ACIA has programmable word lengths of 5, 6, 7, or 8 bits; even, odd, or no parity; 1, 1½, or 2 stop bits.

The ACIA is designed for maximum programmed control from the microprocessor (MPU), to simplify hardware implementation. Three separate registers permit the MPU to easily select the R6551's operating modes and data checking parameters and determine operational status.

The Command Register controls parity, receiver echo mode, transmitter interrupt control, the state of the $\overline{RTS}$ line, receiver interrupt control, and the state of the $\overline{DTR}$ line.

The Control Register controls the number of stop bits, word length, receiver clock source, and baud rate.

The Status Register indicates the states of the $\overline{IRQ}$, $\overline{DSR}$, and $\overline{DCD}$ lines, Transmitter and Receiver Data Registers, and Overrun, Framing, and Parity Error conditions.

The Transmitter and Receiver Data Registers are used for temporary data storage by the ACIA Transmit and Receiver circuits.

ORDERING INFORMATION

Part No.: R6551___

- Temperature Range (T_L to T_H):
  - Blank = 0°C to +70°C
  - E = −40°C to +85°C
- Package:
  - C = Ceramic
  - P = Plastic
- Frequency Range:
  - No Letter = 1 MHz
  - A = 2 MHz

FEATURES

- Compatible with 8-bit microprocessors
- Full duplex operation with buffered receiver and transmitter
- Data set/modem control functions
- Internal baud rate generator with 15 programmable baud rates (50 to 19,200)
- Program-selectable internally or externally controlled receiver rate
- Programmable word lengths, number of stop bits, and parity bit generation and detection
- Programmable interrupt control
- Program reset
- Program-selectable serial echo mode
- Two chip selects
- 2 or 1 MHz operation
- 5.0 Vdc ± 5% supply requirements
- 28-pin plastic or ceramic DIP
- Full TTL compatibility
- Compatible with R6500, R6500/* and R65C00 microprocessors

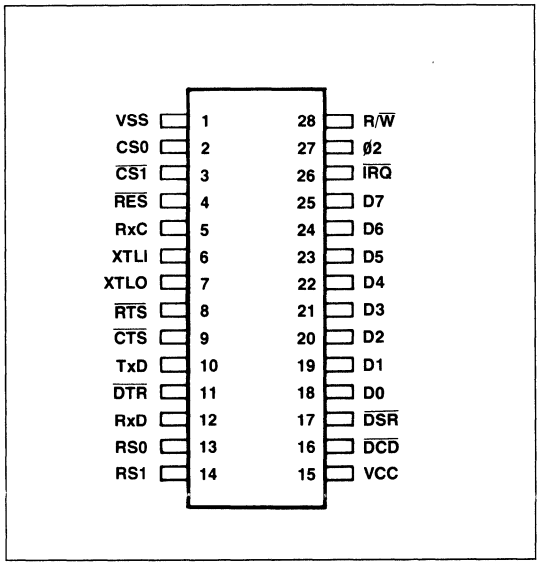


Figure 1. R6551 ACIA Pin Configuration

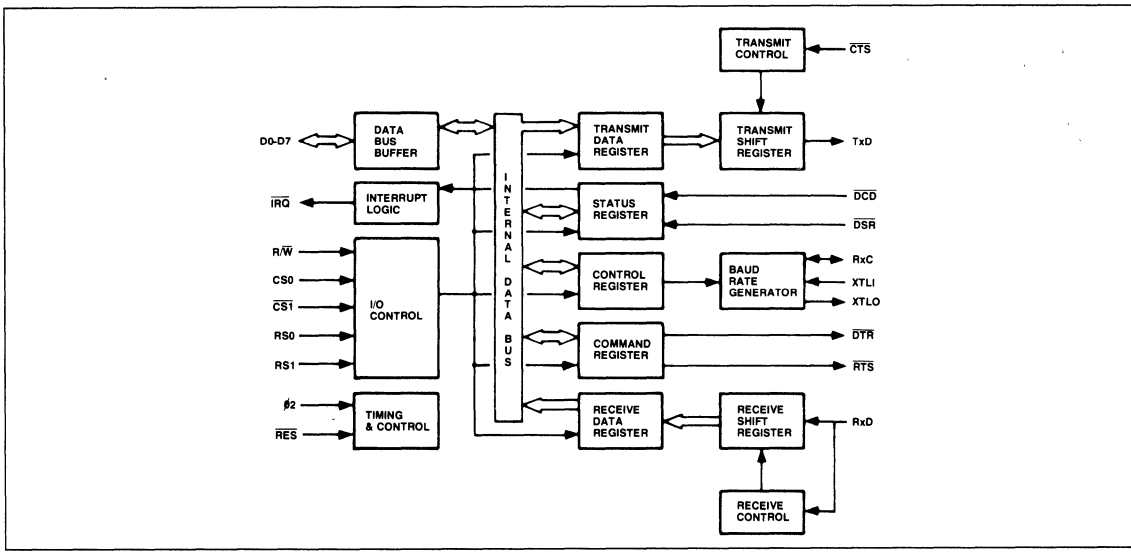


Figure 2. ACIA Internal Organization

FUNCTIONAL DESCRIPTION

A block diagram of the ACIA is presented in Figure 2 followed by a description of each functional element of the device.

DATA BUS BUFFERS

The Data Bus Buffer interfaces the system data lines to the internal data bus. The Data Bus Buffer is bi-directional. When the R/$\overline{W}$ line is low and the chip is selected, the Data Bus Buffer writes the data from the system data lines to the ACIA internal data bus. When the R/$\overline{W}$ line is high and the chip is selected, the Data Bus Buffer drives the data from the internal data bus to the system data bus.

INTERRUPT LOGIC

The Interrupt Logic will cause the $\overline{IRQ}$ line to the microprocessor to go low when conditions are met that require the attention of the microprocessor. The conditions which can cause an interrupt will set bit 7 and the appropriate bit of bits 3 through 6 in the Status Register, if enabled. Bits 5 and 6 correspond to the Data Carrier Detect ($\overline{DCD}$) logic and the Data Set Ready ($\overline{DSR}$) logic. Bits 3 and 4 correspond to the Receiver Data Register full and the Transmitter Data Register empty conditions. These conditions can cause an interrupt request if enabled by the Command Register.

I/O CONTROL

The I/O Control Logic controls the selection of internal registers in preparation for a data transfer on the internal data bus and the direction of the transfer to or from the register.

The registers are selected by the Receiver Select (RS1, RS0) and Read/Write (R/$\overline{W}$) lines as described later in Table 1.

TIMING AND CONTROL

The Timing and Control logic controls the timing of data transfers on the internal data bus and the registers, the Data Bus Buffer, and the microprocessor data bus, and the hardware reset features.

Timing is controlled by the system Ø2 clock input. The chip will perform data transfers to or from the microcomputer data bus during the Ø2 high period when selected.

All registers will be initialized by the Timing and Control Logic when the Reset ($\overline{RES}$) line goes low. See the individual register description for the state of the registers following a hardware reset.

TRANSMITTER AND RECEIVER DATA REGISTERS

These registers are used as temporary data storage for the ACIA Transmit and Receive Circuits. Both the Transmitter and Receiver are selected by a Register Select 0 (RS0) and Register Select 1 (RS1) low condition. The Read/Write (R/$\overline{W}$) line determines which actually uses the internal data bus; the Transmitter Data Register is write only and the Receiver Data Register is read only.

Bit 0 is the first bit to be transmitted from the Transmitter Data Register (least significant bit first). The higher order bits follow in order. Unused bits in this register are "don't care".

The Receiver Data Register holds the first received data bit in bit 0 (least significant bit first). Unused high-order bits are "0". Parity bits are not contained in the Receiver Data Register. They are stripped off after being used for parity checking.

STATUS REGISTER

The Status Register indicates the state of interrupt conditions and other non-interrupt status lines. The interrupt conditions are the Data Set Ready, Data Carrier Detect, Transmitter Data Register Empty and Receiver Data Register Full as reported in bits 6 through 3, respectively. If any of these bits are set, the Interrupt (IRQ) indicator (bit 7) is also set. Overrun, Framing Error, and Parity Error are also reported (bits 2 through 0 respectively).

7	6	5	4	3	2	1	0
IRQ	$\overline{DSR}$	$\overline{DCD}$	TDRE	RDRE	OVRN	FE	PE

Bit 7 **Interrupt (IRQ)**
- 0 No interrupt
- 1 Interrupt has occurred

Bit 6 **Data Set Ready ($\overline{DSR}$)**
- 0 $\overline{DSR}$ low (ready)
- 1 $\overline{DSR}$ high (not ready)

Bit 5 **Data Carrier Detect ($\overline{DCD}$)**
- 0 $\overline{DCD}$ low (detected)
- 1 $\overline{DCD}$ high (not detected)

Bit 4 **Transmitter Data Register Empty**
- 0 Not empty
- 1 Empty

Bit 3 **Receiver Data Register Full**
- 0 Not full
- 1 Full

Bit 2 **Overrun***
- 0 No overrun
- 1 Overrun has occurred

Bit 1 **Framing Error***
- 0 No framing error
- 1 Framing error detected

Bit 0 **Parity Error***
- 0 No parity error
- 1 Parity error detected

*No interrupt occurs for these conditions

Reset Initialization

7	6	5	4	3	2	1	0	
0	—	—	1	0	0	0	0	**Hardware reset**
—	—	—	—	—	0	—	—	**Program reset**

Parity Error (Bit 0), Framing Error (Bit 1), and Overrun (2)

None of these bits causes a processor interrupt to occur, but they are normally checked at the time the Receiver Data Register is read so that the validity of the data can be verified. These bits are self clearing (i.e., they are automatically cleared after a read of the Receiver Data Register).

Receiver Data Register Full (Bit 3)

This bit goes to a 1 when the ACIA transfers data from the Receiver Shift Register to the Receiver Data Register, and goes to a 0 (is cleared) when the processor reads the Receiver Data Register.

Transmitter Data Register Empty (Bit 4)

This bit goes to a 1 when the ACIA transfers data from the Transmitter Data Register to the Transmitter Shift Register, and goes to a 0 (is cleared) when the processor writes new data onto the Transmitter Data Register.

Data Carrier Detect (Bit 5) and Data Set Ready (Bit 6)

These bits reflect the levels of the $\overline{DCD}$ and $\overline{DSR}$ inputs to the ACIA. A 0 indicates a low level (true condition) and a 1 indicates a high level (false). Whenever either of these inputs change state, an immediate processor interrupt (IRQ) occurs, unless bit 1 of the Command Register (IRD) is set to a 1 to disable $\overline{IRQ}$. When the interrupt occurs, the status bits indicate the levels of the inputs immediately after the change of state occurred. Subsequent level changes will not affect the status bits until the Status Register is interrogated by the processor. At that time, another interrupt will immediately occur and the status bits reflect the new input levels. These bits are not automatically cleared (or reset) by an internal operation.

Interrupt (Bit 7)

This bit goes to a 1 whenever an interrupt condition occurs and goes to a 0 (is cleared) when the Status Register is read.

CONTROL REGISTER

The Control Register selects the desired baud rate, frequency source, word length, and the number of stop bits.

7	6	5	4	3	2	1	0
SBN	WL		RCS	SBR			
	WL1	WL0		SBR3	SBR2	SBR1	SBR0

Bit 7 — Stop Bit Number (SBN)

0	1 Stop bit
1	2 Stop bits
1	1½ Stop bits For WL = 5 and no parity
1	1 Stop bit For WL = 8 and parity

Bits 6-5 — Word Length (WL)

6	5	No. Bits
0	0	8
0	1	7
1	0	6
1	1	5

Bit 4 — Receiver Clock Source (RCS)

0	External receiver clock
1	Baud rate

Bits 3-0 — Selected Baud Rate (SBR)

3	2	1	0	Baud
0	0	0	0	16x External Clock
0	0	0	1	50
0	0	1	0	75
0	0	1	1	109.92
0	1	0	0	134.58
0	1	0	1	150
0	1	1	0	300
0	1	1	1	600
1	0	0	0	1200
1	0	0	1	1800
1	0	1	0	2400
1	0	1	1	3600
1	1	0	0	4800
1	1	0	1	7200
1	1	1	0	9600
1	1	1	1	19,200

Reset Initialization

7	6	5	4	3	2	1	0	
0	0	0	0	0	0	0	0	Hardware reset ($\overline{RES}$)
–	–	–	–	–	–	–	–	Program reset

Selected Baud Rate (Bits 0, 1, 2, 3)

These bits select the Transmitter baud rate, which can be at $^1/_{16}$ an external clock rate or one of 15 other rates controlled by the internal baud rate generator

If the Receiver clock uses the same baud rate as the transmitter. then RxC becomes an output and can be used to slave other circuits to the ACIA. Figure 3 shows the Transmitter and Receiver layout.

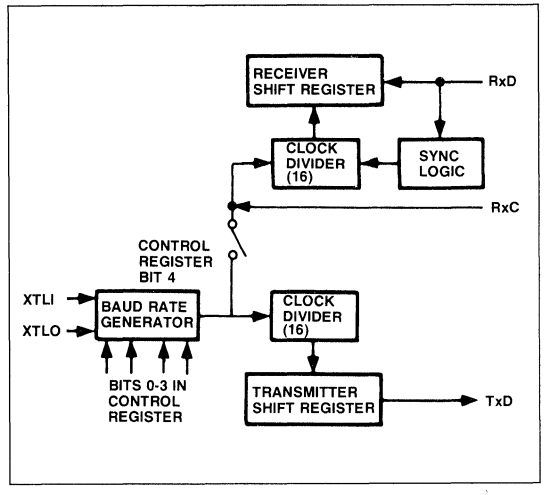


Figure 3. Transmitter/Receiver Clock Circuits

Receiver Clock Source (Bit 4)

This bit controls the clock source to the Receiver. A 0 causes the Receiver to operate at a baud rate of $^1/_{16}$ an external clock. A 1 causes the Receiver to operate at the same baud rate as is selected for the transmitter

Word Length (Bits 5, 6)

These bits determine the word length to be used (5, 6, 7 or 8 bits).

Stop Bit Number (Bit 7)

This bit determines the number of stop bits used. A 0 always indicates one stop bit. A 1 indicates 1½ stop bits if the word length is 5 with no parity selected, 1 stop bit if the word length is 8 with parity selected, or 2 stop bits in all other configurations.

COMMAND REGISTER

The Command Register controls specific modes and functions.

7	6	5	4	3	2	1	0
PMC		PME	REM	TIC		IRD	DTR
PMC1	PMC0			TIC1	TIC0		

Bits 7-6 Parity Mode Control (PMC)

7	6	
0	0	Odd parity transmitted/received
0	1	Even parity transmitted/received
1	0	Mark parity bit transmitted Parity check disabled
1	1	Space parity bit transmitted Parity check disabled

Bit 5 Parity Mode Enabled (PME)

0	Parity mode disabled No parity bit generated Parity check disabled
1	Parity mode enabled

Bit 4 Receiver Echo Mode (REM)

0	Receiver normal mode
1	Receiver echo mode bits 2 and 3 Must be zero for receiver echo mode, $\overline{RTS}$ will be low.

Bits 3-2 Transmitter Interrupt Control (TIC)

3	2	
0	0	$\overline{RTS}$ = High, transmitter disabled
0	1	$\overline{RTS}$ = Low, transmit interrupt enabled
1	0	$\overline{RTS}$ = Low, transmit interrupt disabled
1	1	$\overline{RTS}$ = Low, transmit interrupt disabled transmit break on TxD

Bit 1 Receiver Interrupt Request Disabled (IRD)

0	$\overline{IRQ}$ enabled (receiver)
1	$\overline{IRQ}$ disabled (receiver)

Bit 0 Data Terminal Ready (DTR)

0	Data terminal not ready ($\overline{DTR}$ high)*
1	Data terminal ready ($\overline{DTR}$ low)

NOTE

*The transmitter is disabled immediately. The receiver is disabled but will first complete receiving a byte in process of being received.

Data Terminal Ready (Bit 0)

This bit enables all selected interrupts and controls the state of the Data Terminal Ready ($\overline{DTR}$) line. A 0 indicates the microcomputer system is not ready by setting the $\overline{DTR}$ line high. A 1 indicates the microcomputer system is ready by setting the $\overline{DTR}$ line low. $\overline{DTR}$ also enables and disables the transmitter and receiver.

Receiver Interrupt Control (Bit 1)

This bit disables the Receiver from generating an interrupt when set to a 1. The Receiver interrupt is enabled when this bit is set to a 0 and Bit 0 is set to a 1.

Transmitter Interrupt Control (Bits 2, 3)

These bits control the state of the Ready to Send ($\overline{RTS}$) line and the Transmitter interrupt

Receiver Echo Mode (Bit 4)

A 1 enables the Receiver Echo Mode and a 0 disables the Receiver Echo Mode. When bit 4 is a 1 bits 2 and 3 must be 0. In the Receiver Echo Mode, the Transmitter returns each transmission received by the Receiver delayed by one-half bit time.

Parity Mode Enable (Bit 5)

This bit enables parity bit generation and checking. A 0 disables parity bit generation by the Transmitter and parity bit checking by the Receiver. A 1 bit enables generation and checking of parity bits.

Parity Mode Control (Bits 6, 7)

These bits determine the type of parity generated by the Transmitter, (even, odd, mark or space) and the type of parity check done by the Receiver (even, odd, or no check).

Reset Initialization

7	6	5	4	3	2	1	0	
0	0	0	0	0	0	0	0	**Hardware reset ($\overline{RES}$)**
–	–	–	0	0	0	0	0	**Program reset**

INTERFACE SIGNALS

Figure 4 shows the ACIA interface signals associated with the microprocessor and the modem.

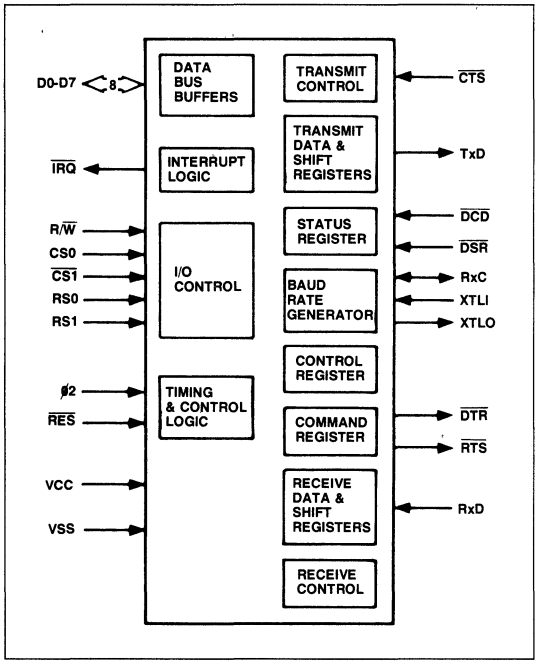


Figure 4. ACIA Interface Diagram

MICROPROCESSOR INTERFACE

Reset ($\overline{RES}$)

During system initialization a low on the $\overline{RES}$ input causes a hardware reset to occur. Upon reset, the Command Register and the Control Register are cleared (all bits set to 0). The Status Register is cleared with the exception of the indications of Data Set Ready and Data Carrier Detect, which are externally controlled by the $\overline{DSR}$ and $\overline{DCD}$ lines, and the transmitter Empty bit, which is set. $\overline{RES}$ must be held low for one Ø2 clock cycle for a reset to occur.

Input Clock (Ø2)

The input clock is the system Ø2 clock and clocks all data transfers between the system microprocessor and the ACIA.

Read/Write (R/$\overline{W}$)

The R/$\overline{W}$ input, generated by the microprocessor controls the direction of data transfers. A high on the R/$\overline{W}$ pin allows the processor to read the data supplied by the ACIA, a low allows a write to the ACIA.

Interrupt Request ($\overline{IRQ}$)

The $\overline{IRQ}$ pin is an interrupt output from the interrupt control logic. It is an open drain output, permitting several devices to be connected to the common $\overline{IRQ}$ microprocessor input. Normally a high level, $\overline{IRQ}$ goes low when an interrupt occurs.

Data Bus (D0-D7)

The eight data line (D0-D7) pins transfer data between the processor and the ACIA. These lines are bi-directional and are normally high-impedance except during Read cycles when the ACIA is selected.

Chip Selects (CS0, $\overline{CS1}$)

The two chip select inputs are normally connected to the processor address lines either directly or through decoders. The ACIA is selected when CS0 is high and $\overline{CS1}$ is low. When the ACIA is selected, the internal registers are addressed in accordance with the register select lines (RS0, RS1).

Register Selects (RS0, RS1)

The two register select lines are normally connected to the processor address lines to allow the processor to select the various ACIA internal registers. Table 1 shows the internal register select coding.

Table 1. ACIA Register Selection

		Register Operation	
RS1	RS0	R/$\overline{W}$ = Low	R/$\overline{W}$ = High
L	L	Write Transmit Data Register	Read Receiver Data Register
L	H	Programmed Reset (Data is "Don't Care")	Read Status Register
H	L	Write Command Register	Read Command Register
H	H	Write Control Register	Read Control Register

Only the Command and Control registers can both be read and written. The programmed Reset operation does not cause any data transfer, but is used to clear bits 4 through 0 in the Command register and bit 2 in the Status Register. The Control Register is unchanged by a programmed Reset. It should be noted that the programmed Reset is slightly different from the hardware Reset ($\overline{RES}$); refer to the register description.

ACIA/MODEM INTERFACE

Crystal Pins (XTLI, XTLO)

These pins are normally directly connected to the parallel mode external crystal (1.8432 MHz) to derive the various baud rates. Alternatively, an externally generated clock can drive the XTLI pin, in which case the XTLO pin must float. XTLI is the input pin for the transmit clock.

Transmit Data (TxD)

The TxD output line transfers serial nonreturn-to-zero (NRZ) data to the modem. The least significant bit (LSB) of the Transmit Data Register is the first data bit transmitted and the rate of data transmission is determined by the baud rate selected or under control of an external clock. This selection is made by programming the Control Register.

Receive Data (RxD)

The RxD input line transfers serial NRZ data into the ACIA from the modem, LSB first. The receiver data rate is either the programmed baud rate or under the control of an externally generated receiver clock. The selection is made by programming the Control Register.

Receive Clock (RxC)

The RxC is a bi-directional pin which is either the receiver 16x clock input or the receiver 16x clock output. The latter mode results if the internal baud rate generator is selected for receiver data clocking.

Request to Send ($\overline{RTS}$)

The $\overline{RTS}$ output pin controls the modem from the processor. The state of the $\overline{RTS}$ pin is determined by the contents of the Command Register.

Clear to Send ($\overline{CTS}$)

The $\overline{CTS}$ input pin controls the transmitter operation. The enable state is with $\overline{CTS}$ low. The transmitter is automatically disabled if $\overline{CTS}$ is high.

Data Terminal Ready ($\overline{DTR}$)

This output pin indicates the status of the ACIA to the modem. A low on $\overline{DTR}$ indicates the ACIA is enabled, a high indicates it is disabled. The processor controls this pin via bit 0 of the Command Register.

Data Set Ready ($\overline{DSR}$)

The $\overline{DSR}$ input pin indicates to the ACIA the status of the modem. A low indicates the "ready" state and a high, "not-ready."

Data Carrier Detect ($\overline{DCD}$)

The $\overline{DCD}$ input pin indicates to the ACIA the status of the carrier-detect output of the modem. A low indicates that the modem carrier signal is present and a high, that it is not.

TRANSMITTER AND RECEIVER OPERATION

Continuous Data Transmit

In the normal operating mode, the interrupt request output ($\overline{IRQ}$) signals when the ACIA is ready to accept the next data word to be transmitted. This interrupt occurs at the beginning of the Start Bit. When the processor reads the Status Register of the ACIA, the interrupt is cleared.

The processor must then identify that the Transmit Data Register is ready to be loaded and must then load it with the next data word. This must occur before the end of the Stop Bit, otherwise a continuous "MARK" will be transmitted. Figure 5 shows the continuous Data Transmit timing relationship.

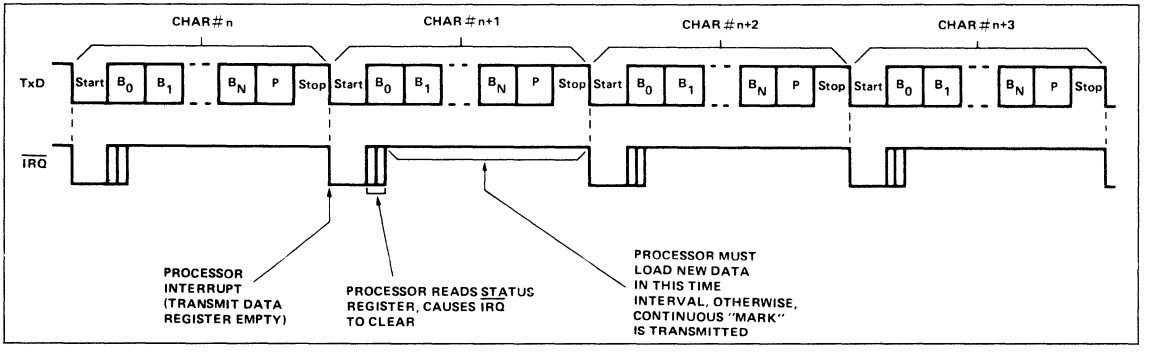


Figure 5. Continuous Data Transmit

Continuous Data Receive

Similar to the Continuous Data Transmit case, the normal operation of this mode is to assert $\overline{IRQ}$ when the ACIA has received a full data word. This occurs at about $^{9}/_{16}$ point through the Stop Bit. The processor must read the Status Register and read the data word before the next interrupt, otherwise the Overrun condition occurs. Figure 6 shows the continuous Data Receive Timing Relationship.

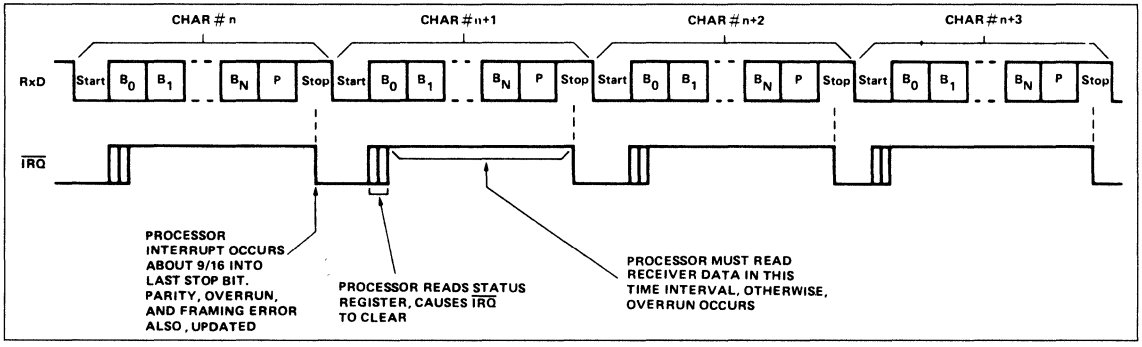


Figure 6. Continuous Data Receive

Transmit Data Register Not Loaded by Processor

If the processor is unable to load the Transmit Data Register in the allocated time, then the TxD line goes to the "MARK" condition until the data is loaded. $\overline{IRQ}$ interrupts continue to occur at the same rate as previously, except no data is transmitted. When the processor finally loads new data, a Start Bit immediately occurs, the data word transmission is started, and another interrupt is initiated, signaling for the next data word. Figure 7 shows the timing relationship for this mode of operation.

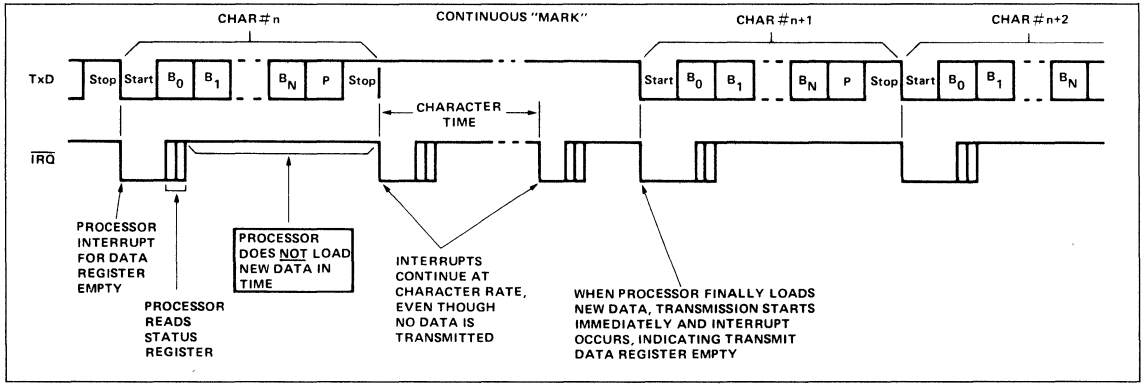


Figure 7. Transmit Data Register Not Loaded by Processor

Effect of $\overline{CTS}$ on Transmitter

$\overline{CTS}$ is the Clear-to-Send Signal generated by the modem. It is normally low (true state) but may go high in the event of some modem problems. When this occurs, the TxD line immediately goes to the "MARK" condition. Interrupts continue at the same rate, but the Status Register does not indicate that the Transmit Data Register is empty. Since there is no status bit for $\overline{CTS}$, the processor must deduce that $\overline{CTS}$ has gone to the FALSE (high) state. $\overline{CTS}$ is a transmit control line only, and has no effect on the R6551 Receiver Operation. Figure 8 shows the timing relationship for this operation.

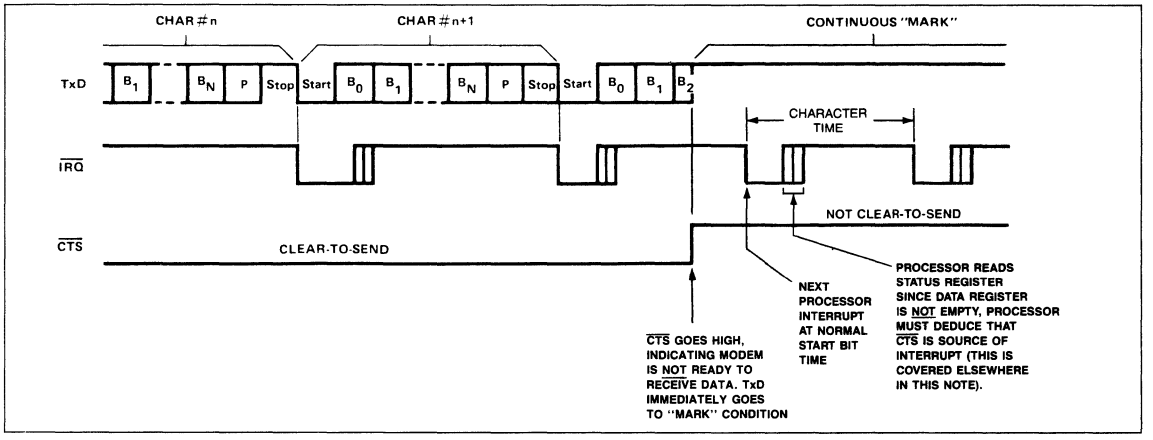


Figure 8. Effect of CTS on Transmitter

Effect of Overrun on Receiver

If the processor does not read the Receiver data Register in the allocated time, then, when the following interrupt occurs, the new data word is not transferred to the Receiver Data Register, but the Overrun status bit is set. Thus, the Data Register will contain the last valid data word received and all following data is lost. Figure 9 shows the timing relationship for this mode.

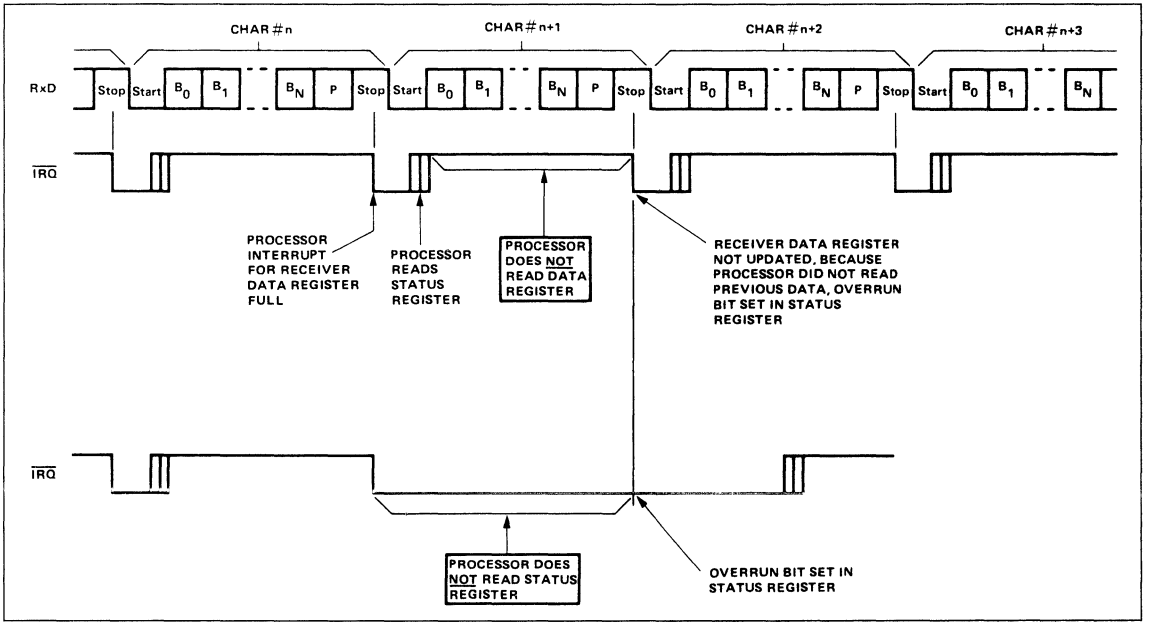


Figure 9. Effect of Overrun on Receiver

Echo Mode Timing

In Echo Mode, the TxD line re-transmits the data on the RxD line, delayed by ½ of the bit time, as shown in Figure 10.

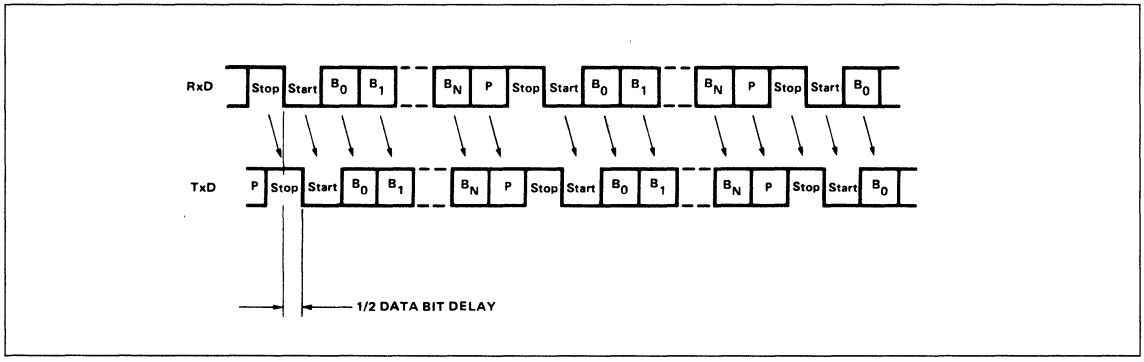


Figure 10. Echo Mode Timing

Effect of $\overline{CTS}$ on Echo Mode Operation

In Echo Mode, the Receiver operation is unaffected by $\overline{CTS}$, however, the Transmitter is affected when $\overline{CTS}$ goes high, i.e., the TxD line immediately goes to a continuous "MARK" condition. In this case, however, the Status Request indicates that the Receiver Data Register is full in response to an $\overline{IRQ}$, so the processor has no way of knowing that the Transmitter has ceased to echo. See Figure 11 for the timing relationship of this mode.

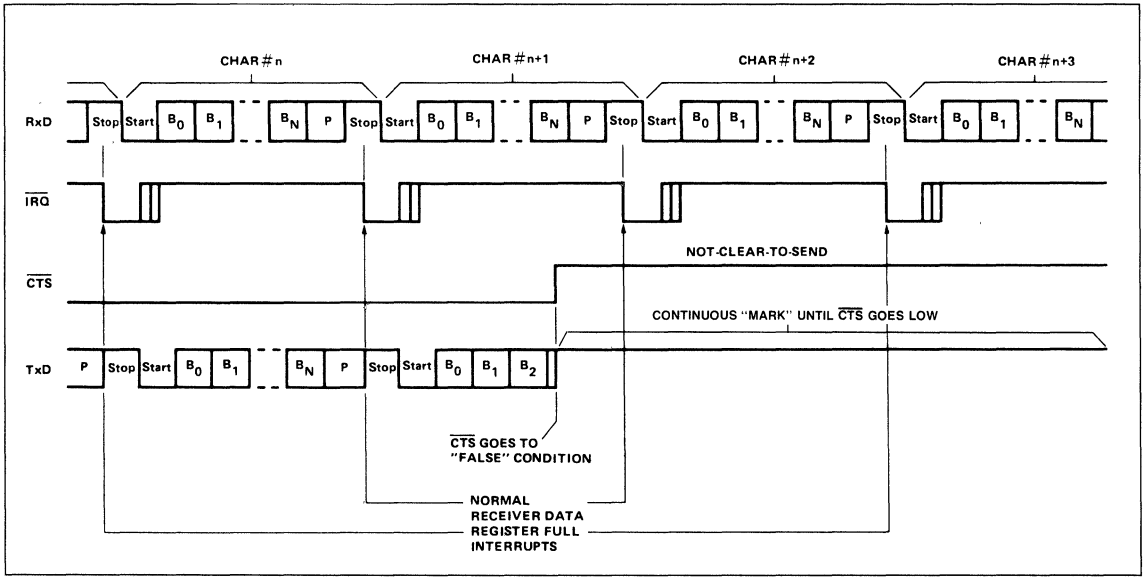


Figure 11. Effect of $\overline{CTS}$ on Echo Mode

Overrun in Echo Mode

If Overrun occurs in Echo Mode, the Receiver is affected the same way as a normal overrun in Receive Mode. For the re-transmitted data, when overrun occurs, the TxD line goes to the "MARK" condition until the first Start Bit after the Receiver Data Register is read by the processor. Figure 12 shows the timing relationship for this mode.

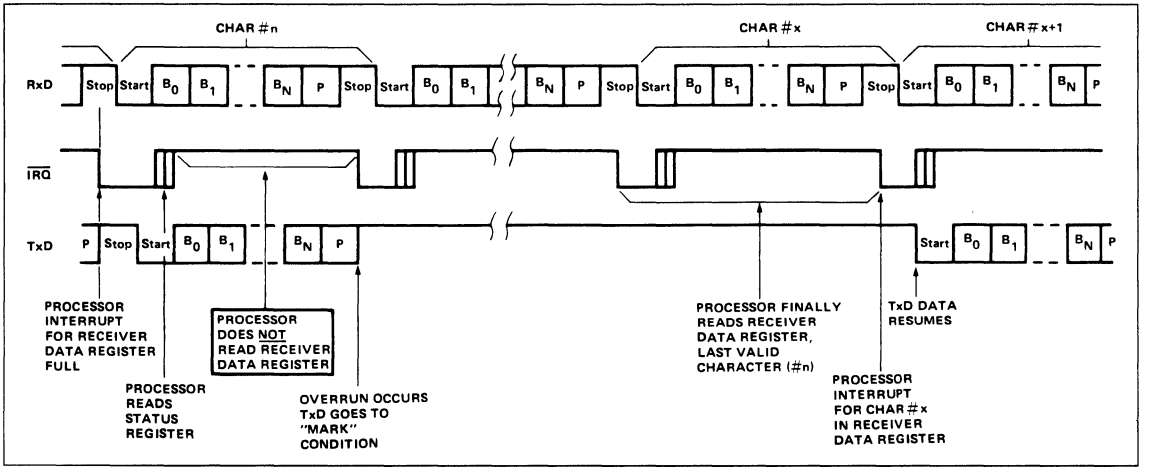


Figure 12. Overrun in Echo Mode

Framing Error

Framing Error is caused by the absence of Stop Bit(s) on received data. A Framing Error is indicated by the setting of bit 4 in the Status Register at the same time the Receiver Data Register Full bit is set, also in the Status Register. In response to $\overline{IRQ}$, generated by RDRF, the Status Register can also be checked for the Framing Error. Subsequent data words are tested for Framing Error separately, so the status bit will always reflect the last data word received. See Figure 13 for Framing Error timing relationship.

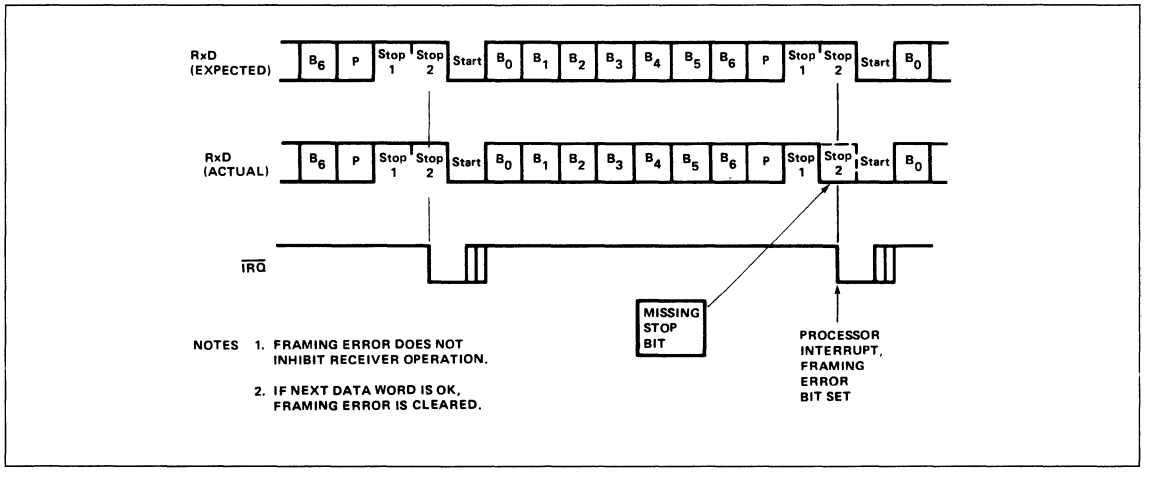


Figure 13. Framing Error

Effect of $\overline{DCD}$ on Receiver

$\overline{DCD}$ is a modem output indicating the status of the carrier-frequency-detection circuit of the modem. This line goes high for a loss of carrier. Normally, when this occurs, the modem will stop transmitting data some time later. The ACIA asserts $\overline{IRQ}$ whenever $\overline{DCD}$ changes state and indicates this condition via bit 5 in the Status Register.

Once such a change of state occurs, subsequent transitions will not cause interrupts or changes in the Status Register until the first interrupt is serviced. When the Status Register is read by the processor, the ACIA automatically checks the level of the $\overline{DCD}$ line, and if it has changed, another $\overline{IRQ}$ occurs (see Figure 14).

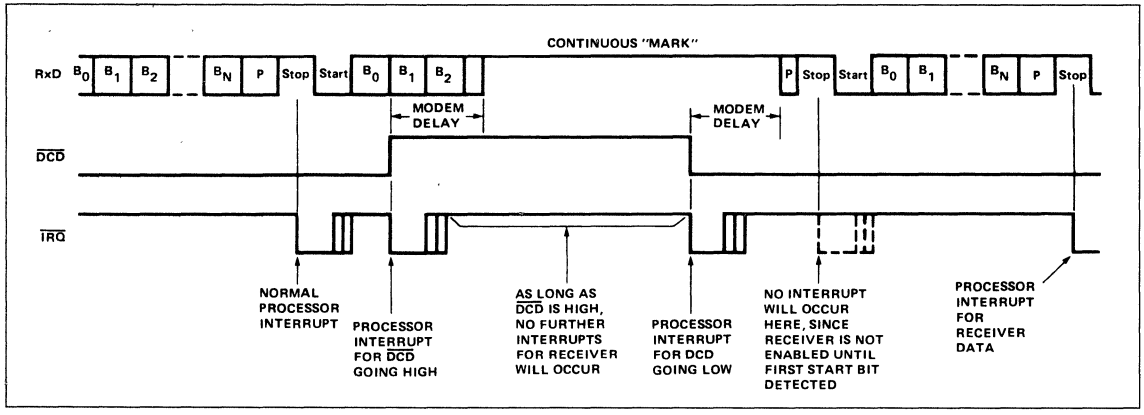


Figure 14. Effect of DCD on Receiver

Timing with 1½ Stop Bits

It is possible to select 1½ Stop Bits, but this occurs only for 5-bit data words with no parity bit. In this case, the $\overline{IRQ}$ asserted for Receiver Data Register Full occurs halfway through the trailing half-Stop Bit. Figure 15 shows the timing relationship for this mode.

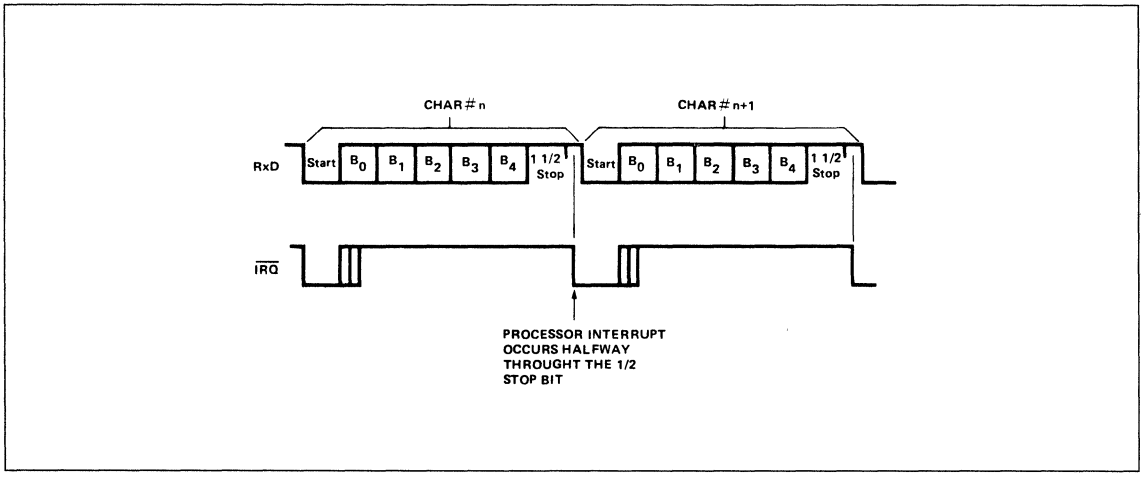


Figure 15. Timing with 1½ Stop Bits

Transmit Continuous "BREAK"

This mode is selected via the ACIA Command Register and causes the Transmitter to send continuous "BREAK" characters, beginning with the next character transmitted. At least one full "BREAK" character will be transmitted, even if the processor quickly re-programs the Command Register transmit mode. Later, when the Command Register is programmed back to normal transmit mode, an immediate Stop Bit will be generated and transmission will resume. Figure 16 shows the timing relationship for this mode.

Note

If, while operating in the Transmit Continuous "BREAK" mode, the $\overline{CTS}$ should go to a high, the TxD will be overridden by the $\overline{CTS}$ and will go to continuous "MARK" at the beginning of the next character transmitted after the $\overline{CTS}$ goes high.

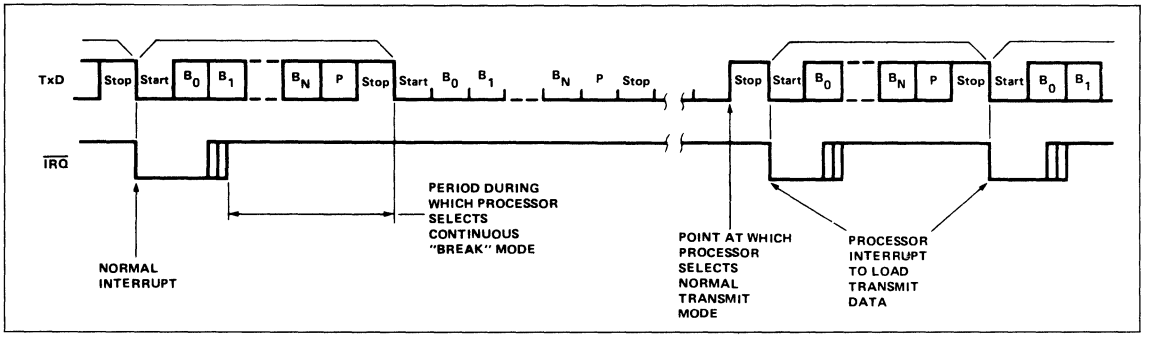


Figure 16. Transmit Continuous "BREAK"

Receive Continuous "BREAK"

In the event the modem transmits continuous "BREAK" characters, the ACIA will terminate receiving. Reception will resume only after a Stop Bit is encountered by the ACIA. Figure 17 shows the timing relationship for continuous "BREAK" characters.

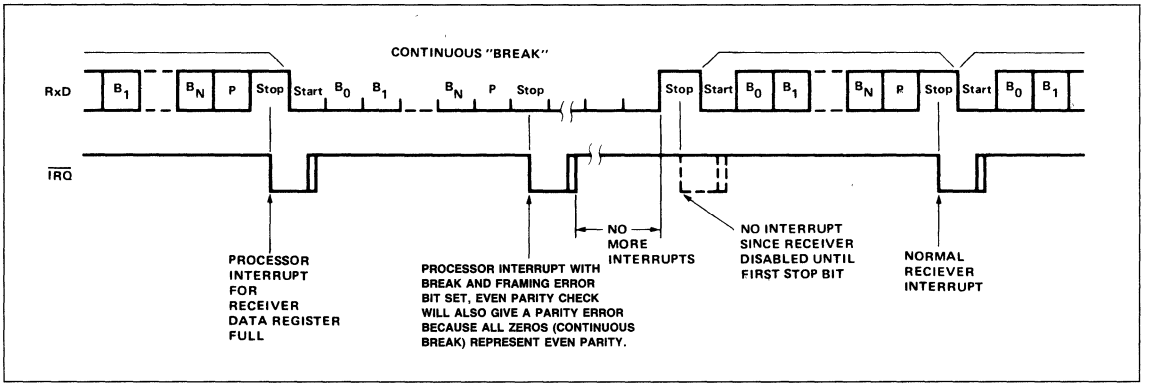


Figure 17. Receive Continuous "BREAK"

STATUS REGISTER OPERATION

Because of the special functions of the various status bits, there is a suggested sequence for checking them. When an interrupt occurs, the ACIA should be interrogated, as follows:

1. Read Status Register

   This operation automatically clears Bit 7 ($\overline{IRQ}$). Subsequent transitions on $\overline{DSR}$ and $\overline{DCD}$ will cause another interrupt.

2. Check IRQ (Bit 7) in the data read from the Status Register

   If not set, the interrupt source is not the ACIA.

3. Check $\overline{DCD}$ and $\overline{DSR}$

   These must be compared to their previous levels, which must have been saved by the processor. If they are both 0 (modem "on-line") and they are unchanged then the remaining bits must be checked.

4. Check RDRF (Bit 3)

   Check for Receiver Data Register Full.

5. Check Parity, Overrun, and Framing Error (Bits 0-2) if the Receiver Data Register is full.

6. Check TDRE (Bit 4)

   Check for Transmitter Data Register Empty.

7. If none of the above conditions exist, then $\overline{CTS}$ must have gone to the false (high) state.

PROGRAM RESET OPERATION

A program reset occurs when the processor performs a write operation to the ACIA with RS0 low and RS1 high. The program reset operates somewhat different from the hardware reset ($\overline{RES}$ pin) and is described as follows:

1. Internal registers are not completely cleared. Check register formats for the effect of a program reset on internal registers.

2. The $\overline{DTR}$ line goes high immediately.

3. Receiver and transmitter interrupts are disabled immediately. If $\overline{IRQ}$ is low when the reset occurs, it stays low until serviced, unless interrupt was caused by $\overline{DCD}$ or $\overline{DSR}$ transition.

4. $\overline{DCD}$ and $\overline{DSR}$ interrupts are disabled immediately. If $\overline{IRQ}$ is low and was caused by $\overline{DCD}$ or $\overline{DSR}$, then it goes high, also $\overline{DCD}$ and $\overline{DSR}$ status bits subsequently will follow the input lines, although no interrupt will occur.

5. Overrun cleared, if set.

MISCELLANEOUS

1. If Echo Mode is selected, $\overline{RTS}$ goes low.

2. If Bit 0 of Command Register ($\overline{DTR}$) is 0 (disabled), then:

   a) All interrupts are disabled, including those caused by $\overline{DCD}$ and $\overline{DSR}$ transitions.
   b) Transmitter is disabled immediately.
   c) Receiver is disabled, but a character currently being received will be completed first.

3. Odd parity occurs when the sum of all the 1 bits in the data word (including the parity bit) is odd.

4. In the receive mode, the received parity bit does not go into the Receiver Data Register, but generates parity error or no parity error for the Status Register.

5. Transmitter and Receiver may be in full operation simultaneously. This is "full-duplex" mode.

6. If the RxD line inadvertently goes low and then high right after a Stop Bit, the ACIA does not interpret this as a Start Bit, but samples the line again halfway into the bit to determine if it is a true Start Bit or a false one. For false Start Bit detection, the ACIA does not begin to receive data, instead, only a true Start Bit initiates receiver operation.

7. Precautions to consider with the crystal oscillator circuit:

   a) The external crystal should be a "series" mode crystal.
   b) The XTALI input may be used as an external clock input. The unused pin (EXTALO) must be floating and may not be used for any other function.

8. $\overline{DCD}$ and $\overline{DSR}$ transitions, although causing immediate processor interrupts, have no affect on transmitter operation. Data will continue to be sent, unless the processor forces transmitter to turn off. Since these are high-impedance inputs, they must not be permitted to float (un-connected). If unused, they must be terminated either to GND or V_{CC}.

GENERATION OF NON-STANDARD BAUD RATES

Divisors

The internal counter/divider circuit selects the appropriate divisor for the crystal frequency by means of bits 0-3 of the ACIA Control Register, as shown in Table 2.

Generating Other Baud Rates

By using a different crystal, other baud rates may be generated. These can be determined by:

$$\text{Baud Rate} = \frac{\text{Crystal Frequency}}{\text{Divisor}}$$

Furthermore, it is possible to drive the ACIA with an off-chip oscillator to achieve other baud rates. In this case, XTALI (pin 6) must be the clock input and XTALO (pin 7) must be a no-connect.

Table 2. Divisor Selection

Control Register Bits				Divisor Selected For The Internal Counter	Baud Rate Generated With 1.8432 MHz Crtstal	Baud Rate Generated With a Crystal of Frequency (F)
3	2	1	0			
0	0	0	0	No Divisor Selected	16 × External Clock at Pin RxC	16 × External Clock at Pin RxC
0	0	0	1	36,864	$\frac{1.8432 \times 10^6}{36,864} = 50$	$\frac{F}{36,864}$
0	0	1	0	24,576	$\frac{1.8432 \times 10^6}{24,576} = 75$	$\frac{F}{24,576}$
0	0	1	1	16,769	$\frac{1.8432 \times 10^6}{16,769} = 109.92$	$\frac{F}{16,769}$
0	1	0	0	13,704	$\frac{1.8432 \times 10^6}{13,704} = 134.51$	$\frac{F}{13,704}$
0	1	0	1	12,288	$\frac{1.8432 \times 10^6}{12,288} = 150$	$\frac{F}{12,288}$
0	1	1	0	6,144	$\frac{1.8432 \times 10^6}{6,144} = 300$	$\frac{F}{6,144}$
0	1	1	1	3,072	$\frac{1.8432 \times 10^6}{3,072} = 600$	$\frac{F}{3,072}$
1	0	0	0	1,536	$\frac{1.8432 \times 10^6}{1,536} = 1,200$	$\frac{F}{1,536}$
1	0	0	1	1,024	$\frac{1.8432 \times 10^6}{1,024} = 1,800$	$\frac{F}{1,024}$
1	0	1	0	768	$\frac{1.8432 \times 10^6}{768} = 2,400$	$\frac{F}{768}$
1	0	1	1	512	$\frac{1.8432 \times 10^6}{512} = 3,600$	$\frac{F}{512}$
1	1	0	0	384	$\frac{1.8432 \times 10^6}{384} = 4,800$	$\frac{F}{384}$
1	1	0	1	256	$\frac{1.8432 \times 10^6}{256} = 7,200$	$\frac{F}{256}$
1	1	1	0	192	$\frac{1.8432 \times 10^6}{192} = 9,600$	$\frac{F}{192}$
1	1	1	1	96	$\frac{1.8432 \times 10^6}{96} = 19,200$	$\frac{F}{96}$

DIAGNOSTIC LOOP-BACK OPERATING MODES

A simplified block diagram for a system incorporating an ACIA is shown in Figure 18.

It may be desirable to include in the system a facility for "loop-back" testing, of which there are two kinds:

1. Local Loop-Back

   Loop-back from the point of view of the processor. In this case, the Modem and Data Link must be effectively disconnected and the ACIA transmitter connected back to its own receiver, so that the processor can perform diagnostic checks on the system, excluding the actual data channel.

2. Remote Loop-Back

   Loop-back from the point of view of the Data Link and Modem. In this case, the processor, itself, is disconnected and all received data is immediately retransmitted, so the system on the other end of the Data Link may operate independent of the local system.

The ACIA does not contain automatic loop-back operating modes, but they may be implemented with the addition of a small amount of external circuitry. Figure 19 indicates the necessary logic to be used with the ACIA. The LLB line is the positive-true signal to enable local loop-back operation. Essentially, LLB = high does the following.

1. Disables outputs TxD, $\overline{DTR}$, and $\overline{RTS}$ (to Modem).
2. Disables inputs RxD, $\overline{DCD}$, $\overline{CTS}$, $\overline{DSR}$ (from Modem).
3. Connects transmitter outputs to respective receiver inputs (i.e., TxD to RxD, $\overline{DTR}$ to $\overline{DCD}$, $\overline{RTS}$ to $\overline{CTS}$).

LLB may be tied to a peripheral control pin (from an R6520 or R6522, for example) to provide processor control of local loop-back operation. In this way, the processor can easily perform local loop-back diagnostic testing.

Remote loop-back does not require this circuitry, so LLB must be set low. However, the processor must select the following:

1. Control Register bit 4 must be 1, so that the transmitter clock equals the receiver clock.
2. Command Register bit 4 must be 1 to select Echo Mode.
3. Command Register bits 3 and 2 must be 1 and 0, respectively to disable $\overline{IRQ}$ interrupt to transmitter.
4. Command Register bit 1 must be 0 to disable $\overline{IRQ}$ interrupt for receiver.

In this way, the system re-transmits received data without any effect on the local system.

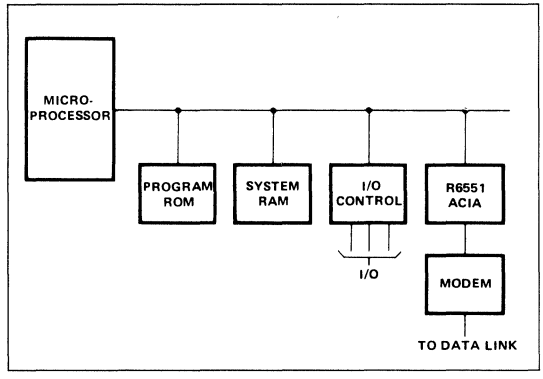


Figure 18. Simplified System Diagram

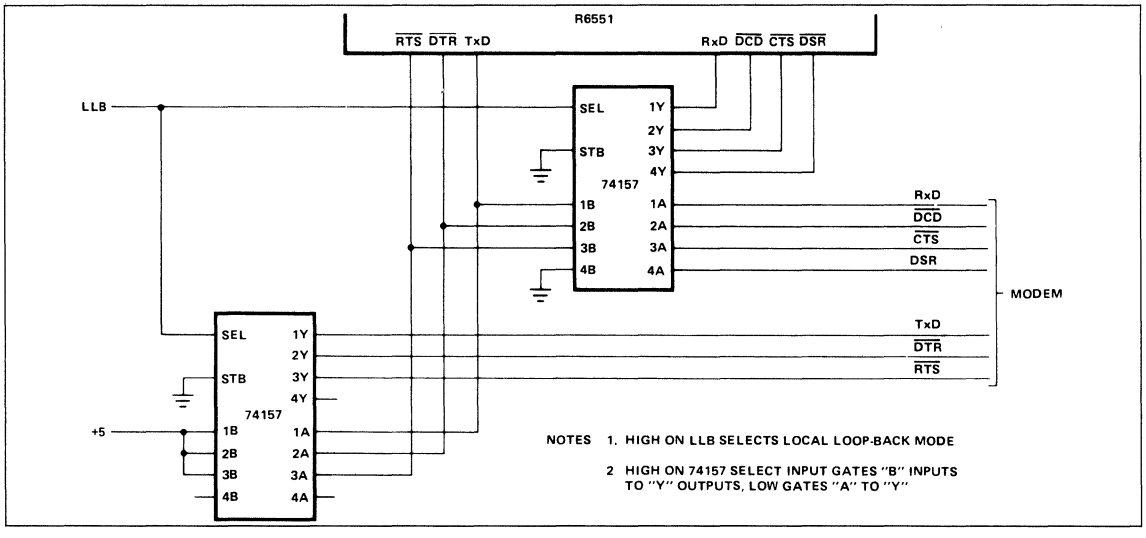


Figure 19. Loop-Back Circuit Schematic

READ TIMING DIAGRAM

Timing diagrams for transmit with external clock, receive with external clock, and $\overline{IRQ}$ generation are shown in Figures 20, 21 and 22, respectively. The corresponding timing characteristics are listed in Table 3.

Table 3. Transmit/Receive Characteristics

Characteristic	Symbol	1 MHz		2 MHz		Unit
		Min	Max	Min	Max	
Transmit/Receive Clock Rate	t_{CCY}	400*	—	400*	—	ns
Transmit/Receive Clock High Time	t_{CH}	175	—	175	—	ns
Transmit/Receive Clock Low Time	t_{CL}	175	—	175	—	ns
XTLI to TxD Propagation Delay	t_{DD}	—	500	—	500	ns
RTS Propagation Delay	t_{DLY}	—	500	—	500	ns
$\overline{IRQ}$ Propagation Delay (Clear)	t_{IRQ}	—	500	—	500	ns
Load Capacitance $\overline{DTR}$, RTS	C_L	—	130	—	130	pF
TxD		—	30	—	30	pF

Notes:
(t_R, t_F = 10 to 30 ns)

*The baud rate with external clocking is: Baud Rate = $\frac{1}{16 \times t_{CCY}}$

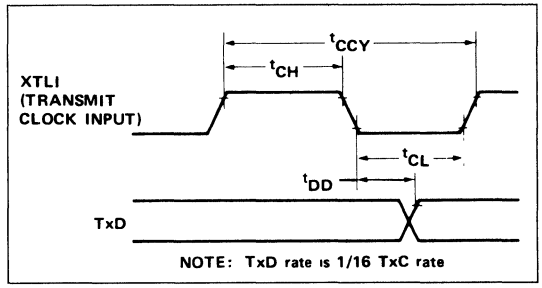


Figure 20. Transmit Timing with External Clock

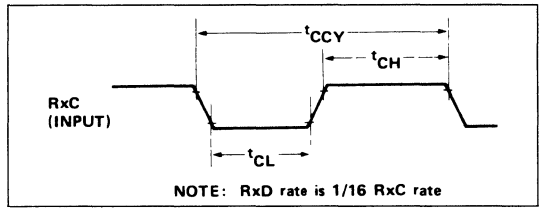


Figure 21. Receive External Clock Timing

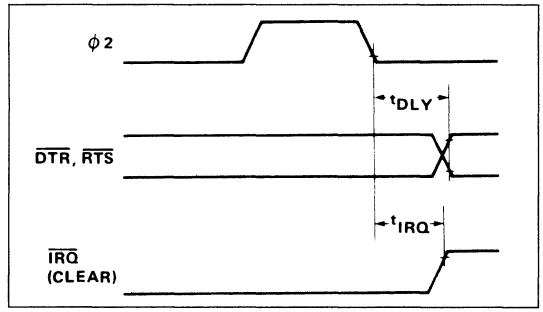


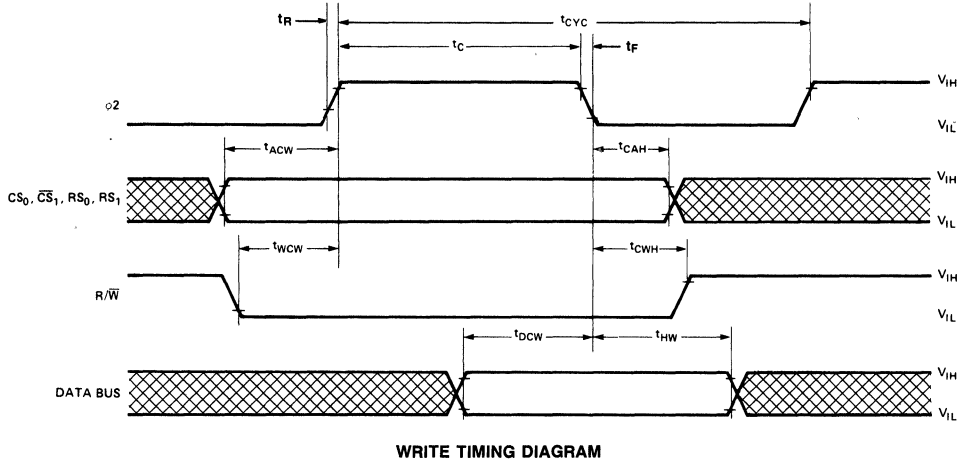
Figure 22. Interrupt and Output Timing

AC CHARACTERISTICS

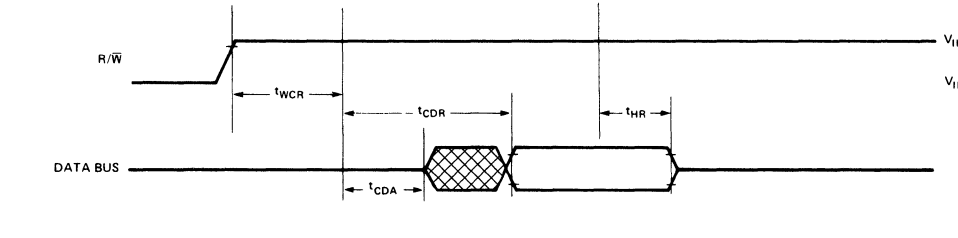
(V_{CC} = 5.0V ± 5%, V_{SS} = 0, T_A = T_L to T_H, unless otherwise noted)

Parameter	Symbol	1 MHz		2 MHz		Unit
		Min	Max	Min	Max	
Cycle Time	t_{CYC}	1.0	40	0.5	40	μs
Ø2 Pulse Width	t_C	400	—	200	—	ns
Address Set-Up Time	t_{ACW}	120	—	70	—	ns
Address Hold Time	t_{CAH}	0	—	0	—	ns
R/$\overline{W}$ Set-Up Time	t_{WCW}	120	—	70	—	ns
R/$\overline{W}$ Hold Time	t_{CWH}	0	—	0	—	ns
Data Bus Set-Up Time	t_{DCW}	150	—	60	—	ns
Data Bus Hold Time	t_{HW}	20	—	20	—	ns
Read Access Time (Valid Data)	t_{CDR}	—	200	—	150	ns
Read Hold Time	t_{HR}	20	—	20	—	ns
Bus Active Time (Invalid Data)	t_{CDA}	40	—	40	—	ns

Notes: 1. V_{CC} = 5.0V ±5%.
2. T_A = T_L to T_H.
3. t_R and t_F = 10 to 30 ns.
4. D0-D7 load capacitance = 130 pF.



WRITE TIMING DIAGRAM



READ TIMING CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to +7.0	Vdc
Input Voltage	V_{IN}	−0.3 to V_{CC}	Vdc
Output Voltage	V_{OUT}	−0.3 to V_{CC}	Vdc
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{STG}	−55 to +150	°C

***NOTE:** Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in other sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2

OPERATING CONDITIONS

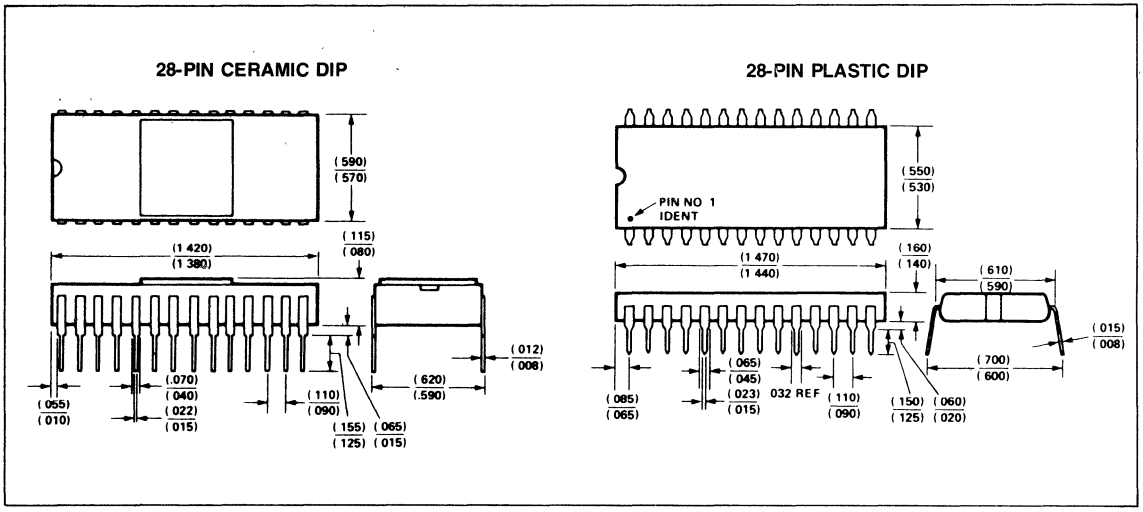
Parameter	Symbol	Value
Supply Voltage	V_{CC}	5V ±5%
Temperature Range Commercial Industrial	T_A	 0° to 70°C −40°C to +85°C

DC CHARACTERISTICS

(V_{CC} = 5.0V ± 5%, V_{SS} = 0, T_A = T_L to T_H, unless otherwise noted)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input High Voltage Except XTLI and XTLO XTLI and XTLO	V_{IH}	 2.0 2.4	 — —	 V_{CC} V_{CC}	V	
Input Low Voltage Except XTLI and XTLO XTLI and XTLO	V_{IL}	 V_{SS} V_{SS}	 — —	 0.8 0.4	V	
Input Leakage Current Ø2, R/W, RES, CS0, CS1, RS0, RS1, CTS, RxD, DCD, DSR	I_{IN}	—	—	2.5	μA	V_{IN} = 0V to 5.25V V_{CC} = 0V
Input Leakage Current for High Impedance (Three State Off) D0–D7	I_{TSI}	—	±2	±10.0	μA	V_{IN} = 0.4V to 2.4V V_{CC} = 5.25V
Output High Voltage D0-D7, TxD, RxC, RTS, DTR	V_{OH}	2.4	—	—	V	I_{LOAD} = −100 μA V_{CC} = 4.75V
Output Low Voltage D0-D7, TxD, RxC, RTS, DTR, IRQ	V_{OL}	—	—	0.4	V	V_{CC} = 4.75V I_{LOAD} = 1.6 mA
Output High Current (Sourcing) D0-D7, TxD, RxC, RTS, DTR	I_{OH}	−100	—	—	μA	V_{OH} = 2.4V
Output Low Current (Sinking) D0-D7, TxD, RxC, RTS, DTR, IRQ	I_{OL}	1.6	—	—	mA	V_{OL} = 0.4V
Output Leakage Current (off state) IRQ	I_{OFF}	—	—	10.0	μA	V_{OUT} = 5V
Clock Capacitance (Ø2)	C_{CLK}	—	—	20	pF	V_{CC} = 5V V_{IN} = 0V f = 1 MHz T_A = 25°C
Input Capacitance except Ø2	C_{IN}	—	—	10	pF	
Output Capacitance	C_{OUT}	—	—	10	pF	
Power Dissipation	P_D	—	170	300	mW	T_A = 25°C

PACKAGE DIMENSIONS



Rockwell

R6592
SINGLE-CHIP PRINTER CONTROLLER

2

INTRODUCTION

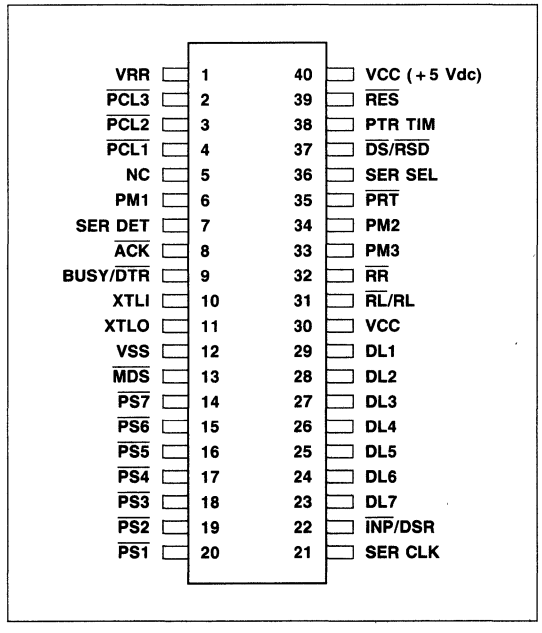
The Rockwell R6592 is a single-chip printer controller for eight different EPSON* dot-matrix impact printers, models 210, 220, 240, 511L, 512, 522, 541L, and 542. The R6592 offers the flexibility to support any of these models with a minimum of circuitry. Generation of 96 standard ASCII upper and lower case characters and 6 special characters is provided. In addition, up to 10 ASCII control commands are accepted, depending upon the printer. Logic is included in the R6592 to print up to 26 columns on the 210, 220, and 240 models, and up to 40 columns on the 511L, 512, 522, 541L and 542 models.

Input data may be selected to be in the RS-232 serial format with selectable baud rate from 50 to 7200 bits/second or the parallel format. External circuitry is required to convert RS-232 logic levels to R6592 interface logic levels. An external latch may be required for the R6592 to sample parallel data. If both selectable serial and parallel data interface capability is desired, two external multiplexers are required; one to combine four serial baud select lines and four parallel data interface lines into four R6592 input lines and the other to combine two serial data/control lines and two parallel control lines into two other R6592 input lines.

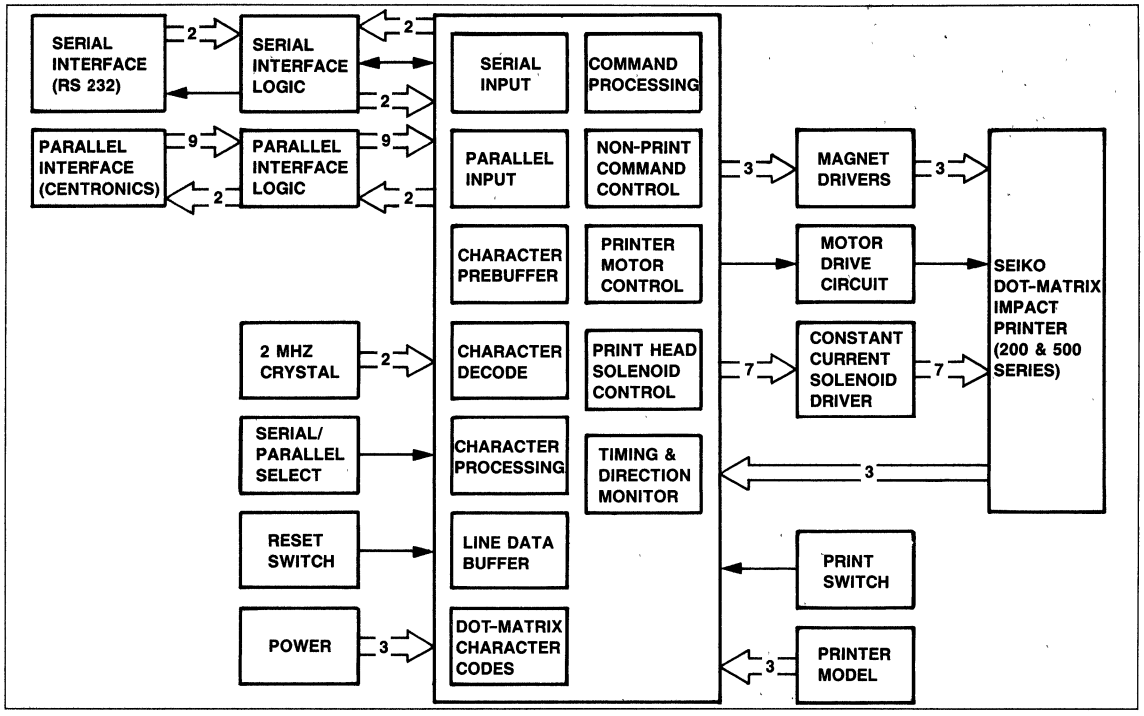
*EPSON is a trade name of Shinshu Seiki Co., Ltd., a member of the Seiko Group. EPSON printers are distributed in the United States by C. Itoh Electronics, Inc. The R6592 meets the printer specifications listed in this data sheet.

FEATURES

- Controls EPSON Dot-Matrix Impact Printers*
  - Model 210
  - Model 220
  - Model 240
  - Model 511L
  - Model 512
  - Model 522
  - Model 541L
  - Model 542
- Minimal Support Circuitry Required
- On-Chip 5 × 7 Dot-Matrix Character Generation
- 96 Standard Upper and Lower Case ASCII Characters (7 Bit Code)
- Six Special ASCII Characters (7 Bit Code)
- Up to 10 ASCII Commands Accepted (Printer Dependent)
- Selectable Serial or Parallel Input Data Operation
- Centronics Standard Parallel Interface
  - — Seven Data Lines Plus Data Strobe and Input Drive Input
  - — Busy and Acknowledge Output
- RS-232C Serial Interface
  - — Baud Rate from 50 to 7200 Bits per Second
  - — Received Data and Data Set Ready Input
  - — Data Terminal Ready Output
- Single +5V ± 10% power supply
- 40 pin plastic or ceramic DIP
- 1 MHz operation (2 MHz external crystal)



R6592 Pin Configuration



R6592 Interface Diagram

INTERFACE SIGNALS

PRINTER SOLENOID 1 ($\overline{PS1}$)
PRINTER SOLENOID 2 ($\overline{PS2}$)
PRINTER SOLENOID 3 ($\overline{PS3}$)
PRINTER SOLENOID 4 ($\overline{PS4}$)
PRINTER SOLENOID 5 ($\overline{PS5}$)
PRINTER SOLENOID 6 ($\overline{PS6}$)

Active low output signals used to command seven constant current print head solenoid drivers. When low, the respective solenoid will be energized to print a dot; and when high, the solenoid will be de-energized to not print a dot. Each solenoid line corresponds to a dot position on the seven row print head. Line $\overline{PS1}$ corresponds to the top dot and $\overline{PS7}$ corresponds to the bottom dot. The output lines are activated by the positive edge of the timing signal (TIM). The TIM signal should also be used to gate PS1 through PS7 to the current drivers and to de-energize the current driver inputs within 600±20 µsec of the start of the TIM signal by means of a one-shot flip-flop.

PRINTER CONTROL LINE 1 ($\overline{PCL1}$)
PRINTER CONTROL LINE 2 ($\overline{PCL2}$)
PRINTER CONTROL LINE 3 ($\overline{PCL3}$)

Active low output control lines used to issue various non-print commands to the printer. These lines are inputs to +24V drivers. When low, these lines cause magnets to be energized in the printer; when high, the magnets are to be de-energized. These lines are assigned to specific signals depending upon printer model:

Printer Model	R6592 Signal Name		
	PCL1	PCL2	PCL3
210	NA	Paper Feed	Change Color
220	Paper Feed (R)	Paper Feed (L)	
240	NA	Paper Feed	Slip Release
511L	NA	Paper Feed	NA
512	NA	Paper Feed	NA
522	Paper Feed (R)	Paper Feed (L)	Stamp and Cut Paper
541L	NA	Paper Feed	Paper Release
542	NA	Paper Feed	Paper Release
NA = Not Assigned			

TIMING (TIM)
RESET LEFT ($\overline{RL}$/RL)
RESET RIGHT ($\overline{RR}$)

Input signals used to indicate print cycle Timing. The R6592 initiates a print cycle on the leading edge (positive transition) of the TIM signal information to the R6592. The RESET signals are active low for the 500 series ($\overline{RR}$ and $\overline{RL}$) and are active high for the 200 series (RL). The printer timing and reset lines are assigned as follows:

Printer Model	R6592 Signal		
	TIM	$\overline{RL}$/RL	$\overline{RR}$
210	T Detector	R Detector (RL)	NA
220	T Detector	R Detector (RL)	NA
240	T Detector	R Detector (RL)	NA
511L	Timing Signal	Reset Signal R-L ($\overline{RL}$)	NA
512	Timing Signal	Reset Signal R-L ($\overline{RL}$)	Reset Signal R-R ($\overline{RR}$)
522	Timing Signal	Reset Signal R-L ($\overline{RL}$)	Reset Signal R-R ($\overline{RR}$)
541L	Timing Signal	Reset Signal R-L ($\overline{RL}$)	NA
542	Timing Signal	Reset Signal R-L ($\overline{RL}$)	Reset Signal R-R ($\overline{RR}$)

See Detail Timing Diagrams in Printer Specifications.

MOTOR DRIVE SIGNAL ($\overline{MDS}$)

Active low output signal used to control application of power from a driver circuit to the printer motor. When high, the motor drive is turned off and when low, the motor drive is turned on. The driver circuit for the 500 series must supply 10 to 30 ma at TTL levels. The driver circuit for the 200 series must additionally provide motor braking.

PRINTER MODEL 1 ($\overline{PM1}$)
PRINTER MODEL 2 ($\overline{PM2}$)
PRINTER MODEL 3 ($\overline{PM3}$)

Encoded input lines used to determine which printer model is connected to the R6592. A connection to GND (low) causes "0" to be read. An open input (high) causes logic "1" to be read. The encoding for the printer model is:

Printer Model	Printer Model Line		
	PM3	PM2	PM1
210	0	0	0
220	0	0	1
240	0	1	0
511L	0	1	1
512	1	0	0
522	1	0	1
541L	1	1	0
542	1	1	1

PRINT ($\overline{PRT}$)

Active low input line used to command R6592 to print a line. When low (GND) print commands will continue to be issued. If the print buffer is partially filled, a line will be printed. Line feeds will subsequently be issued while $\overline{PRT}$ is low. When high (open), print commands will not be issued.

SERIAL SELECT (SER SEL)

Active high input line used to indicate the desired data transmission mode to the R6592. When high (open), input data will be received and processed from the serial interface (RS-232C). When low (GND), input data will be received and processed from the parallel interface (Centronics).

If both transmission modes are to be implemented (but not simultaneously), the SER SEL line should be used to select either serial or parallel signals through multiplexer circuits. If either serial or parallel data transmission is exclusively used, multiplexing of the indicated serial/parallel signals is not required.

DATA LINE 1/BAUD RATE 1 (DL1/BR1)
DATA LINE 2/BAUD RATE 2 (DL2/BR2)
DATA LINE 3/BAUD RATE 3 (DL3/BR3)
DATA LINE 4/BAUD RATE 4 (DL4/BR4)

Active high input signals used as parallel data lines if parallel data transfer mode is selected, or used as baud rate select lines if serial data transfer mode is selected.

If parallel data transfer mode is selected (SER SEL = low) these lines represent four of the seven total data lines (see below). DL1/BR1 represents the least significant bit when ASCII characters are decoded. If serial data transfer mode is selected (SER SEL = high), the data transfer baud rate in bits per second is:

Baud	Data Line/Baud Rate Line			
	DL4/BR4	DL3/BR3	DL2/BR2	DL1/BR1
50	0	0	0	0
75	0	0	0	1
110	0	0	1	0
135	0	0	1	1
150	0	1	0	0
300	0	1	0	1
600	0	1	1	0
1200	0	1	1	1
1800	1	0	0	0
2400	1	0	0	1
3600	1	0	1	0
4800	1	0	1	1
7200*	1	1	0	0

Note: 1 = High (open), 0 = Low (GND).
*Data cannot be sent to the R6592 while the print head is moving.

DATA LINE 5 (DL3)
DATA LINE 6 (DL4)
DATA LINE 7 (DL5)

Active high input signals used as data lines when parallel data transfer mode is selected (SER SEL = low). DL7 represents the most significant bit (MSB) when ASCII characters are decoded. Not used when serial data transfer mode is selected (SER SEL = high).

INPUT PRIME (IP)/DATA SET READY (DSR)

Input line multiplexed between a parallel communications control line (INPUT PRIME) and a serial communications control line (DATA SET READY).

If the parallel data transfer mode is selected (SER SEL = low), this line is assigned to INPUT PRIME (IP). When IP/DSR is high, the R6592 issues prints commands to the printer in a normal fashion. When IP/DSR is low, the R6592 will disable printing. This line can, therefore, be used as a print disable line to selected printers in a multiprinter system.

If the serial data transfer mode is selected (SER SEL = high), the line is assigned to DATA SET READY (DSR). When high, DSR indicates that the transmitter is operative and the R6592 will accept data. When low, DSR indicates that the transmitter is not ready to operate and the R6592 will not accept serial data.

DATA STROBE (DS)/RECEIVED SERIAL DATA (RSD)

Input line multiplexed between a parallel communications control line (DATA STROBE) and the serial communications data line (RECEIVED SERIAL DATA).

If the parallel data transfer mode is selected (SER SEL = low), this line is assigned to the DATA STROBE (DS). When DS goes low, the R6592 detects the negative transition, and samples the data on the parallel data lines. The data must be present on the data lines for at least 50 μsec after DS goes low.

If the serial data transfer mode is selected (SER SEL = high), the line is assigned to RECEIVED SERIAL DATA (RSD). The data is processed in accordance with the selected baud rate. The data must by converted from RS-232 logic levels to R6592 logic levels. The R6592 logic state is inverted from RS-232 logic state.

BUSY DATA TERMINAL READY (BUSY/DTR)

Output line multiplexed between a parallel communication control line (BUSY) and a serial communication control line (DATA TERMINAL READY).

If the parallel data transfer mode is selected (SER SEL = low), this line is assigned to BUSY. When high, BUSY indicates that the R6592 cannot receive data. When low, BUSY indicates that the R6592 is ready to receive data. BUSY is switched high during character print and while non-print commands are being processed.

If the serial data transfer mode is selected (SER SEL = high), this line is assigned to DATA TERMINAL READY (DTR). When high, DTR indicates that the R6592 cannot receive data. When low, DTR indicates that the R6592 is ready to receive data. DTR is switched high during character print and while non-print commands are being processed.

ACKNOWLEDGE (ACK)

Active low output signal used to inform the parallel data transmitter that an input character has been received. ACK is switched low for 5 μsec to indicate receipt of a character.

SERIAL CLOCK (SER CLK)

A bi-directional line used to detect the start of the received serial data and to then clock in the serial data bits. When DET ENA is low, this line monitors the input serial data stream for the start bit. When the leading (falling) edge of the start bit is detected, the DET ENA is switched high and this line is switched to an output. Output pulses are generated on this line to clock the received serial data into the R6592 at the selected baud rate.

SERIAL DETECT ENABLE (DET ENA)

Active high output used to enable the received serial data onto the SER CLK line. Upon detection of the received serial start bit, this line is switched low to disable the received serial data from being placed on the SER CLK line.

PRIMARY POWER (VCC)

R6592 primary power supply: +5V ± 10%. Supplies power to CPU, I/O, timer and supporting circuitry.

RAM POWER (VRR)

R6592 RAM power supply: +5V ± 10%. Supplies power to the internal R6592 RAM. This line should be connected to VCC power supply.

SIGNAL GROUND (VSS)

R6592 power and signal ground.

XTLI

Input from 2 MHz crystal.

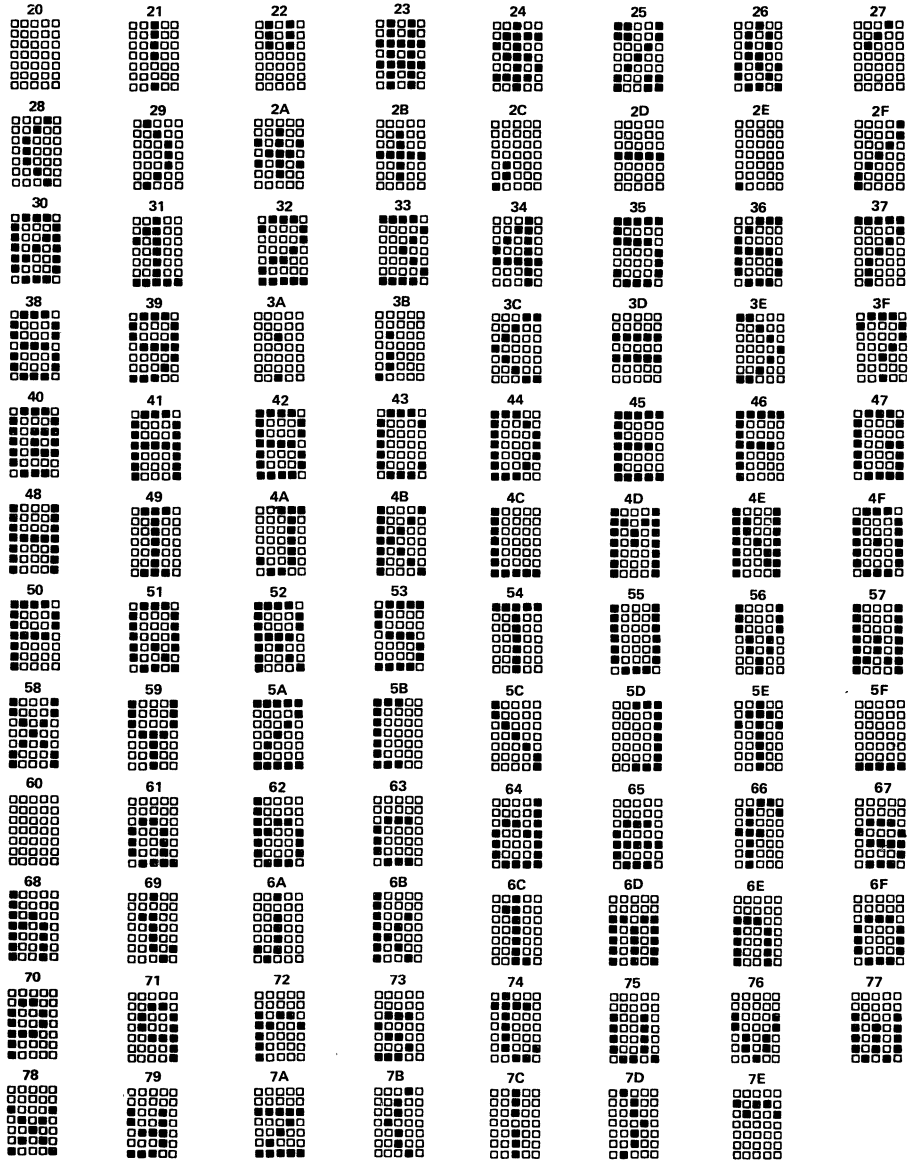
XTLO

Output to 2 MHz crystal.

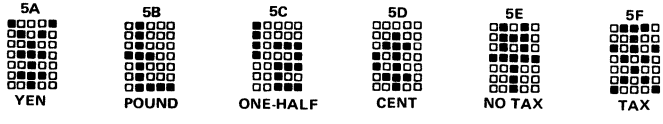
RESET (RES)

Active low signal used to reset and initialize the R6592. Must be held low for at least 8 μsec after VCC reaches operating voltage and the clock frequency on XTLO has stabilized.

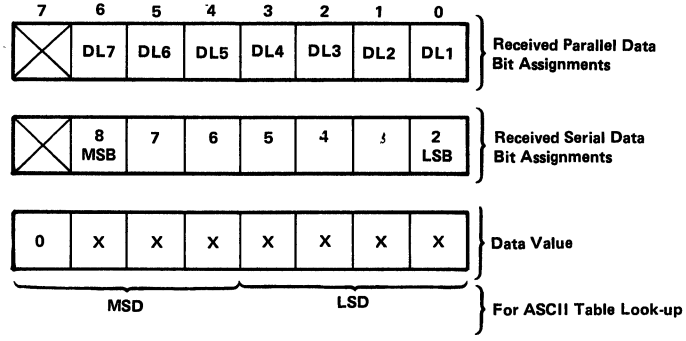
Standard 96 Character 5x7 Matrix Dot Patterns



Special 6 Character 5x7 Matrix Dot Patterns



R6592 Internal Data Format for 7-Bit ASCII Table Character Look-Up



ASCII 7-Bit Code Character Set Table

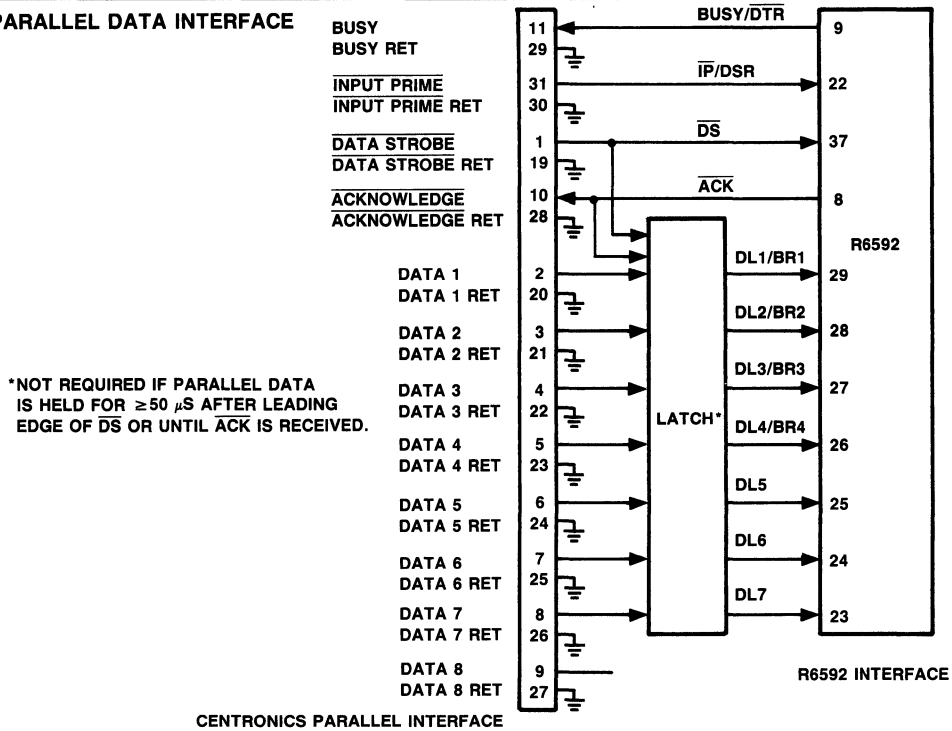
LSD	MSD	0 000	1 001	2 010	3 011	4 100	5 101	6 110	7 111
0	0000			SP	0	@	P		p
1	0001		DC1	!	1	A	Q	a	q
2	0010		DC2	"	2	B	R	b	r
3	0011		DC3	#	3	C	S	c	s
4	0100		DC4	$	4	D	T	d	t
5	0101			%	5	E	U	e	u
6	0110			&	6	F	V	f	v
7	0111			'	7	G	W	g	w
8	1000		CAN	(	8	H	X	h	x
9	1001			)	9	I	Y	i	y
A	1010	LF	¥	*	:	J	Z	j	z
B	1011	VT	t	+	;	K	[	k	{
C	1100	FF	1_2	,	<	L	\	l	|
D	1101	CR	¢	-	=	M	]	m	}
E	1110		N T	.	>	N	↑	n	~
F	1111		T X	/	?	O	←	o	DEL

LF — Line Feed
VT — Vertical Tabulation
FF — Form Feed
CR — Carriage Return
DC1 — Device Control 1
DC2 — Device Control 2
DC3 — Device Control 3
DC4 — Device Control 4

CAN — Cancel
¥ — Yen
t — Pound
¢ — Cent
1_2 — One-Half
N T — No Tax
T X — Tax

Note: Valid control commands are dependent upon printer model.

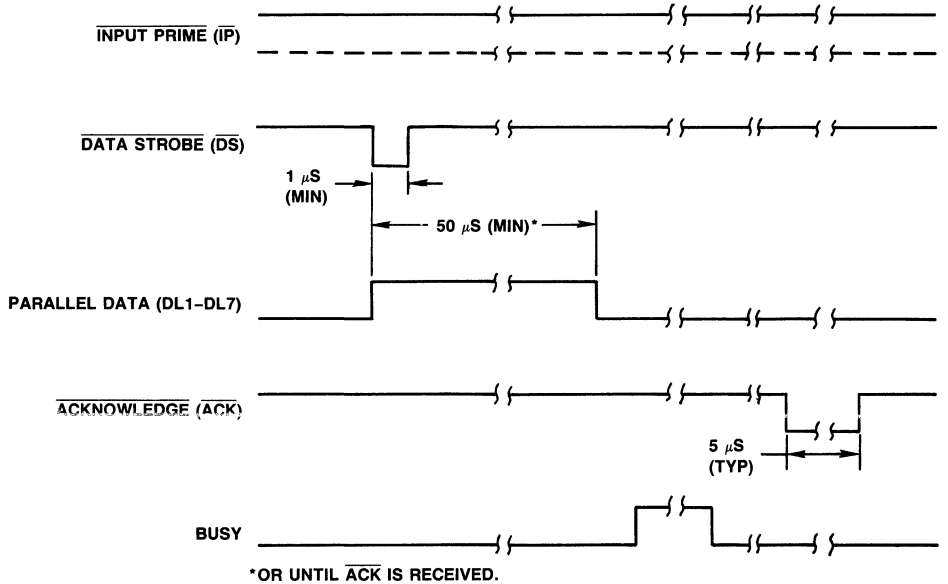
PARALLEL DATA INTERFACE



*NOT REQUIRED IF PARALLEL DATA IS HELD FOR ≥50 μS AFTER LEADING EDGE OF DS OR UNTIL ACK IS RECEIVED.

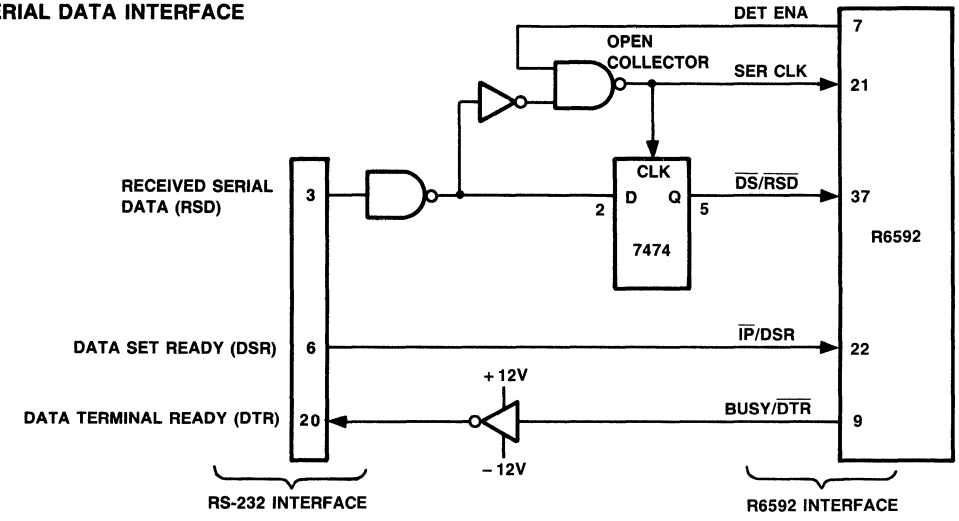
CENTRONICS PARALLEL INTERFACE

PARALLEL DATA TIMING

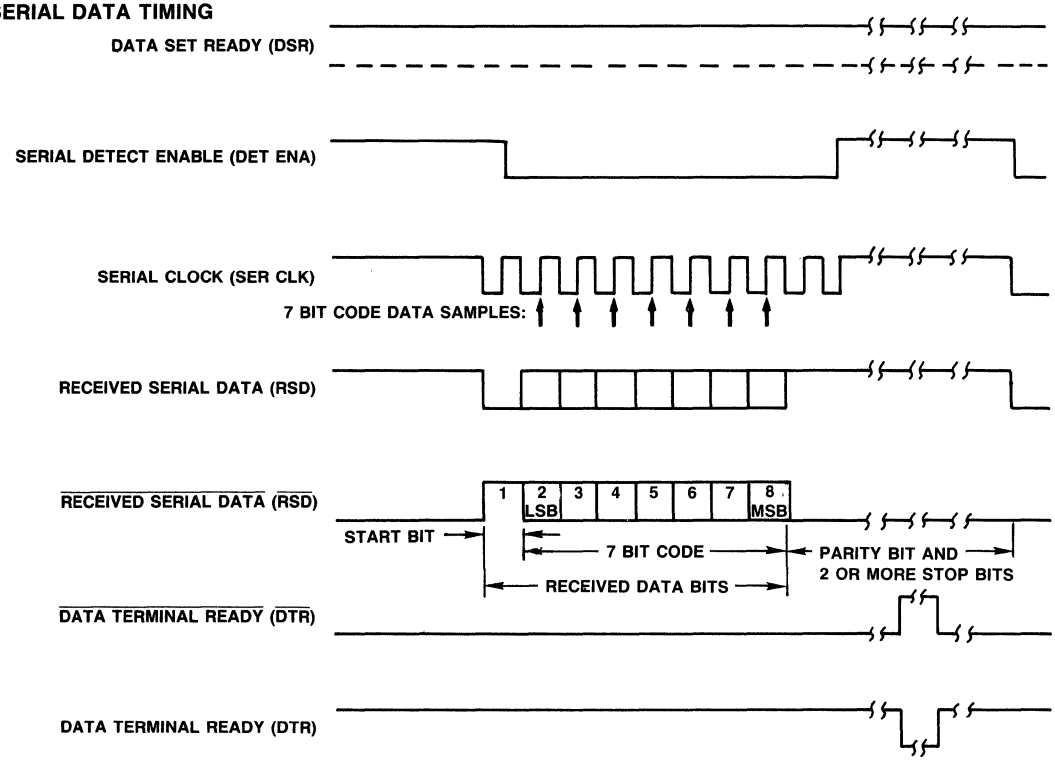


*OR UNTIL ACK IS RECEIVED.

SERIAL DATA INTERFACE



SERIAL DATA TIMING



PRINTER INTERFACE SPECIFICATIONS

The R6592 is designed to meet the interface requirements stated in the following printer specification:

Model-210 Impact Dot Matrix Mini-Printer (Preliminary)
Rev. 4, AUGUST 30, 1978

Model-220 Impact Dot Matrix Mini-Printer,
SEPTEMBER 18, 1978

Model-240 Impact Dot Matrix Mini-Printer,
SEPTEMBER 18, 1978

Model-511L Impact Dot Matrix Printer (Enlarged Character)
Revision 1 JULY 13, 1978

Model 512 Dot-Matrix Impact Printer (P512DF),
APRIL 10, 1978

Model 522 Dot-Matrix Impact Printer (P522DF),
MARCH 1, 1978

Model 541L Impact Dot Matrix Printer (Enlarged Character),
Revision 1, July 19, 1978

Model 542 Dot-Matrix Impact Printer (P542DF),
MARCH 1, 1978

For further printer information, contact:

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23844 Hawthorne Blvd. Ltd.
Torrance, CA 90505
Phone: (213) 378-2220
TWX: 910-344-7390

C. Itoh Electronics, Inc.
5301 Beethoven Street
Los Angeles, Calif. 90066
Phone: (213) 390-7778
Telex: WU 65-2451

C. Itoh Electronics, Inc.
280 Park Avenue
New York, New York, 10017
Phone: (212) 682-0420
Telex: WUD-12-5059

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to +7.0	Vdc
Input Voltage	V_{IN}	−0.3 to V_{CC} +0.3	Vdc
Output Voltage	V_{OUT}	−0.3 to V_{CC} +0.3	Vdc
Operating Temperature Commercial Industrial	T_A	 0 to +70 −40 to +85	°C
Storage Temperature	T_{STG}	−55 to +150	°C

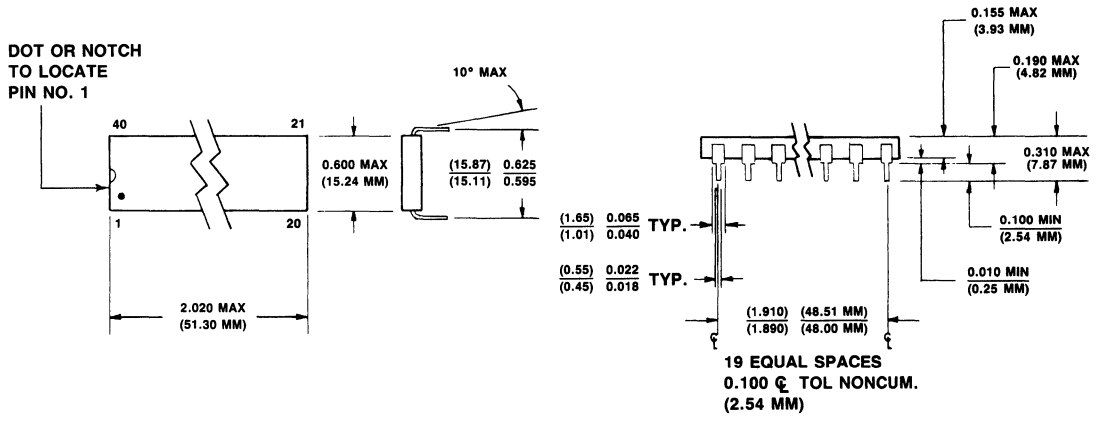
***NOTE:** Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the other sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

STATIC DC CHARACTERISTICS

(V_{CC} = 5.0V ±10%)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power Dissipation (Outputs High)	P_D	—	500	—	mW
Input High Voltage (Normal Operating Levels)	V_{IH}	+2.0	—	V_{CC}	Vdc
Input Low Voltage (Normal Operating Levels)	V_{IL}	−0.3	—	+0.8	Vdc
Input Threshold Voltage	V_{IT}	0.8	—	2.0	Vdc
Input Leakage Current V_{in} = 0 to 5.0 Vdc $\overline{RES}$	I_{IN}	—	±1.0	±2.5	μAdc
Input High Voltage (XTLI)	V_{IHXT}	+4.0	—	V_{CC}	Vdc
Input Low Voltage (XTLI)	V_{ILXT}	−0.3	—	+0.8	Vdc
Input Low Current (V_{IL} = 0.4 Vdc)	I_{IL}	—	−1.0	−1.6	mAdc
Output High Voltage (V_{CC} = min, I_{Load} = −100 μAdc)	V_{OH}	2.4	—	—	Vdc
Output Low Voltage (V_{CC} = min, I_{Load} = 1.6 mAdc)	V_{OL}	—	—	−0.4	Vdc
Output High Current (Sourcing) (V_{OH} = 2.4 Vdc)	I_{OH}	−100		—	μAdc
Output Low Current (Sinking) (V_{OL} = 0.4 Vdc)	I_{OL}	1.6	—	—	mAdc
Input Capacitance (V_{in} − 0, T_A = 25°C, f = 1.0 MHz) Pins 2–9, 13–29 and 31–38 XTLI, XTLO	C_{in}	 — —	 — —	 10 50	pF
Output Capacitance (V_{in} − 0, T_A = 25°C, f = 1.0 MHz)	C_{OUT}	—	—	10	pF
Note: Negative sign indicates outward current flow, positive indicates inward flow.					

PACKAGE DIMENSIONS



NOTE: PIN NO. 1 IS IN LOWER LEFT CORNER WHEN SYMBOLIZATION IS IN NORMAL ORIENTATION.

2

Rockwell

R65560
MULTI-PROTOCOL COMMUNICATIONS CONTROLLER (MPCC)

PRELIMINARY

DESCRIPTION

The R65560 Multi-Protocol Communications Controller (MPCC) interfaces a single serial communications channel to a 6500/6800 microcomputer-based system using either asynchronous or synchronous protocol. High speed bit rate, automatic formatting, low overhead programming, eight character buffering, and two channel DMA interface optimize MPCC performance to take full advantage of the 6500/6800 processing capabilities.

In synchronous operation, the MPCC supports bit-oriented protocols (BOP), such as SDLC/HDLC, and character-oriented protocols (COP), such as IBM Bisync (BSC) in either ASCII or EBCDIC coding. Formatting, synchronizing, validation and error detection is performed automatically in accordance with protocol requirements and selected options. Asynchronous (ASYNC) and isochronous (ISOC) modes are also supported. In addition, modem interface handshake signals are available for general use.

Control, status and data are transferred between the MPCC and the microcomputer bus via 19 directly addressable registers and a DMA interface. Two first-in first-out (FIFO) registers, addressable through separate receiver and transmitter data registers, each buffer up to eight characters at a time to allow more CPU/MPU processing time to service data received or to be transmitted and to maximize bus throughput, especially during DMA operation. The two-channel Direct Memory Access (DMA) interface operates with the MC6844 DMA Controller.

An on-chip oscillator drives the internal baud rate generator (BRG) and an external clock output with an 8 MHz input crystal or clock frequency. The BRG, in conjunction with two selectable prescalers and 16-bit programmable divisor, provides a data bit rate of DC to 4 MHz.

ORDERING INFORMATION

Part Number	Frequency	Temperature Range
R65560	4 MHz	0°C to 70°C

Package: C = Ceramic
P = Plastic

FEATURES

- Full duplex synchronous/asynchronous receiver and transmitter
- Fully implements IBM Binary Synchronous Communications (BSC) in two coding formats: ASCII and EBCDIC
- Supports other synchronous character-oriented protocols (COP), such as six-bit BSC, X3.28, ISO IS1745, ECMA-16, etc.
- Supports synchronous bit-oriented protocols (BOP), such as SDLC, HDLC, X.25, etc.
- Asynchronous and isochronous modes
- Modem handshake interface
- High speed serial data rate (DC to 4 MHz)
- Internal oscillator and Baud Rate Generator (BRG) with programmable data rate
- Crystal or TTL level clock input and buffered clock output (8 MHz)
- Direct interface to 6500/6800 microprocessor bus
- Eight-character receiver and transmitter buffer registers
- 19 directly addressable registers for flexible option selection, complete status reporting, and data transfer
- Maskable interrupt conditions for receiver, transmitter and serial interface
- Programmable microprocessor bus data transfer: polled, interrupt and two-channel DMA transfer compatible with MC6844
- Clock control register for receiver clock divisor and receiver and transmitter clock routing
- Selectable full/half duplex, autoecho and local loop-back modes
- Selectable parity (enable, odd, even) and CRC (control field enable, CRC-16, CCITT V.41, VRC/LRC)

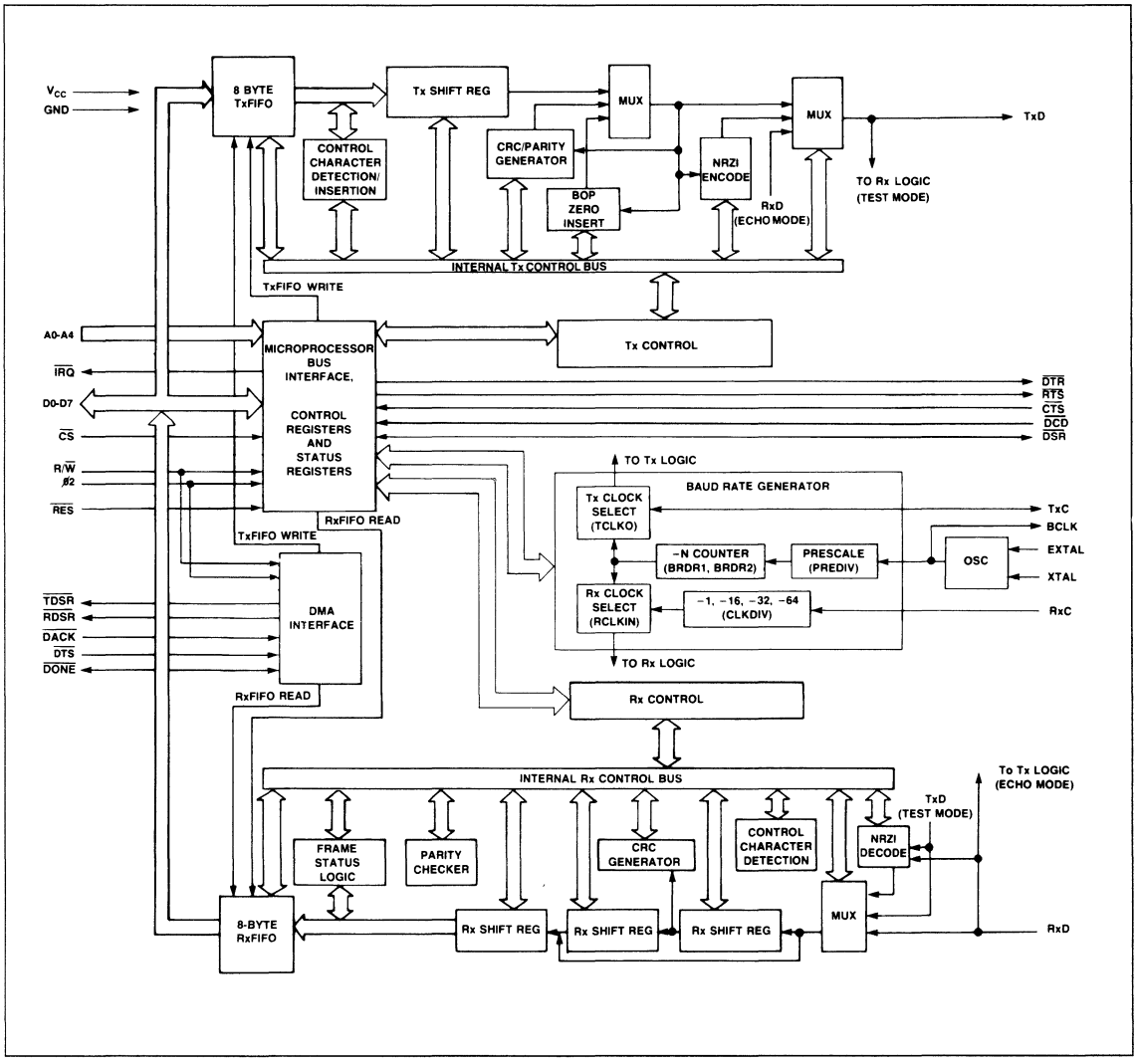


Figure 1. MPCC Block Diagram

PIN DESCRIPTION

Throughout the document, signals are presented using the terms active and inactive or asserted and negated independent of whether the signal is active in the high-voltage state or low-voltage state. (The active state of each logic pin is described below.) Active low signals are denoted by a superscript bar. R/$\overline{W}$ indicates a write is active low and a read active high.

A0 – A4—Address Lines. A0 – A4 are active high inputs used in conjunction with the $\overline{CS}$ input to access the internal registers. The address map for these registers is shown in Table 1.

D0 – D7—Data Lines. The bidirectional data lines transfer data between the MPCC and the CPU, memory or other peripheral device. The data bus is tri-stated when $\overline{CS}$ is inactive. (See exceptions in DMA mode.)

$\overline{CS}$—Chip Select. $\overline{CS}$ low selects the MPCC for programmed transfers with the host. The MPCC is deselected when the $\overline{CS}$ input is inactive in non-DMA mode.

R/$\overline{W}$—Read/Write. R/$\overline{W}$ controls the direction of data flow through the bidirectional data bus by indicating that the current bus cycle is a read (high) or write (low) cycle.

Ø2—Phase 2. During a write (R/$\overline{W}$ low), the Ø2 negative transition latches data on data bus lines D0 – D7 into the MPCC. During a read (R/$\overline{W}$), Ø2 high enables data from the MPCC to data bus

$\overline{IRQ}$—Interrupt Request. The active low $\overline{IRQ}$ output requests interrupt service by the CPU. $\overline{IRQ}$ is driven high after assertion prior to being tri-stated.

$\overline{TDSR}$—Transmitter Data Service Request. When Transmitter DMA mode is active, the low $\overline{TDSR}$ output requests DMA service.

$\overline{RDSR}$—Receiver Data Service Request. When receiver DMA mode is active, the low $\overline{RDSR}$ output requests DMA service.

$\overline{DACK}$—DMA Acknowledge. The $\overline{DACK}$ low input indicates that that the data bus has been acquired by the DMAC and that the requested bus cycle is beginning.

$\overline{DTS}$—DMA Transfer Strobe. The $\overline{DTS}$ low input causes a DMA transfer to occur on the next Ø2 cycle. When R/$\overline{W}$ is high, data is transferred into the TxFIFO; when R/$\overline{W}$ is low, data is transferred from the RxFIFO.

$\overline{DONE}$—Done. $\overline{DONE}$ is a bidirectional active low signal. The $\overline{DONE}$ signal is asserted by the DMAC when the DMA transfer count is exhausted and there is no more data to be transferred. $\overline{DONE}$ will also be asserted by the MPCC, if enabled by bit 5 in the RCR, when the status byte folloiwng the last character of a frame (block) is being transferred in response to a $\overline{RDSR}$. The $\overline{DONE}$ signal asserted by the DMAC in response to a $\overline{TDSR}$ will be stored to track with the data byte through the TxFIFO.

$\overline{RES}$—Reset. $\overline{RES}$ is an active low, high impedance input that initializes all MPCC functions. $\overline{RES}$ must be asserted for at least 500 ns to initialize the MPCC.

$\overline{DTR}$—Data Terminal Ready. The $\overline{DTR}$ active low output is general purpose in nature, and is controlled by the DTRLVL bit in the Serial Interface Control Register (SICR)

$\overline{RTS}$—Request to Send. The $\overline{RTS}$ active low output is general

$\overline{CTS}$—Clear to Send. The $\overline{CTS}$ active low input positive transition and level are reported in the CTS and CTSLVL bits in the Serial Interface Status Register (SISR), respectively.

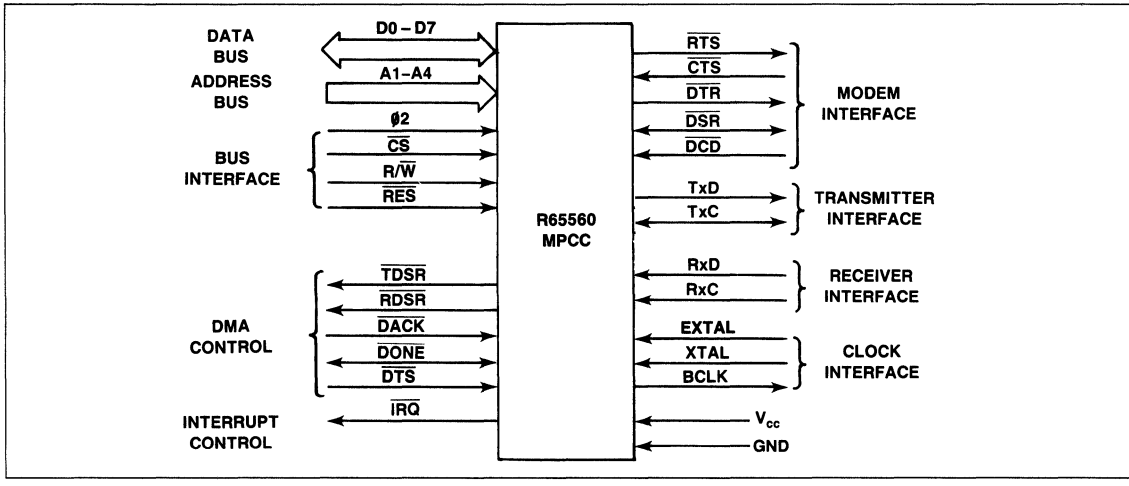


Figure 2. MPCC Input and Output Signals

$\overline{DSR}$—Data Set Ready. The $\overline{DSR}$ active low input negative transition and level are reported in the DSRT and DSRLVL bits in the SISR, respectively. $\overline{DSR}$ is also an output for RSYN.

$\overline{DCD}$—Data Carrier Detect. The $\overline{DCD}$ active low input positive transition and level are reported in the DCDT and DCDLVL bits in the the SISR, respectively.

TxD—Transmitted Data. The MPCC transmits serial data on the TxD output. The TxD output changes on the negative going edge of TxC.

RxD—Received Data. The MPCC receives serial data on the RxD input. The RxD input is shifted into the receiver with the negative going edge of RxC.

TxC—Transmitter Clock. TxC can be programmed to be an input or an output. When TxC is selected to be an input, the transmitter clock must be provided externally. When TxC is programmed to be an output, a clock is generated by the MPCC's internal baud rate generator. The low-to-high transition of the clock signal nominally indicates the center of a serial data present on the TxD output.

RxC—Receiver Clock. RxC provides the MPCC receiver with received data timing information. The clock transition from low-to-high nominally indicates the center of each serial data bit on the RxD input.

EXTAL—Crystal/External Clock Input.
XTAL Crystal Return. EXTAL and XTAL connect an 8 MHz external crystal to the MPCC internal oscillator. The pin EXTAL may also be used as a TTL level input to supply a DC to 8 MHz reference timing from an external clock source. XTAL must be tied to ground when applying an external clock to the EXTAL input.

BCLK—Buffered Clock. BCLK is the internal oscillator buffered output available to other MPCC devices eliminating the need for additional crystals.

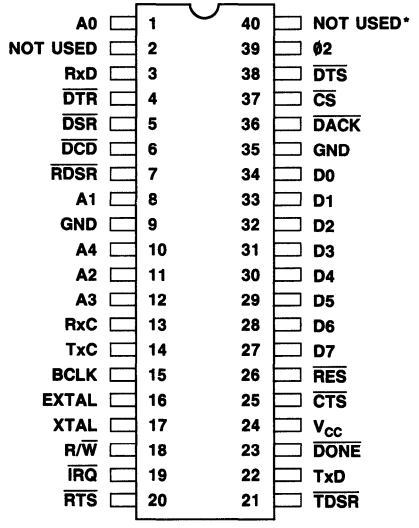
Vcc—Power. 5V ±5%.

GND—Ground. Ground (V_{SS}).

MPCC REGISTERS

Nineteen 8-bit registers define, control and monitor the data communications process. These registers and their access are listed in Table 1.

Table 2 summarizes the MPCC register bit assignments and their access. A read from an unassigned location results in a read from a "null register." A null register returns all ones for data and results in a normal bus cycle. Unused bits of a defined register are read as zeros unless otherwise noted.



*Must be connected to V_{CC}.

R65560

Pin Configuration

Table 1. R65560 Accessible Registers

Register(s)	R/W	Addr (Hex.)	Address Lines A4	A3	A2	A1	A0
7 0							
Receiver Status Register (RSR)	R/W	00	0	0	0	0	0
Receiver Control Register (RCR)	R/W	01	0	0	0	0	1
Receiver Data Register (RDR)[1]	R	02	0	0	0	1	0
Receiver Interrupt Enable Register (RIER)	R/W	05	0	0	1	0	1
Transmitter Statue Register (TSR)	R/W	08	0	1	0	0	0
Transmitter Control Register (TCR)	R/W	09	0	1	0	0	1
Transmitter Data Register (TDR)[2]	W	0A	0	1	0	1	0
Transmitter Interrupt Enable Register (TIER)	R/W	0D	0	1	1	0	1
Serial Interface Status Register (SISR)	R/W	10	1	0	0	0	0
Serial Interface Control Register (SICR)	R/W	11	1	0	0	0	1
Serial Interrupt Enable Register (SIER)	R/W	15	1	0	1	0	1
Protocol Select Register 1 (PSR1)	R/W	18	1	1	0	0	0
Protocol Select Register 2 (PSR2)	R/W	19	1	1	0	0	1
Address Register 1 (AR1)	R/W	1A	1	1	0	1	0
Address Register 2 (AR2)	R/W	1B	1	1	0	1	1
Baud Rate Divider Register 1 (BRDR1)	R/W	1C	1	1	1	0	0
Baud Rate Divider Register 2 (BRDR2)	R/W	1D	1	1	1	0	1
Clock Control Register (CCR)	R/W	1E	1	1	1	1	0
Error Control Register (ECR)	R/W	1F	1	1	1	1	1

Notes:
1. Accessible register of the eight byte RxFIFO. The data is not initialized, however, $\overline{RES}$ resets the RxFIFO pointer to the start of the first byte.
2. Accessible register of the eight byte TxFIFO. The data is not initialized, however, $\overline{RES}$ resets the TxFIFO pointer to the start of the first byte.
3. Reserved registers may contain random bit values.

Table 2. MPCC Register Bit Assignments

R/W Access	Bit Number 7	6	5	4	3	2	1	0	Reset** Value	
R/W	RDA	EOF	0	C/PERR	FRERR	ROVRN	RA/B	RIDLE	00	Receiver Status Register (RSR)
R/W	0	RDSREN	DONEEN	RSYNEN	STRSYN	0	RABTEN	RRES	01	Receiver Control Register (RCR)
R	RECEIVED DATA (RxFIFO)								— —	Receiver Data Register (RDR)
R/W	RDA IE	EOF IE	0	C/PERR IE	FRERR IE	ROVRN IE	RA/B IE	0	00	Receiver Interrupt Enable Register (RIER)
R/W	TDRA	TFC	0	0	0	TUNRN	TFERR	0	80	Transmitter Status Register (TSR)
R/W	TEN	TDSREN	TICS	0	TLAST	TSYN	TABT	TRES	01	Transmitter Control Register (TCR)
W	TRANSMITTED DATA (TxFIFO)								— —	Transmitter Data Register (TDR)
R/W	TDRA IE	TFC IE	0	0	0	TUNRN IE	TFERR IE	0	00	Transmitter Interrupt Enable Register (TIER)
R/W	CTST	DSRT	DCDT	CTSLVL	DSRLVL	DCDLVL	0	0	00	Serial Interface Status Register (SISR)
R/W	RTSLVL	DTRLVL	0	0	0	ECHO	TEST	0	00	Serial Interface Control Register (SICR)
R/W	CTS IE	DSR IE	DCD IE	0	0	0	0	0	00	Serial Interrupt Enable Register (SIER)
R/W	0	0	0	0	0	0	CTLEX	ADDEX	00	Protocol Select Register 1 (PSR1)
R/W	0	STOP BIT SEL		CHAR LEN SEL		PROTOCOL SEL			00	Protocol Select Register 2 (PSR2)
		SB2	SB1	CL2	CL1	PS3	PS2	PS1		
R/W	BOP ADDRESS/BSC & COP PAD								00	Address Register 1 (AR1)
R/W	BOP ADDRESS/BSC & COP SYN								00	Address Register 2 (AR2)
R/W	BAUD RATE DIVIDER (LSH)								01	Baud Rate Divider Register 1 (BRDR1)
R/W	BAUD RATE DIVIDER (MSH)								00	Baud Rate Divider Register 2 (BRDR2)
R/W	0	0	0	PSCDIV	TCLKO	RCLKIN	CLK SEL		00	Clock Control Register (CCR)
							CK2	CK1		
R/W	PAREN	ODDPAR	0	0	CFCRC	CRCPRE	CRC SEL		04	Error Control Register (ECR)
							CR2	CR1		

Notes:
**RESET = Register contents upon power up or $\overline{RES}$.

REGISTER DEFINITIONS

RECEIVER REGISTERS

Receiver Status Register (RSR)

7	6	5	4	3	2	1	0
RDA	EOF	0	C/PERR	FRERR	ROVRN	RA/B	RIDLE

Reset value = $00

The Receiver Status Register (RSR) contains the status of the receiver including error conditions. Status bits are cleared by writing a 1 into respective positions, by writing a 1 into the RCR RRES bit or by RES. If an EOF, C/PERR, or FRERR is set in the RSR, the data reflecting the error (the first byte or word in the RxFIFO) must be read prior to resetting the corresponding status bit in the RSR. The IRQ output is asserted if any of the conditions reported by the status bits occur and the corresponding interrupt enable bit in the RIER is set.

The RSR format is the same as the frame status format (see below) except as noted.

RSR
7 RDA —Receiver Data Available. (RSR only).
0 The RxFIFO is empty (i.e., no received data is available).
1 Received data is available in the RxFIFO and can be read via the RDR.

RSR
6 EOF —End of Frame.
0 No end of frame or block detected.
1 End of frame or block detected (BOP and BSC).

RSR
5 —Not Used.

RSR
4 C/PERR —CRC/Parity Error.
0 No CRC or parity error detected.
1 CRC error detected (BOP, BSC), Parity error detected (ASYNC, ISOC and COP).

RSR
3 FRERR —Frame Error.
0 No frame error detected.
1 Short Frame or a closing FLAG detected off boundary (BOP), Frame error (ASYNC, ISOC) or receiver overrun.

RSR
2 ROVRN —Receiver Overrun.
0 No receiver overrun detected.
1 Receiver overrun detected. Indicates that receiver data was attempted to be transferred into the RxFIFO when it was full, resulting in loss of received data. The data that is already in RxFIFO are not affected and may be read by the processor.

RSR
1 RA/B —Receiver Abort/Break.
0 Normal Operation.
1 ABORT detected after an opening flag (BOP), ENQ detected in a block of text data (BSC), or BREAK ended (ASYNC).

RSR
0 RIDLE —Receiver Idle. (RSR only).
0 Receiver not idle.
1 15 or more consecutive "1's" have been received and the receiver is in an inactive idle state.

Frame Status (RSR)

7	6	5	4	3	2	1	0
0	EOF	RHW	C/PERR	FRERR	ROVRN	RA/B	0

For the BSC and BOP protocols which have defined message blocks or frames, a "frame status" byte will be loaded into the RxFIFO following the last data byte of each block (see Figure 3). The EOF status in the RSR is then set when the byte/word containing the frame status is the next byte/word to be read from the RxFIFO.

In the receiver DMA mode, when the EOF status in the RSR is set, DONE is asserted to the DMAC. Thus the last byte accessed by the DMAC is always a status byte, which the processor may read to check the validity of entire frame.

The frame status contains all the status contained within the RSR with the exception of RDA and RIDLE.

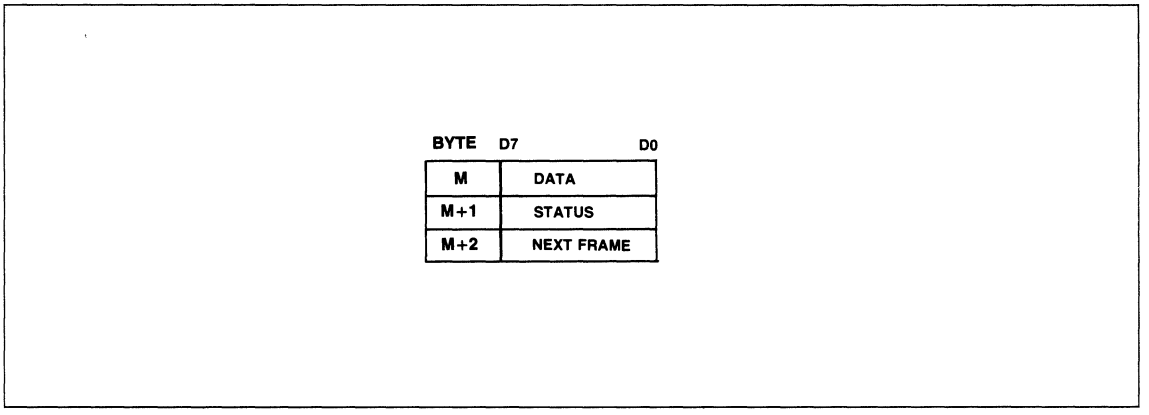


Figure 3. BSC/BOP Block/Frame Status Location

Receiver Control Register (RCR)

7	6	5	4	3	2	1	0
0	RDSREN	DONEEN	RSYNEN	STRSYN	0	RABEN	RRES

Reset value = $01

The Receiver Control Register (RCR) selects receiver control options.

RCR
7 —**Not used.**

RCR
6 RDSREN —Receiver Data Service Request Enable.
0 Disable receiver DMA mode.
1 Enable receiver DMA mode.

RCR
5 DONEEN —$\overline{\text{DONE}}$ Output Enable.
0 Disable $\overline{\text{DONE}}$ output.
1 Enable $\overline{\text{DONE}}$ output. (When the receiver is in the DMA mode, i.e., RDSREN = 1).

RCR
4 RSYNEN —RSYNEN Output Enable. Selects the DSR signal input or the RSYN SYNC signal output on the $\overline{\text{DSR}}$ pin.
0 Input DSR on $\overline{\text{DSR}}$.
1 Output RSYN on $\overline{\text{DSR}}$.

RCR
3 STRSYN —Strip SYN Character (COP only).
0 Do not strip SYN character.
1 Strip SYN character.

RCR
2 MUST BE ZERO
0

RCR
1 RABTEN —Receiver Abort Enable (BOP only).
0 Do not abort frame upon error detection.
1 Abort frame upon RxFIFO overrun (ROVRN bit = 1 in the RSR) or CFCRC error detection (C/PERR bit = 1 in the RSR). If either error occurs, the MPCC ignores the remainder of the current frame and searches for the beginning of the next frame.

RCR
0 RRES —Receiver Reset Command.
0 Enable normal receiver operation.
1 Reset receiver. Resets the receiver section including the RxFIFO and the RSR (but not the RCR). RRES is set by $\overline{\text{RES}}$ or by writing a 1 into this bit for one write cycle and is cleared by writing a 0 into this bit. RRES requires clearing after $\overline{\text{RES}}$.

Receiver Data Register (RDR)

7	6	5	4	3	2	1	0
MSB			Received Data (RxFIFO)				LSB

The receiver has an 8-byte First In First Out (FIFO) register file (RxFIFO) where received data are stored before being transferred to the bus. The received data is transferred out of the RxFIFO via the RDR. When the RxFIFO has a data byte ready to be transferred, the RDA status bit in the RSR is set to 1.

Receiver Interrupt Enable Register (RIER)

7	6	5	4	3	2	1	0
RDA IE	EOF IE	0	C/PERR IE	FRERR IE	ROVRN IE	RA/B IE	—

Reset value = $00

The Receiver Interrupt Enable Register (RIER) contains interrupt enable bits for the Receiver Status Register (RSR). When enabled, the $\overline{IRQ}$ output is asserted when the corresponding condition is detected and reported in the RSR.

RIER
7 RDA IE —Receiver Data Available Interrupt Enable.
0 Disable RDA Interrupt.
1 Enable RDA Interrupt.

RIER
6 EOF IE —End of Frame Interrupt Enable.
0 Disable EOF Interrupt.
1 Enable EOF Interrupt.

RIER
5 —Not used.

RIER
4 C/PERR IE —CRC/Parity Error Interrupt Enable.
0 Disable C/PERR Interrupt.
1 Enable C/PERR Interrupt.

RIER
3 FRERR IE —Frame Error Interrupt Enable.
0 Disable FRERR Interrupt.
1 Enable FRERR Interrupt.

RIER
2 ROVRN IE —Receiver Overrun Interrupt Enable.
0 Disable ROVRN Interrupt.
1 Enable ROVRN Interrupt.

RIER
1 RA/B IE —Receiver Abort/Break Interrupt Enable.
0 Disable RA/B Interrupt.
1 Enable RA/B Interrupt.

RIER
0 —Not used.

TRANSMITTER REGISTERS

Transmitter Status Register (TSR)

7	6	5	4	3	2	1	0
TDRA	TFC	0	0	0	TUNRN	TFERR	0

Reset value = $80

The Transmitter Status Register (TSR) contains the transmitter status including error conditions. The transmitter status bits are cleared by writing a 1 into their respective positions, by writing a 1 into the TCR TRES bit, or by $\overline{RES}$. The $\overline{IRQ}$ output is asserted if any of the conditions reported by the status bits occur and the corresponding interrupt enable bit in the TIER is set.

TSR
7 TDRA —Transmitter Data Register Available.
0 The TxFIFO is full.
1 The TxFIFO is not full (i.e., available) and data to transmit can be loaded via the TDR.

TSR
6 TFC —Transmitted Frame Complete. (BOP, BSC and COP only).
0 Frame not complete.
1 Closing FLAG or ABORT character has been transmitted (BOP), Trailing PAD has been transmitted (BSC), or the last character of a frame or block as defined by TLAST (TCR bit 3) has been transmitted (COP).

TSR
5-3 —Not used.

TSR
2 TUNRN —Transmitter Underrun (BOP, BSC and COP only). A transmitter underrun occurs when the transmitter runs out of data during a transmission. For BOP, the underrun condition is treated as an abort. For BSC and COP, SYN characters are transmitted until more data is available in the TxFIFO.
0 No transmitter underrun occurred.
1 Transmitter underrun occurred.

TSR
1 TFERR —Transmit Frame Error (BOP only).
0 No frame error has occurred.
1 No control field was present (short frame).

Transmitter Control Register (TCR)

7	6	5	4	3	2	1	0
TEN	TDSREN	TICS	0	TLAST	TSYN	TABT	TRES

Reset value = $01

The Transmitter Control Register (TCR) selects transmitter control function.

TCR
7 TEN —Transmitter Enable.
0 Disable transmitter. TxD output is idled. The TxFIFO may be loaded while the transmitter is disabled.
1 Enable transmitter.

TCR
6 **TDSREN** —**Transmitter Data Service Request Enable.**
0 Disable transmitter DMA mode.
1 Enable transmitter DMA mode.

TCR
5 **TICS** —**Transmitter Idle Character Select.** Selects the idle character to be transmitted when the transmitter is in an active idle mode (transmitter enabled or disabled).
0 Mark Idle (TxD output is held high).
1 Content of AR2 (BSC and COP), BREAK condition (ASYNC and ISOC), or FLAG character (BOP).

TCR
4 —**Not Used.** This bit is initialized to 0 by $\overline{RES}$ and must not be set to 1.

TCR
3 **TLAST** —**Transmit Last Character** (BOP, BSC and COP only).
0 The next character is not the last character in a frame or block.
1 The next character to be written into the TDR is the last character of the message. The TLAST bit automatically returns to a 0 when the associated word/byte is written to the TxFIFO. If the transmitter DMA mode is enabled, TLAST is set to a 1 by $\overline{DONE}$ from the DMAC. In this case the character written into the TDR in the current cycle is the last character.

TCR
2 **TSYN** —**Transmit SYN** (BSC and COP only).
0 Do not transmit SYN characters.
1 Transmit SYN characters. Causes a pair of SYN characters to be transmitted immediately following the current character. If BSC transparent mode is active, a DLE SYN sequence is transmitted. The TSYN bit automatically returns to a 0 when the SYN character is loaded into the Transmitter Shift Register.

TCR
1 **TABT** —**Transmit ABORT** (BOP only).
0 Enable normal transmitter operation.
1 Causes an abort by sending eight consecutive 1's. A data word/byte must be loaded into the TxFIFO after setting this bit in order to complete the command. The TABT bit clears automatically when the subsequent data word/byte is loaded into the TxFIFO.

TCR
0 **TRES** —**Transmitter Reset Command.**
0 Enable normal transmitter operation.
1 Reset transmitter. Clears the transmitter section including the TxFIFO and the TSR (but not the TCR). The TxD output is held in "Mark" condition. TRES is set by $\overline{RES}$ or by writing a 1 into this bit for one write cycle and is cleared by writing a 0 into this bit. TRES requires clearing after $\overline{RES}$.

Transmit Data Register (TDR)

7	6	5	4	3	2	1	0
MSB			Transmitted Data (TxFIFO)				LSB

The transmitter has an 8-byte FIFO register file (TxFIFO). Data to be transmitted is transferred from the bus into the TxFIFO via the TDR. The TDRA status bit in the TSR is set to 1 when the TxFIFO is ready to accept another data byte.

Transmitter Interrupt Enable Register (TIER)

7	6	5	4	3	2	1	0
TDRA IE	TFC IE	0	0	0	TUNRN IE	TFERR IE	—

Reset value = $00

The Transmitter Interrupt Enable Register (TIER) contains interrupt enable bits for the Transmitter Status Register. When enabled, the $\overline{IRQ}$ output is asserted when the corresponding condition is detected and reported in the TSR.

TIER
7 **TDRA IE** —**Transmitter Data Register (TDR) Available Interrupt Enable.**
0 Disable TDRA Interrupt.
1 Enable TDRA Interrupt.

TIER
6 **TFC IE** —**Transmit Frame Complete (TFC) Interrupt Enable.**
0 Disable TFC Interrupt.
1 Enable TFC Interrupt.

TIER
5-3 —**Not used.**

TIER
2 **TUNRN IE** —**Transmitter Underrun (TUNRN) Interrupt Enable.**
0 Disable TUNRN Interrupt.
1 Enable TUNRN Interrupt.

TIER
1 **TFERR IE** —**Transmit Frame Error (TFERR) Interrupt Enable.**
0 Disable TFERR Interrupt.
1 Enable TFERR Interrupt.

TIER
0 —**Not used.**

SERIAL INTERFACE REGISTERS

Serial Interface Status Register (SISR)

7	6	5	4	3	2	1	0
CTST	DSRT	DCDT	CTSLVL	DSRLVL	DCDLVL	0	0

Reset value = $00

The Serial Interface Status Register (SISR) contains the serial interface status information. The transition status bits (CTST, DSRT and DCDT) are cleared by writing a 1 into their respective positions, or by RESET. The level status bits (CTSLVL, DSRLVL and DCDLVL) reflect the state of their respective inputs and cannot be cleared internally. The IRQ output is asserted if any of the conditions reported by the transition status bits occur and the corresponding interrupt enable bit in the SIER is set.

SISR
7 CTST —Clear to Send Transition Status.
1 CTS has transitioned positive (from active to inactive). (TRES must be a zero).
0 CTS has not transitioned positive.

SISR
6 DSRT —Data Set Ready Transition Status.
1 DSR has transitioned negative (from inactive to active).
0 DSR has not transitioned negative.

SISR
5 DCDT —Data Carrier Detect Transition Status.
1 DCD has transitioned positive (from active to inactive).
0 DCD has not transitioned positive.

SISR
4 CTSLVL —Clear to Send Level.
0 CTS input level is negated (high).
1 CTS input level is asserted (low).

SISR
3 DSRLVL —Data Set Ready Level.
0 DSR input level is negated (high).
1 DSR input level is asserted (low).

SISR
2 DCDLVL —Data Carrier Detect Level.
0 DCD input level is negated (high).
1 DCD input level is asserted (low).

SISR
1-0 —Not used.

Serial Interface Control Register (SICR)

7	6	5	4	3	2	1	0
RTSLVL	DTRLVL	—	—	—	ECHO	TEST	0

Reset value = $00

The Serial Interface Control Register (SICR) controls various serial interface signals and test functions.

SICR
7 RTSLVL —Request to Send Level.
0 Negate RTS output (high).
1 Assert RTS output (low).

NOTE

In BOP, BSC, or COP, when the RTSLVL bit is cleared in the middle of data transmission, the RTS output remains asserted until the end of the current frame or block has been transmitted. In ASYNC or ISOC, the RTS output is negated when the TxFIFO is empty. If the transmitter is idling when the RTSLVL bit is reset, the RTS output is negated within two bit times.

SICR
6 DTRLVL —Data Terminal Ready Level.
0 Negate DTR output (high).
1 Assert DTR output (low).

SICR
5-3 —Not used. These bits are initialized to 0 by RESET and must not be set to 1.

SICR
2 ECHO —Echo Mode Enable.
0 Disable Echo mode (enable normal operation).
1 Enable Echo mode. Received data (RxD) is routed back through the transmitter to TxD. The contents of the TxFIFO is undisturbed. This mode may be used for remote test purposes.

SICR
1 TEST —Self-test Enable.
0 Disable self-test (enable normal operation).
1 Enable self-test. The transmitted data (TxD) and clock (TxC) are routed back through to the receiver through RxD and RxC, respectively (DCD and CTS are ignored). This "loopback" self-test may be used for all protocols. RxC is external regardless of the state of CCR bit 2. CCR bit 3 may be a 0 or a 1.

SICR
0 MUST BE ZERO
0

Serial Interrupt Enable Register (SIER)

7	6	5	4	3	2	1	0
CTS IE	DSR IE	DCD IE	—	—	—	—	—

Reset value = $00

The Serial Interrupt Enable Register (SIER) contains interrupt enable bits for the Serial Interface Status Register. When an interrupt enable bit is set, the $\overline{IRQ}$ output is asserted when the corresponding condition occurs as reported in the SISR.

SIER
7 CTS IE —Clear to Send (CTS) Interrupt Enable.
0 Disable CTS Interrupt.
1 Enable CTS Interrupt.

SIER
6 DSR IE —Data Set Ready (DSR) Interrupt Enable.
0 Disable DSR Interrupt.
1 Enable DSR Interrupt.

SIER
5 DCD IE —Data Carrier Detect (DCD) Interrupt Enable.
0 Disable DCD Interrupt.
1 Enable DCD Interrupt.

SIER
4-0 —Not used.

GLOBAL REGISTERS

The global registers contain command information applying to different modes of operation and protocols. After changing global register data, TRES in the TCR and RRES in the RCR should be set then cleared prior to performing normal mode processing.

Protocol Select Register 1 (PSR1)

7	6	5	4	3	2	1	0
—	—	—	—	—	—	CTLEX	ADDEX

Reset value = $00

Protocol Select Register 1 (PSR1) selects BOP protocol related options.

PSR1
7-2 —Not used.

PSR1
1 CTLEX —Control Field Extend (BOP only).
0 Select 8-bit control field.
1 Select 16-bit control field.

PSR1
0 ADDEX —Address Extend (BOP only).
0 Disable address extension. All eight bits of the address byte are utilized for addressing.
1 Enable address extension. When bit 0 in the address byte is a 0 the address field is extended by one byte. An exception to the address field extension occurs when the first address byte is all 0's (null address).

Protocol Select Register 2 (PSR2)

7	6	5	4	3	2	1	0
WD/BYT	STOP BIT SEL		CHAR LEN SEL		PROTOCOL SEL		
	SB2	SB1	CL2	CL1	PS3	PS2	PS1

Reset value = $00

Protocol Select Register 2 (PSR2) selects protocols, character size, the number of stop bits, and word/byte mode.

PSR2
7 —Not Used. This bit is initialized to 0 by $\overline{RES}$ and must not be changed to 1.

PSR2
6-5 STOP BIT SEL —Number of Stop Bits Select. Selects the number of stop bits transmitted at the end of the data bins in ASYNC and ISOC modes.

6 SB2	5 SB1	No. of Stop Bits ASYNC	No. of Stop Bits ISOC
0	0	1	1
0	1	1-1/2	2
1	0	2	2

PSR2
4-3 CHAR LEN SEL —Character Length Select. Selects the character length except in BOP and BSC where the character length is always eight bits. Parity is not included in the character length.

4 CL2	3 CL1	Character Length
0	0	5 bits
0	1	6 bits
1	0	7 bits
1	1	8 bits

PSR2
2-0 PROTOCOL SEL—Protocol Select. Selects protocol and defines the protocol dependent control bits.

2 PS3	1 PS2	0 PS1	Protocol
0	0	0	BOP (Primary)
0	0	1	BOP (Secondary)
0	1	0	Reserved
0	1	1	COP
1	0	0	BSC EBCDIC
1	0	1	BSC ASCII
1	1	0	ASYNC
1	1	1	ISOC

Address Register 1 (AR1)

7	6	5	4	3	2	1	0
BOP ADDRESS/BSC & COP PAD							

Reset value = $00

Address Register 2 (AR2)

7	6	5	4	3	2	1	0
BSC & COP SYN							

Reset value = $00

The protocol selected in PSR2 (BOP, BSC and COP only) determines the function of the two 8-bit Address Registers (AR1 and AR2). As a secondary station in BOP, the contents of AR1 is used for address matching. In BSC and COP, AR1 and AR2 contain programmable leading PAD and programmable SYN characters, respectively.

Address Register (AR) Contents

Protocol Selected	AR1	AR2
BOP (Primary)	X	X
BOP (Secondary)	Address	X
BSC EBCDIC	Leading PAD	SYN
BSC ASCII	Leading PAD	SYN
COP	Leading PAD	SYN
*X = Not used		

Baud Rate Divider Register 1 (BRDR1)

7	6	5	4	3	2	1	0
BAUD RATE DIVIDER (LSH)							

Reset value = $01

Baud Rate Divider Register 2 (BRDR2)

7	6	5	4	3	2	1	0
BAUD RATE DIVIDER (MSH)							

Reset value = $00

The two 8-bit Baud Rate Divider Registers (BRDR1 and BRDR2) hold the divisor of the Baud Rate Divider circuit. BRDR1 contains the least significant half (LSH) and BRDR2 contains the most significant half (MSH), With an 8.064 MHz EXTAL input, standard bit rates can be selected using the combination of Prescaler Divider (in the CCR) and Baud Rate Divider values shown in Table 3. For isochronous or synchronous protocols, the Baud Rate Divider value must be multiplied by two for the same Prescaler Divider value.

The Baud Rate Divider (BRD) value can be computed for other crystal frequency, prescaler divider and desired baud rate values as follows:

$$BRD = \frac{\text{Crystal Frequency}}{\text{(Prescaler Divider) (Baud Rate) (K)}}$$

where: K = 1 for isochronous or synchronous
2 for asynchronous

Clock Control Register (CCR)

7	6	5	4	3	2	1	0
—	—	—	PSCDIV	TCLKO	RCLKIN	CLK SEL	
						CK2	CK1

Reset value = $00

The CCR selects various clock options.

CCR 7-5 —**Not used.**

CCR 4 PSCDIV —**Prescaler Divider.** The Prescaler Divider network reduces the external/oscillator frequency to a value for use by the internal Baud Rate Generator.

0 Divide by 2.
1 Divide by 3.

CCR 3 TCLKO —**Transmitter Clock Output Select.**

0 Select TxC to be an input.
1 Select TxC to be an output. (1 X clock)

CCR 2 RCLKIN —**Receiver Clock Internal Select** (ASYNC only).

0 Select External RxC.
1 Select Internal RxC.

CCR 1-0 CLK DIV —**External Receiver Clock Divider.** Selects the divider of the external RxC to determine the receiver data rate.

CK2	CK1	Divider
0	0	1 (ISOC)
0	1	16
1	0	32
1	1	64

Table 3. Standard Baud Selection (8.064 MHz Crystal)

Desired Baud Rate (Bit Rate)	Prescaler Divider		Baud Rate Divider					
			Asynchronous			Isochronous and Synchronous		
				Hexadecimal Value			Hexadecimal Value	
	Decimal Value	PSCDIV (0 to 1)	Decimal Value	BRDR2 (MSH)	BRDR1 (LSH)	Decimal Value	BRDR2 (MSH)	BRDR1 (LSH)
50	3	1	26,880	69	00	53,760	D2	00
75	2	0	26,880	69	00	53,760	D2	00
110	3	1	12,218	2F	BA	24,436	5F	74
135	2	0	14,933	3A	55	29,866	74	AA
150	3	1	8,960	23	00	17,920	46	00
300	2	0	6,720	1A	40	13,440	34	80
1200	3	1	1,120	04	60	2,240	08	C0
1800	2	0	1,120	04	60	2,240	08	C0
2400	2	0	840	03	48	1,680	06	90
3600	2	0	560	02	30	1,120	04	60
4800	3	1	280	01	18	560	02	30
7200	2	0	280	01	18	560	02	30
9600	3	1	140	00	8C	280	01	18
19200	3	1	70	00	46	140	00	8C
38400	3	1	35	00	23	70	00	46

Error Control Register (ECR)

7	6	5	4	3	2	1	0
PAREN	ODDPAR	—	—	CFCRC	CRCPRE	CRCSEL	
						CR2	CR1

Reset value = $04

The Error Control Register (ECR) selects the error detection method used by the MPCC.

ECR
7 PAREN —Parity Enable. (ASYNC, ISOC and COP only).
0 Disable parity generation/checking.
1 Enable parity generation/checking.

ECR
6 ODDPAR —Odd/Even Parity Select (Effective only when PAREN = 1).
0 Generate/check even parity.
1 Generate/check odd parity.

ECR
5-4 —Not used.

ECR
3 CFCRC —Control Field CRC Enable.
0 Disable control field CRC. Enables an intermediate CRC remainder to be appended after the address/control field in transmitted BOP frames and checked in received frames. The CRC generator is reset after control field CRC calculation.

ECR
2 CRCPRE —CRC Generator Preset Select.
0 Preset CRC Generator to 0.
1 Preset CRC Generator to 1 and transmit the 1's complement of the resulting remainder.

ECR
1-0 CRCSEL —CRC Polynomial Select. Selects one of the RC polynominals.

1 CR2	0 CR1	Polynominal
0	0	$x^{16}+x^{12}+x^5+1$ (CCITT V.41)
0	1	$x^{16}+x^{15}+x^2+1$ (CRC-16)
1	0	x^8+1 (VRC/LRC)*
1	1	Not used.

*VRC: Odd-parity check is performed on each character including the LRC character.

INPUT/OUTPUT FUNCTIONS

MPU INTERFACE

Transfer of data between the MPCC and the system bus involves the following signals: Address lines A0 through A4, Data Bus Lines D0 through D7, and control signals consisting of R/$\overline{W}$, $\overline{CS}$, and Ø2. Figures 10 and 11 show typical interface connections.

Read/Write Operation

The R/$\overline{W}$ input controls the direction of data flow on the data bus. $\overline{CS}$ (Chip Select) enables the MPCC for access to the internal registers and other operations. When $\overline{CS}$ is asserted, the data I/O buffer acts as an output driver during a read operation and as an input buffer during a write operation.

When the MPCC is selected (CS low) during a read (R/$\overline{W}$ high), eight bits of register data are placed on data bus lines D0 – D7 when Ø2 is asserted. When the MPCC is selected ($\overline{CS}$ low) for a write (R/$\overline{W}$ low), Ø2 strobes data from the D0 – D7 data lines into the selected register. Figures 12 and 13 show the read and write timing relationships.

DMA INTERFACE

The MPCC is capable of providing DMA data transfers up to 2 Mbytes per second when used with the MC68440 DMAC in the single address mode. Based on 4 Mb/s serial data rate and 5 bits/character, the maximum DMA required transfer rate is 800 Kbytes per second.

The MPCC has separate DMA enable bits for the transmitter and receiver, each of which requires a DMA channel. Both the transmitter and receiver data are implicitly addressed (TDR or RDR) therefore addressing of the data register is not required before data may be transferred. Communication between the MPCC and the DMAC is accomplished by a two-signal request/acknowledge handshake. Since the MPCC has only one acknowledge input ($\overline{DACK}$) for its two DMA request lines, an external OR function must be provided to combine the two DMA acknowledge signals. The MPCC uses the R/$\overline{W}$ input to distinguish between the Transmitter Data Service Request ($\overline{TDSR}$ acknowledge and the Receiver Data Service Request ($\overline{RDSR}$) acknowledge.

Receiver DMA Mode

The receiver DMA mode is enabled when the RDSREN bit in the RCR is set to 1. When data is available in the RxFIFO, Receiver Data Service Request ($\overline{RDSR}$) is asserted for one receiver clock period (BOP and BSC) to initiate the MPCC to memory DMA transfer. For asynchronous operation, $\overline{RDSR}$ is asserted for 2-3 periods of the system clock depending on prescale factor. The next $\overline{RDSR}$ cycle may be initiated as soon as the current $\overline{RDSR}$ cycle is completed (i.e., a full sequence of $\overline{DACK}$, Ø2, and $\overline{DTS}$).

In response to $\overline{RDSR}$ assertion, the DMAC sets the R/$\overline{W}$ line to write and asserts the memory address, DMA transfer strobe ($\overline{DTS}$), and DMA acknowledge ($\overline{DACK}$). The MPCC outputs data from the RxFIFO to the data bus during Ø2. The memory latches the data to complete the data transfer. Figure 13 shows the timing relationships for the receiver DMA mode.

$\overline{RDSR}$ is inhibited when either RDSREN is reset to 0 or RRES is set to 1 (both in the RCR), or when $\overline{RES}$ is asserted.

Transmitter DMA Mode

The transmitter DMA mode is enabled when the TDSREN bit in the TCR is set to 1. When the TxFIFO is available, Transmitter Data Service Request ($\overline{TDSR}$) is asserted for one transmitter clock period to initiate the memory to MPCC DMA transfer. For asynchronous operation, $\overline{TDSR}$ is asserted for a period of one-half the transmitter baud rate. The next $\overline{TDSR}$ cycle may be initiated as soon as the current $\overline{TDSR}$ cycle is completed.

In the transmitter DMA mode, the TxFIFO Is implicitly addressed. That is, when the transfer is from memory to the TxFIFO, only the memory is addressed. In response to $\overline{TDSR}$ assertion, the DMAC sets the R/$\overline{W}$ line to read and asserts the memory address, DMA transfer strobe ($\overline{DTS}$) and DMA acknowledge ($\overline{DACK}$). The The memory places data on the data bus and the MPCC loads the data into the TxFIFO to complete the data transfer. A timing diagram for the transmitter DMA mode is shown in Figure 15.

$\overline{TDSR}$ is inhibited when either TDSREN is reset to 0 or TRES is set to 1 (both in the TCR), or when $\overline{RES}$ is asserted.

$\overline{DONE}$ Signal

When the DMA transfer count is exhausted in transmitter DMA mode, the DMAC asserts $\overline{DONE}$ which sets the TLAST bit in the TCR to indicate that the last word/byte has been transferred. In the receiver DMA mode, $\overline{DONE}$ is asserted by the MPCC when the last character of the frame/block is being transferred from the RxFIFO to the data bus if the DONEEN bit is set to a 1 in the RCR.

CAUTION

$\overline{DONE}$ is reasserted for each occurence of $\overline{DACK}$ until EOF is cleared in the RSR.

INTERRUPTS

There are three possible sources of an interrupt request ($\overline{IRQ}$): the receiver section (as reported in the RSR), the transmitter section (as reported in the TSR), and the serial interface (as reported in the SISR). When an interrupt generating status occurs and the interrupt is enabled by a corresponding bit in the associated interrupt enable register, $\overline{IRQ}$ is asserted. The interrupt processing software must examine all status registers that have interrupt status bits enabled to determine the cause of the interrupt and perform the required processing to clear the interrupt. $\overline{IRQ}$ will remain asserted until all interrupt causing conditions reported in status registers have been cleared.

SERIAL INTERFACE

The MPCC is a high speed, high performance device supporting the more popular bit and character oriented data protocols. The lower speed asynchronous (ASYNC) and isochronous (ISOCH) modes are also supported. An on-chip clock oscillator and baud rate generator provide an output data clock at a frequency of DC to 4 MHz. The clock can also be used in the ASYNC mode to provide a receive clock for the incoming data. The serial interface consists of the following signals:

$\overline{RTS}$ (Request to Send) Output

The $\overline{RTS}$ output to the DCE is controlled by the RTSLVL bit in the SICR in conjunction with the state of the transmitter section. When the RTSLVL bit is set to 1, the $\overline{RTS}$ output is asserted. When the RTSLVL bit is reset to 0, the $\overline{RTS}$ output remains asserted until the TxFIFO becomes empty or the end of the message (or frame), complete with CRC code if any, has been transmitted. $\overline{RTS}$ also is negated when the RTSLVL bit is reset during transmitter idle, or when the $\overline{RES}$ input is asserted.

$\overline{CTS}$ (Clear to Send) Input

The $\overline{CTS}$ input signal is normally generated by the DCE to indicate whether or not the data set is ready to receive data. The $\overline{CTST}$ bit in the SISR reflects the transition status of the $\overline{CTS}$ input while the CTSLVL bit in the SISR reflects the current level. A positive transition on the $\overline{CTS}$ pin asserts $\overline{IRQ}$ if the CTS IE bit in the SIER is set. The $\overline{CTS}$ input in an inactive state disables the start of transmission of each new frame.

$\overline{DCD}$ (Data Carrier Detect) Input

The $\overline{DCD}$ input signal is normally generated by the DCE and indicates that the DCE is receiving a data carrier signal suitable for demodulation. The $\overline{DCDT}$ bit in the SISR reports the transition status of the $\overline{DCD}$ input while the DCDLVL bit in the SISR contains the current level. A positive transition on the $\overline{DCD}$ pin asserts the $\overline{IRQ}$ output if the DCD IE bit in the SIER is set. A negated DCD input disables the start of the receiver but does not stop the operation of an incoming message already in progress.

$\overline{DSR}$ (Data Set Ready) Input/RSYN Output

The $\overline{DSR}$ input from the DCE indicates the status of the local data set. The $\overline{DSRT}$ bit in the SISR contains the transition status of the $\overline{DSR}$ input while the DSRLVL bit in the SISR reports the current level. A negative transition on the $\overline{DSR}$ pin asserts the $\overline{IRQ}$ output if the DSR IE bit in the SIER is set.

When the RSYN bit in the RCR is set to 1, the frame synchronization signal (RSYN) in the receiver is output on the $\overline{DSR}$ pin. In this mode, $\overline{DSR}$ output low indicates detection of SYN in BSC or COP, or an address match in BOP.

$\overline{DTR}$ (Data Terminal Ready) Output

The $\overline{DTR}$ output is general purpose in nature and can be used to control switching of the DCE. The $\overline{DTR}$ output is controlled by the DTRLVL bit in the SICR.

TxC (Transmitter Clock) Input/Output

The transmitter clock (TxC) may be programmed to be input or an output. When the TCLKO control bit in the CCR is set to a 1, the TxC pin becomes an output and provides the DCE with a clock whose frequency is determined by the internal baud rate generator. When the TCLKO control bit is reset, TxC is an input and the transmitter shift timing must be provided externally. The TxD output changes state on the negative-going edge of the transmitter clock. In the asynchronous mode when TCLKO = 0 in the CCR, the TxC input frequency must be two times the desired baud rate.

TxD (Transmitted Data) Output

The serial data transmitted from the MPCC is coded in NRZ or NRZI (zero complement) data format as selected by the NRZI control bit in the SICR.

RxC (Receiver Clock) Input

The receiver latches data on the negative transition of the RxC.

RxD (Received Data) Input

The serial data received by the MPCC can be coded in NRZ or NRZI data format. The MPCC will decode the received data in accordance with the NRZI control bit setting in the SICR.

Serial Interface Timing

The timing for the serial interface clock and data lines is shown in Figure 16. The MPCC supports high speed synchronous operation. As shown, the TxD output changes with the negative-going edge of TxC and the received data on RxD is latched on the negative edge of RxC. This assures high speed two-way operation between two MPCCs connected as shown in Figure 18.

For low speed operation between the MPCC and a modem or RS-232C Data Communications Equipment (DCE), an inverter can be used in the TxC output lines as shown in Figure 18. RS-232 and RS-423 (covering serial data interface up to 100K baud) require that data be centered ±25% about the negative-going edge of the RxC. This criteria is met for frequencies up to 1.25 MHz using the inverter. Use of the inverter also allows MPCC to MPCC operation up to 2.17 MHz.

SERIAL COMMUNICATION MODES AND PROTOCOLS

ASYNCHRONOUS AND ISOCHRONOUS MODES

Asynchronous and isochronous data are transferred in frames. Each frame consists of a start bit, 5 to 8 data bits plus optional even or odd parity, and 1, 1½, or 2 stop bits. The data character is transmitted with the least significant bit (LSB) first. The data line is normally held high (MARK) between frames, however, a BREAK (minimum of one frame length for which the line is held low) is used for control purposes. Figure 4 illustrates the frame format supported by the MPCC.

Asynchronous Receive

In the asynchronous (ASYNC) mode, data received on RxD occurs in three phases: (1) detection of the start bit and bit synchronization, (2) character assembly and optional parity check, and (3) stop bit detection. The receiver bit stream may be synchronized by the internal baud rate generator clock or by an external clock on RxC. When RCLKIN in the CCR is set to 0, an external clock with a frequency of 16, 32, or 64 times the data rate establishes the data bit midpoint and maintains bit synchronization. The character assembly process does not start if the start bit is less than one-half bit time. Framing and parity errors are detected and buffered along with the character on which errors occurred. They are passed on to the RxFIFO and set appropriate status bits in the RSR when the character with an error reaches the last RxFIFO register where it is ready to be transferred onto the data bus via the RDR.

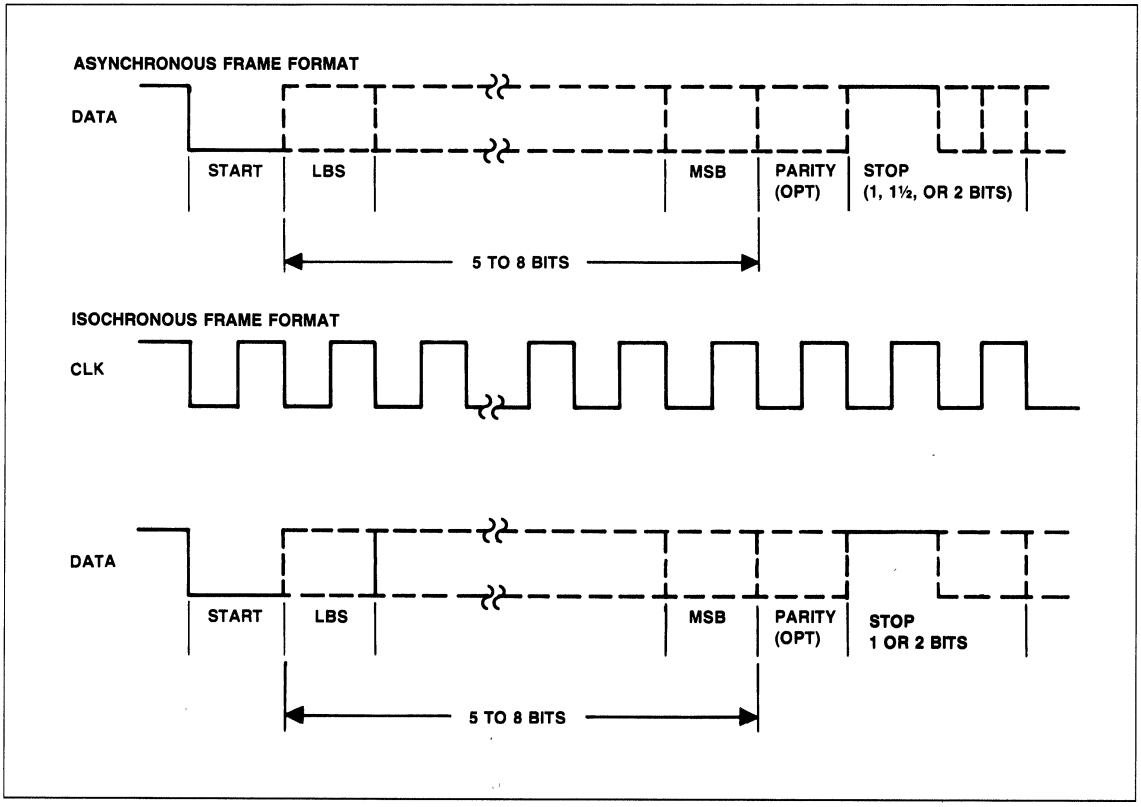


Figure 4. Asynchronous and Isochronous Frame Format

Isochronous Receive

In the isochronous (ISOC) mode, a 1 times clock on RxC is required with the data on RxD and the serial data bit is latched on the falling edge of each clock pulse. The requirement for the detection of a valid start bit, or the beginning of a break, is satisfied by the detection of a high-to-low transition on the serial data input line. Error detection and status indication are the same as the asynchronous mode.

Asynchronous and Isochronous Transmit

In asynchronous and isochronous transmit modes, output data tansmission on TxD begins with the start bit. This is followed by the data character which is transmitted LSB first. If parity generation is enabled, the parity bit is transmitted after the MSB of the character.

SYNCHRONOUS MODES

In synchronous modes, a one-times clock is provided along with the data. Serial output data is shifted out and input data is latched on the falling edge of the clock.

BIT ORIENTED PROTOCOLS (BOP)

In bit oriented protocols (BOP), messages (data) are transmitted and received in frames. Each frame contains an opening flag, address field, control field, frame check sequence, and a closing flag. A frame may also contain an information field. (See Figure 5).

The opening flag is a special character whose bit pattern is 01111110. It marks the frame boundaries and is the interframe fill character. The address field of a frame contains the address of the secondary station which is receiving or responding to a command. The address field may be one or more bytes long. The address field can be extended by setting the ADDEX bit to a 1 in PSR1. In this case, the address field will be extended until the occurrence of an address byte with a 1 in bit 0. The first byte of the address field is automatically checked when the MPCC is programmed to be a secondary station in BOP. An automatic check for global (11111111) or null (00000000) address is also made. The control field of one or two bytes is transparent to the MPCC and sent directly to the host without interpretation.

The optional information field consists of 8-bit characters. Cyclic redundancy checking is used for error detection and the CRC remainder resulting from the calculation is transmitted as the frame check sequence field. For BOP, the polynomial $X^{16} + X^{12} + X^5 + 1$ (CRC-CCITT) should be used, i.e., selected in the CRC SEL bits in the ECR. The registers representing the CRC-CCITT polynomial are generally preset to all 1s, and the 1s complement of the resulting remainder is transmitted. (See X.25 Recommendation.)

Zero insertion/deletion is employed to prevent valid frame data from being confused with the special characters. A 0 is inserted by the transmitter after every fifth consecutive 1 in the data stream. These inserted zeros are removed by the receiver to restore the data to its original form. The inserted zeros are not included in the CRC calculation.

The end of the frame is determined by the detection of the closing Flag special character which is the same is the opening Flag.

With the control options offered by the MPCC, commony used bit oriented protocols such as SDLC, HDLC and X.25 standards can be supported. Figure 6 compares the requirements of these options.

BOP Receiver Operation

In BOP, the receiver starts assembling characters and accumulating CRC immediately after the detection of a Flag. The receiver also continues to search for additional Flag, or Abort, characters on a bit-by-bit basis. Zero deletion is implemented in the Receiver Shift Register after the Flag detection logic and before the CRC circuitry. The receiver recognizes the shared flag (the closing flag for one frame serves as the opening flag for the next frame) and the shared zero (the ending 0 of a closing flag serves as the beginning 0 of an opening flag forming the pattern "011111101111110."

Character assembly and CRC accumulation are stopped when a closing Flag or Abort is detected. The CRC accumulation includes all the characters between the opening Flag and the closing Flag. The contents of the CRC register are checked at the close of a frame and the C/PERR bit in the RSR is updated. The FCS and the Flag are not passed on to the RxFIFO.

If the Flag is a closing flag, checks for short frame (no control field) and CRC error conditions are made and the appropriate status is updated. When an Abort (seven 1s) is detected, the remaining frame is discarded and the FA/B bit is set in the RSR. When a link idle (15 or more consecutive 1s) is detected, the RIDLE status bit is set in the RSR. The zeros that have been inserted to distinguish data from special characters are detected and deleted from the data stream before characters are assembled. The MPCC programmed as a secondary station provides automatic address matching of the first byte. If there is no address match, the receiver (secondary station) ignores the remainder of the frame by searching for the Flag. If there is a match, the address bytes are transferred to the RxFIFO as they are assembled.

For the control field, one or two bytes are assembled and passed on to the RxFIFO depending on the state of the extended control field bit.

If the CFCRC bit in the ECR is set to 1, an intermediate CRC check will be made after the address and control field. The Frame Check Sequence is still calculated over the remainder of the frame.

BOP Transmitter Operation

In BOP, the TxFIFO can be preloaded through the TDR while the transmitter is disabled (TEN = 0 in the TCR). When the transmitter is enabled (TEN = 1 in the TCR), the leading FLAG is automatically sent prior to transmitting data from the TxFIFO. The TDRA bit is set to 1 in the TSR as long as TxFIFO is not full. If an underrun occurs, the TUNRN bit in the TSR is set to a 1 and an ABORT (11111111) is transmitted followed by continuous FLAGSs or marks until a new sequence is initiated.

The TLAST bit in the TCR must be set prior to loading the last character of the message to signal the transmitter to append the two-byte Frame Check Sequence (FCS) following the last character. If the transmitter DMA mode is selected (the TDSREN bit set to 1 in the TCR) the TLAST bit is set by the $\overline{\text{DONE}}$ signal from the DMAC.

FLAG 01111110	ADDRESS 1 OR N BYTES	CONTROL 1 OR 2 BYTES	INFORMATION N BYTES (OPTIONAL)	FCS 2 BYTES	FLAG 01111110

Figure 5. Bit Oriented Protocol (BOP) Frame Format

IBM SDLS FRAME FORMAT

FLAG 01111110	ADDRESS 1 BYTE	CONTROL 1 BYTE	INFORMATION N BYTES	FCS 2 BYTES	FLAG 01111110

ADCCP/HDLC FRAME FORMAT

FLAG 01111110	ADDRESS N BYTES	CONTROL 1 OR 2 BYTES	INFORMATION N BYTES	FCS 2 BYTES	FLAG 01111110

Figure 6. Implemented Bit Oriented Protocols

A message may be terminated at any time by setting the TABT bit in the TCR to 1. This causes the transmitter to send an Abort character followed by the remainder of the current frame data in the TxFIFO.

The serial data from the Transmitter Shift Register is continuously monitored for five consecutive 1s, and a 0 is inserted in the data stream each time this condition occurs (excluding Flag and Abort characters).

CRC accumulation begins with the first non-Flag character and includes all subsequent characters. The CRC remainder is transmitted as the FCS following the last data character. If the CTLCRC bit in the ECR is set to 1, an intermediate CRC remainder is appended after the Address and Control field. The final Frame Check Sequence is calculated over the balance of the frame.

BISYNC (BSC)

The structure of messages utilizing the IBM Binary Synchronous Communications (BSC) protocol, commonly called Bisync, is shown in Figure 7. The MPCC can process both transparent and nontransparent messages using either the EBCDIC or the ASCII codes. The CRC-16 polynomial should be selected by setting the appropriate CRCSEL bits in the ECR for both transparent and non-transparent EBCDIC and for transparent ASCII coded messages. VRC/LRC should be selected for non-transparent ASCII coded messages. BSC messages are formatted using defined data-link control characters. Data-link control characters generated and recognized by the MPCC are listed in Table 4.

Table 4. BSC Data-Link Control Characters

ASCII			EBCDIC		
Command	**Byte 1**	**Byte 2**	**Command**	**Byte 1**	**Byte 2**
SYN	16*	—	SYN	32*	—
SOH	01	—	SOH	01	—
STX	02	—	STX	02	—
ETB	17	—	EOB (ETB)	26	—
ETX	03	—	ETX	03	—
ENQ	05	—	ENQ	2D	—
DLE	10	—	DLE	10	—
ITB	1F	—	ITB	1F	—
EOT	04	—	EOT	37	—
ACK N*	10	30-37	ACK 0	10	70
NAK	15	—	ACK 1	10	61
WACK	10	3B	NAK	3D	—
RVI	10	3C	WACK	10	6B
			RVI	10	7C

Note: *Programmable

A heading is a block of data starting with an SOH and containing one or more characters that are used for message control (e.g., message identification, routing, and priority). The SOH initiates the block-check-character (BCC) accumulation, but is not included in the accumulation. The heading is terminated by STX when it is part of a block containing both heading and text. A block containing only a heading is terminated with an ITB or an ETB followed by the BCC. Only the first SOH or STX in a transmission block following a line turnaround causes the BCC to reset. All succeeding STX or SOH characters are included in the BCC. This permits the entire transmission (excluding the first SOH or STX) to be block-checked.

The text data is transmitted in complete units called messages, which are initiated by STX and concluded with ETX. A message can be subdivided into smaller blocks for ease in processing and more efficient error control. Each block starts with STX and ends with ETB (except for the last block of a message, which ends with ETX). A single transmission can contain any number of blocks (ending with ETB) or messages (ending with ETX). An EOT following the last ETX block indicates a normal end of transmission. Message blocking without line turnaround can be accomplished by using ITB (see the Additional Data Link Capabilities section, IBM GA 27-3004-2).

Two modes of data transfers are used in BSC. In non-transparent mode, data link control characters may not appear as text data. In transparent mode, each control character is preceded by a data link escape (DLE) character to differentiate it from the text data. Table 5 indicates which control characters are excluded in the CRC generation. All characters not shown in the table are included in the CRC generation. Figure 8 shows various formats for Control/Response Blocks and Heading and Text Blocks.

Table 5. BSC Control Sequences — Inclusion in CRC Accumulation

	Included in CRC Accumulation	
Character of Sequence	**Yes**	**No**
TSYN	—	DLESYN
TSOH	—	DLESOH
TSTX*	—	DLESTX
TETB	ETB	DLE
TETX	ETX	DLE
TDLE	(DLE)DLE	DLE(DLE)

*If not preceded within the same block by transparent heading information.

LEADING PAD 1 BYTE (AR1)	SYN 1 BYTE (AR2)	SYN 1 BYTE (AR2)	BODY	BCC	TRAILING PAD 11111111

Figure 7. BSC Block Format

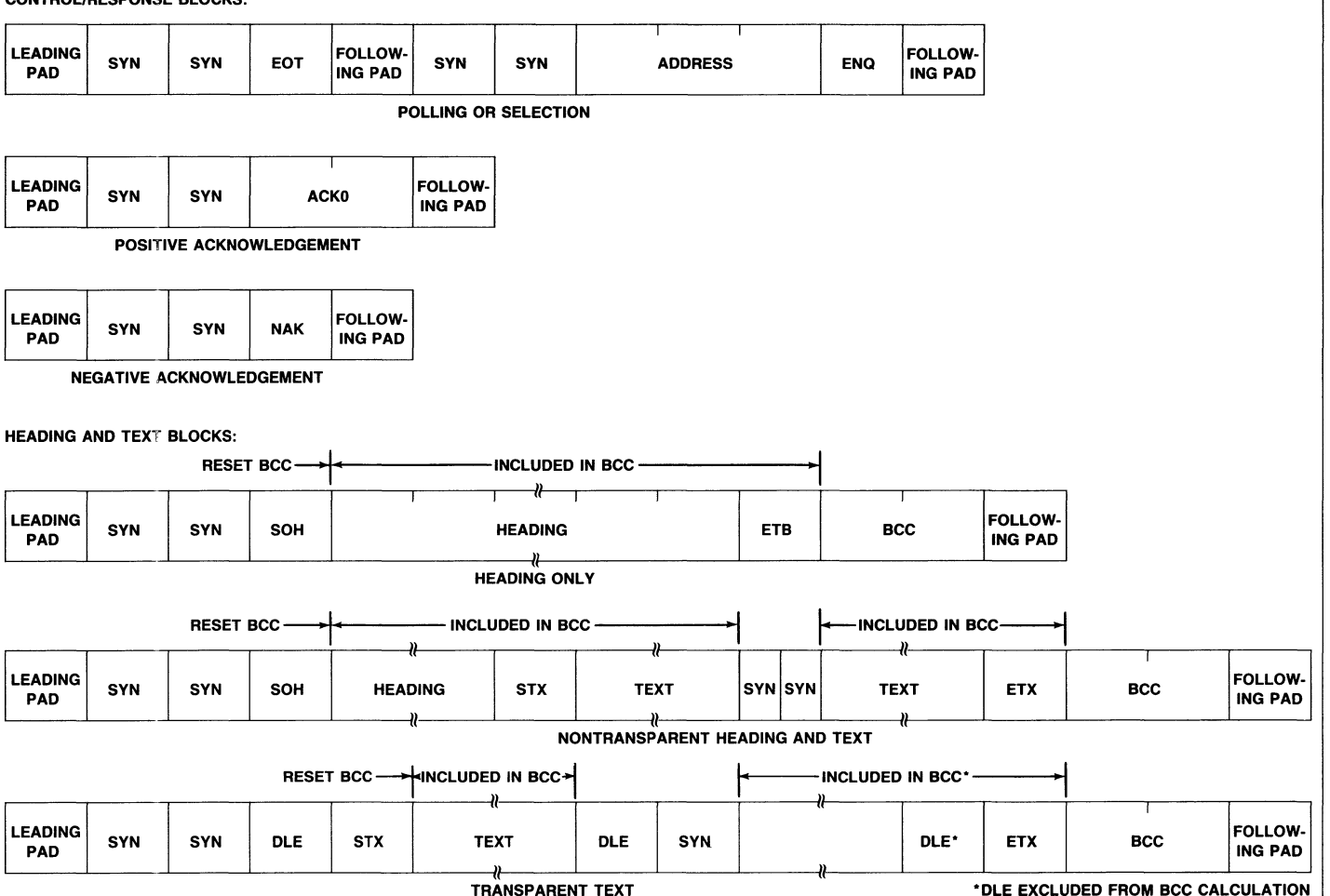


Figure 8. BSC Message Format Examples

BSC Receiver Operation

Character length defaults to eight bits in BSC mode. When ASCII is selected, the eighth bit is used for parity provided that VRC/LRC polynomial is selected. Character assembly starts after the receipt of two consecutive SYN characters. Serial data bits are shifted through the Receiver Shift Register into the Serial-to-Parallel Register and transferred to the RxFIFO. The RDA status bit in the RSR is set to 1 each time data is transferred to the RxFIFO. The SYN character pairs in non-transparent mode and DLE-SYN pairs in transparent mode are discarded.

The receiver starts each block in the non-transparent mode. It switches to transparent mode if a block begins with a DLE-SOH or DLE-STX pair. The receiver remains in transparent mode until a DLE-ITB, DLE-ETB, DLE-ETX or DLE-ENQ pair is received. BCC accumulation begins after an opening SOH, STX, or DLE-STX. SYN characters in non-transparent mode or DLE-SYN pairs in transparent mode are excluded from the BCC accumulation. The first DLE of a DLE-DLE sequence is not included in the BCC accumulation and is discarded. The BCC is checked after receipt of an ITB, ETB, or ETX in non-transparent mode or DLE-ITB, DLE-ETB, DLE-ETX in transparent mode. If a CRC error is detected, the C/PERR and EOF bits in the RSR are set to 1. If no error is detected only the EOF bit is set. If the closing character was an ITB, BCC accumulation and character assembly starts again on the first character following the BCC.

BSC Transmitter Operation

BSC transmission begins with the sending of an opening pad (PAD) and two sync (SYN) characters. These characters are programmable and stored in AR1(PAD) and AR2(SYN). SOH or STX initiates the block-check-character (BCC) accumulation. An initial SOH or STX is not included in the BCC accumulation. Should an underrun condition occur, the content of AR2 (normally SYN character) is transmitted until new characters become available.

The message is terminated by the transmission of the BCC followed by a closing pad when an ETB, ITB, or ETX is fetched from the TxFIFO. The closing PAD is generated by the MPCC.

In transparent mode, the BCC accumulation is initiated by DLE-STX and is terminated by the sequences DLE-ETX, DLE-ETB, or DLE-ITB. See Table 5 for character sequence and inclusion in CRC accumulation. If an underrun occurs, DLE-SYN characters will be transmitted until new characters are available in the TxFIFO. ETC, ETX, ITB, or ENQ with a TLAST tag is treated as a control character and the MPCC automatically inserts a DLE immediately preceding these characters. DLE-ETB, DLE-ETX, DLE-ITB, or DLE-ENQ terminates a block of transparent text, and returns the data link to normal mode. BCC generation is not used for messages beginning with characters other than SOH, STX, DLE-SOH, or DLE-STX. On all message types, if the TSYN bit is set to 1 in the TCR, a SYN-SYN (DLE-SYN sequence on transparent messages) sequence is transmitted before the next character is fetched from the TxFIFO.

CHARACTER ORIENTED PROTOCOLS

The character oriented protocol (COP) option uses the format shown in Figure 9. It may be used for various character oriented protocols with 5-8 bit character sizes and optional parity checking. The input data is checked on a bit-by-bit basis for a pair of consecutive SYN characters to establish character synchronization. These SYN characters are discarded after detection. The PAD and SYN characters may be 5-8 bits long and are user programmable as stored in AR1 and AR2, respectively.

If parity checking is enabled the characters assembled after character sync are checked for parity errors. If STRSYN is set in the RCR, all SYN characters detected within the message will be discarded and will not be passed on to the RxFIFO. If STRSYN is reset, SYNs detected within the message will be treated as data.

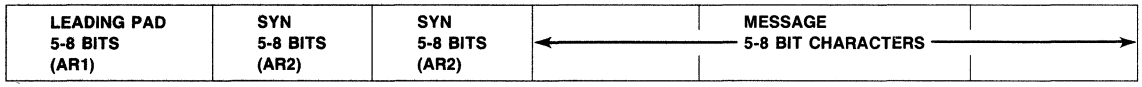


Figure 9. Character Oriented Protocol Format

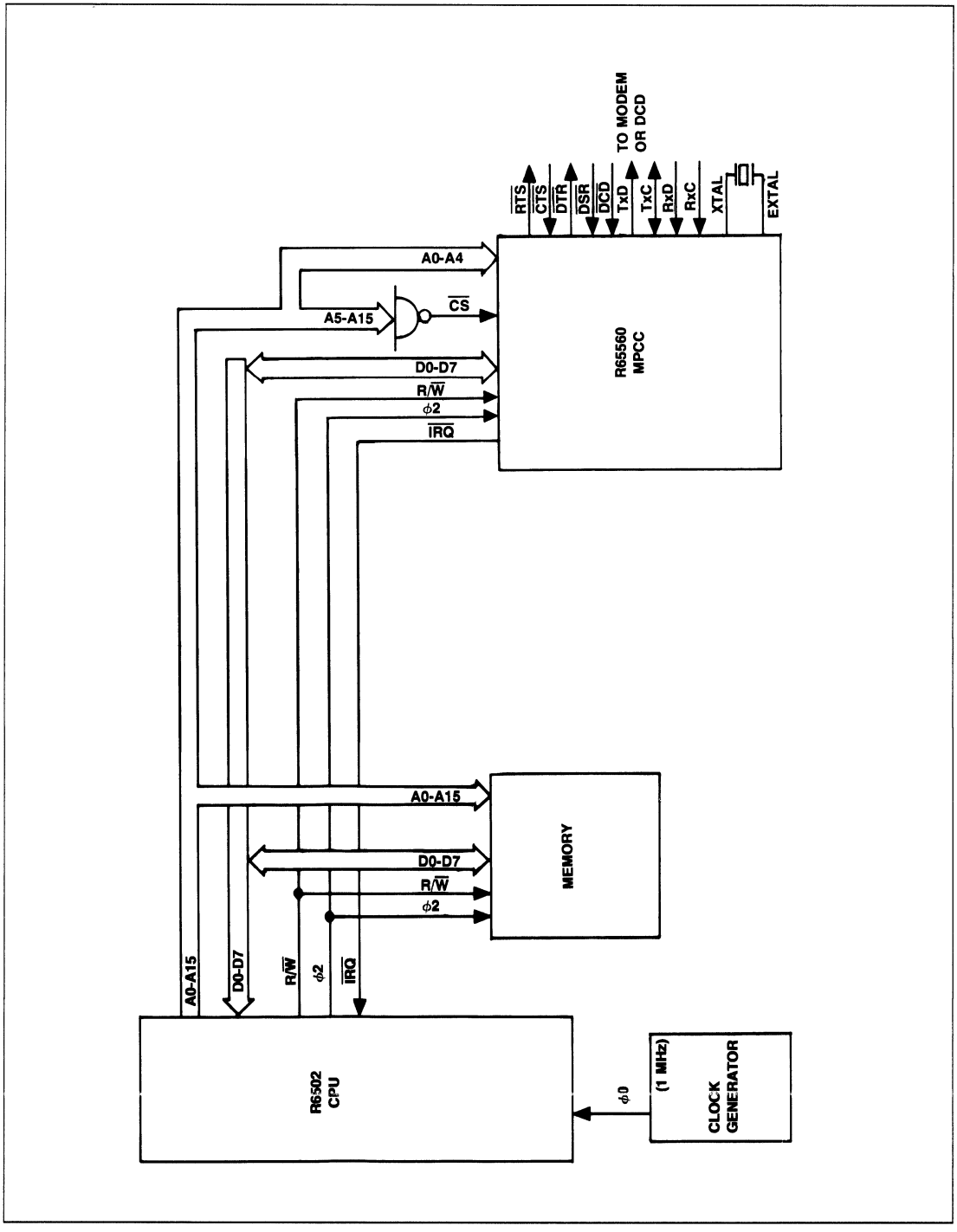


Figure 10. Typical Interface to 6500-Based System

2

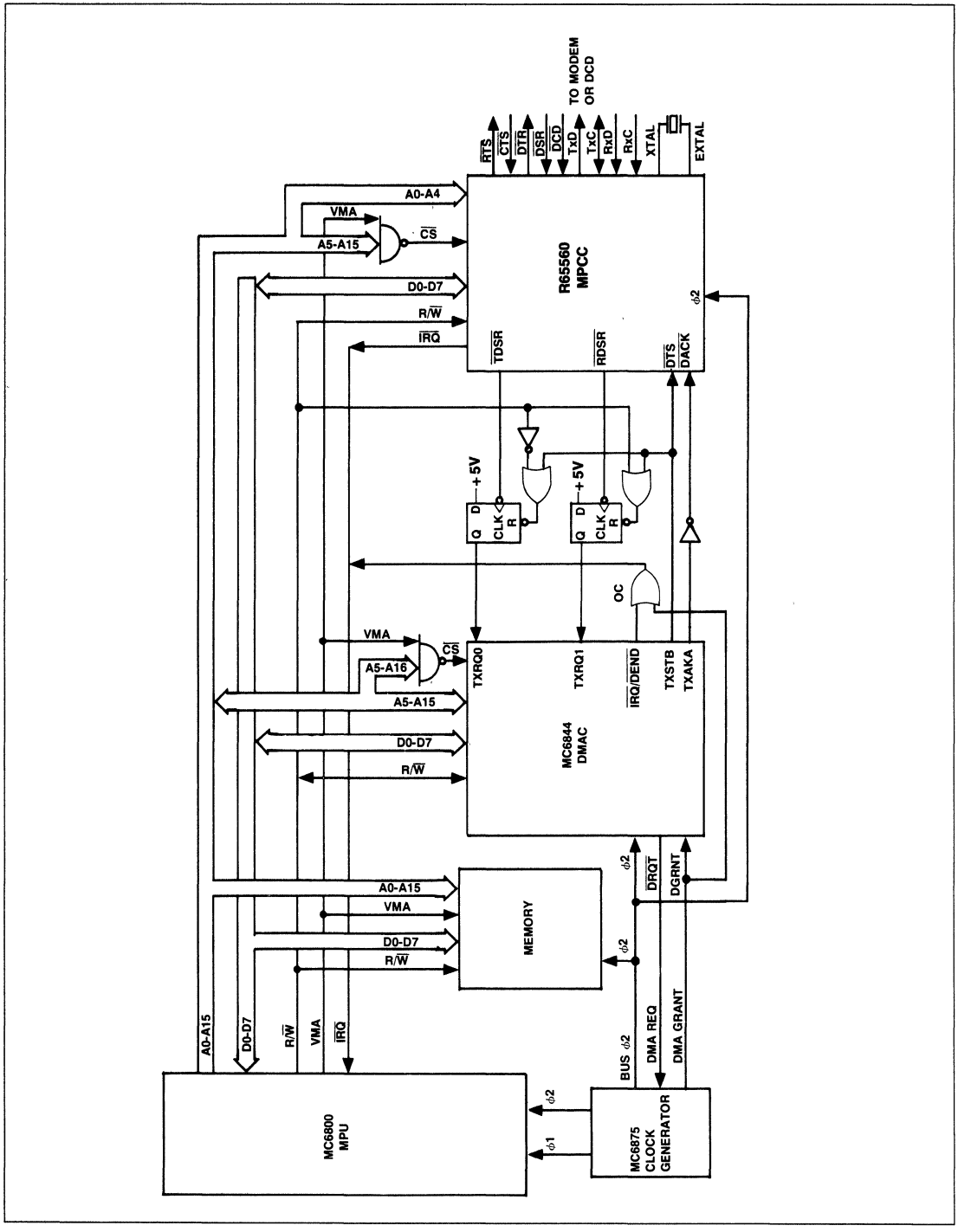
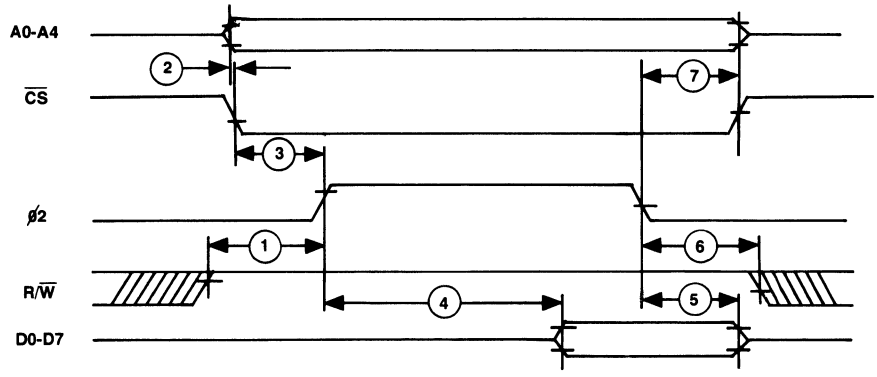
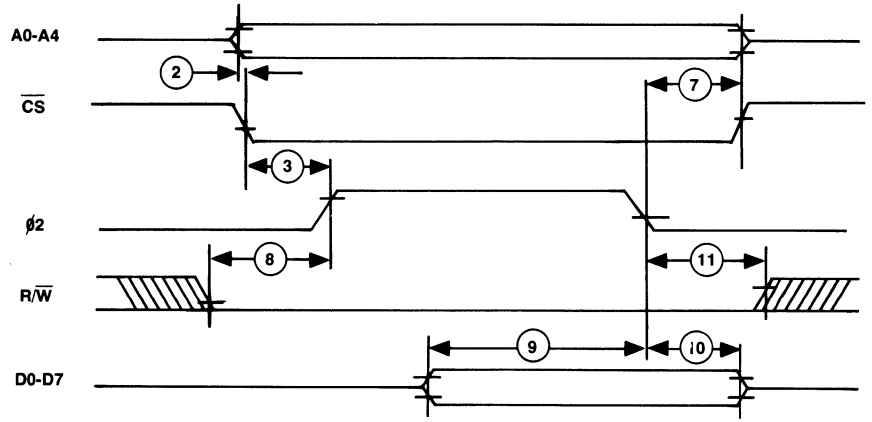


Figure 11. Typical Interface to 6800-Based System



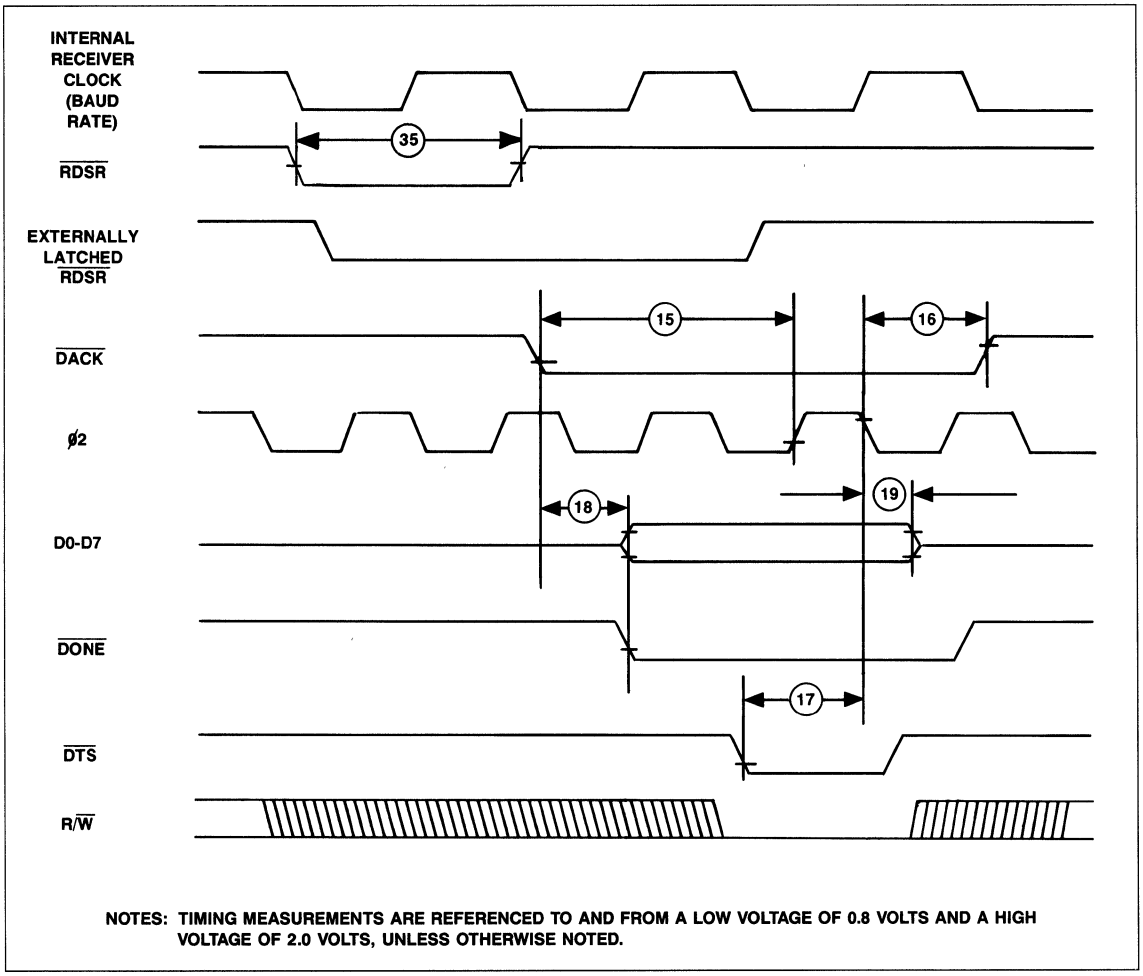
NOTES: TIMING MEASUREMENTS ARE REFERENCED TO AND FROM A LOW VOLTAGE OF 0.8 VOLTS AND A HIGH VOLTAGE OF 2.0 VOLTS, UNLESS OTHERWISE NOTED.

Figure 12. MPCC Read Cycle Timing



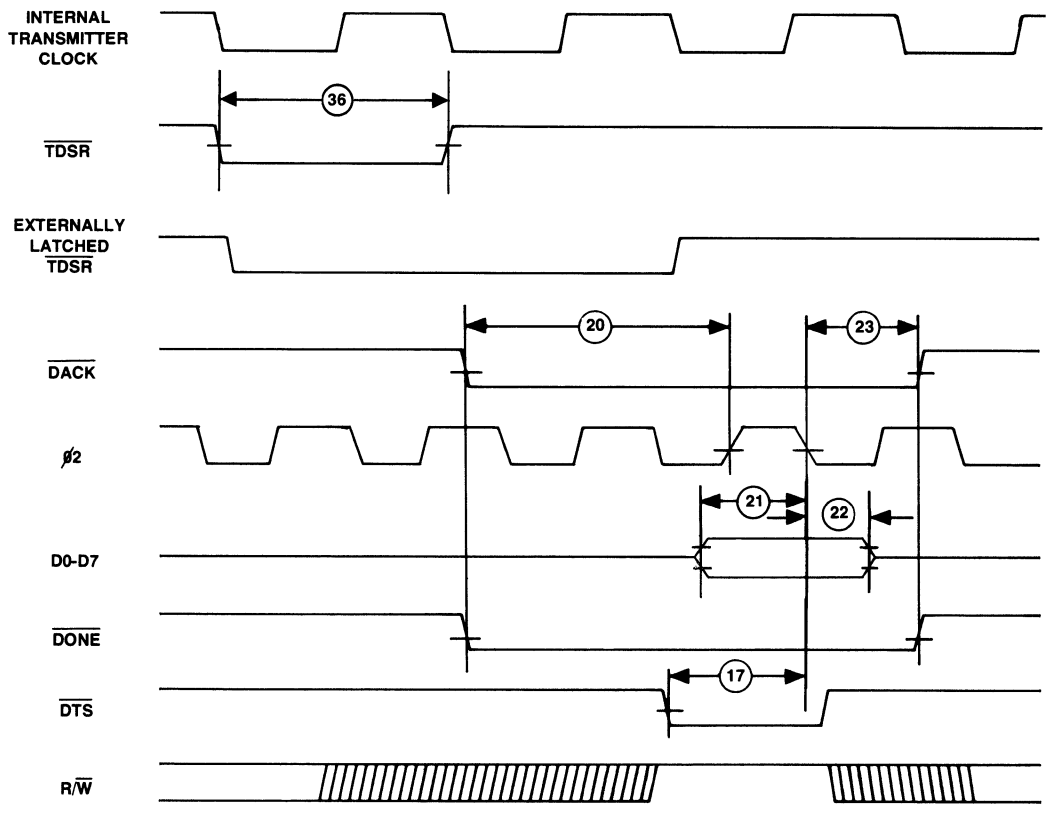
NOTES: TIMING MEASUREMENTS ARE REFERENCED TO AND FROM A LOW VOLTAGE OF 0.8 VOLTS AND A HIGH VOLTAGE OF 2.0 VOLTS, UNLESS OTHERWISE NOTED.

Figure 13. MPCC Write Cycle Timing



NOTES: TIMING MEASUREMENTS ARE REFERENCED TO AND FROM A LOW VOLTAGE OF 0.8 VOLTS AND A HIGH VOLTAGE OF 2.0 VOLTS, UNLESS OTHERWISE NOTED.

Figure 14. MPCC to Memory DMA Transfer Cycle Timing (Receiver DMA Mode).



NOTES: TIMING MEASUREMENTS ARE REFERENCED TO AND FROM A LOW VOLTAGE OF 0.8 VOLTS AND A HIGH VOLTAGE OF 2.0 VOLTS, UNLESS OTHERWISE NOTED.

Figure 15. Memory to MPCC DMA Transfer Cycle Timing (Transmitter DMA Mode).

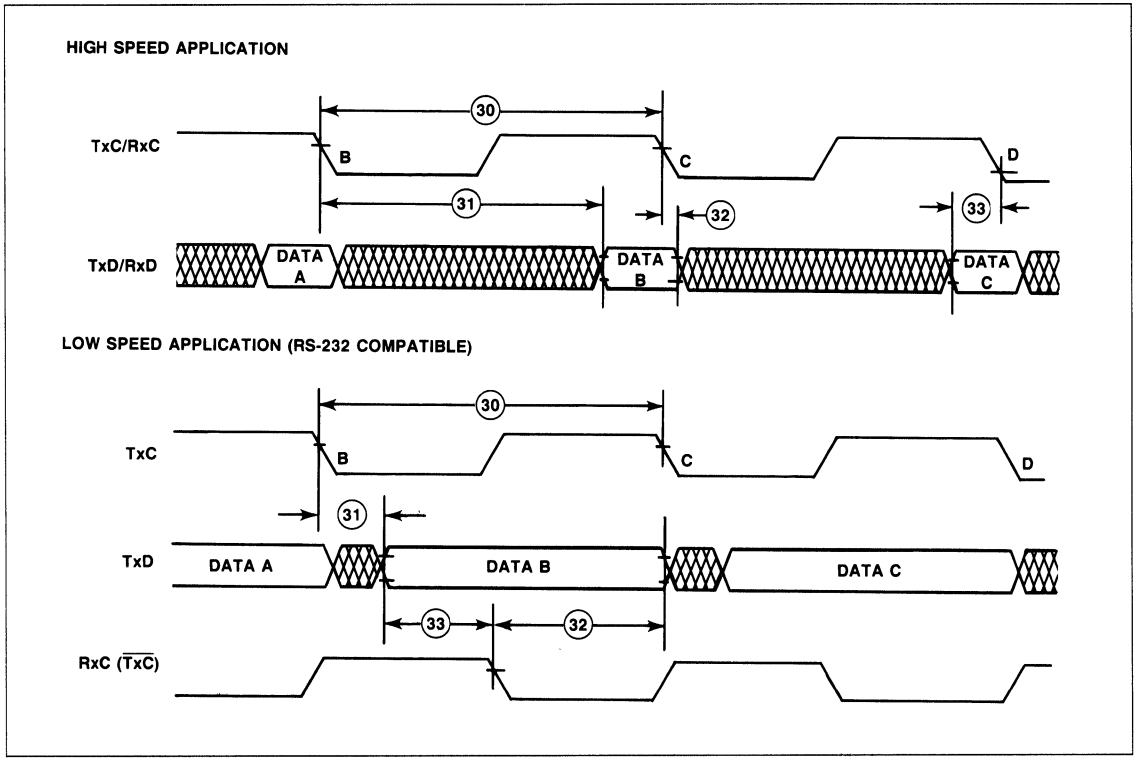
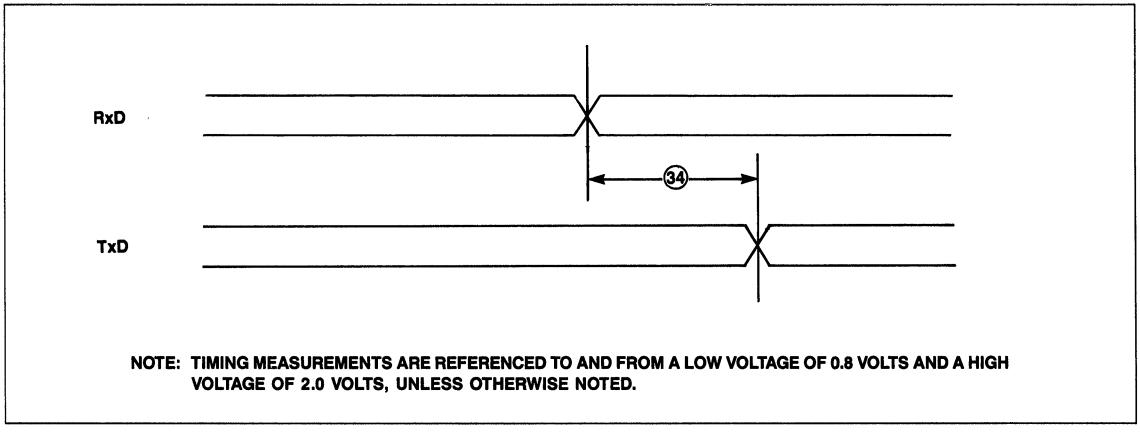


Figure 16. Serial Interface Timing



NOTE: TIMING MEASUREMENTS ARE REFERENCED TO AND FROM A LOW VOLTAGE OF 0.8 VOLTS AND A HIGH VOLTAGE OF 2.0 VOLTS, UNLESS OTHERWISE NOTED.

Figure 17. Serial Interface Echo Mode Timing

AC CHARACTERISTICS

(V_{CC} = 5.0 Vdc ±5%, V_{SS} = 0 Vdc, T_A = 0°C to 70°C)

Number	Parameter	Symbol	Min	Max	Unit
1	R/$\overline{W}$ High to Ø2 High	t_{RH2H}	0	—	ns
2	Address Valid to $\overline{CS}$ Low	t_{AVSL}	30	—	ns
3	$\overline{CS}$ Low to Ø2 High	t_{SL2H}	30	—	ns
4	Ø2 High to Data Valid	t_{2HDV}	0	140	ns
5	Ø2 Low to Data Invalid	t_{2LDXR}	10	150	ns
6	Ø2 Low to R/$\overline{W}$ Low	t_{2LRL}	20	—	ns
7	Ø2 Low to Address Invalid	t_{2LAI}	20	—	ns
8	R/$\overline{W}$ Low to Ø2 High	t_{RL2H}	0	—	ns
9	Data Valid to Ø2 Low	t_{DV2L}	60	—	ns
10	Ø2 Low to Data Invalid	t_{2LDXW}	0	—	ns
11	Ø2 Low to R/$\overline{W}$ High	t_{2LRH}	20	—	ns
15	$\overline{DACK}$ Low to Ø2 High	t_{AL2H}	125	—	ns
16	Ø2 Low to $\overline{DACK}$ High	t_{2LAH}	65	—	ns
17	$\overline{DTS}$ Low to Ø2 Low	t_{SL2L}	60	—	ns
18	$\overline{DACK}$ Low to Data Valid, $\overline{DONE}$ Low	t_{ALDV}	0	140	ns
19	Ø2 Low to Data Invalid	t_{2LDXDR}	10	150	ns
20	$\overline{DACK}$, $\overline{DONE}$ Low to Ø2 High	t_{AL2H}	125	—	ns
21	Data Valid to Ø2 Low	t_{DV2L}	60	—	ns
22	Ø2 Low to Data Invalid	t_{2LDXDW}	0	—	ns
23	Ø2 Low to $\overline{DACK}$, $\overline{DONE}$ High	t_{2LDH}	65	—	ns
30	RxC and TxC Period	t_{CP}	248	—	ns
31	TxC Low to TxD Delay	t_{TCLTD}	0	200	ns
32	RxC Low to RxD Transition (Hold)	t_{RCLRD}	0	—	ns
33	RxD Transition to RxC Low (Setup)	t_{RDRCL}	30	—	ns
34	RxD to TxD Delay (Echo Mode)	t_{RDTD}	—	200	ns
35[1, 2]	$\overline{RDSR}$ Pulse Width	t_{RPW}	1	—	clock period
36[1, 3]	$\overline{TDSR}$ Pulse Width	t_{TPW}	1	—	clock period

Notes:
1. For synchronous protocols, this is one full serial clock period of RxC for $\overline{RDSR}$ and TxC for $\overline{TDSR}$.
2. For asynchronous protocols, $\overline{RDSR}$ is asserted for two system clock periods for a prescale factor of 2 and for three system clock periods for a prescale factor of 3.
3 For asynchronous protocols, $\overline{TDSR}$ is asserted of one-half the baud rate.

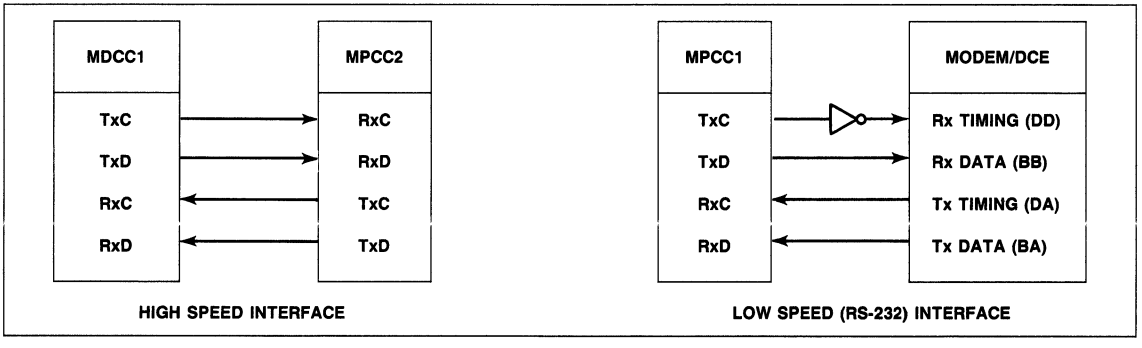


Figure 18. Serial Interface

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to +7.0	V
Input Voltage	V_{IN}	−0.3 to +7 0	V
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{STG}	−55 to +150	°C

***NOTE:** Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in other sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL CHARACTERISTICS

Parameter	Symbol	Value	Rating
Thermal Resistance	θ_{JA}		°C/W
Ceramic		50	
Plastic		68	

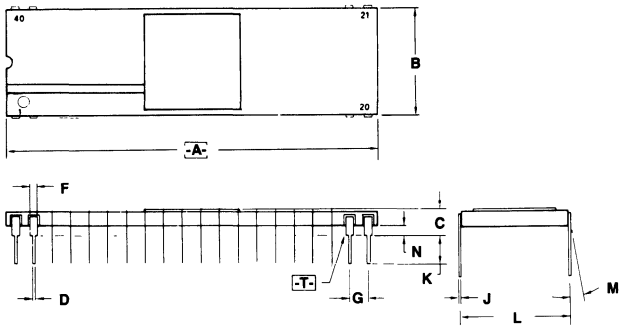
DC CHARACTERISTICS

(V_{CC} = 5.0 Vdc ±5%, V_{SS} = 0 Vdc, T_A = 0°C to 70°C unless otherwise noted)

Parameter	Symbol	Min	Max	Unit	Test Conditions
Input High Voltage All Inputs	V_{IH}	+2 0	V_{CC}	V	
Input Low Voltage All Inputs	V_{IL}	−0.3	+0 8	V	
Input Leakage Current R/$\overline{W}$, $\overline{RES}$, $\overline{CS}$	I_{IN}	—	10.0	μA	V_{IN} = 0 to 5.25V V_{CC} = 5.25V
Three-State (Off State) Input Current $\overline{IRQ}$, D0-D7	T_{TSI}	—	10.0	μA	V_{IN} = 0 4 to 2.4V V_{CC} = 5 25V
Output High Voltage $\overline{RDSR}$, $\overline{TDSR}$, $\overline{IRQ}$, D0-D7, $\overline{DSR}$, $\overline{DTR}$, $\overline{RTS}$, TxD, TxC	V_{OH}	V_{SS} + 2.4	—	V	V_{CC} = 4.75V I_{LOAD} = −400 μA, C_{LOAD} = 130 pF
BCLK	V_{OH}	V_{SS} + 2.4	—	V	V_{CC} = 4 75V I_{LOAD} = 0 C_{LOAD} = 30 pF
Output Low Voltage $\overline{RDSR}$, $\overline{TDSR}$, $\overline{IRQ}$, D0-D7, $\overline{DSR}$, $\overline{DTR}$, $\overline{RTS}$, TxD, TxC, $\overline{BCLK}$	V_{OL}	—	0.5	V	V_{CC} = 4.75V I_{LOAD} = 3.2 mA
$\overline{DONE}$					V_{CC} = 4.75V I_{LOAD} = 8.8 mA
Internal Power Dissipation	P_{INT}	—	1	W	T_A = 25°C
Input Capacitance	C_{IN}	—	13	pF	V_{IN} = 0V T_A = 25°C f = 1 MHz

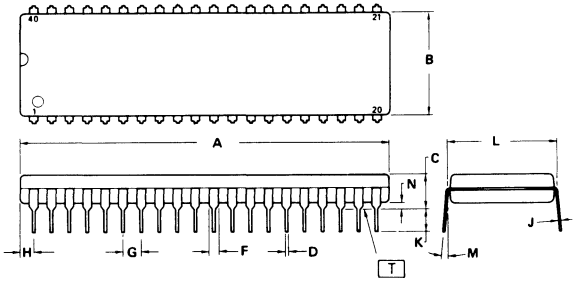
PACKAGE DIMENSIONS

40-PIN CERAMIC DIP



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	50 29	51 56	1 980	2 030
B	14 73	15 49	0 580	0 610
C	1 78	3 05	0 070	0 120
D	0 38	0 58	0 015	0 023
F	1 02	1 65	0 040	0 065
G	2 29	2 80	0 090	0 110
J	0 20	0 38	0 008	0 015
K	3 18	3 81	0 125	0 150
L	14 99	16 51	0 590	0 650
M	0°	10°	0°	10°
N	0 58	1 78	0 020	0 070

40-PIN PLASTIC DIP



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	51 28	52 32	2 040	2 060
B	13 72	14 22	0 540	0 560
C	3 55	5 08	0 140	0 200
D	0 36	0 51	0 014	0 020
F	1 02	1 52	0 040	0 060
G	2 54 BSC		0 100 BSC	
H	1 65	2 16	0 065	0 085
J	0 20	0 30	0 008	0 012
K	3 05	3 56	0 120	0 140
L	15 24 BSC		0 600 BSC	
M	7°	10°	7°	10°
N	0 51	1 02	0 020	0 040

Rockwell

R65C02, R65C102, AND R65C112
R65C00 MICROPROCESSORS (CPU)

DESCRIPTION

The 8-bit R65C00 microprocessor family of devices are produced using CMOS silicon gate technology which provides advanced system architecture for performance speed and system cost-effectiveness enhancements over their NMOS counterparts, the R6500 family of microprocessor devices.

Three CPU devices are available. All are software-compatible and provide 64K bytes of addressable memory, interrupt input, and on-chip clock oscillators and drivers options. All are bus-compatible with the NMOS R6500 family devices.

The CMOS family includes two microprocessors (R65C02 and R65C102) with on-board clock oscillators and drivers and one microprocessor (R65C112) driven by external clocks. The on-chip clock versions are aimed at high performance, low-cost applications where single phase inputs, crystal or RC inputs provide the time base. The slave processor version is geared for multiprocessor system applications where maximum timing control is mandatory. All R65C00 microprocessors are available in ceramic and plastic packaging, operating frequency of 1 MHz, 2 MHz, 3 MHz and 4 MHz, and commercial and industrial temperature versions. All three devices are housed in 40-pin packages.

ENHANCEMENTS OVER R6502

The CMOS family of microprocessor devices has been designed with many enhancements over the R6502 NMOS device while maintaining software compatibility. Besides the increased speed and lower power consumption inherent in CMOS technology, the R65C00 family has added the following characteristics.

- 12 new instructions for a total of 68
- 59 new op codes, for a total of 210
- Two new addressing modes
- Seven software/operational enhancements
- Two hardware enhancements

FEATURES

- CMOS silicon gate technology
- Low Power (4mA/MHz)
- Software compatible with R6502
- Single 5V +5% power supply requirements
- Eight bit parallel processing
- Decimal and binary arithmetic
- True indexing capability
- Programmable stack pointer
- Interrupt capability
- Non-maskable interrupt
- Eight-bit bidirectional data bus
- Addressable memory range of up to 64K bytes
- "Ready" input
- Direct memory access (DMA) capability
- Memory lock output
- 1 MHz, 2 MHz, 3 MHz, and 4 MHz versions
- Choice of external or on-chip clocks
- On-chip clock options
  - —External single clock input
  - —Direct crystal input (÷ 4)
- Commercial and industrial temperature versions
- Pipeline architecture
- Slave processor version (R65C112)

ORDERING INFORMATION

Part Number:

R65C02 _ _ _
R65C102 _ _ _
R65C112 _ _ _

Temp. Range (T_L to T_H)
Blank = 0°C to +70°C
E = −40°C to +85°C

Frequency Range
1 = 1 MHz
2 = 2 MHz
3 = 3 MHz
4 = 4 MHz

Package
C = Ceramic
P = Plastic

FUNCTIONAL DESCRIPTION

With the exception of a crystal oscillator, clock signals, Memory Latch (ML), and Bus Enable (BE) signals, the internal architecture of the three members of the R65C00 CPU of devices is identical. Figure 1 shows the block diagram of the R65C00 CPU internal architecture for all three devices. This block diagram supports the following text that describes the function of each of the device's major elements.

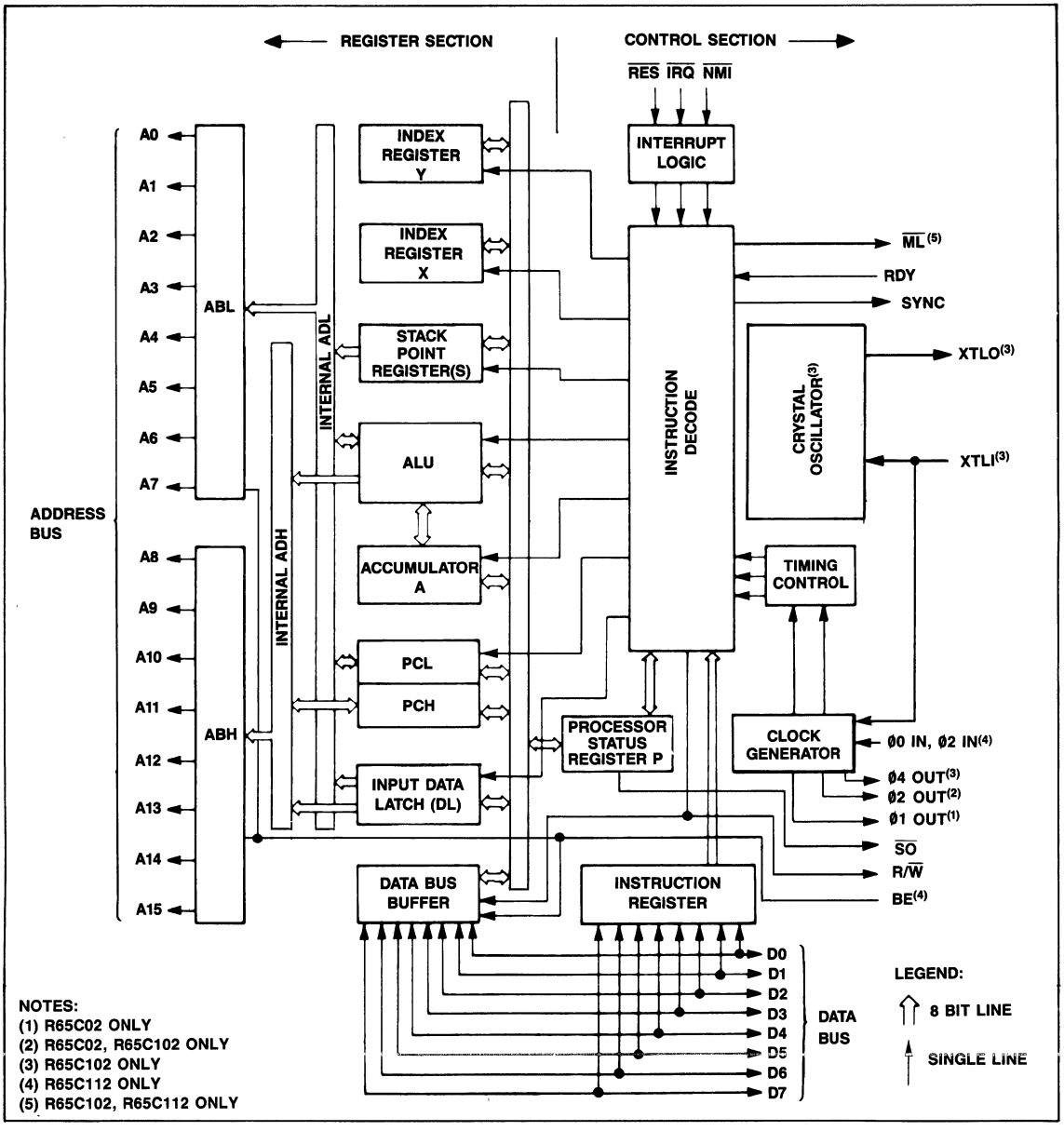


Figure 1. R65C00 Internal Architecture

CRYSTAL OSCILLATOR (R65C102 Only)

The crystal oscillator, driven by a crystal across XTLO and XTAI, divides the crystal frequency by four to provide the basic Ø2 clock signal that drives the internal clock generator.

CLOCK GENERATOR

The clock generator develops all internal clock signals, and (where applicable) external clock signals, associated with the device. It is the clock generator that drives the timing control unit and the external timing for slave mode operations.

TIMING CONTROL

The timing control unit keeps track of the instruction cycle being monitored. The unit is set to zero each time an instruction fetch is executed and is advanced at the beginning of each phase one clock pulse for as many cycles as is required to complete the instruction. Each data transfer which takes place between the registers depends upon decoding the contents of both the instruction register and the timing control unit.

PROGRAM COUNTER

The 16-bit program counter provides the addresses which step the microprocessor through sequential instructions in a program.

Each time the microprocessor fetches an instruction from program memory, the lower byte of the program counter (PCL) is placed on the low-order bits of the address bus and the higher byte of the program counter (PCH) is placed on the high-order 8 bits. The counter is incremented each time an instruction or data is fetched from program memory.

INSTRUCTION REGISTER AND DECODE

Instructions fetched from memory are gated onto the internal data bus. These instructions are latched into the instruction register, then decoded, along with timing and interrupt signals, to generate control signals for the various registers.

ARITHMETIC AND LOGIC UNIT (ALU)

All arithmetic and logic operations take place in the ALU including incrementing and decrementing internal registers (except the program counter). The ALU has no internal memory and is used only to perform logical and transient numerical operations.

ACCUMULATOR

The accumulator is a general purpose 8-bit register that stores the results of most arithmetic and logic operations, and in addition, the accumulator usually contains one of the two data words used in these operations.

INDEX REGISTERS

There are two 8-bit index registers (X and Y), which may be used to count program steps or to provide an index value to be used in generating an effective address.

When executing an instruction which specifies indexed addressing, the CPU fetches the op code and the base address, and modifies the address by adding the index register to it prior to performing the desired operation. Pre- or post-indexing of indirect addresses is possible (see addressing modes).

STACK POINTER

The stack pointer is an 8-bit register used to control the addressing of the variable-length stack on page one. The stack pointer is automatically incremented and decremented under control of the microprocessor to perform stack manipulations under direction of either the program or interrupts ($\overline{NMI}$ and $\overline{IRQ}$). The stack allows simple implementation of nested subroutines and multiple level interrupts. The stack pointer should be initialized before any interrupts or stack operations occur.

PROCESSOR STATUS REGISTER

The 8-bit processor status register contains seven status flags. Some of the flags are controlled by the program, others may be controlled both by the program and the CPU. The R65C00 instruction set contains a number of conditional branch instructions which are designed to allow testing of these flags.

HARDWARE ENHANCEMENTS

The R65C00 family of CPU devices have incorporated hardware enhancements over their NMOS counterpart, the R6502. These hardware enhancements are:

- The NMOS device would ignore the assertion of a Ready (RDY) during a write operation. The CMOS family will stop the processor during Ø2 clock if RDY is asserted during a write operation.
- On the NMOS device, unused input-only pins ($\overline{IRQ}$, $\overline{NMI}$, RDY, $\overline{RES}$, and $\overline{SO}$) must be connected to a low impedance signal to avoid noise problems. These unused pins on the CMOS devices are internally connected by a high impedance to V_{CC} (approximately 250K ohms).

MAJOR FEATURES AND DIFFERENCES

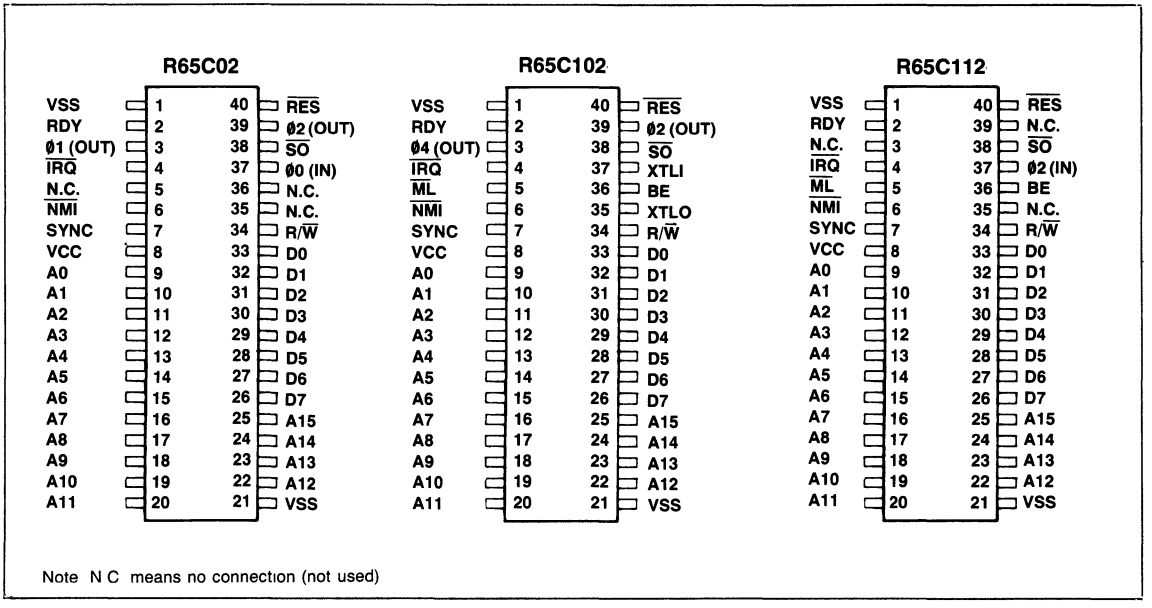
The functional aspects of and differences between the microprocessor configurations are shown in Table 1.

Table 1. Family Comparison Chart

Feature	R65C02	R65C102	R65C112
Pin compatible with NMOS R6502	X		
64K addressable bytes of memory	X	X	X
$\overline{IRQ}$ interrupt	X	X	X
On-chip clock oscillator	X	X	
External clock only			X
TTL level single phase clock input	X	X	
RC time base clock input	X	X	
Crystal time base clock input	X	X	
Single phase clock input			X
Two phase output clock	X	X	
SYNC and RDY signals	X	X	X
Bus Enable ($\overline{BE}$) signal		X	X
Memory Lock ($\overline{ML}$) output signal		X	X
Direct Memory Access (DMA) capacity		X	X
$\overline{NMI}$ interrupt signal	X	X	X

PIN ASSIGNMENTS

Figure 2 shows the pin assignments for the three members of the R65C00 CPU family. All three devices are housed in 40-pin, dual-in-line, ceramic or plastic packages.



Note N C means no connection (not used)

Figure 2. Pin Assignments

SIGNAL DESCRIPTIONS

Reference the timing diagrams (Figures 3, 4 and 5) for the particular device in the following discussion.

CLOCK SIGNALS (R65C02)

The R65C02 requires an external Ø0 clock. See Figure 6 for an example clock circuit. Ø0 is a TTL level input that is used to generate the internal clocks of the R65C02. Two full level output clocks are generated by the R65C02. The Ø2 clock is in phase with Ø0. The Ø1 clock output is 180° out of phase with Ø0. When the input clock is stopped, the CPU is in the standby mode. See Figure 8 for special standby mode considerations.

For non-critical timing configurations, a simple RC or crystal network may be strapped between Ø0 (IN) and Ø1 (OUT).

CLOCK SIGNALS (R65C102)

The R65C102 internal clocks may be generated by a TTL level single phase input, an RC time base input, or a crystal time base input ($\div$ 4) using the XTLO and XTLI input pins. See Figure 7 for an example of a crystal time base circuit. Two full level output clocks are generated by the R65C102. The Ø2 clock output provides timing for external R/$\overline{W}$ operations. Addresses are valid after the address setup time (t_{ADS}) referenced to the falling edge of Ø1 (OUT). The Ø4 output is a quadrature output clock that is delayed from the falling edge of the Ø2 clock by delay time t_{AVS}. Using the Ø4 clock, addresses are valid at the rising edge of Ø4.

CLOCK SIGNALS (R65C112)

All internal clock signals for the R65C112 are generated by the input clock signal Ø2 (IN). Since this device is intended to be operated in the slave mode it does not have internal clock generation, but rather requires the external clock Ø2 (IN) from a host device. Figure 7 shows an example of a clock circuit for the R65C112 configured for slave mode.

ADDRESS BUS (A0-A15)

A0-A15 forms a 16-bit address bus for memory and I/O exchanges on the data bus. The output of each address line is TTL compatible, capable of driving one standard TTL load and 130pF.

DATA BUS (D0-D7)

The data lines (D0-D7) constitute an 8-bit bidirectional data bus used for data exchanges to and from the device and peripherals. The outputs are tri-state buffers capable of driving one TTL load and 130pF.

BUS ENABLE (BE)

This signal allows external control of the data and the address output buffers and R/$\overline{W}$. For normal operation, BE is high causing the address buffers and R/$\overline{W}$ to be active and the data buffers to be active during a write cycle. For external control, BE is held low to disable the buffers. BE is an asynchronous signal and therefore not related to, or controlled by the CPU internal clock signals. Figure 5 shows timing relationships of BE to R/$\overline{W}$ and address output buffers.

INTERRUPT REQUEST ($\overline{IRQ}$)

This TTL compatible input requests that an interrupt sequence begin within the microprocessor. The $\overline{IRQ}$ is sampled during Ø2 operation; if the interrupt flag in the processor status register is zero, the current instruction is completed and the interrupt sequence begins during Ø1. The program counter and processor status register are stored in the stack. The microprocessor will then set the interrupt mask flag high so that no further $\overline{IRQ}$s may occur. At the end of this cycle, the program counter low byte will be loaded from address FFFE, and program counter high byte from location FFFF, thus transferring program control to the memory vector located at these addresses. The RDY signal must be in the high state for any interrupt to be recognized. A 3K ohm external resistor should be used for proper wire OR operation.

MEMORY LOCK ($\overline{ML}$)

In a multiprocessor system, the $\overline{ML}$ output indicates the need to defer the rearbitration of the next bus cycle to ensure the integrity of read-modify-write instructions. $\overline{ML}$ goes low during ASL, DEC, INC, LSR, ROL, ROR, TRB, TSB memory referencing instructions. This signal is low for the modify and write cycles.

NON-MASKABLE INTERRUPT ($\overline{NMI}$)

A negative-going edge on this input requests that a non-maskable interrupt sequence be generated within the microprocessor. The $\overline{NMI}$ is sampled during Ø2; the current instruction is completed and the interrupt sequence begins during Ø1. The program counter is loaded with the interrupt vector from locations FFFA (low byte) and FFFB (high byte), thereby transferring program control to the non-maskable interrupt routine.

NOTE

Since this interrupt is non-maskable, another $\overline{NMI}$ can occur before the first is finished. Care should be taken when using $\overline{NMI}$ to avoid this.

READY (RDY)

This input allows the user to single-cycle the microprocessor on all cycles including write cycles. A negative transition to the low state, during or coincident with Ø1, will halt the microprocessor with the output address lines reflecting the current address being fetched. This condition will remain through a subsequent Ø2 in which the ready signal is low. This feature allows microprocessor interfacing with low-speed memory as well as direct memory access (DMA).

READ/WRITE (R/$\overline{W}$)

This signal is normally in the high state indicating that the microprocessor is reading data from memory or I/O bus. In the low state the data bus has valid data from the microprocessor to be stored at the addressed memory location.

SET OVERFLOW ($\overline{SO}$)

A negative transition on this line sets the overflow bit (V) in the processor status register. The signal is sampled prior to the leading edge of Ø2 by the processor control time (t_{SOS}).

RESET ($\overline{RES}$)

This input resets the microprocessor. Reset must be held low for at least two clock cycles after V_{CC} reaches operating voltage from a power down. A positive transistion on this pin will then cause an initialization sequence to begin. Likewise, after the system has been operating, a low on this line of at least two cycles will cease microprocessing activity, followed by initialization after the positive edge on $\overline{RES}$.

When a positive edge is detected, there is an initialization sequence lasting six clock cycles. Then the interrupt mask flag is set, the decimal mode is cleared, and the program counter is loaded with the restart vector from locations FFFC (low byte) and FFFD (high byte). This is the start location for program control. This input should be high in normal operation.

SYNCHRONIZE (SYNC)

This output line identifies those cycles during which the microprocessor is fetching the instruction operation code (OP CODE). The SYNC line goes high during Ø1 of an OP CODE fetch and stays high for the remainder of that cycle. If the RDY line is pulled low during the Ø1 clock pulse in which SYNC went high, the processor will stop in its current state and will remain in the state until the RDY line goes high. In this manner, the SYNC signal can be used to control RDY to cause single instruction execution.

OPERATIONAL ENHANCEMENTS

Table 2 lists the operational enhancements that have been added to the CMOS family of CPU devices and compares the results with their NMOS R6502 counterpart.

Table 2. CMOS Operational Enhancements

Function	NMOS R6502 Microprocessor	CMOS R65C00 Family Microprocessor
Indexed addressing across page boundary.	Extra read of invalid address.	Extra read of last instruction byte.
Execution of invalid op codes.	Some terminate only by reset. Results are undefined.	All are NOPs (reserved for future use).
Jump indirect, operand = XXFF.	Page address does not increment.	Page address increments and adds one additional cycle.
Read/modify/write instructions at effective address.	One read and two write cycles.	Two read and one write cycle.
Decimal flag.	Indeterminate after reset.	Initialized to binary mode (D=0) after reset and interrupts.
Flags after decimal operation.	Invalid N, V and Z flags.	Valid flag adds one additional cycle.
Interrupt after fetch of BRK instruction.	Interrupt vector is loaded, BRK vector is ignored.	BRK is executed, then interrupt is executed.

ADDRESSING MODES

The R65C00 CPU family has 15 addressing modes (two more than the NMOS equivalent family). In the following discussion of these addressing modes, a bracketed expression follows the title of the mode. This expression is the term used in the Instruction Set Op Code Matrix table (later in this product description) to make it easier to identify the actual addressing mode used by the instruction.

ACCUMULATOR ADDRESSING [Accum]—This form of addressing is represented with a one byte instruction, implying an operation on the accumulator.

IMMEDIATE ADDRESSING [IMM]—In immediate addressing, the second byte of the instruction contains the operand, with no further memory addressing required.

ABSOLUTE ADDRESSING [ABS]—In absolute addressing, the second byte of the instruction specifies the eight low order bits of the effective address while the third byte specifies the eight high order bits. Thus the absolute addressing mode allows access to the entire 64K bytes of addressable memory.

ZERO PAGE ADDRESSING [ZP]—The zero page instructions allow for shorter code and execution times by fetching only the second byte of the instruction and assuming a zero high address byte. Careful use of the zero page can result in significant increase in code efficiency.

ZERO PAGE INDEXED ADDRESSING [ZP, X or Y]—(X, Y indexing)—This form of addressing is used with the index register and is referred to as "Zero Page, X" or "Zero Page, Y". The effective address is calculated by adding the second byte to the contents of the index register. Since this is a form of "Zero Page" addressing, the content of the second byte references a location in page zero. Additionally, due to the "Zero Page" addressing nature of this mode, no carry is added to the high order eight bits of memory and crossing of page boundaries does not occur.

ABSOLUTE INDEXED ADDRESSING [ABS, X or Y]—(X, Y indexing)—This form of addressing is used in conjunction with X and Y index register and is referred to as "Absolute, X" and "Absolute, Y". The effective address is formed by adding the contents of X or Y to the address contained in the second and third bytes of the instruction. This mode allows the index register to contain the index or count value and the instruction to contain the base address. This type of indexing allows any location referencing and the index to modify multiple fields, resulting in reduced coding and execution time.

INDEXED ABSOLUTE INDIRECT [(ABS, X)]*
The contents of the second and third instruction bytes are added to the X-register. The sixteen-bit result is a memory address containing the effective address. (JMP (ABS, X) only).

IMPLIED ADDRESSING [Implied]—In the implied addressing mode, the address containing the operand is implicitly stated in the operation code of the instruction.

RELATIVE ADDRESSING [Relative]—Relative addressing is used only with branch instructions and establishes a destination for the conditional branch.

The second byte of the instruction becomes the operand which is an "Offset" added to the contents of the lower eight bits of the program counter when the counter is set at the next instruction. The range of the offset is −128 to +127 bytes from the next instruction.

ZERO PAGE RELATIVE ADDRESSING [ZP REL]*—This mode bit tests the zero page location specified for bit set/reset per the mask and performs a conditional relative branch based on the results of the bit test.

INDEXED INDIRECT ADDRESSING [(IND, X)]—In indexed indirect addressing (referred to as (Indirect, X)), the second byte of the instruction is added to the contents of the X index register, discarding the carry. The result of this addition points to a memory location on page zero whose contents are the low order eight bits of the effective address. The next memory location in page zero contains the high order eight bits of the effective address. Both memory locations specifying the high and low order bytes of the effective address must be in page zero.

INDIRECT INDEXED ADDRESSING [(IND), Y]—In indirect indexed addressing (referred to as (Indirect), Y), the second byte of the instruction points to a memory location in page zero. The contents of this memory location are added to the contents of the Y index register, the result being the low order eight bits of the effective address. The carry from this addition is added to the contents of the next page zero memory location, the result being the high order eight bits of the effective address.

ABSOLUTE INDIRECT [(ABS)]—The second byte of the instruction contains the low order eight bits of a memory location. The high order eight bits of that memory location are contained in the third byte of the instruction. The contents of the fully specified memory location are the low order byte of the effective address. The next memory location contains the high order byte of the effective address which is loaded into the sixteen bits of the program counter. (JMP (ABS) only.)

INDIRECT [(IND)]*—The second byte of the instruction contains a zero page address serving as the indirect pointer.

NOTE

*These addressing modes are not available to the NMOS CPU family (e.g., the R6502).

INSTRUCTION SET

Table 3 lists the instruction set for the CMOS CPU family in alphabetic order according to mnemonic. Table 4 lists the hexadecimal codes for each of the instructions that are new to the CMOS family and were not available in the NMOS R6502 device family. Table 5 lists those instructions that were available on the NMOS family, but have been assigned new addressing modes in the CMOS CPU family.

Table 3. Alphabetic Listing of Instruction Set

Mnemonic	Function	Mnemonic	Function
(2) ADC	Add Memory to Accumulator with Carry	NOP	No Operation
(2) AND	"AND" Memory with Accumulator		
ASL	Shift Left One Bit (Memory or Accumulator)	(2) ORA	"OR" Memory with Accumlator
(1) BBR	Branch on Bit Reset	PHA	Push Accumulator on Stack
(1) BBS	Branch on Bit Set	PHP	Push Processor Status on Stack
BCC	Branch on Carry Clear	(1) PHX	Push X Register on Stack
BCS	Branch on Carry Set	(1) PHY	Push Y Register on Stack
BEQ	Branch on Result Zero	PLA	Pull Accumulator from Stack
(2) BIT	Test Bits in Memory with Accumulator	PLP	Pull Processor Status from Stack
BMI	Branch on Result Minus	(1) PLX	Pull X Register from Stack
BNE	Branch on Result not Zero	(1) PLY	Pull Y Register from Stack
BPL	Branch on Result Plus		
(1) BRA	Branch Always	(1) RMB	Reset Memory Bit
BRK	Force Break	ROL	Rotate One Bit Left (Memory or Accumulator)
BVC	Branch on Overflow Clear	ROR	Rotate One Bit Right (Memory or Accumulator)
BVS	Branch on Overflow Set	RTI	Return from Interrupt
		RTS	Return from Subroutine
CLC	Clear Carry Flag		
CLD	Clear Decimal Mode	SBC	Subtract Memory from Accumulator with Borrow
CLI	Clear Interrupt Disable Bit	SEC	Set Carry Flag
CLV	Clear Overflow Flag	SED	Set Decimal Mode
(2) CMP	Compare Memory and Accumulator	SEI	Set Interrupt Disable Status
CPX	Compare Memory and Index X	(1) SMB	Set Memory Bit
CPY	Compare Memory and Index Y	(2) STA	Store Accumulator in Memory
		STX	Store Index X in Memory
(2) DEC	Decrement Memory by One	STY	Store Index Y in Memory
DEX	Decrement Index X by One	(1) STZ	Store Zero
DEY	Decrement Index Y by One		
		TAX	Transfer Accumulator to Index X
(2) EOR	"Exclusive-OR" Memory with Accumulator	TAY	Transfer Accumulator to Index Y
		(1) TRB	Test and Reset Bits
(2) INC	Increment Memory by One	(1) TSB	Test and Set Bits
INX	Increment Index X by One	TSX	Transfer Stack Pointer to Index X
INY	Increment Index Y by One	TXA	Transfer Index X to Accumulator
		TXS	Transfer Index X to Stack Register
(2) JMP	Jump to New Location	TYA	Transfer Index Y to Accumulator
JSR	Jump to New Location Saving Return Address		
(2) LDA	Load Accumulator with Memory		
LDX	Load Index X with Memory		
LDY	Load Index Y with Memory		
LSR	Shift One Bit Right (Memory or Accumulator)		

Notes:
(1) Instruction not available on the NMOS family.
(2) R6502 instruction with additional addressing mode(s).

Table 4. Hexadecimal Codes For New Instructions in The CMOS Family

Hex	Mnemonic	Description
80	BRA	Branch relative always [Relative]
3A	DEC	Decrement accumulator [Accum]
1A	INC	Increment accumulator [Accum]
DA	PHX	Push X on stack [Implied]
5A	PHY	Push Y on stack [Implied]
FA	PLX	Pull X from stack [Implied]
7A	PLY	Pull Y from stack [Implied]
9C	STZ	Store zero [Absolute]
9E	STZ	Store zero [ABS, X]
64	STZ	Store zero [ZP]
74	STZ	Store zero [ZP, X]
1C	TRB	Test and reset memory bits with accumulator [ABS]
14	TRB	Test and reset memory bits with accumulator [ZP]
0C	TSB	Test and set memory bits with accumulator [ABS]
04	TSB	Test and set memory bits with accumulator [ZP]
89	BIT	Test Immediate with accumulator [IMM]
0F-7F(1)	BBR	Branch on bit reset [Bit Manipulation, ZP, REL]
8F-FF(1)	BBS	Branch on bit set [Bit Manipulation, ZP, REL]
07-77(1)	RMB	Reset memory bit [Bit Manipulation, ZP]
87-F7(1)	SMB	Set memory bit [Bit Manipulation, ZP]

Note:
1. Most significant digit change only.

Table 5. Hexadecimal Codes For Instructions With New CMOS Addressing Modes

Hex	Mnemonic	Description
72	ADC	Add memory to accumulator with carry [(IND)]
32	AND	AND memory with accumulator [(IND)]
3C	BIT	Test memory bits with accumulator [ABS, X]
34	BIT	Test memory bits with accumulator [ZP, X]
D2	CMP	Compare memory and accumulator [(IND)]
52	EOR	Exclusive Or memory with accumulator [(IND)]
7C	JMP	Jump (New addressing mode) [(ABS, X)]
B2	LDA	Load accumulator with memory [(IND)]
12	ORA	OR memory with accumulator [(IND)]
F2	SBC	Subtract Memory from accumulator with borrow [(IND)]
92	STA	Store accumulator in memory [(IND)]

INSTRUCTION SET OP CODE MATRIX

The following matrix shows the 210 Op Codes associated with the R65C00 family of CPU devices. The matrix identifies the hexadecimal code, the mnemonic code, the addressing mode, the number of instruction bytes, and the number of machine cycles associated with each Op Code. Also, refer to the instruction set summary for additional information on these Op Codes.

MSD \ LSD	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	MSD
0	BRK Implied 1 7	ORA (IND, X) 2 6			TSB ZP 2 5	ORA ZP 2 3	ASL ZP 2 5	RMB0 ZP 2 5	PHP Implied 1 3	ORA IMM 2 2	ASL Accum 1 2		TSB ABS 3 6	ORA ABS 3 4	ASL ABS 3 6	BBR0 ZP 3 5**	0
1	BPL Relative 2 2**	ORA (IND), Y 2 5*	ORA (IND) 2 5		TRB ZP 2 5	ORA ZP, X 2 4	ASL ZP, X 2 6	RMB1 ZP 2 5	CLC Implied 1 2	ORA ABS, Y 3 4*	INC Accum 1 2		TRB ABS 3 6	ORA ABS, X 3 4*	ASL ABS, X 3 7	BBR1 ZP 3 5**	1
2	JSR ABS 3 6	AND (IND, X) 2 6			BIT ZP 2 3	AND ZP 2 3	ROL ZP 2 5	RMB2 ZP 2 5	PLP Implied 1 4	AND IMM 2 2	ROL Accum 1 2		BIT ABS 3 4	AND ABS 3 4	ROL ABS 3 6	BBR2 ZP 3 5**	2
3	BMI Relative 2 2**	AND (IND), Y 2 5*	AND (IND) 2 5		BIT ZP, X 2 4	AND ZP, X 2 4	ROL ZP, X 2 6	RMB3 ZP 2 5	SEC Implied 1 2	AND ABS, Y 3 4*	DEC Accum 1 2		BIT ABS, X 3 4*	AND ABS, X 3 4*	ROL ABS, X 3 7	BBR3 ZP 3 5**	3
4	RTI Implied 1 6	EOR (IND, X) 2 6				EOR ZP 2 3	LSR ZP 2 5	RMB4 ZP 2 5	PHA Implied 1 3	EOR IMM 2 2	LSR Accum 1 2		JMP ABS 3 3	EOR ABS 3 4	LSR ABS 3 6	BBR4 ZP 3 5**	4
5	BVC Relative 2 2**	EOR (IND), Y 2 5*	EOR (IND) 2 5			EOR ZP, X 2 4	LSR ZP, X 2 6	RMB5 ZP 2 5	CLI Implied 1 2	EOR ABS, Y 3 4*	PHY Implied 1 3			EOR ABS, X 3 4*	LSR ABS, X 3 7	BBR5 ZP 3 5**	5
6	RTS Implied 1 6	ADC (IND, X) 2 6†			STZ ZP 2 3	ADC ZP 2 3†	ROR ZP 2 5	RMB6 ZP 2 5	PLA Implied 1 4	ADC IMM 2 2†	ROR Accum 1 2		JMP (ABS) 3 6	ADC ABS 3 4†	ROR ABS 3 6	BBR6 ZP 3 5**	6
7	BVS Relative 2 2**	ADC (IND), Y 2 5*†	ADC (IND) 2 5†		STZ ZP, X 2 4	ADC ZP, X 2 4†	ROR ZP, X 2 6	RMB7 ZP 2 5	SEI Implied 1 2	ADC ABS, Y 3 4*†	PLY Implied 1 4		JMP (ABS, X) 3 6	ADC ABS, X 3 4*†	ROR ABS, X 3 7	BBR7 ZP 3 5**	7
8	BRA Relative 2 3*	STA (IND, X) 2 6			STY ZP 2 3	STA ZP 2 3	STX ZP 2 3	SMB0 ZP 2 5	DEY Implied 1 2	BIT IMM 2 2	TXA Implied 1 2		STY ABS 3 4	STA ABS 3 4	STX ABS 3 4	BBS0 ZP 3 5**	8
9	BCC Relative 2 2**	STA (IND), Y 2 6	STA (IND) 2 5		STY ZP, X 2 4	STA ZP, X 2 4	STX ZP, Y 2 4	SMB1 ZP 2 5	TYA Implied 1 2	STA ABS, Y 3 5	TXS Implied 1 2		STZ ABS 3 4	STA ABS, X 3 5	STZ ABS, X 3 5	BBS1 ZP 3 5**	9
A	LDY IMM 2 2	LDA (IND, X) 2 6	LDX IMM 2 2		LDY ZP 2 3	LDA ZP 2 3	LDX ZP 2 3	SMB2 ZP 2 5	TAY Implied 1 2	LDA IMM 2 2	TAX Implied 1 2		LDY ABS 3 4	LDA ABS 3 4	LDX ABS 3 4	BBS2 ZP 3 5**	A
B	BCS Relative 2 2**	LDA (IND), Y 2 5*	LDA (IND) 2 5		LDY ZP, X 2 4	LDA ZP, X 2 4	LDX ZP, Y 2 4	SMB3 ZP 2 5	CLV Implied 1 2	LDA ABS, Y 3 4*	TSX Implied 1 2		LDY ABS, X 3 4*	LDA ABS, X 3 4*	LDX ABS, Y 3 4*	BBS3 ZP 3 5**	B
C	CPY IMM 2 2	CMP (IND, X) 2 6			CPY ZP 2 3	CMP ZP 2 3	DEC ZP 2 5	SMB4 ZP 2 5	INY Implied 1 2	CMP IMM 2 2	DEX Implied 1 2		CPY ABS 3 4	CMP ABS 3 4	DEC ABS 3 6	BBS4 ZP 3 5**	C
D	BNE Relative 2 2**	CMP (IND), Y 2 5*	CMP (IND) 2 5			CMP ZP, X 2 4	DEC ZP, X 2 6	SMB5 ZP 2 5	CLD Implied 1 2	CMP ABS, Y 3 4*	PHX Implied 1 3			CMP ABS, X 3 4*	DEC ABS, X 3 7	BBS5 ZP 3 5**	D
E	CPX IMM 2 2	SBC (IND, X) 2 6†			CPX ZP 2 3	SBC ZP 2 3†	INC ZP 2 5	SMB6 ZP 2 5	INX Implied 1 2	SBC IMM 2 2†	NOP Implied 1 2		CPX ABS 3 4	SBC ABS 3 4†	INC ABS 3 6	BBS6 ZP 3 5**	E
F	BEQ Relative 2 2**	SBC (IND), Y 2 5*†	SBC (IND) 2 5†			SBC ZP, X 2 4†	INC ZP, X 2 6	SMB7 ZP 2 5	SED Implied 1 2	SBC ABS, Y 3 4*†	PLX Implied 1 4			SBC ABS, X 3 4*†	INC ABS, X 3 7	BBS7 ZP 3 5**	F
	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	

— New Opcode

0
0 BRK Implied 1 7
—OP Code
—Addressing Mode
—Instruction Bytes, Machine Cycles

†Add 1 to N if in decimal mode.
*Add 1 to N if page boundary is crossed.
**Add 1 to N if branch occurs to same page,
Add 2 to N if branch occurs to different page.

MNEMONIC	OPERATION	ADDRESSING MODES: IMMEDIATE OP	n	#	ABSOLUTE OP	n	#	ZERO PAGE OP	n	#	ZP REL OP	n	#	ACCUM OP	n	#	IMPLIED OP	n	#	(IND, X) OP	n	#	(IND), Y OP	n	#	Z PAGE, X OP	n	#	ABS, X OP	n	#	(ABS, X) OP	n	#	ABS, Y OP	n	#	RELATIVE OP	n	#	(IND) OP	n	#	Z. PAGE, Y OP	n	#	PROCESSOR STATUS CODES 7	6	5	4	3	2	1	0
																																												N	V	.	B	D	I	Z	C
ADC	A + M + C → A (1) (5) (7)	69	2	2	6D	4	3	65	3	2										61	6	2	71	5	2	75	4	2	7D	4	3				79	4	3				72	5	2				N	V	.	.	.	.	Z	C
AND	A M → A (1)	29	2	2	2D	4	3	25	3	2										21	6	2	31	5	2	35	4	2	3D	4	3				39	4	3				32	5	2				N	.	.	.	.	.	Z	.
ASL	C ← [7 ... Ø] ← Ø				ØE	6	3	Ø6	5	2				ØA	2	1										16	6	2	1E	7	3													N	.	.	.	.	.	Z	C
BBR [#(Ø-7)]	Branch on M_0 = Ø										ØF-7F	5	3																																	.	.	.	.	.	.	.	.
BBS [#(Ø-7)]	Branch on M_0 = 1										8F-FF	5	3																																	.	.	.	.	.	.	.	.
BCC	Branch on C = Ø (2)																																					9Ø	2	2							.	.	.	.	.	.	.	.
BCS	Branch on C = 1 (2)																																					BØ	2	2							.	.	.	.	.	.	.	.
BEQ	Branch on Z = 1 (2)																																					FØ	2	2							.	.	.	.	.	.	.	.
BIT	A > M (6)	89	2	2	2C	4	3	24	3	2																34	4	2	3C	4	3														M	M_6	.	.	.	.	Z	.
BMI	Branch on N = 1 (2)																																					3Ø	2	2							.	.	.	.	.	.	.	.
BNE	Branch on Z = Ø (2)																																					DØ	2	2							.	.	.	.	.	.	.	.
BPL	Branch on N = Ø (2)																																					1Ø	2	2							.	.	.	.	.	.	.	.
BRA	Branch Always (2)																																					8Ø	3	2							.	.	.	.	.	.	.	.
BRK	Break																ØØ	7	1																											.	.	.	1	.	1	.	.
BVC	Branch on V = Ø (2)																																					5Ø	2	2							.	.	.	.	.	.	.	.
BVS	Branch on V = 1 (2)																																					7Ø	2	2							.	.	.	.	.	.	.	.
CLC	Ø → C																18	2	1																											.	.	.	.	.	.	.	Ø
CLD	Ø → D																D8	2	1																											.	.	.	.	Ø	.	.	.
CLI	Ø → I																58	2	1																											.	.	.	Ø	.	.	.	.
CLV	Ø → V																B8	2	1																											.	Ø	.	.	.	.	.	.
CMP	A − M (1)	C9	2	2	CD	4	3	C5	3	2										C1	6	2	D1	5	2	D5	4	2	DD	4	3				D9	4	3				D2	5	2				N	.	.	.	.	.	Z	C
CPX	X − M	E0	2	2	EC	4	3	E4	3	2																																					N	.	.	.	.	.	Z	C
CPY	Y − M	C0	2	2	CC	4	3	C4	3	2																																					N	.	.	.	.	.	Z	C
DEC	M − 1 → M or A − 1 → A				CE	6	3	C6	5	2				3A	2	1										D6	6	2	DE	7	3														N	.	.	.	.	.	Z	.
DEX	X − 1 → X																CA	2	1																											N	.	.	.	.	.	Z	.
DEY	Y − 1 → Y																88	2	1																											N	.	.	.	.	.	Z	.
EOR	A ⊻ M → A	49	2	2	4D	4	3	45	3	2										41	6	2	51	5	2	55	4	2	5D	4	3				59	4	3				52	5	2				N	.	.	.	.	.	Z	.
INC	M + 1 − M or A + 1 → A				EE	6	3	E6	5	2				1A	2	1										F6	6	2	FE	7	3														N	.	.	.	.	.	Z	.
INX	X + 1 → X																E8	2	1																											N	.	.	.	.	.	Z	.
INY	Y + 1 → Y																C8	2	1																											N	.	.	.	.	.	Z	.
JMP	Jump to New Loc (8)				4C	3	3																									7C	6	3													.	.	.	.	.	.	.	.
JSR	Jump Sub				2Ø	6	3																																								.	.	.	.	.	.	.	.
LDA	M → A (1)	A9	2	2	AD	4	3	A5	3	2										A1	6	2	B1	5	2	B5	4	2	BD	4	3				B9	4	3				B2	5	2				N	.	.	.	.	.	Z	.
LDX	M → X (1)	A2	2	2	AE	4	3	A6	3	2																												BE	4	3							B6	4	2	N	.	.	.	.	.	Z	.
LDY	M → Y (1)	A0	2	2	AC	4	3	A4	3	2																B4	4	2	BC	4	3																			N	.	.	.	.	.	Z	.
LSR	Ø → [7 ... Ø] → C				4E	6	3	46	5	2				4A	2	1									56	6	2	5E	7	3																			Ø	.	.	.	.	.	Z	C
NOP	No Operation																EA	2	1																											.	.	.	.	.	.	.	.
ORA	A ∨ M → A (1)	Ø9	2	2	ØD	4	3	Ø5	3	2										Ø1	6	2	11	5	2	15	4	2	1D	4	3				19	4	3				12	5	2				N	.	.	.	.	.	Z	.
PHA	A → Ms S − 1 → S																48	3	1																											.	.	.	.	.	.	.	.
PHP	P → Ms S − 1 → S																Ø8	3	1																											.	.	.	.	.	.	.	.
PHX	X → Ms S − 1 → S																DA	3	1																											.	.	.	.	.	.	.	.
PHY	Y → Ms S − 1 → S																5A	3	1																											.	.	.	.	.	.	.	.
PLA	S + 1 → S Ms → A																68	4	1																											N	.	.	.	.	.	Z	.
PLP	S + 1 → S Ms → P																28	4	1																											(Restored)							
PLX	S + 1 → S Ms → X																FA	4	1																											N	.	.	.	.	.	Z	.
PLY	S + 1 → S Ms → Y																7A	4	1																											N	.	.	.	.	.	Z	.
RMB [#(Ø-7)]	Ø → M_0 (4)							Ø7-77	5	2																																					.	.	.	.	.	.	.	.
ROL	[7 ... Ø] ← C				2E	6	3	26	5	2				2A	2	1									36	6	2	3E	7	3																			N	.	.	.	.	.	Z	C
ROR	C → [7 ... Ø]				6E	6	3	66	5	2				6A	2	1									76	6	2	7E	7	3																			N	.	.	.	.	.	Z	C
RTI	Rtrn Int																4Ø	6	1																											(Restored)							
RTS	Rtrn Sub																6Ø	6	1																											.	.	.	.	.	.	.	.
SBC	A − M − $\overline{C}$ → A (1) (3) (5)	E9	2	2	ED	4	3	E5	3	2										E1	6	2	F1	5	2	F5	4	2	FD	4	3				F9	4	3				F2	5	2				N	V	.	.	.	.	Z	$\overline{C}$
SEC	1 → C																38	2	1																											.	.	.	.	.	.	.	1
SED	1 → D																F8	2	1																											.	.	.	.	1	.	.	.
SEI	1 → I																78	2	1																											.	.	.	.	.	1	.	.
SMB [#(Ø-7)]	1 → M_0 (4)							Ø7-F7	5	2																																					.	.	.	.	.	.	.	.
STA	A → M				8D	4	3	85	3	2										81	6	2	91	6	2	95	4	2	9D	5	3				99	5	3				92	5	2				.	.	.	.	.	.	.	.
STX	X → M				8E	4	3	86	3	2																96	4	2																			.	.	.	.	.	.	.	.
STY	Y → M				8C	4	3	84	3	2																94	4	2																			.	.	.	.	.	.	.	.
STZ	Ø → M				9C	4	3	64	3	2																74	4	2	9E	5	3																			.	.	.	.	.	.	.	.
TAX	A → X																AA	2	1																											N	.	.	.	.	.	Z	.
TAY	A → Y																A8	2	1																											N	.	.	.	.	.	Z	.
TRB	$\overline{A}$ ∧ M → M				1C	6	3	14	5	2																																					.	.	.	.	.	.	Z	.
TSB	A ∨ M → M				0C	6	3	04	5	2																																					.	.	.	.	.	.	Z	.
TSX	S → X																BA	2	1																											N	.	.	.	.	.	Z	.
TXA	X → A																8A	2	1																											N	.	.	.	.	.	Z	.
TXS	X → S																9A	2	1																											.	.	.	.	.	.	.	.
TYA	Y → A																98	2	1																											N	.	.	.	.	.	Z	.

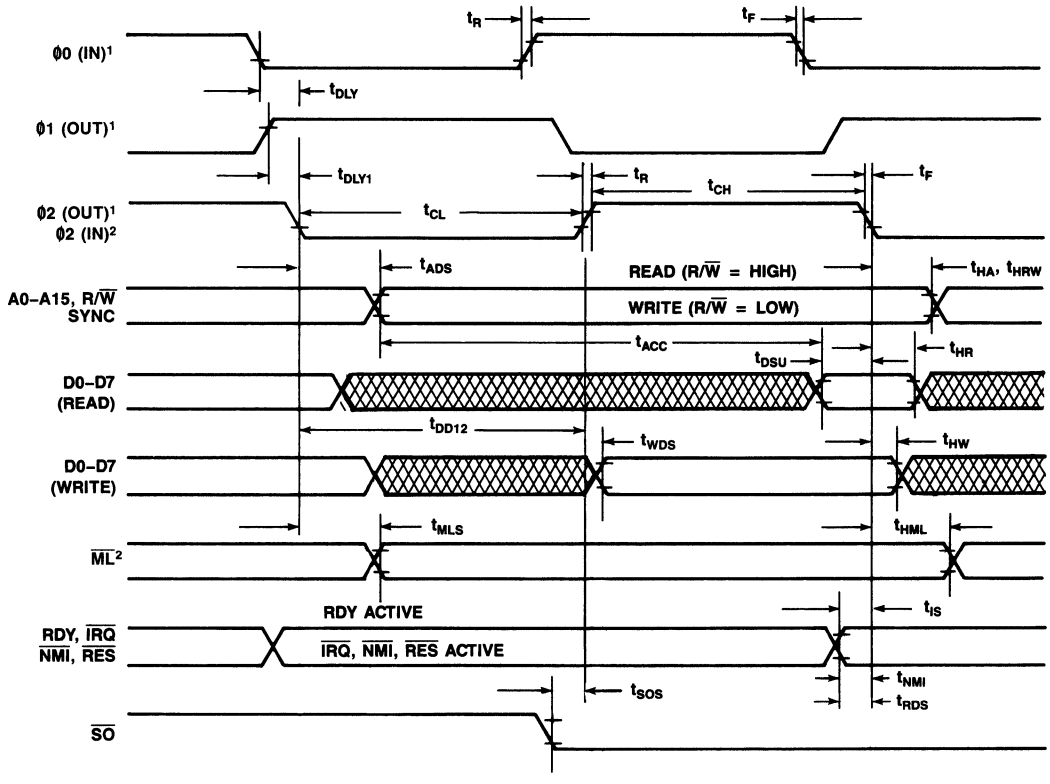
Notes:
1 Add 1 to N if page boundary is crossed
2 Add 1 to N if branch occurs to same page
Add 2 to N if branch occurs to different page
3 Carry not ($\overline{C}$) = Borrow
4 Effects 8-bit data field of the specified zero page address
5 Add 1 to N if in Decimal Mode
6 On the Bit immediate instruction, the results of the M_7 and M_6 bits (N and V flags) are indeterminate and should be considered invalid
7 If in Decimal Mode, Z flag is invalid Accumulator must be checked for zero result
8 JMP (OP Code 6C) is an Absolute Indirect Addressing Mode (ABS)

LEGEND
X = Index X
Y = Index Y
A = Accumulator
M = Memory per effective address
M_s = Memory per stack pointer
M_b = Selecter zero page memory bit
M_7 = Memory Bit 7
M_6 = Memory Bit 6
• = Add
− = Subtract
∧ = And
∨ = Or
⊻ = Exclusive or
n = Number of cycles
# = Number of Bytes

AC CHARACTERISTICS

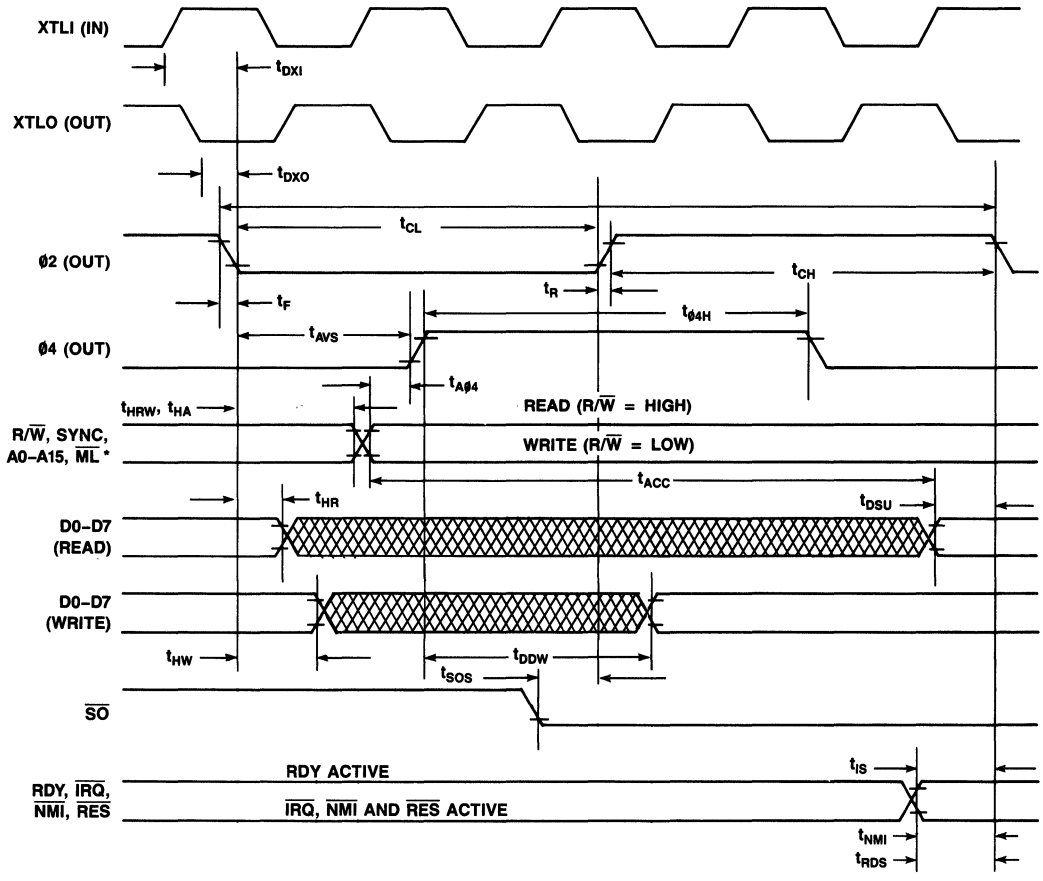
Parameter	Symbol	1 MHz		2 MHz		3 MHz		4 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
CLOCK TIMING										
Ø2 Cycle Time	t_{CYC}	1000	Note 1	500	Note 1	333	Note 1	250	Note 1	ns
Ø2 Low Pulse Width	t_{CL}	430	5000	210	5000	150	5000	100	5000	ns
Ø2 High Pulse Width	t_{CH}	450	—	220	—	160	—	110	—	ns
Ø0 Low to Ø2 Low Skew[2]	t_{DLY}	—	50	—	50		40	—	30	ns
Ø2 Low to Ø1 High Skew[3]	t_{DLY1}	-20	20	-20	20	-20	20	-20	20	ns
XTLI High to Ø2 Low[4]	t_{DXI}	—	100	—	100	—	100	—	100	ns
XTLO Low to Ø2 Low[4]	t_{DXO}	—	75	—	75	—	75	—	75	ns
Ø2 Low to Ø4 High Delay[4]	t_{AVS}	250	—	125	—	85	—	65	ns	
Ø4 Low Pulse Width[4]	$t_{\phi 4L}$	430	—	210	—	150	—	100	—	ns
Ø4 High Pulse Width[4]	$t_{\phi 4H}$	450	5000	220	5000	160	5000	110	5000	ns
Clock Rise and Fall Times	t_R, t_F	—	25	—	20	—	15	—	12	ns
READ/WRITE TIMING										
R/$\overline{W}$ Setup Time	t_{RWS}	—	125	—	100	—	75	—	60	ns
R/$\overline{W}$ Hold Time	t_{HRW}	15	—	15	—	15	—	15	—	ns
Address Setup Time	t_{ADS}	—	125	—	100	—	85	—	70	ns
Address Valid to Ø4 High[4]	$t_{A\phi 4}$	100	—	25	—	10	—	0	—	ns
Address Hold Time	t_{HA}	15	—	15	—	15	—	15	—	ns
Read Access Time	t_{ACC}	775	—	340	—	215	—	160	—	ns
Read Data Setup Time	t_{DSU}	100	—	60	—	40	—	30	—	ns
Read Data Hold Time	t_{HR}	10	—	10	—	10	—	10	—	ns
Write Data Delay Time[2]	t_{WDS}	—	200	—	110	—	85	—	55	ns
Write Data Delay Time[4]	t_{DDW}	—	200	—	110	—	85	—	55	ns
Write Data Delay Time[6]	t_{DD12}	—	450	—	235	—	170	—	120	ns
Write Data Hold Time	t_{HW}	30	—	30	—	30	—	30	—	ns
CONTROL LINE TIMING										
SYNC Delay	t_{SYS}	—	125	—	100	—	85	—	70	ns
RDY Setup Time	t_{RDS}	200	—	110	—	80	—	60	—	ns
$\overline{SO}$ Setup Time	t_{SOS}	75	—	50	—	40	—	30	—	ns
ML Delay Time[5]	t_{MLS}	—	125	—	100	—	75	—	60	ns
ML Hold Time[4]	t_{MLH}	10	—	10	—	10	—	10	—	ns
ML Hold Time[6]	t_{MLH}	15	—	15	—	15	—	15	—	ns
BE Delay Time[5][9]	t_{BE}	—	40	—	40		40		40	ns
$\overline{IRQ}$, $\overline{RES}$ Setup Time	t_{IS}	200	—	110	—	80	—	60	—	ns
$\overline{NMI}$ Setup Time	t_{NMI}	300	—	200	—	170	—	150	—	ns

Notes:
1. R65C02 and R65C102 minimum operating frequency is limited by Ø2 low pulse width. All processors can be stopped with Ø2 held high.
2. R65C02 only.
3. R65C02 and R65C102 only.
4. R65C102 only.
5. R65C102 and R65C112 only.
6. R65C112 only.
7. Voltage levels shown are $V_L \leq 0.4V$ and $V_H \geq 2.4V$ unless otherwise stated.
8. Measurement points shown are 0.8V (low) and 2.0V (high) for inputs and 1.5V (low and high) for outputs, unless otherwise specified.
9. BE signal is asynchronous.



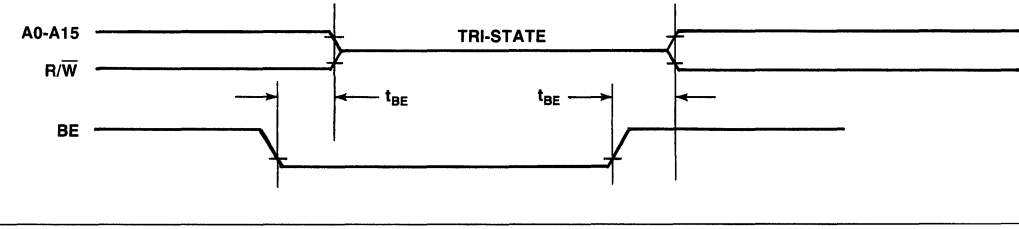
NOTES:
1. R65C02
2. R65C112
3. ALL TIMING IS REFERENCED FROM A HIGH VOLTAGE OF 2.4 VOLTS AND A LOW OF 0.5 VOLTS

Figure 3. Timing Diagram for the R65C02 and R65C112



NOTE: ALL TIMING IS REFERENCED FROM A HIGH VOLTAGE OF 2.4 VOLTS AND A LOW OF 0.5 VOLTS

Figure 4. Timing Diagram for the R65C102



NOTE: BUS ENABLE APPLIES TO THE R65C102 AND R65C112. BE IS ASYNCHRONOUS AND THEREFORE NOT DIRECTLY RELATED TO THE Ø2 CLOCK.

Figure 5. Timing Diagram for Bus Enable (BE)

CLOCK/CRYSTAL CONSIDERATIONS

A crystal controlled time base generator circuit should be used to drive ØO (IN) (R65C02) or the XTLI and XTLO (R65C102) inputs.

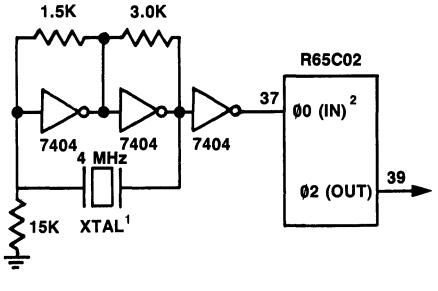
Figure 6 shows a time base generation scheme, for a 4 MHz operation of the R65C02, that has been tested and proven reliable for normal environments.

Figure 7 shows a possible external clock scheme for a R65C102 and R65C112 master/slave configuration. Table 6 identifies the typical values for external capacitors at various crystal frequencies.

NOTE

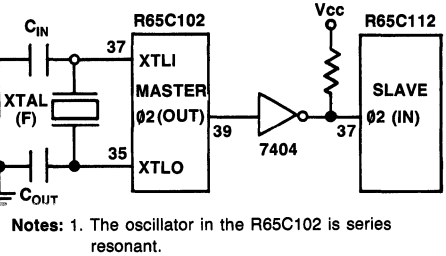
As with any clock oscillator circuit, stray capacitance due to board layout can affect circuit operation requiring "fine tuning" (e.g., component repositioning or value change) of the circuits shown in Figures 6 and 7.

Table 6 identifies nominal crystal parameters for five crystal frequencies.



Notes: 1. Crystal CTS Knight MP Series.
2. See STOPPING THE CLOCK CAUTION.

Figure 6. Example of R65C02 External Time Base Generator Circuit.



Notes: 1. The oscillator in the R65C102 is series resonant.
2. R65C102 crystal frequency is divided by 4, i.e., ØZ (OUT) = F/4.
3. See STOPPING THE CLOCK CAUTION.
4. See Table 6 for component values.

Figure 7. Example of R65C102/R65C112 Master/Slave Clock Circuit

Table 6. Typical R65C102/R65C112 Master/Slave Clock Circuit Component Values

XTAL FREQ (MHz)	C_{IN} (pF)	C_{OUT} (pF)	ØZ FREQ (MH_3)
16.0	16	16	4
8.0	18	18	2
6.0	20	20	1.5
4.0	24	24	1

Table 7. Nominal Crystal Parameters

KTAL FREQ (MHz)	R_S (ohms)	C_0 (pF)	C_1 (pF)	Q (K)
16.0	10-30	3-5	0.01-0.02	720K
8.0	20-40	4-6	0.01-0.02	720K
6.0	30-50	4-6	0 01-0.02	720K
4.0	50	6 5	0 025	730K
3.58	60	3.5	0.015	740K

Note: These represent cut crystal parameters only. Others may be used.

STOPPING THE CLOCK-STANDBY MODE

Caution must be exercised when configuring the R65C02 or R65C112 in the standby mode (i.e., ØO IN or ØZ IN clock stopped). The input clock can be held in the high state indefinitely; however, if the input clock is held in the low state longer than 5 microseconds, internal register and data status can be lost. Figure 8 shows a circuit that will stop the ØO IN (R65C02) or ØZ IN R65C112) clock in the high state during standby mode.

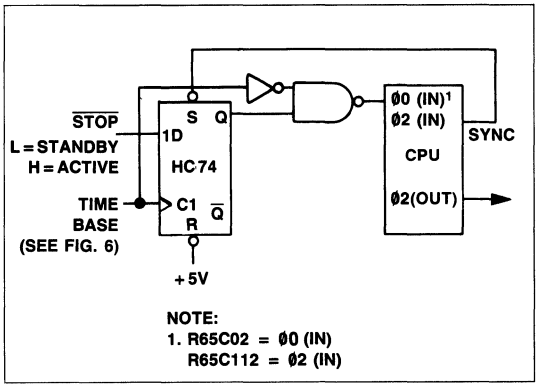


Figure 8. Stopping the Clock (Standby Mode) Circuit

MAXIMUM RATINGS*

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to +7.0	Vdc
Input Voltage	V_{IN}	−0.3 to V_{CC} +0.3	Vdc
Output Voltage	V_{OUT}	−0.3 to V_{CC} +0.3	Vdc
Operating Temperature Commercial Industrial	T_A	 0 to +70 −40 to +85	°C
Storage Temperature	T_{STG}	−55 to +150	°C

***Note**

Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in other sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING CONDITIONS

Parameter	Symbol	Value
Supply Voltage	V_{CC}	5V ±5%
Temperature Range Commercial Industrial	T_A	 0° to 70°C −40°C to +85°C

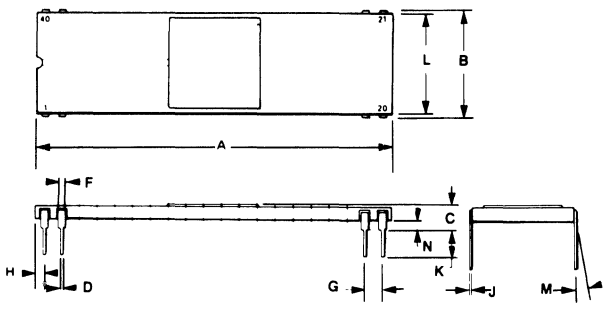
DC CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input High Voltage	V_{IH}				V	
All Other Input Pins		2.0		V_{CC} + 0.3		
Ø0 on R65C02		2.4		V_{CC} + 0.3		
Ø2 on R65C112		V_{CC} − 0.4		V_{CC} + 0.3		
Input Low Voltage	V_{IL}				V	
All Other Input Pins		−0.3		+0.8		
Ø0 on R65C02		−0.3		+0.4		
Ø2 on R65C112		−0.3		+0.4		
Input Leakage Current	I_{IN}				μA	V_{IN} = 0V to 5.25V
$\overline{NMI}$, $\overline{IRQ}$, BE, RDY, $\overline{RES}$, $\overline{SO}$		—		−50		V_{CC} = 0V
Ø2 IN, Ø0 IN, XTLI		—		1.0		
Three-State (Off State) Input Current	I_{TSI}				μA	V_{IN} = 0.4V to 2.4V
Data Lines		—		10		V_{CC} = 5.25V
Output High Voltage						
SYNC, Data, A0–A15, R/$\overline{W}$, Ø1, Ø2, Ø4, $\overline{ML}$	V_{OH}	2.4		—	V	V_{CC} = 4.75V I_{LOAD} = −100 μA
Output Low Voltage	V_{OL}	—		+0.4	V	V_{CC} = 4.75V
SYNC, Data, A0–A15, R/$\overline{W}$, Ø1, Ø2, Ø4, $\overline{ML}$						I_{LOAD} = 1.6 mA
Supply Current						
Standby[4]	I_{CC}	—	2	10	μA	V_{CC} = 5.0V
Active (R65C02)		—	2.6	4	mA/MHz	
Active (R65C102)		—	5	7	mA/MHz	
Active (R65C112)		—	2	4	mA/MHz	
Low Power (R65C02)		—	1.1	2	mA/MHz	RDY = 0
Low Power (R65C102)			3	4	mA/MHz	RDY = 0
Low Power (R65C112)			0.7	1	mA/MHz	
Capacitance	C				pF	
$\overline{NMI}$, $\overline{IRQ}$, $\overline{SO}$, BE, RDY	C_{IN}	—		7		V_{CC} = 5.0V
Data, Ø1, Ø2, Ø4, $\overline{ML}$, XTLO		—		10		V_{IN} = 0V
A0–A15, R/$\overline{W}$, SYNC	C_{OUT}					f = 1 MHz
Ø0 (IN), XTLI	C_0			10		T_A = 25°C
Ø2 (IN)	C_2	—		30		

Notes:
1. All units are direct current (dc).
2. Negative sign indicates outward current flow, positive indicates inward flow.
3. $\overline{IRQ}$ and $\overline{NMI}$ require external pull-up resistor.
4. Typical values are shown for V_{CC} = 5.0V and T_A = 25°C

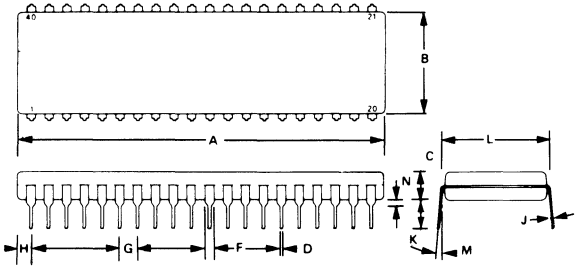
PACKAGE DIMENSIONS

40-PIN CERAMIC DIP



DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	50 29	51 31	1 980	2 020
B	14 86	15 62	0 585	0 615
C	2 54	4 19	0 100	0 165
D	0 38	0 53	0 015	0 021
F	0 76	1 40	0 030	0 055
G	2 54 BSC		0 100 BSC	
H	0 76	1 78	0 030	0 070
J	0 20	0 33	0 008	0 013
K	2 54	4 19	0 100	0 165
L	14 60	15 37	0 575	0 605
M	0°	10°	0°	10°
N	0 51	1 52	0 020	0 060

40-PIN PLASTIC DIP



DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	51 28	52 32	2 040	2 060
B	13 72	14 22	0 540	0 560
C	3 55	5 08	0 140	0 200
D	0 36	0 51	0 014	0 020
F	1 02	1 52	0 040	0 060
G	2 54 BSC		0 100 BSC	
H	1 65	2 16	0 065	0 085
J	0 20	0 30	0 008	0 012
K	3 05	3 56	0 120	0 140
L	15 24 BSC		0 600 BSC	
M	7°	10°	7°	10°
N	0 51	1 02	0 020	0 040

Rockwell

R65C21
PERIPHERAL INTERFACE ADAPTER (PIA)

PRELIMINARY

DESCRIPTION

The R65C21 Peripheral Interface Adapter (PIA) is designed to solve a broad range of peripheral control problems in the implementation of microcomputer systems. This device allows a very effective trade-off between software and hardware by providing significant capability and flexibility in a low cost chip. When coupled with the power and speed of the R6500, R6500/* or R65C00 family of microprocessors, the R65C21 allows implementation of very complex systems at a minimum overall cost.

Control of peripheral devices is handled primarily through two 8-bit bidirectional ports. Each of these lines can be programmed to act as either an input or an output. In addition, four peripheral control/interrupt input lines are provided. These lines can be used to interrupt the processor or to "handshake" data between the processor and a peripheral device

FEATURES

- Low power CMOS N-well silicon gate technology
- Direct replacement for NMOS R6520 or MC6821 PIA
- Two 8-bit bidirectional I/O ports with individual data direction control
- Automatic "Handshake" control of data transfers
- Two interrupts (one for each port) with program control
- 1, 2, 3, and 4 MHz versions
- Commercial and industrial temperature range versions
- 40-pin plastic and ceramic versions
- 5 volt ±5% supply requirements
- Compatible with the R6500, R6500/* and R65C00 family of microprocessors

ORDERING INFORMATION

The R65C21 is available in both a ceramic and a plastic 40-pin package, a commercial or industrial operating temperature range, and operating frequencies of 1, 2, 3, or 4 MHz These versions are coded into the part number as follows:

Part Number:
R65C21___

- Temperature Range (T_L to T_H):
  - Blank = 0°C to +70°C
  - E = −40°C to +85°C
- Frequency Range:
  - 1 = 1 MHz
  - 2 = 2 MHz
  - 3 = 3 MHz
  - 4 = 4 MHz
- Package.
  - C = Ceramic
  - P = Plastic

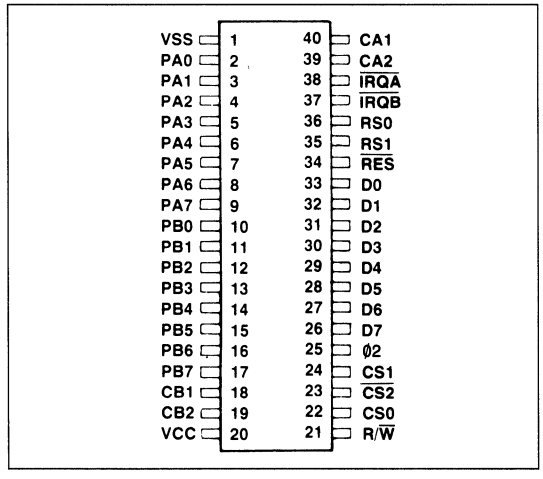


Figure 1. R65C21 Pin Configuration

FUNCTIONAL DESCRIPTION

The R65C21 PIA is organized into two independent sections referred to as the A Side and the B Side. Each section consists of a Control Register (CRA, CRB), Data Direction Register (DDRA, DDRB), Output Register (ORA, ORB), Interrupt Status Control (ISCA, ISCB), and the buffers necessary to drive the Peripheral Interface buses. Data Bus Buffers (DBB) interface data from the two sections to the data bus, while the Data Input Register (DIR) interfaces data from the DBB to the PIA registers. Chip Select and R/$\overline{W}$ control circuitry interface to the processor bus control lines. Figure 2 is a block diagram of the R65C21 PIA.

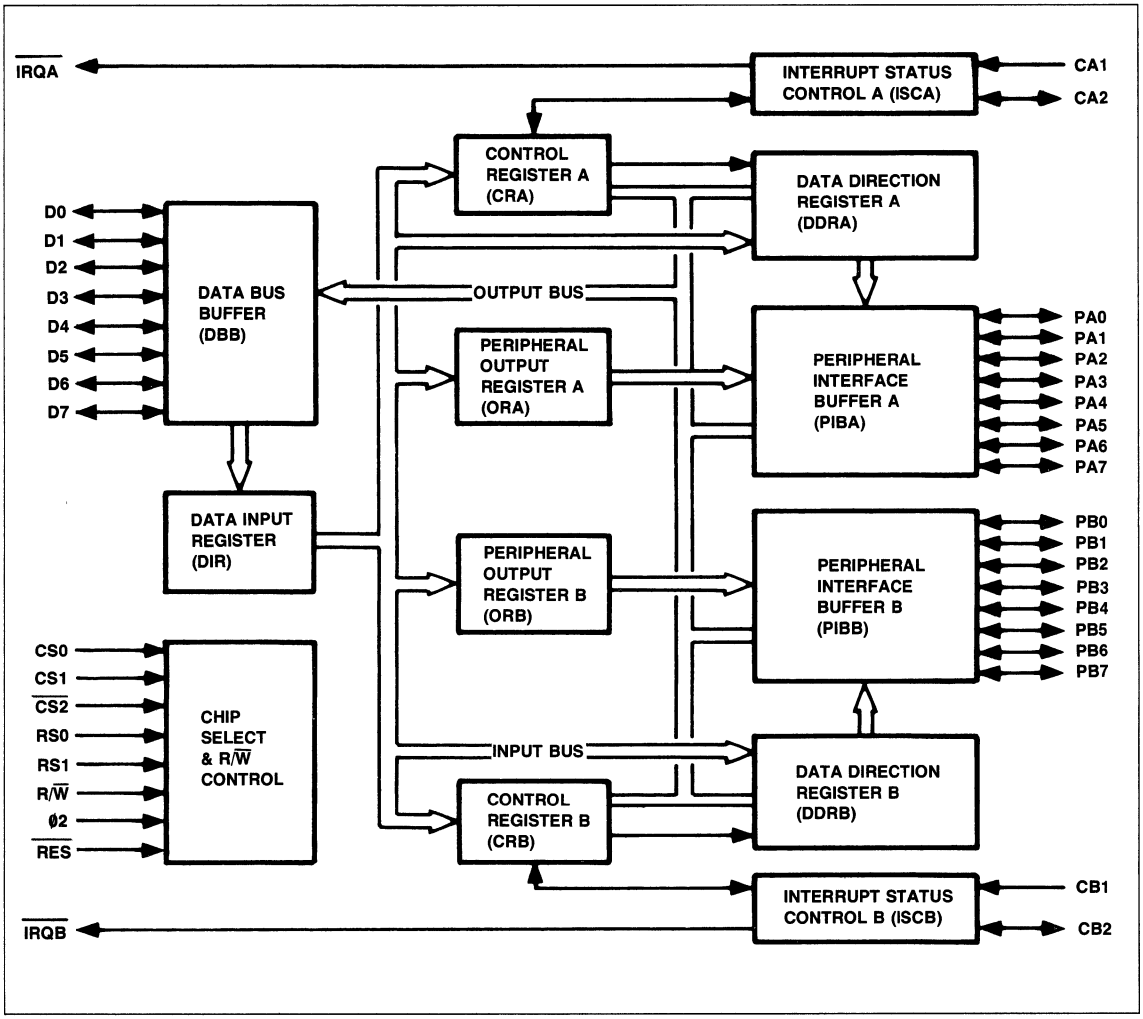


Figure 2. R65C21 PIA Block Diagram

DATA INPUT REGISTER (DIR)

When the microprocessor writes data into the PIA, the data which appears on the data bus during the Ø2 clock pulse is latched into the Data Input Register (DIR). The data is then transferred into one of six internal registers of the PIA after the trailing edge of the Ø2 clock. This assures that the data on the peripheral output lines will make smooth transitions from high to low (or from low to high) and the voltage will remain stable except when it is going to the opposite polarity.

CONTROL REGISTERS (CRA AND CRB)

Table 1 illustrates the bit designation and functions in the two control registers. The control registers allow the microprocessor to control the operation of the Interrupt Control inputs (CA1, CA2, CB1, CB2), and Peripheral Control outputs (CA2, CB2). Bit 2 in each register controls the addressing of the Data Direction Registers (DDRA, DDRB) and the Output Registers (ORA, ORB). In addition, two bits (bit 6 and 7) in each control register indicate the status of the Interrupt Input lines (CA1, CA2, CB1, CB2). These Interrupt Status bits (IRQA1, IRQA2 or IRQB1, IRQB2) are normally interrogated by the microprocessor during the $\overline{IRQ}$ interrupt service routine to determine the source of the interrupt.

DATA DIRECTION REGISTERS (DDRA, DDRB)

The Data Direction Registers (DDRA, DDRB) allow the processor to program each line in the 8-bit Peripheral I/O port to be either an input or an output. Each bit in DDRA controls the corresponding line in the Peripheral A port and each bit in DDRB controls the corresponding line in the Peripheral B port. Writing a "0" in a bit position in the Data Direction Register causes the corresponding Peripheral I/O line to act as an input; a "1" causes it to act as an output.

Bit 2 (DDRA, DDRB) in each Control Register (CRA and CRB) controls the accessing to the Data Direction Register or the Peripheral interface. If bit 2 is a "1," a Peripheral Output register (ORA, ORB) is selected, and if bit 2 is a "0," a Data Direction Register (DDRA, DDRB) is selected. The Data Direction Register Access Control bit, together with the Register Select lines (RS0, RS1) selects the various internal registers as shown in Table 2.

In order to write data into DDRA, ORA, DDRB, or ORB registers, bit 2 in the proper Control Register must first be set. The desired register may then be accessed with the address determined by the address interconnect technique used.

PERIPHERAL OUTPUT REGISTERS (ORA, ORB)

The Peripheral Output Registers (ORA, ORB) store the output data from the Data Bus Buffers (DBB) which appears on the Peripheral I/O port. If a line on the Peripheral A Port is programmed as an output by the DDRA, writing a 0 into the corresponding bit in the ORA causes that line to go low (<0.4 V); writing a 1 causes the line to go high. The lines of the Peripheral B port are controlled by ORB in the same manner.

INTERRUPT STATUS CONTROL (ISCA, ISCB)

The four interrupt/peripheral control lines (CA1, CA2, CB1, CB2) are controlled by the Interrupt Status Control logic (A, B). This logic interprets the contents of the corresponding Control Register and detects active transitions on the interrupt inputs.

PERIPHERAL I/O PORTS (PA0-PA7, PB0-PB7)

The Peripheral A and Peripheral B I/O ports allow the microprocessor to interface to the input lines on the peripheral device by writing data into the Peripheral Output Register. They also allow the processor to interface with the peripheral device output lines by reading the data on the Peripheral Port input lines directly onto the data bus and into the internal registers of the processor.

Each of the Peripheral I/O lines can be programmed to act as an input or an output. This is accomplished by setting a 1 in the corresponding bit in the Data Direction Register for those lines which are to act as outputs. A 0 in a bit of the Data Direction Register causes the corresponding Peripheral I/O lines to act as an input.

The buffers which drive the Peripheral A I/O lines contain "passive" pull-up devices. These pull-up devices are resistive in nature and therefore allow the output voltage to go to VCC for a logic 1. The switches can sink a full 3.2 mA, making these buffers capable of driving two standard TTL loads.

In the input mode, the pull-up devices are still connected to the I/O pin and still supply current to this pin. For this reason, these lines also represent two standard TTL loads in the input mode.

The Peripheral B I/O port duplicates many of the functions of the Peripheral A port. The process of programming these lines to act as an input or an output is similar to the Peripheral A port, as is the effect of reading or writing this port. However, there are several characteristics of the buffers driving these lines which affect their use in peripheral interfacing.

Table 1. Control Registers Bit Designations

	7	6	5	4	3	2	1	0
CRA	IRQA1	IRQA2	CA2 Control			DDRA Access	CA1 Control	
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CRB	IRQB1	IRQB2	CB2 Control			DDRB Access	CB1 Control	

The Peripheral B I/O port buffers are push-pull devices i.e., the pull-up devices are switched OFF in the 0 state and ON for a logic 1. Since these pull-ups are active devices, the logic 1 voltage will not go higher than +2.4V.

Another difference between the PA0-PA7 lines and the PB0 through PB7 lines is that they have three-state capability which allows them to enter a high impedance state when programmed to be used as input lines. In addition, data on these lines will be read properly, when programmed as output lines, even if the data signals fall below 2.0 volts for a "high" state or are above 0.8 volts for a "low" state. When programmed as output, each line can drive at least a two TTL load and may also be used as a source of up to 3.2 milliamperes at 1.5 volts to directly drive the base of a transistor switch, such as a Darlington pair.

Because these outputs are designed to drive transistors directly, the output data is read directly from the Peripheral Output Register for those lines programmed to act as inputs.

The final characteristic is the high-impedance input state which is a function of the Peripheral B push-pull buffers. When the Peripheral B I/O lines are programmed to act as inputs, the output buffer enters the high impedance state.

DATA BUS BUFFERS (DBB)

The Data Bus Buffers are 8-bit bidirectional buffers used for data exchange, on the D0-D7 Data Bus, between the microprocessor and the PIA. These buffers are tri-state and are capable of driving a two TTL load (when operating in an output mode) and represent a one TTL load to the microprocessor (when operating in an input mode).

INTERFACE SIGNALS

The PIA interfaces to the R6500, R6500/* or the R65C00 microprocessor family with a reset line, a Ø2 clock line, a read/write line, two interrupt request lines, two register select lines, three chip select lines, and an 8-bit bidirectional data bus.

The PIA interfaces to the peripheral devices with four interrupt/control lines and two 8-bit bidirectional data buses.

Figure 1 (on the front page) shows the pin assignments for these interface signals and Figure 3 shows the interface relationship of these signal as they pertain to the CPU and the peripheral devices.

CHIP SELECT (CS0, CS1, $\overline{CS2}$)

The PIA is selected when CS0 and CS1 are high and $\overline{CS2}$ is low. These three chip select lines are normally connected to the processor address lines either directly or through external decoder circuits. When the PIA is selected, data will be transferred between the data lines and PIA registers, and/or peripheral interface lines as determined by the R/$\overline{W}$, RS0, and RS1 lines and the contents of Control Registers A and B.

RESET SIGNAL ($\overline{RES}$)

The Reset ($\overline{RES}$) input initializes the R65C21 PIA. A low signal on the $\overline{RES}$ input causes all internal registers to be cleared.

CLOCK SIGNAL (Ø2)

The Phase 2 Clock Signal (Ø2) is the system clock that triggers all data transfers between the CPU and the PIA. Ø2 is generated by the CPU and is therefore the synchronizing signal between the CPU and the PIA.

READ/WRITE SIGNAL (R/$\overline{W}$)

Read/Write (R/$\overline{W}$) controls the direction of data transfers between the PIA and the data lines associated with the CPU and the peripheral devices. A high on the R/$\overline{W}$ line permits the peripheral devices to transfer data to the CPU from the PIA. A low on the R/$\overline{W}$ line allows data to be transfered from the CPU to the peripheral devices from the PIA.

REGISTER SELECT (RS0, RS1)

The two Register Select lines (RS0, RS1), in conjunction with the Control Registers (CRA, CRB) Data Direction Register access bits (see Table 1, bit 2) select the various R65C21 registers to be accessed by the CPU. RS0 and RS1 are normally connected to the microprocessor (CPU) address output lines. Through control of these lines, the CPU can write directly into the Control

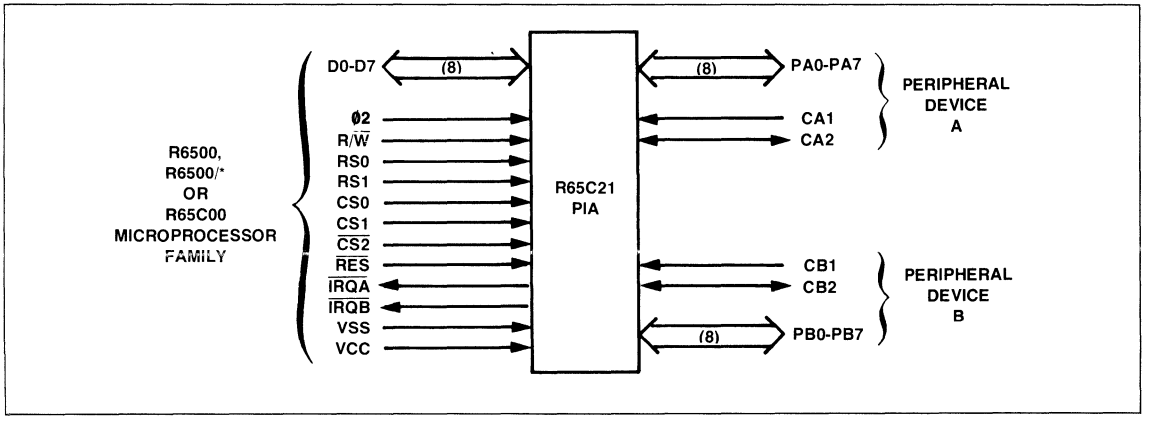


Figure 3. Interface Signals Relationship

Registers (CRA, CRB) the Data Direction Registers (DDRA, DDRB) and the Peripheral Output Registers (ORA, ORB). In addition, the processor may directly read the contents of the Control Registers and the Data Direction Registers. Accessing the Peripheral Output Register for the purpose of reading data back into the processor operates differently on the ORA and the ORB registers and therefore are shown separately in Table 2.

Table 2. ORA and ORB Register Addressing

Register Address (Hex)	Register Select Lines		Data Direction Control		Register Operation	
	RS1	RS0	CRA (Bit 2)	CRB (Bit 2)	R/$\overline{W}$=H	R/$\overline{W}$=L
0	L	L	1	—	Read PIBA	Write ORA
0	L	L	0	—	Read DDRA	Write DDRA
1	L	H	—	—	Read CRA	Write CRA
2	H	L	—	1	Read PIBB	Write ORB
2	H	L	—	0	Read DDRB	Write DDRB
3	H	H	—	—	Read CRB	Write CRB

INTERRUPT REQUEST LINES ($\overline{IRQA}$, $\overline{IRQB}$)

The active low Interrupt Request lines ($\overline{IRQA}$ and $\overline{IRQB}$) act to interrupt the microprocessor either directly or through external interrupt priority circuitry. These lines are open drain and are capable of sinking 1.6 milliamps from an external source. This permits all interrupt request lines to be tied together in a wired-OR configuration. The A and B in the titles of these lines correspond to the peripheral port A and the peripheral port B so that each interrupt request line services one peripheral data port.

Each Interrupt Request line has two interrupt flag bits which can cause the Interrupt Request line to go low. These flags are bits 6 and 7 in the two Control Registers (CRA, CRB). These flags act as the link between the peripheral interrupt signals and the microprocessor interrupt inputs. Each flag has a corresponding interrupt disable bit which allows the processor to enable or disable the interrupt from each of the four interrupt inputs (CA1, CA2, CB1, CB2). The four interrupt flags are set (enabled) by active transitions of the signal on the interrupt input (CA1, CA2, CB1, CB2).

CRA bit 7 (IRQA1) is always set by an active transition of the CA1 interrupt input signal. However, $\overline{IRQA}$ can be disabled by setting bit 0 in CRA to a 0. Likewise, CRA bit 6 (IRQA2) can be set by an active transition of the CA2 interrupt input signal and $\overline{IRQA}$ can be disabled by setting bit 3 in CRA to a 0.

Both bit 6 and bit 7 in CRA are reset by a "Read Peripheral Output Register A" operation. This is defined as an operation in which the read/write, proper data direction register and register select signals are provided to allow the processor to read the Peripheral A I/O port. A summary of $\overline{IRQA}$ control is shown in Table 3.

Control of $\overline{IRQB}$ is performed in exactly the same manner as that described above for $\overline{IRQA}$. Bit 7 in CRB (IRQB1) is set by an active transition on CB1 and $\overline{IRQB}$ from this flag is controlled by CRB bit 0. Likewise, bit 6 (IRQB2) in CRB is set by an active transition on CB2, and $\overline{IRQB}$ from this flag is controlled by CRB bit 3.

Also, both bit 6 and bit 7 of CRB are reset by a "Read Peripheral B Output Register" operation. A summary of $\overline{IRQB}$ control is shown in Table 3.

Table 3. $\overline{IRQA}$ and $\overline{IRQB}$ Control Summary

Control Register Bits	Action
CRA-7=1 and CRA-0=1	$\overline{IRQA}$ goes low (Active)
CRA-6=1 and CRA-3=1	$\overline{IRQA}$ goes low (Active)
CRB-7=1 and CRB-0=1	$\overline{IRQB}$ goes low (Active)
CRB-6=1 and CRB-3=1	$\overline{IRQB}$ goes low (Active)

Note:

The flags act as the link between the peripheral interrupt signals and the processor interrupt inputs. The interrupt disable bits allow the processor to control the interrupt function.

INTERRUPT INPUT/PERIPHERAL CONTROL LINES (CA1, CA2, CB1, CB2)

The four interrupt input/peripheral control lines provide a number of special peripheral control functions. These lines greatly enhance the power of the two general purpose interface ports (PA0-PA7, PB0-PB7). Figure 4 summarizes the operation of these control lines.

CA1 is an interrupt input only. An active transition of the signal on this input will set bit 7 of the Control Register A to a logic 1. The active transition can be programmed by setting a "0" in bit 1 of the CRA if the interrupt flag (bit 7 of CRA) is to be set on a negative transition of the CA1 signal or a "1" if it is to be set on a positive transition.

NOTE:

A negative transition is defined as a transition from a high to a low, and a positive transition is defined as a transition from a low to a high voltage.

CA2 can act as a totally independent interrupt or as a peripheral control output. As an input (CRA, bit 5 = 0) it acts to set the interrupt flag, bit 6 of CRA, to a logic 1 on the active transition selected by bit 4 of CRA.

These control register bits and interrupt inputs serve the same basic function as that described above for CA1. The input signal sets the interrupt flag which serves as the link between the peripheral device and the processor interrupt structure. The interrupt disable bit allows the processor to exercise control over the system interrupt.

In the output mode (CRA, bit 5 = 1), CA2 can operate independently to generate a simple pulse each time the microprocessor reads the data on the Peripheral A I/O port. This mode is selected by setting CRA, bit 4 to a 0 and CRA, bit 3 to a 1. This pulse output can be used to control the counters, shift registers, etc., which make sequential data available on the Peripheral input lines.

CONTROL REGISTER A (CRA)

CA2 INPUT MODE (BIT 5 = 0)

7	6	5	4	3	2	1	0
IRQA1 FLAG	IRQA2 FLAG	CA2 INPUT MODE SELECT (=0)	IRQA2 POSITIVE TRANSITION	$\overline{\text{IRQA}}$ ENABLE FOR IRQA2	ORA SELECT	IRQA1 POSITIVE TRANSITION	$\overline{\text{IRQA}}$ ENABLE FOR IRQA1
			IRQA/IRQA2 CONTROL			$\overline{\text{IRQA}}$/IRQA1 CONTROL	

CA2 OUTPUT MODE (BIT 5 = 1)

7	6	5	4	3	2	1	0
IRQA1 FLAG	0	CA2 OUTPUT MODE SELECT (=1)	CA2 OUTPUT CONTROL	CA2 RESTORE CONTROL	ORA SELECT	IRQA1 POSITIVE TRANSITION	$\overline{\text{IRQA}}$ ENABLE FOR IRQA1
			CA2 CONTROL			$\overline{\text{IRQA}}$/IRQA1 CONTROL	

CA2 INPUT OR OUTPUT MODE (BIT 5 = 0 or 1)

Bit 7 IRQA1 FLAG
- 1 A transition has occurred on CA1 that satisfies the bit 1 IRQA1 transition polarity criteria. This bit is cleared by a read of Output Register A or by $\overline{\text{RES}}$.
- 0 No transition has occurred on CA1 that satisfies the bit 1 IRQA1 transition polarity criteria.

Bit 2 OUTPUT REGISTER A SELECT
- 1 Select Output Register A.
- 0 Select Data Direction Register A.

Bit 1 IRQA1 POSITIVE TRANSITION
- 1 Set IRQA1 Flag (bit 7) on a positive (low-to-high) transition of CA1.
- 0 Set IRQA1 Flag (bit 7) on a negative (high-to-low) transition of CA1.

Bit 0 $\overline{\text{IRQA}}$ ENABLE FOR IRQA1
- 1 Enable assertion of $\overline{\text{IRQA}}$ when IRQA1 Flag (bit 7) is set.
- 0 Disable assertion of $\overline{\text{IRQA}}$ when IRQA1 Flag (bit 7) is set.

CA2 INPUT MODE (BIT 5 = 0)

Bit 6 IRQA2 FLAG
- 1 A transition has occurred on CA2 that satisfies the bit 4 IRQA2 transition polarity criteria. This flag is cleared by a read of Output Register A or by $\overline{\text{RES}}$.
- 0 No transition has occurred on CA2 that satisfies the bit 4 IRQA2 transition polarity criteria.

Bit 5 CA2 MODE SELECT
- 0 Select CA2 Input Mode.

Bit 4 IRQA2 POSITIVE TRANSITION
- 1 Set IRQA2 Flag (bit 6) on a positive (low-to-high) transition of CA2.
- 0 Set IRQA2 Flag (bit 6) on a negative (high-to-low) transition of CA2.

Bit 3 $\overline{\text{IRQA}}$ ENABLE FOR IRQA2
- 1 Enable assertion of $\overline{\text{IRQA}}$ when IRQA2 Flag (bit 6) is set.
- 0 Disable assertion of $\overline{\text{IRQA}}$ when IRQA2 Flag (bit 6) is set.

CA2 OUTPUT MODE (BIT 5 = 1)

Bit 6 NOT USED
- 0 Always zero.

Bit 5 CA2 MODE SELECT
- 1 Select CA2 Output Mode.

Bit 4 CA2 OUTPUT CONTROL
- 1 CA2 goes low when a zero is written into CRA bit 3. CA2 goes high when a one is written into CRA bit 3.
- 0 CA2 goes low on the first negative (high-to-low) $\phi 2$ clock transition following a read of Output Register A. CA2 returns high as specified by bit 3.

Bit 3 CA2 READ STROBE RESTORE CONTROL (4 = 0)
- 1 CA2 returns high on the next $\phi 2$ clock negative transition following a read of Output Register A.
- 0 CA2 returns high on the next active CA1 transition following a read of Output Register A as specified by bit 1.

Figure 4. Control Line Operations Summary (1 of 2)

CONTROL REGISTER B (CRB)

CB2 INPUT MODE (BIT 5 = 0)

7	6	5	4	3	2	1	0
IRQB1 FLAG	IRQB2 FLAG	CB2 INPUT MODE SELECT (=0)	IRQB2 POSITIVE TRANSITION	$\overline{\text{IRQB}}$ ENABLE FOR IRQB2	ORB SELECT	IRQB1 POSITIVE TRANSITION	$\overline{\text{IRQB}}$ ENABLE FOR IRQB1
			$\overline{\text{IRQB}}$/IRQB2 CONTROL			$\overline{\text{IRQB}}$/IRQB1 CONTROL	

CB2 OUTPUT MODE (BIT 5 = 1)

7	6	5	4	3	2	1	0
IRQB1 FLAG	0	CB2 OUTPUT MODE SELECT (=1)	CB2 OUTPUT CONTROL	CB2 RESTORE CONTROL	ORB SELECT	IRQB1 POSITIVE TRANSITION	$\overline{\text{IRQB}}$ ENABLE FOR IRQB1
			CB2 CONTROL			$\overline{\text{IRQB}}$/IRQB1 CONTROL	

CB2 INPUT OR OUTPUT MODE (BIT 5 = 0 or 1)

Bit 7 IRQB1 FLAG
- 1 A transition has occurred on CB1 that satisfies the bit 1 IRQB1 transition polarity criteria. This bit is cleared by a read of Output Register B or by $\overline{\text{RES}}$.
- 0 No transition has occurred on CB1 that satisfies the bit 1 IRQB1 transition polarity criteria.

Bit 2 OUTPUT REGISTER B SELECT
- 1 Select Output Register B.
- 0 Select Data Direction Register B.

Bit 1 IRQB1 POSITIVE TRANSITION
- 1 Set IRQB1 Flag (bit 7) on a positive (low-to-high) transition of CB1.
- 0 Set IRQB1 Flag (bit 7) on a negative (high-to-low) transition of CB1.

Bit 0 $\overline{\text{IRQB}}$ ENABLE FOR IRQB1
- 1 Enable assertion of $\overline{\text{IRQB}}$ when IRQB1 Flag (bit 7) is set.
- 0 Disable assertion of $\overline{\text{IRQB}}$ when IRQB1 Flag (bit 7) is set.

CB2 INPUT MODE (BIT 5 = 0)

Bit 6 IRQB2 FLAG
- 1 A transition has occurred on CB2 that satisfies the bit 4 IRQB2 transition polarity criteria. This flag is cleared by a read of Output Register B or by $\overline{\text{RES}}$.
- 0 No transition has occurred on CB2 that satisfies the bit 4 IRQB2 transition polarity criteria.

Bit 5 CB2 MODE SELECT
- 0 Select CB2 Input Mode.

Bit 4 IRQB2 POSITIVE TRANSITION
- 1 Set IRQB2 Flag (bit 6) on a positive (low-to-high) transition of CB2.
- 0 Set IRQB2 Flag (bit 6) on a negative (high-to-low) transition of CB2.

Bit 3 $\overline{\text{IRQB}}$ ENABLE FOR IRQB2
- 1 Enable assertion of $\overline{\text{IRQB}}$ when IRQB2 Flag (bit 6) is set.
- 0 Disable assertion of $\overline{\text{IRQB}}$ when IRQB2 Flag (bit 6) is set.

CB2 OUTPUT MODE (BIT 5 = 1)

Bit 6 NOT USED
- 0 Always zero.

Bit 5 CB2 MODE SELECT
- 1 Select CB2 Output Mode.

Bit 4 CB2 OUTPUT CONTROL
- 1 CB2 goes low when a zero is written into CRB bit 3. CB2 goes high when a one is written into CRB bit 3.
- 0 CB2 goes low on the first negative (high-to-low) Ø2 clock transition following a write to Output Register B. CB2 returns high as specified by bit 3.

Bit 3 CB2 WRITE STROBE RESTORE CONTROL (BIT 4 = 0)
- 1 CB2 returns high on the next Ø2 clock negative transition following a write to Output Register B.
- 0 CB2 returns high on the next active CB1 transition following a write to Output Register B as specified by bit 1.

Figure 4. Control Line Operations Summary (2 of 2)

A second output mode allows CA2 to be used in conjunction with CA1 to "handshake" between the processor and the peripheral device. On the A side, this technique allows positive control of data transfers from the peripheral device into the microprocessor. The CA1 input signals the processor that data is available by interrupting the processor. The processor reads the data and sets CA2 low. This signals the peripheral device that it can make new data available.

The final output mode can be selected by setting bit 4 of CRA to a 1. In this mode, CA2 is a simple peripheral control output which can be set high or low by setting bit 3 of CRA to a 1 or a 0 respectively.

CB1 operates as an interrupt input only in the same manner as CA1. Bit 7 of CRB is set by the active transition selected by bit 0 of CRB. Likewise, the CB2 input mode operates exactly the same as the CA2 input modes. The CB2 output modes, CRB bit 5 = 1, differ somewhat from those of CA2. The pulse output occurs when the processor writes data into the Peripheral B Output Register. Also, the "handshaking" operates on data transfers from the processor into the peripheral device.

READING THE PERIPHERAL A I/O PORT

Performing a Read operation with RS1 = 0, RS0 = 0 and the Data Direction Register Access Control bit (CRA-2) = 1, directly transfers the data on the Peripheral A I/O lines to the data bus. In this situation, the data bus will contain both the input and output data. The processor must be programmed to recognize and interpret only those bits which are important to the particular peripheral operation being performed.

Since the processor always reads the Peripheral A I/O port pins instead of the actual Peripheral Output Register (ORA), it is possible for the data read by the processor to differ from the contents of the Peripheral Output Register for an output line. This is true when the I/O pin is not allowed to go to a full +2.4V DC when the Peripheral Output register contains a logic 1. In this case, the processor will read a 0 from the Peripheral A pin, even though the corresponding bit in the Peripheral Output register is a 1.

READING THE PERIPHERAL B I/O PORT

Reading the Peripheral B I/O port yields a combination of input and output data in a manner similar to the Peripheral A port. However, data is read directly from the Peripheral B Output Register (ORB) for those lines programmed to act as outputs. It is therefore possible to load down the Peripheral B Output lines without causing incorrect data to be transferred back to the processor on a Read operation.

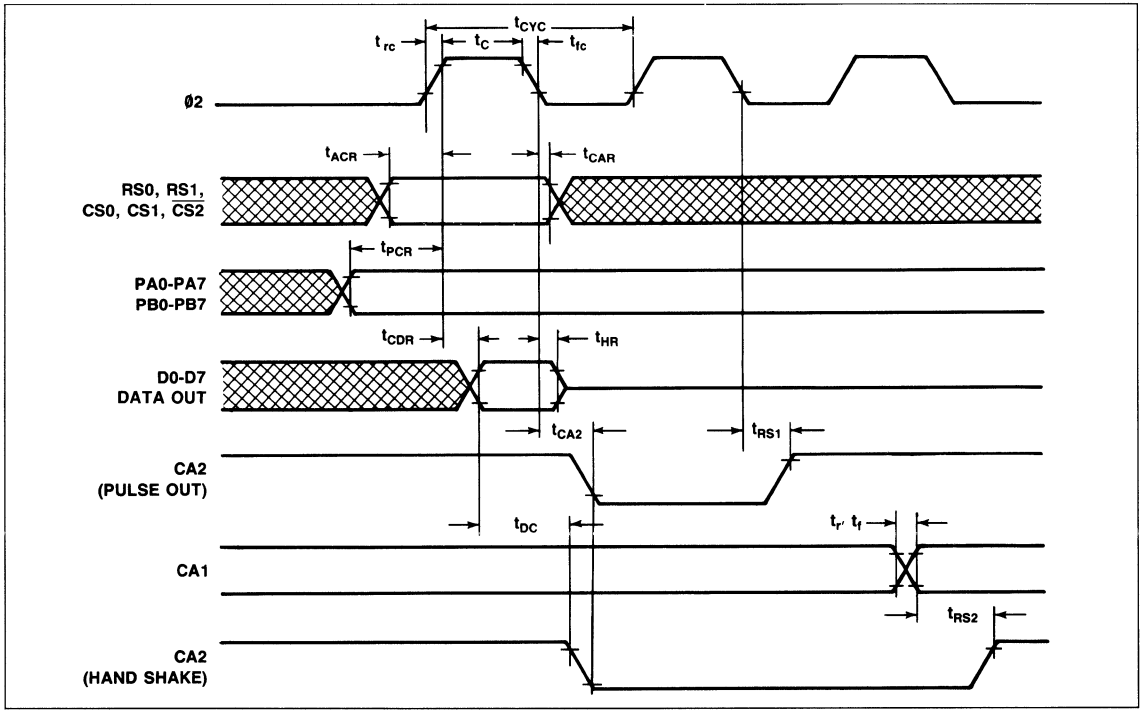


Figure 5. Read Timing Waveforms

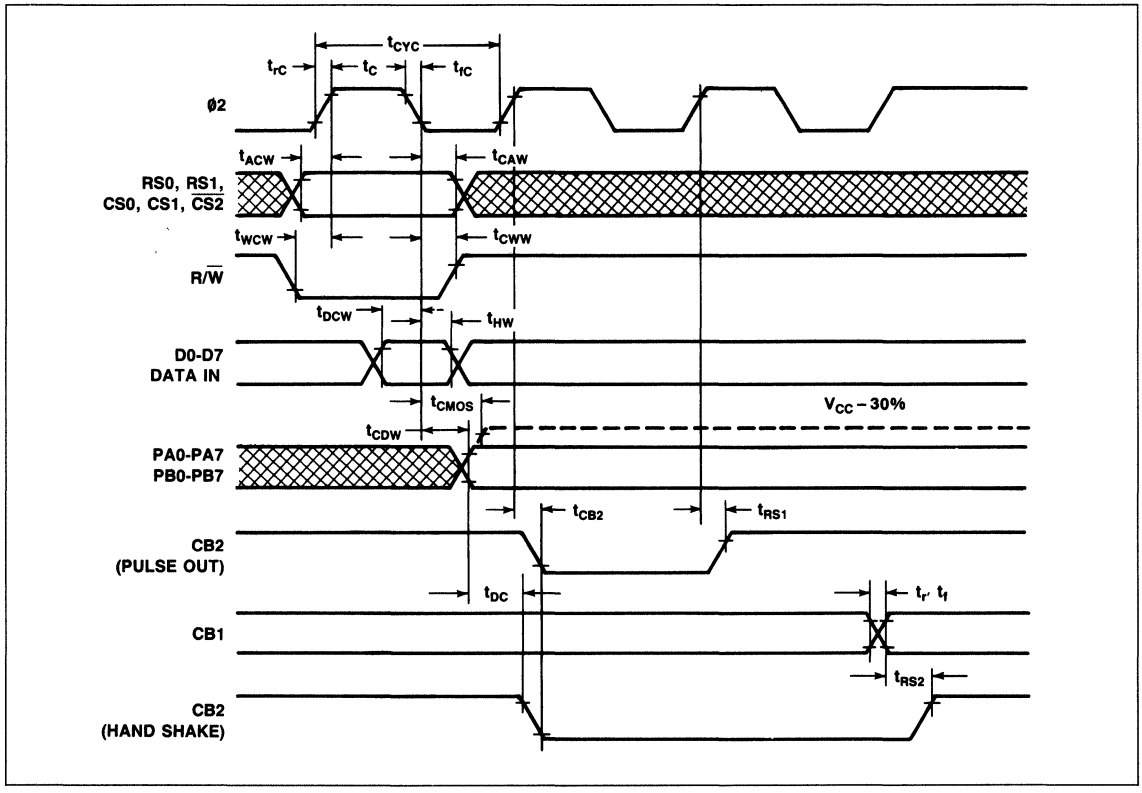


Figure 6. Write Timing Waveforms

BUS TIMING CHARACTERISTICS

Parameter	Symbol	1 MHz		2 MHz		3 MHz		4 MHz		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Ø2 Cycle	t_{CYC}	1.0	—	0.5	—	0.33	—	0.25	—	μs
Ø2 Pulse Width	t_C	450	—	220	—	160	—	110	—	ns
Ø2 Rise and Fall Time	t_{rc}, t_{fc}	—	25	—	15	—	12	—	10	ns

READ TIMING

Address Set-Up Time	t_{ACR}	140	—	70	—	53	—	35	—	ns
Address Hold Time	t_{CAR}	0	—	0	—	0	—	0	—	ns
Peripheral Data Set-Up Time	t_{PCR}	300	—	150	—	110	—	75	—	ns
Data Bus Delay Time	t_{CDR}	—	335	—	145	—	105	—	80	ns
Data Bus Hold Time	t_{HR}	20	—	20	—	20	—	20	—	ns

WRITE TIMING

Address Set-Up Time	t_{ACW}	140	—	70	—	53	—	35	—	ns
Address Hold Time	t_{CAW}	0	—	0	—	0	—	0	—	ns
R/$\overline{W}$ Set-Up Time	t_{WCW}	180	—	90	—	67	—	45	—	ns
R/$\overline{W}$ Hold Time	t_{CWW}	0	—	0	—	0	—	0	—	ns
Data Bus Set-Up Time	t_{DCW}	180	—	90	—	67	—	45	—	ns
Data Bus Hold Time	t_{HW}	10	—	10	—	10	—	10	—	ns
Peripheral Data Delay Time	t_{CPW}	—	1.0	—	0.5	—	0.33	—	0.25	μs
Peripheral Data Delay Time to CMOS Level	t_{CMOS}	—	2.0	—	1.0	—	0.7	—	0.5	μs

PERIPHERAL INTERFACE TIMING

Peripheral Data Set-Up	t_{PCR}	300	—	150	—	110	—	75	—	ns
Ø2 Low to CA2 Low Delay	t_{CA2}	—	1.0	—	0.5	—	0.33	—	0.25	μs
Ø2 Low to CA2 High Delay	t_{RS1}	—	1.0	—	0.5	—	0.33	—	0.25	μs
CA1 Active to CA2 High Delay	t_{RS2}	—	2.0	—	1.0	—	0.67	—	0.5	μs
Ø2 High to CB2 Low Delay	t_{CB2}	—	1.0	—	0.5	—	0.33	—	0.25	μs
Peripheral Data Valid to CB2 Low Delay	t_{DC}	0	1.5	0	0.75	0	0.5	0	0.37	μs
Ø2 High to CB2 High Delay	t_{RS1}	—	1.0	—	0.5	—	0.33	—	0.25	μs
CB1 Active to CB2 High Delay	t_{RS2}	—	2.0	—	1.0	—	0.67	—	0.5	μs
CA1, CA2, CB1 and CB2 Input Rise and Fall Time	t_r, t_f	—	1.0	—	1.0	—	1.0	—	1.0	μs

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to +7.0	Vdc
Input Voltage	V_{IN}	−0.3 to V_{CC} +0.3	Vdc
Output Voltage	V_{OUT}	−0.3 to V_{CC} +0.3	Vdc
Operating Temperature Range Commercial Industrial	T_A	 0 to +70 −40 to +85	°C
Storage Temperature	T_{STG}	−55 to +150	°C

*NOTE: Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in other sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING CONDITIONS

Parameter	Symbol	Value
Supply Voltage	V_{CC}	5V ±5%
Temperature Range Commercial Industrial	T_A	 0°C to 70°C −40°C to +85°C

DC CHARACTERISTICS

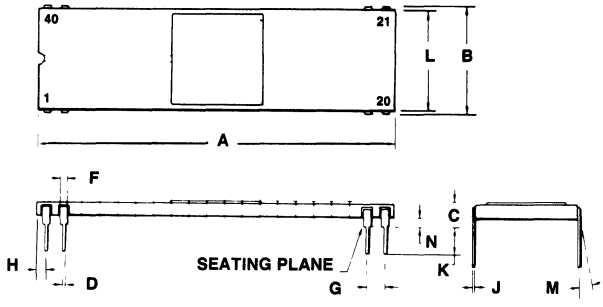
(V_{CC} = 5.0V ±5%, V_{SS} = 0, T_A = T_L to T_H, unless otherwise noted)

Parameter	Symbol	Min.	Typ.[3]	Max.	Unit[2]	Test Conditions
Input High Voltage All except PB0–PB7, $\overline{RES}$ PB0–PB7, $\overline{RES}$	V_{IH}	 +2.0 +2.4	 — —	 V_{CC} V_{CC}	 V V	
Input Low Voltage	V_{IL}	−0.3	—	+0.8	V	
Input Leakage Current R/$\overline{W}$, $\overline{RES}$, RS0, RS1, CS0, CS1, $\overline{CS2}$, CA1, CB1, Ø2	I_{IN}	—	±1	±2.5	μA	V_{IN} = 0V to V_{CC} V_{CC} = 5.25V
Input Leakage Current for Three-State Off D0–D7, PB0–PB7, CB2	I_{TSI}	—	±2	±10	μA	V_{IN} = 0.4V to 2.4V V_{CC} = 5.25V
Input High Current PA0–PA7, CA2	I_{IH}	−200	−300	—	μA	V_{IH} = 2.4V
Input Low Current PA0–PA7, CA2	I_{IL}	—	−2	−3.2	mA	V_{IL} = 0.4V
Output High Voltage Logic PB0–PB7, CB2 (Darlington Drive)	V_{OH}	 2.4 1.5	 — —	 — —		V_{CC} = 4.75V I_{LOAD} = −200μA I_{LOAD} = −3.2mA
Output Low Voltage PA0–PA7, CA2, PB0–PB7, CB2 D0–D7, $\overline{IRQA}$, $\overline{IRQB}$	V_{OL}	—	—	+0.4	V	V_{CC} = 4.75V I_{LOAD} = 3.2 mA I_{LOAD} = 1.6 mA
Output High Current (Sourcing Logic PB0–PB7, CB2 (Darlington Drive)	I_{OH}	 −200 −3.2	 −1500 −6	 — —	 μA mA	V_{OH} = 2.4V V_{OH} = 1.5V
Output Low Current (Sinking) PA0–PA7, PB0–PB7, CB2, CA2 D0–D7, $\overline{IRQA}$, $\overline{IRQB}$	I_{OL}	 3.2 1.6	 — —	 — —	 mA mA	V_{OL} = 0.4V
Output Leakage Current (Off State) $\overline{IRQA}$, $\overline{IRQB}$	I_{OFF}	—	1	±10	μA	V_{OH} = 2.4V V_{CC} = 5.25V
Power Dissipation	P_D		7	10		mW/MHz
Input Capacitance D0–D7, PA0–PA7, PB0–PB7, CA2, CB2 R/$\overline{W}$, $\overline{RES}$, RS0, RS1, CS0, CS1, $\overline{CS2}$ CA1, CB1, Ø2	C_{IN}	 — — —	 — — —	 10 7 20	 pF pF pF	V_{CC} = 5.0V V_{IN} = 0V f = 2 MHz T_A = 25°C
Output Capacitance	C_{OUT}	—	—	10	pF	

Notes:
1. All units are direct current (dc) except capacitance.
2. Negative sign indicates outward current flow, positive indicates inward flow.
3. Typical values are shown for V_{CC} = 5.0V and T_A = 25°C.

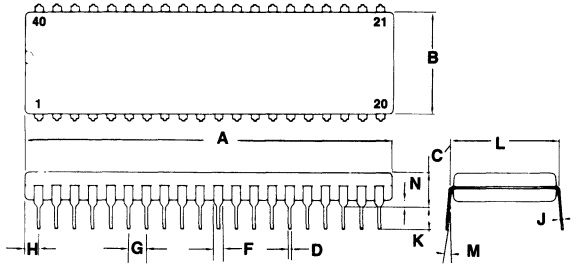
PACKAGE DIMENSIONS

40-PIN CERAMIC DIP



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	50 29	51 31	1 980	2 020
B	14 86	15 62	0 585	0 615
C	2 54	4 19	0 100	0 165
D	0 38	0 53	0 015	0 021
F	0 76	1 40	0 030	0 055
G	2 54 BSC		0 100 BSC	
H	0 76	1 78	0 030	0 070
J	0 20	0 33	0 008	0 013
K	2 54	4 19	0 100	0 165
L	14 60	15 37	0 575	0 605
M	0°	10°	0°	10°
N	0 51	1 52	0 020	0 060

40-PIN PLASTIC DIP



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	51 28	52 32	2 040	2 060
B	13 72	14 22	0 540	0 560
C	3 55	5 08	0 140	0 200
D	0 36	0 51	0 014	0 020
F	1 02	1 52	0 040	0 060
G	2 54 BSC		0 100 BSC	
H	1 65	2 16	0 065	0 085
J	0 20	0 30	0 008	0 012
K	3 05	3 56	0 120	0 140
L	15 24 BSC		0 600 BSC	
M	7	10	7	10
N	0 51	1 02	0 020	0 040

Rockwell

R65C22
VERSATILE INTERFACE ADAPTER (VIA)

PRELIMINARY

DESCRIPTION

The R65C22 Versatile Interface Adapter (VIA) is a very flexible I/O control device. In addition, this device contains a pair of very powerful 16-bit interval timers, a serial-to-parallel/parallel-to serial shift register and input data latching on the peripheral ports. Expanded handshaking capability allows control of bidirectional data transfers between VIA's in multiple processor systems.

The R65C22 includes functions for programmed control of up to two peripheral devices (Ports A and B). These two program controlled 8-bit bidirectional peripheral I/O ports allow direct interfacing between the microprocessor and selected peripheral units. Each port has input data latching capability. Two programmable Data Direction Registers (A and B) allow selection of data direction (input or output) on an individual line basis. The R65C22 also has two programmable 16-bit Interval Timer/Counters with latches. Timer 1 may be operated in a One-Shot Interrupt Mode with interrupts on each count-to-zero, or in a Free-Run Mode with a continuous series of evenly spaced interrupts. Timer 2 functions as both an interval and pulse counter. Serial data transfers are provided by a serial-to-parallel/parallel-to-serial shift register. Application versatility is further increased by various control registers, including—the Interrupt Flag Register, the Interrupt Enable Register, the Auxiliary Control Register and the Peripheral Control Register.

ORDERING INFORMATION

Part Number:
R65C22_ _ _

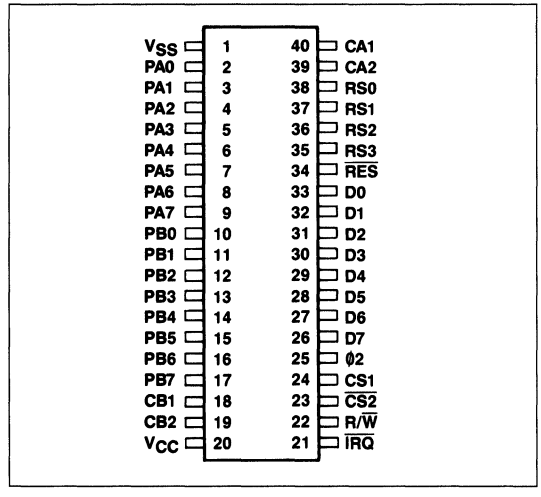
Temperature Range (T_L to T_H):
Blank = 0°C to +70°C
E = −40°C to +85°C

Frequency
1 = 1 MHz
2 = 2 MHz
3 = 3 MHz
4 = 4 MHz

Package
C = Ceramic
P = Plastic

FEATURES

- Low power CMOS N-well silicon gate technology
- Fully compatible with NMOS 6522 devices
- Two 8-bit bidirectional I/O ports
- Two 16-bit programmable timer/counters
- Serial bidirectional peripheral I/O
- TTL compatible peripheral control lines
- Expanded "handshake" capability allows positive control of data transfers between processor and peripheral devices.
- Latched output and input registers on both I/O ports
- 1, 2, 3, and 4 MHz operation
- Single +5V power supply
- 40-pin ceramic or plastic DIP



R65C22 Pin Configuration

INTERFACE SIGNALS

Figure 1 shows the relationship of R65C22 interface signals to the microprocessor and peripheral devices.

RESET ($\overline{RES}$)

Reset ($\overline{RES}$) clears all internal registers (except T1 and T2 counters and latches, and the Shift Register (SR)). In the $\overline{RES}$ condition, all peripheral interface lines (PA and PB) are placed in the input state. Also, the Timers (T1 and T2), SR and interrupt logic are disabled from operation.

INPUT CLOCK (PHASE 2)

The system Phase 2 (Ø2) Input Clock controls all data transfers between the R65C22 and the microprocessor.

READ/WRITE (R/$\overline{W}$)

The direction of the data transfers between the R65C22 and the system processor is controlled by the R/$\overline{W}$ line in conjunction with the CS1 and $\overline{CS2}$ inputs. When R/$\overline{W}$ is low, (write operation) and the R65C22 is selected, data is transferred from the processor bus into the selected R65C22 register. When R/$\overline{W}$ is high, (read operation) and the R65C22 is selected, data is transferred from the selected R65C22 register to the processor bus.

DATA BUS (D0–D7)

The eight bidirectional Data Bus lines transfer data between the R65C22 and the microprocessor. During a read operation, the contents of the selected R65C22 internal register are transferred to the microprocessor via the Data Bus lines. During a write operation, the Data Bus lines serve as high impedance inputs over which data is transferred from the microprocessor to a selected R65C22 register. The Data Bus lines are in the high impedance state when the R65C22 is unselected.

CHIP SELECTS (CS1, $\overline{CS2}$)

Normally, the two Chip Select lines are connected to the microprocessor address lines. This connection may be direct or through decoding. To access a selected R65C22 register, CS1 must be high (Logic 1) and $\overline{CS2}$ must be low (Logic 0).

REGISTER SELECTS (RS0–RS3)

The Register Select inputs allow the microprocessor to select one of 16 internal registers within the R65C22. Refer to Table 1 for Register Select coding and a functional description.

INTERRUPT REQUEST ($\overline{IRQ}$)

The Interrupt Request ($\overline{IRQ}$) output signal is generated whenever an internal Interrupt Flag bit is set and the corresponding Interrupt Enable bit is a Logic 1. The Interrupt Request output is an open-drain configuration, thus allowing the $\overline{IRQ}$ signal to be wire-0Red to a common microprocessor $\overline{IRQ}$ input line.

PERIPHERAL PORT A (PA0–PA7)

Peripheral Data Port A is an 8-line, bidirectional bus for the transfer of data, control and status information between the R65C22 and a peripheral device. Each Peripheral Data Port bus line may be individually programmed as either an input or output under control of a Data Direction Register. Data flow direction may be selected on a line-by-line basis with intermixed input and output lines within the same port. When a "0" is written to any bit position of the Data Direction Register, the corresponding line will be programmed as an input. When a "1" is written into any bit position of the register, the corresponding data line will serve as an output. Polarity of the data output is determined by the Output Register, while input data may be latched into the Input Register under control of the CA1 line. All modes are program controlled by the microprocessor by way of the R65C22's internal control registers. Each Peripheral Data Port line represents one TTL load in the input mode and will drive one standard TTL load in the output mode. A typical output circuit for Peripheral Data Port A is shown in Figure 2.

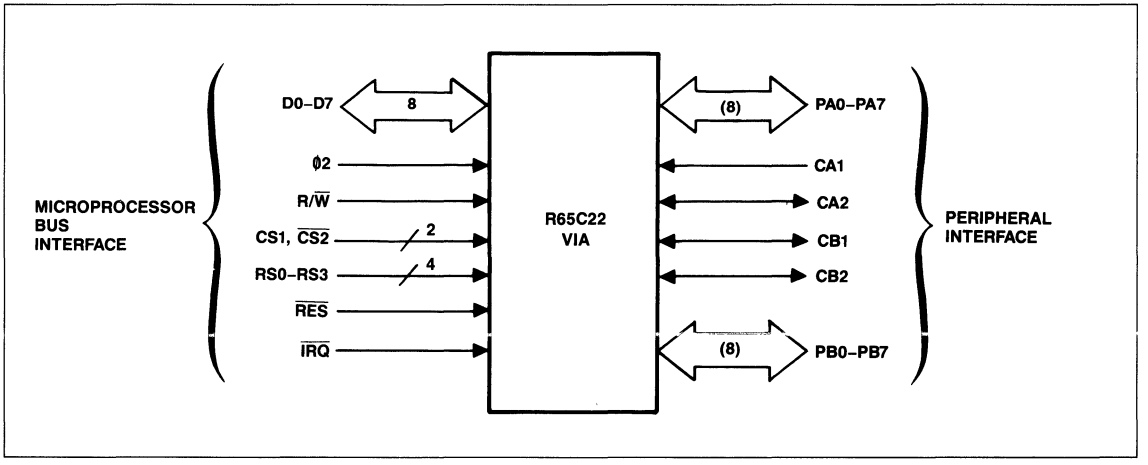


Figure 1. R65C22 VIA Interface Signals

PORT A CONTROL LINES (CA1, CA2)

Control lines CA1 and CA2 serve as interrupt inputs or handshake outputs for Peripheral Data Port A. Each line controls an internal Interrupt Flag with a corresponding Interrupt Enable bit. CA1 also controls the latching of Input Data on Port A. CA1 is a high impedance input, while CA2 represents one standard TTL load in the input mode. In the output mode, CA2 will drive one standard TTL load.

PORT B (PB0–PB7)

Peripheral Data Port B is an 8-line, bidirectional bus which is controlled by an Output Register, Input Register and Data Direction Register in a manner much the same as Data Port A. With respect to Port B, the output signal on line PB7 may be controlled by Timer 1 while Timer 2 may be programmed to count pulses on the PB6 line. Port B lines represent one standard TTL load in the input mode and will drive one TTL load in the output mode. Port B lines are also capable of sourcing 3.0 mA at 1.5 Vdc in the output mode. This allows the outputs to directly drive Darlington transistor circuits. A typical output circuit for Port B is shown in Figure 3.

PORT B CONTROL LINES (CB1, CB2)

Control lines CB1 and CB2 serve as interrupt inputs or handshake outputs for Peripheral Data Port B. Like Port A, these two control lines control an internal Interrupt Flag with a corresponding Interrupt Enable bit. These lines also serve as a serial data port under control of the Shift Register (SR). Each control line represents one standard TTL load in the input mode and can drive one TTL load in the output mode. Note that CB1 and CB2 cannot drive Darlington transistor circuits.

Table 1. R65C22 Register Addressing

Register Number	RS Coding				Register Desig.	Register/Description	
	RS3	RS2	RS1	RS0		Write (R/$\overline{W}$ = L)	Read (R/$\overline{W}$ = H)
0	0	0	0	0	ORB/IRB	Output Register B	Input Register B
1	0	0	0	1	ORA/IRA	Output Register A	Input Register A
2	0	0	1	0	DDRB	Data Direction Register B	
3	0	0	1	1	DDRA	Data Direction Register A	
4	0	1	0	0	T1C-L	T1 Low-Order Latches	T1 Low-Order Counter
5	0	1	0	1	T1C-H	T1 High-Order Counter	
6	0	1	1	0	T1L-L	T1 Low-Order Latches	
7	0	1	1	1	T1L-H	T1 High-Order Latches	
8	1	0	0	0	T2C-L	T2 Low-Order Latches	T2 Low-Order Counter
9	1	0	0	1	T2C-H	T2 High-Order Counter	
10	1	0	1	0	SR	Shift Register	
11	1	0	1	1	ACR	Auxiliary Control Register	
12	1	1	0	0	PCR	Peripheral Control Register	
13	1	1	0	1	IFR	Interrupt Flag Register	
14	1	1	1	0	IER	Interrupt Enable Register	
15	1	1	1	1	ORA/IRA	Output Register B*	Input Register B*

NOTE: *Same as Register 1 except no handshake.

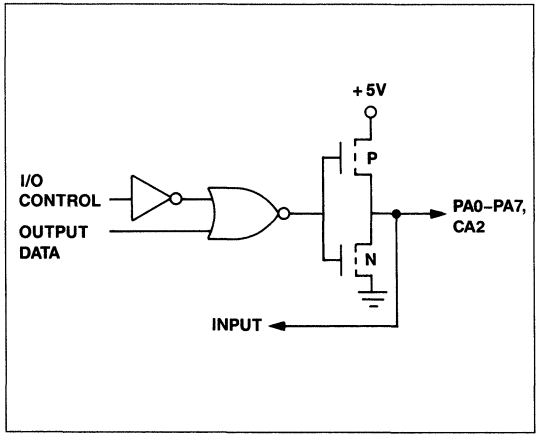


Figure 2. Port A Output Circuit

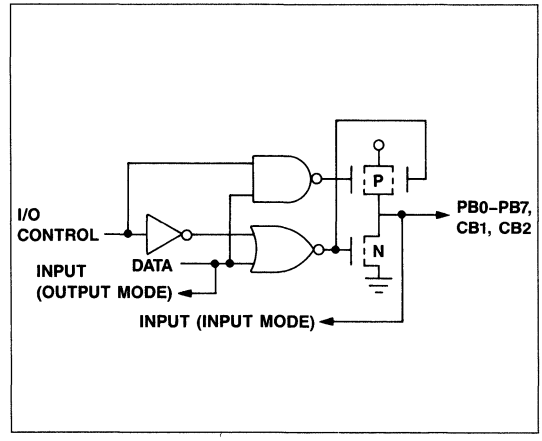


Figure 3. Port B Output Circuit

FUNCTIONAL

The internal org. VIA is illustrated in Figure 4.

PORT A AND

The R65C22 VIA I/O ports (Port A and Port B) and each d control lines.

Each 8-bit periphe ection Register (DDRA, DDRB) for specify eral pins are to act as inputs or outputs. ata Direction Register causes the corresp act as an input. A "1" causes the pin to

Each peripheral pi by a bit in the Output Register (ORA, OR gister (IRA, IRB). When the pin is progra the voltage on the pin is controlled by the cor the Output Register. A "1" in the Output Registe ie output to go high, and a "0" causes the output to go low. Data may be written into Output Register bits corresponding to pins which are programmed as inputs. In this case, however, the output signal is unaffected.

Reading a peripheral port causes the contents of the Input Register (IRA, IRB) to be transferred onto the Data Bus. With input latching disabled, IRA will always reflect the levels on the PA pins. With input latching enabled, IRA will reflect the levels on the PA pins at the time the latching occurred (via CA1).

The IRB register operates similar to the IRA register. However, for pins programmed as outputs there is a difference. When reading IRA, the *level on the pin* determines whether a "0" or a "1" is sensed. When reading IRB, however, the bit stored in the *output register,* ORB, is the bit sensed. Thus, for outputs which have large loading effects and which pull an output "1" down or which pull an output "0" up, reading IRA may result in reading a "0" when a "1" was actually programmed, and reading a "1" when a "0" was programmed. Reading IRB, on the other hand, will read the "1" or "0" level actually programmed, no matter what the loading on the pin.

Figures 5 through 8 illustrate the formats of the port registers. In addition, the input latching modes selected by the Auxiliary Control Register are shown in Figure 14.

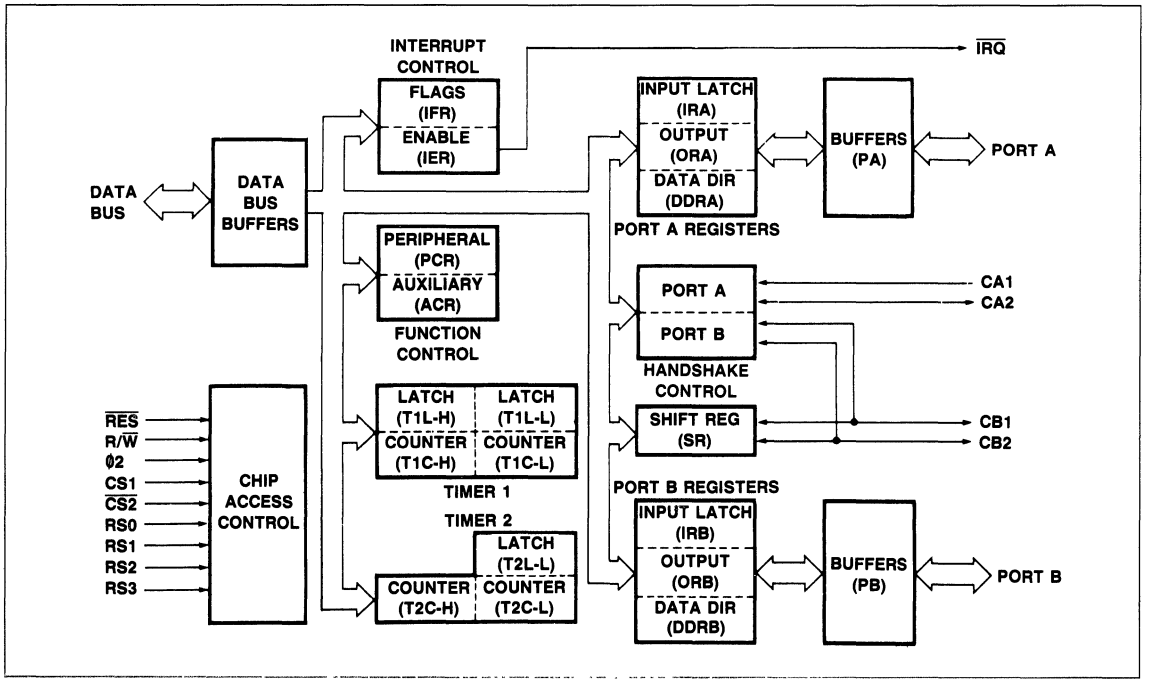


Figure 4. R65C22 VIA Block Diagram

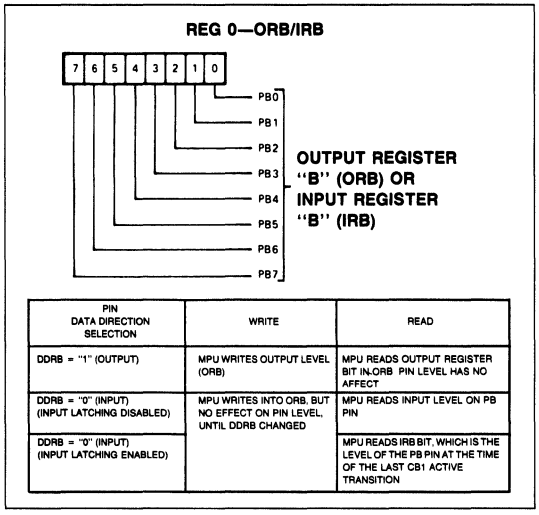
HANDSHAKE CONTROL OF DATA TRANSFERS

The R65C22 allows positive control of data transfers between the system processor and peripheral devices through the operation of "handshake" lines. Port A lines (CA1, CA2) handshake data on both a read and a write operation while the Port B lines (CB1, CB2) handshake on a write operation only.

Read Handshake

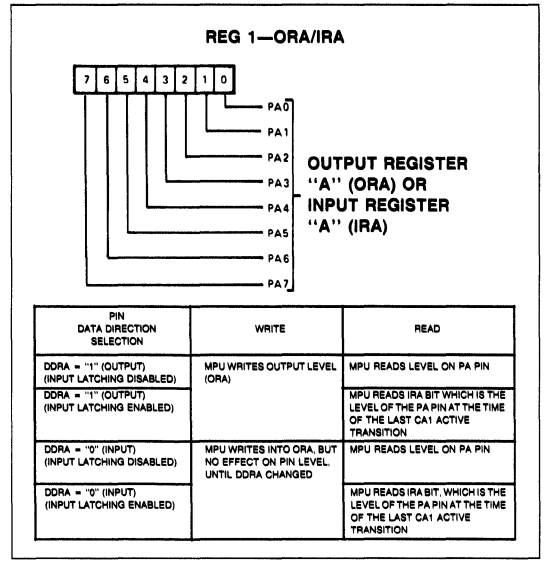
Positive control of data transfers from peripheral devices into the system processor can be accomplished very effectively using Read Handshaking. In this case, the peripheral device must generate the equivalent of a "Data Ready" signal to the processor signifying that valid data is present on the peripheral port. This signal normally interrupts the processor, which then reads the data, causing generation of a "Data Taken" signal. The peripheral device responds by making new data available. This process continues until the data transfer is complete.

In the R65C22, automatic "Read" Handshaking is possible on the Peripheral A port only. The CA1 interrupt input pin accepts the "Data Ready" signal and CA2 generates the "Data Taken" signal. The "Data Ready" signal will set an internal flag which may interrupt the processor or which may be polled under program control. The "Data Taken" signal can either be a pulse or a level which is set low by the system processor and is cleared by the "Data Ready" signal. These options are shown in Figure 9 which illustrates the normal Read Handshake sequence.



PIN DATA DIRECTION SELECTION	WRITE	READ
DDRB = "1" (OUTPUT)	MPU WRITES OUTPUT LEVEL (ORB)	MPU READS OUTPUT REGISTER BIT IN ORB. PIN LEVEL HAS NO AFFECT
DDRB = "0" (INPUT) (INPUT LATCHING DISABLED)	MPU WRITES INTO ORB, BUT NO EFFECT ON PIN LEVEL, UNTIL DDRB CHANGED	MPU READS INPUT LEVEL ON PB PIN
DDRB = "0" (INPUT) (INPUT LATCHING ENABLED)		MPU READS IRB BIT, WHICH IS THE LEVEL OF THE PB PIN AT THE TIME OF THE LAST CB1 ACTIVE TRANSITION

Figure 5. Output Register B (ORB), Input Register B (IRB)



PIN DATA DIRECTION SELECTION	WRITE	READ
DDRA = "1" (OUTPUT) (INPUT LATCHING DISABLED)	MPU WRITES OUTPUT LEVEL (ORA)	MPU READS LEVEL ON PA PIN
DDRA = "1" (OUTPUT) (INPUT LATCHING ENABLED)		MPU READS IRA BIT WHICH IS THE LEVEL OF THE PA PIN AT THE TIME OF THE LAST CA1 ACTIVE TRANSITION
DDRA = "0" (INPUT) (INPUT LATCHING DISABLED)	MPU WRITES INTO ORA, BUT NO EFFECT ON PIN LEVEL, UNTIL DDRA CHANGED	MPU READS LEVEL ON PA PIN
DDRA = "0" (INPUT) (INPUT LATCHING ENABLED)		MPU READS IRA BIT, WHICH IS THE LEVEL OF THE PA PIN AT THE TIME OF THE LAST CA1 ACTIVE TRANSITION

Figure 6. Output Register A (ORA), Input Register A (IRA)

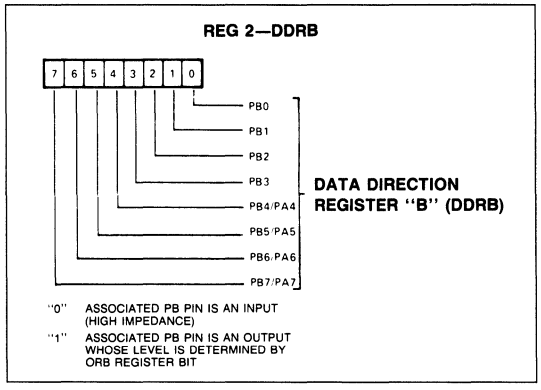


Figure 7. Data Direction Register B (DDRB)

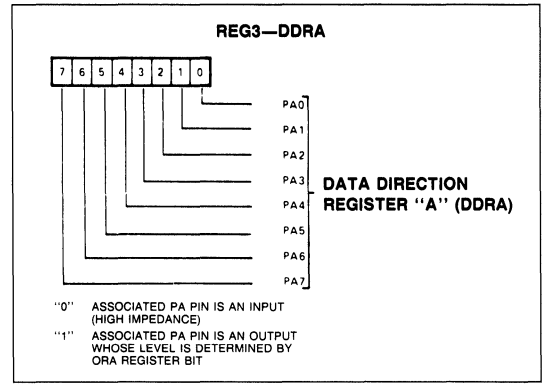


Figure 8. Data Direction Register A (DDRA)

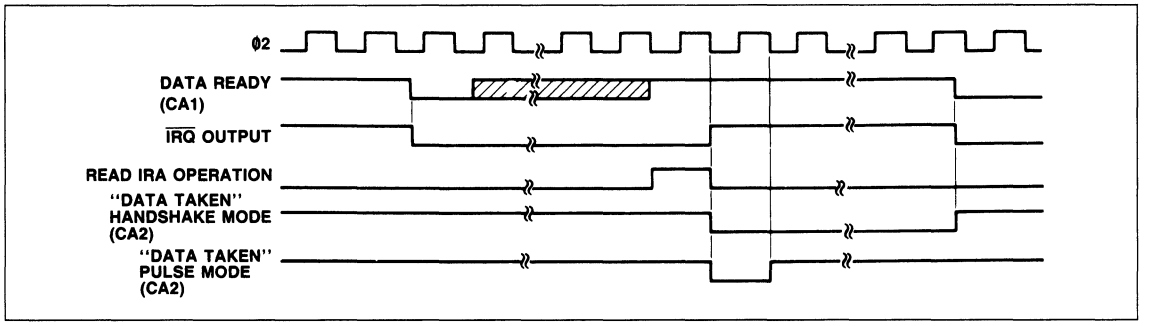


Figure 9. Read Handshake Timing (Port A Only)

Write Handshake

The sequence of operations which allows handshaking data from the system processor to a peripheral device is very similar to that described for Read Handshaking. However, for Write Handshaking, the R65C22 generates the "Data Ready" signal and the peripheral device must respond with the "Data Taken" signal. This can be accomplished on both the PA port and the PB port on the R65C22. CA2 or CB2 act as a "Data Ready" output in either the handshake mode or pulse mode and CA1 or CB1 accept the "Data Taken" signal from the peripheral device, setting the interrupt flag and clearing the "Data Ready" output. This sequence is shown in Figure 10.

Selection of operating modes for CA1, CA2, CB1, and CB2 is accomplished by the Peripheral Control Register (Figure 11).

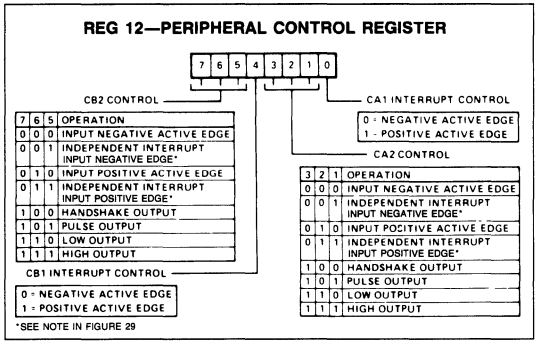


Figure 11. Peripheral Control Register (PCR)

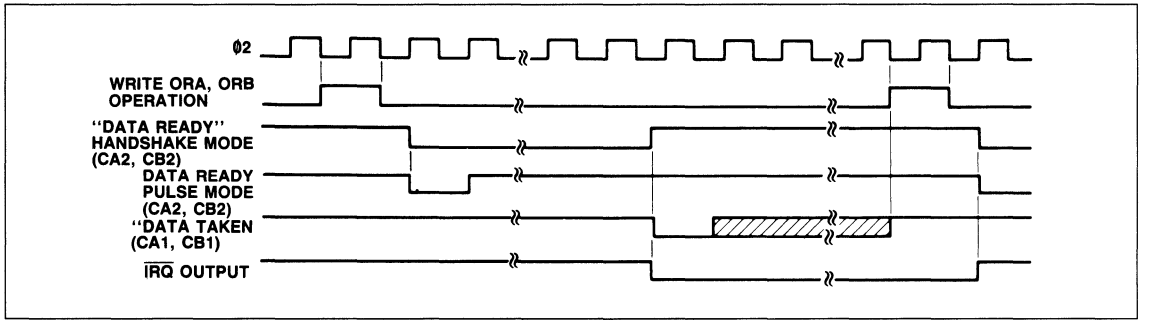


Figure 10. Write Handshake Timing

COUNTER/TIMERS

There are two independent 16-bit counter/timers (called Timer 1 and Timer 2) in the R65C22. Each timer is controlled by writing bits into the Auxiliary Control Register (ACR) to select the mode of operation (Figure 14).

Timer 1 Operation

Interval Timer T1 consists of two 8-bit latches (Figure 12) and a 16-bit counter (Figure 13). The latches store data which is to be loaded into the counter. After loading, the counter decrements at Ø2 clock rate. Upon reaching zero, an interrupt flag is set, and IRQ goes low if the T1 interrupt is enabled. Timer 1 then disables any further interrupts and automatically transfers the contents of the latches into the counter and continues to decrement. In addition, the timer may be programmed to invert the output signal on peripheral pin PB7 each time it "times-out". Each of these modes is discussed separately below.

Note that the processor does not write directly into the low-order counter (T1C-L). Instead, this half of the counter is loaded automatically from the low order latch (T1L-L) when the processor writes into the high order counter (T1C-H). In fact, it may not be necessary to write to the low order counter in some applications since the timing operation is triggered by writing to the high order latch.

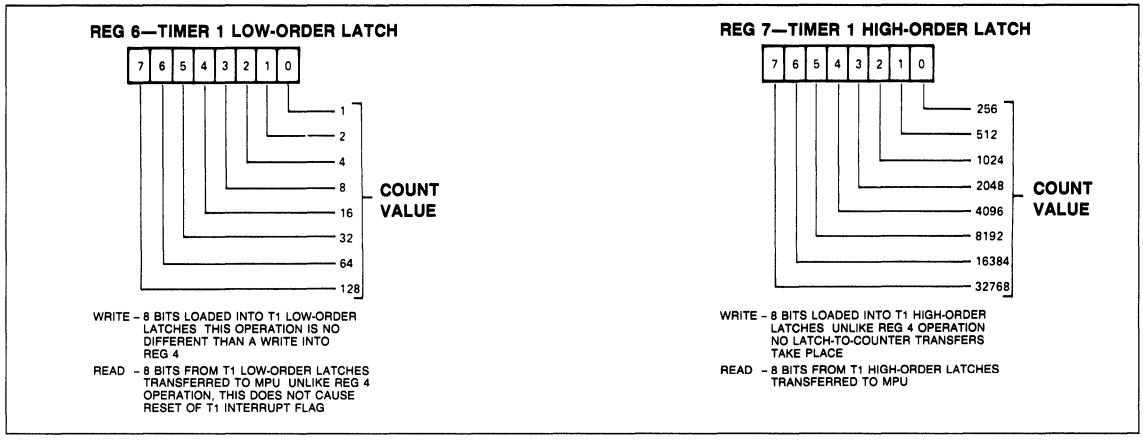


Figure 12. Timer 1 (T1) Latch Registers

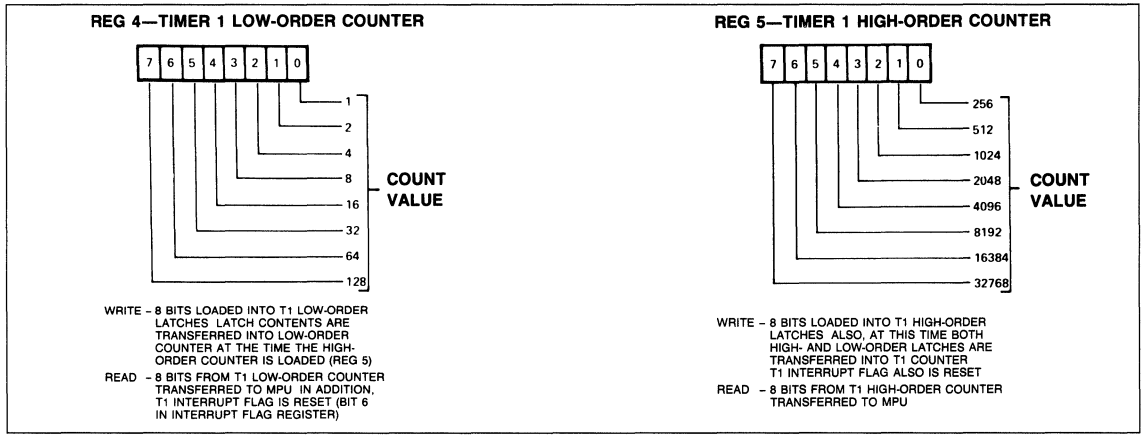


Figure 13. Timer 1 (T1) Counter Registers

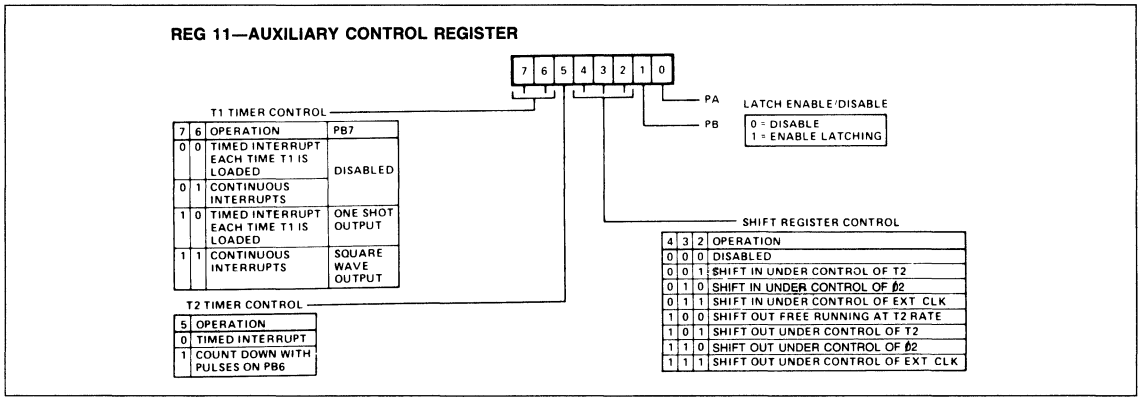


Figure 14. Auxiliary Control Register (ACR)

Timer 1 One-Shot Mode

The Timer 1 one-shot mode generates a single interrupt for each timer load operation. As with any interval timer, the delay between the "write T1C-H" operation and generation of the processor interrupt is a direct function of the data loaded into the timing counter. In addition to generating a single interrupt, Timer 1 can be programmed to produce a single negative pulse on the PB7 peripheral pin. With the output enabled (ACR7 = 1) a "write T1C-H" operation will cause PB7 to go low. PB7 will return high when Timer 1 times out. The result is a single programmable width pulse.

Timing for the R65C22 interval timer one-shot modes is shown in Figure 15.

In the one-shot mode, writing into the T1L-H has no effect on the operation of Timer 1. However, it will be necessary to assure that the low order latch contains the proper data before initiating the count-down with a "write T1C-H" operation. When the processor writes into the high order counter (T1C-H), the T1 interrupt flag will be cleared, the contents of the low order latch will be transferred into the low order counter, and the timer will begin to decrement at system clock rate. If the PB7 output is enabled, this signal will go low on the Ø2 following the write operation. When the counter reaches zero, the T1 interrupt flag will be set, the $\overline{IRQ}$ pin will go low (interrupt enabled), and the signal on PB7 will go high. At this time the counter will continue to decrement at system clock rate. This allows the system processor to read the contents of the counter to determine the time since interrupt. However, the T1 interrupt flag cannot be set again unless it has been cleared as described in this specification.

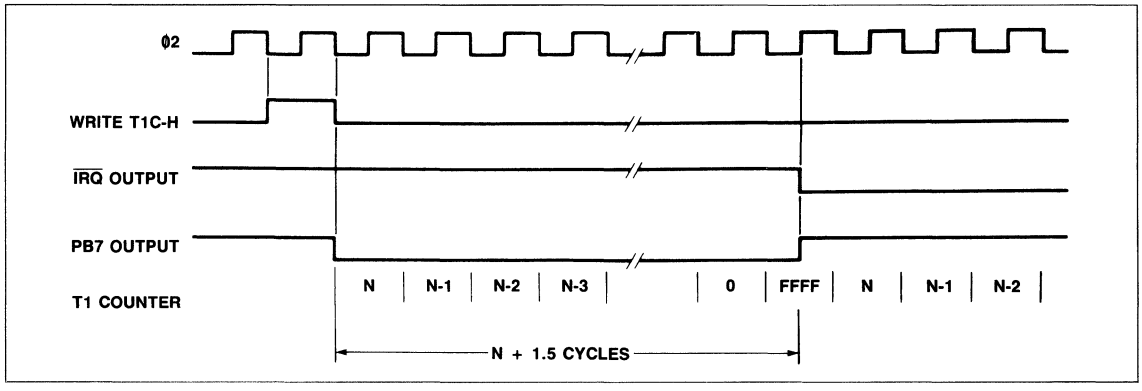


Figure 15. Timer 1 One-Shot Mode Timing

Timer 1 Free-Run Mode

The most important advantage associated with the latches in T1 is the ability to produce a continuous series of evenly spaced interrupts and the ability to produce a square wave on PB7 whose frequency is not affected by variations in the processor interrupt response time. This is accomplished in the "free-running" mode.

In the free-running mode, the interrupt flag is set and the signal on PB7 is inverted each time the counter reaches zero at which time the timer automatically transfers the contents of the latch into the counter (16 bits) and continues to decrement from there. The interrupt flag can be cleared by writing T1C-H, by reading T1C-L, or by writing directly into the flag as described later. However, it is not necessary to rewrite the timer to enable setting the interrupt flag on the next time-out.

All interval timers in the R65C22 are "re-triggerable". Rewriting the counter will always re-initialize the time-out period. In fact, the time-out can be prevented completely if the processor continues to rewrite the timer before it reaches zero. Timer 1 will operate in this manner if the processor writes into the high order counter (T1C-H). However, by loading the latches only, the processor can access the timer during each down-counting operation without affecting the time-out in process. Instead, the data loaded into the latches will determine the length of the next time-out period. This capability is particularly valuable in the free-running mode with the output enabled. In this mode, the signal on PB7 is inverted and the interrupt flag is set with each time-out. By responding to the interrupts with new data for the latches, the processor can determine the period of the next half cycle during each half cycle of the output signal on PB7. In this manner, very complex waveforms can be generated.

A precaution to take in the use of PB7 as the timer output concerns the Data Direction Register contents for PB7. *Both* DDRB bit 7 and ACR bit 7 must be 1 for PB7 to function as the timer output. If one is 1 and other is 0, then PB7 functions as a normal outpin pin, controlled by ORB bit 7.

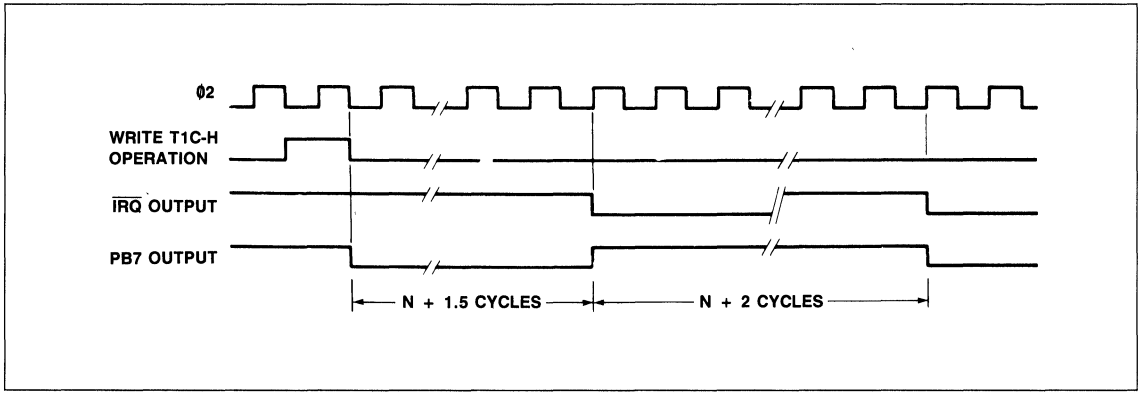


Figure 16. Timer 1 Free-Run Mode Timing

Timer 2 Operation

Timer 2 operates as an interval timer in the "one-slot" mode only), or as a counter for counting negative pulses on the PB6 peripheral pin. A single control bit in the Auxiliary Control Register selects between these two modes. This timer is comprised of a "write-only" lower-order latch (T2L-L), a "read-only" low-order counter (T2C-L) and a read/write high order counter (T2C-H). The counter registers act as a 16-bit counter which decrements at Φ2 rate. Figure 17 illustrates the T2 Latch/Counter Registers.

Timer 2 One-Shot Mode

As an interval timer, T2 operates in the "one-shot" mode similar to Timer 1. In this mode, T2 provides a single interrupt for each "write T2C-H" operation. After timing out, the counter will continue to decrement. However, setting of the interrupt flag is disabled after initial time-out so that it will not be set by the counter decrementing again through zero. The processor must rewrite T2C-H to enable setting of the interrupt flag. The interrupt flag is cleared by reading T2C-L or by writing T2C-H. Timing for this operation is shown in Figure 18.

Timer 2 Pulse Counting Mode

In the pulse counting mode, T2 counts a predetermined number of negative-going pulses on PB6. This is accomplished by first loading a number into T2. Writing into T2C-H clears the interrupt flag and allows the counter to decrement each time a pulse is applied to PB6. The interrupt flag is set when T2 counts down past zero. The counter will then continue to decrement with each pulse on PB6. However, it is necessary to rewrite T2C-H to allow the interrupt flag to set on a subsequent time-out. Timing for this mode is shown in Figure 19. The pulse must be low on the leading edge of Φ2.

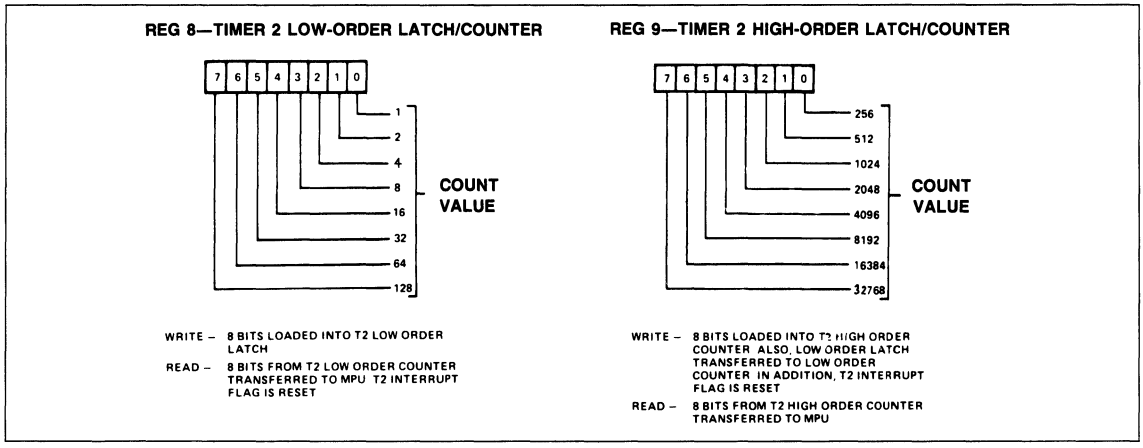


Figure 17. Timer 2 (T2) Latch/Counter Registers

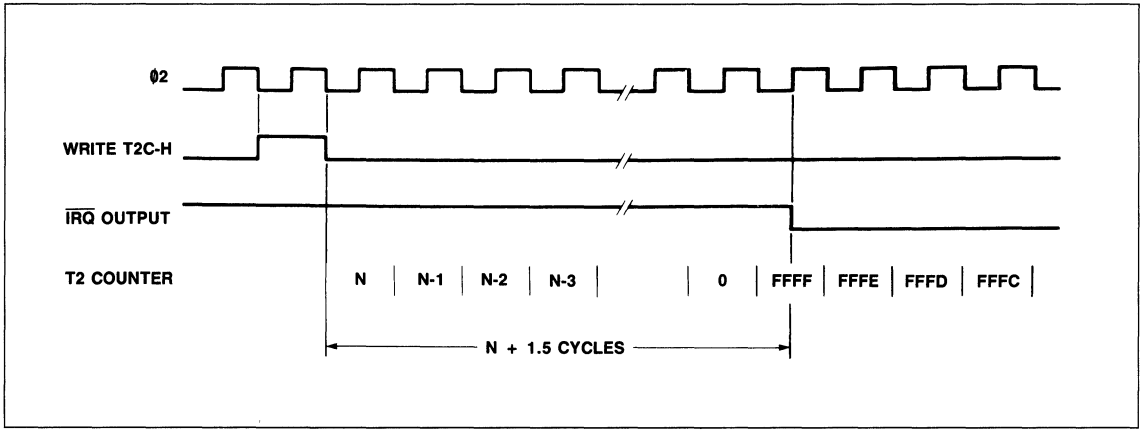


Figure 18. Timer 2 One-Shot Mode Timing

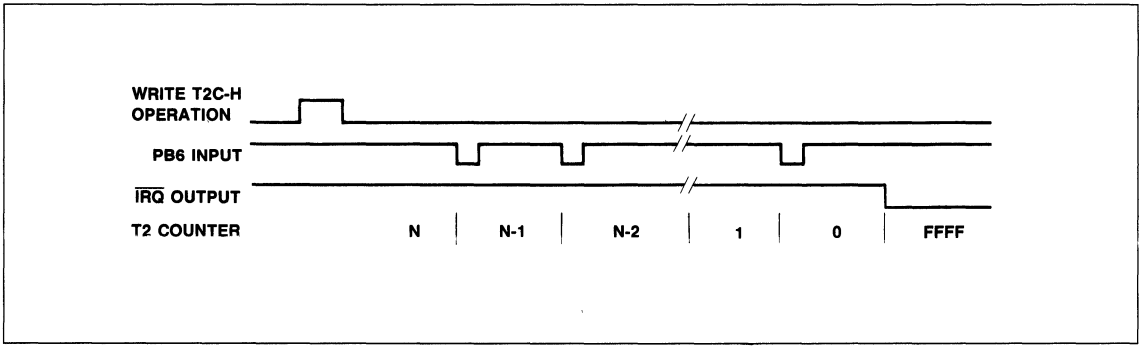


Figure 19. Timer 2 Pulse Counting Mode

SHIFT REGISTER OPERATION

The Shift Register (SR) performs serial data transfers into and out of the CB2 pin under control of an internal modulo-8 counter. Shift pulses can be applied to the CB1 pin from an external source or, with the proper mode selection, shift pulses generated internally will appear on the CB1 pin for controlling external devices.

The control bits which select the various shift register operating modes are located in the Auxiliary Control Register. Figure 20 illustrates the configuration of the SR data bits and Figure 21 shows the SR control bits of the ACR.

SR Mode 0 — Disabled

Mode 0 disables the Shift Register. In this mode the microprocessor can write or read the SR and the SR will shift on each CB1 positive edge shifting in the value on CB2. In this mode the SR interrupt Flag is disabled (held to a logic 0).

SR Mode 1 — Shift In Under Control of T2

In mode 1, the shifting rate is controlled by the low order 8 bits of T2 (Figure 22). Shift pulses are generated on the CB1 pin to control shifting in external devices. The time between transitions of this output clock is a function of the system clock period and the contents of the low order T2 latch (N).

The shifting operation is triggered by the read or write of the SR if the SR flag is set in the IFR. Otherwise the first shift will occur at the next time-out of T2 after a read or write of the SR. Data is shifted first into the low order bit of SR and is then shifted into the next higher order bit of the shift register on the negative-going edge of each clock pulse. The input data should change before the positive-going edge of CB1 clock pulse. This data is shifted into the shift register during the Ø2 clock cycle following the positive-going edge of the CB1 clock pulse. After 8 CB1 clock pulses, the shift register interrupt flag will set and $\overline{IRQ}$ will go low.

SR Mode 2 — Shift In Under Ø2 Control

In mode 2, the shift rate is a direct function of the system clock frequency (Figure 23). CB1 becomes an output which generates shift pulses for controlling external devices. Timer 2 operates as an independent interval timer and has no effect on SR. The shifting operation is triggered by reading or writing the Shift Register. Data is shifted, first into bit 0 and is then shifted into the next higher order bit of the shift register on the trailng edge of each Ø2 clock pulse. After 8 clock pulses, the shift register interrupt flag will be set, and the output clock pulses on CB1 will stop.

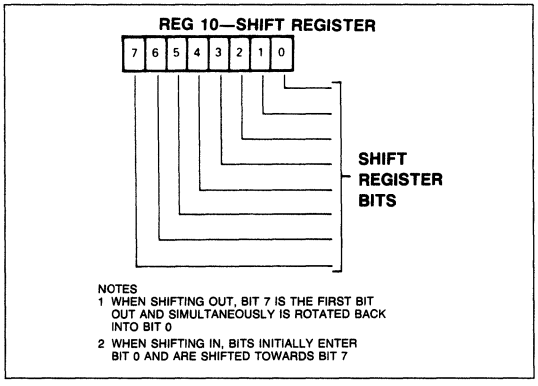
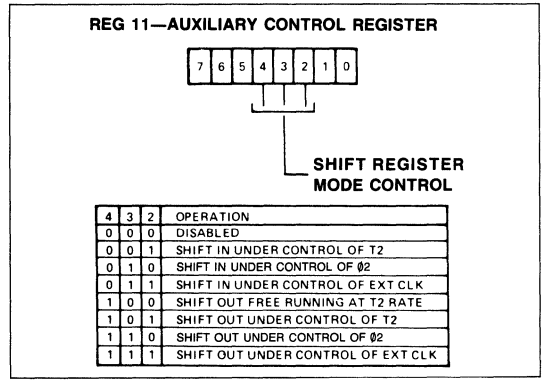


Figure 20. Shift Registers



4	3	2	OPERATION
0	0	0	DISABLED
0	0	1	SHIFT IN UNDER CONTROL OF T2
0	1	0	SHIFT IN UNDER CONTROL OF Ø2
0	1	1	SHIFT IN UNDER CONTROL OF EXT CLK
1	0	0	SHIFT OUT FREE RUNNING AT T2 RATE
1	0	1	SHIFT OUT UNDER CONTROL OF T2
1	1	0	SHIFT OUT UNDER CONTROL OF Ø2
1	1	1	SHIFT OUT UNDER CONTROL OF EXT CLK

Figure 21. Shift Register Modes

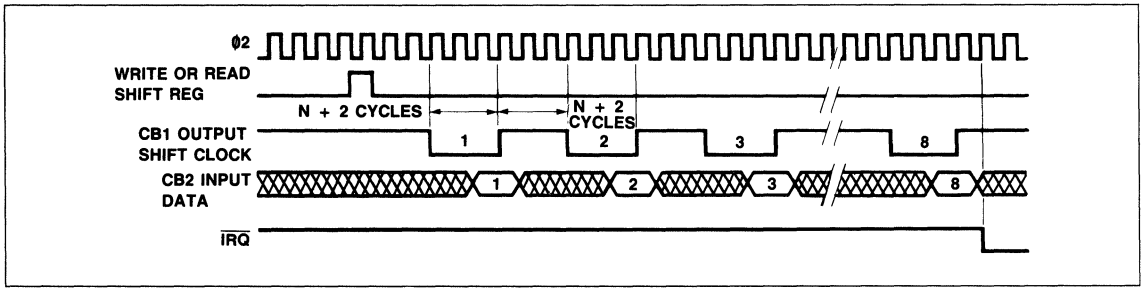


Figure 22. SR Mode 1 — Shift In Under T2 Control

SR Mode 3 — Shift in Under CB1 Control

In mode 3, external pin CB1 becomes an input (Figure 24). This allows an external device to load the shift register at its own pace. The shift register counter will interrupt the processor each time 8 bits have been shifted in. The shift register stops after 8 counts and must be reset to start again. Reading or writing the Shift Register resets the Interrupt Flag and initializes the SR counter to count another 8 pulses.

Note that the data is shifted during the first system clock cycle following the positive-going edge of the CB1 shift pulse. For this reason, data must be held stable during the first full cycle following CB1 going high.

SR Mode 4 — Shift Out Under T2 Control (Free-Run)

Mode 4 is very similar to mode 5 in which the shifting rate is set by T2. However, in mode 4 the SR Counter does not stop the shifting operation (Figure 25). Since the Shift Register bit 7 (SR7) is recirculated back into bit 0, the 8 bits loaded into the shift register will be clocked onto CB2 repetitively. In this mode the shift register counter is disabled.

SR Mode 5 — Shift Out Under T2 Control

In mode 5, the shift rate is controlled by T2 (as in mode 4). The shifting operation is triggered by the read or write of the SR if the SR flag is set in the IFR (Figure 26). Otherwise the first shift will occur at the next time-out of T2 after a read or write of the SR. However, with each read or write of the shift register the SR Counter is reset and 8 bits are shifted onto CB2. At the same time, 8 shift pulses are generated on CB1 to control shifting in external devices. After the 8 shift pulses, the shifting is disabled, the SR Interrupt Flag is set and CB2 remains at the last data level.

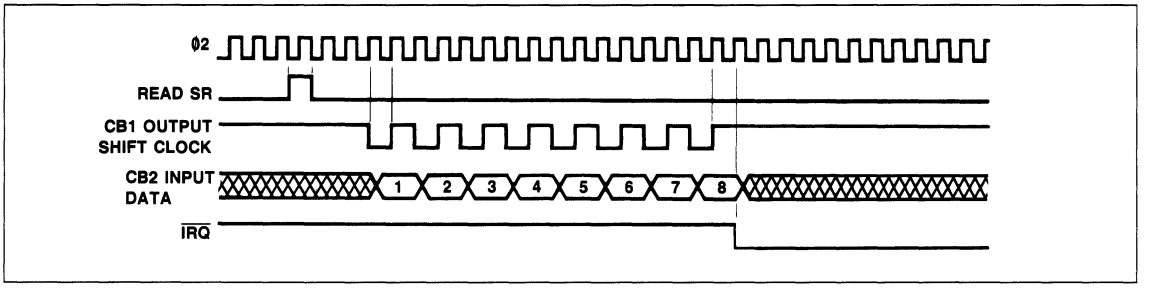


Figure 23. SR Mode 2 — Shift In Under Φ2 Control

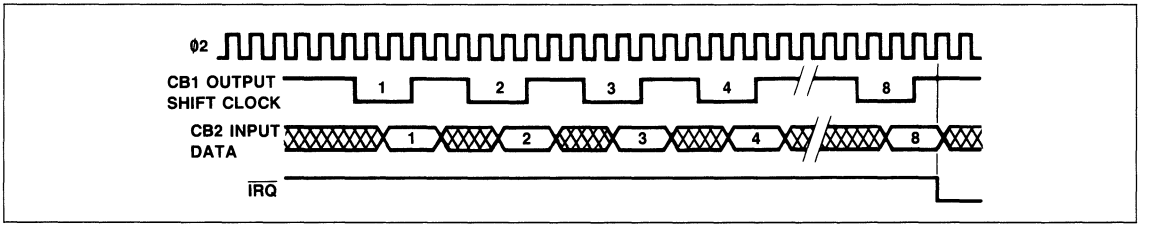


Figure 24. SR Mode 3 — Shift In Under CB1 Control

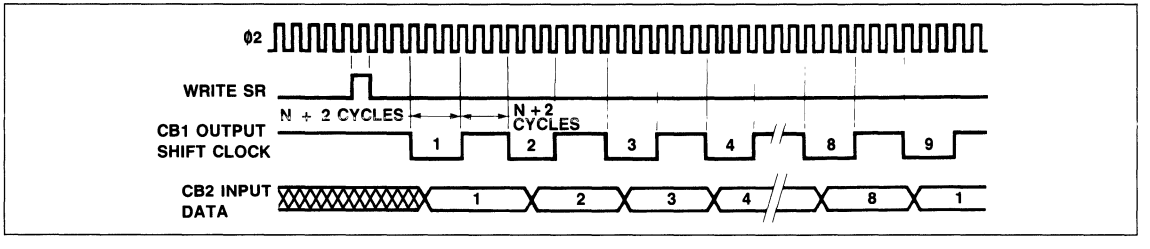


Figure 25. SR Mode 4 — Shift Our Under T2 Control (Free-Run)

SR Mode 6 — Shift Out Under Ø2 Control

In mode 6, the shift rate is controlled by the Ø2 system clock (Figure 27).

SR Mode 7 — Shift Out Under CB1 Control

In mode 7, shifting is controlled by pulses applied to the CB1 pin by an external device (Figure 28). The SR counter sets the SR Interrupt Flag each time it counts 8 pulses but it does not disable the shifting function. Each time the microprocessor, writes or reads the shift register, the SR Interrupt Flag is reset and the SR counter is initialized to begin counting the next 8 shift pulses on pin CB1. After 8 shift pulses, the Interrupt Flag is set. The microprocessor can then load the shift register with the next byte of data.

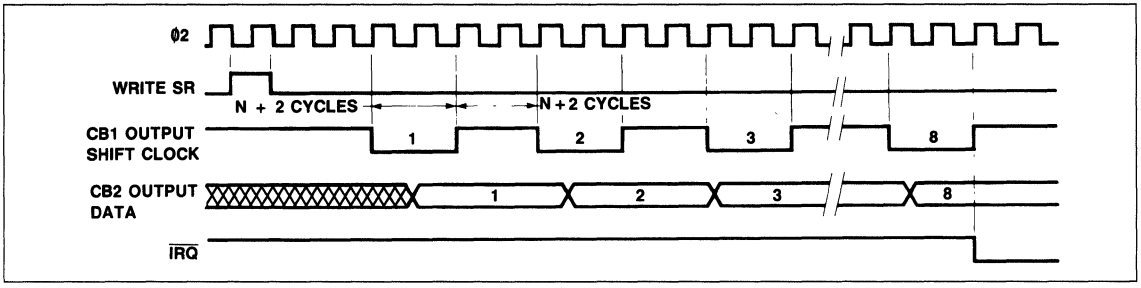


Figure 26. SR Mode 5 — Shift Out Under T2 Control

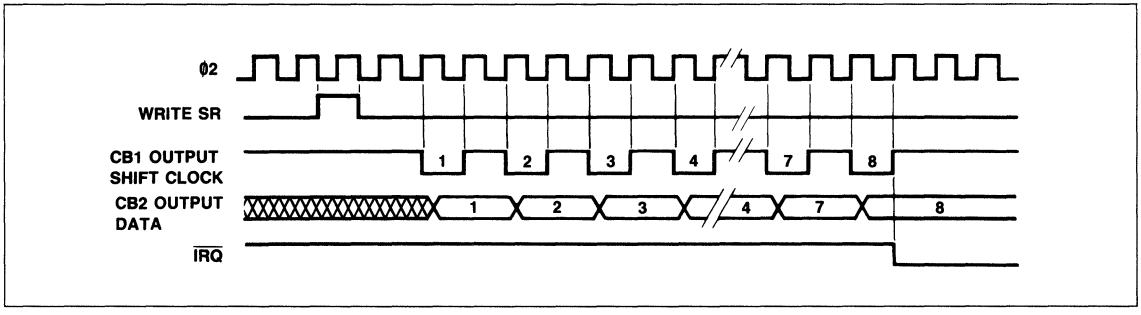


Figure 27. SR Mode 6 — Shift Out Under Ø2 Control

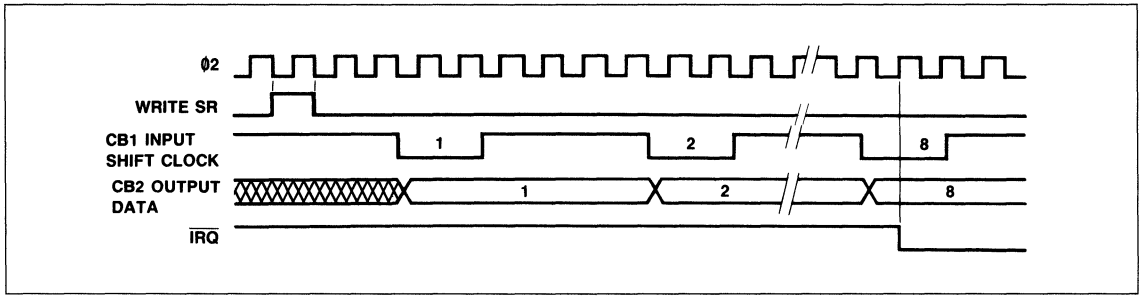


Figure 28. SR Mode 7 — Shift Out Under CB1 Control

Interrupt Operation

Controlling interrupts within the R65C22 involves three principal operations. These are flagging the interrupts, enabling interrupts and signaling to the processor that an active interrupts exists within the chip. Interrupt flags are set in the Interrupt Flag Register (IFR) by conditions detected within the R65C22 or on inputs to the R65C22. These flags normally remain set until the interrupt has been serviced. To determine the source of an interrupt, the microprocessor must examine these flags in order, from highest to lowest priority.

Associated with each interrupt flag is an interrupt enable bit in the Interrupt Enable Register (IER). This can be set or cleared by the processor to enable interrupting the processor from the corresponding interrupt flag. If an interrupt flag is set to a logic 1 by an interrupting condition, and the corresponding interrupt enable bit is set to a 1, the Interrupt Request Output ($\overline{IRQ}$) will go low. $\overline{IRQ}$ is an "open-collector" output which can be "wire-OR'ed" with other devices in the system to interrupt the processor.

Interrupt Flag Register (IRF)

In the R65C22, all the interrupt flags are contained in one register, i.e., the IFR (Figure 29). In addition, bit 7 of this register will be read as a logic 1 when an interrupt exists within the chip. This allows very convenient polling of several devices within a system to locate the source of an interrupt.

The Interrupt Flag Register (IRF) may be read directly by the processor. In addition, individual flag bits may be cleared by writing a "1" into the appropriate bit of the IFR. When the proper chip select and register signals are applied to the chip, the contents of this register are placed on the data bus. Bit 7 indicates the status of the $\overline{IRQ}$ output. This bit corresponds to the logic function: $\overline{IRQ}$ = IFR6 × IER6 + IFR5 × IER5 + IFR4 × IER4 + IFR3 × IER3 + IFR2 × IER2 + IFR1 × IER1 + IFR0 × IER0.

Note:

× = logic AND, + = Logic OR.

The IFR bit 7 is not a flag. Therefore, this bit is not directly cleared by writing a logic 1 into it. It can only be cleared by clearing all the flags in the register or by disabling all the active interrupts as discussed in the next section.

Interrupt Enable Register (IER)

For each interrupt flag in IFR, there is a corresponding bit in the Interrupt Enable Register (IER) (Figure 30). Individual bits in the IER can be set or cleared to facilitate controlling individual interrupts without affecting others. This is accomplished by writing to the (IER) after bit 7 set or cleared to, in turn, set or clear selected enable bits. If bit 7 of the data placed on the system data bus during this write operation is a 0, each 1 in bits 6 through 0 clears the corresponding bit in the Interrupt Enable Register. For each zero in bits 6 through 0, the corresponding bit is unaffected.

Selected bits in the IER can be set by writing to the IER with bit 7 in the data word set to a 1. In this case, each 1 in bits 6 through 0 will set the corresponding bit. For each zero, the corresponding bit will be unaffected. This individual control of the setting and clearing operations allows very convenient control of the interrupts during system operation.

In addition to setting and clearing IER bits, the contents of this register can be read at any time. Bit 7 will be read as a logic 1, however.

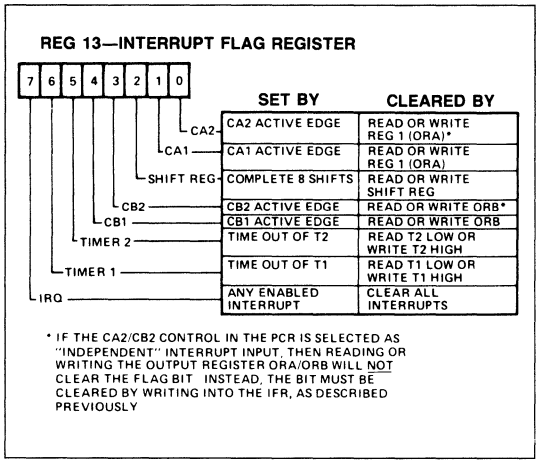


Figure 29. Interrupt Flag Register (IFR)

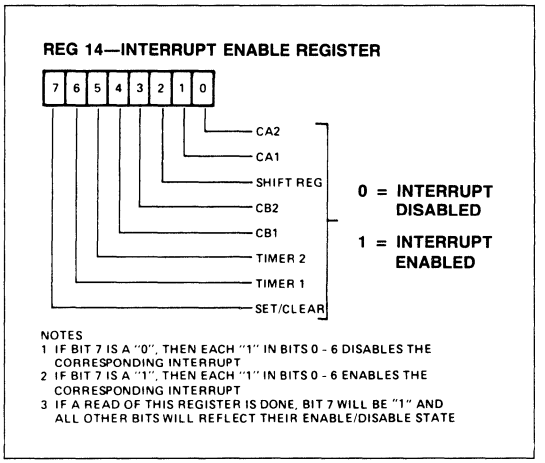


Figure 30. Interrupt Enable Register (IER)

PERIPHERAL INTERFACE CHARACTERISTICS

Symbol	Characteristic	Min.	Max.	Unit	Figure
t_r, t_f	Rise and Fall Time for CA1, CB1, CA2 and CB2 Input Signals	—	1.0	μs	—
t_{CA2}	Delay Time, Clock Negative Transition to CA2 Negative Transition (read handshake or pulse mode)	—	1.0	μs	31a, 31b
t_{RS1}	Delay Time, Clock Negative Transition to CA2 Positive Transition (pulse mode)	—	1.0	μs	31a
t_{RS2}	Delay Time, CA1 Active Transition to CA2 Positive Transition (handshake mode)	—	2.0	μs	31b
t_{WHS}	Delay Time, Clock Positive Transition to CA2 or CB2 Negative Transition (write handshake)	0.05	1.0	μs	31c, 31d
t_{DS}	Delay Time, Periphral Data Valid to CB2 Negative Transition	0.20	1.5	μs	31c, 31d
t_{RS3}	Delay Time, Clock Positive Transition to CA2 or CB2 Positive Transition (pulse mode)	—	1.0	μs	31c
t_{RS4}	Delay Time, CA1 or CB1 Active Transition to CA2 or CB2 Positive Transition (handshake mode)	—	2.0	μs	31d
t_{21}	Delay Time Required from CA2 Output to CA1 Active Transition (handshake mode)	400	—	ns	31d
t_{IL}	Setup Time, Peripheral Data Valid to CA1 or CB1 Active Transition (input latching)	300	—	ns	31e
t_{AL}	CA1, CB1 Setup Prior to Transition to Arm Latch	300	—	ns	31e
t_{PDH}	Peripheral Data Hold After CA1, CB1 Transition	150	—	ns	31e
t_{SR1}	Shift-Out Delay Time — Time from ϕ_2 Falling Edge to CB2 Data Out	—	300	ns	31f
t_{SR2}	Shift-In Setup Time — Time from CB2 Data In to ϕ_2 Rising Edge	300	—	ns	31g
t_{SR3}	External Shift Clock (CB1) Setup Time Relative to ϕ_2 Trailing Edge	100	T_{CY}	ns	31g
t_{IPW}	Pulse Width — PB6 Input Pulse	2 × T_{CY}	—		31i
t_{ICW}	Pulse Width — CB1 Input Clock	2 × T_{CY}	—		31h
t_{IPS}	Pulse Spacing — PB6 Input Pulse	2 × T_{CY}	—		31i
t_{ICS}	Pulse Spacing — CB1 Input Pulse	2 × T_{CY}	—		31h

Notes:
1. V_{CC} = 5.0 Vdc ±5%
2. T_A = T_L to T_H

PERIPHERAL INTERFACE WAVEFORMS

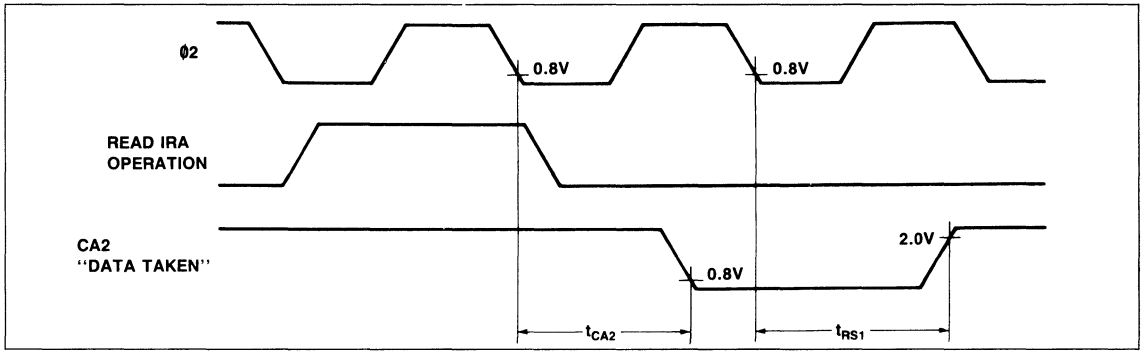


Figure 31a. CA2 Timing for Read Handshake, Pulse Mode

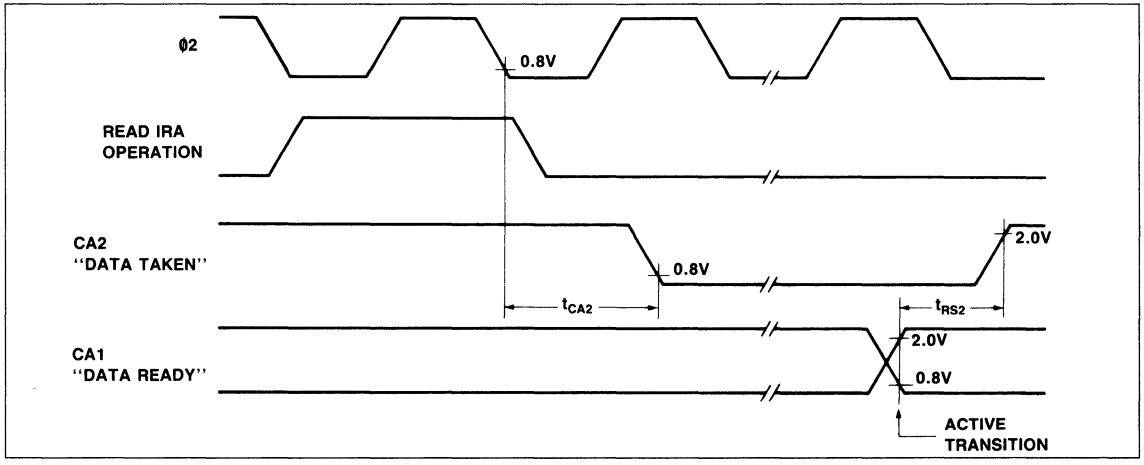


Figure 31b. CA2 Timing for Read Handshake, Handshake Mode

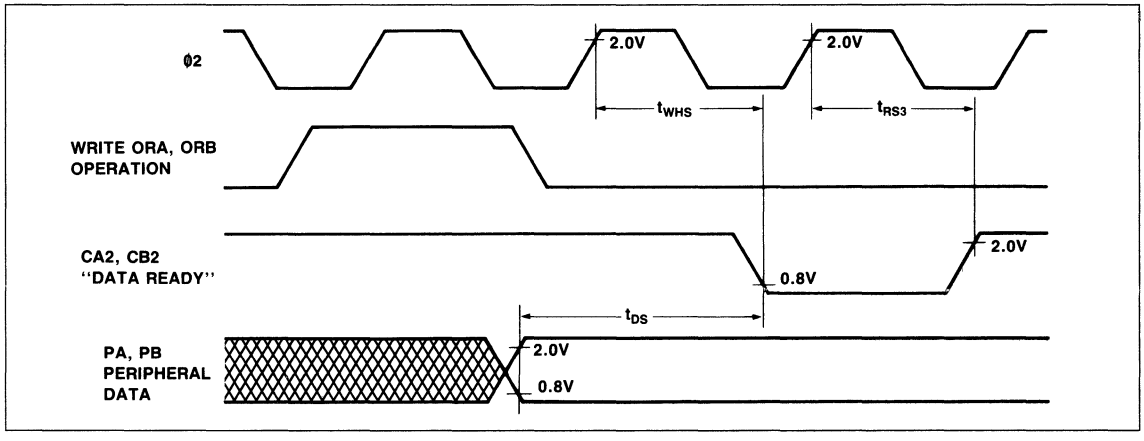


Figure 31c. CA2, CB2 Timing for Write Handshake, Pulse Mode

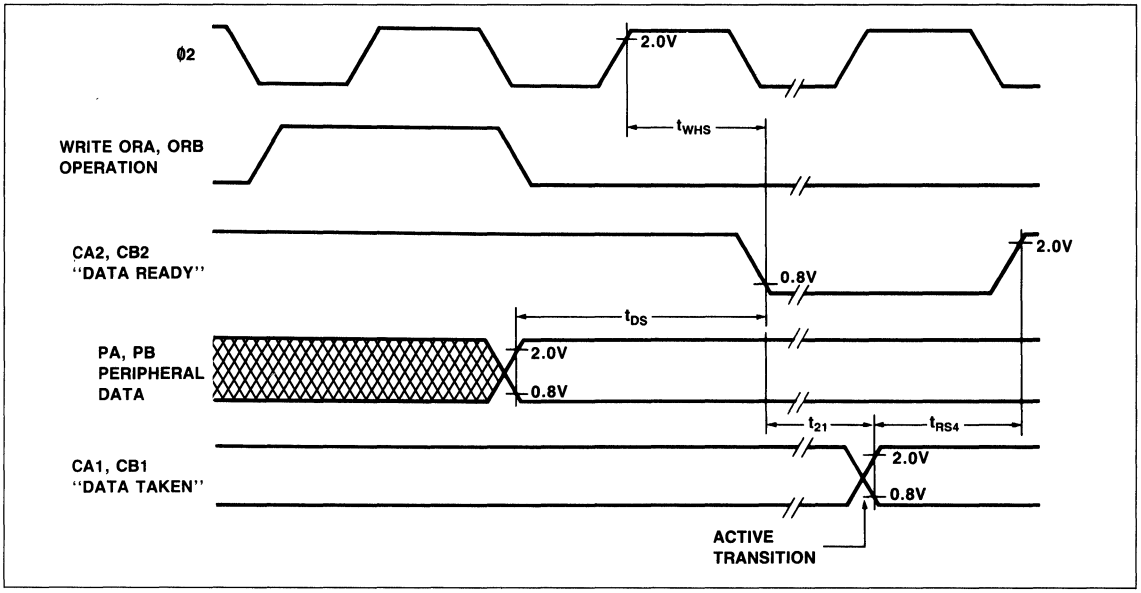


Figure 31d. CA2, CB2 Timing for Write Handshake, Handshake Mode

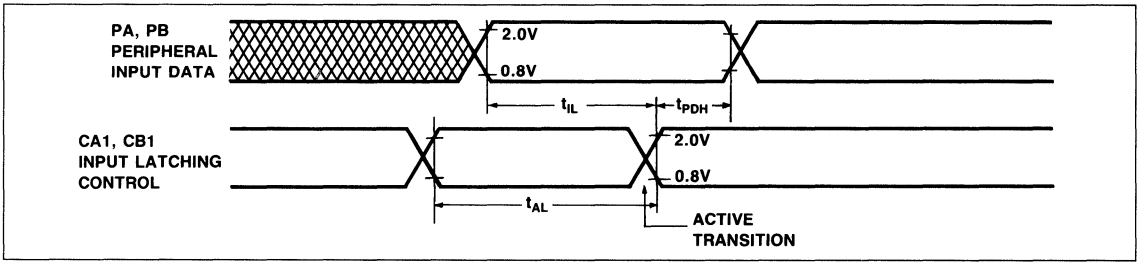


Figure 31e. Peripheral Data Input Latching Timing

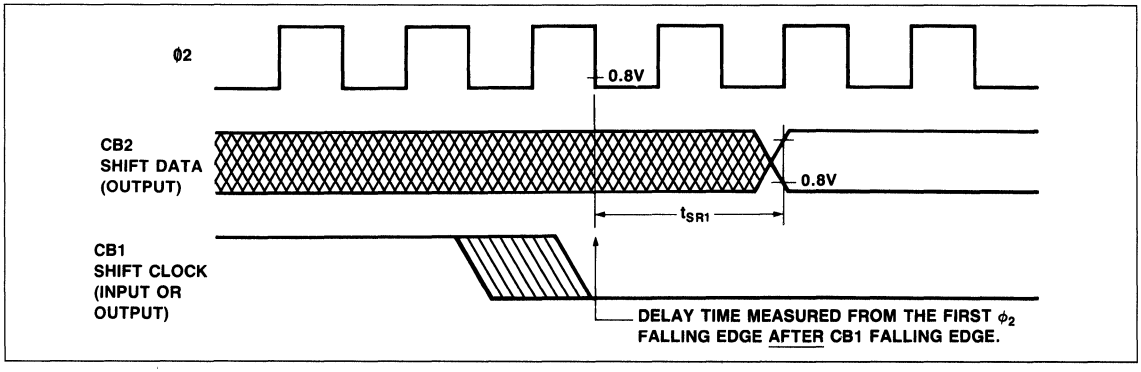


Figure 31f. Timing for Shift Out with Internal or External Shift Clocking

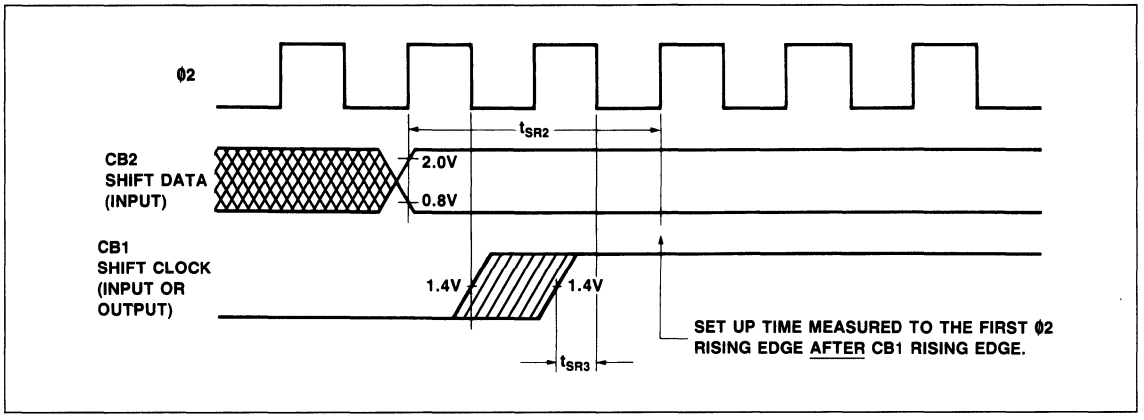


Figure 31g. Timing for Shift In with Internal or External Shift Clocking

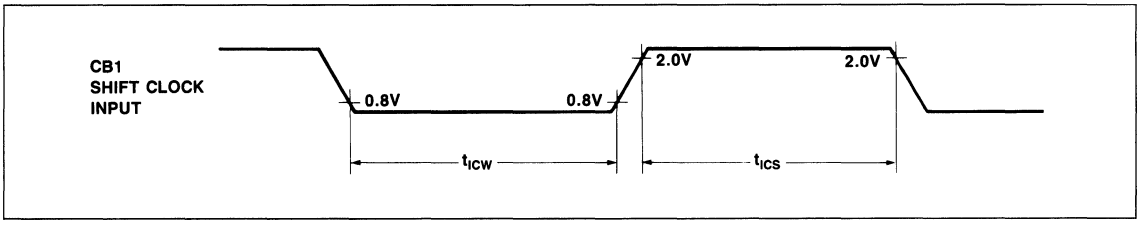


Figure 31h. External Shift Clock Timing

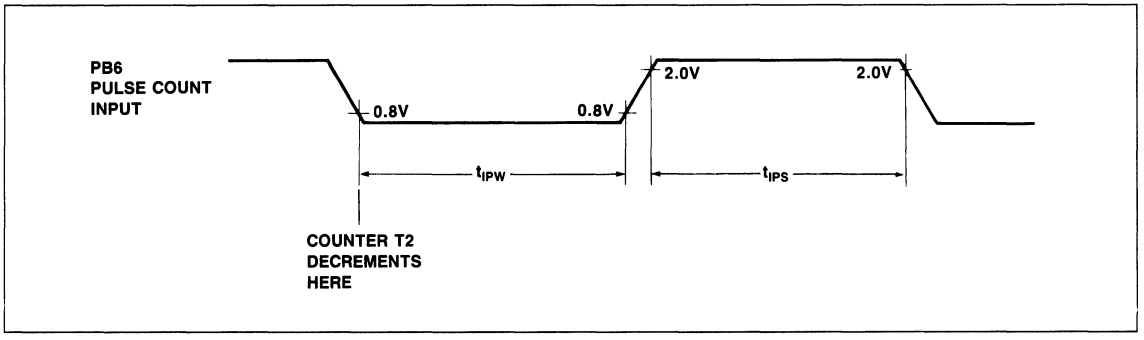


Figure 31i. Pulse Count Input Timing

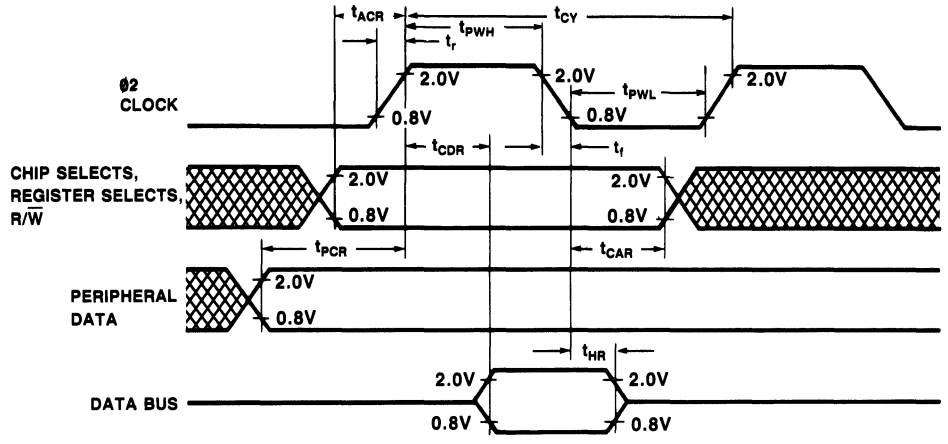
BUS TIMING CHARACTERISTICS

		1 MHz		2 MHz		3 MHz		4 MHz		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
Cycle Time	t_{CY}	1000	—	500	—	330	—	250	—	ns
Phase 2 Pulse Width High	t_{PWH}	470	—	240	—	160	—	120	—	ns
Phase 2 Pulse Width Low	t_{PWL}	470	—	240	—	160	—	120	—	ns
Phase 2 Transition	$t_{R,F}$	—	30	—	30	—	30	—	30	ns
READ TIMING										
Select, R/$\overline{W}$ Setup	t_{ACR}	160	—	90	—	65	—	45	—	ns
Select, R/$\overline{W}$ Hold	t_{CAR}	0	—	0	—	0	—	0	—	ns
Data Bus Delay	t_{CDR}	—	320	—	190	—	130	—	90	ns
Data Bus Hold	t_{HR}	10	—	10	—	10	—	10	—	ns
Peripheral Data Setup	t_{PCR}	300	—	150	—	110	—	75	—	ns
WRITE TIMING										
Select R/$\overline{W}$ Setup	t_{ACW}	160	—	90	—	65	—	45	—	ns
Select, R/$\overline{W}$ Hold	t_{CAW}	0	—	0	—	0	—	0	—	ns
Data Bus Setup	t_{DCW}	195	—	90	—	65	—	45	—	ns
Data Bus Hold	t_{HW}	10	—	10	—	10	—	10	—	ns
Peripheral Data Delay	t_{CPW}	—	1000	—	500	—	330	—	250	ns

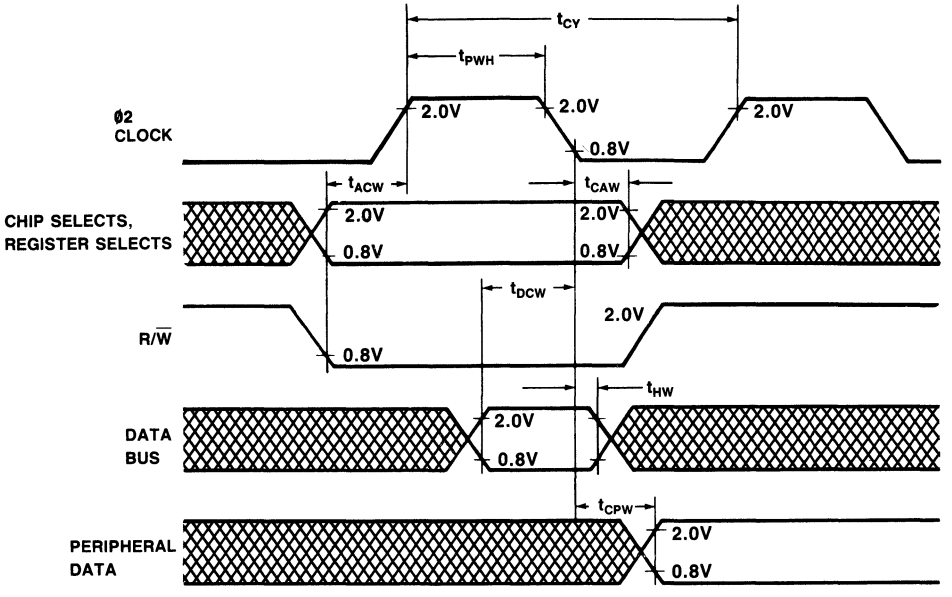
Notes:
1. V_{CC} = 5.0 Vdc ±5%
2. $T_A = T_L$ to T_H

BUS TIMING WAVEFORMS

Read Timing Waveforms



Write Timing Waveforms



ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to −7.0	Vdc
Input Voltage	V_{IN}	−0.3 to +7.0	Vdc
Operating Temperature Commercial Industrial	T_A	 0 to +70 −40 to +85	 °C °C
Storage Temperature	T_{STG}	−55 to +150	°C

*NOTE: Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the other sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING CONDITIONS

Parameter	Symbol	Value
Supply Voltage	V_{CC}	5V ±5%
Temperature Range Commercial	T_A	T_L to T_H 0°C to 70°C

DC CHARACTERISTICS

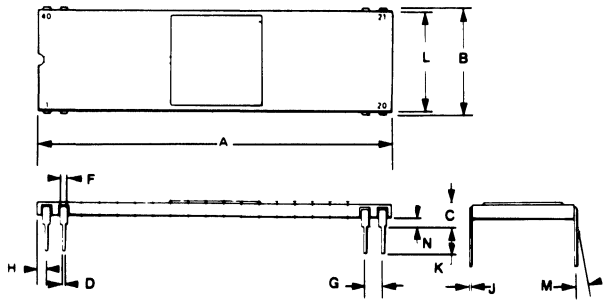
(V_{CC} = 5.0 Vdc ±5%, V_{SS} = 0, T_A = T_L to T_H, unless otherwise noted)

Parameter	Symbol	Min.	Typ.[3]	Max.	Unit[1]	Test Conditions
Input High Voltage	V_{IH}	+2.0	—	V_{CC}	V	
Input Low Voltage	V_{IL}	−0.3	—	+0.8	V	
Input Leakage Current R/W, RES, RS0, RS1, RS2, RS3, CS1, CS2, CA1, Ø2	I_{IN}	—	±1	±2.5	µA	V_{IN} = 0V to V_{CC} V_{CC} = 5.25V
Input Leakage Current for Three-State Off D0–D07	I_{TSI}	—	±2	±10	µA	V_{IN} = 0.4V to 2.4V V_{CC} = 5.25V
Input High Current PA0–PA7, CA2, PB0–PB7, CB1, CBS	I_{IH}	−200	−400	—	µA	V_{IN} = 2.4V
Input Low Current PA0–PA7, CA2, PB0–PB7, CB1, CB2	I_{IL}	—	−2	−3.2	mA	V_{IL} = 0.4V
Output High Voltage All outputs PB0–PB7, CB2 (Darlington Drive)	V_{OH}	 2.4 1.5	 — —	 — —	 V V	V_{CC} = 4.75V I_{LOAD} = 200 µA I_{LOAD}[2] = −3.2 mA
Output Low Voltage	V_{OL}	—	—	+0.4	V	V_{CC} = 4.75V I_{LOAD} = 3.2 mA I_{LOAD} = 1.6 mA
Output High Current (Sourcing) Logic PB0–PB7, CB2 (Darlington Drive)	I_{OH}	 −200 −3.2	 −1500 −6	 — —	 µA mA	 V_{OH} = 2.4V V_{OH} = 1.5V
Output Low Current (Sinking)	I_{OL}	3.2	—	—	mA	V_{OL} = 0.4
Output Leakage Current (Off State) IRQ	I_{OFF}	—	1	±10	µA	V_{OH} = 2.4V V_{CC} = 5.25V
Power Dissipation	P_D	—	7	10	mW/MHz	
Input Capacitance R/W, RES, RS0, RS1, RS2, RS3, CS1, CS2, D0–D7, PA0–PA7, CA1, CA2, PB0–PB7 CB1, CB2, Ø2	C_{IN}	 — — —	 — — —	 10 7 20	 pF pF pF	V_{CC} = 5.0V V_{IN} = 0V f = 2 MHz T_A = 25/C
Output Capacitance	C_{OUT}	—	—	10	pF	

Notes:
1. All units are direct current (DC) except for capacitance.
2. Negative sign indicates outward current flow, positive indicates inward flow.
3. Typical values shown for V_{CC} = 5.0V and T_A = 25°C.

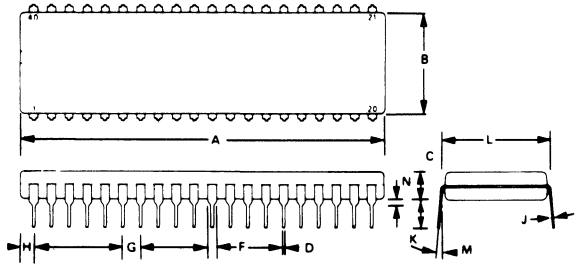
PACKAGE DIMENSIONS

40-PIN CERAMIC DIP



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	50 29	51 31	1 980	2 020
B	14 86	15 62	0 585	0 615
C	2 54	4 19	0 100	0 165
D	0 38	0 53	0 015	0 021
F	0 76	1 40	0 030	0 055
G	2 54 BSC		0 100 BSC	
H	0 76	1 78	0 030	0 070
J	0 20	0 33	0 008	0 013
K	2 54	4 19	0 100	0 165
L	14 60	15 37	0 575	0.605
M	0	10°	0°	10
N	0 51	1 52	0 020	0 060

40-PIN PLASTIC DIP



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	51 28	52 32	2 040	2 060
B	13 72	14 22	0 540	0 560
C	3 55	5 08	0 140	0 200
D	0 36	0 51	0 014	0 020
F	1 02	1 52	0 040	0 060
G	2 54 BSC		0 100 BSC	
H	1 65	2 16	0 065	0 085
J	0 20	0 30	0 008	0 012
K	3 05	3 56	0 120	0 140
L	15 24 BSC		0 600 BSC	
M	7°	10°	7°	10
N	0 51	1 02	0 020	0 040

Rockwell

R65C24
PERIPHERAL INTERFACE ADAPTER/TIMER (PIAT)

PRELIMINARY

DESCRIPTION

The R65C24 Peripheral Interface Adapter/Timer (PIAT) is designed to solve a broad range of peripheral control problems in the implementation of microcomputer systems. This device allows a very effective trade-off between software and hardware by providing significant capability and flexibility in a low cost chip. When coupled with the power and speed of the R6500, R6500/* or R65C00 family of microprocessors, the R65C24 allows implementation of very complex systems at a minimum overall cost.

Control of peripheral devices is handled primarily through two 8-bit bidirectional ports. Each of these lines can be programmed to act as either an input or an output. In addition, four peripheral control/interrupt input lines are provided. These lines can be used to interrupt the processor or to "handshake" data between the processor and a peripheral device.

The PIAT also contains one 16-bit Counter/Timer comprised of a 16-bit counter, two 8-bit latches associated with the counter, and an 8-bit snapshot latch for the upper half of the counter. A counter mode control register, under software direction, selects any one of eight counter modes of operation, and the status register contains an underflow flag to report counter time-out. A maskable interrupt request allows immediate CPU notification upon counter time-out.

ORDERING INFORMATION

The R65C24 is available in both a ceramic and a plastic 40-pin package, a commercial or industrial temperature range, and operating frequencies of 1, 2, 3, or 4 MHz. These versions are coded into the part number as follows:

Part Number:
R65C24___

- Temperature Range:
  - Blank = 0°C to +70°C
  - E = −40°C to +85°C
- Frequency Range:
  - 1 = 1 MHz
  - 2 = 2 MHz
  - 3 = 3 MHz
  - 4 = 4 MHz
- Package:
  - C = Ceramic
  - P = Plastic

FEATURES

- Low power CMOS N-well silicon gate technology
- Two 8-bit bidirectional I/O ports with individual data direction control
- Programmable 16-bit Counter/Timer with eight modes of operation
- Three 8-bit latches associated with the Counter/Timer
- Selectable divide-by-sixteen prescaler for all modes
- Automatic "Handshake" control of data transfers
- Two interrupts (one for each port) with program control
- 1, 2, 3, and 4 MHz versions
- Commercial and industrial temperature range versions
- 40-pin plastic and ceramic versions
- Single 5V ± 5% supply requirements
- Compatible with the R6500, R6500/* and R65C00 family of microprocessors

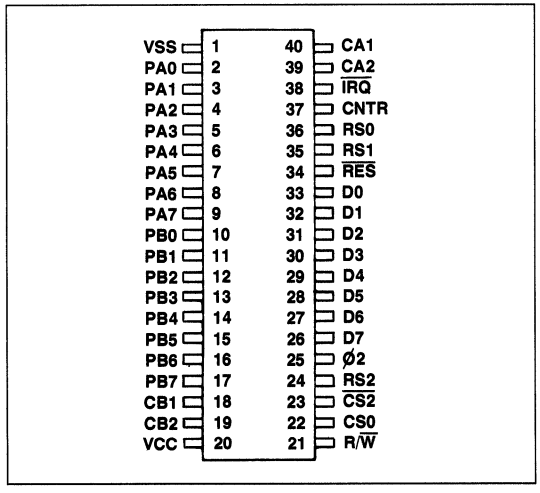


Figure 1. R65C24 Pin Configuration

FUNCTIONAL DESCRIPTION

The R65C24 PIAT is organized into three independent sections referred to as the A Side, the B Side, and a Counter/Timer. The A Side and B Side each consist of a Control Register (CRA, CRB), Data Direction Register (DDRA, DDRB), Output Register (ORA, ORB), Interrupt Status Control (ISCA, ISCB), and the buffers necessary to drive the Peripheral Interface buses. Data Bus Buffers (DBB) interface data from the two sections to the data bus, while the Data Input Register (DIR) interfaces data from the DBB to the PIAT registers. Chip Select and R/$\overline{W}$ control circuitry interface to the processor bus control lines. The Counter/Timer consists of a 16-bit counter; i.e., an 8-bit Upper Counter (UC) and 8-bit Lower Counter (LC), an 8-bit Upper Latch (UL), an 8-bit Lower Latch (LL), an 8-bit Snapshot Latch (SL), and a Status Register (SR). A Counter Mode Control Register (CMCR) selects the Counter/Timer mode of operation. Figure 2 is a block diagram of the R65C24 PIAT.

2

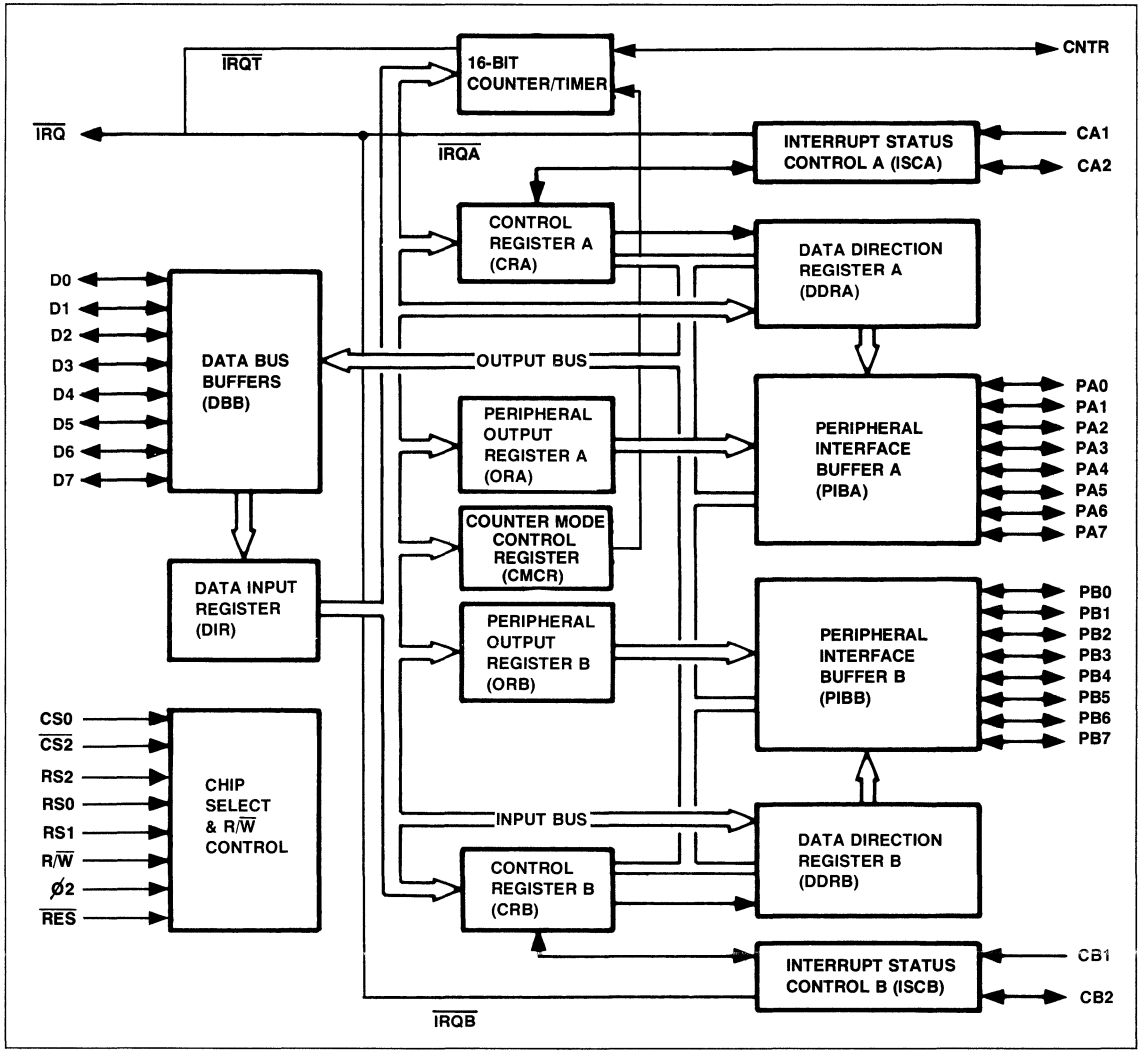


Figure 2. R65C24 PIAT Block Diagram

DATA INPUT REGISTER (DIR)

When the microprocessor writes data into the PIAT, the data which appears on the data bus during the Ø2 clock pulse is latched into the Data Input Register (DIR). The data is then transferred into one of six internal registers of the PIAT after the trailing edge of the Ø2 clock. This assures that the data on the peripheral output lines will make smooth transitions from high to low (or from low to high) and the voltage will remain stable except when it is going to the opposite polarity.

CONTROL REGISTERS (CRA AND CRB)

Table 1 illustrates the bit designation and functions in the two control registers. The control registers allow the microprocessor to control the operation of the Interrupt Control inputs (CA1, CA2, CB1, CB2), and Peripheral Control outputs (CA2, CB2). Bit 2 in each register controls the addressing of the Data Direction Registers (DDRA, DDRB) and the Output Registers (ORA, ORB). In addition, two bits (bit 6 and 7) in each control register indicate the status of the Interrupt Input lines (CA1, CA2, CB1, CB2). These Interrupt Status bits (IRQA1, IRQA2 or IRQB1, IRQB2) are normally interrogated by the microprocessor during the $\overline{IRQ}$ interrupt service routine to determine the source of the interrupt.

DATA DIRECTION REGISTERS (DDRA, DDRB)

The Data Direction Registers (DDRA, DDRB) allow the processor to program each line in the 8-bit Peripheral I/O port to be either an input or an output. Each bit in DDRA controls the corresponding line in the Peripheral A port and each bit in DDRB controls the corresponding line in the Peripheral B port. Writing a "0" in a bit position in the Data Direction Register causes the corresponding Peripheral I/O line to act as an input; a "1" causes it to act as an output.

Bit 2 (DDRA, DDRB) in each Control Register (CRA and CRB) controls the accessing to the Data Direction Register or the Peripheral interface. If bit 2 is a "1," a Peripheral Output register (ORA, ORB) is selected, and if bit 2 is a "0," a Data Direction Register (DDRA, DDRB) is selected. The Data Direction Register Access Control bit, together with the Register Select lines (RS0, RS1 and RS2) selects the various internal registers as shown in Table 2.

In order to write data into DDRA, ORA, DDRB, or ORB registers, bit 2 in the proper Control Register must first be set. The desired register may then be accessed with the address determined by the address interconnect technique used.

PERIPHERAL OUTPUT REGISTERS (ORA, ORB)

The Peripheral Output Registers (ORA, ORB) store the output data from the Data Bus Buffers (DBB) which appears on the Peripheral I/O port. If a line on the Peripheral A Port is programmed as an output by the DDRA, writing a 0 into the corresponding bit in the ORA causes that line to go low (<0.4 V); writing a 1 causes the line to go high. The lines of the Peripheral B port are controlled by ORB in the same manner.

INTERRUPT STATUS CONTROL (ISCA, ISCB)

The four interrupt/peripheral control lines (CA1, CA2, CB1, CB2) are controlled by the Interrupt Status Control logic (A, B). This logic interprets the contents of the corresponding Control Register and detects active transitions on the interrupt inputs.

PERIPHERAL I/O PORTS (PA0-PA7, PB0-PB7)

The Peripheral A and Peripheral B I/O ports allow the microprocessor to interface to the input lines on the peripheral device by writing data into the Peripheral Output Register. They also allow the processor to interface with the peripheral device output lines by reading the data on the Peripheral Port input lines directly onto the data bus and into the internal registers of the processor.

Each of the Peripheral I/O lines can be programmed to act as an input or an output. This is accomplished by setting a 1 in the corresponding bit in the Data Direction Register for those lines which are to act as outputs. A 0 in a bit of the Data Direction Register causes the corresponding Peripheral I/O lines to act as an input.

The buffers which drive the Peripheral A I/O lines contain "passive" pull-up devices. These pull-up devices are resistive in nature and therefore allow the output voltage to go to VCC for a logic 1. The switches can sink a full 3.2 mA, making these buffers capable of driving two standard TTL loads.

In the input mode, the pull-up devices are still connected to the I/O pin and still supply current to this pin. For this reason, these lines also represent two standard TTL loads in the input mode.

The Peripheral B I/O port duplicates many of the functions of the Peripheral A port. The process of programming these lines to act as an input or an output is similar to the Peripheral A port, as is the effect of reading or writing this port. However, there are several characteristics of the buffers driving these lines which affect their use in peripheral interfacing.

Table 1. Control Registers Bit Designations

	7	6	5	4	3	2	1	0
CRA	IRQA1	IRQA2	CA2 Control			DDRA Access	CA1 Control	
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CRB	IRQB1	IRQB2	CB2 Control			DDRB Access	CB1 Control	

The Peripheral B I/O port buffers are push-pull devices i.e., the pull-up devices are switched OFF in the 0 state and ON for a logic 1. Since these pull-ups are active devices, the logic 1 voltage will not go higher than +2.4V.

Unlike the PA0-PA7 lines (which have pull-up devices), the PB0 through PB7 lines have three-state capability which allows them to enter a high impedance state when programmed to be used as input lines. In addition, data on these lines will be read properly, when programmed as output lines, even if the data signals fall below 2.0 volts for a "high" state or are above 0.8 volts for a "low" state. When programmed as output, each line can drive at least a two TTL load and may also be used as a source of up to 3.2 milliamperes at 1.5 volts to directly drive the base of a transistor switch, such as a Darlington pair.

Because these outputs are designed to drive transistors directly, the output data is read directly from the Peripheral Output Register for those lines programmed to act as inputs.

The final characteristic is the high-impedance input state which is a function of the Peripheral B push-pull buffers. When the Peripheral B I/O lines are programmed to act as inputs, the output buffer enters the high impedance state.

DATA BUS BUFFERS (DBB)

The Data Bus Buffers are 8-bit bidirectional buffers used for data exchange, on the D0-D7 Data Bus, between the microprocessor and the PIAT. These buffers are tri-state and are capable of driving a two TTL load (when operating in an output mode) and represent a one TTL load to the microprocessor (when operating in an input mode).

COUNTER/TIMER

The Counter/Timer includes a 16-bit counter and three 8-bit data latches. It also includes an 8-bit Counter Mode Control Register (CMCR) to select the Counter/Timer operating mode and options and an 8-bit Status Register to report time-out condition as well as peripheral data port interrupt conditions. Figure 3 illustrates the Timer/Counter.

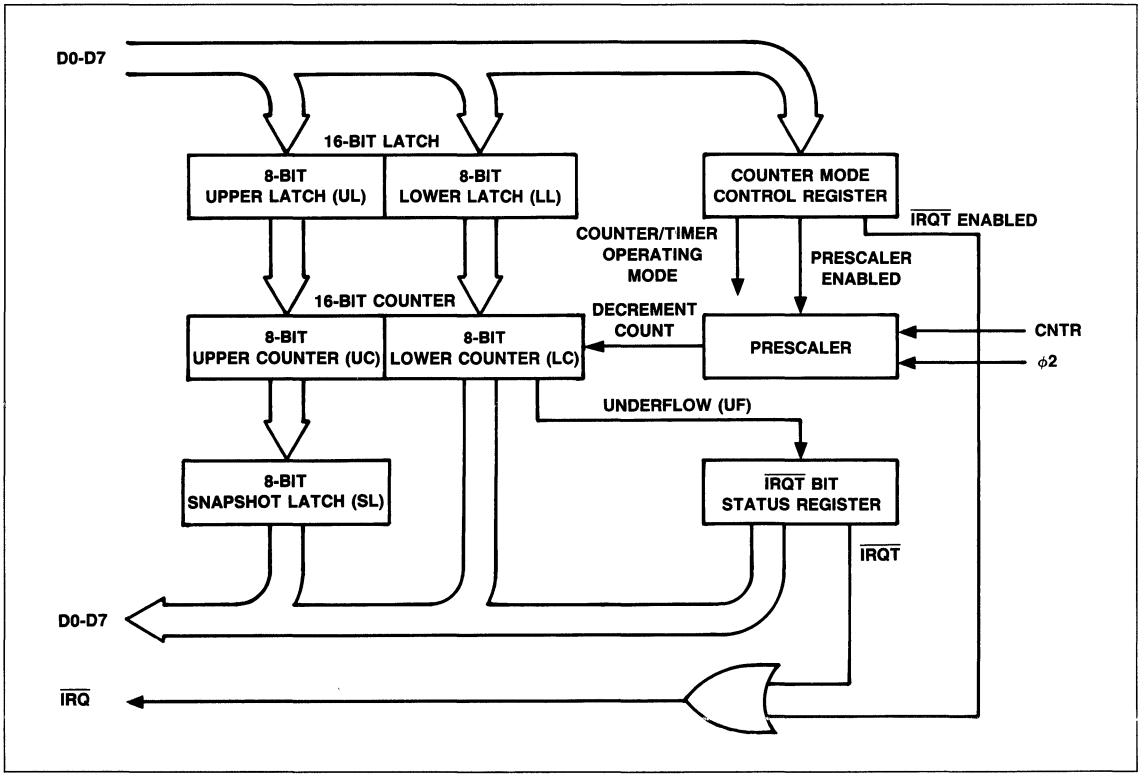


Figure 3. Counter/Timer

Counter/Latches—The Upper Counter (UC) and Lower Counter (LC) form a 16-bit down-counter that counts either $\phi 2$ clock pulses from the processor bus or external events from input line CNTR, depending on the mode selected. The Upper Latch (UL) and Lower Latch (LL) hold the initial higher- and lower-order count values to be loaded into the counter. The Snapshot Latch (SL) is loaded with the value of the UC when the LC is read or the LL is written into by the PIAT. After a read of the LC, the Snapshot Latch is read to provide the current 16-bit value of the counter. The Underflow Flag (UF) in the Status Register (SR) is set to a 1 whenever the counter (UC, LC) decrements past $0000. A Prescaler can be program activated to divide-by-sixteen rather than divide-by-one for any of the Counter/Timer modes.

Counter Mode Control Register—The Counter Mode Control Register (CMCR) allows program selection of any of eight Counter/Timer modes of operation, for the enabling or disabling of the Prescaler, and the enabling or disabling of the $\overline{IRQT}$ interrupt line. Bits 2, 1, 0 of the CMCR selects one of the following Counter/Timer operating modes:

Disable Counter/Timer
One-Shot Interval Timer
Free-Run Interval Timer
Pulse Width Measurement
Event Counter
One-Shot Pulse Width Generation
Free-Run Pulse Generation
Retriggerable Interval Timer

Bit 7 of the CMCR determines whether the $\overline{IRQT}$ line is enabled or disabled for generating an interrupt request on the $\overline{IRQ}$ output to the processor. When bit 7 is set to a 1, $\overline{IRQT}$ is enabled so that an Underflow Flag (UF bit in the Status Register set to a 1) will cause $\overline{IRQ}$ to be asserted. When bit 7 is set to a 0, the $\overline{IRQT}$ is disabled.

Bit 4 of the CMCR enables or disables the Prescaler. A 1 in bit 4 causes the Prescaler to be enabled so that the Counter/Timer is operating in a divide-by-sixteen mode. When this bit is a 0, the Prescaler is disabled so that the Counter/Timer is operating in a normal (divide-by-one) mode.

Status Register—Bit 7 of the Status Register (SR) reports the Counter Underflow Status. This underflow (UF) bit is set to 1 when the counter decrements past $0000. When this bit is set, the $\overline{IRQ}$ output will be asserted if the Interrupt Enable bit in the CMCR is set to a 1. The status of the Port A Interrupt Flag ($\overline{IRQA}$) and Port B Interrupt Flag ($\overline{IRQB}$) are reported in bits 6 and 5, respectively, in addition to being reported in the ISCA and ISCB registers.

INTERFACE SIGNALS

The PIAT interfaces to the R6500, R6500/* or the R65C00 microprocessor family with a reset line, a $\phi 2$ clock line, a read/write line, an interrupt request line, three register select lines, two chip select lines, and an 8-bit bidirectional data bus.

The PIAT interfaces to the peripheral devices with four interrupt/control lines and two 8-bit bidirectional data buses. A Counter/Timer input/output line (CNTR) also interfaces to a peripheral device.

Figure 1 (on the front page) shows the pin assignments for these interface signals and Figure 4 shows the interface relationship of these signal as they pertain to the CPU and the peripheral devices.

CHIP SELECT (CS0, $\overline{CS2}$)

The PIAT is selected when CS0 is high and $\overline{CS2}$ is low. These two chip select lines are normally connected to the processor address lines either directly or through external decoder circuits. When the PIAT is selected, data will be transferred between the data lines and PIAT registers, and/or peripheral interface lines as determined by the R/$\overline{W}$, RS0, RS1 and RS2 lines and the contents of Control Registers A and B.

Note:

An R65C24 PIAT may be installed in a circuit in place of an R65C21 PIA subject to chip select considerations. Since the R65C21 has a CS1 input and the R65C24 does not have a CS1 input, the PIAT will be selected in the same addresses as the PIA *and maybe more* depending upon external address decoding circuitry.

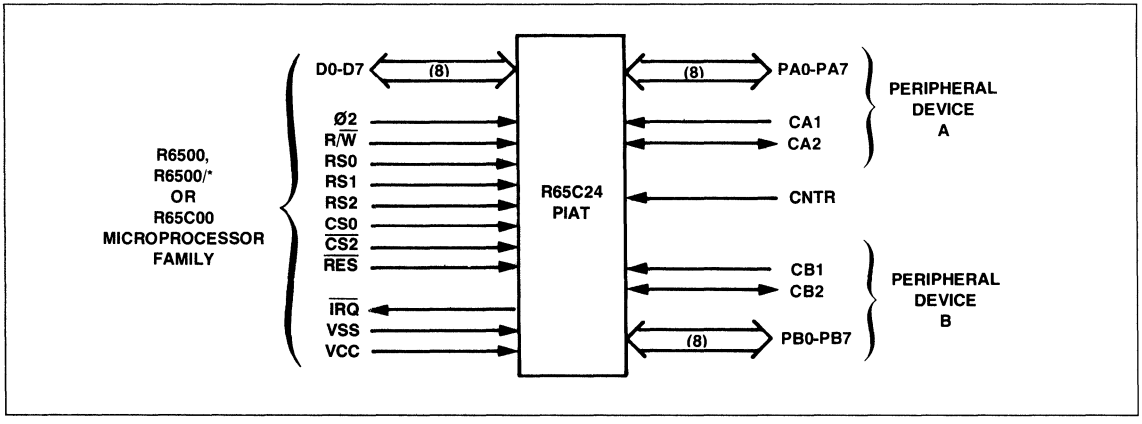


Figure 4. Interface Signals Relationship

RESET SIGNAL ($\overline{RES}$)

The Reset ($\overline{RES}$) input initializes the R65C24 PIAT. A low signal on the $\overline{RES}$ input causes all internal registers to be cleared.

CLOCK SIGNAL ($\phi 2$)

The Phase 2 Clock Signal ($\phi 2$) is the system clock that triggers all data transfers between the CPU and the PIAT. $\phi 2$ is generated by the CPU and is therefore the synchronizing signal between the CPU and the PIAT.

READ/WRITE SIGNAL (R/$\overline{W}$)

Read/Write (R/$\overline{W}$) controls the direction of data transfers between the PIAT and the data lines associated with the CPU and the peripheral devices. A high on the R/$\overline{W}$ line permits the peripheral devices to transfer data to the CPU from the PIAT. A low on the R/$\overline{W}$ line allows data to be transfered from the CPU to the peripheral devices from the PIAT.

REGISTER SELECT (RS0, RS1, RS2)

Two of the Register Select lines (RS0, RS1), in conjunction with the Control Registers (CRA, CRB) Data Direction Register access bits select various R65C24 registers to be accessed by the CPU. RS0 and RS1 are normally connected to the microprocessor (CPU) address output lines. Through control of these lines, the CPU can write directly into the Control Registers (CRA, CRB) the Data Direction Registers (DDRA, DDRB) and the Peripheral Output Registers (ORA, ORB). In addition, the processor may directly read the contents of the Control Registers and the Data Direction Registers. Accessing the Peripheral Output Register for the purpose of reading data back into the processor operates differently on the ORA and the ORB registers and therefore are shown separately in Table 2.

Note:

In order to address the ORA and ORB Registers in the PIAT, Register Select line RS2 *must be high.* When RS2 is low, the Counter/Timer registers are selected (as shown in Table 3).

Table 2. Peripheral Register Addressing

Register Address (Hex)	Register Select Lines			Data Direction Register Control		Register Operation	
	RS2	RS1	RS0	CRA (Bit 2)	CRB (Bit 2)	R/$\overline{W}$ = H	R/$\overline{W}$ = L
4	H	L	L	1	—	Read PIBA	Write ORA
4	H	L	L	0	—	Read DDRA	Write DDRA
5	H	L	H	—	—	Read CRA	Write CRA
6	H	H	L	—	1	Read PIBB	Write ORB
6	H	H	L	—	0	Read DDRB	Write DDRA
7	H	H	H	—	—	Read CRB	Write CRB

Register Select line RS2 determines whether the addressed registers are part of the Counter/Timer or the peripheral Port A and Port B sections of the PIAT. When RS2 is high, the Port A/Port B registers shown in Table 2 are selected. When the RS2 is low, the Counter/Timer registers are selected and operated upon as shown in Table 3.

Table 3. Counter/Timer Register Addressing

Register Address (Hex)	Register Select Lines			Counter/Timer Operation	
	RS2	RS1	RS0	(R/$\overline{W}$ = H)	(R/$\overline{W}$ = L)
0	L	L	L	Read Snapshot Latch (SL) SL → D0-D7 0 → UF	Write Upper Latch (UL) D0-D7 → UL 0 → UF Load and Enable Counter UL → UC, LL → LC
1	L	L	H	Read Upper Counter (UC) UC → D0-D7	Write Upper Latch (UL) D0-D7 → UL
2	L	H	L	Read Lower Counter (LC) LC → D0-D7 UC → SL	Write Lower Latch (LL) D0-D7 → LL UC → SL
3	L	H	H	Read Status Register (SR) SR → D0-D7 0 → UF,	Write Counter Control Mode Register (CMCR) D0-D7 → CMCR

INTERRUPT REQUEST LINE ($\overline{IRQ}$)

Three internal active low Interrupt Request lines ($\overline{IRQA}$, $\overline{IRQB}$, and $\overline{IRQT}$) act to interrupt the microprocessor through the external $\overline{IRQ}$ output. $\overline{IRQ}$ is an open drain output and is capable of sinking 1.6 milliamps from an external source. This permits all interrupt request lines to be tied together in a wired-OR configuration. The A and B in the titles of these internal lines correspond to the peripheral port A and the peripheral port B so that each interrupt request line services one peripheral data port. The T corresponds to the Counter/Timer generated interrupt request.

$\overline{IRQA}$ and $\overline{IRQB}$ Lines—These two internal Interrupt Request lines are associated with the Port A and Port B sections of the PIAT and are controlled by Control Registers CRA and CRB, and the Peripheral Control lines CA1, CA2, CB1, and CB2.

These Interrupt Request lines have three interrupt flag bits which can cause the Interrupt Request line to go low. These flags are bits 6 and 7 in the two Control Registers (CRA, CRB). These flags act as the link between the peripheral interrupt signals and the microprocessor interrupt inputs. Each flag has a corresponding interrupt disable bit which allows the processor to enable or disable the interrupt from each of the four interrupt

inputs (CA1, CA2, CB1, CB2). The four interrupt flags are set (enabled) by active transitions of the signal on the interrupt input (CA1, CA2, CB1, CB2).

CRA bit 7 (IRQA1) is always set by an active transition of the CA1 interrupt input signal. However, $\overline{IRQA}$ can be disabled by setting bit 0 in CRA to a 0. Likewise, CRA bit 6 (IRQA2) can be set by an active transition of the CA2 interrupt input signal and $\overline{IRQA}$ can be disabled by setting bit 3 in CRA to a 0.

Both bit 6 and bit 7 in CRA are reset by a "Read Peripheral Output Register A" operation. This is defined as an operation in which the read/write, proper data direction register and register select signals are provided to allow the processor to read the Peripheral A I/O port. A summary of $\overline{IRQA}$ control is shown in Table 3.

Control of $\overline{IRQB}$ is performed in exactly the same manner as that described above for $\overline{IRQA}$. Bit 7 in CRB (IRQB1) is set by an active transition on CB1 and $\overline{IRQB}$ from this flag is controlled by CRB bit 0. Likewise, bit 6 (IRQB2) in CRB is set by an active transition on CB2, and $\overline{IRQB}$ from this flag is controlled by CRB bit 3.

Also, both bit 6 and bit 7 of CRB are reset by a "Read Peripheral B Output Register" operation. A summary of $\overline{IRQB}$ control is shown in Table 4.

Table 4. $\overline{IRQA}$ and $\overline{IRQB}$ Control Summary

Control Register Bits	Action
CRA-7=1 and CRA-0=1	$\overline{IRQA}$ goes low (Active)
CRA-6=1 and CRA-3=1	$\overline{IRQA}$ goes low (Active)
CRB-7=1 and CRB-0=1	$\overline{IRQB}$ goes low (Active)
CRB-6=1 and CRB-3=1	$\overline{IRQB}$ goes low (Active)

Note:

The flags act as the link between the peripheral interrupt signals and the processor interrupt inputs. The interrupt disable bits allow the processor to control the interrupt function.

$\overline{IRQT}$ Line—The internal $\overline{IRQT}$ line is associated with the Counter/Timer and is controlled by the $\overline{IRQT}$ Enable bit in the Counter Mode Control Register and the Underflow Flag in the Status Register. A thorough discussion of the functions and operation of the $\overline{IRQT}$ line is given in the Counter/Timer Operation section of this product description.

INTERRUPT INPUT/PERIPHERAL CONTROL LINES (CA1, CA2, CB1, CB2)

The four interrupt input/peripheral control lines provide a number of special peripheral control functions. These lines greatly enhance the power of the two general purpose interface ports (PA0-PA7, PB0-PB7). Figure 5 summarizes the operation of these control lines.

CA1 is an interrupt input only. An active transition of the signal on this input will set bit 7 of the Control Register A to a logic 1. The active transition can be programmed by setting a "0" in bit 1 of the CRA if the interrupt flag (bit 7 of CRA) is to be set on a negative transition of the CA1 signal or a "1" if it is to be set on a positive transition.

Note:

A negative transition is defined as a transition from a high to a low, and a positive transition is defined as a transition from a low to a high voltage.

CA2 can act as a totally independent interrupt or as a peripheral control output. As an input (CRA, bit 5 = 0) it acts to set the interrupt flag, bit 6 of CRA, to a logic 1 on the active transition selected by bit 4 of CRA.

These control register bits and interrupt inputs serve the same basic function as that described above for CA1. The input signal sets the interrupt flag which serves as the link between the peripheral device and the processor interrupt structure. The interrupt disable bit allows the processor to exercise control over the system interrupt.

In the output mode (CRA, bit 5 = 1), CA2 can operate independently to generate a simple pulse each time the microprocessor reads the data on the Peripheral A I/O port. This mode is selected by setting CRA, bit 4 to a 0 and CRA, bit 3 to a 1. This pulse output can be used to control the counters, shift registers, etc. which make sequential data available on the Peripheral input lines.

A second output mode allows CA2 to be used in conjunction with CA1 to "handshake" between the processor and the peripheral device. On the A side, this technique allows positive control of data transfers from the peripheral device into the microprocessor. The CA1 input signals the processor that data is available by interrupting the processor. The processor reads the data and sets CA2 low. This signals the peripheral device that it can make new data available.

The final output mode can be selected by setting bit 4 of CRA to a 1. In this mode, CA2 is a simple peripheral control output which can be set high or low by setting bit 3 of CRA to a 1 or a 0 respectively.

CB1 operates as an interrupt input only in the same manner as CA1. Bit 7 of CRB is set by the active transition selected by bit 0 of CRB. Likewise, the CB2 input mode operates exactly the same as the CA2 input modes. The CB2 output modes, CRB bit 5 = 1, differ somewhat from those of CA2. The pulse output occurs when the processor writes data into the Peripheral B Output Register. Also, the "handshaking" operates on data transfers from the processor into the peripheral device.

CA2 INPUT MODE (BIT 5 = 0) **CONTROL REGISTER A (CRA)**

7	6	5	4	3	2	1	0
IRQA1 FLAG	IRQA2 FLAG	CA2 INPUT MODE SELECT (=0)	IRQA2 POSITIVE TRANSITION	$\overline{\text{IRQA}}$ ENABLE FOR IRQA2	ORA SELECT	IRQA1 POSITIVE TRANSITION	$\overline{\text{IRQA}}$ ENABLE FOR IRQA1
			$\overline{\text{IRQA}}$/IRQA2 CONTROL			$\overline{\text{IRQA}}$/IRQA1 CONTROL	

CA2 OUTPUT MODE (BIT 5 = 1)

7	6	5	4	3	2	1	0
IRQA1 FLAG	0	CA2 OUTPUT MODE SELECT (=1)	CA2 OUTPUT CONTROL	CA2 RESTORE CONTROL	ORA SELECT	IRQA1 POSITIVE TRANSITION	$\overline{\text{IRQA}}$ ENABLE FOR IRQA1
			CA2 CONTROL			$\overline{\text{IRQA}}$/IRQA1 CONTROL	

CA2 INPUT OR OUTPUT MODE (BIT 5 = 0 or 1)

Bit 7 IRQA1 FLAG
1 A transition has occurred on CA1 that satisfies the bit 1 IRQA1 transition polarity criteria. This bit is cleared by a read of Output Register A or by $\overline{\text{RES}}$
0 No transition has occurred on CA1 that satisfies the bit 1 IRQA1 transition polarity criteria

Bit 2 OUTPUT REGISTER A SELECT
1 Select Output Register A
0 Select Data Direction Register A

Bit 1 IRQA1 POSITIVE TRANSITION
1 Set IRQA1 Flag (bit 7) on a positive (low-to-high) transition of CA1.
0 Set IRQA1 Flag (bit 7) on a negative (high-to-low) transition of CA1.

Bit 0 $\overline{\text{IRQA}}$ ENABLE FOR IRQA1
1 Enable assertion of $\overline{\text{IRQA}}$ when IRQA1 Flag (bit 7) is set
0 Disable assertion of $\overline{\text{IRQA}}$ when IRQA1 Flag (bit 7) is set.

CA2 INPUT MODE (BIT 5 = 0)

Bit 6 IRQA2 FLAG
1 A transition has occurred on CA2 that satisfies the bit 4 IRQA2 transition polarity criteria. This flag is cleared by a read of Output Register A or by $\overline{\text{RES}}$.
0 No transition has occurred on CA2 that satisfies the bit 4 IRQA2 transition polarity criteria

Bit 5 CA2 MODE SELECT
0 Select CA2 Input Mode

Bit 4 IRQA2 POSITIVE TRANSITION
1 Set IRQA2 Flag (bit 6) on a positive (low-to-high) transition of CA2
0 Set IRQA2 Flag (bit 6) on a negative (high-to-low) transition of CA2

Bit 3 $\overline{\text{IRQA}}$ ENABLE FOR IRQA2
1 Enable assertion of $\overline{\text{IRQA}}$ when IRQA2 Flag (bit 6) is set
0 Disable assertion of $\overline{\text{IRQA}}$ when IRQA2 Flag (bit 6) is set

CA2 OUTPUT MODE (BIT 5 = 1)

Bit 6 NOT USED
0 Always zero.

Bit 5 CA2 MODE SELECT
1 Select CA2 Output Mode

Bit 4 CA2 OUTPUT CONTROL
1 CA2 goes low when a zero is written into CRA bit 3 CA2 goes high when a one is written into CRA bit 3
0 CA2 goes low on the first negative (high-to-low) $\phi 2$ clock transition following a read of Output Register A. CA2 returns high as specified by bit 3

Bit 3 CA2 READ STROBE RESTORE CONTROL (BIT 4 = 0)
1 CA2 returns high on the next $\phi 2$ clock negative transition following a read of Output Register A
0 CA2 returns high on the next active CA1 transition following a read of Output Register A as specified by bit 1

Figure 5. Summary of Control Lines Operation (1 of 2)

CB2 INPUT MODE (BIT 5 = 0)

CONTROL REGISTER B (CRB)

7	6	5	4	3	2	1	0
IRQB1 FLAG	IRQB2 FLAG	CB2 INPUT MODE SELECT (=0)	IRQB2 POSITIVE TRANSITION	$\overline{\text{IRQB}}$ ENABLE FOR IRQB2	ORB SELECT	IRQB1 POSITIVE TRANSITION	$\overline{\text{IRQB}}$ ENABLE FOR IRQB1
			$\overline{\text{IRQB}}$/IRQB2 CONTROL			$\overline{\text{IRQB}}$/IRQB1 CONTROL	

CB2 OUTPUT MODE (BIT 5 = 1)

7	6	5	4	3	2	1	0
IRQB1 FLAG	0	CB2 OUTPUT MODE SELECT (=1)	CB2 OUTPUT CONTROL	CB2 RESTORE CONTROL	ORB SELECT	IRQB1 POSITIVE TRANSITION	$\overline{\text{IRQB}}$ ENABLE FOR IRQB1
			CB2 CONTROL			$\overline{\text{IRQB}}$/IRQB1 CONTROL	

CB2 INPUT OR OUTPUT MODE (BIT 5 = 0 or 1)

Bit 7 IRQB1 FLAG
1 A transition has occurred on CB1 that satisfies the bit 1 IRQB1 transition polarity criteria This bit is cleared by a read of Output Register B or by $\overline{\text{RES}}$
0 No transition has occurred on CB1 that satisfies the bit 1 IRQB1 transition polarity criteria

Bit 2 OUTPUT REGISTER B SELECT
1 Select Output Register B
0 Select Data Direction Register B

Bit 1 IRQB1 POSITIVE TRANSITION
1 Set IRQB1 Flag (bit 7) on a positive (low-to-high) transition of CB1.
0 Set IRQB1 Flag (bit 7) on a negative (high-to-low) transition of CB1

Bit 0 $\overline{\text{IRQB}}$ ENABLE FOR IRQB1
1 Enable assertion of $\overline{\text{IRQB}}$ when IRQB1 Flag (bit 7) is set
0 Disable assertion of $\overline{\text{IRQB}}$ when IRQB1 Flag (bit 7) is set

CB2 INPUT MODE (BIT 5 = 0)

Bit 6 IRQB2 FLAG
1 A transition has occurred on CB2 that satisfies the bit 4 IRQB2 transition polarity criteria This flag is cleared by a read of Output Register B or by $\overline{\text{RES}}$
0 No transition has occurred on CB2 that satisfies the bit 4 IRQB2 transition polarity criteria

Bit 5 CB2 MODE SELECT
0 Select CB2 Input Mode

Bit 4 IRQB2 POSITIVE TRANSITION
1 Set IRQB2 Flag (bit 6) on a positive (low-to-high) transition of CB2
0 Set IRQB2 Flag (bit 6) on a negative (high-to-low) transition of CB2

Bit 3 $\overline{\text{IRQB}}$ ENABLE FOR IRQB2
1 Enable assertion of $\overline{\text{IRQB}}$ when IRQB2 Flag (bit 6) is set
0 Disable assertion of $\overline{\text{IRQB}}$ when IRQB2 Flag (bit 6) is set

CB2 OUTPUT MODE (BIT 5 = 1)

Bit 6 NOT USED
0 Always zero

Bit 5 CB2 MODE SELECT
1 Select CB2 Output Mode.

Bit 4 CB2 OUTPUT CONTROL
1 CB2 goes low when a zero is written into CRB bit 3. CB2 goes high when a one is written into CRB bit 3
0 CB2 goes low on the first negative (high-to-low) $\phi 2$ clock transition following a write to Output Register B CB2 returns high as specified by bit 3

Bit 3 CB2 WRITE STROBE RESTORE CONTROL (BIT 4 = 0)
1 CB2 returns high on the next $\phi 2$ clock negative transition following a write to Output Register B
0 CB2 returns high on the next active CB1 transition following a write to Output Register B as specified by bit 1

Figure 5. Summary of Control Lines Operation (2 of 2)

COUNTER/TIMER REGISTERS

COUNTER MODE CONTROL REGISTER (CMCR)

The 8-bit Counter Mode Control Register (CMCR) selects the Counter/Timer mode of operation and enables or disables both the internal $\overline{IRQT}$ and the Prescaler. The format of the CMCR is:

7	6	5	4	3	2 1 0
$\overline{IRQT}$ Enabled	0	0	Prescaler Enabled	0	Counter/Timer Mode

Bit 7 **$\overline{IRQT}$ Enabled**
0 $\overline{IRQT}$ Disabled
1 $\overline{IRQT}$ Enabled

Bits 6-5 **Not used, don't care value during write.**

Bit 4 **Prescaler Enabled**
0 Prescaler Disabled (−1)
1 Prescaler Enabled (−16)

Bit 3 **Not used, don't care value during write.**

Bits 2-0 **Counter/Timer Mode**
0 0 0 Mode 0—Disable Counter/Timer
0 0 1 Mode 1—One-Shot Interval Timer
0 1 0 Mode 2—Free-Run Interval Timer
0 1 1 Mode 3—Pulse Width Measurement
1 0 0 Mode 4—Event Counter
1 0 1 Mode 5—One-Shot Pulse Width Generation
1 1 0 Mode 6—Free-Run Pulse Generation
1 1 1 Mode 7—Retriggerable Interval Timer

The CMCR can be written into at any time without disabling or stopping the Counter/Timer. This allows the Counter/Timer mode of operation to be changed while it is still in operation. However, selecting Mode 0 disables the Counter/Timer and stops its operation. The Prescaler and the $\overline{IRQT}$ interrupt can also be enabled or disabled at any time. The CMCR is written to when the register address is 3 and R/$\overline{W}$ is low.

STATUS REGISTER (SR)

The 8-bit Status Register (SR) reports the status of two interrupt conditions: Counter underflow ($\overline{IRQT}$) and Port A interrupt ($\overline{IRQA}$). The format of the Status Register is:

7	6	5	4	3	2	1	0
UF (IRQT) Interrupt Flag	IRQA Interrupt Flag	0	1	1	1	1	1

Bit 7 **Counter Underflow (UF) Interrupt Flag**
0 Counter underflow has not occurred.
1 Counter underflow has occurred.

Bit 6 **IRQA Interrupt Flag**
0 Port A interrupt has not occurred.
1 Port A interrupt has not occurred.

Bit 5-0 **Not used, always read as shown in register figure.**

The Counter underflow (UF), bit 7, is updated in the same clock cycle that an underflow condition occurs on the Counter/Timer. The $\overline{IRQA}$ interrupt flag (bit 6) is updated at the rising edge of the next Ø2 clock immediately following the setting of corresponding interrupt bits (IRQA1, IRQA2) in the CRA register. $\overline{IRQA}$ is set whenever IRQA1 or IRQA2 is set. The underflow bit is cleared whenever the Status Register is read, the Snapshot Latch is read, the UL is written to at register address 0, Mode 0 is selected in the CMCR, or a $\overline{RES}$ occurs. Reading the Status Register also clears the $\overline{IRQA}$ interrupt flag. The Status Register is read when the register address is 3 and R/$\overline{W}$ is high.

LOWER LATCH (LL)

The Lower Latch (LL) holds the least significant 8-bits of the 16-bit latch value. The LL is written from the data bus (D0-D7) when the register address is 2 and R/$\overline{W}$ is low. When the LL is loaded, the contents of the UC are copied into the Snapshot Latch (SL) without affecting the counting operation of the UC.

UPPER LATCH (UL)

The Upper Latch (UL) holds the most significant 8-bits of the 16-bit latch value. The UL is written from the data bus (D0-D7) when R/$\overline{W}$ is low and the register address is either 0 or 1. The difference in the two register address functions are:

Register Address 0

1. The UL is loaded from D0-D7.
2. The contents of the Latch (UL and LL) are transferred to the Counter (UC and LC, respectively).
3. The UF bit is cleared in the SR.
4. The Counter is enabled, i.e., the count in UC and LC is decremented by one upon detection of a rising edge on either Ø2 or CNTR (depending upon mode selection) as scaled by the Prescaler.

Register Address 1

1. The UL is loaded from D0-D7.
2. All other elements of the Counter/Timer are unaffected.

LOWER COUNTER (LC)

The Lower Counter (LC) holds the least significant 8-bits of the 16-bit counter.

When the LC decrements below $00, 1 is borrowed from the UC to load $FF into the LC.

The LC is read to the data bus (D0-D7) when the register address is 2 and R/$\overline{W}$ is high. When LC is read, the 8-bit contents of the UC is transferred to the Snapshot Latch without affecting the operation of the counter (i.e., the count-down continues without interruption).

UPPER COUNTER

The Upper Counter (UC) holds the most significant 8-bits of the 16-bit counter. The UC is read to the data bus (D0-D7) when the register address is 1 and R/$\overline{W}$ is high. When the UC is read, there is no other effect on the Counter/Timer operation. Counter underflow occurs when the LC borrows a 1 from the UC value of $00.

Note:

When reading the UC directly, the value read can be one count too high if the LC value is just above $0000 at the start of the read since an underflow in the LC will result in decrementing the UC by one count. The Snapshot Latch should be read to obtain the UC value corresponding to the LC value.

SNAPSHOT LATCH (SL)

The Snapshot Latch holds the value of the UC corresponding to the LC value. The SL is loaded with the value of the UC when the LL is written to, or when the LC is read. The SL is read to the data bus (D0-D7) when the register address is 0 and R/$\overline{W}$ is high, without affecting the counting operation. When the SL is read, the UF in the SR is cleared. Since the SL is loaded with the value of the UC whenever the LC is read, an accurate count of the total 16-bit counter can be made without the need for further calculations to account for delays between the reading of the LC and the UC.

COUNTER/TIMER OPERATION

The Counter/Timer has eight modes of operation. The Counter/Timer is always either disabled (mode 0) or operating in one of the other seven modes as selected in the Counter Mode Control Register (CMCR).

To operate the Counter/Timer, first issue Mode 0 to stop any counting in progress due to a previously selected mode, to clear the counter underflow bit in the SR and to disable the $\overline{IRQT}$ interrupt. The order of mode selection and latch loading depends upon the desired mode. Generally, if a timer mode based on the Ø2 clock rate is to be selected, first select the mode then write the timer initialization value to the latch. Write the LL first then the UL value (to register address 0). When the UL is written, the UL and LL values are loaded into the UC and LC, respectively, and the counter is enabled. The counter then decrements one count for every positive edge (low to high) transition detected on the Ø2 or CNTR input (depending on the selected mode) as scaled by the Prescaler. In most modes, each time the counter underflows below $0000, the underflow bit is set in the SR, the counter reloads to the latch value and the down-counting continues. If the UF bit is set when the $\overline{IRQT}$ is enabled in the CMCR, the $\overline{IRQ}$ output will be asserted to the processor.

MODE 0—DISABLE COUNTER/TIMER

The Counter/Timer is disabled (all counting stops), the $\overline{IRQT}$ interrupt (bit 7 in the CMCR) is disabled, and the counter underflow (bit 7 in the SR) is cleared. Mode 0 may be selected at any time by selecting Mode 0 in the CMCR or upon $\overline{RES}$ which initializes the CMCR to $00. Selecting Mode 0 in the CMCR does not affect any data in the LL or UL, any count in the LC or UC, or any data in the SL.

MODE 1—ONE SHOT INTERVAL TIMER

The counter counts down once from the latch value at the Ø2 clock rate (as scaled by the Prescaler) and sets the UF bit in the SR upon underflow. The counter starts when data is written to the UL at register address 0, which causes the UL and LL values to be loaded into the UC and LC, respectively. When the counter decrements below $0000, the UF bit in the SR is set. The set UF bit causes $\overline{IRQ}$ to be asserted if the $\overline{IRQT}$ Enable bit is set in the CMCR. Upon decrementing below $0000, the UC and LC are automatically reset to a value of $FFFF and the counter continues down-counting. However, the UF bit in the SR will not be set again (due to the counter again decrementing through $0000) until the UL is again written at register address 0. The CNTR line is not used in this mode. Figure 6 shows the timing relationship for Mode 1 operation.

Typical Application: Can be used for an accurate time delay such as would be required to control the duration of time to have a thermal printer element activated.

MODE 2—FREE-RUN INTERVAL TIMER

The counter repetitively counts down at the Ø2 clock rate, as scaled by the Prescaler, and sets the UF bit in the SR each time the counter underflows. The counter is initialized to the UL and LL values and starts down counting at the clock rate when the UL value is written to register address 0. Each time the counter decrements below $0000, the UF bit in the SR is set, the counter is reloaded with the UL and LL value, and the count-down cycle continues. If the $\overline{IRQT}$ Enable bit is set in the CMCR, $\overline{IRQ}$ will thus be asserted upon each time-out. The CNTR line is not used in this mode. Figure 7 shows the timing relationship for Mode 2 operation.

Typical Application: Can be used for a timed interrupt structure when a hardware location needs updating at specific intervals, such as would be required to update a multiplexed display.

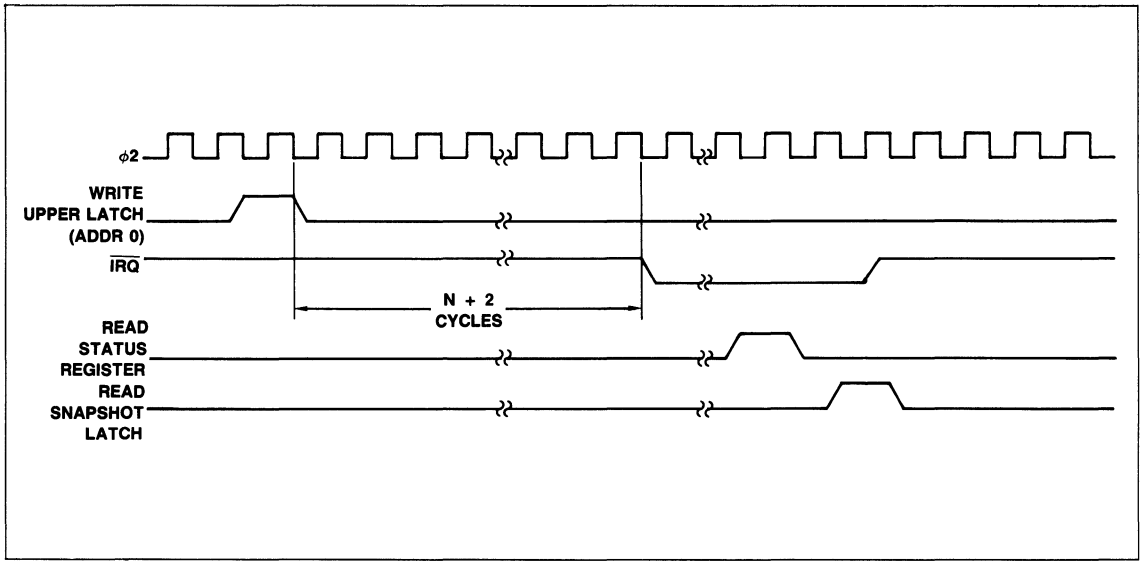


Figure 6. Mode 1—One-Shot Interval Timer Timing

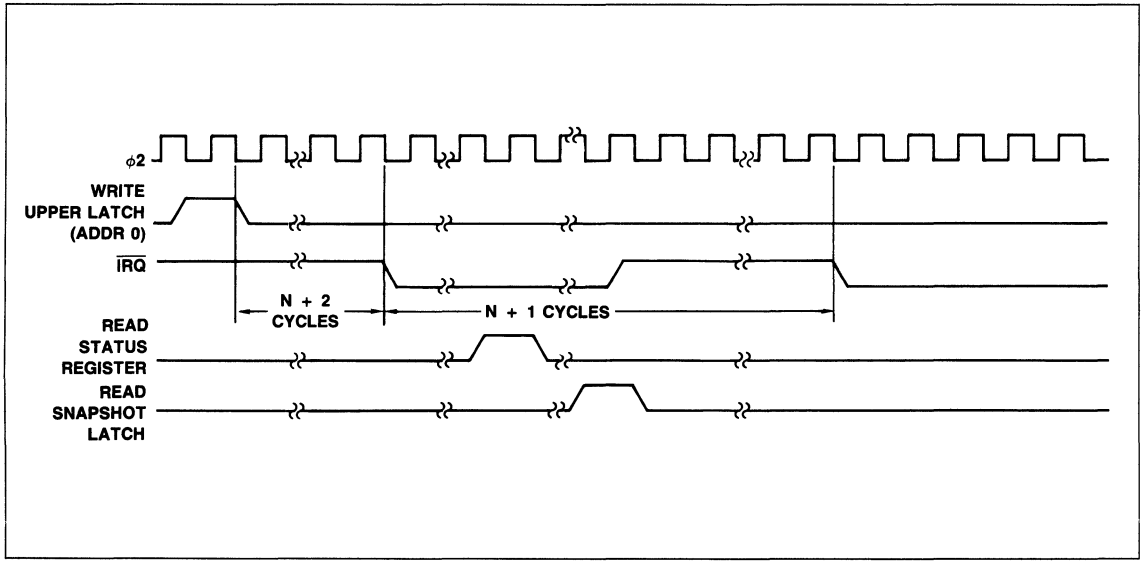


Figure 7. Mode 2—Free-Run Interval Timer Timing

MODE 3—PULSE WIDTH MEASUREMENT

The counter counts down from the latch value at the $\phi 2$ clock rate (scaled by the Prescaler) from the time the CNTR input goes low until CNTR goes high to provide a measurement of the CNTR low pulse duration. The counter is loaded with the value of the UL and LL upon writing UL to register address 0. The counter starts decrementing at the scaled $\phi 2$ clock rate when the CNTR line goes low and stops decrementing when the CNTR line returns high. If the counter decrements below $0000 before the CNTR line goes low, the UF bit in the SR is set, the counter is reloaded with the UL and LL value, and the cycle continues down until CNTR goes high. Once the CNTR line has cycled from high to low and back to high, the Counter/Timer will ignore any additional high to low transitions on the CNTR line. To reinitiate Mode 3, it is necessary to reload the UL by writing to register address 0. Figure 8 shows the timing relationships for a Mode 3 operation.

Typical Application: Can be used to measure the duration of an event from an external device. Allows an accurate measurement of the duration of a logical low pulse on the CNTR line.

MODE 4—EVENT COUNTER

CNTR is an input and the Counter/Timer counts the number of positive transitions on CNTR. The counter is initially loaded with the UL and LL value when the UL is written to register address 0. The counter then decrements one count on the rising edge of the $\phi 2$ clock after a rising edge (low to high transition) is detected on the CNTR input (as scaled by the Prescaler). The maximum rate at which this rising edge can be detected is one-half the $\phi 2$ clock rate. When the counter decrements below $0000, the UF bit in the SR is set, the counter is reloaded with the UL and LL value and the operation repeats. Figure 9 shows the timing relationship of a Mode 4 operation.

Typical Application: Can be used with a timed software loop to count external events (i.e., a frequency counter).

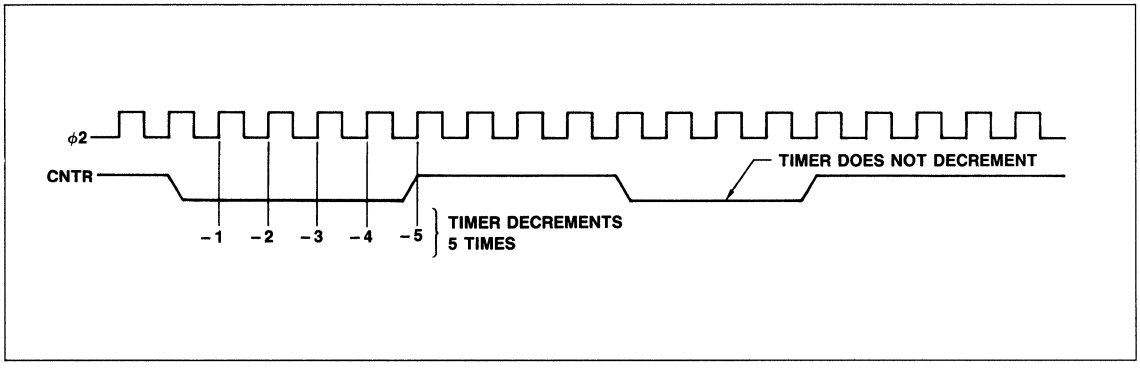


Figure 8. Mode 3—Pulse Width Measurement Timing

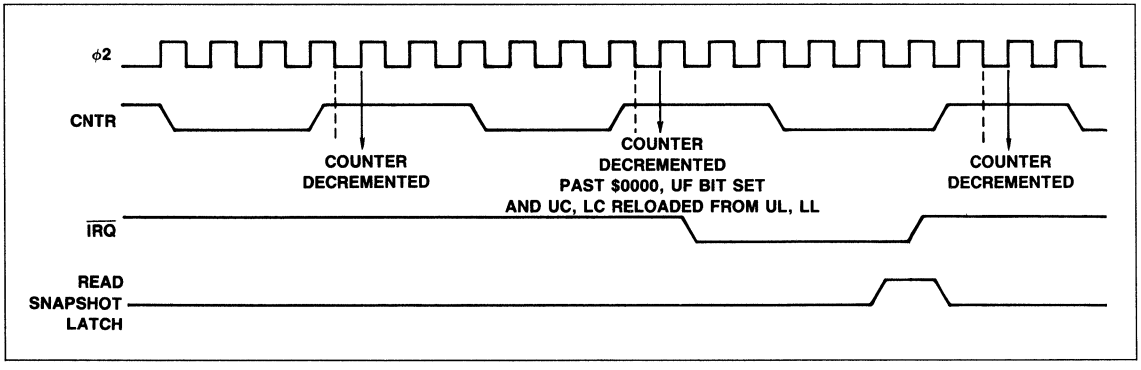


Figure 9. Mode 4—Event Counter Timing

MODE 5—ONE-SHOT PULSE WIDTH GENERATION

CNTR is an output which can be pulsed low for a programmed time interval. When this mode is selected in the CMCR, the CNTR output goes high (if the UF bit is set) or goes low (if the UF bit is cleared). The CNTR line then goes low when data is written to the UL at register address 0, which also starts the counter. The counter decrements from the UL and LL value at the Ø2 clock rate as scaled by the Prescaler. When the counter decrements below $0000, the CNTR output goes high, the UF bit is set in the SR, the counter is reloaded with $FFFF and the count-down continues. Figure 10 shows the timing relationship of Mode 5 operation.

Note that clearing the UF bit after it is set upon the first timeout causes CNTR to go low, in which case CNTR will again go high upon the next counter timeout.

Typical Application: Can be used to hold-off (delay) an external hardware event on an asynchronous basis such as disallowing a motor startup until certain parameters are met.

MODE 6—FREE-RUN PULSE GENERATION

CNTR is an output and the Counter/Timer can be programmed to generate a symmetrical waveform, an asymmetrical waveform, or a string of varying width pulses on CNTR. The CNTR line is forced low (if high upon mode selection) or remains low (if low upon mode selection) when data is written to the UL at register address 0 which also starts the counter. The counter decrements at the Ø2 clock rate as scaled by the Prescaler. When the counter decrements below $0000, CNTR toggles from low to high (or high to low depending upon its initial state), the counter is reloaded with the UL and LL value and the counter continues down-counting. The UF bit in the SR is set the first time the counter decrements past $0000 and is cleared only if a new write to UL at register address 0 occurs. Figure 11 shows the timing relationship of a Mode 6 operation.

This mode can be used to generate an asymmetrical waveform by toggling the UL and LL with the CNTR high and low times. Immediately after starting the counter with the first CNTR low time, load the LL and UL (by writing to register address 1, which does not restart the counter) with the CNTR high time. When the first counter underflow occurs, the counter loads the new latch value (i.e., the CNTR high time) into the counter and continues counting. During the $\overline{IRQ}$ interrupt processing resulting from the first counter time-out, load the LL and UL (at register address 1) with the original CNTR low time. Continue to alternate loading of the high and low time latch values during the interrupt processing for the duration of the mode.

Typical Application: Can be used to supply external circuitry with a software variable clock based upon the system Ø2 clock (e.g., a tone generator for audio feedback).

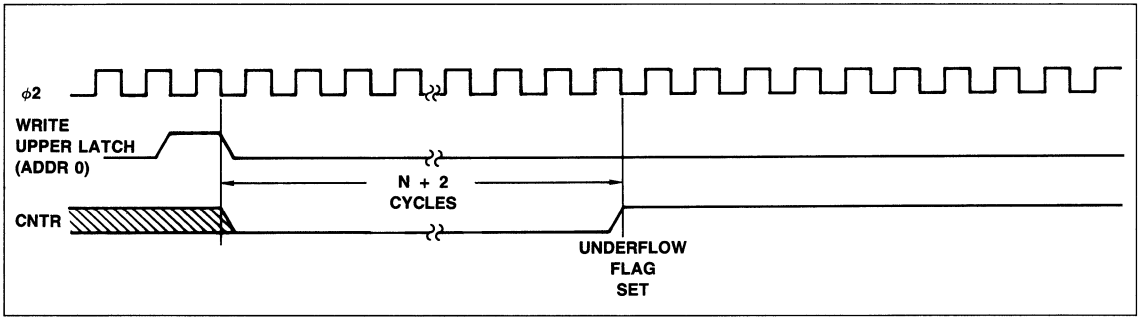


Figure 10. Mode 5—One-Shot Pulse Width Generation Timing

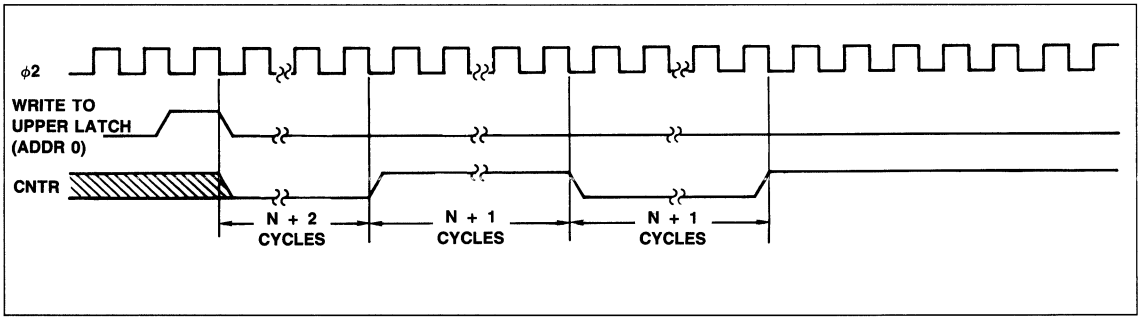


Figure 11. Mode 6—Free-Run Pulse Generation Timing

MODE 7—RETRIGGERABLE INTERVAL TIMER

The Counter/Timer operates as a timer which is retriggered, i.e., reinitialized to its starting value, upon detection of a negative transition on the CNTR input. The counter is initially loaded with the UL and LL value when the UL is written to register address 0. The counter starts decrementing at the Ø2 clock rate (as scaled by the Prescaler) when a falling edge (high to low transition) is detected on CNTR. The counter is reinitialized to the UL and LL value whenever a falling edge is subsequently detected on CNTR. If the counter decrements past $0000 before the falling edge is detected, the UF bit is set in the SR, the counter is initialized to the UL and LL value and the count-down continues.

Typical Application: Can be used to monitor signals that should be periodic and can interrupt the processor if the signal being monitored does not occur within a specified time frame; such as a synchronous motor that has fallen out of synchronization.

PRESCALER

The Counter/Timer operates in either the divide by one or divide by sixteen mode. In the divide by one mode, the counter holds from 1 to 65,535 counts. The counter capacity is therefore 1 μs to 65,535 μs at 1 MHz Ø2 clock rate or 0.25 μs to 16,383 μs at a 4 MHz Ø2 clock rate. Timer intervals greater than the maximum counter value can be easily measured by counting underflow flags or $\overline{IRQ}$ interrupt requests.

The divide by sixteen prescaler can be enabled to extend the timing interval by 16. This provides timing from 1048.56 ms (1 MHz) to 260.21 ms (4 MHz). The prescaler clocks the Counter/Timer at the Ø2 clock rate divided by sixteen, except for Mode 4. In Mode 4, sixteen positive CNTR edges must occur to decrement the Counter/Timer by one count.

INITIALIZING THE COUNTER/TIMER

The following program segment is one suggested technique for initializing the Counter/Timer:

```
;Data Definition
SL      = $XXX0     ;Snapshot Latch
UC      = $XXX1     ;Upper Counter
LC      = $XXX2     ;Lower Counter
SR      = $XXX3     ;Status Register
ULEC    = $XXX0     ;Upper Latch and Enable Counter
UL      = $XXX1     ;Upper Latch
LL      = $XXX2     ;Lower Latch
CMCR    = $XXX3     ;Counter Mode Control Register

;Program
LDA     #$mode0     ;disable Counter/Timer
STA     CMCR        ;write to mode register
LDA     #$mode      ;select mode and Prescaler and
                      IRQT enable/disable
STA     CMCR        ;write to mode register
LDA     #$lovalue   ;lower latch value
STA     LL          ;write to lower latch
LDA     #$hivalue   ;upper latch value
STA     ULEC        ;write to upper latch
                    ;clear underflow flag, and enable
                      counter
```

The following instructions is a way to change modes while the Counter/Timer is in operation:

```
LDA     #$mode      ;select desired mode, except
                      mode 0
STA     CMCR        ;write to mode register
```

The change of mode operation will take effect immediately. Thus, the Free-Run Internal Timer mode (Mode 2) could be systematically stopped by changing to the One-Shot Interval Timer mode (Mode 1). The Counter/Timer will then halt operation when the underflow condition occurs. This technique can also be used to enable or disable $\overline{IRQ}$ during program execution.

READING THE COUNTER/TIMER

To service an interrupt request, the following sequence can be used:

```
BIT     $status     ;get underflow flag
BNE     error       ;check if flag is set
LDA     $LC         ;get low counter value for overflow
LDX     $SL         ;get high counter value for overflow
                    ;underflow flag is cleared
```

By reading the LC and SL, it is possible to determine the amount of time between the interrupt request and servicing the interrupt.

To read a timer value at any time, the suggested technique is as follows:

```
LDA     $LC         ;get low counter value
                    ;upper counter transferred to
                      snapshot
        .           ;any miscellaneous code to store
        .             value if desired
LDA     $SL         ;get high counter value
```

READ/WRITE TIMING CHARACTERISTICS OF PIAT

Figure 12 is a timing diagram for the R65C24 PIAT during a Read operation (input mode). Figure 13 is a timing diagram for the PIAT during a Write operation (output mode). Table 5 shows the characteristics of the times shown in Figures 12 and 13.

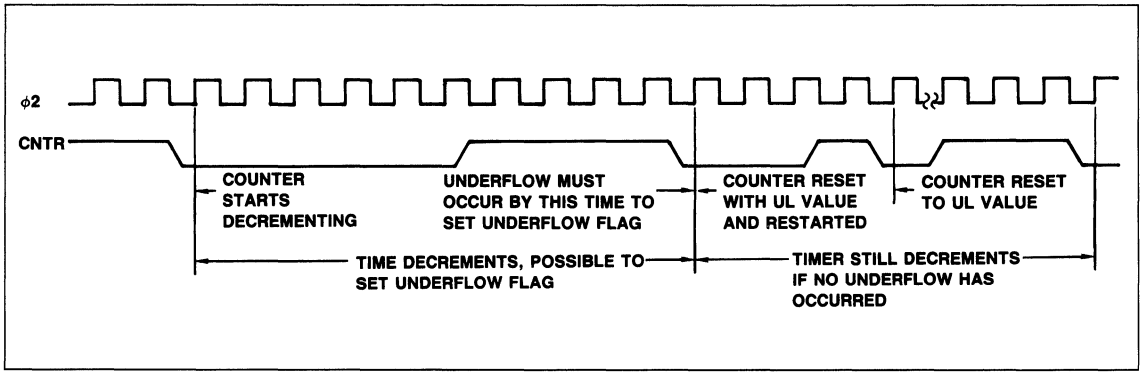


Figure 12. Mode 7—Retriggerable Interval Timer Timing

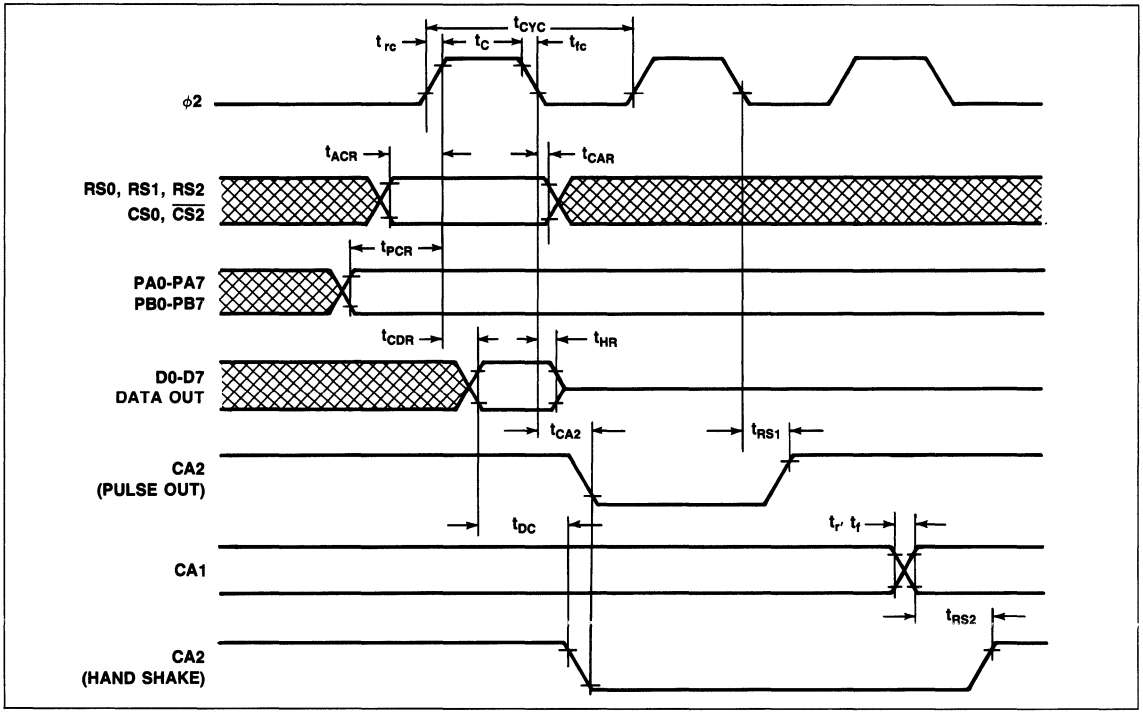


Figure 13. Read Timing Diagram

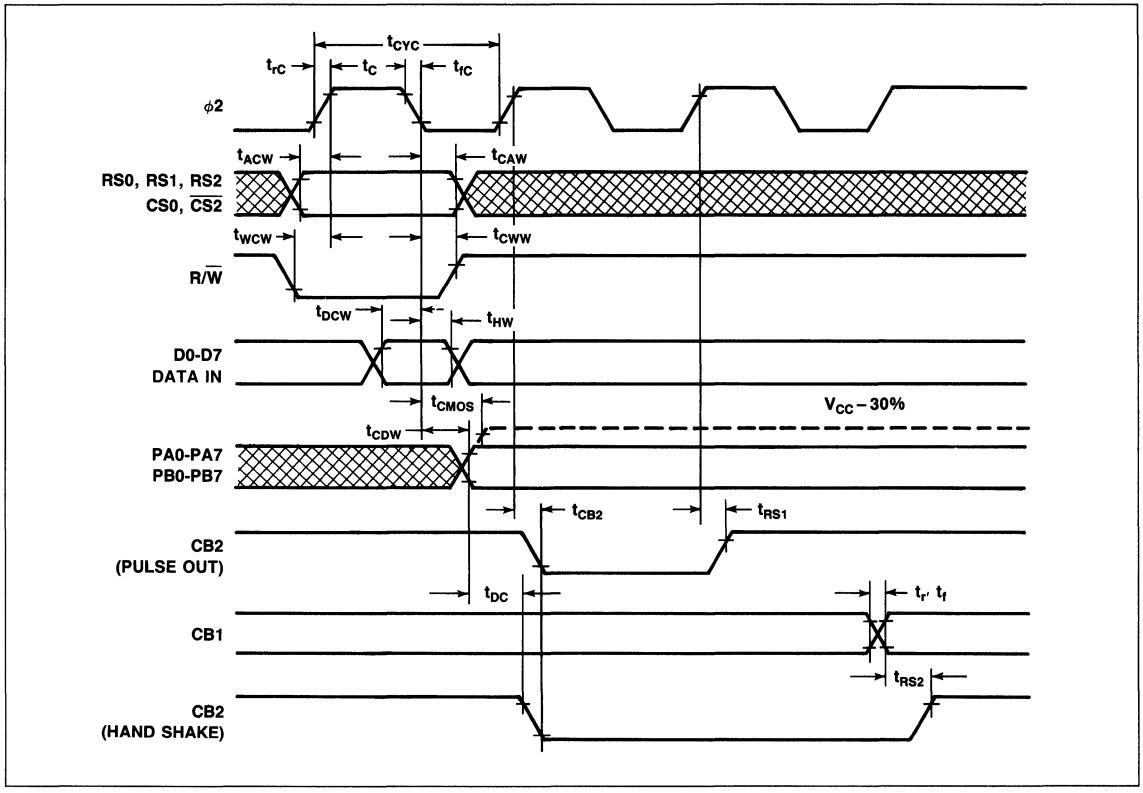


Figure 14. Write Timing Diagram

READING THE PERIPHERAL A I/O PORT

Performing a Read operation with RS1 = 0, RS0 = 0 and the Data Direction Register Access Control bit (CRA-2) = 1, directly transfers the data on the Peripheral A I/O lines to the data bus. In this situation, the data bus will contain both the input and output data. The processor must be programmed to recognize and interpret only those bits which are important to the particular peripheral operation being performed.

Since the processor always reads the Peripheral A I/O port pins instead of the actual Peripheral Output Register (ORA), it is possible for the data read by the processor to differ from the contents of the Peripheral Output Register for an output line. This is true when the I/O pin is not allowed to go to a full +2.4V DC when the Peripheral Output register contains a logic 1. In this case, the processor will read a 0 from the Peripheral A pin, even though the corresponding bit in the Peripheral Output register is a 1.

READING THE PERIPHERAL B I/O PORT

Reading the Peripheral B I/O port yields a combination of input and output data in a manner similar to the Peripheral A port. However, data is read directly from the Peripheral B Output Register (ORB) for those lines programmed to act as outputs. It is therefore possible to load down the Peripheral B Output lines without causing incorrect data to be transferred back to the processor on a Read operation.

BUS TIMING CHARACTERISTICS

Parameter	Symbol	1MHz		2MHz		3MHz		4MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
ϕ2 Cycle	T_{CYC}	1.0	—	0.5	—	0.33	—	0.25	—	μs
ϕ2 Pulse Width	t_C	450	—	220	—	160	—	110	—	ns
ϕ2 Rise and Fall Time	t_{rc}, t_{fc}	—	25	—	15	—	12	—	10	ns

READ TIMING

Address Set-Up Time	t_{ACR}	140	—	70	—	53	—	35	—	ns
Address Hold Time	t_{CAR}	0	—	0	—	0	—	0	—	ns
Peripheral Data Set-Up Time	t_{PCR}	300	—	150	—	110	—	75	—	ns
Data Bus Delay Time	t_{CDR}	—	325	—	145	—	105	—	80	ns
Data Bus Hold Time	t_{HR}	20	—	20	—	20	—	20	—	ns

WRITE TIMING

Address Set-Up Time	t_{ACW}	140	—	70	—	53	—	53	—	ns
Address Hold Time	t_{CAW}	0	—	0	—	0	—	0	—	ns
R/$\overline{W}$ Set-Up Time	t_{WCW}	180	—	90	—	67	—	45	—	ns
R/$\overline{W}$ Hold Time	t_{CWW}	0	—	0	—	0	—	0	—	ns
Data Bus Set-Up Time	t_{DCW}	180	—	90	—	67	—	45	—	ns
Data Bus Hold Time	t_{HW}	10	—	10	—	10	—	10	—	ns
Peripheral Data Delay Time	t_{CPW}	—	1.0	—	0.5	—	0.33	—	0.25	μs
Peripheral Data Delay Time to CMOS Level	t_{CMOS}	—	2.0	—	1.0	—	0.7	—	0.5	μs

PERIPHERAL INTERFACE TIMING

Parameter	Symbol	1MHz		2MHz		3MHz		4MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Peripheral Data Setup	t_{PCR}	300	—	150	—	110	—	75	—	ns
ϕ2 Low to CA2 Low Delay	t_{CA2}	—	1.0	—	0.5	—	0.33	—	0.25	μs
ϕ2 Low to CA2 High Delay	t_{RS1}	—	1.0	—	0.5	—	0.33	—	0.25	μs
CA1 Active to CA2 High Delay	t_{RS2}	—	2.0	—	1.0	—	0.67	—	0.5	μs
ϕ2 High to CB2 Low Delay	t_{CB2}	—	1.0	—	0.5	—	0.33	—	0.25	μs
Peripheral Data Valid to CB2 Low Delay	t_{DC}	0	1.5	0	0.75	0	0.5	0	0.37	μs
ϕ2 High to CB2 Hgh Delay	t_{RS1}	—	1.0	—	0.5	—	0.33	—	0.25	μs
CB1 Active to CB2 High Delay	t_{RS2}	—	2.0	—	1.0	—	0.67	—	0.5	μs
CA1, CA2, CB1 and CB2 Input Rise and Fall Time	t_r, t_f	—	1.0	—	1 0	—	1.0	—	1.0	μs

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to +7.0	Vdc
Input Voltage	V_{IN}	−0.3 to V_{CC} +0.3	Vdc
Output Voltage	V_{OUT}	−0.3 to V_{CC} +0.3	Vdc
Operating Temperature Commercial Industrial	T_A	 0 to +70 −40 to +85	°C
Storage Temperature	T_{STG}	−55 to +150	°C

*Note: Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in other sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING CONDITIONS

Parameter	Symbol	Value
Supply Voltage	Vcc	5V ±5%
Temperature Range Commercial Industrial	T_A	 0° to 70°C −40° to +85°C

DC CHARACTERISTICS

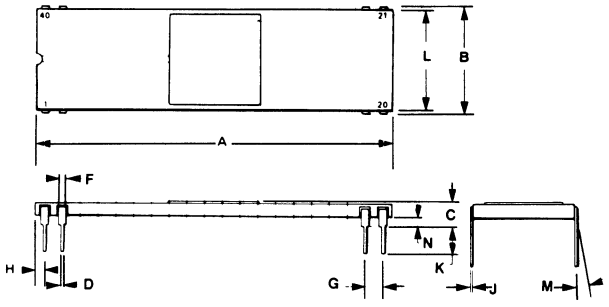
V_{CC} = 5.0V ±5%, V_{SS} = 0, T_A = T_L to T_H, (unless otherwise noted)

Parameter	Symbol	Min	Typ[3]	Max	Unit[1]	Test Conditions
Input High Voltage	V_{IH}	+2.0	—	V_{CC}	V	
Input Low Voltage	V_{IL}	−0.3	—	+0.8	V	
Input Leakage Current: R/$\overline{W}$, $\overline{RES}$, RS0, RS1, RS2, CS0, $\overline{CS2}$, CA1, CB1, ϕ2	I_{IN}	—	±1	±2.5	μA	V_{IN} = 0V to V_{CC} V_{CC} = 5.25V
Input Leakage Current for Three-State Off D0-D7, PB0-PB7, CB2	I_{TSI}	—	±2	±10	μA	V_{IN} = 0.4V to 2.4V V_{CC} = 5.25V
Input High Current PA0-PA7, CA2	I_{IH}	−200	−400	—	μA	V_{IH} = 2.4V
Input Low Current PA0-PA7, CA2	I_{IL}	—	−2	−3.2	mA	V_{IL} = 0.4V
Output High Voltage Logic PB0-PB7, CB2 (Darlington Drive)	V_{OH}	 2.4 1.5	 — —	 — —	 V V	V_{CC} = 4.75V I_{LOAD} = 200μA I_{LOAD}[2] = −3.2 mA
Output Low Voltage PA0-PA7, CA2, PB0-PB7, CB2 D0-D7, IRQ, CNTR	V_{OL}	—	—	+0.4	V	V_{CC} = 4.75V I_{LOAD} = 3.2 mA I_{LOAD} = 1.6 mA
Output High Current (Sourcing) Logic PB0-PB7, CB2 (Darlington Drive)	I_{OH}	 −200 −3.2	 −1500 −6	 — —	 μA mA	 V_{OH} = 2.4V V_{OH} = 1.5V
Output Low Current (Sinking) PA0-PA7, PB0-PB7, CB2, CA2 D0-D7, $\overline{IRQ}$, CNTR	I_{OL}	 3.2 1.6	 — —	 — —	 mA mA	V_{OL} = 0.4V
Output Leakage Current (Off State): $\overline{IRQ}$	I_{OFF}	—	1	±10	μA	V_{OH} = 2.4V V_{CC} = 5.25V
Power Dissipation	P_D	—	7	10	mW/MHz	
Input Capacitance D0–D7, PA0–PA7, PB0–PB7, CA2, CB2, CNTR R/$\overline{W}$, $\overline{RES}$, RS0, RS1, RS2, CS0, $\overline{CS2}$ CA1, CB1, ϕ2	C_{IN}	 — — —	 — — —	 10 7 20	 pF pF pF	V_{CC} = 5.0V V_{IN} = 0V f = 2 MHz T_A = 25°C
Output Capacitance	C_{OUT}	—	—	10	pF	

Notes:
1. All units are direct current (dc) except for capacitance.
2. Negative sign indicates outward current flow, positive indicates inward flow.
3. Typical values are shown for V_{CC} = 5.0V and TA = 25°C.

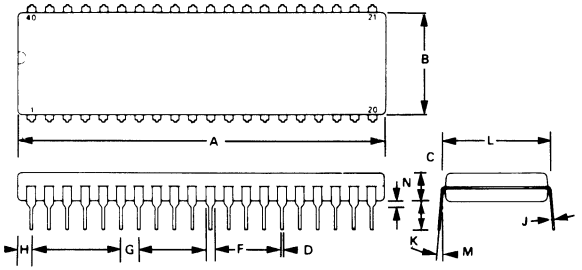
PACKAGE DIMENSIONS

40-PIN CERAMIC DIP



DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	50 29	51 31	1 980	2 020
B	14 86	15 62	0 585	0 615
C	2 54	4 19	0 100	0 165
D	0 38	0 53	0 015	0 021
F	0 76	1 40	0 030	0 055
G	2 54 BSC		0 100 BSC	
H	0 76	1 78	0 030	0 070
J	0 20	0 33	0 008	0 013
K	2 54	4 19	0 100	0 165
L	14 60	15 37	0 575	0 605
M	0°	10°	0°	10°
N	0 51	1 52	0 020	0 060

40-PIN PLASTIC DIP



DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	51 28	52 32	2 040	2 060
B	13 72	14 22	0 540	0 560
C	3 55	5 08	0 140	0 200
D	0 36	0 51	0 014	0 020
F	1 02	1 52	0 040	0 060
G	2 54 BSC		0 100 BSC	
H	1 65	2 16	0 065	0 085
J	0 20	0 30	0 008	0 012
K	3 05	3 56	0 120	0 140
L	15 24 BSC		0 600 BSC	
M	7°	10°	7°	10°
N	0 51	1 02	0 020	0 040

R65C51
ASYNCHRONOUS COMMUNICATIONS INTERFACE ADAPTER (ACIA)

PRELIMINARY

DESCRIPTION

The Rockwell CMOS R65C51 Asynchronous Communications Interface Adapter (ACIA) provides an easily implemented, program controlled interface between 8-bit microprocessor-based systems and serial communication data sets and modems.

The ACIA has an internal baud rate generator. This feature eliminates the need for multiple component support circuits, a crystal being the only other part required. The Transmitter baud rate can be selected under program control to be either 1 of 15 different rates from 50 to 19,200 baud, or at $^1/_{16}$ times an external clock rate. The Receiver baud rate may be selected under program control to be either the Transmitter rate, or at $^1/_{16}$ times the external clock rate. The ACIA has programmable word lengths of 5, 6, 7, or 8 bits; even, odd, or no parity; 1, 1½, or 2 stop bits.

The ACIA is designed for maximum programmed control from the microprocessor (MPU), to simplify hardware implementation. Three separate registers permit the MPU to easily select the R65C51's operating modes and data checking parameters and determine operational status.

The Command Register controls parity, receiver echo mode, transmitter interrupt control, the state of the $\overline{RTS}$ line, receiver interrupt control, and the state of the $\overline{DTR}$ line.

The Control Register controls the number of stop bits, word length, receiver clock source, and baud rate.

The Status Register indicates the states of the $\overline{IRQ}$, $\overline{DSR}$, and $\overline{DCD}$ lines, Transmitter and Receiver Data Registers, and Overrun, Framing, and Parity Error conditions.

The Transmitter and Receiver Data Registers are used for temporary data storage by the ACIA Transmit and Receiver circuits.

ORDERING INFORMATION

Part No.: R65C51

- Temperature Range (T_L to T_H):
  - Blank = 0°C to +70°C
  - E = −40°C to +85°C
- Frequency Range:
  - 1 = 1 MHz
  - 2 = 2 MHz
- Package:
  - C = Ceramic
  - P = Plastic

FEATURES

- Low power CMOS N-well silicon gate technology
- Direct replacement for NMOS R6551 ACIA
- Full duplex operation with buffered receiver and transmitter
- Data set/modem control functions
- Internal baud rate generator with 15 programmable baud rates (50 to 19,200)
- Program-selectable internally or externally controlled receiver rate
- Programmable word lengths, number of stop bits, and parity bit generation and detection
- Programmable interrupt control
- Program reset
- Program-selectable serial echo mode
- Two chip selects
- 1 or 2 MHz operation
- 5.0 Vdc ± 5% supply requirements
- 28-pin plastic or ceramic DIP
- Full TTL compatibility
- Compatible with R6500, R6500/* and R65C00 microprocessors

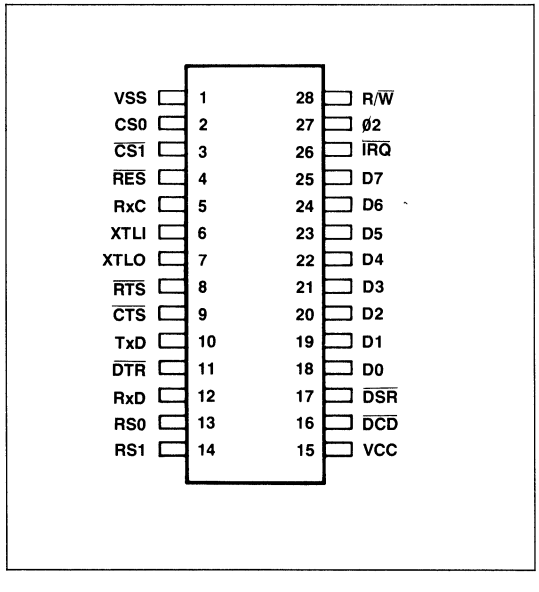


Figure 1. R65C51 ACIA Pin Configuration

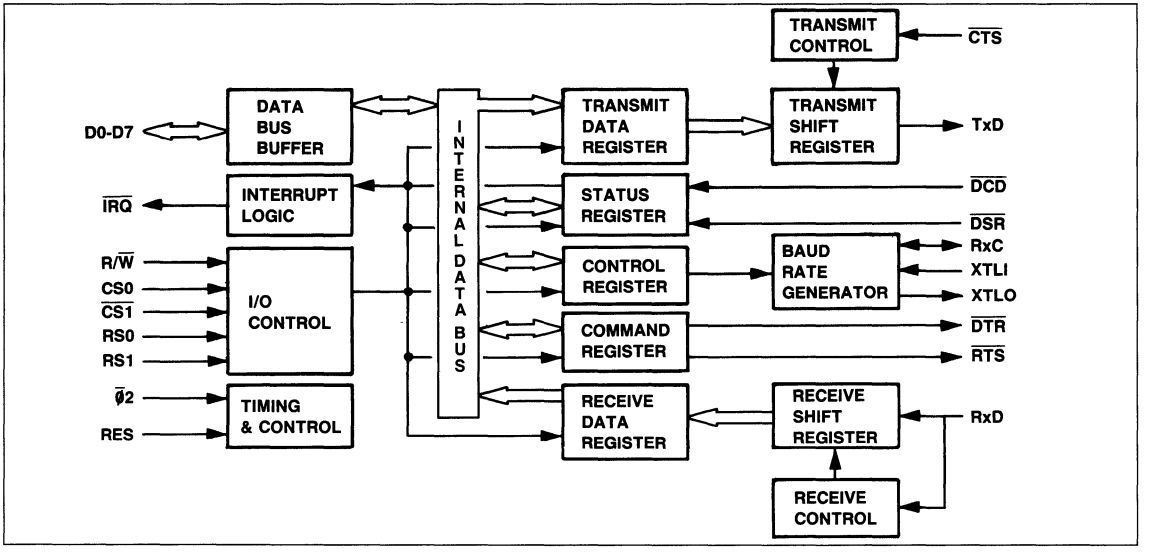


Figure 2. ACIA Internal Organization

FUNCTIONAL DESCRIPTION

A block diagram of the ACIA is presented in Figure 2 followed by a description of each functional element of the device.

DATA BUS BUFFERS

The Data Bus Buffer interfaces the system data lines to the internal data bus. The Data Bus Buffer is bi-directional. When the R/$\overline{W}$ line is low and the chip is selected, the Data Bus Buffer writes the data from the system data lines to the ACIA internal data bus. When the R/$\overline{W}$ line is high and the chip is selected, the Data Bus Buffer drives the data from the internal data bus to the system data bus.

INTERRUPT LOGIC

The Interrupt Logic will cause the $\overline{IRQ}$ line to the microprocessor to go low when conditions are met that require the attention of the microprocessor. The conditions which can cause an interrupt will set bit 7 and the appropriate bit of bits 3 through 6 in the Status Register, if enabled. Bits 5 and 6 correspond to the Data Carrier Detect ($\overline{DCD}$) logic and the Data Set Ready ($\overline{DSR}$) logic. Bits 3 and 4 correspond to the Receiver Data Register full and the Transmitter Data Register empty conditions. These conditions can cause an interrupt request if enabled by the Command Register.

I/O CONTROL

The I/O Control Logic controls the selection of internal registers in preparation for a data transfer on the internal data bus and the direction of the transfer to or from the register.

The registers are selected by the Receiver Select (RS1, RS0) and Read/Write (R/$\overline{W}$) lines as described later in Table 1.

TIMING AND CONTROL

The Timing and Control logic controls the timing of data transfers on the internal data bus and the registers, the Data Bus Buffer, and the microprocessor data bus, and the hardware reset features.

Timing is controlled by the system Ø2 clock input. The chip will perform data transfers to or from the microcomputer data bus during the Ø2 high period when selected.

All registers will be initialized by the Timing and Control Logic when the Reset ($\overline{RES}$) line goes low. See the individual register description for the state of the registers following a hardware reset.

TRANSMITTER AND RECEIVER DATA REGISTERS

These registers are used as temporary data storage for the ACIA Transmit and Receive Circuits. Both the Transmitter and Receiver are selected by a Register Select 0 (RS0) and Register Select 1 (RS1) low condition. The Read/Write (R/$\overline{W}$) line determines which actually uses the internal data bus; the Transmitter Data Register is write only and the Receiver Data Register is read only.

Bit 0 is the first bit to be transmitted from the Transmitter Data Register (least significant bit first). The higher order bits follow in order. Unused bits in this register are "don't care".

The Receiver Data Register holds the first received data bit in bit 0 (least significant bit first). Unused high-order bits are "0". Parity bits are not contained in the Receiver Data Register. They are stripped off after being used for parity checking.

STATUS REGISTER

The Status Register indicates the state of interrupt conditions and other non-interrupt status lines. The interrupt conditions are the Data Set Ready, Data Carrier Detect, Transmitter Data Register Empty and Receiver Data Register Full as reported in bits 6 through 3, respectively. If any of these bits are set, the Interrupt (IRQ) indicator (bit 7) is also set. Overrun, Framing Error, and Parity Error are also reported (bits 2 through 0 respectively).

7	6	5	4	3	2	1	0
IRQ	$\overline{DSR}$	$\overline{DCD}$	TDRE	RDRE	OVRN	FE	PE

Bit 7 Interrupt (IRQ)
0 No interrupt
1 Interrupt has occurred

Bit 6 Data Set Ready (DSR)
0 DSR low (ready)
1 DSR high (not ready)

Bit 5 Data Carrier Detect (DCD)
0 DCD low (detected)
1 DCD high (not detected)

Bit 4 Transmitter Data Register Empty
0 Not empty
1 Empty

Bit 3 Receiver Data Register Full
0 Not full
1 Full

Bit 2 Overrun*
0 No overrun
1 Overrun has occurred

Bit 1 Framing Error*
0 No framing error
1 Framing error detected

Bit 0 Parity Error*
0 No parity error
1 Parity error detected

*No interrupt occurs for these conditions

Reset Initialization

7	6	5	4	3	2	1	0	
0	—	—	1	0	0	0	0	**Hardware reset**
—	—	—	—	—	0	—	—	**Program reset**

Parity Error (Bit 0), Framing Error (Bit 1), and Overrun (2)

None of these bits causes a processor interrupt to occur, but they are normally checked at the time the Receiver Data Register is read so that the validity of the data can be verified. These bits are self clearing (i.e., they are automatically cleared after a read of the Receiver Data Register).

Receiver Data Register Full (Bit 3)

This bit goes to a 1 when the ACIA transfers data from the Receiver Shift Register to the Receiver Data Register, and goes to a 0 (is cleared) when the processor reads the Receiver Data Register.

Transmitter Data Register Empty (Bit 4)

This bit goes to a 1 when the ACIA transfers data from the Transmitter Data Register to the Transmitter Shift Register, and goes to a 0 (is cleared) when the processor writes new data onto the Transmitter Data Register.

Data Carrier Detect (Bit 5) and Data Set Ready (Bit 6)

These bits reflect the levels of the $\overline{DCD}$ and $\overline{DSR}$ inputs to the ACIA. A 0 indicates a low level (true condition) and a 1 indicates a high level (false). Whenever either of these inputs change state, an immediate processor interrupt (IRQ) occurs, unless bit 1 of the Command Register (IRD) is set to a 1 to disable $\overline{IRQ}$. When the interrupt occurs, the status bits indicate the levels of the inputs immediately after the change of state occurred. Subsequent level changes will not affect the status bits until the Status Register is interrogated by the processor. At that time, another interrupt will immediately occur and the status bits reflect the new input levels. These bits are not automatically cleared (or reset) by an internal operation.

Interrupt (Bit 7)

This bit goes to a 1 whenever an interrupt condition occurs and goes to a 0 (is cleared) when the Status Register is read.

CONTROL REGISTER

The Control Register selects the desired baud rate, frequency source, word length, and the number of stop bits.

7	6	5	4	3	2	1	0
SBN	WL		RCS	SBR			
	WL1	WL0		SBR3	SBR2	SBR1	SBR0

Bit 7 Stop Bit Number (SBN)

0	1 Stop bit
1	2 Stop bits
1	1½ Stop bits For WL = 5 and no parity
1	1 Stop bit For WL = 8 and parity

Bits 6-5 Word Length (WL)

6	5	No. Bits
0	0	8
0	1	7
1	0	6
1	1	5

Bit 4 Receiver Clock Source (RCS)

0	External receiver clock
1	Baud rate

Bits 3-0 Selected Baud Rate (SBR)

3	2	1	0	Baud
0	0	0	0	16x
0	0	0	1	50
0	0	1	0	75
0	0	1	1	109.92
0	1	0	0	134.58
0	1	0	1	150
0	1	1	0	300
0	1	1	1	600
1	0	0	0	1200
1	0	0	1	1800
1	0	1	0	2400
1	0	1	1	3600
1	1	0	0	4800
1	1	0	1	7200
1	1	1	0	9600
1	1	1	1	19,200

Reset Initialization

7	6	5	4	3	2	1	0	
0	0	0	0	0	0	0	0	Hardware reset ($\overline{RES}$)
–	–	–	–	–	–	–	–	Program reset

Selected Baud Rate (Bits 0, 1, 2, 3)

These bits select the Transmitter baud rate, which can be at $^1/_{16}$ an external clock rate or one of 15 other rates controlled by the internal baud rate generator.

If the Receiver clock uses the same baud rate as the transmitter, then RxC becomes an output and can be used to slave other circuits to the ACIA. Figure 3 shows the Transmitter and Receiver layout.

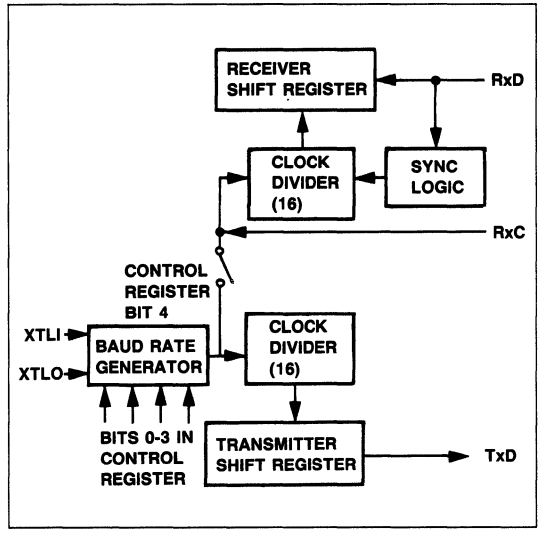


Figure 3. Transmitter/Receiver Clock Circuits

Receiver Clock Source (Bit 4)

This bit controls the clock source to the Receiver. A 0 causes the Receiver to operate at a baud rate of $^1/_{16}$ an external clock. A 1 causes the Receiver to operate at the same baud rate as is selected for the transmitter.

Word Length (Bits 5, 6)

These bits determine the word length to be used (5, 6, 7 or 8 bits).

Stop Bit Number (Bit 7)

This bit determines the number of stop bits used. A 0 always indicates one stop bit. A 1 indicates 1½ stop bits if the word length is 5 with no parity selected, 1 stop bit if the word length is 8 with parity selected, and 2 stop bits in all other configurations.

COMMAND REGISTER

The Command Register controls specific modes and functions.

7	6	5	4	3	2	1	0
PMC		PME	REM	TIC		IRD	DTR
PNC1	PNC0			TIC1	TIC0		

Bits 7-6 Parity Mode Control (PMC)

7	6	
0	0	Odd parity transmitted/received
0	1	Even parity transmitted/received
1	0	Mark parity bit transmitted Parity check disabled
1	1	Space parity bit transmitted Parity check disabled

Bit 5 Parity Mode Enabled (PME)

0	Parity mode disabled No parity bit generated Parity check disabled
1	Parity mode enabled

Bit 4 Receiver Echo Mode (REM)

0	Receiver normal mode
1	Receiver echo mode bits 2 and 3 Must be zero for receiver echo mode, $\overline{RTS}$ will be low.

Bits 3-2 Transmitter Interrupt Control (TIC)

3	2	
0	0	$\overline{RTS}$ = High, transmitter disabled
0	1	$\overline{RTS}$ = Low, transmit interrupt enabled
1	0	$\overline{RTS}$ = Low, transmit interrupt disabled
1	1	$\overline{RTS}$ = Low, transmit interrupt disabled transmit break on TxD

Bit 1 Receiver Interrupt Request Disabled (IRD)

0	$\overline{IRQ}$ enabled (receiver)
1	$\overline{IRQ}$ disabled (receiver)

Bit 0 Data Terminal Ready (DTR)

0	Data terminal not ready ($\overline{DTR}$ high)*
1	Data terminal ready ($\overline{DTR}$ low)

NOTE

*The transmitter is disabled immediately. The receiver is disabled but will first complete receiving a byte in process of being received.

Data Terminal Ready (Bit 0)

This bit enables all selected interrupts and controls the state of the Data Terminal Ready ($\overline{DTR}$) line. A 0 indicates the microcomputer system is not ready by setting the $\overline{DTR}$ line high. A 1 indicates the microcomputer system is ready by setting the $\overline{DTR}$ line low. $\overline{DTR}$ line low. $\overline{DTR}$ also enables and disables the transmitter and receiver.

Receiver Interrupt Control (Bit 1)

This bit disables the Receiver from generating an interrupt when set to a 1. The Receiver interrupt is enabled when this bit is set to a 0 and Bit 0 is set to a 1.

Transmitter Interrupt Control (Bits 2, 3)

These bits control the state of the Ready to Send ($\overline{RTS}$) line and the Transmitter interrupt.

Receiver Echo Mode (Bit 4)

A 1 enables the Receiver Echo Mode and a 0 disables the Receiver Echo Mode. When bit 4 is a 1 bits 2 and 3 must be 0. In the Receiver Echo Mode, the Transmitter returns each transmission received by the Receiver delayed by one-half bit time.

Parity Mode Enable (Bit 5)

This bit enables parity bit generation and checking. A 0 disables parity bit generation by the Transmitter and parity bit checking by the Receiver. A 1 bit enables generation and checking of parity bits.

Parity Mode Control (Bits 6, 7)

These bits determine the type of parity generated by the Transmitter, (even, odd, mark or space) and the type of parity check done by the Receiver (even, odd, or no check).

Reset Initialization

7	6	5	4	3	2	1	0	
0	0	0	0	0	0	0	0	**Hardware reset ($\overline{RES}$)**
—	—	—	0	0	0	0		**Program reset**

INTERFACE SIGNALS

Figure 4 shows the ACIA interface signals associated with the microprocessor and the modem.

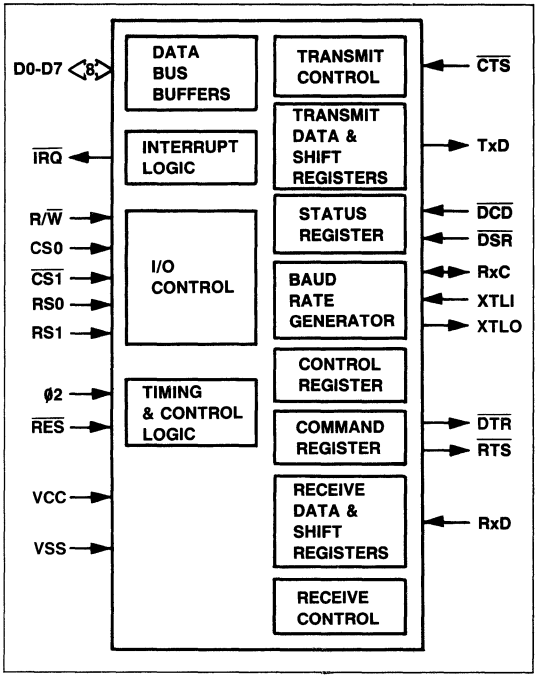


Figure 4. ACIA Interface Diagram

MICROPROCESSOR INTERFACE

Reset ($\overline{RES}$)

During system initialization a low on the $\overline{RES}$ input causes a hardware reset to occur. Upon reset, the Command Register and the Control Register are cleared (all bits set to 0). The Status Register is cleared with the exception of the indications of Data Set Ready and Data Carrier Detect, which are externally controlled by the $\overline{DSR}$ and $\overline{DCD}$ lines, and the transmitter Empty bit, which is set. $\overline{RES}$ must be held low for one ø2 clock cycle for a reset to occur.

Input Clock (ø2)

The input clock is the system ø2 clock and clocks all data transfers between the system microprocessor and the ACIA.

Read/Write (R/$\overline{W}$)

The R/$\overline{W}$ input, generated by the microprocessor controls the direction of data transfers. A high on the R/$\overline{W}$ pin allows the processor to read the data supplied by the ACIA, a low allows a write to the ACIA.

Interrupt Request ($\overline{IRQ}$)

The $\overline{IRQ}$ pin is an interrupt output from the interrupt control logic. It is an open drain output, permitting several devices to be connected to the common $\overline{IRQ}$ microprocessor input. Normally a high level, $\overline{IRQ}$ goes low when an interrupt occurs.

Data Bus (D0-D7)

The eight data line (D0-D7) pins transfer data between the processor and the ACIA. These lines are bi-directional and are normally high-impedance except during Read cycles when the ACIA is selected.

Chip Selects (CS0, $\overline{CS1}$)

The two chip select inputs are normally connected to the processor address lines either directly or through decoders. The ACIA is selected when CS0 is high and $\overline{CS1}$ is low. When the ACIA is selected, the internal registers are addressed in accordance with the register select lines (RS0, RS1).

Register Selects (RS0, RS1)

The two register select lines are normally connected to the processor address lines to allow the processor to select the various ACIA internal registers. Table 1 shows the internal register select coding.

Table 1. ACIA Register Selection

		Register Operation	
RS1	RS0	R/$\overline{W}$ = Low	R/$\overline{W}$ = High
L	L	Write Transmit Data Register	Read Receiver Data Register
L	H	Programmed Reset (Data is "Don't Care")	Read Status Register
H	L	Write Command Register	Read Command Register
H	H	Write Control Register	Read Control Register

Only the Command and Control registers can both be read and written. The programmed Reset operation does not cause any data transfer, but is used to clear bits 4 through 0 in the Command register and bit 2 in the Status Register. The Control Register is unchanged by a programmed Reset. It should be noted that the programmed Reset is slightly different from the hardware Reset ($\overline{RES}$); refer to the register description.

ACIA/MODEM INTERFACE

Crystal Pins (XTLI, XTLO)

These pins are normally directly connected to the parallel mode external crystal (1.8432 MHz) to derive the various baud rates. Alternatively, an externally generated clock can drive the XTLI pin, in which case the XTLO pin must float. XTLI is the input pin for the transmit clock.

Transmit Data (TxD)

The TxD output line transfers serial nonreturn-to-zero (NRZ) data to the modem. The least significant bit (LSB) of the Transmit Data Register is the first data bit transmitted and the rate of data transmission is determined by the baud rate selected or under control of an external clock. This selection is made by programming the Control Register.

Receive Data (RxD)

The RxD input line transfers serial NRZ data into the ACIA from the modem, LSB first. The receiver data rate is either the programmed baud rate or under the control of an externally generated receiver clock. The selection is made by programming the Control Register.

Receive Clock (RxC)

The RxC is a bi-directional pin which is either the receiver 16x clock input or the receiver 16x clock output. The latter mode results if the internal baud rate generator is selected for receiver data clocking.

Request to Send ($\overline{RTS}$)

The $\overline{RTS}$ output pin controls the modem from the processor. The state of the $\overline{RTS}$ pin is determined by the contents of the Command Register.

Clear to Send ($\overline{CTS}$)

The $\overline{CTS}$ input pin controls the transmitter operation. The enable state is with $\overline{CTS}$ low. The transmitter is automatically disabled if $\overline{CTS}$ is high.

Data Terminal Ready ($\overline{DTR}$)

This output pin indicates the status of the ACIA to the modem. A low on $\overline{DTR}$ indicates the ACIA is enabled, a high indicates it is disabled. The processor controls this pin via bit 0 of the Command Register.

Data Set Ready ($\overline{DSR}$)

The $\overline{DSR}$ input pin indicates to the ACIA the status of the modem. A low indicates the "ready" state and a high, "not-ready."

Data Carrier Detect ($\overline{DCD}$)

The $\overline{DCD}$ input pin indicates to the ACIA the status of the carrier-detect output of the modem. A low indicates that the modem carrier signal is present and a high, that it is not.

TRANSMITTER AND RECEIVER OPERATION

Continuous Data Transmit

In the normal operating mode, the interrupt request output ($\overline{IRQ}$) signals when the ACIA is ready to accept the next data word to be transmitted. This interrupt occurs at the beginning of the Start Bit. When the processor reads the Status Register of the ACIA, the interrupt is cleared.

The processor must then identify that the Transmit Data Register is ready to be loaded and must then load it with the next data word. This must occur before the end of the Stop Bit, otherwise a continuous "MARK" will be transmitted. Figure 5 shows the continuous Data Transmit timing relationship.

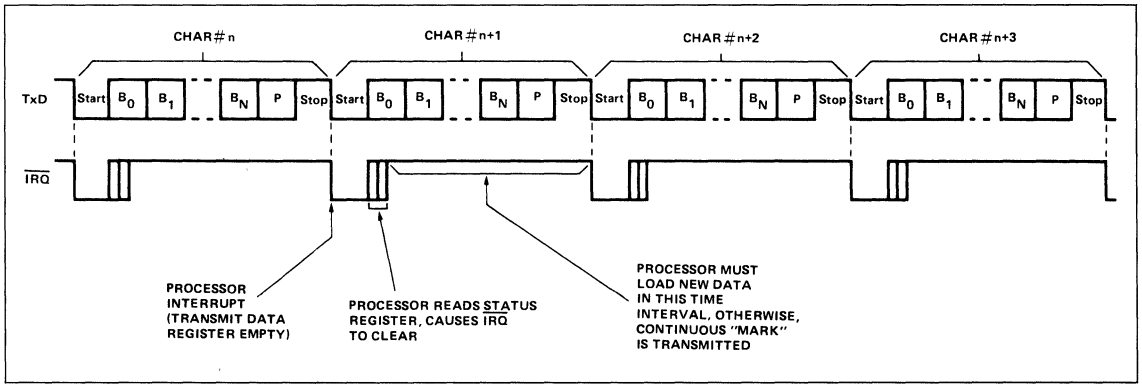


Figure 5. Continuous Data Transmit

Continuous Data Receive

Similar to the Continuous Data Transmit case, the normal operation of this mode is to assert $\overline{IRQ}$ when the ACIA has received a full data word. This occurs at about $^{9}/_{16}$ point through the Stop Bit. The processor must read the Status Register and read the data word before the next interrupt, otherwise the Overrun condition occurs. Figure 6 shows the continuous Data Receive Timing Relationship.

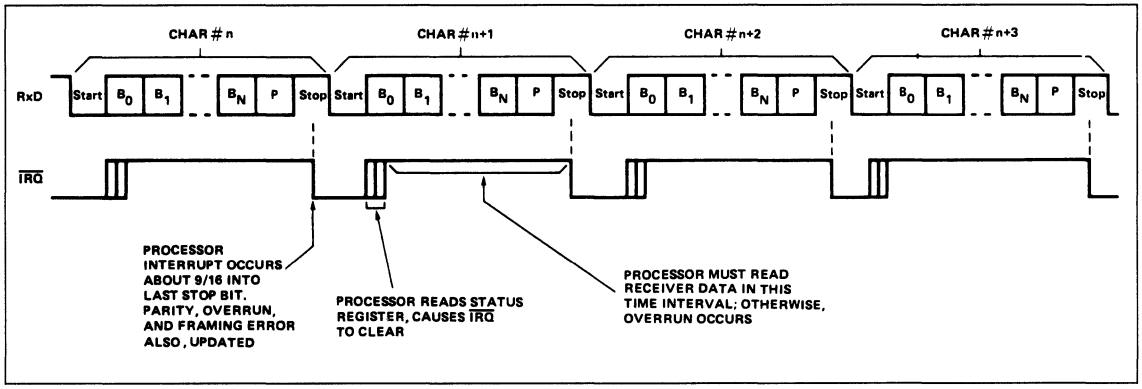


Figure 6. Continuous Data Receive

Transmit Data Register Not Loaded by Processor

If the processor is unable to load the Transmit Data Register in the allocated time, then the TxD line goes to the "MARK" condition until the data is loaded. $\overline{IRQ}$ interrupts continue to occur at the same rate as previously, except no data is transmitted. When the processor finally loads new data, a Start Bit immediately occurs, the data word transmission is started, and another interrupt is initiated, signaling for the next data word. Figure 7 shows the timing relationship for this mode of operation.

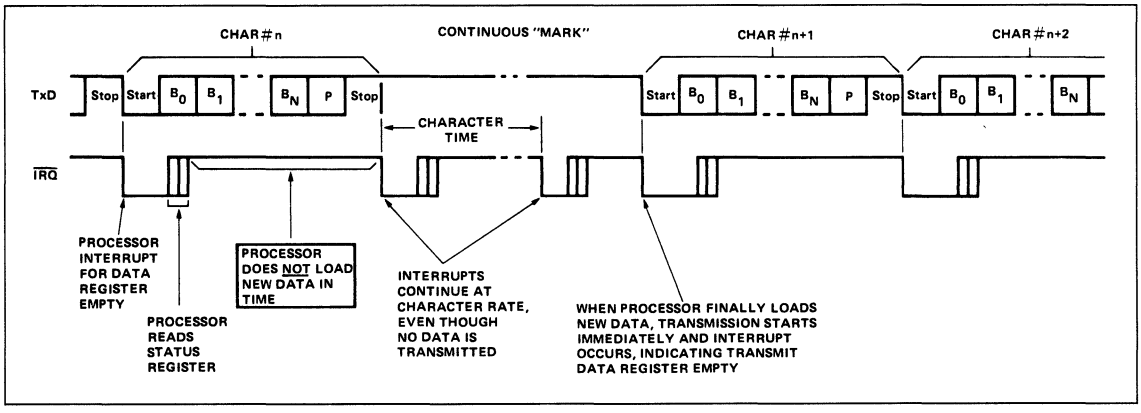


Figure 7. Transmit Data Register Not Loaded by Processor

Effect of $\overline{CTS}$ on Transmitter

$\overline{CTS}$ is the Clear-to-Send signal generated by the modem. It is normally low (true state) but may go high in the event of some modem problems. When this occurs, the TxD line goes to the "MARK" condition after the entire last character (including parity and stop bit) have been transmitted. Bit 4 in the Status Register indicates that the Transmitter Data Register is not empty and $\overline{IRQ}$ is *not* asserted. $\overline{CTS}$ is a transmit control line only, and has no effect on the ACIA Receiver Operation. Figure 8 shows the timing relationship for this mode of operation.

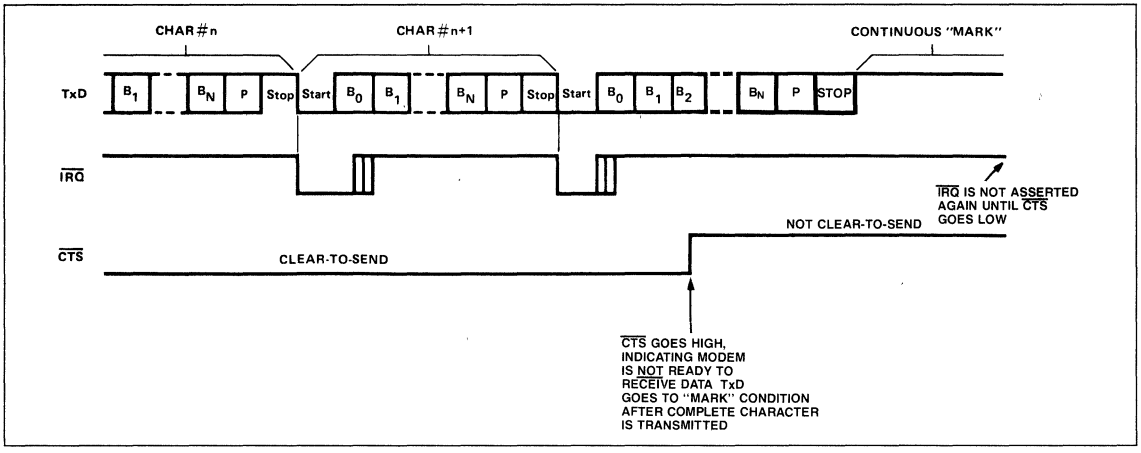


Figure 8. Effect of CTS on Transmitter

Effect of Overrun on Receiver

If the processor does not read the Receiver data Register in the allocated time, then, when the following interrupt occurs, the new data word is not transferred to the Receiver Data Register, but the Overrun status bit is set. Thus, the Data Register will contain the last valid data word received and all following data is lost. Figure 9 shows the timing relationship for this mode.

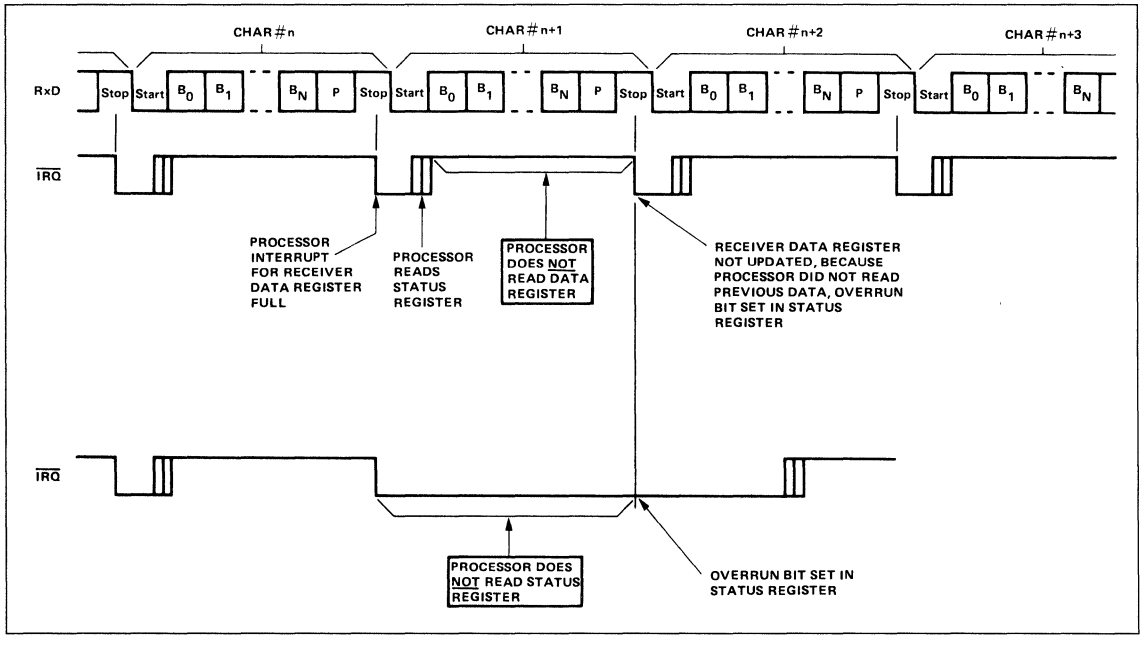


Figure 9. Effect of Overrun on Receiver

Echo Mode Timing

In Echo Mode, the TxD line re-transmits the data on the RxD line, delayed by ½ of the bit time, as shown in Figure 10.

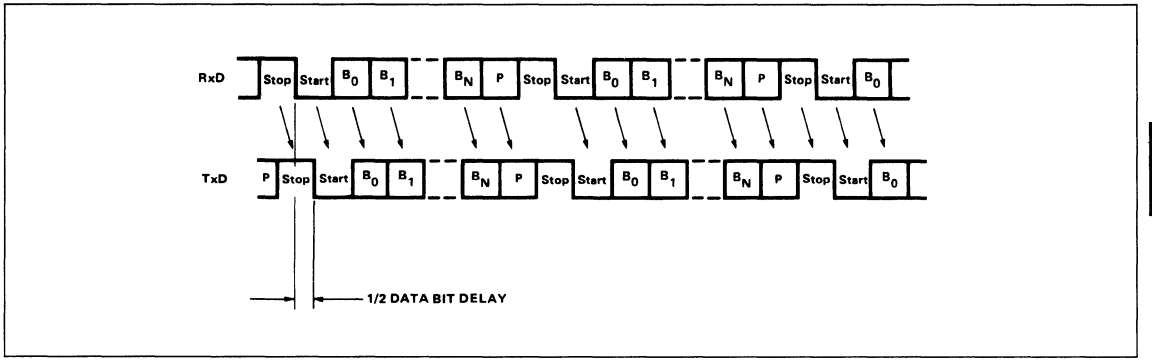


Figure 10. Echo Mode Timing

Effect of $\overline{CTS}$ on Echo Mode Operation

In Echo Mode, the Receiver operation is unaffected by $\overline{CTS}$, however, the Transmitter is affected when $\overline{CTS}$ goes high, i.e., the TxD line immediately goes to a continuous "MARK" condition. In this case, however, the Status Request indicates that the Receiver Data Register is full in response to an $\overline{IRQ}$, so the processor has no way of knowing that the Transmitter has ceased to echo. See Figure 11 for the timing relationship of this mode.

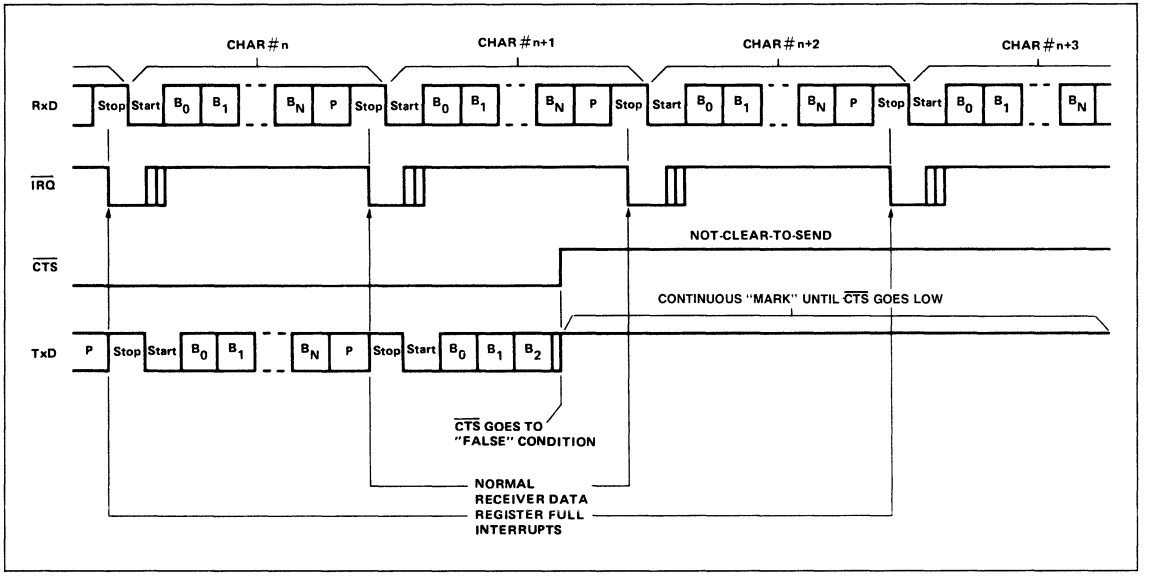


Figure 11. Effect of $\overline{CTS}$ on Echo Mode

Overrun in Echo Mode

If Overrun occurs in Echo Mode, the Receiver is affected the same way as a normal overrun in Receive Mode. For the re-transmitted data, when overrun occurs, the TxD line goes to the "MARK" condition until the first Start Bit after the Receiver Data Register is read by the processor. Figure 12 shows the timing relationship for this mode.

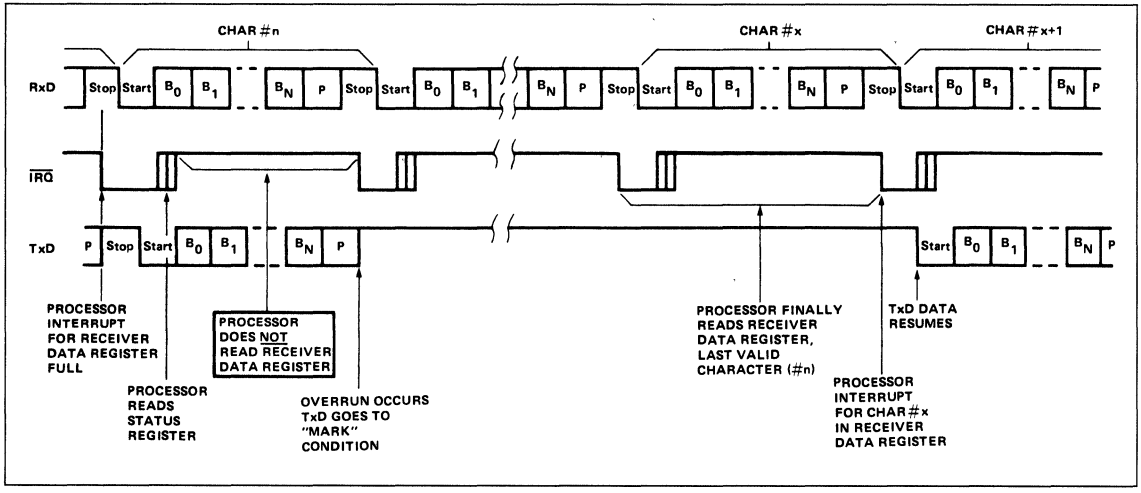


Figure 12. Overrun in Echo Mode

Framing Error

Framing Error is caused by the absence of Stop Bit(s) on received data. A Framing Error is indicated by the setting of bit 4 in the Status Register at the same time the Receiver Data Register Full bit is set, also in the Status Register. In response to $\overline{IRQ}$, generated by RDRF, the Status Register can also be checked for the Framing Error. Subsequent data words are tested for Framing Error separately, so the status bit will always reflect the last data word received. See Figure 13 for Framing Error timing relationship.

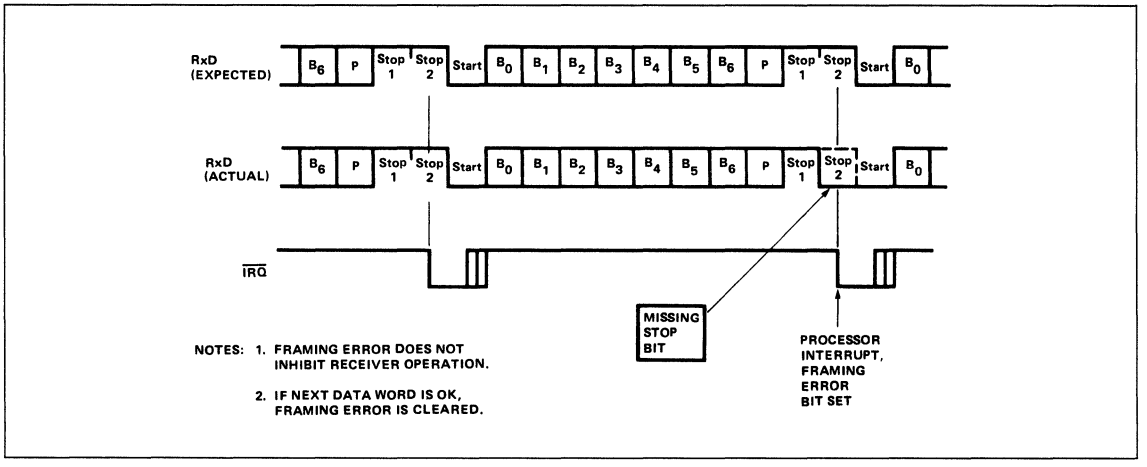


Figure 13. Framing Error

Effect of $\overline{DCD}$ on Receiver

$\overline{DCD}$ is a modem output indicating the status of the carrier-frequency-detection circuit of the modem. This line goes high for a loss of carrier. Normally, when this occurs, the modem will stop transmitting data some time later. The ACIA asserts $\overline{IRQ}$ whenever $\overline{DCD}$ changes state and indicates this condition via bit 5 in the Status Register.

Once such a change of state occurs, subsequent transitions will not cause interrupts or changes in the Status Register until the first interrupt is serviced. When the Status Register is read by the processor, the ACIA automatically checks the level of the $\overline{DCD}$ line, and if it has changed, another $\overline{IRQ}$ occurs (see Figure 14).

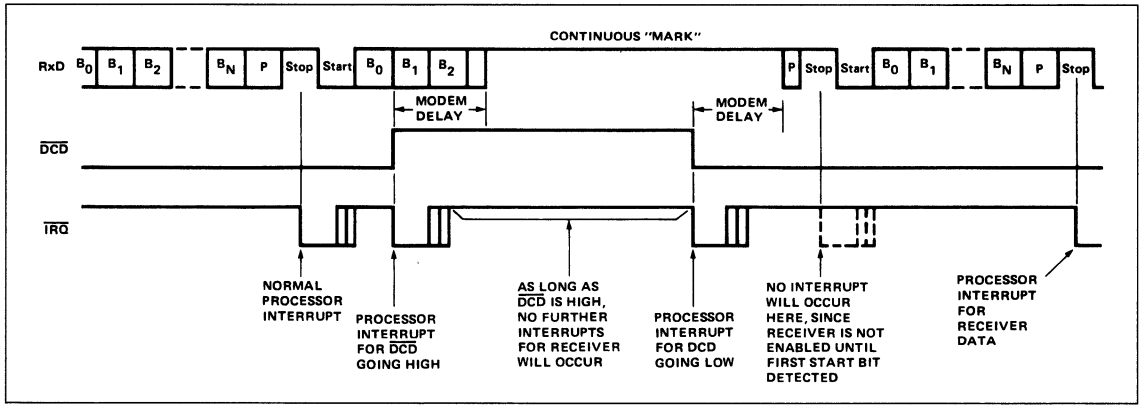


Figure 14. Effect of $\overline{DCD}$ on Receiver

Timing with 1½ Stop Bits

It is possible to select 1½ Stop Bits, but this occurs only for 5-bit data words with no parity bit. In this case, the $\overline{IRQ}$ asserted for Receiver Data Register Full occurs halfway through the trailing half-Stop Bit. Figure 15 shows the timing relationship for this mode.

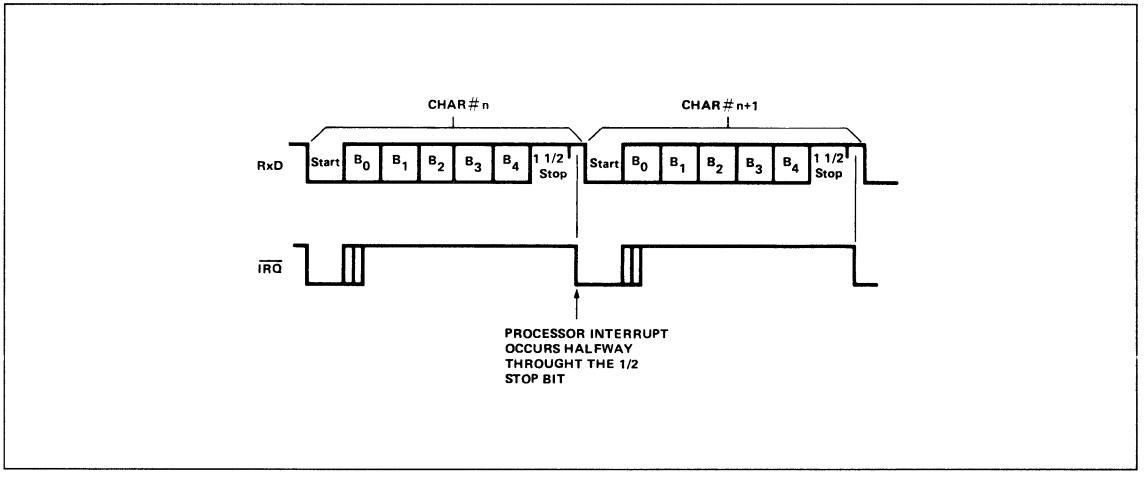


Figure 15. Timing with 1½ Stop Bits

Transmit Continuous "BREAK"

This mode is selected via the ACIA Command Register and causes the Transmitter to send continuous "BREAK" characters, beginning with the next character transmitted. At least one full "BREAK" character will be transmitted, even if the processor quickly re-programs the Command Register transmit mode. Later, when the Command Register is programmed back to normal transmit mode, an immediate Stop Bit will be generated and transmission will resume. Figure 16 shows the timing relationship for this mode.

Note

If, while operating in the Transmit Continuous "BREAK" mode, the $\overline{CTS}$ should go to a high, the TxD will be overridden by the $\overline{CTS}$ and will go to continuous "MARK" at the beginning of the next character transmitted after the $\overline{CTS}$ goes high.

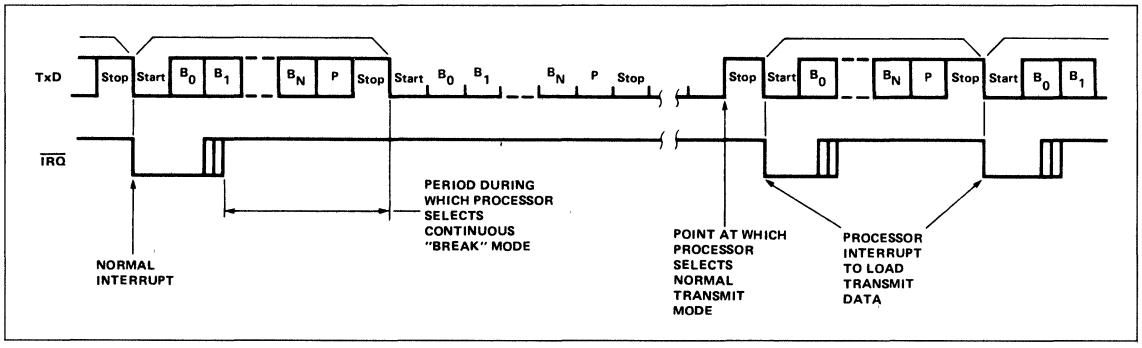


Figure 16. Transmit Continuous "BREAK"

Receive Continuous "BREAK"

In the event the modem transmits continuous "BREAK" characters, the ACIA will terminate receiving. Reception will resume only after a Stop Bit is encountered by the ACIA. Figure 17 shows the timing relationship for continuous "BREAK" characters.

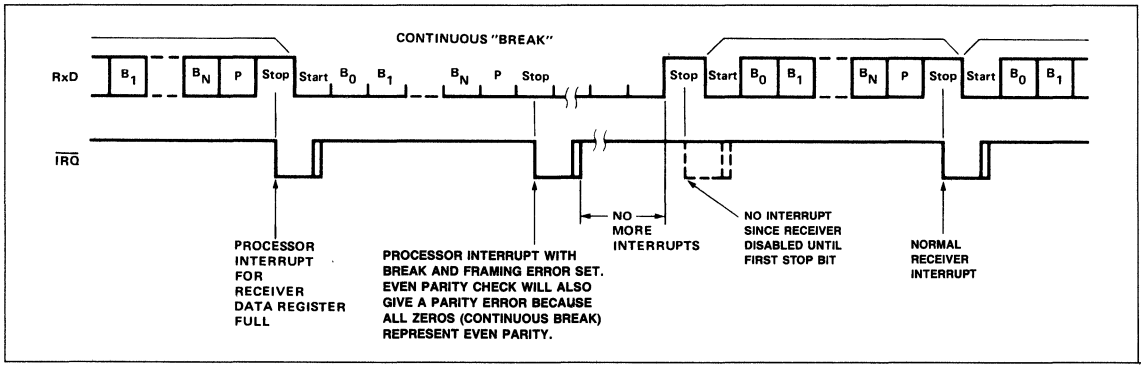


Figure 17. Receive Continuous "BREAK"

STATUS REGISTER OPERATION

Because of the special functions of the various status bits, there is a suggested sequence for checking them. When an interrupt occurs, the ACIA should be interrogated, as follows:

1. Read Status Register

   This operation automatically clears Bit 7 ($\overline{IRQ}$). Subsequent transitions on $\overline{DSR}$ and $\overline{DCD}$ will cause another interrupt

2. Check $\overline{IRQ}$ (Bit 7) in the data read from the Status Register

   If not set, the interrupt source is not the ACIA.

3. Check $\overline{DCD}$ and $\overline{DSR}$

   These must be compared to their previous levels, which must have been saved by the processor. If they are both 0 (modem "on-line") and they are unchanged then the remaining bits must be checked

4. Check RDRF (Bit 3)

   Check for Receiver Data Register Full.

5. Check Parity, Overrun, and Framing Error (Bits 0-2) if the Receiver Data Register is full

6. Check TDRE (Bit 4)

   Check for Transmitter Data Register Empty.

7. If none of the above conditions exist, then $\overline{CTS}$ must have gone to the false (high) state.

PROGRAM RESET OPERATION

A program reset occurs when the processor performs a write operation to the ACIA with RS0 low and RS1 high. The program reset operates somewhat different from the hardware reset ($\overline{RES}$ pin) and is described as follows:

1. Internal registers are not completely cleared. Check register formats for the effect of a program reset on internal registers.

2. The $\overline{DTR}$ line goes high immediately.

3. Receiver and transmitter interrupts are disabled immediately. If $\overline{IRQ}$ is low when the reset occurs, it stays low until serviced, unless interrupt was caused by $\overline{DCD}$ or $\overline{DSR}$ transition.

4. $\overline{DCD}$ and $\overline{DSR}$ interrupts are disabled immediately. If $\overline{IRQ}$ is low and was caused by $\overline{DCD}$ or $\overline{DSR}$, then it goes high, also $\overline{DCD}$ and $\overline{DSR}$ status bits subsequently will follow the input lines, although no interrupt will occur.

5. Overrun cleared, if set.

MISCELLANEOUS

1. If Echo Mode is selected, $\overline{RTS}$ goes low.

2. If Bit 0 of Command Register ($\overline{DTR}$) is 0 (disabled), then:

   a) All interrupts are disabled, including those caused by $\overline{DCD}$ and $\overline{DSR}$ transitions.
   b) Transmitter is disabled immediately.
   c) Receiver is disabled, but a character currently being received will be completed first.

3. Odd parity occurs when the sum of all the 1 bits in the data word (including the parity bit) is odd.

4. In the receive mode, the received parity bit does not go into the Receiver Data Register, but generates parity error or no parity error for the Status Register.

5. Transmitter and Receiver may be in full operation simultaneously. This is "full-duplex" mode.

6. If the RxD line inadvertently goes low and then high right after a Stop Bit, the ACIA does not interpret this as a Start Bit, but samples the line again halfway into the bit to determine if it is a true Start Bit or a false one. For false Start Bit detection, the ACIA does not begin to receive data, instead, only a true Start Bit initiates receiver operation.

7. Precautions to consider with the crystal oscillator circuit:

   a) The external crystal should be a "series" mode crystal.
   b) The XTALI input may be used as an external clock input. The unused pin (EXTALO) must be floating and may not be used for any other function.

8. $\overline{DCD}$ and $\overline{DSR}$ transitions, although causing immediate processor interrupts, have no affect on transmitter operation. Data will continue to be sent, unless the processor forces transmitter to turn off. Since these are high-impedance inputs, they must not be permitted to float (un-connected). If unused, they must be terminated either to GND or V_{CC}.

GENERATION OF NON-STANDARD BAUD RATES

Divisors

The internal counter/divider circuit selects the appropriate divisor for the crystal frequency by means of bits 0-3 of the ACIA Control Register, as shown in Table 2.

Generating Other Baud Rates

By using a different crystal, other baud rates may be generated. These can be determined by:

$$\text{Baud Rate} = \frac{\text{Crystal Frequency}}{\text{Divisor}}$$

Furthermore, it is possible to drive the ACIA with an off-chip oscillator to achieve other baud rates. In this case, XTALI (pin 6) must be the clock input and XTALO (pin 7) must be a no-connect.

Table 2. Divisor Selection

Control Register Bits				Divisor Selected For The Internal Counter	Baud Rate Generated With 1.8432 MHz Crtstal	Baud Rate Generated With a Crystal of Frequency (F)
3	2	1	0			
0	0	0	0	No Divisor Selected	16 × External Clock at Pin RxC	16 × External Clock at Pin RxC
0	0	0	1	36,864	$\frac{1.8432 \times 10^6}{36,864} = 50$	$\frac{F}{36,864}$
0	0	1	0	24,576	$\frac{1.8432 \times 10^6}{24,576} = 75$	$\frac{F}{24,576}$
0	0	1	1	16,769	$\frac{1.8432 \times 10^6}{16,769} = 109.92$	$\frac{F}{16,769}$
0	1	0	0	13,704	$\frac{1.8432 \times 10^6}{13,704} = 134.51$	$\frac{F}{13,704}$
0	1	0	1	12,288	$\frac{1.8432 \times 10^6}{12,288} = 150$	$\frac{F}{12,288}$
0	1	1	0	6,144	$\frac{1.8432 \times 10^6}{6,144} = 300$	$\frac{F}{6,144}$
0	1	1	1	3,072	$\frac{1.8432 \times 10^6}{3,072} = 600$	$\frac{F}{3,072}$
1	0	0	0	1,536	$\frac{1.8432 \times 10^6}{1,536} = 1,200$	$\frac{F}{1,536}$
1	0	0	1	1,024	$\frac{1.8432 \times 10^6}{1,024} = 1,800$	$\frac{F}{1,024}$
1	0	1	0	768	$\frac{1.8432 \times 10^6}{768} = 2,400$	$\frac{F}{768}$
1	0	1	1	512	$\frac{1.8432 \times 10^6}{512} = 3,600$	$\frac{F}{512}$
1	1	0	0	384	$\frac{1.8432 \times 10^6}{384} = 4,800$	$\frac{F}{384}$
1	1	0	1	256	$\frac{1.8432 \times 10^6}{256} = 7,200$	$\frac{F}{256}$
1	1	1	0	192	$\frac{1.8432 \times 10^6}{192} = 9,600$	$\frac{F}{192}$
1	1	1	1	96	$\frac{1.8432 \times 10^6}{96} = 19,200$	$\frac{F}{96}$

DIAGNOSTIC LOOP-BACK OPERATING MODES

A simplified block diagram for a system incorporating an ACIA is shown in Figure 18.

It may be desirable to include in the system a facility for "loop-back" testing, of which there are two kinds:

1. Local Loop-Back

   Loop-back from the point of view of the processor. In this case, the Modem and Data Link must be effectively disconnected and the ACIA transmitter connected back to its own receiver, so that the processor can perform diagnostic checks on the system, excluding the actual data channel.

2. Remote Loop-Back

   Loop-back from the point of view of the Data Link and Modem. In this case, the processor, itself, is disconnected and all received data is immediately retransmitted, so the system on the other end of the Data Link may operate independent of the local system.

The ACIA does not contain automatic loop-back operating modes, but they may be implemented with the addition of a small amount of external circuitry. Figure 19 indicates the necessary logic to be used with the ACIA. The LLB line is the positive-true signal to enable local loop-back operation. Essentially, LLB = high does the following:

1. Disables outputs TxD, $\overline{DTR}$, and $\overline{RTS}$ (to Modem).
2. Disables inputs RxD, $\overline{DCD}$, $\overline{CTS}$, $\overline{DSR}$ (from Modem).
3. Connects transmitter outputs to respective receiver inputs (i.e., TxD to RxD, $\overline{DTR}$ to $\overline{DCD}$, $\overline{RTS}$ to $\overline{CTS}$).

LLB may be tied to a peripheral control pin (from an R65C21 or R65C24, for example) to provide processor control of local loop-back operation. In this way, the processor can easily perform local loop-back diagnostic testing.

Remote loop-back does not require this circuitry, so LLB must be set low. However, the processor must select the following:

1. Control Register bit 4 must be 1, so that the transmitter clock equals the receiver clock.
2. Command Register bit 4 must be 1 to select Echo Mode.
3. Command Register bits 3 and 2 must be 1 and 0, respectively to disable $\overline{IRQ}$ interrupt to transmitter.
4. Command Register bit 1 must be 0 to disable $\overline{IRQ}$ interrupt for receiver.

In this way, the system re-transmits received data without any effect on the local system.

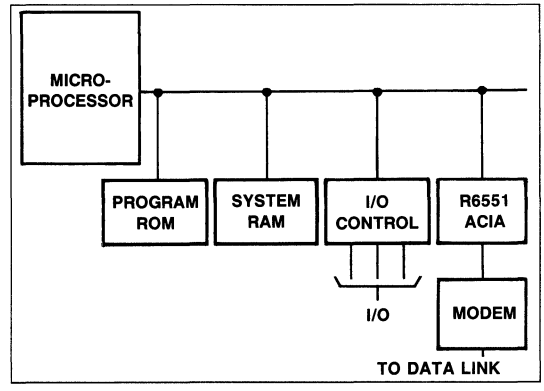


Figure 18. Simplified System Diagram

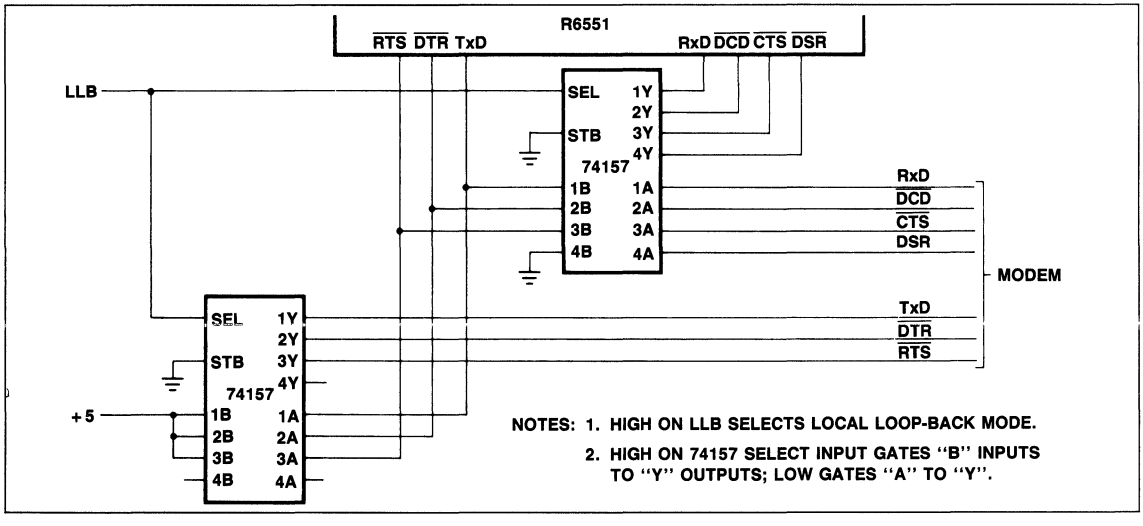


Figure 19. Loop-Back Circuit Schematic

READ TIMING DIAGRAM

Timing diagrams for transmit with external clock, receive with external clock, and $\overline{IRQ}$ generation are shown in Figures 20, 21 and 22, respectively. The corresponding timing characteristics are listed in Table 3.

Table 3. Transmit/Receive Characteristics

Characteristic	Symbol	1 MHz		2 MHz		Unit
		Min	Max	Min	Max	
Transmit/Receive Clock Rate	t_{CCY}	400*	—	400*	—	ns
Transmit/Receive Clock High Time	t_{CH}	175	—	175	—	ns
Transmit/Receive Clock Low Time	t_{CL}	175	—	175	—	ns
XTLI to TxD Propagation Delay	t_{DD}	—	500	—	500	ns
RTS Propagation Delay	t_{DLY}	—	500	—	500	ns
$\overline{IRQ}$ Propagation Delay (Clear)	t_{IRQ}	—	500	—	500	ns

Notes:
(t_R, t_F = 10 to 30 ns)

*The baud rate with external clocking is: Baud Rate = $\frac{1}{16 \times t_{CCY}}$

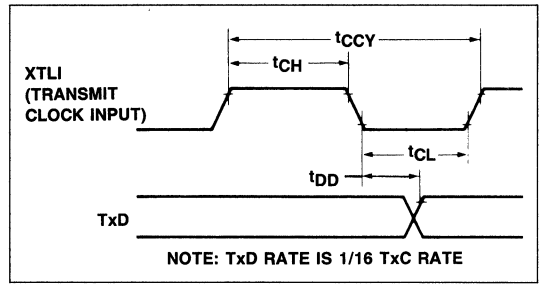


Figure 20. Transmit Timing with External Clock

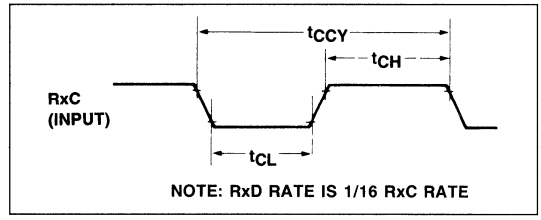


Figure 21. Receive External Clock Timing

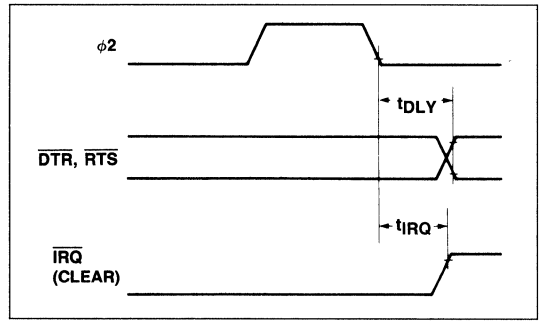


Figure 22. Interrupt and Output Timing

AC CHARACTERISTICS

Parameter	Symbol	1 MHz		2 MHz		Unit
		Min	Max	Min	Max	
ϕ2 Cycle Time	t_{CYC}	1000	—	500	—	ns
ϕ2 Pulse Width	t_C	400	—	200	—	ns
Address Set-Up Time	t_{ACW}	120	—	60	—	ns
Address Hold Time	t_{CAH}	0	—	0	—	ns
R/$\overline{W}$ Set-Up Time	t_{WCW}	120	—	60	—	ns
R/$\overline{W}$ Hold Time	t_{CWH}	0	—	0	—	ns
Data Bus Set-Up Time	t_{DCW}	120	—	60	—	ns
Data Bus Hold Time	t_{HW}	20	—	10	—	ns
Read Access Time (Valid Data)	t_{CDR}	—	200	—	100	ns
Read Hold Time	t_{HR}	20	—	10	—	ns
Bus Active Time (Invalid Data)	t_{CDA}	40	—	20	—	ns

Notes:
1. V_{CC} = 5 0V ±5%
2. T_A = T_L to T_H
3 t_R and t_F = 10 to 30 ns

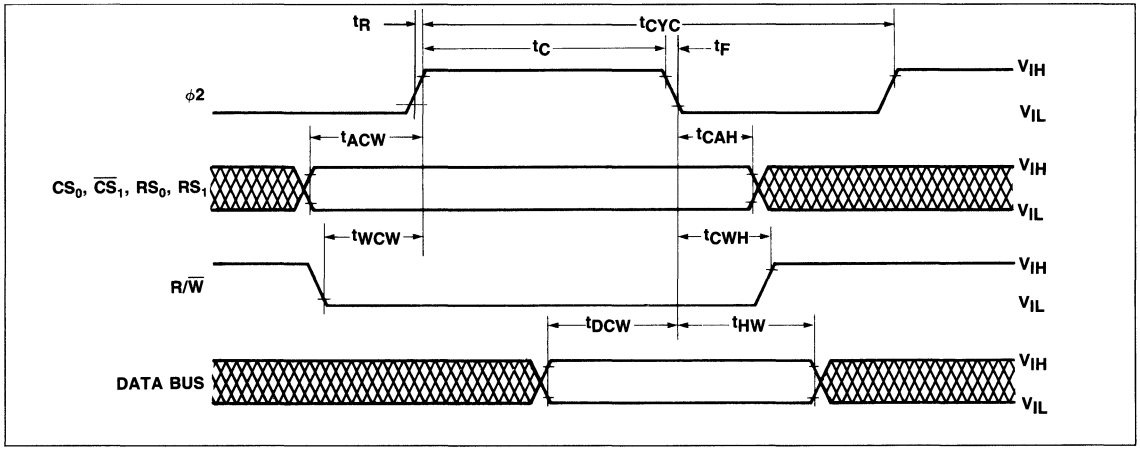


Figure 23. Write Timing Diagram

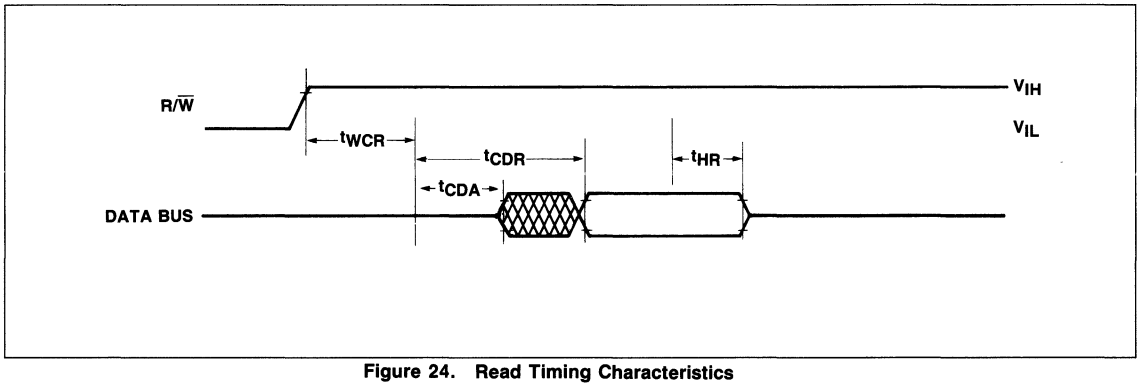


Figure 24. Read Timing Characteristics

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to +7.0	Vdc
Input Voltage	V_{IN}	−0.3 to V_{CC} +0.3	Vdc
Output Voltage	V_{OUT}	−0.3 to V_{CC} +0.3	Vdc
Operating Temperature Commercial Industrial	T_A	 0 to +70 −40 to +85	°C
Storage Temperature	T_{STG}	−55 to +150	°C

*NOTE: Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in other sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING CONDITIONS

Parameter	Symbol	Value
Supply Voltage	V_{CC}	5V ±5%
Temperature Range Commercial Industrial	T_A	 0° to 70°C −40°C to +85°C

DC CHARACTERISTICS

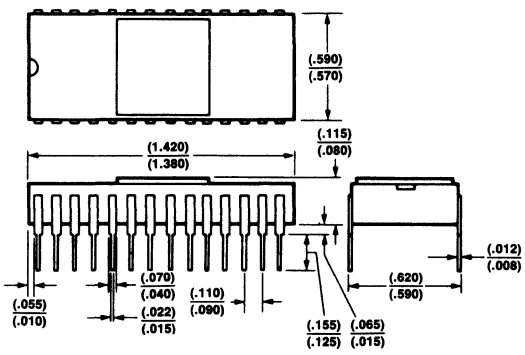
(V_{CC} = 5.0V ±5%, V_{SS} = 0, T_A = T_L to T_H, unless otherwise noted)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input High Voltage	V_{IH}	2.0	—	V_{CC}	V	
Input Low Voltage	V_{IL}	−0.3	—	+0.8	V	
Input Leakage Current: Ø2, R/$\overline{W}$, $\overline{RES}$, CS0, $\overline{CS1}$, RS0, RS1, $\overline{CTS}$, RxD, $\overline{DCD}$, DSR	I_{IN}	—	±1	±2.5	μA	V_{IN} = 0V to V_{CC} V_{CC} = 5.25V
Input Leakage Current (Three State Off) D0–D7	I_{TSI}	—	±2	±10	μA	V_{IN} = 0.4V to 2.4V V_{CC} = 5.25V
Output High Voltage: D0–D7, TxD, RxC, $\overline{RTS}$, $\overline{DTR}$	V_{OH}	2.4	—	—	V	V_{CC} = 4.75V I_{LOAD} = −100 μA
Output Low Voltage: D0–D7, TxD, RxC, $\overline{RTS}$, $\overline{DTR}$, $\overline{IRQ}$	V_{OL}	—	—	0.4	V	V_{CC} = 4.75V I_{LOAD} = 1.6 mA
Output High Current (Sourcing): D0–D7, TxD, RxC, $\overline{RTS}$, $\overline{DTR}$	I_{OH}	−200	−400	—	μA	V_{OH} = 2.4V
Output Low Current (Sinking): D0–D7, TxD, RxC, $\overline{RTS}$, $\overline{DTR}$, $\overline{IRQ}$	I_{OL}	1.6	—	—	mA	V_{OL} = 0.4V
Output Leakage Current (off state): $\overline{IRQ}$	I_{OFF}	—		10	μA	V_{OUT} = 5.0V
Power Dissipation	P_D	—	7	10	mW/MHz	
Input Capacitance All except Ø2 Ø2	 C_{CLK} C_{IN}	 — —		 20 10	 pF pF	V_{CC} = 5.0V V_{IN} = 0V f = 2 MHz T_A = 25°C
Output Capacitance	C_{OUT}	—		10	pF	

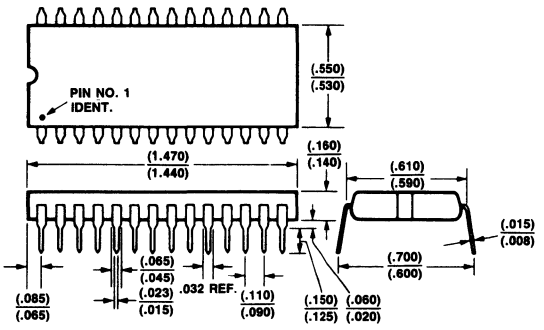
Notes:
1. All units are direct current (dc) except for capacitance.
2. Negative sign indicates outward current flow, positive indicates inward flow.
3. Typical values are shown for V_{CC} = 5.0V and TA = 25°C.

PACKAGE DIMENSIONS

28-PIN CERAMIC DIP



28-PIN PLASTIC DIP



R65C52
DUAL ASYNCHRONOUS COMMUNICATIONS INTERFACE ADAPTER (DACIA)

PRELIMINARY

DESCRIPTION

The Rockwell CMOS R65C52 Dual Asynchronous Communications Interface Adapter (DACIA) provides an easily implemented, program controlled interface between 8-bit microprocessor-based systems and serial communication data sets and modems.

The DACIA has an internal baud rate generator. This feature eliminates the need for multiple component support circuits, a crystal being the only other part required. The Transmitter baud rate can be selected under program control to be either 1 of 15 different rates from 50 to 38,400 baud, or at 1/16 times an external clock rate. The Receiver baud rate may be selected under program control to be either the Transmitter rate, or at 1/16 times the external clock rate. The DACIA is programmable for word lengths of 5, 6, 7 or 8 bits; even, odd, or no parity; and 1 or 2 stop bits.

The DACIA is designed for maximum programmed control from the microprocessor (MPU) to simplify hardware implementation. Dual sets of registers allow independent control and monitoring of each channel. The DACIA also provides a unique, programmable Automatic Address Recognition Mode for use in a multi-drop environment.

The Control Register and Status Register permit the MPU to easily select the R65C52's operating modes and determine operational status.

The Interrupt Enable Registers (IER) and Interrupt Status Registers (ISR) allow the MPU to control and monitor the interrupt capabilities of the DACIA.

The Control and Format Register (CFR) permits selection of baud rates, word lengths, parity and stop bits as well as control of DTR and RTS output signals.

The Status Register (SR) gives the MPU access to the state of the modem control lines, framing error, transmitter underrun and break conditions.

The Compare Data Registers (CDR) hold the data value to be used in the compare mode and the Transmit Break Register (TBR) commands a Transmit Break and provides for parity/address recognition, for Automatic Address Mode.

The Transmitter Data Register and Receiver Data Register are used for temporary data storage of input and output data.

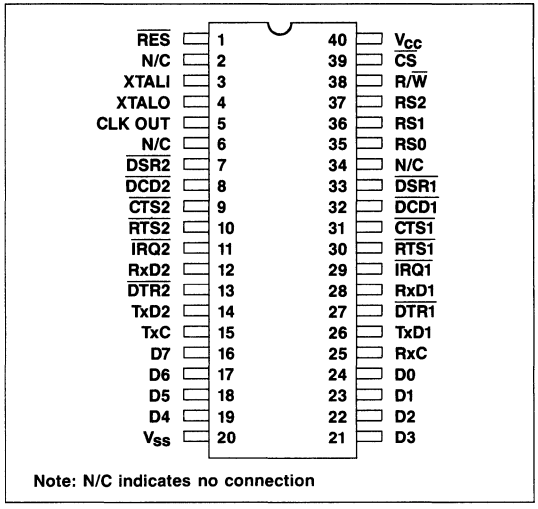
FEATURES

- Low power CMOS N-well silicon gate technology
- Two independent full duplex channels with buffered receivers and transmitters.
- Data set/modem control functions
- Internal baud rate generator with 15 programmable baud rates (50 to 38,400)
- Program-selectable internally or externally controlled receiver rate
- Programmable word lengths, number of stop bits, and parity bit generation and detection
- Programmable interrupt control
- Programmable control of edge detect for DCD, DSR, DTR, RTS, and CTS
- Program-selectable serial echo mode for each channel
- Automatic Address Recognition Mode for multi-drop operation.
- Up to 4 MHz host bus operation
- 5.0 Vdc ±5% supply requirements
- 40-pin plastic or ceramic DIP
- Full TTL or CMOS input/output compatibility
- Compatible with R6500 and R65C00 microprocessors and R6500/* microcomputers.

ORDERING INFORMATION

Part Number:
R65C52

- Temperature Range (T_L to T_H)
  - Blank = 0°C to +70°C
  - E = −40°C to +85°C
- Frequency Range
  - 2 = 2 MHz
  - 4 = 4 MHz
- Package
  - C = Ceramic
  - P = Plastic



Note: N/C indicates no connection

Figure 1. R65C52 Pin Configuration

INTERFACE SIGNALS

Figure 2 shows the DACIA interface signals associated with the microprocessor and the modem.

DATA BUS (D0–D7)

The D0–D7 pins are eight data lines that transfer data between the microprocessor (MPU) and the DACIA. These lines are bidirectional and are normally high-impedance except during READ cycle when the DACIA is selected.

REGISTER SELECTS (RS0, RS1, RS2)

The three register select lines are normally connected to the processor address lines to allow the MPU to select the various internal registers. Table 1 shows the internal register select coding and identifies the abbreviations (ABBR) used throughout the text for each register.

READ/WRITE (R/$\overline{W}$)

The R/$\overline{W}$ input, generated by the microprocessor, controls the direction of data transfer. A high on the R/$\overline{W}$ line indicates a read cycle, while a low indicates a write cycle.

CHIP SELECT ($\overline{CS}$)

The chip select input is normally connected to the processor address lines either directly or through decoders. The DACIA latches address and R/$\overline{W}$ inputs on the falling edge of $\overline{CS}$ and latches the data bus inputs on the rising edge of $\overline{CS}$.

RESET ($\overline{RES}$)

During system initialization a low level on the $\overline{RES}$ input causes a RESET to occur. At this time the IER's are set to $80, the $\overline{DTR}$ and $\overline{RTS}$ lines go to the high state, the RDR register is cleared, the TBR is set to $0F, the compare mode is disabled, and the $\overline{CTS}$, $\overline{DCD}$, $\overline{DSR}$ flags are cleared. No other bits are affected.

TRANSMIT DATA (TXD1, TXD2)

The TxD outputs transfer serial non-return to zero (NRZ) data to the data communications equipment (DCE). The data is transferred, LSB first, at a rate determined by the baud rate generator.

RECEIVE DATA (RXD1, RXD2)

The RxD inputs transfer serial NRZ data into the DACIA from the DCE, LSB first. The receiver baud rate is determined by the baud rate generator.

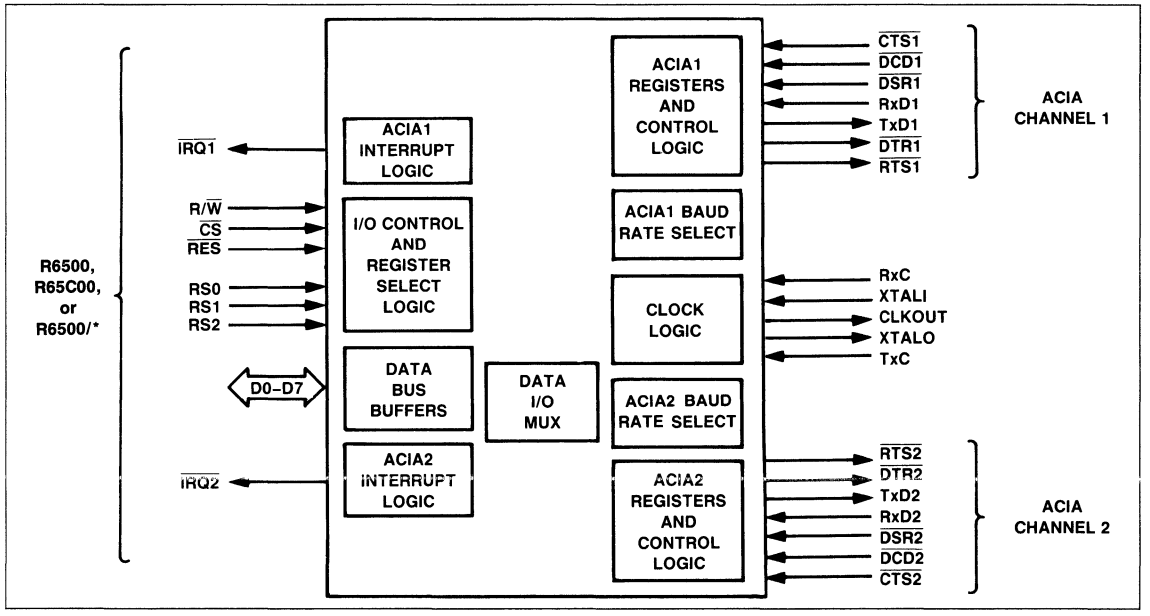


Figure 2. DACIA Interface Signals

CLEAR TO SEND ($\overline{CTS1}$, $\overline{CTS2}$)

The $\overline{CTS}$ control line inputs allow handshaking by the transmitter. When $\overline{CTS}$ is low, the data is transmitted continuously. When $\overline{CTS}$ is high, the Transmit Data Register empty bit in the ISR is not set. The word presently in the Transmit Shift Register is sent normally. Any active transition on the $\overline{CTS}$ lines sets the $\overline{CTS}$ bit in the appropriate ISR. The $\overline{CTS}$ status bit in the CSR reflects the current high or low state of $\overline{CTS}$.

DATA CARRIER DETECT ($\overline{DCD1}$, $\overline{DCD2}$)

These two lines may be used as general purpose inputs. An active transition sets the $\overline{DCD}$ bit in the ISR. The $\overline{DCD}$ bit in the CSR reflects the current state of the $\overline{DCD}$ line.

DATA SET READY ($\overline{DSR1}$, $\overline{DSR2}$)

These two lines may be used as general purpose inputs. An active transition sets the $\overline{DSR}$ bit in the ISR. The $\overline{DSR}$ bit in the CSR reflects the current state of the $\overline{DSR}$ line.

REQUEST TO SEND ($\overline{RTS1}$, $\overline{RTS2}$)

These two lines may be used as general purpose outputs. They are set high upon reset. Their state may be programmed by setting the appropriate bits in the CFR high or low. The state of the $\overline{RTS}$ line is reflected by the $\overline{RTS}$ bit in the CSR.

DATA TERMINAL READY ($\overline{DTR1}$, $\overline{DTR2}$)

These two lines may be used as general purpose outputs. They are set high upon reset. Their state may be programmed by setting the appropriate bits in the CFR high or low. The state of the $\overline{DTR}$ line is reflected by the $\overline{DTR}$ bit in the CSR.

INTERRUPT REQUEST ($\overline{IRQ1}$, $\overline{IRQ2}$)

The $\overline{IRQ}$ lines are open-drain outputs from the interrupt control logic. $\overline{IRQ1}$ is associated with ACIA1 and $\overline{IRQ2}$ is associated with ACIA2. These lines are normally high but go low when one of the flags in the ISR is set, provided that its corresponding enable bit is set in the IER.

Table 1. DACIA Register Selection

HEX ADDR	REGISTER SELECT LINES			CONTROL AND FORMAT REGISTER BITS		REG ABBR	REGISTER ACCESS	
	RS2	RS1	RS0	CFR-7	CFR-6		WRITE	READ
00	L	L	L	—	—	IER1 ISR1	INTERRUPT ENABLE REGISTER 1	INTERRUPT STATUS REGISTER 1
01	L	L	H	0	—	CFR1 SR1	CONTROL REGISTER 1	STATUS REGISTER 1
				1	—	CFR1	FORMAT REGISTER 1	INVALID
02	L	H	L	—	0	CDR1	COMPARE DATA REGISTER 1	INVALID
				—	1	TBR1	TRANSMIT BREAK REGISTER 1	INVALID
03	L	H	H	—	—	TDR1 RDR1	TRANSMIT DATA REGISTER 1	RECEIVE DATA REGISTER 1
04	H	L	L	—	—	IER2 ISR2	INTERRUPT ENABLE REGISTER 2	INTERRUPT STATUS REGISTER 2
05	H	L	H	0	—	CFR2 SR2	CONTROL REGISTER 2	STATUS REGISTER 2
				1	—	CFR2	FORMAT REGISTER 2	INVALID
06	H	H	L	—	0	CDR2	COMPARE DATA REGISTER 2	INVALID
				—	1	TBR2	TRANSMIT BREAK REGISTER 2	INVALID
07	H	H	H	—	—	TDR2 RDR2	TRANSMIT DATA REGISTER 2	RECEIVE DATA REGISTER 2

FUNCTIONAL DESCRIPTION

Figure 3 is a block diagram of the DACIA which consists of two asynchronous communications interface adapters with common microprocessor interface control logic and data bus buffers. The individual functional elements of the DACIA are described in the following paragraphs.

INTERRUPT LOGIC

The interrupt logic causes the $\overline{IRQ}$ lines ($\overline{IRQ1}$ or $\overline{IRQ2}$) to go low when conditions are met that require the attention of the MPU. There are two registers (the Interrupt Enable Register and the Interrupt Status Register) involved in the control of interrupts in the DACIA. Corresponding bits in both registers must be set to cause an $\overline{IRQ}$.

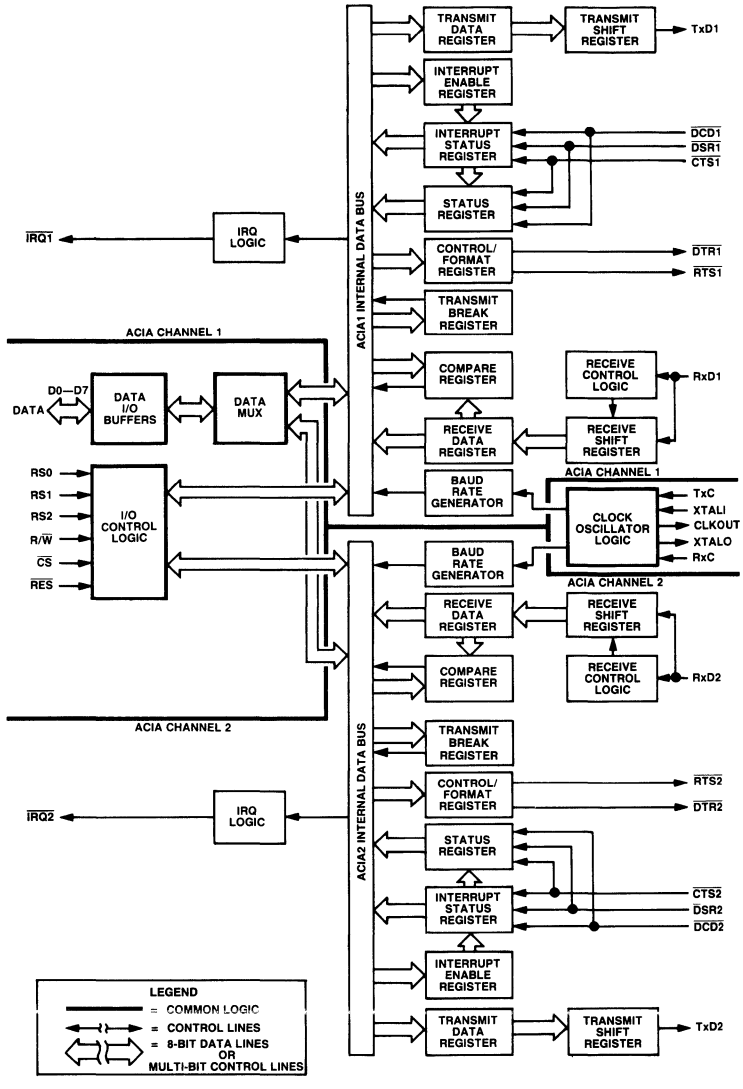


Figure 3. DACIA Block Diagram

DATA BUS BUFFER

The Data Bus Buffer is a bidirectional interface between the system data lines and the internal data bus. When R/$\overline{W}$ is low and $\overline{CS}$ is low, the Data Bus Buffer writes data from the internal data bus to the system data lines. When R/$\overline{W}$ is high and $\overline{CS}$ is low, data is driven into the DACIA from the system data bus. Table 2 summarizes the Data Bus Buffer states.

Table 2. Data Bus Buffer Summary

Control Signals R/$\overline{W}$	Control Signals $\overline{CS}$	Data Bus Buffer State
L	L	Write Mode — Tri-State
H	L	Read Mode — Output Data

TRANSMIT AND RECEIVE DATA REGISTERS

These registers are used as temporary data storage for the DACIA Transmit and Receive circuits. The Transmit Data Register is characterized as follows:

- Bit 0 is the leading bit to be transmitted.
- Unused data bits are the high-order bits and are "don't care" for transmission.
- Write-only register.

The Receive Data Register is characterized in a similar fashion as follows:

- Bit 0 is the leading bit received.
- Unused data bits are the high order bits and are "0" for the receiver.
- Parity bits are not contained in the Receive Data Register, but are stripped off after being used for external parity checking. Parity and all unused high-order bits are "0".
- Read-only register

Figure 4 shows an example of a Parity Mode single transmitted or received data word. In this example, the data word is formatted with 8 data bits, parity, and two stop bits. Figure 4 also shows a single character transmitted or received in Address/Data Mode. In this example, the address or data word is 8 bits, there is no parity bit, and there are two stop bits. The 10th bit (normal parity bit) is an address/data indicator. A 1 means the 8 bits are an address and a 0 means the 8 bits are data.

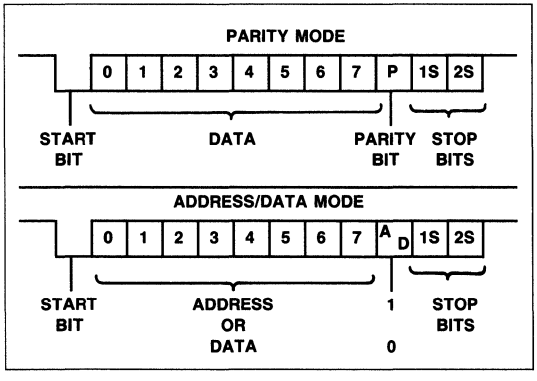


Figure 4. Typical Character

CLOCK CIRCUIT

The internal clock oscillator supplies the time base for the baud rate generator. The oscillator can be driven by a crystal or an external clock, or it can be disabled, in which case the time base for the baud rate is generated by the Receiver External Clock (RxC) and Transmitter External Clock (TxC) input pins. Figure 5 shows the three possible clock configurations.

Crystal (XTALI, XTALO)

These pins are normally connected to an external 3.6864 MHz crystal used as the time base for the baud rate generator. As an alternative, the XTLI pin may be driven with an externally generated clock in which case the XTALO pin must float.

Receiver Clock (RxC)

This pin is the Receiver 16x clock input when the baud rate generator is programmed for external clock. Figure 15 shows timing considerations for RxC.

Transmitter Clock (TxC)

This pin is the transmitter 16x clock input when the baud rate generator is programmed for external clock. Figure 16 shows timing considerations for TxC.

Note

When RxC and TxC are used for external clock input, XTALI must be tied to ground (Vss) and XTALO must be left open (floating).

Clock Out (CLK OUT)

This output is a buffered output from the 3.6864 MHz crystal oscillator. It may be used to drive the XTALI input of another DACIA. This allows multiple DACIA chips to be used in a system with only one crystal needed. CLK OUT is in phase with XTALI.

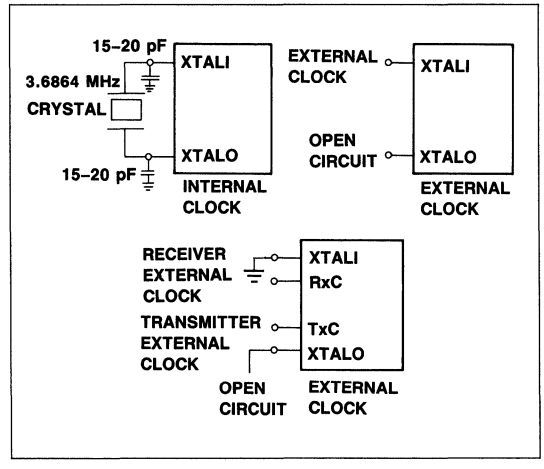


Figure 5. DACIA Clock Generation

CONTROL AND FORMAT REGISTER (CFR)

The Control and Format Register (CFR) is a dual-function, write-only register which allows control of word length, baud rate, control line outputs, parity, echo mode, and compare/TBR access. When the CFR is written to with bit 7 = 0, the CFR functions as a Control Register. When the CFR is written to with bit 7 = 1, the CFR operates as a Formal Register.

Control Register (CFR Addressed with Bit 7 = 0)

7	6	5	4	3 2 1 0
0	TBR/CDR	NO. STOP BITS	ECHO	BAUD RATE SELECTION

Bit 7 — **Control or Format Register**
0 — Control Register

Bit 6 — **TBR/CDR**
1 — Access the Transmit Break Register (TBR)
0 — Access the Compare Data Register (CDR)

Bit 5 — **Number of Stop Bits Per Character**
1 — Two stop bits
0 — One stop bit

Bit 4 — **Echo Selection (ECHO)**
1 — Echo activated
0 — Echo deactivated

Bits 3-0 — **Baud Rate Selection**

3	2	1	0	Baud Rate
0	0	0	0	50
0	0	0	1	109.2
0	0	1	0	134.58
0	0	1	1	150
0	1	0	0	300
0	1	0	1	600
0	1	1	0	1200
0	1	1	1	1800
1	0	0	0	2400
1	0	0	1	3600
1	0	1	0	4800
1	0	1	1	7200
1	1	0	0	9600
1	1	0	1	19200
1	1	1	0	38400
1	1	1	1	External TxC and RxC Clocks

Format Register (CFR Addressed with Bit 7 = 1)

7	6 5	4 3	2	1	0
1	NUMBER OF DATA BITS	PARITY SELECTION	PARITY ENABLE	$\overline{\text{DTR}}$ CONTROL	$\overline{\text{RTS}}$ CONTROL

Bit 7 — **Control or Format Register**
1 — Format Register

Bits 6-5 — **Number of Data Bits Per Character**

6	5	No. Bits
0	0	5
0	1	6
1	0	7
1	1	8

Bits 4-3 — **Parity Mode Selection**

4	3	Selects
0	0	Odd Parity
0	1	Even Parity
1	0	Mark Parity
1	1	Space Parity

Bit 2 — **Parity Enable**
1 — Parity as specified by bits 4-3
0 — No Parity

Bit 1 — **$\overline{\text{DTR}}$ Control**
1 — $\overline{\text{DTR}}$ high
0 — $\overline{\text{DTR}}$ low

Bit 0 — **$\overline{\text{RTS}}$ Control**
1 — $\overline{\text{RTS}}$ high
0 — $\overline{\text{RTS}}$ low

INTERRUPT ENABLE REGISTER (IER)

The Interrupt Enable Register (IER) is a write-only register that allows each of the possible IRQ sources to be enabled, or disabled, individually without affecting any of the other interrupt enable bits in the register. IRQ sources are enabled by writing to the IER with bit 7 set to a 1 and every bit set to a 1 that corresponds to the IRQ source to be enabled. IRQ sources are disabled by writing to the IER with bit 7 set to a 0 and every bit set to a 1 that corresponds to the IRQ source to be disabled. Any bit (except bit 7) to which a 0 is written is unaffected and remains in its original state. As an example, writing $7F to the IER will disable all IRQ source bits, but writing $FF to the IER will enable all IRQ source bits. A hardware reset ($\overline{\text{RES}}$) clears all IRQ source bits to the 0 state. Bit assignments for the IER are as follows:

7	6	5	4	3	2	1	0
CLEAR/ SET BITS	TDR EMPTY IE	$\overline{\text{CTS}}$ IE	$\overline{\text{DCD}}$ IE	$\overline{\text{DSR}}$ IE	PARITY ERROR IE	FRM OVR BRK CPR IE	RDR FULL IE

INTERRUPT STATUS REGISTER (ISR)

The Interrupt Status Register (ISR) is a read-only register that identifies the current status condition for each DACIA internal IRQ source. Bits 6 through 0 of the ISR are set to a 1 whenever the corresponding IRQ source condition has occurred in the DACIA. Bit 7 identifies if any of the IRQ source status bits have been set in the ISR.

7	6	5	4	3	2	1	0
ANY BIT SET	TDR EMPTY	$\overline{\text{CTS}}$ TRANS	$\overline{\text{DCD}}$ TRANS	$\overline{\text{DSR}}$ TRANS	PARITY ERROR	FRM OVR BRK CPR	RDR FULL

Bit 7 **Any Bit Set**
1 Any bit (6 through 0) has been set to a 1
0 No bits have been set to a 1

Bit 6 **Transmit Data Register Empty (TDR EMPTY)**
1 Transmit Data Register has been transferred to the shift register
0 New data has been written to the Transmit Data Register

Bit 5 **Transition On $\overline{\text{CTS}}$ Line ($\overline{\text{CTS}}$ TRANS)**
1 A positive or negative transition has occurred on $\overline{\text{CTS}}$
0 No transition has occurred on $\overline{\text{CTS}}$, or ISR has been Read

Bit 4 **Transition On $\overline{\text{DCD}}$ Line ($\overline{\text{DCD}}$ TRANS)**
1 A positive or negative transition has occurred on $\overline{\text{DCD}}$
0 No transition has occurred on $\overline{\text{DCD}}$, or ISR has been Read

Bit 3 **Transition On $\overline{\text{DSR}}$ Line ($\overline{\text{DSR}}$ TRANS)**
1 A positive or negative transition has occurred on $\overline{\text{DSR}}$
0 No transition has occurred on $\overline{\text{DSR}}$, or ISR has been Read

Bit 2 **Parity Error**
1 A parity error has occurred in received data
0 No parity error has occurred, or the Receive Data Register (RDR) has been Read

Bit 1 **Frame Error, Overrun or Break (FRM, OVR, BRK, CPR)**
1 A framing error, receive overrun, or receive break has occured, or, in Compare Mode
0 No error, overrun, break has occured, RDR has been Read, or not in Compare Mode

Bit 0 **Receive Data Register Full (RDR FULL)**
1 Shift register data has been transferred to Receive Data Register
0 Receive Data Register has been Read

CONTROL STATUS REGISTER (CSR)

The Control Status Register (CSR) is a read-only register that provides I/O status and error condition information. The CSR is normally read after an IRQ has occurred to determine the exact cause of the interrupt condition.

7	6	5	4	3	2	1	0
FRAMING ERROR	TRANS UNDR	$\overline{\text{CTS}}$ STATUS	$\overline{\text{DCD}}$ STATUS	$\overline{\text{DSR}}$ STATUS	REC BREAK	$\overline{\text{DTR}}$ STATUS	$\overline{\text{RTS}}$ STATUS

Bit 7 **Framing Error**
1 A framing error occurred in receive data
0 No framing error occurred, or the RDR was Read

Bit 6 **Transmitter Underrun (TRANS UNDR)**
1 Transmit shift register is empty and TDRE bits in IER and ISR are set
0 A write to the TDR has occurred

Bit 5 **$\overline{\text{CTS}}$ Status**
1 A low-to-high transition occurred on $\overline{\text{CTS}}$ line
0 A high-to-low transition occurred on $\overline{\text{CTS}}$ line

Bit 4 **$\overline{\text{DCD}}$ Status**
1 A low-to-high transition occurred on $\overline{\text{DCD}}$ line
0 A high-to-low transition occurred on $\overline{\text{DCD}}$ line

Bit 3 **$\overline{\text{DSR}}$ Status**
1 A low-to-high transition occurred on $\overline{\text{DSR}}$ line
0 A high-to-low transition occurred on $\overline{\text{DSR}}$ line

Bit 2 **REC Break**
1 A Receive Break has occurred
0 No Receive Break occurred, or RDR, was read

Bit 1 **$\overline{\text{DTR}}$ Status**
1 A low-to-high transition occurred on $\overline{\text{DTR}}$ line
0 A high-to-low transition occurred on $\overline{\text{DTR}}$ line

Bit 0 **$\overline{\text{RTS}}$ Status**
1 A low-to-high transition occurred on $\overline{\text{RTS}}$ line
0 A high-to-low transition occurred on $\overline{\text{RTS}}$ line

TRANSMIT BREAK REGISTER (TBR)

The DACIA has two Transmit Break Registers which are write-only registers. Only two bits of these registers are used; one during the Receive mode to command a Transmit Break and the other to provide for Parity/Address recognition. Writing a 1 to bit 1 of the TBR causes a continuous Break to be transmitted by the ACIA associated with the register. Writing a 0 to this bit allows normal transmission to resume. Writing a 1 to bit 0 of the TBR commands the value of the Parity bit to be sent to the Parity Error bit (bit 2 of the ISR). Writing a 0 to this bit allows normal Parity Error recognition to be in force. When an $\overline{RES}$ is received by the DACIA, both of these bits are reset to 0. The bits format for the TBR are as follows:

7	6	5	4	3	2	1	0
NOT USED						TRANS BRK	PAR/ ADDR

Bits 7-2 **Not used (don't care)**

Bit 1 **Transmit Break (TRANS BRK)**
1 Transmit continuous Break until disabled
0 Resume normal transmission

Bit 0 **Parity/Address Recognition (PAR ADDR)**
1 Send value of parity to ISR bit 2
0 Return to normal Parity Error recognition mode

COMPARE DATA REGISTER

The Compare Data Register (CDR) is a write-only register which can be accessed when CFR bit 6 = 0. By writing a value into the CDR, the DACIA is put in the compare mode. In this mode, setting of the RDRF bit is inhibited and the FRM/OVR/BRK/CPR bit (bit 1) on the ISR is set until a character is received which matches the value in the CDR. The next character is then received and the RDRF bit is set. The receiver will now operate normally until the CDR is again loaded.

SUMMARY OF REGISTERS

Table 3 shows the control and status registers associated with the DACIA in a single summary table. Each of the ACIA's has its own set of these seven registers.

OPERATION

The following paragraphs describe ten modes (or conditions) of operation of the DACIA. The modes described are:

- Continuous Data Transmit
- Continuous Data Receive
- Transmit Underrun Condition
- Effects of CTS on Transmitter
- Effects of Overrun on Receiver
- Echo Mode Timing
- Framing Error
- Transmit Break Character
- Receive Break Character
- Automatic Address Recognition

Table 3. Control and Status Registers Format Summary

REGISTER BIT NUMBERS								REGISTER	$\overline{RES}$
7	6	5	4	3	2	1	0		
CLEAR/SET BITS	TDR EMPTY IE	$\overline{CTS}$ IE	$\overline{DCD}$ IE	$\overline{DSR}$ IE	PARITY ERROR IE	FRM, OVR BRK, CPR IE	RDR FULL IE	INTERRUPT ENABLE REGISTERS	$80
ANY BIT SET	TDR EMPTY	$\overline{CTS}$ TRANS	$\overline{DCD}$ TRANS	$\overline{DSR}$ TRANS	PARITY ERROR	FRM, OVR BRK, CPR	RDR FULL	INTERRUPT STATUS REGISTERS	—
FRAMING ERROR	TRANS UNDR	$\overline{CTS}$ STATUS	$\overline{DCD}$ STATUS	$\overline{DSR}$ STATUS	REC BREAK	$\overline{DTR}$ STATUS	$\overline{RTS}$ STATUS	STATUS REGISTERS	—
0	TBR/ CDR	NO. STOP BITS	ECHO	BAUD RATE SELECTION				CONTROL REGISTERS AND FORMAT REGISTERS	—
1	NUMBER OF DATA BITS		PARITY SELECTION		PARITY ENABLE	$\overline{DTR}$ CONTROL	$\overline{RTS}$ CONTROL		
NOT USED						TRANS BRK	PAR/ ADDR	TRANSMIT BREAK REGISTERS	$0F
COMPARE BITS (ADDRESS RECOGNITION)								COMPARE DATA REGISTERS	—

CONTINUOUS DATA TRANSMIT

In the normal operating mode, the TDRE bit in the ISR signals the MPU that the DACIA is ready to accept the next data word. An $\overline{IRQ}$ occurs if the corresponding TDRE IRQ enable bit is set in the IER. The TDRE bit is set at the beginning of the start bit. When the MPU writes a word to the TDR the TDRE bit is cleared. In order to maintain continuous transmission the TDR must be loaded before the stop bit(s) are ended. Figure 6 shows the relationship between $\overline{IRQ}$ and TxD for the Continuous Data Transmit mode.

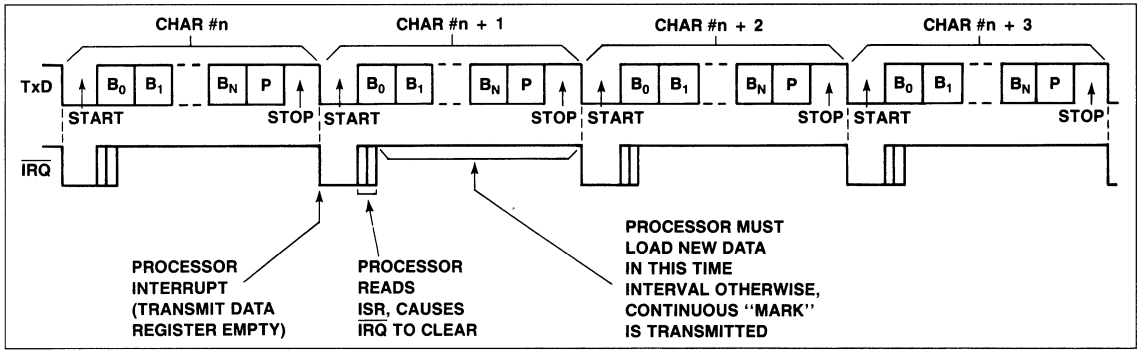


Figure 6. Continuous Data Transmit

CONTINUOUS DATA RECEIVE

Similar to the continuous data transmit mode, the normal receive mode sets the RDRF bit in the ISR when the DACIA has received a full data word. This occurs at about the 9/16 point through the stop bit. The processor must read the RDR before the next stop bit, or an overrun error occurs. Figure 7 shows the relationship between $\overline{IRQ}$ and RxD for the continuous Data Receive mode.

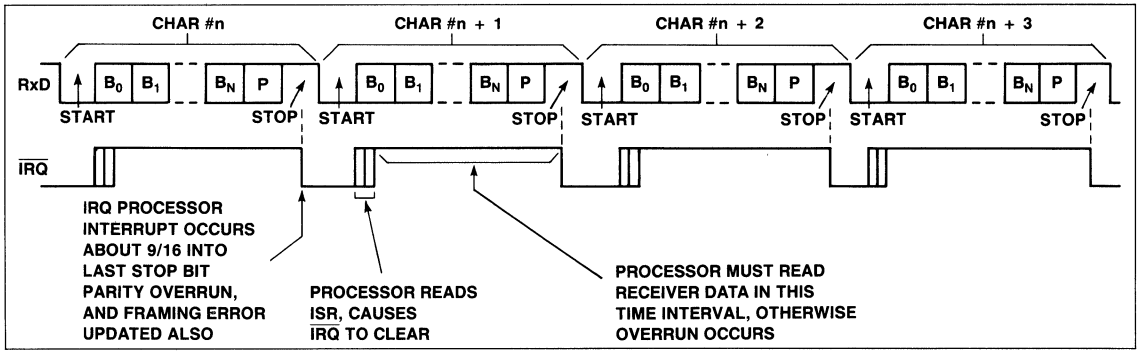


Figure 7. Continuous Data Receive

TRANSMIT UNDERRUN CONDITION

If the MPU is unable to load the TDR before the last stop bit is sent, the TxD line goes to the MARK condition and the underrun flag is set. This condition persists until the TDR is loaded with a new word. Figure 8 shows the relation between $\overline{IRQ}$ and TxD for the Transmit Underrun Condition.

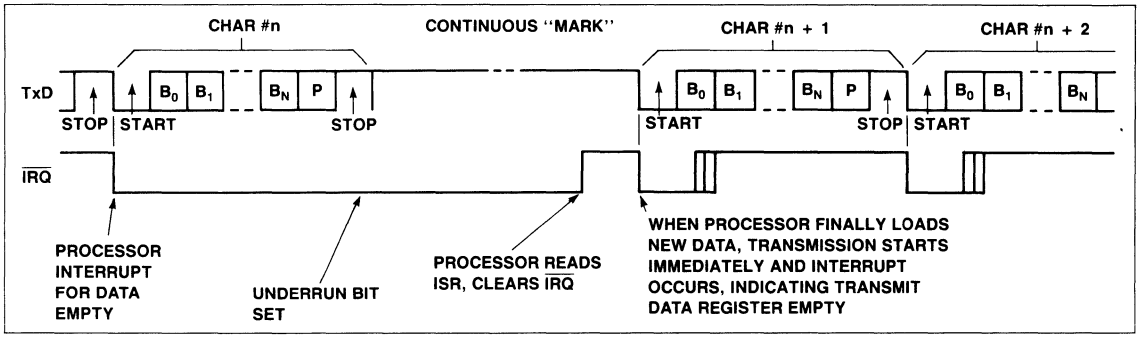


Figure 8. Transmit Underrun Condition Relationship

EFFECTS OF $\overline{CTS}$ ON TRANSMITTER

The $\overline{CTS}$ control line controls the transmission of data or the handshaking of data to a "busy" device (such as a printer). When the $\overline{CTS}$ line is low, the transmitter operates normally. Any transition on this line sets the $\overline{CTS}$ bit in the ISR. A high condition inhibits the TDRE bit in the ISR from becoming set. The word currently in the shift register continues to be sent but any word in the TDR is held until $\overline{CTS}$ goes low. At the high-to-low transition the $\overline{CTS}$ bit in the ISR is again set. Figure 9 shows the relationship of $\overline{IRQ}$, TxD, and $\overline{CTS}$ for the effects of $\overline{CTS}$ on the transmitter.

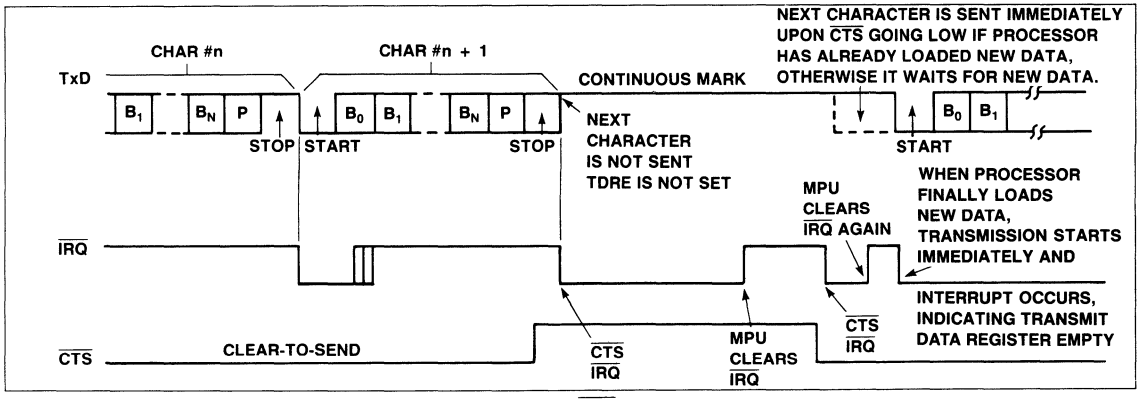


Figure 9. Effects of $\overline{CTS}$ on Transmitter

EFFECTS OF OVERRUN ON RECEIVER

If the processor does not read the RDR before the stop bit of the next word, an overrun error occurs, the overrun bit is set in the ISR, and the new data word is not transferred to the RDR. The RDR contains the last word not read by the MPU and all following data is lost. The receiver will return to normal operation when the RDR is read. Figure 10 shows the relation of $\overline{IRQ}$ and RxD for the effects of overrun on the receiver.

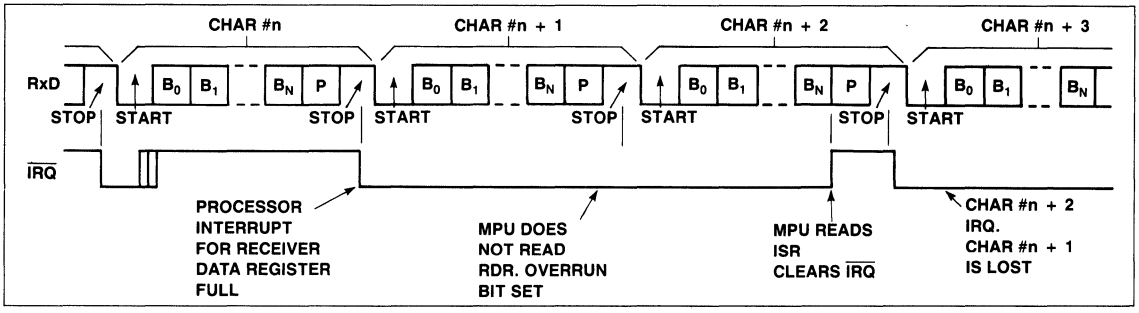


Figure 10. Effects of Overrun on Receiver

ECHO MODE TIMING

In the Echo Mode, the TxD line re-transmits the data received on the RxD line, delayed by 1/2 of a bit time. An internal underrun mode must occur before Echo Mode will start transmitting. In normal transmit mode if TDRE occurs (indicating end of data) an underflow flag would be set and continuous Mark transmitted. If Echo is initiated, the underflow flag will not be set at end of data and continuous Mark will not be transmitted. Figure 11 shows the relationship of RxD and TxD for Echo Mode.

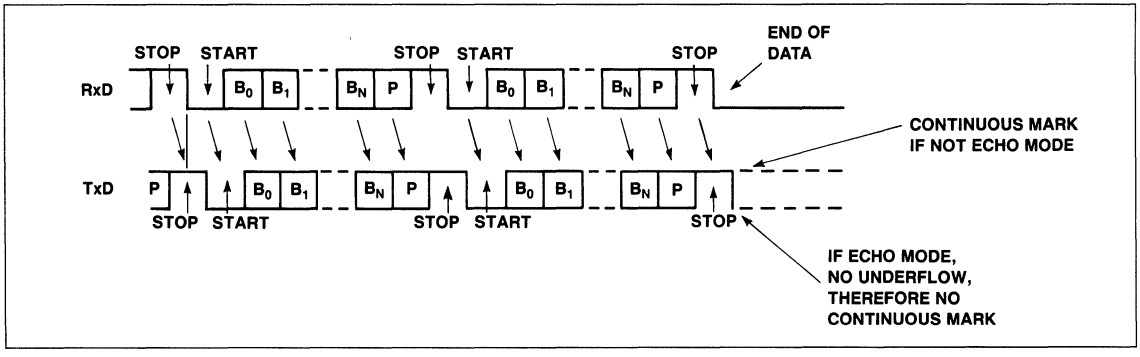


Figure 11. Echo Mode Timing

FRAMING ERROR

Framing error is caused by the absence of stop bit(s) on received data. The framing error bit is set when the RDRF bit is set. Subsequent data words are tested separately, so the status bit always reflects the last data word received. Figure 12 shows the relationship of $\overline{IRQ}$ and RxD when a framing error occurs.

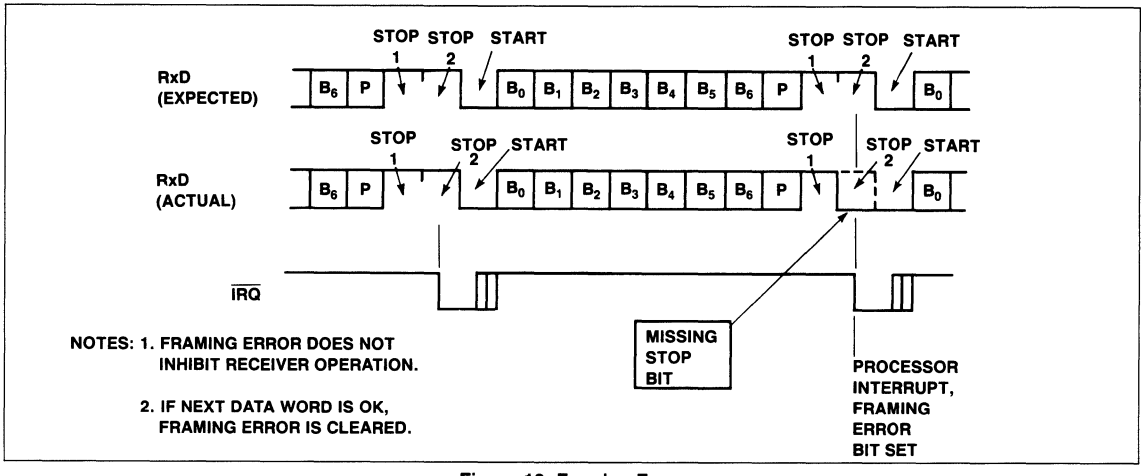


Figure 12. Framing Error

TRANSMIT BREAK CHARACTER

A Break may be transmitted by storing a value of $00 in the IER. After storing zero in the IER the Break is transmitted immediately. Care should be exercised so that a character in transmission is not disturbed inadvertently. The Break level lasts until other than $00 is stored in the IER at which time a stop bit is sent and transmission may resume. At least one full word time of Break will be sent regardless of the length of time between starting and stopping the Break character. Figure 13 shows the relationship of $\overline{IRQ}$ and TxD for a Transmit Break character.

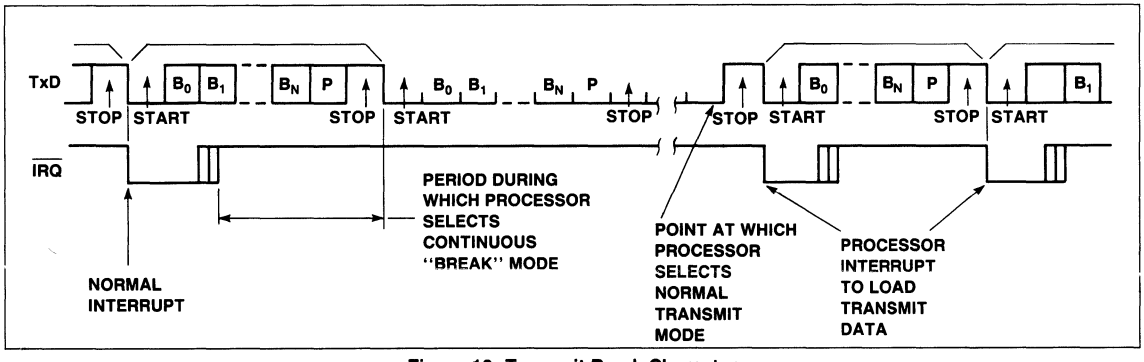


Figure 13. Transmit Break Character

RECEIVE BREAK CHARACTER

In the event that a Break character is received by the receiver, the Break bit is set. The receiver does not set the RDRF bit and remains in this state until a stop bit is received. At this time the next character is to be received normally. Figure 14 shows the relationship of $\overline{IRQ}$ and RxD for a Receive Break Character.

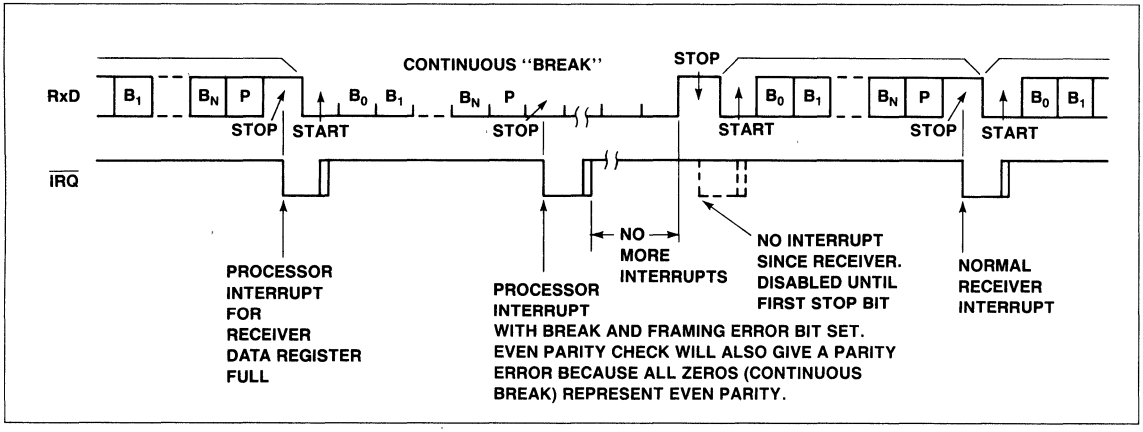


Figure 14. Receive Break Character

AUTOMATIC ADDRESS RECOGNITION

The DACIA offers a unique solution to the standard problem associated with multi-drop environment UARTs and communication interface controllers. In the standard configuration used by other devices, the slave CPU must be constantly interrupted to analyze incoming characters on the communications net to determine if an address word is present and if so, does that address match the address assigned to the slave UART. This CPU interrupt scheme can become intolerable in very large multi-drop networks because every slave on the communications net must "wake-up" it's CPU for every character sent down the network by the master. The end result is that the CPUs on the communications net are constantly being interrupted for the mundane task of address recognition.

To avoid this constant CPU interrupt problem, the DACIA has been designed to do address comparison and recognition internally without the need for CPU intervention. Therefore, the slave CPU is not interrupted until the DACIA has determined that the character sent over the communications net by the master was an address and the address matched the address stored in the DACIA Compare Register. At this point the DACIA interrupts the CPU, goes out of Compare Mode, and receives the string of characters being transmitted by the master, (i.e., the data characters). When all data has been received by the slave, it's CPU must again write the slave address into the DACIA Compare Register which automatically puts it back into the Compare Mode, waiting for another address character.

GENERATION OF NON-STANDARD BAUD RATES

Divisors

The internal counter/divider circuit selects the appropriate divisor for the crystal frequency by means of bits 0-3 of the CFR Control Register, as shown in Table 4.

Generating Other Baud Rates

By using a different crystal, other baud rates may be generated. These can be determined by:

$$\text{Baud Rate} = \frac{\text{Crystal Frequency}}{\text{Divisor}}$$

Furthermore, it is possible to drive the DACIA with an off-chip oscillator to achieve other baud rates. In this case, XTALI (pin 3) must be the clock input and XTALO (pin 4) must be a nonconnect.

Table 4. Divisor Selection

Control Register Bits				Divisor Selected For The Internal Counter	Baud Rate Generated With 3.6864 MHz Crystal	Baud Rate Generated With a Crystal of Frequency (f)
3	2	1	0			
0	0	0	0	73,728	(3 6864 x 10^6)/73,728 = 50	f/73,728
0	0	0	1	33,538	(3 6864 x 10^6)/33,538 = 109 92	f/33,538
0	0	1	0	27,408	(3 6864 x 10^6)/27,408 = 134 58	f/27,408
0	0	1	1	24,576	(3.6864 x 10^6)/24,576 = 150	f/24,576
0	1	0	0	12,288	(3 6864 x 10^6)/12,288 = 300	f/12,288
0	1	0	1	6,144	(3 6864 x 10^6)/6,144 = 600	f/6,144
0	1	1	0	3,072	(3.6864 x 10^6)/3,072 = 1,200	f/3,072
0	1	1	1	2,048	(3 6864 x 10^6)/2,048 = 1,800	f/2,048
1	0	0	0	1,536	(3 6864 x 10^6)/1,536 = 2,400	f/1,536
1	0	0	1	1,024	(3 6864 x 10^6)/1,024 = 3,600	f/1,024
1	0	1	0	768	(3 6864 x 10^6)/768 = 4,800	f/768
1	0	1	1	512	(3 6864 x 10^6)/512 = 7,200	f/512
1	1	0	0	384	(3.6864 x 10^6)/384 = 9,600	f/384
1	1	0	1	192	(3 6864 x 10^6)/192 = 19,200	f/192
1	1	1	0	96	(3.6864 x 10^6)/96 = 38,400	f/96
1	1	1	1	16	TxC/16 = Baud Rate or RxC/16 = Baud Rate	

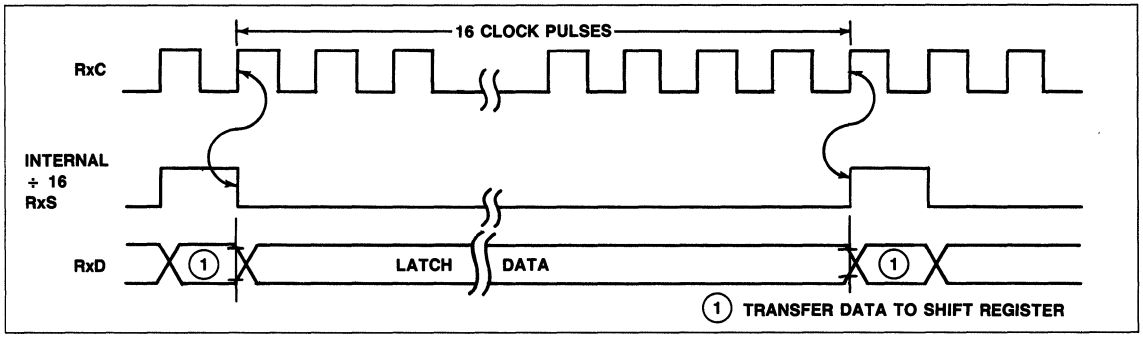


Figure 15. DACIA External Clock Timing — Receive Data

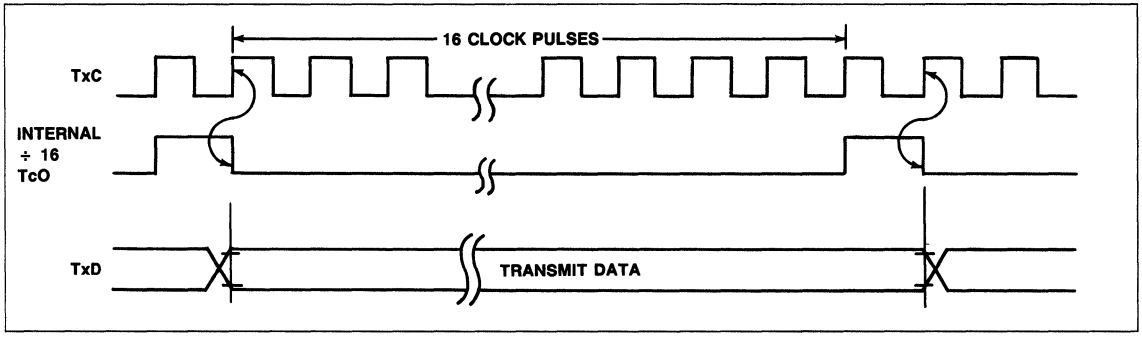


Figure 16. DACIA External Clock Timing — Transmit Data

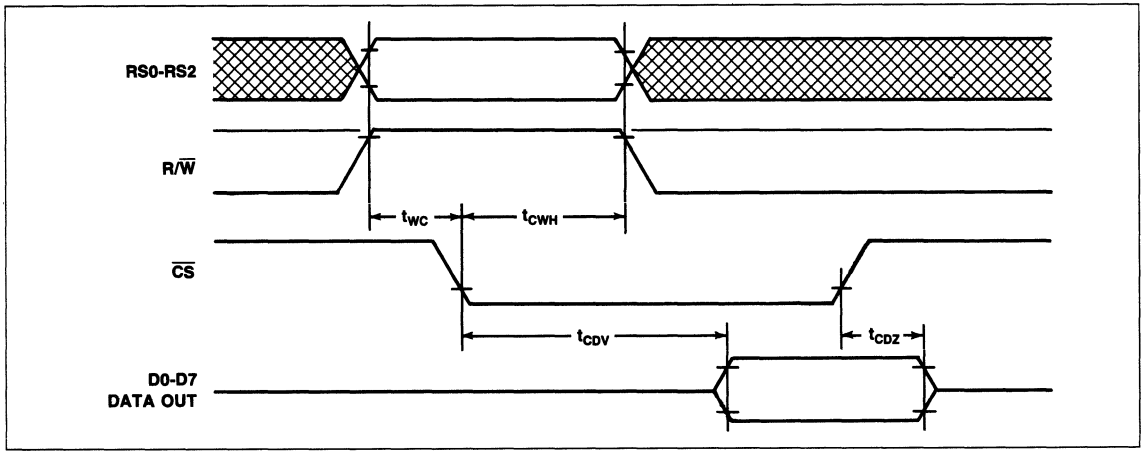
AC CHARACTERISTICS

(V_{CC} = 5.0V ±5%, V_{SS} = 0V, T_A = T_L to T_H)

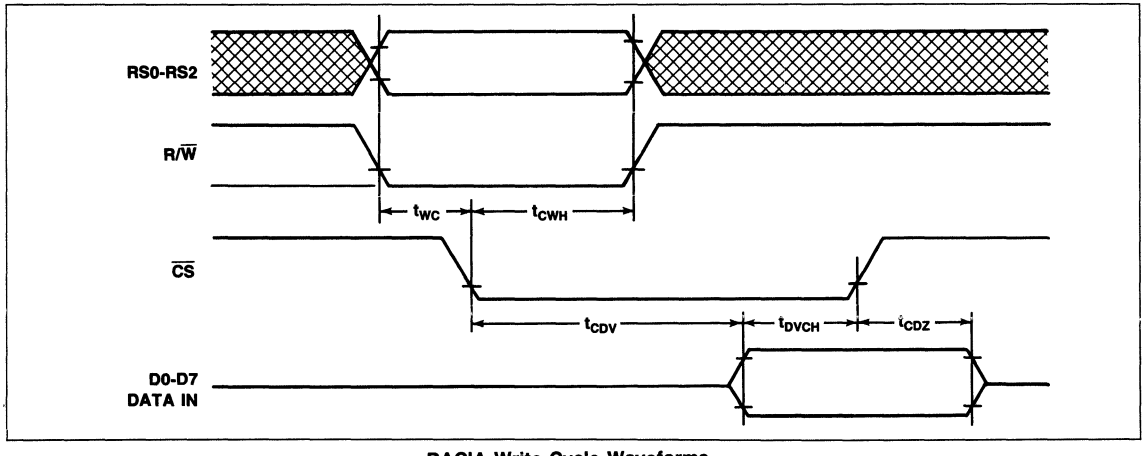
READ/WRITE TIMING

Characteristic	Symbol	2 MHz		4 MHz		Unit
		Min	Max	Min	Max	
R/$\overline{W}$, RS0–RS2 Valid to $\overline{CS}$ Low (Setup Time)	t_{WC}	0	—	0	—	ns
$\overline{CS}$ Low to R/$\overline{W}$, RS0–RS2 (Hold Time)	t_{CWH}	65	—	65	—	ns
$\overline{CS}$ Low to Data Valid	t_{CDV}	—	100	—	100	ns
$\overline{CS}$ High to Data Invalid (Hold Time)	t_{CDZ}	—	10	—	10	ns
Data Valid to $\overline{CS}$ High	t_{DVCH}	20		20		ns

Note:
1. All times are in nanoseconds.



DACIA Read Cycle Waveforms

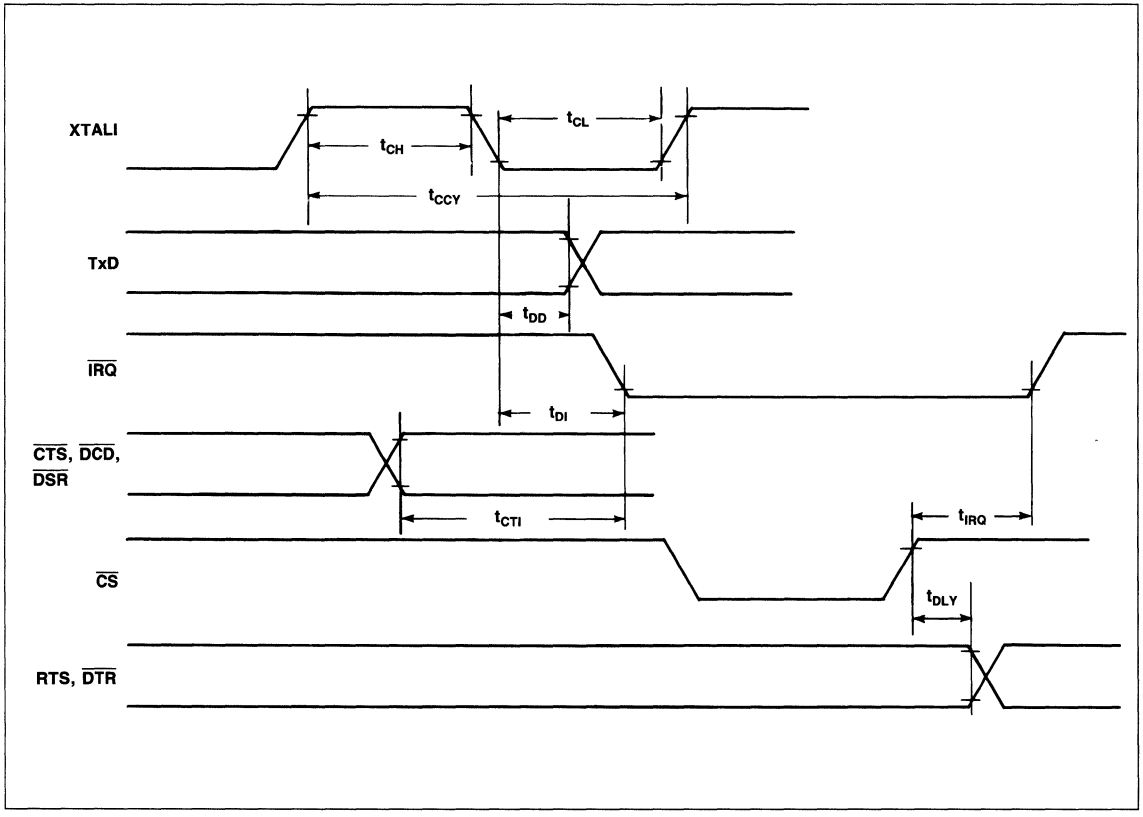


DACIA Write Cycle Waveforms

TRANSMIT/RECEIVE TIMING

Characteristic	Symbol	Min	Max	Unit
Transmit/Receive Clock Rate	t_{CCY}	250	—	ns
Transmit/Receive Clock High Time	t_{CH}	100	—	ns
Transmit/Receive Clock Low Time	t_{CL}	100	—	ns
XTALI to TxD Propagation Delay	t_{DD}	—	250	ns
XTALI to $\overline{IRQ}$ Propagation Delay	t_{DI}	—	250	ns
$\overline{CTS}$, $\overline{DCD}$, $\overline{DSR}$ to $\overline{IRQ}$	t_{CTI}	—	150	ns
$\overline{IRQ}$ Propagation Delay (Clear)	t_{IRQ}	—	150	ns
$\overline{RTS}$, $\overline{DTR}$ Propagation Delay	t_{DLY}	—	150	ns

Note:
1. All times are in nanoseconds.



DACIA Transmit/Receive Timing

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to +7.0	Vdc
Input Voltage	V_{IN}	−0.3 to V_{CC} +0.3	Vdc
Output Voltage	V_{OUT}	−0.3 to V_{CC} +0.3	Vdc
Operating Temperature Commercial Industrial	T_A	 0 to +70 −40 to +85	°C
Storage Temperature	T_{STG}	−55 to +150	°C

*NOTE: Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in other sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2

OPERATING CONDITIONS

Parameter	Symbol	Value
Supply Voltage	V_{CC}	5V ±5%
Temperature Range Commercial Industrial	T_A	 0° to 70°C −40°C to +85°C

DC CHARACTERISTICS

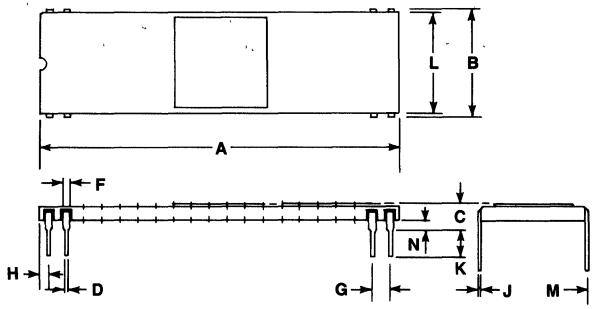
(V_{CC} = 5.0 V ±5%, V_{SS} = 0V, T_A = T_L to T_H, unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Conditions
Input High Voltage Except XTALI and XTALO XTALI and XTALO	V_{IH}	 +2.0 +2.4	 — —	 V_{CC} + 0.3 V_{CC} + 0.3	V	
Input Low Voltage Except XTALI and XTALO XTALI and XTALO	V_{IL}	 −0.3 −0.3	 — —	 +0.8 +0.4	V	
Input Leakage Current R/$\overline{W}$, $\overline{RES}$, RS0, RS1, RS2, RxD, $\overline{CTS}$, $\overline{DCD}$, $\overline{DSR}$, $\overline{RxC}$, $\overline{TxC}$, $\overline{CS}$	I_{IN}	—	10	 50	μA	V_{IN} = 0V to V_{CC} V_{CC} = 5.25V
Input Leakage Current for Three-State Off D0–D7	I_{TSI}	 —	 ±2	 10	 μA	V_{IN} = 0.4V to 2.4V V_{CC} = 5.25V
Output High Voltage D0–D7, TxD, CLK OUT, RTS, DTR	V_{OH}	+2.4 1.5	— —	— —	V	V_{CC} = 4.75V I_{LOAD} = −100 μA
Output Low Voltage D0–D7, TxD, CLK OUT, RTS, DTR	V_{OL}	—	—	+0.4	V	V_{CC} = 4.75V I_{LOAD} = 1.6 mA
Output Leakage Current (Off State) $\overline{IRQ}$	I_{OFF}	 —	 ±2	 ±10	 μA	V_{CC} = 5.25V V_{OUT} = 0 to 2.4V
Power Dissipation	P_D	—		10	mW/MHz	
Input Capacitance Except XTALI and XTALO XTALI and XTALO	C_{IN}	 — —	 — —	 5 10	 pF pF	V_{CC} = 5.0V V_{IN} = 0V f = 2 MHz T_A = 25°C
Output Capacitance	C_{OUT}	—	—	10	pF	

Notes:
1. All units are direct current (dc) except for capacitance.
2. Negative sign indicates outward current flow, positive indicates inward flow.
3. Typical values are shown for V_{CC} = 5.0V and T_A = 25°C.

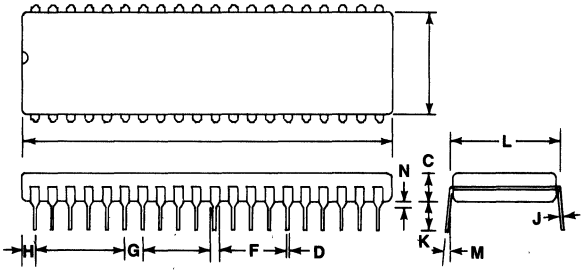
PACKAGE DIMENSIONS

40-PIN CERAMIC DIP



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	50 29	51 31	1 980	2 020
B	14 86	15 62	0 585	0 615
C	2 54	4 19	0 100	0 165
D	0 38	0 53	0 015	0 021
F	0 76	1 40	0 030	0 055
G	2 54 BSC		0 100 BSC	
H	0 76	1 78	0 030	0 070
J	0 20	0 33	0 008	0 013
K	2 54	4 19	0 100	0 165
L	14 60	15 37	0 575	0 605
M	0°	10°	0°	10°
N	0 51	1 52	0 020	0 060

40-PIN PLASTIC DIP



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	51 28	52 32	2 040	2 060
V	13 72	14 22	0 540	0 560
C	3 55	5 08	0 140	0 200
D	0 36	0 51	0 014	0 020
F	1 02	1 52	0 040	0 060
G	2 54 BSC		0 100 BSC	
H	1 65	2 16	0 065	0 085
J	0 20	0 30	0 008	0 012
K	3 05	3 56	0 120	0 140
L	15 24 BSC		0 600 BSC	
M	7°	10°	7°	10°
N	0 51	1 02	0 020	0 040

Rockwell

R6265, R6765
DOUBLE-DENSITY FLOPPY DISK CONTROLLER (DDFDC)

PRELIMINARY

2

DESCRIPTION

The R6765 Double-Density Floppy Disk Controller (DDFDC) interfaces up to four floppy disk drives to an 8-bit or 16-bit microprocessor-based system including Z 80, 8080A, 8085A, 8086, and 8088. The DDFDC simplifies the system design by minimizing both the number of external hardware components and software steps needed to implement the floppy disk drive (FDD) interface. Control signals supplied by the DDFDC reduce the number of components required in external phase locked loop and write precompensation circuitry. Memory-mapped registers containing commands, status and data simplify the software interface. Built-in functions reduce the software overhead needed to control the FDD interface. The DDFDC supports both the IBM 3740 Single-Density (FM) and IBM System 34 Double-Density (MFM) formats.

The R6265 interfaces to the 3½″ Sony Micro Floppy disk drive as well as 5¼″ and 8″ disk drives. The R6265 writes and reads in the Sony compatible format and can also read from disks formatted in IBM compatible format. A combination of up to four 3½″, 5¼″ and 8″ drives can be interfaced to and controlled by the R6265. The R6265 is pin-compatible with, and electrically identical to, the R6765.

The DDFDC interfaces directly to the synchronous microprocessor bus and operates with 8-bit byte length data transferred on the bus in either DMA or non-DMA mode. In DMA mode, the CPU need only load the command into the DDFDC and all data transfers occur under DMA control. The R6265/R6765 is directly compatible with the Z8410/μPD8257 Direct Memory Access Controller (DMAC). In non-DMA mode, the DDFDC generates an interrupt to the CPU indicating that a byte of data is available.

Controller commands, command or device status, and data are transferred between the DDFDC and the CPU via six internal registers. The Main Status Register (MSR) stores the DDFDC status information while four additional status registers provide result information to the CPU following each controller command. The Data Register (DR) stores actual disk data, parameters, controller commands and FDD status information for use by the CPU.

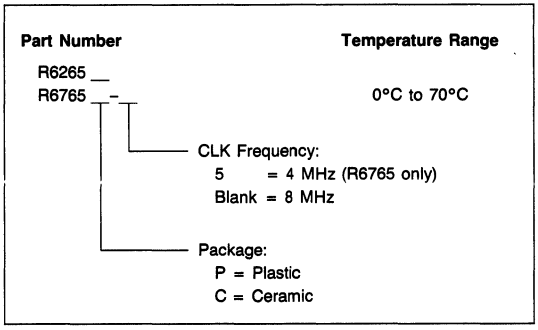
The DDFDC executes 15 separate multi-byte commands:

Read Data	Specify
Write Data	Format a Track
Read Deleted Data	Scan Equal
Write Deleted Data	Scan High or Equal
Read a Track	Scan Low or Equal
Read ID	Sense Interrupt Status
Seek	Sense Drive Status
Recalibrate (Restore to Track 0)	

FEATURES

- Address mark detection circuitry
- Software control of
  —Track stepping rate
  —Head load time
  —Head unload time
- Writes in:
  —IBM compatible (single- and double-density format (R6765)
  —Sony compatible (EMCA) format (R6265)
- Reads data written in:
  —IBM compatible format (R6265 and R6765)
  —Sony compatible format (R6265)
- Programmable data record lengths: 128, 256, 512, 1024, 2048, 4096 or 8192 bytes/sector
- Multi-sector and multi-track transfer capability
- Controls up to four floppy disk drives
- Data scan capability—will scan a single sector or an entire track of data fields, comparing on a byte-by-byte basis data in the processor's memory with data read from the disk
- Data transfers in DMA or non-DMA mode
- Parallel seek operations on up to four drives
- Directly compatible with an 8-bit or 16-bit synchronous microprocessor bus including Z-80/8080A/8085A, 8086, and 8088
- The R6765 replaces the NEC μPD765A and Intel 8272
- The R6265 replaces the NEC μPD7265
- Single phase 4 or 8 MHz clock (R6765) or 8 MHz clock (R6265)
- Single +5 volt power supply

ORDERING INFORMATION



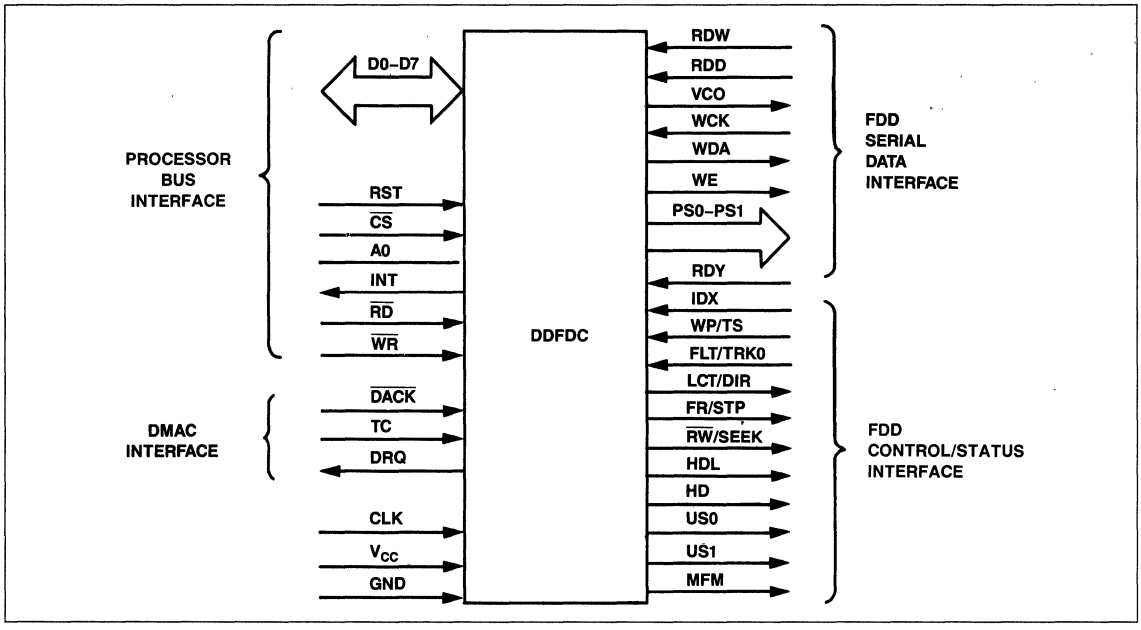


Figure 1. DDFDC Input and Output Signals

PIN DESCRIPTION

Throughout this document signals are presented using the terms active and inactive, or asserted and negated, independent of whether the signal is active in the high-voltage state or low-voltage state. (The active state of each logic pin is described below.) Active low signals are denoted by a superscript bar.

BUS INTERFACE

D0-D7—Data Lines. The bidirectional data lines transfer data between the DDFDC and the 8-bit data bus.

CLK—CLOCK. The clock is a TTL compatible 4 or 8 MHz square wave signal.

RST—RESET. This active high input places the DDFDC in the idle state and resets the output lines to the floppy disk drive (FDD) to the low state. RST does not affect the Step Rate Time (SRT), Head Unload Time (HUT) or Head Load Time (HLT) set by a Specify command. If RDY goes high while RST is high, the DDFDC will assert INT within 1.024 ms. This interrupt can be cleared by issuing a Sense Interrupt Status command.

$\overline{CS}$—Chip Select. The DDFDC is selected when the $\overline{CS}$ input is low.

A0—Data/Status Register Select. This input selects the Data or Status Register for reading from or writing to. When A0 = high, the Data Register is selected and the state of $\overline{RD}$ or $\overline{WR}$ determines whether it is a read ($\overline{RD}$ = low) or a write ($\overline{WR}$ = low) operation. When A0 = low, the Status Register is selected. This register may only be read ($\overline{RD}$ = low); the state $\overline{WR}$ = low is invalid when the Status Register is selected.

INT—Interrupt Request. This active high output is the interrupt request generated by the DDFDC to the CPU. INT is asserted upon completion of some DDFDC commands and before a data byte is transferred between the DDFDC and the data bus (in the Non-DMA mode).

$\overline{RD}$—Read. This active low input defines the data bus transfer as a read cycle. When low, the data transfer is from the DDFDC to the data bus.

$\overline{WR}$—Write. This active low input defines the data bus transfer as a write cycle. When low, the data transfer is from the data bus to the DDFDC.

DIRECT MEMORY ACCESS CONTROLLER (DMAC) INTERFACE

$\overline{DACK}$—DMA Acknowledge. The DMA transfer acknowledge signal is a TTL compatible input generated by the DMA controller (DMAC) controlling the DDFDC. The DMA cycle is active when $\overline{DACK}$ is low and the DDFDC is performing a DMA transfer.

DRQ—Data DMA Request. The transfer request signal is a TTL compatible output generated by the DDFDC to request a data transfer operation under control of the DMAC (in the DMA mode). The request is active when DRQ = high. The signal is reset inactive when DMA Acknowledge ($\overline{DACK}$) is asserted (low).

TC—Terminal Count. This input signal is issued to the DDFDC when the DMA transfer for a channel is complete. The signal is active high concurrent with the $\overline{DACK}$ input when the DMA operation is complete as a result of that transfer.

FDD SERIAL DATA INTERFACE

RDD—Read Data. Read Data input from the floppy disk drive (FDD) containing clock and data bits.

RDW—Read Data Window. Data Window input generated by the Phase Locked Loop (PLL) and used to sample data from the FDD.

VCO—Voltage Controlled Oscillator Sync. This output signal inhibits the VCO in the PLL circuit when low and enables the VCO in the PLL circuit when high. This inhibits RDD and RDW from being generated until valid data is detected from the FDD.

WCK—Write Clock. This input clock determines the Write Data rate to the FDD. The data rate is 500 KHz in the FM mode (MFM = low) and 1 MHz in the MFM mode (MFM = high). The pulse width is 250 ns (typical) in both modes.

WDA—Write Data. Serial write data output to the FDD containing both clock and data bits.

WE—Write Enable. This output signal enables the Write Data into the FDD when high.

PS0-PS1—Preshift. These outputs are encoded to convey write compensation status during the MFM mode to determine early, late or normal times as follows:

Write Precompensation Status	Preshift Outputs	
	PS0	PS1
Normal	0	0
Late	0	1
Early	1	0
Invalid	1	1
0 = Low, 1 = High		

FDD STATUS INTERFACE

RDY—Ready. An active high input signal indicates the FDD is ready to send data to, or receive data from, the DDFDC.

IDX—Index. An active high input signal from the FDD indicates the index hole is under the index sensor. Index is used to synchronize DDFDC timing.

$\overline{RW}$/SEEK—Read Write/Seek. Mode selection signal to the FDD which controls the multiplexer from the multiplexed signals. When $\overline{RW}$/SEEK is low, the Read/Write mode is commanded; when $\overline{RW}$/SEEK is high, the Seek mode is commanded.

$\overline{RW}$/SEEK	Mode	Active FDD Interface Signals
Low	Read/Write	WP, FLT, LCT, FR
High	Seek	TS, TRK0, DIR, STP

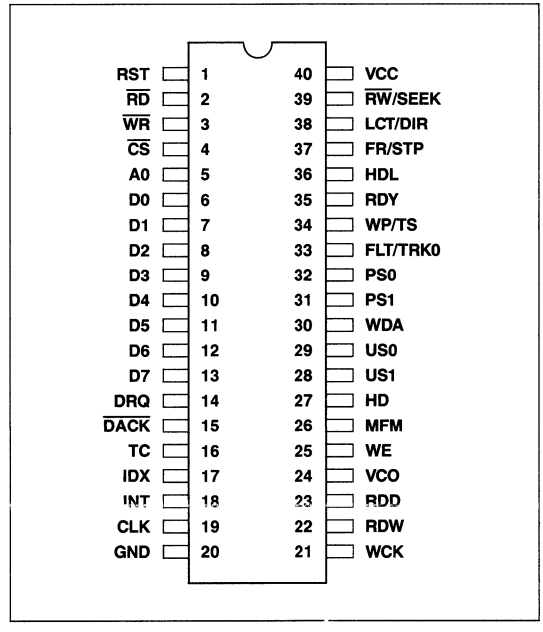
WP/TS—Write Protect/Two Side. An active high multiplexed input signal from the FDD. In the Read/Write mode, WP/TS high indicates the media is write-protected. In the Seek mode, WP/TS high indicates the media is two-sided.

FLT/TRK0—Fault/Track Zero. An active high multiplexed input from the FDD. In the Read/Write mode ($\overline{RW}$/SEEK = low), FLT/TRK0 high indicates an FDD fault. In the Seek mode, FLT/TRK0 high indicates that the read/write head is positioned over track zero.

LCT/DIR—Low Current/Direction. A multiplexed output to the FDD. In the Read/Write mode, LCT/DIR is low when the read/write head is to be positioned over the inner tracks and the LCT/DIR is high when the head is to be positioned over the outer tracks. In the Seek mode, LCT/DIR controls the head direction. When LCT/DIR is high, the head steps to the outside of the disk; when LCT/DIR is low, the head steps to the inside of the disk.

FR/STP—Fault Reset/Step. A multiplexed output to the FDD. In the Read/Write mode, FR/STP high resets the fault indicator in the FDD. An FR pulse is issued at the beginning of each read or write command prior to issuing HDL. In the Seek mode, FR/STP provides the step pulses to move the read/write head to another track in the direction indicated by the LCT/DIR signal.

HDL—Head Load. An active high output to notify the FDD that the read/write head should be loaded (placed in contact with the media). A low level indicates the head should be unloaded.



DDFDC Pin Diagram

HD—Head Select. An output to the FDD to select the proper read/write head. Head One is selected when HD = high and Head Zero is selected when HD = low.

US0-US1—Unit Select. Output signals for floppy disk drive selection as follows:

Unit Select		Floppy Disk Drive Select
US0	US1	
0	0	0
0	1	1
1	0	2
1	1	3
0 = Low, 1 = High		

MFM—MFM Mode. Output signal to the FDD to indicate MFM or FM mode. Selects the MFM mode when MFM = high and the FM mode MFM = Low.

VCC—Power. +5 Vdc.

GND-Ground (V_{ss}).

DDFDC REGISTERS

The DDFDC contains six registers which may be accessed by the processor or DMA controller via the system (i.e., microprocessor) bus: a Main Status Register, a Data Register, and four Result Status Registers. The 8-bit Main Status Register (MSR) contains the status information of the DDFDC, and may be accessed at any time. The 8-bit Data Register, consisting of several registers in a stack with only one register presented to the data bus at a time, stores data, commands, parameters and FDD status information. Bytes of data are read out of, or written into, the Data Register in order to initiate a command or to obtain the results of a command execution.

The read-only Main Status Register facilitates the transfer of data between the system and the DDFDC. The other Status Registers (ST0, ST1, ST2 and ST3) are only available during the result phase, and may be read only after completing a command. The particular command which has been executed determines how many of the Status Registers will be read.

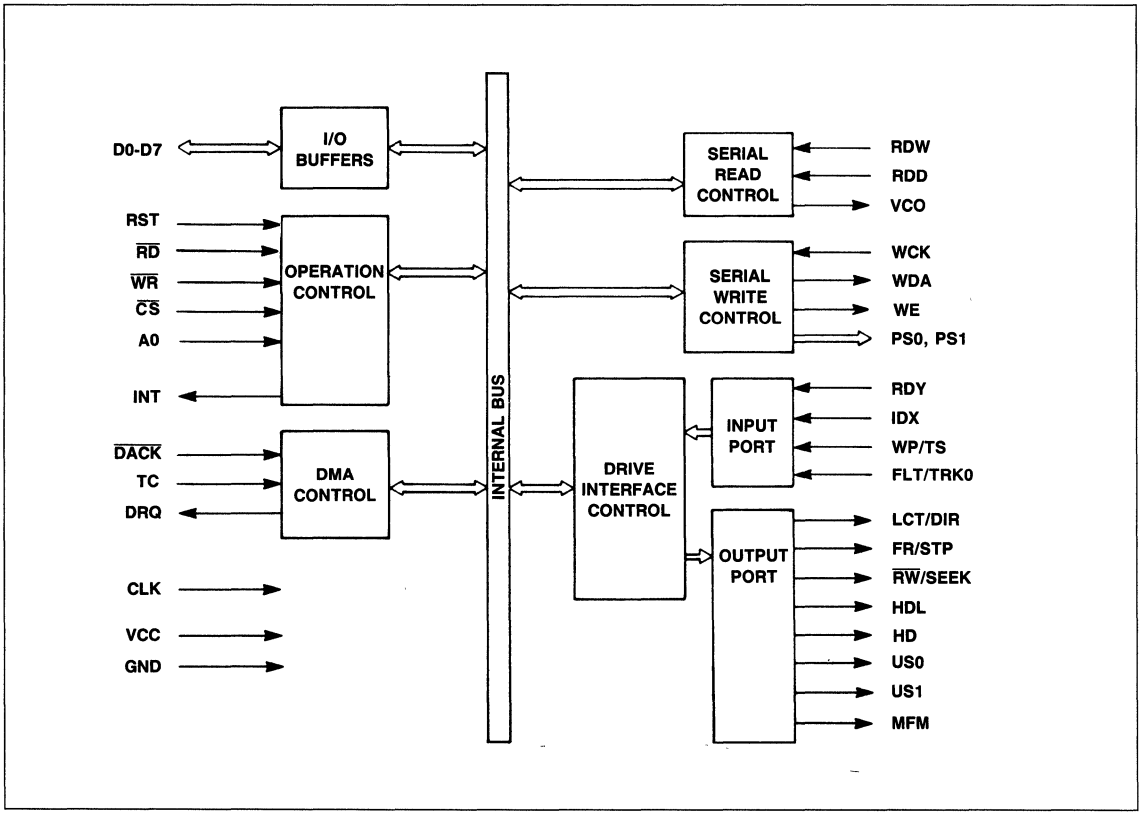


Figure 2. DDFDC Block Diagram

The relationship between the status/data registers and the $\overline{WR}$, $\overline{RD}$ and A0 signals is shown below.

A0	$\overline{RD}$	$\overline{WR}$	Function
0	0	0	Illegal
0	0	1	Read Main Status Register
0	1	0	Illegal
1	0	0	Illegal
1	0	1	Read from Data Register
1	1	0	Write into Data Register
0 = Low, 1 = High			

Table 1 shows each of the status registers used by the DDFDC and each bit assignment within the individual registers. Table 2 defines the symbols used throughout the command definitions. Each register bit symbol is defined in the register descriptions that follow Table 2.

REGISTER DEFINITIONS

Main Status Register (MSR)

7	6	5	4	3	2	1	0
RQM	DIO	EXM	CB	D3B	D2B	D1B	D0B

The Main Status Register (MSR) contains the status information of the DDFDC, and must be read by the processor before each byte is written to, or read from, the Data Register during the command or result phase. MSR reads are not required during the execution phase. The Data Input/Output (DIO) and Request for Master (RQM) bits in the MSR indicate when data is ready and in which direction data will be transferred on the data bus. The maximum time between the last $\overline{RD}$ or $\overline{WR}$ during command or result phases and the DIO and RQM getting set or reset is 12 μs. For this reason, every time the MSR is read the processor should wait 12 μs. The maximum time from the trailing edge of the last $\overline{RD}$ in the result phase to when bit 4 (DDFDC Busy) goes low is also 12 μs.

The DIO and RQM timing chart is shown in Figure 3.

MSR
7 RQM —Request for Master.
0 Data Register is not ready.
1 Data Register is ready.

MSR
6 DIO —Data Input/Output.
0 Data transfer is from system to the Data Register.
1 Data transfer is from Data Register to the system.

MSR
5 EXM —Execution Mode. (Non-DMA mode only).
0 Execution phase ended, result phase begun.
1 Execution phase started.

MSR
4 CB —Controller (DDFDC) Busy.
0 DDFDC is not busy, will accept a command.
1 DDFDC is busy, will not accept a command.

MSR
3 D3B —Floppy Disk Drive (FDD) 3 Busy.
0 FDD 3 is not busy, DDFDC will accept read or write command.
1 FDD 3 is busy, DDFDC will not accept read or write command.

MSR
2 D2B —FDD 2 Busy.
0 FDD 2 is not busy, DDFDC will accept read or write command.
1 FDD 2 is busy, DDFDC will not accept read or write command.

MSR
1 D1B —FDD 1 Busy.
0 FDD 1 is not busy, DDFDC will accept read or write command.
1 FDD 1 is busy, DDFDC will not accept read or write command.

MSR
0 D0B —FDD 0 Busy.
0 FDD 0 is not busy, DDFDC will accept read or write command.
1 FDD 0 is busy, DDFDC will not accept read or write command.

Status Register 0 (ST0)

7	6	5	4	3	2	1	0
IC		SE	EC	NR	HD	US	
						US1	US0

The Status Register 0 (ST0) as well as the other status registers (ST1-ST3), are available only during the result phase, and may be read only after completing a command. The particular command executed determines which status registers are used and may be read.

ST0
7 6 IC —Interrupt Code.
0 0 Normal Termination (NT). Command was properly executed and completed.
0 1 Abnormal Termination (AT). Command execution was started, but was not successfully completed.
1 0 Invalid Command (IC). Received command was invalid.
1 1 Abnormal Termination (AT). The Ready (RDY) signal from the FDD changed state during command execution.

ST0
5 SE —Seek End.
0 Seek command is not completed.
1 Seek command completed by DDFDC.

ST0
4 EC —Equipment Check.
0 No error.
1 Either a fault signal is received from the FDD or the track 0 signal failed to occur after 256 step pulses (Recalibrate command).

Table 1. DDFDC Status Register Bit Assignments

	Bit Number							
	7	6	5	4	3	2	1	0
Main Status Register (MSR)	RQM	DIO	EXM	CB	D3B	D2B	D1B	D0B
Status Register 0 (ST0)	IC		SE	EC	NR	HD	US	
							US1	US0
Status Register 1 (ST1)	EN	0	DE	OR	0	ND	NW	MA
Status Register 2 (ST2)	0	CM	DD	WT	SH	SN	BT	MD
Status Register 3 (ST3)	FLT	WP	RDY	TRK0	TS	HD	US1	US0

Table 2. Command Symbol Description

Symbol	Name	Description
A0	Address Line A0	Controls selection of Main Status Register (A0 = low) or Data Register (A0 = high).
D	Data	The data pattern which is going to be written into a sector
D0-D7	Data Bus	8-bit data bus, where D0 is the least significant data line and D7 is the most significant data line.
DTL	Data Length	When N is defined as 00, DTL is the number of data bytes to read from or write into the sector
EOT	End of Track	The final sector number on a track. During read or write operation, the DDFDC stops data transfer after reading from or writing to the sector equal to EOT.
GPL	Gap Length	The length of Gap 3. During read/write commands this value determines the number of bytes that the VCO will stay low after two CRC bytes. During the Format a Track command it determines the size of Gap 3.
H	Head Address	Head number 0 or 1, as specified in ID field.
HD (H)	Head	A selected head number 0 or 1 which controls the polarity of pin 27. (H = HD in all command words).
HLT	Head Load Time	The head load time in the FDD (2 to 254 ms in 2 ms increments).
HUT	Head Unload Time	The head unload time after a read or write operation has occurred (16 to 240 ms in 16 ms increments)
MF	FM or MFM Mode	When MF = 0, FM mode is selected; and when MF = 1, MFM mode is selected.
MT	Multi-Track	When MT = 1, a multi-track operation is to be performed. After finishing a read/write operation on side 0, the DDFDC will automatically start searching for sector 1 on side 1.
N	Bytes/Sector	The number of data bytes written in a sector.
ND	Non-DMA Mode	When ND = 1, operation is in the Non-DMA mode; when ND = 0, operation is in the DMA mode.
NTN	New Track Number	A new track number, which will be reached as a result of the Seek command. Desired head position.
PTN	Present Track Number	The track number at the completion of Sense Interrupt Status command. Present head position.
R	Record (Sector)	The sector number to be read or written.
R/W	Read/Write	Either read (R) or write (W) signal.
ST	Sectors/Track	The number of sectors per track.
SK	Skip	Skip Deleted Data Address Mark.
SRT	Step Rate Time	The stepping rate for the FDD (1 to 16 ms in 1 ms increments). Stepping rate applies to all drives (F = 1 ms, E = 2 ms, etc.)
ST0 ST1 ST2 ST3	Status 0 Status 1 Status 2 Status 3	Four registers which store the status information after a command has been executed. This information is available during the result phase after command execution. These registers should not be confused with the Main Status Register (selected by A0 = low). ST0-ST3 may be read only after a command has been executed and contain information relevant to that particular command.
STP	Sector Test Process	During a Scan command, if STP = 01, the data in contiguous sectors is compared byte by byte with data sent from the processor (or DMA controller); and if STP = 02, then alternate sectors are read and compared.
T	Track Number	The current/selected track number of the medium (0–255).
US0,US1	Unit Select	A selected drive number (0-3).

ST0
3 NR —Not Ready.
0 FDD is ready.
1 FDD is not ready at issue of read or write command. If a read or write command is issued to side 1 of a single-sided drive, this bit is also set.

ST0
2 HD —Head Address. (At Interrupt).
0 Head Select 0.
1 Head Select 1.

ST0
1 0 US —Unit Selected. (At Interrupt).
0 0 FDD 0 selected.
0 1 FDD 1 selected.
1 0 FDD 2 selected.
1 1 FDD 3 selected.

Status Register 1 (ST1)

7	6	5	4	3	2	1	0
EN	0	DE	OR	0	ND	NW	MA

ST1
7 EN —End of Track.
0 No error.
1 DDFDC attempted to access a sector beyond the last sector of a track.

ST1
6 —Not Used. Always Zero.

ST1
5 DE —Data Error.
0 No error.
1 DDFDC detected a CRC error in ID field or the Data field.

ST1
4 OR —Overrun.
0 No error.
1 DDFDC was not serviced by the system during data transfers, within a predetermined time interval.

ST1
3 —Not Used. Always Zero.

ST1
2 ND —No Data.
0 No error.
1 3 possible errors.

1. DDFDC cannot find sector specified in the Internal Data Register (IDR) during execution of Read Data, Write Deleted Data or Scan commands.
2. DDFDC cannot read ID field without an error during Read ID command.
3. DDFDC cannot find starting sector during execution of Read a Track command.

ST1
1 NW —Not Writable.
0 No error.
1 DDFDC detected a write protect signal from FDD during execution of Write Data, Write Deleted Data or Format a Track commands.

ST1
0 MA —Missing Address Mark.
0 No error.
1 2 possible errors.

1. DDFDC cannot detect the ID Address Mark after encountering the index hole twice.
2. DDFDC cannot detect the Data Address Mark or Deleted Data Address Mark. The MD (Missing Address Mark in Data field) of Status Register 2 is also set.

Status Register 2 (ST2)

7	6	5	4	3	2	1	0
0	CM	DD	WT	SH	SN	BT	MD

ST2
7 —Not Used. Always Zero.

ST2
6 CM —Control Mark.
0 No error.
1 DDFDC encountered a sector which contained a Deleted Data Address Mark during execution of a Read Data, Read a Track, or Scan command, or which contained a Data Address Mark during execution of a Read Deleted Data command.

ST2
5 DD —Data Error in Data Field.
0 No error.
1 DDFDC detected a CRC error in the Data field.

ST2
4 WT —Wrong Track.
0 No error.
1 Contents of T on the disk is different from that stored in IDR. Bit is related to ND (Bit 2) of Status Register 1.

ST2
3 SH —Scan Equal Hit.
0 No "equal" condition during a scan command.
1 "Equal" condition satisfied during a scan command.

ST2
2 SN —Scan Not Satisfied.
0 No error.
1 DDFDC cannot find a sector on the track which meets the scan command condition.

ST2
1 **BT —Bad Track.**
0 No error.
1 Contents of T on the disk is different from that stored in the IDR and T = FF. Bit is related to ND (Bit 2) of Status Register 1.

ST2
0 **MD —Missing Address Mark In Data Field.**
0 No error.
1 DDFDC cannot find a Data Address Mark or Deleted Data Address Mark during a data read from the disk.

Status Register 3 (ST3)

7	6	5	4	3	2	1	0
FLT	WP	RDY	TRK0	TS	HD	US1	US0

Status Register 3 (ST3) holds the results of the Sense Drive Status command.

ST3
7 **FLT —Fault.**
0 Fault (FLT) signal from the FDD is low.
1 Fault (FLT) signal from the FDD is high.

ST3
6 **WP —Write Protect.**
0 Write Protect (WP) signal from the FDD is low.
1 Write Protect (WP) signal from the FDD is high.

ST3
5 **RDY —Ready.**
0 Ready (RDY) signal from the FDD is low.
1 Ready (RDY) signal from the FDD is high.

ST3
4 **TRK0 —Track 0.**
0 Track 0 (TRK0) signal from the FDD is low.
1 Track 0 (TRK0) signal is from the FDD is high.

ST3
3 **TS —Two Side.**
0 Two Side (TS) signal from the FDD is low.
1 Two Side (TS) signal from the FDD is high.

ST3
2 **HD —Head Select.**
0 Head Select (HD) signal to the FDD is low.
1 Head Select (HD) signal to the FDD is high.

ST3
1 **US1 —Unit Select 1.**
0 Unit Select 1 (US1) signal to the FDD is low.
1 Unit Select 1 (US1) signal to the FDD is high.

ST3
0 **US0 —Unit Select 0.**
0 Unit Select 0 (US0) signal to the FDD is low.
1 Unit Select 0 (US1) signal to the FDD is high.

COMMAND SEQUENCE

The DDFDC is capable of performing 15 different commands. Each command is initiated by a multi-byte transfer of data from the system. After command execution, the result of the command may be a multi-byte transfer of data back to the system. Because of this multi-byte transfer of information between the DDFDC and the system, each command consists of three phases:

Command Phase—The DDFDC receives all information required to perform a particular operation from the system.

Execution Phase—The DDFDC performs the instructed operation.

Result Phase—After completion of the operation, status and other housekeeping information are made available to the system.

The bytes of data sent to the DDFDC to form a command, and read out of the DDFDC in the result phase, must occur in the order shown for each command sequence. That is, the command code byte must be sent first followed by the other bytes in the specified sequence. All command bytes must be written and all result bytes must be read in each phase. After the last byte of data in the command phase is received by the DDFDC, the execution phase starts. Similarly, when the last byte of data is read out in the result phase, the command is ended and the DDFDC is ready to accept a new command. A command can be terminated by asserting the Terminal Count (TC) signal to the DDFDC. This ensures that the processor can always get the DDFDC's attention even if the command in process hangs up in an abnormal manner.

COMMAND DESCRIPTION

READ DATA

A command set of nine bytes places the DDFDC into the Read Data mode. After the Read Data command has been received the DDFDC loads the head (if it is unloaded), waits the specified Head Settling Time (defined in the Specify command), then begins reading ID Address Marks and ID fields from the disk. When the current sector number (R) stored in the ID Register (IDR) matches the sector number read from the disk, the DDFDC transfers data from the disk Data field to the data bus.

After completion of the read operation from the current sector, the DDFDC increments the Sector Number (R) by one, and the data from the next sector is read and output to the data bus. This continuous read function is called a "Multi-Sector Read Operation." The Read Command terminates after reading the last data byte from sector R when R = EOT. ST0 bits 7 and 6 are set to 0 and 1, respectively, and ST1 bit 7 (EN) is set to a 1.

The Read Data command can also be terminated by a high Terminal Count (TC) signal. TC should be issued at the same time that the $\overline{\text{DACK}}$ for the last byte of data is sent. Upon receipt of TC, the DDFDC stops outputting data to the data bus, but continues to read data from the current sector, checks CRC (Cyclic Redundancy Count) bytes, and then at the end of that sector terminates the Read Data command and sets bits 7 and 6 in ST0

to 0. The amount of data which can be handled with a single command to the DDFDC depends upon MT (Multi-Track), MF (MFM/FM), and N (Number of Bytes/Sector) values. Table 3 shows the transfer capacity.

The multi-track function (MT) allows the DDFDC to read data from both sides of the disk. For a particular track, data is transferred starting at sector 1, side 0 and completed at sector L, side 1 (sector L = last sector on the side). This function pertains to only one track (the same track) on each side of the disk.

When N = 0 in command byte 6 (FM mode), the Data Length (DTL) in command byte 9 defines the data length that the DDFDC must treat as a sector. If DTL is smaller than the actual data length in a sector, the data beyond the DTL is not sent to the data bus. The DDFDC reads (internally) the complete sector, performs the CRC check, and depending upon the manner of command termination, may perform a multi-sector Read operation. When N is non-zero (MFM mode), DTL has no meaning and should be set to FF.

At the completion of the Read Data command, the head is not unloaded until the Head Unload Time (HUT) interval defined in the Specify command has elapsed. The head settling time may be avoided between subsequent reads if the processor issues another command before the head unloads. This time savings is considerable when disk contents are copied from one drive to another.

If the DDFDC detects the Index Hole twice in succession without finding the right sector (indicated in R), then the DDFDC sets the No Data (ND) flag in Status Register 1 (ST1) to a 1, sets Status Register 0 (ST0) bits 7 and 6 to 0 and 1, respectively, and terminates the Read Data command.

After reading the ID and Data fields in each sector, the DDFDC checks the CRC bytes. If a read error is detected (incorrect CRC in ID field), the DDFDC sets the Data Error (DE) flag in ST1 to a 1, sets the Data Error in Data Field (DD) flag in ST2 to a 1 if a CRC error occurs in the Data field, sets bits 7 and 6 in ST0 to 0 and 1, respectively, and terminates the command.

If the DDFDC reads a **Deleted Data Address Mark** from the disk, and the Skip Deleted Data Address Mark bit in the first command byte is not set (SK = 0), then the DDFDC reads all the data in the sector, sets the Control Mark (CM) flag in ST2 to a 1, and terminates the command. If SK = 1, the DDFDC skips the sector with the **Deleted Data Address Mark** and reads the next sector. The CRC bits in the deleted data field are not checked when SK = 1.

During disk data transfers from the DDFDC to the system, the DDFDC must be serviced by the system within 27 μs in the FM mode, and within 13 μs in the MFM mode, otherwise the DDFDC sets the Over Run (OR) flag in ST1 to a 1, sets bits 7 and 6 in ST0 to 0 and 1, respectively, and terminates the command.

If the processor terminates a read (or write) operation in the DDFDC, then the ID information in the result phase is dependent upon the state of the MT bit in the first command byte and the End of Track (EOT) byte. Table 4 shows the values for Track Number (T), Head Number (H), Sector Number (R), and Number of Data Bytes/Sector (N), when the processor terminates the command.

Command Phase:

R/W	BYTE	7	6	5	4	3	2	1	0
W	1	MT	MF	SK	0	0	1	1	0
	2	X	X	X	X	X	HD	US1	US0
	3	Track Number (T)							
	4	Head Number (H)							
	5	Sector Number (R)							
	6	Number of Data Bytes per Sector (N)							
	7	End of Track (EOT)							
	8	Gap Length (GPL)							
	9	Data Length (DTL)							

Table 3. DDFDC Transfer Capacity

Multi-Track (MT)	MFM/FM (MF)	Bytes/Sector (N)	Maximum Transfer Capacity (Bytes/Sector) (Number of Sectors)	Final Sector Read from Disk
0	0	00	(128) (26) = 3,328	26 at Side 0
0	1	01	(256) (26) = 6,656	or 26 at Side 1
1	0	00	(128) (52) = 6,656	26 at Side 1
1	1	01	(256) (52) = 13,312	
0	0	01	(256) (15) = 3,840	15 at Side 0
0	1	02	(512) (15) = 7,680	or 15 at Side 1
1	0	01	(256) (30) = 7,680	15 at Side 1
1	1	02	(512) (30) = 15,360	
0	0	02	(512) (8) = 4,096	8 at Side 0
0	1	03	(1024) (8) = 8,192	or 8 at Side 1
1	0	02	(512) (16) = 8,192	8 at Side 1
1	1	03	(1024) (16) = 16,384	

Table 4. DDFDC Command Termination Values

Command Phase ID		Final Sector Transferred to/from Data Bus	Result Phase ID			
Multi-Track (MT)	Head Number (HD)		Track Number (T)	Head Number (H)	Sector Number (R)	No. of Data Bytes (N)
0	0	Less than EOT	NC	NC	R + 1	NC
	0	Equal to EOT	T + 1	NC	01	NC
	1	Less than EOT	NC	NC	R + 1	NC
	1	Equal to EOT	T + 1	NC	01	NC
1	0	Less than EOT	NC	NC	R + 1	NC
	0	Equal to EOT	NC	LSB	01	NC
	1	Less than EOT	NC	NC	R + 1	NC
	1	Equal to EOT	T + 1	LSB	01	NC

Notes:
1. NC (No Change): The same value as the one at the beginning of command execution.
2. LSB (Least Significant Bit): The least significant bit of H is complemented.

Result Phase:

R	1	Status Register 0 (ST0)
	2	Status Register 1 (ST1)
	3	Status Register 2 (ST2)
	4	Track Number (T)
	5	Head Number (H)
	6	Sector Number (R)
	7	Number of Data Bytes per Sector (N)

WRITE DATA

A command set of nine bytes places the DDFDC in the Write Data mode. After the Write Data command has been received the DDFDC loads the head (if it is unloaded), waits the specified Head Settling Time (defined in the Specify command), then begins reading ID fields from the disk. When the four bytes (T, H, R, N) loaded during the command match the four bytes of the ID field from the disk, the DDFDC transfers data from the data bus to the disk Data field.

After writing data into the current sector, the DDFDC increments the sector number (R) by one, and writes into the Data field in the next sector. The DDFDC continues this multi-sector write operation until the last byte is written to sector R when R = EOT. ST0 bits 7 and 6 are set to 0 and 1, respectively, and ST1 bit 7 (EN) is set to a 1.

The command can also be terminated by a high on Terminal Count (TC). If TC is sent to the DDFDC while writing into the current sector, then the remainder of the Data field is filled with 00 (zeros). In this case, ST0 bits 7 and 6 are set to 0 and the command is terminated.

The DDFDC reads the ID field of each sector and checks the CRC bytes. If the DDFDC detects a read error (incorrect CRC) in one of the ID fields, it terminates the Write Data command, sets the DE flag in ST1 to a 1, and sets bits 7 and 6 in ST0 to 0 and 1, respectively.

The Write Data command operates in much the same manner as the Read Data command. Refer to the Read Data command for the handling of the following items:

- Transfer Capacity
- End of Track (EN) flag
- No Data (ND) flag
- Head Unload Time (HUT) interval
- ID information when the processor terminates command (see Table 4)
- Definition of Data Length (DTL) when N = 0 and when N ≠ 0

In the Write Data mode, data transfers from the data bus to the DDFDC must occur within 27 μs in the FM mode, and within 13 μs in the MFM mode. If the time interval between data transfers is longer than this, then the DDFDC terminates the Write Data command, sets the Over Run (OR) flag in ST1 to a 1, and sets bits 7 and 6 in ST0 to 0 and 1, respectively.

Command Phase:

R/W	BYTE	7	6	5	4	3	2	1	0
W	1	MT	MF	0	0	0	1	0	1
	2	X	X	X	X	X	HD	US1	US0
	3	Track Number (T)							
	4	Head Number (H)							
	5	Sector Number (R)							
	6	Number of Data Bytes per Sector (N)							
	7	End of Track (EOT)							
	8	Gap Length (GPL)							
	9	Data Length (DTL)							

Result Phase:

R	1	Status Register 0 (ST0)
	2	Status Register 1 (ST1)
	3	Status Register 2 (ST2)
	4	Track Number (T)
	5	Head Number (H)
	6	Sector Number (R)
	7	Number of Data Bytes per Sector (N)

WRITE DELETED DATA

The Write Deleted Data command is the same as the Write Data command except a Deleted Data Address Mark is written at the beginning of the Data field instead of the normal Data Address Mark.

Command Phase:

R/W	BYTE	7	6	5	4	3	2	1	0
W	1	MT	MF	0	0	1	0	0	1
	2	X	X	X	X	X	HD	US1	US0
	3	Track Number (T)							
	4	Head Number (H)							
	5	Sector Number (R)							
	6	Number of Data Bytes per Sector (N)							
	7	End of Track (EOT)							
	8	Gap Length (GPL)							
	9	Data Length (DTL)							

Result Phase:

R	1	Status Register 0 (ST0)
	2	Status Register 1 (ST1)
	3	Status Register 2 (ST2)
	4	Track Number (T)
	5	Head Number (H)
	6	Sector Number (R)
	7	Number of Data Bytes per Sector(N)

READ DELETED DATA

The Read Deleted Data command is the same as the Read Data command except that if SK = 0 when the DDFDC detects a **Data Address Mark** at the beginning of a Data field, it reads all the data in the sector and sets the CM flag in ST2 to a 1, and then terminates the command. If SK = 1, then the DDFDC skips the sector with the **Data Address Mark** and reads the next sector.

Command Phase:

R/W	BYTE	7	6	5	4	3	2	1	0
W	1	MT	MF	SK	0	1	1	0	0
	2	X	X	X	X	X	HD	US1	US0
	3	Track Number (T)							
	4	Head Number (H)							
	5	Sector Number (R)							
	6	Number of Data Bytes per Sector (N)							
	7	End of Track (EOT)							
	8	Gap Length (GPL)							
	9	Data Length (DTL)							

Result Phase:

R	1	Status Register 0 (ST0)
	2	Status Register 1 (ST1)
	3	Status Register 2 (ST2)
	4	Track Number (T)
	5	Head Number (H)
	6	Sector Number (R)
	7	Number of Data Bytes per Sector (N)

READ A TRACK

The Read a Track command is similar to the Read Data command except that this is a continuous read operation where all Data fields from each of the sectors on a track are read and transferred to the data bus. Immediately after encountering the Index Hole, the DDFDC starts reading the Data fields as continuous blocks of data. This command terminates when the number of sectors read is equal to EOT. Multi-track operations are not allowed with this command.

If the DDFDC finds an error in the ID or Data CRC check bytes, it continues to read data from the track. The DDFDC compares the ID information read from each sector with the value stored in the IDR, and sets the ND flag in ST1 to a 1 if there is no match.

If the DDFDC does not find an ID Address Mark on the disk after it encounters the Index Hole for the second time it terminates the command, sets the Missing Address Mark (MA) flag in ST1 to a 1, and sets bits 7 and 6 of ST0 to 0 and 1, respectively.

Command Phase:

R/W	BYTE	7	6	5	4	3	2	1	0
W	1	0	MF	SK	0	0	0	1	0
	2	X	X	X	X	X	HD	US1	US0
	3	Track Number (T)							
	4	Head Number (H)							
	5	Sector Number (R)							
	6	Number of Data Bytes per Sector (N)							
	7	End of Track (EOT)							
	8	Gap Length (GPL)							
	9	Data Length (DTL)							

Result Phase:

R	1	Status Register 0 (ST0)
	2	Status Register 1 (ST1)
	3	Status Register 2 (ST2)
	4	Track Number (T)
	5	Head Number (H)
	6	Sector Number (R)
	7	Number of Data Bytes per Sector (N)

READ ID

The two-byte Read ID command returns the present position of the read/write head. The DDFDC obtains the value from the first ID field it is able to read, sets bits 7 and 6 in ST0 to 0 and terminates the command.

If no proper ID Address Mark is found on the disk before the Index Hole is encountered for the second time then the Missing Address Mark (MA) flag in ST1 is set to a 1, and if no data is found then the ND flag in ST1 is also set to a 1. Bits 7 and 6 in ST0 are set to 0 and 1, respectively and the command is terminated.

During this command there is no data transfer between DDFDC and the data bus except during the result phase.

Command Phase:

R/W	BYTE	7	6	5	4	3	2	1	0
W	1	0	MF	0	0	1	0	1	0
	2	X	X	X	X	X	HD	US1	US0

Result Phase:

R	1	Status Register 0 (ST0)
	2	Status Register 1 (ST1)
	3	Status Register 2 (ST2)
	4	Track Number (T)
	5	Head Number (H)
	6	Sector Number (R)
	7	Number of Data Bytes per Sector (N)

FORMAT A TRACK

The six-byte Format a Track command formats an entire track. After the Index Hole is detected, data is written on the disk: Gaps, Address Marks, ID fields and Data fields; all are recorded in either the double-density IBM System 34 format (MF = 1) or the single-density IBM 3740 format (MF = 0). The particular format written is also controlled by the values of Number of Bytes/Sector (N), Sectors/Track (ST), Gap Length (GPL) and Data Pattern (D) which are supplied by the processor during the command phase. The Data field is filled with the data pattern stored in D.

The ID field for each sector is supplied by the processor in response to four data requests per sector issued by the DDFDC. The type of data request depends upon the Non-DMA flag (ND) in the Specify command. In the DMA mode (ND = 0), the DDFDC asserts the DMA Request (DRQ) output four times per sector. In the Non-DMA mode (ND = 1), the DDFDC asserts Interrupt Request (INT) output four times per sector.

The processor must write one data byte in response to each request, sending (in the consecutive order) the Track Number (T), Head Number (H), Sector Number (R) and Number of Bytes/Sector (N). This allows the disk to be formatted with non-sequential sector numbers, if desired.

The processor must send new values for T, H, R, and N to the DDFDC for each sector on the track. For sequential formatting R is incremented by one after each sector is formatted, thus, R contains the total numbers of sectors formatted when it is read during the result phase. This incrementing and formatting continues for the whole track until the DDFDC, upon encountering the Index Hole for the second time, terminates the command and sets bits 7 and 6 in ST0 to 0.

If the Fault (FLT) signal is high from the FDD at the end of a write operation, the DDFDC sets the Equipment Check (EC) flag in ST0 to a 1, sets bits 7 and 6 of ST0 to 0 and 1, respectively, and terminates the command. Also, a low (RDY) signal at the beginning of a command execution phase causes bits 7 and 6 of ST0 to be set to 0 and 1, respectively.

Table 5 shows the relationship between N, ST, and GPL for various disk and sector sizes.

Command Phase:

R/W	BYTE	7	6	5	4	3	2	1	0
W	1	0	MF	0	0	1	1	0	1
	2	X	X	X	X	X	HD	US1	US0
	3	Number of Bytes per Sector (N)							
	4	Sectors per Track (ST)							
	5	Gap Length (GPL)							
	6	Data Pattern (D)							

Table 5. Standard Floppy Disk Sector Size Relationship

Disk Size	Mode	Sector Size Bytes/Sector	No. of Data Bytes/Sector (N)	No. of Sectors/Track (ST)	Gap Length (GPL)[4]		Remarks
					Read/Write Command[1]	Format Command[2]	
8″	FM	128	00	1A	07	1B	
		256	01	0F	0E	2A	
		512	02	08	1B	3A	
		1024	03	04	47	8A	
		2048	04	02	C8	FF-	
		4096	05	01	C8	FF	
	MFM[3]	256	01	1A	0E	36	
		512	02	0F	1B	54	
		1024	03	08	35	74	
		2048	04	04	99	FF	
		4096	05	02	C8	FF	
		8192	06	01	C8	FF	
5¼″	FM	128	00	12	07	09	
		128	00	10	10	19	
		256	01	08	18	30	
		512	02	04	46	87	
		1024	03	02	C8	FF	
		2048	04	01	C8	FF	
	MFM[3]	256	01	12	0A	0C	
		256	01	10	20	32	
		512	02	08	2A	50	
		1024	03	04	80	F0	
		2048	04	02	C8	FF	
		4096	05	01	C8	FF	
3½″	FM	128	00	0F	07	1B	
		256	01	09	0E	2A	
		512	02	05	1B	3A	
	MFM[3]	256	01	0F	0E	36	
		512	02	09	1B	54	
		1024	03	05	35	74	

Notes:
1. Suggested values of GPL in Read or Write commands to avoid overlapping between Data field and ID field of contiguous sections.
2. Suggested values of GPL in Format a Track command.
3. In MFM mode the DDFDC cannot perform a read/write/format operation with 128 bytes/sector (N = 00).
4. Values of ST and GPL are in hexadecimal.

Result Phase:

R	1	Status Register 0 (ST0)
	2	Status Register 1 (ST1)
	3	Status Register 2 (ST2)
	4	Track Number (T)*
	5	Head Number (H)*
	6	Sector Number (R)*
	7	Number of Data Bytes per Sector (N)*

* The ID information has no meaning in this command.

SCAN COMMANDS

The scan commands compare data read from the disk to data supplied from the data bus. The DDFDC compares the data, and looks for a sector of data which meets the conditions of $D_{FDD} = D_{BUS}$, $D_{FDD} \leq D_{BUS}$, or $D_{FDD} \geq D_{BUS}$ (D = the data pattern in hexadecimal). A magnitude comparison is performed (FF = largest number, 00 = smallest number). The hexadecimal byte of FF either from the bus or from FDD can be used as a mask byte because it always meets the condition of the compare. After a whole sector of data is compared, if the conditions are not met, the sector number is incremented (R + STP → R), and the scan operation is continued. The scan operation continues until one of the following events occur: the conditions for scan are met (equal, low or equal, or high or equal), the last sector on the track is reached (EOT), or TC is received.

If conditions for scan are met, the DDFDC sets the Scan Hit (SH) flag in ST2 to a 1, and terminates the command. If the conditions for scan are not met between the starting sector (as specified by R) and the last sector on the track (EOT), then the DDFDC sets the Scan Not Satisfied (SN) flag in ST2 to a 1, and terminates the command. The receipt of TC from the processor or DMA controller during the scan operation will cause the DDFDC to complete the comparison of the particular byte which is in process, and then to terminate the command. Table 6 shows the status of bits SH and SN under various conditions of scan.

Table 6. Scan Status Codes

Command	Status Register 2		Comments
	Bit 2 = SN	Bit 3 = SH	
Scan Equal	0	1	$D_{FDD} = D_{BUS}$
	1	0	$D_{FDD} \neq D_{BUS}$
Scan Low or Equal	0	1	$D_{FDD} = D_{BUS}$
	0	0	$D_{FDD} < D_{BUS}$
	1	0	$D_{FDD} > D_{BUS}$
Scan High or Equal	0	1	$D_{FDD} = D_{BUS}$
	0	0	$D_{FDD} > D_{BUS}$
	1	0	$D_{FDD} < D_{BUS}$

If SK = 0 and the DDFDC encounters a Deleted Data Address Mark on one of the sectors, it regards that sector as the last sector of the track, sets the Control Mark (CM) bit in ST2 to a 1 and terminates the command. If SK = 1, the DDFDC skips the sector with the Deleted Data Address Mark, sets the CM flag to a 1 in order to show that a Deleted Sector has been encountered, and reads the next sector.

When either the STP sectors are read (contiguous sectors = 01, or alternate sectors = 02) or MT (Multi-Track) is set, **the last sector on the track must be read.** For example, if STP = 02, MT = 0, the sectors are numbered sequentially 1 through 26, and the scan command starts reading at sector 21. Sectors 21, 23, and 25 are read, then the next sector (26) is skipped and the Index Hole is encountered before the EOT value of 26 can be read. This results in an abnormal termination of the command. If the EOT had been set at 25 or the scanning started at sector 20, then the scan command would be completed in a normal manner.

During a scan command data is supplied from the data bus for comparison against the data read from the disk. In order to avoid having the Over Run (OR) flag set in ST1, data must be available from the data bus in less than 27 μs (FM mode) or 13 μs (MFM mode). If an OR occurs, the DDFDC terminates the command and sets bits 7 and 6 of ST0 to 0 and 1, respectively.

The following tables specify the command bytes and describe the result bytes for the three scan commands.

SCAN EQUAL

Command Phase:

R/W	BYTE	7	6	5	4	3	2	1	0
W	1	MT	MF	SK	1	0	0	0	1
	2	X	X	X	X	X	HD	US1	US0
	3	Track Number (T)							
	4	Head Number (H)							
	5	Sector Number (R)							
	6	Number of Data Bytes per Sector (N)							
	7	End of Track (EOT)							
	8	Gap Length (GPL)							
	9	Sector Test Process (STP)							

Result Phase:

R	1	Status Register 0 (ST0)
	2	Status Register 1 (ST1)
	3	Status Register 2 (ST2)
	4	Track Number (T)
	5	Head Number (H)
	6	Sector Number (R)
	7	Number of Data Bytes per Sector (N)

SCAN LOW OR EQUAL

Command Phase:

R/W	BYTE	7	6	5	4	3	2	1	0
W	1	MT	MF	SK	1	1	1	0	1
	2	X	X	X	X	X	HD	US1	US0
	3	Track Number (T)							
	4	Head Number (H)							
	5	Sector Number (R)							
	6	Number of Data Bytes per Sector (N)							
	7	End of Track (EOT)							
	8	Gap Length (GPL)							
	9	Sector Test Process (STP)							

Result Phase:

R	1	Status Register 0 (ST0)
	2	Status Register 1 (ST1)
	3	Status Register 2 (ST2)
	4	Track Number (T)
	5	Head Number (H)
	6	Sector Number (R)
	7	Number of Data Bytes per Sector (N)

SCAN HIGH OR EQUAL

Command Phase:

R/W	BYTE	7	6	5	4	3	2	1	0
W	1	MT	MF	SK	1	1	1	0	1
	2	X	X	X	X	X	HD	US1	US0
	3	Track Number (T)							
	4	Head Number (H)							
	5	Sector Number (R)							
	6	Number of Data Bytes per Sector (N)							
	7	End of Track (EOT)							
	8	Gap Length (GPL)							
	9	Sector Test Process (STP)							

Result Phase:

R	1	Status Register 0 (ST0)
	2	Status Register 1 (ST1)
	3	Status Register 2 (ST2)
	4	Track Number (T)
	5	Head Number (H)
	6	Sector Number (R)
	7	Number of Data Bytes per Sector (N)

SEEK

The three-byte Seek command steps the FDD read/write head from track to track. The DDFDC has four independent Present Track Registers for each drive. They are cleared only by the Recalibrate command. The DDFDC compares the Present Track Number (PTN) which is the current head position with the New Track Number (NTN), and if there is a difference, performs the following operation:

If PTN < NTN: Sets the direction output (LCT/DIR) high and issues step pulses (FR/STP) to the FDD to cause the read/write head to step in.

If PTN > NTN: Sets the direction output (LCT/DIR) low and issues step pulses to the FDD to cause the read/write head to step out.

The rate at which step pulses are issued is controlled by the Step Rate Time (SRT) in the Specify command. After each step pulse is issued, NTN is compared against PTN. When NTN = PTN, then the Seek End (SE) flag in ST0 is set to a 1, bits 7 and 6 in ST0 are set to 0, and the command is terminated. At this point DDFDC asserts INT.

The FDD Busy flag (bit 0-3) in the Main Status Register (MSR) corresponding to the FDD performing the Seek operation is set to a 1.

After command termination, all FDD Busy bits set are cleared by the Sense Interrupt Status command.

During the command phase of the Seek operation the DDFDC sets the Controller Busy (CB) flag in the MSR to 1; but during the execution phase the CB flag is set to 0 to indicate DDFDC non-busy. While the DDFDC is in the non-busy state, another Seek command may be issued, and in this manner parallel seek operations may be performed on all drives at once.

No command other than Seek will be accepted while the DDFDC is sending step pulses to any FDD. If a different command type is attempted, the DDFDC will set bits 7 and 6 in ST0 to a 1 and 0, respectively, to indicate an invalid command.

If the FDD is in a not ready state at the beginning of the command execution phase or during the seek operation, then the DDFDC sets the Not Ready (NR) flag in ST0 to a 1, sets ST0 bits 7 and 6 to 0 and 1, respectively, and terminates the command.

If the time to write the three bytes of the Seek command exceeds 150 μs, the time between the first two step pulses may be shorter than the Step Rate Time (SRT) defined by the Specify command by as much as 1 ms.

Command Phase:

R/W	BYTE	7	6	5	4	3	2	1	0
W	1	0	0	0	0	1	1	1	1
	2	X	X	X	X	X	0	US1	US0
	3	New Track Number (NTN)							

Result Phase: None.

RECALIBRATE

This two-byte command retracts the FDD read/write head to the Track 0 position. The DDFDC clears the contents of the PTN counters, and checks the status of the Track 0 signal from the FDD. As long as the Track 0 signal (TRK0) is low, the direction signal (LCT/DIR) output remains low and step pulses are issued on FR/STP. When TRK0 goes high the DDFDC sets the Seek End (SE) flag in ST0 to a 1 and terminates the command. If the TRK0 is still low after 256 step pulses have been issued, the DDFDC sets Seek End (SE) and Equipment Check (EC) flags in ST0 to 1s, sets bits 7 and 6 of ST0 to 0 and 1, respectively, and terminates the command.

The ability to do overlap Recalibrate commands to multiple FDDs and the loss of the RDY signal, as described in the Seek command, also applies to the Recalibrate command.

Command Phase:

R/W	BYTE	7	6	5	4	3	2	1	0
W	1	0	0	0	0	0	1	1	1
	2	X	X	X	X	X	0	US1	US0

Result Phase: None.

SENSE INTERRUPT STATUS

Interrupt Request (INT) is asserted by the DDFDC when any of the following conditions occur:

1. Upon entering the result phase of:
   a. Read Data command
   b. Read a Track command
   c. Read ID command
   d. Read Deleted Data command
   e. Write Data command
   f. Format a Track command
   g. Write Deleted Data command
   h. Scan commands
2. Ready (RDY) line from the FDD changes state
3. Seek or Recalibrate command termination
4. During execution phase in the Non-DMA mode

INT caused by reasons 1 and 4 above occur during normal command operations and are easily discernible by the processor. During an execution phase in Non-DMA mode, bit 5 in the MSR is set to 1. Upon entering result phase this bit is set to 0. Reasons 1 and 4 do not require the Sense Interrupt Status command. The interrupt is cleared by reading or writing data to DDFDC. Interrupts caused by reasons 2 and 3 are identified with the aid of the Sense Interrupt Status command. This command resets INT and sets/resets bits 5, 6, and 7 of ST0 to identify the cause of the interrupt. Table 7 defines the seek and interrupt codes.

The Sense Interrupt Status command is used in conjunction with the Seek and Recalibrate commands which have no result phase. When the disk drive has reached the desired head position the DDFDC asserts interrupt output. The host CPU must then issue a Sense Interrupt Status command to determine the actual cause of the interrupt, which could be Seek End or a change in ready status from one of the drives (see example in Figure 3).

Issuing a Sense Interrupt Status command without an interrupt pending is treated as an invalid command.

Table 7. ST0 Seek and Interrupt Code Definition for Sense Interrupt Status

Status Register 0 (ST0) Bits			
Interrupt Code (IC)		Seek End (SE)	Cause
7	6	5	
1	1	0	RDY line changed state, either polarity
0	0	1	Normal termination of Seek or Recalibrate command
0	1	1	Abnormal termination of Seek or Recalibrate command

Command Phase:

R/W	BYTE	7	6	5	4	3	2	1	0
W	1	0	0	0	0	1	0	0	0

Result Phase:

R	1	Status Register 0 (ST0)
	2	Present Track Number (PTN)

SPECIFY

The three-byte Specify command sets the initial values for each of the three internal timers. The Head Unload Time (HUT) defines the time from the end of the execution phase of one of the read/write commands to the head unload state. This timer is programmable from 16 to 240 ms in increments of 16 ms (1 = 16 ms, 2 = 32 ms, . . . F = 240 ms).

The Step Rate Time (SRT) defines the time interval between adjacent step pulses. This timer is programmable from 1 to 16 ms in increments of 1 ms (F = 1 ms, E = 2 ms, D = 3 ms, . . . 0 = 16 ms.)

The Head Load Time (HLT) defines the time between the Head Load (HDL) signal going high and the start of the read/write operation. This timer is programmable from 2 to 254 ms in increments of 2 ms (01 = 2 ms, 02 = 4 ms, 03 = 6 ms, . . . 7F = 254 ms).

The time intervals are a direct function of the clock (CLK on pin 19). Times indicated above are for an 8 MHz clock. If the clock is reduced to 4 MHz (mini-floppy application) then all time intervals are increased by a factor of two.

The choice of DMA or Non-DMA operation is made by the Non-DMA mode (ND) bit. When this bit = 1 the Non-DMA mode is selected, and when ND = 0 the DMA mode is selected.

Command Phase:

R/W	BYTE	7	6	5	4	3	2	1	0
W	1	0	0	0	0	0	0	1	1
	2	SRT				HUT			
	3	HLT							ND

SRT — Step Rate Time
HUT — Head Unload Time
HLT — Head Load Time
ND — Non-DMA mode

Result Phase: None.

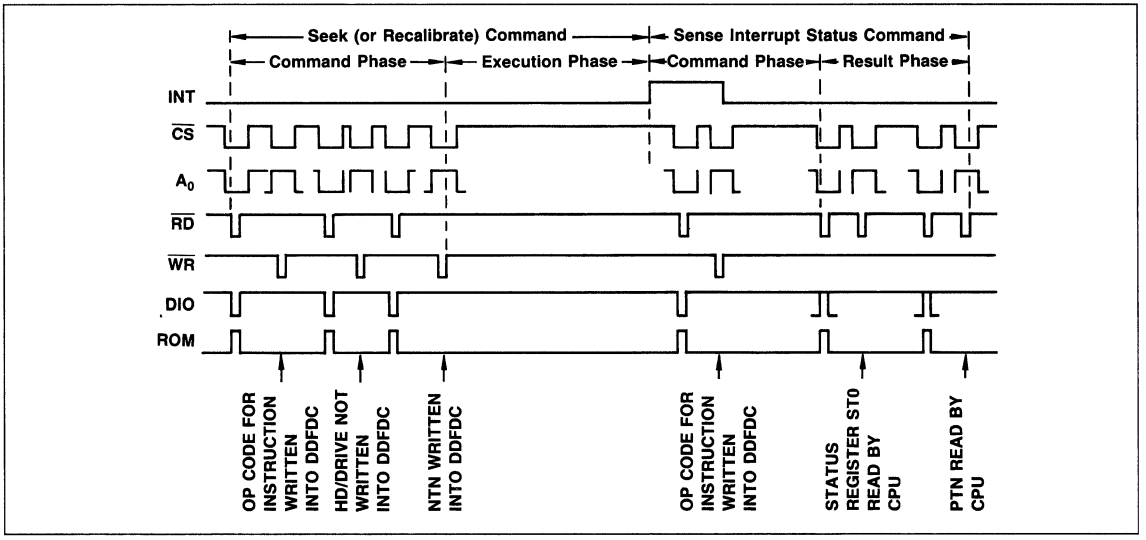


Figure 3. Sense Interrupt Status

SENSE DRIVE STATUS

This two-byte command obtains and reports the status of the FDDs. Status Register 3 (ST3) is returned in the result phase and contains the drive status.

Command Phase:

R/W	BYTE	7	6	5	4	3	2	1	0
W	1	0	0	0	0	0	1	0	0
	2	X	X	X	X	X	HD	US1	US0

Result Phase:

R	1	Status Register 3 (ST3)

INVALID COMMAND

If an invalid command (i.e., a command not previously defined) is received by the DDFDC, then the DDFDC terminates the command after setting bits 7 and 6 of ST0 to 1 and 0, respectively. The DDFDC does not generate an interrupt during this condition. Bits 6 and 7 (DIO and RQM) in the MSR are both set to a 1 indicating to the processor that the DDFDC is in the result phase and that ST0 must be read. A hex 80 in ST0 indicates that an invalid command was received.

A Sense Interrupt Status command must be sent after a Seek or Recalibrate interrupt, otherwise the DDFDC considers the next command to be an invalid command.

In some applications the user may wish to use this command as a No-Op command, to place the DDFDC in a standby or no operation state.

Command Phase:

R/W	BYTE	7	6	5	4	3	2	1	0
W	1	Invalid Codes							

Result Phase:

R	1	Status Register 0 (ST0) = 80

PROCESSOR INTERFACE

During the command or result phases, the Main Status Register (MSR) must be read by the processor before each byte of information is transferred to, or from, the DDFDC Data Register. After each byte of data is written to, or read from, the Data Register, the processor should wait 12 μs before reading the MSR. Bits 6 and 7 in the MSR must be a 0 and 1, respectively, before each command byte can be written to the DDFDC. During the result phase, bits 6 and 7 of the MSR must both be 1s prior to reading each byte from the Data Register onto the data bus. Note that this status reading of bits 6 and 7 of the MSR before each byte transfer to and from the DDFDC is required in only the command and result phases and not during the execution phase.

During the result phase all bytes shown in the result phase must be read by the processor. The Read Data command, for example, has seven bytes of data in the result phase. All seven bytes must be read to successfully complete the Read Data command. The DDFDC will not accept a new command until all seven bytes have been read. Other commands may require fewer bytes to be read during the result phase.

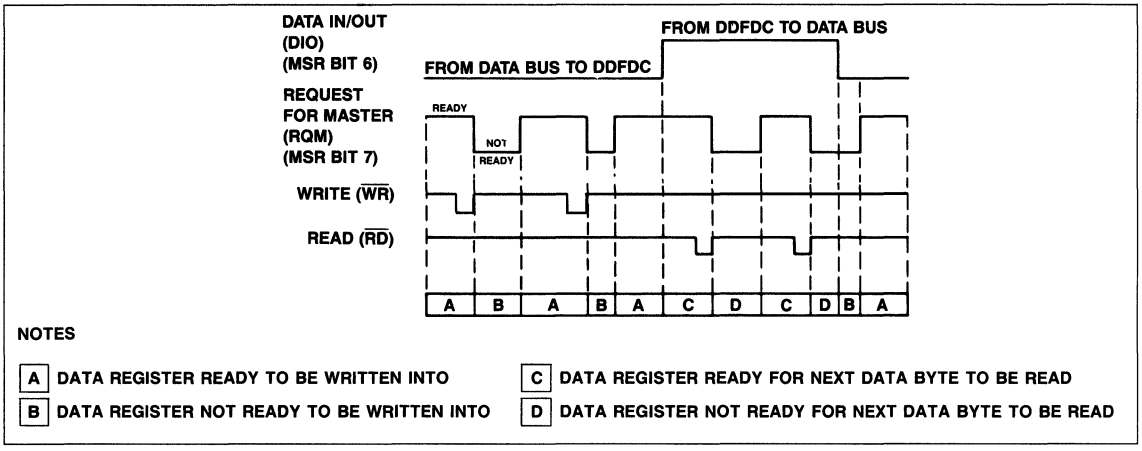


Figure 4. DDFDC and System Data Transfer Timing

INTERRUPT REQUEST MODE

During the execution phase, the MSR need not be read. The receipt of each data byte from the FDD is indicated by INT high on pin 18. When the DDFDC is in Non-DMA mode, INT is asserted during the execution phase. When the DDFDC is in the DMA mode, INT is asserted at the result phase. The INT signal is reset by a read ($\overline{RD}$ low) or write ($\overline{WR}$ low) of data to the DDFDC. A further explanation of the INT signal is described in the Sense Interrupt Status command on page 16. If the system cannot handle interrupts fast enough (within 13 μs for MFM mode or 27 μs for FM mode), it should poll bit 7 (RQM) in the MSR. In this case, RQM in the MSR functions as an Interrupt Request (INT). If the RQM bit is not set, the Over Run (OR) flag in ST1 will be set to a 1 and bits 7 and 6 of ST0 will be set to a 0 and 1, respectively.

DMA MODE

When the DDFDC is in the DMA mode (ND = 0 in the third command byte of the Specify command), DRQ (DMA Request) is asserted during the execution phase (rather than INT) to request the transfer of a data byte between the data bus and the DDFDC.

During a read command, the DDFDC asserts DRQ as each byte of data is available to be read. The DMA controller responds to this request with $\overline{DACK}$ low (DMA Acknowledge) and $\overline{RD}$ low (read). When $\overline{DACK}$ goes low the DMA Request is reset (DRQ low). After the execution phase has been completed (TC high or the EOT sector is read), INT is asserted to indicate the beginning of the result phase. When the first byte of data is read during the result phase, INT is reset low.

During a write command, the DDFDC asserts DRQ as each byte of data is required. The DMA controller responds to this request with $\overline{DACK}$ (DMA Acknowledge) and $\overline{WR}$ low (write). When DACK goes low the DMA Request is reset (DRQ low). After the execution phase has been completed (TC high or the EOT sector is written), INT is asserted. This signals the beginning of the result phase. When the first byte of data is read during the result phase, the INT is reset low.

FDD POLLING

After the Specify command has been received by the DDFDC, the Unit Select lines (US0 and US1) begin the polling mode. Between commands (and between step pulses in the Seek Command) the DDFDC polls all the FDD's looking for a change in the RDY line from any of the drives. If the RDY line changes state (usually due to the door opening or closing) then the DDFDC asserts INT. When Status Register 0 (ST0) is read (after Sense Interrupt Status command is issued), Not Ready (NR = 1) will be indicated. The polling of the RDY line by the DDFDC occurs continuously between commands, thus notifying the processor which drives are on- or off-line. Each drive is polled every 1.024 ms except during read/write commands.

R6765 (FM MODE)

FIELD	GAP 4a	SYNC	IAM	GAP 1	SYNC	IDAM	CYL	HD	SEC	NO	CRC	GAP 2	SYNC	DATA AM	DATA		GAP 3	GAP 4b
NO. OF BYTES	40×	6×		26×	6×							11×	6×		①	CRC	①	
DATA	FF	00	FC	FF	00	FE						FF	00	FB OR F8				

INDEX — REPEAT N TIMES

R6265 (FM MODE)

FIELD	GAP 1	SYNC	IDAM	CYL	HD	SEC	NO	CRC	GAP 2	SYNC	DATA AM	DATA		GAP 3	GAP 4
NO OF BYTES	16×	6×							11×	6×		①	CRC	①	
DATA	FF	00	FC						FF	00	FB OR F8				

INDEX — REPEAT N TIMES

R6765 (MFM MODE)

GAP 4a	SYNC	IAM		GAP 1	SYNC	IDAM		CYL	HD	SEC	NO	CRC	GAP 2	SYNC	DATA AM		DATA		GAP 3	GAP 4b
80×	12×	3×		50×	12×	3×							22x	12×	3×	FB	①	CRC	①	
4E	00	C2	FC	4E	00	A1	FE						4E	00	A1	F8				

INDEX — REPEAT N TIMES

R6265 (MFM MODE)

FIELD	GAP 1	SYNC	IDAM		CYL	HD	SEC	NO	CRC	GAP 2	SYNC	DATA AM		DATA		GAP 3	GAP 4
NO OF BYTES	32×	12×	3×							22x	12×	3×	FB	①	CRC	①	
DATA	4E	00	A1	FE						4E	00	A1	F8				

INDEX — REPEAT N TIMES

Figure 5. DDFDC Formats

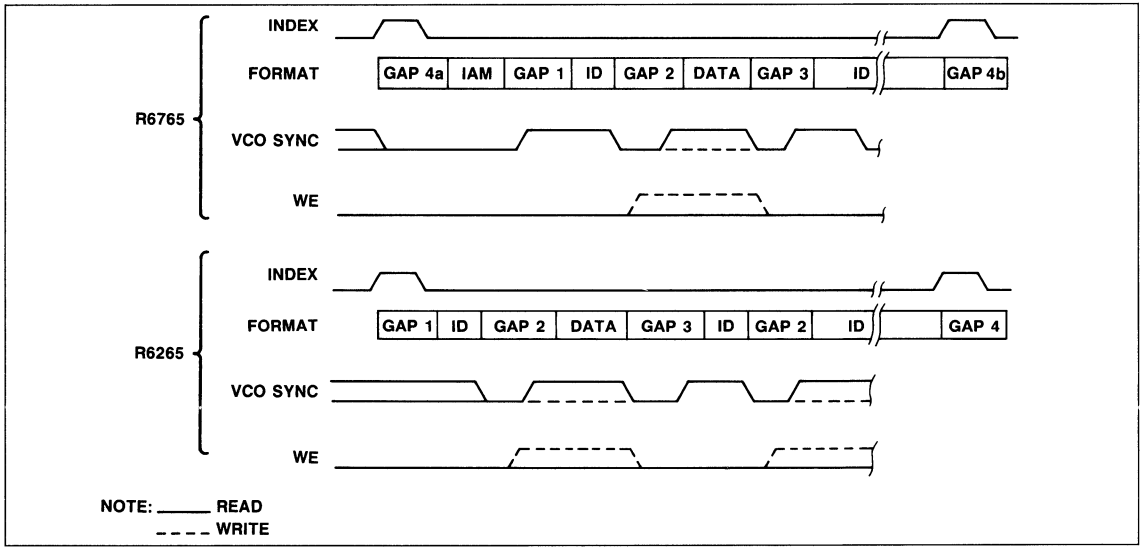


Figure 6. DDFDC Formats

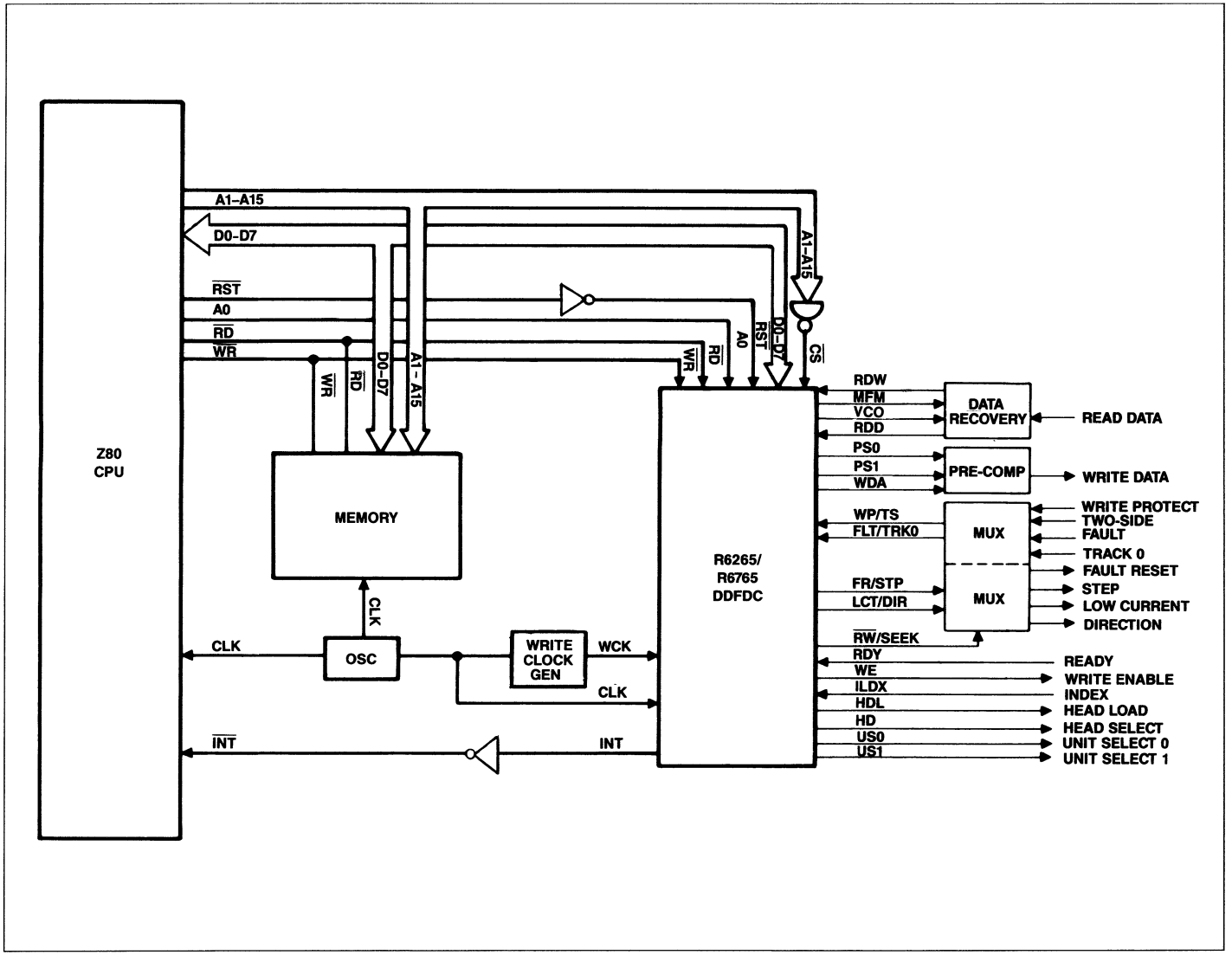


Figure 7. R6265/R6765 DDFDC Interface to Z 80

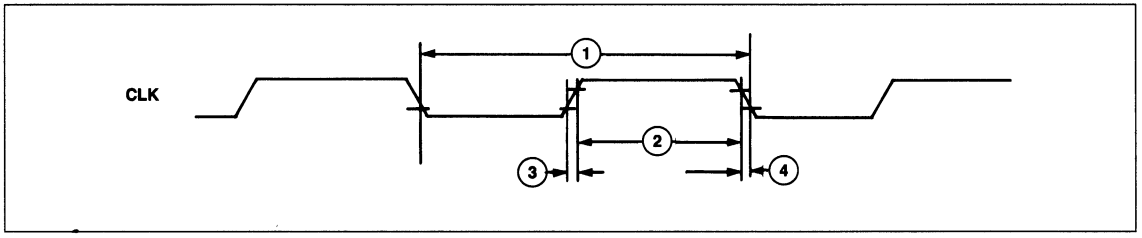


Figure 8. Clock Timing

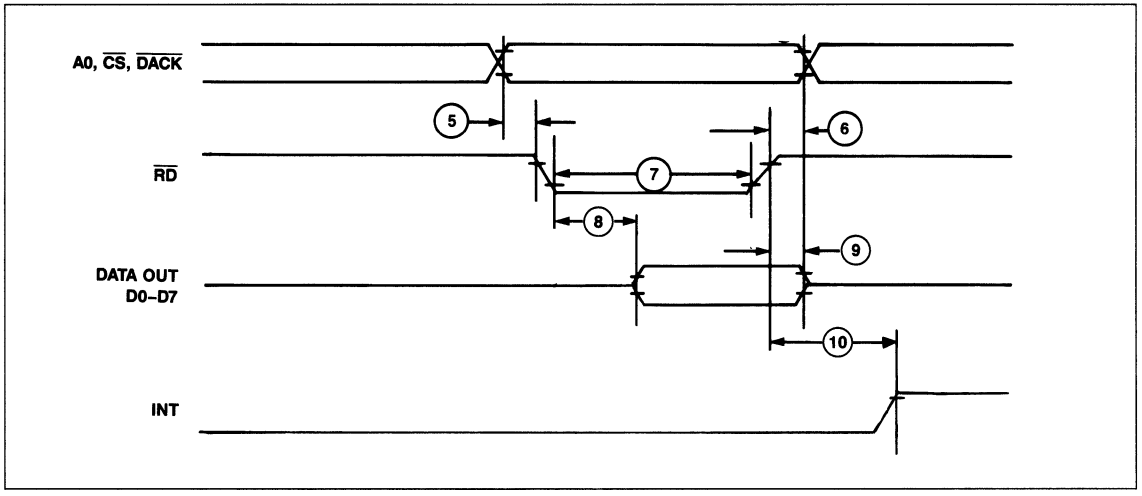


Figure 9. Read Cycle Timing

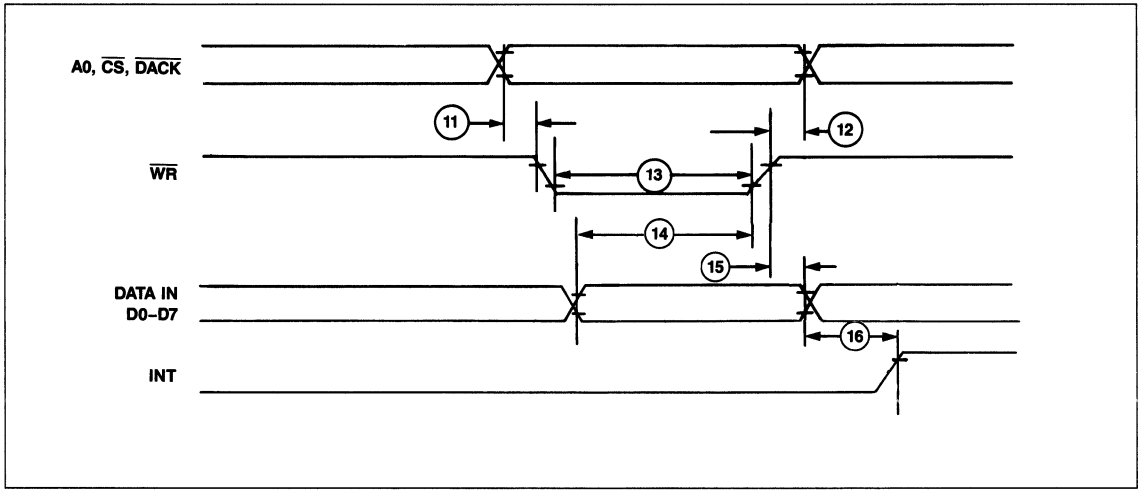


Figure 10. Write Cycle Timing

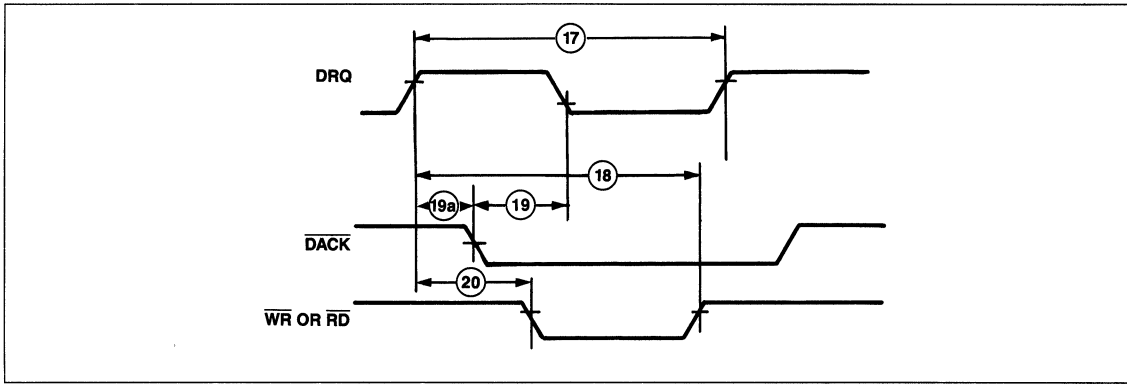


Figure 11. DMA Operation Timing

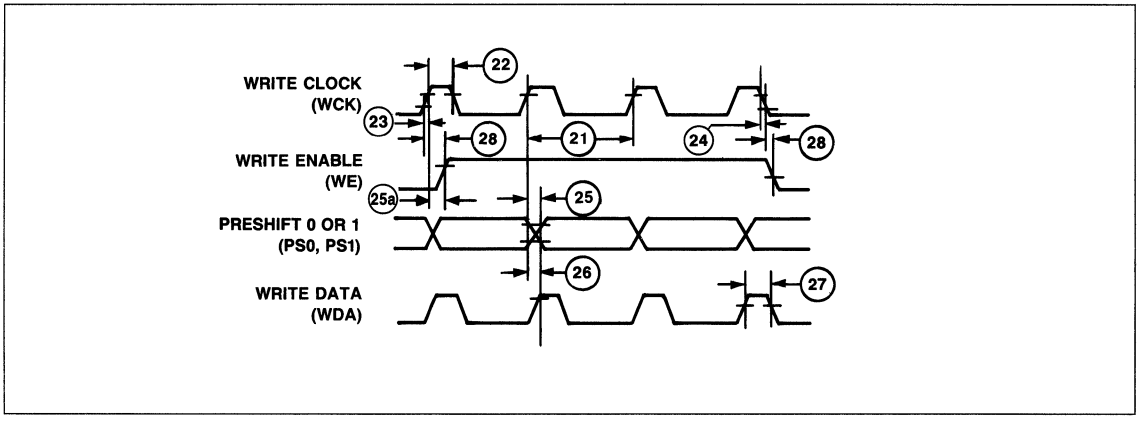


Figure 12. FDD Write Operation Timing

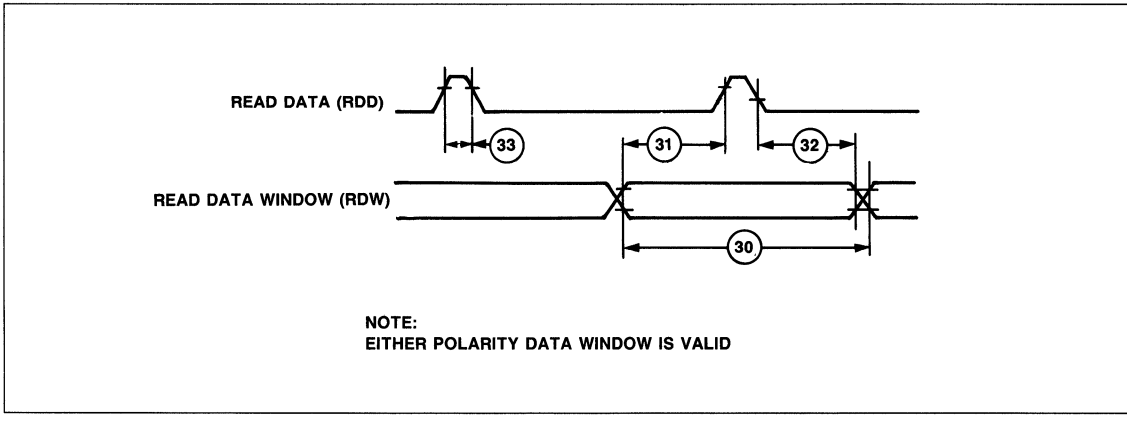


Figure 13. FDD Read Operation Timing

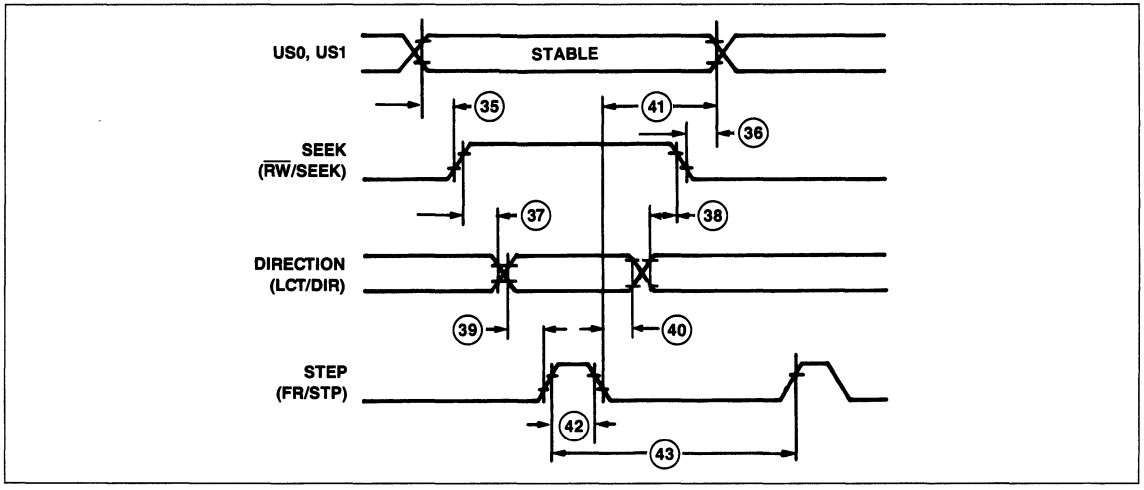


Figure 14. Seek Operation Timing

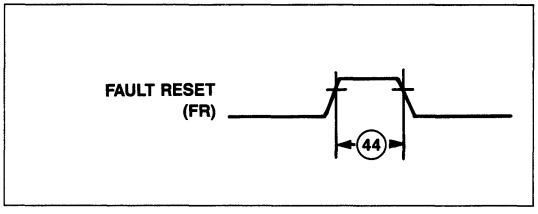


Figure 15. Fault Reset Timing

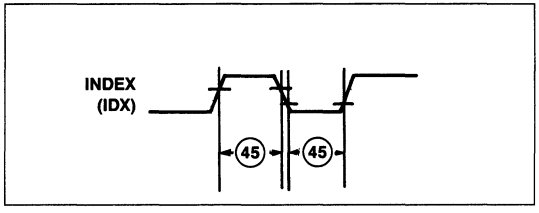


Figure 16. Index Timing

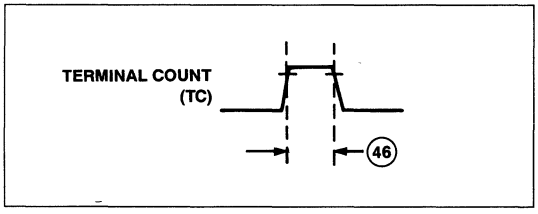


Figure 17. Terminal Count Timing

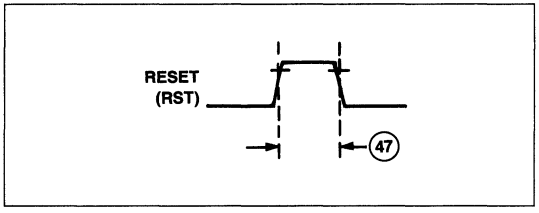
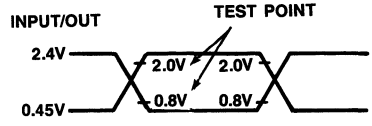
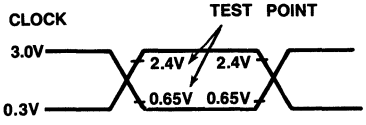


Figure 18. Reset Timing



INPUTS ARE DRIVEN AT 2.4V FOR A LOGIC "1" AND 0.45 V FOR A LOGIC "0." TIMING MEASUREMENTS ARE MADE AT 2.0V FOR A LOGIC "1" AND 0.8V FOR A LOGIC "0."



CLOCKS ARE DRIVEN AT 3.0V FOR A LOGIC "1" AND 0.3V FOR A LOGIC "0." TIMING MEASUREMENTS ARE MADE AT 2.4V FOR A LOGIC "1" AND 0.65V FOR A LOGIC "0."

Figure 19. AC Timing Measurement Conditions

AC CHARACTERISTICS

(V_{CC} = 5.0 Vdc ±5%, V_{SS} = 0 Vdc, T_A = 0°C to 70°C)

Ref. Fig.	No.	Characteristic		Symbol	Alt. Sym.	Min.	Typ.	Max.	Unit	Test Conditions
5	1	Clock Period	(8″ or 3-1/2″ FDD)	t_{CY}	ϕ_{CY}	120	125	500	ns	CLK = 8 MHz
			(5-1/4″ FDD)			—	250	—	ns	CLK = 4 MHz
	2	Clock High		t_{CA}	ϕ_0	40	—	—	ns	CLK = 8 MHz
						40	62.5	—	ns	CLK = 8 MHz
	3	Clock Rise Time		t_{CLCH}	ϕ_r	—	—	20	ns	
	4	Clock Fall Time		t_{CHCL}	ϕ_f	—	—	20	ns	
6	5	A0, $\overline{CS}$, $\overline{DACK}$ Valid to $\overline{RD}$ Low (Setup)		t_{SLRL}	t_{AR}	0	—	—	ns	
	6	$\overline{RD}$ High to A0, $\overline{CS}$, $\overline{DACK}$ Invalid (Hold)		t_{RHSH}	t_{RA}	0	—	—	ns	
	7	$\overline{RD}$ Low Width		t_{RLRH}	t_{RR}	250	—	—	ns	
	8	$\overline{RD}$ Low to Data Valid (Access)		t_{RLDV}	t_{RD}	—	—	200	ns	C_L = 100 pF
	9	$\overline{RD}$ High to Output High Z		t_{RHDZ}	t_{DF}	20	—	100	ns	
	10	$\overline{RD}$ High to INT High		t_{RHIH}	t_{RI}	—	—	500	ns	CLK = 8 MHz
7	11	A0, $\overline{CS}$, $\overline{DACK}$ Valid to $\overline{WR}$ Low (Setup)		t_{SLWL}	t_{AW}	0	—	—	ns	
	12	$\overline{WR}$ High to A0, $\overline{CS}$, $\overline{DACK}$ Invalid (Hold)		t_{WHSH}	t_{WA}	0	—	—	ns	
	13	$\overline{WR}$ Low Width		t_{WLWH}	t_{WW}	250	—	—	ns	
	14	Data Valid to $\overline{WR}$ High (Setup)		t_{DVWH}	t_{DW}	150	—	—	ns	
	15	$\overline{WR}$ High to Data Invalid (Hold)		t_{WHDX}	t_{WD}	5	—	—	ns	
	16	$\overline{WR}$ High to INT High		t_{WHIH}	t_{WI}	—	—	500	ns	
8	17	DRQ Cycle Time		t_{QCY}	t_{MCY}	13	—	—	µs	CLK = 8 MHz
	18	DRQ High to $\overline{RD}$, $\overline{WR}$ High (Response)		t_{QHXH}	t_{MRW}	—	—	12	µs	
	19	$\overline{DACK}$ Low to DRQ Low (Delay)		t_{ALQL}	t_{AM}	—	—	200	ns	
	19a	DRQ High to $\overline{DACK}$ Low (Delay)		t_{QHAL}	t_{MA}	200	—	—	ns	t_{CY} = 125 ns
	20	DRQ High to $\overline{RD}$ Low (Delay)		t_{QHRL}	t_{MR}	800	—	—	ns	CLK = 8 MHz
		DRQ High to $\overline{WR}$ Low (Delay)		t_{QHWL}	t_{MW}	250	—	—	ns	
9	21	WCK Cycle Time	(8″ or 3-1/2″ FDD)	t_{KCY}	t_{CY}	—	2	—	µs	MFM = 0
						—	1	—	µs	MFM = 1
			(5-1/4″ FDD)			—	4	—	µs	MFM = 0
						—	2	—	µs	MFM = 1
	22	WCK High Width		t_{KHKL}	t_0	80	250	350	ns	
	23	WCK Rise Time		t_{KLKH}	t_r	—	—	20	ns	
	24	WCK Fall Time		t_{KHKL}	t_f	—	—	20	ns	
	25	WCK High to PS0, PS1 Valid (Delay)		t_{KHPV}	t_{CP}	20	—	100	ns	
	25a	WCK High to WE High (Delay)		t_{DHEN}	t_{CWE}	20	—	100	ns	
	26	PS0, PS1 Valid to WDA High (Delay)		t_{PVDH}	t_{CD}	20	—	100	ns	
	27	WDA High Width		t_{DHDL}	t_{WDD}	t_{WCH} −50	—	—	ns	
	28	WE High to WCK High or WE Low to WCK Low		t_{EHKH}	t_{WE}	20	—	100	ns	
10	30	RDW Cycle Time	(8″ or 3-1/2″ FDD)	t_{WCY}	t_{WCY}	—	2	—	µs	MFM = 0
						—	1	—	µs	MFM = 1
			(5-1/4″ FDD)			—	4	—	µs	MFM = 0
						—	2	—	µs	MFM = 1
	31	RDW Valid to RDD High (Setup)		t_{WVRH}	t_{WRD}	15	—	—	ns	
	32	RDD Low to RDW Invalid (Hold)		t_{RLWI}	t_{RDW}	15	—	—	ns	
	33	RDD High Width		t_{RHRL}	t_{RDD}	40	—	—	ns	
11	35	US0, US1 Valid to SEEK High (Setup)		t_{UVSH}	t_{US}	12	—	—	µs	CLK = 8 MHz
	36	SEEK Low to US0, US1 Invalid (Hold)		t_{SLUI}	t_{SU}	15	—	—	µs	
	37	SEEK High to DIR Valid (Setup)		t_{SHDV}	t_{SD}	7	—	—	µs	
	38	DIR Invalid to SEEK Low (Hold)		t_{DXSL}	t_{DS}	30	—	—	µs	
	39	DIR Valid to STP High (Setup)		t_{DVTH}	t_{DST}	1	—	—	µs	
	40	STP Low to DIR Invalid (Hold)		t_{TLDX}	t_{STD}	24	—	—	µs	
	41	STP Low to US0, US1 Invalid (Hold)		t_{TLUX}	t_{STU}	5	—	—	µs	
	42	STP High Width		t_{THTL}	t_{STP}	6	7	8	µs	
	43	STP Cycle Time		t_{TCY}	t_{SC}	33[1]	—	note 1	µs	
12	44	FR High Width		t_{FHFL}	t_{FR}	8	—	10	µs	
13	45	IDX High Width		t_{IHIL}	t_{IDX}	10	—	—	t_{CY}	
14	46	TC High Width		t_{THTL}	t_{TC}	1	—	—	t_{CY}	
15	47	RST High Width		t_{RHRL}	t_{RST}	14	—	—	t_{CY}	

1. t_{SC} = 33 µs min. is for different drive units. In the case of the same unit, t_{SC} can range from 1 ms to 16 ms with 8 MHz clock period, and 2 ms to 32 ms with 4 MHz clock, under software control.

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to +7.0	V
Input Voltage	V_{IN}	−0.3 to +7.0	V
Output Voltage	V_{OUT}	−0.3 to +7.0	V
Operating Temperature Range	T_A	0 to +70	C°
Storage Temperature Range	T_{STG}	−55 to +150	C°

***NOTE:** Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in other sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2

OPERATING CONDITIONS

Parameter	Range
V_{CC} Power Supply	5.0V ±5%
Operating Temperature	0°C to 70°C

DC CHARACTERISTICS

(V_{CC} = 5.0 Vdc ±5%, V_{SS} = 0 Vdc, T_A = 0°C to 70°C, unless otherwise noted)

Parameter	Symbol	Min	Max	Unit	Test Conditions
Input Low Voltage	V_{IL}			V	
Logic		−0.5	0.8		
CLK and WCK		−0.5	0.65		
Input High Voltage	V_{IH}			V	
Logic		2.0	V_{CC} + 0.5		
CLK and WCK		2.4	V_{CC} + 0.5		
Output Low Voltage	V_{OL}		0.45	V	V_{CC} = 4.75V, I_{OL} = 2.0 mA
Output High Voltage	V_{OH}	2.4	V_{CC}	V	V_{CC} = 4.75V, I_{OH} = −200 µA
V_{CC} Supply Current	I_{CC}		150	mA	V_{CC} = 4.75V
Input Load Current	I_{IL}		10	µA	V_{IN} = V_{CC}
All Inputs			−10	µA	V_{IN} = 0V
High Level Output Leakage Current	I_{LOH}		10	µA	V_{CC} = 0V to 5.25V, V_{SS} = 0V V_{OUT} = V_{CC}
Low Level Output Leakage Current	I_{LOL}		−10	µA	V_{CC} = 0V to 5.25V, V_{SS} = 0V V_{OUT} = +0.45V
Internal Power Dissipation	P_{INT}	—	1.0	W	T_A = 25°C

CAPACITANCE

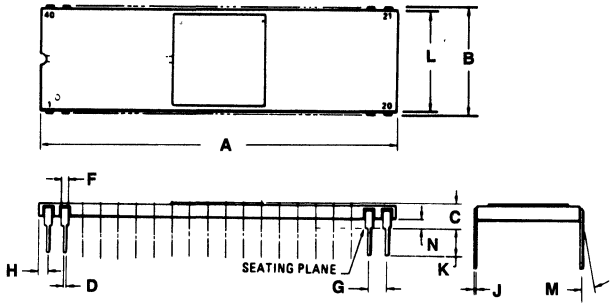
(T_A = 25°C; f_c = 1 MHz; V_{CC} = 0V)

Parameter	Symbol	Max Limit	Unit
Clock Input	$C_{IN(\phi)}$	20	pF
Input	C_{IN}	10	pF
Output	C_{OUT}	20	pF

Note: All pins except pin under test tied to ground.

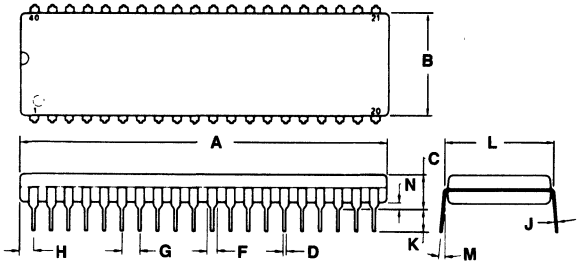
PACKAGE DIMENSIONS

40-PIN CERAMIC DIP



DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	50.29	51.31	1.980	2.020
B	14.86	15.62	0.585	0.615
C	2.54	4.19	0.100	0.165
D	0.38	– 0.53	0.015	0.021
F	0.76	1.40	0.030	0.055
G	2.54 BSC		0.100 BSC	
H	0.76	1.78	0.030	0.070
J	0.20	0.33	0.008	0.013
K	2.54	4.19	0.100	0.165
L	14.60	15.37	0.575	0.605
M	0°	10°	0°	10°
N	0.51	1 52	0.020	0 060

40-PIN PLASTIC DIP



DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	51.28	52.32	2.040	2.060
B	13.72	14.22	0.540	0.560
C	3.55	5 08	0.140	0.200
D	0.36	0.51	0.014	0 020
F	1.02	1.52	0.040	0 060
G	2.54 BSC		0.100 BSC	
H	1.65	2 16	0.065	0.085
J	0.20	0 30	0 008	0 012
K	3 05	3.56	0.120	0.140
L	15 24 BSC		0.600 BSC	
M	7°	10°	7°	10°
N	0.51	1.02	0.020	0.040

SECTION 3
R6500/* MICROCOMPUTERS

R6500/* SINGLE-CHIP MICROCOMPUTER FAMILY
Higher Performance, Broader Applications, Software Compatibility

The R6500/* single-chip microcomputers are completely software compatible with the 8-bit multi-chip family. They let you move easily from a multi-chip to a single-chip system solution when the application warrants it. They also function as intelligent peripheral controllers. The family continues to expand to include dual processors and CMOS versions. The R6500/* devices have faster execution speeds for most applications, based on our competitors own figures, even though some others use higher frequency crystals.

Features include 1.5 to 4K bytes of ROM, 64 to 192 bytes of RAM, 23 to 56 I/O ports, multiple use counter/timers, serial communication channels, new bit manipulation instructions, expansion bus, multiple bus interfaces, directly executable RAM with low power standby, multiple interrupts, all from a single 5V power supply.

Three intelligent peripheral controllers offer design effective upgrading potentials for existing 6800, 8080, Z80 and 6500 systems. They're also available in ROM-less versions, for large memory system applications and for developing and simulating products in prototype, with external memory.

And, two versions even have all system software on chip, including an operating system and high level FORTH language. It's an extremely versatile single-chipper, and available in three configurations to accommodate application programs to 48K.

Three different sets of development ROM permit systems from 16 to 40 I/O and 8K to 48K of application program memory.

As the highest performance single-chip family, the R6500/* devices are in use now in applications such as printers, telephone answering equipment, fixed disk drives, stereos, industrial controllers, telecom, cash registers, sewing machines, test equipment and more.

Check for yourself and see how a Rockwell R6500/* can solve your system problem. There are no higher performing 8-bit single chippers, regardless of clock speeds.

ROCKWELL NMOS MICROCOMPUTERS—THE TOP PERFORMERS IN INDUSTRY

Features/Models	R6500/1	R6500/11	R6500/15	R6500/12	R6500/16	R6501Q/11Q	R6500/41	R6500/42	R6541Q
• ROM (x8)	2048	3072	4096	3072	4096	—	1536	1536	256
• RAM (x8)	64	192	192	192	192	192	64	64	64
• I/O Lines	32	32	32	56	56	32	23	47	23
• Serial Comm.	—	USART	USART	USART	USART	USART	—	—	—
• 16-Bit Counters	ONE	TWO	TWO	TWO	TWO	TWO	ONE	ONE	ONE
• Host/Slave Bus	—	—	—	—	—	—	80/65	80/65	80/65
• Expansion Bus	—	16K	16K	16K	16K	65K	4K	4K	8K/4K
• Interrupts									
— External	4	6	6	6	6	6	4	4	5
— Internal	1	4	4	4	4	4	1	1	1
— Host	—	—	—	—	—	—	2	2	2
• Standby RAM (mW)	35	12	12	12	12	12	—	—	—
• Package	40 DIP	40 DIP	40 DIP	64 QUIP	64 QUIP	64 QUIP	40 DIP	64 QUIP	64 QUIP
Alternatives for	8048/49	8051				8031	8041		

R65C00/21 DUAL CMOS MICROCOMPUTER AND R65C29 DUAL CMOS MICROPROCESSOR

PRELIMINARY

INTRODUCTION

FEATURES

- Two enhanced CMOS R6502 CPU's in one device
  - —Common memory and I/O
  - —Shared data and subroutines
  - —Independent CPU registers and interrupt vectors
  - —Independent reset operation and programs
  - —R6502 software and timing compatible
- 10 new instructions for faster and smaller programs
  - —Unsigned Multiply (MUL)
  - —Set and Reset Memory Bit (SMB and RMB)
  - —Branch on Bit Set and Reset (BBS and BBR)
  - —Unconditional Branch (BRA)
  - —Push and Pull Index Registers (PHX, PHY, PLX, PLY)
- Microcomputer/microprocessor/peripheral controller operation
  - —Stand-alone microcomputer
    2048 × 8 mask programmable ROM
    128 × 8 random access memory (RAM)
  - —Enhanced microprocessor
    Built-in RAM, ROM and I/O with expandability
    8-, 12- or 16-bit extension address bus
  - —Programmable peripheral controller
    Host data bus interface (Z80/8080 or 6500/6800 option)
    Self-contained or expandable
- 16-bit Counter/Timer A with eight modes, and prescaler
  - —Timer Off
  - —Free-Run Event Counter
  - —Free-Run Pulse Width Measurement
  - —One-Shot Retriggerable Timer
  - —One-Shot Interval Timer
  - —Free-Run Interval Timer
  - —One-Shot Pulse Generator
  - —Free-Run Pulse Generator
- 16-bit Counter/Timer B with four modes
  - —Free-Run Interval Timer
  - —Free-Run Pulse Generator
  - —Event Counter
  - —Pulse Width Measurement
- Up to 52 general purpose input/output lines
  - —Five bidirectional 8-bit ports (PA, PB, PC, PD and PF)
  - —One 8-bit output port (PE)
  - —One 4-bit input port (PG)
  - —Multi-purpose operation for selected ports
- Nine interrupts
  - —Positive and negative edge detect
  - —Low level detect (external IRQ)
  - —Counter/Timer A and B underflow
  - —Inter-processor communication
  - —Host computer data transfer
  - —Non-maskable
  - —Reset
- Flexible system operation
  - —Memory mapped I/O for easy programming
  - —Page zero location for memory efficient access
- Low power at normal frequency (40 mw at 2 MHz)
- Reduced power at low frequency (2.0 mw at 2 MHz/128)
- System clock rates from 10 KHz to 4 MHz
- 5V ± 10% power supply
- 64-pin QUIP

SUMMARY

The Rockwell R65C00/21 is a complete, high performance 8-bit, CMOS dual microcomputer in a single chip and is compatible with all R6500 microprocessors except that it has additional instructions including a 10-clock time multiply.

The R65C00/21 consists of two enhanced instruction set 6502 CPU's in one device. The device also has 2048 bytes of Read-Only Memory (ROM), 128 bytes of Random Access Memory (RAM) and versatile interface circuitry. The interface circuitry consists of two multimode programmable 16-bit counter/timers and 52 general purpose input/output lines. Some of these input/output lines may be used as address, data and control lines for expanded systems or as data and control lines when the R65C00/21 is used as a programmable peripheral controller.

The two CPU's in the R65C00/21 are functionally independent. Each has its own set of registers, its own reset and interrupt vectors and operates under control of its own program. The two CPU's do, however, share the same memory and system I/O resources. This allows direct communication between the two CPU's and allows sharing of subroutines and common data areas where desired. Programming and system design for applications which require simultaneous control of two or more independent asynchronous processes is thus simplified because one CPU may control one process while the other controls

another one. Consequently, complex programming usually needed to interleave the control functions or to implement an interrupt driven system, is not required.

In a multiple computer approach, both processors may need the same subroutines so that some portions of memory must be duplicated in both systems. The dual CPU's share the same program memory, therefore only one set of subroutines is required and both CPU's may even be using them at the same time without interference.

In addition to the dual CPU's, the R65C00/21 also has the innovative architecture and the demonstrated high performance of the well established R6502 CPU, flexible input/output which provides improvements over the R6522 Versatile Interface Adapter (VIA) device, and production efficient on-chip ROM and RAM. These features make the R65C00/21 a leading candidate for most imbedded microcomputer applications.

A system using the R65C00/21 Dual CMOS Microcomputer will be simpler in design, use less program memory, require fewer components, reduce circuit board sizes, simplify test requirements, and minimize field maintenance—all contributing to lower production and support costs. In addition, simpler designs shorten development effort and time—leading to reduced development costs and faster product to market.

The R65C29 Dual CMOS Microprocessor, a ROM-less version of the R65C00/21 with permanently extended data and address bus, is also available. The R65C29 is ideal for dual CPU applications requiring changeable ROM and/or extended RAM, ROM or I/O, and can also be used for R65C00/21 prototype circuit development. The R65C00/21 can also operate in an emulation mode, like the R65C29, with its internal ROM disabled.

DEVELOPMENT SYSTEM SUPPORT

Prototype circuit and software development support are available using the Rockwell Design Center (RDC) and R65C00/21 Personality Module. Program development and debugging aids such as text editing, symbolic assembly with conditionals and macros at the absolute and relocatable/linking level, and single/multiple step execution with instruction/data tracing are provided. Real-time in-circuit emulation in the target environment is also supported.

NOTE

All descriptions of R65C00/21 operation in this document also apply to the R65C29 except for internal ROM, and as otherwise noted.

ORDERING INFORMATION

The R65C00/21 Dual CMOS Microcomputer can be ordered in volume quantities with the following speed capability and mask option indicated in the R65C00/21 ROM Code Order Form (Document Order No. 2134)

- 1, 2, 3, or 4 MHz system clock (Ø2)
- Crystal/master clock or slaved clock input mask option

The R65C29 Dual CMOS Microprocessor has the following characteristics:

- Crystal/master clock input
- 8-bit data bus and 16-bit address bus extension
- No internal ROM

INTERFACE

The interfaces for the R65C00/21 and R65C29 are illustrated in Figure 1.

The pin assignments for the R65C00/21 and the R65C29 are shown in Figure 2. The R65C29 pin assignments are the same as the R65C00/21 except that bus expansion functions are permanently assigned instead of general purpose ports D and E.

The interface signals for the R65C00/21 and R65C29 are described in Table 2. The descriptions of the selectable bus expansion pins (16-bit address mode) for the R65C00/21 apply to permanent bus expansion pins for the R65C29.

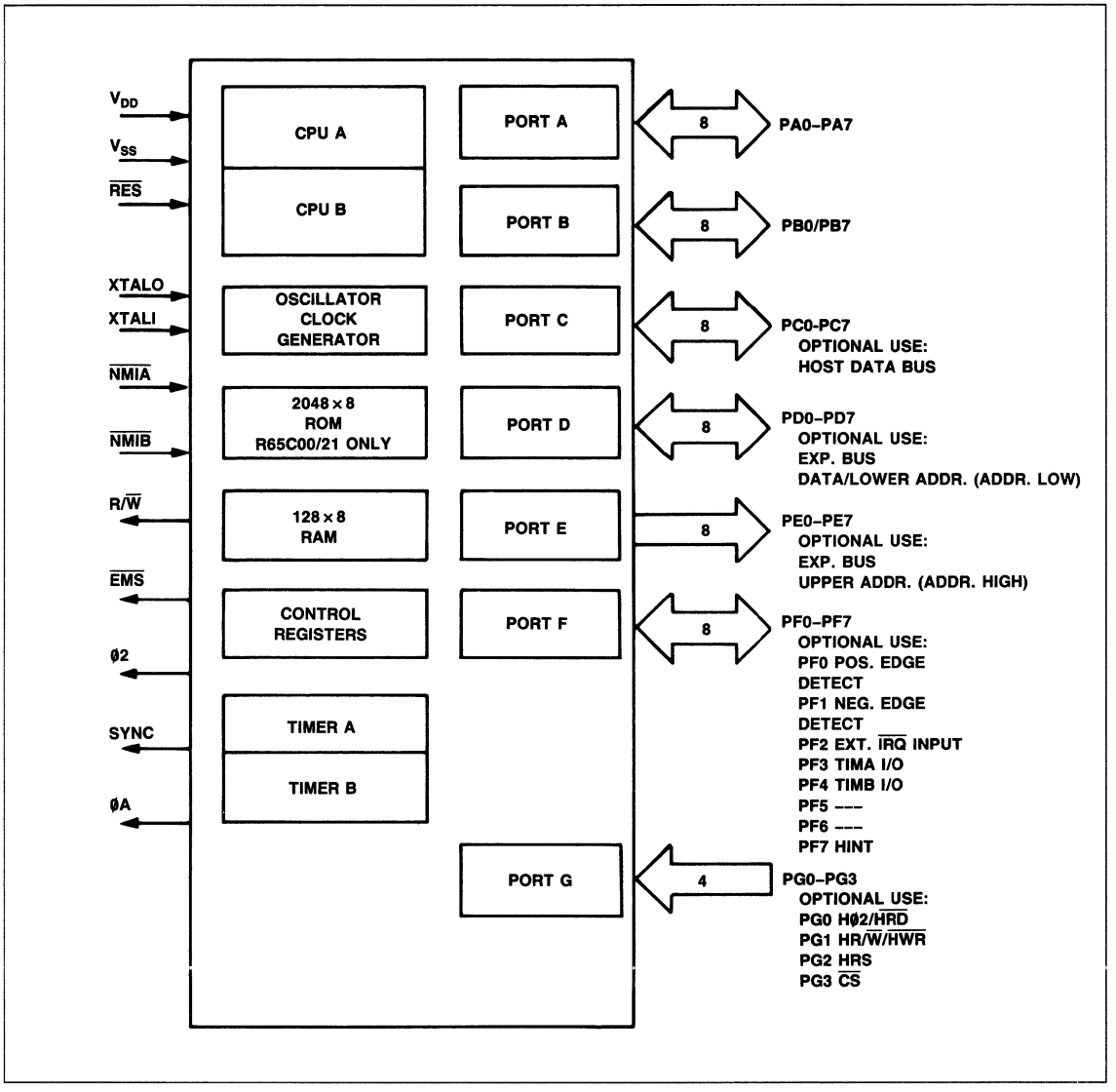


Figure 1. R65C00/21 and R65C29 Interface Diagram

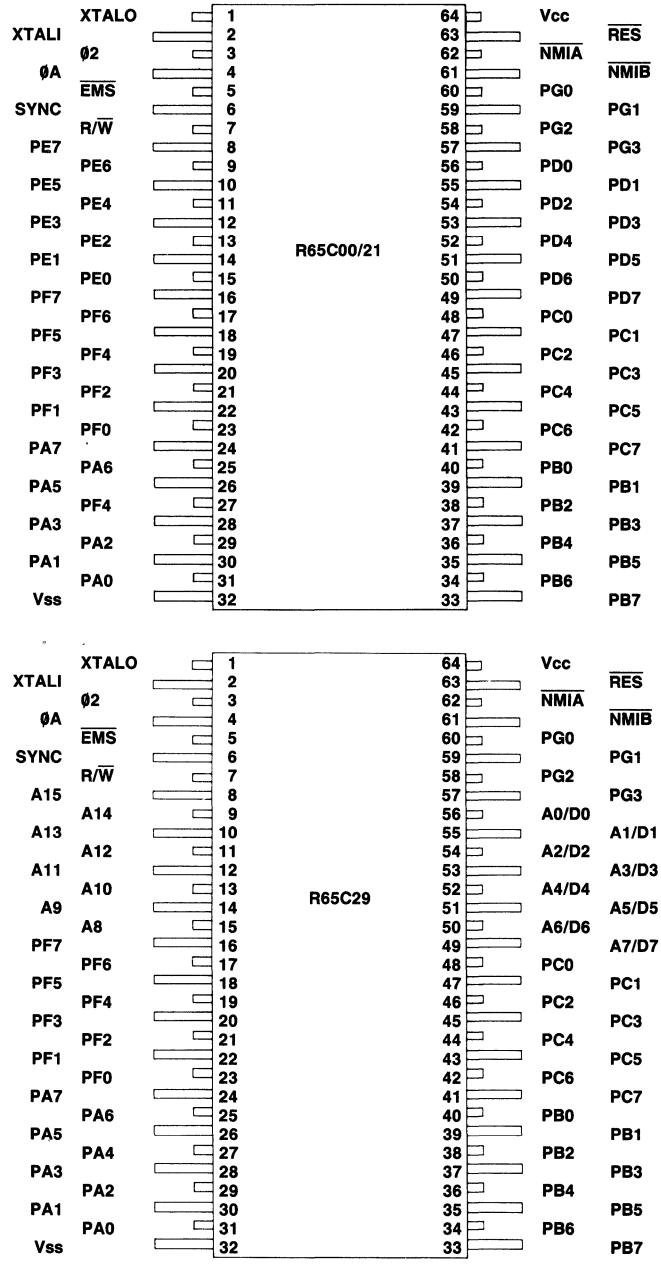


Figure 2. R65C00/21 and R65C29 Pin Assignments

Table 1. R65C00/21 Pin Description

Signal Name	Pin No.	I/O	Description
PA0-PA7	31-24	I/O	**Port A.** General purpose 8-bit I/O Port A.
PB0-PB7	40-33	I/O	**Port B.** General purpose 8-bit I/O Port B.
PC0-PC7	48-41	I/O	**Port C.** General purpose 8-bit I/O Port C. Host Data Bus in Host Mode.
PD0-PD7	56-49	I/O	**Port D.** General purpose 8-bit I/O Port D. Multiplexed lower address (A0 to A7) and Data Bus (D0-D7) when Bus Extension Mode is selected.
PE0-PE7	15-8	O	**Port E.** General purpose 8-bit output Port E. Upper address (A8 to A11 or A8 to A15) when Bus Expansion Mode is selected.
PF0-PF7	23-16	I/O	**Port F.** General purpose 8-bit I/O Port F. Under software control, each line has alternate functions as follows:
PF0NEG (PF0)	23	I	**PF0 Positive Edge Detect.** Maskable CPU interrupt on PF0 Positive Transition.
PF1POS (PF)	22	I	**PF1 Negative Edge Detect.** Maskable CPU interrupt on PF1 Negative Transition.
PF2LOW (PF2)	21	I	**PF2 Low Level Detect.** Maskable CPU interrupt on PF2 Low (external IRQ).
TIMA (PF3)	20	I/O	**Timer A External Input/Output.**
TIMB (PF4)	19	I/O	**Timer B External Input/Output.**
$\overline{\text{HINT}}$ (PF7)	16	O	**Host Interrupt.** Active-low maskable interrupt request to Host.
PG0-PG3	60-57	I	**Port G.** General purpose 4-bit input Port G. Under software control, Port G serves as the Host Control Bus as follows:
Hø2/$\overline{\text{HRD}}$ (PG0)	60	I	**Host Bus Clock/Read Strobe Input.** ø2 for 6500/6800 bus; Read Strobe for Z80/8080 bus.
HR/$\overline{\text{W}}$/$\overline{\text{HWR}}$ (PG1)	59	I	**Host Bus Read-Write/Write Strobe Input.** R/$\overline{\text{W}}$ for 6500/6800 bus; Write Strobe for Z80/8080 bus.
HRS (PG2)	58	I	**Host Bus Register Select Input.** Low selects Data Buffer; high selects Status Flags.
$\overline{\text{CS}}$ (PG3)	57	I	**Host Bus Active-Low Chip Select Input.** Low selects Host Bus operation depending on HRS and HR/$\overline{\text{W}}$/$\overline{\text{HWR}}$ coding and Host Control and Status Register contents; high disables Host Bus interface.
$\overline{\text{RES}}$	63	I	**Reset.** Active-low Reset input initializes R65C00/21 to initial conditions—resets all registers and I/O lines.
$\overline{\text{NMIA}}$	62	I	**CPU A Non-Maskable Interrupt.** Non-maskable negative edge sensitive interrupt input to CPU A.
$\overline{\text{NMIB}}$	61	I	**CPU B Non-Maskable Interrupt.** Non-maskable negative edge sensitive interrupt input to CPU B.
$\overline{\text{EMS}}$	5	O	**External Memory Strobe.** Active-low.
ø2	3	O	**System Phase 2 Clock Output.** Maskable as system clock input for slave operation.
R/$\overline{\text{W}}$	7	O	**Read/Write.** Read/write control output. High during read, low during write.
SYNC	6	O	**Sync.** Instruction sync output. High When Op Code fetched
øA	4	O	**Phase A.** Phase A clock output. High during CPU A bus cycle, low during CPU B bus cycle.
XTALO	1	O	**Crystal/Master Clock Return.** Output connection to crystal (or no connection if external master clock connected to XTALI). Input frequency is two times system clock (ø2) rate.
XTALI	2	I	**Crystal/Master Clock Input.** Input connection from crystal (or external master clock).
VCC	64		**Power.** 5.0 Vdc.
VSS	32		**GND.** Signal and power ground.

FUNCTIONAL DESCRIPTION

The R65C00/21 consists of two central processor units (CPU's), a 2048 × 8 read-only memory (ROM), a 128 × 8 random access memory (RAM), five 8-bit parallel I/O ports, one 8-bit output port, one 4-bit input port, two 16-bit counter/timer systems, a variety of I/O control registers, and an independent interrupt control system for each CPU. All of the ROM, RAM, I/O, internal buses, and the arithmetic logic unit (ALU) are shared by the two CPU's. A memory map of the system is shown in Figure 3. An overall block diagram of the R65C00/21 is shown in Figure 4.

NOTE

Throughout this document, unless specified otherwise, all memory or register address locations are specified in hexadecimal notation.

INTERNAL MEMORY

INTERNAL READ-ONLY-MEMORY (ROM)

The ROM in the R65C00/21 consists of 2048 (2K) bytes of mask programmable memory with an address space from F800 to FFFF. ROM locations FFF2 through FFFF are assigned to interrupt and reset vectors for the two CPU's.

INTERNAL RANDOM ACCESS MEMORY (RAM)

The internal RAM consists of 128 bytes of read/write memory with assigned page zero addresses of 0080 through 00FF.

EXTERNAL MEMORY

External memory can be addressed by selecting the Bus Expansion Mode in the Bus Control Register. Address space from 0200 through EFFF may be accessed for either RAM, ROM, or I/O purposes as the particular application requires it. In addition, there are 32 bytes from 0020 through 003F which may be used for I/O expansion and 256 bytes from 0100 through 01FF which may be external RAM.

CPU LOGIC

Each CPU in the R65C00/21 is effectively a standard R6502 CPU with 10 extra instructions utilizing 40 operation codes which are unused in the R6502. Therefore, each CPU has an 8-bit accumulator, two 8-bit index registers (X and Y), an 8-bit Stack Pointer Register, an 8-bit Status Register, a 16-bit Program Counter, independent interrupt circuitry, and an instruction register with state counter. The internal buses, memory, instruction decoding circuitry, and ALU are shared by the two CPU's on alternate clock cycles.

ACCUMULATORS

The accumulator in each CPU is a general purpose 8-bit register that stores the results of most arithmetic and logic operations. Additionally, the accumulator contains one of the two data words used in these operations.

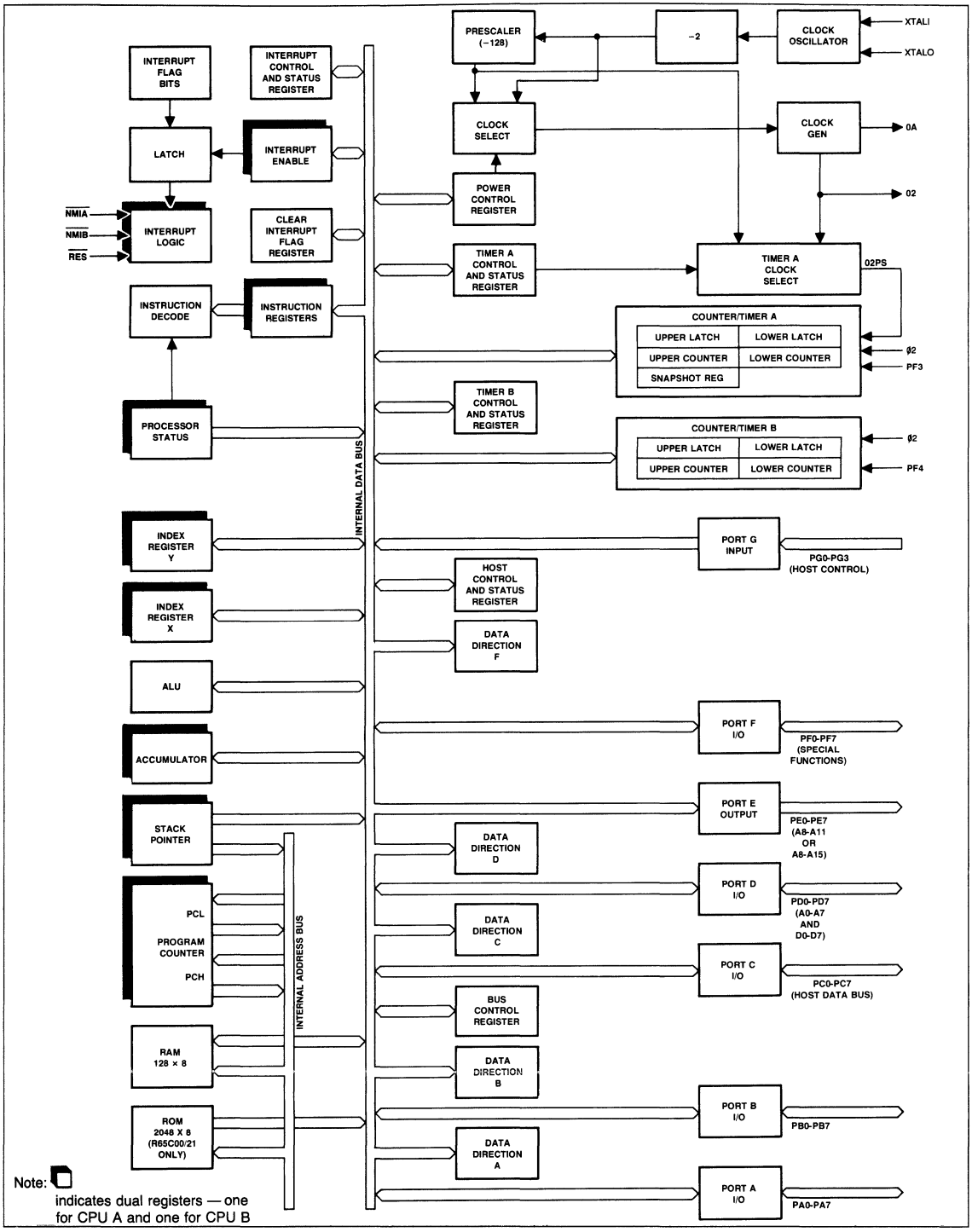
INDEX REGISTERS

Each CPU has two index registers, X and Y. Each index register may be used as a modifier to a base address supplied as a part of the instruction being processed. The resulting effective address is usually the sum of the base address plus the contents of the indicated index register. The index registers are used in a number of the addressing modes including zero page indexed, absolute indexed, post-indexed indirect and pre-indexed indirect. Each index register also has a family of instructions which allow loading, storing, incrementing, decrementing, and comparing the contents of the register. These are discussed thoroughly in the R6500 Programming Manual (Order No. 202).

ADDRESS (HEX)	
0000 001F	I/O AND CONTROL REGISTERS
0020 003F	EXTERNAL I/O EXPANSION[2]
0040 007F	NOT ACCESSIBLE
0080 00FF	INTERNAL RAM (128 BYTES)[1] (SHARED WITH 0180-01FF)
0100 017F	EXTERNAL RAM EXPANSION[2]
0180 01FF	INTERNAL RAM (128 BYTES)[1] (SHARED WITH 0080-00FF)
0200 EFFF	EXTERNAL MEMORY AND I/O EXPANSION[2]
F000 F7FF	NOT ACCESSIBLE
F800 FFF1	INTERNAL ROM (2048 BYTES)
FFF2 FFF3	NMIB VECTOR
FFF4 FFF5	RESB VECTOR
FFF6 FFF7	IRQB VECTOR
FFF8 FFF9	NOT USED
FFFA FFFB	NMIA VECTOR
FFFC FFFD	RESA VECTOR
FFFE FFFF	IRQA VECTOR

Notes:
1. When bit 4 of the Bus Control Register (BCR) is a 0 (default value), the 128 bytes of internal RAM are redundantly mapped into both page zero and page one and are addressable as either 0080-00FF or 0180-01FF. When BCR bit 4 is a 1, all of page one RAM (256 bytes) is mapped externally (0100-01FF) and the 128 bytes of internal RAM are dedicated to page zero (0080-00FF).
2. Accessible in bus expansion mode.

Figure 3. R65C00/21 Memory Map



Note: ❐ indicates dual registers — one for CPU A and one for CPU B

Figure 4. R65C00/21 and R65C29 Block Diagram

STACK POINTERS

Each CPU in the R65C00/21 has its own independent 8-bit Stack Pointer Register located in RAM on page zero/one and is pointed to by a Stack Pointer. Each Stack Register is automatically incremented and decremented under control of the appropriate CPU to perform proper stack manipulations in response to user instructions, an IRQ interrupt or an external NMI interrupt of the appropriate CPU. The Stack Pointers must be initialized by the user program.

These stacks allow simple implementation of multiple level independent interrupts in each CPU, subroutine nesting, and simplification of many types of data manipulation without the programmer continually being aware of specific memory addresses. The JSR, BRK, RTI, RTS, PHA, PLA, PHP, PLP, PHX, PLX, PHY and PLY instructions all make use of the stack and the appropriate CPU's Stack Pointer.

Each stack may be visualized as a deck of cards which may only be accessed from the bottom of the deck. The value to be stored is written on a card and then that card is placed on the bottom of the deck (pushed onto the stack). When the data are to be read, the bottom card is removed from the deck and the value on it transferred to the appropriate register (pulled from the stack to the specific register). Each time data are to be used as an address, the value is stored in the addressed memory cell, and the Stack Pointer is decremented by 1. When the data are read (or "pulled") from the stack, the Stack Pointer is incremented by 1 and the resulting value can be used to address the data. The data are read from the addressed memory cell and then transferred to the appropriate register in the CPU.

Each CPU must have an independent starting location for its stack. It is the programmer's responsibility to see that the RAM utilized for each CPU stack does not conflict. It is recommended that the CPU requiring less depth in its stack be assigned the OXFF location and the other stack be started a safe distance below it. The two stacks are physically located either on page zero (although addressed as page one) for single-chip operation, or externally on page one when extended addressing is selected. (See Note 1 in Figure 3). The default areas for the stacks are on page zero. In either case, both stacks are on the same page.

ARITHMETIC AND LOGIC UNIT (ALU)

All arithmetic and logic operations for both CPU's take place in a shared ALU. Incrementing and decrementing of the index registers and memory also take place here. The ALU stores data for only one cycle. Consequently, data placed on the inputs at the beginning of a cycle are processed and gated to one of the registers, or to memory, during the next cycle.

Each bit of the ALU has two inputs. These inputs may be tied to various internal buses or to a logic zero; the ALU then generates the function (AND, OR, SUM, etc.) using the data on the two inputs.

PROGRAM COUNTERS

The 16-bit program counters for each CPU provide addresses that step each processor through sequential instructions in a stored program. The program counter for each CPU is initially set to the value stored as the reset vector in CPU A (RESA at FFFC) and in CPU B (RESB at FFF4) when power is applied to the R65C00/21. Each time a processor fetches an instruction from memory, the lower (least significant) byte of its program counter (PCL) is placed on the low-order eight bits of the address bus and the higher (most significant) byte of the program counter (PCH) is placed on the high-order eight bits of the address bus. The counter is incremented each time an instruction or operand is fetched from memory.

The contents of the program counter are replaced with a new value when a JMP, JSR, RTS, RTI, BRK, or any of the branch instructions are executed. Also, the program counter value is replaced when an external non-maskable interrupt $\overline{\text{NMIA}}$ or $\overline{\text{NMIB}}$, an internal interrupt request, an external interrupt request via PF2 (see Port F description) or reset ($\overline{\text{RES}}$) occurs.

INSTRUCTION REGISTERS AND INSTRUCTION DECODE

Instructions selected by the program counter are fetched from ROM or RAM (or Port D if in Expanded Bus Mode) and gated onto the internal data bus. These instructions are latched into the proper instruction register and then decoded using common decoding circuits for both CPU's. Timing, status bits, and interrupt controls are interpreted together with the instruction code to generate control signals for the various registers in the appropriate CPU.

INTERRUPT LOGIC

Each CPU has its own logic which controls the sequencing of three types of interrupts: $\overline{\text{RES}}$, $\overline{\text{NMI}}$, and $\overline{\text{IRQ}}$. The same RESET ($\overline{\text{RES}}$) pin is used for both CPU's; consequently, reset occurs on both CPU's at the same time. A different reset vector (RESA and RESB) exists for each CPU to allow initialization of the separate and independent programs.

Separate pins are used for the two processors' non-maskable interrupts ($\overline{\text{NMIA}}$ and $\overline{\text{NMIB}}$). Each processor has its own NMI vector; CPU A uses NMIA Vector at FFFA and CPU B uses NMIB Vector at FFF2.

Three different types of external interrupt conditions can be detected by connecting the external signal to one of three Port F input pins. A positive-going edge, a negative-going edge, and an external interrupt request ($\overline{\text{IRQ}}$), i.e., a low level, can be detected on PF0, PF1 and PF2, respectively. Internally, IRQ conditions can be generated by time-out of either of the two 16-bit counter/timers, upon interprocessor-communication request by the other CPU, or by the Host Interface Port.

In each case, the interrupt condition is reported as an interrupt flag in a control/status register associated with the functional area. Each CPU can either enable or disable IRQ generation by setting or resetting a corresponding interrupt enable bit in the same or associated control/status register.

Furthermore, each CPU can control whether or not its processing is interrupted when an interrupt request ($\overline{\text{IRQ}}$) is generated. Each CPU has its own Processor Status Register (PSRA and PSRB) with the capability of disabling $\overline{\text{IRQ}}$ interrupts when its own "I flag" bit is a 1.

NEW AND MODIFIED INSTRUCTIONS

In addition to the standard R6502 instruction set, ten new instructions have been added and minor timing and other changes have been made to a few other instructions. All of these additions and changes are discussed in this section. Refer to the Instruction Set Op Code Matrix for the operation codes and addressing modes of all instructions. The times indicated for each instruction are given in terms of CPU clock-times.

UNSIGNED MULTIPLY (MUL)

The 10 clock-time hardware multiply instruction multiplies the 8-bit contents of the Y register by the 8-bit contents of the A register to give a 16-bit product. At the completion of the multiply operation, the most significant half of the product resides in the A register and the least significant half in the Y register. This operation uses unsigned numbers only. This instruction uses the implied addressing mode and, consequently, requires one byte for the op code.

SET MEMORY BIT (SMB m, ADDRESS.)

This instruction uses zero page addressing only and requires five cycle times. It sets the designated bit in the addressed memory cell or I/O port to a 1. The first byte of the two-byte instruction identifies the operation and the bit to be set while the second byte designates the address of the word in which the bit is to be set. Eight op codes are used for the eight bit locations in a byte.

RESET MEMORY BIT (RMB m, ADDRESS.)

This instruction operates in the same way as the SMB instruction except that the bit is set to 0.

BRANCH ON BIT SET RELATIVE (BBS m, ADDRESS, DESTINATION)

This instruction tests one of eight bits designated by a three-bit immediate field within the first byte of the instruction. The second byte designates the address of the byte to be tested within the zero page address range (memory or I/O ports). The third byte of the instruction specifies the 8-bit relative address to which the instruction branches if the bit tested is a 1. If the bit tested is not set to a 1, the next sequential instruction is executed. This instruction requires five cycles if the branch is not executed, six cycles if the branch executes to the same page, or seven cycles if it branches to a different page.

BRANCH ON BIT RESET RELATIVE (BBR m, ADDRESS, DESTINATION)

This instruction is similar to the BBS instruction except that the branch takes place if the bit tested is a 0.

INDEX REGISTER STACK OPERATIONS (PHX, PLX, PHY, AND PLY)

These instructions are similar to the PHA and PLA instructions in the conventional R6502 except that they push or pull the X or Y registers to and from the stack, respectively. The push instructions require three instruction cycles and the pull instructions require four cycles.

UNCONDITIONAL BRANCH (BRA)

This unconditional branch is a branch always instruction. It operates similar to the conditional branches of the R6502 except that the relative branch always occurs. It executes in three cycles if the branch is to the same page or four cycles if it is not. Two bytes are required, one for the op code and the other for the relative address.

INSTRUCTION DIFFERENCES FROM R6502

Decimal add and decimal subtract instructions on the R65C00/21 require one cycle time longer than their binary equivalents. The add and subtract times are the same for both decimal and binary operation on the R6502.

The decimal mode flag (D) in the processor status registers default to binary (D=0) operation when the R65C00/21 is RESET, whereas this bit is uninitialized on the R6502.

The indirect jump instruction increments the page address when the indirect pointer crosses a page boundary, whereas on the R6502 it does not.

PROCESSOR STATUS REGISTERS

Each CPU has its own 8-bit Processor Status Register. Each register contains seven status flags. Some of these flags are controlled by the user program; others may be controlled both by the user's program and the appropriate CPU. The R65C00/21 instruction set contains a number of conditional branch instructions which are designed to allow testing of these flags.

CARRY BIT (C)

The carry bit (C) can be considered the ninth bit of an arithmetic operation. It is set to a 1 if a carry from the eighth bit has occurred, or it is cleared to 0 if no carry has occurred, as a result of arithmetic or shift operations.

The carry bit may be set or cleared under program control by use of the Set Carry (SEC) or Clear Carry (CLC) instructions, respectively. Other operations which affect the carry bit are ADC, ASL, CMP, CPX, CPY, LSR, PLP, ROL, ROR, RTI, and SBC.

ZERO BIT (Z)

The zero bit (Z) is set to a 1 by the CPU during any data movements, or calculations, which sets all eight bits of the result to zero for that CPU. This bit is cleared to a 0 when all eight bits of a data movement, or calculation, operations are not all zero for that CPU. The R6500 instruction set contains no instruction to specifically set or clear the Z flag bit. The Z flag bit is, however, affected by the following instructions: ADC, AND, ASL, BIT, CMP, CPX, CPY, DEC, DEX, DEY, EOR, INC, INX, INY, LDA, LDX, LSR, ORA, PLA, PLP, PLX, PLY, ROL, ROR, RTI, SBC, TAX, TAY, TXA, TSX, and TYA.

INTERRUPT DISABLE BIT (I)

The interrupt disable bit (I) controls the servicing of an interrupt request ($\overline{IRQ}$). If the I bit is set to a 0 in the Processor Status Register of one, or both, of the CPU's, the $\overline{IRQ}$ signal will be serviced by that particular CPU. If the bit is set to a 1 for one or both of the CPU's, the $\overline{IRQ}$ signal will be ignored by that CPU. Each CPU will set its interrupt disable bit to a 1 if a $\overline{RES}$, an $\overline{IRQ}$, or its non-maskable interrupt ($\overline{NMI}$) signal is detected. Interrupting one processor does not affect the other one unless it is programmed to respond to the same interrupt.

The I bit is cleared for each CPU when that CPU executes a Clear Interrupt Disable (CLI) instruction and is set under software control by a Set Interrupt Disable (SEI) instruction. This bit is also set by the Break (BRK) instruction. The Return From Interrupt (RTI) and Pull Processor Status (PLP) instructions also affect the I bit by setting it to the value which was stored on the stack.

DECIMAL MODE BIT (D)

The decimal mode bit (D) controls the arithmetic mode of its CPU. When this bit is set to a 1, the adder operates as a decimal adder for the Add with Carry (ADC) and the Subtract With Carry (SBC) instructions. These instructions, in the decimal mode, require one additional CPU cycle time compared with binary mode or the decimal mode in the conventional R6500. (In the conventional R6500, the decimal and binary arithmetic operations are the same speed.) When the bit is a 0, the arithmetic is performed in straight binary. The decimal mode is controlled only by the programmer for each of the CPU's. The Set Decimal Mode (SED) instruction causes decimal arithmetic to be performed and the Clear Decimal Mode (CLD) instruction causes binary arithmetic to be performed by that CPU. The PLP and RTI instructions also affect the decimal mode bit.

The D bit for each CPU is automatically set to the zero state (binary mode) when the R65C00/21 is reset by $\overline{RES}$.

BREAK BIT (B)

The break bit (B) determines the type of condition which caused the IRQ service routine to be entered. If the IRQ service routine was entered because a BRK instruction was executed by its CPU, the B bit is set to a 1. If the service routine was entered because of an $\overline{IRQ}$ signal being generated, the B is set to a 0. There are no instructions which directly set or clear this bit.

OVERFLOW BIT (V)

The overflow bit (V) indicates that the result of a signed binary addition or subtraction operation is a value which cannot be contained in seven bits (outside the range of −128 to +127). This indicator only has meaning when signed arithmetic is performed. In this case, the arithmetic operations are being performed on the sign and seven magnitude bits for one byte, or the most significant byte of a longer signed number. When the ADC or SBC instruction is executed, the overflow bit is set to a 1 if the polarity of the sign bit is changed because the result exceeds +127 or −128 in absolute magnitude. Otherwise, the V bit is cleared to a 0. The V bit may be cleared by the programmer by executing a Clear Overflow (CLV) instruction in the appropriate CPU.

The overflow bit is also affected by the BIT instruction. The BIT instruction samples specific bits in memory or I/O interrupt status words. Most of the I/O devices used in the R6500 family and most of the interrupt flags in the R65C00/21 have interrupt flags in the upper two bits of the register. The BIT command copies these two most significant bits of the addressed word into the N and V flags. The V flag is set to the same state as bit 6 of the addressed words and the N flag copies bit 7.

The instructions which affect the V flag are ADC, BIT, CLV, PLP, RTI and SBC.

NEGATIVE BIT (N)

The negative bit (N) indicates that the sign bit (bit 7) in the resulting value of a data movement or arithmetic operation is a 1. If the value represents a signed number, the most significant bit being a 1 indicates a negative number. If the sign bit is a 0, the result is interpreted as a positive value. The BIT instruction copies the most significant bit of the addressed memory cell or I/O register into the N flag bit.

There are no instructions that set or clear the N bit directly since the N bit represents only the status of a result. The instructions which produce a result that affects the state of the N bit are AND, ASL, BIT, CMP, CPX, CPY, DEC, DEX, DEY, EOR, INC, INX, INY, LDA, LDX, LDY, LSR, ORA, PLA, PLP, PLX, PLY, ROL, ROR, RTI, SBC, TAX, TAY, TSX, TXA, and TYA.

Processor Status Registers (PSRA and PSRB)

7	6	5	4	3	2	1	0
NEG (N)	OVFL (V)	NOT USED	BRK (B)	DEC (D)	IRQ ENBL (I)	ZERO (Z)	CARRY (C)

Bit 7 **Negative (N)**[1]
1 Negative Value
0 Positive Value

Bit 6 **Overflow (0)**[1]
1 Overflow Set
0 Overflow Clear

Bit 5 **Not Used** (Don't care value)

Bit 4 **Break Command (B)**[1]
1 Break Command
0 Non-break Command

Bit 3 **Decimal Mode (D)**[3]
1 Decimal Mode
0 Binary Mode

Bit 2 **Interrupt Enable (I)**[2]
1 IRQ Interrupt Disable
0 IRQ Interrupt Enable

Bit 1 **Zero (Z)**[1]
1 Zero Result
0 Non-Zero Result

Bit 0 **Carry (C)**[1]
1 Carry Set
0 Carry Clear

Notes:
1. Not initialized by $\overline{RES}$.
2. Set logic 1 by $\overline{RES}$.
3. Cleared to logic 0 by $\overline{RES}$
4. There are two Processor Status Registers, one for each CPU.

INPUT/OUTPUT AND CONTROL/STATUS REGISTERS

REGISTER ADDRESSES

Table 2 shows the input/output, control/status and timer/counter registers which are addressed on page zero from locations 00 through 1D. Some of the registers combine other functions when they are read or written. The table lists both the primary and secondary types of functions. Table 3 summarizes the register formats.

All control/status registers and data direction registers are cleared to zero by a $\overline{RES}$. Thus, the zero state of each bit defines the default operating modes. Each register is associated with a functional area in the microcomputer, e.g., parallel input/output, timer/counter, bus control, etc. The detail operation of each register is defined in the appropriate sections.

Thirteen registers are used for input/output functions and nine registers used for timer/counter functions. The use of these registers is discussed in later sections.

Seven control/status registers control and monitor the basic operation of the R65C00/21. The registers and their primary functions are as follows:

- BCR Bus Control Register—defines expansion bus modes
- HCSR Host Control and Status Register—defines host bus and interrupts
- ICSR Interrupt Control and Status Register—enables and reports interrupt conditions
- CIFR Clear Interrupt Flags Register
- PCR Power Control Register—selects low power mode
- TACSR Timer A Control and Status Register—controls and monitors Timer A operation
- TBCSR Timer B Control and Status Register—controls and monitors Timer B operation

Table 2. I/O, Control/Status and Timer Registers

Address	Read	Write	Register Names/Notes
00	PA Data	PA Data	Port A Data I/O
01	PB Data	PB Data	Port B Data I/O
02	PC Data, 0→IBF[3]	PC Data, 1→OBE, 0→RSO[3]	Port C Data I/O
03	PC Data, 0→IBF[3]	PC Data, 1→OBE, 1→RSO[3]	Port C Data I/O
04	PD Data[1]	PD Data[1]	Port D Data I/O
05	—	PE Data[1]	Port E Data Output Only
06	PF Data	PF Data	Port F Data I/O
07	PG Data	—	Port G Data Input Only
08	—	PA Direction	Port A Direction
09	—	PB Direction	Port B Direction
0A	—	PC Direction	Port C Direction
0B	—	PC Direction	Port C Direction
0C	—	PD Direction[1]	Port D Direction
0D	—	—	
0E	—	PF Direction	Port F Direction
0F	—	—	
10	BCR	BCR	Bus Control Register
11	HCSR	HCSR	Host Control and Status Register
12	ICSR	ICSR	Interrupt Control and Status Register
13	—	CIFR	Clear Interrupt Flags Register
14	—	IPCIR	Inter-Processor Communication Interrupt Register
15	PCR	PCR	Power Control Register
16	TACSR	TACSR	Timer A Control and Status Register
17	LCA, UCA→SLA	LLA	Timer A Lower Counter (LCA)/Lower Latch (LLA)
18	SLA	ULA	Timer A Snapshot Latch (SLA)/Upper Latch (ULA)
19	SLA, 0→UFA[2]	ULA, ULA→UCA, LLA→LCA, 0→UFA[2]	Timer A Snapshot Latch (SLA)/Upper Latch, Download and Start Timer
1A	TBCSR	TBCSR	Timer B Control and Status Register
1B	LCB	LLB	Timer B Lower Counter (LCB)/Lower Latch (LLB)
1C	UCB	ULB	Timer B Upper Counter (UCB)/Upper Latch (ULB)
1D	UCB, 0→UFB[2]	ULB, ULB→UCB, LLB→LCB, 0→UFB[2]	Timer B Upper Counter (UCB)/Upper Latch (ULB), Download and Start Timer
1E	—	—	
1F	—	—	

Notes:
1. Addressed externally when in expanded bus mode.
2. Counter/Timer underflow flags:
   UFA = Timer A Underflow Flag bit in TACSR
   UFB = Timer B Underflow Flag bit in TBCSR
3. R65C00/21 to/from Host data transfer bits in HCSR:
   IBF = Input Buffer Full flag bit
   OBE = Output Buffer Empty flag bit
   RSI = Register Select Input bit
   RSO = Register Select Output bit
4. — = Not used—indeterminate data when read

Table 3. Control/Status Registers Formats Summary

Address (Hex)	Bit Number 7	6	5	4	3	2	1	0	
10	CPU A ACTIVE	NOT USED		PAGE ONE EXT	PORT A NIBBLE MODE		BUS EXTENSION MODE		BUS CONTROL REGISTER (BCR)
11	O/P BUFF FULL INT FLAG (OBF)	I/P BUFF FULL INT FLAG (IBF)	I/O REG SEL (RSI) (RSO)	NOT USED	I/OA INT ENBL I/OB INT ENBL	HOST INT ENBL	HOST BUS ENBL	HOST BUS TYPE	HOST CONTROL AND STATUS REGISTER (HCSR)
12	IPCA INT FLAG IPCB INT FLAG	PF2 LOW INT FLAG	PF1 NEG EDGE INT FLAG	PF0 POS EDGE INT FLAG	IPCA INT ENBL IPCB INT ENBL	PF2A INT ENBL IPCB INT ENBL	PF1A INT ENBL PF1B INT ENBL	PF0A INT ENBL PF0B INT ENBL	INTERRUPT CONTROL AND STATUS REGISTER (ICSR)
13	CLR IPCA INT FLAG CLR IPCB INT FLAG	NOT USED	CLR PF1 NEG INT FLAG	CLR PF0 POS INT FLAG	NOT USED				CLEAR INTERRUPT FLAGS REGISTER (CIFR)
14	WRITE ONLY REGISTER—NO SPECIFIC BIT (IPCIR)								INTER-PROCESSOR COMMUNICATION INTERRUPT REGISTER (IPCIR)
15	NOT USED						LOW PWR CPU B (LPB)	LOW PWR CPU A (LPA)	POWER CONTROL REGISTER (PCR)
16	TMR A UNFL FLAG (UFA)	PF3 LEVEL IND	NOT USED	TMR A INT ENBL	TMR A CLK PRESC SEL	TIMER A MODE SELECT			TIMER A CONTROL AND STATUS REGISTER (TACSR)
1A	TMR B UNFL FLAG (UFB)	PF4 LEVEL IND	NOT USED	TMR B INT ENBL	NOT USED		TIMER B MODE SELECT		TIMER B CONTROL AND STATUS REGISTER (TBCSR)

Note: All control and status registers are cleared to zero by $\overline{RES}$

INTERRUPT CONTROL AND STATUS

Unlike other R6500 family devices, the R65C00/21 does not concentrate the interrupt flags into a single register. The R65C00/21, in general, places the interrupt flags in registers which also have to do with the control of the particular function which can cause the interrupt.

Interrupt enable control is located in the following registers:

HCSR Host Control and Status Register
ICSR Interrupt Control and Status Register
TACSR Timer A Control and Status Register
TBCSR Timer B Control and Status Register

Portions of each of these registers relating to interrupt enables are duplicated for each of the two CPU's. However, only one memory address has been allocated so that each CPU uses the same address to select its own interrupt enables. The specific details of the usage of the interrupt control bits are discussed in the corresponding functional area.

CLOCK CIRCUITS

CLOCK OSCILLATOR

The internal clock oscillator generates the system clock (Ø2) which clocks all R65C00/21 operations. The system clock frequency ranges from 10 KHz to 4 MHz (the upper limit determined by the R65C00/21 part number) which is one-half the external crystal (or master clock) frequency. Each CPU in turn operates at one-half the system clock frequency (alternate cycles). All operations to memory or I/O take place at the system clock frequency. Since each CPU shares the common segments of the system on alternate system clock cycles, all internal operations occur at the system clock rate but, for CPU timing purposes, a CPU cycle rate of half the system rate is used. Thus with a 4 MHz crystal frequency, the system clock rate is 2 MHz and each CPU operates at an effective 1 MHz rate. Every two system clock periods sees one cycle devoted to CPU A and one cycle devoted to CPU B.

The Ø2 clock is normally routed externally to clock external memory operations in the extended bus mode. A mask option allows the Ø2 clock to be configured as an input so the R65C00/21 can operate in a slaved clock mode. In this case, the crystal input (XTALI) is grounded and crystal output (XTALO) is left open as shown in Figure 5.

LOW POWER OPERATION

The divide-by-128 clock prescaler operates in one of three ways (see Figure 6). One is the prescaler switched completely out which gives a system clock rate (Ø2) at one-half of the crystal frequency. Another way is to select the low power operation for both CPUs which switches in the clock prescaler. The clock prescaler divides the system clock frequency by 128 to generate the prescaled system clock rate (Ø2PS). This reduces the device power requirements and also reduces the counting rate of both counter/timers by a factor of 128. The third operating mode for the prescaler is to use it for prescaling Timer A only. This mode is discussed under the Counter/Timer Operation.

POWER CONTROL REGISTER (PCR)

Two bits in the Power Control Register (PCR) determine operation of the clock prescaler. Each CPU can set its own power control bit and read both of them. When both power control bits are a 1, the system switches to the low power operation at a clock rate of Ø2/128 (Ø2PS). The system reverts to normal power and speed when either power control bit is a 0 or when an enabled interrupt occurs. In the latter case, the system continues to operate at the low rate until the current instruction is completed, then it switches to the normal rate.

NOTE

An enabled interrupt automatically clears the PCR bit for the affected CPU. It must be set again by software to resume low power mode.

Power Control Register (PCR)

7	6	5	4	3	2	1	0
NOT USED						LOW PWR CPU B (LPB)	LOW PWR CPU A (LPA)

Bits 7-2 **Not Used** (Don't care)

Bit 1 **Low Power Mode Select for CPU B (LPB)**
- 1 Low power mode requested by CPU B
- 0 Normal power mode requested by CPU B

Bit 0 **Low Power Mode Select for CPU A (LPA)**
- 1 Low power mode requested by CPU A
- 0 Normal power mode requested by CPU A

Notes:
1. Both CPU's can read both bits.
2. Each CPU can only write its power control bit.
3. Both bits must be set to enable low power mode.

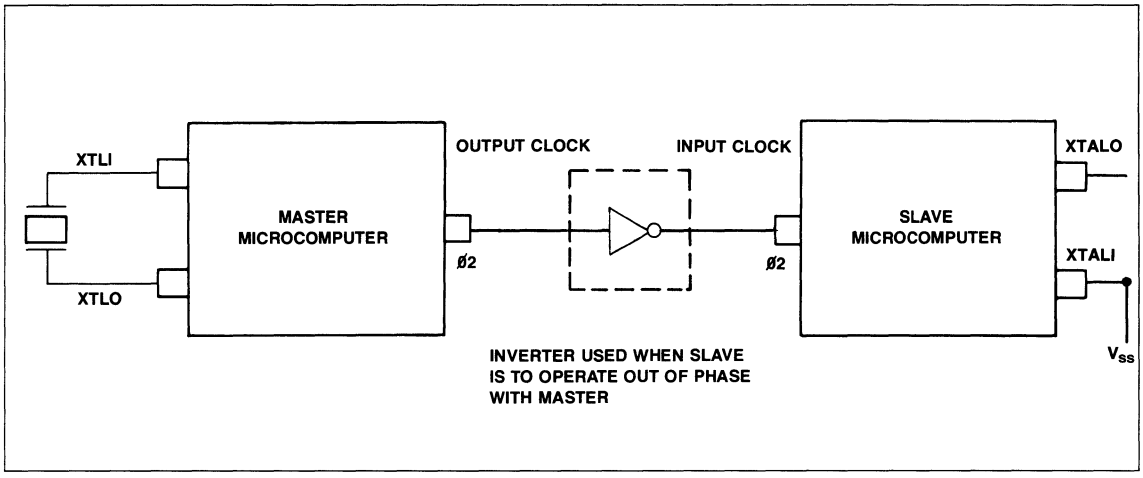
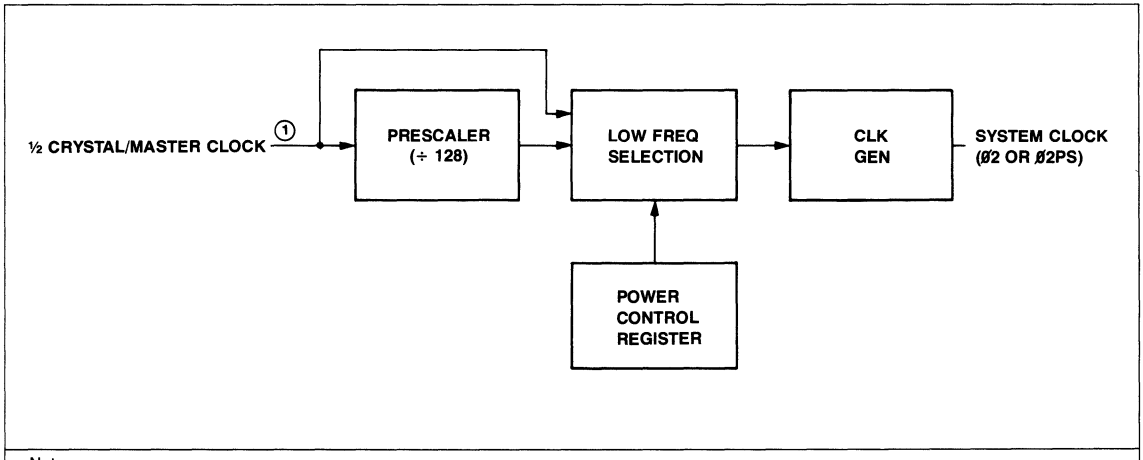


Figure 5. Master/Slave Cock Connection



Notes.
1. Crystal or Master clock frequency is divided by two internally.
2 System clock is Ø2 or Ø2PS (Ø2 – 128) if low frequency operation for both CPU's is selected in the Power Control Register.
3. When a device is strapped for slave clock mode, the input Ø2 by-passes the prescaler (i.e , PCR bits will have no affect on the internal Ø2 clock rate of the slave processor.

Figure 6. System Clock Operation

PARALLEL INPUT/OUTPUT PORTS

The R65C00/21 parallel input/output interface consists of five 8-bit, bidirection input/output ports, one 8-bit output only port, and one 4-bit input only port.

BIDIRECTIONAL PORTS A, B, C, D AND F

The five 8-bit bidirectional ports (Ports A, B, C, D and F) each have an associated data direction register which configures individual data ports for either input or output. Port E is output only and port G is input only, therefore, no data direction registers are required for these two ports.

OUTPUT MODE

If the data direction register for a particular bit position in a bidirectional port is a 1, that bit is defined as an output pin. The information written into each bit position of the data word is loaded into a latch. The information will remain in that latch until new data is transmitted to the data word or the power is shut off. The output latches are individually connected to output drivers for each bit position for which a corresponding bit in the data direction register is a 1. The output drivers are double-ended, push-pull type. The drivers force the output pins high ($\geq$2.4V) if the output data bit is a 1, or low ($\geq$0.4V) if the output data bit is a 0. The output drivers are TTL compatible.

INPUT MODE

If the data direction register for a particular bit position in a bidirectional port is 0, that bit position is defined as an input pin. When the input/output port is read via an LDA, LDX, LDY, ADC, SBC, ORA, AND, EOR, or a BIT instruction, all of the information on that port's pins are read into the corresponding register and processed as directed by the instruction. Since the input signal lines are at a "float" state, the logic level on them will be read as either a 1 or a 0 for that pin position. A low ($\geq$0.8V) input causes a logic 0 to be read and a high ($\geq$2.0V) input causes a logic 1 to be read. The output values can also be read (if the direction bit = 1) since the outputs are also on the pins. The input receivers are TTL compatible, are not latched, and are sampled near the end of each clock cycle ϕ2 and gated onto the internal bus when selected.

PORT A NIBBLE ADDRESSING

Whenever a port is shared as an output, care must be exercised that one CPU does not destroy the other CPU's output data. In general, this can be avoided by allocating complete output ports to each CPU so that there is no possibility of conflict. However, there may be some situations where at least one port must be shared for outputs to get the proper mix for the required application. Port A is slightly different from the other bidirectional ports to allow port A to be safely shared as an output port by both CPU's.

Port A is divided into two 4-bit "nibble ports". Each half (nibble) of Port A may be independently addressed by each CPU as defined by two bits in the Bus Control Register (BCR2 and BCR3) as described in Bus Extension and Host Interface section. Depending upon the control bits, either CPU may be assigned to write to both halves, write to neither half (only read—the other CPU writes to the whole register), write to top half, or write to bottom half. When a mode has been selected for writing to only one-half of the port, the other half is unaffected.

ALTERNATIVE MODES OF OPERATION

Bidirectional Ports C, D, and F all have alternative modes of operation which may be selected in lieu of the bidirectional port capabilities.

Port C is a data bus for a host computer when the R65C00/21 is being used as a programmable peripheral device. This is discussed in more detail under Bus Extension and Host Interface.

Port D is a multiplexed data bus (D0 through D7) and address bus (A0 through A7) when the R65C00/21 is used as a microcomputer with external memory and I/O devices. This is also detailed under Bus Extension and Host Interface.

Port F also has the capability of operating in conjunction with other segments of the R65C00/21 architecture as described below.

PORT F CONTROL AND STATUS

The Interrupt Control and Status Register (ICSR) and the Clear Interrupt Flags Register (CIFR) control and monitor the operation of the Port F external interrupts (bits 2, 1, 0) as well as interprocessor communication interrupts.

When the PF0 edge-sensitive circuit detects a positive transition, bit 4 of the ICSR is set to a 1. An internal interrupt request ($\overline{IRQ}$) is generated to a CPU whenever this bit is set and the corresponding PF0 Interrupt Enable Flag (ICSR bit 0) is set to a 1 for that CPU. Similarly, a negative going transition on PF1 sets the edge detect flag in ICR bit 5. ICSR bit 1 is the corresponding PF1 Interrupt Enable bit. As in all cases of the interrupt enable bits, each CPU has its own set, addressed at the same location, but held separately.

Port F signal PF2 has an external interrupt request ($\overline{IRQ}$) capability. When this signal goes low, bit 6 of the Interrupt Control and Status Register is set and remains set as long as the signal is low. If the corresponding PF2 Interrupt Enable bit (bit 2) in its segment of the Interrupt Control and Status Register is a 1 while the PF2 Low Interrupt bit (bit 6) is a 1, an interrupt request is generated.

Each CPU may thus control the external interrupt independently of the internal interrupts. If the I flag in the Processor Status Register of a particular CPU is a 1, no $\overline{IRQ}$'s will be honored. If the I flag is a 0 and that CPU's interrupt enable in bit 2 of the Interrupt Control and Status Register is a 0, only internal interrupts will interrupt that CPU. If bit 2 is a 1, any $\overline{IRQ}$ will be honored.

The Port F signals PF3 and PF4 can be used as external interfaces for Counter/Timers A and B, respectively (refer to the Counter/Timers description). Finally, PF7 can be used as an active-low interrupt to a host processor. The operation of the R65C00/21 with a host processor is discussed under Bus Extension mode.

The Inter-Processor Communication Interrupt (IPCA and IPCB) bit in the ICSR allows each CPU to interrupt the other CPU if all of the other normal IRQ conditions are correct. CPU A sets the IPCB Interrupt Flag in CPU B's Interrupt Control and Status Register and CPU B sets the IPCA Interrupt Flag in CPU A by any write to location 0014, the Inter-Processor communications Interrupt Register. This is not an actual register, but writing any value here sets the other CPU IPCI flag. This inter-processor communications is illustrated in Figure 7.

Interrupt Control And Status Register (ICSR)

7	6	5	4	3	2	1	0
IPCA INT FLAG	PF2 LOW INT FLAG	PF1 NEG EDGE INT FLAG	PF0 POS EDGE INT FLAG	IPCA INT ENBL	PF2A INT ENBL	PF1A INT ENBL	PF0A INT ENBL
IPCB INT FLAG				IPCB INT ENBL	PF2B INT ENBL	PF1B INT ENBL	PF0B INT ENBL

Bit 7 **Inter-Processor Communication (IPC) Interrupt Flag (A or B)**
- 1 An inter-processor interrupt is requested by the other CPU
- 0 No internal interrupt is requested

Bit 6 **PF2 Low Interrupt Flag (A and B)**
- 1 PF2 is low
- 0 PF2 is high

Bit 5 **PF1 Negative Edge Detect Interrupt Flag**
- 1 A positive-to-negative transition on PF1 occurred
- 0 No positive-to-negative transition on PF1 occurred

Bit 4 **PF0 Positive Edge Detect Interrupt Flag**
- 1 A positive-to-negative transition on PF0 occurred
- 0 No positive-to-negative transition on PF0 occurred

Bit 3 **Inter-Processor Communication Interrupt Enable (A or B)**
- 1 Enables inter-processor communication interrupt (bit 7)
- 0 Disables inter-processor communication interrupt (bit 7)

Bit 2 **PF2 Interrupt Enable (A or B)**
- 1 Enables PF2 interrupt (bit 6)
- 0 Disables PF2 interrupt (bit 6)

Bit 1 **PF1 Interrupt Enable (A or B)**
- 1 Enables PF1 interrupt (bit 5)
- 0 Disables PF1 interrupt (bit 5)

Bit 0 **PF0 Interrupt Enable (A or B)**
- 1 Enables PF0 interrupt (bit 4)
- 0 Disables PF0 interrupt (bit 4)

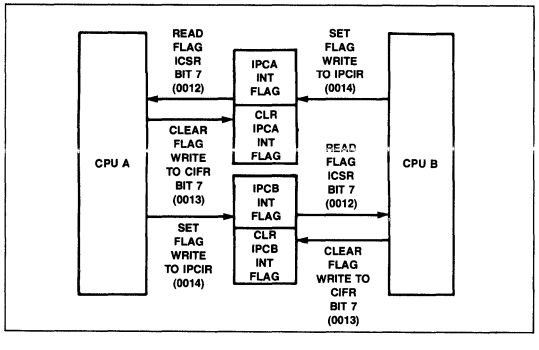


Figure 7. Inter Processor Communication

CLEAR INTERRUPT FLAGS REGISTER (CIFR)

The Clear Interrupt Flags Register (CIFR) is similar to the ICSR in that only one address is used but the bit pattern operates only on the status bits for its own processor. Thus only CPU A may clear IPCA but either may clear the edge detection flag bits. Bit 6 will only be cleared when the signal on PF2 goes high. Actually, the Clear Interrupt Flags Register is not a register at all, but addressing a bit pattern to this location performs the function. Any bit to which a zero is written will clear the corresponding interrupt flag. A read of this word returns logic one's so that the new Reset Memory Bit instructions may be used to clear these flags.

Clear Interrupt Flags Register (CIFR)

7	6	5	4	3	2	1	0
CLR IPCA INT FLAG	NOT USED	CLR PF1 NEG INT FLAG	CLR PF0 POS INT FLAG	NOT USED			
CLR IPCB INT FLAG							

Bit 7 **Clear Inter-Processing Communication Interrupt Flag**
- 1 Has no effect on the IPC Flag
- 0 Clears the IPC Interrupt Flag (specific CPU, A or B)

Bit 6 **Not Used**

Bit 5 **Clear PF1 Interrupt Flag**
- 1 Has no effect on the PF1 Interrupt Flag
- 0 Clears the PF1 Interrupt Flag (either CPU)

Bit 4 **Clear PF0 Interrupt Flag**
- 1 Has no effect on the PFO Interrupt Flag
- 0 Clears the PF0 Interrupt Flag (either CPU)

Bit 3-0 **Not Used**

OUTPUT ONLY PORT E

The output characteristics of Port E are identical to that of the bidirectional ports. The main difference is that there is no data direction register and also no capability of reading the information being output. Attempting to read Port E loads indeterminate data onto the internal bus.

Port E is a dual function port which, in addition to being an output port, can also serve as address bits A15 through A8 when the R65C00/21 is addressing external memory and I/O devices. This is discussed in more detail under Bus Extension and Host Interface.

INPUT ONLY PORT G

The input characteristics of the 4-bit Port G are the same as a bidirectional port in an input mode. The difference is that only four bits are input into the least significant bits of the data register and the most significant bits are loaded as zeros.

COUNTER/TIMERS

There are two separate 16-bit counter/timer systems in the R65C00/21: Counter/Timer A and Counter/Timer B. The block diagram of the counter/timers (also referred to as the timers, the counters, Timer A, or Timer B) is shown in Figure 8. Timer A has eight operating modes and five registers while Timer B has four operating modes and four registers. Both counter/timers have a 16-bit counter comprised of two 8-bit segments: Lower Counter (LCA and LCB, where A and B refer to Counter/Timer A and B) and Upper Counter (UCA and UCB). Both counter/timers also have a 16-bit latch section consisting of two 8-bit segments: Lower Latch (LLA and LLB) and Upper Latch (ULA and ULB). In addition, only Timer A has an 8-bit Snapshot Latch (SLA) register.

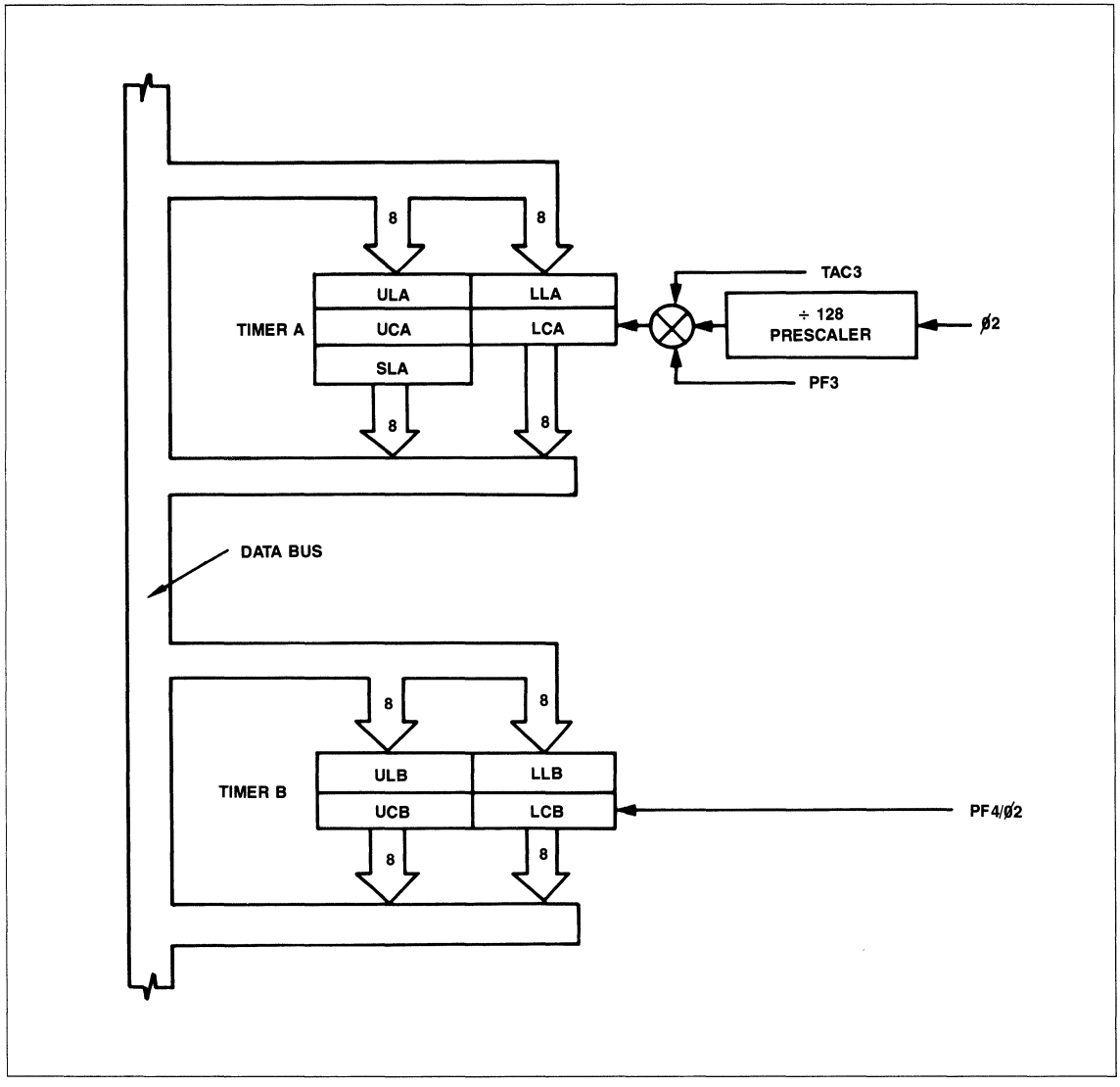


Figure 8. Counter/Timer Block Diagram

Data are written to the latches which act as holding registers for loading or reloading the initial counter/timer values upon mode initiation or counter/timer restart.

Both timers count down from the pre-set latch value and set an appropriate underflow flag when the counter counts through zero. The counter actually never counts below zero. At the time the counter would go negative, the contents of the latches replace the count value with no time delay.

Each counter/timer has three addresses for accessing the five (Counter/Timer A) or four (Counter/Timer B) 8-bit registers in its system. Consequently, the R/$\overline{W}$ line also aids in addressing the registers. Reading or writing to specific registers may also have other effects such as clearing an interrupt flag or transferring latch data to the counter. Consult the input/output and control register memory map in Table 2 for the effects of reading or writing to specific registers in the two counter/timer systems.

Each counter/timer has operating modes which are clocked either at the system clock rate (Ø2) or an external event clock rate. In addition, Timer A can operate with a prescaled Ø2/128 clock rate.

COUNTER/TIMER A (TA)

Counter/Timer A, with its four additional modes and Snapshot Latch, is generally more flexible than Counter/Timer B.

The Snapshot Latch (SLA) solves a problem which sometimes occurs when a timer is read. The problem is that between the time when the low byte of the 16-bit counter is read and the time when the high byte is read it is possible for the high byte to have been decremented. The resulting 16-bit value would, in this case be incorrect. In many modes of timer, the values are not actually read but the zero count transition is important. These types of applications do not require the use of the Snapshot Latch register. If the timer count value is to be used directly from a running timer, however, the Timer A Snapshot Latch should be used.

Timer A overcomes the problem stated above by sampling the value of the upper counter byte into the Snapshot Latch every time the lower counter byte is read. The value of the Upper Counter can be obtained by first reading the Lower Counter at address 0017, then reading the Snapshot Latch at address 0018 or 0019. Note that reading address 0019 also resets the Timer A Underflow (UFA) flag.

A second architectural difference between the two timers is that Timer A can have its clock input scaled down by a factor of 128 during normal power operation. This allows Timer A to measure longer periods of time internally while the microcomputer in operating at the Ø2 system clock rate. With a 4 MHz system clock, more than two second time intervals (up to 2.097 seconds) can be measured directly without any software intervention. Without the prescaler, 16.384 ms is the longest time interval at 4 MHz.

Timer A Mode Control

The operation of Timer A is controlled and monitored by the Timer A Control and Status Register (TACRS).

Bits 0-2 select the Timer A mode of operation.

Bit 3, when set to a 1, causes the clock prescaler to be switched into the circuit so that the timer may count longer intervals in modes which allow it.

Timer A Interrupt Enable, TACSR bit 4, if set to a 1 by a CPU, enables generation of an internal $\overline{IRQ}$ to that CPU when the UFA flag is set.

Bit 6 copies bit 3 of Port F (PF3).

Bit 7 is the UFA bit which indicates that Timer A has counted down through zero. This may be detected by reading the bit or may be used to cause an $\overline{IRQ}$ interrupt if bit 4 of the TACSR is set to a 1. The UFA flag is reset to a 0 by reading SLA or writing ULA at address 0019.

Timer A Control And Status Register (TACSR)

7	6	5	4	3	2	1	0
TMR A UNFL FLAG (UFA)	PF3 LEVEL IND	NOT USED	TMR A INT ENBL	TMR A CLK PRESC SEL	TIMER A MODE SELECT		

Bit 7 **Timer A Underflow Flag (UFA)**
- 1 Underflow condition occurred
- 0 No underflow

Bit 6 **Port F Bit 3 (PF3) Level**
- 1 PF3 High
- 0 PF3 Low

Bit 5 **Not Used** (Don't care)

Bit 4 **Timer A Interrupt Enable**
- 1 Enable Timer A Interrupt
- 0 Disable Timer A Interrupt

Bit 3 **Timer A Clock Prescaler Enable**[1]
- 1 Enable Clock Prescaler (Ø2/128)
- 0 Disable Clock Prescaler (Ø2)

Bits 2 to 0 **Timer A Mode Select (TAMS)**

2	1	0	
0	0	0	Timer A Off
0	0	1	Free-Run Event Counter Mode[1]
0	1	0	Free-Run Pulse Width Measurement Mode[1]
0	1	1	Retriggerable One-Shot Timer Mode[1]
1	0	0	One-Shot Interval Timer Mode
1	0	1	Free-Run Interval Timer Mode
1	1	0	One-Shot Pulse Generation Mode
1	1	1	Free-Run Pulse Generation Mode

Note:
1. Prescaler must be disabled (bit 3=0) for Free-Run Event Counter Mode, Free-Run Pulse Width Measurement Mode, and Retriggerable One-Shot Timer Mode. These three modes do not allow prescaling.

Timer A Operating Modes

The Timer A mode of operation is selected by setting bits 0-2 of the Timer A Control and Status Register (TACSR) to the appropriate code.

Timer A Off, Mode 0

Timer A is turned off in this mode. The Timer A Underflow Flag (UFA) stays at its current state. The counter holds its current value and may be read. Writing to the registers performs the usual functions associated with that address but the counter remains stopped. This is the default condition.

Timer A Free-Run Event Counter, Mode 1

The Timer A Upper Counter (UCA) and Lower Counter (LCA) is loaded with the Timer A Upper Latch (ULA) and Lower Latch (LLA) value when the data is written to the Timer A Upper Latch at address 0019. Timer A then decrements by 1 at each negative transition of the signal on input Port PF3. (The Port F data direction register must have a 0 in bit 3.) The Timer A Underflow Flag (UFA) is set to 1 when the counter decrements below zero. At this same time, the latch value is reloaded into UCA and LCA. The maximum rate of the signal on PF3 which may be detected is one-half of the Ø2 system clock rate.

Timer A Free-Run Pulse Width Measurement, Mode 2

Writing to ULA at 0019 transfers the 16-bit latch to the counter which operates as a timer in this mode. The initial value in the timer is decremented at the Ø2 rate when the PF3 signal is low. Otherwise, the counter holds its value. Counting stops when the PF3 signal goes high and will resume if the signal goes low again. If the counter counts below zero, the counter initial value is reloaded from the latches and the UFA flag is set.

Timer A One-Shot Retriggerable Timer, Mode 3

This mode is similar to Mode 4 except that the timer restarts each time PF3 goes through a high-to-low transition and counts down until the counter goes through zero. A second difference is that the clock prescaler may not be used with this mode. The data direction register bit 3 (PF3) must be zero to select input.

Timer A One-Shot Interval Timer, Mode 4

Writing to ULA at 0019 transfers the initial value from the latches and starts the timer. The timer counts at either the Ø2, or scaled Ø2 (Ø2/128), rate. When the counter counts through zero, the latch value is transferred to the counter, the UFA flag is set and the counter stops counting.

Timer A Free-Run Interval Timer, Mode 5

Writing ULA at 0019 transfers the 16-bit latch value to the timer and starts it running. The counter counts down at either the Ø2, or the scaled Ø2 (Ø2/128), rate. When the counter counts through zero the UFA flag is set, the value in the latches is transferred to the counter, and the counter continues to count down.

Timer A One-Shot Pulse Generation, Mode 6

The PF3 data direction register bit must be set to a 1 before starting this mode to initially force a high output. Writing ULA at 0019 starts the timer and clears the PF3 data output bit to a 0 causing a low output. The PF3 output remains low until the timer counts through zero. At this time, the PF3 output goes high until the mode is restarted or a new mode is selected. The UFA flag is also set at this time and the counter is stopped. The timer counts at either the Ø2, or the scaled Ø2 (Ø2/128), rate.

Timer A Free-Run Pulse Generation, Mode 7

The data direction register for PF3 must be set to a 1 to select the PF3 output before starting this mode. Writing to ULA at 0019 sets PF3 to 0 forcing a low output and starts the timer. Each time the timer counts through zero, the PF3 output changes state to generate a square wave at a rate dependent upon the latch value. The timer counts at either Ø2, or the scaled Ø2 (Ø2/128), rate. Each time the counter counts through zero, the latch contents are automatically transferred to the timer registers and the UFA flag is set.

COUNTER/TIMER B (TB)

Timer B is a simpler timer than Timer A but it still retains great flexibility. Unlike Timer A, there is no "off" mode (the default mode is the Free-Run Interval Timer Mode) and there is no separate selectable clock prescaler. All counting (except for counting external events) is done either at the Ø2 clock rate or Ø2/128 rate (when low power mode is selected). Another difference is that Timer B does not have the snapshot latch register for freezing the upper timer byte for reading. However, in its normal modes the counter counts through zero to set the Underflow Flag B (UFB) so that a snapshot latch register is not required.

Timer B Mode Control

The operation of Timer B is controlled and monitored by the Timer B Control and Status Register (TBCSR).

Bits 0-1 select the Timer B operating mode.

Timer B Interrupt Enable, bit 4, when set to a 1 by a CPU, enables generation of an internal interrupt request ($\overline{IRQ}$) to that CPU when the UFB flag is set.

Bit 6 of the TBCSR copies bit 4 of Port F (PF4).

Bit 7 in the TBCSR is the UFB bit which indicates that Timer B has counted down through zero. This may be detected by reading the bit or may be used to cause an $\overline{IRQ}$ interrupt if bit 4 of the TBCSR is set to a 1. The UFB bit is reset by either reading UCB or writing to ULB at address 001D.

Timer B Control and Status Register (TBCSR)

7	6	5	4	3	2	1	0
TMR B UNFL FLAG (UFB)	PF4 LEVEL IND	NOT USED	TMR B INT ENBL	NOT USED		TIMER B MODE SELECT	

Bit 7	**Timer B Underflow Flag (UFB)**
1	Underflow condition occurred
0	No underflow
Bit 6	**Port F Bit 4 (PF4) Level Indicator**
1	PF4 High
0	PF4 Low
Bit 5	**Not Used** (Don't care)
Bit 4	**Timer B Interrupt Enable**
1	Enable Timer B Interrupt
0	Disable Timer B Interrupt
Bits 3-2	**Not Used** (Don't care)

Bits 1-0		**Timer B Mode Select (TMS)**
1	0	
0	0	Free-Run Interval Timer Mode
0	1	Free-Run Pulse Generator Mode
1	0	Event Counter Mode
1	1	Pulse Width Measurement Mode

Timer B Operating Modes

The Timer B operating mode is selected by setting bits 0 and 1 in the TBCSR to the appropriate code.

Timer B Free-Run Interval Timer, Mode 0

Writing to Timer B Upper Latch (ULB) at 001D transfers the 16-bit latch value to the timer and starts it running. The counter counts down at the Ø2 rate. When the counter counts through zero, the Timer B Underflow Flag (UFB) is set to a 1, the value in the latches is transferred to the counter and the counter continues to count down.

Timer B Free-Run Pulse Generation, Mode 1

The data direction register for PF4 must be set to a 1 to select PF4 output before starting this mode. Writing to ULB at 001D sets PF4 to 0 to force the PF4 output low and starts the timer. Each time the timer counts through zero, the PF4 output changes state to generate a square wave at a rate dependent upon the initial value loaded into the latches. The timer counts at the Ø2 rate. Each time the counter counts through zero, the latch values are automatically transferred to the timer registers and the UFB flag is set to a 1.

Timer B Event Counter, Mode 2

The data direction register bit for PF4 must be set to a 0 to select PF4 input prior to selecting this mode. The counter is loaded with the latch value when the ULB data is written to address 001D. Timer B then decrements by 1 at each negative transition on input Port PF4. The Timer B Underflow Flag (UFB) is set to a 1, when Counter B counts through zero. At this same time, the latch value is reloaded into Timer B. The maximum rate of the signal on PF4 which may be detected is one-half of the Ø2 clock rate.

Timer B Pulse Width Measurement, Mode 3

Writing to ULB at 001D transfers the 16-bit latch value to the counter. The initial value in the timer is decremented at the Ø2 rate when the PF4 signal is low. Each time the PF4 signal goes high, the counter stops and then continues when the signal is low again. If the counter counts through zero, the UFB flag is set to 1 and the latch value transfers to reinitialize the counter and the countdown continues as long as PF4 is low.

BUS EXTENSION

In addition to its application as a single-chip microcomputer, the bus extension mode allows the R65C00/21 to operate as a microprocessor with external memory and I/0.

BUS EXTENSION MODE

When the R65C00/21 is used as a single-chip microcomputer, all of the output ports may be used as input or output ports. However, to use the R65C00/21 with external ROM, RAM, or I/O, a number of the ports act as extensions of the internal address and data buses. Specifically, Port D becomes dedicated as a multiplexed 8-bit data and address bus. Port D provides both the data bus (D0 through D7) and the low bits of the address (A0 through A7) on pins PD0 through PD7. When a bus extension mode is selected, the Port D Data Direction Register must be cleared to zero (its default condition) to configure Port D as all inputs. The R65C00/21 then controls Port D as an extension of the internal bus structure and provides an active-low External Memory Select ($\overline{EMS}$) strobe signal at the time the address bits are available. The $\overline{EMS}$ signal is present even when Port D is being used as a normal input/output register.

The R65C00/21 has the option of using 8-, 12- or 16-bit address bus extensions. Selection of the bus extension mode is controlled by bits 0 and 1 of the Bus Control Register (BCR). When the 8-bit mode is selected, only the Port D multiplexed address/data bus function is required. However, if either the 12- or 16-bit address bus extension is selected, either one half or all of output Port E also becomes dedicated to the bus extension function. If a 16-bit bus extension is selected, then all of Port E becomes the upper address bits A8 through A15 on pins PE0 through PE7, respectively. If the 12-bit bus extension is selected, then the address lines A8 through A11 appear on PE0 through PE3. In this case, PE4 through PE7 have their usual output function.

Since Port D is multiplexed, it is necessary that external latches be supplied to hold the lower eight bits of the address bus. The EMS output is low when the address is being supplied from Port D. All of the other necessary control bus signals are also provided; these include Ø2 and R/$\overline{W}$. The SYNC and ØA signals are also brought out for use by development systems and bus analyzers for system debugging.

In a one-chip configuration, the 128 bytes of internal page one RAM (address 0180 through 01FF), is logically combined with page (0080-00FF). However, when an extended bus is used, the stack page may be addressed in its normal range in external memory (0100-01FF). When bit 4 of the Bus Control Register is a 0, page one is internal and shared with page zero; when it is a 1, page one is external allowing full 256 bytes available to the two stacks.

Figure 9 is an overall block diagram of a system using the R65C00/21 in the bus extension mode.

The CPU A Active signal (bit 7 of the BCR) is high when CPU A is controlling the system bus, and low when CPU B is active. This bit copies the state of the ØA output signal. Consequently, the bit may be sampled in common subroutines to determine the calling CPU, or for bank selection purposes. Thus, CPU A and CPU B may have some external memory or I/O dedicated to their exclusive use. Each may separately address as much as 59.5K bytes of external memory map, or external memory may be shared.

Bus Control Register (BCR)

7	6	5	4	3	2	1	0
CPU A ACTIVE	NOT USED		PAGE ONE EXT	PORT A NIBBLE MODE		BUS EXTENSION MODE	

Bit 7 — **CPU A Active**
- 1 — CPU A active
- 0 — CPU B active

Bits 6-5 — **Not Used (Don't Care)**

Bit 4 — **Page One External/Internal Mapping**
- 1 — Page One External
- 0 — Page One Internal

Bits 3-2 — **Port A Write Nibble Control***

3	2	
0	0	CPU A writes to both halves (PAO-PA7).
0	1	CPU A writes to upper half (PA4-PA7); CPU B writes to lower half (PA0-PA3).
1	0	CPU A writes to lower half (PA0-PA3); CPU B writes to upper half (PA04-PA7).
1	1	CPU B writes to both halves (PA0-PA7).

Bits 1-0 — **Bus Extension Mode**

1	0	
0	0	Bus Extension Mode not selected.
0	1	8-bit Address Extension Mode. Range equals 256.
1	0	12-bit Address Extension Mode. Range equals 4096.
1	1	16-bit Address Extension Mode. Range equals 65,536.

Note:
*Either CPU may read the full port at any time.

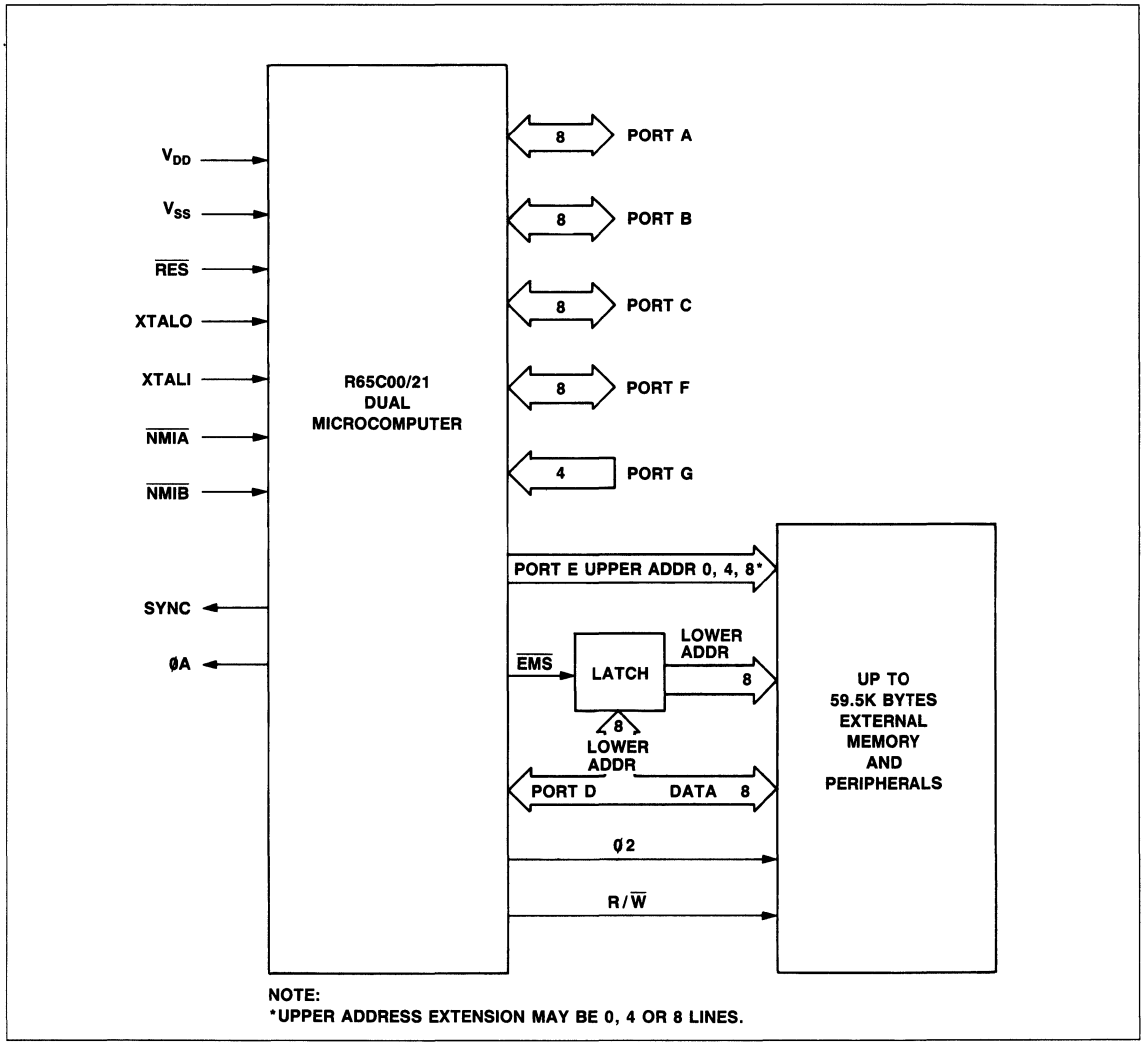


Figure 9. Bus Extension Mode Block Diagram

PROGRAMMABLE PERIPHERAL TO A HOST MODE

An overall block diagram of a system using an R65C00/21 as an intelligent controller is shown in Figure 10.

In this configuration, three of the R65C00/21 input/output ports have special significance. Port C becomes the interface with the host data bus (Port C's Data Direction Register must specify as the input; i.e., all zeros). Pin PF7 becomes an active-low Host Interrupt ($\overline{HINT}$) line, and the 4-bit input Port G becomes the control pins interface to the Host computer.

The R65C00/21 is configured to operate as a peripheral for either the R6500 or 6800 families, or the Z80 or 8080 families. When operating in the 6500/6800 mode, PG0 is an input for the host Ø2 (HØ2) and PG1 is the input for the host R/$\overline{W}$ (HRW) control lines.

When operating in the Z80/8080 mode, PG0 accepts the host $\overline{RD}$ ($\overline{HRD}$) control and PG1 provides the host $\overline{WR}$ ($\overline{HWR}$) control.

In both cases, PG2 serves as a register select (HRS) and PG3 acts as an active-low chip select ($\overline{CS}$) from the host. HRS is used in conjunction with the $\overline{CS}$ and $\overline{HWR}$ to control reading or writing of data or status information as shown in Table 4.

Control of the host mode options is provided by the Host Control and Status Register (HCSR).

When the host writes a byte into the Input Buffer (Port C), the Input Buffer Full (IBF) flag is set to a 1. Similarly, when a byte is read from the Output Buffer (Port C) by the host, the Output Buffer Full (OBF) flag is cleared to a 0. Setting bit 3 of the HCSR enables generation of an internal interrupt request (IRQ) when either the IBF flag is a 1 or the OBF flag is a 0. This logic is duplicated for both CPU's.

Setting bit 2 of the HCSR to a 1 enables generation of any interrupt signal to the host computer. In this case, bit 7 of Port F is pulled low by either a write to Port C (Output Buffer) or a read from Port C (Input Buffer), by either of the R65C00/21 CPU's.

Bit 5 of the HCSR is actually two different bits representing Register Select Input (RSI) and Register Select Output (RSO). The R65C00/21 writes bit RSO and reads bit RSI, while the host writes RSI and reads RSO. The R65C00/21 writes a 0 to this bit when Port C is addressed at 0002 and a 1 when Port C is addressed at 0003. When the host writes to the R65C00/21 through Port C, the level of the HRS input is copied into the RSI bit. This bit allows the communications between the host system and the R65C00/21 to flag the type of data being transferred so that command information may be distinguished from data.

Table 4. Register Select Control

$\overline{CS}$ (PG3)	HRS (PG2)	HRW (PG1)	HØ2 (PG0)	Host Function (6500/6800 Mode)
H	—	—	—	Host Interface Deselected
L	L	L	H	Write Input Buffer, HCSR5 RSI cleared, set IBF
L	L	H	H	Read Output Buffer, Clear OBF
L	H	L	H	Write Input Buffer, HCSR5 RS1 set, set IBF
L	H	H	H	Read upper 3 bits of HCSR; OBF, IBF & RSO
$\overline{CS}$ (PG3)	**HRS (PG2)**	**$\overline{HWR}$ (PG1)**	**$\overline{HRD}$ (PG0)**	**Host Function (8080/Z80 Mode)**
H	—	—	—	Deselected
L	L	L	H	Write Input Buffer, HCSR5 RSI cleared, set IBF
L	L	H	L	Read Output Buffer, Clear OBF
L	H	L	H	Write Input Buffer, HCSR5 RS1 set, set IBF
L	H	H	L	Read upper 3 bits of HCSR; OBF, IBF & RSO

Host Control and Status Register (HCSR)

7	6	5	4	3	2	1	0
O/P BUFF FULL INT FLAG (OBE)	I/O BUFF FULL INT FLAG (IBF)	I/O REG SEL (RSI) (RSO)	NOT USED	I/OA INT ENBL I/OB INT ENBL	HOST INT ENBL	HOST BUS ENBL	HOST BUS TYPE

Bit 7 **Output Buffer Empty (OBE) Flag**
- 1 Output Buffer Full
- 0 Output Buffer Empty

Bit 6 **Input Buffer Full (IBF) Flag**
- 1 Input Buffer Full
- 0 Input Buffer Empty

Bit 5 **Register Select**
- — Distinguishes commands from data. Host reads RSO and R65C00/21 reads RSI. Selection of 1 or 0 to represent commands or data is user defined.

Bit 4 **Not Used.** (Don't care)

Bit 3 **Input/Output Buffer Interrupt Enable**
- 1 Enable IRQ IBF = 1)
- 0 Disable IRQ

Bit 2 **Host Interrupt ($\overline{HINT}$) Output Enable**
- 1 Disable $\overline{HINT}$ Output to Host
- 0 Enable $\overline{HINT}$ Output to Host (OBF = 1)

Bit 1 **Host Bus Enable**
- 1 Disable Host Bus
- 0 Enable Host Bus

Bit 0 **Host Bus Type**
- 1 Host Bus is Z80/8080
- 0 Host Bus is 6500/6800

Note:
Register is cleared to all zeros by $\overline{RES}$.

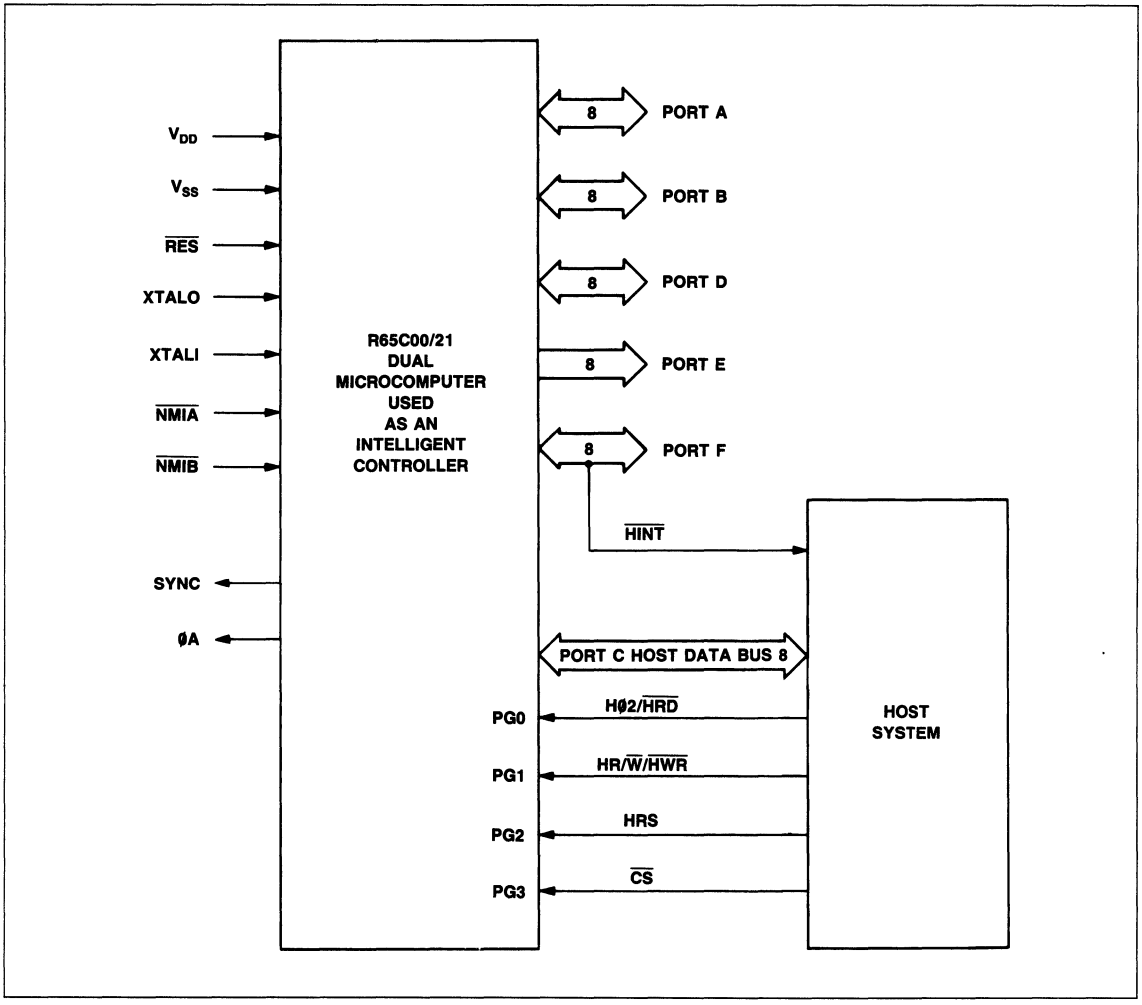


Figure 10. Host Mode Block Diagam

EMULATION MODE

The R65C00/21 can operate in an emulation mode under external signal control.

Emulation mode deselects the internal ROM and enables the 16-bit Expanded Bus mode, independent of the bus mode programmed in the Bus Control Register. Since the Expanded Bus mode uses peripheral Ports D and E, provision is made for these to be emulated in external hardware. This is accomplished by forcing all memory references to Ports D and E to be External Bus cycles. Accesses to the Data Direction Register for Port D are also forced external.

To further aid program development in emulation mode, all bus cycles which perform a memory or I/O write operation, whether the true destination is internal or external, will assert the External Memory Strobe ($\overline{EMS}$) signal. This allows a copy of internal register and memory values to be kept in external memory.

Emulation mode is selected by applying the Ø2 output clock signal to the $\overline{RES}$ input pin.

INSTRUCTION SET IN ALPHABETIC SEQUENCE

The following table contains a summary of the R65C00/21 and R65C29 CPU instruction set. For detailed information, consult the R6502 Microcomputer System Programming Manual, Order No. 202.

The instructions notated with a * are added instructions for the R65C00/21 and R65C29 which are not part of the standard 6502 instruction set.

Instruction Set in Alphabetic Sequence

Mnemonic	Description	Mnemonic	Description
ADC	Add Memory to Accumulator with Carry	LDA	Load Accumulator with Memory
AND	"AND" Memory with Accumulator	LDX	Load Index X with Memory
ASL	Shift Left One Bit (Memory or Accumulator)	LDY	Load Index Y with Memory
		LSR	Shift One Bit Right (Memory or Accumulator)
*BRA	Branch Always		
*BBR	Branch on Bit Reset Relative	*MUL	Multiply
*BBS	Branch on Bit Set Relative		
BCC	Branch on Carry Clear	NOP	No Operation
BCS	Branch on Carry Set		
BEQ	Branch on Result Zero	ORA	"OR" Memory with Accumulator
BIT	Test Bits in Memory with Accumulator		
BMI	Branch on Result Minus	PHA	Push Accumulator or Stack
BNE	Branch on Result not Zero	PHP	Push Processor Status on Stack
BPL	Branch on Result Plus	*PHX	Push Index X
BRK	Force Break	*PHY	Push Index Y
BVC	Branch on Overflow Clear	PLA	Pull Accumulator from Stack
BVS	Branch on Overflow Set	PLP	Pull Processor Status from Stack
		*PLX	Pull Index X
CLC	Clear Carry Flag	*PLY	Pull Index Y
CLD	Clear Decimal Mode		
CLI	Clear Interrupt Disable Bit	*RMB	Reset Memory Bit
CLV	Clear Overflow Flag	ROL	Rotate One Bit Left (Memory or Accumulator)
CMP	Compare Memory and Accumulator	ROR	Rotate One Bit Right (Memory or Accumulator)
CPX	Compare Memory and Index X	RTI	Return from Interrupt
CPY	Compare Memory and Index Y	RTS	Return from Subroutine
DEC	Decrement Memory by One	SBC	Subtract Memory from Accumulator with Borrow
DEX	Decrement Index X by One	SEC	Set Carry Flag
DEY	Decrement Index Y by One	SED	Set Decimal Mode
		SEI	Set Interrupt Disable Status
EOR	"Exclusive-Or" Memory with Accumulator	*SMB	Set Memory Bit
		STA	Store Accumulator in Memory
INC	Increment Memory by One	STX	Store Index X in Memory
INX	Increment Index X by One	STY	Store Index Y in Memory
INY	Increment Index Y by One		
		TAX	Transfer Accumulator to Index X
JMP	Jump to New Location	TAY	Transfer Accumulator to Index Y
JSR	Jump to New Location Saving Return Address	TSX	Transfer Stack Pointer to Index X
		TXA	Transfer Index X to Accumulator
		TXS	Transfer Index X to Stack Register
		TYA	Transfer Index Y to Accumulator

INSTRUCTION SET SUMMARY

MNEMONIC	OPERATION	IMMEDIATE			ABSOLUTE			ZERO PAGE			ACCUM.			IMPLIED			(IND, X)			(IND), Y			Z PAGE, X			ABS, X			ABS, Y			RELATIVE			INDIRECT			Z PAGE, Y			BIT ADDRESSING (OP BY BIT #)								PROCESSOR STATUS CODES							
		OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	ø	1	2	3	4	5	6	7	7 6	5	4	3	2	1	ø
ADC	A+M+C→A (4) (1)	69	2	2	6D	4	3	65	3	2							61	6	2	71	5	2	75	4	2	7D	4	3	79	4	3																		N	V	·	·	·	·	Z	C
AND	A M→A (1)	29	2	2	2D	4	3	25	3	2							21	6	2	31	5	2	35	4	2	3D	4	3	39	4	3																		N	·	·	·	·	·	Z	·
ASL	C← 7 ø ←ø				øE	6	3	ø6	5	2													16	6	2	1E	7	3																		N	·	·	·	·	·	Z	C
BBR[#(ø-7)]	Branch on M_b=0 (5)																																							øF	1F	2F	3F	4F	5F	6F	7F	·	·	·	·	·	·	·	·
BBS[#(ø-7)]	Branch on M_b=1 (5)																																							8F	9F	AF	BF	CF	DF	EF	FF	·	·	·	·	·	·	·	·
BCC	Branch on C=ø (2)																															9ø	2	2															·	·	·	·	·	·	·	·
BCS	Branch on C=1 (2)																															Bø	2	2															·	·	·	·	·	·	·	·
BEQ	Branch on Z=1 (2)																															Fø	2	2															·	·	·	·	·	·	·	·
BIT	A M				2C	4	3	24	3	2																																							M₇	M₆	·	·	·	·	Z	·
BMI	Branch on N=1 (2)																															3ø	2	2															·	·	·	·	·	·	·	·
BNE	Branch on Z=ø (2)																															Dø	2	2															·	·	·	·	·	·	·	·
BPL	Branch on N=ø (2)																															1ø	2	2															·	·	·	·	·	·	·	·
BRA	Branch Always (1)																															80	3	2															·	·	·	·	·	·	·	·
BRK	Break													00	7	1																															·	·	·	1	·	1	·	·
BVC	Branch on V=ø (2)																															5ø	2	2															·	·	·	·	·	·	·	·
BVS	Branch on V=1 (2)																															7ø	2	2															·	·	·	·	·	·	·	·
CLC	ø→C													18	2	1																															·	·	·	·	·	·	·	ø
CLD	ø→D													D8	2	1																															·	·	·	·	ø	·	·	·
CLI	ø→I													58	2	1																															·	·	·	·	ø	·	·	·
CLV	ø→V													B8	2	1																															·	ø	·	·	·	·	·	·
CMP	A M	C9	2	2	CD	4	3	C5	3	2							C1	6	2	D1	5	2	D5	4	2	DD	4	3	D9	4	3																		N	·	·	·	·	·	Z	C
CPX	X M	Eø	2	2	EC	4	3	E4	3	2																																					N	·	·	·	·	·	Z	C
CPY	Y M	Cø	2	2	CC	4	3	C4	3	2																																					N	·	·	·	·	·	Z	C
DEC	M 1→M				CE	6	3	C6	5	2													D6	6	2	DE	7	3																		N	·	·	·	·	·	Z	·
DEX	X 1→X													CA	2	1																															N	·	·	·	·	·	Z	·
DEY	Y 1→Y													88	2	1																															N	·	·	·	·	·	Z	·
EOR	AVM→A (1)	49	2	2	4D	4	3	45	3	2							41	6	2	51	5	2	55	4	2	5D	4	3	59	4	3																		N	·	·	·	·	·	Z	·
INC	M 1→M				EE	6	3	E6	5	2													F6	6	2	FE	7	3																		N	·	·	·	·	·	Z	·
INX	X 1→X													E8	2	1																															N	·	·	·	·	·	Z	·
INY	Y 1→Y													C8	2	1																															N	·	·	·	·	·	Z	·
JMP	Jump to New Loc				4C	3	3																													6C	6	3														·	·	·	·	·	·	·	·
JSR	Jump Sub				2ø	6	3																																														·	·	·	·	·	·	·	·
LDA	M→A (1)	A9	2	2	AD	4	3	A5	3	2							A1	6	2	B1	5	2	B5	4	2	BD	4	3	B9	4	3																		N	·	·	·	·	·	Z	·
LDX	M→X (1)	A2	2	2	AE	4	3	A6	3	2																			BE	4	3							B6	4	2								N	·	·	·	·	·	Z	·
LDY	M→Y (1)	Aø	2	2	AC	4	3	A4	3	2													B4	4	2	BC	4	3																		N	·	·	·	·	·	Z	·
LSR	ø→ 7 ø →C				4E	6	3	46	5	2	4A	2	1										56	6	2	5E	7	3																		ø	·	·	·	·	·	Z	C
NOP	No Operation													EA	2	1																															·	·	·	·	·	·	·	·
MUL	A * Y → A_{15-8} Y_{7-0}													02	10	1																															·	·	·	·	·	·	·	·
ORA	AVM→A (1)	ø9	2	2	øD	4	3	ø5	3	2							ø1	6	2	11	5	2	15	4	2	1D	4	3	19	4	3																		N	·	·	·	·	·	Z	·
PHA	A→Ms S 1→S													48	3	1																															·	·	·	·	·	·	·	·
PHP	P→Ms S 1→S													08	3	1																															·	·	·	·	·	·	·	·
PHX	X→Ms S 1→S													DA	3	1																															·	·	·	·	·	·	·	·
PHY	Y→Ms S 1→S													5A	3	1																															·	·	·	·	·	·	·	·
PLA	S 1→S Ms→A													68	4	1																															N	·	·	·	·	·	Z	·
PLP	S 1→S Ms→P													28	4	1																																		(Restored)						
PLX	S 1→S Ms→X													FA	4	1																															N	·	·	·	·	·	Z	·
PLY	S 1→S Ms→Y													7A	4	1																															N	·	·	·	·	·	Z	·
RMB[#(ø-7)]	ø →M_b (5)																																														ø7	17	27	37	47	57	67	77	·	·	·	·	·	·	·	·
ROL	7 ø C				2E	6	3	26	5	2	2A	2	1										36	6	2	3E	7	3																		N	·	·	·	·	·	Z	C
ROR	C 7 ø				6E	6	3	66	5	2	6A	2	1										76	6	2	7E	7	3																		N	·	·	·	·	·	Z	C
RTI	Rtrn Int													4ø	6	1																																		(Restored)						
RTS	Rtrn Sub													6ø	6	1																															·	·	·	·	·	·	·	·
SBC	A-M $\bar{C}$→A (1) (5)	E9	2	2	ED	4	3	E5	3	2							E1	6	2	F1	5	2	F5	4	2	FD	4	3	F9	4	3																		N	V	·	·	·	·	Z	C
SEC	1→C													38	2	1																															·	·	·	·	·	·	·	1
SED	1→D													F8	2	1																															·	·	·	·	1	·	·	·
SEI	1→I													78	2	1																															·	·	·	·	1	·	·	·
SMB[#(ø-7)]	1→M_b (5)																																														87	97	A7	B7	C7	D7	E7	F7	·	·	·	·	·	·	·	·
STA	A→M				8D	4	3	85	3	2							81	6	2	91	6	2	95	4	2	9D	5	3	99	5	3																		·	·	·	·	·	·	·	·
STX	X→M				8E	4	3	86	3	2																															96	4	2								·	·	·	·	·	·	·	·
STY	Y→M				8C	4	3	84	3	2													94	4	2																							·	·	·	·	·	·	·	·
TAX	A→X													AA	2	1																															N	·	·	·	·	·	Z	·
TAY	A→Y													A8	2	1																															N	·	·	·	·	·	Z	·
TSX	S→X													BA	2	1																															N	·	·	·	·	·	Z	·
TXA	X→A													8A	2	1																															N	·	·	·	·	·	Z	·
TXS	X→S													9A	2	1																															·	·	·	·	·	·	·	·
TYA	Y→A													98	2	1																															N	·	·	·	·	·	Z	·

Notes:

1 Add 1 to N if page boundary is crossed
2 Add 1 to N if branch occurs to same page
Add 2 to N if branch occurs to different page
3 Carry not ($\bar{C}$) = Borrow
4 If in decimal mode Z flag is invalid
accumulator must be checked on zero result
5 Effects 8-bit data field of the specified zero page address

LEGEND

X = Index X
Y = Index Y
A = Accumulator
M = Memory per effective address
M_s = Memory per stack pointer
M_b = Selecter zero page memory bit
M_7 = Memory Bit 7
M_6 = Memory Bit 6
• = Add
– = Subtract
∧ = And
V = Or
∀ = Exclusive or
m = Number of cycles
# = Number of Bytes

INSTRUCTION SET OPERATION CODE MATRIX

The following matrix shows the op codes associated with the R65C00/21 and R65C29 CPUs. The matrix identifies the hexadecimal code, the mnemonic code, the addressing mode, the number of instruction bytes, and the number of machine cycles associated with each op code. Also, refer to the instruction set summary for additional information on these op codes.

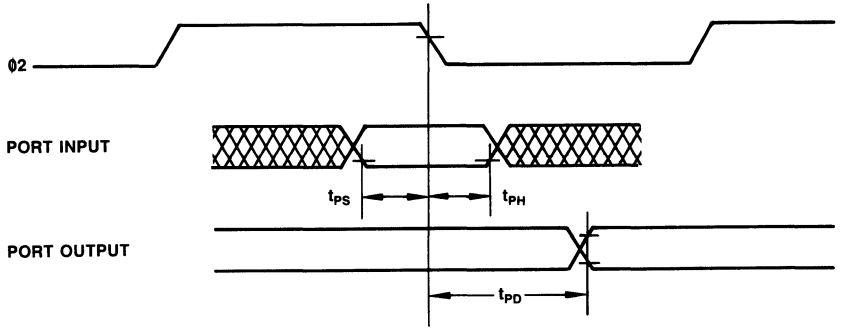
MSD \ LSD	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	MSD
0	BRK Implied 1 7	ORA (IND, X) 2 6	MUL Implied 1 10			ORA ZP 2 3	ASL ZP 2 5	RMB0 ZP 2 5	PHP Implied 1 3	ORA IMM 2 2	ASL Accum 1 2			ORA ABS 3 4	ASL ABS 3 6	BBR0 ZP 3 5**	0
1	BPL Relative 2 2**	ORA (IND), Y 2 5*				ORA ZP, X 2 4	ASL ZP, X 2 6	RMB1 ZP 2 5	CLC Implied 1 2	ORA ABS, Y 3 4*				ORA ABS, X 3 4*	ASL ABS, X 3 7	BBR1 ZP 3 5**	1
2	JSR Absolute 3 6	AND (IND, X) 2 6			BIT ZP 2 3	AND ZP 2 3	ROL ZP 2 5	RMB2 ZP 2 5	PLP Implied 1 4	AND IMM 2 2	ROL Accum 1 2		BIT ABS 3 4	AND ABS 3 4	ROL ABS 3 6	BBR2 ZP 3 5**	2
3	BMI Relative 2 2**	AND (IND, Y) 2 5*				AND ZP, X 2 4	ROL ZP, X 2 6	RMB3 ZP 2 5	SEC Implied 1 2	AND ABS, Y 3 4*				AND ABS, X 3 4*	ROL ABS, X 3 7	BBR3 ZP 3 5**	3
4	RTI Implied 1 6	EOR (IND, X) 2 6				EOR ZP 2 3	LSR ZP 2 5	RMB4 ZP 2 5	PHA Implied 1 3	EOR IMM 2 2	LSR Accum 1 2		JMP ABS 3 3	EOR ABS 3 4	LSR ABS 3 6	BBR4 ZP 3 5**	4
5	BVC Relative 2 2**	EOR (IND), Y 2 5*				EOR ZP, X 2 4	LSR ZP, X 2 6	RMB5 ZP 2 5	CLI Implied 1 2	EOR ABS, Y 3 4*	PHY Implied 1 3			EOR ABS, X 3 4*	LSR ABS, X 3 7	BBR5 ZP 3 5**	5
6	RTS Implied 1 6	ADC (IND, X) 2 6				ADC ZP 2 3	ROR ZP 2 5	RMB6 ZP 2 5	PLA Implied 1 4	ADC IMM 2 2	ROR Accum 1 2		JMP Indirect 3 5	ADC ABS 3 4	ROR ABS 3 6	BBR6 ZP 3 5**	6
7	BVS Relative 2 2**	ADC (IND, Y) 2 5*				ADC ZP, X 2 4	ROR ZP, X 2 6	RMB7 ZP 2 5	SEI Implied 1 2	ADC ABS, Y 3 4*	PLY Implied 1 4			ADC ABS, X 3 4*	ROR ABS, X 3 7	BBR7 ZP 3 5**	7
8	BRA Relative 2 3*	STA (IND, X) 2 6			STY ZP 2 3	STA ZP 2 3	STX ZP 2 3	SMB0 ZP 2 5	DEY Implied 1 2		TXA Implied 1 2		STY ABS 3 4	STA ABS 3 4	STX ABS 3 4	BBS0 ZP 3 5**	8
9	BCC Relative 2 2**	STA (IND, Y) 2 6			STY ZP, X 2 4	STA ZP, X 2 4	STX ZP, Y 2 4	SMB1 ZP 2 5	TYA Implied 1 2	STA ABS, Y 3 5	TXS Implied 1 2			STA ABS, X 3 5		BBS1 ZP 3 5**	9
A	LDY IMM 2 2	LDA (IND, X) 2 6	LDX IMM 2 2		LDY ZP 2 3	LDA ZP 2 3	LDX ZP 2 3	SMB2 ZP 2 5	TAY Implied 1 2	LDA IMM 2 2	TAX Implied 1 2		LDY ABS 3 4	LDA ABS 3 4	LDX ABS 3 4	BBS2 ZP 3 5**	A
B	BCS Relative 2 2**	LDA (IND), Y 2 5*			LDY. ZP, X 2 4	LDA ZP, X 2 4	LDX ZP, Y 2 4	SMB3 ZP 2 5	CLV Implied 1 2	LDA ABS, Y 3 4*	TSX Implied 1 2		LDY ABS, X 3 4*	LDA ABS, X 3 4*	LDX ABS, Y 3 4*	BBS3 ZP 3 5**	B
C	CPY IMM 2 2	CMP (IND, X) 2 6			CPY ZP 2 3	CMP ZP 2 3	DEC ZP 2 5	SMB4 ZP 2 5	INY Implied 1 2	CMP IMM 2 2	DEX Implied 1 2		CPY ABS 3 4	CMP ABS 3 4	DEC ABS 3 6	BBS4 ZP 3 5**	C
D	BNE Relative 2 2**	CMP (IND), Y 2 5*				CMP ZP, X 2 4	DEC ZP, X 2 6	SMB5 ZP 2 5	CLD Implied 1 2	CMP ABS, Y 3 4*	PHX Implied 1 3			CMP ABS, X 3 4*	DEC ABS, X 3 7	BBS5 ZP 3 5**	D
E	CPX IMM 2 2	SBC (IND, X) 2 6			CPX ZP 2 3	SBC ZP 2 3	INC ZP 2 5	SMB6 ZP 2 5	INX Implied 1 2	SBC IMM 2 2	NOP Implied 1 2		CPX ABS 3 4	SBC ABS 3 4	INC ABS 3 6	BBS6 ZP 3 5**	E
F	BEQ Relative 2 2**	SBC (IND), Y 2 5*				SBC ZP, X 2 4	INC ZP, X 2 6	SMB7 ZP 2 5	SED Implied 1 2	SBC ABS, Y 3 4*	PLX Implied 1 4			SBC ABS, X 3 4*	INC ABS, X 3 7	BBS7 ZP 3 5**	F
	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	

—OP Code
—Addressing Mode
—Instruction Bytes; Machine Cycles

—New Opcode

*Add 1 to N if page boundary is crossed.
**Add 1 to N if branch occurs to same page;
Add 2 to N if branch occurs to different page.

I/O PORT WAVEFORMS—ALL PORTS



I/O PORT TIMING—ALL PORTS

Parameter	Symbol	2 MHz		4 MHz	
		Min	Max	Min	Max
Input Data Setup Time	t_{PS}	50	—	35	—
Input Data Hold Time (Port D)	t_{PH}	10	—	10	—
Input Data Hold Time (All ports except D)		25	—	25	—
Output Data Delay Time	t_{PD}	—	120	—	100

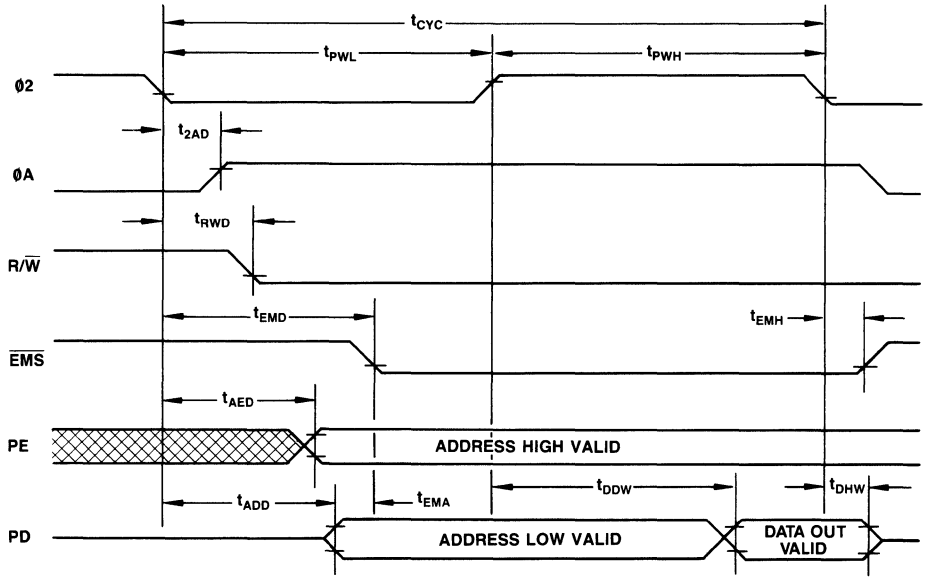
EXPANSION BUS TIMING

(V_{CC} = 5.0V ± 10%, T_A = 0°C to 70°C

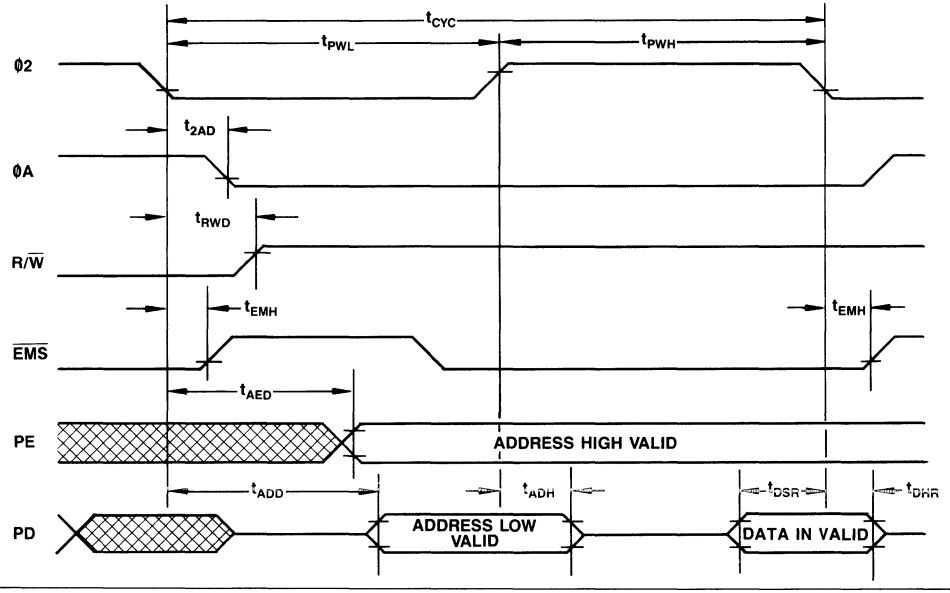
Parameter	Symbol	2 MHz		4 MHz		Unit
		Min.	Max.	Min.	Max.	
Clock/Control Timing						
Ø2 Cycle Time	t_{CYC}	500	See Note 1	250	See Note 1	ns
Pulse Width Ø2 Low	t_{PWL}	235	265	115	135	ns
Pulse Width Ø2 High	t_{PWH}	235	265	115	135	ns
ØA Delay Time — Ø2 to Ø2A	t_{2AD}	0	60	0	50	ns
$\overline{EMS}$ Delay Time — Address Valid to $\overline{EMS}$ Low	t_{EMA}	10	—	10	—	ns
$\overline{EMS}$ Delay Time — Ø2 to $\overline{EMS}$ Low	t_{EMD}	—	150	—	115	ns
$\overline{EMS}$ Hold Time	t_{EMH}	10	—	10	—	ns
$R\overline{W}$ Delay Time	t_{RWD}	20	100	10	80	ns
PE Address Delay Time	t_{AED}	20	100	10	80	ns
PD Address Delay Time	t_{ADD}	20	120	10	100	ns
Write Timing						
Data Delay Time — Write	t_{DDW}	—	120	—	100	ns
Data Hold Time — Write	t_{DHW}	20	—	20	—	ns
Read Timing						
PD Address Hold Time — Read	t_{ADH}	0	80	0	60	ns
Data Setup Time — Read	t_{DSR}	50	—	35	—	ns
Data Hold Time — Read	t_{DHR}	10	—	10	—	ns

Note: 1. The Ø2 clock should never be held static at a dc level. The maximum cycle time (t_{CYC}) that guarantees no data loss to internal registers is 20 microseconds.

EXPANSION BUS WRITE CYCLE WAVE FORMS



EXPANSION BUS READ CYCLE WAVE FORMS



MAXIMUM RATINGS*

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to +7.0	Vdc
Input Voltage	V_{IN}	−0.3 to V_{CC} +0.3	Vdc
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{STG}	−55 to +150	°C

***NOTE:** This device contains circuitry to protect the inputs against damage due to high static voltages, however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this circuit.

DC CHARACTERISTICS

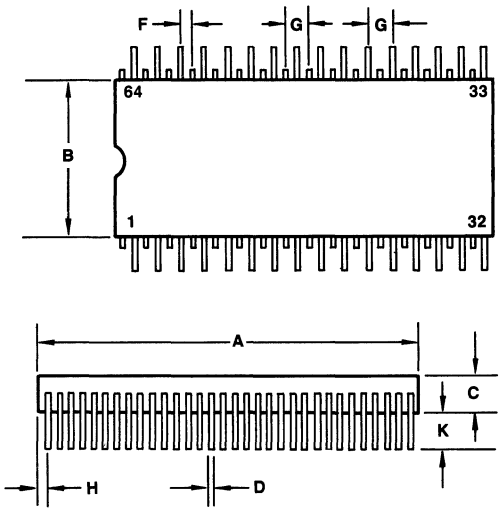
V_{CC} = +5.0V ± 10%, T_A = 0°C to 70°C (unless otherwise specified)

Parameter	Symbol	Min	Max	Unit	Test Condition
Input High Voltage	V_{IH}	+2.0	—	V	
Input Low Voltage	V_{IL}	—	+0.8	V	
Output High Voltage	V_{OH}	+2.4	—	V	V_{CC} = 4.5V I_{LOAD} = −100μA
Input Leakage Current	I_{IN}	—	±10	μA	V_{IN} = 0V or V_{CC} V_{CC} = 0V
Output Low Voltage	V_{OL}	—	+0.4	V	V_{CC} = 4.5V I_{LOAD} = 1.6 mA
Output Low Current (All ports except Port G)	I_{OUT}	—	−1.6	mA	V_{OL} = 0.4V
Input Capacitance (XTALO, XTALI) (All Others)	C_{IN}	— — —	 25 5	 pF pF	V_{CC} = 5V f = 2 MHz T_A = 25°C
Output Capacitance	C_{OUT}	—	10	pF	
Operating Frequency Crystal or Master Clock Ø2 Clock	—	 .02 .01	 8.0 4.0	 MHz MHz	
Power Dissipation	P_D	—	40	mW	V_{CC} = 5V f = 2 MHz T_A = 25°C

Note: Negative sign indicates outward current flow, positive sign indicates inward current flow.

PACKAGE DIMENSIONS

64 PIN PLASTIC QUIP (QUAD IN-LINE PACKAGE)



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	41.15	41.66	1.620	1 640
B	17.02	17.53	0.670	0.690
C	3.05	4.57	0.120	0.180
D	0.38	0.51	0.024	0.020
F	1.27 BSC		0.050 BSC	
G	2.54 BSC		0.100 BSC	
H	1.02	1.14	0.040	0.045
J	—	7°	—	7°
K	2.79	4.32	0.110	0.170
L	18.92	19.81	0.745	0.755
M	23.37	23 62	0.920	0 930

3

Rockwell

R65F11 AND R65F12 FORTH BASED MICROCOMPUTERS

SECTION 1 INTRODUCTION

1.1 FEATURES

- FORTH kernel in ROM
- Enhanced 6502 CPU
  - —Four new bit manipulation instructions:
    - Set Memory Bit (SMB)
    - Reset Memory Bit (RMB)
    - Branch on Bit Set (BBS)
    - Branch on Bit Reset (BBR)
  - —Decimal and binary arithmetic modes
  - —13 addressing modes
  - —True indexing
- 192-byte static RAM
- 16 bidirectional, TTL-compatible I/O lines (two ports, R65F11) or 40 bidirectional, TTL-compatible I/O lines (five ports, R65F12)
- One 8-bit port with programmable latched input
- Two 16-bit programmable counter/timers, with latches
  - —Pulse width measurement
  - —Asymmetrical pulse generation
  - —Pulse generation
  - —Interval timer
  - —Event counter
  - —Retriggerable interval timer
- Serial port
  - —Full-duplex asynchronous operation mode
  - —Selectable 5- to 8-bit characters
  - —Wake-up feature
  - —Synchronous shift register mode
  - —Standard programmable bit rates, programmable up to 62.5K bits/sec
- Ten interrupts
  - —Four edge-sensitive lines; two positive, two negative
  - —Reset
  - —Non-maskable
  - —Two counter
  - —Serial data received
  - —Serial data transmitted
- Expandable to 16K bytes of external memory
- Flexible clock circuitry
  - —2-MHz or 1-MHz internal operation
  - —Internal clock with external XTAL at two times internal frequency
  - —External clock input divided by one or two
- 1 μs minimum instruction execution time @ 2 MHz
- NMOS silicon gate, depletion load technology
- Single +5V power supply
- 12 mW standby power for 32 bytes of the 192-byte RAM
- 40-pin DIP (R65F11)
- 64-pin QUIP (R65F12) has three additional 8-bit I/O ports to provide a total of 40 I/O lines.

1.2 SUMMARY

The Rockwell R65F11 and R65F12 are complete, high-performance 8-bit NMOS single chip microcomputers, and are compatible with all members of the R6500 family.

The kernel of the high level Rockwell Single Chip RSC-FORTH language is contained in the preprogrammed ROM of the R65F11 and R65F12. RSC-FORTH is based on the popular fig-FORTH model with extensions. All of the run time functions of RSC-FORTH are contained in the ROM, including 16- and 32-bit mathematical, logical and stack manipulation, plus memory and input/output operators. The RSC-FORTH Operating System allows an external user program written in RSC-FORTH or Assembly Language to be executed from external EPROM, or development of such a program under the control of the R65FR1 RSC-FORTH Development ROM. Other development ROM's can also be accommodated.

The R65F11 and R65F12 consist of an enhanced 6502 CPU, an internal clock oscillator, 192 bytes of Random Access Memory (RAM) and versatile interface circuitry. The interface circuitry includes two 16-bit programmable timer/counters, 16 bidirectional input/output lines (including four edge-sensitive lines and input latching on one 8-bit port), a full-duplex serial I/O channel, ten interrupts and bus expandability.

The innovative architecture and the demonstrated high performance of the R6502 CPU, as well as instruction simplicity, results in system cost-effectiveness and a wide range of

computational power These features in combination with the FORTH high level operating system make the R65F11 and R65F12 ideal for microcomputer applications.

For systems requiring additional I/O ports, the 64-pin QUIP version, the R65F12, provides three additional 8-bit ports.

A complete RSC-FORTH development system can be created with three MOS parts: the R65F11, one RAM chip and the R65FR1 Development ROM.

This product description is for the reader familiar with the R6502 CPU hardware and programming capabilities. A detailed description of the R6502 CPU hardware is included in the R6500 Microcomputer System Hardware Manual (Order Number 201). A description of the instruction capabilites of the R6502 CPU is contained in the R6500 Microcomputer System Programming Manual (Order Number 202).

1.3 ORDERING INFORMATION

Part No.	Description
R65F11P	40-Pin FORTH Based Microcomputer at 1 MHz
R65F11AP	40-Pin FORTH Based Microcomputer at 2 MHz
R65F12Q	64-Pin FORTH Based Microcomputer at 1 MHz
R65F12AQ	64-Pin FORTH Based Microcomputer at 2 MHz
R65FR1P	FORTH Development ROM for R65F11 or R65F12
R65FR2P	FORTH Development ROM for expanded capacity
R65FK2P	FORTH Kernel ROM for expanded capacity development
R65FR3P	FORTH Development ROM for R6501Q
R65FK3P	FORTH Kernel ROM for R6501Q
Order No.	**Description**
2148	FORTH Based Microcomputer User's Manual*

Note:
*Included with R65FR1.

3

SECTION 2
INTERFACE REQUIREMENTS

This section describes the interface requirements for the R65F11 and R65F12 single chip microcomputers. Figure 2-1 is the Interface Diagram for the R65F11 and R65F12, Figure 2-2 shows the pin out configuration and Table 2-1 describes the function of each pin of the R65F11 and R65F12. Figure 3-1 is a detailed block diagram.

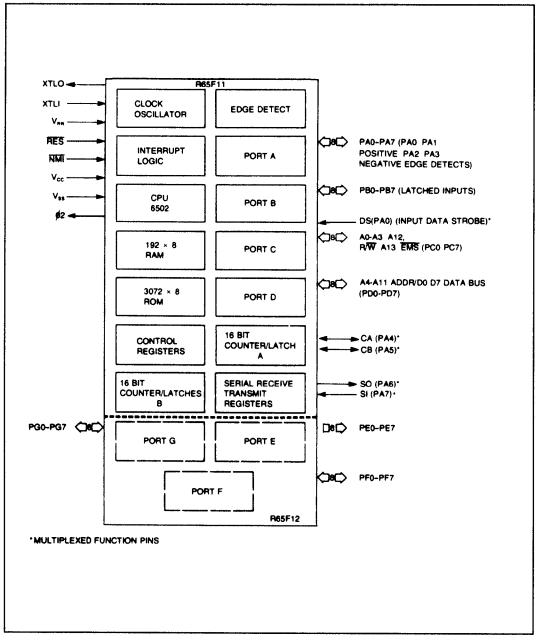
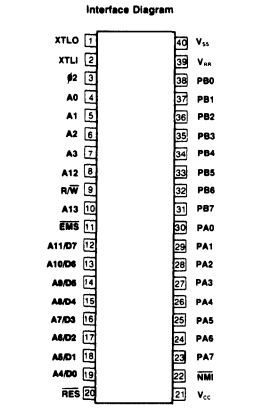


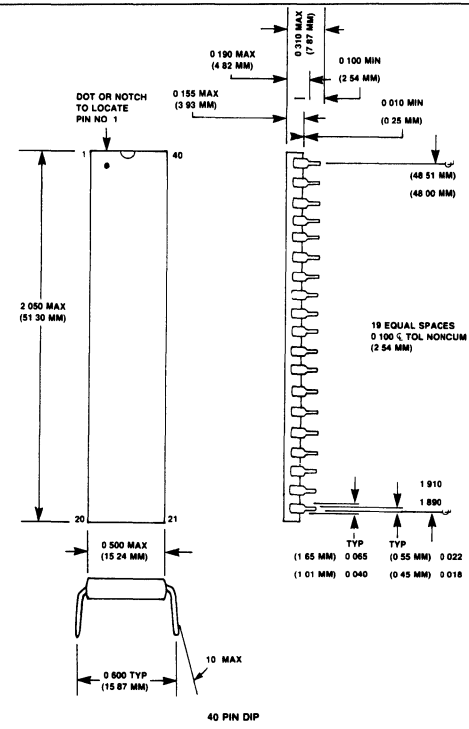
Figure 2-1. R65F11 and R65F12 Interface Diagram

Table 2-1. R65F11 and R65F12 Pin Descriptions

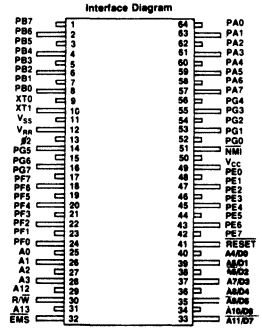
Signal Name	Pin No. R65F11	Pin No. R65F12	Description
V_{CC}	21	50	Main power supply +5V
V_{RR}	39	12	Separate power pin for RAM. In the event that V_{CC} power is lost, this power retains RAM data.
V_{SS}	40	11	Signal and power ground (0V)
XTLI	2	10	Crystal or clock input for internal clock oscillator. Also allows input of X1 clock signal if XTLO is connected to V_{SS}, or X2 or X4 clock if XTLO is floated.
XTLO	1	9	Crystal output from internal clock oscillator.
$\overline{RES}$	20	41	The Reset input is used to initialize the R65F11. This signal must not transition from low to high for at least eight cycles after V_{CC} reaches operating range and the internal oscillator has stabilized.
ϕ2	3	13	Clock signal output at internal frequency.
$\overline{NMI}$	22	51	A negative going edge on the Non-Maskable Interrupt signal requests that a non-maskable interrupt be generated within the CPU.
PA0-PA7 PB0-PB7	30-23 38-31	64-57 8-1	Two 8-bit ports used for either input/output. Each line of Ports A and B consist of an active transistor to V_{SS} and a passive pull-up to V_{CC}.
PC0-PC7 A0-A3 A12, R/$\overline{W}$ A13, $\overline{EMS}$	4-11	25-32	Port C has an active pull-up transistor. Port D has active pull-up and pull-down transistors. Ports C and D lines form the external multiplexed address and data bus to allow external memory addressing.
PD0-PD7 A4-A11 D0-D7	19-12	40-33	
PE0-PE7 PF0-PF7 PG0-PG4 PG5-PG7		49-42 24-17 52-56, 14-16	On the R65F12, Port E may be used for output only. Ports F and G are similar to Ports A and B in construction and may be used for inputs or outputs.



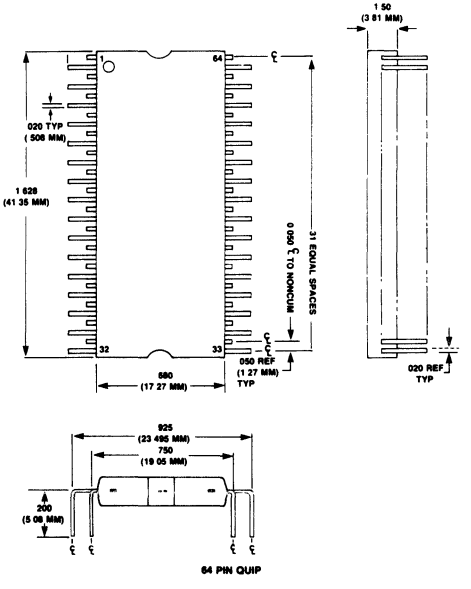
R65F11 Pin Out Designation



R65F11 Dimensional Outline



R65F12 Pin Out Designation



R65F12 Dimensional Outline

Figure 2-2. Pin Out Configuration

SECTION 3
SYSTEM ARCHITECTURE

This section provides a functional description of the R65F11 and R65F12. Functionally the R65F11 consists of a CPU, RAM memory, two 8-bit parallel I/O ports (five in the 64-pin R65F12), a serial I/O port, dual counter/latch circuits, a mode control register, an interrupt flag/enable dual register circuit, and an internal Operating System. The kernel of FORTH in ROM complements the system hardware. A block diagram of the system is shown in Figure 3-1.

NOTE

Throughout this document, unless specified otherwise, all memory or register address locations are specified in hexadecimal notation.

3.1 CPU LOGIC

The R65F11 internal CPU is a standard 6502 configuration with an 8-bit Accumulator register, two 8-bit Index Registers (X and Y); an 8-bit Stack Pointer register, and ALU, a 16-bit Program Counter, and standard instruction register/decode and internal timing control logic.

3.1.1 Accumulator

The accumulator is a general purpose 8-bit register that stores the results of most arithmetic and logic operations. In addition, the accumulator usually contains one of the two data words used in these operations.

3.1.2 Index Registers

There are two 8-bit index registers, X and Y. Each index register can be used as a base to modify the address data program counter and thus obtain a new address—the sum of the program counter contents and the index register contents.

When executing an instruction which specifies indirect addressing, the CPU fetches the op code and the address, and modifies the address from memory by adding the index register to it prior to loading or storing the value of memory.

Indexing greatly simplifies many types of programs, especially those using data tables.

3.1.3 Stack Pointer

The Stack Pointer is an 8-bit register. It is automatically incremented and decremented under control of the microprocessor to perform stack manipulation in response to either user instructions, an internal $\overline{IRQ}$ interrupt, or the external interrupt line $\overline{NMI}$. The Stack Pointer must be initialized by the user program.

The stack allows simple implementation of multiple level interrupts, subroutine nesting and simplification of many types of data manipulation. The JSR, BRK, RTI and RTS instructions use the stack and Stack Pointer.

The stack can be envisioned as a deck of cards which may only be accessed from the top. The address of a memory location is stored (or "pushed") onto the stack. Each time data are to be pushed onto the stack, the Stack Pointer is placed on the Address Bus, data are written into the memory location addressed by the Stack Pointer, and the Stack Pointer is decremented by 1. Each time data are read (or "pulled") from the stack, the Stack Pointer is incremented by 1. The Stack Pointer is then placed on the Address Bus, and data are read from the memory location addressed by the Pointer.

The stack is located on zero page, i.e., memory locations 00FF-0040. After reset, which leaves the Stack Pointer indeterminate, normal usage calls for its initialization at 00FF.

3.1.4 Processor Status Register

The 8-bit Processor Status Register contains seven status flags. Some of these flags are controlled by the user program; others may be controlled both by the user's program and the CPU. The R6500 instruction set contains a number of conditional branch instructions which are designed to allow testing of these flags. See Appendix B for details.

3.1.5 Program Counter

The 16-bit Program Counter provides the addresses that are used to step the processor through sequential instructions in a program. Each time the processor fetches an instruction from program memory, the lower (least significant) byte of the Program Counter (PCL) is placed on the low-order bits of the Address Bus and the higher (most significant) byte of the Program Counter (PCH) is placed on the high-order 8 bits of the Address Bus. The Counter is incremented each time an instruction or data is fetched from program memory.

3.1.6 Arithmetic And Logic Unit (ALU)

Each bit of the ALU has two inputs. These inputs can be tied to various internal buses or to a logic zero; the ALU then generates the function (AND, OR, SUM, and so on) using the data on the two inputs.

3.1.7 Instruction Register and Instruction Decode

Instructions are fetched from ROM or RAM and gated onto the Internal Data Bus. These instructions are latched into the Instruction Register then decoded along with timing and interrupt signals to generate control signals for the various registers.

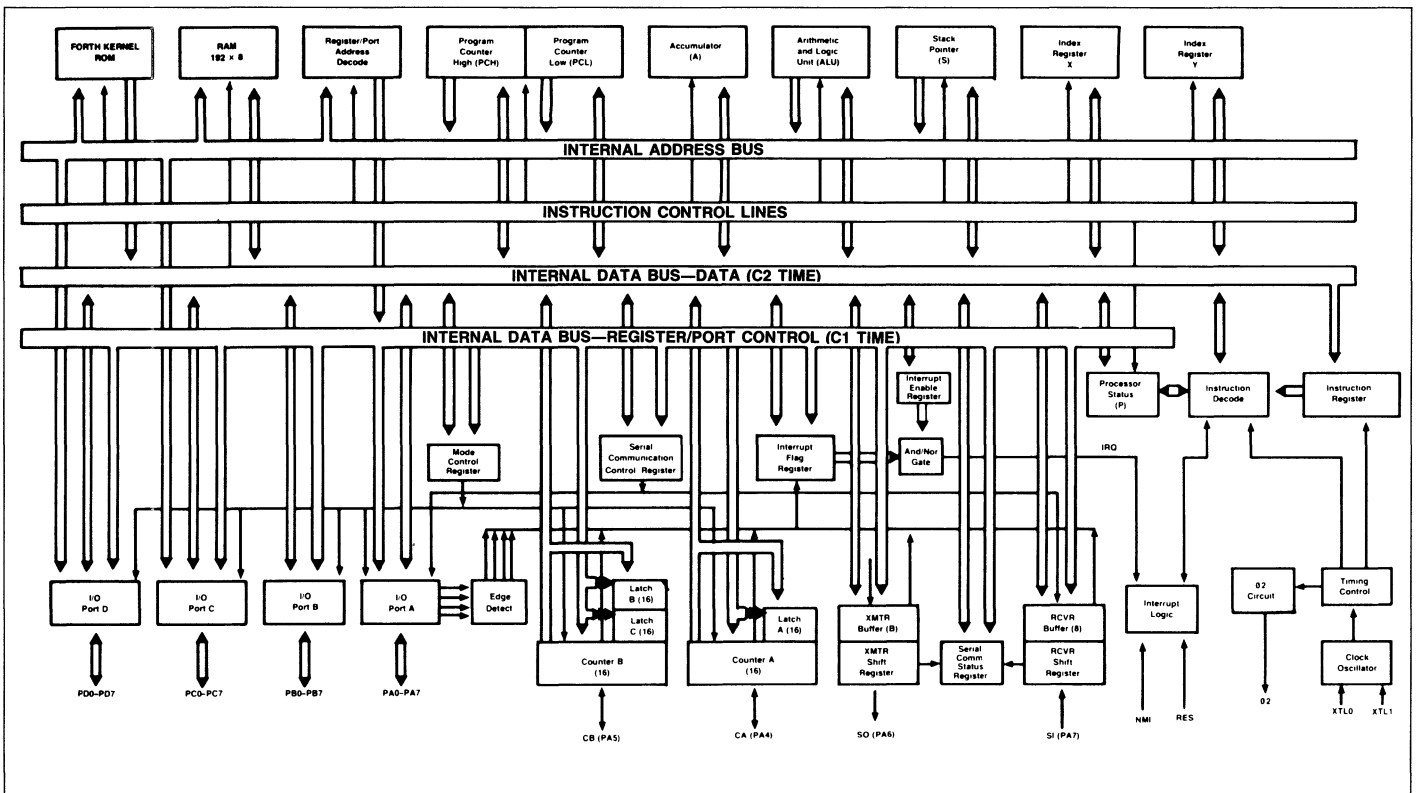


Figure 3-1. Detailed Block Diagram

3.1.8 Timing Control

The Timing Control Logic keeps track of the specific instruction cycle being executed. This logic is set to T0 each time an instruction fetch is executed and is advanced at the beginning of each Phase One clock pulse for as many cycles as are required to complete the instruction. Each data transfer which takes place between the registers is caused by decoding the contents of both the instruction register and timing control unit.

3.1.9 Interrupt Logic

Interrupt logic controls the sequencing of three interrupts; $\overline{RES}$, $\overline{NMI}$ and $\overline{IRQ}$. $\overline{IRQ}$ is generated by any one of eight conditions: 2 Counter Overflows, 2 Positive Edge Detects, 2 Negative Edge Detects, and 2 Serial Port Conditions.

3.2 CPU INSTRUCTION SET

The machine code instruction set of the R65F11 and R65F12 microcomputers are based on the popular R6500 microprocessor set. They contain all the instructions in the standard R6502 set, with the addition of the four new bit instructions added to the R6511 processor family. Refer to Appendix A for the Op Code mnemonics addressing matrix for details on these instructions.

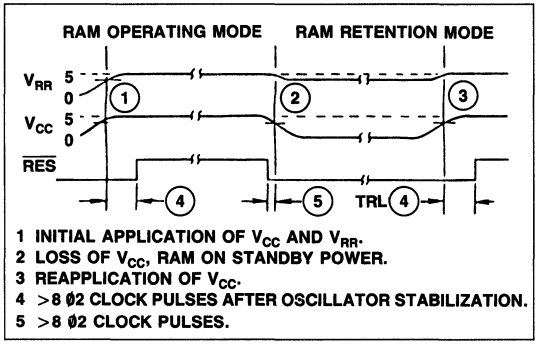
3.3 READ-ONLY-MEMORY (ROM)

The ROM consists of preprogrammed memory with an address space from F400 to FFFF. It contains the run time kernel of the high level language Rockwell Single Chip FORTH. There are 133 included functions stored in the ROM. Codes are in the format of a two byte code field, which identifies the interpreter assigned to execute that word, followed by a variable length Parameter Field, which contains the instructions and data used by that interpreter according to the programmed intention of that definition. See Appendix D for a complete list of the names of all included words. All words needed for support of the run time operation of dedicated applications programs are included. The RSC-FORTH Operating System is also part of the ROM code and is entered upon Reset. This Operating System allow the R65F11 and R65F12 to auto start a user program written in either RSC-FORTH or Assembly Language or enter a Development ROM if one is present. If no auto start program is found, an attempt will be made to boot an operating program from floppy disk.

3.4 RANDOM ACCESS MEMORY (RAM)

The RAM consists of 192 bytes of read/write memory with an assigned page zero address of 0040 through 00FF. The R65F11 and R65F12 provide a separate power pin (V_{RR}) which may be used for standby power for 32 bytes located at 0040-005F. In the event of the loss of V_{CC} power, the lowest 32 bytes of RAM data will be retained if standby power is supplied to the V_{RR} pin. If the RAM data retention is not required then V_{RR} must be connected to V_{CC}. During operation V_{RR} must be at the V_{CC} level.

For the RAM to retain data upon loss of V_{CC}, V_{RR} must be supplied within operating range and $\overline{RES}$ must be driven low at least eight Ø2 clock pulses before V_{CC} falls out of operating range. $\overline{RES}$ must then be held low while V_{CC} is out of operating range and until at least eight Ø2 clock cycles after V_{CC} is again within operating range and the internal Ø2 oscillator is stabilized. V_{RR} must remain within V_{CC} operating range during normal operation. When V_{CC} is out of operating range, V_{RR} must remain within the V_{RR} retention range in order to retain data. Figure 3-2 shows typical waveforms.



1 INITIAL APPLICATION OF V_{CC} AND V_{RR}.
2 LOSS OF V_{CC}, RAM ON STANDBY POWER.
3 REAPPLICATION OF V_{CC}.
4 >8 Ø2 CLOCK PULSES AFTER OSCILLATOR STABILIZATION.
5 >8 Ø2 CLOCK PULSES.

Figure 3-2. Data Retention Timing

3.5 CLOCK OSCILLATOR

A reference frequency can be generated with the on-chip oscillator using an external crystal. The oscillator reference frequency passes through an internal countdown network (divide by 2) to obtain the internal operating frequency (see Figure 3-3a).

Internal timing can also be controlled by driving the XTLI pin with an external frequency source. Figure 3-3b shows typical connections. If XTLO is left floating, the external source is divided by the internal countdown network. However, if XTLO is tied to V_{SS}, the internal coundown network is bypassed causing the chip to operate at the frequency of the external source.

The R65F11 and R65F12 operate in the CLOCK MASTER mode. In this mode a frequence source (crystal or external source) must be applied to the XTLI and XTLO pins.

NOTE: When operating at a 1 MHz internal frequency place a 15-22 pF capacitor between XTLO and GND.

Ø2 is a buffered output signal which closely approximates the internal timing. When a common external source is used to drive multiple devices the internal timing between devices as well as their Ø2 outputs will be skewed in time. If skewing represents a system problem it can be avoided by the Master/Slave connection and options shown in Figure 3-4.

The R65F11 and R65F12 is operated in the CLOCK MASTER MODE. A second processor could be operated in the CLOCK

SLAVE MODE. Mask options in the SLAVE unit convert the Ø2 signal into a clock input pin which is tightly coupled to the internal timing generator. As a result the internal timing of the MASTER and SLAVE units are synchronized with minimum skew. If the Ø2 signal to the SLAVE unit is inverted, the MASTER and SLAVE UNITS WILL OPERATE OUT OF PHASE. This approach allows the two devices to share external memory using cycle stealing techniques.

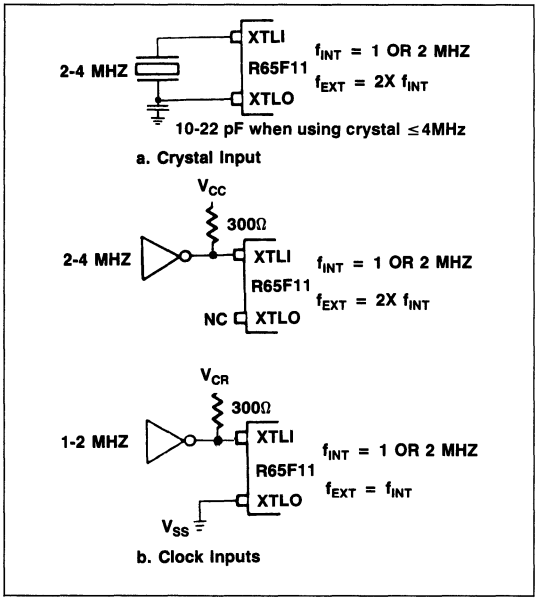


Figure 3-3. Clock Oscillator Input Options

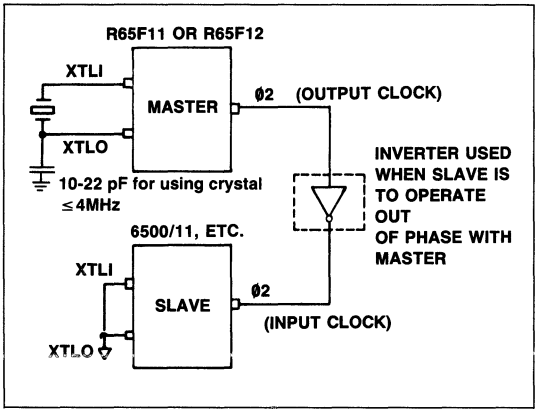


Figure 3-4. Master/Slave Connections

3.6 MODE CONTROL REGISTER (MCR)

The Mode Control Register contains control bits for the multifunction I/O ports and mode select bits for Counter A and Counter B. Its setting, along with the setting of the Serial Communications Control Register (SCCR), determines the basic configuration of the R65F11 and R65F12 in any application. The Mode Control Register bit assignment is shown in Figure 3-5. MCR Bits 7, 6, 5 must remain 1's in order for external memory referencing to be enabled.

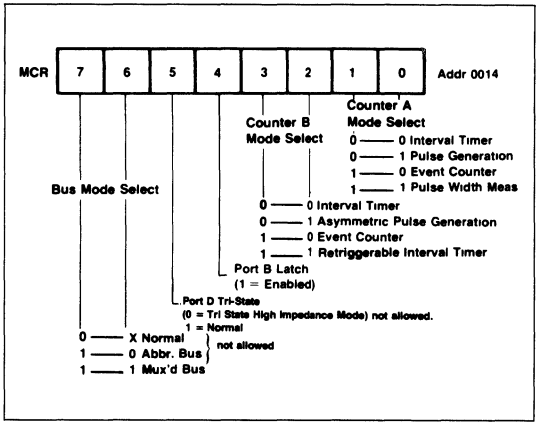


Figure 3-5. Mode Control Register

The use of Counter A Mode Select is shown in Section 6.1.

The use of Counter B Mode Select is shown in Section 6.2.

The use of Port B Latch Enable is shown in Section 4.4.

3.7 INTERRUPT FLAG REGISTER (IFR) AND INTERRUPT ENABLE REGISTER (IER)

An $\overline{IRQ}$ interrupt request can be initiated by any or all of eight possible sources. These sources are all capable of being enabled or disabled by the use of the appropriate interrupt enabled bits in the Interrupt Enable Register (IER). Multiple simultaneous interrupts will cause the $\overline{IRQ}$ interrupt request to remain active until all interrupting conditions have been serviced and cleared.

The Interrupt Flag Register contains the information that indicates which I/O or counter needs attention. The contents of the Interrupt Flag Register may be examined at any time by reading at address: 0011. Edge detect IFR bits may be cleared in low level code by executing a RMB instruction at address location 0010. The RMB X, (0010) instruction reads FF, modifies bit X to a "0", and writes the modified value at address location 0011. In this way IFR bits set to a "1" after the read cycle of a Read-Modify-Write instruction (such as RMB) are protected from being cleared. A logic "1" is ignored when writing to edge detect IFR bits.

Each IFR bit has a corresponding bit in the Interrupt Enable Register which can be set to a "1" by writing a "1" in the respective bit position at location 0012. Individual IER bits may be cleared by writing a "0" in the respective bit position, or by $\overline{RES}$. If set to a "1", an IRQ will be generated when the corresponding IFR bit becomes true. The Interrupt Flag Register and Interrupt Enable Register bit assignments are shown in Figure 3-6 and the functions of each bit are explained in Table 3-1.

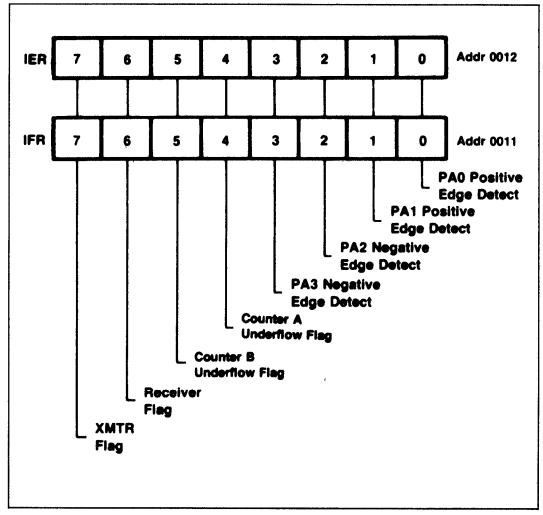


Figure 3-6. Interrupt Enable and Flag Registers

Table 3-1. Interrupt Flag Register Bit Codes

Bit Code	Function
IFR 0:	PA0 Positive Edge Detect Flag—Set to a "1" when a positive going edge is detected on PA0. Cleared by RMB 0 (0010) instruction or by $\overline{RES}$.
IFR 1:	PA1 Positive Edge Detect Flag—Set to a 1 when a positive going edge is detected on PA1. Cleared by RMB 1 (0010) instruction or by $\overline{RES}$.
IFR 2:	PA2 Negative Edge Detect Flag—Set to a 1 when a negative going edge is detected on PA2. Cleared by RMB 2 (0010) instruction or by $\overline{RES}$.
IFR 3:	PA3 Negative Edge Detect Flag—Set to 1 when a negative going edge is detected on PA3. Cleared by RMB 3 (0010) instruction or by $\overline{RES}$.
IFR 4:	Counter A Underflow Flag—Set to a 1 when Counter A underflow occurs. Cleared by reading the Lower Counter A at location 0018, by writing to address location 001A, or by $\overline{RES}$.
IFR 5:	Counter B Underflow Flag—Set to a 1 when Counter B underflow occurs. Cleared by reading the Lower Counter B at location 001C, by writing to address location 001E, or by $\overline{RES}$.
IFR 6:	Receiver Interrupt Flag—Set to a 1 when any of the Serial Communication Status Register bits 0 through 3 is set to a 1. Cleared when the Receiver Status bits (SCSR 0-3) are cleared or by $\overline{RES}$.
IFR 7:	Transmitter Interrupt Flag—Set to a 1 when SCSR 6 is set to a 1 while SCSR 5 is a 0 or SCSR 7 is set to a 1. Cleared when the Transmitter Status bits (SCSR 6 & 7) are cleared or by $\overline{RES}$.

3.8 OPERATING SYSTEM

The system startup function, COLD, is executed upon Reset. COLD, a high level FORTH word, forms the basis of the RSC Operating System. Upon reset this function initializes the R65F11 or R65F12 registers to establish the external 16K byte memory map and disable all interrupt sources. It also sets up the serial channel for 1200 baud (assuming a 1 MHz internal clock) asynchronous transmission (seven bits, parity disabled). The internal FORTH structure "W" is prepared for use and the low level input/output vectors are forced to point to the system serial channel routines. The FORTH User Area Pointer, UP, is assigned the value 0300 Hex.

A test is made of the variable CLD/WRM in memory location 030E. If this contains a value other than A55A Hex a cold reset is assumed. In this case, the low level IRQ vector, IRQVEC; the low level NMI Vector, NMIVEC, and the high level interrupt vector, INTVEC, are all forced to point to the system reset routine. This prevents an unintentionally generated interrupt from crashing the system. System variables TIB, RO, SO, UC/L, UPAD, UR/W and BASE are also initialized to their default values.

Whether a warm or cold reset, the memory map is then searched at every 1K byte boundary starting at location 0400 Hex. The first two bytes at each boundary are checked against an A55A Hex bit pattern. This pattern indicates that an auto start program is installed. The next two bytes are assumed to point to the Parameter Field of the high level RSC-FORTH word to be executed upon reset. This may be the main function of a user defined program or the start up routine of a Development ROM. Figure 3-7 details proper alignment.

If no auto start ROM is found, the Operating System turns control over to a program that issues a "NO ROM" message to the systems terminal via the serial channel and attempts to boot a program from disk. A floppy disk controller, compatible with the WD1793 type, is assumed to be present at address 0100 Hex. The first half of Track 0 Sector 1 is loaded from a double density boot diskette into RAM starting at address 005F. When successfully loaded execution will be turned over to this boot program.

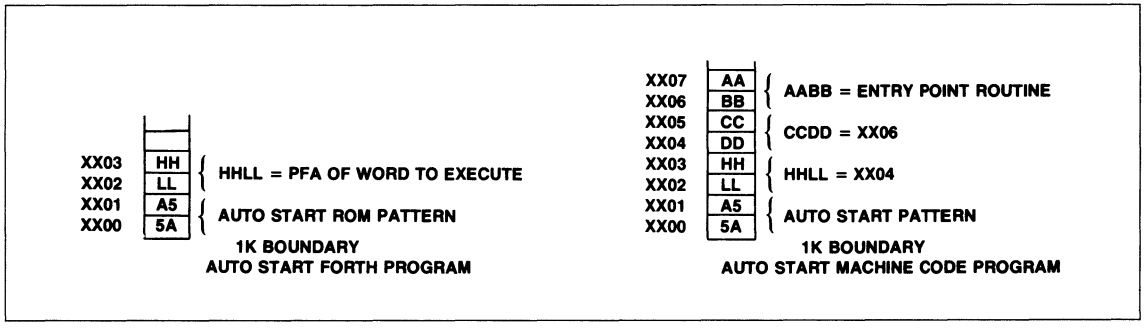


Figure 3-7. Auto Start ROM

SECTION 4
PARALLEL INPUT/OUTPUT PORTS

The R65F11 has 16 I/O lines grouped into two 8-bit ports (PA, PB) and 16 lines programmed as an Address/Data bus (PC & PD). Ports A and B may be used either for input or output individually or in groups of any combination. The R65F12 has 24 additional port lines grouped into three 8-bit ports (PE, PF, PG).

Multifunction I/O's such as Port A are protected from normal port I/O instructions when they are programmed to perform a multiplexed function.

Internal pull-up resistors (FET's with an impedance range of 3K ≤ Rpu ≤ 12K ohm) are provided on all port pins.

The direction of the I/O lines are controlled by 8-bit port registers located in page zero. This arrangement provides quick programming access using simple two-byte zero page address instructions. There are no direction registers associated with the I/O ports, which simplifies I/O handling. The I/O addresses are shown in Table 4-1.

Table 4-1. I/O Port Addresses

Port	Address
A	0000
B	0001
E	0004
F	0005
G	0006

Appendix F.4 shows the I/O Port Timing.

4.1 INPUTS

Inputs for Ports A and B are enabled by loading logic 1 into all I/O port register bit positions that are to correspond to I/O input lines. A low (<0.8V) input signal will cause a logic 0 to be read when a read instruction is issued to the port register. A high (>2.0V) input will cause a logic 1 to be read. An $\overline{RES}$ signal forces all I/O port registers to logic 1 thus initially treating all I/O lines as inputs.

The status of the input lines can be interrogated at any time by reading the I/O port addresses. Note that this will return the actual status of the input lines, not the data written into the I/O port registers.

Read/Modify/Write instructions can be used to modify the operation of PA and PB. During the Read cycle of a Read/Modify/Write instruction the Port I/O register is read. For all other read instructions the port input lines are read. Read/Modify/Write instructions are: ASL, DEC, INC, LSR, RMB, ROL, ROR, and SMB.

4.2 OUTPUTS

Outputs for Ports A and B are controlled by writing the desired I/O line output states into the corresponding I/O port register bit positions. A logic 1 will force a high (>2.4V) output while a logic 0 will force a low (<0.4V) output.

4.3 PORT A (PA)

Port A can be programmed via the Mode Control Register (MCR) and the Serial Communications Control Register (SCCR) as a standard parallel 8-bit, bit independent, I/O port or as serial channel I/O lines, counter I/O lines, or an input data strobe for the Port B input latch option. Table 4-3 tabulates the control and usage of Port A.

In addition to their normal I/O functions, PA0 and PA1 can detect positive going edges, and PA2 and PA3 can detect negative going edges. A proper transition on these pins will set a corresponding status bit in the IFR and generate an interrupt request if the respective Interrupt Enable Bit is set. The maximum rate at which an edge can be detected is one-half the Ø2 clock rate. Edge detection timing is shown in Appendix F.4.

4.4 PORT B (PB)

Port B can be programmed as an 8 bit, bit independent I/O port. It has a latched input capability which may be enabled or disabled via the Mode Control Register (MCR). Table 4-2 tabulates the control and usage of Port B. An Input Data Strobe signal must be provided thru PA0 when Port B is programmed to be used with latched input option. Input data latch timing for Port B is shown in Appendix F.4.

Table 4-2. Port B Control & Usage

Pin No. R65F11	Pin No. R65F12	I/O Mode MCR4 = 0 Signal Name	I/O Mode MCR4 = 0 Signal Type (1)	Latch Mode MCR4 = 1 (2) Signal Name	Latch Mode MCR4 = 1 (2) Signal Type
38	8	PB0	I/O	PB0	INPUT
37	7	PB1	I/O	PB1	INPUT
36	6	PB2	I/O	PB2	INPUT
35	5	PB3	I/O	PB3	INPUT
34	4	PB4	I/O	PB4	INPUT
33	3	PB5	I/O	PB5	INPUT
32	2	PB6	I/O	PB6	INPUT
31	1	PB7	I/O	PB7	INPUT

(1) Resistive pull-up, active buffer pull down
(2) Input data is stored in port B latch by PA0 pulse

Table 4-3. Port A Control and Usage

R65F11/R65F12 PORT[5]	PA0 I/O		PORT B LATCH MODE	
	MCR4 = 0		MCR4 = 1	
	SIGNAL		SIGNAL	
	NAME	TYPE	NAME	TYPE
PA0[2]	PA0	I/O	PORT B LATCH STROBE	INPUT[1]

	PA1-PA3 I/O	
	SIGNAL	
	NAME	TYPE
PA1[2] PA2[3] PA3[3]	PA1 PA2 PA3	I/O I/O I/O

PA4	PA4 I/O		COUNTER A I/O			
	MCR0 = 0 MCR1 = 0 SCCR7 = 0 RCVR S/R MODE = 0[4] [6]		MCR0 = 1 MSR1 = 0 SCCR7 = 0 RCVR S/R MODE = 0[4]		SCCR7 = 0 SCCR6 = 0 MCR1 = 1	
	SIGNAL		SIGNAL		SIGNAL	
	NAME	TYPE	NAME	TYPE	NAME	TYPE
	PA4	I/O	CNTA	OUTPUT	CNTA	INPUT (1)
	SERIAL I/O SHIFT REGISTER CLOCK					
	SCCR7 = 1 SCCR5 = 1		RCVR S/R MODE = 1[4]			
	SIGNAL		SIGNAL			
	NAME	TYPE	NAME	TYPE		
	XMTR CLOCK	OUTPUT	RCVR CLOCK	INPUT (1)		

PA5	PA5 I/O		COUNTER B I/O			
	MCR3 = 0 MCR2 = 0		MCR3 = 0 MCR2 = 1		MCR3 = 1 MCR2 = X	
	SIGNAL		SIGNAL		SIGNAL	
	NAME	TYPE	NAME	TYPE	NAME	TYPE
	PA5	I/O	CNTB	OUTPUT	CNTB	INPUT (1)

PA6	PA6 I/O		SERIAL I/O XMTR OUTPUT	
	SCCR7 = 0		SCCR7 = 1	
	SIGNAL		SIGNAL	
	NAME	TYPE	NAME	TYPE
	PA6	I/O	XMTR	OUTPUT

PA7	PA7 I/O		SERIAL I/O RCVR INPUT	
	SCCR6 = 0		SCCR6 = 1	
	SIGNAL		SIGNAL	
	NAME	TYPE	NAME	TYPE
	PA7	I/O	RCVR	INPUT (1)

(1) HARDWARE BUFFER FLOAT
(2) POSITIVE EDGE DETECT
(3) NEGATIVE EDGE DETECT
(4) RCVR S/R MODE = 1 WHEN SCCR6 • SCCR5 • SCCR4 = 1
(5) APPLIES TO EITHER R65F11 OR R65F12 PORT (SEE PIN DIAGRAM)
(6) FOR THE FOLLOWING MODE COMBINATIONS PA4 IS AVAILABLE AS AN INPUT ONLY PIN.
$\overline{SCCR7} \cdot SCCR6 \cdot SCCR5 \cdot \overline{MCR1} + \overline{SCCR7} \cdot SCCR6 \cdot \overline{SCCR4} \cdot MCR1 + SCCR7 \cdot \overline{SCCR6} \cdot \overline{SCCR5} + SCCR7 \cdot \overline{SCCR5} \cdot \overline{SCCR4}$

4.5 PORT C (PC)

Port C is preprogrammed as part of the Address/Data bus. PC0-PC7 function as A0-A3, A12, R/W, A13, and $\overline{EMS}$, respectively, as shown in Table 4-4. $\overline{EMS}$ (External Memory Select) is asserted (low) whenever the internal processor accesses memory area between 0100 and 3FFF. (See Memory Map, Appendix C). The leading edge of $\overline{EMS}$ may be used to strobe the eight address lines multiplexed on Port D. See Appendix F.3 for Port C timing.

4.6 PORT D (PD)

Port D is also preprogrammed as part of the Address/Data bus. Data bits D0 through D7 are time multiplexed with address bits A4 through A11, respectively. Refer to the Memory Maps (Appendix C) for Multiplexed memory assignments. See Appendix F.3 for Port D timing.

4.7 PORT E (PE), PORT F (PF), PORT G (PG)

Ports E, F and G are available on the R65F12 only. Port E can only be used as outputs. Port F and Port G can be used for inputs or outputs and are similar to Port A and Port B in operation.

Table 4-4. Port C Control and Usage

R65F11/ R65F12 Port	Multiplexed Mode MCR7 = 1 MCR6 = 1 Signal	
	Name	Type (1)
PC0	A0	OUTPUT
PC1	A1	OUTPUT
PC2	A2	OUTPUT
PC3	A3	OUTPUT
PC4	A12	OUTPUT
PC5	R/W	OUTPUT
PC6	A13	OUTPUT
PC7	EMS	OUTPUT

Table 4-5. Port D Control and Usage

R65F11/ R65F12 Port	Multiplexed Mode MCR7 = 1 MCR6 = 1 MCR5 = 1 Signal Phase 1		Signal Phase 2	
	Name	Type (2)	Name	Type (3)
PD0	A4	OUTPUT	DATA0	I/O
PD1	A5	OUTPUT	DATA1	I/O
PD2	A6	OUTPUT	DATA2	I/O
PD3	A7	OUTPUT	DATA3	I/O
PD4	A8	OUTPUT	DATA4	I/O
PD5	A9	OUTPUT	DATA5	I/O
PD6	A10	OUTPUT	DATA6	I/O
PD7	A11	OUTPUT	DATA7	I/O

(1) Active Buffer Pull-up and Pull-Down
(2) Tri-State Buffer is in Active Mode
(3) Tri-State Buffer is in Active Mode only during the Phase 2 Portion of a Write Cycle

SECTION 5
SERIAL INPUT/OUTPUT CHANNEL

The R65F11 and R65F12 Microcomputers provide a full duplex Serial I/O channel with programmable bit rates and operating modes. The serial I/O functions are controlled by the Serial Communication Control Register (SCCR). The SCCR bit assignment is shown in Figure 5-1. The serial bit rate is determined by Counter A for all modes except the Receiver Shift Register (RCVR S/R) mode for which an external shift clock must be provided. The maximum data rate using the internal clock is 62.5K bits per second (@ Ø2 = 1 MHZ). The transmitter (XMTR) and receiver (RCVR) can be independently programmed to operate in different modes and can be independently enabled or disabled.

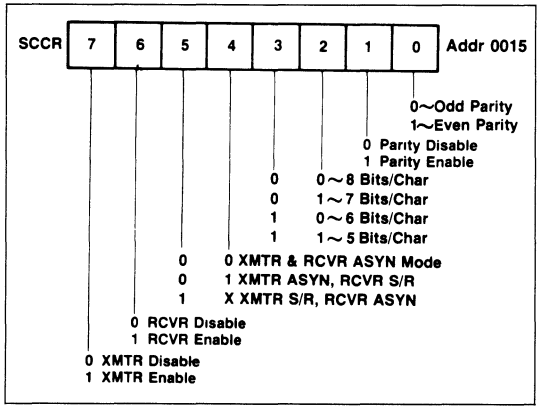


Figure 5-1. Serial Communication Control Register

Except for the Receiver Shift Register Mode (RCVR S/R), all XMTR and RCVR bit rates will occur at one sixteenth of the Counter A interval timer rate. Counter A is forced into an interval timer mode whenever the serial I/O is enabled in a mode requiring an internal clock.

Whenever Counter A is required as a timing source it must be loaded with the hexadecimal code that selects the data rate for the serial I/O Port Refer to Counter A (paragraph 6.1) for a table of hexadecimal values to represent the desired data rate.

5.1 TRANSMITTER OPERATION (XTMR)

The XTMR operation and the transmitter related control/status functions are enabled by bit 7 of the Serial Communications Control Register (SCCR). The transmitter, when in the Asynchronous (ASYN) mode, automatically adds a start bit, one or two stop bits, and, when enabled, a parity bit to the transmitted data. A word of transmitted data (in asynchronous parity mode) can have 5, 6, 7, or 8 bits of data. The nine data modes are shown below. When parity is disabled, the 5, 6, 7 or 8 bits of data are terminated with two stop bits.

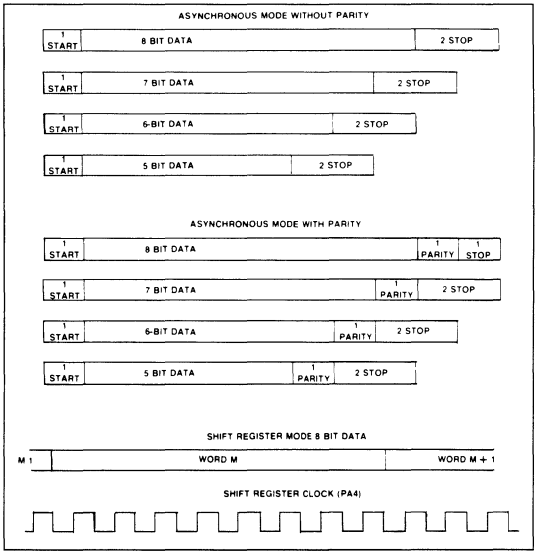


Figure 5-2. Bit Allocations

In the S/R mode, eight data bits are always shifted out. Bits/character and parity control bits are ignored The serial data is shifted out via the SO output (PA6) and the shift clock is available at the CA (PA4) pin. When the transmitter underruns in the S/R mode the SO output and shift clock are held in a high state.

The XMTR Interrupt Flag bit (IFR7) is controlled by Serial Communication Status Register bits SCCR5, SCCR6 and SCCR7.

$$IFR7 = SCSR6 (\overline{SCCR5} + SCCR7)$$

5.2 RECEIVER OPERATION (RCVR)

The receiver and its selected control and status functions are enabled when SCCR-6 is set to a "1." In the ASYN mode, data format must have a start bit, appropriate number of data bits, a parity bit (if enabled) and one stop bit. Refer to Figure 5-2 for a diagram of bit allocations. The receiver bit period is divided into 8 sub-intervals for internal synchronization. The receiver bit stream is synchronized by the start bit and a strobe signal is generated at the approximate center of each incoming bit. Refer to Figure 5-3 for ASYN Receive Data Timing. The character assembly process does not start if the start bit signal is less than one-half the bit time after a low level is detected on the Receive Data Input. Framing error, over-run, and parity error conditions or a RCVR Data Register Full will set the appropriate status bits, and any of the above conditions will cause an Interrupt Request if the Receiver Interrupt Enable bit is set to logic 1.

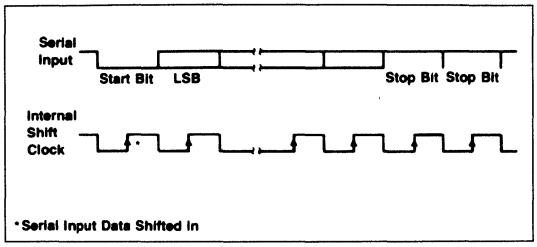


Figure 5-3. ASYN Receive Data Timing

In the S/R mode, an external shift clock must be provided at CA (PA4) pin along with 8 bits of serial data (LSB first) at the SI input (PA7). The maximum data rate using an external shift clock is one-eighth the internal clock rate. Refer to Figure 5-4 for S/R Mode Timing.

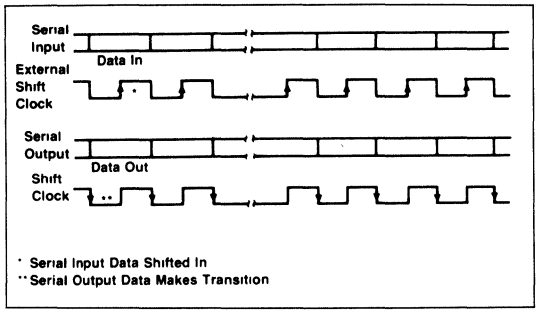


Figure 5-4. S/R Mode Timing

A RCVR interrupt (IFR6) is generated whenever any of SCSR0-3 are true.

5.3 SERIAL COMMUNICATION STATUS REGISTER (SCSR)

The Serial Communication Status Register (SCSR) holds information on various communication error conditions, status of the transmitter and receiver data registers, a transmitter end-of-transmission condition, and a receiver idle line condition (Wake-Up Feature). The SCSR bit assignment is shown in Figure 5-5. Bit assignments and functions of the SCSR are as follows:

SCSR 0: *Receiver Data Register Full*—Set to a logic 1 when a character is transferred from the Receiver Shift Register to the Receiver Data Register. This bit is cleared by reading the Receiver Data Register, or by $\overline{RES}$ and is disabled if SCCR 6 = 0. The SCSR 0 bit will not be set to a logic 1 if the received data contains an error condition, however, a corresponding error bit will be set to a logic 1 instead.

SCSR 1: *Over-Run Error*—Set to a logic 1 when a new character is transferred from the Receiver Shift Register, with the last character still in the Receiver Data Register. This bit is cleared by reading the Receiver Data Register, or by $\overline{RES}$

SCSR 2. *Parity Error*—Set to logic 1 when the RCVR is in the ASYN Mode, Parity Enable bit is set, and the received data has a parity error This bit is cleared by reading the Receiver Data Register or by $\overline{RES}$.

SCSR 3: *Framing Error*—Set to a logic 1 when the received data contains a zero bit after the last data or parity bit in the stop bit slot. Cleared by reading the Receiver Data Register or by $\overline{RES}$. (ASYN Mode only).

SCSR 4: *Wake-Up*—Set to a logic 1 by writing a "1" in bit 4 of address: 0016. The Wake-Up bit is cleared by $\overline{RES}$ or when the receiver detects a string of ten consecutive 1's. When the Wake-Up bit is set SCSR0 through SCSR3 are inhibited.

SCSR 5: *End of Transmission*—Set to a logic 1 by writing a "1" in bit position 5 of address: 0016. The End of Transmission bit is cleared by $\overline{RES}$ or upon writing a new data word into the Transmitter Data Register. When the End-of-Transmission bit is true the Transmitter Register Empty bit is disabled until a Transmitter Under-Run occurs.

SCSR 6. *Transmitter Data Register Empty*—Set to a logic 1 when the contents of the Transmitter Data Register is transferred to the Transmitter Shift Register. Cleared upon writing new data into the Transmit Data Register. This bit is initialized to a logic 1 by $\overline{RES}$.

SCSR 7. *Transmitter Under-Run*—Set to a logic 1 when the last data bit is transmitted if the transmitter is in a S/R Mode or when the last stop bit is transmitted if the XMTR is in the ASYN Mode while the Transmitter Data Register Empty Bit is set. Cleared by a transfer of new data into the Transmitter Shift Register, or by $\overline{RES}$.

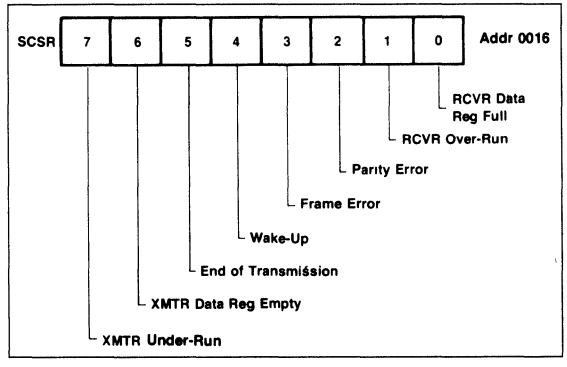


Figure 5-5. SCSR Bit Allocations

5.4 WAKE-UP FEATURE

In a multi-distributed microprocessor or microcomputer applications, a destination address is usually included at the beginning of the message. The Wake-Up Feature allows non-selected CPU's to ignore the remainder of the message until the beginning of the next message by setting the Wake-Up bit. As long as the Wake-Up flag is true, the Receiver Data Register Full Flag remains false. The Wake-Up bit is automatically cleared when the receiver detects a string of ten consecutive 1's which indicates an idle transmit line. When the next byte is received, the Receiver Data Register Full Flag signals the CPU to wake-up and read the received data.

SECTION 6
COUNTER/TIMERS

The R65F11 and R65F12 Microcomputers contain two 16-bit counters (Counter A and Counter B) and three 16-bit latches associated with the counters. Counter A has one 16-bit latch and Counter B has two 16-bit latches. Each counter can be independently programmed to operate in one of four modes:

Counter A	Counter B
• Pulse width measurement	• Retriggerable Interval Counter
• Pulse Generation	• Asymmetrical Pulse Generation
• Interval Timer	• Interval Timer
• Event Counter	• Event Counter

Operating modes of Counter A and Counter B are controlled by the Mode Control Register. All counting begins at the initialization value and decrements. When modes are selected requiring a counter input/output line, PA4 is automatically selected for Counter A and PA5 is automatically selected for Counter B (see Table 4.2).

6.1 COUNTER A

Counter A consists of a 16-bit counter and a 16-bit latch organized as follows: Lower Counter A (LCA), Upper Counter A (UCA), Lower Latch A (LLA), and Upper Latch A (ULA). The counter contains the count of either Ø2 clock pulses or external events, depending on the counter mode selected. The contents of Counter A may be read any time by executing a read at location 0019 for the Upper Counter A and at location 001A or location 0018 for the Lower Counter A. A read at location 0018 also clears the Counter A Underflow Flag (IFR4).

The 16-bit latch contains the counter initialization value, and can be loaded at any time by executing a write to the Upper Latch A at location 0019 and the Lower Latch A at location 0018. In either case, the contents of the accumulator are copied into the applicable latch register.

Counter A can be started at any time by writing to address: 001A. The contents of the accumulator will be copied into the Upper Latch A before the contents of the 16-bit latch are transferred to Counter A. Counter A is set to the latch value whenever Counter A underflows. When Counter A decrements from 0000 the next counter value will be the latch value, not FFFF, and the Counter A Underflow Flag (IFR 4) will be set to "1". This bit may be cleared by reading the Lower Counter A at location 0018, by writing to address location 001A, or by $\overline{RES}$.

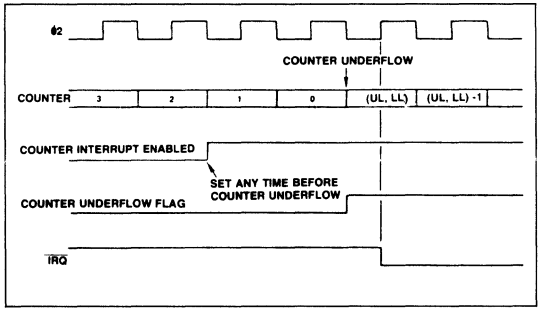


Figure 6-1. Interval Timer Timing Diagram

Counter A operates in any of four modes. These modes are selected by the Counter A Mode Control bits in the Control Register. See Table 6-1.

Table 6-1. Counter A Control Bits

MCR1 (bit 1)	MCR0 (bit 0)	Mode
0	0	Interval Timer
0	1	Pulse Generation
1	0	Event Counter
1	1	Pulse Width Measurement

The Interval Timer, Pulse Generation, and Pulse Width Measurement Modes are Ø2 clock counter modes. The Event Counter Mode counts the occurrences of an external event on the CNTR line.

The Counter is set to the Interval Timer Mode (00) when a $\overline{RES}$ signal is generated.

6.1.1 Interval Timer

In the Interval Timer mode the Counter is initialized to the Latch value by either of two conditions:

1. When the Counter is decremented from 0000, the next Counter value is the Latch value (not FFFF).

2. When a write operation is performed to the Load Upper Latch and Transfer Latch to Counter address 001A, the Counter is loaded with the Latch value. Note that the contents of the Accumulator are loaded into the Upper Latch before the Latch value is transferred to the Counter.

The Counter value is decremented by one count at the Ø2 clock rate. The 16-bit Counter can hold from 1 to 65535 counts The Counter Timer capacity is therefore 1μs to 65 535 ms at the 1 MHz Ø2 clock rate or 0.5 μs to 32.767 ms at the 2 MHz Ø2 clock rate. Time intervals greater than the maximum Counter value can be easily measured by counting $\overline{IRQ}$ interrupt requests in the counter $\overline{IRQ}$ interrupt routine.

When Counter A decrements from 0000, the Counter A Underflow (IFR4) is set to logic 1. If the Counter A Interrupt Enable Bit (IER4) is also set, an $\overline{IRQ}$ interrupt request will be generated. The Counter A Underflow bit in the Interrupt Flag Register can be examined in the $\overline{IRQ}$ interrupt routine to determine that the $\overline{IRQ}$ was generated by the Counter A Underflow.

While the timer is operating in the Interval Timer Mode, PA4 operates as a PA I/O bit.

A timing diagram of the Interval Timer Mode is shown in Figure 6-1.

6.1.2 Pulse Generation Mode

In the Pulse Generation mode, the CA line operates as a Counter Output. The line toggles from low to high or from high to low whenever a Counter A Underflow occurs, or a write is performed to address 001A.

The normal output waveform is a symmetrical square-wave. The CA output is initialized high when entering the mode and transitions low when writing to 001A.

Asymmetric waveforms can be generated if the value of the latch is changed after each counter underflow.

A one-shot waveform can be generated by changing from Pulse Generation to Interval Timer mode after only one occurrence of the output toggle condition.

6.1.3 Event Counter Mode

In this mode the CA is used as an Event Input line, and the Counter will decrement with each rising edge detected on this line. The maximum rate at which this edge can be detected is one-half the ϕ2 clock rate.

The Counter can count up to 65,535 occurrences before underflowing. As in the other modes, the Counter A Underflow bit (IER4) is set to logic 1 if the underflow occurs.

Figure 6 2 is a timing diagram of the Event Counter Mode.

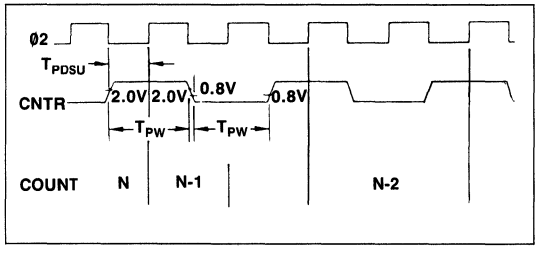


Figure 6-2. Event Counter Mode

6.1.4 Pulse Width Measurement Mode

This mode allows the accurate measurement of a low pulse duration on the CA line. The Counter decrements by one count at the ϕ2 clock rate as long as the CA line is held in the low state. The Counter is stopped when CA is in the high state

The Counter A underflow flag will be set only when the count in the timer reaches zero. Upon reaching zero the timer will be loaded with the latch value and continue counting down as long as the CA pin is held low. After the counter is stopped by a high level on CA, the count will hold as long as CA remains high. Any further low levels on CA will again cause the counter to count down from its present value. The state of the CA line can be determined by testing the state of PA4.

A timing diagram for the Pulse Width Measurement Mode is shown in Figure 6-3.

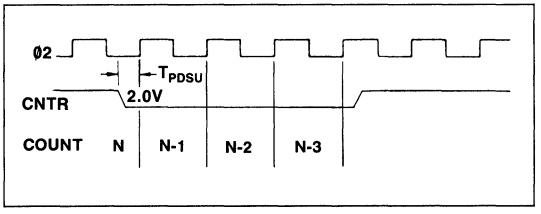


Figure 6-3. Pulse Width Measurement

6.1.5 Serial I/O Data Rate Generation

Counter A also provides clock timing for the Serial I/O which establishes the data rate for the Serial I/O port. When the Serial I/O is enabled, Counter A is forced to operate at the internal clock rate. Counter A is not required for the RCVR S/R mode. The Counter I/O (PA4) may also be required to support the Serial I/O (see Table 4-2).

Table 6-2 identifies the values to be loaded in Counter A for selecting standard data rates with a ϕ2 clock rate of 1 MHz and 2 MHz. Although Table 6-2 identifies only the more common data rates, any data rate from 1 to 62.5K bps can be selected by using the formula:

$$N = \frac{\phi 2}{16 \times \text{bps}} - 1$$

where

N = decimal value to be loaded into Counter A using its hexadecimal equivalent.
ϕ2 = the clock frequency (1 MHz or 2 MHz)
bps = the desired data rate.

NOTE

In Table 6-2 you will notice that the standard data rate and the actual data rate may be slightly different. Transmitter and receiver errors of 1.5% or less are acceptable. A revised clock rate is included in Table 6-2 for those baud rates which fall outside this limit.

Table 6-2. Counter A Values for Baud Rate Selection

Standard Baud Rate	Hexadecimal Value		Actual Baud Rate At		Clock Rate Needed To Get Standard Baud Rate	
	1 MHz	2 MHz	1 MHz	2 MHz	1 MHz	2 MHz
50	04E1	09C3	50.00	50.00	1 0000	2 0000
75	0340	0682	75 03	74.99	1.0000	2 0000
110	0237	046F	110.04	110.04	1.0000	2.0000
150	01A0	0340	149.88	150.06	1 0000	2.0000
300	00CF	01A0	300 48	299.76	1.0000	2 0000
600	0067	00CF	600.96	600.96	1 0000	2.0000
1200	0033	0067	1201 92	1201.92	1.0000	2 0000
2400	0019	0033	2403.85	2403.85	1 0000	2.0000
3600	0010	0021	3676 47	3676.47	0 9792	1.9584
4800	000C	0019	4807 69	4807 69	1 0000	2 0000
7200	0008	0010	6944.44	7352 94	1 0368	1.9584
9600	0006	000C	8928.57	9615 38	1 0752	2 0000

6.2 COUNTER B

Counter B consists of a 16-bit counter and two 16-bit latches organized as follows Lower Counter B (LCB), Upper Counter B (UCB), Lower Latch B (LLB), Upper Latch B (ULB), Lower Latch C (LLC), and Upper Latch C (ULC). Latch C is used only in the asymmetrical pulse generation mode. The counter contains the count of either Ø2 clock pulses or external events depending on the counter mode selected. The contents of Counter B may be read any time by executing a read at location 001D for the Upper Counter B and at location 001E or 001C for the Lower Counter B. A read at location 001C also clears the Counter B Underflow Flag.

Latch B contains the counter initialization value, and can be loaded at any time by executing a write to the Upper Latch B at location 001D and the Lower Latch B at location 001C In each case, the contents of the accumulator are copied into the applicable latch register

Counter B can be initialized at any time by writing to address. 001E The contents of the accumulator is copied into the Upper Latch B before the value in the 16-bit Latch B is transferred to Counter B. Counter B will also be set to the latch value and the Counter B Underflow Flag bit (IFR5) will be set to a "1" whenever Counter B underflows by decrementing from 0000.

IFR 5 may be cleared by reading the Lower Counter B at location 001C, by writing to address location 001E, or by $\overline{RES}$.

Counter B operates in the same manner as Counter A in the Interval Timer and Event Counter modes. The Pulse Width Measurement Mode is replaced by the Retriggerable Interval Timer mode and the Pulse Generation mode is replaced by the Asymmetrical Pulse Generation Mode.

6.2.1 Retriggerable Interval Timer Mode

When operating in the Retriggerable Interval Timer mode, Counter B is initialized to the latch value by writing to address 001E, by a Counter B underflow, or whenever a positive edge occurs on the CB pin (PA5). The Counter B interrupt flag will be set if the counter underflows before a positive edge occurs on the CB line. Figure 6-4 illustrates the operation.

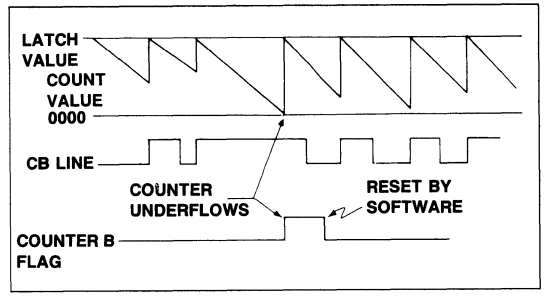


Figure 6-4. Counter B. Retriggerable Interval Timer Mode

6.2.2 Asymmetrical Pulse Generation Mode

Counter B has a special Asymmetrical Pulse Generation Mode whereby a pulse train with programmable pulse width and period can be generated without the processor intervention once the latch values are initialized.

In this mode, the 16-bit Latch B is initialized with a value which corresponds to the duration between pulses (referred to as D in the following descriptions). The 16-bit Latch C is initialized with a value which corresponds to the desired pulse width (referred to as P in the following descriptions) The initialization sequence for Latch B and C and the starting of a counting sequence are as follows.

1. The lower 8 bits of P are loaded into LLB by writing to address 001C, and the upper 8 bits of P are loaded into ULB and the full 16 bits are transferred to Latch C by writing to address location 001D. At this point both Latch B and Latch C contain the value of P.
2. The lower 8 bits of D are loaded into LLB by writing to address 001C, and the upper 8 bits of D are loaded into ULB by writing to address location 001E. Writing to address location 001E also causes the contents of the 16-bit Latch B to be downloaded into the Counter B and causes the CB output to go low as shown in Figure 6-5.
3. When the Counter B underflow occurs the contents of the Latch C is loaded into the Counter B, and the CB output toggles to a high level and stays high until another underflow occurs. Latch B is then down-loaded and the CB output toggles to a low level repeating the whole process.

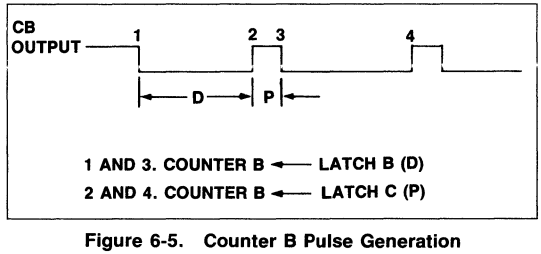


Figure 6-5. Counter B Pulse Generation

SECTION 7
POWER ON/INITIALIZATION CONSIDERATIONS

7.1 POWER-ON-RESET

The occurrence of $\overline{RES}$ going from low to high will cause the R65F11 or R65F12 to reset and enter the RSC-FORTH Operating System. As was described in Section 3.8, upon reset certain system variables will be initialized. See Appendix C.4 for a list of these variables names, locations and contents. The external memory map will be searched for an auto start ROM.

A bit pattern of A55A at a 1K byte page boundary indicates that an auto start program follows. The next two bytes are assumed to be a pointer to the high level RSC-FORTH word that is the entry point to that program. Auto start programs is written in assembly language, rather than RSC-FORTH, a series of indirect pointers as shown in 3-7 can be used to initiate program execution.

7.2 POWER ON TIMING

After application of V_{CC} and V_{RR} power to the R65F11 or R65F12, $\overline{RES}$ must be held low for at least eight $\phi 2$ clock cycles after V_{CC} reaches operating range and the internal oscillator has stabilized. This stabilization time is dependent upon the input V_{CC} voltage and performance of the internal oscillator. The clock can be monitored at $\phi 2$ (pin 3). Figure 7-1 illustrates the power turn-on waveforms. Clock stabilization time is typically 20 ms.

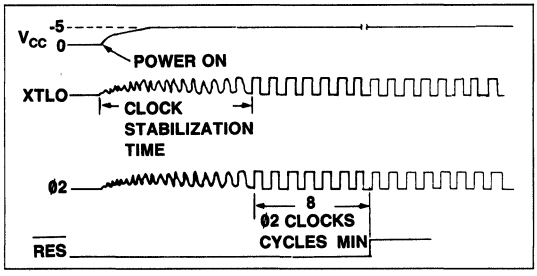


Figure 7-1. Power Turn-On Timing Detail

7.3 RESET ($\overline{RES}$) CONDITIONING

When $\overline{RES}$ is driven from low to high the R65F11 or R65F12 is put in a reset state. The registers and I/O ports are configured as shown in Table 7-1 when the external ROM is autostarted.

Table 7-1. RES Initialization of I/O Ports and Registers

	7	6	5	4	3	2	1	0
REGISTERS								
Mode Control (MCR)	1	1	1	0	0	0	0	0
Int. Enable (IER)	0	0	0	0	0	0	0	0
Int. Flag (IFR)	0	0	0	0	0	0	0	0
Ser. Com. Control (SCCR)	1	1	0	0	0	1	0	0
Ser. Com. Status (SCSR)	0	1	0	0	0	0	0	0
PORTS								
PA Latch	1	1	1	1	1	1	1	1
PB Latch	1	1	1	1	1	1	1	1

APPENDIX A
R65F11 AND R65F12 INSTRUCTION SET

This appendix contains a summary of the R6500 instruction set. For detailed information, consult the R6500 Microcomputer System Programming Manual, Document 29650 N30. The four instructions notated with a * are added instructions for the R65F11 and R65F12 which are not part of the standard 6502 instruction set.

A.1 INSTRUCTION SET IN ALPHABETIC SEQUENCE

Mnemonic	Instruction	Mnemonic	Instruction
ADC	Add Memory to Accumulator with Carry	LDA	Load Accumulator with Memory
AND	"AND" Memory with Accumulator	LDX	Load Index X with Memory
ASL	Shift Left One Bit (Memory or Accumulator)	LDY	Load Index Y with Memory
		LSR	Shift One Bit Right (Memory or Accumulator)
*BBR	Branch on Bit Reset Relative		
*BBS	Branch on Bit Set Relative		
BCC	Branch on Carry Clear	NOP	No Operation
BCS	Branch on Carry Set		
BEQ	Branch on Result Zero	ORA	"OR" Memory with Accumulator
BIT	Test Bits in Memory with Accumulator		
BMI	Branch on Result Minus	PHA	Push Accumulator on Stack
BNE	Branch on Result not Zero	PHP	Push Processor Status on Stack
BPL	Branch on Result Plus	PLA	Pull Accumulator from Stack
BRK	Force Break	PLP	Pull Processor Status from Stack
BVC	Branch on Overflow Clear		
BVS	Branch on Overflow Set	*RMB	Reset Memory Bit
		ROL	Rotate One Bit Left (Memory or Accumulator)
CLC	Clear Carry Flag		
CLD	Clear Decimal Mode	ROR	Rotate One Bit Right (Memory or Accumulator)
CLI	Clear Interrupt Disable Bit		
CLV	Clear Overflow Flag	RTI	Return from Interrupt
CMP	Compare Memory and Accumulator	RTS	Return from Subroutine
CPX	Compare Memory and Index X		
CPY	Compare Memory and Index Y	SBC	Subtract Memory from Accumulator with Borrow
DEC	Decrement Memory by One	SEC	Set Carry Flag
DEX	Decrement Index X by One	SED	Set Decimal Mode
DEY	Decrement Index Y by One	SEI	Set Interrupt Disable Status
		*SMB	Set Memory Bit
EOR	"Exclusive-Or" Memory with Accumulator	STA	Store Accumulator in Memory
		STX	Store Index X in Memory
		STY	Store Index Y in Memory
INC	Increment Memory by One		
INX	Increment Index X by One	TAX	Transfer Accumulator to Index X
INY	Increment Index Y by One	TAY	Transfer Accumulator to Index Y
		TSX	Transfer Stack Pointer to Index X
JMP	Jump to New Location	TXA	Transfer Index X to Accumulator
JSR	Jump to New Location Saving Return Address	TXS	Transfer Index X to Stack Register
		TYA	Transfer Index Y to Accumulator

A.2 R65F11 AND R65F12 INSTRUCTION SET SUMMARY TABLE

INSTRUCTIONS		R65F11 AND R65F12 ADDRESS MODES																																		PROCESSOR STATUS CODES								
		IMMEDIATE			ABSOLUTE			ZERO PAGE			ACCUM			IMPLIED			(IND, X)			(IND), Y			Z PAGE, X			ABS, X			ABS, Y			RELATIVE			INDIRECT			Z PAGE, Y			BIT ADDRESSING (OP BY BIT #)								
MNEMONIC	OPERATION	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	0	1	2	3	4	5	6	7
ADC	A M C→A (4)(1)	69	2	2	6D	4	3	65	3	2							61	6	2	71	5	2	75	4	2	7D	4	3	79	4	3																
AND	A M→A (1)	29	2	2	2D	4	3	25	3	2							21	6	2	31	5	2	35	4	2	3D	4	3	39	4	3																
ASL	C← 7 0 ←0				0E	6	3	06	5	2	0A	2	1										16	6	2	1E	7	3																	
BBR[#(0-7)]	Branch on M_6 = 0 (5)(2)																																												
BBS[#(0-7)]	Branch on M_6 = 1 (5)(2)																																												
BCC	Branch on C = 0 (2)																															90	2	2												
BCS	Branch on C = 1 (2)																															B0	2	2												
BEQ	Branch on Z = 1 (2)																															F0	2	2												
BIT	A∧M				2C	4	3	24	3	2																																				
BMI	Branch on N = 1 (2)																															30	2	2												
BNE	Branch on Z = 0 (2)																															D0	2	2												
BPL	Branch on N = 0 (2)																															10	2	2												
BRK	Break													00	7	1																														
BVC	Branch on V = 0 (2)																															50	2	2												
BVS	Branch on V = 1 (2)																															70	2	2												
CLC	0→C													18	2	1																														
CLD	0→D													D8	2	1																														
CLI	0→I													58	2	1																														
CLV	0→V													B8	2	1																														
CMP	A M (1)	C9	2	2	CD	4	3	C5	3	2							C1	6	2	D1	5	2	D5	4	2	DD	4	3	D9	4	3																
CPX	X M	E0	2	2	EC	4	3	E4	3	2																																				
CPY	Y M	C0	2	2	CC	4	3	C4	3	2																																				
DEC	M 1→M				CE	6	3	C6	5	2													D6	6	2	DE	7	3																	
DEX	X 1→X													CA	2	1																														
DEY	Y 1→Y													88	2	1																														
EOR	A∀M→A (1)	49	2	2	4D	4	3	45	3	2							41	6	2	51	5	2	55	4	2	5D	4	3	59	4	3																
INC	M 1→M				EE	6	3	E6															F6	6	2	FE	7	3																	
INX	X 1→X													E8	2	1																														
INY	Y 1→Y													C8	2	1																														
JMP	Jump to New Loc				4C	3	3																												6C	5	3									
JSR	Jump Sub				20	6	3																																							
LDA	M→A (1)	A9	2	2	AD	4	3	A5	3	2							A1	6	2	B1	5	2	B5	4	2	BD	4	3	B9	4	3																
LDX	M→X (1)	A2	2	2	AE	4	3	A6	3	2																			BE	4	3							B6	4	2						
LDY	M→Y (1)	A0	2	2	AC	4	3	A4	3	2													B4	4	2	BC	4	3																	
LSR	0→ 7 0 →C				4E	6	3	46	5	2	4A	2	1										56	6	2	5E	7	3																	
NOP	No Operation													EA	2	1																														
ORA	A∨M→A (1)	09	2	2	0D	4	3	05	3	2							01	6	2	11	5	2	15	4	2	1D	4	3	19	4	3																
PHA	A→Ms S 1→S													48	3	1																														
PHP	P→Ms S 1→S													08	3	1																														
PLA	S 1→S Ms→A													68	4	1																														
PLP	S 1→S Ms→P													28	4	1																														
RMB[#(0-7)]	0→M_b (5)																																													
ROL	7 0 C				2E	6	3	26	5	2	2A	2	1										36	6	2	3E	7	3																	
ROR	C 7 0				6E	6	3	66	5	2	6A	2	1										76	6	2	7E	7	3																	
RTI	Rtrn Int													40	6	1																														
RTS	Rtrn Sub													60	6	1																														
SBC	A M C→A (1) (4)	E9	2	2	ED	4	3	E5	3	2							E1	6	2	F1	5	2	F5	4	2	FD	4	3	F9	4	3																
SEC	1→C													38	2	1																														
SED	1→D													F8	2	1																														
SEI	1→I													78	2	1																														
SMB[#(0-7)]	1→M_b (5)																																													
STA	A→M				8D	4	3	85	3	2							81	6	2	91	6	2	95	4	2	9D	5	3	‹ ,	5	3																
STX	X→M				8E	4	3	86	3	2																													96	4	2						
STY	Y→M				8C	4	3	84	3	2													94	4	2																				
TAX	A→X													AA	2	1																														
TAY	A→Y													A8	2	1																														
TSX	S→X													BA	2	1																														
TXA	X→A													8A	2	1																														
TXS	X→S													9A	2	1																														
TYA	Y→A													98	2	1																														

NOTES

1 Add 1 to N if page boundary is crossed
2 Add 1 to N if branch occurs to same page
Add 2 to N if branch occurs to different page
3 Carry not = Borrow
4 If in decimal mode Z flag is invalid
accumulator must be checked on zero result
5 Effects 8-bit data field of the specified zero page address

LEGEND

X = Index X
Y = Index Y
A = Accumulator
M = Memory per effective address
M_s = Memory per stack pointer
M_b = Selecter zero page memory bit
M_7 = Memory Bit 7
M_6 = Memory Bit 6
• = Add
– = Subtract
∧ = And
∨ = Or
∀ = Exclusive Or
n = Number of cycles
# = Number of Bytes

A.3 INSTRUCTION CODE MATRIX

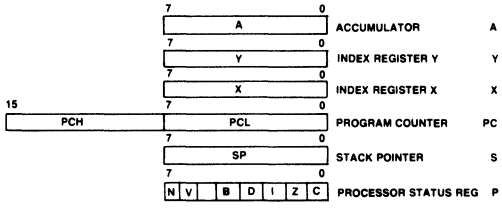
MSD \ LSD	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	MSD
0	BRK Implied 1 7	ORA (IND, X) 2 6				ORA ZP 2 3	ASL ZP 2 5	RMB0 ZP 2 5	PHP Implied 1 3	ORA IMM 2 2	ASL Accum 1 2			ORA ABS 3 4	ASL ABS 3 6	BBR0 ZP 3 5**	0
1	BPL Relative 2 2**	ORA (IND), Y 2 5*				ORA ZP, X 2 4	ASL ZP, X 2 6	RMB1 ZP 2 5	CLC Implied 1 2	ORA ABS, Y 3 4*				ORA ABS, X 3 4*	ASL ABS, X 3 7	BBR1 ZP 3 5**	1
2	JSR Absolute 3 6	AND (IND, X) 2 6			BIT ZP 2 3	AND ZP 2 3	ROL ZP 2 5	RMB2 ZP 2 5	PLP Implied 1 4	AND IMM 2 2	ROL Accum 1 2		BIT ABS 3 4	AND ABS 3 4	ROL ABS 3 6	BBR2 ZP 3 5**	2
3	BMI Relative 2 2**	AND (IND, Y) 2 5*				AND ZP, X 2 4	ROL ZP, X 2 6	RMB3 ZP 2 5	SEC Implied 1 2	AND ABS, Y 3 4*				AND ABS, X 3 4*	ROL ABS, X 3 7	BBR3 ZP 3 5**	3
4	RTI Implied 1 6	EOR (IND, X) 2 6				EOR ZP 2 3	LSR ZP 2 5	RMB4 ZP 2 5	PHA Implied 1 3	EOR IMM 2 2	LSR Accum 1 2		JMP ABS 3 3	EOR ABS 3 4	LSR ABS 3 6	BBR4 ZP 3 5**	4
5	BVC Relative 2 2**	EOR (IND), Y 2 5*				EOR ZP, X 2 4	LSR ZP, X 2 6	RMB5 ZP 2 5	CLI Implied 1 2	EOR ABS, Y 3 4*				EOR ABS, X 3 4*	LSR ABS, X 3 7	BBR5 ZP 3 5**	5
6	RTS Implied 1 6	ADC (IND, X) 2 6				ADC ZP 2 3	ROR ZP 2 5	RMB6 ZP 2 5	PLA Implied 1 4	ADC IMM 2 2	ROR Accum 1 2		JMP Indirect 3 5	ADC ABS 3 4	ROR ABS 3 6	BBR6 ZP 3 5**	6
7	BVS Relative 2 2**	ADC (IND, Y) 2 5*				ADC ZP, X 2 4	ROR ZP, X 2 6	RMB7 ZP 2 5	SEI Implied 1 2	ADC ABS, Y 3 4*				ADC ABS, X 3 4*	ROR ABS, X 3 7	BBR7 ZP 3 5**	7
8		STA (IND, X) 2 6			STY ZP 2 3	STA ZP 2 3	STX ZP 2 3	SMB0 ZP 2 5	DEY Implied 1 2		TXA Implied 1 2		STY ABS 3 4	STA ABS 3 4	STX ABS 3 4	BBS0 ZP 3 5**	8
9	BCC Relative 2 2**	STA (IND, Y) 2 6			STY ZP, X 2 4	STA ZP, X 2 4	STX ZP, Y 2 4	SMB1 ZP 2 5	TYA Implied 1 2	STA ABS, Y 3 5	TXS Implied 1 2			STA ABS, X 3 5		BBS1 ZP 3 5**	9
A	LDY IMM 2 2	LDA (IND, X) 2 6	LDX IMM 2 2		LDY ZP 2 3	LDA ZP 2 3	LDX ZP 2 3	SMB2 ZP 2 5	TAY Implied 1 2	LDA IMM 2 2	TAX Implied 1 2		LDY ABS 3 4	LDA ABS 3 4	LDX ABS 3 4	BBS2 ZP 3 5**	A
B	BCS Relative 2 2**	LDA (IND), Y 2 5*			LDY ZP, X 2 4	LDA ZP, X 2 4	LDX ZP, Y 2 4	SMB3 ZP 2 5	CLV Implied 1 2	LDA ABS, Y 3 4*	TSX Implied 1 2		LDY ABS, X 3 4*	LDA ABS, X 3 4*	LDX ABS, Y 3 4*	BBS3 ZP 3 5**	B
C	CPY IMM 2 2	CMP (IND, X) 2 6			CPY ZP 2 3	CMP ZP 2 3	DEC ZP 2 5	SMB4 ZP 2 5	INY Implied 1 2	CMP IMM 2 2	DEX Implied 1 2		CPY ABS 3 4	CMP ABS 3 4	DEC ABS 3 6	BBS4 ZP 3 5**	C
D	BNE Relative 2 2**	CMP (IND), Y 2 5*				CMP ZP, X 2 4	DEC ZP, X 2 6	SMB5 ZP 2 5	CLD Implied 1 2	CMP ABS, Y 3 4*				CMP ABS, X 3 4*	DEC ABS, X 3 7	BBS5 ZP 3 5**	D
E	CPX IMM 2 2	SBC (IND, X) 2 6			CPX ZP 2 3	SBC ZP 2 3	INC ZP 2 5	SMB6 ZP 2 5	INX Implied 1 2	SBC IMM 2 2	NOP Implied 1 2		CPX ABS 3 4	SBC ABS 3 4	INC ABS 3 6	BBS6 ZP 3 5**	E
F	BEQ Relative 2 2**	SBC (IND), Y 2 5*				SBC ZP, X 2 4	INC ZP, X 2 6	SMB7 ZP 2 5	SED Implied 1 2	SBC ABS, Y 3 4*				SBC ABS, X 3 4*	INC ABS, X 3 7	BBS7 ZP 3 5**	F
	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	

0

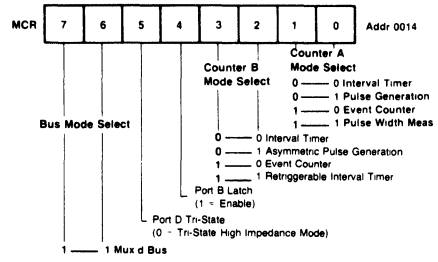
BRK	—OP Code
0 Implied	—Addressing Mode
1 7	—Instruction Bytes; Machine Cycles

*Add 1 to N if page boundary is crossed.
**Add 1 to N if branch occurs to same page;
add 2 to N if branch occurs to different page.

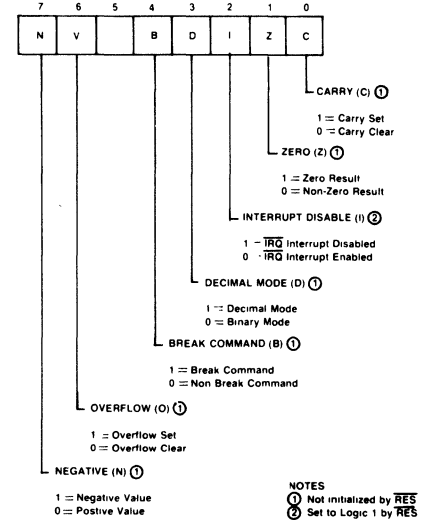
APPENDIX B
KEY REGISTER SUMMARY



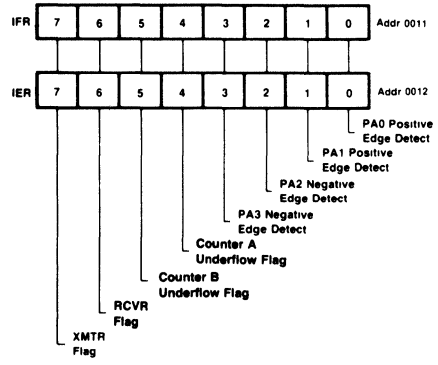
CPU Registers



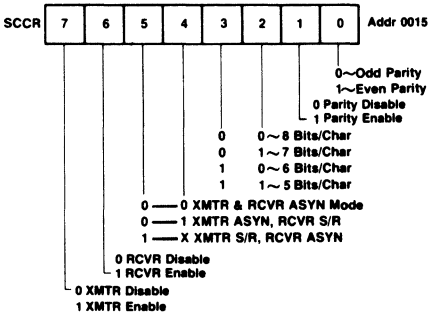
Mode Control Register



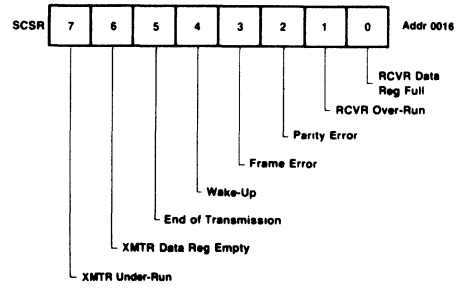
Processor Status Register



Interrupt Enable and Flag Registers



Serial Communications Control Register



Serial Communications Status Register

APPENDIX C
ADDRESS ASSIGNMENTS/MEMORY MAPS/PIN FUNCTIONS

C.1 I/O AND INTERNAL REGISTER ADDRESSES

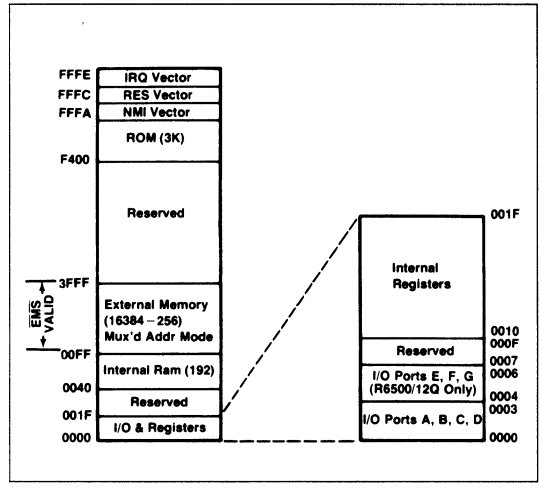
ADDRESS (HEX)	READ	WRITE
001F	— —	— —
1E	Lower Counter B	Upper Latch B, Cntr B←Latch B, CLR Flag
1D	Upper Counter B	Upper Latch B, Latch C←Latch B
1C	Lower Counter B, CLR Flag	Lower Latch B.
1B	— —	— —
1A	Lower Counter A	Upper Latch A, Cntr A←Latch A, CLR Flag
19	Upper Counter A	Upper Latch A
18	Lower Counter A, CLR Flag	Lower Latch A
17	Serial Receiver Data Register	Serial Transmitter Data Register
16	Serial Comm. Status Register	Serial Comm. Status Reg. Bits 4 & 5 only
15	Serial Comm. Control Register	Serial Comm. Control Register
14	Mode Control Register	Mode Control Register
13	— —	— —
12	Interrupt Enable Register	Interrupt Enable Register
11	Interrupt Flag Register	— —
10	Read FF	Clear Int Flag (Bits 0-3 only, Write 0's only)
0F	— —	— —
0E	— —	— —
0D	— —	— —
0C	— —	— —
0B	— —	— —
0A	— —	— —
09	— —	— —
08	— —	— —
07	— —	— —
06	Port G*	Port G*
05	Port F*	Port F*
04	Port E *	Port E*
03	— —	— —
02	— —	— —
01	Port B	Port B
0000	Port A	Port A

NOTE: *R65F12 Only

C.2 MULTIPLE FUNCTION PIN ASSIGNMENTS— PORT C AND PORT D

PIN NUMBER		I/O PORT FUNCTION	MULTIPLEXED PORT FUNCTION
R65F11	R65F12	REPLACED	
4	25	PC0	A0
5	26	PC1	A1
6	27	PC2	A2
7	28	PC3	A3
8	29	PC4	A12
9	30	PC5	R/W
10	31	PC6	A13
11	32	PC7	EMS
19	40	PD0	A4/D0
18	39	PD1	A5/D1
17	38	PD2	A6/D2
16	37	PD3	A7/D3
15	36	PD4	A8/D4
14	35	PD5	A9/D5
13	34	PD6	A10/D6
12	33	PD7	A11/D7

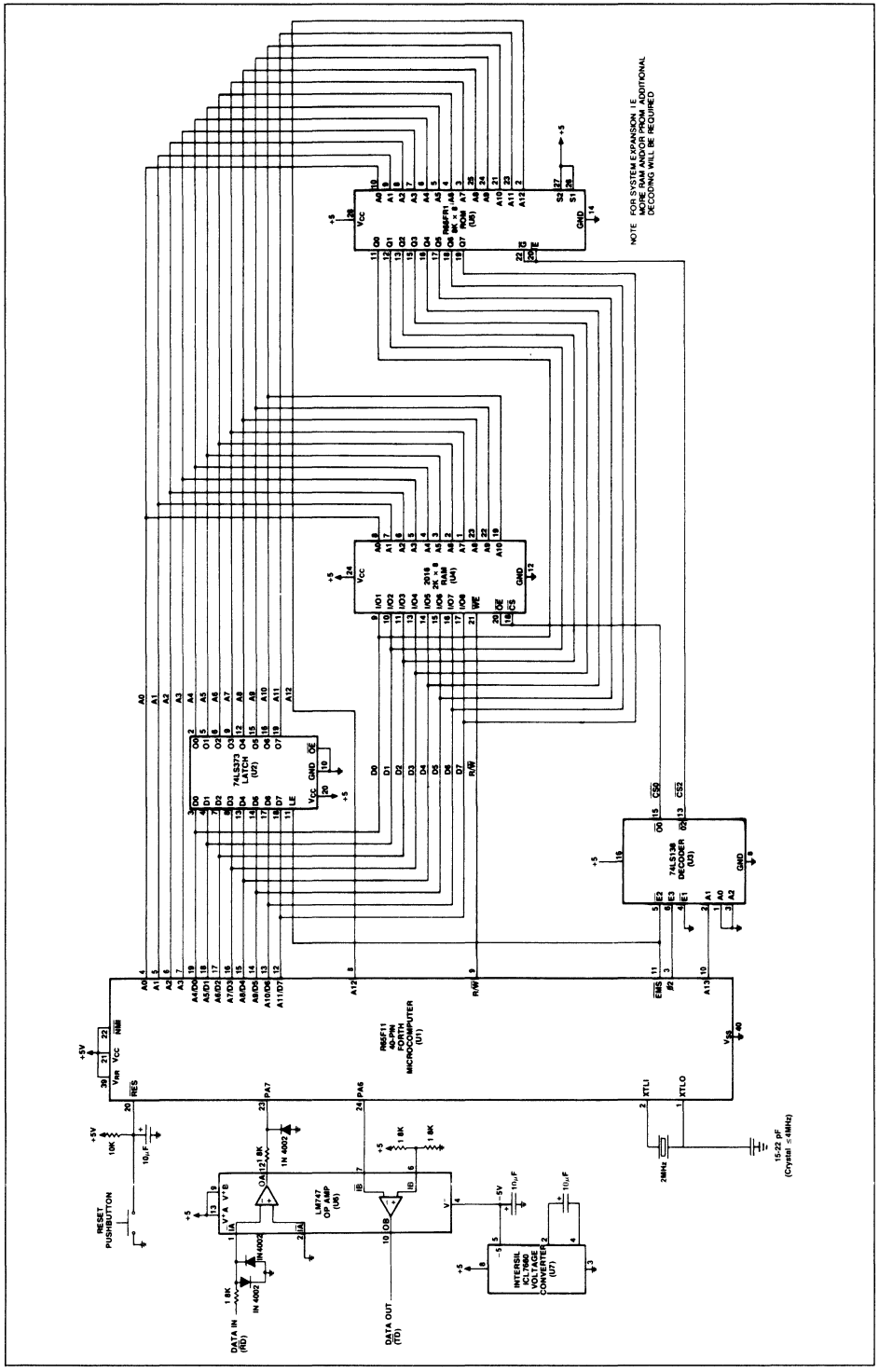
C.3 MULTIPLEXED MODE MEMORY MAP



C.4 SYSTEM VARIABLES IN RAM

ADDRESS	NAME	COLD START VALUE	WARM START VALUE
0040	IRQVEC	(COLD)	—
0042	NMIVEC	(COLD)	—
0044	UKEY	(INK)	(INK)
0046	UEMIT	(OUT)	(OUT)
0048	UP	0300	0300
004A	INTFLG	00	00
004B	(W-1)	6C	6C
004C	W	—	—
004E	IP	—	—
0050	(N-1)	—	—
0051	N	—	—
0059	XSAVE	—	—
005B	INTVEC	(COLD)	—
005D	TOS	—	—
0300	TIB	0380	0380
0302	R0	00FF	00FF
0304	S0	00C2	00C2
0306	UC/L	0050	—
0308	UPAD	037E	—
030A	UR/W	(DISK)	—
030C	BASE	0010	—
030E	CLD/WRM	—	—
0310	IN	—	—
0312	DPL	—	—
0314	HLD	—	—
0316	DISKNO	—	—
0318	CURCYL	—	—
031C	B/SIDE	—	—

APPENDIX D
TYPICAL MINIMUM HOOKUP



APPENDIX E
ELECTRICAL SPECIFICATIONS

MAXIMUM RATINGS*

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC} & V_{RR}	−0.3 to +7.0	Vdc
Input Voltage	V_{IN}	−0.3 to +7.0	Vdc
Operating Temperature Range, Commercial	T_A	T_L to T_H 0 to +70	°C
Storage Temperature	T_{STG}	−55 to +150	°C

***NOTE:** Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the other sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

(V_{CC} = 5.0V ±5%, V_{RR} = V_{CC}; V_{SS} = 0V; T_A = 0° to 70°, unless otherwise specified)

Parameter	Symbol	Min	Typ[1]	Max	Unit	Test Conditions
RAM Standby Voltage (Retention Mode)	V_{RR}	3.0		V_{CC}	V	
RAM Standby Current (Retention Mode)	I_{RR}	—	4	—	mA	T_A = 25°C
Input High Voltage All Except XTLI XTLI	V_{IH}	 +2.0 +4.0	 — —	 V_{CC} V_{CC}	V	
Input Low Voltage	V_{IL}	−0.3	—	+0.8	V	
Input Leakage Current $\overline{RES}$, $\overline{NMI}$	I_{IN}	—	—	±10.0	μA	V_{IN} = 0 to 5.0V
Input Low Current PA, PB, PC, PD, PF[3], PG[3]	I_{IL}	—	−1.0	−1.6	mA	V_{IL} = 0.4V
Output High Voltage (Except XTLO)	V_{OH}	+2.4	—	V_{CC}	V	I_{LOAD} = −100 μA
Output Low Voltage	V_{OL}	—	—	+0.4	V	I_{LOAD} = 1.6 mA
I/O Port Pull-Up Resistance PA0–PA7, PB0–PB7, PC0–PC7, PF0–PF7[3], PG0–PG7[3]	R_L	3.0	6.0	11.5	Kohm	
Output Leakage Current (Three-State Off)	I_{OUT}	—	—	±10	μA	
Darlington Current Drive PE[3]	I_{OH}	−1.0	—	—	mA	V_{OUT} = 1.5V
Input Capacitance XTLI, XTLO All Others	C_{IN}	 — —	 — —	 50 10	pF	T_A = 25°C V_{IN} = 0V f = 1.0 MHz
Output Capacitance (Three-State Off)	C_{OUT}	—	—	10	pF	T_A = 25°C V_{IN} = 0V f = 1.0 MHz
Power Dissipation (Outputs High)	P_D	—		1000	mW	T_A = 25°C

Notes:
1. Typical values measured at T_A = 25°C and V_{CC} = 5.0V.
2. Negative sign indicates outward current flow, positive indicates inward flow.
3. R65F12 only.

APPENDIX F
TIMING REQUIREMENTS AND CHARACTERISTICS

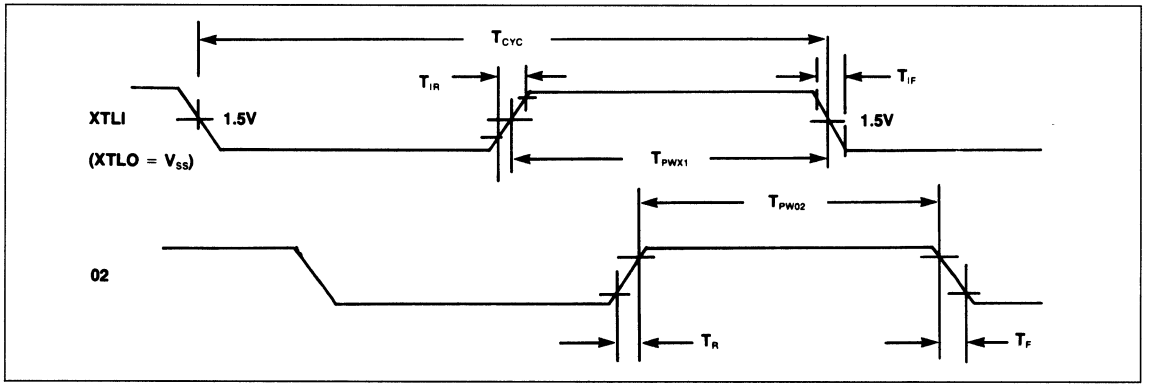
F.1 GENERAL NOTES

1. V_{CC} = 5V ± 5%, 0°C ≤ TA ≤ 70°C
2. A valid V_{CC} – RES sequence is required before proper operation is achieved.
3. All timing reference levels are 0.8V and 2.0V, unless otherwise specified.
4. All time units are nanoseconds, unless otherwise specified.
5. All capacitive loading is 130pf maximum, except as noted below:

   PA, PB, PE, PF, PG — 50pf maximum

F.2 CLOCK TIMING

SYMBOL	PARAMETER	1 MHz		2 MHz	
		MIN	MAX	MIN	MAX
T_{CYC}	Cycle Time	1000	10 μs	500	10 μs
T_{PWX1}	XTLI Input Clock Pulse Width XTLO = VSS	500 ± 25	—	250 ± 10	—
T_{PW02}	Output Clock Pulse Width at Minimum T_{CYC}	T_{PWX1}	T_{PWX1} ± 25	T_{PWX1}	T_{PWX1} ± 20
T_R, T_F	Output Clock Rise, Fall Time	—	25	—	15
T_{IR}, T_{IF}	Input Clock Rise, Fall Time	—	10	—	10



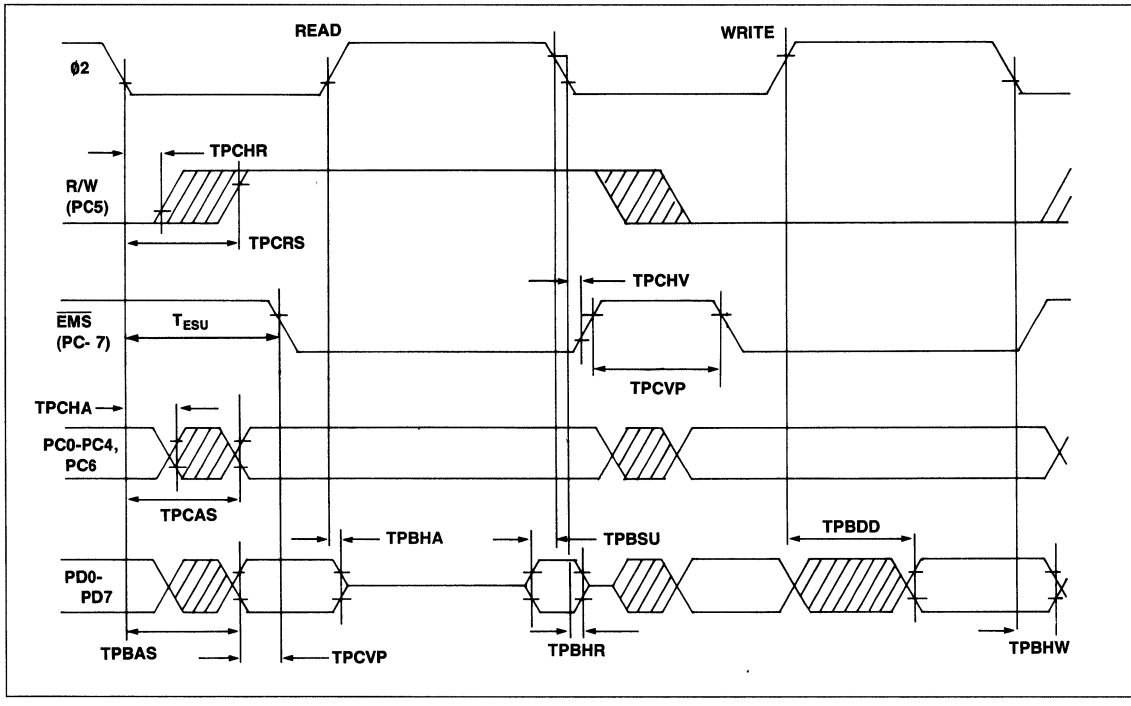
F.3 MULTIPLEXED MODE TIMING—PC AND PD

(MCR 5 = 1, MCR 6 = 1, MCR 7 = 1)

SYMBOL	PARAMETER	1 MHz		2 MHz	
		MIN	MAX	MIN	MAX
T_{PCRS}	(PC5) R/W Setup Time	—	225	—	140
T_{PCAS}	(PC0-PC4, PC6) Address Setup Time	—	225	—	140
T_{PBAS}	(PD) Address Setup Time	—	225	—	140
T_{PBSU}	(PD) Data Setup Time	50	—	35	—
T_{PBHR}	(PD) Data Read Hold Time	10	—	10	—
T_{PBHW}	(PD) Data Write Hold Time	30	—	30	—
T_{PBDD}	(PD) Data Output Delay	—	175	—	150
T_{PCHA}	(PC0-PC4, PC6) Address Hold Time	30	—	30	—
T_{PBHA}	(PD) Address Hold Time	10	100	10	80
T_{PCHR}	(PC5) R/W Hold Time	30	—	30	—
T_{PCHV}	(PC7) EMS Hold Time	10	—	10	—
T_{PCVD}[1]	(PC7) Address to EMS Delay Time	30	—	30	—
T_{PCVP}	(PC7) EMS Stabilization Time	30	—	30	—
T_{ESU}	$\overline{EMS}$ Set Up Time	—	350	—	210

NOTE 1 Values assume PC0-PC4, PC6 and PC7 have the same capacitive load

F.3.1 Multiplex Mode Timing Diagram

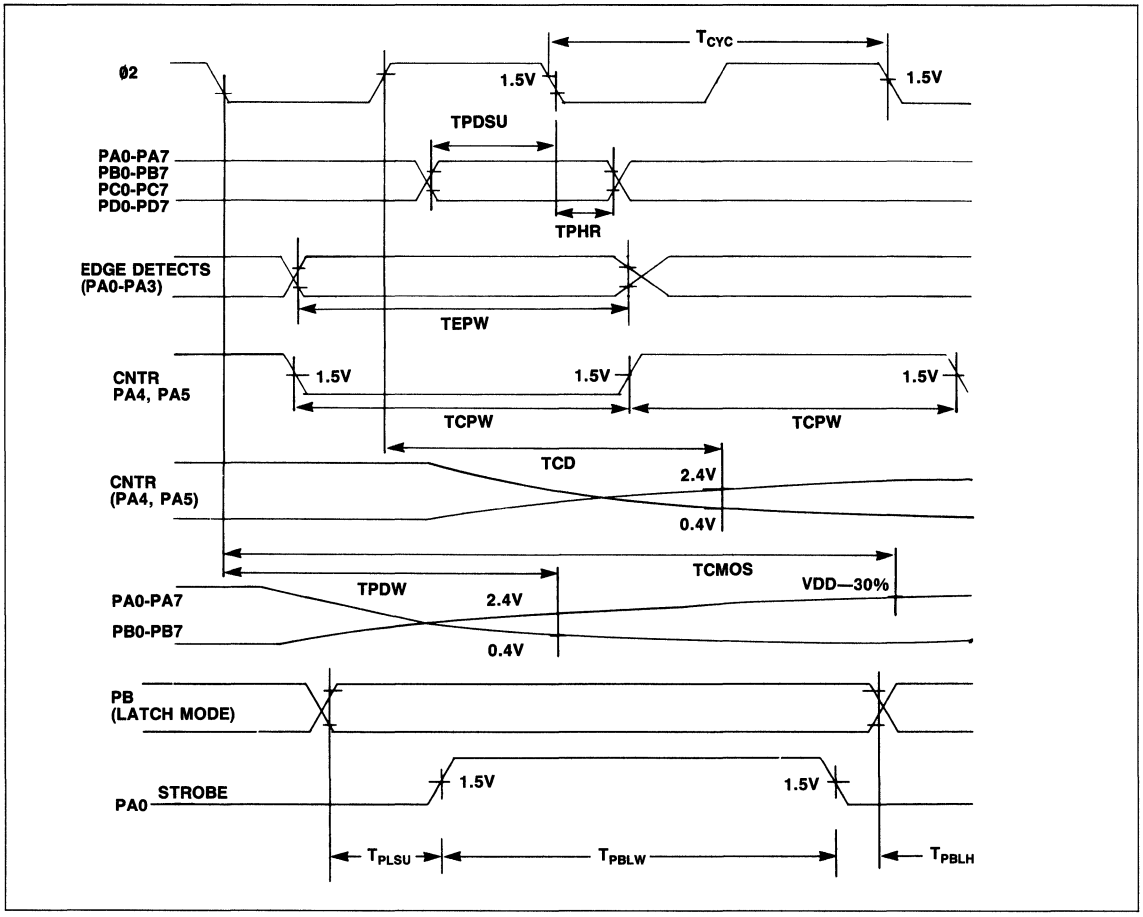


F.4 I/O, EDGE DETECT, COUNTERS, AND SERIAL I/O TIMING

SYMBOL	PARAMETER	1 MHz		2 MHz	
		MIN	MAX	MIN	MAX
	Internal Write to Peripheral Data Valid				
T_{PDW}(1)	PA, PB TTL	—	500	—	500
T_{CMOS}(1)	PA, PB CMOS	—	1000	—	1000
	Peripheral Data Setup Time				
T_{PDSU}	PA, PB	200	—	200	—
	Peripheral Data Hold Time				
T_{PHR}	PA, PB	75	—	75	—
T_{EPW}	PA0-PA3 Edge Detect Pulse Width	T_{CYC}	—	T_{CYC}	—
	Counters A and B				
T_{CPW}	PA4, PA5 Input Pulse Width	T_{CYC}	—	T_{CYC}	—
T_{CD}(1)	PA4, PA5 Output Delay	—	500	—	500
	Port B Latch Mode				
T_{PBLW}	PA0 Strobe Pulse Width	T_{CYC}	—	T_{CYC}	—
T_{PLSU}	PB Data Setup Time	175	—	150	—
T_{PBLH}	PB Data Hold Time	30	—	30	—
	Serial I/O				
T_{PDW}(1)	PA6 XMTR TTL	—	500	—	500
T_{CMOS}(1)	PA6 XMTR CMOS	—	1000	—	1000
T_{CPW}	PA4 RCVR S/R Clock Width	4 T_{CYC}	—	4 T_{CYC}	—
T_{PDW}(1)	PA4 XMTR Clock—S/R Mode (TTL)	—	500	—	500
T_{CMOS}(1)	PA4 XMTR Clock—S/R Mode (CMOS)	—	1000	—	1000

NOTE 1. Maximum Load Capacitance: 50pF Passive Pull-Up Required

F.4.1 I/O Edge Detect, Counter, and Serial I/O Timing



APPENDIX G
INCLUDED FORTH FUNCTIONS IN ROM

BANKEXECUTE	BANKEEC!	BANKC@	BANKC!
EEC!	•	.R	D.
?	#S	• #	SIGN
D.R	<#	SPACES	SEEK
#>	DWRITE	DREAD	SELECT
INIT	M/MOD	*/	*/MOD
DISK	/	/MOD	*
MOD	M*	MAX	MIN
M/	ABS	D+-	+-
DABS	COLD	(NUMBER)	HOLD
S->D	ERASE	FILL	QUERY
BLANKS	(.")	-TRAILING	TYPE
EXPECT	DECIMAL	HEX	-DUP
COUNT	PICK	ROT	>
SPACE	U<	=	-
<	1-	2+	1+
2-	C/L	HLD	DPL
PAD	CLD/WRM	BASE	UR/W
IN	UC/L	R0	S0
UPAD	BL	4	3
TIB	1	0	C!
2	C@	@	TOGGLE
!	BOUNDS	2DUP	DUP
+!	2DROP	DROP	OVER
SWAP	NEGATE	D+	+
DNEGATE	0=	R	R>
0<	LEAVE	;S	RP@
>R	SP!	SP@	XOR
RP!	AND	U/	U*
OR	CR	?TERMINAL	KEY
CMOVE	ENCLOSE	(FIND)	DIGIT
EMIT	(+LOOP)	(LOOP)	0BRANCH
(DO)	EXECUTE	CLIT	LIT
BRANCH			

Rockwell

R65FRx AND R65FKx RSC FORTH DEVELOPMENT AND KERNEL ROMS

INTRODUCTION

The Rockwell Single Chip (RSC) FORTH System can be configured using the R65F11, R65F12 microcomputers or the R6501Q ROM-less microcomputer. One of these microcomputers, when used in conjunction with a development ROM and a FORTH kernel ROM, provide the designer with maximum flexibility when developing FORTH applications.

RSC-FORTH is based on the popular fig-FORTH model with extensions. The R65F11 and R65F12 both have the kernel of the high level Rockwell Single Chip RSC-FORTH language contained in the preprogrammed ROM. The R65FK2 and R65FK3 Kernel ROMs are preprogrammed ROMs for use with the R6501Q when developing larger applications requiring more memory and I/O line support. All of the run time functions of the RSC-FORTH are contained in these ROMs, including 16- and 32-bit mathematical, logical and stack manipulation, plus memory and input/output operators. The RSC-FORTH Operating System allows an external user program written in RSC-FORTH or Assembly Language to be executed from external EPROM, or development of such a program under the control of the R65FR1, R65FR2 or R65FR3 RSC-FORTH Development ROMs.

This document describes five different RSC-FORTH system configurations using the development and kernel ROMs.

ORDERING INFORMATION

Part No.	Description
R65FR1P	FORTH Development ROM for R65F11 or R65F12
R65FR2P	FORTH Development ROM for R6501Q
R65FR3P	FORTH Development ROM for R6501Q
R65FK2P	FORTH Kernel ROM for R6501Q
R65FK3P	FORTH Kernel ROM for R6501Q
R65F11P	40-Pin FORTH Based Microcomputer at 1 MHz
R65F11AP	40-Pin FORTH Based Microcomputer at 2 MHz
R65F12Q	64-Pin FORTH Based Microcomputer at 1 MHz
R65F12AQ	64-Pin FORTH Based Microcomputer at 2 MHz
R6501Q	64-Pin One-Chip Microprocessor at 1 MHz
R6501AQ	64-Pin One-Chip Microprocessor at 2 MHz
Order No.	**Description**
2145	R6501Q One-Chip Microprocessor Product Description
2146	R65F11 and R65F12 FORTH Based Microcomputer Product Description
2148	RSC-FORTH User's Manual
2162	Application Note: A Low-Cost Development Module for the R65F11 FORTH Microcomputer

FEATURES

- R65FR1 FORTH Development ROM
  - —8K ROM
  - —Addressable from $2000 through $3FFF in FORTH development configuration memory map
  - —R65F11 and R65F12 compatible
  - —Operates in the R65F11/F12 FORTH development configuration
- R65FR2 FORTH Development ROM
  - —8K ROM
  - —Addressable from $4000 through $5FFF in the FORTH development configuration memory map
  - —R6501Q compatible for use in emulation of the R65F11/F12 FORTH development configuration
- R65FR3 FORTH Development ROM
  - —8K ROM
  - —Addressable from $C000 through $DFFF in the FORTH development configuration memory map
  - —Operates in the R6501Q FORTH development configuration
- R65FK2 FORTH Kernel ROM
  - —4K ROM
  - —Addressable from $F400 through $FFFF in the FORTH development configuration memory map
  - —R6501Q compatible for use in the emulation of the R65F11/F12 FORTH development configuration
  - —Replaces the FORTH kernel contained in the R65F11 and R65F12 microcomputers during development
- R65FK3 FORTH Kernel ROM
  - —4K ROM
  - —Addressable from $F400 through $FFFF in the FORTH development and production configuration memory maps
  - —R6501Q compatible
  - —Operates in the R6501Q FORTH development and production configurations

RSC-FORTH SYSTEM CONFIGURATIONS

The three configurations of the RSC-FORTH System are identified by the CPU-Development ROM combinations listed below:

RSC-FORTH System Configurations

CPU	Kernel ROM	Development ROM	RSC Configuration
R65F11	none	R65FR1	1
R65F12	none	R65FR1	1
R6501Q	R65FK2	R65FR2	2
R6501Q	R65FK3	R65FR3	3

RSC-FORTH CONFIGURATION 1 (R65FR1)

R65F11/R65F12 DEVELOPMENT AND PRODUCTION

The RSC-FORTH Configuration 1 provides the designer with a FORTH development and application environment at a minimal cost. The application program is developed using an R65F11 or R65F12 microcomputer, an R65FR1 Development ROM and external RAM. Up to 8K bytes of RAM space is available using this configuration. However, Configuration 1 is limited to 5K or less bytes of RAM during development. This is the result of allocating 2K bytes of RAM for disk buffers and at least 1K bytes of RAM for the "Program heads". The program heads are contained in a dictionary containing the Name (NFA), Link Field Address (LFA) and the Parameter Field Address Pointer (PFA). This dictionary is a list of FORTH word words and user-defined FORTH words used in the development of a FORTH program and is not present during the execution of the FORTH program.

Although programs may reside in the upper 8K bytes of memory area, normally filled by the R65FR1 Development ROM, it is difficult to develop code for that area using this configuration of the RSC-FORTH System.

The difference in using the R65F11 or the R65F12 is in the number of I/O lines available to the user. The R65F11 supports 16 I/O lines, the R65F12 supports 40 I/O lines.

Figure 1 shows the development and production configurations for the R65F11/F12. Configurations 1A and 1B list the features, memory maps, and the relationship of the R65F11 and R65F12 to the R65FR1 Development ROM in the development and production environment.

3

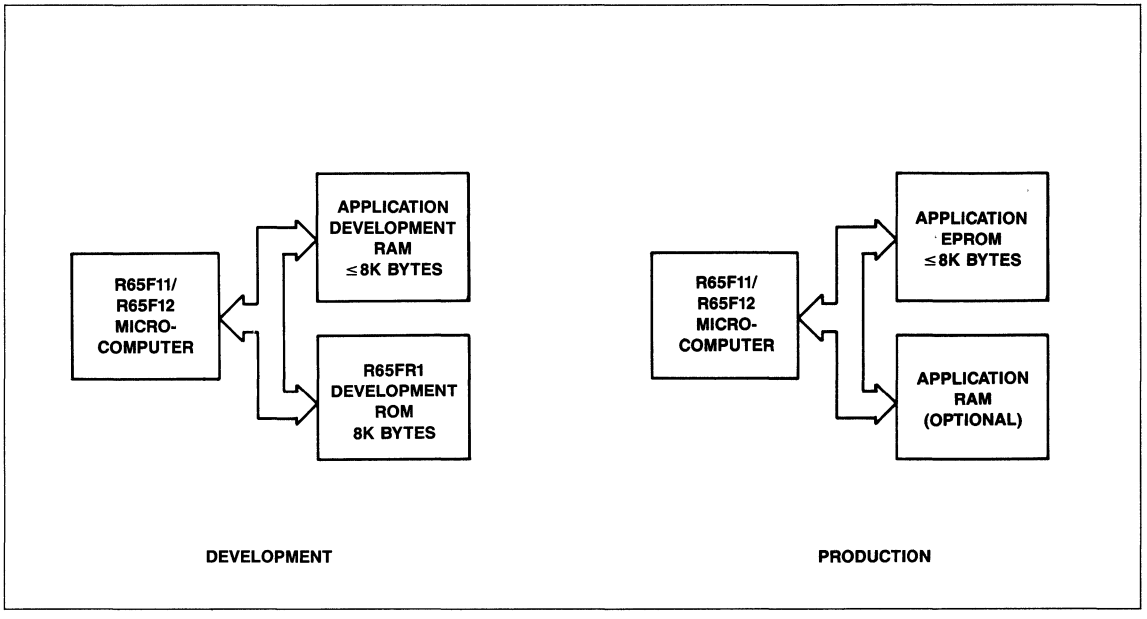


Figure 1. R65FR1 Configuration 1 Block Diagram

CONFIGURATION 1A CONSIDERATIONS

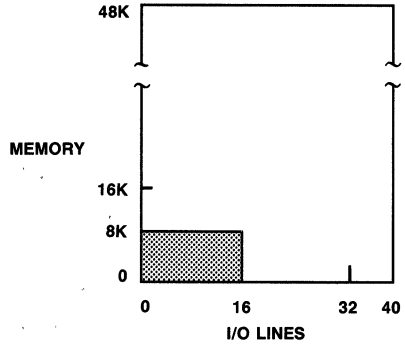
Features
- 8K Bytes of User Memory
- 16 I/O Lines

Device Configuration

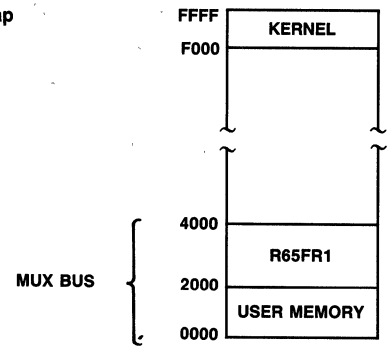
	DEVELOPMENT	PRODUCTION
R65F11 Microcomputer	✓	✓
R65FR1 Development ROM	✓	

User Memory—I/O Resource Matrix

User memory may be a mix of ROM, EEROM, UVPROM or RAM.



Memory Map



CONFIGURATION 1B CONSIDERATIONS

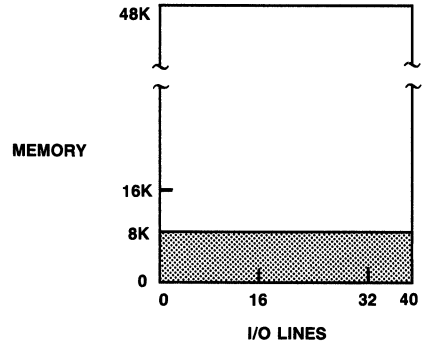
Features
- 8K Bytes of User Memory
- 40 I/O Lines

Device Configuration

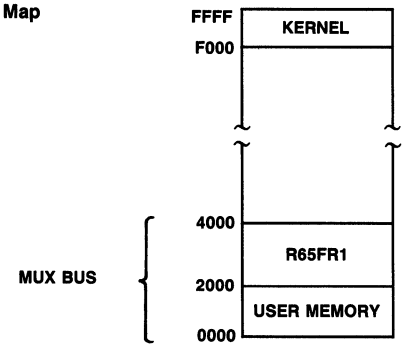
	DEVELOPMENT	PRODUCTION
R65F12 Microcomputer	✓	✓
R65FR1 Development ROM	✓	

User Memory—I/O Resource Matrix

User memory may be a mix of ROM, EEROM, UVPROM or RAM.



Memory Map



RSC-FORTH CONFIGURATION 2 (R65FR2, R65FK2)

R6501Q DEVELOPMENT AND R65F11/F12 PRODUCTION

The RSC-FORTH Configuration 2 provides the designer with the capability of using the full 16K bytes of external address space of the R65F11 and R65F12.

The R6501Q ROM-less microprocessor, when used with the R65FK2 Kernel ROM and the R65FR2 Development ROM, emulates the operation of the R65F11/F12. Because of the greater address space of the R6501Q, the R65FR2 Development ROM can be relocated to address $4000 and the disk buffers and HEADS program to $6000. This expands the available user memory space to 16K bytes, $0000 through $3FFF.

Using this configuration, the application program can be developed using the R6501Q and then later installed in an R65F11 or R65F12 microcomputer without modification.

Figure 2 shows the development and production configuration for the R6501Q. Configurations 2A and 2B list the features, memory maps, and the relationship of the R6501Q to the R65FR2 Development ROM and R65FK2 Kernel ROM in the development and production environment. Figure 3 is a schematic of the R6501Q, R65FR2, R65FK2 development setup.

3

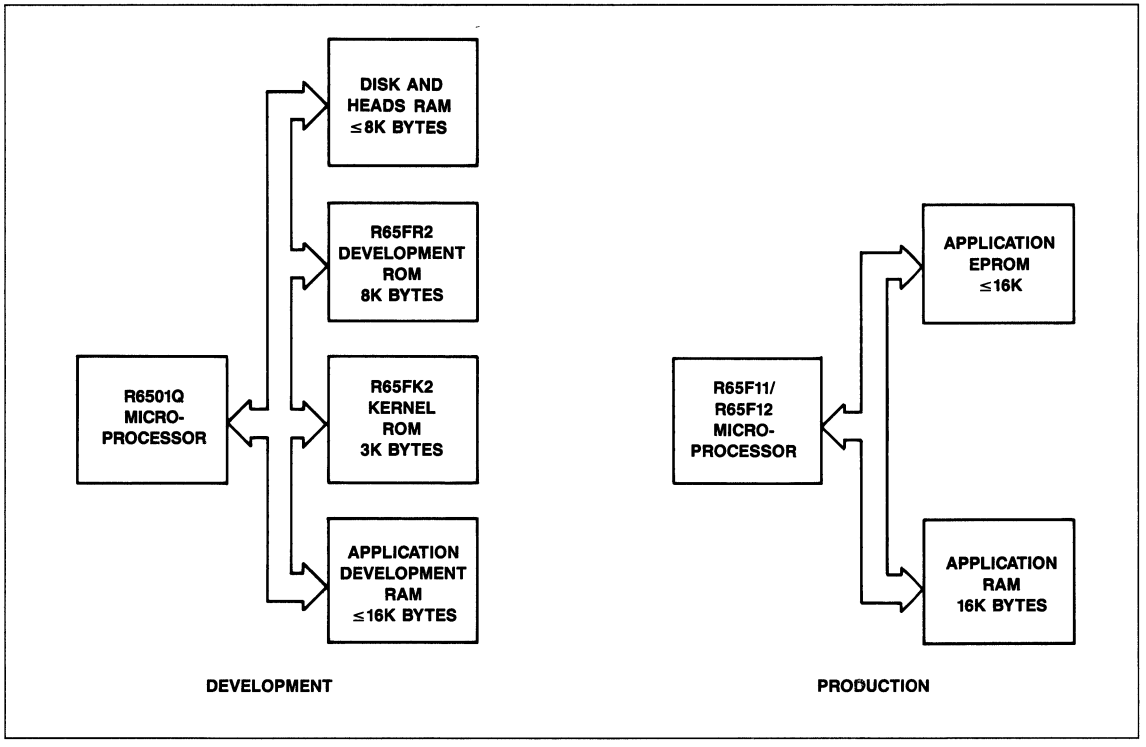


Figure 2. R65FR2 and R65FK2 Configuration 2 Block Diagrams

CONFIGURATION 2A CONSIDERATIONS

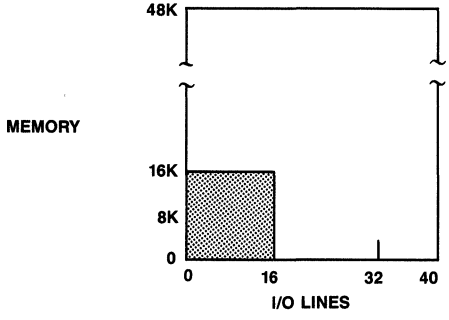
Features
- 16K Bytes of User "Headerless" Memory
- 16 I/O Lines

Device Configuration

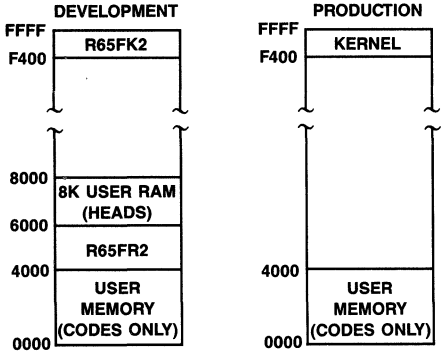
	DEVELOPMENT	PRODUCTION
R65F11 Microcomputer		✓
R6501Q Microprocessor	✓	
R65FR2 Development ROM	✓	
R65FK2 Kernel ROM	✓	

Memory—I/O Matrix

If floppy disk is used in the application, space for the disk buffers must be allocated in memory from $0500 through $3FFF or $6000 through $7FFF. User memory can be a mix of ROM, EEROM, UVROM or RAM.



Memory Maps



CONFIGURATION 2B CONSIDERATIONS

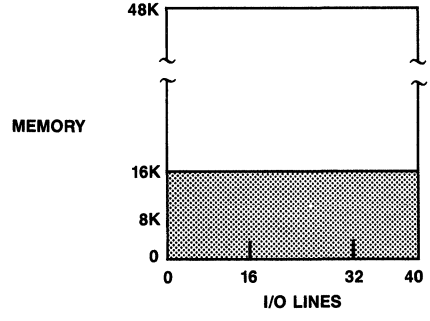
Features
- 16K Bytes of User "Headerless" Memory
- 40 I/O Lines

Device Configuration

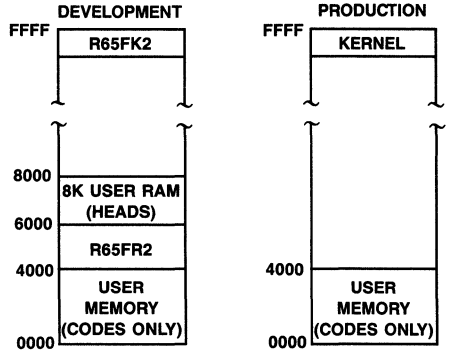
	DEVELOPMENT	PRODUCTION
R65F12 Microcomputer		✓
R6501Q Microprocessor	✓	
R65FR2 Development ROM	✓	
R65FK2 Kernel ROM	✓	

Memory—I/O Matrix

If floppy disk is used in the application, space for the disk buffers must be allocated in memory $0000 through $3FFF. User memory can be a mix of ROM, EEROM, UVROM or RAM.



Memory Maps



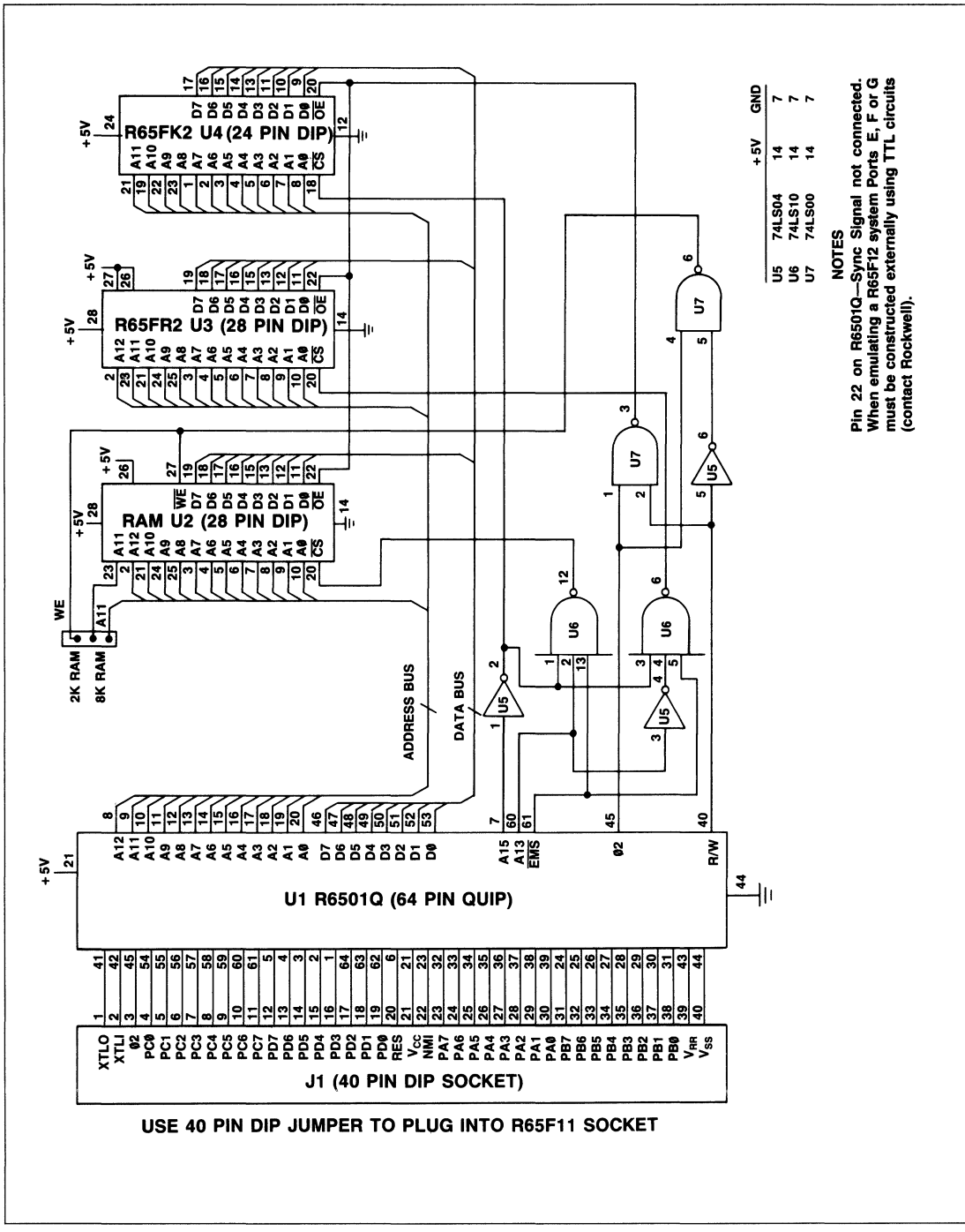


Figure 3. R6501Q, R65FR2 and R65K2 Application Configuration Schematic

3

RSC-FORTH CONFIGURATION 3 (R65FR3, R65FK3)

R6501Q BASED SYSTEM DEVELOPMENT AND PRODUCTION

The RSC-FORTH Configuration 3 is designed for those applications which require a larger amount of ROM or RAM space than the R65F11 or R65F12 can provide.

In the development configuration, the user is provided with up to 48K bytes of memory. The user memory is located from $0000 through $BFFF. The program heads will use some of this area but the user will still have considerably more memory space available then in the previous configurations.

The production configuration provides up to 56K bytes of user memory. This is due to the fact that the R65FR3 Development ROM, used in the development configuration, is not required in the production configuration and releases the 8K bytes of memory space. This memory is located at $C000 through $DFFF.

Figure 4 shows the development and production configurations for the R6501Q. Configuration 3 lists the features, memory maps, and the relationship of the R6501Q to the R65FR3 Development ROM and the R65FK3 Kernel ROM in the development and production environment.

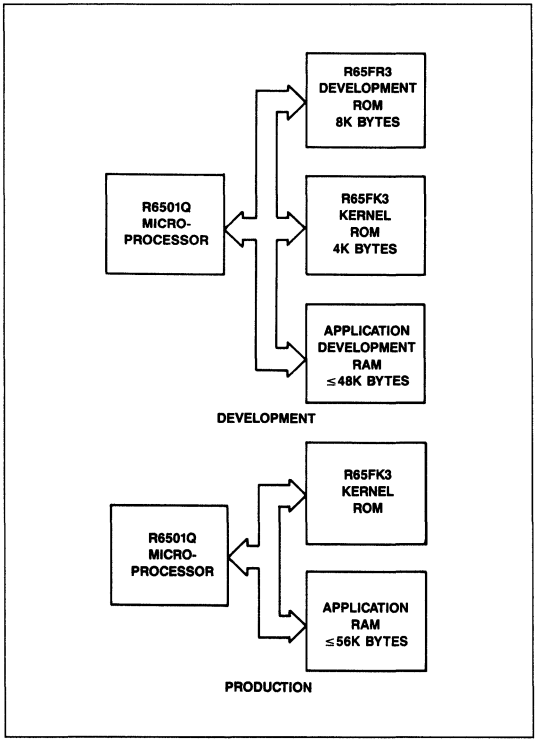


Figure 4. R65FR3 and R65FK3 Configuration 3 Block Diagrams

CONFIGURATION 3 CONSIDERATIONS

Features

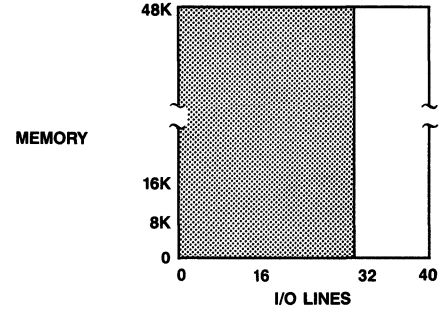
- R6501Q w/FORTH
- 48K Bytes of User Memory
- 30 I/O Lines

Device Configuration

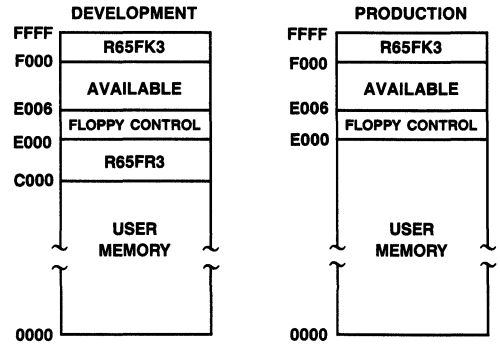
	DEVELOPMENT	PRODUCTION
R6501Q Microcomputer	✓	✓
R65FK3 Development ROM	✓	
R65FR3 Kernel ROM	✓	✓

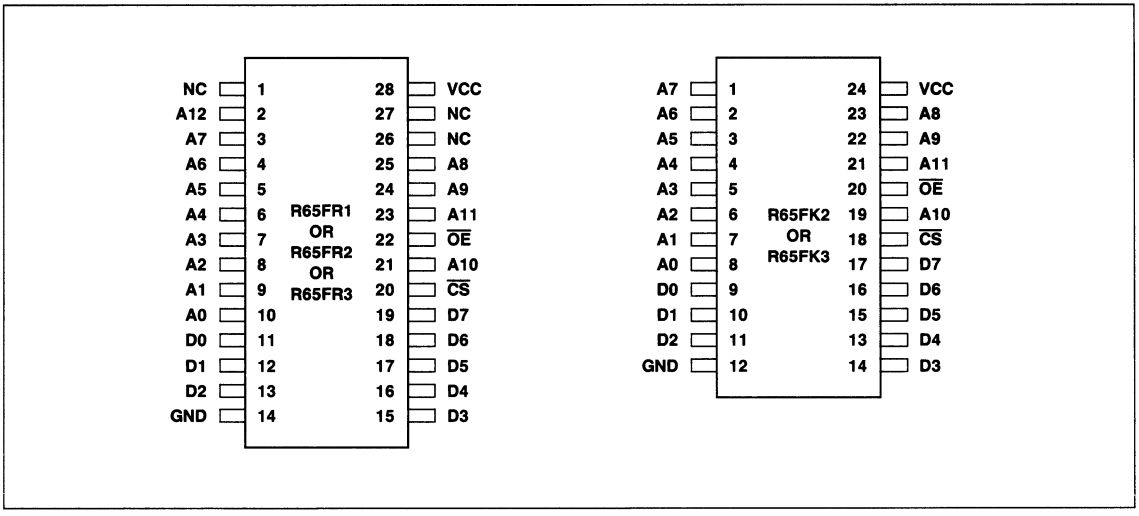
User Memory—I/O Resource Matrix

All ports act as I/O ports. Memory is on the bus. PC6 & PC7 (I/O lines) are assigned to memory. User memory can be a mix of ROM, EEROM, UVPROM or RAM.



Memory Maps





RSC-FORTH ROM Pin Assignments

Rockwell

R6501Q
ONE-CHIP MICROPROCESSOR

SECTION 1
INTRODUCTION

1.1 FEATURES OF THE R6501Q

- Enhanced 6502 CPU
  - —Four new bit manipulation instructions
    - Set Memory Bit (SMB)
    - Reset Memory Bit (RMB)
    - Branch on Bit Set (BBS)
    - Branch on Bit Reset (BBR)
  - —Decimal and binary arithmetic modes
  - —13 addressing modes
  - —True indexing
- 192-byte static RAM
- 32 bidirectional, TTL-compatible I/O lines (four ports)
- One 8-bit port may be tri-stated under software control
- One 8-bit port may have latched inputs under software control
- Two 16-bit programmable counter/timers, with latches
  - —Pulse width measurement
  - —Asymmetrical pulse generation
  - —Pulse generation
  - —Interval timer
  - —Event counter
  - —Retriggerable interval timer
- Serial port
  - —Full-duplex asynchronous operation mode
  - —Selectable 5- to 8-bit characters
  - —Wake-up feature
  - —Synchronous shift register mode
  - —Standard programmable bit rates programmable up to 62.5K bits/sec @ 1 MHz
- Ten interrupts
  - —Four edge-sensitive lines; two positive, two negative
  - —Reset
  - —Non-maskable
  - —Two counter underflows
  - —Serial data received
  - —Serial data transmitted
- Bus expandable to 64K bytes of external memory
- Flexible clock circuitry
  - —2-MHz or 1-MHz internal operation
  - —4 MHz Crystal used to generate internal clocks
- 1 μs minimum instruction execution time at 2 MHz
- NMOS-3 silicon gate, depletion load technology
- Single +5V power supply
- 12 mW stand-by power for 32 bytes of the 192-byte RAM
- 64-pin QUIP

1.2 SUMMARY

The Rockwell R6501Q is a complete, high-performance 8-bit NMOS-3 microcomputer on a single chip and is compatible with all members of the R6500 family.

The R6501Q consists of an enhanced 6502 CPU, an internal clock oscillator, 192 bytes of Random Access Memory (RAM), and versatile interface circuitry. The interface circuitry includes two 16-bit programmable timer/counters, 32 bidirectional input/output lines (including four edge-sensitive lines and input latching on one 8-bit port), a full-duplex serial I/O channel, ten interrupts, and bus expandability.

The innovative architecture and the demonstrated high performance of the R6502 CPU, as well as instruction simplicity, results in system cost-effectiveness and a wide range of computational power. These features make the R6501Q a leading candidate for microcomputer applications.

Rockwell supports development of the R6501Q with the System 65 Microcomputer Development System and the R6500/* Family of Personality Modules. Complete in-circuit emulation with the R6500/* Family of Personality Modules allows total system test and evaluation.

This product description assumes that the reader is familiar with the R6502 CPU hardware and programming capabilities. A detailed description of the R6502 CPU hardware is included in the R6500 Microcomputer System Hardware Manual (Document Order No. 201). A description of the instruction capabilities of the R6502 CPU is contained in the R6500 Microcomputer System Programming Manual (Document Order No. 202).

1.3 CUSTOMER OPTIONS

The R6501Q has no customer specified mask options. It has the following characteristics.

- Crystal Oscillator
- Clock Divide by 4
- Clock MASTER Mode
- Reset Vector at FFFC
- Internal pull-up resistors on Ports PA, PB, and PC

1.4 ORDERING INFORMATION

R6501Q — 4 MHz Xtal, 1 MHz Operation—Commercial
R6501AQ—4 MHz Xtal, 2 MHz Operation—Commercial
R6501EQ—4 MHz Xtal, 1 MHz Operation—Industrial
R6501AEQ—4 MHz Xtal, 2 MHz Operation—Industrial

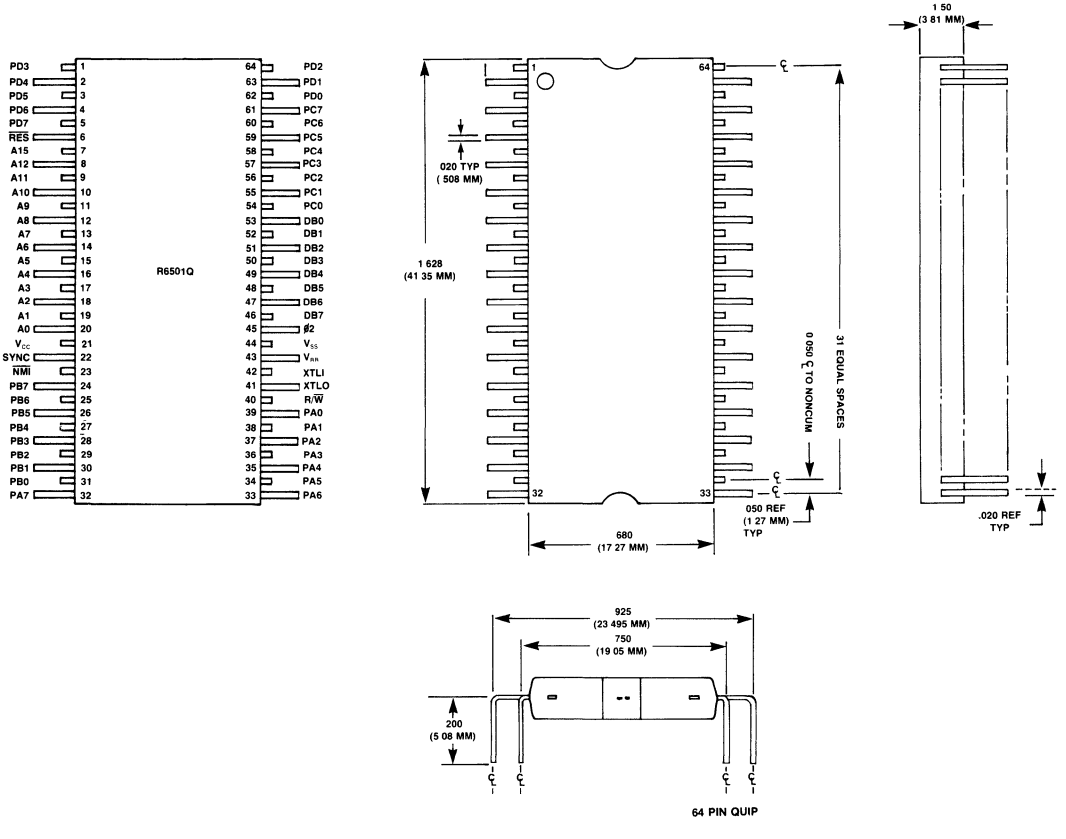


Figure 2-1. Mechanical Outline & Pin Out Configuration

SECTION 2
INTERFACE REQUIREMENTS

This section describes the interface requirements for the R6501Q. Figure 2-1 and 2-2 show the Interface Diagram and the pin out configuration for both devices. Table 2-1 describes the function of each pin. Figure 3-1 has a detailed block diagram of the R6501Q ports which illustrates the internal function of the device.

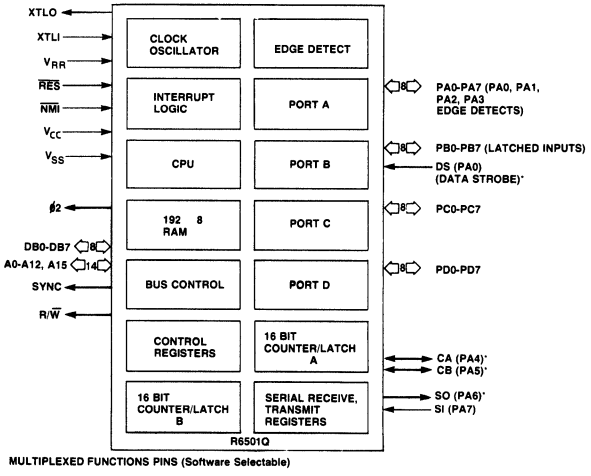


Figure 2-2. Interface Diagram

TABLE 2-1. R6501Q Pin Descriptions

SIGNAL NAME	PIN NO.	DESCRIPTION
V_{CC}	21	Main power supply +5V
V_{RR}	43	Separate power pin for RAM. In the event that V_{CC} power is off, this power retains RAM data.
V_{SS}	44	Signal and power ground (0V)
XTLI	42	Crystal or clock input for internal clock oscillator. Allows input of X1 clock signal if XTLO is connected to V_{SS} or of X4 clock if XTLO is floated.
XTLO	41	Crystal output from internal clock oscillator.
$\overline{RES}$	6	The Reset input is used to initialize the device. This signal must not transition from low to high for at least eight cycles after V_{CC} reaches operating range and the internal oscillator has stabilized.
φ2	45	Clock signal output at internal frequency.
$\overline{NMI}$	23	A negative going edge on the Non-Maskable Interrupt signal requests that a non-maskable interrupt be generated with the CPU.
PA0-PA7 PB0-PB7 PC0-PC7 PD0-PD7	39-32 31-24 54-61 62-64, 1-5	Four 8-bit ports used for either input/output. Each line of Ports A, B and C consists of an active transistor to V_{SS} and a passive pull-up to V_{CC}. Port D functions as either an 8-bit input or 8-bit output port. It has active pull-up and pull-down transistors.
A0-A12, A15	20-7	Fourteen address lines used to address a complete 65K external address space. Note: A13 & A14 are sourced through PC6 & PC7 when in the Full Address Mode.
DB0-DB7	53-46	Eight bidirectional data bus lines used to transmit data to and from external memory.
SYNC	22	SYNC is a positive going signal for the full clock cycle whenever the CPU is performing an OP CODE fetch.
R/$\overline{W}$	40	Controls the direction of data transfer between the CPU and the external 65K address space. The signal is high when reading and low when writing.

SECTION 3
SYSTEM ARCHITECTURE

This section provides a functional description of the R6501Q. Functionally the R6501Q consists of a CPU, RAM, four 8-bit parallel I/O ports, a serial I/O port, dual counter/latch circuits, a mode control register, and an interrupt flag/enable dual register circuit. A block diagram of the system is shown in Figure 3-1.

NOTE

Throughout this document, unless specified otherwise, all memory or register address locations are specified in hexadecimal notation.

3.1 CPU LOGIC

The R6501Q internal CPU is a standard 6502 configuration with an 8-bit Accumulator register, two 8-bit Index Registers (X and Y); an 8-bit Stack Pointer register, an ALU, a 16-bit Program Counter, and standard instruction register/decode and internal timing control logic.

3.1.1 Accumulator

The accumulator is a general purpose 8-bit register that stores the results of most arithmetic and logic operations. In addition, the accumulator usually contains one of the two data words used in these operations.

3.1.2 Index Registers

There are two 8-bit index registers, X and Y. Each index register can be used as a base to modify the address data program counter and thus obtain a new address—the sum of the program counter contents and the index register contents.

When executing an instruction which specifies indirect addressing, the CPU fetches the op code and the address and modifies the address from memory by adding the index register to it prior to loading or storing the value of memory.

Indexing greatly simplifies many types of programs, especially those using data tables.

3.1.3 Stack Pointer

The Stack Pointer is an 8-bit register. It is automatically incremented and decremented under control of the microprocessor to perform stack manipulation in response to either user instructions, an internal $\overline{IRQ}$ interrupt, or the external interrupt line $\overline{NMI}$. The Stack Pointer must be initialized by the user program.

The stack allows simple implementation of multiple level interrupts, subroutine nesting and simplification of many types of data manipulation. The JSR, BRK, RTI and RTS instructions use the stack and Stack Pointer.

The stack can be envisioned as a deck of cards which may be accessed only from the top. The address of a memory location is stored (or "pushed") onto the stack. Each time data are to be pushed onto the stack, the Stack Pointer is placed on the Address Bus, data are written into the memory location addressed by the Stack Pointer, and the Stack Pointer is decremented by 1. Each time data are read (or "pulled") from the stack, the Stack Pointer is incremented by 1. The Stack Pointer is then placed on the Address Bus and data are read from the memory location addressed by the Pointer.

The stack is located on zero page, i.e., memory locations 00FF-0040. After reset, which leaves the Stack Pointer indeterminate, normal usage calls for its initialization at 00FF.

3.1.4 Arithmetic And Logic Unit (ALU)

All arithmetic and logic operations take place in the ALU, including incrementing and decrementing internal registers (except the Program Counter). The ALU cannot store data for more than one cycle. If data are placed on the inputs to the ALU at the beginning of a cycle, the result is always gated into one of the storage registers or to external memory during the next cycle.

Each bit of the ALU has two inputs. These inputs can be tied to various internal buses or to a logic zero; the ALU then generates the function (AND, OR, SUM, and so on) using the data on the two inputs

3.1.5 Program Counter

The 16-bit Program Counter provides the addresses that are used to step the processor through sequential instructions in a program Each time the processor fetches an instruction from program memory, the lower (least significant) byte of the Program Counter (PCL) is placed on the low-order bits of the Address Bus and the higher (most significant) byte of the Program Counter (PCH) is placed on the high-order 8 bits of the Address Bus. The Counter is incremented each time an instruction or data is fetched from program memory.

3.1.6 Instruction Register and Instruction Decode

Instructions are fetched from ROM or RAM and gated onto the Internal Data Bus. These instructions are latched into the Instruction Register, then decoded along with timing and interrupt signals to generate control signals for the various registers.

3.1.7 Timing Control

The Timing Control Logic keeps track of the specific instruction cycle being executed. This logic is set to T0 each time an instruction fetch is executed and is advanced at the beginning of each Phase One clock pulse for as many cycles as are required to complete the instruction. Each data transfer which takes place between the registers is caused by decoding the contents of both the instruction register and timing control unit.

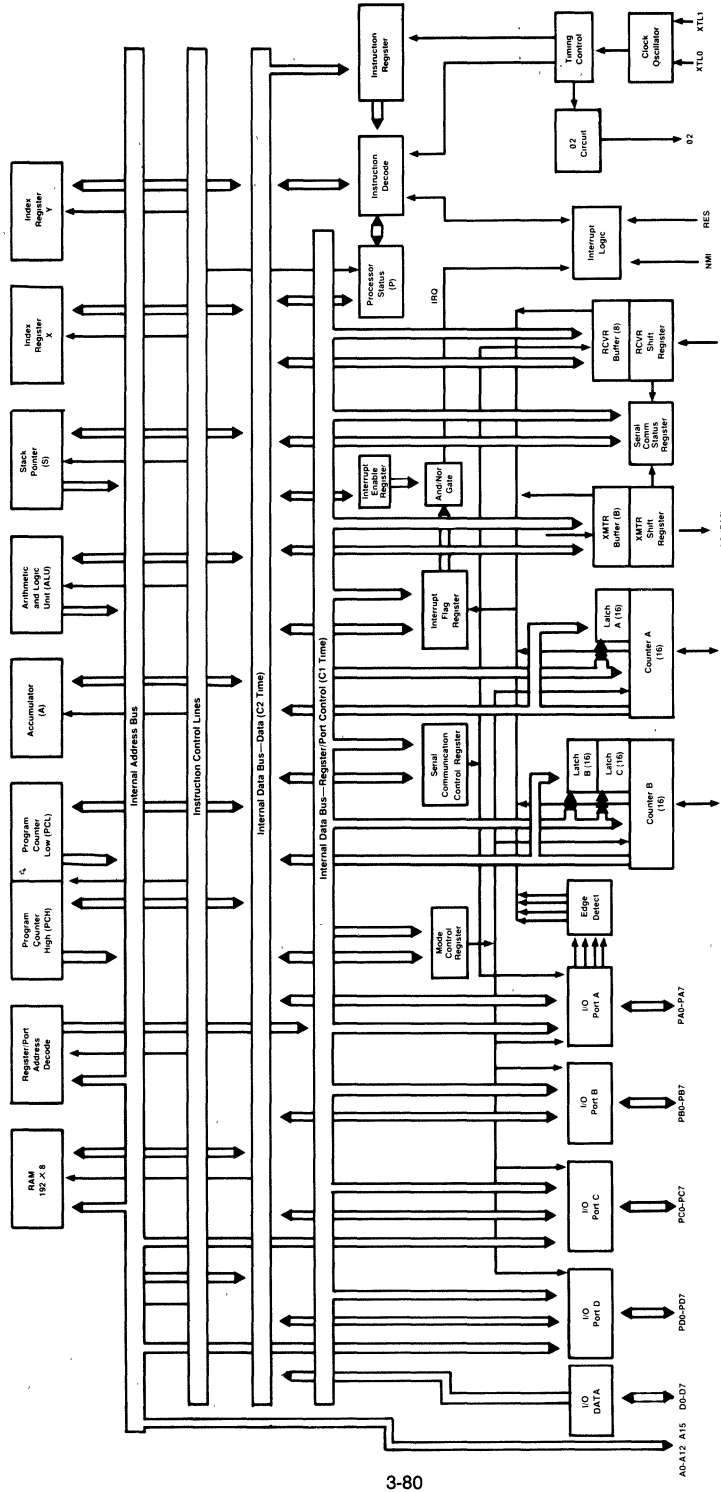


Figure 3-1. Detailed Block Diagram

3.1.8 Interrupt Logic

Interrupt logic controls the sequencing of three interrupts; $\overline{RES}$, $\overline{NMI}$ and $\overline{IRQ}$. $\overline{IRQ}$ is generated by any one of eight conditions: 2 Counter Overflows, 2 Positive Edge Detects, 2 Negative Edge Detects, and 2 Serial Port Conditions.

3.2 NEW INSTRUCTIONS

In addition to the standard R6502 instruction set, four new bit manipulation instructions have been added to the R6501Q. The added instructions and their format are explained in the following paragraphs. Refer to Appendix A for the Op Code mnemonic addressing matrix for these added instructions. The four added instructions do not impact the CPU processor status register.

3.2.1 Set Memory Bit (SMB m, Addr.)

This instruction sets to "1" one of the 8-bit data field specified by the zero page address (memory or I/O port). The first byte of the instruction specifies the SMB operation and one of eight bits to be set. The second byte of the instruction designates address (0-255) of the byte to be operated upon.

3.2.2 Reset Memory Bit (RMB m, Addr.)

This instruction is the same operation and format as SMB instruction except a reset to "0" of the bit results.

3.2.3 Branch On Bit Set Relative (BBS m, Addr, DEST)

This instruction tests one of eight bits designated by a 3-bit immediate field within the first byte of the instruction. The second byte is used to designate the address of the byte to be tested within the zero page address range (memory or I/O ports). The third byte of the instruction is used to specify the 8-bit relative address to which the instruction branches if the bit tested is a "1". If the bit tested is not set, the next sequential instruction is executed.

3.2.4 Branch On Bit Reset Relative (BBR m, Addr, DEST)

This instruction is the same operation and format as the BBS instruction except that a branch takes place if the bit tested is a "0".

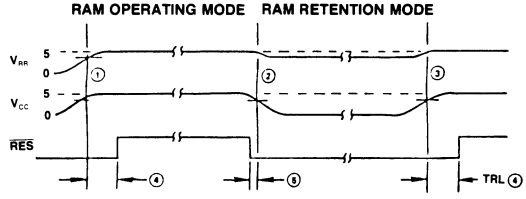
3.3 READ-ONLY-MEMORY (ROM)

The R6501Q has no ROM and its Reset vector is at FFFC.

3.4 RANDOM ACCESS MEMORY (RAM)

The RAM consists of 192 bytes of read/write memory with an assigned page zero address of 0040 through 00FF. The R6501Q provides a separate power pin (V_{RR}) which may be used for standby power for 32 bytes located at 0040-005F. In the event of the loss of V_{CC} power, the lowest 32 bytes of RAM data will be retained if standby power is supplied to the V_{RR} pin. If the RAM data retention is not required then V_{RR} must be connected to V_{CC}. During operation V_{RR} must be at the V_{CC} level.

For the RAM to retain data upon loss of V_{CC}, V_{RR} must be supplied within operating range and $\overline{RES}$ must be driven low at least eight Ø2 clock pulses before V_{CC} falls out of operating range. $\overline{RES}$ must then be held low while V_{CC} is out of operating range and until at least eight Ø2 clock cycles after V_{CC} is again within operating range and the internal Ø2 oscillator is stabilized. V_{RR} must remain within V_{CC} operating range during normal operation. When V_{CC} is out of operating range, V_{RR} must remain within the V_{RR} retention range in order to retain data. Figure 3.2 shows typical waveforms.



1 INITIAL APPLICATION OF V_{CC} AND V_{RR}
2 LOSS OF V_{CC}, RAM ON STANDBY POWER
3 REAPPLICATION OF V_{CC}.
4 >8 Ø2 CLOCK PULSES AFTER OSCILLATOR STABILIZATION
5 >8 Ø2 CLOCK PULSES

Figure 3-2. Data Retention Timing

3.5 CLOCK OSCILLATOR

The R6501Q has been configured for a crystal oscillator, a countdown network, and for Master Mode Operation.

A reference frequency can be generated with the on-chip oscillator using either an external crystal or an external oscillator. The oscillator reference frequency passes through an internal countdown network to obtain the internal operating frequency (see Figures 3-3a and 3-3b). The external crystal generated reference frequency is a preferred method since the resistor method can have tolerances approaching 50%.

Note:

When operating at 1 MHz interval frequency (R6501Q) place a 15-22 pt capacitor between XTLO and ground.

Internal timing can also be controlled by driving the XTLI pin with an external frequency source. Figure 3-3c shows typical connections. If XTLO is left floating, the external source is divided by the internal countdown network. However, if XTLO is tied to V_{SS}, the internal countdown network is bypassed causing the chip to operate at the frequency of the external source.

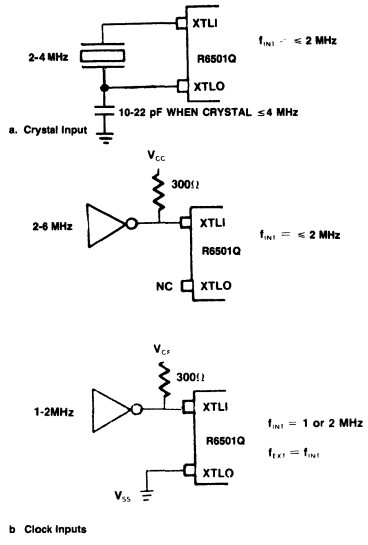


Figure 3-3. Clock Oscillator Input Options

3.6 MODE CONTROL REGISTER (MCR)

The Mode Control Register contains control bits for the multifunction I/O ports and mode select bits for Counter A and Counter B. Its setting, along with the setting of the Serial Communications Control Register (SCCR), determines the basic configuration of the R6501Q in any application. Initializing this register is one of the first actions of any software program. The Mode Control Register bit assignment is shown in Figure 3-5.

3.7 INTERRUPT FLAG REGISTER (IFR) AND INTERRUPT ENABLE REGISTER (IER)

An $\overline{IRQ}$ interrupt request can be initiated by any or all of eight possible sources. These sources are all capable of being enabled or disabled by the use of the appropriate interrupt enabled bits in the Interrupt Enable Register (IER). Multiple simultaneous interrupts cause the $\overline{IRQ}$ interrupt request to remain active until all interrupting conditions have been serviced and cleared.

The Interrupt Flag Register contains the information that indicates which I/O or counter needs attention. The contents of the Interrupt Flag Register may be examined at any time by reading at address: 0011. Edge detect IFR bits may be cleared by executing a RMB instruction at address location 0010. The RMB X, (0010) instruction reads FF, modifies bit X to a "0", and writes the modified value at address location 0011. In this way IFR bits set to a "1" after the read cycle of a Read-Modify-Write instruction (such as RMB) are protected from being cleared. A logic "1" is ignored when writing to edge detect IFR bits.

Each IFR bit has a corresponding bit in the Interrupt Enable Register which can be set to a "1" by writing a "1" in the respective bit position at location 0012. Individual IER bits may be cleared by writing a "0" in the respective bit position, or by $\overline{RES}$. If set to a "1", an IRQ will be generated when the corresponding IFR bit becomes true. The Interrupt Flag Register and Interrupt Enable Register bit assignments are shown in Figure 3-6 and the functions of each bit are explained in Table 3-1.

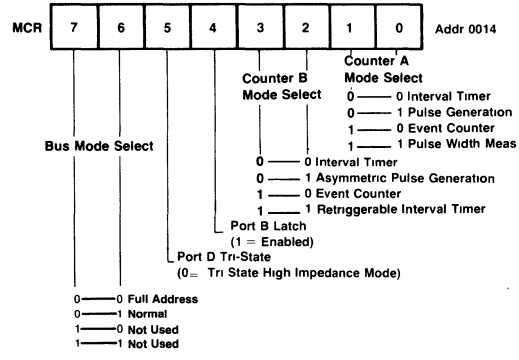


Figure 3-5. Mode Control Register

The use of Counter A Mode Select is shown in Section 6.1.

The use of Counter B Mode Select is shown in Section 6.2.

The use of Port B Latch Enable is shown in Section 4.4.

The use of Port D in Tri-State Enable is shown in Section 4.6.

The use of Bus Mode Select is shown in Section 4.5 and 4.6.

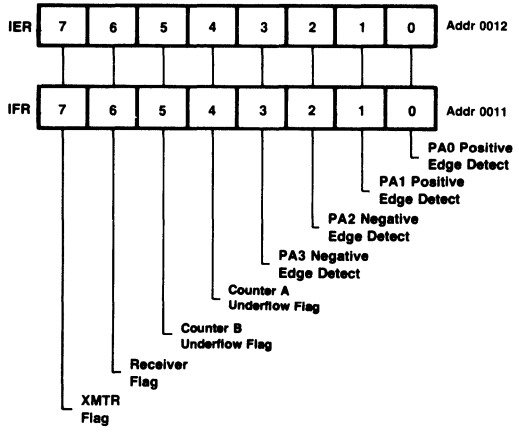


Figure 3-6. Interrupt Enable and Flag Registers

3.8 PROCESSOR STATUS REGISTER

The 8-bit Processor Status Register, shown in Figure 3-7, contains seven status flags. Some of these flags are controlled by the user program; others may be controlled both by the user's program and the CPU. The R6502 instruction set contains a number of conditional branch instructions which are designed to allow testing of these flags. Each of the eight processor status flags is described in the following sections.

3.8.1 Carry Bit (C)

The Carry Bit (C) can be considered as the ninth bit of an arithmetic operation. It is set to logic 1 if a carry from the eighth bit has occurred or cleared to logic 0 if no carry occurred as the result of arithmetic operations.

The Carry Bit may be set or cleared under program control by use of the Set Carry (SEC) or Clear Carry (CLC) instruction, respectively. Other operations which affect the Carry Bit are ADC, ASL, CMP, CPX, CPY, LSR, PLP, ROL, ROR, RTI, and SBC.

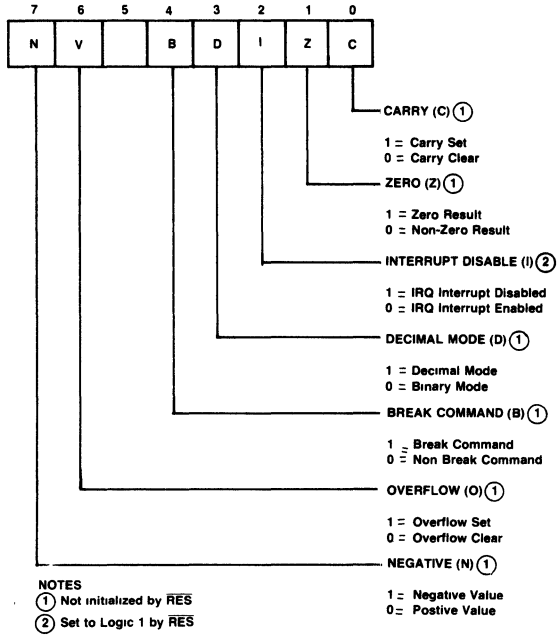


Figure 3-7. Processor Status Register

Table 3-1. Interrupt Flag Register Bit Codes

BIT CODE	FUNCTION
IFR 0:	PA0 Positive Edge Detect Flag—Set to a "1" when a positive going edge is detected on PA0. Cleared by RMB 0 (0010) instruction or by $\overline{RES}$.
IFR 1:	PA1 Positive Edge Detect Flag—Set to a 1 when a positive going edge is detected on PA1. Cleared by RMB 1 (0010) instruction or by $\overline{RES}$.
IFR 2:	PA2 Negative Edge Detect Flag—Set to a 1 when a negative going edge is detected on PA2. Cleared by RMB 2 (0010) instruction or by $\overline{RES}$.
IFR 3:	PA3 Negative Edge Detect Flag—Set to 1 when a negative going edge is detected on PA3. Cleared by RMB 3 (0010) instruction or by $\overline{RES}$.
IFR 4:	Counter A Underflow Flag—Set to a 1 when Counter A underflow occurs. Cleared by reading the Lower Counter A at location 0018, by writing to address location 001A, or by $\overline{RES}$.
IFR 5:	Counter B Underflow Flag—Set to a 1 when Counter B underflow occurs. Cleared by reading the Lower Counter B at location 001C, by writing to address location 001E, or by $\overline{RES}$.
IFR 6:	Receiver Interrupt Flag—Set to a 1 when any of the Serial Communication Status Register bits 0 through 3 is set to a 1. Cleared when the Receiver Status bits (SCSR 0-3) are cleared or by $\overline{RES}$.
IFR 7:	Transmitter Interrupt Flag—Set to a 1 when SCSR 6 is set to a 1 while SCSR 5 is a 0 or SCSR 7 is set to a 1. Cleared when the Transmitter Status bits (SCSR 6 & 7) are cleared or by $\overline{RES}$.

3.8.2 Zero Bit (Z)

The Zero Bit (Z) is set to logic 1 by the CPU during any data movement or calculation which sets all 8 bits of the result to zero. This bit is cleared to logic 0 when the resultant 8 bits of a data movement or calculation operation are not all zero. The R6500 instruction set contains no instruction to specifically set or clear the Zero Bit The Zero Bit is, however, affected by the following instructions; ADC, AND, ASL, BIT, CMP, CPX, CPY, DEC, DEX, DEY, EOR, INC, INX, INY, LDA, LDX, LDY, LSR, ORA, PLA, PLP, ROL, ROR, RTI, SBC, TAX, TAY, TXA, TSX, and TYA.

3.8.3 Interrupt Disable Bit (I)

The Interrupt Disable Bit (I) is used to control the servicing of an interrupt request ($\overline{IRQ}$). If the I Bit is reset to logic 0, the $\overline{IRQ}$ signal will be serviced. If the bit is set to logic 1, the $\overline{IRQ}$ signal will be ignored. The CPU will set the Interrupt Disable Bit to logic 1 if a RESET ($\overline{RES}$), $\overline{IRQ}$, or Non-Maskable Interrupt ($\overline{NMI}$) signal is detected

The I bit is cleared by the Clear Interrupt Mask Instruction (CLI) and is set by the Set Interrupt Mask Instruction (SEI). This bit is set by the BRK Instruction. The Return from Interrupt (RTI) and Pull Processor Status (PLP) instructions will also affect the I bit

3.8.4 Decimal Mode Bit (D)

The Decimal Mode Bit (D) is used to control the arithmetic mode of the CPU. When this bit is set to logic 1, the adder operates as a decimal adder. When this bit is cleared to logic 0, the adder operates as a straight binary adder. The adder mode is controlled only by the programmer. The Set Decimal Mode (SED) instruction will set the D bit; the Clear Decimal Mode (CLD) instruction clears it. The PLP and RTI instructions also affect the Decimal Mode Bit.

CAUTION

The Decimal Mode Bit will either set or clear in an unpredictable manner upon power application. This bit must be initialized to the desired state by the user program or erroneous results may occur.

3.8.5 Break Bit (B)

The Break Bit (B) is used to determine the condition which caused the $\overline{IRQ}$ service routine to be entered. If the $\overline{IRQ}$ service routine was entered because the CPU executed a BRK command, the Break Bit will be set to logic 1. If the $\overline{IRQ}$ routine was entered as the result of an $\overline{IRQ}$ signal being generated, the B bit will be cleared to logic 0 There are no instructions which can set or clear this bit.

3.8.6 Overflow Bit (V)

The Overflow Bit (V) is used to indicate that the result of a signed, binary addition, or subtraction, operation is a value that cannot be contained in seven bits ($-128 \leq n \leq 127$). This indicator only has meaning when signed arithmetic (sign and seven magnitude bits) is performed. When the ADC or SBC instruction is performed, the Overflow Bit is set to logic 1 if the polarity of the sign bit (bit 7) is changed because the result exceeds +127 or −128, otherwise the bit is cleared to logic 0 The V bit may also be cleared by the programmer using a Clear Overflow (CLV) instruction.

The Overflow Bit may also be used with the BIT instruction. The BIT instruction—which may be used to sample interface devices—allows the overflow flag to reflect the condition of bit 6 in the sampled field. During a BIT instruction the Overflow Bit is set equal to the content of the bit 6 on the data tested with BIT instruction. When used in this mode, the overflow has nothing to do with signed arithmetic, but is just another sense bit for the microprocessor. Instructions affecting the V flag are ADC, BIT, CLV, PLP, RTI and SBC.

3.8.7 Negative Bit (N)

The Negative Bit (N) is used to indicate that the sign bit (bit 7) in the resulting value of a data movement or data arithmetic operation is set to logic 1. If the sign bit is set to logic 1, the resulting value of the data movement or arithmetic operation is negative; if the sign bit is cleared, the result of the data movement or arithmetic operation is positive. There are no instructions that set or clear the Negative Bit since the Negative Bit represents only the status of a result. The instructions that effect the state of the Negative Bit are: ADC, AND, ASL, BIT, CMP, CPX, CPY, DEC, DEX, DEY, EOR, INC, INX, INY, LDA, LDX, LDY, LSR, ORA, PLA, PLP, ROL, ROR, RTI, SBC, TAX, TAY, TSX, TXA, and TYA.

SECTION 4
PARALLEL INPUT/OUTPUT PORTS & BUS MODES

The devices have 32 I/O lines grouped into four 8-bit ports (PA, PB, PC, and PD). Ports A through C may be used either for input or output individually or in groups of any combination. Port D may be used as all inputs or all outputs.

Multifunction I/O's such as Port A and Port C are protected from normal port I/O instructions when they are programmed to perform a multiplexed function.

Internal pull-up resistors (FET's with an impedance range of $3K \leq R_L \leq 12K$ ohm) are provided on all port pins except Port D.

The direction of the 32 I/O lines are controlled by four 8-bit port registers located in page zero. This arrangement provides quick programming access using simple two-byte zero page address instructions. There are no direction registers associated with the I/O ports, thus simplifying I/O handling. The I/O addresses are shown in Table 4-1. Appendix E.4 shows the I/O Port Timing.

Table 4-1. I/O Port Addresses

PORT	ADDRESS
A	0000
B	0001
C	0002
D	0003

4.1 INPUTS

Inputs for Ports A, B, and C are enabled by loading logic 1 into all I/O port register bit positions that are to correspond to I/O input lines. A low (<0.8V) input signal will cause a logic 0 to be read when a read instruction is issued to the port register. A high (>2.0V) input will cause a logic 1 to be read. An $\overline{RES}$ signal forces all I/O port registers to logic 1 thus initially treating all I/O lines as inputs.

Port D may only be all inputs or all outputs. All inputs is selected by setting bit 5 of the Mode Control Register (MCR5) to a "0".

The status of the input lines can be interrogated at any time by reading the I/O port addresses. Note that this will return the actual status of the input lines, not the data written into the I/O port registers.

Read/Modify/Write instructions can be used to modify the operation of PA, PB, PC, & PD. During the Read cycle of a Read/Modify/Write instruction the Port I/O register is read. For all other read instructions the port input lines are read. Read/Modify/Write instructions are: ASL, DEC, INC, LSR, RMB, ROL, ROR, and SMB.

4.2 OUTPUTS

Outputs for Ports A thru D are controlled by writing the desired I/O line output states into the corresponding I/O port register bit positions. A logic 1 will force a high (>2.4V) output while a logic 0 will force a low (<0.4V) output.

Port D all outputs is selected by setting MCR5 to a "1".

4.3 Port A (PA)

Port A can be programmed via the Mode Control Register (MCR) and the Serial Communications Control Register (SCCR) as a standard parallel 8-bit, bit independent, I/O port or as serial channel I/O lines, counter I/O lines, or an input data strobe for the Port B input latch option. Table 4-2 tabulates the control and usage of Port A.

In addition to their normal I/O functions, PA0 and PA1 can detect positive going edges and PA2 and PA3 can detect negative going edges. A proper transition on these pins will set a corresponding status bit in the IFR and generate an interrupt request if the respective Interrupt Enable Bit is set. The maximum rate at which an edge can be detected is one-half the $\phi 2$ clock rate. Edge detection timing is shown in Appendix E.3.

Table 4-2. Port A Control and Usage

	PA0 I/O		PORT B LATCH MODE	
	MCR4 = 0		MCR4 = 1	
	SIGNAL		SIGNAL	
	NAME	TYPE	NAME	TYPE
PA0 (2) PIN 39	PA0	I/O	PORT B LATCH STROBE	INPUT (1)

	PA1-PA3 I/O	
	SIGNAL	
	NAME	TYPE
PA1 (2) PIN 38 PA2 (3) PIN 37 PA3 (3) PIN 36	PA1 PA2 PA3	I/O I/O I/O

	PA4 I/O		COUNTER A I/O			
	MCR0 = 0 MCR1 = 0 SCCR7 = 0 RCVR S/R MODE = 0 (4) (5)		MCR0 = 1 MCR1 = 0 SCCR7 = 0 RCVR S/R MODE = 0 (4)		SCCR7 = 0 SCCR6 = 0 MCR1 = 1	
	SIGNAL		SIGNAL		SIGNAL	
	NAME	TYPE	NAME	TYPE	NAME	TYPE
PA4 PIN 35	PA4	I/O	CNTA	OUTPUT	CNTA	INPUT (1)
	SERIAL I/O SHIFT REGISTER CLOCK					
	SCCR7 = 1 SCCR5 = 1		RCVR S/R MODE = 1 (4)			
	SIGNAL		SIGNAL			
	NAME	TYPE	NAME	TYPE		
	XMTR CLOCK	OUTPUT	RCVR CLOCK	INPUT (1)		

	PA5 I/O		COUNTER B I/O			
	MCR3 = 0 MCR2 = 0		MCR3 = 0 MCR2 = 1		MCR3 = 1 MCR2 = X	
	SIGNAL		SIGNAL		SIGNAL	
	NAME	TYPE	NAME	TYPE	NAME	TYPE
PA5 PIN 34	PA5	I/O	CNTB	OUTPUT	CNTB	INPUT (1)

	PA6 I/O		SERIAL I/O XMTR OUTPUT	
	SCCR7 = 0		SCCR7 = 1	
	SIGNAL		SIGNAL	
	NAME	TYPE	NAME	TYPE
PA6 PIN 33	PA6	I/O	XMTR	OUTPUT

	PA7 I/O		SERIAL I/O RCVR INPUT	
	SCCR6 = 0		SCCR6 = 1	
	SIGNAL		SIGNAL	
	NAME	TYPE	NAME	TYPE
PA7 PIN 32	PA7	I/O	RCVR	INPUT (1)

(1) HARDWARE BUFFER FLOAT
(2) POSITIVE EDGE DETECT
(3) NEGATIVE EDGE DETECT
(4) RCVR S/R MODE = 1 WHEN SCCR6 · $\overline{\text{SCCR5}}$ · SCCR4 = 1
(5) For the following mode combinations PA4 is available as an Input Only pin:
$\overline{\text{SCCR7}}$•SCCR6•$\overline{\text{SCCR5}}$•MCR1
+ $\overline{\text{SCCR7}}$•SCCR6•$\overline{\text{SCCR4}}$•MCR1
+ SCCR7•$\overline{\text{SCCR6}}$•$\overline{\text{SCCR5}}$
+ SCCR7•$\overline{\text{SCCR5}}$•$\overline{\text{SCCR4}}$•

4.4 PORT B (PB)

Port B can be programmed as an 8-bit, bit-independent I/O port. It has a latched input capability which may be enabled or disabled via the Mode Control Register (MCR). Table 4-3 tabulates the control and usage of Port B. An Input Data Strobe signal must be provided thru PA0 when Port B is programmed to be used with latched input option. Input data latch timing for Port B is shown in Appendix E.3.

Table 4-3. Port B Control & Usage

		I/O MODE		LATCH MODE	
		MCR4 = 0		MCR4 = 1 (2)	
PIN #	PIN NAME	SIGNAL NAME	SIGNAL TYPE (1)	SIGNAL NAME	SIGNAL TYPE
31	PB0	PB0	I/O	PB0	INPUT
30	PB1	PB1	I/O	PB1	INPUT
29	PB2	PB2	I/O	PB2	INPUT
28	PB3	PB3	I/O	PB3	INPUT
27	PB4	PB4	I/O	PB4	INPUT
26	PB5	PB5	I/O	PB5	INPUT
25	PB6	PB6	I/O	PB6	INPUT
24	PB7	PB7	I/O	PB7	INPUT

(1) RESISTIVE PULL-UP, ACTIVE BUFFER PULL DOWN
(2) INPUT DATA IS STORED IN PORT B LATCH BY PA0 PULSE

4.5 PORT C (PC)

Port C can be programmed as an I/O port, or as part of the full address bus. When operating in the Full Address Mode PC6 and PC7 serve as A13 and A14 with PC0-PC5 operating as normal I/O pins.

4.6 PORT D (PD)

Port D can be programmed as an I/O Port. Mode selection for Port D is made by the Mode Control Register (MCR). The Port D output drivers can be selected as tri-state drivers by setting bit 5 of the MCR to 1 (one). Table 4-5 shows the necessary settings for the MCR to achieve the various modes for Port D.

4.7 BUS MODES

In the Full Address Mode, the separate address and data bus are used in conjunction with PC6 and PC7, which automatically provide A13 and A14. The remaining ports perform the normal I/O function.

In the I/O Bus Mode all ports serve as I/O. The address and data bus are still functional but without A13 and A14. Since the internal RAM and registers are in the OOXX location, A15 can be used for chip select and A0-A12 used for selecting 8K of external memory.

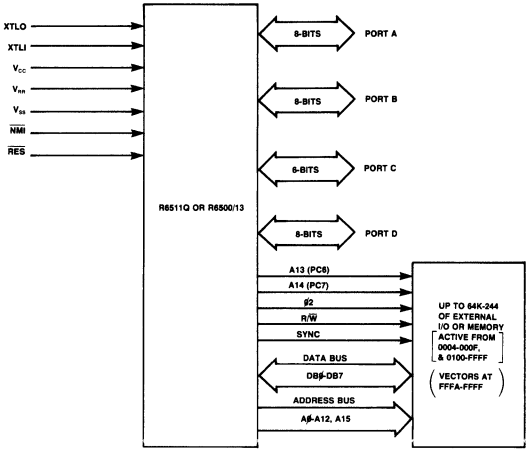


Figure 4-1a. Full Address Mode

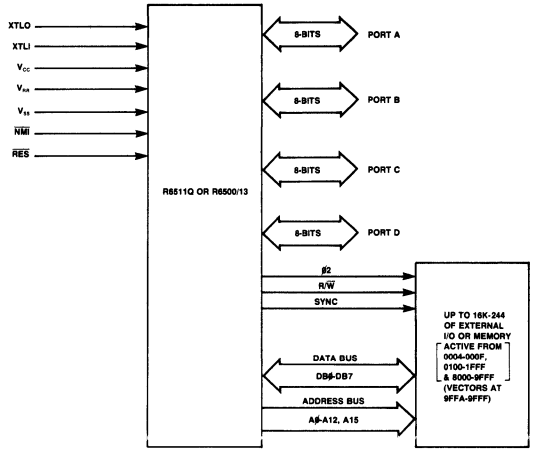


Figure 4-1b. Normal Bus Mode

Table 4-4. Port C Control and Usage

		FULL ADDRESS MODE MCR7 = 0 MCR6 = 0		I/O MODE MCR7 = 0 MCR6 = 1	
		SIGNAL		SIGNAL	
PIN #	PIN NAME	NAME	TYPE	NAME	TYPE (1)
54	PC0	PC0	I/O (1)	PC0	I/O
55	PC1	PC1	I/O (1)	PC1	I/O
56	PC2	PC2	I/O (1)	PC2	I/O
57	PC3	PC3	I/O (1)	PC3	I/O
58	PC4	PC4	I/O (1)	PC4	I/O
59	PC5	PC5	I/O (1)	PC5	I/O
60	PC6	A13	OUTPUT (2)	PC6	I/O
61	PC7	A14	OUTPUT (2)	PC7	I/O

NOTES:
1. Resistive Pull-Up, Active Buffer Pull-Down
2. Active Buffer Pull-Up and Pull-Down

Table 4-5. Port D Control and Usage

		I/O MODES MCR7 = 0 MCR6 = X MCR5 = 0		MCR7 = 0 MCR6 = X MCR5 = 1	
		SIGNAL		SIGNAL	
PIN #	PIN NAME	NAME	TYPE (1)	NAME	TYPE (2)
62	PD0	PD0	INPUT	PD0	OUTPUT
63	PD1	PD1	INPUT	PD1	OUTPUT
64	PD2	PD2	INPUT	PD2	OUTPUT
1	PD3	PD3	INPUT	PD3	OUTPUT
2	PD4	PD4	INPUT	PD4	OUTPUT
3	PD5	PD5	INPUT	PD5	OUTPUT
4	PD6	PD6	INPUT	PD6	OUTPUT
5	PD7	PD7	INPUT	PD7	OUTPUT

NOTES:
1. Tri-State Buffer is in High Impedance Mode
2 Tri-State Buffer is in Active Mode

SECTION 5
SERIAL INPUT/OUTPUT CHANNEL

The device provides a full duplex Serial I/O channel with programmable bit rates and operating modes. The serial I/O functions are controlled by the Serial Communication Control Register (SCCR). The SCCR bit assignment is shown in Figure 5-1. The serial bit rate is determined by Counter A for all modes except the Receiver Shift Register (RCVR S/R) mode for which an external shift clock must be provided. The maximum data rate using the internal clock is 62.5K bits per second (at $\phi 2$ = 1 MHZ). The transmitter (XMTR) and receiver (RCVR) can be independently programmed to operate in different modes and can be independently enabled or disabled.

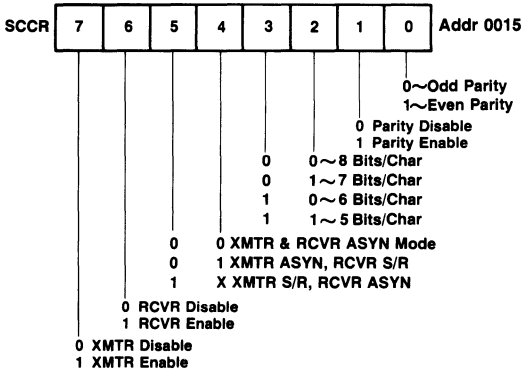


Figure 5-1. Serial Communication Control Register

Except for the Receiver Shift Register Mode (RCVR S/R), all XMTR and RCVR bit rates will occur at one sixteenth of the Counter A interval timer rate. Counter A is forced into an interval timer mode whenever the serial I/O is enabled in a mode requiring an internal clock.

Whenever Counter A is required as a timing source it must be loaded with the hexadecimal code that selects the data rate for the serial I/O Port. Refer to Counter A (paragraph 6.1) for a table of hexadecimal values to represent the desired data rate.

5.1 TRANSMITTER OPERATION (XTMR)

The XTMR operation and the transmitter related control/status functions are enabled by bit 7 of the Serial Communications Control Register (SCCR). The transmitter, when in the Asynchronous (ASYN) mode, automatically adds a start bit, one or two stop bits, and, when enabled, a parity bit to the transmitted data. A word of transmitted data (in asynchronous parity mode) can have 5, 6, 7, or 8 bits of data. The nine data modes are shown in Figure 5-2. When parity is disabled, the 5, 6, 7 or 8 bits of data are terminated with two stop bits.

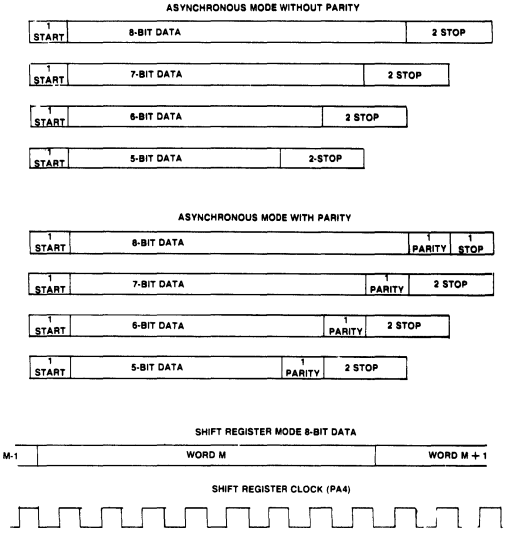


Figure 5-2. SIO Data Modes

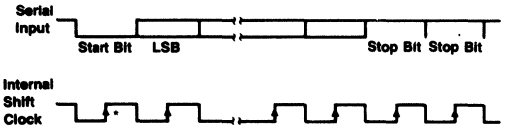
In the S/R mode, eight data bits are always shifted out. Bits/character and parity control bits are ignored. The serial data is shifted out via the SO output (PA6) and the shift clock is available at the CA (PA4) pin. When the transmitter underruns in the S/R mode the SO output and shift clock are held in a high state.

The XMTR Interrupt Flag bit (IFR7) is controlled by Serial Communication Status Register bits SCSR5, SCSR6 and SCSR7.

$$IFR7 = SCSR6\ (\overline{SCSR5} + SCSR7)$$

5.2 RECEIVER OPERATION (RCVR)

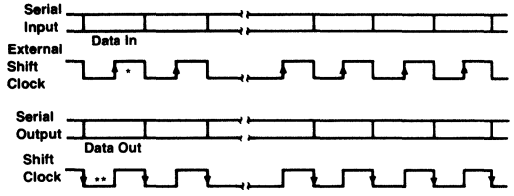
The receiver and its selected control and status functions are enabled when SCCR-6 is set to a "1." In the ASYN mode, data format must have a start bit, the appropriate number of data bits, a parity bit (if enabled), and one stop bit. Refer to paragraph 5.1 for a diagram of bit allocations. The receiver bit period is divided into 8 sub-intervals for internal synchronization. The receiver bit stream is synchronized by the start bit and a strobe signal is generated at the approximate center of each incoming bit. Refer to Figure 5-3 for ASYN Receive Data Timing. The character assembly process does not start if the start bit signal is less than one-half the bit time after a low level is detected on the Receive Data Input. Framing error, over-run, and parity error conditions or a RCVR Data Register Full will set the appropriate status bits. Any of the above conditions will cause an Interrupt Request if the Receiver Interrupt Enable bit is set to logic 1.



*Serial Input Data Shifted In

Figure 5-3. ASYN Receive Data Timing

In the S/R mode, an external shift clock must be provided at CA (PA4) pin along with 8 bits of serial data (LSB first) at the SI input (PA7). The maximum data rate using an external shift clock is one-eighth the internal clock rate. Refer to Figure 5-4 for S/R Mode Timing.



* Serial Input Data Shifted In
** Serial Output Data Makes Transition

Figure 5-4. S/R Mode Timing

A RCVR interrupt (IFR6) is generated whenever any of SCSR0-3 are true.

5.3 SERIAL COMMUNICATION STATUS REGISTER (SCSR)

The Serial Communication Status Register (SCSR) holds information on various communication error conditions, status of the transmitter and receiver data registers, a transmitter end-of-transmission condition, and a receiver idle line condition (Wake-Up Feature). The SCSR bit assignment is shown in Figure 5-5. Bit assignments and functions of the SCSR are as follows:

SCSR 0: *Receiver Data Register Full*—Set to a logic 1 when a character is transferred from the Receiver Shift Register to the Receiver Data Register. This bit is cleared by reading the Receiver Data Register, or by $\overline{RES}$ and is disabled if SCCR 6 = 0. The SCSR 0 bit will not be set to a logic 1 if the received data contains an error condition; instead, a corresponding error bit will be set to a logic 1.

SCSR 1: *Over-Run Error*—Set to a logic 1 when a new character is transferred from the Receiver Shift Register with the last character still in the Receiver Data Register. This bit is cleared by reading the Receiver Data Register or by $\overline{RES}$.

SCSR 2: *Parity Error*—Set to logic 1 when the RCVR is in the ASYN Mode, Parity Enable bit is set, and the received data has a parity error. This bit is cleared by reading the Receiver Data Register or by $\overline{RES}$.

SCSR 3: *Framing Error*—Set to a logic 1 when the received data contains a zero bit after the last data or parity bit in the stop bit slot. Cleared by reading the Receiver Data Register or by $\overline{RES}$ (ASYN Mode only).

SCSR 4: *Wake-Up*—Set to a logic 1 by writing a "1" in bit 4 of address: 0016. The Wake-Up bit is cleared by $\overline{RES}$ or when the receiver detects a string of ten consecutive 1's. When the Wake-Up bit is set SCSR0 through SCSR3 are inhibited.

SCSR 5: *End of Transmission*—Set to a logic 1 by writing a "1" in bit position 5 of address: 0016. The End of Transmission bit is cleared by $\overline{RES}$ or upon writing a new data word into the Transmitter Data Register. When the End-of-Transmission bit is true the Transmitter Register Empty bit is disabled until a Transmitter Under-Run occurs.

SCSR 6: *Transmitter Data Register Empty*—Set to a logic 1 when the contents of the Transmitter Data Register are transferred to the Transmitter Shift Register. Cleared upon writing new data into the Transmit Data Register. This bit is initialized to a logic 1 by $\overline{RES}$.

SCSR 7: *Transmitter Under-Run*—Set to a logic 1 when the last data bit is transmitted if the transmitter is in a S/R Mode or when the last stop bit is transmitted if the XMTR is in the ASYN Mode while the Transmitter Data Register Empty Bit is set. Cleared by a transfer of new data into the Transmitter Shift Register or by $\overline{RES}$.

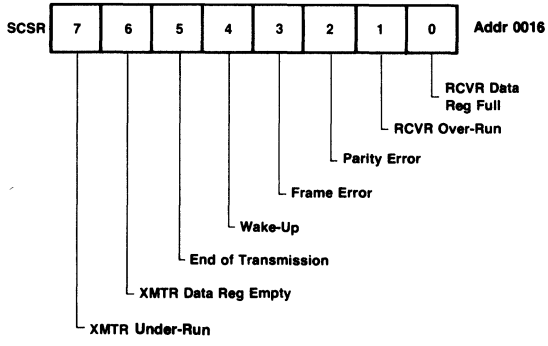


Figure 5-5. SCSR Bit Allocations

5.4 WAKE-UP FEATURE

In a multi-distributed microprocessor or microcomputer appliations, a destination address is usually included at the beginning of the message. The Wake-Up Feature allows non-selected CPU's to ignore the remainder of the message until the beginning of the next message by setting the Wake-Up bit. As long as the Wake-Up flag is true, the Receiver Data Register Full Flag remains false. The Wake-Up bit is automatically cleared when the receiver detects a string of eleven consecutive 1's which indicates an idle transmit line. When the next byte is received, the Receiver Data Register Full Flag signals the CPU to wake-up and read the received data.

SECTION 6
COUNTER/TIMERS

The device contains two 16-bit counters (Counter A and Counter B) and three 16-bit latches associated with the counters. Counter A has one 16-bit latch and Counter B has two 16-bit latches. Each counter can be independently programmed to operate in one of four modes:

Counter A	Counter B
• Pulse width measurement	• Retriggerable Interval Counter
• Pulse Generation	• Asymmetrical Pulse Generation
• Interval Timer	• Interval Timer
• Event Counter	• Event Counter

Operating modes of Counter A and Counter B are controlled by the Mode Control Register. All counting begins at the initialization value and decrements. When modes are selected requiring a counter input/output line, PA4 is automatically selected for Counter A and PA5 is automatically selected for Counter B (see Table 4.2).

6.1 COUNTER A

Counter A consists of a 16-bit counter and a 16-bit latch organized as follows: Lower Counter A (LCA), Upper Counter A (UCA), Lower Latch A (LLA), and Upper Latch A (ULA). The counter contains the count of either Ø2 clock pulses or external events, depending on the counter mode selected. The contents of Counter A may be read any time by executing a read at location 0019 for the Upper Counter A and at location 001A or location 0018 for the Lower Counter A. A read at location 0018 also clears the Counter A Underflow Flag (IFR4).

The 16-bit latch contains the counter initialization value and can be loaded at any time by executing a write to the Upper Latch A at location 0019 and the Lower Latch A at location 0018. In either case, the contents of the accumulator are copied into the applicable latch register.

Counter A can be started at any time by writing to address: 001A. The contents of the accumulator will be copied into the Upper Latch A before the contents of the 16-bit latch are transferred to Counter A. Counter A is set to the latch value whenever Counter A underflows. When Counter A decrements from 0000 the next counter value will be the latch value—not FFFF—and the Counter A Underflow Flag (IFR 4) will be set to "1". This bit may be cleared by reading the Lower Counter A at location 0018, by writing to address location 001A, or by $\overline{RES}$.

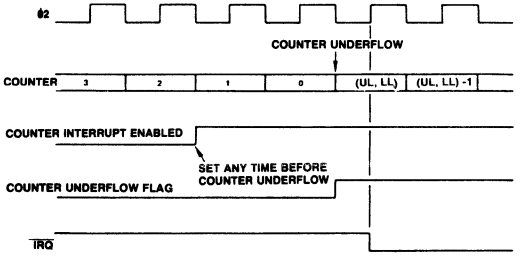


Figure 6-1. Interval Timer Timing Diagram

Counter A operates in any of four modes. These modes are selected by the Counter A Mode Control bits in the Control Register.

MCR1 (bit 1)	MCR0 (bit 0)	Mode
0	0	Interval Timer
0	1	Pulse Generation
1	0	Event Counter
1	1	Pulse Width Measurement

The Interval Timer, Pulse Generation, and Pulse Width Measurement Modes are Ø2 clock counter modes. The Event Counter Mode counts the occurrences of an external event on the CNTR line.

The Counter is set to the Interval Timer Mode (00) when a $\overline{RES}$ signal is generated.

6.1.1 Interval Timer

In the Interval Timer mode the Counter is initialized to the Latch value by either of two conditions:

1. When the Counter is decremented from 0000, the next Counter value is the Latch value (not FFFF).

2. When a write operation is performed to the Load Upper Latch and Transfer Latch to Counter address 001A, the Counter is loaded with the Latch value. Note that the contents of the Accumulator are loaded into the Upper Latch before the Latch value is transferred to the Counter.

The Counter value is decremented by one count at the 02 clock rate. The 16-bit Counter can hold from 1 to 65535 counts. The Counter Timer capacity is therefore 1μs to 65.535 ms at the 1 MHz Ø2 clock rate or 0.5 μs to 32.767 ms at the 2 MHz Ø2 clock rate. Time intervals greater than the maximum Counter value can be easily measured by counting $\overline{IRQ}$ interrupt requests in the counter $\overline{IRQ}$ interrupt routine.

When Counter A decrements from 0000, the Counter A Underflow (IFR4) is set to logic 1. If the Counter A Interrupt Enable Bit (IER4) is also set, an $\overline{IRQ}$ interrupt request will be generated. The Counter A Underflow bit in the Interrupt Flag Register can be examined in the $\overline{IRQ}$ interrupt routine to determine that the $\overline{IRQ}$ was generated by the Counter A Underflow.

While the timer is operating in the Interval Timer Mode, PA4 operates as a PA I/O bit.

A timing diagram of the Interval Timer Mode is shown in Figure 6-1.

6.1.2 Pulse Generation Mode

In the Pulse Generation mode, the CA line operates as a Counter Output. The line toggles from low to high or from high to low whenever a Counter A Underflow occurs or a write is performed to address 001A.

The normal output waveform is a symmetrical square-wave. The CA output is initialized high when entering the mode and transitions low when writing to 001A.

Asymmetric waveforms can be generated if the value of the latch is changed after each counter underflow.

A one-shot waveform can be generated by changing from Pulse Generation to Interval Timer mode after only one occurrence of the output toggle condition.

6.1.3 Event Counter Mode

In this mode the CA is used as an Event Input line, and the Counter will decrement with each rising edge detected on this line. The maximum rate at which this edge can be detected is one-half the $\phi 2$ clock rate.

The Counter can count up to 65,535 occurrences before underflowing. As in the other modes, the Counter A Underflow bit (IER4) is set to logic 1 if the underflow occurs.

Figure 6.2 is a timing diagram of the Event Counter Mode.

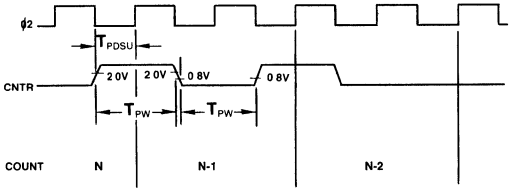


Figure 6-2. Event Counter Mode

6.1.4 Pulse Width Measurement Mode

This mode allows the accurate measurement of a low pulse duration on the CA line. The Counter decrements by one count at the $\phi 2$ clock rate as long as the CA line is held in the low state. The Counter is stopped when CA is in the high state.

The Counter A underflow flag will be set only when the count in the timer reaches zero. Upon reaching zero the timer will be loaded with the latch value and continue counting down as long as the CA pin is held low. After the counter is stopped by a high level on CA, the count will hold as long as CA remains high. Any further low levels on CA will again cause the counter to count down from its present value. The state of the CA line can be determined by testing the state of PA4.

A timing diagram for the Pulse Width Measurement Mode is shown in Figure 6.3.

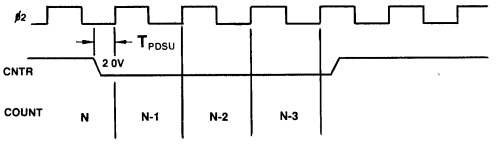


Figure 6-3. Pulse Width Measurement

6.1.5 Serial I/O Data Rate Generation

Counter A also provides clock timing for the Serial I/O which establishes the data rate for the Serial I/O port. When the Serial I/O is enabled, Counter A is forced to operate at the internal clock rate. Counter A is not required for the RCVR S/R mode. The Counter I/O (PA4) may also be required to support the Serial I/O (see Table 4-2).

Table 6-1 identifies the values to be loaded in Counter A for selecting standard data rates with a $\phi 2$ clock rate of 1 MHz and 2 MHz. Although Table 6-1 identifies only the more common data rates, any data rate from 1 to 62.5K bps can be selected by using the formula:

$$N = \frac{\phi 2}{16 \times bps} - 1$$

where

- N = decimal value to be loaded into Counter A using its hexadecimal equivalent.
- $\phi 2$ = the clock frequency (1 MHz or 2 MHz)
- bps = the desired data rate.

NOTE

In Table 6-1 you will notice that the standard data rate and the actual data rate may be slightly different. Transmitter and receiver errors of 1.5% or less are acceptable. A revised clock rate is included in Table 6-1 for those baud rates which fall outside this limit.

Table 6-1. Counter A Values for Baud Rate Selection

STANDARD BAUD RATE	HEXADECIMAL VALUE		03 ACTUAL BAUD RATE AT		CLOCK RATE NEEDED TO GET STANDARD BAUD RATE	
	1 MHz	2 MHz	1 MHz	2 MHz	1 MHz	2 MHz
50	04E1	09C3	50.00	50.00	1.0000	2.0000
75	0340	0682	75.03	74.99	1.0000	2.0000
110	0237	046F	110.04	110.04	1.0000	2.0000
150	01A0	0340	149.88	150.06	1.0000	2.0000
300	00CF	01A0	300.48	299.76	1.0000	2.0000
600	0067	00CF	600 96	600.96	1 0000	2.0000
1200	0033	0067	1201.92	1201.92	1.0000	2.0000
2400	0019	0033	2403.85	2403.85	1.0000	2.0000
3600	0010	0021	3676.47	3676.47	0.9792	1.9584
4800	000C	0019	4807.69	4807 69	1 0000	2.0000
7200	0008	0010	6944.44	7352.94	1.0368	1.9584
9600	0006	000C	8928.57	9615.38	1.0752	2.0000

6.2 COUNTER B

Counter B consists of a 16-bit counter and two 16-bit latches organized as follows: Lower Counter B (LCB), Upper Counter B (UCB), Lower Latch B (LLB), Upper Latch B (ULB), Lower Latch C (LLC), and Upper Latch C (ULC). Latch C is used only in the asymmetrical pulse generation mode. The counter contains the count of either Ø2 clock pulses or external events depending on the counter mode selected. The contents of Counter B may be read any time by executing a Read at location 001D for the Upper Counter B and at location 001E or 001C for the Lower Counter B. A Read at location 001C also clears the Counter B Underflow Flag.

Latch B contains the counter initialization value and can be loaded at any time by executing a Write to the Upper Latch B at location 001D and the Lower Latch B at location 001C. In each case, the contents of the accumulator are copied into the applicable latch register.

Counter B can be initialized at any time by writing to address: 001E. The contents of the accumulator is copied into the Upper Latch B before the value in the 16-bit Latch B is transferred to Counter B. Counter B will also be set to the latch value and the Counter B Underflow Flag bit (IFR5) will be set to a "1" whenever Counter B underflows by decrementing from 0000.

IFR 5 may be cleared by reading the Lower Counter B at location 001C, by writing to address location 001E, or by $\overline{RES}$.

Counter B operates in the same manner as Counter A in the Interval Timer and Event Counter modes. The Pulse Width Measurement Mode is replaced by the Retriggerable Interval Timer mode and the Pulse Generation mode is replaced by the Asymmetrical Pulse Generation Mode. Mode Control Register bits MCR2 and MCR3 select the four Counter B modes in a similar manner and coding as MCR0 and MCR1 select the modes of Counter A.

6.2.1 Retriggerable Interval Timer Mode

When operating in the Retriggerable Interval Timer mode, Counter B is initialized to the latch value by writing to address 001E, by a Counter B underflow, or whenever a positive edge occurs on the CB pin (PA5). The Counter B interrupt flag will be set if the counter underflows before a positive edge occurs on the CB line. Figure 6-4 illustrates the operation.

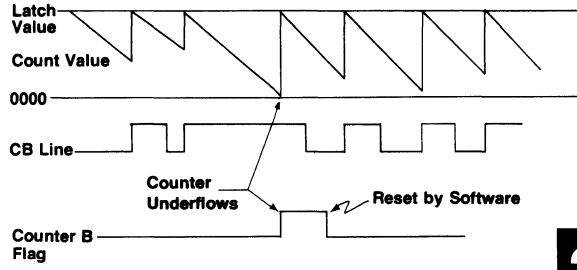


Figure 6-4. Counter B Retriggerable Interval Timer Mode

6.2.2 Asymmetrical Pulse Generation Mode

Counter B has a special Asymmetrical Pulse Generation Mode whereby a pulse train with programmable pulse width and period can be generated without the processor intervention once the latch values are initialized.

In this mode, the 16-bit Latch B is initialized with a value which corresponds to the duration between pulses (referred to as D in the following descriptions). The 16-bit Latch C is initialized with a value corresponding to the desired pulse width (referred to as P in the following descriptions). The initialization sequence for Latch B and C and the starting of a counting sequence are as follows:

1. The lower 8 bits of P are loaded into LLB by writing to address 001C; the upper 8 bits of P are loaded into ULB and the full 16 bits are transferred to Latch C by writing to address location 001D. At this point both Latch B and Latch C contain the value of P.

2. The lower 8 bits of D are loaded into LLB by writing to address 001C; the upper 8 bits of D are loaded into ULB by writing to address location 001E. Writing to address location 001E also causes the contents of the 16-bit Latch B to be downloaded into the Counter B and the CB output to go low as shown in Figure 6-5.

3. When Counter B underflow occurs the contents of the Latch C are loaded into the Counter B and the CB output toggles to a high level, staying high until another underflow occurs. Latch B is then down-loaded and the CB output toggles to a low level repeating the whole process.

SECTION 7
POWER ON/INITIALIZATION CONSIDERATIONS

7.1 POWER ON TIMING

After application of V_{CC} and V_{RR} power to the device, $\overline{RES}$ must be held low for at least eight $\phi 2$ clock cycles after V_{CC} reaches operating range and the internal oscillator has stabilized. This stabilization time is dependent upon the input V_{CC} voltage and performance of the internal oscillator. The clock can be monitored at $\phi 2$ (pin 3). Figure 7-1 illustrates the power turn-on waveforms. Clock stabilization time is typically 20 ms.

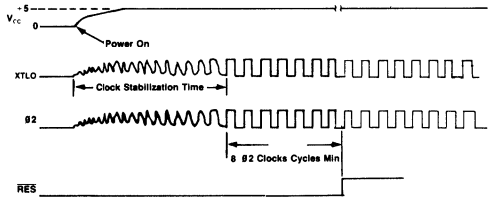


Figure 7-1. Power Turn-On Timing Detail

7.2 POWER-ON RESET

When $\overline{RES}$ goes from low to high, the device sets the Interrupt Mask Bit—bit 2 of the Processor Status Register—and initiates a reset vector fetch at address FFFC and FFFD to begin user program execution. All of the I/O ports (PA, PB, PC, PD) will be forced to the high (logic 1) state. All bits of the Control Register will be cleared to logic 0 causing the Interval Timers counter mode (mode 00) to be selected and all interrupt enabled bits to be reset.

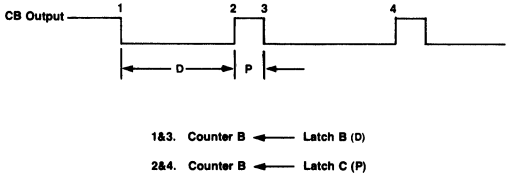


Figure 6-5. Counter B Pulse Generation

7.3 RESET ($\overline{RES}$) CONDITIONING

When $\overline{RES}$ is driven from low to high the device is put in a reset state causing the registers and I/O ports to be configured as shown in Table 7-1.

Table 7-1. $\overline{RES}$ Initialization of I/O Ports and Registers

	7	6	5	4	3	2	1	0
REGISTERS								
Processor Status	—	—	—	—	—	1	—	—
Mode Control (MCR)	0	0	0	0	0	0	0	0
Int. Enable (IER)	0	0	0	0	0	0	0	0
Int. Flag (IFR)	0	0	0	0	0	0	0	0
Ser. Com. Control (SCCR)	0	0	0	0	0	0	0	0
Ser. Com. Status (SCSR)	0	1	0	0	0	0	0	0
PORTS								
PA Latch	1	1	1	1	1	1	1	1
PB Latch	1	1	1	1	1	1	1	1
PC Latch	1	1	1	1	1	1	1	1
PD Latch	1	1	1	1	1	1	1	1

All RAM and other CPU registers will initialize in a random, non-repeatable data pattern.

7.4 INITIALIZATION

Any initialization process for the device should include a $\overline{RES}$, as indicated in the preceeding paragraphs. After stabilization of the internal clock (if a power on situation) an initialization routine should be executed to perform (as a minimum) the following functions:

1. The Stack Pointer should be set
2. Clear or Set Decimal Mode
3. Set or Clear Carry Flag
4. Set up Mode Controls as required
5. Clear Interrupts

A typical initialization subroutine could be as follows:

```
LDX     Load stack pointer starting address into
        X Register
TXS     Transfer X Register value to Stack Pointer
CLD     Clear Decimal Mode
SEC     Set Carry Flag
....    Set-up Mode Control and
....    special function registers
....    and clear RAM as required
CLI     Clear Interrupts
```

APPENDIX A
ENHANCED R6502 INSTRUCTION SET

This appendix contains a summary of the Enhanced R6502 instruction set. For detailed information, consult the R6502 Microcomputer System Programming Manual, Document 29650 N30. The four instructions notated with a * are added instructions to enhance the standard 6502 instruction set.

A.1 INSTRUCTION SET IN ALPHABETIC SEQUENCE

ADC	Add Memory to Accumulator with Carry
AND	"AND" Memory with Accumulator
ASL	Shift Left One Bit (Memory or Accumulator)
*BBR	Branch on Bit Reset Relative
*BBS	Branch on Bit Set Relative
BCC	Branch on Carry Clear
BCS	Branch on Carry Set
BEQ	Branch on Result Zero
BIT	Test Bits in Memory with Accumulator
BMI	Branch on Result Minus
BNE	Branch on Result not Zero
BPL	Branch on Result Plus
BRK	Force Break
BVC	Branch on Overflow Clear
BVS	Branch on Overflow Set
CLC	Clear Carry Flag
CLD	Clear Decimal Mode
CLI	Clear Interrupt Disable Bit
CLV	Clear Overflow Flag
CMP	Compare Memory and Accumulator
CPX	Compare Memory and Index X
CPY	Compare Memory and Index Y
DEC	Decrement Memory by One
DEX	Decrement Index X by One
DEY	Decrement Index Y by One
EOR	"Exclusive-Or" Memory with Accumulator
INC	Increment Memory by One
INX	Increment Index X by One
INY	Increment Index Y by One
JMP	Jump to New Location
JSR	Jump to New Location Saving Return Address
LDA	Load Accumulator with Memory
LDX	Load Index X with Memory
LDY	Load Index Y with Memory
LSR	Shift One Bit Right (Memory or Accumulator)
NOP	No Operation
ORA	"OR" Memory with Accumulator
PHA	Push Accumulator on Stack
PHP	Push Processor Status on Stack
PLA	Pull Accumulator from Stack
PLP	Pull Processor Status from Stack
*RMB	Reset Memory Bit
ROL	Rotate One Bit Left (Memory or Accumulator)
ROR	Rotate One Bit Right (Memory or Accumulator)
RTI	Return from Interrupt
RTS	Return from Subroutine
SBC	Subtract Memory from Accumulator with Borrow
SEC	Set Carry Flag
SED	Set Decimal Mode
SEI	Set Interrupt Disable Status
*SMB	Set Memory Bit
STA	Store Accumulator in Memory
STX	Store Index X in Memory
STY	Store Index Y in Memory
TAX	Transfer Accumulator to Index X
TAY	Transfer Accumulator to Index Y
TSX	Transfer Stack Pointer to Index X
TXA	Transfer Index X to Accumulator
TXS	Transfer Index X to Stack Register
TYA	Transfer Index Y to Accumulator

A.2 INSTRUCTION SET SUMMARY TABLE

ENHANCED R6502 INSTRUCTION SET

INSTRUCTIONS		IMMEDIATE			ABSOLUTE			ZERO PAGE			ACCUM			IMPLIED			(IND, X)			(IND), Y			Z PAGE, X			ABS, X			ABS, Y			RELATIVE			INDIRECT			Z PAGE, Y			BIT ADDRESSING (OP BY BIT #)								PROCESSOR STATUS CODES							
MNEMONIC	OPERATION	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	0	1	2	3	4	5	6	7	7	6	5	4	3	2	1	0
																																									N	V	-	B	D	I	Z	C
ADC	A + M + C→A (4)(1)	69	2	2	6D	4	3	65	3	2							61	6	2	71	5	2	75	4	2	7D	4	3	79	4	3										N	V	-	-	-	-	Z	C
AND	A M→A (1)	29	2	2	2D	4	3	25	3	2							21	6	2	31	5	2	35	4	2	3D	4	3	39	4	3										N	-	-	-	-	-	Z	-
ASL	C← 7 0 ←0				0E	6	3	06	5	2	0A	2	1										16	6	2	1E	7	3													N	-	-	-	-	-	Z	C
BBR[#(0-7)]	Branch on M_6 = 0 (5)(2)																																																						
BBS[#(0-7)]	Branch on M_6 = 1 (5)(2)																																																					
BCC	Branch on C = 0 (2)																															90	2	2																					
BCS	Branch on C = 1 (2)																															B0	2	2																					
BEQ	Branch on Z = 1 (2)																															F0	2	2																					
BIT	A∧M				2C	4	3	24	3	2																																																
BMI	Branch on N = 1 (2)																															30	2	2																					
BNE	Branch on Z = 0 (2)																															D0	2	2																					
BPL	Branch on N = 0 (2)																															10	2	2																					
BRK	Break																00	7	1																																							
BVC	Branch on V = 0 (2)																															50	2	2																					
BVS	Branch on V = 1 (2)																															70	2	2																					
CLC	0→C																18	2	1																																						
CLD	0→D																D8	2	1																																					
CLI	0→I																58	2	1																																					
CLV	0→V																B8	2	1																																					
CMP	A M (1)	C9	2	2	CD	4	3	C5	3	2							C1	6	2	D1	5	2	D5	4	2	DD	4	3	D9	4	3										N	-	-	-	-	-	Z	C
CPX	X M	E0	2	2	EC	4	3	E4	3	2																																														
CPY	Y M	C0	2	2	CC	4	3	C4	3	2																																														
DEC	M - 1→M				CE	6	3	C6	5	2													D6	6	2	DE	7	3													N	-	-	-	-	-	Z	-
DEX	X - 1→X																CA	2	1																																					
DEY	Y - 1→Y																88	2	1																																				
EOR	A∨M→A (1)	49	2	2	4D	4	3	45	3	2							41	6	2	51	5	2	55	4	2	5D	4	3	59	4	3										N	-	-	-	-	-	Z	-
INC	M + 1→M				EE	6	3	E6															F6	6	2	FE	7	3													N	-	-	-	-	-	Z	-
INX	X + 1→X																EB	2	1																																					
INY	Y + 1→Y																C8	2	1																																					
JMP	Jump to New Loc				4C	3	3																													6C	5	3																
JSR	Jump Sub				20	6	3																																																	
LDA	M→A (1)	A9	2	2	AD	4	3	A5	3	2							A1	6	2	B1	5	2	B5	4	2	BD	4	3	B9	4	3										N	-	-	-	-	-	Z	-
LDX	M→X (1)	A2	2	2	AE	4	3	A6	3	2																			BE	4	3							B6	4	2	N	-	-	-	-	-	Z	-
LDY	M→Y (1)	A0	2	2	AC	4	3	A4	3	2													B4	4	2	BC	4	3													N	-	-	-	-	-	Z	-
LSR	0→ 7 0 →C				4E	6	3	46	5	2	4A	2	1										56	6	2	5E	7	3													0	-	-	-	-	-	Z	C
NOP	No Operation													EA	2	1																																							
ORA	A∨M→A (1)	09	2	2	0D	4	3	05	3	2							01	6	2	11	5	2	15	4	2	1D	4	3	19	4	3										N	-	-	-	-	-	Z	-
PHA	A→Ms S - 1→S													48	3	1																																						
PHP	P→Ms S - 1→S													08	3	1																																						
PLA	S + 1→S Ms→A													68	4	1																									N	-	-	-	-	-	Z	-
PLP	S + 1→S Ms→P													28	4	1																																						(Restored)
RMB[#(0-7)]	0→M_b (5)																																																					
R0L	7 0 C				2E	6	3	26	5	2	2A	2	1										36	6	2	3E	7	3													N	-	-	-	-	-	Z	C
R0R	C 7 0				6E	6	3	66	5	2	6A	2	1										76	6	2	7E	7	3													N	-	-	-	-	-	Z	C
RTI	Rtrn Int													40	6	1																																						(Restored)
RTS	Rtrn Sub													60	6	1																																						
SBC	A - M - C→A (1)	E9	2	2	ED	4	3	E5	3	2							E1	6	2	F1	5	2	F5	4	2	FD	4	3	F9	4	3										N	V	-	-	-	-	Z	(3)
SEC	1→C													38	2	1																																						
SED	1→D													F8	2	1																																						
SEI	1→I													78	2	1																																						
SMB[#(0-7)]	1→M_b (5)																																																					
STA	A→M				8D	4	3	85	3	2							81	6	2	91	6	2	95	4	2	9D	5	3	,	5	3																						
STX	X→M				8E	4	3	86	3	2																															96	4	2												
STY	Y→M				8C	4	3	84	3	2													94	4	2																														
TAX	A→X													AA	2	1																																						
TAY	A→Y													A8	2	1																																					
TSX	S→X													BA	2	1																																					
TXA	X→A													8A	2	1																																					
TXS	X→S													9A	2	1																																					
TYA	Y→A													98	2	1																																					

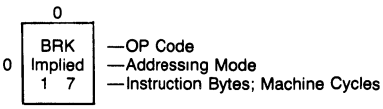
NOTES

1 Add 1 to N if page boundary is crossed
2 Add 1 to N if branch occurs to same page
Add 2 to N if branch occurs to different page
3 Carry not = Borrow
4 If in decimal mode Z flag is invalid accumulator must be checked on zero result
5 Effects 8-bit data field of the specified zero page address

LEGEND

X = Index X
Y = Index Y
A = Accumulator
M = Memory per effective address
M_s = Memory per stack pointer
M_b = Selecter zero page memory bit
M_7 = Memory Bit 7
M_6 = Memory Bit 6
• = Add
– = Subtract
∧ = And
V = Or
∨ = Exclusive Or
n = Number of cycles
# = Number of Bytes

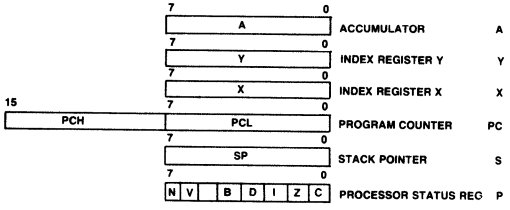
A.3 INSTRUCTION CODE MATRIX



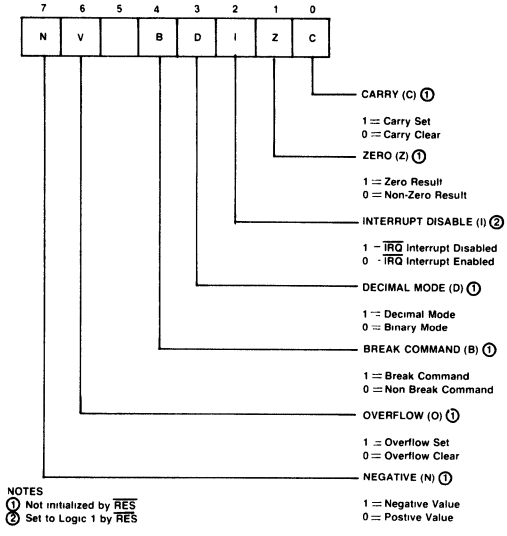
MSD \ LSD	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	MSD
0	BRK Implied 1 7	ORA (IND, X) 2 6				ORA ZP 2 3	ASL ZP 2 5	RMB0 ZP 2 5	PHP Implied 1 3	ORA IMM 2 2	ASL Accum 1 2			ORA ABS 3 4	ASL ABS 3 6	BBR0 ZP 3 5**	0
1	BPL Relative 2 2**	ORA (IND), Y 2 5*				ORA ZP, X 2 4	ASL ZP, X 2 6	RMB1 ZP 2 5	CLC Implied 1 2	ORA ABS, Y 3 4*				ORA ABS, X 3 4*	ASL ABS, X 3 7	BBR1 ZP 3 5**	1
2	JSR Absolute 3 6	AND (IND, X) 2 6			BIT ZP 2 3	AND ZP 2 3	ROL ZP 2 5	RMB2 ZP 2 5	PLP Implied 1 4	AND IMM 2 2	ROL Accum 1 2		BIT ABS 3 4	AND ABS 3 4	ROL ABS 3 6	BBR2 ZP 3 5**	2
3	BMI Relative 2 2**	AND (IND, Y) 2 5*				AND ZP, X 2 4	ROL ZP, X 2 6	RMB3 ZP 2 5	SEC Implied 1 2	AND ABS, Y 3 4*				AND ABS, X 3 4*	ROL ABS, X 3 7	BBR3 ZP 3 5**	3
4	RTI Implied 1 6	EOR (IND, X) 2 6				EOR ZP 2 3	LSR ZP 2 5	RMB4 ZP 2 5	PHA Implied 1 3	EOR IMM 2 2	LSR Accum 1 2		JMP ABS 3 3	EOR ABS 3 4	LSR ABS 3 6	BBR4 ZP 3 5**	4
5	BVC Relative 2 2**	EOR (IND), Y 2 5*				EOR ZP, X 2 4	LSR ZP, X 2 6	RMB5 ZP 2 5	CLI Implied 1 2	EOR ABS, Y 3 4*				EOR ABS, X 3 4*	LSR ABS, X 3 7	BBR5 ZP 3 5**	5
6	RTS Implied 1 6	ADC (IND, X) 2 6				ADC ZP 2 3	ROR ZP 2 5	RMB6 ZP 2 5	PLA Implied 1 4	ADC IMM 2 2	ROR Accum 1 2		JMP Indirect 3 5	ADC ABS 3 4	ROR ABS 3 6	BBR6 ZP 3 5**	6
7	BVS Relative 2 2**	ADC (IND, Y) 2 5*				ADC ZP, X 2 4	ROR ZP, X 2 6	RMB7 ZP 2 5	SEI Implied 1 2	ADC ABS, Y 3 4*				ADC ABS, X 3 4*	ROR ABS, X 3 7	BBR7 ZP 3 5**	7
8		STA (IND, X) 2 6			STY ZP 2 3	STA ZP 2 3	STX ZP 2 3	SMB0 ZP 2 5	DEY Implied 1 2		TXA Implied 1 2		STY ABS 3 4	STA ABS 3 4	STX ABS 3 4	BBS0 ZP 3 5**	8
9	BCC Relative 2 2**	STA (IND, Y) 2 6			STY ZP, X 2 4	STA ZP, X 2 4	STX ZP, Y 2 4	SMB1 ZP 2 5	TYA Implied 1 2	STA ABS, Y 3 5	TXS Implied 1 2			STA ABS, X 3 5		BBS1 ZP 3 5**	9
A	LDY IMM 2 2	LDA (IND, X) 2 6	LDX IMM 2 2		LDY ZP 2 3	LDA ZP 2 3	LDX ZP 2 3	SMB2 ZP 2 5	TAY Implied 1 2	LDA IMM 2 2	TAX Implied 1 2		LDY ABS 3 4	LDA ABS 3 4	LDX ABS 3 4	BBS2 ZP 3 5**	A
B	BCS Relative 2 2**	LDA (IND), Y 2 5*			LDY ZP, X 2 4	LDA ZP, X 2 4	LDX ZP, Y 2 4	SMB3 ZP 2 5	CLV Implied 1 2	LDA ABS, Y 3 4*	TSX Implied 1 2		LDY ABS, X 3 4*	LDA ABS, X 3 4*	LDX ABS, Y 3 4*	BBS3 ZP 3 5**	B
C	CPY IMM 2 2	CMP (IND, X) 2 6			CPY ZP 2 3	CMP ZP 2 3	DEC ZP 2 5	SMB4 ZP 2 5	INY Implied 1 2	CMP IMM 2 2	DEX Implied 1 2		CPY ABS 3 4	CMP ABS 3 4	DEC ABS 3 6	BBS4 ZP 3 5**	C
D	BNE Relative 2 2**	CMP (IND), Y 2 5*				CMP ZP, X 2 4	DEC ZP, X 2 6	SMB5 ZP 2 5	CLD Implied 1 2	CMP ABS, Y 3 4*				CMP ABS, X 3 4*	DEC ABS, X 3 7	BBS5 ZP 3 5**	D
E	CPX IMM 2 2	SBC (IND, X) 2 6			CPX ZP 2 3	SBC ZP 2 3	INC ZP 2 5	SMB6 ZP 2 5	INX Implied 1 2	SBC IMM 2 2	NOP Implied 1 2		CPX ABS 3 4	SBC ABS 3 4	INC ABS 3 6	BBS6 ZP 3 5**	E
F	BEQ Relative 2 2**	SBC (IND), Y 2 5*				SBC ZP, X 2 4	INC ZP, X 2 6	SMB7 ZP 2 5	SED Implied 1 2	SBC ABS, Y 3 4*				SBC ABS, X 3 4*	INC ABS, X 3 7	BBS7 ZP 3 5**	F
	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	

*Add 1 to N if page boundary is crossed.
**Add 1 to N if branch occurs to same page;
add 2 to N if branch occurs to different page.

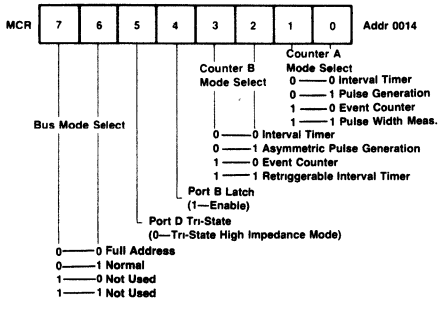
APPENDIX B
KEY REGISTER SUMMARY



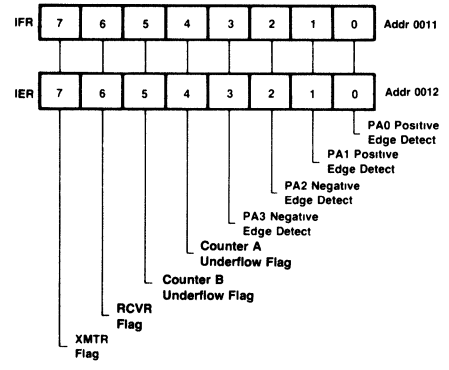
CPU Registers



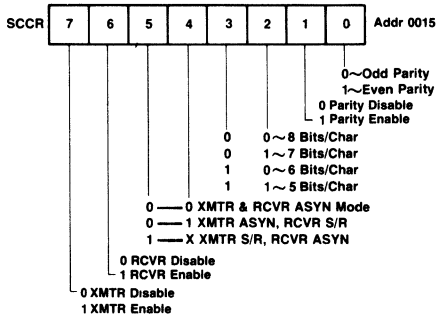
Processor Status Register



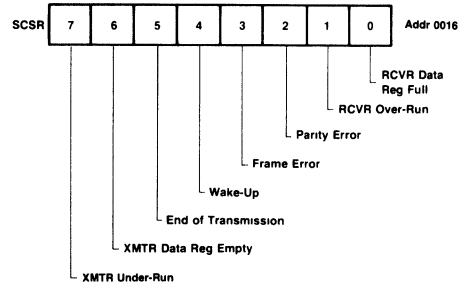
Mode Control Register



Interrupt Enable and Flag Registers



Serial Communications Control Register



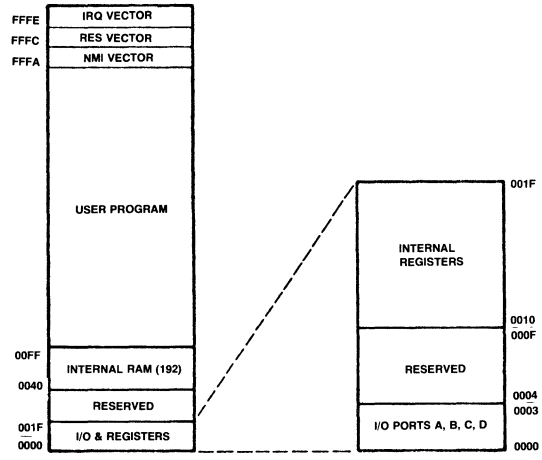
Serial Communications Status Register

APPENDIX C
ADDRESS ASSIGNMENTS/MEMORY MAPS/PIN FUNCTIONS

C.1 I/O AND INTERNAL REGISTER ADDRESSES

ADDRESS (HEX)	READ	WRITE
001F	— —	— —
1E	Lower Counter B	Upper Latch B, Cntr B←Latch B, CLR Flag
1D	Upper Counter B	Upper Latch B, Latch C←Latch B
1C	Lower Counter B, CLR Flag	Lower Latch B
1B	— —	— —
1A	Lower Counter A	Upper Latch A, Cntr A←Latch A, CLR Flag
19	Upper Counter A	Upper Latch A
18	Lower Counter A, CLR Flag	Lower Latch A
17	Serial Receiver Data Register	Serial Transmitter Data Register
16	Serial Comm Status Register	Serial Comm. Status Reg Bits 4 & 5 only
15	Serial Comm. Control Register	Serial Comm. Control Register
14	Mode Control Register	Mode Control Register
13	— —	— —
12	Interrupt Enable Register	Interrupt Enable Register
11	Interrupt Flag Register	— —
0010	Read FF	Clear Int Flag (Bits 0-3 only, Write 0's only)
0F	**RESERVED**	
0E		
0D	These addresses are reserved and are used by the CPU during Read and Write operation over the external Data Bus (D0-D7).	
0C		
0B		
0A		
09		
08		
07		
06		
05		
04		
03	Port D	Port D
02	Port C	Port C
01	Port B	Port B
0000	Port A	Port A

C.2 FULL ADDRESS MODE MEMORY MAP R6501Q



C.4 MULTIPLE FUNCTION PIN ASSIGNMENTS —PORT C AND PORT D

PIN NUMBER	FULL ADDRESS MODE	I/O PORT FUNCTION
54	PC0	PC0
55	PC1	PC1
56	PC2	PC2
57	PC3	PC3
58	PC4	PC4
59	PC5	PC5
60	A13	PC6
61	A14	PC7
62	PD0	PD0
63	PD1	PD1
64	PD2	PD2
1	PD3	PD3
2	PD4	PD4
3	PD5	PD5
4	PD6	PD6
5	PD7	PD7

APPENDIX D
ELECTRICAL SPECIFICATIONS

MAXIMUM RATINGS*

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC} & V_{RR}	−0.3 to +7.0	Vdc
Input Voltage	V_{IN}	−0.3 to +7.0	Vdc
Operating Temperature Range, Commercial	T_A	T_L to T_M 0 to +70	°C
Storage Temperature Range	T_{STG}	−55 to +150	°C

***NOTE:** Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the other sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

3

DC CHARACTERISTICS

(V_{CC} = 5.0V ±5%, V_{RR} = V_{CC}; V_{SS} = 0V; T_A = 0° to 70°C, unless otherwise specified)

Parameter	Symbol	Min	Typ[1]	Max	Unit	Test Conditions
RAM Standby Voltage (Retention Mode)	V_{RR}	3.0		V_{CC}	V	
RAM Standby Current (Retention Mode)	I_{RR}	—	4	—	mA	T_A = 25°C
Input High Voltage All Except XTLI XTLI	V_{IH}	 +2.0 +4.0	 — —	 V_{CC} V_{CC}	V	
Input Low Voltage	V_{IL}	−0.3	—	+0.8	V	
Input Leakage Current $\overline{RES}$, $\overline{NMI}$	I_{IN}	—	—	±10.0	μA	V_{IN} = 0 to 5.0V
Input Low Current PA, PB, PC, PD	I_{IL}	—	−1.0	−1.6	mA	V_{IL} = 0.4V
Output High Voltage (Except XTLO)	V_{OH}	+2.4	—	V_{CC}	V	I_{LOAD} = −100 μA
Output Low Voltage	V_{OL}	—	—	+0.4	V	I_{LOAD} = 1.6 mA
I/O Port Pull-Up Resistance PA0–PA7, PB0–PB7, PC0–PC7	R_L	3.0	6.0	11.5	Kohm	
Output Leakage Current (Three-State Off)	I_{OUT}	—	—	±10	μA	
Input Capacitance XTLI, XTLO All Others	C_{IN}	 — —	 — —	 50 10	pF	T_A = 25°C V_{IN} = 0V f = 1.0 MHz
Output Capacitance (Three-State Off)	C_{OUT}	—	—	10	pF	T_A = 25°C V_{IN} = 0V f = 1.0 MHz
Power Dissipation (Outputs High)	P_D	—	750	1100	mW	T_A = 0°C

Notes:
1. Typical values measured at T_A = 25°C and V_{CC} = 5.0V.
2. Negative sign indicates outward current flow, positive indicates inward flow.

APPENDIX E
TIMING REQUIREMENTS AND CHARACTERISTICS

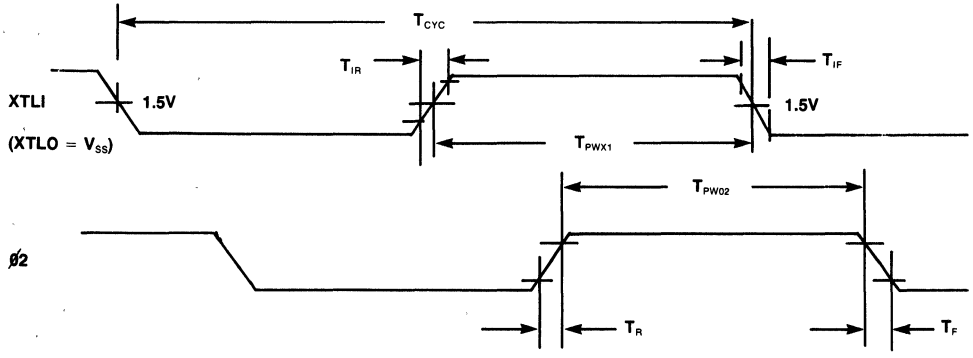
E.1 GENERAL NOTES

1. V_{CC} = 5V ±5%, 0°C ≤ TA ≤ 70°C
2. A valid V_{CC} – $\overline{RES}$ sequence is required before proper operation is achieved.
3. All timing reference levels are 0.8V and 2.0V, unless otherwise specified.
4. All time units are nanoseconds, unless otherwise specified.
5. All capacitive loading is 130pf maximum, except as noted below:

PA, PB	—	50pf maximum
PC (I/O Modes Only)	—	50pf maximum
PC (ABB and Mux Mode)	—	130pf maximum
PC6, PC7 (Full Address Mode)	—	130pf maximum

E.2 CLOCK TIMING

SYMBOL	PARAMETER	1 MHz		2 MHz	
		MIN	MAX	MIN	MAX
T_{CYC}	Cycle Time	1000	10 μs	500	10 μs
T_{PWX1}	XTLI Input Clock Pulse Width XTLO = VSS	500 ± 25	—	250 ± 10	—
T_{PW02}	Output Clock Pulse Width at Minimum T_{CYC}	T_{PWX1}	T_{PWX1} ± 25	T_{PWX1}	T_{PWX1} ± 20
T_R, T_F	Output Clock Rise, Fall Time	—	25	—	15
T_{IR}, T_{IF}	Input Clock Rise, Fall Time	—	10	—	10

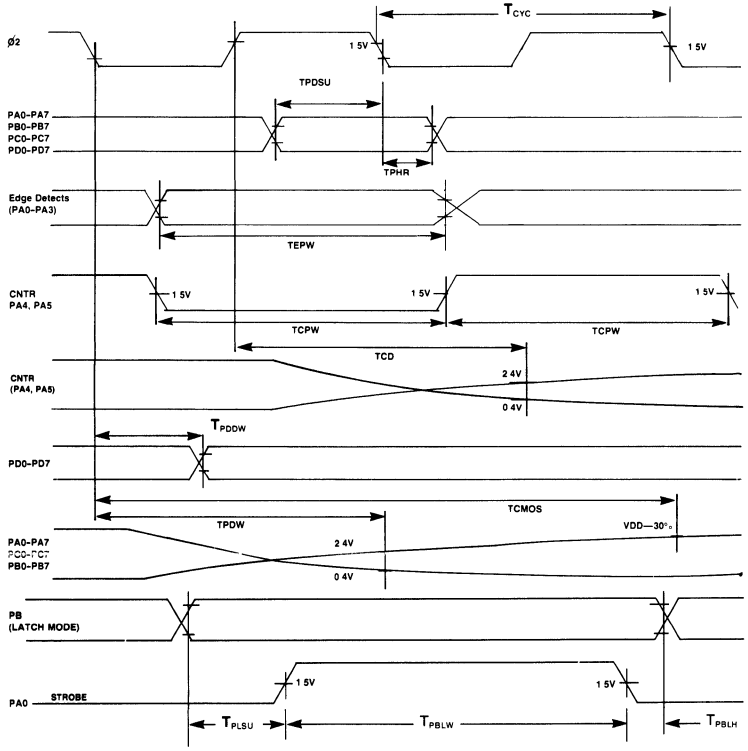


E.3 I/O, EDGE DETECT, COUNTERS, AND SERIAL I/O TIMING

SYMBOL	PARAMETER	1 MHz		2 MHz	
		MIN	MAX	MIN	MAX
	Internal Write to Peripheral Data Valid				
T_{PDW}[1]	PA, PB, PC TTL	—	500	—	500
T_{CMOS}[1]	PA, PB, PC CMOS	—	1000	—	1000
T_{PDDW}	PD	—	175	—	150
	Peripheral Data Setup Time				
T_{PDSU}	PA, PB, PC	200	—	200	—
T_{PDSU}	PD	50	—	50	—
	Peripheral Data Hold Time				
T_{PHR}	PA, PB, PC	75	—	75	—
T_{PHR}	PD	10	—	10	—
T_{EPW}	PA0–PA3 Edge Detect Pulse Width	T_{CYC}	—	T_{CYC}	—
	Counters A and B				
T_{CPW}	PA4, PA5 Input Pulse Width	T_{CYC}	—	T_{CYC}	—
T_{CD}[1]	PA4, PA5 Output Delay	—	500	—	500
	Port B Latch Mode				
T_{PBLW}	PA0 Strobe Pulse Width	T_{CYC}	—	T_{CYC}	—
T_{PLSU}	PB Data Setup Time	175	—	150	—
T_{PBLH}	PB Data Hold Time	30	—	30	—
	Serial I/O				
T_{PDW}[1]	PA6 XMTR TTL	—	500	—	500
T_{CMOS}[1]	PA6 XMTR CMOS	—	1000	—	1000
T_{CPW}	PA4 RCVR S/R Clock Width	4 T_{CYC}	—	4 T_{CYC}	—
T_{PDW}[1]	PA4 XMTR Clock—S/R Mode (TTL)	—	500	—	500
T_{CMOS}[1]	PA4 XMTR Clock—S/R Mode (CMOS)	—	1000	—	1000

NOTE 1 Maximum Load Capacitance 50pF
Passive Pull-Up Required

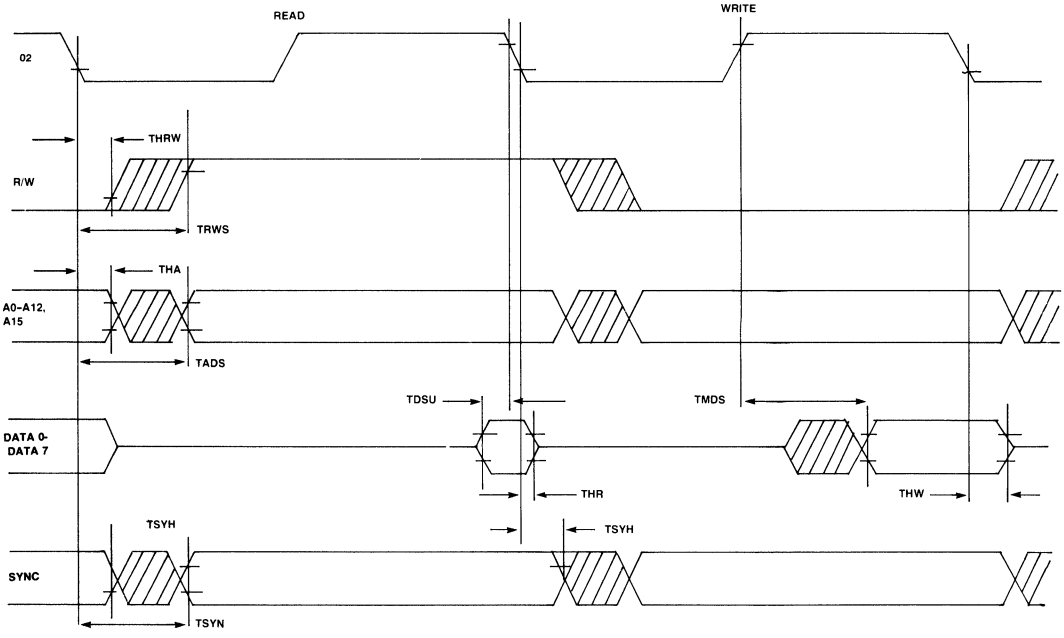
E.3.1 I/O, Edge Detect, Counter, and Serial I/O Timing



E.4 MICROPROCESSOR TIMING (D0-D7, A0-A12, A15, SYNC, R/W)

SYMBOL	PARAMETER	1 MHz		2 MHz	
		MIN	MAX	MIN	MAX
T_{RWS}	R/W Setup Time	—	225	—	140
T_{ADS}	A0-A12, A15 Setup Time	—	150	—	75
T_{DSU}	D0-D7 Data Setup Time	50	—	35	—
T_{HR}	D0-D7 Read Hold Time	10	—	10	—
T_{HW}	D0-D7 Write Hold Time	30	—	30	—
T_{MOS}	D0-D7 Write Output Delay	—	175	—	130
T_{SYN}	SYNC Setup	—	225	—	175
T_{HA}	A0-A12, A15 Hold Time	30	—	30	—
T_{HRW}	R/W Hold Time	30	—	30	—
T_{ACC}	External Memory Access Time $T_{ACC} = T_{CYC} - T_F - T_{ADS} - T_{DSU}$	—	T_{ACC}	—	T_{ACC}
T_{SYH}	SYNC Hold Time	30	—	30	—

E.4.1 Microprocessor Timing Diagram



Rockwell

R6500/1
ONE-CHIP MICROCOMPUTER

SECTION 1
INTRODUCTION

3

The Rockwell R6500/1 microcomputer is a complete 8-bit computer fabricated on a single chip using an N-channel silicon gate MOS process. The R6500/1 complements an established and growing line of R6500 products and has a wide range of microcomputer applications.

The R6500/1 consists of an R6502 Central Processing Unit (CPU), 2048 bytes of Read Only Memory (ROM), 64 bytes of Random Access Memory (RAM) and interface circuitry for peripheral devices.

The innovative architecture and the demonstrated high performance of the R6502 CPU, as well as instruction simplicity, results in system cost-effectiveness and a wide range of computational power. These features make the R6500/1 a leading candidate for microcomputer applications.

To facilitate system and program development for the R6500/1, Rockwell has developed an R6500/1E Emulator part. A description of the R6500/1E is contained in Appendix D.

This product description is for the reader familiar with the R6502 CPU hardware and programming capabilities. A detailed description of the R6502 CPU hardware is included in the R6500 Microcomputer System Hardware Manual (Document Number 29650N31). A description of the instruction capabilities of the R6502 CPU is contained in the R6500 Microcomputer System Programming Manual (Document Order No. 202).

FEATURES

- Single-chip microcomputer
- R6502 software compatible
- Eight-bit parallel processing
- Decimal or binary arithmetic
- Variable length stack
- True indexing capability
- Thirteen addressing modes
- 1 or 2 MHz clock operation, with the following options:
  - — External single clock input
  - — RC time base input
  - — Crystal time base input
- Single +5V power supply
- 500 mw operating power
- Separate power pin for RAM with standby power only 10% of operating power
- 2K x 8 ROM on chip
- 64 x 8 RAM on chip
- 40-pin dual in-line package
- 64-pin Emulator part available, with 40 signals identical to production part
- Pipeline architecture
- 32 bidirectional TTL compatible I/O lines
  - — 1 positive edge sensitive I/O line
  - — 1 negative edge sensitive I/O line
- 1 bidirectional TTL compatible counter I/O line
- 16-bit timer/counter
- Four timer/counter modes
  - — Internal timer
  - — Pulse generator
  - — Event counter
  - — Pulse width measurement
- Three maskable interrupts
  - — 1 counter overflow
  - — 2 I/O edge detect
- NMI and Reset interrupts

SECTION 2
INTERFACE REQUIREMENTS

This section describes the interface requirements for the R6500/1 single chip microcomputer. Figure 2-1 is the Interface Diagram for the R6500/1. Figure 2-2 shows the pin out configuration and Table 2-1 describes the function of each pin of the R6500/1.

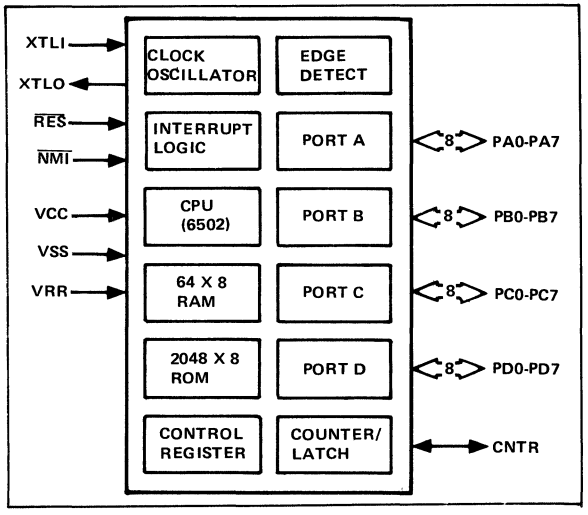


Figure 2-1. R6500/1 Interface Diagram

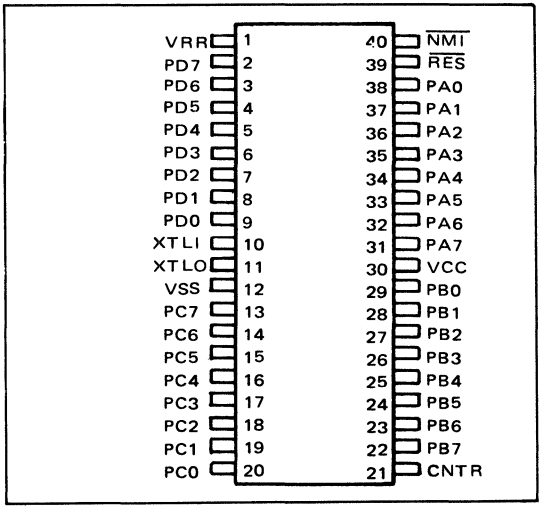


Figure 2-2. R6500/1 Pin Out Designation

Table 2-1. R6500/1 Pin Description

Signal Name	Pin No.	Description
VCC	30	Main power supply +5V
VRR	1	Separate power pin for RAM. In the event that VCC power is lost, this power retains RAM data.
VSS	12	Signal and power ground (0V)
XTLI	10	Crystal, clock or RC network input for internal clock oscillator.
XTLO	1	Crystal or RC network output from internal clock oscillator.
$\overline{RES}$	39	The Reset input is used to initialize the R6500/1. The signal must not transition from low to high for at least eight cycles after VCC reaches operating range and the internal oscillator has stabilized (see section 5). +10V input enables the test mode.
$\overline{NMI}$	40	A negative going edge on the Non-Maskable Interrupt signal requests that a non-maskable interrupt be generated within the CPU.
PA0-PA7 PB0-PB7 PC0-PC7 PD0-PD7	38-31 29-22 20-13 9-2	Four 8-bit ports used for either input/output. Each line consists of an active transistor to VSS and an optional passive pull-up to VCC. The two lower bits of the PA port (PA0-PA1) also serve as edge detect inputs with maskable interrupts.
CNTR	21	This line is used as a Counter input/output line. CNTR is an input in the Event Counter and Pulse Width Measurement modes and is an output in the Interval Timer and Pulse Generator modes. It consists of an active transistor to VSS and an optional passive pull-up to VCC.

SECTION 3
SYSTEM ARCHITECTURE

This section provides a functional description of the R6500/1. A block diagram of the R6500/1 is presented in Figure 3-1.

3.1 INDEX REGISTERS

There are two 8-bit index registers, X and Y. Each index register can be used as a base to modify the address data program counter and thus obtain a new address — the sum of the program counter contents and the and the index register contents.

When executing an instruction which specifies indirect addressing, the CPU fetches the op code and the address, and modifies the address from memory by adding the index register to it prior to loading or storing the value of memory.

Indexing greatly simplifies many types of programs, especially those using data tables.

3.2 STACK POINTER

The Stack Pointer is an 8-bit register. It is automatically incremented and decremented under control of the microprocessor to perform stack manipulation in response to either user instructions or the interrupt lines $\overline{NMI}$ and $\overline{IRQ}$. The Stack Pointer must be initialized by the user program.

The stack allows simple implementation of multiple level interrupts, subroutine nesting and simplification of many types of data manipulation. The JSR, BRK, RTI and RTS instructions use the stack and Stack Pointer.

The stack can be envisioned as a deck of cards which may only be accessed from the top. The address of a memory location is stored (or "pushed") onto the stack. Each time data are to be pushed onto the stack, the Stack Pointer is placed on the Address Bus, data are written into the memory location addressed by the Stack Pointer, and the Stack Pointer is decremented by 1. Each time data are read (or "pulled") from the stack, the Stack Pointer is incremented by 1. The Stack Pointer is then placed on the Address Bus, and data are read from the memory location addressed by the Pointer.

3.3 ARITHMETIC AND LOGIC UNIT (ALU)

All arithmetic and logic operations take place in the ALU, including incrementing and decrementing internal registers

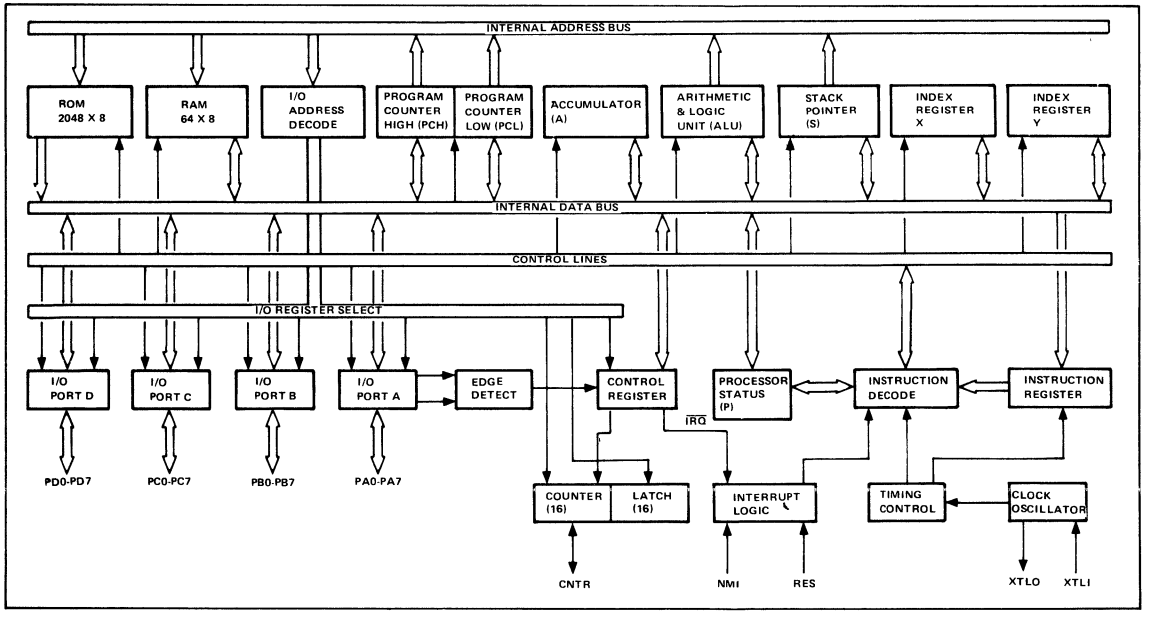


Figure 3-1. R6500/1 Block Diagram

(except the Program Counter). The ALU cannot store data for more than one cycle. If data are placed on the inputs to the ALU at the beginning of a cycle, the result is always gated into one of the storage registers or to external memory during the next cycle.

Each bit of the ALU has two inputs. These inputs can be tied to various internal buses or to a logic zero; the ALU then generates the function (AND, OR, SUM, and so on) using the data on the two inputs.

3.4 ACCUMULATOR

The accumulator is a general purpose 8-bit register that stores the results of most arithmetic and logic operations. In addition, the accumulator usually contains one of the two data words used in these operations.

3.5 PROGRAM COUNTER

The 12-bit Program Counter provides the addresses that are used to step the processor through sequential instructions in a program. Each time the processor fetches an instruction from program memory, the lower (least significant) byte of the Program Counter (PCL) is placed on the low-order bits of the Address Bus and the higher (most significant) byte of the Program Counter (PCH) is placed on the high-order 4 bits of the Address Bus. The Counter is incremented each time an instruction or data is fetched from program memory.

3.6 INSTRUCTION REGISTER AND INSTRUCTION DECODE

Instructions are fetched from ROM or RAM and gated onto the Internal Data Bus. These instructions are latched into the Instruction Register then decoded along with timing and interrupt signals to generate control signals for the various registers.

3.7 TIMING CONTROLS

The Timing Control Logic keeps track of the specific instruction cycle being executed. This logic is set to T0 each time an instruction fetch is executed and is advanced at the beginning of each Phase One clock pulse for as many cycles as are required to complete the instruction. Each data transfer which takes place between the registers is caused by decoding the contents of both the instruction register and timing control unit.

3.8 INTERRUPT LOGIC

Interrupt logic controls the sequencing of three interrupts; $\overline{RES}$, $\overline{NMI}$ and $\overline{IRQ}$. $\overline{IRQ}$ is generated by any one of three conditions: Counter Overflow, PA0 Positive Edge Detected, and PA1 Negative Edge Detected.

3.9 CLOCK OSCILLATOR

The Clock Oscillator provides the basic timing signals used by the R6500/1 CPU. The reference frequency is provided by an external source, and can be from a crystal, clock or RC network input. The RC network mode is a mask option. The external frequency can vary from 200 kHz to 4 MHz. The internal Phase 2 (Ø2) frequency is one-half the external reference frequency. Figure 3-2 shows typical connections.

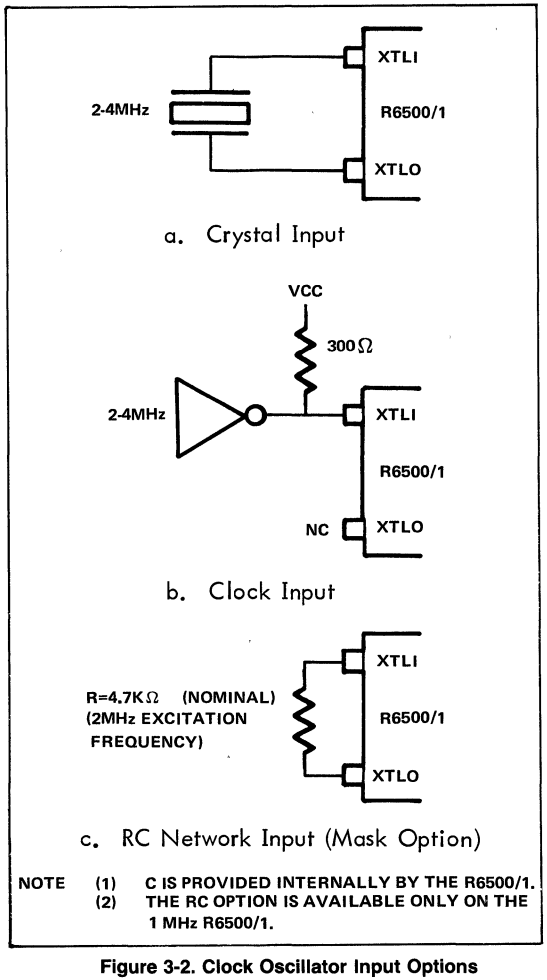


Figure 3-2. Clock Oscillator Input Options

3.10 PROCESSOR STATUS REGISTER

The 8-bit Processor Status Register, shown in Figure 3-3, contains seven status flags. Some of these flags are controlled by the user program; others may be controlled both by the user's program and the CPU. The R6500 instruction

set contains a number of conditional branch instructions which are designed to allow testing of these flags. Each of the eight processor status flags is described in the following sections.

3.10.1 CARRY BIT (C)

The Carry Bit (C) can be considered as the ninth bit of an arithmetic operation. It is set to logic 1 if a carry from the eighth bit has occurred or cleared to logic 0 if no carry occurred as the result of arithmetic operations.

The Carry Bit may be set or cleared under program control by use of the Set Carry (SEC) or Clear Carry (CLC) instruction, respectively. Other operations which affect the Carry Bit are ADC, ASL, CMP, CPX, CPY, LSR, PLP, ROL, ROR, RTI, and SBC.

3.10.2 ZERO BIT (Z)

The Zero Bit (Z) is set to logic 1 by the CPU during any data movement or calculation which sets all 8 bits of the result to zero. This bit is cleared to logic 0 when the resultant 8 bits of a data movement or calculation operation are not all zero. The R6500 instruction set contains no instruction to specifically set or clear the Zero Bit. The Zero Bit is, however, affected by the following instructions: ADC, AND, ASL, BIT, CMP, CPX, CPY, DEC, DEX, DEY, EOR, INC, INX, INY, LDA, LDX, LDY, LSR, ORA, PLA, PLP, ROL, ROR, RTI, SBC, TAX, TAY, TXA, TSX, and TYA.

3.10.3 INTERRUPT DISABLE BIT (I)

The Interrupt Disable Bit (I) is used to control the servicing of an interrupt request (IRQ). If the I Bit is reset to logic 0, the $\overline{IRQ}$ signal will be serviced. If the bit is set to logic 1, the $\overline{IRQ}$ signal will be ignored. The CPU will set the Interrupt Disable Bit to logic 1 if a RESET ($\overline{RES}$) or Non-Maskable Interrupt ($\overline{NMI}$) signal is detected.

The I bit is cleared by the Clear Interrupt (CLI) instruction, the Pull Processor Status from Stack (PLP) instruction, or as the result of executing a Return from Interrupt (RTI) instruction (providing the Interrupt Disable Bit was cleared prior to the interrupt). The Interrupt Disable Bit may be set or cleared under program control using a Set Interrupt Disable (SEI) or a Clear Interrupt Disable (CLI) instruction, respectively.

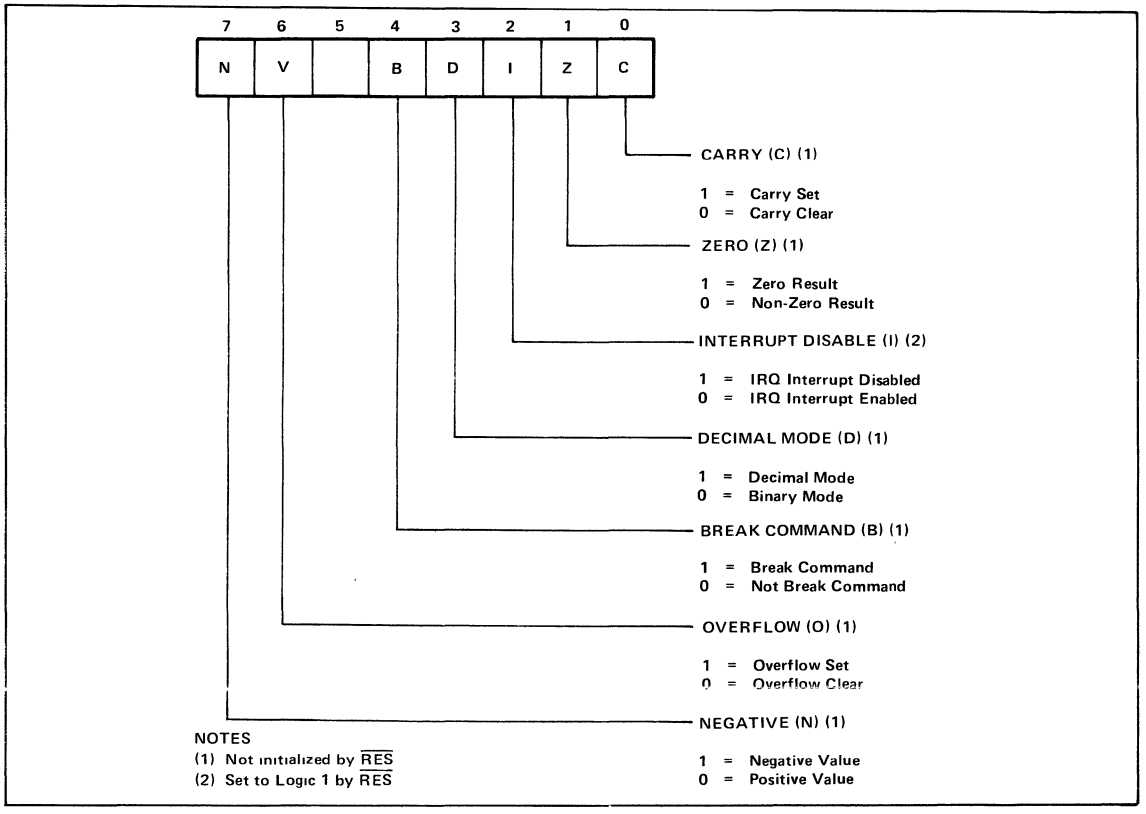


Figure 3-3. Processor Status Register

3.10.4 DECIMAL MODE BIT (D)

The Decimal Mode Bit (D), is used to control the arithmetic mode of the CPU. When this bit is set to logic 1, the adder operates as a decimal adder. When this bit is cleared to logic 0, the adder operates as a straight binary adder. The adder mode is controlled only by the programmer. The Set Decimal Mode (SED) instruction will set the D bit; the Clear Decimal Mode (CLD) instruction will clear it. The PLP and RTI instructions also effect the Decimal Mode Bit.

CAUTION

The Decimal Mode Bit will either set or clear in an unpredictable manner upon power application to R6500/1. This bit must be initialized to the desired state by the user program or erroneous results may occur.

3.10.5 BREAK BIT (B)

The Break Bit (B) is used to determine the condition which caused the $\overline{IRQ}$ service routine to be entered. If the $\overline{IRQ}$ service routine was entered because the CPU executed a BRK command, the Break Bit will be set to logic 1. If the $\overline{IRQ}$ routine was entered as the result of an $\overline{IRQ}$ signal being generated, the B bit will be cleared to logic 0. There are no instructions which can set or clear this bit.

3.10.6 OVERFLOW BIT (V)

The Overflow Bit (V) is used to indicate that the result of a signed, binary addition, or subtraction, operation is a value that cannot be contained in seven bits ($-128 \leq n \leq 127$). This indicator only has meaning when signed arithmetic (sign and seven magnitude bits) is performed. When the ADC or SBC instruction is performed, the Overflow Bit is set to logic 1 if the polarity of the sign bit (bit 7) is changed because the result exceeds +127 or -128; otherwise the bit is cleared to logic 0. The V bit may also be cleared by the programmer using a Clear Overflow (CLV) instruction.

The Overflow Bit may also be used with the BIT instruction. The BIT instruction which may be used to sample interface devices, allows the overflow flag to reflect the condition of bit 6 in the sampled field. Durliing a BIT instruction the Overflow Bit is set equal to the content of the bit 6 on the data tested with BIT instruction. When used in this mode, the overflow has nothing to do with signed arithmetic, but is just another sense bit for the microprocessor. Instructions which affect the V flag are ADC, BIT, CLV, PLP, RTI and SBC.

3.10.7 NEGATIVE BIT (N)

The Negative Bit (N) is used to indicate that the sign bit (bit 7), in the resulting value of a data movement or data arithmetic operation, is set to logic 1. If the sign bit is set to logic 1, the resulting value of the data movement or arithmetic operation is negative; if the sign bit is cleared, the result of the data movement or arithmetic operation s positive. There are no instructions that set or clear the Negative Bit since the Negative Bit represents only the status of a result. The instructions that effect the state of the Negative Bit are: ADC, AND, ASL, BIT, CMP, CPX, CPY, DEC, DEX, DEY, EOR, INC, INX, INY, LDA, LDX, LDY, LSR, ORA, PLA, PLP, ROL, ROR, RTI, SBC, TAX, TAY, TSX, TXA, and TYA.

3.11 2K × 8 ROM

The R6500/1 2048 byte × 8-bit Read Only Memory (ROM) usually contains the user's program instructions and other fixed constants. These program instructions and constants are mask-programmed into the ROM during fabrication of the R6500/1 device. The R6500/1 ROM is memory mapped from 800 to FFF.

3.12 64 × 8 RAM

The 64 byte × 8-bit Random Access Memory (RAM) contains the user program stack and is used for scratchpad memory during system operation. This RAM is completely static in operation and requires no clock or dynamic refresh. The data contained in RAM is read out nondestructively with the same polarity as the input data. A standby power pin, V_{RR} allows RAM memory to be maintained on 10% of the operating power. In the event that VCC power is lost and execution stops, this standby power retains RAM data until execution resumes.

In order to take advantage of zero page addressing capabilities, the R6500/1 RAM is assigned page zero memory address 0 to 03F.

3.13 CONTROL REGISTER

The Control Register (CR), shown in Figure 3-4, is located at address 08F. The CR contains five control signals and three status signals.

The control signals are summarized in Table 3-1. The control signals are set to logic 1 by writing logic 1 into the respective bit positions and cleared to logic 0 either by writing logic 0 into the respective bit position or by the occurrence of a $\overline{RES}$ signal.

Table 3-1. CR Control Signals

Control Signal Name	Bit Number
Counter Mode Control 0 (CMC0)	0
Counter Mode Control 1 (CMC1)	1
PA1 Interrupt Enabled (A1IE)	2
PA0 Interrupt Enabled (A0IE)	3
Counter Interrupt Enabled (CIE)	4

The three status signals are summarized in Table 3-2.

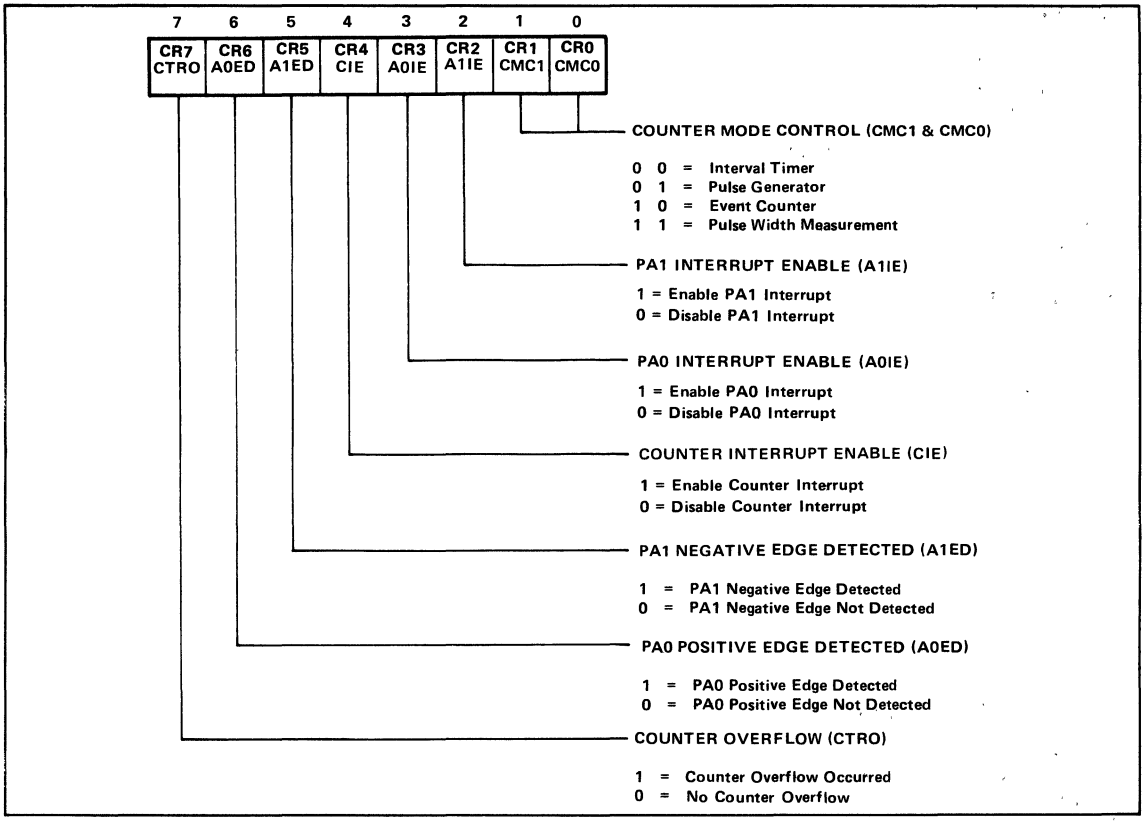


Figure 3-4. Control Register (CR)

Table 3-2. CR Status Signals

Status Signal Name	Bit Number
PA1 Negative Edge Detected (A1ED)	5
PA0 Positive Edge Detected (A0ED)	6
Counter Overflow (CTRO)	7

The status signals are read-only information. The status bits are set to logic 1 by hardware monitoring logic and cleared to logic 0 by the occurrence of $\overline{RES}$ signal or by specific address commands. Each of these signals is described in the following sections.

3.13.1 COUNTER MODE CONTROL 0 AND 1

Counter Mode Control signals CMC0 and CMC1 (bits 0 and 1) control the Counter operating modes. The modes of operation and the corresponding configuration of CMC0 and CMC1 are summarized in Table 3-3.

These modes are controlled by writing the appropriate bit values into the Counter Mode Control bits.

Table 3-3. Counter Mode Control Selection

CMC1 (Bit 1)	CMC0 (Bit 0)	Mode
0	0	Interval Timer
0	1	Pulse Generator
1	0	Event Counter
1	1	Pulse Width Measurement

The Counter is set to the Interval Timer Mode (00) when a $\overline{RES}$ signal is generated or if the user program stores logic 0 into Bits 0 and 1 of the Control Register. A complete description of each of the Counter modes is given in Section 3.14.1.

3.13.2 PA1 INTERRUPT ENABLE BIT (A1IE)

If the PA1 Interrupt Enable Bit (CR2) is set to logic 1, an $\overline{IRQ}$ interrupt request signal will be generated when the PA1 Negative Edge Detected Bit (CR5) is set.

3.13.3 PA0 INTERRUPT ENABLE BIT (A0IE)

If the PA0 Interrupt Enable Bit (CR3) is set to logic 1, the $\overline{IRQ}$ interrupt request signal will be generated when the PA0 Positive Edge Detected Bit (CR6) is set.

3.13.4 COUNTER INTERRUPT ENABLE BIT (CIE)

If the Counter Interrupt Enable Bit (CR4) is set to logic 1, the $\overline{IRQ}$ interrupt request signal will be generated when Counter Overflow (CR7) is set.

3.13.5 PA1 NEGATIVE EDGE DETECTED BIT (A1ED)

The PA1 Negative Edge Detected Bit (CR5) is set to logic 1 whenever a negative (falling) edge is detected on PA1. This bit is cleared to logic 0 by $\overline{RES}$ or by writing to address 08A.

The edge detecting circuitry is active when PA1 is used either as an input or as an output. When PA1 is used as an output, A1ED will be set when the negative edge is detected during a logical 1 to 0 transition.

When PA1 is used as an input and the negative edge detecting circuitry is used, A1ED should be cleared by the user program upon initialization and when the PA1 Negative Edge Detected $\overline{IRQ}$ processing is completed.

3.13.6 PA0 POSTIIVE EDGE DETECTED BIT (A0ED)

The PA0 Positive Edge Detected Bit (CR6) is set to logic 1 whenever a positive (rising) edge is detected on PA0. The bit is cleared to logic 0 by $\overline{RES}$ or by writing to address 089.

The edge detecting circuitry is active when PA0 is used either as an input or as an output. When PA0 is used as an output, A0ED will be set when the positive edge is detected during a logical 0 to 1 transition.

When PA0 is used as an input and the positive edge detecting circuitry is used, A0ED should be cleared by the user program upon initialization and upon completion of PA0 Positive Edge Detected $\overline{IRQ}$ processing.

3.13.7 COUNTER OVERFLOW BIT (CTRO)

The Counter Overflow Bit (CR7) is set to logic 1 whenever a counter overflow occurs in any of the four counter operating modes. Overflow occurs when the counter is decremented one count from 0000. This bit is cleared to logic 0 by $\overline{RES}$ or by reading from address 087 or writing to address 088.

This bit should be cleared by the user program upon initialization and upon completion of Counter Overflow $\overline{IRQ}$ interrupt processing.

When a Counter Overflow occurs, the Upper Count (UC) in address 086 and the Lower Count (LC) in address 087 are reset to the values contained in the Upper Latch (UL) in address 084 and in the Lower Latch (LL) in address 085, respectively. Therefore, it is important to load the Lower Latch value prior to executing the Write to Upper Latch and Transfer Latch to Counter (address 088) in order to prevent an unpredicted reoccurrence of Counter Overflow and, if enabled, an $\overline{IRQ}$ interrupt request.

3.14 COUNTER/LATCH

The Counter/Latch consists of a 16-bit Counter and a 16-bit Latch. The Counter resides in two 8-bit registers: address 086 contains the Upper Count value (bits 8-15 of the Counter) and address 087 contains the Lower Count value (bits 0-7 of the Counter). The Counter contains the count of either Ø2 clock periods or external events depending on which counter mode is selected in the Control Register (Section 3.13.1).

The Latch contains the Counter initialization value. The Latch resides in two 8-bit registers: address 084 contains the Upper Latch value (bits 8-15 of the Latch) and address 085 contains the Lower Latch value (bits 0-7 of the Latch). The 16-bit Latch can hold values from 0 to 65535.

The Latch registers can be loaded at any time by executing a write to the Upper Latch Address (084) and the Lower Latch Address (085). In each case, the contents of the Accumulator are copied into the applicable Latch register. The Upper Latch and Lower Latch can be loaded independently; it is not required to load both registers at the same time or sequentially. The Upper Latch can also be loaded by writing to address 088.

The Counter can be initialized at any time by writing to address 088. The contents of the Accumulator will be copied into the Upper Latch before the value in the Upper Latch is transferred to the Upper Counter.

The Counter will also be initialized to the Latch value whenever the Counter overflows. When the Counter decrements from 0000, the next Counter value will be the Latch value, not FFFF.

Whenever the Counter overflows, the Counter Overflow Bit (CR7) is set to logic 1. This bit is cleared whenever the lower eight bits of the counter are read from address 087 or by writing to address 088.

3.14.1 COUNTER MODES

The Counter operates in any of four modes. These modes are selected by the Counter Mode Control bits in the Control Register.

Mode	CMC1	CMC0
Interval Timer	0	0
Pulse Generator	0	1
Event Counter	1	0
Pulse Width Measurement	1	1

The Interval Timer, Pulse Generator, and Pulse Width Measurement Modes are ø2 clock counter modes. The Event Counter Mode counts the occurrences of an external event on the CNTR line.

Interval Timer (Mode 0)

In the Interval Timer mode the Counter is initialized to the Latch value by either of two conditions:

1. When the Counter is decremented from 0000, the next Counter value is the Latch value (not FFFF).
2. When a write operation is performed to the Load Upper Latch and Transfer Latch to counter address (088), the Counter is loaded with the Latch value. Note that the contents of the Accumulator are loaded into the Upper Latch before the Latch value is transferred to the Counter.

The Counter value is decremented by one count at the ø2 clock rate. The 16-bit Counter can hold from 1 to 65535 counts The Counter Timer capacity is therefore 1μs to 65.535ms at the 1 MHz ø2 clock rate or 0.5μs to 32.768ms at the 2 MHz ø2 clock rate. Time intervals greater than the maximum Counter value can be easily measured by counting $\overline{IRQ}$ interrupt requests in the counter $\overline{IRQ}$ interrupt routine.

When the Counter decrements from 0000, the Counter Overflow (CR7) is set to logic 1 at the next ø2 clock pulse. If the Counter Interrupt enable bit (CR4) is also set, an $\overline{IRQ}$ interrupt request will be generated. The Counter Overflow bit in the Control Register can be examined in the $\overline{IRQ}$ interrupt routine to determine that the $\overline{IRQ}$ was generated by the Counter Overflow.

While the timer is operating in the Interval Timer Mode, the Counter Out/Event line is held in the high (output disabled) state.

A timing diagram of the Interval Timer Mode is shown in Figure 3-5.

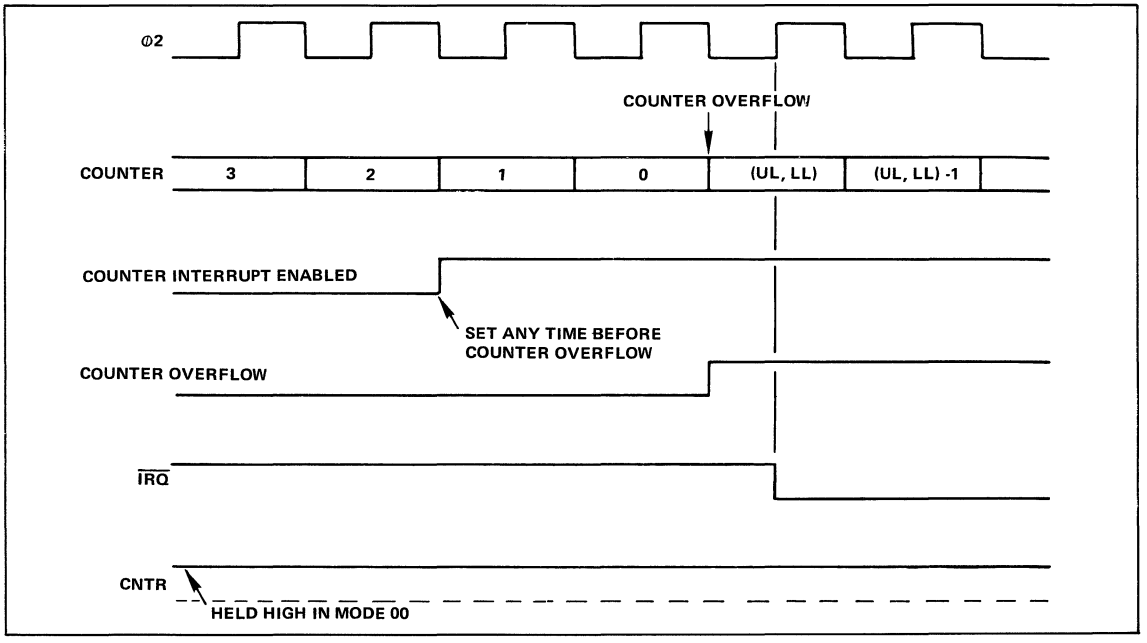


Figure 3-5. Interval Timer (Mode 0) Timing Diagram

Pulse Generator Mode (Mode 1)

In the Pulse Generator mode, the Counter Out/Event In line (CNTR) operates as a Counter Out. The CNTR line toggles from low to high or from high to low whenever a Counter Overflow occurs, or a write is performed to address 088.

Either a symmetric or asymmetric output waveform can be output on the CNTR line in this mode. The CNTR output is initialized high by a $\overline{RES}$ since the Interval Timer mode is established by $\overline{RES}$.

A one-shot waveform can be easily generated by changing from Mode 1 Pulse Generator to Mode 0 (Interval Timer) after only one occurrence of the output toggle condition.

Event Counter Mode (Mode 2)

In this mode the CNTR line is used as an Event Counter. The Counter will decrement with each rising edge detected on this line. The maximum rate at which this edge can be detected is one-half the ϕ2 clock rate.

The Counter can count up to 65,535 occurrences before overflowing. As in the other modes, the Counter Overflow bit (CR7) is set to logic 1 if the overflow occurs.

Figure 3-6 is a timing diagram of the Event Counter Mode.

Pulse Width Measurement Mode (Mode 3)

This mode allows the accurate measurement of a low pulse duration on the CNTR line. In this mode, CNTR is used in the Event In capacity. The Counter decrements by one count at the ϕ2 clock rate as long as the CNTR line is held in the low state. The Counter is stopped when CNTR is in the high state.

If the CNTR pin is left disconnected, this mode may be selected to stop the Counter since the internal pull-up device will cause the CNTR input to be in the high (>2.0V) state.

A timing diagram for the Pulse Width Measurement Mode is shown in Figure 3-7.

3.15 INPUT/OUTPUT PORTS

The R6500/1 provides four 8-bit Input/Output (I/O) ports (PA, PB, PC, PD). These 32 I/O lines are completely bidirectional. All lines may be used either for input or output in any combination; that is, there are no line grouping or port association restrictions.

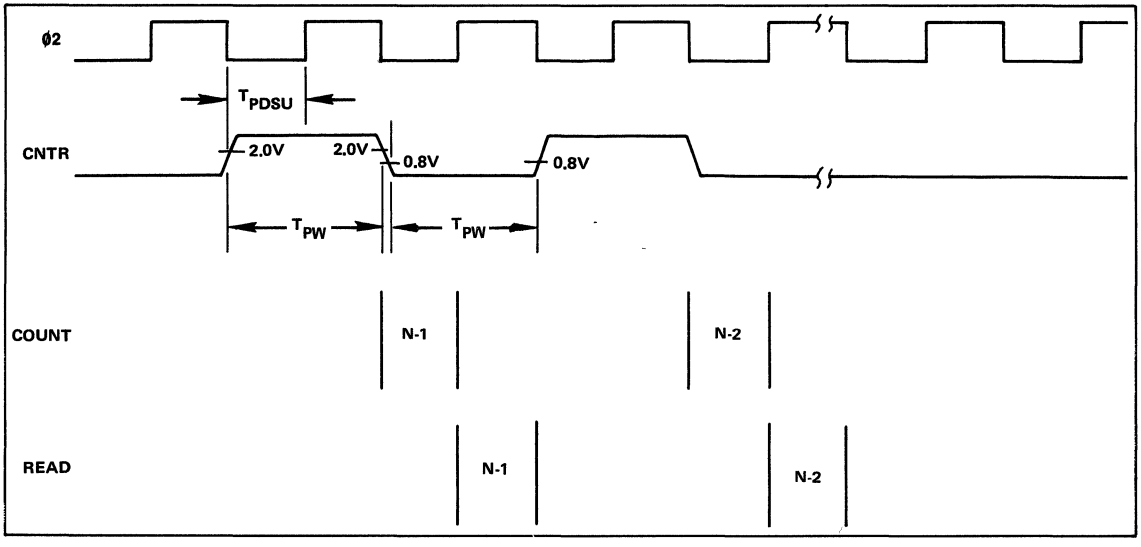


Figure 3-6. Event Counter Mode (Mode 2)

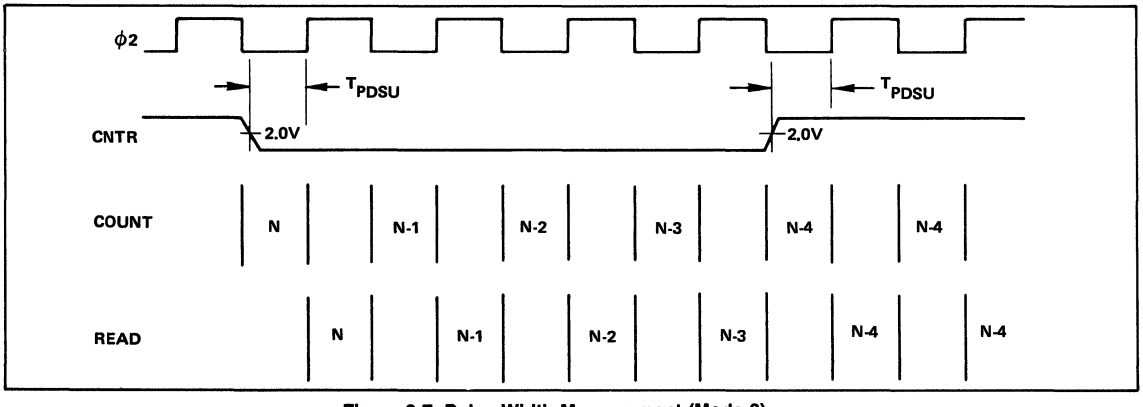


Figure 3-7. Pulse Width Measurement (Mode 3)

The direction of the 32 I/O lines are controlled by four 8-bit port registers located in page zero. This arrangement provides quick programming access using simple two-byte zero page address instructions. There are no direction registers associated with the I/O ports, which simplifies I/O handling. The I/O addresses are shown in Table 3-4.

Table 3-4. I/O Port Addresses

Port	Address
A	080
B	081
C	082
D	083

Figure 3-8 shows the I/O Port Timings.

3.15.1 INPUTS

Inputs are enabled by loading logic 1 into all I/O port register bit positions that are to correspond to I/O input lines. A low (<0 8V) input signal will cause a logic 0 to be read when a read instruction is issued to the port register A high (>2.0V) input will cause a logic 1 to be read. An $\overline{RES}$ signal forces all I/O port registers to logic 1 thus initially treating all I/O lines as inputs.

The status of the input lines can be interrogated at any time by reading the I/O port addresses. Note that this will return the actual status of the input lines, not the data written into the I/O port registers.

3.15.2 OUTPUTS

Outputs are controlled by writing the desired I/O line output states into the corresponding I/O port register bit positions. A logic 1 will force a high (>2.4V) output while a logic 0 will force a low (<0.4V) output.

3.15.3 EDGE DETECTION CAPABILITY

Ports PA0 and PA1 have an edge detection capability. Figure 3-9 shows the edge detection timing.

PA0 Positive Edge Detecting Capability

In addition to its normal I/O function, PA0 will detect an asynchronous positive (rising) edge signal and set the PA0 Positive Edge Detected signal (CR6) to logic 1. The maximum rate at which this positive edge can be detected is one-half the Ø2 clock rate.

If the PA0 Interrupt Enable Bit (CR3) is set, an $\overline{IRQ}$ interrupt request will also be generated. The PA0 Positive Edge Detected signal can be cleared by writing to address 089.

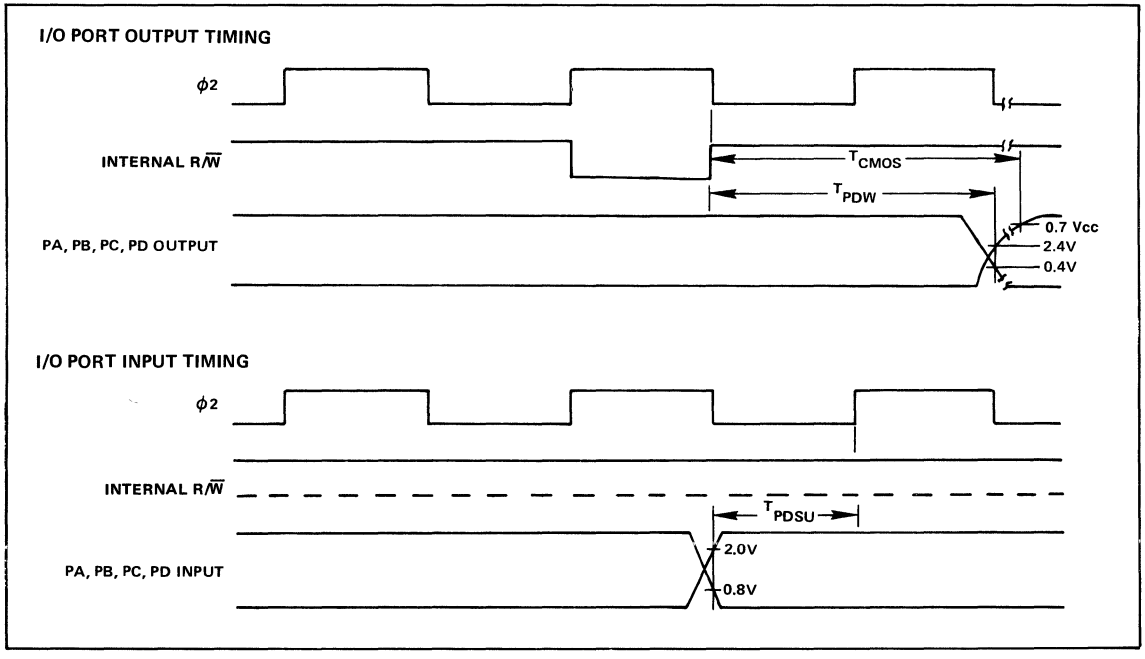


Figure 3-8. I/O Port Timing

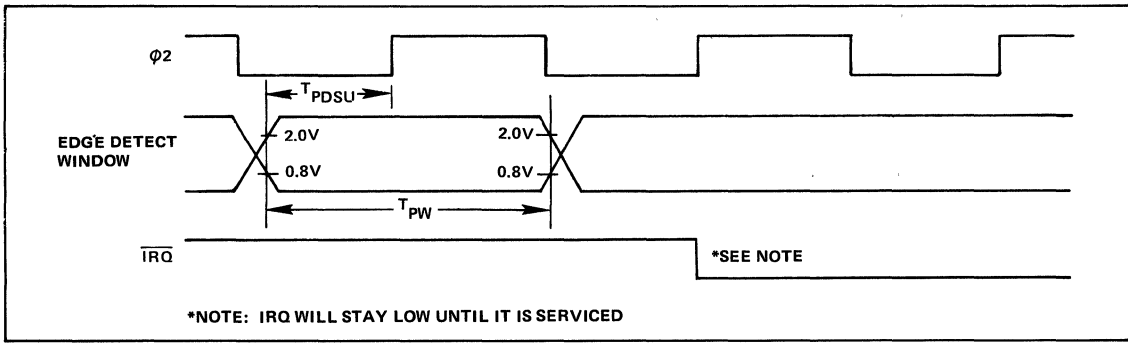


Figure 3-9. PA0 and PA1 Edge Detection Timing

PA1 Negative Edge Detecting Capability

In addition to its normal I/O function, PA1 will detect an asynchronous negative (falling) edge signal and set the PA1 Negative Edge Detected signal (CR5) to logic 1. The maximum rate at which this negative edge can be detected is one-half the ∅2 clock rate.

If the PA1 Interrupt Enable signal (CR2) is set, an $\overline{IRQ}$ interrupt request will also be generated. The PA1 Negative Edge Detected signal may be cleared by writing to address 08A.

3.16 MASK OPTIONS

An option is provided to delete the internal pull-up resistance from PA, PB, PC and/or PD ports at mask time. This option is available for 8-bit port groups only, not for individual port lines. This option may by used to aid interface with CMOS drivers, or in order to interface with external pull-up devices.

An option is also provided to delete the internal pull-up resistance on the CNTR line.

SECTION 4
$\overline{\text{IRQ}}$ INTERRUPT REQUEST GENERATION

An $\overline{\text{IRQ}}$ interrupt request can be initiated by any or all of three possible sources. These sources are all capable of being enabled or disabled by the use of the appropriate interrupt enabled bits in the Control Register.

The first source of $\overline{\text{IRQ}}$ is Counter Overflow. The $\overline{\text{IRQ}}$ interrupt request will be driven low whenever both the Counter Interrupt Enable (CR4) and the Counter Overflow (CR7) are logic 1.

The second source of $\overline{\text{IRQ}}$ is detection of a positive edge on PA0. The $\overline{\text{IRQ}}$ inerrupt request will be driven low whenever both the PA0 Interrupt Enable (CR3) and the PA0 Positive Edge Detected (CR6) are logic 1.

The third source of $\overline{\text{IRQ}}$ is detection of a negative edge on PA1. The $\overline{\text{IRQ}}$ interrupt request will be driven low whenever both the PA1 Interrupt Enable (CR2) and the PA1 Negative Edge Detected (CR5) are logic 1.

Multiple simultaneous interrupts will cause the $\overline{\text{IRQ}}$ interrupt request to remain active until all interrupting conditions have been serviced and cleared.

CAUTION

If the same data, i.e., the same RAM, counter/latch or I/O addresses, are operated on asynchronously by a normal processing routine and by an interrupt service routine, care must be taken to prevent loss of data due to the interrupt routine altering the data during update of the data by the normal processing routine. This situation can be prevented by disabling the $\overline{\text{IRQ}}$ interrupt with the SEI instruction before starting the data update in the normal processing and then enabling the interrupt with the CLI instruction upon completion of data update.

3

SECTION 5
POWER ON/OFF CONSIDERATIONS

5.1 POWER-ON RESET

The occurrence of $\overline{RES}$ going from low to high will cause the R6500/1 to set the Interrupt Mask Bit — bit 2 of the Processor Status Register — and initiate a reset vector fetch at address FFE and FFF to begin user program execution. All of the I/O ports (PA, PB, PC, and PD) and CNTR will be forced to the high (logic 1) state. All bits of the Control Register will be cleared to logic 0 causing the Interval Timer counter mode (mode 00) to be selected and causing all interrupt enabled bits to be reset.

5.2 POWER ON/OFF TIMING

After application of VCC power to the R6500/1, $\overline{RES}$ must be held low for at least eight Ø2 clock cycles after VCC reaches operating range and the internal clock oscillator has stabilized. This stabilization time is dependent upon the input VCC voltage and performance of the crystal, clock, or RC network input circuit. The clock oscillator output can be monitored on XTLO (pin 11).

Figure 5-1 illustrates the power turn-on waveforms.

5.3 RAM DATA RETENTION — VRR REQUIREMENTS

For the RAM to retain data upon loss of VCC, VRR must be supplied within operating range and $\overline{RES}$ must be driven low at least eight Ø2 clock pulses before VCC falls out of operating range. RES must then be held low while VCC is out of operating range and until at least eight Ø2 clock cycles after VCC is again within operating range and the internal Ø2 oscillator is stabilzed. VRR must remain within VCC operation range during normal R6500/1 operation. When VCC is out of operating range, VRR must remain within the VRR retention range in order to retain data. Figure 5-2 shows typical waveforms.

5.4 RAM DATA RETENTION OPERATION

The requirement for R6500/1 RAM data retention and restart operation is application dependent. If R6500/1 RAM data retention is not required during loss of VCC, then VRR can be connected to the same power source as VCC. With this configuration a complete initialization of R6500/1 program variables in RAM is required upon VCC and VRR power application.

If the R6500/1 RAM is to retain data during loss of VCC, the following is required:

1. Connection of VCC and VRR to separate power supplies or to the same primary power supply with isolation diodes and battery or other backup power for VRR.
2. VCC power monitor hardware with power loss and cold/warm start indications to the R6500/1.
3 Power loss detection as well as cold and warm start initialization in the R6500/1 program.

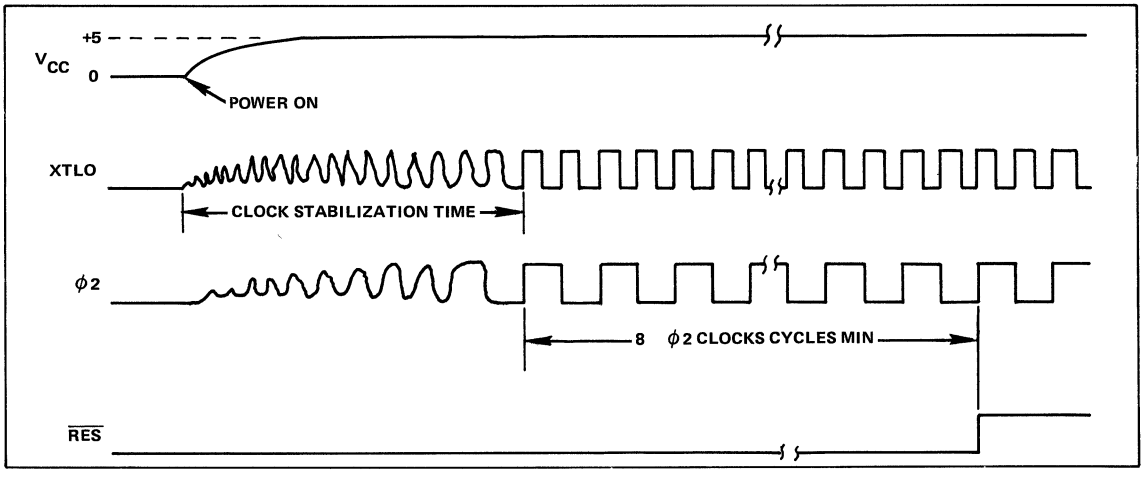
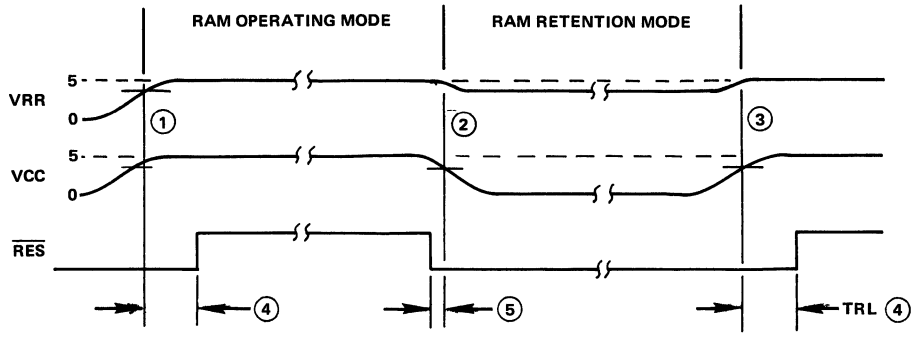


Figure 5-1. Power Turn-On Timing Detail



(1) INITIAL APPLICATION OF VCC AND VRR.

(2) LOSS OF VCC, RAM ON STANDBY POWER.

(3) REAPPLICATION OF VCC.

(4) ⩾8 ϕ2 CLOCK PULSES AFTER ϕ2 OSCILLATOR STABILIZATION.

(5) ⩾8 ϕ2 CLOCK PULSES.

Figure 5-2. RAM Retention Mode Timing

The power monitor hardware must sense the loss of VCC power in sufficient time to allow the R6500/1 to save required CPU register data in RAM. The power loss indication line can be connected to the $\overline{\text{NMI}}$ interrupt input in order to cause an immediate R6500/1 interrupt upon power loss detection.

The power monitor hardware should also provide an indication of cold start (initial VCC and VRR power application) or warm start (VCC power re-application while VRR is retained on backup power) provided as input on a data I/O pin.

A level indication is sufficient. The R6500/1 program can then initialize all, or partial, program variables upon initialization then jump to any other starting address as required depending upon cold/warm start condition.

Upon power loss detection, the R6500/1 should save all required CPU register data in either the stack or dedicated RAM. The stack may be preferred if dedicated RAM is not available. If the program is to restart at the interrupted address, then all CPU registers must be saved, i.e., S, P, PC, A, X, and Y. The stack pointer must be saved in a dedicated RAM address. Note that processor status P and the program counter, PC, are already saved on the stack by the NMI interrupt R6500/1 hardware processing. If the warm start can be performed at a specific address, then the saving of the register data at power loss detection may not be required. Figure 5-3 shows top level flowcharts of typical power down and power-up processing.

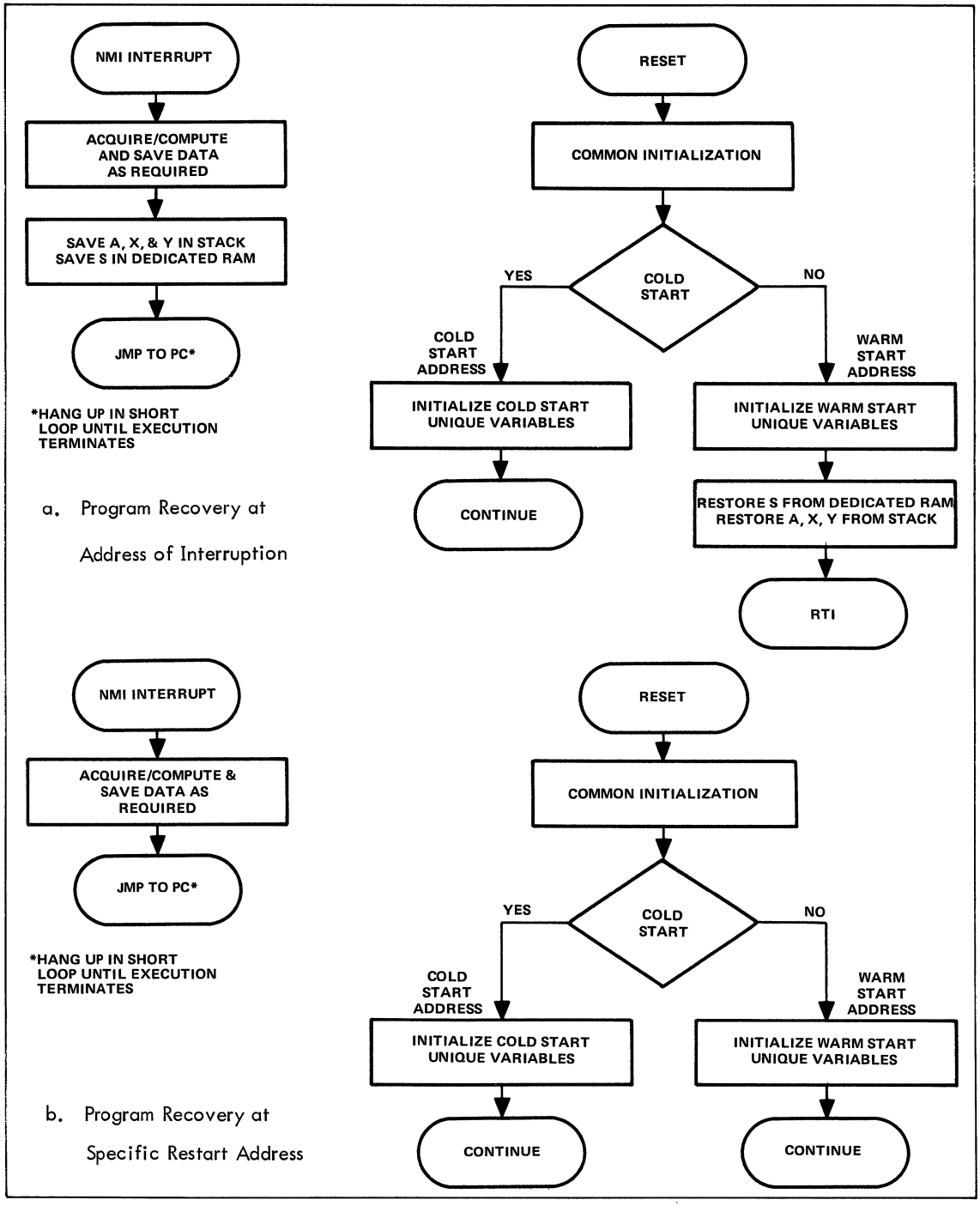


Figure 5-3. Typical R6500/1 Power Loss Recovery Flowcharts

SECTION 6
TEST

6.1 TEST MODE

The R6500/1 test function is multiplexed on the $\overline{RES}$ input pin. The three input states for this pin are:

1. <0.8V	Reset state. All R6500/1 outputs are forced to the high state.
2. >2.0V and <5.5V	Normal run state. The low to high transition on the $\overline{RES}$ pin initiates fetch of the reset vector from address FFC and FFD and starts user program execution at the vectored address.
3. >10.0V and <10.5V	Test state. The only internal action that takes place is switching of the data source for instruction memory from internal ROM to I/O port "C". Bit 0 of port "C" is the data least significant bit (LSB).

The test mode allows instructions and data to be input externally through I/O port "C". This capability is used at Rockwell to test all of the R6500/1 logic, registers and internal data RAM A ROM dump may be accomplished by using the test feature to load into the internal RAM a small program to fetch each byte of ROM and output it to an I/O port. After this program is loaded the CPU is directed to begin execution out of RAM, e.g., JMP to 00. After the jump is executed, the $\overline{RES}$ line is returned to the normal run state. The normal run state allows data fetches to occur out of the internal ROM and returns port "C" to its normal function.

The detail support hardware and software required to use the R6500/1 test mode is fairly complex and time critical. For normal application testing, it is recommended that a test program be loaded into RAM and executed as explained in Section 6.2.

6.2 PROGRAM LOADING INTO RAM

A test or application program can easily be loaded into the R6500/1 RAM and executed without forcing the R6500/1 into the test mode. To do this, a short program loader function must be permanently included in the application program stored in ROM. Upon test mode selection during R6500/1 initialization, the loader reads instructions or data from an I/O port and stores them into RAM. At the first completion of the load, the loader then jumps to the first instruction in RAM to start program execution.

A program is described which may be used to load test or application program into RAM. It can easily be adapted to specific requirements by re-assigning I/O as required. The loader uses positive handshake between the R6500/1 and the interfacing host equipment. One I/O line is dedicated to the test mode selection. The other pins assigned to loader interface signals may be assigned to normal application I/O interface signals when the test mode is not selected.

I/O is assigned for the RAM Program Loader as follows:

PA0	Data Ready (DR) — Positive edge indicates data is ready for sampling by the R6500/1.
PA1	End of Data ($\overline{EOD}$) — Negative edge indicates that all the data has been transferred to the R6500/1.
PA2	Data Taken (DT) — 0 = Data Not Taken 1 = Data Taken
PA7	Normal Mode Select (NMS) — 0 = Test Mode 1 = Normal Mode
PB7-PB0	Data input, i.e., instruction or data (PB7 = MSB, PB0 = LSB)

The flowchart in Figure 6-1 shows the loader operation. The handshake waveforms between the R6500/1 and the host are illustrated in Figure 6-2. The following description corresponds to the handshake events identified in Figure 6-2:

1) Host sees PA2 high, which indicates previous data, if any, has been taken by the R6500/1. The host then drops PA0 low to indicate new data is not ready. This signal should be initialized low by the host.
2) R6500/1 detects PA0 low then drops PA2 low to indicate that data has not been taken.
3) Host sees PA2 low then sets up new data.
4) Host sets PA0 high to indicate new data is ready.
5) Upon detecting positive edge of PA0, R6500/1 reads data on PB7-PB0. R6500/1 then sets PA2 high to indicate that the data has been taken.
6 When no more data is available, the host drops PA1 low to indicate end of data ($\overline{EOD}$). The R6500/1 then jumps to address $000 to start program execution. If all RAM is loaded without $\overline{EOD}$ detected, the R6500/1 also jumps to address $000.

An assembly listing of the RAM Program Loader is shown in Table 6-1.

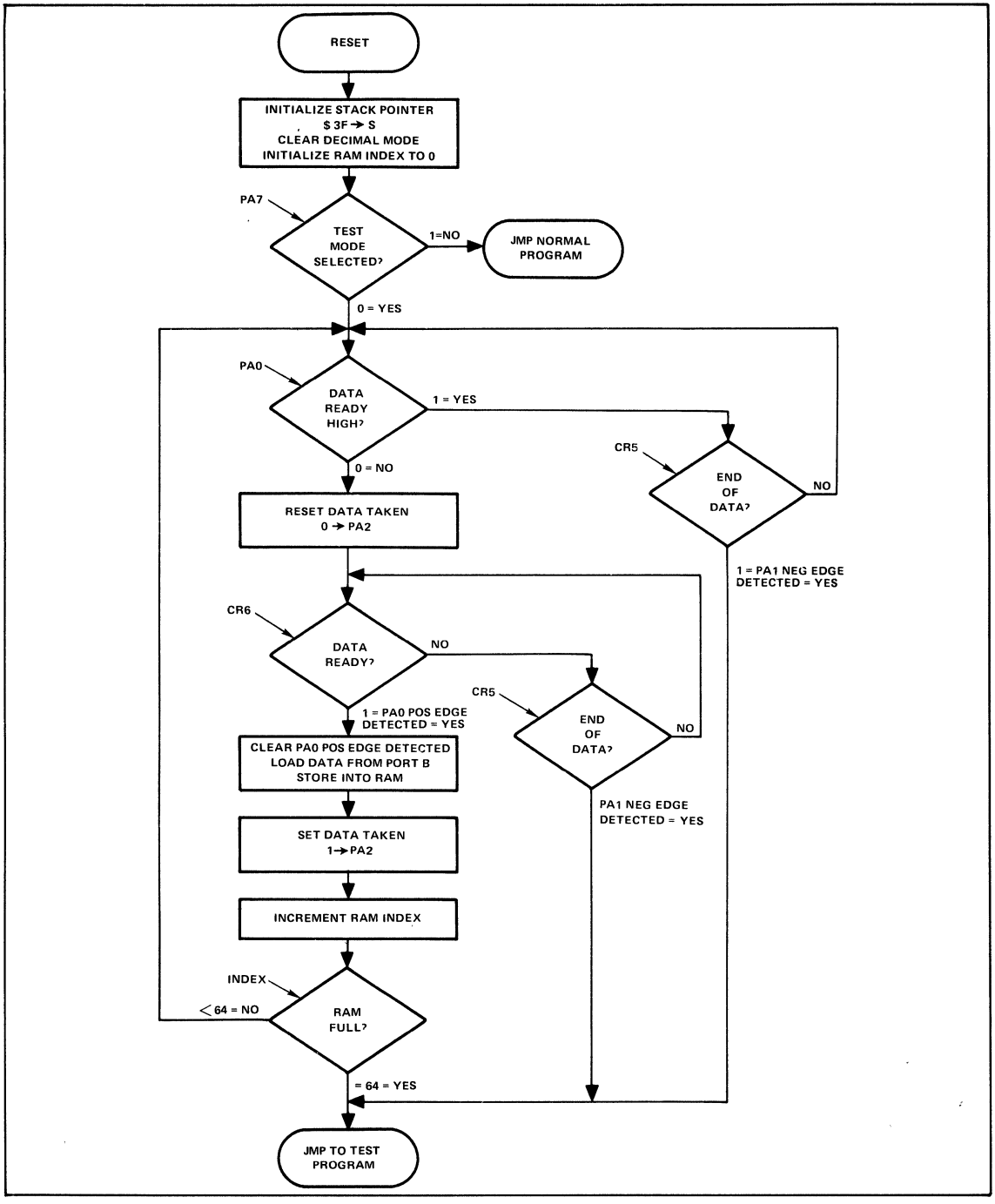


Figure 6-1. RAM Program Loader Flowchart

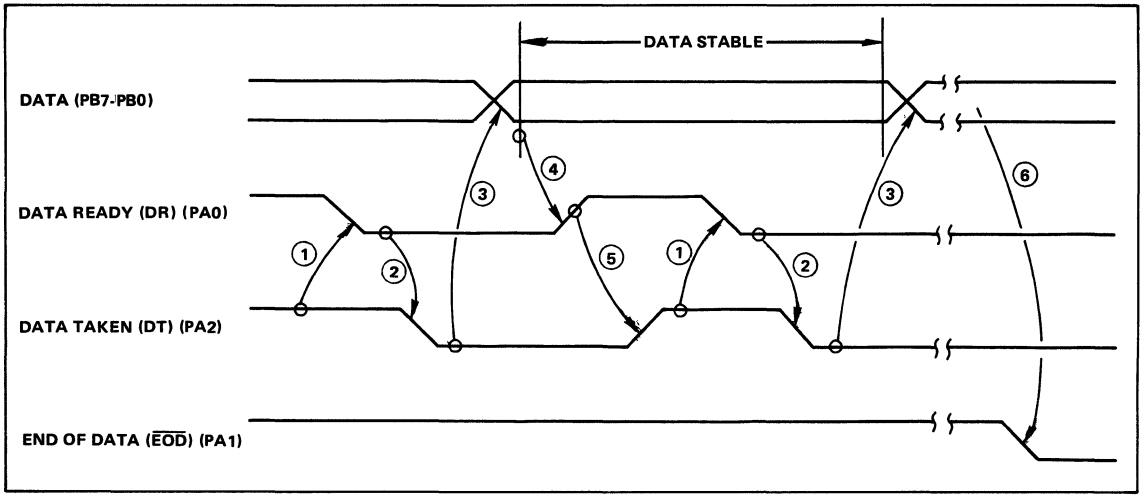


Figure 6-2. R6500/1 RAM Program Load Handshake

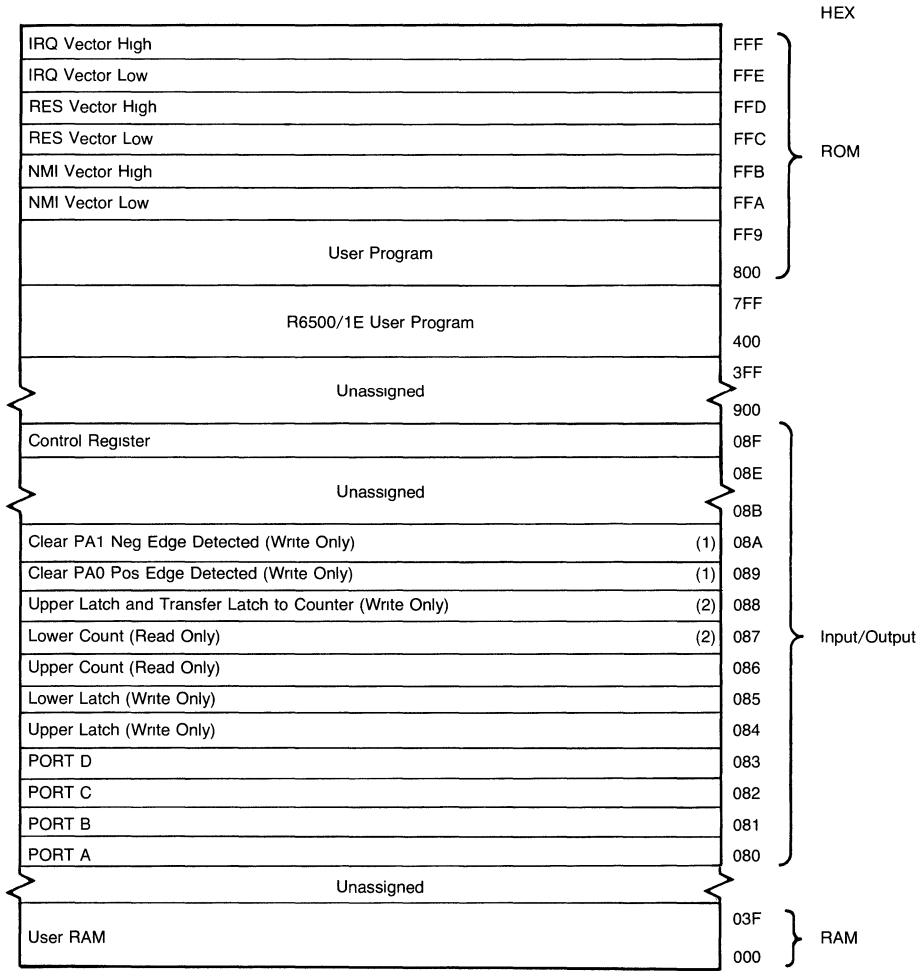
Table 6-1. RAM Program Loader Assembly Listing

R6500/1 RAM LOADER ..... PAGE 001

LINE #	LOC	CODE	LINE		
0002	0000		PORTB = $81		;Port B Address
0003	0000		PORTA = $80		;Port A Address
0004	0000		CLRPA0 = $89		;CLR PA0 Edge Detect
0005	0000		CTLREG = $8F		;Control Register
0006	0000		BEGIN = $000		;RAM First Address
0008	0000			*=$0800	
0009	0800	A2 3F	Reset	LDX #$3F	
0010	0802	9A		TXS	;Initialize Stack Pointer
0011	0803	D8		CLD	;Set Binary Add Mode
0012	0804	A2 00		LDX #$00	;Initialize RAM Index
0013	0806	A5 80		LDA PORTA	
0014	0808	30 2D		BMI INIT	;Test Mode Selected (PA7 = 0)?
0016	080A	A5 80	PAZCK	LDA PORTA	;Yes
0017	080C	4A		LSR A	
0018	080D	B0 1C		BCS EODCK1	;Data Ready High (PA0 = 1)?
0020	080F	A9 FB		LDA #$FB	;No, Reset Data Taken
0021	0811	B5 80		STA PORTA	;0->PA2
0023	0813	A9 20	RDYCK	LDA #$20	
0024	0815	24 8F		BIT CTLREG	
0025	0817	50 1A		BVC EODCK2	;Data Ready (PA0 Pos Edge Detected)?
0027	0819	85 89		STA CLRPA0	;Yes, Clear PA0 Pos Edge Detected
0028	081B	A5 81		LDA PORTB	;Load Data From Port B
0029	0081D	95 00		STA BEGIN,X	;Store in RAM
0030	081F	A9 FF		LDA #$FF	
0031	0821	85 80		STA PORTA	;Set Data Taken (1->PA2)
0032	0823	E8		INX	;Increment RAM Index
0033	0824	E0 40		CPX #$40	
0034	0826	D0 E2		BNE PAZCK	;Is RAM Full?
0036	0828	4C 00 00	JMPBEG	JMP BEGIN	;Yes, Go To RAM Program Execution
0038	082B	A9 20	EODCK1	LDA #$20	
0039	082D	25 8F		AND CTLREG	
0040	082F	F0 D9		BEQ PAZCK	;End of Data (PA1 Neg Edge Detected)?
0041	0831	D0 F5		BNE JMPBEG	;Yes, Go To RAM Program Execution
0043	0833	F0 DE	EODCK2	BEQ RDYCK	;End of Data (PA1 Neg Edge Detected)?
0044	0835	D0 F1		BNE JMPBEG	;Yes, Go To Ram Program Execution
0046	0837		INIT		;First Address of Normal Program
0048	0837			*=$FFC	
0049	OFFC	00 08	RES	.WOR RESET	;Reset Vector
0050	OFFE			.END	

Errors = 0000 <0000>
End of Assembly

APPENDIX A — SYSTEM MEMORY MAP



Notes:
(1) I/O command only; i.e , no stored data.
(2) Clears Counter Overflow — Bit 7 in Control Register.

APPENDIX B — R6500 INSTRUCTION SET

This appendix contains a summary of the R6500 instruction set. For detailed information, consult the R6500 Microcomputer System Programming Manual, Document Order No. 202.

B.1 INSTRUCTION SET IN ALPHABETIC SEQUENCE

ADC	Add Memory to Accumulator with Carry
AND	"AND" Memory with Accumulator
ASL	Shift Left One Bit (Memory or Accumulator)
BCC	Branch on Carry Clear
BCS	Branch On Carry Set
BEQ	Branch on Result Zero
BIT	Test Bits in Memory with Accumulator
BMI	Branch on Result Minus
BNE	Branch on Result not Zero
BPL	Branch on Result Plus
BRK	Force Break
BVC	Branch on Overflow Clear
BVS	Branch on Overflow Set
CLC	Clear Carry Flag
CLD	Clear Decimal Mode
CLI	Clear Interrupt Disable Bit
CLV	Clear Overflow Flag
CMP	Compare Memory and Accumulator
CPX	Compare Memory and Index X
CPY	Compare Memory and Index Y
DEC	Decrement Memory by One
DEX	Decrement Index X by One
DEY	Decrement Index Y by One
EOR	"Exclusive-Or" Memory with Accumulator
INC	Increment Memory by One
INX	Increment Index X by One
INY	Increment Index Y by One
JMP	Jump to New Location
JSR	Jump to New Location Saving Return Address
LDA	Load Accumulator with Memory
LDX	Load Index X with Memory
LDY	Load Index Y with Memory
LSR	Shift One Bit Right (Memory or Accumulator)
NOP	No Operation
ORA	"OR" Memory with Accumulator
PHA	Push Accumulator on Stack
PHP	Push Processor Status on Stack
PLA	Pull Accumulator from Stack
PLP	Pull Processor Status from Stack
ROL	Rotate One Bit Left (Memory or Accumulator)
ROR	Rotate One Bit Right (Memory or Accumulator)
RTI	Return from Interrupt
RTS	Return from Subroutine
SBC	Subtract Memory from Accumulator with Borrow
SEC	Set Carry Flag
SED	Set Decimal Mode
SEI	Set Interrupt Disable Status
STA	Store Accumulator in Memory
STX	Store Index X in Memory
STY	Store Index Y in Memory
TAX	Transfer Accumulator to Index X
TAY	Transfer Accumulator to Index Y
TSX	Transfer Stack Pointer to Index X
TXA	Transfer Index X to Accumulator
TXS	Transfer Index X to Stack Register
TYA	Transfer Index Y to Accumulator

B2. INSTRUCTION SET SUMMARY TABLE

INSTRUCTIONS		IMMEDIATE			ABSOLUTE			ZERO PAGE			ACCUM			IMPLIED			(IND, X)			(IND), Y			Z PAGE, X			ABS X			ABS, Y			RELATIVE			INDIRECT			Z PAGE, Y			PROCESSOR STATUS CODES	
MNEMONIC	OPERATION	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	7 6 5 4 3 2 1 0 N V • B D I Z C	MNEMONIC
ADC	A + M + C → A (4) (1)	69	2	2	6D	4	3	65	3	2							61	6	2	71	5	2	75	4	2	7D	4	3	79	4	3										N V • • • • Z C	ADC
AND	A∧M → A (1)	29	2	2	2D	4	3	25	3	2							21	6	2	31	5	2	35	4	2	3D	4	3	39	4	3										N • • • • • Z •	AND
ASL	C ← [7 6 5 4 3 2 1 0] ← 0				0E	6	3	06	5	2	0A	2	1										16	6	2	1E	7	3													N • • • • • Z C	ASL
BCC	BRANCH ON C = 0 (2)																															90	2	2								• • • • • • • •	BCC
BCS	BRANCH ON C = 1 (2)																															B0	2	2								• • • • • • • •	BCS
BEQ	BRANCH ON Z = 1 (2)																															F0	2	2								• • • • • • • •	BEQ
BIT	A∧M				2C	4	3	24	3	2																																M_7 M_6• • • • Z •	BIT
BMI	BRANCH ON N = 1 (2)																															30	2	2								• • • • • • • •	BMI
BNE	BRANCH ON Z = 0 (2)																															D0	2	2								• • • • • • • •	BNE
BPL	BRANCH ON N = 0 (2)																															10	2	2								• • • • • • • •	BPL
BRK	BREAK													00	7	1																										• • • 1 • 1 • •	BRK
BVC	BRANCH ON V = 0 (2)																															50	2	2								• • • • • • • •	BVC
BVS	BRANCH ON V = 1 (2)																															70	2	2								• • • • • • • •	BVS
CLC	0 → C													18	2	1																										• • • • • • • 0	CLC
CLD	0 → D													D8	2	1																										• • • • 0 • • •	CLD
CLI	0 → I													58	2	1																										• • • • • 0 • •	CLI
CLV	0 → V													B8	2	1																										• 0 • • • • •	CLV
CMP	A − M	C9	2	2	CD	4	3	C5	3	2							C1	6	2	D1	5	2	D5	4	2	DD	4	3	D9	4	3										N • • • • • Z C	CMP
CPX	X − M	E0	2	2	EC	4	3	E4	3	2																																N • • • • • Z C	CPX
CPY	Y − M	C0	2	2	CC	4	3	C4	3	2																																N • • • • • Z C	CPY
DEC	M − 1 → M				CE	6	3	C6	5	2													D6	6	2	DE	7	3													N • • • • • Z •	DEC
DEX	X − 1 → X													CA	2	1																										N • • • • • Z •	DEX
DEY	Y − 1 → Y													88	2	1																										N • • • • • Z •	DEY
EOR	A ∀ M → A (1)	49	2	2	4D	4	3	45	3	2							41	6	2	51	5	2	55	4	2	5D	4	3	59	4	3										N • • • • • Z •	EOR
INC	M + 1 → M				EE	6	3	E6	5	2													F6	6	2	FE	7	3													N • • • • • Z •	INC
INX	X + 1 → X													E8	2	1																										N • • • • • Z •	INX
INY	Y + 1 → Y													C8	2	1																										N • • • • • Z •	INY
JMP	JUMP TO NEW LOC				4C	3	3																												6C	5	3				• • • • • • • •	JMP
JSR	JUMP SUB				20	6	3																																			• • • • • • • •	JSR
LDA	M → A (1)	A9	2	2	AD	4	3	A5	3	2							A1	6	2	B1	5	2	B5	4	2	BD	4	3	B9	4	3										N • • • • • Z •	LDA
LDX	M → X (1)	A2	2	2	AE	4	3	A6	3	2																			BE	4	3							B6	4	2	N • • • • • Z •	LDX
LDY	M → Y (1)	A0	2	2	AC	4	3	A4	3	2													B4	4	2	BC	4	3													N • • • • • Z •	LDY
LSR	0 → [7 6 5 4 3 2 1 0] → C				4E	6	3	46	5	2	4A	2	1										56	6	2	5E	7	3													0 • • • • • Z C	LSR
NOP	NO OPERATION													EA	2	1																										• • • • • • • •	NOP
ORA	A ∨ M → A	09	2	2	0D	4	3	05	3	2							01	6	2	11	5	2	15	4	2	1D	4	3	19	4	3										N • • • • • Z •	ORA
PHA	A → Ms S − 1 → S													48	3	1																										• • • • • • • •	PHA
PHP	P → Ms S − 1 → S													08	3	1																										• • • • • • • •	PHP
PLA	S + 1 → S Ms → A													68	4	1																										N • • • • • Z •	PLA
PLP	S + 1 → S Ms → P													28	4	1																										(RESTORED)	PLP
ROL	[C 7 6 5 4 3 2 1 0] ←				2E	6	3	26	5	2	2A	2	1										36	6	2	3E	7	3													N • • • • • Z C	ROL
ROR	→ [C 7 6 5 4 3 2 1 0]				6E	6	3	66	5	2	6A	2	1										76	6	2	7E	7	3													N • • • • • Z C	ROR
RTI	RTRN INT													40	6	1																										(RESTORED)	RTI
RTS	RTRN SUB													60	6	1																										• • • • • • • •	RTS
SBC	A − M − $\overline{C}$ → A (1)	E9	2	2	ED	4	3	E5	3	2							E1	6	2	F1	5	2	F5	4	2	FD	4	3	F9	4	3										N V • • • • Z (3)	SBC
SEC	1 → C													38	2	1																										• • • • • • • 1	SEC
SED	1 → D													F8	2	1																										• • • • 1 • • •	SED
SEI	1 → I													78	2	1																										• • • • • 1 • •	SEI
STA	A → M				8D	4	3	85	3	2							81	6	2	91	6	2	95	4	2	9D	5	3	99	5	3										• • • • • • • •	STA
STX	X → M				8E	4	3	86	3	2																														96	4	2	• • • • • • • •	STX
STY	Y → M				8C	4	3	84	3	2													94	4	2																		• • • • • • • •	STY
TAX	A → X													AA	2	1																										N • • • • • Z •	TAX
TAY	A → Y													A8	2	1																										N • • • • • Z •	TAY
TSX	S → X													BA	2	1																										N • • • • • Z •	TSX
TXA	X → A													8A	2	1																										N • • • • • Z •	TXA
TXS	X → S													9A	2	1																										• • • • • • • •	TXS
TYA	Y → A													98	2	1																										N • • • • • Z •	TYA

(1) ADD 1 to N IF PAGE BOUNDARY IS CROSSED

(2) ADD 1 TO N IF BRANCH OCCURS TO SAME PAGE
ADD 2 TO N IF BRANCH OCCURS TO DIFFERENT PAGE

(3) CARRY NOT = BORROW

(4) IF IN DECIMAL MODE Z FLAG IS INVALID
ACCUMULATOR MUST BE CHECKED FOR ZERO RESULT

X	INDEX X	+	ADD
Y	INDEX Y	−	SUBTRACT
A	ACCUMULATOR	∧	AND
M	MEMORY PER EFFECTIVE ADDRESS	∨	OR
Ms	MEMORY PER STACK POINTER	∀	EXCLUSIVE OR
M_7	MEMORY BIT 7		
M_6	MEMORY BIT 6		
n	NO CYCLES		
#	NO BYTES		

3

APPENDIX C — SYSTEM SPECIFICATIONS

MAXIMUM RATINGS*

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}, V_{RR}	−0.3 to +7.0	Vdc
Input Voltage	V_{IN}	−0.3 to +7.0	Vdc
Operating Temperature Commercial Industrial	T_A	T_L to T_H 0 to +70 −40 to +150	°C
Storage Temperature	T_{STG}	−55 to +150	°C

***NOTE:** Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in other sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

(V_{CC} = 5.0V ±5%, V_{RR} = V_{CC}; V_{SS} = 0V; T_A = 0° to 70°C, unless otherwise specified)

Parameter	Symbol	Min	Typ[1]	Max	Unit	Test Conditions
RAM Standby Voltage (Retention Mode)	V_{RR}	3.0		V_{CC}	V	
RAM Standby Current (Retention Mode) Commercial Industrial	I_{RR}	 — —	 10 12	 — —	mA	
Input High Voltage All Except XTLI XTLI	V_{IH}	 +2.0 +4.0	 — —	 V_{CC} V_{CC}	V	
Input Low Voltage	V_{IL}	−0.3	—	+0.8	V	
Input Leakage Current $\overline{RES}$, $\overline{NMI}$	I_{IN}	—	±1.0	±2.5	μA	V_{IN} = 0 to 5.0V
Input Low Current	I_{IL}	—	−1.0	−1.6	mA	V_{IL} = 0.4V
Output High Voltage	V_{OH}	+2.4	—	—	V	I_{LOAD} = −100 μA V_{CC} = 4.75V
Output High Voltage (CMOS)	V_{CMOS}	V_{CC} = 30%	—	—	V	V_{CC} = 4.75V
Output Low Voltage	V_{OL}	—	—	+0.4	V	I_{LOAD} = 1.6 mA
I/O Port Pull-Up Resistance PA0–PA7, PB0–PB7, PC0–PC7, PD0–PD7, CNTR	R_L	3.0	6.0	11.5	Kohm	
Output High Current (Sourcing)	I_{OH}	−100	—	—	μA	V_{OUT} = 2.4V
Output Low Current (Sinking)	I_{OL}	1.6	—	—	mA	V_{OUT} = 0.4V
Input Capacitance XTLI, XTLO PA, PB, PC, PD, CNTR	C_{IN}	 — —	 — —	 50 10	pF	T_A = 25°C V_{IN} = 0V f = 1.0 MHz
Output Capacitance (Three-State Off)	C_{OUT}	—	—	10	pF	T_A = 25°C V_{IN} = 0V f = 1.0 MHz
Power Dissipation (Outputs High)	P_D	—	750	1100	mW	T_A = 0°C

Notes:
1. Typical values measured at T_A = 25°C and V_{CC} = 5.0V.
2. Negative sign indicates outward current flow, positive indicates inward flow.

AC CHARACTERISTICS

(V_{CC} = 5V ±10% for R6500/1, V_{CC} = 5V ±% for R6500/1A)

Parameter	Symbol	1 MHz		2 MHz		Unit
		Min	Max	Min	Max	
XTLI Input Clock Cycle Time	T_{cyc}	0.500	5.0	0.250	5.0	µsec
Internal Write to Peripheral Data Valid (TTL)	T_{PDW}	1.0		0.5		µsec
Internal Write to Peripheral Data Valid (CMOS)	T_{CMOS}	2.0		1.0		µsec
Peripheral Data Setup Time	T_{PDSU}	400		200		nsec
Count and Edge Detect Pulse Width	T_{PW}	1.0		0.5		µsec

APPENDIX D — R6500/1E EMULATOR PART

D.1 INTRODUCTION

To aid the user in designing R6500/1 microcomputer systems, Rockwell has developed an R6500/1E Emulator. The basic architecture of the Emulator is the same as that of the R6500/1 single-chip microcomputer except the Emulator brings the address, data, and required control lines off the chip to an external memory.

This appendix describes only the differences between the R6500/1 single-chip microcomputer and the R6500/1E Emulator. All sections of the Emulator not described in this appendix are identical to the corresponding section of the R6500/1 single chip microcomputer.

D.2 R6500/1 EMULATOR INTERFACE REQUIREMENTS

This section describes the interface requirements for the R6500/1E Emulator. Figure D-1 is the Emulator Interface diagram. Figure D-2 shows the Emulator pin configuration. Table D-1 describes the function of each pin of the Emulator that differs from the R6500/1 device.

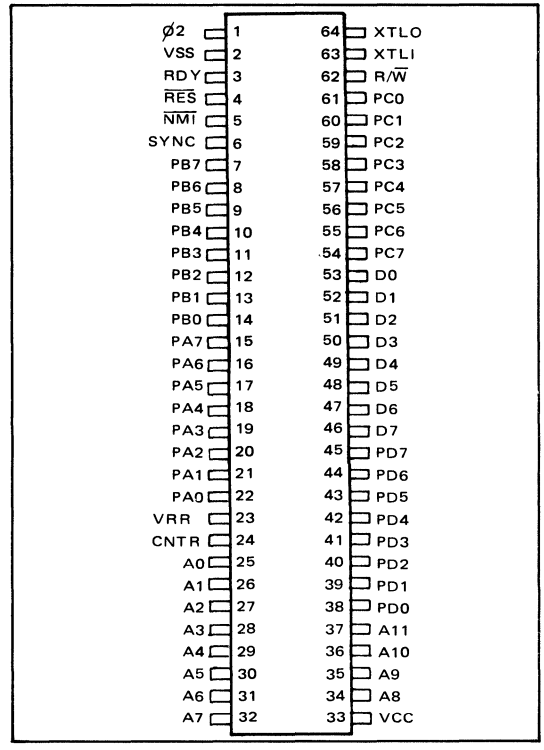


Figure D-2. Emulator Pin Configuration

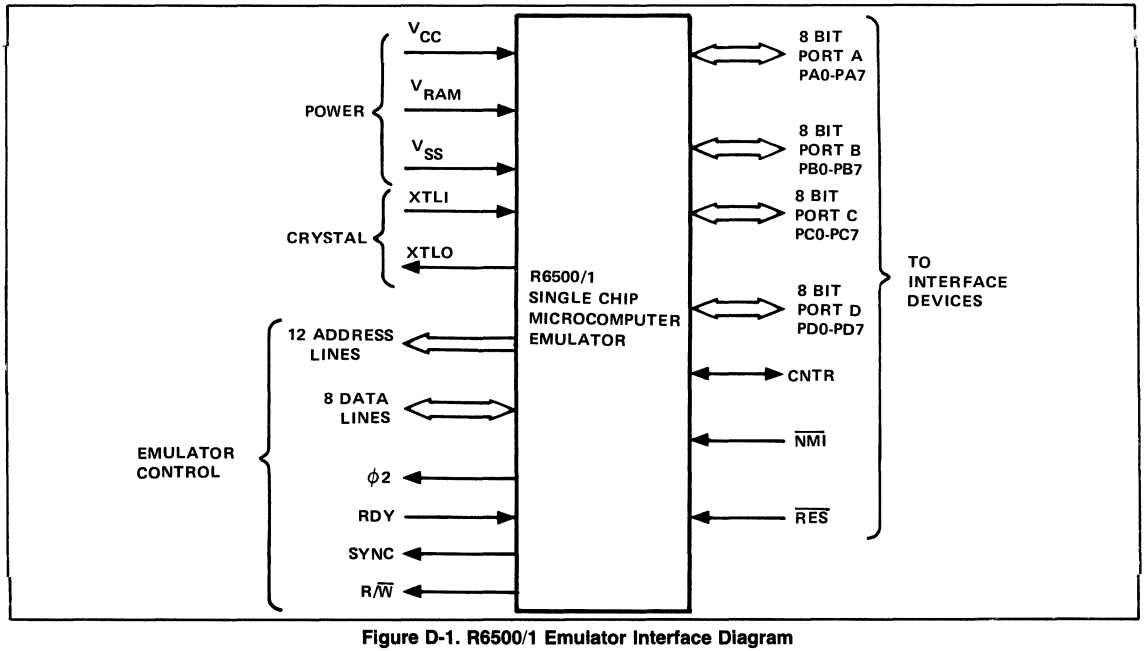


Figure D-1. R6500/1 Emulator Interface Diagram

Table D-1. R6500/1E Emulator Pin Description

Signal Name	Pin No.	Description
R/W	62	Read/Write allows the CPU to control the direction of data transfers between the R6500/1E Emulator CPU and external memory. This line is high when reading data from memory and is low when writing data to memory.
RDY	3	The Ready input delays execution of any cycle during which the RDY line is low. This allows the user to halt or single step the CPU on all cycles except write cycles. A negative transition to the low state during the Ø2 clock low pulse will halt the CPU with the address lines containing the current address being fetched. If RDY is low during a write cycle, it is ignored until the following read operation. This condition will remain through a subsequent Ø2 clock pulse in which the RDY line is low. This feature allows the CPU to interface with memories having slow access times, such as EPROMS used with the R6500/1 Emulator part during prototype system development.
SYNC	6	The Sync signal is provided to identify cycles in which the CPU is performing OP CODE fetch. SYNC goes high during the Ø2 clock low pulse of an OP CODE fetch and stays high for the remainder of that cycle. If the RDY line is pulled low during the Ø2 clock low pulse in which SYNC went high, the CPU will halt in its current state and will remain in that state until the RDY line goes high. Using this technique, the SYNC signal can be used to control RDY to cause single instruction execution.
Ø2	1	Phase 2 (Ø2) clock pulse. Data transfer takes place only during Ø2 clock pulse high.
A0-A11	25-37	Address Bus lines. The address bus buffers on the R6500/1E are push/pull type drivers capable of driving at least 130 pf and one standard TTL load. The address bus always contains known data. The addressing technique involves putting an address on the address bus which is known to be either in program sequence, on the same page in program memory, or at a known point in memory. The I/O address commands are also placed on these lines.
D0-D7	53-46	Data Bus lines. All transfers of instructions and data between the CPU and memory, I/O, and other interfacing circuitry take place on the data bus lines. The buffers driving the data bus lines have full three-state capability, which is necessitated by the fact that the lines are bidirectional. Each data bus pin is connected to an input and output buffer, with the output buffer remaining in the floating condition.

3

D.3 SYSTEM ARCHITECTURE

Figure D-3 is a block diagram of the R6500/1E Emulator. The function of each block is identical to its counterpart in the R6500/1 microcomputer. The main differences between the two products are in the ROM, the clock oscillator, the input/output ports and write-only monitoring.

D.3.1 ROM

To facilitate debugging, the R6500/1 ROM has been removed from the R6500/1E Emulator, and has been replaced by external memory. Also, an additional 1024 bytes of memory (400-7FF) are addressable.

D.3.2 CLOCK OSCILLATOR

The external frequency reference for the R6500/1E Emulator may be either a crystal or a clock. The RC option is not available for this device.

D.3.3 INPUT/OUTPUT PORTS

The R6500/1E has the internal I/O and CNTR port pull-up resistance only. The option to delete the pull-up resistance is not included in this device.

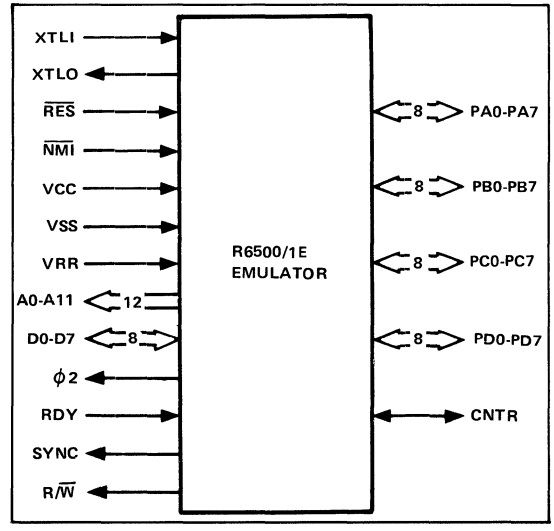


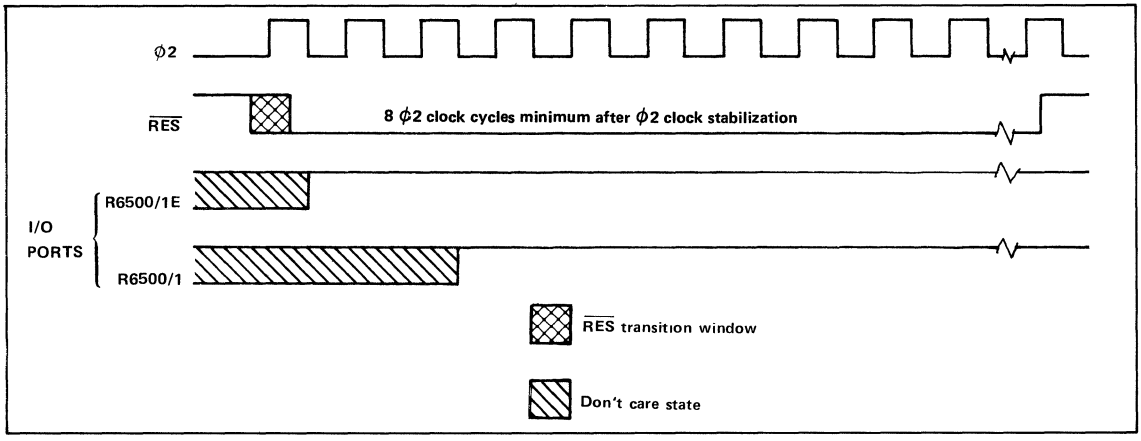
Figure D-3. R6500/1E Emulator Block Diagram

D.3.4 WRITE-ONLY MONITORING

The R6500/1E allows the user to monitor write operations to the internal RAM and I/O by routing those operations externally as well as internally. Read operations are not routed externally.

D.4 R6500/1E I/O PORT INITIALIZATION

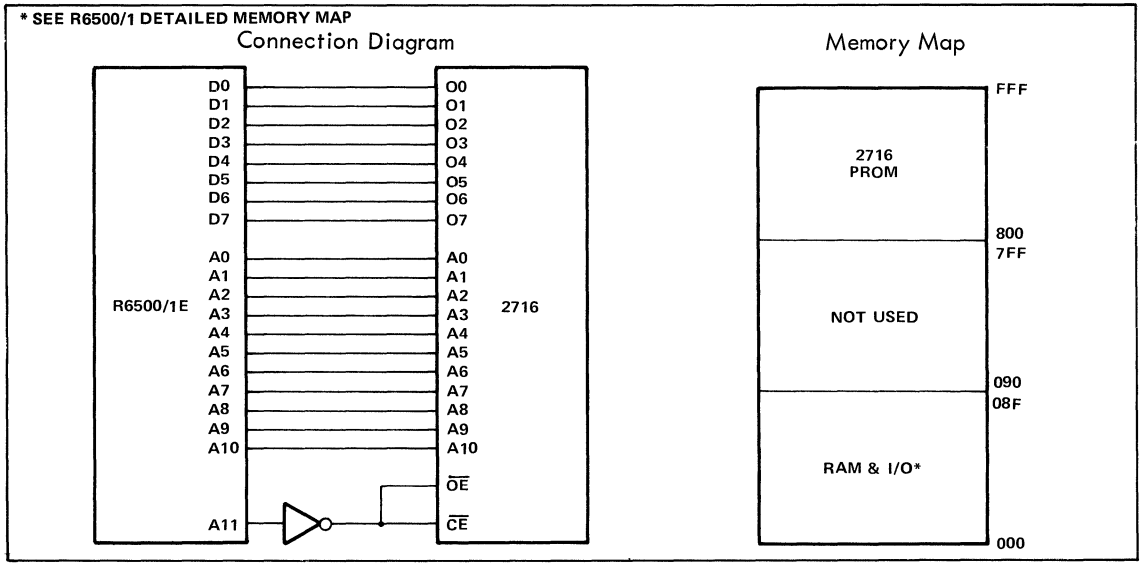
Ports A, B, C and D and the CNTR line in R6500/1E are initialized to the logic high state two Ø2 clock cycles earlier than in the R6500/1. It is still required, however, that the $\overline{RES}$ line to the R6500/1E be held low for at least eight Ø2 clock cycles after VCC reaches operating range and the Ø2 clock oscillator has stabilized.



D.5 TYPICAL R6500/1E PROGRAM MEMORY INTERCONNECTIONS

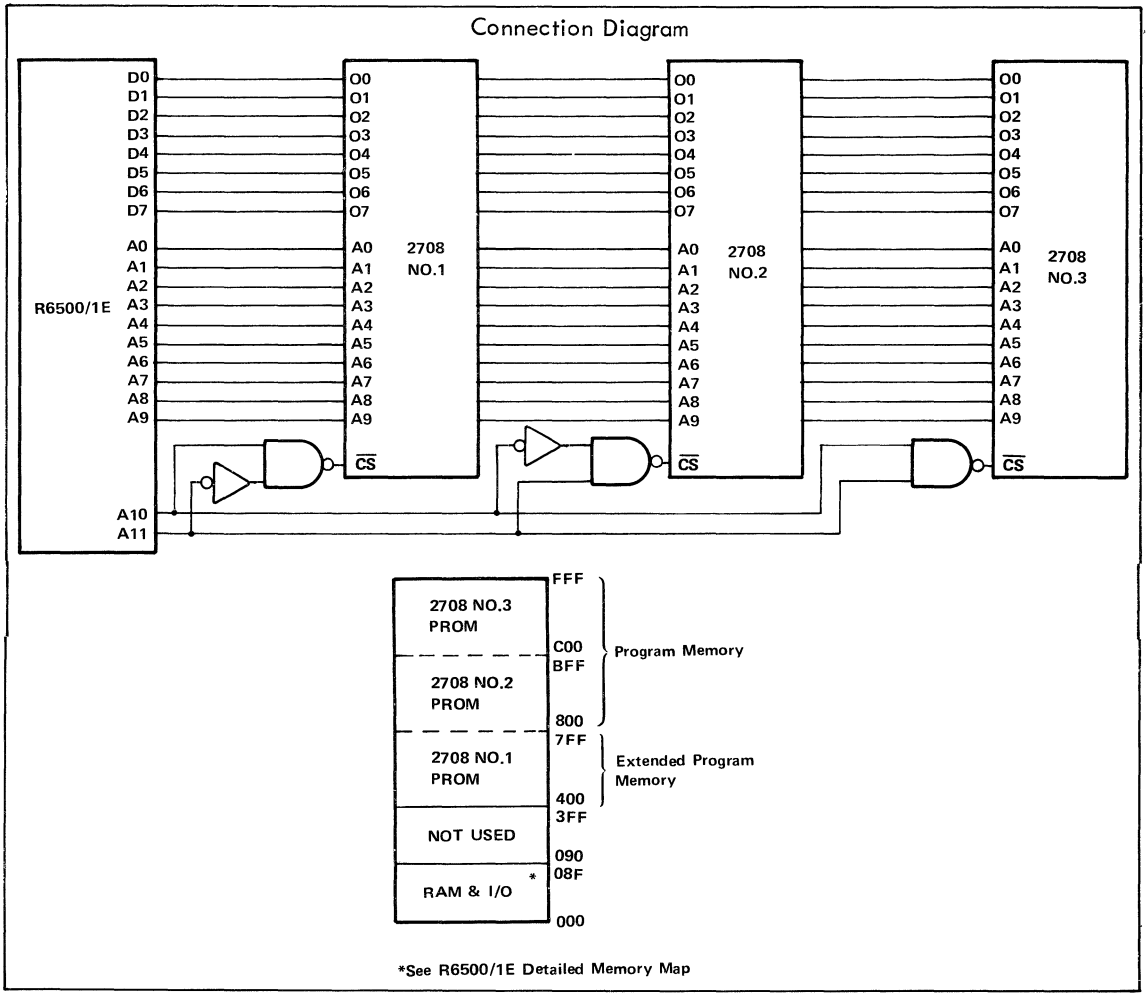
Shown below and on the following page are two typical connections between the R6500/1E and program memory (in this case, type 2716 and 2708 PROMs). Example 1 shows a connection to a 2K 2716 PROM. Since the R6500/1 has a 2K ROM capacity, the contents of the PROM could be masked directly into the production R6500/1 ROM.

Example 1. R6500/1E Connected to One 2716 PROM (2K Bytes)



Example 2 shows a connection to 3K of 2708 PROMs. The extra 1K PROM allows expanded or additional programs be used during R6500/1 firmware development. The production program, however, must be reduced to 2K maximum (between addresses 800 and FFF) before committing to R6500/1 ROM.

Example 2. R6500/1E Connected to Three PROMs (3K Bytes)



Truth Table

Address		PROM Select			Selected Address Range
A11	A10	2708 No. 1 CE	2708 No. 2 CE	2808 No. 3 CE	
0	0	1	1	1	000-3FF
0	1	0	1	1	400-7FF
1	0	1	0	1	800-BFF
1	1	1	1	0	C00-FFF

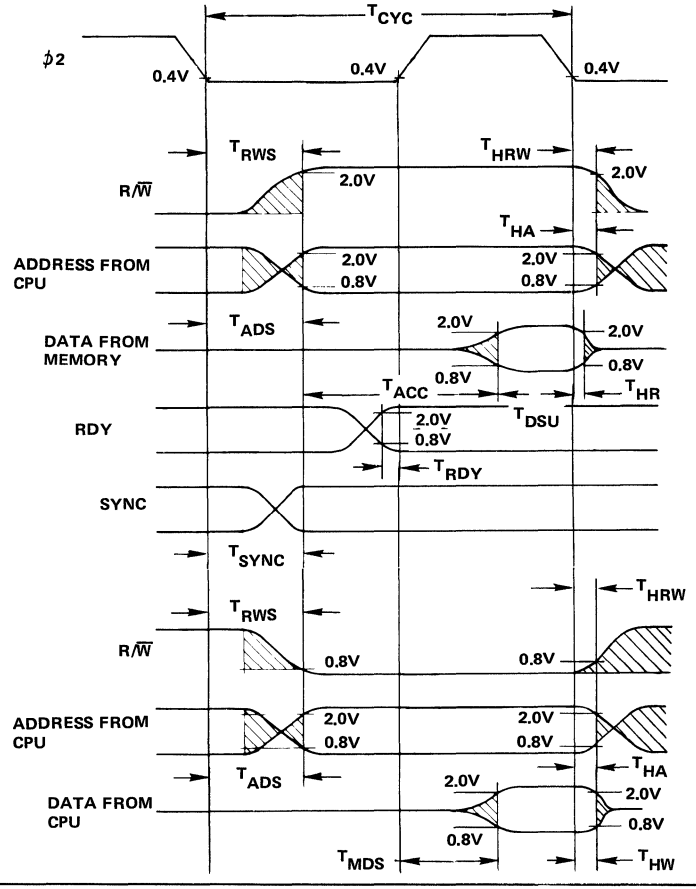
D.6 R6500/1E TIMING

Signal	Symbol	1 MHz		2 MHz		Unit
		Min.	Max.	Min.	Max.	
R/$\overline{W}$ setup time from CPU	T_{RWS}		300		200	ns
Address setup time from CPU	T_{ADS}		300		200	ns
Memory read access time	T_{ACC}		525		225	ns
Data stabilization time	T_{DSU}	150		75		ns
Data hold time — Read	T_{HR}	10		10		ns
Data hold time — Write	T_{HW}	30		30		ns
Data delay time from CPU	T_{MDS}		200		150	ns
RDY setup time	T_{RDY}	100		50		ns
SYNC delay time from CPU	T_{SYNC}		350		175	ns
Address hold time	T_{HA}	30		30		ns
R/$\overline{W}$ hold time	T_{HRW}	30		30		ns
Cycle Time	T_{CYC}	1.0	10.0	0.5	10.0	µs

PHASE 2 (ϕ2) TIMING REFERENCE

TIMING FOR READING DATA FROM EXTERNAL MEMORY

TIMING FOR WRITING DATA TO EXTERNAL MEMORY



D.7 R6500/1E DC CHARACTERISTICS

(V_{CC} = 5.0V ±5%, V_{SS} = 0V; T_A = 0° to 70°C, unless otherwise specified)

Parameter	Symbol	Min	Typ[1]	Max	Unit	Test Conditions
Input High Voltage D0–D7, RDY	V_{IH}	V_{SS} +2.4	—	—	V	
Input Low Voltage D0–D7, RDY	V_{IL}	—	—	V_{SS} +0.8	V	
Input Leakage Current (Three-State Off) D0–D7	I_{IN}	—	—	±10.0	μA	V_{IN} = 0 to 5.0V V_{CC} = 5.25V
Output High Voltage D0–D7, SYNC, A0–A11, R/$\overline{W}$, Ø2	V_{OH}	V_{SS} +2.4	—	—	V	I_{LOAD} = −100 μA V_{CC} = 4.75V
Output Low Voltage D0–D7, SYNC, A0–A11, R/$\overline{W}$, Ø2	V_{OL}	—	—	V_{SS} +0.6	V	I_{LOAD} = 1.6 mA V_{CC} = 4.75V
I/O Port Pull-Up Resistance	R_L	3.0	6.0	11.5	Kohm	
Input Capacitance RDY D0–D7	C_{IN}	— —	— —	10 15	pF	T_A = 25°C V_{IN} = 0V f = 1.0 MHz
Output Capacitance A0–A11, R/$\overline{W}$, SYNC Ø2	C_{OUT}	— —	— 50	12 80	pF	T_A = 25°C V_{IN} = 0V f = 1.0 MHz
Power Dissipation (Outputs High)	P_D	—	750	1200	mW	T_A = 0°C

Notes:
1. Typical values measured at T_A = 25°C and V_{CC} = 5.0V.
2. Negative sign indicates outward current flow, positive indicates inward flow.

Rockwell

R6500/1E
MICROPROCESSOR EMULATOR DEVICE

INTRODUCTION

The R6500/1EC and R6500/1EQ devices provide all the features of the R6500/1 Microcomputer in a ROMless form suitable for use as an advanced microprocessor complete with 16 bit counter and 32 I/O lines, and an address and data bus for 4K of external memory.

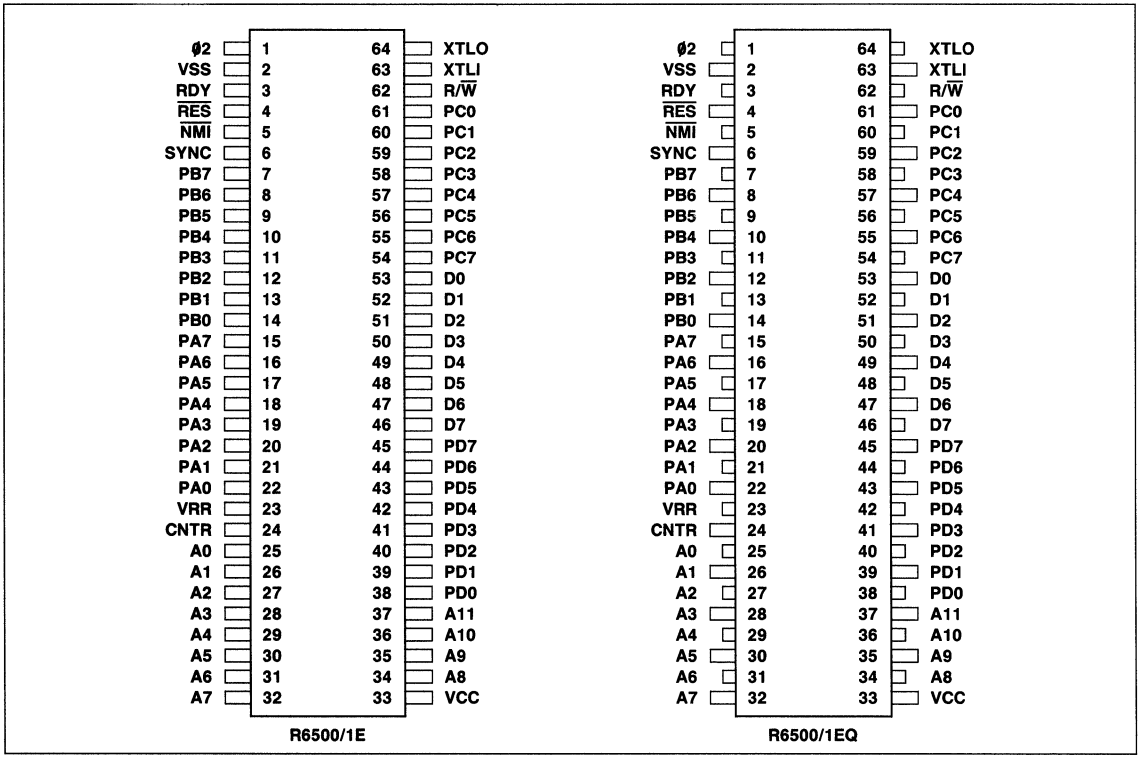
To aid in designing R6500/1 microcomputer systems, it may also be used as an Emulator device. Device architecture is basically the same as the R6500/1 except that the address, data, and associated control lines are routed off the chip for connection to an external memory.

The functions and operation of the devices are identical to the R6500/1 except for minor differences. The R6500/1 Data Sheet Order No. D51 (Document No. 2900D51) contains a description of R6500/1 and R6500/1 common interface signals and functions.

The device is available in both 64-pin DIP ceramic (R6500/1EC) and 64-pin QUIP Plastic (R6500/1EQ).

ORDERING INFORMATION

Part Number	Package Type	Frequency Option	Temperature Range
R6500/1EC	Ceramic	1 MHz	0°C to 70°C
R6500/1EAC	Ceramic	2 MHz	0°C to 70°C
R6500/1EQ	Plastic	1 MHz	0°C to 70°C
R6500/1EAQ	Plastic	2 MHz	0°C to 70°C



Pin Configuration

SIGNAL DESCRIPTIONS

All R6500/1 interface signals are provided in the device. While the pin assignments are different from the R6500/1 in order to accommodate the 64-pin package, the interface electrical characteristics are identical. The device provides 24 additional signals to route the address bus (12 lines), the data bus (8 lines), and control signals (4 lines) off the chip for connection to external memory.

MEMORY MAP

An additional 1024 bytes of memory (400-7FF) are addressable in the device.

EXTERNAL FREQUENCY REFERENCE

The external frequency reference may be a crystal or a clock — the RC option is not available in the device.

I/O PORT PULLUPS

The device has internal I/O port pullup resistance only.

DEVICE ADDITIONAL SIGNALS

Signal Name	Pin No.	Description
R/$\overline{W}$	62	Read/Write. The Read/Write output controls the direction of data transfer between the CPU and external memory. This line is high when reading data from memory and low when writing data to memory.
RDY	3	Ready. The Ready input delays execution of any cycle during which the RDY line is low. This allows the user to halt or single step the CPU on any cycle except a write cycle. A negative transition to the low state during the Φ2 clock low pulse will halt the CPU with the address lines containing the current address being fetched. If RDY is low during a write cycle, it is ignored until the following read operation. This condition will remain through a subsequent Φ2 clock pulse in which the RDY line is low.
SYNC	6	Sync. The Sync signal is provided to identify those cycles in which the CPU is performing an OP CODE fetch. SYNC goes high during Φ2 clock-low pulse during an OP CODE fetch and stay high for the remainder of that cycle. If the RDY line is pulled low during the Φ2 clock low pulse in which SYNC went high, the CPU will halt in its current state and will remain in that state until the RDY line goes high. Using this technique, the SYNC signal can be used to control RDY to cause single instruction execution.
Φ2	1	Phase 2 (Φ2) clock pulse. Data transfer can take place only during Φ2 clock pulse.
A0-A11	25-32 34-37	Address Bus Lines. The address bus buffers on the device are push/pull type drivers capable of driving at least 130 pf and one standard TTL load. The address bus always contains known data. The addressing technique involves putting an address on the address bus which is known to be either in program sequence, on the same page in program memory, or at a known point in memory. The I/O addresses are also placed on these lines.
D0-D7	53-46	Data bus Lines. All transfers of instructions and data between the CPU and external memory take place on the data bus lines. The buffers driving the data bus lines have full three-state capability. Each data bus pin is connected to an input and an output buffer, with the output buffer remaining in the floating condition.

I/O PORT INITIALIZATION

Ports A, B, C and D and the CNTR line in the device are initialized to the logic high state two Φ2 clock cycles earlier than in the R6500/1. It is still required, however, that the $\overline{RES}$ line be held low for at least eight Φ2 clock cycles after V_{CC} reaches operating range (Figure 1).

TYPICAL PROGRAM MEMORY INTERCONNECTIONS

Illustrated are two typical connections between the R6500/1E and program memory (in this case, type 2716 and 2708 PROMS). Figure 2 shows a connection to a 2K 2716 PROM. Since the R6500/1 has a 2K ROM capacity, the contents of the PROM could be masked directly into the production R6500/1 ROM.

Figure 3 shows a connection to 3K of 2708 PROMS. The extra 1K PROM allows expanded or additional programs be used during R6500/1 firmware development. The production program, however, must be reduced to 2K maximum (between addresses 800 and FFF) before committing to R6500/1 ROM.

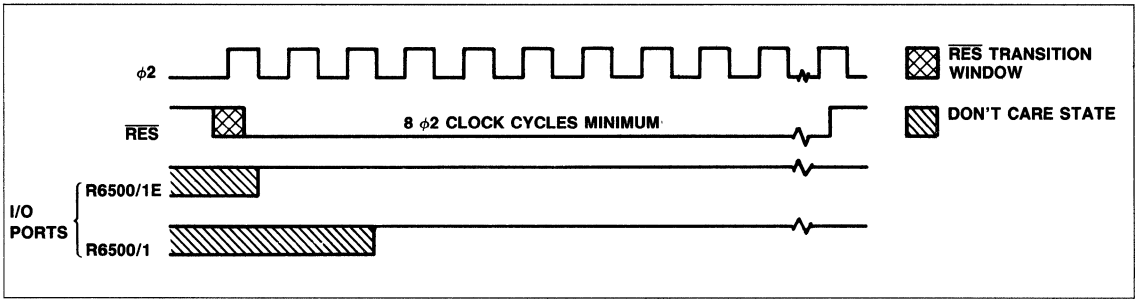


Figure 1. I/O Port Initialization

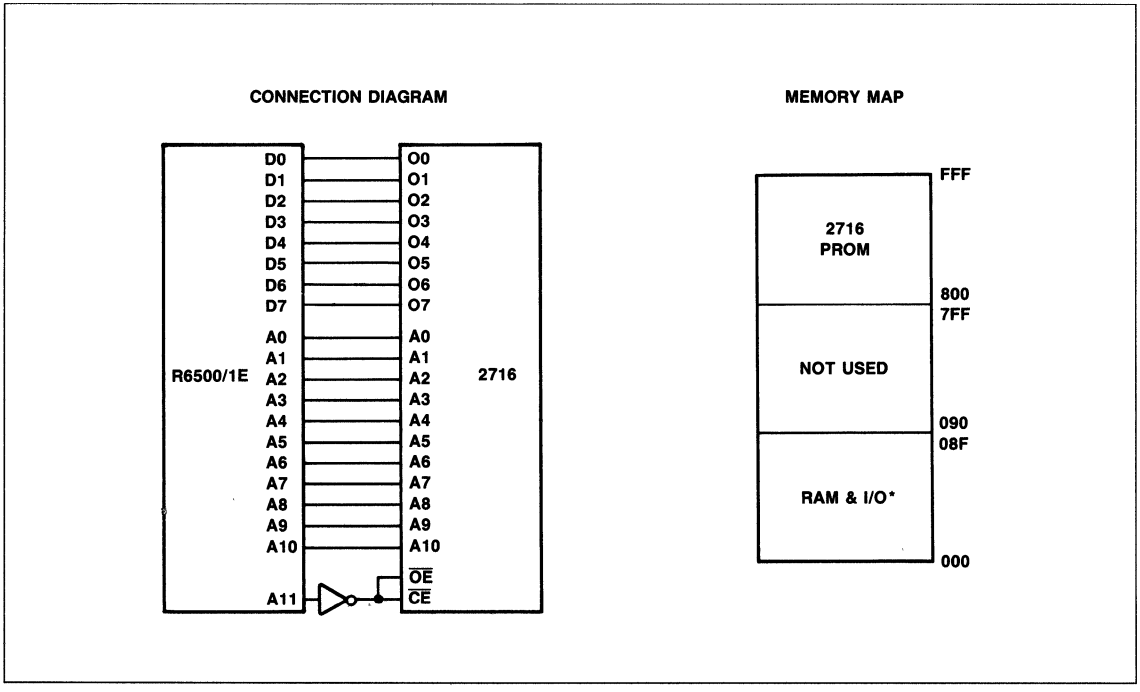


Figure 2. Device Connected to One 2716 PROM (2K Bytes)

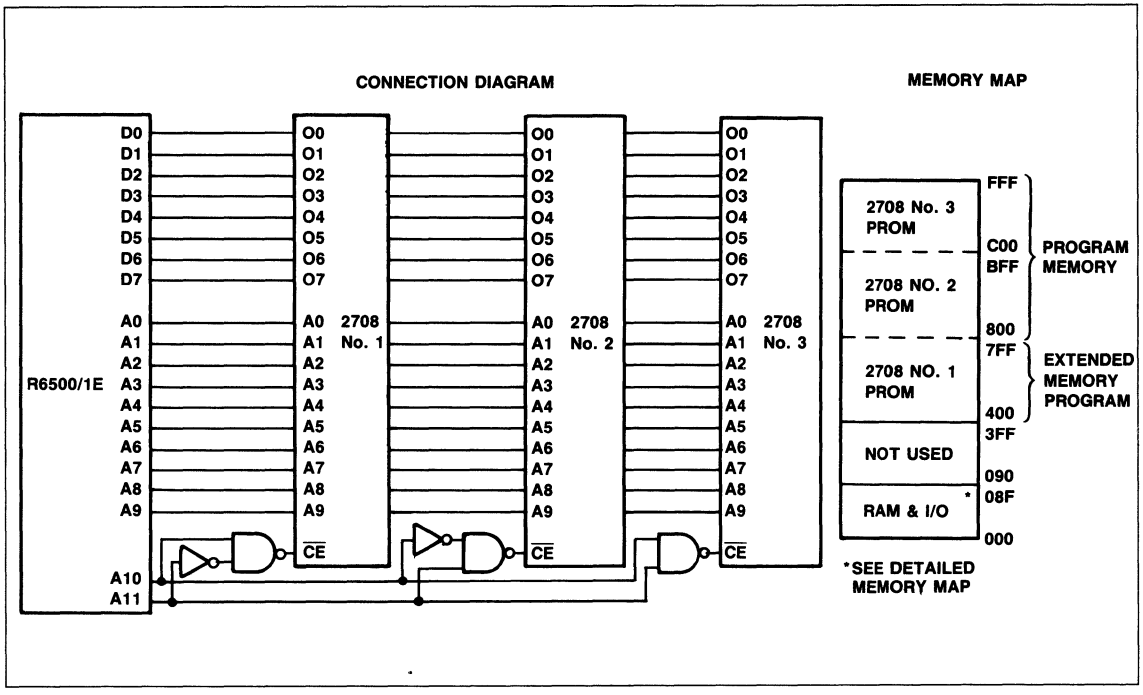


Figure 3. Device Connected to Three PROMS (3K Bytes)

TRUTH TABLE

Address		PROM Select			
A11	A10	2708 No. 3 $\overline{CE}$	2708 No. 2 $\overline{CE}$	2808 No. 1 $\overline{CE}$	Selected Address Range
0	0	1	1	1	000-3FF
0	1	1	1	0	400-7FF
1	0	1	0	1	800-BFF
1	1	0	1	1	C00-FFF

DEVICE TIMING

Signal	Symbol	1 MHz		2 MHz		Unit
		Min.	Max.	Min.	Max.	
R/$\overline{W}$ setup time from CPU	T_{RWS}		300		200	ns
Address setup time from CPU	T_{ADS}		300		200	ns
Memory read access time	T_{ACC}		525		225	ns
Data stabilization time	T_{DSU}	150		75		ns
Data hold time — Read	T_{HR}	10		10		ns
Data hold time — Write	T_{HW}	30		30		ns
Data delay time from CPU	T_{MDS}		200		150	ns
RDY setup time	T_{RDY}	100		50		ns
SYNC delay time from CPU	T_{SYNC}		350		175	ns
Address hold time	T_{HA}	30		30		ns
R/$\overline{W}$ hold time	T_{HRW}	30		30		ns
Cycle Time	T_{CYC}	1.0	10.0	0.5	10.0	μs

ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0 ±5%, V_{SS} = 0, T_A = 25°C)

Characteristic	Symbol	Min	Typ	Max	Unit
Input High Threshold Voltage D0-D7, RDY,	V_{IHT}	V_{SS} + 2 4	—	—	Vdc
Input Low Threshold Voltage D0-D7, RDY,	V_{ILT}	—	—	V_{SS} + 0.8	Vdc
Three-State (Off State) Input Current (V = 0 4 to 2 4V, V_{CC} = 5.25V) D0-D7	I_{TSI}	—	—	10	μA
Output High Voltage (I_{LOAD} = 100μAdc, V_{CC} = 4.75V) D0-D7, SYNC, A0-A11, R/$\overline{W}$, ϕ2	V_{OH}	V_{SS} + 2.4	—	—	Vdc
Output Low Voltage (I_{LOAD} = 1.6 mAdc, V_{CC} = 4.75V) D0-D7, SYNC, A0-A11, R/$\overline{W}$, ϕ2	V_{OL}	—	—	V_{SS} + 0 6	Vdc
Power Dissipation	P_D	—	0.75	1 20	W
Capacitance (V_{in} = 0, T_A = 25°C, f = 1 MHz) RDY D0-D7 A0-A11, R/$\overline{W}$, SYNC ϕ2	C C_{in} C_{out} $C_{\phi 2}$	 — — — —	 — — — 50	 10 15 12 80	pF
I/O Port Pull-up Resistance	R_L	3.0	6 0	11.5	kohm

DETAILED MEMORY MAP

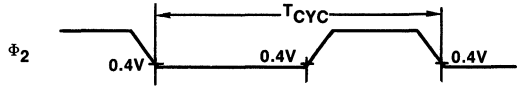
	HEX	
IRQ VECTOR HIGH	FFF	ROM
IRQ VECTOR LOW	FFE	
RES VECTOR HIGH	FFD	
RES VECTOR LOW	FFC	
NMI VECTOR HIGH	FFB	
NMI VECTOR LOW	FFA	
R6500/1 USER PROGRAM	FF9 – 800	
R6500/1E EXTENDED PROGRAM AREA (1)	7FF – 400	
UNASSIGNED		
CONTROL REGISTER	08F	INPUT/OUTPUT
UNASSIGNED	08E – 08B	
CLEAR PA1 NEG EDGE DETECTED (2)	08A	
CLEAR PA0 POS EDGE DETECTED (2)	089	
UPPER LATCH AND TRANSFER LATCH TO COUNTER (3)	088	
LOWER COUNT (3)	087	
UPPER COUNT	086	
LOWER LATCH	085	
UPPER LATCH	084	
PORT D	083	
PORT C	082	
PORT B	081	
PORT A	080	
UNASSIGNED		
USER RAM	03F – 000	RAM(4)

NOTES:
(1) Additional 1024 bytes are decoded for external memory addressing. This area can be used during debut, but cannot be used in a masked ROM R6500/1.
(2) I/O command only; i.e., no stored data.
(3) Clears Counter Overflow — Bit 7 in Control Register
(4) CAUTION: The device allows RAM mapping into 040-07F, 100-13F, 140-17F, 200-23F, 240-27F, 300-33F, and 340-37F; as well as 000-03F. The production R6500/1, however allows RAM mapping only at 000-03F.

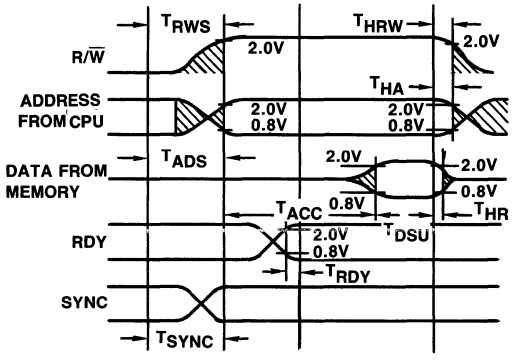
3

TIMING DIAGRAMS

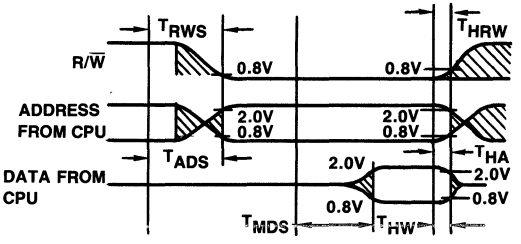
PHASE 2 (Φ2) TIMING REFERENCE



TIMING FOR READING FROM MEMORY

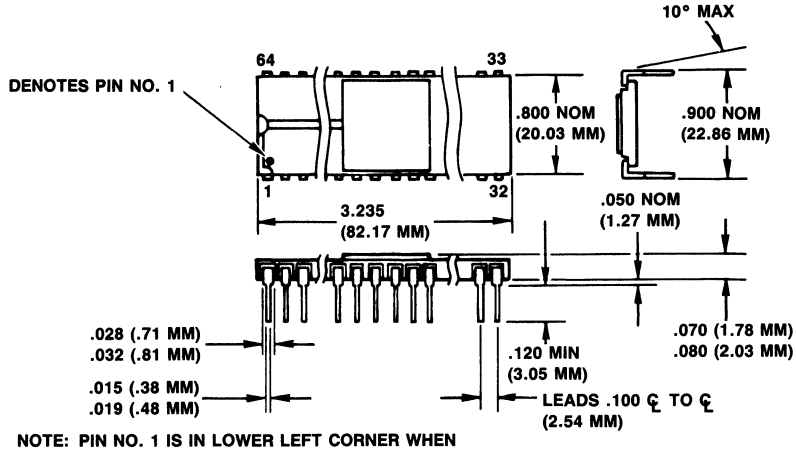


TIMING FOR WRITING TO MEMORY



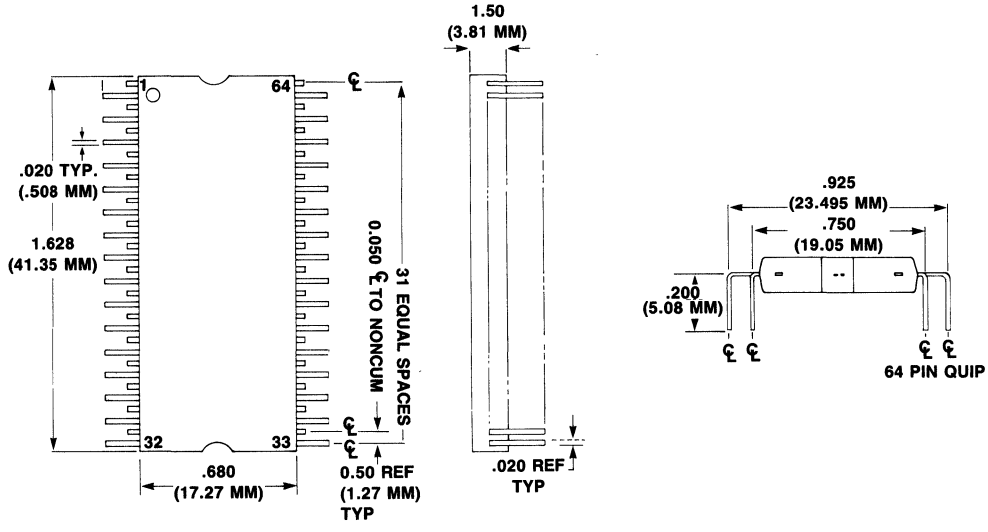
PACKAGE DIMENSIONS

R6500/1EC 64-PIN DIP CERAMIC



NOTE: PIN NO. 1 IS IN LOWER LEFT CORNER WHEN SYMBOLIZATION IS IN NORMAL ORIENTATION

R6500/1EQ 64-PIN QUIP PLASTIC



Rockwell

R6500/1EB and R6500/1EAB BACKPACK EMULATOR

INTRODUCTION

The Rockwell R6500/1EB and R6500/1EAB Backpack Emulator is the PROM prototyping version of the 8-bit, masked-ROM R6500/1 one-chip microcomputer. Like the R6500/1, the backpack device is totally upward/downward compatible with all members of the R6500/1 family. It is designed to accept standard 5-volt, 24-pin EPROMs or ROMs directly, in a socket on top of the Emulator. This packaging concept allows a standard EPROM to be easily removed, reprogrammed, then reinserted as often as desired.

The backpack devices have the same pinouts as the masked-ROM R6500/1 microcomputer. These 40 pins are functionally and operationally identical to the pins on the R6500/1, with some minor differences (described herein). The R6500/1 Microcomputer Product Description Document Order No. 212 includes a description of the interface signals and their functions. Whereas the masked-ROM R6500/1 provides 2K bytes of read-only memory, the R6500/1EB will address 3K bytes of external program memory. This extra memory accommodates program patches, test programs or optional programs during breadboard and prototype development states.

FEATURES

- PROM version of the R6500/1
- Completely pin compatible with R6500/1 single-chip microcomputers
- Profile approaches 40-pin DIP of R6500/1
- Accepts 5-volt, 24-pin industry-standard EPROMs —4K memories—2732, 2732A (3K bytes addressable)
- Use as prototyping tool or for low volume production
- 3K bytes of memory capacity (4K memories)
- 64 × 8 static RAM
- Separate power pin for RAM
- Software compatibility with the R6500 family
- 32 bi-directional TTL compatible I/O lines (4 ports)
- 1 bi-directional TTL compatible counter I/O line
- 16-bit programmable counter/latch with four modes (interval timer, pulse generator, event counter, pulse width measurement)
- 5 interrupts (reset, non-maskable, two external edge sensitive, counter)
- Crystal or external time base
- Single +5V power supply

3

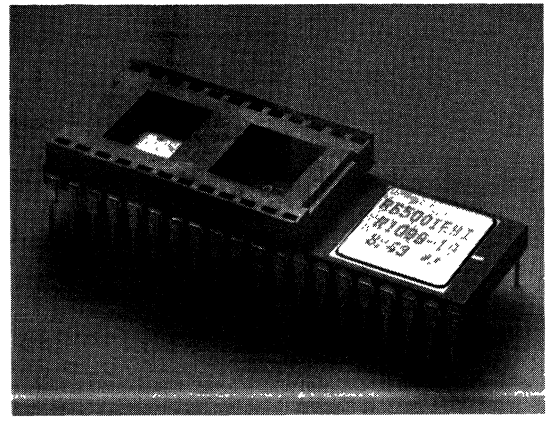
ORDERING INFORMATION

BACKPACK EMULATOR

Part Number	Memory Capacity	Compatible Memories	Temperature Range and Speed
R6500/1EB3	3K × 8	2732	0°C to 70°C 1 MHz
R6500/1EAB3	3K × 8	2732A (250 ns)	0°C to 70°C 2 MHz

SUPPORT PRODUCTS

Part Number	Description
S65-101	System 65 Microcomputer Development System
M65-040	PROM Programmer Module
M65-081	1-MHz R6500/1 Personality Module
M65-082	2-MHz R6500/1 Personality Module



R6500/1EB-R6500/1EAB Backpack Emulator

CONFIGURATION

The external memory must always occupy the upper 2K of available memory (addresses 800 through FFF) for implementation of interrupt vectors. See Memory Map. The Backpack Emulator provides a read block to the external memory where internal RAM or I/O are located in the same addresses as that occupied by external memory.

EXTERNAL FREQUENCY REFERENCE

The external frequency reference may be a crystal or a clock—the RC option is not available in the emulator device. The R6500/1EB and R6500/1EAB divide the input clock by two regardless of the source.

I/O PORT PULLUPS

The emulator devices have internal I/O port pullup resistors.

TEST MODE DELETED

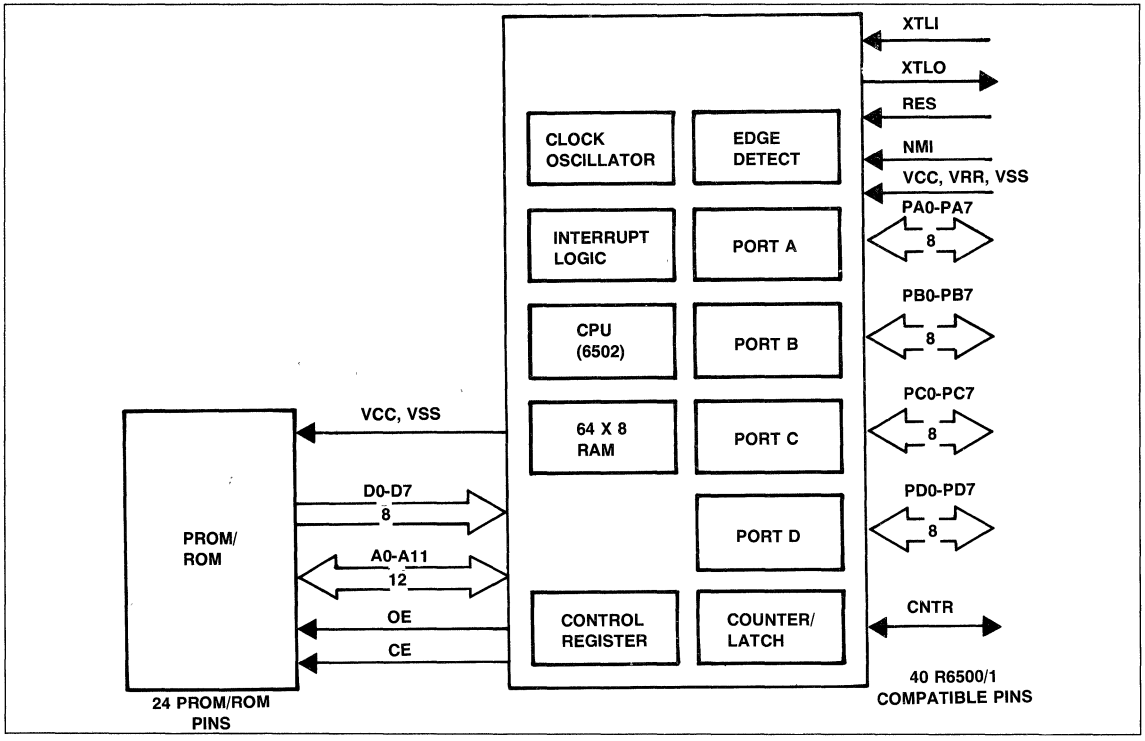
The test mode of the R6500/1 is not available on the Backpack Emulator.

PRODUCT SUPPORT

The Backpack Emulator is just one of the products that Rockwell offers to facilitate system and program development for the R6500/1.

The System 65 Microcomputer Development System with R6500/1 Personality Module supports both hardware and software development. Complete in-circuit user emulation with the R6500/1 Personality Module allows total system test and evaluation. With the optional PROM Programmer, System 65 can also be used to program EPROMs for the development activity. When PROM programs have been finalized, the PROM device can be sent to Rockwell for masking into the 2K ROM of the R6500/1.

In addition to support products, Rockwell offers regularly-scheduled designer's courses at regional centers.



R6500/1EB Interface Diagram

DETAILED MEMORY MAP

			HEX
PROM	IRQ VECTOR HIGH		FFF
	IRQ VECTOR LOW		FFE
	RES VECTOR HIGH		FFD
	RES VECTOR LOW		FFC
	NMI VECTOR HIGH		FFB
	NMI VECTOR LOW		FFA
	R6500/1 USER PROGRAM		FF9
			400
PROM	R6500/1EB EXTENDED PROGRAM AREA (1)		3FF
			400
NOT USED	UNASSIGNED		
I/O	CONTROL REGISTER		08F
	UNASSIGNED		08E
			08B
	CLEAR PA1 NEG EDGE DETECTED	(2)	08A
	CLEAR PA0 POS EDGE DETECTED	(2)	089
	UPPER LATCH AND TRANSFER LATCH TO COUNTER	(3)	088
	LOWER COUNT	(3)	087
	UPPER COUNT		086
	LOWER LATCH		085
	UPPER LATCH		084
	PORT D		083
	PORT C		082
	PORT B		081
	PORT A		080
NOT USED	UNASSIGNED		03F
RAM	USER RAM		000

NOTES

(1) Additional 1024 bytes are decoded for external memory addressing by the Backpack Emulator Device. This area can be used during debug, but cannot be used in a masked ROM R6500/1.

(2) I/O command only; i.e., no stored data.

(3) Clears Counter Overflow—Bit 7 in Control Register

(4) CAUTION: The device allows RAM mapping into 040-07F, 100-13F, 140-17F, 200-23F, 240-27F, 300-33F, and 340-37F; as well as 000-03F. The production R6500/1, however allows RAM mapping only at 000-03F.

RAM MAPPING

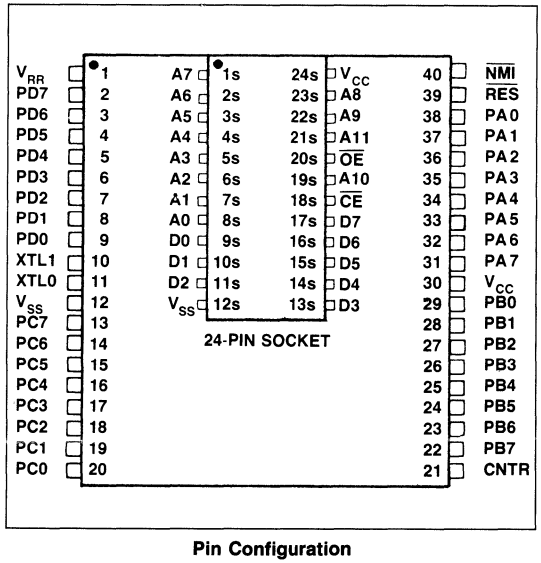
The Backpack Emulator allows RAM mapping into 040-07F, 100-13F, 140-17F, 200-23F, 240-27F, 300-33F and 340-37F, as well as 000-03F. The production R6500/1, however, allows RAM mapping only at 000-03F. This means that a write to location 40, for example, will write to location 0 in the Backpack Emulator, and to invalid RAM in the R6500/1 production part.

I/O PORT INITIALIZATION

Ports A, B, C, and D and the CNTR line in the Backpack Emulator are initialized to the logic high state two Ø2 clock cycles earlier than in the R6500/1. The $\overline{RES}$ line to the device must, however, still be held low for at least eight Ø2 clock cycles after V_{CC} reaches operating range. See timing diagram.

BACKPACK MEMORY SIGNAL DESCRIPTION

Signal Name	Pin No.	Description
D0-D7	9S-11S, 13S-17S	Data Bus Lines All instruction and data transfers take place on the data bus lines. The buffers driving the data bus lines have full three-state capability. Each data bus pin is connected to an input and an output buffer, with the output buffer remaining in the floating condition.
A0-A9	1S-8S, 23S, 24S	Address Bus Lines. The address bus lines are buffered by push/pull type drivers that can drive one standard TTL load.
A10	19S	Address Bus Line 10. This address line has the same characteristics and functions as Lines A0-A9
$\overline{CE}$	18S	$\overline{CE}$ is active when the address is 400-FFF This line can drive one TTL load
$\overline{OE}$	20S	Memory Enable Line This signal provides the output enable for the memory to place information on the data bus lines This signal is driven by the R/$\overline{W}$ signal from the CPU and then inverted by a standard TTL inverter, to form $\overline{OE}$.
V_{CC}	24S	Main Power Supply $5V. This pin is tied directly to pin 30 (V_{CC}).
A11	21S	Address Bus Line II. This pin is tied to A11. During backup power, power is supplied only to the RAM memory, and not to the PROMs.
V_{SS}	12S	Signal and Power Ground (zero volts). This pin is tied directly to pin 12 (V_{SS}).

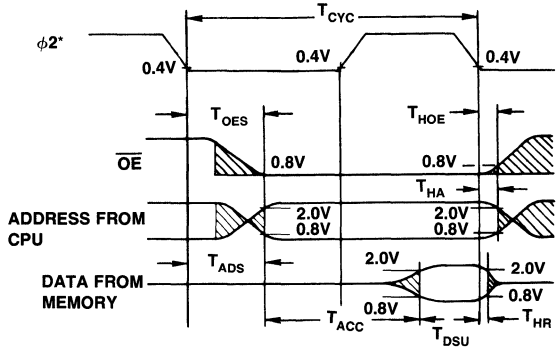


Pin Configuration

READ TIMING CHARACTERISTICS

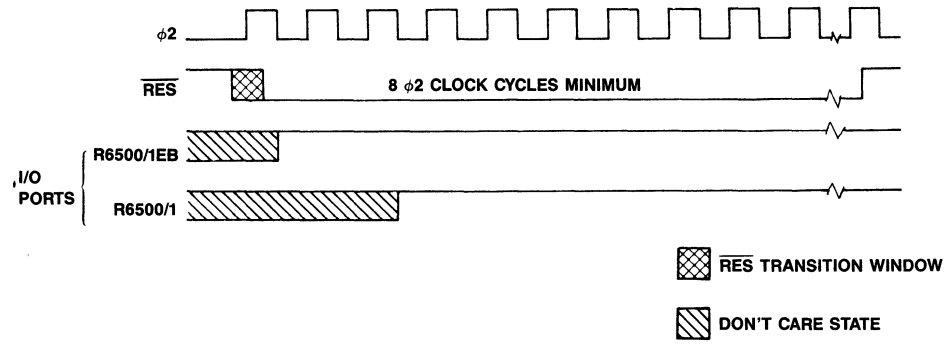
Signal	Symbol	1 MHz		2 MHz		Unit
		Min.	Max.	Min.	Max.	
$\overline{OE}$ setup time from CPU	T_{OES}	—	300	—	150	ns
Address setup time from CPU	T_{ADS}	—	300	—	150	ns
Memory read access time	T_{ACC}	—	525	—	250	ns
Data stabilization time	T_{DSU}	150	—	100	—	ns
Data hold time—Read	T_{HR}	10	—	10	—	ns
Address hold time	T_{HA}	30	—	30	—	ns
$\overline{OE}$ hold time	T_{HOE}	30	—	30	—	ns
Cycle Time	T_{CYC}	1.0	10.0	0.5	10.0	μs

READ TIMING WAVEFORMS



*ϕ2 IS SHOWN FOR REFERENCE ONLY AND IS NOT AVAILABLE EXTERNAL TO THE DEVICE.

I/O PORT INITIALIZATION TIMING



MAXIMUM RATINGS*

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to +7.0	Vdc
Input Voltage	V_{IN}	−0.3 to +7.0	Vdc
Operating Temperature Commercial	T_A	T_L to T_H 0 to +70	°C
Storage Temperature	T_{STG}	−55 to +150	°C

***NOTE:** Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in other sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

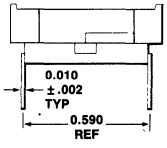
(V_{CC} = 5.0V ±5%, V_{SS} = 0V; T_A = 0° to 70°, unless otherwise specified)

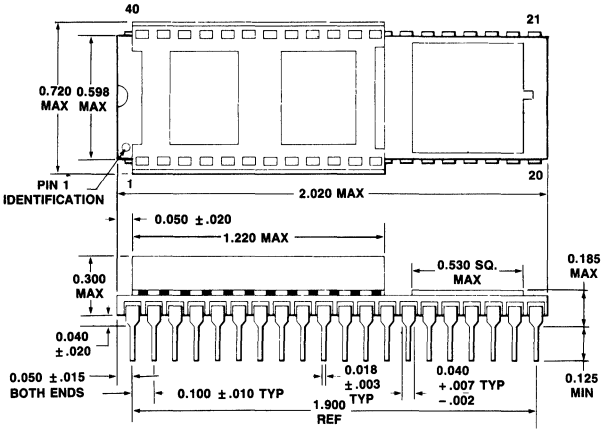
Parameter	Symbol	Min	Typ[1]	Max	Unit	Test Conditions
Input High Voltage D0–D7	V_{IH}	V_{SS} +2 4	—	—	V	
Input Low Voltage D0–D7	V_{IL}	—	—	V_{SS} +0.8	V	
Input Leakage Current (Three-State Off) D0–D7	I_{IN}	—	—	±10.0	µA	V_{IN} = 0.4 to 2.4V V_{CC} = 5.25V
Output High Voltage (Except XTLO) D0–D7, A0–A11, $\overline{OE}$	V_{OH}	V_{SS} +2.4	—	—	V	I_{LOAD} = −100 µA V_{SS} = 4.75V
Output Low Voltage D0–D7, A0–A11, $\overline{OE}$	V_{OL}	—	—	V_{SS} +0.6	V	I_{LOAD} = 1.6 mA V_{SS} = 4.75V
I/O Port Pull-Up Resistance	R_L	3.0	6.0	11 5	Kohm	
Input Capacitance D0–D7	C_{IN}	—	—	15	pF	T_A = 25°C V_{IN} = 0V f = 1.0 MHz
Output Capacitance (Three-State Off) A0–A11	C_{OUT}	—	—	12	pF	T_A = 25°C V_{IN} = 0V f = 1.0 MHz
Power Dissipation (Loss EPROM)	P_D	—	800	1300	mW	T_A = 0°C

Notes:
1. Typical values measured at T_A = 25°C and V_{CC} = 5.0V.
2. Negative sign indicates outward current flow, positive indicates inward flow.

PACKAGE DIMENSIONS

40-PIN BACKPACK





Rockwell

R6500/11, R6500/12, R6500/15 AND R6500/16 ONE-CHIP MICROCOMPUTERS

SECTION 1 INTRODUCTION

1.1 FEATURES

- Enhanced 6502 CPU
  - —Four new bit manipulation instructions:
    - Set Memory Bit (SMB)
    - Reset Memory Bit (RMB)
    - Branch on Bit Set (BBS)
    - Branch on Bit Reset (BBR)
  - —Decimal and binary arithmetic modes
  - —13 addressing modes
  - —True indexing
- 3K-byte mask-programmable ROM (R6500/11, R6500/12)
- 4K-byte mask-programmable ROM (R6500/15, R6500/16)
- 192-byte static RAM
- 32 TTL-compatible I/O lines (R6500/11, R6500/15)
- 56 TTL-compatible I/O lines (R6500/12, R6500/16)
- One 8-bit port may be tri-stated under software control
- One 8-bit port with programmable latched input
- Two 16-bit programmable counter/timers, with latches
  - —Pulse width measurement
  - —Asymmetrical pulse generation
  - —Pulse generation
  - —Interval timer
  - —Event counter
  - —Retriggerable interval timer
- Serial port
  - —Full-duplex asynchronous operation mode
  - —Selectable 5- to 8-bit characters
  - —Wake-up feature
  - —Synchronous shift register mode
  - —Standard programmable bit rates, programmable up to 62.5K bits/sec @ 1 MHz
- Ten interrupts
  - —Four edge-sensitive lines; two positive, two negative
  - —Reset
  - —Non-maskable
  - —Two counter underflows
  - —Serial data received
  - —Serial data transmitted
- Bus expandable to 16K bytes of external memory
- Flexible clock circuitry
  - —2-MHz or 1-MHz internal operation
  - —Internal clock with external 2 MHz to 4 MHz series resonant XTAL at two or four times internal frequency
  - —External clock input divided by one, two or four
- 1μs minimum instruction execution time @ 2 MHz
- NMOS-3 silicon gate, depletion load technology
- Single +5V power supply
- 12 mW stand-by power for 32 bytes of the 192-byte RAM
- 40-pin DIP (R6500/11 and R6500/15)
- 64-pin QUIP (R6500/12 and R6500/16)

3

1.2 SUMMARY

These Rockwell microcomputers are complete, high-performance 8-bit NMOS-3 microcomputers on a single chip, and are compatible with all members of the R6500 family.

The R6500/11 consists of an enhanced 6502 CPU, an internal clock oscillator, 3072 bytes of Read-Only Memory, 192 bytes of Random Access Memory (RAM) and versatile interface circuitry. The interface circuitry includes two 16-bit programmable timer/counters, 32 bidirectional input/output lines (including four edge-sensitive lines and input latching on one 8-bit port), a full-duplex serial I/O channel, ten interrupts and bus expandability.

The R6500/15 is identical to the R6500/11 except it has 4K of ROM.

The R6500/12 consists of all the features of the R6500/11 plus three additional I/O ports. It is packaged in a 64 pin QUIP.

The R6500/16 is identical to the R6500/12 except it has 4K of ROM.

The innovative architecture and the demonstrated high performance of the R6502 CPU, as well as instruction simplicity, results in system cost-effectiveness and a wide range of computational power. These features make either device a leading candidate for microcomputer applications.

To allow prototype circuit development, Rockwell offers a PROM-compatible 64-pin extended microprocessor device. This device, the R6511Q, provides all R6500/11 or R6500/15 interface lines, plus the address bus, data bus and control lines to interface with external memory. With the addition of external circuits it can also be used to emulate the R6500/12 or R6500/16 (contact Rockwell sales offices listed on the back page for details).

A backpack emulator, the R65/11EB, is available for developing R6500/11 applications. No backpack part is available for the R6500/12.

The R6511Q may also be used as a CPU-RAM-I/O counter device in multichip systems.

Rockwell supports development of the devices with the System 65 Microcomputer Development System and the R6500/* Family of Personality Modules. Complete in-circuit emulation with the R6500/* Family of Personality Modules allows total system test and evaluation.

This product description is for the reader familiar with the R6502 CPU hardware and programming capabilities. A detailed description of the R6502 CPU hardware is included in the R6500 Microcomputer System Hardware Manual (Order Number 201). A description of the instruction capabilities of the R6502 CPU is contained in the R6500 Microcomputer System Programming Manual (Order Number 202).

1.3 CUSTOMER OPTIONS

The R6500/11 microcomputer is available with the following customer specified mask options:

- Option 1 Crystal or RC oscillator
- Option 2 Clock divide by 2 or 4
- Option 3 Clock MASTER Mode or SLAVE Mode
- Option 4 Port A with or without internal pull-up resistors
- Option 5 Port B with or without internal pull-up resistors
- Option 6 Port C with or without internal pull-up resistors

All options should be specified on an R6500/11 or /15 order form.

The R6500/12 or /16 is available with all of the above options plus:

- Option 7 Port F with or without internal pull-up resistors
- Option 8 Port G with or without internal pull-up resistors

SECTION 2
INTERFACE REQUIREMENTS

This section describes the interface requirements for the single chip microcomputer devices. Figure 2-1 is the Interface Diagram for the devices, Figure 2-2 and Figure 2-3 show the mechanical outline and pin out configurations and Table 2-1 describes the function of each pin. Figure 3-1 has a detailed block diagram of the device which illustrates its internal functions.

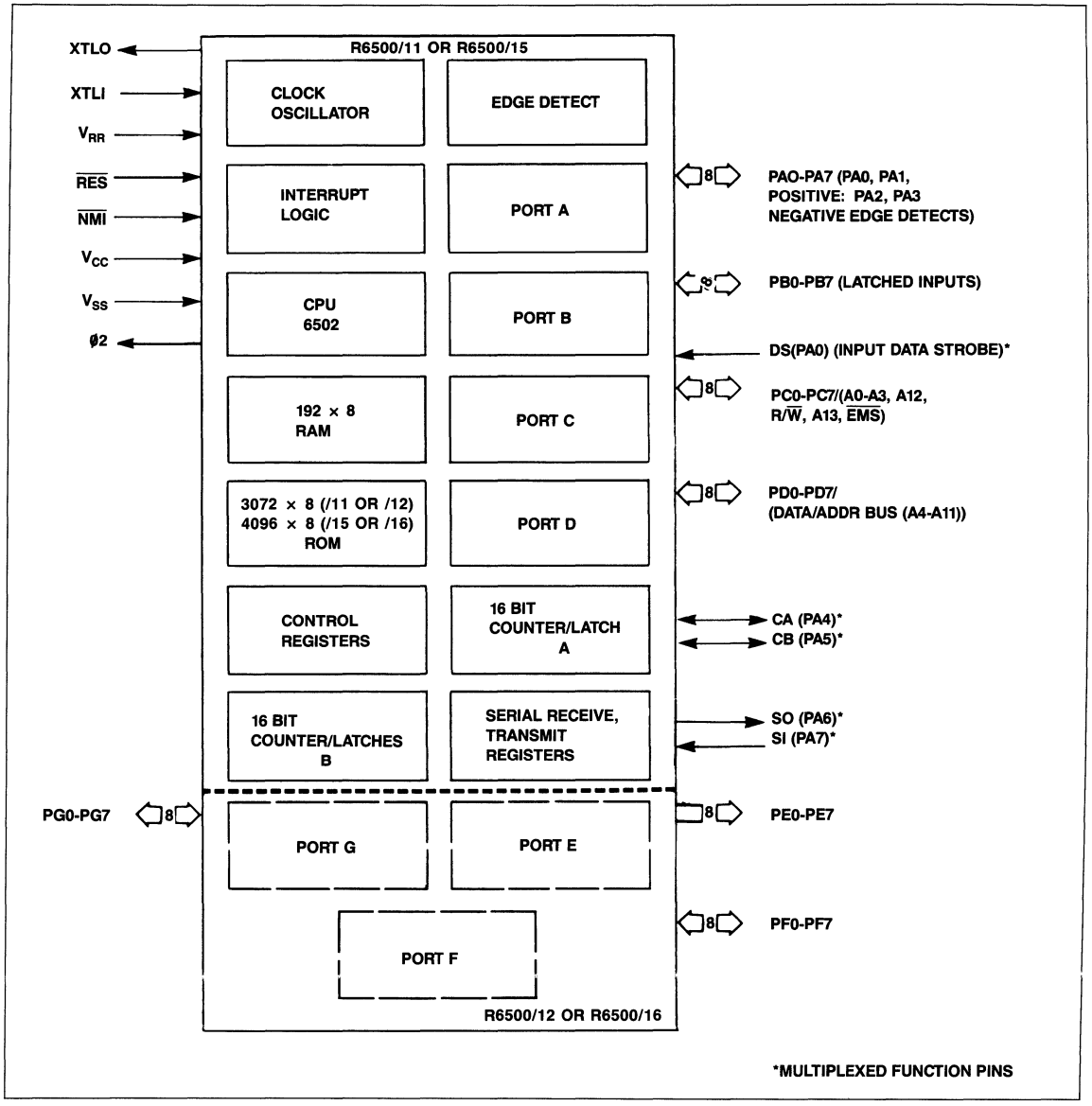


Figure 2.1 Interface Diagram

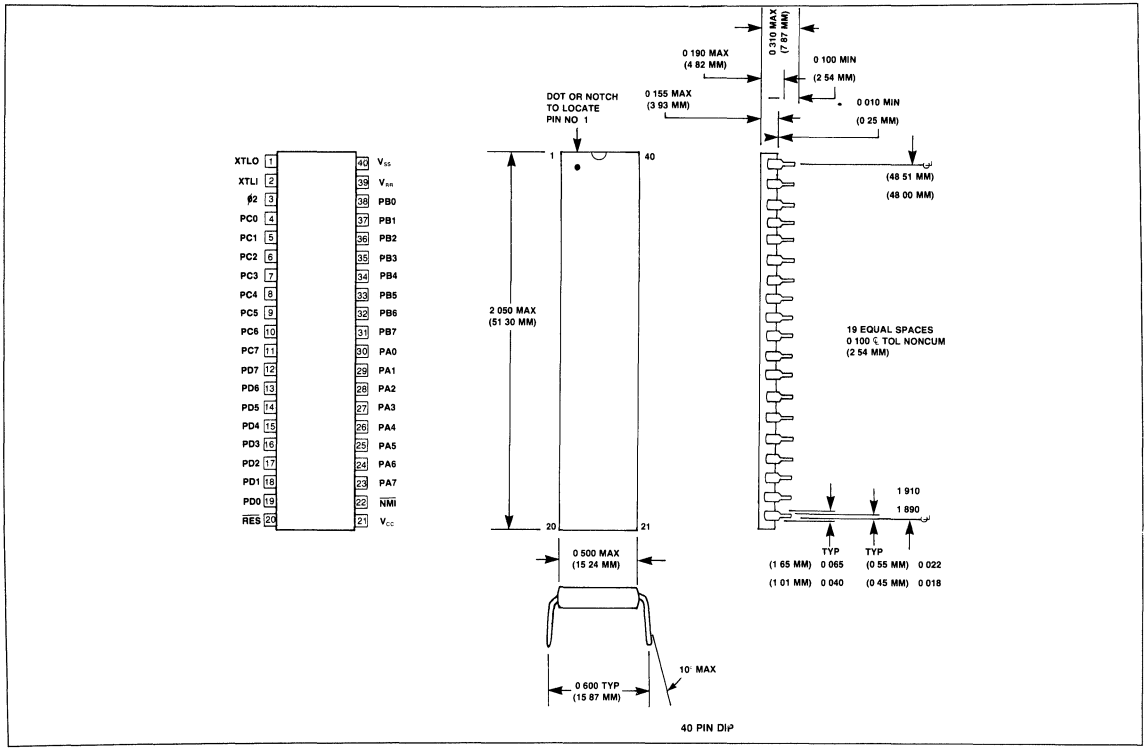


Figure 2-2. R6500/11 or /15 Mechanical Outline and Pin Out Configuration

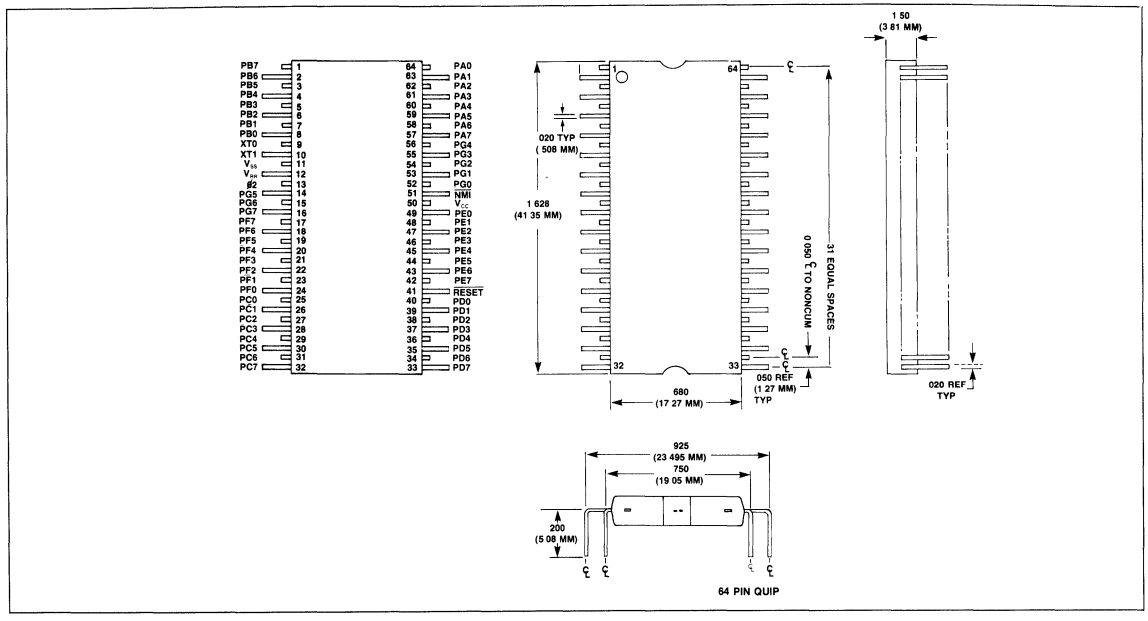


Figure 2-3. R6500/12 or /16 Mechanical Outline and Pin Out Configuration

Table 2-1. Pin Descriptions

Signal Name	Pin Number		Description
	R6500/11 or /15	R6500/12 or /16	
V_{CC}	21	50	Main power supply +5V
V_{RR}	39	12	Separate power pin for RAM. In the event that V_{CC} power is lost, this power retains RAM data.
V_{SS}	40	11	Signal and power ground (0V)
XTLI	2	10	Crystal or clock input for internal clock oscillator. Also allows input of X1 clock signal if XTLO is connected to V_{SS}, or X2 or X4 clock if XTLO is floated
XTLO	1	9	Crystal output from internal clock oscillator.
$\overline{RES}$	20	41	The Reset input is used to initialize the device. This signal must not transition from low to high for at least eight cycles after V_{CC} reaches operating range and the internal oscillator is stabilized.
$\phi 2$	3	13	Clock signal output at internal frequency.
$\overline{NMI}$	22	51	A negative going edge on the Non-Maskable Interrupt signal requests that a non-maskable interrupt be generated within the CPU.
PA0-PA7 PB0-PB7 PC0-PC7 PD0-PD7	30-23 38-31 4-11 19-12	64-57 8-1 25-32 40-33	Four 8-bit ports used for either input/output. Each line of Ports A, B and C consist of an active transistor to V_{SS} and an optional passive pull-up to V_{CC}. In the abbreviated or multiplexed modes of operation Port C has an active pull-up transistor. Port D functions as either an 8-bit input or 8-bit output port. It has active pull-up and pull-down transistors.
PE0-PE7 PF0-PF7 PG0-PG7	N/A N/A N/A	49-42 24-17 52-56 4 14-16	For the R6500/12 or /16, the 64 pin QUIP version, three additional ports (24 lines) are provided. Each line consists of an active transistor to V_{SS}. PF0-PF7 and PG0-PG7 are bidirectional, and an optional passive pull-up to V_{CC} is provided. PE0-PE7 is outputs only with an active pull-up. All ports will source 100 μamps at 2.4V except port E (PE0-PE7) which will source 1 mA at 1.5V.

SECTION 3
SYSTEM ARCHITECTURE

This section provides a functional description of the devices. Functionally they consist of a CPU, both ROM and RAM memories, four 8-bit parallel I/O ports (seven in the 64-pin versions), a serial I/O port, dual counter/latch circuits, a mode control register, and an interrupt flag/enable dual register circuit. A block diagram of the system is shown in Figure 3-1.

NOTE

Throughout this document, unless specified otherwise, all memory or register address locations are specified in hexadecimal notation.

3.1 CPU LOGIC

The internal CPU is a standard 6502 configuration with an 8-bit Accumulator register, two 8-bit Index Registers (X and Y); an 8-bit Stack Pointer register, an ALU, a 16-bit Program Counter, and standard instruction register/decode and internal timing control logic.

3.1.1 Accumulator

The accumulator is a general purpose 8-bit register that stores the results of most arithmetic and logic operations. In addition, the accumulator usually contains one of the two data words used in these operations.

3.1.2 Index Registers

There are two 8-bit index registers, X and Y. Each index register can be used as a base to modify the address data program counter and thus obtain a new address—the sum of the program counter contents and the index register contents.

When executing an instruction which specifies indirect addressing, the CPU fetches the op code and the address, and modifies the address from memory by adding the index register to it prior to loading or storing the value of memory.

Indexing greatly simplifies many types of programs, especially those using data tables.

3.1.3 Stack Pointer

The Stack Pointer is an 8-bit register. It is automatically incremented and decremented under control of the microprocessor to perform stack manipulation in response to either user instructions, an internal $\overline{IRQ}$ interrupt, or the external interrupt line $\overline{NMI}$. The Stack Pointer must be initialized by the user program.

The stack allows simple implementation of multiple level interrupts, subroutine nesting and simplification of many types of data manipulation. The JSR, BRK, RTI and RTS instructions use the stack and Stack Pointer.

The stack can be envisioned as a deck of cards which may only be accessed from the top. The address of a memory location is stored (or "pushed") onto the stack. Each time data are to be pushed onto the stack, the Stack Pointer is placed on the Address Bus, data are written into the memory location addressed by the Stack Pointer, and the Stack Pointer is decremented by 1. Each time data are read (or "pulled") from the stack, the Stack Pointer is incremented by 1. The Stack Pointer is then placed on the Address Bus, and data are read from the memory location addressed by the Pointer.

The stack is located on zero page, i.e., memory locations 00FF-0040. After reset, which leaves the Stack Pointer indeterminate, normal usage calls for its initialization at 00FF.

3.1.4 Arithmetic And Logic Unit (ALU)

All arithmetic and logic operations take place in the ALU, including incrementing and decrementing internal registers (except the Program Counter). The ALU cannot store data for more than one cycle. If data are placed on the inputs to the ALU at the beginning of a cycle, the result is always gated into one of the storage registers or to external memory during the next cycle.

Each bit of the ALU has two inputs. These inputs can be tied to various internal buses or to a logic zero; the ALU then generates the function (AND, OR, SUM, and so on) using the data on the two inputs.

3.1.5 Program Counter

The 16-bit Program Counter provides the addresses that are used to step the processor through sequential instructions in a program. Each time the processor fetches an instruction from program memory, the lower (least significant) byte of the Program Counter (PCL) is placed on the low-order bits of the Address Bus and the higher (most significant) byte of the Program Counter (PCH) is placed on the high-order 8 bits of the Address Bus. The Counter is incremented each time an instruction or data is fetched from program memory.

3.1.6 Instruction Register and Instruction Decode

Instructions are fetched from ROM or RAM and gated onto the Internal Data Bus. These instructions are latched into the Instruction Register then decoded along with timing and interrupt signals to generate control signals for the various registers.

3.1.7 Timing Control

The Timing Control Logic keeps track of the specific instruction cycle being executed. This logic is set to T0 each time an instruction fetch is executed and is advanced at the beginning of each Phase One clock pulse for as many cycles as are required to complete the instruction. Each data transfer which takes place between the registers is caused by decoding the contents of both the instruction register and timing control unit.

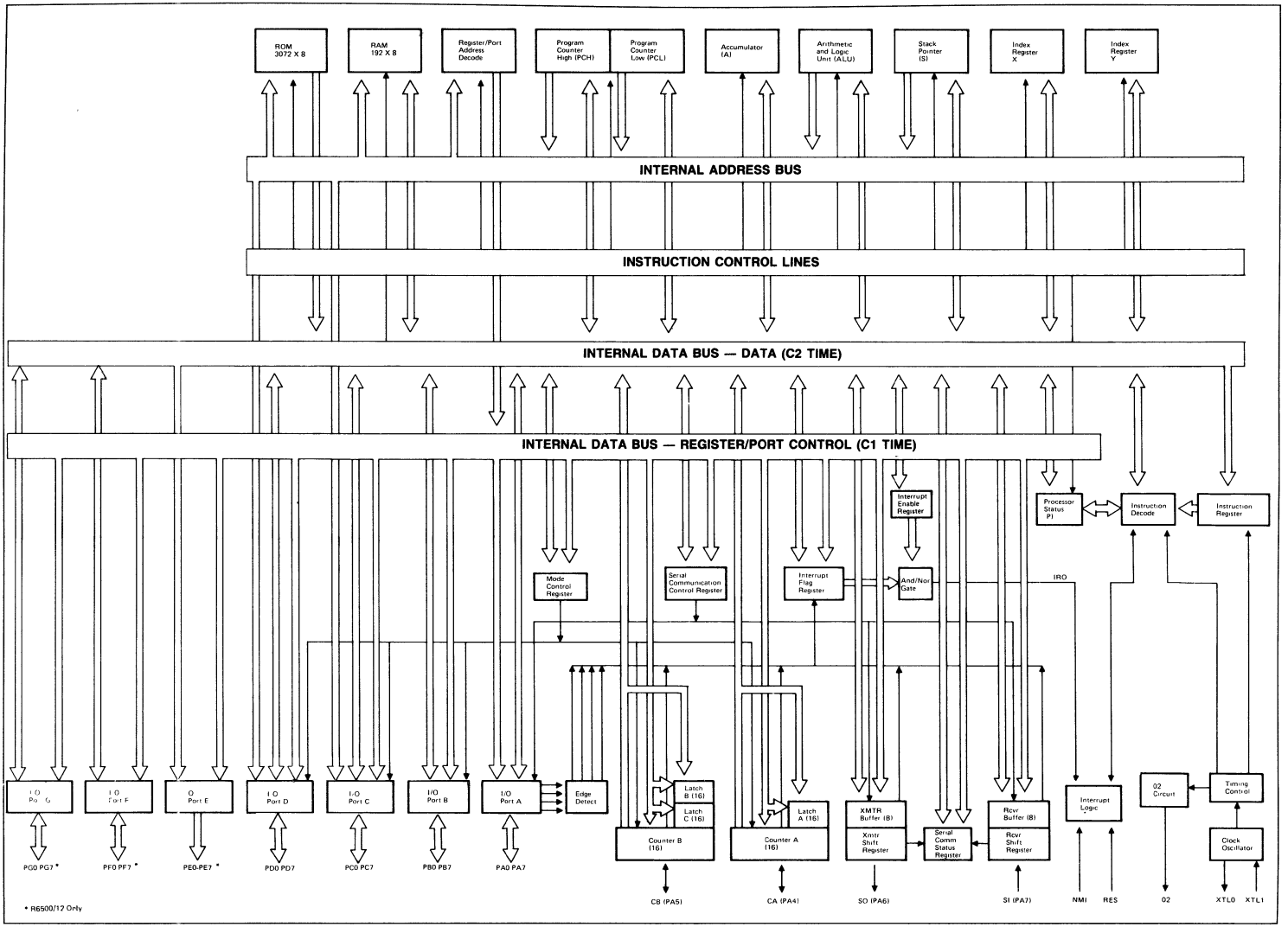


Figure 3-1. System Block Diagram

3.1.8 Interrupt Logic

Interrupt logic controls the sequencing of three interrupts; $\overline{RES}$, $\overline{NMI}$ and $\overline{IRQ}$. $\overline{IRQ}$ is generated by any one of eight conditions: 2 Counter Overflows, 2 Positive Edge Detects, 2 Negative Edge Detects, and 2 Serial Port Conditions.

3.2 NEW INSTRUCTIONS

In addition to the standard 6502 instruction set, four instructions have been added to the devices to simplify operations that previously required a read/modify/write operation. In order for these instructions to be equally applicable to any I/O ports, with or without mixed input and output functions, the I/O ports have been designed to read the contents of the specified port data register during the Read cycle of the read/modify/write operation, rather than I/O pins as in normal read cycles. The added instructions and their format are explained in the following subparagraphs. Refer to Appendix A for the Op Code mnemonic addressing matrix for these added instructions.

3.2.1 Set Memory Bit (SMB m, Addr.)

This instruction sets to "1" one of the 8-bit data field specified by the zero page address (memory or I/O port). The first byte of the instruction specifies the SMB operation and 1 of 8 bits to be set. The second byte of the instruction designates address (00-FF) of the byte or I/O port to be operated upon.

3.2.2 Reset Memory Bit (RMB m, Addr.)

This instruction is the same operation and format as SMB instruction except a reset to "0" of the bit results.

3.2.3 Branch On Bit Set Relative (BBS m, Addr, DEST)

This instruction tests one of 8 bits designated by a three bit immediate field within the first byte of the instruction. The second byte is used to designate the address of the byte to be tested within the zero page address range (memory or I/O ports). The third byte of the instruction is used to specify the 8 bit relative address to which the instruction branches if the bit tested is a "1". If the bit tested is not set, the next sequential instruction is executed.

3.2.4 Branch On Bit Reset Relative (BBR m, Addr, DEST)

This instruction is the same operation and format as the BBS instruction except that a branch takes place if the bit tested is a "0".

3.3 READ-ONLY-MEMORY (ROM)

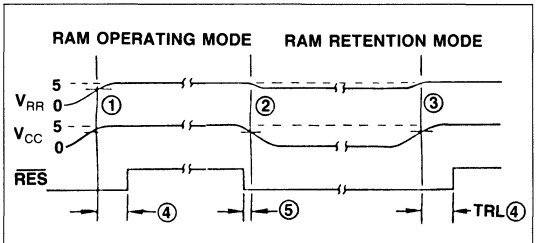
In the R6500/11 or R6500/12 the ROM consists of 3072 bytes (3K) of mask programmable memory with an address space from F400 to FFFF. ROM locations FFFA through FFFF are assigned for interrupt and reset vectors.

In the R6500/15 or R6500/16 the ROM consists of 4096 bytes (4K) of mask programmable memory with an address space from F000 to FFFF. ROM locations FFFA through FFFF are assigned for interrupt and reset vectors.

3.4 RANDOM ACCESS MEMORY (RAM)

The RAM consists of 192 bytes of read/write memory with an assigned page zero address of 0040 through 00FF. The R6500/11 provides a separate power pin (V_{RR}) which may be used for standby power for 32 bytes located at 0040-005F. In the event of the loss of V_{CC} power, the lowest 32 bytes of RAM data will be retained if standby power is supplied to the V_{RR} pin. If the RAM data retention is not required then V_{RR} must be connected to V_{CC}. During operation V_{RR} must be at the V_{CC} level.

For the RAM to retain data upon loss of V_{CC}, V_{RR} must be supplied within operating range and $\overline{RES}$ must be driven low at least eight Ø2 clock pulses before V_{CC} falls out of operating range. $\overline{RES}$ must then be held low while V_{CC} is out of operating range and until at least eight Ø2 clock cycles after V_{CC} is again within operating range and the internal Ø2 oscillator is stabilized. V_{RR} must remain within V_{CC} operating range during normal operation. When V_{CC} is out of operating range, V_{RR} must remain within the V_{RR} retention range in order to retain data. Figure 3.2 shows typical waveforms.



1 INITIAL APPLICATION OF V_{CC} AND V_{RR}.
2 LOSS OF V_{CC}, RAM ON STANDBY POWER.
3 REAPPLICATION OF V_{CC}.
4 >8 Ø2 CLOCK PULSES AFTER OSCILLATOR STABILIZATION.
5 >8 Ø2 CLOCK PULSES.

Figure 3-2. Data Retention Timing

3.5 CLOCK OSCILLATOR

Three customer selectable mask options are available for controlling the device timing. It can be ordered with a *crystal or RC* oscillator, a *divide by 2 or divide by 4* countdown network and for *clock master mode or clock slave mode* operation.

For 2 MHz internal operations the divide by two option must be specified.

A reference frequency can be generated with the on-chip oscillator using either an external crystal or an external resistor depending on the mask option selected. The oscillator reference frequency passes through an internal countdown network (divide by 2 or divide by 4 option) to obtain the internal operating frequency (see Figure 3-3a and 3-3b). The external crystal generated reference frequency is a preferred method since the resistor method can have tolerances approaching 50%.

Note:
When operating at a 1 MHz internal frequency place a 15-22 pf capacitor between XTLO and ground.

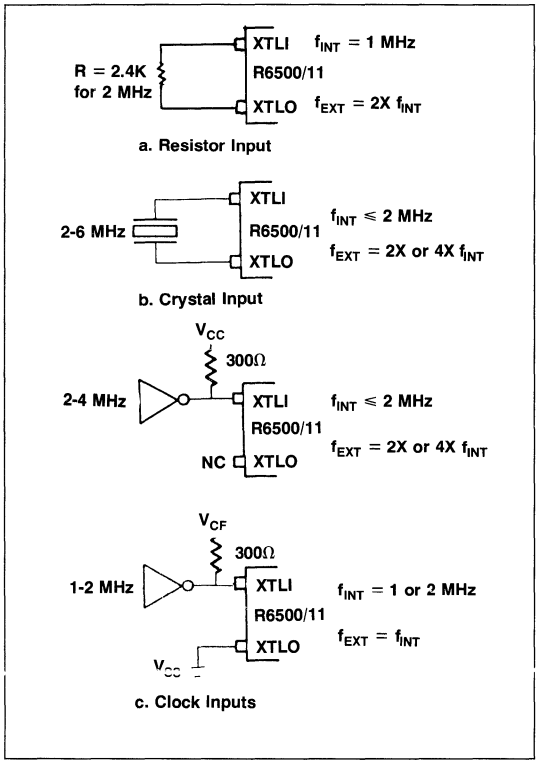


Figure 3-3. Clock Oscillator Input Options

Internal timing can also be controlled by driving the XTLI pin with an external frequency source. Figure 3-3c shows typical connections. If XTLO is left floating, the external source is divided by the internal countdown network. However, if XTLO is tied to V_{SS}, the internal countdown network is bypassed causing the chip to operate at the frequency of the external source.

The operation described above assumed a CLOCK MASTER MODE mask option. In this mode a frequence source (crystal, RC network or external source) must be applied to the XTLI and XTLO pins. Ø2 is a buffered output signal which closely approximates the internal timing. When a common external source is used to drive multiple devices the internal timing between devices as well as their Ø2 outputs will be skewed in time. If skewing represents a system problem it can be avoided by the Master/Slave connection and options shown in Figure 3-4.

One device is operated in the CLOCK MASTER MODE and a second in the CLOCK SLAVE MODE. Mask options in the SLAVE unit convert the Ø2 signal into a clock input pin which is tightly coupled to the internal timing generator. As a result the internal timing of the MASTER and SLAVE units are synchronized with minimum skew. If the Ø2 signal to the SLAVE unit is inverted, the MASTER and SLAVE UNITS WILL OPERATE OUT OF PHASE. This approach allows the two devices to share external memory using cycle stealing techniques.

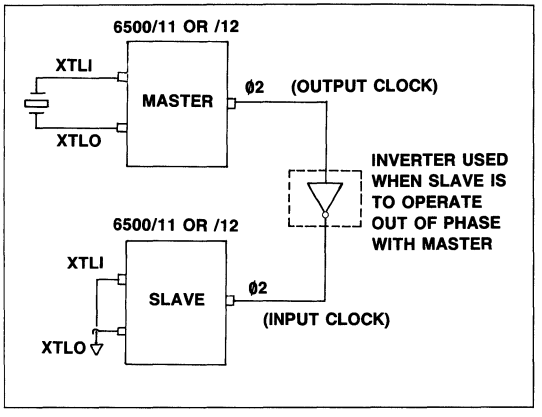


Figure 3-4. Master/Slave Connections

3.6 MODE CONTROL REGISTER (MCR)

The Mode Control Register contains control bits for the multifunction I/O ports and mode select bits for Counter A and Counter B. Its setting, along with the setting of the Serial Communications Control Register (SCCR), determines the basic configuration of the device in any application. Initializing this register is one of the first actions of any software program. The Mode Control Register bit assignment is shown in Figure 3-5.

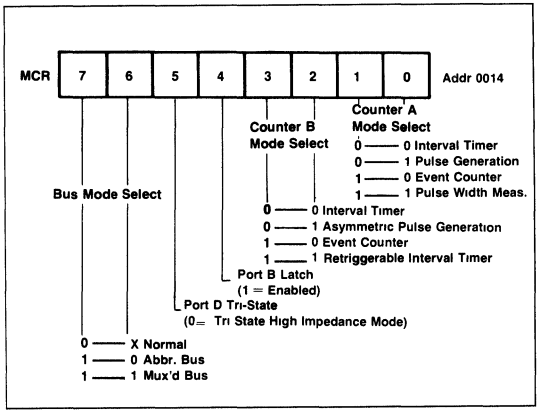


Figure 3-5. Mode Control Register

The use of Counter A Mode Select is shown in Section 6.1.

The use of Counter B Mode Select is shown in Section 6.2.

The use of Port B Latch Enable is shown in Section 4.4.

The use of Port D in Tri-State Enable is shown in Section 4.6.

The use of Bus Mode Select is shown in Section 4.5 and 4.6.

3.7 INTERRUPT FLAG REGISTER (IFR) AND INTERRUPT ENABLE REGISTER (IER)

An $\overline{IRQ}$ interrupt request can be initiated by any or all of eight possible sources. These sources are all capable of being enabled or disabled by the use of the appropriate interrupt enabled bits in the Interrupt Enable Register (IER). Multiple simultaneous interrupts will cause the $\overline{IRQ}$ interrupt request to remain active until all interrupting conditions have been serviced and cleared.

The Interrupt Flag Register contains the information that indicates which I/O or counter needs attention. The contents of the Interrupt Flag Register may be examined at any time by reading at address: 0011. Edge detect IFR bits may be cleared by executing a RMB instruction at address location 0010. The RMB X, (0010) instruction reads FF, modifies bit X to a "0", and writes the modified value at address location 0011. In this way IFR bits set to a "1" after the read cycle of a Read-Modify-Write instruction (such as RMB) are protected from being cleared. A logic "1" is ignored when writing to edge detect IFR bits.

Each IFR bit has a corresponding bit in the Interrupt Enable Register which can be set to a "1" by writing a "1" in the respective bit position at location 0012. Individual IER bits may be cleared by writing a "0" in the respective bit position, or by $\overline{RES}$. If set to a "1", an IRQ will be generated when the corresponding IFR bit becomes true. The Interrupt Flag Register and Interrupt Enable Register bit assignments are shown in Figure 3-6 and the functions of each bit are explained in Table 3-1.

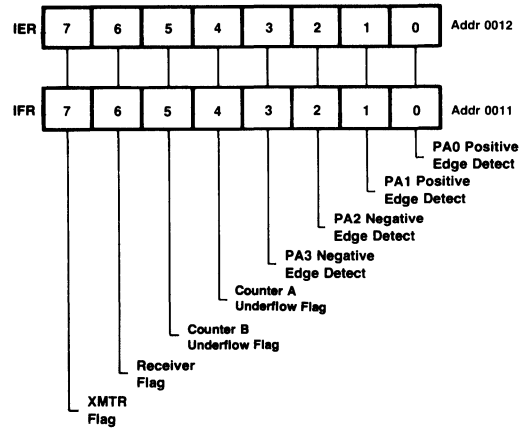


Figure 3-6. Interrupt Enable and Flag Registers

Table 3-1. Interrupt Flag Register Bit Codes

BIT CODE	FUNCTION
IFR 0:	PA0 Positive Edge Detect Flag—Set to a "1" when a positive going edge is detected on PA0. Cleared by RMB O (0010) instruction or by $\overline{RES}$.
IFR 1:	PA1 Positive Edge Detect Flag—Set to a 1 when a positive going edge is detected on PA1. Cleared by RMB 1 (0010) instruction or by $\overline{RES}$.
IFR 2:	PA2 Negative Edge Detect Flag—Set to a 1 when a negative going edge is detected on PA2. Cleared by RMB 2 (0010) instruction or by $\overline{RES}$.
IFR 3:	PA3 Negative Edge Detect Flag—Set to 1 when a negative going edge is detected on PA3. Cleared by RMB 3 (0010) instruction or by $\overline{RES}$.
IFR 4:	Counter A Underflow Flag—Set to a 1 when Counter A underflow occurs. Cleared by reading the Lower Counter A at location 0018, by writing to address location 001A, or by $\overline{RES}$.
IFR 5:	Counter B Underflow Flag—Set to a 1 when Counter B underflow occurs. Cleared by reading the Lower Counter B at location 001C, by writing to address location 001E, or by $\overline{RES}$.
IFR 6:	Receiver Interrupt Flag—Set to a 1 when any of the Serial Communication Status Register bits 0 through 3 is set to a 1. Cleared when the Receiver Status bits (SCSR 0-3) are cleared or by $\overline{RES}$
IFR 7:	Transmitter Interrupt Flag—Set to a 1 when SCSR 6 is set to a 1 while SCSR 5 is a 0 or SCSR 7 is set to a 1. Cleared when the Transmitter Status bits (SCSR 6 & 7) are cleared or by $\overline{RES}$.

3.8 PROCESSOR STATUS REGISTER

The 8-bit Processor Status Register, shown in Figure 3-7, contains seven status flags. Some of these flags are controlled by the user program; others may be controlled both by the user's program and the CPU. The R6502 instruction set contains a number of conditional branch instructions which are designed to allow testing of these flags. Each of the eight processor status flags is described in the following sections.

3.8.1 Carry Bit (C)

The Carry Bit (C) can be considered as the ninth bit of an arithmetic operation. It is set to logic 1 if a carry from the eighth bit has occurred or cleared to logic 0 if no carry occurred as the result of arithmetic operations.

The Carry Bit may be set or cleared under program control by use of the Set Carry (SEC) or Clear Carry (CLC) instruction, respectively. Other operations which affect the Carry Bit are ADC, ASL, CMP, CPX, CPY, LSR, PLP, ROL, ROR, RTI, and SBC.

3.8.2 Zero Bit (Z)

The Zero Bit (Z) is set to logic 1 by the CPU during any data movement or calculation which sets all 8 bits of the result to zero. This bit is cleared to logic 0 when the resultant 8 bits of a data movement or calculation operation are not all zero. The R6500 instruction set contains no instruction to specifically set or clear the Zero Bit. The Zero Bit is, however, affected by the following instructions; ADC, AND, ASL, BIT, CMP, CPX, CPY, DEC, DEX, DEY, EOR, INC, INX, INY, LDA, LDX, LDY, LSR, ORA, PLA, PLP, ROL, ROR, RTI, SBC, TAX, TAY, TXA, TSX, and TYA.

3.8.3 Interrupt Disable Bit (I)

The Interrupt Disable Bit (I) is used to control the servicing of an interrupt request ($\overline{IRQ}$). If the I Bit is reset to logic 0, the $\overline{IRQ}$ signal will be serviced. If the bit is set to logic 1, the $\overline{IRQ}$ signal will be ignored. The CPU will set the Interrupt Disable Bit to logic 1 if a RESET ($\overline{RES}$), $\overline{IRQ}$, or Non-Maskable Interrupt ($\overline{NMI}$) signal is detected.

The I bit is cleared by the Clear Interrupt Mask Instruction (CLI) and is set by the Set Interrupt Mask Instruction (SEI). This bit is set by the BRK Instruction. The Return from Interrupt (RTI) and Pull Processor Status (PLP) instructions will also affect the I bit.

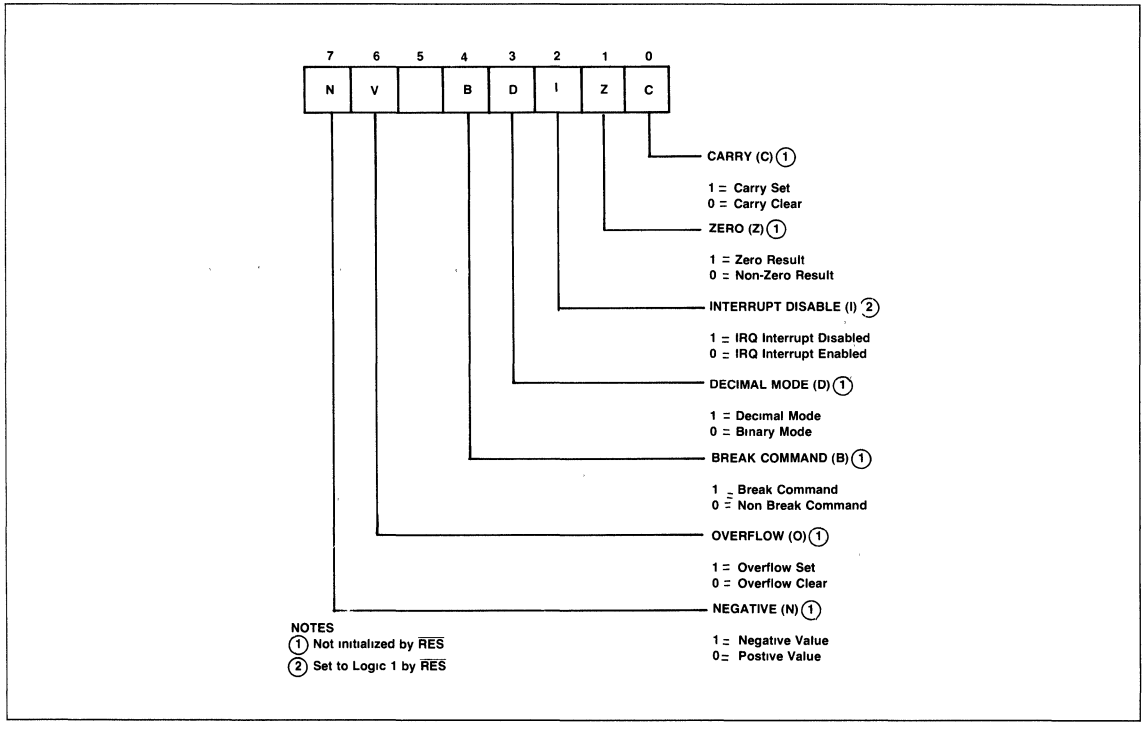


Figure 3-7. Processor Status Register

3.8.4 Decimal Mode Bit (D)

The Decimal Mode Bit (D), is used to control the arithmetic mode of the CPU. When this bit is set to logic 1, the adder operates as a decimal adder. When this bit is cleared to logic 0, the adder operates as a straight binary adder. The adder mode is controlled only by the programmer. The Set Decimal Mode (SED) instruction will set the D bit; the Clear Decimal Mode (CLD) instruction will clear it. The PLP and RTI instructions also effect the Decimal Mode Bit.

CAUTION

The Decimal Mode Bit will either set or clear in an unpredictable manner upon power application. This bit must be initialized to the desired state by the user program or erroneous results may occur.

3.8.5 Break Bit (B)

The Break Bit (B) is used to determine the condition which caused the $\overline{IRQ}$ service routine to be entered. If the $\overline{IRQ}$ service routine was entered because the CPU executed a BRK command, the Break Bit will be set to logic 1. If the $\overline{IRQ}$ routine was entered as the result of an $\overline{IRQ}$ signal being generated, the B bit will be cleared to logic 0. There are no instructions which can set or clear this bit.

3.8.6 Overflow Bit (V)

The Overflow Bit (V) is used to indicate that the result of a signed, binary addition, or subtraction, operation is a value that cannot be contained in seven bits ($-128 \leq n \leq 127$). This indicator only has meaning when signed arithmetic (sign and seven magnitude bits) is performed. When the ADC or SBC instruction is performed, the Overflow Bit is set to logic 1 if the polarity of the sign bit (bit 7) is changed because the result exceeds +127 or −128; otherwise the bit is cleared to logic 0. The V bit may also be cleared by the programmer using a Clear Overflow (CLV) instruction.

The Overflow Bit may also be used with the BIT instruction. The BIT instruction which may be used to sample interface devices, allows the overflow flag to reflect the condition of bit 6 in the sampled field. During a BIT instruction the Overflow Bit is set equal to the content of the bit 6 on the data tested with BIT instruction. When used in this mode, the overflow has nothing to do with signed arithmetic, but is just another sense bit for the microprocessor. Instructions which affect the V flag are ADC, BIT, CLV, PLP, RTI and SBC.

3.8.7 Negative Bit (N)

The Negative Bit (N) is used to indicate that the sign bit (bit 7), in the resulting value of a data movement or data arithmetic operation, is set to logic 1. If the sign bit is set to logic 1, the resulting value of the data movement or arithmetic operation is negative; if the sign bit is cleared, the result of the data movement or arithmetic operation is positive. There are no instructions that set or clear the Negative Bit since the Negative Bit represents only the status of a result. The instructions that effect the state of the Negative Bit are: ADC, AND, ASL, BIT, CMP, CPX, CPY, DEC, DEX, DEY, EOR, INC, INX, INY, LDA, LDX, LDY, LSR, ORA, PLA, PLP, ROL, ROR, RTI, SBC, TAX, TAY, TSX, TXA, and TYA.

SECTION 4
PARALLEL INPUT/OUTPUT PORTS

The R6500/11 or R6500/15 has 32 I/O lines grouped into four 8-bit ports (PA, PB, PC, and PD). Ports A through C may be used either for input or output individually or in groups of any combination. Port D may be used as all inputs or all outputs.

The R6500/12 or R6500/16, a 64 pin QUIP device, has three additional ports: PE, PF and PG. PE is outputs only; PF and PG are bidirectional.

Multifunction I/O's such as Port A and Port C are protected from normal port I/O instructions when they are programmed to perform a multiplexed function.

Internal pull-up resistors (FET's with an impedance range of $3K \leq Rpu \leq 12K$ ohm) may be provided on all port pins except Port D and E as a mask option.

The direction of the I/O lines are controlled by four 8-bit port registers located in page zero. This arrangement provides quick programming access using simple two-byte zero page address instructions. There are no direction registers associated with the I/O ports, which simplifies I/O handling. The I/O addresses are shown in Table 4-1. Section E.6 shows the I/O Port Timing.

Table 4-1. I/O Port Addresses

Port	Address
A	0000
B	0001
C	0002
D	0003
E	0004
F	0005
G	0006

4.1 INPUTS

Inputs for Ports A, B, and C and also Ports F and G of the R6500/12 or R6500/16 are enabled by loading logic 1 into all I/O port register bit positions that are to correspond to I/O input lines. A low (<0.8V) input signal will cause a logic 0 to be read when a read instruction is issued to the port register. A high (>2.0V) input will cause a logic 1 to be read. An RES signal forces all I/O port registers to logic 1 thus initially treating all I/O lines as inputs.

Port D may only be all inputs or all outputs. All inputs is selected by setting bit 5 of the Mode Control Register (MCR5) to a "0".

The status of the input lines can be interrogated at any time by reading the I/O port addresses. Note that this will return the actual status of the input lines, not the data written into the I/O port registers.

Read/Modify/Write instructions can be used to modify the operation of PA, PB, PC, & PD and also ports PF and PG of the R6500/12. During the Read cycle of a Read/Modify/Write instruction the Port I/O register is read. For all other read instructions the port input lines are read. Read/Modify/Write instructions are: ASL, DEC, INC, LSR, RMB, ROL, ROR, and SMB.

4.2 OUTPUTS

Outputs for Ports A thru D and Ports E thru G of the R6500/12 or R6500/16 are controlled by writing the desired I/O line output states into the corresponding I/O port register bit positions. A logic 1 will force a high (>2.4V) output while a logic 0 will force a low (<0.4V) output.

Port D all outputs is selected by setting MCR5 to a "1".

Port E is always all outputs.

4.3 PORT A (PA)

Port A can be programmed via the Mode Control Register (MCR) and the Serial Communications Control Register (SCCR) as a standard parallel 8-bit, bit independent, I/O port or as serial channel I/O lines, counter I/O lines, or an input data strobe for the Port B input latch option. Table 4-2 tabulates the control and usage of Port A.

In addition to their normal I/O functions, PA0 and PA1 can detect positive going edges, and PA2 and PA3 can detect negative going edges. A proper transition on these pins will set a corresponding status bit in the IFR and generate an interrupt request if the respective Interrupt Enable Bit is set. The maximum rate at which an edge can be detected is one-half the 02 clock rate. Edge detection timing is shown in Section E.5.

Table 4-2. Port A Control & Usage

PA0 (2)	PA0 I/O		PORT B LATCH MODE	
	MCR4 = 0		MCR4 = 1	
	SIGNAL		SIGNAL	
	NAME	TYPE	NAME	TYPE
	PA0	I/O	PORT B LATCH STROBE	INPUT (1)
PA1 (2) **PA2 (3)** **PA3 (3)**	PA1–PA3 I/O			
	SIGNAL			
	NAME	TYPE		
	PA1 PA2 PA3	I/O I/O I/O		
PA4	PA4 I/O		COUNTER A I/O	
	MCR0 = 0 MCR1 = 0 SCCR7 = 0 RCVR S/R MODE = 0 (4) (5)		MCR0 = 1 MCR1 = 0 SCCR7 = 0 RCVR S/R MODE = 0 (4)	SCCR7 = 0 SCCR6 = 0 MCR1 = 1
	SIGNAL		SIGNAL	SIGNAL
	NAME	TYPE	NAME TYPE	NAME TYPE
	PA4	I/O	CNTA OUTPUT	CNTA INPUT (1)
	SERIAL I/O SHIFT REGISTER CLOCK			
	SCCR7 = 1 SCCR5 = 1		RCVR S/R MODE = 1 (4)	
	SIGNAL		SIGNAL	
	NAME	TYPE	NAME	TYPE
	XMTR CLOCK	OUTPUT	RCVR CLOCK	INPUT (1)
PA5	PA5 I/O		COUNTER B I/O	
	MCR3 = 0 MCR2 = 0		MCR3 = 0 MCR2 = 1	MCR3 = 1 MCR2 = X
	SIGNAL		SIGNAL	SIGNAL
	NAME	TYPE	NAME TYPE	NAME TYPE
	PA5	I/O	CNTB OUTPUT	CNTB INPUT (1)
PA6	PA6 I/O		SERIAL I/O XMTR OUTPUT	
	SCCR7 = 0		SCCR7 = 1	
	SIGNAL		SIGNAL	
	NAME	TYPE	NAME TYPE	
	PA6	I/O	XMTR OUTPUT	
PA7	PA7 I/O		SERIAL I/O RCVR INPUT	
	SCCR6 = 0		SCCR6 = 1	
	SIGNAL		SIGNAL	
	NAME	TYPE	NAME TYPE	
	PA7	I/O	RCVR INPUT (1)	

Notes:
(1) Hardware Buffer Float
(2) Positive Edge Detect
(3) Negative Edge Detect
(4) RCVR S/R Mode = 1 when SCCR6 • $\overline{\text{SCCR5}}$ • SCCR4 = 1
(5) For the following mode combinations PA4 is available as an input only pin:
$\overline{\text{SCCR7}}$•SCCR6•$\overline{\text{SCCR5}}$•MCR1
+ $\overline{\text{SCCR7}}$•SCCR6•$\overline{\text{SCCR4}}$•MCR1
+ SCCR7•$\overline{\text{SCCR6}}$•$\overline{\text{SCCR5}}$
+ SCCR7•$\overline{\text{SCCR5}}$•$\overline{\text{SCCR4}}$•

4.4 PORT B (PB)

Port B can be programmed as an 8 bit, bit independent I/O port. It has a latched input capability which may be enabled or disabled via the Mode Control Register (MCR). Table 4-3 tabulates the control and usage of Port B. An Input Data Strobe signal must be provided thru PA0 when Port B is programmed to be used with latched input option. Input data latch timing for Port B is shown in Section E.5.

Table 4-3. Port B Control & Usage

Pin Name	I/O Mode MCR4 = 0 Signal Name	I/O Mode MCR4 = 0 Signal Type (1)	Latch Mode MCR4 = 1 (2) Signal Name	Latch Mode MCR4 = 1 (2) Signal Type
PB0	PB0	I/O	PB0	INPUT
PB1	PB1	I/O	PB1	INPUT
PB2	PB2	I/O	PB2	INPUT
PB3	PB3	I/O	PB3	INPUT
PB4	PB4	I/O	PB4	INPUT
PB5	PB5	I/O	PB5	INPUT
PB6	PB6	I/O	PB6	INPUT
PB7	PB7	I/O	PB7	INPUT

(1) Resistive pull-up, active buffer pull down
(2) Input data is stored in port B latch by PA0 pulse

4.5 PORT C (PC)

Port C can be programmed as an I/O port and in conjunction with Port D, as an abbreviated bus, or as a multiplexed bus. When used in the abbreviated or multiplexed bus modes, PC0-PC7 function as A0-A3, A12, R/W, A13, and $\overline{EMS}$, respectively, as shown in Table 4-4. $\overline{EMS}$ (External Memory Select) is asserted (low) whenever the internal processor accesses memory area between 0100 and 3FFF. (See Memory Map, Appendix B). The leading edge of $\overline{EMS}$ may be used to strobe the eight address lines multiplexed on Port D in the Multiplexed Bus Mode. See Appendix E.3 through E.5 for Port C timing.

4.6 PORT D (PD)

Port D can be programmed as an I/O Port, an 8-bit tri-state data bus, or as a multiplexed bus. Mode selection for Port D is made by the Mode Control Register (MCR). The Port D output drivers can be selected as tri-state drivers by setting bit 5 of the MCR to 0 (zero). Table 4-5 shows the necessary settings for the MCR to achieve the various modes for Port D. When Port D is selected to operate in the Abbreviated Mode PD0-PD7 serves as data register bits D0-D7. When Port D is selected to operate in the Multiplexed Mode data bits D0 through D7 are time multiplexed with address bits A4 through A11, respectively. Refer to the Memory Maps (Appendix C) for Abbreviated and Multiplexed memory assignments. See Appendix E.3 through E.5 for Port D timing.

4.7 PORT E, PORT F AND PORT G (PE, PF & PG) R6500/12 OR /16 ONLY

Port E only operates in the Output mode. It provides a Darlington output that can source current at the high (1) level. Port F and Port G operate identically and can be programmed as bidirectional I/O ports. They have standard output capability. See Appendix E.5 for Port E, F & Port G timing.

Table 4-4. Port C Control and Usage

Pin Name	I/O Mode MCR7 = 0 MCR6 = X Signal Name	I/O Mode Type (1)	Abbreviated Mode MCR7 = 1 MCR6 = 0 Signal Name	Abbreviated Mode Type (2)	Multiplexed Mode MCR7 = 1 MCR6 = 1 Signal Name	Multiplexed Mode Type (2)
PC0	PC0	I/O	A0	OUTPUT	A0	OUTPUT
PC1	PC1	I/O	A1	OUTPUT	A1	OUTPUT
PC2	PC2	I/O	A2	OUTPUT	A2	OUTPUT
PC3	PC3	I/O	A3	OUTPUT	A3	OUTPUT
PC4	PC4	I/O	A12	OUTPUT	A12	OUTPUT
PC5	PC5	I/O	RW	OUTPUT	RW	OUTPUT
PC6	PC6	I/O	A13	OUTPUT	A13	OUTPUT
PC7	PC7	I/O	EMS	OUTPUT	EMS	OUTPUT

(1) Resistive Pull-Up, Active Buffer Pull-Down
(2) Active Buffer Pull-Up and Pull-Down

Table 4-5. Port D Control and Usage

Pin Name	I/O Modes MCR7 = 0 MCR6 = X MCR5 = 0 Signal Name	Type (1)	I/O Modes MCR7 = 0 MCR6 = X MCR5 = 1 Signal Name	Type (2)	Abbreviated Mode MCR7 = 1 MCR6 = 0 MCR5 = 1 Signal Name	Type (3)	Multiplexed Mode MCR7 = 1 MCR5 = 1 MCR5 = 1 Signal Phase 1 Name	Type (2)	Signal Phase 2 Name	Type (3)
PD0	PD0	INPUT	PD0	OUTPUT	DATA0	I/O	A4	OUTPUT	DATA0	I/O
PD1	PD1	INPUT	PD1	OUTPUT	DATA1	I/O	A5	OUTPUT	DATA1	I/O
PD2	PD2	INPUT	PD2	OUTPUT	DATA2	I/O	A6	OUTPUT	DATA2	I/O
PD3	PD3	INPUT	PD3	OUTPUT	DATA3	I/O	A7	OUTPUT	DATA3	I/O
PD4	PD4	INPUT	PD4	OUTPUT	DATA4	I/O	A8	OUTPUT	DATA4	I/O
PD5	PD5	INPUT	PD5	OUTPUT	DATA5	I/O	A9	OUTPUT	DATA5	I/O
PD6	PD6	INPUT	PD6	OUTPUT	DATA6	I/O	A10	OUTPUT	DATA6	I/O
PD7	PD7	INPUT	PD7	OUTPUT	DATA7	I/O	A11	OUTPUT	DATA7	I/O

(1) Tri-State Buffer is in High Impedance Mode
(2) Tri-State Buffer is in Active Mode
(3) Tri-State Buffer is in Active Mode Only During the Phase 2 Portion of a Write Cycle

SECTION 5
SERIAL INPUT/OUTPUT CHANNEL

The device provides a full duplex Serial I/O channel with programmable bit rates and operating modes. The serial I/O functions are controlled by the Serial Communication Control Register (SCCR). The SCCR bit assignment is shown in Figure 5-1. The serial bit rate is determined by Counter A for all modes except the Receiver Shift Register (RCVR S/R) mode for which an external shift clock must be provided. The maximum data rate using the internal clock is 62.5K bits per second (@ ∅2 = 1 MHz). The transmitter (XMTR) and receiver (RCVR) can be independently programmed to operate in different modes and can be independently enabled or disabled.

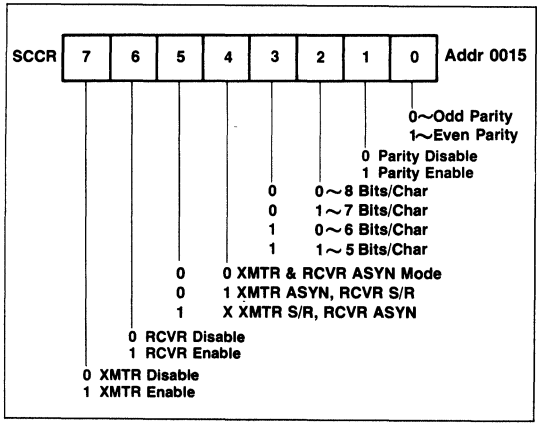


Figure 5-1. Serial Communication Control Register

Except for the Receiver Shift Register Mode (RCVR S/R), all XMTR and RCVR bit rates will occur at one sixteenth of the Counter A interval timer rate. Counter A is forced into an interval timer mode whenever the serial I/O is enabled in a mode requiring an internal clock.

Whenever Counter A is required as a timing source it must be loaded with the hexadecimal code that selects the data rate for the serial I/O Port. Refer to Counter A (paragraph 6.1) for a table of hexadecimal values to represent the desired data rate.

5.1 TRANSMITTER OPERATION (XTMR)

The XTMR operation and the transmitter related control/status functions are enabled by bit 7 of the Serial Communications Control Register (SCCR). The transmitter, when in the Asynchronous (ASYN) mode, automatically adds a start bit, one or two stop bits, and, when enabled, a parity bit to the transmitted data. A word of transmitted data (in asynchronous parity mode) can have 5, 6, 7, or 8 bits of data. The nine data modes are in Figure 5-2. When parity is disabled, the 5, 6, 7 or 8 bits of data are terminated with two stop bits.

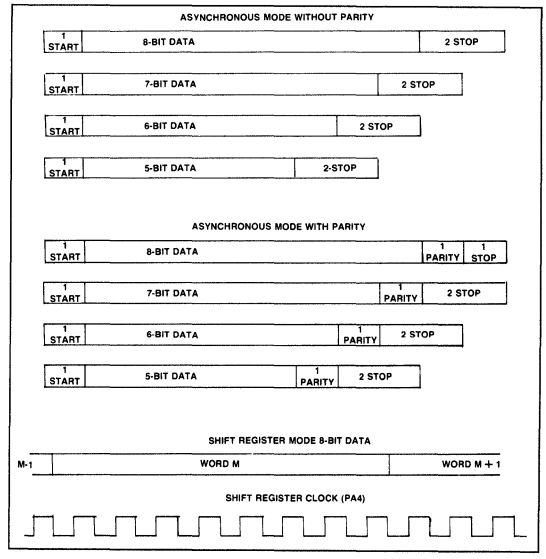


Figure 5-2. Transmitted Data Modes

In the S/R mode, eight data bits are always shifted out. Bits/character and parity control bits are ignored. The serial data is shifted out via the SO output (PA6) and the shift clock is available at the CA (PA4) pin. When the transmitter underruns in the S/R mode the SO output and shift clock are held in a high state.

The XMTR Interrupt Flag bit (IFR7) is controlled by Serial Communication Status Register bits SCSR5, SCSR6 and SCSR7.

$$IFR7 = SCSR6\ (\overline{SCSR5} + SCSR7)$$

5.2 RECEIVER OPERATION (RCVR)

The receiver and its selected control and status functions are enabled when SCCR-6 is set to a "1." In the ASYN mode, data format must have a start bit, appropriate number of data bits, a parity bit (if enabled) and one stop bit. Refer to paragraph 5.1 for a diagram of bit allocations. The receiver bit period is divided into 8 sub-intervals for internal synchronization. The receiver bit stream is synchronized by the start bit and a strobe signal is generated at the approximate center of each incoming bit. Refer to Figure 5-3 for ASYN Receive Data Timing. The character assembly process does not start if the start bit signal is less than one-half the bit time after a low level is detected on the Receive Data Input. Framing error, over-run, and parity error conditions or a RCVR Data Register Full will set the appropriate status bits, and any of the above conditions will cause an Interrupt Request if the Receiver Interrupt Enable bit is set to logic 1.

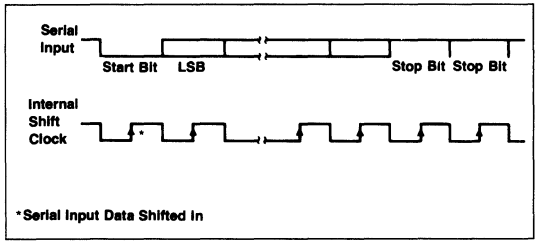


Figure 5-3. ASYN Receive Data Timing

In the S/R mode, an external shift clock must be provided at CA (PA4) pin along with 8 bits of serial data (LSB first) at the SI input (PA7). The maximum data rate using an external shift clock is one-eighth the internal clock rate. Refer to Figure 5-4 for S/R Mode Timing.

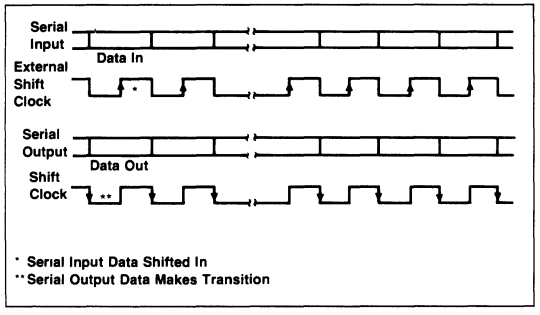


Figure 5-4. S/R Mode Timing

A RCVR interrupt (IFR6) is generated whenever any of SCSR0-3 are true.

5.3 SERIAL COMMUNICATION STATUS REGISTER (SCSR)

The Serial Communication Status Register (SCSR) holds information on various communication error conditions, status of the transmitter and receiver data registers, a transmitter end-of-transmission condition, and a receiver idle line condition (Wake-Up Feature). The SCSR bit assignment is shown in Figure 5-5. Bit assignments and functions of the SCSR are as follows:

SCSR0: *Receiver Data Register Full*—Set to a logic 1 when a character is transferred from the Receiver Shift Register to the Receiver Data Register. This bit is cleared by reading the Receiver Data Register, or by $\overline{RES}$ and is disabled if SCCR6 = 0. The SCSR 0 bit will not be set to a logic 1 if the received data contains an error condition, instead, a corresponding error bit will be set to a logic 1.

SCSR 1: *Over-Run Error*—Set to a logic 1 when a new character is transferred from the Receiver Shift Register, with the last character still in the Receiver Data Register. This bit is cleared by reading the Receiver Data Register, or by $\overline{RES}$.

SCSR 2: *Parity Error*—Set to logic 1 when the RCVR is in the ASYN Mode, Parity Enable bit is set, and the received data has a parity error. This bit is cleared by reading the Receiver Data Register or by $\overline{RES}$.

SCSR 3: *Framing Error*—Set to a logic 1 when the received data contains a zero bit after the last data or parity bit in the stop bit slot. Cleared by reading the Receiver Data Register or by $\overline{RES}$. (ASYN Mode only).

SCSR 4: *Wake-Up*—Set to a logic 1 by writing a "1" in bit 4 of address: 0016. The Wake-Up bit is cleared by $\overline{RES}$ or when the receiver detects a string of ten consecutive 1's. When the Wake-Up bit is set SCSR0 through SCSR3 are inhibited.

SCSR 5: *End of Transmission*—Set to a logic 1 by writing a "1" in bit position 5 of address: 0016. The End of Transmission bit is cleared by $\overline{RES}$ or upon writing a new data word into the Transmitter Data Register. When the End-of-Transmission bit is true the Transmitter Register Empty bit is disabled until a Transmitter Under-Run occurs.

SCSR 6: *Transmitter Data Register Empty*—Set to a logic 1 when the contents of the Transmitter Data Register is transferred to the Transmitter Shift Register. Cleared upon writing new data into the Transmit Data Register. This bit is initialized to a logic 1 by $\overline{RES}$.

SCSR 7: *Transmitter Under-Run*—Set to a logic 1 when the last data bit is transmitted if the transmitter is in a S/R Mode or when the last stop bit is transmitted if the XMTR is in the ASYN Mode while the Transmitter Data Register Empty Bit is set. Cleared by a transfer of new data into the Transmitter Shift Register, or by $\overline{RES}$.

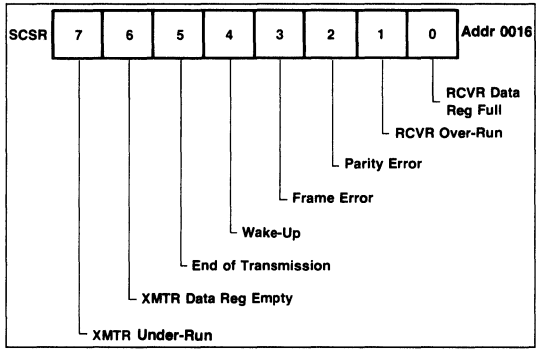


Figure 5-5. SCSR Bit Allocation

5.4 WAKE-UP FEATURE

In a multi-distributed microprocessor or microcomputer applications, a destination address is usually included at the beginning of the message. The Wake-Up Feature allows non-selected CPU's to ignore the remainder of the message until the beginning of the next message by setting the Wake-Up bit. As long as the Wake-Up flag is true, the Receiver Data Register Full Flag remains false. The Wake-Up bit is automatically cleared when the receiver detects a string of eleven consecutive 1's which indicates an idle transmit line. When the next byte is received, the Receiver Data Register Full Flag signals the CPU to wake-up and read the received data.

SECTION 6
COUNTER/TIMERS

The device contains two 16-bit counters (Counter A and Counter B) and three 16-bit latches associated with the counters. Counter A has one 16-bit latch and Counter B has two 16-bit latches. Each counter can be independently programmed to operate in one of four modes:

Counter A	Counter B
• Pulse width measurement	• Retriggerable Interval Counter
• Pulse Generation	• Asymmetrical Pulse Generation
• Interval Timer	• Interval Timer
• Event Counter	• Event Counter

Operating modes of Counter A and Counter B are controlled by the Mode Control Register. All counting begins at the initialization value and decrements. When modes are selected requiring a counter input/output line, PA4 is automatically selected for Counter A and PA5 is automatically selected for Counter B (see Table 4.2).

6.1 COUNTER A

Counter A consists of a 16-bit counter and a 16-bit latch organized as follows: Lower Counter A (LCA), Upper Counter A (UCA), Lower Latch A (LLA), and Upper Latch A (ULA). The counter contains the count of either Ø2 clock pulses or external events, depending on the counter mode selected. The contents of Counter A may be read any time by executing a read at location 0019 for the Upper Counter A and at location 001A or location 0018 for the Lower Counter A. A read at location 0018 also clears the Counter A Underflow Flag (IFR4).

The 16-bit latch contains the counter initialization value, and can be loaded at any time by executing a write to the Upper Latch A at location 0019 and the Lower Latch A at location 0018. In either case, the contents of the accumulator are copied into the applicable latch register.

Counter A can be started at any time by writing to address. 001A. The contents of the accumulator will be copied into the Upper Latch A before the contents of the 16-bit latch are transferred to Counter A. Counter A is set to the latch value whenever Counter A underflows. When Counter A decrements from 0000 the next counter value will be the latch value, not FFFF, and the Counter A Underflow Flag (IFR 4) will be set to "1". This bit may be cleared by reading the Lower Counter A at location 0018, by writing to address location 001A, or by $\overline{RES}$.

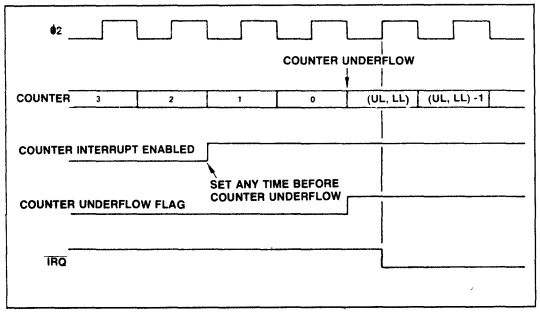


Figure 6-1. Interval Timer Timing Diagram

Counter A operates in any of four modes. These modes are selected by the Counter A Mode Control bits in the Control Register.

MCR1 (bit 1)	MCR0 (bit 0)	Mode
0	0	Interval Timer
0	1	Pulse Generation
1	0	Event Counter
1	1	Pulse Width Measurement

The Interval Timer, Pulse Generation, and Pulse Width Measurement Modes are Ø2 clock counter modes. The Event Counter Mode counts the occurrences of an external event on the CNTR line.

The Counter is set to the Interval Timer Mode (00) when a $\overline{RES}$ signal is generated.

6.1.1 Interval Timer

In the Interval Timer mode the Counter is initialized to the Latch value by either of two conditions:

1. When the Counter is decremented from 0000, the next Counter value is the Latch value (not FFFF).

2. When a write operation is performed to the Load Upper Latch and Transfer Latch to Counter address 001A, the Counter is loaded with the Latch value. Note that the contents of the Accumulator are loaded into the Upper Latch before the Latch value is transferred to the Counter.

The Counter value is decremented by one count at the Ø2 clock rate. The 16-bit Counter can hold from 1 to 65535 counts. The Counter Timer capacity is therefore 1μs to 65,535 ms at the 1 MHz Ø2 clock rate or 0.5 μs to 32.767 ms at the 2 MHz Ø2 clock rate. Time intervals greater than the maximum Counter value can be easily measured by counting $\overline{IRQ}$ interrupt requests in the counter $\overline{IRQ}$ interrupt routine.

When Counter A decrements from 0000, the Counter A Underflow (IFR4) is set to logic 1. If the Counter A Interrupt Enable Bit (IER4) is also set, an $\overline{IRQ}$ interrupt request will be generated. The Counter A Underflow bit in the Interrupt Flag Register can be examined in the $\overline{IRQ}$ interrupt routine to determine that the $\overline{IRQ}$ was generated by the Counter A Underflow.

While the timer is operating in the Interval Timer Mode, PA4 operates as a PA I/O bit.

A timing diagram of the Interval Timer Mode is shown in Figure 6-1.

6.1.2 Pulse Generation Mode

In the Pulse Generation mode, the CA line operates as a Counter Output. The line toggles from low to high or from high to low whenever a Counter A Underflow occurs, or a write is performed to address 001A.

The normal output waveform is a symmetrical square-wave. The CA output is initialized high when entering the mode and transitions low when writing to 001A.

Asymmetric waveforms can be generated if the value of the latch is changed after each counter underflow.

A one-shot waveform can be generated by changing from Pulse Generation to Interval Timer mode after only one occurrence of the output toggle condition.

6.1.3 Event Counter Mode

In this mode the CA is used as an Event Input line, and the Counter will decrement with each rising edge detected on this line. The maximum rate at which this edge can be detected is one-half the ϕ2 clock rate.

The Counter can count up to 65,535 occurrences before underflowing. As in the other modes, the Counter A Underflow bit (IER4) is set to logic 1 if the underflow occurs.

Figure 6.2 is a timing diagram of the Event Counter Mode.

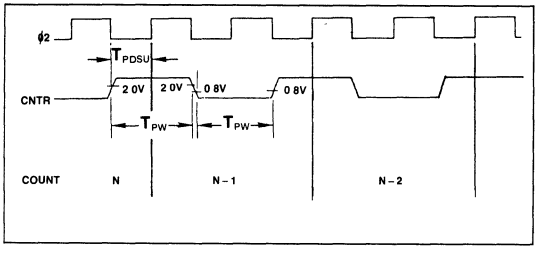


Figure 6-2. Event Counter Mode

6.1.4 Pulse Width Measurement Mode

This mode allows the accurate measurement of a low pulse duration on the CA line. The Counter decrements by one count at the ϕ2 clock rate as long as the CA line is held in the low state. The Counter is stopped when CA is in the high state.

The Counter A underflow flag will be set only when the count in the timer reaches zero. Upon reaching zero the timer will be loaded with the latch value and continue counting down as long as the CA pin is held low. After the counter is stopped by a high level on CA, the count will hold as long as CA remains high. Any further low levels on CA will again cause the counter to count down from its present value. The state of the CA line can be determined by testing the state of PA4.

A timing diagram for the Pulse Width Measurement Mode is shown in Figure 6.3.

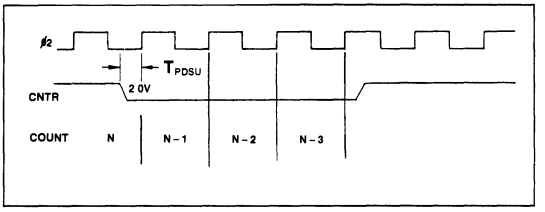


Figure 6-3. Pulse Width Measurement

6.1.5 Serial I/O Data Rate Generation

Counter A also provides clock timing for the Serial I/O which establishes the data rate for the Serial I/O port. When the Serial I/O is enabled, Counter A is forced to operate at the internal clock rate. Counter A is not required for the RCVR S/R mode. The Counter I/O (PA4) may also be required to support the Serial I/O (see Table 4-2).

Table 6-1 identifies the values to be loaded in Counter A for selecting standard data rates with a ϕ2 clock rate of 1 MHz and 2 MHz. Although Table 6-1 identifies only the more common data rates, any data rate from 1 to 62.5K bps can be selected by using the formula:

$$N = \frac{\phi 2}{16 \times bps} - 1$$

where

- N = decimal value to be loaded into Counter A using its hexadecimal equivalent.
- ϕ2 = the clock frequency (1 MHz or 2 MHz)
- bps = the desired data rate.

NOTE

In Table 6-1 you will notice that the standard data rate and the actual data rate may be slightly different. Transmitter and receiver errors of 1.5% or less are acceptable. A revised clock rate is included in Table 6-1 for those baud rates which fall outside this limit.

Table 6-1. Counter A Values for Baud Rate Selection

Standard Baud Rate	Hexadecimal Value		Actual Baud Rate At		Clock Rate Needed To Get Standard Baud Rate	
	1 MHz	2 MHz	1 MHz	2 MHz	1 MHz	2 MHz
50	04E1	09C3	50.00	50.00	1.0000	2.0000
75	0340	0682	75.03	74.99	1.0000	2.0000
110	0237	046F	110.04	110.04	1.0000	2.0000
150	01A0	0340	149.88	150.06	1.0000	2.0000
300	00CF	01A0	300.48	299.76	1.0000	2.0000
600	0067	00CF	600.96	600.96	1.0000	2.0000
1200	0033	0067	1201.92	1201.92	1.0000	2.0000
2400	0019	0033	2403.85	2403.85	1.0000	2.0000
3600	0010	0021	3676.47	3676.47	0.9792	1.9584
4800	000C	0019	4807.69	4807.69	1.0000	2.0000
7200	0008	0010	6944.44	7352.94	1.0368	1.9584
9600	0006	000C	8928.57	9615.38	1.0752	2.0000

6.2 COUNTER B

Counter B consists of a 16-bit counter and two 16-bit latches organized as follows: Lower Counter B (LCB), Upper Counter B (UCB), Lower Latch B (LLB), Upper Latch B (ULB), Lower Latch C (LLC), and Upper Latch C (ULC). Latch C is used only in the asymmetrical pulse generation mode. The counter contains the count of either Ø2 clock pulses or external events depending on the counter mode selected. The contents of Counter B may be read any time by executing a read at location 001D for the Upper Counter B and at location 001E or 001C for the Lower Counter B. A read at location 001C also clears the Counter B Underflow Flag.

Latch B contains the counter initialization value, and can be loaded at any time by executing a write to the Upper Latch B at location 001D and the Lower Latch B at location 001C. In each case, the contents of the accumulator are copied into the applicable latch register.

Counter B can be initialized at any time by writing to address: 001E. The contents of the accumulator is copied into the Upper Latch B before the value in the 16-bit Latch B is transferred to Counter B. Counter B will also be set to the latch value and the Counter B Underflow Flag bit (IFR5) will be set to a "1" whenever Counter B underflows by decrementing from 0000.

IFR 5 may be cleared by reading the Lower Counter B at location 001C, by writing to address location 001E, or by $\overline{RES}$.

Counter B operates in the same manner as Counter A in the Interval Timer and Event Counter modes. The Pulse Width Measurement Mode is replaced by the Retriggerable Interval Timer mode and the Pulse Generation mode is replaced by the Asymmetrical Pulse Generation Mode.

6.2.1 Retriggerable Interval Timer Mode

When operating in the Retriggerable Interval Timer mode, Counter B is initialized to the latch value by writing to address 001E, by a Counter B underflow, or whenever a positive edge occurs on the CB pin (PA5). The Counter B interrupt flag will be set if the counter underflows before a positive edge occurs on the CB line. Figure 6-4 illustrates the operation.

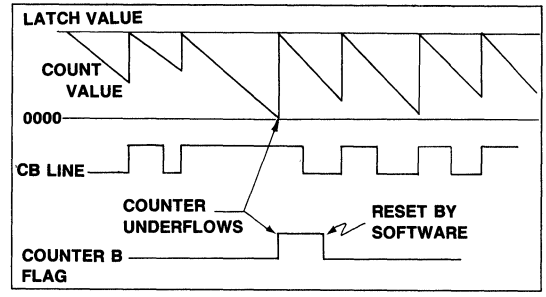


Figure 6-4. Counter B Retriggerable Interval Timer Mode

6.2.2 Asymmetrical Pulse Generation Mode

Counter B has a special Asymmetrical Pulse Generation Mode whereby a pulse train with programmable pulse width and period can be generated without the processor intervention once the latch values are initialized.

In this mode, the 16-bit Latch B is initialized with a value which corresponds to the duration between pulses (referred to as D in the following descriptions). The 16-bit Latch C is initialized with a value which corresponds to the desired pulse width (referred to as P in the following descriptions). The initialization sequence for Latch B and C and the starting of a counting sequence are as follows:

1. The lower 8 bits of P are loaded into LLB by writing to address 001C, and the upper 8 bits of P are loaded into ULB and the full 16 bits are transferred to Latch C by writing to address location 001D. At this point both Latch B and Latch C contain the value of P.

2. The lower 8 bits of D are loaded into LLB by writing to address 001C, and the upper 8 bits of D are loaded into ULB by writing to address location 001E. Writing to address location 001E also causes the contents of the 16-bit Latch B to be downloaded into the Counter B and causes the CB output to go low as shown in Figure 6-5.

3. When the Counter B underflow occurs the contents of the Latch C is loaded into the Counter B, and the CB output toggles to a high level and stays high until another underflow occurs. Latch B is then down-loaded and the CB output toggles to a low level repeating the whole process.

SECTION 7
POWER ON/INITIALIZATION CONSIDERATIONS

7.1 POWER-ON TIMING

After applications of V_{CC} and V_{RR} power to the device, $\overline{RES}$ must be held low for at least eight Ø2 clock cycles after V_{CC} reaches operating range and the interal oscillator has stabilized. This stabilization time is dependent upon the input V_{CC} voltage and performance of the internal oscillator. The clock can be monitored at Ø2 (pin 3). Figure 7-1 illustrates the power turn-on waveforms. Clock stabilization time is typically 20 ms.

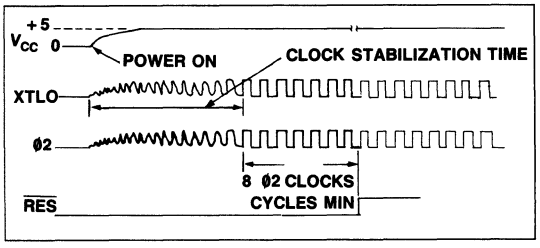


Figure 7-1. Power Turn-on Timing Detail

7.2 POWER-ON RESET

The occurrence of $\overline{RES}$ going from low to high will cause the device to set the Interrupt Mask Bit — bit 2 of the Processor Status Register — and initiate a reset vector fetch at address FFFC and FFFD to begin user program execution. All of the I/O ports (PA, PB, PC, PD) will be forced to the high (logic 1) state. All bits of the Control Register will be cleared to logic 0 causing the Interval Timers counter mode (mode 00) to be selected and causing all interrupt enabled bits to be reset.

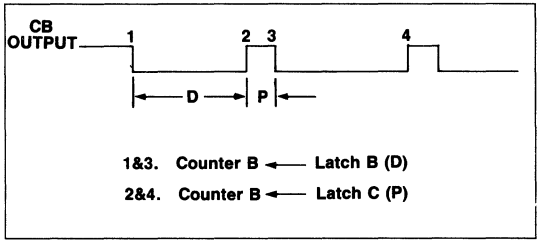


Figure 6-5. Counter B Pulse Generation

7.3 RESET ($\overline{RES}$) CONDITIONING

When $\overline{RES}$ is driven from low to high the device is put in a reset state causing the registers and I/O ports to be configured as shown in Table 7-1.

Table 7-1. $\overline{RES}$ Initialization of I/O Ports and Registers

	7	6	5	4	3	2	1	0
Registers								
Processor Status	—	—	—	—	—	1	—	—
Mode Control (MCR)	0	0	0	0	0	0	0	0
Int. Enable (IER)	0	0	0	0	0	0	0	0
Int Flag (IFR)	0	0	0	0	0	0	0	0
Ser. Com. Control (SCCR)	0	0	0	0	0	0	0	0
Ser. Com. Status (SCSR)	0	1	0	0	0	0	0	0
Ports								
PA Latch	1	1	1	1	1	1	1	1
PB Latch	1	1	1	1	1	1	1	1
PC Latch	1	1	1	1	1	1	1	1
PD Latch	1	1	1	1	1	1	1	1

All RAM and other CPU registers will initialize in a random, non-repeatable data pattern.

7.4 INITIALIZATION

Any initialization process for the device should include a $\overline{RES}$, as indicated in the preceding paragraphs. After stabilization of the internal clock (if a power on situation) an initialization subroutine should be executed to perform (as a minimum) the following functions:

1. The Stack Pointer should be set
2. Clear or Set Decimal Mode
3. Set or Clear Carry Flag
4. Set up Mode Controls as required
5. Clear Interrupts

A typical initialization subroutine could be as follows:

LDX	Load stack pointer starting address into X Register
TXS	Transfer X Register value to Stack Pointer
CLD	Clear Decimal Mode
SEC	Set Carry Flag
.	Set-up Mode Control and
. . . .	special function
. . . .	registers as required
CLI	Clear Interrupts

APPENDIX A
ENHANCED R6502 INSTRUCTION SET

This appendix contains a summary of the R6502 instruction set. For detailed information, consult the R6502 Microcomputer System Programming Manual, Order No. 202. The four instructions notated with a * are added instructions to enhance the standard 6502 instruction set.

A.1 INSTRUCTION SET IN ALPHABETIC SEQUENCE

ADC	Add Memory to Accumulator with Carry
AND	"AND" Memory with Accumulator
ASL	Shift Left One Bit (Memory or Accumulator)
*BBR	Branch on Bit Reset Relative
*BBS	Branch on Bit Set Relative
BCC	Branch on Carry Clear
BCS	Branch on Carry Set
BEQ	Branch on Result Zero
BIT	Test Bits in Memory with Accumulator
BMI	Branch on Result Minus
BNE	Branch on Result not Zero
BPL	Branch on Result Plus
BRK	Force Break
BVC	Branch on Overflow Clear
BVS	Branch on Overflow Set
CLC	Clear Carry Flag
CLD	Clear Decimal Mode
CLI	Clear Interrupt Disable Bit
CLV	Clear Overflow Flag
CMP	Compare Memory and Accumulator
CPX	Compare Memory and Index X
CPY	Compare Memory and Index Y
DEC	Decrement Memory by One
DEX	Decrement Index X by One
DEY	Decrement Index Y by One
EOR	"Exclusive-Or" Memory with Accumulator
INC	Increment Memory by One
INX	Increment Index X by One
INY	Increment Index Y by One
JMP	Jump to New Location
JSR	Jump to New Location Saving Return Address
LDA	Load Accumulator with Memory
LDX	Load Index X with Memory
LDY	Load Index Y with Memory
LSR	Shift One Bit Right (Memory or Accumulator)
NOP	No Operation
ORA	"OR" Memory with Accumulator
PHA	Push Accumulator on Stack
PHP	Push Processor Status on Stack
PLA	Pull Accumulator from Stack
PLP	Pull Processor Status from Stack
*RMB	Reset Memory Bit
ROL	Rotate One Bit Left (Memory or Accumulator)
ROR	Rotate One Bit Right (Memory or Accumulator)
RTI	Return from Interrupt
RTS	Return from Subroutine
SBC	Subtract Memory from Accumulator with Borrow
SEC	Set Carry Flag
SED	Set Decimal Mode
SEI	Set Interrupt Disable Status
*SMB	Set Memory Bit
STA	Store Accumulator in Memory
STX	Store Index X in Memory
STY	Store Index Y in Memory
TAX	Transfer Accumulator to Index X
TAY	Transfer Accumulator to Index Y
TSX	Transfer Stack Pointer to Index X
TXA	Transfer Index X to Accumulator
TXS	Transfer Index X to Stack Register
TYA	Transfer Index Y to Accumulator

A.2 INSTRUCTION SET SUMMARY TABLE

R6500/11 OR R6500/15 INSTRUCTION SET

INSTRUCTIONS

MNEMONIC	OPERATION	IMMEDIATE OP	n	#	ABSOLUTE OP	n	#	ZERO PAGE OP	n	#	ACCUM OP	n	#	IMPLIED OP	n	#
ADC	A · M C→A (4)(1)	69	2	2	6D	4	3	65	3	2						
AND	A M→A (1)	29	2	2	2D	4	3	25	3	2						
ASL	C← [7 0] ←0				0E	6	3	06	5	2	0A	2	1			
BBR[#(0-7)]	Branch on $M_6 = 0$ (5)(2)															
BBS[#(0-7)]	Branch on $M_6 = 1$ (5)(2)															
BCC	Branch on C = 0 (2)															
BCS	Branch on C = 1 (2)															
BEQ	Branch on Z = 1 (2)															
BIT	A∧M				2C	4	3	24	3	2						
BMI	Branch on N = 1 (2)															
BNE	Branch on Z = 0 (2)															
BPL	Branch on N = 0 (2)															
BRK	Break													00	7	1
BVC	Branch on V = 0 (2)															
BVS	Branch on V = 1 (2)															
CLC	0→C													18	2	1
CLD	0→D													D8	2	1
CLI	0→I													58	2	1
CLV	0→V													B8	2	1
CMP	A M (1)	C9	2	2	CD	4	3	C5	3	2						
CPX	X M	E0	2	2	EC	4	3	E4	3	2						
CPY	Y M	C0	2	2	CC	4	3	C4	3	2						
DEC	M 1→M				CE	6	3	C6	5	2						
DEX	X 1→X													CA	2	1
DEY	Y 1→Y													88	2	1
EOR	A∀M→A (1)	49	2	2	4D	4	3	45	3	2						
INC	M 1→M				EE	6	3	E6								
INX	X 1→X													EB	2	1
INY	Y 1→Y													C8	2	1
JMP	Jump to New Loc				4C	3	3									
JSR	Jump Sub				20	6	3									
LDA	M→A (1)	A9	2	2	AD	4	3	A5	3	2						
LDX	M→X (1)	A2	2	2	AE	4	3	A6	3	2						
LDY	M→Y (1)	A0	2	2	AC	4	3	A4	3	2						
LSR	0→ [7 0] →C				4E	6	3	46	5	2	4A	2	1			
NOP	No Operation													EA	2	1
ORA	AVM→A (1)	09	2	2	0D	4	3	05	3	2						
PHA	A→Ms S 1→S													48	3	1
PHP	P→Ms S 1→S													08	3	1
PLA	S 1→S Ms→A													68	4	1
PLP	S 1→S Ms→P													28	4	1
RMB[#(0-7)]	0→M_b (5)															
ROL	[7 0] ← [C]				2E	6	3	26	5	2	2A	2	1			
ROR	[C] → [7 0]				6E	6	3	66	5	2	6A	2	1			
RTI	Rtrn Int													40	6	1
RTS	Rtrn Sub													60	6	1
SBC	A M C→A (1)	E9	2	2	ED	4	3	E5	3	2						
SEC	1→C													38	2	1
SED	1→D													F8	2	1
SEI	1→T													78	2	1
SMB[#(0-7)]	1→M_b (5)															
STA	A→M				8D	4	3	85	3	2						
STX	X→M				8E	4	3	86	3	2						
STY	Y→M				8C	4	3	84	3	2						
TAX	A→X													AA	2	1
TAY	A→Y													A8	2	1
TSX	S→X													BA	2	1
TXA	X→A													8A	2	1
TXS	X→S													9A	2	1
TYA	Y→A													98	2	1

MNEMONIC	(IND, X) OP	n	#	(IND), Y OP	n	#	Z PAGE, X OP	n	#	ABS, X OP	n	#	ABS, Y OP	n	#	RELATIVE OP	n	#	INDIRECT OP	n	#	Z PAGE, Y OP	n	#
ADC	61	6	2	71	5	2	75	4	2	7D	4	3	79	4	3									
AND	21	6	2	31	5	2	35	4	2	3D	4	3	39	4	3									
ASL							16	6	2	1E	7	3												
BBR[#(0-7)]																								
BBS[#(0-7)]																								
BCC																90	2	2						
BCS																B0	2	2						
BEQ																F0	2	2						
BIT																								
BMI																30	2	2						
BNE																D0	2	2						
BPL																10	2	2						
BRK																								
BVC																50	2	2						
BVS																70	2	2						
CLC																								
CLD																								
CLI																								
CLV																								
CMP	C1	6	2	D1	5	2	D5	4	2	DD	4	3	D9	4	3									
CPX																								
CPY																								
DEC							D6	6	2	DE	7	3												
DEX																								
DEY																								
EOR	41	6	2	51	5	2	55	4	2	5D	4	3	59	4	3									
INC							F6	6	2	FE	7	3												
INX																								
INY																								
JMP																			6C	5	3			
JSR																								
LDA	A1	6	2	B1	5	2	B5	4	2	BD	4	3	B9	4	3									
LDX													BE	4	3							B6	4	2
LDY							B4	4	2	BC	4	3												
LSR							56	6	2	5E	7	3												
NOP																								
ORA	01	6	2	11	5	2	15	4	2	1D	4	3	19	4	3									
PHA																								
PHP																								
PLA																								
PLP																								
RMB[#(0-7)]																								
ROL							36	6	2	3E	7	3												
ROR							76	6	2	7E	7	3												
RTI																								
RTS																								
SBC	E1	6	2	F1	5	2	F5	4	2	FD	4	3	F9	4	3									
SEC																								
SED																								
SEI																								
SMB[#(0-7)]																								
STA	81	6	2	91	6	2	95	4	2	9D	5	3	[illegible]	5	3									
STX																						96	4	2
STY							94	4	2															
TAX																								
TAY																								
TSX																								
TXA																								
TXS																								
TYA																								

MNEMONIC	BIT ADDRESSING (OP BY BIT #) 0	1	2	3	4	5	6	7	PROCESSOR STATUS CODES 7 N	6 V	5 ·	4 B	3 D	2 I	1 Z	0 C
ADC									N	V	·	·	·	·	Z	C
AND									N	·	·	·	·	·	Z	·
ASL									N	·	·	·	·	·	Z	C
BBR[#(0-7)]	0F	1F	2F	3F	4F	5F	6F	7F	·	·	·	·	·	·	·	·
BBS[#(0-7)]	8F	9F	AF	BF	CF	DF	EF	FF	·	·	·	·	·	·	·	·
BCC									·	·	·	·	·	·	·	·
BCS									·	·	·	·	·	·	·	·
BEQ									·	·	·	·	·	·	·	·
BIT									M	M_6	·	·	·	·	Z	·
BMI									·	·	·	·	·	·	·	·
BNE									·	·	·	·	·	·		·
BPL									·	·	·	·	·	·	·	·
BRK									·	·	·	1	·	1	·	·
BVC									·	·	·	·	·	·	·	·
BVS									·	·	·	·	·	·	·	·
CLC									·	·	·	·	·	·	·	0
CLD									·	·	·	·	0	·	·	·
CLI									·	·	·	·	·	0	·	·
CLV									·	0	·	·	·	·	·	·
CMP									N	·	·	·	·	·	Z	C
CPX									N	·	·	·	·	·	Z	C
CPY									N	·	·	·	·	·	Z	C
DEC									N	·	·	·	·	·	Z	·
DEX									N	·	·	·	·	·	Z	·
DEY									N	·	·	·	·	·	Z	·
EOR									N	·	·	·	·	·	Z	·
INC									N	·	·	·	·	·	Z	·
INX									N	·	·	·	·	·	Z	·
INY									N	·	·	·	·	·	Z	·
JMP									·	·	·	·	·	·	·	·
JSR									·	·	·	·	·	·	·	·
LDA									N	·	·	·	·	·	Z	·
LDX									N	·	·	·	·	·	Z	·
LDY									N	·	·	·	·	·	Z	·
LSR									0	·	·	·	·	·	Z	C
NOP									·	·	·	·	·	·	·	·
ORA									N	·	·	·	·	·	Z	·
PHA									·	·	·	·	·	·	·	·
PHP									·	·	·	·	·	·	·	·
PLA									N	·	·	·	·	·	Z	·
PLP									(Restored)							
RMB[#(0-7)]	07	17	27	37	47	57	67	77	·	·	·	·	·	·	·	·
ROL									N	·	·	·	·	·	Z	C
ROR									N	·	·	·	·	·	Z	C
RTI									(Restored)							
RTS									·	·	·	·	·	·	·	·
SBC									N	V	·	·	·	·	Z	(3)
SEC									·	·	·	·	·	·	·	1
SED									·	·	·	·	1	·	·	·
SEI									·	·	·	·	·	1	·	·
SMB[#(0-7)]	87	97	A7	B7	C7	D7	E7	F7	·	·	·	·	·	·	·	·
STA									·	·	·	·	·	·	·	·
STX									·	·	·	·	·	·	·	·
STY									·	·	·	·	·	·	·	·
TAX									N	·	·	·	·	·	Z	·
TAY									N	·	·	·	·	·	Z	·
TSX									N	·	·	·	·	·	Z	·
TXA									N	·	·	·	·	·	Z	·
TXS									·	·	·	·	·	·	·	·
TYA									N	·	·	·	·	·	Z	·

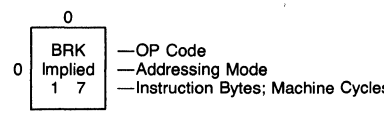
NOTES

1 Add 1 to N if page boundary is crossed
2 Add 1 to N if branch occurs to same page
  Add 2 to N if branch occurs to different page
3 Carry not = Borrow
4 If in decimal mode Z flag is invalid
  accumulator must be checked on zero result
5 Effects 8-bit data field of the specified zero page address

LEGEND

X	=	Index X
Y	=	Index Y
A	=	Accumulator
M	=	Memory per effective address
M_s	=	Memory per stack pointer
M_b	=	Selecter zero page memory bit
M_7	=	Memory Bit 7
M_6	=	Memory Bit 6
•	=	Add
–	=	Subtract
∧	=	And
V	=	Or
∀	=	Exclusive Or
n	=	Number of cycles
#	=	Number of Bytes

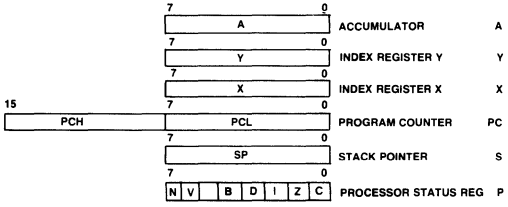
A.3 INSTRUCTION CODE MATRIX



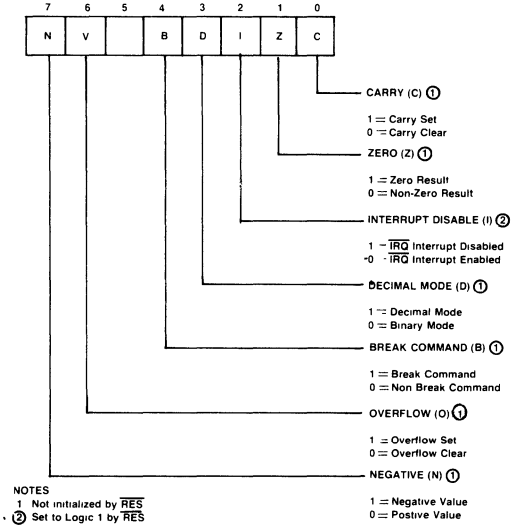
MSD \ LSD	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	MSD
0	BRK Implied 1 7	ORA (IND, X) 2 6				ORA ZP 2 3	ASL ZP 2 5	RMB0 ZP 2 5	PHP Implied 1 3	ORA IMM 2 2	ASL Accum 1 2			ORA ABS 3 4	ASL ABS 3 6	BBR0 ZP 3 5**	0
1	BPL Relative 2 2**	ORA (IND), Y 2 5*				ORA ZP, X 2 4	ASL ZP, X 2 6	RMB1 ZP 2 5	CLC Implied 1 2	ORA ABS, Y 3 4*				ORA ABS, X 3 4*	ASL ABS, X 3 7	BBR1 ZP 3 5**	1
2	JSR Absolute 3 6	AND (IND, X) 2 6			BIT ZP 2 3	AND ZP 2 3	ROL ZP 2 5	RMB2 ZP 2 5	PLP Implied 1 4	AND IMM 2 2	ROL Accum 1 2		BIT ABS 3 4	AND ABS 3 4	ROL ABS 3 6	BBR2 ZP 3 5**	2
3	BMI Relative 2 2**	AND (IND, Y) 2 5*				AND ZP, X 2 4	ROL ZP, X 2 6	RMB3 ZP 2 5	SEC Implied 1 2	AND ABS, Y 3 4*				AND ABS, X 3 4*	ROL ABS, X 3 7	BBR3 ZP 3 5**	3
4	RTI Implied 1 6	EOR (IND, X) 2 6				EOR ZP 2 3	LSR ZP 2 5	RMB4 ZP 2 5	PHA Implied 1 3	EOR IMM 2 2	LSR Accum 1 2		JMP ABS 3 3	EOR ABS 3 4	LSR ABS 3 6	BBR4 ZP 3 5**	4
5	BVC Relative 2 2**	EOR (IND), Y 2 5*				EOR ZP, X 2 4	LSR ZP, X 2 6	RMB5 ZP 2 5	CLI Implied 1 2	EOR ABS, Y 3 4*				EOR ABS, X 3 4*	LSR ABS, X 3 7	BBR5 ZP 3 5**	5
6	RTS Implied 1 6	ADC (IND, X) 2 6				ADC ZP 2 3	ROR ZP 2 5	RMB6 ZP 2 5	PLA Implied 1 4	ADC IMM 2 2	ROR Accum 1 2		JMP Indirect 3 5	ADC ABS 3 4	ROR ABS 3 6	BBR6 ZP 3 5**	6
7	BVS Relative 2 2**	ADC (IND, Y) 2 5*				ADC ZP, X 2 4	ROR ZP, X 2 6	RMB7 ZP 2 5	SEI Implied 1 2	ADC ABS, Y 3 4*				ADC ABS, X 3 4*	ROR ABS, X 3 7	BBR7 ZP 3 5**	7
8		STA (IND, X) 2 6			STY ZP 2 3	STA ZP 2 3	STX ZP 2 3	SMB0 ZP 2 5	DEY Implied 1 2		TXA Implied 1 2		STY ABS 3 4	STA ABS 3 4	STX ABS 3 4	BBS0 ZP 3 5**	8
9	BCC Relative 2 2**	STA (IND, Y) 2 6			STY ZP, X 2 4	STA ZP, X 2 4	STX ZP, Y 2 4	SMB1 ZP 2 5	TYA Implied 1 2	STA ABS, Y 3 5	TXS Implied 1 2			STA ABS, X 3 5		BBS1 ZP 3 5**	9
A	LDY IMM 2 2	LDA (IND, X) 2 6	LDX IMM 2 2		LDY ZP 2 3	LDA ZP 2 3	LDX ZP 2 3	SMB2 ZP 2 5	TAY Implied 1 2	LDA IMM 2 2	TAX Implied 1 2		LDY ABS 3 4	LDA ABS 3 4	LDX ABS 3 4	BBS2 ZP 3 5**	A
B	BCS Relative 2 2**	LDA (IND), Y 2 5*			LDY ZP, X 2 4	LDA ZP, X 2 4	LDX ZP, Y 2 4	SMB3 ZP 2 5	CLV Implied 1 2	LDA ABS, Y 3 4*	TSX Implied 1 2		LDY ABS, X 3 4*	LDA ABS, X 3 4*	LDX ABS, Y 3 4*	BBS3 ZP 3 5**	B
C	CPY IMM 2 2	CMP (IND, X) 2 6			CPY ZP 2 3	CMP ZP 2 3	DEC ZP 2 5	SMB4 ZP 2 5	INY Implied 1 2	CMP IMM 2 2	DEX Implied 1 2		CPY ABS 3 4	CMP ABS 3 4	DEC ABS 3 6	BBS4 ZP 3 5**	C
D	BNE Relative 2 2**	CMP (IND), Y 2 5*				CMP ZP, X 2 4	DEC ZP, X 2 6	SMB5 ZP 2 5	CLD Implied 1 2	CMP ABS, Y 3 4*				CMP ABS, X 3 4*	DEC ABS, X 3 7	BBS5 ZP 3 5**	D
E	CPX IMM 2 2	SBC (IND, X) 2 6			CPX ZP 2 3	SBC ZP 2 3	INC ZP 2 5	SMB6 ZP 2 5	INX Implied 1 2	SBC IMM 2 2	NOP Implied 1 2		CPX ABS 3 4	SBC ABS 3 4	INC ABS 3 6	BBS6 ZP 3 5**	E
F	BEQ Relative 2 2**	SBC (IND), Y 2 5*				SBC ZP, X 2 4	INC ZP, X 2 6	SMB7 ZP 2 5	SED Implied 1 2	SBC ABS, Y 3 4*				SBC ABS, X 3 4*	INC ABS, X 3 7	BBS7 ZP 3 5**	F
	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	

*Add 1 to N if page boundary is crossed
**Add 1 to N if branch occurs to same page,
add 2 to N if branch occurs to different page.

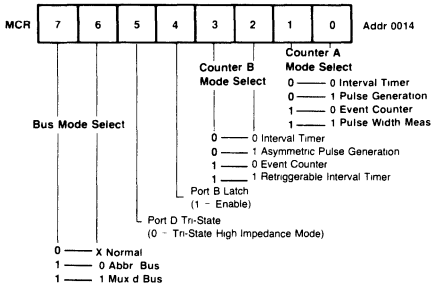
APPENDIX B
KEY REGISTER SUMMARY



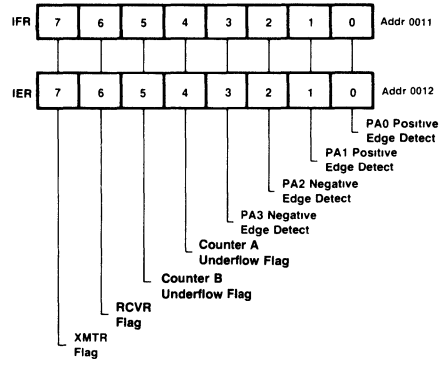
CPU Registers



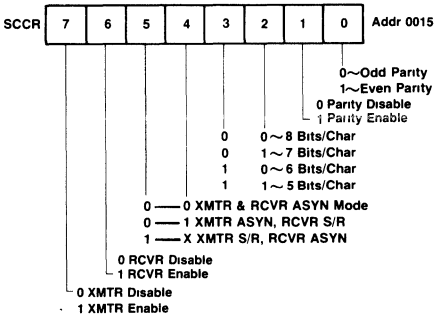
Processor Status Register



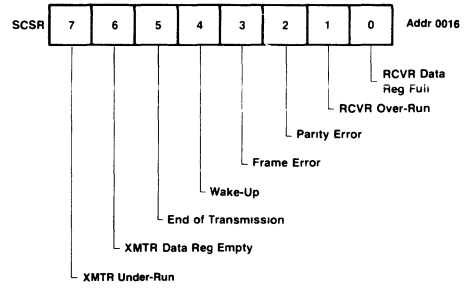
Mode Control Register



Interrupt Enable and Flag Registers



Serial Communications Control Register



Serial Communications Status Register

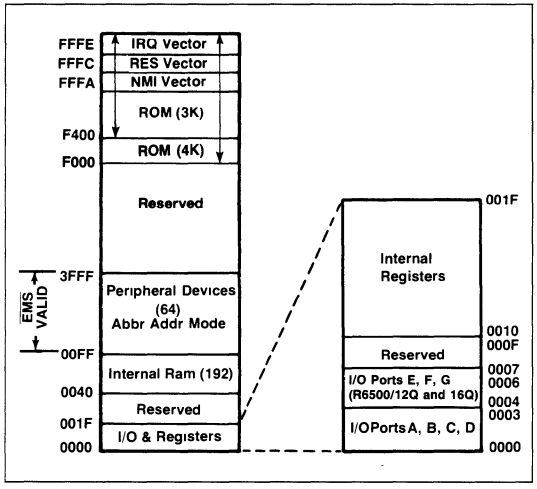
APPENDIX C
ADDRESS ASSIGNMENTS/MEMORY MAPS/PIN FUNCTIONS

C.1 I/O AND INTERNAL REGISTER ADDRESSES

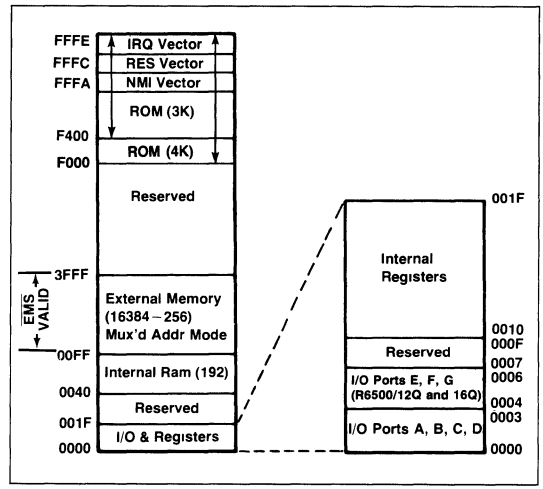
ADDRESS (HEX)	READ	WRITE
001F	— —	— —
1E	Lower Counter B	Upper Latch B, Cntr B←Latch B, CLR Flag
1D	Upper Counter B	Upper Latch B, Latch C←Latch B
1C	Lower Counter B, CLR Flag	Lower Latch B
1B	— —	— —
1A	Lower Counter A	Upper Latch A, Cntr A←Latch A, CLR Flag
19	Upper Counter A	Upper Latch A
18	Lower Counter A, CLR Flag	Lower Latch A
17	Serial Receiver Data Register	Serial Transmitter Data Register
16	Serial Comm. Status Register	Serial Comm Status Reg Bits 4 & 5 only
15	Serial Comm. Control Register	Serial Comm. Control Register
14	Mode Control Register	Mode Control Register
13	— —	— —
12	Interrupt Enable Register	Interrupt Enable Register
11	Interrupt Flag Register	— —
0010	Read FF	Clear Int Flag (Bits 0-3 only, Write 0's only)
0F	— —	— —
0E	— —	— —
0D	— —	— —
0C	— —	— —
0B	— —	— —
0A	— —	— —
09	— —	— —
08	— —	— —
07	— —	— —
06	Port G*	Port G*
05	Port F*	Port F*
04	Port E*	Port E*
03	Port D	Port D
02	Port C	Port C
01	Port B	Port B
0000	Port A	Port A

NOTE: *R6500/12Q or /16Q only.

C.2 ABBREVIATED MODE MEMORY MAP



C.3 MULTIPLEXED MODE MEMORY MAP



C.4 MULTIPLE FUNCTION PIN ASSIGNMENTS—PORT C AND PORT D

PIN NUMBER	I/O PORT FUNCTION	ABBREVIATED PORT FUNCTION	MULTIPLEXED PORT FUNCTION
4	PC0	A0	A0
5	PC1	A1	A1
6	PC2	A2	A2
7	PC3	A3	A3
8	PC4	A12	A12
9	PC5	R/$\overline{W}$	R/$\overline{W}$
10	PC6	A13	A13
11	PC7	$\overline{EMS}$	$\overline{EMS}$
19	PD0	D0	A4/D0
18	PD1	D1	A5/D1
17	PD2	D2	A6/D2
16	PD3	D3	A7/D3
15	PD4	D4	A8/D4
14	PD5	D5	A9/D5
13	PD6	D6	A10/D6
12	PD7	D7	A11/D7

APPENDIX D
ELECTRICAL SPECIFICATIONS

MAXIMUM RATINGS*

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC} & V_{RR}	−0.3 to +7.0	Vdc
Input Voltage	V_{IN}	−0.3 to +7.0	Vdc
Operating Temperature Commercial	T_A	T_L to T_H 0 to +70	°C
Storage Temperature	T_{STG}	−55 to +150	°C

***NOTE:** Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in other sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

(V_{CC} = 5.0V ±5%, V_{RR} = V_{CC}; V_{SS} = 0V; T_A = 0° to 70°, unless otherwise specified)

Parameter	Symbol	Min	Typ[1]	Max	Unit	Test Conditions
RAM Standby Voltage (Retention Mode)	V_{RR}	3.0		V_{CC}	V	
RAM Standby Current (Retention Mode)	I_{RR}	—	4	—	mA	T_A = 25°C
Input High Voltage All Except XTLI and Ø2 in Slave Option XTLI and Ø2 in Slave Option	V_{IH}	 +2.0 +4.0	 — —	 V_{CC} V_{CC}	V	
Input Low Voltage	V_{IL}	−0.3	—	+0.8	V	
Input Leakage Current $\overline{RES}$, $\overline{NMI}$	I_{IN}	—	—	±10.0	μA	V_{IN} = 0 to 5.0V
Input Low Current PA, PB, PC, PD, PF[3], PG[3]	I_{IL}	—	−1.0	−1.6	mA	V_{IL} = 0.4V
Output High Voltage (Except XTLO)	V_{OH}	+2.4	—	V_{CC}	V	I_{LOAD} = −100 μA
Output Low Voltage	V_{OL}	—	—	+0.4	V	I_{LOAD} = 1.6 mA
I/O Port Pull-Up Resistance PA0–PA7, PB0–PB7, PC0–PC7, PF0–PF7[3], PG0–PG7[3]	R_L	3.0	6.0	11.5	Kohm	
Output Leakage Current (Three-State Off)	I_{OUT}	—	—	±10	μA	
Input Capacitance XTLI, XTLO PA, PB, PC, PD, PF[3], PG[3]	C_{IN}	 — —	 — —	 50 10	pF	T_A = 25°C V_{IN} = 0V f = 1.0 MHz
Output Capacitance (Three-State Off)	C_{OUT}	—	—	10	pF	T_A = 25°C V_{IN} = 0V f = 1.0 MHz
Power Dissipation (Outputs High)	P_D	—	—	1200	mW	T_A = 25°C

Notes:
1. Typical values measured at T_A = 25°C and V_{CC} = 5.0V.
2. Negative sign indicates outward current flow, positive indicates inward flow.
3. R6500/12Q and R6500/16Q only.

APPENDIX E
TIMING REQUIREMENTS AND CHARACTERISTICS

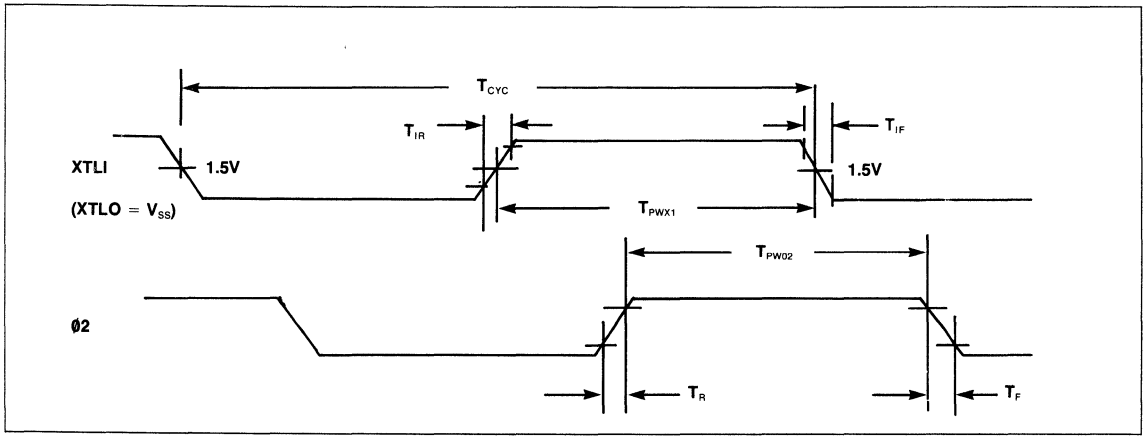
E.1 GENERAL NOTES

1. V_{CC} = 5V ±5%, 0°C ≤ TA ≤ 70°C
2. A valid V_{CC} – $\overline{RES}$ sequence is required before proper operation is achieved.
3. All timing reference levels are 0.8V and 2.0V, unless otherwise specified.
4. All time units are nanoseconds, unless otherwise specified.
5. All capacitive loading is 130pf maximum, except as noted below:

PA, PB	—	50pf maximum
PC (I/O Modes Only)	—	50pf maximum
PC (ABB and Mux Mode)	—	130pf maximum
PC6, PC7 (Full Address Mode)	—	130pf maximum

E.2 CLOCK TIMING

SYMBOL	PARAMETER	1 MHz		2 MHz	
		MIN	MAX	MIN	MAX
T_{CYC}	Cycle Time	1000	10 μs	500	10 μs
T_{PWX1}	XTLI Input Clock Pulse Width XTLO = VSS	500 ± 25	—	250 ± 10	—
T_{PW02}	Output Clock Pulse Width at Minimum T_{CYC}	T_{PWX1}	T_{PWX1} ± 25	T_{PWX1}	T_{PWX1} ± 20
T_R, T_F	Output Clock Rise, Fall Time	—	25	—	15
T_{IR}, T_{IF}	Input Clock Rise, Fall Time	—	10	—	10



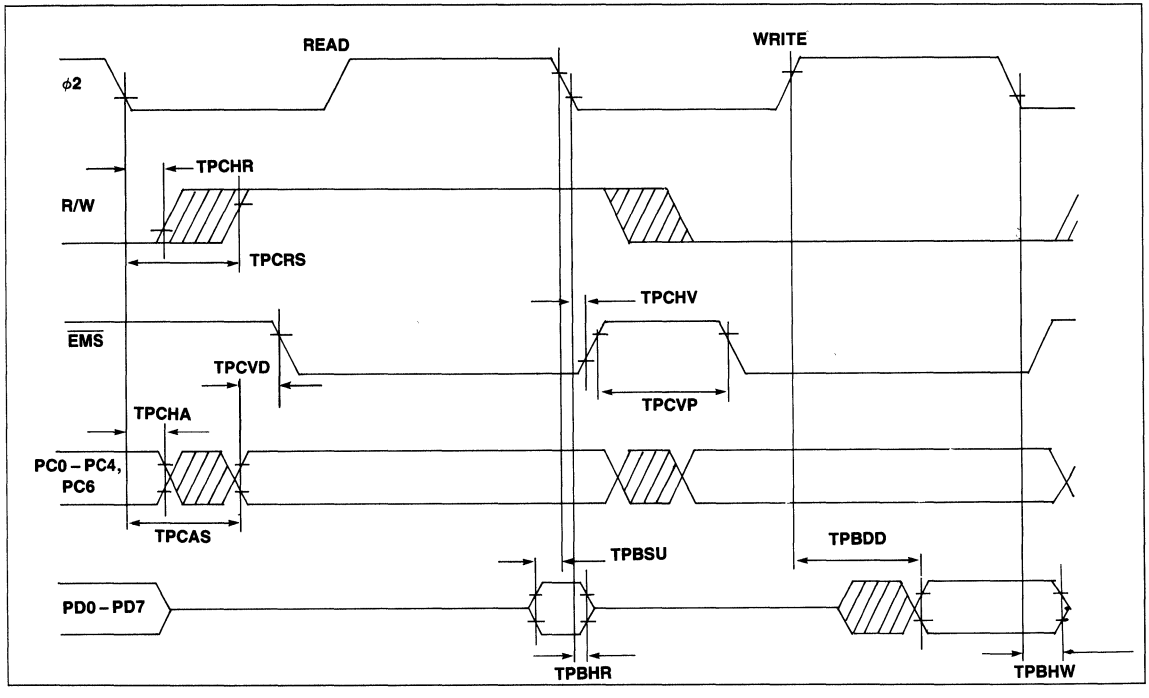
E.3 ABBREVIATED MODE TIMING—PC AND PD

(MCR 5 = 1, MCR 6 = 0, MCR 7 = 1)

SYMBOL	PARAMETER	1 MHz		2 MHz	
		MIN	MAX	MIN	MAX
T_{PCRS}	(PC5) R/W Setup Time	—	225	—	140
T_{PCAS}	(PC0-PC4, PC6) Address Setup Time	—	200	—	140
T_{PBSU}	(PD) Data Setup Time	50	—	35	—
T_{PBHR}	(PD) Data Read Hold Time	10	—	10	—
T_{PBHW}	(PD) Data Write Hold Time	30	—	30	—
T_{PBDD}	(PD) Data Output Delay	—	175	—	130
T_{PCHA}	(PC0-PC4, PC6) Address Hold Time	30	—	30	—
T_{PCHR}	(PC5) R/W Hold Time	30	—	30	—
T_{PCHV}	(PC7) $\overline{EMS}$ Hold Time	10	—	10	—
T_{PCVD}(1)	(PC7) Address to $\overline{EMS}$ Delay Time	30	220	30	130
T_{PCVP}	(PC7) $\overline{EMS}$ Stabilization Time	30	—	30	—

NOTE 1 Values assume PC0-PC4, PC6 and PC7 have the same capacitive load.

E.3.1 Abbreviated Mode Timing Diagram



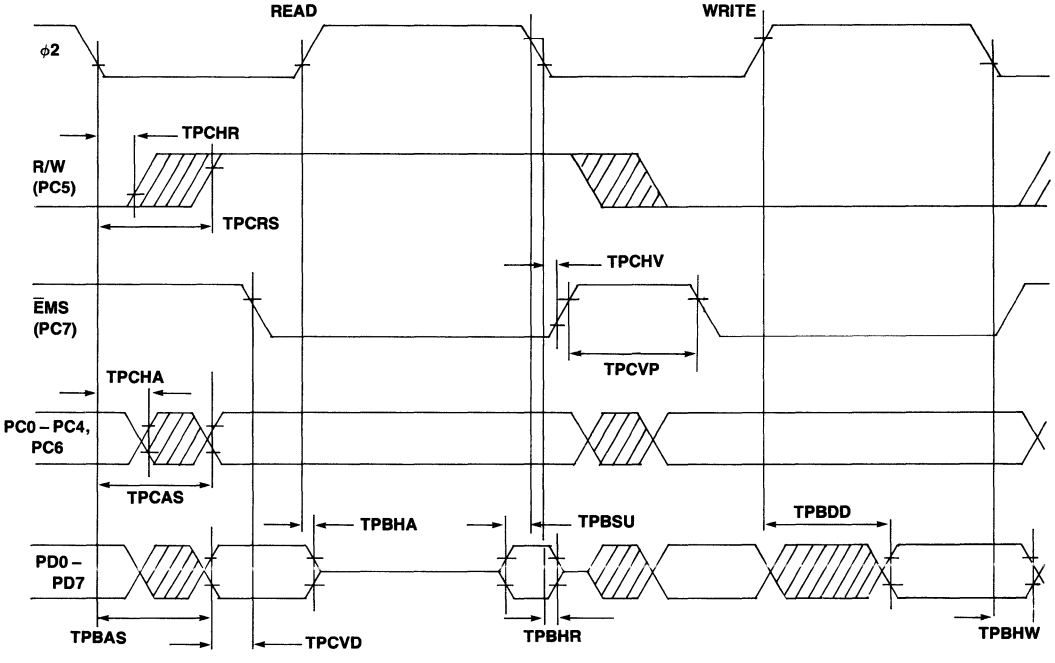
E.4 MULTIPLEXED MODE TIMING—PC AND PD

(MCR 5 = 1, MCR 6 = 1, MCR 7 = 1)

SYMBOL	PARAMETER	1 MHz		2 MHz	
		MIN	MAX	MIN	MAX
T_{PCRS}	(PC5) R/W Setup Time	—	225	—	140
T_{PCAS}	(PC0-PC4, PC6) Address Setup Time	—	200	—	140
T_{PBAS}	(PD) Address Setup Time	—	220	—	120
T_{PBSU}	(PD) Data Setup Time	50	—	35	—
T_{PBHR}	(PD) Data Read Hold Time	10	—	10	—
T_{PBHW}	(PD) Data Write Hold Time	30	—	30	—
T_{PBDD}	(PD) Data Output Delay	—	175	—	140
T_{PCHA}	(PC0-PC4, PC6) Address Hold Time	30	—	30	—
T_{PBHA}	(PD) Address Hold Time	40	100	40	80
T_{PCHR}	(PC5) R/W Hold Time	30	—	30	—
T_{PCHV}	(PC7) $\overline{EMS}$ Hold Time	10	—	10	—
T_{PCVD}[1]	(PC7) Address to $\overline{EMS}$ Delay Time	30	200	30	150
T_{PCVP}	(PC7) $\overline{EMS}$ Stabilization Time	30	—	30	—

NOTE 1. Values assume PD0-PD7 and PC7 have the same capactive load.

E.4.1 Multiplex Mode Timing Diagram

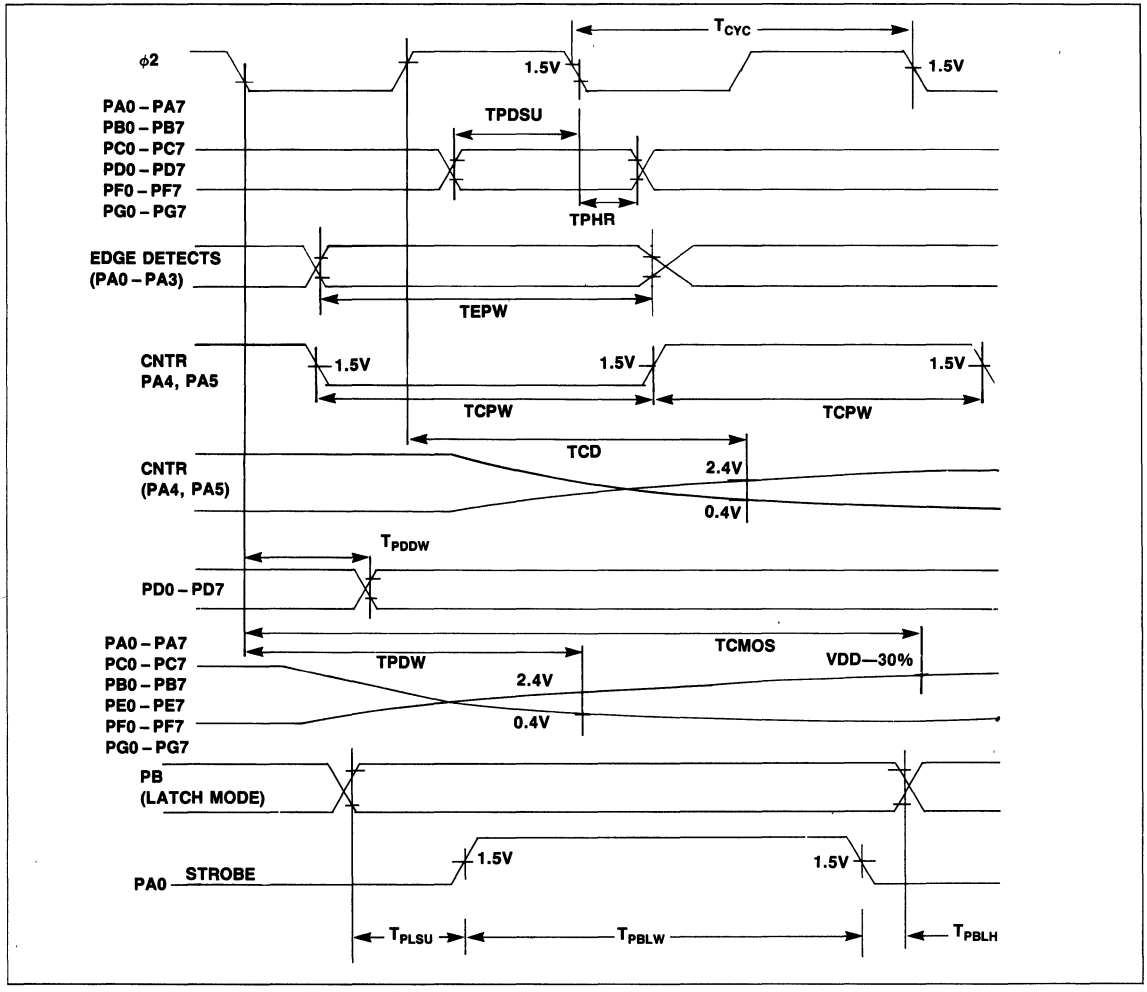


E.5 I/O, EDGE DETECT, COUNTERS, AND SERIAL I/O TIMING

SYMBOL	PARAMETER	1 MHz		2 MHz	
		MIN	MAX	MIN	MAX
	Internal Write to Peripheral Data Valid				
T_{PDW}(1)	PA, PB, PC, PE, PF, PG, TTL	—	500	—	500
T_{CMOS}(1)	PA, PB, PC, PE, PF, PG, CMOS	—	1000	—	1000
T_{PDDW}	PD	—	175	—	150
	Peripheral Data Setup Time				
T_{PDSU}	PA, PB, PC, PF, PG	200	—	200	—
T_{PDSU}	PD	50	—	50	—
	Peripheral Data Hold Time				
T_{PHR}	PA, PB, PC, PF, PG	75	—	75	—
T_{PHR}	PD	10	—	10	—
T_{EPW}	PA0-PA3 Edge Detect Pulse Width	T_{CYC}	—	T_{CYC}	—
	Counters A and B				
T_{CPW}	PA4, PA5 Input Pulse Width	T_{CYC}	—	T_{CYC}	—
T_{CD}(1)	PA4, PA5 Output Delay	—	500	—	500
	Port B Latch Mode				
T_{PBLW}	PA0 Strobe Pulse Width	T_{CYC}	—	T_{CYC}	—
T_{PLSU}	PB Data Setup Time	175	—	150	—
T_{PBLH}	PB Data Hold Time	30	—	30	—
	Serial I/0				
T_{PDW}(1)	PA6 XMTR TTL	—	500	—	500
T_{CMOS}(1)	PA6 XMTR CMOS	—	1000	—	1000
T_{CPW}	PA4 RCVR S/R Clock Width	4 T_{CYC}	—	4 T_{CYC}	—
T_{PDW}(1)	PA4 XMTR Clock—S/R Mode (TTL)	—	500	—	500
T_{CMOS}(1)	PA4 XMTR Clock—S/R Mode (CMOS)	—	1000	—	1000

NOTE 1: Maximum Load Capacitance: 50pF Passive Pull-Up Required

E.5.1 I/O, Edge Detect, Counter, and Serial I/O Timing



Rockwell

R65/11EB AND R65/11EAB BACKPACK EMULATORS

INTRODUCTION

The Rockwell R65/11EB and R65/11EAB Backpack Emulator is the PROM prototyping version of the 8-bit, masked-ROM R6500/11 one-chip microcomputer. Like the R6500/11, the backpack device is totally upward/downward compatible with all members of the R6500/11 family. It is designed to accept standard 5-volt, 24-pin EPROMs or ROMs directly, in a socket on top of the Emulator. This packaging concept allows a standard EPROM to be easily removed, re-programmed, then reinserted as often as desired.

The backpack devices have the same pinouts as the masked-ROM R6500/11 microcomputer. These 40 pins are functionally and operationally identical to the pins on the R6500/11. The R6500/11 Microcomputer Product Description (Rockwell Document No. 29651N23, Order No. 2119) includes a description of the interface signals and their functions. Whereas the masked-ROM R6500/11 provides 3K bytes of read-only memory, the R65/11EB will address 4K bytes of external program memory. This extra memory accommodates program patches, test programs or optional programs during breadboard and prototype development states.

ORDERING INFORMATION

Backpack Emulator

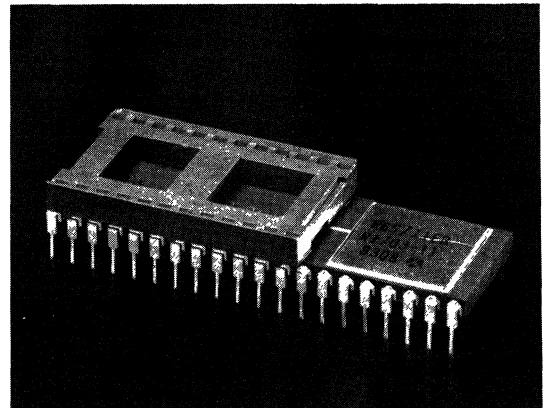
Part Number	Memory Capacity	Compatible Memories	Temperature Range and Speed
R65/11EB	4K × 8	2732	0°C to 70°C 1MHz
R65/11EAB	4K × 8	2732A	0°C to 70°C 2 MHz

Support Products

Part Number	Description
S65-101	SYSTEM 65 Microcomputer Development System
M65-040	PROM Programmer Module
M65-131	1-MHz R6500/11 Personality Module
M65-132	2-MHz R6500/11 Personality Module
RDC-1001	Rockwell Design Center
RDC-101	1 MHz R6500/11P Personality Module (RDC)
RDC-102	2 MHz R6500/11AP Personality Module (RDC)

FEATURES

- PROM version of the R6500/11
- Completely pin compatible with R6500/11 single-chip microcomputers
- Profile approaches 40-pin DIP of R6500/11
- Accepts 5 volt, 24-pin industry-standard EPROMs —4K memories—2732, 2732A (4K bytes addressable)
- Use as prototyping tool or for low volume production
- 4K bytes of memory capacity
- 192 × 8 static RAM
- Separate power pin for 32 bytes of RAM
- Software compatibility with the R6500 family
- 32 bi-directional TTL compatible I/O lines (4 ports)
- Two 16 bit programmable counter/latches with six modes (interval timer, pulse generator, event counter, pulse width measurement, asymmetrical pulse generator, and retriggerable interval timer)
- 10 interrupts (reset, non-maskable, four external edge sensitive, 2 counters, serial data received, serial data transmitted).
- Crystal or external time base
- Single +5V power supply



R65/11EB Backpack Emulator

CONFIGURATIONS

The Backpack Emulator is available in two different versions, to accommodate 1 MHz and 2 MHz speeds. Both versions provide 192 bytes of RAM and I/O, as well as 24 signals to support the external memory "backpack" socket.

The emulator will relocate the EPROM address space to FXXX (see Memory Map). EPROM addresses FFA through FFF must contain the interrupt vectors.

EXTERNAL FREQUENCY REFERENCE

The external frequency reference may be a crystal or a clock—the RC option of the R6500/11 is not available in the emulator device. The R65/11EB and R65/11EAB divide the input clock by two regardless of the source.

I/O PORT PULLUPS

The devices have internal I/O port pullup resistors on ports A, B, & C. Port D has push-pull drivers.

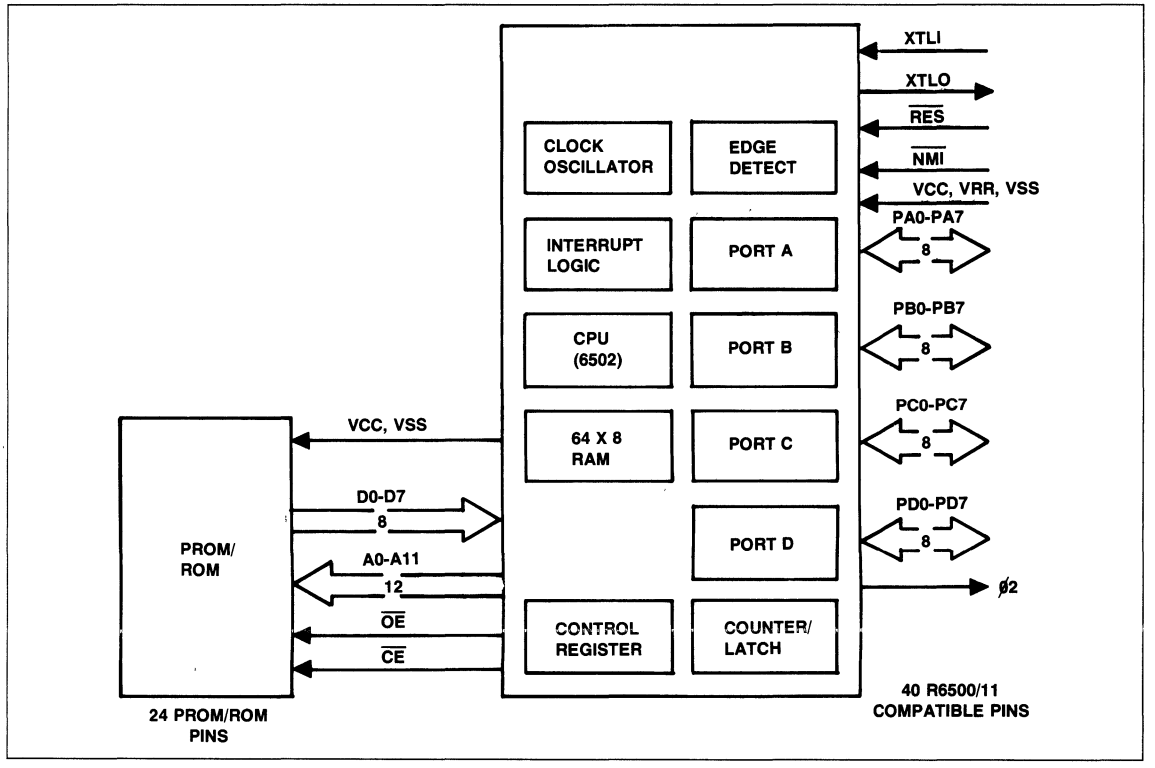
PRODUCT SUPPORT

The Backpack Emulator is just one of the products that Rockwell offers to facilitate system and program development for the R6500/11.

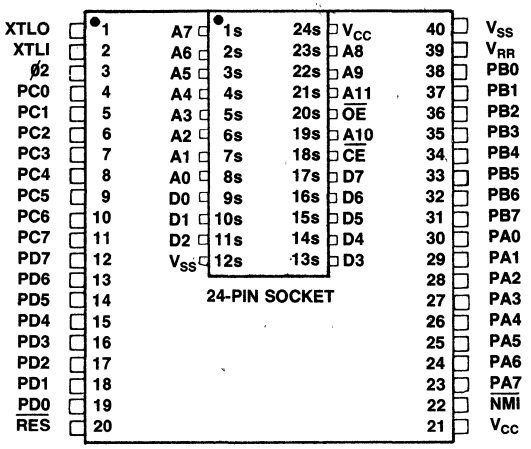
The SYSTEM 65 Microcomputer Development System with R6500/11 Personality Module supports both hardware and software development. Complete in-circuit user emulation with the R6500/11 Personality Module allows total system test and evaluation. With the optional PROM Programmer, SYSTEM 65 can also be used to program EPROMs for the development activity. When PROM programs have been finalized, the PROM device can be sent to Rockwell for masking into the 3K ROM of the R6500/11.

In addition to support products, Rockwell offers regularly-scheduled designer courses at regional centers.

3



R65/11EB Interface Diagram



Pin Configuration

BACKPACK MEMORY SIGNAL DESCRIPTION

Signal Name	Pin No.	Description
D0-D7	9S-11S, 13S-17S	Data Bus Lines. All instruction and data transfers take place on the data bus lines. The buffers driving the data bus lines have full three-state capability. Each data bus pin is connected to an input and an output buffer, with the output buffer remaining in the floating condition.
A0-A7 A8, A9 A10 A11	1S-8S, 23S, 24S 19S 21S	Address Bus Lines. The address bus lines are buffered by push/pull type drivers that can drive one standard TTL load.
$\overline{CE}$	18S	Chip Enable. $\overline{CE}$ is active when the address is 8000-FFFF. This line can drive one TTL load.
$\overline{OE}$	20S	Memory Enable Line. This signal provides the output enable for the memory to place information on the data bus lines. This signal is driven by an inverted R/$\overline{W}$ signal from the CPU. It can drive 1 TTL load.
V_{CC}	24S	Main Power Supply +5V. This pin is tied directly to pin 21 (V_{CC}).
V_{SS}	12S	Signal and Power Ground (zero volts). This pin is tied directly to pin 40 (V_{SS}).

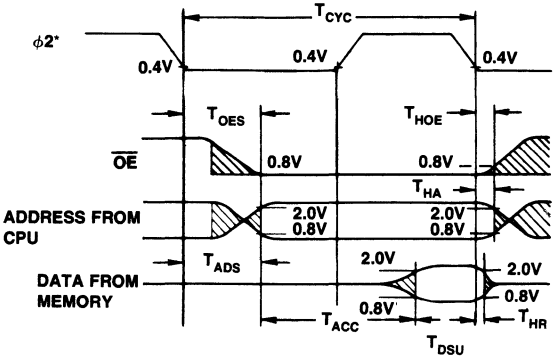
I/O AND INTERNAL REGISTER ADDRESSES

Address (Hex)	Read	Write
001F	— —	— —
1E	Lower Counter B	Upper Latch B, Cntr B←Latch B, CLR Flag
1D	Upper Counter B	Upper Latch B, Latch C←Latch B
1C	Lower Counter B, CLR Flag	Lower Latch B
1B	— —	— —
1A	Lower Counter A	Upper Latch A, Cntr A←Latch A, CLR Flag
19	Upper Counter A	Upper Latch A
18	Lower Counter A, CLR Flag	Lower Latch A
17	Serial Receiver Data Register	Serial Transmitter Data Register
16	Serial Comm. Status Register	Serial Comm. Status Reg. Bits 4 & 5 only
15	Serial Comm. Control Register	Serial Comm. Control Register
14	Mode Control Register	Mode Control Register
13	— —	— —
12	Interrupt Enable Register	Interrupt Enable Register
11	Interrupt Flag Register	— —
0010	Read FF	Clear Int Flag (Bits 0-3 only, Write 0's only)
04 thru 0F	— —	— —
03	Port D	Port D
02	Port C	Port C
01	Port B	Port B
0000	Port A	Port A

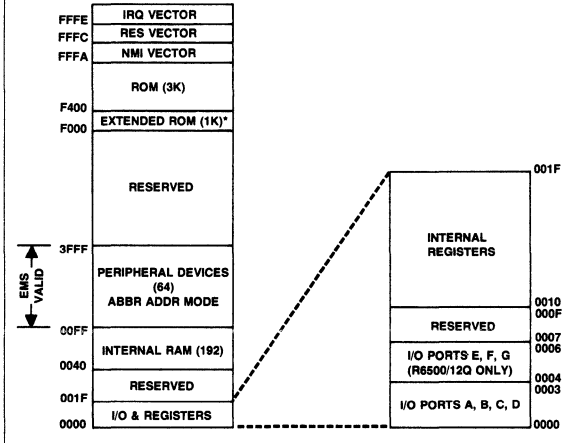
READ TIMING CHARACTERISTICS

Signal	Symbol	1 MHz		2 MHz		Unit
		Min.	Max.	Min.	Max.	
$\overline{OE}$ and $\overline{CE}$ setup time from CPU	T_{OES}	—	225	—	140	ns
Address setup time from CPU	T_{ADS}	—	225	—	140	ns
Memory read access time	T_{ACC}	—	700	—	315	ns
Data set up time	T_{DSU}	50	—	35	—	ns
Data hold time—Read	T_{HR}	10	—	10	—	ns
Address hold time	T_{HA}	30	—	30	—	ns
$\overline{OE}$ and $\overline{CE}$ hold time	T_{HOE}	30	—	30	—	ns
Cycle Time	T_{CYC}	1.0	10.0	0.5	10.0	μs

READ TIMING WAVEFORMS

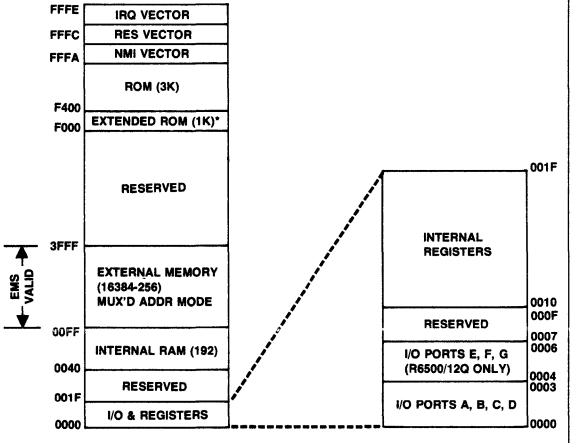


ABBREVIATED MODE MEMORY MAP



*NOT AVAILABLE FOR MASKED ROM R6500/11.

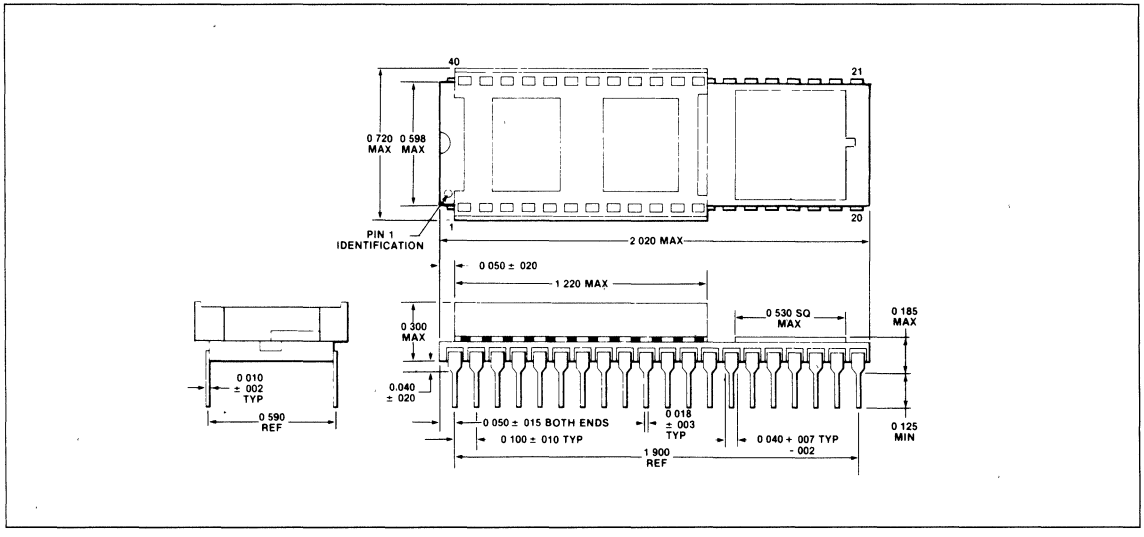
MULTIPLEXED MODE MEMORY MAP



ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0 ± 5%, V_{SS} = 0, T_A = 25°C)

Characteristic	Symbol	Min	Typ	Max	Unit
Input High Threshold Voltage D0-D7	V_{IHT}	V_{SS} + 2.0	—	—	Vdc
Input Low Threshold Voltage D0-D7	V_{ILT}	—	—	V_{SS} + 0.8	Vdc
Three-State (Off State) Input Current (V = 0.4 to 2.4V, V_{CC} = 5.25V) D0-D7	I_{TSI}	—	—	± 10	μA
Output High Voltage (I_{LOAD} = 100μ Adc, V_{CC} = 4.75V) D0-D7, A0-A11, $\overline{OE}$, $\overline{CE}$	V_{OH}	V_{SS} + 2.4	—	—	Vdc
Output Low Voltage (I_{LOAD} = 1.6 mAdc, V_{CC} = 4.75V) D0-D7, A0-A11, $\overline{OE}$, $\overline{CE}$	V_{OL}	—	—	V_{SS} + 0.4	Vdc
Power Dissipation (less EPROM)	P_D	—	0.80	1.20	W
Capacitance (V_{in} = 0, T_A = 25°C, f = 1 MHz) D0-D7 (High Impedance State) Input Capacitance	C C_{out} C_{in}	— —	— —	 10 10	pF
I/O Port Pull-up Resistance	R_L	3.0	6.0	11.5	kohm



40-Pin Backpack Package

Rockwell

R6511Q and R6500/13 ONE-CHIP MICROPROCESSOR and ONE-CHIP MICROCOMPUTER

SECTION 1 INTRODUCTION

1.1 FEATURES

- Enhanced 6502 CPU
  - —Four new bit manipulation instructions
    - Set Memory Bit (SMB)
    - Reset Memory Bit (RMB)
    - Branch on Bit Set (BBS)
    - Branch on Bit Reset (BBR)
  - —Decimal and binary arithmetic modes
  - —13 addressing modes
  - —True indexing
- 256-byte mask-programmable ROM or no ROM*
- 192-byte static RAM
- 32 bidirectional, TTL-compatible I/O lines (four ports)
- One 8-bit port may be tri-stated under software control
- One 8-bit port may have latched inputs under software control
- Two 16-bit programmable counter/timers, with latches
  - —Pulse width measurement
  - —Asymmetrical pulse generation
  - —Pulse generation
  - —Interval timer
  - —Event counter
  - —Retriggerable interval timer
- Serial port
  - —Full-duplex asynchronous operation mode
  - —Selectable 5- to 8-bit characters
  - —Wake-up feature
  - —Synchronous shift register mode
  - —Standard programmable bit rates programmable up to 62.5K bits/sec @ 1 MHz
- Ten interrupts
  - —Four edge-sensitive lines; two positive, two negative
  - —Reset
  - —Non-maskable
  - —Two counter underflows
  - —Serial data received
  - —Serial data transmitted
- Bus expandable to 64K bytes of external memory

*R6511Q has no ROM.

- Flexible clock circuitry
  - —2-MHz or 1-MHz internal operation
  - —Internal clock with external XTAL at two or four times internal frequency
  - —External clock input divided by one, two or four
- 1 μs minimum instruction execution time @ 2 MHz
- NMOS-3 silicon gate, depletion load technology
- Single +5V power supply
- 12 mW stand-by power for 32 bytes of the 192-byte RAM
- 64-pin QUIP

NOTE

This document uses the term R6500/13 to describe both parts. See section 1.3 for a description of the options available when using the R6500/13 and the fixed features of the R6511Q.

1.2 SUMMARY

The Rockwell R6500/13 is a complete, high-performance 8-bit NMOS-3 microcomputer on a single chip and is compatible with all members of the R6500 family.

The R6500/13 consists of an enhanced 6502 CPU, an internal clock oscillator, an optional 256 bytes of Read-Only Memory, 192 bytes of Random Access Memory (RAM) and versatile interface circuitry. The interface circuitry includes two 16-bit programmable timer/counters, 32 bidirectional input/output lines (including four edge-sensitive lines and input latching on one 8-bit port), a full-duplex serial I/O channel, ten interrupts and bus expandability.

The innovative architecture and the demonstrated high performance of the R6502 CPU, as well as instruction simplicity, results in system cost-effectiveness and a wide range of computational power. These features make the R6500/13 a leading candidate for microcomputer applications.

The R6511Q contains all the features of the R6500/13 except it has no ROM and is thus intended as a high feature microprocessor with full 65K address bus.

To allow prototype circuit development, Rockwell offers a PROM-compatible 64-pin extended microprocessor device. This device, the R6511Q, provides all R6500/11 interface lines, plus the address bus, data bus and control lines to interface with external memory. The R6511Q also can be used to emulate the R6500/13. With the addition of external circuits it can also emulate the R6500/12.

Rockwell supports development of the R6500/13 with the System 65 Microcomputer Development System and the R6500/* Family of Personality Modules. Complete in-circuit emulation with the R6500/* Family of Personality Modules allows total system test and evaluation.

This product description assumes that the reader is familiar with the R6502 CPU hardware and programming capabilities. A detailed description of the R6502 CPU hardware is included in the R6500 Microcomputer System Hardware Manual (Document Number 29650N31). A description of the instruction capabilities of the R6502 CPU is contained in the R6500 Microcomputer System Programming Manual (Document Number 29650N30).

1.3 CUSTOMER OPTIONS

The R6500/13 microcomputer is available with the following customer specified mask options.

- Option 1 Crystal or RC oscillator
- Option 2 Clock divide by 2 or 4
- Option 3 Clock MASTER Mode or SLAVE Mode
- Option 4 with or without a 256 byte ROM
- Option 5 Reset Vector at FFFC or 7FFF
- Option 6 Port A with or without internal pull-up resistors
- Option 7 Port B with or without internal pull-up resistors
- Option 8 Port C with or without internal pull-up resistors

All options should be specified on an R6500/13 order form.

The R6511Q has no customer specified mask options. It has the following characteristics.

- Crystal Oscillator
- Clock Divide by 2
- Clock MASTER Mode
- Without ROM
- Reset Vector at FFFC
- No internal pull-up resistors or any Port (PA, PB, or PC)

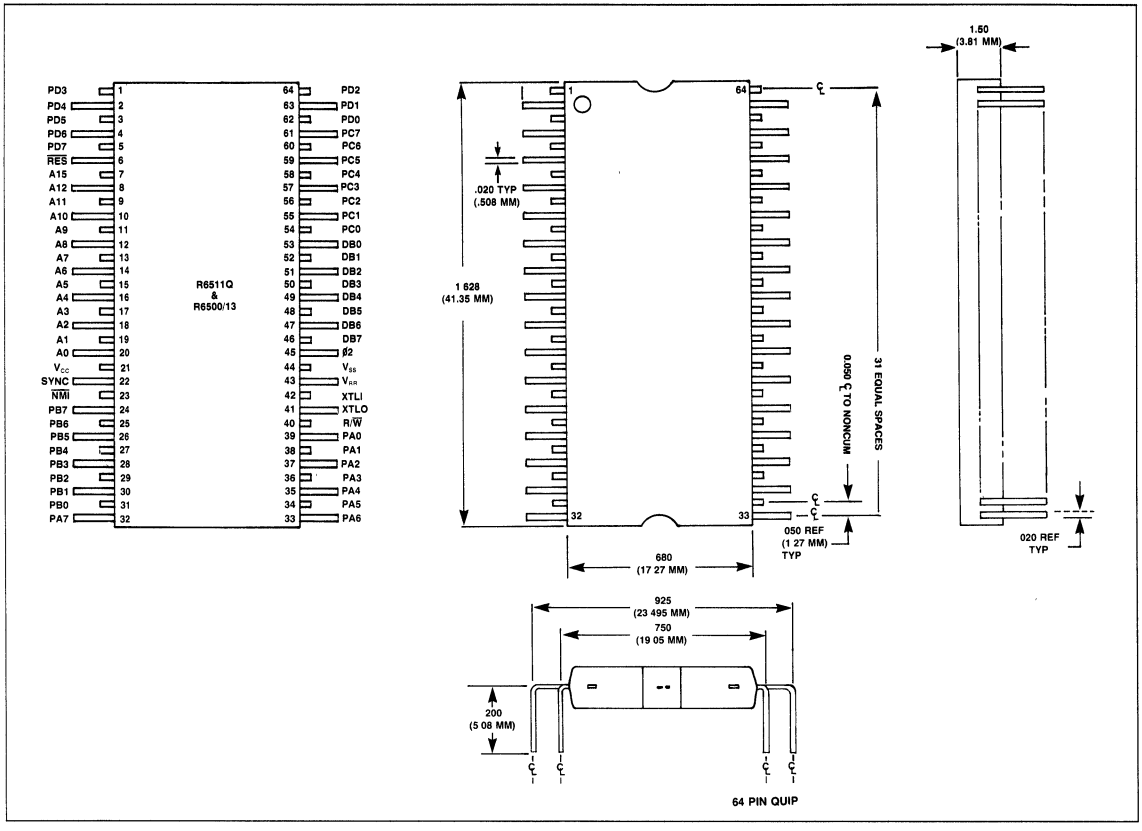


Figure 2-1. Mechanical Outline & Pin Out Configuration

SECTION 2
INTERFACE REQUIREMENTS

This section describes the interface requirements for the R6511Q and R6500/13. Figure 2-1 and 2-2 show the Interface Diagram and the pin out configuration for both devices. Table 2-1 describes the function of each pin. Figure 3-1 has a detailed block diagram of the R6500/13 ports which illustrates the internal function of the device.

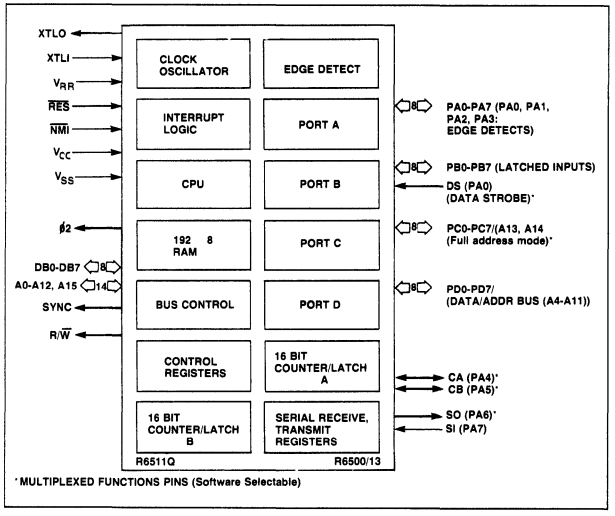


Figure 2-2. Interface Diagram

Table 2-1. R6500/13 Pin Descriptions

Signal Name	Pin No.	Description
V_{CC}	21	Main power supply +5V
V_{RR}	43	Separate power pin for RAM. In the event that V_{CC} power is off, this power retains RAM data.
V_{SS}	44	Signal and power ground (0V)
XTLI	42	Crystal or clock input for internal clock oscillator. Also allows input of X1 clock signal if XTLO is connected to V_{SS}, or X2 or X4 clock if XTLO is floated.
XTLO	41	Crystal output from internal clock oscillator.
$\overline{RES}$	6	The Reset input is used to initialize the device. This signal must not transition from low to high for at least eight cycles after V_{CC} reaches operating range and the internal oscillator has stabilized.
$\phi 2$	45	Clock signal output at internal frequency.
$\overline{NMI}$	23	A negative going edge on the Non-Maskable Interrupt signal requests that a non-maskable interrupt be generated with the CPU.
PA0-PA7 PB0-PB7 PC0-PC7 PD0-PD7	39-32 31-24 54-61 62-64, 1-5	Four 8-bit ports used for either input/output. Each line of Ports A, B and C consists of an active transistor to V_{SS} and an optional passive pull-up to V_{CC}. In the abbreviated or multiplexed modes of operation Port C has an active pull-up transistor. Port D functions as either an 8-bit input or 8-bit output port. It has active pull-up and pull-down transistors.
A0-A12, A15	20-7	Fourteen address lines used to address a complete 65K external address space. Note: A13 & A14 are sourced through PC6 & PC7 when in the Full Address Mode.
DB0-DB7	53-46	Eight bidirectional data bus lines used to transmit data to and from external memory.
SYNC	22	SYNC is a positive going signal for the full clock cycle whenever the CPU is performing an OP CODE fetch.
R/$\overline{W}$	40	Controls the direction of data transfer between the CPU and the external 65K address space. The signal is high when reading and low when writing.

3

SECTION 3
SYSTEM ARCHITECTURE

This section provides a functional description of the R6500/13. Functionally the R6500/13 consists of a CPU, both RAM and optional ROM memories, four 8-bit parallel I/O ports, a serial I/O port, dual counter/latch circuits, a mode control register, and an interrupt flag/enable dual register circuit. A block diagram of the system is shown in Figure 3-1.

NOTE

Throughout this document, unless specified otherwise, all memory or register address locations are specified in hexadecimal notation.

3.1 CPU LOGIC

The R6500/13 internal CPU is a standard 6502 configuration with an 8-bit Accumulator register, two 8-bit Index Registers (X and Y); an 8-bit Stack Pointer register, an ALU, a 16-bit Program Counter, and standard instruction register/decode and internal timing control logic.

3.1.1 Accumulator

The accumulator is a general purpose 8-bit register that stores the results of most arithmetic and logic operations. In addition, the accumulator usually contains one of the two data words used in these operations.

3.1.2 Index Registers

There are two 8-bit index registers, X and Y. Each index register can be used as a base to modify the address data program counter and thus obtain a new address—the sum of the program counter contents and the index register contents

When executing an instruction which specifies indirect addressing, the CPU fetches the op code and the address and modifies the address from memory by adding the index register to it prior to loading or storing the value of memory.

Indexing greatly simplifies many types of programs, especially those using data tables

3.1.3 Stack Pointer

The Stack Pointer is an 8-bit register. It is automatically incremented and decremented under control of the microprocessor to perform stack manipulation in response to either user instructions, an internal $\overline{IRQ}$ interrupt, or the external interrupt line $\overline{NMI}$. The Stack Pointer must be initialized by the user program.

The stack allows simple implementation of multiple level interrupts, subroutine nesting and simplification of many types of data manipulation. The JSR, BRK, RTI and RTS instructions use the stack and Stack Pointer.

The stack can be envisioned as a deck of cards which may be accessed only from the top. The address of a memory location is stored (or "pushed") onto the stack. Each time data are to be pushed onto the stack, the Stack Pointer is placed on the Address Bus, data are written into the memory location addressed by the Stack Pointer, and the Stack Pointer is decremented by 1. Each time data are read (or "pulled") from the stack, the Stack Pointer is incremented by 1. The Stack Pointer is then placed on the Address Bus and data are read from the memory location addressed by the Pointer.

The stack is located on zero page, i.e., memory locations 00FF-0040. After reset, which leaves the Stack Pointer indeterminate, normal usage calls for its initialization at 00FF.

3.1.4 Arithmetic And Logic Unit (ALU)

All arithmetic and logic operations take place in the ALU, including incrementing and decrementing internal registers (except the Program Counter) The ALU cannot store data for more than one cycle. If data are placed on the inputs to the ALU at the beginning of a cycle, the result is always gated into one of the storage registers or to external memory during the next cycle

Each bit of the ALU has two inputs. These inputs can be tied to various internal buses or to a logic zero, the ALU then generates the function (AND, OR, SUM, and so on) using the data on the two inputs.

3.1.5 Program Counter

The 16-bit Program Counter provides the addresses that are used to step the processor through sequential instructions in a program Each time the processor fetches an instruction from program memory, the lower (least significant) byte of the Program Counter (PCL) is placed on the low-order bits of the Address Bus and the higher (most significant) byte of the Program Counter (PCH) is placed on the high-order 8 bits of the Address Bus The Counter is incremented each time an instruction or data is fetched from program memory.

3.1.6 Instruction Register and Instruction Decode

Instructions are fetched from ROM or RAM and gated onto the Internal Data Bus. These instructions are latched into the Instruction Register, then decoded along with timing and interrupt signals to generate control signals for the various registers.

3.1.7 Timing Control

The Timing Control Logic keeps track of the specific instruction cycle being executed. This logic is set to T0 each time an instruction fetch is executed and is advanced at the beginning of each Phase One clock pulse for as many cycles as are required to complete the instruction. Each data transfer which takes place between the registers is caused by decoding the contents of both the instruction register and timing control unit.

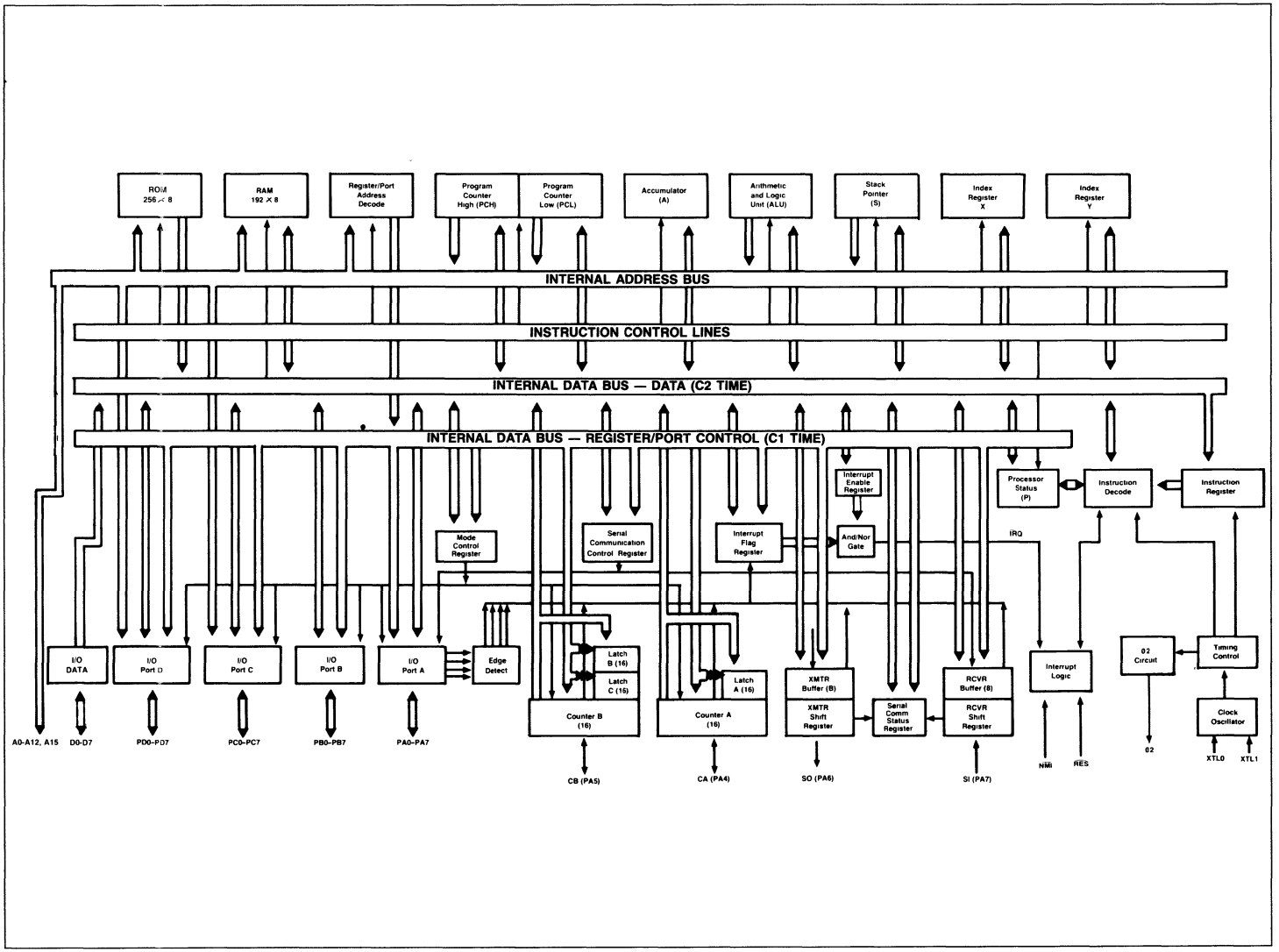


Figure 3-1. Detailed Block Diagram

3.1.8 Interrupt Logic

Interrupt logic controls the sequencing of three interrupts; $\overline{RES}$, $\overline{NMI}$ and $\overline{IRQ}$. $\overline{IRQ}$ is generated by any one of eight conditions: 2 Counter Overflows, 2 Positive Edge Detects, 2 Negative Edge Detects, and 2 Serial Port Conditions.

3.2 NEW INSTRUCTIONS

In addition to the standard R6502 instruction set, four new bit manipulation instructions have been added to the R6500/13. The added instructions and their format are explained in the following paragraphs. Refer to Appendix A for the Op Code mnemonic addressing matrix for these added instructions. The four added instructions do not impact the CPU processor status register.

3.2.1 Set Memory Bit (SMB m, Addr.)

This instruction sets to "1" one of the 8-bit data field specified by the zero page address (memory or I/O port). The first byte of the instruction specifies the SMB operation and one of eight bits to be set. The second byte of the instruction designates address (0-255) of the byte to be operated upon.

3.2.2 Reset Memory Bit (RMB m, Addr.)

This instruction is the same operation and format as SMB instruction except a reset to "0" of the bit results.

3.2.3 Branch On Bit Set Relative (BBS m, Addr, DEST)

This instruction tests one of eight bits designated by a 3-bit immediate field within the first byte of the instruction. The second byte is used to designate the address of the byte to be tested within the zero page address range (memory or I/O ports). The third byte of the instruction is used to specify the 8-bit relative address to which the instruction branches if the bit tested is a "1". If the bit tested is not set, the next sequential instruction is executed.

3.2.4 Branch On Bit Reset Relative (BBR m, Addr, DEST)

This instruction is the same operation and format as the BBS instruction except that a branch takes place if the bit tested is a "0".

3.3 READ-ONLY-MEMORY (ROM)

The optional ROM consists of 256 bytes mask programmable memory with an address space from 7F00 to 7FFF. ROM locations FFFA to FFFF are assigned for interrupt vectors. The reset vector can be optionally at 7FFE or FFFC.

The R6511Q has no ROM and its Reset vector is at FFFC.

3.4 RANDOM ACCESS MEMORY (RAM)

The RAM consists of 192 bytes of read/write memory with an assigned page zero address of 0040 through 00FF. The R6500/13 provides a separate power pin (V_{RR}) which may be used for standby power for 32 bytes located at 0040-005F. In the event of the loss of V_{CC} power, the lowest 32 bytes of RAM data will be retained if standby power is supplied to the V_{RR} pin. If the RAM data retention is not required then V_{RR} must be connected to V_{CC}. During operation V_{RR} must be at the V_{CC} level.

For the RAM to retain data upon loss of V_{CC}, V_{RR} must be supplied within operating range and $\overline{RES}$ must be driven low at least eight Ø2 clock pulses before V_{CC} falls out of operating range. $\overline{RES}$ must then be held low while V_{CC} is out of operating range and until at least eight Ø2 clock cycles after V_{CC} is again within operating range and the internal Ø2 oscillator is stabilized. V_{RR} must remain within V_{CC} operating range during normal operation. When V_{CC} is out of operating range, V_{RR} must remain within the V_{RR} retention range in order to retain data. Figure 3.2 shows typical waveforms.

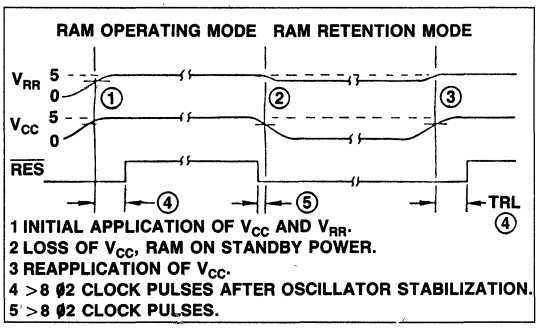


Figure 3-2. Data Retention Timing

3.5 CLOCK OSCILLATOR

The R6511Q has been configured for a crystal oscillator, a divide by 2 countdown network, and for Master Mode Operation.

Three customer selectable mask options are available for controlling the R6500/13 timing. The R6500/13 can be ordered with a *crystal or RC* oscillator, a *divide by 2 or divide by 4* countdown network and for *clock master mode or clock slave mode* operation.

For 2MHz interval operation the divide-by-2 options must be specified.

A reference frequency can be generated with the on-chip oscillator using either an external crystal or an external resistor depending on the mask option selected. The oscillator reference frequency passes through an internal countdown network (divide by 2 or divide by 4 option) to obtain the internal operating frequency (see Figures 3-3a and 3-3b). The external crystal generated reference frequency is a preferred method since the resistor method can have tolerances approaching 50%.

Internal timing can also be controlled by driving the XTLI pin with an external frequency source. Figure 3-3c shows typical connections. If XTLO is left floating, the external source is divided by the internal countdown network However, if XTLO is tied to V_{SS}, the internal countdown network is bypassed causing the chip to operate at the frequency of the external source.

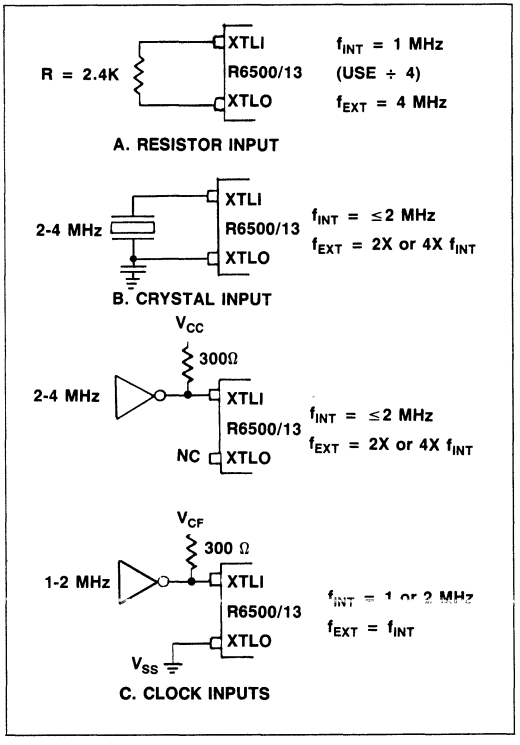


Figure 3-3. Clock Oscillator Input Options

The operation escribed above assumed a CLOCK MASTER MODE mask option. In this mode a frequence source (crystal, RC network, or external source) must be applied to the XTLI and XTLO pins.

Note:
When operating at a 1 MHz internal frequency place a 15-22 pt capacitor between XTLO and GND.

Ø2 is a buffered output signal which closely approximates the internal timing. When a common external source is used to drive multiple devices the internal timing between devices as well as their Ø2 outputs will be skewed in time. If skewing represents a system problem it can be avoided by the Master/Slave connection and options shown in Figure 3-4.

One R6500/13 is operated in the CLOCK MASTER MODE and a second in the CLOCK SLAVE MODE. Mask options in the SLAVE unit convert to Ø2 signal into a clock input pin which is tightly coupled to the internal timing generator. As a result the internal timing of the MASTER and SLAVE units are synchronized with minimum skew. If the Ø2 signal to the SLAVE unit is inverted, the MASTER and SLAVE UNITS WILL OPERATE OUT OF PHASE. This approach allows the two devices to share external memory using cycle stealing techniques.

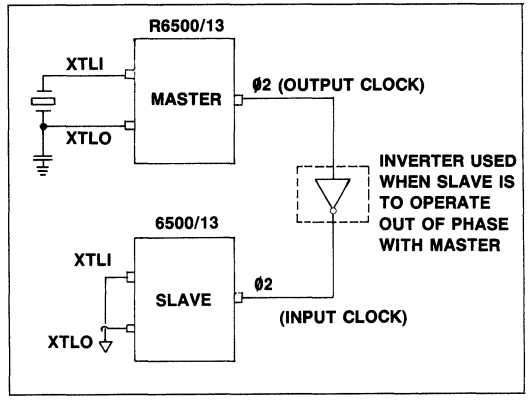


Figure 3-4. Master/Slave Connections

3.6 MODE CONTROL REGISTER (MCR)

The Mode Control Register contains control bits for the multifunction I/O ports and mode select bits for Counter A and Counter B. Its setting, along with the setting of the Serial Communications Control Register (SCCR), determines the basic configuration of the R6500/13 in any application. Initializing this register is one of the first actions of any software program. The Mode Control Register bit assignment is shown in Figure 3-5.

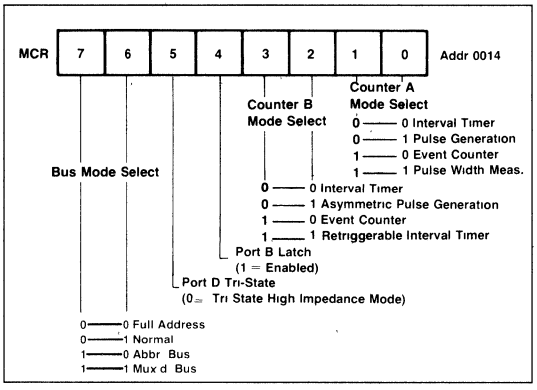


Figure 3-5. Mode Control Register

The use of Counter A Mode Select is shown in Section 6.1.

The use of Counter B Mode Select is shown in Section 6.2.

The use of Port B Latch Enable is shown in Section 4.4.

The use of Port D in Tri-State Enable is shown in Section 4.6.

The use of Bus Mode Select is shown in Section 4.5 and 4.6

3.7 INTERRUPT FLAG REGISTER (IFR) AND INTERRUPT ENABLE REGISTER (IER)

An $\overline{IRQ}$ interrupt request can be initiated by any or all of eight possible sources. These sources are all capable of being enabled or disabled by the use of the appropriate interrupt enabled bits in the Interrupt Enable Register (IER). Multiple simultaneous interrupts cause the $\overline{IRQ}$ interrupt request to remain active until all interrupting conditions have been serviced and cleared.

The Interrupt Flag Register contains the information that indicates which I/O or counter needs attention. The contents of the Interrupt Flag Register may be examined at any time by reading at address: 0011. Edge detect IFR bits may be cleared by executing a RMB instruction at address location 0010. The RMB X, (0010) instruction reads FF, modifies bit X to a "0", and writes the modified value at address location 0011. In this way IFR bits set to a "1" after the read cycle of a Read-Modify-Write instruction (such as RMB) are protected from being cleared. A logic "1" is ignored when writing to edge detect IFR bits.

Each IFR bit has a corresponding bit in the Interrupt Enable Register which can be set to a "1" by writing a "1" in the respective bit position at location 0012. Individual IER bits may be cleared by writing a "0" in the respective bit position, or by $\overline{RES}$. If set to a "1", an IRQ will be generated when the corresponding IFR bit becomes true. The Interrupt Flag Register and Interrupt Enable Register bit assignments are shown in Figure 3-6 and the functions of each bit are explained in Table 3-1.

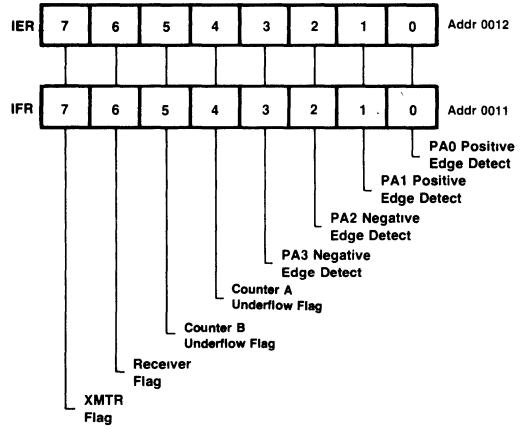


Figure 3-6. Interrupt Enable and Flag Registers

Table 3-1. Interrupt Flag Register Bit Codes

Bit Code	Function
IFR 0	PA0 Positive Edge Detect Flag—Set to a "1" when a positive going edge is detected on PA0. Cleared by RMB O (0010) instruction or by $\overline{RES}$
IFR 1	PA1 Positive Edge Detect Flag—Set to a 1 when a positive going edge is detected on PA1 Cleared by RMB 1 (0010) instruction or by $\overline{RES}$
IFR 2	PA2 Negative Edge Detect Flag—Set to a 1 when a negative going edge is detected on PA2 Cleared by RMB 2 (0010) instruction or by $\overline{RES}$
IFR 3	PA3 Negative Edge Detect Flag—Set to 1 when a negative going edge is detected on PA3. Cleared by RMB 3 (0010) instruction or by $\overline{RES}$
IFR 4	Counter A Underflow Flag—Set to a 1 when Counter A underflow occurs. Cleared by reading the Lower Counter A at location 0018, by writing to address location 001A, or by $\overline{RES}$.
IFR 5	Counter B Underflow Flag—Set to a 1 when Counter B underflow occurs. Cleared by reading the Lower Counter B at location 001C, by writing to address location 001E, or by $\overline{RES}$.
IFR 6	Receiver Interrupt Flag—Set to a 1 when any of the Serial Communication Status Register bits 0 through 3 is set to a 1. Cleared when the Receiver Status bits (SCSR 0-3) are cleared or by $\overline{RES}$.
IFR 7	Transmitter Interrupt Flag—Set to a 1 when SCSR 6 is set to a 1 while SCSR 5 is a 0 or SCSR 7 is set to a 1. Cleared when the Transmitter Status bits (SCSR 6 & 7) are cleared or by $\overline{RES}$

3.8 PROCESSOR STATUS REGISTER

The 8-bit Processor Status Register, shown in Figure 3-7, contains seven status flags. Some of these flags are controlled by the user program; others may be controlled both by the user's program and the CPU. The R6502 instruction set contains a number of conditional branch instructions which are designed to allow testing of these flags. Each of the eight processor status flags is described in the following sections.

3.8.1 Carry Bit (C)

The Carry Bit (C) can be considered as the ninth bit of an arithmetic operation. It is set to logic 1 if a carry from the eighth bit has occurred or cleared to logic 0 if no carry occurred as the result of arithmetic operations.

The Carry Bit may be set or cleared under program control by use of the Set Carry (SEC) or Clear Carry (CLC) instruction, respectively. Other operations which affect the Carry Bit are ADC, ASL, CMP, CPX, CPY, LSR, PLP, ROL, ROR, RTI, and SBC.

3.8.2 Zero Bit (Z)

The Zero Bit (Z) is set to logic 1 by the CPU during any data movement or calculation which sets all 8 bits of the result to zero. This bit is cleared to logic 0 when the resultant 8 bits of a data movement or calculation operation are not all zero. The R6500 instruction set contains no instruction to specifically set or clear the Zero Bit. The Zero Bit is, however, affected by the following instructions; ADC, AND, ASL, BIT, CMP, CPX, CPY, DEC, DEX, DEY, EOR, INC, INX, INY, LDA, LDX, LDY, LSR, ORA, PLA, PLP, ROL, ROR, RTI, SBC, TAX, TAY, TXA, TSX, and TYA.

3.8.3 Interrupt Disable Bit (I)

The Interrupt Disable Bit (I) is used to control the servicing of an interrupt request ($\overline{IRQ}$). If the I Bit is reset to logic 0, the $\overline{IRQ}$ signal will be serviced. If the bit is set to logic 1, the $\overline{IRQ}$ signal will be ignored. The CPU will set the Interrupt Disable Bit to logic 1 if a RESET ($\overline{RES}$), $\overline{IRQ}$, or Non-Maskable Interrupt ($\overline{NMI}$) signal is detected.

The I bit is cleared by the Clear Interrupt Mask Instruction (CLI) and is set by the Set Interrupt Mask Instruction (SEI). This bit is set by the BRK Instruction. The Return from Interrupt (RTI) and Pull Processor Status (PLP) instructions will also affect the I bit.

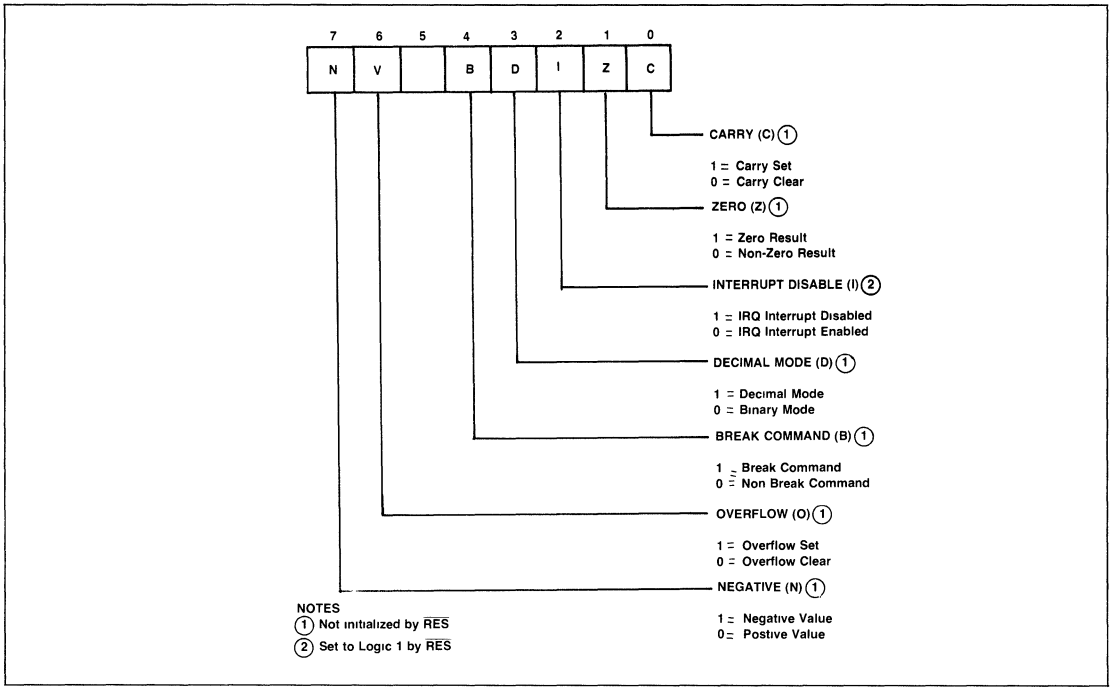


Figure 3-7. Processor Status Register

3.8.4 Decimal Mode Bit (D)

The Decimal Mode Bit (D) is used to control the arithmetic mode of the CPU. When this bit is set to logic 1, the adder operates as a decimal adder. When this bit is cleared to logic 0, the adder operates as a straight binary adder. The adder mode is controlled only by the programmer. The Set Decimal Mode (SED) instruction will set the D bit; the Clear Decimal Mode (CLD) instruction clears it. The PLP and RTI instructions also affect the Decimal Mode Bit.

CAUTION

The Decimal Mode Bit will either set or clear in an unpredictable manner upon power application. This bit must be initialized to the desired state by the user program or erroneous results may occur.

3.8.5 Break Bit (B)

The Break Bit (B) is used to determine the condition which caused the $\overline{IRQ}$ service routine to be entered. If the $\overline{IRQ}$ service routine was entered because the CPU executed a BRK command, the Break Bit will be set to logic 1. If the $\overline{IRQ}$ routine was entered as the result of an $\overline{IRQ}$ signal being generated, the B bit will be cleared to logic 0. There are no instructions which can set or clear this bit.

3.8.6 Overflow Bit (V)

The Overflow Bit (V) is used to indicate that the result of a signed, binary addition, or subtraction, operation is a value that cannot be contained in seven bits ($-128 \leq n \leq 127$). This indicator only has meaning when signed arithmetic (sign and seven magnitude bits) is performed. When the ADC or SBC instruction is performed, the Overflow Bit is set to logic 1 if the polarity of the sign bit (bit 7) is changed because the result exceeds +127 or −128; otherwise the bit is cleared to logic 0. The V bit may also be cleared by the programmer using a Clear Overflow (CLV) instruction.

The Overflow Bit may also be used with the BIT instruction. The BIT instruction—which may be used to sample interface devices—allows the overflow flag to reflect the condition of bit 6 in the sampled field. During a BIT instruction the Overflow Bit is set equal to the content of the bit 6 on the data tested with BIT instruction. When used in this mode, the overflow has nothing to do with signed arithmetic, but is just another sense bit for the microprocessor. Instructions affecting the V flag are ADC, BIT, CLV, PLP, RTI and SBC.

3.8.7 Negative Bit (N)

The Negative Bit (N) is used to indicate that the sign bit (bit 7) in the resulting value of a data movement or data arithmetic operation is set to logic 1. If the sign bit is set to logic 1, the resulting value of the data movement or arithmetic operation is negative; if the sign bit is cleared, the result of the data movement or arithmetic operation is positive. There are no instructions that set or clear the Negative Bit since the Negative Bit represents only the status of a result. The instructions that effect the state of the Negative Bit are: ADC, AND, ASL, BIT, CMP, CPX, CPY, DEC, DEX, DEY, EOR, INC, INX, INY, LDA, LDX, LDY, LSR, ORA, PLA, PLP, ROL, ROR, RTI, SBC, TAX, TAY, TSX, TXA, and TYA.

SECTION 4
PARALLEL INPUT/OUTPUT PORTS & BUS MODES

The devices have 32 I/O lines grouped into four 8-bit ports (PA, PB, PC, and PD). Ports A through C may be used either for input or output individually or in groups of any combination. Port D may be used as all inputs or all outputs.

Multifunction I/O's such as Port A and Port C are protected from normal port I/O instructions when they are programmed to perform a multiplexed function.

Internal pull-up resistors (FET's with an impedance range of $3K \leq R_L \leq 12K$ ohm) are provided on all port pins except Port D. A mask option to delete the internal pull-ups in 8-bit port groups is available.

The direction of the 32 I/O lines are controlled by four 8-bit port registers located in page zero. This arrangement provides quick programming access using simple two-byte zero page address instructions. There are no direction registers associated with the I/O ports, thus simplifying I/O handling. The I/O addresses are shown in Table 4-1. Appendix E.6 shows the I/O Port Timing.

Table 4-1. I/O Port Addresses

Port	Address
A	0000
B	0001
C	0002
D	0003

4.1 INPUTS

Inputs for Ports A, B, and C are enabled by loading logic 1 into all I/O port register bit positions that are to correspond to I/O input lines. A low (<0.8V) input signal will cause a logic 0 to be read when a read instruction is issued to the port register. A high (>2.0V) input will cause a logic 1 to be read. An $\overline{RES}$ signal forces all I/O port registers to logic 1 thus initially treating all I/O lines as inputs.

Port D may only be all inputs or all outputs. All inputs is selected by setting bit 5 of the Mode Control Register (MCR5) to a "0".

The status of the input lines can be interrogated at any time by reading the I/O port addresses. Note that this will return the actual status of the input lines, not the data written into the I/O port registers.

Read/Modify/Write instructions can be used to modify the operation of PA, PB, PC, & PD. During the Read cycle of a Read/Modify/Write instruction the Port I/O register is read. For all other read instructions the port input lines are read. Read/Modify/Write instructions are: ASL, DEC, INC, LSR, RMB, ROL, ROR, and SMB.

4.2 OUTPUTS

Outputs for Ports A thru D are controlled by writing the desired I/O line output states into the corresponding I/O port register bit positions. A logic 1 will force a high (>2.4V) output while a logic 0 will force a low (<0.4V) output.

Port D all outputs is selected by setting MCR5 to a "1".

4.3 Port A (PA)

Port A can be programmed via the Mode Control Register (MCR) and the Serial Communications Control Register (SCCR) as a standard parallel 8-bit, bit independent, I/O port or as serial channel I/O lines, counter I/O lines, or an input data strobe for the Port B input latch option. Table 4-2 tabulates the control and usage of Port A.

In addition to their normal I/O functions, PA0 and PA1 can detect positive going edges and PA2 and PA3 can detect negative going edges. A proper transition on these pins will set a corresponding status bit in the IFR and generate an interrupt request if the respective Interrupt Enable Bit is set. The maximum rate at which an edge can be detected is one-half the $\phi 2$ clock rate. Edge detection timing is shown in Appendix E.5.

Table 4-2. Port A Control & Usage

	PA0 I/O		PORT B LATCH MODE	
	MCR4 = 0		MCR4 = 1	
	SIGNAL		SIGNAL	
	NAME	TYPE	NAME	TYPE
PA0 (2) PIN 39	PA0	I/O	PORT B LATCH STROBE	INPUT (1)

	PA1-PA3 I/O	
	SIGNAL	
	NAME	TYPE
PA1 (2) PIN 38	PA1	I/O
PA2 (3) PIN 37	PA2	I/O
PA3 (3) PIN 36	PA3	I/O

	PA4 I/O		COUNTER A I/O			
	MCR0 = 0 MCR1 = 0 SCCR7 = 0 RCVR S/R MODE = 0 (4) (5)		MCR0 = 1 MCR1 = 0 SCCR7 = 0 RCVR S/R MODE = 0 (4)		SCCR7 = 0 SCCR6 = 0 MCR1 = 1	
	SIGNAL		SIGNAL		SIGNAL	
	NAME	TYPE	NAME	TYPE	NAME	TYPE
PA4 PIN 35	PA4	I/O	CNTA	OUTPUT	CNTA	INPUT (1)
	SERIAL I/O SHIFT REGISTER CLOCK					
	SCCR7 = 1 SCCR5 = 1		RCVR S/R MODE = 1 (4)			
	SIGNAL		SIGNAL			
	NAME	TYPE	NAME	TYPE		
	XMTR CLOCK	OUTPUT	RCVR CLOCK	INPUT (1)		

	PA5 I/O		COUNTER B I/O			
	MCR3 = 0 MCR2 = 0		MCR3 = 0 MCR2 = 1		MCR3 = 1 MCR2 = X	
	SIGNAL		SIGNAL		SIGNAL	
	NAME	TYPE	NAME	TYPE	NAME	TYPE
PA5 PIN 34	PA5	I/O	CNTB	OUTPUT	CNTB	INPUT (1)

	PA6 I/O		SERIAL I/O XMTR OUTPUT	
	SCCR7 = 0		SCCR7 = 1	
	SIGNAL		SIGNAL	
	NAME	TYPE	NAME	TYPE
PA6 PIN 33	PA6	I/O	XMTR	OUTPUT

	PA7 I/O		SERIAL I/O RCVR INPUT	
	SCCR6 = 0		SCCR6 = 1	
	SIGNAL		SIGNAL	
	NAME	TYPE	NAME	TYPE
PA7 PIN 32	PA7	I/O	RCVR	INPUT (1)

(1) Hardware Buffer Float
(2) Positive Edge Detect
(3) Negative Edge Detect
(4) RCVR S/R Mode = 1 when SCCR6 • $\overline{\text{SCCR5}}$ • SCCR4 = 1
(5) For the following mode combinations PA4 is available as an input only pin:
SCCR7•SCCR6•SCCR5•MCR1
+ SCCR7•SCCR6•7SCCR4•MCR1
+ SCCR7•SCCR6•SCCR5
+ SCCR7•SCCR5C•SCCR4.

4.4 PORT B (PB)

Port B can be programmed as an 8-bit, bit-independent I/O port. It has a latched input capability which may be enabled or disabled via the Mode Control Register (MCR). Table 4-3 tabulates the control and usage of Port B. An Input Data Strobe signal must be provided thru PA0 when Port B is programmed to be used with latched input option. Input data latch timing for Port B is shown in Appendix E.5.

Table 4-3. Port B Control & Usage

		I/O Mode		Latch Mode	
		MCR4 = 0		MCR4 = 1 (2)	
		Signal		Signal	
Pin #	Pin Name	Name	Type (1)	Name	Type
31	PB0	PB0	I/O	PB0	INPUT
30	PB1	PB1	I/O	PB1	INPUT
29	PB2	PB2	I/O	PB2	INPUT
28	PB3	PB3	I/O	PB3	INPUT
27	PB4	PB4	I/O	PB4	INPUT
26	PB5	PB5	I/O	PB5	INPUT
25	PB6	PB6	I/O	PB6	INPUT
24	PB7	PB7	I/O	PB7	INPUT

(1) Resistive Pull-Up, Active Buffer Pull-Down
(2) Input data is stored in Port B latch by PA0 Pulse

4.5 PORT C (PC)

Port C can be programmed as an I/O port, as part of the full address bus, and, in conjunction with Port D, as an abbreviated bus, or as a multiplexed bus. When operating in the Full Address Mode PC6 and PC7 serve as A13 and A14 with PC0-PC5 operating as normal I/O pins. When used in the abbreviated or multiplexed bus modes, PC0-PC7 function as A0-A3, A12, R/W, A13, and $\overline{EMS}$, respectively, as shown in Table 4-4. $\overline{EMS}$ (External Memory Select) is asserted (low) whenever the internal processor accesses memory area between 0100 and 3FFF. (See Memory Map, Appendix B). The leading edge of $\overline{EMS}$ may be used to strobe the eight address lines multiplexed on Port D in the Multiplexed Bus Mode. See Appendices E.3 through E.5 for Port C timing.

4.6 PORT D (PD)

Port D can be programmed as an I/O Port, an 8-bit tri-state data bus, or as a multiplexed bus. Mode selection for Port D is made by the Mode Control Register (MCR). The Port D output drivers can be selected as tri-state drivers by setting bit 5 of the MCR to 1 (one). Table 4-5 shows the necessary settings for the MCR to achieve the various modes for Port D. When Port D is selected to operate in the Abbreviated Mode PD0-PD7 serves as data register bits D0-D7. When Port D is selected to operate in the Multiplexed Mode data bits D0 through D7 are time multiplexed with address bits A4 through A11, respectively. Refer to the Memory Maps (Appendix C) for Abbreviated and Multiplexed memory assignments. See Appendices E.3 through E.5 for Port D timing.

4.7 BUS MODES

A special attribute of Port C and Port D is their capability to be configured via the Mode Control Register (see Section 3.6) into four different modes.

In the Full Address Mode, the separate address and data bus are used in conjunction with PC6 and PC7, which automatically provide A13 and A14. The remaining ports perform the normal I/O function.

In the I/O Bus Mode all ports serve as I/O. The address and data bus are still functional but without A13 and A14. Since the internal RAM and registers are in the OOXX location, A15 can be used for chip select and A0-A12 used for selecting 8K of external memory. Thus, the device can be used to emulate the R6500/11 in the Normal Bus Mode.

In the Abbreviated Bus Mode, the address and data lines can be used as in the I/O Bus Mode to emulate the R6500/11. Port C and Port D are automatically transformed into an abbreviated address bus and control signals (Port C) and a bidirectional data bus (Port D). 64 Peripheral addresses can be selected. In general usage, these 64 addresses would be distributed to several external I/O devices such as R6522 and R6520, etc., each of which may contain more than one unique address.

In the Multiplexed Bus Mode, the operation is similar to the Abbreviated Mode except that a full 16K of external addresses are provided. Port C provides the lower addresses and control signals. Port D multiplexes functions. During the first half of the cycle it contains the remaining necessary 8 address bits for 16K; during the second half of the cycle it contains a bidirectional data bus. The address bits appearing on Port D must be latched into an external holding register. The leading edge of $\overline{EMS}$, which indicates that the bus function is active, may be used for this purpose.

Figures 4-1a thru 4-1d show the possible configurations of the four bus modes. Figure 4-2 shows a memory map of the port as a function of the Bus Mode and further shows which addresses are active or inactive on each of the three possible buses.

Table 4-4. Port C Control & Usage

		Full Address Mode		I/O Mode		Abbreviated Mode		Multiplexed Mode	
		MCR7 = 0 MCR6 = 0		MCR7 = 0 MCR6 = 1		MCR7 = 1 MCR6 = 0		MCR7 = 1 MCR6 = 1	
		Signal		Signal		Signal		Signal	
Pin #	Pin Name	Name	Type	Name	Type (1)	Name	Type (2)	Name	Type (2)
54	PC0	PC0	I/O (1)	PC0	I/O	A0	OUTPUT	A0	OUTPUT
55	PC1	PC1	I/O (1)	PC1	I/O	A1	OUTPUT	A1	OUTPUT
56	PC2	PC2	I/O (1)	PC2	I/O	A2	OUTPUT	A2	OUTPUT
57	PC3	PC3	I/O (1)	PC3	I/O	A3	OUTPUT	A3	OUTPUT
58	PC4	PC4	I/O (1)	PC4	I/O	A12	OUTPUT	A12	OUTPUT
59	PC5	PC5	I/O (1)	PC5	I/O	$R\overline{W}$	OUTPUT	$R\overline{W}$	OUTPUT
60	PC6	A13	OUTPUT (2)	PC6	I/O	A13	OUTPUT	A13	OUTPUT
61	PC7	A14	OUTPUT (2)	PC7	I/O	$\overline{EMS}$	OUTPUT	$\overline{EMS}$	OUTPUT

(1) Resistive Pull-Up, Active Buffer Pull-Down
(2) Active Buffer Pull-Up and Pull-Down

3

Table 4-5. Port D Control & Usage

		I/O Modes				Abbreviated Mode		Multiplexed Mode			
		MCR7 = 0 MCR6 = X MCR5 = 0		MCR7 = 0 MCR6 = X MCR5 = 1		MCR7 = 1 MCR6 = 0 MCR5 = 1		MCR7 = 1 MCR6 = 1 MCR5 = 1			
		Signal		Signal		Signal		Signal		Signal	
								Ø2 Low		Ø2 High	
Pin #	Pin Name	Name	Type (1)	Name	Type (2)	Name	Type (3)	Name	Type (2)	Name	Type (3)
62	PD0	PD0	INPUT	PD0	OUTPUT	DATA0	I/O	A4	OUTPUT	DATA0	I/O
63	PD1	PD1	INPUT	PD1	OUTPUT	DATA1	I/O	A5	OUTPUT	DATA1	I/O
64	PD2	PD2	INPUT	PD2	OUTPUT	DATA2	I/O	A6	OUTPUT	DATA2	I/O
1	PD3	PD3	INPUT	PD3	OUTPUT	DATA3	I/O	A7	OUTPUT	DATA3	I/O
2	PD4	PD4	INPUT	PD4	OUTPUT	DATA4	I/O	A8	OUTPUT	DATA4	I/O
3	PD5	PD5	INPUT	PD5	OUTPUT	DATA5	I/O	A9	OUTPUT	DATA5	I/O
4	PD6	PD6	INPUT	PD6	OUTPUT	DATA6	I/O	A10	OUTPUT	DATA6	I/O
5	PD7	PD7	INPUT	PD7	OUTPUT	DATA7	I/O	A11	OUTPUT	DATA7	I/O

(1) Tri-State Buffer is in High Impedance Mode
(2) Tri-State Buffer is in Active Mode
(3) Tri-State Buffer is in Active Mode only during the phase 2 portion of a Write Cycle

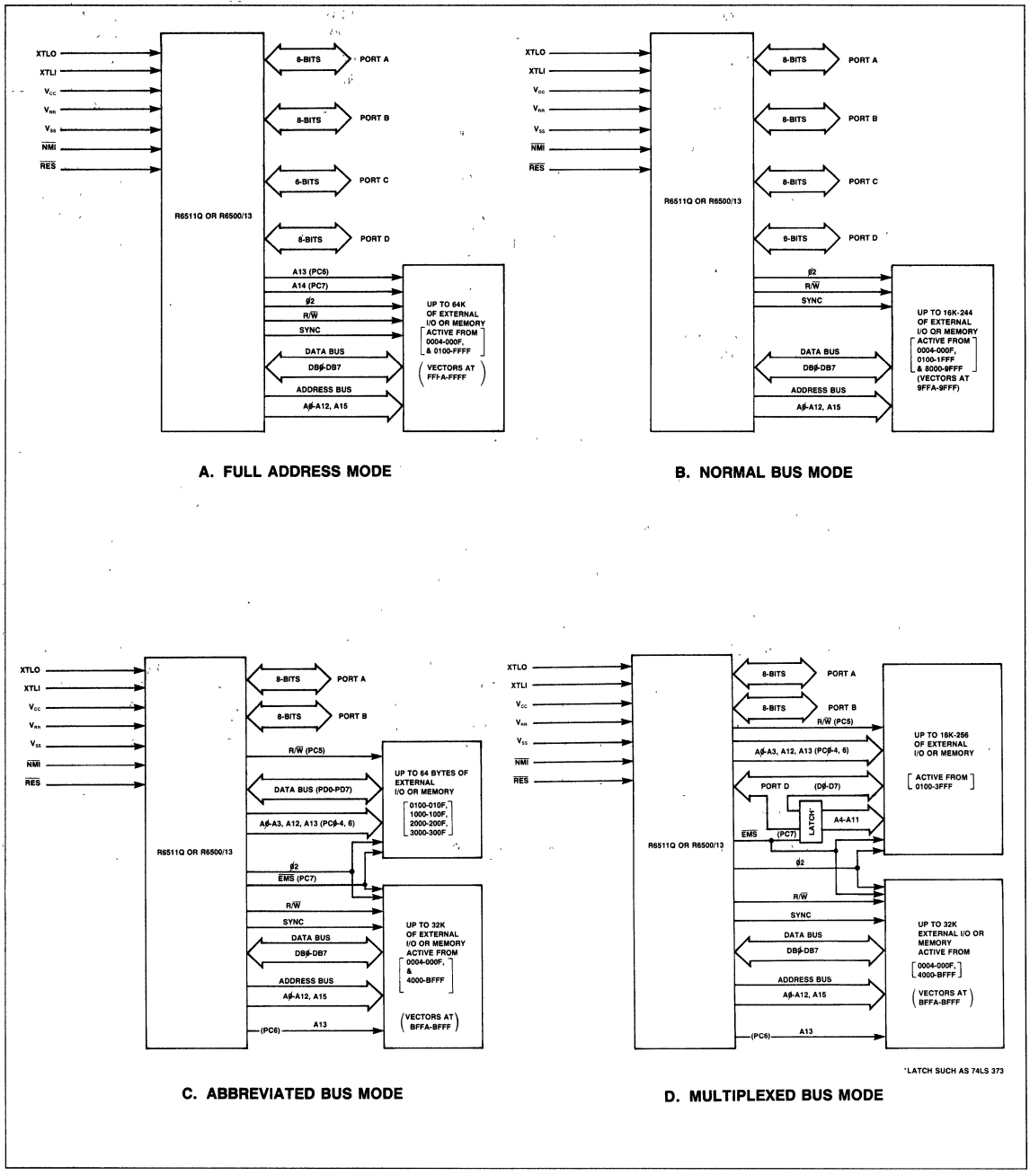


Figure 4-1. Bus Mode Configurations

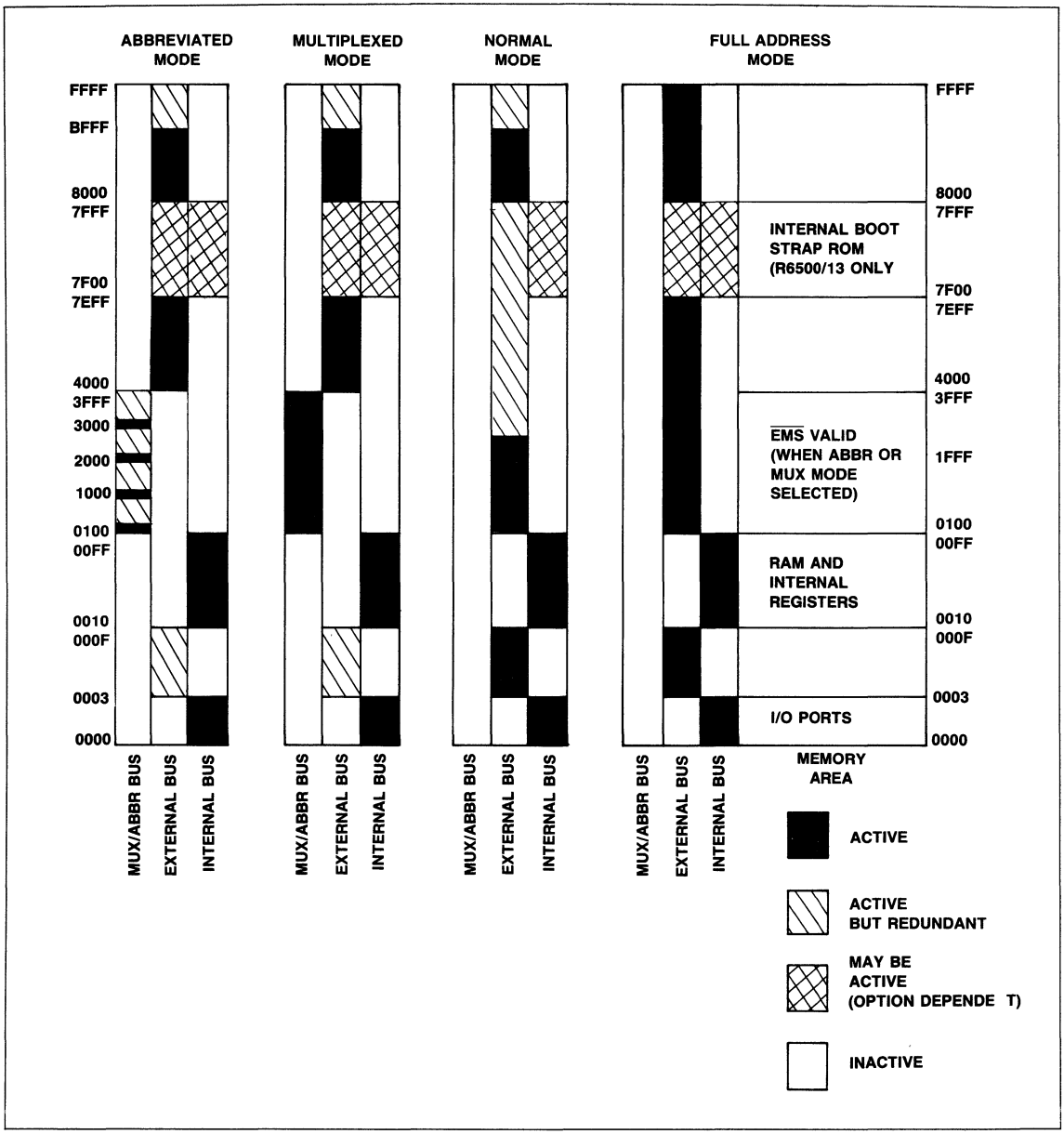


Figure 4-2. Memory Map

SECTION 5
SERIAL INPUT/OUTPUT CHANNEL

The device provides a full duplex Serial I/O channel with programmable bit rates and operating modes. The serial I/O functions are controlled by the Serial Communication Control Register (SCCR). The SCCR bit assignment is shown in Figure 5-1. The serial bit rate is determined by Counter A for all modes except the Receiver Shift Register (RCVR S/R) mode for which an external shift clock must be provided. The maximum data rate using the internal clock is 62.5K bits per second (at $\phi 2$ = 1 MHZ). The transmitter (XMTR) and receiver (RCVR) can be independently programmed to operate in different modes and can be independently enabled or disabled.

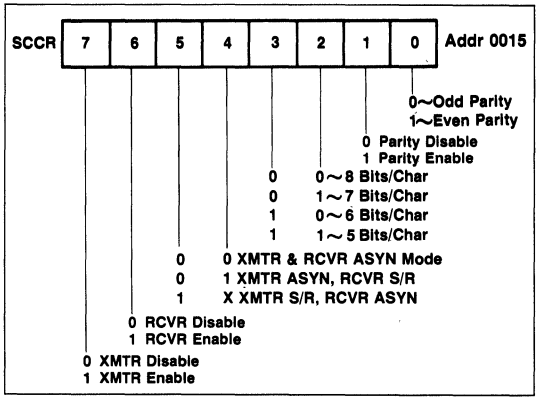


Figure 5-1. Serial Communication Control Register

Except for the Receiver Shift Register Mode (RCVR S/R), all XMTR and RCVR bit rates will occur at one sixteenth of the Counter A interval timer rate. Counter A is forced into an interval timer mode whenever the serial I/O is enabled in a mode requiring an internal clock.

Whenever Counter A is required as a timing source it must be loaded with the hexadecimal code that selects the data rate for the serial I/O Port. Refer to Counter A (paragraph 6.1) for a table of hexadecimal values to represent the desired data rate.

5.1 TRANSMITTER OPERATION (XTMR)

The XTMR operation and the transmitter related control/status functions are enabled by bit 7 of the Serial Communications Control Register (SCCR). The transmitter, when in the Asynchronous (ASYN) mode, automatically adds a start bit, one or two stop bits, and, when enabled, a parity bit to the transmitted data. A word of transmitted data (in asynchronous parity mode) can have 5, 6, 7, or 8 bits of data. The nine data modes are shown in Figure 5-2. When parity is disabled, the 5, 6, 7 or 8 bits of data are terminated with two stop bits.

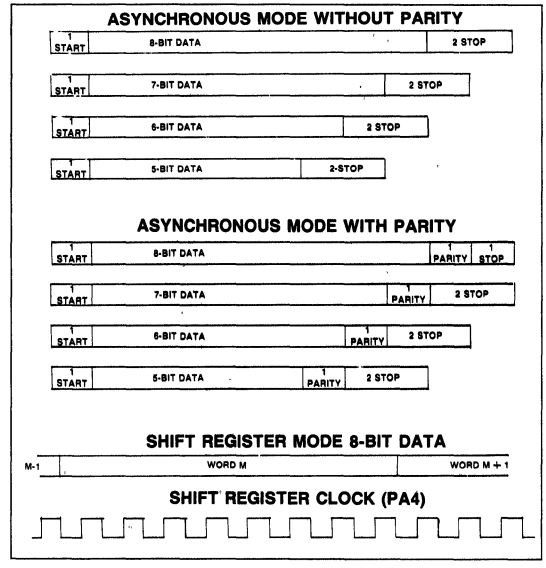


Figure 5-2. SIO Data Modes

In the S/R mode, eight data bits are always shifted out. Bits/character and parity control bits are ignored. The serial data is shifted out via the SO output (PA6) and the shift clock is available at the CA (PA4) pin. When the transmitter underruns in the S/R mode the SO output and shift clock are held in a high state.

The XMTR Interrupt Flag bit (IFR7) is controlled by Serial Communication Status Register bits SCSR5, SCSR6 and SCSR7.

$$IFR7 = SCSR6\ (\overline{SCSR5} + SCSR7)$$

5.2 RECEIVER OPERATION (RCVR)

The receiver and its selected control and status functions are enabled when SCCR-6 is set to a "1." In the ASYN mode, data format must have a start bit, the appropriate number of data bits, a parity bit (if enabled), and one stop bit. Refer to paragraph 5.1 for a diagram of bit allocations. The receiver bit period is divided into 8 sub-intervals for internal synchronization. The receiver bit stream is synchronized by the start bit and a strobe signal is generated at the approximate center of each incoming bit. Refer to Figure 5-3 for ASYN Receive Data Timing. The character assembly process does not start if the start bit signal is less than one-half the bit time after a low level is detected on the Receive Data Input. Framing error, over-run, and parity error conditions or a RCVR Data Register Full will set the appropriate status bits. Any of the above conditions will cause an Interrupt Request if the Receiver Interrupt Enable bit is set to logic 1.

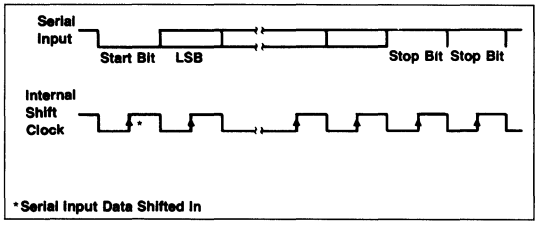


Figure 5-3. ASYN Receive Data Timing

In the S/R mode, an external shift clock must be provided at CA (PA4) pin along with 8 bits of serial data (LSB first) at the SI input (PA7). The maximum data rate using an external shift clock is one-eighth the internal clock rate. Refer to Figure 5-4 for S/R Mode Timing.

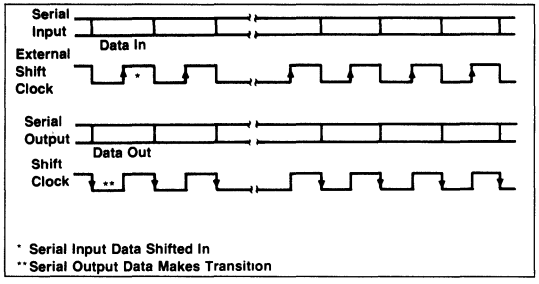


Figure 5-4. S/R Mode Timing

A RCVR interrupt (IFR6) is generated whenever any of SCSR0-3 are true.

5.3 SERIAL COMMUNICATION STATUS REGISTER (SCSR)

The Serial Communication Status Register (SCSR) holds information on various communication error conditions, status of the transmitter and receiver data registers, a transmitter end-of-transmission condition, and a receiver idle line condition (Wake-Up Feature). The SCSR bit assignment is shown in Figure 5-5. Bit assignments and functions of the SCSR are as follows:

SCSR 0: *Receiver Data Register Full*—Set to a logic 1 when a character is transferred from the Receiver Shift Register to the Receiver Data Register. This bit is cleared by reading the Receiver Data Register, or by $\overline{RES}$ and is disabled if SCCR 6 = 0. The SCSR 0 bit will not be set to a logic 1 if the received data contains an error condition; instead, a corresponding error bit will be set to a logic 1.

SCSR 1: *Over-Run Error*—Set to a logic 1 when a new character is transferred from the Receiver Shift Register with the last character still in the Receiver Data Register. This bit is cleared by reading the Receiver Data Register or by $\overline{RES}$.

SCSR 2: *Parity Error*—Set to logic 1 when the RCVR is in the ASYN Mode, Parity Enable bit is set, and the received data has a parity error. This bit is cleared by reading the Receiver Data Register or by $\overline{RES}$.

SCSR 3: *Framing Error*—Set to a logic 1 when the received data contains a zero bit after the last data or parity bit in the stop bit slot. Cleared by reading the Receiver Data Register or by $\overline{RES}$ (ASYN Mode only).

SCSR 4. *Wake-Up*—Set to a logic 1 by writing a "1" in bit 4 of address. 0016. The Wake-Up bit is cleared by $\overline{RES}$ or when the receiver detects a string of ten consecutive 1's. When the Wake-Up bit is set SCSR0 through SCSR3 are inhibited.

SCSR 5: *End of Transmission*—Set to a logic 1 by writing a "1" in bit position 5 of address: 0016. The End of Transmission bit is cleared by $\overline{RES}$ or upon writing a new data word into the Transmitter Data Register. When the End-of-Transmission bit is true the Transmitter Register Empty bit is disabled until a Transmitter Under-Run occurs.

SCSR 6: *Transmitter Data Register Empty*—Set to a logic 1 when the contents of the Transmitter Data Register are transferred to the Transmitter Shift Register. Cleared upon writing new data into the Transmit Data Register. This bit is initialized to a logic 1 by $\overline{RES}$.

SCSR 7: *Transmitter Under-Run*—Set to a logic 1 when the last data bit is transmitted if the transmitter is in a S/R Mode or when the last stop bit is transmitted if the XMTR is in the ASYN Mode while the Transmitter Data Register Empty Bit is set. Cleared by a transfer of new data into the Transmitter Shift Register or by $\overline{RES}$.

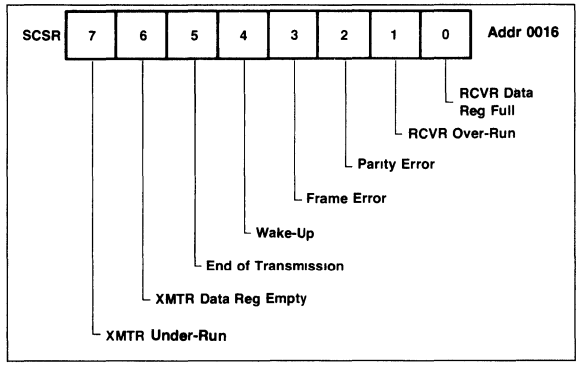


Figure 5-5. SCSR Bit Allocations

5.4 WAKE-UP FEATURE

In a multi-distributed microprocessor or microcomputer applications, a destination address is usually included at the beginning of the message. The Wake-Up Feature allows non-selected CPU's to ignore the remainder of the message until the beginning of the next message by setting the Wake-Up bit. As long as the Wake-Up flag is true, the Receiver Data Register Full Flag remains false. The Wake-Up bit is automatically cleared when the receiver detects a string of 11 consecutive 1's which indicates an idle transmit line. When the next byte is received, the Receiver Data Register Full Flag signals the CPU to wake-up and read the received data.

SECTION 6
COUNTER/TIMERS

The device contains two 16-bit counters (Counter A and Counter B) and three 16-bit latches associated with the counters. Counter A has one 16-bit latch and Counter B has two 16-bit latches. Each counter can be independently programmed to operate in one of four modes:

Counter A	Counter B
• Pulse width measurement	• Retriggerable Interval Counter
• Pulse Generation	• Asymmetrical Pulse Generation
• Interval Timer	• Interval Timer
• Event Counter	• Event Counter

Operating modes of Counter A and Counter B are controlled by the Mode Control Register. All counting begins at the initialization value and decrements. When modes are selected requiring a counter input/output line, PA4 is automatically selected for Counter A and PA5 is automatically selected for Counter B (see Table 4.2).

6.1 COUNTER A

Counter A consists of a 16-bit counter and a 16-bit latch organized as follows: Lower Counter A (LCA), Upper Counter A (UCA), Lower Latch A (LLA), and Upper Latch A (ULA). The counter contains the count of either Ø2 clock pulses or external events, depending on the counter mode selected. The contents of Counter A may be read any time by executing a read at location 0019 for the Upper Counter A and at location 001A or location 0018 for the Lower Counter A. A read at location 0018 also clears the Counter A Underflow Flag (IFR4).

The 16-bit latch contains the counter initialization value and can be loaded at any time by executing a write to the Upper Latch A at location 0019 and the Lower Latch A at location 0018. In either case, the contents of the accumulator are copied into the applicable latch register.

Counter A can be started at any time by writing to address: 001A. The contents of the accumulator will be copied into the Upper Latch A before the contents of the 16-bit latch are transferred to Counter A. Counter A is set to the latch value whenever Counter A underflows. When Counter A decrements from 0000 the next counter value will be the latch value—not FFFF—and the Counter A Underflow Flag (IFR 4) will be set to "1". This bit may be cleared by reading the Lower Counter A at location 0018, by writing to address location 001A, or by $\overline{RES}$.

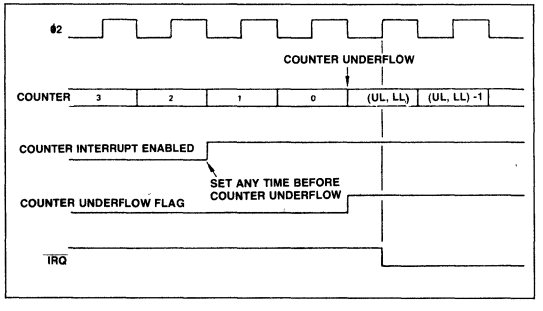


Figure 6-1. Interval Timer Timing Diagram

Counter A operates in any of four modes. These modes are selected by the Counter A Mode Control bits in the Control Register.

MCR1 (bit 1)	MCR0 (bit 0)	Mode
0	0	Interval Timer
0	1	Pulse Generation
1	0	Event Counter
1	1	Pulse Width Measurement

The Interval Timer, Pulse Generation, and Pulse Width Measurement Modes are Ø2 clock counter modes. The Event Counter Mode counts the occurrences of an external event on the CNTR line.

The Counter is set to the Interval Timer Mode (00) when a $\overline{RES}$ signal is generated.

6.1.1 Interval Timer

In the Interval Timer mode the Counter is initialized to the Latch value by either of two conditions:

1. When the Counter is decremented from 0000, the next Counter value is the Latch value (not FFFF).

2. When a write operation is performed to the Load Upper Latch and Transfer Latch to Counter address 001A, the Counter is loaded with the Latch value. Note that the contents of the Accumulator are loaded into the Upper Latch before the Latch value is transferred to the Counter.

The Counter value is decremented by one count at the 02 clock rate. The 16-bit Counter can hold from 1 to 65535 counts. The Counter Timer capacity is therefore 1μs to 65,535 ms at the 1 MHz Ø2 clock rate or 0.5 μs to 32.767 ms at the 2 MHz Ø2 clock rate. Time intervals greater than the maximum Counter value can be easily measured by counting $\overline{IRQ}$ interrupt requests in the counter $\overline{IRQ}$ interrupt routine.

When Counter A decrements from 0000, the Counter A Underflow (IFR4) is set to logic 1. If the Counter A Interrupt Enable Bit (IER4) is also set, an $\overline{IRQ}$ interrupt request will be generated. The Counter A Underflow bit in the Interrupt Flag Register can be examined in the $\overline{IRQ}$ interrupt routine to determine that the $\overline{IRQ}$ was generated by the Counter A Underflow.

While the timer is operating in the Interval Timer Mode, PA4 operates as a PA I/O bit.

A timing diagram of the Interval Timer Mode is shown in Figure 6-1.

6.1.2 Pulse Generation Mode

In the Pulse Generation mode, the CA line operates as a Counter Output. The line toggles from low to high or from high to low whenever a Counter A Underflow occurs or a write is performed to address 001A.

The normal output waveform is a symmetrical square-wave. The CA output is initialized high when entering the mode and transitions low when writing to 001A.

Asymmetric waveforms can be generated if the value of the latch is changed after each counter underflow.

A one-shot waveform can be generated by changing from Pulse Generation to Interval Timer mode after only one occurrence of the output toggle condition.

6.1.3 Event Counter Mode

In this mode the CA is used as an Event Input line, and the Counter will decrement with each rising edge detected on this line. The maximum rate at which this edge can be detected is one-half the $\phi 2$ clock rate.

The Counter can count up to 65,535 occurrences before underflowing. As in the other modes, the Counter A Underflow bit (IER4) is set to logic 1 if the underflow occurs.

Figure 6.2 is a timing diagram of the Event Counter Mode.

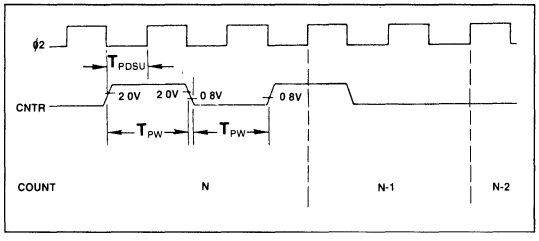


Figure 6-2. Event Counter Mode

6.1.4 Pulse Width Measurement Mode

This mode allows the accurate measurement of a low pulse duration on the CA line. The Counter decrements by one count at the $\phi 2$ clock rate as long as the CA line is held in the low state. The Counter is stopped when CA is in the high state.

The Counter A underflow flag will be set only when the count in the timer reaches zero. Upon reaching zero the timer will be loaded with the latch value and continue counting down as long as the CA pin is held low. After the counter is stopped by a high level on CA, the count will hold as long as CA remains high. Any further low levels on CA will again cause the counter to count down from its present value. The state of the CA line can be determined by testing the state of PA4.

A timing diagram for the Pulse Width Measurement Mode is shown in Figure 6.3.

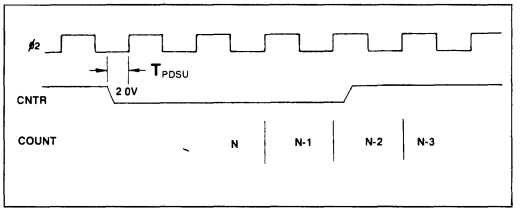


Figure 6-3. Pulse Width Measurement

6.1.5 Serial I/O Data Rate Generation

Counter A also provides clock timing for the Serial I/O which establishes the data rate for the Serial I/O port. When the Serial I/O is enabled, Counter A is forced to operate at the internal clock rate. Counter A is not required for the RCVR S/R mode. The Counter I/O (PA4) may also be required to support the Serial I/O (see Table 4-2).

Table 6-1 identifies the values to be loaded in Counter A for selecting standard data rates with a $\phi 2$ clock rate of 1 MHz and 2 MHz. Although Table 6-1 identifies only the more common data rates, any data rate from 1 to 62.5K bps can be selected by using the formula:

$$N = \frac{\phi 2}{16 \times bps} - 1$$

where

- N = decimal value to be loaded into Counter A using its hexadecimal equivalent.
- $\phi 2$ = the clock frequency (1 MHz or 2 MHz)
- bps = the desired data rate.

NOTE

In Table 6-1 you will notice that the standard data rate and the actual data rate may be slightly different. Transmitter and receiver errors of 1.5% or less are acceptable. A revised clock rate is included in Table 6-1 for those baud rates which fall outside this limit.

Table 6-1. Counter A Values for Baud Rate Selection

Standard Baud Rate	Hexadecimal Value		Actual Baud Rate At		Clock Rate Needed To Get Standard Baud Rate	
	1 MHz	2 MHz	1 MHz	2 MHz	1 MHz	2 MHz
50	04E1	09C3	50.00	50.00	1.0000	2.0000
75	0340	0682	75.03	74.99	1.0000	2.0000
110	0237	046F	110.04	110.04	1.0000	2.0000
150	01A0	0340	149.88	150.06	1.0000	2.0000
300	00CF	01A0	300.48	299.76	1.0000	2.0000
600	0067	00CF	600.96	600 96	1.0000	2.0000
1200	0033	0067	1201.92	1201 92	1.0000	2 0000
2400	0019	0033	2403.85	2403.85	1 0000	2.0000
3600	0010	0021	3676.47	3676.47	0.9792	1.9584
4800	000C	0019	4807.69	4807.69	1.0000	2.0000
7200	0008	0010	6944 44	7352.94	1.0368	1.9584
9600	0006	000C	8928 57	9615.38	1.0752	2.0000

6.2 COUNTER B

Counter B consists of a 16-bit counter and two 16-bit latches organized as follows: Lower Counter B (LCB), Upper Counter B (UCB), Lower Latch B (LLB), Upper Latch B (ULB), Lower Latch C (LLC), and Upper Latch C (ULC). Latch C is used only in the asymmetrical pulse generation mode. The counter contains the count of either Ø2 clock pulses or external events depending on the counter mode selected. The contents of Counter B may be read any time by executing a Read at location 001D for the Upper Counter B and at location 001E or 001C for the Lower Counter B. A Read at location 001C also clears the Counter B Underflow Flag.

Latch B contains the counter initialization value and can be loaded at any time by executing a Write to the Upper Latch B at location 001D and the Lower Latch B at location 001C. In each case, the contents of the accumulator are copied into the applicable latch register.

Counter B can be initialized at any time by writing to address: 001E. The contents of the accumulator is copied into the Upper Latch B before the value in the 16-bit Latch B is transferred to Counter B. Counter B will also be set to the latch value and the Counter B Underflow Flag bit (IFR5) will be set to a "1" whenever Counter B underflows by decrementing from 0000.

IFR 5 may be cleared by reading the Lower Counter B at location 001C, by writing to address location 001E, or by $\overline{RES}$.

Counter B operates in the same manner as Counter A in the Interval Timer and Event Counter modes. The Pulse Width Measurement Mode is replaced by the Retriggerable Interval Timer mode and the Pulse Generation mode is replaced by the Asymmetrical Pulse Generation Mode. Mode Control Register bits MCR2 and MCR3 select the four Counter B modes in a similar manner and coding as MCR0 and MCR1 select the modes of Counter A.

6.2.1 Retriggerable Interval Timer Mode

When operating in the Retriggerable Interval Timer mode, Counter B is initialized to the latch value by writing to address 001E, by a Counter B underflow, or whenever a positive edge occurs on the CB pin (PA5). The Counter B interrupt flag will be set if the counter underflows before a positive edge occurs on the CB line. Figure 6-4 illustrates the operation.

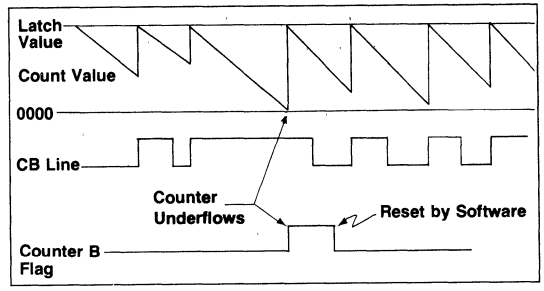


Figure 6-4. Counter B. Retriggerable Interval Timer Mode

6.2.2 Asymmetrical Pulse Generation Mode

Counter B has a special Asymmetrical Pulse Generation Mode whereby a pulse train with programmable pulse width and period can be generated without the processor intervention once the latch values are initialized.

In this mode, the 16-bit Latch B is initialized with a value which corresponds to the duration between pulses (referred to as D in the following descriptions). The 16-bit Latch C is initialized with a value corresponding to the desired pulse width (referred to as P in the following descriptions). The initialization sequence for Latch B and C and the starting of a counting sequence are as follows:

1. The lower 8 bits of P are loaded into LLB by writing to address 001C; the upper 8 bits of P are loaded into ULB and the full 16 bits are transferred to Latch C by writing to address location 001D. At this point both Latch B and Latch C contain the value of P.

2. The lower 8 bits of D are loaded into LLB by writing to address 001C; the upper 8 bits of D are loaded into ULB by writing to address location 001E. Writing to address location 001E also causes the contents of the 16-bit Latch B to be downloaded into the Counter B and the CB output to go low as shown in Figure 6-5.

3. When Counter B underflow occurs the contents of the Latch C are loaded into the Counter B and the CB output toggles to a high level, staying high until another underflow occurs. Latch B is then down-loaded and the CB output toggles to a low level repeating the whole process.

SECTION 7
POWER ON/INITIALIZATION CONSIDERATIONS

7.1 POWER ON TIMING

After application of V_{CC} and V_{RR} power to the device, $\overline{RES}$ must be held low for at least eight $\phi 2$ clock cycles after V_{CC} reaches operating range and the internal oscillator has stabilized. This stabilization time is dependent upon the input V_{CC} voltage and performance of the internal oscillator. The clock can be monitored at $\phi 2$ (pin 3). Figure 7-1 illustrates the power turn-on waveforms. Clock stabilization time is typically 20 ms.

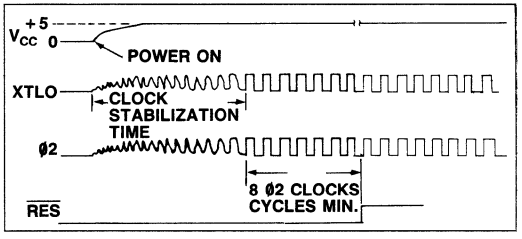


Figure 7-1. Power Turn-On Timing Detail

7.2 POWER-ON RESET

When $\overline{RES}$ goes from low to high, the device sets the Interrupt Mask Bit—bit 2 of the Processor Status Register—and initiates a reset vector fetch at address FFFC and FFFD (or optionally 7FFE and 7FFF) to begin user program execution. All of the I/O ports (PA, PB, PC, PD) will be forced to the high (logic 1) state. All bits of the Control Register will be cleared to logic 0 causing the Interval Timers counter mode (mode 00) to be selected and all interrupt enabled bits to be reset.

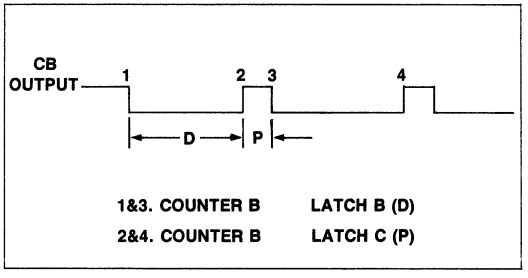


Figure 6-5. Counter B Pulse Generation

7.3 RESET ($\overline{RES}$) CONDITIONING

When $\overline{RES}$ is driven from low to high the device is put in a reset state causing the registers and I/O ports to be configured as shown in Table 7-1.

Table 7-1. $\overline{RES}$ Initialization of I/O Ports and Registers

Bit No.	7	6	5	4	3	2	1	0
REGISTERS								
Processor Status	—	—	—	—	—	1	—	—
Mode Control (MCR)	0	0	0	0	0	0	0	0
Int. Enable (IER)	0	0	0	0	0	0	0	0
Int Flag (IFR)	0	0	0	0	0	0	0	0
Ser. Com Control (SCCR)	0	0	0	0	0	0	0	0
Ser. Com. Status (SCSR)	0	1	0	0	0	0	0	0
PORTS								
PA Latch	1	1	1	1	1	1	1	1
PB Latch	1	1	1	1	1	1	1	1
PC Latch	1	1	1	1	1	1	1	1
PD Latch	1	1	1	1	1	1	1	1

All RAM and other CPU registers will initialize in a random, non-repeatable data pattern.

7.4 INITIALIZATION

Any initialization process for the device should include a $\overline{RES}$, as indicated in the preceeding paragraphs. After stabilization of the internal clock (if a power on situation) an initialization subroutine should be executed to perform (as a minimum) the following functions:

1. The Stack Pointer should be set
2. Clear or Set Decimal Mode
3. Set or Clear Carry Flag
4. Set up Mode Controls as required
5. Clear Interrupts

A typical initialization subroutine could be as follows:

LDX	Load stack pointer starting address into X Register
TXS	Transfer X Register value to Stack Pointer
CLD	Clear Decimal Mode
SEC	Set Carry Flag
. . . .	Set-up Mode Control and
. . . .	special function registers
. . . .	and clear RAM as required
CLI	Clear Interrupts

APPENDIX A
ENHANCED R6502 INSTRUCTION SET

This appendix contains a summary of the Enhanced R6502 instruction set. For detailed information, consult the R6502 Microcomputer System Programming Manual, Document 29650 N30. The four instructions notated with a * are added instructions to enhance the standard 6502 instruction set.

A.1 INSTRUCTION SET IN ALPHABETIC SEQUENCE

MNEMONIC	INSTRUCTION	MNEMONIC	INSTRUCTION
ADC	Add Memory to Accumulator with Carry	LDA	Load Accumulator with Memory
AND	"AND" Memory with Accumulator	LDX	Load Index X with Memory
ASL	Shift Left One Bit (Memory or Accumulator)	LDY	Load Index Y with Memory
		LSR	Shift One Bit Right (Memory or Accumulator)
*BBR	Branch on Bit Reset Relative		
*BBS	Branch on Bit Set Relative		
BCC	Branch on Carry Clear	NOP	No Operation
BCS	Branch on Carry Set		
BEQ	Branch on Result Zero	ORA	"OR" Memory with Accumulator
BIT	Test Bits in Memory with Accumulator		
BMI	Branch on Result Minus	PHA	Push Accumulator on Stack
BNE	Branch on Result not Zero	PHP	Push Processor Status on Stack
BPL	Branch on Result Plus	PLA	Pull Accumulator from Stack
BRK	Force Break	PLP	Pull Processor Status from Stack
BVC	Branch on Overflow Clear		
BVS	Branch on Overflow Set	*RMB	Reset Memory Bit
		ROL	Rotate One Bit Left (Memory or Accumulator)
CLC	Clear Carry Flag		
CLD	Clear Decimal Mode	ROR	Rotate One Bit Right (Memory or Accumulator)
CLI	Clear Interrupt Disable Bit		
CLV	Clear Overflow Flag	RTI	Return from Interrupt
CMP	Compare Memory and Accumulator	RTS	Return from Subroutine
CPX	Compare Memory and Index X		
CPY	Compare Memory and Index Y	SBC	Subtract Memory from Accumulator with Borrow
DEC	Decrement Memory by One	SEC	Set Carry Flag
DEX	Decrement Index X by One	SED	Set Decimal Mode
DEY	Decrement Index Y by One	SEI	Set Interrupt Disable Status
		*SMB	Set Memory Bit
EOR	"Exclusive-Or" Memory with Accumulator	STA	Store Accumulator in Memory
		STX	Store Index X in Memory
		STY	Store Index Y in Memory
INC	Increment Memory by One		
INX	Increment Index X by One	TAX	Transfer Accumulator to Index X
INY	Increment Index Y by One	TAY	Transfer Accumulator to Index Y
		TSX	Transfer Stack Pointer to Index X
JMP	Jump to New Location	TXA	Transfer Index X to Accumulator
JSR	Jump to New Location Saving Return Address	TXS	Transfer Index X to Stack Register
		TYA	Transfer Index Y to Accumulator

A.2 R6511Q AND R6500/13 INSTRUCTION SET SUMMARY TABLE

ADDRESSING MODES

MNEMONIC	OPERATION	IMMEDIATE			ABSOLUTE			ZERO PAGE			ACCUM			IMPLIED			(IND, X)			(IND), Y		
		OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#
ADC	A • M • C→A (4)(1)	69	2	2	6D	4	3	65	3	2							61	6	2	71	5	2
AND	A M→A (1)	29	2	2	2D	4	3	25	3	2							21	6	2	31	5	2
ASL	C← [7 0] ←0				0E	6	3	06	5	2	0A	2	1									
BBR[#(0-7)]	Branch on M_6 = 0 (5)(2)																					
BBS[#(0-7)]	Branch on M_6 = 1 (5)(2)																					
BCC	Branch on C = 0 (2)																					
BCS	Branch on C = 1 (2)																					
BEQ	Branch on Z = 1 (2)																					
BIT	A ∧ M				2C	4	3	24	3	2												
BMI	Branch on N = 1 (2)																					
BNE	Branch on Z = 0 (2)																					
BPL	Branch on N = 0 (2)																					
BRK	Break (See Fig 1)													00	7	1						
BVC	Branch on V = 0 (2)																					
BVS	Branch on V = 1 (2)																					
CLC	0→C													18	2	1						
CLD	0→D													D8	2	1						
CLI	0→I													58	2	1						
CLV	0→V													B8	2	1						
CMP	A M (1)	C9	2	2	CD	4	3	C5	3	2							C1	6	2	D1	5	2
CPX	X M	E0	2	2	EC	4	3	E4	3	2												
CPY	Y M	C0	2	2	CC	4	3	C4	3	2												
DEC	M 1→M				CE	6	3	C6	5	2												
DEX	X 1→X													CA	2	1						
DEY	Y 1→Y													88	2	1						
EOR	A∀M→A (1)	49	2	2	4D	4	3	45	3	2							41	6	2	51	5	2
INC	M • 1→M				EE	6	3	E6														
INX	X • 1→X													EB	2	1						
INY	Y 1→Y													C8	2	1						
JMP	Jump to New Loc				4C	3	3															
JSR	Jump Sub (See Fig 2)				20	6	3															
LDA	M→A (1)	A9	2	2	AD	4	3	A5	3	2							A1	6	2	B1	5	2
LDX	M→X (1)	A2	2	2	AE	4	3	A6	3	2												
LDY	M→Y (1)	A0	2	2	AC	4	3	A4	3	2												
LSR	0→ [7 0] → C				4E	6	3	46	5	2	4A	2	1									
NOP	No Operation													EA	2	1						
ORA	AVM→A (1)	09	2	2	0D	4	3	05	3	2							01	6	2	11	5	2
PHA	A→Ms S - 1→S													48	3	1						
PHP	P→Ms S 1→S													08	3	1						
PLA	S • 1→S Ms→A													68	4	1						
PLP	S 1→S Ms→P													28	4	1						
RMB[#(0-7)]	0→M_b (5)																					
RØL	←[7 0]←[C]←				2E	6	3	26	5	2	2A	2	1									
RØR	→[C]→[7 0]→				6E	6	3	66	5	2	6A	2	1									
RTI	Rtrn Int (See Fig 1)													40	6	1						
RTS	Rtrn Sub (See Fig 2)													60	6	1						
SBC	A - M - C→A (1)	E9	2	2	ED	4	3	E5	3	2							E1	6	2	F1	5	2
SEC	1→C													38	2	1						
SED	1→D													F8	2	1						
SEI	1→T													78	2	1						
SMB[#(0-7)]	1→M_b (5)																					
STA	A→M				8D	4	3	85	3	2							81	6	2	91	6	2
STX	X→M				8E	4	3	86	3	2												
STY	Y→M				8C	4	3	84	3	2												
TAX	A→X													AA	2	1						
TAY	A→Y													A8	2	1						
TSX	S→X													BA	2	1						
TXA	X→A													8A	2	1						
TXS	X→S													9A	2	1						
TYA	Y→A													98	2	1						

MNEMONIC	Z PAGE, X			ABS, X			ABS, Y			RELATIVE			INDIRECT			Z PAGE, Y		
	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#
ADC	75	4	2	7D	4	3	79	4	3									
AND	35	4	2	3D	4	3	39	4	3									
ASL	16	6	2	1E	7	3												
BBR[#(0-7)]																		
BBS[#(0-7)]																		
BCC										90	2	2						
BCS										B0	2	2						
BEQ										F0	2	2						
BIT																		
BMI										30	2	2						
BNE										D0	2	2						
BPL										10	2	2						
BRK																		
BVC										50	2	2						
BVS										70	2	2						
CLC																		
CLD																		
CLI																		
CLV																		
CMP	D5	4	2	DD	4	3	D9	4	3									
CPX																		
CPY																		
DEC	D6	6	2	DE	7	3												
DEX																		
DEY																		
EOR	55	4	2	5D	4	3	59	4	3									
INC	F6	6	2	FE	7	3												
INX																		
INY																		
JMP													6C	5	3			
JSR																		
LDA	B5	4	2	BD	4	3	B9	4	3									
LDX							BE	4	3							B6	4	2
LDY	B4	4	2	BC	4	3												
LSR	56	6	2	5E	7	3												
NOP																		
ORA	15	4	2	1D	4	3	19	4	3									
PHA																		
PHP																		
PLA																		
PLP																		
RMB[#(0-7)]																		
RØL	36	6	2	3E	7	3												
RØR	76	6	2	7E	7	3												
RTI																		
RTS																		
SBC	F5	4	2	FD	4	3	F9	4	3									
SEC																		
SED																		
SEI																		
SMB[#(0-7)]																		
STA	95	4	2	9D	5	3	[illegible]	5	3									
STX																96	4	2
STY	94	4	2															
TAX																		
TAY																		
TSX																		
TXA																		
TXS																		
TYA																		

MNEMONIC	BIT ADDRESSING (OP BY BIT #) 0	1	2	3	4	5	6	7	PROCESSOR STATUS CODES 7 6 5 4 3 2 1 0 / N V · B D I Z C
ADC									N V · · · · Z C
AND									N · · · · · Z ·
ASL									N · · · · · Z C
BBR[#(0-7)]	0F	1F	2F	3F	4F	5F	6F	7F	· · · · · · · ·
BBS[#(0-7)]	8F	9F	AF	BF	CF	DF	EF	FF	· · · · · · · ·
BCC									· · · · · · · ·
BCS									· · · · · · · ·
BEQ									· · · · · · · ·
BIT									M_7 M_6 · · · · Z ·
BMI									· · · · · · · ·
BNE									· · · · · · · ·
BPL									· · · · · · · ·
BRK									· · · 1 · 1 · ·
BVC									· · · · · · · ·
BVS									· · · · · · · ·
CLC									· · · · · · · 0
CLD									· · · · 0 · · ·
CLI									· · · · · 0 · ·
CLV									· 0 · · · · · ·
CMP									N · · · · · Z C
CPX									N · · · · · Z C
CPY									N · · · · · Z C
DEC									N · · · · · Z ·
DEX									N · · · · · Z ·
DEY									N · · · · · Z ·
EOR									N · · · · · Z ·
INC									N · · · · · Z ·
INX									N · · · · · Z ·
INY									N · · · · · Z ·
JMP									· · · · · · · ·
JSR									· · · · · · · ·
LDA									N · · · · · Z ·
LDX									N · · · · · Z ·
LDY									N · · · · · Z ·
LSR									0 · · · · · Z C
NOP									· · · · · · · ·
ORA									N · · · · · Z ·
PHA									· · · · · · · ·
PHP									· · · · · · · ·
PLA									N · · · · · Z ·
PLP									(Restored)
RMB[#(0-7)]	07	17	27	37	47	57	67	77	· · · · · · · ·
RØL									N · · · · · Z C
RØR									N · · · · · Z C
RTI									(Restored)
RTS									· · · · · · · ·
SBC									N V · · · · Z (3)
SEC									· · · · · · · 1
SED									· · · · 1 · · ·
SEI									· · · · · 1 · ·
SMB[#(0-7)]	87	97	A7	B7	C7	D7	E7	F7	· · · · · · · ·
STA									· · · · · · · ·
STX									· · · · · · · ·
STY									· · · · · · · ·
TAX									N · · · · · Z ·
TAY									N · · · · · Z ·
TSX									N · · · · · Z ·
TXA									N · · · · · Z ·
TXS									· · · · · · · ·
TYA									N · · · · · Z ·

NOTES

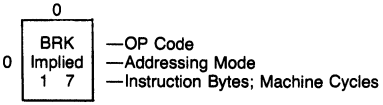
1 Add 1 to N if page boundary is crossed
2 Add 1 to N if branch occurs to same page
Add 2 to N if branch occurs to different page
3 Carry not = Borrow
4 If in decimal mode Z flag is invalid
accumulator must be checked on zero result
5 Effects 8-bit data field of the specified zero page address

LEGEND

X = Index X
Y = Index Y
A = Accumulator
M = Memory per effective address
M_s = Memory per stack pointer
M_b = Selecter zero page memory bit
M_7 = Memory Bit 7
M_6 = Memory Bit 6
• = Add
− = Subtract
∧ = And
V = Or
∀ = Exclusive Or
n = Number of cycles
# = Number of Bytes

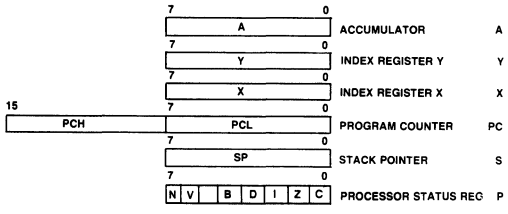
A.3 INSTRUCTION CODE MATRIX

MSD \ LSD	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	MSD
0	BRK Implied 1 7	ORA (IND, X) 2 6				ORA ZP 2 3	ASL ZP 2 5	RMB0 ZP 2 5	PHP Implied 1 3	ORA IMM 2 2	ASL Accum 1 2			ORA ABS 3 4	ASL ABS 3 6	BBR0 ZP 3 5**	0
1	BPL Relative 2 2**	ORA (IND), Y 2 5*				ORA ZP, X 2 4	ASL ZP, X 2 6	RMB1 ZP 2 5	CLC Implied 1 2	ORA ABS, Y 3 4*				ORA ABS, X 3 4*	ASL ABS, X 3 7	BBR1 ZP 3 5**	1
2	JSR Absolute 3 6	AND (IND, X) 2 6			BIT ZP 2 3	AND ZP 2 3	ROL ZP 2 5	RMB2 ZP 2 5	PLP Implied 1 4	AND IMM 2 2	ROL Accum 1 2		BIT ABS 3 4	AND ABS 3 4	ROL ABS 3 6	BBR2 ZP 3 5**	2
3	BMI Relative 2 2**	AND (IND, Y) 2 5*				AND ZP, X 2 4	ROL ZP, X 2 6	RMB3 ZP 2 5	SEC Implied 1 2	AND ABS, Y 3 4*				AND ABS, X 3 4*	ROL ABS, X 3 7	BBR3 ZP 3 5**	3
4	RTI Implied 1 6	EOR (IND, X) 2 6				EOR ZP 2 3	LSR ZP 2 5	RMB4 ZP 2 5	PHA Implied 1 3	EOR IMM 2 2	LSR Accum 1 2		JMP ABS 3 3	EOR ABS 3 4	LSR ABS 3 6	BBR4 ZP 3 5**	4
5	BVC Relative 2 2**	EOR (IND), Y 2 5*				EOR ZP, X 2 4	LSR ZP, X 2 6	RMB5 ZP 2 5	CLI Implied 1 2	EOR ABS, Y 3 4*				EOR ABS, X 3 4*	LSR ABS, X 3 7	BBR5 ZP 3 5**	5
6	RTS Implied 1 6	ADC (IND, X) 2 6				ADC ZP 2 3	ROR ZP 2 5	RMB6 ZP 2 5	PLA Implied 1 4	ADC IMM 2 2	ROR Accum 1 2		JMP Indirect 3 5	ADC ABS 3 4	ROR ABS 3 6	BBR6 ZP 3 5**	6
7	BVS Relative 2 2**	ADC (IND, Y) 2 5*				ADC ZP, X 2 4	ROR ZP, X 2 6	RMB7 ZP 2 5	SEI Implied 1 2	ADC ABS, Y 3 4*				ADC ABS, X 3 4*	ROR ABS, X 3 7	BBR7 ZP 3 5**	7
8		STA (IND, X) 2 6			STY ZP 2 3	STA ZP 2 3	STX ZP 2 3	SMB0 ZP 2 5	DEY Implied 1 2		TXA Implied 1 2		STY ABS 3 4	STA ABS 3 4	STX ABS 3 4	BBS0 ZP 3 5**	8
9	BCC Relative 2 2**	STA (IND, Y) 2 6			STY ZP, X 2 4	STA ZP, X 2 4	STX ZP, Y 2 4	SMB1 ZP 2 5	TYA Implied 1 2	STA ABS, Y 3 5	TXS Implied 1 2			STA ABS, X 3 5		BBS1 ZP 3 5**	9
A	LDY IMM 2 2	LDA (IND, X) 2 6	LDX IMM 2 2		LDY ZP 2 3	LDA ZP 2 3	LDX ZP 2 3	SMB2 ZP 2 5	TAY Implied 1 2	LDA IMM 2 2	TAX Implied 1 2		LDY ABS 3 4	LDA ABS 3 4	LDX ABS 3 4	BBS2 ZP 3 5**	A
B	BCS Relative 2 2**	LDA (IND), Y 2 5*			LDY ZP, X 2 4	LDA ZP, X 2 4	LDX ZP, Y 2 4	SMB3 ZP 2 5	CLV Implied 1 2	LDA ABS, Y 3 4*	TSX Implied 1 2		LDY ABS, X 3 4*	LDA ABS, X 3 4*	LDX ABS, Y 3 4*	BBS3 ZP 3 5**	B
C	CPY IMM 2 2	CMP (IND, X) 2 6			CPY ZP 2 3	CMP ZP 2 3	DEC ZP 2 5	SMB4 ZP 2 5	INY Implied 1 2	CMP IMM 2 2	DEX Implied 1 2		CPY ABS 3 4	CMP ABS 3 4	DEC ABS 3 6	BBS4 ZP 3 5**	C
D	BNE Relative 2 2**	CMP (IND), Y 2 5*				CMP ZP, X 2 4	DEC ZP, X 2 6	SMB5 ZP 2 5	CLD Implied 1 2	CMP ABS, Y 3 4*				CMP ABS, X 3 4*	DEC ABS, X 3 7	BBS5 ZP 3 5**	D
E	CPX IMM 2 2	SBC (IND, X) 2 6			CPX ZP 2 3	SBC ZP 2 3	INC ZP 2 5	SMB6 ZP 2 5	INX Implied 1 2	SBC IMM 2 2	NOP Implied 1 2		CPX ABS 3 4	SBC ABS 3 4	INC ABS 3 6	BBS6 ZP 3 5**	E
F	BEQ Relative 2 2**	SBC (IND), Y 2 5*				SBC ZP, X 2 4	INC ZP, X 2 6	SMB7 ZP 2 5	SED Implied 1 2	SBC ABS, Y 3 4*				SBC ABS, X 3 4*	INC ABS, X 3 7	BBS7 ZP 3 5**	F
	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	

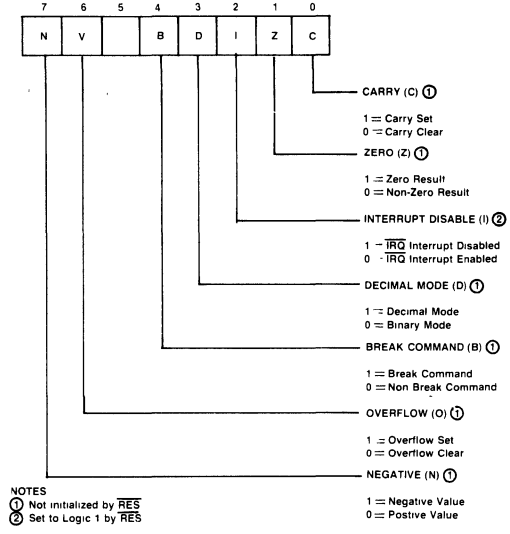


*Add 1 to N if page boundary is crossed.
**Add 1 to N if branch occurs to same page;
add 2 to N if branch occurs to different page.

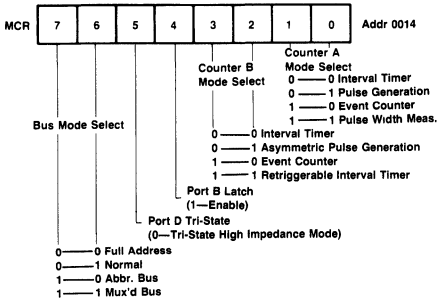
APPENDIX B
KEY REGISTER SUMMARY



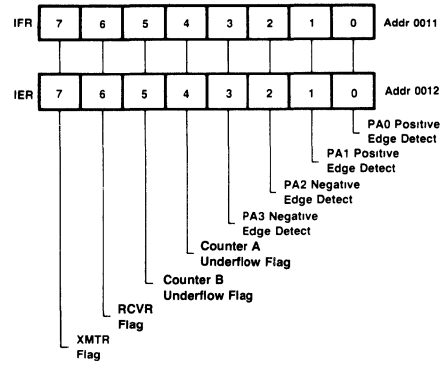
CPU Registers



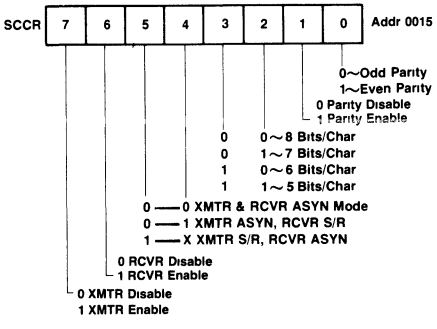
Processor Status Register



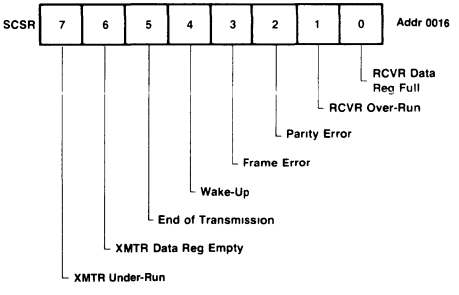
Mode Control Register



Interrupt Enable and Flag Registers



Serial Communications Control Register



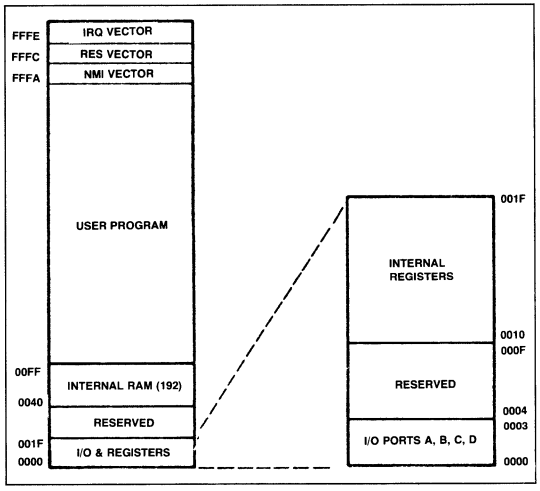
Serial Communications Status Register

APPENDIX C
ADDRESS ASSIGNMENTS/MEMORY MAPS/PIN FUNCTIONS

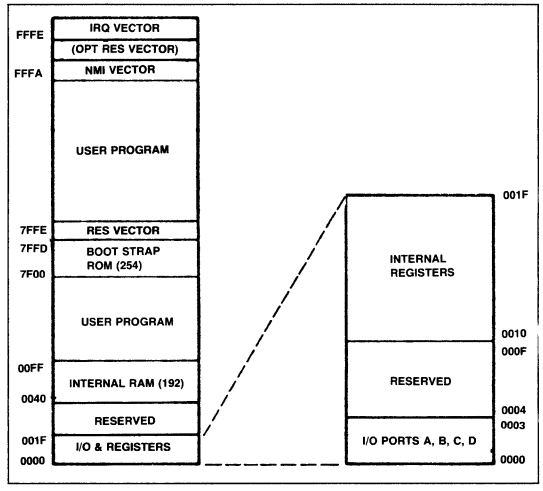
C.1 I/O AND INTERNAL REGISTER ADDRESSES

ADDRESS (HEX)	READ	WRITE
001F	— —	— —
1E	Lower Counter B	Upper Latch B, Cntr B←Latch B, CLR Flag
1D	Upper Counter B	Upper Latch B, Latch C←Latch B
1C	Lower Counter B, CLR Flag	Lower Latch B.
1B	— —	— —
1A	Lower Counter A	Upper Latch A, Cntr A←Latch A, CLR Flag
19	Upper Counter A	Upper Latch A
18	Lower Counter A, CLR Flag	Lower Latch A
17	Serial Receiver Data Register	Serial Transmitter Data Register
16	Serial Comm. Status Register	Serial Comm. Status Reg. Bits 4 & 5 only
15	Serial Comm. Control Register	Serial Comm Control Register
14	Mode Control Register	Mode Control Register
13	— —	— —
12	Interrupt Enable Register	Interrupt Enable Register
11	Interrupt Flag Register	— —
0010	Read FF	Clear Int Flag (Bits 0-3 only, Write 0's only)
0F	**RESERVED**	
0E		
0D	These addresses are reserved and are used by the CPU during Read and Write	
0C	operation over the external Data Bus (D0-D7).	
0B		
0A		
09		
08		
07		
06		
05		
04		
03	Port D	Port D
02	Port C	Port C
01	Port B	Port B
0000	Port A	Port A

C.2 FULL ADDRESS MODE MEMORY MAP R6511Q OR R6500/13



C.3 FULL ADDRESS MODE MEMORY MAP R6500/13 ONLY



C.4 MULTIPLE FUNCTION PIN ASSIGNMENTS—PORT C AND PORT D

PIN NUMBER	FULL ADDRESS MODE	I/O PORT FUNCTION	ABBREVIATED PORT FUNCTION	MULTIPLEXED PORT FUNCTION
54	PC0	PC0	A0	A0
55	PC1	PC1	A1	A1
56	PC2	PC2	A2	A2
57	PC3	PC3	A3	A3
58	PC4	PC4	A12	A12
59	PC5	PC5	R/W	R/W
60	A13	PC6	A13	A13
61	A14	PC7	EMS	EMS
62	PD0	PD0	D0	A4/D0
63	PD1	PD1	D1	A5/D1
64	PD2	PD2	D2	A6/D2
1	PD3	PD3	D3	A7/D3
2	PD4	PD4	D4	A8/D4
3	PD5	PD5	D5	A9/D5
4	PD6	PD6	D6	A10/D6
5	PD7	PD7	D7	A11/D7

APPENDIX D
ELECTRICAL SPECIFICATIONS

MAXIMUM RATINGS*

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC} & V_{RR}	−0.3 to +7.0	Vdc
Input Voltage	V_{IN}	−0.3 to +7.0	Vdc
Operating Temperature Commercial Industrial	T_A	T_L to T_H 0 to +70 −40 to +85	°C
Storage Temperature	T_{STG}	−55 to +150	°C

***NOTE:** Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the other sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

(V_{CC} = 5.0V ±5%, V_{RR} = V_{CC}; V_{SS} = 0V; T_A = 0° to 70°, unless otherwise specified)

Parameter	Symbol	Min	Typ[1]	Max	Unit	Test Conditions
RAM Standby Voltage (Retention Mode)	V_{RR}	3.0		V_{CC}	V	
RAM Standby Current (Retention Mode) Commercial Industrial	I_{RR}	 — —	 4 5.2	 — —	mA	T_A = 25°C
Input High Voltage All Except XTLI and Ø2 in Slave Option XTLI and Ø2 in Slave Option	V_{IH}	 +2.0 +4.0	 — —	 V_{CC} V_{CC}	V	
Input Low Voltage	V_{IL}	−0.3	—	+0.8	V	
Input Leakage Current $\overline{RES}$, $\overline{NMI}$	I_{IN}	—	—	±10.0	µA	V_{IN} = 0 to 5.0V
Input Low Current PA, PB, PC, PD	I_{IL}	—	−1.0	−1.6	mA	V_{IL} = 0.4V
Output High Voltage (Except XTLO)	V_{OH}	+2.4	—	V_{CC}	V	I_{LOAD} = −100 µA
Output Low Voltage	V_{OL}	—	—	+0.4	V	I_{LOAD} = 1.6 mA
I/O Port Pull-Up Resistance PA0–PA7, PB0–PB7, PC0–PC7	R_L	3.0	6.0	11.5	Kohm	
Output Leakage Current (Three-State Off)	I_{OUT}	—	—	±10	µA	
Input Capacitance XTLI, XTLO All Others	C_{IN}	 — —	 — —	 50 10	pF	T_A = 25°C V_{IN} = 0V f = 1.0 MHz
Output Capacitance (Three-State Off)	C_{OUT}	—	—	10	pF	T_A = 25°C V_{IN} = 0V f = 1.0 MHz
Power Dissipation (Outputs High) Commercial Industrial	P_D	 — —	 750 —	 1100 1200	mW	T_A = 0°C

Notes:
1. Typical values measured at T_A = 25°C and V_{CC} = 5.0V.
2. Negative sign indicates outward current flow, positive indicates inward flow.

APPENDIX E
TIMING REQUIREMENTS AND CHARACTERISTICS

E.1 GENERAL NOTES

1. V_{CC} = 5V ±5%, 0°C ≤ TA ≤ 70°C

2. A valid V_{CC} – $\overline{RES}$ sequence is required before proper operation is achieved.

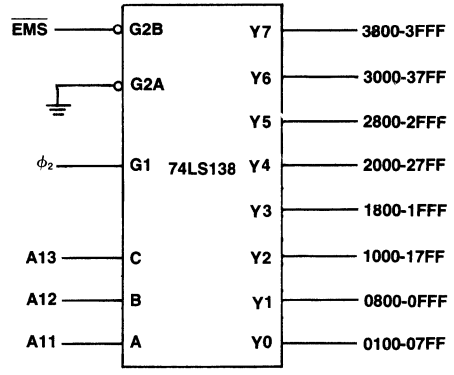
3. All timing reference levels are 0.8V and 2.0V, unless otherwise specified.

4. All time units are nanoseconds, unless otherwise specified.

5. All capacitive loading is 130pf maximum, except as noted below:

PA, PB	—	50pf maximum
PC (I/O Modes Only)	—	50pf maximum
PC (ABB and Mux Mode)	—	130pf maximum
PC6, PC7 (Full Address Mode)	—	130pf maximum

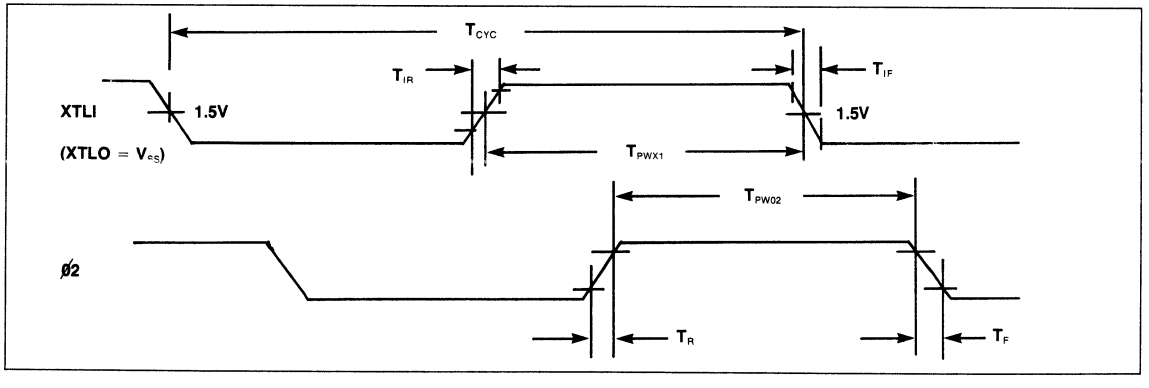
6. Example of External Chip Select (Multiplexed Bus)



Note that *both* $\overline{EMS}$ and Phase 2 (ϕ_2) must be used to correctly enable the chip selects in the multiplexed or abbreviated bus modes.

E.2 CLOCK TIMING

SYMBOL	PARAMETER	1 MHz		2 MHz	
		MIN	MAX	MIN	MAX
T_{CYC}	Cycle Time	1000	10 μs	500	10 μs
T_{PWX1}	XTLI Input Clock Pulse Width XTLO = VSS	500 ± 25	—	250 ± 10	—
T_{PW02}	Output Clock Pulse Width at Minimum T_{CYC}	T_{PWX1}	T_{PWX1} ± 25	T_{PWX1}	T_{PWX1} ± 20
T_R, T_F	Output Clock Rise, Fall Time	—	25	—	15
T_{IR}, T_{IF}	Input Clock Rise, Fall Time	—	10	—	10

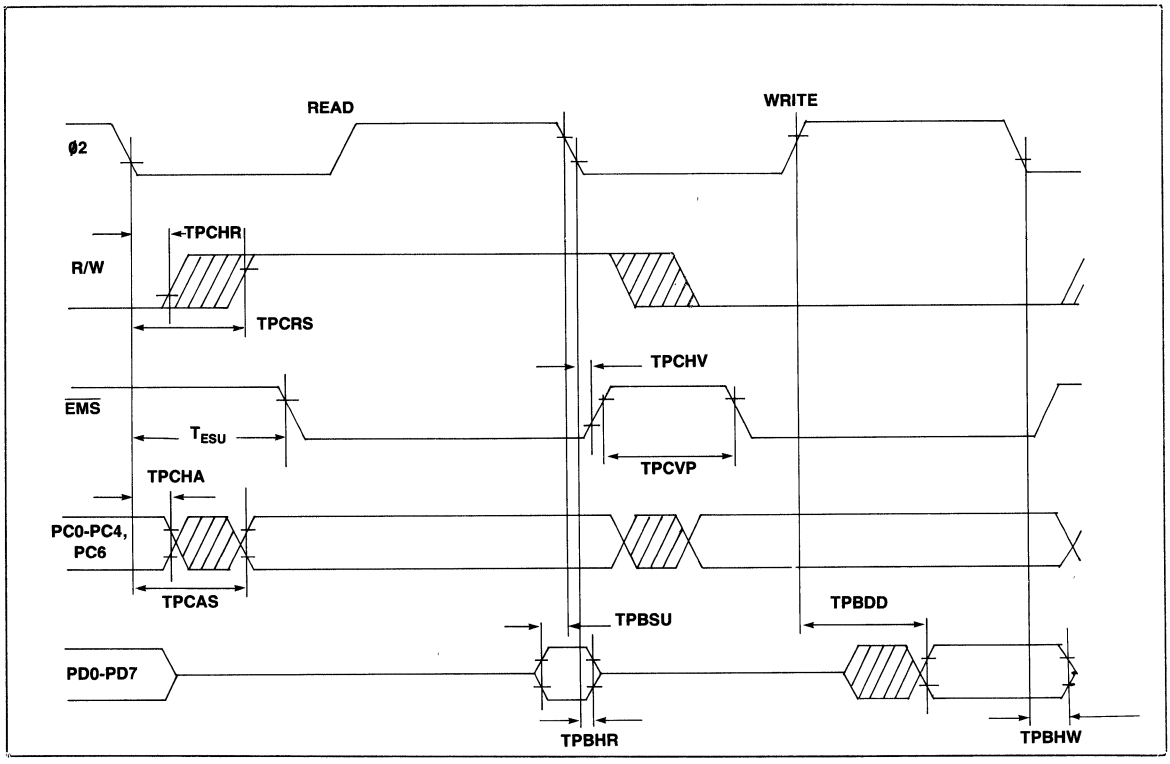


E.3 ABBREVIATED MODE TIMING—PC AND PD

(MCR 5 = 1, MCR 6 = 0, MCR 7 = 1)

SYMBOL	PARAMETER	1 MHz		2 MHz	
		MIN	MAX	MIN	MAX
T_{PCRS}	(PC5) R/W Setup Time	—	225	—	140
T_{PCAS}	(PC0-PC4, PC6) Address Setup Time	—	200	—	100
T_{PBSU}	(PD) Data Setup Time	50	—	35	—
T_{PBHR}	(PD) Data Read Hold Time	10	—	10	—
T_{PBHW}	(PD) Data Write Hold Time	30	—	30	—
T_{PBDD}	(PD) Data Output Delay	—	175	—	130
T_{PCHA}	(PC0-PC4, PC6) Address Hold Time	30	—	30	—
T_{PCHR}	(PC5) R/W Hold Time	30	—	30	—
T_{PCHV}	(PC7) $\overline{EMS}$ Hold Time	10	—	10	—
T_{PCVP}	(PC7) $\overline{EMS}$ Stabilization Time	30	—	30	—
T_{ESU}	$\overline{EMS}$ Setup Time	—	350	—	210

E.3.1 Abbreviated Mode Timing Diagram



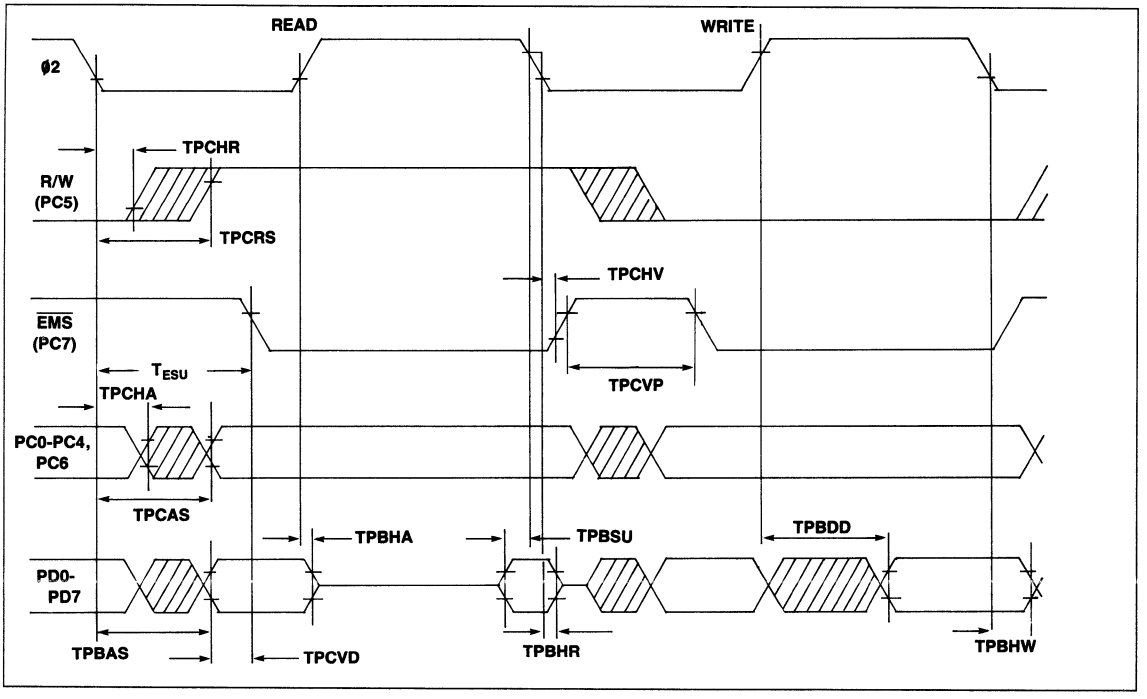
E.4 MULTIPLEXED MODE TIMING—PC AND PD

(MCR 5 = 1, MCR 6 = 1, MCR 7 = 1)

SYMBOL	PARAMETER	1 MHz		2 MHz	
		MIN	MAX	MIN	MAX
T_{PCRS}	(PC5) R/W Setup Time	—	225	—	140
T_{PCAS}	(PC0-PC4, PC6) Address Setup Time	—	200	—	100
T_{PBAS}	(PD) Address Setup Time	—	220	—	120
T_{PBSU}	(PD) Data Setup Time	50	—	35	—
T_{PBHR}	(PD) Data Read Hold Time	10	—	10	—
T_{PBHW}	(PD) Data Write Hold Time	30	—	30	—
T_{PBDD}	(PD) Data Output Delay	—	175	—	140
T_{PCHA}	(PC0-PC4, PC6) Address Hold Time	30	—	30	—
T_{PBHA}	(PD) Address Hold Time	10	100	10	80
T_{PCHR}	(PC5) R/W Hold Time	30	—	30	—
T_{PCHV}	(PC7) $\overline{EMS}$ Hold Time	10	—	10	—
T_{PCVD}[1]	(PC7) Address to $\overline{EMS}$ Delay Time	30		30	
T_{PCVP}	(PC7) $\overline{EMS}$ Stabilization Time	30	—	30	—
T_{ESU}	$\overline{EMS}$ Setup Time	—	350	—	210

NOTE 1 Values assume PC0-PC4, PC6 and PC7 have the same capacitive load

E.4.1 Multiplex Mode Timing Diagram

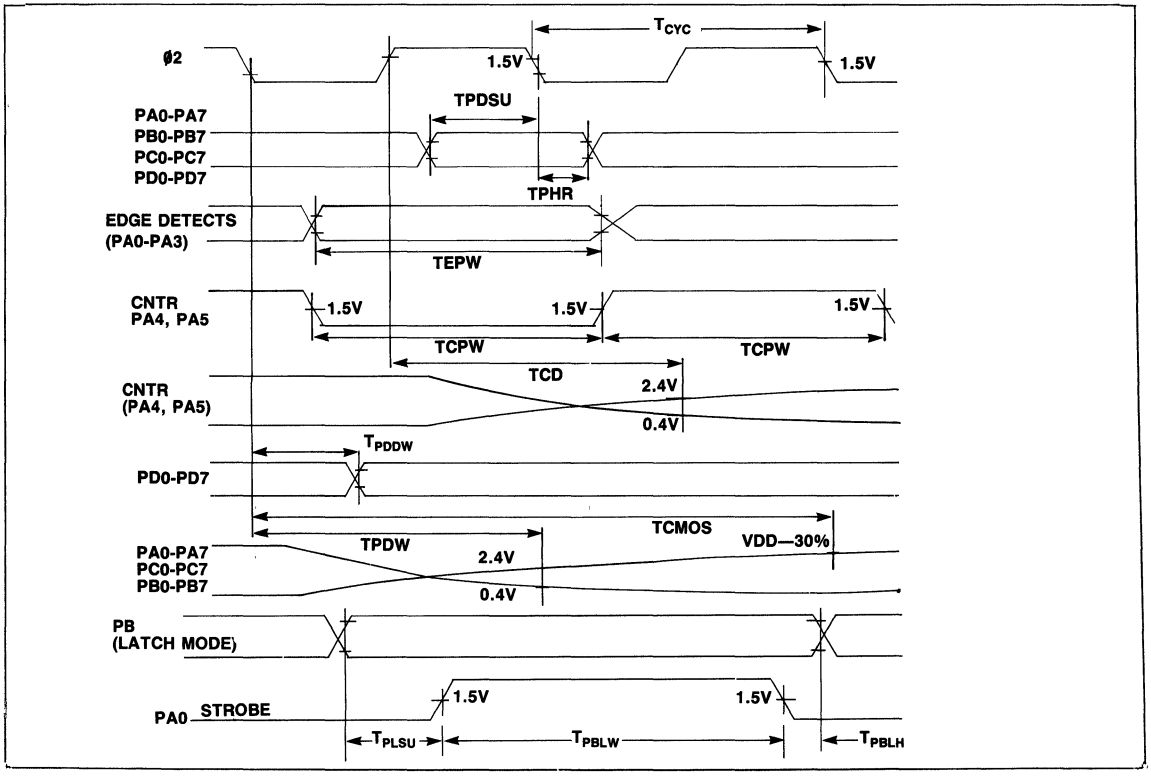


E.5 I/O, EDGE DETECT, COUNTERS, AND SERIAL I/O TIMING

SYMBOL	PARAMETER	1 MHz		2 MHz	
		MIN	MAX	MIN	MAX
	Internal Write to Peripheral Data Valid				
T_{PDW}(1)	PA, PB, PC TTL	—	500	—	500
T_{CMOS}(1)	PA, PB, PC CMOS	—	1000	—	1000
T_{PDDW}	PD	—	175	—	150
	Peripheral Data Setup Time				
T_{PDSU}	PA, PB, PC	200	—	200	—
T_{PDSU}	PD	50	—	50	—
	Peripheral Data Hold Time				
T_{PHR}	PA, PB, PC	75	—	75	—
T_{PHR}	PD	10	—	10	—
T_{EPW}	PA0–PA3 Edge Detect Pulse Width	T_{CYC}	—	T_{CYC}	—
	Counters A and B				
T_{CPW}	PA4, PA5 Input Pulse Width	T_{CYC}	—	T_{CYC}	—
T_{CD}(1)	PA4, PA5 Output Delay	—	500	—	500
	Port B Latch Mode				
T_{PBLW}	PA0 Strobe Pulse Width	T_{CYC}	—	T_{CYC}	—
T_{PLSU}	PB Data Setup Time	175	—	150	—
T_{PBLH}	PB Data Hold Time	30	—	30	—
	Serial I/0				
T_{PDW}(1)	PA6 XMTR TTL	—	500	—	500
T_{CMOS}(1)	PA6 XMTR CMOS	—	1000	—	1000
T_{CPW}	PA4 RCVR S/R Clock Width	4 T_{CYC}	—	4 T_{CYC}	—
T_{PDW}(1)	PA4 XMTR Clock—S/R Mode (TTL)	—	500	—	500
T_{CMOS}(1)	PA4 XMTR Clock—S/R Mode (CMOS)	—	1000	—	1000

NOTE 1 Maximum Load Capacitance. 50pF
Passive Pull-Up Required

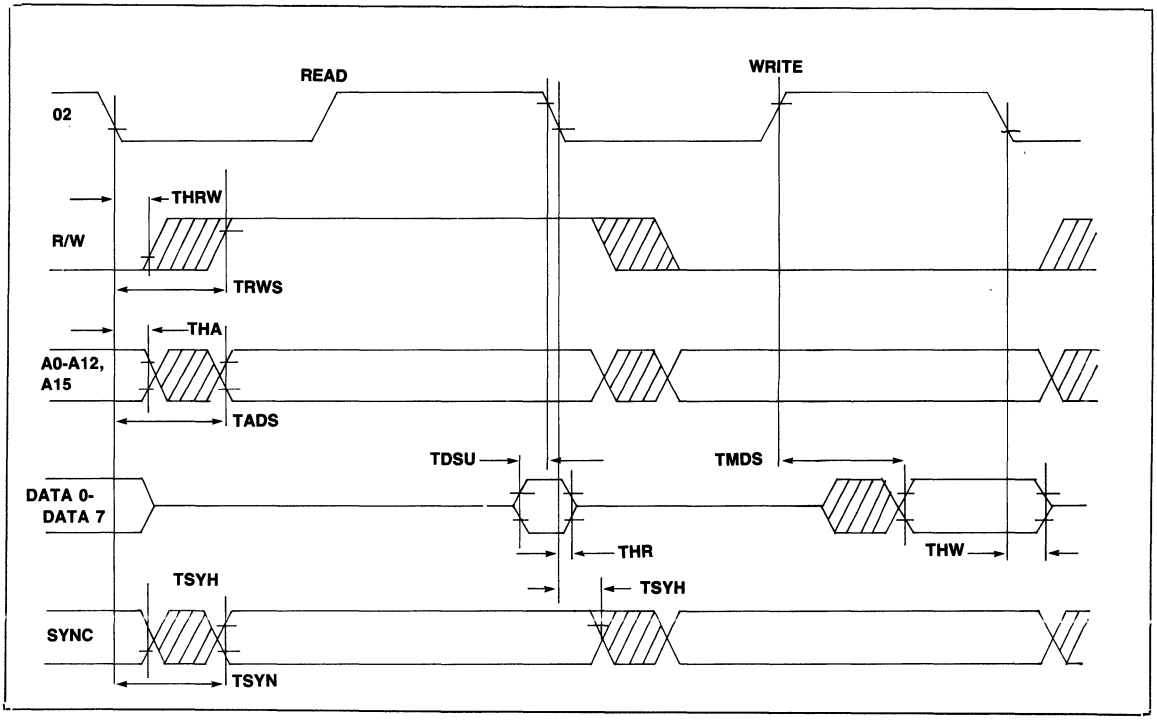
E.5.1 I/O, Edge Detect, Counter, and Serial I/O Timing



E.6 MICROPROCESSOR TIMING (D0-D7, A0-A12, A15, SYNC, R/W)

SYMBOL	PARAMETER	1 MHz		2 MHz	
		MIN	MAX	MIN	MAX
T_{RWS}	R/W Setup Time	—	225	—	140
T_{ADS}	A0-A12, A15 Setup Time	—	225	—	140
T_{DSU}	D0-D7 Data Setup Time	50	—	35	—
T_{HR}	D0-D7 Read Hold Time	10	—	10	—
T_{HW}	D0-D7 Write Hold Time	30	—	30	—
T_{MOS}	D0-D7 Write Output Delay	—	175	—	150
T_{SYN}	SYNC Setup	—	225	—	175
T_{HA}	A0-A12, A15 Hold Time	30	—	30	—
T_{HRW}	R/W Hold Time	30	—	30	—
T_{ACC}	External Memory Access Time $T_{ACC} = T_{CYC} - T_F - T_{ADS} - T_{DSU}$	—	T_{ACC}	—	T_{ACC}
T_{SYH}	SYNC Hold Time	30	—	30	—

E.6.1 Microprocessor Timing Diagram



Rockwell

R6500/41 AND R6500/42 ONE-CHIP INTELLIGENT PERIPHERAL CONTROLLERS

SECTION 1 INTRODUCTION

1.1 FEATURES

- Directly compatible with 6500, 6800, 8080, and Z80 bus families
- Asynchronous Host interface that allows independent clock operation
- Input, Output and Status Registers for CPU/Host data transfer
- Status register for CPU/Host data transfer operations
- Interrupt or polled data interchange with Host
- Enhanced 6502 CPU
  - —Four new bit manipulation instructions:
    - Set Memory Bit (SMB)
    - Reset Memory Bit (RMB)
    - Branch on Bit Set (BBS)
    - Branch on Bit Reset (BBR)
  - —Decimal and binary arithmetic modes
  - —13 addressing modes
  - —True indexing
- 1536-byte mask-programmable ROM
- 64-byte static RAM
- 23 TTL-compatible I/O lines (R6500/41 only)
- 47 TTL-compatible I/O lines (R6500/42 only)
- A 16-bit programmable counter/timer, with latch
  - —Pulse width measurement
  - —Pulse generation
  - —Interval timer
  - —Event counter
- Seven interrupts
  - —Two edge-sensitive lines; one positive, one negative
  - —Reset
  - —Counter Underflow
  - —Host data received
  - —Output Data Register full
  - —Input Data Register empty
- Multiplexed bus expandable to 4K bytes of external memory
- Unmultiplexed bus for Peripheral I/O expansion
- 68% of the instructions are executed in less than 2μs @ 2 MHz
- NMOS-3 silicon gate, depletion load technology
- Single +5V power supply
- 40-pin DIP (R6500/41 only)
- 64-pin QUIP (R6500/42 only)

NOTE

This document describes both the R6500/41 and R6500/42. In the text, the terms IPC or device will be used when describing both parts. The few differences will be described in the text using the terms R6500/41 or R6500/42.

1.2 SUMMARY

The Rockwell R6500/41 and R6500/42 One-Chip Intelligent Peripheral Controllers (IPC) are general purpose, programmable interface I/O devices designed for use with a variety of 8-bit and 16-bit microprocessor systems. The one-chip R6500/41 IPC has an enhanced R6502 CPU, 1.5K by 8-bit ROM, 64 by 8-bit RAM, three I/O ports with multiplexed special functions, and a multi-function timer all contained within a 40-pin package.

For systems requiring additional I/O ports, the device is also available in a 64-pin QUIP version, R6500/42, that provides three additional 8-bit ports. In both versions, special interface registers allow these IPC devices to function as peripheral controllers for the 6500, 6800, Z80, 8080, and other 8-bit or 16-bit host microcomputer systems.

The innovative architecture and the demonstrated high performance of the R6502 CPU, as well as instruction simplicity, results in system cost-effectiveness and a wide range of computational power. These features make the device a leading candidate for IPC computer applications.

To facilitate system and program development for the device Rockwell has developed the R6541Q which can be used as an Emulator. A description of the R6541Q is contained in the R6541Q Product Description (Document Order No. 2136).

Rockwell supports development of the R6500/41 and R6500/42 with the System 65 Microcomputer Development System and the R6500/★ Family of Personality Modules. Complete in-circuit emulation with the R6500/★ Family of Personality Modules allows total system test and evaluation.

This product description is for the reader familiar with the R6502 CPU hardware and programming capabilities. A detailed description of the R6502 CPU hardware is included in the R6500 Microcomputer System Hardware Manual (Order Number 201). A description of the instruction capabilities of the R6502 CPU is contained in the R6500 Microcomputer System Programming Manual (Order Number 202).

1.3 MASK OPTIONS

The R6500/41 has provision for internal pull-up resistors on PA and PC ports as a mask option. This option is available for port groups only, not for individual port lines.

The R6500/42 has provision for pull-up resistors on PA, PC, PF, and PG ports as a mask option. This option is available for port groups only, not for individual port lines.

SECTION 2
INTERFACE REQUIREMENTS

This section describes the interface requirements for the Intelligent Peripheral Controller. Figure 2-1 is the Interface Diagram for the devices. Figures 2-2 and 2-4 show the pin out configurations and Table 2-1 describes the function of each pin of the devices. Figures 2-3 and 2-5 show the mechanical dimensions of the devices. Section 5 describes the Host computer interface protocol and timing requirements.

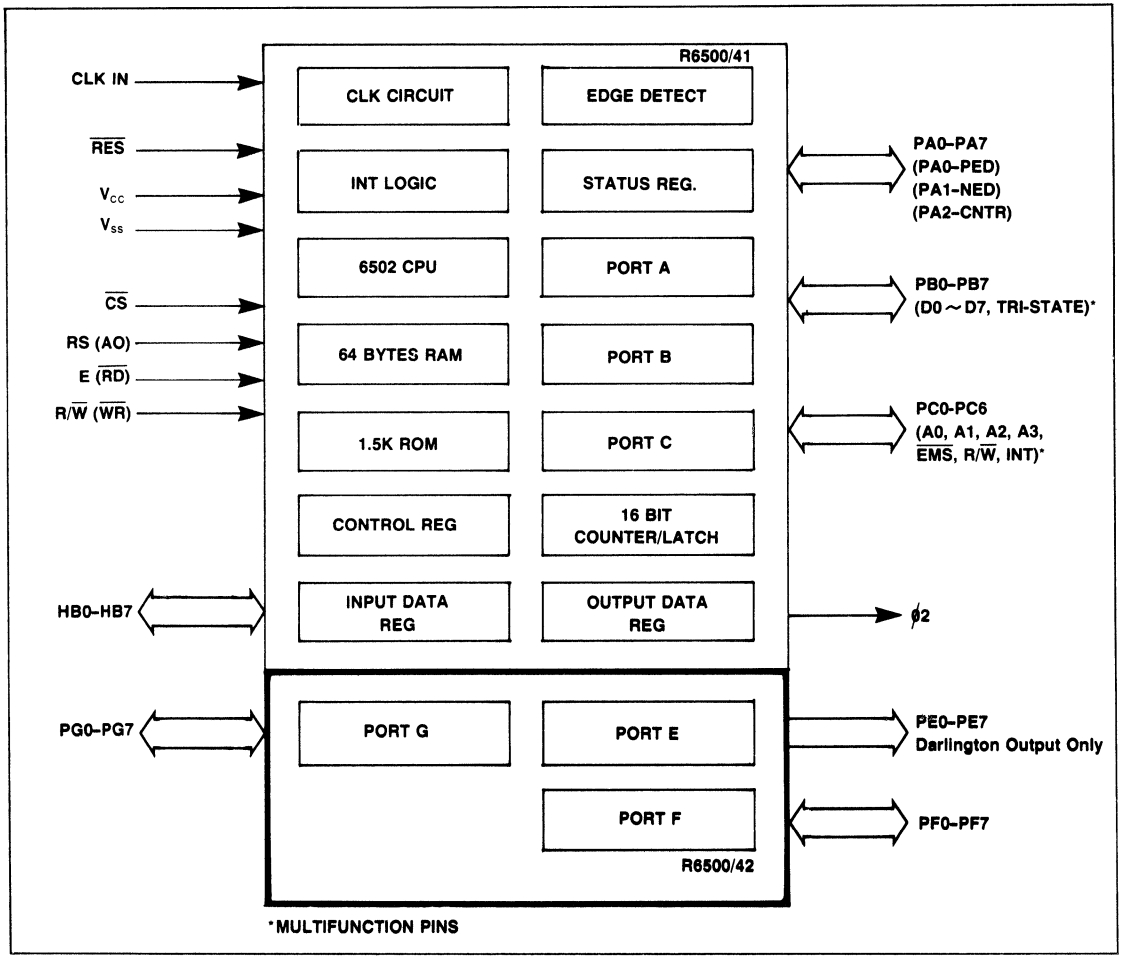


Figure 2-1. Interface Diagram

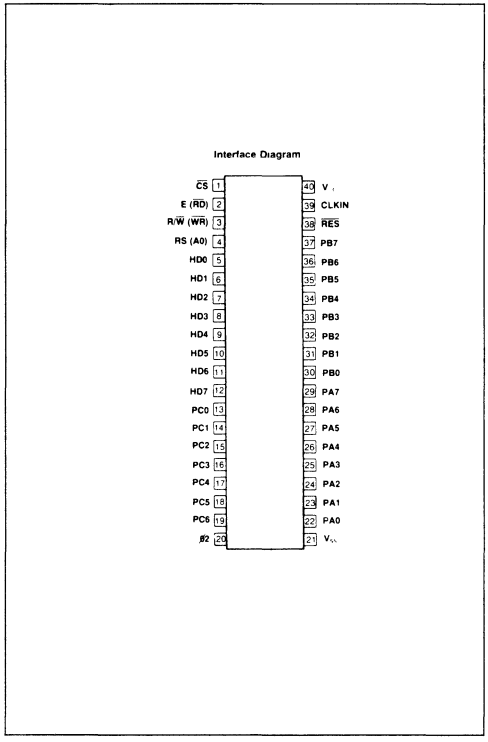


Figure 2.2 R6500/41 Pin Out Designation (40 PIN DIP)

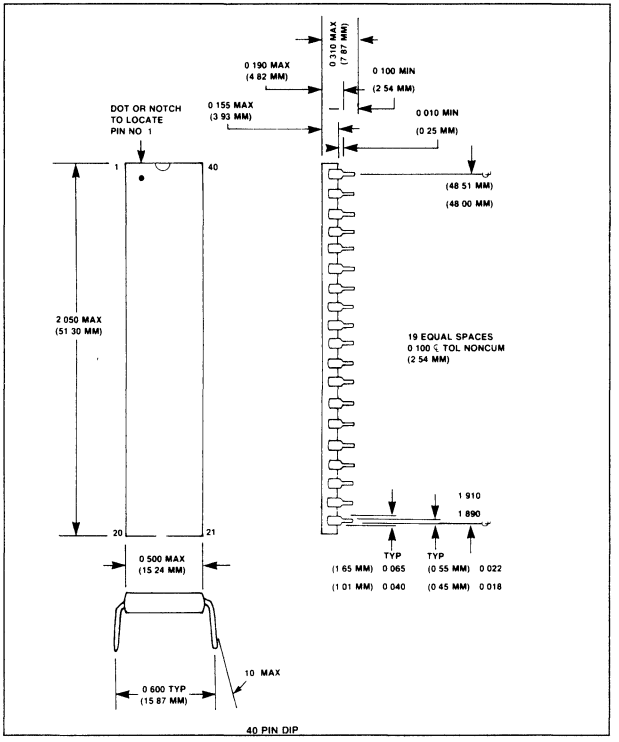


Figure 2-3. R6500/41 Dimensional Outline

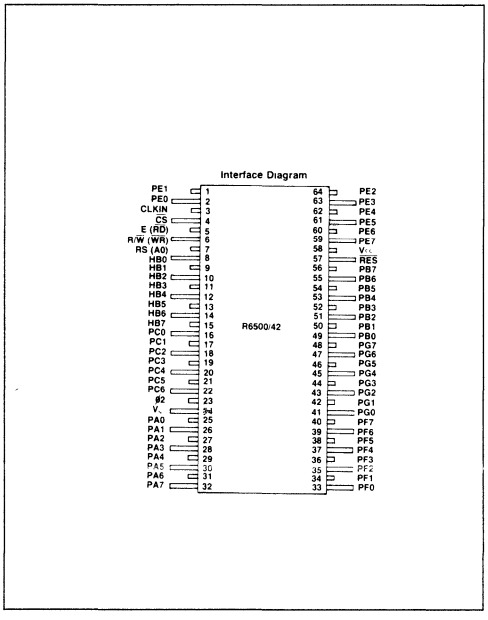


Figure 2-4. R6500/42 Pin Out Designation (64 PIN QUIP)

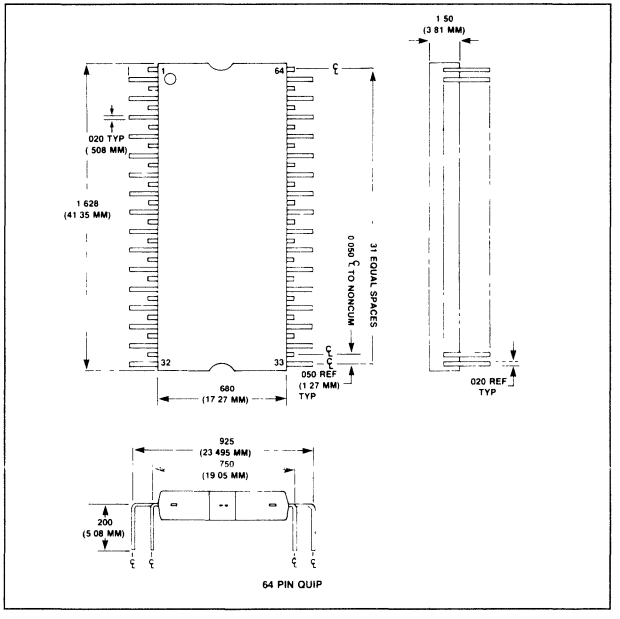


Figure 2-5. R6500/42 Dimensional Outline

Table 2-1. Pin Description

SIGNAL NAME	PIN NO. R6500/41	PIN NO. R6500/42	DESCRIPTION
CLKIN	39	3	Symmetrical square wave 100 KHz to 2 MHZ, TTL compatible input
ø2	20	23	Output timing signal—This is an internally synchronized 1 × clock output suitable for external memory or peripheral interfacing
$\overline{RES}$	38	57	The reset input is used to initialize the device Section 7 describes the process and conditions of the $\overline{RES}$ procedure
VCC	40	58	Power supply input (+5V)
VSS	21	24	Signal and power ground (OV)
$\overline{CS}$	1	4	Chip select pin
RS (A0)	4	7	Register select input pin used by the Host processor to indicate that information being written into the IPC is a data or command byte or to indicate that information being read from the IPC is a status or data byte
E ($\overline{RD}$)	2	5	Host timing control signal for data register write and read
R/$\overline{W}$ ($\overline{WR}$)	3	6	Host timing control signal for data register write and read.
HB0-HB7	5-12	8-15	Data bus between Host and IPC data input and output registers

SIGNAL NAME	PIN NO. R6500/41	PIN NO. R6500/42	DESCRIPTION
PA0-PA7	22-29	25-32	8 bit I/O port used for either input or output Each line consists of an active transistor to V_{SS} and an optional passive pull-up to V_{CC}. The two lower bits PA0 and PA1 also serve as edge detect inputs. PA2 is time shared with the 16 bit Counter Input or output pin, CNTR, and is mode selected
PB0-PB7	30-37	49-56	8 bit I/O port used for either input or output Each line consists of an active transistor to V_{SS} and an active pull-up to V_{CC} This port becomes a tri-state data bus, D0-D7, in the Abbreviated or Multiplexed Bus Mode. D0-D7 are multiplexed with address lines A4-A11 in the Multiplexed Bus Mode
PC0-PC6	13-19	16-22	7 bit I/O port used for either input or output Each line consists of an active transistor to V_{SS} and an optional passive pull-up to V_{CC} The pins PC0 to PC5 are multiplexed with address and control signals for use in abbreviated and multiplex modes. PC6 is multiplexed with $\overline{INT}$ and is program selectable. In these two modes PC0-PC5 have active pull-ups
PE0-PE7 PF0-PF7 PG0-PG7	N/A N/A N/A	1, 2, 64-59 33-40 41-48	For the R6500/42, the 64 pin QUIP version, three additional ports (24 lines) are provided. Each line consists of an active transistor to V_{SS} PF0-PF7 and PG0-PG7 are bidirectional, and an optional passive pull-up to V_{CC} is provided. PE0-PE7 is outputs only with an active pullup. All ports will source 100 μamps. at 2.4v except port E (PE0-PE7) which will source 1 ma at 1 5v

SECTION 3
SYSTEM ARCHITECTURE

This section provides a functional description of the IPC device. Functionally, the device consists of a CPU, both ROM and RAM memories, three parallel I/O ports (six in the 64-pin R6500/42), counter/latch circuit, a mode control register, and an interrupt flag/enable dual register circuit. A block diagram of the system is shown in Figure 3-1.

NOTE

Throughout this document, unless specified otherwise, all memory or register address locations are specified in hexadecimal notation.

3.1 CPU LOGIC

The internal CPU of the device is an enhanced R6502 configuration with an 8-bit Accumulator register, two 8-bit Index Registers (X and Y); an 8-bit Stack Pointer register, an ALU, a 16-bit Program Counter, and standard instruction register/decode and internal timing control logic.

3.1.1 Accumulator

The accumulator is a general purpose 8-bit register that stores the results of most arithmetic and logic operations. In addition, the accumulator usually contains one of the two data words used in these operations.

3.1.2 Index Registers

There are two 8-bit index registers, X and Y. Each index register can be used as a base to modify the address data program counter and thus obtain a new address—the sum of the program counter contents and the index register contents.

When executing an instruction which specifies indirect addressing, the CPU fetches the op code and the address, and modifies the address from memory by adding the index register to it prior to loading or storing the value of memory.

Indexing greatly simplifies many types of programs, especially those using data tables.

3.1.3 Stack Pointer

The Stack Pointer is an 8-bit register. It is automatically incremented and decremented under control of the microprocessor to perform stack manipulation in response to either user instructions, or an internal $\overline{IRQ}$ interrupt. The Stack Pointer must be initialized by the user program.

The stack allows simple implementation of multiple level interrupts, subroutine nesting and simplification of many types of data manipulation. The JSR, BRK, RTI and RTS instructions use the stack and Stack Pointer.

The stack can be envisioned as a deck of cards which may only be accessed from the top. The address of a memory location is stored (or "pushed") onto the stack. Each time data are to be pushed onto the stack, the Stack Pointer is placed on the Address Bus, data are written into the memory location addressed by the Stack Pointer, and the Stack Pointer is decremented by 1. Each time data are read (or "pulled") from the stack, the Stack Pointer is incremented by 1. The Stack Pointer is then placed on the Address Bus, and data are read from the memory location addressed by the Pointer.

The stack is located on zero page, i.e., memory locations 007F-0040. Normal usage calls for the initialization of the Stack Pointer at 007F.

3.1.4 Arithmetic and Logic Unit (ALU)

All arithmetic and logic operations take place in the ALU, including incrementing and decrementing internal registers (except the Program Counter). The ALU cannot store data for more than one cycle. If data are placed on the inputs to the ALU at the beginning of a cycle, the result is always gated into one of the storage registers or to external memory during the next cycle.

Each bit of the ALU has two inputs. These inputs can be tied to various internal buses or to a logic zero; the ALU then generates the function (AND, OR, SUM, and so on) using the data on the two inputs.

3.1.5 Program Counter

The 16-bit Program Counter provides the addresses that are used to step the processor through sequential instructions in a program. Each time the processor fetches an instruction from program memory, the lower (least significant) byte of the Program Counter (PCL) is placed on the low-order bits of the Address Bus and the higher (most significant) byte of the Program Counter (PCH) is placed on the high-order 8 bits of the Address Bus. The Counter is incremented each time an instruction or data is fetched from program memory.

3.1.6 Instruction Register and Instruction Decode

Instructions are fetched from ROM or RAM and gated onto the Internal Data Bus. These instructions are latched into the Instruction Register then decoded along with timing and interrupt signals to generate control signals for the various registers.

3.1.7 Timing Control

The Timing Control Logic keeps track of the specific instruction cycle being executed. This logic is initialized each time an instruction fetch is executed and is advanced at the beginning of each low level of the Clock In pulse for as many cycles as are required to complete the instruction. Each data transfer which takes place between the registers is caused by decoding the contents of both the instruction register and timing control unit.

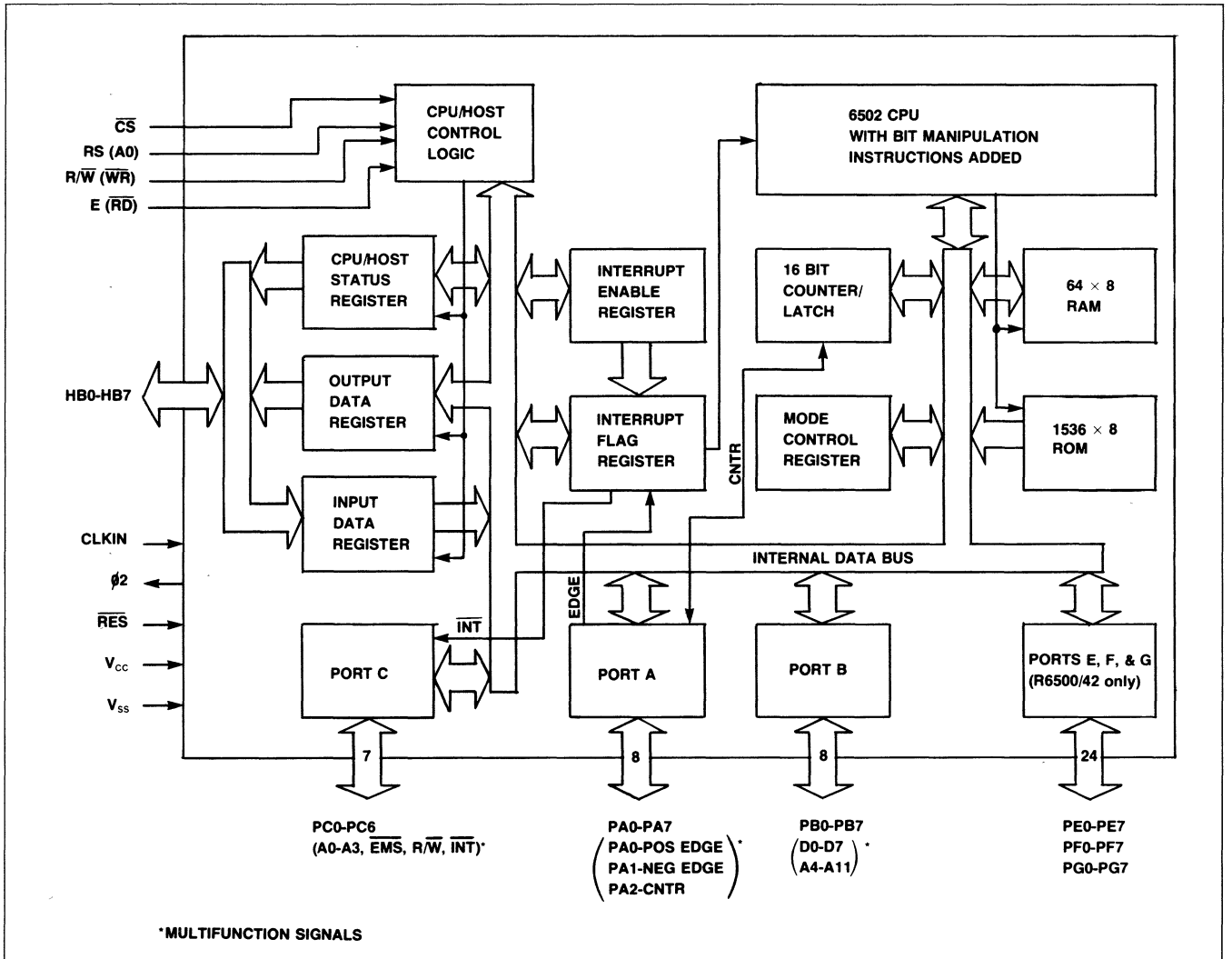


Figure 3-1. R6500/41 & R6500/42 Block Diagram

3.1.8 Interrupt Logic

Interrupt logic controls the sequencing of two interrupts: $\overline{RES}$ and $\overline{IRQ}$. $\overline{IRQ}$ is generated by any one of four conditions: Counter Overflow, Positive Edge Detect, Negative Edge Detect, and Input Data Register Full.

3.2 NEW INSTRUCTIONS

In addition to the standard 6502 instruction set, four instructions have been added to the devices to simplify operations that previously required a read/modify/write operation. In order for these instructions to be equally applicable to any I/O ports, with or without mixed input and output functions, the I/O ports have been designed to read the contents of the specified port data register during the Read cycle of the read/modify/write operation, rather than I/O pins as in normal read cycles. The added instructions and their format are explained in the following subparagraphs. Refer to Appendix A for the Op Code mnemonic addressing matrix for these added instructions.

3.2.1 Set Memory Bit (SMB m, Addr.)

This instruction sets to "1" one of the 8-bit data field specified by the zero page address (memory or I/O port). The first byte of the instruction specifies the SMB operation and 1 of 8 bits to be set. The second byte of the instruction designates address (00-FF) of the byte or I/O port to be operated upon.

3.2.2 Reset Memory Bit (RMB m, Addr.)

This instruction is the same operation and format as SMB instruction except a reset to "0" of the bit results.

3.2.3 Branch on Bit Set Relative (BBS m, Addr, DEST)

This instruction tests one of 8 bits designated by a three bit immediate field within the first byte of the instruction. The second byte is used to designate the address of the byte to be tested within the zero page address range (memory or I/O ports). The third byte of the instruction is used to specify the 8 bit relative address to which the instruction branches if the bit tested is a "1". If the bit tested is not set, the next sequential instruction is executed.

3.2.4 Branch On Bit Reset Relative (BBR m, Addr, DEST)

This instruction is the same operation and format as the BBS instruction except that a branch takes place if the bit tested is a "0".

3.3 READ-ONLY-MEMORY (ROM)

The ROM consists of 1536 bytes (1.5K) mask programmable memory with an address space from FAOO to FFFF. ROM locations FFFC through FFFF are assigned for interrupt and reset vectors.

3.4 RANDOM ACCESS MEMORY (RAM)

The RAM consists of 64 bytes of read/write memory with an assigned page zero address of 0040 through 007F.

3.5 SYSTEM CLOCK

The device functions with an external clock. It is fully asynchronous in reference to the Host computer timing. The device clock frequency equals the external clock frequency. It is also made available for any external device synchronization at pin $\phi 2$.

3.6 MODE CONTROL REGISTER (MCR)

The Mode Control Register contains control bits for the multifunction I/O ports and mode select bits for the Counter, the 6500 or 8080 Bus Select, and the Interrupt ($\overline{INT}$). Its setting determines the basic configuration of the device in any application. Initializing this register is one of the first actions of any software program. The Mode Control Register bit assignment is shown in Figure 3-2.

The use of Counter A Mode Select is shown in Section 6.

The use of the 6500/8080 Host Bus Select is shown in Section 6.

The use of Interrupt Select is shown in Section 4.5.

The use of Bus Mode Select is shown in Sections 4.4 and 4.5.

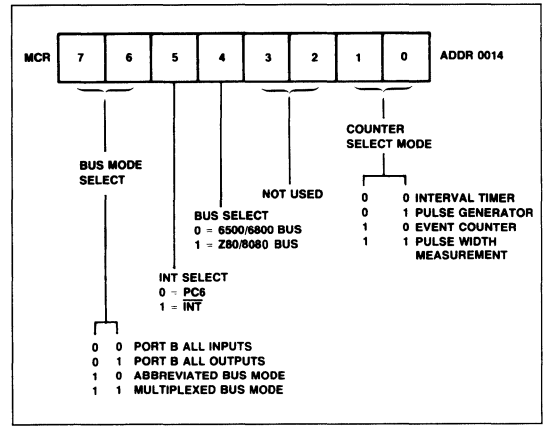


Figure 3-2. Mode Control Register Bit Allocations

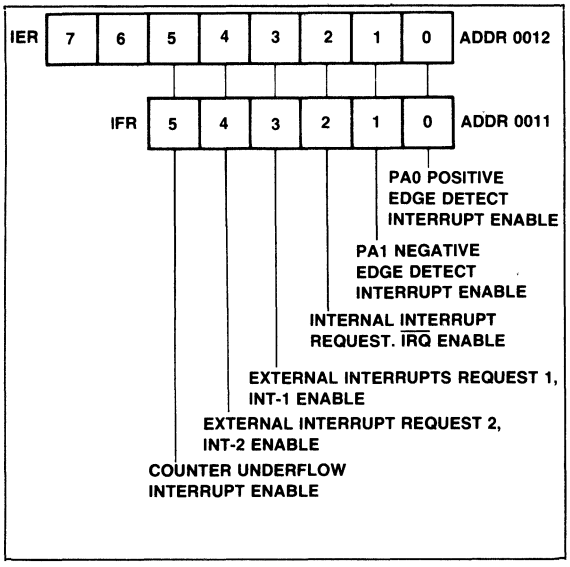


Figure 3-3. Interrupt Enable and Flag Registers

Table 3-1. Interrupt Enable Signals

Control Signal	Description
IER 0	Positive Edge Detect, Interrupt Enable—when this bit is true, a positive going signal on PA0 will generate an $\overline{IRQ}$ and set the corresponding flag bit
IER 1	Negative Edge Detect Interrupt Enable—when this bit is set to a "1" a negative going signal on PA1 will generate an $\overline{IRQ}$ and set the corresponding flag bit.
IER 2	Input Data Register Full Interrupt Enable—setting this bit to a "1" allows an $\overline{IRQ}$ to be generated each time the Host fills the IDR setting the IDFR bit
IER 3	Output Data Register Full Interrupt Enable—when this bit is an interrupt request to the Host is generated each time the ODRF flag is set to a "1". (See External Interrupts, Paragraph 3 7 1) Reading the ODR clears INT-1 and ODRF flags
IER 4	Input Data Register Empty Interrupt Enable—when this is set to a "1" an interrupt is generated to the Host each time the IDR is read by the CPU The interrupt occurs when the IDRF flag is cleared INT-2 is cleared when the Host reads the status flag register (See External Interrupts, Paragraph 3 7 1)
IER 5	Counter Interrupt Enable—if enabled, an $\overline{IRQ}$ is generated whenever the Counter overflows

3.7 INTERRUPT FLAG REGISTER (IFR) AND INTERRUPT ENABLE REGISTER (IER)

An $\overline{IRQ}$ interrupt request can be initiated by any or all of four possible sources. These sources are all capable of being enabled or disabled by the use of the appropriate interrupt enabled bits in the Interrupt Enable Register (IER). Multiple simultaneous interrupts will cause the $\overline{IRQ}$ interrupt request to remain active until all interrupting conditions have been serviced and cleared.

The Interrupt Flag Register contains the information that indicates which I/O or counter needs attention. The contents of the Interrupt Flag Register may be examined at any time by reading at address: 0011. Edge detect IFR bits may be cleared by executing a RMB instruction at address location 0010. The RMB X, (0010) instruction reads FF, modifies bit X to a "0", and writes the modified value at address location 0011. In this way IFR bits set to a "1" after the read cycle of a Read-Modify-Write instruction (such as RMB) are protected from being cleared. IFR bits 6 and 7 are indeterminate on a Read.

Each IFR bit has a corresponding bit in the Interrupt Enable Register which can be set to a "1" by writing a "1" in the respective bit position at location 0012. Individual IER bits may be cleared by writing a "0" in the respective bit position, or by $\overline{RES}$. If set to a "1", an $\overline{IRQ}$ will be generated when the corresponding IFR bit becomes true. The Interrupt Flag Register and Interrupt Enable Register bit assignments are shown in Figure 3-3 and the functions of each bit are explained in Table 3-1

3.7.1 External Interrupts ($\overline{INT}$)

An external interrupt $\overline{INT}$ to the Host computer may be selected in two modes. (See Section 5 for information on the Host/Device interface).

OUTPUT DATA REGISTER (ODR) FULL

When IER 3 of the Interrupt Enable Register is set to a "1", the device will assert the $\overline{INT}$ (PC6) line each time it loads the ODR. The ODRF flag of the Status Flag Register and the IFR 3 of the IFR will be set to a "1" indicating the ODR is full. The ODRF and IFR 3 flags are cleared and $\overline{INT}$ is negated when the Host processor reads the ODR.

INPUT DATA REGISTER (IDR) EMPTY

When IER 4 of the Interrupt Enable Register is set to a "1", the device will assert the $\overline{INT}$ (PC6) line each time it reads the IDR. The IDRF flag of the Host Status Flag Register will be cleared and the IFR 4 flag of the IFR will be set to a "1" indicating the IDR has just been read by the device. The IFR 4 flag is cleared and $\overline{INT}$ is negated when the Host processor reads the Host Status Flag Register. $\overline{RES}$ clears the IDR and sets the IFR4 flag to indicate the register is empty.

3.8 PROCESSOR STATUS REGISTER

The 8-bit Processor Status Register, shown in Figure 3-4, contains seven status flags. Some of these flags are controlled by the user program; others may be controlled both by the user's program and the CPU. The R6502 instruction set contains a number of conditional branch instructions which are designed to allow testing of these flags. Each of the eight processor status flags is described in the following sections.

3.8.1 Carry Bit (C)

The Carry Bit (C) can be considered as the ninth bit of an arithmetic operation. It is set to logic 1 if a carry from the eighth bit has occurred or cleared to logic 0 if no carry occurred as the result of arithmetic operations.

The Carry Bit may be set or cleared under program control by use of the Set Carry (SEC) or Clear Carry (CLC) instruction, respectively Other operations which affect the Carry Bit are ADC, ASL, CMP, CPX, CPY, LSR, PLP, ROL, ROR, RTI, and SBC.

3.8.2 Zero Bit (Z)

The Zero Bit (Z) is set to logic 1 by the CPU during any data movement or calculation which sets all 8 bits of the result to zero. This bit is cleared to logic 0 when the resultant 8 bits of a data movement or calculation operation are not all zero. The R6502 instruction set contains no instruction to specifically set or clear the Zero Bit. The Zero Bit is, however, affected by the following instructions; ADC, AND, ASL, BIT, CMP, CPX, CPY, DEC, DEX, DEY, EOR, INC, INX, INY, LDA, LDX, LDY, LSR, ORA, PLA, PLP, ROL, ROR, RTI, SBC, TAX, TAY, TXA, TSX, and TYA.

3.8.3 Interrupt Disable Bit (I)

The Interrupt Disable Bit (I) is used to control the servicing of an interrupt request (IRQ). If the I Bit is reset to logic 0, the $\overline{IRQ}$ signal will be serviced. If the bit is set to logic 1, the $\overline{IRQ}$ signal will be ignored. The CPU will set the Interrupt Disable Bit to logic 1 if a RESET ($\overline{RES}$) or Non-Maskable Interrupt ($\overline{NMI}$) signal is detected.

The I bit is cleared by the Clear Interrupt Mask Instruction (CLI) and is set by the Set Interrupt Mask Instruction (SEI). This bit may also be set by the BRK Instruction. The Return from Interrupt (RTI) and Pull Processor Status (PLP) instructions will also affect the I bit.

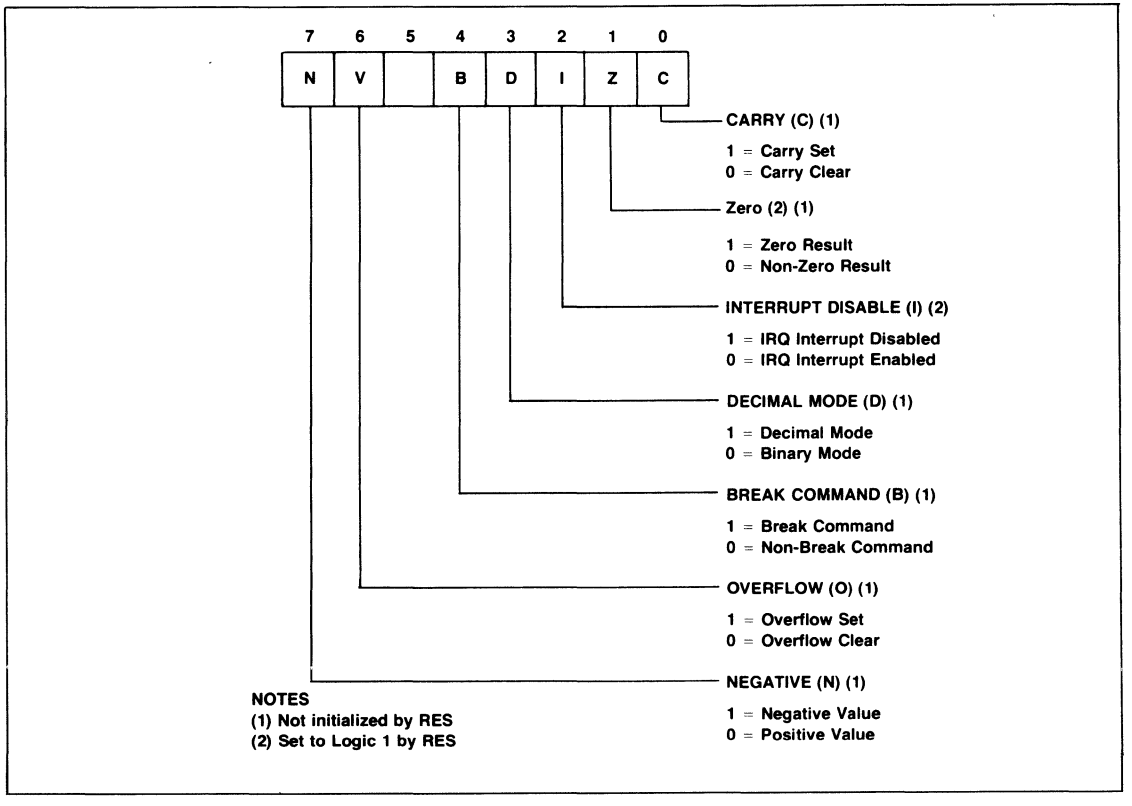


Figure 3-4. Processor Status Register

3.8.4 Decimal Mode Bit (D)

The Decimal Mode Bit (D), is used to control the arithmetic mode of the CPU. When this bit is set to logic 1, the adder operates as a decimal adder. When this bit is cleared to logic 0, the adder operates as a straight binary adder. The adder mode is controlled only by the programmer. The Set Decimal Mode (SED) instruction will set the D bit; the Clear Decimal Mode (CLD) instruction will clear it. The PLP and RTI instructions also effect the Decimal Mode Bit.

CAUTION

The Decimal Mode Bit will either set or clear in an unpredictable manner upon power application to the device. This bit must be initialized to the desired state by the user program or erroneous results may occur

3.8.5 Break Bit (B)

The Break Bit (B) is used to determine the condition which caused the $\overline{IRQ}$ service routine to be entered If the $\overline{IRQ}$ service routine was entered because the CPU executed a BRK command, the Break Bit will be set to logic 1 If the $\overline{IRQ}$ routine was entered as the result of an $\overline{IRQ}$ signal being generated, the B bit will be cleared to logic 0. There are no instructions which can set or clear this bit

3.8.6 Overflow Bit (V)

The Overflow Bit (V) is used to indicate that the result of a signed, binary addition, or subtraction, operation is a value that cannot be contained in seven bits ($-128 \leq n \leq 127$). This indicator only has meaning when signed arithmetic (sign and seven magnitude bits) is performed. When the ADC or SBC instruction is performed, the Overflow Bit is set to logic 1 if the polarity of the sign bit (bit 7) is changed because the result exceeds +127 or −128, otherwise the bit is cleared to logic 0. The V bit may also be cleared by the programmer using a Clear Overflow (CLV) instruction.

The Overflow Bit may also be used with the BIT instruction. The BIT instruction which may be used to sample interface devices, allows the overflow flag to reflect the condition of bit 6 in the sampled field. During a BIT instruction the Overflow Bit is set equal to the content of the bit 6 on the data tested with BIT instrction. When used in this mode, the overflow has nothing to do with signed arithmetic, but is just another sense bit for the microprocessor. Instructions which affect the V flag are ADC, BIT, CLV, PLP, RTI and SBC.

3.8.7 Negative Bit (N)

The Negative Bit (N) is used to indicate that the sign bit (bit 7), in the resulting value of a data movement or data arithmetic operation, is set to logic 1. If the sign bit is set to logic 1, the resulting value of the data movement or arithmetic operation is negative, if the sign bit is cleared, the result of the data movement or arithmetic operation is positive. There are no instructions that set or clear the Negative Bit since the Negative Bit represents only the status of a result. The instructions that effect the state of the Negative Bit are. ADC, AND, ASL, BIT, CMP, CPX, CPY, DEC, DEX, DEY, EOR, INC, INX, INY, LDA, LDX, LDY, LSR, ORA, PLA, PLP, ROL, ROR, RTI, SBC, TAX, TAY, TSX, TXA, and TYA.

SECTION 4
PARALLEL INPUT/OUTPUT PORTS

INPUT/OUTPUT PORTS

The IPC device provides three ports (PA, PB, and PC). The 15 lines of PA and PC are completely bidirectional, that is, there are no line grouping or port association restrictions. The eight lines of Port B may be programmed as all inputs or all outputs. Port PC, however, may be multiplexed under program control with seven other signals. Six of these signals form an address and control bus for extended addressing. The seventh signal is multiplexed with an external interrupt output, $\overline{INT}$. All eight Port B lines are tri-state to permit their use as a data bus during extended addressing modes.

The R6500/42, a 64 pin QUIP device, has three additional ports: PE, PF, and PG. PE is outputs only. PF and PG are bidirectional.

Internal pull-up resistors (FET's with an impedance range of $3K \leq Rpu \leq 12K$ ohm) may be provided on ports PA and PC and ports PF & PG (R6500/42 only), as a mask option.

The direction of the I/O lines are controlled by 8-bit port registers located in page zero. This arrangement provides quick programming access using simple two-byte zero page address instructions. There are no direction registers associated with the I/O ports, which simplifies I/O handling. The I/O addresses are shown in Table 4-1. Section E.6 shows the I/O Port Timing.

Table 4-1. I/O Port Addresses

PORT		ADDRESS
A		0000
B		0001
C		0002
E	R6500/42 only.	0004
F		0005
G		0006

4.1 INPUTS

Inputs for Ports A and C, and also Ports F and G of the R6500/42, are enabled by loading logic 1 into all I/O port register bit positions that are to correspond to I/O input lines. A low (<0.8V) input signal will cause a logic 0 to be read when a read instruction is issued to the port register. A high (>2.0V) input will cause a logic 1 to be read. An $\overline{RES}$ signal forces all I/O port registers to logic 1 thus initially treating all I/O lines as inputs.

Port B may be all inputs or all outputs. All inputs is selected by setting bits MCR6 and MCR7 of the Mode Control Register to a "0".

The status of the input lines can be interrogated at any time by reading the I/O port addresses. Note that this will return the actual status of the input lines, not the data written into the I/O port registers.

Read/Modify/Write instructions can be used to modify the operation of PA, PB, PC, and also PF, & PG of the R6500/42. During the Read cycle of a Read/Modify/Write instruction the Port I/O register is read. For all other read instructions the port input lines are read. Read/Modify/Write instructions are: ASL, BBS, BBR, DEC, INC, LSR, RMB, ROL, ROR, and SMB.

4.2 OUTPUTS

Outputs for Ports A thru C, and Ports E thru G of the R6500/42, are controlled by writing the desired I/O line output states into the corresponding I/O port register bit positions. A logic 1 will force a high (>2.4V) output while a logic 0 will force a low (<0.4V) output. Port B also requires that MCR6 be set to a "1" and MCR7 be set to a "0".

4.3 PORT A (PA)

Port A can be programmed via the Mode Control Register (MCR) as a standard parallel 8-bit, bit independent, I/O port, or a counter I/O line. Table 4-2 tabulates the control and usage of Port A.

In addition to their normal I/O functions, PA0 can detect positive going edges, and PA1 can detect negative going edges. An edge transition on these pins will set a corresponding status bit in the IFR and generate an interrupt request if the respective Interrupt Enable Bit is set. The maximum rate at which an edge can be detected is one-half the $\phi 2$ clock rate. Edge detection timing is shown in Section E.5.

Table 4-2. Port A Control & Usage

PA0-PA1 I/O		PA2 I/O		PA2 COUNTER				PA3-PA7 I/O	
		MCR0 = 0 MCR1 = 0		MCR0 = 1 MCR1 = 0		MCR0 = X MCR1 = 1			
SIGNAL		SIGNAL		SIGNAL		SIGNAL		SIGNAL	
NAME	TYPE	NAME	TYPE	NAME	TYPE	NAME	TYPE	NAME	TYPE
PA0 (1) PA1(2)	I/O I/O	PA2	I/O	CNTR	OUTPUT	CNTR	INPUT (3)	PA3-PA7	I/O

(1) POSITIVE EDGE DETECT (2) NEGATIVE EDGE DETECT (3) HARDWARE BUFFER FLOAT

4.4 PORT B (PB)

Port B can be programmed as an I/O Port, an 8-bit tri-state data bus, or as a multiplexed bus. Mode selection for Port B is made by the Mode Control Register (MCR). The Port B output drivers can be selected as tri-state output drivers by setting bit 7 of the MCR to 0 (zero) and bit 6 of the MCR to 1. An all inputs condition is created by setting both MCR6 and MCR7 to 0 (zero) Table 4-3 shows the necessary settings for the MCR to achieve the various modes for Port B. When Port B is selected to operate in the Abbreviated Mode PB0-PB7 serves as data register bits D0-D7. When Port B is selected to operate in the Multiplexed Mode data bits D0 through D7 are time multiplexed with address bits A4 through A11, respectively Refer to the Memory Maps (Appendix B) for Abbreviated and Multiplexed memory assignments. See Appendix E.3 through E.5 for Port B timing.

4.5 PORT C (PC)

Port C can be programmed as an I/O port and in conjunction with Port B, as an abbreviated bus, or as a multiplexed bus. When used in the abbreviated or multiplexed bus modes, PC0-PC5 function as A0-A3, R/W, and $\overline{EMS}$, respectively, as shown in Table 4-4. $\overline{EMS}$ (External Memory Select) is asserted (low) whenever the internal processor accesses memory area between 0080 and 0FFF. (See Memory Map, Appendix C). The leading edge of $\overline{EMS}$ may be used to strobe the eight address lines multiplexed on Port B in the Multiplexed Bus Mode. See Appendix E.3 through E.5 for Port C timing.

4.6 PORT E, PORT F AND PORT G (PE, PF & PG) R6500/42 ONLY

Port E only operates in the Output mode. It provides a Darlington output that can source current at the high (1) level. Port F and Port G operate identically and can be programmed as bidirectional I/O ports. They have standard output capability. See Appendix E.3 through E 5 for Port E, F & Port G timing

Table 4-3. Port B Control & Usage

R6500/41 PIN #	R6500/42 PIN #	I/O MODES MCR7 = 0 MCR6 = 0 SIGNAL NAME	I/O MODES TYPE (1)	MCR7 = 0 MCR6 = 1 SIGNAL NAME	TYPE (2)	ABBREVIATED MODE MCR7 = 1 MCR6 = 0 SIGNAL NAME	TYPE (3)	MULTIPLEXED MODE MCR7 = 1 MCR6 = 1 PHASE 1 SIGNAL NAME	TYPE (2)	PHASE 2 SIGNAL NAME	TYPE (3)
30	49	PB0	INPUT	PB0	OUTPUT	D0	I/O	A4	OUTPUT	D0	I/O
31	50	PB1	INPUT	PB1	OUTPUT	D1	I/O	A5	OUTPUT	D1	I/O
32	51	PB2	INPUT	PB2	OUTPUT	D2	I/O	A6	OUTPUT	D2	I/O
33	52	PB3	INPUT	PB3	OUTPUT	D3	I/O	A7	OUTPUT	D3	I/O
34	53	PB4	INPUT	PB4	OUTPUT	D4	I/O	A8	OUTPUT	D4	I/O
35	54	PB5	INPUT	PB5	OUTPUT	D5	I/O	A9	OUTPUT	D5	I/O
36	55	PB6	INPUT	PB6	OUTPUT	D6	I/O	A10	OUTPUT	D6	I/O
37	56	PB7	INPUT	PB7	OUTPUT	D7	I/O	A11	OUTPUT	D7	I/O

(1) TRI-STATE BUFFER IS IN HIGH IMPEDANCE MODE (2) TRI-STATE BUFFER IS IN ACTIVE MODE
(3) TRI-STATE BUFFER IS IN ACTIVE MODE ONLY DURING THE PHASE 2 PORTION OF A WRITE CYCLE

Table 4-4. Port C Control & Usage

R6500/41 PIN #	R6500/42 PIN #	I/O MODE MCR7 = 0 MCR6 = X SIGNAL NAME	I/O MODE TYPE (1)	ABBREVIATED MODE MCR7 = 1 MCR6 = 0 SIGNAL NAME	TYPE (2)	MULTIPLEXED MODE MCR7 = 1 MCR6 = 1 SIGNAL NAME	TYPE (2)
13	16	PC0	I/O	A0	OUTPUT	A0	OUTPUT
14	17	PC1	I/O	A1	OUTPUT	A1	OUTPUT
15	18	PC2	I/O	A2	OUTPUT	A2	OUTPUT
16	19	PC3	I/O	A3	OUTPUT	A3	OUTPUT
17	20	PC4	I/O	$\overline{EMS}$	OUTPUT	$\overline{EMS}$	OUTPUT
18	21	PC5	I/O	R/$\overline{W}$	OUTPUT	R/$\overline{W}$	OUTPUT
19	22	PC6*	I/O	$\overline{INT}$*	OUTPUT	$\overline{INT}$*	OUTPUT

(1) RESISTIVE PULL-UP, ACTIVE BUFFER PULL-DOWN
(2) ACTIVE BUFFER PULL-UP AND PULL-DOWN

*PC6 if MCR5 = 0, $\overline{INT}$ if MCR5 = 1

SECTION 5
HOST INTERFACE BUS

Two way data transfers are performed between the IPC and the Host microprocessor by means of the Output Data Register and the Input Data Register. The Host can also write a command to the IDR and read from the Host Status Flag Register. Table 5-1 shows the Host addressing matrix. A hardware interrupt procedure and a software polling procedure is available to control data traffic between the CPU and Host.

Table 5-1. Host Addressing Matrix

RS (A_0)	READ	WRITE
1	HOST STATUS FLAG	COMMAND INPUT
0	DATA REG OUTPUT	DATA REG INPUT

5.1 DATA REGISTERS

The device has an 8-bit Input Data Register (IDR) and an 8-bit Output Data Register (ODR). The IDR serves as a temporary storage for commands and data from the Host to the device. When transferring data from the Host to the device, the following conditions are in effect:

- $\overline{CS}$ is asserted
- RS (AO) indicates command input or data input.
- The contents of the host data bus (HB0-HB7) are copied into the IDR when the appropriate Host bus write signals are asserted.

The ODR serves as a temporary storage for data from the device to the Host When the Host is reading data from the device, the following conditions are in effect.

- $\overline{CS}$ is asserted
- RS (AO) input selects ODR or HSFR
- The contents of ODR or the Flag Register are placed on the host data bus (HB0-HB7) when the appropriate Host read signals are asserted.

5.2 HOST STATUS FLAG REGISTER

A Host Status Flag Register facilitates a software protocol that permits independent and uninterrupted flow of data asynchronously between the host computer and the device.

The Host Status Flag Register contains 8 flag bits that can be read at anytime by either the Host or the device See Figure 5-1. General purpose flags F2 through F6 are serviced by the device in either read or write modes and monitored by the Host (Read Only).

Flag F1 can be read at anytime by either the host or the device. The F1 flag copies the A0 (RS) input signal during any host write data exchange. The device can write to the F1 flag at any time.

The ODRF (Output Data Register Full) flag is set each time the device writes to the Output Data Register. The setting of the ODRF sets the device Interrupt Status Register IFR3 flag. An Output Interrupt ($\overline{INT}$) may be generated under program control by setting IER3 in the interrupt enable register The ODRF flag is reset only by a hardware reset or by the host performing a read on the output data register The ODRF flag is reset following the conclusion of any host output data register read The resetting of the ODRF causes the reset of the IFR3 flag and thus the reset of the external interrupt ($\overline{INT}$).

The IDRF (Input Data Register Full) flag is set following the conclusion of any host write data exchange The setting of the IDRF causes IFR2 of the device status register to be set An internal interrupt may be generated under program control by setting IER2 in the Interrupt Enable Register The setting of IDRF also causes IFR4 to be reset The IDRF resets during device read of the input data register IFR2 sets and IFR4 resets following the reset of IDRF IFR4 may generate an external output interrupt (INT, input buffer empty), under program control by setting IER4 in the interrupt enable register

The Host Status Flag Register is cleared by the $\overline{RES}$ input

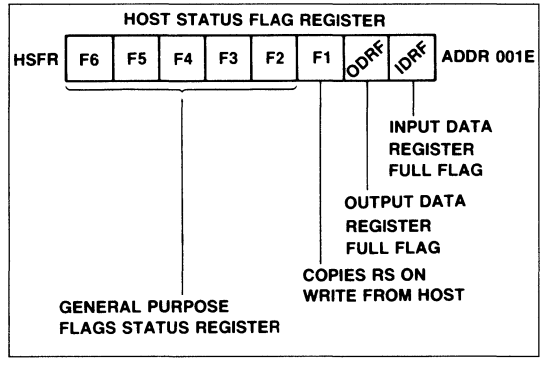


Figure 5-1. Host Status Flag Register Bit Allocation

5.3 HOST COMPUTER INTERFACE

The device will work with a variety of Host Computers The HOST interface consists of a chip select, one address line, 2 control lines and an 8 bit three state data bus. Internal logic of the device, controlled by MCR4, configures, the address and two control lines to either a 6500 or 8080 operational methodology. The interface is completely asynchronous and will work with a Host Computer up to a 5 MHz bus transfer rate The device clock input frequency need not be the same as the Host's. A mode control register is set to match the interface to that of the Host device as follows:

MCR4 = 0 When MCR4 is set to a logic zero, the IPC is configured to operate on a 6502/6800 type host bus. In this mode, the E input is connected to the host transfer strobe (VMA or 02 for 6800, 02 for 6500) and the R/W input is connected to the host microprocessor R/W output line. Figure 5-3 and Table 5-2, together, specify the relevant timing for read and write cycles on this type of host bus.

MCR4 = 1 When MCR4 is set to a logic one, the IPC is configured for operation on an 8080/Z80 type bus. In this mode, the RD input is used as a read strobe and the WR input is connected to the write strobe of the host microprocessor bus. Figure 5-4 and Table 5-3 show the relevant timing characteristics for this mode of operation.

Table 5-2. Host Interface Timing Characteristics BSEL = 0 (6500)

Characteristics 1 and 2 MHz	Symbol	Min	Max
$\overline{CS}$, R/$\overline{W}$, RS Setup Time	t_{CS}	10	—
Access Time	t_{DA}	—	90°
Data Hold Time	t_{DHR}	10	—
Control Hold Time	t_{HC}	10	—
Write Data Setup Time	t_{WDS}	75	—
Write Data Hold Time	t_{DHW}	10	—
Write Stroke Width	t_{WR}	75	—

Note:
90 ns when loading = 130 pF + 1 TTL LOAD and
75 ns when loading = 90 pF + 1 TTL LOAD.

Table 5-3. Host Interface Timing Characteristics BSEL = 1 (8080)

Characteristics 1 and 2 MHz	Symbol	Min	Max
$\overline{CS}$, A0 Setup Time	t_{CS}	10	—
Data Access Time on Read	t_{DA}	—	90°
Data Hold Time	t_{DHR}	10	—
Control Hold Time	t_{HC}	10	—
Write Data Setup Time	t_{WDS}	75	—
Write Data Hold Time	t_{DHW}	10	—
Write Stroke Width	t_{WR}	75	—

Note:
90 ns when loading = 130 pF + 1 TTL LOAD and
75 ns when loading = 90 pF + 1 TTL LOAD.

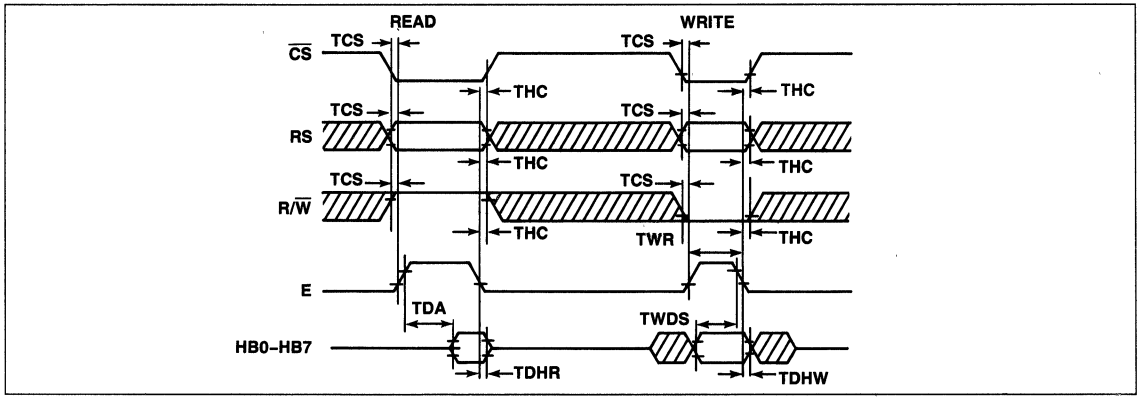


Figure 5-3. Timing Diagram—Host Interface (MCR4 = 0) (6500 Version)

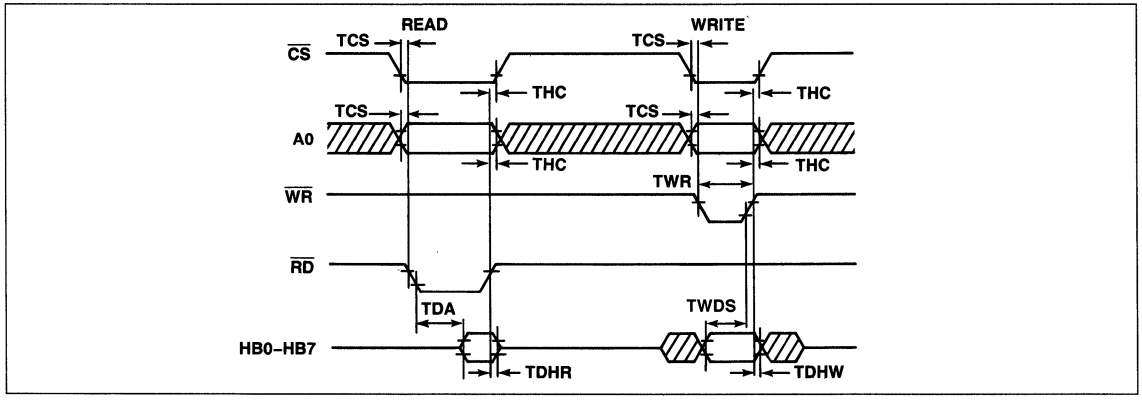


Figure 5-4. Timing Diagram—Host Interface (MCR4 = 1) (8080 Version)

SECTION 6
COUNTER/TIMERS

The device contains a 16-bit counter and a 16-bit latch associated with it The counter can be independently programmed to operate in one of four modes:

Counter

- Pulse width measurement
- Pulse Generation
- Interval Timer
- Event Counter

Operating modes of the Counter are controlled by the Mode Control Register. All counting begins at the initialization value and decrements. When modes are selected requiring a counter input/output line, PA2 is selected for Counter I/O.

6.1 COUNTER

The Counter consists of a 16-bit counter and a 16-bit latch organized as follows: Lower Counter (LC), Upper Counter (UC), Lower Latch (LL), and Upper Latch (UL). The counter contains the count of either $\phi 2$ clock pulses or external events, depending on the counter mode selected The contents of the Counter may be read any time by executing a read at location 0018 for the Upper Counter and at location 001A or location 0019 for the Lower Counter. A read at location 0019 also clears the Counter Underflow Flag (IFR5)

The 16-bit latch contains the counter initialization value, and can be loaded at any time by executing a write to the Upper Latch at location 0018 and the Lower Latch at location 001A. In either case, the contents of the accumulator are copied into the applicable latch register.

The Counter can be started at any time by writing to address 0019. The contents of the accumulator will be copied into the Upper Latch before the contents of the 16-bit latch are transferred to the Counter. The counter is set to the latch value whenever the Counter underflows. When the Counter decrements from 0000 the next counter value will be the latch value, not FFFF, and the Counter Underflow Flag (IFR 5) will be set to "1". This bit may be cleared by reading the Lower Counter at location 0019, by writing to address location 0019, or by $\overline{RES}$.

The Counter operates in any of four modes. These modes are selected by the Counter Mode Control bits in the Control Register

MCR1 (bit 1)	MCR0 (bit 0)	Mode
0	0	Interval Timer
0	1	Pulse Generation
1	0	Event Counter
1	1	Pulse Width Measurement

The Interval Timer, Pulse Generation, and Pulse Width Measurement Modes are $\phi 2$ clock counter modes The Event Counter Mode counts the occurrences of an external event on the CNTR line (PA2)

The Counter is set to the Interval Timer Mode (00) when a $\overline{RES}$ signal is generated

6.1.1 Interval Timer Mode

In the Interval Timer mode the Counter is initialized to the Latch value by either of two conditions

1. When the Counter is decremented from 0000, the next Counter value is the Latch value (not FFFF)

2. When a write operation is performed to the Load Upper Latch and Transfer Latch to Counter address 0019, the Counter is loaded with the Latch value. Note that the contents of the Accumulator are loaded into the Upper Latch before the Latch value is transferred to the Counter.

The Counter value is decremented by one count at the $\phi 2$ clock rate. The 16-bit Counter can hold from 1 to 65535 counts The Counter Timer capacity is therefore 1μs to 65.535 ms at the 1 MHz $\phi 2$ clock rate or 0.5μs to 32 767 ms at the 2 MHz $\phi 2$ clock rate Time intervals greater than the maximum Counter value can be easily measured by counting $\overline{IRQ}$ interrupt requests in the counter $\overline{IRQ}$ interrupt routine

When the Counter decrements from 0000, the Counter Underflow (IFR5) is set to logic 1 If the Counter Interrupt Enable Bit (IER5) is also set, an $\overline{IRQ}$ interrupt request will be generated. The Counter Underflow bit in the Interrupt Flag Register can be examined in the $\overline{IRQ}$ interrupt routine to determine that the $\overline{IRQ}$ was generated by the Counter Underflow.

While the timer is operating in the Interval Timer Mode, PA2 operates as a PA I/O.

A timing diagram of the Interval Timer Mode is shown in Figure 6-1.

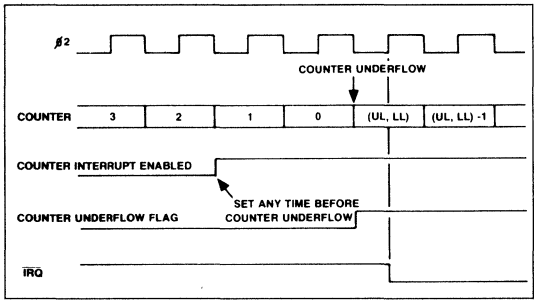


Figure 6-1. Interval Timer Timing Diagram

6.1.2 Pulse Generation Mode

In the Pulse Generation mode, the PA2 line operates as a Counter Output The line toggles from low to high or from high to low whenever a Counter Underflow occurs, or a write is performed to address 0019

The normal output waveform is a symmetrical square-wave The PA2 output is initialized high when entering the mode and transitions low when writing to 0019

Asymmetric waveforms can be generated if the value of the latch is changed after each counter underflow

A one-shot waveform can be generated by changing from Pulse Generation to Interval Timer mode after only one occurrence of the output toggle condition

6.1.3 Event Counter Mode

In this mode PA2 is used as an Event Input line, and the Counter will decrement with each rising edge detected on this line The maximum rate at which this edge can be detected is one-half the ϕ2 clock rate.

The Counter can count up to 65,535 occurrences before underflowing. As in the other modes, the Counter Underflow bit (IER5) is set to logic 1 if the underflow occurs

Figure 6 2 is a timing diagram of the Event Counter Mode

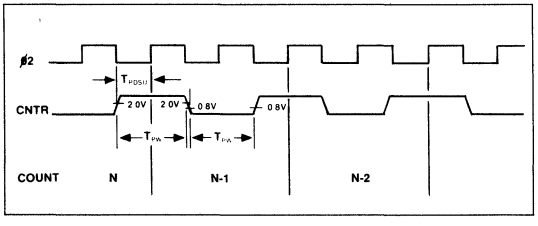
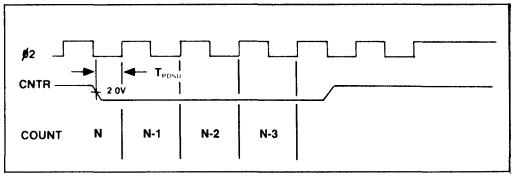


Figure 6-2. Event Counter Mode

6.1.4 Pulse Width Measurement Mode

This mode allows the accurate measurement of a low pulse duration on the PA2 line. The Counter decrements by one count at the ϕ2 clock rate as long as the PA2 line is held in the low state. The Counter is stopped when PA2 is in the high state

The Counter underflow flag will be set only when the count in the timer reaches zero. Upon reaching zero the timer will be loaded with the latch value and continue counting down as long as the PA2 pin is held low. After the counter is stopped by a high level on PA2, the count will hold as long as PA2 remains high. Any further low levels on PA2 will again cause the counter to count down from its present value. The state of the PA2 line can be determined by testing the state of PA2.



SECTION 7
POWER ON/INITIALIZATION CONSIDERATIONS

7.1 POWER ON TIMING

After application of VCC power to the device, $\overline{RES}$ must be held low for at least eight stable $\phi 2$ clock cycles after V_{CC} reaches operating range

Figure 7-1 illustrates the power turn-on waveforms External clock stabilization time is typically 20ms

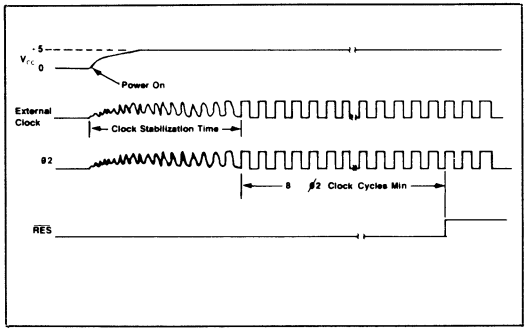


Figure 7-1. Power Turn-On Timing Detail

7.2 POWER-ON RESET

The occurrence of $\overline{RES}$ going from low to high will cause the device to set the Interrupt Mask Bit—bit 2 of the Processor Status Register—and initiate a reset vector fetch at address FFFC and FFFD to begin user program execution All of the I/O ports will be initialized to the high (logic 1) state All bits of the Control Register will be cleared causing the Interval Timer counter mode to be selected and causing all interrupt enabled bits to be reset

7.3 RESET ($\overline{RES}$) CONDITIONS

When $\overline{RES}$ is driven from low to high the device is put in a reset state causing the registers and I/O ports to be set as shown in Table 7-1

Table 7-1. $\overline{RES}$ Initialization of I/O Ports and Registers

BIT NO. ⟶		7	6	5	4	3	2	1	0
REGISTERS									
Processor Status		—	—	—	—	—	1	—	—
Mode Control (MCR)		0	0	0	0	0	0	0	0
Int Enable (IER)		0	0	0	0	0	0	0	0
Int Flag (IFR)		0	0	0	1	0	0	0	0
Host Status Flag		0	0	0	0	0	0	0	0
Input Data		0	0	0	0	0	0	0	0
Output Data		0	0	0	0	0	0	0	0
PORTS									
PA Latch		1	1	1	1	1	1	1	1
PB Latch		1	1	1	1	1	1	1	1
PC Latch		1	1	1	1	1	1	1	1
PE Latch	R6500/42 only	1	1	1	1	1	1	1	1
PF Latch	R6500/42 only	1	1	1	1	1	1	1	1
PG Latch	R6500/42 only	1	1	1	1	1	1	1	1

All RAM and other CPU registers will initialize in a random, non-repeatable data pattern

7.4 INITIALIZATION

Any initialization process for the device should include a $\overline{RES}$ as indicated in the preceding paragraphs. After stabilization of the external clock (if a power on situation) an initialization routine should be executed to perform (as a minimum) the following functions

1. The Stack Pointer should be set
2. Clear or Set Decimal Mode
3. Set or Clear Carry Flag
4. Set up Mode Controls and Counter as required
5. Clear Interrupts.

A typical initialization routine could be as follows

LDX	Load stack pointer starting address into X Register
TXS	Transfer X Register value to Stack Pointer
CLD	Clear Decimal Mode
SEC	Set Carry Flag
	Set-up Mode Control, Counter, special function registers and Clear RAM as required
CLI	Clear Interrupts

APPENDIX A
EXPANDED R6502 INSTRUCTION SET

This appendix contains a summary of the R6502 instruction set. For detailed information, consult the R6502 Microcomputer System Programming Manual, Document 29650 N30.

The four instructions notated with a * are added instructions for the IPC devices which enhance the standard 6502 instruction set.

A.1 INSTRUCTION SET IN ALPHABETIC SEQUENCE

MNEMONIC	INSTRUCTION	MNEMONIC	INSTRUCTION
ADC	Add Memory to Accumulator with Carry	LDA	Load Accumulator with Memory
AND	"AND" Memory with Accumulator	LDX	Load Index X with Memory
ASL	Shift Left One Bit (Memory or Accumulator)	LDY	Load Index Y with Memory
		LSR	Shift One Bit Right (Memory or Accumulator)
*BBR	Branch on Bit Reset Relative		
*BBS	Branch on Bit Set Relative		
BCC	Branch on Carry Clear	NOP	No Operation
BCS	Branch on Carry Set		
BEQ	Branch on Result Zero		
BIT	Test Bits in Memory with Accumulator	ORA	"OR" Memory with Accumulator
BMI	Branch on Result Minus		
BNE	Branch on Result not Zero		
BPL	Branch on Result Plus	PHA	Push Accumulator on Stack
BRK	Force Break	PHP	Push Processor Status on Stack
BVC	Branch on Overflow Clear	PLA	Pull Accumulator from Stack
BVS	Branch on Overflow Set	PLP	Pull Processor Status from Stack
CLC	Clear Carry Flag	*RMB	Reset Memory Bit
CLD	Clear Decimal Mode	ROL	Rotate One Bit Left (Memory or Accumulator)
CLI	Clear Interrupt Disable Bit		
CLV	Clear Overflow Flag	ROR	Rotate One Bit Right (Memory or Accumulator)
CMP	Compare Memory and Accumulator		
CPX	Compare Memory and Index X	RTI	Return from Interrupt
CPY	Compare Memory and Index Y	RTS	Return from Subroutine
DEC	Decrement Memory by One	SBC	Subtract Memory from Accumulator with Borrow
DEX	Decrement Index X by One		
DEY	Decrement Index Y by One	SEC	Set Carry Flag
		SED	Set Decimal Mode
		SEI	Set Interrupt Disable Status
EOR	"Exclusive-Or" Memory with Accumulator	*SMB	Set Memory Bit
		STA	Store Accumulator in Memory
		STX	Store Index X in Memory
		STY	Store Index Y in Memory
INC	Increment Memory by One		
INX	Increment Index X by One		
INY	Increment Index Y by One	TAX	Transfer Accumulator to Index X
		TAY	Transfer Accumulator to Index Y
		TSX	Transfer Stack Pointer to Index X
JMP	Jump to New Location	TXA	Transfer Index X to Accumulator
JSR	Jump to New Location Saving Return Address	TXS	Transfer Index X to Stack Register
		TYA	Transfer Index Y to Accumulator

A.2 R6500/41 AND R6500/42 INSTRUCTION SET SUMMARY TABLE

ADDRESSING MODE

MNEMONIC	OPERATION	IMMEDIATE OP	n	#	ABSOLUTE OP	n	#	ZERO PAGE OP	n	#	ACCUM OP	n	#	IMPLIED OP	n	#
ADC	A+M+C→A (4)(1)	69	2	2	6D	4	3	65	3	2						
AND	A M→A (1)	29	2	2	2D	4	3	25	3	2						
ASL	C← [7 Ø] ←Ø				ØE	6	3	Ø6	5	2	ØA	2	1			
BBR[#(Ø-7)]	Branch on M_b=Ø (5)															
BBS[#(Ø-7)]	Branch on M_b=1 (5)															
BCC	Branch on C=Ø (2)															
BCS	Branch on C=1 (2)															
BEQ	Branch on Z=1 (2)															
BIT	A M				2C	4	3	24	3	2						
BMI	Branch on N=1 (2)															
BNE	Branch on Z=Ø (2)															
BPL	Branch on N=Ø (2)															
BRK	Break													00	7	1
BVC	Branch on V=Ø (2)															
BVS	Branch on V=1 (2)															
CLC	Ø→C													18	2	1
CLD	Ø→D													D8	2	1
CLI	Ø→I													58	2	1
CLV	Ø→V													B8	2	1
CMP	A-M	C9	2	2	CD	4	3	C5	3	2						
CPX	X-M	EØ	2	2	EC	4	3	E4	3	2						
CPY	Y-M	CØ	2	2	CC	4	3	C4	3	2						
DEC	M-1→M				CE	6	3	C6	5	2						
DEX	X-1→X													CA	2	1
DEY	Y-1→Y													88	2	1
EOR	AVM→A (1)	49	2	2	4D	4	3	45	3	2						
INC	M+1→M				EE	6	3	E6								
INX	X+1→X													EB	2	1
INY	Y+1→Y													C8	2	1
JMP	Jump to New Loc				4C	3	3									
JSR	Jump Sub				2Ø	6	3									
LDA	M→A (1)	A9	2	2	AD	4	3	A5	3	2						
LDX	M→X (1)	A2	2	2	AE	4	3	A6	3	2						
LDY	M→Y (1)	AØ	2	2	AC	4	3	A4	3	2						
LSR	Ø→ [7 Ø] →C				4E	6	3	46	5	2	4A	2	1			
NOP	No Operation													EA	2	1
ORA	AVM→A	Ø9	2	2	ØD	4	3	Ø5	3	2						
PHA	A→Ms S-1→S													48	3	1
PHP	P→Ms S-1→S													08	3	1
PLA	S+1→S Ms→A													68	4	1
PLP	S+1→S Ms→P													28	4	1
RMB[#(Ø-7)]	Ø→M_b (5)															
RØL	[7 Ø] ← [C]				2E	6	3	26	5	2	2A	2	1			
RØR	[C] → [7 Ø]				6E	6	3	66	5	2	6A	2	1			
RTI	Rtrn Int													4Ø	6	1
RTS	Rtrn Sub													6Ø	6	1
SBC	A-M-C→A (1)	E9	2	2	ED	4	3	E5	3	2						
SEC	1→C													38	2	1
SED	1→D													F8	2	1
SEI	1→T													78	2	1
SMB[#(Ø-7)]	1→M_b (5)															
STA	A→M				8D	4	3	85	3	2						
STX	X→M				8E	4	3	86	3	2						
STY	Y→M				8C	4	3	84	3	2						
TAX	A→X													AA	2	1
TAY	A→Y													A8	2	1
TSX	S→X													BA	2	1
TXA	X→A													8A	2	1
TXS	X→S													9A	2	1
TYA	Y→A													98	2	1

MNEMONIC	(IND, X) OP	n	#	(IND), Y OP	n	#	Z PAGE, X OP	n	#	ABS, X OP	n	#	ABS, Y OP	n	#
ADC	61	6	2	71	5	2	75	4	2	7D	4	3	79	4	3
AND	21	6	2	31	5	2	35	4	2	3D	4	3	39	4	3
ASL							16	6	2	1E	7	3			
BBR[#(Ø-7)]															
BBS[#(Ø-7)]															
BCC															
BCS															
BEQ															
BIT															
BMI															
BNE															
BPL															
BRK															
BVC															
BVS															
CLC															
CLD															
CLI															
CLV															
CMP	C1	6	2	D1	5	2	D5	4	2	DD	4	3	D9	4	3
CPX															
CPY															
DEC							D6	6	2	DE	7	3			
DEX															
DEY															
EOR	41	6	2	51	5	2	55	4	2	5D	4	3	59	4	3
INC							F6	6	2	FE	7	3			
INX															
INY															
JMP															
JSR															
LDA	A1	6	2	B1	5	2	B5	4	2	BD	4	3	B9	4	3
LDX													BE	4	3
LDY							B4	4	2	BC	4	3			
LSR							56	6	2	5E	7	3			
NOP															
ORA	Ø1	6	2	11	5	2	15	4	2	1D	4	3	19	4	3
PHA															
PHP															
PLA															
PLP															
RMB[#(Ø-7)]															
RØL							36	6	2	3E	7	3			
RØR							76	6	2	7E	7	3			
RTI															
RTS															
SBC	E1	6	2	F1	5	2	F5	4	2	FD	4	3	F9	4	3
SEC															
SED															
SEI															
SMB[#(Ø-7)]															
STA	81	6	2	91	6	2	95	4	2	9D	5	3	[illegible]	5	3
STX															
STY							94	4	2						
TAX															
TAY															
TSX															
TXA															
TXS															
TYA															

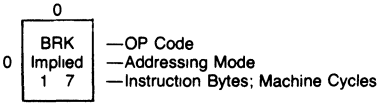
MNEMONIC	RELATIVE OP	n	#	INDIRECT OP	n	#	Z PAGE, Y OP	n	#	BIT ADDRESSING (OP BY BIT #) Ø	1	2	3	4	5	6	7	PROCESSOR STATUS CODES 7 6 5 4 3 2 1 Ø / N V · B D I Z C
ADC																		N V · · · · Z C
AND																		N · · · · · Z ·
ASL																		N · · · · · Z C
BBR[#(Ø-7)]										0F	1F	2F	3F	4F	5F	6F	7F	· · · · · · · ·
BBS[#(Ø-7)]										8F	9F	AF	BF	CF	DF	EF	FF	· · · · · · · ·
BCC	9Ø	2	2															· · · · · · · ·
BCS	BØ	2	2															· · · · · · · ·
BEQ	FØ	2	2															· · · · · · · ·
BIT																		M_7 M_6 · · · · Z ·
BMI	3Ø	2	2															· · · · · · · ·
BNE	DØ	2	2															· · · · · · · ·
BPL	1Ø	2	2															· · · · · · · ·
BRK																		· · · 1 · 1 · ·
BVC	5Ø	2	2															· · · · · · · ·
BVS	7Ø	2	2															· · · · · · · ·
CLC																		· · · · · · · Ø
CLD																		· · · · Ø · · ·
CLI																		· · · · · Ø · ·
CLV																		· Ø · · · · · ·
CMP																		N · · · · · Z C
CPX																		N · · · · · Z C
CPY																		N · · · · · Z C
DEC																		N · · · · · Z ·
DEX																		N · · · · · Z ·
DEY																		N · · · · · Z ·
EOR																		N · · · · · Z ·
INC																		N · · · · · Z ·
INX																		N · · · · · Z ·
INY																		N · · · · · Z ·
JMP				6C	5	3												· · · · · · · ·
JSR																		· · · · · · · ·
LDA																		N · · · · · Z ·
LDX							B6	4	2									N · · · · · Z ·
LDY																		N · · · · · Z ·
LSR																		Ø · · · · · Z C
NOP																		· · · · · · · ·
ORA																		N · · · · · Z ·
PHA																		· · · · · · · ·
PHP																		· · · · · · · ·
PLA																		N · · · · · Z ·
PLP																		(Restored)
RMB[#(Ø-7)]										Ø7	17	27	37	47	57	67	77	· · · · · · · ·
RØL																		N · · · · · Z C
RØR																		N · · · · · Z C
RTI																		(Restored)
RTS																		· · · · · · · ·
SBC																		N V · · · · Z (3)
SEC																		· · · · · · · 1
SED																		· · · · 1 · · ·
SEI																		· · · · · 1 · ·
SMB[#(Ø-7)]										87	97	A7	B7	C7	D7	E7	F7	· · · · · · · ·
STA																		· · · · · · · ·
STX							96	4	2									· · · · · · · ·
STY																		· · · · · · · ·
TAX																		N · · · · · Z ·
TAY																		N · · · · · Z ·
TSX																		N · · · · · Z ·
TXA																		N · · · · · Z ·
TXS																		· · · · · · · ·
TYA																		N · · · · · Z ·

NOTES
1 Add 1 to N if page boundary is crossed
2 Add 1 to N if branch occurs to same page
Add 2 to N if branch occurs to different page
3 Carry not = Borrow
4 If in decimal mode Z flag is invalid
accumulator must be checked on zero result
5 Effects 8-bit data field of the specified zero page address

LEGEND

X	=	Index X
Y	=	Index Y
A	=	Accumulator
M	=	Memory per effective address
M_s	=	Memory per stack pointer
M_b	=	Selecter zero page memory bit
M_7	=	Memory Bit 7
M_6	=	Memory Bit 6
+	=	Add
−	=	Subtract
∧	=	And
V	=	Or
⊻	=	Exclusive Or
m	=	Number of cycles
#	=	Number of Bytes

A.3 INSTRUCTION CODE MATRIX

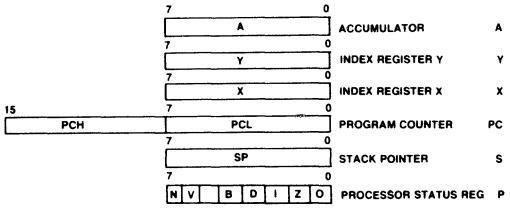


MSD \ LSD	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	MSD
0	BRK Implied 1 7	ORA (IND, X) 2 6				ORA ZP 2 3	ASL ZP 2 5	RMB0 ZP 2 5	PHP Implied 1 3	ORA IMM 2 2	ASL Accum 1 2			ORA ABS 3 4	ASL ABS 3 6	BBR0 ZP 3 5**	0
1	BPL Relative 2 2**	ORA (IND), Y 2 5*				ORA ZP, X 2 4	ASL ZP, X 2 6	RMB1 ZP 2 5	CLC Implied 1 2	ORA ABS, Y 3 4*				ORA ABS, X 3 4*	ASL ABS, X 3 7	BBR1 ZP 3 5**	1
2	JSR Absolute 3 6	AND (IND, X) 2 6			BIT ZP 2 3	AND ZP 2 3	ROL ZP 2 5	RMB2 ZP 2 5	PLP Implied 1 4	AND IMM 2 2	ROL Accum 1 2		BIT ABS 3 4	AND ABS 3 4	ROL ABS 3 6	BBR2 ZP 3 5**	2
3	BMI Relative 2 2**	AND (IND, Y) 2 5*				AND ZP, X 2 4	ROL ZP, X 2 6	RMB3 ZP 2 5	SEC Implied 1 2	AND ABS, Y 3 4*				AND ABS, X 3 4*	ROL ABS, X 3 7	BBR3 ZP 3 5**	3
4	RTI Implied 1 6	EOR (IND, X) 2 6				EOR ZP 2 3	LSR ZP 2 5	RMB4 ZP 2 5	PHA Implied 1 3	EOR IMM 2 2	LSR Accum 1 2		JMP ABS 3 3	EOR ABS 3 4	LSR ABS 3 6	BBR4 ZP 3 5**	4
5	BVC Relative 2 2**	EOR (IND), Y 2 5*				EOR ZP, X 2 4	LSR ZP, X 2 6	RMB5 ZP 2 5	CLI Implied 1 2	EOR ABS, Y 3 4*				EOR ABS, X 3 4*	LSR ABS, X 3 7	BBR5 ZP 3 5**	5
6	RTS Implied 1 6	ADC (IND, X) 2 6				ADC ZP 2 3	ROR ZP 2 5	RMB6 ZP 2 5	PLA Implied 1 4	ADC IMM 2 2	ROR Accum 1 2		JMP Indirect 3 5	ADC ABS 3 4	ROR ABS 3 6	BBR6 ZP 3 5**	6
7	BVS Relative 2 2**	ADC (IND, Y) 2 5*				ADC ZP, X 2 4	ROR ZP, X 2 6	RMB7 ZP 2 5	SEI Implied 1 2	ADC ABS, Y 3 4*				ADC ABS, X 3 4*	ROR ABS, X 3 7	BBR7 ZP 3 5**	7
8		STA (IND, X) 2 6			STY ZP 2 3	STA ZP 2 3	STX ZP 2 3	SMB0 ZP 2 5	DEY Implied 1 2		TXA Implied 1 2		STY ABS 3 4	STA ABS 3 4	STX ABS 3 4	BBS0 ZP 3 5**	8
9	BCC Relative 2 2**	STA (IND, Y) 2 6			STY ZP, X 2 4	STA ZP, X 2 4	STX ZP, Y 2 4	SMB1 ZP 2 5	TYA Implied 1 2	STA ABS, Y 3 5	TXS Implied 1 2			STA ABS, X 3 5		BBS1 ZP 3 5**	9
A	LDY IMM 2 2	LDA (IND, X) 2 6	LDX IMM 2 2		LDY ZP 2 3	LDA ZP 2 3	LDX ZP 2 3	SMB2 ZP 2 5	TAY Implied 1 2	LDA IMM 2 2	TAX Implied 1 2		LDY ABS 3 4	LDA ABS 3 4	LDX ABS 3 4	BBS2 ZP 3 5**	A
B	BCS Relative 2 2**	LDA (IND), Y 2 5*			LDY ZP, X 2 4	LDA ZP, X 2 4	LDX ZP, Y 2 4	SMB3 ZP 2 5	CLV Implied 1 2	LDA ABS, Y 3 4*	TSX Implied 1 2		LDY ABS, X 3 4*	LDA ABS, X 3 4*	LDX ABS, Y 3 4*	BBS3 ZP 3 5**	B
C	CPY IMM 2 2	CMP (IND, X) 2 6			CPY ZP 2 3	CMP ZP 2 3	DEC ZP 2 5	SMB4 ZP 2 5	INY Implied 1 2	CMP IMM 2 2	DEX Implied 1 2		CPY ABS 3 4	CMP ABS 3 4	DEC ABS 3 6	BBS4 ZP 3 5**	C
D	BNE Relative 2 2**	CMP (IND), Y 2 5*				CMP ZP, X 2 4	DEC ZP, X 2 6	SMB5 ZP 2 5	CLD Implied 1 2	CMP ABS, Y 3 4*				CMP ABS, X 3 4*	DEC ABS, X 3 7	BBS5 ZP 3 5**	D
E	CPX IMM 2 2	SBC (IND, X) 2 6			CPX ZP 2 3	SBC ZP 2 3	INC ZP 2 5	SMB6 ZP 2 5	INX Implied 1 2	SBC IMM 2 2	NOP Implied 1 2		CPX ABS 3 4	SBC ABS 3 4	INC ABS 3 6	BBS6 ZP 3 5**	E
F	BEQ Relative 2 2**	SBC (IND), Y 2 5*				SBC ZP, X 2 4	INC ZP, X 2 6	SMB7 ZP 2 5	SED Implied 1 2	SBC ABS, Y 3 4*				SBC ABS, X 3 4*	INC ABS, X 3 7	BBS7 ZP 3 5**	F
	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	

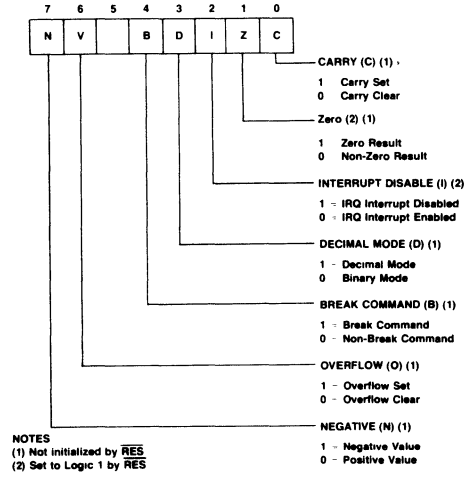
*Add 1 to N if page boundary is crossed.
**Add 1 to N if branch occurs to same page;
add 2 to N if branch occurs to different page.

APPENDIX B
KEY REGISTER SUMMARY

CPU Registers

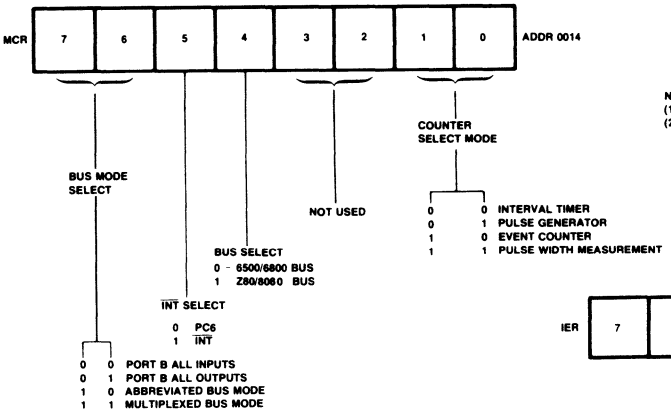


Processor Status Register

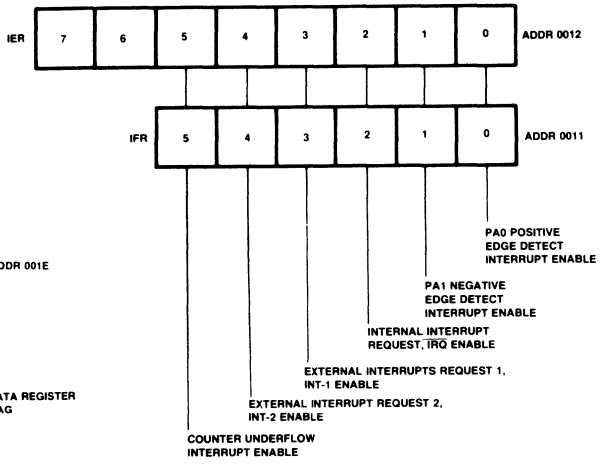


3

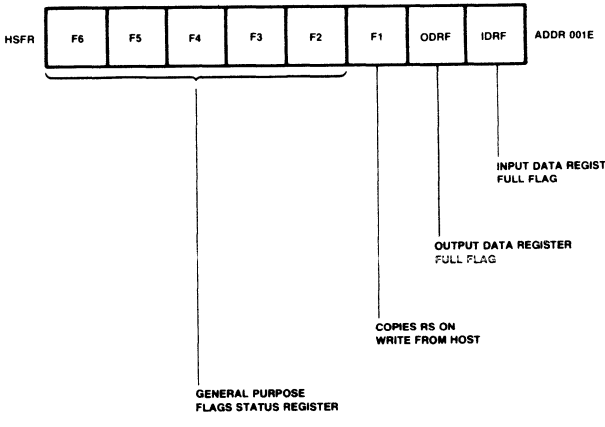
Mode Control Register



Interrupt Enable and Flag Registers



Host Status Flag Register

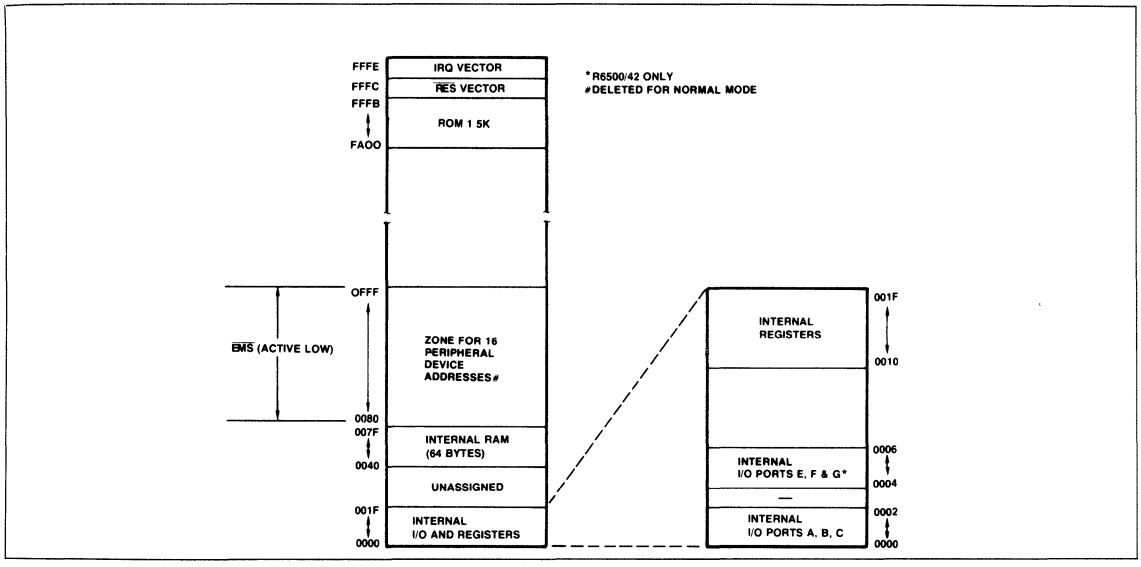


Host Addressing Matrix

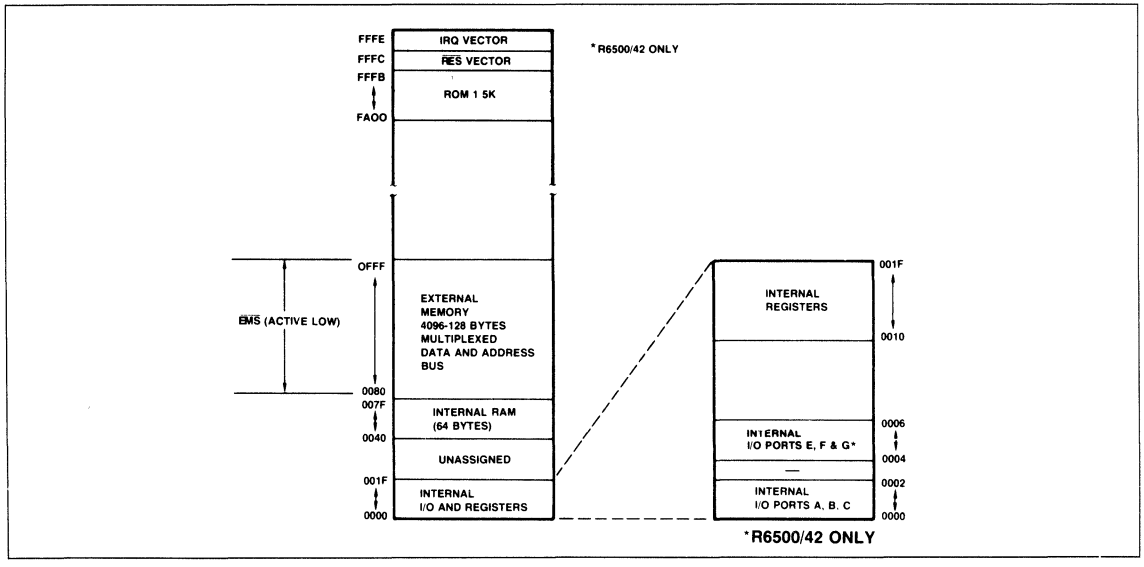
RS (A_0)	READ	WRITE
1	HOST STATUS FLAG	COMMAND INPUT
0	DATA REG OUTPUT	DATA REG INPUT

APPENDIX C
MEMORY MAPS AND ADDRESS AND PIN ASSIGNMENTS

C.1 ABBREVIATED BUS MODE MEMORY MAP



C.2 MULTIPLEXED BUS MODE MEMORY MAP



C.3 I/O AND INTERNAL REGISTER ADDRESSES

ADDRESS	READ	WRITE
001F	— —	— —
1E	Host Status Flag Register	Host Status Flag Register
1D	— —	— —
1C	Input Data Register (IDR)	Output Data Register (ODR)
1B	— —	— —
1A	Lower Counter	Lower Latch
19	Lower Counter & Clear Flag (IFR5)	Upper Latch/Transfer Latch to Counter & Clear Flag (IFR5)
18	Upper Counter	Upper Latch
17	— —	— —
16	— —	— —
15	— —	— —
14	Mode Control Register	Mode Control Register
13	— —	— —
12	Interrupt Enable Register	Interrupt Enable Register
11	Interrupt Flag Register	— —
10	Read "FF"	Clear Int Flag Bit
0F	— —	— —
0E	— —	— —
0D	— —	— —
0C	— —	— —
0B	— —	— —
0A	— —	— —
09	— —	— —
08	— —	— —
07	— —	— —
06	Port G (R6500/42 only)	Port G (R6500/42 only)
05	Port F (R6500/42 only)	Port F (R6500/42 only)
04	Port E (R6500/42 only)	Port E (R6500/42 only)
03	— —	— —
02	Port C	Port C
01	Port B	Port B
00	Port A	Port A

C.4 MULTIPLE FUNCTION PIN ASSIGNMENTS

PIN NUMBER R6500/41	PIN NUMBER R6500/42	I/O FUNCTION	ABBREVIATED PORT FUNCTION	MULTIPLEXED PORT FUNCTION
13	16	PC0	A0	A0
14	17	PC1	A1	A1
15	18	PC2	A2	A2
16	19	PC3	A3	A3
17	20	PC4	R/$\overline{W}$	R/$\overline{W}$
18	21	PC5	$\overline{EMS}$	$\overline{EMS}$
19	22	PC6/$\overline{INT}$	PC6/$\overline{INT}$	PC6/$\overline{INT}$
30	49	PB0	D0	A4/D0
31	50	PB1	D1	A5/D1
32	51	PB2	D2	A6/D2
33	52	PB3	D3	A7/D3
34	53	PB4	D4	A8/D4
35	54	PB5	D5	A9/D5
36	55	PB6	D6	A10/D6
37	56	PB7	D7	A11/D7

MAXIMUM RATINGS*

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to +7.0	Vdc
Input Voltage	V_{IN}	−0.3 to +7.0	Vdc
Operating Temperature Commercial	T_A	T_L to T_H 0 to +70	°C
Storage Temperature	T_{STG}	−55 to +150	°C

***NOTE:** Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the other sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

(V_{CC} = 5.0V ±5%, V_{SS} = 0V; T_A = 0° to 70°C, unless otherwise specified)

Parameter	Symbol	Min	Typ[1]	Max	Unit	Test Conditions
Input High Voltage	V_{IH}	+2.0	—	V_{CC}	V	
Input Low Voltage	V_{IL}	−0.3	—	+0.8	V	
Input Leakage Current $\overline{RES}$, $\overline{NMI}$	I_{IN}	—	—	±10.0	μA	V_{IN} = 0 to 5.0V
Input Low Current	I_{IL}	—	−1.0	−1.6	mA	V_{IL} = 0.4V
Output High Voltage	V_{OH}	+2.4	—	V_{CC}	V	I_{LOAD} = −100 μA V_{CC} = 4.75V
Output High Voltage (CMOS)	V_{CMOS}	V_{CC}−30%	—	V_{CC}	V	V_{CC} = 4.75V
Output Low Voltage	V_{OL}	—	—	+0.4	V	I_{LOAD} = 1.6 mA V_{CC} = 4.75V
I/O Port Pull-Up Resistance PA0–PA7, PC0–PC7, PF0–PF7[3], PG0–PG7[3]	R_L	3.0	6.0	11.5	Kohm	
Output High Current (Sourcing)	I_{OH}	−100	—	—	μA	V_{OH} = 2.4V
Output Low Current (Sinking, PE[3])	I_{OL}	1.6	—	—	mA	V_{OL} = 0.4V
Darlington Current Drive (PE[3])	I_{OH}	−1.0	—	—	mA	V_{OH} = 1.5V
Input Capacitance PA, PB, PC, PF[3], PG[3]	C_{IN}	—	—	10	pF	T_A = 25°C V_{IN} = 0V f = 1.0 MHz
Output Capacitance (Three-State Off)	C_{OUT}	—	—	10	pF	T_A = 25°C V_{IN} = 0V f = 1.0 MHz
Power Dissipation (Outputs High)	P_D	—	550	1050	mW	T_A = 25°C

Notes:
1. Typical values measured at T_A = 25°C and V_{CC} = 5.0V.
2. Negative sign indicates outward current flow, positive indicates inward flow.
3. R6500/42 only.

APPENDIX E
TIMING REQUIREMENTS AND CHARACTERISTICS

E.1 GENERAL NOTES

1 V_{CC} 5V ± 5%, 0 C ≤ TA ≤ 70 C

2 A valid V_{CC} — RES sequence is required before proper operation is achieved

3 All timing reference levels are 0 8V and 2 0V, unless otherwise specified

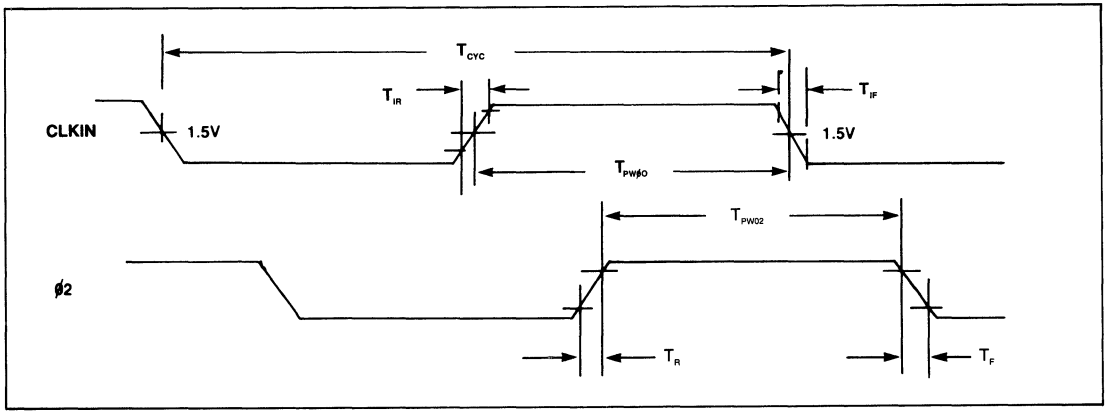
4 All time units are nanoseconds, unless otherwise specified

5 All capacitive loading is 130pf maximum, except as noted below

PA, PB	—	50pf maximum
PB, PC (I/O Modes Only)	—	50pf maximum
PB, PC (ABB and Mux Mode)	—	130pf maximum

E.2 CLOCK TIMING

SYMBOL	PARAMETER	1 MHz		2 MHz	
		MIN	MAX	MIN	MAX
T_{CYC}	Cycle Time	1000	10 μs	500	10 μs
$T_{PW\phi O}$	CLKIN Input Clock Pulse Width	475	—	240	—
T_{PW02}	Output Clock Pulse Width at Minimum T_{CYC}	$T_{PW\phi O}$	$T_{PW\phi O}$ +25	$T_{PW\phi O}$	$T_{PW\phi O}$ +20
T_R, T_F	Output Clock Rise, Fall Time	—	25	—	15
T_{IR} T_{IF}	Input Clock Rise Fall Time	—	10	—	10



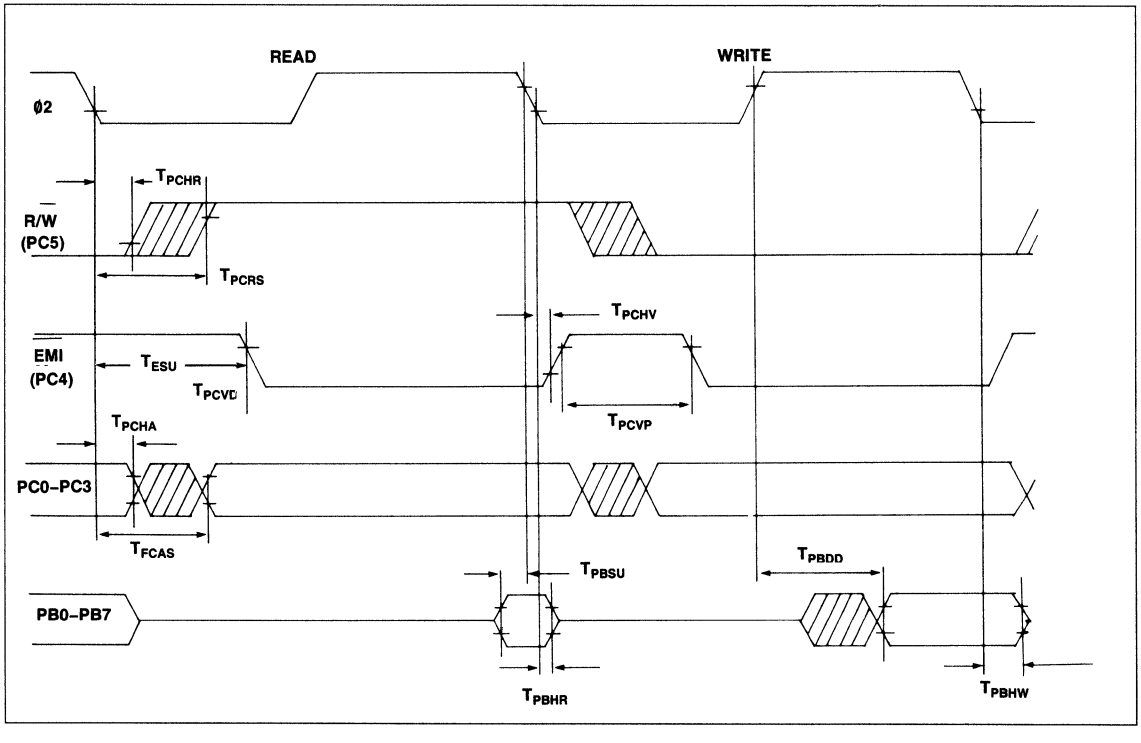
E.3 ABBREVIATED MODE TIMING—PB AND PC

(MCR 5 = 1, MCR 6 = 0, MCR 7 = 1)

SYMBOL	PARAMETER	1 MHz		2 MHz	
		MIN	MAX	MIN	MAX
T_{PCRS}	(PC5) R/W Setup Time	—	225	—	140
T_{PCAS}	(PC0-PC3) Address Setup Time	—	225	—	140
T_{PBSU}	(PB) Data Setup Time	50	—	35	—
T_{PBHR}	(PB) Data Read Hold Time	10	—	10	—
T_{PBHW}	(PB) Data Write Hold Time	30	—	30	—
T_{PBDD}	(PB) Data Output Delay	—	175	—	150
T_{PCHA}	(PC0-PC3) Address Hold Time	30	—	30	—
T_{PCHR}	(PC5) R/W Hold Time	30	—	30	—
T_{PCHV}	(PC4) $\overline{EMS}$ Hold Time	10	—	10	—
T_{PCVP}	(PC4) $\overline{EMS}$ Stabilization Time	30	—	30	—
T_{ESV}	$\overline{EMS}$ Setup Time	—	350	—	210

NOTE 1. Values assume PC0-PC5 have the same capacitive load

E.3.1 Abbreviated Mode Timing Diagram



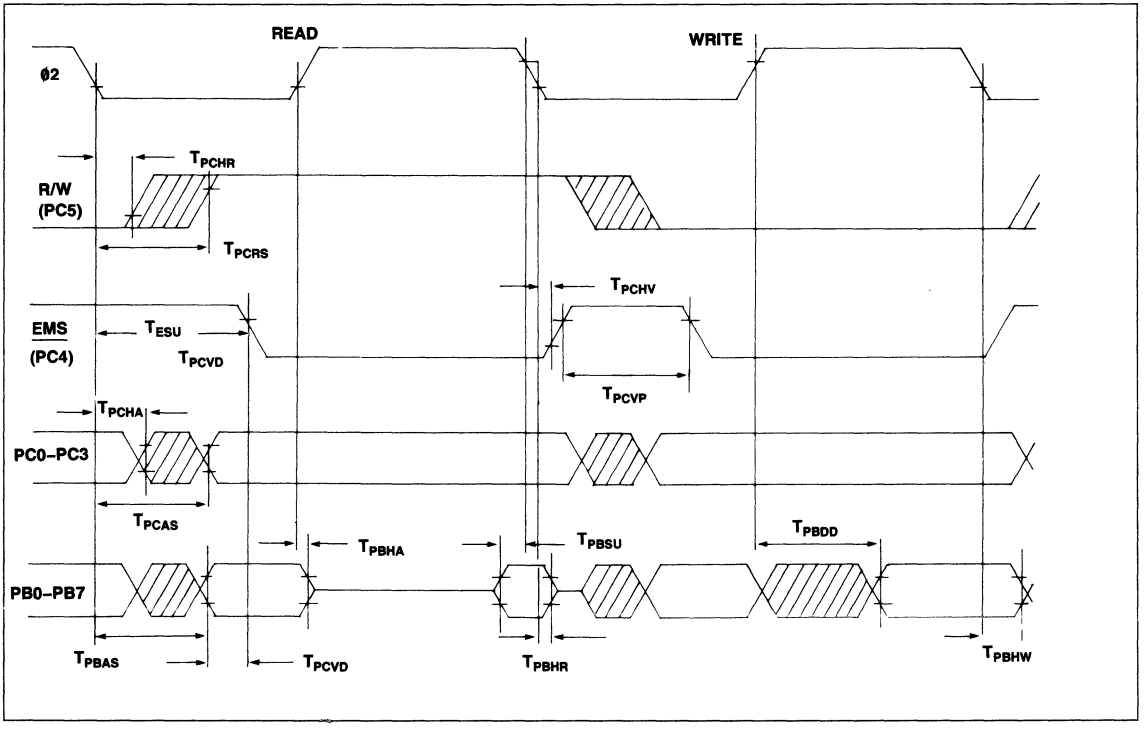
E.4 MULTIPLEXED MODE TIMING—PB AND PC

(MCR 5 = 1, MCR 6 = 1, MCR 7 = 1)

SYMBOL	PARAMETER	1 MHz		2 MHz	
		MIN	MAX	MIN	MAX
T_{PCRS}	(PC5) R/W Setup Time	—	225	—	140
T_{PCAS}	(PC0-PC3) Address Setup Time	—	225	—	140
T_{PBAS}	(PB) Address Setup Time	—	225	—	140
T_{PBSU}	(PB) Data Setup Time	50	—	35	—
T_{PBHR}	(PB) Data Read Hold Time	10	—	10	—
T_{PBHW}	(PB) Data Write Hold Time	30	—	30	—
T_{PBDD}	(PB) Data Output Delay	—	175	—	150
T_{PCHA}	(PC0-PC3) Address Hold Time	30	—	30	—
T_{PBHA}	(PB) Address Hold Time	0	100	0	80
T_{PCHR}	(PC5) R/W Hold Time	30	—	30	—
T_{PCHV}	(PC4) $\overline{EMS}$ Hold Time	10	—	10	—
T_{PCVD}[1]	(PC4) Address to $\overline{EMS}$ Delay Time	30	—	30	—
T_{PCVP}	(PC4) $\overline{EMS}$ Stabilization Time	30	—	30	—
T_{ESU}	$\overline{EMS}$ Setup Time	—	350	—	210

NOTE 1: Values assume PC0-PC5 have the same capacitive load.

E.4.1 Multiplex Mode Timing Diagram

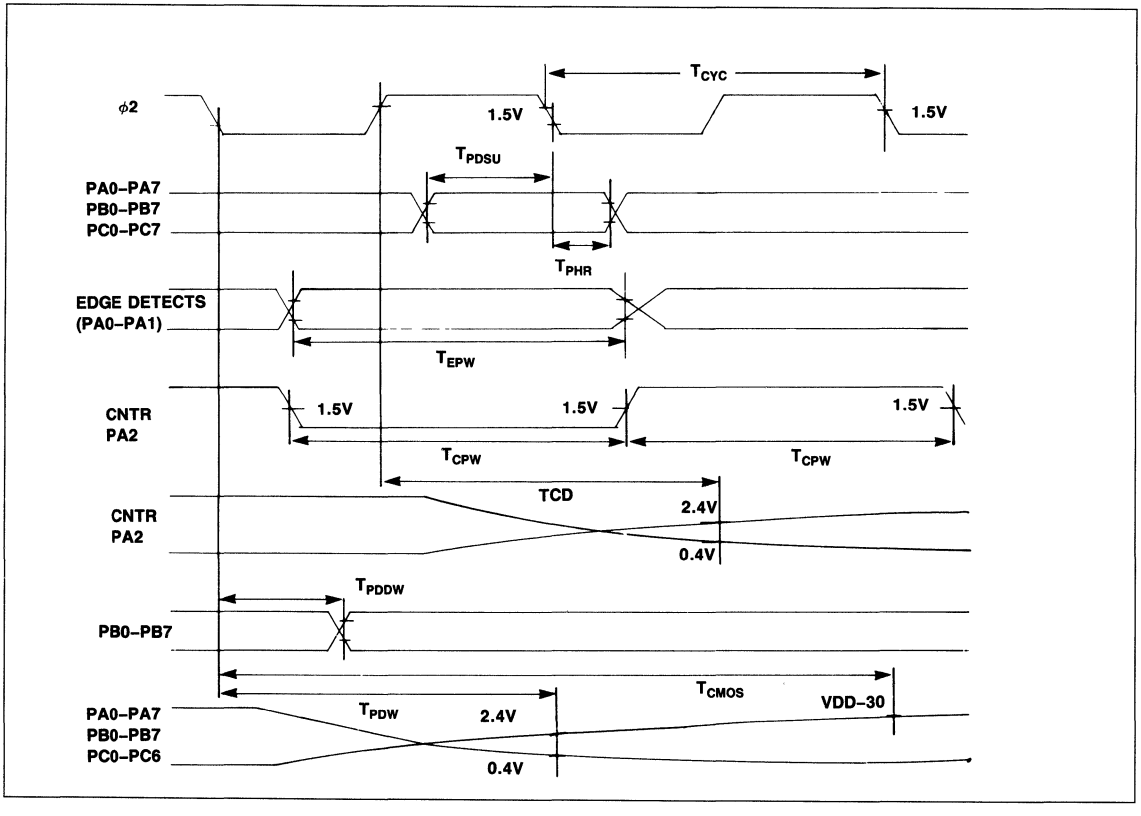


E.5 I/O, EDGE DETECT AND COUNTER TIMING

SYMBOL	PARAMETER	1 MHz		2 MHz	
		MIN	MAX	MIN	MAX
	Internal Write to Peripheral Data Valid				
T_{PDW}[1]	PA, PC TTL	—	500	—	500
T_{CMOS}[1]	PA, PC CMOS	—	1000	—	1000
T_{PDDW}	PB	—	175	—	150
	Peripheral Data Setup Time				
T_{PDSU}	PA, PC	200	—	200	—
T_{PDSU}	PB	50	—	50	—
	Peripheral Data Hold Time				
T_{PHR}	PA, PC	75	—	75	—
T_{PHR}	PB	10	—	10	—
T_{EPW}	PA0-PA1 Edge Detect Pulse Width	T_{CYC}	—	T_{CYC}	—
	Counter				
T_{CPW}	PA2 Input Pulse Width	T_{CYC}	—	T_{CYC}	—
T_{CD}[1]	PA2 Output Delay	—	500	—	500

NOTE 1 Maximum Load Capacitance 50pF Passive Pull-Up Required

E.5.1 I/O, Edge Detect, Counter



Rockwell

R65/41EB AND R65/41EAB BACKPACK EMULATORS

INTRODUCTION

The Rockwell R65/41EB and R65/41EAB Backpack Emulator is the PROM prototyping version of the 8-bit, masked-ROM R6500/41 one-chip microcomputer. Like the R6500/41, the backpack device is totally upward/downward compatible with all members of the R6500/41 family. It is designed to accept standard 5-volt, 24-pin EPROMs or ROMs directly, in a socket on top of the Emulator. This packaging concept allows a standard EPROM to be easily removed, re-programmed, then reinserted as often as desired.

The backpack devices have the same pinouts as the masked-ROM R6500/41 microcomputer. These 40 pins are functionally and operationally identical to the pins on the R6500/41. The R6500/41 Microcomputer Product Description (Rockwell Document No. 29651N38, Order No. 2135) includes a description of the interface signals and their functions. Whereas the masked-ROM R6500/41 provides 1.5K bytes of read-only memory, the R65/41EB will address 4.0K bytes of external program memory. This extra memory accommodates program patches, test programs or optional programs during breadboard and prototype development states.

ORDERING INFORMATION

Backpack Emulator

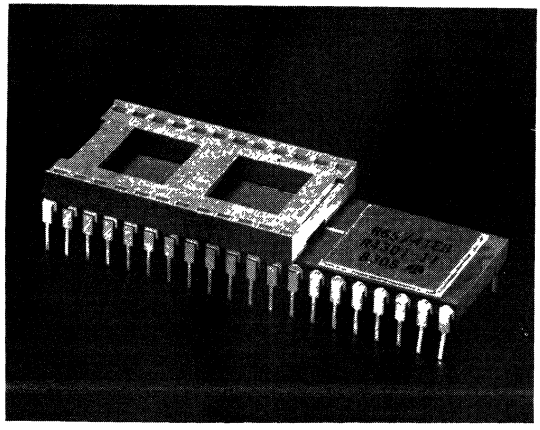
Part Number	Memory Capacity	Compatible Memories	Temperature Range and Speed
R65/41EB	4K × 8	2732	0°C to 70°C 1MHz
R65/41EAB	4K × 8	2732A	0°C to 70°C 2 MHz

Support Products

Part Number	Description
S65-101	SYSTEM 65 Microcomputer Development System
M65-040	PROM Programmer Module
M65-131	1-MHz R6500/41 Personality Module
M65-132	2-MHz R6500/41 Personality Module
RDC-1001	Rockwell Development Center
RDC-131	1 MHz R6500/41 Personality Set (RDC)
RDC-132	2 MHz R6500/41 Personality Set (RDC)

FEATURES

- PROM version of the R6500/41
- All Host bus features of R6500/41
- Completely pin compatible with R6500/41 single-chip microcomputers
- Profile approaches 40-pin DIP of R6500/41
- Accepts 5 volt, 24-pin industry-standard EPROMs —4K memories—2732, 2732A
- Use as prototyping tool or for low volume production
- 4K bytes of memory capacity
- 64 × 8 static RAM
- Software compatibility with the R6500 family
- 23 bi-directional TTL compatible I/O lines
- 16 bit programmable counter/latch with four modes (interval timer, pulse generator, event counter, pulse width measurement)
- 7 interrupts (reset, two external edge sensitive, counter underflow, Host data received, Output data register full, Input data register empty).
- External time base
- Single +5V power supply



R65/41EB-R65/41EAB Backpack Emulator

CONFIGURATIONS

The Backpack Emulator is available in two different versions, to accommodate 1 MHz and 2 MHz speeds. Both versions provide 192 bytes of RAM and I/O, as well as 24 signals to support the external memory "backpack" socket.

External 4K memories with addresses of 000 to FFF, are upward translated to addresses F000 to FFFF when assembled to form the Backpack Emulator.

EXTERNAL FREQUENCY REFERENCE

The external frequency reference is an output timing signal ø2. This is an internally synchronized 1 x clock output suitable for external memory or peripheral interfacing.

I/O PORT PULLUPS

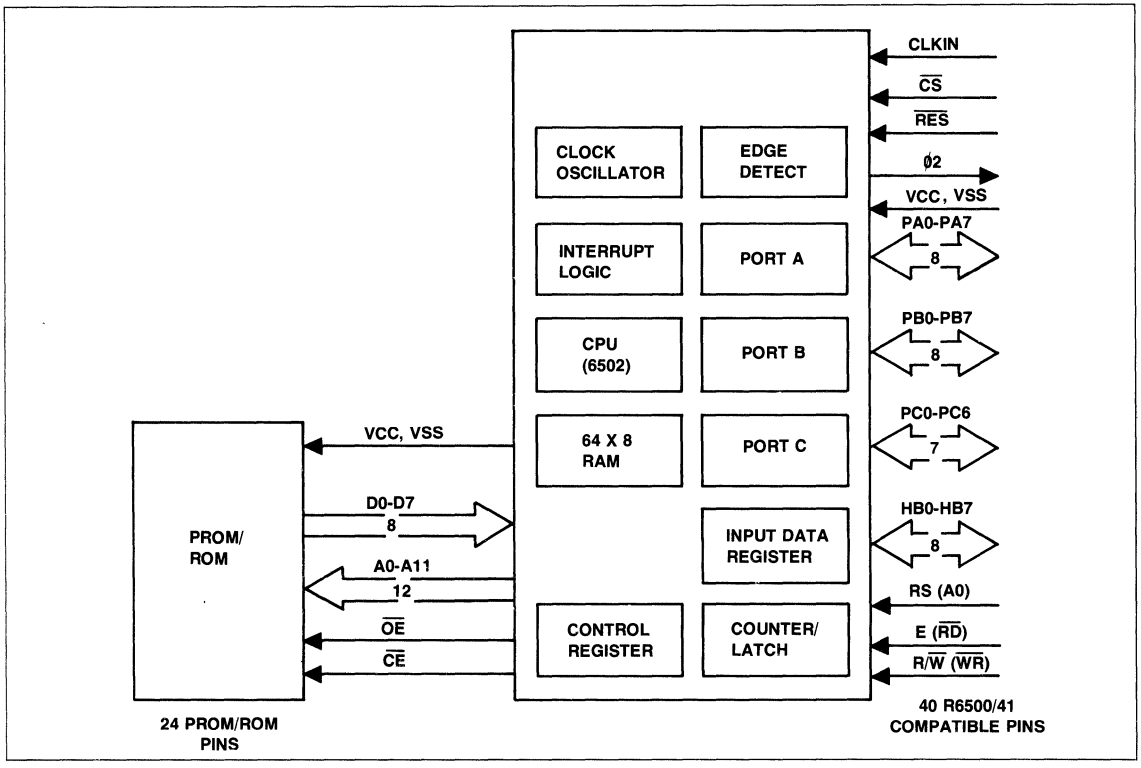
The emulator devices have internal I/O port pullup resistors on ports A and C. Port B has tri-state drivers.

PRODUCT SUPPORT

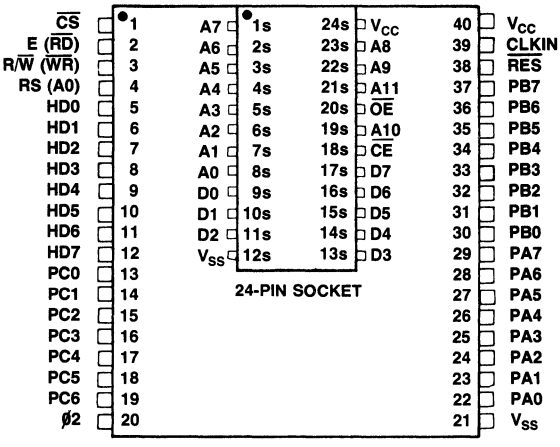
The Backpack Emulator is just one of the products that Rockwell offers to facilitate system and program development for the R6500/41.

The SYSTEM 65 Microcomputer Development System with R6500/41 Personality Module supports both hardware and software development. Complete in-circuit user emulation with the R6500/41 Personality Module allows total system test and evaluation. With the optional PROM Programmer, SYSTEM 65 can also be used to program EPROMs for the development activity. When PROM programs have been finalized, the PROM device can be sent to Rockwell for masking into the 1.5K ROM of the R6500/41.

In addition to support products, Rockwell offers regularly-scheduled designer courses at regional centers.



R65/41EB Interface Diagram



Pin Configuration

(1) PIN 21 is V_{CC} for R65/41EB or A11 for R65/41EB

BACKPACK MEMORY SIGNAL DESCRIPTION

Signal Name	Pin No.	Description
D0–D7	9S–11S, 13S–17S	Data Bus Lines. All instruction and data transfers take place on the data bus lines. The buffers driving the data bus lines have full three-state capability. Each data bus pin is connected to an input and an output buffer, with the output buffer remaining in the floating condition.
A0–A9 A10, A11	1S–8S, 22S, 23S 19S, 21S	Address Bus Lines. The address bus lines are buffered by push/pull type drivers that can drive one standard TTL load.
$\overline{CE}$	18S	Chip Enable.
$\overline{OE}$	20S	Memory Enable Line. This signal provides the output enable for the memory to place information on the data bus lines. This signal is driven by the R/$\overline{W}$ signal from the CPU and then inverted to form $\overline{OE}$. This signal is driven by the inverted address line A11. The $\overline{OE}$ signal will be low for addresses greater than 0FFF
V_{CC}	24S	Main Power Supply +5V. This pin is tied directly to pin 40 (V_{CC}).
V_{SS}	12S	Signal and Power Ground (zero volts). This pin is tied directly to pin 21 (V_{SS}).

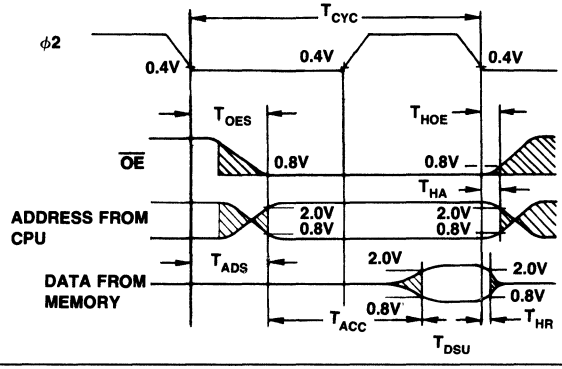
I/O AND INTERNAL REGISTER ADDRESSES

Address	Read	Write
001F	— —	— —
1E	Host Status Flag Register	Host Status Flag Register
1D	— —	— —
1C	Input Data Register (IDR)	Output Data Register (ODR)
1B	— —	— —
1A	Lower Counter	Lower Latch
19	Lower Counter & Clear Flag (IFR5)	Upper Latch/Transfer Latch to Counter & Clear Flag (IFR5)
18	Upper Counter	Upper Latch
17	— —	— —
16	— —	— —
15	— —	— —
14	Mode Control Register	Mode Control Register
13	— —	— —
12	Interrupt Enable Register	Interrupt Enable Register
11	Interrupt Flag Register	— —
10	Read "FF"	Clear Int Flag Bit
03 thru 0F	— —	— —
02	Port C	Port C
01	Port B	Port B
0000	Port A	Port A

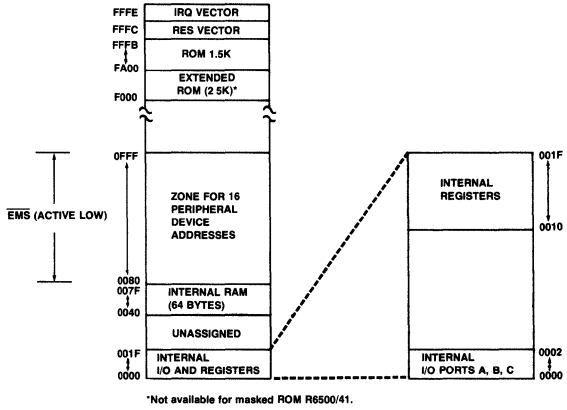
READ TIMING CHARACTERISTICS

Signal	Symbol	1 MHz		2 MHz		Unit
		Min.	Max.	Min.	Max.	
$\overline{OE}$ and $\overline{CE}$ setup time from CPU	T_{OES}	—	225	—	140	ns
Address setup time from CPU	T_{ADS}	—	225	—	140	ns
Memory read access time	T_{ACC}	—	700	—	315	ns
Data set up time	T_{DSU}	50	—	35	—	ns
Data hold time—Read	T_{HR}	10	—	10	—	ns
Address hold time	T_{HA}	30	—	30	—	ns
$\overline{OE}$ and $\overline{CE}$ hold time	T_{HOE}	30	—	30	—	ns
Cycle Time	T_{CYC}	1 0	10.0	0.5	10.0	μs

READ TIMING WAVEFORMS

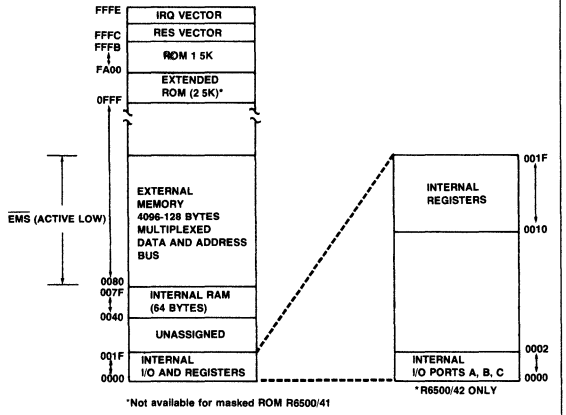


ABBREVIATED BUS MODE MEMORY MAP



*Not available for masked ROM R6500/41.

MULTIPLEXED BUS MODE MEMORY MAP



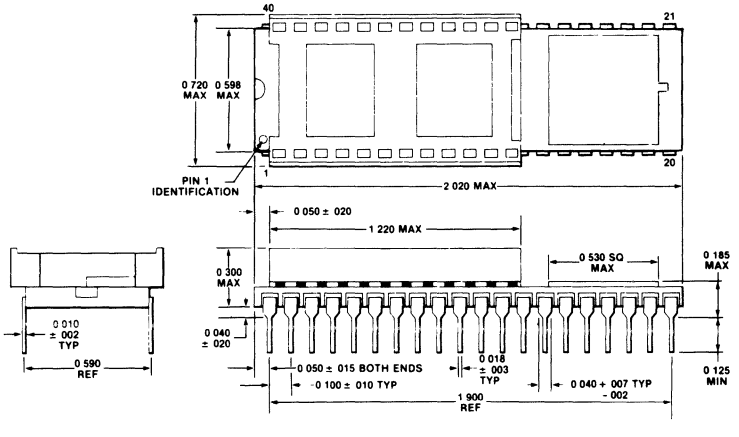
*Not available for masked ROM R6500/41

*R6500/42 ONLY

ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0 ± 5%, V_{SS} = 0, T_A = 25°C)

Characteristic	Symbol	Min	Typ	Max	Unit
Input High Threshold Voltage D0-D7	V_{IHT}	V_{SS} + 2.0	—	—	Vdc
Input Low Threshold Voltage D0-D7	V_{ILT}	—	—	V_{SS} + 0.8	Vdc
Three-State (Off State) Input Current (V = 0.4 to 2.4V, V_{CC} = 5.25V) D0-D7	I_{TSI}	—	—	± 10	μA
Output High Voltage (I_{LOAD} = 100μ Adc, V_{CC} = 4.75V) D0-D7, A0-A11, $\overline{OE}$, $\overline{CE}$	V_{OH}	V_{SS} + 2.4	—	—	Vdc
Output Low Voltage (I_{LOAD} = 1.6 mAdc, V_{CC} = 4.75V) D0-D7, A0-A11, $\overline{OE}$, $\overline{CE}$	V_{OL}	—	—	V_{SS} + 0.4	Vdc
Power Dissipation (less EPROM)	P_D	—	0.50	—	W
Capacitance (V_{in} = 0, T_A = 25°C, f = 1 MHz) D0-D7 (High Impedance State) Input Capacitance	C C_{out} C_{in}	— —	— —	10 10	pF
I/O Port Pull-up Resistance	R_L	3.0	6.0	11.5	kohm



40-Pin Backpack Package

Rockwell

R6541Q AND R6500/43 INTELLIGENT PERIPHERAL CONTROLLERS

SECTION 1 INTRODUCTION

1.1 FEATURES

- Directly compatible with 6500, 6800, 8080, and Z80 bus families
- Asynchronous Host interface that allows independent clock operation
- Input, Output and Status Registers for CPU/Host data transfer
- Status register for CPU/Host data transfer operations
- Interrupt or polled data interchange with Host
- Enhanced 6502 CPU
  - Four new bit manipulation instructions
    - Set Memory Bit (SMB)
    - Reset Memory Bit (RMB)
    - Branch on Bit Set (BBS)
    - Branch on Bit Reset (BBR)
  - Decimal and binary arithmetic modes
  - 13 addressing modes
  - True indexing
- 256-byte mask-programmable ROM*
- 64-byte static RAM
- 23 TTL-compatible I/O lines
- A 16-bit programmable counter/timer, with latch
  - Pulse width measurement
  - Pulse generation
  - Interval timer
  - Event counter
- Eight interrupts
  - Two edge-sensitive lines; one positive, one negative
  - Reset
  - Counter Underflow
  - Host data received
  - Output Data Register full
  - Input Data Register empty
  - Non-maskable
- Multiplexed bus expandable to 4K bytes of external memory

*R6541Q has no ROM.

- Unmultiplexed Address and Data buses for 4K of Peripheral I/O expansion
- 68% of the instructions are executed in less than 2μs @ 2 MHz
- NMOS-3 silicon gate, depletion load technology
- Single +5V power supply
- 64-pin QUIP

NOTE

This document describes both the R6541Q and R6500/43. In the text, the terms IPC or device will be used when describing both parts. See Section 1.3 for a description of the options available for the R6500/43 and the fixed features of the R6541Q.

1.2 SUMMARY

The Rockwell R6541Q and R6500/43 One-Chip Intelligent Peripheral Controllers (IPC) are general purpose, programmable interface I/O devices designed for use with a variety of 8-bit and 16-bit microprocessor systems. They have an enhanced R6502 CPU, an optional 256 by 8-bit ROM, 64 by 8-bit RAM, three I/O ports with multiplexed special functions, a multi-function timer, and a full 4K address and data buses all contained within a 64-pin Quad-in-line package.

In both versions, special interface registers allow these IPC devices to function as peripheral controllers for the 6500, 6800, Z80, 8080, and other 8-bit or 16-bit host microcomputer systems.

The innovative architecture and the demonstrated high performance of the R6502 CPU, as well as instruction simplicity, results in system cost-effectiveness and a wide range of computational power. These features make the device a leading candidate for IPC computer applications.

Rockwell supports development of the R6541Q and R6500/43 with the System 65 Microcomputer Development System and the R6500/* Family of Personality Modules. Complete in-circuit emulation with the R6500/* Family of Personality Modules allows total system test and evaluation.

This product description assumes that the reader is familiar with the R6502 CPU hardware and programming capabilities. A detailed description of the R6502 CPU hardware is included in the R6500 Microcomputer System Hardware Manual (Document Order Number 201). A descrption of the instruction capabilities of the R6502 CPU is contained in the R6500 Microcomputer System Programming Manual (Document Order Number 202).

1.3 CUSTOMER OPTIONS

The R6500/43 microcomputer is available with the following customer specified mask options.

- Option 1 with or without a 256 byte ROM
- Option 2 Reset Vector at FFFC or 0FFC
- Option 3 Port A with or without internal pull-up resistors
- Option 4 Port C with or without internal pull-up resistors

All options should be specified on an R6500/43 order form.

The R6541Q has no customer specified mask options. It has the following characteristics.

- Without ROM
- Reset Vector at FFFC
- No internal pull-up resistors on any Port (PA or PC)

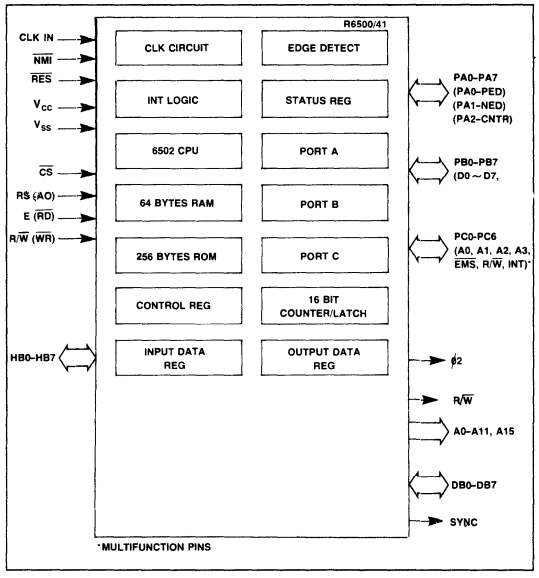


Figure 2-1. Interface Diagram

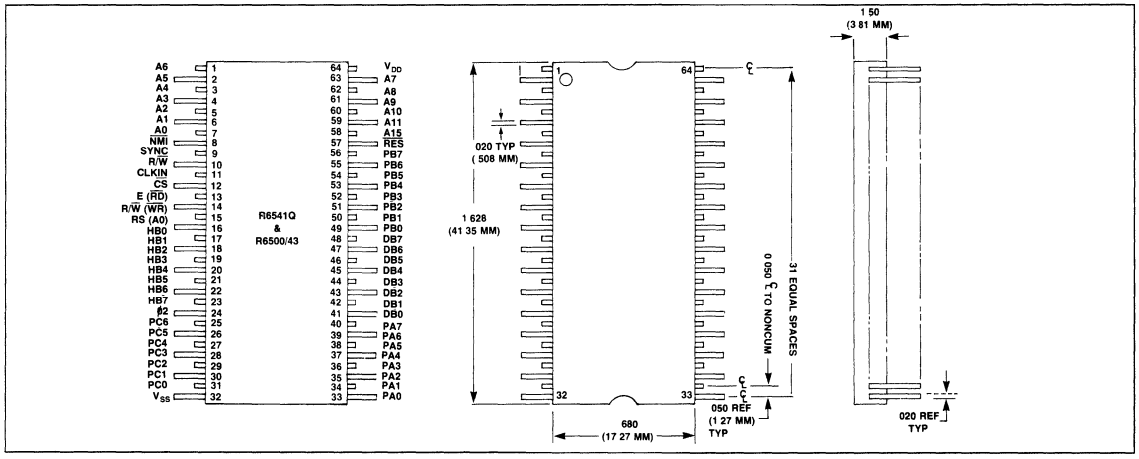


Figure 2-2. R6541Q & R6500/43 Pin Out Designation (64 PIN QUIP)

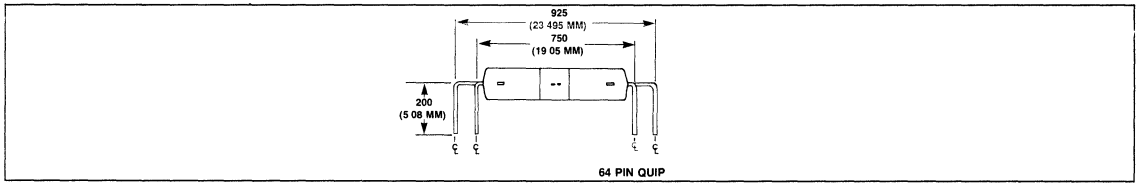


Figure 2-3. R6541Q & R6500/43 Dimensional Outline

SECTION 2
INTERFACE REQUIREMENTS

This section describes the interface requirements for the Intelligent Peripheral Controller. Figure 2-1 is the Interface Diagram for the devices. Figure 2-2 shows the pin out configuration and Table 2-1 describes the function of each pin of the devices. Figure 2-3 shows the mechanical dimensions of the devices. Section 5 describes the Host computer interface protocol and timing requirements.

Table 2-1. Pin Description

SIGNAL NAME	PIN NO. R6541Q & R6500/43	DESCRIPTION
CLKIN	11	Symmetrical square wave 100 KHz to 2 MHZ, TTL compatible input.
$\phi 2$	24	Output timing signal—This is an internally synchronized 1 × clock output suitable for external memory or peripheral interfacing.
$\overline{RES}$	57	The reset input is used to initialize the device. Section 7 describes the process and conditions of the $\overline{RES}$ procedure.
VCC	64	Power supply input (+5V)
VSS	32	Signal and power ground (OV).
$\overline{CS}$	12	Chip select pin for host interface.
RS (A0)	15	Register select input pin used by the Host processor to indicate that information being written into the IPC is a data or command byte or to indicate that information being read from the IPC is a status or data byte.
E ($\overline{RD}$)	13	Host timing control signal for data register write and read.
R/$\overline{W}$ ($\overline{WR}$)	14	Host timing control signal for data register write and read.
HB0-HB7	16-23	Data bus between Host and IPC data input and output registers.
$\overline{NMI}$	8	A negative going edge on the Non-Maskable Interrupt signal requests that a non-maskable interrupt be generated with the CPU.
PA0-PA7	33-40	8 bit I/O port used for either input or output. Each line consists of an active transistor to V_{SS} and an optional passive pull-up to V_{CC}. The two lower bits PA0 and PA1 also serve as edge detect inputs. PA2 is time shared with the 16 bit Counter Input or output pin, CNTR, and is mode selected.
PB0-PB7	49-56	8 bit I/O port used for either input or output. Each line consists of an active transistor to V_{SS} and an active pull-up to V_{CC}. This port becomes a tri-state data bus, D0-D7, in the Abbreviated or Multiplexed Bus Mode. D0-D7 are multiplexed with address lines A4-A11 in the Multiplexed Bus Mode.
PC0-PC6	31-25	7 bit I/O port used for either input or output. Each line consists of an active transistor to V_{SS} and an optional passive pull-up to V_{CC}. The pins PC0 to PC5 are multiplexed with address and control signals for use in abbreviated and multiplex modes. PC6 is multiplexed with $\overline{INT}$ and is program selectable. In these two modes PC0-PC5 have active pull-ups.
A0-A11, A15	7-1 63-58	Thirteen address lines used to address a complete 8K external address space.
DB0-DB7	41-48	Eight bidirectional data bus lines used to transmit data to and from external memory.
SYNC	9	SYNC is a positive going signal for the full clock cycle whenever the CPU is performing an OP CODE fetch.
R/$\overline{W}$	10	Controls the direction of data transfer between the CPU and the external 65K address space. The signal is high when reading and low when writing.

SECTION 3
SYSTEM ARCHITECTURE

This section provides a functional description of the IPC device. Functionally, the device consists of a CPU, RAM and optional ROM memories, three parallel I/O ports (actually 23 I/O lines), counter/latch circuit, a mode control register, and an interrupt flag/enable dual register circuit. A block diagram of the system is shown in Figure 3-1.

NOTE

Throughout this document, unless specified otherwise, all memory or register address locations are specified in hexadecimal notation.

3.1 CPU LOGIC

The internal CPU of the device is an enhanced R6502 configuration with an 8-bit Accumulator register, two 8-bit Index Registers (X and Y), an 8-bit Stack Pointer register, an ALU, a 16-bit Program Counter, and standard instruction register/decode and internal timing control logic.

3.1.1 Accumulator

The accumulator is a general purpose 8-bit register that stores the results of most arithmetic and logic operations. In addition, the accumulator usually contains one of the two data words used in these operations.

3.1.2 Index Registers

There are two 8-bit index registers, X and Y. Each index register can be used as a base to modify the address data program counter and thus obtain a new address—the sum of the program counter contents and the index register contents.

When executing an instruction which specifies indirect addressing, the CPU fetches the op code and the address, and modifies the address from memory by adding the index register to it prior to loading or storing the value of memory.

Indexing greatly simplifies many types of programs, especially those using data tables.

3.1.3 Stack Pointer

The Stack Pointer is an 8-bit register. It is automatically incremented and decremented under control of the microprocessor to perform stack manipulation in response to either user instructions, or an internal $\overline{IRQ}$ interrupt. The Stack Pointer must be initialized by the user program.

The stack allows simple implementation of multiple level interrupts, subroutine nesting and simplification of many types of data manipulation. The JSR, BRK, RTI and RTS instructions use the stack and Stack Pointer.

The stack can be envisioned as a deck of cards which may only be accessed from the top. The address of a memory location is stored (or "pushed") onto the stack. Each time data are to be pushed onto the stack, the Stack Pointer is placed on the Address Bus, data are written into the memory location addressed by the Stack Pointer, and the Stack Pointer is decremented by 1. Each time data are read (or "pulled") from the stack, the Stack Pointer is incremented by 1. The Stack Pointer is then placed on the Address Bus, and data are read from the memory location addressed by the Pointer.

The stack is located on zero page, i.e., memory locations 007F-0040. Normal usage calls for the initialization of the Stack Pointer at 007F

3.1.4 Arithmetic and Logic Unit (ALU)

All arithmetic and logic operations take place in the ALU, including incrementing and decrementing internal registers (except the Program Counter) The ALU cannot store data for more than one cycle If data are placed on the inputs to the ALU at the beginning of a cycle, the result is always gated into one of the storage registers or to external memory during the next cycle.

Each bit of the ALU has two inputs. These inputs can be tied to various internal buses or to a logic zero; the ALU then generates the function (AND, OR, SUM, and so on) using the data on the two inputs

3.1.5 Program Counter

The 16-bit Program Counter provides the addresses that are used to step the processor through sequential instructions in a program. Each time the processor fetches an instruction from program memory, the lower (least significant) byte of the Program Counter (PCL) is placed on the low-order bits of the Address Bus and the higher (most significant) byte of the Program Counter (PCH) is placed on the high-order 8 bits of the Address Bus. The Counter is incremented each time an instruction or data is fetched from program memory.

3.1.6 Instruction Register and Instruction Decode

Instructions are fetched from ROM or RAM and gated onto the Internal Data Bus. These instructions are latched into the Instruction Register then decoded along with timing and interrupt signals to generate control signals for the various registers.

3.1.7 Timing Control

The Timing Control Logic keeps track of the specific instruction cycle being executed. This logic is initialized each time an instruction fetch is executed and is advanced at the beginning of each low level of the Clock In pulse for as many cycles as are required to complete the instruction. Each data transfer which takes place between the registers is caused by decoding the contents of both the instruction register and timing control unit.

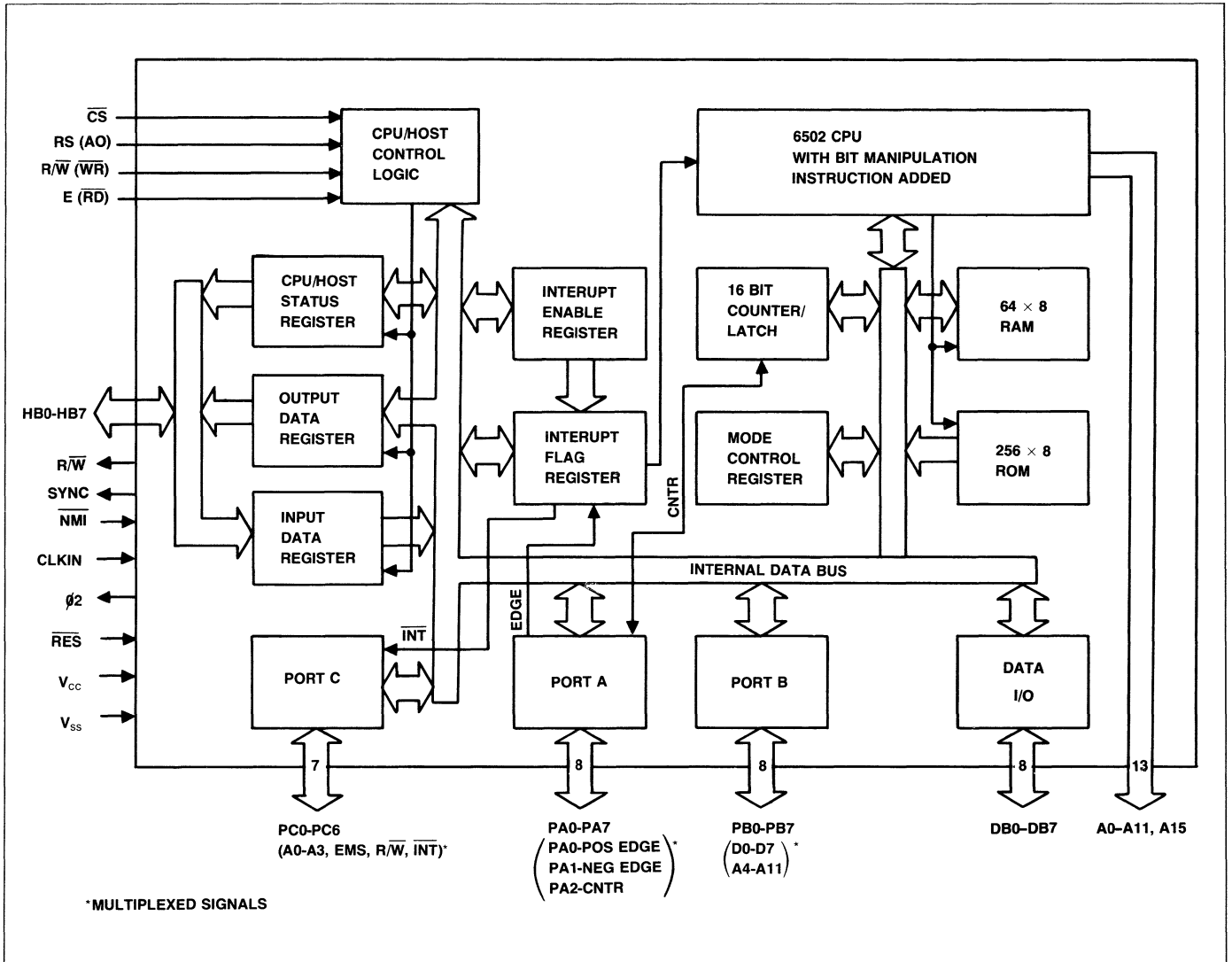


Figure 3-1. R6541Q & R6500/43 Block Diagram

3.1.8 Interrupt Logic

Interrupt logic controls the sequencing of three interrupts: $\overline{RES}$, $\overline{NMI}$, and $\overline{IRQ}$. $\overline{IRQ}$ is generated by any one of four conditions: Counter Overflow, Positive Edge Detect, Negative Edge Detect, and Input Data Register Full.

3.2 NEW INSTRUCTIONS

In addition to the standard 6502 instruction set, four instructions have been added to the devices to simplify operations that previously required a read/modify/write operation. In order for these instructions to be equally applicable to any I/O ports, with or without mixed input and output functions, the I/O ports have been designed to read the contents of the specified port data register during the Read cycle of the read/modify/write operation, rather than I/O pins as in normal read cycles. The added instructions and their format are explained in the following subparagraphs. Refer to Appendix A for the Op Code mnemonic addressing matrix for these added instructions.

3.2.1 Set Memory Bit (SMB m, Addr.)

This instruction sets to "1" one of the 8-bit data field specified by the zero page address (memory or I/O port). The first byte of the instruction specifies the SMB operation and 1 of 8 bits to be set. The second byte of the instruction designates address (00-FF) of the byte or I/O port to be operated upon.

3.2.2 Reset Memory Bit (RMB m, Addr.)

This instruction is the same operation and format as SMB instruction except a reset to "0" of the bit results.

3.2.3 Branch on Bit Set Relative (BBS m, Addr, DEST)

This instruction tests one of 8 bits designated by a three bit immediate field within the first byte of the instruction. The second byte is used to designate the address of the byte to be tested within the zero page address range (memory or I/O ports). The third byte of the instruction is used to specify the 8 bit relative address to which the instruction branches if the bit tested is a "1". If the bit tested is not set, the next sequential instruction is executed.

3.2.4 Branch On Bit Reset Relative (BBR m, Addr, DEST)

This instruction is the same operation and format as the BBS instruction except that a branch takes place if the bit tested is a "0".

3.3 READ-ONLY-MEMORY (ROM)

The optional ROM consists of 256 bytes mask programmable memory with an address space from OFOO to OFFF. ROM locations FFFA through FFFF are assigned for interrupt vectors. The Reset vector can be optionally at OFFC or FFFC.

The R6541Q has no ROM and its reset vector is at FFFC.

3.4 RANDOM ACCESS MEMORY (RAM)

The RAM consists of 64 bytes of read/write memory with an assigned page zero address of 0040 through 007F.

3.5 SYSTEM CLOCK

The device functions with an external clock. It is fully asynchronous in reference to the Host computer timing. The device clock frequency equals the external clock frequency. It is also made available for any external device synchronization at pin Ø2.

3.6 MODE CONTROL REGISTER (MCR)

The Mode Control Register contains control bits for the multifunction I/O ports and mode select bits for the Counter, the 6500 or 8080 Bus Select, and the Interrupt ($\overline{INT}$). Its setting determines the basic configuration of the device in any application. Initializing this register is one of the first actions of any software program. The Mode Control Register bit assignment is shown in Figure 3-2.

The use of Counter A Mode Select is shown in Section 6

The use of the 6500/8080 Host Bus Select is shown in Section 6

The use of Interrupt Select is shown in Section 4.5.

The use of Bus Mode Select is shown in Sections 4 4 and 4.5.

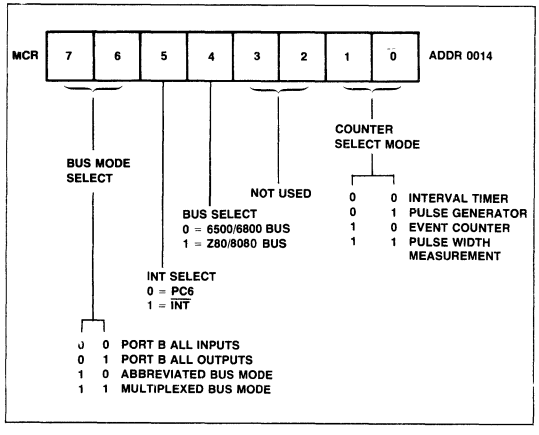


Figure 3-2. Mode Control Register Bit Allocations

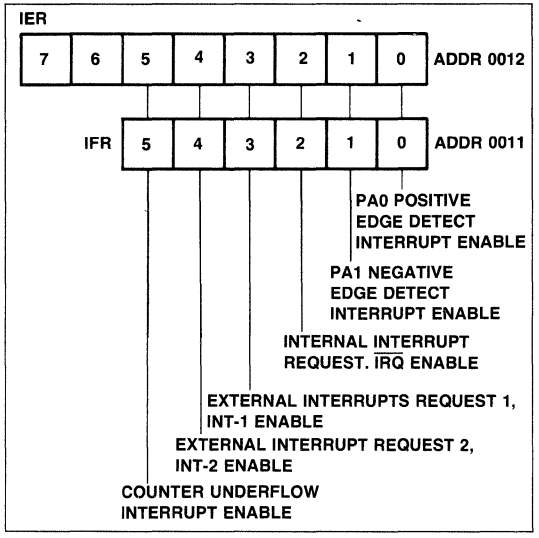


Figure 3-3. Interrupt Enable and Flat Registers

Table 3-1. Interrupt Enable Signals

Control Signal	Description
IER 0	Positive Edge Detect, Interrupt Enable—when this bit is true, a positive going signal on PA0 will generate an $\overline{IRQ}$ and set the corresponding flag bit.
IER 1	Negative Edge Detect Interrupt Enable—when this bit is set to a "1" a negative going signal on PA1 will generate an $\overline{IRQ}$ and set the corresponding flag bit.
IER 2	Input Data Register Full Interrupt Enable—setting this bit to a "1" allows an $\overline{IRQ}$ to be generated each time the Host fills the IDR setting the IDFR bit.
IER 3	Output Data Register Full Interrupt Enable—when this bit is an interrupt request to the Host is generated each time the ODRF flag is set to a "1". (See External Interrupts, Paragraph 3.7.1) Reading the ODR clears INT-1 and ODRF flags.
IER 4	Input Data Register Empty Interrupt Enable—when this is set to a "1" an interrupt is generated to the Host each time the IDR is read by the CPU. The interrupt occurs when the IDRF flag is cleared. INT-2 is cleared when the Host reads the status flag register. (See External Interrupts, Paragraph 3.7.1).
IER 5	Counter Interrupt Enable—if enabled, an $\overline{IRQ}$ is generated whenever the Counter overflows.

3.7 INTERRUPT FLAG REGISTER (IFR) AND INTERRUPT ENABLE REGISTER (IER)

An $\overline{IRQ}$ interrupt request can be initiated by any or all of four possible sources. These sources are all capable of being enabled or disabled by the use of the appropriate interrupt enabled bits in the Interrupt Enable Register (IER). Multiple simultaneous interrupts will cause the $\overline{IRQ}$ interrupt request to remain active until all interrupting conditions have been serviced and cleared.

The Interrupt Flag Register contains the information that indicates which I/O or counter needs attention. The contents of the Interrupt Flag Register may be examined at any time by reading at address: 0011. Edge detect IFR bits may be cleared by executing a RMB instruction at address location 0010. The RMB X, (0010) instruction reads FF, modifies bit X to a "0", and writes the modified value at address location 0011. In this way IFR bits set to a "1" after the read cycle of a Read-Modify-Write instruction (such as RMB) are protected from being cleared. IFR bits 6 and 7 are indeterminate on a Read.

Each IFR bit has a corresponding bit in the Interrupt Enable Register which can be set to a "1" by writing a "1" in the respective bit position at location 0012. Individual IER bits may be cleared by writing a "0" in the respective bit position, or by $\overline{RES}$. If set to a "1", an $\overline{IRQ}$ will be generated when the corresponding IFR bit becomes true. The Interrupt Flag Register and Interrupt Enable Register bit assignments are shown in Figure 3-3 and the functions of each bit are explained in Table 3-1.

3.7.1 External Interrupts ($\overline{INT}$)

An external interrupt $\overline{INT}$ to the Host computer may be selected in two modes. (See Section 5 for information on the Host/Device interface).

OUTPUT DATA REGISTER (ODR) FULL

When IER 3 of the Interrupt Enable Register is set to a "1", the device will assert the $\overline{INT}$ (PC6) line each time it loads the ODR. The ODRF flag of the Status Flag Register and the IFR 3 of the IFR will be set to a "1" indicating the ODR is full. The ODRF and IFR 3 flags are cleared and $\overline{INT}$ is negated when the Host processor reads the ODR.

INPUT DATA REGISTER (IDR) EMPTY

When IER 4 of the Interrupt Enable Register is set to a "1", the device will assert the $\overline{INT}$ (PC6) line each time it reads the IDR. The IDRF flag of the Host Status Flag Register will be cleared and the IFR 4 flag of the IFR will be set to a "1" indicating the IDR has just been read by the device. The IFR 4 flag is cleared and $\overline{INT}$ is negated when the Host processor reads the Host Status Flag Register. $\overline{RES}$ clears the IDR and sets the IFR4 flag to indicate the register is empty.

3.8 PROCESSOR STATUS REGISTER

The 8-bit Processor Status Register, shown in Figure 3-4, contains seven status flags. Some of these flags are controlled by the user program; others may be controlled both by the user's program and the CPU. The R6502 instruction set contains a number of conditional branch instructions which are designed to allow testing of these flags. Each of the eight processor status flags is described in the following sections.

3.8.1 Carry Bit (C)

The Carry Bit (C) can be considered as the ninth bit of an arithmetic operation. It is set to logic 1 if a carry from the eighth bit has occurred or cleared to logic 0 if no carry occurred as the result of arithmetic operations.

The Carry Bit may be set or cleared under program control by use of the Set Carry (SEC) or Clear Carry (CLC) instruction, respectively. Other operations which affect the Carry Bit are ADC, ASL, CMP, CPX, CPY, LSR, PLP, ROL, ROR, RTI, and SBC.

3.8.2 Zero Bit (Z)

The Zero Bit (Z) is set to logic 1 by the CPU during any data movement or calculation which sets all 8 bits of the result to zero. This bit is cleared to logic 0 when the resultant 8 bits of a data movement or calculation operation are not all zero. The R6502 instruction set contains no instruction to specifically set or clear the Zero Bit. The Zero Bit is, however, affected by the following instructions; ADC, AND, ASL, BIT, CMP, CPX, CPY, DEC, DEX, DEY, EOR, INC, INX, INY, LDA, LDX, LDY, LSR, ORA, PLA, PLP, ROL, ROR, RTI, SBC, TAX, TAY, TXA, TSX, and TYA.

3.8.3 Interrupt Disable Bit (I)

The Interrupt Disable Bit (I) is used to control the servicing of an interrupt request (IRQ). If the I Bit is reset to logic 0, the $\overline{IRQ}$ signal will be serviced. If the bit is set to logic 1, the $\overline{IRQ}$ signal will be ignored. The CPU will set the Interrupt Disable Bit to logic 1 if a RESET ($\overline{RES}$) or Non-Maskable Interrupt ($\overline{NMI}$) signal is detected.

The I bit is cleared by the Clear Interrupt Mask Instruction (CLI) and is set by the Set Interrupt Mask Instruction (SEI). This bit may also be set by the BRK Instruction. The Return from Interrupt (RTI) and Pull Processor Status (PLP) instructions will also affect the I bit.

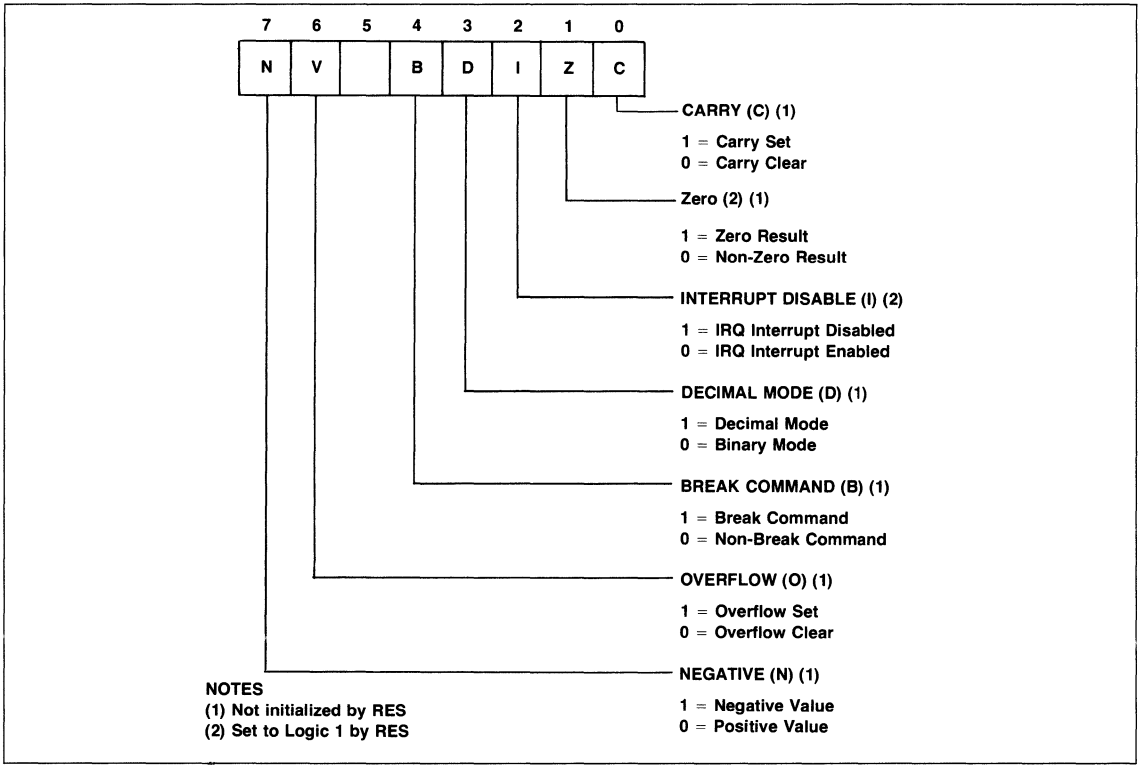


Figure 3-4. Processor Status Register

3.8.4 Decimal Mode Bit (D)

The Decimal Mode Bit (D), is used to control the arithmetic mode of the CPU. When this bit is set to logic 1, the adder operates as a decimal adder. When this bit is cleared to logic 0, the adder operates as a straight binary adder. The adder mode is controlled only by the programmer. The Set Decimal Mode (SED) instruction will set the D bit; the Clear Decimal Mode (CLD) instruction will clear it. The PLP and RTI instructions also effect the Decimal Mode Bit.

CAUTION

The Decimal Mode Bit will either set or clear in an unpredictable manner upon power application to the device. This bit must be initialized to the desired state by the user program or erroneous results may occur.

3.8.5 Break Bit (B)

The Break Bit (B) is used to determine the condition which caused the $\overline{IRQ}$ service routine to be entered. If the $\overline{IRQ}$ service routine was entered because the CPU executed a BRK command, the Break Bit will be set to logic 1. If the $\overline{IRQ}$ routine was entered as the result of an $\overline{IRQ}$ signal being generated, the B bit will be cleared to logic 0. There are no instructions which can set or clear this bit.

3.8.6 Overflow Bit (V)

The Overflow Bit (V) is used to indicate that the result of a signed, binary addition, or subtraction, operation is a value that cannot be contained in seven bits ($-128 \leq n \leq 127$). This indicator only has meaning when signed arithmetic (sign and seven magnitude bits) is performed. When the ADC or SBC instruction is performed, the Overflow Bit is set to logic 1 if the polarity of the sign bit (bit 7) is changed because the result exceeds +127 or −128; otherwise the bit is cleared to logic 0. The V bit may also be cleared by the programmer using a Clear Overflow (CLV) instruction.

The Overflow Bit may also be used with the BIT instruction. The BIT instruction which may be used to sample interface devices, allows the overflow flag to reflect the condition of bit 6 in the sampled field. During a BIT instruction the Overflow Bit is set equal to the content of the bit 6 on the data tested with BIT instrction. When used in this mode, the overflow has nothing to do with signed arithmetic, but is just another sense bit for the microprocessor. Instructions which affect the V flag are ADC, BIT, CLV, PLP, RTI and SBC.

3.8.7 Negative Bit (N)

The Negative Bit (N) is used to indicate that the sign bit (bit 7), in the resulting value of a data movement or data arithmetic operation, is set to logic 1. If the sign bit is set to logic 1, the resulting value of the data movement or arithmetic operation is negative; if the sign bit is cleared, the result of the data movement or arithmetic operation is positive. There are no instructions that set or clear the Negative Bit since the Negative Bit represents only the status of a result. The instructions that effect the state of the Negative Bit are: ADC, AND, ASL, BIT, CMP, CPX, CPY, DEC, DEX, DEY, EOR, INC, INX, INY, LDA, LDX, LDY, LSR, ORA, PLA, PLP, ROL, ROR, RTI, SBC, TAX, TAY, TSX, TXA, and TYA.

SECTION 4
PARALLEL INPUT/OUTPUT PORTS

INPUT/OUTPUT PORTS

The IPC device provides three ports (PA, PB, and PC). The 15 lines of PA and PC are completely bidirectional, that is, there is no line grouping or port association restrictions. The eight lines of Port B may be programmed as all inputs or all outputs. Port PC, however, may be multiplexed under program control with seven other signals. Six of these signals form an address and control bus for extended addressing. The seventh signal is multiplexed with an external interrupt output, $\overline{INT}$. All eight Port B lines are tri-state to permit their use as a data bus during extended addressing modes.

Internal pull-up resistors (FET's with an impedance range of $3K \leq Rpu \leq 12K$ ohm) may be provided on ports PA and/or PC. The R6541Q does not have these resistors.

The direction of the I/O lines are controlled by 8-bit port registers located in page zero. This arrangement provides quick programming access using simple two-byte zero page address instructions. There are no direction registers associated with the I/O ports, which simplifies I/O handling. The I/O addresses are shown in Table 4-1. If a part is being used to emulate a R6500/42 the ports must be provided in external circuitry and addressed through locations 0004-0006.

Table 4-1. I/O Port Addresses

PORT		ADDRESS
A		0000
B		0001
C		0002
E	R6500/42 only	0004
F	R6500/42 only	0005
G	R6500/42 only	0006

4.1 INPUTS

Inputs for Ports A and C, and also Ports F and G if emulating the R6500/42, are enabled by loading logic 1 into all I/O port register bit positions that are to correspond to I/O input lines. A low (<0.8V) input signal will cause a logic 0 to be read when a read instruction is issued to the port register. A high (>2.0V) input will cause a logic 1 to be read. An $\overline{RES}$ signal forces all I/O port registers to logic 1 thus initially treating all I/O lines as inputs.

Port B may be all inputs or all outputs. All inputs is selected by setting bits MCR6 and MCR7 of the Mode Control Register to a "0".

The status of the input lines can be interrogated at any time by reading the I/O port addresses. Note that this will return the actual status of the input lines, not the data written into the I/O port registers.

Read/Modify/Write instructions can be used to modify the operation of PA, PB, PC, and also PF, & PG of an emulated R6500/42. During the Read cycle of a Read/Modify/Write instruction the Port I/O register is read. For all other read instructions the port input lines are read. Read/Modify/Write instructions are: ASL, BBS, BBR, DEC, INC, LSR, RMB, ROL, ROR, and SMB.

4.2 OUTPUTS

Outputs for Ports A thru C, and emulated Ports E thru G of the R6500/42, are controlled by writing the desired I/O line output states into the corresponding I/O port register bit positions. A logic 1 will force a high (>2.4V) output while a logic 0 will force a low (<0.4V) output. Port B also requires that MCR6 be set to a "1" and MCR7 be set to a "0".

4.3 PORT A (PA)

Port A can be programmed via the Mode Control Register (MCR) as a standard parallel 8-bit, bit independent, I/O port, or a counter I/O line. Table 4-2 tabulates the control and usage of Port A.

In addition to their normal I/O functions, PA0 can detect positive going edges, and PA1 can detect negative going edges. An edge transition on these pins will set a corresponding status bit in the IFR and generate an interrupt request if the respective Interrupt Enable Bit is set. The maximum rate at which an edge can be detected is one-half the Ø2 clock rate. Edge detection timing is shown in Section E.5.

Table 4-2. Port A Control & Usage

PA0-PA1 I/O		PA2 I/O		PA2 COUNTER				PA3-PA7 I/O	
		MCR0 = 0 MCR1 = 0		MCR0 = 1 MCR1 = 0		MCR0 = X MCR1 = 1			
SIGNAL		SIGNAL		SIGNAL		SIGNAL		SIGNAL	
NAME	TYPE	NAME	TYPE	NAME	TYPE	NAME	TYPE	NAME	TYPE
PA0 (1) PA1(2)	I/O I/O	PA2	I/O	CNTR	OUTPUT	CNTR	INPUT (3)	PA3-PA7	I/O

(1) POSITIVE EDGE DETECT (2) NEGATIVE EDGE DETECT (3) HARDWARE BUFFER FLOAT

4.4 PORT B (PB)

Port B can be programmed as an I/O Port, an 8-bit tri-state data bus, or as a multiplexed bus. Mode selection for Port B is made by the Mode Control Register (MCR). The Port B output drivers can be selected as tri-state output drivers by setting bit 7 of the MCR to 0 (zero) and bit 6 of the MCR to 1. An all inputs condition is created by setting both MCR6 and MCR7 to 0 (zero). Table 4-3 shows the necessary settings for the MCR to achieve the various modes for Port B. When Port B is selected to operate in the Abbreviated Mode PB0-PB7 serves as data register bits D0-D7. When Port B is selected to operate in the Multiplexed Mode data bits D0 through D7 are time multiplexed with address bits A4 through A11, respectively. Refer to the Memory Maps (Appendix B) for Abbreviated and Multiplexed memory assignments. See Appendix E.3 through E.5 for Port B timing.

4.5 PORT C (PC)

Port C can be programmed as an I/O port and in conjunction with Port B, as an abbreviated bus, or as a multiplexed bus. When used in the abbreviated or multiplexed bus modes, PC0-PC5 function as A0-A3, R/W, and $\overline{EMS}$, respectively, as shown in Table 4-4. $\overline{EMS}$ (External Memory Select) is asserted (low) whenever the internal processor accesses memory area between 0080 and 0FFF. (See Memory Map, Appendix C). The leading edge of $\overline{EMS}$ may be used to strobe the eight address lines multiplexed on Port B in the Multiplexed Bus Mode. See Appendix E.3 through E.5 for Port C timing.

Table 4-3. Port B Control & Usage

R6541Q & R6500/43	I/O MODES				ABBREVIATED MODE		MULTIPLEXED MODE			
	MCR7 = 0 MCR6 = 0		MCR7 = 0 MCR6 = 1		MCR7 = 1 MCR6 = 0		MCR7 = 1 MCR6 = 1			
	SIGNAL		SIGNAL		SIGNAL		PHASE 1		PHASE 2	
							SIGNAL		SIGNAL	
PIN #	NAME	TYPE (1)	NAME	TYPE (2)	NAME	TYPE (3)	NAME	TYPE (2)	NAME	TYPE (3)
49	PB0	INPUT	PB0	OUTPUT	D0	I/O	A4	OUTPUT	D0	I/O
50	PB1	INPUT	PB1	OUTPUT	D1	I/O	A5	OUTPUT	D1	I/O
51	PB2	INPUT	PB2	OUTPUT	D2	I/O	A6	OUTPUT	D2	I/O
52	PB3	INPUT	PB3	OUTPUT	D3	I/O	A7	OUTPUT	D3	I/O
53	PB4	INPUT	PB4	OUTPUT	D4	I/O	A8	OUTPUT	D4	I/O
54	PB5	INPUT	PB5	OUTPUT	D5	I/O	A9	OUTPUT	D5	I/O
55	PB6	INPUT	PB6	OUTPUT	D6	I/O	A10	OUTPUT	D6	I/O
56	PB7	INPUT	PB7	OUTPUT	D7	I/O	A11	OUTPUT	D7	I/O

(1) TRI-STATE BUFFER IS IN HIGH IMPEDANCE MODE (2) TRI-STATE BUFFER IS IN ACTIVE MODE
(3) TRI-STATE BUFFER IS IN ACTIVE MODE ONLY DURING THE PHASE 2 PORTION OF A WRITE CYCLE

Table 4-4. Port C Control & Usage

R6541Q & R6500/43	I/O MODE		ABBREVIATED MODE		MULTIPLEXED MODE	
	MCR7 = 0 MCR6 = X		MCR7 = 1 MCR6 = 0		MCR7 = 1 MCR6 = 1	
	SIGNAL		SIGNAL		SIGNAL	
PIN #	NAME	TYPE (1)	NAME	TYPE (2)	NAME	TYPE (2)
31	PC0	I/O	A0	OUTPUT	A0	OUTPUT
30	PC1	I/O	A1	OUTPUT	A1	OUTPUT
29	PC2	I/O	A2	OUTPUT	A2	OUTPUT
28	PC3	I/O	A3	OUTPUT	A3	OUTPUT
27	PC4	I/O	$\overline{EMS}$	OUTPUT	$\overline{EMS}$	OUTPUT
26	PC5	I/O	R/$\overline{W}$	OUTPUT	R/$\overline{W}$	OUTPUT
25	PC6*	I/O	$\overline{INT}$*	OUTPUT	$\overline{INT}$*	OUTPUT

(1) RESISTIVE PULL-UP, ACTIVE BUFFER PULL-DOWN
(2) ACTIVE BUFFER PULL-UP AND PULL-DOWN

*PC6 if MCR5 = 0; $\overline{INT}$ if MCR5 = 1

4.7 BUS MODES

A special attribute of Port B and Port C is their capability to be configured via the Mode Control Register (see Section 3.6) into four different modes

In the Port B All Inputs and Port B All Outputs modes the separate address and data bus are used. The difference lies in the direction of Port B—all inputs or all outputs. The receiving ports perform the normal I/O function. A15 is usually used as a chip select for external memory.

In the Abbreviated Bus Mode, the address and data lines can be used as above to emulate the R6500/41. Port B and Port C are automatically transformed into an abbreviated address bus and control signals (Port C) and a bidirectional data bus (Port B). 16 Peripheral addresses can be selected. In general usage, these 16 addresses would be distributed to several external I/O devices such as R6522 and R6520, etc., each of which may contain more than one unique address.

In the Multiplexed Bus Mode, the operation is similar to the Abbreviated Mode except that a full 4K of external addresses are provided. Port C provides the lower addresses and control signals. Port B multiplexes functions. During the first half of the cycle it contains the remaining necessary 8 address bits for 4K; during the second half of the cycle it contains a bidirectional data bus The address bits appearing on Port B must be latched into an external holding register. The leading edge of $\overline{EMS}$, which indicates that the bus function is active, may be used for this purpose.

Figures 4-1a thru 4-1d show the possible configurations of the four bus modes. Appendix C1 shows a memory map of the port as a function of the Bus Mode and further shows which addresses are active or inactive on each of the three possible buses.

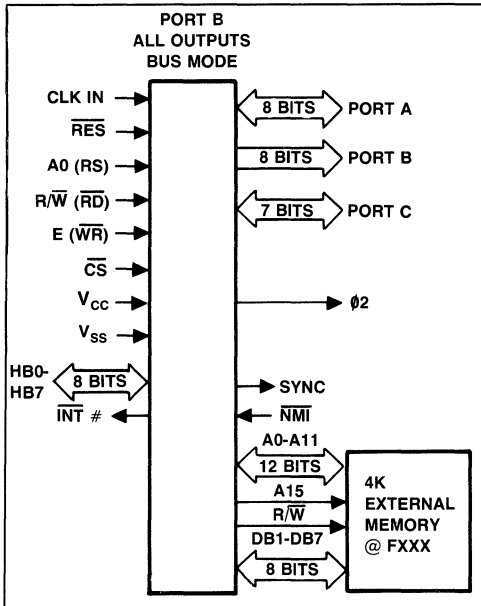


Figure 4-1a.

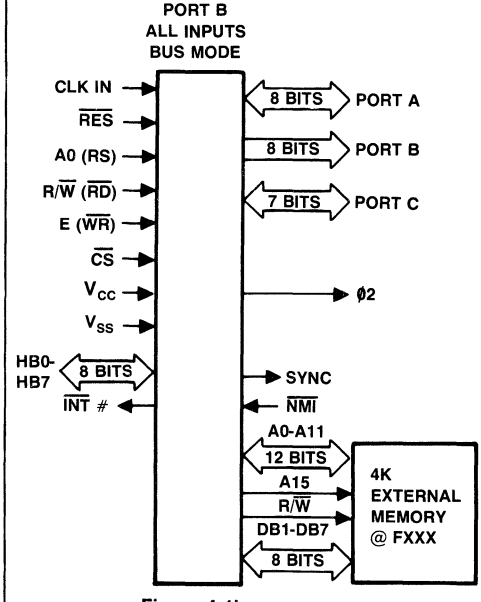


Figure 4-1b.

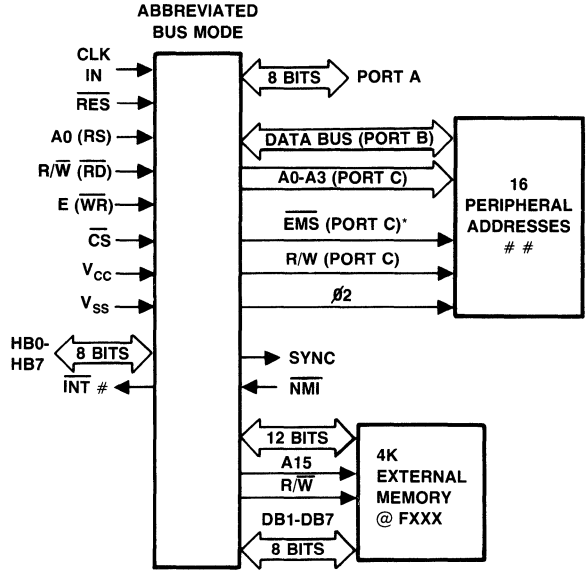


Figure 4-1c.

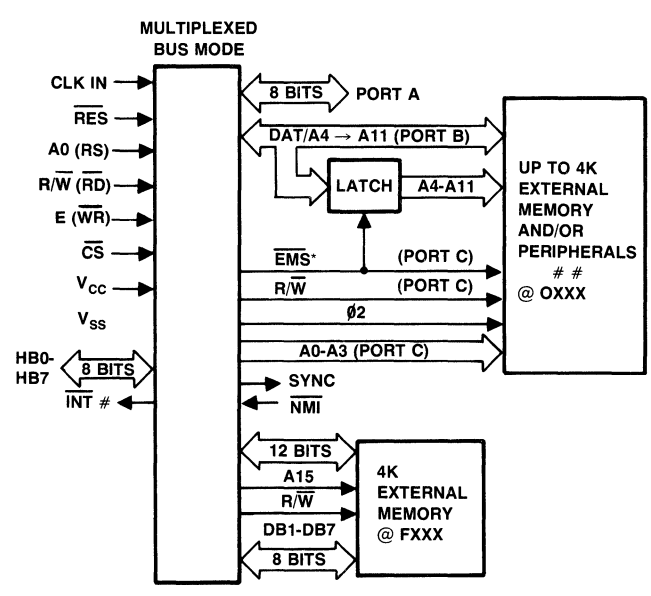


Figure 4-1d.

OPTIONAL PC6
NOT AVAILABLE WITH BOOTSTRAP ROM OPTION
* EMS VALID @ 0100 THRU OFFF

SECTION 5
HOST INTERFACE BUS

Two way data transfers are performed between the IPC and the Host microprocessor by means of the Output Data Register and the Input Data Register. The Host can also write a command to the IDR and read from the Host Status Flag Register. Figure 5-1 shows the Host addressing matrix. A hardware interrupt procedure and a software polling procedure is available to control data traffic between the CPU and Host.

RS (A_0)	READ	WRITE
1	HOST STATUS FLAG	COMMAND INPUT
0	DATA REG OUTPUT	DATA REG INPUT

Figure 5-1. Host Addressing Matrix

5.1 DATA REGISTERS

The device has an 8-bit Input Data Register (IDR) and an 8-bit Output Data Register (ODR). The IDR serves as a temporary storage for commands and data from the Host to the device. When transferring data from the Host to the device, the following conditions are in effect:

- $\overline{CS}$ is asserted
- RS (AO) indicates command input or data input.
- The contents of the host data bus (HB0-HB7) are copied into the IDR when the appropriate Host bus write signals are asserted.

The ODR serves as a temporary storage for data from the device to the Host. When the Host is reading data from the device, the following conditions are in effect·

- $\overline{CS}$ is asserted
- RS (AO) input selects ODR or HSFR
- The contents of ODR or the Flag Register are placed on the host data bus (HB0-HB7) when the appropriate Host read signals are asserted.

5.2 HOST STATUS FLAG REGISTER

A Host Status Flag Register facilitates a software protocol that permits independent and uninterrupted flow of data asynchronously between the host computer and the device.

The Host Status Flag Register contains 8 flag bits that can be read at anytime by either the Host or the device. See Figure 5-2. General purpose flags F2 through F6 are serviced by the device in either read or write modes and monitored by the Host (Read Only).

Flag F1 can be read at anytime by either the host or the device. The F1 flag copies the A0 (RS) input signal during any host write data exchange. The device can write to the F1 flag at any time.

The ODRF (Output Data Register Full) flag is set each time the device writes to the Output Data Register. The setting of the ODRF sets the device Interrupt Status Register IFR3 flag. An Output Interrupt ($\overline{INT}$) may be generated under program control by setting IER3 in the interrupt enable register. The ODRF flag is reset only by a hardware reset or by the host performing a read on the output data register. The ODRF flag is reset following the conclusion of any host output data register read. The resetting of the ODRF causes the reset of the IFR3 flag and thus the reset of the external interrupt ($\overline{INT}$).

The IDRF (Input Data Register Full) flag is set following the conclusion of any host write data exchange. The setting of the IDRF causes IFR2 of the device status register to be set. An internal interrupt may be generated under program control by setting IER2 in the Interrupt Enable Register. The setting of IDRF also causes IFR4 to be reset. The IDRF resets during device read of the input data register. IFR2 sets and IFR4 resets following the reset of IDRF. IFR4 may generate an external output interrupt (INT, input buffer empty), under program control by setting IER4 in the interrupt enable register.

The Host Status Flag Register is cleared by the $\overline{RES}$ input.

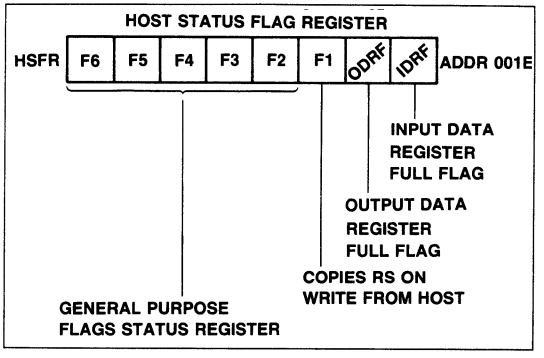


Figure 5-2. Host Status Flag Register Bit Allocation

5.3 HOST COMPUTER INTERFACE

The device will work with a variety of Host Computers. The HOST interface consists of a chip select, one address line, 2 control lines and an 8 bit three state data bus. Internal logic of the device, controlled by MCR4, configures, the address and two control lines to either a 6500 or 8080 operational methodology. The interface is completely asynchronous and will work with a Host Computer up to a 5 MHz bus transfer rate. The device clock input frequency need not be the same as the Host's. A mode control register is set to match the interface to that of the Host device as follows:

MCR4 = 0 When MCR4 is set to a logic zero, the IPC is configured to operate on a 6502/6800 type host bus. In this mode, the E input is connected to the host transfer strobe (VMA or Ø2 for 6800, Ø2 for 6500) and the R/$\overline{W}$ input is connected to the host microprocessor R/$\overline{W}$ output line. Figure 5-3 and Table 5-1, together, specify the relevant timing for read and write cycles on this type of host bus.

MCR4 = 1 When MCR4 is set to a logic one, the IPC is configured for operation on an 8080/Z80 type bus. In this mode, the $\overline{RD}$ input is used as a read strobe and the $\overline{WR}$ input is connected to the write strobe of the host microprocessor bus. Figure 5-4 and Table 5-2 show the relevant timing characteristics for this mode of operation.

Table 5-1. Host Interface Timing Characteristics BSEL = 0 (6500)

CHARACTERISTICS 1 AND 2 MHz	SYMBOL	MIN	MAX
CS, R/W, RS Setup Time	t_{CS}	10	—
Access Time	t_{DA}	—	90*
Data Hold Time	t_{DHR}	10	—
Control Hold Time	t_{HC}	10	—
Write Data Setup Time	t_{WDS}	75	—
Write Data Hold Time	t_{DHW}	10	—
Write Stroke Width	t_{WR}	75	—

*NOTE.
90 ns when loading = 130 pf + 1 TTL LOAD and
75 ns when loading = 90 pf + 1 TTL LOAD.

Table 5-2. Host Interface Timing Characteristics BSEL = 1 (8080)

CHARACTERISTICS 1 AND 2 MH	SYMBOL	MIN	MAX
CS, A0 Setup Time	t_{CS}	10	—
Data Access Time on Read	t_{DA}	—	90*
Data Hold Time	t_{DHR}	10	—
Control Hold Time	t_{HC}	10	—
Write Data Setup Time	t_{WDS}	75	—
Write Data Hold Time	t_{DHW}	10	—
Write Strobe Width	t_{WR}	75	—

*NOTE
90 ns when loading = 130 pf + 1 TTL LOAD and
75 ns when loading = 90 pf + 1 TTL LOAD.

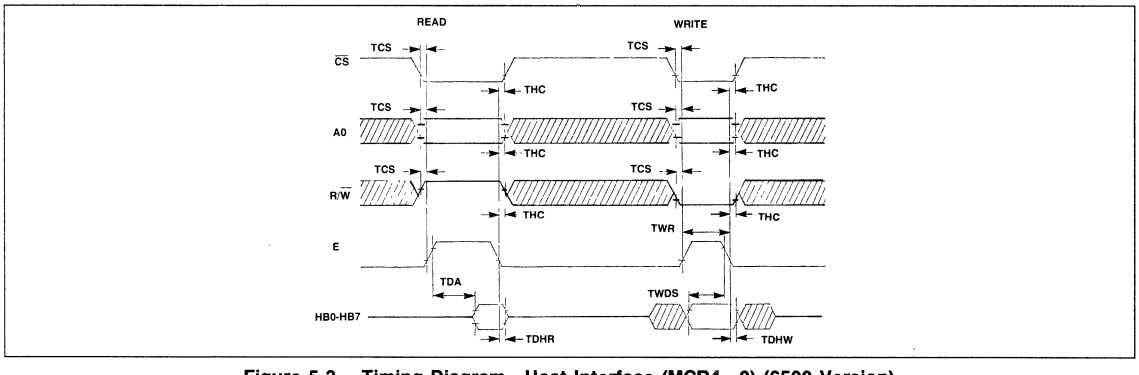


Figure 5-3. Timing Diagram—Host Interface (MCR4 = 0) (6500 Version)

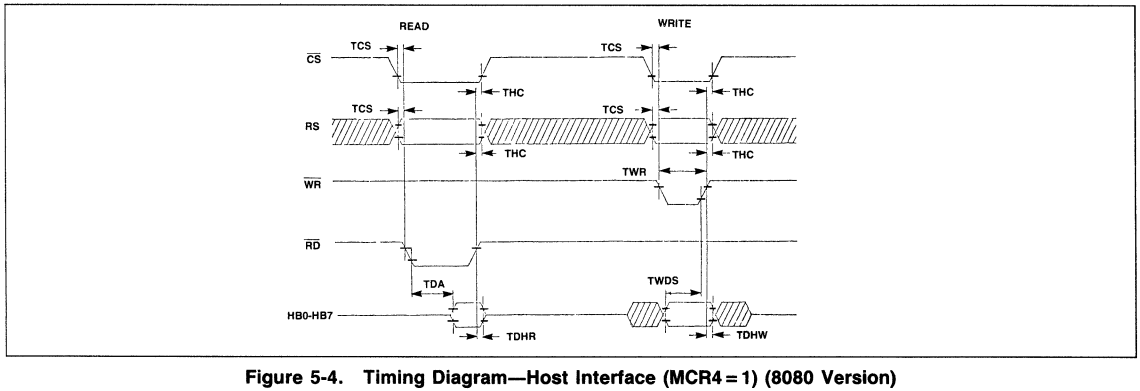


Figure 5-4. Timing Diagram—Host Interface (MCR4 = 1) (8080 Version)

SECTION 6
COUNTER/TIMERS

The device contains a 16-bit counter and a 16-bit latch associated with it. The counter can be independently programmed to operate in one of four modes:

Counter

- Pulse width measurement
- Pulse Generation
- Interval Timer
- Event Counter

Operating modes of the Counter are controlled by the Mode Control Register. All counting begins at the initialization value and decrements When modes are selected requiring a counter input/output line, PA2 is selected for Counter I/O

6.1 COUNTER

The Counter consists of a 16-bit counter and a 16-bit latch organized as follows: Lower Counter (LC), Upper Counter (UC), Lower Latch (LL), and Upper Latch (UL). The counter contains the count of either Ø2 clock pulses or external events, depending on the counter mode selected. The contents of the Counter may be read any time by executing a read at location 0018 for the Upper Counter and at location 001A or location 0019 for the Lower Counter. A read at location 0019 also clears the Counter Underflow Flag (IFR5).

The 16-bit latch contains the counter initialization value, and can be loaded at any time by executing a write to the Upper Latch at location 0018 and the Lower Latch at location 001A. In either case, the contents of the accumulator are copied into the applicable latch register.

The Counter can be started at any time by writing to address 0019. The contents of the accumulator will be copied into the Upper Latch before the contents of the 16-bit latch are transferred to the Counter. The counter is set to the latch value whenever the Counter underflows. When the Counter decrements from 0000 the next counter value will be the latch value, not FFFF, and the Counter Underflow Flag (IFR 5) will be set to "1". This bit may be cleared by reading the Lower Counter at location 0019, by writing to address location 0019, or by $\overline{RES}$.

The Counter operates in any of four modes. These modes are selected by the Counter Mode Control bits in the Control Register.

MCR1 (bit 1)	MCR0 (bit 0)	Mode
0	0	Interval Timer
0	1	Pulse Generation
1	0	Event Counter
1	1	Pulse Width Measurement

The Interval Timer, Pulse Generation, and Pulse Width Measurement Modes are Ø2 clock counter modes. The Event Counter Mode counts the occurrences of an external event on the CNTR line (PA2).

The Counter is set to the Interval Timer Mode (00) when a $\overline{RES}$ signal is generated.

6.1.1 Interval Timer Mode

In the Interval Timer mode the Counter is initialized to the Latch value by either of two conditions:

1. When the Counter is decremented from 0000, the next Counter value is the Latch value (not FFFF).

2. When a write operation is performed to the Load Upper Latch and Transfer Latch to Counter address 0019, the Counter is loaded with the Latch value. Note that the contents of the Accumulator are loaded into the Upper Latch before the Latch value is transferred to the Counter.

The Counter value is decremented by one count at the Ø2 clock rate. The 16-bit Counter can hold from 1 to 65535 counts. The Counter Timer capacity is therefore 1μs to 65.535 ms at the 1 MHz Ø2 clock rate or 0.5μs to 32.767 ms at the 2 MHz Ø2 clock rate. Time intervals greater than the maximum Counter value can be easily measured by counting $\overline{IRQ}$ interrupt requests in the counter $\overline{IRQ}$ interrupt routine.

When the Counter decrements from 0000, the Counter Underflow (IFR5) is set to logic 1. If the Counter Interrupt Enable Bit (IER5) is also set, an $\overline{IRQ}$ interrupt request will be generated. The Counter Underflow bit in the Interrupt Flag Register can be examined in the $\overline{IRQ}$ interrupt routine to determine that the $\overline{IRQ}$ was generated by the Counter Underflow.

While the timer is operating in the Interval Timer Mode, PA2 operates as a PA I/O.

A timing diagram of the Interval Timer Mode is shown in Figure 6-1.

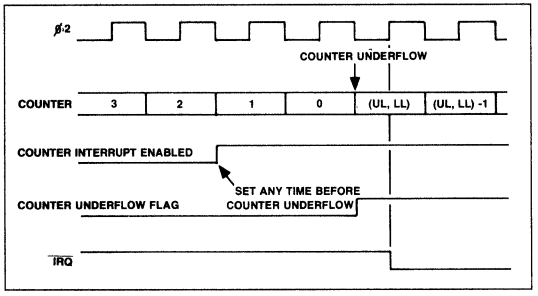


Figure 6-1. Interval Timer Timing Diagram

6.1.2 Pulse Generation Mode

In the Pulse Generation mode, the PA2 line operates as a Counter Output. The line toggles from low to high or from high to low whenever a Counter Underflow occurs, or a write is performed to address 0019.

The normal output waveform is a symmetrical square-wave. The PA2 output is initialized high when entering the mode and transitions low when writing to 0019.

Asymmetric waveforms can be generated if the value of the latch is changed after each counter underflow.

A one-shot waveform can be generated by changing from Pulse Generation to Interval Timer mode after only one occurrence of the output toggle condition.

6.1.3 Event Counter Mode

In this mode PA2 is used as an Event Input line, and the Counter will decrement with each rising edge detected on this line. The maximum rate at which this edge can be detected is one-half the ϕ2 clock rate.

The Counter can count up to 65,535 occurrences before underflowing. As in the other modes, the Counter Underflow bit (IER5) is set to logic 1 if the underflow occurs.

Figure 6.2 is a timing diagram of the Event Counter Mode.

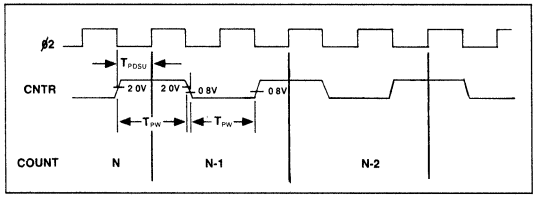
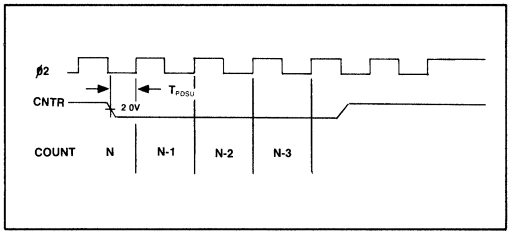


Figure 6-2. Event Counter Mode

6.1.4 Pulse Width Measurement Mode

This mode allows the accurate measurement of a low pulse duration on the PA2 line. The Counter decrements by one count at the ϕ2 clock rate as long as the PA2 line is held in the low state. The Counter is stopped when PA2 is in the high state.

The Counter underflow flag will be set only when the count in the timer reaches zero. Upon reaching zero the timer will be loaded with the latch value and continue counting down as long as the PA2 pin is held low. After the counter is stopped by a high level on PA2, the count will hold as long as PA2 remains high. Any further low levels on PA2 will again cause the counter to count down from its present value. The state of the PA2 line can be determined by testing the state of PA2.



SECTION 7
POWER ON/INITIALIZATION CONSIDERATIONS

7.1 POWER ON TIMING

After application of VCC power to the device, $\overline{RES}$ must be held low for at least eight stable ø2 clock cycles after V_{CC} reaches operating range.

Figure 7-1 illustrates the power turn-on waveforms. External clock stabilization time is typically 20ms.

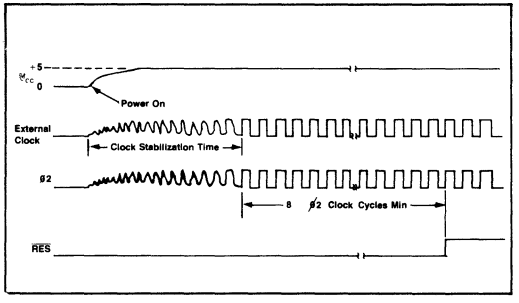


Figure 7-1. Power Turn-On Timing Detail

7.2 POWER-ON RESET

The occurrence of $\overline{RES}$ going from low to high will cause the device to set the Interrupt Mask Bit—bit 2 of the Processor Status Register—and initiate a reset vector fetch at address FFFC and FFFD to begin user program execution. All of the I/O ports will be initialized to the high (logic 1) state. All bits of the Control Register will be cleared causing the Interval Timer counter mode to be selected and causing all interrupt enabled bits to be reset.

7.3 RESET ($\overline{RES}$) CONDITIONS

When $\overline{RES}$ is driven from low to high the device is put in a reset state causing the registers and I/O ports to be set as shown in Table 7-1.

Table 7-1. $\overline{RES}$ Initialization of I/O Ports and Registers

	7	6	5	4	3	2	1	0
REGISTERS								
Processor Status	—	—	—	—	—	1	—	—
Mode Control (MCR)	0	0	0	0	0	0	0	0
Int. Enable (IER)	0	0	0	0	0	0	0	0
Int. Flag (IFR)	0	0	0	1	0	0	0	0
Host Status Flag	0	0	0	0	0	0	0	0
Input Data	0	0	0	0	0	0	0	0
Output Data	0	0	0	0	0	0	0	0
PORTS								
PA Latch	1	1	1	1	1	1	1	1
PB Latch	1	1	1	1	1	1	1	1
PC Latch	1	1	1	1	1	1	1	1

All RAM and other CPU registers will initialize in a random, non-repeatable data pattern

7.4 INITIALIZATION

Any initialization process for the device should include a $\overline{RES}$ as indicated in the preceding paragraphs. After stabilization of the external clock (if a power on situation) an initialization routine should be executed to perform (as a minimum) the following functions:

1. The Stack Pointer should be set
2. Clear or Set Decimal Mode
3. Set or Clear Carry Flag
4. Set up Mode Controls and Counter as required
5. Clear Interrupts.

A typical initialization routine could be as follows:

LDX	Load stack pointer starting address into X Register
TXS	Transfer X Register value to Stack Pointer
CLD	Clear Decimal Mode
SEC	Set Carry Flag
. . . .	Set-up Mode Control,
. . . .	Counter, special function
. . . .	registers and Clear RAM as required
CLI	Clear Interrupts

APPENDIX A
EXPANDED R6502 INSTRUCTION SET

This appendix contains a summary of the R6502 instruction set. For detailed information, consult the R6502 Microcomputer System Programming Manual, Document 29650 N30.

The four instructions notated with a * are added instructions for the IPC devices which are not part of the standard 6502 instruction set.

A.1 INSTRUCTION SET IN ALPHABETIC SEQUENCE

MNEMONIC	INSTRUCTION	MNEMONIC	INSTRUCTION
ADC	Add Memory to Accumulator with Carry	LDA	Load Accumulator with Memory
AND	"AND" Memory with Accumulator	LDX	Load Index X with Memory
ASL	Shift Left One Bit (Memory or Accumulator)	LDY	Load Index Y with Memory
		LSR	Shift One Bit Right (Memory or Accumulator)
*BBR	Branch on Bit Reset Relative		
*BBS	Branch on Bit Set Relative		
BCC	Branch on Carry Clear	NOP	No Operation
BCS	Branch on Carry Set		
BEQ	Branch on Result Zero		
BIT	Test Bits in Memory with Accumulator	ORA	"OR" Memory with Accumulator
BMI	Branch on Result Minus		
BNE	Branch on Result not Zero		
BPL	Branch on Result Plus	PHA	Push Accumulator on Stack
BRK	Force Break	PHP	Push Processor Status on Stack
BVC	Branch on Overflow Clear	PLA	Pull Accumulator from Stack
BVS	Branch on Overflow Set	PLP	Pull Processor Status from Stack
CLC	Clear Carry Flag	*RMB	Reset Memory Bit
CLD	Clear Decimal Mode	ROL	Rotate One Bit Left (Memory or Accumulator)
CLI	Clear Interrupt Disable Bit		
CLV	Clear Overflow Flag	ROR	Rotate One Bit Right (Memory or Accumulator)
CMP	Compare Memory and Accumulator		
CPX	Compare Memory and Index X	RTI	Return from Interrupt
CPY	Compare Memory and Index Y	RTS	Return from Subroutine
DEC	Decrement Memory by One	SBC	Subtract Memory from Accumulator with Borrow
DEX	Decrement Index X by One		
DEY	Decrement Index Y by One	SEC	Set Carry Flag
		SED	Set Decimal Mode
		SEI	Set Interrupt Disable Status
EOR	"Exclusive-Or" Memory with Accumulator	*SMB	Set Memory Bit
		STA	Store Accumulator in Memory
		STX	Store Index X in Memory
		STY	Store Index Y in Memory
INC	Increment Memory by One		
INX	Increment Index X by One		
INY	Increment Index Y by One	TAX	Transfer Accumulator to Index X
		TAY	Transfer Accumulator to Index Y
		TSX	Transfer Stack Pointer to Index X
JMP	Jump to New Location	TXA	Transfer Index X to Accumulator
JSR	Jump to New Location Saving Return Address	TXS	Transfer Index X to Stack Register
		TYA	Transfer Index Y to Accumulator

A.2 R6500/1-11 INSTRUCTION SET SUMMARY TABLE

ADDRESSING MODES

MNEMONIC	OPERATION	IMMEDIATE OP	n	#	ABSOLUTE OP	n	#	ZERO PAGE OP	n	#	ACCUM OP	n	#	IMPLIED OP	n	#
ADC	A+M+C→A (4)(1)	69	2	2	6D	4	3	65	3	2						
AND	A M→A (1)	29	2	2	2D	4	3	25	3	2						
ASL	C← [7 Ø] ←Ø				ØE	6	3	Ø6	5	2	ØA	2	1			
BBR[#(Ø-7)]	Branch on M_b=Ø (5)															
BBS[#(Ø-7)]	Branch on M_b=1 (5)															
BCC	Branch on C=Ø (2)															
BCS	Branch on C=1 (2)															
BEQ	Branch on Z=1 (2)															
BIT	A M				2C	4	3	24	3	2						
BMI	Branch on N=1 (2)															
BNE	Branch on Z=Ø (2)															
BPL	Branch on N=Ø (2)															
BRK	Break													00	7	1
BVC	Branch on V=Ø (2)															
BVS	Branch on V=1 (2)															
CLC	Ø→C													18	2	1
CLD	Ø→D													D8	2	1
CLI	Ø→I													58	2	1
CLV	Ø→V													B8	2	1
CMP	A-M	C9	2	2	CD	4	3	C5	3	2						
CPX	X-M	EØ	2	2	EC	4	3	E4	3	2						
CPY	Y-M	CØ	2	2	CC	4	3	C4	3	2						
DEC	M-1→M				CE	6	3	C6	5	2						
DEX	X-1→X													CA	2	1
DEY	Y-1→Y													88	2	1
EOR	AVM→A (1)	49	2	2	4D	4	3	45	3	2						
INC	M+1→M				EE	6	3	E6								
INX	X+1→X													EB	2	1
INY	Y+1→Y													C8	2	1
JMP	Jump to New Loc				4C	3	3									
JSR	Jump Sub				2Ø	6	3									
LDA	M→A (1)	A9	2	2	AD	4	3	A5	3	2						
LDX	M→X (1)	A2	2	2	AE	4	3	A6	3	2						
LDY	M→Y (1)	AØ	2	2	AC	4	3	A4	3	2						
LSR	Ø→ [7 Ø] →C				4E	6	3	46	5	2	4A	2	1			
NOP	No Operation													EA	2	1
ORA	AVM→A	Ø9	2	2	ØD	4	3	Ø5	3	2						
PHA	A→Ms S-1→S													48	3	1
PHP	P→Ms S-1→S													08	3	1
PLA	S+1→S Ms→A													68	4	1
PLP	S+1→S Ms→P													28	4	1
RMB[#(Ø-7)]	Ø→M_b (5)															
RØL	←[7 Ø]←[C]←				2E	6	3	26	5	2	2A	2	1			
RØR	→[C]→[7 Ø]→				6E	6	3	66	5	2	6A	2	1			
RTI	Rtrn Int													4Ø	6	1
RTS	Rtrn Sub													6Ø	6	1
SBC	A-M-C→A (1)	E9	2	2	ED	4	3	E5	3	2						
SEC	1→C													38	2	1
SED	1→D													F8	2	1
SEI	1→T													78	2	1
SMB[#(Ø-7)]	1→M_b (5)															
STA	A→M				8D	4	3	85	3	2						
STX	X→M				8E	4	3	86	3	2						
STY	Y→M				8C	4	3	84	3	2						
TAX	A→X													AA	2	1
TAY	A→Y													A8	2	1
TSX	S→X													BA	2	1
TXA	X→A													8A	2	1
TXS	X→S													9A	2	1
TYA	Y→A													98	2	1

MNEMONIC	(IND, X) OP	n	#	(IND), Y OP	n	#	Z PAGE, X OP	n	#	ABS, X OP	n	#	ABS, Y OP	n	#
ADC	61	6	2	71	5	2	75	4	2	7D	4	3	79	4	3
AND	21	6	2	31	5	2	35	4	2	3D	4	3	39	4	3
ASL							16	6	2	1E	7	3			
CMP	C1	6	2	D1	5	2	D5	4	2	DD	4	3	D9	4	3
DEC							D6	6	2	DE	7	3			
EOR	41	6	2	51	5	2	55	4	2	5D	4	3	59	4	3
INC							F6	6	2	FE	7	3			
LDA	A1	6	2	B1	5	2	B5	4	2	BD	4	3	B9	4	3
LDX													BE	4	3
LDY							B4	4	2	BC	4	3			
LSR							56	6	2	5E	7	3			
ORA	Ø1	6	2	11	5	2	15	4	2	1D	4	3	19	4	3
RØL							36	6	2	3E	7	3			
RØR							76	6	2	7E	7	3			
SBC	E1	6	2	F1	5	2	F5	4	2	FD	4	3	F9	4	3
STA	81	6	2	91	6	2	95	4	2	9D	5	3	[illegible]	5	3
STY							94	4	2						

MNEMONIC	RELATIVE OP	n	#	INDIRECT OP	n	#	Z PAGE, Y OP	n	#	BIT ADDRESSING (OP BY BIT #) Ø	1	2	3	4	5	6	7	PROCESSOR STATUS CODES 7 6 5 4 3 2 1 Ø / N V • B D I Z C
ADC																		N V • • • • Z C
AND																		N • • • • • Z •
ASL																		N • • • • • Z C
BBR[#(Ø-7)]										ØF	1F	2F	3F	4F	5F	6F	7F	• • • • • • • •
BBS[#(Ø-7)]										8F	9F	AF	BF	CF	DF	EF	FF	• • • • • • • •
BCC	9Ø	2	2															• • • • • • • •
BCS	BØ	2	2															• • • • • • • •
BEQ	FØ	2	2															• • • • • • • •
BIT																		M_7 M_6 • • • • Z •
BMI	3Ø	2	2															• • • • • • • •
BNE	DØ	2	2															• • • • • • • •
BPL	1Ø	2	2															• • • • • • • •
BRK																		• • • 1 • 1 • •
BVC	5Ø	2	2															• • • • • • • •
BVS	7Ø	2	2															• • • • • • • •
CLC																		• • • • • • • Ø
CLD																		• • • • Ø • • •
CLI																		• • • • • Ø • •
CLV																		• Ø • • • • • •
CMP																		N • • • • • Z C
CPX																		N • • • • • Z C
CPY																		N • • • • • Z C
DEC																		N • • • • • Z •
DEX																		N • • • • • Z •
DEY																		N • • • • • Z •
EOR																		N • • • • • Z •
INC																		N • • • • • Z •
INX																		N • • • • • Z •
INY																		N • • • • • Z •
JMP				6C	5	3												• • • • • • • •
JSR																		• • • • • • • •
LDA																		N • • • • • Z •
LDX							B6	4	2									N • • • • • Z •
LDY																		N • • • • • Z •
LSR																		Ø • • • • • Z C
NOP																		• • • • • • • •
ORA																		N • • • • • Z •
PHA																		• • • • • • • •
PHP																		• • • • • • • •
PLA																		N • • • • • Z •
PLP																		(Restored)
RMB[#(Ø-7)]										Ø7	17	27	37	47	57	67	77	• • • • • • • •
RØL																		N • • • • • Z C
RØR																		N • • • • • Z C
RTI																		(Restored)
RTS																		• • • • • • • •
SBC																		N V • • • • Z (3)
SEC																		• • • • • • • 1
SED																		• • • • 1 • • •
SEI																		• • • • • 1 • •
SMB[#(Ø-7)]										87	97	A7	B7	C7	D7	E7	F7	• • • • • • • •
STA																		• • • • • • • •
STX							96	4	2									• • • • • • • •
STY																		• • • • • • • •
TAX																		N • • • • • Z •
TAY																		N • • • • • Z •
TSX																		N • • • • • Z •
TXA																		N • • • • • Z •
TXS																		• • • • • • • •
TYA																		N • • • • • Z •

NOTES
1 Add 1 to N if page boundary is crossed
2. Add 1 to N if branch occurs to same page
Add 2 to N if branch occurs to different page
3 Carry not = Borrow
4 If in decimal mode Z flag is invalid
accumulator must be checked on zero result
5. Effects 8-bit data field of the specified zero page address

LEGEND
X = Index X
Y = Index Y
A = Accumulator
M = Memory per effective address
M_s = Memory per stack pointer
M_b = Selecter zero page memory bit
M_7 = Memory Bit 7
M_6 = Memory Bit 6
• = Add
– = Subtract
∧ = And
V = Or
⊻ = Exclusive Or
m = Number of cycles
\# = Number of Bytes

A.3 INSTRUCTION CODE MATRIX

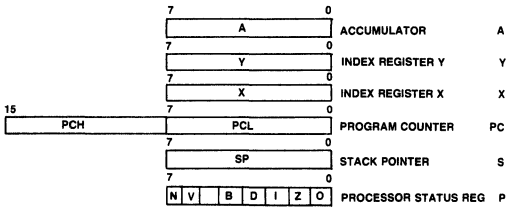
MSD \ LSD	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	MSD
0	BRK Implied 1 7	ORA (IND, X) 2 6				ORA ZP 2 3	ASL ZP 2 5	RMB0 ZP 2 5	PHP Implied 1 3	ORA IMM 2 2	ASL Accum 1 2			ORA ABS 3 4	ASL ABS 3 6	BBR0 ZP 3 5**	0
1	BPL Relative 2 2**	ORA (IND), Y 2 5*				ORA ZP, X 2 4	ASL ZP, X 2 6	RMB1 ZP 2 5	CLC Implied 1 2	ORA ABS, Y 3 4*				ORA ABS, X 3 4*	ASL ABS, X 3 7	BBR1 ZP 3 5**	1
2	JSR Absolute 3 6	AND (IND, X) 2 6			BIT ZP 2 3	AND ZP 2 3	ROL ZP 2 5	RMB2 ZP 2 5	PLP Implied 1 4	AND IMM 2 2	ROL Accum 1 2		BIT ABS 3 4	AND ABS 3 4	ROL ABS 3 6	BBR2 ZP 3 5**	2
3	BMI Relative 2 2**	AND (IND, Y) 2 5*				AND ZP, X 2 4	ROL ZP, X 2 6	RMB3 ZP 2 5	SEC Implied 1 2	AND ABS, Y 3 4*				AND ABS, X 3 4*	ROL ABS, X 3 7	BBR3 ZP 3 5**	3
4	RTI Implied 1 6	EOR (IND, X) 2 6				EOR ZP 2 3	LSR ZP 2 5	RMB4 ZP 2 5	PHA Implied 1 3	EOR IMM 2 2	LSR Accum 1 2		JMP ABS 3 3	EOR ABS 3 4	LSR ABS 3 6	BBR4 ZP 3 5**	4
5	BVC Relative 2 2**	EOR (IND), Y 2 5*				EOR ZP, X 2 4	LSR ZP, X 2 6	RMB5 ZP 2 5	CLI Implied 1 2	EOR ABS, Y 3 4*				EOR ABS, X 3 4*	LSR ABS, X 3 7	BBR5 ZP 3 5**	5
6	RTS Implied 1 6	ADC (IND, X) 2 6				ADC ZP 2 3	ROR ZP 2 5	RMB6 ZP 2 5	PLA Implied 1 4	ADC IMM 2 2	ROR Accum 1 2		JMP Indirect 3 5	ADC ABS 3 4	ROR ABS 3 6	BBR6 ZP 3 5**	6
7	BVS Relative 2 2**	ADC (IND, Y) 2 5*				ADC ZP, X 2 4	ROR ZP, X 2 6	RMB7 ZP 2 5	SEI Implied 1 2	ADC ABS, Y 3 4*				ADC ABS, X 3 4*	ROR ABS, X 3 7	BBR7 ZP 3 5**	7
8		STA (IND, X) 2 6			STY ZP 2 3	STA ZP 2 3	STX ZP 2 3	SMB0 ZP 2 5	DEY Implied 1 2		TXA Implied 1 2		STY ABS 3 4	STA ABS 3 4	STX ABS 3 4	BBS0 ZP 3 5**	8
9	BCC Relative 2 2**	STA (IND, Y) 2 6			STY ZP, X 2 4	STA ZP, X 2 4	STX ZP, Y 2 4	SMB1 ZP 2 5	TYA Implied 1 2	STA ABS, Y 3 5	TXS Implied 1 2			STA ABS, X 3 5		BBS1 ZP 3 5**	9
A	LDY IMM 2 2	LDA (IND, X) 2 6	LDX IMM 2 2		LDY ZP 2 3	LDA ZP 2 3	LDX ZP 2 3	SMB2 ZP 2 5	TAY Implied 1 2	LDA IMM 2 2	TAX Implied 1 2		LDY ABS 3 4	LDA ABS 3 4	LDX ABS 3 4	BBS2 ZP 3 5**	A
B	BCS Relative 2 2**	LDA (IND), Y 2 5*			LDY ZP, X 2 4	LDA ZP, X 2 4	LDX ZP, Y 2 4	SMB3 ZP 2 5	CLV Implied 1 2	LDA ABS, Y 3 4*	TSX Implied 1 2		LDY ABS, X 3 4*	LDA ABS, X 3 4*	LDX ABS, Y 3 4*	BBS3 ZP 3 5**	B
C	CPY IMM 2 2	CMP (IND, X) 2 6			CPY ZP 2 3	CMP ZP 2 3	DEC ZP 2 5	SMB4 ZP 2 5	INY Implied 1 2	CMP IMM 2 2	DEX Implied 1 2		CPY ABS 3 4	CMP ABS 3 4	DEC ABS 3 6	BBS4 ZP 3 5**	C
D	BNE Relative 2 2**	CMP (IND), Y 2 5*				CMP ZP, X 2 4	DEC ZP, X 2 6	SMB5 ZP 2 5	CLD Implied 1 2	CMP ABS, Y 3 4*				CMP ABS, X 3 4*	DEC ABS, X 3 7	BBS5 ZP 3 5**	D
E	CPX IMM 2 2	SBC (IND, X) 2 6			CPX ZP 2 3	SBC ZP 2 3	INC ZP 2 5	SMB6 ZP 2 5	INX Implied 1 2	SBC IMM 2 2	NOP Implied 1 2		CPX ABS 3 4	SBC ABS 3 4	INC ABS 3 6	BBS6 ZP 3 5**	E
F	BEQ Relative 2 2**	SBC (IND), Y 2 5*				SBC ZP, X 2 4	INC ZP, X 2 6	SMB7 ZP 2 5	SED Implied 1 2	SBC ABS, Y 3 4*				SBC ABS, X 3 4*	INC ABS, X 3 7	BBS7 ZP 3 5**	F
	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	

—OP Code
—Addressing Mode
—Instruction Bytes; Machine Cycles

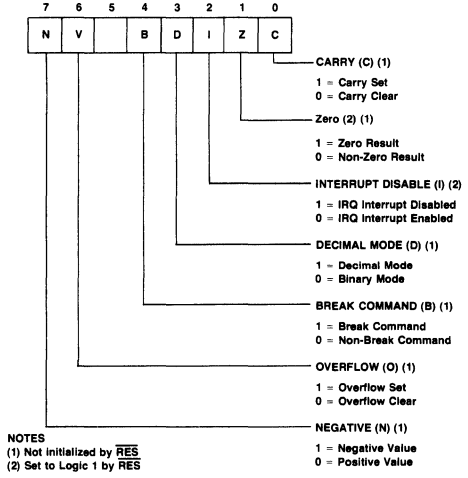
*Add 1 to N if page boundary is crossed.
**Add 1 to N if branch occurs to same page;
add 2 to N if branch occurs to different page.

APPENDIX B
KEY REGISTER SUMMARY

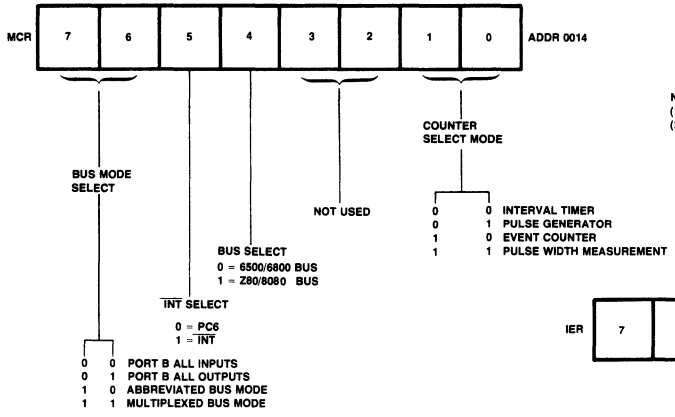
CPU Registers



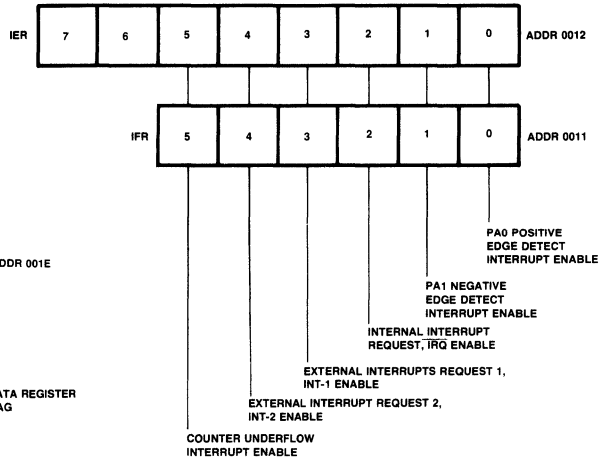
Processor Status Register



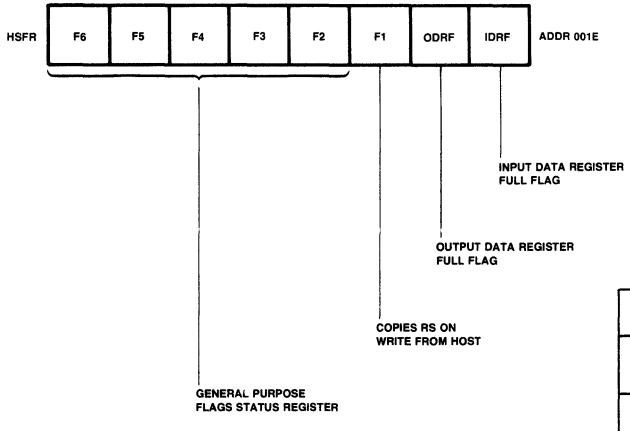
Mode Control Register



Interrupt Enable and Flag Registers



Host Status Flag Register

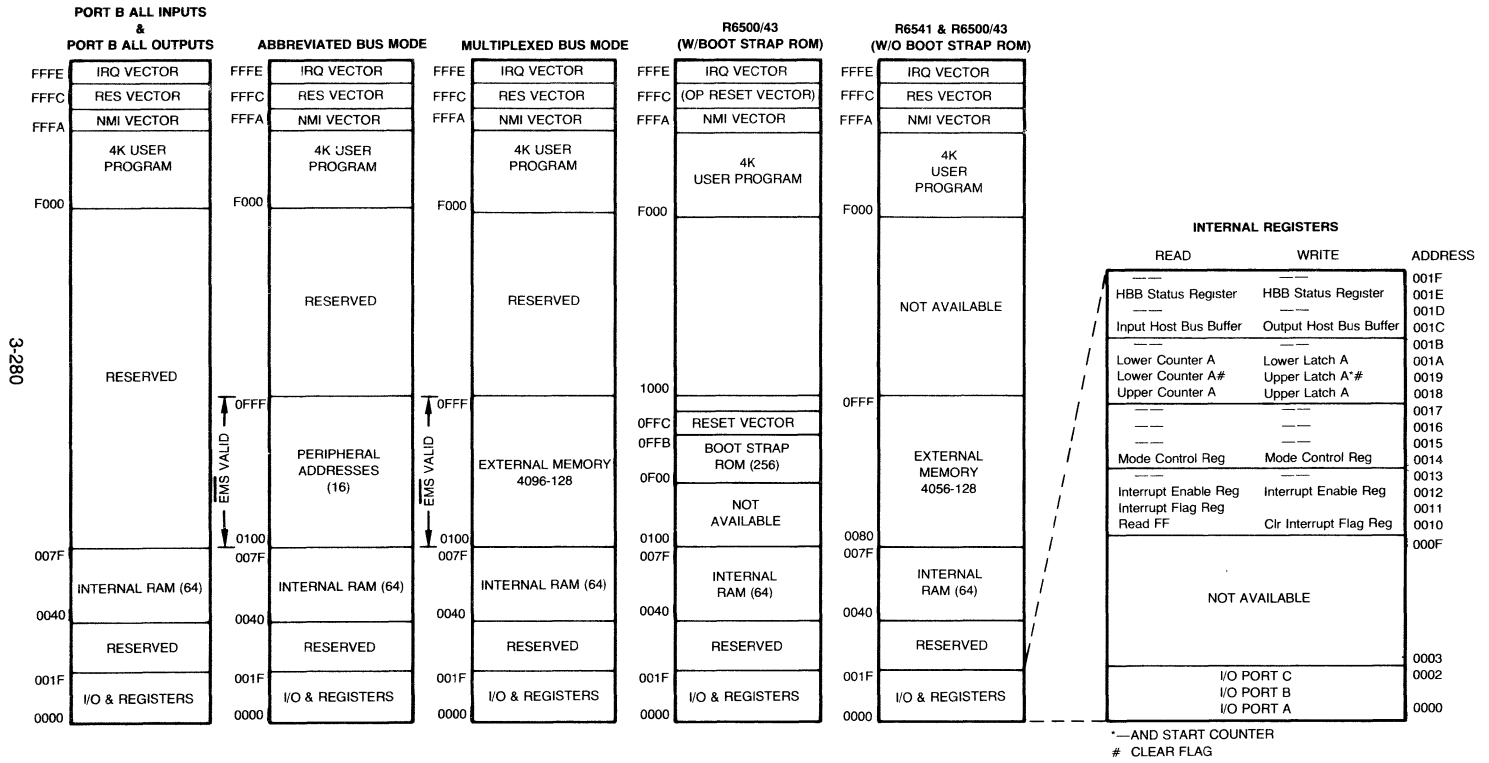


Host Addressing Matrix

RS (A_0)	READ	WRITE
1	HOST STATUS FLAG	COMMAND INPUT
0	DATA REG OUTPUT	DATA REG INPUT

APPENDIX C

C.1 MEMORY MAPS AND ADDRESS AND PIN ASSIGNMENTS



C.2 I/O AND INTERNAL REGISTER ADDRESSES

ADDRESS	READ	WRITE
001F	— —	— —
1E	Host Status Flag Register	Host Status Flag Register
1D	— —	— —
1C	Input Data Register (IDR)	Output Data Register (ODR)
1B	— —	— —
1A	Lower Counter	Lower Latch
19	Lower Counter & Clear Flag (IFR5)	Upper Latch/Transfer Latch to Counter & Clear Flag (IFR5)
18	Upper Counter	Upper Latch
17	— —	— —
16	— —	— —
15	— —	— —
14	Mode Control Register	Mode Control Register
13	— —	— —
12	Interrupt Enable Register	Interrupt Enable Register
11	Interrupt Flag Register	— —
10	Read "FF"	Clear Int Flag Bit
0F	— —	— —
0E	— —	— —
0D	— —	— —
0C	— —	— —
0B	— —	— —
0A	— —	— —
09	— —	— —
08	— —	— —
07	— —	— —
06	— —	— —
05	— —	— —
04	— —	— —
03	— —	— —
02	Port C	Port C
01	Port B	Port B
00	Port A	Port A

C.3 MULTIPLE FUNCTION PIN ASSIGNMENTS

PIN NUMBER R6541Q	PIN NUMBER R6500/43	I/O FUNCTION	ABBREVIATED PORT FUNCTION	MULTIPLEXED PORT FUNCTION
31		PC0	A0	A0
30		PC1	A1	A1
29		PC2	A2	A2
28		PC3	A3	A3
27		PC4	R/$\overline{W}$	R/$\overline{W}$
26		PC5	$\overline{EMS}$	$\overline{EMS}$
25		PC6/$\overline{INT}$	PC6/$\overline{INT}$	PC6/$\overline{INT}$
49		PB0	D0	A4/D0
50		PB1	D1	A5/D1
51		PB2	D2	A6/D2
52		PB3	D3	A7/D3
53		PB4	D4	A8/D4
54		PB5	D5	A9/D5
55		PB6	D6	A10/D6
56		PB7	D7	A11/D7

APPENDIX D
ELECTRICAL SPECIFICATIONS

MAXIMUM RATINGS*

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to +7.0	Vdc
Input Voltage	V_{IN}	−0.3 to +7.0	Vdc
Operating Temperature Commercial	T_A	T_L to T_H 0 to +70	°C
Storage Temperature	T_{STG}	−55 to +150	°C

***NOTE:** Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in other sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

(V_{CC} = 5.0V ±5%, V_{SS} = 0V; T_A = 0° to 70°, unless otherwise specified)

Parameter	Symbol	Min	Typ[1]	Max	Unit	Test Conditions
Input High Voltage	V_{IH}	+2.0	—	V_{CC}	V	
Input Low Voltage	V_{IL}	−0.3	—	+0.8	V	
Input Leakage Current	I_{IN}	—	—	±10.0	µA	V_{IN} = 0 to 5.25V
Input Low Current	I_{IL}	—	−1.0	−1.6	mA	V_{IL} = 0.4V
Output High Voltage	V_{OH}	+2.4	—	V_{CC}	V	I_{LOAD} = −100 µA V_{CC} = 4.75V
Output High Voltage (CMOS)	V_{CMOS}	V_{CC} −30%	—	V_{CC}	V	V_{CC} = 4.75V
Output Low Voltage	V_{OL}	—	—	+0.4	V	I_{LOAD} = 1.6 mA V_{CC} = 4.75V
I/O Port Pull-Up Resistance PA0–PA7, PC0–PC7, PF0–PF7[3], PG0, PG7[3]	R_L	3.0	6.0	11.5	Kohm	
Output High Current (Sourcing)	I_{OH}	−100	—	—	µA	V_{OUT} = 2.4V
Output Low Current (Sinking, PE[3])	I_{OL}	1.6	—	—	mA	V_{OUT} = 0.4V
Darlington Current Drive (PE[3])	I_{OH}	−1.0	—	—	mA	V_{OUT} = 1.5V
Input Capacitance XTLI, XTLO All Others	C_{IN}	 — —	 — —	 50 10	pF	T_A = 25°C V_{IN} = 0V f = 1.0 MHz
Output Capacitance (Three-State Off)	C_{OUT}	—	—	10	pF	T_A = 25°C V_{IN} = 0V f = 1.0 MHz
Power Dissipation (Outputs High)	P_D	—	750	1100	mW	T_A = 25°C

Notes:
1. Typical values measured at T_A = 25°C and V_{CC} = 5.0V.
2. Negative sign indicates outward current flow, positive indicates inward flow.
3. R6500/43 only.

APPENDIX E
TIMING REQUIREMENTS AND CHARACTERISTICS

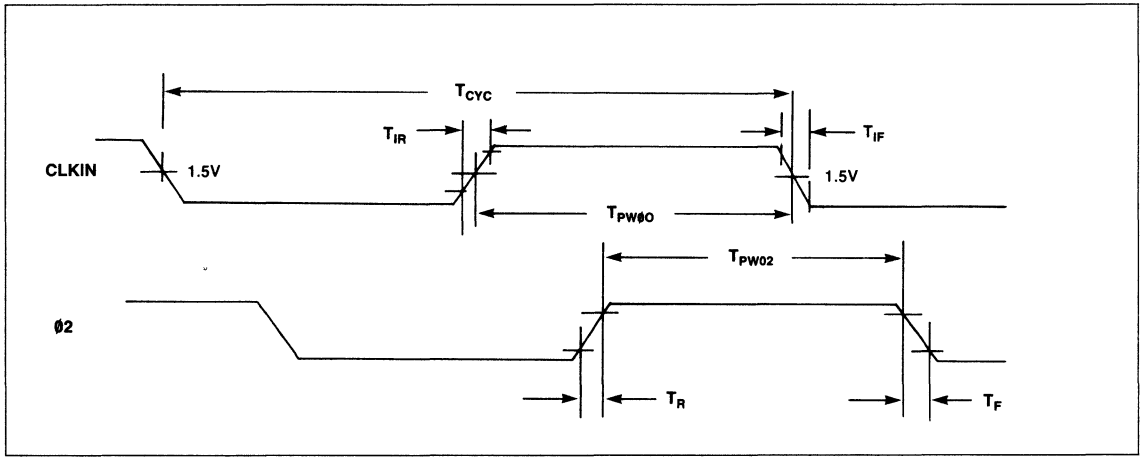
E.1 GENERAL NOTES

1. V_{CC} 5V ±5%, 0°C ≤ T_A ≤ 70°C
2. A valid V_{CC} – $\overline{RES}$ sequence is required before proper operation is achieved.
3. All timing reference levels are 0.8V and 2.0V, unless otherwise specified.
4. All time units are nanoseconds, unless otherwise specified.
5. All capacitive loading is 130 pF maximum, except as noted below:

PA, PB	— 50 pF maximum
PB, PC (I/O Modes Only)	— 50 pF maximum
PB, PC (ABB and Mux Mode)	— 130 pF maximum

E.2 CLOCK TIMING

Symbol	Parameter	1 MHz		2 MHz	
		Min	Max	Min	Max
T_{CYC}	Cycle Time	1000	10 μs	500	10 μs
$T_{PW\phi O}$	CLKIN Input Clock Pulse Width	475	—	240	—
T_{PW02}	Output Clock Pulse Width at Minimum T_{CYC}	$T_{PW\phi O}$	$T_{PW\phi O}$ +25	$T_{PW\phi O}$	$T_{PW\phi O}$ +20
T_R, T_F	Output Clock Rise, Fall Time	—	25	—	15
T_{IR}, T_{IF}	Input Clock Rise, Fall Time	—	10	—	10



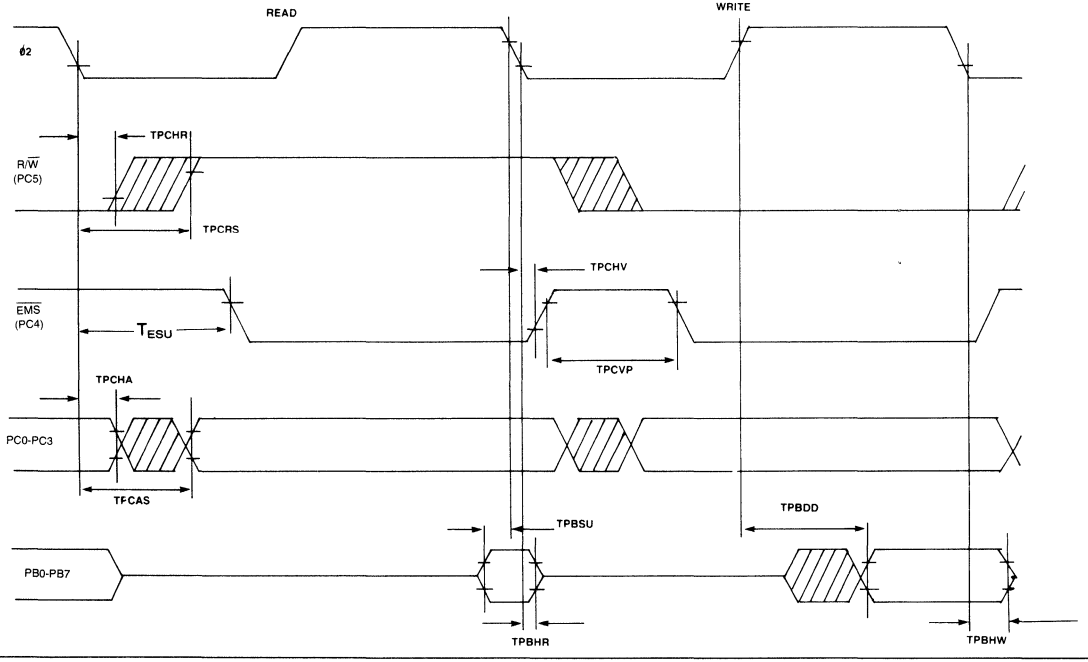
E.3 ABBREVIATED MODE TIMING—PB AND PC

(MCR 5 = 1, MCR 6 = 0, MCR 7 = 1)

SYMBOL	PARAMETER	1 MHz		2 MHz	
		MIN	MAX	MIN	MAX
T_{PCRS}	(PC5) R/W Setup Time	—	225	—	140
T_{PCAS}	(PC0-PC3) Address Setup Time	—	225	—	140
T_{PBSU}	(PB) Data Setup Time	50	—	35	—
T_{PBHR}	(PB) Data Read Hold Time	10	—	10	—
T_{PBHW}	(PB) Data Write Hold Time	30	—	30	—
T_{PBDD}	(PB) Data Output Delay	—	175	—	150
T_{PCHA}	(PC0-PC3) Address Hold Time	30	—	30	—
T_{PCHR}	(PC5) R/W Hold Time	30	—	30	—
T_{PCHV}	(PC4) $\overline{EMS}$ Hold Time	10	—	10	—
T_{PCVP}	(PC4) $\overline{EMS}$ Stabilization Time	30	—	30	—
T_{ESU}	$\overline{EMS}$ Setup Time	—	350	—	210

NOTE 1 Values assume PC0-PC5 have the same capacitive load

E.3.1 Abbreviated Mode Timing Diagram



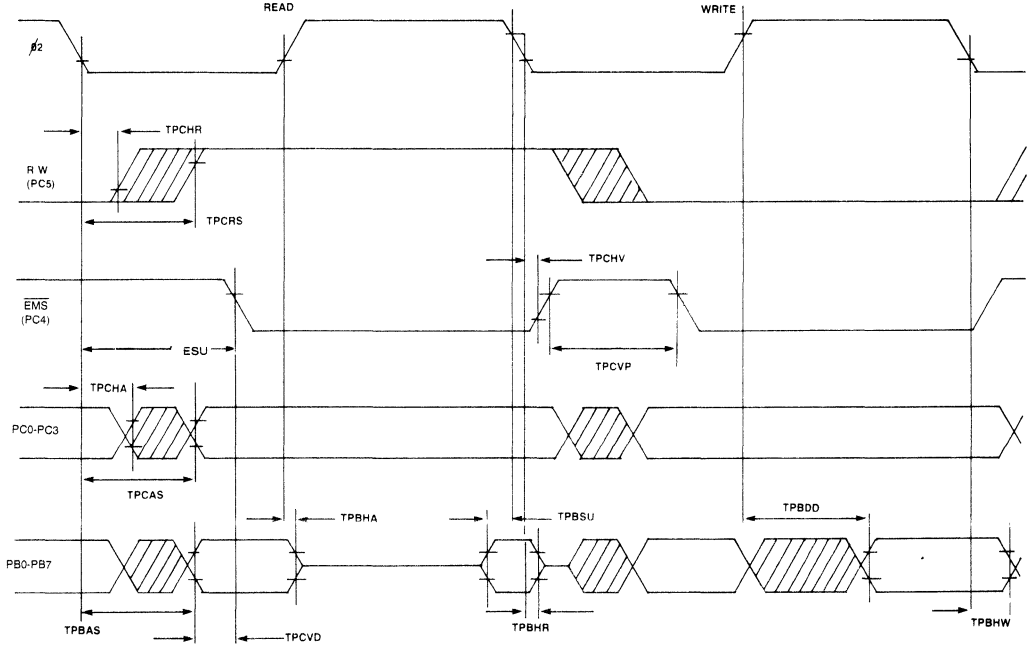
E.4 MULTIPLEXED MODE TIMING—PB AND PC

(MCR 5 = 1, MCR 6 = 1, MCR 7 = 1)

SYMBOL	PARAMETER	1 MHz		2 MHz	
		MIN	MAX	MIN	MAX
T_{PCRS}	(PC5) R/W Setup Time	—	225	—	140
T_{PCAS}	(PC0-PC3) Address Setup Time	—	225	—	140
T_{PBAS}	(PB) Address Setup Time	—	225	—	140
T_{PBSU}	(PB) Data Setup Time	50	—	35	—
T_{PBHR}	(PB) Data Read Hold Time	10	—	10	—
T_{PBHW}	(PB) Data Write Hold Time	30	—	30	—
T_{PBDD}	(PB) Data Output Delay	—	175	—	150
T_{PCHA}	(PC0-PC3) Address Hold Time	30	—	30	—
T_{PBHA}	(PB) Address Hold Time	0	100	0	80
T_{PCHR}	(PC5) R/$\overline{W}$ Hold Time	30	—	30	—
T_{PCHV}	(PC4) $\overline{EMS}$ Hold Time	10	—	10	—
T_{PCVD}[1]	(PC4) Address to $\overline{EMS}$ Delay Time	30	—	30	—
T_{PCVP}	(PC4) $\overline{EMS}$ Stabilization Time	30	—	30	—
T_{ESU}	$\overline{EMS}$ Setup Time	—	350	—	210

NOTE 1 Values assume PC0-PC5 have the same capacitive load.

E.4.1 Multiplex Mode Timing Diagram

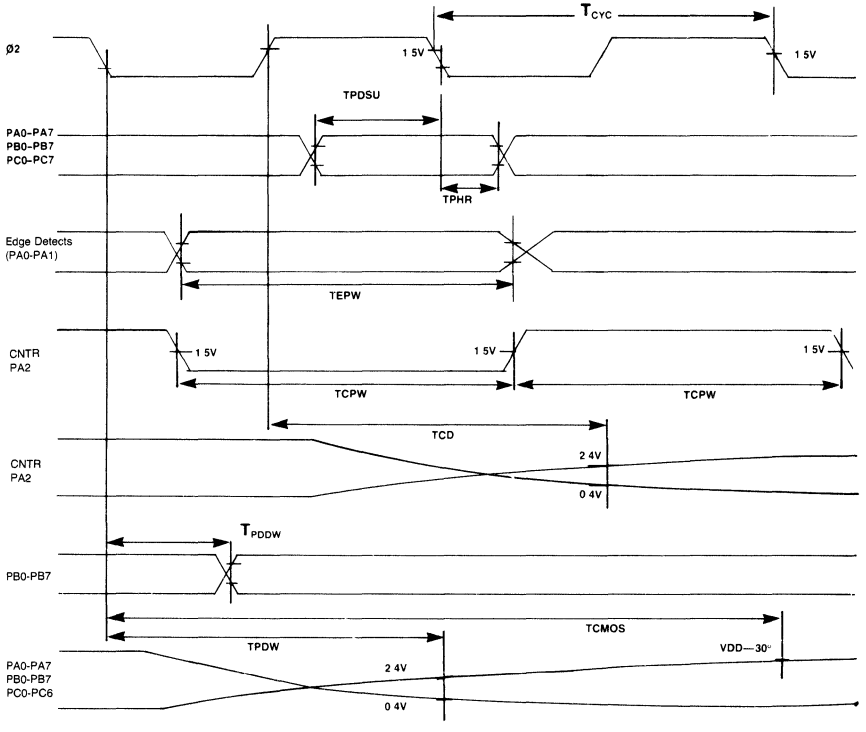


E.5 I/O, EDGE DETECT AND COUNTER TIMING

SYMBOL	PARAMETER	1 MHz		2 MHz	
		MIN	MAX	MIN	MAX
	Internal Write to Peripheral Data Valid				
T_{PDW}(1)	PA, PC TTL	—	500	—	500
T_{CMOS}(1)	PA, PC CMOS	—	1000	—	1000
T_{PDDW}	PB	—	175	—	150
	Peripheral Data Setup Time				
T_{PDSU}	PA, PC	200	—	200	—
T_{PDSU}	PB	50	—	50	—
	Peripheral Data Hold Time				
T_{PHR}	PA, PC	75	—	75	—
T_{PHR}	PB	10	—	10	—
T_{EPW}	PA0-PA1 Edge Detect Pulse Width	T_{CYC}	—	T_{CYC}	—
	Counter				
T_{CPW}	PA2 Input Pulse Width	T_{CYC}	—	T_{CYC}	—
T_{CD}(1)	PA2 Output Delay	—	500	—	500

NOTE 1 Maximum Load Capacitance 50pF Passive Pull-Up Required

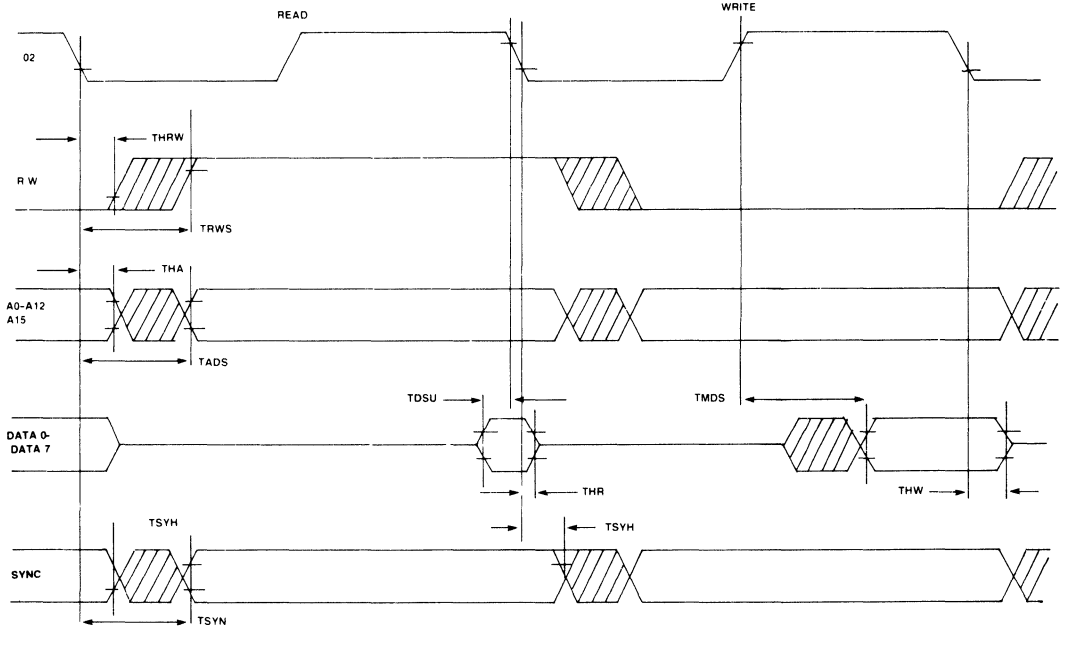
E.5.1 I/O, Edge Detect, Counter.



E.6 MICROPROCESSOR TIMING (DO-D7, A0-A12, A15, SYNC, R/W)

SYMBOL	PARAMETER	1 MHz		2 MHz	
		MIN	MAX	MIN	MAX
T_{RWS}	R/W Setup Time	—	225	—	140
T_{ADS}	A0-A12, A15 Setup Time	—	150	—	75
T_{DSU}	D0-D7 Data Setup Time	50	—	35	—
T_{HR}	D0-D7 Read Hold Time	10	—	10	—
T_{HW}	D0-D7 Write Hold Time	30	—	30	—
T_{MOS}	D0-D7 Write Output Delay	—	175	—	130
T_{SYN}	SYNC Setup	—	225	—	175
T_{HA}	A0-A12, A15 Hold Time	30	—	30	—
T_{HRW}	R/W Hold Time	30	—	30	—
T_{ACC}	External Memory Access Time T_{ACC} $T_{CYC}—T_F—T_{ADS}—T_{DSU}$	—	T_{ACC}	—	T_{ACC}
T_{SYH}	SYNC Hold Time	30	—	30	—

E.6.1 Microprocessor Timing Diagram



SECTION 4
MEMORY PRODUCTS

4

MEMORY PRODUCTS
High Density NMOS ROMs and Low Power CMOS ROMs/EPROM

Rockwell NMOS and CMOS masked ROMs support a broad range of high volume permanent memory applications. A wide selection of different size ROMs with various speed, power and temperature range options—backed by Rockwell dependability and service—will meet your production needs—on schedule and at the right price. Industry standard pin-outs allow easy prototyping with popular EPROMS.

Covering a wide spectrum of sizes—32K through 256K bits, Rockwell NMOS ROMs can efficiently implement such applications as single 4K-byte ROM-based controllers to multiple 32K-byte ROM-based personal computers and graphics work stations. Low-power standby mode is a standard feature on larger density ROMs and a mask option on lower density ROMs.

For low power applications, such as battery powered portable computers and terminals, Rockwell CMOS ROMs are unsurpassed. Extremely low power dissipation in both active and standby modes, reduce power supply requirements and extend operating time between battery replacement/recharge. Latched address (and optional latched chip select) features enhance design-in for both multiplexed and non-multiplexed address/data bus structures. The latched address scheme is compatible with systems using a clocked chip enable, a good engineering practice to eliminate contention and reduce noise. In addition, the ROM output drivers are not enabled until valid data is available. This eliminates noise and excess power consumption due to unneeded output data line transitions.

For many permanent memory applications, or ROM code prototyping, the Rockwell R87C64 is ideal. With low-power dissipation in both active and standby modes, the R87C64 will meet your most demanding power sensitive requirements and allow in-line cost-reduction upgrade to Rockwell CMOS ROMs for larger production runs.

Rockwell Has The Right ROM For Your System

NMOS ROMS									
				Active Power (mW)		Standby Power (mW)			
Density	Organization	Part No.	Max. Access Time (ns)	Typ.	Max.	Typ.	Max.	Package	Compatible PROM
32K	4096 x 8	R2332A	200/250/300/450	125	275	—	—	24-pin DIP	2532
		R2332AS	250/300/450	125	275	37.5	80	24-pin DIP	2532
		R2332B	200/250/300/450	125	275	—	—	24-pin DIP	2732
		R2332BS	250/300/450	125	275	37.5	80	24-pin DIP	2732
64K	8192 x 8	R2364A	200/250/300	125	275	—	—	24-pin DIP	MCM68764
		R2364AS	200/250/300	125	275	37.5	80	24-pin DIP	MCM68764
		R2364B	200/250/300	125	275	—	—	28-pin DIP	2764
		R2364BS	200/250/300	125	275	37.5	80	28-pin DIP	2764
128K	16384 x 8	R23128	250/300	125	275	37.5	80	28-pin DIP	2764
256K	32768 x 8	R23256	200/250/450	125	400	40	100	28-pin DIP	2764
		R23257	200/250/450	125	400	40	100	28-pin DIP	2564
CMOS ROMS									
64K	8192 x 8	R23C64	150/250/300	5[1]	10[1]	0.03	0.05	28-pin DIP	2764[2]
128K	16384 x 8	R23C128	150/250/300	8[1]	15[1]	0.03	0.05	28-pin DIP	2764[2]

Notes:
1. @ 1 μs cycle time.
2. The R23C64 and R23C128 latch the address inputs on the falling edge of $\overline{E}$.

R2332A AND R2332B
32K (4K × 8) STATIC ROM

DESCRIPTION

The R2332A and R2332B ROMs are 32,768-bit static Read-Only Memories (ROMs), organized as 4,096 eight-bit bytes, that offer maximum access times of 200 to 450 nanoseconds, respectively. These ROMs are in industry-standard 24-pin, dual in-line packages, and are available in ceramic or low-cost plastic These fully-static 32K-bit ROMs are compatible with industry standard microprocessors.

All R2332A and R2332B ROMs operate totally asynchronously and require no clock input These devices provide tri-state output buffers for memory expansion These ROMs offer TTL input and output levels with a minimum noise immunity of 0 4 volts

The mask-programmable chip enable input (E/$\overline{E}$) may be programmed to function as a chip select without power down standby mode or as a chip enable with power down standby mode The active level of the enable input is also programmable

FEATURES

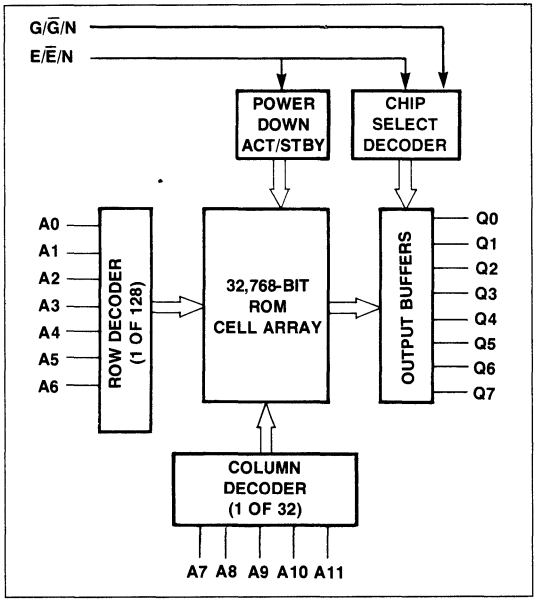
- 4,096 × 8 organization
- Access time· 200 ns, 250 ns, 300 ns, and 450 ns (max.)
- Low power dissipation is 125 mW active, 37.5 mW standby
- Drives two TTL loads and 100 pF
- Single +5V ± 10% power supply
- Totally static operation, no input clock required
- Completely TTL compatible
- Mask-programmable chip enable and chip select
- Tri-state outputs for memory expansion

ORDERING INFORMATION

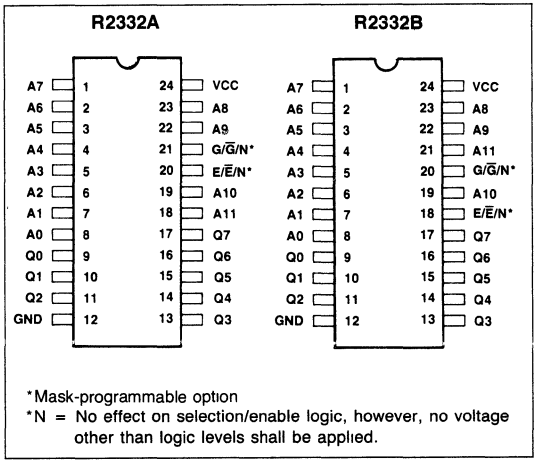
Part Number: R2332-_____

- Package
  - C = Ceramic
  - P = Plastic
- Temperature Range
  - No letter = 0°C to +70°C
  - E = −40°C to +85°C
- Power Down Standby Mode
  - S = Yes
  - No letter = No
- Access Time (Max)
  - 2 = 200 ns
  - 25 = 250 ns
  - 3 = 300 ns
  - No number(s) = 450 ns
- Model
  - A = R2332A
  - B = R2332B

Note Submit ROM codes using Rockwell ROM Code Order Form, Order No 2137



R2332A and R2332B Block Diagram



*Mask-programmable option
*N = No effect on selection/enable logic, however, no voltage other than logic levels shall be applied.

R2332A and R2332B Pin Configuration

4

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.5 to +7.0	Vdc
Input Voltage	V_{IN}	−0.5 to +7.0	Vdc
Output Voltage	V_{OUT}	−0.5 to +7.0	Vdc
Temperature Under Bias Commercial Industrial	T_A	 −10 to +80 −50 to +95	°C
Storage Temperature	T_{STG}	−65 to +150	°C
Power Dissipation	P	1.0	W

***NOTE:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS V_{CC} = 5.0V ± 10%, T_A = 0°C to 70°C (unless otherwise specified)

Symbol	Parameter	Min	Typ[3]	Max	Units	Test Conditions
V_{OH}	Output High Voltage	2.4		V_{CC}	V	V_{CC} = 4.5V, I_{OH} = −400 μA
V_{OL}	Output Low Voltage			0.4	V	V_{CC} = 4.5V, I_{OL} = 3.3 mA
V_{IH}	Input High Voltage	2.0		V_{CC}	V	
V_{IL}	Input Low Voltage	−0.5		0.8	V	
I_{LI}	Input Load Current			10	μA	V_{CC} = 5.5V, 0V ≤ V_{IN} ≤ 5.5V
I_{LO}	Output Leakage Current			±10	μA	V_{CC} = 5.5V, chip deselected, V_{OUT} = +0.4V to V_{CC}
I_{CC}	Power Supply Current, Active		25	55	mA	V_{CC} = 5.5V
I_{SB}	Power Supply Current, Standby[1]		7.5	16	mA	
C_I	Input Capacitance[2]			7	pF	V_{CC} = 5.0V, chip deselected, pin under test at 0V, T_A = 25°C, f = 1 MHz
C_O	Output Capacitance[2]			10	pF	

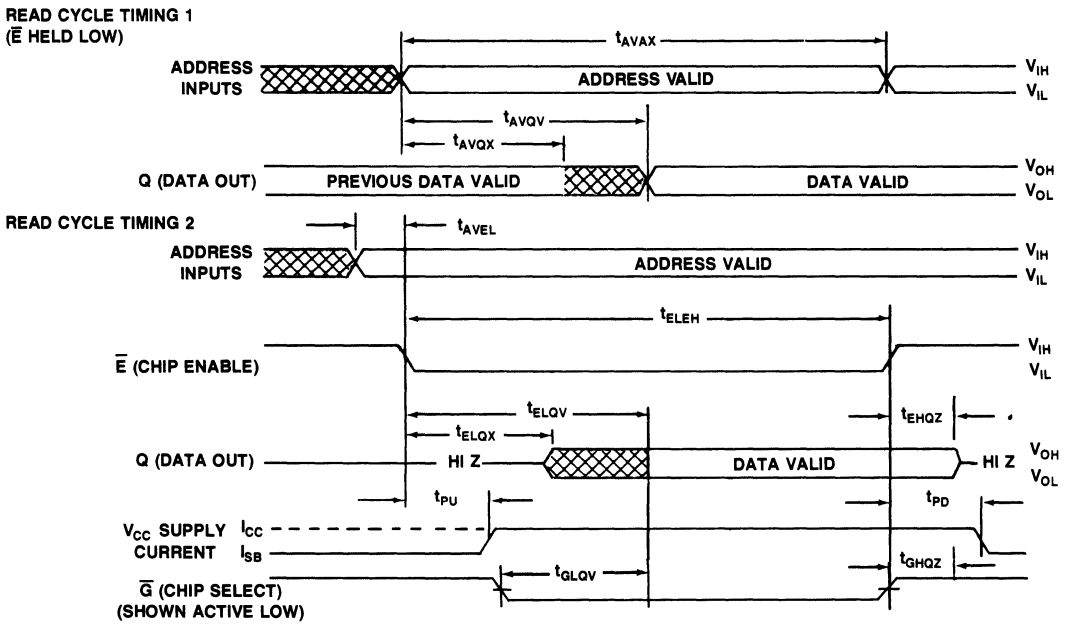
Notes:
1. Applies only to chip enable with power down standby mode
2. This parameter is periodically sampled and is not 100% tested
3. Typical values are for T_A = 25°C and V_{CC} = 5.0V

AC CHARACTERISTICS V_{CC} = 5.0V ± 10%, T_A = 0°C to 70°C (unless otherwise specified)

		R2332-2		R2332-25		R2332-3		R2332-45		
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Min	Max	Unit
t_{AVAX}	Address Valid to Address Don't Care	200		250		300		450		ns
t_{ELEH}	Chip Enable Low to Chip Enable High[2]	200		250		300		450		ns
t_{AVQV}	Address Valid to Output Valid (t_{ACC}) (Access)		200		250		300		450	ns
t_{ELQV}	Chip Enable Low to Output Valid (Access)[2]		200		250		300		450	ns
t_{AVQX}	Address Valid to Output (t_{OH}) Invalid	10		10		10		10		ns
t_{ELQX}	Chip Enable Low to Output (t_{CO}) Invalid	10		10		10		10		ns
t_{EHQZ}	Chip Enable High to Output High Z (t_{DF})	10	70[4]	10	70[4]	10	70[4]	10	70[4]	ns
t_{PU}	Chip Selection to Power Up Time[2]	0		0		0		0		ns
t_{PD}	Chip Deselection to Power Down Time[2]		100[4]		100[4]		100[4]		100[4]	ns
t_{AVEL}	Address Valid to Chip Enable Low	0		0		0		0		ns
t_{GLQV}	Chip Select Low to Output Valid[3]	10	90[4]	10	90[4]	10	90[4]	10	90[4]	ns
t_{GHQZ}	Chip Select High to Output High Z[3]	10	70[4]	10	70[4]	10	70[4]	10	70[4]	ns

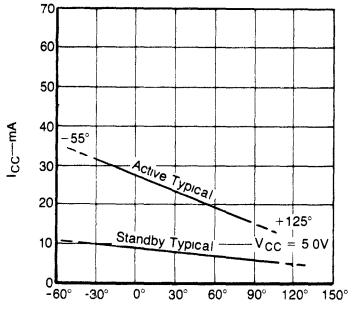
Notes:
1. Test Conditions:
   Output Load: 2 TTL Loads and 100 pF, Input Transition Time: 20 ns; Timing Reference Levels: Input: 1.5V; Output: 0.8V, 2.0V.
2. Mask-programmed for chip enable with power down standby mode.
3. Mask-programmed for chip enable without power down standby mode.
4. Add 20 ns for extended temperature devices (−40°C to +85°C).

TIMING DIAGRAMS



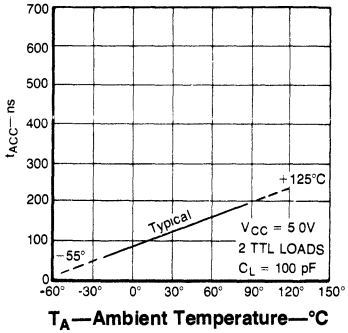
TYPICAL CHARACTERISTICS

SUPPLY CURRENT VS AMBIENT TEMPERATURE



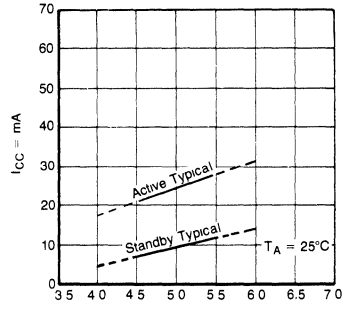
T_A—Ambient Temperature—°C

ACCESS TIME VS AMBIENT TEMPERATURE



T_A—Ambient Temperature—°C

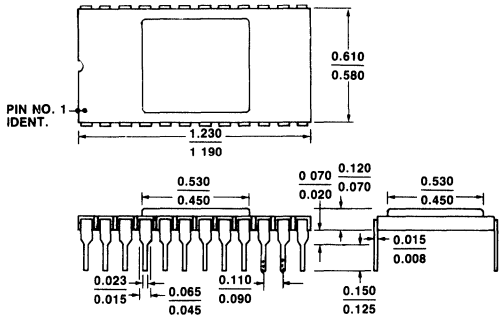
SUPPLY CURRENT VS SUPPLY VOLTAGE



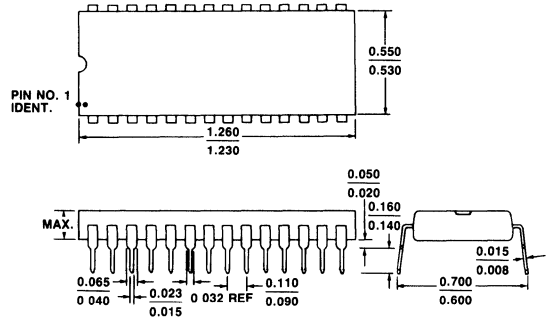
V_{CC}—Volts

PACKAGE DIMENSIONS

24-PIN CERAMIC DIP



24-PIN PLASTIC DIP



Rockwell

R2364A
64K (8K × 8) STATIC ROM

DESCRIPTION

The R2364A2, R2364A25 and R2364A3 are 65,536-bit static Read-Only Memories (ROMs), organized as 8,192 eight-bit bytes, that offer maximum access times of 200, 250 and 300 nanoseconds, respectively. These ROMs are in industry-standard 24-pin, dual in-line packages, and are available in ceramic or low-cost plastic. These fully-static 64K-bit ROMs are compatible with industry standard microprocessors.

All three R2364A ROMs operate totally asynchronously, and require no clock input. These devices provide tri-state output buffers for memory expansion. The R2364A ROMs offer TTL input and output levels with a minimum noise immunity of 0.4 volts.

The mask-programmable chip enable input (E/$\overline{E}$) may be programmed to function as a chip select without power down standby mode or as a chip enable with power down standby mode. The active level of the enable input is also programmable.

FEATURES

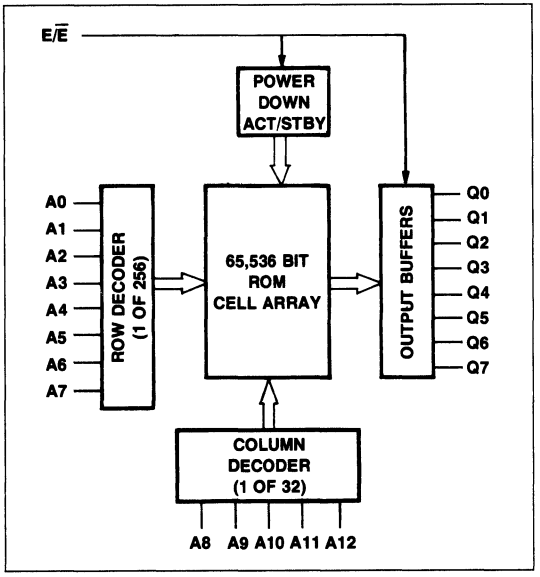
- 8,192 × 8 organization
- Access time: 200 ns, 250 ns, and 300 ns (max.)
- Low power dissipation: 125 mW active, 37.5 mW standby
- Drives two TTL loads and 100 pf
- Single +5V ± 10% power supply
- Totally static operation, no input clock required
- Completely TTL compatible
- Mask-programmable chip enable
- Tri-state outputs for memory expansion

ORDERING INFORMATION

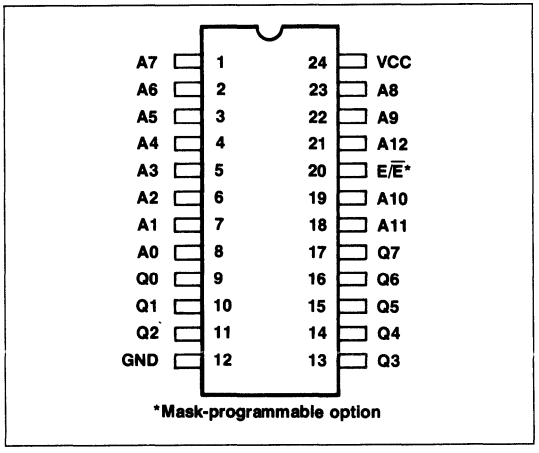
Part Number: R2364A— — — —

- Package:
  - C = Ceramic
  - P = Plastic
- Temperature Range:
  - No letter = 0°C to +70°C
  - E = −40°C to +85°C
- Power Down Standby Mode:
  - S = Yes
  - No letter = No
- Access Time (Max):
  - 2 = 200 ns
  - 25 = 250 ns
  - 3 = 300 ns

Note: Submit ROM codes using Rockwell ROM Code Order Form, Order No. 2137.



R2364A Block Diagram



*Mask-programmable option

R2364A Pin Configuration

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.5 to +7.0	Vdc
Input Voltage	V_{IN}	−0.5 to +7.0	Vdc
Output Voltage	V_{OUT}	−0.5 to +7.0	Vdc
Temperature Under Bias Commercial Industrial	T_A	 −10 to +80 −50 to +95	°C
Storage Temperature	T_{STG}	−65 to +150	°C
Power Dissipation	P	1.0	W

***NOTE:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

V_{CC} = 5.0V ± 10%, T_A = 0°C to 70°C (unless otherwise specified)

Symbol	Parameter	Min	Typ[3]	Max	Units	Test Conditions
V_{OH}	Output High Voltage	2.4		V_{CC}	V	V_{CC} = 4.5V, I_{OH} = −400 μA
V_{OL}	Output Low Voltage			0.4	V	V_{CC} = 4.5V, I_{OL} = 3.3 mA
V_{IH}	Input High Voltage	2.0		V_{CC}	V	
V_{IL}	Input Low Voltage	−0.5		0.8	V	
I_{LI}	Input Load Current			10	μA	V_{CC} = 5.5V, 0V ≤ V_{IN} ≤ 5.5V
I_{LO}	Output Leakage Current			±10	μA	V_{CC} = 5.5V, chip deselected, V_{OUT} = +0.4V to V_{CC}
I_{CC}	Power Supply Current, Active		25	55	mA	V_{CC} = 5.5V
I_{SB}	Power Supply Current, Standby[1]		7.5	16	mA	
C_I	Input Capacitance[2]			7	pF	V_{CC} = 5.0V, chip deselected, pin under test at 0V, T_A = 25°C
C_O	Output Capacitance[2]			10	pF	f = 1 MHz

Notes:
1. Applies only to chip enable with power down standby mode.
2. This parameter is periodically sampled and is not 100% tested.
3. Typical values are for T_A = 25°C and V_{CC} = 5.0V.

AC CHARACTERISTICS

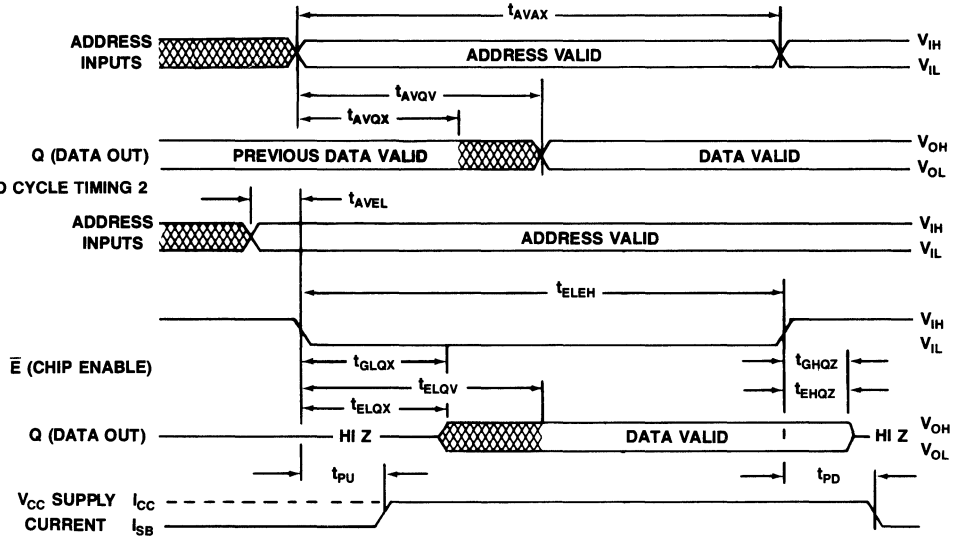
V_{CC} = 5.0V ± 10%, T_A = 0°C to 70°C (unless otherwise specified)

Symbol	Parameter	R2364A2		R2364A25		R2364A3		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{AVAX}	Address Valid to Address Don't Care	200		250		300		ns
t_{ELEH}	Chip Enable Low to Chip Enable High[2]	200		250		300		ns
t_{AVQV}	Address Valid to Output Valid (t_{ACC}) (Access)		200		250		300	ns
t_{ELQV}	Chip Enable Low to Output Valid (Access)[2]		200		250		300	ns
t_{AVQX}	Address Valid to Output (t_{OH}) Invalid	10		10		10		ns
t_{ELQX}	Chip Enable Low to Output (t_{CO}) Invalid	10		10		10		ns
t_{EHQZ}	Chip Enable High to Output High Z (t_{DF})	10	70[4]	10	70[4]	10	70[4]	ns
t_{PU}	Chip Selection to Power Up Time[2]	0		0		0		ns
t_{PD}	Chip Deselection to Power Down Time[2]		100[4]		100[4]		100[4]	ns
t_{AVEL}	Address Valid to Chip Enable Low	0		0		0		ns
t_{GLQX}	Chip Select Low to Output Invalid[3]	10	90[4]	10	90[4]	10	90[4]	ns
t_{GHQZ}	Chip Select High to Output High Z	10	70[4]	10	70[4]	10	70[4]	ns

Notes:
1. Test Conditions:
   Output Load: 2 TTL Loads and 100 pF; Input Transition Time: 20 ns; Timing Reference Levels: Input: 1.5V, Output: 0.8V, 2.0V.
2. Mask-programmed for chip enable with power down standby mode.
3. Mask-programmed for chip enable without power down standby mode.
4. Add 20 ns for extended temperature devices (−40°C to +85°C).

TIMING DIAGRAMS

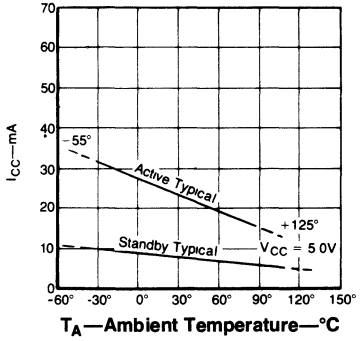
READ CYCLE TIMING 1 ($\overline{E}$ HELD LOW)



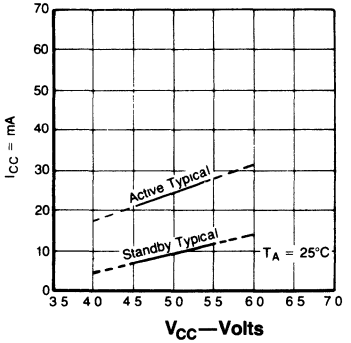
4

TYPICAL CHARACTERISTICS

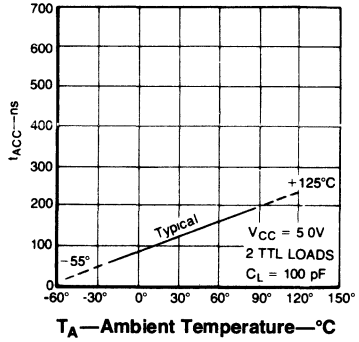
SUPPLY CURRENT VS AMBIENT TEMPERATURE



SUPPLY CURRENT VS SUPPLY VOLTAGE

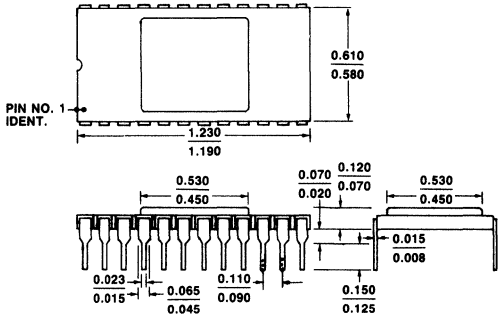


ACCESS TIME VS AMBIENT TEMPERATURE

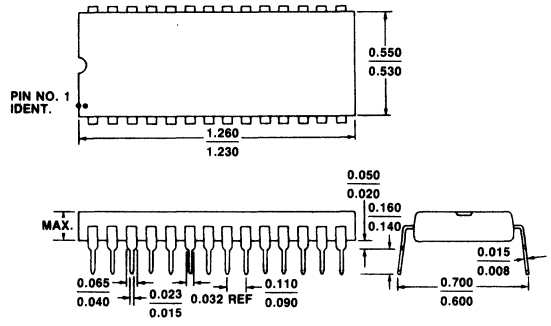


PACKAGE DIMENSIONS

24-PIN CERAMIC DIP



24-PIN PLASTIC DIP



Rockwell

R2364B
64K (8K × 8) STATIC ROM

DESCRIPTION

The R2364B2, R2364B25 and R2364B3 are 65,536-bit static Read-Only Memories (ROMs), organized as 8,192 eight-bit bytes, that offer maximum access times of 200, 250 and 300 nanoseconds, respectively. These ROMs are in industry-standard 28-pin, dual in-line packages, and are available in ceramic or low-cost plastic. These fully-static 64K-bit ROMs are compatible with industry standard microprocessors.

All three R2364B ROMs operate totally asynchronously, and require no clock input. Three mask-programmable chip select inputs allow up to eight 64K ROMs to be OR-tied without external decoding. These devices provide tri-state output buffers for memory expansion. The R2364B ROMs offer TTL input and output levels with a minimum noise immunity of 0.4 volts.

The mask-programmable chip enable input (E/$\overline{E}$) may be programmed to function as a chip select without power down standby mode or as a chip enable with power down standby mode. The active level of the enable input is also programmable.

FEATURES

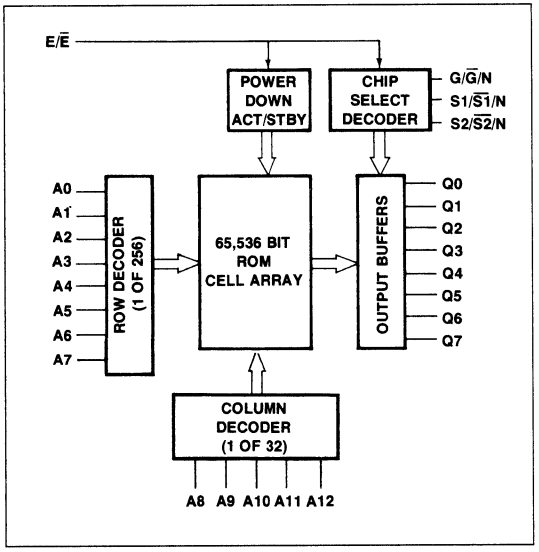
- 8,192 × 8 organization
- Access time: 200 ns, 250 ns and 300 ns (max.)
- Low power dissipation: 125 mW active, 37.5 mW standby
- Drives two TTL loads and 100 pF
- Single +5V ±10% power supply
- Totally static operation, no input clock required
- Completely TTL compatible
- Three tri-state mask-programmable chip select inputs
- Mask-programmable chip enable
- Tri-state outputs for memory expansion

ORDERING INFORMATION

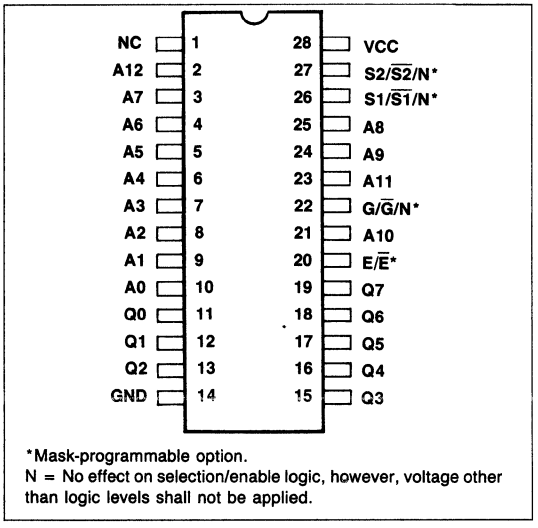
Part Number: R2364B_ _ _ _ _

- Package:
  - C = Ceramic
  - P = Plastic
- Temperature Range:
  - No letter = 0°C to +70°C
  - E = −40°C to +85°C
- Power Down Standby Mode
  - S = Yes
  - No letter = No
- Access Time (Max):
  - 2 = 200 ns
  - 25 = 250 ns
  - 3 = 300 ns

Note: Submit ROM codes using Rockwell ROM Code Order Form, Order No. 2137



R2364B Block Diagram



*Mask-programmable option.
N = No effect on selection/enable logic, however, voltage other than logic levels shall not be applied.

R2364B Pin Configuration

4

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.5 to +7.0	Vdc
Input Voltage	V_{IN}	−0.5 to +7.0	Vdc
Output Voltage	V_{OUT}	−0.5 to +7.0	Vdc
Temperature Under Bias Commercial Industrial	T_A	 −10 to +80 −50 to +95	°C
Storage Temperature	T_{STG}	−65 to +150	°C
Power Dissipation	P	1.0	W

***NOTE:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

V_{CC} = 5.0V ± 10%, T_A = 0°C to 70°C (unless otherwise specified)

Symbol	Parameter	Min	Typ[3]	Max	Units	Test Conditions
V_{OH}	Output High Voltage	2 4		V_{CC}	V	V_{CC} = 4.5V, I_{OH} = −400 μA
V_{OL}	Output Low Voltage			0.4	V	V_{CC} = 4.5V, I_{OL} = 3.3 mA
V_{IH}	Input High Voltage	2.0		V_{CC}	V	
V_{IL}	Input Low Voltage	−0.5		0.8	V	
I_{LI}	Input Load Current			10	μA	V_{CC} = 5.5V, 0V ≤ V_{IN} ≤ 5.5V
I_{LO}	Output Leakage Current			±10	μA	V_{CC} = 5.5V, chip deselected, V_{OUT} = +0.4V to V_{CC}
I_{CC}	Power Supply Current, Active		25	55	mA	V_{CC} = 5.5V
I_{SB}	Power Supply Current, Standby[1]		7.5	16	mA	
C_I	Input Capacitance[2]			7	pF	V_{CC} = 5.0V, chip deselected, pin under test at 0V, T_A = 25°C
C_O	Output Capacitance[2]			10	pF	f = 1 MHz

Notes·
1. Applies only to chip enable with power down standby mode.
2. This parameter is periodically sampled and is not 100% tested
3. Typical values are for T_A = 25°C and V_{CC} = 5.0V.

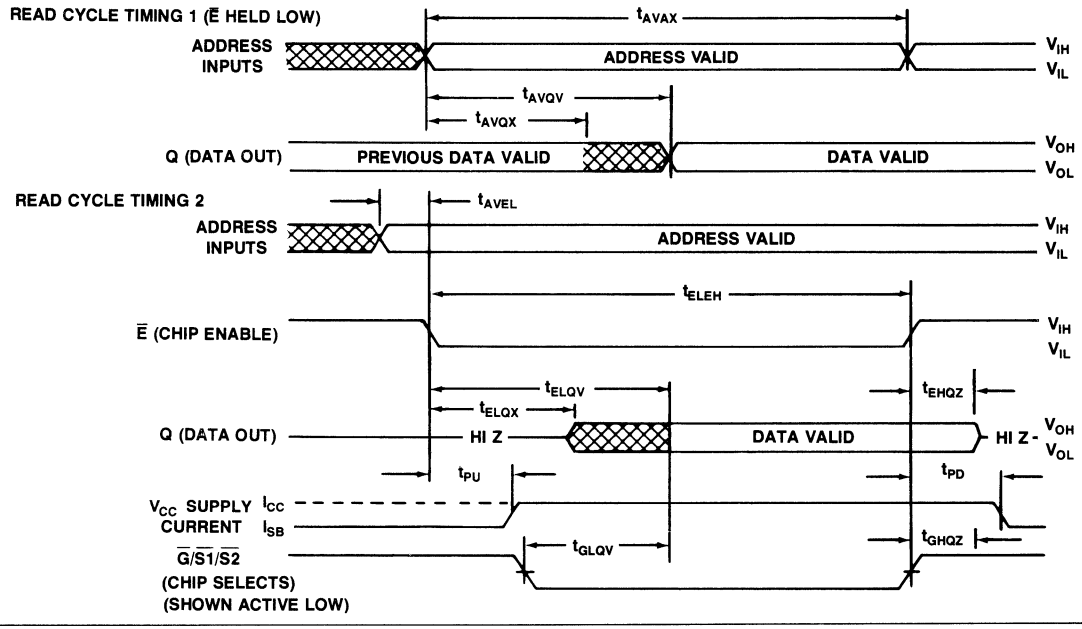
AC CHARACTERISTICS

V_{CC} = 5.0V ± 10%, T_A = 0°C to 70°C (unless otherwise specified)

Symbol	Parameter	R2364B2		R2364B25		R2364B3		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{AVAX}	Address Valid to Address Don't Care	200		250		300		ns
t_{ELEH}	Chip Enable Low to Chip Enable High[2]	200		250		300		ns
t_{AVQV}	Address Valid to Output Valid (t_{ACC}) (Access)		200		250		300	ns
t_{ELQV}	Chip Enable Low to Output Valid (Access)[2]		200		250		300	ns
t_{AVQX}	Address Valid to Output (t_{OH}) Invalid	10		10		10		ns
t_{ELQX}	Chip Enable Low to Output (t_{CO}) Invalid	10		10		10		ns
t_{EHQZ}	Chip Enable High to Output High Z (t_{DF})	10	70[4]	10	70[4]	10	70[4]	ns
t_{PU}	Chip Selection to Power Up Time[2]	0		0		0		ns
t_{PD}	Chip Deselection to Power Down Time[2]		100[4]		100[4]		100[4]	ns
t_{AVEL}	Address Valid to Chip Enable Low	0		0		0		ns
t_{GLQV}	Chip Select Low to Output Valid[3]	10	90[4]	10	90[4]	10	90[4]	ns
t_{GHQZ}	Chip Select High to Output High Z	10	70[4]	10	70[4]	10	70[4]	ns

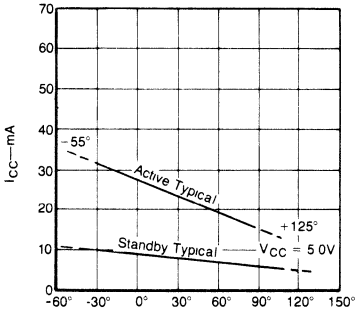
Notes
1. Test Conditions:
   Output Load· 2 TTL Loads and 100 pF, Input Transition Time: 20 ns, Timing Reference Levels Input· 1.5V, Output· 0.8V, 2.0V.
2. Mask programmed for chip enable with power down standby mode.
3. Mask programmed for chip enable without power down standby mode
4. Add 20 ns for extended temperature devices (−40°C to +85°C).
5. $\overline{G}$ may be delayed up to $t_{AVQV} - t_{GLQV}$ after the falling edge of $\overline{E}$ without impact on t_{AVQV}. Data is available at the Q outputs after a delay of t_{GLQV} from the falling edge of $\overline{G}$, provided that $\overline{E}$ has been low (V_{IL}) and addresses have been valid for at least $t_{AVQV} - t_{GLQV}$.
6. t_{GHQZ} and t_{EHQZ} are specified from $\overline{G}$ or $\overline{E}$, whichever occurs first

TIMING DIAGRAMS



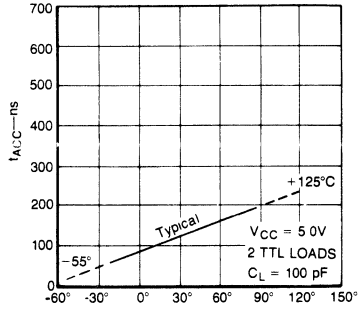
TYPICAL CHARACTERISTICS

SUPPLY CURRENT VS AMBIENT TEMPERATURE



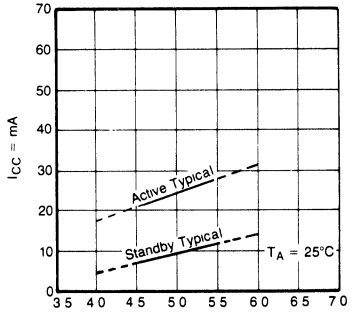
T_A—Ambient Temperature—°C

ACCESS TIME VS AMBIENT TEMPERATURE



T_A—Ambient Temperature—°C

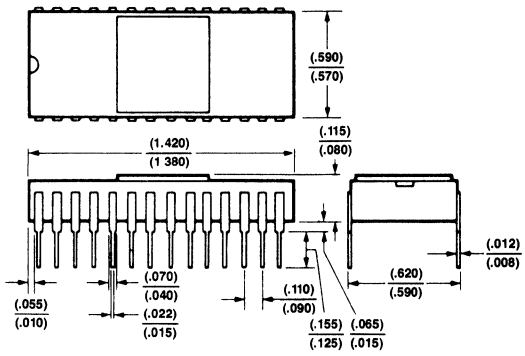
SUPPLY CURRENT VS SUPPLY VOLTAGE



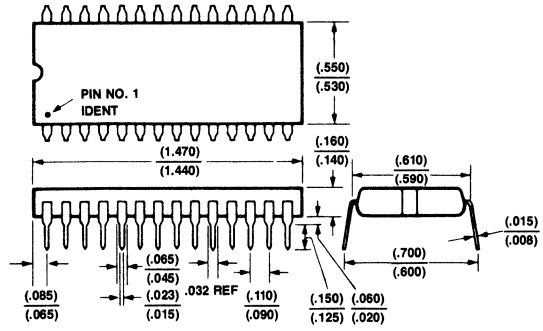
V_{CC}—Volts

PACKAGE DIMENSIONS

28-PIN CERAMIC DIP



28-PIN PLASTIC DIP



R23C64
64K (8K × 8) CMOS ROM

PRELIMINARY

DESCRIPTION

The Rockwell R23C64 is an 8K × 8 (65,536 bits) CMOS read-on-memory (ROM) housed in a 28-pin JEDEC standard package. It is fabricated in CMOS technology to achieve high performance with extremely low power dissipation. This device is available with maximum access times of 150, 250, or 300 nanoseconds, latched or non-latched chip selects, optional extended temperature range, and packaged in ceramic or low-cost plastic.

The R23C64 is controlled via the chip enable ($\overline{E}$) and the mask programmable output enable (G/$\overline{G}$/N) and chip selects (S1/$\overline{S1}$/N and S2/$\overline{S2}$N). The address is latched on the falling edge of $\overline{E}$, allowing the R23C64 to operate on a multiplexed bus as well as a non-multiplexed bus. The output enable and chip selects control the output buffers, however, these buffers do not become active until valid data is present from the internal data latches. This prevents spurious, invalid outputs that increase power dissipation. When $\overline{E}$ is high, the output buffers are in the high impedance state and the address, output enable and chip select pins are ignored (standby). $\overline{E}$ may also be held low indefinitely, keeping the address latched and the output buffers under output enable and chip select control. The R23C64 is in a low-power quiescient active mode when $\overline{E}$ is low and the other control inputs (G, S1 and S2) are steady state.

FEATURES

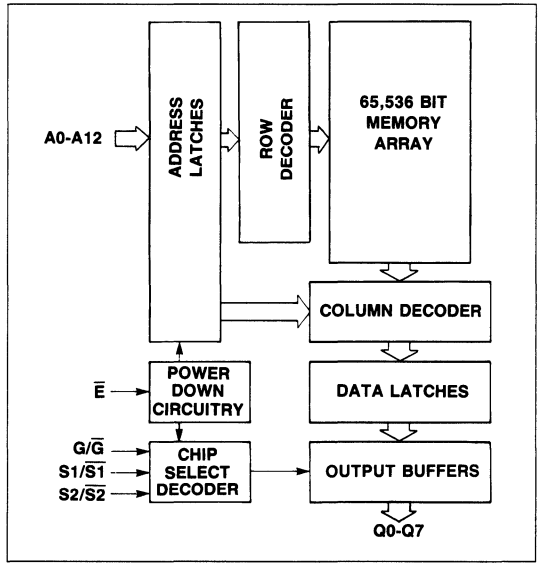
- 8,192 × 8 organization
- JEDEC standard pinout
- Extremely low power
  - — Active 10 mW/MHz (max.)
  - — Active quiescent 50 μW (max.)
  - — Standby 50 μW (max.)
- Fast access times: 150 ns, 250 ns and 300 ns (max.)
- Mask programmable chip selects and output enable
- Latched addresses and (optional) latched chip selects
- Drives two TTL loads and 100 pF
- Single 5V ± 10% power supply
- Pin compatible with Mostek MK37000

ORDERING INFORMATION

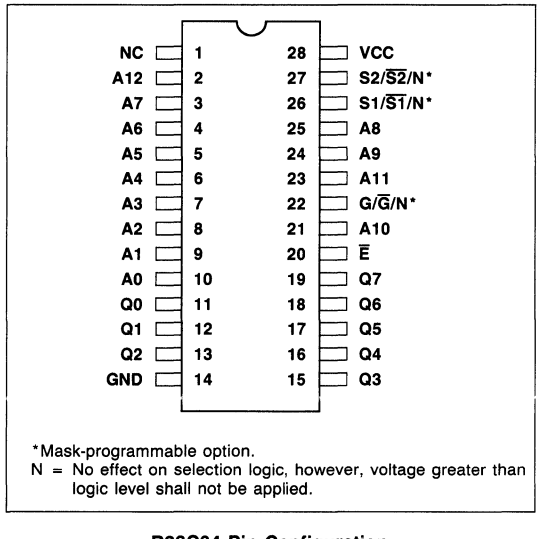
Part Number: R23C64 _ _ _ _

- Package:
  - C = Ceramic
  - P = Plastic
- Temperature Range:
  - No letter = 0°C to +70°C
  - E = −40°C to +85°C
- Access Time (Max):
  - 15 = 150 ns
  - 25 = 250 ns
  - 3 = 300 ns

Note: Submit ROM codes using Rockwell ROM Code Order Form, Order No. 2137.



R23C64 Block Diagram



*Mask-programmable option.
N = No effect on selection logic, however, voltage greater than logic level shall not be applied.

R23C64 Pin Configuration

4

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to +7.0	Vdc
Input Voltage	V_{IN}	−0.3 to V_{CC} +0.3	Vdc
Output Voltage	V_{OUT}	−0.3 to V_{CC} +0.3	Vdc
Temperature Under Bias Commercial Industrial	T_A	 −10 to +80 −50 to +95	°C
Storage Temperature	T_{STG}	−55 to +150	°C
Power Dissipation	P	1.0	W

***NOTE**: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

V_{CC} = 5.0V ±10%, T_A = 0°C to 70°C (unless otherwise specified)

Symbol	Parameter	Min	Typ[3]	Max	Units	Test Conditions
V_{OH}	Output High Voltage	2.4		V_{CC}	V	V_{CC} = 4.5V, I_{OH} = −200 μA
V_{OL}	Output Low Voltage			0.4	V	V_{CC} = 4.5V, I_{OL} = 3.2 mA
V_{IH}	Input High Voltage	2.0		V_{CC}	V	
V_{IL}	Input Low Voltage	−0.3		0.8	V	
I_{LI}	Input Load Current			±1	μA	V_{CC} = 5.5V, 0V < V_{IN} < 5.5V
I_{LO}	Output Leakage Current			±10	μA	V_{CC} = 5.5V, chip deselected, V_{OUT} = +0.4V to V_{CC}
I_{CC1}	Power Supply Current, Active			2	mA	t_{ELQV} = 150 ns[1], V_{CC} = 5.5V
I_{CC2}	Power Supply Current, Standby			10	μA	$\overline{E}$ = V_{CC} −0.5V; all other pins active
I_{CC3}	Power Supply Current, Active Quiescent			10	μA	E = V_{IL} $\overline{G}$ = $\overline{S1}$ = $\overline{S2}$ = Steady State (V_{IL} or V_{IH})
C_I	Input Capacitance (all but $\overline{E}$)[2] ($\overline{E}$)			7 10	pF pF	V_{CC} = 5.0V, chip deselected, pin under test at 0V, T_A = 25°C, f = 1 MHZ
C_O	Output Capacitance[2]			10	pF	

Notes:
1. t_{ELEH} = 150 ns, all pins active, no loads, 1 μs cycle time (t_{ELEL} = 1 μs).
2. This parameter is periodically sampled and is not 100% tested.
3. Typical values are for T_A = 25°C and V_{CC} = 5.0V.

AC CHARACTERISTICS

V_{CC} = 5.0V ± 10%, T_A = 0°C to 70°C (unless otherwise specified)

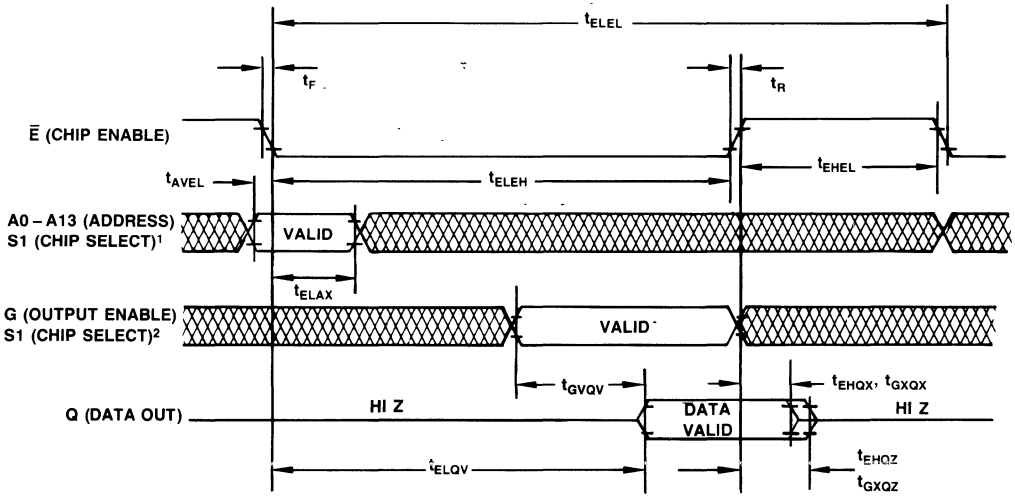
Symbol	Parameter	R23C64-15		R23C64-25		R23C64-3		Unit
		Min	Max	Min	Max	Min	Max	
t_{ELEL}	Cycle Time	220		365		465		ns
t_{ELEH}	Chip Enable Low to Chip Enable High	150		250		300		ns
t_{EHEL}	Chip Enable High to Chip Enable Low	60		100		150		ns
t_{ELQV}	Chip Enable Low to Output Valid (Access)		150		250		300	ns
t_{AVEL}	Address Setup Time	0		0		0		ns
t_{ELAX}	Address Hold Time	50		65		80		ns
t_{GVQV}	Output Enable Valid to Output Valid	75		100		150		ns
t_{EHQX}	Chip Enable High to Output Invalid	10		10		10		ns
t_{GXQX}	Output Enable Invalid to Output Invalid	10		10		10		ns
t_{EHQZ}[4]	Chip Enable High to Output High Z		50		65		70	ns
t_{GXQZ}[4]	Output Enable Invalid to Output High Z		60		75		90	ns
t_F, t_R	Rise and Fall Times[2]		10		15		20	ns

Notes:
1. Test Conditions Output Load: 2 TTL Loads and 100 pF; Input Transition Time. 20 ns; Timing Reference Levels: Input 1 5V, Output 0 8V, 2 0V
2. Rise and Fall times stated are required for these high performance parameters only and may be relaxed for slower operation, e g , 100 kHz operation.
3. $\overline{G}$ may be delayed up to $t_{AVQV} - t_{GLQV}$ after the falling edge of $\overline{E}$ without impact on t_{AVQV}. Data is available at the Q outputs after a delay of t_{GLQV} from the falling edge of $\overline{G}$, provided that $\overline{E}$ has been low (V_{IL}) and addresses have been valid for at least $t_{AVQV} - t_{GLQV}$.
4. t_{EHQZ}, t_{GHQZ} are specified from $\overline{G}$ or $\overline{E}$, whichever occurs first.

4

TIMING DIAGRAM

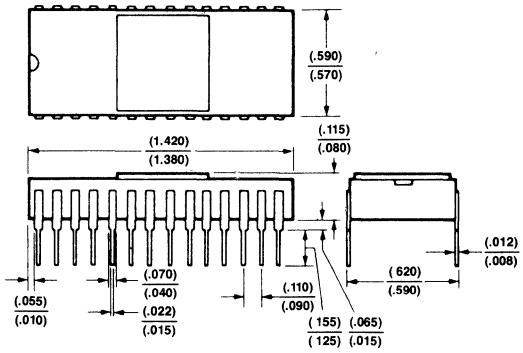
READ CYCLE TIMING



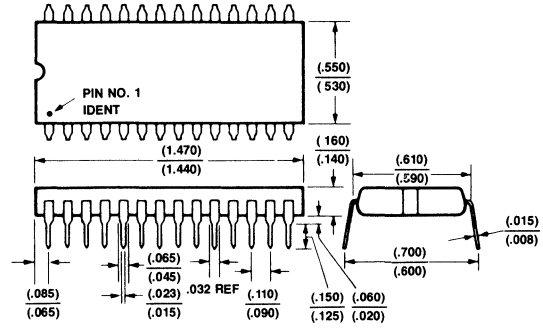
NOTES:
1. **CHIP SELECTS (S1/$\overline{S1}$ AND S2/$\overline{S2}$) LATCHED.**
2. **CHIP SELECTS (S1/$\overline{S1}$ AND S2/$\overline{S2}$) NOT LATCHED.**

PACKAGE DIMENSIONS

28-PIN CERAMIC DIP



28-PIN PLASTIC DIP



Rockwell

R23128
128K (16K × 8) STATIC ROM

DESCRIPTION

The R23128-25 and R23128-3 are 131,072-bit static Read-Only Memories (ROMs), organized as 16,384 eight-bit bytes, that offer maximum access times of 250 and 300 nanoseconds, respectively. These ROMs are in industry-standard 28-pin, dual in-line packages, and are available in ceramic or low-cost plastic. These fully-static 128K-bit ROMs are compatible with industry standard microprocessors.

The R23128 ROMs operate totally asynchronously, and require no clock input. The mask-programmable chip select (S1/$\overline{S1}$) input allows two 128K ROMs to be OR-tied without external decoding. These devices provides tri-state output buffers for memory expansion. The R23128 ROMs offer TTL input and output levels with a minimum noise immunity of 0.4 volts.

The chip enable input ($\overline{E}$) functions as a chip enable with power down standby mode. When this line is high the chip is disabled and enters a low power standby state.

FEATURES

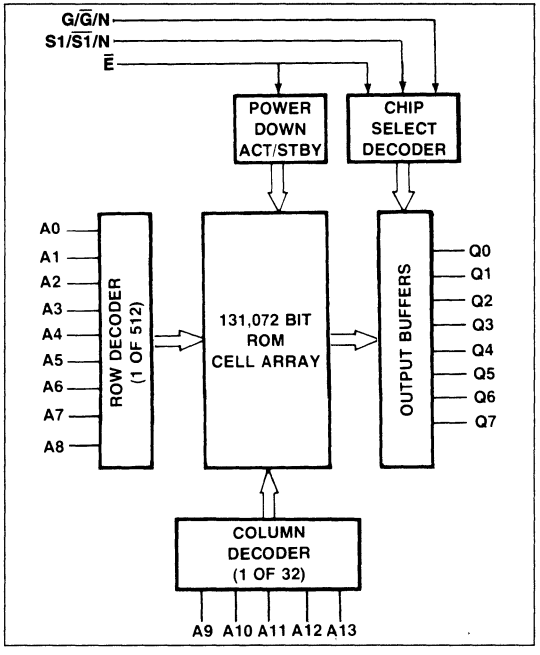
- 16,384 × 8 organization bytes
- Access time: 250 ns and 300 ns (max.)
- Low typical power dissipation is 100 mW active, 20 mW standby
- Drives two TTL loads and 100 pF
- Single +5V ± 10% power supply
- Totally static operation, no input clock required
- Completely TTL compatible
- Three mask-programmable chip select inputs
- Tri-state outputs for memory expansion

ORDERING INFORMATION

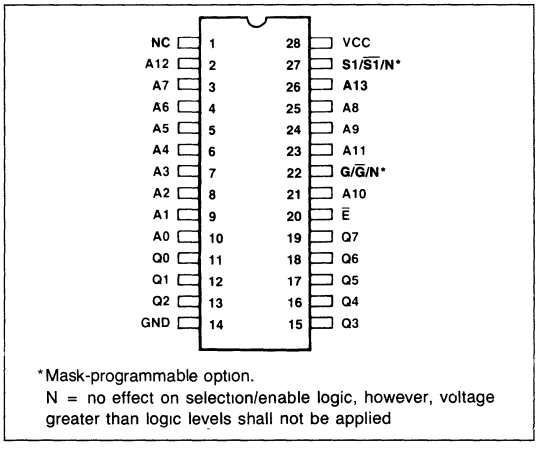
Part Number: R23128 _ _ – – –

- Package:
  - C = Ceramic
  - P = Plastic
- Temperature Range:
  - No letter = 0°C to +70°C
  - E = −40°C to +85°C
- Access Time (Max):
  - 25 = 250 ns
  - 3 = 300 ns

Note: Submit ROM codes using Rockwell ROM Code Order Form, Order No 2137



R23128 Block Diagram



*Mask-programmable option.
N = no effect on selection/enable logic, however, voltage greater than logic levels shall not be applied

R23128 Pin Configuration

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.5 to +7.0	Vdc
Input Voltage	V_{IN}	−0.5 to +7.0	Vdc
Output Voltage	V_{OUT}	−0.5 to +7.0	Vdc
Temperature under Bias Commercial Industrial	T_A	 −10 to +80 −50 to +95	°C
Storage Temperature	T_{STG}	−65 to +150	°C
Power Dissipation	P	1.0	W

***NOTE:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

V_{CC} = 5.0V ± 10%, T_A = 0°C to 70°C (unless otherwise specified)

Symbol	Parameter	Min	Typ[2]	Max	Units	Test Conditions
V_{OH}	Output HIGH Voltage	2.4		V_{CC}	V	V_{CC} = 4.5V, I_{OH} = −400 μA
V_{OL}	Output LOW Voltage			0.4	V	V_{CC} = 4.5V, I_{OL} = 3.3 mA
V_{IH}	Input HIGH Voltage	2.0		V_{CC}	V	
V_{IL}	Input LOW Voltage	−0.5		0.8	V	
I_{LI}	Input Load Current			10	μA	V_{CC} = 5.5V, 0V ≤ V_{IN} ≤ 5 5V
I_{LO}	Output Leakage Current			±10	μA	V_{CC} = 5 5V, chip deselected V_{OUT} = +0.4V to V_{CC}
I_{CC}	Power Supply Current, Active		20	55	mA	V_{CC} = 5.5V
I_{SB}	Power Supply Current, Standby		7.5	16	mA	
C_I	Input Capacitance[1]			7	pF	V_{CC} = 5.0V, chip deselected, pin under test at 0V, T_A = 25°C f = 1 MHz
C_O	Output Capacitance[1]			10	pF	

Note:
1. This parameter is periodically sampled and is not 100% tested.
2. Typical values are for T_A = 25°C and V_{CC} = 5.0V

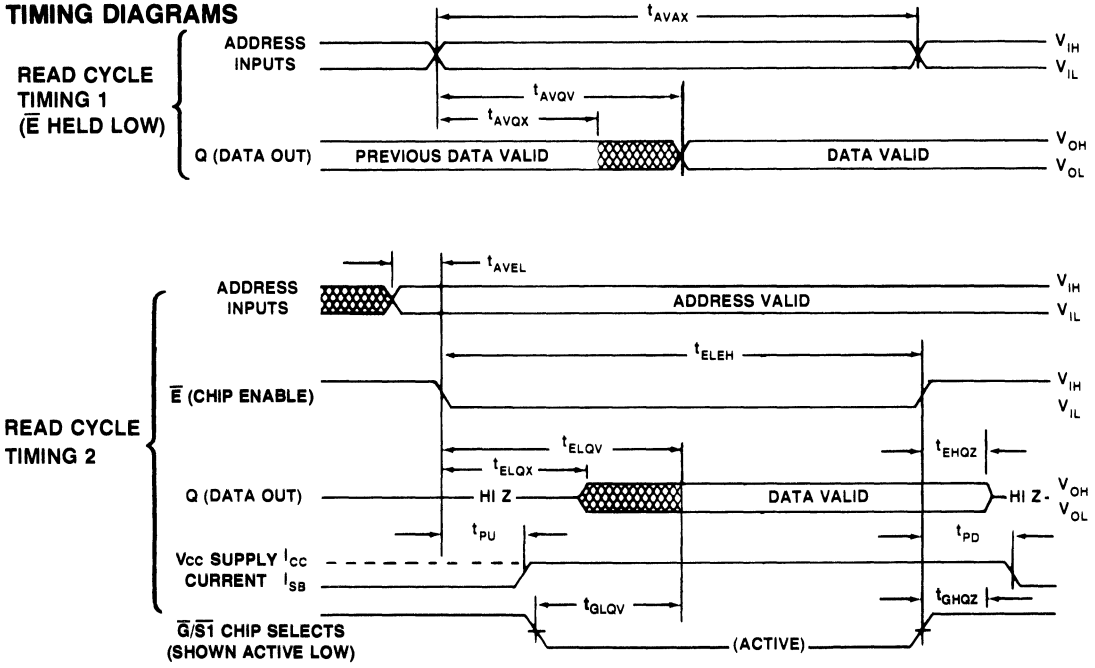
AC CHARACTERISTICS

V_{CC} = 5.0V ± 10%, T_A = 0°C to 70°C (unless otherwise specified)

Symbol	Parameter	R23128-25		R23128-3		Units
		Min	Max	Min	Max	
t_{AVAX}	Address Valid to Address Don't Care	250		300		ns
t_{ELEH}	Chip Enable Low to Chip Enable High	250		300		ns
t_{AVQV}	Address Valid to Output Valid (t_{ACC}) (Access)		250		300	ns
t_{ELQV}	Chip Enable Low to Output Valid (Access)		250		300	ns
t_{AVQX}	Address Valid to Output (t_{OH}) Invalid	10		10		ns
t_{ELQX}	Chip Enable Low to Output (t_{CO}) Invalid	10		10		ns
t_{EHQZ}	Chip Enable High to Output High Z (t_{DF})	10	70	10	70	ns
t_{PU}	Chip Selection to Power Up Time	0		0		ns
t_{PD}	Chip Deselection to Power Down Time		100		100	ns
t_{AVEL}	Address Valid to Chip Enable Low	0		0		ns
t_{GLQV}	Chip Select Low to Output Valid	10	90[2]	10	90[2]	ns
t_{GHQZ}	Chip Select High to Output High Z	10	70[2]	10	70[2]	ns

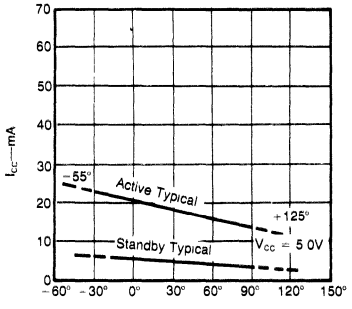
Notes:
1. Test Conditions:
   Output load 2 TTL loads and 100 pF
   Input transition time: 20 ns
   Timing reference levels: Input: 1.5V; Output: 0.8V, 2.0V
2. Add 20 ns for extended temperature devices (−40°C to +85°C)
3. $\overline{G}$ may be delayed up to t_{AVQV}−t_{GLQV} after the falling edge of $\overline{E}$ without impact on t_{AVQV}. Data is available at the Q outputs after a delay of t_{GLQV} from the falling edge of $\overline{G}$, provided that $\overline{E}$ has been low (V_{IL}) and addresses have been valid for at least t_{AVQV}−t_{GLQV}
4. t_{GHQZ} and t_{EHQZ} are specified from $\overline{G}$ or $\overline{E}$, whichever occurs first.

TIMING DIAGRAMS



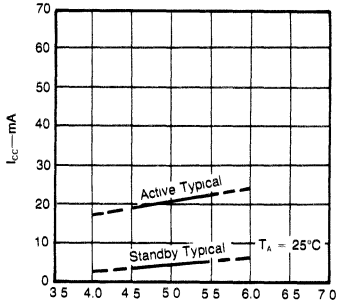
TYPICAL CHARACTERISTICS

SUPPLY CURRENT VS AMBIENT TEMPERATURE



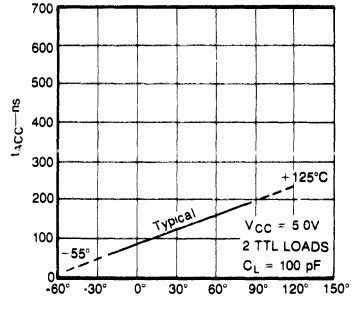
TA—Ambient Temperature—°C

SUPPLY CURRENT VS SUPPLY VOLTAGE



VCC—Volts

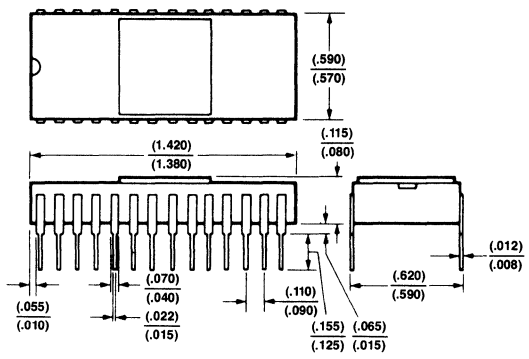
ACCESS TIME VS AMBIENT TEMPERATURE



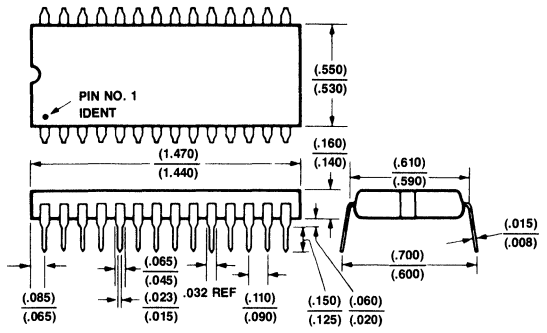
TA—Ambient Temperature—°C

PACKAGE DIMENSIONS

28-PIN CERAMIC DIP



28-PIN PLASTIC DIP



Rockwell

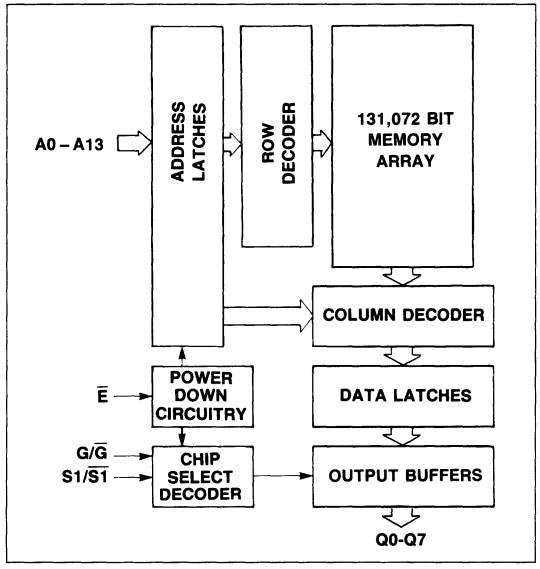
R23C128
128K (16K × 8) CMOS ROM

PRELIMINARY

DESCRIPTION

The Rockwell R23C128 is a 16K × 8 (131,072 bits) CMOS read-only-memory (ROM) housed in a 28-pin JEDEC standard package. It is fabricated in CMOS technology to achieve high performance with extremely low power dissipation. This device is available with maximum access times of 150, 250, or 300 nanoseconds, latched or non-latched chip select, optional extended temperature range, and packaged in ceramic or low-cost plastic.

The R23C128 is controlled via the chip enable ($\overline{E}$) and the mask programmable output enable (G/$\overline{G}$/N) and chip select (S1/$\overline{S1}$/N). The address is latched on the falling edge of $\overline{E}$, allowing the R23C128 to operate on a multiplexed bus as well as a non-multiplexed bus. The output enable and chip select control the output buffers, however, these buffers do not become active until valid data is present from the internal data latches. This prevents spurious, invalid outputs that increase power dissipation. When $\overline{E}$ is high, the output buffers are in the high impedance state and the address, output enable and chip select pins are ignored (standby). $\overline{E}$ may also be held low indefinitely, keeping the address latched and the output buffers under output enable and chip select control. The R23C128 is in a low-power quiescent active mode when $\overline{E}$ is low and the other control inputs (G and S1) are steady state.



R23C128 Block Diagram

FEATURES

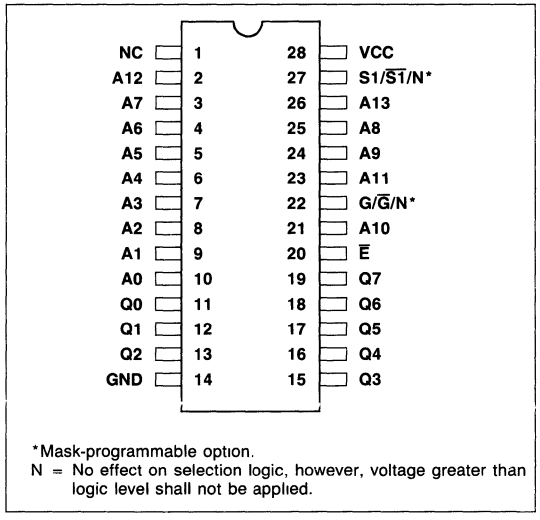
- 16,384 × 8 organization
- JEDEC standard pinout
- Extremely low power
  - — Active 15 mW/MHz (max.)
  - — Active quiescent 50 μW (max.)
  - — Standby 50 μW (max.)
- Fast access times: 150 ns, 250 ns and 300 ns (max.)
- Mask programmable chip select and output enable
- Latched addresses and (optional) latched chip select
- Drives two TTL loads and 100 pF
- Single 5V ± 10% power supply

ORDERING INFORMATION

Part Number: R23C128 _ _ _ _

- Package
  - C = Ceramic
  - P = Plastic
- Temperature Range
  - No letter = 0°C to +70°C
  - E = −40°C to +85°C
- Access Time (Max).
  - 15 = 150 ns
  - 25 = 250 ns
  - 3 = 300 ns

Note: Submit ROM codes using Rockwell ROM Code Order Form, Order No. 2137



*Mask-programmable option.
N = No effect on selection logic, however, voltage greater than logic level shall not be applied.

R23C128 Pin Configuration

4

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to +7.0	Vdc
Input Voltage	V_{IN}	−0.3 to V_{CC} +0.3	Vdc
Output Voltage	V_{OUT}	−0.3 to V_{CC} +0.3	Vdc
Temperature Under Bias Commercial Industrial	T_A	 −10 to +80 −50 to +95	°C
Storage Temperature	T_{STG}	−55 to +150	°C
Power Dissipation	P	1.0	W

***NOTE:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

V_{CC} = 5.0V ±10%, T_A = 0°C to 70°C (unless otherwise specified)

Symbol	Parameter	Min	Typ[3]	Max	Units	Test Conditions
V_{OH}	Output High Voltage	2.4		V_{CC}	V	V_{CC} = 4.5V, I_{OH} = −200 μA
V_{OL}	Output Low Voltage			0.4	V	V_{CC} = 4.5V, I_{OL} = 3.2 mA
V_{IH}	Input High Voltage	2.0		V_{CC}	V	
V_{IL}	Input Low Voltage	−0.3		0.8	V	
I_{LI}	Input Load Current			±1	μA	V_{CC} = 5.5V, 0V < V_{IN} < 5.5V
I_{LO}	Output Leakage Current			±10	μA	V_{CC} = 5.5V, chip deselected, V_{OUT} = +0.4V to V_{CC}
I_{CC1}	Power Supply Current, Active			3	mA	t_{ELQV} = 150 ns[1], V_{CC} = 5.5V
I_{CC2}	Power Supply Current, Standby			10	μA	$\overline{E}$ = V_{CC} −0.5V; all other pins active
I_{CC3}	Power Supply Current, Active Quiescent			10	μA	$\overline{E}$ = V_{IL} $\overline{G}$ = $\overline{S1}$ = Steady State (V_{IL} or V_{IH})
C_I	Input Capacitance (all but $\overline{E}$)[2] ($\overline{E}$)			7 10	pF pF	V_{CC} = 5.0V, chip deselected, pin under test at 0V, T_A = 25°C, f = 1 MHZ
C_O	Output Capacitance[2]			10	pF	

Notes:
1. t_{ELEH} = 150 ns, all pins active, no loads, 1 μs cycle time (t_{ELEL} = 1 μs).
2. This parameter is periodically sampled and is not 100% tested.
3. Typical values are for T_A = 25°C and V_{CC} = 5.0V.

AC CHARACTERISTICS

V_{CC} = 5.0V ± 10%, T_A = 0°C to 70°C (unless otherwise specified)

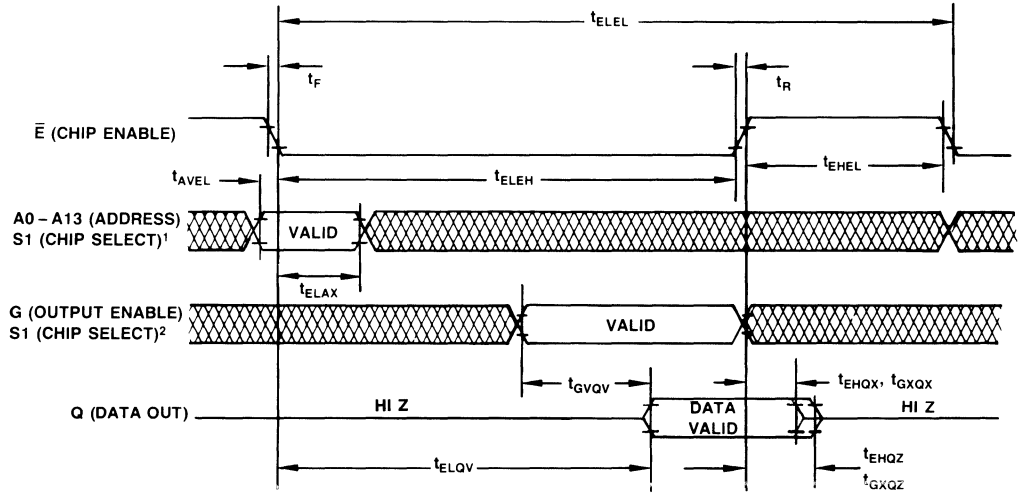
Symbol	Parameter	R23C128-15		R23C128-25		R23C128-3		Unit
		Min	Max	Min	Max	Min	Max	
t_{ELEL}	Cycle Time	220		365		465		ns
t_{ELEH}	Chip Enable Low to Chip Enable High	150		250		300		ns
t_{EHEL}	Chip Enable High to Chip Enable Low	60		100		150		ns
t_{ELQV}	Chip Enable Low to Output Valid (Access)		150		250		300	ns
t_{AVEL}	Address Setup Time	0		0		0		ns
t_{ELAX}	Address Hold Time	50		65		80		ns
t_{GVQV}	Output Enable Valid to Output Valid	75		100		150		ns
t_{EHQX}	Chip Enable High to Output Invalid	10		10		10		ns
t_{GXQX}	Output Enable Invalid to Output Invalid	10		10		10		ns
t_{EHQZ}[4]	Chip Enable High to Output High Z		50		60		70	ns
t_{GXQZ}[4]	Output Enable Invalid to Output High Z		60		75		90	ns
t_F, t_R	Rise and Fall Times[2]		10		15		20	ns

Notes:
1. Test Conditions: Output Load: 2 TTL Loads and 100 pF, Input Transition Time: 20 ns, Timing Reference Levels: Input: 1.5V; Output: 0.8V, 2.0V.
2. Rise and Fall times stated are required for these high performance parameters only and may be relaxed for slower operation, e.g., 100 kHz operation.
3. $\overline{G}$ may be delayed up to $t_{AVQV} - t_{GLQV}$ after the falling edge of $\overline{E}$ without impact on t_{AVQV}. Data is available at the Q outputs after a delay of t_{GLQV} from the falling edge of $\overline{G}$, provided that $\overline{E}$ has been low (V_{IL}) and addresses have been valid for at least $t_{AVQV} - t_{GLQV}$.
4. t_{EHQZ}, t_{GHQZ} are specified from $\overline{G}$ or $\overline{E}$, whichever occurs first.

4

TIMING DIAGRAM

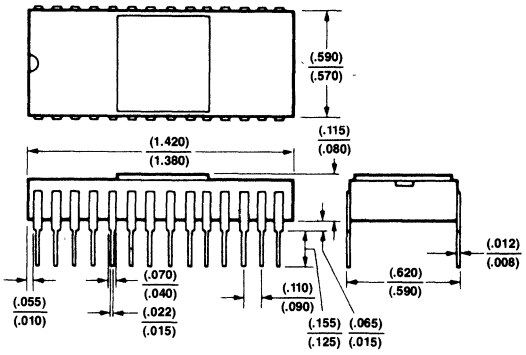
READ CYCLE TIMING



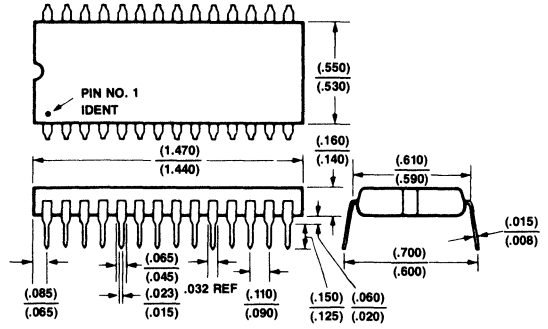
NOTES:
1. **CHIP SELECT (S1/$\overline{S1}$) LATCHED.**
2. **CHIP SELECT (S1/$\overline{S1}$) NOT LATCHED.**

PACKAGE DIMENSIONS

28-PIN CERAMIC DIP



28-PIN PLASTIC DIP



R23256 AND R23257
256K (32K × 8) STATIC ROMS

PRELIMINARY

DESCRIPTION

The R23256 and R23257 are 262,144-bit static Read-Only Memories (ROMs), organized as 32,768 eight-bit bytes, that offer maximum access times of 200 nanoseconds. These ROMs are in industry-standard 28-pin, dual in-line packages, and are available in ceramic or low-cost plastic. These fully-static 256K-bit ROMs are compatible with industry standard microprocessors and are designed for installation in systems requiring high-performance large-capacity storage and simple interfacing.

The R23256 and R23257 ROMs operate totally asynchronously, and require no clock input. These ROMs offer TTL input and output levels with a minimum noise immunity of 0.4 volts. The R23256 has a Chip Select (S1/$\overline{S1}$) input which allows two of these ROMs to be wire-ORed without external decoding. The R23256 also has an Output Enable (G/$\overline{G}$) input to eliminate bus contention in multiple-bus systems. The R23256 has two Chip Select (S1/$\overline{S1}$ and S2/$\overline{S2}$) inputs which allow up to four of these ROMs to be wire-ORed without external decoding.

The chip enable input ($\overline{E}$) functions as a chip enable with power down standby mode. When this line is high the chip is disabled and enters a low power standby state.

The R23256 is pin compatible with the 2764 EPROM and the R23257 is pin compatible with the 2564 EPROM, which eliminates the need to redesign printed circuit boards for volume mask programmable ROMs after prototyping with EPROMs.

FEATURES

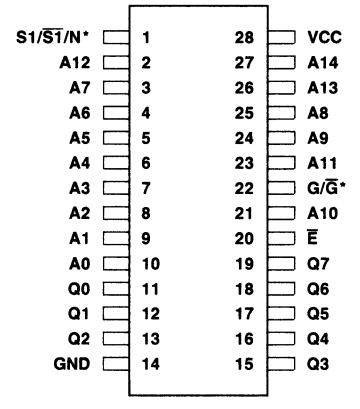
- 32,768 × 8 organization
- Access times: 200 ns, 250 ns, and 450 ns (max)
- Low max. power dissipation: 400 mW (active), 100 mW (standby)
- Drives two TTL loads and 100 pF
- Single +5V ±10% power supply
- Totally static operation, no input clock required
- Completely TTL compatible
- Mask-programmable chip select/output enable lines
- Tri-state outputs for memory expansion
- R23256 pin compatible with 2764 EPROM
- R23257 pin compatible with 2564 EPROM

ORDERING INFORMATION

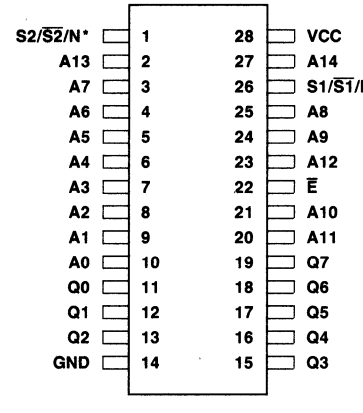
Part Number: R23256 ____
R23257 ____

- Package:
  - C = Ceramic
  - P = Plastic
- Temperature Range:
  - No letter = 0°C to +70°C
  - E = −40°C to +85°C
- Access Time (Max):
  - 20 = 200 ns
  - 25 = 250 ns
  - 45 = 450 ns

Note: Submit ROM codes using Rockwell ROM Code Order Form, Order No. 2137.



R23256



R23257

*Mask-programmable option.
N = No effect on selection logic, however, voltage greater than logic level shall not be applied.

R23256 and R23257 Pin Configurations

4

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.5 to +7.0	Vdc
Input Voltage	V_{IN}	−0.5 to +7.0	Vdc
Output Voltage	V_{OUT}	−0.5 to +7.0	Vdc
Temperature under Bias Commercial Industrial	T_A	 −10 to +80 −50 to +95	°C
Storage Temperature	T_{STG}	−65 to +150	°C
Power Dissipation	P	1.0	W

***NOTE**: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

V_{CC} = 5.0V ±10%, T_A = 0°C to 70°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ	Max	Units	Test Conditions
V_{OH}	Output HIGH Voltage	2.4		V_{CC}	V	V_{CC} = 4.5V, I_{OH} = −1.0 mA
V_{OL}	Output LOW Voltage			0.4	V	V_{CC} = 4.5V, I_{OL} = 3.2 mA
V_{IH}	Input HIGH Voltage	2.0		V_{CC}	V	
V_{IL}	Input LOW Voltage	−0.5		0.8	V	
I_{LI}	Input Load Current			10	μA	V_{CC} = 5.5V, 0V ≤ V_{IN} ≤ 5.5V
I_{LO}	Output Leakage Current			±10	μA	V_{CC} = 5.5V, chip deselected, V_{OUT} = +0.4V to V_{CC}
I_{CC}	Power Supply Current, Active			80	mA	V_{CC} = 5.5V
I_{SB}	Power Supply Current, Standby			20	mA	$\overline{E}$ = V_{IH}
C_I	Input Capacitance[1]			7	pF	V_{CC} = 5.0V, chip deselected, pin under test at 0V, T_A = 25°C f = 1 MHz.
C_O	Output Capacitance[1]			10	pF	

Notes:
1. This parameter is periodically sampled and is not 100% tested.

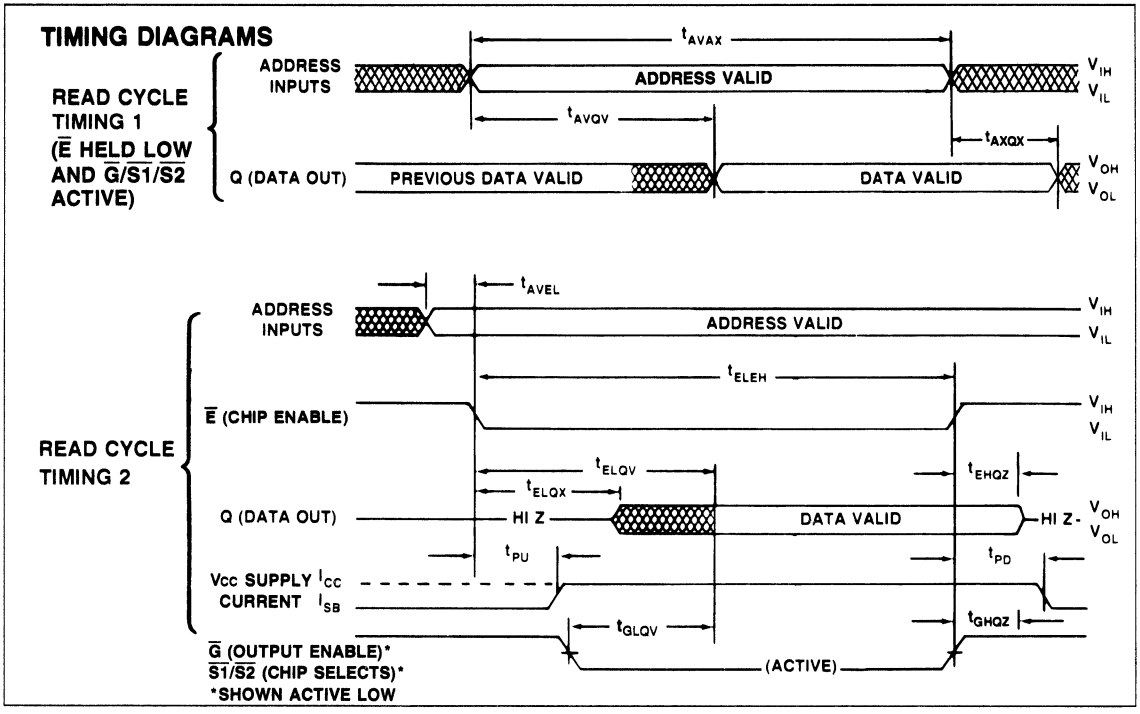
AC CHARACTERISTICS

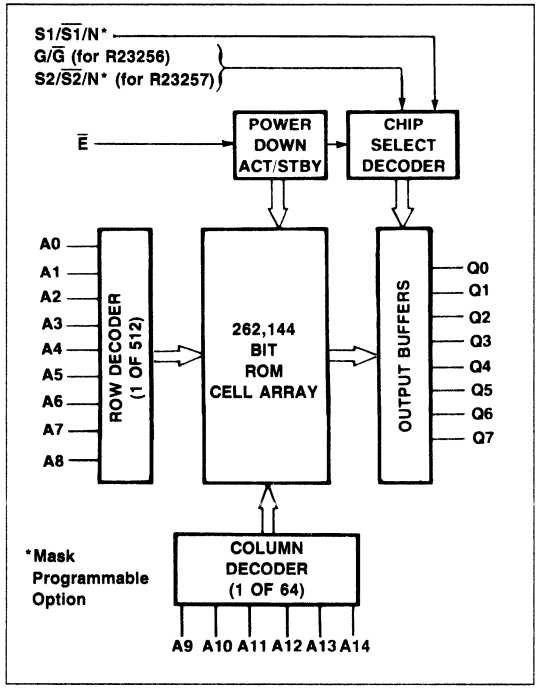
V_{CC} = 5.0V ± 10%, T_A = 0°C to 70°C (unless otherwise specified)

		R23256-20 R23257-20		R23256-25 R23257-25		R23256-45 R23257-45		
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Units
t_{AVAX}	Address Valid to Address Don't Care	200		250		450		ns
t_{ELEH}	Chip Enable Low to Chip Enable High	200		250		450		ns
t_{AVQV}	Address Valid to Output Valid (t_{ACC})(Access)		200		250		450	ns
t_{ELQV}	Chip Enable Low to Output Valid (Access)		200		250		450	ns
t_{AXQX}	Address Change to Output Invalid (t_{OH})	10		10		10		ns
t_{ELQX}	Chip Enable Low to Output Active (t_{CO})	10		10		10		ns
t_{EHQZ}	Chip Enable High to Output High Z (t_{DF})		85		100		150	ns
t_{PU}	Chip Selection to Power Up Time	0		0		0		ns
t_{PD}	Chip Deselection to Power Down Time		85		100		150	ns
t_{AVEL}	Address Setup to Chip Enable Low	0		0		0		ns
t_{GLQV}	Output Enable Low to Output Valid	10	85	10	100	10	150	ns
t_{GHQZ}	Output Enable High to Output High Z		85		100		150	ns

Notes:
1. Test Conditions: Output Load: 2 TTL loads and 100 pF; Input transition time: 20 ns; Timing reference levels: Input: 1.5V; Output: 0.8V, 2.0V
2. Add 20 ns for extended temperature devices (−40°C to +85°C).
3. $\overline{G}$ may be delayed up to $t_{AVQV} - t_{GLQV}$ after the falling edge of $\overline{E}$ without impact on t_{AVQV}. Data is available at the Q outputs after a delay of t_{GLQV} from the falling edge of $\overline{G}$, provided that $\overline{E}$ has been low (V_{IL}) and addresses have been valid for at least $t_{AVQV} - t_{GLQV}$.
4. t_{GHQZ} and t_{EHQZ} are specified from $\overline{G}$ or $\overline{E}$ whichever occurs first.

TIMING DIAGRAMS

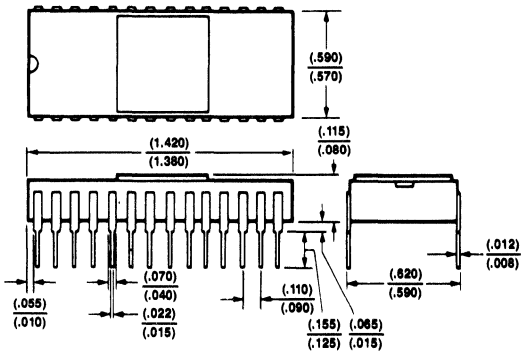




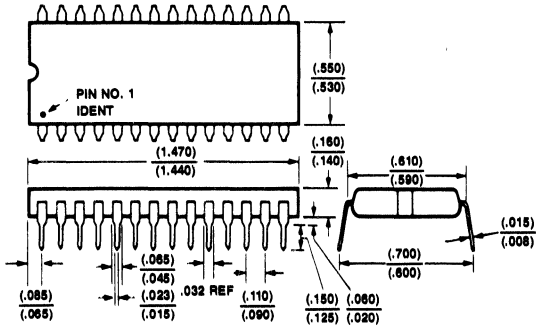
R23256 and R23257 Block Diagram

PACKAGE DIMENSIONS

28-PIN CERAMIC DIP



28-PIN PLASTIC DIP



R87C64
64K (8K × 8) CMOS UV EPROM

PRELIMINARY

DESCRIPTION

The Rockwell R87C64 is an 8K × 8 (65,536 bits) ultraviolet (UV) light erasable programmable read-only-memory (EPROM). It is manufactured using CMOS technology for low power dissipation in both active and standby operating modes.

Initially, and also after erasure, all bits are in the "1" state. Data is programmed by applying 21V to V_{PP} a TTL low to $\overline{E}$, and a 50 ms low pulse on $\overline{P}$ while the desired data is stable on DQ0-DQ7 lines and the address is stable on A0-A12 lines. All bits may be erased to the "1" state by exposure to a UV light source through the transparent window on the top of the device package.

The R87C64 EPROM is ideal for system development or production applications requiring non-volatile memory in either multiple chip or single chip microcomputers with extended bus configurations. The low power requirements especially support applications using the R65C00 CMOS Microcomputer device family.

FEATURES

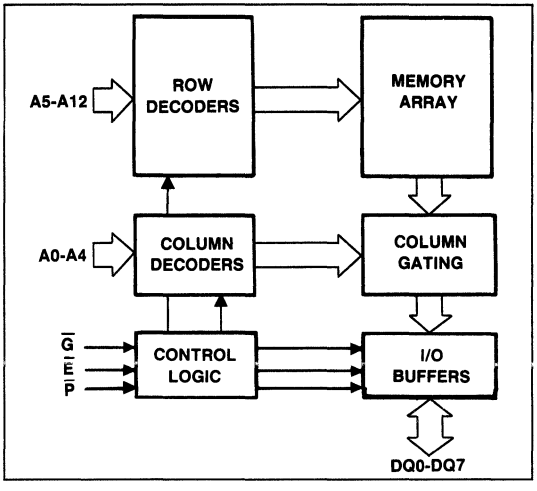
- 8,192 × 8 organization
- JEDEC approved pin-out
- Low Power
  —Active 75 mW (max.)
  —Standby 500 μW (max.)
- Access times: 250 ns, 300 ns and 350 ns (max.)
- Single 5V power supply
- Static operation, no clocks required
- TTL compatible inputs and tri-state outputs during both read and program mode
- Pin compatible with INTEL 2764A EPROM and Rockwell R23C64 and R2364B ROMs.

4

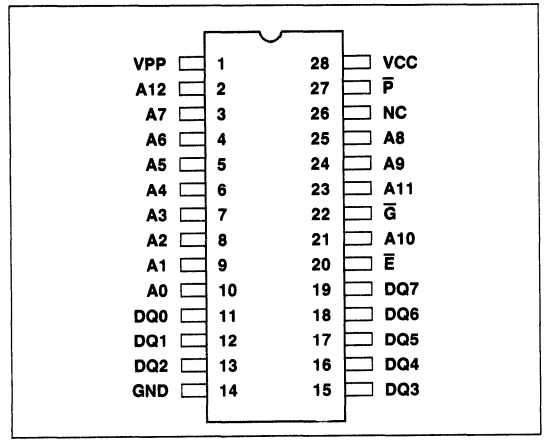
ORDERING INFORMATION

Part Number: R87C64 _ _

Access Time:
25 = 250 ns
30 = 300 ns
35 = 350 ns



R87C64 Block Diagram



R87C64 Pin Configuration

A0-A12	ADDRESSES
$\overline{E}$	CHIP ENABLE
$\overline{G}$	OUTPUT ENABLE
DQ0-DQ7	DATA INPUT/OUTPUT
$\overline{P}$	PROGRAM ENABLE

R87C64 Pin Names

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to +7.0	Vdc
Input Voltage All, except Vpp during Programming Vpp during Programming	V_{IN}	 −0.3 to V_{CC} +0.3 −0.3 to +22.0	Vdc
Output Voltage	V_{OUT}	−0.3 to V_{CC} +0.3	Vdc
Temperature under Bias	T_A	−10 to +80	°C
Storage Temperature	T_{STG}	−40 to +125	°C
Power Dissipation	P	1.0	W

***NOTE:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC OPERATING CHARACTERISTICS DURING READ

V_{CC} = 5.0V ±5%, T_A = 0°C to 70°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.[3]	Max.	Unit	Test Conditions
V_{OH}	Output High Voltage	2.4		—	V	I_{OH} = −400 μA
V_{OL}	Output Low Voltage	—		0.45	V	I_{OL} = 2.1 mA
V_{IH}	Input High Voltage	2.0		V_{CC} +0.3	V	
V_{IL}	Input Low Voltage	−0.1		0.8	V	
I_{CC1}	V_{CC} Standby Current		2	100	μA	$\overline{E}$ = V_{CC}, $\overline{G}$ = V_{IL}, V_{IN} = 0V or V_{CC}
I_{CC2}	V_{CC} Active Current		2	15	mA	$\overline{E}$ = $\overline{G}$ = V_{IL}, note 4
I_{PP}	V_{PP} Current			100	μA	V_{PP} = V_{CC} max.
I_{IN}	Input Leakage Current			±10	μA	V_{IN} = 0V to V_{CC}
I_O	Output Leakage Current			±10	μA	V_{OUT} = 0V to V_{CC}
C_I	Input Capacitance[2]			7	pF	V_{CC} = 5 0V, chip deselected, pin under test at 0V, T_A = 25°C f = 1 MHz
C_O	Output Capacitance[2]			10	pF	

Notes:
1. Applies only to chip enable with power down standby mode.
2. This parameter is periodically sampled and is not 100% tested.
3. Typical values are for T_A = 25°C and V_{CC} = 5.0V
4. Cycle Time = 1 μs, all pins active, no loads.

DC OPERATING CHARACTERISTICS DURING PROGRAMMING

V_{CC} = 5.0V ±5%, T_A = 20°C to 30°C, V_{PP} = 21.0V ±0.5V

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
V_{IH}	Input High Voltage	2.0		V_{CC} +0.3	V	
V_{IL}	Input Low Voltage	−0.1		0.8	V	
I_{CC}	V_{CC} Active Current			0.5	mA	$\overline{E}$ = $\overline{P}$ = V_{IL}, $\overline{G}$ = V_{IH}
I_{PP}	V_{PP} Active Current			30	mA	
I_{IN}	Input Leakage Current			10	μA	V_{IN} = 0V to V_{CC}

AC CHARACTERISTICS DURING READ

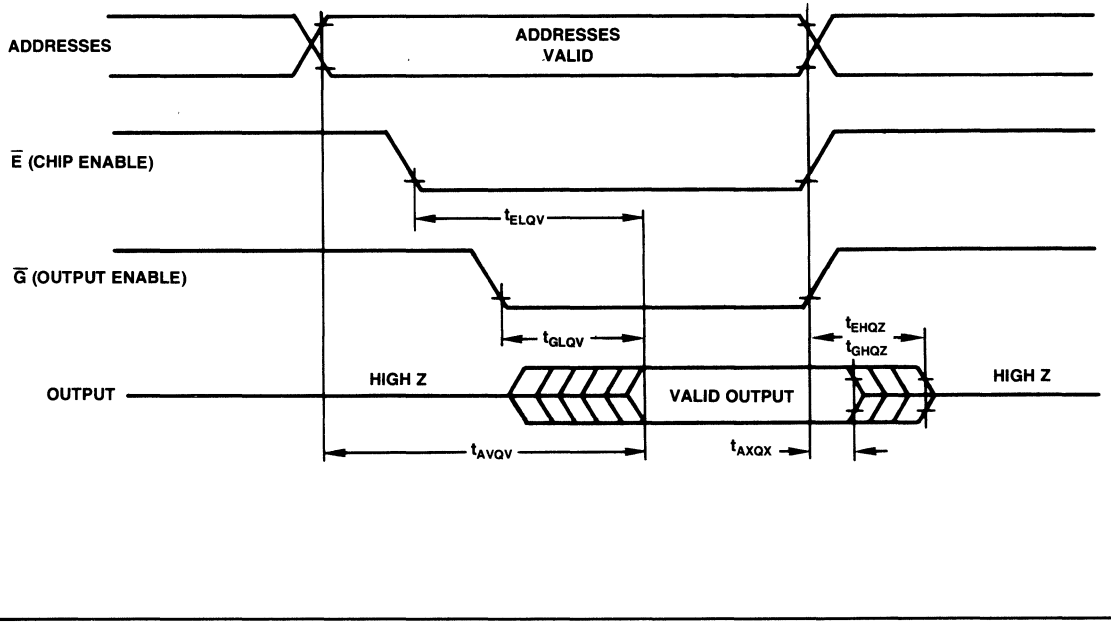
V_{CC} = 5.0V ± 5%, T_A = 0°C to 70°C (unless otherwise specified)

Symbol	Parameter	R87C64-25			R87C64-35			Unit	Test Conditions[3]
		Min.	Typ.	Max.	Min.	Typ.	Max.		
t_{AVQV}	Address to Data Valid			250			350	ns	$\overline{E} = \overline{G} = V_{IL}$
t_{ELQV}	Chip Enable to Data Valid			250			350	ns	$\overline{G} = V_{IL}$
t_{GLQV}[1]	Output Enable to Data Valid	10		100	10		120	ns	$\overline{E} = V_{IL}$
t_{GHQZ}[2]	Output Enable to High Impedance	0		90	0		100	ns	$\overline{E} = V_{IL}$
t_{AXQX}	Address to Output Hold	0			0			ns	$\overline{E} = \overline{G} = V_{IL}$
t_{EHQZ}	Chip Enable to High Impedance	0		90	0		100	ns	$\overline{G} = V_{IL}$

Notes:
1. $\overline{G}$ may be delayed up to $t_{AVQV}-t_{GLQV}$ after the falling edge of $\overline{E}$ without impact on t_{AVQV}. Data is available at the DQ outputs after a delay of t_{GLQV} from the falling edge of $\overline{G}$, provided that $\overline{E}$ has been low (V_{IL}) and addresses have been valid for at least $t_{AVQV}-t_{GLQV}$.
2. t_{GHQZ} and t_{EHQZ} are specified from $\overline{G}$ or $\overline{E}$, whichever occurs first.
3. Test Conditions:
   Output Load: 1 TTL gate and C_L = 100 pF
   Input Rise and Fall Times: ≤20 ns
   Input Pulse Levels: 0.45V to 2.4V
   Timing Measurement Reference Level: Inputs 1V and 2V
   Outputs 0.8V and 2V

4

READ TIMING DIAGRAM



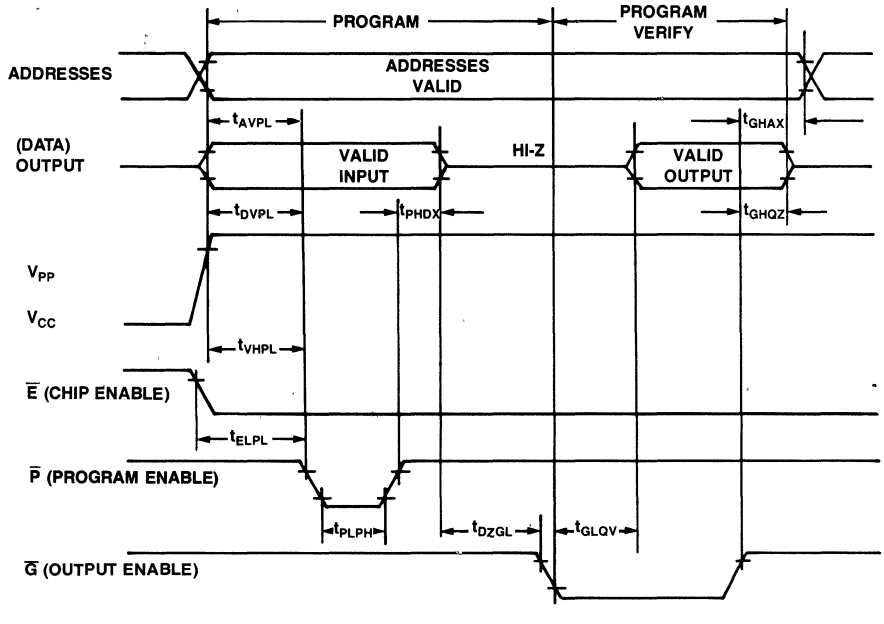
AC CHARACTERISTICS DURING PROGRAM

V_{CC} = 5.0V ± 5%, T_A = 20°C to 30°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units
t_{AVPL}	Address set-up time	2			μs
t_{DZGL}	$\overline{G}$ set-up time	2			μs
t_{DVPL}	Data set-up time	2			μs
t_{ELPL}	$\overline{E}$ set-up time	2			μs
t_{VHPL}	V_{PP} set-up time	2			μs
t_{PHDX}	Data hold time	2			μs
t_{GHAX}	Address hold time	0			μs
t_{GLQV}	Output enable to data valid			120	ns
t_{GHQZ}	Output disable to output high impedance	0		100	ns
t_{PLPH}	$\overline{PE}$ pulse width during programming	45	50	55	ms

Notes:
Test Conditions:
Output Load: 1 TTL gate and C_L = 100 pF
Input Rise and Fall Times: ≤20 ns
Input Pulse Levels: 0.45V to 2.4V
Timing Measurement Reference Level: Inputs 1V and 2V
Outputs 0.8V and 2V

PROGRAM TIMING DIAGRAM



OPERATING MODES

The Rockwell R87C64 has five modes of operation (see table 1).

Read Mode

The read mode is governed by two control pins, $\overline{E}$ and $\overline{G}$. In order to obtain data at the outputs, both $\overline{E}$ and $\overline{G}$ must be V_{IL}. $\overline{E}$ is the power control and should be used for device selection. $\overline{G}$ is the output control and should be used to gate data to the output pins. Valid data will appear on the output pins after T_{AVQV}, T_{ELQV} or T_{GLQV} times, depending on which is limiting.

Standby Mode

The standby mode of the R87C64 reduces power dissipation. The R87C64 is placed in the standby mode by making $\overline{E}$ = V_{IH}. This is independent of $\overline{G}$ and automatically puts the outputs in their high impedance (High-Z) state.

Program Mode

The R87C64 is in the program mode when V_{PP} is at 21V with $\overline{E}$ input at V_{IL}. The data to be programmed is applied to the data output pins. When the address controls and data are stable, a 50 msec program pulse is applied to the $\overline{P}$ input.

Program Verify Mode

A program verify should be performed on the programmed bits to determine that they were correctly programmed. The verify may be performed with V_{PP} at 21V. Data should be verified to t_{GLQV} after the falling edge of $\overline{G}$.

Program Inhibit Mode

The program inhibit mode allows programming several R87C64 EPROMs simultaneously with different data for each by using E to control which devices respond to the program pulse on $\overline{P}$.

Table 1. Mode Selection

Mode \ Pin	$\overline{E}$ (20)	$\overline{G}$ (22)	$\overline{P}$ (27)	V_{PP} (1)	V_{CC} (28)	DQ0-DQ7 (11-13, 15-19)
Read	V_{IL}	V_{IL}	V_{IH}	+5	+5	Q_{OUT}
Standby	V_{IH}	No Effect	No Effect	+5	+5	High-Z
Program	V_{IL}	No Effect	V_{IL}	+21	+5	D_{In}
Program verify	V_{IL}	V_{IL}	V_{IH}	+21	+5	Q_{OUT}
Program inhibit	V_{IH}	No Effect	No Effect	+21	+5	High-Z
Program inhibit	No Effect	No Effect	V_{IH}	+21	+5	High-Z

Note: No Effect = No effect on selection/enable logic, however, no voltage other than logic levels shall be applied.

ERASURE PROCEDURE

Initially, and after each erasure by ultraviolet light, all bits of the R87C64 are in the "1" state. In Program Mode, "0"s are selectively programmed into the desired bit locations. The only way to change a "0" to a "1" is by ultra-violet light erasure.

The recommended erasure procedure for the R87C64 is exposure to ultra-violet light which has a wavelength of 2537 Angstroms.

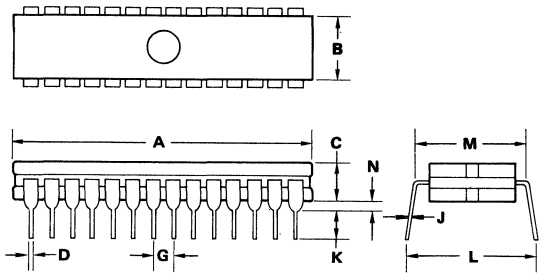
The integrated dose for erasure should be a minimum of 15 W-sec/cm^2. The erasure time with this dosage is 20 minutes using an ultraviolet lamp with a 12000 uW/cm^2 power rating.

Caution

The erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms. Sunlight and certain types of fluorescent lamps have wavelengths in the 3000-4000 Angstroms range.

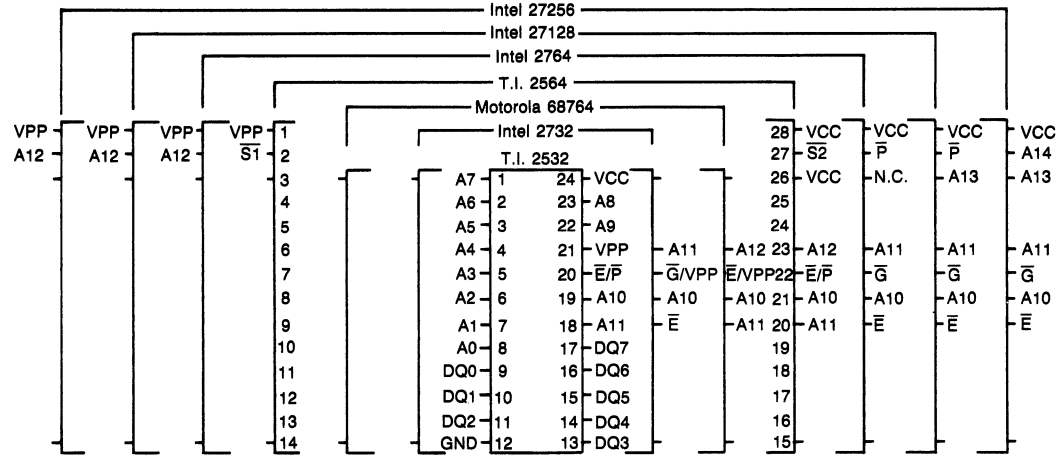
PACKAGE DIMENSIONS

28-PIN CERDIP



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	36.32	37.34	1.430	1.470
B	12.95	13.46	0.510	0.530
C	3.68	4.19	0.145	0.165
D	0.41	0.51	0.016	0.020
F	1.27	1.52	0 050	0 060
G	2.54 BSC		0.100 BSC	
J	0.20	0.30	0.008	0.012
J	0.20	0.30	0.008	0.012
K	3.18	4.19	0.125	0.165
L	16.13	17.41	0.635	0.685
M	15.24	15.75	0.600	0.620
N	0.89	1.14	0.035	0.045

EPROM PINOUTS GUIDE



NOTE: Pins without their function designated are the same as the corresponding pin on the 2532.

4

MOS ROM/EPROM Memory Device Pin Symbols & Names

JEDEC Standard 21A Symbol	Older Symbol	Pin Name
A		Address Input
DQ		Data Input/Output
$\overline{S}$	$\overline{CS}$	Chip Select
$\overline{E}$	$\overline{CE}$, PD	Chip Enable, Power Down
$\overline{G}$	$\overline{OE}$	Output Enable
$\overline{P}$	$\overline{PGM}$	Program Enable
VCC		System/Logic Voltage
VPP		Programming Voltage
VSS, GND		System Ground

Rockwell ROM/EPROM Compatibility

Size	Rockwell ROM/EPROM	Compatible EPROM
32K	R2332A	2532
	R2332B	2732
64K	R2364A	68764
	R2364B	2764
	R23C64*	2764
	R87C64	2764
128K	R23128	27128
	R23C128*	27128
28K	R23256	27256

***NOTE:** Address lines are latched on the falling edge of $\overline{E}$.

SECTION 5
INTELLIGENT DISPLAY CONTROLLERS

INTELLIGENT DISPLAY CONTROLLERS
Cut Costs 30¢/digit, Replace Up To 11 TTL Devices, Interface With Any Host μC

Rockwell display controllers drastically cut the cost and complexity of designing vacuum fluorescent (VF) displays into systems, can actually save up to 30 cents per digit. One 10937 can replace up to eleven TTL devices and can interface with any host microcomputer. VF Display manufacturers Futaba, NEC, and Noritake have all specified these controllers.

The 10937 is a single-chip alphanumeric display controller which directly drives 14 to 18 segment VF displays of up to 16 characters. It includes brightness and refresh controls and logic, its own RAM buffer, PLA segment decoder, and output driver.

The 10951 single-chip display controller is similar to the 10937 except the PLA segment decoder has been reprogrammed to drive a bar graph display and numerics.

If neither the 10937 nor the 10951 PLA segment codes satisfy the user's requirements, a custom code may be specified for the single-chip display controller.

The 10938 segment decoder/driver and the 10939 digit controller/driver operate as a set to drive dot matrix displays. A single set controls 5 x 7 dot matrix displays of up to 20 characters or cascaded to control up to 80 characters. Operating at 50V, the sets can drive VF displays and, with external drivers, LED, CCD, gas discharge and incandescent displays.

The 10941 can team with the 10939 to drive alphanumeric 14-18 segment VF displays of 20 to 40 characters and bar graphs. The 10942 and 10943 can team with the 10939 to drive 40 to 80 character 5 x 12 dot matrix displays.

The Rockwell display controllers are finding wide application in printers, photo copiers, typewriters, FAX machines and in various automotive and white goods uses. If the user has special requirements, a custom code may be specified for the segment decoder/driver device which can be packaged in a 40, 28, or 24 pin DIP according to the device type selected.

A new single-chip controller 10955, now available, is similar to the 10937/10951 devices except the user has control over the number of display outputs allocated as strobes or segments, the PLA is doubled in size to allow 128 characters and the PLA can be bypassed to allow direct control of segments.

VACUUM FLUORESCENT CONTROLLER APPLICATIONS

Display Type	Single Chip	Multi-Chip Display Controller	
	Display Controller (See Part No.)	Anode Driver Type (See Part No.)	Grid Driver (10939)
• 8 Char. 14-18 Seg.	1 (10937)		
• 10 Char. 14-18 Seg.	1 (10937)		
• 16 Char. 14-18 Seg.	1 (10937)		
• 20 Char. 14-18 Seg.		1 (10941)*	1
• 32 Char. 14-18 Seg.		1 (10941)*	2
• 40 Char. 14-18 Seg.		1 (10941)*	2
• 20 Char. 5 x 7 MTX		1 (10938)	1
• 32 Char. 5 x 7 MTX		1 (10938)	2
• 40 Char. 5 x 7 MTX		1 (10938)	2
• 40 Char. 5 x 12 MTX		1 EA (10942) (10943)	2
• 80 Char. 5 x 7 MTX		1 (10938)	4
• 80 Char. 5 x 12 MTX		1 EA (10942) (10943)	4
• Numeric + Bar Graph	1 (10951)		
• Alpha-Numeric + Bar Graph with PLA Bypass	1 (10955)		

Note: *Also controls Bar Graph Displays

Rockwell

10937 and 10957 ALPHANUMERIC DISPLAY CONTROLLER

DESCRIPTION

The 10937 and 10957 Alphanumeric Display Controllers, two of the Rockwell Intelligent Display Controller products, are MOS/LSI general purpose display controllers designed to interface to segmented displays (vacuum fluorescent, or LED).

The 10937 or 10957 will drive displays with up to 16 characters with 14 or 16 segments plus a decimal point and comma tail. Segment decoding within each device provides for the ASCII character set (upper case only). No external drive circuitry is required for displays that operate on 20 ma of drive current up to 50 volts. A 16 × 64-bit segment decoder provides internal ASCII character set decoding for the display.

The 10937 and 10957 are identical with the exception that the 10957 has two additional decodings for the decimal point and comma tail.

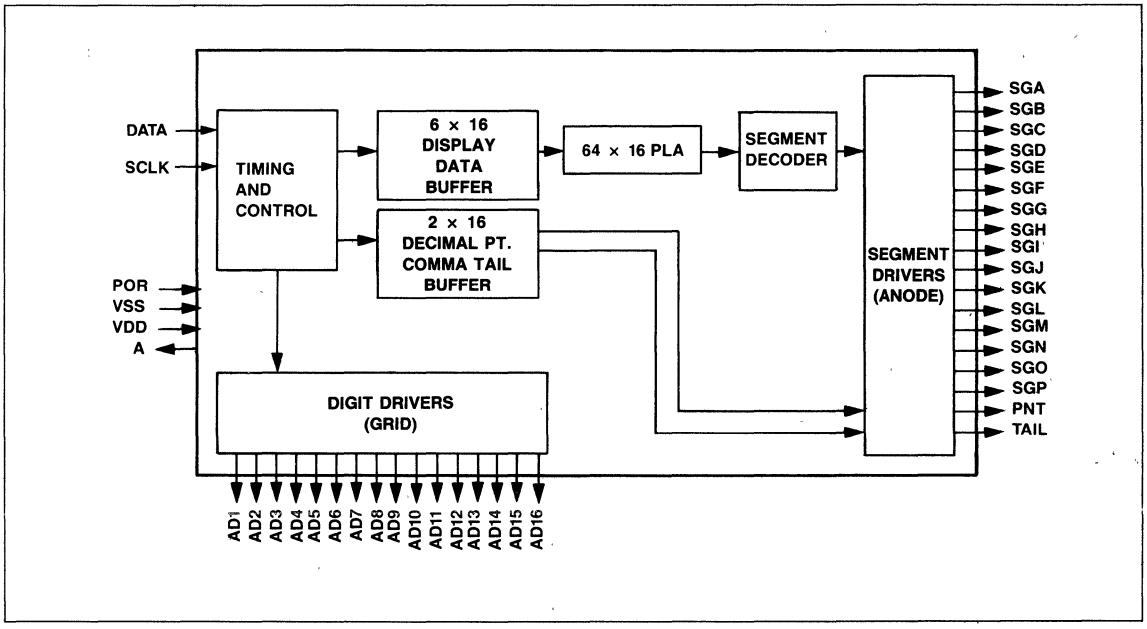
FEATURES

- 16 character display driver with decimal point and comma tail
- 14 or 16 drivers
- Up to 66 kHz data rate
- TTL compatible
- Direct digit drive of 20 ma at 50 volts
- Supports vacuum fluorescent, or LED displays
- 64 × 16-bit PLA provides segment decoding for ASCII character set (all caps only)
- Serial data input for 8-bit display and control words.
- 40-Pin DIP

ORDERING INFORMATION

Part Number	Package Type	Drive Voltage	Temperature Range (°C)
109X7P-40	Plastic	40V	0 to +70
109X7P-50	Plastic	50V	0 to +70
109X7PE-40	Plastic	40V	−40 to +85
109X7PE-50	Plastic	50V	−40 to +85

Note: X = 3 or 5



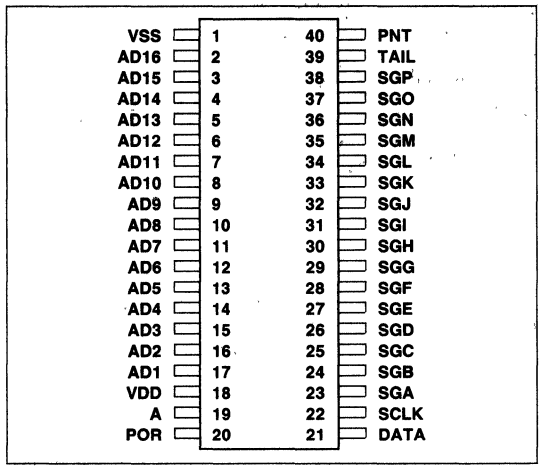
10937 and 10957 Block Diagram

5

INTERFACE DESCRIPTION

Pin Functions

Signal Name	Pin No.	Function
VSS	1	Power and signal reference
AD16–AD1	2–17	Digits 16 through 1 driver outputs
VDD	18	DC power connection
A	19	A clock output used for testing
POR	20	Power-on reset input
DATA	21	Serial data input
SCLK	22	Serial data clock input
SGA–SGP	23–38	Segments A through P driver outputs
TAIL	39	Comma tail driver output
PNT	40	Decimal point driver output



Pin Configuration

SPECIFICATIONS

MAXIMUM RATINGS*

All voltages are specified relative to V_{SS}.

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{DD}	+0.3	−20	V
Input Voltage	V_{IN}	+0.3	−20	V
Output Voltage	V_{OUT}	+0.3	−50	V
Operating Temperature				
Commercial	T_C	0	+70	°C
Industrial	T_I	−40	+85	°C
Storage Temperature	T_{STG}	−55	+125	°C
Input Capacitance	C_{IN}		5	pF
Output Capacitance	C_{OUT}		10	pF

***NOTE:** Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

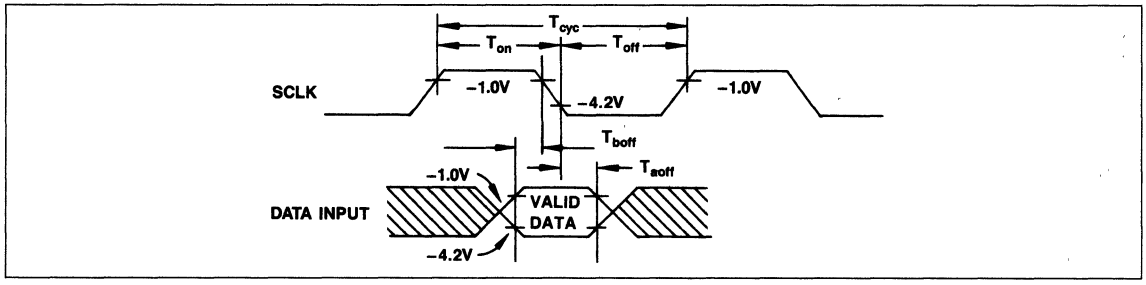
DC CHARACTERISTICS

Parameter	Limits (V_{SS} = 0) Min.	Typ.	Max.	Limits (V_{SS} = +5V) Min.	Typ.	Max.	Conditions	Unit
Supply Voltage (V_{DD})	−16.5	−15.0	−13.5	−11.5	−10.0	−8.5		V
Input DATA, SCLK,								V
Logic "1"	−1.0		+0.3	+4.0		+5.3		V
Logic "0"	V_{DD}		−4.2	V_{DD}		+0.8		
Input POR								
Logic "1"	−3.0		+0.3	+2.0		+5.3		
Logic "0"	V_{DD}		−10.0	V_{DD}		−5.0		
Output Digit and Segment Strobes								
Driver On								
Commercial			−1.5			+3.5	At 10 mA	V
Industrial			−1.7			+3.3	At 10 mA	V
Driver Off 109X7-40			−40			−35	Actual value determined by external circuit	V
Driver Off 109X7-50			−50			−45	Actual value determined by external circuit	V
Output Leakage			10			10	Per driver when driver is off	μA
Input Leakage			10			10	Per driver when driver is off	μA

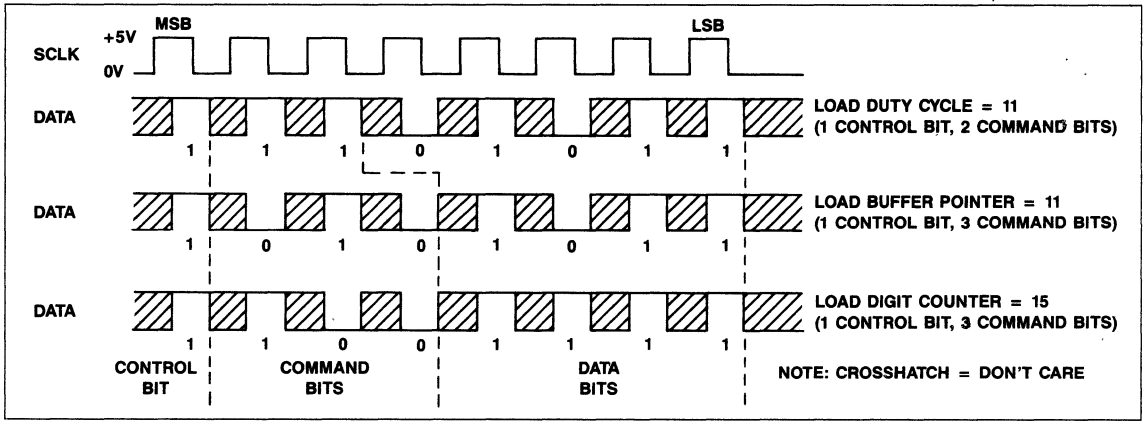
Notes: All outputs require pulldown resistors. X = 3 or 5 depending on device.

AC CHARACTERISTICS

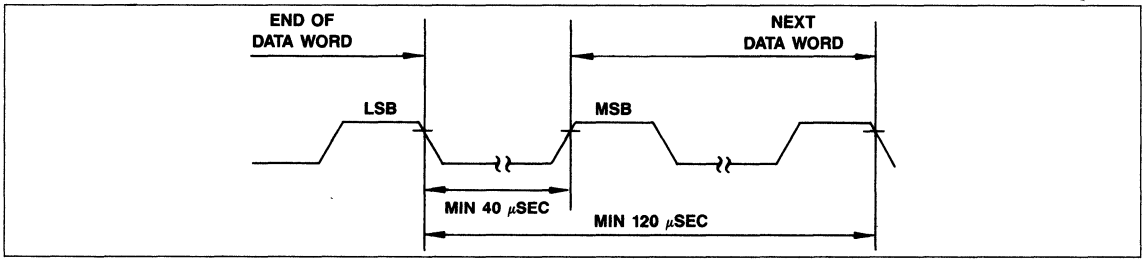
Parameter	Symbol	Min	Typ	Max	Unit
SCLK Clock					
On Time	T_{on}	1.0		20.0	μs
Off Time	T_{off}	1.0			μs
Data Input Sample Time					
Before SCLK Clock Off	T_{boff}	200			ns
After SCLK Clock Off	T_{aoff}	100			ns



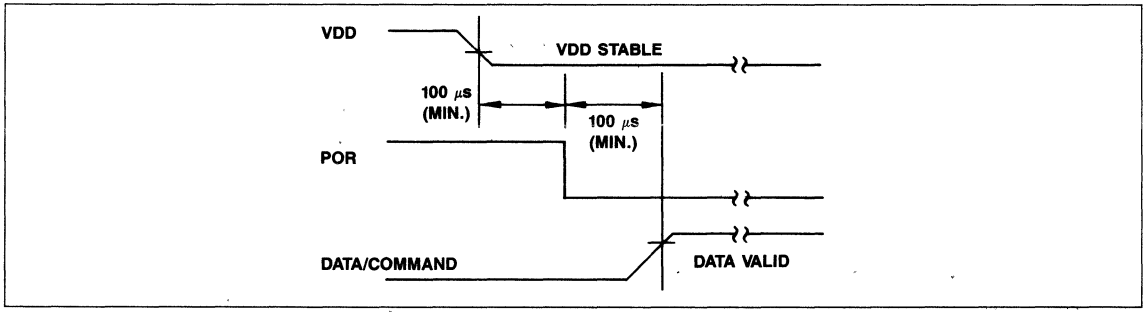
SLK and Serial Data Timing



SCLK and Serial Data (Control Word) Examples



Data Word LSB/MSB Timing



Power-On Reset Timing

FUNCTIONAL DESCRIPTION

The 10937 or 10957 is a general purpose display controller for multiplexed, segmented displays with up to 16 character positions and 14 or 16 segments, plus decimal point and comma tail. No external drive circuitry is needed for displays requiring up to 20 ma of drive current up to 50 volts. All timing signals required to control the display are generated in the 10937 or 10957 device without any refresh input from the host processor.

Input data is loaded into the Display Data Buffer via the Serial Data Input (Data) channel. Internal timing and control blocks synchronize the segment and digit output signals to provide the proper timing for the multiplexing operation. A 16 x 64-bit PLA is provided for segment decoding for the full ASCII character set (upper case only).

Input data is loaded into the 10937 or 10957 ADC as a series of 8-bit words with the most significant bit (MSB), bit 7, first. If bit 7 of any word loaded is a logic 1 (this bit is referred to as the control bit C), the loaded word is a control data word. If the C bit of any word is a logic 0, the loaded word is a display data word. The following paragraphs describe the format and functions of these control and display data words.

INPUT CONTROL DATA WORDS

When the C-Bit (bit 7) of the 8-bit input word is a logic 1, bits 5 and 6 are decoded into one of four control commands while data associated with the command are extracted from bits 0 – 4 (see Table 1). The four control codes perform the following display functions:

- Load the Display Data Buffer pointer,
- Load the Digit Counter,
- Load the Duty Cycle register,
- Enter Test Mode.

Table 1 lists the control codes and their functions.

Buffer Pointer Control

The Buffer Pointer Control code allows the Display Data Buffer pointer to be set to any digit position so that individual characters may be modified. The Buffer Pointer is loaded with a decimal equivalent value 2 less than the desired value (i.e., to point to the digit controlled by AD6 of the display, a value of 4 is entered). See Table 2 for a complete list of the Buffer Pointer values.

Table 2. Buffer Pointer Control Codes

Hex Code	Pointer Value	Character Controlled By
A0	16	AD2
A1	1	AD3
A2	2	AD4
A3	3	AD5
A4	4	AD6
A5	5	AD7
A6	6	AD8
A7	7	AD9
A8	8	AD10
A9	9	AD11
AA	10	AD12
AB	11	AD13
AC	12	AD14
AD	13	AD15
AE	14	AD16
AF	15	AD1

Digit Counter Control

The Digit Counter Control code is normally used only during initialization routines to define the number of character positions to be controlled. This code maximizes the duty cycle for any display. If 16 characters are to be controlled, enter a value of 0 (zero). Otherwise, enter the value desired.

Duty Cycle Control

The Duty Cycle Control code is used to turn the display on and off, and to adjust display brightness. As shown in the block diagram, the time slot for each character is 32 clock cycles. The segment and digit drivers for each character are on for a maximum of 31 cycles with a 1 cycle inter-digit off-time. The Duty Cycle Control code contains a 5-bit numeric field which modifies the on-time for the driver outputs from 0 to 31 cycles. A duty cycle of 0 puts both the segment and digit drivers into the off state.

Enter Test Mode

The Enter Test Mode code is a device test function only. If executed, it will lock the device in the Test Mode. Once locked in, the device can only be removed from Test Mode by performing a power-on reset.

If this mode is activated, the digit time is reduced from 32 to 4 clock cycles to speed up the output driver sequencing time for ease in testing.

INPUT DISPLAY DATA WORDS

Display data words are loaded as 8-bit ASCII format codes. The 64 codes available (with the C-bit set to 0 to indicate a display data word) are shown in Table 3 with their corresponding ASCII characters.

Table 1. Control Data Words

8-Bit Control Word		
C-Bit (Bit 7)	7-Bit Code (Bits 6 – 0)	Function
1	010NNNN(1)	BUFFER POINTER CONTROL (Position of character to be changed)
1	100NNNN(1)	DIGIT COUNTER CONTROL (Number of characters to be output)
1	11NNNNN(2)	DUTY CYCLE CONTROL (On/off and brightness control)
1	00NNNNN(3)	ENTER TEST MODE (Not a user function)

Notes: 1. NNNN is a 4-bit binary value representing the digit number to be loaded.
2. NNNNN is a 5-bit binary value representing the number of clock cycles each digit is on.
3. This code is a device test function only. If executed it will lock the device in the test mode. Once locked in, the device can only be removed from Test Mode by performing a power-on reset.

Sixteen display data words must be entered to completely load the Display Data Buffer. The Buffer Pointer is automatically incremented before each data word is stored in the Display Buffer except for decimal point and comma words. These do not cause the Buffer Pointer to increment and thus are always associated with the previous character entered. To select the next character position to be loaded out of the normal sequence, use the Buffer Pointer Control command before entering the display data word. It is not necessary to use the Buffer Pointer Control command to cycle back to position 1 when less than 16 character positions are being used.

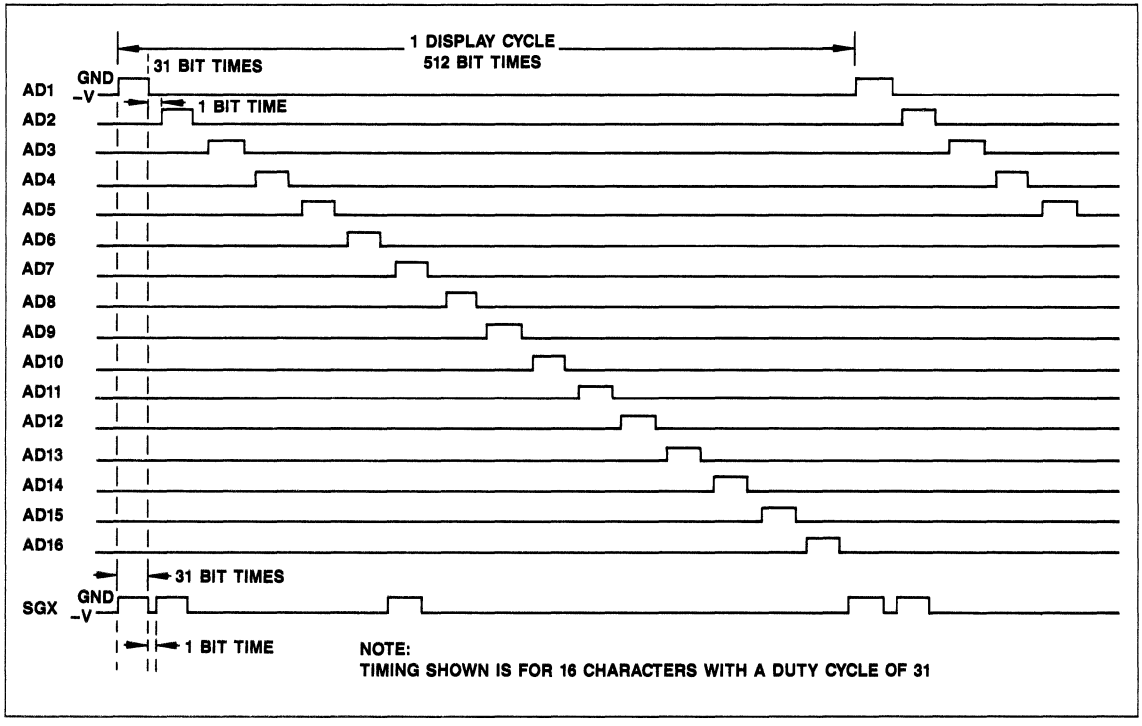


Figure 1. Display Scan Timing Diagram (Duty Cycle)

Table 3. Character Assignments for Display Data Words

DATA WORD		CHARACTER	DATA WORD		CHARACTER	DATA WORD		CHARACTER	DATA WORD		CHARACTER
BINARY	HEX		BINARY	HEX		BINARY	HEX		BINARY	HEX	
0X000000	00	@	0X010000	10	P	0X100000	20		0X110000	30	0
0X000001	01	A	0X010001	11	Q	0X100001	21	!	0X110001	31	1
0X000010	02	B	0X010010	12	R	0X010010	22	"	0X110010	32	2
0X000011	03	C	0X010011	13	S	0X100011	23	#	0X110011	33	3
0X000100	04	D	0X010100	14	T	0X100100	24	$	0X110100	34	4
0X000101	05	E	0X010101	15	U	0X100101	25	%	0X110101	35	5
0X000110	06	F	0X010110	16	V	0X100110	26	&	0X110110	36	6
0X000111	07	G	0X010111	17	W	0X100111	27	'	0X110111	37	7
0X001000	08	H	0X011000	18	X	0X101000	28	(	0X111000	38	8
0X001001	09	I	0X011001	19	Y	0X101001	29	)	0X111001	39	9
0X001010	0A	J	0X011010	1A	Z	0X101010	2A	*	0X111010	3A	:
0X001011	0B	K	0X011011	1B	[	0X101011	2B	+	0X111011	3B	;
0X001100	0C	L	0X011100	1C	/	0X101100	2C	'	0X111100	3C	<
0X001101	0D	M	0X011101	1D	]	0X101101	2D	—	0X111101	3D	=
0X001110	0E	N	0X011110	1E	/\	0X101110	2E	.	0X111110	3E	>
0X001111	0F	O	0X011111	1F	-	0X101111	2F	\	0X111111	3F	?

Note: X means this bit (bit 7) is a "don't care" bit except for PNT and TAIL on 10957 only. The hex codes shown assume bit 7 is a zero.

POWER-ON RESET (POR)

The Power-On Reset (POR) initializes the internal circuits of the 10937 or 10957 ADC when power (V_{DD} is applied. The following conditions are established after a Power-On Reset:

a. The Digit Drivers (AD1 – AD16) are in the off state (floating).
b. The Segment Drivers (SGA – SGP) are in the off state (floating). This includes PNT and Tail.
c. The Duty Cycle is set to 0.
d. The Digit Counter is set to 16 (a bit code value of 0).
e. The Buffer Pointer points to the character controlled by AD1.

DIGIT DRIVERS (AD1–AD16)

The sixteen Digit Drivers (AD1 – AD16) are used to select each of the display digits sequentially during a refresh scan. Display segments will be illuminated when both the Digit Drivers and Segment Drivers for a particular character are energized simultaneously. The timing characteristics of both the digits and segments are shown in Figure 1. See POR for the Power-On Reset state of these drivers.

Table 4. Additional Codes for PNT and Tail On 10957

DATA WORD		CHARACTER
BINARY	HEX	
01101100	6C	, (Tail only)
01101110	6E	Blank

SEGMENT DRIVERS (SGA–SGP)

Sixteen (16) Segment Drivers are provided (SGA – SGP), plus the decimal point (PNT) and comma tail (TAIL). The segment outputs are internally decoded from the 8-bit characters in the Display Data Buffer by means of a 64 × 16-bit PLA. The Segment Driver Allocations are shown in Figure 2. Data codes and their corresponding segment patterns are shown in Figure 3. Timing characteristics for the segment outputs are shown in Figure 1. See POR for the Power-On Reset state of these drivers.

NOTE

For 14-segment displays, SGA is used for the top segment and SGF is used for the bottom segment. SGB and SGE can be floated.

TYPICAL SYSTEM HOOK-UP

Figure 4 shows the 10937 or 10957 as it would be connected to a V-F display when driven by a host system. E_K is determined by the V-F display specifications and R_C is selected to provide proper biasing current for zeners. Pull down resistors R_A and R_G are determined by the interconnection capacitance between the device and the display.

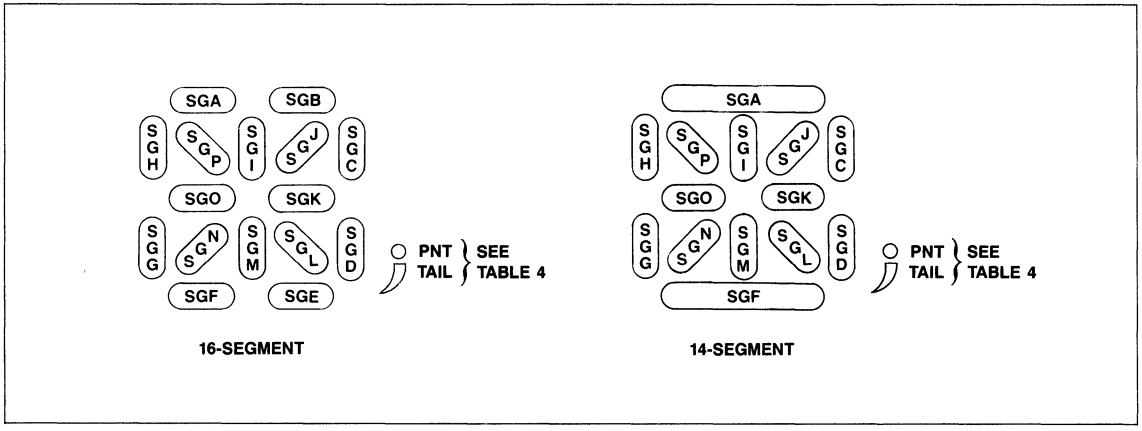
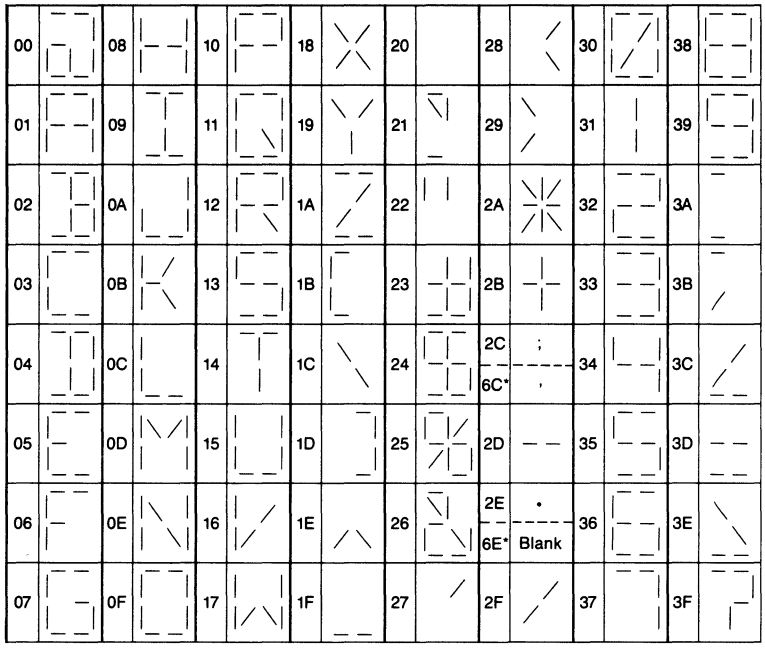
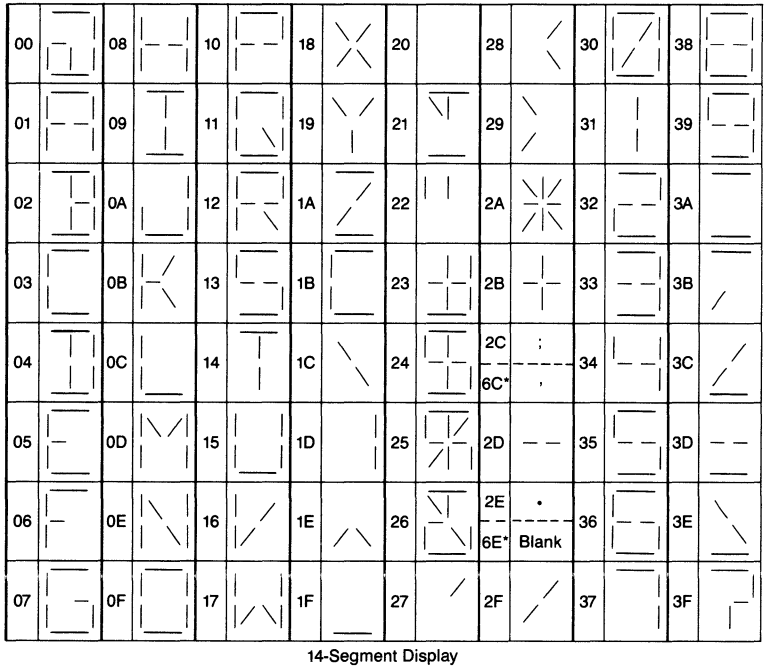


Figure 2. Segment Driver Allocations



16-Segment Display



14-Segment Display

Notes: Bit 7 of the data byte is a "don't care" bit except for PNT and TAIL on 10957. Data byte hex codes shown assume bit 7 is a zero.
* = 10957 only.

Figure 3. Display Segment Driver Character Patterns

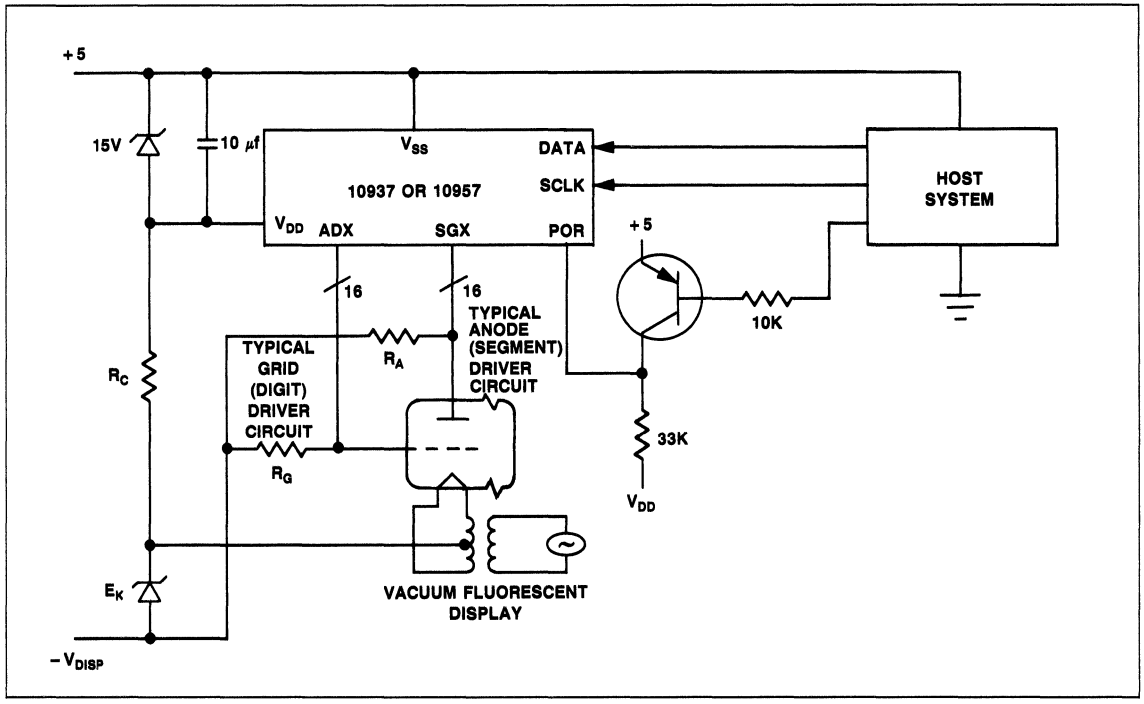


Figure 4. Partial System Schematic

Rockwell

10938 AND 10939
DOT MATRIX DISPLAY CONTROLLER

DESCRIPTION

The Rockwell 10938 and 10939 Dot Matrix Display Controller is a two-chip MOS/LSI general purpose display controller system designed to interface to dot matrix displays (vacuum-fluorescent or LED).

The two-chip set will drive displays with up to 35 anodes (dots) and up to 20 grids (characters) plus a cursor. The chips can be cascaded to drive larger displays of as many as 80 characters. An internal PLA-type decoder provides character decoding and dot pattern generation for the full 96-character ASCII set and an additional 32 special characters.

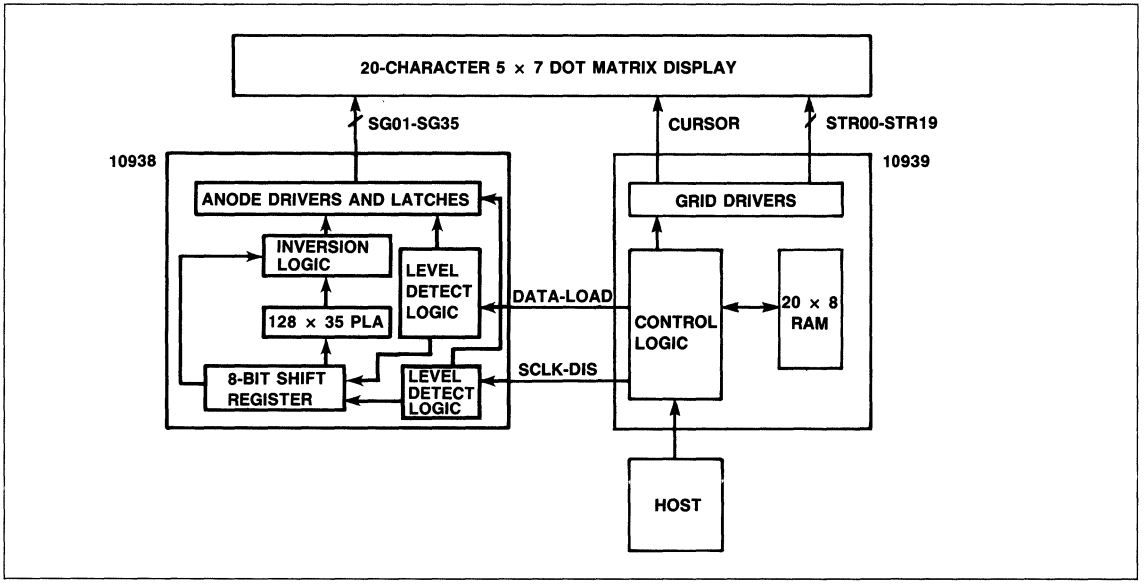
ORDERING INFORMATION

Part Number	Package Type	Temperature Range (°C)
10938P	Plastic	0 to +70
10938PE	Plastic	−40 to +85
10939P	Plastic	0 to +70
10939PE	Plastic	−40 to +85

FEATURES

- 20-character display driver cascadable to 80
- Standard 5 x 7 character font. Custom fonts available by special order
- Separate cursor driver output
- Direct drive capability for vacuum-fluorescent displays
- 128 x 35 PLA provides segment decoding for full 96-character ASCII set, plus 32 special characters
- Serial or parallel data input for 8-bit display and control characters
- Brightness, refresh rate, and display mode controls
- 40-pin DIP

5

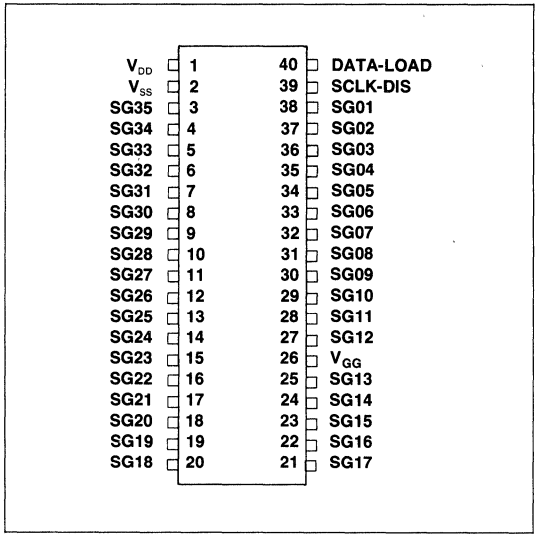


Block Diagram of 10938 and 10939

INTERFACE DESCRIPTION

10938 Pin Functions

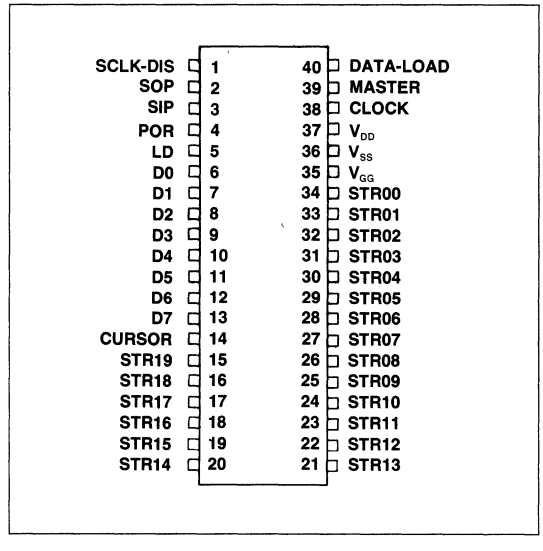
Signal Name	Pin No.	Function
V_{SS}	2	Power and signal reference
SG01-SG35	3-25, 27-38	Anode driver outputs
SCLK-DIS	39	Serial data shift clock
DATA-LOAD	40	Serial data output/latch control
V_{DD}	1	DC Power
V_{GG}	26	Display voltage



10938 Pin Configuration

10939 Pin Functions

Signal Name	Pin No.	Function
V_{SS}	36	Power and signal reference
V_{DD}	37	DC Power
CLOCK	38	Synchronization Clock
CURSOR	14	Cursor drive output
MASTER	39	Master/Slave Mode control
SIP	3	Sync Input
SOP	2	Sync Output
D0-D7	6-13	Serial or parallel data input
LD	5	Input data strobe
POR	4	Power-on reset
SCLK-DIS	1	Serial data shift clock
DATA-LOAD	40	Serial data output/latch control
STR00-STR19	15-34	Grid Driver Outputs
V_{GG}	35	Display voltage



10939 Pin Configuration

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS*

Voltages are referenced to V_{SS}

Parameter	Symbol	Value	Unit
Operating Temperature			
Commercial	Tc	0 to +70	°C
Industrial	Ti	−40 to +85	°C
Storage Temperature		−55 to +125	°C
Operating Voltage	V_{DD}	−22 to −18	Vdc
Operating Display Voltage	V_{GG}	−50	Vdc

***NOTE:** Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in other sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

All voltages referenced to V_{SS}

Parameter	Notes	Symbol	Min	Typ	Max	Unit
Input D0-D7, LD, SIP	2					
Logic "1"		V_{IH}	−1.2		+0.3	V
Logic "0"		V_{IL}	V_{DD}		−4.2	V
Input POR	2					
Logic "1"		V_{IHPO}	−3.0		+0.3	V
Logic "0"		V_{ILPO}	V_{DD}		−10.0	V
Output SOP	2					
Logic "1"		V_{OHSY}	−1 2		V_{SS}	V
Logic "0"		V_{OLSY}	V_{DD}		−4.2	V
Output Grids, Cursor, and Anodes	1					
Logic "1" (I_{load} = 10 mA 10939, 2 mA 10938)		V_{OH}	−1.5		V_{SS}	V
Logic "0" (I_{load} = 0 mA)		V_{OL}	V_{GG}		0.95 × V_{GG}	V

Notes: 1. Designates characteristics for both 10938 and 10939
2. Designates characteristics for 10939

OPERATING CURRENTS

Parameter	Maximum		Typical	Unit
	Industrial **TA = −40°C** **V_{DD} = −22 Vdc** **V_{GG} = −50 Vdc**	**Commercial** **TA = 0°C** **V_{DD} = −22 Vdc** **V_{GG} = −50 Vdc**	**TA = 25°C** **V_{DD} = −20 Vdc** **V_{GG} = −50 Vdc**	
10938[1]				
I_{DD}	4.5	3.6	3.2	mA
I_{GG}	11.2	9.0	8.0	mA
10939 (master)[2]				
I_{DD}	13.6	10.9	6.0	mA
I_{GG}	1.0	0.8	0.5	mA
10939 (slave)[2]				
I_{DD}	9.1	7.3	4.0	mA
I_{GG}	1.0	0.8	0.5	mA

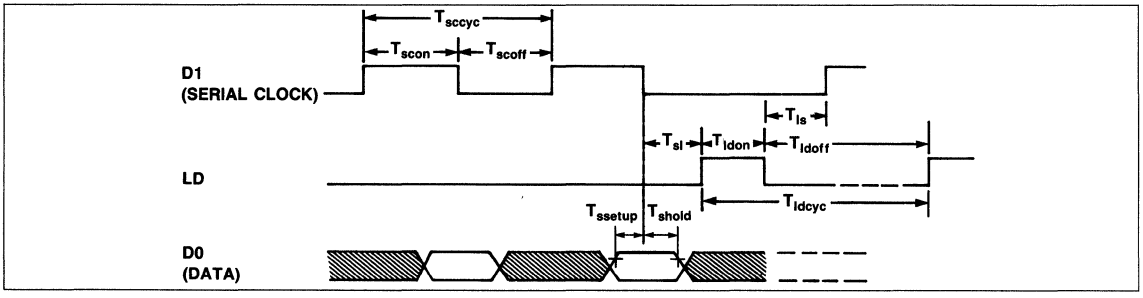
Notes.
1. The 10938 has 35 internal drivers which are brought out I_{GG} is proportional to the number of drivers on. The values given are for all 35 drivers on. Divide I_{GG} shown by 35 to determine I_{GG} for one driver
2. The 10939 will never have more than two drivers on at any one time; one grid driver and the cursor. The values shown are for two drivers on with 100% duty cycle.

5

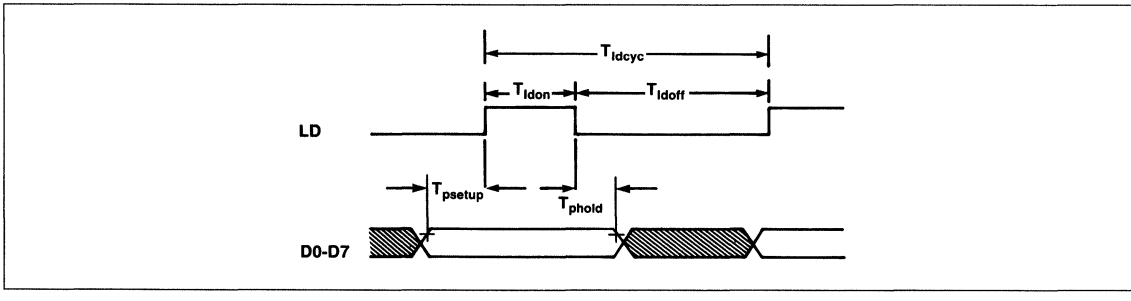
AC CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Unit
GENERAL INTERFACE TIMING					
Data Load (LD)					
On Time	T_{ldon}	1.0			µs
Off time	T_{ldoff}				
Commercial		40.0			µs
Industrial		44.5			µs
Cycle Time	T_{ldcyc}				
Commerical		60.0			µs
Industrial		66.7			µs
SERIAL INTERFACE TIMING					
Serial Clock (D1)					
On Time	T_{scon}	1.0		20.0	µs
Off Time	T_{scoff}	1.0			µs
Cycle Time	T_{sccyc}	2.0			µs
Serial Clock (D0)					
Set-up Time	T_{ssetup}	400			ns
Hold Time	T_{shold}	400			ns
Serial Clock to LD Time	T_{sl}	1.0			µs
LD to Serial Clock	T_{ls}	1.0			µs
PARALLEL INTERFACE TIMING					
Parallel Data (D0–D7)					
Set-up Time	T_{psetup}	0			ns
Hold Time	T_{phold}	200			ns

TIMING WAVEFORMS



Serial Interface Timing Waveforms



Parallel Interface Timing Waveforms

FUNCTIONAL DESCRIPTION

Once the display buffer has been loaded from the host processor, the 10938/10939 system generates all timing signals required to control the display.

Input data is loaded into the Display Data Buffer as a series of 8-bit words via the Serial or Parallel Data Input channel on the 10939. Internal timing and control logic synchronize the digit output signals with the Serial Data and Load signals to the 10938 to provide the proper timing for the multiplexing operation. A 128 × 35 bit PLA is provided for decoding the full 96 character ASCII set, plus 32 special characters.

The parallel data input mode is implemented by toggling any of data lines D2–D7 after POR has gone low. Once the parallel data load mode has been implemented, a power-on reset procedure must be performed to return to serial data load mode. Parallel data transfer is accomplished by putting the command or display data on the data lines, then pulsing the LD line. The load cycle time must be at least 60 μs with the LD line set high for at least one μs and held low for at least 40 μs.

The serial data input mode is implemented during the power-on reset procedure. In those systems using serial mode, ports D2–D7 should be tied low to prevent the inadvertent implementation of the parallel load mode. Serial data bytes are shifted into a data buffer MSB first on line D0 using line D1 as the serial clock. The last eight bits clocked in are latched into the display controller by a pulse on the LD line. The cycle time for each data bit is 2 μs and the load time for each byte is 60 μs.

Input data may be Control or Display data. The following paragraphs describe the format and functions of these control and display data words.

CONTROL DATA WORDS

Control data words are used to select the operating parameters of the display controller. They must be preceded by a Control Prefix word (0000 0001, hexadecimal 01) to be distinguished from Display Data words.

Buffer Pointer Control

The Buffer Pointer Control code sets the Display Data Buffer pointer. The lower 5 bits of the code are loaded into the buffer pointer (see Table 2).

Table 1. Control Word Assignments

Hex Value	Function
00	Not used
01	Load 01 into Data Buffer
02	Not used
03	Not used
04	Not used
05	Set digit time to 16 cycles per grid
06	Set digit time to 32 cycles per grid
07	Set digit time to 64 cycles per grid
08	Enable Normal Display Mode (MSB in data words is used for cursor control only)
09	Enable Blank Mode (data words with MSB = 1 will be blanked and cursor will be on)
0A	Enable Inverse Mode (data words with MSB = 1 will be "inversed" and cursor will be on)
0B	Not used
0C	Not used
0D	Not used
0E	Start Display Refresh Cycle (use only once after reset)
0F	Not used
10–3F	Not used
40–4F	Load Duty Cycle Register with lower 6 bits (0–63)
80–9F	Load Digit Counter (80 = 32, 81 = 1, 82 = 2, etc.)
A0–BF	Not used
C0–D3	Load Buffer Pointer Register with lower 5 bits
E0–FF	Not used

Table 2. Buffer Pointer Control Codes

Code Value	Pointer Value	Character Position
C0	00	0
C1	01	1
C2	02	2
C3	03	3
C4	04	4
C5	05	5
C6	06	6
C7	07	7
C8	08	8
C9	09	9
CA	0A	10
CB	0B	11
CC	0C	12
CD	0D	13
CE	0E	14
CF	0F	15
D0	10	16
D1	11	17
D2	12	18
D3	13	19

Note:
DO NOT USE CHARACTER POSITIONS 20–31 (CODES D4–DF)

5

Digit Counter Control

The Digit Counter Control code defines the number of character positions (grids) to be controlled. This code is normally used only during initialization routines, but it may also be used in conjunction with the Duty Cycle Control code to extend the range of brightness control (see Table 3).

Duty Cycle Control

The Duty Cycle Control code turns the display on and off, adjusts display brightness, and modifies display timing. The time slot for each character is 16, 32, or 64 cycles as selected by the Digit Time Control codes (see Table 3). The anode and grid drivers for each character are on for a maximum of 13, 29, or 61 cycles with a 3 cycle inter-digit off-time. The lower 6 bits of the Duty Cycle Control code are loaded into the Duty Cycle Register. Resultant duty cycles are shown in Table 4.

Table 3. Digit Counter Control Codes

Code	Digit Counter Value	No. of Grids Controlled
80	00	32
81	01	1
82	02	2
83	03	3
84	04	4
85	05	5
86	06	6
87	07	7
88	08	8
89	09	9
8A	0A	10
8B	0B	11
8C	0C	12
8D	0D	13
8E	0E	14
8F	0F	15
90	10	16
91	11	17
92	12	18
93	13	19
94	14	20
95	15	21
96	16	22
97	17	23
98	18	24
99	19	25
9A	1A	26
9B	1B	27
9C	1C	28
9D	1D	29
9E	1E	30
9F	1F	31

Digit Time Select

The Digit Time Select code sets the total time for each character during the refresh cycle. Three values can be set using the three codes shown in Table 1. The default value set at power-on is 64 cycles per grid. For displays with 40 or more characters, or under conditions where the display can be subjected to quick movements during viewing (e.g. portable or vehicle-mounted applications), it may be necessary to increase the refresh rate by selecting 16 or 32 cycles per grid with the appropriate control code.

Table 4. Duty Cycle Control Codes

	Digit Time = 16		Digit Time = 32		Digit Time = 64	
Code	On	Off	On	Off	On	Off
40	—	16	—	32	—	64
41	—	16	—	32	—	64
42	—	16	—	32	—	64
43	1	15	1	31	1	63
44	2	14	2	30	2	62
45	3	13	3	29	3	61
46	4	12	4	28	4	60
47	5	11	5	27	5	59
48	6	10	6	26	6	58
49	7	9	7	25	7	57
4A	8	8	8	24	8	56
4B	9	7	9	23	9	55
4C	10	6	10	22	10	54
4D	11	5	11	21	11	53
4E	12	4	12	20	12	52
4F	13	3	13	19	13	51
50	13	3	14	18	14	50
51	13	3	15	17	15	49
52	13	3	16	16	16	48
53	13	3	17	15	17	47
.	.	.	.	.	.	.
.	.	.	.	.	.	.
.	.	.	.	.	.	.
5B	13	3	25	7	25	39
5C	13	3	26	6	26	38
5D	13	3	27	5	27	37
5E	13	3	28	4	28	36
5F	13	3	29	3	29	35
60	13	3	29	3	30	34
61	13	3	29	3	31	33
62	13	3	29	3	32	32
.	.	.	.	.	.	.
.	.	.	.	.	.	.
.	.	.	.	.	.	.
7C	13	3	29	3	58	6
7D	13	3	29	3	59	5
7E	13	3	29	3	60	4
7F	13	3	29	3	61	3

Display Mode Select

Each ASCII character is represented by the lower seven bits of the 8-bit value loaded into the 10939. The eighth (most significant) bit controls the cursor (see Cursor Control). This bit is known as the data byte control bit. If either Blank or Inverse mode is selected, a "0" in this bit causes a normal character display, while "1" selects either Blank or Inverse mode, depending on which mode is enabled. Three control codes are provided (see Table 1) to Enable Blank Mode, Enable Inverse Mode, or Enable Normal Display Mode.

In the Blank mode, any character with the MSB = "1" will be blanked. In the Inverse mode, it will be displayed with all segment driver outputs inverted. On video displays, this is referred to as "Inverse Video" format. These controls allow individual characters or groups of characters to be blinked or blanked by simply changing the mode without changing the data in the Display Buffer.

Cursor Control

The data byte control bit (MSB 8), besides selecting Blank, Inverse, or Normal mode, also controls the cursor output which is enabled on all characters with the MSB equal to one. Therefore, when the Normal mode is enabled and the MSB of the data byte is set to a one, the normal character is displayed with the cursor on. When the Blank mode is enabled and the MSB is set to a one, the character is blanked but the cursor is on. If Inverse mode is enabled and the MSB is set to a one, the inverse character is displayed and the cursor is on but not inversed.

Start Refresh

At power on, the 10939 is held in an internal halt mode. The normal display refresh sequence starts upon receipt of a Start Refresh control code. This is particularly useful for synchronizing systems using more than one 10939. Only the Master 10939 in a multi-chip system will recognize the Start Refresh code. The Master starts the Slave(s) at the appropriate time, using the SOP signal.

INPUT DISPLAY DATA WORDS

Display data words are loaded as 8-bit codes. The eighth (most significant) bit specifies normal (0) or blank/inverse (1) display mode, depending on the blank/inverse mode selection (see Control data words 09 and 0A in Table 1). This bit also controls the cursor.

Twenty display data words must be entered to completely load the Display Data Buffer. The Buffer Pointer automatically increments after each data word is stored in the buffer. To select a character position to be loaded out of sequence, use the Buffer Pointer control code. The Buffer Pointer will automatically reset to character position 0 when its value is equal to the programmed Digit Count.

POWER-ON RESET

The Power-On Reset (POR) initializes the internal circuits of the 10939. This is normally accomplished when power (V_{DD}) is applied. The following conditions are established by application of POR:

a. The Grid Drivers (STR00–STR19) on the 10939 are in the off state.
b. The Anode Drivers (SG01–SG35) on the 10938 are in the off state.
c. The Duty Cycle is set to 0.
d. The Digit Counter is set to 32.
e. The Buffer Pointer is set to 0.
f. The Digit time is set to 64.
g. The Normal display mode is set.
h. DATA-LOAD is set to high impedance state.
i. SCLK-DIS is set to V_{OL} to disable the anode drivers in the 10938.
j. SOP is set to V_{OL} to disable the sync pulse.

NOTE:

1. When the POR signal is removed, SCLK-DIS is set to the high impedance state.
2. During the initial rise time of V_{DD} at power turn-on, the magnitude of V_{GG} should not exceed the magnitude of V_{DD}.

GRID (DIGIT) DRIVERS (STR00–STR19) PLUS CURSOR

The 20 Digit Drivers select each of the display character positions sequentially during a refresh scan. Display dots will be illuminated when both the Digit Drivers and Dot Drivers for a particular character are energized simultaneously. The cursor segment is generated by the 10939, but its timing characteristics are identical to the anode timing generated by the 10938.

ANODE (DOT) DRIVERS (SG01–SG35)

35 Dot Drivers are provided in the 10938. The output states for each character pattern are internally decoded from the 8-bit characters received from the 10939 by means of a 128 × 35-bit PLA. Data codes and the corresponding patterns are shown in Figure 1. Figure 2 shows the Dot Drivers (SG01–SG35) assignments as they relate to the 5 × 7 dot matrix patterns.

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TYPICAL SYSTEM HOOKUPS

Figure 3 shows a 10938 and 10939 in a parallel interface with the host system driving a 20 character display. Figure 4 shows a 10938 and a 10939 in a serial interface with the host system driving a 20 character display. Figure 5 shows a 10938 and two 10939's in a parallel interface with the host system driving a 40 character display.

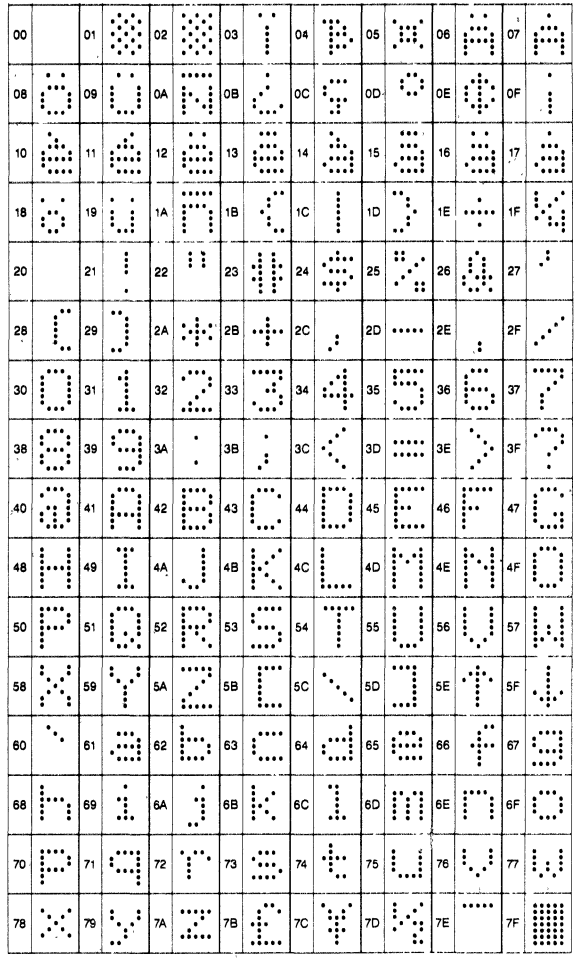

Figure 1. 5 x 7 Dot Matrix PLA Patterns

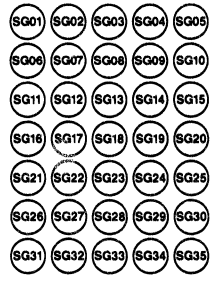

Figure 2. Anode (Dot) Driver Assignments

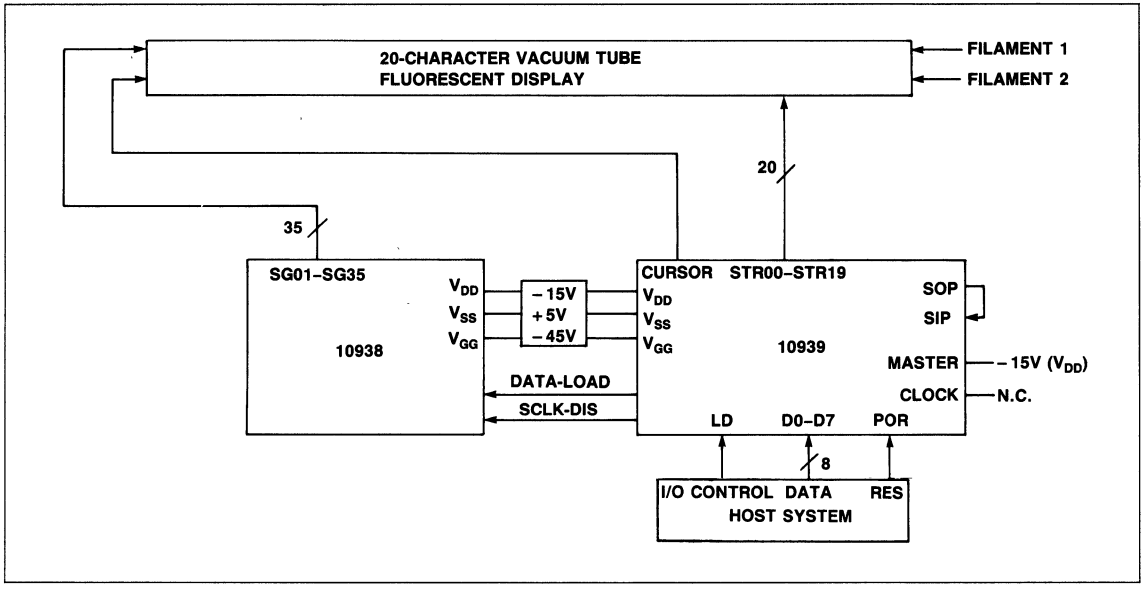

Figure 3. Typical Display System with Parallel Interface to Host System

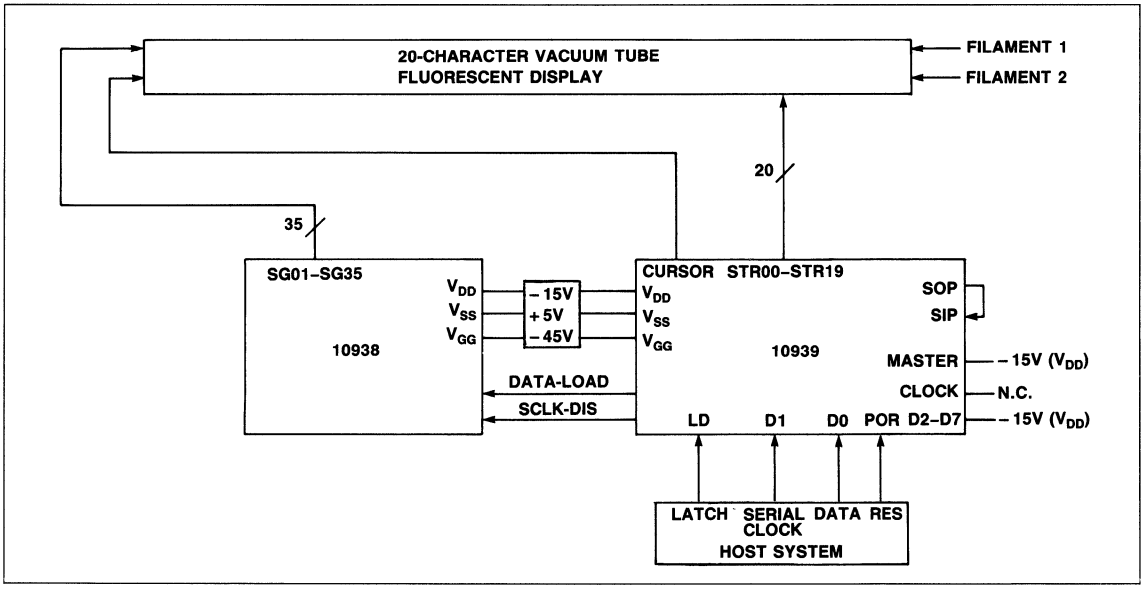

Figure 4. Typical Display System with Serial Interface to Host System

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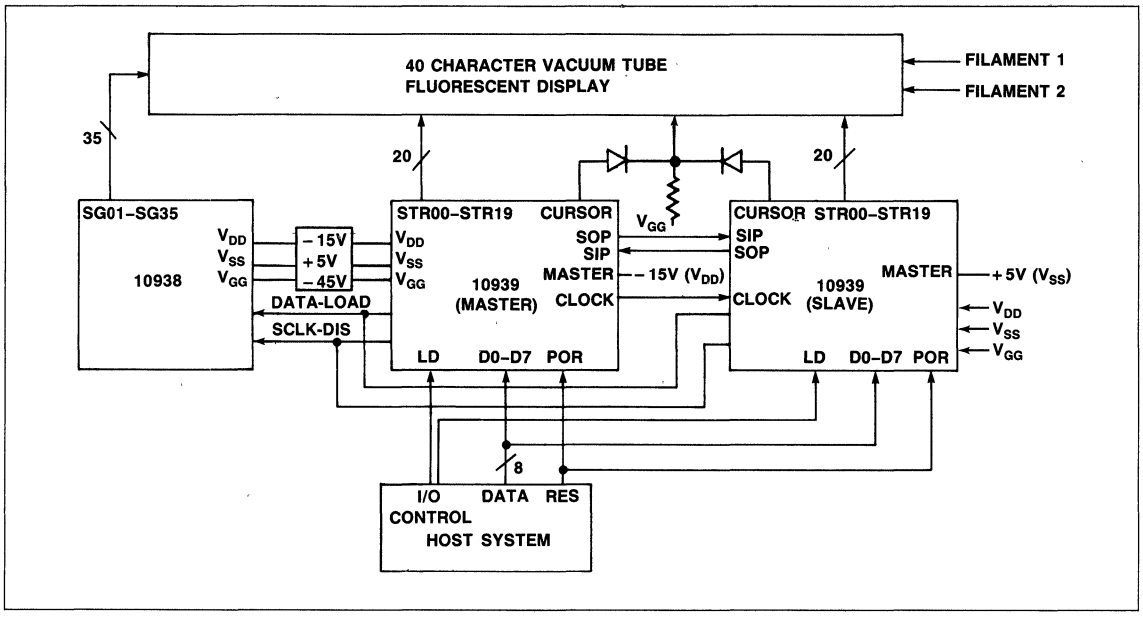

Figure 5. Typical Display System with Parallel Interface to Host and Two 10939 Devices

Rockwell

10939, 10942, AND 10943 DOT MATRIX DISPLAY CONTROLLER

DESCRIPTION

The Rockwell 10939, 10942, and 10943 Dot Matrix Display Controller is a three-chip MOS/LSI general purpose display controller system designed to interface to dot matrix displays (vacuum-fluorescent or LED).

The three-chip set will drive displays with up to 46 anodes (dots) and up to 20 grids (characters) plus a cursor. The chips can be cascaded to drive larger displays of up to 80 characters. An internal PLA-type decoder provides character decoding and dot pattern generation for the full 96-character ASCII set and an additional 32 special characters.

ORDERING INFORMATION

Part Number	Package Type	Temperature Range (°C)
10939P	Plastic	0 to +70
10939PE	Plastic	−40 to +85
10942P	Plastic	0 to +70
10942PE	Plastic	−40 to +85
10943P	Plastic	0 to +70
10943PE	Plastic	−40 to +85

FEATURES

- 20-character display driver cascadable to 80 characters
- Standard 5 × 12 character font. Custom fonts available by special order
- Separate cursor driver output
- Two 128 × 23 PLAs provide decoding for full 96-character ASCII set plus 32 special characters
- Serial or parallel data input for 8-bit display and control characters
- Brightness, refresh rate, and display mode controls
- 10939 provided in 40-pin DIP
- 10942 and 10943 provided in 28-pin DIP

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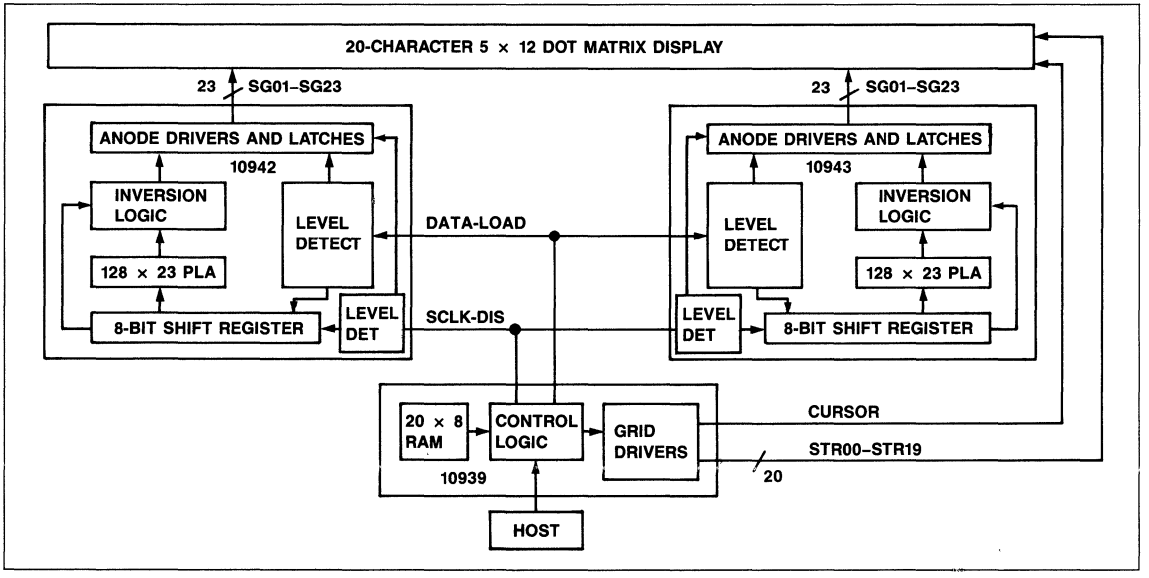
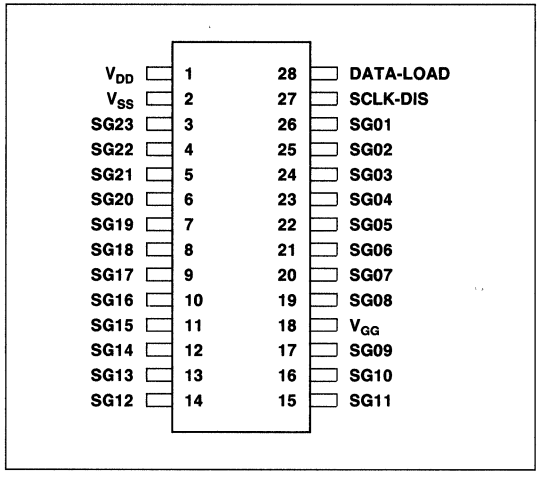


Block Diagram of 10939, 10942, 10943

INTERFACE DESCRIPTION

10942 and 10943 Pin Functions

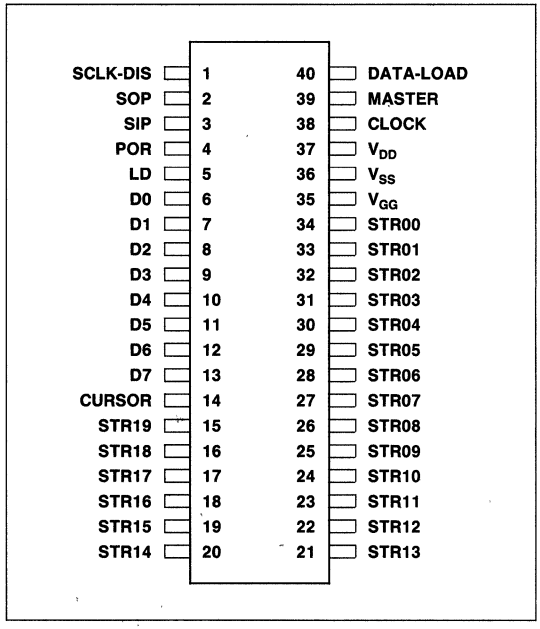
Signal Name	Pin No.	Function
V_{DD}	1	DC Power
V_{SS}	2	Power and signal reference
SG01–SG23	3–17, 19–26	Anode (Dot) driver outputs
V_{GG}	18	Display voltage
SCLK-DIS	27	Serial data shift clock
DATA-LOAD	28	Serial data output/latch control



10942 and 10943 Pin Configurations

10939 Pin Functions

Signal Name	Pin No.	Function
V_{SS}	36	Power and signal reference
V_{DD}	37	DC Power
CLOCK	38	Synchronization Clock
CURSOR	14	Cursor driver output
MASTER	39	Master/Slave Mode control
SIP	3	Sync Input
SOP	2	Sync Output
D0–D7	6–13	Serial or parallel data input
LD	5	Input data strobe
POR	4	Power-on reset
SCLK-DIS	1	Serial data shift clock
DATA-LOAD	40	Serial data output/latch control
STR00–STR19	15–34	Digit (grid) driver outputs
V_{GG}	35	Display voltage



10939 Pin Configurations

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS*

Voltages are referenced to V_{SS}, where V_{SS} = +5 Vdc

Parameter	Symbol	Value	Unit
Operating Temperature	T_A		
Commercial		0 to +70	°C
Industrial		−40 to +85	°C
Storage Temperature	T_S	−55 to +125	°C
Operating Voltage	V_{DD}	−22 to −18 −20 typical	Vdc
Operating Display Voltage	V_{GG}	−50	Vdc

***NOTE:** Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the other sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

(V_{DD} = −18.0 to −22 Vdc, V_{SS} = 0 Vdc, unless otherwise noted. All voltages referenced to V_{SS}.)

Parameter	Symbol	Min.	Typical	Max.	Unit
10942 and 10943					
Output Anodes (Dots)					
Logic "1" (I_{LOAD} = 2 mA)	V_{OH}	−1.5		V_{SS}	V
Logic "0" (I_{LOAD} = 0 mA)	V_{OL}	V_{GG}		0.95 × V_{GG}	V
10939					
Input D0–D7, LD, SIP					
Logic "1"	V_{IH}	−1.2		+0.3	V
Logic "0"	V_{IL}	V_{DD}		−4.2	V
Input POR					
Logic "1"	V_{IHPO}	−3.0		+0.3	V
Logic "0"	V_{ILPO}	V_{DD}		−10.0	V
Output SOP					
Logic "1"	V_{OHSY}	−1.2		V_{SS}	V
Logic "0"	V_{OLSY}	V_{DD}		−4 2	V
Output Digits, Cursor					
Logic "1" (I_{LOAD} = 10 mA)	V_{OH}	−1.5		V_{SS}	V
Logic "0" (I_{LOAD} = 0 mA)	V_{OL}	V_{GG}		0.95 × V_{GG}	V

Note: TA = 0°C to +70°C (commercial) or −40°C to +85°C (industrial), unless otherwise noted.

OPERATING CURRENTS

Parameter	Maximum		Typical	Unit
	Industrial TA = −40°C V_{DD} = −22 Vdc V_{GG} = −50 Vdc	Commercial TA = 0°C V_{DD} = −22 Vdc V_{GG} = −50 Vdc	TA = 25°C V_{DD} = −20 Vdc V_{GG} = −50 Vdc	
10942 or 10943				
I_{DD}	4.5	3.6	3.2	mA
I_{GG}[1]	7.4	5.9	5.3	mA
10939 (master)				
I_{DD}	13.6	10.9	6.0	mA
I_{GG}[2]	1 0	0.8	0 5	mA
10939 (slave)				
I_{DD}	9.1	7.3	4 0	mA
I_{GG}[2]	1 0	0.8	0.5	mA

Notes:

1 The 10942 and 10943 each have 23 driver outputs. I_{GG} is proportional to the number of drivers on. The values given are for all 23 drivers on. Divide I_{GG} shown by 23 to determine I_{GG} for one driver. Multiply I_{GG} by 2 to find total current requirements for all drivers on for both devices.

2 The 10939 will never have more than two drivers on at any one time; one grid driver and the cursor. The values shown are for two drivers on with 100% duty cycle

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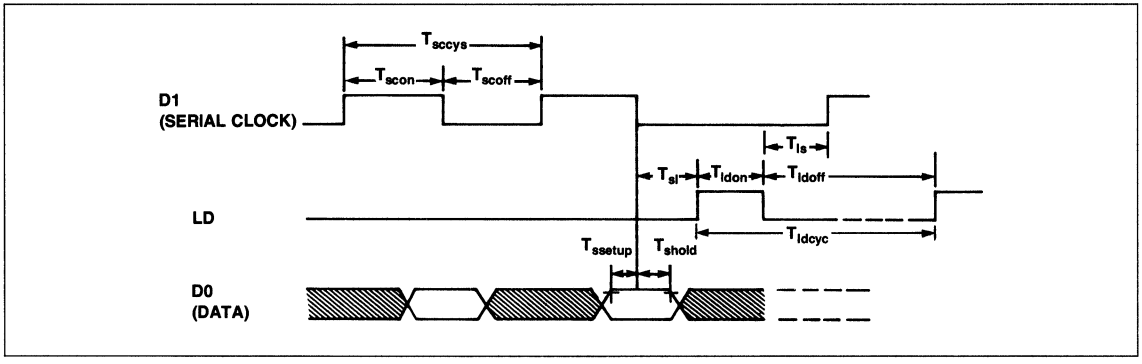
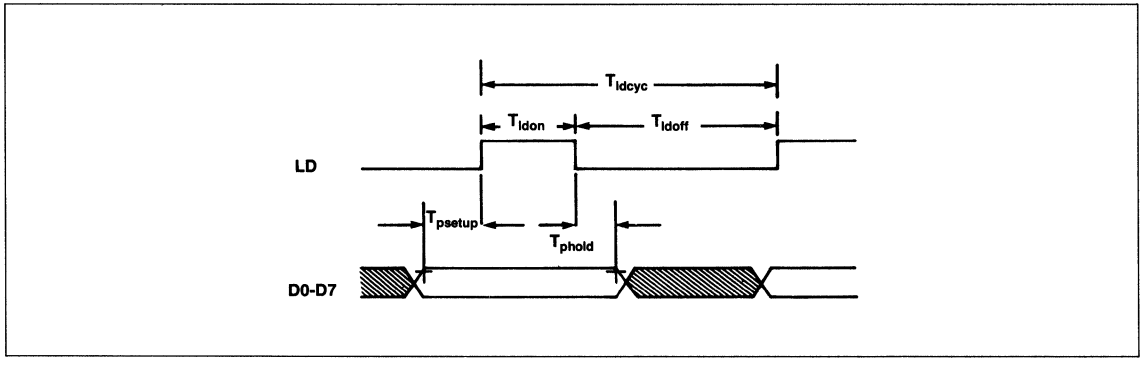
AC CHARACTERISTICS

Parameter	Symbol	Min.	Typical	Max.	Unit
Data Load (LD)					
On Time	T_{ldon}	1.0			µs
Off Time	T_{ldoff}				
Commercial		40.0			µs
Industrial		44.5			µs
Cycle Time	T_{ldcyc}				µs
Commercial		60.0			µs
Industrial		66.7			µs
SERIAL INTERFACE TIMING					
Serial Clock (D1)					
On Time	T_{scon}	1.0		20.0	µs
Off Time	T_{scoff}	1.0			µs
Cycle Time	T_{sccyc}	2.0			µs
Serial Data (D0)					
Set-up time	T_{ssetup}	400			ns
Hold Time	T_{shold}	400			ns
Serial Clock to LD Time	T_{sl}	1.0			µs
LD to Serial Clock	T_{ls}	1.0			µs
PARALLEL INTERFACE TIMING					
Parallel Data (D0–D7)					
Set-up Time	T_{psetup}	0			ns
Hold Time	T_{phold}	200			ns

TIMING WAVEFORMS



Serial Interface Timing Waveforms



Parallel Interface Timing Waveforms

FUNCTIONAL DESCRIPTION

Once the display buffer has been loaded from the host processor, the 10939, 10942, and 10943 system generates all timing signals required to control the display.

Input data is loaded into the Display Data Buffer as a series of 8-bit words via the Serial or Parallel Data Input channel on the 10939. Internal timing and control logic synchronize the digit output signals with the Serial Data and Load signals to the 10942/10943 to provide the proper timing for the multiplexing operation. Two 128 × 23 bit PLAs, one in the 10942 and the other in the 10943, decode the full 96-character ASCII set plus 32 special characters.

The parallel data input mode is implemented by toggling any of data lines D2–D7 after POR has gone low. Once the parallel data load mode has been implemented, a power-on reset procedure must be performed to return to serial data load mode. Parallel data transfer is accomplished by putting the command or display data on the data lines, then pulsing the LD line. The load cycle time must be at least 60 μs with the LD line set high for at least one μs and held low for at least 40 μs.

The serial data input mode is implemented during the power-on reset procedure. In those systems using serial mode, ports D2–D7 should be tied low to prevent the inadvertent implementation of the parallel load mode. Serial data bytes are shifted into a data buffer MSB first on line D0 using line D1 as the serial clock. The last eight bits clocked in are latched into the display controller by a pulse on the LD line. The cycle time for each data bit is 2 μs and the load time for each byte is 60 μs.

Input data may be Control or Display data. The following paragraphs describe the format and functions of these control and display data words.

CONTROL DATA WORDS

Control data words are used to select the operating parameters of the display controller. They must be preceded by a control prefix word (0000 0001, hexadecimal 01) to be distinguished from display data words.

Buffer Pointer Control

The Buffer Pointer Control code sets the Display Data Buffer pointer. The lower 5 bits of the code are loaded into the buffer pointer (see Table 2).

Digit Counter Control

The Digit Counter Control code defines the number of character positions (grids) to be controlled. This code is normally used only during initialization routines, but it may also be used in conjunction with the Duty Cycle Control code to extend the range of brightness control (see Table 3).

Duty Cycle Control

The Duty Cycle Control code is used to turn the display on and off, to adjust display brightness, or to modify display timing. The time slot for each character is 16, 32, or 64 cycles as selected by the Digit Time Control codes (see Table 1). The segment and digit drivers for each character are on for a maximum of 13, 29, or 61 cycles with a 3 cycle inter-digit off-time. The lower 6 bits of the Duty Cycle Control code are loaded into the Duty Cycle Register. Resultant duty cycles are shown in Table 4.

Table 1. Control Word Assignments

Hex Value	Function
00	Not Used
01	Load 01 into Data Buffer
02	Not used
03	Not used
04	Not used
05	Set Digit Time to 16 cycles per grid
06	Set Digit Time to 32 cycles per grid
07	Set Digit Time to 64 cycles per grid
08	Enable Normal Display Mode (MSB in data words is ignored
09	Enable Blank Mode (data words with MSB = 1 will be blanked)
0A	Enable Inverse Mode (data words with MSB = 1 will be "inversed")
0B	Not used
0C	Not used
0D	Not used
0E	Start Display Refresh Cycle (use only once after reset)
0F	Not used
10–3F	Not used
40–7F	Load Duty Cycle Register
80–9F	Load Digit Counter (80 = 32, 81 = 1, 82 = 2, etc.)
A0–BF	Not used
C0–DF	Load Buffer Pointer Register with lower 5 bits
E0–FF	Not used

Table 2. Buffer Pointer Control Codes

Code Value	Pointer Value	Character Position
C0	00	0
C1	01	1
C2	02	2
C3	03	3
C4	04	4
C5	05	5
C6	06	6
C7	07	7
C8	08	8
C9	09	9
CA	0A	10
CB	0B	11
CC	0C	12
CD	0D	13
CE	0E	14
CF	0F	15
D0	10	16
D1	11	17
D2	12	18
D3	13	19

Note: Do not use character positions 20–31 (Codes D4-DF)

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Table 3. Digit Counter Control Codes

Code	Digit Counter Value	No. of Grids Controlled
80	00	32
81	01	1
82	02	2
83	03	3
84	04	4
85	05	5
86	06	6
87	07	7
88	08	8
89	09	9
8A	0A	10
8B	0B	11
8C	0C	12
8D	0D	13
8E	0E	14
8F	0F	15
90	10	16
91	11	17
92	12	18
93	13	19
94	14	20
95	15	21
96	16	22
97	17	23
98	18	24
99	19	25
9A	1A	26
9B	1B	27
9C	1C	28
9D	1D	29
9E	1E	30
9F	1F	31

Digit Time Select

The Digit Time Select code sets the total time for each character during the refresh cycle. Three values can be set using the three codes shown in Table 1. The default value set at power-on is 64 cycles per grid. For displays with 40 or more characters,or under conditions where the display can be subjected to quick movements during viewing (e.g. portable or vehicle-mounted applications), it may be necessary to increase the refresh rate by selecting 16 or 32 cycles per grid with the appropriate control code.

Display Mode Select

Each ASCII character is represented by the lower seven bits of the 8-bit value loaded into the 10939. The eighth (most significant) bit is used to turn the cursor (see Cursor Control) on in Normal display mode. If either Blank or Inverse mode is selected, a "0" in this bit causes a normal character display mode, while a "1" selects either Blank or Inverse mode, depending on which mode is enabled. Three control codes are provided (see Table 1) to Enable Blank mode, Enable Inverse mode, or Enable Normal display mode.

In the Blank mode, any character with the MSB = "1" will be blanked. In the Inverse mode, it will be displayed with all segment driver outputs inverted. On video displays, this is referred to as "Inverse Video" format. These controls allow individual characters or groups of characters to be blinked or blanked by simply changing the mode without changing the data in the Display Buffer.

Table 4. Duty Cycle Control Codes

	Digit Time = 16		Digit Time = 32		Digit Time = 64	
Code	On	Off	On	Off	On	Off
40	—	16	—	32	—	64
41	—	16	—	32	—	64
42	—	16	—	32	—	64
43	1	15	1	31	1	63
44	2	14	2	30	2	62
45	3	13	3	29	3	61
46	4	12	4	28	4	60
47	5	11	5	27	5	59
48	6	10	6	26	6	58
49	7	9	7	26	7	57
4A	8	8	8	24	8	56
4B	9	7	9	23	9	55
4C	10	6	10	22	10	54
4D	11	5	11	21	11	53
4E	12	4	12	20	12	52
4F	13	3	13	19	13	51
50	13	3	14	18	14	50
51	13	3	15	17	15	49
52	13	3	16	16	16	48
53	13	3	17	15	17	47
.	.	.	.	.	.	.
.	.		.	.		.
.			.	.	.	.
5B	13	3	25	7	25	39
5C	13	3	26	6	26	38
5D	13	3	27	5	27	37
5E	13	3	28	4	28	36
5F	13	3	29	3	29	35
60	13	3	29	3	30	34
61	13	3	29	3	31	33
62	13	3	29	3	32	32
.	.				.	.
.	.	.			.	.
.	.				.	.
7C	13	3	29	3	58	6
7D	13	3	29	3	59	5
7E	13	3	29	3	60	4
7F	13	3	29	3	61	3

Cursor Control

The data byte control (MSB 8), besides selecting Blank, Inverse, or Normal mode, also controls the cursor output which is enabled on all characters with the MSB equal to one. Therefore, when the Normal mode is enabled and the MSB of the data byte is set to a one, the normal character is displayed with the cursor on. When the Blank mode is enabled and the MSB is set to a one, the character is blanked but the cursor is on. If Inverse mode is enabled and the MSB is set to a one, the inverse character is displayed, and the cursor is on but not inversed.

Start Refresh

At power on, the 10939 is held in an internal halt mode. The normal display refresh sequence starts upon receipt of a Start Refresh control code. This is particularly useful for synchronizing systems using more than one 10939. Only the Master 10939 in a multi-chip system will recognize the Start Refresh code. The Master starts the Slave(s) at the appropriate time, using the SOP signal.

INPUT DISPLAY DATA WORDS

Display data words are loaded as 8-bit codes. The eighth (most significant) bit is a dual purpose bit. This bit specifies normal (0) or blank/inverse (1) display mode, depending on the blank/inverse mode selection (see control data words 09 and 0A in Table 1). It also controls the cursor output from the 10939; on (1) or off (0). Note, that this bit always controls the cursor no matter what display mode is selected.

Twenty display data words must be entered to completely load the Display Data Buffer. The Buffer Pointer automatically increments after each data word is stored in the buffer. To select a character position to be loaded out of sequence, use the Buffer Pointer Control code command. The Buffer Pointer will automatically reset to character position 0 when its value is equal to the programmed Digit Counter.

DIGIT GRID DRIVERS (STR00–STR19) PLUS CURSOR

The 20 Digit Drivers select each of the display character positions sequentially during a refresh scan. Display dots are illuminated when both the Digit Drivers and Anode (Dot) Drivers for a particular character are energized simultaneously. The Cursor output is generated by the 10939, but its timing characteristics are identical to the 46 segment outputs generated by the 10942 and the 10943.

ANODE (DOT) DRIVERS (SG01–SG23)

A total of 46 Dot Drivers are provided by the 10942 and the 10943. The output states for each ASCII charcter pattern are internally decoded from the 8-bit characters received from the 10939 by means of two 128 × 23-bit PLAs, one in the 10942 and the other in the 10943. Figure 1 shows the dot matrix drivers (SG01–SG23) as they relate to the 10942 and 10943. Data codes and the corresponding character patterns are also shown in Figure 1.

POWER-ON RESET

The Power-On Reset (POR) initializes the internal circuits of the 10939. This is normally accomplished when power (V_{DD}) is applied. The following conditions are established by the application of POR:

a. The Grid Drivers (STR00–STR19) on the 10939 are in the off state.

b. The Anode Drivers, SG01–SG23 on the 10942 and SG01–SG23 on the 10943, are in the off state.

c. The Duty Cycle is set to 0.

d. The Digit Counter is set to 32.

e. The Buffer Pointer is set to 0.

f. The Digit time is set to 64.

g. The Normal display mode is set.

h. DATA-LOAD is set to high impedance state.

i. SCLK-DIS is set to V_{OL} to disable the anode drivers in the 10942 and 10943.

j. SOP is set to V_{OL} to disable the sync pulse.

NOTE:

1. When th POR signal is removed, SCLK-DIS is set to the high impedance state.
2. During the initial rise time of V_{DD} at power turn-on, the magnitude of V_{GG} should not exceed the magnitude of V_{DD}.

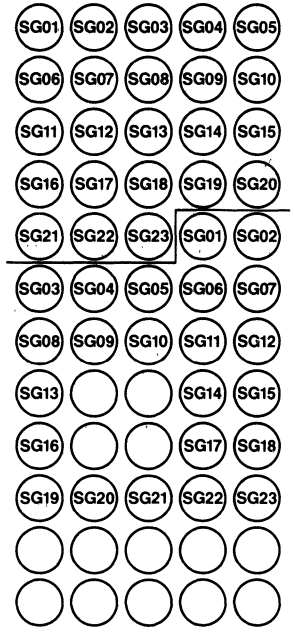
TYPICAL SYSTEM HOOKUPS

Figure 2 shows a 10939, 10942, and a 10943 in a parallel interface with the host system driving a 20-character display. Figure 3 shows a 10939, 10942, and a 10943 in a serial interface with the host system driving a 20-character display. Figure 4 shows two 10939s, a 10942, and a 10943 in a parallel interface with the host system driving a 40-character display.

5

Input Data	Character	Input Data	Character	Input Data	Character	Input Data	Character	Input Data	Character	Input Data	Character	Input Data	Character	Input Data	Character
00		01		02		03		04		05		06		07	
08		09		0A		0B		0C		0D		0E		0F	
10		11		12		13		14		15		16		17	
18		19		1A		1B		1C		1D		1E		1F	
20		21		22		23		24		25		26		27	
28		29		2A		2B		2C		2D		2E		2F	
30		31		32		33		34		35		36		37	
38		39		3A		3B		3C		3D		3E		3F	
40		41		42		43		44		45		46		47	
48		49		4A		4B		4C		4D		4E		4F	
50		51		52		53		54		55		56		57	
58		59		5A		5B		5C		5D		5E		5F	
60		61		62		63		64		65		66		67	
68		69		6A		6B		6C		6D		6E		6F	
70		71		72		73		74		75		76		77	
78		79		7A		7B		7C		7D		7E		7F	

Segments Driven By 10942



Segments Driven By 10943

10942 and 10943 Driver Assignments

Figure 1. 5 x 12 Dot Matrix PLA Patterns and Driver Assignments

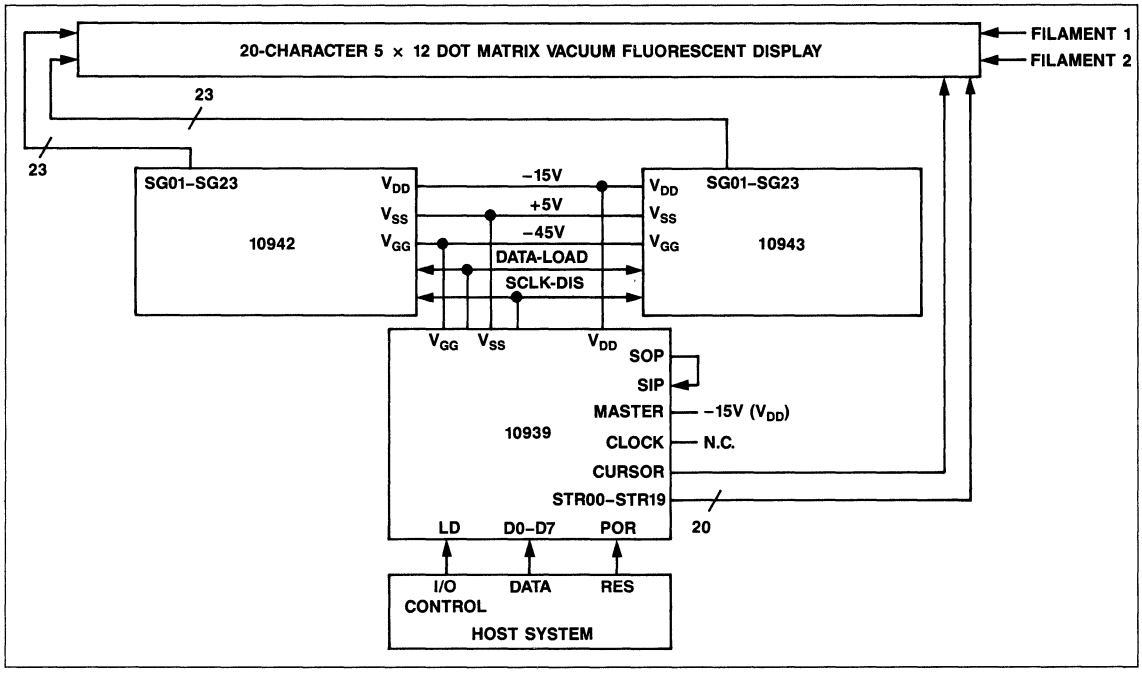


Figure 2. Typical Display System with Parallel Interface to Host System

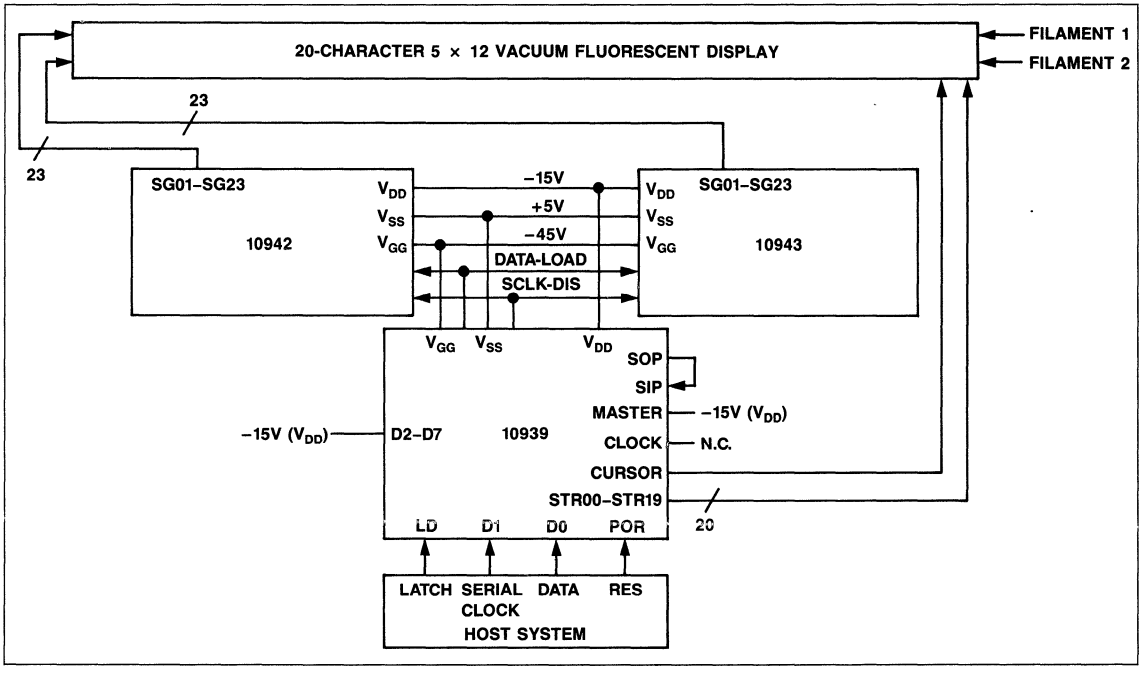


Figure 3. Typical Display System with Serial Interface to Host System

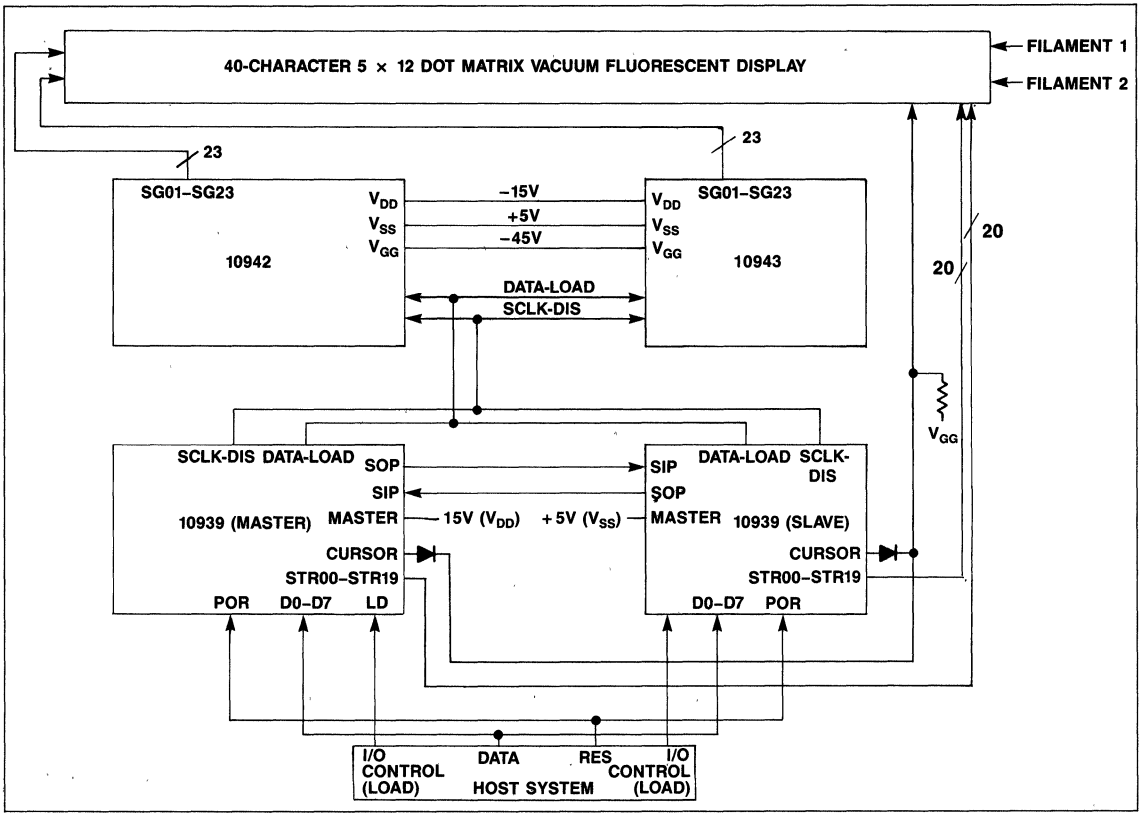


Figure 4. Typical Display System with Parallel Interface to Host and Two 10939 Devices

Rockwell

10941 AND 10939 ALPHANUMERIC AND BARGRAPH DISPLAY CONTROLLER

DESCRIPTION

The Rockwell 10939 and 10941 Alphanumeric and Bargraph Display Controller is a two-chip MOS/LSI general purpose display controller system designed to interface with bargraph and segmented displays (vacuum-fluorescent or LED).

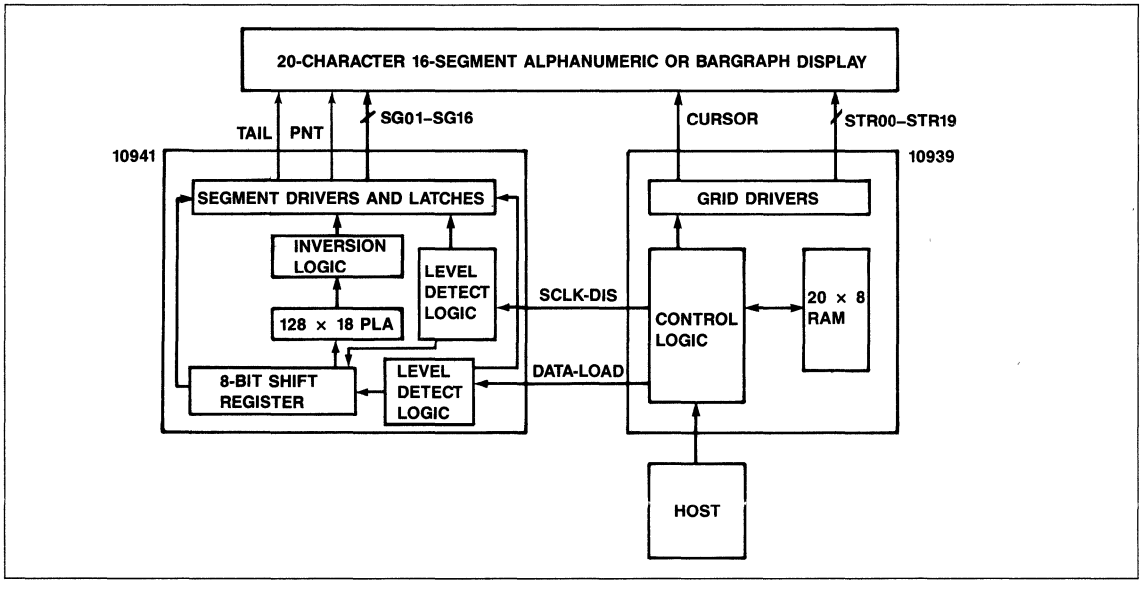
The two-chip set will drive displays with up to 16 segments (plus decimal point and comma tail) and up to 20 grids (characters) plus a cursor. The chips can be cascaded to drive larger displays of 80 characters. Segment decoding for ASCII characters and bargraph patterns is accomplished through an internal PLA.

FEATURES

- 20-character display driver cascadable to 80 characters
- Direct drive capability for vacuum-fluorescent displays
- 128 x 18 PLA provides segment decoding for ASCII characters (all caps only) and bargraph patterns
- Serial or parallel data input for 8-bit display and control characters
- Brightness, refresh rate, and display mode controls
- Separate cursor driver output
- 10939—40-pin DIP package
- 10941—24-pin DIP package

ORDERING INFORMATION

Part Number	Package Type	Temperature Range (°C)
10941P	Plastic	0 to +70
10941PE	Plastic	−40 to +85
10939P	Plastic	0 to +70
10939PE	Plastic	−40 to +85

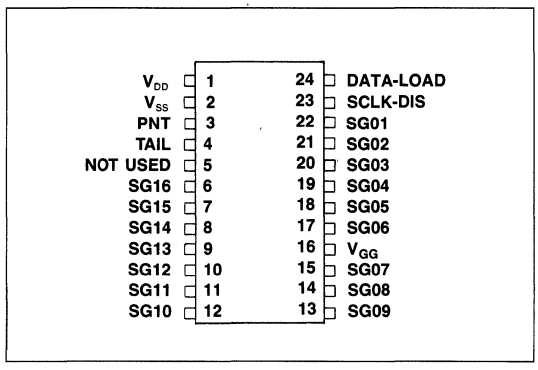


Block Diagram of 10941 and 10939

INTERFACE DESCRIPTION

10941 Pin Functions

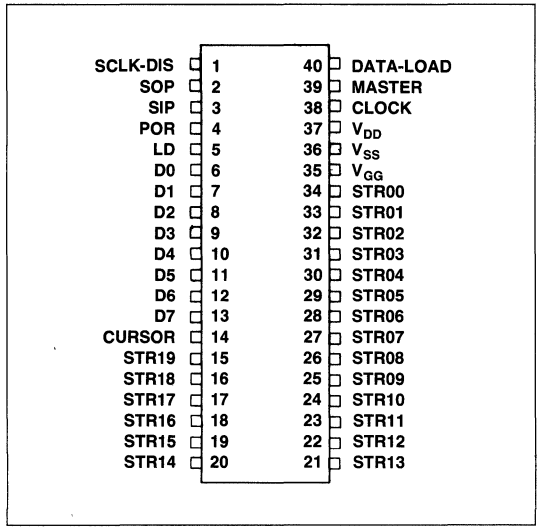
Signal Name	Pin No.	Function
V_{SS}	2	Power and signal reference
SG01-SG16	6-15, 17-22	Segment driver outputs
SCLK-DIS	23	Serial data shift
DATA-LOAD	24	Serial data output/latch control
PNT	4	Decimal Point driver output
TAIL	5	Comma Tail driver output
V_{DD}	1	DC Power
V_{GG}	16	Display voltage



10941 Pin Configuration

10939 Pin Functions

Signal Name	Pin No.	Function
V_{SS}	36	Power and signal reference
V_{DD}	37	DC Power
CLOCK	38	Synchronization Clock
CURSOR	14	Cursor driver output
MASTER	39	Master/Slave Mode control
SIP	3	Sync Input
SOP	2	Sync Output
D0-D7	6-13	Serial or parallel data input
LD	5	Input data strobe
POR	4	Power-on reset
SCLK-DIS	1	Serial data shift clock
DATA-LOAD	40	Serial data output/latch control
STR00-STR19	15-34	Grid Driver Outputs
V_{GG}	35	Display voltage



10939 Pin Configuration

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS*

Voltages are referenced to V_{SS}

Parameter	Symbol	Value	Unit
Operating Temperature			
Commercial		0 to +70	°C
Industrial	Tc	−40 to +85	°C
Storage Temperature	TI	−55 to +125	°C
Operating Voltage	V_{DD}	−22 to −18 −20 (typical)	Vdc
Operating Display Voltage	V_{GG}	−50	Vdc

***NOTE:** Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in other sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

All voltages referenced to V_{SS}

Parameter	Symbol	Min	Typ	Max	Unit
10941					
Output Segments					
Logic "1" (I_{load} = 2 mA)	V_{OH}	−1.5		V_{SS}	V
Logic "1" (I_{LOAD} = 0 mA)	V_{OL}	V_{GG}		0.95 × V_{GG}	V
10939					
Input D0-D7, LD, SIP					
Logic "1"	V_{IH}	−1.2		+0 3	V
Logic "0"	V_{IL}	V_{DD}		−4.2	V
Input POR					
Logic "1"	V_{IHPO}	−3.0		+0.3	V
Logic "0"	V_{ILPO}	V_{DD}		−10.0	V
Output SOP					
Logic "1"	V_{OHSY}	−1.2		V_{SS}	V
Logic "0"	V_{OLSY}	V_{DD}		−4.2	V
Output Digits, Cursor					
Logic "1" (I_{load} = 10 mA)	V_{OH}	−1.5		V_{SS}	V
Logic "0" (I_{load} = 0 mA)	V_{OL}	V_{GG}		0.95 × V_{GG}	V

OPERATING CURRENTS

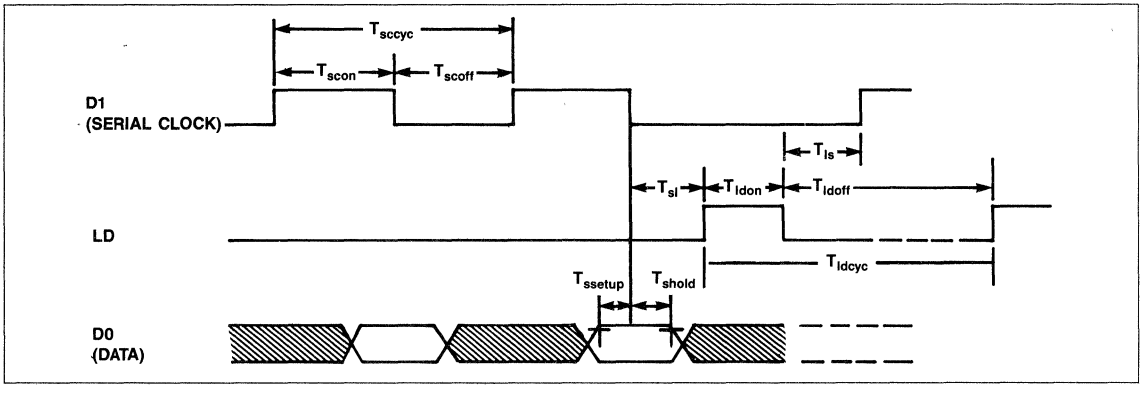
Parameter	Notes	Maximum		Typical	Unit
		Industrial TA = −40°C V_{DD} = −22 Vdc V_{GG} = −50 Vdc	**Commercial** TA = 0°C V_{DD} = −22 Vdc V_{GG} = −50 Vdc	TA = 25°C V_{DD} = −20 Vdc V_{GG} = −50 Vdc	
10941					
I_{DD}	1	4.5	3.6	3 2	mA
I_{GG}		5.7	4.6	2 9	mA
10939 (master)					
I_{DD}	2	13 6	10.9	6 0	mA
I_{GG}		1.0	0.8	0 5	mA
10939 (slave)					
I_{DD}	2	9.1	7.3	4 0	mA
I_{GG}		1.0	0.8	0.5	mA

Notes:
1. The 10941 has 18 internal drivers which are brought out I_{GG} is proportional to the number of drivers on. The values given are for all 18 drivers on. Divide I_{GG} shown by 18 to determine I_{GG} for one driver.
2. The 10939 will never have more than two drivers on at any one time; one grid driver and the cursor. The values shown are for two drivers on with 100% duty cycle.

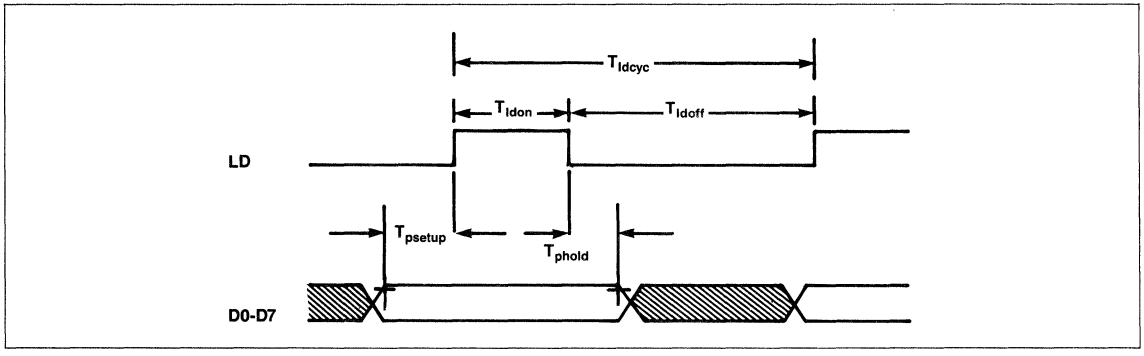
AC CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Unit
GENERAL INTERFACE TIMING					
Data Load (LD)					
On Time	T_{ldon}	1.0			µs
Off time	T_{ldoff}				
Commercial		40.0			µs
Industrial		44.5			µs
Cycle Time	T_{ldcyc}				
Commerical		60.0			µs
Industrial		66.7			µs
SERIAL INTERFACE TIMING					
Serial Clock (D1)					
On Time	T_{scon}	1 0		20.0	µs
Off Time	T_{scoff}	1.0			µs
Cycle Time	T_{sccyc}	2 0			µs
Serial Data (D0)					
Set-up Time	T_{ssetup}	400			ns
Hold Time	T_{shold}	400			ns
Serial Clock to LD Time	T_{sl}	1 0			µs
LD to Serial Clock	T_{ls}	1.0			µs
PARALLEL INTERFACE TIMING					
Parallel Data (D0–D7)					
Set-up Time	T_{psetup}	0			ns
Hold Time	T_{phold}	200			ns

TIMING WAVEFORMS



Serial Interface Timing Waveforms



Parallel Interface Timing Waveforms

FUNCTIONAL DESCRIPTION

Once the display buffer has been loaded from the host processor, the 10941/10939 system generates all timing signals required to control the display.

Input data is loaded into the Display Data Buffer as a series of 8-bit words via the Serial or Parallel Data Input channel on the 10939. Internal timing and control logic synchronize the digit output signals with the Serial Data and Load signals to the 10941 to provide the proper timing for the multiplexing operation. A 128 x 18 bit PLA is provided for decoding the character set and bargraph codes.

The parallel data input mode is implemented by toggling any of data lines D2–D7 after POR has gone low. Once the parallel data load mode has been implemented, a power-on reset procedure must be performed to return to serial data load mode. Parallel data transfer is accomplished by putting the command or display data on the data lines, then pulsing the LD line. The load cycle time must be at least 60 μs with the LD line set high for at least one μs and held low for at least 40 μs.

The serial data input mode is implemented during the power-on reset procedure. In those systems using serial mode, ports D2–D7 should be tied low to prevent the inadvertent implementation of the parallel load mode. Serial data bytes are shifted into a data buffer MSB first on line D0 using line D1 as the serial clock. The last eight bits clocked in are latched into the display controller by a pulse on the LD line. The cycle time for each data bit is 2 μs and the load time for each byte is 60 μs.

Input data may be Control or Display data. The following paragraphs describe the format and functions of these control and display data words.

CONTROL DATA WORDS

Control data words are used to select the operating parameters of the display controller. They must be preceded by a Control Prefix word (0000 0001, hexadecimal 01) to be distinguished from Display Data words. Table 1. shows the Control Word code assignments and functions.

Buffer Pointer Control

The Buffer Pointer Control code sets the Display Data Buffer pointer. The lower 5 bits of the code are loaded into the buffer pointer (see Table 2).

Table 1. Control Word Assignments

Hex Value	Function
00	Not used
01	Load 01 into Data Buffer
02	Not used
03	Not used
04	Not used
05	Set digit time to 16 cycles per grid
06	Set digit time to 32 cycles per grid
07	Set digit time to 64 cycles per grid
08	Enable Normal Display Mode (MSB in data words is cursor control only)
09	Enable Blank Mode (data words with MSB = 1 will be blanked and cursor will be on)
0A	Enable Inverse Mode (data words with MSB = 1 will be "inversed" and cursor will be on)
0B	Not used
0C	Not used
0D	Not used
0E	Start Display Refresh Cycle (use only once after reset)
0F	Not used
10–3F	Not used
40–7F	Load Duty Cycle Register with lower 6 bits (0–63)
80–9F	Load Digit Counter (80 = 32, 81 = 1, 82 = 2, etc.)
A0–BF	Not used
C0–DF	Load Buffer Pointer Register with lower 5 bits
E0–FF	Not used

Table 2. Buffer Pointer Control Codes

Code Value	Pointer Value	Character Position
C0	00	0
C1	01	1
C2	02	2
C3	03	3
C4	04	4
C5	05	5
C6	06	6
C7	07	7
C8	08	8
C9	09	9
CA	0A	10
CB	0B	11
CC	0C	12
CD	0D	13
CE	0E	14
CF	0F	15
D0	10	16
D1	11	17
D2	12	18
D3	13	19

Note:
DO NOT USE CHARACTER POSITIONS 20–31 (Codes D4–DF).

5

Digit Counter Control

The Digit Counter Control code defines the number of character positions (grids) to be controlled. This code is normally used only during initialization routines, but it may also be used in conjunction with the Load Duty Cycle control code to extend the range of brightness control (see Table 3).

Duty Cycle Control

The Duty Cycle Control code turns the display on and off, adjusts display brightness, or modifies display timing. The time slot for each character is 16, 32, or 64 cycles as selected by the Digit Time Control codes (see Table 3). The segment and digit drivers for each character are on for a maximum of 13, 29, or 61 cycles with a 3 cycle inter-digit off-time. The lower 6 bits of the Duty Cycle Control code are loaded into the Duty Cycle Register. Resultant duty cycles are shown in Table 4.

Digit Time Select

The Digit Time Select code sets the total time for each character during the refresh cycle. Three values can be set using the three codes shown in Table 1. The default value set at power-on is 64 cycles per grid. For displays with 40 or more character, or under conditions where the display can be subjected to quick movements during viewing (e.g. portable or vehicle-mounted applications), it may be necessary to increase the refresh rate by selecting 16 or 32 cycles per grid with the appropriate control code.

Table 3. Digit Counter Control Codes

Code	Digit Counter Value	No. of Grids Controlled
80	00	32
81	01	1
82	02	2
83	03	3
84	04	4
85	05	5
86	06	6
87	07	7
88	08	8
89	09	9
8A	0A	10
8B	0B	11
8C	0C	12
8D	0D	13
8E	0E	14
8F	0F	15
90	10	16
91	11	17
92	12	18
93	13	19
94	14	20
95	15	21
96	16	22
97	17	23
98	18	24
99	19	25
9A	1A	26
9B	1B	27
9C	1C	28
9D	1D	29
9E	1E	30
9F	1F	31

Display Mode Select

Each ASCII character is represented by the lower seven bits of the 8-bit value loaded into the 10939. The eighth (most significant) bit controls the cursor (see Cursor Control). This bit is known as the data byte control bit. If either Blank or Inverse mode is selected, a "0" in this bit causes a normal character display, while a "1" selects either Blank or Inverse mode, depending on which mode is enabled. Three control codes are provided (see Table 1) to Enable Blank mode, Enable Inverse mode, or Enable Normal Display mode.

Table 4. Duty Cycle Control Codes

	Digit Time = 16		Digit Time = 32		Digit Time = 64	
Code	On	Off	On	Off	On	Off
40	—	16	—	32	—	64
41	—	16	—	32	—	64
42	—	16	—	32	—	64
43	1	15	1	31	1	63
44	2	14	2	30	2	62
45	3	13	3	29	3	61
46	4	12	4	28	4	60
47	5	11	5	27	5	59
48	6	10	6	26	6	58
49	7	9	7	25	7	57
4A	8	8	8	24	8	56
4B	9	7	9	23	9	55
4C	10	6	10	22	10	54
4D	11	5	11	21	11	53
4E	12	4	12	20	12	52
4F	13	3	13	19	13	51
50	13	3	14	18	14	50
51	13	3	15	17	15	49
52	13	3	16	16	16	48
53	13	3	17	15	17	47
.	.	.	.	.	.	.
.	.	.	.	.	.	.
5B	13	3	25	7	25	39
5C	13	3	26	6	26	38
5D	13	3	27	5	27	37
5E	13	3	28	4	28	36
5F	13	3	29	3	29	35
60	13	3	29	3	30	34
61	13	3	29	3	31	33
62	13	3	29	3	32	32
.	.	.	.	.	.	.
.	.	.	.	.	.	.
7C	13	3	29	3	58	6
7D	13	3	29	3	59	5
7E	13	3	29	3	60	4
7F	13	3	29	3	61	3

In the Blank mode, any character with the MSB = "1" will be blanked. In the Inverse mode, it will be displayed with all segment driver outputs inverted. On video displays, this is referred to as "Inverse Video" format. These controls allow individual characters or groups of characters to be blinked or blanked by simply changing the mode without changing the data in the Display Buffer.

Cursor Control

The data byte control bit (MSB 8), besides selecting Blank, Inverse, or Normal mode, also controls the cursor output which is enabled on all characters with the MSB equal to one. Therefore, when the Normal mode is enabled and the MSB of the data byte is set to a one, the normal character is displayed with the cursor on. When the Blank mode is enabled and the MSB is set to a one, the character is blanked but the cursor is on. If Inverse mode is enabled and the MSB is set to a one, the inverse character is displayed and the cursor is on but not inversed.

Start Refresh

At power on, the 10939 is held in an internal halt mode. The normal display refresh sequence starts upon receipt of a Start Refresh control code. This is particularly useful for synchronizing systems using more than one 10939. Only the Master 10939 in a multi-chip system will recognize the Start Refresh code. The Master starts the Slave(s) at the appropriate time, using the SOP signal.

INPUT DISPLAY DATA WORDS

Display data words are loaded as 8-bit codes. The eighth (most significant) bit specifies normal (0) or blank/inverse (1) display mode, depending on the blank/inverse mode selection (see Control data words 09 and 0A in Table 1). This bit also controls the cursor.

Twenty display data words must be entered to completely load the Display Data Buffer. The Buffer Pointer automatically increments after each data word is stored in the buffer. To select a character position to be loaded out of sequence, use the Buffer Pointer control code. The Buffer Pointer will automatically reset to character position 0 when its value is equal to the programmed Digit Count.

POWER-ON RESET

The Power-On Reset (POR) initializes the internal circuits of the 10939. This is normally accomplished when power (V_{DD}) is applied. The following conditions are established by application of POR:

a. The Grid Drivers (STR00–STR19) on the 10939 are in the off state.
b. The Segment Drivers (SG01–SG16) on the 10941 are in the off state.
c. The Duty Cycle is set to 0.
d. The Digit Counter is set to 32.
e. The Buffer Pointer is set to 0.
f. The Digit time is set to 64.
g. The Normal display mode is set.
h. DATA-LOAD is set to high impedance state.
i. SCLK-DIS is set to V_{OL} to disable the anode drivers in the 10941.
j. SOP is set to V_{OL} to disable the sync pulse.

Note:
1. When the POR signal is removed, SCLK-DIS is set to the high impedance state.
2. During the initial rise time of V_{DD} at power turn-on, the magnitude of V_{GG} should not exceed the magnitude of V_{DD}.

DIGIT (GRID) DRIVERS (STR00–STR19) PLUS CURSOR

The 20 Digit (Grid) Drivers select each of the display character positions sequentially during a refresh scan. Display segments are illuminated when both the Digit Drivers and Segment Drivers for a particular character are energized simultaneously. The Cursor segment is generated by the 10939, but its timing characteristics are identical to the 16 segments generated by the 10941.

SEGMENT (ANODE) DRIVERS (SG01–SG16, PNT, TAIL)

Eighteen Segment (Anode) Drivers are provided in the 10941. The output states for each character pattern and each bargraph pattern are internally decoded from the 8-bit characters received from the 10939 by means of a 128 × 18-bit PLA. Data codes and the corresponding segment patterns are shown in Figure 1. Data codes and the corresponding bargraph patterns are shown in Figure 2.

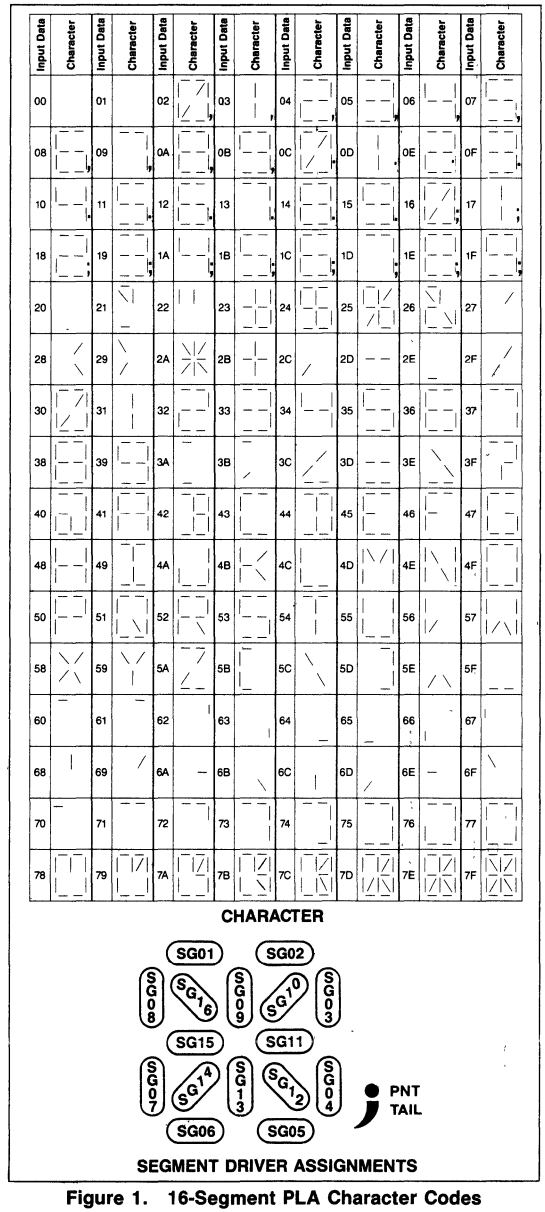


Figure 1. 16-Segment PLA Character Codes

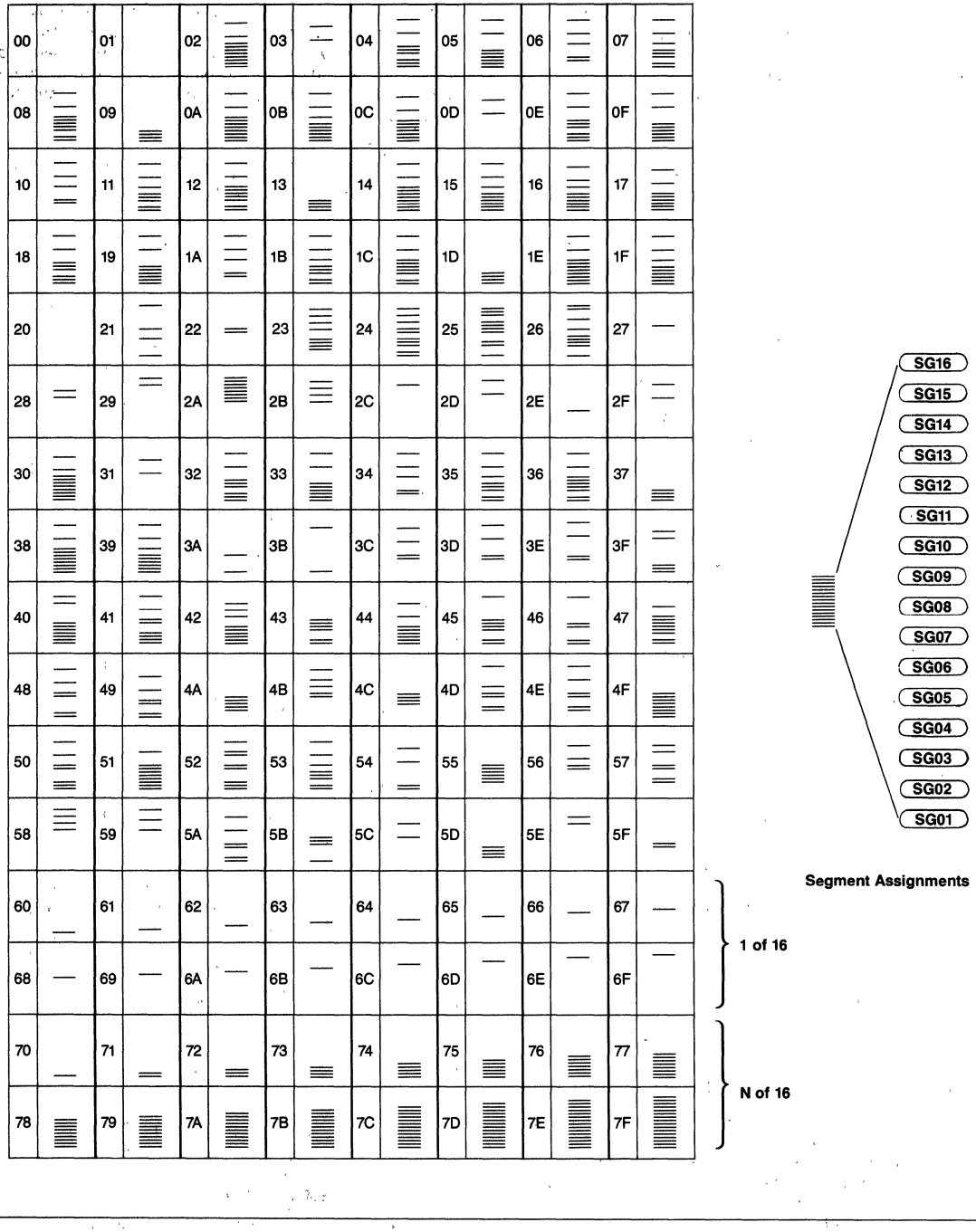


Figure 2. 16-Segment BarGraph Codes

TYPICAL SYSTEM HOOKUPS

Figure 3 shows a 10941 and 10939 in a parallel interface with the host system driving a 20 character display. Figure 4 shows a 10941 and a 10939 in a serial interface with the host system driving a 20 character display. Figure 5 shows a 10941 and two 10939's in a parallel interface with the host system driving a 40 character display.

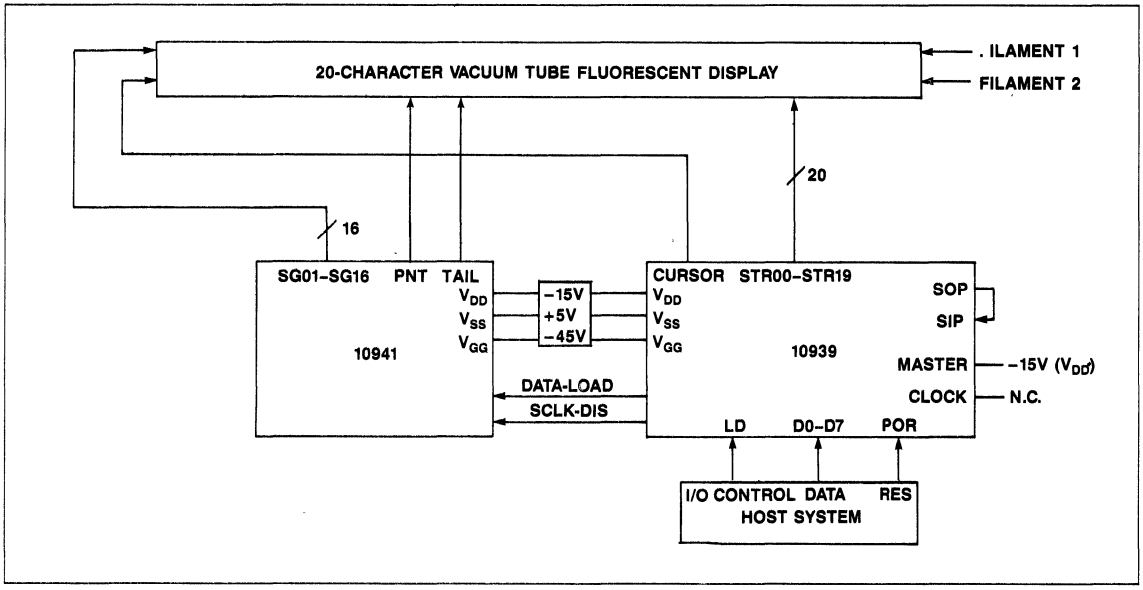


Figure 3. Typical Display System with Parallel Interface to Host System

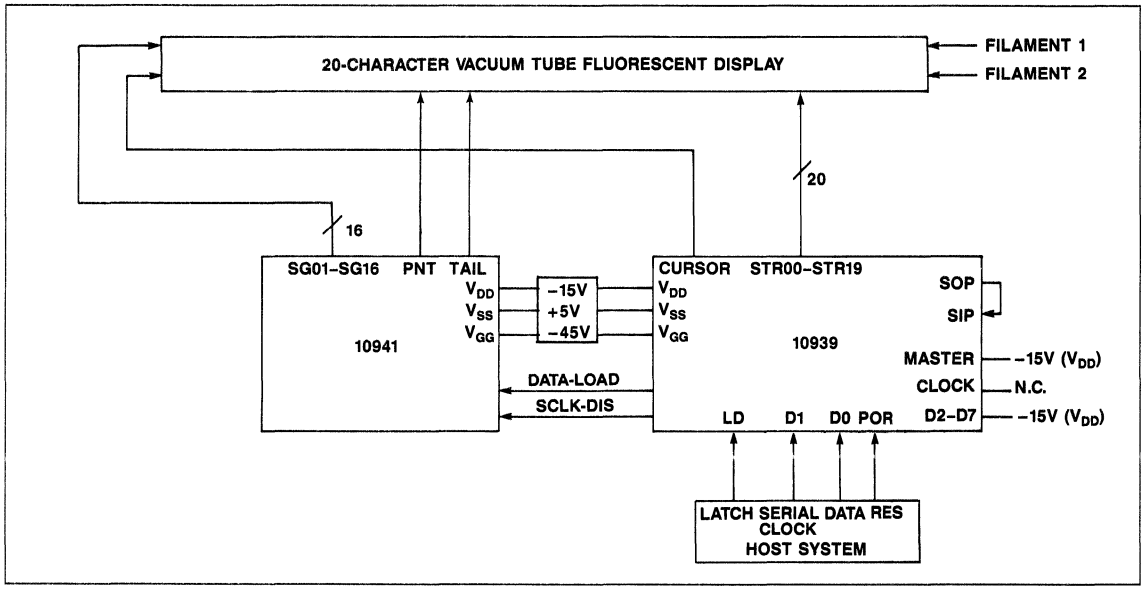


Figure 4. Typical Display System with Serial Interface to Host System

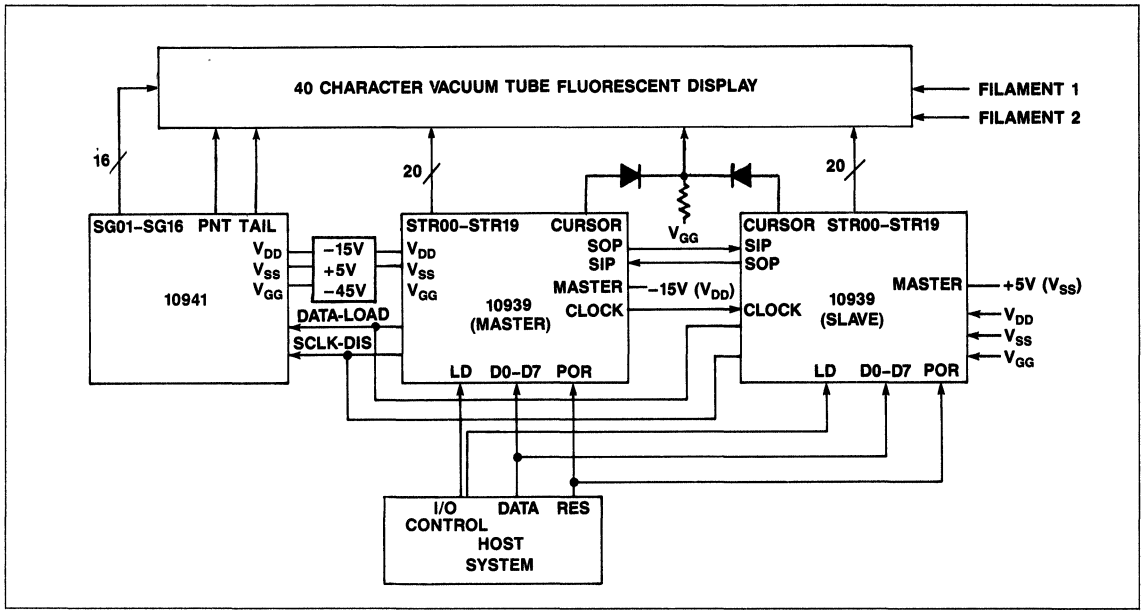


Figure 5. Typical Display System with Parallel Interface to Host and Two 10939 Devices

Rockwell

10951
BARGRAPH AND NUMERIC DISPLAY CONTROLLER

PRELIMINARY

DESCRIPTION

The Rockwell 10951 Bargraph and Numeric Display Controller is an LSI general purpose display controller designed to interface to bargraph and numeric displays (vacuum fluorescent or LED).

The 10951 will drive 16-segment bargraph or seven-segment plus comma and decimal numeric displays with up to 16 display positions. The controller accepts command and data input words on a clocked serial input line. Commands control the on/off duty cycle, starting character position and number of characters to display. Encoded data words display bargraph position (single segment or increasing bar length), numbers, comma, decimal and selected upper and lower case letters. No external drive circuitry is required for displays that operate on 20 mA of drive current up to 50 volts. A 64 × 16-bit segment decoder provides character set decoding for the display.

ORDERING INFORMATION

Part Number	Package Type	Drive Voltage	Temperature Range (°C)
10951P-40	Plastic	40V	0 to +70
10951P-50	Plastic	50V	0 to +70
10951PE-40	Plastic	40V	−40 to +85
10951PE-50	Plastic	50V	−40 to +85

FEATURES

- 16 segment drivers plus decimal point and comma tail drivers
- 16 digit drivers
- Up to 66 kHz data rate
- TTL compatible
- Direct digit drive of 20 mA for up to 50 volt displays
- Supports vacuum fluorescent or LED displays
- Serial data input for 8-bit display and control data words
- 64 × 16-bit PLA provides data decoding driving
  - — Any 1 of 16 bargraph segments
  - — 1 to 16 bargraph segments
  - — Ten seven-segment numeric characters (0–9)
  - — Comma and decimal
  - — Eight upper and lower case seven-segment characters
- Command functions
  - — On/off duty cycle
  - — Character position
  - — Number of characters
- 40-Pin DIP package

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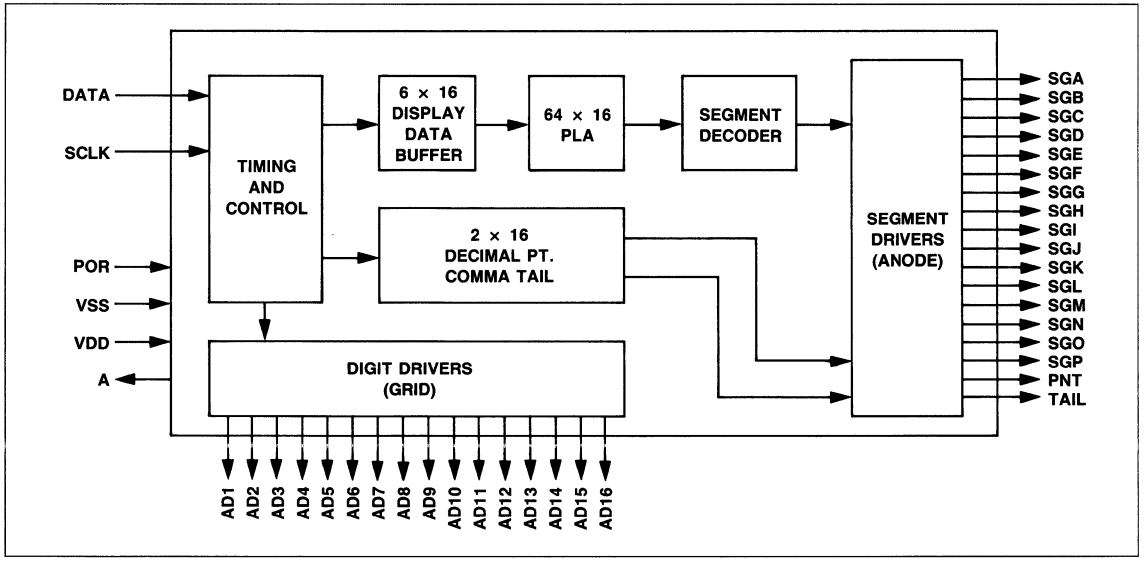
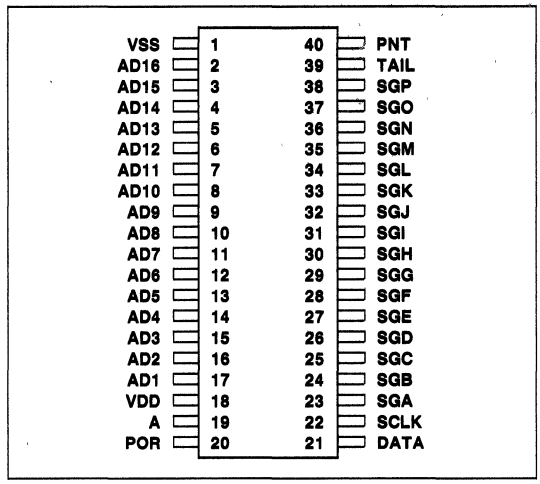


10951 Block Diagram

INTERFACE DESCRIPTION

10951 Pin Functions

Signal Name	Pin No.	Function
V_{SS}	1	Power and signal reference
AD16–AD1	2–17	Digits 16 through 1 driver outputs
V_{DD}	18	DC power connection
A	19	A clock output used for testing
POR	20	Power-on reset input
DATA	21	Serial data input
SCLK	22	Serial data clock input
SGA–SGP	23–38	Segments A through P driver outputs
TAIL	39	Comma tail driver output
PNT	40	Decimal point driver output



10951 Pin Configuration

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS*

All voltages are specified relative to V_{SS}.

Parameter	Symbol	Value	Unit
Supply Voltage	V_{DD}	+0.3 to −20	V
Operating Current	I_{DD}	7	mA
Input Voltage	V_{IN}	+0.3 to −20	V
Output Voltage	V_{OUT}	+0.3 to −50	V
Operating Temperature			
Commercial	T_C	0 to +70	°C
Industrial	T_I	−40 to +85	°C
Storage Temperature	T_{STG}	−55 to +125	°C
Input Capacitance	C_{IN}	5	pF
Output Capacitance	C_{OUT}	10	pF

***NOTE:** Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the other sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

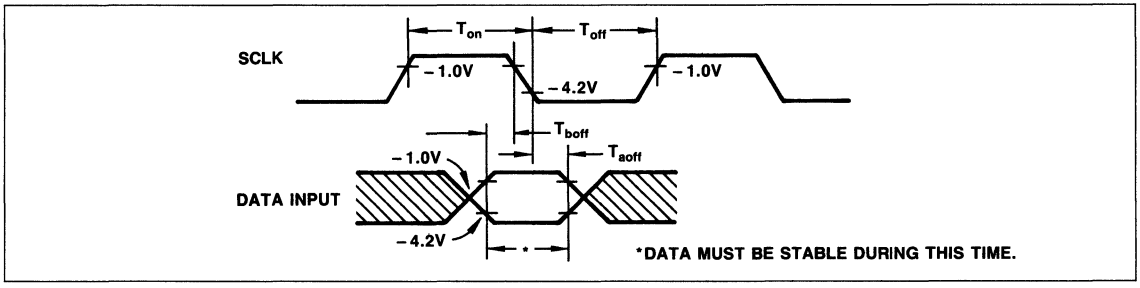
DC CHARACTERISTICS

Parameter	Limits (V_{SS} = 0)			Limits (V_{SS} = +5V)			Conditions	Unit
	Min	Typ	Max	Min	Typ	Max		
Supply Voltage (V_{DD})	−16.5	−15.0	−13.5	−11.5	−10.0	−8.5		V
Input DATA,SCLK,								
Logic "1"	−1.0		+0.3	+4.0		+5.3		V
Logic "0"	V_{DD}		−4.2	V_{DD}		+0.8		
Input POR								
Logic "1"	−3.0		+0.3	+2.0		+5.3		
Logic "0"	V_{DD}		−10.0	V_{DD}		−5.0		
Output Digit and Segment Strobes Driver On								
Commercial			−1.5			+3.5	At 10 mA	V
Industrial			−1.7			+3.3		V
Driver Off 10951-40	−40		−35	−35		−30	Actual value determined by external circuit	V
Driver Off 10951-50	−50		−45	−45		−40		V
Output Leakage			10			10	Per driver at driver off	μA
Input Leakage			10			10		μA

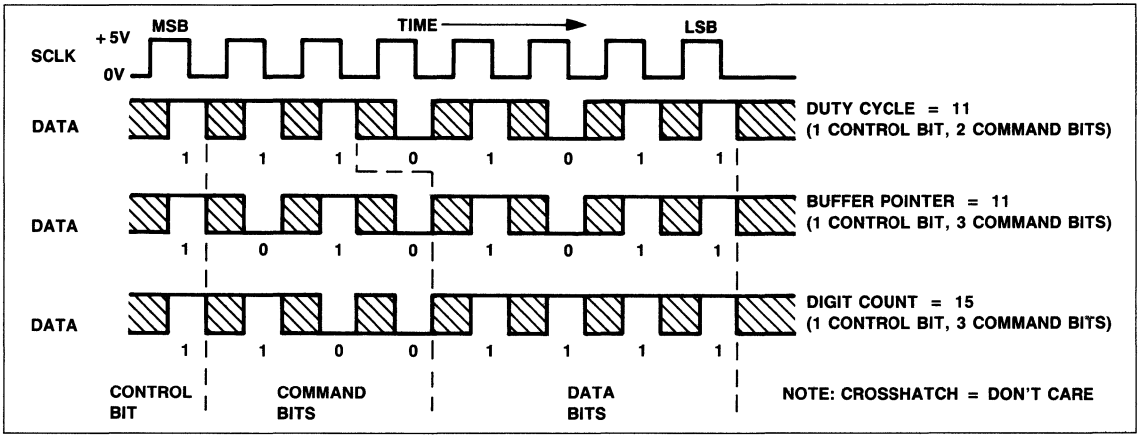
Note: All outputs require Pulldown Resistors.

AC CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Unit
SCLK Clock					
On Time	T_{on}	1.0		20.0	μs
On Time	T_{off}	1.0			μs
Data Input Sample Time					
Before SCLK Clock Off	T_{boff}	200			ns
After SCLK Clock Off	T_{aoff}	100			ns



SCLK and Serial Data Timing



SCLK and Serial Data (Control Word) Examples

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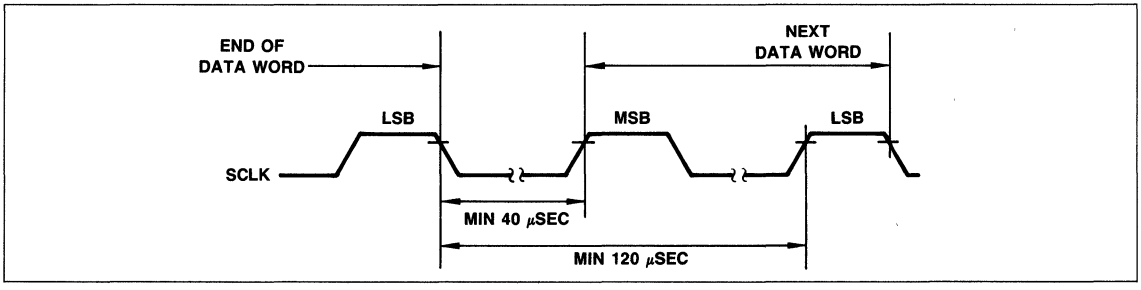
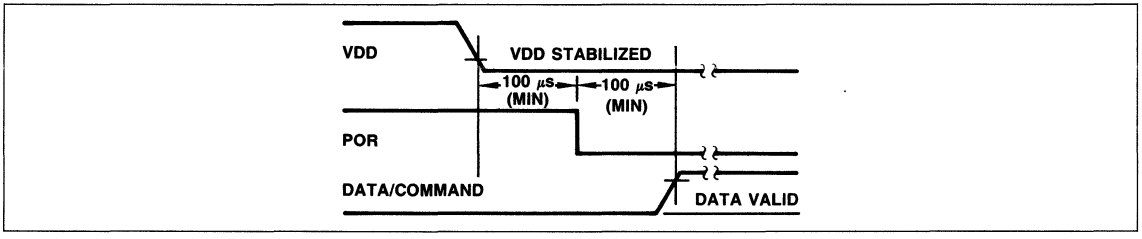


Data Word LSB/MSB Timing



Power-On Reset

FUNCTIONAL DESCRIPTION

The 10951 receives commands and data on a serial input line clocked externally by a separate clock input line. The controller decodes the commands from control data words, decodes the data words in accordance with an internal 64 x 16-bit programmable logic array (PLA) and turns on and off segment and digit output drivers. The segment output patterns are controlled by the decoded data words while the digit output and segment output timing are controlled by the decoded control words. All timing signals required to control the display are generated in the 10951 device without any refresh input from the host processor.

Input data is loaded into the Display Data Buffer via the Serial Data Input (Data) channel. Internal timing and control blocks synchronize the segment and digit output signals to provide the proper timing for the multiplexing operation. The 16 x 64 PLA decodes 8-bit data words to drive the 16 segment, comma and decimal point drivers. The decoded data words will drive 16 segments to display bargaph patterns (single segment and multiple segment for increasing length displays) or seven-segment patterns to display numbers, selected upper and lower case letters, comma and decimal point.

Input data is loaded into the 10951 as a series of 8-bit words with the most significant bit (MSB), bit 7 first. If the MSB is a logic 1 (this bit is referred to as the control bit C), the loaded word is a control data word. If the C bit of any word is a logic 0, the loaded word is a display data word. The following paragraphs describe the format and functions of these control and display data words.

INPUT CONTROL DATA WORDS

When the C-Bit (bit 7) of the 8-bit input word is a logic 1, bits 5 and 6 are decoded into one of four control commands while data associated with the command are extracted from bits 0–4. There are four control codes which perform the following display functions:

- Load the Display Data Buffer pointer,
- Load the Digit Counter,
- Load the Duty Cycle register,
- Enter Test Mode.

Table 1 lists the control codes and their functions.

Buffer Pointer Control

The Buffer Pointer Control code allows the Display Data Buffer pointer to be set to any digit position so that individual characters may be modified. The Buffer Pointer is loaded with a decimal equivalent value 2 less than the desired value (i.e., to point to the digit controlled by AD6 of the display, a value of 4 is entered). See Table 2 for a complete list of the Buffer Pointer values.

Digit Counter Control

The Digit Counter Control code is normally used only during initialization routines to define the number of character positions to be controlled. This code maximizes the duty cycle for any display. If 16 characters are to be controlled, enter a value of 0 (zero). Otherwise, enter the value desired.

Duty Cycle

The Duty Cycle Control code is used to turn the display on and off, and to adjust display brightness. As shown in the block diagram, the time slot for each character is 32 clock cycles. The Segment and digit drivers for each character are on for a maximum of 31 cycles with a 1 cycle inter-digit off-time. The Duty Cycle Control code contains a 5-bit numeric field which modifies the on-time for the driver outputs from 0 to 31 cycles. A duty cycle of 0 puts both the segment and digit drivers into the off state. Figure 1 shows the timing characteristics for the segment outputs.

Test Mode Enable

The Test Mode Enable code is a device test function only. If executed, it will lock the device in the Test Mode. This mode can be disabled only by performing a power-on reset.

If this mode is activated, the digit time is reduced from 32 to 4 clock cycles to speed up the output driver sequencing time for ease in testing.

Table 1. Control Data Words

8-Bit Control Word		Function
C-Bit	7-Bit Code	
1	010NNNN[1]	Load Buffer Pointer (Position of character to be changed)
1	100NNNN[1]	Load Digit Counter (Number of characters to be output)
1	11NNNNN[2]	Load Duty Cycle (On/off and brightness control)
1	00NNNNN[3]	Enter Test Mode (Not a user function)

Note:
1. NNNN is a 4-bit binary value representing the digit number to be loaded.
2. NNNNN is a 5-bit binary value representing the number of clock cycles each digit is on.
3. This code is a device test function only. If executed it will lock the device in the Test Mode. Test Mode can be disabled only by performing a power-on reset.

Table 2. Buffer Pointer Control Codes

Hex Code	Pointer Value	Character Controlled By
A0	16	AD2
A1	1	AD3
A2	2	AD4
A3	3	AD5
A4	4	AD6
A5	5	AD7
A6	6	AD8
A7	7	AD9
A8	8	AD10
A9	9	AD11
AA	10	AD12
AB	11	AD13
AC	12	AD14
AD	13	AD15
AE	14	AD16
AF	15	AD1

INPUT DISPLAY DATA WORDS

Display data words are loaded as 8-bit format codes. There are 64 codes available (with the C-bit set to 0 to indicate a display data word).

Sixteen display data words must be entered to completely load the Display Data Buffer. The Buffer Pointer is automatically incremented before each data word is stored in the Display Buffer except for decimal point and comma words. The decimal point and comma words do not cause the Buffer Pointer to increment and thus are always associated with the previous character entered. To enter a character position out of the normal sequence, use the Buffer Pointer control command before entering the display data word. It is not necessary to use the Buffer Pointer control command to cycle back to position 1 when less than 16 character positions are being used (Digit Counter ≠ 0).

DIGIT DRIVERS (AD1–AD16)

The sixteen Digit Drivers (AD1 – AD16) are used to select each of the display digits sequentially during a refresh scan. Display segments will be illuminated when both the Digit Drivers and Segment Drivers for a particular character are energized simultaneously. The timing characteristics of both the digits and segments are shown in Figure 1. See POR for the Power-On Reset state of these drivers.

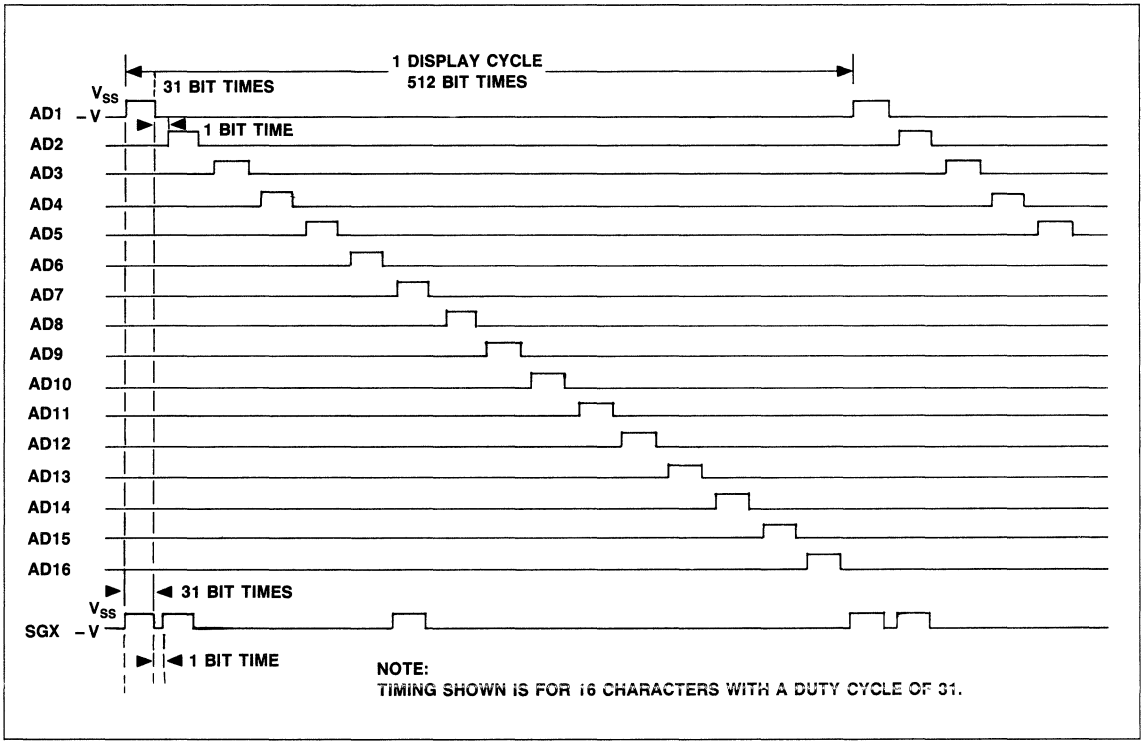


Figure 1. Display Scan Timing Diagram (Duty Cycle)

POWER-ON RESET (POR)

The Power-On Reset (POR) initializes the internal circuits of the 10951 when power (V_{DD}) is applied. The following conditions are established after a Power-On Reset:

a. The Digit Drivers (AD1-AD16) are in the off state (floating).
b. The Segment Drivers (SGA-SGP) are in the off state (floating). This includes PNT and TAIL.
c. The Duty Cycle is set to 0.
d. The Digit Counter is set to 16 (a bit code value of 0).
e. The Buffer Pointer points to the character controlled by AD1.

SEGMENT DRIVERS (SGA–SGP)

Sixteen (16) Segment Drivers are provided (SGA-SGP), plus the decimal point (PNT) and comma tail (TAIL). The segment, PNT and TAIL outputs are internally decoded from the 8-bit characters in the Display Data Buffer by means of a 64 × 16-bit PLA. The driver allocations for the 16-segment bargraph display and the seven-segment alphanumeric character plus comma and decimal point are shown in Figure 2. The input codes associated with seven-segment alphanumeric, comma and decimal point display are also shown in Figure 2. The complete set of 8-bit codes for the bargraph and alphanumeric display is shown in Table 3. Note that only segment drivers SGA-SGG are used to drive the seven-segment characters. Segment drivers SGH-SGP may be used for other purposes as decoded in accordance with Table 3. Figure 3 shows the total allocation of the 16-segment drivers as they would appear on a 7-segment display or a 16-segment bargraph display. Timing characteristics for the segment outputs are shown in Figure 1. See POR for the Power-On Reset state of these drivers.

TYPICAL SYSTEM HOOK-UP

Figure 4 shows the 10951 as it would be connected to a V-F display when driven by a host system. E_K is determined by the V-F display specifications and R_C is selected to provide proper biasing current for zeners. Pull down resistors R_A and R_G are determined by the interconnection capacitance between the 10951 and the display.

Table 3. 10951 Data Codes

Input Code								Function	Segment Driver Output Patterns (1 = On)																
7	6	5	4	3	2	1	0		SGA	SGB	SGC	SGD	SGE	SGF	SGG	SGH	SGI	SGJ	SGK	SGL	SGM	SGN	SGO	SGP	PNT	TAIL
0	X	0	0	0	0	0	0	Segment A On	1																	
0	X	0	0	0	0	0	1	Segment B On		1																
0	X	0	0	0	0	1	0	Segment C On			1															
0	X	0	0	0	0	1	1	Segment D On				1														
0	X	0	0	0	1	0	0	Segment E On					1													
0	X	0	0	0	1	0	1	Segment F On						1												
0	X	0	0	0	1	1	0	Segment G On							1											
0	X	0	0	0	1	1	1	Segment H On								1										
0	X	0	0	1	0	0	0	Segment I On									1									
0	X	0	0	1	0	0	1	Segment J On										1								
0	X	0	0	1	0	1	0	Segment K On											1							
0	X	0	0	1	0	1	1	Segment L On												1						
0	X	0	0	1	1	0	0	Segment M On													1					
0	X	0	0	1	1	0	1	Segment N On														1				
0	X	0	0	1	1	1	0	Segment O On															1			
0	X	0	0	1	1	1	1	Segment P On																1		
0	X	0	1	0	0	0	0	Segment A On	1																	
0	X	0	1	0	0	0	1	Segments A&B On	1	1																
0	X	0	1	0	0	1	0	Segment A-C On	1	1	1															
0	X	0	1	0	0	1	1	Segment A-D On	1	1	1	1														
0	X	0	1	0	1	0	0	Segment A-E On	1	1	1	1	1													
0	X	0	1	0	1	0	1	Segment A-F On	1	1	1	1	1	1												
0	X	0	1	0	1	1	0	Segment A-G On	1	1	1	1	1	1	1											
0	X	0	1	0	1	1	1	Segment A-H On	1	1	1	1	1	1	1	1										
0	X	0	1	1	0	0	0	Segment A-I On	1	1	1	1	1	1	1	1	1									
0	X	0	1	1	0	0	1	Segment A-J On	1	1	1	1	1	1	1	1	1	1								
0	X	0	1	1	0	1	0	Segment A-K On	1	1	1	1	1	1	1	1	1	1	1							
0	X	0	1	1	0	1	1	Segment A-L On	1	1	1	1	1	1	1	1	1	1	1	1						
0	X	0	1	1	1	0	0	Segment A-M On	1	1	1	1	1	1	1	1	1	1	1	1	1					
0	X	0	1	1	1	0	1	Segment A-N On	1	1	1	1	1	1	1	1	1	1	1	1	1	1				
0	X	0	1	1	1	1	0	Segment A-O On	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1			
0	X	0	1	1	1	1	1	Segment A-P On	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1		
0	X	1	0	0	0	0	0	Number 0	1	1	1	1	1	1		1	1	1	1	1						
0	X	1	0	0	0	0	1	Number 1		1	1					1	1	1	1	1						
0	X	1	0	0	0	1	0	Number 2	1	1		1	1		1	1	1	1	1	1						
0	X	1	0	0	0	1	1	Number 3	1	1	1	1			1	1	1	1	1	1						
0	X	1	0	0	1	0	0	Number 4		1	1			1	1	1	1	1	1	1						
0	X	1	0	0	1	0	1	Number 5	1		1	1		1	1	1	1	1	1	1						
0	X	1	0	0	1	1	0	Number 6	1		1	1	1	1	1	1	1	1	1	1						
0	X	1	0	0	1	1	1	Number 7	1	1	1					1	1	1	1	1						
0	X	1	0	1	0	0	0	Number 8	1	1	1	1	1	1	1	1	1	1	1	1						
0	X	1	0	1	0	0	1	Number 9	1	1	1	1		1	1	1	1	1	1	1						
0	X	1	0	1	0	1	0	Letter P	1	1			1	1	1						1	1	1	1		
0	X	1	0	1	0	1	1	Letter L				1	1	1							1	1	1	1		
0	X	1	0	1	1	0	0	Comma								1	1	1	1	1					1*	1*
0	X	1	0	1	1	0	1	Blank								1	1	1	1	1						
0	X	1	0	1	1	1	0	Decimal													1	1	1	1	1**	
0	X	1	0	1	1	1	1	Blank													1	1	1	1		
0	X	1	1	0	0	0	0	Number 0	1	1	1	1	1	1							1	1	1	1		
0	X	1	1	0	0	0	1	Number 1		1	1										1	1	1	1		
0	X	1	1	0	0	1	0	Number 2	1	1		1	1		1						1	1	1	1		
0	X	1	1	0	0	1	1	Number 3	1	1	1	1			1						1	1	1	1		
0	X	1	1	0	1	0	0	Number 4		1	1			1	1						1	1	1	1		
0	X	1	1	0	1	0	1	Number 5	1		1	1		1	1						1	1	1	1		
0	X	1	1	0	1	1	0	Number 6	1		1	1	1	1	1						1	1	1	1		
0	X	1	1	0	1	1	1	Number 7	1	1	1										1	1	1	1		
0	X	1	1	1	0	0	0	Number 8	1	1	1	1	1	1	1						1	1	1	1		
0	X	1	1	1	0	0	1	Number 9	1	1	1	1		1	1						1	1	1	1		
0	X	1	1	1	0	1	0	Letter A	1	1	1		1	1	1						1	1	1	1		
0	X	1	1	1	0	1	1	Letter b			1	1	1	1	1						1	1	1	1		
0	X	1	1	1	1	0	0	Letter C	1			1	1	1							1	1	1	1		
0	X	1	1	1	1	0	1	Letter d		1	1	1	1		1						1	1	1	1		
0	X	1	1	1	1	1	0	Letter E	1			1	1	1	1						1	1	1	1		
0	X	1	1	1	1	1	1	Letter F	1				1	1	1						1	1	1	1		

Notes:

* Sets comma and decimal outputs for last character entered.

** Sets decimal output for last character entered.

Any 1 of 16 Segments

Bargraph Codes

1 to 16 Segments

Alphanumeric and Special Codes

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00		08		10		18		20		28		30		38	
01		09		11		19		21		29		31		39	
02		0A		12		1A		22		2A		32		3A	
03		0B		13		1B		23		2B		33		3B	
04		0C		14		1C		24		2C	;	34		3C	
05		0D		15		1D		25		2D		35		3D	
06	—	0E		16		1E		26		2E	.	36		3E	
07		0F		17		1F		27		2F		37		3F	

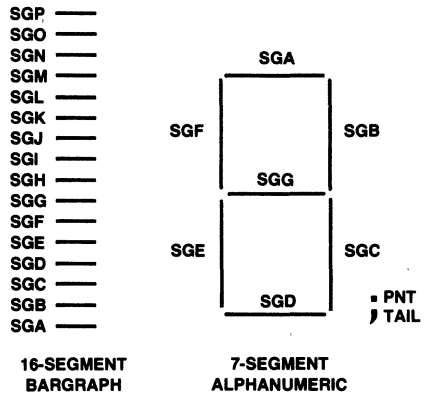


Figure 2. Segment Allocation and 7-Segment Alphanumeric Codes

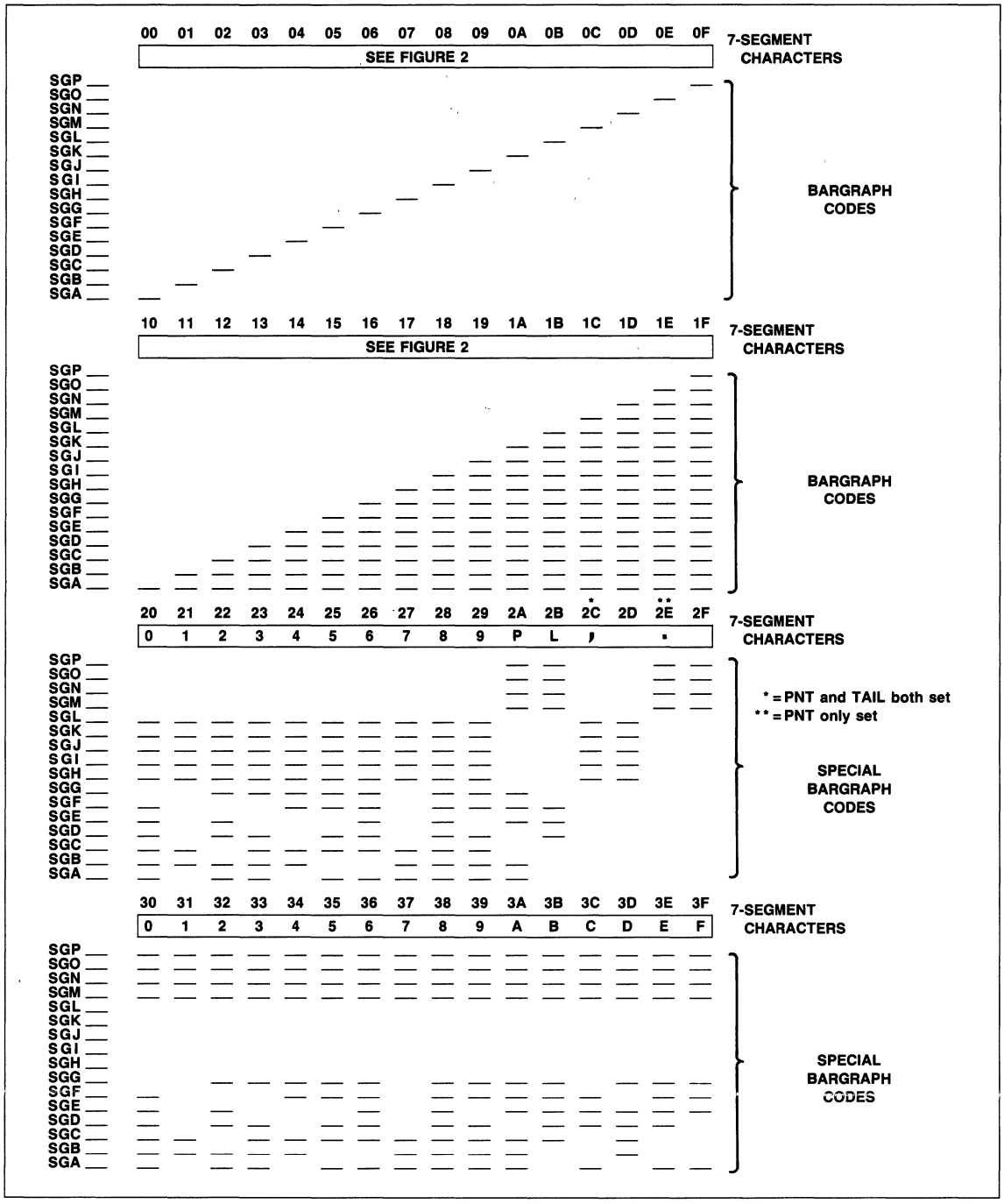


Figure 3. Total Character Allocation for Bargraph or 7-Segment Displays

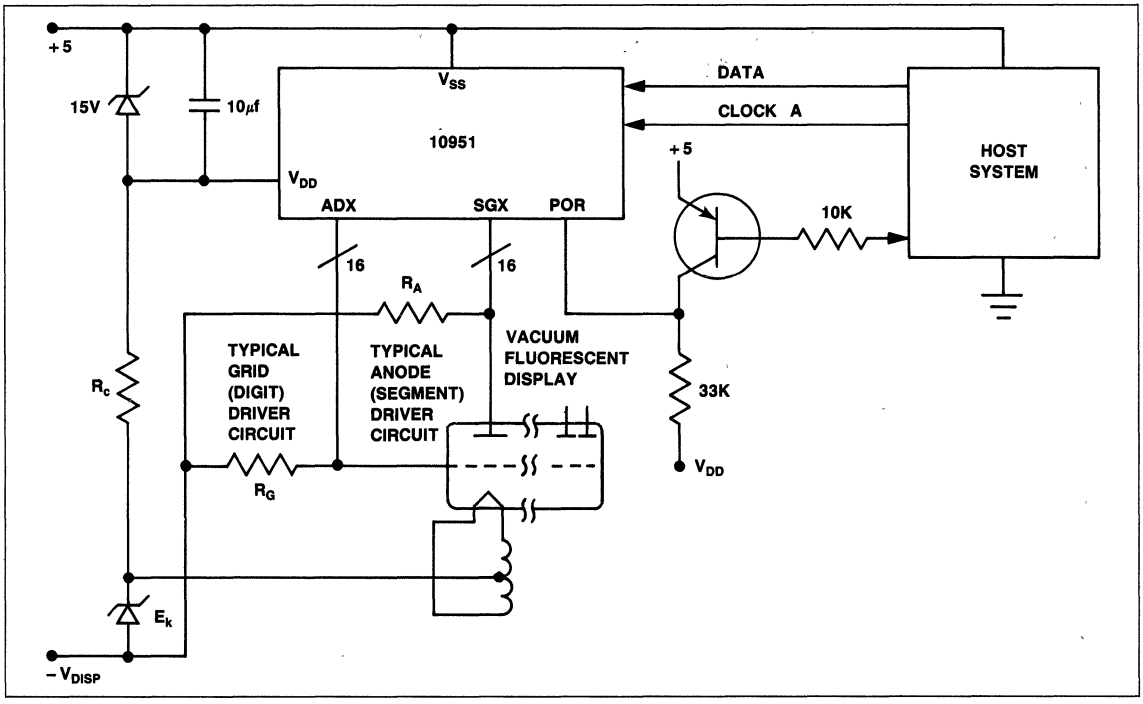


Figure 4. Partial System Schematic

Rockwell

10955
SEGMENTED DISPLAY CONTROLLER/DRIVER

PRELIMINARY

DESCRIPTION

The 10955 Segmented Display/Driver is a MOS/LSI device capable of directly driving both the grids and anodes of multiplexed vacuum-fluorescent segmented displays. All timing circuits (including a clock generator) required to control the display drivers are contained within the device. The 10955 can drive segmented displays with 8 or 16 grids (characters) and 8, 16, or 24 anodes (segments). A serial interface allows for a host microprocessor to transmit commands and display data to the 10955 directly.

A 128 x 16 bit PLA provides coding for both 16-segment and 14-segment alphanumeric ASCII code character sets (all caps only). The PLA is divided into lower 64 and upper 64 code sets. Only one set can be selected at a time. In lower set mode the 16-segment display characters are selected. In upper set mode the 14-segment display characters are selected. The PLA can also be bypassed so that data words from the host microprocessor are loaded directly into segment drivers without decoding by the PLA. This mode is especially useful for creating special display patterns such as bar graph displays. Bypass mode is limited to eight drivers per data word.

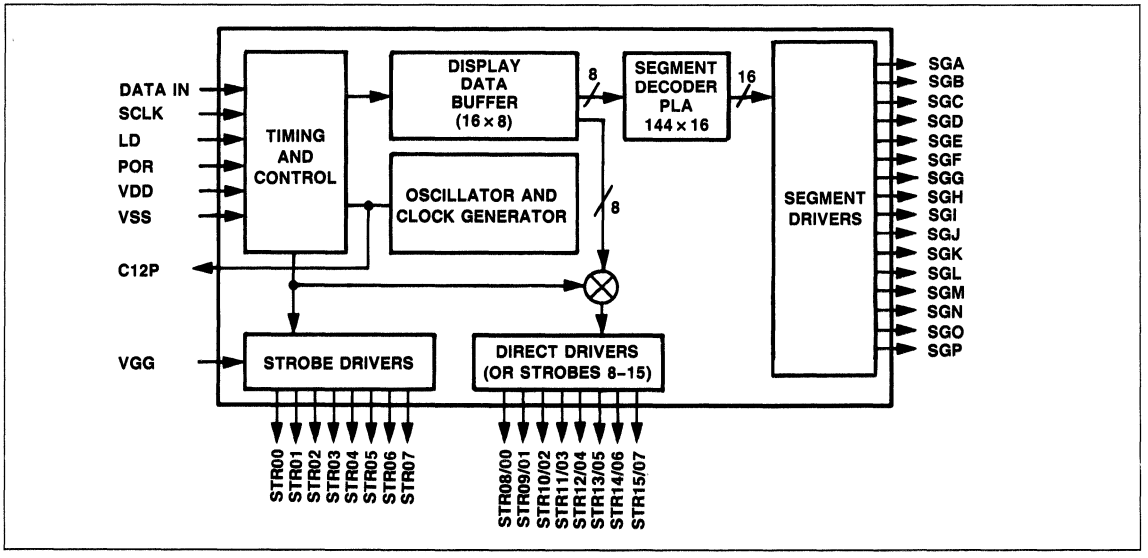
FEATURES

- 8- or 16-character display driver
- 8-, 16-, or 24-segment drivers
- Average data rate 66 kHz
- Single character burst rate 500 kHz
- Direct digit drive of 20 ma for up to 40 or 50 volt vacuum-fluorescent serial displays
- 128 x 16-bit PLA provides 16- or 14-segment alpha-numeric character set
- Internal clock generator circuit
- Serial host interface
- PLA bypass mode
- 40-pin DIP

ORDERING INFORMATION

Part Number	Package Type	Drive Voltage	Temperature Range (°C)
10955P-40	Plastic	40V	0 to +70
10955P-50	Plastic	50V	0 to +70
10955PE-40	Plastic	40V	−40 to +85
10955PE-50	Plastic	50V	−40 to +85

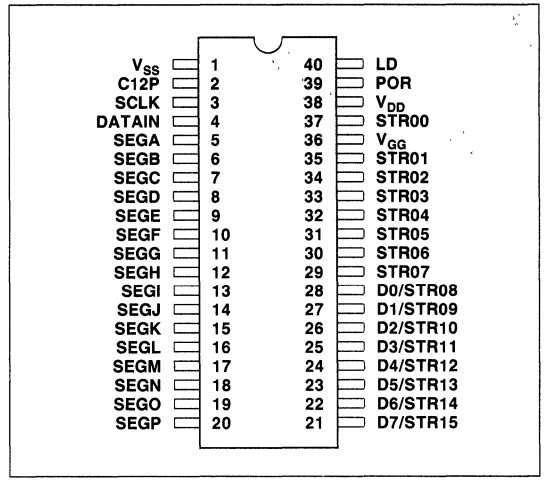
5



10955 Block Diagram

INTERFACE DESCRIPTION

Signal Name	Pin No.	Function
V_{SS}	1	Power and signal reference
C12P	2	Test clock—factory test
SCLK	3	Serial input data clock
DATAIN	4	Serial data input
SEGA-SEGP	5–20	Segments A through P driver outputs
D7/STR15–D0/STR08	21–28	Direct segment outputs or strobe outputs
STR07–STR00	29–35, 37	Strobe outputs
V_{GG}	36	Display voltage
V_{DD}	38	Logic supply voltage
POR	39	Power on reset
LD	40	Data Load Strobe



10955 Pin Configuration

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS*

All voltages are specified relative to V_{SS}.

Parameter	Symbol	Value	Unit
Supply Voltage	V_{DD}	+0 3 to -25	V
Operating Current	I_{DD}	8	mA
Input Voltage	V_{IN}	+0.3 to -25	V
Display Voltage	V_{GG}	+0.3 to -50	V
Operating Temperature			
Commercial	T_C	0 to +70	°C
Industrial	T_I	-40 to +85	°C
Storage Temperature	T_{STG}	-55 to +125	°C
Input Capacitance	C_{IN}	5	pF
Output Capacitance	C_{OUT}	10	pF

***Note:** Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the other sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

(V_{DD} = −18.0 to −22.0 Vdc, V_{SS} = 0 Vdc, TA = 0°C to +70°C (commercial) or −40°C to +85°C (industrial), unless otherwise noted. All voltages referenced to V_{SS}.)

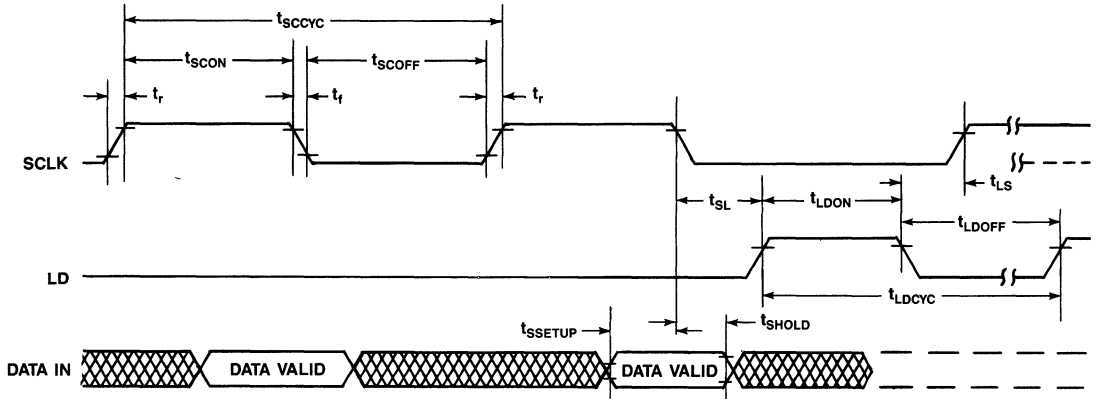
Parameter	Symbol	Min.	Typical 3	Max.	Unit
Operating Current, Logic	I_{DD}				mA
Commercial		—	3.2	6.4	
Industrial		—	4.0	8.0	
Operating Current Display	I_{GG}				
(1 strobe plus 24 segment)					
Commercial		—	—	6.5	mA
Industrial		—	—	8.0	mA
(1 strobe plus 16 segment)					
Commercial		—	—	4.3	mA
Industrial		—	—	5.3	mA
(All display drivers)					
V_{GG} and 85°C		—	—	320	μA
Display voltage	V_{GG}				V
10955-40		-40.0	—	—	
10955-50		-50.0	—	—	
Input Leakage (at −20V)	I_{IL}	—	—	10	uA
Input (DATAIN, LD, SCLK)					V
Logic "1"	V_{IH}	-1.2	-0 5	+0.3	
Logic "0"	V_{IL}	V_{DD}	-6.0	-4.2	
Input POR					V
Logic "1"	V_{IHPO}	-3.0	—	+0.3	
Logic "0"	V_{ILPO}	V_{DD}	-12.0	-10.0	
Output (C12P)					V
Logic "1"	V_{OHSY}	-0.7	—	+0.3	
Logic "0"[1]	V_{OLSY}	V_{DD}		—	
Output (Strobe STR00–07, D0–D7, SGA–SGP)					V
Logic "1" (I_{Load} = 10 mA)	V_{OH}	-1.5	-1.0	V_{SS}	
Logic "1" (I_{Load} = 20 mA)[2]	V_{OH}	—	-2.0	V_{SS}	
Logic "0" (I_{Load} = 0 mA)	V_{OL}	V_{GG}	0.5 + V_{GG}	0.95 × V_{GG}	

Notes:
1. Open drain driver. Requires external pull-down resistor for testing only.
2. STR00–STR07 only (also for D0–D7 when used as character drivers)
3. Typical measured at V_{DD} = 20.0V and Y_A = 25°C.

AC CHARACTERISTICS

Characteristic	Symbol	Min.	Typical	Max.	Unit
Clock Timing Cycle Time	t_{CYC}				
Commercial		6.66		20.0	usec
Industrial		5.88		22.2	usec
HOST INTERFACE TIMING					
Serial Clock (SCLK)					
On Time	t_{SCON}	1.0		40.0	usec
Off Time	t_{SCOFF}	1.0		—	usec
Cycle Time	t_{SCCYC}	2.0		—	usec
Serial Data (DATAIN)					
Set-up Time	t_{SSETUP}	400		—	nsec
Hold Time	t_{SHOLD}	400		—	nsec
Serial Clock to LD Time	t_{SL}	600		—	nsec
LD to Serial Clock	t_{LS}	400		—	nsec
Data Load (LD)					
On Time	t_{LDON}	1.0		—	usec
Off Time (Commercial	t_{LDOFF}	40.0		—	usec
Off Time (Industrial)	t_{LDOFF}	44.5		—	usec
Cycle Time (Commercial)	t_{LDCYC}	60.0		—	usec
Cycle Time (Industrial)	t_{LDCYC}	66.7		—	usec

Note:
t_r and t_f = rise and fall time of clocking signals which are 10 to 30 nsec.



Serial Interface Timing Waveforms

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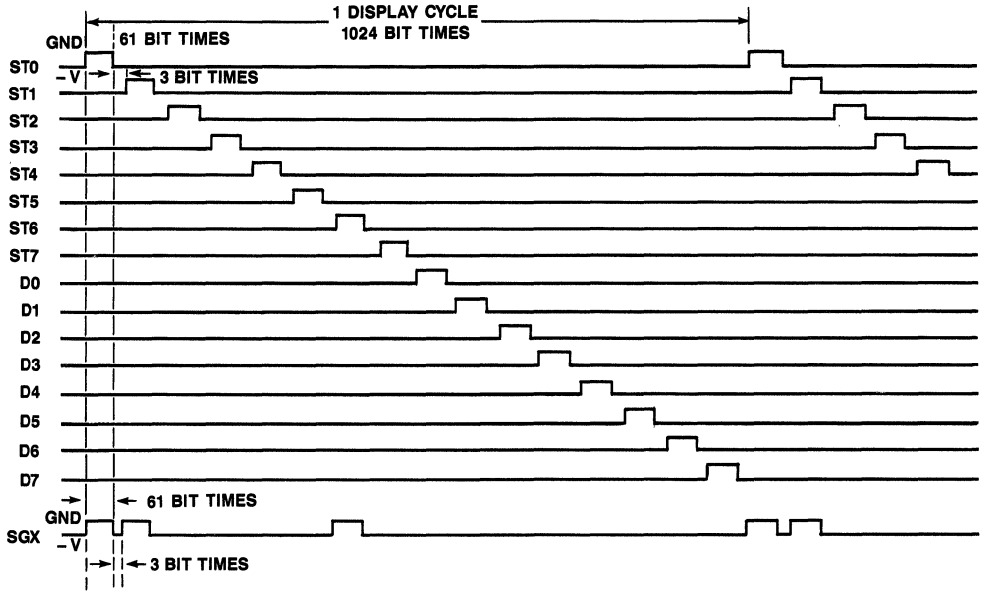


Notes:
1. t_{CYC} = 2 bit times.
2. Timing shown is for 16 characters with a duty cycle of 61.

Display Scan Timing Diagram

FUNCTIONAL DESCRIPTION

All timing signals required to control the display are generated by the 10955 device after the display buffer and control registers have been loaded from the host processor. In the following functional description, refer to the 10955 block diagram.

Input data is loaded into the Display Data Buffer via the serial data input channel. Internal timing and control logic synchronize the digit output signals with the segment output signals to provide the proper timing for the multiplexing operation. The segment decoding is performed in a 128 x 16 PLA character code set.

CHARACTER DRIVERS (STR00-STR07)

The eight character (grid) drivers are used to select the display character positions sequentially during a refresh scan. Display characters are illuminated when both the character driver for a particular character position and the segment (anode) drivers are energized simultaneously.

DISCRETE DRIVERS (D0-D7)

The function of these eight drivers depends on the display mode. In some modes these drivers act as segment (anode) drivers loaded directly from the Data Buffer (RAM). In other modes these drivers are used as extra character (grid) drivers (STR8-STR15). See Display Modes for further discussion of these driver functions.

SEGMENT DRIVERS (SGA-SGP)

Depending on the display mode, the sixteen segment drivers are loaded through an 8 x 16 PLA decoder or directly from the Data Buffer RAM.

SYSTEM CLOCK

Each 10955 device has its own on-board oscillator and clock generator.

POWER-ON RESET

The Power-On Reset (POR) input initializes the internal circuits of the 10955. This is normally performed when power (VDD) is applied. The following conditions are established by application of POR:

a. The grid and anode drivers (STR00-STR07, D0-D7, and SGA-SGP) are in the off state.

b. Duty Cycle register is set to zero.
c. The Digit Counter is set to 32 digits.
d. The Buffer Pointer is set to zero.
e. The Digit Time is set to 64.
f. The PLA Bypass/Sixteen Digit display mode is set.

At power on, the 10955 is held in an internal halt mode. This allows the host system to load the control registers and the data buffer without flashing invalid data on the display.

During the initial rise time of VDD at power turn-on, the magnitude of VGG should not exceed the magnitude of VDD.

HOST SYSTEM INTERFACE

Input data is loaded into the 10955 via a serial data input channel as a series of nine-bit words.

After nine bits of data (with the most significant bit first) have been shifted into the data buffer, a pulse on the LD signal loads the data into an internal buffer and informs the 10955 that a new data word is available. After the LD pulse, a new data word may be shifted in while the 10955 is processing the first word.

The following sections describe the format and functions of the input words which may contain either control data or display data.

Input Display Data Words

Display data words are loaded as nine bit codes. The lower eight bits (7-0) are data. The ninth bit (the most significant) is always a zero (0).

Sixteen display data words must be entered to completely load the Display Data Buffer. The Buffer Pointer is automatically incremented after each data word is stored in the buffer. To select the next character position to be loaded out of the normal sequence, use the Load Buffer Pointer command. The Buffer Pointer will automatically reset to character position 0 when its value is equal to the Digit Counter programmed value.

Control Data Words

Control data words are distinguished from display words by the fact that the most significant bit is always a one. Control words and their functions are defined below. The most significant bit is implied as always being a 1 for these functions.

8	7	6	5	4	3	2	1	0	BIT
			DATA						DUTY CYCLE, DIGIT COUNTER, BUFFER POINTER
1	LOAD		PLA MODE			CONFIG.	DIGIT TIME		← CONTROL REGISTER
	0	1	X	X	X	X	X	X	LOAD DUTY CYCLE REGISTER (with lower 6 bits)
	1	0	0	X	X	X	X	X	LOAD DIGIT COUNTER (with lower 5 bits)
	1	1	0	0	X	X	X	X	LOAD BUFFER POINTER (with lower 4 bits)
	0	0	0	X	X	X	X	X	LOAD CONTROL REGISTER (5 bits coded as shown below)
	0	0	0	X	X	X	0	0	64 cycles per grid
	0	0	0	X	X	X	0	1	16 cycles per grid
	0	0	0	X	X	X	1	0	32 cycles per grid
	0	0	0	X	X	X	1	1	8 cycles per grid
	0	0	0	X	X	0			16 digit configuration
	0	0	0	X	X	1			8 digit and two output
	0	0	0	0	0				PLA bypass
	0	0	0	0	1				Reserved for upgrade
	0	0	0	1	0				Lower 64 PLA (64U)
	0	0	0	1	1				Lower 64 PLA (64L)

5

Load Buffer Pointer

The Load Buffer Pointer code sets the Display Data Buffer Pointer. The three most significant bits of the loaded code value are dropped and the five least significant bits are loaded into the Control Data Word to provide the character position data shown in Table 1.

Table 1. Load Buffer Pointer Codes

Load Code Value	Pointer Value	Character Position Selected
C0	00	0
C1	01	1
C2	02	2
C3	03	3
C4	04	4
C5	05	5
C6	06	6
C7	07	7
C8	08	8
C9	09	9
CA	0A	10
CB	0B	11
CC	0C	12
CD	0D	13
CE	0E	14
CF	0F	15

Note: D0–DF (Not Used)

Load Digit Counter

The Load Digit Counter command defines the number of character positions (grids) to be controlled. This code is normally used only during initialization routines, but it may also be used in conjunction with the Load Duty Cycle control code to extend the range of brightness control. The display should be set up with digit 0 on the left and digit 15 on the right. The number of positions to be controlled starts at position 0 and increases to position 15. If 17 through 32 grids are specified, extra time slots are generated for these phantom strobes. When the phantom strobes are active, strobes 0 through 15 are off so the displayed data is not affected although the duty cycle is decreased as each phantom strobe is added. The code, digit counter value, and number of grids controlled by the Digit Counter are shown in Table 2.

Table 2. Load Digit Counter Control Codes

Code	Digit Counter Value	No. of Grids Controlled
80	00	32
81	01	1
82	02	2
83	03	3
84	04	4
85	05	5
86	06	6
87	07	7
88	08	8
89	09	9
8A	0A	10
8B	0B	11
8C	0C	12
8D	0D	13
8E	0E	14
8F	0F	15
90	10	16
91	11	17
92	12	18
93	13	19
94	14	20
95	15	21
96	16	22
97	17	23
98	18	24
99	19	25
9A	1A	26
9B	1B	27
9C	1C	28
9D	1D	29
9E	1E	30
9F	1F	31

Load Duty Cycle

The Load Duty Cycle code is used to turn on and off the display, to adjust display brightness, or to modify display timing. The time slot for each character is 8, 16, 32, or 64 internal cycles (an internal cycle = 1/2 t_{CYC} as selected by the Set Digit Time codes. The segment and digit drivers for each character are on for a maximum of 13, 29, or 61 cycles with a 3 cycle inter-digit off time. The lower six bits of the Load Duty Cycle code are loaded into the Duty Cycle Register. Resultant duty cycles, on-times, and off-times are shown in Table 3.

Table 3. Load Duty Cycle Control Codes

	Digit Time = 8		Digit Time = 16		Digit Time = 32		Digit Time = 64	
Code	On	Off	On	Off	On	Off	On	Off
40	—	8	—	16	—	32	—	64
41	—	8	—	16	—	32	—	64
42	—	8	—	16	—	32	—	64
43	1	7	1	15	1	31	1	63
44	2	6	2	14	2	30	2	62
45	3	5	3	13	3	29	3	61
46	4	4	4	12	4	28	4	60
47	5	3	5	11	5	27	5	59
48	5	3	6	10	6	26	6	58
49	5	3	7	9	7	25	7	57
4A	5	3	8	8	8	24	8	56
4B	5	3	9	7	9	23	9	55
4C	5	3	10	6	10	22	10	54
4D	5	3	11	5	11	21	11	53
4E	5	3	12	4	12	20	12	52
4F	5	3	13	3	13	19	13	51
50	5	3	13	3	14	18	14	50
51	5	3	13	3	15	17	15	49
52	5	3	13	3	16	16	16	48
53	5	3	13	3	17	15	17	47
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
5B	5	3	13	3	25	7	25	39
5C	5	3	13	3	26	6	26	38
5D	5	3	13	3	27	5	27	37
5E	5	3	13	3	28	4	28	36
5F	5	3	13	3	29	3	29	35
60	5	3	13	3	29	3	30	34
61	5	3	13	3	29	3	31	33
62	5	3	13	3	29	3	32	32
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
7C	5	3	13	3	29	3	58	6
7D	5	3	13	3	29	3	59	5
7E	5	3	13	3	29	3	60	4
7F	5	3	13	3	29	3	61	3

Load Control Register

There is a 5-bit control register, which can be loaded by the control word, 000XXXXX. The lower 5 bits of the control word is loaded into the control register.

The least significant two bits of the control register set the total Digit Time for each character during the refresh cycle. Four values can be set using the codes, 8, 16, 32, or 64 cycles per grid. The default value set at power-on is 64 cycles per grid. Under conditions where the display can be subjected to quick movements during viewing (e.g. portable or vehicle mounted applications) it may be necessary to increase the refresh rate by selecting 8, 16 or 32 cycles per grid with the appropriate control codes.

The middle bit of the 5 bit determines the sixteen digit or eight digit configurations. The last 2 bits select one of the four PLA Modes.

ENABLE DISPLAY MODE

The 10955 can operate in one of eight display modes which control the maximum number of active strobes and segments and the manner in which the RAM Data Buffer is decoded onto the segment drivers.

16-Digit Configuration

If the third bit of the control register is zero or is reset by the POR signal, the 16-digit configuration is selected, in which case, a maximum of 16 segments and 16 strobes are provided. The 16 words in the RAM Data Buffer correspond to the 16 strobes. The 8 data bits of each word are sent to the PLA for decode.

8 Digit Configuration

If the third bit of the control register is set, the 10955 is configured into 8-digit mode, in which case, a maximum of 8 strobes and 24 segments are allowed. The 8-bit words in the RAM Data Buffer are grouped into 8 word pairs which correspond to strobes STR0–STR7: 0-1, 2-3, 4-5, 6-7, 8-9, 10-11, 12-13, and 14-15. The data in the even-numbered word of each pair is loaded into the direct-output segment drivers (D0–D7), but the data in the odd-numbered word of each pair is decoded in the segment PLA decoder before being loaded into the 16-segment output drivers (SGA–SGP).

PLA Bypass Mode

If both of the most significant bits of the control register are zero, the PLA Bypass Mode is selected. In this mode, the PLA is bypassed. Each data word is loaded directly into the segment drivers without being decoded by the PLA. Since there are only 8 data bits but 16 drivers, each data bit is loaded into two adjacent drivers which can be connected externally to provide twice the current drive of an individual driver. The data bits/segments selection allocation is as follows:

Data bit	7	6	5	4	3	2	1	0
Segments	O,P	M,N	K,L	I,J	G,H	E,F	C,D	A,B

Upper 64 PLA Mode (64U)

In this mode (bit 5 = 1, bit 4 = 0) the Upper 64 out of the 128 codes are used, (i.e., 64 to 127). Since 64 codes can be specified by a 6-bit word, the most significant two bits of the 8-bit word from the RAM are not used. Another feature of this 64U-PLA mode is that the most significant two bits of the data can be brought out directly to SEGO and SEGP outputs. Therefore, the 64 codes can be decoded to the 16-segment outputs, or only 14-segment outputs leaving two for direct output from the RAM.

Lower 64 PLA Mode (64L)

This mode (bit 5 = 1, bit 4 = 1) is similar to the Upper 64 PLA Mode, but only the lower 64 codes (0–63) out of the 128 codes are used. The 64L and 64U PLA modes allow two independent sets of 64 codes to be programmed into one chip. In running the display, only one set can be selected at a time.

Fourth PLA Mode

A fourth PLA mode is reserved for future expansion of the 10955. This code (bit 5 = 0, bit 4 = 1) should not be used. Selecting this PLA mode may result in non-defined characters appearing on the display.

PLA CHARACTER SET CODES

Figure 1 shows the 16-segment and 14-segment driver assignments for the corresponding segmented displays. Figure 2 shows the 16-segment and 14-segment PLA character set patterns coded into the 10955.

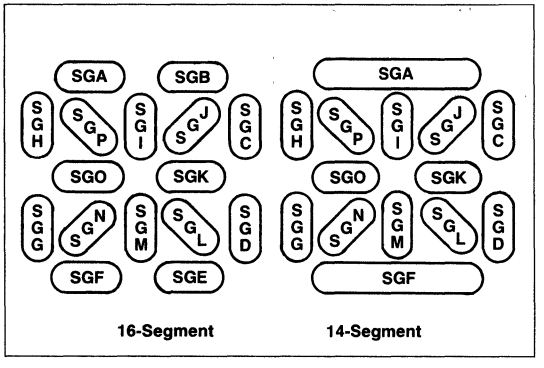
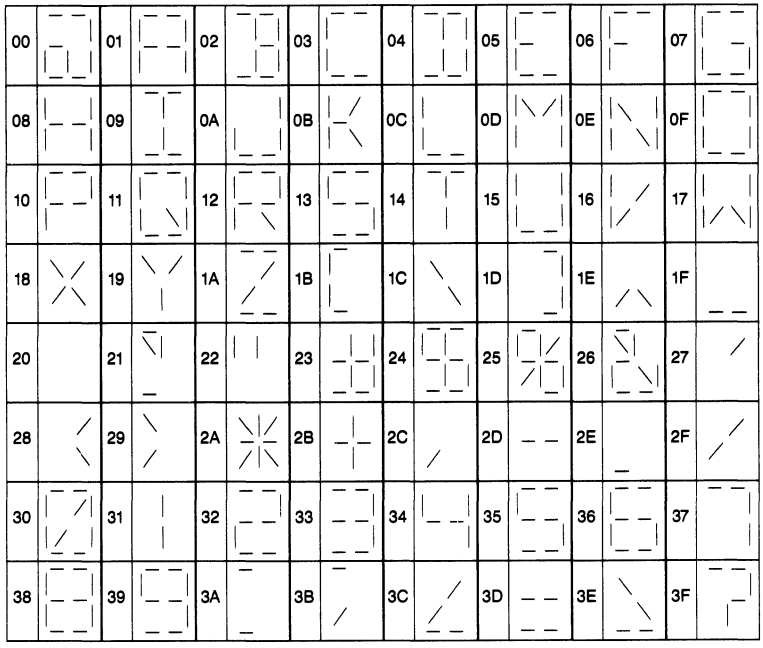
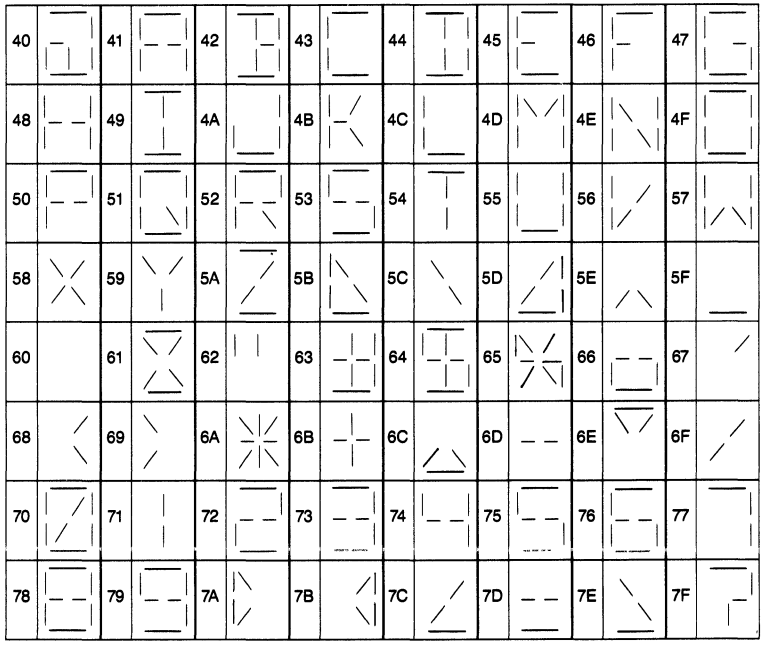


Figure 1. Segment Driver Assignments



16-Segment PLA Patterns

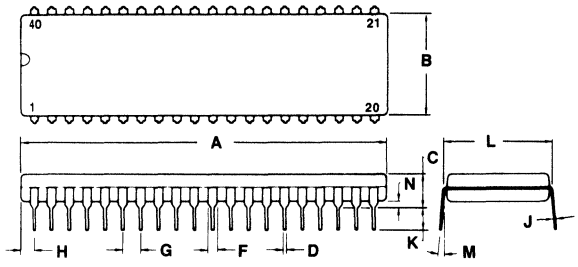


14-Segment PLA Patterns

Figure 2. 16- and 14-Segment PLA Character Sets

PACKAGE DIMENSIONS

40-PIN PLASTIC DIP



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	51 28	52 32	2 040	2 060
B	13 72	14 22	0 540	0 560
C	3 55	5 08	0 140	0 200
D	0 36	0 51	0 014	0 020
F	1 02	1 52	0 040	0 060
G	2 54 BSC		0 100 BSC	
H	1 65	2 16	0 065	0 085
J	0 20	0 30	0 008	0 012
K	3 05	3 56	0 120	0 140
L	15 24 BSC		0 600 BSC	
M	7°	10°	7°	10°
N	0 51	1 02	0 020	0 040

SECTION 6
MICROCOMPUTER DEVELOPMENT SYSTEMS

6

MICROCOMPUTER DEVELOPMENT SYSTEMS
Low Cost, Flexible Systems Work With Multiple μCs

To support product development, Rockwell offers a range of microcomputer development systems, each extremely economical when compared on a cost/performance basis with competitive development systems.

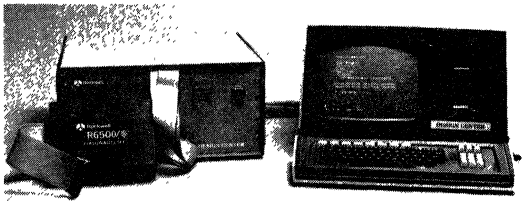
The new Low Cost Emulator (LCE) system links popular personal computers (PCs) to your application. Code is developed on the PC, downloaded to LCE, and it runs in-circuit emulation in your application. LCE also accepts downloads from other manufacturers development systems via cross assemblers.

The AIM 65 microcomputer functions as an extremely low cost, expandable, development system when used with the Rockwell Software Preparation System kit. The Rockwell Design Center (RDC) is an excellent, low cost, disk based development system, allowing concurrent development of up to four target R6500 and R6500/* systems.

The RDC is an easy to use, powerful development system for multi-chip and one-chip R6500 systems. A full line of support modules, macro assembler, link editor and high level PL/65 language are also available. R6500/* personality modules, additional RAM and a PROM programmer help add versatility.

The RDC supports the growing trend to using single-chip microcomputers as slaves with multi- or single-chip microprocessor systems. The advantages of slaves include both cost and technical savings, such as eliminating some complex timing relationships. With the RDC, up to four different microprocessor personality modules can be performing in-circuit-emulation under control of the system. The RDC mainframe is constructed modularly, using the proven RM Eurocard design, so it can be expanded readily, as needed. The terminal unit includes CRT, disk drives, and keyboard. Up to 1.28 Mbytes can be addressed on the two 96 TPI, double sided, double density, 5 ¼-inch disk drives.

The RDC allows designers to economically and efficiently develop multiple microcomputer systems, regardless of the microcomputer device involved. Personality sets and target RAM modules are available for all R6500 and R6500/* configurations.



Rockwell Design Center Development System

Low Cost Emulator System

Rockwell

RDC-1001/2 MULTIPLE TARGET DEVELOPMENT SYSTEM (MTDS)

INTRODUCTION

The Multiple Target Development System (MTDS) is a development system vertically integrated to support the entire R6500 family of microprocessors and microcomputers. The MTDS allows emulation, development, and software debugging of up to four separate microprocessors and microcomputers concurrently, even if the four devices are different members of the R6500 family. The MTDS is a disk-based system with two 96 TPI, doubled-sided, double-density 5¼-inch floppy disk drives that provide a storage capacity of up to 1.3M bytes of data (formatted).

A unique bus structure provides a separate system bus and four target busses which can operate at different speeds (up to 4 MHz) for the target bus which supports the emulator device. Construction of the MTDS is modular based on the proven RM 65 design using both single- and double-sized eurocards and highly reliable DIN 41612 pin and socket connectors. The double eurocards allow use of both the system bus and a target bus which can operate at different speeds.

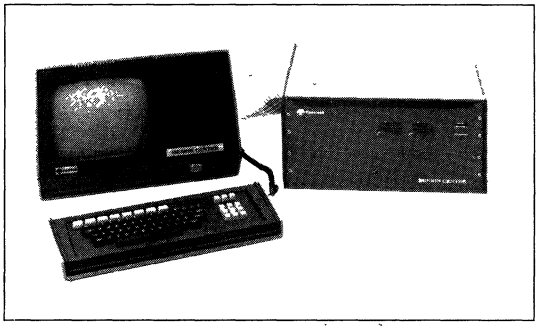
Featuring Softkey function keys, the MTDS eliminates the need for an operator to learn extra key strokes and command structures. A command line of operating modes is displayed across the bottom of the CRT screen so that the user need only push the corresponding function key to command the MTDS to enter the mode of operation desired.

SYSTEM FEATURES

- Modular construction based on proven RM 65 architecture
- Non-glare 12-inch CRT, green phosphor
- Detachable full ASCII intelligent keyboard
- Dual 96 TPI, double-sided, double-density 5¼-inch floppy disk drives
- Separate system bus and four independent target busses
- Separate system and target memory map
- Two serial ports—one for MTDS terminal interface—one for host system download
- Two parallel ports—one for MTDS terminal interface—one for external printer
- 64K byte RAM system memory
- Internal self-test panel for system troubleshooting
- Three separate CPUs for keyboard, CRT, and system control
- Designed for built-in PROM programmer option
- Requires only Personality Set for complete in-circuit debugging

For users who already have an Intel Development System (IDS) with mass storage program management, an R6500 cross-assembler is available. This allows the MTDS to function as a satellite, providing a powerful debug system. The MTDS is also capable of receiving files from the Rockwell System 65 Microcomputer.

When used with the R6500/* Microcomputer or R6502-R65C02 Microprocessor Personality Sets, the MTDS is a powerful emulation system for the complete family of Rockwell R6500/* one-chip microcomputers or NMOS R6502 and CMOS R65C02 families of microprocessors. The multiple target bus structure of the MTDS allows the user to emulate four devices concurrently, and at different speeds.



Multiple Target Development System (MTDS)

- Self-contained, disk-based operating system
- Softkey function access to menu-driven operational modes
- Disk based Text Editor
- Disk based R6500 Macro Assembler with all instruction subsets
- SYSGEN configurable to user environment
- Automatic power-up initialization of system and configurations
- Separate system and target memory map
- Allows Real-time in-circuit emulation, up to 4 MHz
- Five hardware breakpoints per target, 32-bits (16 addr, 8 data and 8 control) wide with "don't care" bits
- External trigger input allows TTL level to cause a user breakpoint
- Configurable as a satellite for an IDS host system or Rockwell System 65

6

PRODUCT OVERVIEW

The MTDS consists of three assemblies; the mainframe, a CRT terminal with floppy disk drives and a full ASCII keyboard. The mainframe contains the following components:

- The system bus and target/user busses
- Power supply and system cooling fans
- Two 32K Dynamic RAM modules for system memory
- Single Board Computer (SBC) module
- Floppy Disk Controller (FDC) module
- Asynchronous Communications Interface Adapter (ACIA) module with 2 channels for keyboard interface and user RS-232C
- Multi-function Peripheral Interface (MPI) module with two ports for interface to the CRT terminal and to a printer
- 24-pin and 28-pin PROM sockets for optional PROM Programmer module

The terminal assembly consists of a non-glare 12-inch, green phosphor CRT, a video display controller module, and two 5¼-inch floppy disk drives. The keyboard is intelligent for full ASCII operation.

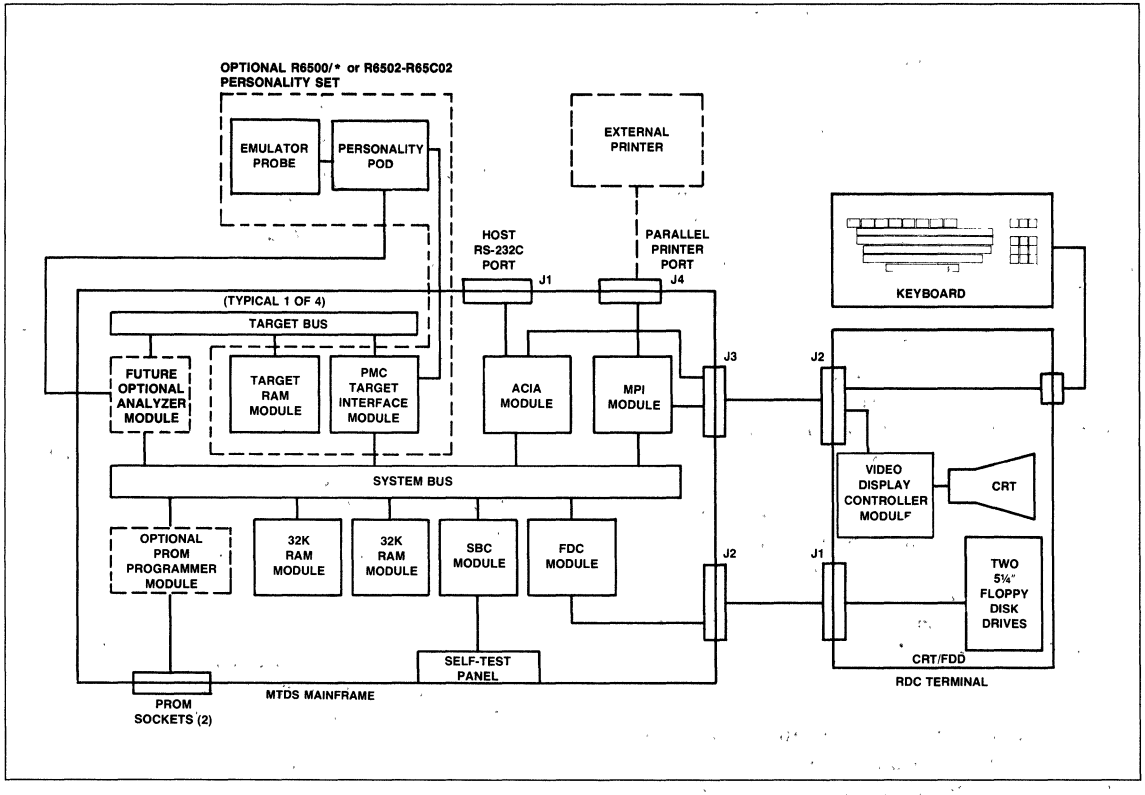
FUNCTION DESCRIPTION

Major Components and Interfaces

The block diagram shows the architecture of the MTDS system and identifies the relationship between the system bus and the target busses. Although the block diagram shows only one Target Interface, it represents the architecture of each of the four target busses. The terminal keyboard interfaces with the MTDS system through one of the RS-232C ports (J3 connected to the ACIA module). The CRT interfaces with the MTDS system through a parallel port (J3 connected to the MPI module). The disk drives interface to the MTDS system through a separate port (J2 connected to the FDC module). All other control functions of the MTDS system interface directly through the MTDS system bus. Note that the Personality Set PMC module interfaces the MTDS system bus to the target bus.

Bus Structure

The MTDS system operates through a multiple bus structure—a system bus and four target busses. The system bus contains 21 card slots to accommodate singe Eurocard modules or

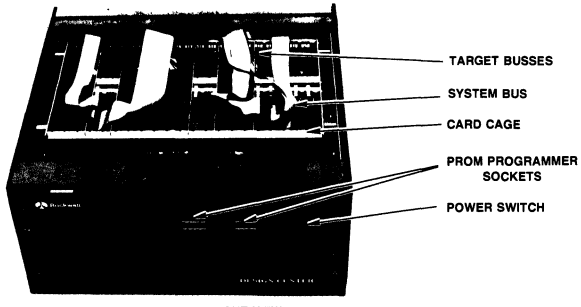


MTDS System Block Diagram

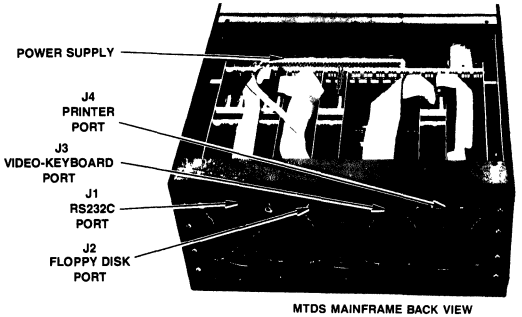
double Eurocard modules. Double Eurocard modules plugged into the system bus are common to the system bus and the target bus. Double Eurocard modules (such as the R6500/* Personality Set PMC module) are used for microcomputer emulation support. Single Eurocard module connectors on the system bus are used to interface with MTDS microcomputer system modules such as the 32K RAM(2), SBC, FDC, ACIA, and MPI.

The four target busses are segmented so that four separate emulations can be controlled by the system concurrently. Three of the target busses have four card slots each. Three of these slots will accept double Eurocard modules, and the fourth will accept a single Eurocard module. The double card slots are intended for a Personality Module Controller (PMC) module and future growth up to two Analyzer modules. The single card slot is intended for plugging in a target (emulation) RAM module (8K x 8, 32K x 8 or 64K x 8 depending upon the microcomputer to be emulated). These three target busses are color coded (blue, red, and yellow) on the MTDS card cage for easy identification of the division of the target bus segments. The fourth target bus consists of nine Euroconnectors, four of which will accept double Eurocard modules and five of which will accept single Eurocard modules.

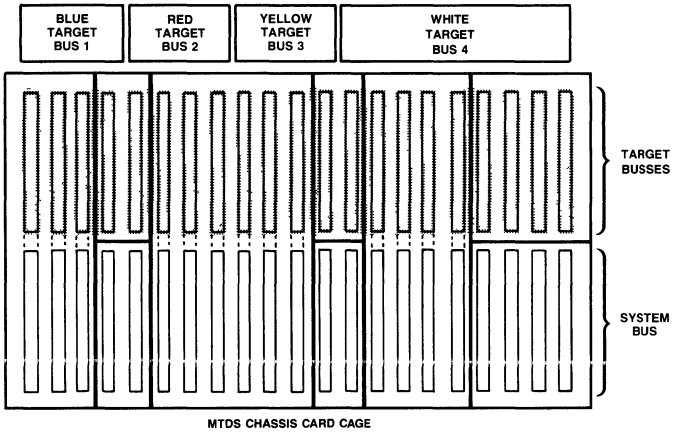
A typical single target emulation configuration will consist of an R6500/* or R6502-R65C02 Personality Set (comprising a PMC module, Personality Pod, and Emulator Interface) and a target RAM module, as a minimum. Since up to four fully configured emulation systems can be supported concurrently, the MTDS could be configured with any combination of four R6500/* or R6502-R65C02 Personality Sets, and four target RAM modules in addition to the RDC system control modules.



MTDS MAINFRAME FRONT VIEW



MTDS MAINFRAME BACK VIEW



MTDS CHASSIS CARD CAGE

MTDS Internal Layout and Card Cage Bus Structure

Operating Modes

The MTDS bootstrap ROM is initiated whenever the system is powered-up. The bootstrap program then loads the SYSGEN data and system program from the system disk drive. When the bootstrap is completed the CRT displays a Softkey menu for the function keys on the keyboard. It is this menu that prompts the user to select the mode of operation required. The Softkey prompts displayed at this time are:

SATELLITE LOCAL SYSGEN HELP

These Softkey prompts represent the primary modes of operation for the MTDS system. When the function key corresponding to the CRT prompt location is pressed, one of the following modes is selected:

SATELLITE—This mode provides the menus available for interfacing the MTDS as a satellite to the host system (Intel ISIS II)

LOCAL —This mode provides the menus available to the user from within the MTDS without requiring host resources.

SYSGEN —This mode allows the user to modify the diskette-stored system parameters on either a permanent (until another power-up condition) or a temporary basis.

HELP —This mode displays information which briefly describes the operational mode options available in SATELLITE, LOCAL and SYSGEN modes. All Softkey menus include a HELP which is always located on the CRT screen directly over the far right hand function key on the keyboard.

Each Softkey prompt, when selected by the function key, invokes a new set of Softkey prompts which further define the tasks to be performed by the mode. As an example, if the LOCAL prompt is selected, a new Softkey prompt menu displays:

UTILITY, DEBUG HELP

If UTILITY is selected from this prompt, a new menu displays:

DISK FILE EXEC HELP

Selecting DISK invokes a new menu which asks:

COPY BACKUP FORMAT DIR INIT HELP

This hierarchy continues until all parameters of the tasks of the mode selected have been established. At any time during the mode selection process the user has the option of calling back the previous set of Softkey menu prompts by simply pushing the – (minus) key.

The illustration shows the depth to which the command line prompts guide the user through selecting the desired mode of operation.

Software Command Overview

SYSGEN FUNCTIONS

BAUD	Select baud rate for host interface
WORD LEN	Select word length for host interface
PARITY	Select parity for host interface
STOP BITS	Select stop bits for host interface
TARGET	Select the processor type emulating for each of the targets
PROTOTYPE	Select areas to be mapped external for each target
PRINTER	Set up paging parameters for parallel printer
BEEPER	Turn on or off the BELL to indicate errors
DISPLAY	Show the current sysgen setup parameters
KEEP	Save the current sysgen parameters onto system disk

UTILITY FUNCTIONS

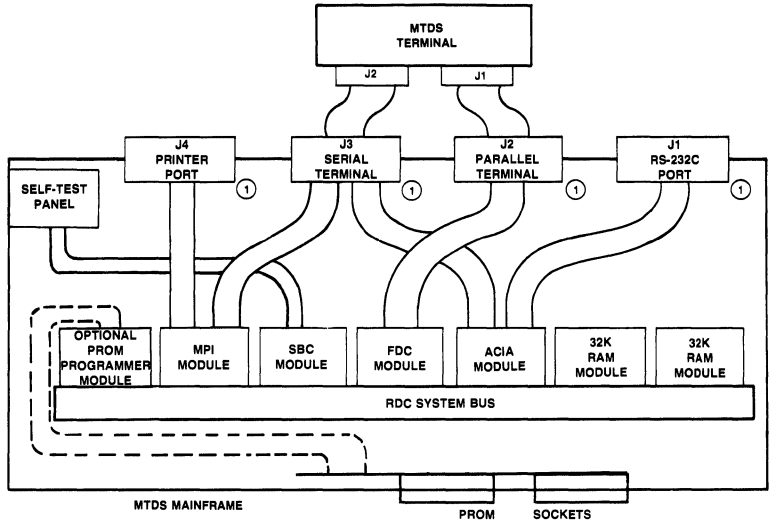
COPY	Copy diskettes
BACKUP	Copies disk files
FORMAT	Format new diskette
INITIALIZE	Initialize diskette directory
DIRECTORY	List or Print diskette directory
LIST	List fole to printer, screen or disk file
DELETE	Remove disk file
RECOVER	Recover deleted disk file
RENAME	Rename disk file
EXEC	Executive a disk-based utility (i.e. Text Editor, Macro Assembler, etc.)
DOWNLOAD	Transfer object file from host computer (System 65 or Intel ISIS)

DEBUG FUNCTIONS

DUMP	Show an image of user memory (Hex and ASCII)
MODIFY	Allow changes to user memory (Hex and ASCII)
DISASSM	Disassemble selected area of user memory
LOAD	Load selected area of user memory with object code file
SAVE	Save selected area of user memory to disk file
VERIFY	Verify contents of user memory with data in disk file
PROTECT	Set and clear areas to be write protected
RUN	Execute at normal speed until any breakpoint condition occurs
STEP	Execute user program displaying every instruction and register
RESET	Reset all debut parameters and hardware
REGISTER	Show and accept changes to, load or save emulator registers
BREAKPOINT	Show and accept changes to the breakpoint conditions

INTERFACE

Interface between the MTDS system control modules and the port connectors on the back panel are made through ribbon cables. The ribbon cables are permanently attached to the port connectors. The terminal interfaces to the MTDS system through two cables with mating connectors on each end that are keyed for proper installation. The MTDS Cable Interface figure shows how these cables are routed in the system. The Self-Test Panel interface ribbon cable is attached to the test panel and has a connector on the other end that mates to the SBC module I/O connector. The optional PROM programmer module connects to the two PROM sockets through a single ribbon cable.



NOTE: (1) RIBBON CABLES ARE PHYSICALLY ATTACHED TO MTDS MAINFRAME CONNECTORS J1 THROUGH J4 AND HAVE CONNECTORS ON THE OTHER END THAT MATE TO THE MODULES.

MTDS Mainframe Internal/External Ribbon Cable Connections

SPECIFICATIONS

Parameter	MTDS Mainframe	MTDS Terminal	
		CRT/FDD	Keyboard
Dimensions			
Height	11 in. (27 94 cm)	14 in. (35.56 cm)	3 in. (7.62 cm)
Width	20 in. (50.80 cm)	20 in. (50.80 cm)	20 in. (50.80 cm)
Depth	18 in. (45.72 cm)	16 in. (40.64 cm)	8 in. (20.32 cm)
Weight	40 lbs. (18 Kg)	42 lbs. (19 Kg)	6 lbs. (2.7 Kg)
Electrical			
AC Input Voltage	105 to 125 (RDC-1001) 210 to 250 (RDC-1002)	105 to 125 (RDC-1001) 210 to 250 (RDC-1002)	
AC Frequency	47 to 63 Hz	47 to 63 Hz	
Fuse Requirement	3 A slo-blo (RDC-1001) 1.5 A slo-blo (RDC-1002)	3 A slo-blo (RDC-1001) 1.5 A slo-blo (RDC-1002)	
Environmental			
Temperature	59°F to 104°F (15°C to 40°C) operating -4°F to 140°F (-20°C to 60°C) shipping -4°F to 122°F (-20°C to 50°C) storage		
With/Disk Media			
Humidity	20% to 80% non-condensing operating* 1% to 95% non-condensing shipping 1% to 95% non-condensing storage		

NOTE: *Disk media maximum wet bulb temperature 84.9°F (29.4°C)

ORDERING INFORMATION

Part Number	Description
RDC-1001	MTDS System (100 Vac)(1)
RDC-1002	MTDS System (220 Vac)(1)
RDC-1020	64K Target RAM Module
RDC-1022	32K Target RAM Module
RDC-1024	8K Target RAM Module
RDC-1030	PROM Programmer Module
RDC-2000	R6500 Cross Assembler for Intel IDS
Order Number(2)	**Document Title**
RDC06	RDC R6500/* Personality Set Data Sheet
RDC09	R6500 Cross Assembler for IDS Data Sheet
RDC11	RDC R6502-R65C02 Personality Set Data Sheet
RDC12	MTDS PROM Programmer Data Sheet

Notes:
(1) Both system configurations are shipped with the following components:
- MTDS Mainframe
- MTDS Terminal with 12″ CRT and Dual 5¼″ Floppy Disk Drives and detached Keyboard
- Six System Control modules—ACIA, FDC, SBC, MPI, and two 32K DRAM
- All Required Interface Cables
- Software Package (Utilities, Text Editor, Macro Assembler)
- Documentation Package

(2) Documents provide further information about the MTDS system.

PERSONALITY SETS

Personality Sets are available for the MTDS that allow emulation, development, and software debugging of the complete family of R6500/* Microcomputers and R6502-R65C02 Microprocessors. The microcomputers and microprocessors supported by these Personality Sets are:

- R6500/11P
- R6500/12P
- R6541Q
- R65C102
- R6504
- R6512
- R6500/13P
- R6500/41P
- R6501Q
- R65C112
- R6505
- R6513
- R6500/42P
- R6500/43P
- R6502
- R6506
- R6514
- R6500/1P
- R6511Q
- R65C02
- R6503
- R6507
- R6515
- R6500/15P
- R6500/16Q

For complete information on ordering any particular Personality Set or groups of Personality Sets, refer to the RDC R6500/* Personality Set Data Sheet, Order Number RDC06, or RDC R6502-R65C02 Personality Set Data Sheet, Order Number RDC11.

Rockwell

RDC-3101/2
LOW COST EMULATOR (LCE)

INTRODUCTION

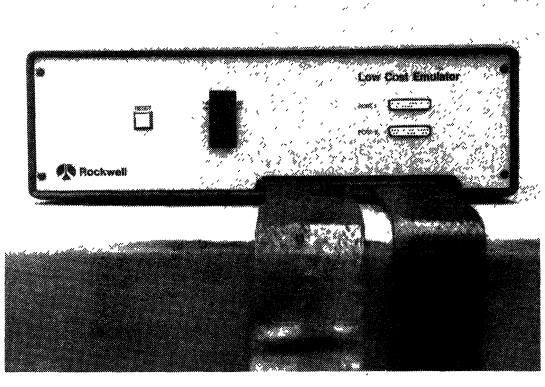
The Low Cost Emulator (LCE) is a development system vertically integrated to support the entire R6500 family of microprocessors and microcomputers. The LCE allows emulation, development, and software debugging of microprocessors and microcomputers of the R6500 family.

A unique bus structure provides a separate system bus and target bus which can operate at different speeds (up to 4 MHz) for the target bus which supports the emulator device. Construction of the LCE is modular based on the proven RM 65 design using both single- and double-sized Eurocards and highly reliable DIN 41612 pin and socket connectors. Additional slots allow expansion.

Featuring Softkey function keys, the LCE eliminates the need for an operator to learn extra key strokes and command structures. A command line of operating modes is displayed across the bottom of the CRT screen so that the user need only push the corresponding function key to command the LCE to enter the mode of operation desired.

For users who already have an Intel development system with mass storage program management, an R6500 cross-assembler is available. This allows the LCE to function as a satellite, providing a powerful debug system. The LCE is also capable of receiving files from the Rockwell System 65 Microcomputer.

When used with the R6500/* Microcomputer or R6502-R65C02 Microprocessor Personality Sets, the LCE is a powerful emulation system for the complete family of Rockwell R6500/* one-chip microcomputers or NMOS R6502 and CMOS R65C02 families of microprocessors.



Low Cost Emulator (LCE)

FEATURES

- Compact desktop modular design construction allows future options
- SYSGEN configurable to user environment
- Front panel reset switch with 'warm' option to maintain SYSGEN parameters
- Two serial ports—one for terminal interface—one for host system download or other peripheral devices
- Serial port options for eight baud rates 110 to 19.2K with choice of 7- or 8-bit word length
- Software allows choice of any baud rate, word length or parity options with full handshake signal support from the R6551 ACIA device
- Target emulation of any R6500 multichip or single-chip MPU device
- 24K-byte ROM includes system, debug and self-test firmware
- 10K-byte RAM with 8K bytes for symbol table generation
- Internal default switch/LED panel with software for system troubleshooting
- Self-contained, ROM-based operating system
- Softkey function access to menu-driven operational modes
- R6500 Assembler with all instruction subsets
- Separate system bus and target bus with independent processor
- Allows real-time in-circuit emulation, up to 4 MHz
- Five hardware breakpoints, 32-bits wide (16 address, 8 data 8 control) with "don't care" mask for each bit
- Two hardware matchpoints allow execution to continue with external TTL level trigger signals
- External trigger input allows TTL trigger to cause a user breakpoint
- Configurable as a satellite for any host system including the Rockwell System 65
- Designed for add-on PROM programmer option
- Requires only Personality Set and user supplied terminal for full operation

6

PRODUCT OVERVIEW

The LCE mainframe contains the following components:

- The card cage/backplane with system bus and target bus
- Power supply and system cooling fan
- Single Board Computer (SBC) module (2K RAM, 8K ROM)
- Universal memory module for system memory (8K RAM, 16K ROM)
- Asynchronous Communications Interface Adapter (ACIA) module with 2 channels preconfigured for terminal and host interfaces
- 28-pin PROM socket for optional PROM Programmer module
- Personality Set Module Controller (PMC) with cables to connect a R6500/* or R6502-R65C02 Personality Set

FUNCTIONAL DESCRIPTION

MAJOR COMPONENTS AND INTERFACES

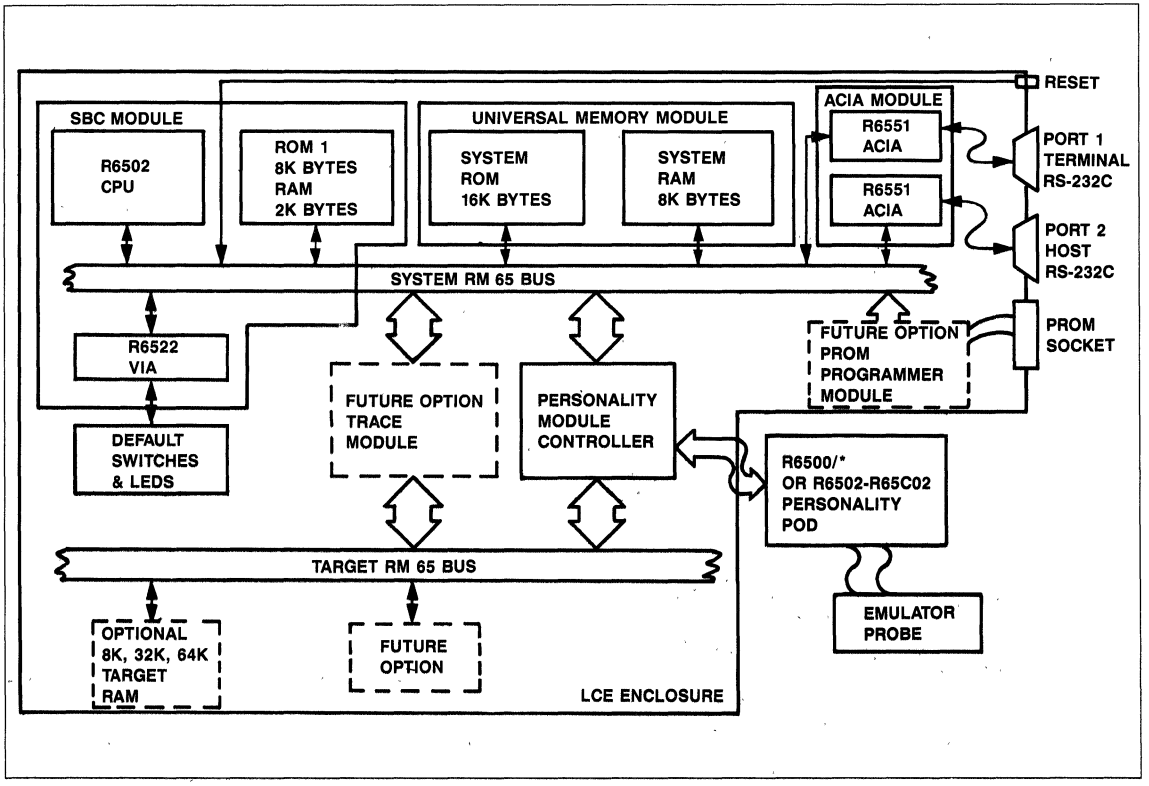
The block diagram shows the architecture of the LCE system and identifies the relationship between the system bus and the target busses.

Bus Structure

The LCE system operates through a multiple bus structure—a system bus and target bus. The system bus contains 4 card slots to accommodate single eurocard modules and 2 card slots for double eurocard modules. Double eurocard modules plugged into the system bus are common to the system bus and the target bus. Double eurocard modules (such as the R6500/* Personality Set PMC module) are used for microcomputer emulation support. Single eurocard module connectors on the system bus are used to interface with LCE microcomputer system modules such as the universal RAM, SBC, and ACIA.

The target bus contains two single card slots and two double slots shared with the system bus. The double card slots are intended for a Personality Module Controller (PMC) module and future growth up to an Analyzer module. The single card slot is intended for plugging in a target emulation RAM module (8K × 8, 32K × 8, or 64K × 8 depending upon the microcomputer to be emulated). The target bus is color coded red on the LCE card cage for easy identification of the division of the target bus segment.

A typical LCE configuration consists of an R6500/* or R6502-R65C02 Personality Set, Personality Pod, and Emulator Interface) and a target RAM module.



LCE System Block Diagram

Operating Modes

The LCE bootstrap ROM is initiated whenever the system is powered-up. The program then loads the SYSGEN data and system program from the system ROM. When the initialization is completed the console device displays a Softkey menu. It is this menu that prompts the user to select the mode of operation required. The Softkey prompts displayed at this time are:

1:SYSGEN 2:MEMORY 3:EMULATE 4:SYMBOL
5:TERMINAL 6:PROM 7:TRACE 8:SPEED

These Softkey prompts represent the primary modes of operation for the LCE system. When the function key corresponding to the prompt location is pressed, one of the following modes is selected:

SYSGEN — This mode allows the user to modify the ROM-stored system parameters on either a permanent (until another power-up condition) or a temporary basis.

MEMORY — This mode allows the user to display or modify the contents of Target as well as Prototype memory.

EMULATE — This mode provides all the functions for controlling run-time characteristics and emulation.

SYMBOL — This mode contains the functions which control the generation and use of symbol tables as it relates to MEMORY functions.

TERMINAL — This mode echoes each character entered from the console device to the host system.

PROM — This mode selects the command options for the optional PROM Programmer module.

TRACE — This mode selects the command options for the optional TRACE module.

SPEED — This mode selects the speed of dump and disassemble data being displayed to the console.

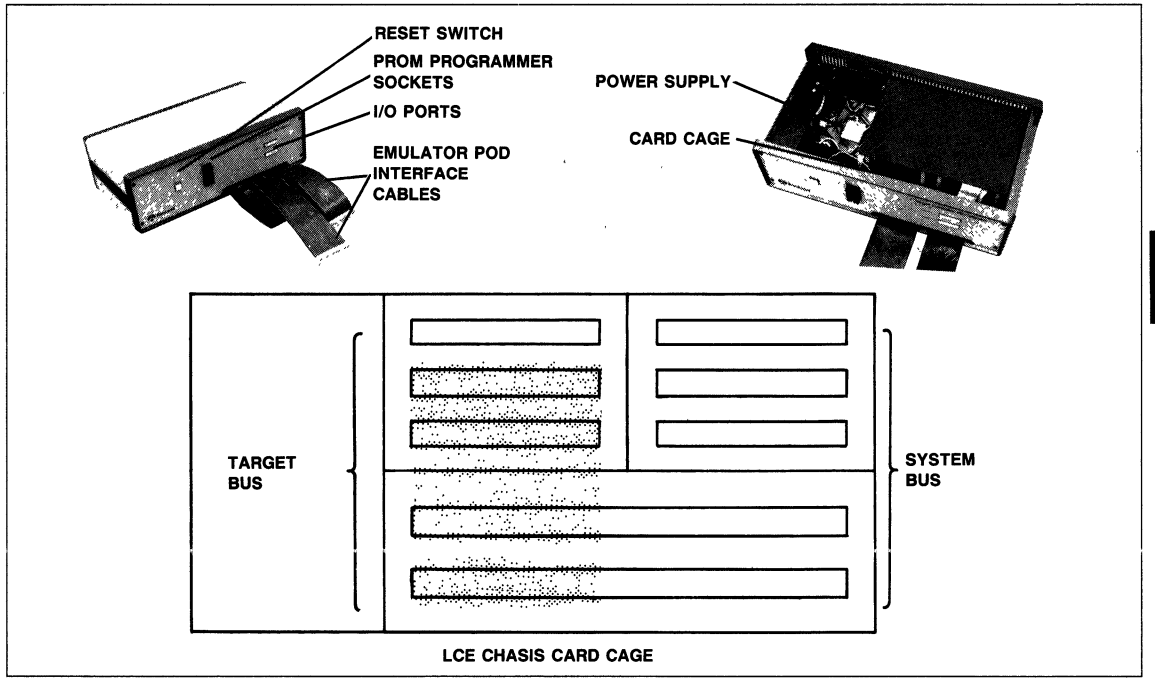
Each Softkey prompt, when selected by the number key, invokes a new set of Softkey prompts which further define the tasks to be performed by the mode. As an example, if the SYSGEN prompt is selected, a new Softkey prompt menu displays:

1:PORT1 2:PORT2 3:TARGET
4:PROTECT 5:BEEPER 6:DISPLAY 7:EXIT

If PROTECT is selected from this prompt, a new menu displays:

1:PROTECT 2:UNPROTECT 3:CLEARALL 4:DISPLAY

This hierarchy continued until all parameters of the tasks of the mode selected have been established. At any time during the mode selection process the user has the option of calling back the previous set of Softkey menu prompts by simply pushing the Ø or – (minus) key.



LCE Internal Layout and Card Cage Bus Structure

Software Command Overview

SYSGEN FUNCTIONS

BAUD	Select baud rate and parity options
WORD LEN	Select serial word length
DELAY	Set delay after linefeed between 0 to 99 mS
FORMAT	Set record format for data files (;,:, or Block)
START CHAR	Set start of file marker character
STOP CHAR	Set end of file marker character
SYSTEM	Select the system console port
TARGET	Select the processor type for emulation
PROTOTYPE	Select areas to mapped external of LCE target memory
PROTECT	Set and clear areas to be write protected
BEEPER	Turn on or off the BELL to indicate errors
DISPLAY	Show the current sysgen setup parameters
EXIT	Accept the current sysgen parameters and exit to primary menu

DEBUG FUNCTIONS

DUMP	Show a screen image at user memory (Hex and ASCII)
MODIFY	Show user memory and allow changes (Hex or ASCII)
ASSEMBLER	Assemble op code text into user memory
DISASSM	Dissassemble op code image of user memory
LOAD	Load a file image into user memory
SAVE	Save a file image of user memory
VERIFY	Verify a file image with user memory
STEP	Execute user program displaying every instruction and associated registers
RUN	Execute user program at full speed until any break condition occurs
SNAPSHOT	Execute user program displaying only breakpoint instructions and registers
MATCH	Execute user program at full speed until a break condition (except BP1 or BP2)
RESET	Reset all debug parameters and hardware
BREAK	Show and accept changes to the breakpoint conditions

MISCELLANEOUS FUNCTIONS

LIST	Show the user symbol table
CREATE	Adapt labels changes to the symbols tables
LOADSYM	Load a file image of the symbol table
SAVESYM	Save a file image of the symbol table
CLRSYM	Clear out the present user symbol table
SYMBOL	Turn on or off the user of labels in disassembly
OBJECT	Turn on or off the creation of object code field in disassembly
SHOW	Show status of symbolic options
SPEED	Control the rate of display update
TERMINAL	Allow transfer between port 1 and port 2 directly
PROM	Future option—PROM Programmer module
TRACE	Future option—Trace module

INTERFACE

Interface between the LCE system control modules and the port connectors on the front panel are made through ribbon cables. The ribbon cables are permanently attached to the port connectors. The LCE Cable Interface figure shows how these cables are routed in the system. The Self-Test Panel mates to the SBC module I/O connector. The optional PROM programmer module connects to the PROM socket through a single ribbon cable.

SPECIFICATIONS

Parameter	LCE Mainframe
Dimensions	
Height	5 in. (12.7 cm)
Width	14 in. (35.56 cm)
Depth	10 in. (25.4 cm)
Weight	20 lbs. (9 kg)
Electrical	
AC Input Voltage	105 to 125 (RDC-3101) 210 to 250 (RDC-3102)
AC Frequency	47 to 63 Hz
Fuse Requirement	3 A slo-blo (RDC-3101) 1.5 A slo-blo (RDC-3102)
Environmental	
Temperature	59°F to 104°F (15° to 40°C) operating
With/Disk Media	−4°F to 140°F (−20°C to 60°C) shipping −4°F to 122°F (−20°C to 150°C) storage
Humidity	20% to 80% non-condensing operating 1% to 95% non-condensing shipping 1% to 95% non-condensing storage

ORDERING INFORMATION

Part Number	Description
RDC-3101	LCE System (100 Vac)(1)
RDC-3102	LCE System (220 Vac)(1)
RDC-1020	64K Target RAM Module
RDC-1022	32K Target RAM Module
RDC-1024	8K Target RAM Module
RDC-3030	PROM Programmer Module
RDC-2000	R6500 Cross Assembler for IDS
RDC-2005	R6500 Cross Assembler for PDS
Order Number(2)	**Document Title**
RDC06	RDC R6500/* Personality Set Data Sheet
RDC11	RDC R6502-R65C02 Personality Set Data Sheet
RDC09	R6500 Cross Assembler for IDS Data Sheet
RDC23	R6500 Cross Assembler for PDS Data Sheet

Notes:
(1) Both system configurations are shipped with the following components:
- LCE Mainframe
- Three System Control modules—ACIA, SBC, and Universal RAM
- PMC and all Required Interface Cables
- Documentation Package

(2) Documents provide further information about the LCE system.

PERSONALITY SETS

Personality Sets are available for the LCE that allow emulation, development, and software debugging of the complete family of R6500/* Microcomputers and R6502-R65C02 Microprocessors. The microcomputers and microprocessors supported by Personality Sets are:

R6500/*		R6502–R65C02	
• R6500/1P	• R6500/41P	• R6502	• R6512
• R6500/11P	• R6500/42P	• R6503	• R6513
• R6500/12P	• R6500/43P	• R6504	• R6514
• R6500/13P	• R6501Q	• R6505	• R6515
• R6500/15P	• R6511Q	• R6506	• R65C02
• R6500/16Q	• R6541Q	• R6507	• R65C102
			• R65C112

For complete information on ordering any particular Personality Set or groups of Personality Sets, refer to the RDC R6500/* Personality Set Data Sheet, Order Number RDC06, or RDC R6502-R65C02 Personality Set Data Sheet, Order Number RDC11.

TYPICAL SYSTEM CONFIGURATION

A typical LCE order should consist of the following

LCE System		Target RAM		Personality Set
RDC-3101 (110V) or RDC-3102 (220V)	+	RDC-1024 (8K RAM) or RDC-1022 (32K RAM)	+	RDC-3XX(1) (R6500/*) or RDC-50X(2) (R6502-R65C02)

(1) Refer to RDC06 for ordering information
(2) Refer to RDC11 for ordering information
These components and a user supplied terminal are all that is required for full in-circuit emulation.

6

RDC-3XX
ROCKWELL DESIGN CENTER (RDC)
R6500/* PERSONALITY SET

INTRODUCTION

The RDC R6500/* Personality Set is a Rockwell Design Center (RDC) option that allows the Multiple Target Development System (MTDS) or Low Cost Emulator (LCE) user to develop, debug and verify programs intended for use by any R6500 one-chip microcomputer system. The R6500/* offers the user a high performance development system specifically designed for emulation of a microcomputer system. This RDC option supports in-circuit emulation for the entire R6500 NMOS family of one-chip microcomputers.

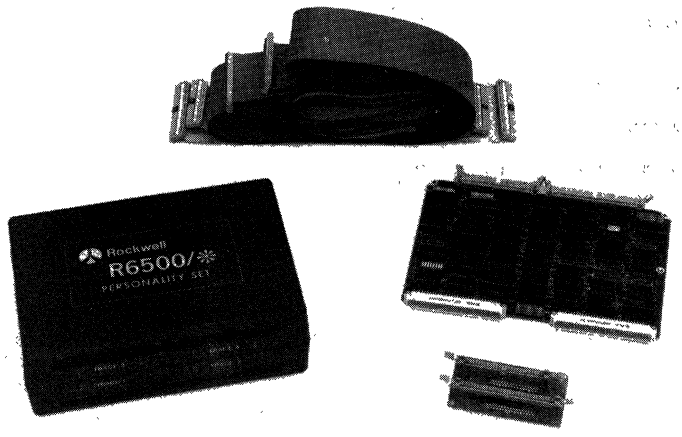
The basic MTDS R6500/* Personality Set includes a Personality Module Controller (PMC), two Personality Emulator Pod Modules, a Device Adapter, an In-Circuit Emulation Probe assembly, an interconnect cable set, and the required software and support documentation.

The R6500/* Personality Set provides the MTDS or LCE with a dual CPU capability. This added feature permits the MTDS or LCE CPU to maintain control and check for breakpoint conditions while the R6500/* CPU is executing a user program, thus providing the user with complete control over the development process.

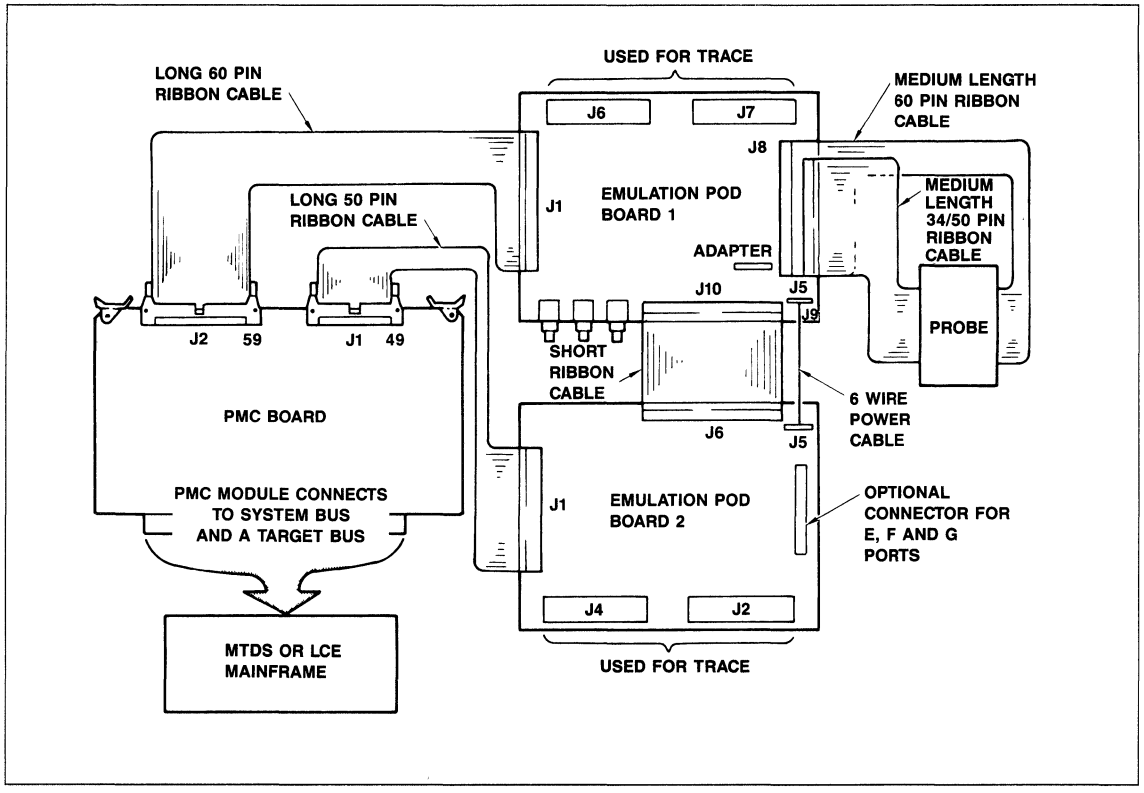
The R6500/* Personality Set can be expanded to include four separate emulation systems which can be run concurrently on the MTDS.

FEATURES

- Disk-based debug monitor and macro assembler (MTDS)
- ROM-based debug monitor and assembler (LCE)
- Real-time in-circuit emulation up to 2 MHz
- Supports full 65K address range for user in prototype or target environment
- Five hardware breakpoints with 2 SYNC outputs for oscilliscope or logic analyzer triggers
- User defined input for external break signal
- Single step through interrupts
- Supports four target developments (MTDS)
- No zero page address conflicts between user and system
- Power down capability
- RAM write protection/detection on 16 byte boundaries
- User or system supplied power and clock
- Supports 8K/32K/64K target RAM for user emulation memory (optional)



RDC R6500/* Personality Set



System Interconnection

EXECUTION COMMAND SUMMARY

The R6500/* Personality Set is designed to allow the R6500/* to execute independent of the MTDS or LCE. Thus, while the R6500/* is executing code, the MTDS or LCE CPU is still in operation. This allows certain functions to be performed by the MTDS or LCE CPU without disturbing the execution of the R6500/*.

The R6500/* Personality Set hardware supports the LCE and MTDS debug software in the following commands:

Memory Functions

Dump memory in Hex and ACSII format
Modify or alter selected memory locations in Hex or ASCII
Examine/modify RAM and I/O one byte at a time (LCE)
Assemble or code text into text memory (LCE)
Disassemble or code image of user memory
Load an object code file into user memory
Save an object file from user memory
Verify an object file with memory
Write protect memory blocks
Select memory areas to be prototype or target environment

Execution Functions

Step through a user program displaying instructions and registers
Run through a program at full execution speed stopping at at breakpoints
Run at full speed with breakpoint signals on Sync connectors (LCE)
Reset the debugger
Examine or alter the registers
Set or modify hardware breakpoints

6

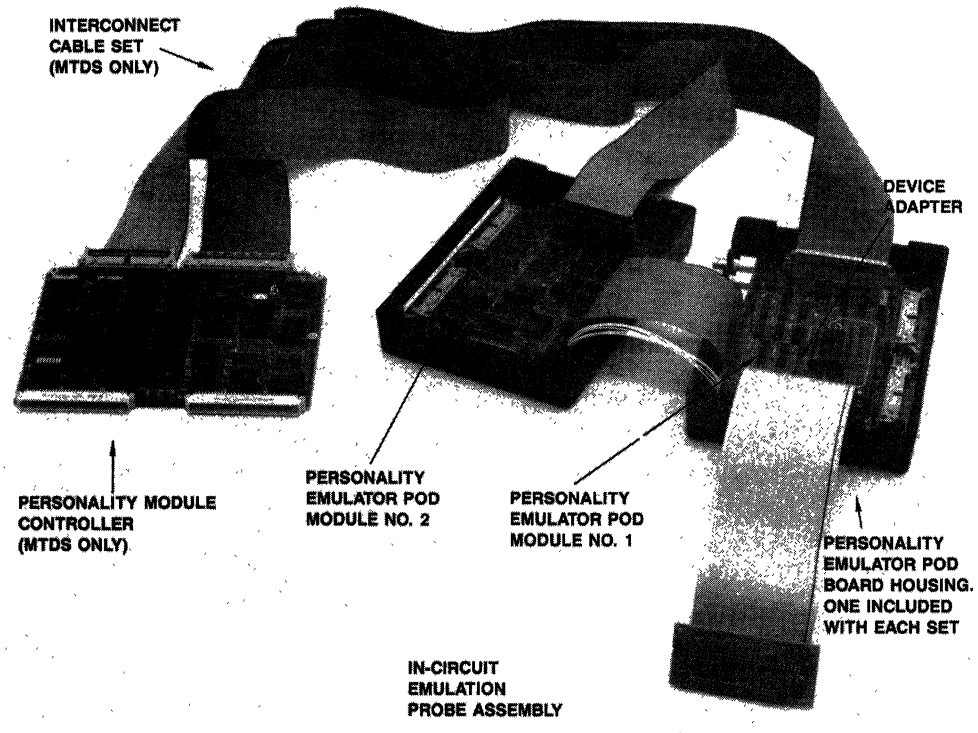
CONFIGURATIONS

The RDC Personality Sets for the R6500/* Microcomputers, shown in the chart below, include one Personality Module Controller (PMC), two Personality Emulator Pod Modules, a Device Adapter, an In-Circuit Emulation Probe assembly, an interconnect cable set, and the required software and support documentation. The LCE configurations do not include a PMC or interconnect cable set because these are already installed as part of the LCE system. The RDC Personality Sets are unbundled without the 8K/32K/64K Target RAM option. This option is needed with typical emulation configurations.

R6500/* Personality Sets

Part Number		Description
MTDS	LCE	
RDC-302	RDC-309	R6500/11, /15 Personality Set, 1 or 2 MHz
RDC-312	RDC-319	R6500/12, /16 Personality Set, 1 or 2 MHz
RDC-322	RDC-329	R6500/13 Personality Set, 1 or 2 MHz
RDC-332	RDC-339	R6500/41 Personality Set, 1 or 2 MHz
RDC-342	RDC-349	R6500/42 Personality Set, 1 or 2 MHz
RDC-352	RDC-359	R6500/43 Personality Set, 1 or 2 MHz
RDC-362	RDC-369	R6500/1 Personality Set, 1 or 2 MHz

Note: MTDS version includes PMC and cables.



Typical R6500/* Personality Set Hardware Components

DEVICE ADAPTERS

The Adapter/Emulator Devices are used to reconfigure RDC Personality Sets for use with other R6500/* Microcomputers. They replace the Adapter/Emulator Devices in the Personality Emulator Pod Module and contain the desired emulator device.

Part Number	Description
RDC-212	Adapter/Emulator Device (R6511AQ) for R6500/11/12/13/15/16, 1 or 2 MHz
RDC-222	Adapter/Emulator Device (R6541AQ) for R6500/41/42/43, 1 or 2 MHz
RDC-232	Adapter/Emulator Device (R6500/1EAC) for R6500/1, 1 or 2 MHz

IN-CIRCUIT EMULATION PROBES

The In-Circuit Emulation Probe assemblies used to reconfigure the RDC Personality Sets for use with other R6500/* Microcomputers are shown in the chart below.

Part Number	Description
RDC-200	40-Pin Probe and cable for R6500/11P/15P. Prerequisite, RDC-212
RDC-201	64-Pin Probe and cables for R6500/12Q/16Q. Prerequisite, RDC-212
RDC-202	64-Pin Probe and cables for R6500/13Q. Prerequisite, RDC-212
RDC-203	40-Pin Probe and cable for R6500/41P. Prerequisite, RDC-222
RDC-204	64-Pin Probe and cables for R6500/42Q. Prerequisite, RDC-222
RDC-205	64-Pin Probe and cables for R6500/43Q. Prerequisite, RDC-222
RDC-206	40-Pin Probe and cable for R6500/1P. Prerequisite, RDC-232

Rockwell

RDC-502, RDC-504 AND RDC-509 ROCKWELL DESIGN CENTER R6502-R65C02 PERSONALITY SET

INTRODUCTION

The RDC R6502-R65C02 Personality Set is a Rockwell Design Center (RDC) option that allows the Multiple Target Development System (MTDS) or Low Cost Emulator (LCE) user to develop, debug and verify programs intended for use by any R6500 one-chip microprocessor system. The R6502-R65C02 offers the user a high performance development system specifically designed for emulation of a microprocessor system. This RDC option supports in-circuit emulation for the entire R6500 and R65C00 family of one-chip microprocessors.

The basic MTDS R6502-R65C02 Personality Set includes a Personality Module Controller (PMC), two Personality Emulator Pod Modules, two emulator devices (R6502, and R65C02), two prototype-to-pod interface cables, an interconnect cable set, and the required software and support documentation.

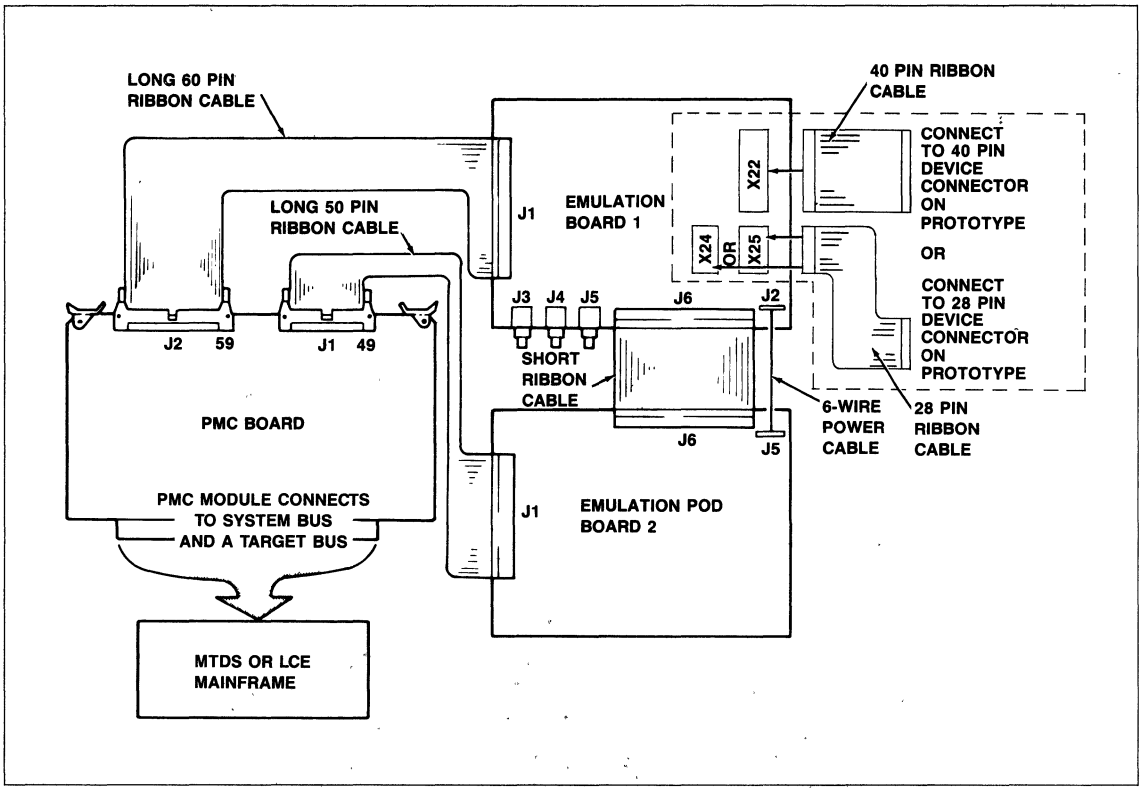
The R6502-R65C02 Personality Set provides the MTDS and LCE with a dual CPU capability. This added feature permits the MTDS and LCE CPU to maintain control and check breakpoint conditions, even while the microprocessor is executing a user program, thus providing the user with complete control over the development process.

The R6502-R65C02 Personality Set can be expanded to include four separate emulation systems which can be run concurrently on the MTDS.

FEATURES

- ROM-based debug monitor and assembler (LCE)
- Disk-based debug monitor and macro assembler (MTDS)
- Real-time in-circuit emulation up to 4 MHz
- Supports full 65K address range for user in prototype or target environment
- Five hardware breakpoints with 2 SYNC outputs for oscilliscope or logic analyzer triggers
- User defined input for external break signal
- Single step through interrupts
- Supports four target developments (MTDS)
- No zero page address conflicts between user and system
- Power down capability
- RAM write protection/detection on 16 byte boundaries
- User or system supplied power and clock
- Supports 8K/32K/64K target RAM for user emulation in system (optional)

RDC R6502-R65C02 Personality Set



System Interconnection

EXECUTION COMMAND SUMMARY

The R6502-R65C02 Personality Set is designed to allow R650X, R651X or R65XXX devices to execute independent of the MTDS or LCE. Thus, while the emulator is executing code, the CPU is still in operation. This allows certain functions to be performed by the MTDS or LCE CPU without disturbing the execution of the emulator device.

The R65C02 Personality Set hardware supports the LCE and MTDS debug software in the following commands:

Memory Functions

- Dump memory in Hex and ACSII format
- Modify or alter selected memory locations in Hex or ASCII
- Examine/modify RAM and I/O one byte at a time (LCE)
- Assemble or code text into text memory (LCE)
- Disassemble or code image of user memory
- Load an object code file into user memory
- Save an object file from user memory
- Verify an object file with memory
- Write protect memory blocks
- Select memory areas to be prototype or target environment

Execution Functions

- Step through a user program displaying instructions and registers
- Run through a program at full execution speed stopping at at breakpoints
- Run at full speed with breakpoint signals on Sync connectors (LCE)
- Reset the debugger
- Examine or alter the registers
- Set or modify hardware breakpoints

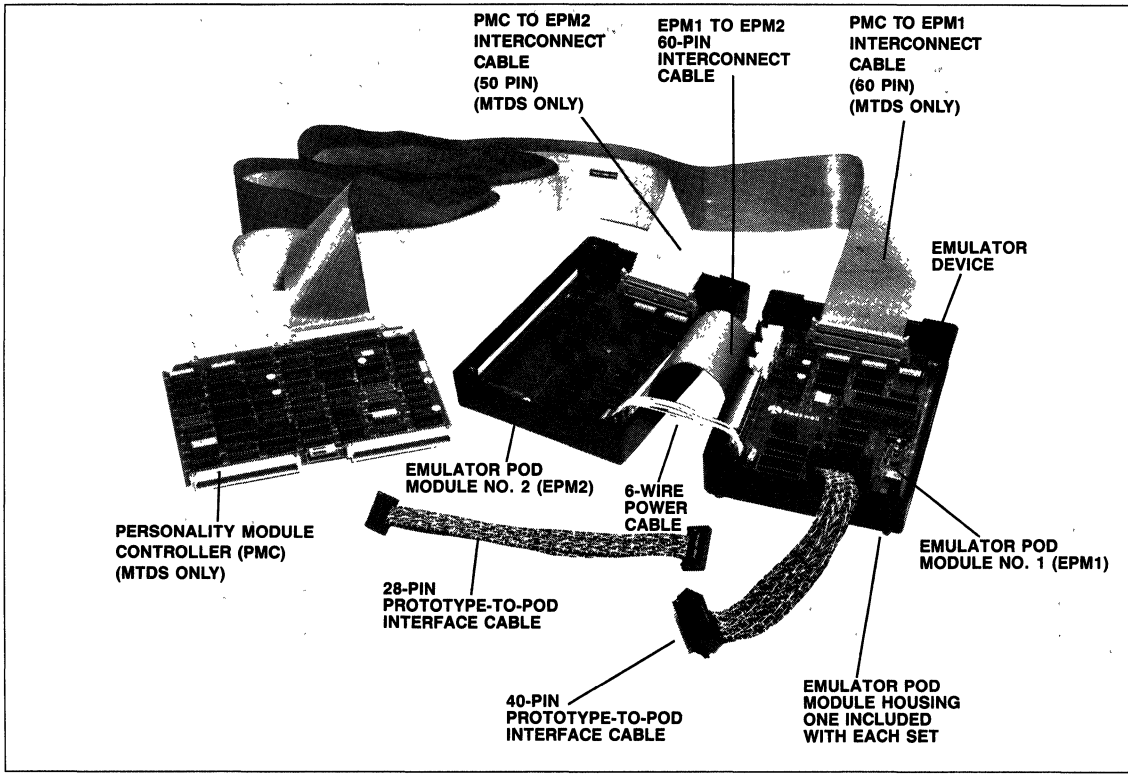
6

CONFIGURATIONS

The RDC Personality Sets for the R6502-R65C02 Microprocessors, shown in the chart below, include one Personality Module Controller (PMC), two Personality Emulator Pod Modules, one Emulator Device set, an interconnect cable set, and the required software and support documentation. In the LCE configuration, the PMC and interconnect cables are already installed in the LCE as part of the system package.

R6502-R65C02 Personality Sets and Memory

Part Number	Description
RDC-502	R6502-R65C02 Personality Set, 1-2 MHz
RDC-509	R6502-R65C02 Personality Set, 1-2 MHz (LCE only)
RDC-1020	64K RAM Target Memory, 1-3 MHz
RDC-1022	32K RAM Target Memory 1-3 MHz
RDC-1024	8K RAM Target Memory, 1-3 MHz only



Typical R6502-R65C02 Personality Set Hardware Components

R6502-R65C02 Personality Set Component List

QUANTITY	ITEM	DESCRIPTION
1	PMC Module	Controller module that plugs into the MTDS and LCE Mainframe. (MTDS only, PMC is installed in LCE when system is shipped.)
1	Emulator Pod Module Assembly	Pod that contains EPM-1 and EPM-2, a short ribbon cable, a six-wire power cable, and the R6502 Emulator Device.
1	Emulator Package	Package contains the R6512, R65C02, R65C102 and R65C112 Emulator devices and 5 jumper headers for the 28-pin processors.
2	PMC to Pod Interface Ribbon Cables (Long Length)	One cable with 60-pin connector on each end with one cable with a 50-pin connector on each end. (MTDS only, cables installed in LCE prior to shipment).
2	Prototype-to-Pod Interface Cables (Medium Length)	One of two possible configurations: a. One ribbon cable with 40-pin connectors on each end. Used for emulating the R6502, R6512, R65C02, R65C102 or R65C112. b. One cable with a 28-pin connector on each end. Used for emulating the R6503, R6504, R6505, R6506, R6507, R6513, R6514 or R6515.

Rockwell

RDC-2000 R6500 CROSS ASSEMBLER FOR INTEL DEVELOPMENT SYSTEM

CROSS ASSEMBLY

The R6500 Cross Assembler provides the user with the capability of developing assembly language programs on the Intel Development System and downloading these programs to the Multiple Target Development System (MTDS) or Target Emulator Workstation (TEW) for debugging and in-circuit operation.

The process of translating microprocessor instructions for a computer program written in symbolic form to executable machine instructions is called an assembly, and the computer program that performs this translation is called an assembler. Assemblers that run on a host computer different from the target computer that the generated machine code is to operate in are called cross assemblers. One assembly language statement usually translates into a single processor instruction. Each statement consists of a label (if required), an arithmetic operator (if required) and an optional comment. Constants are comprising one or more bytes of memory are generated from data statements while one or more bytes of memory are assigned to variables. This cross assembler is a symbolic assembler that allows the programmer to represent memory locations and numeric values with names or symbols.

PRODUCT OVERVIEW

The R6500 Cross Assembler for the Intel Development System allows users who have access to such a system and are accustomed to its text editor (ISIS CREDIT) to enter and edit source code, assemble the program and save both the source and object code on floppy disk. The object code can then be loaded into a MTDS or TEW for program debugging and in-circuit validation using an R6500, R6500/* or R65C00 Personality Set. Up to four personality sets can be installed in one MTDS or TEW main frame to maximize the utility of one Intel Development System and MTDS or TEW. The object code can also be programmed into PROM/ROM for execution by an R6500 NMOS or R65C00 CMOS microprocessor or masked in R6500/* NMOS one-chip microcomputer ROM for execution.

The disk-based R6500 cross assembler is a two-pass symbolic assembler which produces absolute 6500 object code. It performs symbol (1 – 6 characters) definition, syntax checking, assembly/symbol table listings and cross reference generation for effective program development. Assembler operation is automatic once started.

The assembler outputs to the console the pass it is currently performing and a dot for every 16 lines of source code assembled. This enables viewing of the assembly process and observation of detected errors. List (.LST), object (.OBJ), and symbol (.SYM) files are automatically generated with the source name assigned as the header and the particular extension added.

FEATURES

- Intel Development System Host
- Supports Rockwell's 8-bit CPU devices:
  - —R6500 NMOS microprocessor family
  - —R6500/* NMOS microcomputer family
  - —R65C00 CMOS microprocessor family
- Symbolic notation—operands and labels
- Interactive assembler operation
- Operator selected object code output devices
  - —Display/printer
  - —Printer
  - —Floppy Disk
  - —Download to MTDS or TEW
- Operator selected assembly/error listing output
  - —Display/Printer
  - —Printer
  - —Floppy Disk
- Assembler directives
- Symbolic cross-reference
- Communications support—downloading of object code

ORDERING INFORMATION

Part No.	Description
RDC-2000	R6500 Cross Assembler for Intel Development System Disk (8″ ISIS II compatible disk)
Order No.	**Description**
RDC02	R6500 Cross Assembler for Intel Development System User's Manual (included with RDC-2000)

SYSTEM REQUIREMENTS

The Intel Development System must provide 64K bytes of memory and the Dual-Density Drive option to support the R6500 Cross Assembler. 32K bytes are then available for application source code. The other 32K bytes contain the ISIS system (14K) and the cross assembler (18K).

Assembler Directives

Assembly Listing Control

.TTL	Title	.WIDTH	Line Length
.PAGE	Page	.SKIP	Skip
.LINE	Page Length		

Source File Control

.END	End of Assembly
.MOD	Assembly Type

Data Storage

.BYTE	Initialize byte memory location
.WORD	Generate 16-bit address
.DBYTE	Generate 16-bit data word
.SBYTE	Initialize ACSII string

Equate

=	Assign value to symbol

Error Codes

Pass 1

1 OPERAND VALUE IS INVALID OR GT HEX FFF
2 OPERAND VALUE IS GREATER THAN HEX FFFF
3 INCORRECT ADDRESSING MODE
4 SYMBOL NOT PREVIOUSLY DEFINED
5 NO OPERAND
6 ASCII STRING NOT PROPERLY ENCLOSED
7 MISSING .END STATEMENT
8 UNDEFINED ASSEMBLER DIRECTIVE
9 IMPROPER EQUATE FORMAT
10 UNRECOGNIZABLE ASTERISK DEFINITION
11 INDIRECT ADDRESSING OFF OF ZERO PAGE
12 INCORRECT FORM OF INDIRECT ADDRESSING, MISSING Y
13 INCORRECT FORM OF INDEX ADDRESSING, MISSING X
14 OPERAND MUST BE ON ZERO PAGE (00 – $FF)
15 ILLEGAL INSTRUCTION FOR THIS ASSEMBLER

Pass 2

1 .MOD DIRECTIVE MUST BE FIRST LINE ON LISTING
2 INCORRECT FORMAT OF INDEX ADDRESSING, MISSING X OR Y
3 MISSING RIGHT PARENTHESIS
4 LABEL LONGER THAN 6 CHARACTERS
5 LABEL IS DEFINED MORE THAN ONCE
6 RELATIVE BRANCH IS OUT OF RANGE
7 ILLEGAL OR MISSING OPCODE
8 OPERAND LABEL IS DEFINED MORE THAN ONCE
9 SYMBOL TABLE FULL
10 MISSING LABEL FOR EQUATE
11 OPERAND LABEL GREATER THAN 6 CHARACTERS LONG
12 .MOD VALUE IS INCORRECT FOR THIS ASSEMBLER
13 OPERAND NOT BETWEEN 0 – 7
14 SYMBOL HAS ILLEGAL CHARACTER OR IS GREATER THAN ZIJFF

Operators

Prefix Character	Base
(none)	10 (Decimal)
$	16 (Hexadecimal)
@	8 (Octal)
%	2 (Binary)

Constants (Prefix)

Operator	Operation
+	Addition
–	Subtraction
>	High-Byte Selection
<	Low-Byte Selection

Rockwell

RDC-2005
R6500 CROSS ASSEMBLER FOR INTEL PERSONAL DEVELOPMENT SYSTEM

CROSS ASSEMBLY

The R6500 Cross Assembler provides the user with the capability of developing assembly language programs on the Intel Personal Development System (PDS) and downloading these programs to the Low Cost Emulator (LCE) for debugging and in-circuit operation.

The process of translating microprocessor instructions for a computer program written in symbolic form to executable machine instructions is called an assembly, and the computer program that performs this translation is called an assembler. Assemblers that run on a host computer different from the target computer that the generated machine code is to operate in are called cross assemblers. One assembly language statement usually translates into a single processor instruction. Each statement consists of a label (if required), an arithmetic operator (if required) and an optional comment. Constants are comprising one or more bytes of memory are generated from data statements while one or more bytes of memory are assigned to variables. This cross assembler is a symbolic assembler that allows the programmer to represent memory locations and numeric values with names or symbols.

PRODUCT OVERVIEW

The R6500 Cross Assembler for the Intel Personal Development System allows users who have access to such a system and are accustomed to its text editor (ISIS CREDIT) to enter and edit source code, assemble the program and save both the source and object code on floppy disk. The object code can then be loaded into a LCE for program debugging and in-circuit validation using an R6500, R6500/* or R65C00 Personality Set. The object code can also be programmed into PROM/ROM for execution by an R6500 NMOS or R65C00 CMOS microprocessor or masked in R6500/* NMOS one-chip microcomputer ROM for execution.

The disk-based R6500 cross assembler is a two-pass symbolic assembler which produces absolute 6500 object code. It performs symbol (1–6 characters) definition, syntax checking, assembly/symbol table listings and cross reference generation for effective program development. Assembler operation is automatic once started.

The assembler outputs to the console the pass it is currently performing and a dot for every 16 lines of source code assembled. This enables viewing of the assembly process and observation of detected errors. List (.LST), object (.OBJ), and symbol (.SYM) files are automatically generated with the source name assigned as the header and the particular extension added.

FEATURES

- Intel Personal Development System Host
- Supports Rockwell's 8-bit CPU devices:
  - —R6500 NMOS microprocessor family
  - —R6500/* NMOS microcomputer family
  - —R65C00 CMOS microprocessor family
- Symbolic notation—operands and labels
- Interactive assembler operation
- Operator selected object code output devices
  - —Display/printer
  - —Printer
  - —Floppy Disk
  - —Download to LCE
- Operator selected assembly/error listing output
  - —Display/Printer
  - —Floppy Disk
- Assembler directives
- Symbolic cross-reference
- Communications support—downloading of object code

ORDERING INFORMATION

Part No.	Description
RDC-2005	R6500 Cross Assembler for Intel Personal Development System Disk (5-1/4" ISIS II compatible disk)
Order No.	**Description**
RDC02	R6500 Cross Assembler for Intel Personal Development System User's Manual (included with RDC-2005)

Assembler Directives

Assembly Listing Control

.TTL	Title	.WIDTH	Line Length
.PAGE	Page	.SKIP	Skip
LINE	Page Length		

Source File Control

END	End of Assembly
.MOD	Assembly Type

Data Storage

.BYTE	Initialize byte memory location
.WORD	Generate 16-bit address
DBYTE	Generate 16-bit data word
SBYTE	Initialize ACSII string

Equate

=	Assign value to symbol

Error Codes

Pass 1

1 OPERAND VALUE IS INVALID OR GT HEX FFF
2 OPERAND VALUE IS GREATER THAN HEX FFFF
3 INCORRECT ADDRESSING MODE
4 SYMBOL NOT PREVIOUSLY DEFINED
5 NO OPERAND
6 ASCII STRING NOT PROPERLY ENCLOSED
7 MISSING END STATEMENT
8 UNDEFINED ASSEMBLER DIRECTIVE
9 IMPROPER EQUATE FORMAT
10 UNRECOGNIZABLE ASTERISK DEFINITION
11 INDIRECT ADDRESSING OFF OF ZERO PAGE
12 INCORRECT FORM OF INDIRECT ADDRESSING, MISSING Y
13 INCORRECT FORM OF INDEX ADDRESSING, MISSING X
14 OPERAND MUST BE ON ZERO PAGE (00–$FF)
15 ILLEGAL INSTRUCTION FOR THIS ASSEMBLER

Pass 2

1 MOD DIRECTIVE MUST BE FIRST LINE ON LISTING
2 INCORRECT FORMAT OF INDEX ADDRESSING, MISSING X OR Y
3 MISSING RIGHT PARENTHESIS
4 LABEL LONGER THAN 6 CHARACTERS
5 LABEL IS DEFINED MORE THAN ONCE
6 RELATIVE BRANCH IS OUT OF RANGE
7 ILLEGAL OR MISSING OPCODE
8 OPERAND LABEL IS DEFINED MORE THAN ONCE
9 SYMBOL TABLE FULL
10 MISSING LABEL FOR EQUATE
11 OPERAND LABEL GREATER THAN 6 CHARACTERS LONG
12 MOD VALUE IS INCORRECT FOR THIS ASSEMBLER
13 OPERAND NOT BETWEEN 0–7
14 SYMBOL HAS ILLEGAL CHARACTER OR IS GREATER THAN ZIJFF

Operators

Prefix Character	Base
(none)	10 (Decimal)
$	16 (Hexadecimal)
@	8 (Octal)
%	2 (Binary)

Constants (Prefix)

Operator	Operation
+	Addition
–	Subtraction
>	High-Byte Selection
<	Low-Byte Selection

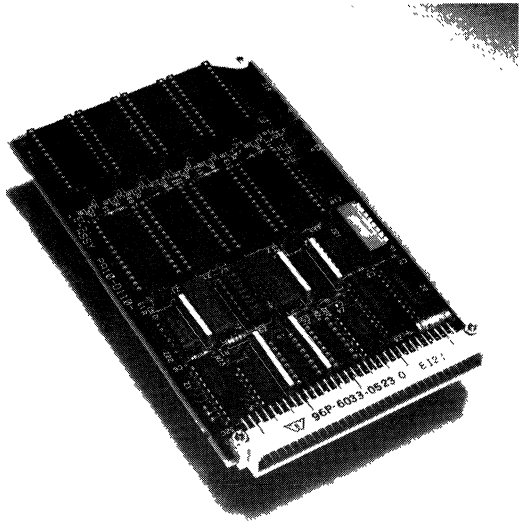
Rockwell

RDC-1020, RDC-1022 AND RDC-1024 ROCKWELL DESIGN CENTER (RDC) 8K/32K/64K TARGET RAM MODULE

INTRODUCTION

The 8K/32K/64K Target RAM Module is one of the hardware options available for the Rockwell Design Center Family of development systems.

The Target RAM Module supports memory operations in conjunction with the R6500/* and R6502-R65C02 Personality Sets used on both the Multiple Target Development System (MTDS) and Low Cost Emulator (LCE). The module in its 8K byte configuration also supports the ROM and RAM area for the TEW operating system.



8K/32K/64K Target RAM Module

FEATURES

- In the high speed mode, supports Multiple Target Development (MTDS) and Low Cost Emulator (LCE) 3 MHz RAM operations
- In the universal memory mode, supports 2K, 4K, 8K, and 16K byte-wide memory devices for up to 128K bytes of memory
- In the high speed mode, supports 8K devices for up to 64K bytes of memory (refer to Devices Supported for part numbers)
- On-board header and shunt configure the module into a 2K to 128K memory space
- Each half (four device sockets) independently configurable in the universal memory mode
- On-board memory bank select switches assign each half of the module to either one or both of two 64K memory banks
- On-board ROM select switches serve as write-protect switches for each half of the memory in universal memory mode
- Compact size—100 mm × 160 mm (approximately 3.9 in. × 6.3 in.)
- Operates from a single +5V power source
- Fully assembled (except for user-supplied memory devices), tested and warranted

OVERVIEW

Two major capabilities are provided in the Target RAM Module: the flexibility of using 2K, 4K, 8K, or 16K memory devices on the module, and use of the memory in either a high-speed mode or a universal memory mode. Typical data-transfer rates are up to 3 MHz (to support the MTDS and LCE) in the high speed mode and 1- to 2-MHz in the universal memory mode. Rates are dependent both on memory devices used and system configuration. Memory devices that can be used with the module are RAMs, ROMs, EPROMs, and EEPROMs.

ORDERING INFORMATION

Part No.	Description
RDC-1020	64K RAM Module (1 to 3 MHz)
RDC-1022	32K RAM Module (1 to 3 MHz)
RDC-1024	8K RAM Module (1 to 3 MHz)

FUNCTIONAL DESCRIPTION

Data Bus Transceivers buffer and invert data signals BD0/ through BD7/. Data signals from the RM 65 Bus pass through the bidirectional transceivers into the module during a write operation and out from the module through the transceivers to the RM 65 Bus during a read operation. Data in is inverted for use in the module, and data out (from the module) is inverted for use on the RM 65 Bus. Transfers occur when any of the chip-select signals and the Ø2 clock pulse are in the active states concurrently. Direction of data flow either into or out of the module is controlled by the R/$\overline{W}$ signal state.

Address and Control Buffer logic consists of inverters that buffer address signals BA0/ through BA13/ and the read/write signal BR/W/. These signals are converted to positive signals BA0 through BA13 and BR/W for use within the module.

Bank Address Select logic is controlled by the state of the BADR/signal, which functions as a seventeenth address bit. The state of the BADR/signal indicates which of the two 65K memory banks is addressed. In the high speed memory mode, the module can be configured to operate in either one or both 65K memory banks. In the universal memory mode, each half of the memory is configurable to either one or both 65K memory banks.

Module Active logic is enabled when any chip-select signal is enabled. Thus, when any memory device in either Memory A or Memory B is enabled by a chip-select signal, the BACT/, or Module Active, signal is in the active state.

Address signals BA13/, BA14/, and BA15/, in conjunction with B0, are decoded by a 3:8 decoder to enable one of eight possible outputs. Each output signal in a low state indicates an 8K address boundary signal. Thus, the 8K address boundaries are $0000, $2000, $4000, . . . $E000. Each of these signals is used as a memory chip-select signal during operation of the memory in the high-speed mode and as a 2K, 4K, 8K, and 16K decoder enabling signal in the universal memory mode.

By connecting a pin on the Address Header to a specific output (chip select) pin from the 8K Decoder, that 8K address boundary signal is connected to one specific memory device (in one of the eight memory device sockets) only in high speed mode.

The module can be used either as a high speed memory or as a universal memory. The removable 16-pin, 8-position shunt is placed either in the High Speed Option Shunt socket for high speed memory operation, or in the Universal Memory Option Shunt socket for universal memory operation. In the high speed mode, Memory A Decoder and Memory B Decoder are not used, and the address (chip-select) signal from the Address Header is applied directly to the applicable Memory A or Memory B devices. As a result, decoding time is saved.

Memory A consists of 2K, 4K, 8K, or 16K memory devices installed in the four sockets assigned as Memory A. Memory B also consists of memory devices located in four sockets designated as Memory B. Thus, the capacity of Memory A or Memory B is dependent on the capacity of the memory devices installed in each socket. Each of the two groups of four sockets can be configured with jumpers to accept one of the four types (2K, 4K, 8K, or 16K) of memory devices. Each memory device in the memory sockets in Memory A or Memory B must have the same capacity.

Device Select A consists of jumpers E3, E4, and E7 through E10 determine the particular type memory device (2K, 4K, 8K, or 16K) installed in the Memory A sockets. Similarly, Device Select B jumpers E5, E6, and E11 through E14 determine memory device types in Memory B.

Memory A Decoder is a programmable array logic (PAL) device internally configured to decode a combination of input signals and generate one output (chip-select) signal. Memory Decoders A and B are used only when the module is being operated in the universal memory mode. Both decoders operate in the same manner, but only one is used at a time. Thus, when Memory A is addressed, Memory Decoder A is used, and Memory Decoder B when Memory B is addressed.

DEVICES SUPPORTED

In the universal memory mode, the following is a partial list of devices supported:

16K of the following 2K devices:

R2316	ROM-Rockwell
2716	EPROM-Intel
2516	EPROM-TI
2016	RAM-Toshiba
5516	RAM-Toshiba
6116	RAM-Hitachi
R5213/2816	EEPROM-Rockwell
X2816	EEROM-XICOR

32K of the following 4K devices:

R2332	ROM-Rockwell
2732A	ROM-Intel
2532 (350 ns)	ROM-TI

64K of the following 8K devices:

R2364A, R2364B	ROM-Rockwell
68A764	EPROM-Motorola
68766	EPROM-Motorola
2764	EPROM-Intel
5564	RAM-Toshiba
6264	RAM-Hitachi
8464	RAM-Fujitsu

128K of the following 16K devices:

R23128	ROM-Rockwell
27128	EPROM-Intel

In the high speed mode, the following is a partial list of devices supported:

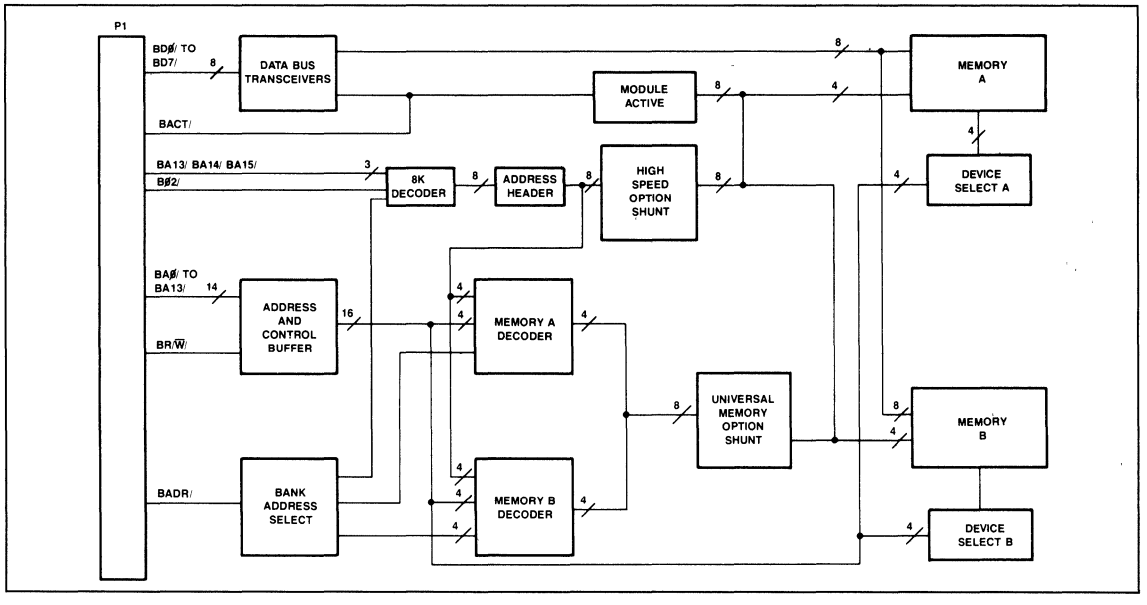
64K of the following 8K devices:

R2364A, R2364B	ROM-Rockwell
68A764	EPROM-Motorola
68766	EPROM-Motorola
2764	EPROM-Intel (TEW)
5564	RAM-Toshiba
6264	RAM-Hitachi (MTDS and TEW)
8464	RAM-Fujitsu

RM 65 Bus Pin Assignments

Bottom (Solder Side)			Top (Component Side)		
Pin	Signal Mnemonic	Signal Name	Pin	Signal Mnemonic	Signal Name
1a	GND	Ground	1c	+5V	+5 Vdc
2a	BADR/	Buffered Bank Address	2c	BA15/	Buffered Address Bit 15
3a	GND	Ground	3c	BA14/	Buffered Address Bit 14
4a	BA13/	Buffered Address Bit 13	4c	BA12/	Buffered Address Bit 12
5a	BA11/	Buffered Address Bit 11	5c	GND	Ground
6a	BA10/	Buffered Address Bit 10	6c	BA9/	Buffered Address Bit 9
7a	BA8/	Buffered Address Bit 8	7c	BA7/	Buffered Address Bit 7
8a	GND	Ground	8c	BA6/	Buffered Address Bit 6
9a	BA5/	Buffered Address Bit 5	9c	BA4/	Buffered Address Bit 4
10a	BA3/	Buffered Address Bit 3	10c	GND	Ground
11a	BA2/	Buffered Address Bit 2	11c	BA1/	Buffered Address Bit 1
12a	BA0/	Buffered Address Bit 0	12c	BØ1	*Buffered Phase 1 Clock
13a	GND	Ground	13c	BSYNC	*Buffered Sync
14a	BSO	*Buffered Set Overflow	14c	BDRQ1/	*Buffered DMA Request 1
15a	BRDY	*Buffered Ready	15c	GND	Ground
16a		*User Spare 1	16c	−12V/−V	*−12 Vdc/−V
17a	+12V/+V	*+12 Vdc/+V	17c		*User Spare 2
18a	GND	Ground Line	18c	BFLT/	*Buffered Bus Float
19a	BDMT/	*Buffered DMA Terminate	19c	BØ0	*Buffered External Phase 0 Clock
20a		*User Spare 3	20c	GND	Ground
21a	BR/$\overline{W}$/	Buffered Read/Write "Not"	21c	BDRQ2/	*Buffered DMA Request 2
22a		*System Spare	22c	BR/$\overline{W}$	*Buffered Read/Write
23a	GND	Ground	23c	BACT/	Buffered Bus Active
24a	BIRQ/	*Buffered Interrupt Request	24c	BNMI/	*Buffered Non-Maskable Interrupt
25a	BØ2/	Buffered Phase 2 "Not" Clock	25c	GND	Ground
26a	BØ2	Buffered Phase 2 Clock	26c	BRES/	*Buffered Reset
27a	BD7/	Buffered Data Bit 7	27c	BD6/	Buffered Data Bit 6
28a	GND	Ground	28c	BD5/	Buffered Data Bit 5
29a	BD4/	Buffered Data Bit 4	29c	BD3/	Buffered Data Bit 3
30a	BD2/	Buffered Data Bit 2	30c	GND	Ground
31a	BD1/	Buffered Data Bit 1	31c	BD0/	Buffered Data Bit 0
32a	+5V	+5 Vdc	32c	GND	Ground

Note: *Not used on this module

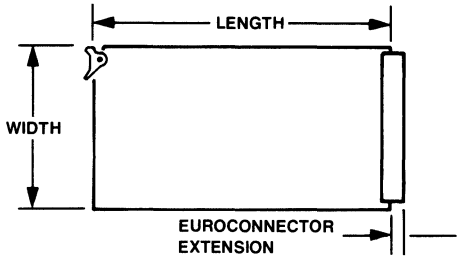


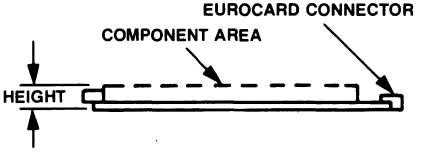
Target RAM Module Block Diagram

SPECIFICATIONS

Parameter	Value
Dimensions[1,2,3]	
Width	100 mm (3.94 in.)
Length	160 mm (6.3 in.)
Height	14 mm (0.55 in.)
Weight	156 g (5.5 oz.)
Environment	
Operating Temperature	0°C to 70°C
Storage Temperature	−40°C to 85°C
Relative Humidity	0% to 85% (without condensation)
Power Requirements	5 0V (420 ma. typical, 640 ma. maximum with no memory devices installed)
Connector	
RM 65 Bus Connector P1	64-pin plug (0.100 in centers) per DIN 41612 (Row b not installed)—mates with Burndy P196B32R00A00L-9 or equivalent

Notes
1 Height includes the maximum values for component height above the board surface (0 4 in. for populated modules), printed circuit board thickness (0.062 in.), and pin extension through the bottom of the module (0 1 in.)
2. Length does not include the added extension due to the module ejector
3 Dimensions conform to DIN 41612





Module Dimensions

6

Rockwell

RDC-1030 MULTIPLE TARGET DEVELOPMENT SYSTEM (MTDS) PROM PROGRAMMER MODULE

INTRODUCTION

The Multiple Target Development System (MTDS) is a development system vertically integrated to support the entire R6500 family of microprocessors and microcomputers. The MTDS allows emulation, development, and software debugging of up to four separate microprocessors and microcomputers concurrently, even if the four devices are different members of the R6500 family. The MTDS is a disk-based system with two 96 TPI, double-sided, double-density 5¼-inch floppy disk drives that provide a storage capacity of up to 1.3M bytes of data (formatted).

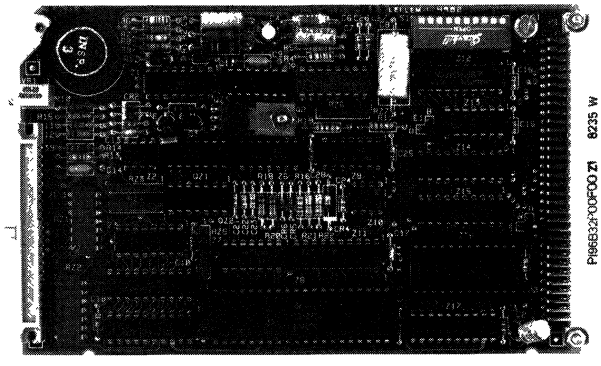
A unique bus structure provides a separate system bus and four target busses which can operate at different speeds (up to 4 MHz). Construction of the MTDS is modular based on the proven RM 65 microcomputer module design using both single- and double-sized Eurocards and highly reliable DIN 41612 pin and socket connectors. The double Eurocards allow use of both the system bus and a target bus which can operate at different speeds.

PRODUCT OVERVIEW

The RDC-1030 PROM Programmer Module, in conjunction with the MTDS, programs industry standard 2K-, 4K- and 8K-byte EPROMs (ultra-violet light erasable programmable read-only memories) and 2K-byte EEROMs (electrically erasable programmable read-only memories). The module consists of an RM 65 module and a 24-inch ribbon cable. A 28-pin and a 24-pin Zero Insertion Force (ZIF) socket are mounted on the MTDS mainframe to allow installation of a 28-pin or 24-pin PROM.

FEATURES

- Programs 2K-byte to 8K-byte UV EPROMs
  - —2K-byte: 2516, 2716
  - —4K-byte: 2532, 2732, 2732A
  - —8K-byte: 2564, 2764, 68764
- Erases and programs 2K-byte EEROMs
  - —2K-byte: R5213/2816, 5213, 2816, 48016
- Connects to PROM socket module installed in the MTDS with
  - —28-pin and 24-pin Zero Insertion Force (ZIF) sockets
  - —Connecting 24-inch cable to RM 65 module
- Easy-to-use interactive softkey commands
  - —PROM interface (check, program, read, verify)
  - —RAM preparation (alter and invert)
  - —Utility functions (PROM type selection, toggle verify mode, etc.)
- Verify during or after programming
- Compact size RM 65 module—about 100 mm × 160 mm (4 in. × 6¼ in.)
- +5V only operation (on-board DC/DC converter)
- Fully assembled and tested with one year warranty



RDC-1030 PROM Programmer Module

ORDERING INFORMATION

Part No.	Description
RDC-1030	MTDS PROM Programmer Module
Order No.	**Description**
RDC12	MTDS PROM Programmer Module User's Manual*

Note:
*Included with RDC-1030.

FUNCTIONAL DESCRIPTION

PROM PROGRAMMER MODULE

The Data Transceivers invert and transfer 8-bits of parallel data between the PROM Programmer module and the RM 65 data bus when enabled by the Chip Select Decoder. The read/write line from the RM 65 bus determines the direction of data flow. During a write operation, data is transferred from the bus to the module; during a read operation, data is transferred from the module to the RM 65 bus.

The Control Signal Buffers invert and transfer the phase 2, read/write, bank address and reset signals from the RM 65 bus to the module. The bus active signal is also driven to the RM 65 bus when data is being transferred between the RM 65 bus and the module.

Address Signal Buffers invert and transfer signals from 13 address lines from the RM 65 bus to the module.

The Chip Select Decoder, in conjunction with Base Address Select, Bank Select and Bank Select Enable switches and the ROM Range Select jumper decodes the address from the RM 65 bus and generates enable signals to other major on-board circuits. When the address matches the I/O Base Address switch positions, one of two Octal Latches, the on-board R6522 Versatile Interface Adapter (VIA), the Digital-to-Analog Converter (DAC) and/or the Data Bus Transceivers are enabled. When the address matches the ROM Base Address switch positions and ROM Range Selection jumper position, the on-board program ROM is enabled along with the Data Bus Transceivers.

Bank Select and Bank Select Enables switches assign the module to one or two 65K-byte memory banks. The Bank Select Enable switch assigns the module to be active in common memory (both Bank 0 and 1).

The R6522 VIA transfers 8-bit data between the RM 65 data bus and the PROM data lines and controls programming voltage levels. During PROM programming, the VIA transfers data from the Data Transceivers for writing into the PROM and during a PROM read, verify or check function, the VIA reads data from the PROM. During PROM programming, the VIA issues control signals to the Power Multiplexer, the Misplaced PROM Detector, and the Vpp Rise/Fall Time Controller.

The Programmable Voltage Regulator, consisting of the 8-bit DAC, a Vpp Rise/Fall Time Controller, a DC/DC Converter and an Analog Buffer, generates the Vpp programming voltage. The DAC outputs a voltage proportional to Vpp for the selected PROM type as controlled by 8-bit data received from the RM 65 data bus. The DAC output voltage is amplified to the full Vpp level, mixed with the rise or fall time control signal, clamped to minimum Vpp level, and output to the Analog Buffer. The +5 to +32V DC/DC Converter provides the high voltage used in the second stage of amplification. The Analog Buffer amplifies the Vpp current for use by the Power Multiplexer.

The Power Multiplexer selects the proper voltage level to output to the PROM during a programming or read operation as controlled by signals from the VIA and Octal Latch A. The output voltage is selected from TTL high, TTL low, Vcc and the Vpp output from the Analog Buffer. The correct voltage is selected by VIA output control lines.

The Misplaced PROM Detector determines if a 24-pin PROM has been installed in the 28-pin ZIF socket on the PROM module. The detected state is input to the VIA and sampled by the programming firmware to prevent application of programming voltage to a misplaced PROM.

The two Octal Latches, A and B, transfer addresses from the Address Buffers to the PROM during PROM access operations. The levels of three programming voltages output by the Power Multiplexer to the PROM are also controlled by Octal Latch A.

PROM SOCKETS AND INTERFACE CABLE

Both 28-pin and 24-pin Zero Insertion Force (ZIF) sockets are mounted on the front panel of the MTDS mainframe and connected to the PROM Programmer module by a 24-inch ribbon cable.

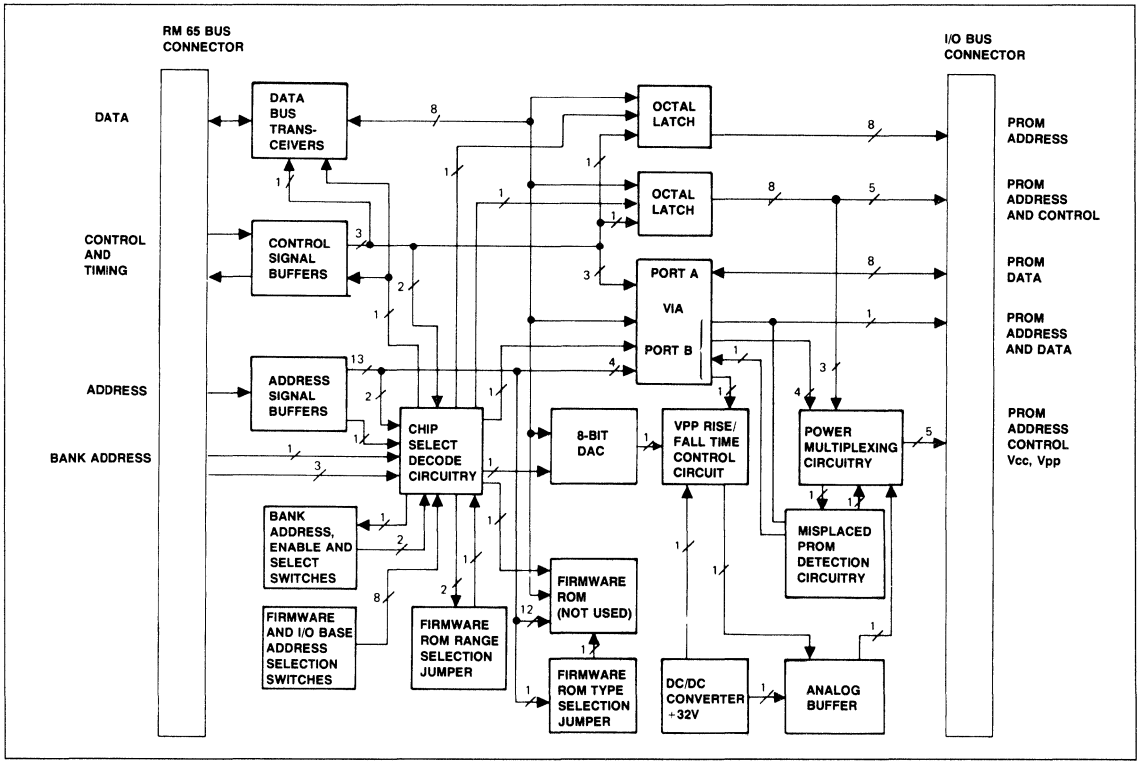
PROM PROGRAMMER COMMANDS

Computer program routines to operate the PROM Programmer module are provided on a diskette to be installed in the MTDS system. Easy-to-use interactive commands perform PROM interface functions (check, program, read and verify), RAM preparation functions (fill and invert) and utility functions (e.g., command and PROM type menus, toggle verification mode, and change PROM type).

PROM Programmer commands are invoked from a command softkey software mode the same as used in the standard MTDS software. The commands listed can then be selected by single keystrokes. Subprompts displayed upon command selection request entry of information pertinent to the specific function. Once initiated, each function operates automatically until successful completion or upon termination due to a detected error.

PROM PROGRAMMER FUNCTIONS

Command	Function
CHECK	Check PROM
PROGRAM	Program PROM
READ	Read PROM
VERIFY	Verify PROM
MODIFY	Modify Memory
ALTER	Alter Memory
INVERT	Invert Memory
SAVE	Save Memory
ERASE	Erase EEROM
SELECT	Select PROM Type
TOG.VER	Toggle Verify Mode
CHEKSUM	Checksum Memory
LOAD	Load
DUMP	Dump
DIR	Display Disk Directory
RENAME	Rename File
DELETE	Delete File
RECOVER	Recover Deleted File



PROM Programmer Module Block Diagram

PROM Socket Pin Assignment

Connector J1 (P2) Pin No.	24-pin PROM Socket Pin Number (1)	28-pin PROM Socket Pin Number	Signal Symbol	Signal Name	Connector J1 (P2) Pin No.	24-pin PROM Socket Pin Number (1)	28-pin PROM Socket Pin Number	Signal Symbol	Signal Name
3, 5, 10,	12	14	GND	Ground	16	9	11	Q0	Data Bit 0
15, 24, 26,					17	10	12	Q1	Data Bit 1
28, 30, 32					18	11	13	Q2	Data Bit 2
35, 37, 39					19	13	15	Q3	Data Bit 3
1, 40	—	28	VCC	PROM Supply Voltage	20	14	16	Q4	Data Bit 4
2	—	1	VPP	Programming Voltage	21	15	17	Q5	Data Bit 5
4	—	2	A12	Address Bit 12	22	16	18	Q6	Data Bit 6
6	1	3	A7	Address Bit 7	23	17	19	Q7	Data Bit 7
7	2	4	A6	Address Bit 6	25	18	20	$\overline{CE}$	Chip Enable
8	3	5	A5	Address Bit 5	27	19	21	A10	Address Bit 10
9	4	6	A4	Address Bit 4	29	20	22	$\overline{OE}$	Output Enable
11	5	7	A3	Address Bit 3	31	21	23	A11	Address Bit 11
12	6	8	A2	Address Bit 2	33	22	24	A9	Address Bit 9
13	7	9	A1	Address Bit 1	34	23	25	A8	Address Bit 8
14	8	10	A0	Address Bit 0	36	24	26	A13/V_{CC}(2)	Address Bit 13
					38	—	27	$\overline{PGM}$	Program

Note: (1) Nomenclature applies to the recommended JEDEC Bytewide pin-out.
(2) Applies to 24-pin devices

RM 65 Bus Pin Assignments

Bottom (Solder Side)			Top (Component Side)		
Pin	Signal Mnemonic	Signal Name	Pin	Signal Mnemonic	Signal Name
1a	GND	Ground	1c	+5V	+5 Vdc
2a	BADR/	Buffered Bank Address	2c	VA15/	Buffered Address Bit 15
3a	GND	Ground	3c	BA14/	Buffered Address Bit 14
4a	BA13/	Buffered Address Bit 13	4c	BA12/	Buffered Address Bit 12
5a	BA11/	Buffered Address Bit 11	5c	GND	Ground
6a	BA10/	Buffered Address Bit 10	6c	BA9/	Buffered Address Bit 9
7a	BA8/	Buffered Address Bit 8	7c	BA7/	Buffered Address Bit 7
8a	GND	Ground	8c	BA6/	Buffered Address Bit 6
9a	BA5/	Buffered Address Bit 5	9c	BA4/	Buffered Address Bit 4
10a	BA3/	Buffered Address Bit 3	10c	GND	Ground
11a	BA2/	Buffered Address Bit 2	11c	BA1/	Buffered Address Bit 1
12a	BA0/	Buffered Address Bit 0	12c	BØ1	*Buffered Phase 1 Clock
13a	GND	Ground	13c	BSYNC	*Buffered Sync
14a	BSO	*Buffered Set Overflow	14c	BDRQ1/	*Buffered DMA Request 1
15a	BRDY	*Buffered Ready	15c	GND	Ground
16a		*User Spare 1	16c	−12V/−V	*−12 Vdc/−V
17a	+12V/+V	*+12 Vdc	17c		*User Spare 2
18a	GND	Ground	18c	BFLT/	*Buffered Bus Float
19a	BDMT/	*Buffered DMA Terminate	19c	BØ0	*Buffered External Phase 0 Clock
20a		*User Spare 3	20c	GND	Ground
21a	BR/$\overline{W}$/	Buffered Read/Write "Not"	21c	BDRQ2/	*Buffered DMA Request 2
22a		*System Spare	22c	BR/$\overline{W}$	*Buffered Read/Write
23a	GND	Ground	23c	BACT/	Buffered Bus Active
24a	BIRQ/	*Buffered Interrupt Request	24c	BNMI/	*Buffered Non-Maskable Interrupt
25a	BØ2/	Buffered Phase 2 "Not" Clock	25c	GND	Ground
26a	BØ2	*Buffered Phase 2 Clock	26c	BRES/	Buffered Reset
27a	BD7/	Buffered Data Bit 7	27c	BD6/	Buffered Data Bit 6
28a	GND	Ground	28c	BD5/	Buffered Data Bit 5
29a	BD4/	Buffered Data Bit 4	29c	BD3/	Buffered Data Bit 3
30a	BD2/	Buffered Data Bit 2	30c	GND	Ground
31a	BD1/	Buffered Data Bit 1	31c	BD0/	Buffered Data Bit 0
32a	+5V	+5 Vdc	32c	GND	Ground

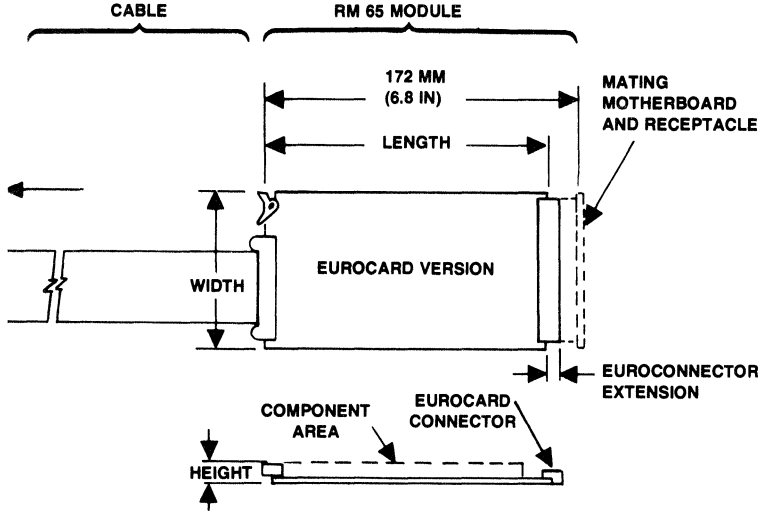
Note:
*Not used on this module

6

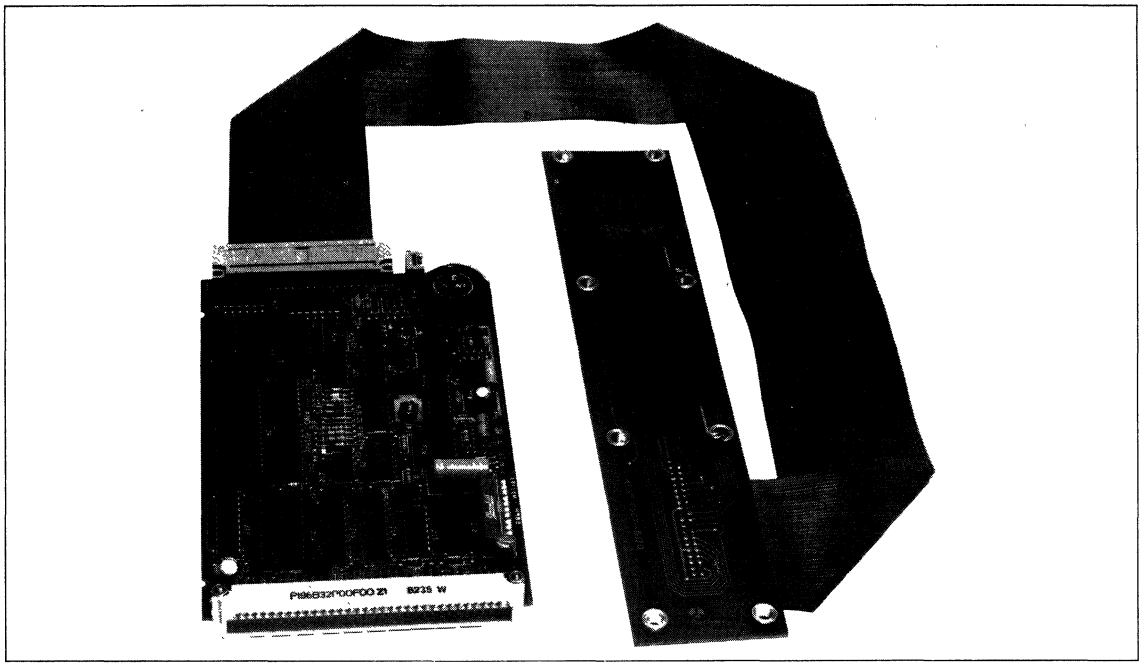
SPECIFICATIONS

Parameter	Value
Dimensions	
PROM Programmer Module	
Width	100 mm (3.94 in.)
Length	167 mm (6.58 in.)
Height(1)	14 mm (0.56 in.)
PROM Programmer Cable	
Length	610 mm (24 in.)
Weight	184 g (6.5 oz.)
Environment	
Operating Temperature	0° to 70°C
Storage Temperature	−40°C to 85°C
Relative Humidity	0% to 85% (without condensation)
Power Requirements	+5V ±5% at 1.1 A typical 2.0 A maximum (average) 2.9 A maximum (peak)
Connectors/Sockets	
RM 65 Bus Connector (P1)	64-pin plug per DIN 41612 (Rows a and b with c not installed)
Socket Module Cable Connector (J1)	40-pin plug (0.100 in. centers) per DIN 41612, mates with 3417-7040 (3M) or equivalent
PROM Sockets	28-pin and 24-pin

Note:
1. Height value includes the maximum values for component height above the board surface (0.4 in.), printed circuit board thickness (0.062 in.), and pin extension through the bottom of the module (0.1 in.).



PROM Programmer Module Outline



RDC-1030 PROM Programmer Module

Rockwell

SPS-200 SOFTWARE PREPARATION SYSTEM (SPS) PERIPHERAL CONNECTOR MODULE

INTRODUCTION

The optional SPS Peripheral Connector Module (PCM) (Part No. SPS-200), which connects directly to the AIM 65 Microcomputer Master Module connector, provides the Software Preparation System (SPS) with a complete set of external I/O interfaces. These I/O interfaces support external printers, serial devices, audio cassettes 20 mA current loop and parallel I/O devices such as the Rockwell RM 65 board family.

The external printer interface routes and buffers (TTL levels) the printer signals to a Centronics compatible 34-pin connector for printer support.

The RS-232 interface operates at the ±5V level. No handshaking signals are provided, but selectable handshake signals have been wired for static levels. Feed throughs are provided to cut and jumper these signals. Data Set/Data Terminal operation is selected using a jumper pair.

The 20 mA current loop interface routes four 20 mA current loop signals from the AIM 65 Master Module connector (J1) to a dedicated Molex connector to provide current loop I/O support.

The audio cassette recorder interface signals are routed to two mini-phone (3.5 mm) jacks for audio cassette support. The remote control lines are controled by reed relays and routed to two sub-mini-phone (2.5 mm) jacks.

The parallel I/O connector interface supports the 40-pin signals routed to the interface by the AIM 65 Master Module User VIA (Z22). The parallel interface connector is compatible with many of the RM 65 modules, e.g., single Board Computer (SBC) and Multi-function Peripheral Interface (MPI), and with the AIM 65/40 Microcomputer connector, e.g., User Parallel I/O, Display Interface and Printer Interface.

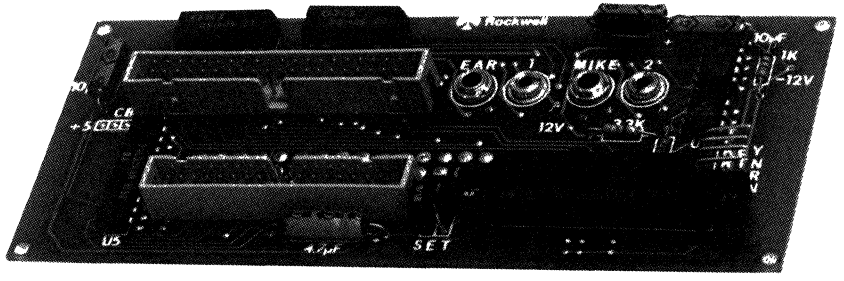
FEATURES

- 34-pin connector for Centronics compatible printer support
- RS-232 connector for serial interface support
- Molex connector for 20 mA current loop support
- 3.5 mm mini-phone jack connectors for audio cassette support
- 2.5 mm sub-mini-phone jack connectors for remote tape control
- 40-pin parallel I/O connector, compatible with the RM 65 module family

REFERENCE DOCUMENTS

The following documents contain information regarding set-up and operation of SPS-200.

Order No.	Title
2167	R6500 Software Preparation System (SPS) User's Manual
209	AIM 65 Microcomputer User's Guide

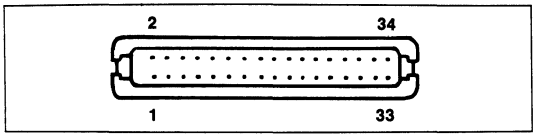


SPS-200 Peripheral Connector Module

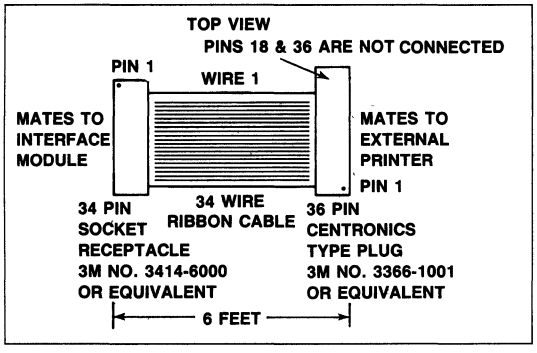
EXTERNAL PRINTER INTERFACE

SPS Module Printer Connector

Pin	Signal	Pin	Signal
1	$\overline{\text{STROBE}}$	13	Data 6
2	Ground	14	Ground
3	Data 1	15	Data 7
4	Ground	16	Ground
5	Data 2	17	Data 8
6	Ground	18	Ground
7	Data 3	19	$\overline{\text{ACK}}$
8	Ground	20	Ground
9	Data 4	21	Not Used
10	Ground	22	Ground
11	Data 5	23 to 34	Not Used
12	Ground		



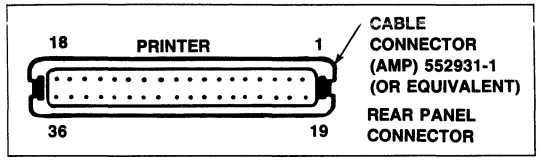
Interface Module Connector



Printer Interface Cable (User Supplied)

Centronics Type Connector Pin Assignment

Pin	Signal	Pin	Signal
J-1	$\overline{\text{STROBE}}$	J-8	Data 7
J-2	Data 1	J-9	Data 8
J-3	Data 2	J-10	$\overline{\text{ACK}}$
J-4	Data 3	J-11 to -17	Not Used
J-5	Data 4	J-19 to -29	Ground
J-6	Data 5	J-30 to -35	Not Used
J-7	Data 6	J-18 and J-36	Not Connected



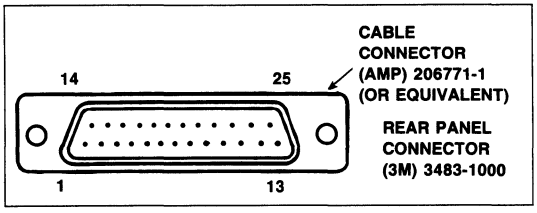
External Printer Connector

RS-232 INTERFACE

RS-232 Connector Pin Assignments

Pin	Signal Mnemonic	Signal Name	Input/Output Data Set	Input/Output Data Term
1	GND	Chassis Ground		
2	$\overline{\text{TD}}$	Transmit Data	I	O
3	$\overline{\text{RD}}$	Receive Data	O	I
5	CTS	Clear to Send[1]	+5V Always	+5V Always
6	DSR	Data Set Ready[1]	+5V Always	+5V Always
7	GND	Signal Ground		
8	DCD	Data Carrier Detected[1]	+5V Always	+5V Always
9-25		Not Used		

[1]This can be cut for a No Connect option

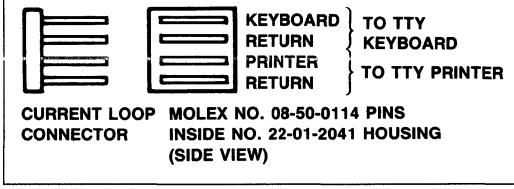


RS-232 Connector Pin Locations

20 mA CURRENT LOOP INTERFACE

20 mA Current Loop Connector Pin Assignments

Pin	Signal Mnemonic	Signal Name
1	TTY KYBD	TTY Keyboard
2	TTY KYBD RETURN (+)	TTY Keyboard Return (+)
3	TTY PTR	TTY Printer
4	TTY PTR RETURN (+)	TTY Printer Return (+)



20 ma Current Loop Connector Pin Locations

6

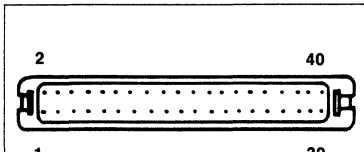
PARALLEL I/O CONNECTOR INTERFACE

Parallel I/O Connector Pin Assignments

Pin	Mnemonic	Signal Name	Input/Output
1*	CB2	Port B, Control No. 2[1]	I/O
2		No Connect	
3*	CB1	Port B, Control No. 1	I/O
5*	PB7	Port B, Bit 7	I/O
7*	PB6	Port B, Bit 6	I/O
9*	PB5	Port B, Bit 5	I/O
11*	PB4	Port B, Bit 4	I/O
13*	PB3	Port B, Bit 3	I/O
15*	PB2	Port B, Bit 2	I/O
17*	PB1	Port B, Bit 1	I/O
19*	PB0	Port B, Bit 0	I/O
21	PA7	Port A, Bit 7	I/O
23	PA6	Port A, Bit 6	I/O
25	PA5	Port A, Bit 5	I/O
27	PA4	Port A, Bit 4	I/O
29	PA3	Port A, Bit 3	I/O
31	PA2	Port A, Bit 2	I/O
33	PA1	Port A, Bit 1	I/O
35	PA0	Port A, Bit 0	I/O
37	CA2	Port A, Control No. 2	I/O
39	CA1	Port A, Control No. 1	I/O
40		No Connect	

Note: Even Numbered pins connected to GND.

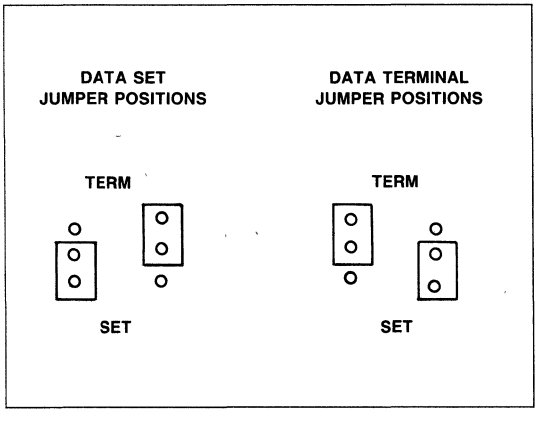
*These signals are used by the Printer Interface.
[1] This can be cut/jumpered to +5V.



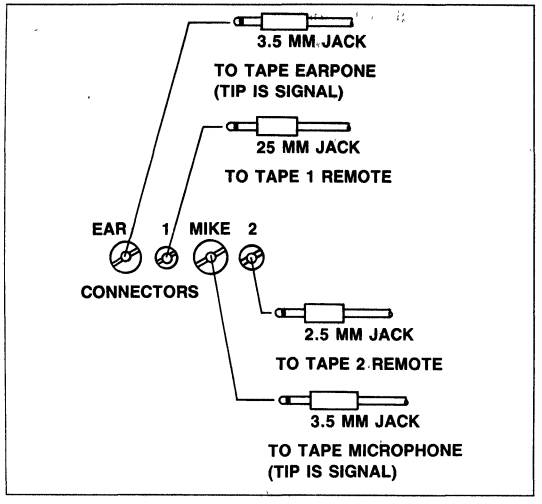
CABLE CONNECTOR: (3M) 3417-6040 (OR EQUIVALENT)
REAR PANEL CONNECTOR: (3M) 3324-0000

Parallel I/O Connector Pin Locations

DATA SET/DATA TERMINAL SETUP



AUDIO CASSETTE RECORDER INTERFACE



Audio Cassette Recorder Interface

WARNING

This equipment generates, uses and can radiate radio frequency energy and if not installed and used in accordance with the instructions manual, may cause interference to radio communications. It has been tested and found to comply with the limits for a Class A computing device pursuant to Subpart J of Part 15 of FCC Rules, which are designed to provide reasonable protection against such interference when operated in a commercial environment. Operation of this equipment in a residential area is likely to cause interference in which case the user at his own expense will be required to take whatever measures may be required to correct the interference.

INFORMATION TO USER: If this equipment does cause interference to radio or television reception which can be determined by turning the equipment on and off, the user is encouraged to try to correct the interference by one or more of the following measures:

- reorient the receiving antenna
- relocate the computer with respect to the receiver
- move the computer with respect to the receiver
- plug the computer into a different outlet so that the computer and receiver are on different circuits

If necessary, the user should consult the dealer or an experienced radio/television technician for additional suggestions. The user may find the following booklet prepared by the Federal Communications Commission helpful:

"How to Identify and Resolve Radio and TV Interference Problems:

This booklet is available from the U.S. Government Printing Office, Washington, D.C. 20402, Stock Number 004-000-0345-4.

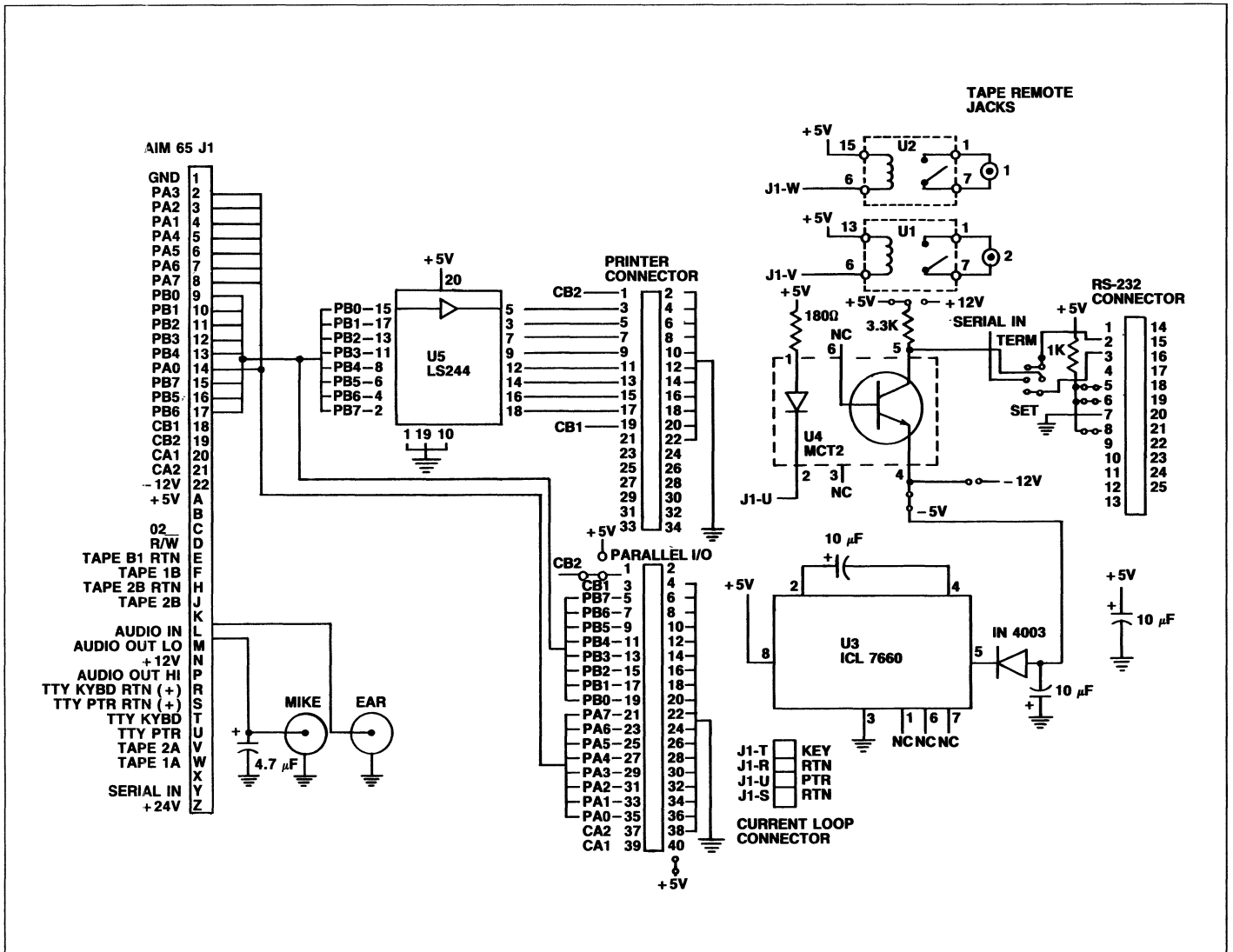


Figure 1. Peripheral Connector Module Schematic

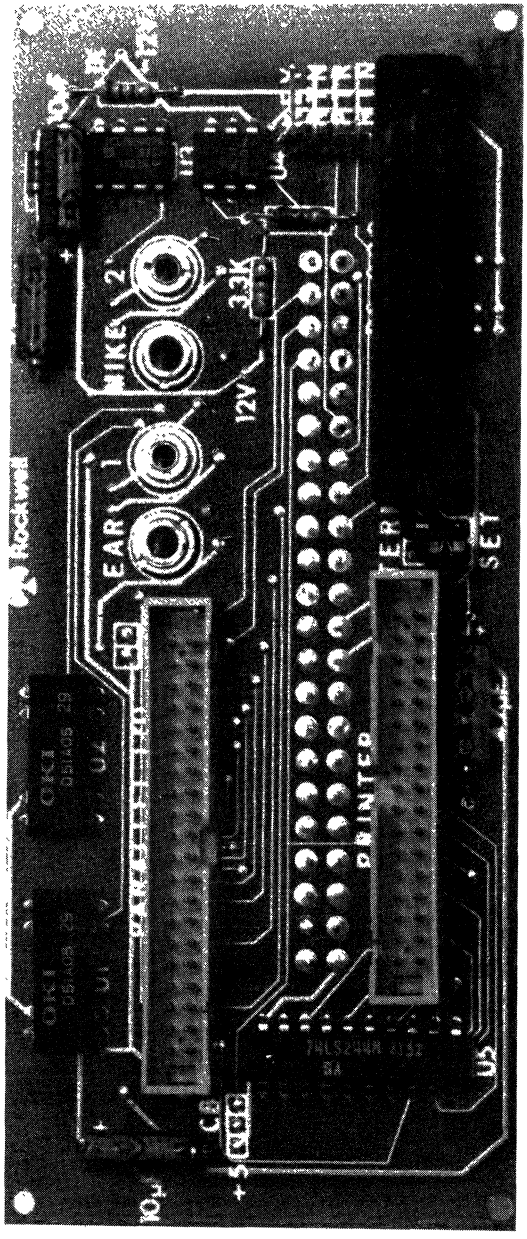


Figure 2. SPS-200 Peripheral Connector Module

INSTALLATION

The PCM connects directly to the AIM 65 Master Module connector J1. The silk screened text on the module should be right-side up when installed as shown in Figure 3.

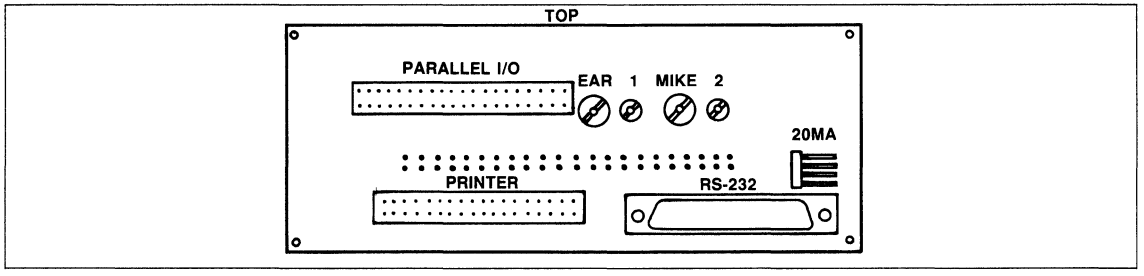


Figure 3. SPS Peripheral Connector Module Orientation

SECTION 7
INTEGRAL MODEMS

INTEGRAL MODEMS
Highest Quality, Performance at the Most Competitive Price

Rockwell International's integral modems offer better performance and greater reliability than any modem products available today. They are the most cost effective and optimal product for computer-communication applications. That is why Rockwell produces more high-speed integral modem subsystems than any other company.

Chances are that if you're using high-speed data communication equipment, a Rockwell subsystem provides the basic modem functions. Practically every sub-minute facsimile machine uses our modems. Rockwell is the leading modem supplier to Japanese Group III facsimile equipment manufacturers.

As for performance, our modems do not lose a bit in a million, even over long distance lines of the public telephone network. Much of this is because of our signal processing capabilities, equalization and diagnostics. With 99.7% of our subsystems accepted by incoming inspection, we have documented an MTBF of 200,000 hours, or about 23 years between service calls.

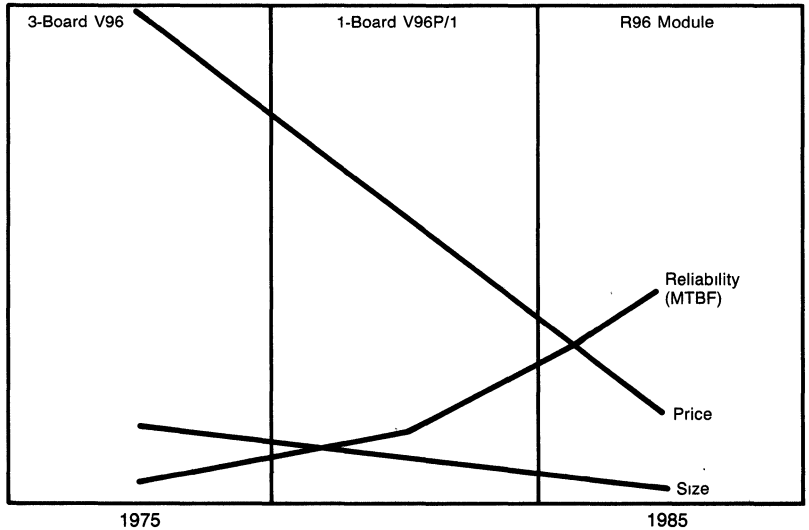
Built-in diagnostics, such as eye pattern and mean squared error, allow thorough modem testing. Several stages of equalization permit accurate transmission over even unconditioned lines. In fact, adaptive equalization, which compensates for phase shifts and frequency delays, was originated in modem technology under a basic patent owned by Rockwell.

Much of modem technology came from Rockwell International. Our first modems date back to vacuum tube versions in 1955. We made the first LSI integral modems in 1969. Using signal processor and integrated analog technology, Rockwell International provides the family of modems which are ideal for those original equipment manufacturers who are in step with the current communication trend. Today, we cover all speeds from 1200 to 9600 bps, with a 14,400 bps model to be announced.

Our newest third-generation LSI family members are designed to be addressed as microcomputer peripherals, thus simplifying design and reducing costs of the host equipment. They are on plug-compatible Eurocard-sized printed circuit boards, so you can switch communication speeds without expensive design changes.

In addition, they are optimized for specific communication products, stand alone modems and statistical multiplexers, facsimile equipment and personal computer or terminal applications.

They are low in price and readily available. Being the largest manufacturer allows us to pass our economical advantages on to our customers. We offer the best cost/performance OEM modems. No one else comes close.



MTBF (Thousand Hours)	50	100	200
ACCEPTANCE (%)	95	99.5	99.7
CARD SIZE (Sq. In.)	112	54	10
PRICE (Current $)	X	1/3 X	1/6 X

Rockwell Integral Modems Lead The Industry

Rockwell

R96FT/SEC
9600 BPS FAST TRAIN MODEM WITH SECONDARY CHANNEL

PRODUCT PREVIEW

PRODUCT PREVIEW

INTRODUCTION

The R96 Fast Train (FT) with 75 bps secondary channel is a synchronous, serial 9600/7200/4800/2400 bps modem suitable for operation over dedicated unconditioned lines. It satisfies the telecommunications requirements specified in CCITT Recommendations V.29 and V.27 bis/ter.

The R96FT/SEC is specifically optimized for use in a multipoint environment requiring a fast training sequence of 22 msec at 9600 bps and 21 msec at 4800 bps. The 75 bps secondary channel, small size (100 mm by 160 mm), and low power consumption (4 watts typical) offer the user flexibility in creating a 9600 bps modem customized for specific packaging and functional requirements.

Data can be transferred to and from the modem either serially over the CCITT V.24 interface or in parallel over the microprocessor bus interface.

The R96FT/SEC is a member of Rockwell's family of plug compatible 9600/4800 bps modems.

Product availability is **APRIL, 1985.**

FEATURES

- Configurations
  —CCITT V.29, V.27 bis/ter
- Fast Training Sequence 22 msec/9600 bps, 21 msec/4800 bps
- Ideal for Multipoint Applications
- Plug Compatible with Rockwell R96DP, R48DP Modems
- Secondary Channel, 75 bps
- Dynamic Range: −43 dBm to 0 dBm
- Equalization
  —Automatic Adaptive
  —Compromise Cable (Selectable)
- DTE Interface: Two Alternate Ports
  —Microprocessor Bus
  —CCITT V.24 (RS-232-C Compatible)
- Diagnostics
  —Provides Telephone Line Quality Monitoring Statistics
- Programmable Transmit Output Level
- Loopbacks
  —Local Analog
  —Remote Analog (Locally Activated)
  —Remote Digital (Locally Activated)
- Small Size—100 mm × 160 mm (3.64″ × 6.30″)
- Power Consumption—4 Watts typical
- TTL and CMOS Compatible

7

Rockwell

R144 SYNCHRONOUS 14.4 KBPS MODEM

PRODUCT PREVIEW

PRODUCT PREVIEW

INTRODUCTION

The Rockwell R144 is a synchronous 14.4 Kbps high performance modem capable of operation over either conditioned or unconditioned lines. This single board modem is designed to satisfy telecommunciation requirements specified in the CCITT Recommendation V.29. The modem is usable in 4-wire full duplex operation and is plug compatible with Rockwell R96 series modems. The R144 is designed for use in multipoint networks.

FEATURES

- 14,400/9600/7200/4800 bps Modes
- V.29 Compatible
- Single Printed Circuit Board— 103 mm × 160 mm
- TTL Compatible
- Full-Duplex (4-Wire)
- Maximum Digital LSI Signal Processing
- Automatic Adaptive Equalizer
- V.54 Loops 2, 3, 4 Diagnostics
- 0 to −45 dBm Dynamic AGC Range
- Power Consumption—5 Watts typical
- Network Control Diagnostics
- 50 msec Training Time at 14.4 Kbps
- 22 msec Training Time at 9.6 Kbps
- Operates Over Unconditioned Lines

SPECIFICATIONS

POWER REQUIREMENTS

Voltages: ±5V (±5%)
+12V (±5%)

ENVIRONMENTAL

Operating temperature: −0°C to +60°C
Humidity: Up to 90%, noncondensing, or a wet bulb temperature up to 35°C, whichever is less.

Rockwell

R4875
4800/75 BPS MODEM

PRODUCT PREVIEW

PRODUCT PREVIEW

INTRODUCTION

The R4875 is a synchronous/asynchronous, serial 4800/75 bps modem suitable for operation over the general switched network. It satisfies the telecommunications requirements specified in CCITT Recommendation V.27 ter. The 75 bps backward channel satisfies CCITT Recommendation V.23.

The R4875 is specifically optimized for use in switched network environments involving videotex transmission.

Data can be transferred to and from the modem serially over the CCITT V.24 interface.

FEATURES

- CCITT V.27 ter-4800 bps forward channel
- CCITT V.23-75 bps backward channel
- Full duplex, 2-wire
- Videotex transmission per Nippon Telephone + Telegraph Captain System and British Telecom Picture Prestel Requirements
- Dynamic Range 0–40 dBm
- Equalization
  —Automatic adaptive
  —Compromise Cable
  —Compromise link amplitude
- Interface: Two alternate ports
  —Microprocessor bus
  —RS-232/CCITT V.24
- Connector: 26-Pin DIN
- TTL and CMOS compatible

SPECIFICATIONS

BOARD DIMENSIONS

Width = 160 mm
Length = 223 mm
Height = 24 mm

POWER REQUIREMENTS

Voltages: +5 Vdc (+5%)
±12 Vdc (+5%)
Consumption: 7 Watts typical

ENVIRONMENTAL

Operating Temperature 0°–60°C
Humidity: up to 90° noncondensing, or a wet bulb temperature up to 35°C, whichever is less

7

Rockwell

R208A/B
4800 BPS MODEM

PRODUCT PREVIEW

PRODUCT PREVIEW

INTRODUCTION

The R208A/B is a synchronous, serial, 4800/2400 bps modem designed for operation over dedicated unconditioned lines or with the general switched telephone network with appropriate line terminations, such as a Data Access Arrangement or transformer, provided externally.

The R208A/B satisfied the telecommunications requirements specified in Bell 208 A/B and CCITT V.27 bis/ter for 4800 bps modems.

The R208A/B is optimized for point-to-point applications and suitable for network applications where the optimum in data transfer is needed. Its small size (100 mm by 120 mm) and low power consumption (4W typical) offer the user flexibility in creating a 4800 bps modem customized for specific packaging and functional requirements.

Data can be transferred to and from the modem either serially over the CCITT V.24 interface or in parallel over the microprocessor bus interface.

The R208A/B is a member of Rockwell's family of plug compatible modems.

Product availability is **APRIL, 1985.**

FEATURES

- Configurations
  —Bell 208 A/B
  —CCITT V.27 bis/ter
- Half-Duplex (2-wire), Full-Duplex (4-wire)
- Ideal for Point-to-Point Applications
- Plug Compatible with Rockwell R96DP, R48DP, R96FT Modems
- Programmable Tone Generation
- Dynamic Range: −43 dBm to 0 dBm
- Equalization
- —Automatic Adaptive
  —Compromise Cable (Selectable)
  —Compromise Link (Selectable)
- DTE Interface: Two Alternate Ports
  —Microprocessor Bus
  —CCITT V.24 (RS-232-C Compatible)
- Diagnostics
  —Provides Telephone Line Quality Monitoring Statistics
- Programmable Transmit Output Level
- Loopbacks
  —Local Analog
  —Remote Analog
  —Remote Digital
- Power Consumption—4 Watts Typical
- TTL and CMOS Compatible

SPECIFICATIONS

POWER REQUIREMENTS

+5 Vdc ±5% <500ma
+12 Vdc ±5% <20ma
−12 Vdc ±5% <80ma

ENVIRONMENTAL

Temperature: Operating 0 to 60°C
Storage −40 to 90°C
Relative Humidity: Up to 90%, noncondensing, or a wet bulb temperature up to 35°C, whichever is less.

Rockwell

R96FAX
9600 BPS FACSIMILE MODEM

INTRODUCTION

The Rockwell R96FAX is a synchronous serial 9600 bps modem designed for operation over either dedicated unconditioned lines or over the general switched telephone network.

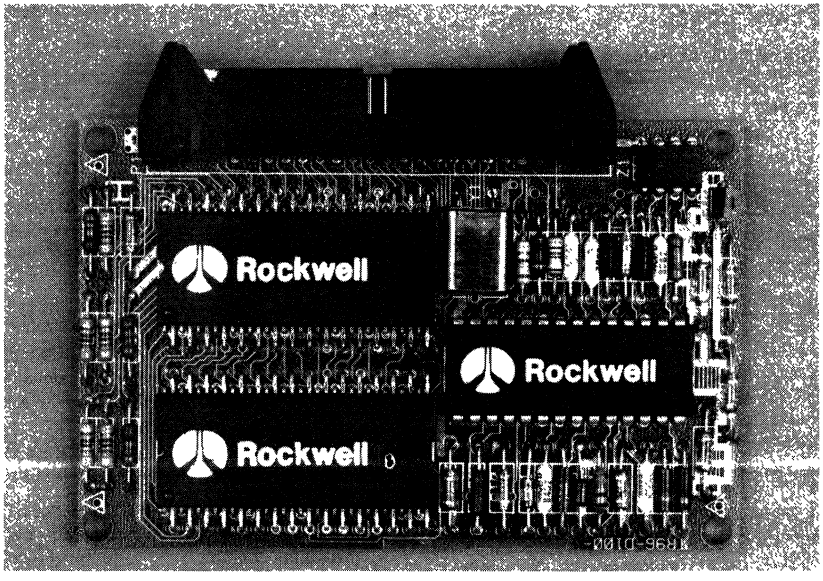
The modem satisfies telecommunications requirements specified in CCITT Recommendations V.29 and V.27 ter, and of Recommendations T.30, T.4 and T.3.

The R96FAX is specifically optimized for use in Group III Facsimile machines with the added capability of Group II compatibility. The small size and low power consumption of the modem offer the user flexibility in creating a 9600 bps modem design customized for specific packaging and functional requirements.

The modem is capable of operating at 9600, 7200, 4800, 2400, and 300 bps.

FEATURES

- Ultimate User Compatibility:
  — CCITT V.29, V.27 ter, T.30, V.21 Channel 2, T.4, T.3
- Group III and Group II Facsimile
- Half-Duplex (2-Wire)
- Tone Detection
- Programmable Tone Generation and Detection
- Dynamic Range –47 dBm to 0 dBm
- Diagnostic Capability
- Equalization:
  — Automatic Adaptive
  — Compromise Cable (Selectable)
  — Compromise Link Amplitude (Selectable)
- DTE Interface:
  — Microprocessor Bus
  — CCITT V.24 (RS-232-C Compatible)
- Small Size — 100 mm x 65 mm (3.94 x 2.56 inches)
- Low Power Consumption (2 watts, Typical)
- Transmit Output Level (+5 dBm ±1 dB)
- TTL and CMOS Compatible



R96FAX Modem

7

TECHNICAL SPECIFICATIONS

TRANSMITTER TONAL SIGNALING AND CARRIER FREQUENCIES

T. 30 Tonal Signaling Frequencies

Function	Frequency (Hz ±0.01 Hz)
Calling Tone (CNG)	1100
Answer Tone (CED)	2100
Group II Identification (C12)	1850
Group II Command (GC2)	2100
Group II Confirmation (CFR2, MCF2)	1650
Line Conditioning Signal (LCS)	1100
End of Message (EOM)	1100
Procedure Interrupt (PIS)	462

Carrier Frequencies

Function	Frequency (Hz ±0.01 Hz)
T.3 Carrier (Group II)	2100
V.27 ter Carrier	1800
V.29 Carrier	1700

TONE GENERATION

Under control of the host processor, the R96FAX can generate voice band tones up to 4800 Hz with a resolution of 0.15 Hz and an accuracy of 0.01%. Tones over 3000 Hz are attenuated.

TONE DETECTION

In the 300 bps FSK receive configuration, the presence of tones at preset frequencies is indicated by bits in the interface memory of the R96FAX.

SIGNALING AND DATA RATES

Signaling/Data Rates

Parameter	Specification (± 0.01%)
Signaling Rate: Data Rate:	2400 Baud 9600 bps, 7200 bps, 4800 bps
Signaling Rate: Date Rate:	1600 Baud 4800 bps
Signaling Rate: Data Rate:	1200 Baud 2400 bps

DATA ENCODING

At 2400 baud, the data stream is encoded per CCITT V.29. At 9600 bps, the data stream is divided in groups of four-bits (quadbits) forming a 16-point structure. At 7200 bps, the data stream is divided into three bits (tribits) forming an 8-point structure. At 4800 bps, the data stream is divided into two bits (dibits) forming a 4-point structure.

At 1600 baud, the 4800 bps data stream is encoded into tribits per CCITT V.27 ter.

At 1200 baud, the 2400 bps data stream is encoded into dibits per CCITT V.27 ter.

EQUALIZERS

The R96FAX provides the following equalization functions which can be used to improve performance when operating over poor lines:

Cable Equalizers — Selectable compromise cable equalizers are provided to optimize performance over different lengths of non-loaded cable of 0.4 mm diameter.

Link Amplitude Equalizer — The selectable compromise amplitude equalizer may be inserted into the transmit and/or receive paths under control of the transmit amplitude equalizer enable and the receive amplitude equalizer enable bits in the interface memory. The amplitude select bit controls which of two amplitude equalizers is selected.

Automatic Adaptive Equalizer — An automatic adaptive equalizer is provided in the receiver circuit for V.27 and V.29 configurations. The equalizer can be configured as either a T or a T/2 equalizer.

TRANSMITTED DATA SPECTRUM

If neither the link amplitude nor cable equalizer is enabled, the transmitter spectrum is shaped by the following raised cosine filter functions:

1. *1200 Baud.* Square root of 90 percent
2. *1600 Baud.* Square root of 50 percent
3. *2400 Baud.* Square root of 20 percent

The out-of-band transmitter power limitations meet those specified by Part 68 of the FCC's Rules, and typically exceed the requirements of foreign telephone regulatory bodies.

SCRAMBLER/DESCRAMBLER

The R96FAX incorporates a self-synchronizing scrambler/descrambler. This facility is in accordance with either V.27 ter or V.29 depending on the selected configuration.

RECEIVED SIGNAL FREQUENCY TOLERANCE

The receiver circuit of the R96FAX can adapt to received frequency error of up to ±10 Hz with less than a 0.2 dB degradation in BER performance. Group II carrier recovery capture range is 2100 ±30 Hz.

RECEIVE LEVEL

The receiver circuit of the R96FAX satisfies all specified performance requirements for received line signal levels from 0 dBm to −43 dBm. The received line signal level is measured at the receiver analog input (RXA).

RECEIVE TIMING

In the receive state, the R96FAX provides a Data Clock (DCLK) output in the form of a square wave. The low to high transitions of this output coincide with the center of received data bits. The timing recovery circuit is capable of tracking a ±0.01% frequency error in the associated transmit timing source.

TRANSMIT LEVEL

The transmitter output level is fixed at +5 dBm ±1 dB. When driving a 600 ohm load the TXA output requires a 600 ohm series resistor to provide −1 dBm ±1 dB to the load.

TRANSMIT TIMING

In the transmit state, the R96FAX provides a Data Clock (DCLK) output with the following characteristics:

1. *Frequency.* Selected data rate of 9600, 7200, 4800, 2400, or 300 Hz (±0.01%). In Group II, DCLK tracks an external 10368 Hz clock.
2. *Duty Cycle.* 50 ±1%

Transmit Data (TXD) must be stable during the 1 microsecond periods immediately preceding and following the rising edge of DCLK.

TURN-ON SEQUENCE

A total of ten selectable turn-on sequences can be generated by the R96FAX, as defined in the following table:

Turn-On Sequences

No.	v.29	V.27 ter	RTS-CTS Time (ms)	Comments
1	9600 bps		253	
2	7200 bps		253	
3	4800 bps		253	
4		4800 bps[2]	708	
5		2400 bps[2]	943	
6	9600 bps		458	Preceded
7	7200 bps		458	By Echo
8	4800 bps		458	Suppressor
9		4800 bps[2]	913	
10		2400 bps[2]	1148	Tone

Notes:

1. Turn-on sequences six through ten are used on lines with protection against talker echo.
2. V.27 ter long training sequence only.

TURN-OFF SEQUENCE

For V.27 ter, the turn-off sequence consists of approximately 10 ms of remaining data and scrambled ones at 1200 baud or approximately 7 ms of data and scrambled ones at 1600 baud followed by a 20 ms period of no transmitted energy. For V.29, the turn-off sequence consists of approximately 5 ms of remaining data and scrambled 1's followed by a 20 ms period of no transmitted energy.

CLAMPING

The following clamps are provided with the R96FAX:

1. *Received Data (RXD).* RXD is clamped to a constant mark (1) whenever RLSD is off.
2. *Received Line Signal Detector (RLSD).* RLSD is clamped off (squelched) during the time when RTS is on.
3. *Extended Squelch.* Optionally, RLSD remains clamped off for 130 ms after the turn-off sequence.

RESPONSE TIMES OF CLEAR-TO-SEND (CTS)

The time between the off-to-on transition of RTS and the off-to-on transition of CTS is dictated by the length of the training sequence. Response time is 253 ms for V.29, 708 ms for V.27 ter at 4800 bps, and 943 ms for V.27 ter at 2400 bps.

The time between the on-to-off transition of RTS and the on-to-off transition of CTS in the data state is a maximum of 2 baud times for all configurations.

RECEIVED LINE SIGNAL DETECTOR (RLSD)

For either V.27 ter or V.29, RLSD turns on at the end of the training sequence. If training is not detected at the receiver, the RLSD off-to-on response time is 15 ±10 ms. The RLSD on-to-off response time for V.27 is 10 ±5 ms and for V.29 is 30 ±9 ms. Response times are measured with a signal at least 3 dB above the actual RLSD on threshold or at least 5 dB below the actual RLSD off threshold.

The RLSD on-to-off response time ensures that all valid data bits have appeared on RXD.

Two threshold options are provided:

1. Greater than −43 dBm (RLSD on)
   Less than −48 dBm (RLSD off)
2. Greater than −47 dBm (RLSD on)
   Less than −52 dBm (RLSD off)

NOTE

Performance may be at a reduced level when the received signal is less than −43 dBm.

A minimum hysteresis action of 2 dB exists between the actual off-to-on and on-to-off transition levels. The threshold levels and hysteresis action are measured with a modulated carrier signal applied to the receiver's audio input (RXA).

MODES OF OPERATION

The R96FAX is capable of being operated in either a serial or a parallel mode of operation.

SERIAL MODE

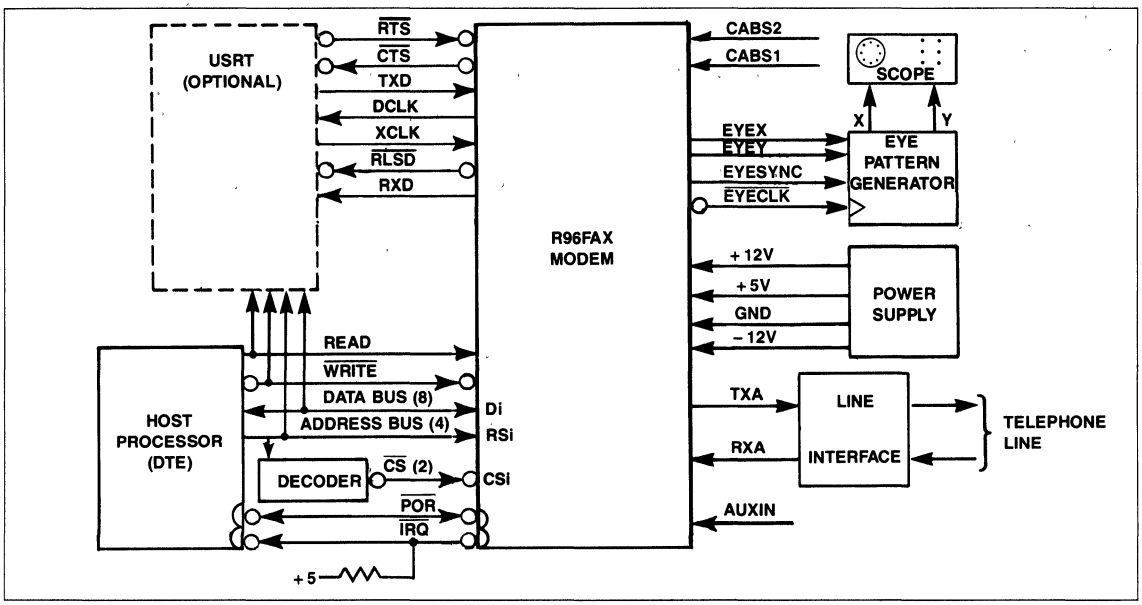
The serial mode uses standard V.24 (RS-232-C compatible) signals to transfer channel data. An optional USRT device (shown in the R96FAX Functional Interconnect Diagram) illustrates this capability.

PARALLEL MODE

The R96FAX has the capability of transferring channel data eight bits at a time via the microprocessor bus.

MODE SELECTION

Selection of either the serial or parallel mode of operation is by means of a control bit. To enable the parallel mode, the control bit must be set to a 1. The modem automatically defaults to the serial mode at power-on. In either mode the R96FAX is configured by the host processor via the microprocessor bus.



R96FAX Functional Interconnect Diagram

INTERFACE CRITERIA

The modem interface comprises both hardware and software circuits. Hardware circuits are assigned to specific pins in a 40-pin ribbon connector. Software circuits are assigned to specific bits in a 32-byte interface memory.

HARDWARE CIRCUITS

Signal names and descriptions of the hardware circuits, including the microprocessor interface, are listed in the R96FAX Hardware Circuits table; the table column titled 'Type' refers to designations found in the Hardware Circuit Characteristics. The microprocessor interface is designed to be directly compatible with an 8080 microprocessor. With the addition of a few external logic gates, it can be made compatible with 6500, 6800, or 68000 microprocessors.

R96FAX Hardware Circuits

Name	Type	Pin No.	Description
A. OVERHEAD:			
Ground	GND	14, 39	Power Supply Return
+5 volts	PWR	3, 4	+5 volt supply
+12 volts	PWR	26	+12 volt supply
–12 volts	PWR	37	–12 volt supply
$\overline{POR}$	I/OA	36	Power-on-reset

R96FAX Hardware Circuits (Cont.)

Name	Type	Pin No.	Description
B. MICROPROCESSOR INTERFACE:			
D7	I/OA	7	
D6	I/OA	5	
D5	I/OA	9	
D4	I/OA	31	Data Bus (8 Bits)
D3	I/OA	15	
D2	I/OA	28	
D1	I/OA	23	
D0	I/OA	29	
RS3	IA	30	
RS2	IA	8	Register Select (4 Bits)
RS1	IA	27	Select Reg. 0 – F
RS0	IA	10	
$\overline{CSO}$	IA	6	Chip Select Sample Rate Device
$\overline{CS1}$	IA	18	Chip Select Baud Rate Device
$\overline{READ}$	IA	1	Read Enable
$\overline{WRITE}$	IA	2	Write Enable
$\overline{IRQ}$	OB	32	Interrupt Request
C. V.24 INTERFACE:			
$\overline{DCLK}$	OC	13	Data Clock
$\overline{XCLK}$	IB	22	External Clock for Group II
$\overline{RTS}$	IB	19	Request-to-Send
$\overline{CTS}$	OC	17	Clear-to-Send
TXD	IB	20	Transmitter Data
$\overline{RXD}$	OC	21	Receiver Data
$\overline{RLSD}$	OC	16	Received Line Signal Detector
D. CABLE EQUALIZER:			
CABS1	IC	33	Cable Select 1
CABS2	IC	34	Cable Select 2

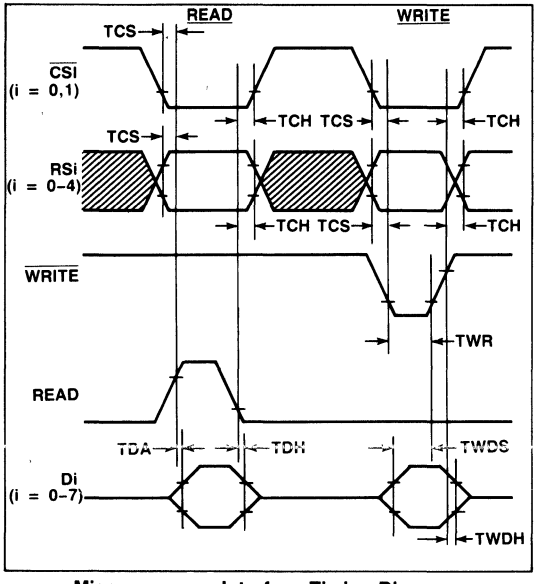
R96FAX Hardware Circuits (Cont.)

Name	Type	Pin No.	Description
E. ANALOG SIGNALS:			
TXA	AA	38	Transmitter Analog Output
RXA	AB	40	Receiver Analog Input
AUXIN	AC	35	Auxiliary Analog Input
F. DIAGNOSTIC:			
EYEX	OC	24	Eye Pattern Data — X Axis
EYEY	OC	25	Eye Pattern Data — Y Axis
$\overline{\text{EYECLK}}$	OA	11	Eye Pattern Clock
EYESYNC	OA	12	Eye Pattern Synchronizing Signal

Eye Pattern Generation

The four hardware diagnostic circuits, identified in the preceding table, allow the user to generate and display an eye pattern. Circuits EYEX and EYEY serially present eye pattern data for the horizontal and vertical display inputs respectively. The 8-bit data words obtained from registers 1:3 and 1:1 (see RAM Data Access) are shifted out most significant bit first clocked by the rising edge of the $\overline{\text{EYECLK}}$ output. The EYESYNC output is provided for word synchronization. The falling edge of EYESYNC may be used to transfer the 8-bit word from the shift register to a holding register. Digital to analog conversion can then be performed for driving the X and Y inputs of an oscilloscope.

MICROPROCESSOR TIMING



Microprocessor Interface Timing Diagram

Critical Timing Requirements

Characteristic	Symbol	Min	Max	Units
$\overline{\text{CSi}}$, RSi setup time prior to Read or $\overline{\text{Write}}$	TCS	30	—	NS
Data Access time after Read	TDA	—	140	NS
Data hold time after Read	TDH	10	50	NS
CSi, RSi hold time after Read or $\overline{\text{Write}}$	TCH	10	—	NS
Write data setup time	TWDS	75	—	NS
Write data hold time	TWDH	10	—	NS
Write strobe pulse width	TWR	75	—	NS

Cable Equalizer Selection

Cable Equalizer Selection

CABS 2	CABS 1	Length of 0.4mm Diameter Cable
0	0	0.0
0	1	1.8 km
1	0	3.6 km
1	1	7.2 km

HARDWARE CIRCUIT CHARACTERISTICS

Digital Interface Characteristics

The digital interface characteristics are listed in the table on the following page.

Analog Interface Characteristics

Analog Interface Characteristics

Name	Type	Characteristics
TXA	AA	The transmitter output is a low impedance operational amplifier output. In order to match to 600 ohms, an external 604 ohm series resistor is required.
RXA	AB	The receiver input impedance is 63.4K ohms ±5%.
AUXIN	AC	The auxiliary analog input allows access to the transmitter for the purpose of interfacing with user provided equipment. Because this is a sampled data input, any signal above 4800 Hz will cause aliasing errors. The input impedance is 1K ohms, and the gain to transmitter output is −1 dB ±1 dB.

SOFTWARE CIRCUITS

The R96FAX comprises two signal processor chips. Each of these chips contains 16 registers to which an external (host) microprocessor has access. Although these registers are within the modem, they may be addressed as part of the host processor's memory space. The host may read data out of or write data into these registers. The registers are referred to as interface memory. Register in chip 0 update at the modem sample rate (9600 bps). Registers in chip 1 update at the selected baud rate.

Digital Interface Characteristics

Symbol	Parameter	Units	Input/Output Type							
			IA	IB	IC	OA	OB	OC	I/O A	I/O B
V_{IN}	Input Voltage, High	V	2.0 min.	2.0 min.	2.0 min				2.0 min.	5.25 max. 2.0 min.
V_{IL}	Input Voltage, Low	V	0.8 max.	0.8 max.	0.8 max.				0.8 max.	0.8 max.
V_{OH}	Output Voltage, High	V				2.4 min.[1]			2.4 min. [1]	2.4 min.[3]
V_{OL}	Output Voltage, Low	V				0.4 max.[2]	0.4 max.[2]	0.4 max.[2]	0.4 max.[2]	0.4 max.[2]
I_{IN}	Input Current, Leakage	μA	±2.5 max.						±12.5 max.[4]	
I_{OH}	Output Current, High	mA				−0.1 max.				
I_{OL}	Output Current, Low	mA				1.6 max.	1.6 max.	1.6 max.		
I_L	Output Current, Leakage	μA					±10 max.			
I_{PU}	Pull-up Current (Short Circuit)	μA		−240 max. −10 min.	−240 max. −10 min.			−240 max. −10 min.		−260 max. −100 min.
C_L	Capacitive Load	pF	5	5	20				10	40
C_D	Capacitive Drive	pF				100	100	100	100	100
	Circuit Type		TTL	TTL w/Pull-up	TTL w/Pull-up	TTL	Open-Drain	Open Drain w/Pull-up	3 State Transceiver	Open-Drain w/Pull-up

Notes
1. I load = −100 μA
2. I load = 1.6 mA
3. I load = −40 μA
4. V_{IN} = 0.4 to 2.4 Vdc, V_{CC} = 5.25 Vdc

When information in these registers is being discussed, the format Y:Z:Q is used. The chip is specified by Y(0 or 1), the register by Z(0-F), and the bit by Q(0-7, 0 = LSB). A bit is considered to be "on" when set to a 1.

Status/Control Bits

The operation of the R96FAX is affected by a number of software control inputs. These inputs are written into registers within the interface memory via the host microprocessor bus. Bits designated by an 'X' are "Don't Care" inputs that can be set to either 1 or 0. Modem operation is monitored by various software flags that are read from interface memory via the host microprocessor bus. All status and control bits are defined in the Interface Memory table. Bits designated by an 'R' are reserved for modem use only and must not be changed by the host.

Ram Data Access

The R96FAX provides the user with access to much of the data stored in the modem's memories. This data is a useful tool in performing certain diagnostic functions.

Two RAM access registers are provided in the interface memory to allow user access to various RAM locations within the modem. The access code stored in 0:F selects the source of data for the RAM data registers in chip 0 (0:0 through 0:3). Similarly, the access code stored in 1:F selects the source of data for registers 1:0 through 1:3. Reading is performed by storing the desired access code in register 0:F (or 1:F), performing a read of 0:0 (or 1:0) to reset 0:E:0 (or 1:E:0), then waiting for 0:E:0 (or 1:E:0) to return to a one. The data may now be read from 0:3 through 0:0 (or 1:3–1:0).

Data in registers 1:3 and 1:1 are presented serially on EYEX and EYEY, respectively.

RAM Access Codes

The RAM access codes defined in the following table allow the host processor to read diagnostic information within the modem.

RAM Access Codes

No.	Function	Access	Chip	Reg. No.
1.	Received Signal Samples	40	0	2,3
2.	Demodulator Output	42	0	0,1,2,3
3.	Low Pass Filter Output	54	0	0,1,2,3
4.	Average Energy	5C	0	2,3
5.	AGC Gain Word	01	0	2,3
6.	Equalizer Input	40	1	0,1,2,3
7.	Equalizer Tap Coefficients	01-20	1	0,1,2,3
8.	Unrotated Equalizer Output	61	1	0,1,2,3
9.	Rotated Equalizer Output (Received Point—Eye Pattern)	22	1	0,1,2,3
10.	Decision Points (Ideal)	62	1	0,1,2,3
11.	Error Vector	63	1	0,1,2,3
12.	Rotation Angle	00	1	0,1
13.	Frequency Correction	28	1	2,3
14.	EQM	2B	1	2,3
15.	Group II Base Band Signal	48	1	2,3
16.	G2 AGC Gain Word	2D	1	2,3

R96FAX Interface Memory Chip 0 ($\overline{CS0}$)

Register \ Bit	7	6	5	4	3	2	1	0
F	PDM	RAM ACCESS S						
E	IA0	R	R	R	SETUP	IE0	R	DA0
D	R	R	R	R	R	R	R	R
C	R	R	R	R	R	R	R	R
B	R	R	R	R	R	R	R	R
A	R	R	R	R	R	R	R	R
9	R	R	R	R	R	R	R	R
8	R	R	R	R	R	R	R	R
7	R	R	R	R	R	R	R	R
6	R	R	R	R	R	R	R	R
5	RTS	TDIS	X	X	EPT	SQEXT	T2	LRTH
4	CONFIGURATION							
3	RAM DATA XSM; FREQM							
2	RAM DATA XSL; FREQL							
1	RAM DATA YSM							
0	RAM DATA YSL; TRANSCEIVER DATA							
Register / Bit	7	6	5	4	3	2	1	0

X = User available (not used by modem).
R = Reserved (modem use only).

R96FAX Interface Memory Chip 1 ($\overline{CS1}$)

Register \ Bit	7	6	5	4	3	2	1	0
F	RAM ACCESS B							
E	IA1	R	R	R	R	IE1	R	DA1
D	X	TLE	RLE	J3L	X	X	X	R
C	X	X	X	X	X	X	X	G2FGC
B	F3	F2	F1	R	R	R	R	R
A	R	R	R	R	R	R	R	R
9	R	R	R	R	R	R	R	R
8	R	R	R	R	R	R	R	R
7	R	$\overline{PNDET}$	R	R	R	R	R	$\overline{CDET}$
6	R	R	R	R	R	R	R	R
5	R	$\overline{FED}$	R	R	R	R	R	R
4	R	R	R	R	R	$\overline{P2DET}$	R	R
3	RAM DATA XBM							
2	RAM DATA XBL							
1	RAM DATA YBM							
0	RAM DATA YBL							
Register / Bit	7	6	5	4	3	2	1	0

X = User available (not used by modem).
R = Reserved (modem use only).

7

R96FAX Interface Memory Definitions

Mnemonic	Name	Memory Location	Description
$\overline{\text{CDET}}$	Carrier Detector	1:7:0	The zero state of $\overline{\text{CDET}}$ indicates passband energy is being detected, and a training sequence is not present. $\overline{\text{CDET}}$ goes to zero at the start of the data state, and returns to one at the end of the received signal.
(None)	Configuration	0:4:0–7	The host processor configures the R96FAX by writing a control code into the configuration register in the interface memory space. ***Configuration Control Codes*** Control codes for the five available R96FAX configurations are: **Configuration** — **Configuration Code (HEX)** V.29 9600 — 14 V.29 7200 — 12 V.29 4800 — 11 V.27 4800 — 0A V 27 2400 — 09 FSK — 20 Group II — 40 Tone Transmit — 80 ***Configuration Definitions*** Definitions for the five available R96FAX configurations are: 1. *V.29.* When any of the V.29 configurations has been selected, the modem operates as specified in CCITT recommendation V.29. 2. *V.27.* When any of the V.27 configurations has been selected, the modem operates as specified in CCITT recommendation V.27 ter. 3. *FSK.* The modem operates as a CCITT T30 compatible 300 bps FSK modem having characteristics of the CCITT V.21 channel 2 modulation system 4. *Group II.* The modem operates as a CCITT T.3 compatible AM modem. This permits transmission to and reception from Group II facsimile apparatus. A carrier frequency of 2100 Hz is used. A black signal is transmitted as no carrier. The phase of the carrier representing white is reversed after each transition through black. When in the receive state, the R96FAX recovers the carrier of the remote transmitting modem to perform a coherent demodulation of the incoming signal. This allows a baseband of 3400 Hz to be recovered. The recovered baseband signal is available on the microprocessor bus. The baseband signal is converted to black or white by comparing the received signal level with a preset threshold number. This number may be changed by the user. Receiver data is presented to the RXD output at a rate of 10368 samples per second. The user should strobe the data on the rising edge of the data clock (DCLK). A logical 1 level (high voltage) represents white. A logical 0 level (low voltage) represents black. 5. *Tone Transmit.* In this configuration, activating signal RTS causes the modem to transmit a tone at a single frequency specified by the user. Two registers in the host interface memory space contain the frequency code. The most significant bits are specified in the FREQM register (0:3). The least significant bits are specified in the FREQL register (0:2). The least significant bit represents 0.146486 Hz ± 0.01%. The frequency generated is: f = 0.146486 (256 FREQM + FREQL) Hz ± 0.01%.
DA0	Data Available (Zero)	0:E:0	DA0 goes to one when the modem writes data into register 0:0. DA0 goes to zero when the host processor reads data from register 0:0. DA0 is used for parallel mode as well as for diagnostic data retrieval.
DA1	Data Available (One)	1:E:0	DA1 goes to one when the modem reads or writes register 1:0. DA1 goes to zero when the host processor reads data from, or writes data into, register 1:0.

R96FAX Interface Memory Definitions (continued)

Mnemonic	Name	Memory Location	Description
EPT	Echo Protector Tone	0:5:3	If EPT is a one, an unmodulated carrier is transmitted for 185 to 200 ms followed by 20 to 25 ms of no transmitted energy at the beginning of the training sequence. This option is available in both the V.27 and V.29 configurations, although it is not specified in the CCITT V.29 recommendation.
$\overline{FED}$	Fast Energy Detector	0:5:6	The zero state of $\overline{FED}$ indicates energy is present above the receiver threshold in the passband. $\overline{FED}$ is not used for Group II Facsimile.
(None)	FREQL/FREQM	0:2 0-7, 0:3:0-7	The host processor conveys tone generation data to the transmitter by writing a 16-bit data word to the FREQL and FREQM registers in the interface memory space, as shown below. *FREQM Register (0:3)* Bit: 7 6 5 4 3 2 1 0 Data Word: 2^{15} 2^{14} 2^{13} 2^{12} 2^{11} 2^{10} 2^{9} 2^{8} *FREQL Register (0:2)* Bit 7 6 5 4 3 2 1 0 Data Word. 2^{7} 2^{6} 2^{5} 2^{4} 2^{3} 2^{2} 2^{1} 2^{0} The frequency number (N) determines the frequency (F) as follows: F = (0.146486) (N) Hz ±0.01%. Hexadecimal frequency numbers (FREQL, FREQ) for commonly generated tones are given below: **Frequency (Hz) FREQM FREQL** 462 0C 52 1100 1D 55 1650 2C 00 1850 31 55 2100 38 00
F1 – F3	Frequency 1,2,3	1:B:5,6,7	The one state of F1, F2 or F3 indicates reception of the respective tonal frequency when the modem is configured for FSK. The default frequencies for F1, F2 and F3 are: **Bit Frequency (Hz)** F1 2100 F2 1100 F3 462
G2FGC	Group II Fast Gain Control	1:C:0	The one state of G2FGC selects a fast AGC rate (8.6 times standard) in Group II Facsimile.
IA1	Interrupt Active (One)	1:E:7	IA1 is a one when Chip 1 is driving $\overline{IRQ}$ to zero volts.
IA0	Interrupt Active (Zero)	0:E:7	IA0 is a one when Chip 0 is driving $\overline{IRQ}$ to zero volts.
IE0	Interrupt Enable (Zero)	0:E:2	The one state of IE0 causes the $\overline{IRQ}$ output to be low when the DA0 bit is a one.
IE1	Interrupt Enable (One)	1:E:2	The one state of IE1 causes the $\overline{IRQ}$ output to be low when the DA1 bit is a one.
J3L	Japanese 3 Link	1:D:4	The one state of J3L selects this standard for link amplitude equalizer. The zero state of J3L selects U.S. survey long
LRTH	Lower Receive Threshold	0:5:0	The one state of LRTH lowers the receiver turn-on threshold from −43 dBm to −47 dBm.
PDM	Parallel Data Mode	0:F:7	The one state of PDM places the modem in the parallel mode and inhibits the reading of Chip 0 diagnostic data.

7

R96FAX Interface Memory Definitions (continued)

Mnemonic	Name	Memory Location	Description
$\overline{\text{PNDET}}$	Period 'N' Detector	1:7:6	The zero state of $\overline{\text{PNDET}}$ indicates a PN sequence has been detected. $\overline{\text{PNDET}}$ sets to a one at the end of the PN sequence.
$\overline{\text{P2DET}}$	Period '2' Detector	1:4:2	The zero state of $\overline{\text{P2DET}}$ indicates a P2 sequence has been detected. $\overline{\text{P2DET}}$ sets to a one at the start of the PN sequence.
(None)	RAM Access B	1:F:0–7	Contains the RAM access code used in reading or writing RAM locations in Chip 1 (baud rate device).
(None)	RAM Access S	0:F:0–6	Contains the RAM access code used in reading RAM locations in Chip 0 (sample rate device).
(None)	RAM Data XBL	1:2:0–7	Least significant byte of 16-bit word x used in reading RAM locations in Chip 1 (baud rate device).
(None)	RAM Data XBM	1:3:0–7	Most significant byte of 16-bit word x used in reading RAM locations in Chip 1 (baud rate device).
(None)	RAM Data XSL	0:2:0–7	Least significant byte of 16-bit word x used in reading RAM locations in Chip 0 (sample rate device).
(None)	RAM Data XSM	0:3:0–7	Most significant byte of 16-bit word x used in reading RAM locations in Chip 0 (sample rate device).
(None)	RAM Data YBL	1:0:0–7	Least significant byte of 16-bit word y used in reading or writing RAM locations in Chip 1 (baud rate device). See DA1.
(None)	RAM Data YBM	1:1:0–7	Most significant byte of 16-bit word y used in reading or writing RAM locations in Chip 1 (baud rate device).
(None)	RAM Data YSL	0:0:0–7	Least significant byte of 16-bit word y used in reading RAM locations in Chip 0 (sample rate device). Shared by parallel data mode for presenting channel data to the host microprocessor bus. See Transceiver Data and DA0.
(None)	RAM Data YSM	0:1:0–7	Most significant byte of 16-bit word y used in reading RAM locations in Chip 0 (sample rate device).
RLE	Receiver Link Equalizer	1:D:5	The one state of RLE enables the link amplitude equalizer in the receiver.
RTS	Request-to-Send	0:5:7	The one state of RTS begins a transmit sequence. The modem will continue to transmit until RTS is turned off, and the turn-off sequence has been completed. RTS parallels the operation of the hardware RTS control input. These inputs are "ORed" by the modem.
SETUP	Setup	0:E:3	The one state of SETUP causes the modem to reconfigure to the control word in the configuration register, and to assume the options specified for equalizer (0:5:1) and threshold (0:5:0). SETUP returns to zero when acted on by the modem.
SQEXT	Squelch Extend	0:5:2	The one state of SQEXT inhibits reception of signals for 130 ms after the turn-off sequence.
TDIS	Training Disable	0:5:6	If TDIS is a one in the receive state, the modem is prevented from entering the training phase. If TDIS is a one prior to RTS going on, the generation of a training sequence is prevented at the start of transmission.
TLE	Transmitter Link Equalizer	1:D:6	The one state of TLE enables the link amplitude equalizer in the transmitter.
(None)	Transceiver Data	0:0:0–7	In parallel data mode, the modem presents eight bits of channel data in register 0:0 for reading by the host microprocessor. After the eight bits have been accumulated they are transferred to 0:0 and bit 0:E:0 goes to a one. When the host reads 0:0, bit 0:E:0 resets to a zero. The first bit of received data is not necessarily located in bit 0:0:0. The host must frame the received data by searching for message sync characters. Bit 0:E:0 sets at one eighth the bit rate in parallel data mode rather than at the sample rate (9600 Hz) as it does when reading RAM locations.
T2	T/2 Equalizer Select	0:5:1	If T2 is a one, an adaptive equalizer with two taps per baud is used. If T2 is a zero, an adaptive equalizer with one tap per baud is used. The number of taps remains the same for both cases.

POWER-ON INITIALIZATION

When power is applied to the R96FAX, a period of 50 to 350 ms is required for power supply settling. The power-on-reset signal (POR) remains low during this period. Approximately 10 ms after the low to high transition of POR, the modem is ready to be configured, and RTS may be activated. If the 5 Vdc power supply drops below 3.5 Vdc for more than 30 msec, the POR cycle is repeated.

At POR time the modem defaults to the following configuration: V.29/9600 bps, T/2 equalizer, serial mode, training enabled, echo protector disable tone, no extended squelch, higher receive threshold, interrupts disabled, no link equalizer, RAM access codes 00.

POR can be connected to a user supplied power-on-reset signal in a wire-or configuration. A low active pulse of 3 μsec or longer applied to the POR pin causes the modem to reset. The modem is ready to be configured 10 msec after the low active pulse is removed from POR.

PERFORMANCE

Whether functioning as a V.27 ter or V.29 type modem, the R96FAX provides the user with unexcelled high performance.

BIT ERROR RATES

The Bit Error Rate (BER) performance of the modem is specified for a test configuration conforming to that specified in CCITT Recommendation V.56, except with regard to the placement of the filter used to bandlimit the white noise source. Bit error rates are measured at a received line signal level of –20 dBm as illustrated.

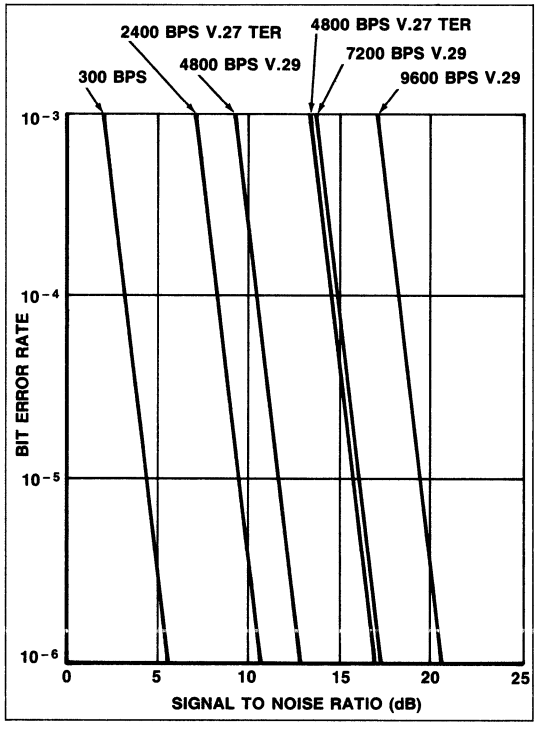
PHASE JITTER

At 2400 bps, the modem exhibits a bit error rate of 10^{-6} or less with a signal-to-noise ratio of 12.5 dB in the presence of 15° peak-to-peak phase jitter at 150 Hz or with a signal-to-noise ratio of 15 dB in the presence of 30° peak-to-peak phase jitter at 120 Hz (scrambler inserted).

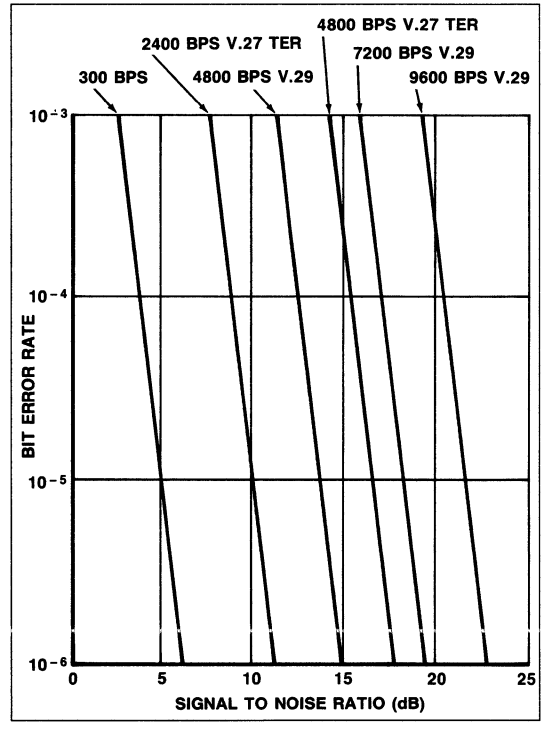
At 4800 bps (V.27 ter), the modem exhibits a bit error rate of 10^{-6} or less with a signal-to-noise ratio of 19 dB in the presence of 15° peak-to-peak phase jitter at 60 Hz.

At 9600 bps, the modem exhibits a bit error rate of 10^{-6} or less with a signal-to-noise ratio of 23 dB in the presence of 10° peak-to-peak phase jitter at 60 Hz. The modem exhibits a bit error rate of 10^{-5} or less with a signal-to-noise ratio of 23 dB in the presence of 20° peak-to-peak phase jitter at 30 Hz.

An example of the BER performance capabilities is given in the following diagrams:

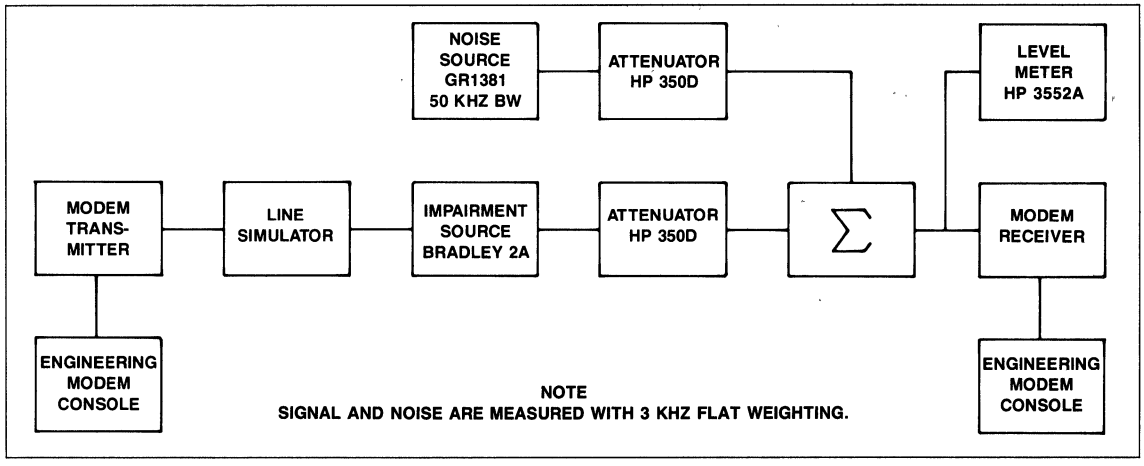


Typical Bit Error Rate (Back to Back, T Equalizer, Level –20 dBm)



Typical Bit Error Rate (Unconditioned (3002) Line, T Equalizer, Level –20 dBm)

The BER performance test set-up is shown in the following diagram:



BER Performance Test Set-up

GENERAL SPECIFICATIONS

Power

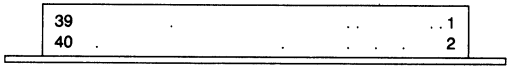
Voltage	Tolerance	Current (Typical) @ 25°C	Current (Max)
+5 Vdc	±5%	400 mA	<500
+12 Vdc	±5%	5 mA	<10
−12 Vdc	±5%	20 mA	<50
Note: All voltages must have ripple ≤0.1 volts peak-to-peak.			

Environmental

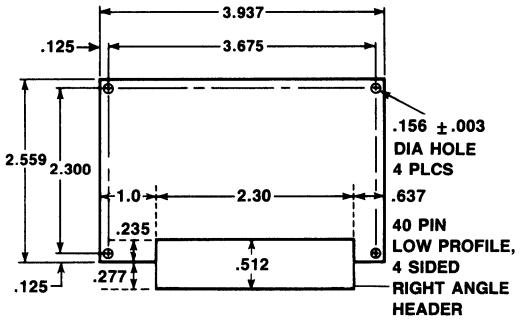
Parameter	Specification
Temperature	
Operating	0°C to +60°C (32 to 140°F)
Storage	−40°C to +80°C (−40 to 176°F) (Stored in heat sealed antistatic bag and shipping container)
Relative Humidity	Up to 90% noncondensing, or a wet bulb temperature up to 35°C, whichever is less.

Mechanical

Parameter	Specification
Board Structure	Single PC board with single right angle header with 40 pins. Burndy FRS 40BS8P or equivalent mating connector.
Dimensions	Length—2.56 in. (65 mm) Width—3.94 in. (100 mm) Height—0.40 in. (10.2 mm)
Weight	Less than—2.6 oz. (73 g)
Lead Extrusion	Maximum—0.100 in. (2.54 mm)



Header Pin Assignment



Printed Circuit Board (PCB) Dimensions

R96FAX Pin Assignment and PCB Dimensions

7

Rockwell

R96DP
9600 BPS DATA PUMP MODEM

INTRODUCTION

The Rockwell R96DP is a synchronous serial 9600 bps modem designed for full-duplex operation over either four-wire dedicated unconditioned lines or half-duplex operation over the general switched telephone network.

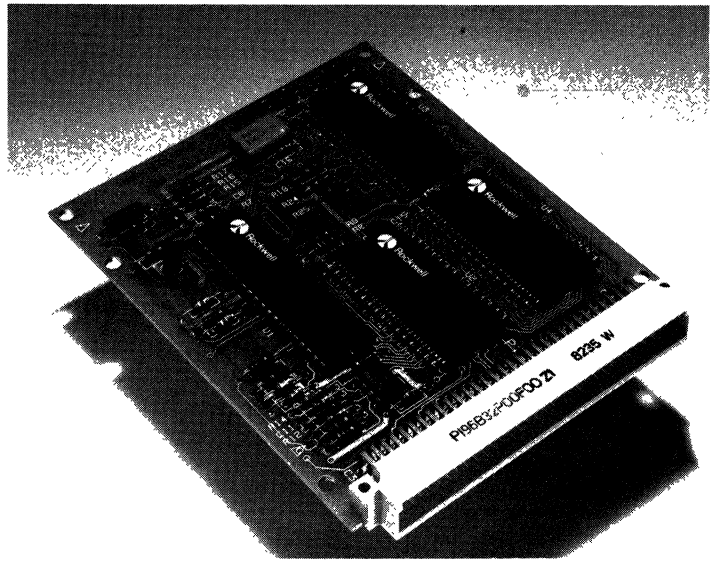
The modem satisfies telecommunications requirements specified in CCITT Recommendations V.29 and V.27 bis/ter.

The small size and low power consumption of the modem offer the user flexibility in creating a 9600 bps modem design customized for specific packaging and functional requirements.

The modem is capable of operating at 9600, 7200, 4800, and 2400 bps.

FEATURES

- User Compatibility:
  - — CCITT V.29, and V.27 bis/ter
- Full-Duplex (4-Wire)
- Half-Duplex
- Programmable Tone Generation
- Dynamic Range – 43 dBm to 0 dBm
- Diagnostic Capability
- Equalization:
  - — Automatic Adaptive
  - — Compromise Cable (Selectable)
  - — Compromise Link (Selectable)
- DTE Interface:
  - — Microprocessor Bus
  - — CCITT V.24 (RS-232-C Compatible)
- Loopbacks
  - — Local Analog (V.54 Loop 3)
  - — Remote Analog (Locally Activated)
  - — Remote Digital (Locally Activated V.54 Loop 2)
- Small Size — 100 mm × 120mm (4.0 × 4.8 inches)
- Low Power Consumption (3 watts, typical)
- Programmable Transmit Output Level
- TTL and CMOS Compatible



R96DP Modem

TECHNICAL SPECIFICATIONS

TRANSMITTER CARRIER FREQUENCIES

Transmitter Carrier Frequencies

Function	Frequency (Hz ±0.01%)
V.27 bis/ter Carrier	1800
V.29 Carrier	1700

TONE GENERATION

Under control of the host processor, the R96DP can generate voice band tones up to 4800 Hz with a resolution of 0.15 Hz and an accuracy of 0.01%. Tones over 3000 Hz are attenuated.

SIGNALING AND DATA RATES

Signaling/Data Rates

Parameter	Specification (±0.01%)
Signaling Rate: Data Rate:	2400 Baud 9600 bps, 7200 bps, 4800 bps
Signaling Rate: Data Rate:	1600 Baud 4800 bps
Signaling Rate: Data Rate:	1200 Baud 2400 bps

DATA ENCODING

At 2400 baud, the data stream is encoded per CCITT V.29. At 9600 bps, the data stream is divided in groups of four-bits (quadbits) forming a 16-point structure. At 7200 bps, the data stream is divided into three bits (tribits) forming an 8-point structure. At 4800 bps, the data stream is divided into two bits (dibits) forming a 4-point structure.

At 1600 baud, the 4800 bps data stream is encoded into tribits per CCITT V.27 bis/ter.

At 1200 baud, the 2400 bps data stream is encoded into dibits per CCITT V.27 bis/ter.

EQUALIZERS

The R96DP provides equalization functions that improve performance when operating over low quality lines.

Cable Equalizers — Selectable compromise cable equalizers in the receiver and transmitter are provided to optimize performance over different lengths of non-loaded cable of 0.4 mm diameter.

Link Equalizers — Selectable compromise link equalizers in the receiver optimize performance over channels exhibiting severe amplitude and delay distortion. Two standards are provided: U.S. survey long and Japanese 3-link.

Automatic Adaptive Equalizer — An automatic adaptive equalizer is provided in the receiver circuit. The equalizer can be configured as either a T or a T/2 equalizer.

TRANSMITTED DATA SPECTRUM

If the cable equalizer is not enabled, the transmitter spectrum is shaped by the following raised cosine filter functions:

1. *1200 Baud.* Square root of 90 percent
2. *1600 Baud.* Square root of 50 percent
3. *2400 Baud.* Square root of 20 percent

The out-of-band transmitter power limitations meet those specified by Part 68 of the FCC's rules, and typically exceed the requirements of foreign telephone regulatory bodies.

SCRAMBLER/DESCRAMBLER

The R96DP incorporates a self-synchronizing scrambler/descrambler. This facility is in accordance with either V.27 bis/ter or V.29 depending on the selected configuration.

RECEIVED SIGNAL FREQUENCY TOLERANCE

The receiver circuit of the R96DP can adapt to received frequency error of up to ±10 Hz with less than 0.2 dB degradation in BER performance.

RECEIVE LEVEL

The receiver circuit of the modem satisfies all specified performance requirements for received line signal levels from 0 dBm to –43 dBm. The received line signal level is measured at the receiver analog input (RXA).

RECEIVE TIMING

The R96DP provides a data derived Receive Data Clock (RDCLK) output in the form of a squarewave. The low to high transitions of this output coincide with the centers of received data bits. The timing recovery circuit is capable of tracking a ±0.01% frequency error in the associated transmit timing source.

TRANSMIT LEVEL

The transmitter output level is accurate to ±1.0 dB and is programmable from –1.0 dBm to –15.0 dBm in 2 dB steps.

TRANSMIT TIMING

The R96DP provides a Transmit Data Clock (TDCLK) output with the following characteristics:

1. *Frequency.* Selected data rate of 9600, 7200, 4800, or 2400 Hz (±0.01%).
2. *Duty Cycle.* 50% ±1%

Input data presented on TXD is sampled by the R96DP at the low to high transition of TDCLK. Data on TXD must be stable for at least one microsecond prior to the rising edge of TDCLK and remain stable for at least one microsecond after the rising edge of TDCLK.

EXTERNAL TRANSMIT CLOCK

The transmitter data clock (TDCLK) can be phase locked to a signal on input XTCLK. This input signal must equal the desired data rate ±0.01% with a duty cycle of 50% ±20%.

TRAIN ON DATA

When train on data is enabled, the receiver typically trains on data in less than 15 seconds for V.29 and 3.5 seconds for V.27.

TURN-ON SEQUENCE

A total of 14 selectable turn-on sequences can be generated as defined in the following table:

Turn-On Sequences

No.	V.29	V.27 bis/ter	CTS Response Time (milliseconds)	Comments
1	9600 bps		253	
2	7200 bps		253	
3	4800 bps		253	
4		4800 bps long	708	
5		2400 bps long	943	
6		4800 bps short	50	
7		2400 bps short	67	
8	9600 bps		458	Preceded by
9	7200 bps		458	Echo Protector
10	4800 bps		458	Tone for lines
11		4800 bps long	913	using echo
12		2400 bps long	1148	supressors*
13		4800 bps short	255	
14		2400 bps short	272	

*For short echo protector tone, subtract 155 ms from values of CTS response time.

TURN-OFF SEQUENCE

For V.27 ter, the turn-off sequence consists of approximately 10 ms of remaining data and scrambled ones at 1200 baud or approximately 7 ms of data and scrambled ones at 1600 baud followed by a 20 ms period of no transmitted energy. For V.29, the turn-off sequence consists of approximately 5 ms of remaining data and scrambled 1's.

CLAMPING

Received Data (RXD) is clamped to a constant mark (one) whenever the Received Line Signal Detector (RLSD) is off.

RESPONSE TIMES OF CLEAR-TO-SEND (CTS)

The time between the off-to-on transition of Request-To-Send (RTS) and the off-to-on transition of CTS is dictated by the length of the training sequence and the echo suppressor disable tone, if used. These times are listed in the Turn-On Sequences table. If training is not enabled RTS/CTS delay is less than 2 baud times.

The time between the on-to-off transition of RTS and the on-to-off transition of CTS in the data state is a maximum of 2 baud times for all configurations.

RECEIVED LINE SIGNAL DETECTOR (RLSD)

For V.27 bis/ter or V.29, RLSD turns on at the end of the training sequence. If training is not detected at the receiver, the RLSD off-to-on response time is 15 ±10 ms. The RLSD on-to-off response time for V.27 is 10 ±5 ms and for V.29 is 30 ±9ms. Response times are measured with a signal at least 3 dB above the actual RLSD on threshold or at least 5 dB below the actual RLSD off threshold.

The RLSD on-to-off response time ensures that all valid data bits have appeared on RXD.

Four threshold options are provided:
1. Greater than −43 dBm (RLSD on)
   Less than −48 dBm (RLSD off)
2. Greater than −33 dBm (RLSD on)
   Less than −38 dBm (RLSD off)
3. Greater than −26 dBm (RLSD on)
   Less than −31 dBm (RLSD off)
4. Greater than −16 dBm (RLSD on)
   Less than −21 dBm (RLSD off)

NOTE

Performance may be at a reduced level when the received signal is less than −43 dBm.

A minimum hysteresis action of 2 dB exists between the actual off-to-on and on-to-off transition levels. The threshold levels and hysteresis action are measured with an unmodulated carrier signal applied to the receiver's audio input (RXA).

MODES OF OPERATION

The R96DP is capable of being operated in either a serial or a parallel mode of operation.

SERIAL MODE

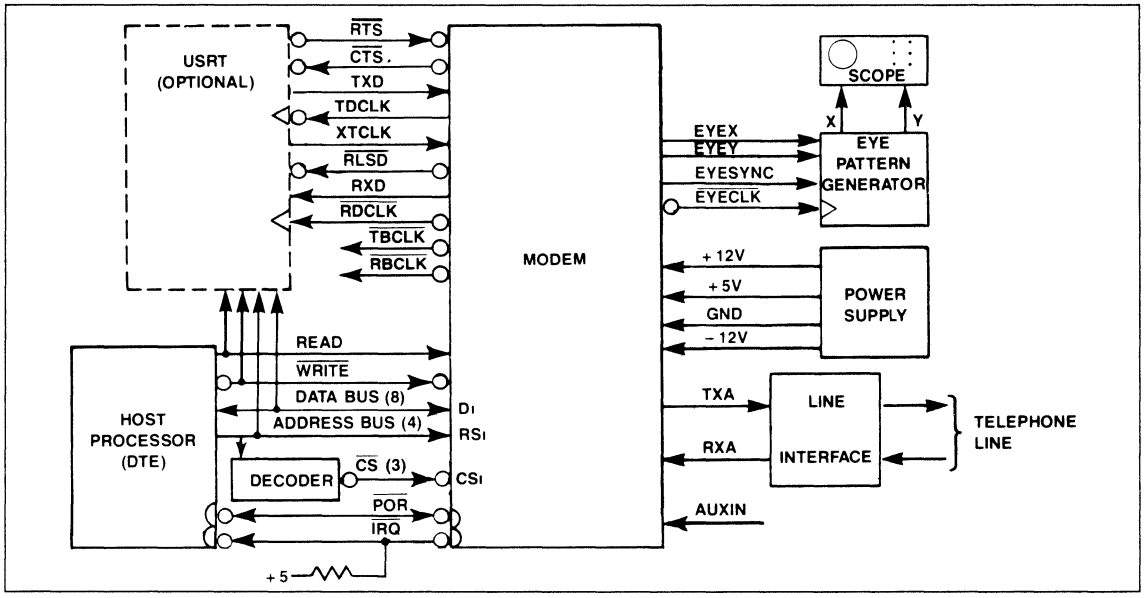
The serial mode uses standard V.24 (RS-232-C compatible) signals to transfer channel data. An optional USRT device (shown in the Functional Interconnect Diagram) illustrates this capability.

PARALLEL MODE

The R96DP has the capability of transferring channel data up to eight bits at a time via the microprocessor bus.

MODE SELECTION

Selection of either the serial or parallel mode of operation is by means of a control bit. To enable the parallel mode, the control bit must be set to a 1. The modem automatically defaults to the serial mode at power-on. In either mode the R96DP is configured by the host processor via the microprocessor bus.



R96DP Functional Interconnect Diagram

INTERFACE CRITERIA

The modem interface comprises both hardware and software circuits. Hardware circuits are assigned to specific pins in a 64-pin DIN connector. Software circuits are assigned to specific bits in a 48-byte interface memory.

HARDWARE CIRCUITS

Signal names and descriptions of the hardware circuits, including the microprocessor interface, are listed in the R96DP Hardware Circuits table. In the table, the column titled 'Type' refers to designations found in the Hardware Circuit Characteristics. The microprocessor interface is designed to be directly compatible with an 8080 microprocessor. With the addition of a few external logic gates, it can be made compatible with 6500, 6800, or 68000 microprocessors.

R96DP Hardware Circuits

Name	Type	Pin No.	Description
A. OVERHEAD:			
Ground (A)	AGND	31C,32C	Analog Ground Return
Ground (D)	DGND	3C,8C,5A,10A	Digital Ground Return
+5 volts	PWR	19C,23C,26C,30C	+5 volt supply
+12 volts	PWR	15A	+12 volt supply
–12 volts	PWR	12A	–12 volt supply
$\overline{POR}$	I/OA	13C	Power-on-reset
B. MICROPROCESSOR INTERFACE:			
D7	I/OA	1C	Data Bus (8 Bits)
D6	I/OA	1A	
D5	I/OA	2C	
D4	I/OA	2A	
D3	I/OA	3A	
D2	I/OA	4C	
D1	I/OA	4A	
D0	I/OA	5C	
RS3	IA	6C	Register Select (4 Bits)
RS2	IA	6A	
RS1	IA	7C	
RS0	IA	7A	
$\overline{CS0}$	IA	10C	Chip Select Transmitter Device
$\overline{CS1}$	IA	9C	Chip Select Receiver Sample Rate Device
$\overline{CS2}$	IA	9A	Chip Select Receiver Baud Rate Device
READ	IA	12C	Read Enable
$\overline{WRITE}$	IA	11A	Write Enable
$\overline{IRQ}$	OB	11C	Interrupt Request

7

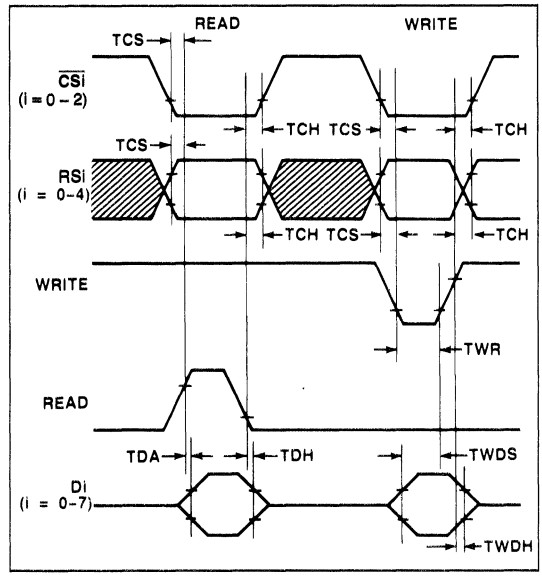
R96DP Hardware Circuits (Cont.)

Name	Type	Pin No.	Description
C. V.24 INTERFACE:			
$\overline{RDCLK}$	OC	21A	Receive Data Clock
TDCLK	OC	23A	Transmit Data Clock
XTCLK	IB	22A	External Transmit Clock
$\overline{RTS}$	IB	25A	Request-to-Send
$\overline{CTS}$	OC	25C	Clear-to-Send
TXD	IB	24C	Transmitter Data
RXD	OC	22C	Receiver Data
$\overline{RLSD}$	OC	24A	Received Line Signal Detector
D. ANCILLARY CIRCUITS:			
$\overline{RBCLK}$	OC	26A	Receiver Baud Clock
$\overline{TBCLK}$	OC	27C	Transmitter Baud Clock
E. ANALOG SIGNALS:			
TXA	AA	31A	Transmitter Analog Output
RXA	AB	32A	Receiver Analog Input
AUXIN	AC	30A	Auxiliary Analog Input
F. DIAGNOSTIC:			
EYEX	OC	15C	Eye Pattern Data—X Axis
EYEY	OC	14A	Eye Pattern Data—Y Axis
$\overline{EYECLK}$	OA	14C	Eye Pattern Clock
EYESYNC	OA	13A	Eye Pattern Synchronizing Signal

EYE PATTERN GENERATION

The four hardware diagnostic circuits, identified in the preceding table, allow the user to generate and display an eye pattern. Circuits EYEX and EYEY serially present eye pattern data for the horizontal and vertical display inputs respectively. The 8-bit data words are shifted out most significant bit first, clocked by the rising edge of the $\overline{EYECLK}$ output. The EYESYNC output is provided for word synchronization. The falling edge of EYESYNC may be used to transfer the 8-bit word from the shift register to a holding register. Digital to analog conversion can then be performed for driving the X and Y inputs of an oscilloscope.

MICROPROCESSOR TIMING



Microprocessor Interface Timing Diagram

Critical Timing Requirements

Characteristic	Symbol	Min	Max	Units
$\overline{CSi}$, RSi setup time prior to Read or $\overline{Write}$	TCS	30	—	nsec
Data access time after Read	TDA	—	140	nsec
Data hold time after Read	TDH	10	50	nsec
CSi, RSi hold time after Read or $\overline{Write}$	TCH	10	—	nsec
Write data setup time	TWDS	75	—	nsec
Write data hold time	TWDH	10	—	nsec
Write strobe pulse width	TWR	75	—	nsec

HARDWARE CIRCUIT CHARACTERISTICS

Digital Interface Characteristics

Digital Interface Characteristics

Symbol	Parameter	Units	Input/Output Type IA	IB	IC	OA	OB	OC	I/O A	I/O B
V_{IH}	Input Voltage, High	V	2.0 Min.	2.0 Min.	2.0 Min.				2.0 Min.	5.25 Max. 2.0 Min.
V_{IL}	Input Voltage, Low	V	0.8 Max.	0.8 Max.	0.8 Max.				0 8 Max.	0 8 Max.
V_{OH}	Output Voltage, High	V				2.4 Min.[1]			2.4 Min.[1]	2.4 Min [3]
V_{OL}	Output Voltage, Low	V				0.4 Max [2]	0.4 Max.[2]	0 4 Max.[2]	0.4 Max.[2]	0.4 Max.[2]
I_{IN}	Input Current, Leakage	μA	±2.5 Max.						±2.5 Max.[4]	
I_{OH}	Output Current, High	mA				−0.1 Max.				
I_{OL}	Output Current, Low	mA				1.6 Max	1.6 Max.	1.6 Max.		
I_L	Output Current, Leakage	μA					±10 Max			
I_{PU}	Pull-up Current (Short Circuit)	μA		−240 Max. −10 Min.	−240 Max. −10 Min.			−240 Max. −10 Min		−260 Max. −100 Min.
C_L	Capacitive Load	pF	5	5	20				10	40
C_D	Capacitive Drive	pF				100	100	100	100	100
	Circuit Type		TTL	TTL w/Pull-up	TTL w/Pull-up	TTL	Open-Drain	Open-Drain w/Pull-up	3-State Transceiver	Open-Drain w/Pull-up

Notes

1. I Load = −100 μA
2. I Load = 1.6 mA
3. I Load = −40 μA
4. V_{IN} = 0.4 to 2 4 Vdc, V_{CC} = 5.25 Vdc

Analog Interface Characteristics

Analog Interface Characteristics

Name	Type	Characteristics
TXA	AA	The transmitter output is a low impedance operational amplifier output. In order to match to 600 ohms, an external series resistor is required.
RXA	AB	The receiver input impedance is 63.4K ohms ±5%.
AUXIN	AC	The auxiliary analog input allows access to the transmitter for the purpose of interfacing with user provided equipment. Because this is a sampled data input, any signal above 4800 Hz will cause aliasing errors. The input impedance is 1K ohms, and the gain to transmitter output is −1 dB ±1 dB.

SOFTWARE CIRCUITS

The R96DP comprises three signal processor chips. Each of these chips contains 16 registers to which an external (host) microprocessor has access. Although these registers are within the modem, they may be addressed as part of the host processor's memory space. The host may read data out of or write data into these registers. The registers are referred to as interface memory. Registers in chip 1 update at half the modem sample rate (4800 bps). Registers in chip 0 and 2 update at the selected baud rate.

When information in these registers is being discussed, the format Y:Z:Q is used. The chip is specified by Y(0 − 2), the register by Z(0 − F), and the bit by Q(0 − 7, 0 = LSB).

Status Control Bits

The operation of the R96DP is affected by a number of software control inputs. These inputs are written into registers within the interface memory via the host microprocessor bus. Bits designated by an 'x' are "Don't Care" inputs that can be set to either 1 or 0. Modem operation is monitored by various software flags that are read from interface memory via the host microprocessor bus. All status and control bits are defined in the Interface Memory table. Bits designated by an 'R' are reserved for modem use only and must not be changed by the host.

RAM Data Access

The R96DP provides the user with access to much of the data stored in the modem's memories. This data is useful for performing certain diagnostic functions.

Two RAM access registers in chip 1 allow user access to RAM locations via the X word registers (1:3 and 1:2) and the Y word registers (1:1 and 1:0). Comparable registers in chip 2 provide access to chip 2 RAM locations. The access code stored in RAM ACCESS XS (1:5) selects the source of data for RAM DATA XSM and RAM DATA XSL (1:3 and 1:2). Similarly, the access code stored in RAM ACCESS YS (1:4) selects the source of data for RAM DATA YSM and RAM DATA YSL (1:1 and 1:0). Chip 2 registers are associated in the same way.

Reading of RAM data is performed by storing the necessary access codes in 1:5 and 1:4 (or 2:5 and 2:4), reading 1:0 (or 2:0) to reset the associated data available bit (1:E:0 or 2:E:0), then waiting for the data available bit to return to a one. Data is now valid and may be read from 1:3 through 1:0 (or 2:3 through 2:0). The contents of registers 2:3 and 2:1 are also available serially on outputs EYEX and EYEY, respectively, unless the IFIX bit (1:6:7) is set to a one. When IFIX is a one, EYEX and EYEY remain fixed on the rotated equalizer output.

7

RAM Access Codes

The RAM access codes defined in the following table allow the host processor to read diagnostic information within the modem.

RAM Access Codes

No.	Function	Chip	X Access	Y Access	Register
1	Received Signal Samples	1	C0	Not Used	2,3
2	Demodulator Output	1	C2	42	0,1,2,3
3	Low Pass Filter Output	1	D4	54	0,1,2,3
4	Average Energy	1	Not Used	04	0,1
5	AGC Gain Word	1	81	Not Used	2,3
6	Equalizer Input	2	C0	40	0,1,2,3
7	Equalizer Tap Coefficients	2	81 – AO	01 – 20	0,1,2,3
8	Unrotated Equalizer Output	2	E1	61	0,1,2,3
9	Rotated Equalizer Output (Received Points)	2	A2	22	0,1,2,3
10	Decision Points (Ideal Data Points)	2	E2	62	0,1,2,3
11	Error	2	E3	63	0,1,2,3
12	Rotation Angle	2	Not Used	00	0,1
13	Frequency Correction	2	AA	Not Used	2,3
14	EQM	2	A7	Not Used	2,3
15	Dual Point	2	AE	2E	0,1,2,3

NOTE

In the interface memory tables that follow, those columns marked by an 'X' indicate a user available bit position that is not currently used by the R96DP. However, those columns marked by an 'R' indicate reserved and are for modem use *only*.

Transmitter Interface Memory Chip 0 ($\overline{CS0}$)

Bit / Register	7	6	5	4	3	2	1	0
F	R	R	R	R	R	R	R	R
E	TIA	R	R	R	TSB	TIE	R	TBA
D	R	R	R	R	R	R	R	R
C	R	R	R	R	R	R	R	R
B	R	R	R	R	R	R	R	R
A	R	R	R	R	R	R	R	R
9	R	R	R	R	R	R	R	R
8	R	R	R	R	R	R	R	R
7	RTS	TTDIS	SDIS	MHLD	EPT	TPDM	XCEN	SEPT
6	TRANSMITTER CONFIGURATION							
5	X	X	CEQ		LAEN	LDEN	A3L	D3L
4	L3ACT	L4ACT	L4HG	TLVL			L2ACT	LCEN
3	FREQM							
2	FREQL							
1	R	R	R	R	R	R	R	R
0	TRANSMITTER DATA							
Register / Bit	7	6	5	4	3	2	1	0

Receiver Interface Memory Chip 1 ($\overline{CS1}$)

Bit / Register	7	6	5	4	3	2	1	0
F	R	R	R	R	R	R	R	R
E	RSIA	R	R	R	RSB	RSIE	R	RSDA
D	R	R	R	R	R	R	R	R
C	R	R	R	R	R	R	R	R
B	R	$\overline{PNDET}$	R	R	R	R	R	$\overline{CDET}$
A	R	R	R	R	R	R	R	R
9	R	$\overline{FED}$	R	R	R	R	R	R
8	R	R	R	R	R	P2DET	R	R
7	RTH		DDIS	RPDM	R	R	T2	RTDIS
6	IFIX	TOD	RECEIVER CONFIGURATION					
5	RAM ACCESS XS							
4	RAM ACCESS YS							
3	RAM DATA XSM							
2	RAM DATA XSL							
1	RAM DATA YSM							
0	RAM DATA YSL; RECEIVER DATA							
Register / Bit	7	6	5	4	3	2	1	0

Receiver Interface Memory Chip 2 ($\overline{CS2}$)

Bit / Register	7	6	5	4	3	2	1	0
F	R	R	R	R	R	R	R	R
E	RBIA	R	R	R	R	RBIE	R	RBDA
D	R	R	R	R	R	R	R	R
C	R	R	R	R	R	R	R	R
B	R	R	R	R	R	R	R	R
A	R	R	R	R	R	R	R	R
9	R	R	R	R	R	R	R	R
8	R	R	R	R	R	R	R	R
7	R	R	R	R	R	R	R	R
6	R	R	R	R	R	R	R	R
5	RAM ACCESS XB							
4	RAM ACCESS YB							
3	RAM DATA XBM							
2	RAM DATA XBL							
1	RAM DATA YBM							
0	RAM DATA YBL							
Register / Bit	7	6	5	4	3	2	1	0

R96DP Interface Memory Definitions

Mnemonic	Name	Memory Location	Description
A3L	Amplitude 3-Link Select	0:5:1	See LAEN.
CEQ	Cable Equalizer Field	0:5:(4,5)	The CEQ Control field simultaneously controls amplitude compromise equalizers in both the transmit and receive paths The following table lists the possible cable equalizer selection codes: **CEQ** — **Cable Length (0.4 mm diameter)** 0 — 0.0 1 — 1 8 km 2 — 3.6 km 3 — 7.2 km
$\overline{\text{CDET}}$	Carrier Detector	1:B:0	When zero, status bit $\overline{\text{CDET}}$ indicates that passband energy is being detected, and that a training sequence is not in process. $\overline{\text{CDET}}$ goes to a zero at the start of the data state, and returns to a one at the end of the received signal.
DDIS	Descramble Disable	1:7·5	When control bit DDIS is a one, the receiver descrambler circuit is removed from the data path.
D3L	Delay 3-Link Select	0.5:0	See LDEN.
EPT	Echo Protector Tone	0:7:3	When control bit EPT is a one, an unmodulated carrier is transmitted for 185 ms (optionally 30 ms) followed by 20 ms of no transmitted energy at the start of transmission. This option is available in the V.27 and V.29 Configurations, although it is not specified in the CCITT V 29 recommendation.
$\overline{\text{FED}}$	Fast Energy Detector	1:9:6	When status bit $\overline{\text{FED}}$ is a zero, it indicates that energy above the receiver threshold is present in the passband.
(None)	FREQL/FREQM	0:2:0–7, 0:3:0–7	The host processor conveys tone generation data to the transmitter by writing a 16-bit data word to the FREQL and FREQM registers in the interface memory space, as shown below: *FREQM Register (0:3)* **Bit:** 7 6 5 4 3 2 1 0 **Data Word:** 2^{15} 2^{14} 2^{13} 2^{12} 2^{11} 2^{10} 2^{9} 2^{8} *FREQL Register (0:2)* **Bit:** 7 6 5 4 3 2 1 0 **Data Word:** 2^{7} 2^{6} 2^{5} 2^{4} 2^{3} 2^{2} 2^{1} 2^{0} The frequency number (N) determines the frequency (F) as follows: F = (0.146486) (N) Hz ±0.01% Hexadecimal frequency numbers (FREQL, FREQM) for commonly generated tones are given below: **Frequency (Hz)** — **FREQM** — **FREQL** 462 — 0C — 52 1100 — 1D — 55 1650 — 2C — 00 1850 — 31 — 55 2100 — 38 — 00
IFIX	Eye Fix	1:6:7	When control bit IFIX is a one, the serial data on EYEX and EYEY reflect the rotated equalizer output and do not follow the data selected by RAM ACCESS XB and RAM ACCESS YB.

7

R96DP Interface Memory Definitions (Continued)

Mnemonic	Name	Memory Location	Description
LAEN	Link Amplitude Equalizer Enable	0:5:3	The link amplitude equalizer enable and select bits control an amplitude compromise equalizer in the receive path according to the following table: **LAEN** / **A3L** / **Curve Matched** 0 / X / No Equalizer 1 / 0 / U.S. Survey Long 1 / 1 / Japanese 3-Link
LCEN	Loop Clock Enable	0:4:0	When control bit LCEN is a one, the transmitter clock tracks the receiver clock.
LDEN	Link Delay Equalizer Enable	0:5:2	The link delay equalizer enable and select bits control a delay compromise equalizer in the receive path according to the following table: **LDEN** / **D3L** / **Curve Matched** 0 / X / No Equalizer 1 / 0 / U.S. Survey Long 1 / 1 / Japanese 3-Link
L2ACT	Remote Digital Loopback Activate	0:4:1	When control bit L2ACT is a one, the receiver digital output is connected to the transmitter digital input in accordance with CCITT recommendation V.54 loop 2.
L3ACT	Local Analog Loopback Activate	0:4:7	When control bit L3ACT is a one, the transmitter analog output is coupled to the receiver analog input through an attenuator in accordance with CCITT recommendation V.54 loop 3.
L4ACT	Remote Analog Loopback Activate	0:4:6	When control bit L4ACT is a one, the receiver analog input is connected to the transmitter analog output through a variable gain amplifier in a manner similar to recommendation V.54 loop 4.
L4HG	Loop 4 High Gain	0:4:5	When control bit L4HG is a one, the loop 4 variable gain amplifier is set for +16 dB, and when at zero the gain is zero dB.
MHLD	Mark Hold	0:7:4	When control bit MHLD is a one, the transmitter input data stream is forced to all marks (ones).
$\overline{\text{PNDET}}$	Period N Detector	1:B:6	When status bit $\overline{\text{PNDET}}$ is a zero, it indicates a PN sequence has been detected. This bit sets to a one at the end of the PN sequence.
$\overline{\text{P2DET}}$	Period Two Detector	1:8:2	When status bit $\overline{\text{P2DET}}$ is a zero, it indicates that a P2 sequence has been detected. This bit sets to a one at the start of the PN sequence.
(None)	RAM Access XB	2:5:0–7	Contains the RAM access code used in reading chip 2 RAM locations via word X (2:3 and 2:2).
(None)	RAM Access XS	1:5:0–7	Contains the RAM access code used in reading chip 1 RAM locations via word X (1:3 and 1:2).
(None)	RAM Access YB	2:4:0–7	Contains the RAM access code used in reading chip 2 RAM locations via word Y (2:1 and 2:0).
(None)	RAM Access YS	1:4:0–7	Contains the RAM access code used in reading chip 1 RAM locations via word Y (1:1 and 1:0).
(None)	RAM Data XBL	2:2:0–7	Least significant byte of 16-bit word X used in reading RAM locations in chip 2.
(None)	RAM Data XBM	2:3:0–7	Most significant byte of 16-bit word X used in reading RAM locations in chip 2.
(None)	RAM Data XSL	1:2:0–7	Least significant byte of 16-bit word X used in reading RAM locations in chip 1.
(None)	RAM Data XSM	1:3:0–7	Most significant byte of 16-bit word X used in reading RAM locations in chip 1.

R96DP Interface Memory Definitions (Continued)

Mnemonic	Name	Memory Location	Description
(None)	RAM Data YBL	2:0:0–7	Least significant byte of 16-bit word Y used in reading RAM locations in chip 2.
(None)	RAM Data YBM	2:1:0–7	Most significant byte of 16-bit word Y used in reading RAM locations in chip 2.
(None)	RAM Data YSL	1:0:0–7	Least significant byte of 16-bit word Y used in reading RAM locations in chip 1. Shared by parallel data mode for presenting channel data to the host microprocessor bus. See 'Receiver Data.'
(None)	RAM Data YSM	1:1:0–7	Most significant byte of 16-bit word Y used in reading RAM locations in chip 1.
RBDA	Receiver Baud Data Available	2:E:0	Status bit RBDA goes to a one when the receiver writes data into register 2:0. The bit goes to a zero when the host processor reads data from register 2:0.
RBIA	Receiver Baud Interrupt Active	2:E:7	This status bit is a one whenever the receiver baud rate device is driving $\overline{IRQ}$ low.
RBIE	Receiver Baud Interrupt Enable	2:E:2	When the host processor writes a one in the RBIE control bit, the $\overline{IRQ}$ line of the hardware interface is driven to zero when status bit RBDA is a one.
(None)	Receiver Configuration	1:6:0–5	The host processor configures the receiver by writing a control code into the receiver configuration field in the interface memory space (see RSB). *Receiver Configuration Control Codes* Control codes for the modem receiver configuration are: **Configuration** — **Configuration Code (Hex)** V.29 9600 — 14 V.29 7200 — 12 V.29 4800 — 11 V.27 4800 Long — 22 V.27 2400 Long — 21 V.27 4800 Short — 02 V.27 2400 Short — 01
(None)	Receiver Data	1:0:0–7	The host processor obtains channel data from the receiver in the parallel data mode by reading a data byte from the receiver data register. The data is divided on baud boundaries as is the transmitter data. When using receiver parallel data mode, the registers 1:3 through 1:0 can not be used for reading the chip 1 RAM.
RPDM	Receiver Parallel Data Mode	1:7:4	When control bit RPDM is a one, the receiver supplies channel data to the receiver data register (1:0) as well as to the hardware serial data output. (See Receiver Data)
RSB	Receiver Setup Bit	1:E:3	When the host processor changes the receiver configuration or the RTH field, the host processor must write a one in the RSB control bit. RSB goes to zero when the changes become effective.
RSDA	Receiver Sample Data Available	1:E:0	Status bit RSDA goes to a one when the receiver writes data to register 1:0. RSDA goes to a zero when the host processor reads data from register 1:0.
RSIA	Receiver Sample Interrupt Active	1:E:7	This status bit is a one whenever the receiver sample rate device is driving $\overline{IRQ}$ to zero.
RSIE	Receiver Sample Interrupt Enable	1:E:2	When the host processor writes a one in the RSIE control bit, the $\overline{IRQ}$ line of the hardware interface is driven to zero when status bit RSDA is a one.
RTDIS	Receiver Training Disable	1:7:0	When control bit RTDIS is a one, the receiver is prevented from recognizing a training sequence and entering the training state.
RTH	Receiver Threshold Field	1:7:6,7	The receiver energy detector threshold is set by the RTH field according to the following codes (see RSB): **RTH** — **RLSD On** — **RLSD Off** 0 — > –43 dBm — < –48 dBm 1 — > –33 dBm — < –38 dBm 2 — > –26 dBm — < –31 dBm 3 — > –16 dBm — < –21 dBm

R96DP Interface Memory Definitions (Continued)

Mnemonic	Name	Memory Location	Description
RTS	Request-to-Send	0:7:7	When control bit RTS goes to a one, the modem begins a transmit sequence. It continues to transmit until RTS is reset to zero, and the turn-off sequence has been completed. This input bit parallels the operation of the hardware RTS control input. These inputs are ORed by the modem.
SDIS	Scrambler Disable	0:7:5	When control bit SDIS is a one, the transmitter scrambler circuit is removed from the data path.
SEPT	Short Echo Protector Tone	0:7:0	When control bit SEPT is a one, the echo protector tone is 30 ms long rather than 185 ms.
TBA	Transmitter Buffer Available	0:E·0	This status bit resets to zero when the host processor writes data to transmitter data register 0:0. When the transmitter empties register 0·0, this bit sets to a one.
TIA	Transmitter Interrupt Active	0:E:7	This status bit is a one whenever the transmitter is driving $\overline{IRQ}$ to a zero.
TIE	Transmitter Interrupt Enable	0:E·2	When the host processor writes a one in control bit TIE, the $\overline{IRQ}$ line of the hardware interface is driven to zero when status bit TBA is at a one.
TLVL	Transmitter Level Field	0:4·2–4	The transmitter analog output level is determined by eight TLVL codes, as follows **TLVL** — **Transmitter Analog Output*** 0 — −1 dBm ±1 dB 1 — −3 dBm ±1 dB 2 — −5 dBm ±1 dB 3 — −7 dBm ±1 dB 4 — −9 dBm ±1 dB 5 — −11 dBm ±1 dB 6 — −13 dBm ±1 dB 7 — −15 dBm ±1 dB *Each step above is a 2 dB change ±0.2 dB.
TOD	Train-on Data	1:6:6	When control bit TOD is a one, it enables the train-on-data algorithm to converge the equalizer if the signal quality degrades sufficiently. When TOD is a one, the modem still recognizes a training sequence and enters the force train state. A BER of approximately 10^{-3} for 0.5 seconds initiates train-on-date.
TPDM	Transmitter Parallel Data Mode	0:7:2	When control bit TPDM is a one, the transmitter accepts data for transmission from the transmitter data register (0:0) rather than the serial hardware data input.
(None)	Transmitter Configuration	0:6:0–7	The host processor configures the transmitter by writing a control byte into the transmitter configuration register in its interface memory space. (See TSB). *Transmitter Configuration Control Codes* Control codes for the modem transmitter configurations are: **Configuration** — **Configuration Code (Hex)** V.29 9600 — 14 V.29 7200 — 12 V.29 4800 — 11 V.27 4800 Long — 22 V.27 2400 Long — 21 V.27 4800 Short — 02 V.27 2400 Short — 01 Tone Transmit — 80

R96DP Interface Memory Definitions (Continued)

<table>
<tr><th>Mnemonic</th><th>Name</th><th>Memory Location</th><th>Description</th></tr>
<tr><td>(None)</td><td>Transmitter Data</td><td>0:0:0–7</td><td>The host processor conveys output data to the transmitter in the parallel mode by writing a data byte to the transmitter data register. The data is divided on baud boundaries, as follows:
NOTE
Data is transmitted bit zero first.
<table>
<tr><th rowspan="2">Configuration</th><th colspan="8">Bits</th></tr>
<tr><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr>
<tr><td>V.29 9600 bps</td><td colspan="4">Baud 1</td><td colspan="4">Baud 0</td></tr>
<tr><td>V.29 7200 bps</td><td colspan="2">Not Used</td><td colspan="3">Baud 1</td><td colspan="3">Baud 0</td></tr>
<tr><td>V.29 4800 bps</td><td colspan="2">Baud 3</td><td colspan="2">Baud 2</td><td colspan="2">Baud 1</td><td colspan="2">Baud 0</td></tr>
<tr><td>V.27 4800 bps</td><td colspan="2">Not Used</td><td colspan="3">Baud 1</td><td colspan="3">Baud 0</td></tr>
<tr><td>V.27 2400 bps</td><td colspan="2">Baud 3</td><td colspan="2">Baud 2</td><td colspan="2">Baud 1</td><td colspan="2">Baud 0</td></tr>
</table></td></tr>
<tr><td>TSB</td><td>Transmitter Setup Bit</td><td>0:E:3</td><td>When the host processor changes the transmitter configuration, the host must write a one in this control bit. TSB goes to a zero when the change becomes effective.</td></tr>
<tr><td>TTDIS</td><td>Transmitter Train Disable</td><td>0:7:6</td><td>When control bit TTDIS is a one, the transmitter does not generate a training sequence at the start of transmission. With training disabled, RTS/CTS delay is less than two baud times.</td></tr>
<tr><td>T2</td><td>T/2 Equalizer Select</td><td>1:7:1</td><td>When control bit T2 is a one, an adaptive equalizer with two taps per baud is used. When T2 is a zero, the equalizer has one tap per baud. The total number of taps remains the same for both cases.</td></tr>
<tr><td>XCEN</td><td>External Clock Enable</td><td>0:7:1</td><td>When control bit XCEN is a zero, the transmitter timing is established by the external clock supplied at the hardware input XTCLK, pin 22A.</td></tr>
</table>

POWER-ON INITIALIZATION

When power is applied to the R96DP, a period of 50 to 350 ms is required for power supply settling. The power-on-reset signal (POR) remains low during this period. Approximately 10 ms after the low to high transition of POR, the modem is ready to be configured, and RTS may be activated. If the 5 Vdc power supply drops below 3.5 Vdc for more than 30 msec, the POR cycle is generated.

At POR time the modem defaults to the following configuration: V.29, 9600 bps, T/2, standard echo protector tone, serial data mode, internal clock, cable equalizers disabled, link amplitude equalizer disabled, link delay equalizer disabled, transmitter output level set to −1 dBm ±1 dB, interrupts disabled, receiver threshold set to −43 dBm, eye pattern selectable, and train-on-data disabled.

POR can be connected to a user supplied power-on-reset signal in a wire-or configuration. A low active pulse of 3 μsec or more applied to the POR pin causes the modem to reset. The modem is ready to be configured 10 msec after POR is removed

PERFORMANCE

Whether functioning as a V.27 ter or V.29 type modem, the R96DP provides the user with unexcelled high performance.

BIT ERROR RATES

The Bit Error Rate (BER) performance of the modem is specified for a test configuratio conforming to that specified in CCITT Recommendation V.56, except with regard to the placement of the filter used to bandlimit the white noise source. Bit error rates are measured at a received line signal level of −20 dBm as illustrated.

PHASE JITTER

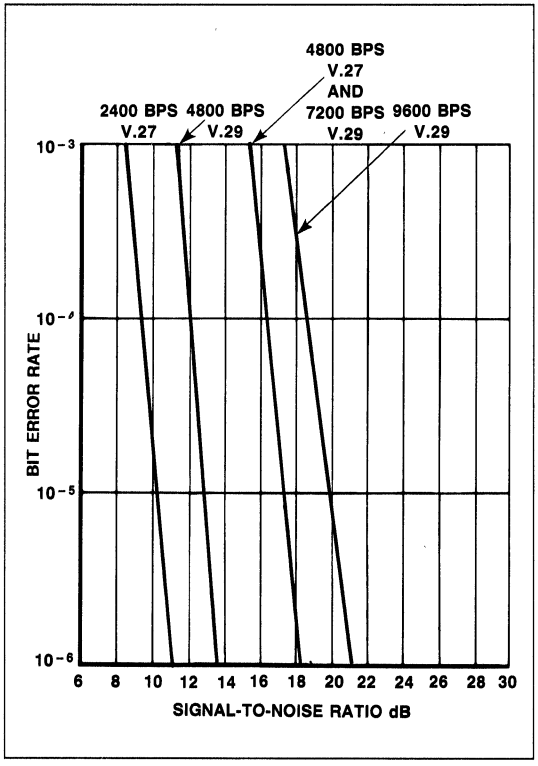
At 2400 bps, the modem exhibits a bit error rate of 10^{-6} or less with a signal-to-noise ratio of 12.5 dB in the presence of 15° peak-to-peak phase jitter at 150 Hz or with a signal-to-noise ratio of 15 dB in the presence of 30° peak-to-peak phase jitter at 120 Hz (scrambler inserted).

At 4800 bps (V.27 bis/ter), the modem exhibits a bit error rate of 10^{-6} or less with a signal-to-noise ratio of 10 dB in the presence of 15° peak-to-peak phase jitter at 60 Hz.

At 9600 bps, the modem exhibits a bit error rate of 10^{-6} or less with a signal-to-noise ratio of 23 dB in the presence of 10° peak-to-peak phase jitter at 60 Hz. The modem exhibits a bit error rate of 10^{-5} or less with a signal-to-noise ratio of 23 dB in the presence of 20° peak-to-peak phase jitter at 30 Hz.

7

An example of the BER performance capabilities is given in the following diagram:



Worst Case BER Performance (Back-to-Back)

GENERAL SPECIFICATIONS

Power

Voltage	Tolerance	Current (Max)
+5 Vdc	±5%	<700 mA
+12 Vdc	±5%	<20 mA
−12 Vdc	±5%	<80 mA

Note: All voltages must have ripple ≤0.1 volts peak-to-peak.

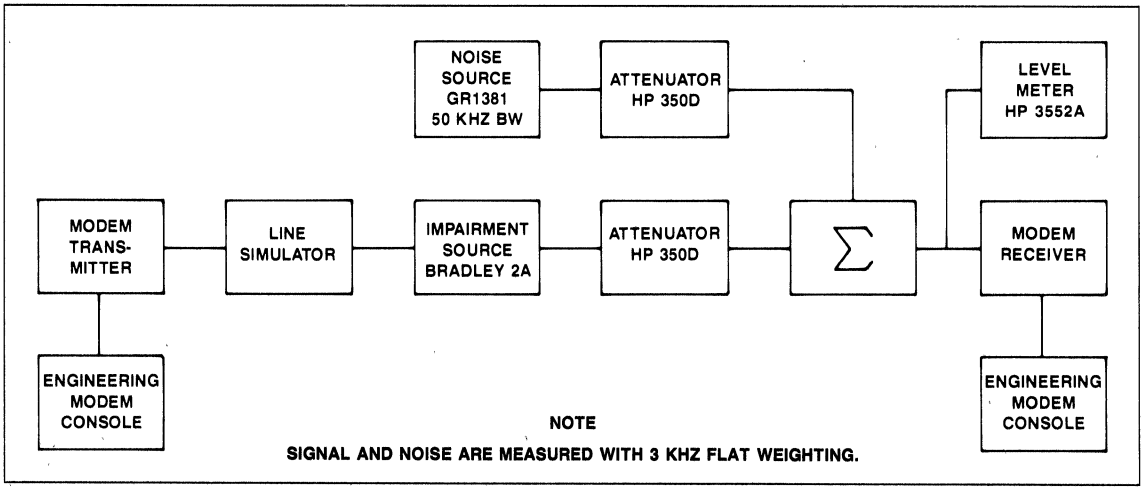
Environmental

Parameter	Specification
Temperature Operating Storage	 0°C to +60°C (32 to 140°F) −40°C to +80°C (−40 to 176°F) Stored in heat sealed antistatic bag and shipping container
Relative Humidity:	Up to 90% noncondensing, or a wet bulb temperature up to 35°C, whichever is less.

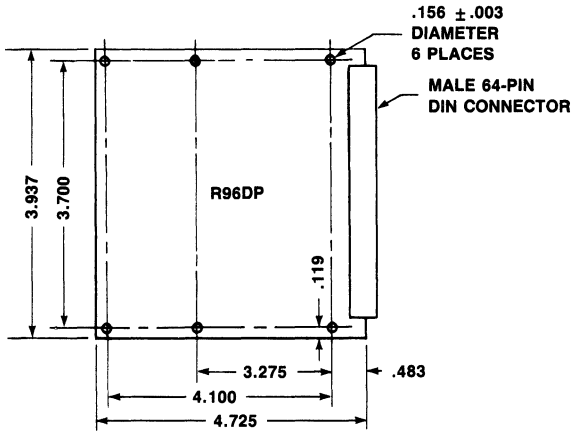
Mechanical

Parameter	Specification
Board Structure	Single PC board with single right angle header with 64 pins, Burndy (P196B32R00A00Z1) or equivalent mating connector.
Dimensions	Width—3.94 in. (100 mm) Length—4.72 in. (120 mm) Height—0.4 in. (10.2 mm)
Weight	Less than 3.6 oz. (100g)

The BER performance test set-up is shown in the following diagram:



BER Performance Test Set-up



Inches	MM
.119	3
.156	4
.483	12
3.275	83
3.700	94
3.937	100
4.100	104
4.725	120

R96DP Circuit Board Dimensions

7

Rockwell

R96FT
9600 BPS FAST TRAIN MODEM

PRELIMINARY

INTRODUCTION

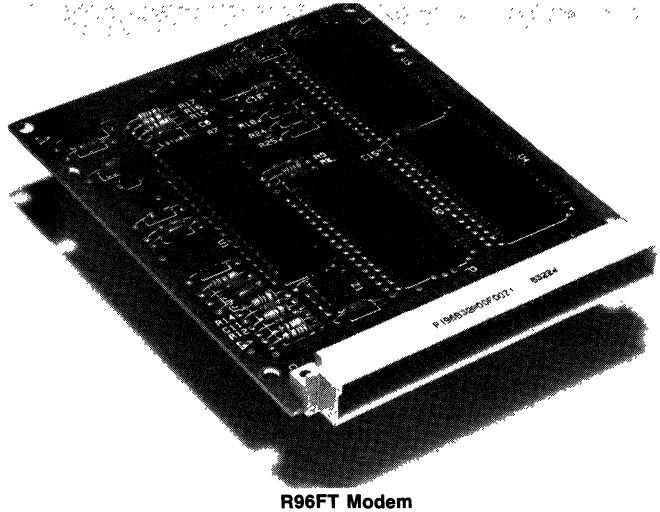
The Rockwell R96FT is a synchronous serial 9600 bps modem designed for multipoint and networking applications. The R96FT allows full-duplex operation over either four-wire dedicated unconditioned lines or half-duplex operation over the general switched telephone network.

Proprietary fast train configurations provide communication at 9600, 7200 and 4800 bps with the ability to train in thirty milliseconds. For applications requiring operation with international standards, fallback configurations compatible with CCITT recommendation V.29 at 9600, 7200 and 4800 bps are available. These configurations require 253 milliseconds to train.

The small size and low power consumption of the R96FT offer the user flexibility in formulating a 9600 bps modem design customized for specific packaging and functional requirements.

FEATURES

- User Compatibility:
  - — Proprietary Fast Train
  - — CCITT V.29
- Train on Data
- Full-Duplex (4-Wire)
- Half-Duplex (2-Wire)
- Programmable Tone Generation
- Dynamic Range –43 dBm to 0 dBm
- Diagnostic Capability
- Equalization:
  - — Automatic Adaptive
  - — Compromise Cable (Selectable)
  - — Compromise Link (Selectable)
- DTE Interface:
  - — Microprocessor Bus
  - — CCITT V.24 (RS-232-C Compatible)
- Loopbacks
  - — Local Analog (V.54 Loop 3)
  - — Remote Analog (Locally Activated)
  - — Remote Digital (Locally Activated V.54 Loop 2)
- Small Size
  - — 100 mm × 120mm (4.0 in. × 4.8 in.)
- Low Power Consumption
  - — 4 watts, typical
- Programmable Transmit Output Level
- TTL and CMOS Compatible



R96FT Modem

TECHNICAL SPECIFICATIONS

TRANSMITTER CARRIER FREQUENCY

The transmitter carrier frequency is 1700 Hz ±0.01% for all configurations.

TONE GENERATION

Under control of the host processor, the R96FT can generate voice band tones up to 4800 Hz with a resolution of 0.15 Hz and an accuracy of 0.01%. Tones over 3000 Hz are attenuated.

SIGNALING AND DATA RATES

Signaling/Data Rates

Parameter	Specification (±0.01%)
Signaling Rate Data Rate:	2400 Baud: 9600 bps, 7200 bps, 4800 bps

DATA ENCODING

The data stream is encoded per CCITT V.29. At 9600 bps, the data stream is divided in groups of four-bits (quad-bits) forming a 16-point structure. At 7200 bps, the data stream is divided into three bits (tribits) forming an 8-point structure. At 4800 bps, the data stream is divided into two bits (dibits) forming a 4-point structure. Signal structure, scrambler, and encoding are compatible with CCITT V.29.

EQUALIZERS

The R96FT provides equilization functions that improve performance when operating over low quality lines.

Cable Equalizers — Selectable compromise cable equalizers in the receiver and transmitter are provided to optimize performance over different lengths of non-loaded cable of 0.4 mm diameter.

Link Equalizers — Selectable compromise link equalizers in the receiver optimize performance over channels exhibiting severe amplitude and delay distortion. Two standards are provided: U.S. survey long and Japanese 3-link.

Automatic Adaptive Equalizer — An automatic adaptive T equalizer is provided in the receiver circuit.

TRANSMITTED DATA SPECTRUM

If the cable equalizer is not enabled, the transmitter spectrum is shaped by a square root of 20 percent raised cosine filter.

The out-of-band transmitter power limitations meet those specified by Part 68 of the FCC's rules.

SCRAMBLER/DESCRAMBLER

The R96FT incorporates a self-synchronizing scrambler/descrambler. This facility is in accordance with V.29.

RECEIVED SIGNAL FREQUENCY TOLERANCE

The receiver circuit of the R96FT can adapt to received frequency error of up to ±10 Hz with less than 0.2 dB degradation in BER performance.

During fast train polling, frequency offset must be less than ±2 Hz for successful training.

RECEIVE LEVEL

The receiver circuit of the modem satisfies all specified performance requirements for received line signal levels from 0 dBm to −43 dBm. The received line signal level is measured at the receiver analog input (RXA).

RECEIVE TIMING

The R96FT provides a data derived Receive Data Clock (RDCLK) output in the form of a squarewave. The low to high transitions of this output coincide with the centers of received data bits. The timing recovery circuit is capable of tracking a ±0.01% frequency error in the associated transmit timing source.

TRANSMIT LEVEL

The transmitter output level is accurate to ±1.0 dB and is programmable from −1.0 dBm to −15.0 dBm in 2 dB steps.

TRANSMIT TIMING

The R96FT provides a Transmit Data Clock (TDCLK) output with the following characteristics:

1. *Frequency.* Selected data rate of 9600, 7200, or 4800 Hz (±0.01%).
2. *Duty Cycle.* 50% ±1%

Input data presented on TXD is sampled by the R96FT at the low to high transition of TDCLK. Data on TXD must be stable for at least one microsecond prior to the rising edge of TDCLK and remain stable for at least one microsecond after the rising edge of TDCLK.

EXTERNAL TRANSMIT CLOCK

The transmitter data clock (TDCLK) can be phase locked to a signal on input XTCLK. This input signal must equal the desired data rate (or a submultiple of the data rate) ±0.01% with a duty cycle of 50% ±20%.

TRAIN ON DATA

When train on data is enabled (by setting a bit in the interface memory), the modem monitors the EQM signal. If EQM indicates a loss of equilization (i.e., BER approximately 10^{-3} for 0.5 seconds) the modem attempts to retrain on the data stream. Retrain is accomplished in three to fifteen seconds depending on line conditions.

TURN-ON SEQUENCE

Nine selectable turn-on sequences can be generated as follows:

Turn-On Sequences

No.	Configuration	CTS Response Time	Comments
1 2 3	FT/9600 FT/7200 FT/4800	30 30 30	Proprietory Fast Train
4 5 6	V.29/9600 V.29/7200 V.29/4800	253 253 253	CCITT Recommendation V.29
7 8 9	V.29/9600 V 29/7200 V.29/4800	458 458 458	V.29 preceded by echo protector tone for lines using echo suppressors*

*For short echo protector tone, subtract 155 msec. from values of CTS response time.

TURN-OFF SEQUENCE

The turn-off sequence consists of approximately 5 ms of remaining data and scrambled 1's.

CLAMPING

Received Data (RXD) is clamped to a constant mark (one) when the Received Line Signal Detector (RLSD) is off.

RESPONSE TIMES OF CLEAR-TO-SEND (CTS)

The time between the off-to-on transition of Request-To-Send (RTS) and the off-to-on transition of CTS is dictated by the length of the training sequence if used. These times are given in the Turn-On Sequences table. If training is not enabled, RTS/CTS delay is less than 2 baud times.

The time between the on-to-off transition of RTS and the on-to-off transition of CTS in the data state is a maximum of 2 baud times for all configurations.

RECEIVED LINE SIGNAL DETECTOR (RLSD)

For the fast train configurations, RLSD is activated by an increase of approximately 15 dB or greater in line power. The RLSD signal turns on at the end of the training sequence. If training is not detected at the receiver, the RLSD off-to-on response time is 32 ±5 ms. The RLSD signal is deactivated by a decrease of approximately 15 dB in line power. RLSD on-to-off response time is 10 ±3 ms.

For V.29 configurations RLSD is activated by line power above a preset threshold. The RLSD signal turns on at the end of the training sequence. If training is not detected at the receiver, the RLSD off-to-on response time is 15 ±10 ms. The RLSD on-to-off response time for V.29 is 30 ±9 ms. Response times are measured with a signal at least 3 dB above the actual RLSD on threshold or at least 5 dB below the actual RLSD off threshold.

Four threshold options are provided:

1. Greater than −43 dBm (RLSD on)
   Less than −48 dBm (RLSD off)
2. Greater than −33 dBm (RLSD on)
   Less than −38 dBm (RLSD off)
3. Greater than −26 dBm (RLSD on)
   Less than −31 dBm (RLSD off)
4. Greater than −16 dBm (RLSD on)
   Less than −21 dBm (RLSD off)

NOTE

Performance may be at a reduced level when the received signal is less than −43 dBm.

A minimum hysteresis action of 2 dB exists between the actual off-to-on and on-to-off transition levels. The threshold levels and hysteresis action are measured with a modulated carrier signal applied to the receiver's audio input (RXA).

MODES OF OPERATION

The R96FT is capable of being operated in either a serial or a parallel mode of operation.

SERIAL MODE

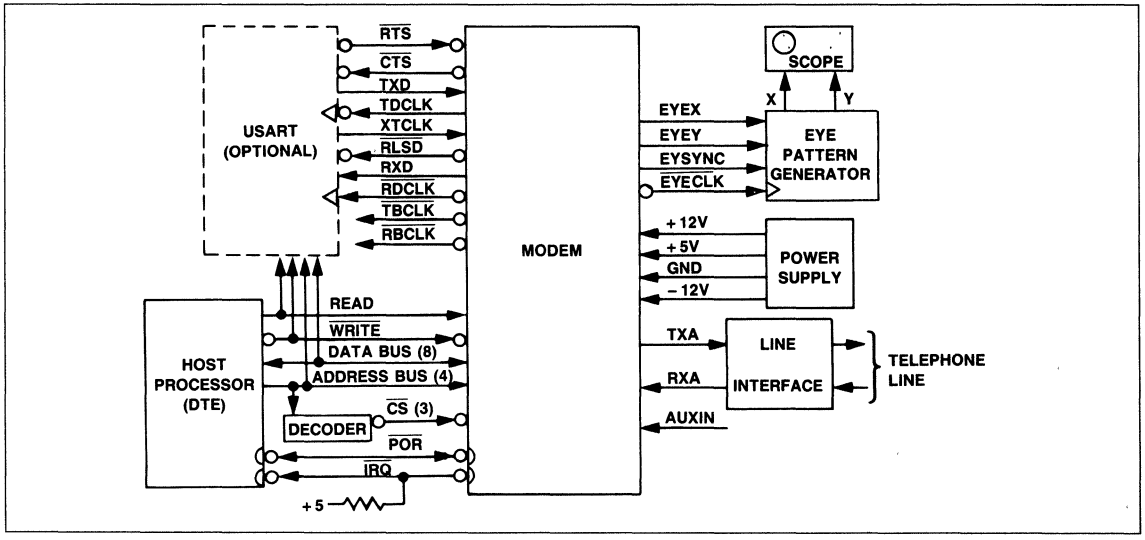
The serial mode uses standard V.24 (RS-232-C compatible) signals to transfer channel data. An optional USRT device (shown in the Functional Interconnect Diagram) illustrates this capability.

PARALLEL MODE

The R96FT has the capability of transferring channel data 8 bits at a time via the microprocessor bus in 9600 or 4800 bps configurations, 6 bits at a time in 7200 bps configuration.

MODE SELECTION

Selection of either the serial or parallel mode of operation is by means of a control bit. To enable the parallel mode, the control bit must be set to a 1. The modem automatically defaults to the serial mode at power-on. In either mode the R96FT is configured by the host processor via the microprocessor bus.



R96FT Functional Interconnect Diagram

INTERFACE CRITERIA

The modem interface comprises both hardware and software circuits. Hardware circuits are assigned to specific pins in a 64-pin DIN connector. Software circuits are assigned to specific bits in a 48-byte interface memory.

HARDWARE CIRCUITS

Signal names and descriptions of the hardware circuits, including the microprocessor interface, are listed in the R96FT Hardware Circuits table. In the table, the column titled 'Type' refers to designations found in the Hardware Circuit Characteristics. The microprocessor interface is designed to be directly compatible with an 8080 microprocessor. With the addition of a few external logic gates, it can be made compatible with 6500, 6800, or 68000 microprocessors.

R96FT Hardware Circuits

Name	Type	Pin No.	Description
A. OVERHEAD:			
Ground (A)	AGND	31C,32C	Analog Ground Return
Ground (D)	DGND	3C,8C,5A,10A	Digital Ground Return
+5 volts	PWR	19C,23C,26C,30C	+5 volt supply
+12 volts	PWR	15A	+12 volt supply
−12 volts	PWR	12A	−12 volt supply
$\overline{POR}$	I/OA	13C	Power-on-reset
B. MICROPROCESSOR INTERFACE:			
D7	I/OA	1C	
D6	I/OA	1A	
D5	I/OA	2C	
D4	I/OA	2A	Data Bus (8 Bits)
D3	I/OA	3A	
D2	I/OA	4C	
D1	I/OA	4A	
D0	I/OA	5C	
RS3	IA	6C	
RS2	IA	6A	Register Select (4 Bits)
RS1	IA	7C	
RS0	IA	7A	
$\overline{CS0}$	IA	10C	Chip Select Transmitter Device
$\overline{CS1}$	IA	9C	Chip Select Receiver Sample Rate Device
$\overline{CS2}$	IA	9A	Chip Select Receiver Baud Rate Device
$\overline{READ}$	IA	12C	Read Enable
$\overline{WRITE}$	IA	11A	Write Enable
$\overline{IRQ}$	OB	11C	Interrupt Request
C. V.24 INTERFACE:			
$\overline{RDCLK}$	OC	21A	Receive Data Clock
TDCLK	OC	23A	Transmit Data Clock
XTCLK	IB	22A	External Transmit Clock
$\overline{RTS}$	IB	25A	Request-to-Send
$\overline{CTS}$	OC	25C	Clear-to-Send
TXD	IB	24C	Transmitter Data
$\overline{RXD}$	OC	22C	Receiver Data
$\overline{RLSD}$	OC	24A	Received Line Signal Detector
D. ANCILLARY CIRCUITS:			
$\overline{RBCLK}$	OC	26A	Receiver Baud Clock
$\overline{TBCLK}$	OC	27C	Transmitter Baud Clock
		29A	(Future Use)
		18C	(Future Use)
E. ANALOG SIGNALS:			
TXA	AA	31A	Transmitter Analog Output
RXA	AB	32A	Receiver Analog Input
AUXIN	AC	30A	Auxiliary Analog Input

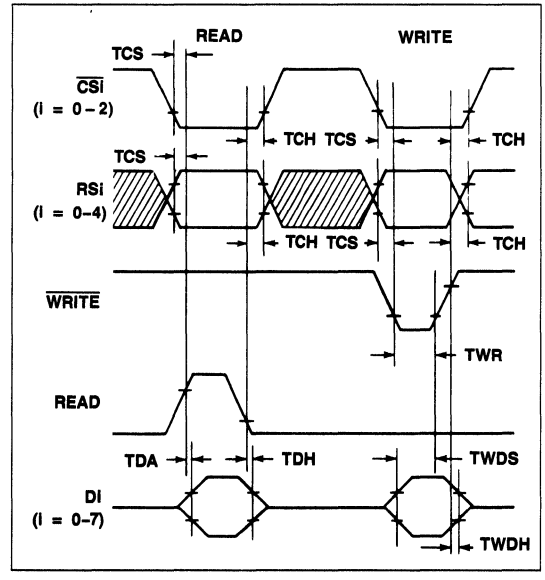
R96FT Hardware Circuits (Continued)

Name	Type	Pin No.	Description
F. DIAGNOSTIC:			
EYEX	OC	15C	Eye Pattern Data—X Axis
EYEY	OC	14A	Eye Pattern Data—Y Axis
$\overline{EYECLK}$	OA	14C	Eye Pattern Clock
EYESYNC	OA	13A	Eye Pattern Synchronizing Signal

EYE PATTERN GENERATION

The four hardware diagnostic circuits, identified in the preceding table, allow the user to generate and display an eye pattern. Circuits EYEX and EYEY serially present eye pattern data for the horizontal and vertical display inputs respectively. The 8-bit data words are shifted out most significant bit first, clocked by the rising edge of the $\overline{EYECLK}$ output. The EYESYNC output is provided for word synchronization. The falling edge of EYESYNC may be used to transfer the 8-bit word from the shift register to a holding register. Digital to analog conversion can then be performed for driving the X and Y inputs of an oscilloscope.

MICROPROCESSOR TIMING



Microprocessor Interface Timing Diagram

Critical Timing Requirements

Characteristic	Symbol	Min	Max	Units
$\overline{CSi}$, RSi setup time prior to Read or $\overline{Write}$	TCS	30	—	nsec
Data access time after Read	TDA	—	140	nsec
Data hold time after Read	TDH	10	50	nsec
CSi, RSi hold time after Read or $\overline{Write}$	TCH	10	—	nsec
Write data setup time	TWDS	75	—	nsec
Write data hold time	TWDH	10	—	nsec
Write strobe pulse width	TWR	75	—	nsec

7

HARDWARE CIRCUIT CHARACTERISTICS

Digital Interface Characteristics

Digital Interface Characteristics

Symbol	Parameter	Units	Input/Output Type IA	IB	IC	OA	OB	OC	I/O A	I/O B
V_{IH}	Input Voltage, High	V	2.0 Min.	2.0 Min.	2.0 Min.				2.0 Min.	5.25 Max. 2.0 Min.
V_{IL}	Input Voltage, Low	V	0.8 Max.	0.8 Max.	0.8 Max.				0.8 Max.	0.8 Max.
V_{OH}	Output Voltage, High	V				2.4 Min.[1]			2.4 Min.[1]	2.4 Min.[3]
V_{OL}	Output Voltage, Low	V				0.4 Max.[2]	0.4 Max.[2]	0.4 Max.[2]	0.4 Max.[2]	0.4 Max.[2]
I_{IN}	Input Current, Leakage	μA	±2.5 Max.						±2.5 Max.[4]	
I_{OH}	Output Current, High	mA				−0.1 Max.				
I_{OL}	Output Current, Low	mA				1.6 Max.	1.6 Max.	1.6 Max.		
I_L	Output Current, Leakage	μA					±10 Max.			
I_{PU}	Pull-up Current (Short Circuit)	μA		−240 Max. −10 Min.	−240 Max. −10 Min.			−240 Max. −10 Min.		−260 Max. −100 Min.
C_L	Capacitive Load	pF	5	5	20				10	40
C_D	Capacitive Drive	pF				100	100	100	100	100
	Circuit Type		TTL	TTL w/Pull-up	TTL w/Pull-up	TTL	Open-Drain	Open-Drain w/Pull-up	3-State Transceiver	Open-Drain w/Pull-up

Notes

1. I Load = −100 μA
2. I Load = 1.6 mA
3. I Load = −40 μA
4. V_{IN} = 0.4 to 2.4 Vdc, V_{CC} = 5.25 Vdc

Analog Interface Characteristics

Analog Interface Characteristics

Name	Type	Characteristics
TXA	AA	The transmitter output is a low impedance operational amplifier output. In order to match to 600 ohms, an external series resistor is required.
RXA	AB	The receiver input impedance is 63.4K ohms ±5%.
AUXIN	AC	The auxiliary analog input allows access to the transmitter for the purpose of interfacing with user provided equipment. Because this is a sampled data input, any signal above 4800 Hz will cause aliasing errors. The input impedance is 1K ohms, and the gain to transmitter output is −1 dB ±1 dB.

SOFTWARE CIRCUITS

The R96FT comprises three signal processor chips. Each of these chips contains 16 registers to which an external (host) microprocessor has access. Although these registers are within the modem, they may be addressed as part of the host processor's memory space. The host may read data out of or write data into these registers. The registers are referred to as interface memory. Registers in chip 1 update at half the modem sample rate (4800 bps). Registers in chip 0 and 2 update at the selected baud rate.

When information in these registers is being discussed, the format Y:Z:Q is used. The chip is specified by Y(0 − 2), the register by Z(0 − F), and the bit by Q(0 − 7, 0 = LSB).

Status Control Bits

The operation of the R96FT is affected by a number of software control inputs. These inputs are written into registers within the interface memory via the host microprocessor bus. Bits designated by an 'X' are "Don't Care" inputs that can be set to either 1 or 0. Modem operation is monitored by various software flags that are read from interface memory via the host microprocessor bus. All status and control bits are defined in the Interface Memory table. Bits designated by an 'R' are reserved for modem use only and must not be changed by the host.

RAM Data Access

The R96FT provides the user with access to much of the data stored in the modem's memories. This data is useful for performing certain diagnostic functions.

Two RAM access registers in chip 1 allow user access to RAM locations via the X word registers (1:3 and 1:2) and the Y word registers (1:1 and 1:0). Comparable registers in chip 2 provide access to chip 2 RAM locations. The access code stored in RAM ACCESS XS (1:5) selects the source of data for RAM DATA XSM and RAM DATA XSL (1:3 and 1:2). Similarly, the access code stored in RAM ACCESS YS (1:4) selects the source of data for RAM DATA YSM and RAM DATA YSL (1:1 and 1:0). Chip 2 registers are associated in the same way.

Reading of RAM data is performed by storing the necessary access codes in 1:5 and 1:4 (or 2:5 and 2:4), reading 1:0 (or 2:0) to reset the associated data available bit (1:E:0 or 2:E:0), then waiting for the data available bit to return to a one. Data is now valid and may be read from 1:3 through 1:0 (or 2:3 through 2:0). The contents of registers 2:3 and 2:1 are also available serially on outputs EYEX and EYEY, respectively, unless the IFIX bit (1:6:7) is set to a one. When IFIX is a one, EYEX and EYEY remain fixed on the rotated equalizer output.

RAM Access Codes

The RAM access codes defined in the following table allow the host processor to read diagnostic information within the modem.

RAM Access Codes

No.	Function	Chip	X Access	Y Access	Register
1	Received Signal Samples	1	E1	Not Used	2,3
2	Demodulator Output	1	C0	40	0,1,2,3
3	Low Pass Filter Output	1	F2	62	0,1,2,3
4	Average Energy	1	Not Used	25	0,1
5	AGC Gain Word	1	A1	Not Used	2,3
6	Equalizer Input	2	C0	40	0,1,2,3
7	Equalizer Tap Coefficients	2	80 – 9F	00-1F	0,1,2,3
8	Unrotated Equalizer Output	2	E1	61	0,1,2,3
9	Rotated Equalizer Output (Received Points)	2	E2	62	0,1,2,3
10	Decision Points (Ideal Data Points)	2	E8	68	0,1,2,3
11	Error	2	E4	64	0,1,2,3
12	Rotation Angle	2	A7	Not Used	2,3
13	Frequency Correction	2	A5	Not Used	2,3
14	EQM	2	BC	Not Used	2,3
15	Dual Point	2	E9	69	0,1,2,3

Receiver Interface Memory Chip 1 ($\overline{CS1}$)

Register \ Bit	7	6	5	4	3	2	1	0
F	R	R	R	R	R	R	R	R
E	RSIA	R	R	R	RSB	RSIE	R	RSDA
D	R	R	R	R	R	R	R	R
C	R	R	R	R	R	R	R	R
B	R	$\overline{PNDET}$	R	R	R	R	R	$\overline{CDET}$
A	R	R	R	R	R	R	R	R
9	R	R	R	R	R	R	R	R
8	R	R	R	R	R	R	R	R
7	RTH		DDIS	RPDM	R	R	R	R
6	IFIX	TOD	RECEIVER CONFIGURATION					
5	RAM ACCESS XS							
4	RAM ACCESS YS							
3	RAM DATA XSM							
2	RAM DATA XSL							
1	RAM DATA YSM							
0	RAM DATA YSL; RECEIVER DATA							
Register / Bit	7	6	5	4	3	2	1	0

NOTE
(X) indicates user available.
(R) indicates reserved for modem use only.

Transmitter Interface Memory Chip 0 ($\overline{CS0}$)

Register \ Bit	7	6	5	4	3	2	1	0
F	R	R	R	R	R	R	R	R
E	TIA	R	R	R	TSB	TIE	R	TBA
D	R	R	R	R	R	R	R	R
C	R	R	R	R	R	R	R	R
B	R	R	R	R	R	R	R	R
A	R	R	R	R	R	R	R	R
9	R	R	R	R	R	R	R	R
8	R	R	R	R	R	R	R	R
7	RTS	TTDIS	SDIS	MHLD	EPT	TPDM	XCEN	SEPT
6	TRANSMITTER CONFIGURATION							
5	X	X	CEQ		LAEN	LDEN	A3L	D3L
4	L3ACT	L4ACT	L4HG	TLVL			L2ACT	LCEN
3	FREQM							
2	FREQL							
1	R	R	R	R	R	R	R	R
0	TRANSMITTER DATA							
Register / Bit	7	6	5	4	3	2	1	0

NOTE
(X) indicates user available.
(R) indicates reserved for modem use only.

Receiver Interface Memory Chip 2 ($\overline{CS2}$)

Register \ Bit	7	6	5	4	3	2	1	0
F	R	R	R	R	R	R	R	R
E	RBIA	R	R	R	R	RBIE	R	RBDA
D	R	R	R	R	R	R	R	R
C	R	R	R	R	R	R	R	R
B	R	R	R	R	R	R	R	R
A	R	R	R	R	R	R	R	R
9	R	R	R	R	R	R	R	R
8	R	R	R	R	R	R	R	R
7	R	R	R	R	R	R	R	R
6	R	R	R	R	R	R	R	R
5	RAM ACCESS XB							
4	RAM ACCESS YB							
3	RAM DATA XBM							
2	RAM DATA XBL							
1	RAM DATA YBM							
0	RAM DATA YBL							
Register / Bit	7	6	5	4	3	2	1	0

NOTE
(X) indicates user available.
(R) indicates reserved for modem use only.

R96FT Interface Memory Definitions

<table>
<tr><th>Mnemonic</th><th>Name</th><th>Memory Location</th><th>Description</th></tr>
<tr><td>A3L</td><td>Amplitude 3-Link Select</td><td>0:5:1</td><td>See LAEN.</td></tr>
<tr><td>CEQ</td><td>Cable Equalizer Field</td><td>0:5:(4,5)</td><td>The CEQ Control field simultaneously controls amplitude compromise equalizers in both the transmit and receive paths. The following table lists the possible cable equalizer selection codes:

CEQ — Cable Length (0.4 mm diameter)
0 — 0.0
1 — 1.8 km
2 — 3.6 km
3 — 7.2 km</td></tr>
<tr><td>$\overline{\text{CDET}}$</td><td>Carrier Detector</td><td>1:B:0</td><td>When zero, status bit $\overline{\text{CDET}}$ indicates that passband energy is being detected, and that a training sequence is not in process. $\overline{\text{CDET}}$ goes to a zero at the start of the data state, and returns to a one at the end of the received signal</td></tr>
<tr><td>DDIS</td><td>Descramble Disable</td><td>1:7:5</td><td>When control bit DDIS is a one, the receiver descrambler circuit is removed from the data path.</td></tr>
<tr><td>D3L</td><td>Delay 3-Link Select</td><td>0:5:0</td><td>See LDEN.</td></tr>
<tr><td>EPT</td><td>Echo Protector Tone</td><td>0:7:3</td><td>When control bit EPT is a one, an unmodulated carrier is transmitted for 185 ms (optionally 30 ms) followed by 20 ms of no transmitted energy at the start of transmission. This option is available in the V.27 and V.29 Configurations, although it is not specified in the CCITT V.29 recommendation.</td></tr>
<tr><td>(None)</td><td>FREQL/FREQM</td><td>0:2:0–7,
0:3:0–7</td><td>The host processor conveys tone generation data to the transmitter by writing a 16-bit data word to the FREQL and FREQM registers in the interface memory space, as shown below:

FREQM Register (0:3)
<table><tr><th>Bit:</th><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr><tr><td>Data Word:</td><td>2^{15}</td><td>2^{14}</td><td>2^{13}</td><td>2^{12}</td><td>2^{11}</td><td>2^{10}</td><td>2^{9}</td><td>2^{8}</td></tr></table>
FREQL Register (0:2)
<table><tr><th>Bit:</th><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr><tr><td>Data Word:</td><td>2^{7}</td><td>2^{6}</td><td>2^{5}</td><td>2^{4}</td><td>2^{3}</td><td>2^{2}</td><td>2^{1}</td><td>2^{0}</td></tr></table>
The frequency number (N) determines the frequency (F) as follows:
F = (0.146486) (N) Hz ±0.01%

Hexadecimal frequency numbers (FREQL, FREQM) for commonly generated tones are given below:

Frequency (Hz) — FREQM — FREQL
462 — 0C — 52
1100 — 1D — 55
1650 — 2C — 00
1850 — 31 — 55
2100 — 38 — 00</td></tr>
<tr><td>IFIX</td><td>Eye Fix</td><td>1:6:7</td><td>When control bit IFIX is a one, the serial data on EYEX and EYEY reflect the rotated equalizer output and do not follow the data selected by RAM ACCESS XB and RAM ACCESS YB.</td></tr>
</table>

R96FT Interface Memory Definitions (Continued)

Mnemonic	Name	Memory Location	Description
LAEN	Link Amplitude Equalizer Enable	0:5:3	The link amplitude equalizer enable and select bits control an amplitude compromise equalizer in the receive path according to the following table: **LAEN** / **A3L** / **Curve Matched** 0 / X / No Equalizer 1 / 0 / U.S. Survey Long 1 / 1 / Japanese 3-Link
LCEN	Loop Clock Enable	0:4:0	When control bit LCEN is a one, the transmitter clock tracks the receiver clock.
LDEN	Link Delay Equalizer Enable	0:5:2	The link delay equalizer enable and select bits control a delay compromise equalizer in the receive path according to the following table: **LDEN** / **D3L** / **Curve Matched** 0 / X / No Equalizer 1 / 0 / U.S. Survey Long 1 / 1 / Japanese 3-Link
L2ACT	Remote Digital Loopback Activate	0:4:1	When control bit L2ACT is a one, the receiver digital output is connected to the transmitter digital input in accordance with CCITT recommendation V.54 loop 2
L3ACT	Local Analog Loopback Activate	0:4:7	When control bit L3ACT is a one, the transmitter analog output is coupled to the receiver analog input through an attenuator in accordance with CCITT recommendation V.54 loop 3.
L4ACT	Remote Analog Loopback Activate	0:4:6	When control bit L4ACT is a one, the receiver analog input is connected to the transmitter analog output through a variable gain amplifier in a manner similar to recommendation V.54 loop 4.
L4HG	Loop 4 High Gain	0:4:5	When control bit L4HG is a one, the loop 4 variable gain amplifier is set for +16 dB, and when at zero the gain is zero dB.
MHLD	Mark Hold	0:7:4	When control bit MHLD is a one, the transmitter input data stream is forced to all marks (ones).
$\overline{\text{PNDET}}$	Period N Detector	1:B:6	When status bit $\overline{\text{PNDET}}$ is a zero, it indicates a PN sequence has been detected. This bit sets to a one at the end of the PN sequence
(None)	RAM Access XB	2:5:0–7	Contains the RAM access code used in reading chip 2 RAM locations via word X (2:3 and 2:2)
(None)	RAM Access XS	1:5:0–7	Contains the RAM access code used in reading chip 1 RAM locations via word X (1:3 and 1:2).
(None)	RAM Access YB	2:4:0–7	Contains the RAM access code used in reading chip 2 RAM locations via word Y (2:1 and 2:0).
(None)	RAM Access YS	1:4:0–7	Contains the RAM access code used in reading chip 1 RAM locations via word Y (1:1 and 1:0).
(None)	RAM Data XBL	2:2:0–7	Least significant byte of 16-bit word X used in reading RAM locations in chip 2.
(None)	RAM Data XBM	2:3:0–7	Most significant byte of 16-bit word X used in reading RAM locations in chip 2.
(None)	RAM Data XSL	1:2:0–7	Least significant byte of 16-bit word X used in reading RAM locations in chip 1
(None)	RAM Data XSM	1:3:0–7	Most significant byte of 16-bit word X used in reading RAM locations in chip 1.

R96FT Interface Memory Definitions (Continued)

Mnemonic	Name	Memory Location	Description
(None)	RAM Data YBL	2:0:0–7	Least significant byte of 16-bit word Y used in reading RAM locations in chip 2.
(None)	RAM Data YBM	2:1:0–7	Most significant byte of 16-bit word Y used in reading RAM locations in chip 2.
(None)	RAM Data YSL	1:0:0–7	Least significant byte of 16-bit word Y used in reading RAM locations in chip 1. Shared by parallel data mode for presenting channel data to the host microprocessor bus. See 'Receiver Data.'
(None)	RAM Data YSM	1:1:0–7	Most significant byte of 16-bit word Y used in reading RAM locations in chip 1.
RBDA	Receiver Baud Data Available	2:E:0	Status bit RBDA goes to a one when the receiver writes data into register 2:0. The bit goes to a zero when the host processor reads data from register 2:0.
RBIA	Receiver Baud Interrupt Active	2:E:7	This status bit is a one whenever the receiver baud rate device is driving $\overline{IRQ}$ low.
RBIE	Receiver Baud Interrupt Enable	2:E:2	When the host processor writes a one in the RBIE control bit, the $\overline{IRQ}$ line of the hardware interface is driven to zero when status bit RBDA is a one.
(None)	Receiver Configuration	1:6:0–5	The host processor configures the receiver by writing a control code into the receiver configuration field in the interface memory space (see RSB). *Receiver Configuration Control Codes* Control codes for the modem receiver configuration are: **Configuration** — **Configuration Code (Hex)** FT/9600 — 1C FT/7200 — 1A FT/4800 — 19 V.29/9600 — 14 V.29/7200 — 12 V.29/4800 — 11
(None)	Receiver Data	1:0:0–7	The host processor obtains input data from the receiver in the parallel data mode by reading a data byte from the receiver data register. The data is divided on baud boundaries as is the transmitter data. When using receiver parallel data mode, the registers 1:3 through 1:0 can not be used for reading the chip 1 RAM.
RPDM	Receiver Parallel Data Mode	1:7:4	When control bit RPDM is a one, the receiver supplies data to the receiver data register (1:0) as well as to the hardware serial data output.
RSB	Receiver Setup Bit	1:E:3	When the host processor changes the receiver configuration (or the RTH field), the host processor must write a one in the RSB control bit. RSB goes to zero when the changes become effective.
RSDA	Receiver Sample Data Available	1:E:0	Status bit RSDA goes to a one when the receiver writes data to register 1:0. RSDA goes to a zero when the host processor reads data from register 1:0.
RSIA	Receiver Sample Interrupt Active	1:E:7	This status bit is a one whenever the receiver sample rate device is driving $\overline{IRQ}$ to zero.
RSIE	Receiver Sample Interrupt Enable	1:E:2	When the host processor writes a one in the RSIE control bit, the $\overline{IRQ}$ line of the hardware interface is driven to zero when status bit RSDA is at a one.
RTH	Receiver Threshold Field	1:7:6,7	The receiver energy detector threshold is set by the RTH field according to the following codes (see RSB): **RTH** — **RLSD On** — **RLSD Off** 0 — > –43 dBm — < –48 dBm 1 — > –33 dBm — < –38 dBm 2 — > –26 dBm — < –31 dBm 3 — > –16 dBm — < –21 dBm

R96FT Interface Memory Definitions (Continued)

Mnemonic	Name	Memory Location	Description
RTS	Request-to-Send	0:7:7	When control bit RTS goes to a one, the modem begins a transmit sequence. It continues to transmit until RTS is reset to zero, and the turn-off sequence has been completed. This input bit parallels the operation of the hardware RTS control input. These inputs are ORed by the modem.
SDIS	Scrambler Disable	0:7:5	When control bit SDIS is a one, the transmitter scrambler circuit is removed from the data path.
SEPT	Short Echo Protector Tone	0:7:0	When control bit SEPT is a one, the echo protector disable tone is 30 ms long rather than 185 ms.
TBA	Transmitter Buffer Available	0:E:0	This status bit resets to zero when the host processor writes data to transmitter data register 0:0. When the transmitter empties register 0:0, this bit sets to a one.
TIA	Transmitter Interrupt Active	0:E:7	This status bit is a one whenever the transmitter is driving $\overline{IRQ}$ to a zero.
TIE	Transmitter Interrupt Enable	0:E:2	When the host processor writes a one in control bit TIE, the $\overline{IRQ}$ line of the hardware interface is driven to zero when status bit TBA is at a one.
TLVL	Transmitter Level Field	0:4:2–4	The transmitter analog output level is determined by eight TLVL codes, as follows: **TLVL** — **Transmitter Analog Output*** 0 — −1 dBm ±1 dB 1 — −3 dBm ±1 dB 2 — −5 dBm ±1 dB 3 — −7 dBm ±1 dB 4 — −9 dBm ±1 dB 5 — −11 dBm ±1 dB 6 — −13 dBm ±1 dB 7 — −15 dBm ±1 dB *Each step above is a 2 dB change ±0.2 dB.
TOD	Train-on Data	1:6:6	When control bit TOD is a one, it enables the train-on-data algorithm to converge the equalizer if the signal quality degrades sufficiently. When TOD is a one, the modem still recognizes a training sequence and enters the force train state. A BER of approximately 10^{-3} for 0.5 seconds initiates train-on-data.
TPDM	Transmitter Parallel Data Mode	0:7:2	When control bit TPDM is a one, the transmitter accepts data for transmission from the transmitter data register (0:0) rather than the serial hardware data input.
(None)	Transmitter Configuration	0:6:0–7	The host processor configures the transmitter by writing a control byte into the transmitter configuration register in its interface memory space. *Transmitter Configuration Control Codes* Control codes for the modem transmitter configurations are: **Configuration** — **Configuration Code (Hex)** FT/9600 — 1C FT/7200 — 1A FT/4800 — 19 V.29/9600 — 14 V.29/7200 — 12 V.29/4800 — 11 Tone Transmit — 80

R96FT Interface Memory Definitions (Continued)

<table>
<tr><th>Mnemonic</th><th>Name</th><th>Memory Location</th><th>Description</th></tr>
<tr><td>(None)</td><td>Transmitter Data</td><td>0:0:0–7</td><td>The host processor conveys output data to the transmitter in the parallel mode by writing a data byte to the transmitter data register. The data is divided on baud boundaries, as follows:

NOTE

Data is transmitted bit zero first.

<table>
<tr><th rowspan="2">Configuration</th><th colspan="8">Bits</th></tr>
<tr><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr>
<tr><td>9600 bps</td><td colspan="4">Baud 1</td><td colspan="4">Baud 0</td></tr>
<tr><td>7200 bps</td><td colspan="2">Not Used</td><td colspan="2">Baud 1</td><td colspan="3">Baud 0</td></tr>
<tr><td>4800 bps</td><td colspan="2">Baud 3</td><td colspan="2">Baud 2</td><td colspan="2">Baud 1</td><td colspan="2">Baud 0</td></tr>
</table></td></tr>
<tr><td>TSB</td><td>Transmitter Setup Bit</td><td>0:E:3</td><td>When the host processor changes the transmitter configuration, the host must write a one in this control bit. TSB goes to a zero when the change becomes effective.</td></tr>
<tr><td>TTDIS</td><td>Transmitter Train Disable</td><td>0:7:6</td><td>When control bit TTDIS is a one, the transmitter does not generate a training sequence at the start of transmission. With training disabled, RTS and CTS delay is less than two baud times.</td></tr>
<tr><td>XCEN</td><td>External Clock Enable</td><td>0:7:1</td><td>When control bit XCEN is a zero, the transmitter timing is established by the external clock supplied at the hardware input XTCLK, pin 22A.</td></tr>
</table>

POWER-ON INITIALIZATION

When power is applied to the R96FT, a period of 50 to 350 ms is required for power supply settling. The power-on-reset signal (POR) remains low during this period. Approximately 10 ms after the low to high transition of POR, the modem is ready to be configured, and RTS may be activated. If the 5 Vdc power supply drops below 3.5 Vdc for more than 30 msec, the POR cycle is generated.

At POR time the modem defaults to the following configuration: fast train, 9600 bps, no echo protect tone, serial data mode, internal clock, cable equalizers disabled, link amplitude equalizer disabled, link delay equalizer disabled, transmitter output level set to -1 dBm ± 1 dB, interrupts disabled, receiver threshold set to -26 dBm, eye pattern selectable, and train-on-data disabled.

POR can be connected to a user supplied power-on-reset signal in a wire-or configuration. A low active pulse of 3 μsec or more applied to the POR pin causes the modem to reset. The modem is ready to be configured 10 msec after POR is removed.

PERFORMANCE

Whether functioning in V.29 or the proprietary fast train configurations, the R96FT provides the user with unexcelled high performance.

POLLING SUCCESS

In fast train configuration the modem achieves a 98% success rate over unconditioned 3002 lines for a signal-to-noise ratio of 26 dB.

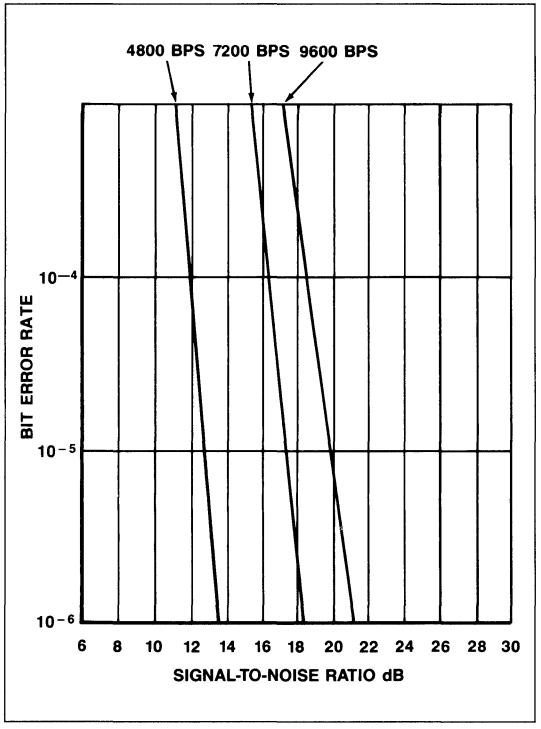
BIT ERROR RATES

The Bit Error Rate (BER) performance of the modem is specified for a test configuration conforming to that specified in CCITT recommendation V.56, except with regard to the placement of the filter used to bandlimit the white noise source. Bit error rates are measured at a received line signal level of -20 dBm as illustrated.

PHASE JITTER

At 9600 bps, the modem exhibits a bit error rate of 10^{-6} or less with a signal-to-noise ratio of 23 dB in the presence of 10° peak-to-peak phase jitter at 60 Hz. The modem exhibits a bit error rate of 10^{-5} or less with a signal-to-noise ratio of 23 dB in the presence of 20° peak-to-peak phase jitter at 30 Hz.

An example of the BER performance capabilities is given in the following diagram:



Worst Case BER Performance (Back-to-Back)

GENERAL SPECIFICATIONS

Power

Voltage	Tolerance	Current (Max)
+5 Vdc	±5%	<700 mA
+12 Vdc	±5%	<20 mA
−12 Vdc	±5%	<80 mA

Note: All voltages must have ripple ≤0 1 volts peak-to-peak

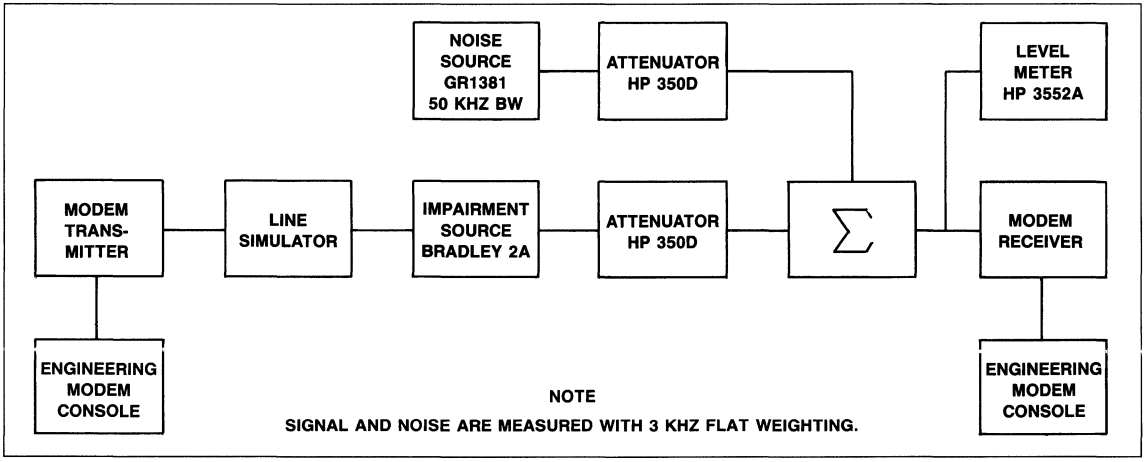
Environmental

Parameter	Specification
Temperature Operating Storage	 0°C to +60°C (32 to 140°F) −40°C to +80°C (−40 to 176°F) Stored in heat sealed antistatic bag and shipping container
Relative Humidity	Up to 90% noncondensing, or a wet bulb temperature up to 35°C, whichever is less

Mechanical

Parameter	Specification
Board Structure	Single PC board with single right angle header with 64 pins, Burndy P196B32R00A00Z1 or equivalent mating connector
Dimensions	Width—3.94 in. (100 mm) Length—4 72 in. (120 mm) Height—0.4 in (10 2 mm)
Weight	Less than 3.6 oz (100g)

The BER performance test set-up is shown in the following diagram:



BER Performance Test Set-up

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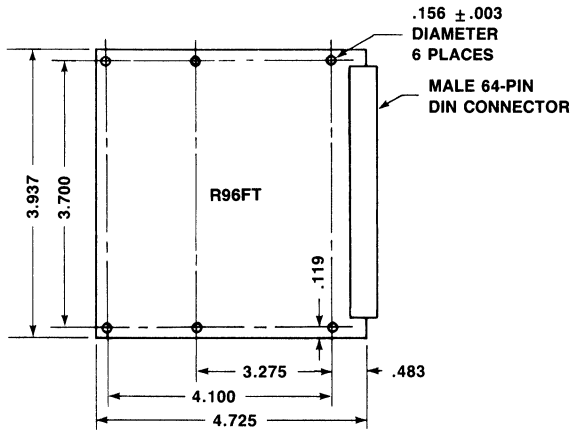


Inches	MM
.119	3
156	4
483	12
3.275	83
3.700	94
3.937	100
4 100	104
4.725	120

R96FT Circuit Board Dimensions

Rockwell

V96P/1
HIGH SPEED 9600 BPS MODEM

INTRODUCTION

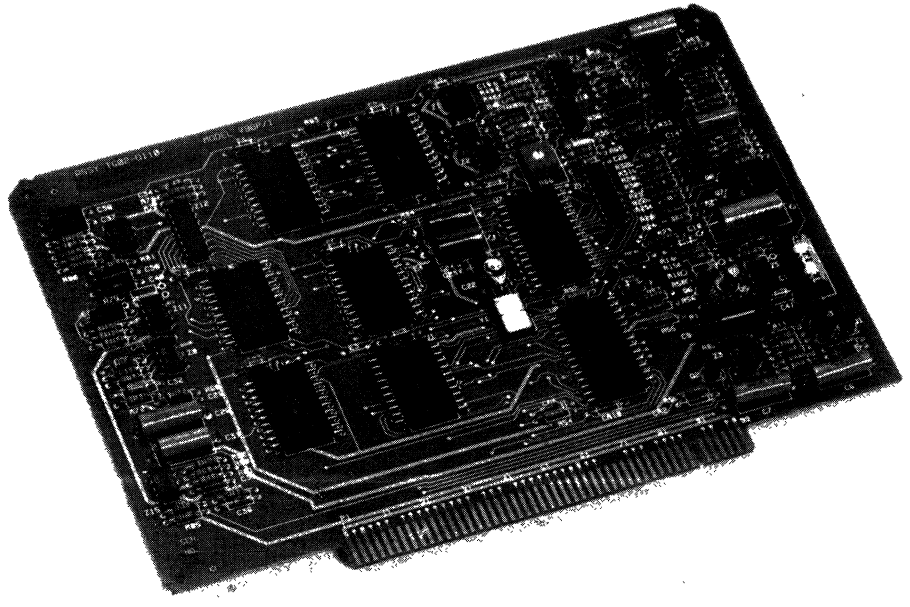
The Rockwell V96P/1 is a versatile, high performance, 9600 bps modem on a single printed circuit board. Being CCITT V.29 and V.27 compatible, the V96P/1 (with minimal interface circuitry) can operate on dedicated 2-wire or 4-wire half-duplex or 4-wire full-duplex lines. The V96P/1 can also operate in half-duplex on the general switched network.

Measuring approximately 9.2 inches (23.3 cm) by 6.3 inches (16.0 cm), the V96P/1 is the smallest full-feature 9600 bps modem that approaches data communication theoretical performance limits.

The V96P/1 meets the tolerances specified in the CCITT V.29, V.27 bis (alternate A), V.27 ter and FSK T.30 specifications. In addition, the V96P/1 can be configured to be functionally compatible with those enhanced specifications available in the Rockwell V96P, M96P, and V29P modem series.

FEATURES

- Single printed circuit card
- 9600/7200/4800/2400 bps modes
- Full-duplex or half-duplex
- Dedicated or general switched network lines operation
- Ultimate user flexibility:
  —CCITT V.29, V.27 ter, V.27 bis compatible
  —Also 300 bps binary signalling per CCITT T.30
- TTL compatibility
- Automatic adaptive equalizer
- Analog loopback test circuitry
- 0 to −45 dBm dynamic AGC
- LSI signal processing
- High reliability
- Low power consumption:
  —Typically 3.5 watts
- Automatic training sequence for receiver



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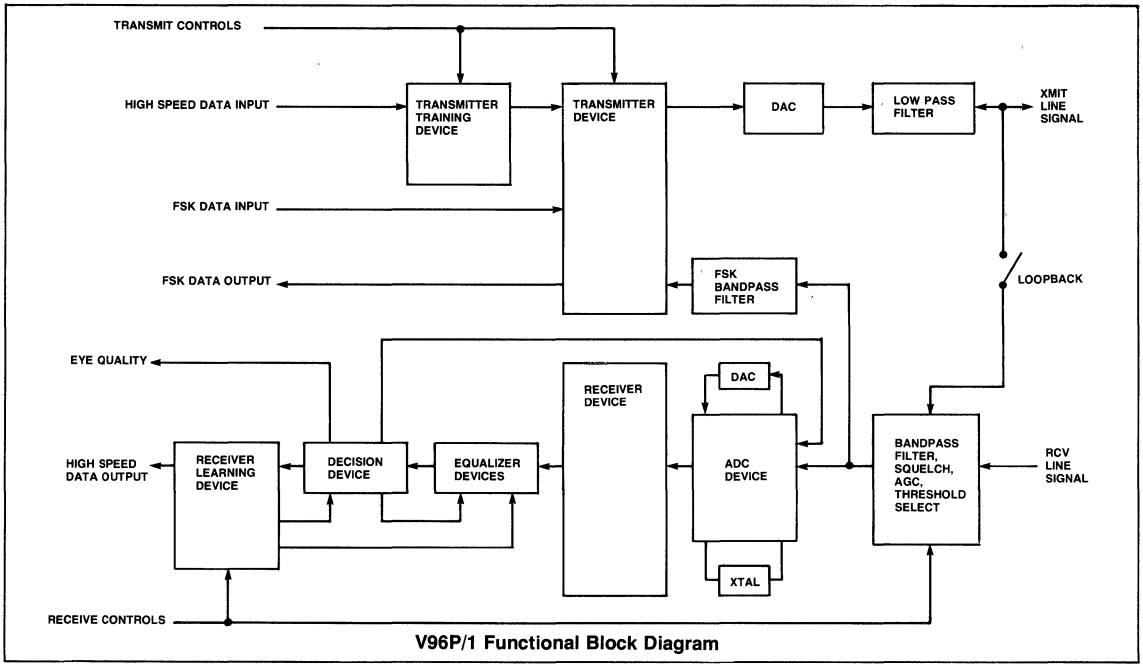
FUNCTIONAL SPECIFICATIONS



V96P/1 Functional Block Diagram

Transmit Carrier and Signalling Frequencies

Carrier Frequency Codex Compatible QAM:	1706.667 Hz ± 0.01%
Carrier Frequency V.29:	1700 Hz ± 0.01%
Carrier Frequency V.27:	1800 Hz ± 0.01%
Echo Suppression Frequencies:	2100 Hz ± 0.01%
	2025 Hz ± 0.01%
Signalling Frequencies of T.30:	1850 Hz ± 0.01%
	1650 Hz ± 0.01%
	1300 Hz ± 0.01%
	1100 Hz ± 0.01%

Received Signal Frequency Tolerance

The receiver can receive frequency errors of up to ± 10 Hz with less than a 0.2 dB degradation in Bit Error Rate performance.

Data Signalling and Modulation Rate

At 2400 baud:	
Signalling Rate—	2400 baud ± 0.01%
Data Rate—	9600 bps ± 0.01%
	7200 bps ± 0.01%
	4800 bps ± 0.01%
At 1600 baud:	
Signalling Rate—	1600 baud ± 0.01%
Data Rate—	4800 bps ± 0.01%
At 1200 baud:	
Signalling Rate—	1200 baud ± 0.01%
Data Rate—	2400 bps ± 0.01%

Transmitted Data Spectrum

At 2400 and 1600 baud the transmitted spectrum is shaped by approximately a square root of 50 percent raised cosine filter function. At 1200 baud the spectrum is shaped by approximately a square root of 90 percent raised cosine filter function.

The 2400 baud configurations require a line with typical 3002-C2 or M1020 characteristics over the frequency range from 450 Hz to 2950 Hz. The 1600 and 1200 baud rate configurations require a usable bandwidth from 950 Hz to 2650 Hz and 1150 Hz to 2450 Hz respectively.

Data Encoding

At 2400 baud the data stream is divided into groups of four bits (quadbits), three bits (tribits), or two bits (dibits). The data rate of 9600 bps, 7200 bps, or 4800 bps is selected by a 16-point, 8-point, or 4-point data structure, respectively. For 2400 baud operation, when V.29 configuration is selected, encoding of the quadbits, tribits, and dibits are per CCITT Recommendation V.29.

At 1600 baud the data stream is divided into groups of three bits (tribits). The data rate of 4800 bps may use either an 8-point QAM structure or 8-phase structure. Encoding of the tribits in the 8-phase structure are per CCITT Recommendation V.27 ter.

At 1200 baud the data stream is divided into groups of two bits (dibits). The data rate of 2400 bps uses a 4-phase data

structure. Encoding of the dibits may be per the fallback rate of CCITT Recommendation V.27 bis and ter (same as V.26A) or V26B depending on the selected configuration.

Turn-on, Turn-off Sequences

The V96P/1 turn-on sequences are compatible with CCITT Recommendations V.29, V.27 bis (alternate i), V.27 and Rockwell M96P modem specifications.

The turn-off sequences for all V.27 modes (except the 1600 baud rate manual V.27 mode) consists of 5 to 10 milliseconds of remaining data followed by continuous scrambled 1's followed by no transmission energy. The period of no transmission energy is provided by turning off the transmitter key signal for a recommended duration of 20 milliseconds.

The turn-off sequences for all non-V.27 modes consists of 4 to 7 milliseconds of remaining data followed by a period of no transmission energy.

Ready For Sending Response Times

The Ready For Sending response time to a Request To Send is determined by the configuration selected and its corresponding training time. In the following chart of configurations, the Training Times are shown in milliseconds. Note, however, that the 1600 baud manual CCITT configurations actually specify the synchronizing sequence timing per CCITT V.27 rather than the training time. Also note the following abbreviations.

ITC (1P–5P): Transmitter Configuration Inputs 1 through 5. These five bits establish the octal code shown where P1 and P2 are the most significant octal digit and P3 through P5 establish the least significant octal digit shown in the chart.

IRC (1P–5P): Receiver Configuration Inputs 1 through 5. These five bits establish the octal code shown where P1 and P2 are the most significant octal digit and P3 through P5 establish the least significant octal digit shown in the chart.

IRSS (1P–2P), ITSS (1P–2P): Receiver Signal Structure and Transmitter Signal Structure. Where P1 and P2 establish an octal code of 0, 1, 2, or 3. They define the signal structures as follows:

0 selects 16-point QAM
1 selects 8-point QAM
2 selects 4-point QAM
3 selects DPSK as:
8-phase at 1600 baud
4-phase at 1200 baud

Received Line Signal Detector (D109)

The time response of the Received Line Signal detector circuit (D109) is a function of the length of the received turn-on sequence. Circuit D109 turns on after synchronizing is completed and prior to user data appearing on the received output line. D109 turns on for approximately 2 milliseconds after the echo protect tone disappears in the V27EP configurations (Nos. 16, 18, 21, 23, 25, 29 and 32 in Table 1).

For non-CCITT configurations (Nos. 7, 8 and 9 in the table on page 4), D109 momentarily goes on at the beginning of the synchronizing sequence.

When no synchronizing signal is detected at the receiver, D109 turns on in 5 to 15 milliseconds for an applied signal greater than 3 dB above the turn-on threshold. If training is not enabled at the receiver, D109 turns on in 5 to 15 milliseconds.

Three threshold options are provided:

1) Greater than −43 dBm: D109 ON
   Less than −48 dBm: D109 OFF
2) Greater than −26 dBm: D109 ON
   Less than − 31 dBm: D109 OFF
3) Greater than −16 dBm: D109 ON
   Less than −21 dBm: D109 OFF

The three threshold options are controlled by the condition of the THRESH1 and THRESH2 control lines as indicated below.

dB Level	THRESH1	THRESH2
−43 dBm ON	Open Circuit	Open Circuit
−26 dBm ON	Open Circuit	0 to −0.5V
−16 dBm ON	0 to −0.5V	Open Circuit

When the received signal drops 5 dB below the D109 turn off threshold, D109 will turn off in 5 to 15 milliseconds. The condition of D109 between the selected turn-on and turn-off thresholds is not specified except that a hysteresis action of greater than 2 dB exists between the off-to-on and on-to-off transition levels.

Recommended circuits to control THRESH1 and THRESH2 input interface lines are shown in the diagrams on page 5 (A, B and C).

Bit Error Rates

The V96P/1 is thoroughly tested to guarantee Bit Error Rate (BER) performance under test conditions equivalent to CCITT Recommendation V.26. The test set-up used by Rockwell is shown in the BER Performance Test Set-up diagram.

The results of these BER performance tests are shown in the Typical Bit Error Rate Performance diagram.

7

V96P/1 Configurations

No.	Configuration	Transmitter ITC (1P-5P) (Octal Code)	Receiver IRC (1P-5P) (Octal Code)	Signal Structure IRSS (1P-2P) ITSS (1P-2P) (Octal Code)	Data Rate (bps)	Training Time (msec)	Carrier Frequency (Hz)
1.	2400 Baud DIAL	02	00	0,1,2		320	1706 2/3
2.	2400 Baud DIAL — T/2	02	01	0,1,2	9600	320	1706 2/3
3.	2400 Baud P-P	00	00	0,1,2	7200	280	1706 2/3
4.	2400 Baud P-P — T/2	00	01	0,1,2	4800	280	1706 2/3
5.	2400 Baud V29	01	02	0,1,2		233	1700
6.	2400 Baud V29 — T/2	01	03	0,1,2		233	1700
7.	1600 Baud DIAL, CCITT DIAL	22	22	1,3	4800	181	NOTE
8.	1600 Baud DIAL — T/2	22	36	1,3	4800	181	NOTE
9.	1600 Baud DIAL Slow	36	22	1,3	4800	221	NOTE
10.	1600 Baud P-P	20	20	1,3	4800	141	NOTE
11.	1600 Baud P-P — T/2	20	32	1,3	4800	141	NOTE
12.	1600 Baud Echo	34	34	1,3	4800	480	NOTE
13.	1600 Baud Manual CCITT	32	30	3	4800	20 (V.27 Sync Sequence)	1800
14.	1600 Baud Manual CCITT	30	30	3	4800	50 (V.27 Sync Sequence)	1800
15.	1600 Baud V27 DIAL/P-P	23	23	3	4800	708	1800
16.	1600 Baud V27 DIAL/P-P EP	27	23	3	4800	923	1800
17.	1600 Baud V27 DIAL/P-P — T/2	23	33	3	4800	708	1800
18.	1600 Baud V27 DIAL/P-P — T/2 EP	27	33	3	4800	923	1800
19.	1600 Baud V27 Multipoint — T/2	21	27	3	4800	50	1800
20.	1600 Baud V27 Resync (use with configuration 15)	21	25	3	4800	50	1800
21.	1600 Baud V27 Resync EP (use with configuration 16)	25	25	3	4800	265	1800
22.	1600 Baud V27 Resync — T/2 (use with configuration 17)	21	35	3	4800	50	1800
23.	1600 Baud V27 Resync — T/2 EP (use with configuration 18)	25	35	3	4800	265	1800
24.	1600 Baud V27 Echo	23	37	3	4800	708	1800
25.	1600 Baud V27 Echo EP	27	37	3	4800	923	1800
26.	1200 Baud DIAL	14	10	3	2400	170	1800
27.	1200 Baud P-P	10	10	3	2400	117	1800
28.	1200 Baud V27 DIAL/P-P	13	11	3	2400	943	1800
29.	1200 Baud V27 DIAL/P-P EP	17	11	3	2400	1158	1800
30.	1200 Baud V27 Multipoint	11	15	3	2400	66	1800
31.	1200 Baud V27 Resync (use with configuration 28)	11	13	3	2400	66	1800
32.	1200 Baud V27 Resync EP (use with configuration 29)	15	13	3	2400	281	1800

NOTE: Carrier frequency is 1706 2/3 Hz when IRSS (1P–2P) is a 1 (8-point).
Carrier frequency is 1800 Hz when IRSS (1P–2P) is a 3 (8-phase DPSK).

Data Scrambler Selection

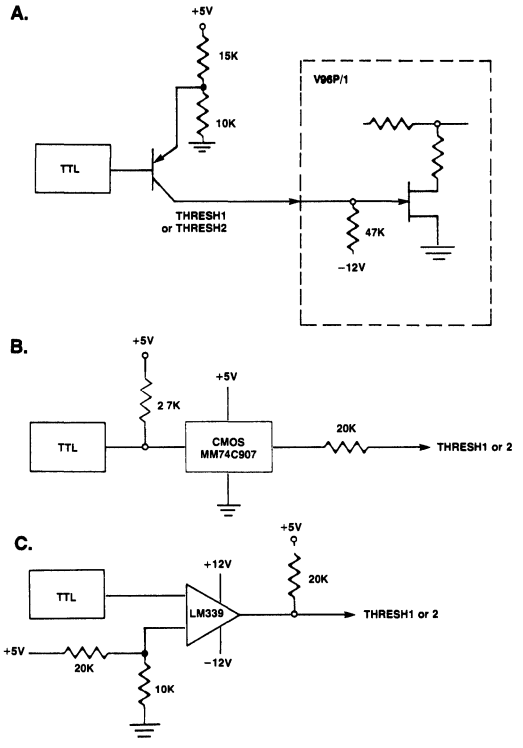
The V96P/1 makes available to the user one CCITT V.29 compatible scrambler, five different period 127 scramblers (and descramblers), and a no-scramble option. These scramblers provide data transmitted by the V96P/1 with the degree of randomness necessary to ensure the continued convergence of all adaptive processes at the receiver. The seven possible scrambler configurations that are user software selectable are:

- Period 127 cryptographic
- Period 127 synchronizing
- CCITT period 127 self-synchronizing (compatible with CCITT Recommendation V.29)
- Period 8,388,607 self-synchronizing (compatible with CCITT Recommendation V.29)
- Period 127 self-synchronizing with 8-bit protection
- CCITT period 127 self-synchronizing (compatible with CCITT Recommendations V.27 bis and ter)
- No scrambler

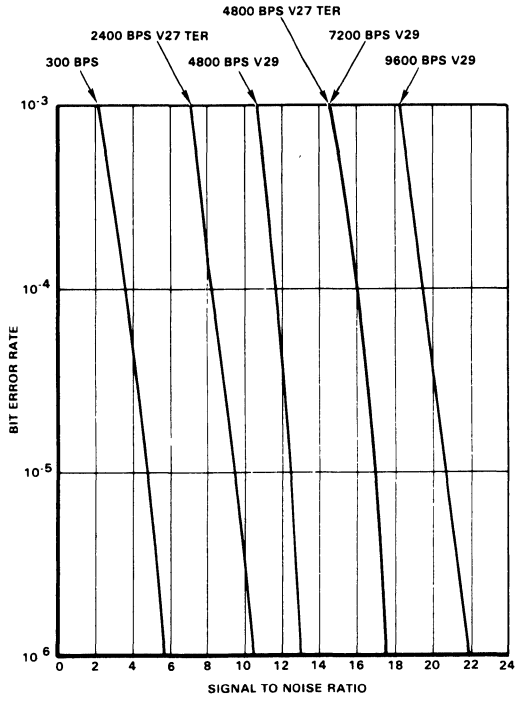
All scramblers can be used with all modem configurations listed in the above table except for the cryptographic scrambler which cannot be used in the CCITT V.29 configuration.

MODES OF OPERATION

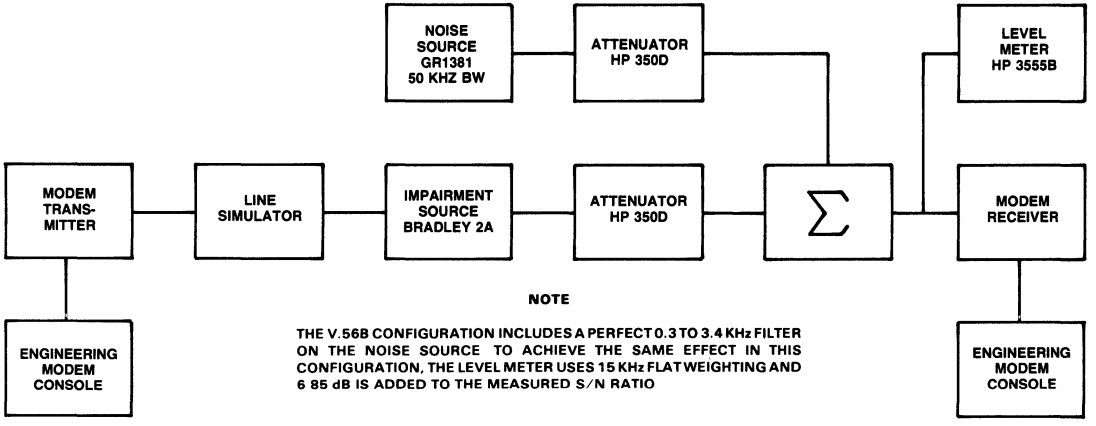
The V96P/1 has two modes of operation; a training mode and a data mode. In order for the receiver to correctly decode the transmitted data, the V96P/1 must detect the presence of a line signal, adjust the AGC, detect the presence of a training sequence, recover the baud timing of the transmitter, phase and frequency lock to the carrier associated with the received signal, and adapt the equalizer to the amplitude and delay characteristics of the channel. This learning process is accomplished most efficiently when the transmitter initiates a training sequence whenever a new transmitter-receiver



Suggested Interface Circuits for Controlling THRESH1 and THRESH2 Input Lines



Typical Bit Error Rate Performance



NOTE

THE V.56B CONFIGURATION INCLUDES A PERFECT 0.3 TO 3.4 KHz FILTER ON THE NOISE SOURCE TO ACHIEVE THE SAME EFFECT IN THIS CONFIGURATION, THE LEVEL METER USES 15 KHz FLAT WEIGHTING AND 6 85 dB IS ADDED TO THE MEASURED S/N RATIO

BER Performance Test Set-up

7

connection is made. It is possible to set up the receiver without a training sequence, but it is a manual mode requiring considerable user effort. In a training mode, an internal generated pattern is transmitted to the receiver to facilitate synchronization. During the training mode, the data input line to the receiver is ignored and the output line does not reflect the state of the data input.

In the data mode of operation, information on the data input is strobed by the transmitter signal element clock and transmitted to the receiver. The receiver demodulates and decodes the passband signal and outputs the recovered data on the output where it is then ready to be strobed by the receiver signal element clock.

Request To Send—Ready For Sending

To initiate transmitter operation in the data or training mode, the Request to Send input is brought high. If a training mode is not initiated, the Ready for Sending indicator goes high within one baud interval and data transmission commences.

The mode of the receiver is indicated by the data channel received line signal detector (D109). For data mode, D109 is high and the receiver training mode indicator is low.

If the receiver enters the training mode, the receiver training mode indicator goes high until the training mode is completed. When training is completed the receiver training mode indicator goes low and, if sufficient signal energy is present on the input line, D109 goes high, enabling the data mode.

Training Mode—Dial and Point-To-Point

For dial and point-to-point configurations, the V96P/1 receiver training is automatically initiated whenever a training sequence is detected in the received line signal. The training sequence consists of two phases: Phase 1 causes the training detector to turn on and also makes a course adjustment of the carrier frequency variable, which compensates for any frequency translation due to the channel; Phase 2 is used to converge the adaptive equalizer, which is part of the V96P/1 structure.

A short scrambler synchronization sequence follows Phase 2 and is used to generate the success indicator. In order for training to be successful, the incoming training sequence must have been generated by a similarly configured transmitter using a compatible training sequence.

At the receiver, detection of a training sequence requires that there be sufficient signal energy and that the receiver's carrier frequency variable be within 30 Hz of nominal.

Training Resync (V.27 bis/ter Turnaround)

In a 2-wire half-duplex data communication system, data can be transmitted in only one direction at any given instant. Therefore, the modems at the local and remote sites are required to interchange their roles as the receiver and the transmitter, respectively. This turnaround operation requires constant resynchronization to meet CCITT Recommendations for V.27 bis/ter.

The resync configurations are used for reacquiring synchronization in turnaround operation without having to go through the normal long training sequence. The resync training sequences are relatively short and are used for recovering carrier phase, symbol timing and achieving equalizer convergence without resetting carrier frequency and equalizer taps.

Training Mode—Multipoint

In the V96P/1 modem, two multipoint configurations are provided for 4-wire circuits conforming to M1020 which permit short training sequences. In these configurations, the first train signal must be high to process the short training sequences; otherwise the receiver will ignore the training sequence and enter directly into the data mode. The receiver will enter into the training mode if the first train signal is high and there is sufficient signal energy.

For 4-wire circuits which are worse than M1020 and for 2-wire circuits, a long training sequence should be used rather than the multipoint configuration. These training sequences require that the receiver be in the proper dial/point-to-point configuration.

Training Mode—Manual

The V96P/1 modem includes two manual configurations in which the remote modem need not transmit a special training sequence to the local receiver. In these configurations, the equalizer tap coefficients for the local receiver must be initialized from an external source. The tap coefficients may be initialized by controlling three input terms—ICR, ICI and ICLCP—in synchronization with the Baud Rate Clock.

In order to operate the modem in the manual configurations, both the transmitter and receiver must be set according to the code shown in Table 1 Modem Configuration. Manual configuration code octal 30 has a longer synchronizing sequence than configuration code octal 32, but both synchronizing sequences conform to the CCITT Recommendation V.27. However, neither sequence is of sufficient duration to aid in training the receiver.

Receiver Operation During Loss of Line Signal

When there is no line signal present, all receiver update relating to the equalizer, carrier frequency variable and baud timing are inhibited and the current values of the equalizer taps and the carrier frequency variable are retained.

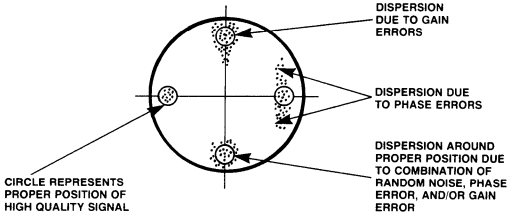
DATA QUALITY

The receiver generates an Eye Quality Monitor (EQM) signal that can be used to determine the equivalent Gaussian signal to noise ratio of the overall system within approximately ±

2 db. Eye quality is determined by calculating the difference between the received signal point after equalization and the transmitted or expected signal point. The receiver output DEQ2P is a filtered version of this error signal. It is a serial word clocked by the system bit clock (345.6 kHz or 230.4 kHz, depending on baud rate). Output signal DQGTP is a gating signal which delineates the eight MSB's of DEQ2P. The use and interpretation of these binary signals are quite complex and are dependent on the application and the signal structure. The user can derive a meaningful interpretation of the EQM readings by monitoring them while testing the modem against his performance criteria.

Visual Display of Eye Pattern

A visual indication of the modem's performance can be obtained by displaying the received baseband signal structure after equalization. This is done by converting the eight MSB's of the real and imaginary equalized signal points available on DRERP and DIERP to analog voltages which are then used to drive the horizontal and vertical sweeps of an oscilloscope. The resultant display will be a symmetrical dot pattern of 16 points, 8 points, or 4 points which is a time representation of the received baseband signal. Any uncompensated distortion over the transmission path will cause each dot in the pattern to enlarge or otherwise show distortion. A typical visual eye pattern of a 4-point display is shown in the following diagram.



Typical Eye Pattern

Success Indicator

A second data quality indicator is provided for in all configurations except the 1200 baud non-V.27 modes. This signal provides a rough indication that the training has been successful and that data will be properly received. This "success" output (DSUCP) will go high during the last one to twenty milliseconds of receiver training, provided training has been successful. During the data mode (DRTMP low and D109 high), DSUCP will go high whenever 15 consecutive data marks or spaces are decoded at the receiver data output.

ADDITIONAL CAPABILITIES

The V96P/1 provides many additional capabilities germane to data communication system design and implementation. Capabilities such as local loopback, tone generation and detection, external clock facilities, and 300 bps FSK operation are briefly described in the following paragraphs.

Local Loopback Capability

A local loopback option is available for all half duplex and full duplex modem configurations. The Local Loopback Command (ILB) connects the transmitter's output through a buffer amplifier to the receiver input, thereby allowing a check of the local modem. The ILB command squelches the input to the receiver and loops the analog signal from the transmitter to the receiver input.

An internal pattern generator is also incorporated in the modem which can be used when no modem test set is available.

Tone Generation And Detection

The transmitter can be used to transmit single frequency tones for disabling echo suppressors or for system signaling. Tones that can be transmitted (selected through software control) are: 1100 Hz, 1300 Hz, 1650 Hz, 1850 Hz, 2025 Hz, and 2100 Hz. Other tones are also possible and the carrier frequency can be altered by selection of values for a binary bit stream.

External Data Clock

The data input to the transmitter can be clocked from an external source when the external clock is used as a reference input to the data clock's phase locked loop. By applying an external clock the reference input will cause the transmitter data clock to track the frequency and phase of the reference. The frequency of the reference clock must be within 100 ppm of nominal in order for the receiver's baud timing to properly track that of the transmitter. The reference clock can be equal to the nominal data clock frequency or be a subharmonic of it as long as the frequency tolerance is adhered to.

300 bps FSK Modem Operation

A CCITT T 30 compatible 300 bps FSK modem having characteristics of the CCITT V.21 channel 2 modulation system can also be configured. The FSK modem is capable of generating the 1100, 1300, 1650 and 1850 Hz tones.

7

SPECIFICATIONS

V96P/1 Specifications

DC Voltages			
Voltage	**Tolerance**	**Current (Typical)**	**Current (Max)**
+ 5 volt	±5%	135 ma	<200 ma
+12 volt	±5%	40 ma	< 70 ma
−12 volt	±5%	175 ma	<230 ma
NOTE: All voltages must have ripple ≤0.1 volts peak-to-peak.			

Environment	
Temperature:	Operating: 0°C to +60°C (32 to 140°F) Storage: −40°C to +80°C (−40 to 176°F) (Stored in heat sealed antistatic bag and shipping container)
Relative Humidity:	Up to 90% noncondensing, or a wet bulb temperature up to 35°C, whichever is less.

Mechanical	
Board Structure:	Single PC board with edge connector
Mating Connector:	100 pin, edge connector, two sided, with 0.1 in (2.54 cm) centers. Recommended Viking 3VH50/IJND5 or equivalent mating connector.
Dimensions:	Width—9.188 in (23.338 cm) Depth—6.288 in (15.972 cm)
Weight:	Less than 0.45 lbs (0.20 kg)

Rockwell

R48DP
4800 BPS DATA PUMP MODEM

INTRODUCTION

The Rockwell R48DP is a synchronous serial 4800 bps modem designed for full-duplex operation over either four-wire dedicated unconditioned lines or half-duplex operation over the general switched telephone network.

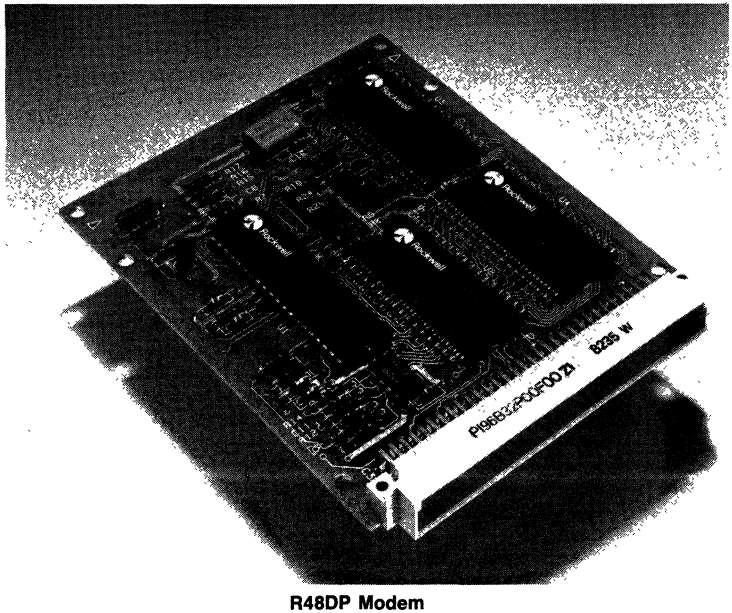
The modem satisfies telecommunications requirements specified in CCITT Recommendations V.27 bis/ter.

The small size and low power consumption of the modem offer the user flexibility in creating a 4800 bps modem design customized for specific packaging and functional requirements.

The modem is capable of operating at 4800 and 2400 bps.

FEATURES

- User Compatibility:
  - — CCITT V.27 bis/ter
- Full-Duplex (4-Wire)
- Half-Duplex
- Programmable Tone Generation
- Dynamic Range –43 dBm to 0 dBm
- Diagnostic Capability
- Equalization:
  - — Automatic Adaptive
  - — Compromise Cable (Selectable)
  - — Compromise Link (Selectable)
- DTE Interface:
  - — Microprocessor Bus
  - — CCITT V.24 (RS-232-C Compatible)
- Loopbacks
  - — Local Analog (V.54 Loop 3)
  - — Remote Analog (Locally Activated)
  - — Remote Digital (Locally Activated V.54 Loop 2)
- Small Size — 100 mm × 120mm (4.0 × 4.8 inches)
- Low Power Consumption (3 watts, typical)
- Programmable Transmit Output Level
- TTL and CMOS Compatible



R48DP Modem

7

TECHNICAL SPECIFICATIONS

TRANSMITTER CARRIER FREQUENCIES

Transmitter Carrier Frequencies

Function	Frequency (Hz ±0.01%)
V.27 bis/ter Carrier	1800

TONE GENERATION

Under control of the host processor, the R48DP can generate voice band tones up to 4800 Hz with a resolution of 0.15 Hz and an accuracy of 0.01%. Tones over 3000 Hz are attenuated.

SIGNALING AND DATA RATES

Signaling/Data Rates

Parameter	Specification (±0.01%)
Signaling Rate: Data Rate:	1600 Baud 4800 bps
Signaling Rate: Data Rate:	1200 Baud 2400 bps

DATA ENCODING

At 1600 baud, the 4800 bps data stream is encoded into tribits per CCITT V.27 bis/ter.

At 1200 baud, the 2400 bps data stream is encoded into dibits per CCITT V.27 bis/ter.

EQUALIZERS

The R48DP provides equalization functions that improve performance when operating over low quality lines.

Cable Equalizers — Selectable compromise cable equalizers in the receiver and transmitter are provided to optimize performance over different lengths of non-loaded cable of 0.4 mm diameter.

Link Equalizers — Selectable compromise link equalizers in the receiver optimize performance over channels exhibiting severe amplitude and delay distortion. Two standards are provided: U.S. survey long and Japanese 3-link.

Automatic Adaptive Equalizer — An automatic adaptive equalizer is provided in the receiver circuit. The equalizer can be configured as either a T or a T/2 equalizer.

TRANSMITTED DATA SPECTRUM

If the cable equalizer is not enabled, the transmitter spectrum is shaped by the following raised cosine filter functions:

1. *1200 Baud.* Square root of 90 percent
2. *1600 Baud.* Square root of 50 percent

The out-of-band transmitter power limitations meet those specified by Part 68 of the FCC's rules, and typically exceed the requirements of foreign telephone regulatory bodies.

SCRAMBLER/DESCRAMBLER

The R48DP incorporates a self-synchronizing scrambler/descrambler. This facility is in accordance with V.27 bis/ter.

RECEIVED SIGNAL FREQUENCY TOLERANCE

The receiver circuit of the R48DP can adapt to received frequency error of up to ± 10 Hz with less than 0.2 dB degradation in BER performance.

RECEIVE LEVEL

The receiver circuit of the modem satisfies all specified performance requirements for received line signal levels from 0 dBm to –43 dBm. The received line signal level is measured at the receiver analog input (RXA).

RECEIVE TIMING

The R48DP provides a data derived Receive Data Clock (RDCLK) output in the form of a squarewave. The low to high transitions of this output coincide with the centers of received data bits. The timing recovery circuit is capable of tracking a ±0.01% frequency error in the associated transmit timing source.

TRANSMIT LEVEL

The transmitter output level is accurate to ±1.0 dB and is programmable from –1.0 dBm to –15.0 dBm in 2 dB steps.

TRANSMIT TIMING

The R48DP provides a Transmit Data Clock (TDCLK) output with the following characteristics:

1. *Frequency.* Selected data rate of 4800 or 2400 Hz (±0.01%).
2. *Duty Cycle.* 50% ±1%

Input data presented on TXD is sampled by the R48DP at the low to high transition of TDCLK. Data on TXD must be stable for at least one microsecond prior to the rising edge of TDCLK and remain stable for at least one microsecond after the rising edge of TDCLK.

EXTERNAL TRANSMIT CLOCK

The transmitter data clock (TDCLK) can be phase locked to a signal on input XTCLK. This input signal must equal the desired data rate ±0.01% with a duty cycle of 50% ±20%.

TRAIN ON DATA

When train on data is enabled, the receiver trains on data in less than 3.5 seconds.

TURN-ON SEQUENCE

A total of 8 selectable turn-on sequences can be generated as defined in the following table:

Turn-On Sequences

No.	V.27 bis/ter	CTS Response Time (milliseconds)	Comments
1	4800 bps long	708	
2	2400 bps long	943	
3	4800 bps short	50	
4	2400 bps short	67	
5	4800 bps long	913	Preceded by Echo Protector Tone for lines using echo supressors*
6	2400 bps long	1148	
7	4800 bps short	255	
8	2400 bps short	272	

*For short echo protector tone, subtract 155 ms from values of CTS response time.

TURN-OFF SEQUENCE

For V.27 ter, the turn-off sequence consists of approximately 10 ms of remaining data and scrambled ones at 1200 baud or approximately 7 ms of data and scrambled ones at 1600 baud followed by a 20 ms period of no transmitted energy.

CLAMPING

Received Data (RXD) is clamped to a constant mark (one) whenever the Received Line Signal Detector (RLSD) is off.

RESPONSE TIMES OF CLEAR-TO-SEND (CTS)

The time between the off-to-on transition of Request-To-Send (RTS) and the off-to-on transition of CTS is dictated by the length of the training sequence and the echo suppressor disable tone, if used. These times are listed in the Turn-On Sequences table. If training is not enabled RTS/CTS delay is less than 2 baud times.

The time between the on-to-off transition of RTS and the on-to-off transition of CTS in the data state is a maximum of 2 baud times for all configurations.

RECEIVED LINE SIGNAL DETECTOR (RLSD)

For V.27 bis/ter, RLSD turns on at the end of the training sequence. If training is not detected at the receiver, the RLSD off-to-on response time is 15 ±10 ms. The RLSD on-to-off response time for V.27 is 10 ±5 ms. Response times are measured with a signal at least 3 dB above the actual RLSD on threshold or at least 5 dB below the actual RLSD off threshold.

The RLSD on-to-off response time ensures that all valid data bits have appeared on RXD.

Four threshold options are provided:

1. Greater than −43 dBm (RLSD on)
   Less than −48 dBm (RLSD off)
2. Greater than −33 dBm (RLSD on)
   Less than −38 dBm (RLSD off)
3. Greater than −26 dBm (RLSD on)
   Less than −31 dBm (RLSD off)
4. Greater than −16 dBm (RLSD on)
   Less than −21 dBm (RLSD off)

NOTE

Performance may be at a reduced level when the received signal is less than −43 dBm.

A minimum hysteresis action of 2 dB exists between the actual off-to-on and on-to-off transition levels. The threshold levels and hysteresis action are measured with an unmodulated carrier signal applied to the receiver's audio input (RXA).

MODES OF OPERATION

The R48DP is capable of being operated in either a serial or a parallel mode of operation.

SERIAL MODE

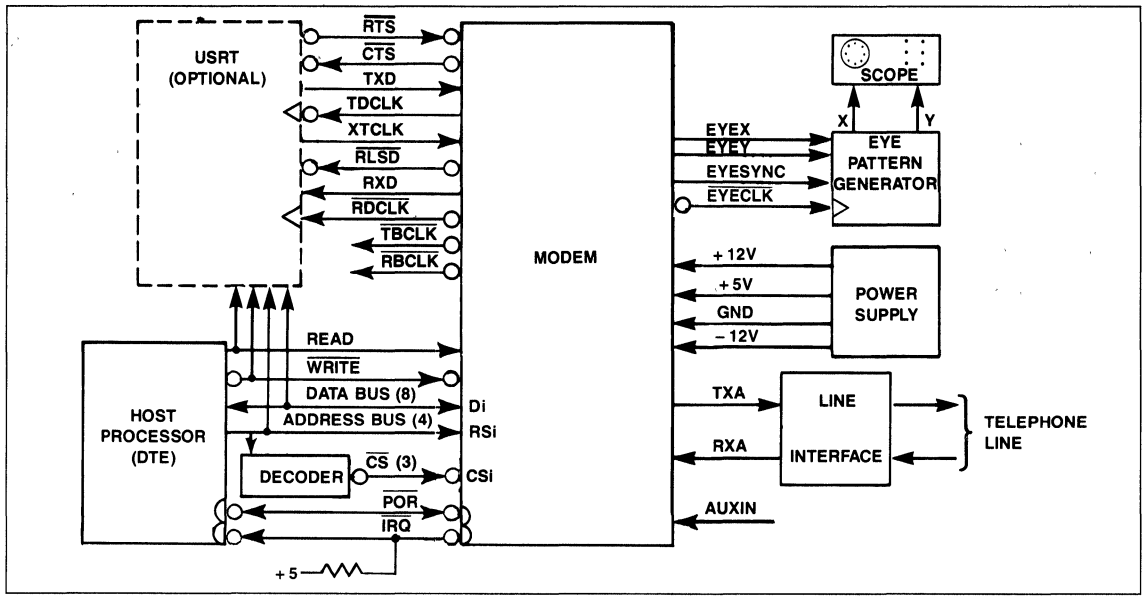
The serial mode uses standard V.24 (RS-232-C compatible) signals to transfer channel data. An optional USRT device (shown in the Functional Interconnect Diagram) illustrates this capability.

PARALLEL MODE

The R48DP has the capability of transferring channel data up to eight bits at a time via the microprocessor bus.

MODE SELECTION

Selection of either the serial or parallel mode of operation is by means of a control bit. To enable the parallel mode, the control bit must be set to a 1. The modem automatically defaults to the serial mode at power-on. In either mode the R48DP is configured by the host processor via the microprocessor bus.



R48DP Functional Interconnect Diagram

INTERFACE CRITERIA

The modem interface comprises both hardware and software circuits. Hardware circuits are assigned to specific pins in a 64-pin DIN connector. Software circuits are assigned to specific bits in a 48-byte interface memory.

HARDWARE CIRCUITS

Signal names and descriptions of the hardware circuits, including the microprocessor interface, are listed in the R48DP Hardware Circuits table. In the table, the column titled 'Type' refers to designations found in the Hardware Circuit Characteristics. The microprocessor interface is designed to be directly compatible with an 8080 microprocessor. With the addition of a few external logic gates, it can be made compatible with 6500, 6800, or 68000 microprocessors.

R48DP Hardware Circuits

Name	Type	Pin No.	Description
A. OVERHEAD:			
Ground (A)	AGND	31C,32C	Analog Ground Return
Ground (D)	DGND	3C,8C,5A,10A	Digital Ground Return
+5 volts	PWR	19C,23C,26C,30C	+5 volt supply
+12 volts	PWR	15A	+12 volt supply
-12 volts	PWR	12A	-12 volt supply
$\overline{POR}$	I/OA	13C	Power-on-reset
B. MICROPROCESSOR INTERFACE:			
D7	I/OA	1C	Data Bus (8 Bits)
D6	I/OA	1A	
D5	I/OA	2C	
D4	I/OA	2A	
D3	I/OA	3A	
D2	I/OA	4C	
D1	I/OA	4A	
D0	I/OA	5C	
RS3	IA	6C	Register Select (4 Bits)
RS2	IA	6A	
RS1	IA	7C	
RS0	IA	7A	
$\overline{CS0}$	IA	10C	Chip Select Transmitter Device
$\overline{CS1}$	IA	9C	Chip Select Receiver Sample Rate Device
$\overline{CS2}$	IA	9A	Chip Select Receiver Baud Rate Device
READ	IA	12C	Read Enable
$\overline{WRITE}$	IA	11A	Write Enable
$\overline{IRQ}$	OB	11C	Interrupt Request

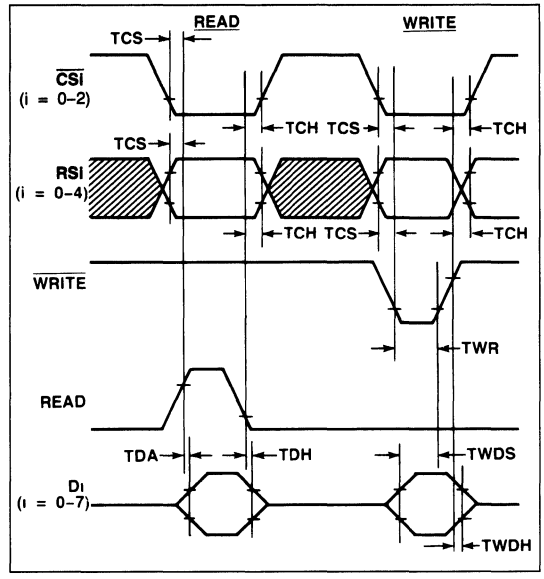
R48DP Hardware Circuits (Cont.)

Name	Type	Pin No.	Description
C. V.24 INTERFACE:			
$\overline{RDCLK}$	OC	21A	Receive Data Clock
TDCLK	OC	23A	Transmit Data Clock
XTCLK	IB	22A	External Transmit Clock
$\overline{RTS}$	IB	25A	Request-to-Send
$\overline{CTS}$	OC	25C	Clear-to-Send
TXD	IB	24C	Transmitter Data
RXD	OC	22C	Receiver Data
$\overline{RLSD}$	OC	24A	Received Line Signal Detector
D. ANCILLARY CIRCUITS:			
$\overline{RBCLK}$	OC	26A	Receiver Baud Clock
$\overline{TBCLK}$	OC	27C	Transmitter Baud Clock
E. ANALOG SIGNALS:			
TXA	AA	31A	Transmitter Analog Output
RXA	AB	32A	Receiver Analog Input
AUXIN	AC	30A	Auxiliary Analog Input
F. DIAGNOSTIC:			
EYEX	OC	15C	Eye Pattern Data—X Axis
EYEY	OC	14A	Eye Pattern Data—Y Axis
$\overline{EYECLK}$	OA	14C	Eye Pattern Clock
EYESYNC	OA	13A	Eye Pattern Synchronizing Signal

EYE PATTERN GENERATION

The four hardware diagnostic circuits, identified in the preceding table, allow the user to generate and display an eye pattern. Circuits EYEX and EYEY serially present eye pattern data for the horizontal and vertical display inputs respectively. The 8-bit data words are shifted out most significant bit first, clocked by the rising edge of the $\overline{EYECLK}$ output. The EYESYNC output is provided for word synchronization. The falling edge of EYESYNC may be used to transfer the 8-bit word from the shift register to a holding register. Digital to analog conversion can then be performed for driving the X and Y inputs of an oscilloscope.

MICROPROCESSOR TIMING



Microprocessor Interface Timing Diagram

Critical Timing Requirements

Characteristic	Symbol	Min	Max	Units
$\overline{CSi}$, RSi setup time prior to Read or Write	TCS	30	—	nsec
Data access time after Read	TDA	—	140	nsec
Data hold time after Read	TDH	10	50	nsec
CSi, RSi hold time after Read or Write	TCH	10	—	nsec
Write data setup time	TWDS	75	—	nsec
Write data hold time	TWDH	10	—	nsec
Write strobe pulse width	TWR	75	—	nsec

7

HARDWARE CIRCUIT CHARACTERISTICS

Digital Interface Characteristics

Digital Interface Characteristics

Symbol	Parameter	Units	Input/Output Type							
			IA	IB	IC	OA	OB	OC	I/O A	I/O B
V_{IH}	Input Voltage, High	V	2.0 Min.	2.0 Min.	2.0 Min.				2.0 Min.	5.25 Max. 2.0 Min.
V_{IL}	Input Voltage, Low	V	0.8 Max.	0.8 Max.	0.8 Max.				0.8 Max.	0.8 Max.
V_{OH}	Output Voltage, High	V				2.4 Min.[1]			2.4 Min.[1]	2.4 Min.[3]
V_{OL}	Output Voltage, Low	V				0.4 Max.[2]	0.4 Max.[2]	0.4 Max.[2]	0.4 Max.[2]	0.4 Max.[2]
I_{IN}	Input Current, Leakage	μA	±2.5 Max.						±2.5 Max.[4]	
I_{OH}	Output Current, High	mA				−0.1 Max.				
I_{OL}	Output Current, Low	mA				1.6 Max.	1.6 Max.	1.6 Max.		
I_L	Output Current, Leakage	μA					±10 Max.			
I_{PU}	Pull-up Current (Short Circuit)	μA		−240 Max. −10 Min.	−240 Max. −10 Min.			−240 Max. −10 Min.		−260 Max. −100 Min.
C_L	Capacitive Load	pF	5	5	20				10	40
C_D	Capacitive Drive	pF				100	100	100	100	100
	Circuit Type		TTL	TTL w/Pull-up	TTL w/Pull-up	TTL	Open-Drain	Open-Drain w/Pull-up	3-State Transceiver	Open-Drain w/Pull-up

Notes

1. I Load = −100 μA
2. I Load = 1.6 mA
3. I Load = −40 μA
4. V_{IN} = 0.4 to 2.4 Vdc, V_{CC} = 5.25 Vdc

Analog Interface Characteristics

Analog Interface Characteristics

Name	Type	Characteristics
TXA	AA	The transmitter output is a low impedance operational amplifier output. In order to match to 600 ohms, an external series resistor is required.
RXA	AB	The receiver input impedance is 63.4K ohms ±5%.
AUXIN	AC	The auxiliary analog input allows access to the transmitter for the purpose of interfacing with user provided equipment. Because this is a sampled data input, any signal above 4800 Hz will cause aliasing errors. The input impedance is 1K ohms, and the gain to transmitter output is −1 dB ±1 dB.

SOFTWARE CIRCUITS

The R48DP comprises three signal processor chips. Each of these chips contains 16 registers to which an external (host) microprocessor has access. Although these registers are within the modem, they may be addressed as part of the host processor's memory space. The host may read data out of or write data into these registers. The registers are referred to as interface memory. Registers in chip 1 update at half the modem sample rate (4800 bps). Registers in chip 0 and 2 update at the selected baud rate.

When information in these registers is being discussed, the format Y:Z:Q is used. The chip is specified by Y(0 – 2), the register by Z(0 – F), and the bit by Q(0 – 7, 0 = LSB).

Status Control Bits

The operation of the R48DP is affected by a number of software control inputs. These inputs are written into registers within the interface memory via the host microprocessor bus. Bits designated by an 'x' are "Don't Care" inputs that can be set to either 1 or 0. Modem operation is monitored by various software flags that are read from interface memory via the host microprocessor bus. All status and control bits are defined in the Interface Memory table. Bits designated by an 'R' are reserved for modem use only and must not be changed by the host.

RAM Data Access

The R48DP provides the user with access to much of the data stored in the modem's memories. This data is useful for performing certain diagnostic functions.

Two RAM access registers in chip 1 allow user access to RAM locations via the X word registers (1:3 and 1:2) and the Y word registers (1:1 and 1:0). Comparable registers in chip 2 provide access to chip 2 RAM locations. The access code stored in RAM ACCESS XS (1:5) selects the source of data for RAM DATA XSM and RAM DATA XSL (1:3 and 1:2). Similarly, the access code stored in RAM ACCESS YS (1:4) selects the source of data for RAM DATA YSM and RAM DATA YSL (1:1 and 1:0). Chip 2 registers are associated in the same way.

Reading of RAM data is performed by storing the necessary access codes in 1:5 and 1:4 (or 2:5 and 2:4), reading 1:0 (or 2:0) to reset the associated data available bit (1:E:0 or 2:E:0), then waiting for the data available bit to return to a one. Data is now valid and may be read from 1:3 through 1:0 (or 2:3 through 2:0). The contents of registers 2:3 and 2:1 are also available serially on outputs EYEX and EYEY, respectively, unless the IFIX bit (1:6:7) is set to a one. When IFIX is a one, EYEX and EYEY remain fixed on the rotated equalizer output.

RAM Access Codes

The RAM access codes defined in the following table allow the host processor to read diagnostic information within the modem.

RAM Access Codes

No.	Function	Chip	X Access	Y Access	Register
1	Received Signal Samples	1	C0	Not Used	2,3
2	Demodulator Output	1	C2	42	0,1,2,3
3	Low Pass Filter Output	1	D4	54	0,1,2,3
4	Average Energy	1	Not Used	04	0,1
5	AGC Gain Word	1	81	Not Used	2,3
6	Equalizer Input	2	C0	40	0,1,2,3
7	Equalizer Tap Coefficients	2	81 – AO	01 – 20	0,1,2,3
8	Unrotated Equalizer Output	2	E1	61	0,1,2,3
9	Rotated Equalizer Output (Received Points)	2	A2	22	0,1,2,3
10	Decision Points (Ideal Data Points)	2	E2	62	0,1,2,3
11	Error	2	E3	63	0,1,2,3
12	Rotation Angle	2	Not Used	00	0,1
13	Frequency Correction	2	AA	Not Used	2,3
14	EQM	2	A7	Not Used	2,3
15	Dual Point	2	AE	2E	0,1,2,3

NOTE

In the interface memory tables that follow, those columns marked by an 'X' indicate a user available bit position that is not currently used by the R48DP. However, those columns marked by an 'R' indicate reserved and are for modem use *only*.

Transmitter Interface Memory Chip 0 ($\overline{CS0}$)

Bit / Register	7	6	5	4	3	2	1	0
F	R	R	R	R	R	R	R	R
E	TIA	R	R	R	TSB	TIE	R	TBA
D	R	R	R	R	R	R	R	R
C	R	R	R	R	R	R	R	R
B	R	R	R	R	R	R	R	R
A	R	R	R	R	R	R	R	R
9	R	R	R	R	R	R	R	R
8	R	R	R	R	R	R	R	R
7	RTS	TTDIS	SDIS	MHLD	EPT	TPDM	XCEN	SEPT
6	TRANSMITTER CONFIGURATION							
5	X	X	CEQ		LAEN	LDEN	A3L	D3L
4	L3ACT	L4ACT	L4HG	TLVL			L2ACT	LCEN
3	FREQM							
2	FREQL							
1	R	R	R	R	R	R	R	R
0	TRANSMITTER DATA							
Register / Bit	7	6	5	4	3	2	1	0

Receiver Interface Memory Chip 1 ($\overline{CS1}$)

Bit / Register	7	6	5	4	3	2	1	0
F	R	R	R	R	R	R	R	R
E	RSIA	R	R	R	RSB	RSIE	R	RSDA
D	R	R	R	R	R	R	R	R
C	R	R	R	R	R	R	R	R
B	R	$\overline{PNDET}$	R	R	R	R	R	$\overline{CDET}$
A	R	R	R	R	R	R	R	R
9	R	$\overline{FED}$	R	R	R	R	R	R
8	R	R	R	R	R	$\overline{P2DET}$	R	R
7	RTH		DDIS	RPDM	R	R	T2	RTDIS
6	IFIX	TOD	RECEIVER CONFIGURATION					
5	RAM ACCESS XS							
4	RAM ACCESS YS							
3	RAM DATA XSM							
2	RAM DATA XSL							
1	RAM DATA YSM							
0	RAM DATA YSL; RECEIVER DATA							
Register / Bit	7	6	5	4	3	2	1	0

Receiver Interface Memory Chip 2 ($\overline{CS2}$)

Bit / Register	7	6	5	4	3	2	1	0
F	R	R	R	R	R	R	R	R
E	RBIA	R	R	R	R	RBIE	R	RBDA
D	R	R	R	R	R	R	R	R
C	R	R	R	R	R	R	R	R
B	R	R	R	R	R	R	R	R
A	R	R	R	R	R	R	R	R
9	R	R	R	R	R	R	R	R
8	R	R	R	R	R	R	R	R
7	R	R	R	R	R	R	R	R
6	R	R	R	R	R	R	R	R
5	RAM ACCESS XB							
4	RAM ACCESS YB							
3	RAM DATA XBM							
2	RAM DATA XBL							
1	RAM DATA YBM							
0	RAM DATA YBL							
Register / Bit	7	6	5	4	3	2	1	0

7

R48DP Interface Memory Definitions

Mnemonic	Name	Memory Location	Description
A3L	Amplitude 3-Link Select	0:5:1	See LAEN.
CEQ	Cable Equalizer Field	0:5:(4,5)	The CEQ Control field simultaneously controls amplitude compromise equalizers in both the transmit and receive paths. The following table lists the possible cable equalizer selection codes: **CEQ** — **Cable Length (0.4 mm diameter)** 0 — 0.0 1 — 1.8 km 2 — 3.6 km 3 — 7.2 km
$\overline{\text{CDET}}$	Carrier Detector	1:B:0	When zero, status bit $\overline{\text{CDET}}$ indicates that passband energy is being detected, and that a training sequence is not in process. $\overline{\text{CDET}}$ goes to a zero at the start of the data state, and returns to a one at the end of the received signal.
DDIS	Descramble Disable	1:7:5	When control bit DDIS is a one, the receiver descrambler circuit is removed from the data path.
D3L	Delay 3-Link Select	0:5:0	See LDEN.
EPT	Echo Protector Tone	0:7:3	When control bit EPT is a one, an unmodulated carrier is transmitted for 185 ms (optionally 30 ms) followed by 20 ms of no transmitted energy at the start of transmission.
$\overline{\text{FED}}$	Fast Energy Detector	1:9:6	When status bit $\overline{\text{FED}}$ is a zero, it indicates that energy above the receiver threshold is present in the passband.
(None)	FREQL/FREQM	0:2:0–7, 0:3:0–7	The host processor conveys tone generation data to the transmitter by writing a 16-bit data word to the FREQL and FREQM registers in the interface memory space, as shown below: *FREQM Register (0:3)* **Bit:** 7 6 5 4 3 2 1 0 **Data Word:** 2^{15} 2^{14} 2^{13} 2^{12} 2^{11} 2^{10} 2^{9} 2^{8} *FREQL Register (0:2)* **Bit:** 7 6 5 4 3 2 1 0 **Data Word:** 2^{7} 2^{6} 2^{5} 2^{4} 2^{3} 2^{2} 2^{1} 2^{0} The frequency number (N) determines the frequency (F) as follows: F = (0.146486) (N) Hz ±0.01% Hexadecimal frequency numbers (FREQL, FREQM) for commonly generated tones are given below: **Frequency (Hz)** — **FREQM** — **FREQL** 462 — 0C — 52 1100 — 1D — 55 1650 — 2C — 00 1850 — 31 — 55 2100 — 38 — 00
IFIX	Eye Fix	1:6:7	When control bit IFIX is a one, the serial data on EYEX and EYEY reflect the rotated equalizer output and do not follow the data selected by RAM ACCESS XB and RAM ACCESS YB.

R48DP Interface Memory Definitions (Continued)

Mnemonic	Name	Memory Location	Description
LAEN	Link Amplitude Equalizer Enable	0:5:3	The link amplitude equalizer enable and select bits control an amplitude compromise equalizer in the receive path acording to the following table: **LAEN** / **A3L** / **Curve Matched** 0 / X / No Equalizer 1 / 0 / U.S. Survey Long 1 / 1 / Japanese 3-Link
LCEN	Loop Clock Enable	0:4:0	When control bit LCEN is a one, the transmitter clock tracks the receiver clock.
LDEN	Link Delay Equalizer Enable	0:5:2	The link delay equalizer enable and select bits control a delay compromise equalizer in the receive path according to the following table: **LDEN** / **D3L** / **Curve Matched** 0 / X / No Equalizer 1 / 0 / U.S. Survey Long 1 / 1 / Japanese 3-Link
L2ACT	Remote Digital Loopback Activate	0:4:1	When control bit L2ACT is a one, the receiver digital output is connected to the transmitter digital input in accordance with CCITT recommendation V 54 loop 2.
L3ACT	Local Analog Loopback Activate	0:4:7	When control bit L3ACT is a one, the transmitter analog output is coupled to the receiver analog input through an attenuator in accordance with CCITT recommendation V.54 loop 3.
L4ACT	Remote Analog Loopback Activate	0:4:6	When control bit L4ACT is a one, the receiver analog input is connected to the transmitter analog output through a variable gain amplifier in a manner similar to recommendation V.54 loop 4.
L4HG	Loop 4 High Gain	0:4:5	When control bit L4HG is a one, the loop 4 variable gain amplifier is set for +16 dB, and when at zero the gain is zero dB.
MHLD	Mark Hold	0:7:4	When control bit MHLD is a one, the transmitter input data stream is forced to all marks (ones).
$\overline{\text{PNDET}}$	Period N Detector	1:B:6	When status bit $\overline{\text{PNDET}}$ is a zero, it indicates a PN sequence has been detected. This bit sets to a one at the end of the PN sequence.
$\overline{\text{P2DET}}$	Period Two Detector	1:8:2	When status bit $\overline{\text{P2DET}}$ is a zero, it indicates that a P2 sequence has been detected. This bit sets to a one at the start of the PN sequence.
(None)	RAM Access XB	2:5:0–7	Contains the RAM access code used in reading chip 2 RAM locations via word X (2:3 and 2:2).
(None)	RAM Access XS	1.5:0–7	Contains the RAM access code used in reading chip 1 RAM locations via word X (1:3 and 1:2).
(None)	RAM Access YB	2:4:0–7	Contains the RAM access code used in reading chip 2 RAM locations via word Y (2:1 and 2:0).
(None)	RAM Access YS	1:4:0–7	Contains the RAM access code used in reading chip 1 RAM locations via word Y (1:1 and 1:0).
(None)	RAM Data XBL	2:2:0–7	Least significant byte of 16-bit word X used in reading RAM locations in chip 2.
(None)	RAM Data XBM	2:3:0–7	Most significant byte of 16-bit word X used in reading RAM locations in chip 2.
(None)	RAM Data XSL	1:2:0–7	Least significant byte of 16-bit word X used in reading RAM locations in chip 1
(None)	RAM Data XSM	1:3:0–7	Most significant byte of 16-bit word X used in reading RAM locations in chip 1.

7

R48DP Interface Memory Definitions (Continued)

Mnemonic	Name	Memory Location	Description
(None)	RAM Data YBL	2:0:0–7	Least significant byte of 16-bit word Y used in reading RAM locations in chip 2.
(None)	RAM Data YBM	2:1:0–7	Most significant byte of 16-bit word Y used in reading RAM locations in chip 2.
(None)	RAM Data YSL	1:0:0–7	Least significant byte of 16-bit word Y used in reading RAM locations in chip 1. Shared by parallel data mode for presenting channel data to the host microprocessor bus. See 'Receiver Data.'
(None)	RAM Data YSM	1:1:0–7	Most significant byte of 16-bit word Y used in reading RAM locations in chip 1.
RBDA	Receiver Baud Data Available	2:E·0	Status bit RBDA goes to a one when the receiver writes data into register 2:0. The bit goes to a zero when the host processor reads data from register 2:0.
RBIA	Receiver Baud Interrupt Active	2:E:7	This status bit is a one whenever the receiver baud rate device is driving $\overline{IRQ}$ low.
RBIE	Receiver Baud Interrupt Enable	2:E:2	When the host processor writes a one in the RBIE control bit, the $\overline{IRQ}$ line of the hardware interface is driven to zero when status bit RBDA is a one.
(None)	Receiver Configuration	1:6:0–5	The host processor configures the receiver by writing a control code into the receiver configuration field in the interface memory space (see RSB). *Receiver Configuration Control Codes* Control codes for the modem receiver configuration are: **Configuration** — **Configuration Code (Hex)** V.27 4800 Long — 22 V.27 2400 Long — 21 V.27 4800 Short — 02 V.27 2400 Short — 01
(None)	Receiver Data	1:0:0–7	The host processor obtains channel data from the receiver in the parallel data mode by reading a data byte from the receiver data register. The data is divided on baud boundaries as is the transmitter data. When using receiver parallel data mode, the registers 1:3 through 1:0 can not be used for reading the chip 1 RAM.
RPDM	Receiver Parallel Data Mode	1:7:4	When control bit RPDM is a one, the receiver supplies channel data to the receiver data register (1:0) as well as to the hardware serial data output. (See Receiver Data)
RSB	Receiver Setup Bit	1:E:3	When the host processor changes the receiver configuration or the RTH field, the host processor must write a one in the RSB control bit. RSB goes to zero when the changes become effective.
RSDA	Receiver Sample Data Available	1:E:0	Status bit RSDA goes to a one when the receiver writes data to register 1:0. RSDA goes to a zero when the host processor reads data from register 1:0.
RSIA	Receiver Sample Interrupt Active	1:E:7	This status bit is a one whenever the receiver sample rate device is driving $\overline{IRQ}$ to zero.
RSIE	Receiver Sample Interrupt Enable	1:E:2	When the host processor writes a one in the RSIE control bit, the $\overline{IRQ}$ line of the hardware interface is driven to zero when status bit RSDA is a one.
RTDIS	Receiver Training Disable	1:7:0	When control bit RTDIS is a one, the receiver is prevented from recognizing a training sequence and entering the training state
RTH	Receiver Threshold Field	1:7:6,7	The receiver energy detector threshold is set by the RTH field according to the following codes (see RSB): **RTH** — **RLSD On** — **RLSD Off** 0 — > –43 dBm — < –48 dBm 1 — > –33 dBm — < –38 dBm 2 — > –26 dBm — < –31 dBm 3 — > –16 dBm — < –21 dBm

R48DP Interface Memory Definitions (Continued)

Mnemonic	Name	Memory Location	Description
RTS	Request-to-Send	0:7:7	When control bit RTS goes to a one, the modem begins a transmit sequence. It continues to transmit until RTS is reset to zero, and the turn-off sequence has been completed. This input bit parallels the operation of the hardware RTS control input. These inputs are ORed by the modem.
SDIS	Scrambler Disable	0:7:5	When control bit SDIS is a one, the transmitter scrambler circuit is removed from the data path.
SEPT	Short Echo Protector Tone	0:7:0	When control bit SEPT is a one, the echo protector tone is 30 ms long rather than 185 ms.
TBA	Transmitter Buffer Available	0:E:0	This status bit resets to zero when the host processor writes data to transmitter data register 0:0. When the transmitter empties register 0:0, this bit sets to a one.
TIA	Transmitter Interrupt Active	0:E:7	This status bit is a one whenever the transmitter is driving $\overline{IRQ}$ to a zero.
TIE	Transmitter Interrupt Enable	0:E:2	When the host processor writes a one in control bit TIE, the $\overline{IRQ}$ line of the hardware interface is driven to zero when status bit TBA is at a one.
TLVL	Transmitter Level Field	0:4:2–4	The transmitter analog output level is determined by eight TLVL codes, as follows. **TLVL** — **Transmitter Analog Output*** 0 — −1 dBm ±1 dB 1 — −3 dBm ±1 dB 2 — −5 dBm ±1 dB 3 — −7 dBm ±1 dB 4 — −9 dBm ±1 dB 5 — −11 dBm ±1 dB 6 — −13 dBm ±1 dB 7 — −15 dBm ±1 dB *Each step above is a 2 dB change ±0 2 dB.
TOD	Train-on Data	1:6:6	When control bit TOD is a one, it enables the train-on-data algorithm to converge the equalizer if the signal quality degrades sufficiently. When TOD is a one, the modem still recognizes a training sequence and enters the force train state. A BER of approximately 10^{-3} for 0 5 seconds initiates train-on data
TPDM	Transmitter Parallel Data Mode	0:7:2	When control bit TPDM is a one, the transmitter accepts data for transmission from the transmitter data register (0:0) rather than the serial hardware data input.
(None)	Transmitter Configuration	0:6:0–7	The host processor configures the transmitter by writing a control byte into the transmitter configuration register in its interface memory space. *Transmitter Configuration Control Codes* Control codes for the modem transmitter configurations are: **Configuration** — **Configuration Code (Hex)** V.27 4800 Long — 22 V.27 2400 Long — 21 V.27 4800 Short — 02 V.27 2400 Short — 01 Tone Transmit — 80

R48DP Interface Memory Definitions (Continued)

<table>
<tr><th>Mnemonic</th><th>Name</th><th>Memory Location</th><th>Description</th></tr>
<tr><td>(None)</td><td>Transmitter Data</td><td>0:0:0–7</td><td>The host processor conveys output data to the transmitter in the parallel mode by writing a data byte to the transmitter data register. The data is divided on baud boundaries, as follows:

NOTE

Data is transmitted bit zero first.

<table>
<tr><th rowspan="2">Configuration</th><th colspan="8">Bits</th></tr>
<tr><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr>
<tr><td>V.27 4800 bps</td><td colspan="2">Not Used</td><td colspan="3">Baud 1</td><td colspan="3">Baud 0</td></tr>
<tr><td>V.27 2400 bps</td><td colspan="2">Baud 3</td><td colspan="2">Baud 2</td><td colspan="2">Baud 1</td><td colspan="2">Baud 0</td></tr>
</table></td></tr>
<tr><td>TSB</td><td>Transmitter Setup Bit</td><td>0:E:3</td><td>When the host processor changes the transmitter configuration, the host must write a one in this control bit. TSB goes to a zero when the change becomes effective.</td></tr>
<tr><td>TTDIS</td><td>Transmitter Train Disable</td><td>0:7:6</td><td>When control bit TTDIS is a one, the transmitter does not generate a training sequence at the start of transmission. With training disabled, RTS/CTS delay is less than two baud times.</td></tr>
<tr><td>T2</td><td>T/2 Equalizer Select</td><td>1:7:1</td><td>When control bit T2 is a one, an adaptive equalizer with two taps per baud is used. When T2 is a zero, the equalizer has one tap per baud. The total number of taps remains the same for both cases.</td></tr>
<tr><td>XCEN</td><td>External Clock Enable</td><td>0:7:1</td><td>When control bit XCEN is a zero, the transmitter timing is established by the external clock supplied at the hardware input XTCLK, pin 22A.</td></tr>
</table>

POWER-ON INITIALIZATION

When power is applied to the R48DP, a period of 50 to 350 ms is required for power supply settling. The power-on-reset signal (POR) remains low during this period. Approximately 10 ms after the low to high transition of POR, the modem is ready to be configured, and RTS may be activated. If the 5 Vdc power supply drops below 3.5 Vdc for more than 30 msec, the POR cycle is generated.

At POR time the modem defaults to the following configuration: V.27 4800 bps, short train, T/2, no echo protector tone, serial data mode, internal clock, cable equalizers disabled, link amplitude equalizer disabled, link delay equalizer disabled, transmitter output level set to −1 dBm ±1 dB, interrupts disabled, receiver threshold set to −43 dBm, eye pattern selectable, and train-on-data disabled.

POR can be connected to a user supplied power-on-reset signal in a wire-or configuration. A low active pulse of 3 μsec or more applied to the POR pin causes the modem to reset. The modem is ready to be configured 10 msec after POR is removed.

PERFORMANCE

Functioning as a V.27 bis/ter type modem, the R48DP provides the user with unexcelled high performance.

BIT ERROR RATES

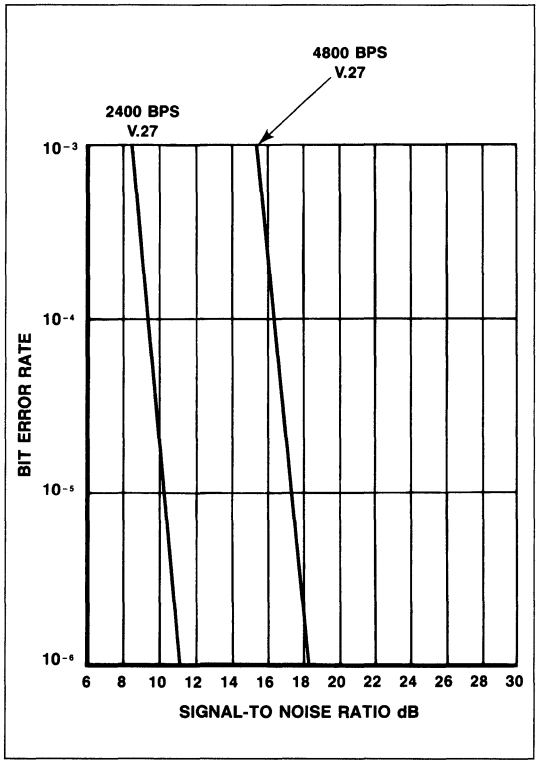
The Bit Error Rate (BER) performance of the modem is specified for a test configuration conforming to that specified in CCITT recommendation V.56, except with regard to the placement of the filter used to bandlimit the white noise source. Bit error rates are measured at a received line signal level of −20 dBm as illustrated.

PHASE JITTER

At 2400 bps, the modem exhibits a bit error rate of 10^{-6} or less with a signal-to-noise ratio of 12.5 dB in the presence of 15° peak-to-peak phase jitter at 150 Hz or with a signal-to-noise ratio of 15 dB in the presence of 30° peak-to-peak phase jitter at 120 Hz (scrambler inserted).

At 4800 bps (V.27 bis/ter), the modem exhibits a bit error rate of 10^{-6} or less with a signal-to-noise ratio of 19 dB in the presence of 15° peak-to-peak phase jitter at 60 Hz.

An example of the BER performance capabilities is given in the following diagram:



Worst Case BER Performance (Back-to-Back)

GENERAL SPECIFICATIONS

Power

Voltage	Tolerance	Current (Max)
+5 Vdc	±5%	<700 mA
+12 Vdc	±5%	<20 mA
−12 Vdc	±5%	<80 mA
Note: All voltages must have ripple ≤0.1 volts peak-to-peak.		

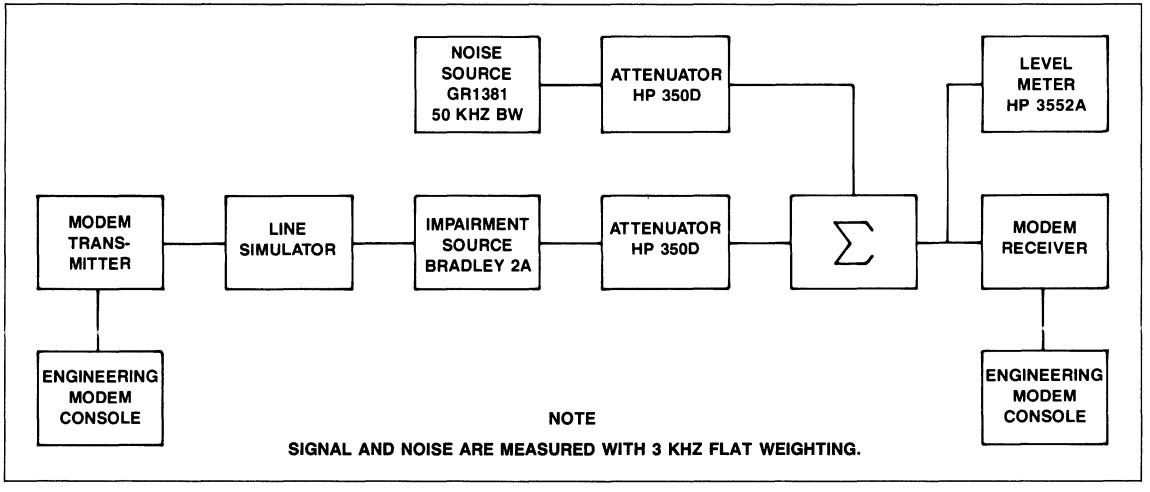
Environmental

Parameter	Specification
Temperature Operating Storage	 0°C to +60°C (32 to 140°F) −40°C to +80°C (−40 to 176°F) Stored in heat sealed antistatic bag and shipping container
Relative Humidity	Up to 90% noncondensing, or a wet bulb temperature up to 35°C, whichever is less

Mechanical

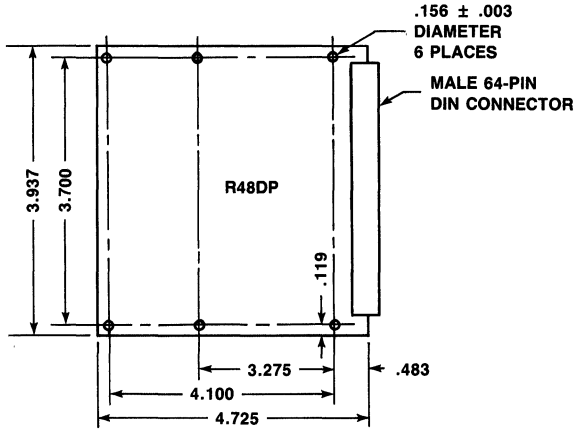
Parameter	Specification
Board Structure	Single PC board with single right angle header with 64 pins, Burndy (P196B32R00A00Z1) or equivalent mating connector.
Dimensions	Width—3.94 in. (100 mm) Length—4.72 in. (120 mm) Height—0.4 in. (10.2 mm)
Weight	Less than 3.6 oz. (100g)

The BER performance test set-up is shown in the following diagram:



BER Performance Test Set-up

7



Inches	MM
.119	3
.156	4
.483	12
3.275	83
3.700	94
3.937	100
4.100	104
4.725	120

R48DP Circuit Board Dimensions

Rockwell

V27P/1
HIGH SPEED 4800 BPS MODEM

INTRODUCTION

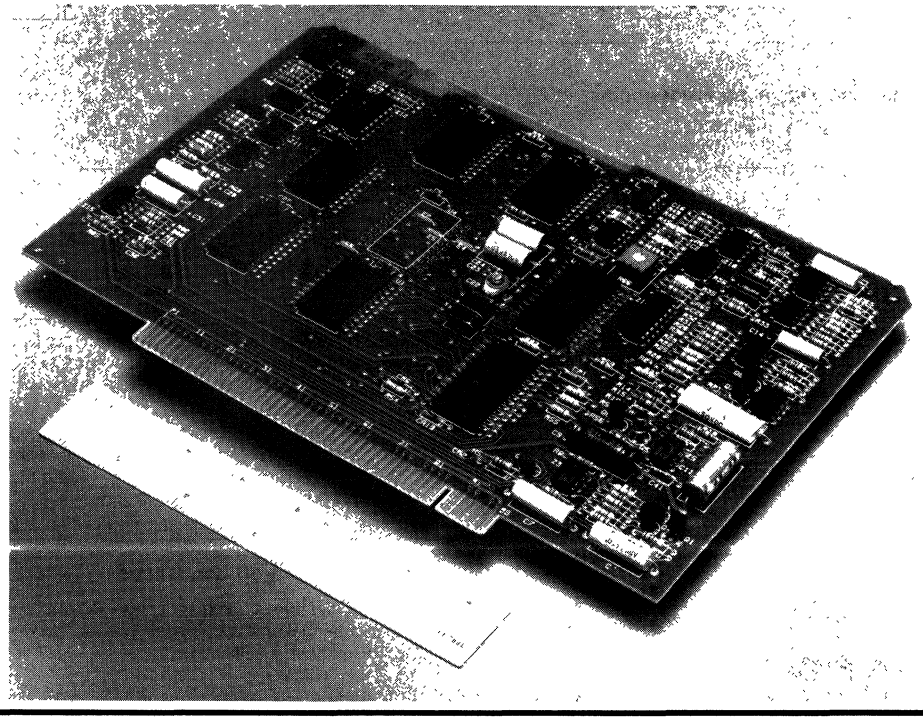
The Rockwell V27P/1 is a versatile, high performance, 4800 bps modem on a single printed circuit board. Being CCITT V.27 compatible, the V27P/1 (with minimal interface circuitry) can operate on dedicated 2-wire or 4-wire half-duplex or 4-wire full-duplex lines. The V27P/1 can also operate in half-duplex on the general switched network.

Measuring approximately 9.2 inches (23.3 cm) by 6.3 inches (16.0 cm), the V27P/1 is the smallest full-feature 4800 bps modem that approaches data communication theoretical performance limits.

The V27P/1 meets the tolerances specified in the CCITT V.27 bis (alternate A), V.27 ter and FSK T.30 specifications. In addition, the V27P/1 can be configured to be functionally compatible with those enhanced specifications available in the Rockwell V27P and M48P modem series.

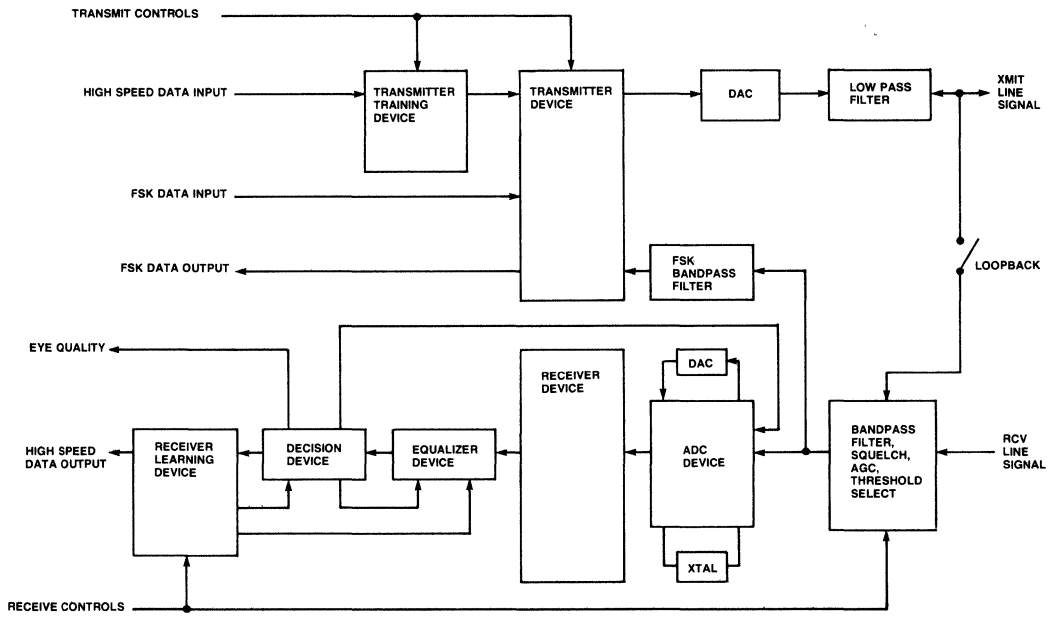
FEATURES

- Single printed circuit card
- 4800/2400 bps modes
- Full-duplex or half-duplex
- Dedicated or general switched network lines operation
- Ultimate user flexibility:
  —CCITT V.27 ter, V 27 bis compatible
  —Also 300 bps binary signalling per CCITT T.30
- TTL compatibility
- Automatic adaptive equalizer
- Analog loopback test circuitry
- 0 to −45 dBm dynamic AGC
- LSI signal processing
- High reliability
- Low power consumption:
  —Typically 3.5 watts
- Automatic training sequence for receiver



7

FUNCTIONAL SPECIFICATIONS



V27P/1 Functional Block Diagram

Transmit Carrier and Signalling Frequencies

Carrier Frequency Codex Compatible QAM:	1706.667 Hz ± 0.01%
Carrier Frequency V.27:	1800 Hz ± 0.01%
Echo Suppression Frequencies:	2100 Hz ± 0.01%
	2025 Hz ± 0.01%
Signalling Frequencies of T.30:	1850 Hz ± 0.01%
	1650 Hz ± 0.01%
	1300 Hz ± 0.01%
	1100 Hz ± 0.01%

Received Signal Frequency Tolerance

The receiver can receive frequency errors of up to ± 10 Hz with less than a 0.2 dB degradation in Bit Error Rate performance.

Data Signalling and Modulation Rate

At 1600 baud:	
Signalling Rate—	1600 baud ± 0.01%
Data Rate—	4800 bps ± 0.01%
At 1200 baud:	
Signalling Rate—	1200 baud ± 0.01%
Data Rate—	2400 bps ± 0.01%

Transmitted Data Spectrum

At 1600 baud the transmitted spectrum is shaped by approximately a square root of 50 percent raised cosine filter function. At 1200 baud the spectrum is shaped by approximately a square root of 90 percent raised cosine filter function.

The 1600 and 1200 baud configurations require a usable bandwidth from 950 Hz to 2650 Hz and 1150 Hz to 2450 Hz respectively.

Data Encoding

At 1600 baud the data stream is divided into groups of three bits (tribits). The data rate of 4800 bps may use either an 8-point QAM structure or 8-phase structure. Encoding of the tribits in the 8-phase structure are per CCITT Recommendation V.27 ter.

At 1200 baud the data stream is divided into groups of two bits (dibits). The data rate of 2400 bps uses a 4-phase data structure. Encoding of the dibits may be per the fallback rate of CCITT Recommendation V.27 bis and ter (same as V.26A) or V26B depending on the selected configuration.

Turn-on, Turn-off Sequences

The V27P/1 turn-on sequences are compatible with CCITT Recommendations V.27 bis (alternate i), V.27, and Rockwell M48P modem specifications.

The turn-off sequences for all V.27 modes (except the 1600 baud rate manual V.27 mode) consists of 5 to 10 millisec-

onds of remaining data followed by continuous scrambled 1's followed by no transmission energy. The period of no transmission energy is provided by turning off the transmitter key signal for a recommended duration of 20 milliseconds.

The turn-off sequences for all non-V.27 modes consists of 4 to 7 milliseconds of remaining data followed by a period of no transmission energy.

Ready For Sending Response Times

The Ready For Sending response time to a Request To Send is determined by the configuration selected and its corresponding training time. In Table 1 the Training Times are shown in milliseconds. Note, however, that the 1600 baud manual CCITT configurations actually specify the synchronizing sequence timing per CCITT V.27 rather than the training time. Also note the following abbreviations.

ITC (1P–5P): Transmitter Configuration Inputs 1 through 5. These five bits establish the octal code shown where P1 and P2 are the most significant octal digit and P3 through P5 establish the least significant octal digit shown in the chart.

IRC (1P–5P): Receiver Configuration Inputs 1 through 5. These five bits establish the octal code shown where P1 and P2 are the most significant octal digit and P3 through P5 establish the least significant octal digit shown in the chart.

IRSS (1P–2P), ITSS (1P–2P): Receiver Signal Structure and Transmitter Signal Structure. Where P1 and P2 establish an octal code of 0, 1, 2, or 3. They define the signal structures as follows:

1 selects 8 point QAM

3 selects DPSK as:
8-phase at 1600 baud
4-phase at 1200 baud

V27P/1 Configurations

No.	Configuration	Transmitter ITC (1P-5P) (Octal Code)	Receiver IRC (1P-5P) (Octal Code)	Signal Structure IRSS (1P-2P) ITSS (1P-2P) (Octal Code)	Data Rate (bps)	Training Time (msec)	Carrier Frequency (hz)
1.	1600 Baud DIAL, CCITT DIAL	22	22	1,3	4800	181	NOTE
2.	1600 Baud DIAL — T/2	22	36	1,3	4800	181	NOTE
3.	1600 Baud DIAL Slow	36	22	1,3	4800	221	NOTE
4.	1600 Baud P-P	20	20	1,3	4800	141	NOTE
5.	1600 Baud P-P — T/2	20	32	1,3	4800	141	NOTE
6.	1600 Baud Manual CCITT	32	30	3	4800	20 (Sync Sequence)	1800
7.	1600 Baud Manual CCITT	30	30	3	4800	50 (Sync Sequence)	1800
8.	1600 Baud V27 DIAL/P-P	23	23	3	4800	708	1800
9.	1600 Baud V27 DIAL/P-P EP	27	23	3	4800	923	1800
10.	1600 Baud V27 DIAL/P-P — T/2	23	33	3	4800	708	1800
11.	1600 Baud V27 DIAL/P-P — T/2 EP	27	33	3	4800	923	1800
12.	1600 Baud V27 Multipoint — T/2	21	27	3	4800	50	1800
13.	1600 Baud V27 Resync (use with configuration 8)	21	25	3	4800	50	1800
14.	1600 Baud V27 Resync EP (use with configuration 9)	25	25	3	4800	265	1800
15.	1600 Baud V27 Resync — T/2 (use with configuration 10)	21	35	3	4800	50	1800
16	1600 Baud V27 Resync — T/2 EP (use with configuration 11)	25	35	3	4800	265	1800
17	1200 Baud DIAL	14	10	3	2400	170	1800
18.	1200 Baud P-P	10	10	3	2400	117	1800
19.	1200 Baud V27 DIAL/P-P	13	11	3	2400	943	1800
20.	1200 Baud V27 DIAL/P-P EP	17	11	3	2400	1158	1800
21.	1200 Baud V27 Multipoint	11	15	3	2400	66	1800
22.	1200 Baud V27 Resync (use with configuration 19)	11	13	3	2400	66	1800
23.	1200 Baud V27 Resync EP (use with configuration 20)	15	13	3	2400	281	1800

Note: Carrier frequency is 1706 2/3 Hz when IRSS (1P–2P) is a 1 (8-point).
Carrier frequency is 1800 Hz when IRSS (1P–2P) is a 3 (8-phase DPSK).

7

Received Line Signal Detector (D109)

The time response of the Received Line Signal detector circuit (D109) is a function of the length of the received turn-on sequence. Circuit D109 turns on after synchronizing is completed and prior to user data appearing on the received output line. D109 turns on for approximately 2 milliseconds after the echo protect tone disappears in the V27EP configurations (No. 9, 11, 14, 16, 20 and 23 of the V27P/1 Configuration Chart).

For non-CCITT configurations (No. 1, 2 and 3 in the table on page 3), D109 momentarily goes on at the beginning of the synchronizing sequence.

When no synchronizing signal is detected at the receiver, D109 turns on in 5 to 15 milliseconds for an applied signal greater than 3 dB above the turn on threshold. If training is not enabled at the receiver, D109 turns on in 5 to 15 milliseconds.

Three threshold options are provided:

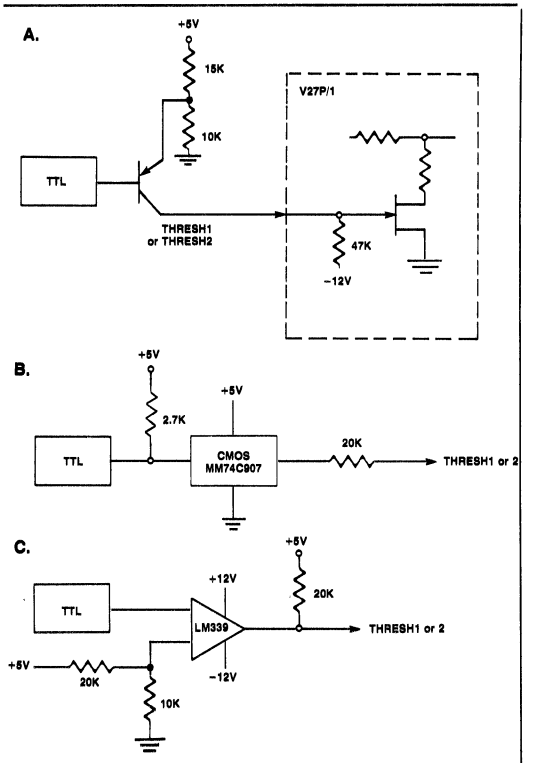
1) Greater than −43 dBm:	D109 ON
Less than −48 dBm:	D109 OFF
2) Greater than −26 dBm:	D109 ON
Less than − 31 dBm:	D109 OFF
3) Greater than −16 dBm:	D109 ON
Less than −21 dBm:	D109 OFF

The three threshold options are controlled by the condition of the THRESH1 and THRESH2 control lines as indicated below.

dB LEVEL	THRESH1	THRESH2
−43 dBm ON	Open Circuit	Open Circuit
−26 dBm ON	Open Circuit	0 to −0.5V
−16 dBm ON	0 to −0.5V	Open Circuit

When the received signal drops 5 dB below the D109 turn off threshold, D109 will turn off in 5 to 15 milliseconds. The condition of D109 between the selected turn on and turn off thresholds is not specified except that a hysteresis action of greater than 2 dB exists between the off-to-on and on-to-off transition levels.

Recommended circuits to control THRESH1 and THRESH2 input interface lines are shown in diagrams (A, B and C).



Suggested Interface Circuits for Controlling THRESH1 and THRESH2 Input Lines

Bit Error Rates

The V27P/1 is thoroughly tested to guarantee Bit Error Rate (BER) performance under test conditions equivalent to CCITT Recommendation V.26. The test set-up used by Rockwell is shown in the BER Performance Test Set-up diagram.

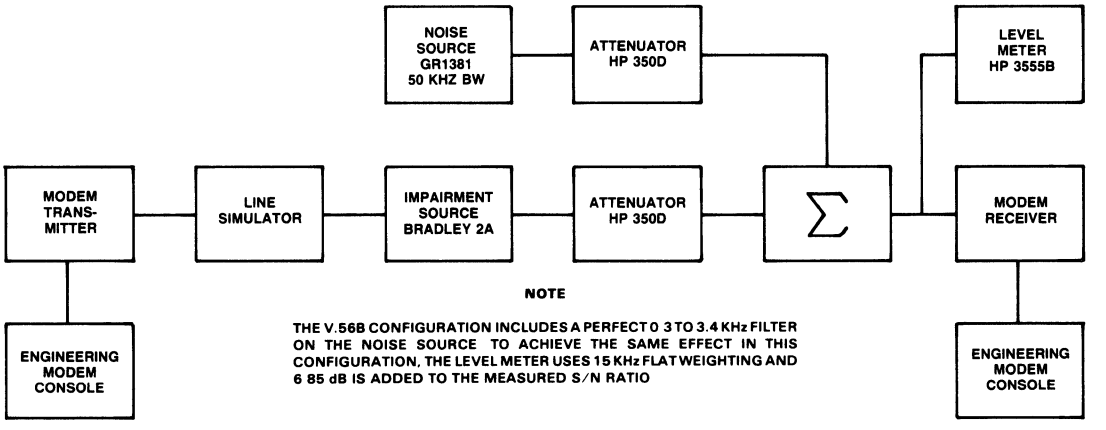
The results of these BER performance tests are shown in the Typical Bit Error Rate Performance diagram.

Data Scrambler Selection

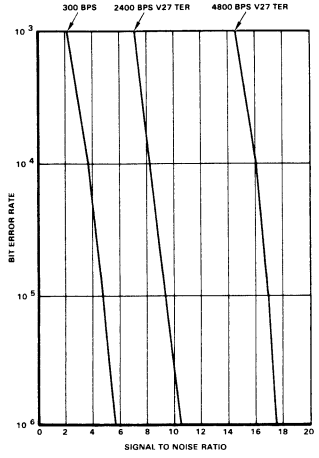
The V27P/1 makes available to the user one CCITT V.29 compatible scrambler, five different period 127 scramblers (and descramblers), and a no scramble option. These scramblers provide data transmitted by the V27P/1 with the degree of randomness necessary to ensure the continued convergence of all adaptive processes at the receiver. The seven possible scrambler configurations that are user software selectable are:

- Period 127 cryptographic
- Period 127 synchronizing
- CCITT period 127 self synchronizing (compatible with CCITT Recommendation V.27)
- Period 8,388,607 self synchronizing (compatible with CCITT Recommendation V.29)
- Period 127 self synchronizing with 8-bit protection
- CCITT period 127 self synchronizing (compatible with CCITT Recommendations V.27 bis and ter)
- No scrambler

All scramblers can be used with all modem configurations listed in the table on page 3.



BER Performance Test Set-up



Typical Bit Error Rate Performance

MODES OF OPERATION

The V27P/1 has two modes of operation; a training mode and a data mode. In order for the receiver to correctly decode the transmitted data the V27P/1 must detect the presence of a line signal, adjust the AGC, detect the presence of a training sequence, recover the baud timing of the transmitter, phase and frequency lock to the carrier associated with the received signal, and adapt the equalizer to the amplitude and delay characteristics of the channel. This learning process is accomplished most efficiently when the transmitter initiates a training sequence whenever a new transmitter-receiver connection is made. It is possible to set up the receiver without a training sequence, but it is a manual mode requiring considerable user effort. In a training mode, an internally generated pattern is transmitted to the receiver to facilitate synchronization. During the training mode, the data input line to the receiver is ignored and the output line does not reflect the state of the data input.

In the data mode of operation, information on the data input is strobed by the transmitter signal element clock and transmitted to the receiver. The receiver demodulates and decodes the passband signal and outputs the recovered data on the output where it is then ready to be strobed by the receiver signal element clock.

Request To Send—Ready For Sending

To initiate transmitter operation in the data or training mode, the Request to Send input is brought high. If a training mode is not initiated the Ready for Sending indicator goes high within one baud interval and data transmission commences.

The mode of the receiver is indicated by the data channel received line signal detector (D109). For data mode, D109 is high and the receiver training mode indicator is low.

If the receiver enters the training mode, the receiver training mode indicator goes high until the training mode is completed. When training is completed the receiver training mode indicator goes low and, if sufficient signal energy is present on the input line, D109 goes high, enabling the data mode.

Training Mode—Dial and Point-To-Point

For dial and point-to-point configurations, the V27P/1 receiver training is automatically initiated whenever a training sequence is detected in the received line signal. The training sequence consists of two phases: Phase 1 causes the training detector to turn on and also makes a course adjustment of the carrier

7

frequency variable which compensates for any frequency translation due to the channel; Phase 2 is used to converge the adaptive equalizer which is part of the V27P/1 structure.

A short scrambler synchronization sequence follows Phase 2 and is used to generate the success indicator. In order for training to be successful, the incoming training sequence must have been generated by a similarly configured transmitter using a compatible training sequence.

At the receiver, detection of a training sequence requires that there be sufficient signal energy and that the receiver's carrier frequency variable be within 30 Hz of nominal.

Training Resync (V.27 bis/ter Turnaround)

In a 2-wire half duplex data communication system, data can be transmitted in only one direction at any given instant. Therefore, the modems at the local and remote sites are required to interchange their roles as the receiver and the transmitter respectively. This turnaround operation requires constant resynchronization to meet CCITT Recommendations for V.27 bis/ter.

The resync configurations are used for reacquiring synchronization in turnaround operation without having to go through the normal long training sequence. The resync training sequences are relatively short and are used for recovering carrier phase, symbol timing and achieving equalizer convergence without resetting carrier frequency and equalizer taps.

Training Mode—Multipoint

In the V27P/1 modem, two multipoint configurations are provided for 4-wire circuits conforming to M1020 which permit short training sequences. In these configurations, the first train signal must be high to process the short training sequences; otherwise the receiver will ignore the training sequence and enter directly into the data mode. The receiver will enter into the training mode if the first train signal is high and there is sufficient signal energy.

For 4-wire circuits which are worse than M1020 and for 2-wire circuits, a long training sequence should be used rather than the multipoint configuration. These training sequences require that the receiver be in the proper dial/point-to-point configuration.

Training Mode—Manual

The V27P/1 modem includes two manual configurations in which the remote modem need not transmit a special training sequence to the local receiver. In these configurations, the equalizer tap coefficients for the local receiver must be initialized from an external source. The tap coefficients may be initialized by controlling three input terms—ICR, ICI and ICLCP—in synchronization with the Baud Rate Clock.

In order to operate the modem in the manual configurations, both the transmitter and receiver must be set according to the code shown in Table 1. Manual configuration code octal 30 has a longer synchronizing sequence than configuration code octal 32, but both synchronizing sequences conform to the CCITT Recommendation V.27. However, neither sequence is of sufficient duration to aid in training the receiver.

Receiver Operation During Loss of Line Signal

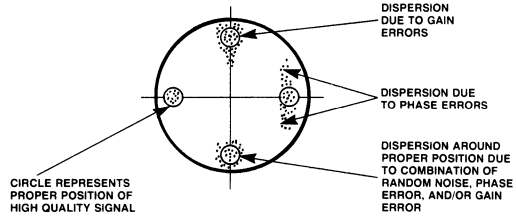
When there is no line signal present, all receiver update relating to the equalizer, carrier frequency variable and baud timing are inhibited and the current values of the equalizer taps and the carrier frequency variable are retained.

DATA QUALITY

The receiver generates an Eye Quality Monitor (EQM) signal that can be used to determine the equivalent Gaussian signal to noise ratio of the overall system within approximately ± 2 db. Eye quality is determined by calculating the difference between the received signal point after equalization and the transmitted or expected signal point. The receiver output DEQ2P is a filtered version of this error signal. It is a serial word clocked by the system bit clock (345.6 KHz or 230.4 KHz, depending on baud rate). Output signal DQGTP is a gating signal which delineates the eight MSB's of DEQ2P. The use and interpretation of these binary signals are quite complex and are dependent on the application and the signal structure. The user can derive a meaningful interpretation of the EQM readings by monitoring them while testing the modem against his performance criteria.

Visual Display of Eye Pattern

A visual indication of the modem's performance can be obtained by displaying the received baseband signal structure after equalization. This is done by converting the eight MSB's of the real and imaginary equalized signal points available on DRERP and DIERP to analog voltages which are then used to drive the horizontal and vertical sweeps of an oscilloscope. The resultant display will be a symmetrical dot pattern of 16 points, 8 points, or 4 points which is a time representation of the received baseband signal. Any uncompensated distortion over the transmission path will cause each dot in the pattern to enlarge or otherwise show distortion. A typical visual eye pattern of a 4 point display is shown in the following diagram.



Typical Eye Pattern

Success Indicator

A second data quality indicator is provided for in all configurations except the 1200 baud non-V.27 modes. This signal provides a rough indication that the training has been successful and that data will be properly received. This "success" output (DSUCP) will go high during the last one to twenty milliseconds of receiver training, provided training has been successful. During the data mode (DRTMP low and D109 high), DSUCP will go high whenever 15 consecutive data marks or spaces are decoded at the receiver data output.

ADDITIONAL CAPABILITIES

The V27P/1 provides many additional capabilities germane to data communication system design and implementation. Capabilities such as local loopback, tone generation and detection, external clock facilities, and 300 bps FSK operation are briefly described in the following paragraphs.

Local Loopback Capability

A local loopback option is available for all half duplex and full duplex modem configurations. The Local Loopback Command (ILB) connects the transmitter's output through a buffer amplifier to the receiver input, thereby allowing a check of the local modem. The ILB command squelches the input to the receiver and loops the analog signal from the transmitter to the receiver input.

An internal pattern generator is also incorporated in the modem which can be used when no modem test set is available.

Tone Generation And Detection

The transmitter can be used to transmit single frequency tones for disabling echo suppressors or for system signaling. Tone that can be transmitted (selected through software control) are: 1100 Hz, 1300 Hz, 1650 Hz, 1850 Hz, 2025 Hz, and 2100 Hz. Other tones are also possible. The carrier frequency can be altered by selection of values for a binary bit stream.

External Data Clock

The data input to the transmitter can be clocked from an external source when the external clock is used as a reference input to the data clock's phase locked loop. By applying an external clock the reference input will cause the transmitter data clock to track the frequency and phase of the reference. The frequency of the reference clock must be within 100 ppm of nominal in order for the receiver's baud timing to properly track that of the transmitter. The reference clock can be equal to the nominal data clock frequency or be a subharmonic of it as long as the frequency tolerance is adhered to.

300 bps FSK Modem Operation

A CCITT T.30 compatible 300 bps FSK modem having characteristics of the CCITT V.21 channel 2 modulation system can also be configured. The FSK modem is capable of generating the 1100, 1300, 1650 and 1850 Hz tones.

SPECIFICATIONS

V27P/1 Specifications

DC Voltages			
Voltage	**Tolerance**	**Current (Typical)**	**Current (Max)**
+ 5 volt	±5%	135 ma	<200 ma
+12 volt	±5%	40 ma	< 70 ma
−12 volt	±5%	175 ma	<230 ma
Note: All voltages must have ripple ≤0.1 volts peak-to-peak.			
Environment			
Temperature:	Operating: 0°C to +60°C (32 to 140°F) Storage: −40°C to +80°C (−40 to 176°F) (Stored in heat sealed antistatic bag and shipping container)		
Relative Humidity:	Up to 90% noncondensing, or a wet bulb temperature up to 35°C, whichever is less.		
Mechanical			
Board Structure:	Single PC board with edge connector		
Mating Connector:	100 pin, edge connector, two sided, with 0.1 in (2.54 cm) centers Recommended Viking 3VH50/IJND5 or equivalent mating connector.		
Dimensions:	Width—9.188 in (23.338 cm) Depth—6.288 in (15.972 cm)		
Weight:	Less than 0.45 lbs (0.20 kg)		

7

Rockwell

R1212DS MODEM DEVICE SET (212A COMPATIBLE)

PRODUCT PREVIEW

PRODUCT PREVIEW

INTRODUCTION

The R1212DS is a high performance 1200/300 bps, full duplex modem device set. Utilizing state-of-the-art LSI and signal processing technology, the R1212DS provides the user with enhanced performance and reliability.

The R1212DS is ideal for designing products for data transmission over the 2-wire dial-up telephone network. CCITT V.22 A, B, Bell 212A and 103 compatible, the R1212DS can handle virtually all applications for full duplex 1200 bps (synchronous or asynchronous) and 0 to 300 bps asynchronous data transmission over the switched network.

Test features such as local analog loopback, remote digital loopback, and a self test configuration offer the user flexibility in creating a 1200 bps modem design customized for specific packaging and functional requirements.

For detail information, reference R1212 Modem Device Set Manual Order No. 652.

Product is available **NOW.**

FEATURES

- Bell 212A and 103 Compatible
- CCITT V.22 A, B Compatible
- Operation—2-Wire Full-Duplex
- Adaptive and Fixed Compromise Equalization
- Outstanding Performance Over Unconditioned Lines
- Test Configurations
  —Local Analog Loopback
  —Remote Digital Loopback
  —Self Test
- Busy Out Option
- Auto/Manual Answer
- Auto/Manual Dial
  —Tone or Pulse Dial
- Synchronous—1200 bps, 600 bps Fallback
- Asynchronous—1200 bps, 600 bps ±.01%, 0–300 bps
  —Character length 8, 9, 10, or 11 bits
- Eye Pattern Generation Capability
- Power Consumption—3 Watts typical
- Power Requirements: +5 Vdc, ±12 Vdc
- Guard Tone Generation (CCITT Configurations)
  —Selectable 1800 Hz and 550 Hz
- 3 Integrated Circuits Provide Total Modem Functions

Rockwell

R2424DS
MODEM DEVICE SET
2400 BPS FULL DUPLEX MODEM

PRODUCT PREVIEW

PRODUCT PREVIEW

INTRODUCTION

The Rockwell R2424DS is a high performance 2400/1200/300 bps full duplex modem device set. Utilizing state-of-the-art VLSI and signal processing technology, the R2424DS provides the user with enhanced performance and reliability.

The R2424DS is ideal for data transmission over the 2-wire dial-up telephone network. CCITT V.22 bis, V.22 A, B, Bell 212A and 103 compatible, the R2424DS can handle virtually all applications for full-duplex 2400 and 1200 bps fallback (synchronous and asynchronous) and 0 to 300 bps asynchronous data transmission over the switched network.

Test features such as local analog loopback, remote digital loopback, and a self test configuration offer the user flexibility in creating a 2400/1200 bps modem design customized for specific packaging and functional requirements.

For detail information, reference R2424 Modem Device Set Manual Order No. 651.

Product is available **NOW.**

FEATURES

- CCITT V.22 bis Compatible
- CCITT V.22 A, B Compatible
- Bell 212A and 103 Compatible
- Operation—2-Wire Full-duplex
- Adaptive and Fixed Compromise Equalization
- Outstanding Performance Over Unconditioned Lines
- Test Configurations
  —Local Analog Loopback
  —Remote Digital Loopback
  —Self Test
- Auto/Manual Answer
- Auto/Manual Dial
  —Tone or Pulse Dial
- Synchronous—2400 bps, 1200 bps, 600 bps ±.01%
- Asynchronous—2400 bps, 1200 bps, 600 bps +1%, −2.5%
  0–300 bps
  —Character length 8, 9, 10, or 11 bits
- Eye Pattern Generation Capability
- Power Consumption—3 Watts typical
- Guard Tone Generation (CCITT Configurations)
  —Selectable 1800 Hz and 550 Hz
- 3 Integrated circuits provide total modem functions

7

Rockwell

R24DP
2400 BPS MODEM
(201C COMPATIBLE)

PRODUCT PREVIEW

PRODUCT PREVIEW

INTRODUCTION

The R24 Data Pump is a synchronous, serial, 2400 bps modem designed for operation over dedicated unconditioned lines or with the general switched telephone network with appropriate line terminations, such as a Data Access Arrangement or transformer, provided externally.

The R24DP satisfies the telecommunications requirements specified in CCITT V.27 bis/ter and Bell 208 A/B for 4800 bps modems.

The R24DP is optimized for point-to-point applications and suitable for network applications where the optimum in data transfer is needed. Its small size (100 mm by 120 mm) and low power consumption (2.5W typical) offer the user flexibility in creating a 2400 bps modem customized for specific packaging and functional requirements.

Data can be transferred to and from the modem either serially over the CCITT V.24 interface or in parallel over the microprocessor bus interface.

The R24DP is a member of Rockwell's family of plug compatible modems.

Product availability is **APRIL, 1985.**

FEATURES

- Configurations
  —Bell 201C
  —CCITT V.26
- Half-Duplex (2-Wire), Full-Duplex (4-Wire)
- Ideal for Point-to-Point Applications
- Plug Compatible with Rockwell R96DP, R48DP, R96FT Modems
- Programmable Tone Generation
- Dynamic Range: −43 dBm to 0 dBm
- Equalization
  —Automatic Adaptive
  —Compromise Cable (Selectable)
  —Compromise Link (Selectable)
- DTE Interface: Two Alternate Ports
  —Microprocessor Bus
  —CCITT V.24 (RS-232-C Compatible)
- Diagnostics
  —Provides Telephone Line Quality Monitoring Statistics
- Programmable Transmit Output Level
- Loopbacks
  —Local Analog
  —Remote Analog
  —Remote Digital
- Power Consumption—2.5 Watts typical
- TTL and CMOS Compatible

SPECIFICATIONS

POWER REQUIREMENTS

+5 Vdc ±5% <500ma
+12 Vdc ±5% <20ma
−12 Vdc ±5% <80ma

ENVIRONMENTAL

Temperature: Operating 0 to 60°C
Storage −40 to 90°C
Relative Humidity: Up to 90%, noncondensing, or a wet bulb temperature up to 35°C, whichever is less.

Rockwell

R1212
1200 BPS FULL-DUPLEX MODEM

INTRODUCTION

The Rockwell R1212 is a high performance full-duplex 1200 bps modem. Using state-of-the-art VLSI and signal processing technology, the R1212 provides the user with enhanced performance and reliability on a single printed circuit board of less than 22 square-inches—overall size.

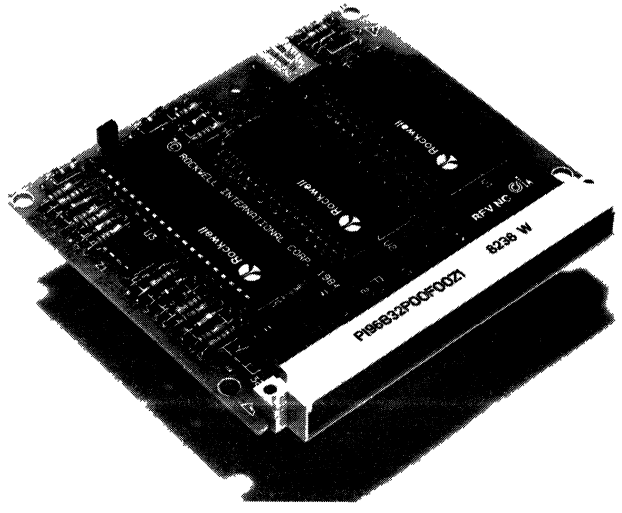
The R1212 modem is ideal for data transmission over the 2-wire dial-up telephone network. The direct-connect, auto dial/answer features are specifically designed for remote and central site computer applications. The bus interface allows easy integration into a personal computer, box modem, microcomputer, terminal or any other communications product that demands the utmost in reliability and performance.

The added test features, such as local analog loopback, remote digital loopback, and a self-test function, offer the user flexibility in creating a 1200 bps modem design customized for specific packaging and functional requirements.

Being CCITT V.22 A, B compatible, as well as Bell 212A and 103 compatible, this modem fits any application for full-duplex 1200 bps (synchronous and asynchronous) and 0 to 300 bps asynchronous data transmission over the general switched telephone network.

FEATURES

- CCITT V.22 A, B Compatible
- Bell 212A and 103 Compatible
- Synchronous: 1200 bps, 600 bps ±0.01%
- Asynchronous: 1200 bps, 600 bps +1%, −2.5%, 0-300 bps
  —Character length 8, 9, 10, or 11 bits
- DTE Interface
  —Functionally: Microprocessor Bus (Configuration/Control) and RS-232-C Interface (Data/Control)
  —Electrically: TTL Compatible
- Operation: 2-wire full-duplex
- Adaptive and Fixed Compromise Equalization
- Test Configurations:
  —Local Analog Loopback
  —Remote Digital Loopback
  —Self Test
- Auto/Manual Answer
- Auto/Manual Dial:
  —Tone or Pulse Dial
- Power Consumption: 3 Watts Typical
- Power Requirements: +5 Vdc, ±12 Vdc
- Plug-compatible member of new Rockwell modem line
- Two Versions: R1212DC (Direct Connect) with FCC approved DAA Part 68 Interface and R1212M (Module) without DAA



R1212 Full-Duplex Modem

7

TECHNICAL SPECIFICATIONS

TRANSMITTER CARRIER AND SIGNALING FREQUENCIES

Transmitter Carrier and Signaling Frequencies Specifications

Frequency	Specification (Hz ±0.01%)
V.22 low channel, Originate Mode	1200
V.22 high channel, Answer Mode	2400
Bell 212A high channel Answer Mode	2400
Bell 212A low channel Originate Mode	1200
Bell 103/113 Originating Mark	1270
Bell 103/113 Originating Space	1070
Bell 103/113 Answer Mark	2225
Bell 103/113 Answer Space	2025

TONE GENERATION

The specifications for tone generation are as follows:

1. **Answer Backtones:** The R1212 generates echo disabling tones both of the CCITT and Bell versions, as follows:
   a. CCITT: 2100 Hz ±15 Hz.
   b. Bell: 2225 Hz ±10 Hz.
2. **Guard Tones:** If GTS is low, an 1800 Hz guard tone frequency is selected; if GTS if high, a 553.846 Hz tone is employed. In accordance with the CCITT V.22 Recommendation, the level of transmitted power for the 1800 Hz guard tone is 6 ±1 dB below the level of the data power in the main channel. The total power transmitted to the line is the same whether or not a guard tone is enabled. If a 553.846 Hz guard is used, its transmitted power is 3 ±1 dB below the level of the main channel power, and again the overall power transmitted to the line will remain constant whether or not a guard tone is enabled. The device accomplishes this by reducing the main channel transmit path gain by .97 dB and 1.76 dB for the cases of the 1800 Hz and 553.846 Hz guard tones respectively.
3. **DTMF Tones:** The R1212 generates dual tone multi-frequency tones. When the transmission of DTMF tones are required, the CRQ and DTMF bits must be set to a 1. (see Interface Memory). When in this mode, the specific DTMF tones generated are decided by loading the dial digit register with the appropriate digit as shown in the following table:

Dial Digits/Tone Pairs

BCD				Dial Digits	Tone Pairs	
0	0	0	0	0	941	1336
0	0	0	1	1	697	1209
0	0	1	0	2	697	1336
0	0	1	1	3	697	1477
0	1	0	0	4	770	1209
0	1	0	1	5	770	1336
0	1	1	0	6	770	1477
0	1	1	1	7	852	1209
1	0	0	0	8	852	1336
1	0	0	1	9	852	1477
1	0	1	0	★	941	1209
1	0	1	1	Spare (B)	697	1633
1	1	0	0	Spare (C)	770	1633
1	1	0	1	Spare (D)	852	1633
1	1	1	0	#	941	1477
1	1	1	1	Spare (F)	941	1633

TONE DETECTION

The R1212 can detect tones in the 340 ±5 Hz to 640 ±5 Hz band.

Detection Level: 0 to −45 dBm
Response Time: 17 ±2 ms

SIGNALING AND DATA RATES

The signaling and data rates for the R1212 are defined in the table below:

Signaling and Data Rates

Operating Mode	Signaling Rate (Baud)	Data Rate
V.22:		
(Alternative A)		
Mode i	600	1200 bps ±0.01% Synchronous
Mode iii	600	600 bps ±0.01% Synchronous
(Alternative B)		
Mode i	600	1200 bps ±0.01% Synchronous
Mode iii	600	600 bps ±0.01% Synchronous
Mode ii	600	1200 bps Asynchronous
Mode iv		8, 9, 10, or 11 Bits Per Character 600 bps Asynchronous 8, 9, 10, or 11 Bits Per Character
Bell 212A	600	1200 bps ±0.01% Synchronous/Asychronous
	0 to 300	0 to 300 Bps Asynchronous

DATA ENCODING

The specifications for data encoding are as follows:

1. *1200 bps (V.22 and Bell 212A).* The transmitted data is divided into groups of two consecutive bits (dibits) forming a four-point signal structure.
2. *600 bps (V.22).* Each bit is encoded as a phase change relative to the phase preceding signal elements.

EQUALIZERS

The R1212 provides equalization functions that improve performance when operating over low quality lines.

Automatic Adaptive Equalizer—An automatic adaptive equalizer is provided in the receiver circuit for V.22 and Bell 212A configurations.

Fixed Compromise Equalizer—Compromise equalization is provided in the transmitter.

TRANSMITTED DATA SPECTRUM

After making allowance for the nominal specified compromise equalizer characteristic, the transmitted line signal has a frequency spectrum shaped by the square root of a 75 percent raised cosine filter. Similarly, the group delay of the transmitter output is within ±100 microseconds over the frequency range 900 to 1500 Hz (low channel) and 2100 to 2700 Hz (high channel).

SCRAMBLER/DESCRAMBLER

The R1212 incorporates a self-synchronizing scrambler/descrambler. In accordance with the CCITT V.22 and the Bell 212A recommendations. This function cannot be disabled.

RECEIVED SIGNAL FREQUENCY TOLERANCE

The receiver circuit of the R1212 can adapt to received frequency errors of up to ±7 Hz with less than a 0.2 dBm degradation in BER performance.

RECEIVE LEVEL

The receiver circuit of the R1212 satisfies all specified performance requirements for the received line signals from 0 dBm to −45 dBm. The received line signal is measured at the receiver analog input RXA.

RECEIVE TIMING

The R1212 provides a Receive Data Clock (RDCLK) output in the form of a (50 ±1% duty cycle) squarewave. The low to high transitions of this output coincide with the center of received data bits. The timing recovery circuit is capable of tracking a ±0.035% (relative) frequency error in the associated transmit timing source.

TRANSMIT LEVEL

The R1212M output control circuitry contains a variable gain buffer which reduces the modem output level. The R1212M can be strapped via the host interface memory to accomplish this.

PERMISSIVE/PROGRAMMABLE CONFIGURATIONS

The R1212M transmit level is +6 dBm to allow a DAA to be used. The DAA then determines the permissive or programmable configuration.

The R1212DC transmit level is strapped in the permissive mode so that the maximum output level is −10 dBm ±1.0 dBm.

TRANSMIT TIMING

The R1212 provides a Transmit Data Clock (TDCLK) output with the following characteristics:

1. *Frequency.* Selected data rate of 1200 or 600 Hz (±0.01%).
2. *Duty Cycle.* 50 ±1%.

Transmit Data (TXD) must be stable during the one microsecond periods immediately preceding and following the rising edge of TDCLK.

CLAMPING

The following clamp is provided with the R1212:

1. *Receive Data (RXD).* RXD is clamped to a constant mark (1) whenever RLSD is off.

RECEIVED LINE SIGNAL DETECTOR

The high and low channel thresholds are greater than −45 dBm (RLSD on) and less than −48 dBm (RLSD off) for V.22 and Bell 212A configurations.

DATA SET READY

The on condition of the R1212 output Data Set Ready (DSR) indicates that the modem is in the data transfer state. The off condition of DSR is an indication that the DTE is to disregard all signals appearing on the interchange circuits—except the calling indicator and the test signal. DSR will switch to the off state when in test state. The on condition of DSR indicates the following:

1. The modem is not in the talk state, i.e., an associated telephone handset is not in control of the line.
2. The modem is not in the process of automatically establishing a call via pulse or DTMF dialing.
3. The modem is generating an answer tone or detecting answer tone.
4. After ring indicate goes on, DSR waits at least two seconds before turning on to allow the telephone company equipment to be engaged.

DSR will go off 50 msec after DTR goes off or 50 msec plus a maximum of 4 sec when SSD is enabled. (Note: All time measurements without a tolerance have a ±0.5 ms tolerance.)

DATA TERMINAL READY

An on condition of DTR prepares the modem to be connected to the communications channel, and maintains the connection established by the DTE (manual answering) or internal (automatic answering) means. The off condition places the modem in the disconnect state.

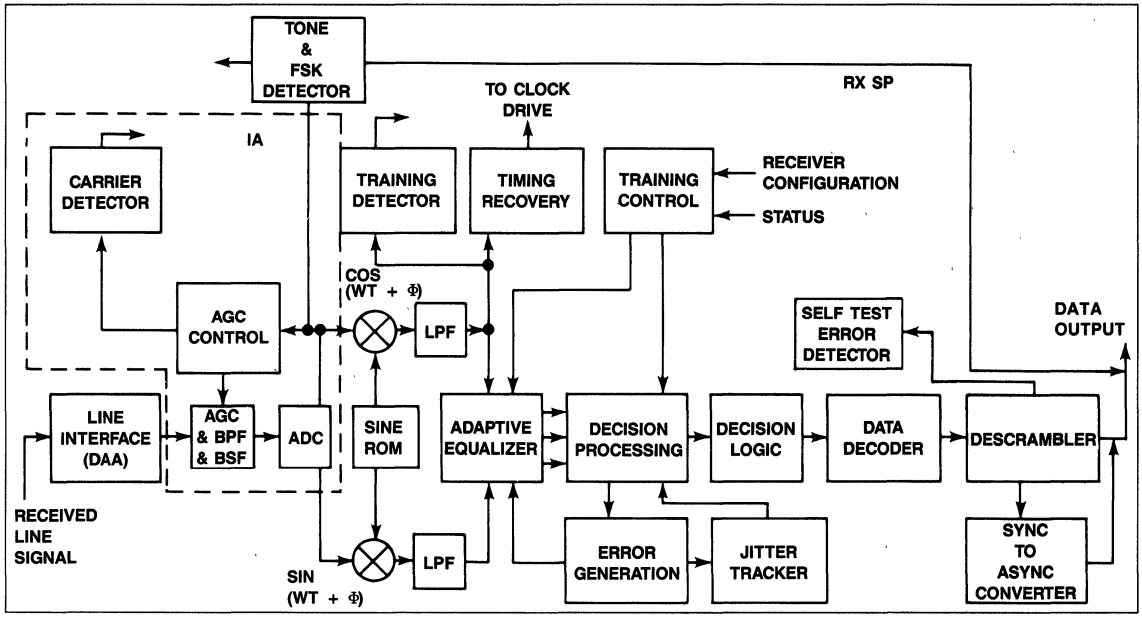
AUTOMATIC RECONFIGURATION

The R1212 is capable of automatically configuring itself to the compatibility of a remote modem. The R1212 can be in either the answer or originate mode for this to occur. The compatibilities

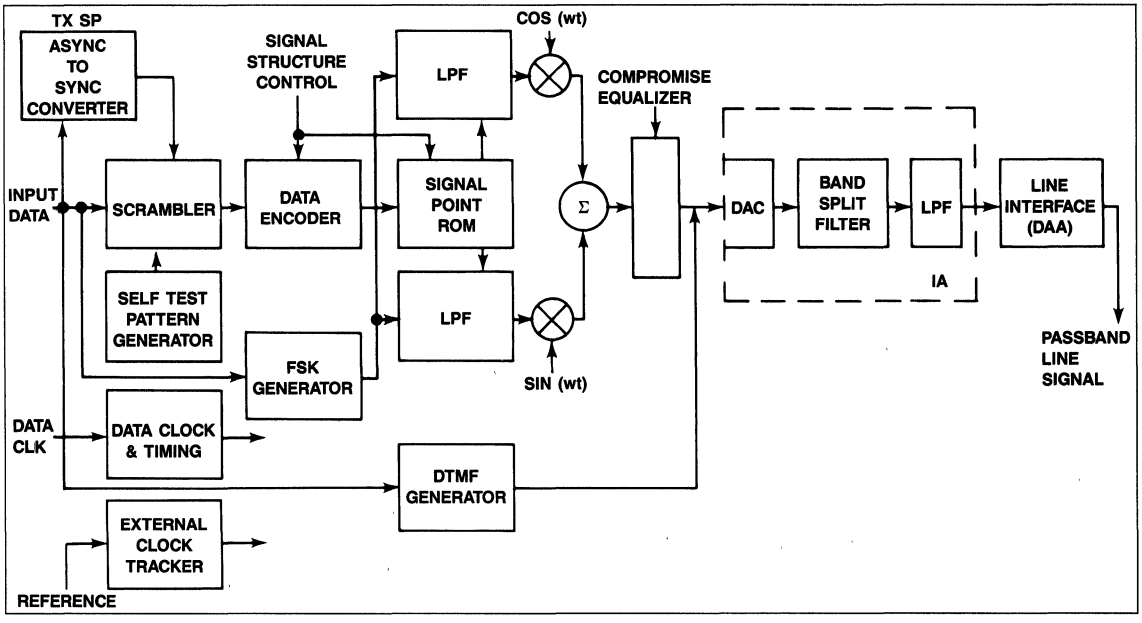
that the R1212 is limited to adapt to are V.22A/B, Bell 212, and Bell 103. If the R1212 is to originate in a specific configuration, the MODE bits must be set.

RECEIVE/TRANSMIT CIRCUITS

The receiver and transmitter circuits are defined in the following block diagrams:



R1212 Receiver/Equalizer Block Diagram



R1212 Transmitter Block Diagram

MODES OF OPERATION

The R1212 is capable of being operated in either a serial or a parallel mode of operation.

SERIAL MODE

The serial mode uses standard V.24 (RS-232-C compatible) signals to transfer channel data. An optional USART device (shown in the Functional Interconnect Diagram) illustrates this capability.

PARALLEL MODE

The R1212 has the capability of modem control via the microprocessor bus. Data transfer is maintained over the serial V.24 channel.

MODE SELECTION

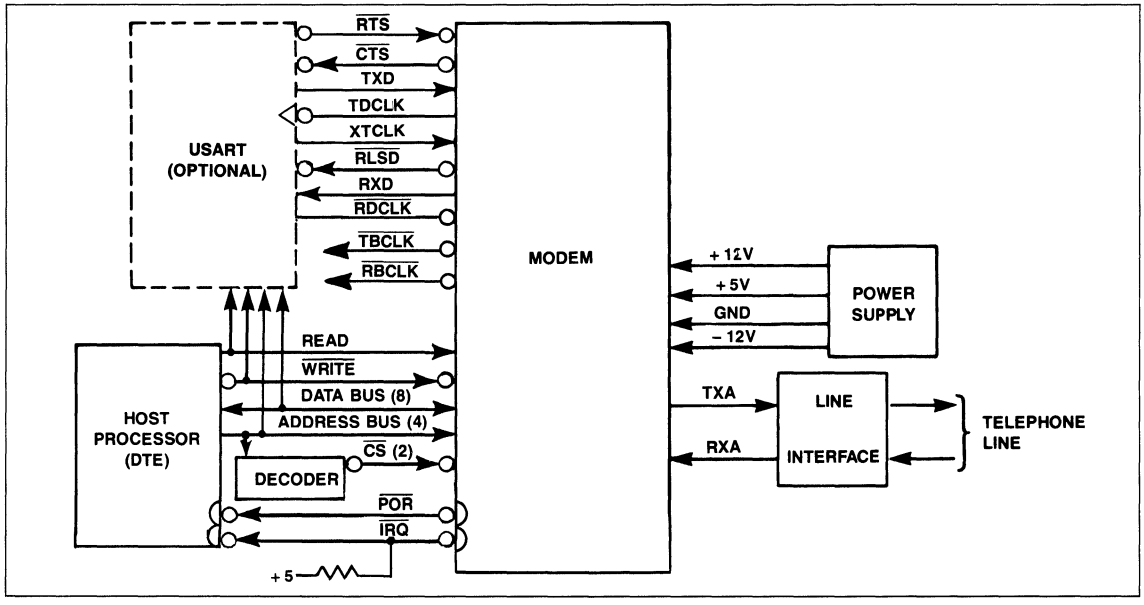
Selection of either the serial ($\overline{DTR}$, $\overline{RTS}$, $\overline{TLK}$, $\overline{ORG}$) or parallel (DTR, RTS, DATA, ORG) control is by means of the BUS bits ([0,1]:D:7). To enable the parallel control, the BUS bits must be set to a one. The modem automatically defaults to the serial mode at power-on. In either mode the R1212 is configured by the host processor via the microprocessor bus.

INTERFACE CRITERIA

The modem interface comprises both hardware and software circuits. Hardware circuits are assigned to specific pins in a 64-pin DIN connector. Software circuits are assigned to specific bits in a 32-byte interface memory.

HARDWARE CIRCUITS

Signal names and descriptions of the hardware circuits, including the microprocessor interface, are listed in the R1212 Hardware Circuits table. In the table, the column titled 'Type' refers to designations found in the Hardware Circuit Characteristics. The microprocessor interface is designed to be directly compatible with an 8080 microprocessor. With the addition of a few external logic gates, it can be made compatible with 6500, 6800, or 68000 microprocessors.



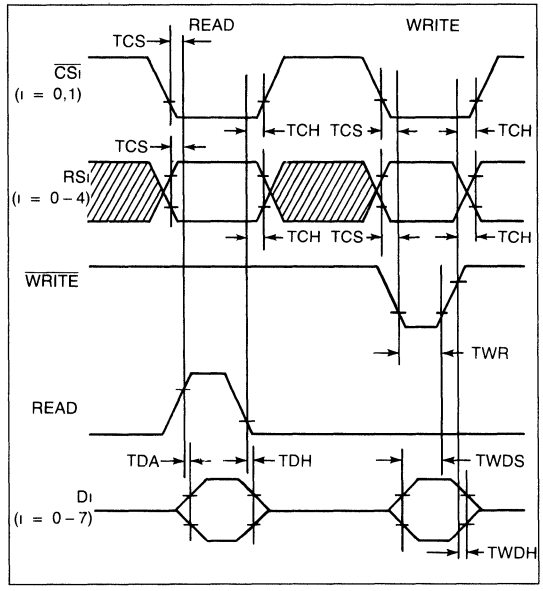
R1212 Functional Interconnect Diagram

7

R1212 Hardware Circuits

Name	Type	Pin No.	Description
A. OVERHEAD:			
Ground (A)	AGND	31C,32C	Analog Ground Return
Ground (D)	DGND	3C,8C,5A,10A	Digital Ground Return
+5 volts	PWR	19C,23C,26C,30C	+5 volt supply
+12 volts	PWR	15A	+12 volt supply
−12 volts	PWR	12A	−12 volt supply
$\overline{POR}$	I/OB	13C	Power-On-Reset
B. MICROPROCESSOR INTERFACE:			
D7	I/OA	1C	Data Bus (8 Bits)
D6	I/OA	1A	
D5	I/OA	2C	
D4	I/OA	2A	
D3	I/OA	3A	
D2	I/OA	4C	
D1	I/OA	4A	
D0	I/OA	5C	
RS3	IA	6C	Register Select (4 Bits)
RS2	IA	6A	
RS1	IA	7C	
RS0	IA	7A	
$\overline{CS0}$	IA	10C	Chip Select Receiver Baud Rate Device
$\overline{CS1}$	IA	9C	Chip Select Transmitter Sample Rate Device
$\overline{READ}$	IA	12C	Read Enable
$\overline{WRITE}$	IA	11A	Write Enable
$\overline{IRQ}$	OB	11C	Interrupt Request
C. V.24 INTERFACE:			
XTCLK	IB	22A	External Transmit Clock
TDCLK	OC	23A	Transmit Data Clock
$\overline{RDCLK}$	OC	21A	Receive Data Clock
$\overline{RTS}$	IB	25A	Request-to-Send
$\overline{CTS}$	OC	25C	Clear-to-Send
TXD	IB	24C	Transmit Data
RXD	OC	22C	Receive Data
$\overline{RLSD}$	OC	24A	Received Line Signal Detector
$\overline{DTR}$	IB	21C	Data Terminal Ready
$\overline{DSR}$	OC	20A	Data Set Ready
$\overline{RI}$	OC	18A	Ring Indicator
D. ANALOG SIGNALS (R1212M ONLY):			
RXA	IB	32A	Receive Analog Input
TXA	OC	31A	Transmit Analog Output
E. SIGNALS TO DAA (R1212M ONLY):			
$\overline{RD}$	IB	27A	Ring Detect
RCCT	OC	28A	Request Coupler Cut Through
$\overline{CCT}$	IB	29C	Coupler Cut Through
OH	OC	29A	Off-Hook Relay Control
F. ANCILLARY CIRCUITS:			
$\overline{TBCLK}$	OC	27C	Transmit Baud Clock
$\overline{RBCLK}$	OC	26A	Receive Baud Clock
$\overline{TLK}$	IC	28C	Talk (TLK = Data)
$\overline{ORG}$	IB	16C	Originate (ORG = Answer)

MICROPROCESSOR TIMING



Microprocessor Interface Timing Diagram

Critical Timing Requirements

Characteristic	Symbol	Min	Max	Units
$\overline{CSi}$, RSi setup time prior to Read or $\overline{Write}$	TCS	30	—	NS
Data Access time after Read	TDA	—	140	NS
Data hold time after Read	TDH	10	50	NS
CSi, RSi hold time after Read or $\overline{Write}$	TCH	10	—	NS
Write data setup time	TWDS	75	—	NS
Write data hold time	TWDH	10	—	NS
Write strobe pulse width	TWR	75	—	NS

HARDWARE CIRCUIT CHARACTERISTICS

Digital Interface Characteristics

Digital Interface Characteristics

Symbol	Parameter	Units	Input/Output Type							
			IA	IB	IC	OA	OB	OC	I/O A	I/O B
V_{IH}	Input Voltage, High	V	2.0 Min.	2.0 Min.	2.0 Min.				2.0 Min.	5.25 Max. 2.0 Min.
V_{IL}	Input Voltage, Low	V	0.8 Max.	0.8 Max.	0.8 Max.				0.8 Max.	0.8 Max.
V_{OH}	Output Voltage, High	V				2.4 Min.[1]			2.4 Min.[1]	2.4 Min.[3]
V_{OL}	Output Voltage, Low	V				0.4 Max.[2]	0.4 Max.[2]	0.4 Max.[2]	0.4 Max.[2]	0.4 Max.[2]
I_{IN}	Input Current, Leakage	μA	±2.5 Max.						±2.5 Max.[4]	
I_{OH}	Output Current, High	mA				−0.1 Max.				
I_{OL}	Output Current, Low	mA				1.6 Max.	1.6 Max.	1.6 Max.		
I_L	Output Current, Leakage	μA					±10 Max.			
I_{PU}	Pull-up Current (Short Circuit)	μA		−240 Max. −10 Min.	−240 Max. −10 Min.			−240 Max. −10 Min.		−260 Max. −100 Min.
C_L	Capacitive Load	pF	5	5	20				10	40
C_D	Capacitive Drive	pF				100	100	100	100	100
	Current Type		TTL	TTL w/Pull-up	TTL w/Pull-up	TTL	Open-Drain	Open-Drain w/Pull-up	3-State Transceiver	Open-Drain w/Pull-up

Notes
1. I Load = −100 μA
2. I Load = 1.6 mA
3. I Load = −40 μA
4. V_{IN} = 0.4 to 2.4 Vdc, V_{CC} = 5.25 Vdc

Analog Interface Characteristics

TXA — The (Type OC) transmitter output is a low impedance operational amplifier output in series with a 604 ohm resistor. In order to have a 0 dBm output, an external 600 ohm resistor to ground is required.

RXA — The (Type IB) receiver input impedance is 63.4K ohms ±5 percent.

Transmission Line Interface Characteristics

The R1212DC interface to the telephone line is the Tip and Ring leads. Lightning induced surge voltages and other hazardous voltages which may appear on the telephone line are limited to approximately 7V peak between the secondary leads of the line coupling transformer.

The DAA (R1212DC *only*) is bi-directional as required by 2-wire full-duplex circuits.

Connection to the telephone line interface pins of the R1212DC to the network are made via two RJ11 jacks. The pin designations are shown in the table below:

R1212DC Network Interface

Connection Type	Telco	Mnemonic	Function
	1		
VSOC	2		
RJ11	3	R	Ring-one side of telephone line
Jack	4	T	Tip-one side of telephone line
	5		
	6		

Ring Indicator — The R1212 provides a ring indicator ($\overline{RI}$) output; its low state indicates the presence of a ring signal on the line. The low condition appears approximately coincident with the on segment of the ring cycle (during rings) on the communication channel. (The ring signal cycle is typically two seconds on, four seconds off.) The high condition of the indicator output is maintained during the off segment of the ring cycle (between rings) and at all other times when ringing is being received. The operation of $\overline{RI}$ is not disabled by an off condition on Data Terminal Ready.

7

$\overline{RI}$ will respond to ring signals in the frequency range of 15.3 Hz to 68 Hz with voltage amplitude levels of 40 to 150 Vrms (applied across Tip and Ring), with the response times given in the following table:

RI Response Time

RI Transition	Response Time
Off-to-On	170 ms to ±50 ms
On-to-Off	110 ms to ±50 ms

This off-to-on (on-to-off) response time is defined as the time interval between the sudden connection (removal) of the ring signal across Tip and Ring and the subsequent on (off) transition $\overline{RI}$.

OH — The R1212M provides an output OH (Off-Hook) which indicates the state of the OH relay. A low condition on OH implies the OH relay is closed and the modem is connected to the telephone line. A high condition on OH implies the OH relay is open (i.e., the modem is on-hook). The delay between the low-to-high or high-to-low transition of OH and the subsequent close-to-open or open-to-close transition of the OH relay is 8 ms maximum.

$\overline{RD}$ — $\overline{RD}$ indicates to the R1212M by an on (low) condition that a ringing signal is present. The $\overline{RD}$ signal should not respond to momentary bursts of ringing less than 125 ms in duration, or to less than 40V rms, 15 to 68 Hz appearing across Tip and Ring with respect to ground.

RCCT — RCCT is used to request that a data transmission path through the DAA be connected to the telephone line. When RCCT goes off (low), the cut-through buffers are disabled and $\overline{CCT}$ should go off (high) within 1 msec. RCCT should be off during dialing but on for tone address signaling.

$\overline{CCT}$ — An on (low) signal to the $\overline{CCT}$ lead indicates to the R1212M that the data transmission path through the DAA is connected.

AUDIO INTERFACE INPUT IMPEDANCE CHARACTERISTICS

Audio Interface Input Impedance Characteristics

On/Off Hook	Measurement
On-Hook (DC)	The DC resistance between Tip and Ring, and between either Tip or Ring and signal ground is greater than 10 megohms for DC voltages up to 100 volts.
On-Hook (AC)	The on-hook AC impedance measured between Tip and Ring is less than 40K ohms (15.3 Hz minimum).
Off-Hook (DC)	Less than 200 ohms.
Off-Hook (AC)	600 ohms nominal when measured between Tip and Ring.

SOFTWARE CIRCUITS

The R1212 comprises two signal processor chips. Each of these chips contains 16 registers to which an external (host) microprocessor has access. Although these registers are within the modem, they may be addressed as part of the host processor's memory space. The host may read data out of or write data into these registers. The registers are referred to as interface memory. Registers in chip 0 update at the modem baud rate (bps) (except RAM Access and RAM Data Update where operation is at sample rate). Registers in chip 1 update at the sample rate (7200 bps).

When information in these registers is being discussed, the format Y:Z:Q is used. The chip is specified by Y(0 or 1), the register by Z(0 – F), and the bit by Q(0 – 7, 0 = LSB).

Status Control Bits

The operation of the R1212 is affected by a number of software control inputs. These inputs are written into registers within the interface memory via the host microprocessor bus. Bits designated by an 'X' are "Don't Care" inputs that can be set to either 1 or 0. Modem operation is monitored by various software flags that are read from interface memory via the host microprocessor bus. All status and control bits are defined in the Interface Memory table. Bits designated by an 'R' are reserved for modem use only and must not be changed by the host.

RAM Data Access

The R1212 provides the user with access to much of the data stored in the modem's memories. This data is useful for performing certain diagnostic functions.

Two RAM access registers are provided in the interface memory to allow user access to various RAM locations within chip 0 and chip 1. The access code stored in 0:F selects the source of data for the RAM data registers in chip 0 (0:5 through 0:2). Similarly, the access code stored in 1:F selects the source of data for registers 1:5 through 1:2. Reading is performed by first storing the desired access code in register 0:F (or 1:F). The data may then be read from 0:5 through 0:2 (or 1:5 through 1:2).

RAM Access Codes

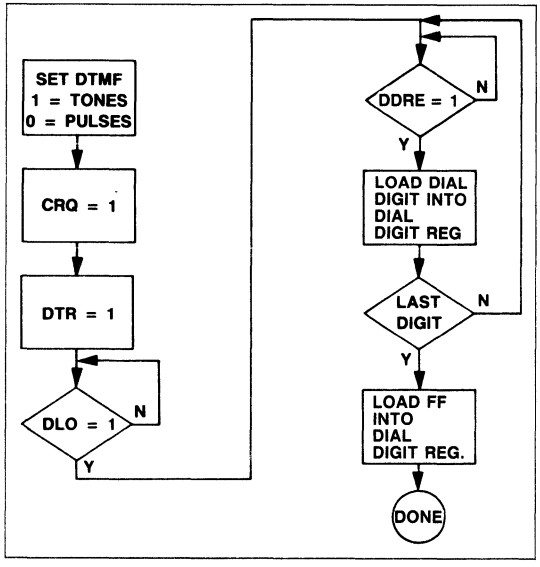
The RAM access codes defined in the following table allow the host processor to read diagnostic information within the modem.

RAM Access Codes (Chip 0)

Function	Access Code	Register No.
Self Test Error Counter	00	2,3 4,5
Equalizer Tap Coefficients	01–0D	2,3,4,5
Phase Error	10	2,3
Rotated Equalizer Output (Received Point Eye Pattern)	11	2,3,4,5
Rotated Angle	12	4,5
Low Pass Filter Output	40	2,3,4,5
Input Signal to Equalizer Tap Coefficients	41–4D	2,3,4,5
Decision Points (Ideal Eye Pattern)	51	2,3,4,5
Rotated Error	52	2,3,4,5
Equalizer Output	53	2,3,4,5
Demodulator Output	56	2,3,4,5

Auto Dial Sequence

The following flow chart defines the auto dial sequence via the microprocessor interface memory.



Auto Dial Sequence Flow Diagram

Note: The modem timing for the auto dialer accounts for inter-digit delay for pulses and tones.

The timing for the pulses and tones are as follows:

Pulses — Relay open 64 ms
Relay closed 36 ms
Interdigit delay 750 ms

Tones — Tone duration 71 ms
Interdigit delay 71 ms
Output Level 1.5 ±1 dBm

R1212 Receiver Interface Memory Chip 0 ($\overline{CS0}$)

Register \ Bit	7	6	5	4	3	2	1	0
F	RAM Access B							
E	IRQ	ENSI	NEWS	R	NEWC	R	R	R
D	BUS	CRQ	X	X	X	LCD	RSD	X
C	X	X	X	CHAR		X	X	X
B	X	X	X	X	X	X	X	AL
A	ERDL	RDL	DL	ST	MODE			
9	X	X	SPEED		X	X	X	X
8	TONE	X	X	X	X	X	TM	RLSD
7	R	R	R	R	R	R	R	R
6	R	R	R	R	R	R	R	R
5	RAM Data YBM							
4	RAM Data YBL							
3	RAM Data XBM							
2	RAM Data XBL							
1	R	R	R	R	R	R	R	R
0	R	R	R	R	R	R	R	R
Register / Bit	7	6	5	4	3	2	1	0

Note
(X) indicates user available.
(R) indicates reserved for modem use only.

R1212 Transmitter Interface Memory Chip 1 ($\overline{CS1}$)

Register \ Bit	7	6	5	4	3	2	1	0
F	RAM Access S							
E	IRQ	ENSI	NEWS	R	NEWC	DDEI	R	DDRE
D	BUS	CRQ	DATA	AAE	DTR	X	X	SSD
C	DSRA	TXCLK		CHAR		X	X	X
B	TX LEVEL			GTE	GTS	3DB	DTMF	AL
A	ERDL	RDL	DL	ST	MODE			
9	BRK	X	ORG	LL	RTS	CC	X	X
8	DLO	CTS	DSR	RI	X	X	X	X
7	R	R	R	R	R	R	R	R
6	R	R	R	R	R	R	R	R
5	RAM Data YSM							
4	RAM Data YSL							
3	RAM Data XSM							
2	RAM Data XSL							
1	R	R	R	R	R	R	R	R
0	Dial Digit Register							
Register / Bit	7	6	5	4	3	2	1	0

Note
(X) indicates user available.
(R) indicates reserved for modem use only.

7

R1212 Interface Memory Definitions

Mnemonic	Name	Memory Location	Description
AAE	Auto Answer Enable	1:D:4	When control bit AAE goes to a one, the modem will automatically answer when a singing signal is present on the line.
AL	Analog Loopback	(0,1):B:0	When control bit AL is a one, the modem is placed in (V.54 Loop 3) local analog loopback. In this loop, the transmitter's analog output is coupled to the receiver's analog input at a point near the modem's telephone line interface. An attenuator is introduced into the loop such that the signal level coupled into the receive path is attenuated 14 ±1 dBm.
BRK	Break	1:9:7	When control bit BRK goes to a one, the modem transmits 2M+3 bits of start polarity. (M is equal to the number of bits per character in the selected format.) BRK will reset to zero after the sequence is sent.
BUS	Bus Select	(0,1):D:7	When control bit BUS goes to a one, the modem is placed in the parallel control mode, and when zero the modem is configured for the serial control mode. BUS can be in either state to configure the modem.
CC	Controlled Carrier	1:9:2	When control bit CC goes to a one, the modem is placed in controlled carrier operation; and when zero, the modem is configured for constant carrier operation.
CHAR	Character Length Select	(0,1):C:(3,4)	These character length bits select either 8, 9, 10, or 11 bit characters, as shown below: **Configuration** — **Configuration Word** 8 bits — 0 0 9 bits — 0 1 10 bits — 1 0 11 bits — 1 1
CRQ	Call Request	(0,1):D:6	When control bit CRQ goes to a one, it places the transmitter in auto dial and the receiver in tone detect mode. The data placed in the dial digit is then treated as digits to be dialed. After the last digit has been dialed, FF (HEX) should be loaded into the dial digit register to tell the modem to go to the data state. CRQ in the transmitter (chip 1) when turned off causes the modem to go on-hook. Therefore, it should be on for the duration of the call and not turned off until it is desired to go on-hook. CRQ in the receiver (chip 0) must be turned off immediately after ringback is detected to put the modem in the data mode, otherwise no answerback tone will be detected.
CTS	Clear-to-Send	1:8:6	When status bit CTS is a one, it indicates to the terminal equipment that the modem will transmit any data which are present at TXD. CTS response times from an on or off condition of RTS are shown below: **CTS Transitions** — **Constant Carrier** — **Controlled Carrier** Off to On — <2 ms — 275 ms On to Off — <2 ms — <2 ms
DATA	Talk/Data	1:D:5	When control bit DATA goes to a one, it places the modem in data state and when zero in the talk state.
DDEI	Dial Digit Empty Interrupt	1:E:2	When control bit DDEI goes to a one, it causes an interrupt to occur when the dial digit register (1:0) is empty (DDRE = 1).
DDR	Dial Digit Register	1:0:(0–7)	DDR is used to load the digits to be dialed. Example: If a 4 is to be dialed, a 04 (HEX) should be loaded. This action also causes the interrupt to be cleared. DDR is a write only register.
DDRE	Dial Digit Register Empty	1:E:0	When status bit DDRE is a one, it indicates that the dial digit register is empty and can be loaded with a new digit to be dialed. After the register is loaded, DDRE goes to zero.
DL	Digital Loopback (Manual)	(0,1):A:5	When control bit DL is a one, the modem is manually placed in remote digital loopback. DL should be set during the data mode. DSA and CTS will be at zero. The local modem can then be tested from the far-end by using the terminal equipment at the far-end to transmit a test pattern and examine the looped data. At the far-end modem, all interface circuits behave normally as in the data mode. At the conclusion of the test, DL must be reset to zero. The local modem will then return to the normal data mode with control reverting the DTE's, DTR.

R1212 Interface Memory Definitions (Continued)

Mnemonic	Name	Memory Location	Description
DLO	Data Line Occupied	1:8:7	When status bit DLO is a one, it indicates that the modem is in the auto dial state, i.e., CRQ is at a one and the modem is off-hook and ready to dial.
DSR	Data Set Ready	1:8:5	When status bit DSR is a one, it indicates that the answerback tone has been detected, the modem handshake has begun and that the data state will follow. DSR alone should not be used to indicate that the communication channel has been completely established. DSR in conjunction with CTS and RLSD will determine this. DSR will be at zero in all test states (except optionally for analog loopback) and when the channel is being used for voice communication (talk).
DSRA	Data Set Ready In Analog Loopback	1:C:7	When control bit DSRA goes to a one, it causes DSR to be set to a one during analog loopback.
DTMF	Touch Tones/ Pulse Dialing	1:B:1	When control bit DTMF goes to a one, it tells the modem to auto dial using tones, and when zero the modem will dial using pulses.
DTR	Data Terminal Ready	1:D:3	Control bit DTR must be a one, before the modem will enter the data state, either manually or automatically. DTR must also be at a one in order for the modem to automatically answer an incoming call.
ENSI	Enable New Status Interrupt	(0,1):E:6	When control bit ENSI goes to a one, it causes an interrupt to occur when the status bits in registers (0:[8,9]) and (1:8) are updated. (NEWS = 1)
ERDL	Enable Response to Remote Digital Loopback	(0,1):A·7	When control bit ERDL goes to a one, it enables the modem to respond to another modem's remote digital loopback request, thus going into loopback.
GTE	Guard Tone Enable	1:B:4	When control bit GTE goes to a one, it causes the specified guard tone to be transmitted (CCITT Configurations only).
GTS	Guard Tone Select	1:B:3	When control bit GTS goes to zero, it selects the 1800 Hz tone and when a one it selects the 550 Hz tone.
IRQ	Interrupt Request	(0,1):E:7	When status bit IRQ is a one, it indicates that an interrupt has been generated.
LCD	Loss of Carrier Disconnect	0:D:2	When control bit LCD goes to a one, the modem terminates a call when a loss of received carrier energy is detected after 400 msec. After the first 40 ms of loss of carrier, RLSD goes off. 360 ms later if no carrier is detected, CTS goes off. LCD is not disabled in leased line operation.
LL	Leased Line	1:9·4	When control bit LL goes to a one, it places the modem in leased line operation; a when zero switched line operation.
MODE	Mode Select	(0,1):A:(0–3)	These bits select the compatibility at which the modem is to operate, as shown below: **Configuration** / **Configuration Word** Bell 212A 1200 Sync. — 0 0 1 0 Bell 212A 1200 Async. — 0 0 1 1 Bell 212A 300 Async. — 0 1 0 0 V.22A 1200 Sync. — 1 0 0 0 V.22B 1200 Async. — 1 0 0 1 V.22A 600 Sync. — 1 0 1 0 V.22B 600 Async. — 1 0 1 1
NEWC	New Configuration	(0,1):E:3	When status bit NEWC is a one, it tells the modem that a new configuration has been written into the configuration registers. The modem will then read the configuration registers and then reset NEWC. NEWC must be set after a new configuration has been written into the following registers :(0:[A–D]) and (1:[9–D]). The remaining registers do not require the use of NEWC to tell the modem that new data was written into them.

R1212 Interface Memory Definitions (Continued)

Mnemonic	Name	Memory Location	Description
NEWS	New Status	(0,1):E:5	When status bit NEWS is a one, it tells the user that there has been a change of status in the status registers. The user must write a zero into NEWS to reset it. This action also causes the interrupt to be cleared.
ORG	Originate/Answer	1:9:5	When status bit ORG is a one, it tells the modem that it is originating a call and when a zero answering a call. (This is only valid in manual originate/answer and analog loopback.)
(None)	RAM Access B	0:F:0-7	Contains the RAM access code used in reading RAM locations in chip 0 (baud rate device).
(None)	RAM Access S	1:F:0-7	Contains the RAM access code used in reading RAM locations in chip 1 (sample rate device).
(None)	RAM Data XBL	0:2:0-7	Least significant byte of 16-bit word X used in reading RAM locations in chip 0.
(None)	RAM Data XBM	0:3:0-7	Most significant byte of 16-bit word X used in reading RAM locations in chip 0.
(None)	RAM Data XSL	1:2:0-7	Least significant byte of 16-bit word X used in reading RAM locations in chip 1.
(None)	RAM Data XSM	1:3:0-7	Most significant byte of 16-bit word X used in reading RAM locations in chip 1.
(None)	RAM Data YBL	0:4:0-7	Least significant byte of 16-bit word Y used in reading RAM locations in chip 0.
(None)	RAM Data YBM	0:5:0-7	Most significant byte of 16-bit word Y used in reading RAM locations in chip 0.
(None)	RAM Data YSL	1:4:0-7	Least significant byte of 16-bit word Y used in reading RAM locations in chip 1.
(None)	RAM Data YSM	1:5:0-7	Most significant byte of 16-bit word Y used in reading RAM locations in chip 1.
RDL	Remote Digital Loopback	(0,1).A:6	When control bit RDL goes to a one, it causes the modem to initiate a request for the remote modem to go into digital loopback.
RI	Ring Indicator	1:8:4	When status bit RI is a one, it indicates that a ringing signal is being detected.
RLSD	Received Line Signal Detector	0:8:0	When status bit RLSD is a one, it indicates that the carrier has successfully been received. RLSD will not respond to the 550, 1800, 2100, or 2225 Hz tones. RLSD response times are given below: **RLSD Transitions[1]** / **Constant Carrier** / **Controlled Carrier** Off to On: 40 to 65 ms / 40 to 65 ms On to Off: 40 to 65 ms / 40 to 65 ms **Note:** 1. After handshake has occurred.
RSD	Receive Space Disconnect	0:D:1	When control bit RSD goes to a one, it causes the modem to go on-hook after receiving approximately 1.6 seconds of continuous spaces.
RTS	Request-to-Send	1:9:3	When control bit RTS goes to a one, it allows the modem to transmit data when CTS becomes active. Responses to RTS are shown below: Assume DTR is on, Talk/Data is set to Data (CRQ or AAE is set for a dial line) and the modem is connected to the line (off-hook). **Leased or Dial Line[1]** / **RTS Off** / **RTS On** Controlled Carrier: CTS Off, Carrier Off / Carrier On, 275 ms Scambled 1's Transmitted, CTS On Constant Carrier: CTS Off, Carrier On, Scrambled 1's Transmitted / CTS On, Carrier On, Data Transmitted **Note:** 1. After handshake is complete. For ease of use in constant carrier mode, RTS should be turned on the same time as DTR.
SPEED	Speed Indication	0:9:(4,5)	00 = 300 bps 10 = 1200 bps 01 = 600 bps
SSD	Send Space Disconnect	1:D:0	When control bit SSD goes to a one, it causes the modem to transmit approximately 4 seconds of spaces before disconnecting, when DTR is at zero.

R1212 Interface Memory Definitions (Continued)

Mnemonic	Name	Memory Location	Description
ST	Self Test (Continued)	(0,1):A:4	*Self Test End-to-End* Upon activation of self-test an internally generated data pattern of alternate binary ones and zeros (reversals) at the selected bit rate are applied to the scrambler. An error detector, capable of identifying errors in a stream of reversals are connected to the output of the descrambler. *Self Test with Loop 3* Loop 3 is applied to the modem as defined in recommendation V.54. Self-test is activated and DCE operation is as in the end-to-end test. In this test DTR is ignored. *Self Test with Loop 2* The modem is conditioned to instigate a loop 2 at the remote modem as specified in recommendation V.54. Self-test is activated and DCE operation is as in the end-to-end test.
3 DB	3 dB Loss to Receive Signal	1:B:2	When control of bit 3 DB is a one, it attenuates the received signal 3 dB. This is only used if the R1212M will see 0 dBm or greater line signal at the receiver input. Insertion of the 3 dB loss will then prevent saturation. This bit is not needed with the R1212DC.
TM	Test Mode	0:8:1	When status bit TM is a one, it indicates that the modem has completed the handshake and is in one of the following test modes: AL, RDL, or DL.
TONE	Tone Detect	0:8:7	TONE follows the energy detected in the 340 to 640 Hz frequency band. The user must determine which tone is present on the line by determining the duty cycle of the TONE bit. TONE is active only when CRQ in chip 0 is a one.
TXCLK	Transmit Clock Select	1:C:(5,6)	TXCLK allows the user to designate the origin of the transmitter data clock, as shown below: **Transmit Clock** — **Configuration Word** Internal — 0 0 Not Used — 0 1 External — 1 0 Slave — 1 1
TX LEVEL	Transmit Level	1:B:(5–7)	TX LEVEL allows the user to change the R2424M transmitter output level, assuming the modem is transmitting into a 600 ohm load. **Transmit Level (±1.0 dBm)** — **Configuration Word** 0 dBm — 0 0 0 –2 dBm — 0 0 1 –4 dBm — 0 1 0 –6 dBm — 0 1 1 –8 dBm — 1 0 0 –10 dBm — 1 0 1 –12 dBm — 1 1 0 –14 dBm — 1 1 1

POWER-ON INITIALIZATION

When power is applied to the R1212, a period of 50 to 300 ms is required for power supply settling. The power-on-reset signal (POR) remains low during this period. Approximately 10 ms after the low to high transition of POR, the modem is ready to be configured, and RTS may be activated. If the 5 Vdc power supply drops below 3.5 Vdc for more than 30 msec, the POR cycle is repeated.

At POR time the modem automatically defaults to Bell 212A 1200 bps, answer state using serial start-stop data 10 bits per character, constant carrier, dial line.

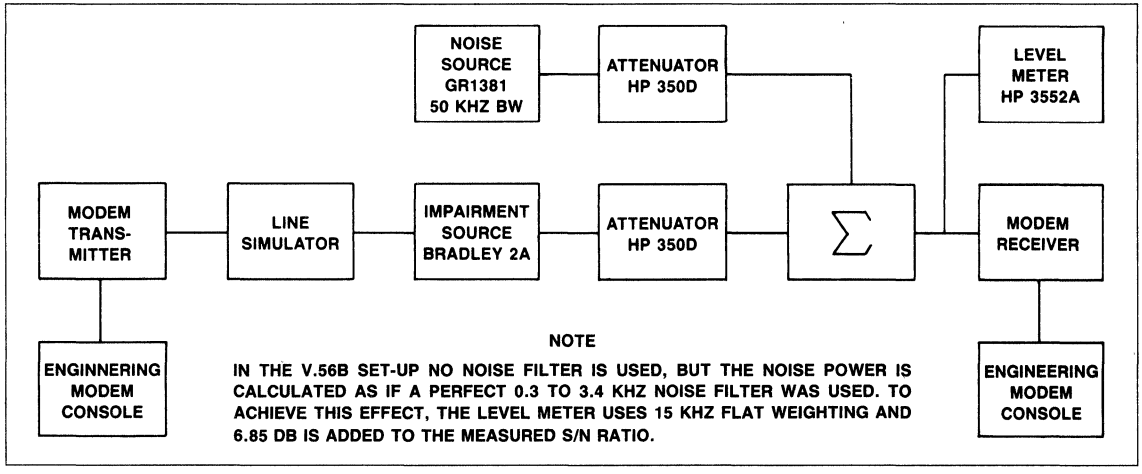
POR can be connected to a user supplied power-on-reset signal in a wire-or configuration. A low active pulse of 3 μsec or more applied to the POR pin causes the modem to reset. The modem is ready to be configured 10 msec after the low active pulse is removed from POR.

PERFORMANCE

Whether functioning as a V.22, or Bell 212A type modem, and regardless of simulated line condition or introduced line impairment, the R1212 provides unexcelled high performance to the user.

BIT ERROR RATES

The Bit Error Rate (BER) performance of the R1212 is specified for a test configuration conforming to that specified in CCITT Recommendation V.56, except with regard to the placement of the filter used to bandlimit the white noise source. Bit error rates are measured at a received line signal level of −43 dBm.



BER Performance Test Set-up

GENERAL SPECIFICATIONS

Power

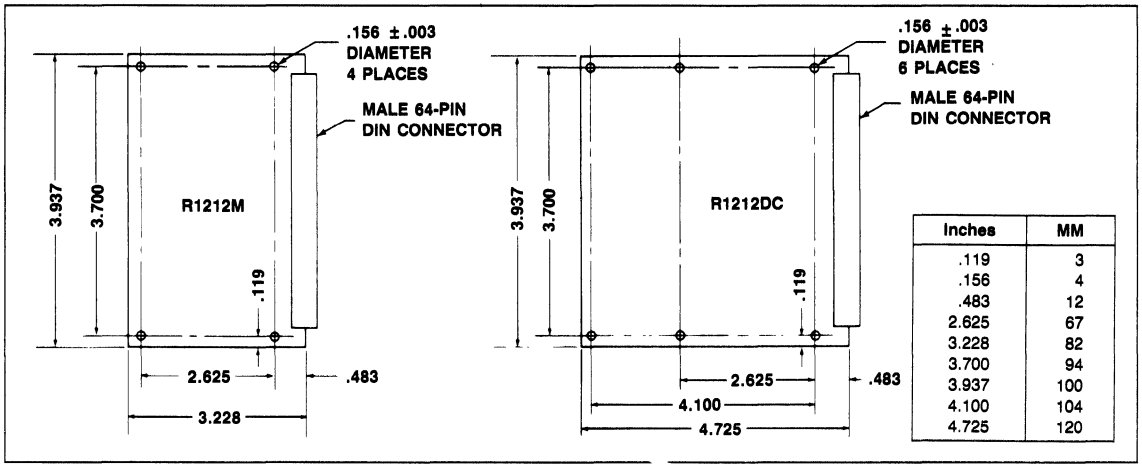
Voltage	Tolerance	Current (Max)
+5 Vdc	±5%	<500 mA
+12 Vdc	±5%	<10 mA
−12 Vdc	±5%	<50 mA
Note: All voltages must have ripple ≤0.1 volts peak-to-peak.		

Environmental

Parameter	Specification
Temperature Operating— Storage—	 0°C to +60°C (32 to 140°F) −40°C to +80°C (−40 to 176°F)
Relative Humidity	Up to 90% noncondensing, or a wet bulb temperature up to 35°C, whichever is less.
Altitude	−200 to +10,000 feet
*PCB's are stored in heat sealed antistatic bags and shipping containers	

Mechanical

Board Structure	Single PC board with right angle male DIN connector.
Mating Connector	Female 3 row 64 pin Euroconnector (DIN) with rows A and C populated. Recommended mating connector: Winchester 96S-6043-0531-1 or equivalent.
PCB Dimensions R1212DC Version R1212M Version	 Width 3.94 in. (100 mm) × Length 4.725 in. (120 mm) × Height 0.75 in. (19 mm) Width 3.94 in. (100 mm) × Length 3.23 in. (82 mm) × Height 0.40 in. (10 mm)
Weight	Less than 0.45 lbs. (0.20 kg.)
Lead Extrusion	0.100 in. (2.54 mm) max.



Inches	MM
.119	3
.156	4
.483	12
2.625	67
3.228	82
3.700	94
3.937	100
4.100	104
4.725	120

R1212 Printed Circuit Board Dimensions

INSTALLATION

IMPORTANT NOTICE TO USER

The R1212DC contains protective circuitry registered with the Federal Communications Commission (FCC) Part 68 to allow direct connection to the switched telephone network. To comply with the FCC regulations the following is required:

1. All direct connections to the telephone lines shall be made through standard plugs and telephone company provided jacks.
2. It is prohibited to connect the modem to pay telephones or party lines.
3. You are required to notify the local telephone company prior to the connection and upon final disconnection of the modem. You must supply to the telephone company the make, model number, FCC registration number, ringer equivalence and particular line to which the connection is to be made. If the proper jacks are not available, you must order the type of jacks to be used from the telephone company.
4. You should disconnect the modem from the telephone line if it appears to be malfunctioning. Reconnect it only when it can be determined that the telephone line is the source of trouble. If the modem needs repair, return it to Rockwell International. This applies to equipment both in and out of warranty. Do not attempt to repair the unit as this will violate FCC rules.
5. The modem contains protective circuitry to prevent harmful voltages from being transmitted to the telephone network. If however such harmful voltages do occur, then the telephone company shall:
   - Promptly notify you of the discontinuance.
   - Afford you the opportunity to correct the situation which caused the discontinuance.

   The FCC requires that the following label be prominently displayed on an outside surface of the OEM's end product.
   - Unit contains Registered Protective Circuitry which complies with Part 68 of FCC Rules.
   - FCC Registration Number: Applied For
   - Ringer Equivalence: 0.5

   Size of the label should be such that all the required information is legible without magnification.

Rockwell

R1212/U
1200 BPS FULL-DUPLEX MODEM WITH INTERNAL USART

INTRODUCTION

The Rockwell R1212/U is a high performance full-duplex 1200 bps modem. Using state-of-the-art VLSI and signal processing technology, the R1212/U provides the user with enhanced performance and reliability on a single printed circuit board of less than 19 square-inches—overall size.

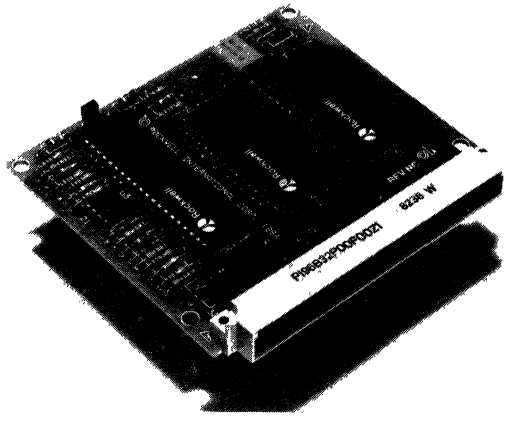
The R1212/U modem is ideal for data transmission over the 2-wire dial-up telephone network. The direct-connect, auto dial/answer features are specifically designed for remote and central site computer applications. The bus interface allows easy integration into a personal computer, box modem, microcomputer, terminal or any other communications product that demands the utmost in reliability and performance.

The added test features, such as local analog loopback, remote digital loopback, and a self-test function, offer the user flexibility in creating a 1200 bps modem design customized for specific packaging and functional requirements.

Being CCITT V.22 A, B compatible, as well as Bell 212A and 103 compatible, this modem fits any application for full-duplex 1200 bps (synchronous and asynchronous) and 0 to 300 bps asynchronous data transmission over the general switched telephone network.

FEATURES

- CCITT V.22 A, B Compatible
- Bell 212A and 103 Compatible
- Synchronous: 1200 bps, 600 bps ±0.01%
- Asynchronous: 1200 bps, 600 bps +1%, −2.5%, 0-300 bps
  —Character length 8, 9, 10, or 11 bits
- USART Internal
- DTE Interface
  —Functionally: Microprocessor Bus (Data/Configuration/Control)
  RS-232-C Interface (Data/Control)
  —Electrically: TTL Compatible
- Operation: 2-wire full-duplex
- Adaptive and Fixed Compromise Equalization
- Test Configurations:
  —Local Analog Loopback
  —Remote Digital Loopback
  —Self Test
- Auto/Manual Answer
- Auto/Manual Dial:
  —Tone or Pulse Dial
- Power Consumption: 3 Watts typical
- Power Requirements: +5 Vdc, ±12 Vdc
- Plug-compatible member of new Rockwell modem line
- Two Versions: R1212DC/U (Direct Connect) with FCC approved DAA Part 68 Interface and R1212M/U (Module) without DAA



R1212/U Full-Duplex Modem

TECHNICAL SPECIFICATIONS

TRANSMITTER CARRIER AND SIGNALING FREQUENCIES

Transmitter Carrier and Signaling Frequencies Specifications

Frequency	Specification (Hz ±0.01%)
V.22 low channel, Originate Mode	1200
V.22 high channel, Answer Mode	2400
Bell 212A high channel Answer Mode	2400
Bell 212A low channel Originate Mode	1200
Bell 103/113 Originating Mark	1270
Bell 103/113 Originating Space	1070
Bell 103/113 Answer Mark	2225
Bell 103/113 Answer Space	2025

TONE GENERATION

The specifications for tone generation are as follows:

1. **Answerback Tones:** The R1212/U is capable of generating echo disabling tones for both of the CCITT and Bell versions, as follows:
   a. CCITT: 2100 Hz ±15 Hz.
   b. Bell: 2225 Hz ±10 Hz.
2. **Guard Tones:** If GTS is low, an 1800 Hz guard tone frequency is selected; if GTS if high, a 553.846 Hz tone is employed. In accordance with the CCITT V.22 Recommendation, the level of transmitted power for the 1800 Hz guard tone is 6 ±1 dB below the level of the data power in the main channel. The total power transmitted to the line is the same whether or not a guard tone is enabled. If a 553.846 Hz guard is used, its transmitted power 3 ±1 dB below the level of the main channel power, and again the overall power transmitted to the line will remain constant whether or not a guard tone is enabled. The device accomplishes this by reducing the main channel transmit path gain by .97 dB and 1.76 dB for the cases of the 1800 Hz and 553.846 Hz guard tones respectively.
3. **DTMF Tones:** The R1212/U generates dual tone multi-frequency tones. When the transmission of DTMF tones are required, the CRQ and DTMF bits must be set to a 1. (see Interface Memory). When in this mode, the specific DTMF tones generated are decided by loading the transmitter data register with the appropriate digit as shown in the following table:

Dial Digits/Tone Pairs

BCD				Dial Digits	Tone Pairs	
0	0	0	0	0	941	1336
0	0	0	1	1	697	1209
0	0	1	0	2	697	1336
0	0	1	1	3	697	1477
0	1	0	0	4	770	1209
0	1	0	1	5	770	1336
0	1	1	0	6	770	1477
0	1	1	1	7	852	1209
1	0	0	0	8	852	1336
1	0	0	1	9	852	1477
1	0	1	0	★	941	1209
1	0	1	1	Spare (B)	697	1633
1	1	0	0	Spare (C)	770	1633
1	1	0	1	Spare (D)	852	1633
1	1	1	0	#	941	1477
1	1	1	1	Spare (F)	941	1633

TONE DETECTION

The R1212/U can detect tones in the 340 ±5 Hz to 640 ±5 Hz band.

Detection Level: 0 to −45 dBm
Response Time: 17 ±2 ms

SIGNALING AND DATA RATES

The signaling and data rates for the R1212/U are defined in the table below:

Signaling and Data Rates

Operating Mode	Signaling Rate (Baud)	Data Rate
V.22.		
(Alternative A)		
Mode i	600	1200 bps ±0.01% Synchronous
Mode iii	600	600 bps ±0.01% Synchronous
(Alternative B)		
Mode i	600	1200 bps ±0.01% Synchronous
Mode iii	600	600 bps ±0.01% Synchronous
Mode ii	600	1200 bps Asynchronous
Mode iv		8, 9, 10, or 11 Bits Per Character 600 bps Asynchronous 8, 9, 10, or 11 Bits Per Character
Bell 212A	600	1200 bps ±0.01% Synchronous/Asychronous
	0 to 300	0 to 300 Bps Asynchronous

7

DATA ENCODING

The specifications for data encoding are as follows:

1. *1200 bps (V.22 and Bell 212A).* The transmitted data is divided into groups of two consecutive bits (dibits) forming a four-point signal structure.
2. *600 bps (V.22).* Each bit is encoded as a phase change relative to the phase preceding signal elements.

EQUALIZERS

The R1212/U provides equalization functions that improve performance when operating over low quality lines:

Automatic Adaptive Equalizer—An automatic adaptive equalizer is provided in the receiver circuit for V.22 and Bell 212A configurations.

Fixed Compromise Equalizer—Compromise equalization is provided in the transmitter.

TRANSMITTED DATA SPECTRUM

After making allowance for the nominal specified compromise equalizer characteristic, the transmitted line signal has a frequency spectrum shaped by the square root of a 75 percent raised cosine filter. Similarly, the group delay of the transmitter output is within ±100 microseconds over the frequency range 900 to 1500 Hz (low channel) and 2100 to 2700 Hz (high channel).

SCRAMBLER/DESCRAMBLER

The R1212/U incorporates a self-synchronizing scrambler/descrambler in accordance with the CCITT V.22 and the Bell 212A recommendations. This function cannot be disabled.

RECEIVED SIGNAL FREQUENCY TOLERANCE

The receiver circuit of the R1212/U can adapt to received frequency errors of up to ±7 Hz with less than a 0.2 dBm degradation in BER performance.

RECEIVE LEVEL

The receiver circuit of the R1212/U satisfies all specified performance requirements for the received line signals from 0 dBm to −45 dBm. The received line signal is measured at the receiver analog input RXA.

RECEIVE TIMING

The R1212/U provides a Receive Data Clock (RDCLK) output in the form of a (50 ±1% duty cycle) squarewave. The low to high transitions of this output coincide with the center of received data bits. The timing recovery circuit is capable of tracking a ±0.035% (relative) frequency error in the associated transmit timing source.

TRANSMIT LEVEL

The R1212M/U output control circuitry contains a variable gain buffer which reduces the modem output level. The R1212M/U can be strapped via the host interface memory to accomplish this.

PERMISSIVE/PROGRAMMABLE CONFIGURATIONS

The R1212M/U transmit level is +6 dBm to allow a DAA to be used. The DAA then determines the permissive or programmable configuration.

The R1212DC/U transmit level is strapped in the permissive mode so that the maximum output level is −10 dBm ±1.0 dBm.

TRANSMIT TIMING

The R1212/U provides a Transmit Data Clock (TDCLK) output with the following characteristics:

1. *Frequency.* Selected data rate of 1200 or 600 Hz (±0.01%).
2. *Duty Cycle.* 50 ±1%.

Transmit Data (TXD) must be stable during the one microsecond periods immediately preceding and following the rising edge of TDCLK.

CLAMPING

The following clamp is provided with the R1212/U:

1. *Receive Data (RXD).* RXD is clamped to a constant mark (1) whenever RLSD is off.

RECEIVED LINE SIGNAL DETECTOR

The high and low channel thresholds are greater than −45 dBm (RLSD on) and less than −48 dBm (RLSD off) for V.22 and Bell 212A configurations.

DATA SET READY

The on condition of the R1212/U output Data Set Ready (DSR) indicates that the modem is in the data transfer state. The off condition of DSR is an indication that the DTE is to disregard all signals appearing on the interchange circuits—except the calling indicator and the test signal. DSR will switch to the off state when in test state. The on condition of DSR indicates the following:

1. The modem is not in the talk state, i.e., an associated telephone handset is not in control of the line.
2. The modem is not in the process of automatically establishing a call via pulse or DTMF dialing.
3. The modem is generating an answer tone or detecting answer tone.
4. After ring indicate goes on, DSR waits at least two seconds before turning on to allow the telephone company equipment to be engaged.

DSR will go off 50 msec after DTR goes off or 50 msec plus a maximum of 4 sec when SSD is enabled. (Note: All time measurements without a tolerance have a ±0.5 ms tolerance.)

DATA TERMINAL READY

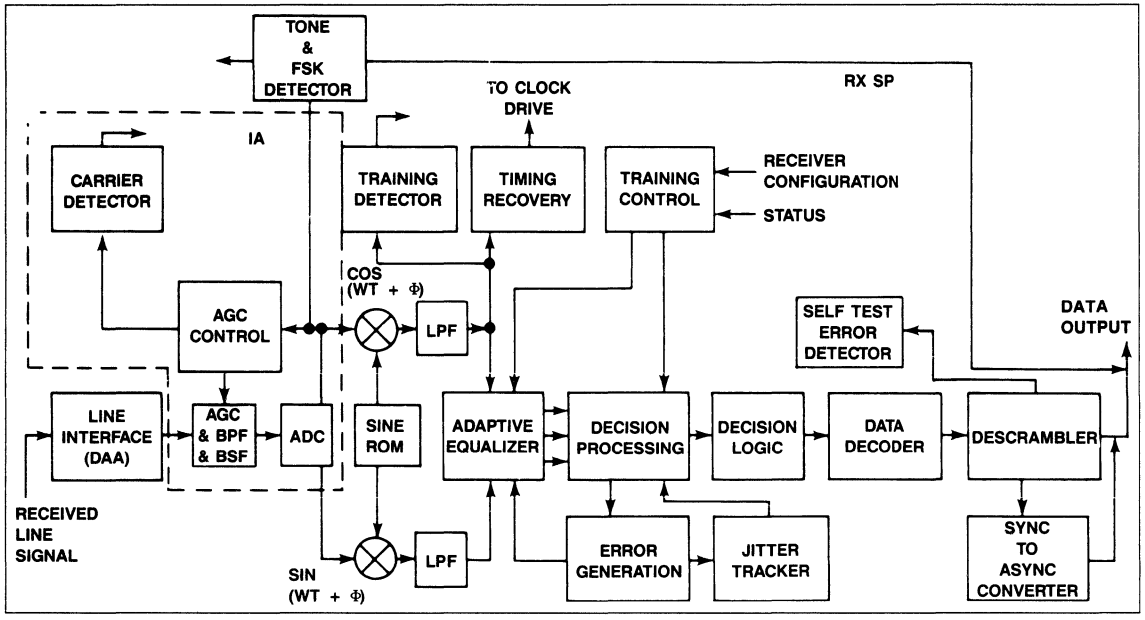
An on condition of DTR prepares the modem to be connected to the communications channel, and maintains the connection established by the DTE (manual answering) or internal (automatic answering) means. The off condition places the modem in the disconnect state.

AUTOMATIC RECONFIGURATION

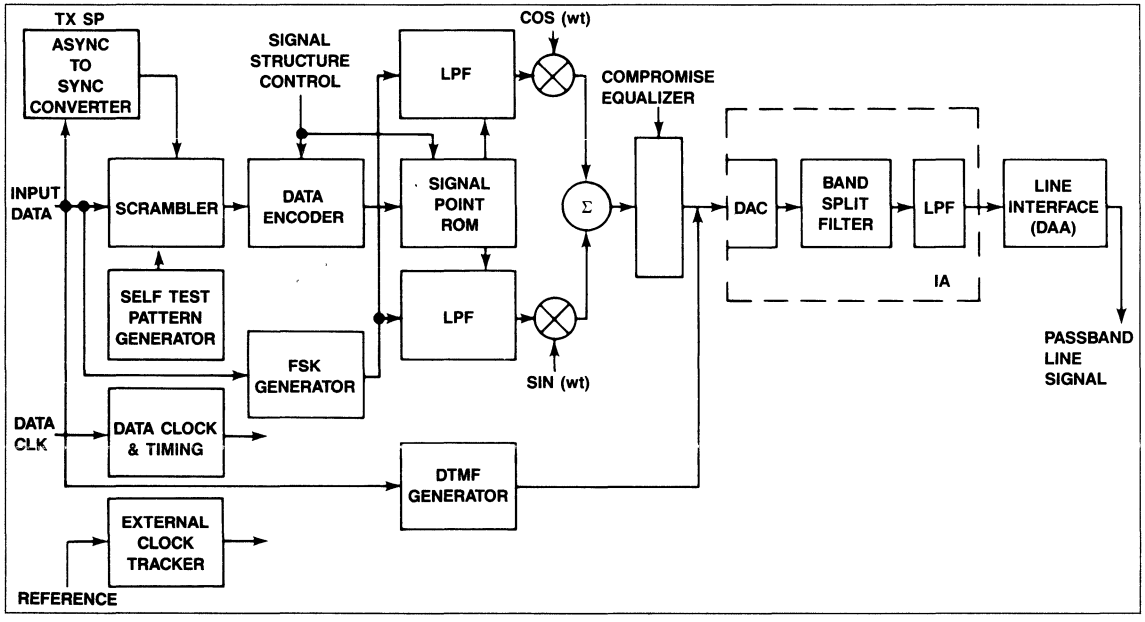
The R1212/U is capable of automatically configuring itself to the compatibility of a remote modem. The R1212/U can be in either the answer or originate mode for this to occur. The compatibilities that the R1212/U is limited to adapt to are V.22A/B, Bell 212, and Bell 103. If the R1212/U is to originate in a specific configuration, the MODE bits must be set.

RECEIVE/TRANSMIT CIRCUITS

The receiver and transmitter circuits are defined in the following block diagrams:



R1212/U Receiver/Equalizer Block Diagram



R1212U Transmitter Block Diagram

MODES OF OPERATION

The R1212/U is capable of being operated in either a serial or a parallel mode of operation.

SERIAL MODE

The serial mode uses standard V.24 (RS-232-C compatible) signals to transfer channel data. An optional USART device (shown in the Functional Interconnect Diagram) illustrates this capability.

PARALLEL MODE

The R1212/U has the capability of transferring channel data up to 8 bits at a time via the microprocessor bus. Both asynchronous and synchronous operation is available over the parallel bus.

MODE SELECTION

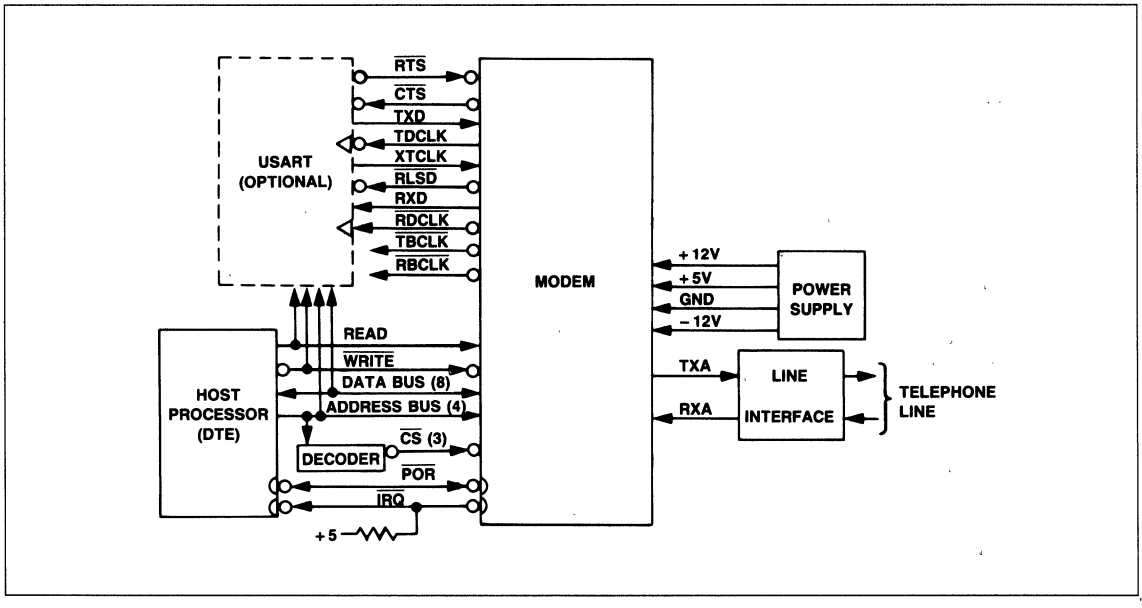
Selection of either the serial or parallel mode is by means of the BUS bits ([0,1]:D:7). To enable the parallel mode, the bus bits must be set to a one. Serial mode can use only serial control inputs ($\overline{DTR}$, $\overline{RTS}$, $\overline{TLK}$, $\overline{ORG}$). Parallel mode requires the use of the register control bits (DTR, RTS, DATA, ORG). Both the register and serial outputs are available concurrently, so either can be used in both modes. The modem automatically defaults to the serial mode at power-on. In either mode the R1212/U is configured by the host processor via the microprocessor bus.

INTERFACE CRITERIA

The modem interface comprises both hardware and software circuits. Hardware circuits are assigned to specific pins in a 64-pin DIN connector. Software circuits are assigned to specific bits in a 32-byte interface memory.

HARDWARE CIRCUITS

Signal names and descriptions of the hardware circuits, including the microprocessor interface, are listed in the R1212/U Hardware Circuits table. In the table, the column titled 'Type' refers to designations found in the Hardware Circuit Characteristics. The microprocessor interface is designed to be directly compatible with an 8080 microprocessor. With the addition of a few external logic gates, it can be made compatible with 6500, 6800, or 68000 microprocessors.

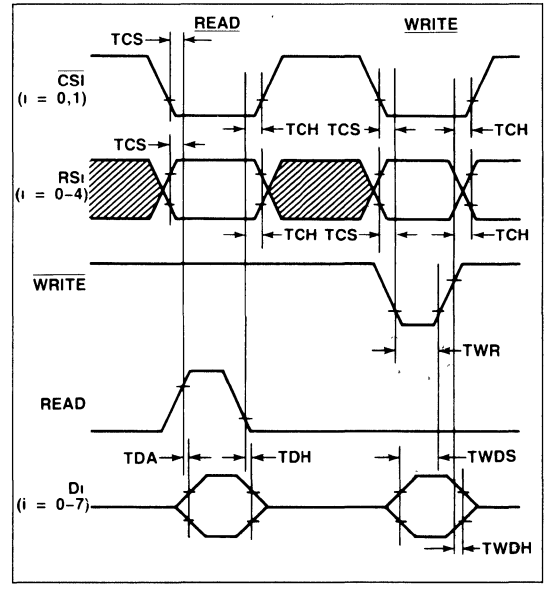


R1212/U Functional Interconnect Diagram

R1212/U Hardware Circuits

Name	Type	Pin No.	Description
A. OVERHEAD:			
Ground (A)	AGND	31C,32C	Analog Ground Return
Ground (D)	DGND	3C,8C,5A,10A	Digital Ground Return
+5 volts	PWR	19C,23C,26C,30C	+5 volt supply
+12 volts	PWR	15A	+12 volt supply
−12 volts	PWR	12A	−12 volt supply
$\overline{POR}$	I/OB	13C	Power-On-Reset
B. MICROPROCESSOR INTERFACE:			
D7	I/OA	1C	
D6	I/OA	1A	
D5	I/OA	2C	
D4	I/OA	2A	Data Bus (8 Bits)
D3	I/OA	3A	
D2	I/OA	4C	
D1	I/OA	4A	
D0	I/OA	5C	
RS3	IA	6C	
RS2	IA	6A	Register Select
RS1	IA	7C	(4 Bits)
RS0	IA	7A	
$\overline{CS0}$	IA	10C	Chip Select Receiver Baud Rate Device
$\overline{CS1}$	IA	9C	Chip Select Transmitter Sample Rate Device
$\overline{READ}$	IA	12C	Read Enable
$\overline{WRITE}$	IA	11A	Write Enable
$\overline{IRQ}$	OB	11C	Interrupt Request
C. V.24 INTERFACE:			
XTCLK	IB	22A	External Transmit Clock
TDCLK	OC	23A	Transmit Data Clock
$\overline{RDCLK}$	OC	21A	Receive Data Clock
$\overline{RTS}$	IB	25A	Request-to-Send
$\overline{CTS}$	OC	25C	Clear-to-Send
TXD	IB	24C	Transmit Data
RXD	OC	22C	Receive Data
$\overline{RLSD}$	OC	24A	Received Line Signal Detector
$\overline{DTR}$	IB	21C	Data Terminal Ready
$\overline{DSR}$	OC	20A	Data Set Ready
$\overline{RI}$	OC	18A	Ring Indicator
D. ANALOG SIGNALS (R1212M/U ONLY):			
RXA	IB	32A	Receive Analog Input
TXA	OC	31A	Transmit Analog Output
E. SIGNALS TO DAA (R1212M/U ONLY):			
$\overline{RD}$	IB	27A	Ring Detect
RCCT	OC	28A	Request Coupler Cut Through
$\overline{CCT}$	IB	29C	Coupler Cut Through
OH	OC	29A	Off-Hook Relay Control
F. ANCILLARY CIRCUITS:			
$\overline{TBCLK}$	OC	27C	Transmit Baud Clock
$\overline{RBCLK}$	OC	26A	Receive Baud Clock
$\overline{TLK}$	IC	28C	Talk (TLK = Data)
$\overline{ORG}$	IB	16C	Originate (ORG = Answer)

MICROPROCESSOR TIMING



Microprocessor Interface Timing Diagram

Critical Timing Requirements

Characteristic	Symbol	Min	Max	Units
$\overline{CSi}$, RSi setup time prior to Read or $\overline{Write}$	TCS	30	—	NS
Data Access time after Read	TDA	—	140	NS
Data hold time after Read	TDH	10	50	NS
CSi, RSi hold time after Read or $\overline{Write}$	TCH	10	—	NS
Write data setup time	TWDS	75	—	NS
Write data hold time	TWDH	10	—	NS
Write strobe pulse width	TWR	75	—	NS

7

HARDWARE CIRCUIT CHARACTERISTICS

Digital Interface Characteristics

Digital Interface Characteristics

Symbol	Parameter	Units	Input/Output Type IA	IB	IC	OA	OB	OC	I/O A	I/O B
V_{IH}	Input Voltage, High	V	2.0 Min.	2.0 Min.	2.0 Min.				2.0 Min.	5.25 Max. 2.0 Min.
V_{IL}	Input Voltage, Low	V	0.8 Max.	0.8 Max.	0.8 Max.				0.8 Max.	0.8 Max.
V_{OH}	Output Voltage, High	V				2.4 Min.[1]			2.4 Min.[1]	2.4 Min.[3]
V_{OL}	Output Voltage, Low	V				0.4 Max.[2]	0.4 Max.[2]	0.4 Max.[2]	0.4 Max.[2]	0.4 Max.[2]
I_{IN}	Input Current, Leakage	μA	±2.5 Max.						±2.5 Max.[4]	
I_{OH}	Output Current, High	mA				−0.1 Max.				
I_{OL}	Output Current, Low	mA				1.6 Max.	1.6 Max.	1.6 Max.		
I_L	Output Current, Leakage	μA					±10 Max.			
I_{PU}	Pull-up Current (Short Circuit)	μA		−240 Max. −10 Min.	−240 Max. −10 Min.			−240 Max. −10 Min.		−260 Max. −100 Min.
C_L	Capacitive Load	pF	5	5	20				10	40
C_D	Capacitive Drive	pF				100	100	100	100	100
	Current Type		TTL	TTL w/Pull-up	TTL w/Pull-up	TTL	Open-Drain	Open-Drain w/Pull-up	3-State Transceiver	Open-Drain w/Pull-up

Notes
1. I Load = −100 μA
2. I Load = 1.6 mA
3. I Load = −40 μA
4. V_{IN} = 0.4 to 2.4 Vdc, V_{CC} = 5.25 Vdc

Analog Interface Characteristics

TXA — The (Type OC) transmitter output is a low impedance operational amplifier output in series with a 604 ohm resistor. In order to have a 0 dBm output, an external 600 ohm to ground is required.

RXA — The (Type IB) receiver input impedance is 63.4K ohms ±5 percent.

Transmission Line Interface Characteristics

The R1212DC/U interface to the telephone line is the Tip and Ring leads. Lightning induced surge voltages and other hazardous voltages which may appear on the telephone line are limited to approximately 7V peak between the secondary leads of the line coupling transformer.

The DAA (R1212DC/U *only*) is bi-directional as required by 2-wire full-duplex circuits.

Connection to the telephone line interface pins of the R1212DC/U to the network are made via two RJ11 jacks. The pin designations are shown in the table below:

R1212DC/U Network Interface

Connection Type	Telco	Mnemonic	Function
	1		
VSOC	2		
RJ11	3	R	Ring-one side of telephone line
Jack	4	T	Tip-one side of telephone line
	5		
	6		

Ring Indicator — The R1212/U provides a ring indicator ($\overline{RI}$) output; its low state indicates the presence of a ring signal on the line. The low condition appears approximately coincident with the on segment of the ring cycle (during rings) on the communication channel. (The ring signal cycle is typically two seconds on, four seconds off.) The high condition of the indicator output is maintained during the off segment of the ring cycle (between rings) and at all other times when ringing is being received. The operation of $\overline{RI}$ is not disabled by an off condition on Data Terminal Ready.

$\overline{RI}$ will respond to ring signals in the frequency range of 15.3 Hz to 68 Hz with voltage amplitude levels of 40 to 150 Vrms (applied across Tip and Ring), with the response times given in the following table:

RI Response Time

RI Transition	Response Time
Off-to-On	170 ±50 ms
On-to-Off	110 ±50 ms

This off-to-on (on-to-off) response time is defined as the time interval between the sudden connection (removal) of the ring signal across Tip and Ring and the subsequent on (off) transition $\overline{RI}$.

OH — The R1212M/U provides an output OH (Off-Hook) which indicates the state of the OH relay. A low condition on OH implies the OH relay is closed and the modem is connected to the telephone line. A high condition on OH implies the OH relay is open (i.e., the modem is on-hook). The delay between the low-to-high or high-to-low transition of OH and the subsequent close-to-open or open-to-close transition of the OH relay is 8 ms maximum.

$\overline{RD}$ — $\overline{RD}$ indicates to the R1212M/U by an on (low) condition that a ringing signal is present. The $\overline{RD}$ signal should not respond to momentary bursts of ringing less than 125 ms in duration, or to less than 40V rms, 15 to 68 Hz appearing across Tip and Ring with respect to ground.

RCCT — RCCT is used to request that a data transmission path through the DAA be connected to the telephone line. When RCCT goes off (low), the cut-through buffers are disabled and $\overline{CCT}$ should go off (high) within 1 msec. RCCT should be off during dialing but on for tone address signaling.

$\overline{CCT}$ — An on (low) signal to the $\overline{CCT}$ lead indicates to the R1212M/U that the data transmission path through the DAA is connected.

AUDIO INTERFACE INPUT IMPEDANCE CHARACTERISTICS

Audio Interface Input Impedance Characteristics

On/Off Hook	Measurement
On-Hook (DC)	The DC resistance between Tip and Ring, and between either Tip or Ring and signal ground is greater than 10 megohms for DC voltages up to 100 volts.
On-Hook (AC)	The on-hook AC impedance measured between Tip and Ring is less than 40K ohms (15.3 Hz minimum).
Off-Hook (DC)	Less than 200 ohms.
Off-Hook (AC)	600 ohms nominal when measured between Tip and Ring.

SOFTWARE CIRCUITS

The R1212/U comprises two signal processor chips. Each of these chips contains 16 registers to which an external (host) microprocessor has access. Although these registers are within the modem, they may be addressed as part of the host processor's memory space. The host may read data out of or write data into these registers. The registers are referred to as interface memory. Registers in chip 0 update at the modem baud rate (bps) (except RAM Access and RAM Data Update where operation is at sample rate). Registers in chip 1 update at the sample rate (7200 bps).

When information in these registers is being discussed, the format Y:Z:Q is used. The chip is specified by Y(0 or 1), the register by Z(0 – F), and the bit by Q(0 – 7, 0 = LSB).

Status Control Bits

The operation of the R1212/U is affected by a number of software control inputs. These inputs are written into registers within the interface memory via the host microprocessor bus. Bits designated by an 'X' are "Don't Care" inputs that can be set to either 1 or 0. Modem operation is monitored by various software flags that are read from interface memory via the host microprocessor bus. All status and control bits are defined in the Interface Memory table. Bits designated by an 'R' are reserved for modem use only and must not be changed by the host.

RAM Data Access

The R1212/U provides the user with access to much of the data stored in the modem's memories. This data is useful for performing certain diagnostic functions.

Two RAM access registers are provided in the interface memory to allow user access to various RAM locations within chip 0 and chip 1. The access code stored in 0:F selects the source of data for the RAM data registers in chip 0 (0:5 through 0:2). Similarly, the access code stored in 1:F selects the source of data for registers 1:5 through 1:2. Reading is performed by first storing the desired access code in register 0:F (or 1:F). The data may then be read from 0:5 through 0:2 (or 1:5 through 1:2).

RAM Access Codes

The RAM access codes defined in the following table allow the host processor to read diagnostic information within the modem.

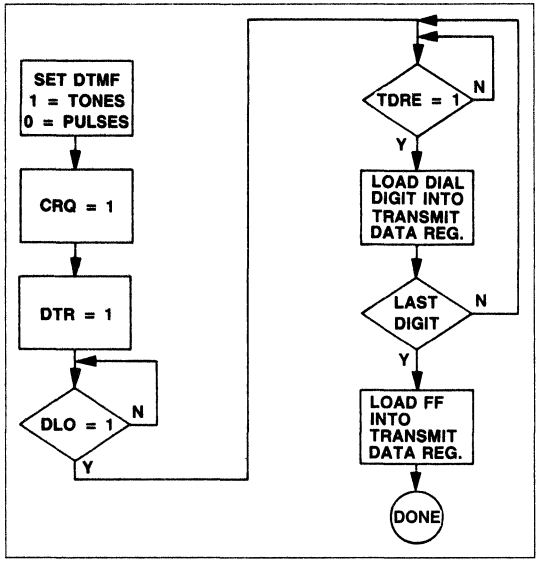
RAM Access Codes (Chip 0)

Function	Access Code	Register No.
Self Test Error Counter	00	2,3
Equalizer Tap Coefficients	01–0D	2,3,4,5
Phase Error	10	2,3
Rotated Equalizer Output (Received Point Eye Pattern)	11	2,3,4,5
Rotated Angle	12	4,5
Low Pass Filter Output	40	2,3,4,5
Input Signal to Equalizer Tap Coefficients	41–4D	2,3,4,5
Decision Points (Ideal Eye Pattern)	51	2,3,4,5
Rotated Error	52	2,3,4,5
Equalizer Output	53	2,3,4,5
Demodulator Output	56	2,3,4,5

7

Auto Dial Sequence

The following flow chart defines the auto dial sequence via the microprocessor interface memory.



Auto Dial Sequence Flow Diagram

Note: The modem timing for the auto dialer accounts for inter-digit delay for pulses and tones.

The timing for the pulses and tones are as follows:

Pulses — Relay open 64 ms
Relay closed 36 ms
Interdigit delay 750 ms

Tones — Tone duration 71 ms
Interdigit delay 71 ms
Output level 1.5 ±1 dBm

R1212/U Receiver Interface Memory Chip 0 ($\overline{CS0}$)

Register \ Bit	7	6	5	4	3	2	1	0
F	RAM Access B							
E	IRQ	ENSI	NEWS	R	NEWC	ERFI	R	RDRF
D	BUS	CRQ	X	X	X	LCD	RSD	X
C	X	X	X	CHAR		PEN	PO	SBN
B	X	X	X	X	X	X	X	AL
A	ERDL	RDL	DL	ST	MODE			
9	X	X	SPEED		PE	FE	OVRN	X
8	TONE	X	X	X	X	X	TM	RLSD
7	R	R	R	R	R	R	R	R
6	R	R	R	R	R	R	R	R
5	RAM Data YBM							
4	RAM Data YBL							
3	RAM Data XBM							
2	RAM Data XBL							
1	R	R	R	R	R	R	R	R
0	Receiver Data Register							
Register / Bit	7	6	5	4	3	2	1	0

Note
(X) indicates user available.
(R) indicates reserved for modem use only.

R1212/U Transmitter Interface Memory Chip 1 ($\overline{CS1}$)

Register \ Bit	7	6	5	4	3	2	1	0
F	RAM Access S							
E	IRQ	ENSI	NEWS	R	NEWC	ETEI	R	TDRE
D	BUS	CRQ	DATA	AAE	DTR	X	X	SSD
C	DSRA	TXCLK		CHAR		PEN	PO	SBN
B	TX LEVEL			GTE	GTS	3DB	DTMF	AL
A	ERDL	RDL	DL	ST	MODE			
9	BRK	X	ORG	LL	RTS	CC	X	X
8	DLO	CTS	DSR	RI	X	X	X	X
7	R	R	R	R	R	R	R	R
6	R	R	R	R	R	R	R	R
5	RAM Data YSM							
4	RAM Data YSL							
3	RAM Data XSM							
2	RAM Data XSL							
1	R	R	R	R	R	R	R	R
0	Transmitter Data Register							
Register / Bit	7	6	5	4	3	2	1	0

Note
(X) indicates user available.
(R) indicates reserved for modem use only.

R1212/U Interface Memory Definitions

Mnemonic	Name	Memory Location	Description
AAE	Auto Answer Enable	1:D:4	When control bit AAE goes to a one, the modem will automatically answer when a singing signal is present on the line.
AL	Analog Loopback	(0,1):B:0	When control bit AL is a one, the modem is placed in (V.54 Loop 3) local analog loopback. In this loop, the transmitter's analog output is coupled to the receiver's analog input at a point near the modem's telephone line interface. An attenuator is introduced into the loop such that the signal level coupled into the receive path is attenuated 14 ±1 dBm.
BRK	Break	1:9:7	When control bit BRK goes to a one, the modem transmits 2M+3 bits of start polarity. (M is equal to the number of bits per character in the selected format.) BRK will reset to zero after the sequence is sent
BUS	Bus Select	(0,1):D:7	When control bit BUS goes to a one, the modem is placed in the parallel mode, and when zero the modem is configured for the serial mode. BUS can be in either state to configure the modem.
CC	Controlled Carrier	1:9:2	When control bit CC goes to a one, the modem is placed in controlled carrier operation; and when zero, the modem is configured for constant carrier operation.
CHAR	Character Length Select	(0,1):C:(3,4)	These character length bits select either 8, 9, 10, or 11 bit characters, as shown below: **Configuration** — **Configuration Word** 8 bits — 0 0 9 bits — 0 1 10 bits — 1 0 11 bits — 1 1
CRQ	Call Request	(0,1):D:6	When control bit CRQ goes to a one, it places the transmitter in auto dial and the receiver in tone detect mode. The data placed in the dial digit is then treated as digits to be dialed. After the last digit has been dialed, FF (HEX) should be loaded into the dial digit register to tell the modem to go to the data state. CRQ in the transmitter (chip 1) when turned off causes the modem to go on-hook. Therefore, it should be on for the duration of the call and not turned off until it is desired to go on-hook. CRQ in the receiver (chip 0) must be turned off immediately after ringback is detected to put the modem in the data mode, otherwise no answerback tone will be detected.
CTS	Clear-to-Send	1:8:6	When status bit CTS is a one, it indicates to the terminal equipment that the modem will transmit any data which are present at TXD. CTS response times from an on or off condition of RTS are shown below: **CTS Transitions** — **Constant Carrier** — **Controlled Carrier** Off to On — <2 ms — 275 ms On to Off — <2 ms — <2 ms
DATA	Talk/Data	1:D:5	When control bit DATA goes to a one, it places the modem in data state and when zero in the talk state.
DL	Digital Loopback (Manual)	(0,1):A:5	When control bit DL is a one, the modem is manually placed in remote digital loopback. DL should be set during the data mode. DSA and CTS will be at zero. The local modem can then be tested from the far-end by using the terminal equipment at the far-end to transmit a test pattern and examine the looped data. At the far-end modem, all interface circuits behave normally as in the data mode. At the conclusion of the test, DL must be reset to zero. The local modem will then return to the normal data mode with control reverting the DTE's, DTR.
DLO	Data Line Occupied	1:8:7	When status bit DLO is a one, it indicates that the modem is in the auto dial state, i.e., CRQ is at a one and the modem is off-hook and ready to dial.

7

R1212/U Interface Memory Definitions (Continued)

Mnemonic	Name	Memory Location	Description
DSR	Data Set Ready	1:8:5	When status bit DSR is a one, it indicates that the answerback tone has been detected, the modem handshake has begun and that the data state will follow. DSR alone should not be used to indicate that the communication channel has been completely established. DSR in conjunction with CTS and RLSD will determine this. DSR will be at zero in all test states (except optionally for analog loopback) and when the channel is being used for voice communication (talk).
DSRA	Data Set Ready In Analog Loopback	1:C:7	When control bit DSRA goes to a one, it causes DSR to be set to a one during analog loopback
DTMF	Touch Tones/ Pulse Dialing	1:B:1	When control bit DTMF goes to a one, it tells the modem to auto dial using tones, and when zero the modem will dial using pulses.
DTR	Data Terminal Ready	1:D:3	Control bit DTR must be a one, before the modem will enter the data state, either manually or automatically. DTR must also be at a one in order for the modem to automatically answer an incoming call.
ENSI	Enable New Status Interrupt	(0,1):E:6	When control bit ENSI goes to a one, it causes an interrupt to occur when the status bits in registers (0:[8,9]) and (1:8) are updated. (NEWS = 1)
ERDL	Enable Response to Remote Digital Loopback	(0,1):A:7	When control bit ERDL goes to a one, it enables the modem to respond to another modem's remote digital loopback request, thus going into loopback.
ERFI	Enable Receiver Full Interrupt	0:E:2	When on, ERFI causes an interrupt to occur when the receiver data register (0.0) is full (RDRF = 1).
ETEI	Enble Transmitter Empty Interrupt	1:E:2	When on, ETEI causes an interrupt to occur when the transmitter data register (1:0) is empty (TDRE = 1).
FE	Framing Error	0:9:2	When on, FE indicates that a framing error has occurred during parallel asynchronous communication.
GTE	Guard Tone Enable	1:B:4	When control bit GTE goes to a one, it causes the specified guard tone to be transmitted (CCITT Configurations only).
GTS	Guard Tone Select	1:B:3	When control bit GTS goes to zero, it selects the 1800 Hz tone and when a one it selects the 550 Hz tone.
IRQ	Interrupt Request	(0,1):E:7	When status bit IRQ is a one, it indicates that an interrupt has been generated.
LCD	Loss of Carrier Disconnect	0:D:2	When control bit LCD goes to a one, the modem terminates a call when a loss of received carrier energy is detected after 400 msec. After the first 40 ms of loss of carrier, RLSD goes off. 360 ms later if no carrier is detected, CTS goes off. LCD is not disabled in leased line operation.
LL	Leased Line	1:9:4	When control bit LL goes to a one, it places the modem in leased line operation; a when zero switched line operation.
MODE	Mode Select	(0,1):A:(0 – 3)	These bits select the compatibility at which the modem is to operate, as shown below: **Configuration** — **Configuration Word** Bell 212A 1200 Sync. — 0 0 1 0 Bell 212A 1200 Async — 0 0 1 1 Bell 212A 300 Async. — 0 1 0 0 V.22A 1200 Sync. — 1 0 0 0 V.22B 1200 Async. — 1 0 0 1 V.22A 600 Sync. — 1 0 1 0 V.22B 600 Async. — 1 0 1 1

R1212/U Interface Memory Definitions (Continued)

Mnemonic	Name	Memory Location	Description
NEWC	New Configuration	(0,1):E:3	When status bit NEWC is a one, it tells the modem that a new configuration has been written into the configuration registers. The modem will then read the configuration registers and then reset NEWC. NEWC must be set after a new configuration has been written into the following registers .(0:[A – D]) and (1:[9 – D]) The remaining registers do not require the use of NEWC to tell the modem that new data was written into them.
NEWS	New Status	(0,1):E:5	When status bit NEWS is a one, it tells the user that there has been a change of status in the status registers. The user must write a zero into NEWS to reset it. This action also causes the interrupt to be cleared
ORG	Originate/Answer	1:9:5	When status bit ORG is a one, it tells the modem that it is originating a call and when a zero answering a call. (This is only valid in manual originate/answer and analog loopback.)
OVRN	Overrun	0:9.1	When on, OVRN signifies that the receiver data register (0.0) was written over due to the user not reading it in the required interval.
PE	Parity Error	0.9 3	When on, PE indicates that a parity error occurred during parallel asynchronous communication.
PEN	Parity Enable	(0,1):C:2	When on, PEN allows the generation of parity bits and tells the receiver that the data includes parity.
PO	Parity Odd	(0,1)·C:1	When on, PO conditions the modem, when PEN = 1, to generate and expect odd parity PO = 0 generates even parity
(None)	RAM Access B	0.F.0 – 7	Contains the RAM access code used in reading RAM locations in chip 0 (baud rate device).
(None)	RAM Access S	1·F·0 – 7	Contains the RAM access code used in reading RAM locations in chip 1 (sample rate device).
(None)	RAM Data XBL	0:2:0 – 7	Least significant byte of 16-bit word X used in reading RAM locations in chip 0.
(None)	RAM Data XBM	0:3:0 – 7	Most significant byte of 16-bit word X used in reading RAM locations in chip 0.
(None)	RAM Data XSL	1:2:0 – 7	Least significant byte of 16-bit word X used in reading RAM locations in chip 1.
(None)	RAM Data XSM	1:3:0 – 7	Most significant byte of 16-bit word X used in reading RAM locations in chip 1.
(None)	RAM Data YBL	0:4:0 – 7	Least significant byte of 16-bit word Y used in reading RAM locations in chip 0.
(None)	RAM Data YBM	0:5:0 – 7	Most significant byte of 16-bit word Y used in reading RAM locations in chip 0.
(None)	RAM Data YSL	1:4.0 – 7	Least significant byte of 16-bit word Y used in reading RAM locations in chip 1.
(None)	RAM Data YSM	1:5:0 – 7	Most significant byte of 16-bit word Y used in reading RAM locations in chip 1.
RDL	Remote Digital Loopback	(0,1):A:6	When control bit RDL goes to a one, it causes the modem to initiate a request for the remote modem to go into digital loopback.
RDR	Receiver Data Register	0:0:0 – 7	RDR is used to read received data. RDR is a read only register. Reading this register causes the receives interrupt to be cleared.
RI	Ring Indicator	1·8·4	When status bit RI is a one, it indicates that a ringing signal is being detected.
RLSD	Received Line Signal Detector	0·8 0	When status bit RLSD is a one, it indicates that the carrier has successfully been received. RLSD will not respond to the 550, 1800, 2100, or 2225 Hz tones. RLSD response times are given below: **RLSD Transitions[1]** / **Constant Carrier** / **Controlled Carrier** Off to On: 40 to 65 ms / 40 to 65 ms On to Off: 40 to 65 ms / 40 to 65 ms Note: 1. After handshake has occurred.

R1212 Interface Memory Definitions (Continued)

Mnemonic	Name	Memory Location	Description
RSD	Receive Space Disconnect	0:D:1	When control bit RSD goes to a one, it causes the modem to go on-hook after receiving approximately 1.6 seconds of continuous spaces.
RTS	Request-to-Send	1:9:3	When control bit RTS goes to a one, it allows the modem to transmit data when CTS becomes active. Responses to RTS are shown below: Assume DTR is on, Talk/Data is set to Data (CRQ or AAE is set for a dial line) and the modem is connected to the line (off-hook). **Leased or Dial Line[1] — RTS Off — RTS On** Controlled Carrier — CTS Off, Carrier Off — Carrier On, 275 ms Scrambled 1's transmitted, CTS On Constant Carrier — CTS Off, Carrier On, Scrambled 1's Transmitted — CTS On, Carrier On, Data Transmitted Note: 1. After handshake is complete. For ease of use in constant carrier mode, RTS should be turned on the same time as DTR.
SBN	Stop Bit Number	(0,1):C:0	When on, SBN tells the modem to generate and expect 2 stop bits per character When off, SBN signifies 1 stop bit per character.
SPEED	Speed Indication	0:9:(4,5)	00 = 300 bps 10 = 1200 bps 01 = 600 bps
SSD	Send Space Disconnect	1:D:0	When control bit SSD goes to a one, it causes the modem to transmit approximately 4 seconds of spaces before disconnecting, when DTR is at zero.
ST	Self Test	(0,1):A:4	When control bit ST is a one, self test is activated. ST must be at zero to end the test. It is possible to perform test with or without DTE connected. During any self test, TXD and RTS are ignored. Self test do not test asynchronous-to-synchronous converter circuits in either the transmitter or receiver. Error detection is accomplished by monitoring the self test error counter in the RAM If the counter increments during the self test, an error was made. The counter contents are available in the diagnostic registers when the RAM access code 00 is loaded in the diagnostic control register (0:F). *Self Test End-to-End* Upon activation of self-test an internally generated data pattern of alternate binary ones and zeros (reversals) at the selected bit rate are applied to the scrambler. An error detector, capable of identifying errors in a stream of reversals are connected to the output of the descrambler. *Self Test with Loop 3* Loop 3 is applied to the modem as defined in recommendation V.54. Self-test is activated and DCE operation is as in the end-to-end test. In this test DTR is ignored. *Self Test with Loop 2* The modem is conditioned to instigate a loop 2 at the remote modem as specified in recommendation V.54. Self-test is activated and DCE operation is as in the end-to-end test.
TDR	Transmitter Data Register	1:0:0–7	TDR is used to load data to be transmitted and digits to be dialed. Example: If a 4 is to be dialed a 04 (HEX) should be loaded. TDR is a write only register. Writing to this register causes the transmitter interrupt to be cleared

R1212 Interface Memory Definitions (Continued)

Mnemonic	Name	Memory Location	Description
TDRE	Transmitter Data Register Empty	1:E:0	When on, TDRE indicates that the transmitter data register is empty and can be loaded with new data whether it is dial digits or data to be transmitted In synchronous operation the user must load the transmitter data register within 8 bit times after TDRE turns on to maintain synchronization. After the register is loaded, TDRE goes off.
3 DB	3 dB Loss to Receive Signal	1:B:2	When control of bit 3 DB is a one, it attenuates the received signal 3 dB. This is only used if the R1212M/U will see 0 dBm or greater line signal at the receiver input. Insertion of the 3 dB loss will then prevent saturation. This bit is not needed with the R1212DC/U.
TM	Test Mode	0·8 1	When status bit TM is a one, it indicates that the modem has completed the handshake and is in one of the following test modes: AL, RDL, or DL.
TONE	Tone Detect	0·8:7	TONE follows the energy detected in the 340 to 645 Hz frequency band. The user must determine which tone is present on the line by determining the duty cycle of the TONE bit. TONE is active only when CRQ in chip 0 is a one.
TXCLK	Transmit Clock Select	1:C:(5,6)	TXCLK allows the user to designate the origin of the transmitter data clock, as shown below: **Transmit Clock** — **Configuration Word** Internal — 0 0 Not Used — 0 1 External — 1 0 Slave — 1 1
TX LEVEL	Transmit Level	1:B:(5–7)	TX LEVEL allows the user to change the R2424M transmitter output level, assuming the modem is transmitting into a 600 ohm load. **Transmit Level (±1.0 dBm)** — **Configuration Word** 0 dBm — 0 0 0 –2 dBm — 0 0 1 –4 dBm — 0 1 0 –6 dBm — 0 1 1 –8 dBm — 1 0 0 –10 dBm — 1 0 1 –12 dBm — 1 1 0 –14 dBm — 1 1 1

POWER-ON INITIALIZATION

When power is applied to the R1212/U, a period of 50 to 300 ms is required for power supply settling. The power-on-reset signal (POR) remains low during this period. Approximately 10 ms after the low to high transition of POR, the modem is ready to be configured, and RTS may be activated. If the 5 Vdc power supply drops below 3.5 Vdc for more than 30 msec, the POR cycle is repeated.

At POR time the modem automatically defaults to Bell 212A 1200 bps, answer state using serial start-stop data 10 bits per character, constant carrier, dial line.

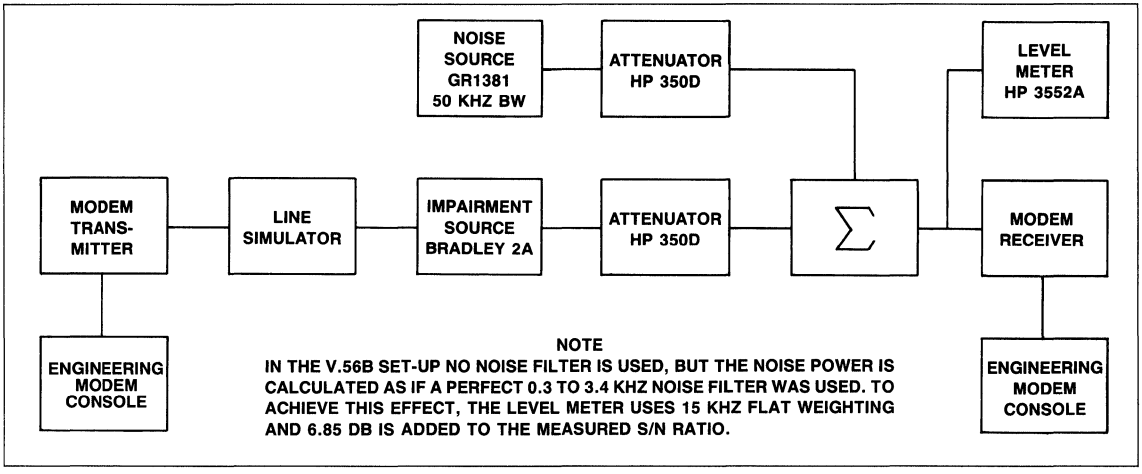
POR can be connected to a user supplied power-on-reset signal in a wire or configuration. A low active pulse of 3 μsec or more applied to the POR pin causes the modem to reset. The modem is ready to be configured 10 msec after the low active pulse is removed from POR.

PERFORMANCE

Whether functioning as a V.22, or Bell 212A type modem, and regardless of simulated line condition or introduced line impairment, the R1212/U provides unexcelled high performance to the user.

BIT ERROR RATES

The Bit Error Rate (BER) performance of the R1212/U is specified for a test configuration conforming to that specified in CCITT Recommendation V.56, except with regard to the placement of the filter used to bandlimit the white noise source. Bit error rates are measured at a received line signal level of −43 dBm.



BER Performance Test Set-up

GENERAL SPECIFICATIONS

Power

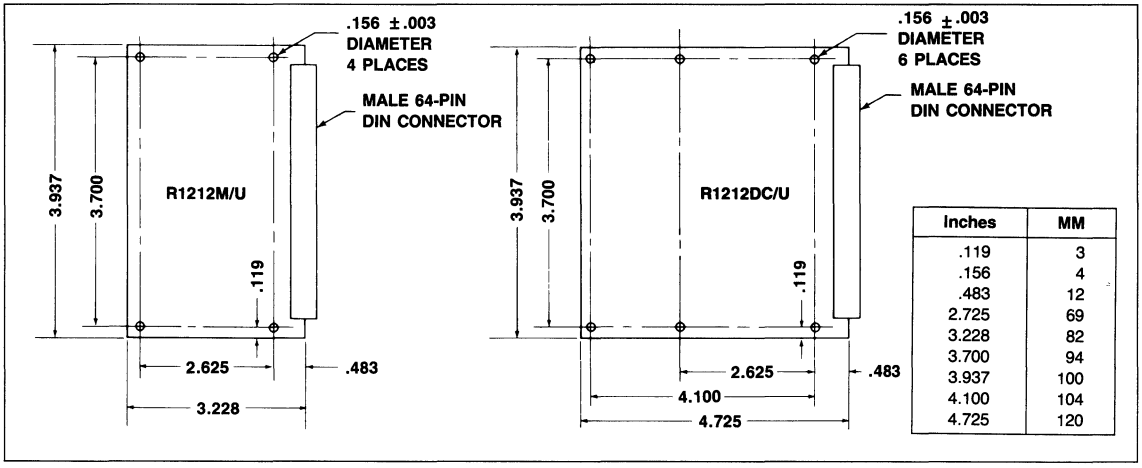
Voltage	Tolerance	Current (Max)
+5 Vdc	±5%	<500 mA
+12 Vdc	±5%	<10 mA
−12 Vdc	±5%	<50 mA
Note: All voltages must have ripple ≤0.1 volts peak-to-peak.		

Environmental

Parameter	Specification
Temperature Operating— Storage—	 0°C to +60°C (32 to 140°F) −40°C to +80°C (−40 to 176°F)
Relative Humidity	Up to 90% noncondensing, or a wet bulb temperature up to 35°C, whichever is less.
Altitude	−200 to +10,000 feet
*PCB's are stored in heat sealed antistatic bags and shipping containers.	

Mechanical

Board Structure	Single PC board with right angle male DIN connector.
Mating Connector	Female 3 row 64 pin Euroconnector (DIN) with rows A and C populated. Recommended mating connector: Winchester 96S-6043-0531-1 or equivalent.
PCB Dimensions R1212DC/U Version R1212M/U Version	 Width 3.94 in. (100 mm) x Length 4.725 in. (120 mm) x Height 0.75 in. (19 mm) Width 3.94 in. (100 mm) x Length 3.23 in. (82 mm) x Height 0.40 in. (10 mm)
Weight	Less than 0.45 lbs. (0.20 kg.)
Lead Extrusion	0.100 in. (2.54 mm) max.



Inches	MM
.119	3
.156	4
.483	12
2.725	69
3.228	82
3.700	94
3.937	100
4.100	104
4.725	120

R1212/U Printed Circuit Board Dimensions

INSTALLATION

IMPORTANT NOTICE TO USER

The R1212DC/U contains protective circuitry registered with the Federal Communications Commission (FCC) Part 68 to allow direct connection to the switched telephone network. To comply with the FCC regulations the following is required:

1. All direct connections to the telephone lines shall be made through standard plugs and telephone company provided jacks.
2. It is prohibited to connect the modem to pay telephones or party lines.
3. You are required to notify the local telephone company prior to the connection and upon final disconnection of the modem. You must supply to the telephone company the make, model number, FCC registration number, ringer equivalence and particular line to which the connection is to be made. If the proper jacks are not available, you must order the type of jacks to be used from the telephone company.
4. You should disconnect the modem from the telephone line if it appears to be malfunctioning. Reconnect it only when it can be determined that the telephone line is the source of trouble. If the modem needs repair, return it to Rockwell International. This applies to equipment both in and out of warranty. Do not attempt to repair the unit as this will violate FCC rules.
5. The modem contains protective circuitry to prevent harmful voltages from being transmitted to the telephone network. If however such harmful voltages do occur, then the telephone company shall:
   - Promptly notify you of the discontinuance.
   - Afford you the opportunity to correct the situation which caused the discontinuance.

   The FCC requires that the following label be prominently displayed on an outside surface of the OEM's end product.
   - Unit contains Registered Protective Circuitry which complies with Part 68 of FCC Rules.
   - FCC Registration Number: Applied For
   - Ringer Equivalence: 0.5

   Size of the label should be such that all the required information is legible without magnification.

Rockwell

R2424
2400 BPS FULL-DUPLEX MODEM

INTRODUCTION

The Rockwell R2424 is a high performance full-duplex 2400 bps modem. Using state-of-the-art VLSI and signal processing technology, the R2424 provides the user with enhanced performance and reliability on a single printed circuit board of less than 22 square-inches—overall size.

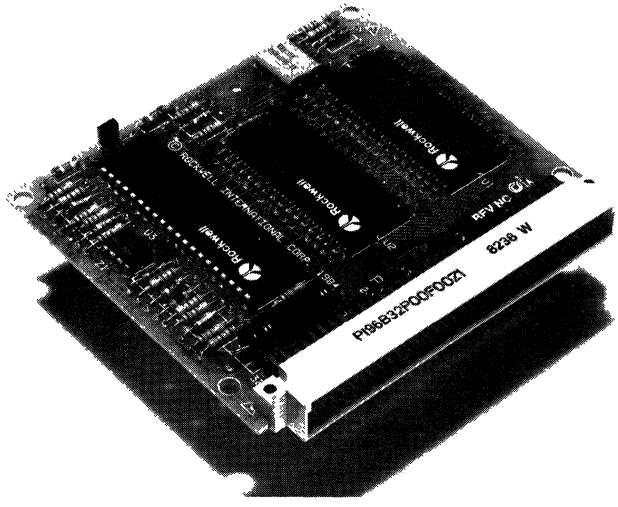
The R2424 modem is ideal for data transmission over the 2-wire dial-up telephone network. The direct-connect, auto dial/answer features are specifically designed for remote and central site computer applications. The bus interface allows easy integration into a personal computer, box modem, microcomputer, terminal or any other communications product that demands the utmost in reliability and performance.

The added test features, such as local analog loopback, remote digital loopback, and a self-test function, offer the user flexibility in creating a 2400 bps modem design customized for specific packaging and functional requirements.

Being CCITT V.22 bis, V.22 A, B compatible, as well as Bell 212A and 103 compatible, this modem fits most applications for full-duplex 2400 and 1200 bps fallback (synchronous and asynchronous) and 0 to 300 bps asynchronous data transmission over the general switched telephone network.

FEATURES

- CCITT V.22 bis, V.22 A, B Compatible
- Bell 212A and 103 Compatible
- Synchronous: 2400 bps, 1200 bps, 600 bps ±0.01%
- Asynchronous: 2400 bps, 1200 bps, 600 bps +1%, −2.5%, 0-300 bps
  —Character length 8, 9, 10, or 11 bits
- DTE Interface
  —Functionally: Microprocessor Bus (Configuration/Control) and RS-232-C Interface (Data/Control)
  —Electrically: TTL Compatible
- Operation: 2-wire full-duplex
- Adaptive and Fixed Compromize Equalization
- Test Configurations:
  —Local Analog Loopback
  —Remote Digital Loopback
  —Self Test
- Auto/Manual Answer
- Auto/Manual Dial:
  —Tone or Pulse Dial
- Power Consumption: 3 Watts Typical
- Power Requirements: +5 Vdc, ±12 Vdc
- Plug-compatible member of new Rockwell modem line
- Two Versions: R2424DC (Direct Connect) with FCC approved DAA Part 68 Interface and R2424M (Module) without DAA



R2424 Full-Duplex Modem

TECHNICAL SPECIFICATIONS

TRANSMITTER CARRIER AND SIGNALING FREQUENCIES

Transmitter Carrier and Signaling Frequencies Specifications

Frequency	Specification (Hz ±0.01%)
V.22 bis low channel, Originate Mode	1200
V.22 low channel, Originate Mode	1200
V.22 high bis channel, Answer Mode	2400
V.22 high channel, Answer Mode	2400
Bell 212A high channel Answer Mode	2400
Bell 212A low channel Originate Mode	1200
Bell 103/113 Originating Mark	1270
Bell 103/113 Originating Space	1070
Bell 103/113 Answer Mark	2225
Bell 103/113 Answer Space	2025

TONE GENERATION

The specifications for tone generation are as follows:

1. **Answer Backtones:** The R2424 generates echo disabling tones both of the CCITT and Bell versions, as follows:
   a. CCITT: 2100 Hz ±15 Hz.
   b. Bell: 2225 Hz ±10 Hz.
2. **Guard Tones:** If GTS is low, an 1800 Hz guard tone frequency is selected; if GTS is high, a 553.846 Hz tone is employed. In accordance with the CCITT V.22 Recommendation, the level of transmitted power for the 1800 Hz guard tone is 6 ±1 dB below the level of the data power in the main channel. The total power transmitted to the line is the same whether or not a guard tone is enabled. If a 553.846 Hz guard is used, its transmitted power is 3 ±1 dB below the level of the main channel power, and again the overall power transmitted to the line will remain constant whether or not a guard tone is enabled. The device accomplishes this by reducing the main channel transmit path gain by .97 dB and 1.76 dB for the cases of the 1800 Hz and 553.846 Hz guard tones respectively.
3. **DTMF Tones:** The R2424 generates dual tone multi-frequency tones. When the transmission of DTMF tones are required, the CRQ and DTMF bits must be set to a 1. (see Interface Memory). When in this mode, the specific DTMF tones generated are decided by loading the dial digit register with the appropriate digit as shown in the following table:

Dial Digits/Tone Pairs

BCD				Dial Digits	Tone Pairs	
0	0	0	0	0	941	1336
0	0	0	1	1	697	1209
0	0	1	0	2	697	1336
0	0	1	1	3	697	1477
0	1	0	0	4	770	1209
0	1	0	1	5	770	1336
0	1	1	0	6	770	1477
0	1	1	1	7	852	1209
1	0	0	0	8	852	1336
1	0	0	1	9	852	1477
1	0	1	0	★	941	1209
1	0	1	1	Spare (B)	697	1633
1	1	0	0	Spare (C)	770	1633
1	1	0	1	Spare (D)	852	1633
1	1	1	0	#	941	1477
1	1	1	1	Spare (F)	941	1633

TONE DETECTION

The R2424 detects tones in the 340 ± 5 Hz to 640 ± 5 Hz band.
Detection Level: 0 to −45dBm
Response Time: 17 ± 2ms

SIGNALING AND DATA RATES

The signaling and data rates for the R2424 are defined in the table below:

Signaling and Data Rates

Operating Mode	Signaling Rate (Baud)	Data Rate
V.22 bis:	600	Synchronous/Asynchronous 2400 bps ±0.01%
V.22 bis:	600	Synchronous/Asynchronous 1200 bps ±0.01%
V.22: (Alternative A) Mode i	600	1200 bps ±0.01% Synchronous
Mode iii	600	600 bps ±0.01% Synchronous
(Alternative B) Mode i Mode iii	600 600	1200 bps ±0.01% Synchronous 600 bps ±0.01% Synchronous
Mode ii		1200 bps Asynchronous 8, 9, 10, or 11 Bits Per Character
Mode iv		600 bps Asynchronous 8, 9, 10, or 11 Bits Per Character
Bell 212A:	600	1200 bps ±0.01% Synchronous/Asynchronous
	0 to 300	0 to 300 bps Asynchronous

DATA ENCODING

The specifications for data encoding are as follows:

1. *2400 bps (V.22 bis).* The transmitted data is divided into groups of four consecutive bits (quad bits) forming a 16-point signal structure.
2. *1200 bps (V.22 and Bell 212A).* The transmitted data is divided into groups of two consecutive bits (dibits) forming a four-point signal structure.
3. *600 bps (V.22).* Each bit is encoded as a phase change relative to the phase preceding signal elements.

EQUALIZERS

The R2424 provides equalization functions that improve performance when operating over low quality lines.

Automatic Adaptive Equalizer—An automatic adaptive equalizer is provided in the receiver circuit for V.22 bis, V.22 and Bell 212A configurations.

Fixed Compromise Equalizer—Compromise equalizers are provided in the transmitter and receiver.

TRANSMITTED DATA SPECTRUM

After making allowance for the nominal specified compromise equalizer characteristic, the transmitted line signal has a frequency spectrum shaped by the square root of a 75 percent raised cosine filter. Similarly, the group delay of the transmitter output is within ±100 microseconds over the frequency range 900 to 1500 Hz (low channel) and 2100 to 2700 Hz (high channel).

SCRAMBLER/DESCRAMBLER

The R2424 incorporates a self-synchronizing scrambler/descrambler. In accordance with the CCITT V.22 bis, V.22 and the Bell 212A recommendations.

RECEIVED SIGNAL FREQUENCY TOLERANCE

The receiver circuit of the R2424 can adapt to received frequency errors of up to ±7 Hz with less than a 0.2 dBm degradation in BER performance.

RECEIVE LEVEL

The receiver circuit of the R2424 satisfies all specified performance requirements for the received line signals from 0 dBm to −45 dBm. The received line signal is measured at the receiver analog input RXA.

RECEIVE TIMING

The R2424 provides a Receive Data Clock (RDCLK) output in the form of a (50 ±1% duty cycle) squarewave. The low to high transitions of this output coincide with the center of received data bits. The timing recovery circuit is capable of tracking a ±.035% (relative) frequency error in the associated transmit timing source.

TRANSMIT LEVEL

The R2424M output control circuitry contains a variable gain buffer which reduces the modem output level. The R2424M can be strapped via the host interface memory to accomplish this.

PERMISSIVE/PROGRAMMABLE CONFIGURATIONS

The R2424M transmit level is +6 dBm to allow a DAA to be used. The DAA then determines the permissive or programmable configuration.

The R2424DC transmit level is strapped in the permissive mode so that the maximum output level is −10 dBm ±1.0 dBm.

TRANSMIT TIMING

The R2424 provides a Transmit Data Clock (TDCLK) output with the following characteristics:

1. *Frequency.* Selected data rate of 2400, 1200 or 600 Hz (±0.01%).
2. *Duty Cycle.* 50 ±1%.

Transmit Data (TXD) must be stable during the one microsecond periods immediately preceding and following the rising edge of TDCLK.

CLAMPING

The following clamp is provided with the R2424:

1. *Receive Data (RXD).* RXD is clamped to a constant mark (1) whenever RLSD is off.

RECEIVED LINE SIGNAL DETECTOR

The high and low channel thresholds are greater than −45 dBm (RLSD on) and less than −48 dBm (RLSD off) for V.22 bis, V.22 and Bell 212A configurations.

DATA SET READY

The on condition of the R2424 output Data Set Ready (DSR) indicates that the modem is in the data transfer state. The off condition of DSR is an indication that the DTE is to disregard all signals appearing on the interchange circuits—except the calling indicator and the test signal. DSR will switch to the off state when in test state. The on condition of DSR indicates the following:

1. The modem is not in the talk state, i.e., an associated telephone handset is not in control of the line.
2. The modem is not in the process of automatically establishing a call via pulse or DTMF dialing.
3. The modem is generating an answer tone or detecting answer tone.
4. After ring indicate goes on, DSR waits at least two seconds before turning on to allow the telephone company equipment to be engaged.

DSR will go off 50 msec after DTR goes off or 50 msec plus a maximum of 4 sec when SSD is enabled. (Note: All time measurements without a tolerance have a ±0.5 ms tolerance.)

DATA TERMINAL READY

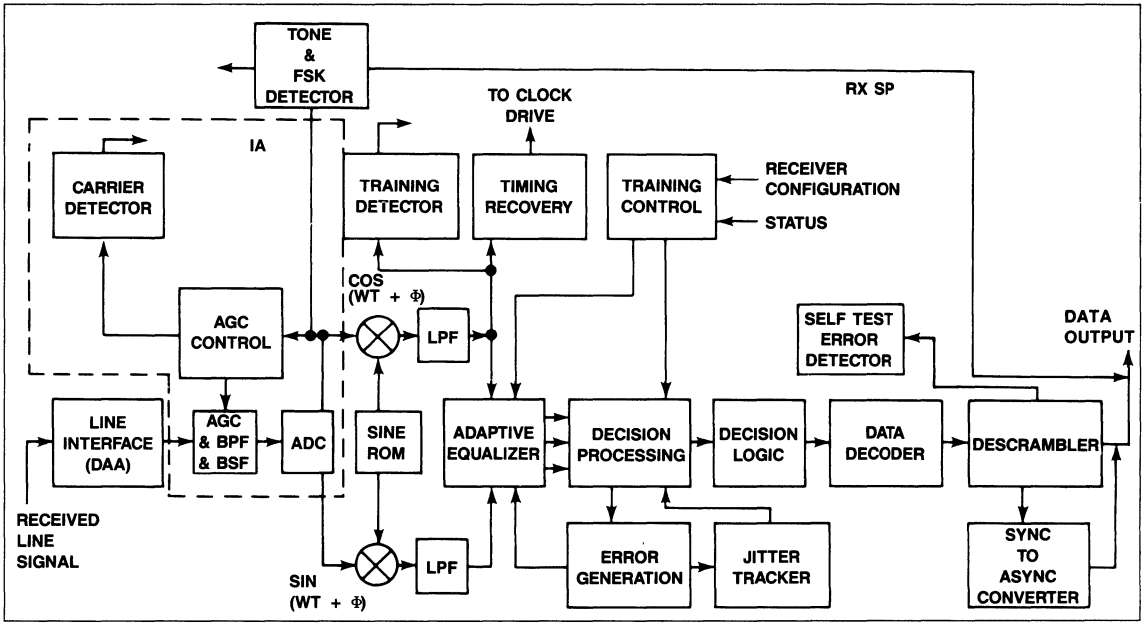
An on condition of DTR prepares the modem to be connected to the communications channel, and maintains the connection established by the DTE (manual answering) or internal (automatic answering) means. The off condition places the modem in the disconnect state.

AUTOMATIC RECONFIGURATION

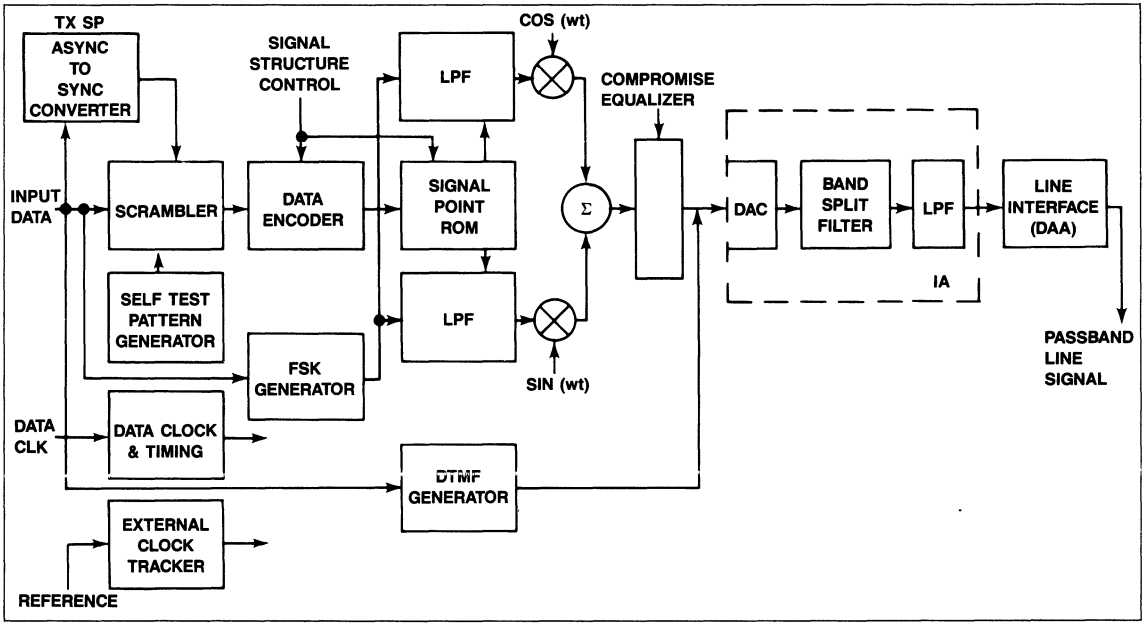
The R2424 is capable of automatically configuring itself to the compatibility of a remote modem. The R2424 can be in either the answer or originate mode for this to occur. The compatibilities that the R2424 are limited to adapt to are V.22 bis, V.22 A/B (1200 bps), Bell 212, and Bell 103. If the R2424 is to originate in a specific configuration, the MODE bits must be set.

RECEIVE/TRANSMIT CIRCUITS

The receiver and transmitter circuits are defined in the following block diagrams:



R2424 Receiver/Equalizer Block Diagram



R2424 Transmitter Block Diagram

MODES OF OPERATION

The R2424 is capable of being operated in either a serial or a parallel mode of operation.

SERIAL MODE

The serial mode uses standard V.24 (RS-232-C compatible) signals to transfer channel data. An optional USART device (shown in the Functional Interconnect Diagram) illustrates this capability.

PARALLEL MODE

The R2424 has the capability of modem control via the microprocessor bus. Data transfer is maintained over the serial V.24 channel.

MODE SELECTION

Selection of either the serial ($\overline{DTR}$, $\overline{RTS}$, $\overline{TLK}$, $\overline{ORG}$) or parallel (DTR, RTS, DATA, ORG) control is by means of the BUS bits ([0,1]:D:7). To enable the parallel control, the BUS bits must be set to a one. The modem automatically defaults to the serial mode at power-on. In either mode, the R2424 is configured by the host processor via the microprocessor bus.

INTERFACE CRITERIA

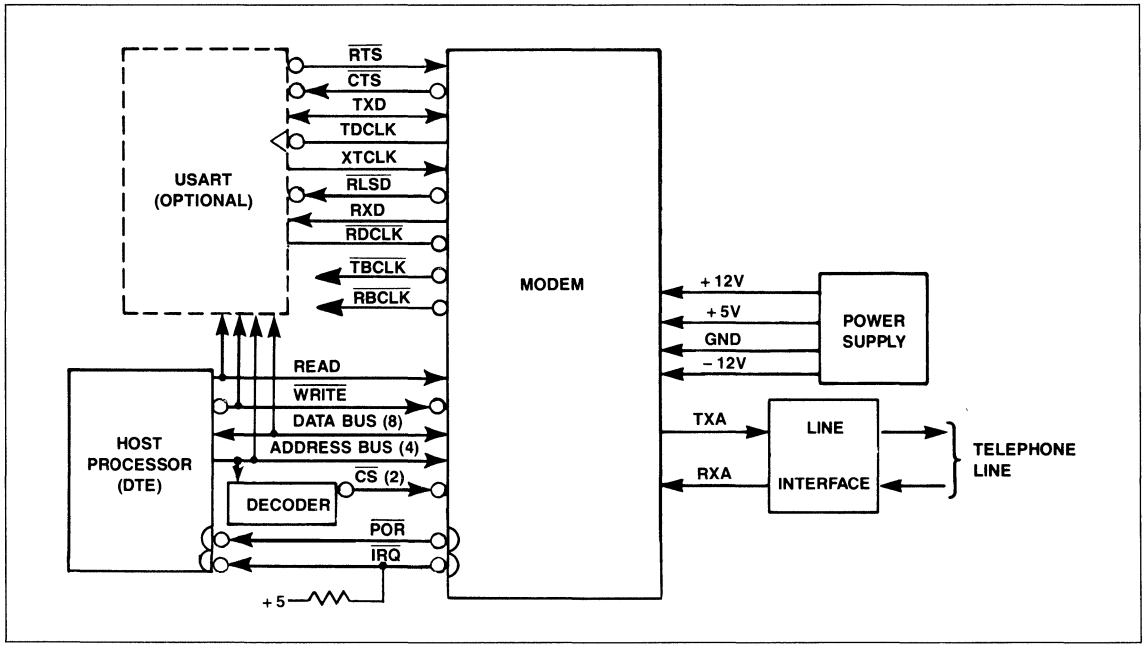
The modem interface comprises both hardware and software circuits. Hardware circuits are assigned to specific pins in a 64-pin DIN connector. Software circuits are assigned to specific bits in a 32-byte interface memory.

HARDWARE CIRCUITS

Signal names and descriptions of the hardware circuits, including the microprocessor interface, are listed in the R2424 Hardware Circuits table. In the table, the column titled 'Type' refers to designations found in the Hardware Circuit Characteristics. The microprocessor interface is designed to be directly compatible with an 8080 microprocessor. With the addition of a few external logic gates, it can be made compatible with 6500, 6800, or 68000 microprocessors.

R2424 Hardware Circuits

Name	Type	Pin No.	Description
A. OVERHEAD			
Ground (A)	AGND	31C, 32C	Analog Ground Return
Ground (D)	DGND	3C, 8C, 5A, 10A	Digital Ground Return
+5 volts	PWR	19C, 23C, 26C, 30C	+5 volt supply
+12 volts	PWR	15A	+12 volt supply
−12 volts	PWR	12A	−12 volt supply
$\overline{POR}$	I/OB	13C	Power-On-Reset

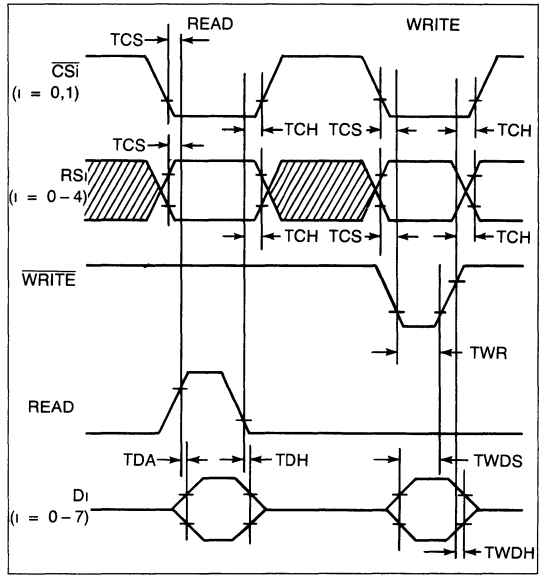


R2424 Functional Interconnect Diagram

R2424 Hardware Circuits (Continued)

Name	Type	Pin No.	Description
B. MICROPROCESSOR INTERFACE:			
D7	I/OA	1C	Data Bus (8-Bits)
D6	I/OA	1A	
D5	I/OA	2C	
D4	I/OA	2A	
D3	I/OA	3A	
D2	I/OA	4C	
D1	I/OA	4A	
D0	I/OA	5C	
RS3	IA	6C	Register Select (4-Bits)
RS2	IA	6A	
RS1	IA	7C	
RS0	IA	7A	
$\overline{CS0}$	IA	10C	Chip Select Receiver Baud Rate Device
$\overline{CS1}$	IA	9C	Chip Select Transmitter Sample Rate Device
READ	IA	12C	Read Enable
$\overline{WRITE}$	IA	11A	Write Enable
$\overline{IRQ}$	OB	11C	Interrupt Request
C. V.24 INTERFACE			
XTCLK	IB	22A	External Transmit Clock
TDCLK	OC	23A	Transmit Data Clock
$\overline{RDCLK}$	OC	21A	Receive Data Clock
$\overline{RTS}$	IB	25A	Request-to-Send
$\overline{CTS}$	OC	25C	Clear-to-Send
TXD	IB	24C	Transmit Data
RXD	OC	22C	Receive Data
$\overline{RLSD}$	OC	24A	Received Line Signal Detector
$\overline{DTR}$	IB	21C	Data Terminal Ready
$\overline{DSR}$	OC	20A	Data Set Ready
$\overline{RI}$	OC	18A	Ring Indicator
D. ANALOG SIGNALS (R2424M ONLY):			
RXA	IB	32A	Receive Analog Input
TXA	OC	31A	Transmit Analog Output
E SIGNALS TO DAA (R2424M ONLY):			
$\overline{RD}$	IB	27A	Ring Detect
RCCT	OC	28A	Request Coupler Cut Through
$\overline{CCT}$	IB	29C	Coupler Cut Through
OH	OC	29A	Off-Hook Relay Control
F. ANCILLARY CIRCUITS			
$\overline{TBCLK}$	OC	27C	Transmit Baud Clock
$\overline{RBCLK}$	OC	26A	Receive Baud Clock
$\overline{TLK}$	IC	28C	Talk (TLK = Data)
$\overline{ORG}$	IB	16C	Originate (ORG = Answer)

MICROPROCESSOR TIMING



Microprocessor Interface Timing Diagram

Critical Timing Requirements

Characteristic	Symbol	Min	Max	Units
$\overline{CSi}$, RSi setup time prior to Read or $\overline{Write}$	TCS	30	—	NS
Data Access time after Read	TDA	—	140	NS
Data hold time after Read	TDH	10	50	NS
$\overline{CSi}$, RSi hold time after Read or $\overline{Write}$	TCH	10	—	NS
Write data setup time	TWDS	75	—	NS
Write data hold time	TWDH	10	—	NS
Write strobe pulse width	TWR	75	—	NS

7

HARDWARE CIRCUIT CHARACTERISTICS

Digital Interface Characteristics

Digital Interface Characteristics

Symbol	Parameter	Units	Input/Output Type							
			IA	IB	IC	OA	OB	OC	I/O A	I/O B
V_{IN}	Input Voltage, High	V	2.0 min.	2.0 min.	2.0 min				2.0 min.	5.25 max.
										2.0 min.
V_{IL}	Input Voltage, Low	V	0.8 max.	0.8 max.	0.8 max.				0.8 max.	0.8 max.
V_{OH}	Output Voltage, High	V				2.4 min.[1]			2.4 min. [1]	2.4 min.[3]
V_{OL}	Output Voltage, Low	V				0.4 max.[2]	0.4 max.[2]	0.4 max.[2]	0.4 max.[2]	0.4 max.[2]
I_{IN}	Input Current, Leakage	μA	±2.5 max.						±2.5 max.[4]	
I_{OH}	Output Current, High	mA				−0.1 max.				
I_{OL}	Output Current, Low	mA				1.6 max.	1.6 max.	1.6 max.		
I_L	Output Current, Leakage	μA					±10 max.			
I_{PU}	Pull-up Current	μA		−240 max.	−240 max.			−240 max.		−260 max.
	(Short Circuit)			−10 min.	−10 min.			−10 min.		−100 min.
C_L	Capacitive Load	pF	5	5	20				10	40
C_D	Capacitive Drive	pF				100	100	100	100	100
	Circuit Type		TTL	TTL w/Pull-up	TTL w/Pull-up	TTL	Open-Drain	Open Drain w/Pull-up	3 State Transceiver	Open-Drain w/Pull-up

Notes
1. I load = −100 μA
2. I load = 1.6 mA
3. I load = −40 μA
4. V_{IN} = 0.4 to 2.4 Vdc, V_{CC} = 5.25 Vdc

Analog Interface Characteristics

TXA—The (Type OC) transmitter output is a low impedance operational amplifier output in series with a 604 ohm resistor. In order to have a 0 dBm output, an external 600 ohm resistor to ground is required.

RXA—The (Type IB) receiver input impedance is 63.4K ohms ±5 percent.

Transmission Line Interface Characteristics

The R2424DC interface to the telephone line is the Tip and Ring leads. Lightning induced surge voltages and other hazardous voltages which may appear on the telephone line are limited to approximately 7V peak between the secondary leads of the line coupling transformer.

The DAA (R2424DC *only*) is bi-directional as required by 2-wire full-duplex circuits.

Connection to the telephone line interface pins of the R2424DC to the network are made via two RJ11 jacks. The pin designations are shown in the table below:

R2424DC Network Interface

Connection Type	Telco	Mnemonic	Function
	1		
VSOC	2		
RJ11	3	R	Ring-one side of telepone line
Jack	4	T	Tip-one side of telephone line
	5		
	6		

Ring Indicator—The R2424 provides a ring indicator ($\overline{RI}$) output; its low state indicates the presence of a ring signal on the line. The low condition appears approximately coincident with the on segment of the ring cycle (during rings) on the communication channel. (The ring signal cycle is typically two seconds on, four seconds off.) The high condition of the indicator output is maintained during the off segment of the ring cycle (between rings) and at all other times when ringing is being received. The operation of $\overline{RI}$ is not disabled by an off condition on Data Terminal Ready.

$\overline{RI}$ will respond to ring signals in the frequency range of 15.3 Hz to 68 Hz with voltage amplitude levels of 40 to 150 Vrms (applied across Tip and Ring), with the response times given in the following table:

RI Response Time

RI Transition	Response Time
Off-to-On	170 ±50 ms
On-to-Off	110 ±50 ms

This off-to-on (on-to-off) response time is defined as the time interval between the sudden connection (removal) of the ring signal across Tip and Ring and the subsequent on (off) transition $\overline{RI}$.

OH—The R2424M provides an output OH (Off-Hook) which indicates the state of the OH relay. A low condition on OH implies the OH relay is closed and the modem is connected to the telephone line. A high condition on OH implies the OH relay is open (i.e., the modem is on-hook). The delay between the low-to-high or high-to-low transition of OH and the subsequent close-to-open or open-to-close transition of the OH relay is 8 ms maximum.

$\overline{RD}$—$\overline{RD}$ indicates to the R2424M by an on (low) condition that a ringing signal is present. The $\overline{RD}$ signal should not respond to momentary bursts of ringing less than 125 ms in duration, or to less than 40V rms, 15 to 68 Hz appearing across Tip and Ring with respect to ground.

RCCT—RCCT is used to request that a data transmission path through the DAA be connected to the telephone line. When RCCT goes off (low), the cut-through buffers are disabled and $\overline{CCT}$ should go off (high) within 1 msec. RCCT should be off during dialing but on for tone address signalling.

$\overline{CCT}$—An on (low) signal to the $\overline{CCT}$ lead indicates to the R2424M that the data transmission path through the DAA is connected.

AUDIO INTERFACE INPUT IMPEDANCE CHARACTERISTICS

Audio Interface Input Impedance Characteristics

On/Off Hook	Measurement
On-Hook (DC)	The DC resistance between Tip and Ring, and between either Tip or Ring and signal ground is greater than 10 megohms for DC voltages up to 100 volts.
On-Hook (AC)	The on-hook AC impedance measured between Tip and Ring is less than 40K ohms (153 Hz minimum).
Off-Hook (DC)	Less than 200 ohms.
Off-Hook (AC)	600 ohms nominal when measured between Tip and Ring.

SOFTWARE CIRCUITS

The R2424 comprises two signal processor chips. Each of these chips contains 16 registers to which an external (host) microprocessor has access. Although these registers are within the modem, they may be addressed as part of the host processor's memory space. The host may read data out of or write date into these registers. The registers are referred to as interface memory. Registers in chip 0 update at the modem baud rate (600 bps) (except RAM access and RAM Data Update where operation is at sample rate). Registers in chip 1 update at the sample rate (7200 bps).

When information in these registers is being discussed, the format Y:Z:Q is used. The chip is specified by Y(0 or 1), the register by Z(0 – F), and the bit by Q (0 – 7, 0 = LSB).

STATUS/CONTROL BITS

The operation of the R2424 is affected by a number of software control inputs. These inputs are written into registers within the interface memory via the host microprocessor bus. Bits designated by an 'X' are "Don't Care" inputs that can be set to either 1 or 0. Modem operation is monitored by various software flags that are read from interface memory via the host microprocessor bus. All status and control bits are defined in the interface Memory table. Bits designated by an 'R' are reserved for modem use only and must not be changed by the host.

RAM Data Access

The R2424 provides the user with access to much of the data stored in the modem's memories. This data is useful for performing certain diagnostic functions.

Two RAM access registers are provided in the interface memory to allow user access to various RAM locations within chip 0 and chip 1. The access code stored in 0:F selects the source of data for the RAM data registers in chip 0 (0:5 through 0:2). Similarly, the access code stored in 1:F selects the source of data for registers 1:5 through 1:2. Reading is performed by first storing the desired access code in register 0:F (or 1:F). The data may then be read from 0:5 through 0:2 (or 1:5 through 1:2).

RAM Access Codes

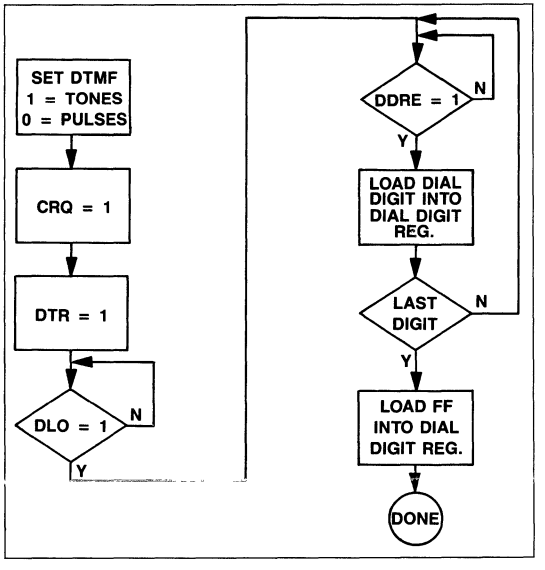
The RAM access codes defined in the following table allow the host processor to read diagnostic information within the modem.

RAM Access Codes (Chip 0)

Function	Access Code	Register No.
Self Test Error Counter	00	2,3
Equalizer Tap Coefficients	01 – 0D	2,3,4,5
Phase Error	10	2,3
Rotated Equalizer Output (Received Point Eye Pattern)	11	2,3,4,5
Rotated Angle	12	4,5
Low Pass Filter Output	40	2,3,4,5
Input Signal to Equalizer Tap Coefficients	41 – 4D	2,3,4,5
Decision Points (Ideal Eye Pattern)	51	2,3,4,5
Rotated Error	52	2,3,4,5
Equalizer Output	53	2,3,4,5
Demodulator Output	56	2,3,4,5

Auto Dial Sequence

The following flow chart defines the auto dial sequence via the microprocessor interface memory.



Auto Dial Sequence Flow Diagram

Note: The modem timing for the auto dialer accounts for inter-digit delay for pulses and tones.

7

The timing for the pulses and tones are as follows:

Pulses — Relay open 64 ms
Relay closed 36 ms
Interdigit delay
750 ms

Tones — Tone duration
71 ms
Interdigit delay
71 ms

Output Level
1.5 ±1 dBm

R2424 Receiver Interface Memory Chip 0 ($\overline{CS0}$)

Register \ Bit	7	6	5	4	3	2	1	0
F	RAM Access B							
E	IRQ	ENSI	NEWS	R	NEWC	R	R	R
D	BUS	CRQ	X	X	X	LCD	RSD	X
C	X	X	X	CHAR		X	X	X
B	X	X	X	X	X	X	X	AL
A	ERDL	RDL	DL	ST	MODE			
9	X	X	SPEED		X	X	X	X
8	TONE	X	X	X	X	X	TM	RLSD
7	R	R	R	R	R	R	R	R
6	R	R	R	R	R	R	R	R
5	RAM Data YBM							
4	RAM Data YBL							
3	RAM Data XBM							
2	RAM Data XBL							
1	R	R	R	R	R	R	R	R
0	R	R	R	R	R	R	R	R
Register / Bit	7	6	5	4	3	2	1	0

Note
(X) indicates user available.
(R) indicates reserved for modem use only.

R2424 Transmitter Interface Memory Chip 1 ($\overline{CS1}$)

Register \ Bit	7	6	5	4	3	2	1	0
F	RAM Access S							
E	IRQ	ENSI	NEWS	R	NEWC	DDEI	R	DDRE
D	BUS	CRQ	DATA	AAE	DTR	X	X	SSD
C	DSRA	TXCLK		CHAR		X	X	X
B	TX LEVEL			GTE	GTS	3DB	DTMF	AL
A	ERDL	RDL	DL	ST	MODE			
9	BRK	RTRN	ORG	LL	RTS	CC	X	X
8	DLO	CTS	DSR	RI	X	X	X	X
7	R	R	R	R	R	R	R	R
6	R	R	R	R	R	R	R	R
5	RAM Data YSM							
4	RAM Data YSL							
3	RAM Data XSM							
2	RAM Data XSL							
1	R	R	R	R	R	R	R	R
0	Dial Digit Register							
Register / Bit	7	6	5	4	3	2	1	0

Note
(X) indicates user available.
(R) indicates reserved for modem use only.

R2424 Interface Memory Definitions

Mnemonic	Name	Memory Location	Description
AAE	Auto Answer Enable	1:D:4	When control bit AAE goes to a one, the modem will automatically answer when a ringing signal is present on the line.
AL	Analog Loopback	(0,1):B:0	When control bit AL is a one, the modem is placed in (V.54 Loop 3) local analog loopback. In this loop, the transmitter's analog output is coupled to the receiver's analog input at a point near the modem's telephone line interface. An attenuator is introduced into the loop such that the signal level coupled into the receive path is attenuated 14 ±1 dBm.
BRK	Break	1:9:7	When control bit BRK goes to a one, the modem transmits 2M + 3 bits of start polarity. (M is equal to the number of bits per character in the selected format.) BRK will reset to zero after the sequence is sent.
BUS	Bus Select	(0,1):D:7	When control bit BUS goes to a one, the modem is placed in the parallel control mode, and when zero the modem is configured for the serial control mode. BUS can be in either state to configure the modem.

R2424 Interface Memory Definitions (Continued)

Mnemonic	Name	Memory Location	Description
CC	Controlled Carrier	1:9:2	When control bit CC goes to a one, the modem is placed in controlled carrier operation; and when zero, the modem is configured for constant carrier operation.
CHAR	Character Length Select	(0,1):C:(3,4)	These character length bits select either 8, 9, 10, or 11 bit characters, as shown below: **Configuration** — **Configuration Word** 8 bits — 0 0 9 bits — 0 1 10 bits — 1 0 11 bits — 1 1
CRQ	Call Request	(0,1):D:6	When control bit CRQ goes to a one, it places the transmitter in auto dial and the receiver in tone detect mode. The data placed in the dial digit register is then treated as digits to be dialed. After the last digit has been dialed, FF (HEX) should be loaded into the dial digit register to tell the modem to go to the data state. CRQ in the transmitter (chip 1) when turned off causes the modem to go on-hook. Therefore, it should be on for the duration of the call and not turned off until it is desired to go on-hook. CRQ in the receiver (chip 0) must be turned off immediately after ringback is detected to put the modem in the data mode, otherwise no answerback tone will be detected.
CTS	Clear-to-Send	1:8:6	When status bit CTS is a one, it indicates to the terminal equipment that the modem will transmit any data which are present at TXD. CTS response times from an on or off condition of RTS are shown below: **CTS Transitions** — **Constant Carrier** — **Controlled Carrier** Off to On — <2 ms — 275 ms On to Off — <2 ms — <2 ms
DATA	Talk/Data	1:D:5	When control bit DATA goes to a one, it places the modem in data state and when zero in the talk state.
DDEI	Dial Digit Empty Interrupt	1:E:2	When control bit DDEI goes to a one, it causes an interrupt to occur when the dial digit register (1:0) is empty (DDRE = 1).
DDR	Dial Digit Register	1:0:(0–7)	DDR is used to load the digits to be dialed. Example: If a 4 is to be dialed, a 04 (HEX) should be loaded. This action also causes the interrupt to be cleared. DDR is a write only register.
DDRE	Dial Digit Register Empty	1:E:0	When status bit DDRE is a one, it indicates that the dial digit register is empty and can be loaded with a new digit to be dialed. After the register is loaded, DDRE goes to a zero.
DL	Digital Loopback (Manual)	(0,1):A:5	When control bit DL is a one, the modem is manually placed in remote digital loopback. DL should be set during the data mode. DSR and CTS will be at zero. The local modem can then be tested from the far-end by using the terminal equipment at the far-end to transmit a test pattern and examine the looped data. At the far-end modem, all interface circuits behave normally as in the data mode. At the conclusion of the test, DL must be reset to zero. The local modem will then return to the normal data mode with control reverting the DTEs, DTR.
DLO	Data Line Occupied	1:8:7	When status bit DLO is a one, it indicates that the modem is in the auto dial state, i.e, CRQ is at a one and the modem is off-hook and ready to dial.
DSR	Data Set Ready	1:8:5	When status bit DSR is a one, it indicates that the answerback tone has been detected, the modem handshake has begun and that the data state will follow. DSR alone should not be used to indicate that the communication channel has been completely established. DSR in conjunction with CTS and RLSD will determine this. DSR will be at zero in all test states (except optionally for analog loopback) and when the channel is being used for voice communication (talk).

R2424 Interface Memory Definitions (Continued)

Mnemonic	Name	Memory Location	Description
DSRA	Data Set Ready In Analog Loopback	1:C:7	When control bit DSRA goes to a one, it causes DSR to be set to a one during analog loopback.
DTMF	Touch Tones/ Pulse Dialing	1:B:1	When control bit DTMF goes to a one, it tells the modem to auto dial using tones, and when zero the modem will dial using pulses.
DTR	Data Terminal Ready	1:D:3	Control bit DTR must be a one, before the modem will enter the data state, either manually or automtically. DTR must also be at a one in order for the modem to automatically answer an incoming call.
ENSI	Enable New Status Interrupt	(0,1):E:6	When control bit ENSI goes to a one, it causes an interrupt to occur when the status bits in registers (0:[8,9]) and (1:8) are updated. (NEWS = 1)
ERDL	Enable Response to Remote Digital Loopback	(0,1):A:7	When control bit ERDL goes to a one, it enables the modem to respond to another modem's remote digital loopback request, thus going into loopback.
GTE	Guard Tone Enable	1:B:4	When control bit GTE goes to a one, it causes the specified guard tone to be transmitted (CCITT Configurations only).
GTS	Guard Tone Select	1:B:3	When control bit GTS goes to zero, it selects the 1800 Hz tone and when a one it selects the 550 Hz tone.
IRQ	Interrupt	(0,1):E:7	When status bit IRQ is a one, it indicates that an interrupt has been generated.
LCD	Loss of Carrier Disconnect	0:D:2	When control bit LCD goes to a one, the modem terminates a call when a loss of received carrier energy is detected after 400 msec. After the first 40 ms of loss of carrier, RLSD goes off. 360 ms later if no carrier is detected, CTS goes off. LCD is not disabled in leased line operation.
LL	Leased Line	1:9:4	When control bit LL goes to a one, it places the modem in leased line operation; and when zero, switched line operation.
MODE	Mode Select	(0,1):A:(0,3)	These bits select the compatibility at which the modem is to operate, as shown below: **Configuration** / **Configuration Word** Bell 212A 1200 Sync. 0 0 1 0 Bell 212A 1200 Async. 0 0 1 1 Bell 212A 300 Async. 0 1 0 0 V.22A 1200 Sync. 1 0 0 0 V.22B 1200 Async. 1 0 0 1 V.22A 600 Sync. 1 0 1 0 V.22B 600 Async. 1 0 1 1 V.22 bis 2400 Sync. 1 1 0 0 V.22 bis 2400 Async. 1 1 0 1 V.22 bis 1200 Sync. 1 1 1 0 V.22 bis 1200 Async. 1 1 1 1
NEWC	New Configuration	(0,1):E:3	When status bit NEWC is a one, it tells the modem that a new configuration has been written into the configuration registers. The modem will then read the configuration registers and then reset NEWC. NEWC must be set after a new configuration has been written into the following registers: (0:[A–D]) and (1:[9–D]). The remaining registers do not require the use of NEWC to tell the modem that new data was written into them.
NEWS	New Status	(0,1):E:5	When status bit NEWS is a one, it tells the user that there has been a change of status in the status registers. The user must write a zero into NEWS to reset it. This action also causes the interrupt to be cleared.

R2424 Interface Memory Definitions (Continued)

Mnemonic	Name	Memory Location	Description
ORG	Originate/Answer	1:9:5	When status bit ORG is a one, it tells the modem that it is originating a call and when a zero answering a call. (This is only valid in manual originate/answer and analog loopback.)
(None)	RAM Access B	0:F:0–7	Contains the RAM access code used in reading RAM locations in chip 0 (baud rate device).
(None)	RAM Access S	1:F:0–7	Contains the RAM access code used in reading RAM locations in chip 1 (sample rate device).
(None)	RAM Data XBL	0:2:0–7	Least significant byte of 16-bit word X used in reading RAM locations in chip 0.
(None)	RAM Data XBM	0:3:0–7	Most significant byte of 16-bit word X used in reading RAM locations in chip 0.
(None)	RAM Data XSL	1:2:0–7	Least significant byte of 16-bit word X used in reading RAM locations in chip 1.
(None)	RAM Data XSM	1:3:0–7	Most significant byte of 16-bit word X used in reading RAM locations in chip 1.
(None)	RAM Data YBL	0:4:0–7	Least significant byte of 16-bit word Y used in reading RAM locations in chip 0.
(None)	RAM Data YBM	0:5:0–7	Most significant byte of 16-bit word Y used in reading RAM locations in chip 0.
(None)	RAM Data YSL	1:4:0–7	Least significant byte of 16-bit word Y used in reading RAM locations in chip 1.
(None)	RAM Data YSM	1:5:0–7	Most significant byte of 16-bit word Y used in reading RAM locations in chip 1.
RDL	Remote Digital Loopback	(0,1):A:6	When control bit RDL goes to a one, it causes the modem to initiate a request for the remote modem to go into digital loopback.
RI	Ring Indicator	1:8:4	When status bit RI is a one, it indicates that a ringing signal is being detected.
RLSD	Received Line Signal Detector	0:8:0	When status bit RLSD is a one, it indicates that the carrier has successfully been received. RLSD will not respond to the 550, 1800, 2100, or 2225 Hz tones. RLSD response times are given below: **RLSD Transitions**[1] — **Constant Carrier** — **Controlled Carrier** Off to On — 40 to 65 ms — 40 to 65 ms On to Off — 40 to 65 ms — 40 to 65 ms **Note:** 1. After handshake has occurred.
RSD	Receive Space Disconnect	0:D:1	When control bit RSD goes to a one, it causes the modem to go on-hook after receiving approximately 1.6 seconds of continuous spaces.
RTRN	Retrain (V.22 bis only)	1:9:6	When control bit RTRN goes to a one, it sends the training sequence. It resets when the sequence is completed.

7

R2424 Interface Memory Definitions (Continued)

Mnemonic	Name	Memory Location	Description
RTS	Request-to-Send	1:9:3	When control bit RTS goes to a one, it allows the modem to transmit data when CTS becomes active. Responses to RTS are shown below: Assume DTR is on, Talk/Data is set to Data (CRQ or AAE is set for a dial line) and the modem is connected to the line (off-hook). **Leased or Dial Line**[1] / **RTS Off** / **RTS On** Controlled Carrier / CTS Off, Carrier Off / Carrier On, 275 ms Scrambled 1's Transmitted, CTS On Constant Carrier / CTS Off, Carrier On, Scrambled 1's Transmitted / CTS On, Carrier On, Data Transmitted **Note:** 1. After handshake is complete. For ease of use in constant carrier mode, RTS should be turned on the same time as DTR.
SPEED	Speed Indication	0:9:(4,5)	00 = 300 bps 10 = 1200 bps 01 = 600 bps 11 = 2400 bps
SSD	Send Space Disconnect	1:D:0	When control bit SSD goes to a one, it causes the modem to transmit approximately 4 seconds of spaces before disconnecting, when DTR is at zero.
ST	Self Test	(0,1):A:4	When control bit ST is a one, self test is activated. ST must be at zero to end the test. It is possible to perform test with or without DTE connected. During any self test, TXD and RTS are ignored. Self test do not test asynchronous-to-synchronous converter circuits in either the transmitter or receiver. Error detection is accomplished by monitoring the self test error counter in the RAM. If the counter increments during the self test, an error was made. The counter contents are available in the diagnostic register when the RAM access code 00 is loaded in the diagnostic control register (0:F). *Self Test End-to-End* Upon activation of self-test an internally generated data pattern of alternate binary ones and zeros (reversals) at the selected bit rate are applied to the scrambler. An error detector, capable of identifying errors in a stream of reversals are connected to the output of the descrambler. *Self Test with Loop 3* Loop 3 is applied to the modem as defined in recommendation V.54 Self-test is activated and DCE operation is as in the end-to-end test. In this test DTR is ignored. *Self Test with Loop 2* The modem is conditioned to instigate a loop 2 at the remote modem as specified in recommendation V 54. Self-test is activated and DCE operation is as in the end-to-end test.
3DB	3 dB Loss to Receive Signal	1:B:2	When control of bit 3DB is a one, it attenuates the received signal 3 dB. This is only used if the R2424M will see 0 dBm or greater line signal at the receiver input. Insertion of the 3 dB loss will then prevent saturation. This bit is not needed with the R2424DC.
TM	Test Mode	0:8:1	When status bit TM is a one, it indicates that the modem has completed the handshake and is in one of the following test modes: AL, RDL, or DL.
TONE	Tone Detect	0:8:7	TONE follows the energy detected in the 340 to 640 Hz frequency band. The user must determine which tone is present on the line by determining the duty cycle of the TONE bit. TONE is active only when CRQ in chip 0 is a one.

R2424 Interface Memory Definitions (Continued)

Mnemonic	Name	Memory Location	Description
TXCLK	Transmit Clock Select	1:C:(5,6)	TXCLK allows the user to designate the origin of the transmitter data clock, as shown below: **Transmit Clock** — **Configuration Word** Internal — 0 0 Not Used — 0 1 External — 1 0 Slave — 1 1
TX LEVEL	Transmit Level	1:B.(5-7)	TX LEVEL allows the User to change the R2424M transmitter output level, assuming the modem is transmitting into a 600 ohm load. **Transmit Level (±1.0 dBm)** — **Configuration Word** 0 dBm — 0 0 0 -2 dBm — 0 0 1 -4 dBm — 0 1 0 -6 dBm — 0 1 1 -8 dBm — 1 0 0 -10 dBm — 1 0 1 -12 dBm — 1 1 0 -14 dBm — 1 1 1

POWER-ON INITIALIZATION

When power is applied to the R2424, a period of 50 to 300 ms is required for power supply settling. The power-on reset signal (POR) remains low during this period. Approximately 10 ms after the low to high transition of POR, the modem is ready to be configured, and RTS may be activated. If the 5 Vdc power supply drops below 3.5 Vdc for more than 30 msec, the POR cycle is repeated.

At POR time the modem automatically defaults to V.22 bis 2400 bps, answer state using serial start-stop data, 10 bits per character, constant carrier, dial line.

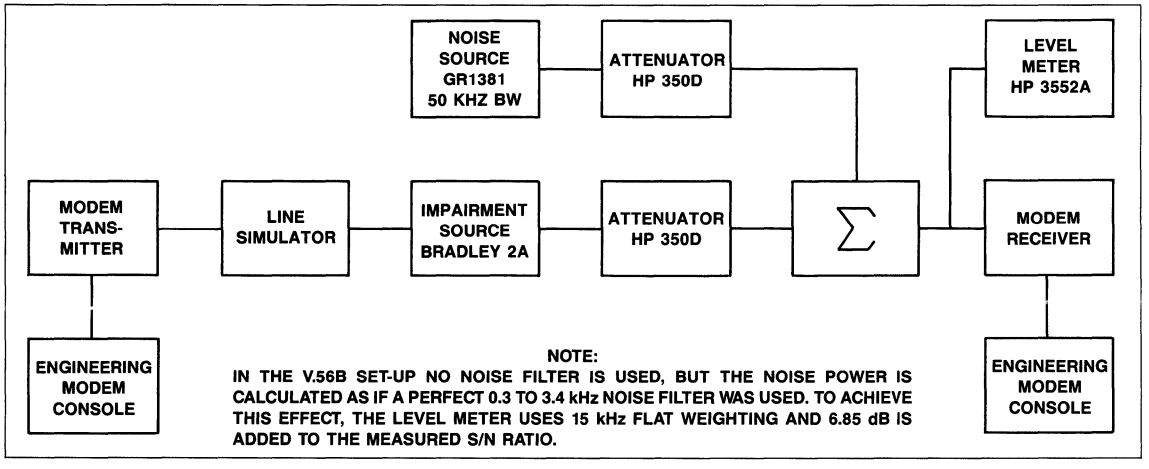
POR can be connected to a user supplied power-on-reset signal in a wire or configuration. A low active pulse of 3 μsec or more applied to the POR pin causes the modem to reset. The modem is ready to be configured 10 msec after the low active pulse is removed from POR.

PERFORMANCE

Whether functioning as a V.22 bis, V.22, or Bell 212A type modem, and regardless of simulated line condition or introduced line impairment, the R2424 provides unexcelled high performance to the user.

BIT ERROR RATES

The Bit Error Rate (BER) performance of the R2424 is specified for a test configuration conforming to that specified in CCITT Recommendation V.56, except with regard to the placement of the filter used to bandlimit the white noise source. Bit error rates are measured at a received line signal level of -43 dBm.



BER Performance Test Setup

GENERAL SPECIFICATIONS

Power

Voltage*	Tolerance	Current (Max)
+5 Vdc	±5%	<500 ma
+12 Vdc	±5%	< 10 ma
−12 Vdc	±5%	< 50 ma

*All voltages must have ripple ≤0.1 volts peak-to-peak.

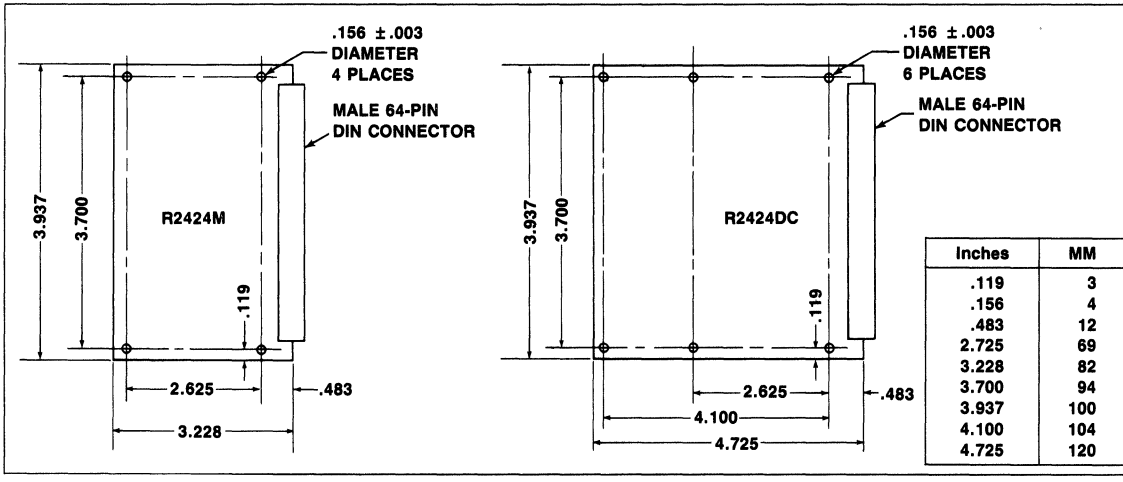
Environmental

Parameter	Specification
Temperature	
Operating	0°C to +60°C (32 to 140°F)
Storage*	−40°C to +80°C (−40 to 176°F)
Relative Humidity	Up to 90% noncondensing, or a wet bulb temperature up to 35°C, whichever is less.
Altitude	−200 to +10,000 feet

*PCB's are stored in heat sealed antistatic bags and shipping containers.

Mechanical

Board Structure	Single PC board with right angle male DIN connector.
Mating Connector	Female 3 row 64 pin Euroconnector (DIN) with rows A and C populated. Recommended mating connector: Winchester 96S-6043-0531-1 or equivalent.
PCB Dimensions	
R2424DC Version	Width 3.94 in. (100 mm) × Length 4.725 in. (120 mm) × Height 0.75 in. (19 mm)
R2424M Version	Width 3.94 in. (100 mm) × Length 3.23 in. (82 mm) × Height 0.40 in. (10 mm)
Weight	Less than 0.45 lbs. (0.20 kg.)
Lead Extrusion	0.100 in. (2.54 mm) max.



Inches	MM
.119	3
.156	4
.483	12
2.725	69
3.228	82
3.700	94
3.937	100
4.100	104
4.725	120

R2424 Printed Circuit Board Dimensions

INSTALLATION

IMPORTANT NOTICE TO USER

The R2424DC contains protective circuitry registered with the Federal Communications Commission (FCC) Part 68 to allow direct connection to the switched telephone network. To comply with the FCC regulations the following is required:

1. All direct connections to the telephone lines shall be made through standard plugs and telephone company provided jacks.
2. It is prohibited to connect the modem to pay telephones or party lines.
3. You are required to notify the local telephone company prior to the connection and upon final disconnection of the modem. You must supply to the telephone company the make, model number, FCC registration number, ringer equivalence and particular line to which the connection is to be made. If the proper jacks are not available, you must order the type of jacks to be used from the telephone company.
4. You should disconnect the modem from the telephone line if it appears to be malfunctioning. Reconnect it only when it can be determined that the telephone line is the source of trouble. If the modem needs repair, return it to Rockwell International. This applies to equipment both in and out of warranty. Do not attempt to repair the unit as this will violate FCC rules.
5. The modem contains protective circuitry to prevent harmful voltages from being transmitted to the telephone network. If however such harmful voltages do occur, then the telephone company shall:
   - Promptly notify you of the discontinuance.
   - Afford you the opportunity to correct the situation which caused the discontinuance.

   The FCC requires that the following label be prominently displayed on an outside surface of the OEM's end product.
   - Unit contains Registered Protective Circuitry which complies with Part 68 of FCC Rules.
   - FCC Registration Number: Applied For
   - Ringer Equivalence: 0.5

   Size of the label should be such that all the required information is legible without magnification.

Rockwell

R24DC
2400 BPS DIRECT CONNECT MODEM

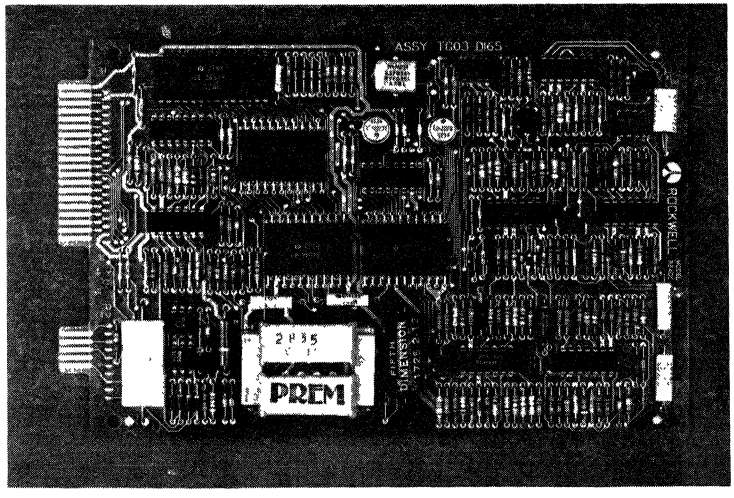
INTRODUCTION

The Rockwell R24DC is a high performance synchronous serial 2400 bps DPSK modem. Extensively utilizing MOS/LSI technology with registered protective circuitry, the R24DC is ideally suitable for direct connection to the domestic switched network or two-wire private lines. Performance and versatility are enhanced while cost and size are reduced by the on-board Rockwell PPS-4/1 One Chip Microcomputer

Having Bell 201C and CCITT V.26 bis compatibility, the R24DC offers the user a high performance 2400 bps modem that is FCC registered for direct connection to the dial-up network. No re-registration of OEM equipment is required when the simple installation instructions, supplied with the R24DC, are followed. OEM's can easily incorporate this single (5″ × 8″) card into their computer terminals, communication networks, PABX equipment, data concentrators, stand-alone box modems or almost any application where reliable data communication is required.

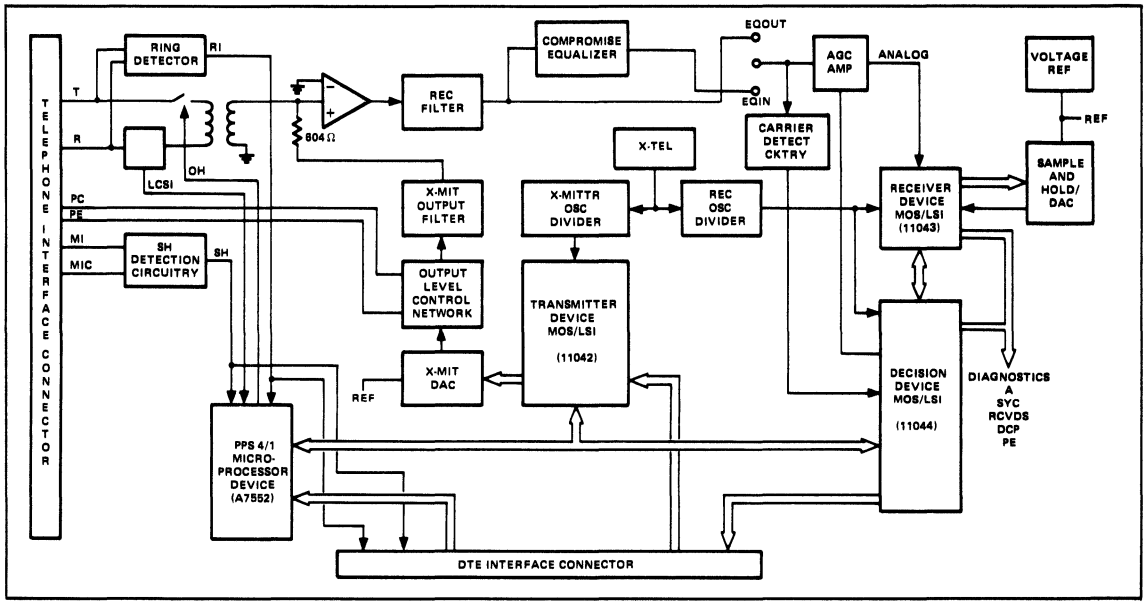
FEATURES

- High Performance; Low Cost
- LSI High Density; Low Power
- Microcomputer Controlled Line Connect/Disconnect Sequence; Low Component Count
- Bell 201 C, CCITT V.26 bis Compatible
- Half Duplex (2-Wire) Operating Mode
- 2400 BPS Data Rate
- Auto or Manual Answer
- Auto or Manual Dial Through (Pulse Dialing)
- Automatic Answer Back Tone Generation upon Auto Answer
- Direct Connect to Switched Network
- Programmable or Permissive Connection Arrangement
- Local Analog Loopback Test Mode
- Compromise Equalizer (Strap Selectable)
- Scrambler/Descrambler Facility (Selectable)
- Line Current Sensing (Selectable)
- DTE Interface LSTTL/CMOS Compatible Levels. RS-232-C Functions
- External Transmit Data Clock Tracking
- Power Requirements, ±12V, +5V
- Typical Power Consumption 3 Watts
- Diagnostic Outputs Available for Eye Pattern and Data Quality Monitor
- 15 Second Abort Timer (Selectable)



R24DC Modem

FUNCTIONAL SPECIFICATIONS



R24DC Functional Block Diagram

Transmitter Carrier Frequency — 1800 Hz ±0.01%

Echo Suppression and Answering Tone Frequencies — 2100 Hz ±0.01% or 2025 Hz ±0.01%.

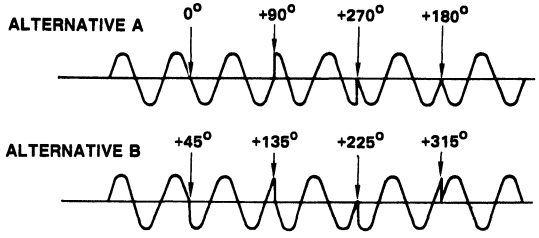
Received Signal Frequency Tolerance — The receiver can adapt to received frequency errors up to ±10 Hz with less than a 0.5 dB degradation in bit error rate.

Data Signaling and Modulation Rate — The normal signaling rate is 1200 baud ±0.01%, and a data rate of 2400 bps ±0.01%. The fallback signaling rate is 1200 baud ±0.01%, and a data rate of 1200 bps ±0.01%.

Transmitted Data Spectrum — The transmitted spectrum's bandwidth extends from 800 Hz to 2800 Hz. Phase distortion characteristics are within the limits specified in CCITT Recommendation V.26 bis. The out of band signal power limitations meet those specified by Part 68 or Tariff 261 of the FCC's regulations, and typically exceed the requirements of international regulatory bodies as well.

Data Encoding (DPSK) — At 2400 bps, differential 4-phase modulation is employed. The data stream to be transmitted is divided into pairs of consecutive bits (dibits). Each dibit is encoded as a phase change relative to the phase of the immediately preceding signal element. Two alternative arrangements of coding are possible (in accordance with CCITT Recommendations V.26 and V.26 bis) as shown in the following chart.

2400 BPS		
	PHASE CHANGE	
DIBIT	V.26A	V.26B/Bell 201
0 0	0°	+45°
0 1	+90°	+135°
1 1	+180°	+225°
1 0	+270°	+315°



Reference Line Signal Diagram (V.26 A&B)

At 1200 bps, differential 2-phase modulation is employed. Each bit to be transmitted is encoded as a phase change relative to the phase of the immediately preceding signal element. The encoding is in accordance with CCITT Recommendation V.26 bis as shown in the following chart.

1200 BPS	
BIT	PHASE CHANGE
0	+90°
1	+270°

Turn On Sequences — A total of six selectable turn on sequences can be generated by the transmitter of the R24DC, as shown in the following chart.

TYPE OF LINE SIGNAL	SEGMENT 1	SEGMENT 2	TOTAL OF SEGMENTS 1, 2	
TURN-ON SEQUENCE NUMBER	CONTINUOUS UNSCRAMBLED ONES	CONTINUOUS SCRAMBLED[1] ONES	NOMINAL TOTAL TURN ON SEQUENCE TIME[2]	COMMENTS
1	90 ms	0 ms	90 ms	V.26, V.26 bis
2	8.33 ms	81.67 ms	90 ms	(scrambler inserted)
3	148.3 ms	0 ms	148.3 ms	Bell 201C
4	8.33 ms	140 ms	148.3 ms	(scrambler inserted)
5	220 ms	0 ms	220 ms	V.26 bis
6	8.33 ms	211.7 ms	220 ms	(scrambler inserted)

As is evident from the above for those turn-on sequences for which the scrambler is inserted, the transmitted line signal corresponds to a continuous "one", unscrambled, for 8.33 ms-ten baud (symbol) intervals – followed by the transmission of a continuous "one", scrambled, for the remainder of the turn-on sequence.

Turn Off Sequence — When the R24DC transmitter has been sending data and Request-to-Send is turned off, any remaining data bit information is transmitted within 6 milliseconds.

Response Times of Clear-to-Send — The Clear-to-Send response times are determined by the selected configuration of the R24DC and its associated turn-on sequence, as shown in the following chart.

TURN-ON SEQUENCE NUMBER	CLEAR-TO-SEND RESPONSE TIMES[1]		
	OFF-TO-ON	ON-TO-OFF	COMMENTS
1	90 ms	0 ms	V.26 bis
2	90 ms	0 ms	V.26 bis w/scrambler
3	148.3 ms	0 ms	Bell 201C
4	148.3 ms	0 ms	Bell 201C w/scrambler
5	220 ms	0 ms	V.26 bis
6	220 ms	0 ms	V.26 bis w/scrambler

The tolerance on each Off-to-On and On-to-Off response time is (+3.4, -0.1) ms.

Scrambler/Descrambler — The R24DC incorporates a self-synchronizing scrambler/descrambler. This feature is enabled by a discrete digital input.

Carrier Detection — The receiver circuit of the R24DC contains a received line signal detector which indicates the presence of energy at the receiver input above a certain threshold for a minimum amount of time.

Carrier Detect Thresholds

Received Level	Carrier Detect
Greater than -43 dBm	On (Line signal present)
Less than -48 dBm	Off (Line signal not present)

Carrier Detect Response Time

Carrier Detect Transition	Response Time
Off-to-On	14 ±1 ms
On-to-Off	8 ±3 ms

Clamping — The following clamps are provided:

1. Received Data. The Received Data output is clamped to a mark when Carrier Detect is off. This action prevents disturbances on the line from getting through the receiver circuit to the data output.
2. Carrier Detect Clamp. The Carrier Detect output is clamped off (squelched) during the time when Request-to-Send is on. An option extends this clamp for 148 ms beyond transitioning off; thus providing echo protection.
3. Receive Clock Clamp. The Receive Clock output is clamped off when Carrier Detect is off. This action prevents any disturbances from propagating through the receiver circuit to the receive clock output.

Equalizer — The R24DC contains a fixed compromise delay equalizer, which can be used to improve performance over the domestic switched network. The equalizer may optionally be positioned in the receiver, or removed entirely, by means of a jumper plug. The equalizer has a nominally flat 0.0 dB amplitude response.

Test Pattern Generation — The scrambler/descrambler function can be used to implement a 127-bit test pattern feature. For example, a constant mark input could be scrambled and transmitted as a pseudo-random signal to be descrambled at the receiver back to the constant mark. A transmission error would be represented as a space for the duration of an incorrect bit.

Receive Level — The R24DC receives line signals from 0 to -43 dBm.

Transmit Timing — The R24DC generates a Transmit Clock having the following characteristics: Frequency — 2400 Hz ±0.01% (1200 Hz ±0.01% in fallback mode), duty cycle — 50 ±1%. The R24DC is also optionally capable of tracking an External Transmit Clock supplied by the user. Both have similar characteristics.

Receive Timing — The modem provides a data derived Receive Clock output in the form of a nominal squarewave (50 ±1% duty cycle). The modem timing recovery function is capable of tracking a ±0.01% frequency error in the associated transmit timing source.

Transmit Level — The R24DC transmitted output line signal level may be regulated in either the permissive or programmable modes. In the permissive mode, the transmitted line signal level is -9 dBm maximum. In the programmable mode, the transmitted line signal level is set by an external resistor installed by the telephone company in the wall jack. Using this method, the transmitted line signal level can be controlled in increments of 1 dBm from 0.0 to -12 dBm, depending on the value of resistance installed.

Answering Tone Generation — When in the automatic answering mode, the R24DC generates a selectable answering tone of 2100 Hz ±0.01% or 2025 Hz ±0.01%. It is also capable of optionally providing this tone when in the manual answer mode.

Answering Tone Frequency

INPUT SELECT 1 (P1-34)	ANSWERING TONE FREQUENCY
High	2100 Hz
Low	2025 Hz

Satellite Option and DSR Selection

Satellite Option	DSR (P1-30) During Analog Loopback	AL-DSR Enable (P1-12)
Yes	OFF (High)	High
No	ON (Low)	Low
Yes	ON Low)	Wired to Analog Loopback
No	OFF (High)	Wired to Analog Loopback [1].

1. Inverse of Signal applied to Analog Loopback Input.

Baud Clocks — Symbol or baud timing is available for both the transmitter and receiver functions. These signals have characteristics similar to the data clocks except that their frequency is equal to the signalling rate of 1200 Hz ±0.01%.

Analog Loopback — The R24DC can be locally commanded into local analog loopback (CCITT Loop 3) via digital input Analog Loopback, when in the wait mode.

Data Structure

INPUT		
DATA SIGNALLING RATE SELECTOR (P1-16)	V.26 A/B (P1-14)	DATA STRUCTURE
Low	Low	2400 bps Alternate A
Low	High	2400 bps V.26 Alternate B (Bell 201C)
High	Low or High	1200 bps

Abort Timer — The R24DC contains a 15 ±1 second abort timer, which may be enabled via the Abort Enable input.

Line Current Interrupt Disconnect — The R24DC contains a 475 ±125 ms line current interrupt abort timer, which may be enabled via the LCIS Enable input.

The digital interchange circuits provide control, status indicators, data clocks and data interface. Traditional RS232-type control functions and additional signals allow the user to access the inherent flexibility and monitoring capabilities of the R24DC.

Carrier Detect Squelch

INPUTS			
ANALOG LOOPBACK (P1-33)	SELECT 2 (P1-35)	REQUEST-TO-SEND (P1-11)	SQUELCH STATUS[1]
Low	Low or High	Low or High	No Squelch
High	Low or High	Low	Squelch
High	High	Low→High	Extended Squelch[2]
High	Low	Low→High	No Extended Squelch

"Squelch" means that Carrier Detect is clamped off (high) regardless of the level of received line signal. When "extended squelch" is enabled, squelch occurs both during the time when Request-to-Send is on (low) and for 148.3 ms (+3.4, -0.1 ms) following the On-to-Off transition of Request-to-Send.

Selection Of Clear-To-Send Response Times

TURN-ON SEQUENCE	INPUTS			CLEAR-TO-SEND RESPONSE TIME[1] (ms)	
	SELECT 1 (P1-34)	SCRAMBLER ENABLE (P1-15)	SELECT 2 (P1-35)	OFF-TO-ON	ON-TO-OFF
1	High	Low	Low	90	0
2	High	High	Low	90	0
3	Low	Low	Low or High	148.3	0
4	Low	High	Low or High	148.3	0
5	High	Low	High	220	0
6	High	High	High	220	0

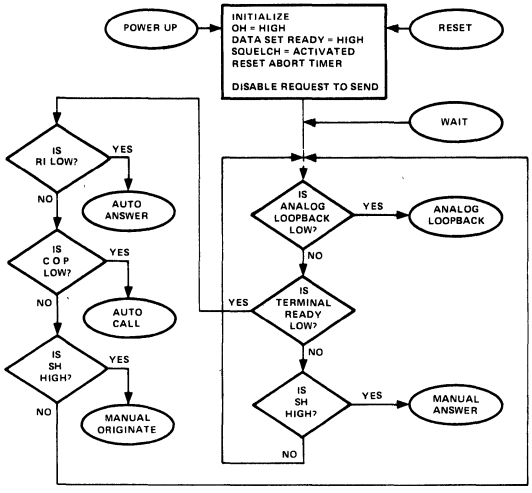
The tolerance on each Off-to-On and On-to-Off response is (-3.4, -0.1 ms).

7

OPERATING MODES

Line connect and disconnect sequences are controlled automatically by the R24DC which is at all times in one of the following modes:

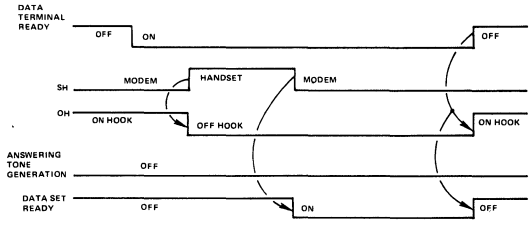
Wait Mode — This is a hot-standby mode. The R24DC enters this mode upon a power-up, Reset, or whenever an operational mode is exited. The following diagrams illustrate the sequence of events for the Wait mode.



Wait Mode Flow Diagram

Analog Loopback Mode — This mode provides the capability of diagnosing a problem in the communications link. In this mode, the transmitter's analog output is connected to the receiver's analog input through an attenuator.

Manual Originate Mode — This mode provides the capability of manual call origination. Calls may be originated in the usual manner by a telephone set. Signal sequence for this mode is shown in the following diagram.



Manual Originate Mode Sequence

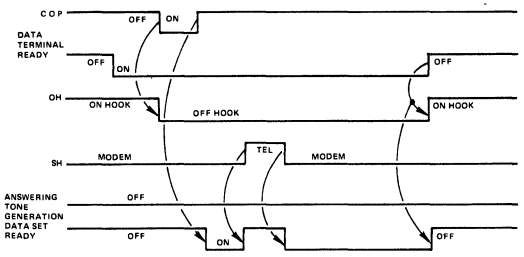
Automatic Call Mode — This mode provides the capability of automatically originating calls by using the pulse dialing technique.

The R24DC allows the user to auto dial by controlling inputs DTR, C.O.P. and DP. To originate a call, DTR and C.O.P. must be on. Then DP (normally off) is pulsed at a rate of 9.5 ±1.5 pulses per second.

The pulse requirement is a uniform train with break intervals at 58% to 64%.

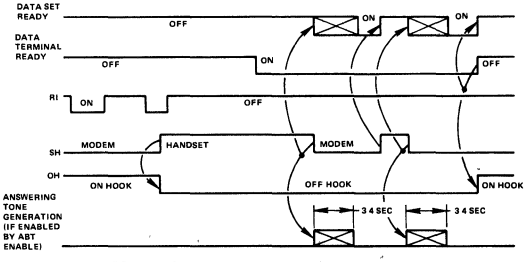
The interdigit time (i.e., the time between the end of the last pulse of a given digit and the beginning of the first pulse of a subsequent digit) should be between 700 ms and 3 seconds.

C.O.P. is turned off after the called modem answers. Signal sequence for this mode is shown in the following diagram.



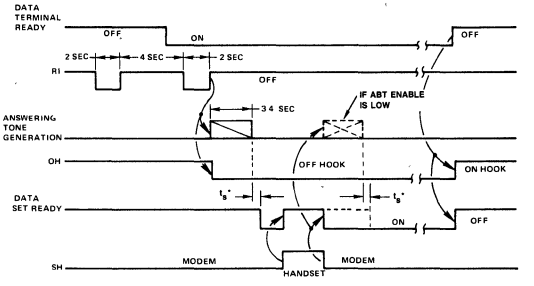
Automatic Call Mode Sequence

Manual Answer Mode — This mode provides the capability of manually answering calls with a telephone set. Signal sequence for this mode is shown in the following diagram.



Manual Answer Mode Sequence

Automatic Answer Mode — This mode provides the capability of automatically answering calls. Signal sequence for this mode is shown in the following diagram.



t_S^* = 275 ms if satellite option is selected
= 65 ms if satellite option is not selected

Automatic Answer Mode Sequence

INTERFACE CRITERIA

The R24DC interface signals are classified as digital interchange signals and analog signals. These signals interface to the user through the board edge connector.

Digital Interchange Circuits — The characteristics of the R24DC digital inputs and outputs are given in the following charts.

Digital Input Characteristics

Input Logic State	Allowed Input Voltage Levels
Low High	0.0V to 0.8V sinking <10 μA +4.0V (VSS - 1V) to +5.0V (VSS) sourcing <10 μA
The digital inputs are directly CMOS compatible. The capacitive loading on each input is 25 pF (maximum).	

Digital Output Characteristics

Ouput Logic State	Allowed Output Voltage Levels
Low High	0.0V to 0.4V sinking 0.36 mA 4.0V (VSS - 1V) to 5.0V (VSS) sourcing 100 μA
The digital outputs are directly CMOS or low-power Schottky TTL compatible.	

DIGITAL OUTPUT CHARACTERISTICS (EXCEPTIONS)

The exceptions to the above are outputs OH, RI, SH and A. Outputs OH, RI and SH have the following characteristics:

Output Logic State	Allowed Output Voltage Levels
Low High	0.0V to 0.4V sinking 0.36 mA 2.4V to 5.0V (VSS) sourcing 100 μA

Output A, useful in the generation of eye pattern and diagnostic information, switches from +5.0V to −12.0V.

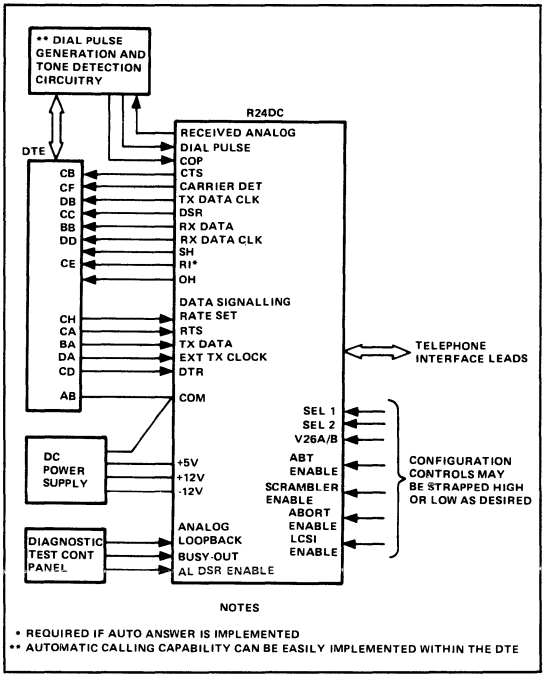
Audio Interface Input Impedance

Parameter	Specification
On-Hook DC	DC resistance between Tip and Ring, and between either Tip or Ring and signal ground is greater than 10 megohms for DC voltages up to 100 volts.
On-Hook AC	On-hook AC impedance measured between Tip and Ring is less than 40 K ohms (15.3 Hz minimum)
Off-Hook DC	Less than 200 ohms
Off-Hook AC	600 ohms nominal when measured between Tip and Ring
Longitudinal Balance	Meets requirements of FCC Rules, Part 68
FCC Registration Number· AMQ9SQ-68813-DM-R Ringer Equivalence. 0 9B	

Analog Interface Circuits — The analog interface circuits defined in the following charts provide power and switched network connections and a means for the user to monitor the incoming line signals.

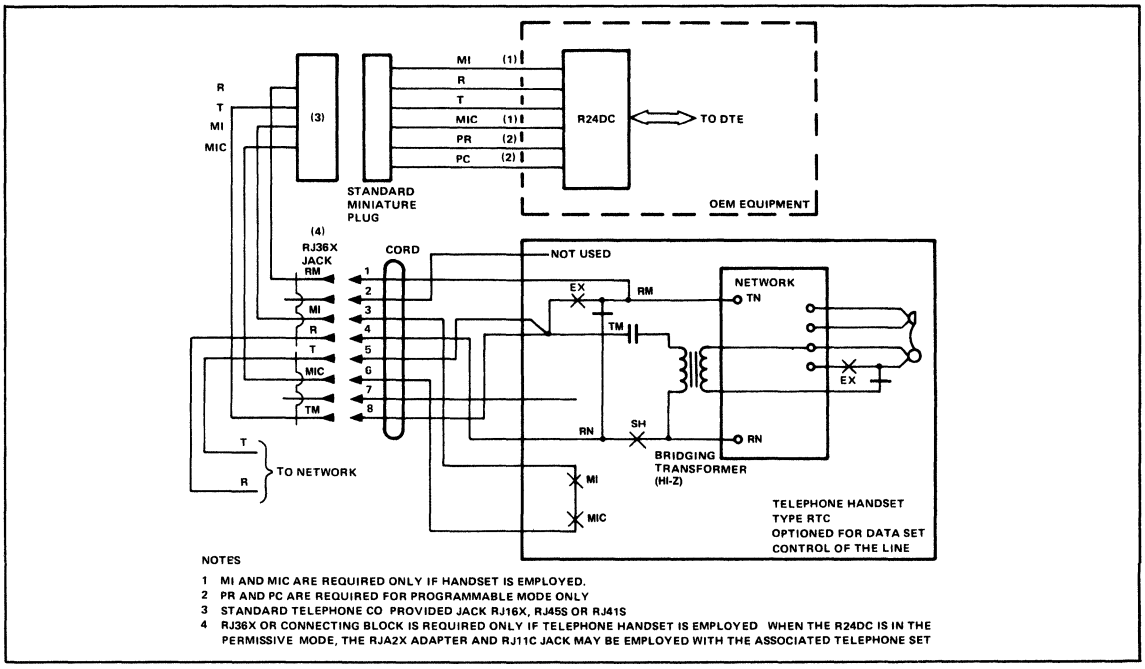
Analog Interface Circuits

TERM	PIN NUMBER	DESCRIPTION
+12V	P1-40	+12V Power Supply
-12V	P1-38	-12V Power Supply
+5V	P1-1	+5V Power Supply
COMMON	P1-2, P1-4	Ground (signal and power return)
Receiver Analog	P1-32	Low impedance output of R24DC receive filter. Gain from Tip and Ring to Receiver Analog is nominally 12.7 dB
		TELEPHONE INTERFACE LEADS
TIP RING	P2-9 P2-10	Telephone Line Leads
PR PC	P2-2 P2-4	Leads to external wall jack resistor for programmable mode
MI MIC	P2-3 P2-1	Leads routed to contact on exclusion key of associated telephone set



Typical R24DC to OEM Interconnections for Half-Duplex Applications

7



NOTES

1 MI AND MIC ARE REQUIRED ONLY IF HANDSET IS EMPLOYED.
2 PR AND PC ARE REQUIRED FOR PROGRAMMABLE MODE ONLY
3 STANDARD TELEPHONE CO PROVIDED JACK RJ16X, RJ45S OR RJ41S
4 RJ36X OR CONNECTING BLOCK IS REQUIRED ONLY IF TELEPHONE HANDSET IS EMPLOYED WHEN THE R24DC IS IN THE PERMISSIVE MODE, THE RJA2X ADAPTER AND RJ11C JACK MAY BE EMPLOYED WITH THE ASSOCIATED TELEPHONE SET

Typical R24DC to Network Interconnection

Telephone Line and OEM Connections — Connection of the R24DC telephone interface pins to the network is made via standard jacks and plugs. A typical installation, including an optional telephone set, is illustrated.

Telephone Set — If it is desirable to have manual call origination or alternate voice capability, an exclusion key telephone set (configured as Modem Controls the Line) may be ordered from your local telephone company.

Mounting and Signal Routing — The R24DC may be physically incorporated into your OEM end product by using either the four corner (0.156 inch) diameter mounting holes or by using board guides. The electrical interface is via edge connector(s).

Interface Mating Connectors

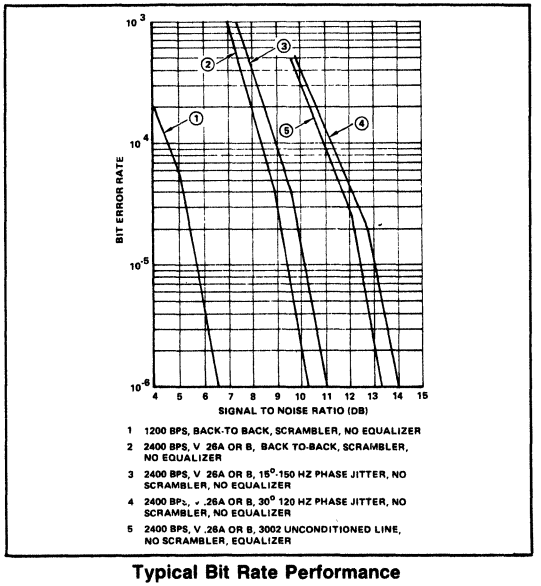
Type/ Manufacturer	P1 (DTE) Connector	P2 (Telephone Line) Connector
Type:	40 pin 0.100 in. spacing 20 pins per side	10 pin 0.100 in. spacing 20 pins per side
Winchester: T&B Ansley: Spectra-Strip:	53-40-0 609-4015M 807-4005-001	53-10-0 609-1015M 807-1005-001

PERFORMANCE DATA

The R24DC is a high performance synchronous 2400 bps DPSK modem, utilizing a coherent demodulation technique to achieve reliable operation over the switched network or unconditioned lines.

Timing Jitter — The maximum steady state timing jitter of Received Clock with respect to Transmit Clock is less than 10% p-p for an input signal-to-noise ratio of 12 dB.

Bit Error Rate — The following graph represents typical R24DC performance.

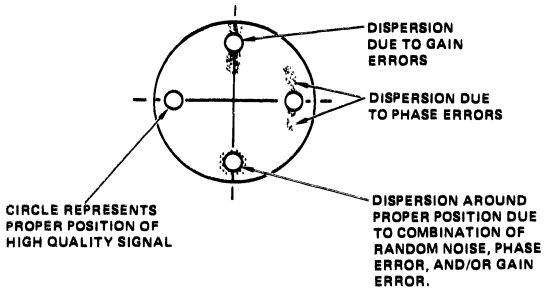


1 1200 BPS, BACK-TO BACK, SCRAMBLER, NO EQUALIZER
2 2400 BPS, V .26A OR B, BACK TO-BACK, SCRAMBLER, NO EQUALIZER
3 2400 BPS, V .26A OR B, 15°-150 HZ PHASE JITTER, NO SCRAMBLER, NO EQUALIZER
4 2400 BPS, V .26A OR B, 30° 120 HZ PHASE JITTER, NO SCRAMBLER, NO EQUALIZER
5 2400 BPS, V .28A OR B, 3002 UNCONDITIONED LINE, NO SCRAMBLER, EQUALIZER

Typical Bit Rate Performance

Phase Error — Phase error can be measured by using the modem's output signals PE, SYC, and A. With an external test circuit, a numerical value can be derived to indicate the quality of received data. This numerical value can be directly correlated to bit error rate performance. The required test circuit can be implemented with discrete circuitry or in software within a microcomputer.

Eye Pattern — By using the modems digital output signals RCVDS, SYC, and A along with an added test circuit, the user can generate an oscilloscope quadrature eye pattern. This pattern displays the received signal as a group of dots in the baseband signal plane; hence, it is a graphic representation of modem performance.



Typical Eye Pattern: 4 Phase-2400 BPS-1200 Baud (V26A)

Phase error and eye pattern can be extremely useful for modem acceptance testing, product evaluation, and observation of line signal quality under actual operation.

POWER REQUIREMENTS

Voltage	Ripple	Maximum Current
+5 VDC ±5%	100 mV p-p	110 mA
+12 VDC ±5%	50 mV p-p	70 mA
-12 VDC ±5%	50 mV p-p	140 mA

ENVIRONMENTAL SPECIFICATIONS

Operating Temperature: 0°C to 60°C
Storage Temperature: -40°C to +90°C
Relative Humidity: to 95% (non-condensing)
Altitude: -200 to 10,000 feet (-61 meters to 3,049 meters)
Burn-In: 96 hours at 70°C

MAXIMUM DIMENSIONS

Width: 4.988 in. (12.669 cm)
Length: 7,900 in. (20.066 cm)
Height: 0.500 in. (1.270 cm)

Rockwell

R24LL
2400 BPS MODEM

INTRODUCTION

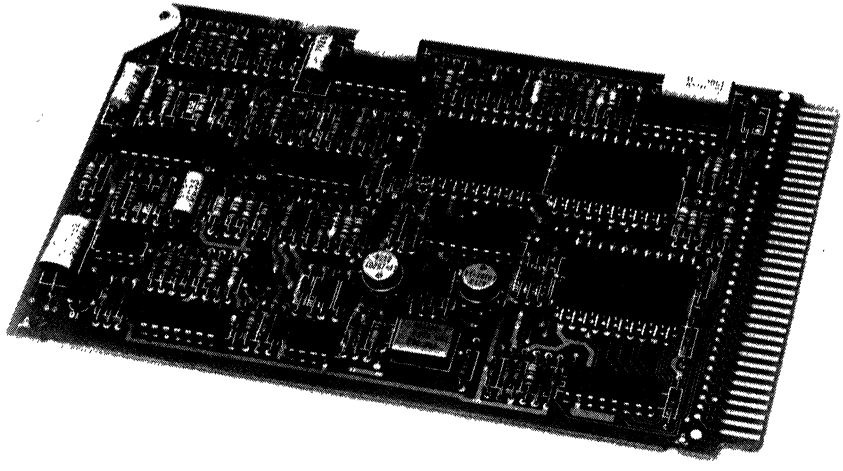
The Rockwell R24LL is a high-performance serial synchronous 2400 bps DPSK modem. By utilizing state-of-the-art MOS/LSI technology, the R24LL provides the user with enhanced performance and reliability in a small package. Implemented on a single printed circuit board, the R24LL is less than 26 square inches.

The R24LL operates in either the full-duplex (4-wire telephone connection) or half-duplex (2-wire telephone connection) mode. The R24LL is designed for easy integration into a user's system, e.g., a simple box or rack-mount modem, statistical multiplexor, error controller, terminal, PBX, or any other communications product that requires the utmost in reliability and performance for data transmission over voice-grade telephone lines.

The R24LL is ideal for data transmission applications over either 2-wire or 4-wire leased (dedicated) telephone lines or the dial-up telephone network. Bell 201 B/C, CCITT V.26 A/B and V.26 bis A/B compatible, the R24LL modem offers the user flexibility in creating a 2400 bps modem design customized for specific packaging and functional requirements.

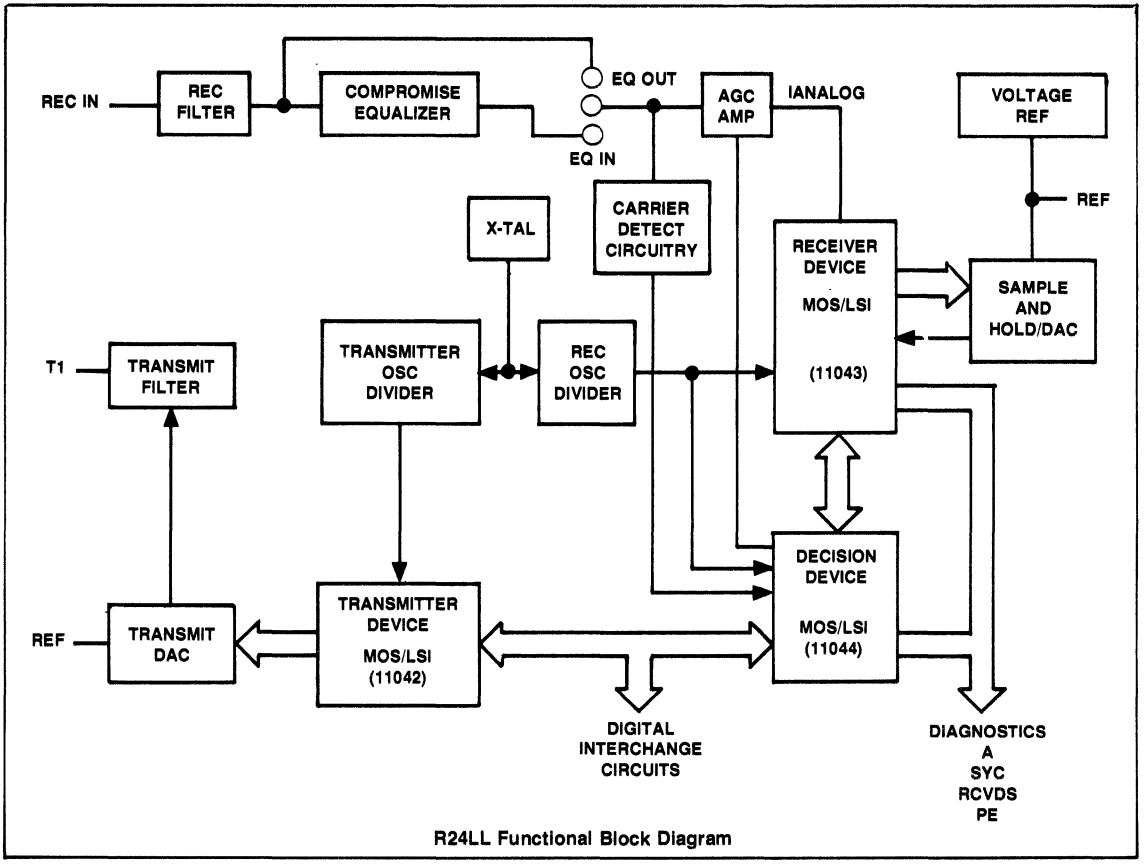
FEATURES

- High Performance—Low Cost
- LSI High Density—Low Power
- Bell 201 B/C, CCITT V.26 A/B Compatibility and V.26 bis A/B Compatibility
- DTE Interface LSTTL/CMOS Compatibility
- External Transmit Data Clock Tracking
- Diagnostic Outputs Available for Eye Pattern Generation and Data Quality Monitoring
- Fixed Compromise Equalizer (Strap Selectable)
- 2400/1200 bps Modes
- Transmitter-Differential Phase Modulation
- Receiver-Coherent Phase Detection
- Operating Modes:
  —Half-Duplex (2-wire)
  —Full-Duplex (4-wire)
- Outstanding Performance Over Unconditioned Lines
- V.27 Scrambler/Descrambler Compatibility
- Answer-Back Tone Generation
- Clear-to-Send Delay Options
- NSYNC Option for Rapid Resynchronization in Multi-Point Applications
- Small Size—Less than 26 sq. in.
- Typical Power Consumption—3 watts
- Power Requirements, +5 Vdc and ± 12 Vdc



Document No. 29200N05

Data Sheet Order No. MD05
Rev. 1, March 1983



R24LL Functional Block Diagram

FUNCTIONAL SPECIFICATIONS

Transmitter Carrier Frequency—1800 Hz ± 0.01%

Echo Suppression and Answering Tone Frequencies—2100 Hz ± 0.01% or 2025 Hz ± 0.01%

Received Signal Frequency Tolerance—The receiver can adapt to received frequency errors up to ± 10 Hz with less than a 0.5 dB degradation in bit error rate.

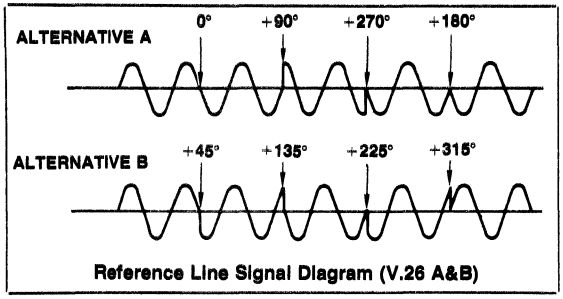
Data Signaling and Modulation Rate—The normal signaling rate is 1200 baud ± 0.01% and a data rate of 2400 bps ± 0.01%. The fallback signaling rate is 1200 baud ± 0.01% and a data rate of 1200 bps ± 0.01%.

Transmitted Data Spectrum—The transmitted spectrum's bandwidth extends from 800 Hz to 2800 Hz. Phase distortion characteristics fall within the limits specified in CCITT Recommendation V.26 bis. The out-of-band signal power limitations meet those specified by Part 68 of Tariff 261 of the FCC's regulations and typically exceed the requirements of international regulatory bodies as well.

Data Encoding (DPSK)—At 2400 bps, differential 4-phase modulation is employed. The data stream to be transmitted divides into pairs of consecutive bits (dibits). Each dibit is encoded as a phase change relative to the phase of the immediately preceding signal element. Two alternative arrangements of coding are possible (in accordance with CCITT Recommendations V.26 and V.26 bis) as shown in the following chart.

Data Encoding

2400 BPS		
	Phase Change	
Dibit	V.26A	V.26B/Bell 201
00	0°	+45°
01	+90°	+135°
11	+180°	+225°
10	+270°	+315°



Reference Line Signal Diagram (V.26 A&B)

At 1200 bps, differential 2-phase modulation is employed. Each bit to be transmitted is encoded as a phase change relative to the phase of the immediately preceding signal element. The encoding is in accordance with CCITT Recommendation V.26 bis as shown in the following chart.

Data Encoding

1200 BPS	
Bit	**Phase Change**
0	+90°
1	+270°

Turn On Sequences—The transmitter of the R24LL can generate a total of 13 selectable turn-on sequences, as shown in the following chart.

Turn Off Sequence—When the transmitter has been sending data and "Request-to-Send" is turned off, any remaining data bit information transmits within 6 milliseconds.

Response Times of Clear-to-Send—The selected configuration of the R24LL and its associated turn-on sequence determine the Clear-to-Send response times, as shown in the following chart.

Scrambler/Descrambler—The R24LL incorporates a self-synchronizing scrambler/descrambler enabled by a discrete digital input.

Carrier Detection—The R24LL contains a received line signal detector. This detector indicates the presence of energy at the receiver input above a certain threshold for a minimum amount of time.

Carrier Detect Thresholds

Received Level	Carrier Detect
Greater than −43 dBm	On (line signal present)
Less than −48 dBm	Off (line signal not present)

Carrier Detect Response Time

Carrier Detect Transition	Response Time
Off-to-On	14 ± 1 ms
On-to-Off	8 ± 3 ms

Turn-On Sequences

Type of Line Signal	Segment 1	Segment 2	Total of Segments 1, 2	Comments
Turn-On Sequence Number	Continuous Unscrambled Ones	Continuous Scrambled[1] Ones	Nominal Total Turn On Sequence Time[2]	
1	0 ms	0 ms	0 ms	
2	6.67 ms	0 ms	6.67 ms	
3	8.33 ms	0 ms	8.33 ms	
4	30 ms	0 ms	30 ms	V.26
5	8.33 ms	21.67 ms	30 ms	(scrambler inserted)
6	90 ms	0 ms	90 ms	V.26, V.26 bis
7	8.33 ms	81.67 ms	90 ms	(scrambler inserted)
8	148.3 ms	0 ms	148.3 ms	
9	8.33 ms	140 ms	148.3 ms	(scrambler inserted)
10	220 ms	0 ms	220 ms	V.26 bis
11	8.33 ms	211.7 ms	220 ms	(scrambler inserted)
12	800 ms	0 ms	800 ms	V.26 bis
13	8.33 ms	791.7 ms	800 ms	(scrambler inserted)

Notes:

1. See paragraph titled Scrambler/Descrambler for a description of scrambler/descrambler facility.
2. For those turn-on sequences in which the scrambler is inserted, the transmitted line signal corresponds to a continuous "one", unscrambled, for 8.33 ms-ten baud (symbol) intervals, followed by the transmission of a continuous "one", scrambled, for the remainder of the turn-on sequence.

Clear-To-Send Response Times

Turn-On Sequence Number	Clear-To-Send Response Times*		Comments
	Off-to-On	On-to-Off	
1	0 ms	0 ms	
2	6.67 ms	0 ms	switched carrier 4-wire (BELL 201)
3	8.33 ms	0 ms	switched carrier 4-wire
4	30 ms	0 ms	CCITT 4-wire
5	30 ms	0 ms	CCITT 4-wire with scrambler
6	90 ms	0 ms	CCITT 2-wire
7	90 ms	0 ms	CCITT 2-wire with scrambler
8	143 3 ms	0 ms	switched carrier 2-wire
9	143.3 ms	0 ms	switched carrier 2-wire with scrambler
10	220 ms	0 ms	CCITT 2-wire echo protection
11	220 ms	0 ms	switched 2-wire echo protection with scrambler
12	800 ms	0 ms	CCITT 2-wire auto call
13	800 ms	0 ms	CCITT 2-wire auto call with scrambler

Note:

*The tolerance on each Off-to-On and On-to-Off response time is (+.9, −.1) ms.

Clamping Options—The following clamps are provided with the R24LL:

1. *Received Data.* The Received Data output is clamped to a mark when Carrier Detect is off. This action prevents disturbances on the line from getting through the receiver circuit to the data output.

2. *Carrier Detect Clamp.* The Carrier Detect output is clamped off (squelched) when Request-to-Send is on. An option extends this clamp for 148 milliseconds beyond transitioning-off, thus providing echo protection.

3. *Receive Clock Clamp.* The Receive Clock output is clamped off when Carrier Detect is off. This action prevents any disturbances from propagating through the receiver circuit to the receive clock output.

Equalizer—The R24LL contains a fixed compromise delay equalizer which improves performance over the domestic switched network. The equalizer may optionally be positioned in the receiver or removed entirely by means of a jumper plug. It has a nominally flat 0.0 dB amplitude response.

Test Pattern Generation—The scrambler/descrambler function can be used to implement a 127-bit test pattern feature. For example, a constant mark input could be scrambled and transmitted as a pseudo-random signal to be descrambled at the receiver back to the constant mark. A transmission error would be represented as a space for the duration of an incorrect bit.

Receive Level—The R24LL receives line signals from 0 to −43 dBm.

Transmit Timing—The R24LL generates a Transmit Clock with the following characteristics: Frequency—2400 Hz ± 0.01% (1200 Hz ± 0.01% in fall back mode), duty cycle—50 ± 1%. The R24LL can also optionally track an External Transmit Clock supplied by the user. Both have similar characteristics.

Receive Timing—The R24LL provides a data derived Receive Clock output in the form of a nominal squarewave (50 ± 1% duty cycle). The timing recovery function can track a ± 0.01% frequency error in the associated transmit timing source.

Secondary Channel—The R24LL provides the user sufficient flexibility to add an external secondary channel if desired. (A secondary channel is a data transmission channel having a lower signalling rate and occupying a different portion of the telephone line bandwidth than the primary channel. The primary and secondary channels share the same transmission facility, the telephone line.) Additional receive filtering to allow simultaneous operation of the secondary channel must be provided external to the R24LL.

Transmit Level—The transmitted output line signal level of the modem is −1.0 dBm ± 1.0 dBm when the transmitter output is terminated with a 600 ohm resistor in series. This applies to all possible transmitted data patterns both at 2400 bps and 1200 bps, as well as to answering tone generation.

Answering Tone Generation—The R24LL can generate an answering tone at 2100 Hz ± 0.01% or 2025 Hz ± 0.01% (selectable) for 3.4 ± 0.2 seconds under the control of an input logic signal (CAUTO). The R24LL also provides a digital output (TONA) indicating the conclusion of answering tone generation.

New Sync—Pulsing the New Sync (NSYNC) digital input forces Carrier Detect Off and causes the R24LL to resynchronize rapidly on sequences of incoming messages. This feature is necessary in some polling applications because the receiver maintains the timing information of the previous message for some time after it has ended—this may interfere with resynchronization on receipt of the next message from a different remote transmitter.

Fast Energy Detector—A received line signal detector, the fast energy detector's output (RLSD) has the same threshold and hysteresis characteristics as the Carrier Detect. For RLSD the maximum turn-on time is 1.6 ms and the maximum turn-off time is 6.6 ms (both times for Equalizer not inserted). Furthermore, the RLSD output will respond to transient line conditions (no momentary dropout or momentary-on glitch protection).

Baud Clocks—Symbol or baud timing is available for both the transmitter and receiver functions. These signals have characteristics similar to the data clocks' except that their frequency is equal to the signalling rate (1200 Hz ± 0.01%). Transitions on Transmitter Baud Clock and Receiver Baud Clock coincide with Off-to-On transitions of Transmit Clock and Receive Clock, respectively. For 2400 bps operation both baud clocks are low for the first data bit in a baud and high for the second data bit.

Analog Loopback—The R24LL provides the flexibility to implement a variety of analog loopback schemes using a minimum amount of external circuitry.

Eye Pattern/Data Quality Detector—The R24LL outputs digital signals (RCVDS, SYC, A) which the user can decode to generate a quadrature eye pattern. The eye pattern is a visual (oscilloscope) display showing the received signal as groupings of dots in the baseband signal plane. It is useful as an incoming modem test and product evaluation tool and as an indication of a line condition in actual operation (useful for some network control applications).

The modem also outputs digital signals (PE, SYC, A) which the user can decode to generate a data signal quality detector. This indicates if a reasonable probability of errors is received on the data channel.

CONFIGURATIONS

The R24LL modem provides the user with a wide range of modem functional configurations. Some of the possibilities are described below.

Half-Duplex (2-Wire)—In a half-duplex application, the user needs both transmit and receive capabilities (although not simultaneously) on a 2-wire connection.

If a hybrid (4-wire → 2-wire) transformer is not employed as a line interface device, REC IN would be strapped to T1 through an external resistor, the user perhaps selecting this resistor to produce a specific output impedance or to compensate for losses in any line interface circuitry.

Digital interface connections. In a typical application, the user controls basic modem operation through the digital signals T103, T105, T106, T114, T104, T115, T109, and perhaps RBCK, T113, or TBC. (T113 is used if transmit timing is to be locked to the customer's clock; TBC may be employed to minimize certain timing delays and is useful in some multiplexing operations). A number of digital inputs can either be fixed (tied directly and permanently to the +5V supply [high] or to signal ground or the −12V supply [low] in accordance with the specific requirements) or, if the user desires programmable flexibility, these signals can be interfaced with his equipment. Signals of this type include T111, V26A, 1, S8GR, K, Y, TC06, 800MS, E, T2W/4W, CP04, CP15, RW/4W, TH09, FSYC, TC09, and PBS. If answerback or echo suppression tone generation capability is required, the input CAUTO (which should be strapped low if not used) and the output TONA are available. Implementation of the New Sync function requires any new sync pulses to be inputted to NSYNC. The outputs SYC, RCVDS, DCP, A, and PE can be used to generate eye pattern and phase error diagnostic information.

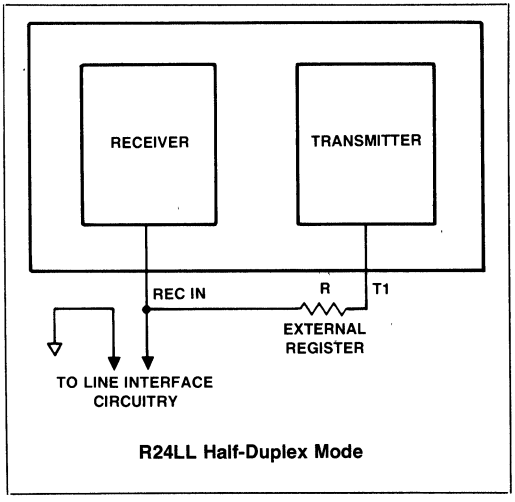
Analog interface connections. The GAIN-G1-G2 jumper (for threshold set selection) should be in the proper location as described in the table at the top of page 9. Note that input impedance at REC IN is a resistive 15.8K ohms. If a 600 ohm receiver input impedance is desired, an external resistor to signal ground must be added. Take care when routing to REC IN (for low level receive signal) from any telephone interface circuitry. Also note that it is possible to insert the equalizer into the receiver or not to insert it by use of the jumper on the board. Implementation of a local analog loopback scheme could be achieved in many ways. If the line interface connection as shown in the diagram below is employed, the user can create a local analog loopback simply by deactivating squelch. To isolate the telephone line during this loopback (no transmitted line signal), additional circuitry must be added.

Full-Duplex—In a full-duplex application, the user needs both transmit and receive capabilities simultaneously. A 4-wire line connection is required.

The only differences with half-duplex are that REC IN is no longer connected to T1 (the transmitter and receiver have independent transmission paths) and the squelch function would be deactivated (except during New Sync) by use of the input T2W/4W.

Digital interface connection is the same as for the half-duplex.

Analog interface connections. With the exception of the 4-wire line interface, analog interface connections are the same as half-duplex. Implementation of a variety of local or remote analog or digital loopback schemes requires the addition of a minimal amount of external circuitry.



R24LL Half-Duplex Mode

INTERFACE CRITERIA

The R24LL interface signals are classified as digital interchange signals and analog signals. The signals interface to the modem user through the board edge connector.

Digital Interchange Circuits—The characteristics of the R24LL digital inputs and outputs are given in the following charts:

Digital Input Characteristics

Input Logic State	Allowed Input Voltage Levels
Low	−12V (V_{DD}) to 0.8V sinking <10 μA
High	+4.0V (V_{SS} − 1V) to +5.0V (V_{SS}) sourcing <10 μA
The digital inputs are directly CMOS compatible. The capacitive loading on each input is 25 pF (maximum).	

Digital Output Characteristics

Output Logic State	Allowed Output Voltage Levels
Low	0.0V to 0.4V (−0.4V to +0.4V for RLSD) sinking 0.36 mA
High	+4.0V (V_{SS} − 1V) to +5.0V (V_{SS}) sourcing 100 μA
The digital outputs are directly CMOS or low-power Schottky TTL compatible.	

Digital Interchange Circuits

Term	Pin Number	Description
TONA	P1-A5	Output indicating completion of answering tone.
800MS	P1-A6	Input affecting Clear-to-Send response time.
TC06	P1-A7	Input affecting Clear-to-Send response time.
K	P1-A8	Input affecting Ready-for-Sending response time.
X	P1-A9	Input affecting T109 Squelch.
CAUTO	P1-A10	Input initiation transmission of answering tone.
New Sync (NSYNC)	P1-A13	Input affecting T109 Squelch.
CLAMP	P1-A15	Input forcing squelch of T109.
Fast Energy Detector (RLSD)	P1-A17	Input generating T109.
Fast Sync (RSYC)	P1-A18	Input determining whether fast sync feature (fast resynchronization upon recovery of received line signal following momentary dropout) is enabled.
S8GR	P1-A19	Input determining whether the modulo 8 pattern guard will be incorporated into the scrambler facility.
DCP	P1-A21	Digital output enabling user to generate eye pattern and phase error diagnostic information.
R2W/4W	P1-A22	Input affecting state of THRH output.
Receiver Baud Clock (RBCK)	P1-A23	For 2400 bps operation.
PBS	P1-A24	Input determining T109 On-to-Off response time.
TH09	P1-A25	Input affecting state of THRH output.
Transmitted Data (T103)	P1-A29	Input for digital data to be transmitted.
Clear-to-Send or Ready-for-Sending (T106)	P1-A30	Output indicating readiness to accept data for transmission.
Data Signalling Rate Selector (T111)	P1-A32	Input determining whether transmitted data rate is 2400 bps or 1200 bps.
Receive Clock (T115)	P1-A33	Output providing received signal element timing information.
E	P1-B6	Inputs affecting Clear-to-Send response time and T109 Squelch.
T2W/4W	P1-B7	
Y	P1-B8	Input affecting Ready-for-Sending response time and answering tone frequency.
Transmitter Baud Clock (TBC)	P1-B10	Output baud clock (1200 Hz).
A	P1-B11	Digital output enabling user to generate eye pattern and phase error diagnostic information.
I	P1-B15	Input determining whether scrambler is to be inserted.
THRH	P1-B18	Output used in conjunction with carrier detect circuitry to implement T109 threshold set select function.
V26A/B	P1-B19	Input selecting dibit encoding at 2400 bps operation as per V.26 Alternate A or V.26 Alternate B.
CP15	P1-B20	Input selecting optional clamping of Receive Clock (T115).
RCVDS	P1-B21	Digital outputs enabling user to generate eye pattern and phase error diagnostic information.
SYC	P1-B22	
PE	P1-B23	
TC09	P1-B24	Input determining T109 Off-to-On response time.
CP04	P1-B25	Input determining T104 damping.
External Transmit Clock (T113)	P1-B29	Input providing modem with transmitted signal element timing information.
Request-to-Send (T105)	P1-B30	Input to transmitter.
Received Data (T104)	P1-B31	Digital data output from modem receiver.
Transmit Clock (T114)	P1-B33	Output providing user with transmitted signal element timing information.
Carrier Detect (T109)	P1-B24	Output indicating presence of signal energy on receiver line.

Note:

The following P1 connector pin locations should be left open and unconnected: A4, A11, A12, A14, A16, A20, A35, B1, B12, B13, B14, B17, B32, and B35.

7

Data Structure

Input		Data Structure
Data Signalling Rate Selector (P1-A32)	V26 A/B (P1-B19)	
Low	Low	2400 bps Alternate A
Low	High	2400 bps V.26 Alternate B (Bell 201C)
High	Don't Care	1200 bps

Tone Generation

Inputs		Outputs	
CAUTO (P1-A10)	Y (P1-B8)	TONA (P1-A5)	Transmitted Signal
Low	Don't Care	High	Normal Operation
High	High	High	2100 Hz Answering Tone
High	Low	High	2025 Hz Answering Tone
High	Don't Care	Low	Normal Operation

Selection of Clear-To-Send Response Times

	Inputs							Clear-To-Send Response Times (ms)	
Turn-On Sequence	Y (P1-B8)	800MS (P1-A6)	K (P1-A8)	TC06 (P1-A7)	T2W/4W (P1-B7)	I (P1-B15)	E (P1-B6)	Off-to-On	On-to-Off
1	Low	High	Don't Care	Don't Care	High	Low	Don't Care	6.67	0
2	High	High	Low	High	High	Low	Don't Care	8.33	0
3	High	High	Low	Low	High	Low	Don't Care	30	0
4	High	High	Low	Don't Care	High	High	Don't Care	30	0
5	High	High	Don't Care	High	Low	Low	Low	90	0
5	High	High	High	High	High	Low	Don't Care	90	0
6	High	High	Don't Care	High	Low	High	Low	90	0
6	High	High	High	High	High	High	Don't Care	90	0
7	Low	High	Don't Care	Don't Care	Low	Low	Don't Care	148.3	0
8	Low	High	Don't Care	Don't Care	Don't Care	High	Don't Care	148.3	0
9	High	High	High	Low	Don't Care	Low	Don't Care	220	0
9	High	High	Don't Care	Don't Care	Low	Low	High	220	0
9	High	High	Don't Care	Low	Low	Low	Don't Care	220	0
10	High	High	High	Low	Don't Care	High	Don't Care	220	0
10	High	High	Don't Care	Don't Care	Low	High	High	220	0
10	High	High	Don't Care	Low	Low	High	Don't Care	220	0
11	High	Low	Don't Care	Don't Care	Don't Care	Low	Don't Care	220	0
12	High	Low	Don't Care	Don't Care	Don't Care	High	Don't Care	800	0

Note: The tolerance on each Off-to-On and On-to-Off response time is (+0.9, −0.1 ms).

Carrier Detect Squelch

Inputs					Squelch Status
X (P1-A9)	T2W/4W (P1-B7)	E (P1-B6)	T105 (P1-B30)	NSYNC (P1-A13)	
Don't Care	Don't Care	Don't Care	Don't Care	Low	Squelch
Don't Care	High	Don't Care	Don't Care	High	No Squelch
Low	Low	Don't Care	Don't Care	High	No Squelch
High	Low	Don't Care	High	High	Squelch
High	Low	High	High→Low	High	Extended Squelch
High	Low	Low	High→Low	High	No Extended Squelch

Notes:

"Squelch" means that Carrier Detect (T109) is clamped off regardless of the level of received line signal. During squelch, CLAMP (T-13) is a low impedance to ground. For normal operation (no squelch) CLAMP (T-13) is in a high impedance ("open drain") state.

When "extended squelch" is enabled, squelch occurs both when Request-to-Send (T105) is On (High) and for 148.3 ms (+0.9, −0.1 ms) following the On-to-Off (High to Low) transition of T105.

Carrier Detect Threshold Selection

THRH	Gain Strap	Selected Threshold Set
High Impedance	G1	−43 dBm, −48 dBm
High Impedance	G2	−33 dBm, −38 dBm
Low Impedance to ground	G1 or G2	−26 dBm, −31 dBm
Gain must be shorted to either G1 or G2.		

THRH Operation

Input		THRH
TH09	R2W/4W	
Low	Low	High Impedance
High	Low	High Impedance
Low	High	High Impedance
High	High	Low Impedance
THRH is an open-drain driver representing either a low impedance to ground (<500 ohms) or a very high impedance state.		

Scrambler/Descrambler

Input		Scrambler/Descrambler Configuration
I (P1-B15)	S8QR (P1-A19)	
Low	Don't Care	No Scrambler
High	Low	Scrambler V.27 bis, ter (modulo 8 pattern guard)
High	High	(no modulo 8 pattern guard)

Analog Interface Circuits—The analog interface circuits of the R24LL defined in the following chart provide the power, the switched network connections, and a means for the user to monitor the incoming line signals.

Analog Interface Circuits

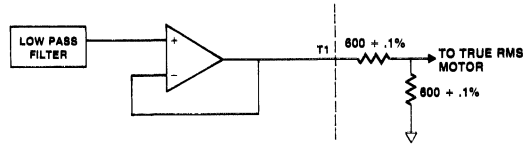
Term	Pin Number	Description
+12V	P1-B5, B9	+12V Power Supply
−12V	P1-A1	−12V Power Supply
+5V	P1-A2, B2	+5V Power Supply
COMMON	P1-A3, A31, B3	Ground (signal and power return)
T1	P1-A34	T1 is the low impedance transmitter analog output (line signal). The T1 allows the user the flexibility needed to customize his output impedance (to compensate for transformer losses, for instance).
SECONDARY IN	P1-B4	Secondary channel input from the DTE.
REC IN	P1-B36	Receive filter input. Input impedance is a resistive 15.8 K ohms ± 1%.

Audio Interface—The audio interface includes the R24LL's interface with the transmission network.

The receiver and transmitter line interfaces are single-ended (non-transformer coupled) signals with the following characteristics:

Transmitter Voice Frequency Output T1

1. Output Impedance: Impedance of Op-Amp
2. Maximum Output Level: ≤0.0 dBm as measured per the following diagram using a true RMS meter.



Receiver Voice Frequency Input REC IN

1. Input Impedance: 15.8K ohms ± 1% resistive
2. Maximum Input Level: ≤0.0 dBm

The output level at the R24LL line interface is less than −60 dBm in the frequency band of 1 Hz to 12 Hz when the modem is not transmitting. A period of 100 milliseconds is required for the line interfaces to stablize following power turn-on.

Low impedance voice frequency output T1 satisfies applications interfacing with lossy transformers or hybrids. The characteristics of T1 output are:

a. Output Impedance: Essentially zero ohms when loaded to ground with greater than 400 ohms (resistive). This is a direct output from an operational amplifier.

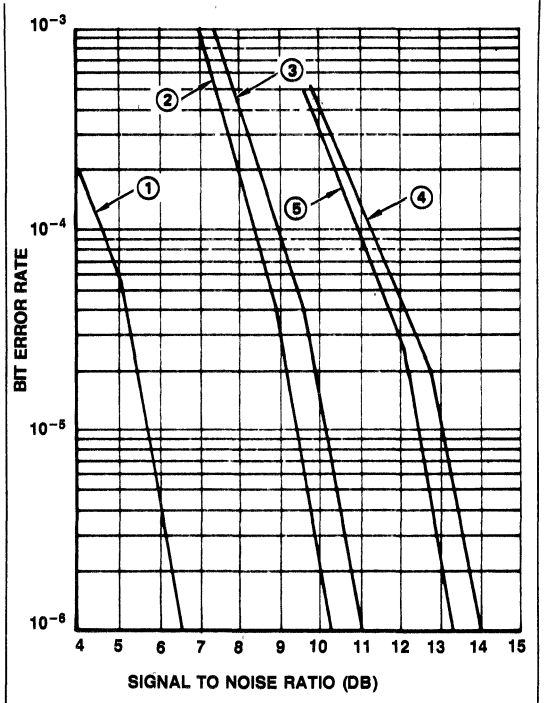
b. Minimum Load: ≥400 ohms (resistive) as measured between T1 and signal ground.

PERFORMANCE DATA

The R24LL is a high performance synchronous 2400 bps DPSK modem. It utilizes a coherent demodulation technique to achieve reliable operation over the switched network or unconditioned lines.

Timing Jitter—The maximum steady state timing jitter of Received Clock with respect to Transmit Clock is less than 10% p-p for an input signal-to-noise ratio of 12 dB.

Bit Error Rate—The following graph represents typical R24LL performance.

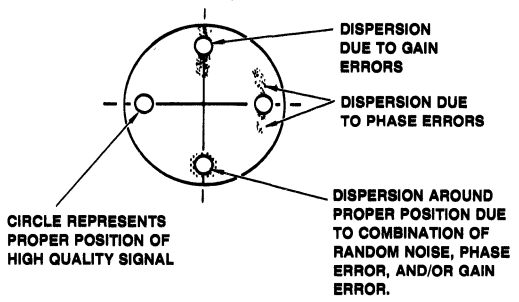


1. 1200 BPS, BACK-TO-BACK, SCRAMBLER, NO EQUALIZER
2. 2400 BPS, V.26A OR B, BACK-TO-BACK, SCRAMBLER NO EQUALIZER
3. 2400 BPS, V.26A OR B, 15°–150 HZ PHASE JITTER, NO SCRAMBLER, NO EQUALIZER
4. 2400 BPS, V.26A OR B, 30°–120 HZ PHASE JITTER, NO SCRAMBLER, NO EQUALIZER
5. 2400 BPS, V.26A OR B, 3002 UNCONDITIONED LINE, NO SCRAMBLER, EQUALIZER

Typical Bit Error Rate Performance

Phase Error—Phase error can be measured with the modem's output signals PE, SYC, and A. With an external test circuit, a numerical value can be derived to indicate the quality of received data and then directly correlated to bit error rate performance. The required test circuit can be implemented with discrete circuitry or in software within a microcomputer.

Eye Pattern—By using the modem's digital output signals RCVDS, SYC, and A along with an added test circuit, the user can generate an oscilloscope quadrature eye pattern. This pattern displays the received signal as a group of dots in the baseband signal plane: it is a graphic representation of modem performance.



Typical Eye Pattern: 4 Phase-2400 BPS-1200 Baud (V26A)

Phase error and eye pattern can be extremely useful for modem acceptance testing, product evaluation, and observation of line signal quality under actual operation.

RECOMMENDED MATING CONNECTORS

The R24LL connector mating contacts are *not* gold covered; therefore, a high quality gas-tight card edge connector should always be used to maintain reliable operation. Rockwell recommends the following in order of preference:

1. Burndy GTBH Series
2. Continental 6100-200 Series
3. Elco 00-6307 Series

POWER REQUIREMENTS

Voltage	Ripple	Maximum Current
+5 VDC ± 5%	100 mV p-p	102 mA
+12 VDC ± 5%	50 mV p-p	64 mA
−12 VDC ± 5%	50 mV p-p	142 mA

ENVIRONMENTAL SPECIFICATIONS

Operating Temperature: 0°C to 60°C
Storage Temperature: −40°C to +80°C
Relative Humidity: to 90% (non-condensing) or a wet bulb temperature up to 35°C, whichever is less.
Altitude: −200 to 10,000 feet (−61 meters to 3,049 meters)

Rockwell

R24
2400 BPS INTEGRAL MODEM

INTRODUCTION

The Rockwell R24 is a high performance synchronous serial 2400 bps DPSK modem. Utilizing extensive MOS/LSI technology, the R24 is implemented in three modular building blocks. It is innovatively designed to enable its economic integration by system designers in a broad range of communication, computer, and control equipment.

Having Bell 201 B/C and CCITT V.26 compatibility, the modular R24 offers the user sufficient flexibility to customize a 2400 bps modem to his specific packaging and functional requirements. With a minimum amount of interface circuitry, the modem can be configured for operation on leased lines or on the general switched network.

MODULE VERSATILITY

The versatility of the R24 design is achieved by dividing the modem's functions into three modules:

Transmitter — Module T
Receiver — Modules R1 and R2

Each module can be plugged into standard connectors or can be wave soldered on one or more printed circuit boards. The pin spacing is on 100 mil centers. Modem modules are functionally independent.

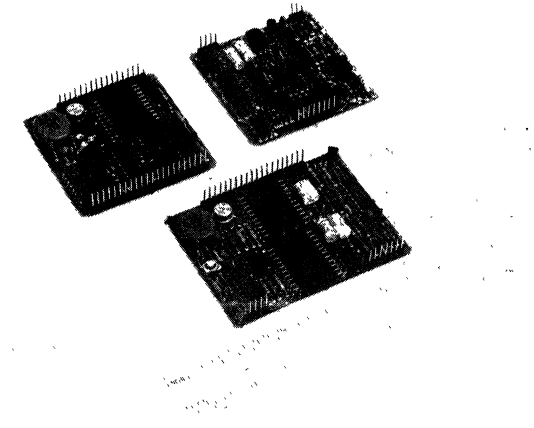
MODEM OPERATION MODES

In general, the modules can be configured to operate in the following modes:

Simplex — Transmit only:	Only the transmitter module (T) is used.
Simplex — Receive only:	R1 and R2 modules are used to implement a complete receiver function.
Half Duplex (2-Wire):	Requires both transmit and receive functions (although not simultaneously), therefore, all three modules are used.
Full Duplex (4-Wire):	Requires both transmit and receive functions simultaneously, again all three modules are used.

FEATURES:

- LSI high density; low power
- 2400/1200 bps modes
- Transmitter-Differential phase shift keying
- Receiver-Coherent phase detection
- Bell 201 B/C, CCITT V.26 compatible
- CCITT A/B encoding options
- Operating modes:
  - Half duplex (2 wire)
  - Full duplex (4 wire)
  - Simplex (Transmit or Receive only)
- Outstanding performance over unconditioned lines
- LSTTL/CMOS compatible digital interface
- Fixed compromise equalizer
- V.27 compatible scrambler/descrambler
- Answer-back tone generation
- Clear-to-send delay options
- New sync option provides rapid resynchronization
- Typical power consumption 2 watts
- Total module area 25 sq. in.
- R24 Modem Evaluation Board facilitates evaluation and design-in tasks.



R24 Integral Modem

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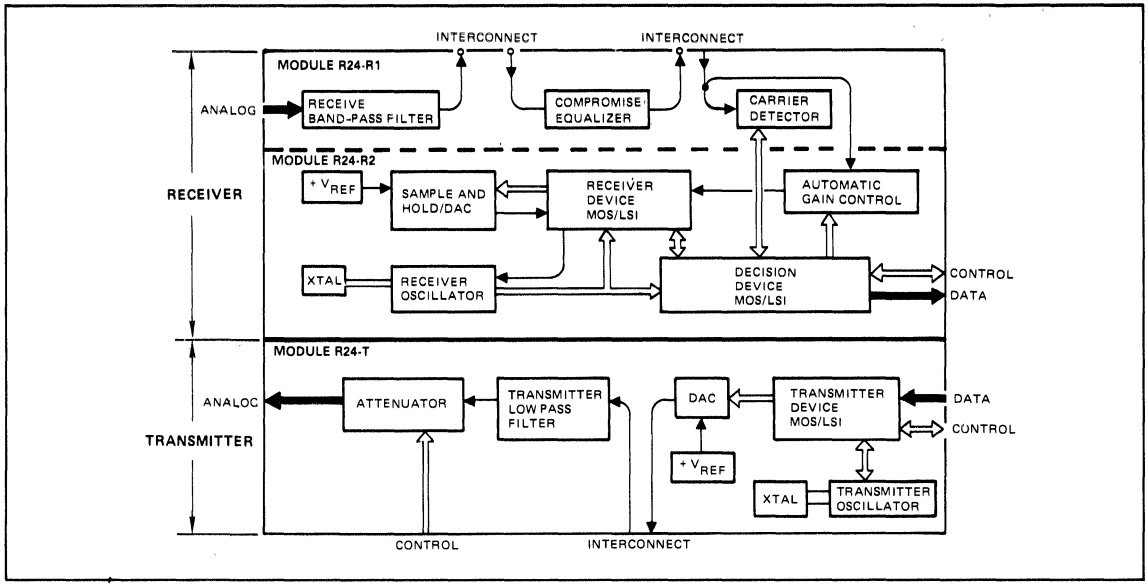


R24 Functional Diagram

TECHNICAL DESCRIPTION

Transmitter carrier frequency — 1800 Hz ±0.01%

Echo suppression and answer tone frequencies — 2100 Hz ±0.01% or 2025 Hz ±0.01%

Received signal frequency tolerance — The receiver can adapt to received frequency errors up to ±10 Hz with less than a 0.5 dB degradation in bit error rate.

Data signaling and modulation rate:

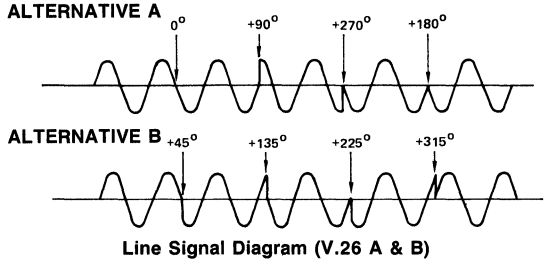
1) Normal: Signaling Rate — 1200 baud ±0.01%.
   Data Rate — 2400 bps ±0.01%.
2) Fallback: Signaling Rate — 1200 baud ±0.01%.
   Data Rate — 1200 bps ±0.01%.

Transmitted Data Spectrum — The transmitted spectrum's bandwidth extends from 800 Hz to 2800 Hz. Phase distortion characteristics are within the limits specified in CCITT Recommendation V.26 bis. The out of band signal power limitations meet those specified by Part 68 or Tariff 261 of the FCC's regulations, and typically exceed the requirements of international regulatory bodies as well.

Data Encoding (DPSK) — At 2400 bps, differential four-phase modulation is used. The data stream is transmitted in pairs of consecutive bits (dibits). Each dibit is encoded as a phase change relative to the phase of the preceding signal element.

The R24 implements the phase A and B recommendations of CCITT V.26. The modulation coding in Bell 201 modems is the same as V.26B. Definition of these coding arrangements is shown in the following table:

2400 BPS		
DIBIT	PHASE CHANGE	
	V.26A	V.26B/Bell 201
0 0	0°	+45°
0 1	+90°	+135°
1 1	+180°	+225°
1 0	+270°	+315°



Line Signal Diagram (V.26 A & B)

At 1200 bps, differential two-phase modulation is used. Each bit is transmitted at a relative phase change to preceding signal element in acordance with CCITT V.26 bis.

1200 BPS	
BIT	PHASE CHANGE
0	+90°
1	+270°

Turn On Sequences — A total of twelve selectable turn on sequences can be generated by the transmitter module.

Turn Off Sequence — When the transmitter has been sending data and "Request to Send" is turned off, any remaining data bit information is transmitted within 6 milliseconds.

Ready for Sending (T106) Response Times — These response times are determined by the modem configuration selected and its associated turn on sequence.

Turn On Sequence Number	Ready for Sending Response Time	Configuration and Carrier Type
1	6 67 msec	Switched Carrier — 4-Wire (Bell 201)
2	8 33 msec	Switched Carrier — 4-Wire
3	30 msec	CCITT — 4-Wire
4	30 msec	CCITT — 4-Wire with Scrambler
5	90 msec	CCITT — 2-Wire
6	90 msec	CCITT — 2-Wire with Scrambler
7	148 3 msec	Switched Carrier — 2-Wire
8	148 3 msec	Switched Carrier — 2-Wire with Scrambler
9	220 msec	CCITT — 2-Wire Echo Protection
10	220 msec	Switched 2-Wire Echo Protection with Scrambler
11	800 msec	CCITT — 2-Wire Auto Call
12	800 msec	CCITT — 2-Wire Auto Call with Scrambler
Response Time tolerance (+ 0 9, -0.1) msec		

Scrambler/Descrambler — As a selectable option, the scrambler/descrambler may be inserted into the transmitter/receiver path. The purpose of this scrambler is to ensure that the line signal will evenly span the allocated bandwidth. This minimizes pattern sensitivity problems arising from simple fixed and periodic data sequences. The scrambler is V.27 or V.27 bis/ter compatible.

Carrier Detect (T109) — The modem receiver incorporates a line signal energy detector whose output responds to three selectable threshold levels.

Set 1 (V.26 bis, switched network)	Greater than -43 dBm Less than -48 dBm	= ON = OFF
Set 2 (V.26 bis, switched network)	Greater than -33 dBm Less than -38 dBm	= ON = OFF
Set 3 (V.26, leased line)	Greater than -26 dBm Less than -31 dBm	= ON = OFF

Selectable T109 Response Times — This time is defined as the interval between the sudden connection or removal of the received line signal to the modems receive filter, and the subsequent transition of Carrier Detect (T109) from one state to the other.

Carrier Detect Transition	Response Time	
OFF to ON (connection)	6 ±1 ms 14 ±1 ms	Selectable
ON to OFF (removal)	8 ±3 ms 22 ±3 ms	Selectable

Receive Level — The modem receives line signals from 0 to -43 dBm.

Transmit Timing — The modem generates a Transmit Clock (T114) having the following characteristics: Frequency — 2400 Hz ±0.1% (1200 Hz ±.01% in fallback mode), duty cycle — 50 ±1%. The modem is also optionally capable of tracking an External Transmit Clock (T113) supplied by the modem user. T113 has similar characteristics to T114.

Receive Timing (T115) — The modem provides a data derived "Receive Clock" output in the form of a nominal squarewave (50 ±1% duty cycle). The modem timing recovery function is capable of tracking a ±0.01% frequency error in the associated transmit timing source.

Transmitter Output Levels — This output can be strap controlled in 2 ±0.2 dB steps from -1 dBm ±1 dB to -15 dBm ±1 dB.

Answer Tone Generation — The modem generates a selectable answering tone of 2100 Hz ±0.01% or 2025 Hz ±0.01%. The 2100 Hz tone meets CCITT Recommendations G.161 and V.25, and the 2025 Hz tone meets Bell System requirements for both answering tone and echo suppressor disabling tone.

Equalizer — As a strap option, the modem contains a fixed compromise delay equalizer which can be used to improve performance over unconditioned schedule 3002 lines. This option is normally positioned in the receiver, but it can be repositioned in the transmitter or bypassed entirely. It is designed to compensate for the mean of the range of group delay distortions generally encountered in the United States. Its amplitude response is nominally flat at 0.0 dB.

Test Pattern Generation — The scrambler/descrambler function can be used to implement a 127-bit test pattern feature. For example, a constant mark input could be scrambled and transmitted as a pseudo-random signal to be descrambled at the receiver back to the constant mark. A transmission error would be represented as a space for the duration of an incorrect bit.

Multipoll Synchronization — The "new sync" (NSYNC) digital input can be pulsed to cause rapid resynchronization of the receiver for sequences of incoming messages. This feature is necessary in some polling applications. However, if the user's hardware/software does not support the use of "new sync" (NSYNC), then the optional "fast sync" (FSYNC) can be utilized to enable a fast resynchronization procedure.

Selectable Clamping Options —

1) Received Data (T104) — This output is clamped to a selectable constant (space or mark) when "Carrier Detect" is off, to prevent disturbances on the line from getting through the receiver to the data output.
2) Carrier Detect (T109) Clamp — This output may be clamped OFF (squelched) in a 2-wire applications during the time when "Request to Send" (T105) is on. An additional option extends this clamp for 148 msec beyond T105 transitioning off, providing echo protection.
3) Receive Clock (T115) — This clock output can be clamped OFF when "Carrier Detect" is off, thereby preventing any disturbances from propagating through the receiver to the receive clock output.

SYSTEM DESIGN

The R24 modem modules provide the user with sufficient flexibility to implement a wide range of modem functional configurations. This flexibility is achieved by digital control at the module interfaces. For a given application, such as a lease network V.26 Alternative B modem (Bell 201B), the complexity of the user interface can be significantly reduced by strapping those data interface inputs which do not change. The modem interface can also be under software control.

Figures 1 and 2 show the basic interface connections for the transmitter module (T) and the receiver modules (R1,R2). These diagrams are applicable for any operation mode of the modem-simplex, half-duplex, or full-duplex.

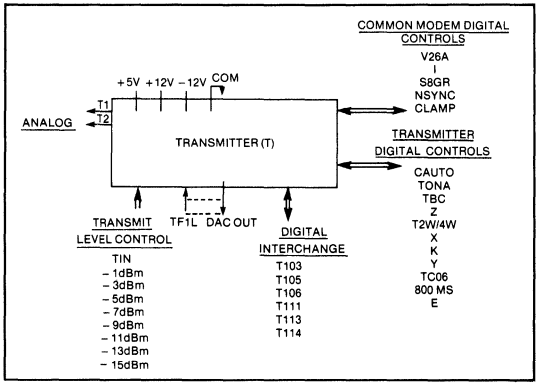


Figure 1. Transmitter Interfaces

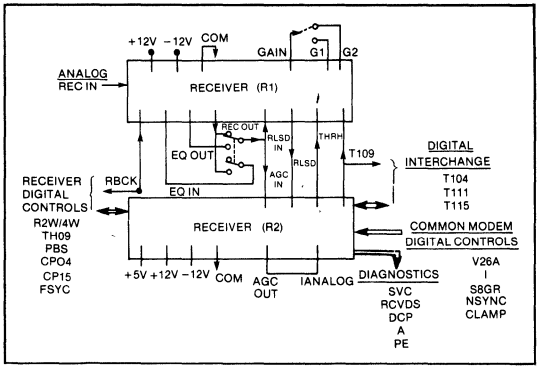


Figure 2. Receiver Interconnection

MODEM OPERATION — HALF OR FULL-DUPLEX

Figure 3 indicates the module interconnections necessary for half-duplex operation. For full-duplex operation, the transmitter/receiver interconnections are similar to the half-duplex case with the exception that "REC IN" is not connected to T2 or T1. In full-duplex operations, the transmission and receiver paths are independent.

As shown, a transformer is sufficient to connect directly to a leased line in the U.S. For the switched network, registered protective circuitry or a data access arrangement (DAA) is generally required. Rockwell offers an FCC registered protective circuitry product to support this application. Requirements for line interface and protective circuitry vary internationally.

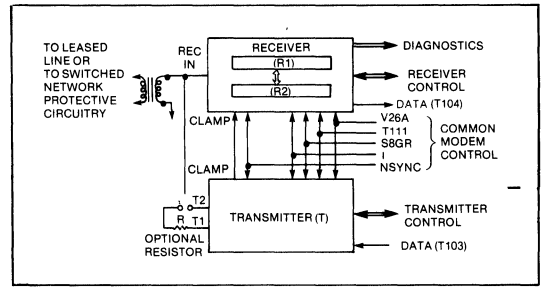
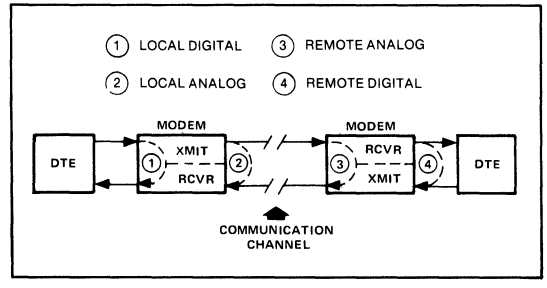


Figure 3. Transmitter-Receiver Interconnection (Half Duplex)

Secondary Channel — The modem modules provide the user with all the interface connections needed to add an external secondary channel if required. This data transmission channel would operate at a lower rate, and in a different portion of the available bandwidth than the primary. Additional external receive filtering would also have to be added to allow simultaneous operation of the primary and secondary channels.

Analog and Digital Loopback — To check out or diagnose the communication link, loopback testing is often performed. A test word is transmitted and "looped" back to the originating DTE. Typical types of loopback tests are:



DTE — Data Terminal Equipment

The modem modules provide the user with all the necessary interfaces connections to implement almost any loopback scheme desired. With a minimum amount of external circuitry, loopback testing can be controlled via a communications adapter/software approach or manually. For local analog, remote analog and remote digital loopback, the V.27 scrambler within the modem can be used to generate a 127-bit word.

INTERFACE DESCRIPTION

STANDARD DIGITAL INTERCHANGE

Term (CCITT V 24 Equivalent)	EIA RS232C Equivalent	Module Interface Input	Module Interface Output	Description
T103	BA	T-9		Transmitted Data
T104	BB		R2-5	Received Data
T105	CA	T-8		Request to Send
T106	CB		T-6	Ready for Sending (Clear to Send)
T109	CF	R1-4	R2-22	Data Channel Received Line Signal Detector (Carrier Detect)
T111	CH	T-12, R2-9		Data Signalling Rate Selector Selects 2400 bps or 1200 bps Mode
T113	DA	T-7		External Transmit Clock (Transmitted Signal Element Timing)
T114	DB		T-10	Transmit Clock (Transmitted Signal Element Timing)
T115	DD		R2-6	Receive Clock (Receive Signal Element Timing)

ANALOG LINE INTERFACES

Term	Module Interface Input	Module Interface Output	Description
REC IN	R1-12		Analog Line Signal Input (Receive Filter Input)
T1		T-1	Low Impedance Transmitter Output
T2		T-2	Standard Transmitter Output 600 ohms Impedance

COMMON MODEM DIGITAL CONTROLS

Term	Module Interface Input	Module Interface Output	Description
V26A	T-16 R2-13		Selects V 26A or V 26B Dibit Encoding
I S8GR	T-15 R2-12 T-17 R2-14		Controls for Scramble Operation
NSYNC	T-14 R2-11		Controls T109 to Force Rapid Resynchronization of the Receiver
CLAMP	R2-10	T-13	Implements Squelch for Carrier Detect (T109)

TRANSMITTER DIGITAL CONTROLS

Term	Module Interface Input	Module Interface Output	Description
CAUTO	T-3		Initiates Answer Tone
TONA		T-5	Indicates Completion of Transmission of Answer Tone
TBC		T-4	Transmitter Baud Clock
Z	T-28		Input Forcing Transmit Clock (T114) to Phase and Frequency Lock to External Transmit Clock (T113)
T2W/4W X K Y TC06 800MS E	T-11 T-24 T-25 T-26 T-27 T-29 T-30		Inputs Affecting Ready for Sending Response Times, Answer Tone Frequency and Carrier Detect (T109) Squelch

TRANSMITTER ANALOG CONTROLS

Term	Module Interface Input	Module Interface Output	Description
DAC OUT		T-22	Output of Digital to Analog Converter
TFIL	T-23		Input to Low Pass Filter DAC OUT is Normally Connected to TFIL Unless Additional Filtering or an Equalizer is to be Inserted
TIN – 1dBm – 3dBm – 5dBm – 7dBm – 9dBm – 11dBm – 13dBm – 15dBm	T-31	 T-39 T-38 T-37 T-36 T-35 T-34 T-33 T-32	These Nine Signals Implement the Transmitter Output Level Attenuator One of the Signals – 1dBm, , – 15dBm is Strapped to TIN to Set the Desired Output Level

RECEIVER DIGITAL CONTROLS

Term	Module Interface Input	Module Interface Output	Description
RBCK	R1-1	R2-25	Receiver Baud Clock
RLSD THRH R2W/4W TH09	R2-24 R1-3 R2-8 R2-18	R1-2 R2-23	Control Signals to Generate Carrier Detect (T109) and Implement T109 Threshold Set Select Function
TC09	R2-15		Determines Carrier Detect (T109) Off-to-On Response
PBS	R2-16		Determines Carrier Detect (T109) On-to-Off Response
CP04	R2-17		Clamps Received Data (T104) to a mark or space when Carrier Detect (T109) is Off
CP15	R2-19		Optional Clamping of Received Clock (T115)
FSYC	R2-20		Fast Sync Optional Fast Resynchronization Procedure

RECEIVER DIGITAL DIAGNOSTICS

Term	Module Interface Input	Module Interface Output	Description
SYC RCVDS DCP A PE		R2-1 R2-2 R2-4 R2-3 R2-7	Digital Outputs which Enable User to Generate Eye Pattern and Phase Error Information

RECEIVER ANALOG CONTROLS

Term	Module Interface Input	Module Interface Output	Description
REC OUT	R1-7		Receive Filter Ouput
EQ IN	R1-8		Equalizer Input
EQ OUT	R1-6		Equalizer Output
RLSD IN	R1-5		Carrier Detect Circuitry Input
AGC IN	R2-21		Automatic Gain Control Circuitry Input
AGC OUT		R2-26	Automatic Gain Control Circuitry Output
GAIN G1 G2	 R1-11 R1-9	R1-10	Optional Carrier Detect (T109) Threshold Selection Controls
IANALOG	R2-27		Sample and Hold Circuitry Input

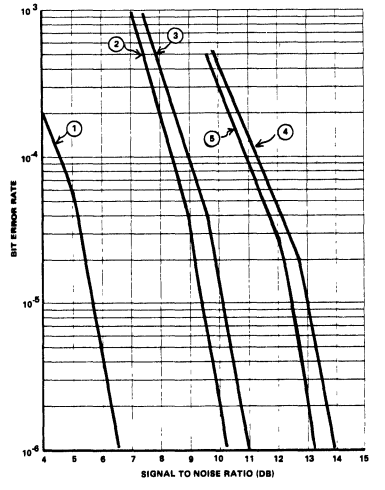
7

MODEM PERFORMANCE

The R24 is a high performance synchronous 2400 bps DPSK modem, utilizing a coherent demodulation technique to achieve reliable operation over the switched network or unconditioned lines. This section contains a quantitative discussion of the R24's typical performance under varying test conditions.

Timing Jitter — The maximum steady state timing jitter of "receive clock" with respect to "transmit clock" is less than 10% p-p for an input signal-to-noise ratio of 12 dB.

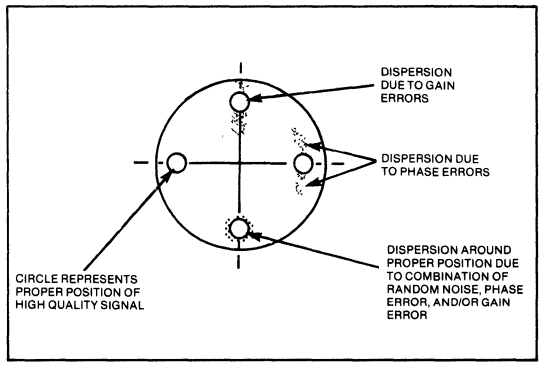
Bit Error Rate — The following graph represents typical R24 performance:



Typical Bit Rate Performance

Phase Error — Phase error can be measured by using the modem's output signals PE, SYC, and A. With an external test circuit, a numerical value can be derived to indicate the quality of received data. This numerical value can be directly correlated to bit error rate performance. The required test circuit can be implemented with discrete circuitry or in software within a microcomputer.

Eye Pattern — By using the modems digital output signals RCVDC, SYC, and A along with an added test circuit, the user can generate an oscilloscope quadrature eye pattern. This pattern displays the received signal as a group of dots in the baseband signal plane; hence, it is a graphic representation of modem performance.



Typical Eye Pattern: 4 Phase-2400 bps-1200 Baud (V26A)

Phase error and eye pattern can be extremely useful for modem acceptance testing, product evaluation, and observation of line signal quality under actual operation.

ELECTRICAL CHARACTERISTICS

POWER REQUIREMENTS

Module	Voltage	Ripple	Maximum Current
T	+5 Vdc ±5% +12 Vdc ±5% -12 Vdc ±5%	100 mV p-p 50 mV p-p 50 mV p-p	38 mA 16 mA 48 mA
R1	+12 Vdc ±5% -12 Vdc ±5%	50 mV p-p 50 mV p-p	23 mA 16 mA
R2	+5 Vdc ±5% +12 Vdc ±5% -12 Vdc ±5%	100 mV p-p 50 mV p-p 50 mV p-p	64 mA 25 mA 78 mA
Maximum total power consumption approximately 3 watts. Typical total power consumption approximately 2 watts.			

DIGITAL INTERFACE

The R24 provides LS TTL or CMOS compatible logic levels that are functionally equivalent to EIA RS232/449 and CCITT V.24.

Input Logic	Allowed Input Voltage Levels
Low	-12.0V to +0.8V Sinking <10 μA
High	+4.0V to +5.0V Sourcing <10 μA

Digital inputs are directly CMOS compatible. Interfacing with standard TTL or low-power Schottky TTL requires an external pull-up resistor.

Output Logic	Allowed Output Voltage Levels
Low	0.0V to +0.4V Sinking 0.36 mA
High	+4.0V to +5.0V Sourcing 100 μA

Digital outputs are directly CMOS or low-power Schottky TTL compatible.

TRANSMISSION LINE INTERFACE

The R24 provides an analog interface that must generally be transformer coupled to ensure normal telephone line isolation. Through appropriate selection of transformers and other interface circuitry, the R24 can be configured to operate on leased or dial-up telephone lines, or on other special private networks. For the dial-up interface, Rockwell offers an FCC registered module that allows direct connection to this network. For the leased line interface, only transformers with characteristics similar to those utilized on the R24 modem evaluation board are required for this connection.

The receiver and transmitter line interfaces are single-ended (non-transformer coupled) signals with the following characteristics:

Transmitter Output (Normal)

Output Impedance: 600 ohms ±2%
Maximum output level: ≤0.0 dBm

Transmitter Output (Alternate) Low Impedance:

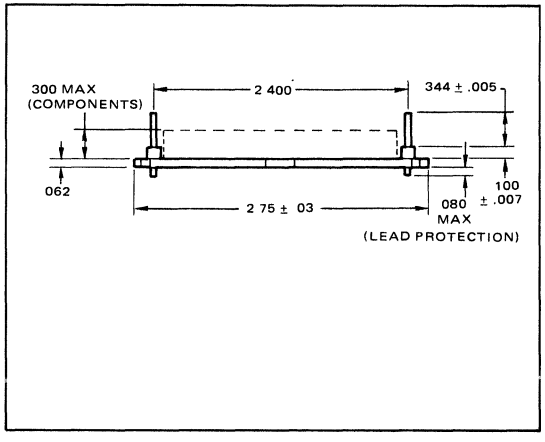
Output Impedance: 0 ohms (op amp output)
Maximum output level ≤ +6.0 dB

Note: This output for transformer loss compensation.

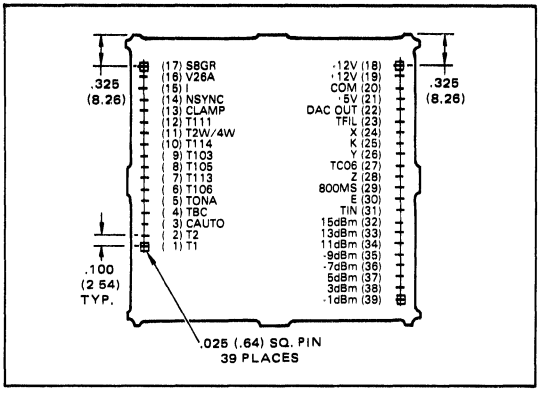
Receiver Input:

Input Impedance: 15.8K ohms ±1%
Maximum Input Level: 0.0 dBm

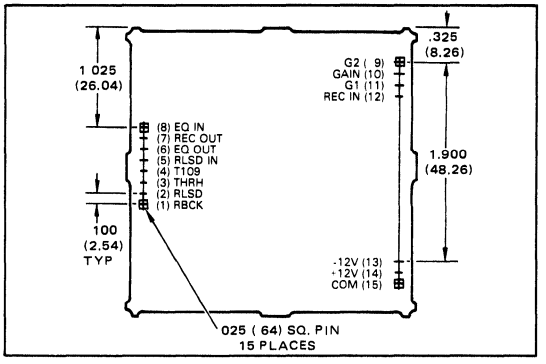
MECHANICAL SPECIFICATIONS



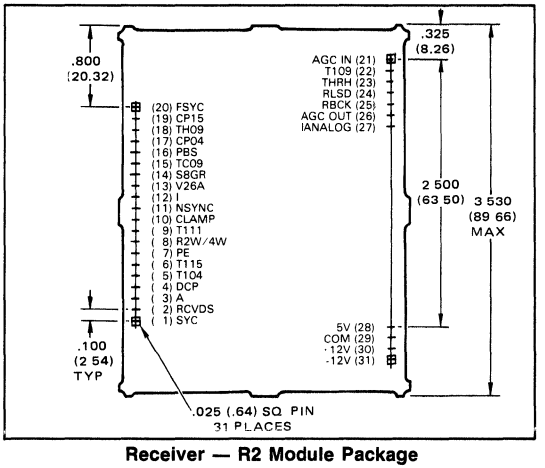
NOTE: This cross-section is common to all modules.



Transmitter Module Package



Receiver — R1 Module Package



Receiver — R2 Module Package

NOTES: 1) Dimensions in inches (millimeters).
2) Component side shown

7

PRINTED CIRCUIT BOARD MOUNTING OPTIONS FOR THE R24 MODULES

Three methods of mounting are commonly used. Each configuration has certain distinct advantages.

Mounting Method	Type of Connection or Connector Used	Basic Advantage
Standard Flush PCB Component Mount	Wave Soldered Into Standard PCB Eyelets	Lowest Height Profile
Above Board Low Profile Socket	Connectors (SAE Series 3000 or Methode Series 1000) These Sockets are Wave Soldered Into Standard PCB Eyelets	Plug-in Capability at Low Cost
PCB Plug-in Sockets (Bullets)	Connectors (AMP Miniature Spring Sockets.) Pin Sockets are Individually Soldered Into PCB Eyelets	Lowest Profile for Plug-in Capability

ENVIRONMENTAL SPECIFICATIONS:

Operating temperature: 0°C to 60°C
Storage temperature: −40°C to +80°C
Relative humidity: to 95% (non-condensing)
Altitude: −200 to 10,000 feet (−6.1 meters to 3,049 meters)
Burn-In: 96 hours at 70°C

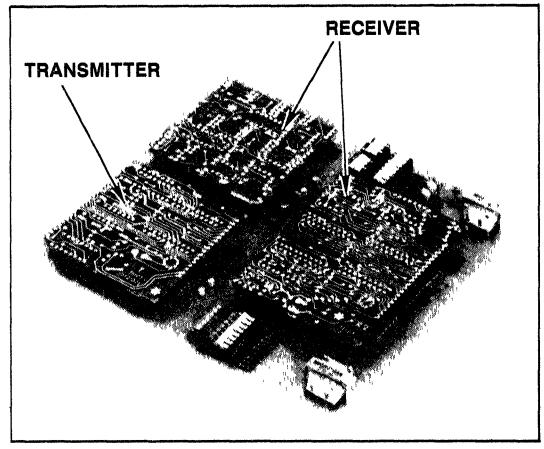
Ordering Information

When ordering, specify products as follows:

R24 — Set of 3 modules (T, R1, R2)
R24MEB — Modem Evaluation Board

R24 MODEM EVALUATION BOARD

To facilitate evaluation and design-in of the R24 modem for new and existing equipment designs, an R24 Modem Evaluation Board (R24MEB) is available. The R24MEB can be easily combined with terminal systems for real-time performance evaluation.



R24 Modem Evaluation Board (R24MEB)

The Modem Evaluation Board is equipped with a standard 31 pin edge connector, control switches, output level jumper, and interface transformers. These features allow full control of the interface circuitry. In addition, this unit can be used directly in a U.S. leased line configuration. The R24MEB is recommended for all first-time users to assist in their evaluation. Complete documentation is supplied with each initial R24MEB.

Rockwell

RDAA
ROCKWELL DATA ACCESS ARRANGEMENT MODULE

PRELIMINARY

SECTION 1 — INTRODUCTION

This document is an aide to customers installing, operating and troubleshooting the Rockwell Data Access Arrangement (RDAA) Module designed and manufactured by Rockwell International.

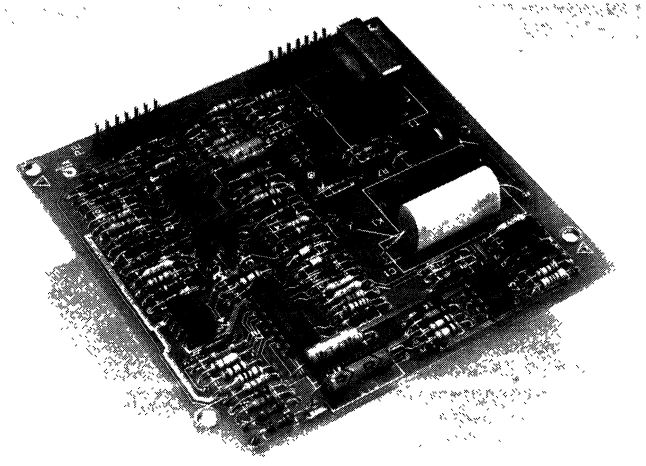
THE RDAA MODULE

The RDAA Module enables the modem user to make direct connections of their modems to the domestic switched telephone network. The RDAA is completely registered with the Federal Communications Commission under Rules Part 68. Therefore, *no* user re-registration of OEM data communication equipment is necessary when used with the RDAA. This means a definite cost-savings for the OEM equipment designer.

In addition to establishing your desired data transmission path, the RDAA also features an automatic answering function, line surge and hazardous voltage protection, switch hook status indication, ringing indication and automatic signal level control. Automatic dialing can be performed by pulsing the OH relay or by transmitting tone pairs.

FEATURES

- Pre-registered (under FCC Rules, Part 68) for direct connection to dial telephone network
- Integral Data Access Arrangement (DAA)
- Automatic dialing—pulse or tone
- Establishes data transmission path
- Automatic answering function
- Surge and hazardous voltage protection
- Switch hook status indication
- Ringing indication
- Automatic line signal output limiting
- Programmable or Permissive (strap selectable) connection arrangements
- Small size (approximately 3.95″ by 3.94″) (100 mm. by 100 mm.)



RDAA Module

The RDAA is easily incorporated into the users end product by either using the provided mounting holes, and/or using the card-guides without card-edge connector. The small size of the RDAA makes it ideal for piggyback type mounting.

The Rockwell RDAA printed circuit board is 3.94 inches (100 mm.) in width and 3.94 inches (100 mm.) in depth.

SELECTABLE CONFIGURATIONS

As a prerequisite, telephone companies require that the signal level received at their local central office not exceed −12 dBm. Several different connection arrangements have been established (as documented in the FCC Rules, Part 68) to meet this requirement.

By jumper selection (Figure 1) the RDAA can be configured to operate in either the Programmable (PG) or Permissive (PM) connection arrangement. This is accomplished by placing the jumper in either the W2 or W1 locations for the desired mode. W1 jumper in, W2 jumper out for the permissive mode. W2 jumper in, W1 jumper out for the programmable mode.

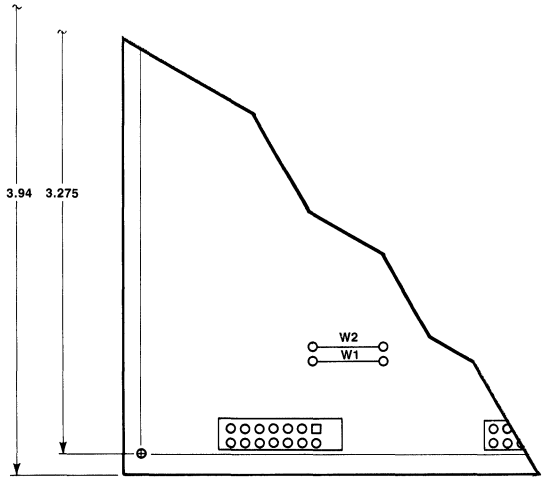


Figure 1. RDAA Module Jumper Selection Location

When using the Programmable connection arrangement, the maximum signal level allowed to be transmitted across T and R is set by a resistor installed by the telephone company in their wall jack (RJ45S or RJ41S) at the customer location. The resistor interacts with the RDAA through the leads PR and PC to program the maximum output level in one dB steps between −12 dBm and 0 dBm. Selection of the resistor from thirteen possible values is based on loop loss measurements performed by the telephone jack installer. The Programmable arrangement provides for the transmission of the maximum allowable amount of power. Therefore, this arrangement offers optimum performance over long loops.

When the Permissive connection arrangement is employed, the maximum signal output level across T and R is fixed at −9 dBm. The Permissive jacks (RJ11C) used for line connections are the same jacks used for standard voice installations. Therefore, this arrangement provides for greater mobility of user equipment.

RDAA DIMENSIONS

The dimensions for the RDAA Module are given in Figure 2.

MATING CONNECTORS

The mating connectors of the RDAA are as follows:

1. Two row (14 pins) ribbon type connectors .1″ spacing between pins.

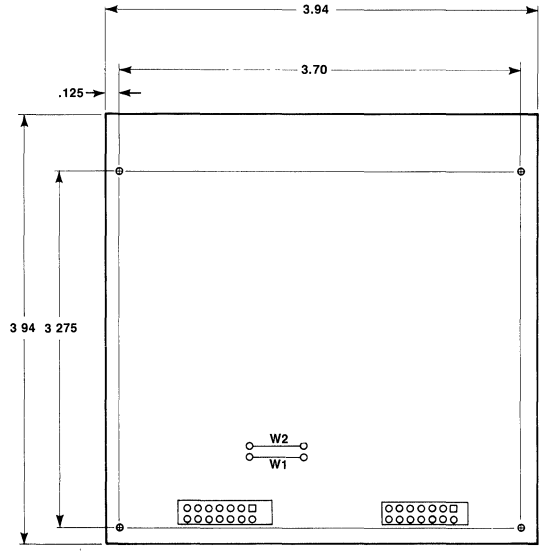


Figure 2. RDAA Module Dimensions

SECTION 2 — INTERFACE DESCRIPTION

INTERFACE CIRCUIT DESCRIPTION

The following paragraphs describe in detail the RDAA interface circuits shown in the block diagram (Figure 3) and the interface circuits listing (Table 2-1).

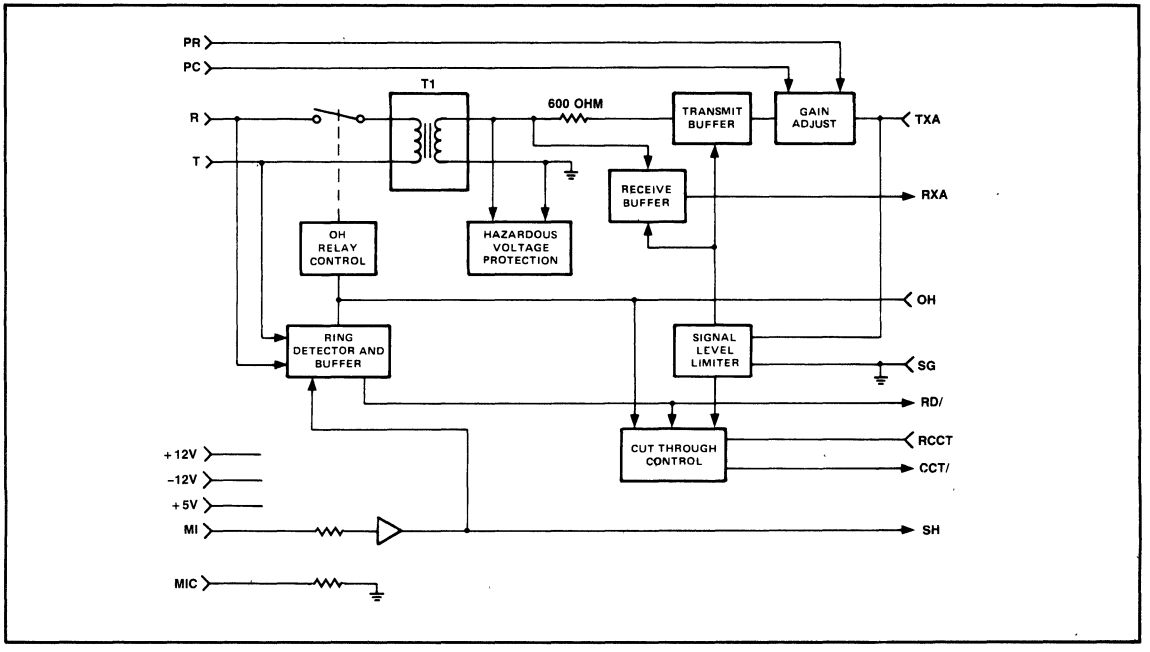


Figure 3. RDAA Functional Block Diagram

Table 2-1. RDAA Interface Circuits

Lead Designation	Signal Direction To: User	RDAA	Both	Function
R, T			X	Transmission leads for data signals.
MI, MIC			X	Leads to telephone set switch hook
PR, PC			X	Leads to programming resistor.
+5V, +12V, −12V		X		DC power required.
SG			X	Signal ground required.
RD/	X			Ringing signal present indication.
RCCT		X		To request data transmission path cut through.
OH		X		To control Off-Hook relay
SH	X			Status of telephone set switch hook.
CCT/	X			Transmission path cut through indication.
TXA		X		Lead to modem output.
RXA	X			Lead to modem input.

SG

The SG (Signal Ground) is the common reference for all modem interface signals.

RD/

RD/ (Ring Detect) indicates to the user by an ON (Low) condition that a ringing signal is present. The RD/ signal will not respond to momentary bursts of ringing less than 125 ms in duration, or to less than 40V rms, 15 to 68 Hz appearing across Tip and Ring with respect to ground. RD/ is also used to disable the transmission path. The electrical characteristics of the RD/ signal are shown in Table 2-2.

Table 2-2. Output Signals RD/ SH and CCT/ Characteristics

Output Logic State	Output Levels
LOW	0.0 to 0 4V while sinking < 1.6 ma
HIGH	2.4 to 5.0V while sourcing < 40 μA

RCCT

RCCT (Request Coupler Cut-Through) is used to request that a data transmission path through the RDAA be connected to the telephone line. When RCCT goes OFF (Low), the cut-through buffers are disabled and CCT will go OFF (High) within 1 millisecond. RCCT must be OFF (Low) during dial pulsing but ON (High) for tone address signaling. The electrical characteristics of the RCCT signal are shown in Table 2-3.

Table 2-3. Input Signals RCCT and OH Characteristics

Input Logic State	Input Levels
OFF or LOW	0.0 to 0.8V, load current ≤ 0.36 ma
ON or HIGH	RCCT = 2.0 to 5.0V, load current ≤ 20 μa
	OH = 2.0V, load current ≤ 100 μa
	5.0V, load current ≤ 250 μa

OH

OH controls the OFF-HOOK relay. Applying an ON (High) signal to OH closes the OH relay and establishes a DC path between T and R. Maximum delay between the ON signal to OH and the close of the OH relay is 10 ms. When originating a call, an ON (High) signal is used to request dial tone. After detecting dial tone, OH can be pulsed to generate the dial pulses corresponding to the number of the called station (see Section 4.2). On incoming calls, an ON (High) signal to the OH lead initiates the answering sequence (see Section 4.1). The characteristics of the OH signal is shown in Table 2-3.

NOTE

WARNING. If OH is asserted to a logic high before the incoming call ring signal is completed, the OH reed relay switch contacts may suffer degradation.

SH

An ON (High) signal on the SH lead indicates to the user that the associated telephone (if used) is in the talk mode i.e., a contact closure exists between MI and MIC. The characteristics of the SH signal are shown in Table 2-2.

CCT/

CCT/ is the Coupler Cut Through. An ON (Low) signal to the CCT/ lead indicates to the user that the data transmission path through the RDAA is connected. The ON (Low) state does not indicate the status of the telephone line or connection. The characteristics of the CCT/ signal are shown in Table 2-2.

TXA

TXA (Transmit Analog) is the lead from modem transmitter output. This lead should be tied to GND when the modem is in the receive only mode.

RXA

RXA (Receive Analog) is the lead to modem receiver input. This lead may be left open when the modem is in the transmit-only mode.

POWER REQUIREMENTS

The following power must be provided at the RDAA interface.

A. +12 VDC ±5% @ 15 ma with a maximum ripple of 50 mv peak-to-peak

B. +5 VDC ±5% @ 20 ma with a maximum ripple of 100 mv peak-to-peak

C. −12 VDC ± 5% @ 15 ma with a maximum ripple of 50 mv peak-to-peak.

HAZARDOUS VOLTAGE PROTECTION

Lightning induced surge voltages and other hazardous voltages are limited to 10.0 volts peak between the secondary leads of the coupling transformer T1. The isolation between the relay contacts and coils provides the protection of the telephone line from hazardous voltages appearing on any control lead.

RING DETECTOR AND TIMER

When the Ring Detector detects the presence of a ringing signal ranging from 15.3 to 68 Hz with voltage levels of 40 to 150 VRMS across Tip and Ring (T and R) leads, after a delay of 125 ms to 500 ms, it will send an RD/ (Ring Detect) signal to the user's data terminal equipment (DTE). If the DTE is conditioned for answering, the DTE will return an ON signal on OH and RCCT. The OH signal closes the OH relay and starts a timer. The timer is used to provide a quiet interval of more than two seconds between the closing of OH relay and the connection of data transmission path. This allows the telephone company to properly engage their billing equipment. After this delay the CCT/ interface lead goes ON (Low) and data transmission may begin.

RD/ will go OFF (High) in less than 400 MSEC after the ringing signal is stopped. The ring detector is disabled when OH is ON (High) or SH is ON (High).

SIGNAL LEVEL LIMITER AND GAIN CONTROL CIRCUITRY

The limiter monitors the signal level applied to the RDAA input lead TXA and is unaffected by the level of receive signal. When the applied signal amplitude becomes greater than +7 dBm for a period of 1.3 to 3 seconds, the transmission path is disconnected via the transmit and receive buffers, and the output signal CCT/ will go OFF (High).

NOTE

The off-hook relay is not affected by the limiting function, therefore, so triggering the limiting function need not result in call termination.

Reducing the input signal amplitude to less than +7 dBm will reset the limiter in less than 4 milliseconds, restore the data transmission path, and cause the signal CCT to go ON (Low).

In order not to activate the limiter during normal operation, care must be taken to ensure that the maximum signal amplitude into the RDAA input TXA never exceeds +6 dBm. If the modem output has a tolerance of ± 1 dB, then it is recommended to set the modem output to +5 dBm (± 1 dB), so that the maximum signal amplitude into TXA is 6 dBm.

The output control circuitry contains a variable gain buffer which reduces the RDAA output to the maximum allowed level across T and R. When the RDAA is jumpered to operate in the Programmable mode, the resistor in the telephone company wall jack sets the output level to one of thirteen possible values. If the RDAA is jumpered to operate in the Permissive mode, then an internal resistor will set the output to a fixed value. The relationship between the RDAA input amplitude (in dBm) across TXA and GND and the nominal RDAA output level across T and R is given below:

A. For Programmable mode: output level across T and R = (input amplitude at TXA −7 dB + (Programmed level set by wall jack resistor).

B. For Permissive mode: output level across T and R = (input amplitude at TXA) −16 dB.

IMPEDANCE SPECIFICATIONS

On-Hook DC:	The DC resistance between T and R, and between either T or R and signal ground are greater than 10 megohms for DC voltages up to 100 volts.
On-Hook AC:	The on-hook AC impedance measured between T and R is less than 40K ohms (15.3 Hz minimum).
Off-Hook DC:	Less than 100 ohms.
Off-Hook AC:	600 ohms nominal when measured between T and R.
TXA and GND:	2 megohms typical (operational amplifier voltage follower input impedance).
RXA and GND:	75 ohms typical (operational amplifier voltage follower output impedance).

INSERTION LOSS

There is no insertion loss for the RDAA. The RDAA contains a receive buffer which compensates for transformer insertion loss. For this reason, additional receive buffering is not necessary.

7

SECTION 3 — INSTALLATION/CHECKOUT

RDAA CONNECTION TO TELEPHONE LINE

Connection of the telephone line interface pins of the RDAA to the network shall be made via standard jacks and plugs as shown in Figure 4. Cable color codes are also shown in Figure 4. A number of telephone line cord manufacturers produce the standard plugs and cables (Meyer Wire Co., Hamden, CT; Virginia Plastics, Roanoke, VA, etc.)

TELEPHONE SET AND JACK ORDERING INFORMATION

If it is desirable to have manual call origination or alternate voice capability, an exclusion key telephone set may be ordered from a local telephone company. The telephone line may be transferred to the telephone set by lifting both the handset and the exclusion key, if the telephone is configured as Data Set Controls Line. This operation is for manual origination or alternate voice transfer (refer to paragraph 4.4 for manual origination procedure). A call may be terminated by replacing the handset in its cradle and taking OH low if OH is not already low.

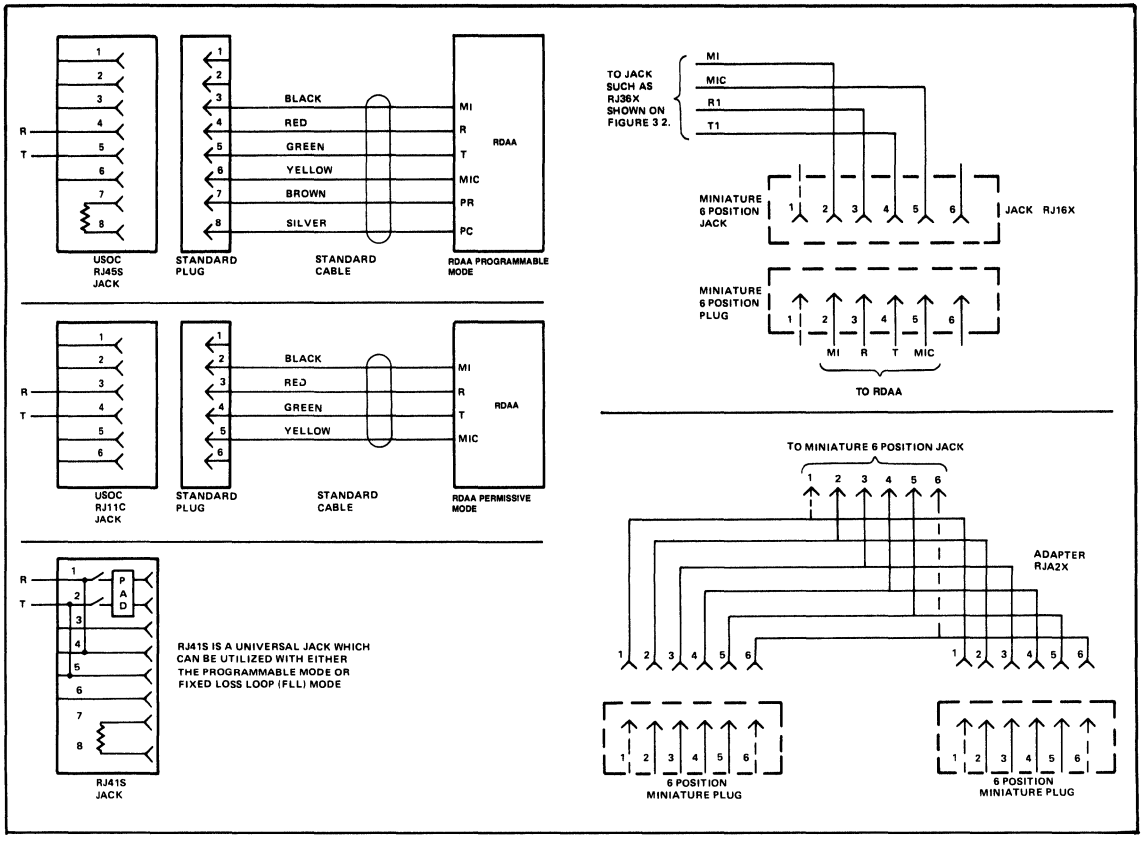


Figure 4. Standard Jacks, Plugs and Cable Color Codes

The ringer of the telephone set may be disconnected by the telephone company to prevent the bell from ringing.

The telephone company provides an exclusion key telephone under the Universal Service Order Code (USOC) RTC. This telephone set has the following customer options:

A. A1 - Telephone set controls line
B. A2 - Data set controls line
C. B3 - Aural monitoring not provided
D. B4 - Aural monitoring provided (See Note 1)
E. C5 - Touch tone dial
F. C6 - Rotary dial
G. D7 - Switch hook indication
H. D8 - Voice mode indication only (See Note 2)

NOTES

1. The aural monitoring feature allows the telephone handset to be used for listening to line signals without interfering with data transmission.
2. In this option the make contact of the exclusion key and a make contact on the switchhook are connected in series and to the mode indication leads MI and MIC of the data jack. Therefore, the SH signal of the RDAA goes ON only when the exclusion key is lifted.

When ordering this telephone, specify the USOC number RTC and the following options:

A. A2 - Data set controls line
B. B3 - Aural monitoring not provided
   or
   B4 - Aural monitoring provided
C. C5 - Touch tone dial telephone (503C)
   or
   C6 - Rotary dial telephone (2503C)
D. D8 - Voice mode indication only

Another telephone set provided by the telephone company is the Model 502 with exclusion key. To order this telephone set, specify the following:

A. Modem 502 with exclusion key
B. Data set controls line

A summary of the information for ordering telephone and jacks is given in Table 3-1. Examples of typical installation are given in Figure 3-2.

Table 3-1. Telephones and Jacks Ordering Information

Output Configuration	Optional Telephone Set	FCC Reg. No.	Ringer Equivalent	Telephone Jack USOC No.	Telephone Set USOC No.
Programmable	With Telephone Set	AMQ9SQ 67943 DP-E	.8B	[1]RJ36X and [2,3]RJ45S	RTC or 502 with exclusion key
	Without Telephone Set	AMQ9SQ 67943 DP-E	.8B	[2,3]RJ45S	N.A.
Permissive	With Telephone Set	AMQ9SQ 67943 DP-E	.8B	[1]RJ36X and RJ16X or [4]RJA2X and RJ11C	RTC or 502 with exclusion key
	Without Telephone Set	AMQ9SQ 67943 DP-E	.8B	RJ11C	N.A.

Notes:
1. RJ36X is an 8 position miniature jack into which the telephone plugs. Rather than using an RJ36X jack, the telephone company may use a connecting block to connect the telephone set and data jack to the telephone line.
2. RJ41S is a universal data jack. It may be used for either Programmable or Fixed-Loss Loop mode. The RJ45S jack is preferred, because it costs less.
3. For multiple connections, the RJ45M jack should be ordered. The letter M indicates multiple single line jack for up to 8 lines. Specify the number of lines required when ordering.
4. RJA2X is the adapter shown in Figure 3-1. The use of the RJ36X and RJ16X jacks is recommended.

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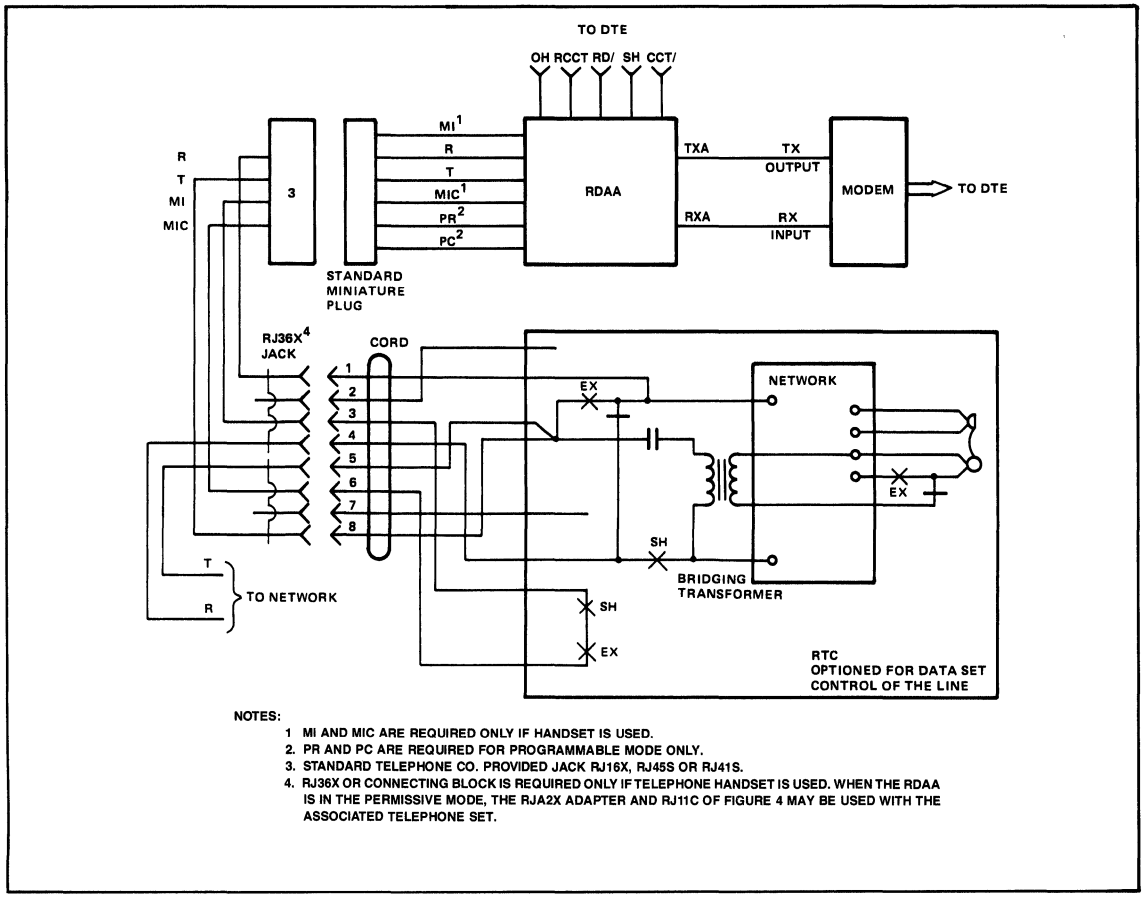


Figure 5. Transmit and Receive (Half Duplex) and (Full Duplex)

MODEM INTERFACE

There are 4 possible two-wire modes of operation configurations: receive-only, transmit-only, and receive and transmit (half duplex) and full-duplex (using two different frequencies simultaneously) as described below:

A. For the half-duplex and full-duplex configurations, the interface connection circuitry could be as shown in Figure 5.

B. For the receive-only configuration, the connection circuitry is the same as that shown in Figure 5, except that the RDAA input lead TXA is grounded rather than connected to the modem transmitter output.

C For the transmit-only configuration, the RDAA lead RXA is left open rather than connected to the modem receiver as shown in Figure 5.

For a 4-wire full-duplex configuration, 2 RDAA modules and 2 telephone lines are required. The connection circuitry consists of one 2-wire receive-only connection, and one 2-wire transmit-only connection.

MODULE MOUNTING AND SECURING

The RDAA may be physically incorporated into the OEM's end product by using the four corner (0.156 inch diameter) mounting holes and self-locking plastic standoffs, or by bolting the RDAA module to a rigid structure. The RDAA module may also be mounted using card guides without card edge connector.

A number of manufacturers such as Richlock Corporation, Chicago, IL., produce plastic standoffs (Part Number CBS-3N).

ELECTRICAL INTERFACE

Electrical connection to the RDAA module is made through ribbon type connectors. The connector(s) interface pins (Figure 2) are contained on the component side of the board. There are two test points brought out to the interface connector of the board. Therefore care must be taken to prevent shorting test points with any of the other interface signals.

The RDAA telephone line interface connector pins are physically separated from the RDAA DTE interface connector pins, as shown in Figure 2 and described in Table 3-2.

Table 3-2. RDAA Telephone and Modem Interface

Type Interface Circuit	RDAA Connectors/ Pin No.	Interface Circuit/Signal
DTE Interface Connections	P2-1	CCT/
	P2-2	RXA
	P2-3	TXA
	P2-4	OH
	P2-5	RCCT
	P2-6	RD/
	P2-7	−12V
	P2-8	SH
	P2-9	GND
	P2-10	TP2 EXCESSIVE POWER DETECT
	P2-11	+12V
	P2-12	+5V
	P2-13	N/U
	P2-14	TP1 BILLING DELAY TIME
Telephone Line Interface Connections	P1-4	PC
	P1-3	PR
	P1-1	MIC
	P1-2	MI
	P1-(5-8) & (11-12)	(Not Used)
	P1-9, 10	R
	P1-13, 14	T

Care must be taken in routing the telephone interface pins to the telephone jack. The FCC (Rules, Part 68) requires that the telephone interface leads shall be separated from the leads or metallic paths connecting to power connections.

NOTE

Power connections are those connections between commercial power and any transformer, power supply rectifier, converter, or other circuitry associated with the RDAA. The connection of the interface pins (including the ±12V and +5V) shown in Figure 2 are not power connections.

The telephone interface leads shall not be routed in the same cable (or use the same connector) as leads or metallic paths connecting to commercial power.

FCC (Rules, Part 68) also requires that the telephone leads T and R be separated from metallic paths to leads connecting to non-registered equipment, when specification details provided to FCC do not show that the interface voltages are less than non-hazardous voltage source limits in Part 68. T and R shall not be routed in the same cable (or use adjacent pins on the same connector) as metallic paths to leads which are not considered non-hazardous. All DTE interface connector signals shown in Table 3-2 have been established as non-hazardous.

Therefore, in routing the telephone interface leads from the RDAA P1 connector to the telephone jack, the following precautions must be strictly adhered to. The telephone jack interface routing path should be as direct as possible. Any cable used in establishing this path should contain no signal leads other than possibly the (previously established as non-hazardous) DTE interface signals shown in Table 3-2. Any connector used in establishing this path should contain no commercial power source signal leads, and adjacent pins to the T and R (Tip and Ring) pins in any such connector should not be utilized by any signals other than possibly those shown in Table 3-2. Also the DTE interface routing path should be made as short as possible.

INSTALLATION PROCEDURE

A. Check the telephone line interface cable(s) plug(s) and jack(s) (Figure 4). If the USOC RJ41S jack is used for the Programmable mode, ensure that the jumper W2 is installed and W1 jumper is removed for the programmable mode of operation.

B. Make sure the telephone company installer has measured the loop loss correctly and has selected the proper programming resistor in the RJ45S or RJ41S jack.

NOTE

You have the right to know the method used by the installer for measuring loop loss and selecting the programming resistor.

7

C. Check the power supplies to see if they meet the proper requirements specified in paragraph 2.2.

D. Insert the telephone cable plug into the jack, and make the DTE interface connection. Then switch on the power supplies.

OPERATIONAL CHECKOUT PROCEDURE

The following procedures check out the RDAA in association with a modem, a data terminal, a telephone set and an automatic dialer. The telephone set is required only in the manual origination mode (refer to paragraph 4.4) or if alternate voice communication is desired. The automatic dialer is required only in the automatic dial mode (refer to paragraph 4.3).

AUTOMATIC ANSWER MODE

A. Set the modem transmitted output level to +5 dBm.

B. Call the local modem from a remote station.

C. Follow the instructions given in Figure 6.

D. Transmit data from the local terminal to the remote terminal and monitor the CCT/ signal. It should stay low.

E. Terminate the call sequence and verify the received data.

AUTOMATIC ORIGINATE MODE

A. Set the modem transmitted output level to +5 dBm.

B. Follow the procedure of Figure 8 for touch tone origination or Figure 7 for pulse dial origination.

C. Transmit data from the local terminal and monitor the CCT/ signal. It should stay low.

D. Terminate the call sequence and verify the received data.

MANUAL OPERATION MODE

A. Set the modem transmitted output level to +5 dBm.

B. Follow the instructions given in paragraph 4.4.

C. Transmit data from the local terminal. CCT should stay low.

D. Terminate the call sequence and verify the received data.

SPECIAL INSTRUCTIONS TO USER

Your Rockwell Data Access Arrangement has been registered with the Federal Communications Commission (FCC). To comply with the FCC regulations you are requested to observe the following:

A. All direct connections to the telephone lines shall be made through standard plugs and jacks as specified in Figure 4 and Table 3-1.

B. It is prohibited to connect the RDAA to pay telephones or party lines.

C. You are required to notify the local telephone company of the connection or disconnection of the RDAA, the make, the modem number, the FCC registration number, the ringer equivalence number (refer to Table 3-1) and the particular line to which the connection is made. If the proper jacks are not available, you must order the type of jacks to be used from the telephone company (Refer to Table 3-1 for the proper jacks and telephones.)

D. You should disconnect the RDAA from the telephone line if it appears to be malfunctioning. If the RDAA needs repair, return it to Rockwell International. This applies to equipment both in and out of warranty. Do not attempt to repair the unit as this will violate the FCC rules.

E. The RDAA contains protective circuitry to prevent harmful voltages being transmitted to the telephone network. If however, such harmful voltages do occur, then the telephone company has the right to temporarily discontinue your service. In this case, the telephone company shall:

1. Promptly notify you of the discontinuance.
2. Afford you the opportunity to correct the situation that caused the discontinuance.
3. Inform you of your right to bring a complaint to the FCC concerning the discontinuance.

F. The telephone company also has the right to make changes in their facilities and services which may affect the operation of your equipment. However, you shall be given notice in writing by the telephone company adequate to allow you to maintain uninterrupted service.

G. Labeling Requirements:

1. The FCC requires that the following label be prominently displayed on an outside surface of the OEM's end product.

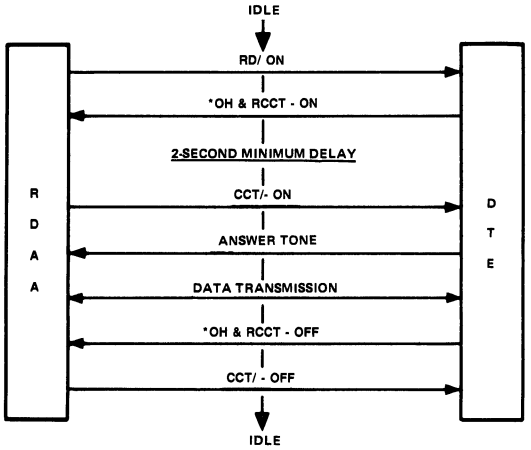
Unit contains Registered Protective Circuitry which complies with Part 68 FCC Rules FCC Registration Number: Ringer Equivalence: .8B

2. The size of the label should be such that all the required information is legible without magnification.

SECTION 4 — OPERATING INSTRUCTIONS

AUTOMATIC ANSWER

The connection of the data transmission path for automatic answer is as described in paragraph 2.4. To disconnect the data transmission path, just turn off OH and/or DA, as shown in Figure 6.



*DA MAY BE ON PERMANENTLY FOR AUTOMATIC ANSWER.

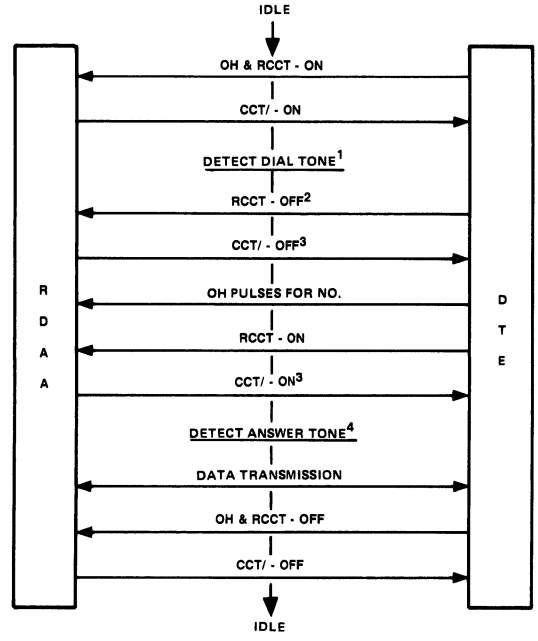
Figure 6. Automatic Answering Sequence

AUTOMATIC DIAL

DIAL PULSE ORIGINATION

The DTE must provide the logic to turn ON the OH and DA leads, detect dial tone (or time for 3 seconds to ensure dial tone present), then turn OFF the DA lead and generate the dial pulses corresponding to the called number (Figure 7). The 2-second delay period between OH and DA going ON and the response of CCT going ON will not be invoked in the origination mode. The DTE should monitor for call progress indication (dial tone, busy tone, answer tone, and call intercept).

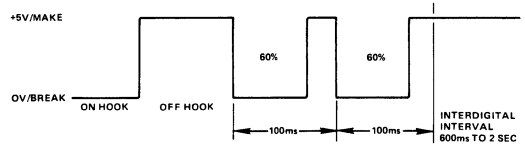
Requirements for proper call establishment exist on the pulse repetition rate (8 to 11 pulses per second), off duty cycle (60 percent nominal), interdigital delay timing (600 ms to 2 seconds) and chatter and spurious makes and breaks. The RDAA off-hook relay is a Reed relay designed to long life. Bell System requirements for pulse and touch-tone dialing are described in their Communications reference "Electrical Characteristics of Bell System Network Facilities at the Interface with Voiceband Ancillary and Data Equipment" (PUB 47001).



NOTES.
1. DIAL TONE DETECTION IS NOT PROVIDED WITHIN THE RDAA. ALTERNATIVELY, DTE MAY START FROM IDLE, TURN ON OH, THEN TIME FOR 3 SECONDS TO ENSURE DIAL TONE PRESENT AND PULSE OH FOR NUMBER.
2. DA MUST BE OFF DURING DIAL PULSING. DA MAY BE ON AT ALL OTHER TIMES.
3. THE DA TO CCT RESPONSE TIME IS LESS THAN 1 MS.
4. ANSWER TONE DETECTION CIRCUITRY IS NOT PROVIDED WITHIN THE RDAA.

Figure 7. Dial Pulse Origination Sequence

The following is an example for pulse dialing the digit #2 through the OH lead.



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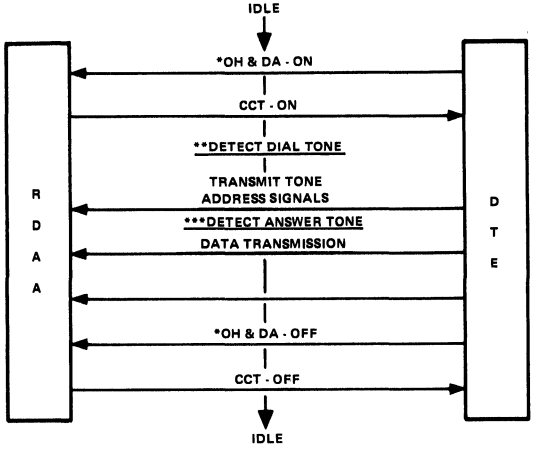
The OH lead can be pulsed directly via microprocessor port, or a commercially available "binary to dial pulse" LSI device such as the Rockwell CRC 8000, the General Instrument AY-5-9151 series, or the Motorola MC 14408. These devices can accept 4-bit binary digital inputs, buffer these digits, and output the OH dial pulses upon command. Also available from numerous semiconductor manufacturers (National, Mostek, General Instrument, Motorola, etc.) are LSI devices capable of interfacing directly to a key board and producing suitable dial pulses.

TOUCH-TONE ORIGINATION

The user's terminal must provide the logic to turn ON the OH and RCCT signals, detect the dial tone (or time for 3 seconds to ensure dial tone present) and transmit the tone-address signals via the TXA lead (Figure 8). The 2-second delay period between OH and RCCT going ON and CCT/ going ON is not invoked in the origination mode. The DTE should monitor for call progress indications (dial tone, busy tone, answer tone, and call intercept).

It should be noted that tone address signaling method is significantly more complicated in terms of hardware requirements than simple pulse dialing. The necessary tone pair generators must be added by the user. A number of semiconductor manufacturers produce monolithic LSI tone generators (AMI, Mostek, Motorola, National, General Instrument, Intersil, etc.). These tone pair generators are designed to interface with keyboards or digital ports and may require varying degrees of additional low pass filtering to reduce harmonic distortion. Touch-tone dialing is significantly faster than pulse dialing, but it may not be available in some locations.



*DA MAY BE PERMANENTLY ON.

**ALTERNATIVELY, USER MAY TIME FOR 3 SECONDS TO ENSURE DIAL TONE PRESENT.

***ANSWER TONE DETECTION CIRCUITRY IS NOT PROVIDED WITHIN THE RDAA

Figure 8. Touch-Tone Origination Sequence

Bell System requirements exist on minimum and maximum tone pair transmit power for proper call address signaling. When the RDAA is in the programmable mode, the gain of the RDAA transmit leg is set by a programming resistor in the telephone jack (over thirteen possible values). This makes establishment of the tone pair signal level to be input to the RDAA (at TXA) which meets the Bell System requirements difficult. It is therefore necessary to operate the RDAA in the Permissive mode for touch-tone origination. In this event the proper input power level (per frequency pair) to the RDAA (at TXA) would be +15 dBM (nominal). This level is well above the RDAA automatic limiter threshold. But the RDAA limiter activates (cuts off transmission path) only if threshold power level is continuously exceeded for about one second minimum, and quickly resets itself if the power level drops below threshold. If the tone pair duration time is restricted to significantly under one second (the minimum duration requirement is only 50 milliseconds) and the minimum interdigital time requirement (45 milliseconds) is observed, the limiter will not be activated. These requirements are easily met if the tone pair generation is under logic control. If the generation is controlled via keyboard input, the limiter will be activated if a key is depressed and held for more than a second, but will recover during the interval between key closures. However, the possibility exists that transients occurring at limiter activation and resetting may endanger proper call origination.

AUTOMATIC CALLING UNIT

Automatic dialing capability may also be added to a data transmission system simply by purchasing or leasing a separate box termed an "Automatic Calling Unit" (ACU). Such units are available from a variety of manufacturers. ACU's are available utilizing pulse or tone dialing. Connections of ACU to the data transmission system may be different for different ACUs. The standard protocol involved in interfacing between the user's data terminal equipment and an ACU is documented in CCITT Recommendation V.25 and also in EIA Standard RS-366. "Interface Between Data Terminal Equipment and Automatic Calling Equipment for Data Communication." It should be re-emphasized that a separate ACU is not necessarily required for automatic dial capability. The RDAA and some external hardware and/or software (as previously described) can suffice.

MANUAL ORIGINATION

For manual origination a telephone set with an exclusion key must be ordered from the local telephone company (refer to Table 3-1). After lifting both the handset and the exclusion key, a call may be originated or answered in the same manner as normal telephone service. When the handset and the exclusion key are lifted (MI is shorted to MIC), the signal SH is turned ON. If the user's data terminal is ready, it may respond with OH and RCCT. The RDAA will then turn ON the CCT/ signal. When answer tone is heard, the operator replaces the handset in its cradle. the SH signal will go Low and the data transmission path is connected. When data transmission is completed, the terminal turns OFF the OH signal and returns to the idle state.

SECTION 5 — FAULT ISOLATION

CUSTOMER REPAIR LIMITATIONS

Under the FCC Rules, no customer is authorized to repair an RDAA module. In the event of an RDAA malfunction, return the faulty RDAA to Rockwell International. It is recommended that the following fault isolation instructions provided in this section be performed prior to returning a suspected RDAA module. A periodic check of the DC power supplies is also recommended.

FAULT ISOLATION

The fault isolation flow chart (Figure 9) has been prepared specifically as an aid to the user for locating possible network and/or RDAA module malfunctions.

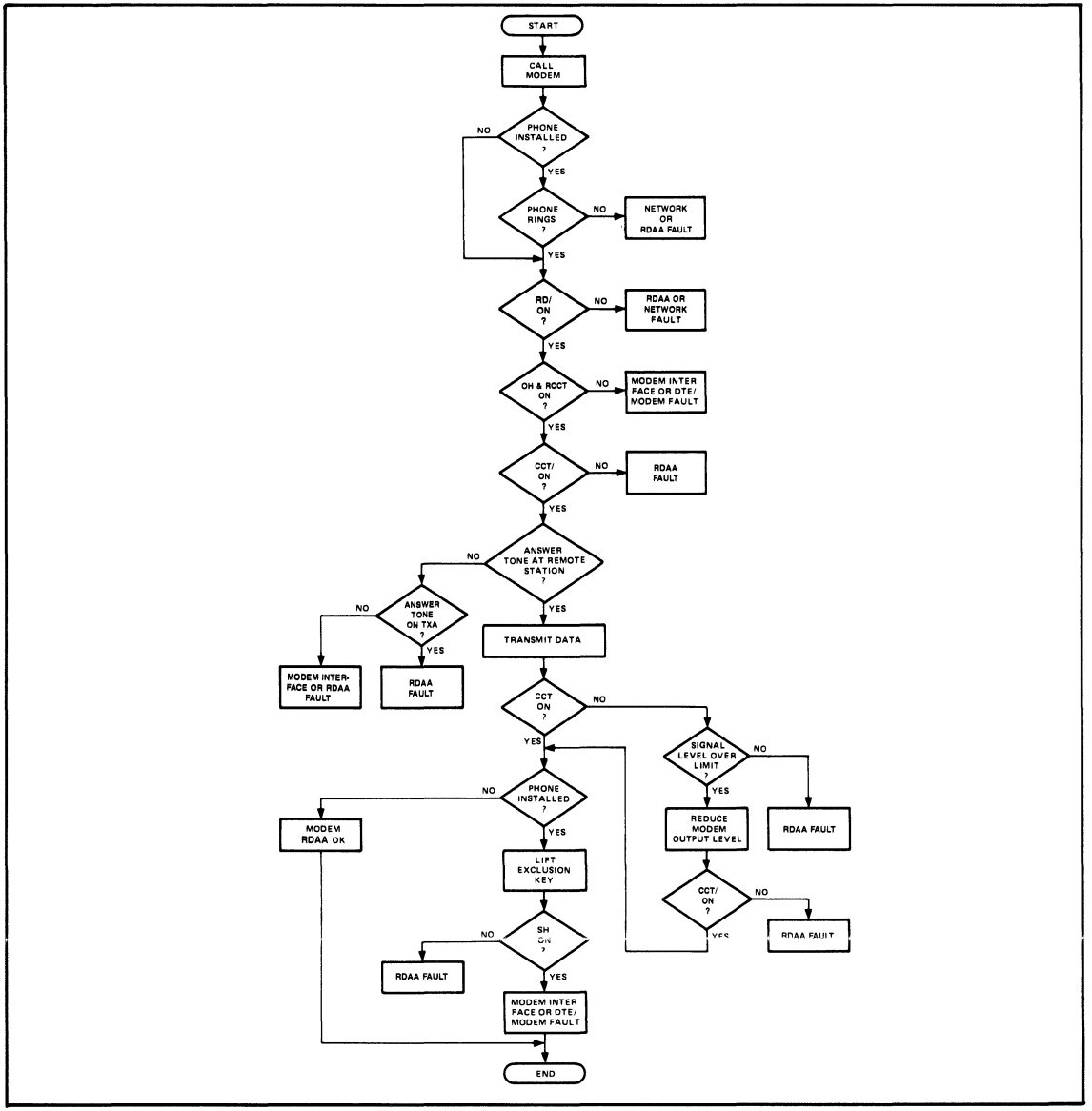


Figure 9. RDAA Fault Isolation Flow Chart

SECTION 8
T-1 AND T-1/CEPT PULSE CODE MODULATION PROTOCOL DEVICES

T-1 AND T-1/CEPT PCM (PULSE CODE MODULATION) PROTOCOL DEVICES Meet AT&T and CCITT Standards

Rockwell International is the first company producing LSI devices for supporting the commercial digital switched network. The 24 or 32 digitized channels meet AT&T and CCITT standards.

This means it is now possible to design T-1/CEPT systems using LSI instead of discrete devices. This results in a much lower parts count, lower power requirements, smaller size and significant cost reductions. It also means an increase in reliability.

Using our LSI devices, the 24 or 32 channels of 64K bps information and signaling are multiplexed over a single pair of wires. All data are transmitted serially, along with framing bits, at 1.544 to 2.048M bps. At the receiving end frame, superframe, and channel synchronization is accomplished, with signaling information outputted and the 24 or 32 channels uniquely identifiable.

Transmission in digital format instead of analog has inherent ability to perfectly regenerate the signal even after noise in the phone network. The TTL compatible devices operate from a single 5V power supply.

For specialized memory for digital PBX and other telecommunication applications, tri-port memory devices are also available. These allow random read and sequential read simultaneously, and, allow addressing sequentially or randomly. They support either time or space division switching as well as elastic storage applications when transmission and write speeds differ.

Rockwell LSI Devices Provide—

- **Parts Count Reduction**
- **Cabling Reduction**
- **Cost Reduction**
- **Increased Reliability**
- **Increased Performance**

Rockwell

R8040
T-1 TRI-PORT MEMORY

OVERVIEW

The Tri-Port Memory circuit is designed to function as an assembly point and temporary storage area for 8-bit T-1 data. It provides 64 8-bit locations of on-chip random access memory which can be accessed via external addresses or internal sequential addressing.

FEATURES

- 64 × 8 bit static memory
- Single +5V supply
- Two totally independent read ports
- Multiple Read access time < 430 ns (worst case)
- Selectable random- or sequential-address Write operation
- On-chip sequential address counter
- Tri-state drivers, for chip-selectable bus operation
- 40-pin plastic dual in-line package
- LSTTL Schottky-compatible (12KΩ pullup, to drive CMOS)

APPLICATIONS

Time-Division Multiplex (TDM) digital switching data and control stores

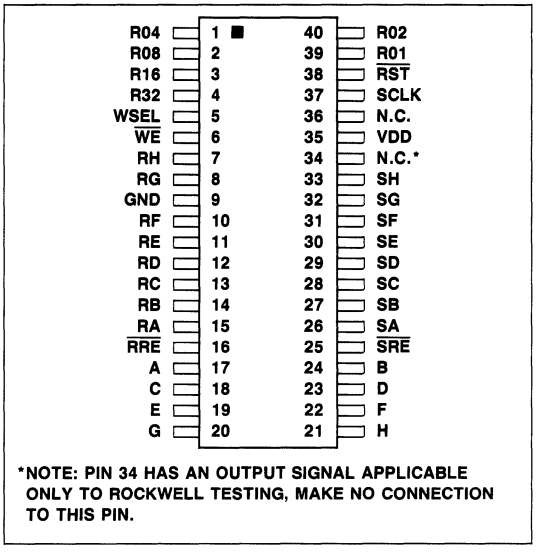
- TDM sequential machines
- Elastic stores
- Hardware/Software control interfaces
- I/O Buffers

TRI-PORT MEMORY OPERATION

The Tri-Port Memory device accepts 8-bit parallel input data on lines A through H. This data is stored in an internal memory location that is selected by either random address lines R01 through R32 or by the device's Sequential Address Counter. Write Select signal WSEL determines the source of the address; in the logic 0 state, WSEL selects the random address, in the logic 1 state, WSEL selects the internal sequential address.

The state of Write Enable signal $\overline{WE}$ determines whether or not the data on lines A through H will be written into memory. Data will only be written into memory when $\overline{WE}$ goes low (to a logic 0 state) and the address inputs have stabilized.

The on-chip, six-bit Sequential Address Counter is a binary counter that increments on each positive transition of Sequential Clock (SCLK). When the Counter attains binary 111111, the next positive transition on SCLK will clear it to binary 000000. The Counter will also be cleared unconditionally if Reset signal $\overline{RST}$ has been set to logic 0 when the positive transition of SCLK occurs.



*NOTE: PIN 34 HAS AN OUTPUT SIGNAL APPLICABLE ONLY TO ROCKWELL TESTING, MAKE NO CONNECTION TO THIS PIN.

Pin Configuration

The Sequential Read Enable signal, $\overline{SRE}$, enables sequentially-addressed read operations. If $\overline{SRE}$ is logic 0, the sequential accessed data outputs (SA through SH) will become valid within 430 ns after the next positive transition on SCLK. If $\overline{SRE}$ is logic 1, and 350 ns have elapsed since the positive transition of SCLK, the sequential accessed data outputs will become valid 80 ns after the negative transition of $\overline{SRE}$. The sequential read data will cease to be valid 100 ns after the negative transition of $\overline{SRE}$ or 20 ns after the next positive transition of SCLK, becoming valid with the content of the next sequential location within 430 ns of that SCLK transition.

The Random Read Enable signal, $\overline{RRE}$, enables random-accessed read operations. If $\overline{RRE}$ is logic 0, the random accessed data outputs (RA through RH) will become valid within 380 ns after the random address lines have stabilized. If $\overline{RRE}$ is logic 1, and 300 ns have elapsed since the random address lines have stabilized, the random accessed data outputs will

8

become valid 80 ns after the negative transition of $\overline{RRE}$. The random accessed data outputs will cease to be valid 100 ns after a positive transition of $\overline{RRE}$ or 20 ns after the random address input lines change, becoming valid with the contents of the newly-addressed location within 380 ns after the random address inputs have stabilized.

In the case of a same location read/write cycle, the sequential and/or random data outputs will cease to be valid after a negative transition of $\overline{WE}$, and will become valid with the newly-written contents within 340 ns of that transition. Control of this parameter minimizes external circuitry required for resolution of read-write contention.

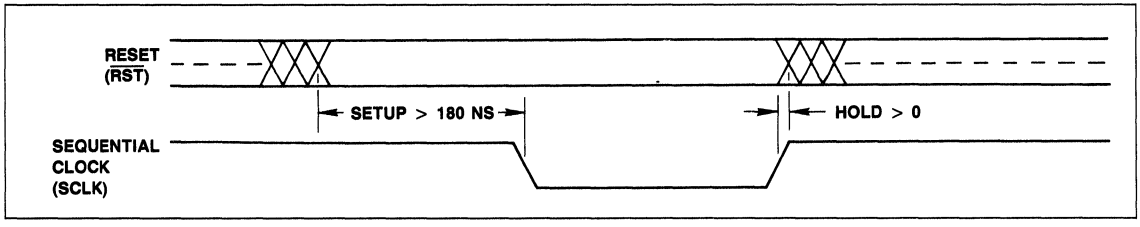
RECOMMENDED OPERATING CONDITIONS

Minimum Setup/Hold Times

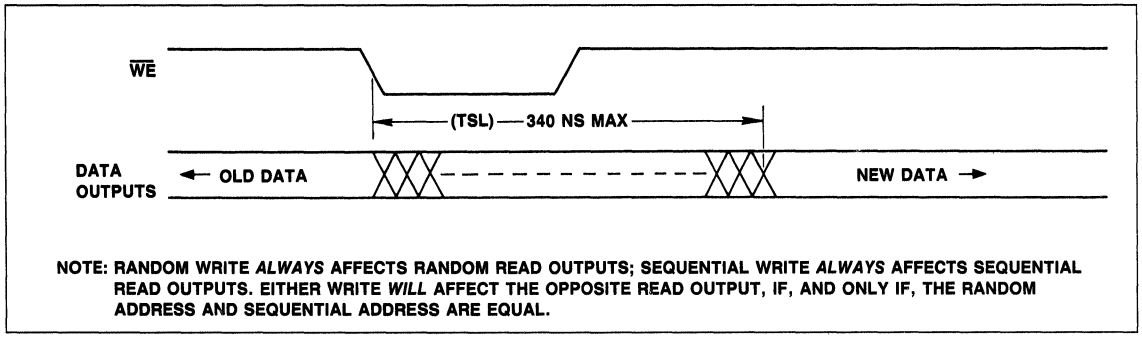
Signal	Setup		Hold	
	Measure to	ns	Measure to	ns
SCLK ↑	$\overline{WE}$ ↓	300	$\overline{WE}$ ↑	0
WSEL	$\overline{WE}$ ↓	280	$\overline{WE}$ ↑	0
R01-R32	$\overline{WE}$ ↓	250	$\overline{WE}$ ↑	0
A-H	$\overline{WE}$ ↑	150	$\overline{WE}$ ↑	100
$\overline{RST}$	SCLK ↓	180	SCLK ↑	0

Minimum Pulse Widths

Signal	Minimum Pulse Width
$\overline{WE}$ (= 0)	170 ns
SCLK	220 ns

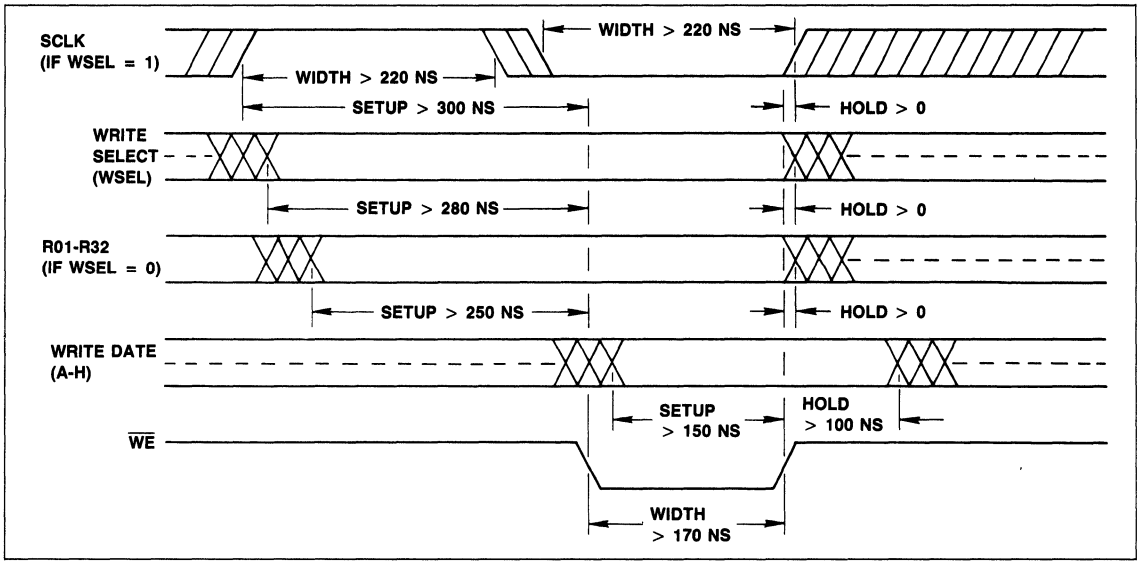


Sequential Counter Reset Setup and Hold Timing

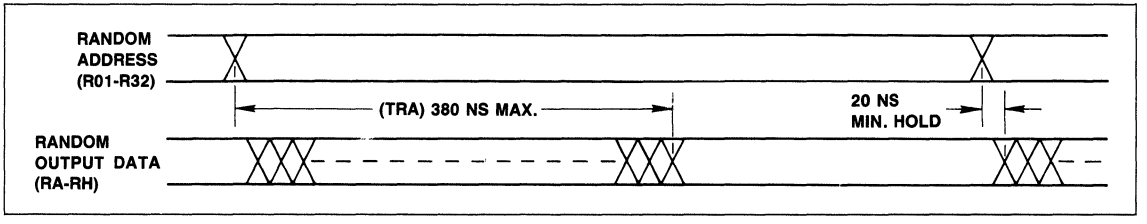


NOTE: RANDOM WRITE *ALWAYS* AFFECTS RANDOM READ OUTPUTS; SEQUENTIAL WRITE *ALWAYS* AFFECTS SEQUENTIAL READ OUTPUTS. EITHER WRITE *WILL* AFFECT THE OPPOSITE READ OUTPUT, IF, AND ONLY IF, THE RANDOM ADDRESS AND SEQUENTIAL ADDRESS ARE EQUAL.

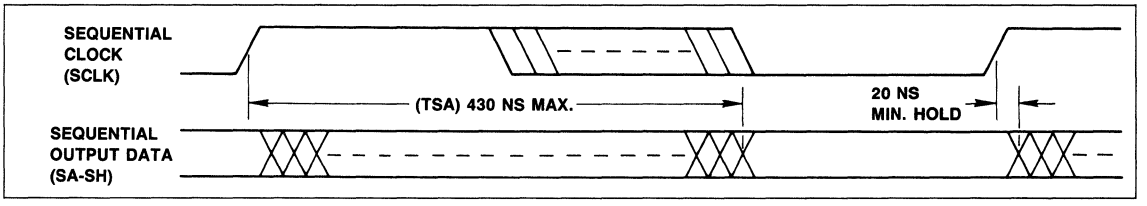
Read Outputs at Same Location as Write (All Other Inputs Stable)



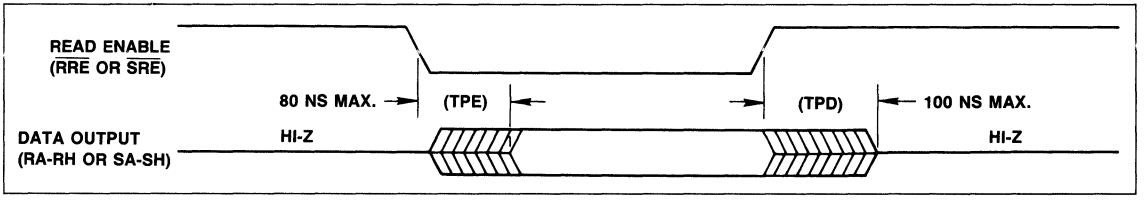
Write Setup and Hold Timing



Random Read ($\overline{RRE}$ = 0, $\overline{WE}$ = 1)



Sequential Read ($\overline{SRE}$ = 0, $\overline{WE}$ = 1)

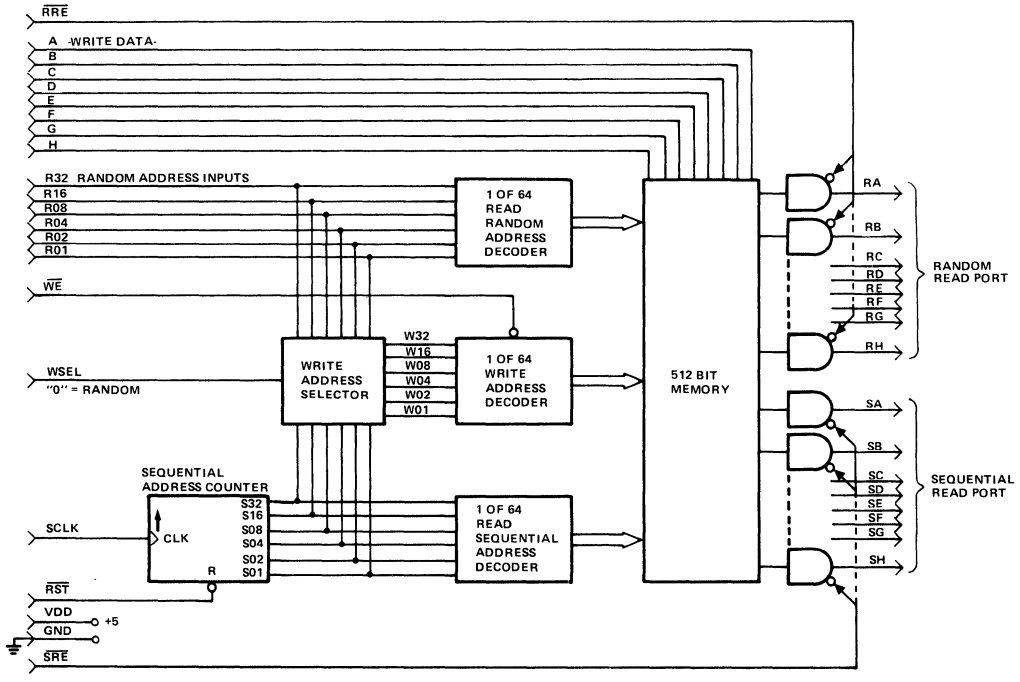


Read Port Enable/Disable (Address Stable, $\overline{WE}$ = 1)

8

Propagation Delays

Parameter	Symbol	Min	Max	Unit
Random Read Access Time	t_{RA}	0	380	ns
Sequential Read Access Time	t_{SA}	0	430	ns
Read Port Disable (to HI-Z)	t_{PD}	0	100	ns
Read Port Enable	t_{PE}	0	80	ns
Same-Location Read After Write	t_{SL}	0	340	ns



Tri-Port Memory Block Diagram

MAXIMUM RATINGS*

Parameter	Symbol	Value	Unit
Supply Voltage	V_{DD}	+4.75 to +5.25	V
Operating Temperature	T_{OP}	0 to +70	°C
Storage Temperature	T_{STG}	−55 to +150	°C

***NOTE:** Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in other sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

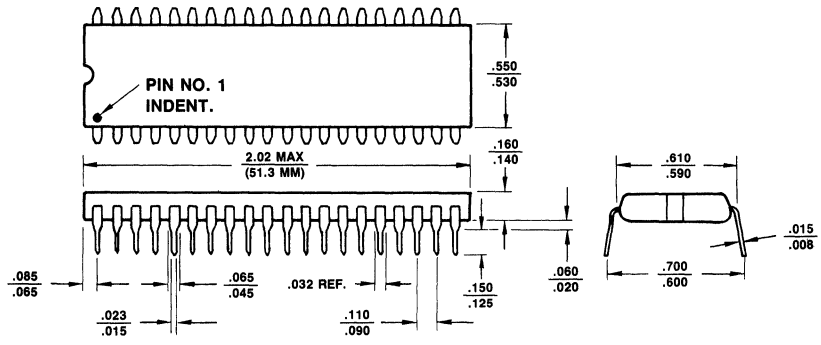
ELECTRICAL CHARACTERISTICS

(V_{DD} = +5V ±5%, V_{SS} = 0V T_A = 25°C)

Parameter	Symbol	Min	Max	Unit
Input Logic "1" Voltage	V_{IH}	2.0		V
Input Logic "0" Voltage	V_{IL}		0.8	V
Input Logic "1" Voltage	V_{OL}	2.4		V
Output Logic "0" Voltage	V_{OL}		0.4	V
Output Source Current	I_{OH}	−100		μA
Output Sink Current	I_{OL}	400		μA
Input Capacitance	C_I		5	pF
Output Capacitance	C_O		25	pF
Power Dissipation (at 25°C)	P_{DSS}		300	mW

8

PACKAGE DIMENSIONS



NOTE: PIN NO. 1 IS IN LOWER LEFT CORNER WHEN SYMBOLIZATION IS IN NORMAL ORIENTATION

Rockwell

R8050
T-1 SERIAL TRANSMITTER

DESCRIPTION

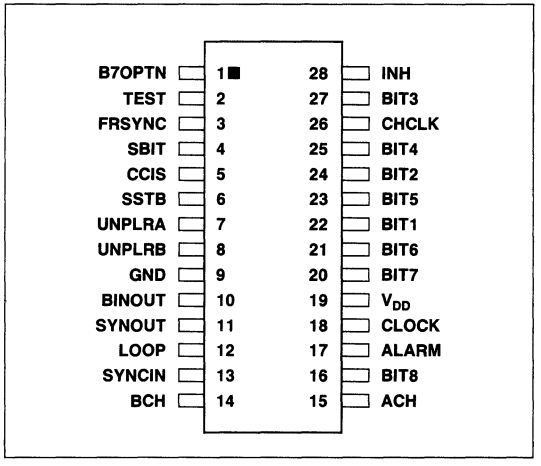
The Rockwell T-1 Serial Transmitter formats data to be serially transmitted according to T-1 D2 or T-1 D3 specifications, inserting framing and signalling bits along with 24 channels of 8-bit channel data. The T-1 Serial Transmitter also provides for alarm reporting via the Bit 2 inhibit method or, with minimal external logic, via the multiframe alignment signal (F_S) modification method.

Figure 1 is a functional block diagram of the T-1 Serial Transmitter. The Mod 193 counter is driven by the clock at 1.544 MHz and is either synchronized to the driving system by input signal SYNCIN or provides synchronization via output signal SYNOUT. Input signal FRSYNC applies synchronization to a Mod 12 counter, which identifies the frame of the 12-frame multiframe being processed.

The input data register latches data during each bit period, when the 8th bit of a channel sample is being transmitted. The data selector outputs the proper sequence of bits, as controlled by a bit count and frame count.

The zero channel monitor function causes Bit 8 or Bit 7 to be transmitted as a "one" if the channel data sample is all "zeros." Input INH provides a means to inhibit the zero channel monitor function. Input B7OPTN controls the particulars of the insertion method.

Two types of transmit formats are provided, a binary output and a paired unipolar output. The unipolar pair provides a means to externally create a single bipolar output with minimal logic.



Pin Configuration

FEATURES

- Single 5V supply, low power Schottky TTL compatible.
- Accepts 8 bits of parallel data as input.
- Generates output as 193 bit serial data stream in T-1, D2, D3 or D4 Mode 3 data format.
- Provides a channel and frame timing signal.
- Provides alternate control for alarm reporting and signalling.
- Provides automatic bit insertion for all-zero channel samples.

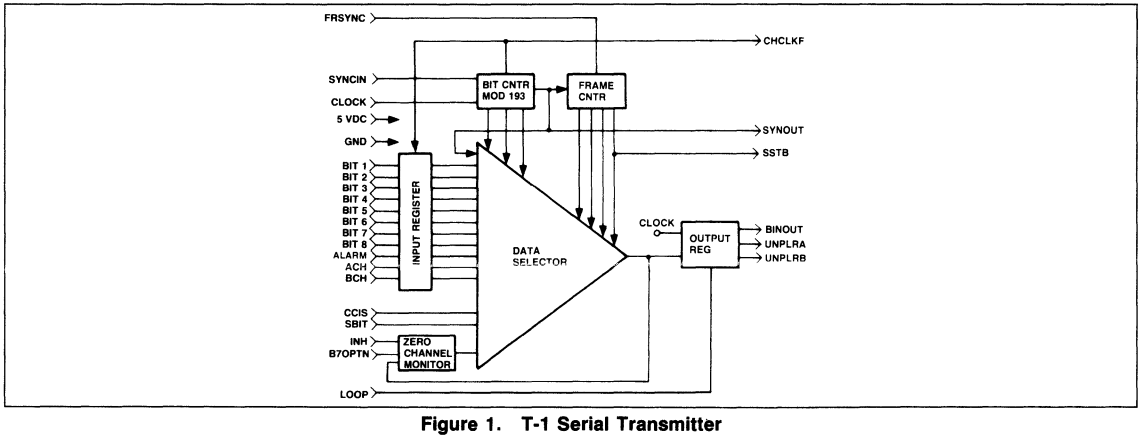


Figure 1. T-1 Serial Transmitter

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T-1 TRANSMITTER INPUTS

Any input ≤0.8V = logic 0, low. Any input ≥2.0V = logic 1, high. The transition from a low level to a high level is called a rising edge, while the converse is defined as a falling edge.

FRSYNC: FRAME SYNCHRONIZATION

Frame sync allows external synchronization of the transmitter's internal frame counter. When FRSYNC becomes high, the frame counter is directly set to frame 1, the first of the twelve frames. If FRYSYNC is held high and does not return to zero before a rising edge of CLOCK, the subsequent states of BINOUT, UNPLRA and UNPLRB are high, high and low, respectively, regardless of the states of any other inputs. The latter mechanism is useful for device and/or board testing only and will cause bit errors and/or bipolar violations if used during field operations. See Figures 6 and 7.

SYNCIN: SYNCHRONIZATION INPUT

SYNCIN allows external synchronization of the internal Modulo 193 bit/channel counter. When SYNCIN becomes high, the Modulo 193 counter is directly set to the state corresponding to the output of the framing (F_T or F_S) bit. The first bit of channel one will be output on BINOUT (and UNPLRA or UNPLRB) as a result of the first rising edge of CLOCK following the return of SYNCIN to logic 0. See Figures 5 and 7.

TEST: ROCKWELL DEVICE TEST INPUT

Used only for Rockwell device testing. **Keep this input grounded.**

CLOCK: T-1 CLOCK

Maximum frequency = 1.6 MHz
Minimum pulse width = 275 ns
The T-1 bit period is bounded by the rising edges of this input.

INH: INHIBIT ZERO CHANNEL MONITOR

If INH is high, the zero channel monitor function is disabled, and Bits 7 and 8 are transmitted per corresponding inputs received. See Table 1.

For channels in signalling frames (6 or 12) in which the first six data bits and the signalling highway are all "zero," BIT 7 will be forced to one if INH is low. For any frame except a signalling frame Bit 8 or Bit 7 as selected by B7OPTN will be transmitted as a "one" if the channel input data is "zero" and INH is low.

BITS 1-8: PARALLEL CHANNEL DATA INPUTS

Bit 1, the sign bit, will be serially transmitted first, followed by Bits 2 through 8. The falling edge of CHCLKF indicates input channel data has been clocked into the input register and always occurs during the transmission of the final bit (Bit 8) of each channel data sample.

ACH: "A" CHANNEL HIGHWAY SIGNALLING

ACH allows the user to transmit one bit of signalling per channel as Bit 8 of each channel data sample in Frame 6 only. ACH is clocked into the input register by the falling edge of CHCLKF. Refer to Table 1 and Figure 4.

BCH: "B" CHANNEL HIGHWAY SIGNALLING

BCH allows the user to transmit one bit of signalling per channel as Bit 8 of each channel data sample in Frame 12 only. BCH is clocked into the input register by the falling edge of CHCLKF. Refer to Table 1 and Figure 4.

S-BIT: MULTIFRAME SIGNALLING BIT

SBIT, in conjunction with CCIS, provides an alternate way to control the multiframe signalling bit (F_S) transmission. The S-Bit input is transmitted as the multiframe signalling bit (F_S) if CCIS is held high. Refer to Table 2.

ALARM: LOCAL ALARM

Used for reporting alarm conditions. If the ALARM signal is high, Bit 2 (the most-significant bit) of every channel data sample of every frame is transmitting as a zero. This is commonly called remote alarm signalling. ALARM is clocked into the input register at the falling edge of CHCLKF. Refer to Table 1 and Figure 4.

LOOP: LOOP STRAP

Provided to aid testing of user applications. When enabled to a high level, LOOP forces the unipolar outputs to transmit alternating ones and zeros, regardless of input conditions, while BINOUT continues to provide normal data outputs. Refer to Figure 3.

CCIS: COMMON CHANNEL INTEROFFICE SIGNALLING STRAP

Provides optional control for replacing the automatic F_S pattern with a 4-kilobit common channel signalling path. When CCIS is high, the SBIT input replaces the F_S pattern and the insertion of ACH and BCH is suspended. The CCIS input may also be used to provide the alternate method of alarm reporting. See Figure 4.

B7OPTN: BIT 7 OPTION

Provides Bit 7 as an alternate bit position for "one" stuffing, as programmed by the zero channel monitor function. Refer to Table 1.

VSS, VDD: GROUND AND POWER

V_{DD} = +5 ±0.25 Vdc
V_{SS} = Ground, 0 Vdc

T-1 TRANSMITTER OUTPUTS

Low power TTL Schottky compatible. "1" ≥ 2.4 Vdc, "0" ≤ 0.4 Vdc, CMOS — 12KΩ pullup to V_{DD} required.

SSTB: 4 kHz SIGNALLING CHANNEL STROBE

SSTB is the least-significant bit of the frame counter. Unless it is directly set by FRSYNC, SSTB will go high as each framing bit (F_T) is serially transmitted, and will return low as each multiframe alignment signal (F_S) is transmitted. Refer to Figure 2.

SYNOUT: CHANNEL SYNC OUTPUT

SYNOUT provides a means to synchronize to the internal bit counter (Mod 193). SYNOUT is high for one bit time, beginning just prior to the first data bit of a frame being serially transmitted. Refer to Figure 7. SYNOUT is the only output determined by the falling edge of CLOCK.

CHCLKF: CHANNEL CLOCK FALSE

The falling edge of CHCLKF, occurring as Bit 8 of any channel is being serially transmitted, indicates input data has been clocked into the input register. With the exception of an extra bit period extending the low level duration at frame bit time, CHCLKF is a divide-by-eight of CLOCK. Refer to Figure 2.

BINOUT: SERIAL DATA OUTPUT, BINARY FORMATTED

BINOUT is the binary formatted serial conversion of the parallel input data. The programmed format of BINOUT follows Tables 1 and 2.

BINOUT is synchronously transmitted as a high level if FRSYNC remains high during the rising edge of CLOCK. Refer to Figures 6 and 7.

UNPLRA, UNPLRB: T-1 SERIAL DATA UNIPOLAR OUTPUTS

Two paired unipolar outputs are provided for the purpose of creating a single serial data output transmission in bipolar format. The unipolar output register toggles for each "one" bit to be serially transmitted. UNPLRA and UNPLRB are transmitted as complements for "one" data bits and as low levels for "zero" data bits. See Figure 3.

The input signal LOOP, if high, forces the unipolar outputs to toggle every bit time, regardless of input data.

FRSYNC perturbs the current bits being transmitted by UNPLRA and UNPLRB. If FRSYNC remains high during the rising edge of CLOCK, UNPLRA will be transmitted as a high level and UNPLRB will be low. Refer to Figures 6 and 7.

Table 1. Serial Channel Sample Output Data Truth Table

Inputs X = don't care													Current Frame Number	Binout Serial Output Channel Bit Position								Notes
ALARM	INH	B7OPTN	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7	BIT 8	ACH	BCH		1	2	3	4	5	6	7	8	
1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0	X	X	X	X	X	X	1
X	X	X	X	0	X	X	X	X	X	X	X	X	X	X	0	X	X	X	X	X	X	1
0	X	X	P	Q	R	S	T	U	V	X	A	X	6	P	Q	R	S	T	U	V	A	2
0	X	X	P	Q	R	S	T	U	V	X	X	B	12	P	Q	R	S	T	U	V	B	2
0	X	X	P	Q	R	S	T	U	V	W	X	X	Y	P	Q	R	S	T	U	V	W	2,3
0	1	X	0	0	0	0	0	0	0	X	A	X	6	0	0	0	0	0	0	0	A	
0	1	X	0	0	0	0	0	0	0	X	X	B	12	0	0	0	0	0	0	0	B	
0	1	X	0	0	0	0	0	0	0	W	X	X	Y	0	0	0	0	0	0	0	W	3
0	0	X	0	0	0	0	0	0	0	X	0	X	6	0	0	0	0	0	0	1	0	
0	0	X	0	0	0	0	0	0	0	X	X	0	12	0	0	0	0	0	0	1	0	
0	0	1	0	0	0	0	0	0	0	0	X	X	Y	0	0	0	0	0	0	1	0	3
0	0	0	0	0	0	0	0	0	0	0	X	X	Y	0	0	0	0	0	0	0	1	3

NOTES (1) ALARM = 1 has the same effect as BIT 2 = 0
(2) P, Q, R, S, T, U and V may not simultaneously be zero, unles A, B or W is 1
(3) Y is any frame $\neq$ 6 and $\neq$ 12 with CCIS = 0, or all frames with CCIS = 1

8

Table 2. Framing Bit (F_T & F_S) Output Data

Frame Number	Processed Bit	Binout	
		CCIS = 0	CCIS = 1
1	F_T	1	1
2	F_S	0	SBIT
3	F_T	0	0
4	F_S	0	SBIT
5	F_T	1	1
6	F_S	1	SBIT
7	F_T	0	0
8	F_S	1	SBIT
9	F_T	1	1
10	F_S	1	SBIT
11	F_T	0	0
12	F_S	0 (NOTE 1)	SBIT

Notes: (1) Alternate remote alarm reporting may be accomplished by holding SBIT and CCIS both high just prior to initiation of Frame 12.
(2) F_T bit insertion is automatic and no optional control is provided.

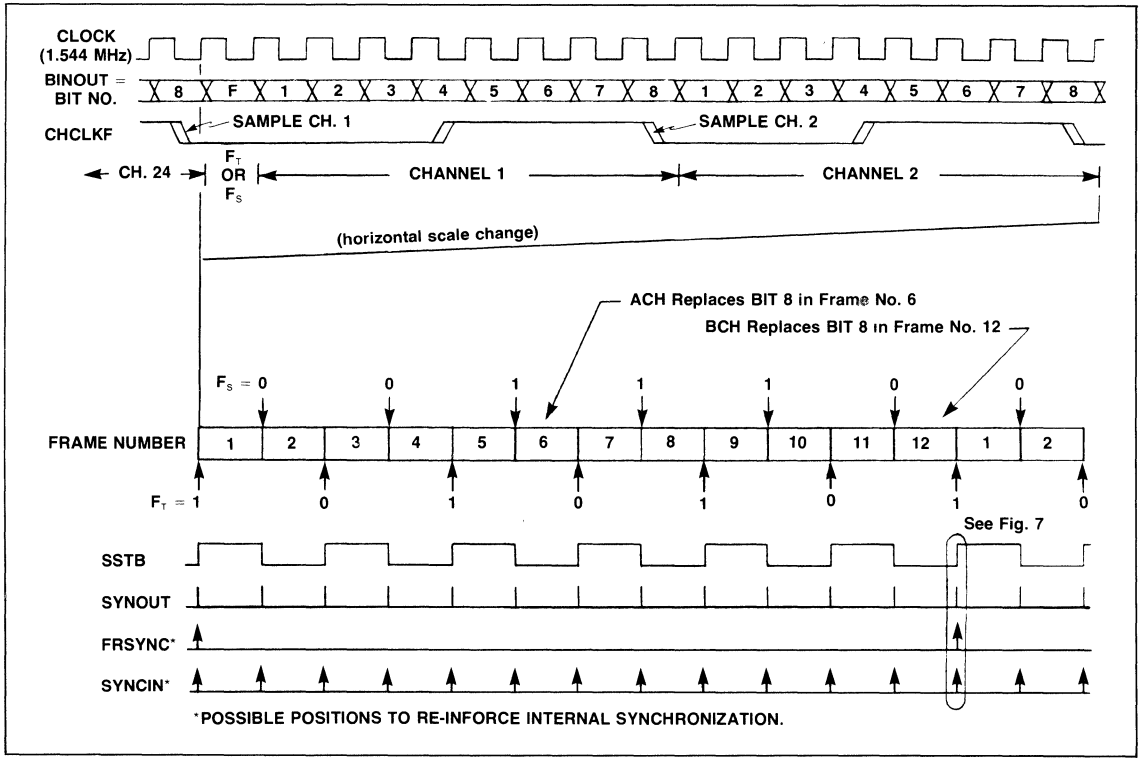


Figure 2. Transmitter Input-Output Signal Relationships

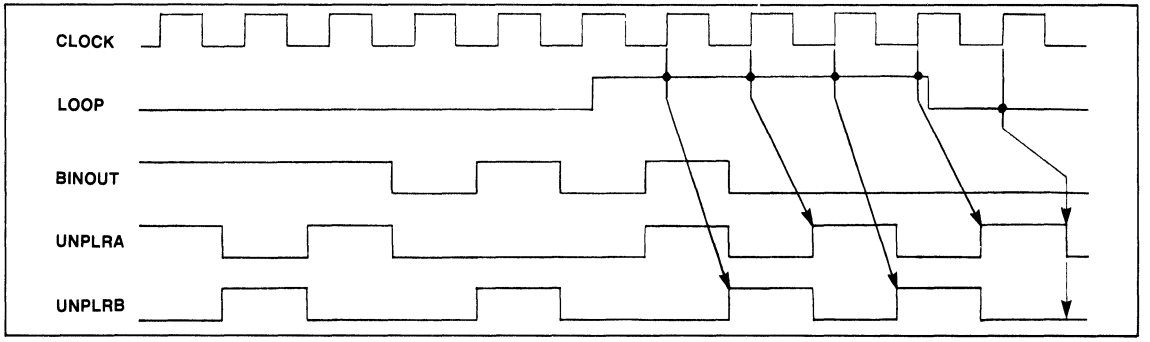


Figure 3. Transmitter Binary, Unipolar Outputs

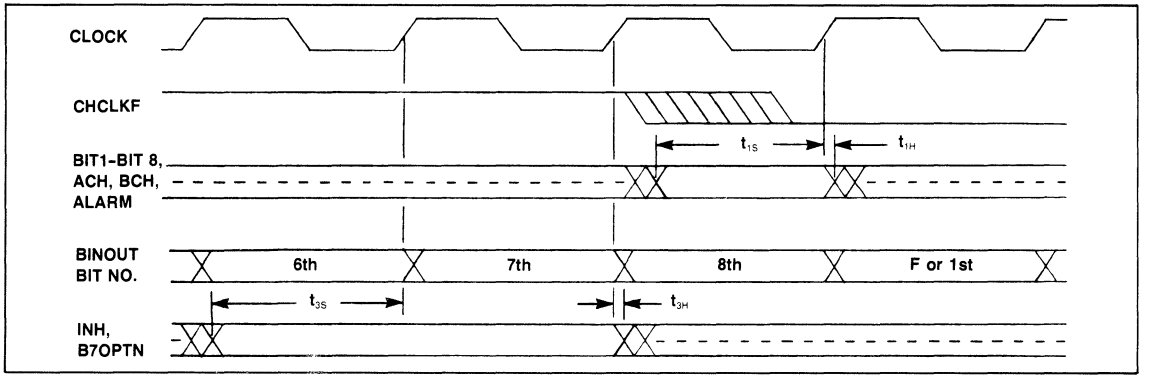


Figure 4 (a). Channel Input Timing

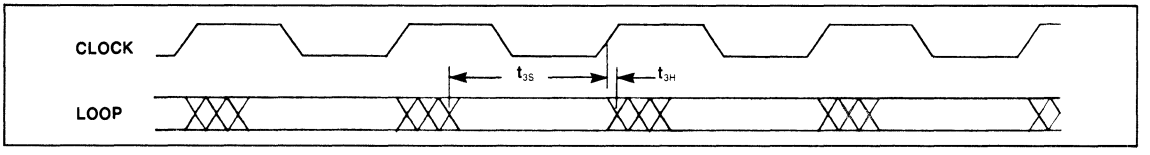
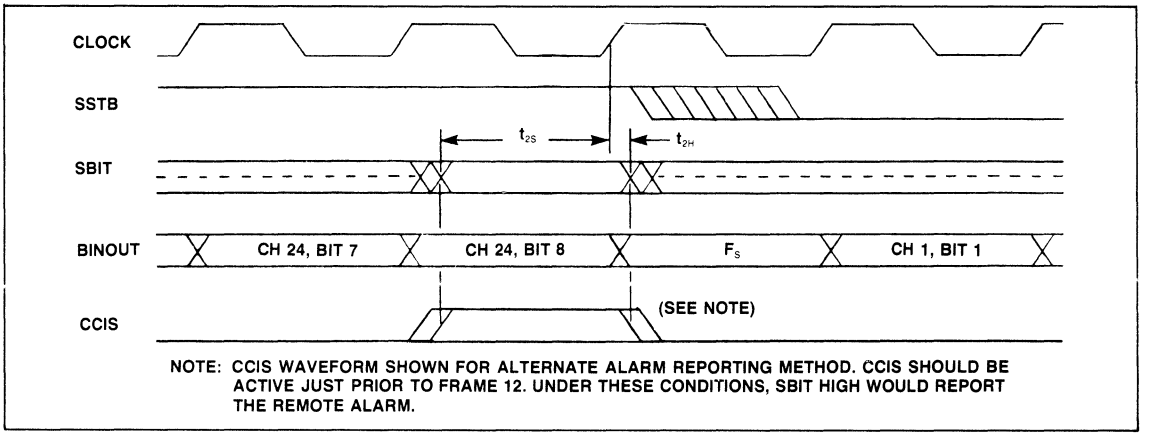


Figure 4 (b). LOOP Input Timing



NOTE: CCIS WAVEFORM SHOWN FOR ALTERNATE ALARM REPORTING METHOD. CCIS SHOULD BE ACTIVE JUST PRIOR TO FRAME 12. UNDER THESE CONDITIONS, SBIT HIGH WOULD REPORT THE REMOTE ALARM.

Figure 4 (c). Control Input Timing

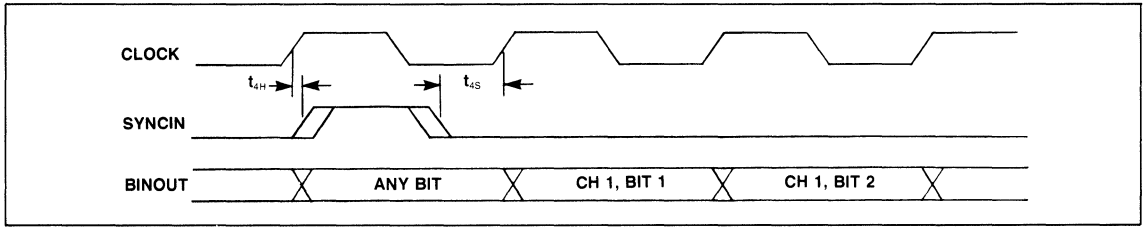


Figure 5. SYNCIN Timing Relationship

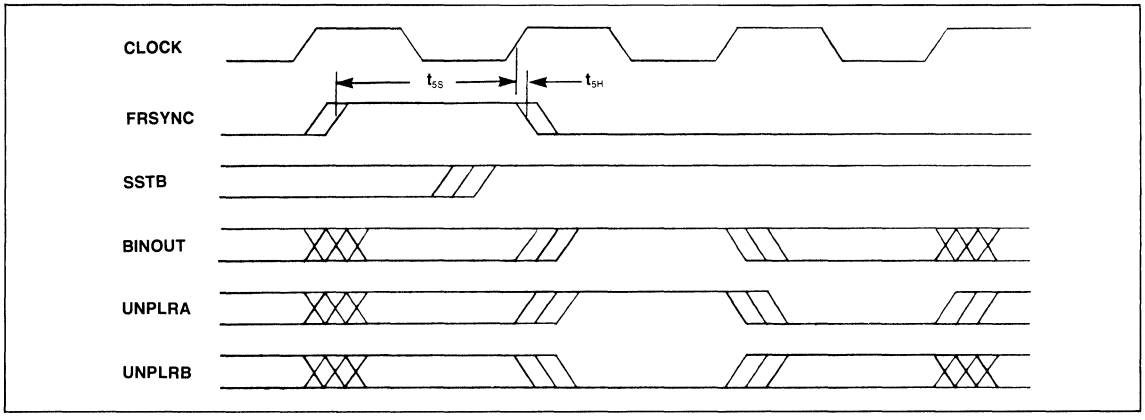


Figure 6. Non-return-to-zero FRSYNC Timing

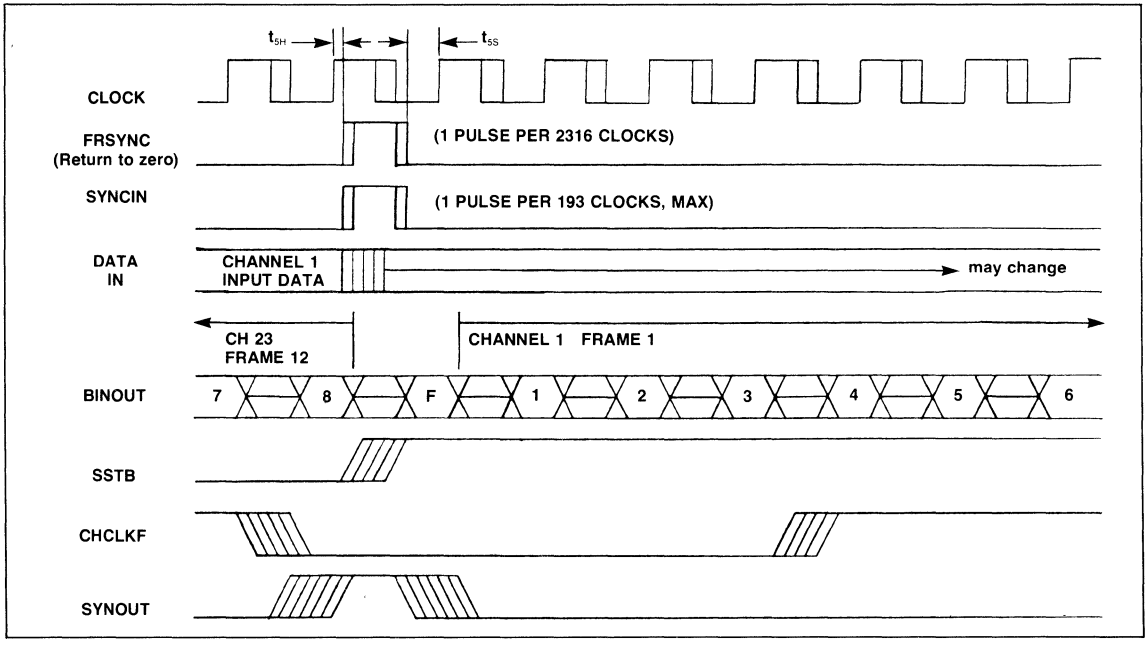


Figure 7. Transmitter External Synchronization (Return-to-zero FRSYNC)

Table 3. Input Timing

Symbol	Parameter	Min	Max	Unit
t_{1S}	Buffered Data Setup Time	450		ns
t_{1H}	Buffered Data Hold Time	0		ns
t_{2S}	Control Input Setup Time	400		ns
t_{2H}	Control Input Hold Time	20		ns
t_{3S}	Asynchronous Control Input Setup Time	350		ns
t_{3H}	Asynchronous Control Input Hold Time	20		ns
t_{4S}	SYNCIN Setup Time	200		ns
t_{4H}	SYNCIN Hold Time	20		ns
	SYNCIN Pulse Width	100		ns
t_{5S}	Frame Sync Setup Time (Return to Zero)	250		ns
t_{5H}	Frame Sync Hold Time (Return to Zero)	20		ns
	Frame Sync Pulse Width	200		ns
t_{5S}	Frame Sync Setup Time (Non-Return to Zero)	525		ns
t_{5H}	Frame Sync Hold Time (Non-Return to Zero)	20		ns

Table 4. Output Propagation Delay, Worst Case
(Measured from Rising Edge of Clock Unless Stated Otherwise)

Output	Max Delay	Unit
SSTB	500	ns
SYNOUT	500	ns
Ref from Falling Edge of Clock		
CHCLKF	500	ns
BINOUT	500	ns
UNPLRA	500	ns
UNPLRB	500	ns

MAXIMUM RATINGS*

Parameter	Symbol	Value	Unit
Supply Voltage	V_{DD}	+4.75 to +5.25	Vdc
Operating Temperature	T_{OP}	0 to 70	°C
Storage Temperature	T_{STG}	−55 to +150	°C

***NOTE:** Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in other sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

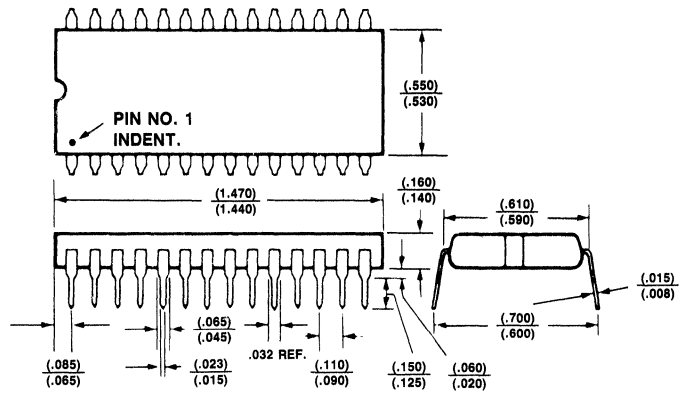
ELECTRICAL CHARACTERISTICS

(V_{DD} = 5.0 ±5%)

Parameter	Symbol	Min	Max	Unit
Logical "1" Input Voltage	V_{OH}	2 0	V_{DD} + 0 3	V
Logicical "0" Input Voltage	V_{IL}	−0 3	0.8	V
Logicical "1" Output Voltage	V_{OH}	2 4	—	V
Logic "0" Output Voltage	V_{OL}	—	0 4	V
Output Source Current	I_{OH}	−100	—	μA
Output Sink Current	I_{OL}	400	—	μA
Capacitance Load (any output)	C	—	25	pF
Input Capacitance (any input)	C_{IN}	—	5	pF
Clock Frequency		—	1.6	MHz
Power Dissipation	P_D	—	250	mW

8

PACKAGE DIMENSIONS



Rockwell

R8060
T-1 SERIAL RECEIVER

DESCRIPTION

The Rockwell T-1 Receiver processes serial unipolar data of a T-1,D2 or T-1,D3 line from which data and a 1.544 MHz clock have been extracted.

Frame synchronization is accomplished by locating the frame bit (F_T) alternating every 386 bits. Loss of frame sync is indicated if a frame bit error occurs within two to four F-Bit frames since the previous frame bit error.

A loss of carrier is indicated if 31 consecutive bit times yield "zeros" at the input. Carrier loss is reset and frame sync search begins when a "one" reappears at the TDATA input.

Signaling bits, which occur 193 bit positions after a framing bit, are monitored to detect signaling frames. The signaling frame output, SIGFR, identifies the present frame as a signaling frame, and the S-Bit output at that time identifies which signaling frame is being processed.

Remote alarm reporting is detected by monitoring the second received bit of every channel sample of every frame. An alarm is indicated if 255 consecutive Bit 2 zeros are received.

Channel data bits are output by an eight-bit parallel register. The rising edge of the signal called channel clock (CHCLK) indicates the extraction of new output channel data.

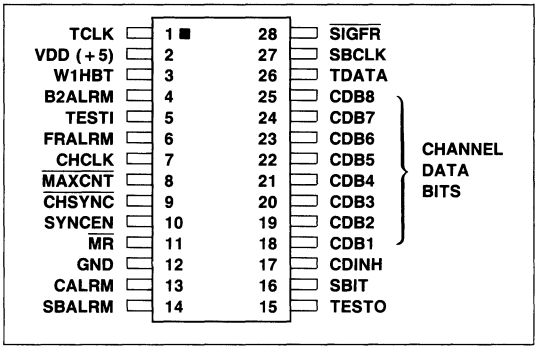
Several signals developed from a MOD 386 counter are provided to aid in the external processing and storage of channel data. Signals are provided to increment counters, synchronize counters, strobe data into memories, etc.

The Rockwell T-1 Receiver chip operates on a single 5 volt supply and directly interfaces to the low power TTL Schottky logic family. The Receiver is packaged in a 28 pin dual in-line (DIP).

Timing relationships are given in figures 3 through 5.

FEATURES

- Synchronizes serial T-1,D2 or T-1,D3 signals in less than 5 ms.
- Extracts 8-bit parallel channel data
- Provides timing signals to capture and synchronize channel and frame information
- Monitors and detects
  - — Errors in signaling bit pattern
  - — Loss of frame sync
  - — Loss of carrier
  - — Remote alarm reporting
- Single 5V supply
- LSTTL Schottky compatible



Pin Configuration

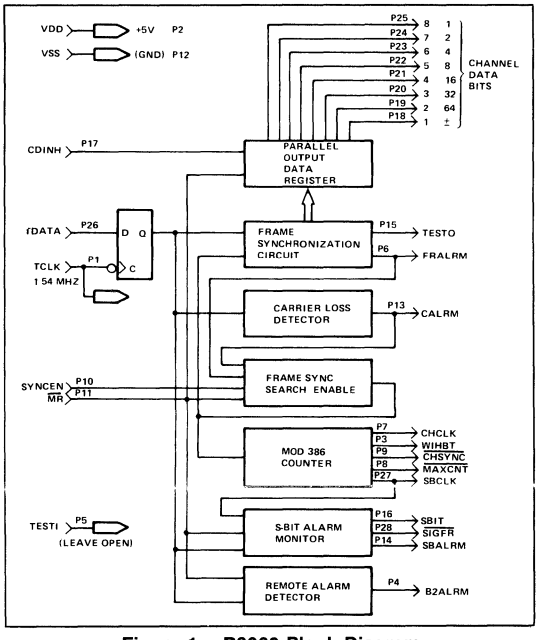


Figure 1. R8060 Block Diagram

8

T-1 RECEIVER INPUTS

Any input ≤0.8V = LOGIC 0, LOW, ZERO. Any input ≥2.0V = LOGIC 1, HIGH, ONE. A transition from a low level to a high level is called a rising edge, while the converse is true for the falling edge.

TDATA: UNIPOLAR T-1-D2, T-1-D3 SERIAL DATA INPUT

Unipolar T-1 Data is clocked in on the falling edge of TCLK. Thereafter, TDATA is processed on the rising edge of TCLK. TDATA must be stable 100 ns before and remain stable 100 ns after the falling edge of TCLK.

TCLK: T-1 CLOCK

Typical clock frequency is 1.544 MHz. Maximum clock frequency is 1.85 MHz. The T-1 bit period is bounded by the rising edges of TCLK. Input levels must be >2.4 volts for LOGIC 1 and ≤0.8 volts for LOGIC 0.

SYNCEN: FRAME SYNCHRONIZATION ENABLE

Provides a means to disable the automatic resync search initiated by a FRAME ALARM condition. If the SYNCEN signal is low, with synchronization function is inhibited and remains inhibited until SYNCEN transitions high. SYNCEN must be stable 200 ns before the rising edge of FRALRM, in order to inhibit the synchronization function.

MR: MASTER RESET

Master Reset, when low performs an initialization clear of the T-1 Receiver; SBALRM and CALRM are reset to low levels while FRALRM, CHCLK, WIHBT and CHSYNC are set to high levels. Frame synchronization search begins on the rising edge of $\overline{MR}$ provided that SYNCEN signal has been high for 200 ns. Minimum pulse width is one T-1 clock period.

CDINH: CHANNEL DATA INHIBIT

Provides a means to disable channel data bit outputs. When at a high level, CDINH forces channel data Bits 1 through 7 high. Bit 8, the least significant channel data bit, is not controlled by CDINH.

TESTI: ROCKWELL DEVICE TEST INPUT

Used only for Rockwell device testing, no connection to TESTI is required for normal operation.

VSS, VDD: GROUND AND POWER

VDD = +5.0 ±0.25 VDC
VSS = Ground, 0 VDC

T-1 RECEIVER OUTPUTS

Low Power TTL Schottky — compatible
"1" ≥ 2.4 Vdc; "0" ≤ 0.4 Vdc
CMOS — 12 K Ω pullup to VDD required.

CDB (1-8): CHANNEL DATA BIT 1 THROUGH 8

Bit 1 is the sign bit, Bit 2 is the most significant bit and Bit 8 is the least significant bit. If CDINH is low, new parallel channel data becomes valid within 200 ns after the rising edge of CHCLK and remains valid until the next rising edge of CHCLK. If CDINH is high, channel data Bits 1 through 7 are forced to a high level. Bit 8, the least significant bit, is not controlled by CDINH. Channel data Bits 1 through 7 are enabled or disabled within 300 ns (R8060) or 150 ns (R8060A) by CDINH. Refer to Figures 3 through 5.

CHCLK — CHANNEL CLOCK

The rising edge of CHCLK indicates a change of parallel output channel data. CHCLK is four TCLKS high then four TCLKS low except for when an "F" or "S" bit is received. Then CHCLK stretches to five TCLKS high and four TCLKS low. Refer to Figures 3 and 4.

$\overline{CHSYNC}$: CHANNEL SYNC

Channel Sync occurs one time in a 24 channel period, making it suitable for synchronizing external counters to the T-1 Frame rate. $\overline{CHSYNC}$ goes low one TCLK period before the falling edge of CHCLK at channel 24 date sample time. $\overline{CHSYNC}$ returns high 1 TCLK period after the next rising edge of CHCLK. Refer to Figures 3 through 5.

TESTO: ROCKWELL DEVICE TEST OUTPUT

Designed to aid in Rockwell device testing. No connection required for normal operation.

WIHBT: WRITE INHIBIT

WIHBT covers the parallel channel data transition period. WIHBT is suitable for clocking or strobing channel data into external memories. WIHBT is high for two TCLK periods, beginning one TCLK period before the rising edge of CHCLK. Refer to Figures 3 and 4.

$\overline{MAXCNT}$: MAXIMUM COUNT OF 386 MODULUS

$\overline{MAXCNT}$ is low for one TCLK period, marking the completion of a two-frame period corresponding to the expected receipt of an F-bit at the TDATA input. Refer to Figures 4 and 5.

SBCLK: S-BIT CLOCK

SBCLK will be high during the S-Bit frame and low during the F-bit frame. The transitions will occur within 300 ns after the rising edge of TCLK as channel 24 data is being transferred to the parallel channel outputs. Refer to Figures 3 through 5.

S-BIT: SIGNALING BIT OUTPUT

The S-Bit output will have the same digital level as the previous S-Bit received which occurred two frames before the receipt of the current S-Bit. An S-Bit output transition occurs one TCLK period after the rising edge of SBCLK.

During a signaling frame (SIGFR is low), frame 6 or "A" highway signaling is identified by S-Bit output being low. If S-Bit is high during a signaling frame, frame 12 or "B" highway signaling is identified. Refer to Figures 3 through 5.

$\overline{\text{SIGFR}}$: SIGNALING FRAME

$\overline{\text{SIGFR}}$ identifies frame 6 or 12 when low. If the sequence of five consecutive received S-Bits is either 0111X or 1X001 (left to right, as received), $\overline{\text{SIGFR}}$ shall go low after the rising edge, but at least 375 ns before the falling edge of WIHBT corresponding to channel 1 data sample time. $\overline{\text{SIGFR}}$ returns high one frame later (193 bits). Refer to Figures 3 through 5.

SBALRM: S-BIT ALARM

SBALRM goes high if the sequence of the five S-Bits received contains four consecutive ones (01111), and remains high until three consecutive "zero" bits are preceded and followed by a "one" S-Bit (10001). The actual transition of SBALRM output occurs after the rising edge, but at least 375 ns before the falling edge of WIHBT corresponding to channel 1 data sample time.

B2ALRM: BIT 2 ALARM

B2ALRM goes high, detecting a remote alarm condition, if 255 consecutive channel data samples are received with Bit 2 low. B2ALRM returns low upon the receipt of any channel sample with Bit 2 high.

CALRM: CARRIER LOSS ALARM

A carrier loss is detected and CALRM is set high if 31 consecutive low level TDATA bits are received. CALRM is reset low, FRALRM is set high and frame sync search begins when the first TDATA high level is received.

FRALRM: FRAME ERROR ALARM

FRALRM detects an out-of-frame condition. FRALRM goes high if:

A) The framing synchronization function is in progress.
B) Within 250 ns after the falling edge of MR.
C) An F-Bit is received which is not the inverse of the last F-Bit and the same condition also occurred two or three or four F-Bit frames earlier.
D) Within 250 ns after the falling edge of CALRM, (CALRM being reset by high level TDATA bit).

FRALRM goes low upon completion of the synchronization function or within 250 ns after the rising edge of CALRM. (Carrier loss condition during frame synchronization function).

OUTPUT CLOCK SIGNALS DURING FRAME SYNCHRONIZATION FUNCTION

Following the Declaration of Frame Sync loss (FRALRM goes high), output signals will continue normally for a two-frame period with the exception of CHSYNC, which has the above mentioned second frame sync pulse inhibited. Following the two-frame period CHCLK, CHSYNC, and WIHBT are held high until frame sync has been located, as indicated by the falling edge of FRALRM. With typical data patterns, frame synchronization takes less than five milliseconds. See Figure 2.

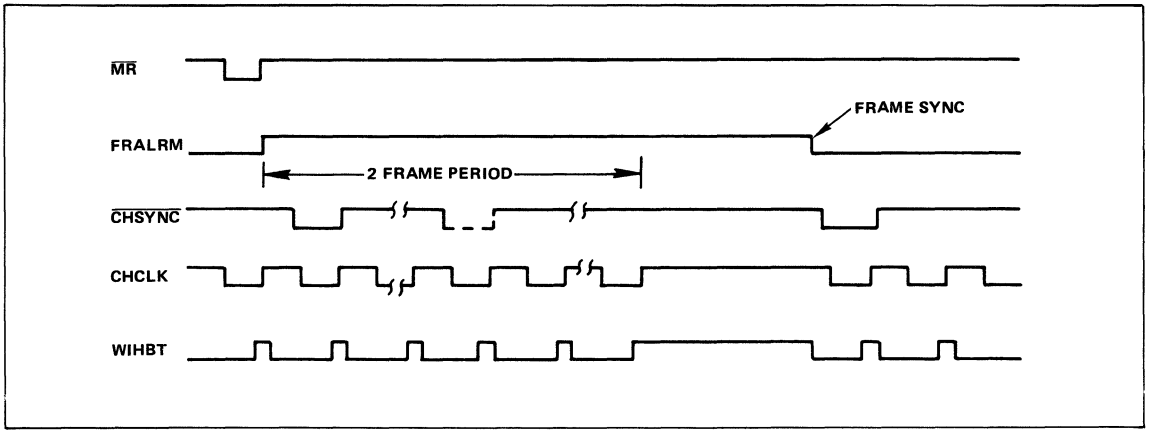


Figure 2. Signal Relationship During Frame Alarm and Search for Resynchronization

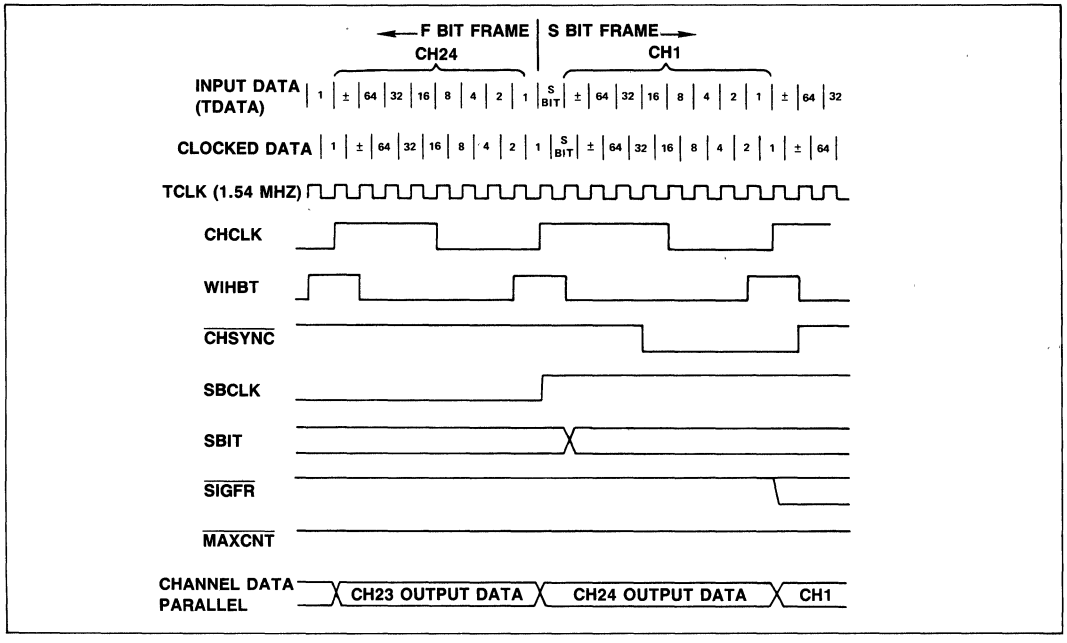


Figure 3. Signal Relationships at Beginning of F_S Frame (S-BIT)

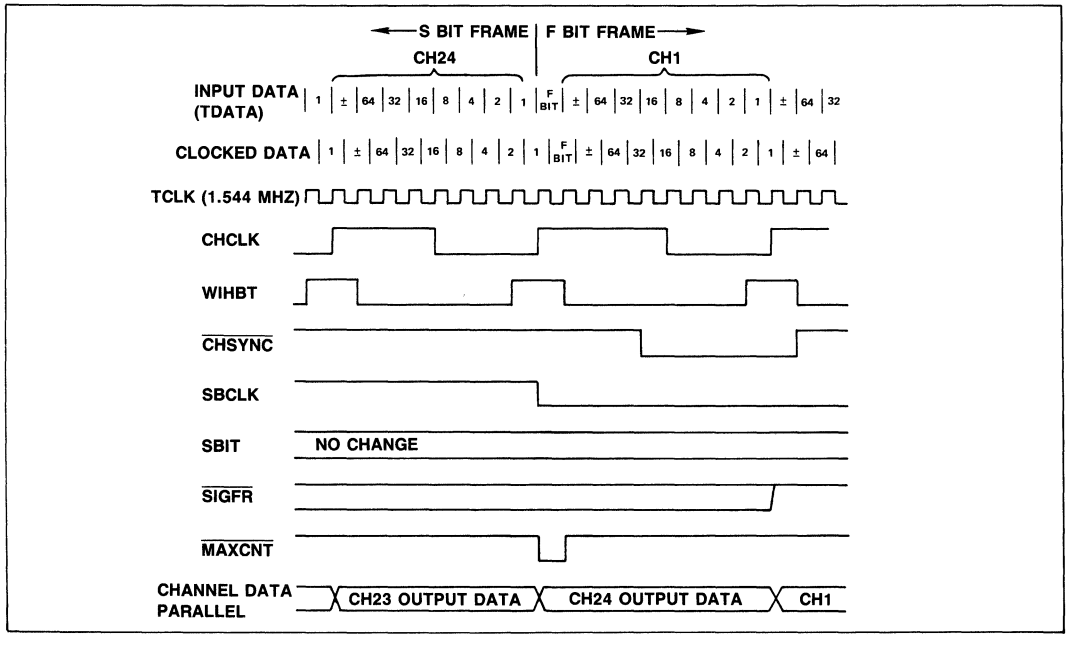
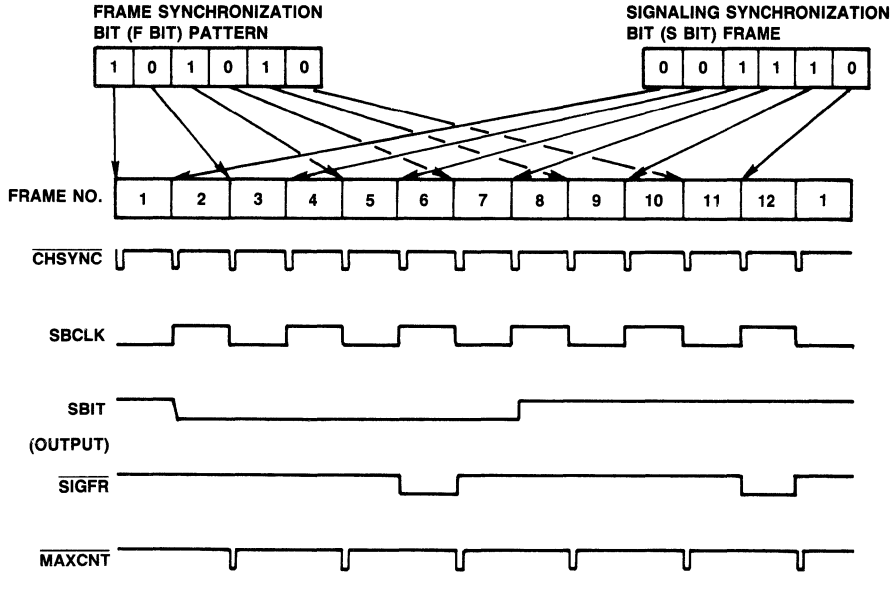


Figure 4. Signal Relationship at Beginning of F_T Frame (F-BIT)



FRAME = 24 TIME SLOTS = 193 BITS = 125 μS
TIME SLOT = 5.18 μS ONE BIT = 648 NS
MULTIFRAME = 12 FRAMES = 1.5 MS.

F BIT (F_T) ALIGNMENT SIGNAL
(ODD-NUMBERED FRAMES)

FRAME	FIRST BIT
1	1
3	0
5	1
7	0
9	1
11	0

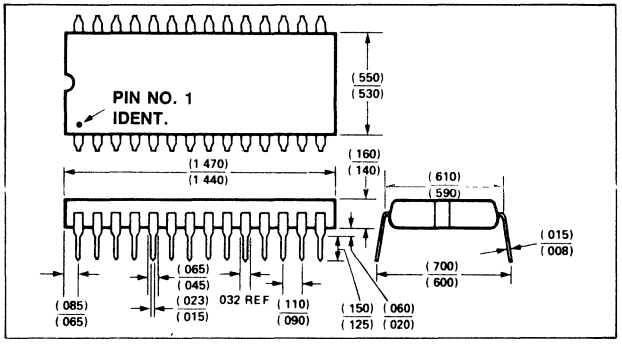
S BIT (F_S) MULTIFRAME ALIGNMENT SIGNAL
(EVEN-NUMBERED FRAMES)

FRAME	FIRST BIT
2	0
4	0
6	1
8	1
10	1
12	0

Figure 5. Multiframe Signal Relationships

Table 1. Output Propagation Delay
Worst Case, From Rising Edge of TCLK

OUTPUT	MAX DELAY (NS)
CHCLK	300
CHSYNC	300
WIHBT	300
MAXCNT	300
SBCLK	400
SBIT	400
SIGFR	475
SBALRM	475
B2ALRM	450
CALRM	300
FRALRM	900
CDB (1–8)	400



Packaging Diagram

MAXIMUM RATINGS*

Parameter	Symbol	Value	Unit
Supply Voltage	V_{DD}	+4.75 to +5.25	V
Operating Temperature Range	T_{OP}	0 to +70	°C
Storage Temperature Range	T_{STG}	−55 to +150	°C

***NOTE:** Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in other sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +5V ±5%, T_A = 25°C)

Parameter	Symbol	Min	Max	Unit
Input Logic "1" Voltage	V_{IH}	2.0	V_{DD} + 0.3	V
Input Logic "0" Voltage	V_{IL}	−0.3	0.8	V
Output Logic "1" Voltage	V_{OH}	2.4		V
Output Logic "0" Voltage	V_{OL}		0.4	V
Output Source Current	I_{OH}	−100		μA
Output Sink Current	I_{OL}	400		μA
Clock Frequency	T_{CLK}		1.85	MHz
Input Capacitance	C_I		5	pF
Output Capacitance	C_O		25	pF
Power Dissipation	P_{DSS}		550	mW

Rockwell

R8070
T-1/CEPT PCM TRANSCEIVER

INTRODUCTION

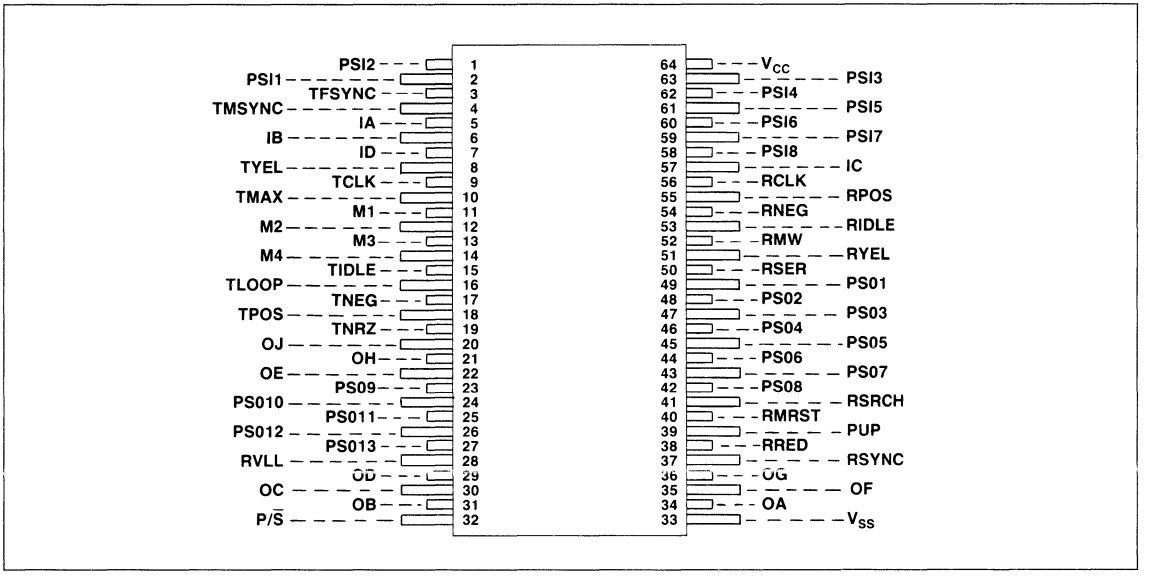
The R8070 is a monolithic silicon gate CMOS device designed to implement PCM transmitter and receiver functions applied in primary-rate digital carrier systems worldwide. Both the transmitter and receiver contain appropriate circuitry for synchronization, channel monitoring and signalling extraction.

The R8070 supports CCITT recommendations G 732, G.733 and applicable sections of G.703, as well as Bell System technical advisories on clear channel capability and extended framing format. This device provides the interfaces between the multiplexed digital signals of the subscriber loop and the PCM highway in a digital telephone switching system. The device operates from a single power supply of 5 volts and a sampling clock of 1.544 to 2.048 MHz, depending on the mode of operation.

Packaged in a 64-pin QUIP (quad in-line package), the R8070 requires less real-estate and provides flexibility in system integration and manufacturing. Specific support of both types of operation modes (parallel/serial) allows the application of the R8070 in virtually every type of voice/data system using either T-1, T-1C, or CEPT specification.

FEATURES

- Autonomous Transmit and Receive Sections in a single chip
- Low Power CMOS 100mw (Operating)
- 5 Volts Single Supply Voltage
- 64-pin QUIP
- Meets CCITT G.732, G 733, and applicable sections of G.703 Specifications and AT&T Advisories
- Operates with EXTENDED FRAMING, CLEAR CHANNEL, and/or CEPT formats
- Supports Multiplex/Demultiplex T-1C, Mode 1 (Synchronous) Operations
- Uses a clock of 1.544 (T-1), 1.576 (1/2 T-1C) or 2.048 (CEPT) MHz, depending on operation mode
- Selectable Serial or Parallel Digital Data Interface
- Reframe Time 10 ms (Mode Dependent)
- TTL/CMOS Compatible Inputs and Outputs



R8070 Pin Configuration

8

FUNCTIONAL CHARACTERISTICS

TRANSMIT SECTION

The transmit section of the R8070 (refer to the R8070 Functional Block Diagram) formats data to be serially transmitted according to CCITT G.732, G.733, applicable sections of G.703, and Bell technical advisories on clear channel capability and extended framing format. The 8-bit PCM data is clocked out by the transmit clock, which can vary between 1.544 and 2.049 MHz, depending on the selected mode of operation. Input signals TSSYNC and TMSYNC provide external synchronization to the R8070 frame counters.

Depending on the mode of operation when a yellow alarm is received, the R8070 is capable of sending idle messages in all message channels by activating the TIDLE input. A TLOOP is provided to aid testing user's applications by connecting internally TNEG and TPOS to RNEG and RPOS. Yellow alarm signalling to remote equipment is conveyed by stuffing or manipulating the appropriate bits in the various data channels, depending on the mode of operation.

Transmit output signals (i.e., TCHCLK, TCHSYNC and TMAX) are provided as a means to synchronize external equipment to the internal bit counters. Two types of data output formats are provided by virtue of pins TNRZ, TPOS and TNEG. TPOS and TNEG can be configured with minimal external circuitry to create a bipolar output. When configured in a parallel mode, the transmit channel data bits T1–T8 are sampled by the rising edges of TCLK. When used in a serial transmit mode, input control signal TSA allows advancement by one bit time of the transitions on TSQ and TSIGSQ. TSIGMD identifies the input source for transmit signalling information. Transmit output signals, designated by TSQ1 through TSQ5, are provided and can be used in decoding schemes to address individual channel cards residing in channel banks, according to D1D or D2 sequential code format.

Various mode dependent signals are used to provide control and signalling to the transmitted data stream. Transmit link input signal, TLINK, is used to input link information at various bit rates, depending on the mode of operation. Provision for insertion of error patterns in the F position is made possible through input TFSIG. In the 193E and S modes, robbed bit signalling information is provided and controlled through inputs TA(C) and TB(D). In the 256S mode, the serial bit stream containing the transmit signalling information is provided at TABCD and sampled at an 8 kHz rate. Repetitive transmission of a certain code sequence in a given channel on TNRZ or TPOS and TNEG provides a 0 dBm 1 KHz signal. When decoded in a properly aligned receiving terminal, this signal is referred to as digital milliwatt. A multiplexed framing pattern generator signal, which is the result of the composite of an externally supplied S BIT and an internally generated data link CRC check bit, is provided at TFGEN. TI1S, TN1S, and TX1S are provisions for inputs that are dedicated for use in the 256 modes and are typically applied in handshaking applications between the transmit and receive terminals. Many other signals are used on different assignments, depending on the selected operating mode, and are described in detail in this document. These input and output signals are used to provide the hooks and handles that are associated with each mode.

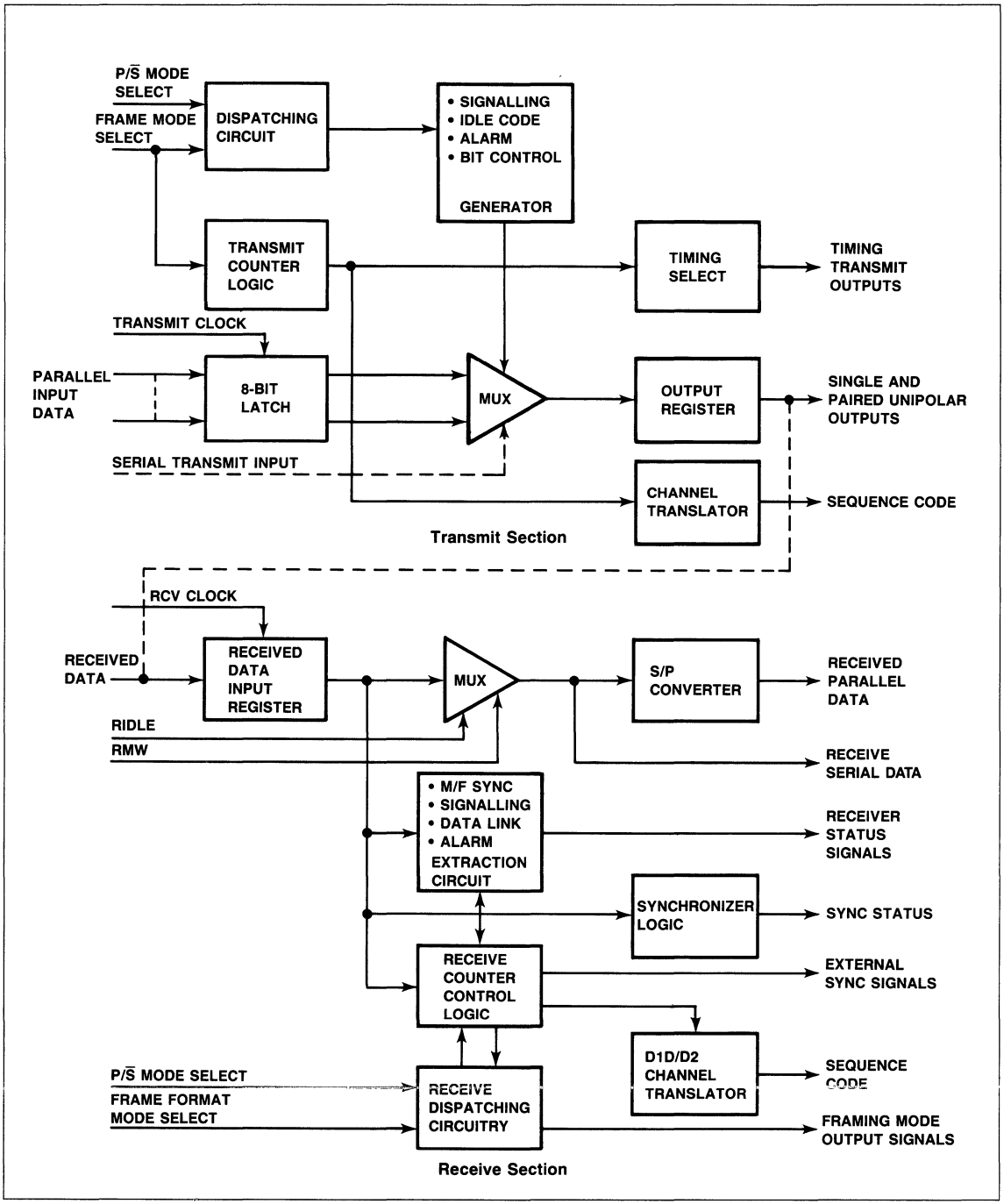
RECEIVE SECTION

In the receive section (refer to R8070 Functional Block Diagram), the received unipolar data is processed serially by the rising edge of RCLK at a rate of 1.544 to 2.048 MHz, depending on the mode of operation (Bell or CCITT). Synchronization is accomplished by locating the F_t bit (framing bit) through a five-stage process, thus eliminating erroneous bit candidates that could cause false synchronization. In the 193N and S modes, synchronization is achieved in less than 5ms, while in the other modes, it is achieved in less than 10ms.

Output signals such as RSYNC, RSRCH, RRED, and RMAX are dependent on the synchronizer receive master state and may be used for status reporting or external processing of the received data. Remote alarm monitoring (yellow alarm) is reported by RYEL in a format appropriate to the transmission mode.

Similar to the transmitter, a provision that allows insertion of idle channel data in the received bit stream is invoked by activating the RIDLE input. RMW input is provided for trunk alignment, causing a 1 kHz milliwatt generator to be substituted for all received message channels.

Receive output signals (i.e., RCHSYNC, RCHCLK, and RWIHBT) are provided for synchronization of external counters to the PCM frame rate and strobing the received data into external memory if necessary. Additional output signals are provided to indicate the status of the received data, the type of alarm received and a bipolar violation indication when it is manifested in the data pattern. Serial mode receive outputs (i.e., RSQ1–RSQ5) are used in a decoding scheme to select channel units residing in channel banks. Receive framing mode dependent signals OA through OJ are used for monitoring of signalling information, error reporting, synchronization reporting and many useful alarm reporting signals.



R8070 Functional Block Diagram

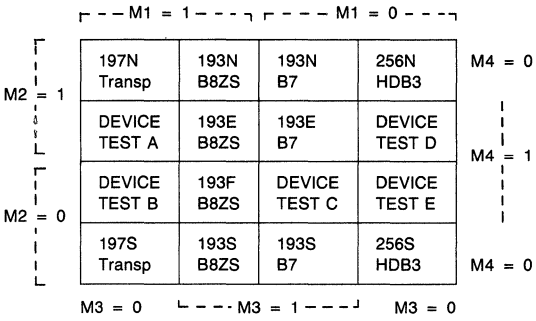
OPERATIONAL MODES

The R8070 is configurable in a parallel or serial operation. The R8070 is mode selectable. By strapping input lines M1–M4, eleven data formats are provided to meet the user's requirements.

The P/$\overline{S}$ (Parallel/Serial) mode straps are as follows:

1. Parallel P/$\overline{S}$ = 1
2. Serial P/$\overline{S}$ = 0

The permissible modes that may be selected are illustrated.



Mode Selection

INTERFACE CRITERIA

PARALLEL/SERIAL MODE-DEPENDENT INPUTS

Parallel Mode-Dependent Inputs

Pin	Name	Description
PSI1	T1	
PSI2	T2	
PSI3	T3	
PSI4	T4	Transmit Channel
PSI5	T5	Data Bits 1–8
PSI6	T6	
PSI7	T7	
PSI8	T8	

Serial Mode-Dependent Inputs

Pin	Name	Description
PSI1	TSER	Transmit Serial Input
PSI2	TSIGMD	Transmit Signalling Mode
PSI3	TABCD	Transmit Signalling Input
PSI4	TSA	Transmit Sequence Advance
PSI5	RSHIFT	Receive Shift
PSI6	D1D	D1D Sequence
PSI7	D2	D2 Sequence
PSI8	RSR	Receiver Sequence Retard

PARALLEL/SERIAL MODE-DEPENDENT OUTPUTS

Parallel Mode-Dependent Outputs

Pin	Name	Description
PSO1	R1	
PSO2	R2	
PSO3	R3	
PSO4	R4	Receive Channel Data Bits 1–8
PSO5	R5	
PSO6	R6	
PSO7	R7	
PSO8	R8	
PSO9	TCHCLK	Transmit Channel Clock
PSO10	TCHSYNC	Transmit Channel Sync
PSO11	RCHCLK	Receive Channel Clock
PSO12	RCHSYNC	Receive Channel Sync
PSO13	RWIHBT	Receive Write Inhibit

Serial Mode-Dependent Outputs

Pin	Name	Description
PSO1	RSQ1	
PSO2	RSQ2	
PSO3	RSQ3	Receive Sequence Code Bits 1–5
PSO4	RSQ4	
PSO5	RSQ5	
PSO6	TSIGSQ/TNSYNC*	
PSO7	RSIGSQ/RIBITS*	
RSO8	R8/RABCD	
PSO9	TSQ1	
PSO10	TSQ2	
PSO11	TSQ3	Transmit Sequence Code Bits 1–5
PSO12	TSQ4	
PSO13	TSQ5	

Notes

*Mode 193 or 197	Transmit Signalling Square Wave	(PSO6)
	Receive Signalling Square Wave	(PSO7)
	Receive Channel Data Bit 8	(PSO8)
*Mode 256	TNSYNC Transmit National Sync	(PSO6)
	RIBITS Receive International	(PSO8)
	RABCD Receive Signalling	(PSO8)

INPUT/OUTPUT SIGNAL CHARACTERISTICS

R8070 Input/Output Signal Characteristics

Mnemonic	Definition	Function
SERIAL MODE COMMON INPUTS:		
D1D, D2	Code Select Modes	These signals, D1D and D2, permit the generation of transmit and receive serial codes, according to CCITT or the D1D and D2 channel assignment format: D1D = 0, D2 = 0 CCITT D1D = 1, D2 = 0 D1D D1D = 0, D2 = 1 D2
COMMON RECEIVE INPUT SIGNALS:		
PUP	Power-Up	This signal initializes the R8070. It can also be used as a "hands off' restart. After power is applied and RCLK and TCLK are active, PUP must be held low for at least 16 clock cycles to ensure output predictability (refer to Power-Up Timing Requirement Diagram).
RCLK	Receive Clock	An external timing source is input via the RCLK pin to provide the master timing for the receive function
RIDLE	Receive Idle Control	When RIDLE is high and RMW is low, idle codes are substituted for all received message channels; this signal is sampled channel-by-channel
RMRST	Receive Master Reset	When RMRST is high, it forces the master state controller to go into a "WAIT" state, if a continuous level is maintained, and holds off entry to "INIT" ("WAIT" = the initial step of the synchronization process).
RMW	Receive Milliwatt	When RMW is high and RIDLE is low, RMW causes the internal 1 kHz milliwatt generator to be substituted for all received message channels. This signal is sampled channel-by-channel.
RPOS, RNEG	Receive Unipolar Positive and Negative	Input data to the receiver which may be of RZ or NRZ nature. When RPOS is strapped to RNEG it causes: 1. B8ZS or HDB3 modes to become transparent for transmit functions and receive functions. 2. Disabling of the bipolar violation detector.
RSRCH	Receive Search Control	When low, RSRCH holds off entry to "INIT", the second step of the initialization process. When RRED and RSRCH are active low during the first time slot of the first frame of the multiframe, bit 5 is skipped.
COMMON RECEIVE OUTPUT SIGNALS:		
RRED	Receive Red Alarm	RRED is high when the receiver is not synchronized. RRED when low indicates that the receiver is frame synchronized. It may or may not be multiframe synchronized.
RSER	Receive Serial Data	RSER represents the received serial data bit stream, including any B8ZS or HDB3 corrections.
RSYNC	Receive Synchronization State Indicator	RSYNC provides a SYNC output that is dependent upon the receive master state. 1. SYNC (North American): Single pulse coinciding with the first 'F' bit for each new multiframe, as shown in the North American Mode Receive Synchronization Timing Diagram. 2. SYNC (European): Single pulse coinciding with bit one of each new multiframe, as shown in the European Receive Synchronization Timing Diagram.
RVLL	Bipolar Violation, Loss of Carrier	RVLL reports bipolar violations as a high-level coincident with the emergence of the accused bit at RSER. Also, RVLL reports failure to receive carrier.
RYEL	Receive Yellow Alarm	RYEL conveys yellow alarm information appropriate to mode. RYEL transitions occur one bit time after the bit that triggered the alarm merges out RSER.

R8070 Input/Output Signal Characteristics (Continued)

Mnemonic	Definition	Function
PARALLEL MODE RECEIVE OUTPUT SIGNALS:		
RCHCLK	Receive Channel Clock	RCHCLK is high during the output of bits 1 through 4 of the channel data on RSER. RCHCLK is low elsewhere.
RCHSYNC	Receive Channel Synchronization	RCHSYNC is suitable for synchronizing external counters to the T-1 or CEPT frame rate. Transitions on RCHSYNC are mode dependent.
R1–R8	Receive Channel Data Bits 1–8	R1–R8 are valid with the current channel data nominally for 8 bit times and extend to 9 or 10 bit times in cases where an 'F' and/or link bit occur Transitions coincide with the output of Bit 1 on RSER. Refer to the Parallel Mode Receive Signals Timing Diagram.
RWIHBT	Receive Write Inhibit	RWIHBT covers the parallel channel data transition period. It goes high-active before, during, and after the transitions on R1–R8.
SERIAL MODE RECEIVE INPUT SIGNALS:		
RSHIFT	Receive Shift	When RSHIFT is high, it causes the RSQ codes to be shifted.
RSR	Receive Sequence Retard	When RSR is high, the RSQ codes and RSIGSQ transitions are delayed by one bit time from their nominal positions.
SERIAL MODE RECEIVE OUTPUT SIGNALS:		
RSIGSQ	Receive Signalling Square Wave	RSIGQ exhibits a high-to-low transition during the output of the F-bit at RSER for frames carrying "B" (D) signalling and low-to-high transition during the output of the F-bit at RSER for frames carrying "A" (C) signalling. It is affected by RSR in the same manner as the RSQ leads.
RSQ1, RSQ2, RSQ3, RSQ4 and RSQ5	Receive Sequence Code Bits 1 through 5	RSQ1 through RSQ5 encode the current channel number according to CCITT convention. During the occurrence of framing, link and CRC bits, special codes are observed. Refer to the 197 Mode Receive Sequence Code Timing Diagram.
MODE DEPENDENT RECEIVE OUTPUT SIGNALS:		
RABCD	Receive ABCD	RABCD represents a serial bit stream containing the most recently received signalling bits for each of the 30 channels. RABCD is channel-aligned with RSER.
RIBITS (OB)	Receive International Bits	RIBITS goes high to indicate that the international bit is present at serial output RSER, as shown in the National and International Bits Timing Diagram.
RNBITS (OE)	Receive National Bits	RNBITS is active-high coincident with the emergence of bits 4 through 8 of TS0 not containing the frame alignment signal.
RTS16 (OC)	Receive Time Slot 16	RTS16 is high for the duration of TS16 bits 1 through 8 emerging from output RSER
RXBITS (OG)	Receive Extra Bits	RXBITS is active-high when RSER contains bits 5, 7 and 8 of TS16 containing the multiframe alignment signal
MODE DEPENDENT RECEIVE ERROR OUTPUT SIGNALS:		
CKERR (OC)	Cyclic Redundancy Check Bit Error	CKERR pulses high with the emergence of the "F" CRC bit at RSER if a cyclic bit error is detected.
ERR (OD)	Error Signal	ERR pulses high for one bit time upon detection of a framing error or check sum error.
FERR (OD)	Framing Error	This signal pulses high for one bit time, upon detection of a framing or check sum error. Response varies according to mode. Applicable to 193A, S & N, 197S & N, & 256N modes.

R8070 Input/Output Signal Characteristics (Continued)

Mnemonic	Definition	Function
MODE DEPENDENT RECEIVE ERROR OUTPUT SIGNALS (Continued):		
FMERR (OD)	Receive Frame Multiframe Error	FMERR pulses high for one bit time to indicate detection of either frame or multiframe errors. Applicable to 256S mode.
RMRED (OC)	Receive Multiframe Red	RMRED is active-high when two consecutive multiframe alignment errors have occurred or if all TS16 data bits are low for a complete multiframe. When RMRED is high, the transmitter transmits a multiframe yellow alarm in bit 6 of TS16, containing the multiframe alignment signal.
RMYEL (OF)	Receive Multiframe Yellow	RMYEL contains the extracted bit 6 of TS16 that represents the multiframe alignment signal.
SERR (OE)	S-Bit Errors	SERR pulses high for one bit time each time an error is observed in the received S-bit pattern.
MODE DEPENDENT RECEIVE SIGNALLING OUTPUT SIGNALS:		
MS1, MS2 (OF, OG)	Master State Sequence Code	The two least significant bits MS1 and MS2 are of the master state sequence code.
RLCLK (OG)	Receive Link Clock	RLCLK represents a square clock at the data rate of RLINK.
RLINK (OF)	Receive Data Link	RLINK reports data extracted from the "Received Link Data," occurring at the rates corresponding to the various transmission modes (refer to 256N mode Receive Link Data Timing Diagram).
RLINK1 (OC)	Receive Link 1	An active-high level indicates the reception of 255 consecutive ones in time slot 16.
RMFA (OA)—193F mode RMFA (OB)—256S mode	Receive Multiframe Alignment	RMFA is high for the duration of frame 24. Transitions coincide with the emergence of the "F" bits at RSER. In the 256S mode, RMFA is active-high for the duration of the frame which contains the multiframe alignment signal.
RSBCLK (OC)	Receive S-Bit Clock	RSBCLK is a 4 kHz square clock whose low to high transition occurs 1 bit after the emergence of RSBIT (F_S) at RSER.
RSIG (OA)	Receive Signalling Frame	RSIG is active-high during the receipt of signalling frames. Activity is suspended if recent errors have been observed in the F-bit or S-bit.mode dependent signal.
RSIGBD (OB)	Receive Signalling B or D	RSIGBD represents a 2 kHz square wave with low-to-high transitions occurring during frames containing the A or C signalling, and high-to-low transitions occurring during frames containing B or D signalling.
RSIGCD (OC)	Receive Signalling C or D	RSIGCD represents a 1/3 kHz square clock with transitions coinciding with the emerging F-bit at RSER.
RSBIT (OB)	Receive Signalling-Framing Bit	RSBIT is the most current received S-bit coincident with the emergence of the S-bit at RSER and is mode dependent.
COMMON TRANSMIT INPUT SIGNALS:		
TCLK	Transmit Clock	All inputs of the transmit section are sampled on the rising edge of TCLK.
TFSYNC	Transmit Frame Sync	TFSYNC synchronously restarts the transmitter to the beginning of a frame TFSYNC reinforces the internal count cycle when pulsed once per frame.

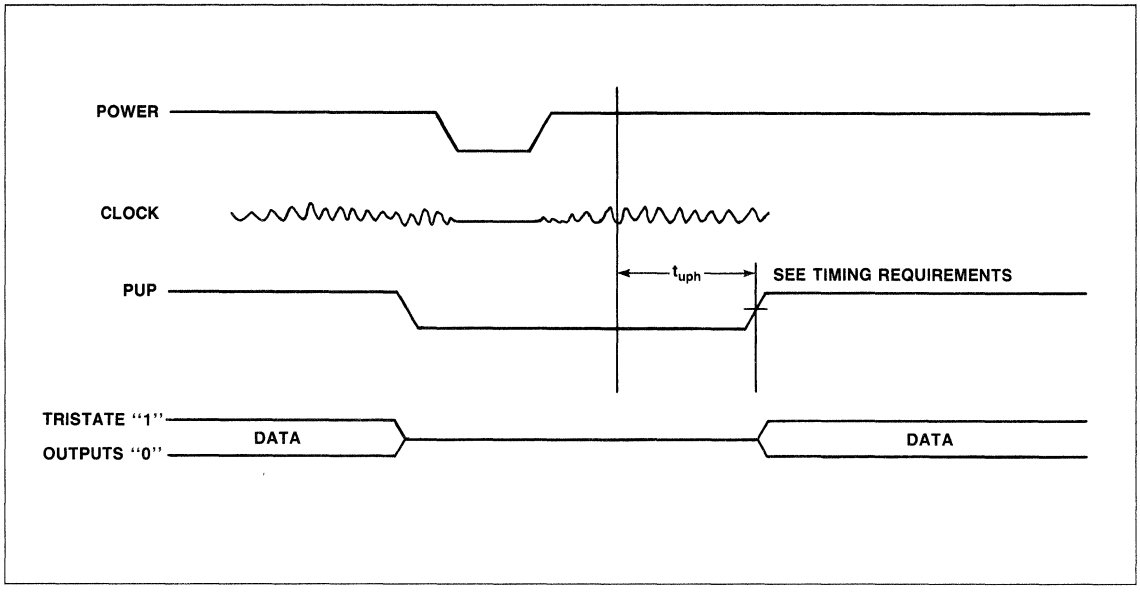
8

R8070 Input/Output Signal Characteristics (Continued)

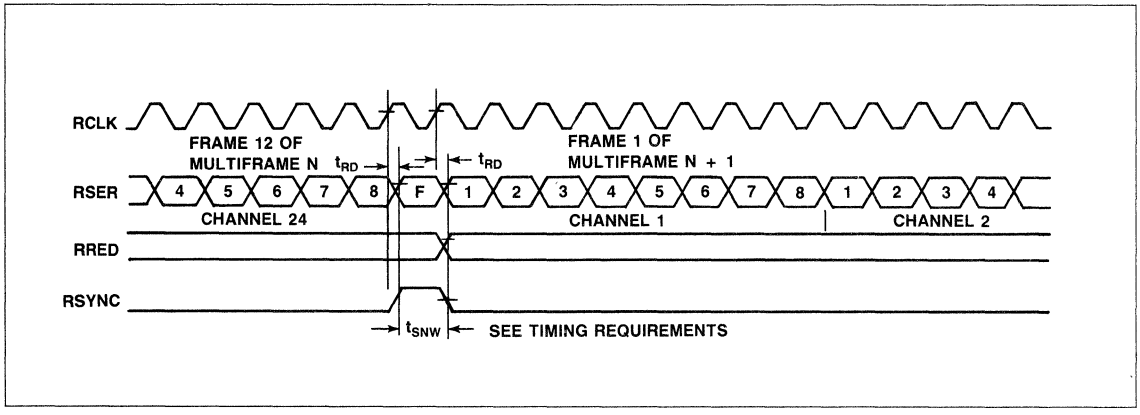
Mnemonic	Definition	Function
COMMON TRANSMIT INPUT SIGNALS (Continued):		
TIDLE	Transmit Idle	When high, TIDLE causes the transmitter to output idle code in all message channels via TNRZ, TPOS and TNEG.
TLOOP	Transmit Loop	When high, TLOOP causes the transmitter to alternately transmit ones on TPOS and TNEG, and the transmitter internal TPOS and TNEG signals to be routed to the receive function in place of RPOS and RNEG. TLOOP does not affect TNRZ.
TMSYNC	Transmit Multiframe Sync	When active-high, it synchronously sets the internal frame counter to the first frame of a multiframe.
TYEL	Transmit Yellow Alarm	High level on TYEL activates the transmission of a yellow alarm and is mode dependent.
COMMON TRANSMIT OUTPUTS:		
TMAX	Transmit Maximum	TMAX pulses high for one bit time coincident with the sampling of the last serial bit of a multiframe.
TNRZ	Transmit Non-Return to Zero	This output contains the non-return-to-zero bit stream of the transmitter. TNRZ is not affected by TLOOP, HDB3 or B8ZS functions.
TPOS, TNEG	Transmit Positive, Negative	TPOS and TNEG contain the transmit output bit stream conditioned for alternate mark inversion. This sequence of steering alternate ones for each of these outputs is deliberately broken when a B8ZS or HDB3 substitution takes place.
PARALLEL MODE TRANSMIT OUTPUT:		
TCHCLK	Transmit Channel Clock	TCHCLK indicates times when parallel data has been sampled.
TCHSYNC	Transmit Channel Sync	TCHSYNC is an 8-bit signal active prior to the sampling of parallel data for the first message channel.
SERIAL MODE RECEIVE INPUT SIGNALS:		
TSA	Transmit Sequence Advance	When TSA is high, transitions on TSQ1–TSQ5 and TSIGSQ are advanced one bit time Refer to the Transmit Seqence Code Timing Diagram.
TSIGMD	Transmit Signalling Mode	TSIGMD indicates that signalling is included within the serially input bit stream or through dedicated signalling inputs. The effect of TSIGMD varies for different modes.
TABCD	Transmit Signalling ABCD	TABCD consists of a serial bit stream containing transmit signalling sampled at an 8 kHz rate for each of the 30 channels, applicable to the 256S mode
TSER	Transmit Serial	TSER is a serial bit stream containing the message data
SERIAL MODE RECEIVE OUTPUT SIGNALS:		
TSIGSQ	Transmit Signalling Square	TSIGSQ is a 2/3 kHz square wave aligned to cause certain per-channel codecs to insert A and B signalling into TSER.
TSQ1–TSQ5	Transmit Sequence Code Bits 1–5	TSQ1–TSQ5 represent the transmit sequence codes with coding identical to RSQ When TSA is high, these transitions occur an additional bit time earlier
PARALLEL MODE TRANSMIT INPUTS:		
T1–T8	Transmit Channel Data Bits 1–8	T1–T8 are sampled by the rising edge of the TCLK These inputs should be applied when TCHCLK is low

R8070 Input/Output Signal Characteristics (Continued)

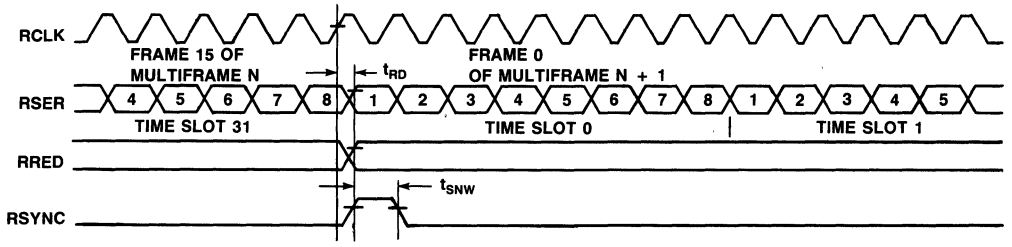
Mnemonic	Definition	Function
FRAMING MODE DEPENDENT TRANSMIT INPUT SIGNALS:		
TDATIS (IC)	Transmit Data Ones	A high level on TDATIS triggers the transmission of all ones in time slot 16.
TLNKMD (ID)	Transmit Link Mode	A one or zero level on TLNKMD selects between data or Link information to be transmitted in TS16 (applicable to 256N mode).
TA(C), TB(D), IA, IB	Transmit TA(C) and TB(D) Signalling	These signals provide A(C) and B(D) robbed-bit signalling A and B are selected when TSIGSEL = 0. C and D are selected when TSIGSEL = 1. These conditions are applicable to the 193E.
TA, TB, IA and IB	Transmit A and B Signalling	TA and TB are sampled at the beginning of a channel time to provide A and B robbed-bit signalling (applicable to the 193S and 197S modes).
TIBITS, TNBITS, TXBITS	Transmit international, national and extra bits	These signals allow the transmission of the international, national and extra bits Applicable to modes 256 S&N.
TFSIG (ID)	Framing-Bit Signal	TFSIG input provides the F_T and F_S bits (mode dependent) The input is sampled coincident with the sampling of channel one parallel data.
TLINK (IC)	Transmit Link	Provides a serial data link input at either 4, 32, or 64 Kbps, depending on mode (equivalent to the rates on RLINK).
YELMD (IC)	Yellow Alarm	YELMD input selects method for Transmission and detection of yellow Alarm If low, yellow Alarm will be transmitted as the inhibit of bit 2 If high, yellow Alarm is identified as the F_S bit for frame 12
TSBIT (IA)	Transmit S-bit	In modes 193N and 197N, this input is sampled to provide the transmitted S-bit to control the S-bit transmission
FRAMING MODE DEPENDENT TRANSMIT OUTPUT SIGNALS:		
TTS16 (OJ)	Transmit Time Slot 16	Active for 8 bit times prior to the sampling of TS16 data at TSER.
TMFA (OH)	Transmit Multiframe Alignment	TMFA is active during sampling of data for frames containing the multiframe alignment signal
TNSYNC	Transmit National Bit-Sync	TNSYNC is active-high during sampling of the national bits (bits 4 through 8) of TS0 for frames not containing frame alignment
TFGEN (OJ)	Framing-Bit Generator	This signal is the composite framing pattern generator. It is the result of multiplexing externally-supplied S-bit data with the internally-generated framing pattern, the data link and the CRC check bits appropriate to the operating mode
TFR24 (OE)	Transmit Frame 24	A high level on TFR24 indicates that frame 24 is being processed.
TLCLK (OH)	Transmit Link Clock	TLCLK represents a square clock at the data rate of TLINK.
TSBCLK (OE)	Framing-Bit Generator	TSBCLK is a 4 kHz square wave whose rising edge occurs two bit times after the TSBIT input has been sampled.
TSIGSEL (OE)	Transmit Signalling Select	When low, it indicates that A and B channels are being sampled When high, it indicates that C and D channels are being sampled Transitions coincide with the sampling time of the "F" bits



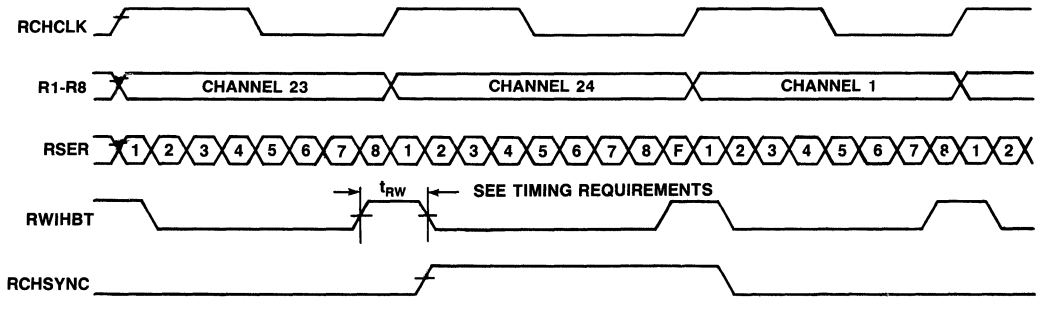
Power Up Timing Requirement



North American 193 Mode Receive Synchronization Timing



European Receive Synchronization Timing



NOTE: ABOVE TIMING IS APPLICABLE TO ALL 193 MODES.

Parallel Mode Receive Signals Timing

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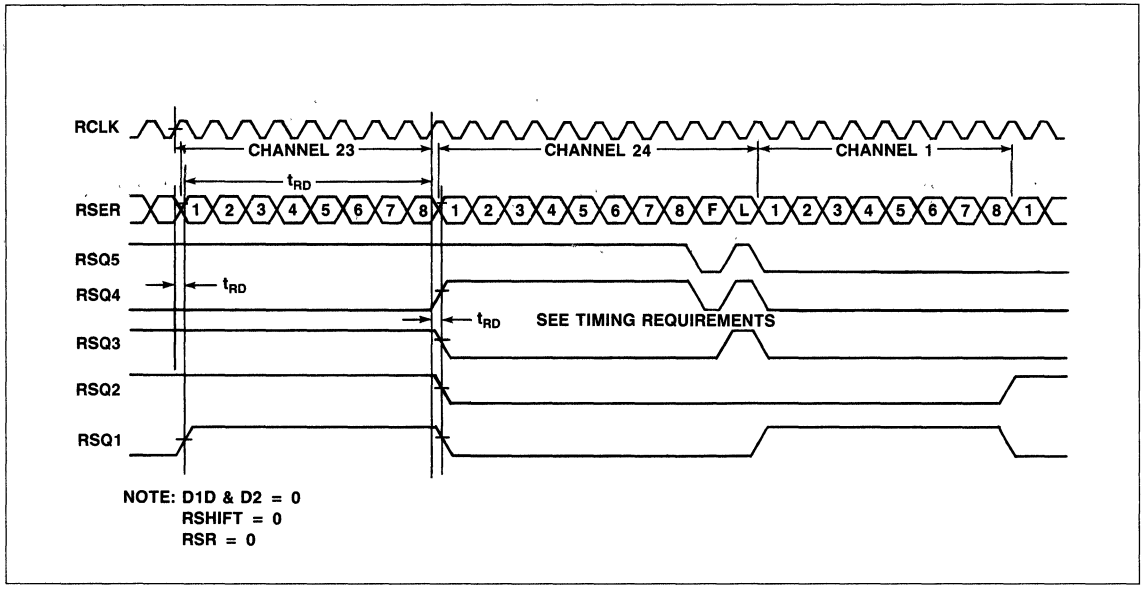
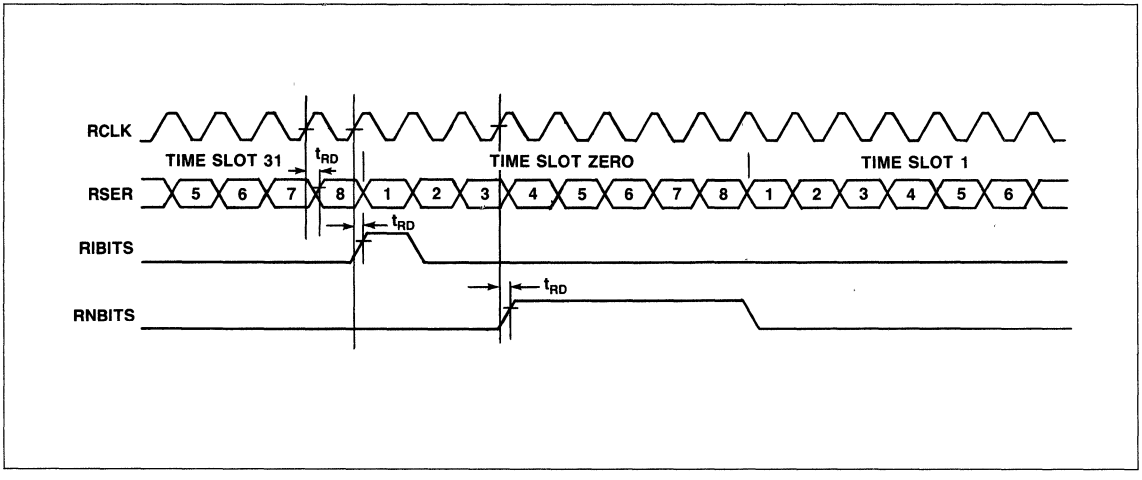
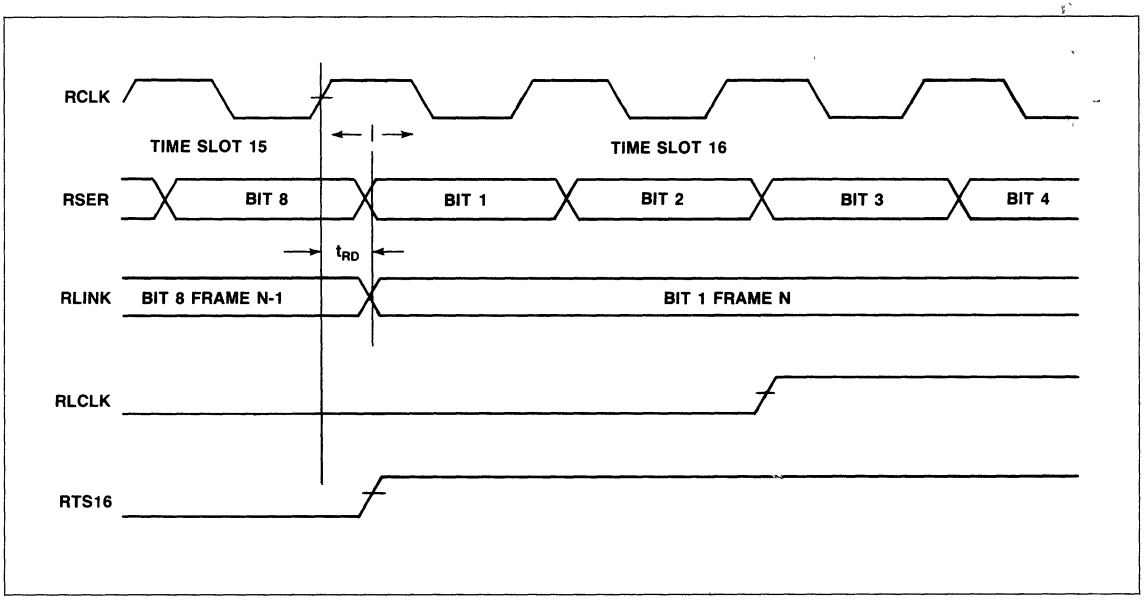


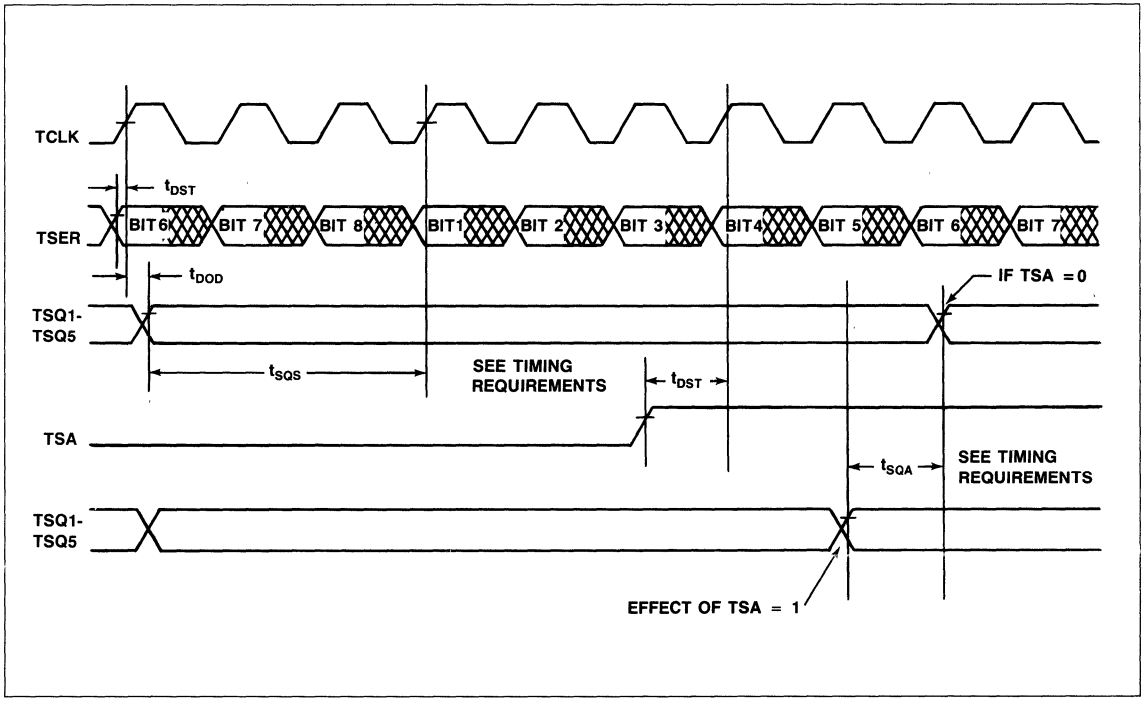
197 Mode Receive Sequence Code Timing



National and International Bit Timing



256N Mode Receive Link Data Timing



Transmit Sequence Code Timing

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FRAMING MODE SUMMARY

The framing mode dependent signals are summarized in the table below. Inputs IA-ID and output OA-OJ are functionally related to the various modes of operation as previously discussed.

Framing Mode-Dependent Signals

Inputs	Modes							
PIN	193N	193S	197N	197S	193E	193F	256N	256S
IA	TSBIT	TA	TSBIT	TA	TA(C)	*	TIBITS	TIBITS
IB	*	TB	*	TB	TB(D)	*	TNBITS	TNBITS
IC	*	YELMD	TLINK	TLINK	TLINK	TLINK	TLINK	TDAIS
ID	TFSIG	TFSIG	TFSIG	TFSIG	TFSIG	TFSIG	TLNKMD	TXBITS
Outputs	**Modes**							
OA	RSIG	RSIG	RSIG	RSIG	RSIG	RMFA	RTS16	RTS16
OB	RSBIT	RSBIT	RSBIT	RSBIT	RSIGBD	**	RIBITS	RMFA
OC	RSBCLK	RSBCLK	RSBCLK	RSBCLK	RSIGCD	CKERR	RLINK1	RMRED
OD	FERR	FERR	FERR	FERR	ERR	FERR	FERR	FMERR
OE	TSBCLK	SERR	TSBCLK	SERR	TSIGSEL	TFR24	RNBITS	RNBITS
OF	MS1	MS1	RLINK	RLINK	RLINK	RLINK	RLINK	RMYEL
OG	MS2	MS2	RLCLK	RLCLK	RLCLK	RLCLK	RLCLK	RXBITS
OH	**	**	TLCLK	TLCLK	TLCLK	TLCLK	TLCLK	TMFA
OJ	TFGEN	TFGEN	TFGEN	TFGEN	TFGEN	TFGEN	TTS16	TTS16

Notes
*Test inputs, preferably tied to a high level
**Test outputs, leave unloaded

INPUT/OUTPUT SETUP/HOLD TIMES

Input/Output Setup/Hold Times

Output (Transmitter/Receiver)	Maximum Delay	Unit
(Measured from rising edge of clock unless stated otherwise)	100	ns
Input (Transmitter/Receiver)	Minimum Setup Time	Unit
Input Setup and Hold Times	60	ns

Timing Requirements

t_{UPH} (power up hold time) = 16 clock periods minimum
t_{SQS} (TSQ setup time) = 1 clock period or 2 depending on TSA
t_{DST} (transmit data setup time) = 60 ns minimum
t_{RD} (receive data ouput delay) = 100 ns maximum
t_{SNW} (RSYNC pulse width) = 1 clock period
t_{RW} (write inhibit pulse width) = 2 clock periods typical
t_{SNW} (RSYNC pulse width) = 1 clock period typical
t_{SQA} (TSQ advance time) = 1 clock period
t_{DOD} (transmit data output delay) = 100 ns maximum
t_{RST} (receive input setup time) = 60 ns minimum
t_{RHT} (receive input hold time) = 60 ns minimum

MAXIMUM RATINGS*

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	+4.75 to 5.25	Vdc
Operating Temperature Commercial Industrial	 T_{OPC} T_{OPI}	 0 to +70 −40 to +85	°C
Storage Temperature	T_{STG}	−55 to +150	°C

***NOTE:** Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the other sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

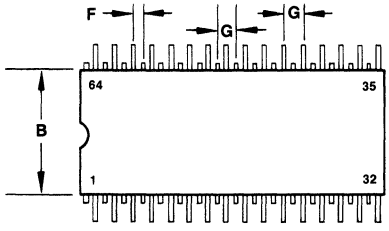
Parameter	Symbol	Min	Max	Unit	Test Condition
Input Logic "1" Voltage	V_{IH}	2.0	V_{CC} + 0.3	V	
Input Logic "0" Voltage	V_{IL}	—	0 8	V	
Output Logic "1" Voltage	V_{OH} T2L CMOS	2 4 3 5	—	V	I_{LOAD} = −1 6mA I_{LOAD} = −100μA
Output Logic "0" Voltage	V_{OL}	—	0 4	V	I_{LOAD} = +1.6 mA
Output Source Current	I_{OH}	−100		μA	V_{OH} = 2.4V
Output Sink Current	I_{OL}		+1.6	mA	V_{OL} = 0 4V
Clock Frequency	T_{CLK}	100 kHz	2.049	MHz	
Input Capacitance	C_{IN}		5	pF	
Output Capacitance	C_{OUT}		50	pF	
Power Dissipation	P_{WD}		100	mw	

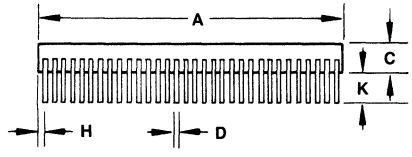
REFERENCE DATA

For detail information refer to the R8070 T-1/CEPT PCM Transceiver Designer's Guide. Order Number 313.

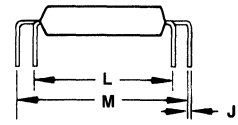
PACKAGE DIMENSIONS

64 PIN PLASTIC QUIP





DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	41 15	41 66	1 620	1 640
B	17 02	17 53	0 670	0 690
C	3 05	4 56	0 120	0 180
D	0 38	0 51	0 024	0 020
F	1 27 BSC		0 050 BSC	
G	2 54 BSC		0 100 BSC	
H	1 02	1 14	0 040	0 045
J	—	7°	—	7°
K	2 79	4 32	0 110	0 170
L	18 92	19 81	0 745	0 755
M	23 37	23 62	0 920	0 930



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