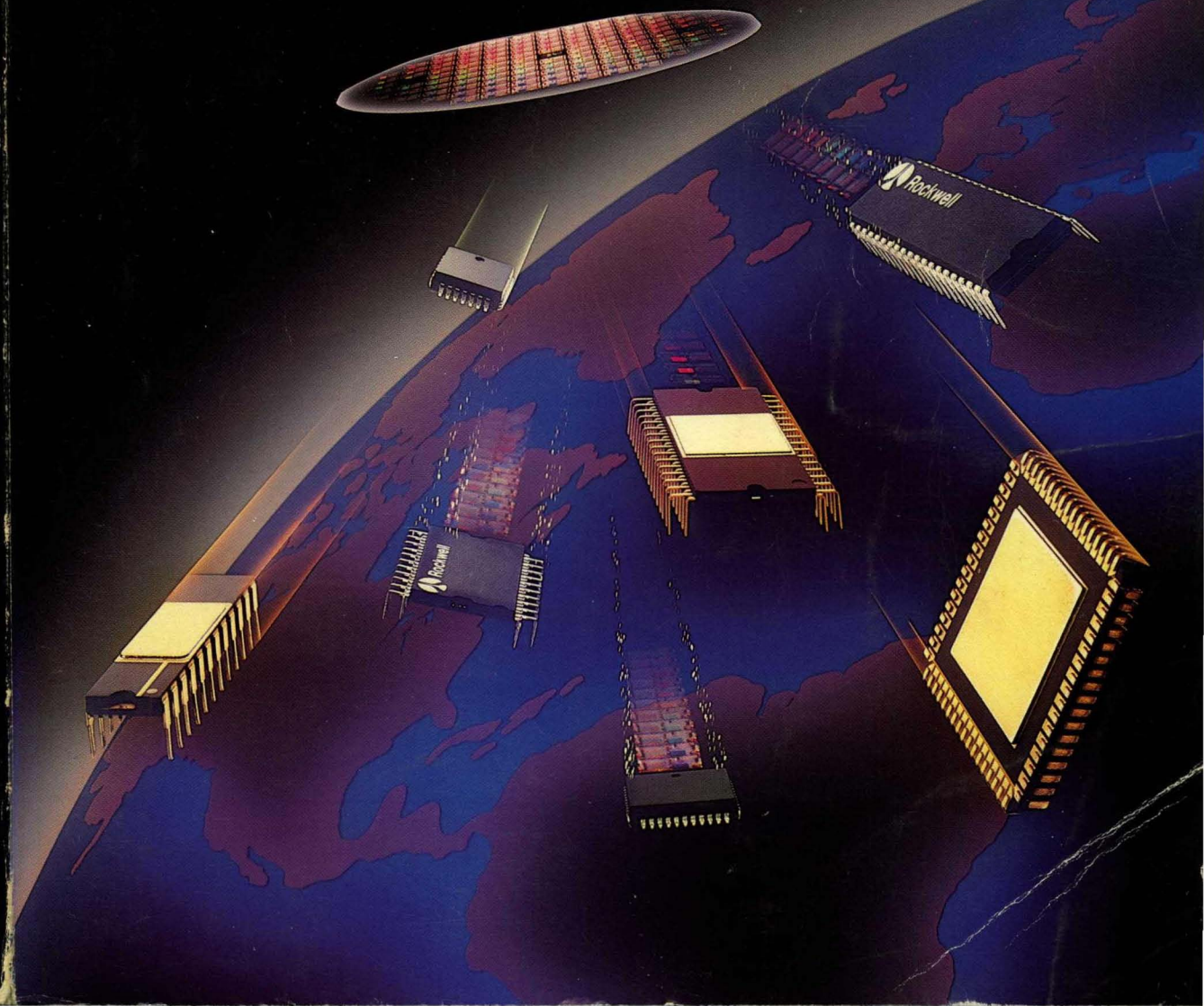
Order No. 3

Rockwell International

Semiconductor Products Division

CONTROLLER PRODUCTS DATA BOOK



ROCKWELL 1987
CONTROLLER PRODUCTS DATA BOOK

Rockwell International

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1987
CONTROLLER PRODUCTS
DATA BOOK

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Order No. 3
July 1987

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DEFINITION OF DOCUMENT TYPES

Document Type	Product Status	Definition
Product Preview	Formative or Development	The document type contains the general features and/or specifications for a product in definition or development. The features and/or specifications may change in any manner without notice.
Product Summary	Development or Production	This document type contains the general features and/or specifications of a product in development or in production. Additional information is usually available in a separate document, not contained in this book, such as a Designer's Guide.
Data Sheet (Preliminary)	Sampling or Pre-Production	This document type contains preliminary or design-to-characteristic data for a product in pre-production. Additional and/or refined characteristic data will be released in subsequent revisions to the document.
Data Sheet	Production	This document type contains final specification information resulting from measured characteristics. This document type is subject to revision if characteristics are further refined during production.
Product Description	Production	This document type contains final specification information resulting from measured characteristics along with additional application aid information. This document type is subject to revision if characteristics are further refined during production.
Application Note	Development or Production	This document type contains application aids in the use of the subject product. Schematics included in an application note are intended to convey system design concept only.

NOTICE

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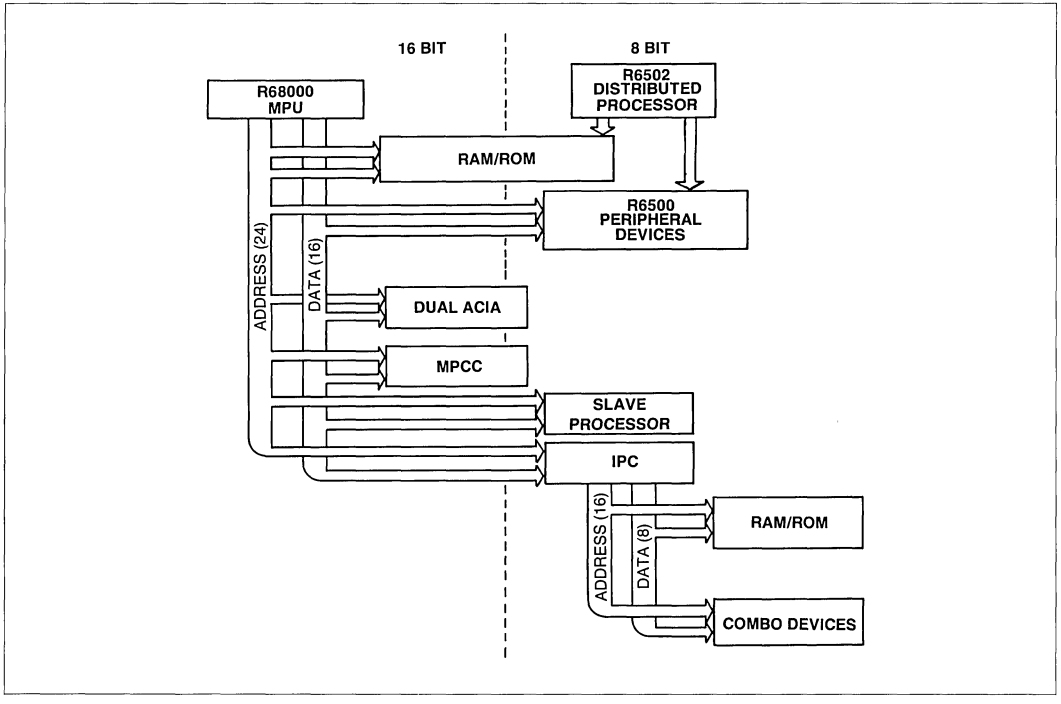
CONTROLLER PRODUCTS
Providing Solutions for Your VLSI Requirements

Rockwell International designs and manufactures a family of VLSI products to serve your system requirements. As shown in the diagram below, compatible controller products are available for a wide range of 16-bit and 8-bit applications. Peripheral devices operate on either the 68000 or the 6500 microprocessor bus structure. Many of the peripheral devices are now being used on additional bus structures such as 8085, 80286 and Z80, just to name a few.

The product line utilizing the R6502 processor, recognized world-wide for its high performance, was recently improved by redesigning it in a CMOS process. Enhancements include a 200% improvement in speed and a 20 times reduction in power dissipation.

These products are produced in high volume at a modern state-of-the-art facility located in Newport Beach, California, and are packaged in a newly constructed, fully automated manufacturing facility in Mexicali, Mexico. The class 10,000 clean room environment produces devices to the most stringent industry standards. Rockwell has the organization, systems and support to manufacture products to existing and future quality levels.

In fact, Rockwell is the first and only semiconductor company to offer a 5 year warranty. You can rely on customer satisfaction and service when choosing a Rockwell semiconductor product.



Serving System Requirements

PRODUCT INDEX

1

Section 1
CMOS 8-Bit Microprocessors & Peripherals

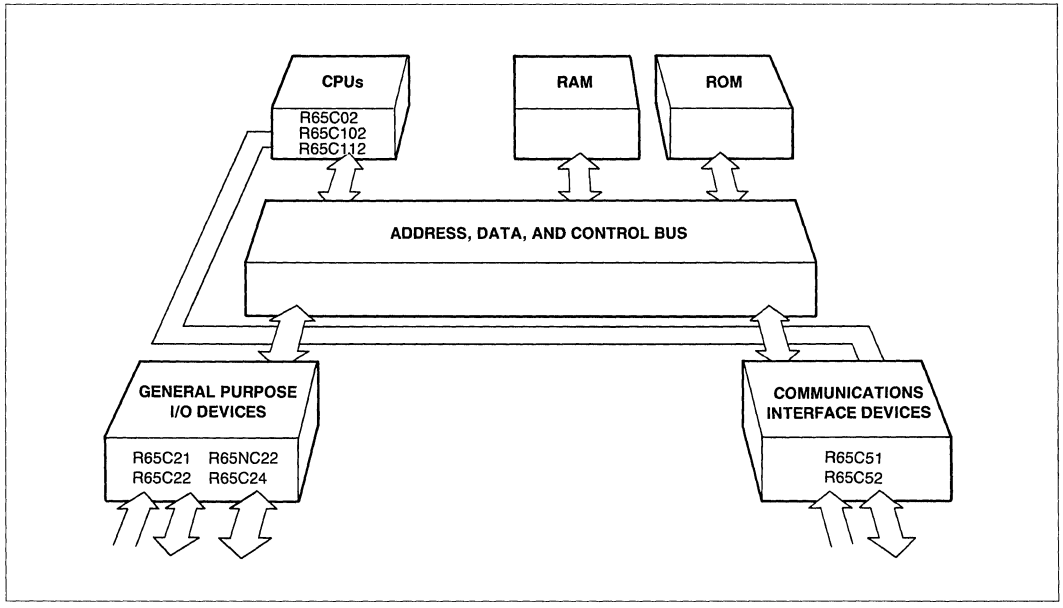
CMOS 8-bit Microprocessors & Peripherals
Fastest Executing — Low Power

There is no CMOS microprocessor family easier to implement than the R65CXX. It is the fastest instruction executing 8-bit family available. It's software compatible with a family of single-chip microcomputers and has three powerful CPUs and peripherals for parallel and serial I/O.

In the 8-bit range, nothing gives faster instruction execution (500 μs) with most parts available in 1, 2, 3 and 4 MHz versions. Thirteen address modes provide the most efficient ways of addressing memory. R65CXX peripherals are system oriented, designed to implement systems with minimum device count.

Because of its inherent characteristics, advanced Rockwell CMOS provides low power consumption, high noise immunity and high speed operation. Its 2 MHz CPU dissipates only 40 mW (compared to 800 mW in NMOS) and requires only 10 mA standby current. Instruction memory requirements are 20% less due to added bit manipulation features.

The entire 8-bit R65CXX family is upward compatible with the 16-bit 68000 bus, software compatible with Rockwell's 8-bit microcomputers, and are the building blocks for a wide range of system applications. It's one of the world's highest performing and lowest cost microprocessors.



CMOS R65CXX Microprocessor Family

Rockwell

R65C02, R65C102 and R65C112 R65C00 Microprocessors (CPU)

1

DESCRIPTION

The 8-bit R65C00 microprocessor family of devices are produced using CMOS silicon gate technology which provides advanced system architecture for performance speed and system cost-effectiveness enhancements over their NMOS counterparts, the R6500 family of microprocessor devices.

Three CPU devices are available. All are software-compatible and provide 64K bytes of memory addressing, two interrupt inputs, and on-chip clock oscillators and/or drivers. All are bus-compatible with the NMOS R6500 family devices.

The CMOS family includes two microprocessors (R65C02 and R65C102) with on-board clock oscillators and drivers and one microprocessor (R65C112) driven by an external clock. The on-chip clock versions are aimed at high performance, low-cost applications where single phase inputs, crystal or RC inputs provide the time base. The slave processor version is geared for multiprocessor system applications where maximum timing control is mandatory. All R65C00 microprocessors are available in ceramic and plastic packaging, operating frequency of 1 MHz, 2 MHz, 3 MHz and 4 MHz, and commercial and industrial temperature versions. All three devices are available in 40-pin DIP or 44-pin PLCC packages.

FEATURES

- CMOS silicon gate technology
- Low Power (4 mA/MHz)
- Software compatible with R6502
- Single 5V ±5% power supply requirements
- Eight-bit parallel processing
- Decimal and binary arithmetic
- True indexing capability
- Programmable stack pointer
- Interrupt capability
- Non-maskable interrupt
- Eight-bit bidirectional data bus
- Memory address range of up to 64K bytes
- "Ready" input
- Direct memory access (DMA) capability
- Memory lock output
- 1 MHz, 2 MHz, 3 MHz, and 4 MHz versions
- Choice of external or on-chip clocks
- On-chip clock options
  —External single clock input
  —Direct crystal input (÷4)
- Commercial and industrial temperature versions
- Pipeline architecture
- Slave processor version (R65C112)

MAJOR FEATURES AND DIFFERENCES

Feature	R65C02	R65C102	R65C112
Pin compatible with NMOS R6502	X		
64K addressable bytes of memory	X	X	X
$\overline{IRQ}$ interrupt	X	X	X
On-chip clock oscillator		X	
External clock only	X		X
TTL level single phase clock input	X	X	
RC time base clock input	X	X	
Crystal time base clock input	X	X	
Single phase clock input			X
Two phase output clock	X	X	
SYNC and RDY signals	X	X	X
Bus Enable ($\overline{BE}$) signal		X	X
Memory Lock ($\overline{ML}$) output signal		X	X
Direct Memory Access (DMA) capacity		X	X
$\overline{NMI}$ interrupt signal	X	X	X

ORDERING INFORMATION

Part Number:

R65C02 ___
R65C102 ___
R65C112 ___

Temp. Range (T_L to T_H)
Blank = 0°C to +70°C
E = −40°C to +85°C
M = −55°C to 125°C

Frequency Range
1 = 1 MHz
2 = 2 MHz
3 = 3 MHz
4 = 4 MHz

Package
C = 40-Pin Ceramic DIP
P = 40-Pin Plastic DIP
J = 44-Pin Plastic Leaded Chip Carrier (PLCC)

INTERFACE SIGNALS

Figure 1 shows the pin assignments for the members of the R65C00 CPU family. All devices are housed in 40-pin ceramic or plastic dual-in-line (DIP) or 44-pin plastic leaded chip carrier (PLCC) packages.

Refer to the timing diagrams (Figures 3, 4, and 5) for the particular device in the following discussion.

CLOCK SIGNALS (R65C02)

The R65C02 requires an external Ø0 clock. See Figure 6 for an example clock circuit. Ø0 is a TTL level input that is used to generate the internal clocks of the R65C02. Two full level output clocks are generated by the R65C02. The Ø2 clock is in phase with Ø0. The Ø1 clock output is 180° out of phase with Ø0. When the input clock is stopped, the CPU is in the standby mode. See Figure 8 for special standby mode considerations.

For non-critical timing configurations, a simple RC or crystal network may be strapped between Ø0 (IN) and Ø1 (OUT).

CLOCK SIGNALS (R65C102)

The R65C102 internal clocks may be generated by a TTL level single phase input, an RC time base input, or a crystal time base input (÷4) using the XTLO and XTLI input pins. See Figure 7 for an example of a crystal time base circuit. Two full level output clocks are generated by the R65C102. The Ø2 clock output provides timing for external R/$\overline{W}$ operations. Addresses are valid after the address delay time (t_{ADS}) referenced to the falling edge of Ø2 (OUT). The Ø4 output is a quadrature output clock that is delayed from the falling edge of the Ø2 clock by delay time t_{AVS}. Using the Ø4 clock, addresses are valid at the rising edge of Ø4.

CLOCK SIGNALS (R65C112)

All internal clock signals for the R65C112 are generated by the input clock signal Ø2 (IN). Since this device is intended to be operated in the slave mode it does not have internal clock generation, but rather requires the external clock Ø2 (IN) from a host device. Figure 7 shows an example of a clock circuit for the R65C112 configured for slave mode.

ADDRESS BUS (A0–A15)

Address lines A0–A15 form a 16-bit address bus for memory and I/O exchanges on the data bus. The output of each address line is TTL compatible, capable of driving one standard TTL load and 130 pF.

DATA BUS (D0–D7)

The data lines (D0–D7) constitute an 8-bit bidirectional data bus used for data exchanges to and from the device and peripherals. The outputs are tri-state buffers capable of driving one TTL load and 130 pF.

BUS ENABLE (BE)

This signal allows external control of the data and the address output buffers and R/$\overline{W}$. For normal operation, BE is high causing the address buffers and R/$\overline{W}$ to be active and the data buffers to be active during a write cycle. For external control, BE is held low to disable the buffers. BE is an asynchronous signal and therefore not related to, or controlled by the CPU internal clock signals. Figure 5 shows timing relationships of BE to R/$\overline{W}$ and address output buffers.

INTERRUPT REQUEST ($\overline{IRQ}$)

This TTL compatible input requests that an interrupt sequence begin within the microprocessor. $\overline{IRQ}$ is sampled at the falling edge of Ø2 prior to the last cycle of the instruction; if the interrupt flag in the processor status register is zero, the current instruction is completed and the interrupt sequence begins during Ø1. The program counter and processor status register are stored in the stack. The microprocessor will then set the interrupt mask flag high so that no further $\overline{IRQ}$s may occur. At the end of this cycle, the program counter low byte will be loaded from address FFFE, and program counter high byte from location FFFF, thus transferring program control to the memory vector located at these addresses. The RDY signal must be in the high state for any interrupt to be recognized. A 3K ohm external resistor should be used for proper wire OR operation.

MEMORY LOCK ($\overline{ML}$)

In a multiprocessor system, the $\overline{ML}$ output indicates the need to defer the rearbitration of the next bus cycle to ensure the integrity of read-modify-write instructions. $\overline{ML}$ goes low during ASL, DEC, INC, LSR, ROL, ROR, RMB, SMB, TRB, TSB memory referencing instructions. This signal is low for the modify and write cycles.

NON-MASKABLE INTERRUPT ($\overline{NMI}$)

A negative-going edge on this input requests that a non-maskable interrupt sequence be generated within the microprocessor. The $\overline{NMI}$ is sampled during Ø2; the current instruction is completed and the interrupt sequence begins during Ø1. The program counter is loaded with the interrupt vector from locations FFFA (low byte) and FFFB (high byte), thereby transferring program control to the non-maskable interrupt routine.

NOTE

Since this interrupt is non-maskable, another $\overline{NMI}$ can occur before the first is finished. Care should be taken when using $\overline{NMI}$ to avoid this.

READY (RDY)

This input allows the user to single-cycle the microprocessor on all cycles including write cycles. A negative transition to the low state, during or coincident with Ø2, will halt the microprocessor with the output address lines reflecting the current address. This condition will remain through a subsequent Ø2 in which the RDY signal is low. This feature allows microprocessor interfacing with low-speed memory as well as direct memory access (DMA).

READ/WRITE (R/$\overline{W}$)

This signal is normally in the high state indicating that the microprocessor is reading data from memory or I/O bus. In the low state the data bus has valid data from the microprocessor to be stored at the addressed memory location.

SET OVERFLOW ($\overline{SO}$)

A negative transition on this line sets the overflow bit (V) in the processor status register. The signal is sampled prior to the rising edge of Ø2 by the $\overline{SO}$ setup time (t_{SOS}).

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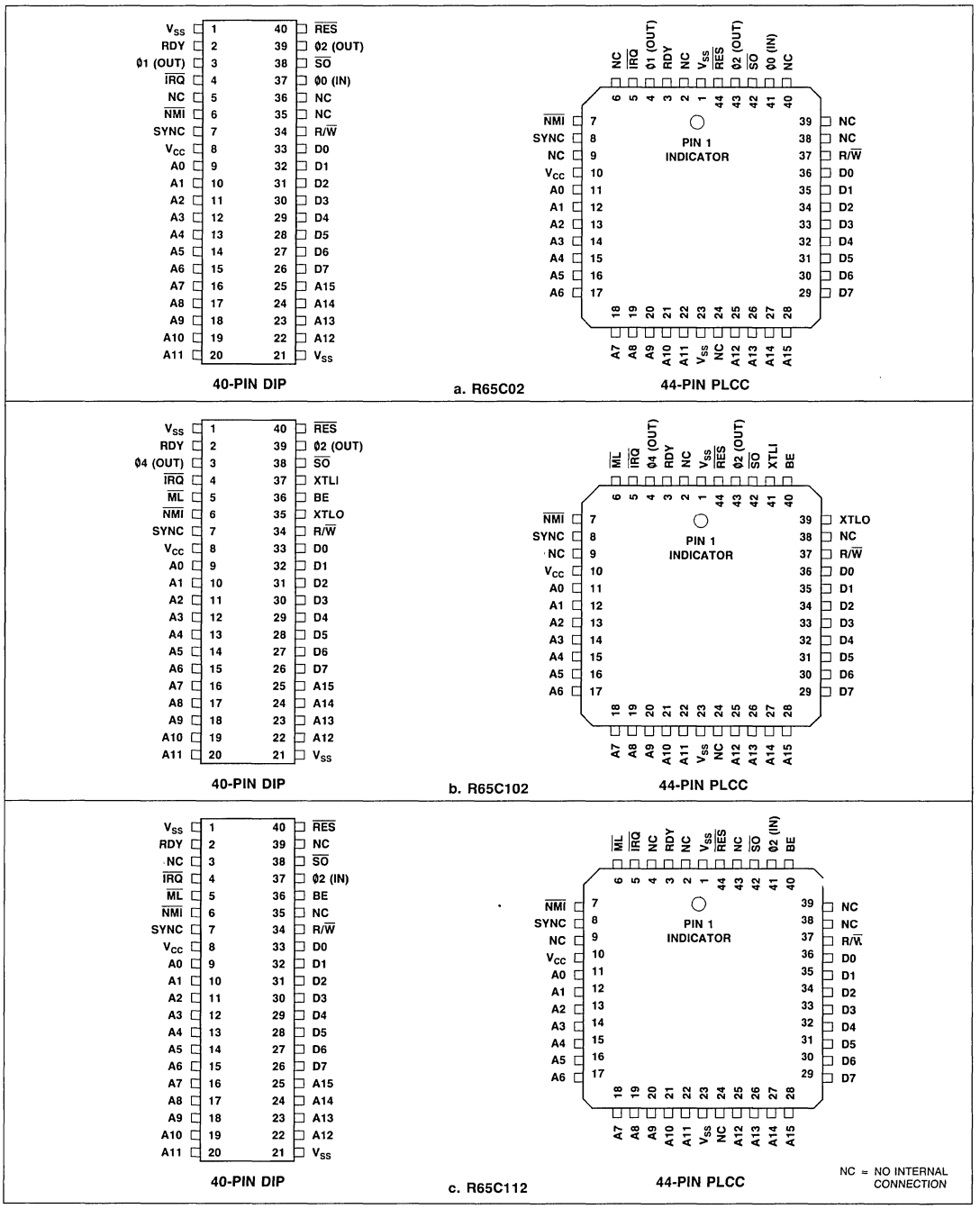


Figure 1. Pin Assignments

RESET ($\overline{RES}$)

This input resets the microprocessor. Reset must be held low for at least two clock cycles after V_{CC} reaches operating voltage from a power down. A positive transition on this pin will then cause an initialization sequence to begin. Likewise, after the system has been operating, a low on this line of at least two cycles will cease microprocessing activity, followed by initialization after the positive edge on $\overline{RES}$.

When a positive edge is detected, there is an initialization sequence lasting seven clock cycles. Then the interrupt mask flag is set, the decimal mode is cleared, and the program counter is loaded with the restart vector from locations FFFC (low byte) and FFFD (high byte). This is the start location for program control. This input should be high in normal operation.

SYNCHRONIZE (SYNC)

This output line identifies those cycles during which the microprocessor is fetching the instruction operation code (OP CODE). The SYNC line goes high during Ø1 of an OP CODE fetch and stays high for the remainder of that cycle. If the RDY line is pulled low during the clock cycle in which SYNC went high, the processor will stop in its current state and will remain in the state until the RDY line goes high. In this manner, the SYNC signal can be used to control RDY to cause single instruction execution.

FUNCTIONAL DESCRIPTION

Figure 2 shows the block diagram of the R65C00 CPU internal architecture for all three devices. With the exception of the crystal oscillator, clock signals, Memory Lock (ML), and Bus Enable (BE) signals, the internal architecture of the three members of the R65C00 CPU of devices is identical. This block diagram supports the following text that describes the function of each of the device's major elements.

CRYSTAL OSCILLATOR (R65C102 Only)

The crystal oscillator, driven by a crystal across XTLO and XTLI, divides the crystal frequency by four to provide the basic Ø2 clock signal that drives the internal clock generator.

CLOCK GENERATOR

The clock generator develops all internal clock signals, and (where applicable) external clock signals, associated with the device. It is the clock generator that drives the timing control unit and the external timing for slave mode operations.

TIMING CONTROL

The timing control unit keeps track of the instruction cycle being monitored. The unit is set to zero each time an instruction fetch is executed and is advanced at the beginning of each phase one clock pulse for as many cycles as is required to complete the instruction. Each data transfer which takes place between the registers depends upon decoding the contents of both the instruction register and the timing control unit.

PROGRAM COUNTER

The 16-bit program counter provides the addresses which step the microprocessor through sequential instructions in a program.

Each time the microprocessor fetches an instruction from program memory, the lower byte of the program counter (PCL) is placed on the low-order bits of the address bus and the higher byte of the program counter (PCH) is placed on the high-order 8 bits. The counter is incremented each time an instruction or data is fetched from program memory.

INSTRUCTION REGISTER AND DECODE

Instructions fetched from memory are gated onto the internal data bus. These instructions are latched into the instruction register, then decoded, along with timing and interrupt signals, to generate control signals for the various registers.

ARITHMETIC AND LOGIC UNIT (ALU)

All arithmetic and logic operations take place in the ALU including incrementing and decrementing internal registers (except the program counter). The ALU has no internal memory and is used only to perform logical and transient numerical operations.

ACCUMULATOR

The accumulator is a general purpose 8-bit register that stores the results of most arithmetic and logic operations, and in addition, the accumulator usually contains one of the two data words used in these operations.

INDEX REGISTERS

There are two 8-bit index registers (X and Y), which may be used to count program steps or to provide an index value to be used in generating an effective address.

When executing an instruction which specifies indexed addressing, the CPU fetches the op code and the base address, and modifies the address by adding the index register to it prior to performing the desired operation. Pre- or post-indexing of indirect addresses is possible (see addressing modes).

STACK POINTER

The stack pointer is an 8-bit register used to control the addressing of the variable-length stack on page one. The stack pointer is automatically incremented and decremented under control of the microprocessor to perform stack manipulations under direction of either the program or interrupts ($\overline{NMI}$ and $\overline{IRQ}$). The stack allows simple implementation of nested subroutines and multiple level interrupts. The stack pointer should be initialized before any interrupts or stack operations occur.

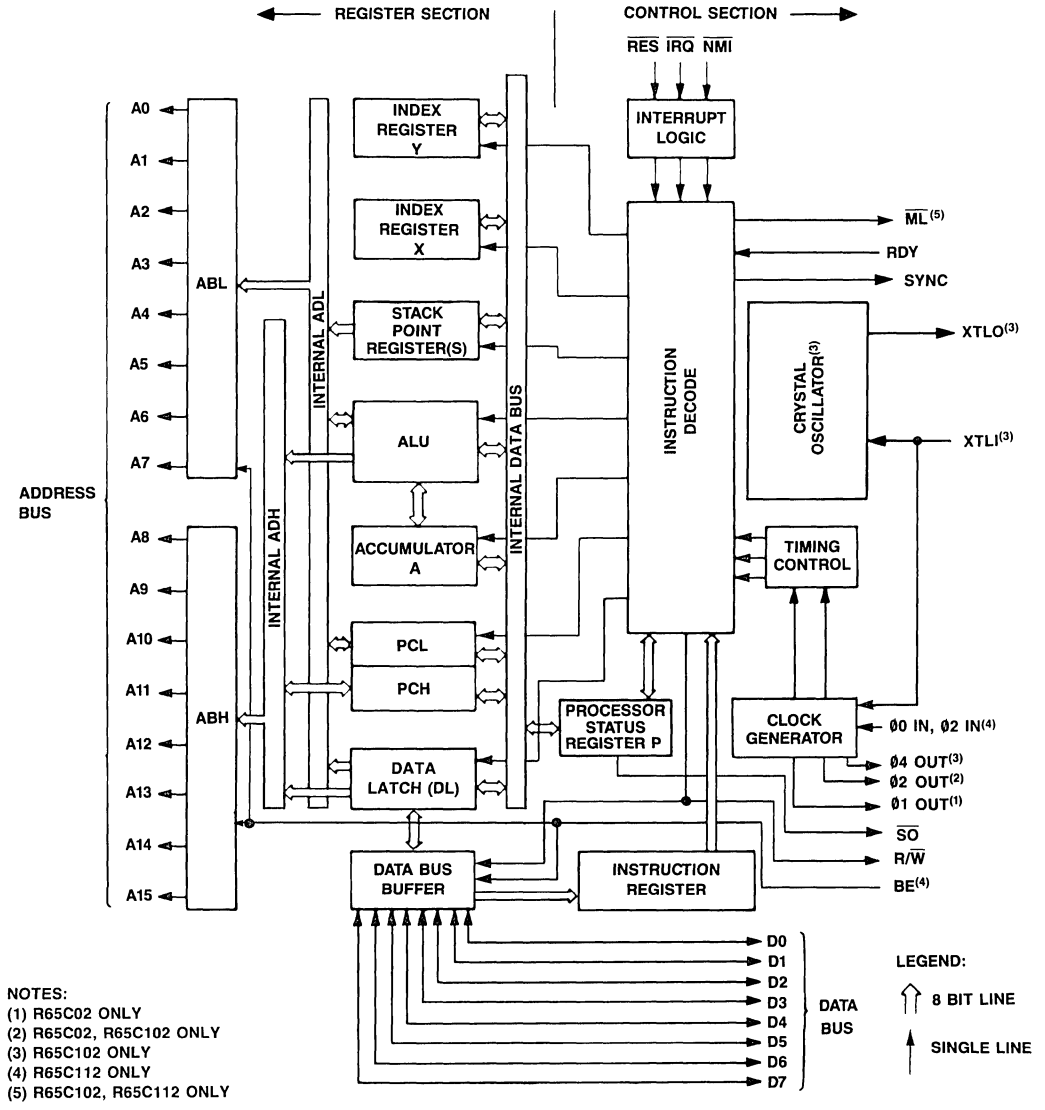
PROCESSOR STATUS REGISTER

The 8-bit processor status register contains seven status flags. Some of the flags are controlled by the program, others may be controlled both by the program and the CPU. The R65C00 instruction set contains a number of conditional branch instructions which are designed to allow testing of these flags.

HARDWARE ENHANCEMENTS

The R65C00 family of CPU devices have incorporated hardware enhancements over their NMOS counterpart, the R6502. These hardware enhancements are:

- The NMOS device would ignore the assertion of a Ready (RDY) during a write operation. The CMOS family will stop the processor during Ø2 clock if RDY is asserted during a write operation.
- On the NMOS device, unused input-only pins ($\overline{IRQ}$, $\overline{NMI}$, RDY, $\overline{RES}$, and $\overline{SO}$) must be connected to a low impedance signal to avoid noise problems. These unused pins on the CMOS devices are internally connected by a high impedance to V_{CC} (approximately 250K ohms).



NOTES:
(1) R65C02 ONLY
(2) R65C02, R65C102 ONLY
(3) R65C102 ONLY
(4) R65C112 ONLY
(5) R65C102, R65C112 ONLY

Figure 2. R65C00 Internal Architecture

ADDRESSING MODES

The R65C00 CPU family has 15 address modes (two more than the NMOS equivalent family). In the following discussion of these addressing modes, a bracketed expression follows the title of the mode. This expression is the term used in the Instruction Set Op Code Matrix table (later in this product description) to make it easier to identify the actual addressing mode used by the instruction.

ACCUMULATOR ADDRESSING [Accum] — This form of addressing is represented with a one byte instruction, implying an operation on the accumulator.

IMMEDIATE ADDRESSING [IMM] — In immediate addressing, the second byte of the instruction contains the operand, with no further memory addressing required.

ABSOLUTE ADDRESSING [ABS] — In absolute addressing, the second byte of the instruction specifies the eight low order bits of the effective address while the third byte specifies the eight high order bits. Thus the absolute addressing mode allows access to the entire 64K bytes of addressable memory.

ZERO PAGE ADDRESSING [ZP] — The zero page instructions allow for shorter code and execution times by fetching only the second byte of the instruction and assuming a zero high address byte. Careful use of the zero page can result in significant increase in code efficiency.

ZERO PAGE INDEXED ADDRESSING [ZP, X or Y] — (X, Y indexing) — This form of addressing is used with the index register and is referred to as "Zero Page, X" or "Zero Page, Y". The effective address is calculated by adding the second byte to the contents of the index register. Since this is a form of "Zero Page" addressing, the content of the second byte references a location in page zero. Additionally, due to the "Zero Page" addressing nature of this mode, no carry is added to the high order eight bits of memory and crossing of page boundaries does not occur.

ABSOLUTE INDEXED ADDRESSING [ABS, X or Y] — (X, Y indexing) — This form of addressing is used in conjunction with X and Y index register and is referred to as "Absolute, X" and "Absolute, Y". The effective address is formed by adding the contents of X or Y to the address contained in the second and third bytes of the instruction. This mode allows the index register to contain the index or count value and the instruction to contain the base address. This type of indexing allows any location referencing and the index to modify fields, resulting in reduced coding and execution time.

INDEXED ABSOLUTE INDIRECT [(ABS, X)]* — The contents of the second and third instruction bytes are added to the X-register. The sixteen-bit result is a memory address containing the effective address. (JMP (ABS, X) only).

IMPLIED ADDRESSING [Implied] — In the implied addressing mode, the address containing the operand is implicitly stated in the operation code of the instruction.

RELATIVE ADDRESSING [Relative] — Relative addressing is used only with branch instructions and establishes a destination for the conditional branch.

The second byte of the instruction becomes the operand which is an "Offset" added to the contents of the lower eight bits of the program counter when the counter is set at the next instruction. The range of the offset is −128 to +127 bytes from the next instruction.

ZERO PAGE RELATIVE ADDRESSING [ZP REL]* — This mode bit tests the zero page location specified for bit set/reset per the mask and performs a conditional relative branch based on the results of the bit test.

INDEXED INDIRECT ADDRESSING [(IND, X)] — In indexed indirect addressing (referred to as (Indirect, X)), the second byte of the instruction is added to the contents of the X index register, discarding the carry. The result of this addition points to a memory location on page zero whose contents are the low order eight bits of the effective address. The next memory location in page zero contains the high order eight bits of the effective address. Both memory locations specifying the high and low order bytes of the effective address must be in page zero.

INDIRECT INDEXED ADDRESSING [(IND), Y] — In indirect indexed addressing (referred to as (Indirect), Y), the second byte of the instruction points to a memory location in page zero. The contents of this memory location are added to the contents of the Y index register, the result being the low order eight bits of the effective address. The carry from this addition is added to the contents of the next page zero memory location, the result being the high order eight bits of the effective address.

ABSOLUTE INDIRECT [(ABS)] — The second byte of the instruction contains the low order eight bits of a memory location. The high order eight bits of that memory location are contained in the third byte of the instruction. The contents of the fully specified memory location are the low order byte of the effective address. The next memory location contains the high order byte of the effective address which is loaded into the sixteen bits of the program counter. (JMP (ABS) only.)

INDIRECT [(IND)]* — The second byte of the instruction contains a zero page address serving as the indirect pointer.

ENHANCEMENTS OVER R6502

The CMOS family of microprocessor devices has been designed with many enhancements over the R6502 NMOS device while maintaining software compatibility. Besides the increased speed and lower power consumption inherent in CMOS technology, the R65C00 family has the following additional characteristics.

- 12 new instructions for a total of 68
- 59 new op codes, for a total of 210
- Two new addressing modes
- Seven software/operational enhancements
- Two hardware enhancements

*These addressing modes are not available to the NMOS CPU family (e.g., the R6502).

INSTRUCTION SET

Table 1 lists the instruction set for the CMOS CPU family in alphabetic order according to mnemonic. Tabe 2 lists the hexadecimal codes for each of the instructions that are new to the CMOS family and were not available in the NMOS R6502 device family. Table 3 lists those instructions that were available on the NMOS family, but have been assigned new addressing modes in the CMOS CPU family.

OPERATIONAL ENHANCEMENTS

Table 4 lists the operational enhancements that have been added to the CMOS family of CPU devices and compares the results with their NMOS R6502 counterpart.

Table 1. Alphabetic Listing of the R65C00 Instruction Set

Mnemonic		Function
(2)	ADC	Add Memory to Accumulator with Carry
(2)	AND	"AND" Memory with Accumulator
	ASL	Shift Left One Bit (Memory or Accumulator)
(1)	BBR	Branch on Bit Reset
(1)	BBS	Branch on Bit Set
	BCC	Branch on Carry Clear
	BCS	Branch on Carry Set
	BEQ	Branch on Result Zero
(2)	BIT	Test Bits in Memory with Accumulator
	BMI	Branch on Result Minus
	BNE	Branch on Result not Zero
	BPL	Branch on Result Plus
(1)	BRA	Branch Always
	BRK	Force Break
	BVC	Branch on Overflow Clear
	BVS	Branch on Overflow Set
	CLC	Clear Carry Flag
	CLD	Clear Decimal Mode
	CLI	Clear Interrupt Disable Bit
	CLV	Clear Overflow Flag
(2)	CMP	Compare Memory and Accumulator
	CPX	Compare Memory and Index X
	CPY	Compare Memory and Index Y
(2)	DEC	Decrement Memory by One
	DEX	Decrement Index X by One
	DEY	Decrement Index Y by One
(2)	EOR	"Exclusive-OR" Memory with Accumulator
(2)	INC	Increment Memory by One
	INX	Increment Index X by One
	INY	Increment Index Y by One
(2)	JMP	Jump to New Location
	JSR	Jump to New Location Saving Return Address
(2)	LDA	Load Accumulator with Memory
	LDX	Load Index X with Memory
	LDY	Load Index Y with Memory
	LSR	Shift One Bit Right (Memory or Accumulator)
	NOP	No Operation
(2)	ORA	"OR" Memory with Accumlator
	PHA	Push Accumulator on Stack
	PHP	Push Processor Status on Stack
(1)	PHX	Push X Register on Stack
(1)	PHY	Push Y Register on Stack
	PLA	Pull Accumulator from Stack
	PLP	Pull Processor Status from Stack
(1)	PLX	Pull X Register from Stack
(1)	PLY	Pull Y Register from Stack
(1)	RMB	Reset Memory Bit
	ROL	Rotate One Bit Left (Memory or Accumulator)
	ROR	Rotate One Bit Right (Memory or Accumulator)
	RTI	Return from Interrupt
	RTS	Return from Subroutine
	SBC	Subtract Memory from Accumulator with Borrow
	SEC	Set Carry Flag
	SED	Set Decimal Mode
	SEI	Set Interrupt Disable Status
(1)	SMB	Set Memory Bit
(2)	STA	Store Accumulator in Memory
	STX	Store Index X in Memory
	STY	Store Index Y in Memory
(1)	STZ	Store Zero
	TAX	Transfer Accumulator to Index X
	TAY	Transfer Accumulator to Index Y
(1)	TRB	Test and Reset Bits
(1)	TSB	Test and Set Bits
	TSX	Transfer Stack Pointer to Index X
	TXA	Transfer Index X to Accumulator
	TXS	Transfer Index X to Stack Register
	TYA	Transfer Index Y to Accumulator

Notes:
(1) Instruction not available on the NMOS family.
(2) R6502 instruction with additional addressing mode(s).

Table 2. Hexadecimal Codes For New Instructions in the R65C00 Microprocessors

Hex	Mnemonic	Description
80	BRA	Branch relative always [Relative]
DA	PHX	Push X on stack [Implied]
5A	PHY	Push Y on stack [Implied]
FA	PLX	Pull X from stack [Implied
7A	PLY	Pull Y from stack [Implied]
9C	STZ	Store zero [Absolute]
9E	STZ	Store zero [ABS, X]
64	STZ	Store zero [ZP]
74	STZ	Store zero [ZP, X]
1C	TRB	Test and reset memory bits with accumulator [ABS]
14	TRB	Test and reset memory bits with accumulator [ZP]
0C	TSB	Test and set memory bits with accumulator [ABS]
04	TSB	Test and set memory bits with accumulator [ZP]
0F-7F(1)	BBR	Branch on bit reset [Bit Manipulation, ZP, REL]
8F-FF(1)	BBS	Branch on bit set [Bit Manipulation, ZP, REL]
07-77(1)	RMB	Reset memory bit [Bit Manipulation, ZP]
87-F7(1)	SMB	Set memory bit [Bit Manipulation, ZP]

Note:
1. Most significant digit change only.

Table 3. Hexadecimal Codes For R65C00 Instructions With New Addressing Modes

Hex	Mnemonic	Description
72	ADC	Add memory to accumulator with carry [(IND)]
32	AND	AND memory with accumulator [(IND)]
3C	BIT	Test memory bits with accumulator [ABS, X]
34	BIT	Test memory bits with accumulator [ZP, X]
89	BIT	Test Immediate with accumulator [IMM]
D2	CMP	Compare memory and accumulator [(IND)]
3A	DEC	Decrement accumulator [Accum]
52	EOR	Exclusive Or memory with accumulator [(IND)]
1A	INC	Increment accumulator [Accum]
7C	JMP	Jump (New addressing mode) [(ABS, X)]
B2	LDA	Load accumulator with memory [(IND)]
12	ORA	OR memory with accumulator [(IND)]
F2	SBC	Subtract Memory from accumulator with borrow [(IND)]
92	STA	Store accumulator in memory [(IND)]

Table 4. R65C00 Operational Enhancements

Function	NMOS R6502 Microprocessor	CMOS R65C00 Family Microprocessor
Indexed addressing across page boundary.	Extra read of invalid address.	Extra read of last instruction byte.
Execution of invalid op codes.	Some terminate only by reset. Results are undefined.	All are NOPs (reserved for future use).
Jump Indirect, operand = XXFF.	Page address does not increment.	Page address increments and adds one additional cycle.
Read/modify/write instructions at effective address.	One read and two write cycles.	Two read and one write cycle.
Decimal flag.	Indeterminate after reset.	Initialized to binary mode (D = 0) after reset and interrupts.
Flags after decimal operation.	Invalid N, V and Z flags.	Valid flag adds one additional cycle.
Interrupt after fetch of BRK instruction.	Interrupt vector is loaded, BRK vector is ignored.	BRK is executed, then interrupt is executed.

INSTRUCTION SET OP CODE MATRIX

The following matrix shows the 210 Op Codes associated with the R65C00 family of CPU devices. The matrix identifies the hexadecimal code, the mnemonic code, the addressing mode, the number of instruction bytes, and the number of machine cycles associated with each Op Code. Also, refer to the instruction set summary for additional information on these Op Codes.

1

MSD \ LSD	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	MSD
0	BRK Implied 1 7	ORA (IND, X) 2 6			TSB ZP 2 5	ORA ZP 2 3	ASL ZP 2 5	RMB0 ZP 2 5	PHP Implied 1 3	ORA IMM 2 2	ASL Accum 1 2		TSB ABS 3 6	ORA ABS 3 4	ASL ABS 3 6	BBR0 ZP 3 5**	0
1	BPL Relative 2 2**	ORA (IND), Y 2 5*	ORA (IND) 2 5		TRB ZP 2 5	ORA ZP, X 2 4	ASL ZP, X 2 6	RMB1 ZP 2 5	CLC Implied 1 2	ORA ABS, Y 3 4*	INC Accum 1 2		TRB ABS 3 6	ORA ABS, X 3 4*	ASL ABS, X 3 7	BBR1 ZP 3 5**	1
2	JSR ABS 3 6	AND (IND, X) 2 6			BIT ZP 2 3	AND ZP 2 3	ROL ZP 2 5	RMB2 ZP 2 5	PLP Implied 1 4	AND IMM 2 2	ROL Accum 1 2		BIT ABS 3 4	AND ABS 3 4	ROL ABS 3 6	BBR2 ZP 3 5**	2
3	BMI Relative 2 2**	AND (IND), Y 2 5*	AND (IND) 2 5		BIT ZP, X 2 4	AND ZP, X 2 4	ROL ZP, X 2 6	RMB3 ZP 2 5	SEC Implied 1 2	AND ABS, Y 3 4*	DEC Accum 1 2		BIT ABS, X 3 4*	AND ABS, X 3 4*	ROL ABS, X 3 7	BBR3 ZP 3 5**	3
4	RTI Implied 1 6	EOR (IND, X) 2 6				EOR ZP 2 3	LSR ZP 2 5	RMB4 ZP 2 5	PHA Implied 1 3	EOR IMM 2 2	LSR Accum 1 2		JMP ABS 3 3	EOR ABS 3 4	LSR ABS 3 6	BBR4 ZP 3 5**	4
5	BVC Relative 2 2**	EOR (IND), Y 2 5*	EOR (IND) 2 5			EOR ZP, X 2 4	LSR ZP, X 2 6	RMB5 ZP 2 5	CLI Implied 1 2	EOR ABS, Y 3 4*	PHY Implied 1 3			EOR ABS, X 3 4*	LSR ABS, X 3 7	BBR5 ZP 3 5**	5
6	RTS Implied 1 6	ADC (IND, X) 2 6†			STZ ZP 2 3	ADC ZP 2 3†	ROR ZP 2 5	RMB6 ZP 2 5	PLA Implied 1 4	ADC IMM 2 2†	ROR Accum 1 2		JMP (ABS) 3 6	ADC ABS 3 4†	ROR ABS 3 6	BBR6 ZP 3 5**	6
7	BVS Relative 2 2**	ADC (IND), Y 2 5*†	ADC (IND) 2 5†		STZ ZP, X 2 4	ADC ZP, X 2 4†	ROR ZP, X 2 6	RMB7 ZP 2 5	SEI Implied 1 2	ADC ABS, Y 3 4*†	PLY Implied 1 4		JMP (ABS, X) 3 6	ADC ABS, X 3 4*†	ROR ABS, X 3 7	BBR7 ZP 3 5**	7
8	BRA Relative 2 3*	STA (IND, X) 2 6			STY ZP 2 3	STA ZP 2 3	STX ZP 2 3	SMB0 ZP 2 5	DEY Implied 1 2	BIT IMM 2 2	TXA Implied 1 2		STY ABS 3 4	STA ABS 3 4	STX ABS 3 4	BBS0 ZP 3 5**	8
9	BCC Relative 2 2**	STA (IND), Y 2 6	STA (IND) 2 5		STY ZP, X 2 4	STA ZP, X 2 4	STX ZP, Y 2 4	SMB1 ZP 2 5	TYA Implied 1 2	STA ABS, Y 3 5	TXS Implied 1 2		STZ ABS 3 4	STA ABS, X 3 5	STZ ABS, X 3 5	BBS1 ZP 3 5**	9
A	LDY IMM 2 2	LDA (IND, X) 2 6	LDX IMM 2 2		LDY ZP 2 3	LDA ZP 2 3	LDX ZP 2 3	SMB2 ZP 2 5	TAY Implied 1 2	LDA IMM 2 2	TAX Implied 1 2		LDY ABS 3 4	LDA ABS 3 4	LDX ABS 3 4	BBS2 ZP 3 5**	A
B	BCS Relative 2 2**	LDA (IND), Y 2 5*	LDA (IND) 2 5		LDY ZP, X 2 4	LDA ZP, X 2 4	LDX ZP, Y 2 4	SMB3 ZP 2 5	CLV Implied 1 2	LDA ABS, Y 3 4*	TSX Implied 1 2		LDY ABS, X 3 4*	LDA ABS, X 3 4*	LDX ABS, Y 3 4*	BBS3 ZP 3 5**	B
C	CPY IMM 2 2	CMP (IND, X) 2 6			CPY ZP 2 3	CMP ZP 2 3	DEC ZP 2 5	SMB4 ZP 2 5	INY Implied 1 2	CMP IMM 2 2	DEX Implied 1 2		CPY ABS 3 4	CMP ABS 3 4	DEC ABS 3 6	BBS4 ZP 3 5**	C
D	BNE Relative 2 2**	CMP (IND), Y 2 5*	CMP (IND) 2 5			CMP ZP, X 2 4	DEC ZP, X 2 6	SMB5 ZP 2 5	CLD Implied 1 2	CMP ABS, Y 3 4*	PHX Implied 1 3			CMP ABS, X 3 4*	DEC ABS, X 3 7	BBS5 ZP 3 5**	D
E	CPX IMM 2 2	SBC (IND, X) 2 6†			CPX ZP 2 3	SBC ZP 2 3†	INC ZP 2 5	SMB6 ZP 2 5	INX Implied 1 2	SBC IMM 2 2†	NOP Implied 1 2		CPX ABS 3 4	SBC ABS 3 4†	INC ABS 3 6	BBS6 ZP 3 5**	E
F	BEQ Relative 2 2**	SBC (IND), Y 2 5*†	SBC (IND) 2 5†			SBC ZP, X 2 4†	INC ZP, X 2 6	SMB7 ZP 2 5	SED Implied 1 2	SBC ABS, Y 3 4*†	PLX Implied 1 4			SBC ABS, X 3 4*†	INC ABS, X 3 7	BBS7 ZP 3 5**	F
	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	

— New Opcode

0
BRK — OP Code
0 Implied — Addressing Mode
1 7 — Instruction Bytes; Machine Cycles

†Add 1 to N if in decimal mode.
*Add 1 to N if page boundary is crossed.
**Add 1 to N if branch occurs to same page;
Add 2 to N if branch occurs to different page.

INSTRUCTION SET SUMMARY

MNEMONIC	OPERATION	IMMEDIATE OP	IMMEDIATE n	IMMEDIATE #	ABSOLUTE OP	ABSOLUTE n	ABSOLUTE #	ZERO PAGE OP	ZERO PAGE n	ZERO PAGE #	ZP REL OP	ZP REL n	ZP REL #	ACCUM. OP	ACCUM. n	ACCUM. #	IMPLIED OP	IMPLIED n	IMPLIED #	(IND, X) OP	(IND, X) n	(IND, X) #	(IND), Y OP	(IND), Y n	(IND), Y #	Z. PAGE, X OP	Z. PAGE, X n	Z. PAGE, X #	ABS, X OP	ABS, X n	ABS, X #	(ABS, X) OP	(ABS, X) n	(ABS, X) #	ABS, Y OP	ABS, Y n	ABS, Y #	RELATIVE OP	RELATIVE n	RELATIVE #	(IND) OP	(IND) n	(IND) #	Z. PAGE, Y OP	Z. PAGE, Y n	Z. PAGE, Y #	PROCESSOR STATUS CODES 7	6	5	4	3	2	1	0
		OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	N	V	.	B	D	I	Z	C
ADC	A + M + C → A (1) (5) (7)	69	2	2	6D	4	3	65	3	2										61	6	2	71	5	2	75	4	2	7D	4	3				79	4	3				72	5	2				N	V					Z	C
AND	A M → A (1)	29	2	2	2D	4	3	25	3	2										21	6	2	31	5	2	35	4	2	3D	4	3				39	4	3				32	5	2				N						Z	
ASL	C ← [7 … Ø] ← Ø				ØE	6	3	Ø6	5	2				ØA	2	1										16	6	2	1E	7	3																N						Z	C
BBR [#(Ø-7)]	Branch on $M_n = Ø$										ØF-7F	5	3																																											
BBS [#(Ø-7)]	Branch on $M_n = 1$										8F-FF	5	3																																											
BCC	Branch on C = Ø (2)																																					9Ø	2	2												
BCS	Branch on C = 1 (2)																																					BØ	2	2												
BEQ	Branch on Z = 1 (2)																																					FØ	2	2												
BIT	A > M (6)	89	2	2	2C	4	3	24	3	2																34	4	2	3C	4	3																M$_7$	M$_6$					Z	
BMI	Branch on N = 1 (2)																																					3Ø	2	2												
BNE	Branch on Z = Ø (2)																																					DØ	2	2												
BPL	Branch on N = Ø (2)																																					1Ø	2	2												
BRA	Branch Always (2)																																					8Ø	3	2												
BRK	Break																ØØ	7	1																																				
BVC	Branch on V = Ø (2)																																					5Ø	2	2												
BVS	Branch on V = 1 (2)																																					7Ø	2	2												
CLC	Ø → C																18	2	1																																				
CLD	Ø → D																D8	2	1																																			
CLI	Ø → I																58	2	1																																			
CLV	Ø → V																B8	2	1																																			
CMP	A − M	C9	2	2	CD	4	3	C5	3	2										C1	6	2	D1	5	2	D5	4	2	DD	4	3				D9	4	3				D2	5	2				N						Z	C
CPX	X − M	E0	2	2	EC	4	3	E4	3	2																																												
CPY	Y − M	C0	2	2	CC	4	3	C4	3	2																																												
DEC	M − 1 → M or A − 1 → A				CE	6	3	C6	5	2				3A	2	1										D6	6	2	DE	7	3																						
DEX	X − 1 → X																CA	2	1																																		
DEY	Y − 1 → Y																88	2	1																																		
EOR	A ⊻ M → A (1)	49	2	2	4D	4	3	45	3	2										41	6	2	51	5	2	55	4	2	5D	4	3				59	4	3				52	5	2				N						Z	
INC	M + 1 → M or A + 1 → A				EE	6	3	E6	5	2				1A	2	1										F6	6	2	FE	7	3																						
INX	X + 1 → X																E8	2	1																																		
INY	Y + 1 → Y																C8	2	1																																		
JMP	Jump to New Loc (8)				4C	3	3																								7C	6	3																			
JSR	Jump Sub				20	6	3																																														
LDA	M → A (1)	A9	2	2	AD	4	3	A5	3	2										A1	6	2	B1	5	2	B5	4	2	BD	4	3				B9	4	3				B2	5	2				N						Z	
LDX	M → X (1)	A2	2	2	AE	4	3	A6	3	2																									BE	4	3														
LDY	M → Y (1)	A0	2	2	AC	4	3	A4	3	2																B4	4	2	BC	4	3																						
LSR	Ø → [7 … Ø] → C				4E	6	3	46	5	2				4A	2	1									56	6	2	5E	7	3																						
NOP	No Operation																																																			
ORA	A ∨ M → A (1)	09	2	2	0D	4	3	05	3	2										01	6	2	11	5	2	15	4	2	1D	4	3				19	4	3				12	5	2				N						Z	
PHA	A → Ms S − 1 → S																48	3	1																																		
PHP	P → Ms S − 1 → S																08	3	1																																		
PHX	X → Ms S − 1 → S																DA	3	1																																		
PHY	Y → Ms S − 1 → S																5A	3	1																																		
PLA	S + 1 → S Ms → A																68	4	1																																N						Z	
PLP	S + 1 → S Ms → P																28	4	1																																(Restored)							
PLX	S + 1 → S Ms → X																FA	4	1																																N						Z	
PLY	S + 1 → S Ms → Y																7A	4	1																																N						Z	
RMB[#(Ø-7)]	Ø → M_n (4)							07-77	5	2																																												
ROL	[7 … Ø] ← C				2E	6	3	26	5	2				2A	2	1									36	6	2	3E	7	3																						
ROR	C → [7 … Ø]				6E	6	3	66	5	2				6A	2	1									76	6	2	7E	7	3																						
RTI	Rtrn Int																40	6	1																																(Restored)							
RTS	Rtrn Sub																60	6	1																																				
SBC	A − M − C → A (1) (3) (5)	E9	2	2	ED	4	3	E5	3	2										E1	6	2	F1	5	2	F5	4	2	FD	4	3				F9	4	3				F2	5	2				N	V					Z	C
SEC	1 → C																38	2	1																																			
SED	1 → D																F8	2	1																																			
SEI	1 → I																78	2	1																																			
SMB[#(Ø-7)]	1 → M_n (4)							87-F7	5	2																																												
STA	A → M				8D	4	3	85	3	2										81	6	2	91	6	2	95	4	2	9D	5	3				99	5	3				92	5	2											
STX	X → M				8E	4	3	86	3	2																																												
STY	Y → M				8C	4	3	84	3	2																94	4	2																										
STZ	Ø → M				9C	4	3	64	3	2																74	4	2	9E	5	3																						
TAX	A → X																AA	2	1																																N						Z	
TAY	A → Y																A8	2	1																																N						Z	
TRB	Ā ∧ M → M				1C	6	3	14	5	2																																											
TSB	A ∨ M → M				0C	6	3	04	5	2																																											
TSX	S → X																BA	2	1																																N						Z	
TXA	X → A																8A	2	1																																N						Z	
TXS	X → S																9A	2	1																																				
TYA	Y → A																98	2	1																																N						Z	

Notes:

1. Add 1 to N if page boundary is crossed.
2. Add 1 to N if branch occurs to same page.
   Add 2 to N if branch occurs to different page.
3. Carry not ($\overline{C}$) = Borrow.
4. Effects 8-bit data field of the specified zero page address.
5. Add 1 to N if in Decimal Mode.
6. On the Bit immediate instruction, the results of the M_7 and M_6 bits (N and V flags) are indeterminate and should be considered invalid.
7. If in Decimal Mode, Z flag is invalid. Accumulator must be checked for zero result.
8. JMP (OP Code 6C) is an Absolute Indirect Addressing Mode (ABS).

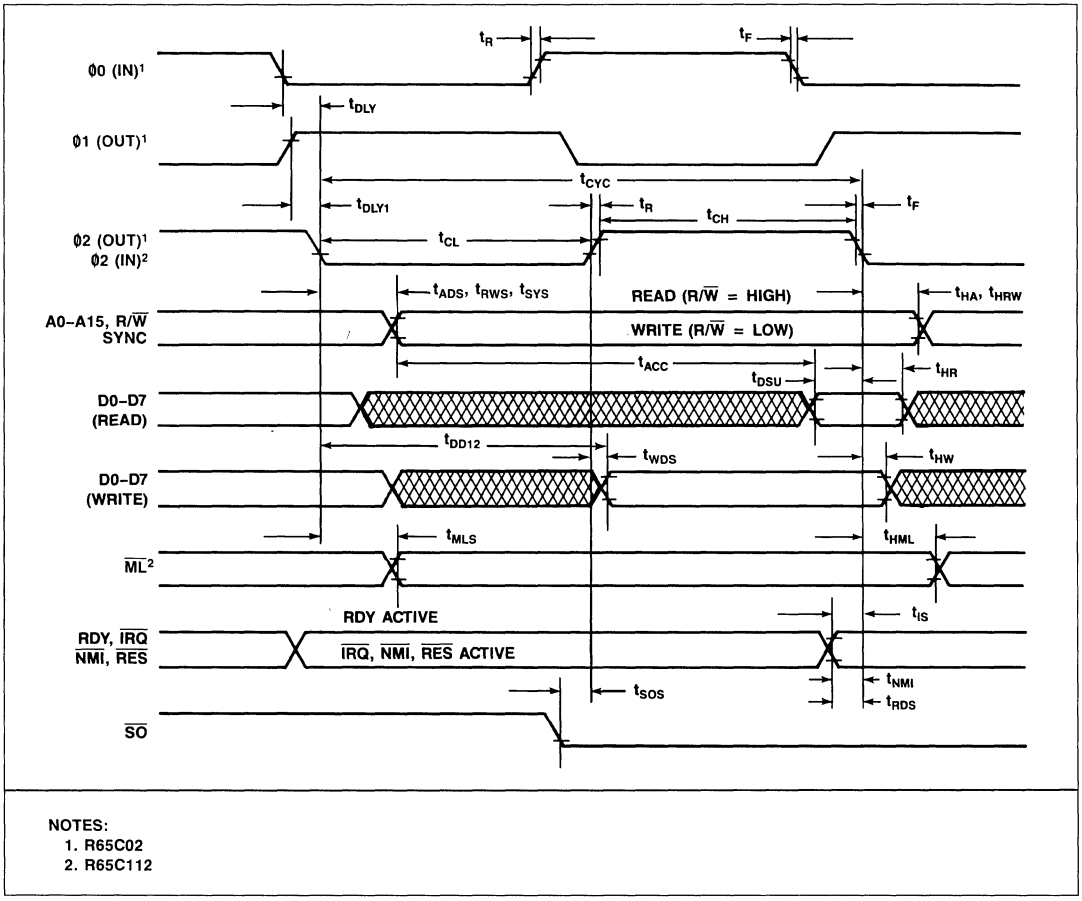
LEGEND

X	= Index X	M_6	= Memory Bit 6
Y	= Index Y	•	= Add
A	= Accumulator	−	= Subtract
M	= Memory per effective address	∧	= And
M_s	= Memory per stack pointer	∨	= Or
M_n	= Selecter zero page memory bit	⊻	= Exclusive or
M_7	= Memory Bit 7	n	= Number of cycles
		#	= Number of Bytes

SWITCHING CHARACTERISTICS (Over operating conditions unless otherwise noted)

Parameter	Symbol	1 MHz		2 MHz		3 MHz		4 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
CLOCK TIMING										
Ø2 Cycle Time	t_{CYC}	1000	Note 1	500	Note 1	333	Note 1	250	Note 1	ns
Ø2 Low Pulse Width	t_{CL}	430	5000	210	5000	150	5000	100	5000	ns
Ø2 High Pulse Width	t_{CH}	450	—	220	—	160	—	110	—	ns
Ø0 Low to Ø2 Low Skew[2]	t_{DLY}	—	50	—	50	—	40	—	30	ns
Ø2 Low to Ø1 High Skew[2]	t_{DLY1}	-20	20	-20	20	-20	20	-20	20	ns
XTLI High to Ø2 Low[4]	t_{DXI}	—	100	—	100	—	100	—	100	ns
XTLO Low to Ø2 Low[4]	t_{DXO}	—	75	—	75	—	75	—	75	ns
Ø2 Low to Ø4 High Delay[4]	t_{AVS}	—	250	—	125	—	85	—	65	ns
Ø4 Low Pulse Width[4]	$t_{Ø4L}$	430	—	210	—	150	—	100	—	ns
Ø4 High Pulse Width[4]	$t_{Ø4H}$	450	5000	220	5000	160	5000	110	5000	ns
Clock Rise and Fall Times	t_R, t_F	—	25	—	20	—	15	—	12	ns
READ/WRITE TIMING										
R/$\overline{W}$ Delay Time	t_{RWS}	—	125	—	100	—	85	—	70	ns
R/$\overline{W}$ Hold Time	t_{HRW}	15	—	15	—	15	—	15	—	ns
Address Delay Time	t_{ADS}	—	125	—	100	—	85	—	70	ns
Address Valid to Ø4 High[4]	$t_{AØ4}$	100	—	25	—	10	—	0	—	ns
Address Hold Time	t_{HA}	15	—	15	—	15	—	15	—	ns
Read Access Time	t_{ACC}	775	—	340	—	215	—	160	—	ns
Read Data Setup Time	t_{DSU}	100	—	60	—	40	—	30	—	ns
Read Data Hold Time	t_{HR}	10	—	10	—	10	—	10	—	ns
Write Data Delay Time[2]	t_{WDS}	—	200	—	110	—	85	—	55	ns
Write Data Delay Time[4]	t_{DDW}	—	200	—	110	—	85	—	65	ns
Write Data Delay Time[6]	t_{DD12}	—	450	—	235	—	170	—	120	ns
Write Data Hold Time	t_{HW}	30	—	30	—	30	—	30	—	ns
CONTROL LINE TIMING										
SYNC Delay	t_{SYS}	—	125	—	100	—	85	—	70	ns
RDY Setup Time	t_{RDS}	200	—	110	—	80	—	60	—	ns
$\overline{SO}$ Setup Time	t_{SOS}	75	—	50	—	40	—	30	—	ns
ML Delay Time[5]	t_{MLS}	—	125	—	100	—	85	—	70	ns
ML Hold Time[4]	t_{HML}	10	—	10	—	10	—	10	—	ns
ML Hold Time[6]	t_{HML}	10	—	10	—	10	—	10	—	ns
BE Delay Time[5][8]	t_{BE}	—	40	—	40	—	40	—	40	ns
$\overline{IRQ}$, $\overline{RES}$ Setup Time	t_{IS}	200	—	110	—	80	—	60	—	ns
$\overline{NMI}$ Setup Time	t_{NMI}	300	—	200	—	170	—	150	—	ns

Notes:
1. R65C02 and R65C102 minimum operating frequency is limited by Ø2 low pulse width. All processors can be stopped with Ø2 held high.
2. R65C02 only.
3. Note 3 deleted.
4. R65C102 only.
5. R65C102 and R65C112 only.
6. R65C112 only.
7. Measurement points shown are 0.8V (low) and 2.0V (high) for outputs and 1.5V (low and high) for inputs, unless otherwise specified.
8. BE signal is asynchronous.



NOTES:
1. R65C02
2. R65C112

Figure 3. Timing Diagram for the R65C02 and R65C112

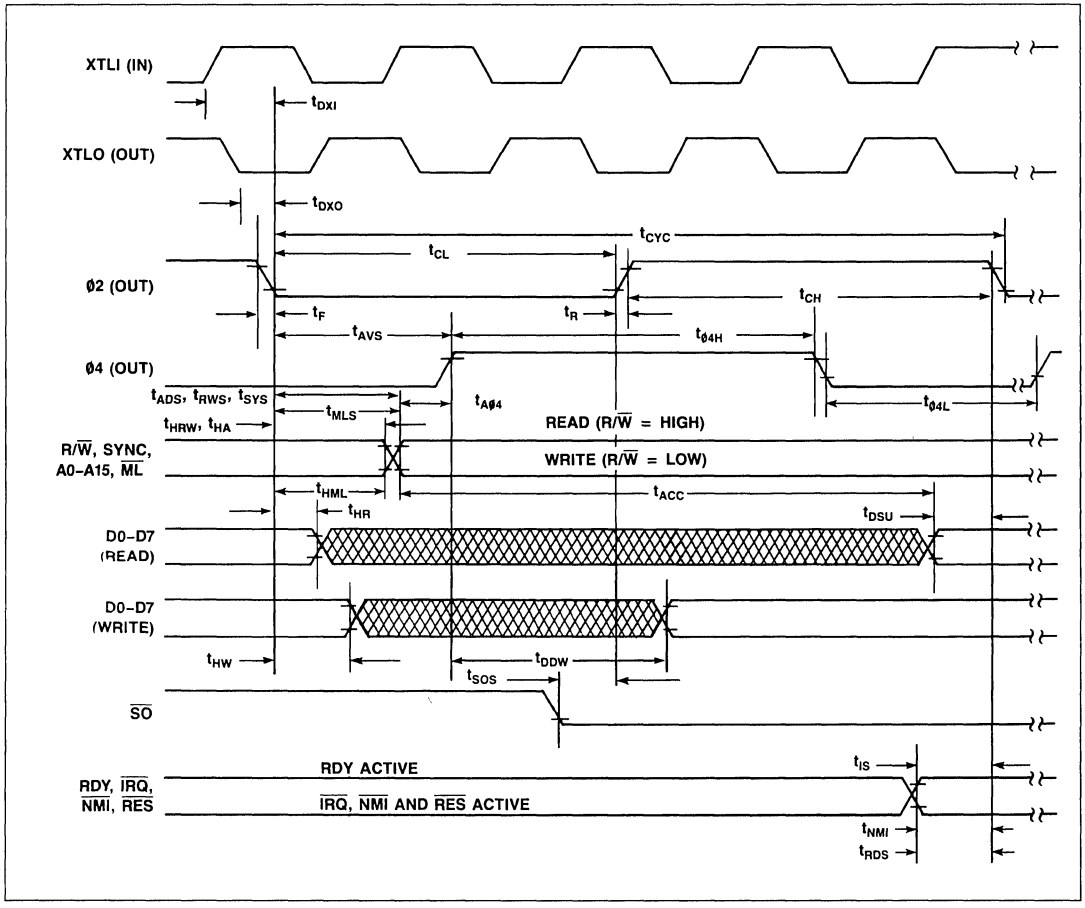
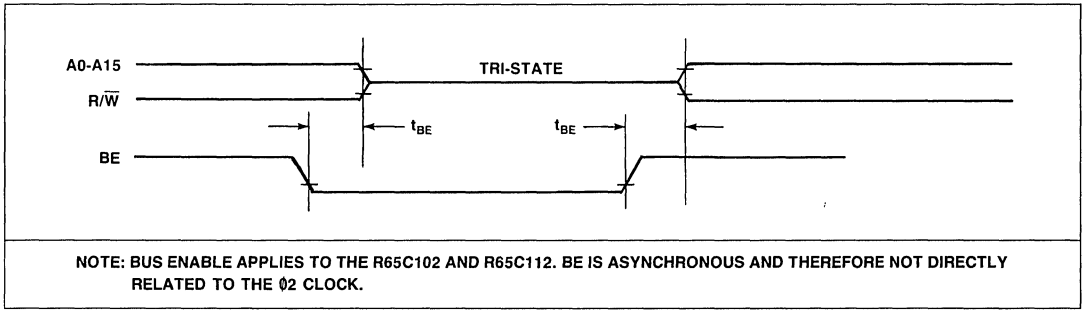


Figure 4. Timing Diagram for the R65C102



NOTE: BUS ENABLE APPLIES TO THE R65C102 AND R65C112. BE IS ASYNCHRONOUS AND THEREFORE NOT DIRECTLY RELATED TO THE Ø2 CLOCK.

Figure 5. Timing Diagram for Bus Enable (BE)

CLOCK/CRYSTAL CONSIDERATIONS

A crystal controlled time base generator circuit should be used to drive Ø0 (IN) (R65C02) or the XTLI and XTLO (R65C102) inputs. Alternatively, a TTL level clock input to XTLI may be used, with XTLO floating.

Figure 6 shows a time base generation scheme, for a 4 MHz operation of the R65C02, that has been tested and proven reliable for normal environments.

Figure 7 shows a possible external clock scheme for a R65C102 and R65C112 master/slave configuration.

The on-chip oscillator is designed for a parallel resonant crystal connected between XTLI and XTLO pins. The equivalent oscillator circuit is shown in Figure 7.

A parallel resonant crystal is specified by its load capacitance and series resonant resistance. For proper oscillator operation, the load capacitance (C_L), series resistance (R_S) and the crystal resonant frequency (F) must meet the following two relations:

$$(C + 5) = 2C_L \quad \text{or} \quad C = 2C_L - 5$$

$$R_S \leq R_{Smax} = \frac{2 \times 10^6}{(FC_L)^2}$$

where: F is in MHz, C and C_L is in pF, and R is in ohms.

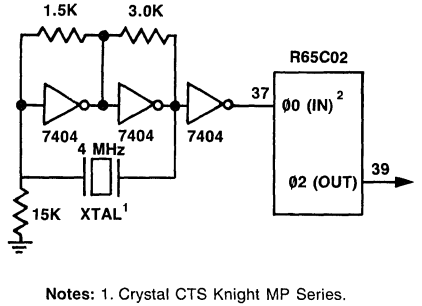
To select a parallel resonant crystal for the oscillator, first select the load capacitance from a crystal manufacturer's catalog. Next, calculate R_{Smax} based on F and C_L. The selected crystal must have a R_S less than the R_{Smax}.

For example, if C_L = 30 pF for a 4 MHz parallel resonant crystal, then

$$C = (2 \times 30) - 5 = 55 \text{ pF}$$
(use standard value of 56 pF)

The series resistance of the crystal must be less than

$$R_{Smax} = \frac{2 \times 10^6}{(4 \times 30)^2} = 138 \text{ ohms}$$

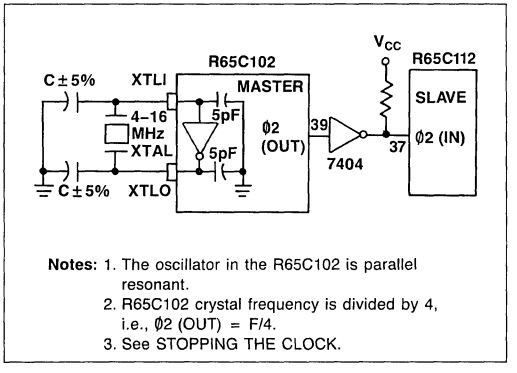


Notes: 1. Crystal CTS Knight MP Series.
2. See STOPPING THE CLOCK.

Figure 6. Example of R65C02 External Time Base Generator Circuit

NOTE

As with any clock oscilltor circuit, stray capacitance due to board layout can affect circuit operation requiring "fine tuning" (e.g. component repositioning or value change) of the circuits shown in Figures 6 and 7. Shunt capacitance (C) includes stray capacitance.

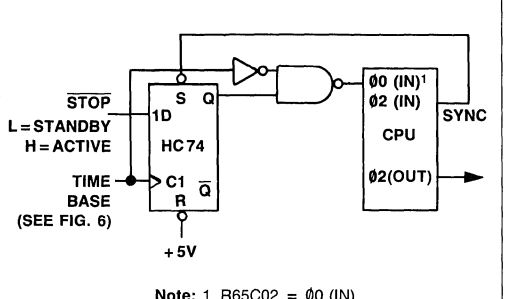


Notes: 1. The oscillator in the R65C102 is parallel resonant.
2. R65C102 crystal frequency is divided by 4, i.e., Ø2 (OUT) = F/4.
3. See STOPPING THE CLOCK.

Figure 7. Example of R65C102/R65C112 Master/Slave Clock Circuit

STOPPING THE CLOCK-STANDBY MODE

Caution must be exercised when configuring the R65C02 or R65C112 in the standby mode (i.e., Ø0 IN or Ø2 IN clock stopped). The input clock can be held in the high state indefinitely; however, if the input clock is held in the low state longer than 5 microseconds, internal register and data status can be lost. Figure 8 shows a circuit that will stop the Ø0 IN (R65C02) or Ø2 IN (R65C112) clock in the high state during standby mode.



Note: 1. R65C02 = Ø0 (IN)
R65C112 = Ø2 (IN)

Figure 8. Stopping the Clock (Standby Mode) Circuit

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to +7.0	Vdc
Input Voltage	V_{IN}	−0.3 to V_{CC} +0.3	Vdc
Output Voltage	V_{OUT}	−0.3 to V_{CC} +0.3	Vdc
Storage Temperature	T_{STG}	−55 to +150	°C

*NOTE: Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the other sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING CONDITIONS

Parameter	Symbol	Value
Supply Voltage	V_{CC}	5 Vdc ±5%
Operating Temperature (Ambient) Commercial Industrial Military	T_L to T_H	 0°C to 70°C −40°C to +85°C −55°C to +125°C

ELECTRICAL CHARACTERISTICS

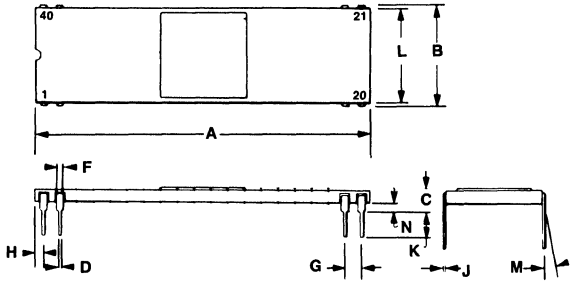
(Over operating conditions unless otherwise noted)

Parameter	Symbol	Min	Typ[4]	Max	Unit	Test Conditions
Input High Voltage −40°C to 85°C −55°C to 125°C	V_{IH}	 2.0 2.4		 V_{CC} +0.3 V_{CC} +0.3	V	
Input Low Voltage −40°C to 85°C −55°C to 125°C	V_{IL}	 −0.3 −0.3		 +0.8 +0.4	V	
Input High Voltage Ø0 R65C02)	V_{IH0}	2.4		V_{CC} +0.3	V	
Input Low Voltage Ø0 (R65C02)	V_{IL0}	−0.3		+0.4	V	
Input High Voltage Ø2 (IN) (R65C112)	V_{IH2}	V_{CC} −0.4		V_{CC} +0.3	V	
Input Low Voltage Ø2 (IN) (R65C112)	V_{IL2}	−0.3		+0.4	V	
Input Leakage Current $\overline{NMI}$, $\overline{IRQ}$, BE, RDY, $\overline{RES}$, $\overline{SO}$ Ø2 (IN), Ø0 (IN), XTLI	I_{IN}	 — —		 −50 1.0	µA	V_{IN} = 0V to 5.25V V_{CC} = 0V
Three-State (Off State) Input Current Data Lines	I_{TSI}	 —		 10	µA	V_{IN} = 0.4V to 2.4V V_{CC} = 5.25V
Output High Voltage SYNC, Data, A0–A15, R/$\overline{W}$, Ø1 (OUT), Ø2 (OUT), Ø4 (OUT), $\overline{ML}$	V_{OH}	2.4		—	V	V_{CC} = 4.75V I_{LOAD} = −100 µA
Output Low Voltage SYNC, Data, A0–A15, R/$\overline{W}$, Ø1 (OUT), Ø2 (OUT), Ø4 (OUT), $\overline{ML}$	V_{OL}	 —		+0.4	V	V_{CC} = 4.75V I_{LOAD} = 1.6 mA
Supply Current Standby[4] Active (R65C02) Active (R65C102) Active (R65C112) Low Power (R65C02) Low Power (R65C102) Low Power (R65C112)	I_{CC}	 — — — — — — —	 2 2.6 5 2 1.5 3 0.7	 10 4 7 4 2 5 1	 µA mA/MHz mA/MHz mA/MHz mA/MHz mA/MHz mA/MHz	V_{CC} = 5.0V RDY = 0 RDY = 0 RDY = 0
Capacitance $\overline{NMI}$, $\overline{IRQ}$, $\overline{SO}$, BE, RDY SYNC, Data, A0–A15, R/$\overline{W}$, Ø1 (OUT), Ø2 (OUT), Ø4 (OUT), $\overline{ML}$, XTLO Ø0 (IN), XTLI Ø2 (IN)	 C_{IN} C_{OUT} C_0 C_2	 — — — —		 7 10 10 30	pF	V_{CC} = 5.0V V_{IN} = 0V V_{IN} = 0V f = 1 MHz T_A = 25°C

Notes:
1. All units are direct current (dc).
2. Negative sign indicates outward current flow, positive indicates inward flow.
3. $\overline{IRQ}$ and $\overline{NMI}$ require external pull-up resistor.
4. Typical values shown for V_{CC} = 5.0V and T_A = 25°C.

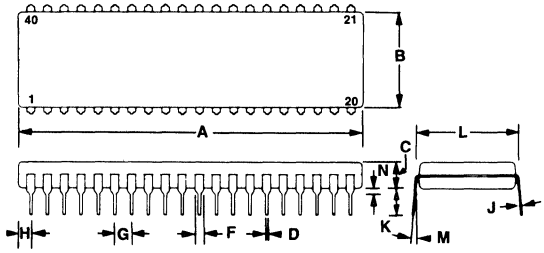
PACKAGE DIMENSIONS

40-PIN CERAMIC DIP



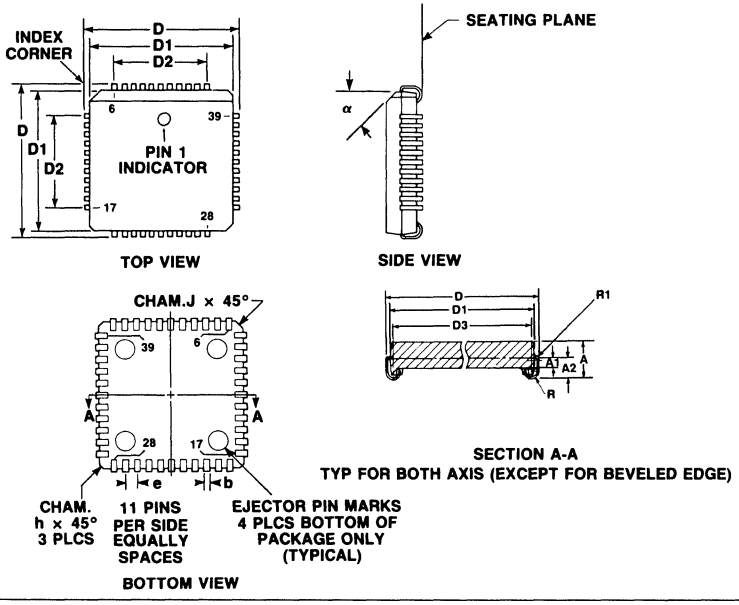
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	50.29	51.31	1.980	2.020
B	15.11	15.88	0.595	0.625
C	2.54	4.19	0.100	0.165
D	0.38	0.53	0.015	0.021
F	0.76	1.27	0.030	0.050
G	2.54 BSC		0.100 BSC	
H	0.76	1.78	0.030	0.070
J	0.20	0.33	0.008	0.013
K	2.54	4.19	0.100	0.165
L	14.60	15.37	0.575	0.605
M	0°	10°	0°	10°
N	0.51	1.52	0.020	0.060

40-PIN PLASTIC DIP



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	51.82	52.32	2.040	2.060
B	13.46	13.97	0.530	0.550
C	3.56	5.08	0.140	0.200
D	0.38	0.53	0.015	0.021
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.30	0.008	0.012
K	3.30	4.32	0.130	0.170
L	15.24 BSC		0.600 BSC	
M	7°	10°	7°	10°
N	0.51	1.02	0.020	0.040

44-PIN PLASTIC LEADED CHIP CARRIER (PLCC)



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.14	4.39	0.163	0.173
A1	1.37	1.47	0.054	0.058
A2	2.31	2.46	0.091	0.097
b	0.457 TYP		0.018 TYP	
D	17.45	17.60	0.687	0.693
D1	16.46	16.56	0.648	0.652
D2	12.62	12.78	0.497	0.503
D3	15.75 REF		0.620 REF	
e	1.27 BSC		0.050 BSC	
h	1.15 TYP		0.045 TYP	
J	0.25 TYP		0.010 TYP	
α	45° TYP		45° TYP	
R	0.89 TYP		0.035 TYP	
R1	0.25 TYP		0.010 TYP	

Rockwell

R65C21
Peripheral Interface Adapter (PIA)

1

DESCRIPTION

The R65C21 Peripheral Interface Adapter (PIA) is designed to solve a broad range of peripheral control problems in the implementation of microcomputer systems. This device allows a very effective trade-off between software and hareware by providing significant capability and flexibility in a low cost chip. When coupled with the power and speed of the R6500, R6500/* or R65C00 family of microprocessors, the R65C21 allows implementation of very complex systems at a minimum overall cost.

Control of peripheral devices is handled primarily through two 8-bit bidirectional ports. Each of these lines can be programmed to act as either an input or an output. In addition, four peripheral control/interrupt input lines are provided. These lines can be used to interrupt the processor or to "handshake" data between the processor and a peripheral device.

FEATURES

- Low power CMOS N-well silicon gate technology
- Direct replacement for NMOS R6520 or MC6821 PIA
- Two 8-bit bidirectional I/O ports with individual data direction control
- Automatic "Handshake" control of data transfers
- Two interrupts (one for each port) with program control
- 1, 2, 3, and 4 MHz versions
- Commercial and industrial temperature range versions
- Wide variety of packages
  - — 40-pin plastic and ceramic DIP
  - — 44-pin plastic leaded chip carrier (PLCC)
- Single +5 Vdc power requirement
- Compatible with the R6500, R6500/* and R65C00 family of microprocessors

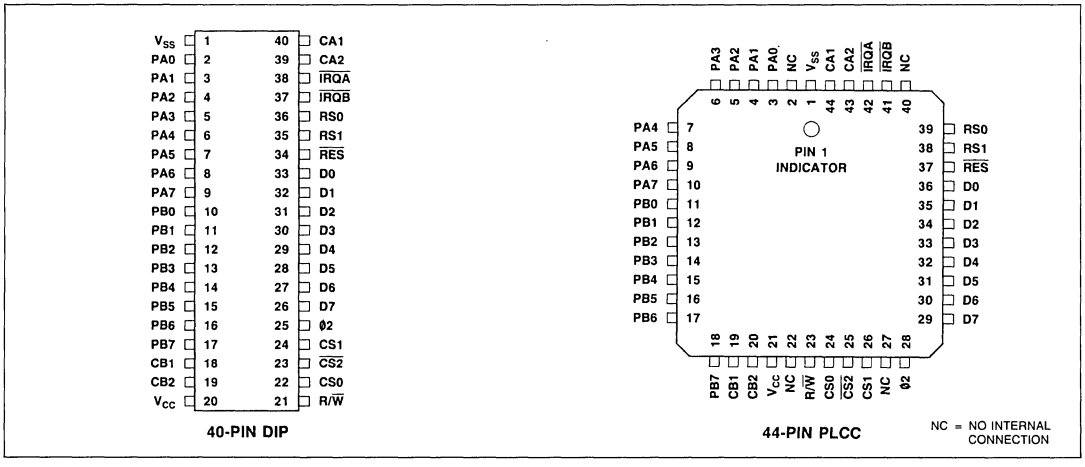


Figure 1. R65C21 Pin Assignments

ORDERING INFORMATION

Part Number:
R65C21

- Temperature Range (T_L to T_H):
  - Blank = 0°C to +70°C
  - E = −40°C to +85°C
- Frequency
  - 1 = 1 MHz
  - 2 = 2 MHz
  - 3 = 3 MHz
  - 4 = 4 MHz
- Package
  - C = 40-Pin Ceramic DIP
  - P = 40-Pin Plastic DIP
  - J = 44-Pin Plastic Leaded Chip Carrier (PLCC)

INTERFACE SIGNALS

The PIA interfaces to the R6500, R6500/* or the R65C00 microprocessor family with a reset line, a ϕ2 clock line, a read/write line, two interrupt request lines, two register select lines, three chip select lines, and an 8-bit bidirectional data bus.

The PIA interfces to the peripheral devices with four interrupt/control lines and two 8-bidirectional data ports.

Figure 1 (on the front page) shows the R65C21 PIA pin assignments and Figure 2 groups the signals by functional interface.

CHIP SELECT (CS0, CS1, $\overline{CS2}$)

The PIA is selected when CS0 and CS1 are high and $\overline{CS2}$ is low. These three chip select lines are normally connected to the processor address lines either directly or through external decoder circuits. When the PIA is selected, data will be transferred between the data lines and PIA registers, and/or peripheral interface lines as determined by the R/$\overline{W}$, RS0, and RS1 lines and the contents of Control Registers A and B.

RESET SIGNAL ($\overline{RES}$)

The Reset ($\overline{RES}$) input initializes the R65C21 PIA. A low signal on the $\overline{RES}$ input causes all internal registers to be cleared.

CLOCK SIGNAL (ϕ2)

The Phase 2 Clock Signal (ϕ2) is the system clock that triggers all data transfers between the CPU and the PIA. ϕ2 is generated by the CPU and is therefore the synchronizing signal between the CPU and the PIA.

READ/WRITE SIGNAL (R/$\overline{W}$)

Read/Write (R/$\overline{W}$) controls the direction of data transfers between the PIA and the data lines associated with the CPU and the peripheral devices. R/$\overline{W}$ high permits the peripheral devices to transfer data to the CPU from the PIA. R/$\overline{W}$ low allows data to be transferred from the CPU to the peripheral devices from the PIA.

REGISTER SELECT (RS0, RS1)

The two Register Select lines (RS0, RS1), in conjunction with the Control Registers' (CRA, CRB) Data Direction Register access bits select the various R65C21 registers to be accessed by the CPU. RS0 and RS1 are normally connected to the microprocessor (CPU) address output lines. Through control of these lines, the CPU can write directly into the Control Registers (CRA, CRB), the Data Direction Registers (DDRA, DDRB) and the Peripheral Output Registers (ORA, ORB). In addition, the processor may directly read the contents of the Control Registers and the Data Direction Registers. Accessing the Peripheral Output Register for the purpose of reading data back into the processor operates differently on the ORA and the ORB registers and, therefore, are shown separately in Table 1.

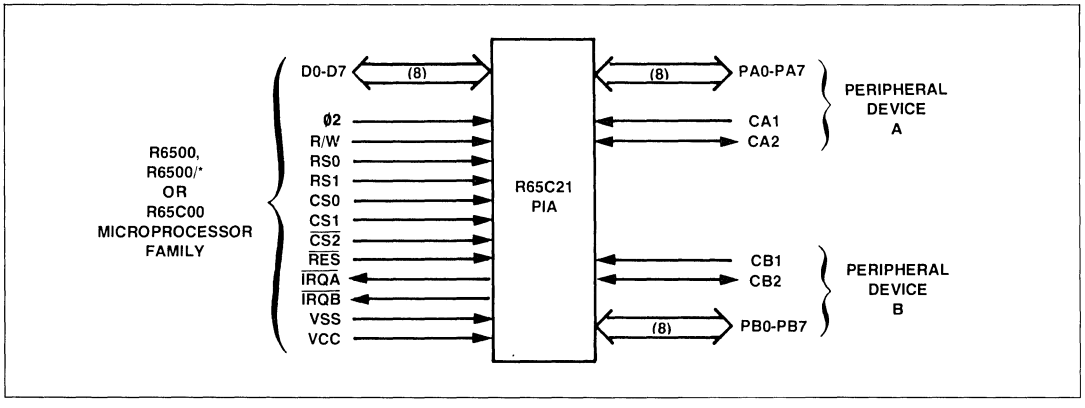


Figure 2. R65C21 ACIA Interface Signals

Table 1. ORA and ORB Register Addressing

Register Address (Hex)	Register Select Lines		Data Direction Control		Register Operation	
	RS1	RS0	CRA (Bit 2)	CRB (Bit 2)	R/$\overline{W}$=H	R/$\overline{W}$=L
0	L	L	1	—	Read PIBA	Write ORA
0	L	L	0	—	Read DDRA	Write DDRA
1	L	H	—	—	Read CRA	Write CRA
2	H	L	—	1	Read PIBB	Write ORB
2	H	L	—	0	Read DDRB	Write DDRB
3	H	H	—	—	Read CRB	Write CRB

INTERRUPT REQUEST LINES ($\overline{IRQA}$, $\overline{IRQB}$)

The active low Interrupt Request lines ($\overline{IRQA}$ and $\overline{IRQB}$) act to interrupt the microprocessor either directly or through external interrupt priority circuitry. These lines are open drain and are capable of sinking 1.6 mA from an external source. This permits all interrupt request lines to be tied together in a wired-OR configuration. The A and B in the titles of these lines correspond to the peripheral port A and the peripheral port B so that each interrupt request line services one peripheral data port.

Each Interrupt Request line has two interrupt flag bits which can cause the Interrupt Request line to go low. These flags are bits 6 and 7 in the two Control Registers (CRA, CRB). These flags act as the link between the peripheral interrupt signals and the microprocessor interrupt inputs. Each flag has a corresponding interrupt disable bit which allows the processor to enable or disable the interrupt from each of the four interrupt inputs (CA1, CA2, CB1, CB2). The four interrupt flags are set by active transitions of the signal on the interrupt input (CA1, CA2, CB1, CB2).

CRA bit 7 (IRQA1) is always set by an active transition of the CA1 interrupt input signal. However, $\overline{IRQA}$ can be disabled by setting bit 0 in CRA to a 0. Likewise, CRA bit 6 (IRQA2) is set by an active transition of the CA2 interrupt input signal and $\overline{IRQA}$ can be disabled by setting bit 3 in CRA to a 0.

Both bit 6 and bit 7 in CRA are reset by a "Read Peripheral Output Register A" operation. This is defined as an operation in which the read/write, proper data direction register and register select signals are provided to allow the processor to read the Peripheral A I/O port. A summary of $\overline{IRQA}$ control is shown in Table 2.

Control of $\overline{IRQB}$ is performed in exactly the same manner as that described above for $\overline{IRQA}$ (Table 2). Bit 7 in CRB (IRQB1) is set by an active transition on CB1 and $\overline{IRQB}$ from this flag is controlled by CRB bit 0. Likewise, bit 6 ($\overline{IRQB2}$) in CRB is set by an active transition on CB2, and $\overline{IRQB}$ from this flag is controlled by CRB bit 3. Also, both bit 6 and bit 7 of CRB are reset by a "Read Peripheral B Output Register" operation.

Table 2. $\overline{IRQA}$ and $\overline{IRQB}$ Control Summary

Control Register Bits	Action
CRA-7 = 1 and CRA-0 = 1	$\overline{IRQA}$ goes low (Active)
CRA-6 = 1 and CRA-3 = 1	$\overline{IRQA}$ goes low (Active)
CRB-7 = 1 and CRB-0 = 1	$\overline{IRQB}$ goes low (Active)
CRB-6 = 1 and CRB-3 = 1	$\overline{IRQB}$ goes low (Active)

INTERRUPT INPUT/PERIPHERAL CONTROL LINES (CA1, CA2, CB1, CB2)

The four interrupt input/peripheral control lines provide a number of special peripheral control functions. These lines greatly enhance the power of the two general purpose interface ports (PA0–PA7), PB0–PB7). Figure 4 summarizes the operation of these control lines.

CA1 is an interrupt input only. An active transition of the signal on this input will set bit 7 of the Control Register A to a logic 1. The active transition can be programmed by setting a 0 in bit 1 of the CRA if the interrupt flag (bit 7 of CRA) is to be set on a negative transition of the CA1 signal or a 1 if it is to be set on a positive transition.

CA2 can act as a totally independent interrupt or as a peripheral control output. As an input (CRA, bit 5 = 0) it acts to set the interrupt flag, bit 6 of CRA, to a logic 1 on the active transition selected by bit 4 of CRA.

These control register bits and interrupt inputs serve the same basic function as that described above for CA1. The input signal sets the interrupt flag which serves as the link between the peripheral device and the processor interrupt structure. The interrupt disable bit allows the processor to exercise control over the system interrupt.

In the output mode (CRA, bit 5 = 1), CA2 can operate independently to generate a simple pulse each time the microprocessor reads the data on the Peripheral A I/O port. This mode is selected by setting CRA, bit 4 to a 0 and CRA, bit 3 to a 1. This pulse output can be used to control the counters, shift registers, etc., which make sequential data available on the Peripheral input lines.

A second output mode allows CA2 to be used in conjunction with CA1 to "handshake" between the processor and the peripheral device. On the A side, this technique allows positive control of data transfers from the peripheral device into the microprocessor. The CA1 input signals the processor that data is available by interrupting the processor. The processor reads the data and sets CA2 low. This signals the peripheral device that it can make new data available.

The final output mode can be selected by setting bit 4 of CRA to a 1. In this mode, CA2 is a simple peripheral control output which can be set high or low by setting bit 3 of CRA to a 1 or 0, respectively.

CB1 operates as an interrupt input only in the same manner as CA1. Bit 7 of CRB is set by the active transition selected by bit 0 of CRB. Likewise, the CB2 input mode operates exactly the same as the CA2 input modes. The CB2 output modes, CRB bit 5 = 1, differ somewhat from those of CA2. The pulse output occurs when the processor writes data into the Peripheral B Output Register. Also, the "handshaking" operates on data transfers from the processor into the peripheral device.

FUNCTIONAL DESCRIPTION

The R65C21 PIA is organized into two independent sections referred to as the A Side and the B Side. Each section consists of a Control Register (CRA, CRB), Data Direction Register (DDRA, DDRB), Output Register (ORA, ORB), Interrupt Status Control (ISCA, ISCB), and the buffers necessary to drive the Peripheral Interface buses. Data Bus Buffers (DBB) interface data from the two sections to the data bus, while the Data Input Register (DIR) interfaces data from the DBB to the PIA registers. Chip Select and R/$\overline{W}$ control circuitry interface to the processor bus control lines. Figure 3 is a block diagram of the R65C21 PIA.

DATA INPUT REGISTER (DIR)

When the microprocessor writes data into the PIA, the data which appears on the data bus during the $\phi 2$ clock pulse is latched into the Data Input Register (DIR). The data is then transferred into one of six internal registers of the PIA after the trailing edge of the $\phi 2$ clock. This assures that the data on the peripheral output lines will make smooth transitions from high to low (or from low to high) and the voltage will remain stable except when it is going to the opposite polarity.

CONTROL REGISTERS (CRA AND CRB)

Table 3 illustrates the bit designation and functions in the two control registers. The control registers allow the microprocessor to control the operation of the Interrupt Control inputs (CA1, CA2, CB1, CB2), and Peripheral Control outputs (CA2, CB2). Bit 2 in each register controls the addressing of the Data Direction Registers (DDRA, DDRB) and the Output Registers (ORA, ORB). In addition, two bits (bit 6 and 7) in each control register indicate the status of the Interrupt Input lines (CA1, CA2, CB1, CB2). These Interrupt Status bits (IRQA1, IRQA2 or IRQB1, IRQB2) are normally interrogated by the microprocessor during the $\overline{IRQ}$ interrupt service routine to determine the source of the interrupt.

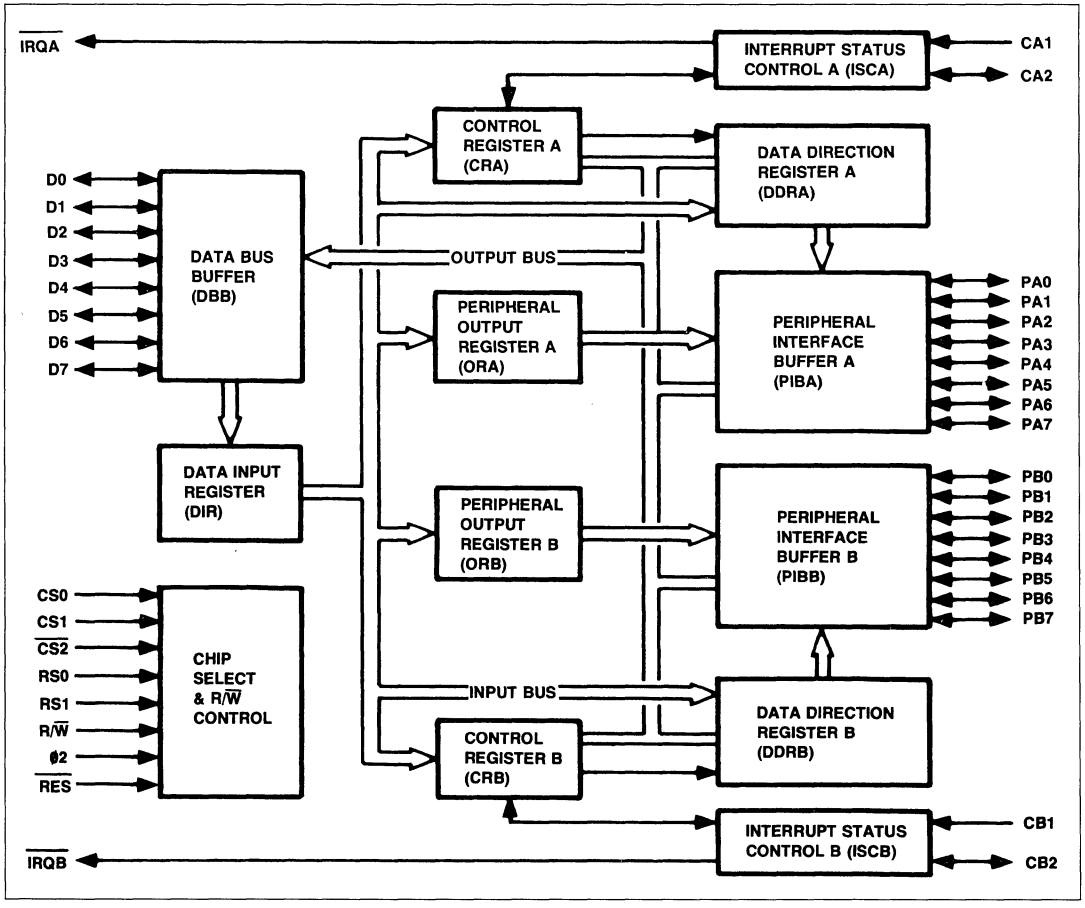


Figure 3. R65C21 PIA Block Diagram

Table 3. Control Registers Bit Designations

	7	6	5	4	3	2	1	0
CRA	IRQA1	IRQA2	CA2 Control			DDRA/ORA Select	CA1 Control	
	7	6	5	4	3	2	1	0
CRB	IRQB1	IRQB2	CB2 Control			DDRB/ORB Select	CB1 Control	

DATA DIRECTION REGISTERS (DDRA, DDRB)

The Data Direction Registers (DDRA, DDRB) allow the processor to program each line in the 8-bit Peripheral I/O port to be either an input or an output. Each bit in DDRA controls the corresponding line in the Peripheral A port and each bit in DDRB controls the corresponding line in the Peripheral B port. Writing a 0 in a bit position in the Data Direction Register causes the corresponding Peripheral I/O line to act as an input; a 1 causes it to act as an output.

Bit 2 in each Control Register (CRA and CRB) controls access to the Data Direction Register or the Peripheral interface. If bit 2 is a 1, a Peripheral Output register (ORA, ORB) is selected, and if bit 2 is a 0, a Data Direction Register (DDRA, DDRB) is selected. The Data Direction Register Access Control bit, together with the Register Select lines (RS0, RS1) selects the various internal registers as shown in Table 1.

PERIPHERAL OUTPUT REGISTER (ORA, ORB)

The Peripheral Output Registers (ORA, ORB) store the output data from the Data Bus Buffers (DBB) which appears on the Peripheral I/O port. If a line on the Peripheral A Port is programmed as an output by the DDRA, writing a 0 into the corresponding bit in the ORA causes that line to go low ($\leq$0.4 Vdc); writing a 1 causes the line to go high. The lines of the Peripheral B port are controlled by ORB in the same manner.

INTERRUPT STATUS CONTROL (ISCA, ISCB)

The four interrupt/peripheral control lines (CA1, CA2, CB1, CB2) are controlled by the Interrupt Status Control logic (A, B). This logic interprets the contents of the corresponding Control Register and detects active transitions on the interrupt inputs.

PERIPHERAL I/O PORTS (PA0–PA7, PB0–PB7)

The Peripheral A and Peripheral B I/O ports allow the microprocessor to interface to the input lines on the peripheral device by writing data into the Peripheral Output Register. They also allow the processor to interface with the peripheral device output lines by reading the data on the Peripheral Port input lines directly onto the data bus and into the internal registers of the processor.

Each of the Peripheral I/O lines can be programmed to act as an input or an output. This is accomplished by setting a 1 in the corresponding bit in the Data Direction Register for those lines which are to act as outputs. A 0 in a bit of the Data Direction Register causes the corresponding Peripheral I/O lines to act as an input.

The buffers which drive the Peripheral A I/O lines contain "passive" pull-up devices. These pull-up devices are resistive in nature and therefore allow the output voltage to go to V_{CC} for a logic 1. The switches can sink a full 3.2 mA, making these buffers capable of driving two standard TTL loads.

In the input mode, the pull-up devices are still connected to the I/O pin and still supply current to this pin. For this reason, these lines also represent two standard TTL loads in the input mode.

The Peripheral B I/O port duplicates many of the functions of the Peripheral A port. The process of programming these lines to act as an input or an output is similar to the Peripheral A port, as is the effect of reading or writing this port. However, there are several characteristics of the buffers driving these lines which affect their use in peripheral interfacing.

The Peripheral B I/O port buffers are push-pull devices, i.e., the pull-up devices are switched OFF in the 0 state and ON for a logic 1. Since these pull-ups are active devices, the logic 1 voltage will not go higher than +2.4 Vdc.

Another difference between the PA0–PA7 lines and the PB0 through PB7 lines is that they have three-state capability which allows them to enter a high impedance state when programmed to be used as input lines. In addition, data on these lines will be read properly, when programmed as output lines, even if the data signals fall below 2.0 Vdc for a "high" state or are above 0.8 Vdc for a "low" state. When programmed as output, each line can drive at least a two TTL load and may also be used as a source of up to 3.2 mA at 1.5 Vdc to directly drive the base of a transistor switch, such as a Darlington pair.

Because these outputs are designed to drive transistors directly, the output data is read directly from the Peripheral Output Register for those lines programmed to act as inputs.

The final characteristic is the high-impedance input state which is a function of the Peripheral B push-pull buffers. When the Peripheral B I/O lines are programmed to act as inputs, the output buffer enters the high impedance state.

DATA BUS BUFFERS (DBB)

The Data Bus Buffers are 8-bit bidirectional buffers used for data exchange, on the D0–D7 Data Bus, between the microprocessor and the PIA. These buffers are tri-state and are capable of driving a two TTL load (when operating in an output mode) and represent a one TTL load to the microprocessor (when operating in an input mode).

CONTROL REGISTER A (CRA)

CA2 INPUT MODE (BIT 5 = 0)

7	6	5	4	3	2	1	0
IRQA1 FLAG	IRQA2 FLAG	CA2 INPUT MODE SELECT (=0)	IRQA2 TRANSITION SELECT	$\overline{\text{IRQA}}$ ENABLE FOR IRQA2	DDRA/ORA SELECT	IRQA1 TRANSITION SELECT	$\overline{\text{IRQA}}$ ENABLE FOR IRQA1
			IRQA/IRQA2 CONTROL			$\overline{\text{IRQA}}$/IRQA1 CONTROL	

CA2 OUTPUT MODE (BIT 5 = 1)

7	6	5	4	3	2	1	0
IRQA1 FLAG	0	CA2 OUTPUT MODE SELECT (=1)	CA2 OUTPUT CONTROL	CA2 RESTORE CONTROL	DDRA/ORA SELECT	IRQA1 TRANSITION SELECT	$\overline{\text{IRQA}}$ ENABLE FOR IRQA1
			CA2 CONTROL			$\overline{\text{IRQA}}$/IRQA1 CONTROL	

CA2 INPUT OR OUTPUT MODE (BIT 5 = 0 OR 1)

Bit 7 — **IRQA1 FLAG**
- 1: A transition has occurred on CA1 that satisfies the bit 1 IRQA1 transition polarity criteria. This bit is cleared by a read of Output Register A or by $\overline{\text{RES}}$.
- 0: No transition has occurred on CA1 that satisfies the bit 1 IRQA1 transition polarity criteria.

Bit 2 — **DATA DIRECTION REGISTER A/OUTPUT REGISTER A SELECT**
- 1: Select Output Register A.
- 0: Select Data Direction Register A.

Bit 1 — **IRQA1 TRANSITION SELECT**
- 1: Set IRQA1 Flag (bit 7) on a positive (low-to-high) transition of CA1.
- 0: Set IRQA1 Flag (bit 7) on a negative (high-to-low) transition of CA1.

Bit 0 — **$\overline{\text{IRQA}}$ ENABLE FOR IRQA1**
- 1: Enable assertion of $\overline{\text{IRQA}}$ when IRQA1 Flag (bit 7) is set.
- 0: Disable assertion of $\overline{\text{IRQA}}$ when IRQA1 Flag (bit 7) is set.

CA2 INPUT MODE (BIT 5 = 0)

Bit 6 — **IRQA2 FLAG**
- 1: A transition has occurred on CA2 that satisfies the bit 4 IRQA2 transition polarity criteria. This flag is cleared by a read of Output Register A or by $\overline{\text{RES}}$.
- 0: No transition has occurred on CA2 that satisfies the bit 4 IRQA2 transition polarity criteria.

Bit 5 — **CA2 MODE SELECT**
- 0: Select CA2 Input Mode.

Bit 4 — **IRQA2 TRANSITION SELECT**
- 1: Set IRQA2 Flag (bit 6) on a positive (low-to-high) transition of CA2.
- 0: Set IRQA2 Flag (bit 6) on a negative (high-to-low) transition of CA2.

Bit 3 — **$\overline{\text{IRQA}}$ ENABLE FOR IRQA2**
- 1: Enable assertion of $\overline{\text{IRQA}}$ when IRQA2 Flag (bit 6) is set.
- 0: Disable assertion of $\overline{\text{IRQA}}$ when IRQA2 Flag (bit 6) is set.

CA2 OUTPUT MODE (BIT 5 = 0)

Bit 6 — **NOT USED**
- 0: Always zero.

Bit 5 — **CA2 MODE SELECT**
- 1: Select CA2 Output Mode.

Bit 4 — **CA2 OUTPUT CONTROL**
- 1: CA2 goes low when a zero is written into CRA bit 3. CA2 goes high when a one is written into CRA bit 3.
- 0: CA2 goes low on the first negative (high-to-low) Ø2 clock transition following a read of Output Register A. CA2 returns high as specified by bit 3

Bit 3 — **CA2 READ STROBE RESTORE CONTROL (4 = 0)**
- 1: CA2 returns high on the next Ø2 clock negative transition following a read of Output Register A.
- 0: CA2 returns high on the next active CA1 transition following a read of Output Register A as specified by bit 1.

Figure 4. Control Line Operations Summary (1 of 2)

CONTROL REGISTER B (CRB)

CB2 INPUT MODE (BIT 5 = 0)

7	6	5	4	3	2	1	0
IRQB1 FLAG	IRQB2 FLAG	CB2 INPUT MODE SELECT (=0)	IRQB2 TRANSITION SELECT	$\overline{\text{IRQB}}$ ENABLE FOR IRQB2	DDRB/ORB SELECT	IRQB1 TRANSITION SELECT	$\overline{\text{IRQB}}$ ENABLE FOR IRQB1
			IRQB/IRQB2 CONTROL			$\overline{\text{IRQB}}$/IRQB1 CONTROL	

CB2 OUTPUT MODE (BIT 5 = 1)

7	6	5	4	3	2	1	0
IRQB1 FLAG	0	CB2 OUTPUT MODE SELECT (=1)	CB2 OUTPUT CONTROL	CB2 RESTORE CONTROL	DDRB/ORB SELECT	IRQB1 TRANSITION SELECT	$\overline{\text{IRQB}}$ ENABLE FOR IRQB1
			CB2 CONTROL			$\overline{\text{IRQB}}$/IRQB1 CONTROL	

CB2 INPUT OR OUTPUT MODE (BIT 5 = 0 OR 1)

Bit 7 — IRQB1 FLAG
- 1: A transition has occurred on CB1 that satisfies the bit 1 IRQB1 transition polarity criteria. This bit is cleared by a read of Output Register B or by $\overline{\text{RES}}$.
- 0: No transition has occurred on CB1 that satisfies the bit 1 IRQB1 transition polarity criteria.

Bit 2 — DATA DIRECTION REGISTER B/OUTPUT REGISTER B SELECT
- 1: Select Output Register B.
- 0: Select Data Direction Register B.

Bit 1 — IRQB1 TRANSITION SELECT
- 1: Set IRQB1 Flag (bit 7) on a positive (low-to-high) transition of CB1.
- 0: Set IRQB1 Flag (bit 7) on a negative (high-to-low) transition of CB1.

Bit 0 — $\overline{\text{IRQB}}$ ENABLE FOR IRQB1
- 1: Enable assertion of $\overline{\text{IRQB}}$ when IRQB1 Flag (bit 7) is set.
- 0: Disable assertion of $\overline{\text{IRQB}}$ when IRQB1 Flag (bit 7) is set.

CB2 INPUT MODE (BIT 5 = 0)

Bit 6 — IRQB2 FLAG
- 1: A transition has occurred on CB2 that satisfies the bit 4 IRQB2 transition polarity criteria. This flag is cleared by a read of Output Register B or by $\overline{\text{RES}}$.
- 0: No transition has occurred on CB2 that satisfies the bit 4 IRQB2 transition polarity criteria.

Bit 5 — CB2 MODE SELECT
- 0: Select CB2 Input Mode.

Bit 4 — IRQB2 TRANSITION SELECT
- 1: Set IRQB2 Flag (bit 6) on a positive (low-to-high) transition of CB2.
- 0: Set IRQB2 Flag (bit 6) on a negative (high-to-low) transition of CB2.

Bit 3 — $\overline{\text{IRQB}}$ ENABLE FOR IRQB2
- 1: Enable assertion of $\overline{\text{IRQB}}$ when IRQB2 Flag (bit 6) is set.
- 0: Disable assertion of $\overline{\text{IRQB}}$ when IRQA2 Flag (bit 6) is set.

CB2 OUTPUT MODE (BIT 5 = 0)

Bit 6 — NOT USED
- 0: Always zero.

Bit 5 — CB2 MODE SELECT
- 1: Select CB2 Output Mode.

Bit 4 — CB2 OUTPUT CONTROL
- 1: CB2 goes low when a zero is written into CRB bit 3. CB2 goes high when a one is written into CRB bit 3.
- 0: CB2 goes low on the first negative (high-to-low) $\phi 2$ clock transition following a read of Output Register B. CB2 returns high as specified by bit 3

Bit 3 — CB2 READ STROBE RESTORE CONTROL (4 = 0)
- 1: CB2 returns high on the next $\phi 2$ clock negative transition following a read of Output Register B.
- 0: CB2 returns high on the next active CB1 transition following a read of Output Register B as specified by bit 1.

Figure 4. Control Line Operations Summary (2 of 2)

READING THE PERIPHERAL A I/O PORT

Performing a Read operation with RS1 = 0, RS0 = 0 and the Data Direction Register Access Control bit (CRA-2) = 1, directly transfers the data on the Peripheral A I/O lines to the data bus. In this situation, the data bus will contain both the input and output data. The processor must be programmed to recognize and interpret only those bits which are important to the particular peripheral operation being performed.

Since the processor always reads the Peripheral A I/O port pins instead of the actual Peripheral Output Register (ORA), it is possible for the data read by the processor to differ from the contents of the Peripheral Output Register for an output line. This is true when the I/O pin is not allowed to go to a full +2.4 Vdc when the Peripheral Output register contains a logic 1. In this case, the processor will read a 0 from the Peripheral A pin, even though the corresponding bit in the Peripheral Output register is a 1.

READING THE PERIPHERAL B I/O PORT

Reading the Peripheral B I/O port yields a combination of input and output data in a manner similar to the Peripheral A port. However, data is read directly from the Peripheral B Output Register (ORB) for those lines programmed to act as outputs. It is therefore possible to load down the Peripheral B Output lines without causing incorrect data to be transferred back to the processor on a Read operation.

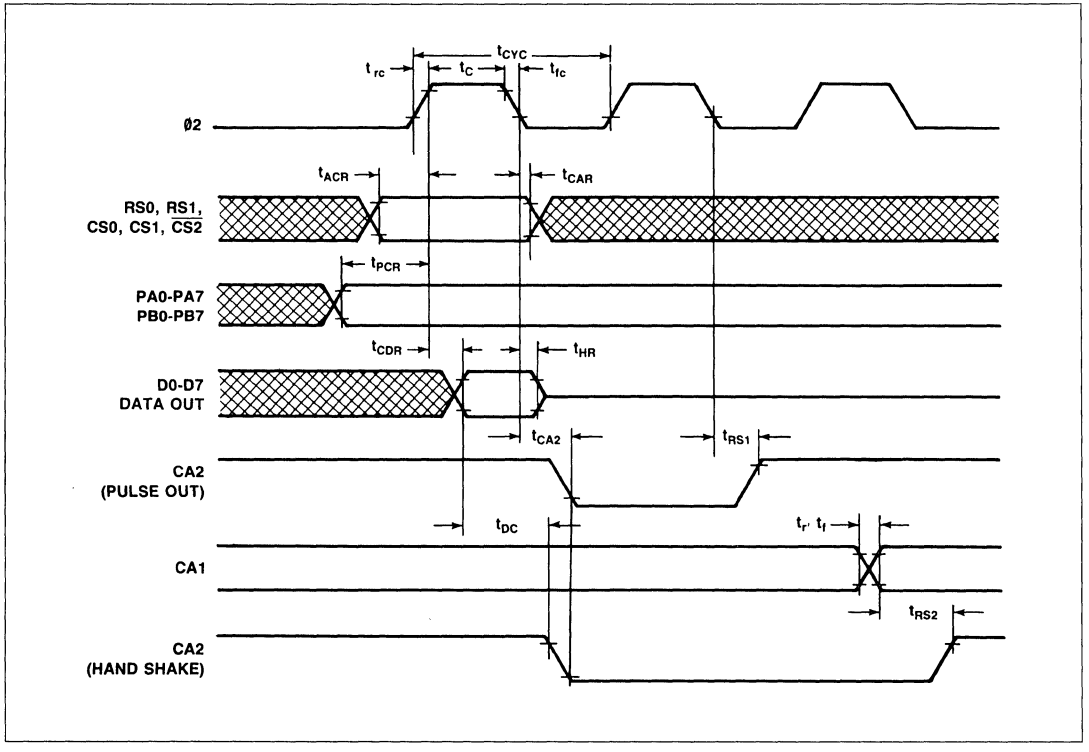


Figure 5. Read Timing Waveforms

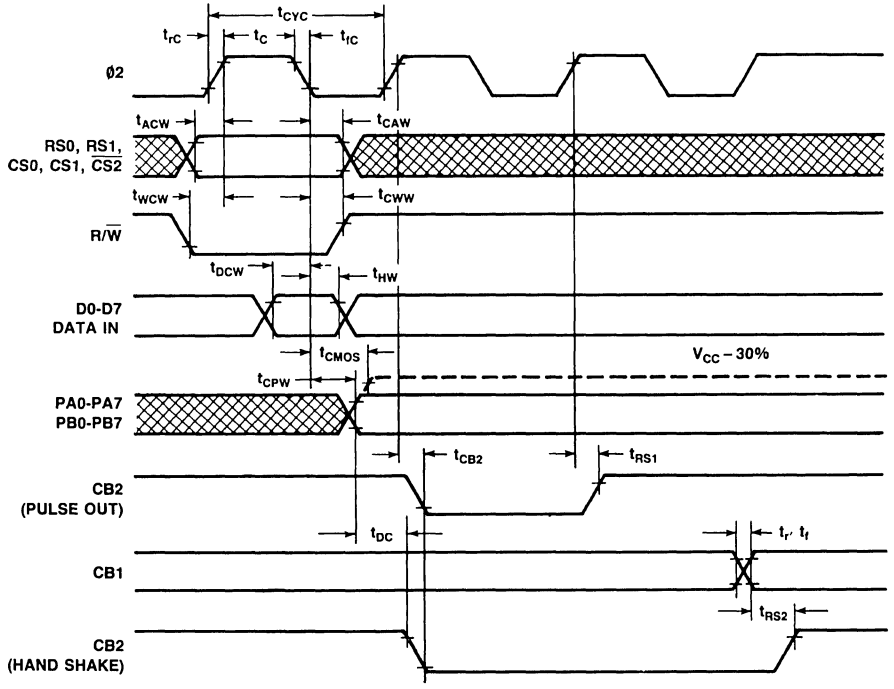


Figure 6. Write Timing Waveform

SWITCHING WAVEFORMS

(V_{CC} = 5.0 Vdc ±5%, V_{SS} = 0, T_A = T_L to T_H, unless otherwise noted)

BUS TIMING

Parameter	Symbol	1 MHz		2 MHz		3 MHz		4 MHz		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Ø2 Cycle	t_{CYC}	1.0	—	0.5	—	0.33	—	0.25	—	μs
Ø2 Pulse Width	t_C	450	—	220	—	160	—	110	—	ns
Ø2 Rise and Fall Time	t_{rc}, t_{fc}	—	25	—	15	—	12	—	10	ns
Read										
Address Set-Up Time	t_{ACR}	140	—	70	—	53	—	35	—	ns
Address Hold Time	t_{CAR}	0	—	0	—	0	—	0	—	ns
Peripheral Data Set-Up Time	t_{PCR}	300	—	150	—	110	—	75	—	ns
Data Bus Delay Time	t_{CDR}	—	335	—	145	—	105	—	85	ns
Data Bus Hold Time	t_{HR}	20	—	20	—	20	—	20	—	ns
Write										
Address Set-Up Time	t_{ACW}	140	—	70	—	53	—	35	—	ns
Address Hold Time	t_{CAW}	0	—	0	—	0	—	0	—	ns
R/$\overline{W}$ Set-Up Time	t_{WCW}	180	—	90	—	67	—	45	—	ns
R/$\overline{W}$ Hold Time	t_{CWW}	0	—	0	—	0	—	0	—	ns
Data Bus Set-Up Time	t_{DCW}	180	—	90	—	67	—	45	—	ns
Data Bus Hold Time	t_{HW}	10	—	10	—	10	—	10	—	ns
Peripheral Data Delay Time	t_{CPW}	—	1.0	—	0.5	—	0.5	—	0.5	μs
Peripheral Data Delay Time to CMOS Level	t_{CMOS}	—	2.0	—	1.0	—	0.7	—	0.5	μs

PERIPHERAL INTERFACE TIMING

Peripheral Data Set-Up	t_{PCR}	300	—	150	—	110	—	75	—	ns
Ø2 Low to CA2 Low Delay	t_{CA2}	—	1.0	—	0.5	—	0.5	—	0.5	μs
Ø2 Low to CA2 High Delay	t_{RS1}	—	1.0	—	0.5	—	0.5	—	0.5	μs
CA1 Active to CA2 High Delay	t_{RS2}	—	2.0	—	1.0	—	1.0	—	1.0	μs
Ø2 High to CB2 Low Delay	t_{CB2}	—	1.0	—	0.5	—	0.5	—	0.5	μs
Peripheral Data Valid to CB2 Low Delay	t_{DC}	0	1.5	0	0.75	0	0.5	0	0.37	μs
Ø2 High to CB2 High Delay	t_{RS1}	—	1.0	—	0.5	—	0.5	—	0.5	μs
CB1 Active to CB2 High Delay	t_{RS2}	—	2.0	—	1.0	—	0.67	—	0.5	μs
CA1, CA2, CB1 and CB2 Input Rise and Fall Time	t_r, t_f	—	1.0	—	1.0	—	1.0	—	1.0	μs

NOTE: Timing measurements are referenced to and from a low voltage of 0.8 Vdc and a high voltage of 2.0 Vdc.

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to +7.0	Vdc
Input Voltage	V_{IN}	−0.3 to V_{CC} +0.3	Vdc
Output Voltage	V_{OUT}	−0.3 to V_{CC} +0.3	Vdc
Operating Temperature Range Commercial Industrial	T_A	 0 to +70 −40 to +85	°C
Storage Temperature	T_{STG}	−55 to +150	°C

*NOTE: Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in other sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING CONDITIONS

Parameter	Symbol	Value
Supply Voltage	V_{CC}	5V ±5%
Temperature Range Commercial Industrial	T_A	T_L to T_H 0°C to 70°C −40°C to +85°C

ELECTRICAL CHARACTERISTICS

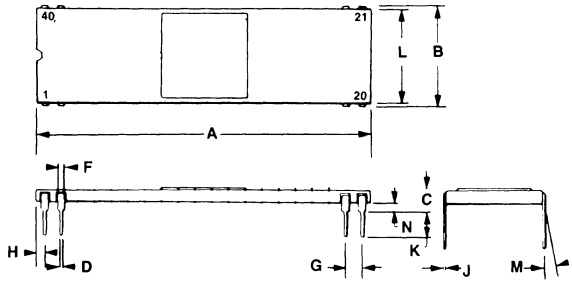
(V_{CC} = 5.0 Vdc ±5%, V_{SS} = 0, T_A = T_L to T_H, unless otherwise noted)

Parameter	Symbol	Min.	Typ.[3]	Max.	Unit[2]	Test Conditions
Input High Voltage	V_{IH}	+2.0	—	V_{CC}	V	
Input Low Voltage	V_{IL}	−0.3	—	+0.8	V	
Input Leakage Current R/W, RES, RS0, RS1, CS0, CS2, CA1, CB1, Ø2 CS1	I_{IN}	 — —	 ±1	 ±2.5 ±10.0	µA	V_{IN} = 0V to V_{CC} V_{CC} = 5.25V
Input Leakage Current for Three-State Off D0–D7, PB0–PB7, CB2	I_{TSI}	—	±2	±10	µA	V_{IN} = 0.4V to 2.4V V_{CC} = 5.25V
Input High Current PA0–PA7, CA2	I_{IH}	−200	−300	—	µA	V_{IH} = 2.0V
Input Low Current PA0–PA7, CA2	I_{IL}	—	−2	−3.2	mA	V_{IL} = 0.8V
Output High Voltage Logic PB0–PB7, CB2 (Darlington Drive)	V_{OH}	 2.4 1.5	 — —	 — —	V	V_{CC} = 4.75V I_{LOAD} = −200µA I_{LOAD} = −3.2mA
Output Low Voltage PA0–PA7, CA2, PB0–PB7, CB2 D0–D7, IRQA, IRQB	V_{OL}	—	—	+0.4	V	V_{CC} = 4.75V I_{LOAD} = 3.2 mA I_{LOAD} = 1.6 mA
Output High Current (Sourcing) Logic PB0–PB7, CB2 (Darlington Drive)	I_{OH}	 −200 −3.2	 −1500 −6	 — —	 µA mA	 V_{OH} = 2.4V V_{OH} = 1.5V
Output Low Current (Sinking) PA0–PA7, PB0–PB7, CB2, CA2 D0–D7, IRQA, IRQB	I_{OL}	 3.2 1.6	 — —	 — —	 mA mA	V_{OL} = 0.4V
Output Leakage Current (Off State) IRQA, IRQB	I_{OFF}	—	1	±10	µA	V_{OH} = 2.4V V_{CC} = 5.25V
Power Dissipation	P_D	—	7	10	mW/MHz	
Input Capacitance D0–D7, PA0–PA7, PB0–PB7, CA2, CB2 R/W, RES, RS0, RS1, CS0, CS1, CS2 CA1, CB1, Ø2	C_{IN}	 — — —	 — — —	 10 7 20	 pF pF pF	V_{CC} = 5.0V V_{IN} = 0V f = 2 MHz T_A = 25°C
Output Capacitance	C_{OUT}	—	—	10	pF	

Notes:
1. All units are direct current (dc) except capacitance.
2. Negative sign indicates outward current flow, positive indicates inward flow.
3. Typical values are shown for V_{CC} = 5.0V and T_A = 25°C.

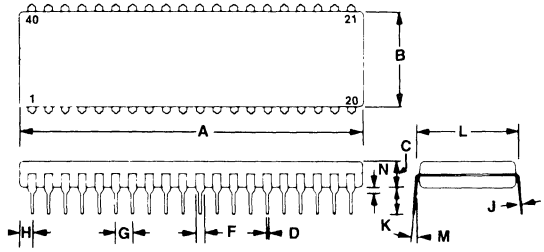
PACKAGE DIMENSIONS

40-PIN CERAMIC DIP



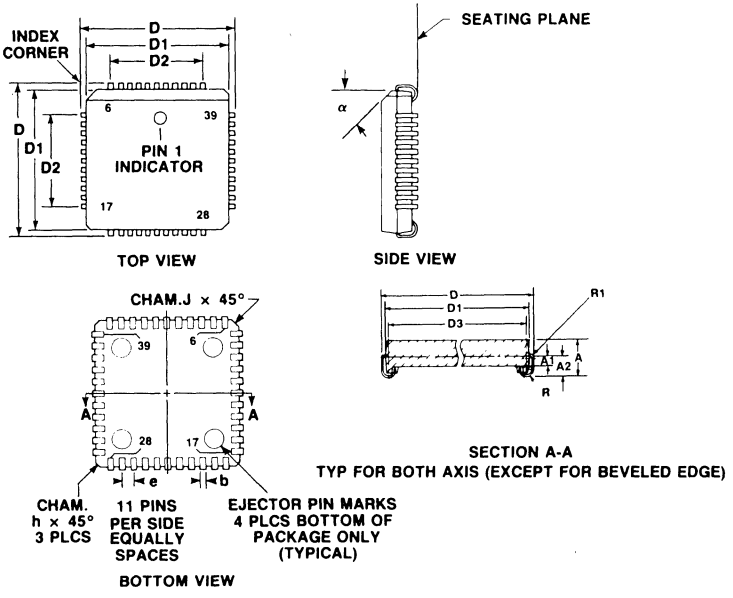
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	50.29	51.31	1.980	2.020
B	15.11	15.88	0.595	0.625
C	2.54	4.19	0.100	0.165
D	0.38	0.53	0.015	0.021
F	0.76	1.27	0.030	0.050
G	2.54 BSC		0.100 BSC	
H	0.76	1.78	0.030	0.070
J	0.20	0.33	0.008	0.013
K	2.54	4.19	0.100	0.165
L	14.60	15.37	0.575	0.605
M	0°	10°	0°	10°
N	0.51	1.52	0.020	0.060

40-PIN PLASTIC DIP



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	51.82	52.32	2.040	2.060
B	13.46	13.97	0.530	0.550
C	3.56	5.08	0.140	0.200
D	0.38	0.53	0.015	0.021
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.30	0.008	0.012
K	3.30	4.32	0.130	0.170
L	15.24 BSC		0.600 BSC	
M	7°	10°	7°	10°
N	0.51	1.02	0.020	0.040

44-PIN PLASTIC LEADED CHIP CARRIER (PLCC)



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.14	4.39	0.163	0.173
A1	1.37	1.47	0.054	0.058
A2	2.31	2.46	0.091	0.097
b	0.457 TYP		0.018 TYP	
D	17.45	17.60	0.687	0.693
D1	16.46	16.56	0.648	0.652
D2	12.62	12.78	0.497	0.503
D3	15.75 REF		0.620 REF	
e	1.27 BSC		0.050 BSC	
h	1.15 TYP		0.045 TYP	
J	0.25 TYP		0.010 TYP	
α	45° TYP		45° TYP	
R	0.89 TYP		0.035 TYP	
R1	0.25 TYP		0.010 TYP	

Rockwell

R65C22
Versatile Interface Adapter (VIA)

1

DESCRIPTION

The R65C22 Versatile Interface Adapter (VIA) is a very flexible I/O control device. In addition, this device contains a pair of very powerful 16-bit interval timers, a serial-to-parallel/parallel-to serial shift register and input data latching on the peripheral ports. Expanded handshaking capability allows control of bidirectional data transfers between VIA's in multiple processor systems.

The R65C22 includes functions for programmed control of up to two peripheral devices (Ports A and B). These two program controlled 8-bit bidirectional peripheral I/O ports allow direct interfacing between the microprocessor and selected peripheral units. Each port has input data latching capability. Two programmable Data Direction Registers (A and B) allow selection of data direction (input or output) on an individual line basis.

The R65C22 also has two programmable 16-bit Interval Timer/Counters with latches. Timer 1 may be operated in a One-Shot Interrupt Mode with interrupts on each count-to-zero, or in a Free-Run Mode with a continuous series of evenly spaced interrupts. Timer 2 functions as both an interval and pulse counter. Serial data transfers are provided by a serial-to-parallel/parallel-to-serial shift register. Application versatility is further increased by various control registers, including—the Interrupt Flag Register, the Interrupt Enable Register, the Auxiliary Control Register and the Peripheral Control Register.

FEATURES

- Low power CMOS N-well silicon gate technology
- Fully compatible with NMOS 6522 devices
- Two 8-bit bidirectional I/O ports
- Two 16-bit programmable timer/counters
- Serial bidirectional peripheral I/O
- TTL compatible peripheral control lines
- Expanded "handshake" capability allows positive control of data transfers between processor and peripheral devices.
- Latched output and input registers on both I/O ports
- 1, 2, 3, and 4 MHz operation
- Commercial and industrial temperature range versions
- Single +5 Vdc power requirement
- Wide variety of packages
  - — 40-pin plastic and ceramic DIP
  - — 44-pin plastic leaded chip carrier (PLCC)

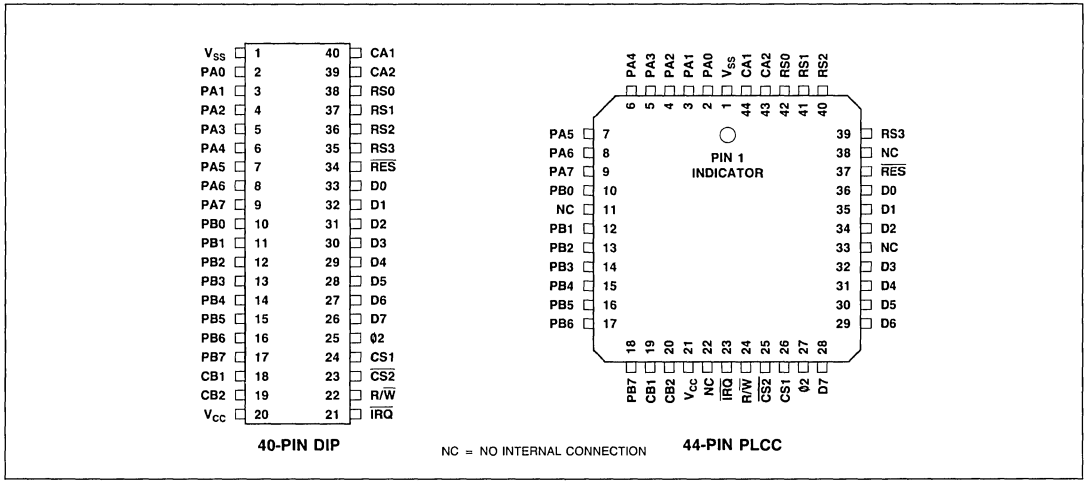


Figure 1. R65C22 Pin Assignments

ORDERING INFORMATION

Part Number:
R65C22

Temperature Range (T_L to T_H):
Blank = 0°C to +70°C
E = -40°C to +85°C

Frequency
1 = 1 MHz
2 = 2 MHz
3 = 3 MHz
4 = 4 MHz

Package
C = 40-Pin Ceramic DIP
P = 40-Pin Plastic DIP
J = 44-Pin Plastic Leaded Chip Carrier (PLCC)

INTERFACE SIGNALS

Figure 1 (on the front page) shows the R65C22 VIA pin assignments and Figure 2 groups the signals by functional interface.

RESET ($\overline{RES}$)

Reset ($\overline{RES}$) clears all internal registers (except T1 and T2 counters and latches, and the Shift Register (SR)). In the $\overline{RES}$ condition, all peripheral interface lines (PA and PB) are placed in the input state. Also, the Timers (T1 and T2), SR and interrupt logic are disabled from operation.

INPUT CLOCK (PHASE 2)

The system Phase 2 ($\phi 2$) Input Clock controls all data transfers between the R65C22 and the microprocessor.

READ/WRITE (R/$\overline{W}$)

The direction of the data transfers between the R65C22 and the system processor is controlled by the R/$\overline{W}$ line in conjunction with the CS1 and $\overline{CS2}$ inputs. When R/$\overline{W}$ is low (write operation) and the R65C22 is selected, data is transferred from the processor bus into the selected R65C22 register. When R/$\overline{W}$ is high (read operation) and the R65C22 is selected, data is transferred from the selected R65C22 register to the processor bus.

DATA BUS (D0-D7)

The eight bidirectional Data Bus lines transfer data between the R65C22 and the microprocessor. During a read operation, the contents of the selected R65C22 internal register are transferred to the microprocessor via the Data Bus lines. During a write operation, the Data Bus lines serve as high impedance inputs over which data is transferred from the microprocessor to a selected R65C22 register. The Data Bus lines are in the high impedance state when the R65C22 is unselected.

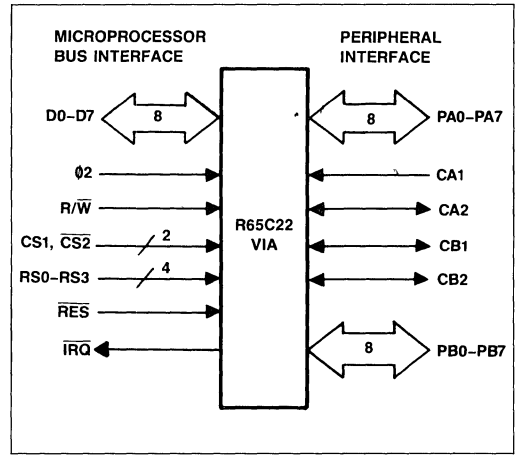


Figure 2. R65C22 VIA Interface Signals

CHIP SELECTS (CS1, $\overline{CS2}$)

Normally, the two chip select lines are connected to the microprocessor address lines. This connection may be direct or through decoding. To access a selected R65C22 register, CS1 must be high (logic 1) and $\overline{CS2}$ must be low (logic 0).

REGISTER SELECTS (RS0-RS3)

The Register Select inputs allow the microprocessor to select one of 16 internal registers within the R65C22. Refer to Table 1 for Register Select coding and a functional description.

INTERRUPT REQUEST ($\overline{IRQ}$)

The Interrupt Request ($\overline{IRQ}$) output signal is generated whenever an internal Interrupt Flag bit is set and the corresponding Interrupt Enable bit is a Logic 1. The Interrupt Request output is an open-drain configuration, thus allowing the $\overline{IRQ}$ signal to be wire-ORed to a common microprocessor $\overline{IRQ}$ input line.

PERIPHERAL PORT A (PA0-PA7)

Peripheral Data Port A is an 8-line, bidirectional bus for the transfer of data, control and status information between the R65C22 and a peripheral device. Each Peripheral Data Port bus line may be individually programmed as either an input or output under control of a Data Direction Register. Data flow direction may be selected on a line-by-line basis with intermixed input and output lines within the same port. When a "0" is written to any bit position of the Data Direction Register, the corresponding line will be programmed as an input. When a "1" is written into any bit position of the register, the corresponding data line will serve as an output. Polarity of the data output is determined by the Output Register, while input data may be latched into the Input Register under control of the CA1 line. All modes are program controlled by the microprocessor by way of the R65C22's internal control registers. Each Peripheral Data Port line represents two TTL loads in the input mode and will drive two standard TTL loads in the output mode. A typical output circuit for Peripheral Data Port A is shown in Figure 3.

PORT A CONTROL LINES (CA1, CA2)

Control lines CA1 and CA2 serve as interrupt inputs or handshake outputs for Peripheral Data Port A. Each line controls an internal Interrupt Flag with a corresponding Interrupt Enable bit. CA1 also controls the latching of Input Data on Port A. CA1 is a high impedance input, while CA2 represents two standard TTL loads in the input mode. In the output mode, CA2 will drive two standard TTL loads.

PORT B (PB0–PB7)

Peripheral Data Port B is an 8-line, bidirectional bus which is controlled by an Output Register, Input Register and Data Direction Register in a manner much the same as Data Port A. With respect to Port B, the output signal on line PB7 may be controlled by Timer 1 while Timer 2 may be programmed to count pulses on the PB6 line. Port B lines represent two standard TTL loads in the input mode and will drive two TTL loads in the output mode. Port B lines are also capable of sourcing 3.2 mA at 1.5 Vdc in the output mode. This allows the outputs to directly drive Darlington transistor circuits. A typical output circuit for Port B is shown in Figure 3.

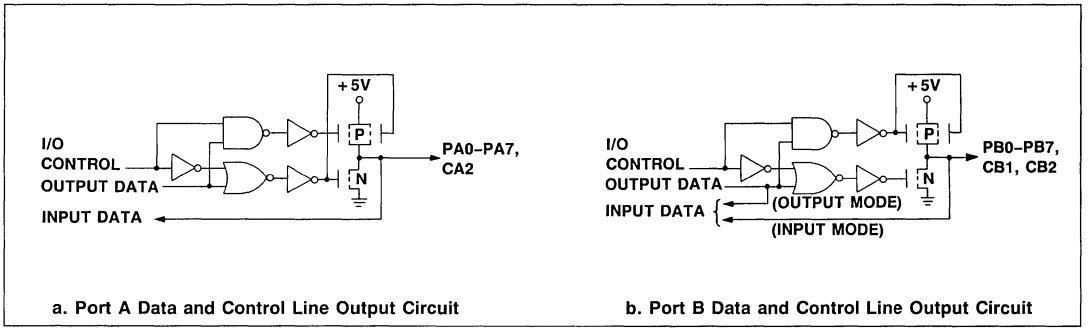
PORT B CONTROL LINES (CB1, CB2)

Control lines CB1 and CB2 serve as interrupt inputs or handshake outputs for Peripheral Data Port B. Like Port A, these two control lines control an internal Interrupt Flag with a corresponding Interrupt Enable bit. These lines also serve as a serial data port under control of the Shift Register (SR). Each control line represents two standard TTL loads in the input mode and can drive two TTL loads in the output mode. Note that CB1 and CB2 can drive Darlington transistor circuits, because they both will source 3.2 mA at 1.5 Vdc. Each line represents two standard TTL loads in the input mode and will drive two standard TTL loads in the output mode.

Table 1. R65C22 Register Addressing

Register Number	RS Coding				Register Desig.	Register/Description	
	RS3	RS2	RS1	RS0		Write (R/$\overline{W}$ = L)	Read (R/$\overline{W}$ = H)
0	0	0	0	0	ORB/IRB	Output Register B	Input Register B
1	0	0	0	1	ORA/IRA	Output Register A	Input Register A
2	0	0	1	0	DDRB	Data Direction Register B	
3	0	0	1	1	DDRA	Data Direction Register A	
4	0	1	0	0	T1C-L	T1 Low-Order Latches	T1 Low-Order Counter
5	0	1	0	1	T1C-H	T1 High-Order Counter	
6	0	1	1	0	T1L-L	T1 Low-Order Latches	
7	0	1	1	1	T1L-H	T1 High-Order Latches	
8	1	0	0	0	T2C-L	T2 Low-Order Latches	T2 Low-Order Counter
9	1	0	0	1	T2C-H	T2 High-Order Counter	
10	1	0	1	0	SR	Shift Register	
11	1	0	1	1	ACR	Auxiliary Control Register	
12	1	1	0	0	PCR	Peripheral Control Register	
13	1	1	0	1	IFR	Interrupt Flag Register	
14	1	1	1	0	IER	Interrupt Enable Register	
15	1	1	1	1	ORA/IRA	Output Register A*	Input Register A*

NOTE: *Same as Register 1 except no handshake.



a. Port A Data and Control Line Output Circuit

b. Port B Data and Control Line Output Circuit

Figure 3. Port A and B Output Circuits

FUNCTIONAL DESCRIPTION

The internal organization of the R65C22 VIA is illustrated in Figure 4.

PORT A AND PORT B OPERATION

The R65C22 VIA has two 8-bit bidirectional I/O ports (Port A and Port B) and each port has two associated control lines.

Each 8-bit peripheral port has a Data Direction Register (DDRA, DDRB) for specifying whether the peripheral pins are to act as inputs or outputs. A "0" in a bit of the Data Direction Register causes the corresponding peripheral pin to act as an input. A "1" causes the pin to act as an output.

Each peripheral pin is also controlled by a bit in the Output Register (ORA, ORB) and the Input Register (IRA, IRB). When the pin is programmed as an output, the voltage on the pin is controlled by the corresponding bit of the Output Register. A "1" in the Output Register causes the output to go high, and a "0" causes the output to go low. Data may be written into Output Register bits corresponding to pins which are programmed as inputs. In this case, however, the output signal is unaffected.

Reading a peripheral port causes the contents of the Input Register (IRA, IRB) to be transferred onto the Data Bus. With input latching disabled, IRA will always reflect the levels on the PA pins. With input latching enabled, IRA will reflect the levels on the PA pins at the time the latching occurred (via CA1).

The IRB register operates similar to the IRA register. However, for pins programmed as outputs there is a difference. When reading IRA, the *level on the pin* determines whether a "0" or a "1" is sensed. When reading IRB, however, the bit stored in the *output register,* ORB, is the bit sensed. Thus, for outputs which have large loading effects and which pull an output "1" down or which pull an output "0" up, reading IRA may result in reading a "0" when a "1" was actually programmed, and reading a "1" when a "0" was programmed. Reading IRB, on the other hand, will read the "1" or "0" level actually programmed, no matter what the loading on the pin.

Figures 5 through 8 illustrate the formats of the port registers.

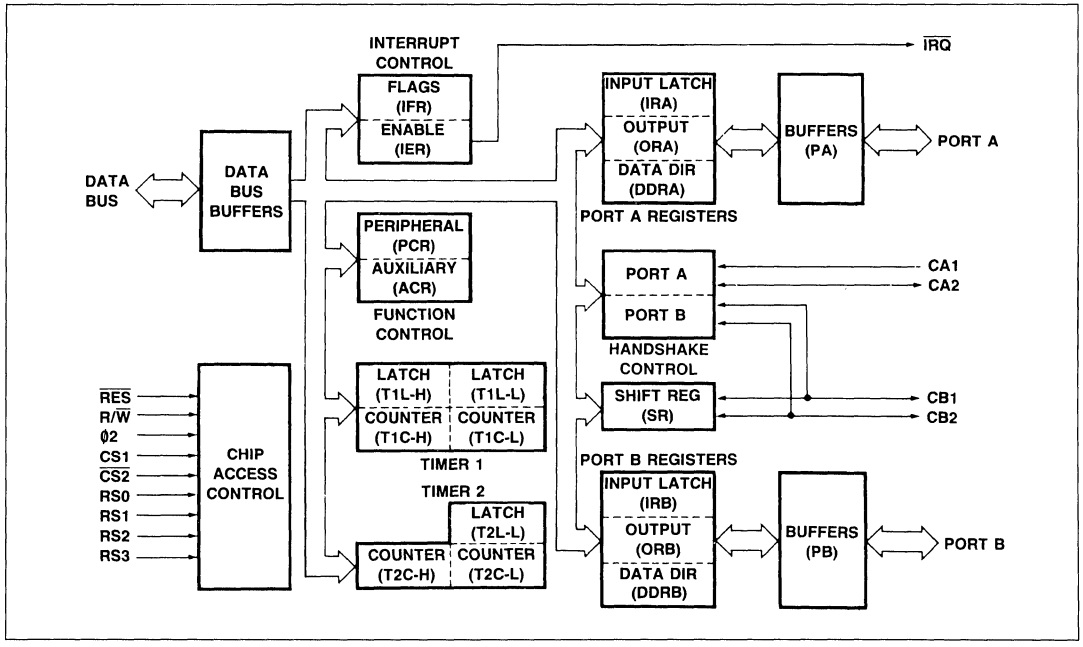


Figure 4. R65C22 VIA Block Diagram

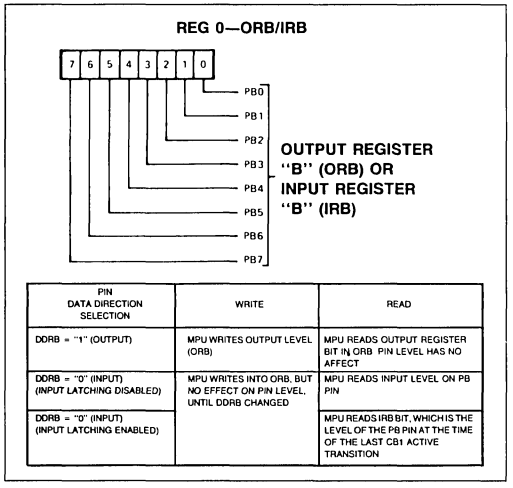
HANDSHAKE CONTROL OF DATA TRANSFERS

The R65C22 allows positive control of data transfers between the system processor and peripheral devices through the operation of "handshake" lines. Port A lines (CA1, CA2) handshake data on both a read and a write operation while the Port B lines (CB1, CB2) handshake on a write operation only.

Read Handshake

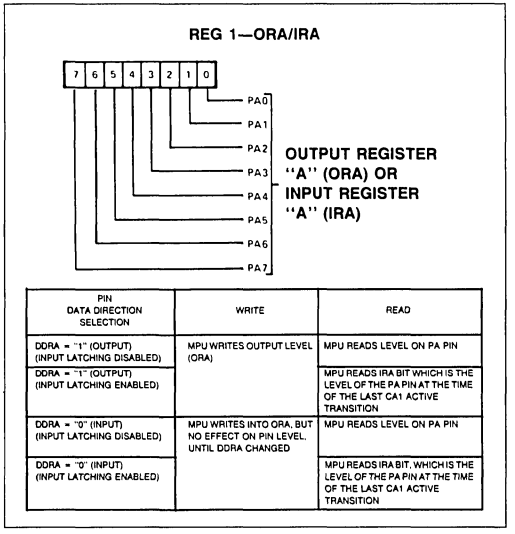
Positive control of data transfers from peripheral devices into the system processor can be accomplished very effectively using Read Handshaking. In this case, the peripheral device must generate the equivalent of a "Data Ready" signal to the processor signifying that valid data is present on the peripheral port. This signal normally interrupts the processor, which then reads the data, causing generation of a "Data Taken" signal. The peripheral device responds by making new data available. This process continues until the data transfer is complete.

In the R65C22, automatic "Read" Handshaking is possible on the Peripheral A port only. The CA1 interrupt input pin accepts the "Data Ready" signal and CA2 generates the "Data Taken" signal. The "Data Ready" signal will set an internal flag which may interrupt the processor or which may be polled under program control. The "Data Taken" signal can either be a pulse or a level which is set low by the system processor and is cleared by the "Data Ready" signal. These options are shown in Figure 9 which illustrates the normal Read Handshake sequence.



PIN DATA DIRECTION SELECTION	WRITE	READ
DDRB = "1" (OUTPUT)	MPU WRITES OUTPUT LEVEL (ORB)	MPU READS OUTPUT REGISTER BIT IN ORB. PIN LEVEL HAS NO AFFECT
DDRB = "0" (INPUT) (INPUT LATCHING DISABLED)	MPU WRITES INTO ORB, BUT NO EFFECT ON PIN LEVEL, UNTIL DDRB CHANGED	MPU READS INPUT LEVEL ON PB PIN
DDRB = "0" (INPUT) (INPUT LATCHING ENABLED)		MPU READS IRB BIT, WHICH IS THE LEVEL OF THE PB PIN AT THE TIME OF THE LAST CB1 ACTIVE TRANSITION

Figure 5. Output Register B (ORB), Input Register B (IRB)



PIN DATA DIRECTION SELECTION	WRITE	READ
DDRA = "1" (OUTPUT) (INPUT LATCHING DISABLED)	MPU WRITES OUTPUT LEVEL (ORA)	MPU READS LEVEL ON PA PIN
DDRA = "1" (OUTPUT) (INPUT LATCHING ENABLED)		MPU READS IRA BIT WHICH IS THE LEVEL OF THE PA PIN AT THE TIME OF THE LAST CA1 ACTIVE TRANSITION
DDRA = "0" (INPUT) (INPUT LATCHING DISABLED)	MPU WRITES INTO ORA, BUT NO EFFECT ON PIN LEVEL, UNTIL DDRA CHANGED	MPU READS LEVEL ON PA PIN
DDRA = "0" (INPUT) (INPUT LATCHING ENABLED)		MPU READS IRA BIT, WHICH IS THE LEVEL OF THE PA PIN AT THE TIME OF THE LAST CA1 ACTIVE TRANSITION

Figure 6. Output Register A (ORA), Input Register A (IRA)

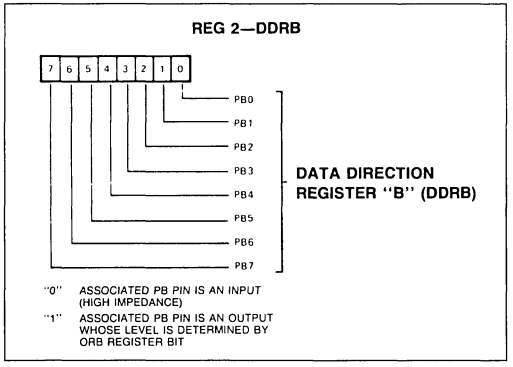


Figure 7. Data Direction Register B (DDRB)

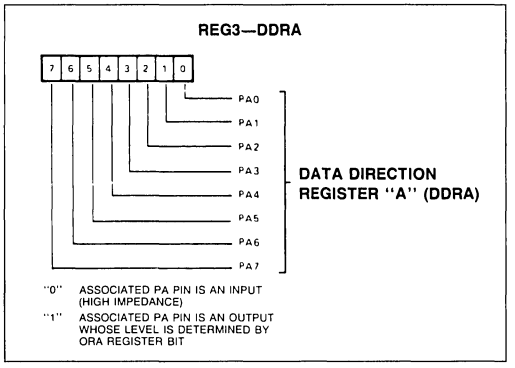


Figure 8. Data Direction Register A (DDRA)

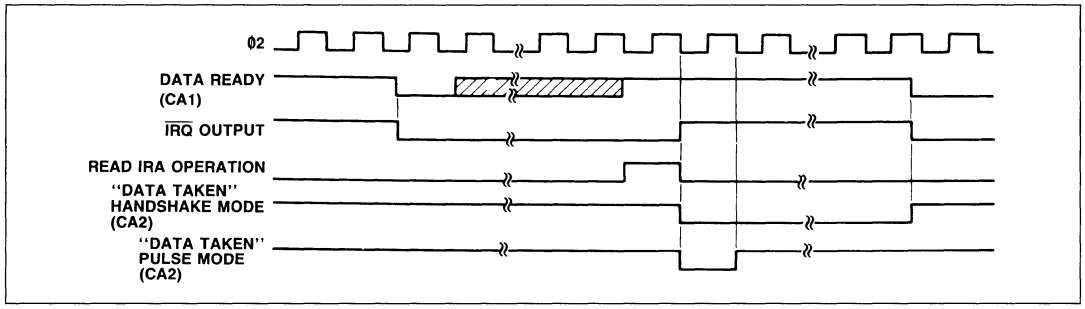


Figure 9. Read Handshake Timing (Port A Only)

Write Handshake

The sequence of operations which allows handshaking data from the system processor to a peripheral device is very similar to that described for Read Handshaking. However, for Write Handshaking, the R65C22 generates the "Data Ready" signal and the peripheral device must respond with the "Data Taken" signal. This can be accomplished on both the PA port and the PB port on the R65C22. CA2 or CB2 act as a "Data Ready" output in either the handshake mode or pulse mode and CA1 or CB1 accept the "Data Taken" signal from the peripheral device, setting the interrupt flag and clearing the "Data Ready" output. This sequence is shown in Figure 10.

Latching

The PA port and the PB port on the R65C22 can be enabled in the Auxiliary Control Register (Figure 14) to be latched by their individual port control lines (CA1, CB1). Latching is selectable to be on the rising or falling edge of the signal at each individual port control line. Selection of operating modes for CA1, CA2, CB1 and CB2 is accomplished by the Peripheral Control Register (Figure 11).

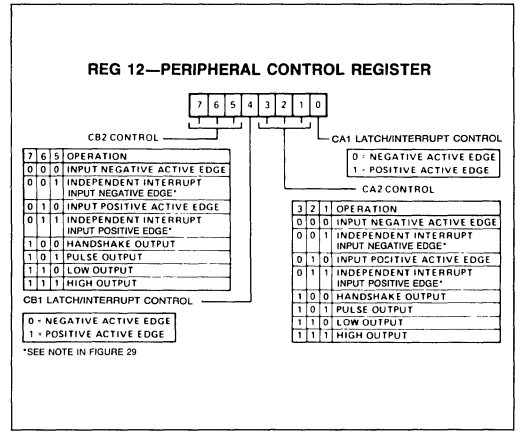


Figure 11. Peripheral Control Register (PCR)

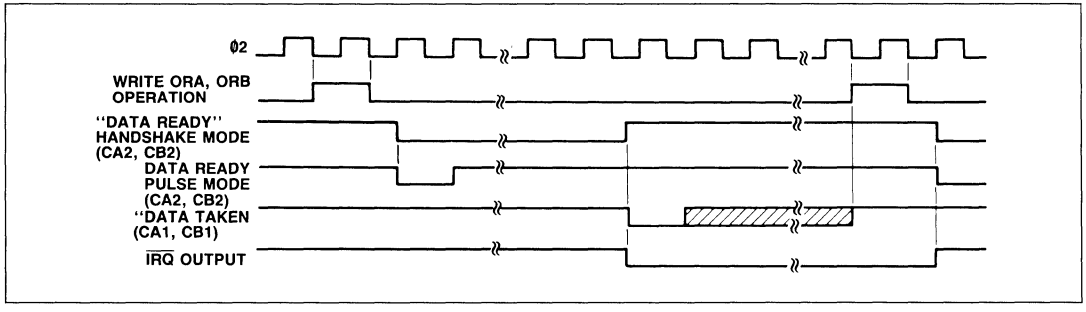


Figure 10. Write Handshake Timing

COUNTER/TIMERS

There are two independent 16-bit counter/timers (called Timer 1 and Timer 2) in the R65C22. Each timer is controlled by writing bits into the Auxiliary Control Register (ACR) to select the mode of operation (Figure 14).

Timer 1 Operation

Interval Timer T1 consists of two 8-bit latches (Figure 12) and a 16-bit counter (Figure 13). The latches store data which is to be loaded into the counter. After loading, the counter decrements at Ø2 clock rate. Upon reaching zero, an interrupt flag is set, and IRQ goes low if the T1 interrupt is enabled. Timer 1 then disables any further interrupts and automatically transfers the contents of the latches into the counter and continues to decrement. In addition, the timer may be programmed to invert the output signal on peripheral pin PB7 each time it "times-out". Each of these modes is discussed separately below.

Note that the processor does not write directly into the low-order counter (T1C-L). Instead, this half of the counter is loaded automatically from the low order latch (T1L-L) when the processor writes into the high order counter (T1C-H). In fact, it may not be necessary to write to the low order counter in some applications since the timing operation is triggered by writing to the high order latch.

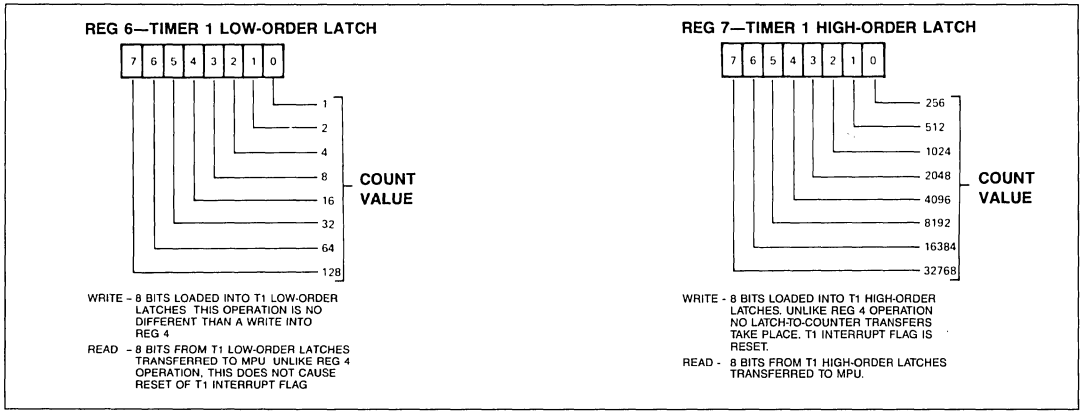


Figure 12. Timer 1 (T1) Latch Registers

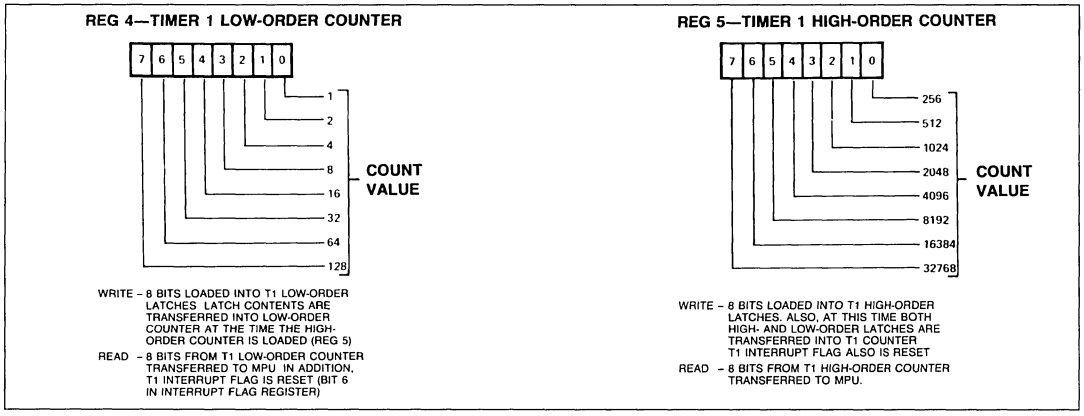


Figure 13. Timer 1 (T1) Counter Registers

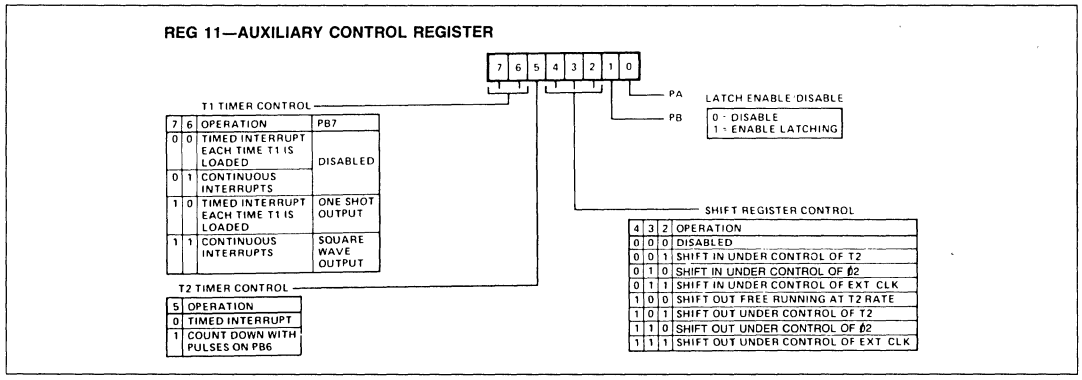


Figure 14. Auxiliary Control Register (ACR)

Timer 1 One-Shot Mode

The Timer 1 one-shot mode generates a single interrupt for each timer load operation. As with any interval timer, the delay between the "write T1C-H" operation and generation of the processor interrupt is a direct function of the data loaded into the timing counter. In addition to generating a single interrupt, Timer 1 can be programmed to produce a single negative pulse on the PB7 peripheral pin. With the output enabled (ACR7 = 1) a "write T1C-H" operation will cause PB7 to go low. PB7 will return high when Timer 1 times out. The result is a single programmable width pulse.

Timing for the R65C22 interval timer one-shot modes is shown in Figure 15.

In the one-shot mode, writing into the T1L-H has no effect on the operation of Timer 1. However, it will be necessary to assure that the low order latch contains the proper data before initiating the count-down with a "write T1C-H" operation. When the processor writes into the high order counter (T1C-H), the T1 interrupt flag will be cleared, the contents of the low order latch will be transferred into the low order counter, and the timer will begin to decrement at system clock rate. If the PB7 output is enabled, this signal will go low on the falling edge of Ø2 following the write operation. When the counter reaches zero, the T1 interrupt flag will be set, the $\overline{IRQ}$ pin will go low (interrupt enabled), and the signal on PB7 will go high. At this time the counter will continue to decrement at system clock rate. This allows the system processor to read the contents of the counter to determine the time since interrupt. However, the T1 interrupt flag cannot be set again unless it has been cleared as described in this specification.

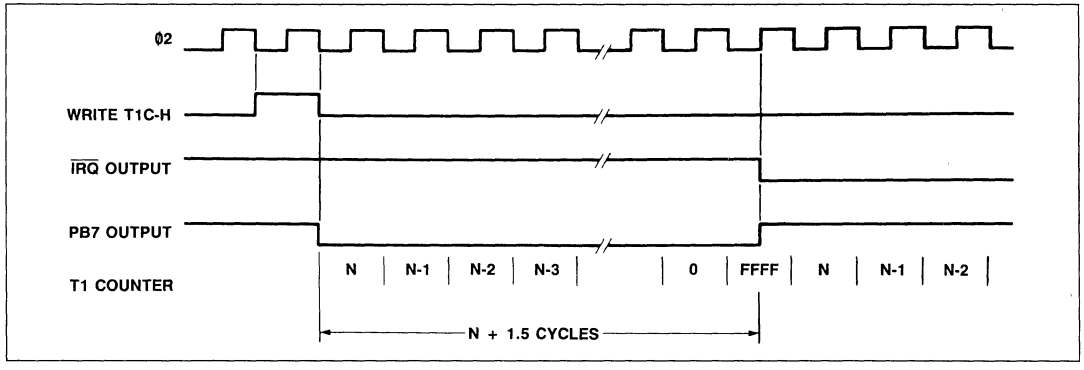


Figure 15. Timer 1 One-Shot Mode Timing

Timer 1 Free-Run Mode

The most important advantage associated with the latches in T1 is the ability to produce a continuous series of evenly spaced interrupts and the ability to produce a square wave on PB7 whose frequency is not affected by variations in the processor interrupt response time. This is accomplished in the "free-running" mode.

In the free-running mode, the interrupt flag is set and the signal on PB7 is inverted each time the counter reaches zero at which time the timer automatically transfers the contents of the latch into the counter (16 bits) and continues to decrement from there. The interrupt flag can be cleared by writing T1C-H or T1L-H, by reading T1C-L, or by writing directly into the flag as described later. However, it is not necessary to rewrite the timer to enable setting the interrupt flag on the next time-out.

All interval timers in the R65C22 are "re-triggerable". Rewriting the counter will always re-initialize the time-out period. In fact, the time-out can be prevented completely if the processor continues to rewrite the timer before it reaches zero. Timer 1 will operate in this manner if the processor writes into the high order counter (T1C-H). However, by loading the latches only, the processor can access the timer during each down-counting operation without affecting the time-out in process. Instead, the data loaded into the latches will determine the length of the next time-out period. This capability is particularly valuable in the free-running mode with the output enabled. In this mode, the signal on PB7 is inverted and the interrupt flag is set with each time-out. By responding to the interrupts with new data for the latches, the processor can determine the period of the next half cycle during each half cycle of the output signal on PB7. In this manner, very complex waveforms can be generated.

A precaution to take in the use of PB7 as the timer output concerns the Data Direction Register contents for PB7. *Both* DDRB bit 7 and ACR bit 7 must be 1 for PB7 to function as the timer output. If one is 1 and other is 0, then PB7 functions as a normal outpin pin, controlled by ORB bit 7.

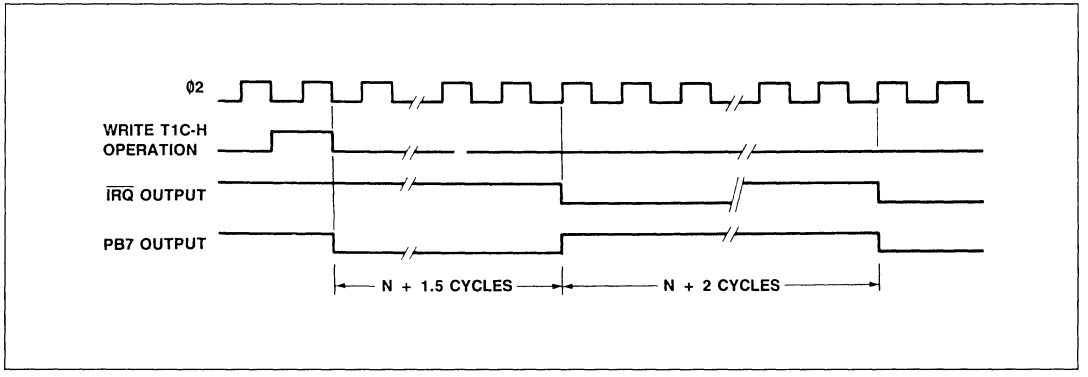


Figure 16. Timer 1 Free-Run Mode Timing

Timer 2 Operation

Timer 2 operates as an interval timer (in the "one-shot" mode only), or as a counter for counting negative pulses on the PB6 peripheral pin. A single control bit in the Auxiliary Control Register selects between these two modes. This timer is comprised of a "write-only" lower-order latch (T2L-L), a "read-only" low-order counter (T2C-L) and a read/write high order counter (T2C-H). The counter registers act as a 16-bit counter which decrements at Ø2 rate. Figure 17 illustrates the T2 Latch/Counter Registers.

Timer 2 One-Shot Mode

As an interval timer, T2 operates in the "one-shot" mode similar to Timer 1. In this mode, T2 provides a single interrupt for each "write T2C-H" operation. After timing out, the counter will continue to decrement. However, setting of the interrupt flag is disabled after initial time-out so that it will not be set by the counter decrementing again through zero. The processor must rewrite T2C-H to enable setting of the interrupt flag. The interrupt flag is cleared by reading T2C-L or by writing T2C-H. Timing for this operation is shown in Figure 18.

Timer 2 Pulse Counting Mode

In the pulse counting mode, T2 counts a predetermined number of negative-going pulses on PB6. This is accomplished by first loading a number into T2. Writing into T2C-H clears the interrupt flag and allows the counter to decrement each time a pulse is applied to PB6. The interrupt flag is set when T2 counts down past zero. The counter will then continue to decrement with each pulse on PB6. However, it is necessary to rewrite T2C-H to allow the interrupt flag to set on a subsequent time-out. Timing for this mode is shown in Figure 19. The pulse must be low on the leading edge of Ø2.

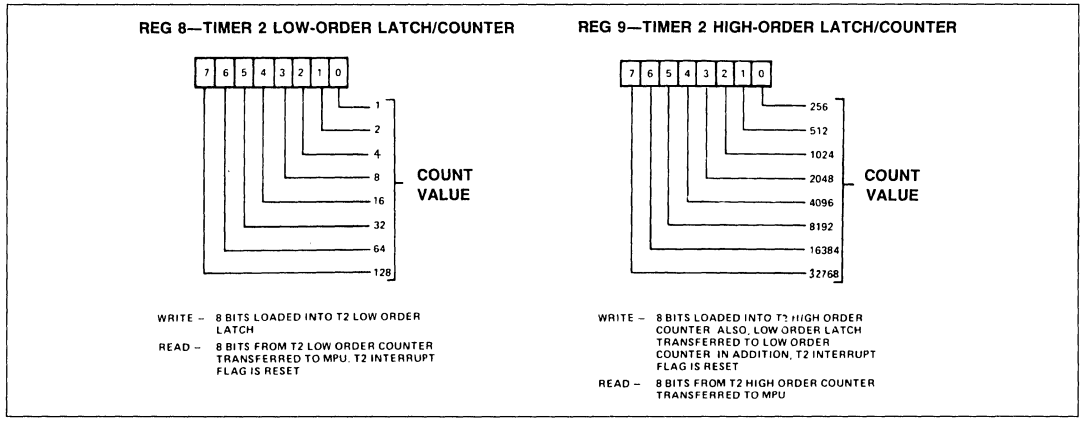


Figure 17. Timer 2 (T2) Latch/Counter Registers

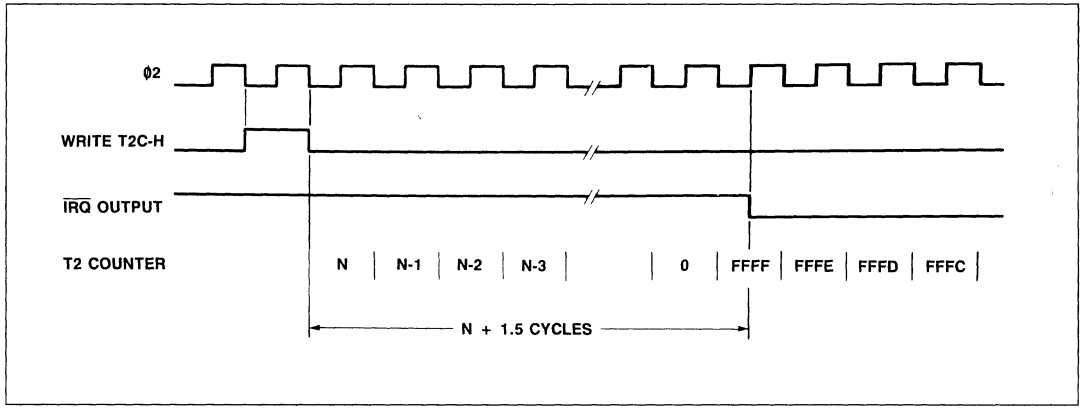


Figure 18. Timer 2 One-Shot Mode Timing

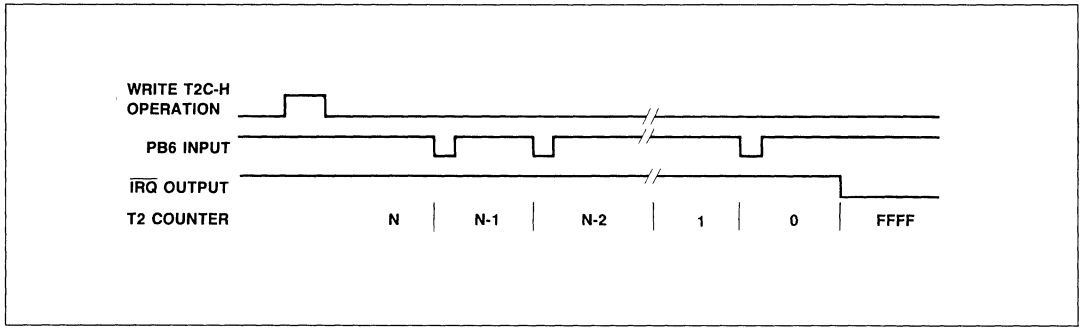


Figure 19. Timer 2 Pulse Counting Mode

SHIFT REGISTER OPERATION

The Shift Register (SR) performs serial data transfers into and out of the CB2 pin under control of an internal modulo-8 counter. Serial data transfer in and out of the Shift Register (SR) begin with the most significant bit (MSB) first. Shift pulses can be applied to the CB1 pin from an external source or, with the proper mode selection, shift pulses generated internally will appear on the CB1 pin for controlling external devices.

The control bits which select the various shift register operating modes are located in the Auxiliary Control Register. Figure 20 illustrates the configuration of the SR data bits and Figure 21 shows the SR control bits of the ACR.

SR Mode 0 — Shift Register Interrupt Disabled

Mode 0 disables the Shift Register interrupt. In this mode the microprocessor can write or read the SR and the SR will shift on each CB1 positive edge shifting in the value on CB2. In this mode the SR interrupt Flag is disabled (held to a logic 0).

SR Mode 1 — Shift In Under Control of T2

In mode 1, the shifting rate is controlled by the low order 8 bits of T2 (Figure 22). Shift pulses are generated on the CB1 pin to control shifting in external devices. The time between transitions of this output clock is a function of the system clock period and the contents of the low order T2 latch (N).

The shifting operation is triggered by the read or write of the SR if the SR flag is set in the IFR. Otherwise the first shift will occur at the next time-out of T2 after a read or write of the SR. The input data should change before the positive-going edge of CB1 clock pulse. This data is shifted into the shift register during the ϕ2 clock cycle following the positive-going edge of the CB1 clock pulse. After 8 CB1 clock pulses, the shift register interrupt flag will set and $\overline{IRQ}$ will go low.

SR Mode 2 — Shift In Under ϕ2 Control

In mode 2, the shift rate is a direct function of the system clock frequency (Figure 23). CB1 becomes an output which generates shift pulses for controlling external devices. Timer 2 operates as an independent interval timer and has no effect on SR. The shifting operation is triggered by reading or writing the Shift Register. Data is shifted, first into bit 0 and is then shifted into the next higher order bit of the shift register on the trailing edge of each ϕ2 clock pulse. After 8 clock pulses, the shift register interrupt flag will be set, and the output clock pulses on CB1 will stop.

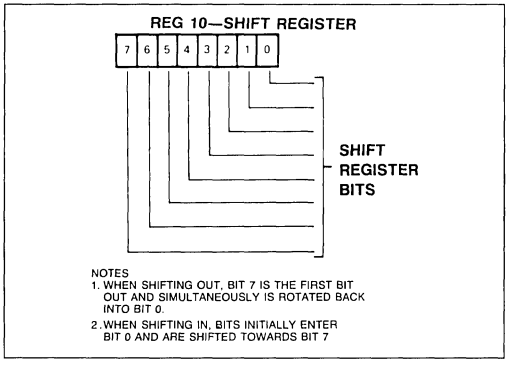
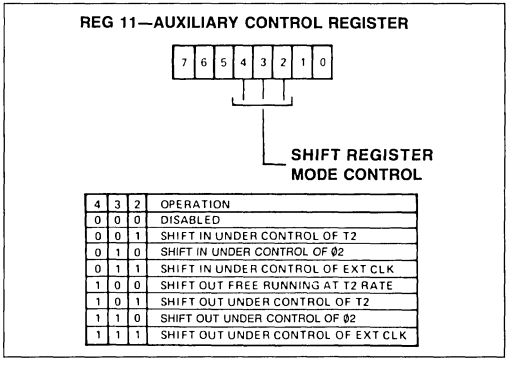


Figure 20. Shift Register



4	3	2	OPERATION
0	0	0	DISABLED
0	0	1	SHIFT IN UNDER CONTROL OF T2
0	1	0	SHIFT IN UNDER CONTROL OF ϕ2
0	1	1	SHIFT IN UNDER CONTROL OF EXT CLK
1	0	0	SHIFT OUT FREE RUNNING AT T2 RATE
1	0	1	SHIFT OUT UNDER CONTROL OF T2
1	1	0	SHIFT OUT UNDER CONTROL OF ϕ2
1	1	1	SHIFT OUT UNDER CONTROL OF EXT CLK

Figure 21. Shift Register Modes

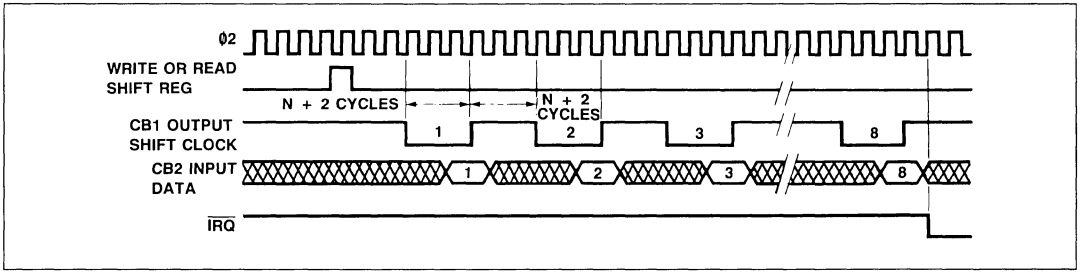


Figure 22. SR Mode 1 — Shift In Under T2 Control

SR Mode 3 — Shift In Under CB1 Control

In mode 3, external pin CB1 becomes an input (Figure 24). This allows an external device to load the shift register at its own pace. The shift register counter will interrupt the processor each time 8 bits have been shifted in. The shift register stops after 8 counts and must be reset to start again. Reading or writing the Shift Register resets the Interrupt Flag and initializes the SR counter to count another 8 pulses.

Note that the data is shifted during the first system clock cycle following the positive-going edge of the CB1 shift pulse. For this reason, data must be held stable during the first full cycle following CB1 going high.

SR Mode 4 — Shift Out Under T2 Control (Free-Run)

Mode 4 is very similar to mode 1 in which the shifting rate is set by T2. However, in mode 4 the SR Counter does not stop the shifting operation (Figure 25). Since the Shift Register bit 7 (SR7) is recirculated back into bit 0, the 8 bits loaded into the shift register will be clocked onto CB2 repetitively. In this mode the shift register counter is disabled.

SR Mode 5 — Shift Out Under T2 Control

In mode 5, the shift rate is controlled by T2 (as in mode 1). The shifting operation is triggered by the read or write of the SR if the SR flag is set in the IFR (Figure 26). Otherwise the first shift will occur at the next time-out of T2 after a read or write of the SR. However, with each read or write of the shift register the SR Counter is reset and 8 bits are shifted onto CB2. At the same time, 8 shift pulses are generated on CB1 to control shifting in external devices. After the 8 shift pulses, the shifting is disabled, the SR Interrupt Flag is set and CB2 remains at the last data level.

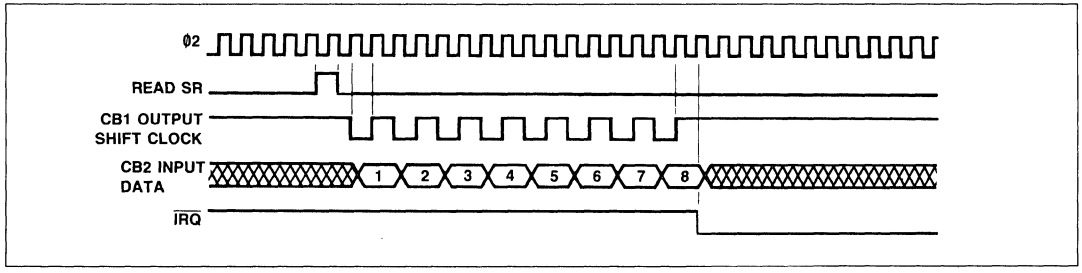


Figure 23. SR Mode 2 — Shift In Under Ø2 Control

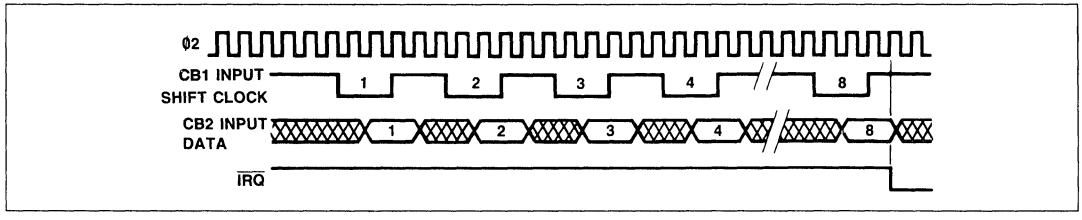


Figure 24. SR Mode 3 — Shift In Under CB1 Control

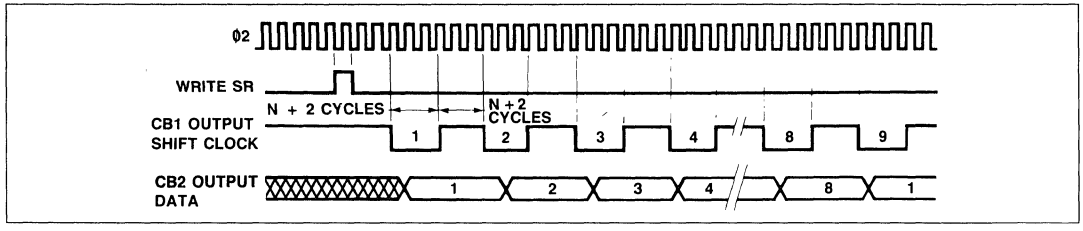


Figure 25. SR Mode 4 — Shift Out Under T2 Control (Free-Run)

SR Mode 6 — Shift Out Under Ø2 Control

In mode 6, the shift rate is controlled by the Ø2 system clock (Figure 27).

SR Mode 7 — Shift Out Under CB1 Control

In mode 7, shifting is controlled by pulses applied to the CB1 pin by an external device (Figure 28). The SR counter sets the SR Interrupt Flag each time it counts 8 pulses but it does not disable the shifting function. Each time the microprocessor, writes or reads the shift register, the SR Interrupt Flag is reset and the SR counter is initialized to begin counting the next 8 shift pulses on pin CB1. After 8 shift pulses, the Interrupt Flag is set. The microprocessor can then load the shift register with the next byte of data.

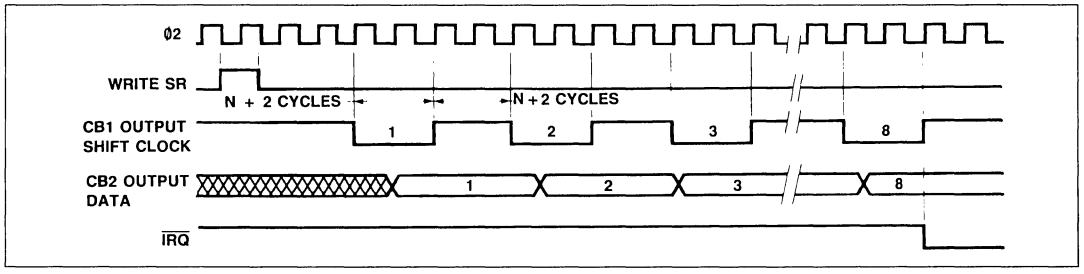


Figure 26. SR Mode 5 — Shift Out Under T2 Control

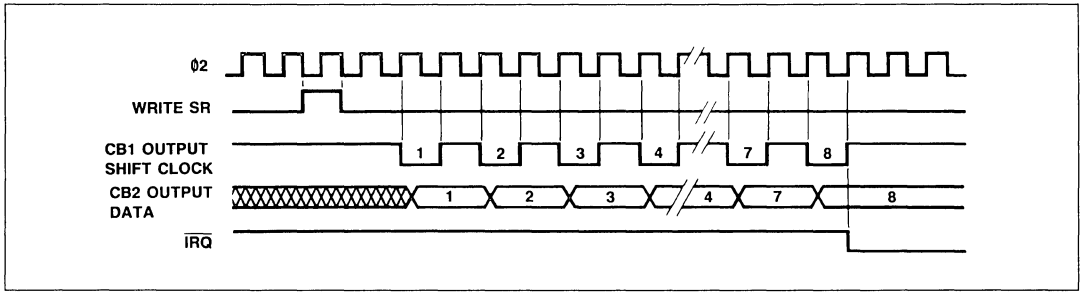


Figure 27. SR Mode 6 — Shift Out Under Ø2 Control

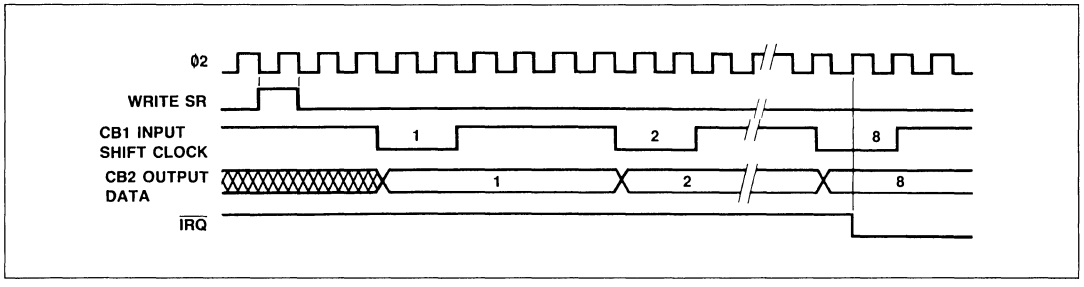


Figure 28. SR Mode 7 — Shift Out Under CB1 Control

INTERRUPT OPERATION

Controlling interrupts within the R65C22 involves three principal operations. These are flagging the interrupts, enabling interrupts and signaling to the processor that an active interrupts exists within the chip. Interrupt flags are set in the Interrupt Flag Register (IFR) by conditions detected within the R65C22 or on inputs to the R65C22. These flags normally remain set until the interrupt has been serviced. To determine the source of an interrupt, the microprocessor must examine these flags in order, from highest to lowest priority.

Associated with each interrupt flag is an interrupt enable bit in the Interrupt Enable Register (IER). This can be set or cleared by the processor to enable interrupting the processor from the corresponding interrupt flag. If an interrupt flag is set to a logic 1 by an interrupting condition, and the corresponding interrupt enable bit is set to a 1, the Interrupt Request Output ($\overline{IRQ}$) will go low. $\overline{IRQ}$ is an "open-collector" output which can be "wire-OR'ed" with other devices in the system to interrupt the processor.

Interrupt Flag Register (IFR)

In the R65C22, all the interrupt flags are contained in one register, i.e., the IFR (Figure 29). In addition, bit 7 of this register will be read as a logic 1 when an interrupt exists within the chip. This allows very convenient polling of several devices within a system to locate the source of an interrupt.

The Interrupt Flag Register (IFR) may be read directly by the processor. In addition, individual flag bits may be cleared by writing a "1" into the appropriate bit of the IFR. When the proper chip select and register signals are applied to the chip, the contents of this register are placed on the data bus. Bit 7 indicates the status of the $\overline{IRQ}$ output. This bit corresponds to the logic function: $\overline{IRQ}$ = IFR6 x IER6 + IFR5 x IER5 + IFR4 x IER4 + IFR3 x IER3 + IFR2 x IER2 + IFR1 x IER1 + IFR0 x IER0.

Note:

x = logic AND, + = Logic OR.

The IFR bit 7 is not a flag. Therefore, this bit is not directly cleared by writing a logic 1 into it. It can only be cleared by clearing all the flags in the register or by disabling all the active interrupts as discussed in the next section.

Interrupt Enable Register (IER)

For each interrupt flag in IFR, there is a corresponding bit in the Interrupt Enable Register (IER) (Figure 30). Individual bits in the IER can be set or cleared to facilitate controlling individual interrupts without affecting others. This is accomplished by writing to the (IER) after bit 7 set or cleared to, in turn, set or clear selected enable bits. If bit 7 of the data placed on the system data bus during this write operation is a 0, each 1 in bits 6 through 0 clears the corresponding bit in the Interrupt Enable Register. For each zero in bits 6 through 0, the corresponding bit is unaffected.

Selected bits in the IER can be set by writing to the IER with bit 7 in the data word set to a 1. In this case, each 1 in bits 6 through 0 will set the corresponding bit. For each zero, the corresponding bit will be unaffected. This individual control of the setting and clearing operations allows very convenient control of the interrupts during system operation.

In addition to setting and clearing IER bits, the contents of this register can be read at any time. Bit 7 will be read as a logic 1, however.

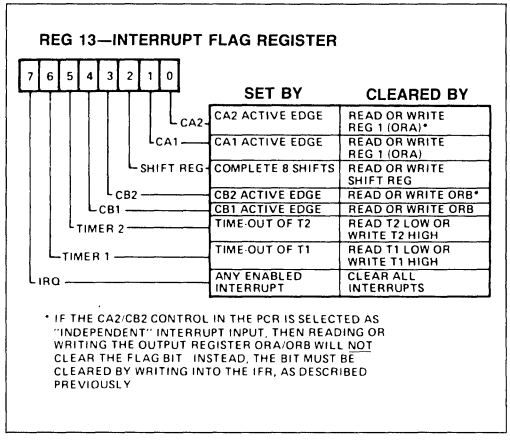


Figure 29. Interrupt Flag Register (IFR)

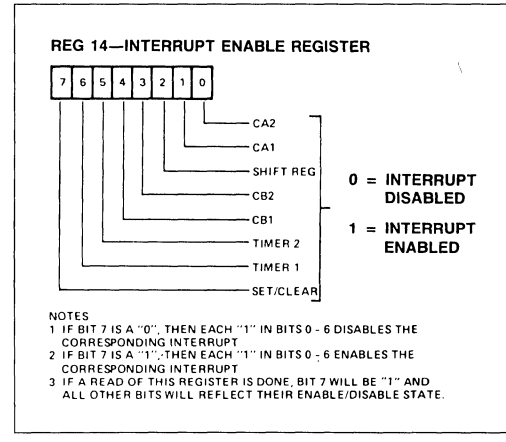


Figure 30. Interrupt Enable Register (IER)

SWITCHING CHARACTERISTICS

(V_{CC} = 5.0 Vdc ±5%, V_{SS} = 0, T_A = T_L to T_H, unless otherwise noted)

PERIPHERAL INTERFACE TIMING

Parameter	Symbol	Min.	Max.	Unit	Figure
Rise and Fall Time for CA1, CB1, CA2 and CB2 Input Signals	t_r, t_f	—	1.0	μs	—
Delay Time, Clock Negative Transition to CA2 Negative Transition (read handshake or pulse mode)	t_{CA2}	—	1.0	μs	31a, 31b
Delay Time, Clock Negative Transition to CA2 Positive Transition (pulse mode)	t_{RS1}	—	1.0	μs	31a
Delay Time, CA1 Active Transition to CA2 Positive Transition (handshake mode)	t_{RS2}	—	2.0	μs	31b
Delay Time, Clock Positive Transition to CA2 or CB2 Negative Transition (write handshake)	t_{WHS}	0.05	1.0	μs	31c, 31d
Delay Time, Periphral Data Valid to CB2 Negative Transition	t_{DS}	0.20	1.5	μs	31c, 31d
Delay Time, Clock Positive Transition to CA2 or CB2 Positive Transition (pulse mode)	t_{RS3}	—	1.0	μs	31c
Delay Time, CA1 or CB1 Active Transition to CA2 or CB2 Positive Transition (handshake mode)	t_{RS4}	—	2.0	μs	31d
Delay Time Required from CA2 Output to CA1 Active Transition (handshake mode)	t_{21}	400	—	ns	31d
Setup Time, Peripheral Data Valid to CA1 or CB1 Active Transition (input latching)	t_{IL}	300	—	ns	31e
CA1, CB1 Setup Prior to Transition to Arm Latch	t_{AL}	300	—	ns	31e
Peripheral Data Hold After CA1, CB1 Transition	t_{PDH}	150	—	ns	31e
Shift-Out Delay Time — Time from Ø2 Falling Edge to CB2 Data Out	t_{SR1}	—	300	ns	31f
Shift-In Setup Time — Time from CB2 Data In to Ø2 Rising Edge	t_{SR2}	300	—	ns	31g
External Shift Clock (CB1) Setup Time Relative to Ø2 Trailing Edge	t_{SR3}	100	T_{CY}	ns	31g
Pulse Width — PB6 Input Pulse	t_{IPW}	2 × T_{CY}	—		31i
Pulse Width — CB1 Input Clock	t_{ICW}	2 × T_{CY}	—		31h
Pulse Spacing — PB6 Input Pulse	t_{IPS}	2 × T_{CY}	—		31i
Pulse Spacing — CB1 Input Pulse	t_{ICS}	2 × T_{CY}	—		31h

BUS TIMING

Parameter	Symbol	1 MHz		2 MHz		3 MHz		4 MHZ		Unit	Figure
		Min	Max	Min	Max	Min	Max	Min	Max		
Cycle Time	t_{CY}	1000	—	500	—	330	—	250	—	ns	
Phase 2 Pulse Width High	t_{PWH}	470	—	240	—	160	—	120	—	ns	32a,
Phase 2 Pulse Width Low	t_{PWL}	470	—	240	—	160	—	120	—	ns	32b
Phase 2 Transition	$t_{R,F}$	—	30	—	30	—	30	—	30	ns	
Read											
Select, R/$\overline{W}$ Setup	t_{ACR}	160	—	90	—	65	—	45	—	ns	
Select, R/$\overline{W}$ Hold	t_{CAR}	0	—	0	—	0	—	0	—	ns	
Data Bus Delay	t_{CDR}	—	320	—	150	—	130	—	75	ns	32a
Data Bus Hold	t_{HR}	10	—	10	—	10	—	10	—	ns	
Peripheral Data Setup	t_{PCR}	300	—	150	—	110	—	75	—	ns	
Write											
Select R/$\overline{W}$ Setup	t_{ACW}	160	—	90	—	65	—	45	—	ns	
Select, R/$\overline{W}$ Hold	t_{CAW}	0	—	0	—	0	—	0	—	ns	
Data Bus Setup	t_{DCW}	195	—	75	—	65	—	45	—	ns	32b
Data Bus Hold	t_{HW}	10	—	10	—	10	—	10	—	ns	
Peripheral Data Delay	t_{CPW}	—	1000	—	500	—	330	—	250	ns	

PERIPHERAL INTERFACE WAVEFORMS

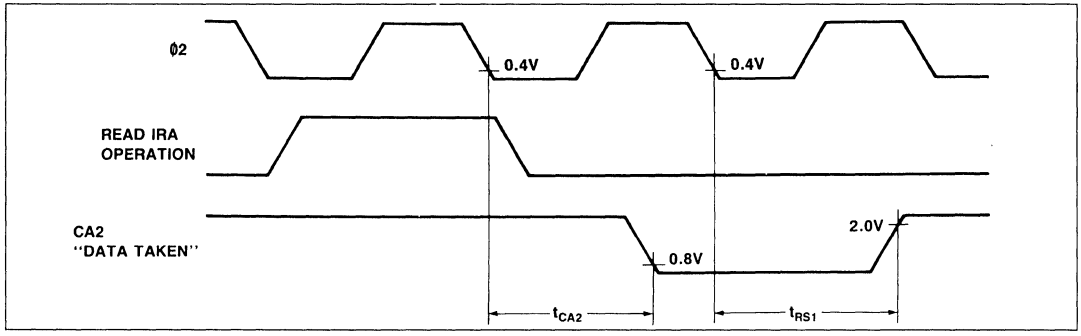


Figure 31a. CA2 Timing for Read Handshake, Pulse Mode

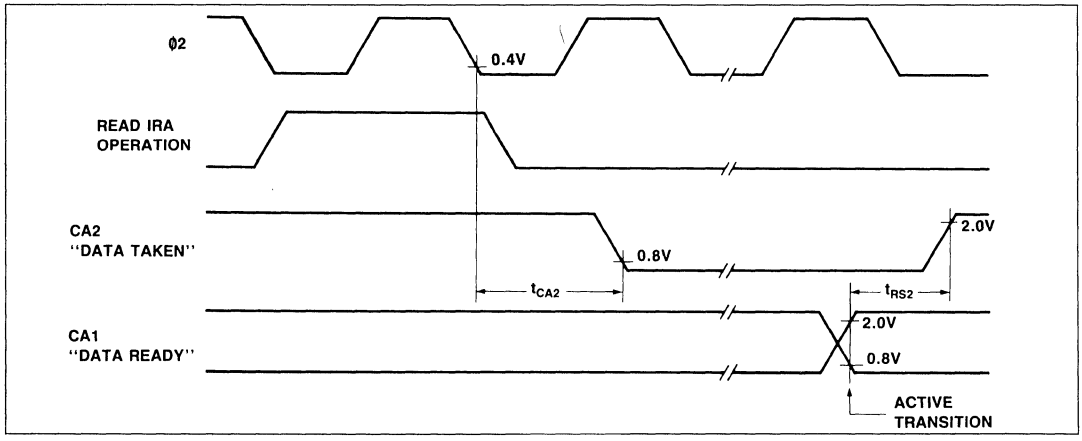


Figure 31b. CA2 Timing for Read Handshake, Handshake Mode

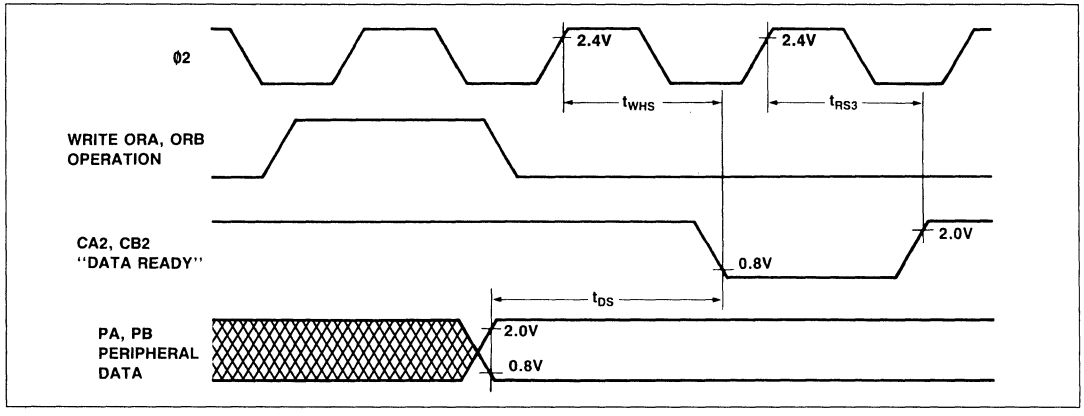


Figure 31c. CA2, CB2 Timing for Write Handshake, Pulse Mode

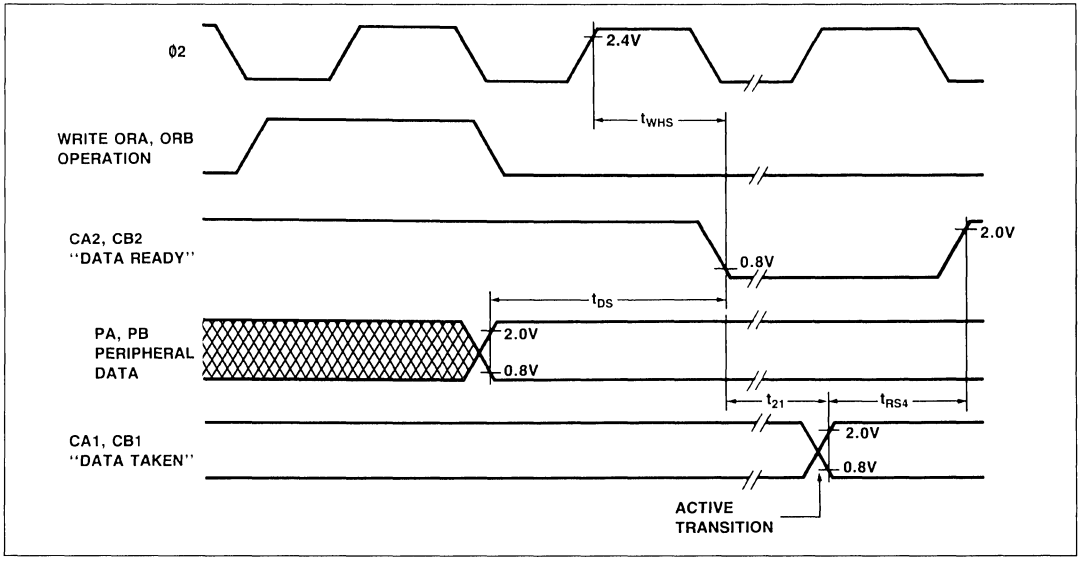


Figure 31d. CA2, CB2 Timing for Write Handshake, Handshake Mode

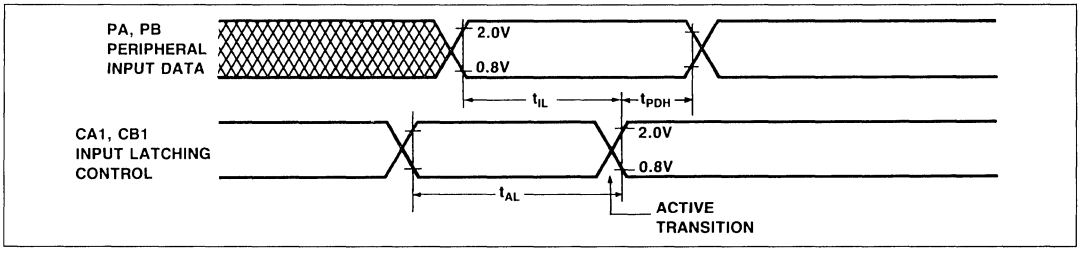


Figure 31e. Peripheral Data Input Latching Timing

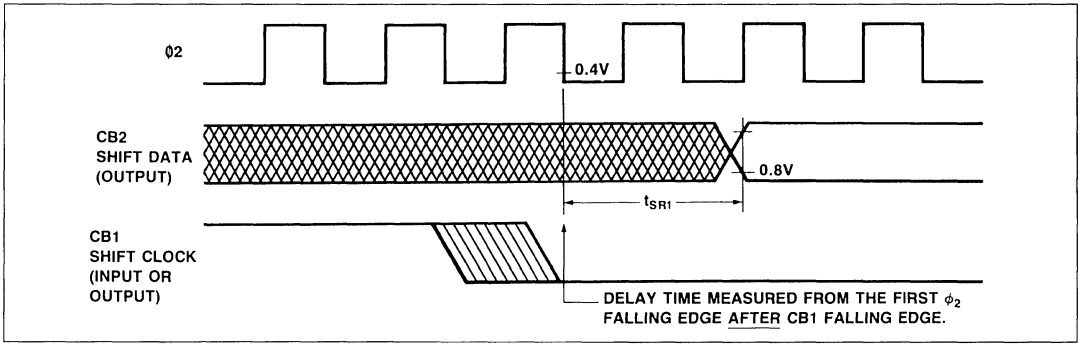


Figure 31f. Timing for Shift Out with Internal or External Shift Clocking

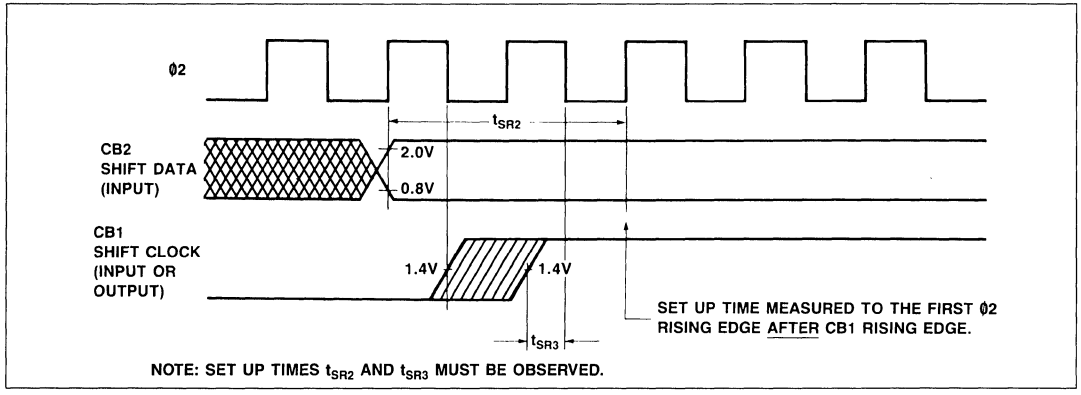


Figure 31g. Timing for Shift In with Internal or External Shift Clocking

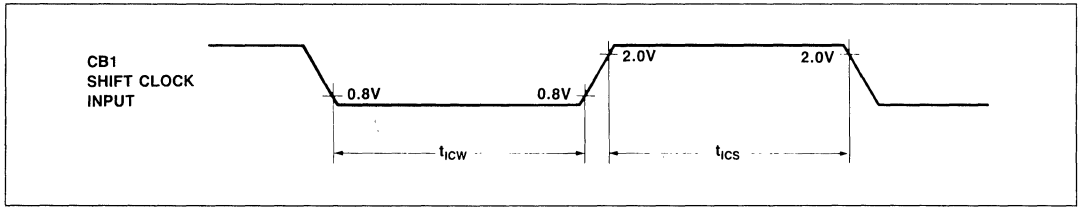


Figure 31h. External Shift Clock Timing

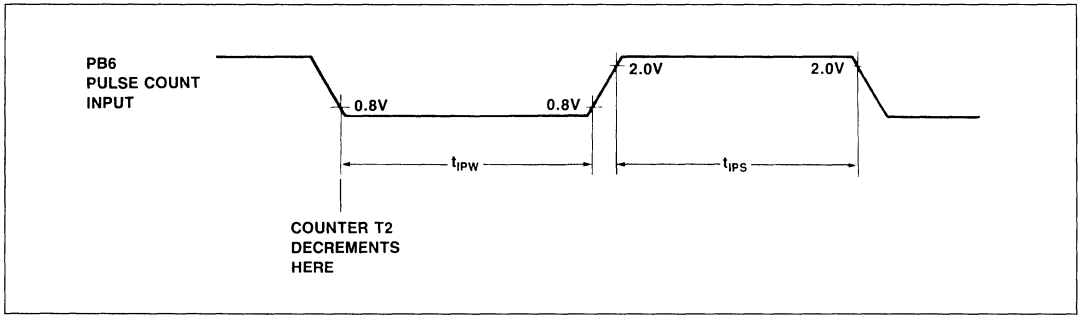


Figure 31i. Pulse Count Input Timing

BUS TIMING WAVEFORMS

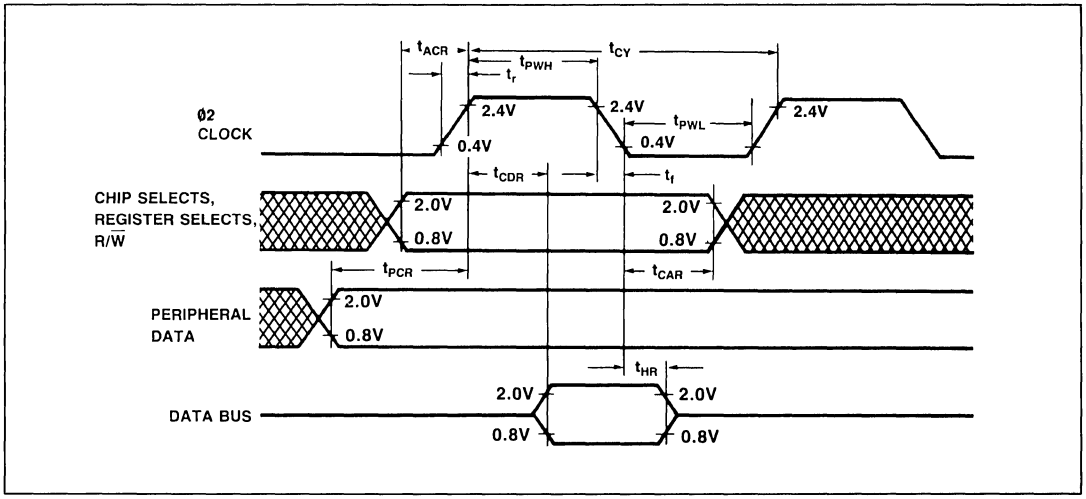


Figure 32a. Read Timing Waveforms

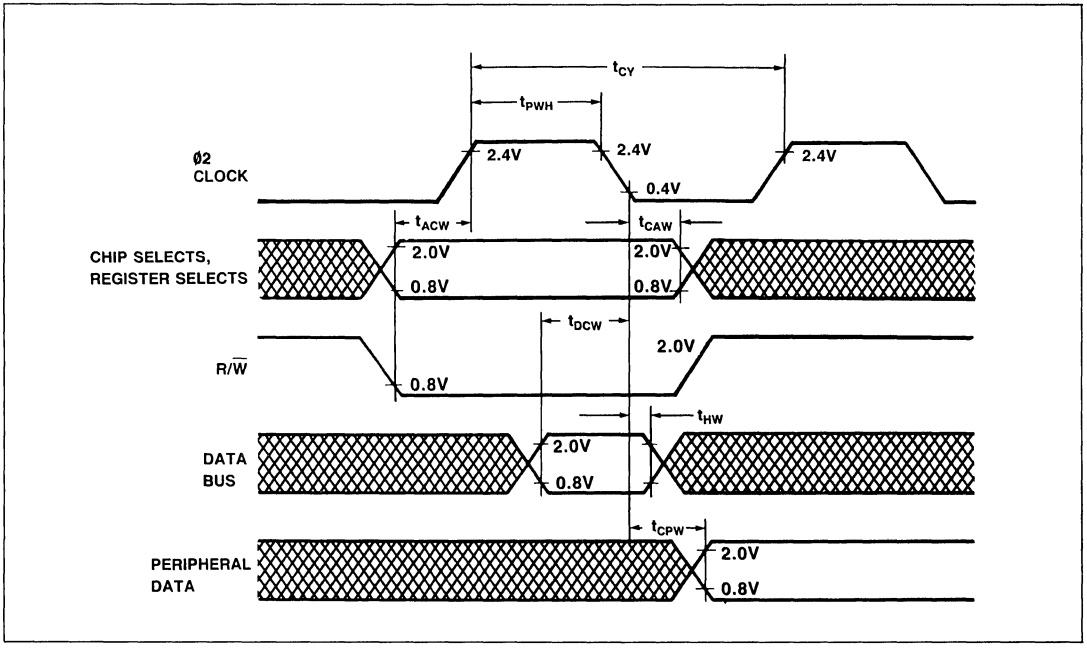


Figure 32b. Write Timing Waveforms

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to +7.0	Vdc
Input Voltage	V_{IN}	−0.3 to V_{CC} +0.3	Vdc
Output Voltage	V_{OUT}	−0.3 to V_{CC} +0.3	Vdc
Operating Temperature Commercial Industrial	T_A	 0 to +70 −40 to +85	°C
Storage Temperature	T_{STG}	−55 to +150	°C

*NOTE: Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the other sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING CONDITIONS

Parameter	Symbol	Value
Supply Voltage	V_{CC}	5V ±5%
Temperature Range Commercial Industrial	T_A	T_L to T_H 0°C to 70°C −40°C to +85°C

ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0 Vdc ±5%, V_{SS} = 0, T_A = T_L to T_H, unless otherwise noted)

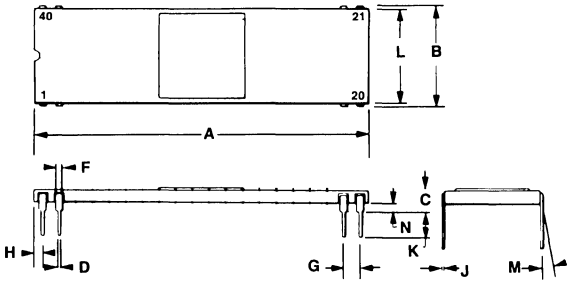
Parameter	Symbol	Min.	Typ.[3]	Max.	Unit[1]	Test Conditions
Input High Voltage Logic ϕ_2	V_{IH}	 +2.0 +2.4	 — —	 V_{CC} V_{CC}	V	
Input Low Voltage Logic ϕ_2	V_{IL}	 −0.3 −0.4	 — —	 +0.8 +0.4	V	
Input Leakage Current R/$\overline{W}$, $\overline{RES}$, RS0, RS1, RS2, RS3, CS1, $\overline{CS2}$, CA1, ϕ2	I_{IN}	—	±1	±2.5	μA	V_{IN} = 0V to V_{CC} V_{CC} = 5.25V
Input Leakage Current for Three-State Off D0–D7	I_{TSI}	—	±2	±10	μA	V_{IN} = 0.4V to 2.4V V_{CC} = 5.25V
Input High Current PA0–PA7, CA2, PB0–PB7, CB1, CB2	I_{IH}	−200	−400	—	μA	V_{IH} = 2.4V
Input Low Current PA0–PA7, CA2, PB0–PB7, CB1, CB2	I_{IL}	—	−2	−2.6	mA	V_{IL} = 0.4V
Output High Voltage All outputs PB0–PB7, CB1 and CB2 (Darlington Drive)	V_{OH}	 2.4 1.5	 — —	 — —	 V V	V_{CC} = 4.75V I_{LOAD} = 200 μA I_{LOAD}[2] = −3.2 mA
Output Low Voltage PA0–PA7, CA2, PB0–PB7, CB1, CB2, D0–D7, $\overline{IRQ}$	V_{OL}	—	—	+0.4	V	V_{CC} = 4.75V I_{LOAD} = 3.2 mA I_{LOAD} = 1.6 mA
Output High Current (Sourcing) Logic PB0–PB7, CB1 and CB2 (Darlington Drive)	I_{OH}	 −200 −3.2	 −1500 −6	 — —	 μA mA	 V_{OH} = 2.4V V_{OH} = 1.5V
Output Low Current (Sinking)	I_{OL}	3.2	—	—	mA	V_{OL} = 0.4V
Output Leakage Current (Off State) $\overline{IRQ}$	I_{OFF}	—	1	±10	μA	V_{OH} = 2.4V V_{CC} = 5.25V
Power Dissipation	P_D	—	7	10	mW/MHz	
Input Capacitance D0–D7, PA0–PA7, CA1, CA2, PB0–PB7, CB1, CB2 R/$\overline{W}$, $\overline{RES}$, RS0, RS1, RS2, RS3, CS1, $\overline{CS2}$, ϕ2	C_{IN}	 — — —	 — — —	 10 7 20	 pF pF pF	V_{CC} = 5.0V V_{IN} = 0V f = 2 MHz T_A = 25°C
Output Capacitance	C_{OUT}	—	—	10	pF	

Notes: .
1. All units are direct current (DC) except for capacitance.
2. Negative sign indicates outward current flow, positive indicates inward flow.
3. Typical values shown for V_{CC} = 5.0V and T_A = 25°C.

1

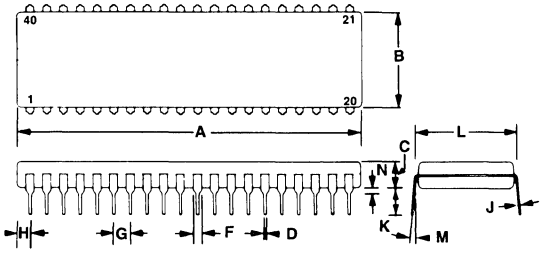
PACKAGE DIMENSIONS

40-PIN CERAMIC DIP



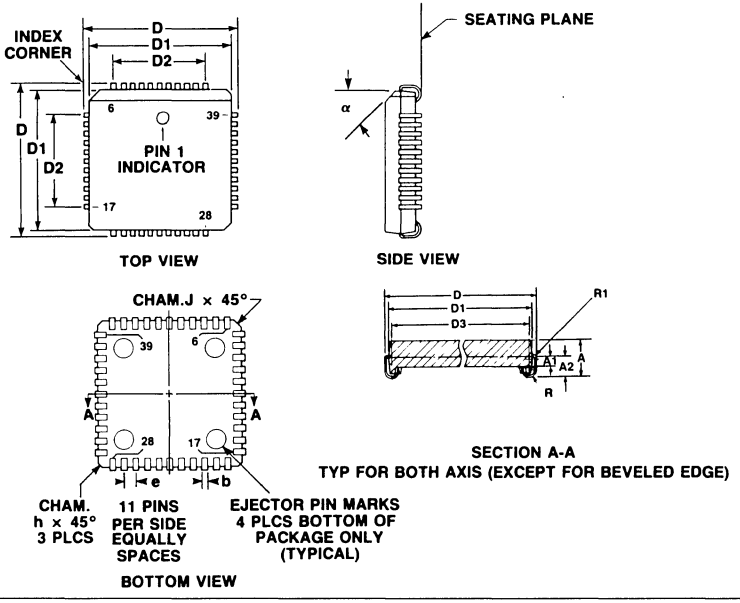
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	50.29	51 31	1 980	2.020
B	15.11	15 88	0.595	0.625
C	2 54	4.19	0.100	0 165
D	0.38	0 53	0 015	0 021
F	0.76	1.27	0.030	0.050
G	2 54 BSC		0.100 BSC	
H	0.76	1 78	0.030	0 070
J	0.20	0.33	0.008	0.013
K	2.54	4.19	0 100	0.165
L	14.60	15.37	0.575	0 605
M	0°	10°	0°	10°
N	0.51	1 52	0.020	0 060

40-PIN PLASTIC DIP



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	51.28	52.32	2.040	2.060
B	13.72	14.22	0.540	0.560
C	3.55	5.08	0.140	0.200
D	0.36	0.51	0.014	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.30	0.008	0.012
K	3.30	4.32	0.130	0.170
L	15.24 BSC		0.600 BSC	
M	7°	10°	7°	10°
N	0.51	1.02	0.020	0.040

44-PIN PLASTIC LEADED CHIP CARRIER (PLCC)



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.14	4.39	0.163	0.173
A1	1.37	1.47	0.054	0.058
A2	2.31	2.46	0.091	0.097
b	0.457 TYP		0.018 TYP	
D	17.45	17.60	0.687	0.693
D1	16.46	16.56	0.648	0.652
D2	12.62	12.78	0.497	0.503
D3	15.75 REF		0.620 REF	
e	1.27 BSC		0.050 BSC	
h	1.15 TYP		0.045 TYP	
J	0.25 TYP		0.010 TYP	
α2	45° TYP		45° TYP	
R	0.89 TYP		0.035 TYP	
R1	0.25 TYP		0.010 TYP	

R65NC22/R65C22 DIFFERENCES

R65C22	R65NC22
1. Register select lines are decoded during $\overline{\phi 2}$.	1. Register select lines are decoded during $\overline{\phi 2}$ only if $\overline{CS2}$ is active low.
2. CB1 must not change during last 100 ns of $\phi 2$. CB1 must have a pulse width greater than one period.	2. CB1 can change anytime but is sampled only during $\overline{\phi 2}$. CB1 must have a pulse greater than one period.
3. PB0–PB7 and CB1, CB2 have active pull-ups.	3. PB0–PB7 and CB1, CB2 have passive pull ups (≈ 3 KΩ).
4. PB0–PB7, CB1 and CB2 represent two standard TTL loads in the input mode and will drive two standard TTL loads in the output mode.	4. PB0–PB7, CB1 and CB2 represent one standard TTL load in the input mode and will drive one standard TTL load in the output mode.

Rockwell

R65NC22
Versatile Interface Adapter (VIA)

1

DESCRIPTION

The R65NC22 Versatile Interface Adapter (VIA) is a very flexible I/O control device. In addition, this device contains a pair of very powerful 16-bit interval timers, a serial-to-parallel/parallel-to serial shift register and input data latching on the peripheral ports. Expanded handshaking capability allows control of bidirectional data transfers between VIA's in multiple processor systems.

The R65NC22 includes functions for programmed control of up to two peripheral devices (Ports A and B). These two program controlled 8-bit bidirectional peripheral I/O ports allow direct interfacing between the microprocessor and selected peripheral units. Each port has input data latching capability. Two programmable Data Direction Registers (A and B) allow selection of data direction (input or output) on an individual line basis.

The R65NC22 also has two programmable 16-bit Interval Timer/Counters with latches. Timer 1 may be operated in a One-Shot Interrupt Mode with interrupts on each count-to-zero, or in a Free-Run Mode with a continuous series of evenly spaced interrupts. Timer 2 functions as both an interval and pulse counter. Serial data transfers are provided by a serial-to-parallel/parallel-to-serial shift register. Application versatility is further increased by various control registers, including—the Interrupt Flag Register, the Interrupt Enable Register, the Auxiliary Control Register and the Peripheral Control Register.

FEATURES

- Low power CMOS N-well silicon gate technology
- Fully compatible with NMOS 6522 devices
- Two 8-bit bidirectional I/O ports
- Two 16-bit programmable timer/counters
- Serial bidirectional peripheral I/O
- TTL compatible peripheral control lines
- Expanded "handshake" capability allows positive control of data transfers between processor and peripheral devices.
- Latched output and input registers on both I/O ports
- 1, 2, 3, and 4 MHz operation
- Commercial and industrial temperature range versions
- Single +5 Vdc power requirement
- Wide variety of packages
  - — 40-pin plastic and ceramic DIP
  - — 44-pin plastic leaded chip carrier (PLCC)

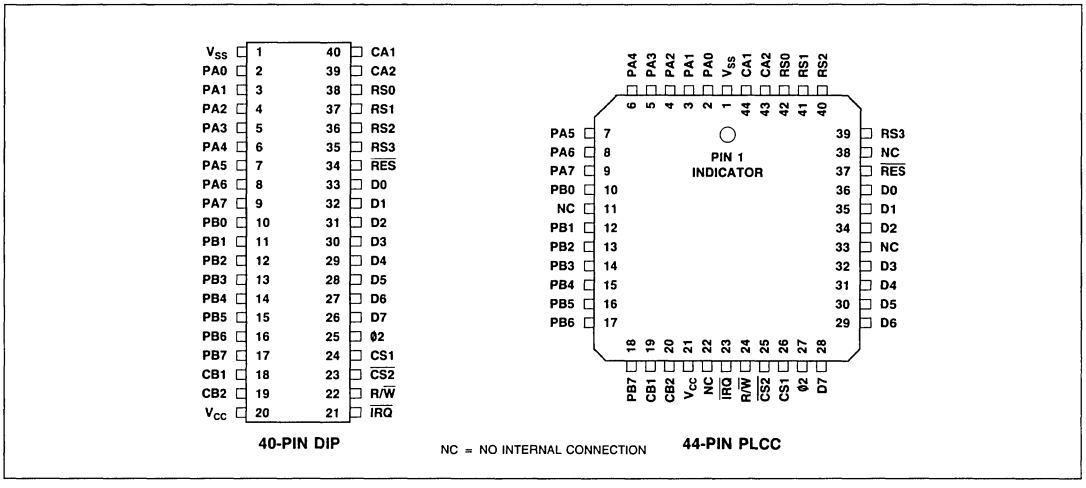


Figure 1. R65NC22 Pin Assignments

ORDERING INFORMATION

Part Number:
R65NC22

- Temperature Range (T_L to T_H):
  - Blank = 0°C to +70°C
  - E = −40°C to +85°C
- Frequency
  - 1 = 1 MHz
  - 2 = 2 MHz
  - 3 = 3 MHz
  - 4 = 4 MHz
- Package
  - C = 40-Pin Ceramic DIP
  - P = 40-Pin Plastic DIP
  - J = 44-Pin Plastic Leaded Chip Carrier (PLCC)

INTERFACE SIGNALS

Figure 1 (on the front page) shows the R65NC22 VIA pin assignments and Figure 2 groups the signals by functional interface.

RESET ($\overline{RES}$)

Reset ($\overline{RES}$) clears all internal registers (except T1 and T2 counters and latches, and the Shift Register (SR)). In the $\overline{RES}$ condition, all peripheral interface lines (PA and PB) are placed in the input state. Also, the Timers (T1 and T2), SR and interrupt logic are disabled from operation.

INPUT CLOCK (PHASE 2)

The system Phase 2 ($\phi 2$) Input Clock controls all data transfers between the R65NC22 and the microprocessor.

READ/WRITE (R/$\overline{W}$)

The direction of the data transfers between the R65NC22 and the system processor is controlled by the R/$\overline{W}$ line in conjunction with the CS1 and $\overline{CS2}$ inputs. When R/$\overline{W}$ is low (write operation) and the R65NC22 is selected, data is transferred from the processor bus into the selected R65NC22 register. When R/$\overline{W}$ is high (read operation) and the R65NC22 is selected, data is transferred from the selected R65NC22 register to the processor bus.

DATA BUS (D0–D7)

The eight bidirectional Data Bus lines transfer data between the R65NC22 and the microprocessor. During a read operation, the contents of the selected R65NC22 internal register are transferred to the microprocessor via the Data Bus lines. During a write operation, the Data Bus lines serve as high impedance inputs over which data is transferred from the microprocessor to a selected R65NC22 register. The Data Bus lines are in the high impedance state when the R65NC22 is unselected.

CHIP SELECTS (CS1, $\overline{CS2}$)

Normally, the two chip select lines are connected to the microprocessor address lines. This connection may be direct or through decoding. To access a selected R65NC22 register, CS1 must be high (logic 1) and $\overline{CS2}$ must be low (logic 0).

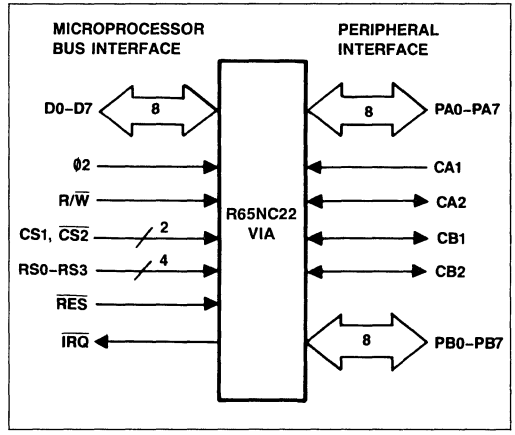


Figure 2. R65NC22 VIA Interface Signals

REGISTER SELECTS (RS0–RS3)

The Register Select inputs allow the microprocessor to select one of 16 internal registers within the R65NC22. Refer to Table 1 for Register Select coding and a functional description. The RS lines are decoded only if $\overline{CS2}$ is low.

INTERRUPT REQUEST ($\overline{IRQ}$)

The Interrupt Request ($\overline{IRQ}$) output signal is generated whenever an internal Interrupt Flag bit is set and the corresponding Interrupt Enable bit is a Logic 1. The Interrupt Request output is an open-drain configuration, thus allowing the $\overline{IRQ}$ signal to be wire-ORed to a common microprocessor $\overline{IRQ}$ input line.

PORT A DATA LINES (PA0–PA7)

Peripheral Data Port A is an 8-line, bidirectional bus for the transfer of data, control and status information between the R65NC22 and a peripheral device. Each Peripheral Data Port bus line may be individually programmed as either an input or output under control of a Data Direction Register. Data flow direction may be selected on a line-by-line basis with intermixed input and output lines within the same port. When a "0" is written to any bit position of the Data Direction Register, the corresponding line will be programmed as an input. When a "1" is written into any bit position of the register, the corresponding data line will serve as an output. Polarity of the data output is determined by the Output Register, while input data may be latched into the Input Register under control of the CA1 line. All modes are program controlled by the microprocessor by way of the R65NC22's internal control registers. Each Peripheral Data Port line represents two TTL loads in the input mode and will drive two standard TTL loads in the output mode. A typical output circuit for Peripheral Data Port A is shown in Figure 3.

PORT A CONTROL LINES (CA1, CA2)

Control lines CA1 and CA2 serve as interrupt inputs or handshake outputs for Peripheral Data Port A. Each line controls an internal Interrupt Flag with a corresponding Interrupt Enable bit. CA1 also controls the latching of Input Data on Port A. CA1 is a high impedance input, while CA2 represents two standard TTL loads in the input mode. In the output mode, CA2 will drive two standard TTL loads.

PORT B DATA LINES (PB0–PB7)

Peripheral Data Port B is an 8-line, bidirectional bus which is controlled by an Output Register, Input Register and Data Direction Register in a manner much the same as Data Port A. With respect to Port B, the output signal on line PB7 may be controlled by Timer 1 while Timer 2 may be programmed to count pulses on the PB6 line. Port B lines represent one standard TTL load in the input mode and will drive one TTL load in the output mode. Port B lines are also capable of sourcing 3.2 mA at 1.5 Vdc in the output mode. This allows the outputs to directly drive Darlington transistor circuits. A typical output circuit for Port B is shown in Figure 3.

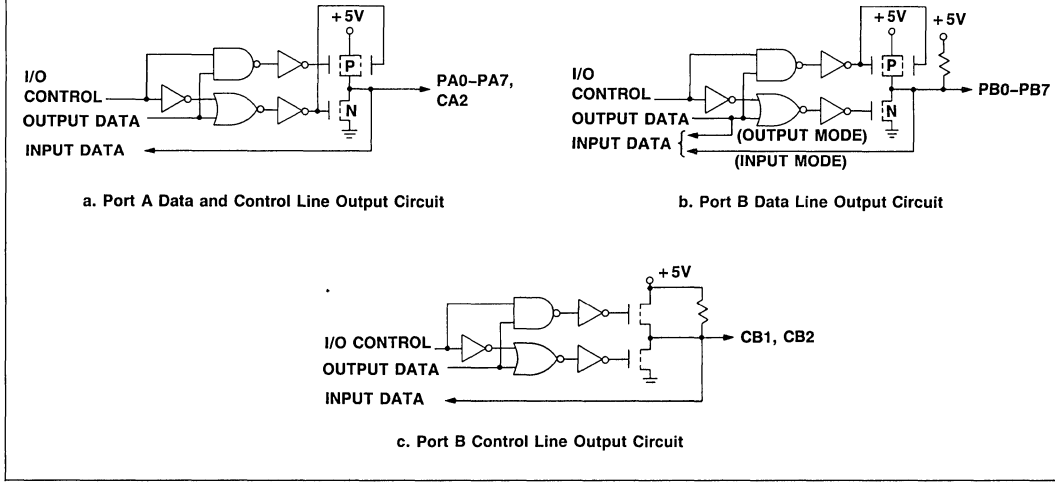
PORT B CONTROL LINES (CB1, CB2)

Control lines CB1 and CB2 serve as interrupt inputs or handshake outputs for Peripheral Data Port B. Like Port A, these two control lines control an internal Interrupt Flag with a corresponding Interrupt Enable bit. Similar to CA1, CB1 controls the latching of input data on Port B. These lines also serve as a serial data port under control of the Shift Register (SR). Each control line represents one standard TTL load in the input mode and can drive one TTL load in the output mode.

Table 1. R65NC22 Register Addressing

Register Number	RS Coding				Register Desig.	Register/Description	
	RS3	RS2	RS1	RS0		Write (R/$\overline{W}$ = L)	Read (R/$\overline{W}$ = H)
0	0	0	0	0	ORB/IRB	Output Register B	Input Register B
1	0	0	0	1	ORA/IRA	Output Register A	Input Register A
2	0	0	1	0	DDRB	Data Direction Register B	
3	0	0	1	1	DDRA	Data Direction Register A	
4	0	1	0	0	T1C-L	T1 Low-Order Latches	T1 Low-Order Counter
5	0	1	0	1	T1C-H	T1 High-Order Counter	
6	0	1	1	0	T1L-L	T1 Low-Order Latches	
7	0	1	1	1	T1L-H	T1 High-Order Latches	
8	1	0	0	0	T2C-L	T2 Low-Order Latches	T2 Low-Order Counter
9	1	0	0	1	T2C-H	T2 High-Order Counter	
10	1	0	1	0	SR	Shift Register	
11	1	0	1	1	ACR	Auxiliary Control Register	
12	1	1	0	0	PCR	Peripheral Control Register	
13	1	1	0	1	IFR	Interrupt Flag Register	
14	1	1	1	0	IER	Interrupt Enable Register	
15	1	1	1	1	ORA/IRA	Output Register A*	Input Register A*

NOTE: *Same as Register 1 except no handshake.



a. Port A Data and Control Line Output Circuit

b. Port B Data Line Output Circuit

c. Port B Control Line Output Circuit

Figure 3. Port A and B Output Circuits

FUNCTIONAL DESCRIPTION

The internal organization of the R65NC22 VIA is illustrated in Figure 4.

PORT A AND PORT B OPERATION

The R65NC22 VIA has two 8-bit bidirectional I/O ports (Port A and Port B) and each port has two associated control lines.

Each 8-bit peripheral port has a Data Direction Register (DDRA, DDRB) for specifying whether the peripheral pins are to act as inputs or outputs. A "0" in a bit of the Data Direction Register causes the corresponding peripheral pin to act as an input. A "1" causes the pin to act as an output.

Each peripheral pin is also controlled by a bit in the Output Register (ORA, ORB) and the Input Register (IRA, IRB). When the pin is programmed as an output, the voltage on the pin is controlled by the corresponding bit of the Output Register. A "1" in the Output Register causes the output to go high, and a "0" causes the output to go low. Data may be written into Output Register bits corresponding to pins which are programmed as inputs. In this case, however, the output signal is unaffected.

Reading a peripheral port causes the contents of the Input Register (IRA, IRB) to be transferred onto the Data Bus. With input latching disabled, IRA will always reflect the levels on the PA pins. With input latching enabled, IRA will reflect the levels on the PA pins at the time the latching occurred (via CA1).

The IRB register operates similar to the IRA register. However, for pins programmed as outputs there is a difference. When reading IRA, the *level on the pin* determines whether a "0" or a "1" is sensed. When reading IRB, however, the bit stored in the *output register,* ORB, is the bit sensed. Thus, for outputs which have large loading effects and which pull an output "1" down or which pull an output "0" up, reading IRA may result in reading a "0" when a "1" was actually programmed, and reading a "1" when a "0" was programmed. Reading IRB, on the other hand, will read the "1" or "0" level actually programmed, no matter what the loading on the pin.

Figures 5 through 8 illustrate the formats of the port registers.

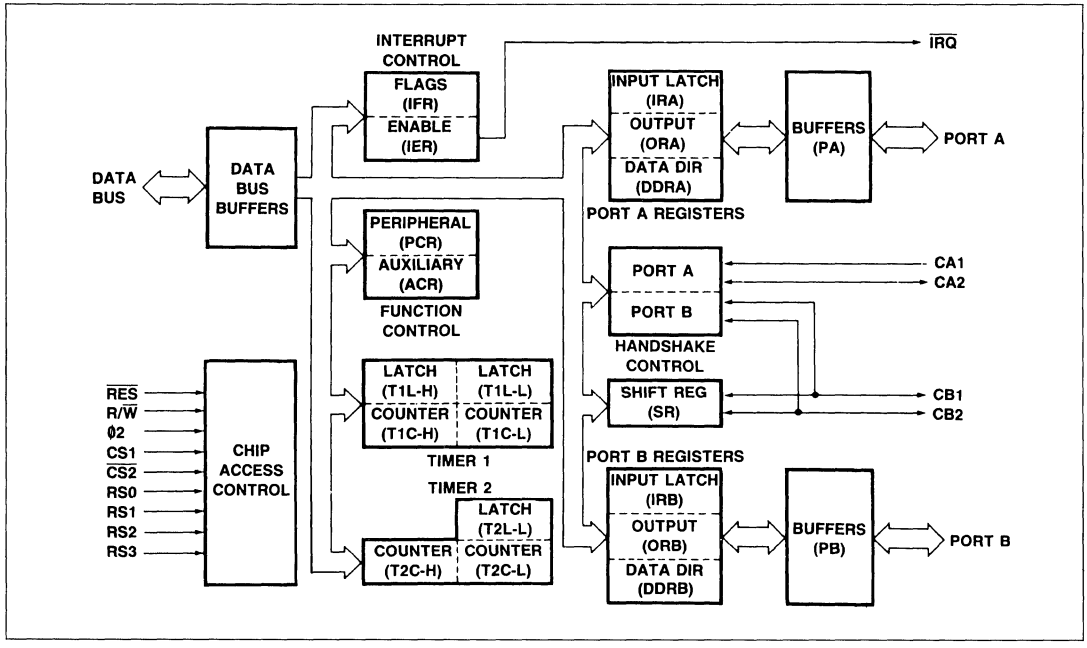


Figure 4. R65NC22 VIA Block Diagram

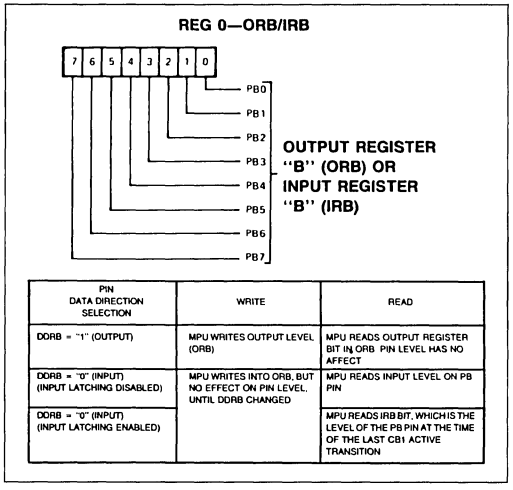
HANDSHAKE CONTROL OF DATA TRANSFERS

The R65NC22 allows positive control of data transfers between the system processor and peripheral devices through the operation of "handshake" lines. Port A lines (CA1, CA2) handshake data on both a read and a write operation while the Port B lines (CB1, CB2) handshake on a write operation only.

Read Handshake

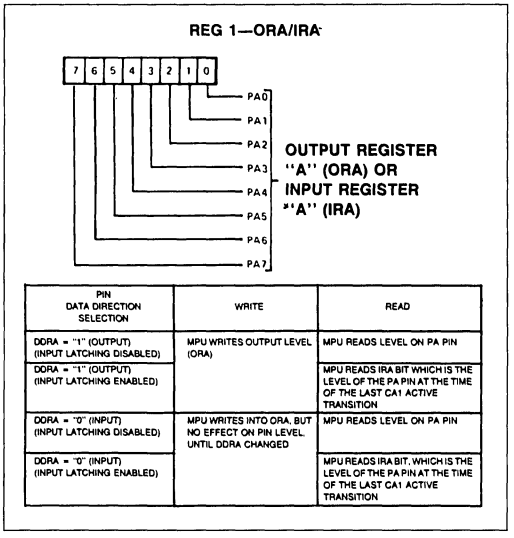
Positive control of data transfers from peripheral devices into the system processor can be accomplished very effectively using Read Handshaking. In this case, the peripheral device must generate the equivalent of a "Data Ready" signal to the processor signifying that valid data is present on the peripheral port. This signal normally interrupts the processor, which then reads the data, causing generation of a "Data Taken" signal. The peripheral device responds by making new data available. This process continues until the data transfer is complete.

In the R65NC22, automatic "Read" Handshaking is possible on the Peripheral A port only. The CA1 interrupt input pin accepts the "Data Ready" signal and CA2 generates the "Data Taken" signal. The "Data Ready" signal will set an internal flag which may interrupt the processor or which may be polled under program control. The "Data Taken" signal can either be a pulse or a level which is set low by the system processor and is cleared by the "Data Ready" signal. These options are shown in Figure 9 which illustrates the normal Read Handshake sequence.



PIN DATA DIRECTION SELECTION	WRITE	READ
DDRB = "1" (OUTPUT)	MPU WRITES OUTPUT LEVEL (ORB)	MPU READS OUTPUT REGISTER BIT IN ORB PIN LEVEL HAS NO AFFECT
DDRB = "0" (INPUT) (INPUT LATCHING DISABLED)	MPU WRITES INTO ORB, BUT NO EFFECT ON PIN LEVEL, UNTIL DDRB CHANGED	MPU READS INPUT LEVEL ON PB PIN
DDRB = "0" (INPUT) (INPUT LATCHING ENABLED)		MPU READS IRB BIT, WHICH IS THE LEVEL OF THE PB PIN AT THE TIME OF THE LAST CB1 ACTIVE TRANSITION

Figure 5. Output Register B (ORB), Input Register B (IRB)



PIN DATA DIRECTION SELECTION	WRITE	READ
DDRA = "1" (OUTPUT) (INPUT LATCHING DISABLED)	MPU WRITES OUTPUT LEVEL (ORA)	MPU READS LEVEL ON PA PIN
DDRA = "1" (OUTPUT) (INPUT LATCHING ENABLED)		MPU READS IRA BIT WHICH IS THE LEVEL OF THE PA PIN AT THE TIME OF THE LAST CA1 ACTIVE TRANSITION
DDRA = "0" (INPUT) (INPUT LATCHING DISABLED)	MPU WRITES INTO ORA, BUT NO EFFECT ON PIN LEVEL UNTIL DDRA CHANGED	MPU READS LEVEL ON PA PIN
DDRA = "0" (INPUT) (INPUT LATCHING ENABLED)		MPU READS IRA BIT, WHICH IS THE LEVEL OF THE PA PIN AT THE TIME OF THE LAST CA1 ACTIVE TRANSITION

Figure 6. Output Register A (ORA), Input Register A (IRA)

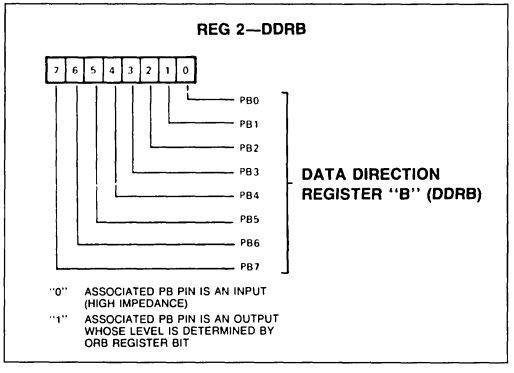


Figure 7. Data Direction Register B (DDRB)

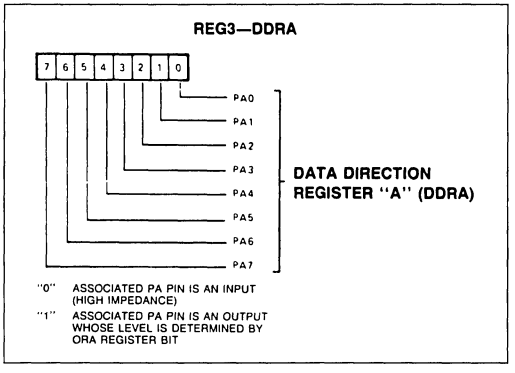


Figure 8. Data Direction Register A (DDRA)

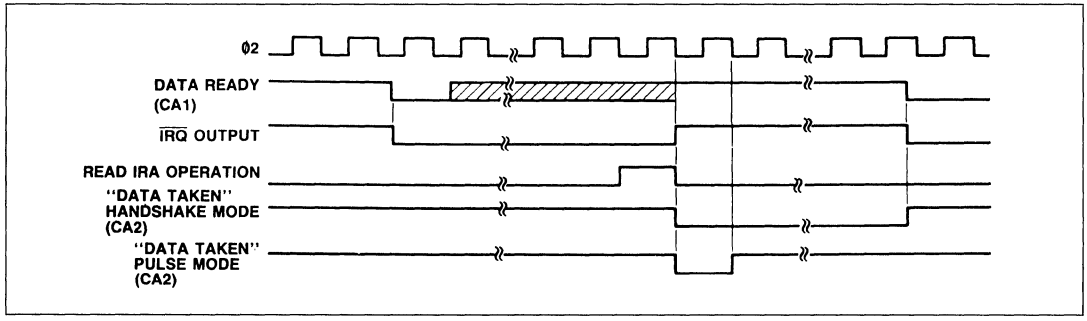


Figure 9. Read Handshake Timing (Port A Only)

Write Handshake

The sequence of operations which allows handshaking data from the system processor to a peripheral device is very similar to that described for Read Handshaking. However, for Write Handshaking, the R65NC22 generates the "Data Ready" signal and the peripheral device must respond with the "Data Taken" signal. This can be accomplished on both the PA port and the PB port on the R65NC22. CA2 or CB2 act as a "Data Ready" output in either the handshake mode or pulse mode and CA1 or CB1 accept the "Data Taken" signal from the peripheral device, setting the interrupt flag and clearing the "Data Ready" output. This sequence is shown in Figure 10.

Latching

The PA port and the PB port on the R65NC22 can be enabled in the Auxiliary Control Register (Figure 14) to be latched by their individual port control lines (CA1, CB1). Latching is selectable to be on the rising or falling edge of the signal at each individual port control line. Selection of operating modes for CA1, CA2, CB1 and CB2 is accomplished by the Peripheral Control Register (Figure 11).

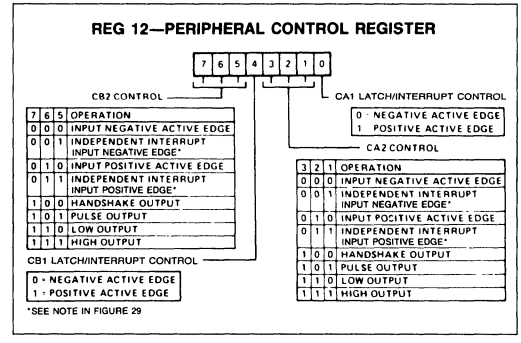


Figure 11. Peripheral Control Register (PCR)

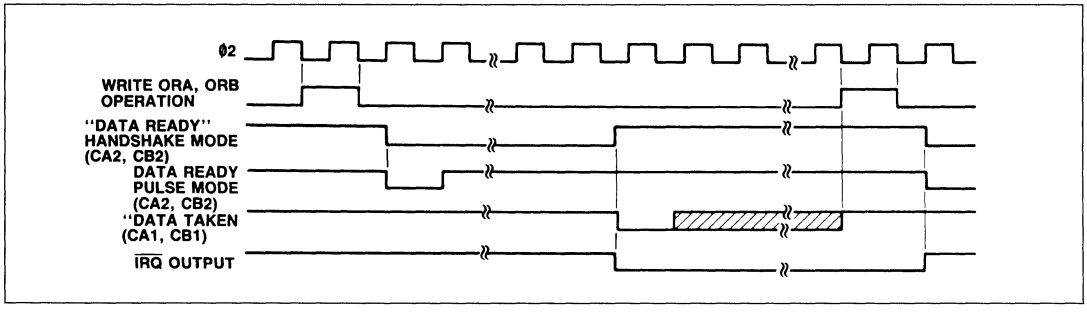


Figure 10. Write Handshake Timing

COUNTER/TIMERS

There are two independent 16-bit counter/timers (called Timer 1 and Timer 2) in the R65NC22. Each timer is controlled by writing bits into the Auxiliary Control Register (ACR) to select the mode of operation (Figure 14).

Timer 1 Operation

Interval Timer T1 consists of two 8-bit latches (Figure 12) and a 16-bit counter (Figure 13). The latches store data which is to be loaded into the counter. After loading, the counter decrements at ϕ2 clock rate. Upon reaching zero, an interrupt flag is set, and IRQ goes low if the T1 interrupt is enabled. Timer 1 then disables any further interrupts and automatically transfers the contents of the latches into the counter and continues to decrement. In addition, the timer may be programmed to invert the output signal on peripheral pin PB7 each time it "times-out". Each of these modes is discussed separately below.

Note that the processor does not write directly into the low-order counter (T1C-L). Instead, this half of the counter is loaded automatically from the low order latch (T1L-L) when the processor writes into the high order counter (T1C-H). In fact, it may not be necessary to write to the low order counter in some applications since the timing operation is triggered by writing to the high order latch.

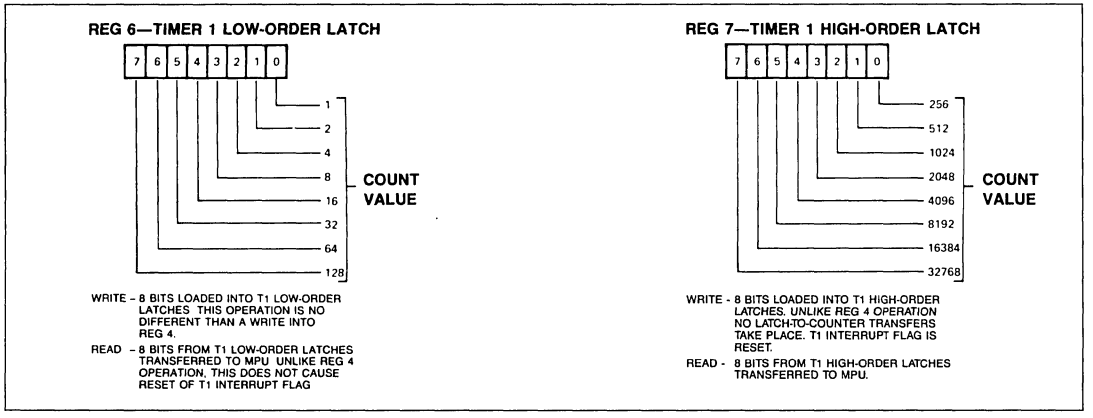


Figure 12. Timer 1 (T1) Latch Registers

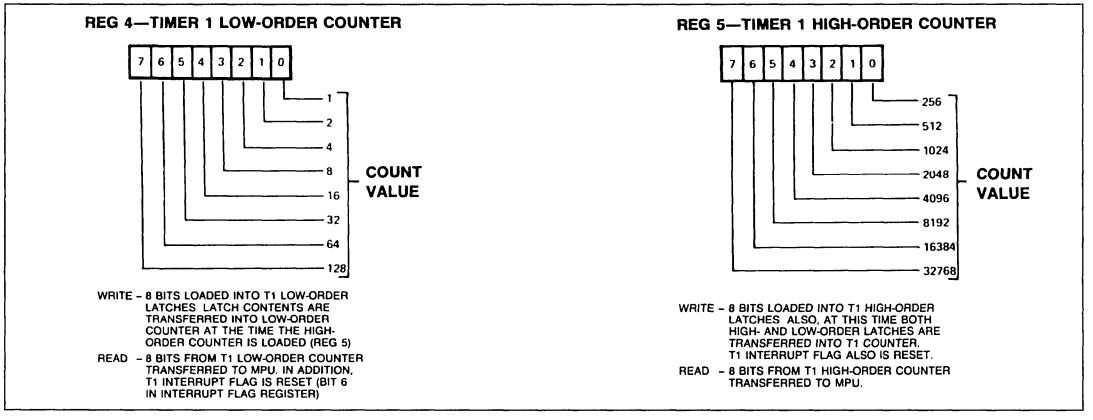


Figure 13. Timer 1 (T1) Counter Registers

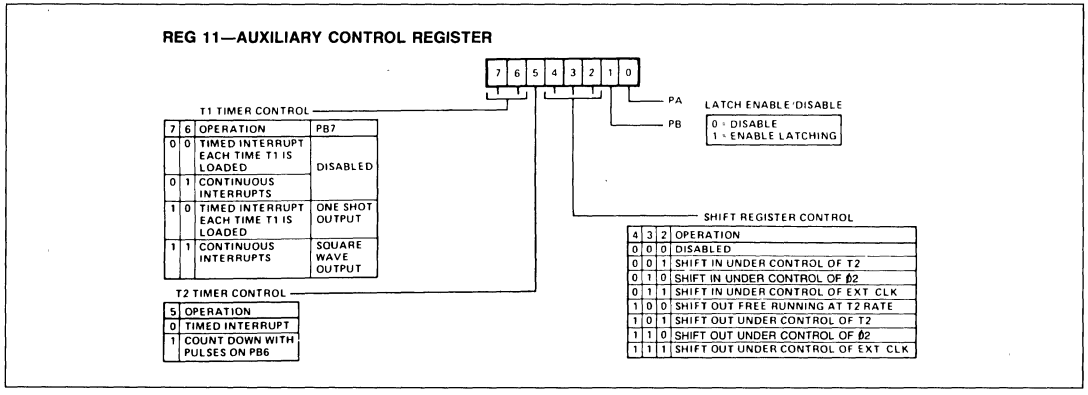


Figure 14. Auxiliary Control Register (ACR)

Timer 1 One-Shot Mode

The Timer 1 one-shot mode generates a single interrupt for each timer load operation. As with any interval timer, the delay between the "write T1C-H" operation and generation of the processor interrupt is a direct function of the data loaded into the timing counter. In addition to generating a single interrupt, Timer 1 can be programmed to produce a single negative pulse on the PB7 peripheral pin. With the output enabled (ACR7 = 1) a "write T1C-H" operation will cause PB7 to go low. PB7 will return high when Timer 1 times out. The result is a single programmable width pulse.

Timing for the R65NC22 interval timer one-shot modes is shown in Figure 15.

In the one-shot mode, writing into the T1L-H has no effect on the operation of Timer 1. However, it will be necessary to assure that the low order latch contains the proper data before initiating the count-down with a "write T1C-H" operation. When the processor writes into the high order counter (T1C-H), the T1 interrupt flag will be cleared, the contents of the low order latch will be transferred into the low order counter, and the timer will begin to decrement at system clock rate. If the PB7 output is enabled, this signal will go low on the falling edge of Ø2 following the write operation. When the counter reaches zero, the T1 interrupt flag will be set, the $\overline{IRQ}$ pin will go low (interrupt enabled), and the signal on PB7 will go high. At this time the counter will continue to decrement at system clock rate. This allows the system processor to read the contents of the counter to determine the time since interrupt. However, the T1 interrupt flag cannot be set again unless it has been cleared as described in this specification.

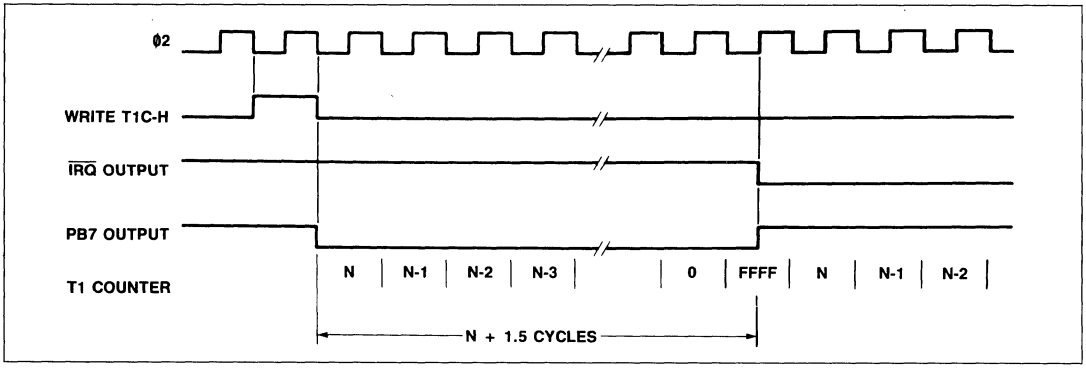


Figure 15. Timer 1 One-Shot Mode Timing

Timer 1 Free-Run Mode

The most important advantage associated with the latches in T1 is the ability to produce a continuous series of evenly spaced interrupts and the ability to produce a square wave on PB7 whose frequency is not affected by variations in the processor interrupt response time. This is accomplished in the "free-running" mode.

In the free-running mode, the interrupt flag is set and the signal on PB7 is inverted each time the counter reaches zero at which time the timer automatically transfers the contents of the latch into the counter (16 bits) and continues to decrement from there. The interrupt flag can be cleared by writing T1C-H or T1L-H, by reading T1C-L, or by writing directly into the flag as described later. However, it is not necessary to rewrite the timer to enable setting the interrupt flag on the next time-out.

All interval timers in the R65NC22 are "re-triggerable". Rewriting the counter will always re-initialize the time-out period. In fact, the time-out can be prevented completely if the processor continues to rewrite the timer before it reaches zero. Timer 1 will operate in this manner if the processor writes into the high order counter (T1C-H). However, by loading the latches only, the processor can access the timer during each down-counting operation without affecting the time-out in process. Instead, the data loaded into the latches will determine the length of the next time-out period. This capability is particularly valuable in the free-running mode with the output enabled. In this mode, the signal on PB7 is inverted and the interrupt flag is set with each time-out. By responding to the interrupts with new data for the latches, the processor can determine the period of the next half cycle during each half cycle of the output signal on PB7. In this manner, very complex waveforms can be generated.

A precaution to take in the use of PB7 as the timer output concerns the Data Direction Register contents for PB7. *Both* DDRB bit 7 and ACR bit 7 must be 1 for PB7 to function as the timer output. If one is 1 and other is 0, then PB7 functions as a normal outpin pin, controlled by ORB bit 7.

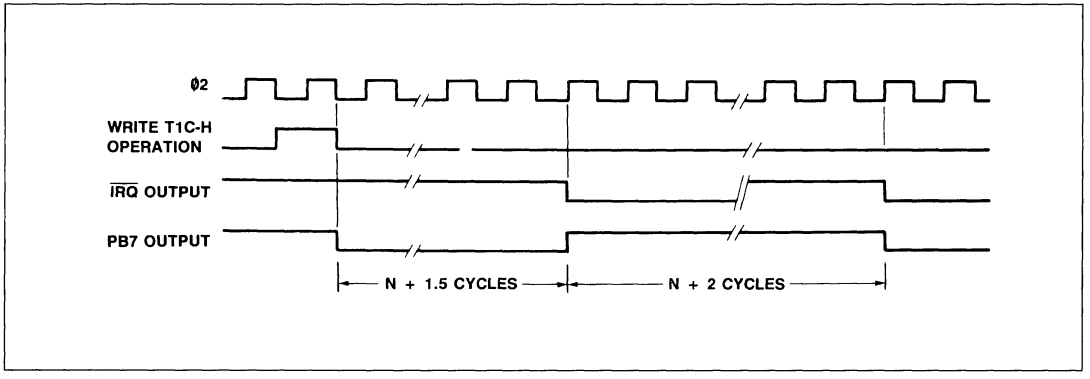


Figure 16. Timer 1 Free-Run Mode Timing

Timer 2 Operation

Timer 2 operates as an interval timer (in the "one-shot" mode only), or as a counter for counting negative pulses on the PB6 peripheral pin. A single control bit in the Auxiliary Control Register selects between these two modes. This timer is comprised of a "write-only" lower-order latch (T2L-L), a "read-only" low-order counter (T2C-L) and a read/write high order counter (T2C-H). The counter registers act as a 16-bit counter which decrements at Ø2 rate. Figure 17 illustrates the T2 Latch/Counter Registers.

Timer 2 One-Shot Mode

As an interval timer, T2 operates in the "one-shot" mode similar to Timer 1. In this mode, T2 provides a single interrupt for each "write T2C-H" operation. After timing out, the counter will continue to decrement. However, setting of the interrupt flag is disabled after initial time-out so that it will not be set by the counter decrementing again through zero. The processor must rewrite T2C-H to enable setting of the interrupt flag. The interrupt flag is cleared by reading T2C-L or by writing T2C-H. Timing for this operation is shown in Figure 18.

Timer 2 Pulse Counting Mode

In the pulse counting mode, T2 counts a predetermined number of negative-going pulses on PB6. This is accomplished by first loading a number into T2. Writing into T2C-H clears the interrupt flag and allows the counter to decrement each time a pulse is applied to PB6. The interrupt flag is set when T2 counts down past zero. The counter will then continue to decrement with each pulse on PB6. However, it is necessary to rewrite T2C-H to allow the interrupt flag to set on a subsequent time-out. Timing for this mode is shown in Figure 19. The pulse must be low on the leading edge of Ø2.

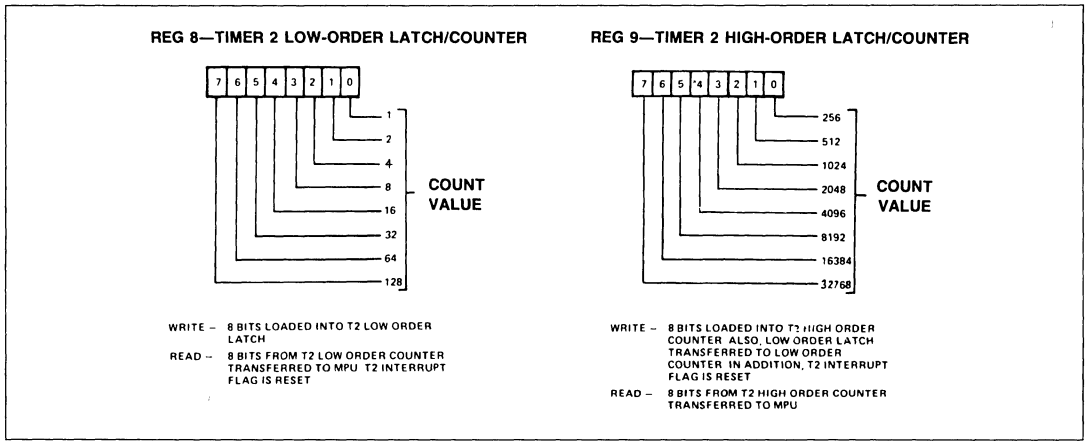


Figure 17. Timer 2 (T2) Latch/Counter Registers

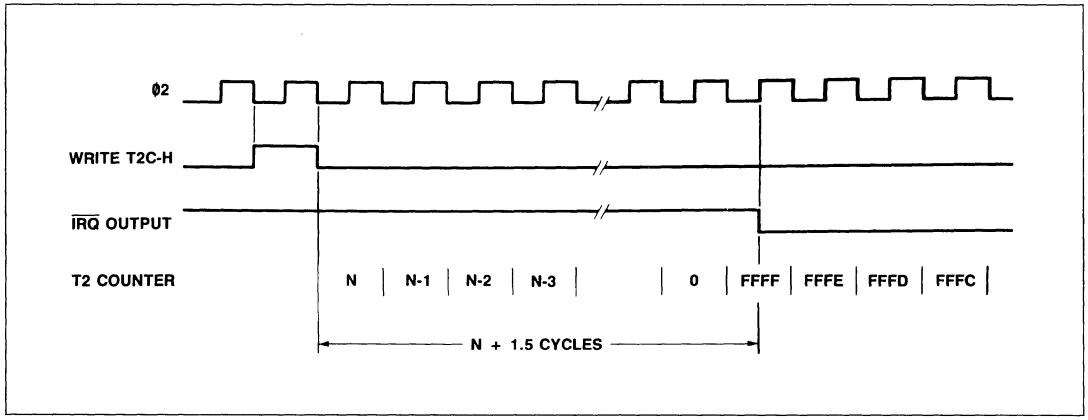


Figure 18. Timer 2 One-Shot Mode Timing

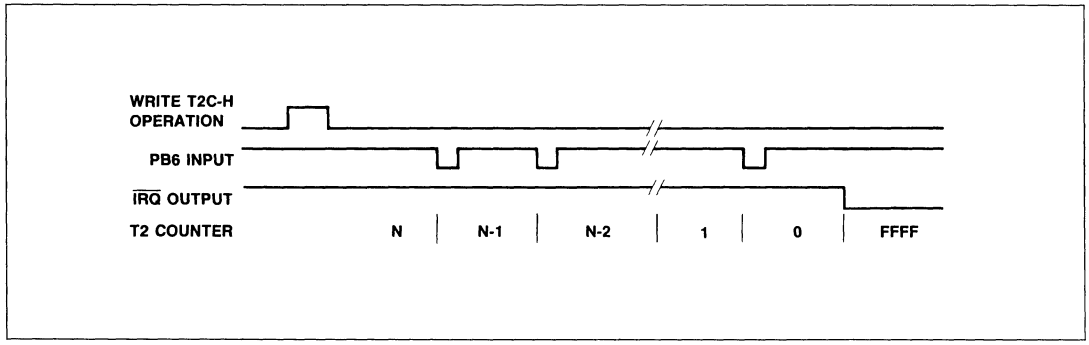


Figure 19. Timer 2 Pulse Counting Mode

SHIFT REGISTER OPERATION

The Shift Register (SR) performs serial data transfers into and out of the CB2 pin under control of an internal modulo-8 counter. Serial data transfer in and out of the Shift Register (SR) begin with the most significant bit (MSB) first. Shift pulses can be applied to the CB1 pin from an external source or, with the proper mode selection, shift pulses generated internally will appear on the CB1 pin for controlling external devices.

The control bits which select the various shift register operating modes are located in the Auxiliary Control Register. Figure 20 illustrates the configuration of the SR data bits and Figure 21 shows the SR control bits of the ACR.

SR Mode 0 — Shift Register Interrupt Disabled

Mode 0 disables the Shift Register interrupt. In this mode the microprocessor can write or read the SR and the SR will shift on each CB1 positive edge shifting in the value on CB2. In this mode the SR interrupt Flag is disabled (held to a logic 0).

SR Mode 1 — Shift In Under Control of T2

In mode 1, the shifting rate is controlled by the low order 8 bits of T2 (Figure 22). Shift pulses are generated on the CB1 pin to control shifting in external devices. The time between transitions of this output clock is a function of the system clock period and the contents of the low order T2 latch (N).

The shifting operation is triggered by the read or write of the SR if the SR flag is set in the IFR. Otherwise the first shift will occur at the next time-out of T2 after a read or write of the SR. The input data should change before the positive-going edge of CB1 clock pulse. This data is shifted into the shift register during the Ø2 clock cycle following the positive-going edge of the CB1 clock pulse. The minimum CB1 positive pulse width must be one clock period. After 8 CB1 clock pulses, the shift register interrupt flag will set and $\overline{IRQ}$ will go low.

SR Mode 2 — Shift In Under Ø2 Control

In mode 2, the shift rate is a direct function of the system clock frequency (Figure 23). CB1 becomes an output which generates shift pulses for controlling external devices. Timer 2 operates as an independent interval timer and has no effect on SR. The shifting operation is triggered by reading or writing the Shift Register. Data is shifted, first into bit 0 and is then shifted into the next higher order bit of the shift register on the trailing edge of each Ø2 clock pulse. After 8 clock pulses, the shift register interrupt flag will be set, and the output clock pulses on CB1 will stop.

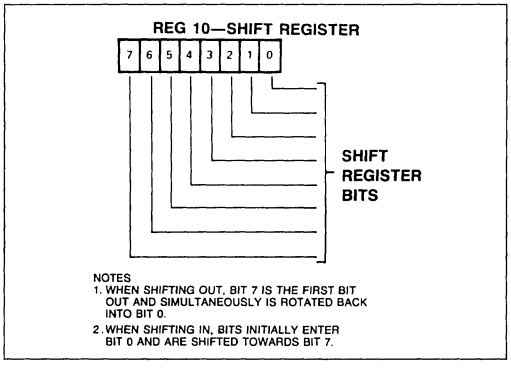


Figure 20. Shift Register

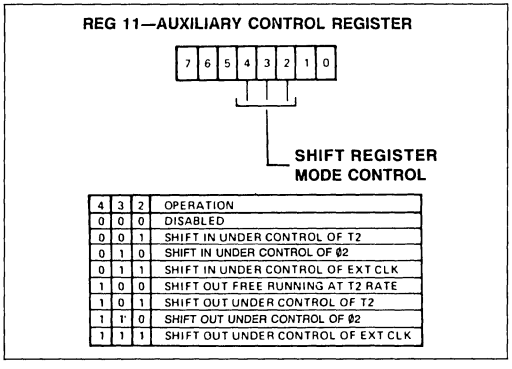


Figure 21. Shift Register Modes

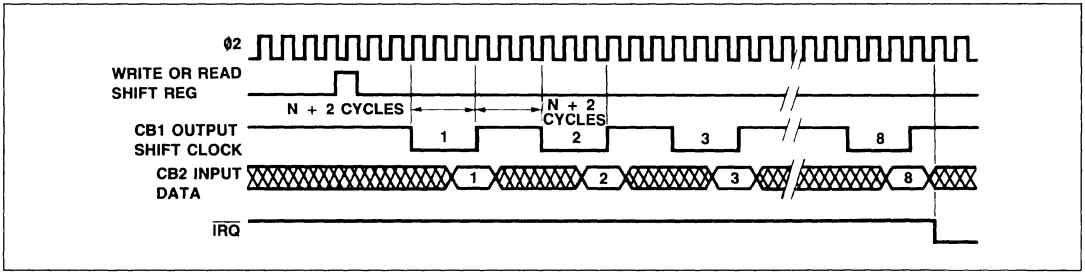


Figure 22. SR Mode 1 — Shift In Under T2 Control

SR Mode 3 — Shift In Under CB1 Control

In mode 3, external pin CB1 becomes an input (Figure 24). This allows an external device to load the shift register at its own pace. The shift register counter will interrupt the processor each time 8 bits have been shifted in. The shift register stops after 8 counts and must be reset to start again. Reading or writing the Shift Register resets the Interrupt Flag and initializes the SR counter to count another 8 pulses.

Note that the data is shifted during the first system clock cycle following the positive-going edge of the CB1 shift pulse. For this reason, data must be held stable during the first full cycle following CB1 going high. The minimum CB1 positive pulse width must be one clock period.

SR Mode 4 — Shift Out Under T2 Control (Free-Run)

Mode 4 is very similar to mode 1 in which the shifting rate is set by T2. However, in mode 4 the SR Counter does not stop the shifting operation (Figure 25). Since the Shift Register bit 7 (SR7) is recirculated back into bit 0, the 8 bits loaded into the shift register will be clocked onto CB2 repetitively. In this mode the shift register counter is disabled.

SR Mode 5 — Shift Out Under T2 Control

In mode 5, the shift rate is controlled by T2 (as in mode 1). The shifting operation is triggered by the read or write of the SR if the SR flag is set in the IFR (Figure 26). Otherwise the first shift will occur at the next time-out of T2 after a read or write of the SR. However, with each read or write of the shift register the SR Counter is reset and 8 bits are shifted onto CB2. At the same time, 8 shift pulses are generated on CB1 to control shifting in external devices. After the 8 shift pulses, the shifting is disabled, the SR Interrupt Flag is set and CB2 remains at the last data level.

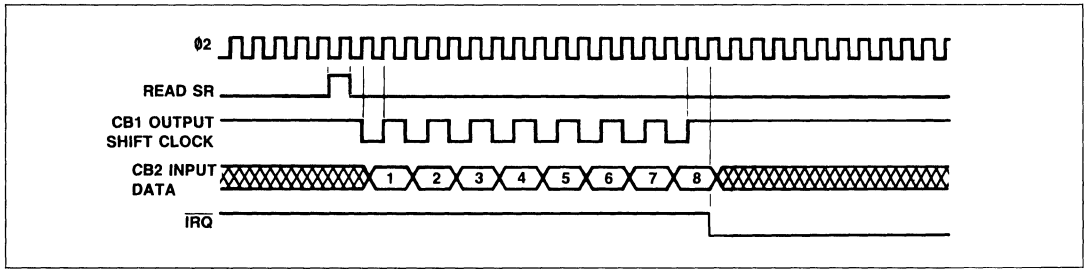


Figure 23. SR Mode 2 — Shift In Under Ø2 Control

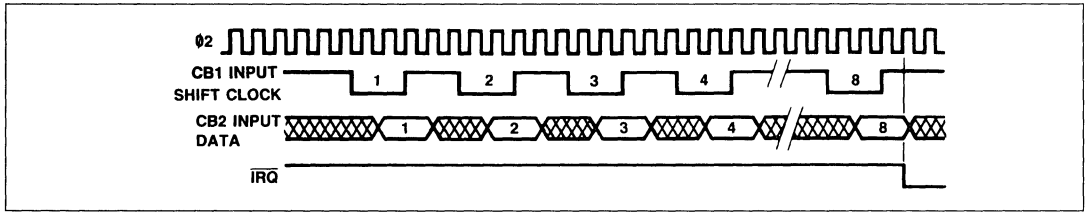


Figure 24. SR Mode 3 — Shift In Under CB1 Control

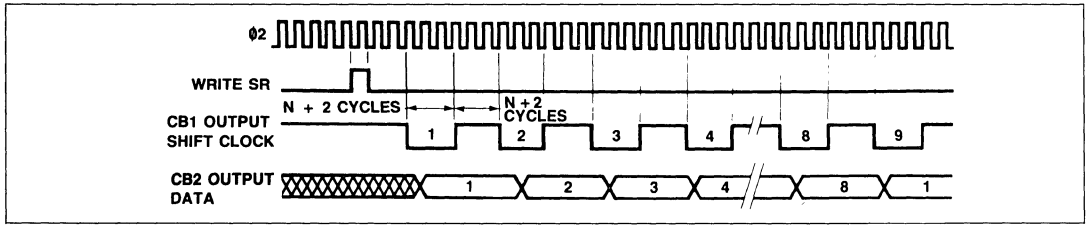


Figure 25. SR Mode 4 — Shift Out Under T2 Control (Free-Run)

SR Mode 6 — Shift Out Under ϕ2 Control

In mode 6, the shift rate is controlled by the ϕ2 system clock (Figure 27).

SR Mode 7 — Shift Out Under CB1 Control

In mode 7, shifting is controlled by pulses applied to the CB1 pin by an external device (Figure 28). The SR counter sets the SR Interrupt Flag each time it counts 8 pulses but it does not disable the shifting function. Each time the microprocessor, writes or reads the shift register, the SR Interrupt Flag is reset and the SR counter is initialized to begin counting the next 8 shift pulses on pin CB1. After 8 shift pulses, the Interrupt Flag is set. The microprocessor can then load the shift register with the next byte of data.

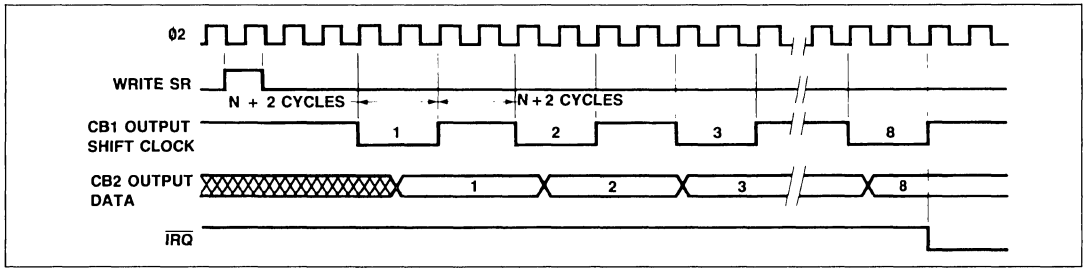


Figure 26. SR Mode 5 — Shift Out Under T2 Control

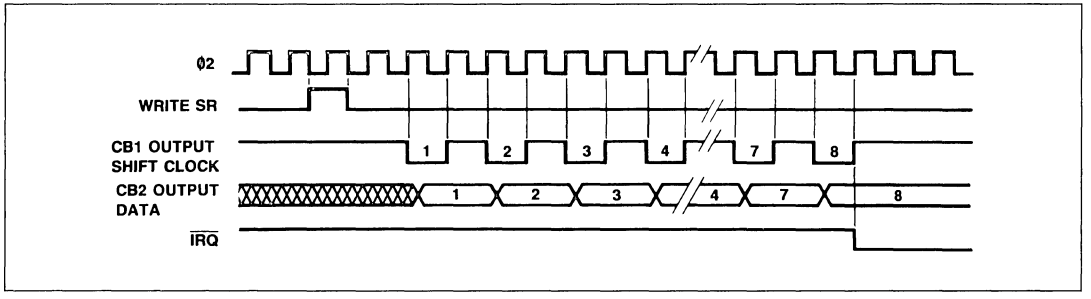


Figure 27. SR Mode 6 — Shift Out Under ϕ2 Control

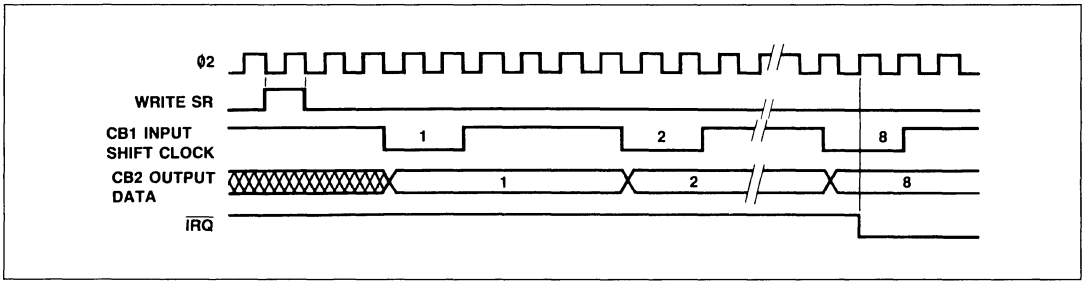


Figure 28. SR Mode 7 — Shift Out Under CB1 Control

INTERRUPT OPERATION

Controlling interrupts within the R65NC22 involves three principal operations. These are flagging the interrupts, enabling interrupts and signaling to the processor that an active interrupts exists within the chip. Interrupt flags are set in the Interrupt Flag Register (IFR) by conditions detected within the R65NC22 or on inputs to the R65NC22. These flags normally remain set until the interrupt has been serviced. To determine the source of an interrupt, the microprocessor must examine these flags in order, from highest to lowest priority.

Associated with each interrupt flag is an interrupt enable bit in the Interrupt Enable Register (IER). This can be set or cleared by the processor to enable interrupting the processor from the corresponding interrupt flag. If an interrupt flag is set to a logic 1 by an interrupting condition, and the corresponding interrupt enable bit is set to a 1, the Interrupt Request Output ($\overline{IRQ}$) will go low. $\overline{IRQ}$ is an "open-collector" output which can be "wire-OR'ed" with other devices in the system to interrupt the processor.

Interrupt Flag Register (IFR)

In the R65NC22, all the interrupt flags are contained in one register, i.e., the IFR (Figure 29). In addition, bit 7 of this register will be read as a logic 1 when an interrupt exists within the chip. This allows very convenient polling of several devices within a system to locate the source of an interrupt.

The Interrupt Flag Register (IFR) may be read directly by the processor. In addition, individual flag bits may be cleared by writing a "1" into the appropriate bit of the IFR. When the proper chip select and register signals are applied to the chip, the contents of this register are placed on the data bus. Bit 7 indicates the status of the $\overline{IRQ}$ output. This bit corresponds to the logic function: $\overline{IRQ}$ = IFR6 × IER6 + IFR5 × IER5 + IFR4 × IER4 + IFR3 × IER3 + IFR2 × IER2 + IFR1 × IER1 + IFR0 × IER0.

Note:

× = logic AND, + = Logic OR.

The IFR bit 7 is not a flag. Therefore, this bit is not directly cleared by writing a logic 1 into it. It can only be cleared by clearing all the flags in the register or by disabling all the active interrupts as discussed in the next section.

Interrupt Enable Register (IER)

For each interrupt flag in IFR, there is a corresponding bit in the Interrupt Enable Register (IER) (Figure 30). Individual bits in the IER can be set or cleared to facilitate controlling individual interrupts without affecting others. This is accomplished by writing to the (IER) after bit 7 set or cleared to, in turn, set or clear selected enable bits. If bit 7 of the data placed on the system data bus during this write operation is a 0, each 1 in bits 6 through 0 clears the corresponding bit in the Interrupt Enable Register. For each zero in bits 6 through 0, the corresponding bit is unaffected.

Selected bits in the IER can be set by writing to the IER with bit 7 in the data word set to a 1. In this case, each 1 in bits 6 through 0 will set the corresponding bit. For each zero, the corresponding bit will be unaffected. This individual control of the setting and clearing operations allows very convenient control of the interrupts during system operation.

In addition to setting and clearing IER bits, the contents of this register can be read at any time. Bit 7 will be read as a logic 1, however.

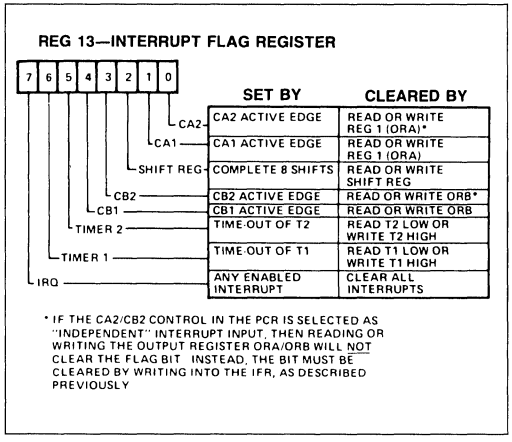


Figure 29. Interrupt Flag Register (IFR)

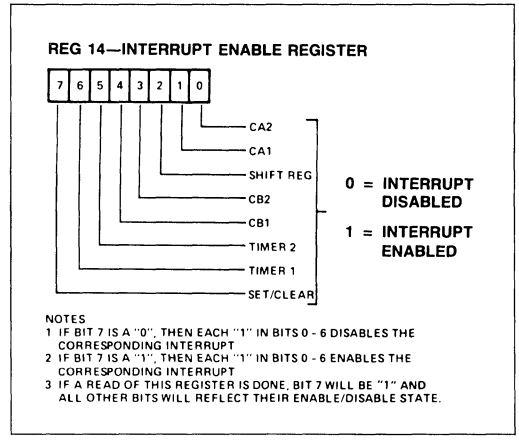


Figure 30. Interrupt Enable Register (IER)

SWITCHING CHARACTERISTICS

(V_{CC} = 5.0 Vdc ±5%, V_{SS} = 0, T_A = T_L to T_H, unless otherwise noted)

PERIPHERAL INTERFACE TIMING

Parameter	Symbol	Min.	Max.	Unit	Figure
Rise and Fall Time for CA1, CB1, CA2 and CB2 Input Signals	t_r, t_f	—	1.0	μs	—
Delay Time, Clock Negative Transition to CA2 Negative Transition (read handshake or pulse mode)	t_{CA2}	—	1.0	μs	31a, 31b
Delay Time, Clock Negative Transition to CA2 Positive Transition (pulse mode)	t_{RS1}	—	1.0	μs	31a
Delay Time, CA1 Active Transition to CA2 Positive Transition (handshake mode)	t_{RS2}	—	2.0	μs	31b
Delay Time, Clock Positive Transition to CA2 or CB2 Negative Transition (write handshake)	t_{WHS}	0.05	1.0	μs	31c, 31d
Delay Time, Periphral Data Valid to CB2 Negative Transition	t_{DS}	0.20	1.5	μs	31c, 31d
Delay Time, Clock Positive Transition to CA2 or CB2 Positive Transition (pulse mode)	t_{RS3}	—	1.0	μs	31c
Delay Time, CA1 or CB1 Active Transition to CA2 or CB2 Positive Transition (handshake mode)	t_{RS4}	—	2.0	μs	31d
Delay Time Required from CA2 Output to CA1 Active Transition (handshake mode)	t_{21}	400	—	ns	31d
Setup Time, Peripheral Data Valid to CA1 or CB1 Active Transition (input latching)	t_{IL}	300	—	ns	31e
CA1, CB1 Setup Prior to Transition to Arm Latch	t_{AL}	300	—	ns	31e
Peripheral Data Hold After CA1, CB1 Transition	t_{PDH}	150	—	ns	31e
Shift-Out Delay Time — Time from Ø2 Falling Edge to CB2 Data Out	t_{SR1}	—	300	ns	31f
Shift Clock Setup Time — Time from CB1 Shift Clock to Ø2 Rising Edge	t_{SR2}	0	—	ns	31g
Pulse Width — PB6 Input Pulse	t_{IPW}	2 × T_{CY}	—		31i
Pulse Width — CB1 Input Clock	t_{ICW}	2 × T_{CY}	—		31h
Pulse Spacing — PB6 Input Pulse	t_{IPS}	2 × T_{CY}	—		31i
Pulse Spacing — CB1 Input Pulse	t_{ICS}	2 × T_{CY}	—		31h
Note: CB1 input sampled while Ø2 is low.					

BUS TIMING

Parameter	Symbol	1 MHz		2 MHz		3 MHz		4 MHZ		Unit	Figure
		Min	Max	Min	Max	Min	Max	Min	Max		
Cycle Time	t_{CY}	1000	—	500	—	330	—	250	—	ns	32a, 32b
Phase 2 Pulse Width High	t_{PWH}	470	—	240	—	160	—	120	—	ns	
Phase 2 Pulse Width Low	t_{PWL}	470	—	240	—	160	—	120	—	ns	
Phase 2 Transition	$t_{R,F}$	—	30	—	30	—	30	—	30	ns	
Read											
Select, R/$\overline{W}$ Setup	t_{ACR}	160	—	90	—	65	—	45	—	ns	32a
Select, R/$\overline{W}$ Hold	t_{CAR}	0	—	0	—	0	—	0	—	ns	
Data Bus Delay	t_{CDR}	—	320	—	150	—	130	—	75	ns	
Data Bus Hold	t_{HR}	10	—	10	—	10	—	10	—	ns	
Peripheral Data Setup	t_{PCR}	300	—	150	—	110	—	75	—	ns	
Write											
Select, R/$\overline{W}$ Setup	t_{ACW}	160	—	90	—	65	—	45	—	ns	32b
Select, R/$\overline{W}$ Hold	t_{CAW}	0	—	0	—	0	—	0	—	ns	
Data Bus Setup	t_{DCW}	195	—	75	—	65	—	45	—	ns	
Data Bus Hold	t_{HW}	10	—	10	—	10	—	10	—	ns	
Peripheral Data Delay	t_{CPW}	—	1000	—	500	—	330	—	250	ns	

PERIPHERAL INTERFACE WAVEFORMS

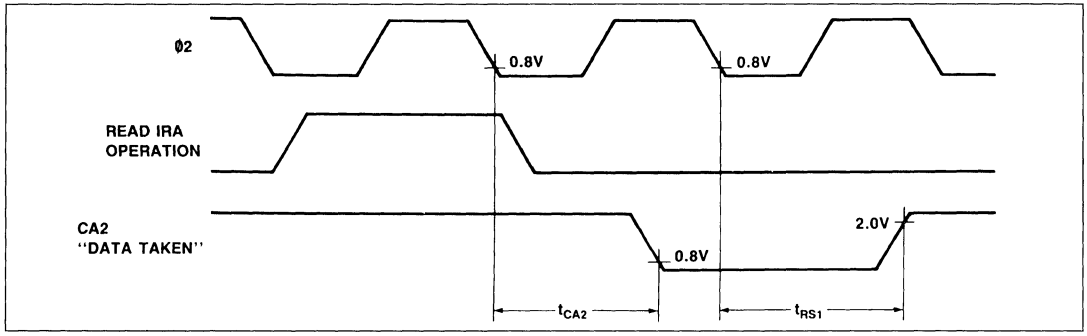


Figure 31a. CA2 Timing for Read Handshake, Pulse Mode

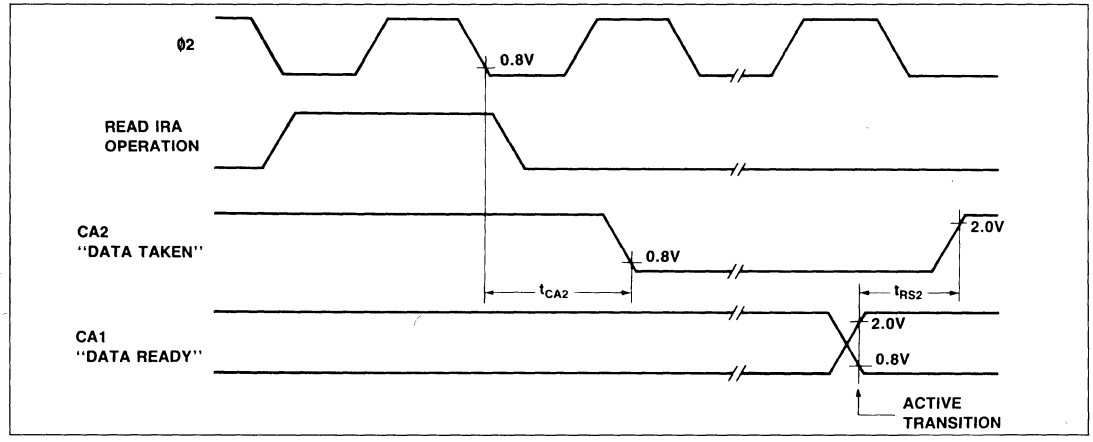


Figure 31b. CA2 Timing for Read Handshake, Handshake Mode

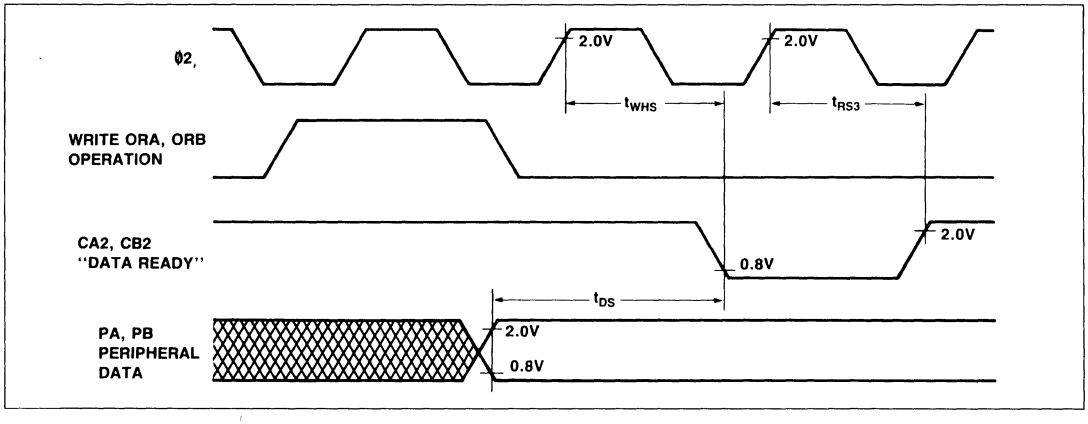


Figure 31c. CA2, CB2 Timing for Write Handshake, Pulse Mode

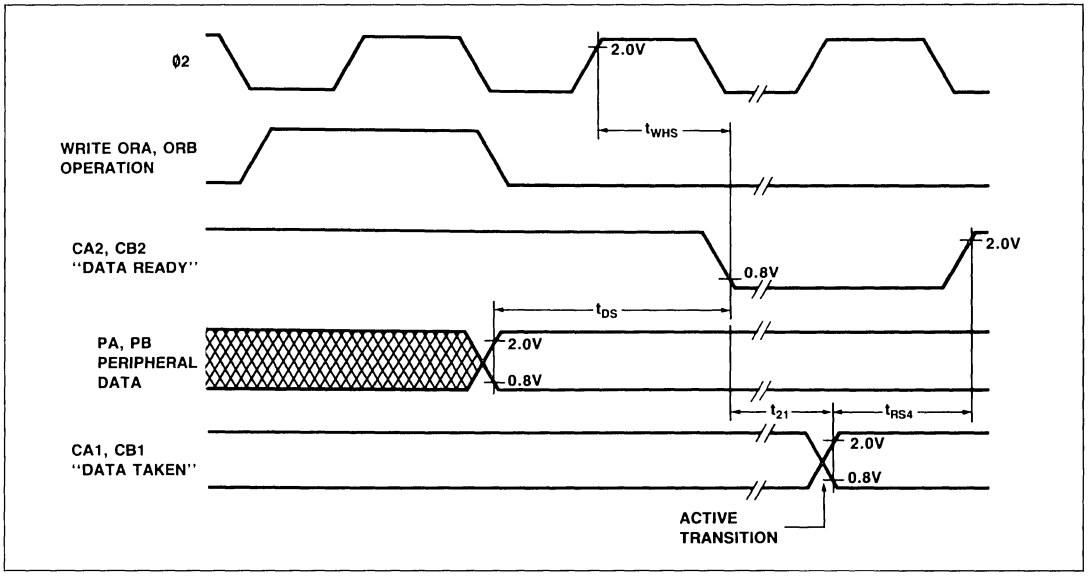


Figure 31d. CA2, CB2 Timing for Write Handshake, Handshake Mode

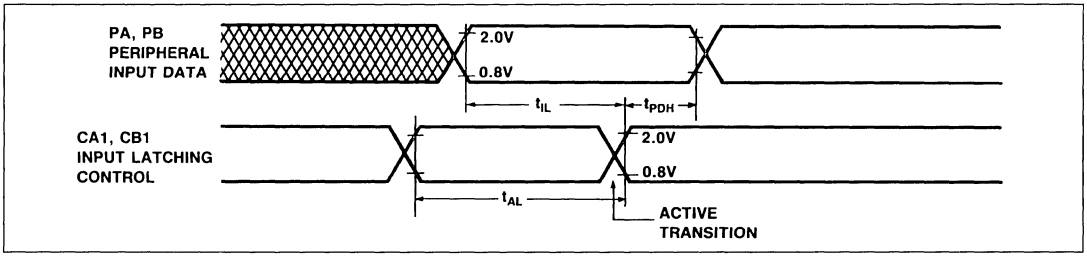


Figure 31e. Peripheral Data Input Latching Timing

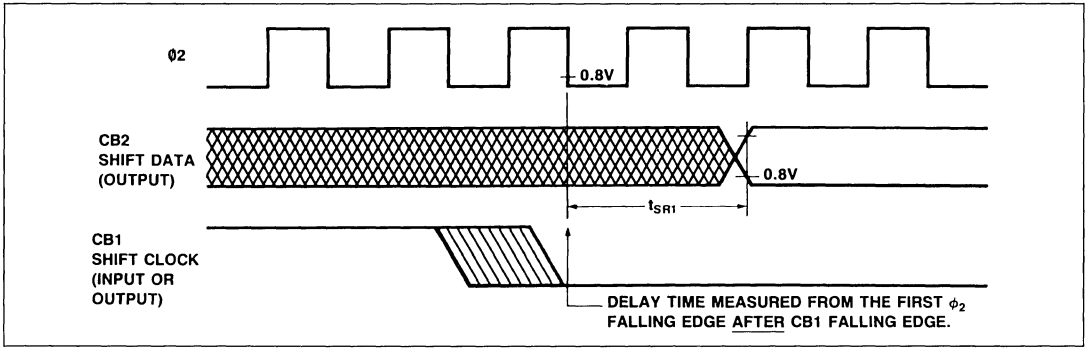


Figure 31f. Timing for Shift Out with Internal or External Shift Clocking

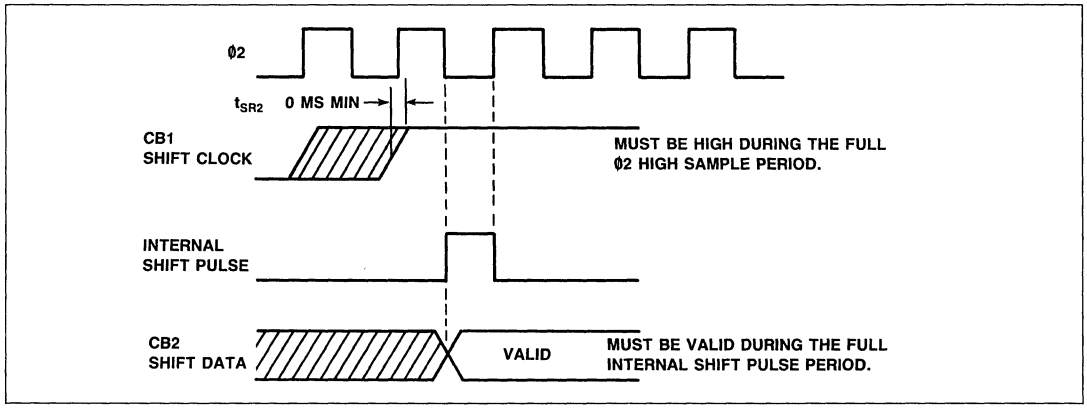


Figure 31g. Timing for Shift In with Internal or External Shift Clocking

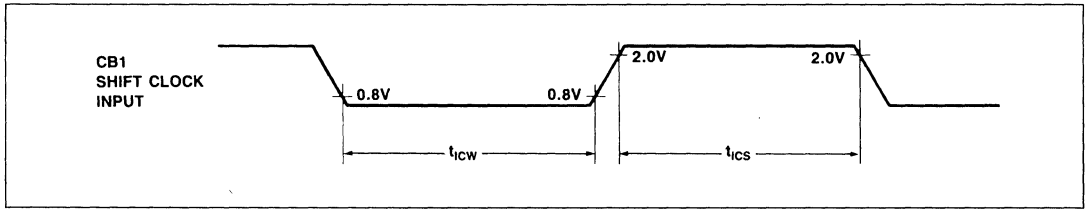


Figure 31h. External Shift Clock Timing

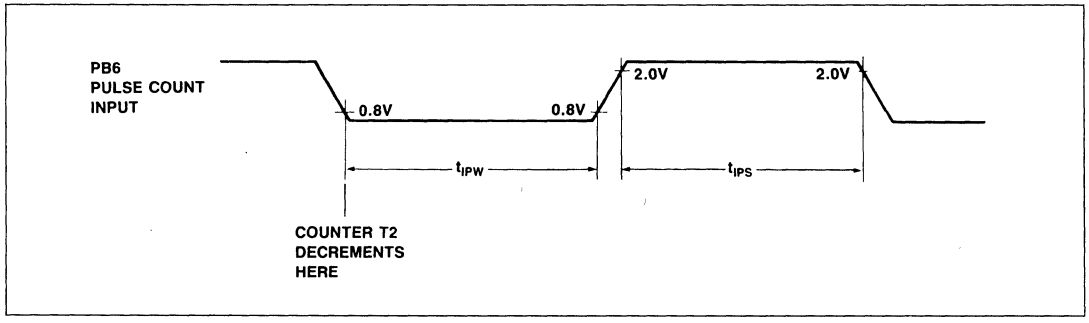


Figure 31i. Pulse Count Input Timing

BUS TIMING WAVEFORMS

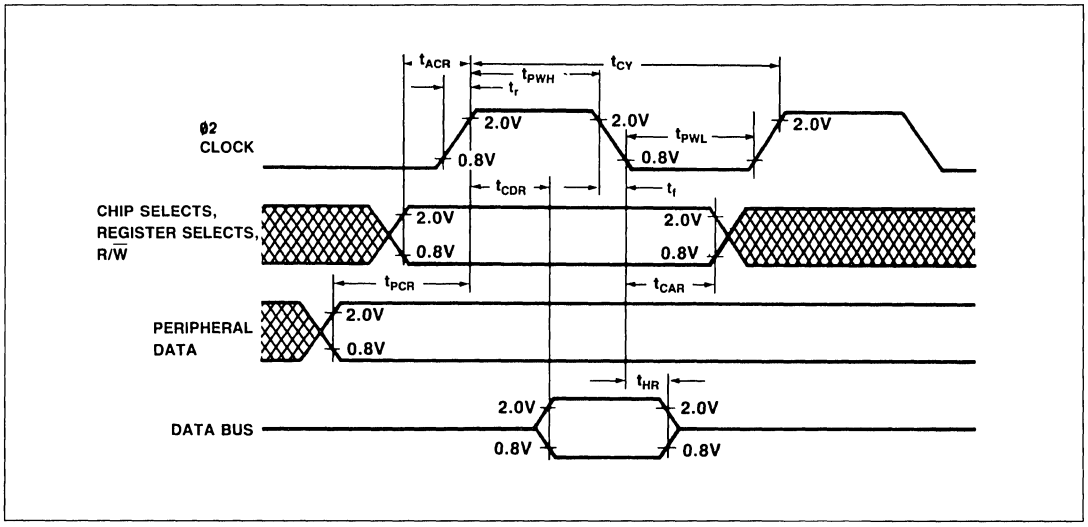


Figure 32a. Read Timing Waveforms

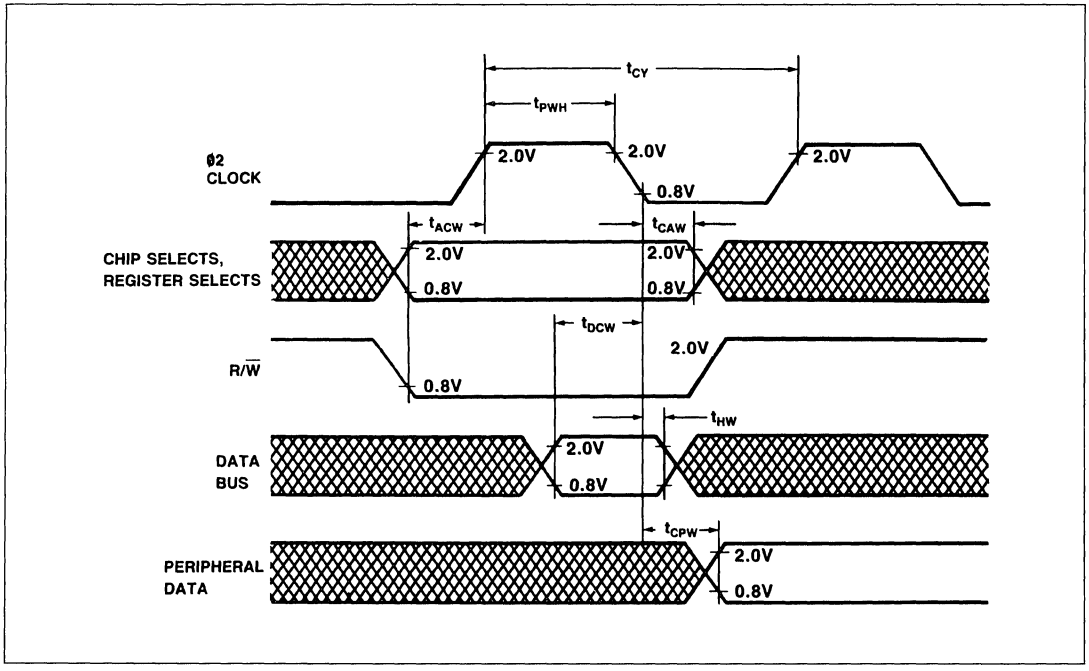


Figure 32b. Write Timing Waveforms

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to +7.0	Vdc
Input Voltage	V_{IN}	−0.3 to V_{CC} +0.3	Vdc
Output Voltage	V_{OUT}	−0.3 to V_{CC} +0.3	Vdc
Operating Temperature Commercial Industrial	T_A	 0 to +70 −40 to +85	°C
Storage Temperature	T_{STG}	−55 to +150	°C

*NOTE: Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the other sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING CONDITIONS

Parameter	Symbol	Value
Supply Voltage	V_{CC}	5V ±5%
Temperature Range Commercial Industrial	T_A	T_L to T_H 0°C to 70°C −40°C to +85°C

ELECTRICAL CHARACTERISTICS

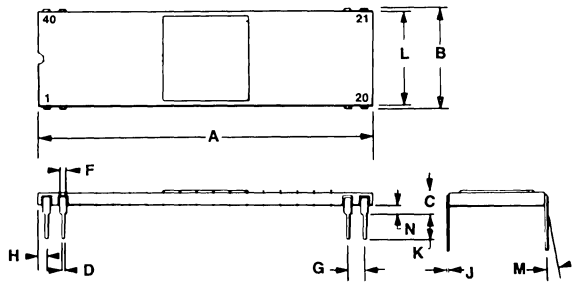
(V_{CC} = 5.0 Vdc ±5%, V_{SS} = 0, T_A = T_L to T_H, unless otherwise noted)

Parameter	Symbol	Min.	Typ.[3]	Max.	Unit[1]	Test Conditions
Input High Voltage Logic	V_{IH}	 +2.0	 —	 V_{CC}	V	
Input Low Voltage Logic	V_{IL}	 −0.3	 —	 +0.8	V	
Input Leakage Current R/W, RES, RS0, RS1, RS2, RS3, CS1, CS2, CA1, Ø2	I_{IN}	—	±1	±2.5	µA	V_{IN} = 0V to V_{CC} V_{CC} = 5.25V
Input Leakage Current for Three-State Off D0–D7	I_{TSI}	—	±2	±10	µA	V_{IN} = 0.4V to 2.4V V_{CC} = 5.25V
Input High Current PA0–PA7, CA2, PB0–PB7, CB1, CB2	I_{IH}	−200	−400	—	µA	V_{IH} = 2.4V
Input Low Current PA0–PA7, CA2 PB0–PB7, CB1, CB2	I_{IL}	 — —	 −1.6 —	 −2.6 −1.6	 mA mA	V_{IL} = 0.4V
Output High Voltage All outputs PB0–PB7 (Darlington Drive)	V_{OH}	 2.4 1.5	 — —	 — —	 V V	V_{CC} = 4.75V I_{LOAD} = 200 µA I_{LOAD}[2] = −3.2 mA
Output Low Voltage PA0–PA7, CA2, D0–D7 IRQ, PB0–PB7, CB1, CB2	V_{OL}	—	—	+0.4	V	V_{CC} = 4.75V I_{LOAD} = 3.2 mA I_{LOAD} = 1.6 mA
Output High Current (Sourcing) All outputs PB0–PB7 (Darlington Drive) CB1, CB2	I_{OH}	 −200 −3.2 −750	 −1500 −6 —	 — — —	 µA mA µA	 V_{OH} = 2.4V V_{OH} = 1.5V V_{OH} = 2.4V
Output Low Current (Sinking) PA0–PA7, CA2, D0–D7 All others	I_{OL}	 3.2 1.6	 — —	 — —	 mA mA	V_{OL} = 0.4V
Output Leakage Current (Off State) IRQ	I_{OFF}	—	1	±10	µA	V_{OH} = 2.4V V_{CC} = 5.25V
Power Dissipation	P_D	—	7	10	mW/MHz	
Input Capacitance D0–D7, PA0–PA7, CA1, CA2, PB0–PB7, CB1, CB2 R/W, RES, RS0, RS1, RS2, RS3, CS1, CS2 Ø2	C_{IN}	 — — —	 — — —	 10 7 20	 pF pF pF	V_{CC} = 5.0V V_{IN} = 0V f = 2 MHz T_A = 25°C
Output Capacitance	C_{OUT}	—	—	10	pF	

Notes:
1. All units are direct current (DC) except for capacitance.
2. Negative sign indicates outward current flow, positive indicates inward flow.
3. Typical values shown for V_{CC} = 5.0V and T_A = 25°C.
4. Maximum loading on CB1 and CB2 is 50 pF.

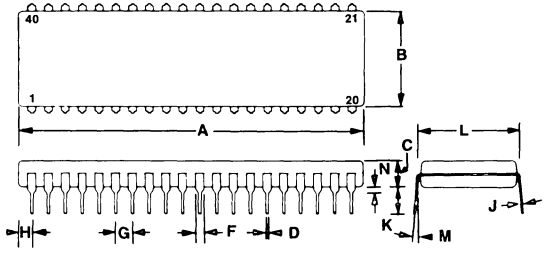
PACKAGE DIMENSIONS

40-PIN CERAMIC DIP



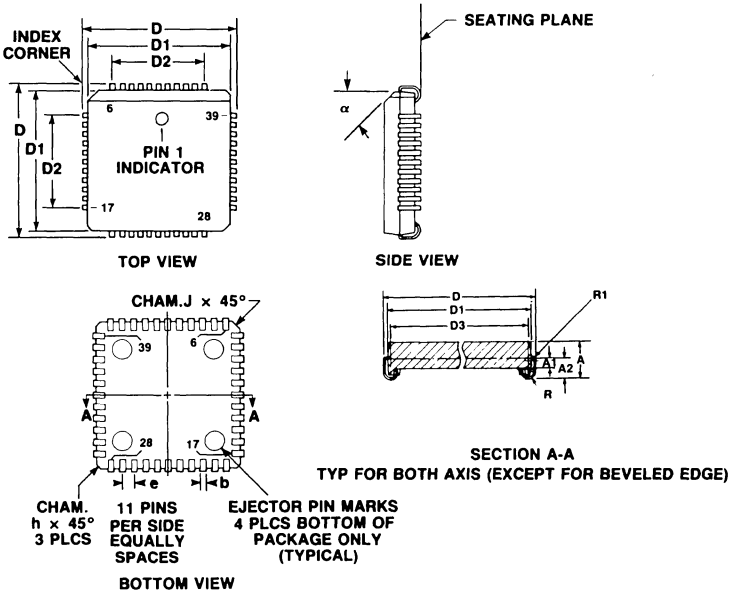
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	50.29	51.31	1.980	2.020
B	14.86	15.62	0.100	0.615
C	2.54	4.19	0.585	0.165
D	0.38	0.53	0.015	0.021
F	0.76	1.40	0.030	0.055
G	2.54 BSC		0.100 BSC	
H	0.76	1.78	0.030	0.070
J	0.20	0.33	0.008	0.013
K	2.54	4.19	0.100	0.165
L	14.60	15.37	0.575	0.605
M	0°	10°	0°	10°
N	0.51	1.52	0.020	0.060

40-PIN PLASTIC DIP



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	51.28	52.32	2.040	2.060
B	13.72	14.22	0.540	0.560
C	3.55	5.08	0.140	0.200
D	0.36	0.51	0.014	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.30	0.008	0.012
K	3.30	4.32	0.130	0.170
L	15.24 BSC		0.600 BSC	
M	7°	10°	7°	10°
N	0.51	1.02	0.020	0.040

44-PIN PLASTIC LEADED CHIP CARRIER (PLCC)



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	4.14	4.39	0.163	0.173
A1	1.37	1.47	0.054	0.058
A2	2.31	2.46	0.091	0.097
b	0.457 TYP		0.018 TYP	
D	17.45	17.60	0.687	0.693
D1	16.46	16.56	0.648	0.652
D2	12.62	12.78	0.497	0.503
D3	15.75 REF		0.620 REF	
e	1.27 BSC		0.050 BSC	
h	1.15 TYP		0.045 TYP	
J	0.25 TYP		0.010 TYP	
α2	45° TYP		45° TYP	
R	0.89 TYP		0.035 TYP	
R1	0.25 TYP		0.010 TYP	

R65NC22/R65C22 DIFFERENCES

R65C22	R65NC22
1. Register select lines are decoded during $\overline{\phi 2}$.	1. Register select lines are decoded during $\overline{\phi 2}$ only if $\overline{CS2}$ is active low.
2. CB1 must not change during last 100 ns of $\phi 2$. CB1 must have a pulse width greater than one period.	2. CB1 can change anytime but is sampled only during $\overline{\phi 2}$. CB1 must have a pulse greater than one period.
3. PB0–PB7 and CB1, CB2 have active pull-ups.	3. PB0–PB7 and CB1, CB2 have passive pull ups ($\approx$3 KΩ).
4. PB0–PB7, CB1 and CB2 represent two standard TTL loads in the input mode and will drive two standard TTL loads in the output mode.	4. PB0–PB7, CB1 and CB2 represent one standard TTL load in the input mode and will drive one standard TTL load in the output mode.

R65C24
Peripheral Interface Adapter/Timer (PIAT)

DESCRIPTION

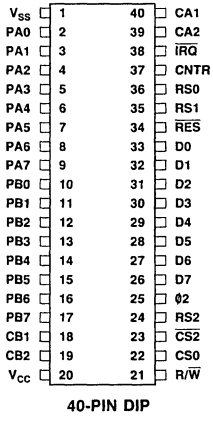
The R65C24 Peripheral Interface Adapter/Timer (PIAT) is designed to solve a broad range of peripheral control problems in the implementation of microcomputer systems. This device allows a very effective trade-off between software and hardware by providing significant capability and flexibility in a low cost chip. When coupled with the power and speed of the R6500, R6500/* or R65C00 family of microprocessors, the R65C24 allows implementation of very complex systems at a minimum overall cost.

Control of peripheral devices is handled primarily through two 8-bit bidirectional ports. Each of these lines can be programmed to act as either an input or an output. In addition, four peripheral control/interrupt input lines are provided. These lines can be used to interrupt the processor or to "handshake" data between the processor and a peripheral device.

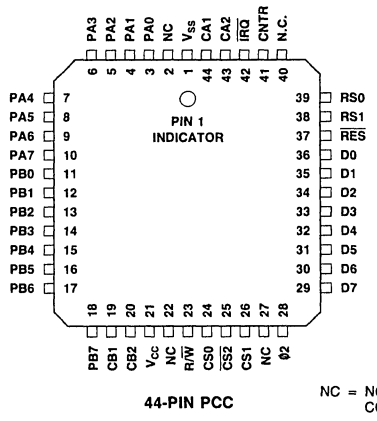
The PIAT also contains one 16-bit Counter/Timer comprised of a 16-bit counter, two 8-bit latches associated with the counter, and an 8-bit snapshot latch for the upper half of the counter. A counter mode control register, under software direction, selects any one of eight counter modes of operation, and the status register contains an underflow flag to report counter time-out. A maskable interrupt request allows immediate CPU notification upon counter time-out.

FEATURES

- Low power CMOS N-well sillicon gate technology
- Two 8-bit bidirectional I/O ports with individual data direction control
- Programmable 16-bit Counter/Timer with eight modes of operation
- Three 8-bit latches associated with the Counter/Timer
- Selectable divide-by-sixteen prescaler for all modes
- Automatic "Handshake" control of data transfers
- Three interrupts with program control
  - — Port A
  - — Port B
  - — Counter/Timer
- 1, 2, 3, and 4 MHz versions
- Commercial and industrial temperature range versions
- Wide variety of packages
  - — 40-pin plastic and ceramic DIP
  - — 44-pin plastic leaded chip carrier (PLCC)
- Single +5 Vdc power requirement
- Compatible with the R6500, R6500/* and R65C00 family of microprocessors



40-PIN DIP



44-PIN PCC

NC = NO INTERNAL CONNECTION

Figure 1. R65C24 Pin Assignments

ORDERING INFORMATION

Part Number:
R65C24

- Temperature Range:
  - Blank = 0°C to +70°C
  - E = −40°C to +85°C
- Frequency Range:
  - 1 = 1 MHz
  - 2 = 2 MHz
  - 3 = 3 MHz
  - 4 = 4 MHz
- Package:
  - C = 40-Pin Ceramic DIP
  - P = 40-Pin Plastic DIP
  - J = 44-Pin Plastic Leaded Chip Carrier (PLCC)

INTERFACE SIGNALS

The PIAT interfaces to the R6500, R6500/* or the R65C00 microprocessor family with a reset line, a Ø2 clock line, a read/write line, an interrupt request line, three register select lines, two chip select lines, and an 8-bit bidirectional data bus.

The PIAT interfaces to the peripheral devices with four interrupt/control lines and two 8-bit bidirectional data ports. A Counter/Timer input/output line (CNTR) also interfaces to a peripheral device.

Figure 1 (on the front page) shows the pin assignments for these interface signals and Figure 2 shows the interface relationship of these signal as they pertain to the CPU and the peripheral devices.

CHIP SELECT (CS0, $\overline{CS2}$)

The PIAT is selected when CS0 is high and $\overline{CS2}$ is low. These two chip select lines are normally connected to the processor address lines either directly or through external decoder circuits. When the PIAT is selected, data will be transferred between the data lines and PIAT registers, and/or peripheral interface lines as determined by the R/$\overline{W}$, RS0, RS1 and RS2 lines and the contents of Control Registers A and B.

NOTE:

An R65C24 PIAT may be installed in a circuit in place of an R65C21 PIA subject to chip select considerations. Since the R65C21 has a CS1 input and the R54C24 does not have a CS1 input, the PIAT will be selected in the same addresses as the PIA *and maybe more* depending upon external address decoding circuitry.

RESET SIGNAL ($\overline{RES}$)

The Reset ($\overline{RES}$) input initializes the R65C24 PIAT. A low signal on the ($\overline{RES}$) input causes all internal registers to be cleared.

CLOCK SIGNAL (Ø2)

The Phase 2 Clock Signal (Ø2) is the system clock that triggers all data transfers between the CPU and the PIAT. Ø2 is generated by the CPU and is therefore the synchronizing signal between the CPU and the PIAT.

READ/WRITE SIGNAL (R/$\overline{W}$)

Read/Write (R/$\overline{W}$) controls the direction of data transfers between the PIAT and the data lines associated with the CPU and the peripheral devices. A high on the R/$\overline{W}$ line permits the peripheral devices to transfer data to the CPU from the PIAT. A low on the R/$\overline{W}$ line allows data to be transfered from the CPU to the peripheral devices from the PIAT.

REGISTER SELECT (RS0, RS1, RS2)

Two of the Register Select lines (RS0, RS1), in conjunction with the Control Registers (CRA, CRB), select various R65C24 registers to be accessed by the CPU. RS0 and RS1 are normally connected to the microprocessor (CPU) address output lines. Through control of these lines, the CPU can write directly into the Control Registers (CRA, CRB), the Data Direction Registers (DDRA, DDRB) and the Peripheral Output Registers (ORA, ORB). In addition, the processor may directly read the contents of the Control Registers and the Data Direction Registers. Accessing the Peripheral Output Register for the purpose of reading data back into the processor operates differently on the ORA and the ORB registers and, therefore, are shown separately in Table 1.

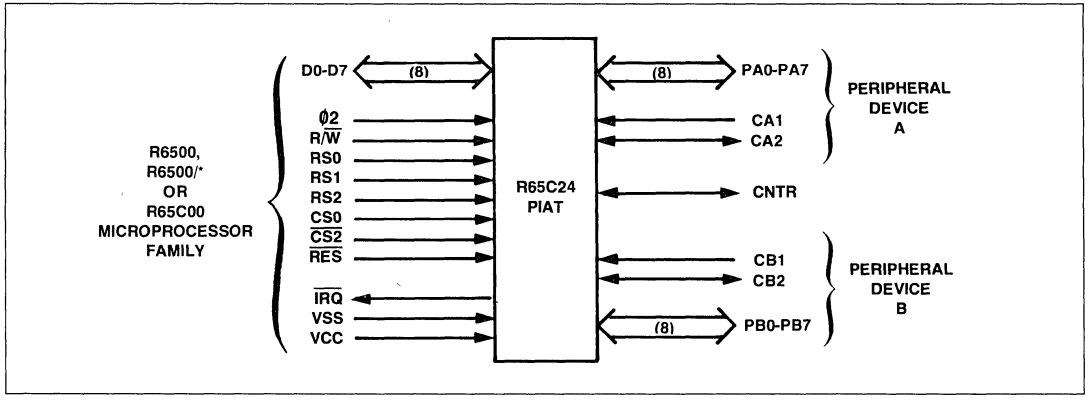


Figure 2. Interface Signals Relationship

Table 1. Peripheral Register Addressing

Register Address (Hex)	Register Select Lines			Data Direction Register Control		Register Operation	
	RS2	RS1	RS0	CRA (Bit 2)	CRB (Bit 2)	R/$\overline{W}$ = H	R/$\overline{W}$ = L
4	H	L	L	1	—	Read PIBA	Write ORA
4	H	L	L	0	—	Read DDRA	Write DDRA
5	H	L	H	—	—	Read CRA	Write CRA
6	H	H	L	—	1	Read PIBB	Write ORB
6	H	H	L	—	0	Read DDRB	Write DDRB
7	H	H	H	—	—	Read CRB	Write CRB

Register Select line RS2 determines whether the addressed registers are part of the Counter/Timer or the peripheral Port A and Port B sections of the PIAT. When RS2 is high, the Port A/Port B registers shown in Table 1 are selected. When the RS2 is low, the Counter/Timer registers are selected and operated upon as shown in Table 2.

Table 2. Counter/Timer Register Addressing

Register Address (Hex)	Register Select Lines			Counter/Timer Operation	
	RS2	RS1	RS0	(R/$\overline{W}$ = H)	(R/$\overline{W}$ = L)
0	L	L	L	Read Snapshot Latch (SL) SL → D0-D7 0 → UF	Write Upper Latch (UL) D0-D7 → UL 0 → UF Load and Enable Counter UL → UC, LL → LC
1	L	L	H	Read Upper Counter (UC) UC → D0-D7	Write Upper Latch (UL) D0-D7 → UL
2	L	H	L	Read Lower Counter (LC) LC → D0-D7 UC → SL	Write Lower Latch (LL) D0-D7 → LL UC → SL
3	L	H	H	Read Status Register (SR) SR → D0-D7 0 → UF,	Write Counter Control Mode Register (CMCR) D0-D7 → CMCR

INTERRUPT REQUEST LINE ($\overline{IRQ}$)

Three internal active low Interrupt Request lines ($\overline{IRQA}$, $\overline{IRQB}$, and $\overline{IRQT}$) act to interrupt the microprocessor through the external $\overline{IRQ}$ output. $\overline{IRQ}$ is an open drain output and is capable of sinking 1.6 mA from an external source. This permits all interrupt request lines to be tied together in a wired-OR configuration. The A and B in the titles of these internal lines correspond to the peripheral port A and the peripheral port B so that each interrupt request line services one peripheral data port. The T corresponds to the Counter/Timer generated interrupt request.

$\overline{IRQA}$ and $\overline{IRQB}$ Lines — These two internal Interrupt Request lines are associated with the Port A and Port B sections of the PIAT and are controlled by Control Registers CRA and CRB, and the Peripheral Control lines CA1, CA2, CB1, and CB2.

These Interrupt Request lines have three interrupt flag bits which can cause the Interrupt Request line to go low. These flags are bits 6 and 7 in the two Control Registers (CRA, CRB). These flags act as the link between the peripheral interrupt signals and the microprocessor interrupt inputs. Each flag has a corresponding interrupt disable bit which allows the processor to enable or disable the interrupt from each of the four interrupt inputs (CA1, CA2, CB1, CB2). The four interrupt flags are set (enabled) by active transitions of the signal on the interrupt input (CA1, CA2, CB1, CB2).

CRA bit 7 (IRQA1) is always set by an active transition of the CA1 interrupt input signal. However, $\overline{IRQA}$ can be disabled by setting bit 0 in CRA to a 0. Likewise, CRA bit 6 (IRQA2) can be set by an active transition of the CA2 interrupt input signal and $\overline{IRQA}$ can be disabled by setting bit 3 in CRA to a 0.

Both bit 6 and bit 7 in CRA are reset by a "Read Peripheral Output Register A" operation. This is defined as an operation in which the read/write, proper data direction register and register select signals are provided to allow the processor to read the Peripheral A I/O port. A summary of $\overline{IRQA}$ control is shown in Table 3.

Control of $\overline{IRQB}$ is performed in exactly the same manner as that described above for $\overline{IRQA}$ (Table 3). Bit 7 in CRB (IRQB1) is set by an active transition on CB1 and $\overline{IRQB}$ from this flag is controlled by CRB bit 0. Likewise, bit 6 (IRQB2) in CRB is set by an active transition on CB2, and $\overline{IRQB}$ from this flag is controlled by CRB bit 3. Also, both bit 6 and bit 7 of CRB are reset by a "Read Peripheral B Output Register" operation.

$\overline{IRQT}$ Line — The internal $\overline{IRQT}$ line is associated with the Counter/Timer and is controlled by the $\overline{IRQT}$ Enable bit in the Counter Mode Control Register and the Underflow Flag in the Status Register. A thorough discussion of the functions and operation of the $\overline{IRQT}$ line is given in the Counter/Timer Operation section of this product description.

Table 3. $\overline{IRQA}$ and $\overline{IRQB}$ Control Summary

Control Register Bits	Action
CRA-7=1 and CRA-0=1	$\overline{IRQA}$ goes low (Active)
CRA-6=1 and CRA-3=1	$\overline{IRQA}$ goes low (Active)
CRB-7=1 and CRB-0=1	$\overline{IRQB}$ goes low (Active)
CRB-6=1 and CRB-3=1	$\overline{IRQB}$ goes low (Active)

INTERRUPT INPUT/PERIPHERAL CONTROL LINES (CA1, CA2, CB1, CB2)

The four interrupt input/peripheral control lines provide a number of special peripheral control functions. These lines greatly enhance the power of the two general purpose interface ports (PA0-PA7, PB0-PB7). Figure 5 summarizes the operation of these control lines.

CA1 is an interrupt input only. An active transition of the signal on this input will set bit 7 of the Control Register A to a logic 1. The active transition can be programmed by setting a 0 in bit 1 of the CRA if the interrupt flag (bit 7 of CRA) is to be set on a negative (high to low) transition of the CA1 signal, or by setting a 1 if it is to be set on a positive (low to high) transition.

CA2 can act as a totally independent interrupt or as a peripheral control output. As an input (CRA, bit 5 = 0) it acts to set the interrupt flag, bit 6 of CRA, to a logic 1 on the active transition selected by bit 4 of CRA.

These control register bits and interrupt inputs serve the same basic function as that described above for CA1. The input signal sets the interrupt flag which serves as the link between the peripheral device and the processor interrupt structure. The interrupt disable bit allows the processor to exercise control over the system interrupt.

In the output mode (CRA, bit 5 = 1), CA2 can operate independently to generate a single pulse each time the microprocessor reads the data on the Peripheral A I/O port. This mode is selected by setting CRA, bit 4 to a 0 and CRA, bit 3 to a 1. This pulse output can be used to control the counters, shift registers, etc. which make sequential data available on the Peripheral input lines.

A second output mode allows CA2 to be used in conjunction with CA1 to "handshake" between the processor and the peripheral device. On the A side, this technique allows positive control of data transfers from the peripheral device into the microprocessor. The CA1 input signals the processor that data is available by interrupting the processor. The processor reads the data and sets CA2 low. This signals the peripheral device that it can make new data available.

The final output mode can be selected by setting bit 4 of CRA to a 1. In this mode, CA2 is a simple peripheral control output which can be set high or low by setting bit 3 of CRA to a 1 or a 0, respectively.

CB1 operates as an interrupt input only in the same manner as CA1. Bit 7 of CRB is set by the active transition selected by bit 0 of CRB. Likewise, the CB2 input mode operates exactly the same as the CA2 input modes. The CB2 output modes, CRB bit 5 = 1, differ somewhat from those of CA2. The pulse output occurs when the processor writes data into the Peripheral B Output Register. Also, the "handshaking" operates on data transfers from the processor into the peripheral device.

FUNCTIONAL DESCRIPTION

The R65C24 PIAT is organized into three independent sections referred to as the A Side, the B Side, and a Counter/Timer. The A Side and B Side each consist of a Control Register (CRA, CRB), Data Direction Register (DDRA, DDRB), Output Register (ORA, ORB), Interrupt Status Control (ISCA, ISCB), and the buffers necessary to drive the Peripheral Interface buses. Data Bus Buffers (DBB) interface data from the two sections to the data bus, while the Data Input Register (DIR) interfaces data from the DBB to the PIAT registers. Chip Select and R/$\overline{W}$ control circuitry interface to the processor bus control lines. The Counter/Timer consists of a 16-bit counter; i.e., an 8-bit Upper Counter (UC) and 8-bit Lower Counter (LC), an 8-bit Upper Latch (UL), an 8-bit Lower Latch (LL), an 8-bit Snapshot Latch (SL), and a Status Register (SR). A Counter Mode Control Register (CMCR) selects the Counter/Timer mode of operation. Figure 3 is a block diagram of the R65C24 PIAT.

DATA INPUT REGISTER (DIR)

When the microprocessor writes data into the PIAT, the data which appears on the data bus during the Ø2 clock pulse is latched into the Data Input Register (DIR). The data is then transferred into one of six internal registers of the PIAT after the trailing edge of the Ø2 clock. This assures that the data on the peripheral output lines will make smooth transitions from high to low (or from low to high) and the voltage will remain stable except when it is going to the opposite polarity.

CONTROL REGISTERS (CRA AND CRB)

Table 4 illustrates the bit designation and functions in the two control registers. The control registers allow the microprocessor to control the operation of the Interrupt Control inputs (CA1, CA2, CB1, CB2), and Peripheral Control outputs (CA2, CB2). Bit 2 in each register controls the addressing of the Data Direction Registers (DDRA, DDRB) and the Output Registers (ORA, ORB). In addition, two bits (bit 6 and 7) in each control register indicate the status of the Interrupt Input lines (CA1, CA2, CB1, CB2). These Interrupt Status bits (IRQA1, IRQA2 or IRQB1, IRQB2) are normally interrogated by the microprocessor during the $\overline{IRQ}$ interrupt service routine to determine the source of the interrupt.

DATA DIRECTION REGISTERS (DDRA, DDRB)

The Data Direction Registers (DDRA, DDRB) allow the processor to program each line in the 8-bit Peripheral I/O port to be either an input or an output. Each bit in DDRA controls the corresponding line in the Peripheral A port and each bit in DDRB controls the corresponding line in the Peripheral B port. Writing a 0 in a bit position in the Data Direction Register causes the corresponding Peripheral I/O line to act as an input; a 1 causes it to act as an output.

Bit 2 (DDRA, DDRB) in each Control Register (CRA and CRB) controls the accessing to the Data Direction Register or the Peripheral interface. If bit 2 is a 1, a Peripheral Output register (ORA, ORB) is selected, and if bit 2 is a 0, a Data Direction Register (DDRA, DDRB) is selected. The Data Direction Register Access Control bit, together with the Register Select lines (RS0, RS1 and RS2) selects the various internal registers as shown in Table 1.

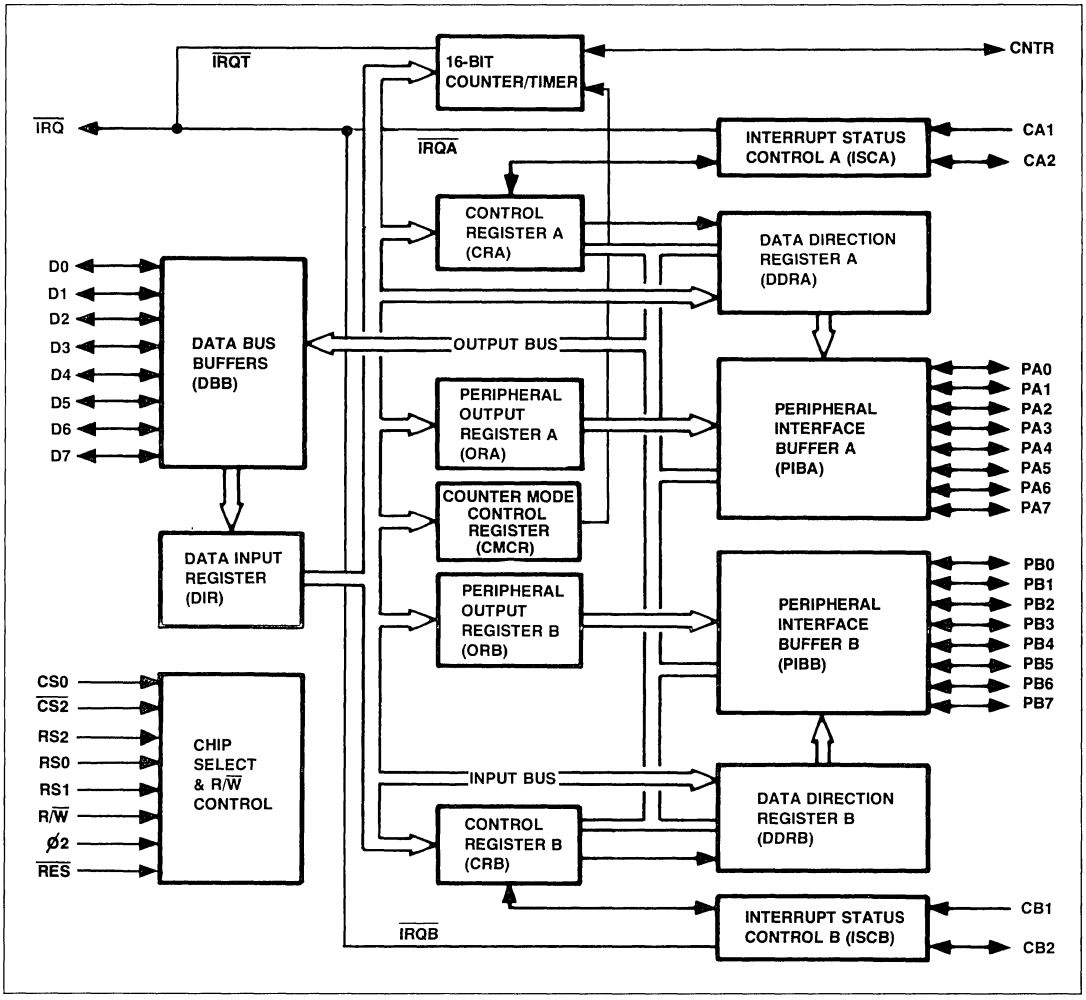


Figure 3. R65C24 PIAT Block Diagram

Table 4. Control Registers Bit Designations

	7	6	5	4	3	2	1	0
CRA	IRQA1	IRQA2	CA2 Control			DDRA Access	CA1 Control	
CRB	IRQB1	IRQB2	CB2 Control			DDRB Access	CB1 Control	

In order to write data into DDRA, ORA, DDRB, or ORB registers, bit 2 in the proper Control Register must first be set. The desired register may then be accessed with the address determined by the address interconnect technique used.

PERIPHERAL OUTPUT REGISTERS (ORA, ORB)

The Peripheral Output Registers (ORA, ORB) store the output data from the Data Bus Buffers (DBB) which appears on the Peripheral I/O port. If a line on the Peripheral A Port is programmed as an output by the DDRA, writing a 0 into the corresponding bit in the ORA causes that line to go low ($\leq$0.4 Vdc); writing a 1 causes the line to go high. The lines of the Peripheral B port are controlled by ORB in the same manner.

INTERRUPT STATUS CONTROL (ISCA, ISCB)

The four interrupt/peripheral control lines (CA1, CA2, CB1, CB2) are controlled by the Interrupt Status Control logic (A, B). This logic interprets the contents of the corresponding Control Register and detects active transitions on the interrupt inputs.

PERIPHERAL I/O PORTS (PA0-PA7, PB0-PB7)

The Peripheral A and Peripheral B I/O ports allow the microprocessor to interface to the input lines on the peripheral device by writing data into the Peripheral Output Register. They also allow the processor to interface with the peripheral device output lines by reading the data on the Peripheral Port input lines directly onto the data bus and into the internal registers of the processor.

Each of the Peripheral I/O lines can be programmed to act as an input or an output. This is accomplished by setting a 1 in the corresponding bit in the Data Direction Register for those lines which are to act as outputs. A 0 in a bit of the Data Direction Register causes the corresponding Peripheral I/O lines to act as an input.

The buffers which drive the Peripheral A I/O lines contain "passive" pull-up devices. These pull-up devices are resistive in nature and therefore allow the output voltage to go to Vcc for a logic 1. The switches can sink a full 3.2 mA, making these buffers capable of driving two standard TTL loads.

In the input mode, the pull-up devices are still connected to the I/O pin and still supply current to this pin. For this reason, these lines also represent two standard TTL loads in the input mode.

The Peripheral B I/O port duplicates many of the functions of the Peripheral A port. The process of programming these lines to act as an input or any output is similar to the Peripheral A port, as is the effect of reading or writing this port. However, there are several characteristics of the buffers driving these lines which affect their use in peripheral interfacing.

The Peripheral B I/O port buffers are push-pull devices i.e., the pull-up devices are switched OFF in the 0 state and ON for a logic 1. Since these pull-ups are active devices, the logic 1 voltage will not go higher than +2.4 Vdc.

Unlike the PA0-PA7 lines (which have pull-up devices), the PB0 through PB7 lines have three-state capability which allows them to enter a high impedance state when programmed to be used as input lines. In addition, data on these lines will be read properly, when programmed as output lines, even if the data signals fall below 2.0 Vdc for a "high" state or are above 0.8 Vdc for a "low" state. When programmed as output, each line can drive at least a two TTL load and may also be used as a source of up to 3.2 mA at 1.5 Vdc to directly drive the base of a transistor switch, such as a Darlington pair.

Because these outputs are designed to drive transistors directly, the output data is read directly from the Peripheral Output Register for those lines programmed to act as inputs.

The final characteristic is the high-impedance input state which is a function of the Peripheral B push-pull buffers. When the Peripheral B I/O lines are programmed to act as inputs, the output buffer enters the high impedance state.

DATA BUS BUFFERS (DBB)

The Data Bus Buffers are 8-bit bidirectional buffers used for data exchange, on the D0-D7 Data Bus, between the miroprocessor and the PIAT. These buffers are tri-state and are capable of driving a two TTL load (when operating in an output mode) and represent a one TTL load to the microprocessor (when operating in an input mode).

COUNTER/TIMER

The Counter/Timer includes a 16-bit counter and three 8-bit data latches. It also includes an 8-bit Counter Mode Control Register (CMCR) to select the Counter/Timer operating mode and options and an 8-bit Status Register to report time-out conditions as well as peripheral data port interrupt conditions. Figure 4 illustrates the Timer/Counter.

Counter/Latches — The Upper Counter (UC) and Lower Counter (LC) form a 16-bit down-counter that counts either ϕ2 clock pulses from the processor bus or external events from input line CNTR, depending on the mode selected. The Upper Latch (UL) and Lower Latch (LL) hold the initial higher- and lower-order count values to be loaded into the counter. The Snapshot Latch (SL) is loaded with the value of the UC when the LC is read or the LL is written into by the PIAT. After a read of the LC, the Snapshot Latch is read to provide the current 16-bit value of the counter. The Underflow Flag (UF) in the Status Register (SR) is set to a 1 whenever the counter (UC, LC) decrements past $0000. A Prescaler can be program activated to divide-by-sixteen rather than divide-by-one for any of the Counter/Timer modes.

Counter Mode Control Register — The Counter Mode Control Register (CMCR) allows program selection of any of eight Counter/Timer modes of operation, for the enabling or disabling of the Prescaler, and the enabling or disabling of the $\overline{IRQT}$ interrupt line. Bits 2, 1 and 0 of the CMCR select one of the following Counter/Timer operating modes:

Disable Counter/Timer
One-Shot Interval Timer
Free-Run Interval Timer
Pulse Width Measurement
Event Counter
One-Shot Pulse Width Generation
Free-Run Pulse Generation
Retriggerable Interval Timer

Bit 7 of the CMCR controls the $\overline{IRQT}$ line. When bit 7 is set to a 1, $\overline{IRQT}$ is enabled and an Underflow Flag (UF bit in the Status Register set to a 1) will cause $\overline{IRQ}$ to be asserted. When bit 7 is set to a 0, the $\overline{IRQT}$ is disabled.

Bit 4 of the CMCR enables or disables the Prescaler. A 1 in bit 4 causes the Prescaler to be enabled so that the Counter/Timer is operating in a divide-by-sixteen mode. When this bit is a 0 the Prescaler is disabled so that the Counter/Timer is operating in a normal (divide-by-one) mode.

Status Register — Bit 7 of the Status Register (SR) reports the Counter Underflow Status. This underflow (UF) bit is set to 1 when the counter decrements past $0000. When this bit is set, the $\overline{IRQ}$ output will be asserted if the Interrupt Enable bit in the CMCR is set to a 1. The status of the Port A Interrupt Flag (IRQA) and Port B Interrupt Flag (IRQB) are reported in bits 6 and 5, respectively, in addition to being reported in the ISCA and ISCB registers.

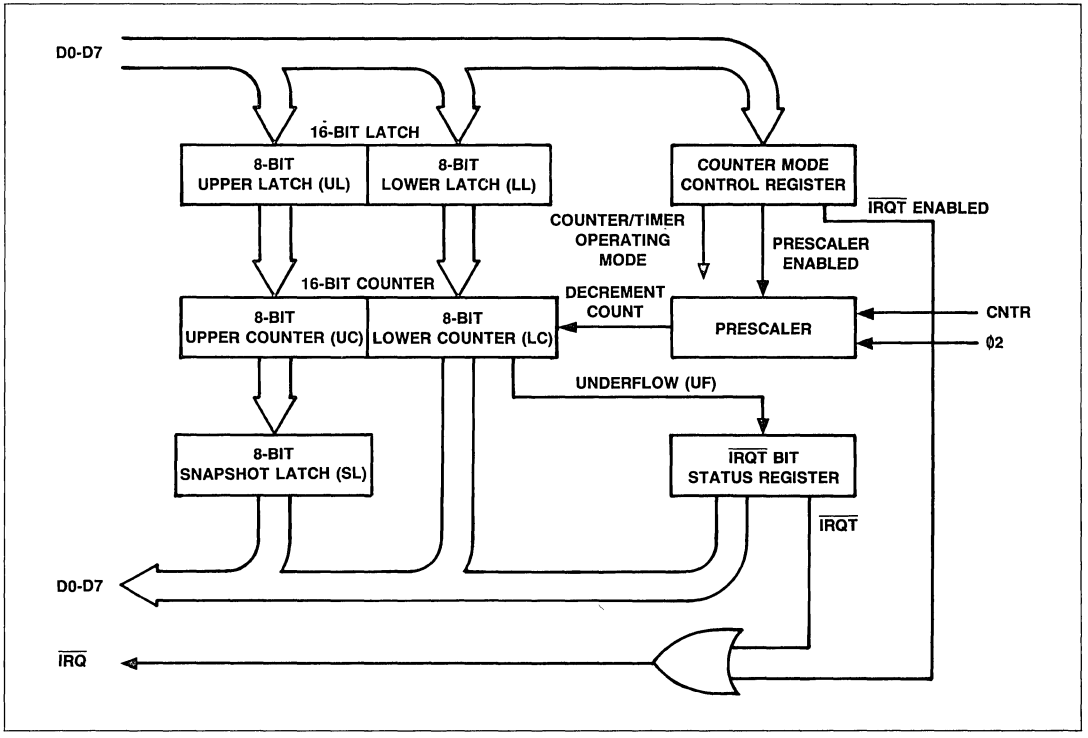


Figure 4. Counter/Timer

CA2 INPUT MODE (BIT 5 = 0) **CONTROL REGISTER A (CRA)**

7	6	5	4	3	2	1	0
IRQA1 FLAG	IRQA2 FLAG	CA2 INPUT MODE SELECT (=0)	IRQA2 POSITIVE TRANSITION	$\overline{\text{IRQA}}$ ENABLE FOR IRQA2	ORA SELECT	IRQA1 POSITIVE TRANSITION	$\overline{\text{IRQA}}$ ENABLE FOR IRQA1
			$\overline{\text{IRQA}}$/IRQA2 CONTROL			$\overline{\text{IRQA}}$/IRQA1 CONTROL	

CA2 OUTPUT MODE (BIT 5 = 1)

7	6	5	4	3	2	1	0
IRQA1 FLAG	0	CA2 OUTPUT MODE SELECT (=1)	CA2 OUTPUT CONTROL	CA2 RESTORE CONTROL	ORA SELECT	IRQA1 POSITIVE TRANSITION	$\overline{\text{IRQA}}$ ENABLE FOR IRQA1
			CA2 CONTROL			$\overline{\text{IRQA}}$/IRQA1 CONTROL	

CA2 INPUT OR OUTPUT MODE (BIT 5 = 0 or 1)

Bit 7 **IRQA1 FLAG**
1 A transition has occurred on CA1 that satisfies the bit 1 IRQA1 transition polarity criteria. This bit is cleared by a read of Output Register A or by $\overline{\text{RES}}$.
0 No transition has occurred on CA1 that satisfies the bit 1 IRQA1 transition polarity criteria.

Bit 2 **OUTPUT REGISTER A SELECT**
1 Select Output Register A.
0 Select Data Direction Register A.

Bit 1 **IRQA1 POSITIVE TRANSITION**
1 Set IRQA1 Flag (bit 7) on a positive (low-to-high) transition of CA1.
0 Set IRQA1 Flag (bit 7) on a negative (high-to-low) transition of CA1.

Bit 0 **$\overline{\text{IRQA}}$ ENABLE FOR IRQA1**
1 Enable assertion of $\overline{\text{IRQA}}$ when IRQA1 Flag (bit 7) is set.
0 Disable assertion of $\overline{\text{IRQA}}$ when IRQA1 Flag (bit 7) is set.

CA2 INPUT MODE (BIT 5 = 0)

Bit 6 **IRQA2 FLAG**
1 A transition has occurred on CA2 that satisfies the bit 4 IRQA2 transition polarity criteria. This flag is cleared by a read of Output Register A or by $\overline{\text{RES}}$.
0 No transition has occurred on CA2 that satisfies the bit 4 IRQA2 transition polarity criteria.

Bit 5 **CA2 MODE SELECT**
0 Select CA2 Input Mode.

Bit 4 **IRQA2 POSITIVE TRANSITION**
1 Set IRQA2 Flag (bit 6) on a positive (low-to-high) transition of CA2.
0 Set IRQA2 Flag (bit 6) on a negative (high-to-low) transition of CA2.

Bit 3 **$\overline{\text{IRQA}}$ ENABLE FOR IRQA2**
1 Enable assertion of $\overline{\text{IRQA}}$ when IRQA2 Flag (bit 6) is set.
0 Disable assertion of $\overline{\text{IRQA}}$ when IRQA2 Flag (bit 6) is set.

CA2 OUTPUT MODE (BIT 5 = 1)

Bit 6 **NOT USED**
0 Always zero.

Bit 5 **CA2 MODE SELECT**
1 Select CA2 Output Mode.

Bit 4 **CA2 OUTPUT CONTROL**
1 CA2 goes low when a zero is written into CRA bit 3. CA2 goes high when a one is written into CRA bit 3.
0 CA2 goes low on the first negative (high-to-low) $\phi 2$ clock transition following a read of Output Register A. CA2 returns high as specified by bit 3.

Bit 3 **CA2 READ STROBE RESTORE CONTROL (BIT 4 = 0)**
1 CA2 returns high on the next $\phi 2$ clock negative transition following a read of Output Register A.
0 CA2 returns high on the next active CA1 transition following a read of Output Register A as specified by bit 1.

Figure 5. Summary of Control Lines Operation (1 of 2)

CB2 INPUT MODE (BIT 5 = 0) CONTROL REGISTER B (CRB)

7	6	5	4	3	2	1	0
IRQB1 FLAG	IRQB2 FLAG	CB2 INPUT MODE SELECT (=0)	IRQB2 POSITIVE TRANSITION	$\overline{\text{IRQB}}$ ENABLE FOR IRQB2	ORB SELECT	IRQB1 POSITIVE TRANSITION	$\overline{\text{IRQB}}$ ENABLE FOR IRQB1
			$\overline{\text{IRQB}}$/IRQB2 CONTROL			$\overline{\text{IRQB}}$/IRQB1 CONTROL	

CB2 OUTPUT MODE (BIT 5 = 1)

7	6	5	4	3	2	1	0
IRQB1 FLAG	0	CB2 OUTPUT MODE SELECT (=1)	CB2 OUTPUT CONTROL	CB2 RESTORE CONTROL	ORB SELECT	IRQB1 POSITIVE TRANSITION	$\overline{\text{IRQB}}$ ENABLE FOR IRQB1
			CB2 CONTROL			$\overline{\text{IRQB}}$/IRQB1 CONTROL	

CB2 INPUT OR OUTPUT MODE (BIT 5 = 0 or 1)

Bit 7 IRQB1 FLAG
1 A transition has occurred on CB1 that satisfies the bit 1 IRQB1 transition polarity criteria. This bit is cleared by a read of Output Register B or by $\overline{\text{RES}}$.
0 No transition has occurred on CB1 that satisfies the bit 1 IRQB1 transition polarity criteria.

Bit 2 OUTPUT REGISTER B SELECT
1 Select Output Register B.
0 Select Data Direction Register B.

Bit 1 IRQB1 POSITIVE TRANSITION
1 Set IRQB1 Flag (bit 7) on a positive (low-to-high) transition of CB1.
0 Set IRQB1 Flag (bit 7) on a negative (high-to-low) transition of CB1.

Bit 0 $\overline{\text{IRQB}}$ ENABLE FOR IRQB1
1 Enable assertion of $\overline{\text{IRQB}}$ when IRQB1 Flag (bit 7) is set.
0 Disable assertion of $\overline{\text{IRQB}}$ when IRQB1 Flag (bit 7) is set.

CB2 INPUT MODE (BIT 5 = 0)

Bit 6 IRQB2 FLAG
1 A transition has occurred on CB2 that satisfies the bit 4 IRQB2 transition polarity criteria. This flag is cleared by a read of Output Register B or by $\overline{\text{RES}}$.
0 No transition has occurred on CB2 that satisfies the bit 4 IRQB2 transition polarity criteria.

Bit 5 CB2 MODE SELECT
0 Select CB2 Input Mode.

Bit 4 IRQB2 POSITIVE TRANSITION
1 Set IRQB2 Flag (bit 6) on a positive (low-to-high) transition of CB2.
0 Set IRQB2 Flag (bit 6) on a negative (high-to-low) transition of CB2.

Bit 3 $\overline{\text{IRQB}}$ ENABLE FOR IRQB2
1 Enable assertion of $\overline{\text{IRQB}}$ when IRQB2 Flag (bit 6) is set.
0 Disable assertion of $\overline{\text{IRQB}}$ when IRQB2 Flag (bit 6) is set.

CB2 OUTPUT MODE (BIT 5 = 1)

Bit 6 NOT USED
0 Always zero.

Bit 5 CB2 MODE SELECT
1 Select CB2 Output Mode.

Bit 4 CB2 OUTPUT CONTROL
1 CB2 goes low when a zero is written into CRB bit 3. CB2 goes high when a one is written into CRB bit 3.
0 CB2 goes low on the first negative (high-to-low) Ø2 clock transition following a write to Output Register B. CB2 returns high as specified by bit 3.

Bit 3 CB2 WRITE STROBE RESTORE CONTROL (BIT 4 = 0)
1 CB2 returns high on the next Ø2 clock negative transition following a write to Output Register B.
0 CB2 returns high on the next active CB1 transition following a write to Output Register B as specified by bit 1.

Figure 5. Summary of Control Lines Operation (2 of 2)

COUNTER/TIMER REGISTERS

COUNTER MODE CONTROL REGISTER (CMCR)

The 8-bit Counter Mode Control Register (CMCR) selects the Counter/Timer mode of operation and enables or disables both the internal $\overline{IRQT}$ and the Prescaler. The format of the CMCR is:

7	6	5	4	3	2 1 0
$\overline{IRQT}$ Enabled	0	0	Prescaler Enabled	0	Counter/Timer Mode

Bit 7 **$\overline{IRQT}$ Enabled**
0 $\overline{IRQT}$ Disabled
1 $\overline{IRQT}$ Enabled

Bits 6-5 **Not used, don't care value during write.**

Bit 4 **Prescaler Enabled**
0 Prescaler Disabled ($\div 1$)
1 Prescaler Enabled ($\div 16$)

Bit 3 **Not used, don't care value during write.**

Bits 2-0

2	1	0	Counter/Timer Mode
0	0	0	Mode 0—Disable Counter/Timer
0	0	1	Mode 1—One-Shot Interval Timer
0	1	0	Mode 2—Free-Run Interval Timer
0	1	1	Mode 3—Pulse Width Measurement
1	0	0	Mode 4—Event Counter
1	0	1	Mode 5—One-Shot Pulse Width Generation
1	1	0	Mode 6—Free-Run Pulse Generation
1	1	1	Mode 7—Retriggerable Interval Timer

The CMCR can be written into at any time without disabling or stopping the Counter/Timer. This allows the Counter/Timer mode of operation to be changed while it is still in operation. However, selecting Mode 0 disables the Counter/Timer and stops its operation. The Prescaler and the $\overline{IRQT}$ interrupt can also be enabled or disabled at any time. The CMCR is written to when the register address is 3 and R/$\overline{W}$ is low.

STATUS REGISTER (SR)

The 8-bit Status Register (SR) reports the status of three interrupt conditions: Counter underflow ($\overline{IRQT}$), Port A interrupt ($\overline{IRQA}$) and Port B interrupt ($\overline{IRQB}$). The format of the Status Register is:

7	6	5	4	3	2	1	0
UF (IRQT) Interrupt Flag	IRQA Interrupt Flag	IRQB Interrupt Flag	1	1	1	1	1

Bit 7 **Counter Underflow (UF) Interrupt Flag**
0 Counter underflow has not occurred.
1 Counter underflow has occurred.

Bit 6 **IRQA Interrupt Flag**
0 Port A interrupt has not occurred.
1 Port A interrupt has occurred.

Bit 5 **IRQB Interrupt Flag**
0 Port B interrupt has not occurred.
1 Port B interrupt has occurred.

Bit 4-0 **Not used, always read as shown in register figure.**

The Counter Underflow (UF) Interrupt, bit 7, is updated in the same clock cycle that an underflow condition occurs on the Counter/Timer. The IRQA and IRQB interrupt flags (bits 6 and 5) are updated at the rising edge of the next Ø2 clock immediately following the setting of corresponding interrupt bits in the CRA register. The IRQA Interrupt Flag is set whenever the IRQA1 or IRQA2 bit is set. The IRQB Interrupt Flag is set whenever the IRQB1 or IRQB2 bit is set. The Counter Underflow bit is cleared whenever the Snapshot Latch is read, the Upper Latch (UL) is written to at register address 0, Mode 0 is selected in the CMCR, or a $\overline{RES}$ occurs. The Status Register is read when the register address is 3 and R/$\overline{W}$ is high.

LOWER LATCH (LL)

The Lower Latch (LL) holds the least significant 8-bits of the 16-bit latch value. The LL is written from the data bus (D0–D7) when the register address is 2 and R/$\overline{W}$ is low. When the LL is loaded, the contents of the UC are copied into the Snapshot Latch (SL) without affecting the counting operation of the UC.

UPPER LATCH (UL)

The Upper Latch (UL) holds the most significant 8-bits of the 16-bit latch value. The UL is written from the data bus (D0–D7) when R/$\overline{W}$ is low and the register address is either 0 or 1. The difference in the two register address functions are:

Register Address 0

1. The UL is loaded from D0–D7.
2. The contents of the latches (UL and LL) are transferred to the counters (UC and LC, respectively).
3. The UF bit is cleared in the SR.
4. The Counter is enabled, i.e., the count in UC and LC is decremented by one upon detection of a rising edge on either Ø2 or CNTR (depending upon mode selection) as scaled by the Prescaler.

Register Address 1

1. The UL is loaded from D0–D7.
2. All other elements of the Counter/Timer are unaffected.

LOWER COUNTER (LC)

The Lower Counter (LC) holds the least significant 8-bits of the 16-bit counter.

When the LC decrements below $00, 1 is borrowed from the UC to load $FF into the LC.

The LC is read to the data bus (D0-D7) when the register address is 2 and R/$\overline{W}$ is high. When LC is read, the 8-bit contents of the UC is transferred to the Snapshot Latch without affecting the operation of the counter (i.e., the count-down continues without interruption).

UPPER COUNTER

The Upper Counter (UC) holds the most significant 8-bits of the 16-bit counter. The UC is read to the data bus (D0-D7) when the register address is 1 and R/$\overline{W}$ is high. When the UC is read, there is no other effect on the Counter/Timer operation. Counter underflow occurs when the LC borrows a 1 from an UC value of $00.

Note:

When reading the UC directly, the value read can be one count too high if the LC value is just above $00 at the start of the read since an underflow in the LC will result in decrementing the UC by one count. The Snapshot Latch should be read to obtain the UC value corresponding to the LC value.

SNAPSHOT LATCH (SL)

The Snapshot Latch holds the value of the UC corresponding to the LC value. The SL is loaded with the value of the UC when the LL is written to, or when the LC is read. The SL is read to the data bus (D0-D7) when the register address is 0 and R/$\overline{W}$ is high, without affecting the counting operation. When the SL is read, the UF in the SR is cleared. Since the SL is loaded with the value of the UC whenever the LC is read, an accurate count of the total 16-bit counter can be made without the need for further calculations to account for delays between the reading of the LC and the UC.

COUNTER/TIMER OPERATION

The Counter/Timer has eight modes of operation. The Counter/Timer is always either disabled (mode 0) or operating in one of the other seven modes as selected in the Counter Mode Control Register (CMCR).

To operate the Counter/Timer, first issue Mode 0 to stop any counting in progress due to a previously selected mode, to clear the counter underflow bit in the SR and to disable the $\overline{IRQT}$ interrupt. The order of mode selection and latch loading depends upon the desired mode. Generally, if a timer mode based on the Ø2 clock rate is to be selected, first select the mode then write the timer initialization value to the latch. Write the LL first then the UL value (to register address 0). When the UL is written, the UL and LL values are loaded into the UC and LC, respectively, and the counter is enabled. The counter then decrements one count for every positive edge (low to high) transition detected on the Ø2 or CNTR input (depending on the selected mode) as scaled by the Prescaler. In most modes, each time the counter underflows below $0000, the underflow bit is set in the SR, the counter reloads to the latch value and the down-counting continues. If the UF bit is set when the $\overline{IRQT}$ is enabled in the CMCR, the $\overline{IRQ}$ output will be asserted to the processor.

MODE 0—DISABLE COUNTER/TIMER

The Counter/Timer is disabled (all counting stops), the $\overline{IRQT}$ interrupt (bit 7 in the CMCR) is disabled, and the counter underflow (bit 7 in the SR) is cleared. Mode 0 may be selected at any time by selecting Mode 0 in the CMCR or upon $\overline{RES}$ which initializes the CMCR to $00. Selecting Mode 0 in the CMCR does not affect any data in the LL or UL, any count in the LC or UC, or any data in the SL.

MODE 1—ONE SHOT INTERVAL TIMER

The counter counts down once from the latch value at the Ø2 clock rate (as scaled by the Prescaler) and sets the UF bit in the SR upon underflow. The counter starts when data is written to the UL at register address 0, which causes the UL and LL values to be loaded into the UC and LC, respectively. When the counter decrements below $0000, the UF bit in the SR is set. The set UF bit causes $\overline{IRQ}$ to be asserted if the $\overline{IRQT}$ Enable bit is set in the CMCR. Upon decrementing below $0000, the UC and LC are automatically reset to a value of $FFFF and the counter continues down-counting. However, the UF bit in the SR will not be set again (due to the counter again decrementing through $0000) until the UL is again written at register address 0. The CNTR line is not used in this mode. Figure 6 shows the timing relationship for Mode 1 operation.

Typical Application: Can be used for an accurate time delay such as would be required to control the duration of time to have a thermal printer element activated.

MODE 2—FREE-RUN INTERVAL TIMER

The counter repetitively counts down at the Ø2 clock rate, as scaled by the Prescaler, and sets the UF bit in the SR each time the counter underflows. The counter is initialized to the UL and LL values and starts down counting at the clock rate when the UL value is written to register address 0. Each time the counter decrements below $0000, the UF bit in the SR is set, the counter is reloaded with the UL and LL value, and the count-down cycle continues. If the $\overline{IRQT}$ Enable bit is set in the CMCR, $\overline{IRQ}$ will be asserted upon each time-out. The CNTR line is not used in this mode. Figure 7 shows the timing relationship for Mode 2 operation.

Typical Application: Can be used for a timed interrupt structure when a hardware location needs updating at specific intervals, such as would be required to update a multiplexed display.

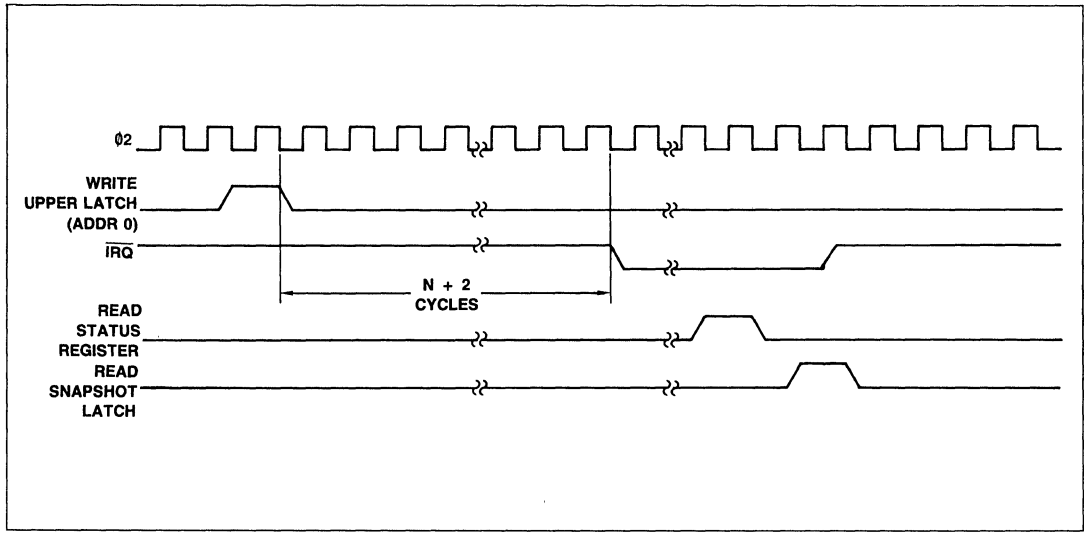


Figure 6. Mode 1—One-Shot Interval Timer Timing

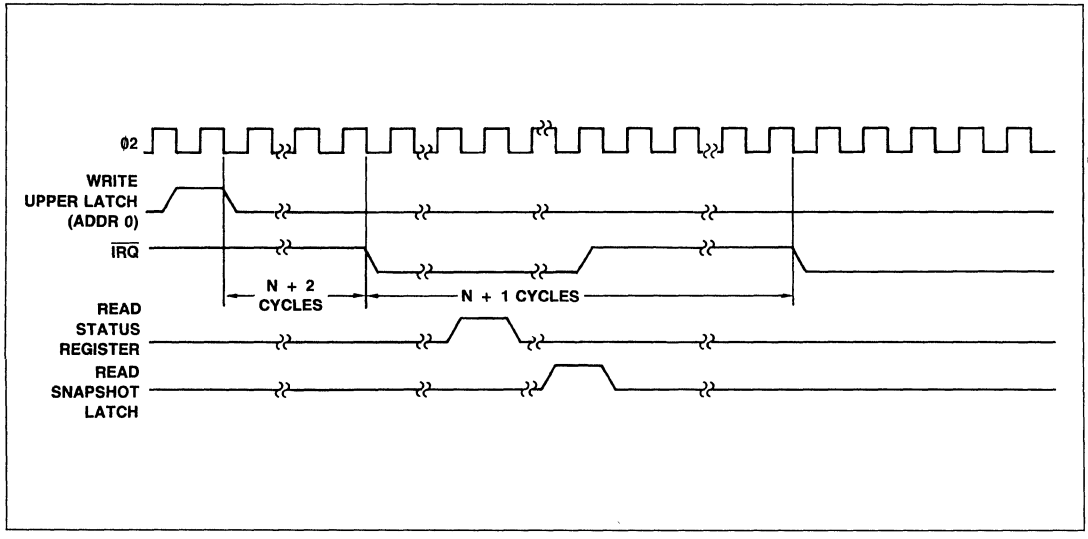


Figure 7. Mode 2—Free-Run Interval Timer Timing

MODE 3—PULSE WIDTH MEASUREMENT

The counter counts down from the latch value at the ϕ2 clock rate (scaled by the Prescaler) from the time the CNTR input goes low until CNTR goes high to provide a measurement of the CNTR low pulse duration. The counter is loaded with the value of the UL and LL upon writing UL to register address 0. The counter starts decrementing at the scaled ϕ2 clock rate when the CNTR line goes low and stops decrementing when the CNTR line returns high. If the counter decrements below $0000 before the CNTR line goes high, the UF bit in the SR is set, the counter is reloaded with the UL and LL value, and the cycle continues down until CNTR goes high. Once the CNTR line has cycled from high to low and back to high, the Counter/Timer will ignore any additional high to low transitions on the CNTR line. To reinitiate Mode 3, it is necessary to reload the UL by writing to register address 0. Figure 8 shows the timing relationships for a Mode 3 operation.

Typical Application: Can be used to measure the duration of an event from an external device. Allows an accurate measurement of the duration of a logical low pulse on the CNTR line.

MODE 4—EVENT COUNTER

CNTR is an input and the Counter/Timer counts the number of positive transitions on CNTR. The counter is initially loaded with the UL and LL value when the UL is written to register address 0. The counter then decrements one count on the falling edge of the CNTR input after a falling edge (high-to-low transition) is detected on the ϕ2 clock. The maximum rate at which this falling edge can be detected is one-half the ϕ2 clock rate. When the counter decrements below $0000, the UF bit in the SR is set, the counter is reloaded with the UL and LL value and the operation repeats. Figure 9 shows the timing relationship of a Mode 4 operation.

Typical Application: Can be used with a timed software loop to count external events (i.e., a frequency counter).

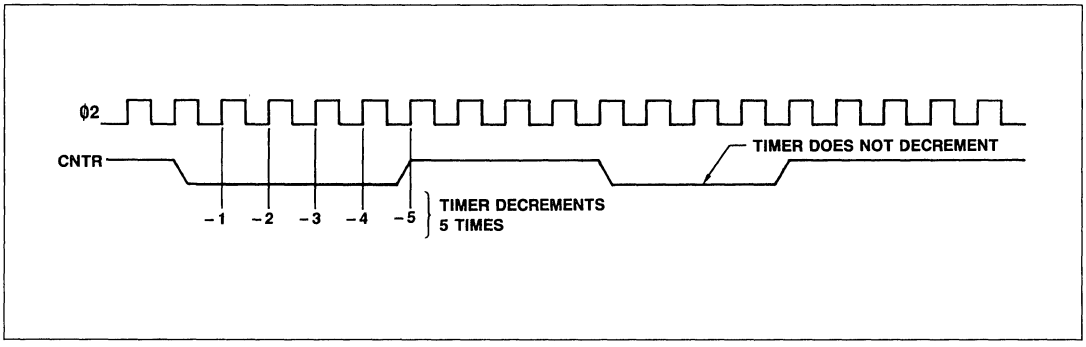


Figure 8. Mode 3—Pulse Width Measurement Timing

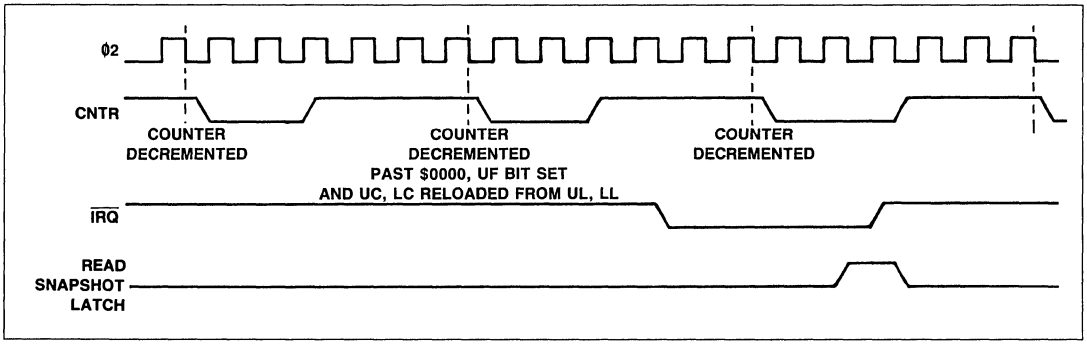


Figure 9. Mode 4—Event Counter Timing

MODE 5—ONE-SHOT PULSE WIDTH GENERATION

CNTR is an output which can be pulsed low for a programmed time interval. When this mode is selected in the CMCR, the CNTR output goes high if the UF bit is set. It goes low if the UF bit is cleared. The CNTR line then goes low when data is written to the UL at register address 0, which also starts the counter. The counter decrements from the UL and LL value at the Ø2 clock rate as scaled by the Prescaler. When the counter decrements below $0000, the CNTR output goes high, the UF bit is set in the SR, the counter is reloaded with $FFFF and the count-down continues. Figure 10 shows the timing relationship of Mode 5 operation.

Note that clearing the UF bit after it is set upon the first timeout causes CNTR to go low, in which case CNTR will again go high upon the next counter timeout.

Typical Application: Can be used to hold-off (delay) an external hardware event on an asynchronous basis such as disallowing a motor startup until certain parameters are met.

MODE 6—FREE-RUN PULSE GENERATION

CNTR is an output and the Counter/Timer can be programmed to generate a symmetrical waveform, an asymmetrical waveform, or a string of varying width pulses on CNTR. The CNTR line is forced low when data is written to the UL at register address 0 which also starts the counter. The counter decrements at the Ø2 clock rate as scaled by the Prescaler. When the counter decrements below $0000, CNTR toggles from low to high (or high to low depending upon its initial state), the counter is reloaded with the UL and LL value and the counter continues down-counting. The UF bit in the SR is set the first time the counter decrements past $0000 and is cleared only if a new write to UL at register address 0 occurs. Figure 11 shows the timing relationship of a Mode 6 operation.

This mode can be used to generate an asymmetrical waveform by toggling the UL and LL with the CNTR high and low times. Immediately after starting the counter with the first CNTR low time, load the LL and UL (by writing to register address 1, which does not restart the counter) with the CNTR high time. When the first counter underflow occurs, the counter loads the new latch value (i.e., the CNTR high time) into the counter and continues counting. During the $\overline{IRQ}$ interrupt processing resulting from the first counter time-out, load the LL and UL (at register address 1) with the original CNTR low time. Continue to alternate loading of the high and low time latch values during the interrupt processing for the duration of the mode.

Typical Application: Can be used to supply external circuitry with a software variable clock based upon the system Ø2 clock (e.g., a tone generator for audio feedback).

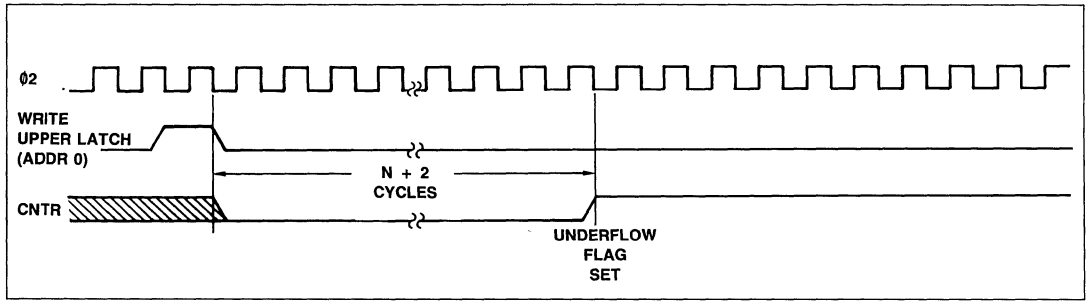


Figure 10. Mode 5—One-Shot Pulse Width Generation Timing

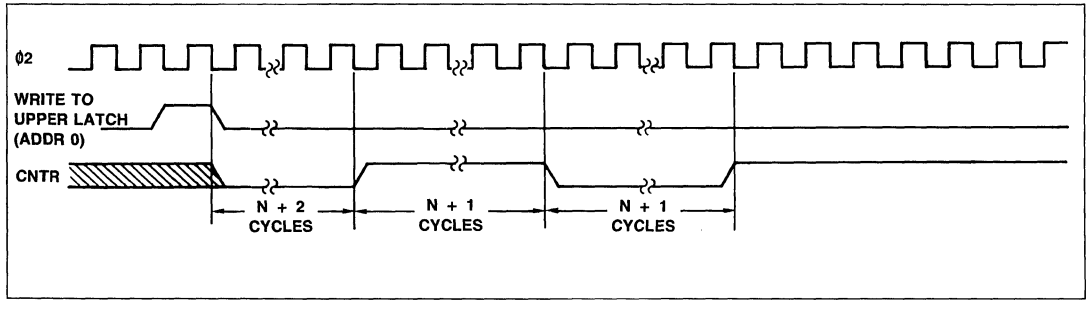


Figure 11. Mode 6—Free-Run Pulse Generation Timing

MODE 7—RETRIGGERABLE INTERVAL TIMER

The Counter/Timer operates as a timer which is retriggered, i.e., reinitialized to its starting value, upon detection of a negative transition on the CNTR input. The counter is initially loaded with the UL and LL value when the UL is written to register address 0. The counter starts decrementing at the Ø2 clock rate (as scaled by the Prescaler) when a falling edge (high to low transition) is detected on CNTR. The counter is reinitialized to the UL and LL value whenever a falling edge is subsequently detected on CNTR. If the counter decrements past $0000 before the falling edge is detected, the UF bit is set in the SR, the counter is initialized to the UL and LL value and the count-down continues.

Typical Application: Can be used to monitor signals that should be periodic and can interrupt the processor if the signal being monitored does not occur within a specified time frame; such as a synchronous motor that has fallen out of synchronization.

PRESCALER

The Counter/Timer operates in either the divide by one or divide by sixteen mode. In the divide by one mode, the counter holds from 1 to 65,535 counts. The counter capacity is therefore 1 μs to 65,535 μs at 1 MHz Ø2 clock rate or 0.25 μs to 16,383 μs at a 4 MHz Ø2 clock rate. Timer intervals greater than the maximum counter value can be easily measured by counting underflow flags or $\overline{IRQ}$ interrupt requests.

The divide by sixteen prescaler can be enabled to extend the timing interval by 16. This provides timing from 1048.56 ms (1 MHz) to 260.21 ms (4 MHz). The prescaler clocks the Counter/Timer at the Ø2 clock rate divided by sixteen, except for Mode 4. In Mode 4, sixteen positive CNTR edges must occur to decrement the Counter/Timer by one count.

INITIALIZING THE COUNTER/TIMER

The following program segment is one suggested technique for initializing the Counter/Timer:

```
;Data Definition
SL      = $XXX0     ;Snapshot Latch
UC      = $XXX1     ;Upper Counter
LC      = $XXX2     ;Lower Counter
SR      = $XXX3     ;Status Register
ULEC    = $XXX0     ;Upper Latch and Enable Counter
UL      = $XXX1     ;Upper Latch
LL      = $XXX2     ;Lower Latch
CMCR    = $XXX3     ;Counter Mode Control Register

;Program
LDA     #$mode0     ;disable Counter/Timer
STA     CMCR        ;write to mode register
LDA     #$mode      ;select mode and Prescaler and
                      IRQT enable/disable
STA     CMCR        ;write to mode register
LDA     #$lovalue   ;lower latch value
STA     LL          ;write to lower latch
LDA     #$hivalue   ;upper latch value
STA     ULEC        ;write to upper latch
                    ;clear underflow flag, and enable
                      counter
```

The following instructions change the mode while the Counter/Timer is in operation:

```
LDA     #$mode      ;select desired mode, except
                      mode 0
STA     CMCR        ;write to mode register
```

The change of mode operation will take effect immediately. Thus, the Free-Run Internal Timer mode (Mode 2) could be systematically stopped by changing to the One-Shot Interval Timer mode (Mode 1). The Counter/Timer will then halt operation when the underflow condition occurs. This technique can also be used to enable or disable $\overline{IRQ}$ during program execution.

READING THE COUNTER/TIMER

To service an interrupt request, the following sequence can be used:

```
BIT     $status     ;get underflow flag
BNE     error       ;check if flag is set
LDA     $LC         ;get low counter value for overflow
LDX     $SL         ;get high counter value for overflow
                    ;underflow flag is cleared
```

By reading the LC and SL, it is possible to determine the amount of time between the interrupt request and servicing the interrupt.

To read a timer value at any time, the suggested technique is as follows:

```
LDA     $LC         ;get low counter value
                    ;upper counter transferred to
                      snapshot
        .
        .           ;any miscellaneous code to store
        .             value if desired
LDA     $SL         ;get high counter value
```

READ/WRITE TIMING CHARACTERISTICS OF PIAT

Figure 13 is a timing diagram for the R65C24 PIAT during a Read operation (input mode). Figure 14 is a timing diagram for the PIAT during a Write operation (output mode).

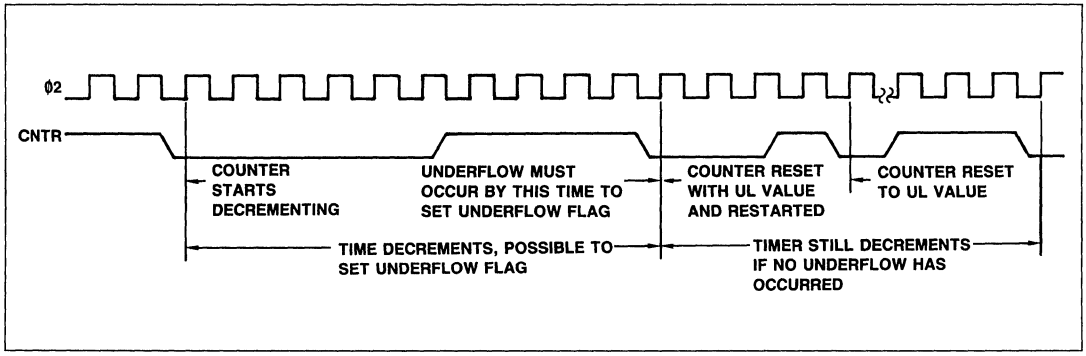


Figure 12. Mode 7—Retriggerable Interval Timer Timing

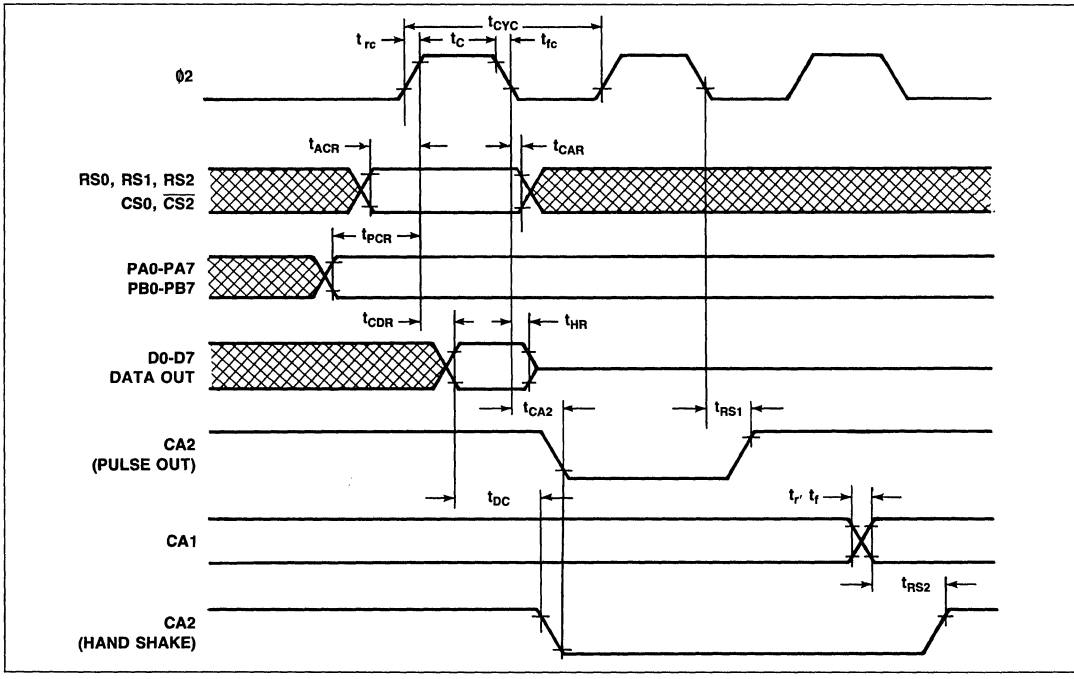


Figure 13. Read Timing Diagram

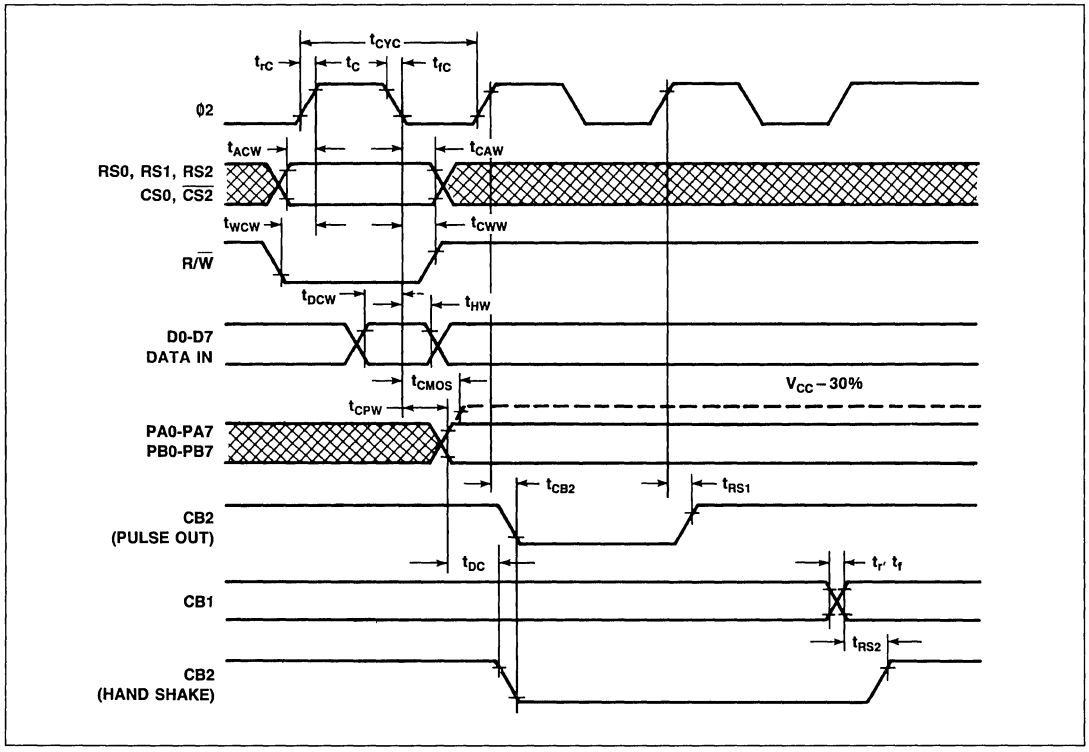


Figure 14. Write Timing Diagram

READING THE PERIPHERAL A I/O PORT

Performing a Read operation with RS1 = 0, RS0 = 0 and the Data Direction Register Access Control bit (CRA-2) = 1, directly transfers the data on the Peripheral A I/O lines to the data bus. In this situation, the data bus will contain both the input and output data. The processor must be programmed to recognize and interpret only those bits which are important to the particular peripheral operation being performed.

Since the processor always reads the Peripheral A I/O port pins instead of the actual Peripheral Output Register (ORA), it is possible for the data read by the processor to differ from the contents of the Peripheral Output Register for an output line. This is true when the I/O pin is not allowed to go to a full +2.4 Vdc when the Peripheral Output register contains a logic 1. In this case, the processor will read a 0 from the Peripheral A pin, even though the corresponding bit in the Peripheral Output register is a 1.

READING THE PERIPHERAL B I/O PORT

Reading the Peripheral B I/O port yields a combination of input and output data in a manner similar to the Peripheral A port. However, data is read directly from the Peripheral B Output Register (ORB) for those lines programmed to act as outputs. It is therefore possible to load down the Peripheral B Output lines without causing incorrect data to be transferred back to the processor on a Read operation.

SWITCHING CHARACTERISTICS

(V_{CC} = 5.0 Vdc ±5%, V_{SS} = 0, T_A = T_L to T_H, unless otherwise noted)

BUS TIMING

Parameter	Symbol	1 MHz		2 MHz		3 MHz		4 MHz		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Ø2 Cycle	t_{CYC}	1.0	—	0.5	—	0.33	—	0.25	—	μs
Ø2 Pulse Width	t_C	450	—	220	—	160	—	110	—	ns
Ø2 Rise and Fall Time	t_{rc}, t_{fc}	—	25	—	15	—	12	—	10	ns
Read										
Address Set-Up Time	t_{ACR}	140	—	70	—	53	—	35	—	ns
Address Hold Time	t_{CAR}	0	—	0	—	0	—	0	—	ns
Peripheral Data Set-Up Time	t_{PCR}	300	—	150	—	110	—	75	—	ns
Data Bus Delay Time	t_{CDR}	—	335	—	145	—	105	—	85	ns
Data Bus Hold Time	t_{HR}	20	—	20	—	20	—	20	—	ns
Write										
Address Set-Up Time	t_{ACW}	140	—	70	—	53	—	35	—	ns
Address Hold Time	t_{CAW}	0	—	0	—	0	—	0	—	ns
R/$\overline{W}$ Set-Up Time	t_{WCW}	180	—	90	—	67	—	45	—	ns
R/$\overline{W}$ Hold Time	t_{CWW}	0	—	0	—	0	—	0	—	ns
Data Bus Set-Up Time	t_{DCW}	180	—	90	—	67	—	45	—	ns
Data Bus Hold Time	t_{HW}	10	—	10	—	10	—	10	—	ns
Peripheral Data Delay Time	t_{CPW}	—	1.0	—	0.5	—	0.5	—	0.5	μs
Peripheral Data Delay Time to CMOS Level	t_{CMOS}	—	2.0	—	1.0	—	0.7	—	0.5	μs

PERIPHERAL INTERFACE TIMING

Peripheral Data Set-Up	t_{PCR}	300	—	150	—	110	—	75	—	ns
Ø2 Low to CA2 Low Delay	t_{CA2}	—	1.0	—	0.5	—	0.5	—	0.5	μs
Ø2 Low to CA2 High Delay	t_{RS1}	—	1.0	—	0.5	—	0.5	—	0.5	μs
Ø2 Low to CNTR Low/High Delay	t_{CNTR}	—	1.0	—	0.5	—	0.5	—	0.5	μs
CA1 Active to CA2 High Delay	t_{RS2}	—	2.0	—	1.0	—	1.0	—	1.0	μs
Ø2 High to CB2 Low Delay	t_{CB2}	—	1.0	—	0.5	—	0.5	—	0.5	μs
Peripheral Data Valid to CB2 Low Delay	t_{DC}	0	1.5	0	0.75	0	0.5	0	0.37	μs
Ø2 High to CB2 High Delay	t_{RS1}	—	1.0	—	0.5	—	0.5	—	0.5	μs
CB1 Active to CB2 High Delay	t_{RS2}	—	2.0	—	1.0	—	0.67	—	0.5	μs
CA1, CA2, CB1 and CB2 Input Rise and Fall Time	t_r, t_f	—	1.0	—	1.0	—	1.0	—	1.0	μs

NOTE: Timing measurements are referenced to and from a low voltage of 0.8 Vdc and a high voltage of 2.0 Vdc.

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to +7.0	Vdc
Input Voltage	V_{IN}	−0.3 to V_{CC} +0.3	Vdc
Output Voltage	V_{OUT}	−0.3 to V_{CC} +0.3	Vdc
Operating Temperature Range Commercial Industrial	T_A	 0 to +70 −40 to +85	°C
Storage Temperature	T_{STG}	−55 to +150	°C

*NOTE: Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in other sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING CONDITIONS

Parameter	Symbol	Value
Supply Voltage	V_{CC}	5V ±5%
Temperature Range Commercial Industrial	T_A	T_L to T_H 0°C to 70°C −40°C to +85°C

ELECTRICAL CHARACTERISTICS

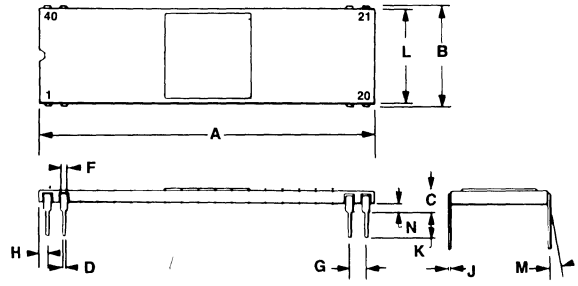
(V_{CC} = 5.0 Vdc ±5%, V_{SS} = 0, T_A = T_L to T_H, unless otherwise noted)

Parameter	Symbol	Min.	Typ.[3]	Max.	Unit[2]	Test Conditions
Input High Voltage All except R/W, CS2 R/W, CS2	V_{IH}	 +2.0 +2.4	 — —	 V_{CC} V_{CC}	V	
Input Low Voltage	V_{IL}	−0.3	—	+0.8	V	
Input Leakage Current R/W, RES, RS0, RS1, CS0, CS2, CA1, CB1, ∅2 RS2	I_{IN}	—	 ±1 ±1	 ±2.5 ±10	μA	V_{IN} = 0V to V_{CC} V_{CC} = 5.25V
Input Leakage Current for Three-State Off D0–D7, PB0–PB7, CB2	I_{TSI}	—	±2	±10	μA	V_{IN} = 0.4V to 2.4V V_{CC} = 5.25V
Input High Current PA0–PA7, CA2	I_{IH}	−200	−400	—	μA	V_{IH} = 2.0V
Input Low Current PA0–PA7, CA2	I_{IL}	—	−2	−3.2	mA	V_{IL} = 0.8V
Output High Voltage Logic PB0–PB7, CB2 (Darlington Drive)	V_{OH}	 2.4 1.5	 — —	 — —	V	V_{CC} = 4.75V I_{LOAD}[2] = −200μA I_{LOAD}[2] = −3.2mA
Output Low Voltage PA0–PA7, CA2, PB0–PB7, CB2 D0–D7, IRQ, CNTR	V_{OL}	—	—	+0.4	V	V_{CC} = 4.75V I_{LOAD} = 3.2 mA I_{LOAD} = 1.6 mA
Output High Current (Sourcing) Logic PB0–PB7, CB2 (Darlington Drive)	I_{OH}	 −200 −3.2	 −1500 −6	 — —	 μA mA	 V_{OH} = 2.4V V_{OH} = 1.5V
Output Low Current (Sinking) PA0–PA7, PB0–PB7, CB2, CA2 D0–D7, IRQ, CNTR	I_{OL}	 3.2 1.6	 — —	 — —	 mA mA	V_{OL} = 0.4V
Output Leakage Current (Off State) IRQ	I_{OFF}	—	1	±10	μA	V_{OH} = 2.4V V_{CC} = 5.25V
Power Dissipation	P_D	—	7	10	mW/MHz	
Input Capacitance D0–D7, PA0–PA7, PB0–PB7, CA2, CB2 R/W, RES, RS0, RS1, RS2, CS0, CS2, CNTR, CA1, CB1, ∅2	C_{IN}	 — — —	 — — —	 10 7 20	 pF pF pF	V_{CC} = 5.0V V_{IN} = 0V f = 2 MHz T_A = 25°C
Output Capacitance	C_{OUT}	—	—	10	pF	

Notes:
1. All units are direct current (dc) except capacitance.
2. Negative sign indicates outward current flow, positive indicates inward flow.
3. Typical values are shown for V_{CC} = 5.0V and T_A = 25°C.

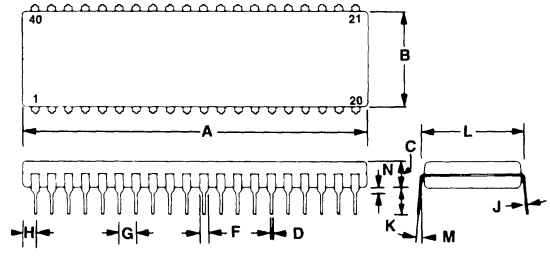
PACKAGE DIMENSIONS

40-PIN CERAMIC DIP



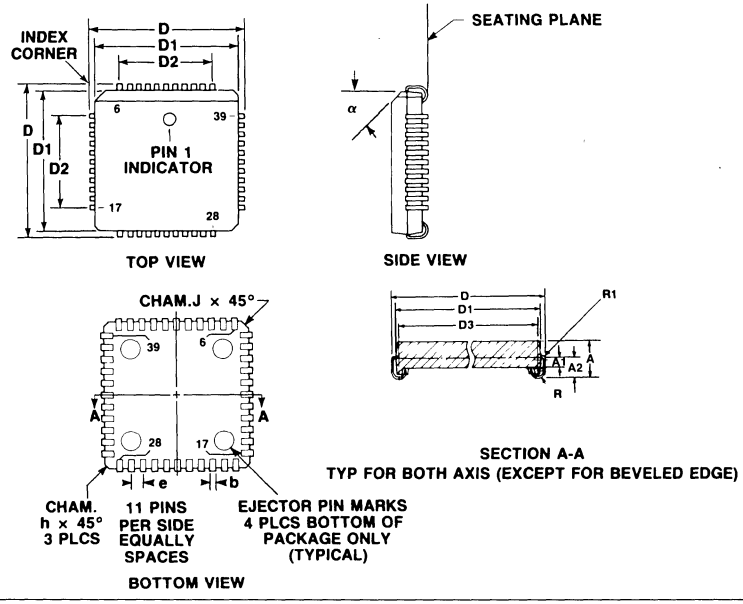
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	50 29	51 31	1 980	2.020
B	15 11	15.88	0.595	0 625
C	2.54	4 19	0 100	0 165
D	0 38	0.53	0 015	0 021
F	0 76	1 27	0 030	0 050
G	2.54 BSC		0.100 BSC	
H	0 76	1.78	0.030	0.070
J	0.20	0.33	0 008	0.013
K	2.54	4.19	0 100	0 165
L	14 60	15.37	0.575	0.605
M	0°	10°	0°	10°
N	0 51	1.52	0.020	0 060

40-PIN PLASTIC DIP



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	51.82	52 32	2 040	2 060
B	13.46	13 97	0 530	0.550
C	3 56	5 08	0.140	0.200
D	0.38	0 53	0 015	0.021
F	1 02	1 52	0.040	0 060
G	2.54 BSC		0 100 BSC	
H	1.65	2.16	0.065	0 085
J	0 20	0.30	0.008	0 012
K	3.30	4.32	0.130	0.170
L	15 24 BSC		0 600 BSC	
M	7°	10°	7°	10°
N	0.51	1.02	0.020	0 040

44-PIN PLASTIC LEADED CHIP CARRIER (PLCC)



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.14	4 39	0.163	0.173
A1	1 37	1 47	0.054	0 058
A2	2 31	2 46	0 091	0 097
b	0 457 TYP		0.018 TYP	
D	17.45	17.60	0 687	0 693
D1	16 46	16 56	0.648	0.652
D2	12.62	12.78	0 497	0 503
D3	15 75 REF		0 620 REF	
e	1 27 BSC		0 050 BSC	
h	1.15 TYP		0.045 TYP	
J	0.25 TYP		0 010 TYP	
α	45° TYP		45° TYP	
R	0 89 TYP		0 035 TYP	
R1	0 25 TYP		0.010 TYP	

Rockwell

R65C51
Asynchronous Communications Interface Adapter (ACIA)

1

DESCRIPTION

The Rockwell CMOS R65C51 Asynchronous Communications Interface Adapter (ACIA) provides an easily implemented, program controlled interface between 8-bit microprocessor-based systems and serial communication data sets and modems.

The ACIA has an internal baud rate generator. This feature eliminates the need for multiple component support circuits, a crystal being the only other part required. The Transmitter baud rate can be selected under program control to be any one of 15 different rates from 50 to 19,200 baud, or $^1/_{16}$ times an external clock rate. The Receiver baud rate may be selected under program control to be either the Transmitter rate, or at $^1/_{16}$ times an external clock rate. The ACIA has programmable word lengths of 5, 6, 7, or 8 bits; even, odd, or no parity; 1, $1^1/_2$, or 2 stop bits.

The ACIA is designed for maximum programmed control from the microprocessor (MPU), to simplify hardware implementation. Three separate registers permit the MPU to easily select the R65C51's operating modes and data checking parameters and determine operational status.

FEATURES

- Low power CMOS N-well silicon gate technology
- Replacement for NMOS R6551 ACIA
- Full duplex operation with buffered receiver and transmitter
- Data set/modem control functions
- Internal baud rate generator with 15 programmable baud rates (50 to 19,200)
- Program-selectable internally or externally controlled receiver rate
- Programmable word lengths, number of stop bits, and parity bit generation and detection
- Programmable interrupt control
- Program reset
- Program-selectable serial echo mode
- Two chip selects
- 1 or 2 MHz operation
- 5.0 Vdc ±5% supply requirements
- Wide range of packages available
  - — 28-pin ceramic or plastic DIP
  - — 28-pin plastic leaded chip carrier (PLCC)
- Full TTL compatibility
- Compatible with R6500, R6500/* and R65C00 microprocessors

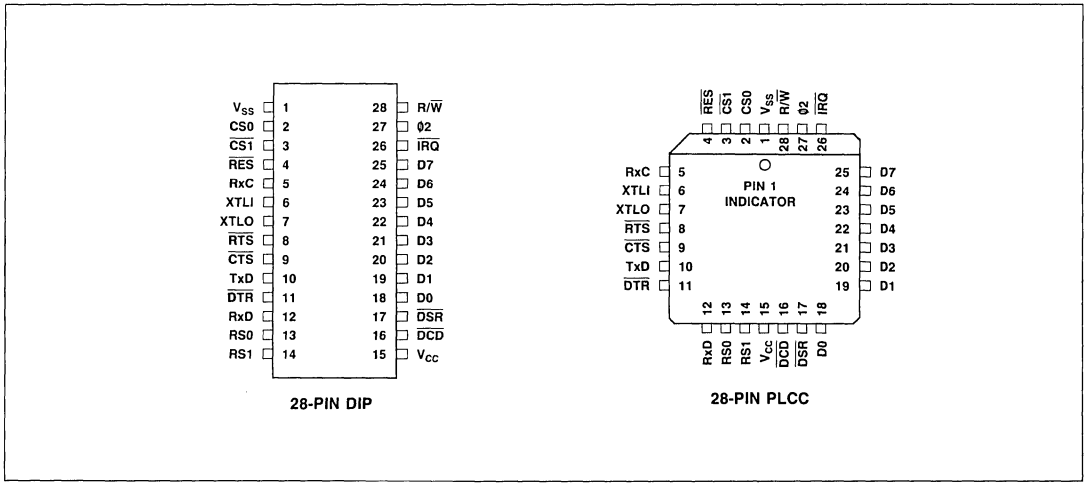
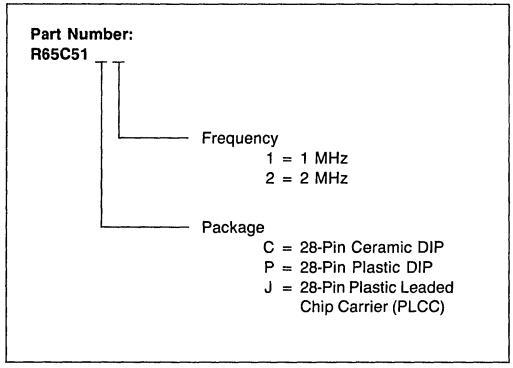


Figure 1. R65C51 ACIA Pin Assignments

ORDERING INFORMATION



INTERFACE SIGNALS

Figure 1 (front page) shows the R65C51 ACIA pin assignments and Figure 2 groups the signals by functional interface.

MICROPROCESSOR INTERFACE

Reset ($\overline{RES}$)

During system initialization, a low on the $\overline{RES}$ input causes a hardware Reset to occur. Upon Reset, the Command Register and the Control Register are cleared (all bits set to 0). The Status Register is cleared with the exception of the indications of Data Set Ready and Data Carrier Detect, which are externally controlled by the $\overline{DSR}$ and $\overline{DCD}$ lines, and the Transmitter Empty bit, which is set. $\overline{RES}$ must be held low for one $\phi 2$ clock cycle for a reset to occur.

Input Clock ($\phi 2$)

The input clock is the system $\phi 2$ clock and clocks all data transfers between the system microprocessor and the ACIA.

Read/Write (R/$\overline{W}$)

The R/$\overline{W}$ input, generated by the microprocessor controls the direction of data transfers. A high on the R/$\overline{W}$ pin allows the processor to read the data supplied by the ACIA, a low allows a write to the ACIA.

Interrupt Request ($\overline{IRQ}$)

The $\overline{IRQ}$ pin is an interrupt output from the interrupt control logic. It is an open drain output, permitting several devices to be connected to the common $\overline{IRQ}$ microprocessor input. Normally a high level, $\overline{IRQ}$ goes low when an interrupt occurs.

Data Bus (D0–D7)

The eight data line (D0–D7) pins transfer data between the processor and the ACIA. These lines are bi-directional and are normally high-impedance except during Read cycles when the ACIA is selected.

Chip Selects (CS0, $\overline{CS1}$)

The two chip select inputs are normally connected to the processor address lines either directly or through decoders. The ACIA is selected when CS0 is high and $\overline{CS1}$ is low. When the ACIA is selected, the internal registers are addressed in accordance with the register select lines (RS0, RS1).

Register Selects (RS0, RS1)

The two register select lines are normally connected to the processor address lines to allow the processor to select the various ACIA internal registers. Table 1 shows the internal register select decoding.

Table 1. ACIA Register Selection

		Register Operation	
RS1	RS0	R/$\overline{W}$ = Low	R/$\overline{W}$ = High
L	L	Write Transmit Data Register	Read Receiver Data Register
L	H	Programmed Reset (Data is "Don't Care")	Read Status Register
H	L	Write Command Register	Read Command Register
H	H	Write Control Register	Read Control Register

The Command Register controls parity, receiver echo mode, transmitter interrupt control, the state of the $\overline{RTS}$ line, receiver interrupt control, and the state of the $\overline{DTR}$ line.

The Control Register controls the number of stop bits, word length, receiver clock source, and baud rate.

The Status Register indicates the states of the $\overline{IRQ}$, $\overline{DSR}$, and $\overline{DCD}$ lines, Transmitter and Receiver Data Registers, and Overrun, Framing, and Parity Error conditions.

The Transmitter and Receiver Data Registers are used for temporary data storage by the ACIA Transmit and Receive circuits.

Only the Command and Control registers can be both read and written. The programmed Reset operation does not cause any data transfer, but is used to clear bits 4 through 0 in the Command register and bit 2 in the Status Register. The control Register is unchanged by a programmed Reset. It should be noted that the programmed Reset is slightly different from the hardware Reset ($\overline{RES}$); refer to the register description.

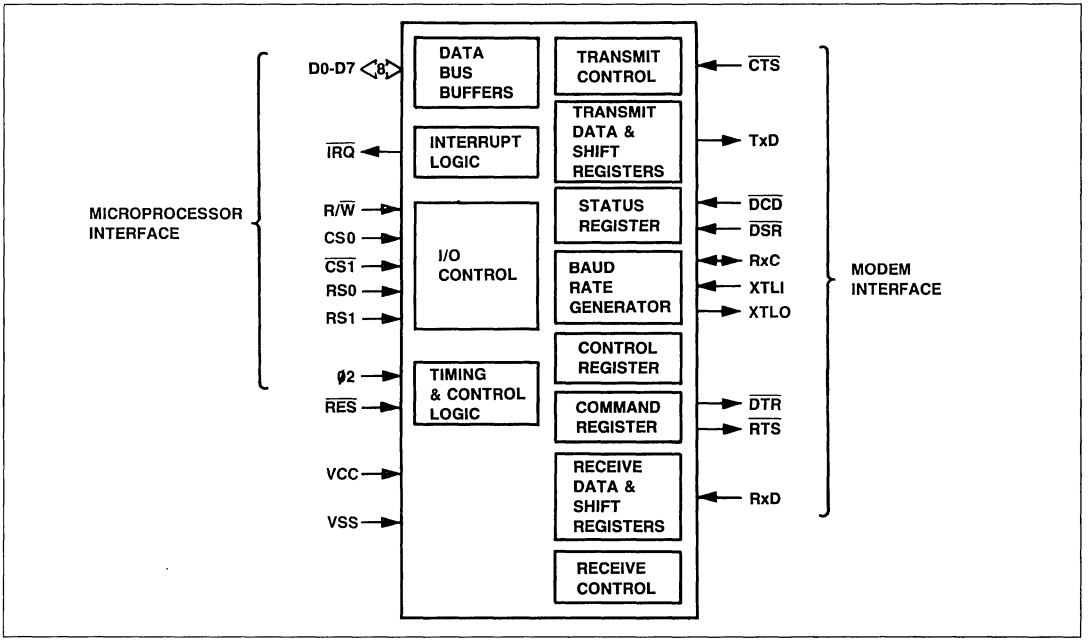


Figure 2. ACIA Interface Diagram

ACIA/MODEM INTERFACE

Crystal Pins (XTLI, XTLO)

These pins are normally directly connected to a parallel mode external crystal (1.8432 MHz) to derive the various baud rates. Note that capacitors are required from XTLI to ground and from XTLO to ground. Alternatively, an externally generated clock can drive the XTLI pin, in which case the XTLO pin must float.

Transmit Data (TxD)

The TxD output line transfers serial non-return-to-zero (NRZ) data to the modem. The least significant bit (LSB) of the Transmit Data Register is the first data bit transmitted and the rate of data transmission is determined by the baud rate selected or by an external transmitter clock. This selection is made by programming the Control Register.

Receive Data (RxD)

The RxD input line transfers serial NRZ data into the ACIA from the modem, LSB first. The receiver data rate is determined by the programmed baud rate or by an externally generated receiver clock. The selection is made by programming the Control Register.

Receive Clock (RxC)

RxC is a bi-directional pin which is either the external receiver clock input or a clock output of 16x the baud rate. The latter mode results if the internal baud rate generator is selected for receiver data clocking.

Request to Send ($\overline{RTS}$)

The $\overline{RTS}$ output pin controls the modem from the processor. The state of the $\overline{RTS}$ pin is determined by the contents of the Command Register.

Clear to Send ($\overline{CTS}$)

The $\overline{CTS}$ input pin controls the transmitter operation. The enable state is with $\overline{CTS}$ low. The transmitter is automatically disabled if $\overline{CTS}$ is high.

Data Terminal Ready ($\overline{DTR}$)

This output pin indicates the status of the ACIA to the modem. A low on $\overline{DTR}$ indicates the ACIA is enabled, a high indicates it is disabled. The processor controls this pin via bit 0 of the Command Register.

Data Set Ready ($\overline{DSR}$)

The $\overline{DSR}$ input pin indicates to the ACIA the status of the modem. A low indicates the "ready" state and a high, "not-ready."

Data Carrier Detect ($\overline{DCD}$)

The $\overline{DCD}$ input pin indicates to the ACIA the status of the carrier-detect output of the modem. A low indicates that the modem carrier signal is present and a high, that it is not.

FUNCTIONAL DESCRIPTION

A block diagram of the R65C51 ACIA is presented in Figure 3. A description of each functional element of the device follows.

DATA BUS BUFFERS

The Data Bus Buffer interfaces the system data lines to the internal data bus. The Data Bus Buffer is bi-directional. When the R/$\overline{W}$ line is low and the chip is selected, the Data Bus Buffer writes the data from the system data lines to the ACIA internal data bus. When the R/$\overline{W}$ line is high and the chip is selected, the Data Bus Buffer drives the data from the internal data bus to the system data bus.

INTERRUPT LOGIC

The Interrupt Logic will cause the $\overline{IRQ}$ line to the microprocessor to go low when conditions are met that require the attention of the microprocessor. The conditions which can cause an interrupt will set bit 7 and the appropriate bit of bits 3 through 6 in the Status Register, if enabled. Bits 5 and 6 correspond to the Data Carrier Detect ($\overline{DCD}$) logic and the Data Set Ready ($\overline{DSR}$) logic. Bits 3 and 4 correspond to the Receive Data Register full and the Transmitter Data Register empty conditions. These conditions can cause an interrupt request if enabled by the Command Register.

I/O CONTROL

The I/O Control Logic controls the selection of internal registers for a data transfer on the internal data bus and the direction of the transfer to or from the register.

The registers are selected by the Register Select (RS1, RS0) and Read/Write (R/$\overline{W}$) lines as shown in Table 1.

TIMING AND CONTROL

The Timing and Control logic controls the timing of data transfers on the internal data bus, the registers, the Data Bus Buffer, the microprocessor data bus, and the hardware reset.

Timing is controlled by the system $\phi 2$ clock input. The chip will perform data transfers to or from the microcomputer data bus during the $\phi 2$ high period when selected.

All registers will be initialized by the Timing and Control Logic when the Reset ($\overline{RES}$) line goes low. See the individual register description for the state of the registers following a hardware reset.

TRANSMITTER AND RECEIVER DATA REGISTERS

These registers are used as temporary data storage for the ACIA Transmit and Receive circuits. Both the Transmitter and Receiver are selected by a Register Select 0 (RS0) and Register Select 1 (RS1) low condition. The Read/Write (R/$\overline{W}$) line determines which actually uses the internal data bus; the Transmitter Data Register is write only and the Receiver Data Register is read only.

Bit 0 is the first bit to be transmitted from the Transmitter Data Register (least significant bit first). The higher order bits follow in order. Unused bits in this register are "don't care" bits.

The Receiver Data Register holds the first received data bit in bit 0 (least significant bit first). Unused high-order bits are "0". Parity bits are not contained in the Receiver Data Register. They are stripped off after being used for parity checking.

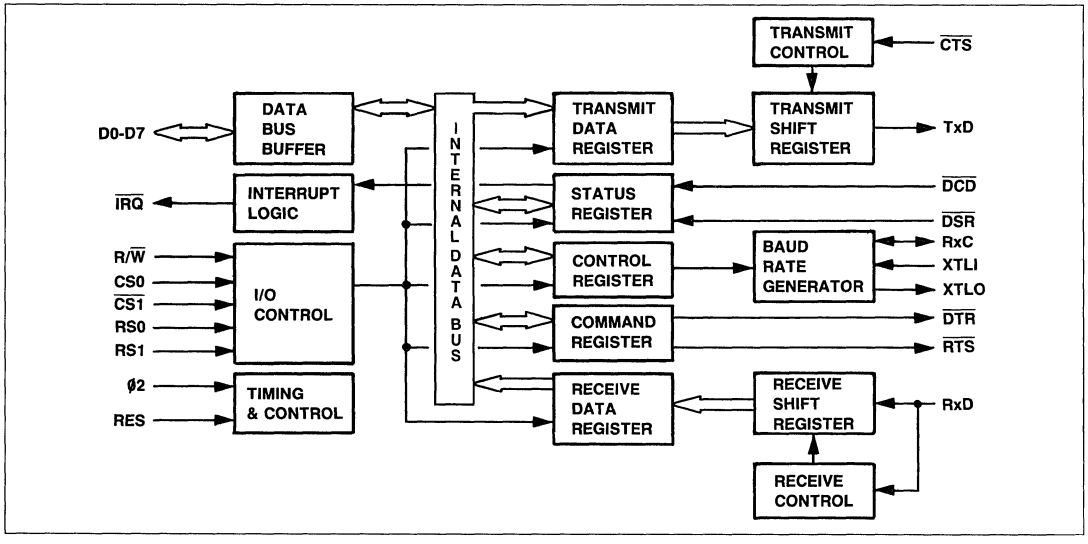


Figure 3. R65C51 ACIA Block Diagram

STATUS REGISTER

The Status Register indicates the state of interrupt conditions and other non-interrupt status information. The interrupt conditions are Data Set Ready and Data Carrier Detect transitions, Transmitter Data Register Empty and Receiver Data Register Full as reported in bits 6 through 3, respectively. If any of these bits are set, the Interrupt (IRQ) indicator (bit 7) is also set. Overrun, Framing Error, and Parity Error are also reported (bits 2 through 0, respectively).

7	6	5	4	3	2	1	0
IRQ	$\overline{DSR}$	$\overline{DCD}$	TDRE	RDRF	OVRN	FE	PE

Bit 7 Interrupt (IRQ)
0 No interrupt
1 Interrupt has occurred

Bit 6 Data Set Ready (DSR)
0 DSR low (ready)
1 DSR high (not ready)

Bit 5 Data Carrier Detect (DCD)
0 DCD low (detected)
1 DCD high (not detected)

Bit 4 Transmitter Data Register Empty
0 Not empty
1 Empty

Bit 3 Receiver Data Register Full
0 Not full
1 Full

Bit 2 Overrun*
0 No overrun
1 Overrun has occurred

Bit 1 Framing Error*
0 No framing error
1 Framing error detected

Bit 0 Parity Error*
0 No parity error
1 Parity error detected

*No interrupt occurs for these conditions

Reset Initialization

7	6	5	4	3	2	1	0	
0	—	—	1	0	0	0	0	Hardware reset
—	—	—	—	—	0	—	—	Program reset

Parity Error (Bit 0), Framing Error (Bit 1), and Overrun (Bit 2)

None of these bits causes a processor interrupt to occur, but they are normally checked at the time the Receiver Data Register is read so that the validity of the data can be verified. These bits are self clearing (i.e., they are automatically cleared after a read of the Receiver Data Register.)

Receiver Data Register Full (Bit 3)

This bit goes to a 1 when the ACIA transfers data from the Receiver Shift Register to the Receiver Data Register, and goes to a 0 (is cleared) when the processor reads the Receiver Data Register.

Transmitter Data Register Empty (Bit 4)

This bit goes to a 1 when the ACIA transfers data from the Transmitter Data Register to the Transmitter Shift Register, and goes to a 0 (is cleared) when the processor writes new data onto the Transmitter Data Register.

NOTE: There is a delay of approximately $\frac{1}{16}$ of a bit time after the TDR becomes empty/full before this flag is updated.

Data Carrier Detect (Bit 5) and Data Set Ready (Bit 6)

These bits reflect the levels of the $\overline{DCD}$ and $\overline{DSR}$ inputs to the ACIA. A 0 indicates a low level (true condition) and a 1 indicates a high level (false). Whenever either of these inputs change state, an immediate processor interrupt (IRQ) occurs, unless bit 1 of the Command Register (IRD) is set to a 1 to disable $\overline{IRQ}$. When the interrupt occurs, the status bits indicate the levels of the inputs immediately after the change of state occurred. Subsequent level changes will not affect the status bits until after the Status Register has been interrogated by the processor. At that time, another interrupt will immediately occur and the status bits will reflect the new state. These bits are not automatically cleared (or reset) by an internal operation.

Interrupt (Bit 7)

This bit goes to a 1 whenever an interrupt condition occurs and goes to a 0 (is cleared) when the Status Register is read.

CONTROL REGISTER

The Control Register selects the desired baud rate, frequency source, word length, and the number of stop bits.

7	6	5	4	3	2	1	0
SBN	WL		RCS	SBR			
	WL1	WL0		SBR3	SBR2	SBR1	SBR0

Bit 7 Stop Bit Number (SBN)

0	1 Stop bit
1	2 Stop bits
1	1½ Stop bits For WL = 5 and no parity
1	1 Stop bit For WL = 8 and parity

Bits 6-5 Word Length (WL)

6	5	No. Bits
0	0	8
0	1	7
1	0	6
1	1	5

Bit 4 Receiver Clock Source (RCS)

0	External receiver clock
1	Baud rate

Bits 3-0 Selected Baud Rate (SBR)

3	2	1	0	Baud
0	0	0	0	TxC rate ÷ 16*
0	0	0	1	50
0	0	1	0	75
0	0	1	1	109.92
0	1	0	0	134.58
0	1	0	1	150
0	1	1	0	300
0	1	1	1	600
1	0	0	0	1200
1	0	0	1	1800
1	0	1	0	2400
1	0	1	1	3600
1	1	0	0	4800
1	1	0	1	7200
1	1	1	0	9600
1	1	1	1	19,200

*XTLI is the input for the External Transmitter Clock (TxC)

Reset Initialization

7	6	5	4	3	2	1	0	
0	0	0	0	0	0	0	0	Hardware reset ($\overline{RES}$)
—	—	—	—	—	—	—	—	Program reset

Selected Baud Rate (Bits 0, 1, 2, 3)

These bits select the Transmitter baud rate, which can be at 1/16 an external transmitter clock rate or one of 15 other rates controlled by the internal baud rate generator.

If the Receiver clock uses the same baud rate as the transmitter (bit 4 = 1), then RxC becomes an output (at 16x the baud rate) and can be used to slave other circuits to the ACIA. Figure 4 shows the Transmitter and Receiver layout.

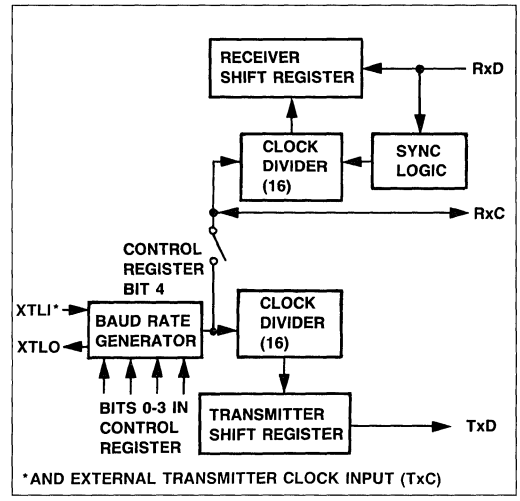


Figure 4. Transmitter/Receiver Clock Circuits

Receiver Clock Source (Bit 4)

This bit controls the clock source to the Receiver. A 0 causes the Receiver to operate at a baud rate of 1/16 the external receiver clock on pin RxC. A 1 causes the Receiver to operate at the same baud rate as is selected for the transmitter.

Word Length (Bits 5, 6)

These bits determine the word length to be used (5, 6, 7 or 8 bits).

Stop Bit Number (Bit 7)

This bit determines the number of stop bits used. A 0 always indicates one stop bit. A 1 indicates 1½ stop bits if the word length is 5 with no parity selected, 1 stop bit if the word length is 8 with parity selected, and 2 stop bits in all other configurations.

COMMAND REGISTER

The Command Register controls specific modes and functions.

7	6	5	4	3	2	1	0
PMC		PME	REM	TIC		IRD	DTR
PNC1	PNC0			TIC1	TIC0		

Bits 7-6 Parity Mode Control (PMC)

7	6	
0	0	Odd parity transmitted/received
0	1	Even parity transmitted/received
1	0	Mark parity bit transmitted Parity check disabled
1	1	Space parity bit transmitted Parity check disabled

Bit 5 Parity Mode Enabled (PME)

0	Parity mode disabled No parity bit generated Parity check disabled
1	Parity mode enabled

Bit 4 Receiver Echo Mode (REM)

0	Receiver normal mode
1	Receiver echo mode Bits 2 and 3 must also be zero for receiver echo mode, $\overline{RTS}$ will be low.

Bits 3-2 Transmitter Interrupt Control (TIC)

3	2	
0	0	$\overline{RTS}$ = High, transmitter disabled*
0	1	$\overline{RTS}$ = Low, transmit interrupt enabled
1	0	$\overline{RTS}$ = Low, transmit interrupt disabled
1	1	$\overline{RTS}$ = Low, transmit interrupt disabled, transmit break on TxD**

Bit 1 Receiver Interrupt Request Disabled (IRD)

0	$\overline{IRQ}$ enabled (receiver)
1	$\overline{IRQ}$ disabled (receiver)

Bit 0 Data Terminal Ready (DTR)

0	Data terminal not ready ($\overline{DTR}$ high)*
1	Data terminal ready ($\overline{DTR}$ low)

NOTE

*The transmitter is disabled immediately. The receiver is disabled but will first complete receiving a byte in process of being received.

**A "BREAK" is transmitted only after the end of a character stream. If the Transmitter Data Register contains a character, the "BREAK" is not transmitted.

Data Terminal Ready (Bit 0)

This bit enables all selected interrupts and controls the state of the Data Terminal Ready ($\overline{DTR}$) line. A 0 indicates the microcomputer system is not ready by setting the $\overline{DTR}$ line high. A 1 indicates the microcomputer system is ready by setting the $\overline{DTR}$ line low. $\overline{DTR}$ also enables and disables the transmitter and receiver.

Receiver Interrupt Control (Bit 1)

This bit disables the Receiver $\overline{DCD}$ and $\overline{DSR}$ from generating an interrupt when set to a 1. The Receiver $\overline{DCD}$ and $\overline{DSR}$ interrupts are enabled when this bit is set to a 0 and Bit 0 is set to a 1.

Transmitter Interrupt Control (Bits 2, 3)

These bits control the state of the Ready to Send ($\overline{RTS}$) line and the Transmitter interrupt.

Receiver Echo Mode (Bit 4)

A 1 enables the Receiver Echo Mode and a 0 disables the Receiver Echo Mode. When bit 4 is a 1 bits 2 and 3 must be 0. In the Receiver Echo Mode, the Transmitter returns each transmission received by the Receiver delayed by one-half bit time.

Parity Mode Enable (Bit 5)

This bit enables parity bit generation and checking. A 0 disables parity bit generation by the Transmitter and parity bit checking by the Receiver. A 1 bit enables generation and checking of parity bits.

Parity Mode Control (Bits 6, 7)

These bits determine the type of parity generated by the Transmitter, (even, odd, mark or space) and the type of parity check done by the Receiver (even, odd, or no check).

Reset Initialization

7	6	5	4	3	2	1	0	
0	0	0	0	0	0	0	0	Hardware reset ($\overline{RES}$)
—	—	—	0	0	0	0	0	Program reset

STATUS REGISTER OPERATION

Because of the special functions of the various status bits, there is a suggested sequence for checking them. When an interrupt occurs, the ACIA should be interrogated, as follows:

1. Read Status Register

   This operation automatically clears Bit 7 ($\overline{IRQ}$). Subsequent transitions on $\overline{DSR}$ and $\overline{DCD}$ will cause another interrupt.

2. Check $\overline{IRQ}$ (Bit 7) in the data read from the Status Register

   If not set, the interrupt source is not the ACIA.

3. Check $\overline{DCD}$ and $\overline{DSR}$

   These must be compared to their previous levels, which must have been saved by the processor. If they are both 0 (modem "on-line") and they are unchanged, then the remaining bits must be checked.

4. Check RDRF (Bit 3)

   Check for Receiver Data Register Full.

5. Check Parity, Overrun, and Framing Error (Bits 0–2) if the Receiver Data Register is full.

6. Check TDRE (Bit 4)

   Check for Transmitter Data Register Empty.

PROGRAM RESET OPERATION

A program Reset occurs when the processor performs a write operation to the ACIA with RS0 low and RS1 high. The program Reset operates somewhat differently from the hardware Reset ($\overline{RES}$ pin) and is described as follows:

1. Internal registers are not completely cleared. Check register formats for the effect of a program Reset on internal registers.

2. The $\overline{DTR}$ line goes high immediately.

3. Receiver and transmitter interrupts are disabled immediately. If $\overline{IRQ}$ is low when the reset occurs,it stays low until serviced, unless interrupt was caused by $\overline{DCD}$ or $\overline{DSR}$ transition.

4. $\overline{DCD}$ and $\overline{DSR}$ interrupts are disabled immediately. If $\overline{IRQ}$ is low and was caused by $\overline{DCD}$ or $\overline{DSR}$, then it goes high, also $\overline{DCD}$ and $\overline{DSR}$ status bits subsequently will follow the input lines, although no interrupt will occur.

5. Overrun cleared, if set.

TRANSMITTER AND RECEIVER OPERATION

Continuous Data Transmit

In the normal operating mode, the interrupt request output ($\overline{IRQ}$) signals when the ACIA is ready to accept the next data word to be transmitted. This interrupt occurs at the beginning of the Start Bit. When the processor reads the Status Register of the ACIA, the interrupt is cleared.

The processor must then identify that the Transmit Data Register is ready to be loaded and must then load it with the next data word. This must occur before the end of the Stop Bit, otherwise a continuous "MARK" will be transmitted. Figure 5 shows the continuous Data Transmit timing relationship.

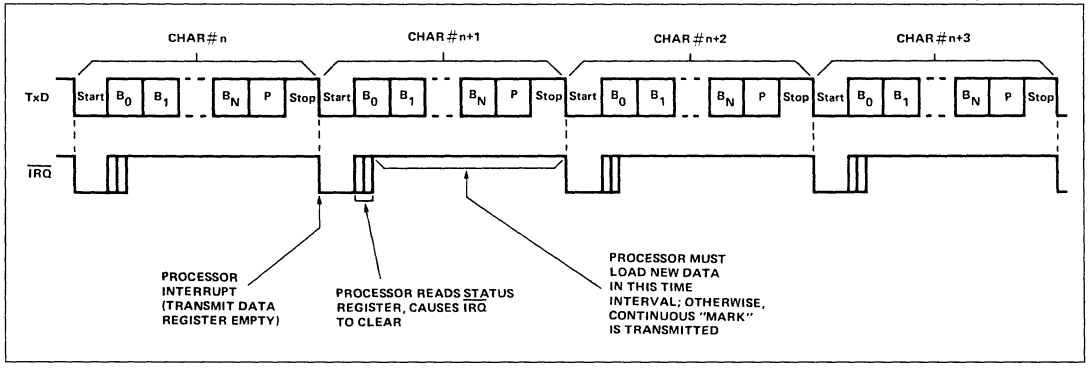


Figure 5. Continuous Data Transmit

Continuous Data Receive

Similar to the Continuous Data Transmit case, the normal operation of this mode is to assert $\overline{IRQ}$ when the ACIA has received a full data word. This occurs at about $^{9}/_{16}$ point through the Stop Bit. The processor must read the Status Register and read the data word before the next interrupt, otherwise the Overrun condition occurs. Figure 6 shows the continuous Data Receive Timing Relationship.

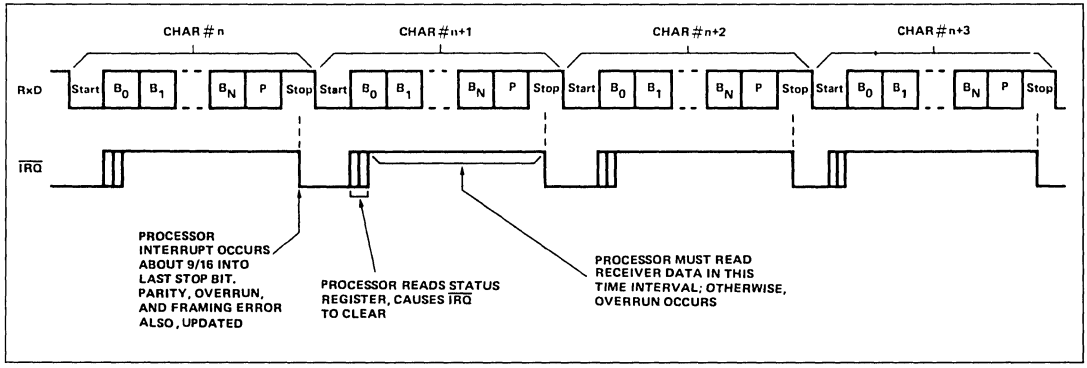


Figure 6. Continuous Data Receive

Transmit Data Register Not Loaded by Processor

If the processor is unable to load the Transmit Data Register in the allocated time, then the TxD line goes to the "MARK" condition until the data is loaded. $\overline{IRQ}$ interrupts continue to occur at the same rate as previously, except no data is transmitted. When the processor finally loads new data, a Start Bit immediately occurs, the data word transmission is started, and another interrupt is initiated, signaling for the next data word. Figure 7 shows the timing relationship for this mode of operation.

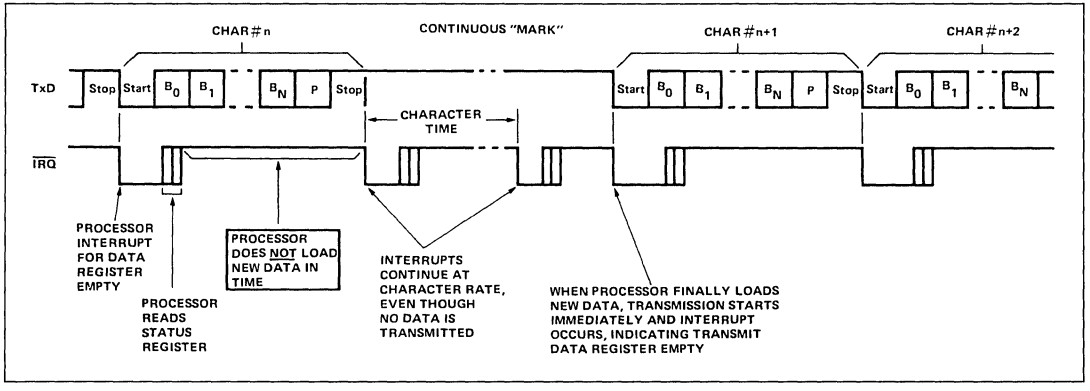


Figure 7. Transmit Data Register Not Loaded by Processor

Effect of $\overline{CTS}$ on Transmitter

$\overline{CTS}$ is the Clear-to-Send signal generated by the modem. It is normally low (true state) but may go high in the event of some modem problems. When this occurs, the TxD line goes to the "MARK" condition after the entire last character (including parity and stop bit) has been transmitted, unless $\overline{CTS}$ goes high during the start bit. Then TxD goes immediately to a "MARK" condition. Bit 4 in the Status Register indicates that the Transmitter Data Register is not empty and $\overline{IRQ}$ is *not* asserted. $\overline{CTS}$ is a transmit control line only, and has no effect on the ACIA Receiver Operation. Figure 8 shows the timing relationship for this mode of operation.

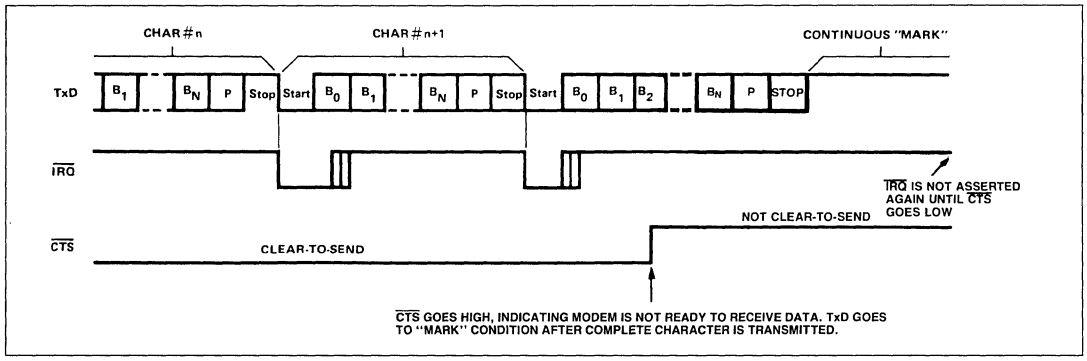


Figure 8. Effect of CTS on Transmitter

Effect of Overrun on Receiver

If the processor does not read the Receiver Data Register in the allocated time, when the next interrupt occurs, the new data word is not transferred to the Receiver Data Register, but the Overrun status bit is set. Thus, the Data Register will contain the last valid data word received and all following data is lost. Figure 9 shows the timing relationship for this mode.

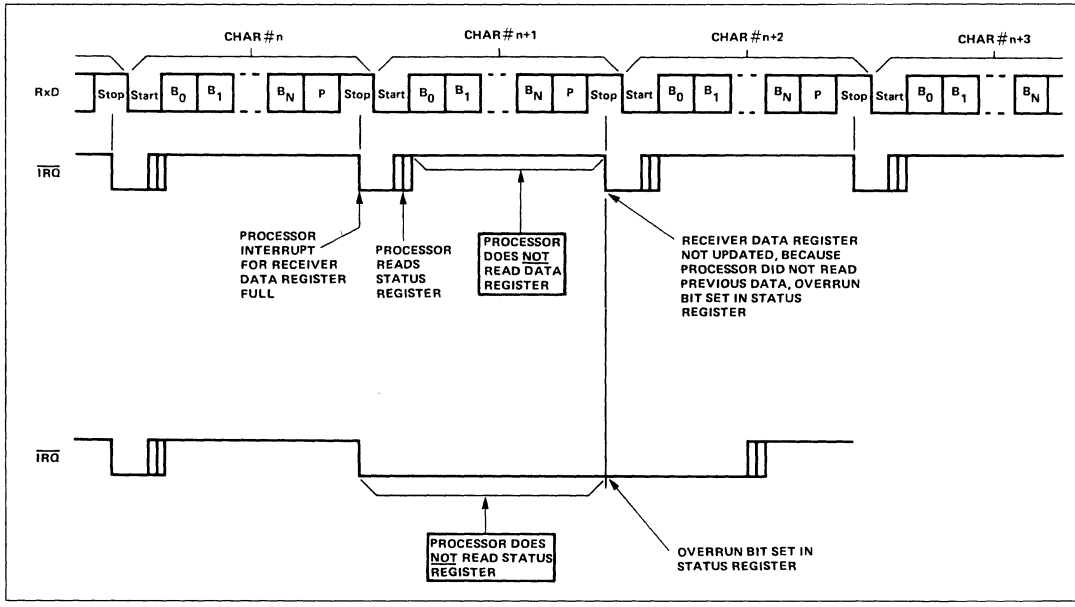


Figure 9. Effect of Overrun on Receiver

Echo Mode Timing

In Echo Mode, the TxD line re-transmits the data on the RxD line, delayed by ½ of the bit time, as shown in Figure 10.

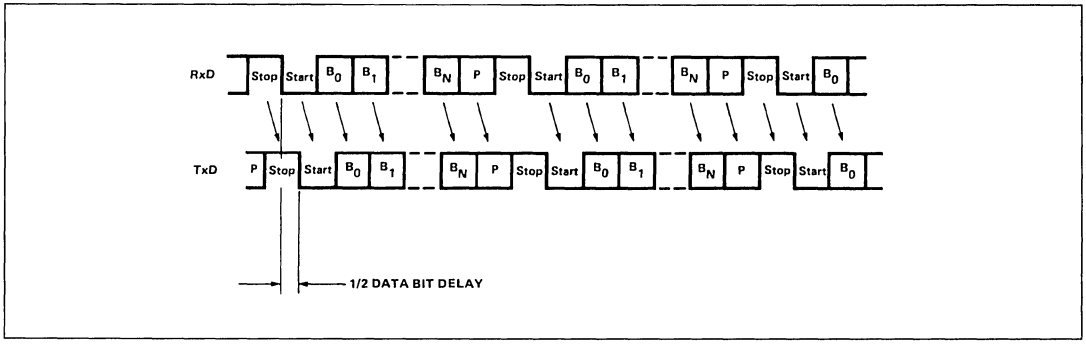


Figure 10. Echo Mode Timing

Effect of $\overline{CTS}$ on Echo Mode Operation

In Echo Mode, the Receiver operation is unaffected by $\overline{CTS}$, however, the Transmitter is affected when $\overline{CTS}$ goes high, i.e., the TxD line immediately goes to a continuous "MARK" condition. In this case, however, the Status Request indicates that the Receiver Data Register is full in response to an $\overline{IRQ}$, so the processor has no way of knowing that the Transmitter has ceased to echo. See Figure 11 for the timing relationship of this mode.

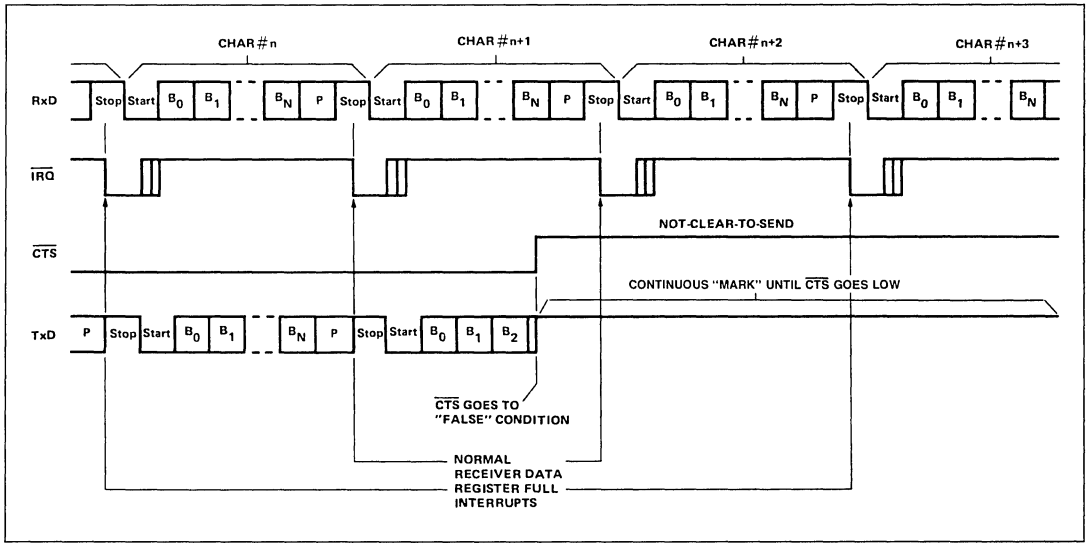


Figure 11. Effect of $\overline{CTS}$ on Echo Mode

Overrun in Echo Mode

If Overrun occurs in Echo Mode, the Receiver is affected the same way as a normal overrun in Receive Mode. For the re-transmitted data, when overrun occurs, the TxD line goes to the "MARK" condition until the first Start Bit after the Receiver Data Register is read by the processor. Figure 12 shows the timing relationship for this mode.

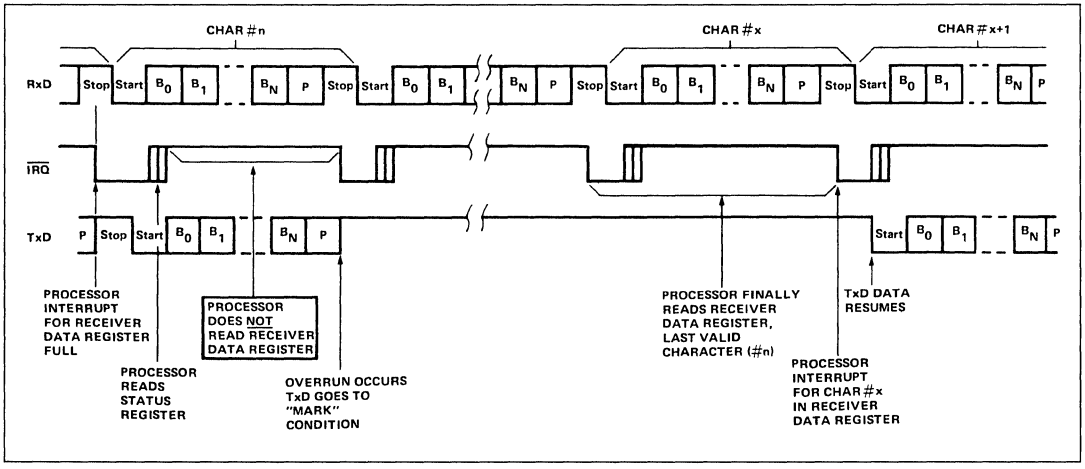


Figure 12. Overrun in Echo Mode

Framing Error

Framing Error is caused by the absence of Stop Bit(s) on received data. A Framing Error is indicated by the setting of bit 1 in the Status Register at the same time the Receiver Data Register Full bit is set, also in the Status Register. In response to $\overline{IRQ}$, generated by RDRF, the Status Register can also be checked for the Framing Error. Subsequent data words are tested for Framing Error separately, so the status bit will always reflect the last data word received. See Figure 13 for Framing Error timing relationship.

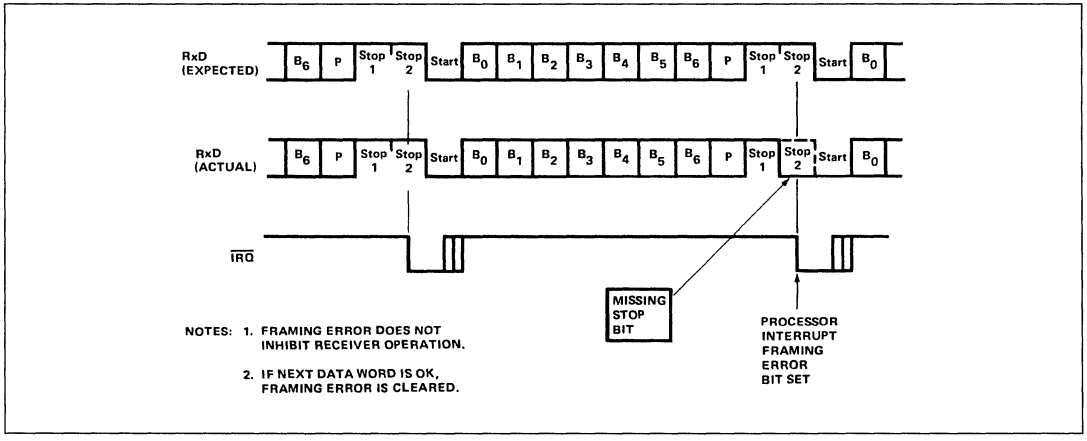


Figure 13. Framing Error

Effect of $\overline{DCD}$ on Receiver

$\overline{DCD}$ is a modem output indicating the status of the carrier-frequency-detection circuit of the modem. This line goes high for a loss of carrier. Normally, when this occurs, the modem will stop transmitting data some time later. The ACIA asserts $\overline{IRQ}$ whenever $\overline{DCD}$ changes state and indicates this condition via bit 5 in the Status Register.

Once such a change of state occurs, subsequent transitions will not cause interrupts or changes in the Status Register until the first interrupt is serviced. When the $\overline{DCD}$ input is high, the receiver is disabled (see Figure 14).

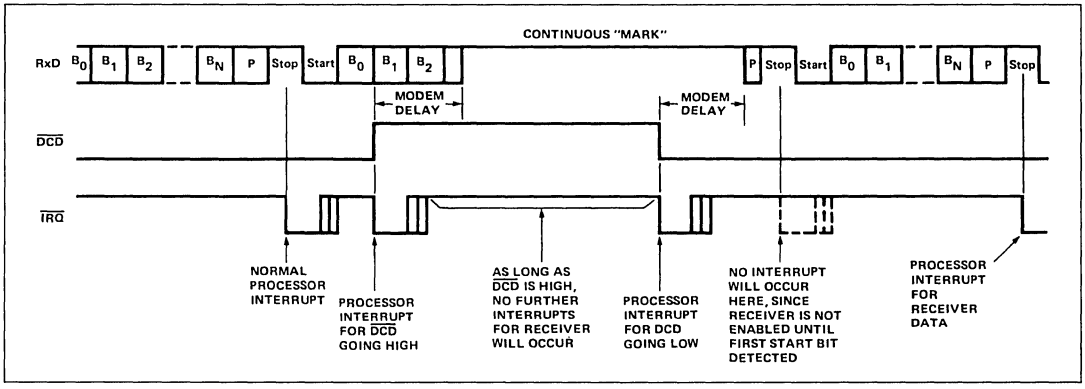


Figure 14. Effect of $\overline{DCD}$ on Receiver

Timing with 1½ Stop Bits

It is possible to select 1½ Stop Bits, but this occurs only for 5-bit data words with no parity bit. In this case, the $\overline{IRQ}$ asserted for Receiver Data Register Full occurs halfway through the trailing half-Stop Bit. Figure 15 shows the timing relationship for this mode.

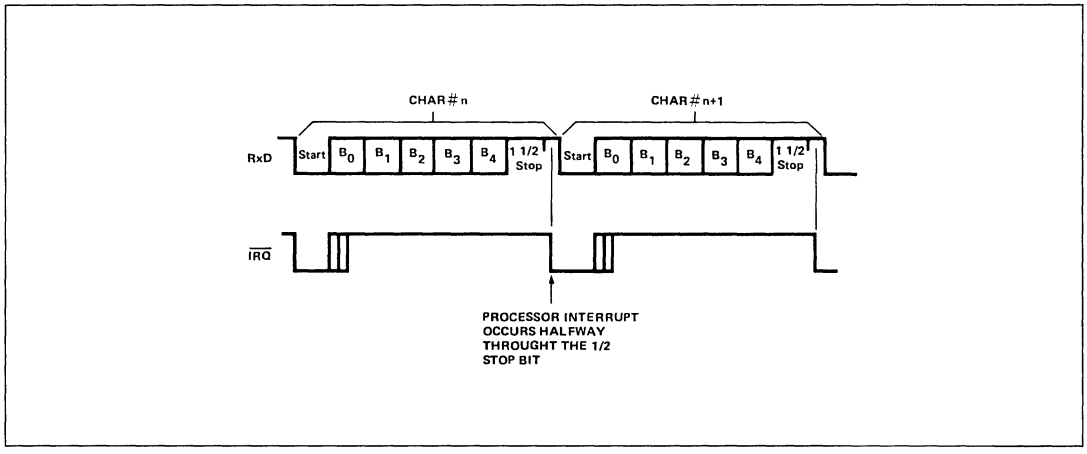


Figure 15. Timing with 1½ Stop Bits

Transmit Continuous "BREAK"

This mode is selected via the ACIA Command Register and causes the Transmitter to send continuous "BREAK" characters, beginning with the next character transmitted. At least one full "BREAK" character will be transmitted, even if the processor quickly re-programs the Command Register transmit mode. Later, when the Command Register is programmed back to normal transmit mode, an immediate Stop Bit will be generated and transmission will resume. Figure 16 shows the timing relationship for this mode.

NOTE

If, while operating in the Transmit Continuous "BREAK" mode, the $\overline{CTS}$ should go to a high, the TxD will be overridden by the $\overline{CTS}$ and will go to continuous "MARK" at the beginning of the next character transmitted after the $\overline{CTS}$ goes high.

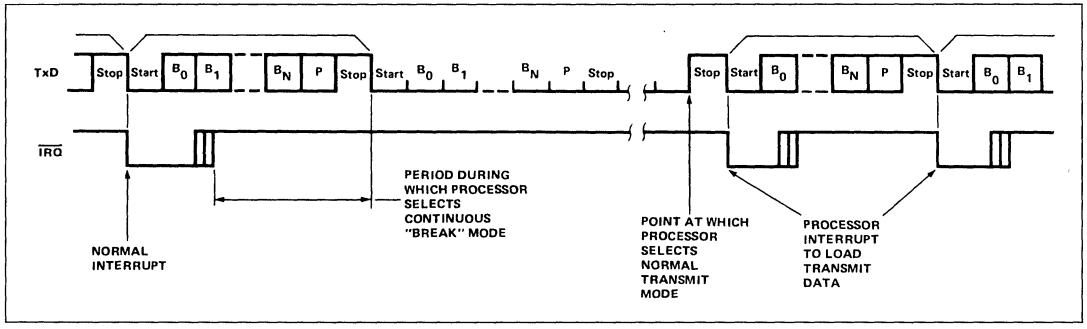


Figure 16. Transmit Continuous "BREAK"

Receive Continuous "BREAK"

In the event the modem transmits continuous "BREAK" characters, the ACIA will terminate receiving. Reception will resume only after a Stop Bit is encountered by the ACIA. Figure 17 shows the timing relationship for continuous "BREAK" characters.

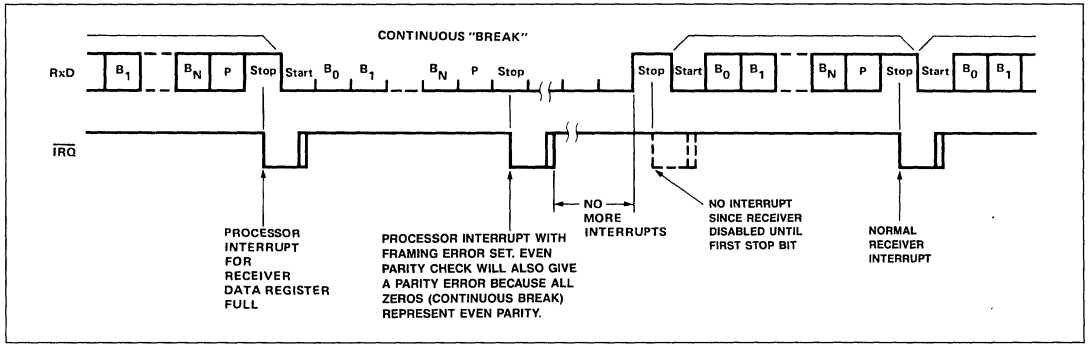


Figure 17. Receive Continuous "BREAK"

CRYSTAL/CLOCK CONSIDERATIONS

CLOCK OSCILLATOR

The on-chip oscillator is designed for a parallel resonant crystal connected between XTLI and XTLO pins. The equivalent oscillator circuit is shown in Figure 18.

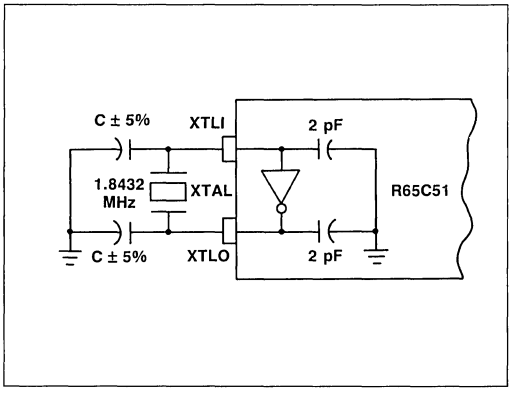


Figure 18. Internal Clock

A parallel resonant crystal is specified by its load capacitance and series resonant resistance. For proper oscillator operation, the load capacitance (C_L), series resistance (R_s) and the crystal resonant frequency (F) must meet the following two relations:

$$(C + 2) = 2C_L \quad \text{or} \quad C = 2C_L - 2$$

$$R_s \leq R_{smax} = \frac{2 \times 10^6}{(FC_L)^2}$$

where: F is in MHz; C and C_L are in pF; R is in ohms.

To select a parallel resonant crystal for the oscillator, first select the load capacitance from a crystal manufacturer's catalog. Next, calculate R_{smax} based on F and C_L. The selected crystal must have a R_s less than the R_{smax}.

For example, if C_L = 13 pF for a 1.8432 MHz parallel resonant crystal, then

$$C = (2 \times 13) - 2 = 18 \text{ pF}$$

The series resistance of the crystal must be less than

$$R_{smax} = \frac{2 \times 10^6}{(1.8432 \times 13)^2} \cong 3.3\text{K ohms}$$

EXTERNAL CLOCK MODES

The XTLI input may be used as an external clock input (Figure 19). For this implementation, a times 16 clock is input on XTLI and XTLO is left open.

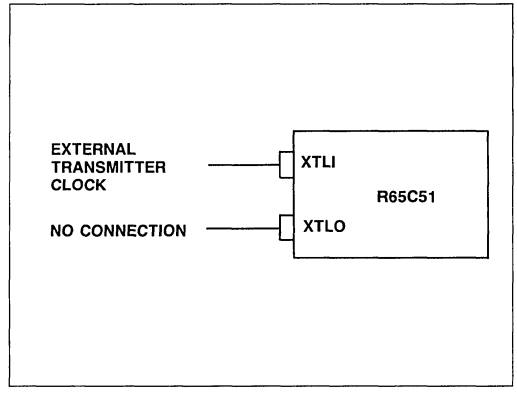


Figure 19. External Clock

GENERATION OF NON-STANDARD BAUD RATES

Divisors

The internal counter/divider circuit generates appropriate divisors to produce standard baud rates when a 1.8432 MHz crystal is connected between XTLI and XTLO. Control Register bits 0–3 select the divisor for a particular baud rate as shown in Table 2.

Generating Non-Standard Baud Rates

By using a different crystal, non-standard baud rates may be generated. These can be determined by:

$$\text{Baud Rate} = \frac{\text{Crystal Frequency}}{\text{Divisor}}$$

Furthermore, it is possible to drive the ACIA with an off-chip oscillator to achieve other baud rates. In this case, XTALI (pin 6) must be the clock input and XTALO (pin 7) must be a no-connect.

Table 2. Divisor Selection

Control Register Bits				Divisor Selected For The Internal Counter	Baud Rate Generated With 1.8432 MHz Crystal	Baud Rate Generated With a Crystal of Frequency (F)
3	2	1	0			
0	0	0	0	16	External Transmitter Clock Rate ÷ 16	External Transmitter Clock Rate ÷ 16
0	0	0	1	36,864	$\frac{1.8432 \times 10^6}{36,864} = 50$	$\frac{F}{36,864}$
0	0	1	0	24,576	$\frac{1.8432 \times 10^6}{24,576} = 75$	$\frac{F}{24,576}$
0	0	1	1	16,769	$\frac{1.8432 \times 10^6}{16,769} = 109.92$	$\frac{F}{16,769}$
0	1	0	0	13,704	$\frac{1.8432 \times 10^6}{13,704} = 134.51$	$\frac{F}{13,704}$
0	1	0	1	12,288	$\frac{1.8432 \times 10^6}{12,288} = 150$	$\frac{F}{12,288}$
0	1	1	0	6,144	$\frac{1.8432 \times 10^6}{6,144} = 300$	$\frac{F}{6,144}$
0	1	1	1	3,072	$\frac{1.8432 \times 10^6}{3,072} = 600$	$\frac{F}{3,072}$
1	0	0	0	1,536	$\frac{1.8432 \times 10^6}{1,536} = 1,200$	$\frac{F}{1,536}$
1	0	0	1	1,024	$\frac{1.8432 \times 10^6}{1,024} = 1,800$	$\frac{F}{1,024}$
1	0	1	0	768	$\frac{1.8432 \times 10^6}{768} = 2,400$	$\frac{F}{768}$
1	0	1	1	512	$\frac{1.8432 \times 10^6}{512} = 3,600$	$\frac{F}{512}$
1	1	0	0	384	$\frac{1.8432 \times 10^6}{384} = 4,800$	$\frac{F}{384}$
1	1	0	1	256	$\frac{1.8432 \times 10^6}{256} = 7,200$	$\frac{F}{256}$
1	1	1	0	192	$\frac{1.8432 \times 10^6}{192} = 9,600$	$\frac{F}{192}$
1	1	1	1	96	$\frac{1.8432 \times 10^6}{96} = 19,200$	$\frac{F}{96}$

DIAGNOSTIC LOOP-BACK OPERATING MODES

It may be desirable to include in the system a facility for local loop-back testing.

In local loop-back testing, the Modem and Data Link must be effectively disconnected and the ACIA transmitter connected back to its own receiver, so that the processor can perform diagnostic checks on the system, excluding the actual data channel.

The ACIA does not contain automatic loop-back operating modes, but they may be implemented with the addition of a small amount of external circuitry. Figure 20 indicates the necessary logic to be used with the ACIA. The LLB line is the positive-true signal to enable local loop-back operation. Essentially, LLB = high does the following:

1. Disables outputs TxD, $\overline{DTR}$, and $\overline{RTS}$ (to Modem).
2. Disables inputs RxD, $\overline{DCD}$, $\overline{CTS}$, $\overline{DSR}$ (from Modem).
3. Connects transmitter outputs to respective received inputs (i.e., TxD to RxD, $\overline{DTR}$ to $\overline{DCD}$, $\overline{RTS}$ to $\overline{CTS}$).

LLB may be tied to a peripheral control pin (from an R65C21 or R65C24, for example) to provide processor control of local loop-back operation. In this way, the processor can easily perform local loop-back diagnostic testing.

MISCELLANEOUS

1. If Echo Mode is selected, $\overline{RTS}$ goes low.
2. If Bit 0 of Command Register ($\overline{DTR}$) is 0 (disabled), then:
   a) All interrupts are disabled, including those caused by $\overline{DCD}$ and $\overline{DSR}$ transitions.
   b) Transmitter is disabled immediately.
   c) Receiver is disabled, but a character currently being received will be completed first.
3. Odd parity occurs when the sum of all the 1 bits in the data word (including the parity bit) is odd.
4. In the receive mode, the received parity bit does not go into the Receiver Data Register, but generates parity error or no parity error for the Status Register.
5. Transmitter and Receiver may be in full operation simultaneously. This is "full-duplex" mode.

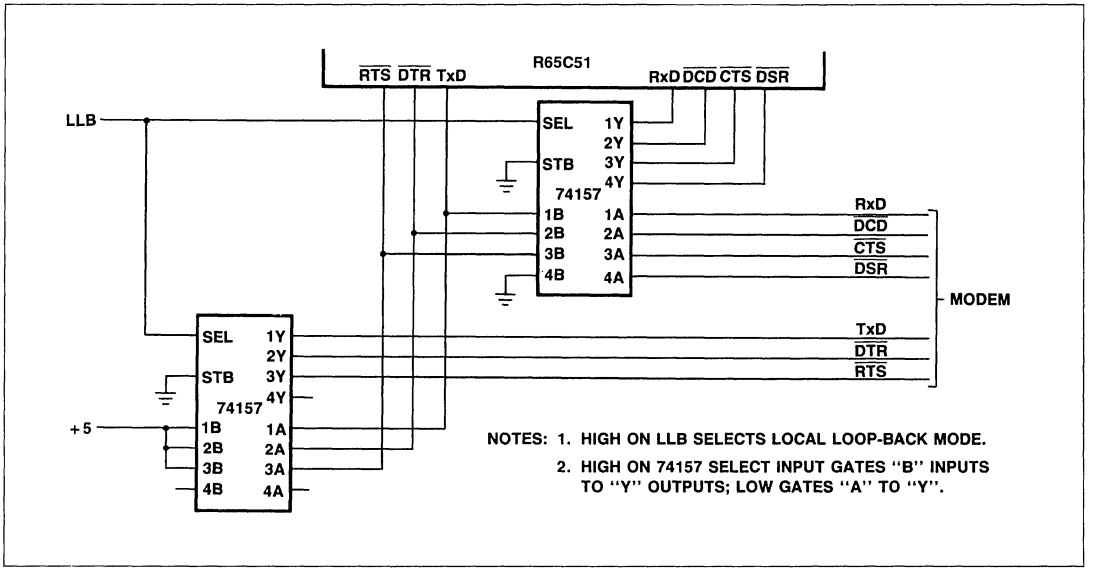


Figure 20. Loop-Back Circuit Schematic

6. If the RxD line inadvertently goes low and then high right after a Stop Bit, the ACIA does not interpret this as a Start Bit, but samples the line again halfway into the bit time to determine if it is a true Start Bit or a false one. For false Start Bit detection, the ACIA does not begin to receive data, instead, only a true Start Bit initiates receiver operation.

7. $\overline{DCD}$ and $\overline{DSR}$ transitions, although causing immediate processor interrupts, have no affect on transmitter operation. Data will continue to be sent, unless the processor forces the transmitter to turn off. Since these are high-impedance inputs, they must not be permitted to float (un-connected). If unused, they must be tied to GND.

8. If TDRE is checked by polling (rather than by interrupt), a period of at least 1/16 Baud clock should be allowed after loading Tx Data Buffer to ensure that TDRE is valid.

READ TIMING DIAGRAM

Timing diagrams for transmit with external clock, receive with external clock, and $\overline{IRQ}$ generation are shown in Figures 21, 22 and 23, respectively. The corresponding timing characteristics are listed in Table 3.

Table 3. Transmit/Receive Characteristics

Characteristic	Symbol	1 MHz		2 MHz		Unit
		Min	Max	Min	Max	
Transmit/Receive Clock Rate	t_{CCY}	400*	—	400*	—	ns
Transmit/Receive Clock High Time	t_{CH}	175	—	175	—	ns
Transmit/Receive Clock Low Time	t_{CL}	175	—	175	—	ns
XTLI to TxD Propagation Delay	t_{DD}	—	500	—	500	ns
$\overline{RTS}$, $\overline{DTR}$ Propagation Delay	t_{DLY}	—	500	—	500	ns
$\overline{IRQ}$ Propagation Delay (Clear)	t_{IRQ}	—	500	—	500	ns

Notes:
(t_R, t_F = 10 to 30 ns)

*The baud rate with external clocking is: Baud Rate = $\frac{1}{16 \times t_{CCY}}$

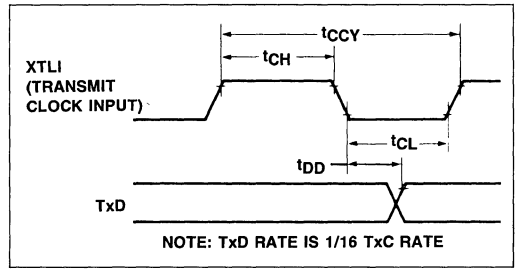


Figure 21. Transmit Timing with External Clock

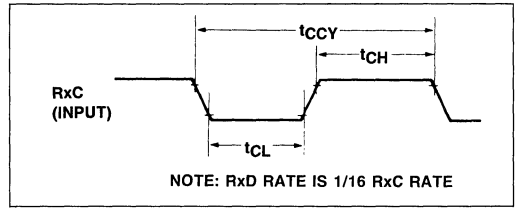


Figure 22. Receive External Clock Timing

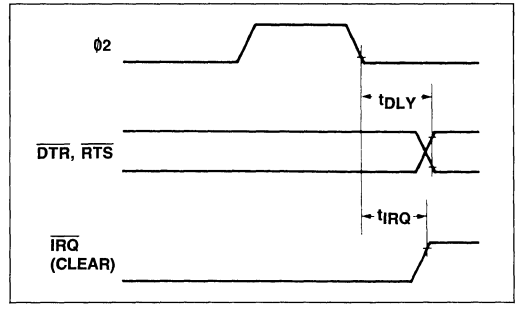


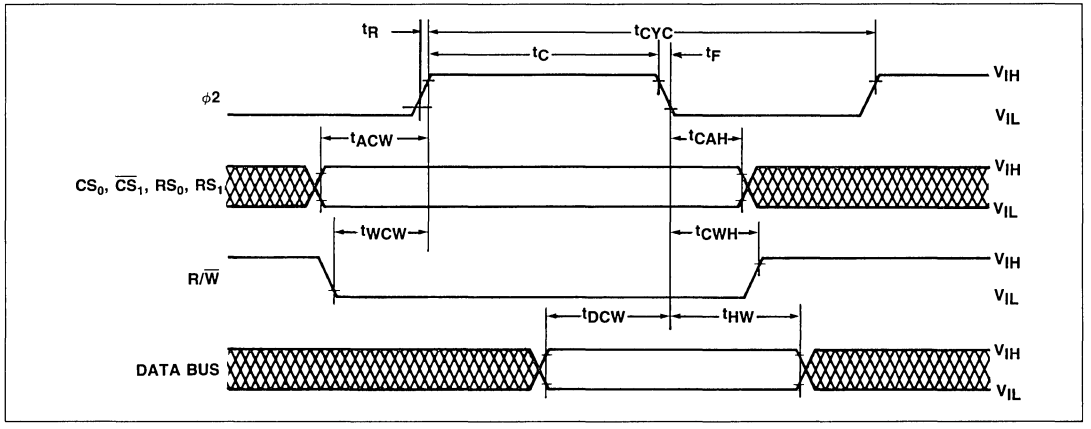
Figure 23. Interrupt and Output Timing

SWITCHING CHARACTERISTICS

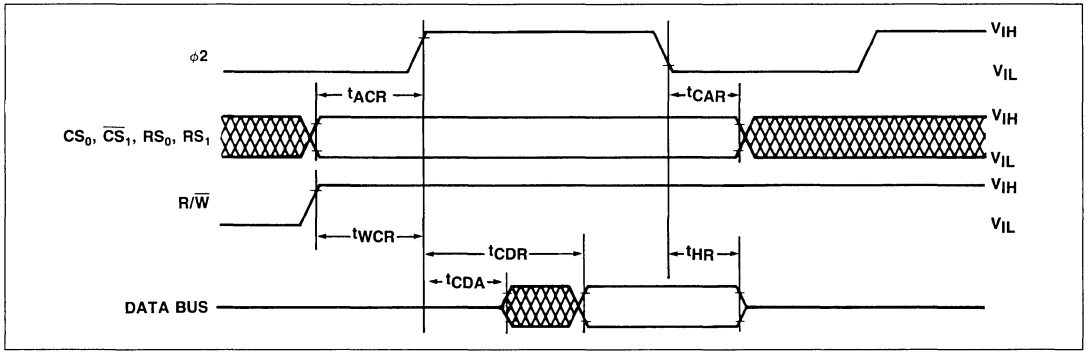
(V_{CC} = 5.0 Vdc ±5%, V_{SS} = 0, T_A = T_L to T_H, unless otherwise noted)

Parameter	Symbol	1 MHz		2 MHz		Unit
		Min	Max	Min	Max	
Ø2 Cycle Time	t_{CYC}	1000	—	500	—	ns
Ø2 Pulse Width	t_C	400	—	200	—	ns
Address Set-Up Time	t_{ACW}, t_{ACR}	120	—	60	—	ns
Address Hold Time	t_{CAH}, t_{CAR}	0	—	0	—	ns
R/$\overline{W}$ Set-Up Time	t_{WCW}, t_{WCR}	120	—	60	—	ns
R/$\overline{W}$ Hold Time	t_{CWH}	0	—	0	—	ns
Data Bus Set-Up Time	t_{DCW}	150	—	60	—	ns
Data Bus Hold Time	t_{HW}	20	—	10	—	ns
Read Access Time (Valid Data)	t_{CDR}	—	200	—	170	ns
Read Hold Time	t_{HR}	20	—	10	—	ns
Bus Active Time (Invalid Data)	t_{CDA}	40	—	20	—	ns

Notes:
1. t_R and t_F = 10 to 30 ns.
2. Timing measurements are referenced to/from a low of 0.8 volts and a high of 2.0 volts.



Write Timing Diagram



Read Timing Diagram

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to +7.0	Vdc
Input Voltage	V_{IN}	−0.3 to V_{CC} +0.3	Vdc
Output Voltage	V_{OUT}	−0.3 to V_{CC} +0.3	Vdc
Operating Temperature Commercial	T_A	0 to +70	°C
Storage Temperature	T_{STG}	−55 to +150	°C

*NOTE: Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in other sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING CONDITIONS

Parameter	Symbol	Value
Supply Voltage	V_{CC}	5Vdc ±5%
Temperature Range Commercial	T_A	T_L to T_H 0° to 70°C

ELECTRICAL CHARACTERISTICS

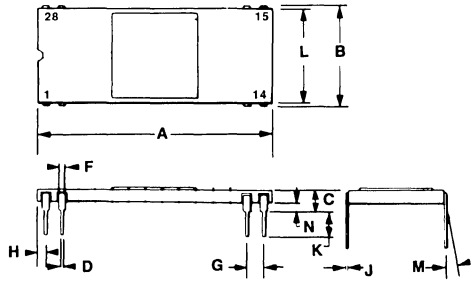
(V_{CC} = 5.0 Vdc ±5%, V_{SS} = 0, T_A = T_L to T_H, unless otherwise noted)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input High Voltage	V_{IH}				V	
Except XTLI		2.0	—	V_{CC}		
XTLI		2.8	—	V_{CC}		
Input Low Voltage	V_{IL}				V	
Except XTLI		−0.3	—	+0.8		
XTLI		−0.3	—	+0.4		
Input Leakage Current: Ø2, R/$\overline{W}$, $\overline{RES}$, CS0, $\overline{CS1}$, RS0, RS1, $\overline{CTS}$, RxD, $\overline{DCD}$, $\overline{DSR}$	I_{IN}	—	±1	±2.5	μA	V_{IN} = 0V to V_{CC} V_{CC} = 5.25V
Input Leakage Current (Three State Off) D0–D7	I_{TSI}	—	±2	±10	μA	V_{IN} = 0.4V to 2.4V V_{CC} = 5.25V
Output High Voltage: D0–D7, TxD, RxC, $\overline{RTS}$, $\overline{DTR}$	V_{OH}	2.4	—	—	V	V_{CC} = 4.75V I_{LOAD} = −100 μA
Output Low Voltage: D0–D7, TxD, RxC, $\overline{RTS}$, $\overline{DTR}$, $\overline{IRQ}$	V_{OL}	—	—	0.4	V	V_{CC} = 4.75V I_{LOAD} = 1.6 mA
Output High Current (Sourcing): D0–D7, TxD, RxC, $\overline{RTS}$, $\overline{DTR}$	I_{OH}	−100	−400	—	μA	V_{OH} = 2.4V
Output Low Current (Sinking): D0–D7, TxD, RxC, $\overline{RTS}$, $\overline{DTR}$, $\overline{IRQ}$	I_{OL}	1.6	—	—	mA	V_{OL} = 0.4V
Output Leakage Current (off state): $\overline{IRQ}$	I_{OFF}	—	—	10	μA	V_{OUT} = 5.0V
Power Dissipation	P_D	—	7	10	mW/MHz	
Input Capacitance						V_{CC} = 5.0V V_{IN} = 0V f = 2 MHz T_A = 25°C
Ø2	C_{CLK}	—	—	20	pF	
All except Ø2	C_{IN}	—	—	10	pF	
Output Capacitance	C_{OUT}	—	—	10	pF	

Notes:
1. All units are direct current (dc) except for capacitance.
2. Negative sign indicates outward current flow, positive indicates inward flow.
3. Typical values are shown for V_{CC} = 5.0V and TA = 25°C.

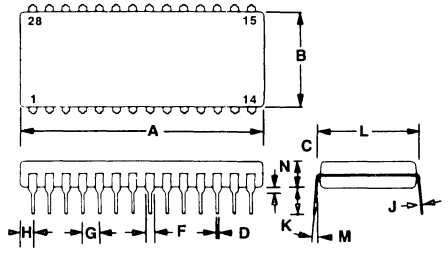
PACKAGE DIMENSIONS

28-PIN CERAMIC DIP



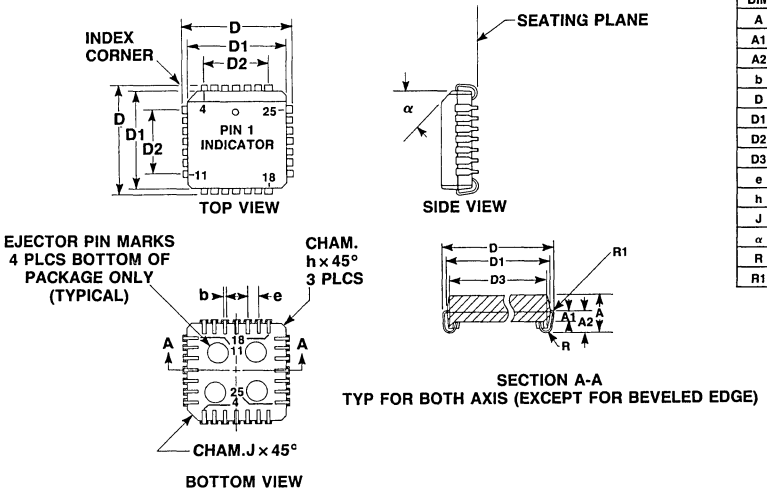
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	35.05	36 07	1.380	1.420
B	15.11	15.88	0 595	0 625
C	2.54	4.19	0.100	0.165
D	0.38	0.53	0.015	0 021
F	0.76	1.27	0.030	0 050
G	2.54 BSC		0.100 BSC	
H	0.76	1.78	0.030	0.070
J	0.20	0.33	0.008	0.013
K	2.54	4.19	0.100	0.165
L	14.60	15.37	0.575	0 605
M	0°	10°	0°	10°
N	0.51	1.52	0.020	0.060

28-PIN PLASTIC DIP



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	36.32	37.34	1.430	1.470
B	13 46	13.97	0.530	0.550
C	3.56	5 08	0.140	0.200
D	0.38	0.53	0.015	0.021
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.30	0.008	0.012
K	3.30	4.32	0.130	0.170
L	15.24 BSC		0.600 BSC	
M	7°	10°	7°	10°
N	0.51	1.02	0.020	0.040

28-PIN PLASTIC LEADED CHIP CARRIER (PLCC)



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	4.14	4.39	0.163	0.173
A1	1.37	1.47	0.054	0.058
A2	2.31	2.46	0.091	0.097
b	0.457 TYP		0.018 TYP	
D	12.37	12.52	0.487	0.493
D1	11.43	11.53	0.450	0.454
D2	7.54	7.70	0.297	0.303
D3	10.67 REF		0.420 REF	
e	1.27 BSC		0.050 BSC	
h	1 15 TYP		0.045 TYP	
J	0.25 TYP		0.010 TYP	
α	45° TYP		45° TYP	
R	0.89 TYP		0.035 TYP	
R1	0.25 TYP		0.010 TYP	

R65C52
Dual Asynchronous Communications Interface Adapter (DACIA)

PRELIMINARY

DESCRIPTION

The Rockwell CMOS R65C52 Dual Asynchronous Communications Interface Adapter (DACIA) provides an easily implemented, program controlled two-channel interface between 8-bit microprocessor-based systems and serial communication data sets and modems.

The DACIA is designed for maximum programmed control from the microprocessor (MPU) to simplify hardware implementation. Dual sets of registers allow independent control and monitoring of each channel.

Transmitter and Receiver bit rates may be controlled by an internal baud rate generator or external times 16 clocks. The baud rate generator accepts either a crystal or a clock input, and provides 15 programmable baud rates. When a 3.6864 MHz crystal is used, the baud rates range from 50 bps to 38,400 bps.

The DACIA may be programmed to transmit and receive frames having word lengths of 5, 6, 7 or 8 bits; even, odd, space, mark or no parity; and 1 or 2 stop bits.

A Compare Register, and the ability to detect address frames, facilitate address recognition in a multidrop mode.

FEATURES

- Low power CMOS N-well silicon gate technology
- Two independent full duplex channels with buffered receivers and transmitters.
- Data set/modem control functions
- Internal baud rate generator with 15 programmable baud rates (50 bps to 38,400 bps)
- Program-selectable internally or externally controlled receiver and transmitter bit rates
- Programmable word lengths, number of stop bits, and parity bit generation and detection
- Programmable interrupt control
- Edge detect for $\overline{DCD}$, $\overline{DSR}$, and $\overline{CTS}$
- Program-selectable echo mode for each channel
- Compare Register
- Address/Data frame recognition
- 5.0 Vdc ±5% supply requirements
- 40-pin plastic or ceramic DIP or 44-pin PLCC
- Full TTL or CMOS input/output compatibility
- Compatible with R6500 and R65C00 microprocessors and R6500/* microcomputers

ORDERING INFORMATION

Part Number:
R65C52 ___

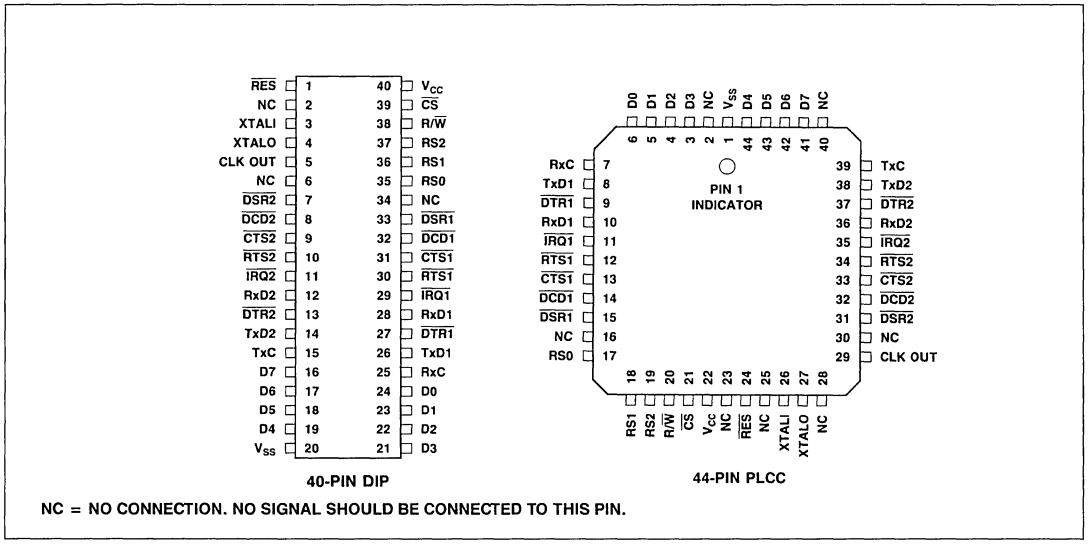
Temperature Range (T_L to T_H):
Blank = 0°C to +70°C
E = −40°C to +85°C

Frequency Range:
1 = 1 MHz
2 = 2 MHz
3 = 3 MHz

Package
C = 40-Pin Ceramic DIP
P = 40-Pin Plastic DIP
J = 44-Pin Plastic Leaded Chip Carrier (PLCC)

INTERFACE SIGNALS

The DACIA is available in a 40-pin DIP or a 44-pin PLCC. Figure 1 shows the pin assignments for each package. The DACIA interface signals are shown in Figure 2. Table 1 contains a description of each signal.



NC = NO CONNECTION. NO SIGNAL SHOULD BE CONNECTED TO THIS PIN.

Figure 1. R65C52 Pin Assignments

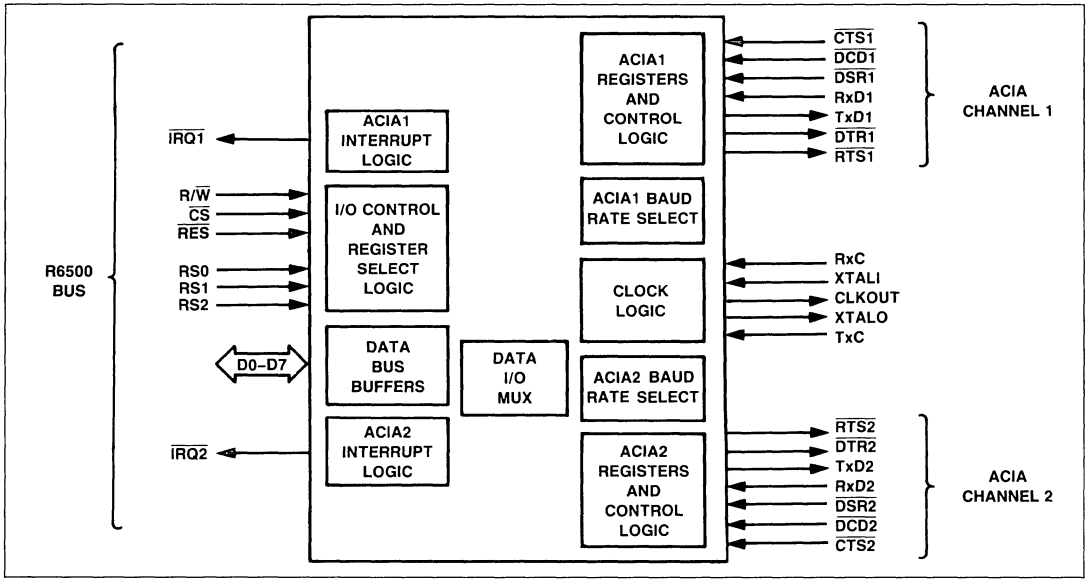


Figure 2. R65C52 DACIA Interface Signals

Table 1. DACIA Interface Signal Definitions

Signal	Pin No. DIP	Pin No. PLCC	I/O	Name/Description
Host Interface				
$\overline{RES}$	1	24	I	**Reset.** Active low input controlling the reset function. This signal must be driven low for a minimum of 4 μs for a valid reset to occur. It is driven high during normal operation.
R/$\overline{W}$	38	20	I	**Read/Write.** Input controlling the direction of data transfer. It is driven low during write cycles, and is driven high at all other times.
$\overline{CS}$	39	21	I	**Chip Select.** Active low input enabling data transfers between the host CPU and the DACIA. The DACIA latches register selects and the R/$\overline{W}$ input on the falling edge of $\overline{CS}$. It latches input data on the rising edge of $\overline{CS}$.
RS0–RS3	35–37	17–19	I	**Register Select.** Three inputs controlling access to the DACIA internal registers. Table 3 lists the coding for each register.
D0–D3 D4–D7	24–21 19–16	6–3 44–41	I/O	**Data Bus.** Eight bidirectional lines used to transfer data between the host and the DACIA. These lines output data during READ cycles when $\overline{CS}$ is low. At all other times, they are in the high impedance state.
$\overline{IRQ1}$ $\overline{IRQ2}$	29 11	11 35	O	**Interrupt Request.** Two active low, open-drain outputs from the interrupt control logic. These outputs are normally high. An $\overline{IRQ}$ line goes low when one of the flags of the associated ISR is set if the corresponding enable bit is set in the IER.
Clock Interface				
XTALI XTALO	3 4	26 27	I O	**Crystal Input/Output.** One input and one output through which the reference signal for the internal clock oscillator is supplied. A parallel resonant crystal may be connected across the pins or a clock may be input at XTALI. When a clock is used, XTALO must be left open.
CLK OUT	5	29	O	**Clock Out.** A buffered output from the internal clock oscillator which is in phase with XTALI. This output may be used to drive the XTALI input of another DACIA. Therefore, several DACIA chips may be driven with one crystal.
RxC	25	7	I	**Receiver Clock.** Input for external 16x receiver clock.
TxC	15	39	I	**Transmitter Clock.** Input for external 16x transmitter clock.
Serial Channel Interface				
$\overline{DTR1}$ $\overline{DTR2}$	27 13	9 37	O	**Data Terminal Ready.** Two general purpose outputs which are set high upon reset. The output level is programmed by setting the appropriate bit in the associated Format Register (FR) high or low. The state of each DTR line is reflected by the $\overline{DTR}$ LVL bit in the associated Control Status Register (CSR).
$\overline{DSR1}$ $\overline{DSR2}$	33 7	15 31	I	**Data Set Ready.** Two general purpose inputs. An active transition sets the $\overline{DSRT}$ bit in the Interrupt Enable Register (ISR). The $\overline{DSR}$ LVL bit in the associated CSR reflects the current state of a $\overline{DSR}$ line.
$\overline{RTS1}$ $\overline{RTS2}$	30 10	12 34	O	**Request To Send.** Two general purpose outputs which are set high upon reset. The output level is programmed by setting the appropriate bit in the associated FR high or low. The state of an $\overline{RTS}$ line is reflected by the $\overline{RTS}$ LVL bit in the associated CSR.
$\overline{CTS1}$ $\overline{CTS2}$	31 9	13 33	I	**Clear To Send.** The $\overline{CTS}$ control line inputs allow handshaking by the transmitters. When $\overline{CTS}$ is low, the data is transmitted continuously. When $\overline{CTS}$ is high, the Transmit Data Register Empty bit (TDRE) in the associated ISR is not set. The word presently in the Transmit Shift Register is sent normally. Any active transition on a $\overline{CTS}$ line sets the $\overline{CTST}$ bit in the appropriate ISR. The $\overline{CTS}$ LVL bit in the associated CSR reflects the current state of $\overline{CTS}$.
TxD1 TxD2	26 14	8 38	O	**Transmit Data.** The TxD outputs transfer serial non-return to zero (NRZ) data to the data communications equipment (DCE). The data is transferred, LSB first, at a rate determined by the baud rate generator or external clock.
$\overline{DCD1}$ $\overline{DCD2}$	32 8	14 32	I	**Data Carrier Detect.** Two general purpose inputs. An active transition sets the $\overline{DCDT}$ bit in the appropriate ISR. The $\overline{DCD}$ LVL bit in the associated CSR reflects the current state of a $\overline{DCD}$ line.
RxD1 RxD2	28 12	10 36	I	**Receive Data.** The RxD inputs transfer serial NRZ data into the DACIA from the DCE, LSB first. The receiver baud rate is determined by the baud rate generator or external clock.
Power				
VCC	40	22	I	**DC Power Input.** 5.0V ±5%.
VSS	20	1	I	**Power and Signal Reference.**

FUNCTIONAL DESCRIPTION

Figure 3 is a block diagram of the DACIA which consists of two asynchronous communications interface adapters with common microprocessor interface control logic and data bus buffers. The individual functional elements of the DACIA are described in the following paragraphs.

RESET LOGIC

The Reset Logic sets various internal registers, status bits and control lines to a known state. The $\overline{RES}$ input must be driven low for a minimum of 4 μs for a valid reset to occur. At this time, the IERs are set to $80, the RDRs and ACRs are cleared, and the compare mode is disabled. Also, the $\overline{DTR}$ and $\overline{RTS}$ outputs are driven high and the $\overline{CTS}$, $\overline{DCD}$ and $\overline{DSR}$ transition detect flags are cleared. No other bits are affected.

DATA BUS BUFFER

The Data Bus Buffer is a bidirectional interface between the data lines and the internal data bus. The state of the Data Bus Buffer is controlled by the I/O Control Logic and the Interrupt Logic. Table 2 summarizes the Data Bus Buffer states.

I/O CONTROL LOGIC

The I/O Control Logic controls data transfers between the Internal Registers and the Data Bus Buffer. Internal Register selection is determined by the Register Select inputs as shown in Table 3. When R/$\overline{W}$ is high and $\overline{CS}$ is low, data from the selected register is transferred from the internal data bus to the data lines. When $\overline{CS}$ is high, the DACIA is deselected and the data lines are tri-stated.

INTERRUPT LOGIC

The interrupt logic causes the $\overline{IRQ}$ lines ($\overline{IRQ1}$ or $\overline{IRQ2}$) to go low when conditions are met that require the attention of the MPU. There are two registers (the Interrupt Enable Register and the Interrupt Status Register) involved in the control of interrupts in the DACIA. Corresponding bits in both registers must be set to cause an $\overline{IRQ}$.

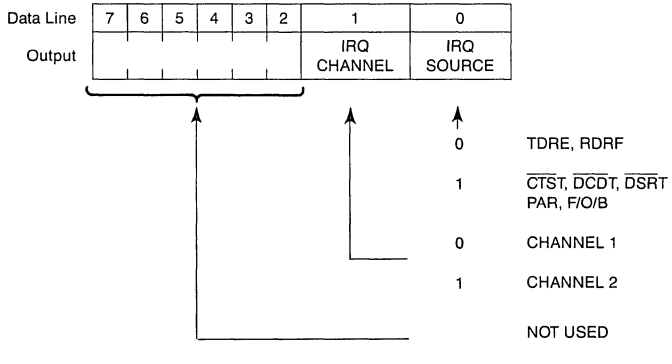
CLOCK OSCILLATOR LOGIC

The internal clock oscillator supplies the time base for the baud rate generator. The oscillator can be driven by a crystal or an external clock.

The baud rate generator may be disabled by connecting XTALI to ground and leaving XTALO open. When this is done, a transmitter times 16 clock must be input at TxC, a receiver times 16 clock must be input at RxC and the Control Registers must be programmed to select TxC and RxC clocks.

Table 2. Data Bus Buffer Summary

Control Signals R/$\overline{W}$	Control Signals $\overline{CS}$	Data Bus Buffer State
L	L	Write Mode — Tri-State
H	L	Read Mode — Output Data
X	H	Deselected — Tri State



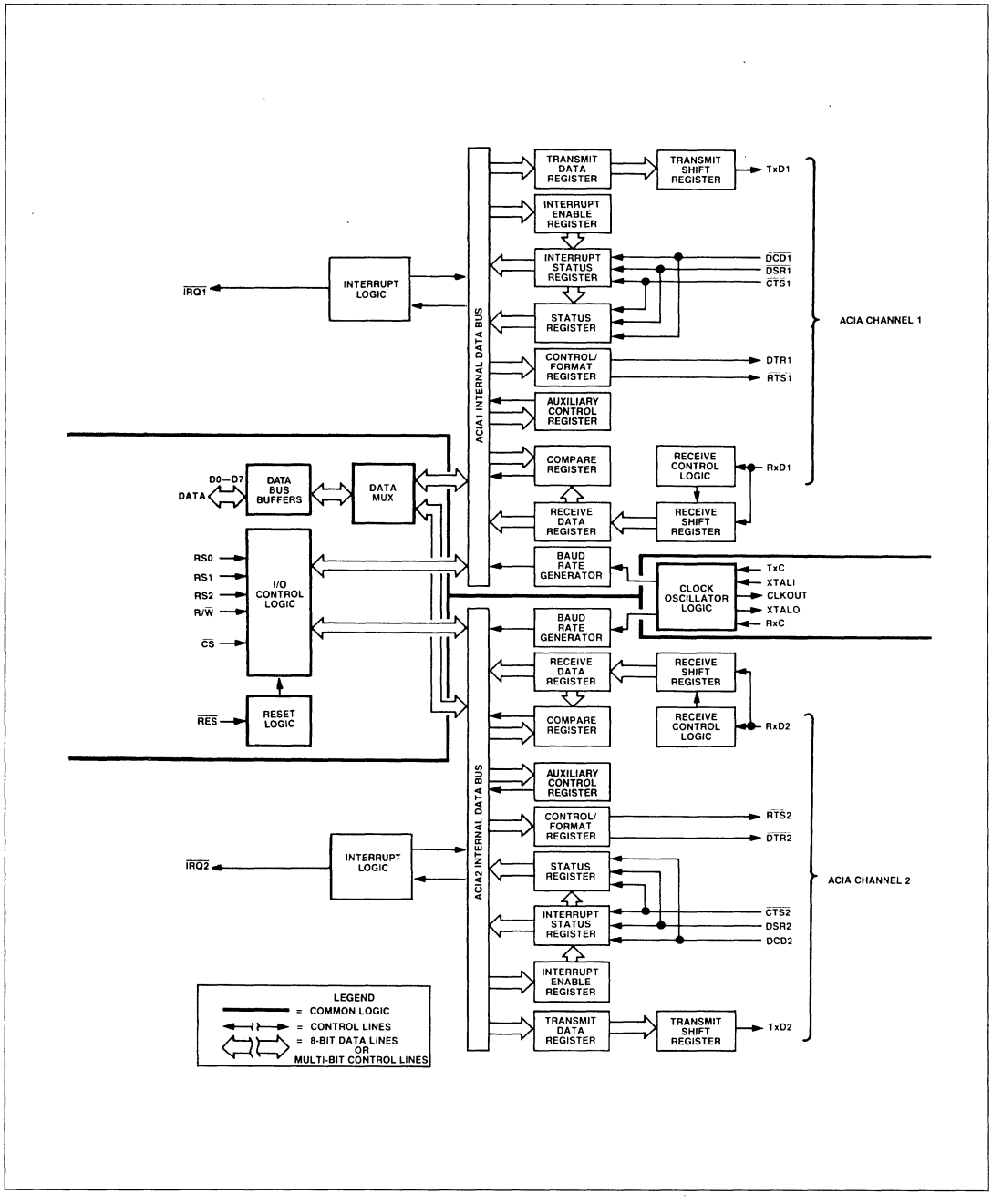


Figure 3. DACIA Block Diagram

Table 3. DACIA Register Selection

Register Select Lines				Register Accessed			
				Write		Read	
HEX	RS2	RS1	RS0	Symbol	Name	Symbol	Name
0	L	L	L	IER1	Interrupt Enable Register 1	ISR1	Interrupt Status Register 1
1	L	L	H	CR1	Control Register 1[1]	CSR1	Control Status Register 1
				FR1	Format Register 1[2]		
2	L	H	L	CDR1	Compare Data Register 1[3]		Not Used
				ACR1	Auxiliary Control Register 1[4]		
3	L	H	H	TDR1	Transmit Data Register 1	RDR1	Receive Data Register 1
4	H	L	L	IER2	Interrupt Enable Register 2	ISR2	Interrupt Status Register 2
5	H	L	H	CR2	Control Register 2[1]	CSR2	Control Status Register 2
				FR2	Format Register 2[2]		
6	H	H	L	CDR2	Compare Data Register 2[3]		Not Used
				ACR2	Auxiliary Control Register 2[4]		
7	H	H	H	TDR2	Transmit Data Register 2	RDR2	Receive Data Register 2

Notes:
1. D7 must be set low to write to the Control Registers.
2. D7 must be set high to write to the Format Registers.
3. Control Register bit 6 must be set to 0 to access the Compare Register.
4. Control Register bit 6 must be set to 1 to access the Auxiliary Control Register.

SERIAL DATA CHANNELS

Two independent serial data channels are available for the full duplex (simultaneous transmit and receive) transfer of asynchronous frames. Separate internal registers are provided for each channel for the selection of frame parameters (number of bits per character, parity options, etc.), status flags, interrupt control and handshake. The asynchronous frame format is shown in Figure 4.

Transmit data from the host system is loaded into the Transmit Data Register. From there, it is transferred to the Transmit Shift Register where it is shifted, LSB first, onto the TxD line. All transmissions begin with a start bit and end with the user selected number of stop bits. A parity bit is transmitted before the stop bit(s) if parity is enabled.

Receive data is shifted into the Receive Shift Register from the associated RxD line. Start and stop bits are stripped from the frame and the data is transferred to the Receive Data Register. Parity bits may be discarded or stored in the ISR.

Five I/O lines are provided for each channel for handshake with the data communications equipment (DCE). Four of these signals ($\overline{RTS}$, $\overline{DTR}$, $\overline{DSR}$ and $\overline{DCD}$) are general purpose inputs or outputs. The fifth signal, $\overline{CTS}$, enables/disables the transmitter. When $\overline{CTS}$ is high and the Transmit Shift Register is empty, the transmitter (except for Echo Mode) is inhibited. When $\overline{CTS}$ is low, the transmitter is enabled.

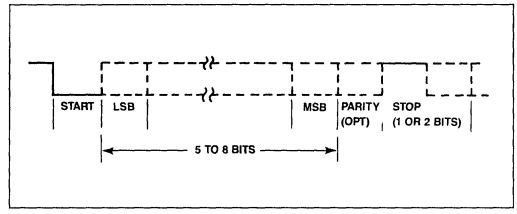


Figure 4. Asynchronous Frame Format

INTERNAL REGISTERS

The DACIA contains ten control registers and four status registers in addition to the transmit and receive registers. The Control Registers provide for control of frame parameters, baud rate, interrupt generation, handshake lines, transmission and reception. The status registers provide status information on transmit and receive registers, error conditions and interrupt sources. Table 4 summarizes the bit definitions of these registers. A detailed description follows.

Table 4. Register Formats

Register Select (Hex)	Register	R/$\overline{W}$	Bit 7	6	5	4	3	2	1	0	Reset Value 76543210
0 4	ISR1 ISR2	R	ANY BIT SET	TDRE	$\overline{CTST}$	$\overline{DCDT}$	$\overline{DSRT}$	PAR	F/O/B	RDRF	1 - 00000 -
0 4	IER1 IER2	W	CLR/SET BITS	TDRE IE	$\overline{CTST}$ IE	$\overline{DCDT}$ IE	$\overline{DSRT}$ IE	PAR IE	F/O/B IE	RDRF IE	- 0000000
1 5	CSR1 CSR2	R	FE	TUR	$\overline{CTS}$ LVL	$\overline{DCD}$ LVL	$\overline{DSR}$ LVL	BRK	$\overline{DTR}$ LVL	$\overline{RTS}$ LVL	1 - - - - 011
1 5	CR1 CR2	W	0	CDR/ ACR	STOP BITS	ECHO	BIT RATE SEL				0 - - - - - - -
1 5	FR1 FR2	W	1	DATA BITS		PAR SEL		PAR EN	$\overline{DTR}$ CNTL	$\overline{RTS}$ CNTL	1 - - - - - - -
2 6	CDR1 CDR2	W (CR6 = 0)	COMPARE DATA								- - - - - - - -
2 6	ACR1 ARC2	W (CR6 = 1)	UNUSED						TRNS BRK	PAR ERR/ST	- - - - - - 00
3 7	RDR1 RDR2	R	RECEIVE DATA REGISTER								00000000
3 7	TDR1 TDR2	W	TRANSMIT DATA REGISTER								- - - - - - - -

INTERRUPT STATUS REGISTERS (ISR1, ISR2)

The Interrupt Status Registers are read-only registers indicating the status of each interrupt source. Bits 6 through 0 are set when the indicated $\overline{IRQ}$ condition has occurred. Bit 7 is set to a 1 when any $\overline{IRQ}$ source bit is set, or if Echo Mode is disabled, when $\overline{CTS}$ is high.

7	6	5	4	3	2	1	0
ANY BIT SET	TDRE	$\overline{CTST}$	$\overline{DCDT}$	$\overline{DSRT}$	PAR	F/O/B	RDRF

Address = 0,4 Reset Value = 1 - 00000 -

Bit 7 **Any Bit Set**
- 1 Any bit (6 through 0) has been set to a 1 or $\overline{CTS}$ is high with echo disabled
- 0 No bits have been set to a 1 or echo is enabled

Bit 6 **Transmit Data Register Empty (TDRE)**
- 1 Transmit Data Register is empty and $\overline{CTS}$ is low
- 0 Transmit Data Register is full or $\overline{CTS}$ is high

Bit 5 **Transition On $\overline{CTS}$ Line ($\overline{CTST}$)**
- 1 A positive or negative transition has occurred on $\overline{CTS}$
- 0 No transition has occurred on $\overline{CTS}$, or ISR has been Read

Bit 4 **Transition On $\overline{DCD}$ Line ($\overline{DCDT}$)**
- 1 A positive or negative transition has occurred on $\overline{DCD}$
- 0 No transition has occurred on $\overline{DCD}$, or ISR has been Read

Bit 3 **Transition On $\overline{DSR}$ Line ($\overline{DSRT}$)**
- 1 A positive or negative transition has occurred on $\overline{DSR}$
- 0 No transition has occurred on $\overline{DSR}$, or ISR has been Read

Bit 2 **Parity Status (PAR)**

ACR bit 0 = 0
- 1 A parity error has occurred in received data
- 0 No parity error has occurred, or the Receive Data Register (RDR) has been Read

ACR bit 0 = 1
- 1 Parity bit = 1
- 0 Parity bit = 0

Bit 1 **Frame Error, Overrun, Break**
- 1 A framing error, receive overrun, or receive break has occurred or has been detected
- 0 No error, overrun, break has occurred or RDR has been Read

Bit 0 **Receive Data Register Full (RDRF)**
- 1 Receive Data Register is full
- 0 Receive Data Register is empty

INTERRUPT ENABLE REGISTERS (IER1, IER2)

The Interrupt Enable Registers are write-only registers that enable/disable the $\overline{IRQ}$ sources. $\overline{IRQ}$ sources are enabled by writing to an IER with bit 7 set to a 1 and the bit for every $\overline{IRQ}$ source to be enabled set to a 1. $\overline{IRQ}$ sources are disabled by writing to an IER with bit 7 reset to a 0 and the bit for every source to be disabled set to a 1. Any source bit reset to 0 is unaffected and remains in its original state. Thus, writing $7F to an IER disables all of that channel's interrupts and writing an $FF to an IER enables all of that channel's interrupts.

7	6	5	4	3	2	1	0
SET BITS	TDRE IE	$\overline{CTST}$ IE	$\overline{DCDT}$ IE	$\overline{DSRT}$ IE	PAR IE	F/O/B IE	RDRF IE

Address = 0,4 Reset Value = - 0000000

Bit 7 **Enable/Disable**
- 1 Enable selected IRQ source
- 0 Disable selected IRQ source

Bits 0-6
- 1 Select for enable/disable
- 0 No change

CONTROL STATUS REGISTERS (CSR1, CSR2)

The Control Status Registers are read-only registers that provide I/O status and error condition information. A CSR is normally read after an IRQ has occurred to determine the exact cause of the interrupt condition.

7	6	5	4	3	2	1	0
FE	TUR	$\overline{CTS}$ LVL	$\overline{DCD}$ LVL	$\overline{DSR}$ LVL	BRK	$\overline{DTR}$ LVL	$\overline{RTS}$ LVL

Address = 1,5 Reset Value = 1 - - - - 011

Bit 7 **Framing Error (FE)**
- 1 A framing error occurred in receive data
- 0 No framing error occurred, or the RDR was read

Bit 6 **Transmitter Underrun (TUR)**
- 1 Transmit Shift Register is empty and TDRE is set
- 0 Transmitter Shift Register is not empty

Bit 5 **$\overline{CTS}$ Level ($\overline{CTS}$ LVL)**
- 1 $\overline{CTS}$ line is high
- 0 $\overline{CTS}$ line is low

Bit 4 **$\overline{DCD}$ Level ($\overline{DCD}$ LVL)**
- 1 $\overline{DCD}$ line is high
- 0 $\overline{DCD}$ line is low

Bit 3 **$\overline{DSR}$ Level ($\overline{DSR}$ LVL)**
- 1 $\overline{DSR}$ line is high
- 0 $\overline{DSR}$ line is low

Bit 2 **Receive Break (BRK)**
- 1 A Receive Break has occurred
- 0 No Receive Break occurred, or RDR was read

Bit 1 **$\overline{DTR}$ Level ($\overline{DTR}$ LVL)**
- 1 $\overline{DTR}$ line is high
- 0 $\overline{DTR}$ line is low

Bit 0 **$\overline{RTS}$ Level ($\overline{RTS}$ LVL)**
- 1 $\overline{RTS}$ line is high
- 0 $\overline{RTS}$ line is low

CONTROL REGISTERS (CR1, CR2)

The Control Registers are write-only registers. They control access to the Auxiliary Control Register and the Compare Data Register. They select the number of stop bits, control Echo Mode, and select the data rate.

(Accessed when Bit 7 = 0)

7	6	5	4	3 2 1 0
0	CDR/ACR	STOP BITS	ECHO	BAUD RATE SEL

Address = 1,5 Reset Value = 0 - - - - - - -

Bit 7 **Control or Format Register**
0 Access Control Register

Bit 6 **CDR/ACR**
1 Access the Auxiliary Control Register (ACR)
0 Access the Compare Data Register (CDR)

Bit 5 **Number of Stop Bits Per Character**
1 Two stop bits
0 One stop bit

Bit 4 **Echo Mode Selection**
1 Echo Mode enabled
0 Echo Mode disabled

Bits 3-0 **Baud Rate Selection**

3	2	1	0	(bits per second with 3.6864 MHz crystal)
0	0	0	0	50
0	0	0	1	109.2
0	0	1	0	134.58
0	0	1	1	150
0	1	0	0	300
0	1	0	1	600
0	1	1	0	1200
0	1	1	1	1800
1	0	0	0	2400
1	0	0	1	3600
1	0	1	0	4800
1	0	1	1	7200
1	1	0	0	9600
1	1	0	1	19200
1	1	1	0	38400
1	1	1	1	External TxC and RxC X16 Clocks

FORMAT REGISTERS (FR1, FR2)

The Format Registers are write-only registers. They select the number of data bits per character and parity generation/checking options. They also control $\overline{RTS}$ and $\overline{DTR}$.

(Accessed when Bit 7 = 1)

7	6 5	4 3	2	1	0
1	DATA BITS	PAR SEL	PAR EN	$\overline{DTR}$ CNTL	$\overline{RTS}$ CNTL

Address = 1,5 Reset Value = 1 - - - - - - -

Bit 7 **Control or Format Register**
1 Access Format Register

Bits 6-5 **Number of Data Bits Per Character**

6	5	
0	0	5
0	1	6
1	0	7
1	1	8

Bits 4-3 **Parity Mode Selection**

4	3	
0	0	Odd Parity
0	1	Even Parity
1	0	Mark in Parity bit
1	1	Space in Parity bit

Bit 2 **Parity Enable**
1 Parity as specified by bits 4-3
0 No Parity

Bit 1 **$\overline{DTR}$ Control**
1 Set $\overline{DTR}$ high
0 Set $\overline{DTR}$ low

Bit 0 **$\overline{RTS}$ Control**
1 Set $\overline{RTS}$ high
0 Set $\overline{RTS}$ low

COMPARE DATA REGISTERS (CDR1, CDR2)

The Compare Data Registers are write-only registers which can be accessed when CR bit 6 = 0. By writing a value into the CDR, the DACIA is put in the compare mode. In this mode, setting of the RDRF bit is inhibited until a character is received which matches the value in the CDR. The next character is then received and the RDRF bit is set. The receiver will now operate normally until the CDR is again loaded.

(Control Register bit 6 = 0)

7	6	5	4	3	2	1	0
COMPARE DATA							

Address = 2,6 Reset Value = - - - - - - - -

AUXILIARY CONTROL REGISTERS (ACR1, ACR2)

The Auxiliary Control Registers are write-only registers. Bits 7-2 are unused. Bit 1 causes the transmitter to transmit a BREAK. Bit 0 determines whether parity error or the parity bit is displayed in ISR bit 2.

(Control Register bit 6 = 1)

7	6	5	4	3	2	1	0
NOT USED						TRNS BRK	PAR ERR/ST

Address = 2,6 Reset Value = - - - - - - 00

Bits 7-2 **Not Used**

Bit 1 **Transmit Break (TRNS BRK)**
1 Transmit continuous Break
0 Normal transmission

Bit 0 **Parity Error/State (PAR ERR/ST)**
1 Send value of parity bit to ISR bit 2 (Address Recognition mode)
0 Send Parity Error status to ISR bit 2

RECEIVE DATA REGISTERS (RDR1, RDR2)

The Receive Data Registers are read-only registers which are loaded with the received data character of each frame. Start bits, stop bits and parity bits are stripped off of incoming frames before the data is transferred from the Receive Shift Register to the Receive Data Register. For characters of less than eight bits, the unused bits are the high order bits which are set to 0.

MSB **LSB**

7	6	5	4	3	2	1	0
RECEIVE DATA							

Address = 3,7 Reset Value = 00000000

TRANSMIT DATA REGISTERS (TDR1, TDR2)

The Transmit Data Registers are write-only registers which are loaded from the CPU with data to be transmitted. For data characters of less than eight bits, the unused bits are the high order bits which are "don't care".

MSB **LSB**

7	6	5	4	3	2	1	0
TRANSMIT DATA							

Address = 3,7 Reset Value = - - - - - - - -

OPERATION

TERMINATION OF UNUSED INPUTS

Noise on floating inputs can affect chip operation. All unused inputs must be terminated. If the baud rate generator is bypassed, XTALI must be connected to ground (XTALO is an output and must be left open). If the external clock mode is not used, RxC and TxC may be tied either to +5V or to ground. If the handshake inputs are not needed, the $\overline{CTS}$ inputs should be tied low to enable the transmitters. The $\overline{DCD}$ and $\overline{DSR}$ inputs may either be tied high or low.

RESET INITIALIZATION

During power on initialization, all readable registers should be read to assure that the status registers are initialized. Specifically, the RDRF bit of the Interrupt Status Registers is not initialized by reset. The Receiver Data Registers must be read to clear this bit.

BAUD RATE CLOCK OPTIONS

The receiver and transmitter clocks may be supplied either by the internal Baud Rate Generator or by user supplied external clocks. Both channels may use the same clock source or one may use the Baud Rate Generator and the other channel external clocks. If both channels use the Baud Rate Generator, each channel may have a different bit rate. The options are shown in Figure 5.

An internal clock oscillator supplies the time base for the Baud Rate Generator. The oscillator can be driven by a crystal or an external clock.

If the on-chip oscillator is driven by a crystal, a parallel resonant crystal is connected between the XTALI and XTALO pins. The equivalent oscillator circuit is shown in Figure 6.

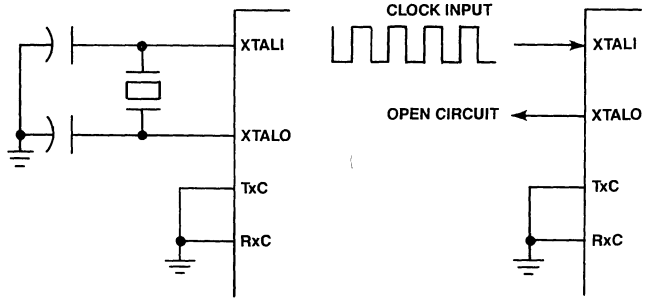
A parallel resonant crystal is specified by its load capacitance and series resonant resistance. For proper oscillator operation, the load capacitance (C_L), series resistance (R_s) and the crystal resonant frequency (F) must meet the following two relations:

$$(C + 2) = 2C_L \quad \text{or} \quad C = 2C_L - 2$$

$$R_s \leq R_{smax} = \frac{2 \times 10^6}{(FC_L)^2}$$

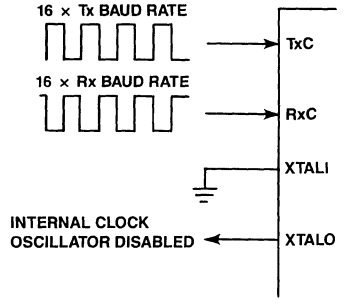
where: F is in MHz; C and C_L are in pF; R is in ohms.

To select a parallel resonant crystal for the oscillator, first select the load capacitance from a crystal manufacturer's catalog. Next, calculate R_{smax} based on F and C_L. The selected crystal must have a R_s less than the R_{smax}.



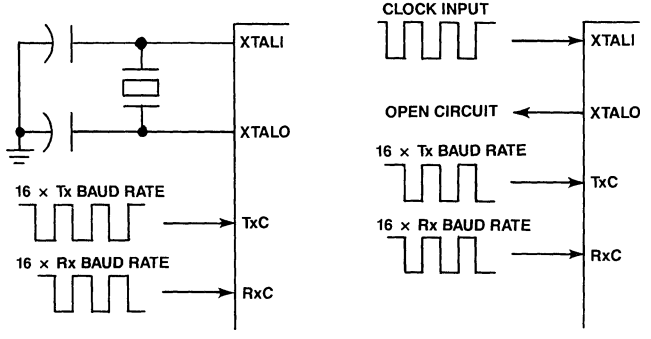
- Baud rate determined by XTALI frequency and 1 of 15 divisors selected in CR1 and CR2. CR1 and CR2 must not be set to all ones.
- Channel 1 baud rate may be different from channel 2 baud rate.
- Receiver baud rate must be the same as transmitter baud rate.

A. Both Channels Use Internal Baud Rate Generator



- Transmitter baud rate 1/16 TxC input frequency.
- Receiver baud rate 1/16 RxC input frequency.
- Channel 1 baud rate is the same as channel 2 baud rate.
- Receiver baud rate may be different from transmitter baud rate.
- Bits 3-0 of CR1 and CR2 must be set to all ones.

B. Both Channels Use External Clocks



- Channel 1 baud rate may be different from channel 2 baud rate.
- Transmitter baud rate may be different from receiver baud rate on channel using external clock.

C. One Channel Uses Internal Baud Rate Generator; One Channel Uses External Clocks

Figure 5. Baud Rate Clock Options

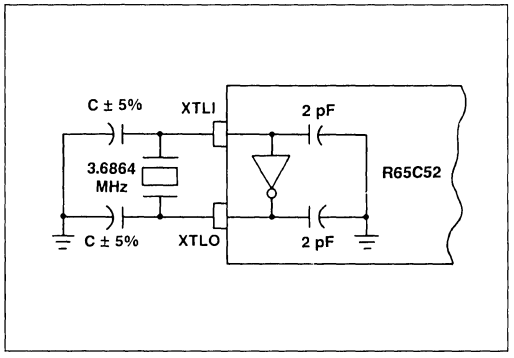


Figure 6.

For example, if C_L = 22 pF for a 3.6864 MHz parallel resonant crystal, then

$C = (2 \times 22) - 2 = 42$ pF (use standard value of 43 pF)

The series resistance of the crystal must be less than

$$R_{smax} = \frac{2 \times 10^6}{(3.6864 \times 22)^2} = 304 \text{ ohms}$$

If the on-chip oscillator is driven by an external clock, the clock is input at XTALI and XTALO is left open.

An internal counter/divider circuit divides the frequency input at XTALI by the divisor selected in bits 3 through 0 of the Control Registers. Table 5 lists the divisors that may be selected and shows the bit rates generated with a 3.6864 MHz crystal or clock input. Other bit rates may be generated by changing the clock or crystal frequency. However, the input frequency must not exceed 4 MHz.

For external clock operation, a transmitter times 16 clock must be supplied at TxC and a receiver times 16 clock must be input at RxC. Since there are separate receiver and transmitter clock inputs, the receiver data rate may be different from the transmitter data rate.

Table 5. Baud Rate Generator Divisor Selection

Control Register Bits				Divisor Selected For The Internal Counter	Baud Rate Generated With 3.6864 MHz Crystal or Clock	Baud Rate Generated* With a Crystal or Clock of Frequency (f)
3	2	1	0			
0	0	0	0	73,728	$(3.6864 \times 10^6)/73{,}728 = 50$	f/73,728
0	0	0	1	33,538	$(3.6864 \times 10^6)/33{,}538 = 109.92$	f/33,538
0	0	1	0	27,408	$(3.6864 \times 10^6)/27{,}408 = 134.58$	f/27,408
0	0	1	1	24,576	$(3.6864 \times 10^6)/24{,}576 = 150$	f/24,576
0	1	0	0	12,288	$(3.6864 \times 10^6)/12{,}288 = 300$	f/12,288
0	1	0	1	6,144	$(3.6864 \times 10^6)/6{,}144 = 600$	f/6,144
0	1	1	0	3,072	$(3.6864 \times 10^6)/3{,}072 = 1{,}200$	f/3,072
0	1	1	1	2,048	$(3.6864 \times 10^6)/2{,}048 = 1{,}800$	f/2,048
1	0	0	0	1,536	$(3.6864 \times 10^6)/1{,}536 = 2{,}400$	f/1,536
1	0	0	1	1,024	$(3.6864 \times 10^6)/1{,}024 = 3{,}600$	f/1,024
1	0	1	0	768	$(3.6864 \times 10^6)/768 = 4{,}800$	f/768
1	0	1	1	512	$(3.6864 \times 10^6)/512 = 7{,}200$	f/512
1	1	0	0	384	$(3.6864 \times 10^6)/384 = 9{,}600$	f/384
1	1	0	1	192	$(3.6864 \times 10^6)/192 = 19{,}200$	f/192
1	1	1	0	96	$(3.6864 \times 10^6)/96 = 38{,}400$	f/96
1	1	1	1	16	Transmitter Baud Rate = TxC/16	Receiver Baud Rate = RxC/16

*Baud Rate = $\frac{\text{Frequency}}{\text{Divisor}}$

CONTINUOUS DATA TRANSMIT

In the normal operating mode, the TDRE bit in the ISR signals the MPU that the DACIA is ready to accept the next data word. An $\overline{IRQ}$ occurs if the corresponding TDRE IRQ enable bit is set in the IER. The TDRE bit is set at the beginning of the start bit. When the MPU writes a word to the TDR the TDRE bit is cleared. In order to maintain continuous transmission the TDR must be loaded before the stop bit(s) are ended. Figure 7 shows the relationship between $\overline{IRQ}$ and TxD for the Continuous Data Transmit mode.

CAUTION:

When the Baud Rate Generator is the clock source, writing to the Format or Control Register of a channel with an active transmitter can result in loss of data. Do not write to the Control or Format Register when the transmitter is shifting out data. This precaution does not apply to channels using the external clock option, i.e., TxC.

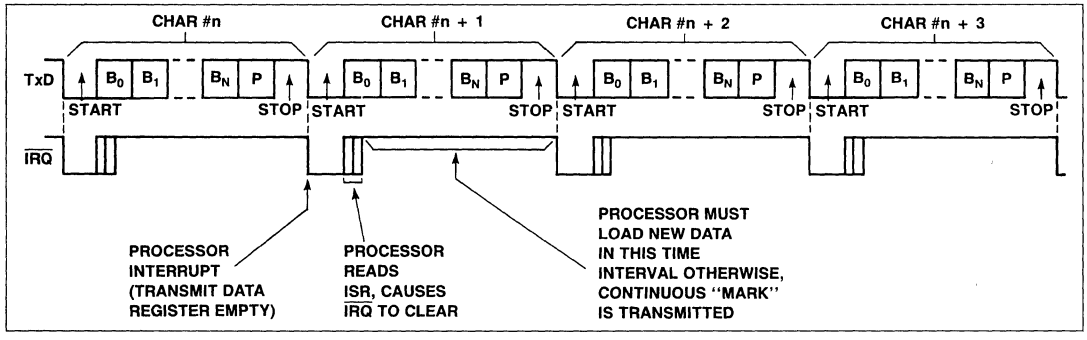


Figure 7. Continuous Data Transmit

TRANSMIT UNDERRUN CONDITION

If the MPU is unable to load the TDR before the last stop bit is sent, the TxD line goes to the MARK condition and the underrun flag (TUR) is set. This condition persists until the TDR is loaded with a new word. Figure 8 shows the relation between $\overline{IRQ}$ and TxD for the Transmit Underrun Condition.

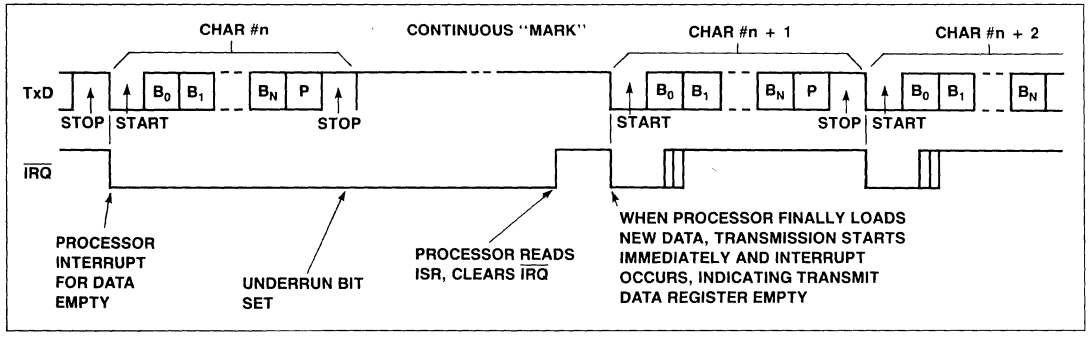


Figure 8. Transmit Underrun Condition Relationship

TRANSMIT BREAK CHARACTER

A BREAK may be transmitted by setting bit 1 of the ACR (Transmit Break bit) to a 1. The BREAK is transmitted after the character in the Transmit Shift Register is sent. If there is a character in the Transmit Data Register, it will be transmitted after the BREAK is terminated. The Transmit Break bit must remain set for at least one character time to assure that a proper BREAK is transmitted. If the Transmit Break bit is cleared before one character time of BREAK has been transmitted, the BREAK will be terminated after one character time has elapsed. If the Transmit Break bit is cleared after one character time of BREAK has been transmitted, the BREAK will be terminated immediately. Figure 9 shows the relationship of TxD, $\overline{IRQ}$ and ACR bit 1 for various BREAK options.

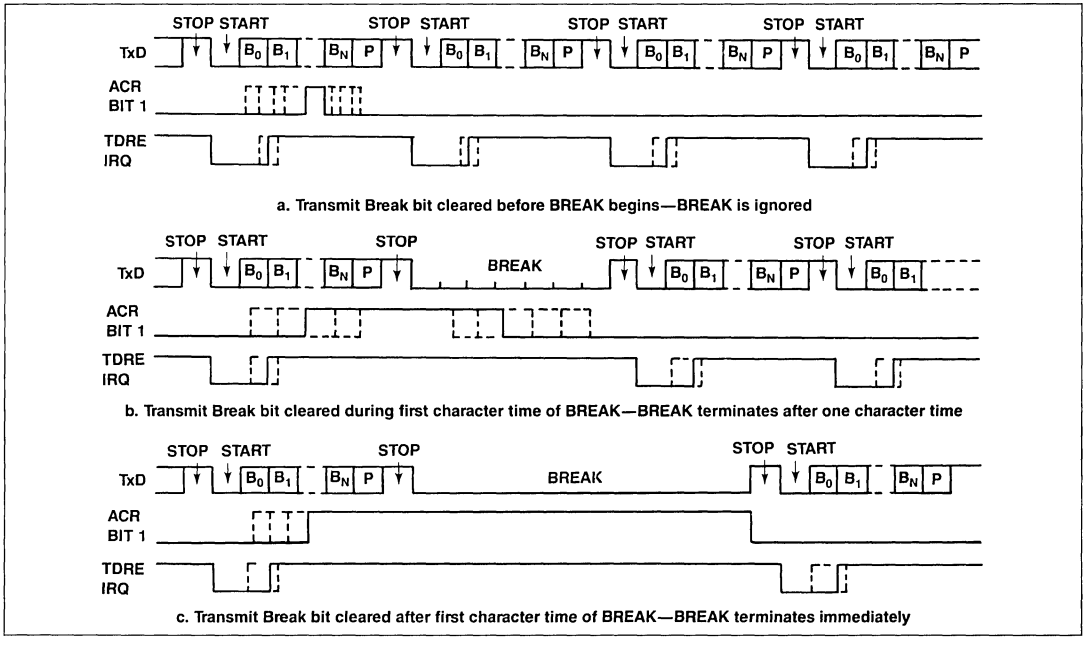


Figure 9. Transmit BREAK

EFFECTS OF $\overline{CTS}$ ON TRANSMITTER

The $\overline{CTS}$ control line controls the transmission of data or the handshaking of data to a "busy" device (such as a printer). When the $\overline{CTS}$ line is low, the transmitter operates normally. A high condition inhibits the TDRE bit in the ISR from becoming set. Transmission of the word currently in the shift register is completed but any word in the TDR is held until $\overline{CTS}$ goes low.

Any transition on $\overline{CTS}$ sets bit 5 ($\overline{CTS}$T) of the ISR. A high on $\overline{CTS}$ forces bit 6 (TDRE) of the ISR to a 0. Bit 7 of the ISR also goes to a 1 when $\overline{CTS}$ is high, if Echo Mode is disabled. Thus, when the ISR is $80, it means that $\overline{CTS}$ is high and no interrupt source requires service. A processor interrupt will not be generated under these circumstances, but an ISR polling routine should accommodate this.

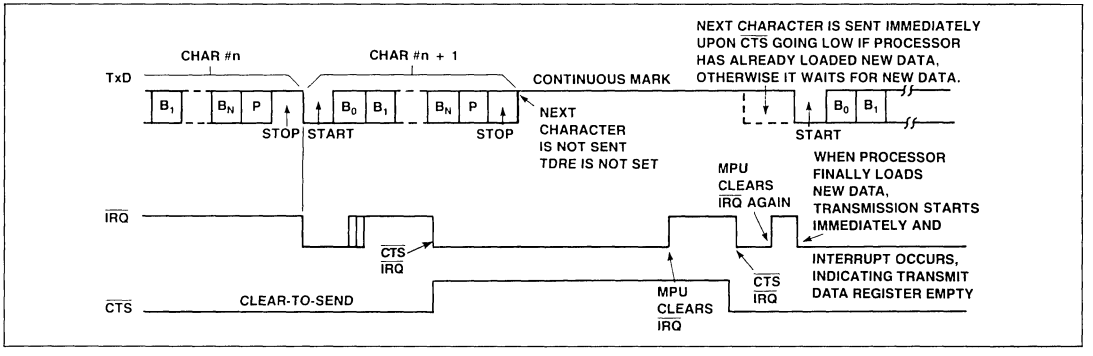


Figure 10. Effects of $\overline{CTS}$ on Transmitter

ECHO MODE TIMING

In the Echo Mode, the TxD line re-transmits the data received on the RxD line, delayed by 1/2 of a bit time. An internal underrun mode must occur before Echo Mode will start transmitting. In normal transmit mode if TDRE occurs (indicating end of data) an underflow flag would be set and continuous Mark transmitted. If Echo is initiated, the underflow flag will not be set at end of data and continuous Mark will not be transmitted. Figure 11 shows the relationship of RxD and TxD for Echo Mode.

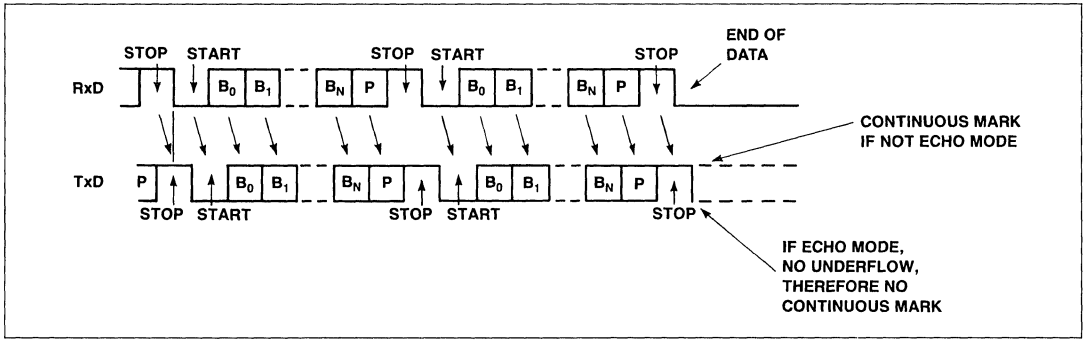


Figure 11. Echo Mode Timing

CONTINUOUS DATA RECEIVE

The normal receive mode sets the RDRF bit in the ISR when the DACIA channel has received a full data word. This occurs at about the 9/16 point through the stop bit. The processor must read the RDR before the next stop bit, or an overrun error occurs. Figure 12 shows the relationship between $\overline{IRQ}$ and RxD for the continuous Data Receive mode.

CAUTION:

When the Baud Rate Generator is the clock source, writing to the Control or Format Registers of a channel with an active receiver can result in loss of data. Do not write to the Control or Format Registers when the receiver is shifting in data. This precaution is not necessary on channels using the external clock option, i.e., RxC.

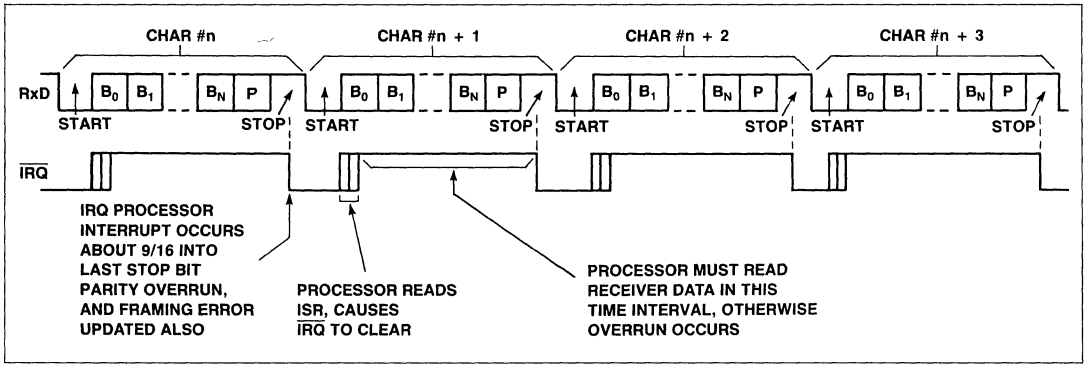


Figure 12. Continuous Data Receive

EFFECTS OF OVERRUN ON RECEIVER

If the processor does not read the RDR before the stop bit of the next word, an overrun error occurs, the overrun bit is set in the ISR, and the new data word is not transferred to the RDR. The RDR contains the last word not read by the MPU and all following data is lost. The receiver will return to normal operation when the RDR is read. Figure 13 shows the relationship of $\overline{IRQ}$ and RxD when overrun occurs.

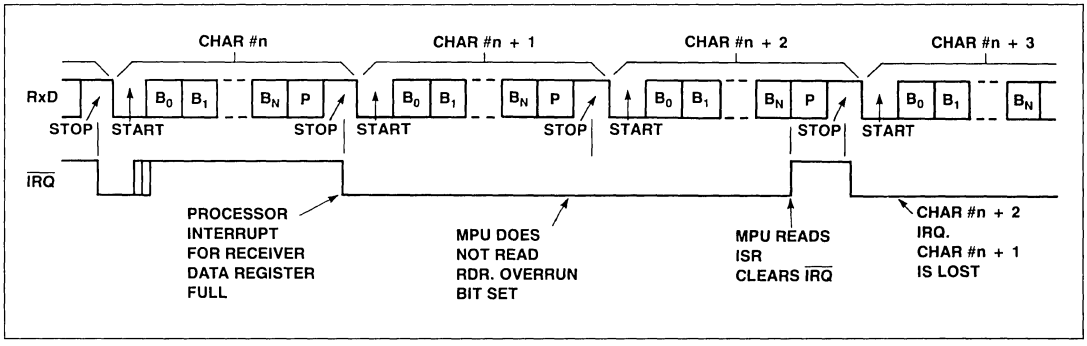


Figure 13. Effects of Overrun on Receiver

RECEIVE BREAK CHARACTER

In the event that a Break character is received by the receiver, the Break bit is set. The receiver does not set the RDRF bit and remains in this state until a stop bit is received. At this time the next character is to be received normally. Figure 14 shows the relationship of $\overline{IRQ}$ and RxD for a Receive Break Character.

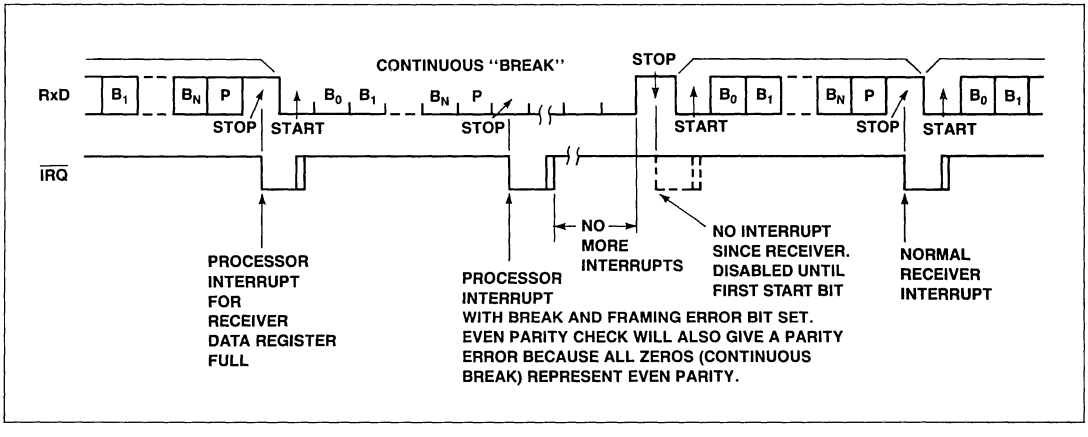


Figure 14. Receive Break Character

FRAMING ERROR

Framing error is caused by the absence of stop bit(s) on received data. The framing error bit is set when the RDRF bit is set. Subsequent data words are tested separately, so the status bit always reflects the last data word received. Figure 15 shows the relationship of $\overline{IRQ}$ and RxD when a framing error occurs.

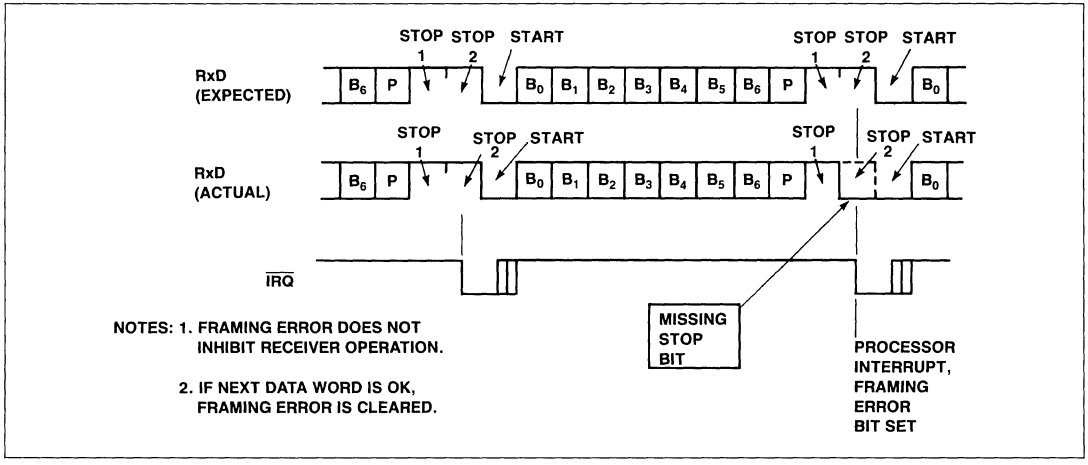


Figure 15. Framing Error

PARITY ERROR DETECT/ADDRESS FRAME RECOGNITION

The Parity Status bit (ISR bit 2) may be programmed to indicate parity errors (ACR bit 0 = 0) or to display the parity bit received (ACR bit 0 = 1).

In applications where parity checking is used, one of the parity checking modes is enabled by setting bits 2, 3 and 4 of the Format Register to the desired option and bit 0 of the Auxiliary Control Register is reset to 0. Then, when the RDRF bit (bit 0) is set in the ISR, the PAR bit (bit 2) will be set when a parity error is detected.

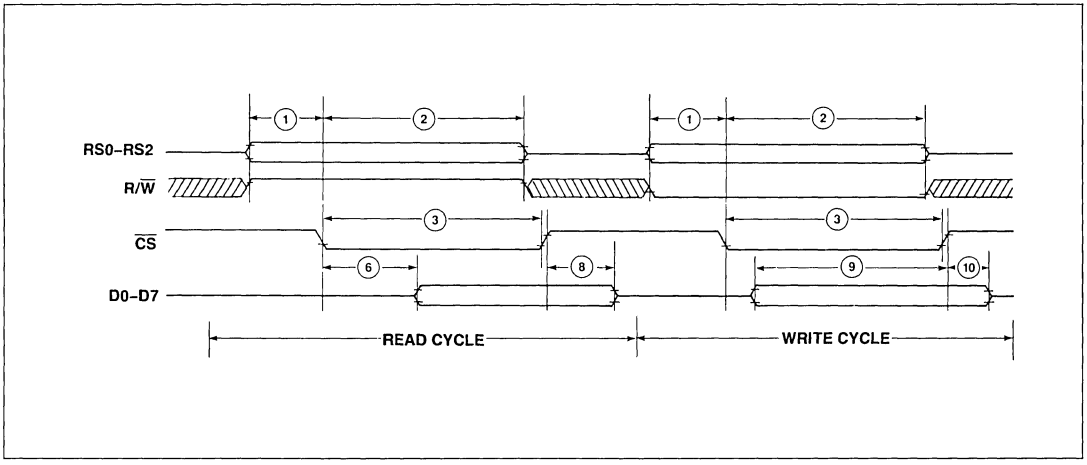
In multi-drop applications, the parity bit is used as an address/data flag. It is set to 1 for address frames and is 0 on data frames. For this type of operation, bit 0 of the ACR is set to a 1 and bits 2, 3 and 4 of the FR select a parity checking mode. Then, ISR bit 2 will be set to a 1 by incoming address frames and it will be a 0 on data frames.

COMPARE MODE

The Compare Mode is automatically enabled, i.e., the channel is put to sleep, whenever data is written to the Compare Data Register. NOTE: Bit 6 of the Control Register must be set to 0 to enable access to the Compare Data Register. When the channel is in the compare mode, the RDRF bit (bit 0 of the ISR) is forced to a 0. Upon receipt of a matching character, normal receiver operation resumes and the RDRF bit (bit 0 of the ISR) will be set upon receipt of the *next* character.

SPECIFICATIONS

DACIA READ/WRITE WAVEFORMS

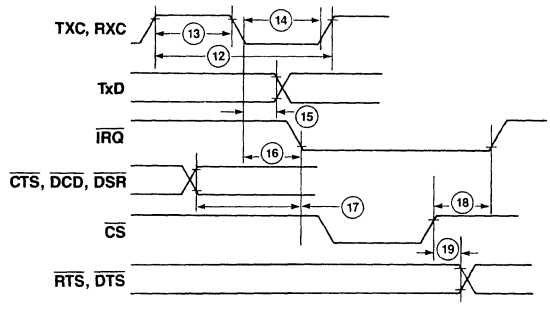


DACIA READ/WRITE CYCLE TIMING

(V_{CC} = 5 Vdc ±5%, V_{SS} = 0 Vdc, T_A = T_L to T_H, unless otherwise noted)

Number	Characteristic	Symbol	1 MHz		2 MHz		3 MHz		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
1	R/$\overline{W}$, RS0–RS2 Valid to $\overline{CS}$ Low (Setup)	T_{RSU}	0	—	0	—	0	—	ns
2	$\overline{CS}$ Low to R/$\overline{W}$, RS0–RS2 Invalid (Hold)	T_{RH}	45	—	45	—	45	—	ns
3	$\overline{CS}$ Pulse Width	T_{CP}	640	—	320	—	210	—	ns
6	$\overline{CS}$ Low to Data Valid (Read)	T_{CDV}	—	340	—	245	—	210	ns
8	$\overline{CS}$ High to Data Invalid (Read)	T_{CDR}	10	50	10	50	10	50	ns
9	Data Valid to $\overline{CS}$ High (Write, Setup)	T_{DSU}	20	—	20	—	20	—	ns
10	$\overline{CS}$ High to Data Invalid (Write Hold)	T_{CDW}	30	—	30	—	30	—	ns

DACIA TRANSMIT/RECEIVER WAVEFORMS



TRANSMIT/RECEIVE AND INTERRUPT ACKNOWLEDGE TIMING

(V_{CC} = 5 Vdc ±5%, V_{SS} = 0 Vdc, T_A = T_L to T_H, unless otherwise noted)

Number	Characteristic	Symbol	Min.	Max.	Unit
TRANSMIT/RECEIVE TIMING					
12	Transmit/Receive Clock Rate	t_{CY}	250	—	ns
13	Transmit/Receive Clock High	t_{CH}	100	—	ns
14	Transmit/Receive Clock Low	t_{CL}	100	—	ns
15	TxC, RxC to TxD Propagation Delay	t_{DD}	—	285	ns
16	TxC, RxC to $\overline{IRQ}$ Propagation Delay	t_{DI}	—	250	ns
17	$\overline{CTS}$, $\overline{DCD}$, $\overline{DSR}$ Valid to $\overline{IRQ}$ Low	t_{CTI}	—	150	ns
18	$\overline{IRQ}$ Propagation Delay (Clear)	t_{IRQ}	—	150	ns
19	$\overline{RTS}$, $\overline{DTR}$ Propagation Delay	t_{DLY}	—	150	ns

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to +7.0	Vdc
Input Voltage	V_{IN}	−0.3 to V_{CC} +0.3	Vdc
Output Voltage	V_{OUT}	−0.3 to V_{CC} +0.3	Vdc
Operating Temperature Commercial Industrial	T_A	 0 to +70 −40 to +85	°C
Storage Temperature	T_{STG}	−55 to +150	°C

*NOTE: Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in other sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING CONDITIONS

Parameter	Symbol	Value
Supply Voltage	V_{CC}	5V ± 5%
Temperature Range Commercial Industrial	T_A	 0 to 70°C −40°C to +85°C

DC CHARACTERISTICS

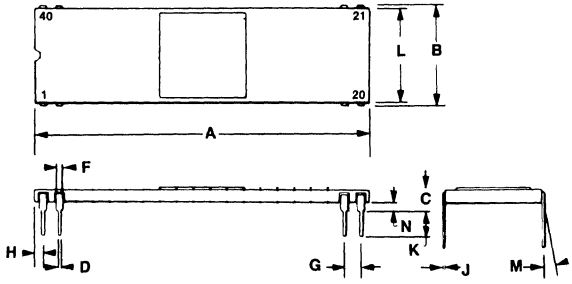
(V_{CC} = 5.0 V ±5%, V_{SS} = 0, T_A = T_L to T_H, unless otherwise noted)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input High Voltage Except XTALI and XTALO XTALI and XTALO	V_{IH}	 +2.0 +2.4	 — —	 V_{CC} + 0.3 V_{CC} + 0.3	V	
Input Low Voltage Except XTALI and XTALO XTALI and XTALO	V_{IL}	 −0.3 −0.3	 — —	 +0.8 +0.4	V	
Input Leakage Current R/$\overline{W}$, $\overline{RES}$, RS0, RS1, RS2, RxD, $\overline{CTS}$, $\overline{DCD}$, $\overline{DSR}$, RxC, TxC, $\overline{CS}$	I_{IN}	—	10	50	μA	V_{IN} = 0V to 5.0V V_{CC} = 5.25V
Input Leakage Current for Three-State Off D0–D7	I_{TSI}	—	±2	10	μA	V_{IN} = 0.4V to 2.4V V_{CC} = 5.25V
Output High Voltage D0–D7, TxD, CLK OUT, RTS, DTR	V_{OH}	+2.4	—	—	V	V_{CC} = 4.75V I_{LOAD} = −100 μA
Output Low Voltage D0–D7, TxD, CLK OUT, RTS, DTR	V_{OL}	—	—	+0.4	V	V_{CC} = 4.75V I_{LOAD} = 1.6 mA
Output Leakage Current (Off State) $\overline{IRQ}$	I_{OFF}	—	±2	±10	μA	V_{CC} = 5.25V V_{OUT} = 0 to 2.4V
Power Dissipation	P_D	—	—	10	mW/MHz	
Input Capacitance Except XTALI and XTALO XTALI and XTALO	C_{IN}	 — —	 — —	 5 10	 pF pF	V_{CC} = 5.0V V_{IN} = 0V f = 2 MHz T_A = 25°C
Output Capacitance	C_{OUT}	—		10	pF	

Notes:
1. All units are direct current (dc) except for capacitance.
2. Negative sign indicates outward current flow, positive indicates inward flow.
3. Typical values are shown for V_{CC} = 5.0V and T_A = 25°C.

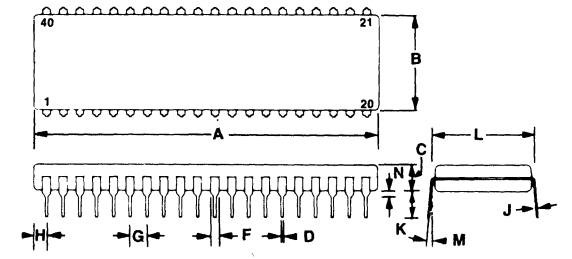
PACKAGE DIMENSIONS

40-PIN CERAMIC DIP



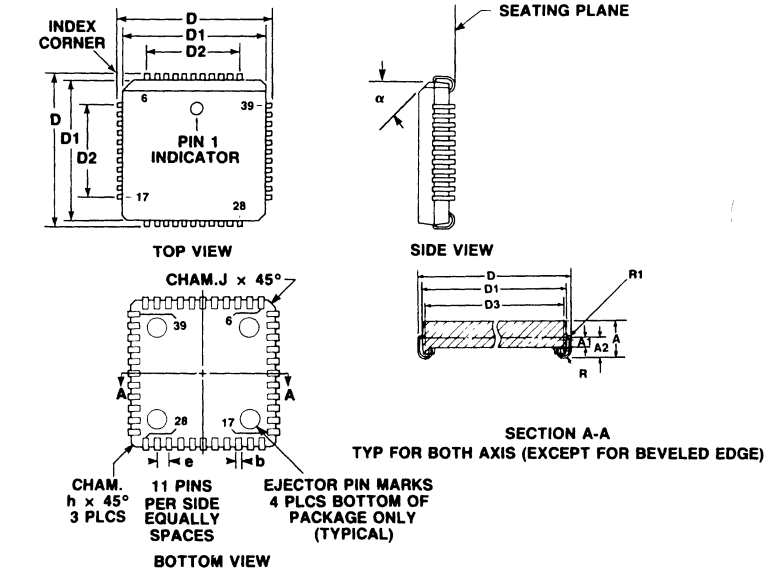
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	50.29	51.31	1.980	2.020
B	15.11	15.88	0.595	0.625
C	2.54	4.19	0.100	0.165
D	0.38	0.53	0.015	0.021
F	0.76	1.27	0.030	0.050
G	2.54 BSC		0.100 BSC	
H	0.76	1.78	0.030	0.070
J	0.20	0.33	0.008	0.013
K	2.54	4.19	0.100	0.165
L	14.60	15.37	0.575	0.605
M	0°	10°	0°	10°
N	0.51	1.52	0.020	0.060

40-PIN PLASTIC DIP



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	51.82	52.32	2.040	2.060
B	13.46	13.97	0.530	0.550
C	3.56	5.08	0.140	0.200
D	0.38	0.53	0.015	0.021
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.30	0.008	0.012
K	3.30	4.32	0.130	0.170
L	15.24 BSC		0.600 BSC	
M	7°	10°	7°	10°
N	0.51	1.02	0.020	0.040

44-PIN PLASTIC LEADED CHIP CARRIER (PLCC)



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.14	4.39	0.163	0.173
A1	1.37	1.47	0.054	0.058
A2	2.31	2.46	0.091	0.097
b	0.457 TYP		0.018 TYP	
D	17.45	17.60	0.687	0.693
D1	16.46	16.56	0.648	0.652
D2	12.62	12.78	0.497	0.503
D3	15.75 REF		0.620 REF	
e	1.27 BSC		0.050 BSC	
h	1.15 TYP		0.045 TYP	
J	0.25 TYP		0.010 TYP	
α	45° TYP		45° TYP	
R	0.89 TYP		0.035 TYP	
R1	0.25 TYP		0.010 TYP	

Section 2
NMOS 8-Bit Microprocessors & Peripherals

2

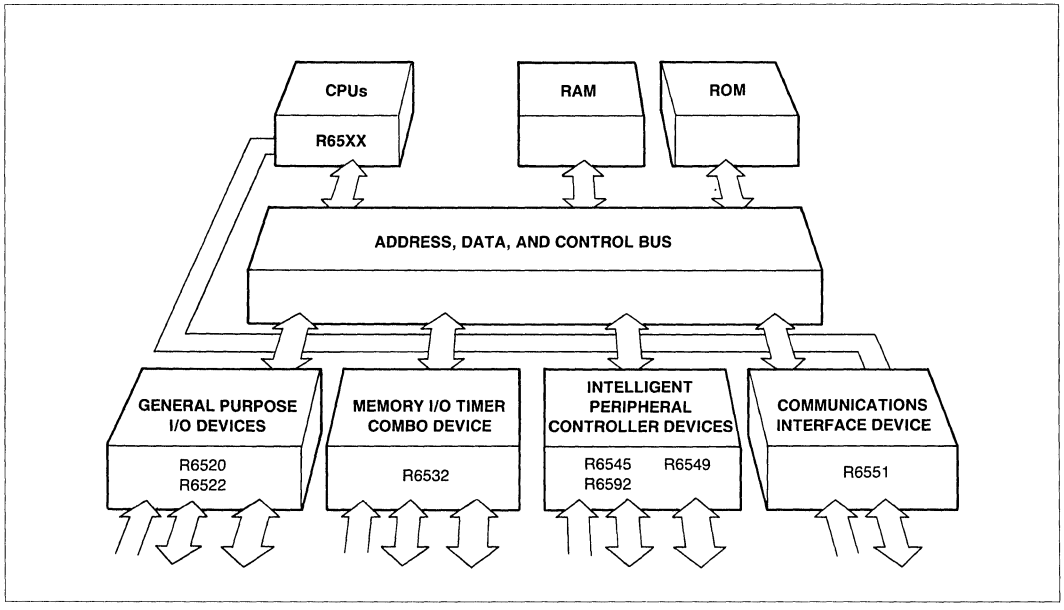
NMOS 8-bit Microprocessors and Peripherals
Largest Selling 8-Bit Family

The NMOS R6500 microprocessor family has a wide range of CPUs and peripheral controllers plus versatile memory-I/O timer combinations. It is software compatible with the CMOS microprocessor and peripheral family, as well as, with the family of single-chip microcomputers.

A parallel processing, pipeline architecture provides faster instruction execution and data throughput. Thirteen address modes provide the most efficient ways of addressing memory.

R6500 peripherals are system oriented and are designed to implement systems with a minimum device count. Fast instruction execution (1 μs and 2 μs) is available in 2 and 1 MHz versions, respectively.

The entire 8-bit R6500 family is upward compatible with the 16-bit 68000 bus, software compatible with the Rockwell 8-bit microcomputers, and are the building blocks for a wide range of system applications.



NMOS R65XX Microprocessor Family

Rockwell

R650X and R651X Microprocessors (CPU)

DESCRIPTION

The 8-bit R6500 microprocessor devices are produced with N-channel, silicon gate technology. Performance speeds are enhanced by advanced system architecture. This innovative architecture results in smaller chips—the semiconductor threshold is cost-effectivity. System cost-effectivity is further enhanced by providing a family of 10 software-compatible microprocessor (CPU) devices, described in this document. Rockwell also provides single chip microcomputers, memory and peripheral devices—as well as low-cost design aids and documentation.

Ten CPU devices are available. All are software-compatible. They provide options of addressable memory, interrupt input, on-chip clock oscillators and drivers. All are bus-compatible with earlier generation microprocessors like the M6800 devices.

The R650X and R651X family includes six microprocessors with on-board clock oscillators and drivers and four microprocessors driven by external clocks. The on-chip clock versions are aimed at high performance, low cost applications where single phase inputs, crystal or RC inputs provide the time base. The external clock versions are geared for multiprocessor system applications where maximum timing control is mandatory. All R6500 microprocessors are also available in a variety of packaging (ceramic and plastic), operating frequency (1 MHz, 2 MHz and 3 MHz) and temperature (commercial and industrial) versions.

ORDERING INFORMATION

Part Number: R65XX___

- Temperature Range (T_L to T_H):
  - No letter = 0°C to +70°C
  - E = −40°C to +85°C
- Package:
  - C = Ceramic DIP
  - P = Plastic DIP
- Frequency Range:
  - No letter = 1 MHz
  - A = 2 MHz
  - B = 3 MHz
- Model Designator:
  - XX = 02, 03, 04, . . . 15

FEATURES

- N-channel, silicon gate, depletion load technology
- 8-bit parallel processing
- 56 instructions
- Decimal and binary arithmetic
- Thirteen addressing modes
- True indexing capability
- Programmable stack pointer
- Variable length stack
- Interrupt request
- Non-maskable interrupt
- Use with any type of speed memory
- 8-bit bidirectional data bus
- Addressable memory range of up to 64K bytes
- "Ready" input
- Direct Memory Access capability
- Bus compatible with M6800
- 1 MHz, 2 MHz, and 3 MHz versions
- Choice of external or on-chip clocks
- On-chip clock options
  - —External single clock input
  - —Crystal time base input
- Commercial and industrial temperature versions
- Pipeline architecture
- Single +5V supply

R6500 CPU FAMILY MEMBERS

Microprocessors with Internal Two Phase Clock Generator

Model	No. Pins	Addressable Memory
R6502	40	64K Bytes
R6503	28	4K Bytes
R6504	28	8K Bytes
R6505	28	4K Bytes
R6506	28	4K Bytes
R6507	28	8K Bytes

Microprocessors with External Two Phase Clock Input

Model	No. Pins	Addressable Memory
R6512	40	64K Bytes
R6513	28	4K Bytes
R6514	28	8K Bytes
R6515	28	4K Bytes

INTERFACE SIGNAL DESCRIPTIONS

CLOCKS (Ø1, Ø2)

The R651X requires a two phase non-overlapping clock that runs at the V_{CC} voltage level. The R650X clocks are supplied with an internal clock generator. The frequency of these clocks is externally controlled.

ADDRESS BUS (A0-A15)

The address line outputs access data in memory device locations or cells, access data in I/O device registers and/or effect logical operations in I/O or controller devices depending on system design. The addressing range is determined by the number of address lines available on the particular CPU device. The R6502 and R6512 can address 64K bytes with a 16-bit address bus (A0-A15); the R6504, R6507, and the R6514 can address 8K bytes with a 13-bit address bus (A0-A12); and the R6503, R6505, R6506, R6513, and R6515 can address 4K bytes with a 12-bit address bus (A0-A11). These outputs are TTL-compatible and are capable of driving one standard TTL load and 130 pF.

DATA BUS (D0-D7)

The data lines (D0-D7) form an 8-bit bidirectional data bus which transfers data between the CPU and memory or peripheral devices. The outputs are tri-state buffers capable of driving one standard TTL load and 130 pF.

DATA BUS ENABLE (DBE, R6512 ONLY)

The TTL-compatible DBE input allows external control of the tri-state data output buffers and will enable the microprocessor bus driver when in the high state. In normal operation DBE is driven by the phase two (Ø2) clock, thus allowing data output from microprocessor only during Ø2. During the read cycle, the data bus drivers are internally disabled, becoming essentially an open circuit. To disable data bus drivers externally, DBE should be held low.

READY (RDY)

The Ready input signal allows the user to halt or single cycle the microprocessor on all cycles except write cycles. A negative transition to the low state during or coincident with phase one (Ø1) will halt the microprocessor with the output address lines reflecting the current address being fetched. If Ready is low during a write cycle, it is ignored until the following read operation. This condition will remain through a subsequent phase two (Ø2) in which the Ready signal is low. This feature allows microprocessor interfacing with the low speed PROMs as well as Direct Memory Access (DMA).

INTERRUPT REQUEST ($\overline{IRQ}$)

The TTL level active-low $\overline{IRQ}$ input requests that an interrupt sequence begin within the microprocessor. The microprocessor will complete the current instruction being executed before recognizing the request. At that time, the interrupt mask bit in the Processor Status Register will be examined. If the interrupt mask flag is not set, the microprocessor will begin an interrupt sequence. The Program Counter and Processor Status Register are stored in the stack. The microprocessor will then set the interrupt mask flag high so that no further interrupts can occur. At the end of this cycle, the program counter low will be loaded from address FFFE, and program counter high from location FFFF, therefore transferring program control to the memory vector located at these addresses. The RDY signal must be in the high state for any interrupt to be recognized. A 3KΩ external resistor should be used for proper wire-OR operation.

NON-MASKABLE INTERRUPT ($\overline{NMI}$)

A negative going edge on the $\overline{NMI}$ input requests that a non-maskable interrupt sequence be generated within the microprocessor.

$\overline{NMI}$ is an unconditional interrupt. Following completion of the current instruction, the sequence of operations defined for $\overline{IRQ}$ will be performed, regardless of the state interrupt mask flag. The vector address loaded into the program counter, low and high, are locations FFFA and FFFB respectively, thereby transferring program control to the memory vector located at these addresses. The instructions loaded at these locations cause the microprocessor to branch to a non-maskable interrupt routine in memory.

$\overline{NMI}$ also requires an external 3KΩ register to V_{CC} for proper wire-OR operations.

Inputs $\overline{IRQ}$ and $\overline{NMI}$ are hardware interrupts lines that are sampled during Ø2 (phase 2) and will begin the appropriate interrupt routine on the Ø1 (phase 1) following the completion of the current instruction.

SET OVERFLOW FLAG ($\overline{SO}$)

A negative going edge on the $\overline{SO}$ input sets the overflow bit in the Processor Status Register. This signal is sampled on the trailing edge of Ø1 and must be externally synchronized.

SYNC

The SYNC output line identifies those cycles in which the microprocessor is doing an OP CODE fetch. The SYNC line goes high during Ø1 of an OP CODE fetch and stays high for the remainder of that cycle. If the RDY line is pulled low during the Ø1 clock pulse in which SYNC went high, the processor will stop in its current state and will remain in the state until the RDY line goes high. In this manner, the SYNC signal can be used to control RDY to cause single instruction execution.

RESET ($\overline{RES}$)

The active low $\overline{RES}$ resets, or starts, the microprocessor from a power down or restart condition. During the time that this line is held low, writing to or from the microprocessor is inhibited. When a positive edge is detected on the input, the microprocessor will immediately begin the reset sequence.

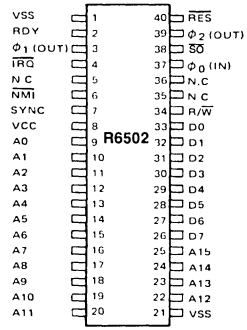
After a system initialization time of six clock cycles, the mask interrupt flag is set and the microprocessor loads the program counter from the memory vector locations FFFC and FFFD. This is the start location for program control.

After V_{CC} reaches 4.75 volts in a power up routine, reset must be held low for at least two clock cycles. At this time the R/$\overline{W}$ and SYNC signals become valid.

2

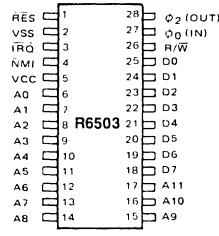
R6502 FEATURES

- 64K addressable bytes of memory (A0–A15)
- On-chip clock
  TTL-level single phase input
  RC time base input
  crystal time base input
- Two phase output clock for timing of support chips
- $\overline{IRQ}$ interrupt
- $\overline{NMI}$ interrupt
- RDY signal
- SYNC signal
  (can be used for single instruction execution)
- 40-pin DIP



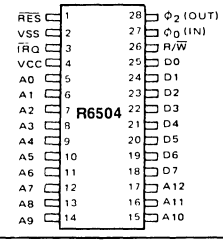
R6503 FEATURES

- 4K addressable bytes of memory (A0-A11)
- On-chip clock
- $\overline{IRQ}$ interrupt
- $\overline{NMI}$ interrupt
- 28-pin DIP



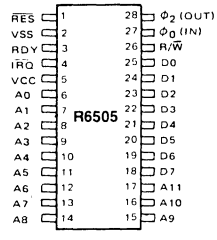
R6504 FEATURES

- 8K addressable bytes of memory (A0-A12)
- On-chip clock
- $\overline{IRQ}$ interrupt
- 28-pin DIP



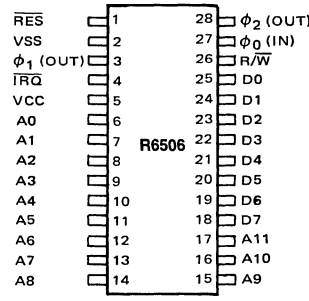
R6505 FEATURES

- 4K addressable bytes of memory (A0-A11)
- On-chip clock
- $\overline{IRQ}$ interrupt
- RDY signal
- 28-pin DIP



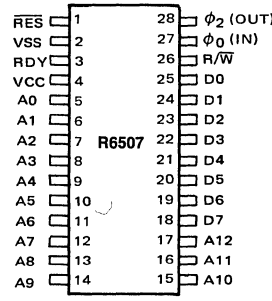
R6506 FEATURES

- 4K addressable bytes of memory (A0–A11)
- On-chip clock
- Two phase output clock for timing of support chips
- $\overline{IRQ}$ interrupt
- 28-pin DIP



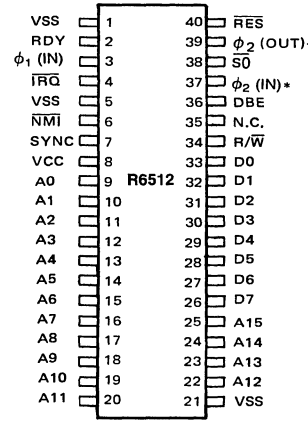
R6507 FEATURES

- 8K addressable bytes of memory (A0-A12)
- On-chip clock
- RDY signal
- 28-pin DIP



R6512 FEATURES

- 64K addressable bytes of memory (A0–A15)
- Two phase clock input
- $\overline{IRQ}$ interrupt
- $\overline{NMI}$ interrupt
- RDY signal
- SYNC signal
- Data Bus Enable
- 40-pin DIP

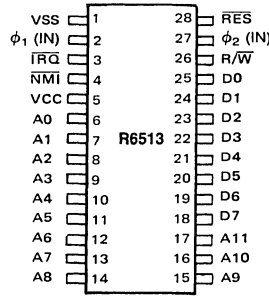


*Pins 37 and 39 are connected internally

2

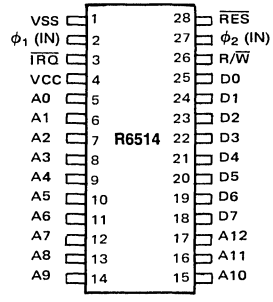
R6513 FEATURES

- 4K addressable bytes of memory (A0-A11)
- Two phase clock input
- $\overline{IRQ}$ interrupt
- $\overline{NMI}$ interrupt
- 28-pin DIP



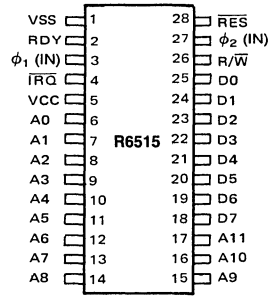
R6514 FEATURES

- 8K addressable bytes of memory (A0-A12)
- Two phase clock input
- $\overline{IRQ}$ interrupt
- 28-pin DIP



R6515 FEATURES

- 4K addressable bytes of memory (A0-A11)
- Two phase clock input
- $\overline{IRQ}$ interrupt
- RDY signal
- 28-pin DIP



FUNCTIONAL DESCRIPTION

The internal organization of all R6500 CPUs is identical except for some variations in clock interface, the number of address output lines, and some unique input/output lines between versions.

CLOCK GENERATOR

The clock generator develops all internal clock signals, and (where applicable) external clock signals, associated with the device. It is the clock generator that drives the timing control unit and the external timing for slave mode operations.

TIMING CONTROL

The timing control unit keeps track of the instruction cycle being monitored. The unit is set to zero each time an instruction fetch is executed and is advanced at the beginning of each phase one clock pulse for as many cycles as is required to complete the instruction. Each data transfer which takes place between the registers depends upon decoding the contents of both the instruction register and the timing control unit.

PROGRAM COUNTER

The 16-bit program counter provides the addresses which step the microprocessor through sequential instructions in a program.

Each time the microprocessor fetches an instruction from program memory, the lower byte of the program counter (PCL) is placed on the low-order bits of the address bus and the higher byte of the program counter (PCH) is placed on the high-order 8 bits. The counter is incremented each time an instruction or data is fetched fromprogram memory.

INSTRUCTION REGISTER AND DECODE

Instructions fetched from memory are gated onto the internal data bus. These instructions are latched into the instuction register, then decoded, along with timing and interrupt signals, to generate control signals for the various registers.

ARITHMETIC AND LOGIC UNIT (ALU)

All arithmetic and logic operations take place in the ALU including incrementing and decrementing internal registers (except the program counter). The ALU has no internal memory and is used only to perform logical and transient numerical operations.

ACCUMULATOR

The accumulator is a general purpose 8-bit register that stores the results of most arithmetic and logic operations, and in addition, the accumulator usually contains one of the two data words used in these operations.

INDEX REGISTERS

There are two 8-bit index registers (X and Y), which may be used to count program steps or to provide an index value to be used in generating an effective address.

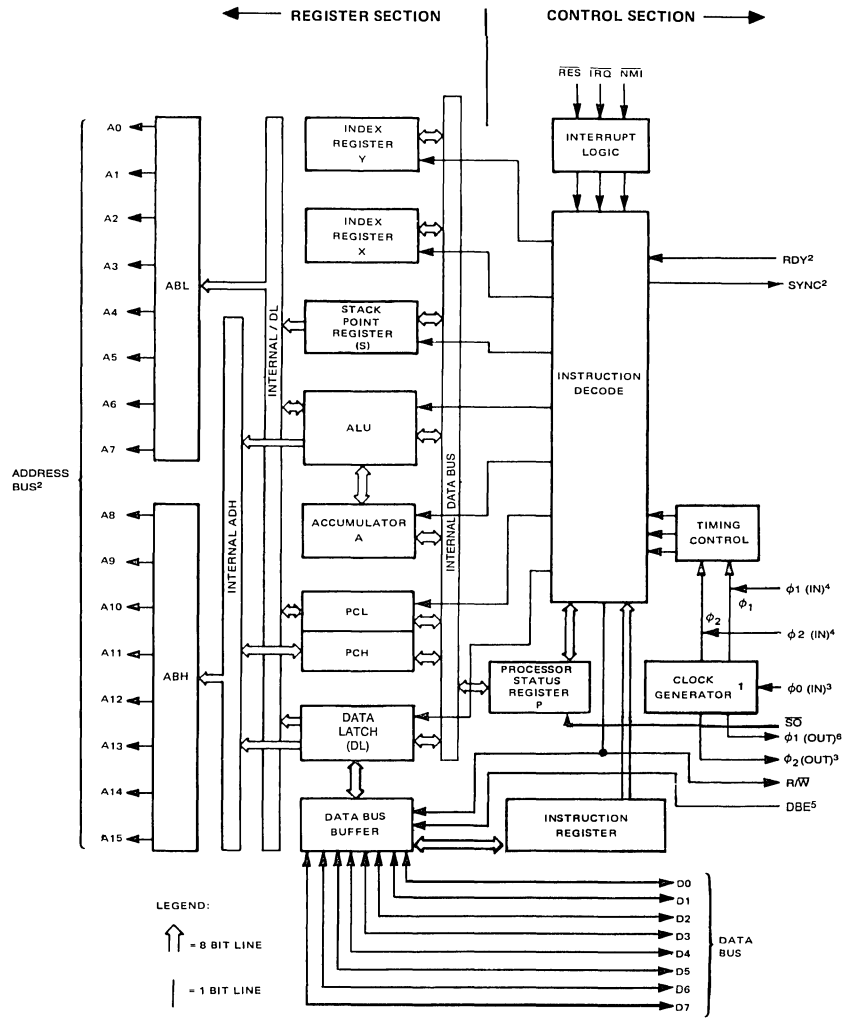
When executing an instruction which specifies indexed addressing, the CPU fetches the op code and the base address, and modifies the address by adding the index register to it prior to performing the desired operation. Pre- or post-indexing of indirect addresses is possible (see addressing modes).

STACK POINTER

The stack pointer is an 8-bit register used to control the addressing of the variable-length stack on page one. The stack pointer is automatically incremented and decremented under control of the microprocessor to perform stack manipulations under direction of either the program or interrupts ($\overline{NMI}$) and $\overline{IRQ}$). The stack allows simple implementation of nested subroutines and multiple level interrupts. The stack pointer should be initialized before any interrupts or stack operations occur.

PROCESSOR STATUS REGISTER

The 8-bit processor status register contains seven status flags. Some of the flags are controlled by the program, others may be controlled both by the program and the CPU.



NOTE

1. CLOCK GENERATOR IS NOT INCLUDED ON R6512, R6513, R6514 AND R6515.
2. ADDRESSING CAPABILITY AND CONTROL OPTIONS VARY WITH EACH OF THE CPUs.
3. R6502, R6503, R6504, R6505, R6506 AND R6507.
4. R6512, R6513, R6514 AND R6515.
5. R6512 ONLY.
6. R6502 AND R6506.

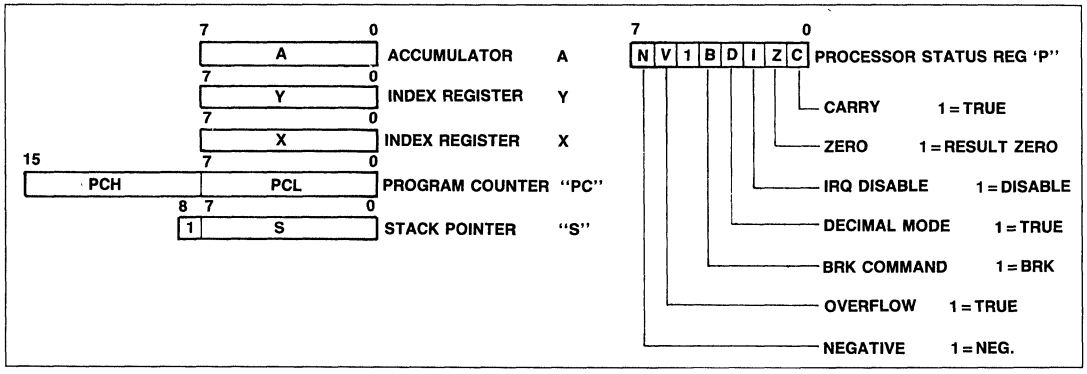
R650X and R651X Internal Architecture

INSTRUCTION SET

The R6500 CPU has 56 instruction types which are enhanced by up to 13 addressing modes for each instruction. The Accumulator, index registers, Program Counter, Stack Pointer and Processor Status Register are illustrated below.

Alphabetic Listing of Instruction Set

Mnemonic	Function	Mnemonic	Function
ADC	Add Memory to Accumulator with Carry	JMP	Jump to New Location
AND	"AND" Memory with Accumulator	JSR	Jump to New Location Saving Return Address
ASL	Shift Left One Bit (Memory or Accumulator)		
		LDA	Load Accumulator with Memory
BCC	Branch on Carry Clear	LDX	Load Index X with Memory
BCS	Branch on Carry Set	LDY	Load Index Y with Memory
BEQ	Branch on Result Zero	LSR	Shift One Bit Right (Memory or Accumulator)
BIT	Test Bits in Memory with Accumulator		
BMI	Branch on Result Minus	NOP	No Operation
BNE	Branch on Result not Zero		
BPL	Branch on Result Plus	ORA	"OR" Memory with Accumulator
BRK	Force Break		
BVC	Branch on Overflow Clear	PHA	Push Accumulator on Stack
BVS	Branch on Overflow Set	PHP	Push Processor Status on Stack
		PLA	Pull Accumulator from Stack
CLC	Clear Carry Flag	PLP	Pull Processor Status from Stack
CLD	Clear Decimal Mode		
CLI	Clear Interrupt Disable Bit	ROL	Rotate One Bit Left (Memory or Accumulator)
CLV	Clear Overflow Flag	ROR	Rotate One Bit Right (Memory or Accumulator)
CMP	Compare Memory and Accumulator	RTI	Return from Interrupt
CPX	Compare Memory and Index X	RTS	Return from Subroutine
CPY	Compare Memory and Index Y		
		SBC	Subtract Memory from Accumulator with Borrow
DEC	Decrement Memory by One	SEC	Set Carry Flag
DEX	Decrement Index X by One	SED	Set Decimal Mode
DEY	Decrement Index Y by One	SEI	Set Interrupt Disable Status
		STA	Store Accumulator in Memory
EOR	"Exclusive-OR" Memory with Accumulator	STX	Store Index X in Memory
		STY	Store Index Y in Memory
INC	Increment Memory by One		
INX	Increment Index X by One	TAX	Transfer Accumulator to Index X
INY	Increment Index Y by One	TAY	Transfer Accumulator to Index Y
		TSX	Transfer Stack Pointer to Index X
		TXA	Transfer Index X to Accumulator
		TXS	Transfer Index X to Stack Register
		TYA	Transfer Index Y to Accumulator



Programming Model

ADDRESSING MODES

The R6500 CPU family has 13 addressing modes. In the following discussion of these addressing modes, a bracketed expression follows the title of the mode. This expression is the term used in the Instruction Set Op Code Matrix table (later in this product description) to make it easier to identify the actual addressing mode used by the instruction.

ACCUMULATOR ADDRESSING [Accum]—This form of addressing is represented with a one byte instruction, implying an operation on the accumulator.

IMMEDIATE ADDRESS [IMM]—In immediate addressing, the second byte of the instruction contains the operand, with no further memory addressing required.

ABSOLUTE ADDRESSING [Absolute]—In absolute addressing, the second byte of the instruction specifies the eight low order bits of the effective address while the third byte specifies the eight high order bits. Thus, the absolute addressing mode allows access to the entire 64K bytes of addressable memory.

ZERO PAGE ADDRESSING [ZP]—The zero page instructions allow for shorter code and execution times by fetching only the second byte of the instruction and assuming a zero high address byte. Careful use of the zero page can result in significant increase in code efficiency.

INDEXED ZERO PAGE ADDRESSING [ZP, X or Y]—This form of addressing is used with the index register and is referred to as "Zero Page, X" or "Zero Page, Y". The effective address is calculated by adding the second byte to the contents of the index register. Since this is a form of "Zero Page" addressing, the content of the second byte references a location in page zero. Additionally, due to the "Zero Page" addressing nature of this mode, no carry is added to the high order eight bits of memory and crossing of page boundaries does not occur.

INDEXED ABSOLUTE ADDRESSING [ABS, X or Y]—This form of addressing is used in conjunction with X and Y index register and is referred to as "Absolute, X" and "Absolute, Y." The effective address is formed by adding the contents of X or Y to the address contained in the second and third bytes of the instruction. This mode allows the index register to contain the index or count value and the instruction to contain the base address. This type of indexing allows referencing of any location and the index may modify multiple fields, resulting in reduced coding and execution time.

IMPLIED ADDRESSING [Implied]—In the implied addressing mode, the address containing the operand is implicitly stated in the operation code of the instruction.

RELATIVE ADDRESSING [Relative]—Relative addressing is used only with branch instructions and establishes a destination for the conditional branch.

The second byte of the instruction is an operand. This operand is an offset which is added to the program counter when the counter is set at the next instruction. The range of the offset is −128 to +127 bytes.

INDEXED INDIRECT ADDRESSING [(IND, X)]—In indexed indirect addressing (referred to as (Indirect, X)), the second byte of the instruction is added to the contents of index register X discarding the carry. The result of this addition points to a memory location on page zero which contains the low order byte of the effective address. The next memory location in page zero contains the high order byte of the effective address. Both memory locations specifying the effective address must be in page zero.

INDIRECT INDEXED ADDRESSING [(IND), Y)]—In indirect indexed addressing (referred to as (Indirect), Y), the second byte of the instruction points to a memory location in page zero. The contents of this memory location are added to the contents of index register Y. The result is the low order byte of the effective address. The carry from this addition is added to the contents of the next page zero memory location, to form the high order byte of the effective address.

ABSOLUTE INDIRECT [Indirect]—The second byte of the instruction contains the low order byte of a memory location. The high order eight bits of that memory location are contained in the third byte of the instruction. The contents of the fully specified memory location are the low order byte of the effective address. The next memnory location contains the high order byte of the effective address which is loaded into the sixteen bits of the program counter. (JMP (IND) only)

INSTRUCTION SET OP CODE MATRIX

The following matrix shows the Op Codes associated with the R6500 family of CPU devices. The matrix identifies the hexadecimal code, the mnemonic code, the addressing mode, the number of instruction bytes, and the number of machine cycles associated with each Op Code. Also, refer to the instruction set summary for additional information on these Op Codes.

MSD \ LSD	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	MSD
0	BRK Implied 1 7	ORA (IND, X) 2 6				ORA ZP 2 3	ASL ZP 2 5		PHP Implied 1 3	ORA IMM 2 2	ASL Accum 1 2			ORA ABS 3 4	ASL ABS 3 6		0
1	BPL Relative 2 2**	ORA (IND), Y 2 5*				ORA ZP, X 2 4	ASL ZP, X 2 6		CLC Implied 1 2	ORA ABS, Y 3 4*				ORA ABS, X 3 4*	ASL ABS, X 3 7		1
2	JSR Absolute 3 6	AND (IND, X) 2 6			BIT ZP 2 3	AND ZP 2 3	ROL ZP 2 5		PLP Implied 1 4	AND IMM 2 2	ROL Accum 1 2		BIT ABS 3 4	AND ABS 3 4	ROL ABS 3 6		2
3	BMI Relative 2 2**	AND (IND), Y 2 5*				AND ZP, X 2 4	ROL ZP, X 2 6		SEC Implied 1 2	AND ABS, Y 3 4*				AND ABS, X 3 4*	ROL ABS, X 3 7		3
4	RTI Implied 1 6	EOR (IND, X) 2 6				EOR ZP 2 3	LSR ZP 2 5		PHA Implied 1 3	EOR IMM 2 2	LSR Accum 1 2		JMP ABS 3 3	EOR ABS 3 4	LSR ABS 3 6		4
5	BVC Relative 2 2**	EOR (IND), Y 2 5*				EOR ZP, X 2 4	LSR ZP, X 2 6		CLI Implied 1 2	EOR ABS, Y 3 4*				EOR ABS, X 3 4*	LSR ABS, X 3 7		5
6	RTS Implied 1 6	ADC (IND, X) 2 6				ADC ZP 2 3	ROR ZP 2 5		PLA Implied 1 4	ADC IMM 2 2	ROR Accum 1 2		JMP Indirect 3 5	ADC ABS 3 4	ROR ABS 3 6		6
7	BVS Relative 2 2**	ADC (IND), Y 2 5*				ADC ZP, X 2 4	ROR ZP, X 2 6		SEI Implied 1 2	ADC ABS, Y 3 4*				ADC ABS, X 3 4*	ROR ABS, X 3 7		7
8		STA (IND, X) 2 6			STY ZP 2 3	STA ZP 2 3	STX ZP 2 3		DEY Implied 1 2		TXA Implied 1 2		STY ABS 3 4	STA ABS 3 4	STX ABS 3 4		8
9	BCC Relative 2 2**	STA (IND), Y 2 6			STY ZP, X 2 4	STA ZP, X 2 4	STX ZP, Y 2 4		TYA Implied 1 2	STA ABS, Y 3 5	TXS Implied 1 2			STA ABS, X 3 5			9
A	LDY IMM 2 2	LDA (IND, X) 2 6	LDX IMM 2 2		LDY ZP 2 3	LDA ZP 2 3	LDX ZP 2 3		TAY Implied 1 2	LDA IMM 2 2	TAX Implied 1 2		LDY ABS 3 4	LDA ABS 3 4	LDX ABS 3 4		A
B	BCS Relative 2 2**	LDA (IND), Y 2 5*			LDY ZP, X 2 4	LDA ZP, X 2 4	LDX ZP, Y 2 4		CLV Implied 1 2	LDA ABS, Y 3 4*	TSX Implied 1 2		LDY ABS, X 3 4*	LDA ABS, X 3 4*	LDX ABS, Y 3 4*		B
C	CPY IMM 2 2	CMP (IND, X) 2 6			CPY ZP 2 3	CMP ZP 2 3	DEC ZP 2 5		INY Implied 1 2	CMP IMM 2 2	DEX Implied 1 2		CPY ABS 3 4	CMP ABS 3 4	DEC ABS 3 6		C
D	BNE Relative 2 2**	CMP (IND), Y 2 5*				CMP ZP, X 2 4	DEC ZP, X 2 6		CLD Implied 1 2	CMP ABS, Y 3 4*				CMP ABS, X 3 4*	DEC ABS, X 3 7		D
E	CPX IMM 2 2	SBC (IND, X) 2 6			CPX ZP 2 3	SBC ZP 2 3	INC ZP 2 5		INX Implied 1 2	SBC IMM 2 2	NOP Implied 1 2		CPX ABS 3 4	SBC ABS 3 4	INC ABS 3 6		E
F	BEQ Relative 2 2**	SBC (IND), Y 2 5*				SBC ZP, X 2 4	INC ZP, X 2 6		SED Implied 1 2	SBC ABS, Y 3 4*				SBC ABS, X 3 4*	INC ABS, X 3 7		F
	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	

0	
0	BRK Implied 1 7

—OP Code
—Addressing Mode
—Instruction Bytes; Machine Cycles

*Add 1 to N if page boundary is crossed.
**Add 1 to N if branch occurs to same page; add 2 to N if branch occurs to different page.

INSTRUCTION SET SUMMARY

INSTRUCTIONS		IMMEDIATE			ABSOLUTE			ZERO PAGE			ACCUM			IMPLIED			(IND, X)			(IND), Y			Z PAGE, X			ABS X			ABS, Y			RELATIVE			INDIRECT			Z PAGE, Y			PROCESSOR STATUS CODES	
MNEMONIC	OPERATION	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	7 6 5 4 3 2 1 0 N V • B D I Z C	MNEMONIC
ADC	A + M + C → A (4) (1)	69	2	2	6D	4	3	65	3	2							61	6	2	71	5	2	75	4	2	7D	4	3	79	4	3										N V • • • • Z C	ADC
AND	A ∧ M → A (1)	29	2	2	2D	4	3	25	3	2							21	6	2	31	5	2	35	4	2	3D	4	3	39	4	3										N • • • • • Z •	AND
ASL	C ← [7 … 0] ← 0				0E	6	3	06	5	2	0A	2	1										16	6	2	1E	7	3													N • • • • • Z C	ASL
BCC	BRANCH ON C = 0 (2)																															90	2	2								• • • • • • • •	BCC
BCS	BRANCH ON C = 1 (2)																															B0	2	2								• • • • • • • •	BCS
BEQ	BRANCH ON Z = 1 (2)																															F0	2	2								• • • • • • • •	BEQ
BIT	A ∧ M				2C	4	3	24	3	2																																M_7 M_6 • • • • Z •	BIT
BMI	BRANCH ON N = 1 (2)																															30	2	2								• • • • • • • •	BMI
BNE	BRANCH ON Z = 0 (2)																															D0	2	2								• • • • • • • •	BNE
BPL	BRANCH ON N = 0 (2)																															10	2	2								• • • • • • • •	BPL
BRK	BREAK													00	7	1																									• • • 1 • 1 • •	BRK
BVC	BRANCH ON V = 0 (2)																															50	2	2								• • • • • • • •	BVC
BVS	BRANCH ON V = 1 (2)																															70	2	2								• • • • • • • •	BVS
CLC	0 → C													18	2	1																									• • • • • • • 0	CLC
CLD	0 → D													D8	2	1																									• • • • 0 • • •	CLD
CLI	0 → I													58	2	1																									• • • • • 0 • •	CLI
CLV	0 → V													B8	2	1																									• 0 • • • • • •	CLV
CMP	A − M	C9	2	2	CD	4	3	C5	3	2							C1	6	2	D1	5	2	D5	4	2	DD	4	3	D9	4	3										N • • • • • Z C	CMP
CPX	X − M	E0	2	2	EC	4	3	E4	3	2																																N • • • • • Z C	CPX
CPY	Y − M	C0	2	2	CC	4	3	C4	3	2																																N • • • • • Z C	CPY
DEC	M − 1 → M				CE	6	3	C6	5	2													D6	6	2	DE	7	3													N • • • • • Z •	DEC
DEX	X − 1 → X													CA	2	1																									N • • • • • Z •	DEX
DEY	Y − 1 → Y													88	2	1																									N • • • • • Z •	DEY
EOR	A ∨ M → A (1)	49	2	2	4D	4	3	45	3	2							41	6	2	51	5	2	55	4	2	5D	4	3	59	4	3										N • • • • • Z •	EOR
INC	M + 1 → M				EE	6	3	E6	5	2													F6	6	2	FE	7	3													N • • • • • Z •	INC
INX	X + 1 → X													E8	2	1																									N • • • • • Z •	INX
INY	Y + 1 → Y													C8	2	1																									N • • • • • Z •	INY
JMP	JUMP TO NEW LOC				4C	3	3																												6C	5	3				• • • • • • • •	JMP
JSR	JUMP SUB				20	6	3																																			• • • • • • • •	JSR
LDA	M → A (1)	A9	2	2	AD	4	3	A5	3	2							A1	6	2	B1	5	2	B5	4	2	BD	4	3	B9	4	3										N • • • • • Z •	LDA
LDX	M → X (1)	A2	2	2	AE	4	3	A6	3	2																			BE	4	3							B6	4	2	N • • • • • Z •	LDX
LDY	M → Y (1)	A0	2	2	AC	4	3	A4	3	2													B4	4	2	BC	4	3													N • • • • • Z •	LDY
LSR	0 → [7 … 0] → C				4E	6	3	46	5	2	4A	2	1										56	6	2	5E	7	3													0 • • • • • Z C	LSR
NOP	NO OPERATION													EA	2	1																									• • • • • • • •	NOP
ORA	A ∨ M → A	09	2	2	0D	4	3	05	3	2							01	6	2	11	5	2	15	4	2	1D	4	3	19	4	3										N • • • • • Z •	ORA
PHA	A → Ms S − 1 → S													48	3	1																									• • • • • • • •	PHA
PHP	P → Ms S − 1 → S													08	3	1																									• • • • • • • •	PHP
PLA	S + 1 → S Ms → A													68	4	1																									N • • • • • Z •	PLA
PLP	S + 1 → S Ms → P													28	4	1																									(RESTORED)	PLP
ROL	[7 … 0] ← [C] ←				2E	6	3	26	5	2	2A	2	1										36	6	2	3E	7	3													N • • • • • Z C	ROL
ROR	[C] → [7 … 0]				6E	6	3	66	5	2	6A	2	1										76	6	2	7E	7	3													N • • • • • Z C	ROR
RTI	RTRN INT													40	6	1																									(RESTORED)	RTI
RTS	RTRN SUB													60	6	1																									• • • • • • • •	RTS
SBC	A − M − $\overline{C}$ → A (1)	E9	2	2	ED	4	3	E5	3	2							E1	6	2	F1	5	2	F5	4	2	FD	4	3	F9	4	3										N V • • • • Z (3)	SBC
SEC	1 → C													38	2	1																									• • • • • • • 1	SEC
SED	1 → D													F8	2	1																									• • • • 1 • • •	SED
SEI	1 → I													78	2	1																									• • • • • 1 • •	SEI
STA	A → M				8D	4	3	85	3	2							81	6	2	91	6	2	95	4	2	9D	5	3	99	5	3										• • • • • • • •	STA
STX	X → M				8E	4	3	86	3	2																														96	4	2	• • • • • • • •	STX
STY	Y → M				8C	4	3	84	3	2													94	4	2																	• • • • • • • •	STY
TAX	A → X													AA	2	1																									N • • • • • Z •	TAX
TAY	A → Y													A8	2	1																									N • • • • • Z •	TAY
TSX	S → X													BA	2	1																									N • • • • • Z •	TSX
TXA	X → A													8A	2	1																									N • • • • • Z •	TXA
TXS	X → S													9A	2	1																									• • • • • • • •	TXS
TYA	Y → A													98	2	1																									N • • • • • Z •	TYA

(1) ADD 1 to N IF PAGE BOUNDARY IS CROSSED

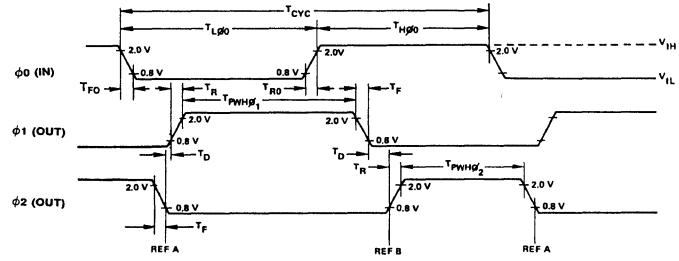
(2) ADD 1 TO N IF BRANCH OCCURS TO SAME PAGE
ADD 2 TO N IF BRANCH OCCURS TO DIFFERENT PAGE

(3) CARRY NOT = BORROW

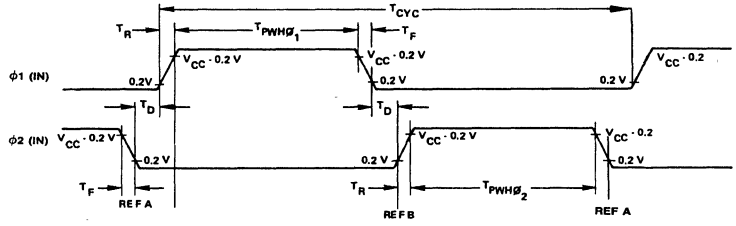
(4) IF IN DECIMAL MODE Z FLAG IS INVALID
ACCUMULATOR MUST BE CHECKED FOR ZERO RESULT

X	INDEX X	+	ADD	M	MEMORY BIT 7
Y	INDEX Y	-	SUBTRACT	M_6	MEMORY BIT 6
A	ACCUMULATOR	∧	AND	n	NO CYCLES
M	MEMORY PER EFFECTIVE ADDRESS	∨	OR	#	NO BYTES
Ms	MEMORY PER STACK POINTER	∀	EXCLUSIVE OR		

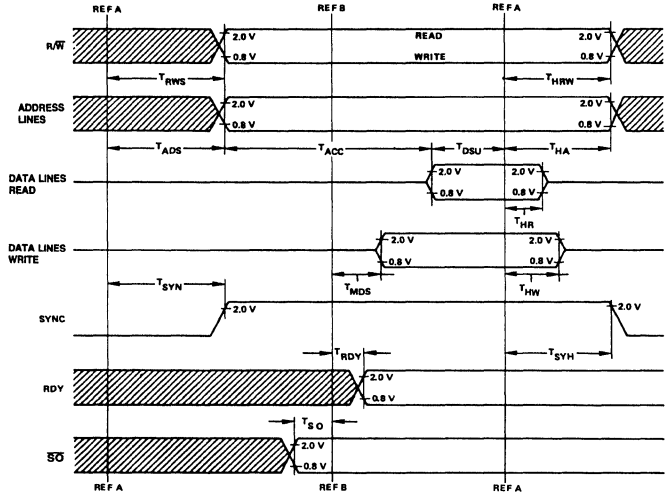
R650X CLOCK TIMING



R651X CLOCK TIMING



R65XX READ WRITE TIMING

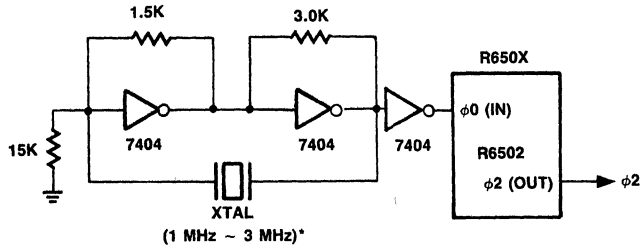


AC CHARACTERISTICS

Characteristic	Symbol	R65XX (1 MHz) Min	R65XX (1 MHz) Max	R65XXA (2 MHz) Min	R65XXA (2 MHz) Max	R65XXB (3 MHz) Min	R65XXB (3 MHz) Max	Unit
R650X CLOCK TIMING								
Clock Cycle Time	T_{CYC}	1.0	10	0.5	10	0.33	10	µs
Ø0 (IN) Low Pulse Width	$T_{LØ0}$	480	—	240	—	160	—	ns
Ø0 (IN) High Pulse Width	$T_{HØ0}$	460	—	240	—	160	—	ns
Ø0 (IN) Rise and Fall Time[1, 2]	T_{R0}, T_{F0}	—	10	—	10	—	10	ns
Ø1 (OUT) High Pulse Width	$T_{PWHØ1}$	460	—	235	—	155	—	ns
Ø2 (OUT) High Pulse Width	$T_{PWHØ2}$	460	—	240	—	160	—	ns
Delay Between Ø1 (OUT) and Ø2 (OUT)	T_D	0	—	0	—	0	—	ns
Ø1 (OUT), Ø2 (OUT) Rise and Fall Time[1, 2]	T_R, T_F	—	25	—	25	—	15	ns
R651X CLOCK TIMING								
Clock Cycle Time	T_{CYC}	1.0	10	0.5	10	0.33	10	µs
Ø1 (IN) High Pulse Width	$T_{PWHØ1}$	430	—	215	—	150	—	ns
Ø2 (IN) High Pulse Width	$T_{PWHØ2}$	470	—	235	—	160	—	ns
Delay Between Ø1 and Ø2	T_D	0	—	0	—	0	—	ns
Ø1 (IN), Ø2 (IN) Rise and Fall Time[1, 3]	T_R, T_F	—	25	—	20	—	15	ns
R65XX READ/WRITE TIMING								
R/$\overline{W}$ Setup Time	T_{RWS}	—	225	—	140	—	110	ns
R/$\overline{W}$ Hold Time	T_{HRW}	30	—	30	—	15	—	ns
Address Setup Time	T_{ADS}	—	225	—	140	—	110	ns
Address Hold Time	T_{HA}	30	—	30	—	15	—	ns
Read Access Time	T_{ACC}	—	650	—	310	—	170	ns
Read Data Setup Time	T_{DSU}	100	—	50	—	50	—	ns
Read Data Hold Time	T_{HR}	10	—	10	—	10	—	ns
Write Data Setup Time	T_{MDS}	—	175	—	100	—	85	ns
Write Data Hold Time	T_{HW}	30	—	30	—	15	—	ns
SYNC Hold Time	T_{SYH}	30	—	30	—	15	—	ns
RDY Setup Time	T_{RDY}	100	—	50	—	35	—	ns
$\overline{SO}$ Setup Time	T_{S0}	100	—	50	—	35	—	ns
SYNC Setup Time	T_{SYN}	—	225	—	140	—	110	ns

Notes:
1. Loads: All output except clocks = 1 TTL + 130 pF. Clock outputs = 1 TTL + 30 pF.
2. Measured between 0.8 and 2.0 points on waveform load.
3. Measured between 10% and 90% points on waveforms.
4. *RDY must never switch states within R_{RDY} to end of Ø2.

EXAMPLE OF TIME BASE GENERATION FOR R6502



*CRYSTAL: CTS KNIGHTS MP SERIES, OR EQUIVALENT

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to +7.0	Vdc
Input Voltage	V_{IN}	−0.3 to +7.0	Vdc
Operating Temperature Range Commercial Industrial	T_A	 −40 to +85	°C
Storage Temperature	T_{STG}	−55 to +150	°C

***NOTE:** Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the other sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING CONDITIONS

Parameter	Symbol	Value
Supply Voltage	V_{CC}	5V ±5%
Temperature Range Commercial Industrial	T_A	 0°C to +70°C −40°C to +85°C

DC CHARACTERISTICS

(V_{CC} = 5.0V ±5%, V_{SS} = 0; T_A = T_L to T_H, unless otherwise noted)

Parameter	Symbol	Min.	Typ.[5]	Max.	Unit[1]	Test Conditions
Input High Voltage Logic Ø0 (IN) Ø1 (IN), Ø2 (IN)	V_{IH}	 2.0 2.4 V_{CC} − 0.3	 — — —	 V_{CC} V_{CC} V_{CC} + 0.25	V	
Input Low Voltage Logic Ø0 (IN), Ø1 (IN), Ø2 (IN)	V_{IL}	 −0.3 −0.3	 — —	 0.8 0.4	V	
Input Leakage Current Logic (Excl. RDY, $\overline{SO}$) Ø1 (IN), Ø2 (IN) Ø0 (IN)	I_{IN}	 — — —	 — — —	 2.5 100 10	µA	V_{IN} = 0V to 5.25V V_C = 0V
Input Leakage Current for Three State Offf D0–D7	I_{TSI}	 —	 —	 10	µA	V_{IN} = 0.4V to 2.4V V_{CC} = 5.25V
Output High Voltage SYNC, D0–D7, A0–A15, R/$\overline{W}$, Ø1 (OUT), Ø2 (OUT)	V_{OH}	 +2.4	 —	 —	V	I_{LOAD} = −100 µA V_{CC} = 4.75V
Output Low Voltage SYNC, D0–D7, A0–A15, R/$\overline{W}$, Ø1 (OUT), Ø2 (OUT)	V_{OL}	 —	 —	 +0.4	V	I_{LOAD} = 1.6 ma V_{CC} = 4.75V
Power Dissipation 1 and 2 MHz 3 MHz	P_D	 — —	 450 500	 700 800	mW	
Capacitance Logic D0–D7 A0–A15, R/$\overline{W}$, SYNC Ø0 (IN) Ø1 (IN) Ø2 (IN)	C C_{IN} C_{OUT} $C\emptyset_{0(IN)}$ $C\emptyset 1$ $C\emptyset 2$	 — — — — — —	 — — — — 30 50	 10 15 12 15 50 80	pF	V_{CC} = 5.0V V_{IN} = 0V f = 1 MHz T_A = 25°C

Notes:
1. All units are direct current (dc) except for capacitance.
2. Negative sign indicates outward current flow, positive indicates inward flow.
3. $\overline{IRQ}$ and $\overline{NMI}$ require 3K pull-up resistor.
4. Ø1 (IN) and Ø2 (IN) apply to R6512, 13, 14, and 15; Ø0 (IN) applies to R6502, 03, 04, 05, 06 and 07.
5. Typical values shown for V_{CC} = 5.0V and T_A = 25°C.

R6520
Peripheral Interface Adapter (PIA)

DESCRIPTION

The R6520 Peripheral Interface Adapter (PIA) is designed to solve a broad range of peripheral control problems in the implementation of microcomputer systems. This device allows a very effective trade-off between software and hardware by providing significant capability and flexibility in a low cost chip. When coupled with the power and speed of the R6500, R6500/* or R65C00 family of microprocessors, the R6520 allows implementation of very complex systems at a minimum overall cost.

Control of peripheral devices is handled primarily through two 8-bit bidirectional ports. Each of these lines can be programmed to act as either an input or an output. In addition, four peripheral control/interrupt input lines are provided. These lines can be used to interrupt the processor or to "handshake" data between the processor and a peripheral device.

FEATURES

- Two 8-bit directional I/O ports with individual data direction control
- Automatic "Handshake" control of data transfers
- Two interrupts (one for each port) with program control
- Commercial and industrial temperature range versions
- 40-pin plastic and ceramic versions
- 5 volt ±5% supply requirements
- Compatible with the R6500, R6500/* and R65C00 family of microprocessors
- 1 and 2 MHz versions

ORDERING INFORMATION

Part Number
R6520 ___

- Temperature Range (T_L to T_H):
  - Blank = 0°C to +70°C
  - E = −40°C to +85°C
- Package:
  - C = 40-Pin Ceramic DIP
  - P = 40-Pin Plastic DIP
- Frequency Range:
  - No letter = 1 MHz
  - A = 2 MHz

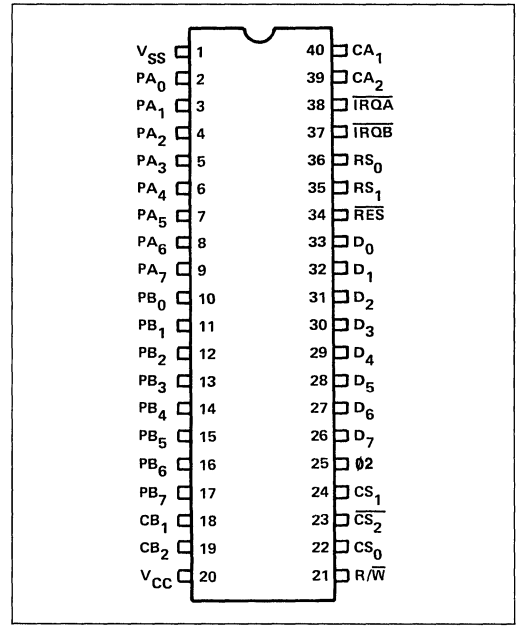


Figure 1. R6520 Pin Configuration

FUNCTIONAL DESCRIPTION

The R6520 PIA is organized into two independent sections referred to as the A Side and the B Side. Each section consists of a Control Register (CRA, CRB), Data Direction Register (DDRA, DDRB), Output Register (ORA, OBR), Interrupt Status Control (ISCA, ISCB), and the buffers necessary to drive the Peripheral Interface buses. Data Bus Buffers (DBB) interface data from the two sections to the data bus, while the Data Input Register (DIR) interfaces data from the DBB to the PIA registers. Chip Select and R/$\overline{W}$ control circuitry interface to the processor bus control lines. Figure 2 is a block diagram of the R6520 PIA.

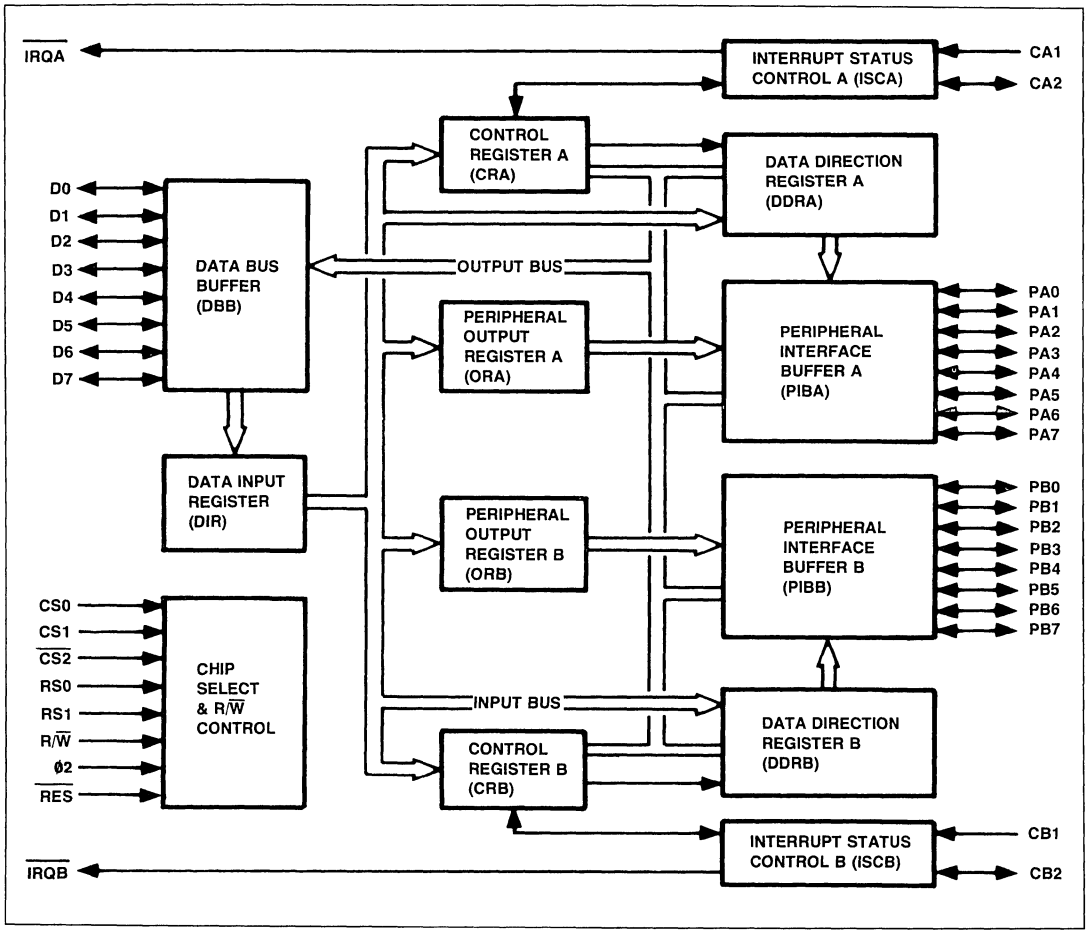


Figure 2. R6520 PIA Block Diagram

DATA INPUT REGISTER (DIR)

When the microprocessor writes data into the PIA, the data which appears on the data bus during the Ø2 clock pulse is latched into the Data Input Register (DIR). The data is then transferred into one of six internal registers of the PIA after the trailing edge of the Ø2 clock. This assures that the data on the peripheral output lines will make smooth transitions from high to low (or from low to high) and the voltage will remain stable except when it is going to the opposite polarity.

CONTROL REGISTERS (CRA and CRB)

Table 1 illustrates the bit designation and functions in the two control registers. The control registers allow the microprocessor to control the operation of the Interrupt Control inputs (CA1, CA2, CB1, CB2), and Peripheral Control outputs (CA2, CB2). Bit 2 in each register controls the addressing of the Data Direction Registers (DDRA, DDRB) and the Output Registers (ORA, ORB). In addition, two bits (bit 6 and 7) in each control register indicate the status of the Interrupt Input lines (CA1, CA2, CB1, CB2). These Interrupt Status bits (IRQA1, IRQA2 or IRQB1, IRQB2) are normally interrogated by the microprocessor during the $\overline{IRQ}$ interrupt service routine to determine the source of the interrupt.

Bit 2 (DDRA, DDRB) in each Control Register (CRA and CRB) controls access to the Data Direction Register or the Peripheral Interface. If bit 2 is a "1," a Peripheral Output Register (ORA, ORB) is selected, and if bit 2 is a "0," a Data Direction Register (DDRA, DDRB) is selected. The Data Direction Register Access Control bit, together with the Register Select lines (RS0, RS1) selects the various internal registers as shown in Table 2.

In order to write data into DDRA, ORA, DDRB, or ORB registers, bit 2 in the proper Control Register must first be set. The desired register may then be accessed with the address determined by the address interconnect technique used.

DATA DIRECTION REGISTERS (DDRA, DDRB)

The Data Direction Registers (DDRA, DDRB) allow the processor to program each line in the 8-bit Peripheral I/O port to be either an input or an output. Each bit in DDRA controls the corresponding line in the Peripheral A port and each bit in DDRB controls the corresponding line in the Peripheral B port. Writing a "0" in a bit position in the Data Direction Register causes the corresponding Peripheral I/O line to act as an input; a "1" causes it to act as an output.

PERIPHERAL OUTPUT REGISTERS (ORA, ORB)

The Peripheral Output Registers (ORA, ORB) store the output data from the Data Bus Buffers (DBB) which appears on the Peripheral I/O port. If a line on the Peripheral A Port is programmed as an output by the DDRA, writing a 0 into the corresponding bit in the ORA causes that line to go low (<0.4 V); writing a 1 causes the line to go high. The lines of the Peripheral B port are controlled by ORB in the same manner.

INTERRUPT STATUS CONTROL (ISCA, ISCB)

The four interrupt/peripheral control lines (CA1, CA2, CB1, CB2) are controlled by the Interrupt Status Control logic (A, B). This logic interprets the contents of the corresponding Control Register and detects active transitions on the interrupt inputs.

PERIPHERAL I/O PORTS (PA0–PA7, PB0–PB7)

The Peripheral A and Peripheral B I/O ports allow the microprocessor to interface to the input lines on a peripheral device by writing data into the Peripheral Output Register. They also allow the processor to interface with the peripheral device output lines by reading the data on the Peripheral Port input lines directly onto the data bus and into the internal registers of the processor.

Each of the Peripheral I/O lines can be programmed to act as an input or an output. This is accomplished by setting a 1 in the corresponding bit in the Data Direction Register for those lines which are to act as outputs. A 0 in a bit of the Data Direction Register causes the corresponding Peripheral I/O lines to act as an input.

The buffers which drive the Peripheral A I/O lines contain "passive" pull-up devices. These pull-up devices are resistive in nature and therefore allow the output voltage to go to VCC for a logic 1. The switches can sink 1.6 mA, making thesse buffers capable of driving one standard TTL load.

In the input mode, the pull-up devices are still connected to the I/O pin and still supply current to this pin. For this reason, these lines also represent one standard TTL load in the input mode.

The Peripheral B I/O port duplicates many of the functions of the Peripheral A port. The process of programming these lines to act as an input or an output is similar to the Peripheral A port, as is the effect of reading or writing this port. However, there are several characteristics of the buffers driving these lines which affect their use in peripheral interfacing.

Table 1. Control Registers Bit Designations

	7	6	5	4	3	2	1	0
CRA	IRQA1	IRQA2	CA2 Control			DDRA/ORA Select	CA1 Control	
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CRB	IRQB1	IRQB2	CB2 Control			DDRB/ORB Select	CB1 Control	

The Peripheral B I/O port buffers are push-pull devices i.e., the pull-up devices are switched OFF in the 0 state and ON for a logic 1. Since these pull-ups are active devices, the logic 1 voltage will not go higher than +2.4V.

Another difference between the PA0–PA7 lines and the PB0 through PB7 lines is that they have three-state capability which allows them to enter a high impedance state when programmed to be used as input lines. In addition, data on these lines will be read properly, when programmed as output lines, even if the data signals fall below 2.0 volts for a "high" state or are above 0.8 volts for a "low" state. When programmed as output, each line can drive at least one TTL load and may also be used as a source of up to 1 milliampere at 1.5 volts to directly drive the base of a transistor switch, such as a Darlington pair.

DATA BUS BUFFER (DBB)

The Data Bus Buffer is an 8-bit bidirectional buffer used for data exchange, on the D0–D7 Data Bus, between the microprocessor and the PIA. This buffer is tri-stateable and is capable of driving a two TTL load (when operating in an output mode) and represents a one TTL load to the microprocessor (when operating in an input mode).

INTERFACE SIGNALS

The PIA interfaces to the R6500, R6500/* or the R65C00 microprocessor family with a reset line, a ϕ clock line, a read/write line, two interrupt request lines, two register select lines, three chip select lines, and an 8-bit bidirectional data bus.

The PIA interfaces to the peripheral device with four interrupt/control lines and two 8-bit bidirectional data ports.

Figure 1 (on the front page) shows the pin assignments for these interface signals and Figure 3 shows the interface relationship of these signals to the CPU and the peripheral devices.

CHIP SELECT (CS0, CS1, $\overline{CS2}$)

The PIA is selected when CS0 and CS1 are high and $\overline{CS2}$ is low. These three chip select lines are normally connected to the processor address lines either directly or through external decoder circuits. When the PIA is selected, data will be transferred between the data lines and PIA registers, and/or peripheral interface lines as determined by the R/$\overline{W}$, RS0, and RS1 lines and the contents of Control Registers A and B.

RESET SIGNAL ($\overline{RES}$)

The Reset ($\overline{RES}$) input initializes the R6520 PIA. A low signal on the $\overline{RES}$ input causes all internal registers to be cleared.

CLOCK SIGNAL (ϕ2)

The Phase 2 Clock Signal (ϕ2) is the system clock that triggers all data transfers between the CPU and the PIA. ϕ2 is generated by the CPU and is therefore the synchronizing signal between the CPU and the PIA.

READ/WRITE SIGNAL (R/$\overline{W}$)

Read/Write (R/$\overline{W}$) controls the direction of data transfers between the PIA and the data lines associated with the CPU and the peripheral devices. A high on the R/$\overline{W}$ line permits the peripheral device to transfer data to the CPU from the PIA. A low on the R/$\overline{W}$ line allows data to be transferred from the CPU to the peripheral devices from the PIA.

REGISTER SELECT (RS0, RS1)

The two Register Select lines (RS0, RS1), in conjunction with the Control Registers (CRA, CRB) Data Direction Register access bits (bit 2), select the various R6520 registers to be accessed by the CPU. RS0 and RS1 are normally connected to the microprocessor (CPU) address output lines. Through control of these lines, the CPU can write directly into the Control

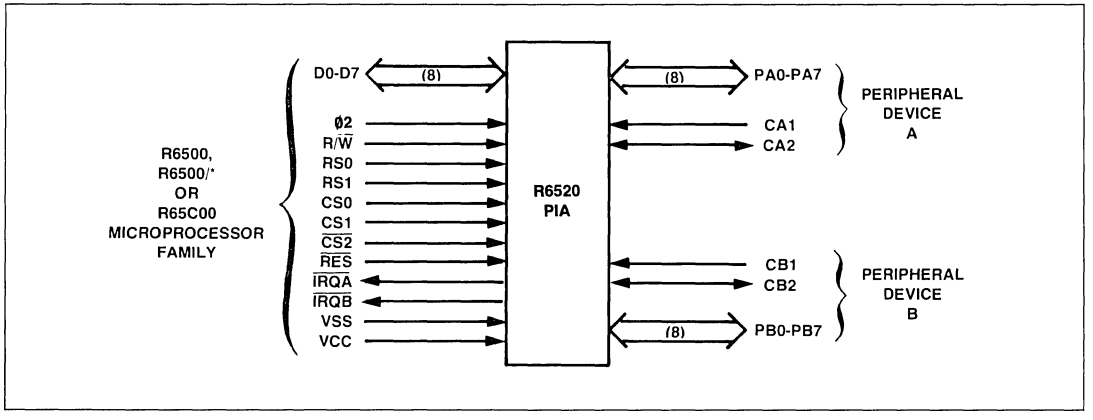


Figure 3. Interface Signals Relationship

Registers (CRA, CRB), the Data Direction Registers (DDRA, DDRB), and the Peripheral Output Registers (ORA, ORB). In addition, the processor may directly read the contents of the Control Registers and the Data Direction Registers. Table 2 shows the internal register address decoding.

Table 2. Internal Register Addressing

Register Address (Hex)	Register Select Lines		Data Direction Control		Register Operation	
	RS1	RS0	CRA (Bit 2)	CRB (Bit 2)	R/$\overline{W}$=H	R/$\overline{W}$=L
0	L	L	1	—	Read PIBA	Write ORA
0	L	L	0	—	Read DDRA	Write DDRA
1	L	H	—	—	Read CRA	Write CRA
2	H	L	—	1	Read PIBB	Write ORB
2	H	L	—	0	Read DDRB	Write DDRB
3	H	H	—	—	Read CRB	Write CRB

INTERRUPT REQUEST LINES ($\overline{IRQA}$, $\overline{IRQB}$)

The active low Interrupt Request lines ($\overline{IRQA}$ and $\overline{IRQB}$) act to interrupt the microprocessor either directly or through external interrupt priority circuitry. These lines are open drain and are capable of sinking 1.6 milliamps from an external source. This permits all interrupt request lines to be tied together in a wired-OR configuration. The A and B in the titles of these lines correspond to the peripheral port A and the peripheral port B so that each interrupt request line services one peripheral data port.

Each Interrupt Request line has two interrupt flag bits which can cause the Interrupt Request line to go low. These flags are bits 6 and 7 in the two Control Registers (CRA, CRB). These flags act as the link between the peripheral interrupt signals and the microprocessor interrupt inputs. Each flag has a corresponding interrupt disable bit which allows the processor to enable or disable the interrupt from each of the four interrupt inputs (CA1, CA2, CB1, CB2). The four interrupt flags are set (enabled) by active transitions of the signal on the interrupt input (CA1, CA2, CB1, CB2).

CRA bit 7 (IRQA1) is always set by an active transition of the CA1 interrupt input signal. However, $\overline{IRQA}$ can be disabled by setting bit 0 in CRA to a 0. Likewise, CRA bit 6 (IRQA2) can be set by an active transition of the CA2 interrupt input signal and $\overline{IRQA}$ can be disabled by setting bit 3 in CRA to a 0.

Both bit 6 and bit 7 in CRA are reset by a "Read Peripheral Output Register A" operation. This is defined as an operation in which the read/write, proper data direction register and register select signals are provided to allow the processor to read the Peripheral A I/O port. A summary of $\overline{IRQA}$ control is shown in Table 3.

Control of $\overline{IRQB}$ is performed in exactly the same manner as that described above for $\overline{IRQA}$. Bit 7 in CRB (IRQB1) is set by an active transition on CB1 and $\overline{IRQB}$ from this flag is controlled transition on CB2, and IRQB from this flag is controlled by CRB bit 3.

Also, both bit 6 and bit 7 of CRB are reset by a "Read Peripheral B Output Register" operation. A summary of $\overline{IRQB}$ control is shown in Table 3.

Table 3. $\overline{IRQA}$ and $\overline{IRQB}$ Control Summary

Control Register Bits	Action
CRA-7=1 and CRA-0=1	$\overline{IRQA}$ goes low (Active)
CRA-6=1 and CRA-3=1	$\overline{IRQA}$ goes low (Active)
CRB-7=1 and CRB-0=1	$\overline{IRQB}$ goes low (Active)
CRB-6=1 and CRB-3=1	$\overline{IRQB}$ goes low (Active)

Note:

The flags act as the link between the peripheral interrupt signals and the processor interrupt inputs. The interrupt disable bits allow the processor to control the interrupt function.

INTERRUPT INPUT/PERIPHERAL CONTROL LINES (CA1, CA2, CB1, CB2)

The four interrupt input/peripheral control lines provide a number of special peripheral control functions. These lines greatly enhance the power of the two general purpose interface ports (PA0-PA7, PB0-PB7). Figure 4 summarizes the operation of these control lines.

CA1 is an interrupt input only. An active transition of the signal on this input will set bit 7 of the Control Register A to a logic 1. The active transition can be programmed by setting a "0" in bit 1 of the CRA if the interrupt flag (bit 7 of CRA) is to be set on a negative transition of the CA1 signal or a "1" if it is to be set on a positive transition.

Note:

A negative transition is defined as a transition from a high to a low, and a positive transition is defined as a transition from a low to a high voltage.

CA2 can act as a totally independent interrupt or as a peripheral control output. As an input (CRA, bit 5 = 0) it acts to set the interrupt flag, bit 6 of CRA, to a logic 1 on the active transition selected by bit 4 of CRA.

These control register bits and interrupt inputs serve the same basic function as that described above for CA1. The input signal sets the interrupt flag which serves as the link between the peripheral device and the processor interrupt structure. The interrupt disable bit allows the processor to exercise control over the system interrupt.

In the output mode (CRA, bit 5 = 1), CA2 can operate independently to generate a simple pulse each time the microprocessor reads the data on the Peripheral A I/O port. This mode is selected by setting CRA, bit 4 to a 0 and CRA, bit 3 to a 1. This pulse output can be used to control the counters, shift registers, etc., which make sequential data available on the Peripheral input lines.

CONTROL REGISTER A (CRA)

CA2 INPUT MODE (BIT 5 = 0)

7	6	5	4	3	2	1	0
IRQA1 FLAG	IRQA2 FLAG	CA2 INPUT MODE SELECT (=0)	IRQA2 POSITIVE TRANSITION	$\overline{\text{IRQA}}$ ENABLE FOR IRQA2	DDRA/ORA SELECT	IRQA1 POSITIVE TRANSITION	$\overline{\text{IRQA}}$ ENABLE FOR IRQA1
			IRQA/IRQA2 CONTROL			$\overline{\text{IRQA}}$/IRQA1 CONTROL	

CA2 OUTPUT MODE (BIT 5 = 1)

7	6	5	4	3	2	1	0
IRQA1 FLAG	0	CA2 OUTPUT MODE SELECT (=1)	CA2 OUTPUT CONTROL	CA2 RESTORE CONTROL	DDRA/ORA SELECT	IRQA1 POSITIVE TRANSITION	$\overline{\text{IRQA}}$ ENABLE FOR IRQA1
			CA2 CONTROL			$\overline{\text{IRQA}}$/IRQA1 CONTROL	

CA2 INPUT OR OUTPUT MODE (BIT 5 = 0 or 1)

Bit 7 IRQA1 FLAG
- 1 A transition has occurred on CA1 that satisfies the bit 1 IRQA1 transition polarity criteria. This bit is cleared by a read of Output Register A or by $\overline{\text{RES}}$.
- 0 No transition has occurred on CA1 that satisfies the bit 1 IRQA1 transition polarity criteria.

Bit 2 OUTPUT REGISTER A SELECT
- 1 Select Output Register A.
- 0 Select Data Direction Register A.

Bit 1 IRQA1 POSITIVE TRANSITION
- 1 Set IRQA1 Flag (bit 7) on a positive (low-to-high) transition of CA1.
- 0 Set IRQA1 Flag (bit 7) on a negative (high-to-low) transition of CA1.

Bit 0 $\overline{\text{IRQA}}$ ENABLE FOR IRQA1
- 1 Enable assertion of $\overline{\text{IRQA}}$ when IRQA1 Flag (bit 7) is set.
- 0 Disable assertion of $\overline{\text{IRQA}}$ when IRQA1 Flag (bit 7) is set.

CA2 INPUT MODE (BIT 5 = 0)

Bit 6 IRQA2 FLAG
- 1 A transition has occurred on CA2 that satisfies the bit 4 IRQA2 transition polarity criteria. This flag is cleared by a read of Output Register A or by $\overline{\text{RES}}$.
- 0 No transition has occurred on CA2 that satisfies the bit 4 IRQA2 transition polarity criteria.

Bit 5 CA2 MODE SELECT
- 0 Select CA2 Input Mode.

Bit 4 IRQA2 POSITIVE TRANSITION
- 1 Set IRQA2 Flag (bit 6) on a positive (low-to-high) transition of CA2.
- 0 Set IRQA2 Flag (bit 6) on a negative (high-to-low) transition of CA2.

Bit 3 $\overline{\text{IRQA}}$ ENABLE FOR IRQA2
- 1 Enable assertion of IRQA when IRQA2 Flag (bit 6) is set.
- 0 Disable assertion of $\overline{\text{IRQA}}$ when IRQA2 Flag (bit 6) is set.

CA2 OUTPUT MODE (BIT 5 = 1)

Bit 6 NOT USED
- 0 Always zero.

Bit 5 CA2 MODE SELECT
- 1 Select CA2 Output Mode.

Bit 4 CA2 OUTPUT CONTROL
- 1 CA2 goes low when a zero is written into CRA bit 3. CA2 goes high when a one is written into CRA bit 3.
- 0 CA2 goes low on the first negative (high-to-low) Ø2 clock transition following a read of Output Register A. CA2 returns high as specified by bit 3.

Bit 3 CA2 READ STROBE RESTORE CONTROL (4 = 0)
- 1 CA2 returns high on the next Ø2 clock negative transition following a read of Output Register A.
- 0 CA2 returns high on the next active CA1 transition following a read of Output Register A as specified by bit 1.

Figure 4. Control Line Operations Summary (1 of 2)

CONTROL REGISTER B (CRB)

CB2 INPUT MODE (BIT 5 = 0)

7	6	5	4	3	2	1	0
IRQB1 FLAG	IRQB2 FLAG	CB2 INPUT MODE SELECT (=0)	IRQB2 POSITIVE TRANSITION	$\overline{\text{IRQB}}$ ENABLE FOR IRQB2	DDRB/ORB SELECT	IRQB1 POSITIVE TRANSITION	$\overline{\text{IRQB}}$ ENABLE FOR IRQB1
			$\overline{\text{IRQB}}$/IRQB2 CONTROL			$\overline{\text{IRQB}}$/IRQB1 CONTROL	

CB2 OUTPUT MODE (BIT 5 = 1)

7	6	5	4	3	2	1	0
IRQB1 FLAG	0	CB2 OUTPUT MODE SELECT (=1)	CB2 OUTPUT CONTROL	CB2 RESTORE CONTROL	DDRB/ORB SELECT	IRQB1 POSITIVE TRANSITION	$\overline{\text{IRQB}}$ ENABLE FOR IRQB1
			CB2 CONTROL			$\overline{\text{IRQB}}$/IRQB1 CONTROL	

CB2 INPUT OR OUTPUT MODE (BIT 5 = 0 or 1)

Bit 7 IRQB1 FLAG
1 A transition has occurred on CB1 that satisfies the bit 1 IRQB1 transition polarity criteria. This bit is cleared by a read of Output Register B or by $\overline{\text{RES}}$.
0 No transition has occurred on CB1 that satisfies the bit 1 IRQB1 transition polarity criteria.

Bit 2 OUTPUT REGISTER B SELECT
1 Select Output Register B.
0 Select Data Direction Register B.

Bit 1 IRQB1 POSITIVE TRANSITION
1 Set IRQB1 Flag (bit 7) on a positive (low-to-high) transition of CB1.
0 Set IRQB1 Flag (bit 7) on a negative (high-to-low) transition of CB1.

Bit 0 $\overline{\text{IRQB}}$ ENABLE FOR IRQB1
1 Enable assertion of $\overline{\text{IRQB}}$ when IRQB1 Flag (bit 7) is set.
0 Disable assertion of $\overline{\text{IRQB}}$ when IRQB1 Flag (bit 7) is set.

CB2 INPUT MODE (BIT 5 = 0)

Bit 6 IRQB2 FLAG
1 A transition has occurred on CB2 that satisfies the bit 4 IRQB2 transition polarity criteria. This flag is cleared by a read of Output Register B or by $\overline{\text{RES}}$.
0 No transition has occurred on CB2 that satisfies the bit 4 IRQB2 transition polarity criteria.

Bit 5 CB2 MODE SELECT
0 Select CB2 Input Mode.

Bit 4 IRQB2 POSITIVE TRANSITION
1 Set IRQB2 Flag (bit 6) on a positive (low-to-high) transition of CB2.
0 Set IRQB2 Flag (bit 6) on a negative (high-to-low) transition of CB2.

Bit 3 $\overline{\text{IRQB}}$ ENABLE FOR IRQB2
1 Enable assertion of $\overline{\text{IRQB}}$ when IRQB2 Flag (bit 6) is set.
0 Disable assertion of $\overline{\text{IRQB}}$ when IRQB2 Flag (bit 6) is set.

CB2 OUTPUT MODE (BIT 5 = 1)

Bit 6 NOT USED
0 Always zero.

Bit 5 CB2 MODE SELECT
1 Select CB2 Output Mode.

Bit 4 CB2 OUTPUT CONTROL
1 CB2 goes low when a zero is written into CRB bit 3. CB2 goes high when a one is written into CRB bit 3.
0 CB2 goes low on the first negative (high-to-low) $\phi 2$ clock transition following a write to Output Register B. CB2 returns high as specified by bit 3.

Bit 3 CB2 WRITE STROBE RESTORE CONTROL (BIT 4 = 0)
1 CB2 returns high on the next $\phi 2$ clock negative transition following a write to Output Register B.
0 CB2 returns high on the next active CB1 transition following a write to Output Register B as specified by bit 1.

Figure 4. Control Line Operations Summary (2 of 2)

A second output mode allows CA2 to be used in conjunction with CA1 to "handshake" between the processor and the peripheral device. On the A side, this technique allows positive control of data transfers from the peripheral device into the microprocessor. The CA1 input signals the processor that data is available by interrupting the processor. The processor reads the data and sets CA2 low. This signals the peripheral device that it can make new data available.

The final output mode can be selected by setting bit 4 of CRA to a 1. In this mode, CA2 is a simple peripheral control output which can be set high or low by setting bit 3 or CRA to a 1 or a 0 respectively.

CB1 operates as an interrupt input only in the same manner as CA1. Bit 7 of CRB is set by the active transition selected by bit 0 of CRB. Likewise, the CB2 input mode operates exactly the same as the CA2 input modes. The CB2 output modes, CRB bit 5 = 1, differ somewhat from those of CA2. The pulse output occurs when the processor writes data into the Peripheral B Output Register. Also, the "handshaking" operates on data transfers from the processor into the peripheral device.

READING THE PERIPHERAL A I/O PORT

Performing a Read operation with RS1 = 0, RS0 = 0 and the Data Direction Register Access Control bit (CRA-2) = 1, directly transfers the data on the Peripheral A I/O lines to the data bus. In this situation, the data bus will contain both the input and output data. The processor must be programmed to recognize and interpret only those bits which are important to the particular peripheral operation being performed.

Since the processor always reads the Peripheral A I/O port pins instead of the actual Peripheral Output Register (ORA), it is possible for the data read by the processor to differ from the contents of the Peripheral Output Register for an output line. This is true when the I/O pin is not allowed to go to a full +2.4V DC when the Peripheral Output register contains a logic 1. In this case, the processor will read a 0 from the Peripheral A pin, even though the corresponding bit in the Peripheral Output register is a 1.

READING THE PERIPHERAL B I/O PORT

Reading the Peripheral B I/O port yields a combination of input and output data in a manner similar to the Peripheral A port. However, data is read directly from the Peripheral B Output Register (ORB) for those lines programmed to act as outputs. It is therefore possible to load down the Peripheral B Output lines without causing incorrect data to be transferred back to the processor on a Read operation.

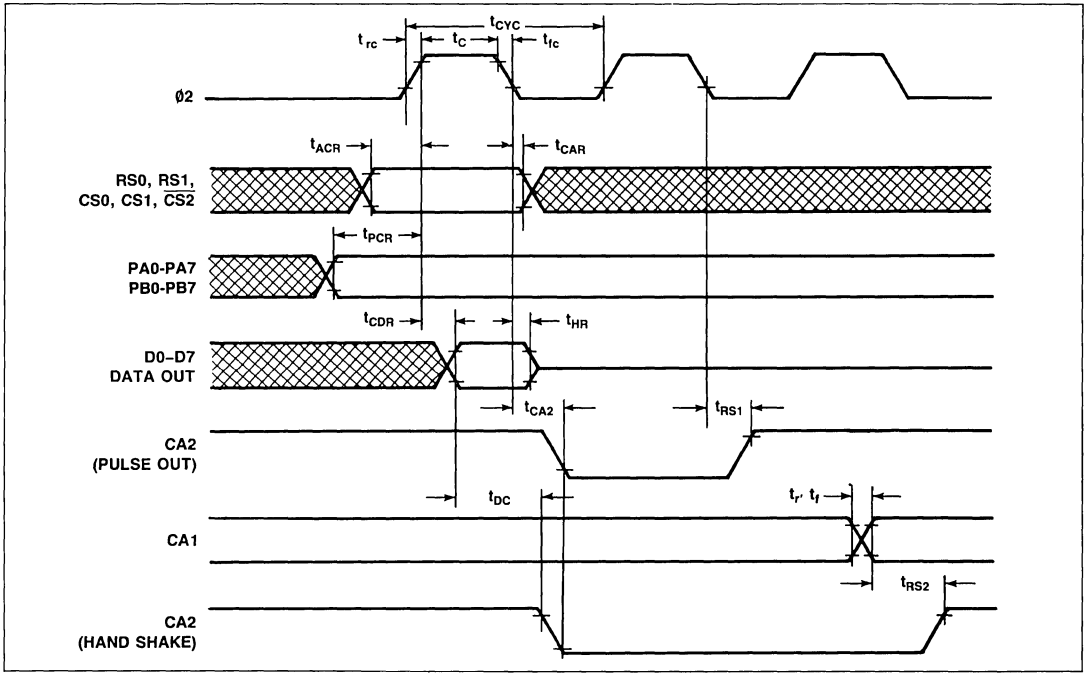


Figure 5. Read Timing Waveforms

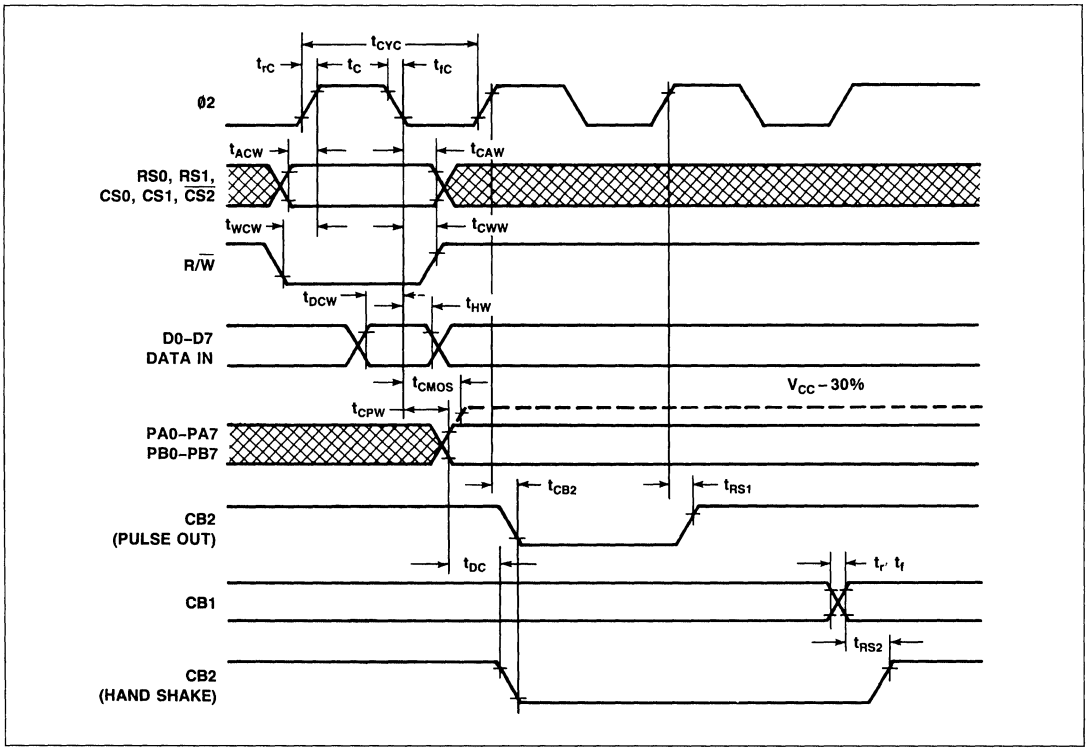


Figure 6. Write Timing Waveforms

BUS TIMING CHARACTERISTICS

Parameter	Symbol	1 MHz		2 MHz		Unit
		Min.	Max.	Min.	Max.	
Ø2 Cycle	t_{CYC}	1.0	—	0.5	—	μs
Ø2 Pulse Width	t_C	0.47	5	0.24	5	μs
Ø2 Rise and Fall Time	t_{rc}, t_{fc}	—	25	—	15	ns

READ TIMING

Address Set-Up Time	t_{ACR}	180	—	90	—	ns
Address Hold Time	t_{CAR}	0	—	0	—	ns
Peripheral Data Set-Up Time	t_{PCR}	300	—	150	—	ns
Data Bus Delay Time	t_{CDR}	—	395	—	190	ns
Data Bus Hold Time	t_{HR}	10	—	10	—	ns

WRITE TIMING

Address Set-Up Time	t_{ACW}	180	—	90	—	ns
Address Hold Time	t_{CAW}	0	—	0	—	ns
R/$\overline{W}$ Set-Up Time	t_{WCW}	130	—	65	—	ns
R/$\overline{W}$ Hold Time	t_{CWW}	50	—	25	—	ns
Data Bus Set-Up Time	t_{DCW}	300	—	150	—	ns
Data Bus Hold Time	t_{HW}	10	—	10	—	ns

PERIPHERAL INTERFACE TIMING

Peripheral Data Set-Up	t_{PCR}	300	—	150	—	ns
Peripheral Data Delay Time	t_{CDW}	—	1.0	—	0.5	μs
Peripheral Data Delay Time to CMOS Level	t_{CMOS}	—	2.0	—	1.0	μs
Ø2 Low to CA2 Low Delay	t_{CA2}	—	1.0	—	0.5	μs
Ø2 Low to CA2 High Delay	t_{RS1}	—	1.0	—	0.5	μs
CA1 Active to CA2 High Delay	t_{RS2}	—	2.0	—	1.0	μs
Ø2 High to CB2 Low Delay	t_{CB2}	—	1.0	—	0.5	μs
Peripheral Data Valid to CB2 Low Delay	t_{DC}	0	1.5	0	0.75	μs
Ø2 High to CB2 High Delay	t_{RS1}	—	1.0	—	0.5	μs
CB1 Active to CB2 High Delay	t_{RS2}	—	2.0	—	1.0	μs
CA1, CA2, CB1 and CB2 Input Rise and Fall Time	t_r, t_f	—	1.0	—	1.0	μs

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to +7.0	Vdc
Input Voltage	V_{IN}	−0.3 to +V_{CC}	Vdc
Operating Temperature Range Commercial Industrial	T_A	T_L T_H 0 to +70 −40 to +85	°C
Storage Temperature	T_{STG}	−55 to +150	°C

***NOTE:** Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the other sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING CONDITIONS

Parameter	Symbol	Value
Supply Voltage	V_{CC}	5V ±5%
Temperature Range Commercial Industrial	T_A	 0°C to 70°C −40°C to +85°C

DC CHARACTERISTICS

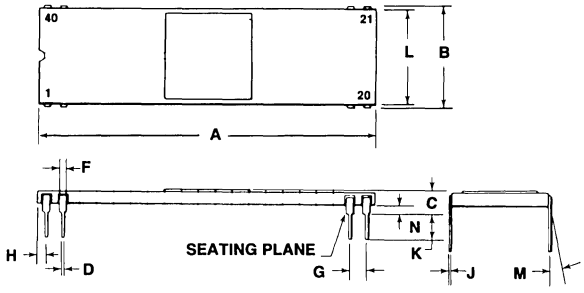
(V_{CC} = 5.0V ±5%, V_{SS} = 0, T_A = T_L to T_H, unless otherwise noted)

Parameter	Symbol	Min.	Typ.[3]	Max.	Unit[1]	Test Conditions
Input High Voltage	V_{IH}	+2.0	—	V_{CC}	V	
Input Low Voltage	V_{IL}	−0.3	—	+0.8	V	
Input Leakage Current R/$\overline{W}$, $\overline{RES}$, RS0, RS1, CS0, CS1, $\overline{CS2}$, CA1, CB1, Ø2	I_{IN}	—	±1	±2.5	µA	V_{IN} = 0V to 5.0V V_{CC} = 0V
Input Leakage Current for Three-State Off D0–D7, PB0–PB7, CB2	I_{TSI}	—	±2	±10	µA	V_{IN} = 0.4V to 2.4V V_{CC} = 5.25V
Input High Current PA0–PA7, CA2	I_{IH}	−100	−250	—	µA	V_{IH} = 2.4V
Input Low Current PA0–PA7, CA2	I_{IL}	—	−1	−1.6	mA	V_{IL} = 0.4V
Output High Voltage All outputs PB0–PB7, CB2 (Darlington Drive)	V_{OH}	 2.4 1.5	 — —	 — —	 V V	V_{CC} = 4.75V I_{LOAD} = −100µA I_{LOAD} = −1.0 mA
Output Low Voltage	V_{OL}	—	—	+0.4	V	V_{CC} = 4.75V I_{LOAD} = 1.6 mA
Output High Current (Sourcing) Logic PB0–PB7, CB2 (Darlington Drive)	I_{OH}	 −100 −1.0	 −1000 −2.5	 — −10	 µA mA	 V_{OH} = 2.4V V_{OH} = 1.5V
Output Low Current (Sinking)	I_{OL}	1.6	—	—	mA	V_{OL} = 0.4V
Output Leakage Current (Off State) $\overline{IRQA}$, $\overline{IRQB}$	I_{OFF}	—	1	±10	µA	V_{OH} = 2.4V V_{CC} = 5.25V
Power Dissipation	P_D		200	500	mW	
Input Capacitance D0–D7, PA0–PA7, PB0–PB7, CA2, CB2 R/$\overline{W}$, $\overline{RES}$, RS0, RS1, CS0, CS1, $\overline{CS2}$ CA1, CB1, Ø2	C_{IN}	 — — —	 — — —	 10 7.0 20	pF	V_{CC} = 5.0V V_{IN} = 0V f = 1 MHz T_A = 25°C
Output Capacitance	C_{OUT}	—	—	10	pF	

Notes:
1. All units are direct current (dc) except for capacitance.
2. Negative sign indicates outward current flow, positive indicates inward flow.
3. Typical values are shown for V_{CC} = 5.0V and T_A = 25°C.

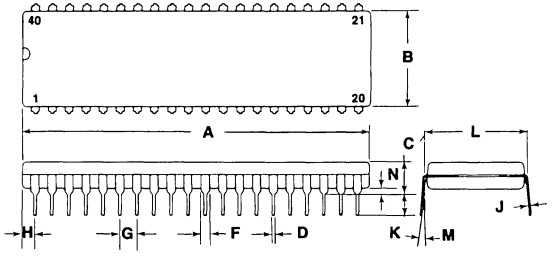
PACKAGE DIMENSIONS

40-PIN CERAMIC DIP



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	50 29	51 31	1 980	2 020
B	14 86	15 62	0 585	0 615
C	2 54	4 19	0 100	0 165
D	0 38	0 53	0 015	0 021
F	0 76	1 40	0 030	0 055
G	2 54 BSC		0 100 BSC	
H	0 76	1 78	0 030	0 070
J	0 20	0 33	0 008	0 013
K	2 54	4 19	0 100	0 165
L	14 60	15 37	0 575	0 605
M	0	10	0	10
N	0 51	1 52	0 020	0 060

40-PIN PLASTIC DIP



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	51 28	52 32	2 040	2 060
B	13 72	14 22	0 540	0 560
C	3 55	5 08	0 140	0 200
D	0 36	0 51	0 014	0 020
F	1 02	1 52	0 040	0 060
G	2 54 BSC		0 100 BSC	
H	1 65	2 16	0 065	0 085
J	0 20	0 30	0 008	0 012
K	3 30	4 32	0 130	0 170
L	15 24 BSC		0 600 BSC	
M	7	10	7	10
N	0 51	1 02	0 020	0 040

Rockwell

R6522
Versatile Interface Adapter (VIA)

DESCRIPTION

The R6522 Versatile Interface Adapter (VIA) is a very flexible I/O control device. In addition, this device contains a pair of very powerful 16-bit interval timers, a serial-to-parallel/parallel-to serial shift register and input data latching on the peripheral ports. Expanded handshaking capability allows control of bidirectional data transfers between VIA's in multiple processor systems.

The R6522 includes functions for programmed control of up to two peripheral devices (Ports A and B). These two program controlled 8-bit bidirectional peripheral I/O ports allow direct interfacing between the microprocessor and selected peripheral units. Each port has input data latching capability. Two programmable Data Direction Registers (A and B) allow selection of data direction (input or output) on an individual line basis.

The R6522 also has two programmable 16-bit Interval Timer/Counters with latches. Timer 1 may be operated in a One-Shot Interrupt Mode with interrupts on each count-to-zero, or in a Free-Run Mode with a continuous series of evenly spaced interrupts. Timer 2 functions as both an interval and pulse counter. Serial data transfers are provided by a serial-to-parallel/parallel-to-serial shift register. Application versatility is further increased by various control registers, including—the Interrupt Flag Register, the Interrupt Enable Register, the Auxiliary Control Register and the Peripheral Control Register.

FEATURES

- Two 8-bit bidirectional I/O ports
- Two 16-bit programmable timer/counters
- Serial bidirectional peripheral I/O
- TTL compatible peripheral control lines
- Expanded "handshake" capability allows positive control of data transfers between processor and peripheral devices.
- Latched output and input registers on both I/O ports
- 1 and 2 MHz operation
- Commercial and industrial temperature range versions
- Single +5 Vdc power requirement

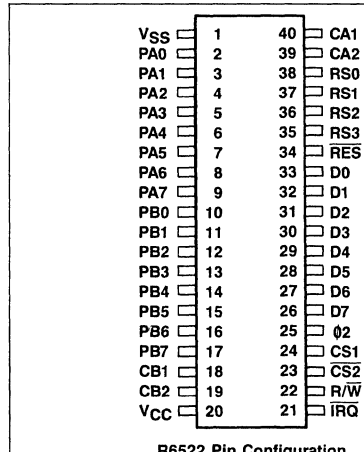
ORDERING INFORMATION

Part Number:
R6522 ___

Temperature Range
Blank = 0°C to +70°C
E = −40°C to +85°C

Package
C = Ceramic
P = Plastic

Frequency
No Letter = 1 MHz
A = 2 MHz



R6522 Pin Configuration

Figure 1. R6522 Pin Assignments

INTERFACE SIGNALS

Figure 1 (on the front page) shows the R6522 VIA pin assignments and Figure 2 groups the signals by functional interface.

RESET ($\overline{RES}$)

Reset ($\overline{RES}$) clears all internal registers (except T1 and T2 counters and latches, and the Shift Register (SR)). In the $\overline{RES}$ condition, all peripheral interface lines (PA and PB) are placed in the input state. Also, the Timers (T1 and T2), SR and interrupt logic are disabled from operation.

INPUT CLOCK (PHASE 2)

The system Phase 2 ($\phi 2$) Input Clock controls all data transfers between the R6522 and the microprocessor.

READ/WRITE (R/$\overline{W}$)

The direction of the data transfers between the R6522 and the system processor is controlled by the R/$\overline{W}$ line in conjunction with the CS1 and $\overline{CS2}$ inputs. When R/$\overline{W}$ is low (write operation) and the R6522 is selected, data is transferred from the processor bus into the selected R6522 register. When R/$\overline{W}$ is high (read operation) and the R6522 is selected, data is transferred from the selected R6522 register to the processor bus.

DATA BUS (D0–D7)

The eight bidirectional Data Bus lines transfer data between the R6522 and the microprocessor. During a read operation, the contents of the selected R6522 internal register are transferred to the microprocessor via the Data Bus lines. During a write operation, the Data Bus lines serve as high impedance inputs over which data is transferred from the microprocessor to a selected R6522 register. The Data Bus lines are in the high impedance state when the R6522 is unselected.

CHIP SELECTS (CS1, $\overline{CS2}$)

Normally, the two chip select lines are connected to the microprocessor address lines. This connection may be direct or through decoding. To access a selected R6522 register, CS1 must be high (logic 1) and $\overline{CS2}$ must be low (logic 0).

REGISTER SELECTS (RS0–RS3)

The Register Select inputs allow the microprocessor to select one of 16 internal registers within the R6522. Refer to Table 1 for Register Select coding and a functional description.

REGISTER SELECTS (RS0–RS3)

The Register Select inputs allow the microprocessor to select one of 16 internal registers within the R6522. Refer to Table 1 for Register Select coding and a functional description.

INTERRUPT REQUEST ($\overline{IRQ}$)

The Interrupt Request ($\overline{IRQ}$) output signal is generated whenever an internal Interrupt Flag bit is set and the corresponding Interrupt Enable bit is a Logic 1. The Interrupt Request output is an

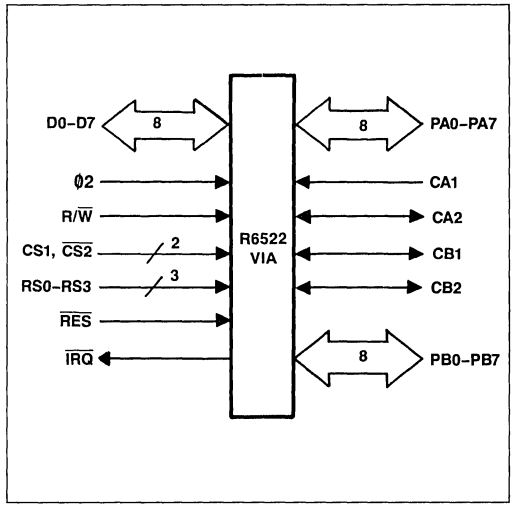


Figure 2. R6522 VIA Interface Signals

open-drain configuration, thus allowing the $\overline{IRQ}$ signal to be wire-ORed to a common microprocessor $\overline{IRQ}$ input line.

PORT A DATA LINES (PA0–PA7)

Peripheral Data Port A is an 8-line, bidirectional bus for the transfer of data, control and status information between the R6522 and a peripheral device. Each Peripheral Data Port bus line may be individually programmed as either an input or output under control of a Data Direction Register. Data flow direction may be selected on a line-by-line basis with intermixed input and output lines within the same port. When a "0" is written to any bit position of the Data Direction Register, the corresponding line will be programmed as an input. When a "1" is written into any bit position of the register, the corresponding data line will serve as an output. Polarity of the data output is determined by the Output Register, while input data may be latched into the Input Register under control of the CA1 line. All modes are program controlled by the microprocessor by way of the R6522's internal control registers. Each Peripheral Data Port line represents one TTL load in the input mode and will drive one standard TTL load in the output mode. A typical output circuit for Peripheral Data Port A is shown in Figure 3.

PORT A CONTROL LINES (CA1, CA2)

Control lines CA1 and CA2 serve as interrupt inputs or handshake outputs for Peripheral Data Port A. Each line controls an internal Interrupt Flag with a corresponding Interrupt Enable bit. CA1 also controls the latching of Input Data on Port A. CA1 is a high impedance input, while CA2 represents one standard TTL load in the input mode. In the output mode, CA2 will drive one standard TTL load.

PORT B DATA LINES (PB0–PB7)

Peripheral Data Port B is an 8-line, bidirectional bus which is controlled by an Output Register, Input Register and Data Direction Register in a manner much the same as Data Port A. With respect to Port B, the output signal on line PB7 may be controlled by Timer 1 while Timer 2 may be programmed to count pulses on the PB6 line. Port B lines represent one standard TTL load in the input mode and will drive one TTL load in the output mode. Port B lines are also capable of sourcing 1.0 mA at 1.5 Vdc in the output mode. This allows the outputs to directly drive Darlington transistor circuits. A typical output circuit for Port B is shown in Figure 3.

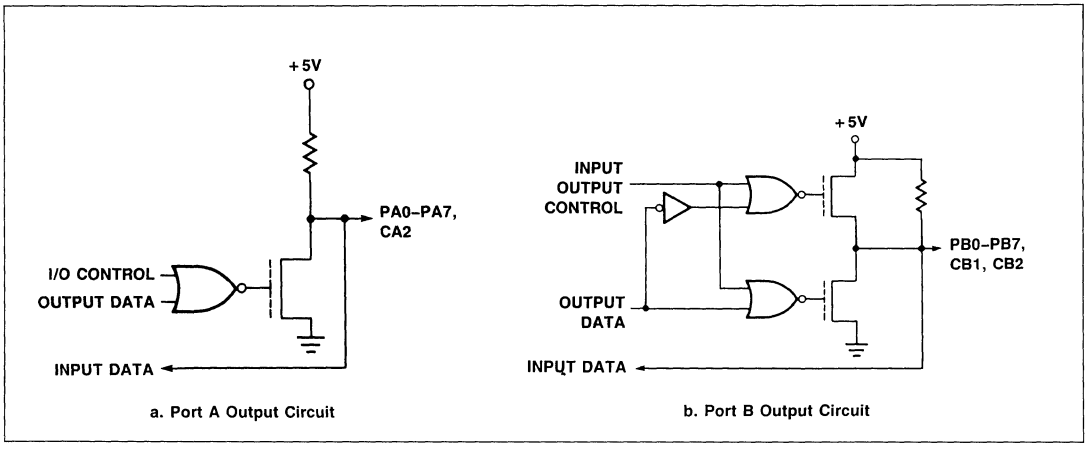
PORT B CONTROL LINES (CB1, CB2)

Control lines CB1 and CB2 serve as interrupt inputs or handshake outputs for Peripheral Data Port B. Like Port A, these two control lines control an internal Interrupt Flag with a corresponding Interrupt Enable bit. Similar to CA1, CB1 controls the latching of input data on Port B. These lines also serve as a serial data port under control of the Shift Register (SR). Each control line represents one standard TTL load in the input mode and can drive one TTL load in the output mode. CB2 can also drive a Darlington transistor circuit; however, CB1 cannot.

Table 1. R6522 Register Addressing

Register Number	RS Coding				Register Desig.	Register/Description	
	RS3	RS2	RS1	RS0		Write (R/$\overline{W}$ = L)	Read (R/$\overline{W}$ = H)
0	0	0	0	0	ORB/IRB	Output Register B	Input Register B
1	0	0	0	1	ORA/IRA	Output Register A	Input Register A
2	0	0	1	0	DDRB	Data Direction Register B	
3	0	0	1	1	DDRA	Data Direction Register A	
4	0	1	0	0	T1C-L	T1 Low-Order Latches	T1 Low-Order Counter
5	0	1	0	1	T1C-H	T1 High-Order Counter	
6	0	1	1	0	T1L-L	T1 Low-Order Latches	
7	0	1	1	1	T1L-H	T1 High-Order Latches	
8	1	0	0	0	T2C-L	T2 Low-Order Latches	T2 Low-Order Counter
9	1	0	0	1	T2C-H	T2 High-Order Counter	
10	1	0	1	0	SR	Shift Register	
11	1	0	1	1	ACR	Auxiliary Control Register	
12	1	1	0	0	PCR	Peripheral Control Register	
13	1	1	0	1	IFR	Interrupt Flag Register	
14	1	1	1	0	IER	Interrupt Enable Register	
15	1	1	1	1	ORA/IRA	Output Register A*	Input Register A*

NOTE: *Same as Register 1 except no handshake.



a. Port A Output Circuit

b. Port B Output Circuit

Figure 3. Port A and B Output Circuits

FUNCTIONAL DESCRIPTION

The internal organization of the R6522 VIA is illustrated in Figure 4.

PORT A AND PORT B OPERATION

The R6522 VIA has two 8-bit bidirectional I/O ports (Port A and Port B) and each port has two associated control lines.

Each 8-bit peripheral port has a Data Direction Register (DDRA, DDRB) for specifying whether the peripheral pins are to act as inputs or outputs. A "0" in a bit of the Data Direction Register causes the corresponding peripheral pin to act as an input. A "1" causes the pin to act as an output.

Each peripheral pin is also controlled by a bit in the Output Register (ORA, ORB) and the Input Register (IRA, IRB). When the pin is programmed as an output, the voltage on the pin is controlled by the corresponding bit of the Output Register. A "1" in the Output Register causes the output to go high, and a "0" causes the output to go low. Data may be written into Output Register bits corresponding to pins which are programmed as inputs. In this case, however, the output signal is unaffected.

Reading a peripheral port causes the contents of the Input Register (IRA, IRB) to be transferred onto the Data Bus. With input latching disabled, IRA will always reflect the levels on the PA pins. With input latching enabled, IRA will reflect the levels on the PA pins at the time the latching occurred (via CA1).

The IRB register operates similar to the IRA register. However, for pins programmed as outputs there is a difference. When reading IRA, the *level on the pin* determines whether a "0" or a "1" is sensed. When reading IRB, however, the bit stored in the *output register,* ORB, is the bit sensed. Thus, for outputs which have large loading effects and which pull an output "1" down or which pull an output "0" up, reading IRA may result in reading a "0" when a "1" was actually programmed, and reading a "1" when a "0" was programmed. Reading IRB, on the other hand, will read the "1" or "0" level actually programmed, no matter what the loading on the pin.

Figures 5 through 8 illustrate the formats of the port registers.

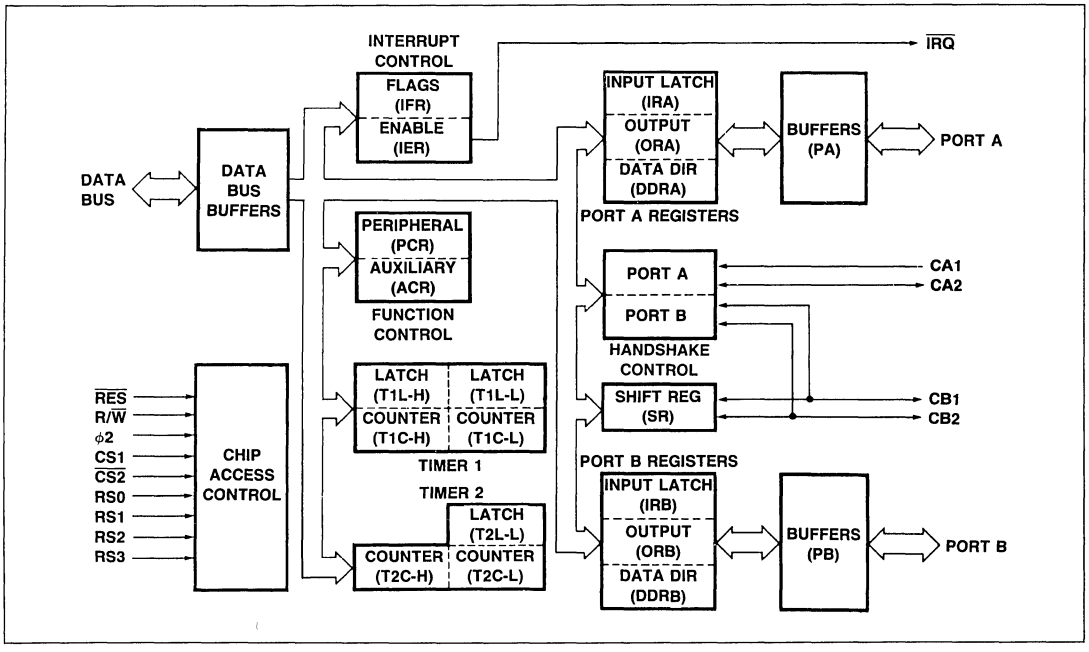


Figure 4. R6522 VIA Block Diagram

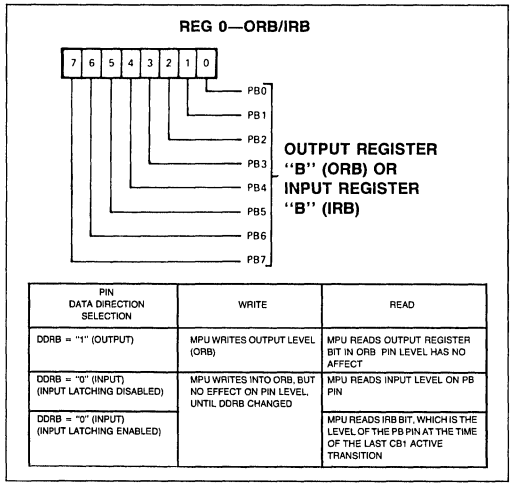
HANDSHAKE CONTROL OF DATA TRANSFERS

The R6522 allows positive control of data transfers between the system processor and peripheral devices through the operation of "handshake" lines. Port A lines (CA1, CA2) handshake data on both a read and a write operation while the Port B lines (CB1, CB2) handshake on a write operation only.

Read Handshake

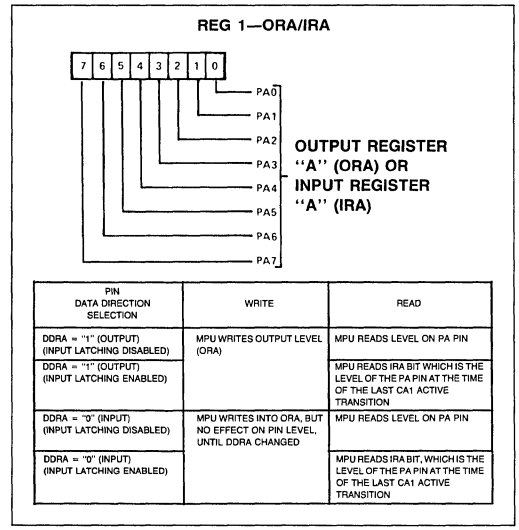
Positive control of data transfers from peripheral devices into the system processor can be accomplished very effectively using Read Handshaking. In this case, the peripheral device must generate the equivalent of a "Data Ready" signal to the processor signifying that valid data is present on the peripheral port. This signal normally interrupts the processor, which then reads the data, causing generation of a "Data Taken" signal. The peripheral device responds by making new data available. This process continues until the data transfer is complete.

In the R6522, automatic "Read" Handshaking is possible on the Peripheral A port only. The CA1 interrupt input pin accepts the "Data Ready" signal and CA2 generates the "Data Taken" signal. The "Data Ready" signal will set an internal flag which may interrupt the processor or which may be polled under program control. The "Data Taken" signal can either be a pulse or a level which is set low by the system processor and is cleared by the "Data Ready" signal. These options are shown in Figure 9 which illustrates the normal Read Handshake sequence.



PIN DATA DIRECTION SELECTION	WRITE	READ
DDRB = "1" (OUTPUT)	MPU WRITES OUTPUT LEVEL (ORB)	MPU READS OUTPUT REGISTER BIT IN ORB PIN LEVEL HAS NO AFFECT
DDRB = "0" (INPUT) (INPUT LATCHING DISABLED)	MPU WRITES INTO ORB, BUT NO EFFECT ON PIN LEVEL, UNTIL DDRB CHANGED	MPU READS INPUT LEVEL ON PB PIN
DDRB = "0" (INPUT) (INPUT LATCHING ENABLED)		MPU READS IRB BIT, WHICH IS THE LEVEL OF THE PB PIN AT THE TIME OF THE LAST CB1 ACTIVE TRANSITION

Figure 5. Output Register B (ORB), Input Register B (IRB)



PIN DATA DIRECTION SELECTION	WRITE	READ
DDRA = "1" (OUTPUT) (INPUT LATCHING DISABLED)	MPU WRITES OUTPUT LEVEL (ORA)	MPU READS LEVEL ON PA PIN
DDRA = "1" (OUTPUT) (INPUT LATCHING ENABLED)		MPU READS IRA BIT WHICH IS THE LEVEL OF THE PA PIN AT THE TIME OF THE LAST CA1 ACTIVE TRANSITION
DDRA = "0" (INPUT) (INPUT LATCHING DISABLED)	MPU WRITES INTO ORA, BUT NO EFFECT ON PIN LEVEL, UNTIL DDRA CHANGED	MPU READS LEVEL ON PA PIN
DDRA = "0" (INPUT) (INPUT LATCHING ENABLED)		MPU READS IRA BIT, WHICH IS THE LEVEL OF THE PA PIN AT THE TIME OF THE LAST CA1 ACTIVE TRANSITION

Figure 6. Output Register A (ORA), Input Register A (IRA)

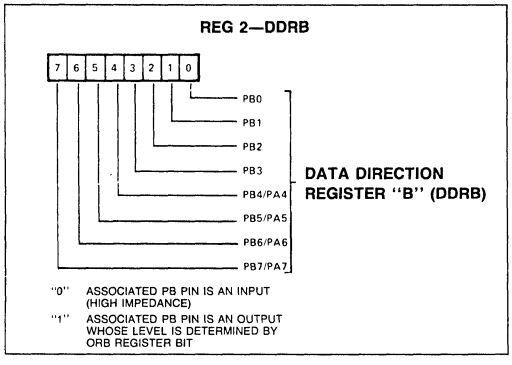


Figure 7. Data Direction Register B (DDRB)

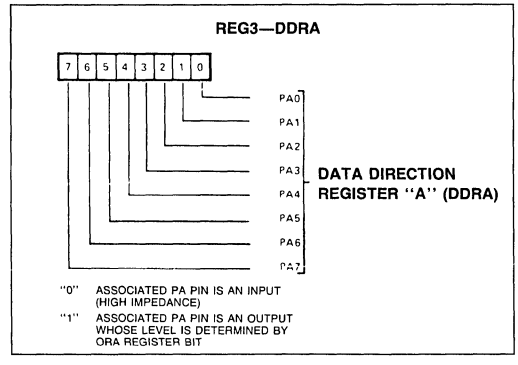


Figure 8. Data Direction Register A (DDRA)

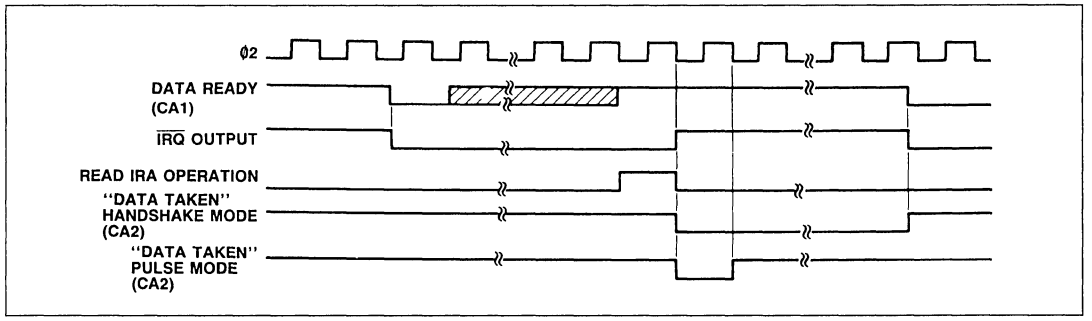


Figure 9. Read Handshake Timing (Port A Only)

Write Handshake

The sequence of operations which allows handshaking data from the system processor to a peripheral device is very similar to that described for Read Handshaking. However, for Write Handshaking, the R6522 generates the "Data Ready" signal and the peripheral device must respond with the "Data Taken" signal. This can be accomplished on both the PA port and the PB port on the R6522. CA2 or CB2 act as a "Data Ready" output in either the handshake mode or pulse mode and CA1 or CB1 accept the "Data Taken" signal from the peripheral device, setting the interrupt flag and clearing the "Data Ready" output. This sequence is shown in Figure 10.

Latching

The PA port and the PB port on the R6522 can be enabled in the Auxiliary Control Register (Figure 14) to be latched by their individual port control lines (CA1, CB1). Latching is selectable to be on the rising or falling edge of the signal at each individual port control line. Selection of operating modes for CA1, CA2, CB1 and CB2 is accomplished by the Peripheral Control Register (Figure 11).

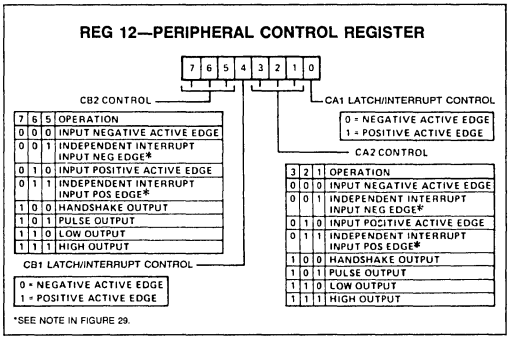


Figure 11. Peripheral Control Register (PCR)

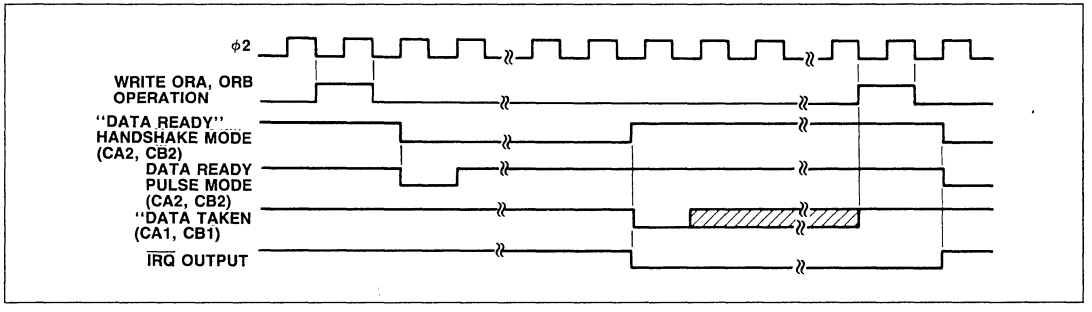


Figure 10. Write Handshake Timing

COUNTER/TIMERS

There are two independent 16-bit counter/timers (called Timer 1 and Timer 2) in the R6522. Each timer is controlled by writing bits into the Auxiliary Control Register (ACR) to select the mode of operation (Figure 14).

Timer 1 Operation

Interval Timer T1 consists of two 8-bit latches (Figure 12) and a 16-bit counter (Figure 13). The latches store data which is to be loaded into the counter. After loading, the counter decrements at $\phi 2$ clock rate. Upon reaching zero, an interrupt flag is set, and IRQ goes low if the T1 interrupt is enabled. Timer 1 then disables any further interrupts and automatically transfers the contents of the latches into the counter and continues to decrement. In addition, the timer may be programmed to invert the output signal on peripheral pin PB7 each time it "times-out". Each of these modes is discussed separately below.

Note that the processor does not write directly into the low-order counter (T1C-L). Instead, this half of the counter is loaded automatically from the low order latch (T1L-L) when the processor writes into the high order counter (T1C-H). In fact, it may not be necessary to write to the low order counter in some applications since the timing operation is triggered by writing to the high order latch.

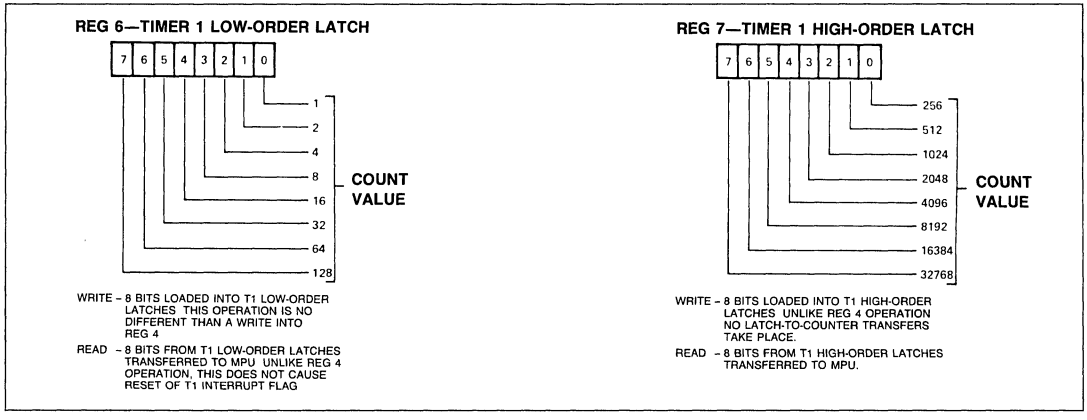


Figure 12. Timer 1 (T1) Latch Registers

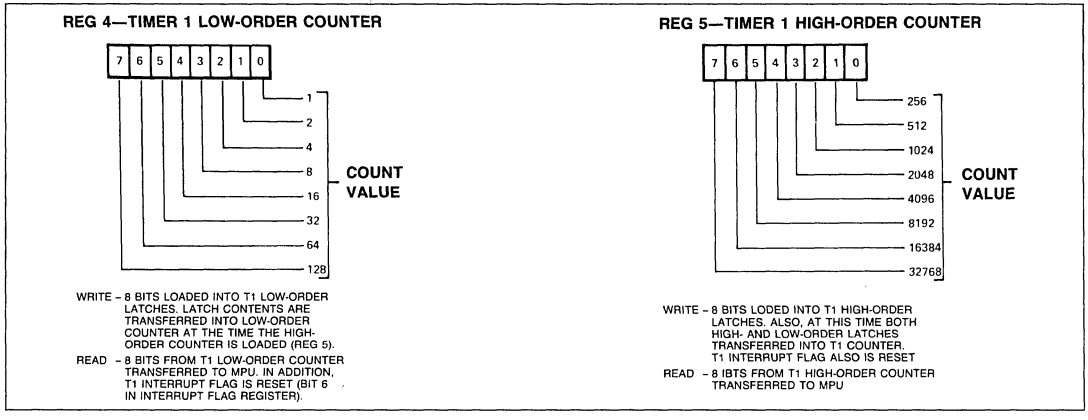


Figure 13. Timer 1 (T1) Counter Registers

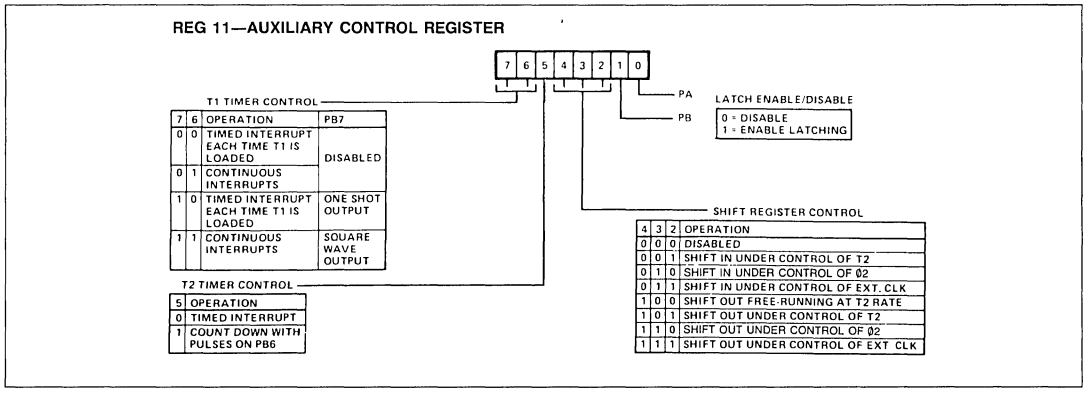


Figure 14. Auxiliary Control Register (ACR)

Timer 1 One-Shot Mode

The Timer 1 one-shot mode generates a single interrupt for each timer load operation. As with any interval timer, the delay between the "write T1C-H" operation and generation of the processor interrupt is a direct function of the data loaded into the timing counter. In addition to generating a single interrupt, Timer 1 can be programmed to produce a single negative pulse on the PB7 peripheral pin. With the output enabled (ACR7 = 1) a "write T1C-H" operation will cause PB7 to go low. PB7 will return high when Timer 1 times out. The result is a single programmable width pulse.

Timing for the R6522 interval timer one-shot modes is shown in Figure 15.

In the one-shot mode, writing into the T1L-H has no effect on the operation of Timer 1. However, it will be necessary to assure that the low order latch contains the proper data before initiating the count-down with a "write T1C-H" operation. When the processor writes into the high order counter (T1C-H), the T1 interrupt flag will be cleared, the contents of the low order latch will be transferred into the low order counter, and the timer will begin to decrement at system clock rate. If the PB7 output is enabled, this signal will go low on the falling edge of Ø2 following the write operation. When the counter reaches zero, the T1 interrupt flag will be set, the $\overline{IRQ}$ pin will go low (interrupt enabled), and the signal on PB7 will go high. At this time the counter will continue to decrement at system clock rate. This allows the system processor to read the contents of the counter to determine the time since interrupt. However, the T1 interrupt flag cannot be set again unless it has been cleared as described in this specification.

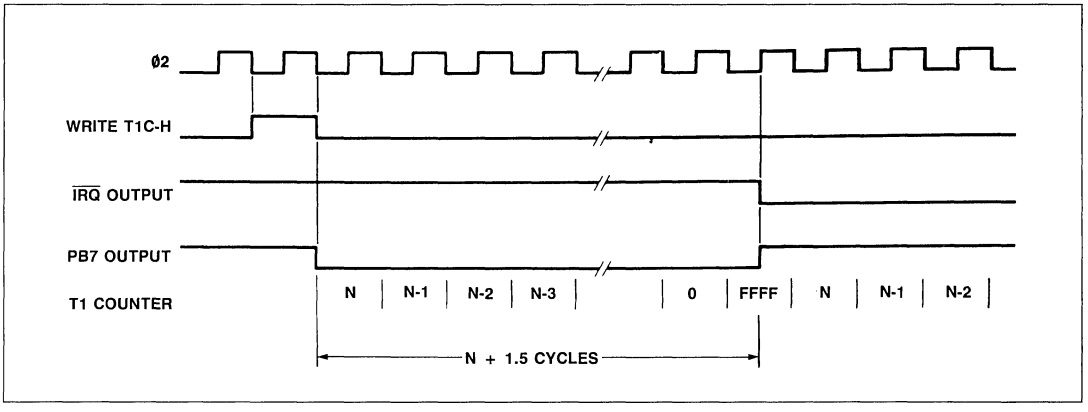


Figure 15. Timer 1 One-Shot Mode Timing

Timer 1 Free-Run Mode

The most important advantage associated with the latches in T1 is the ability to produce a continuous series of evenly spaced interrupts and the ability to produce a square wave on PB7 whose frequency is not affected by variations in the processor interrupt response time. This is accomplished in the "free-running" mode.

In the free-running mode, the interrupt flag is set and the signal on PB7 is inverted each time the counter reaches zero at which time the timer automatically transfers the contents of the latch into the counter (16 bits) and continues to decrement from there. The interrupt flag can be cleared by writing T1C-H or T1L-H, by reading T1C-L, or by writing directly into the flag as described later. However, it is not necessary to rewrite the timer to enable setting the interrupt flag on the next time-out.

All interval timers in the R6522 are "re-triggerable". Rewriting the counter will always re-initialize the time-out period. In fact, the time-out can be prevented completely if the processor continues to rewrite the timer before it reaches zero. Timer 1 will operate in this manner if the processor writes into the high order counter (T1C-H). However, by loading the latches only, the processor can access the timer during each down-counting operation without affecting the time-out in process. Instead, the data loaded into the latches will determine the length of the next time-out period. This capability is particularly valuable in the free-running mode with the output enabled. In this mode, the signal on PB7 is inverted and the interrupt flag is set with each time-out. By responding to the interrupts with new data for the latches, the processor can determine the period of the next half cycle during each half cycle of the output signal on PB7. In this manner, very complex waveforms can be generated.

A precaution to take in the use of PB7 as the timer output concerns the Data Direction Register contents for PB7. *Both* DDRB bit 7 and ACR bit 7 must be 1 for PB7 to function as the timer output. If one is 1 and other is 0, then PB7 functions as a normal outpin pin, controlled by ORB bit 7.

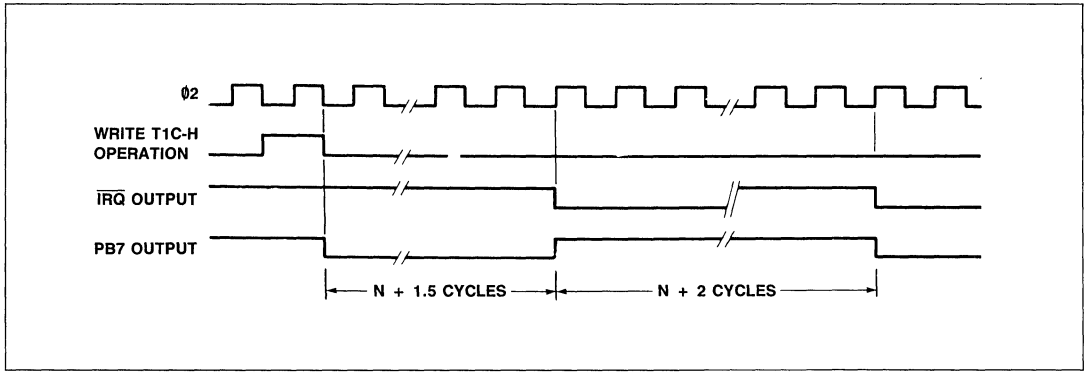


Figure 16. Timer 1 Free-Run Mode Timing

Timer 2 Operation

Timer 2 operates as an interval timer (in the "one-shot" mode only), or as a counter for counting negative pulses on the PB6 peripheral pin. A single control bit in the Auxiliary Control Register selects between these two modes. This timer is comprised of a "write-only" lower-order latch (T2L-L), a "read-only" low-order counter (T2C-L) and a read/write high order counter (T2C-H). The counter registers act as a 16-bit counter which decrements at Ø2 rate. Figure 17 illustrates the T2 Latch/Counter Registers.

Timer 2 One-Shot Mode

As an interval timer, T2 operates in the "one-shot" mode similar to Timer 1. In this mode, T2 provides a single interrupt for each "write T2C-H" operation. After timing out, the counter will continue to decrement. However, setting of the interrupt flag is disabled after initial time-out so that it will not be set by the counter decrementing again through zero. The processor must rewrite T2C-H to enable setting of the interrupt flag. The interrupt flag is cleared by reading T2C-L or by writing T2C-H. Timing for this operation is shown in Figure 18.

Timer 2 Pulse Counting Mode

In the pulse counting mode, T2 counts a predetermined number of negative-going pulses on PB6. This is accomplished by first loading a number into T2. Writing into T2C-H clears the interrupt flag and allows the counter to decrement each time a pulse is applied to PB6. The interrupt flag is set when T2 counts down past zero. The counter will then continue to decrement with each pulse on PB6. However, it is necessary to rewrite T2C-H to allow the interrupt flag to set on a subsequent time-out. Timing for this mode is shown in Figure 19. The pulse must be low on the leading edge of Ø2.

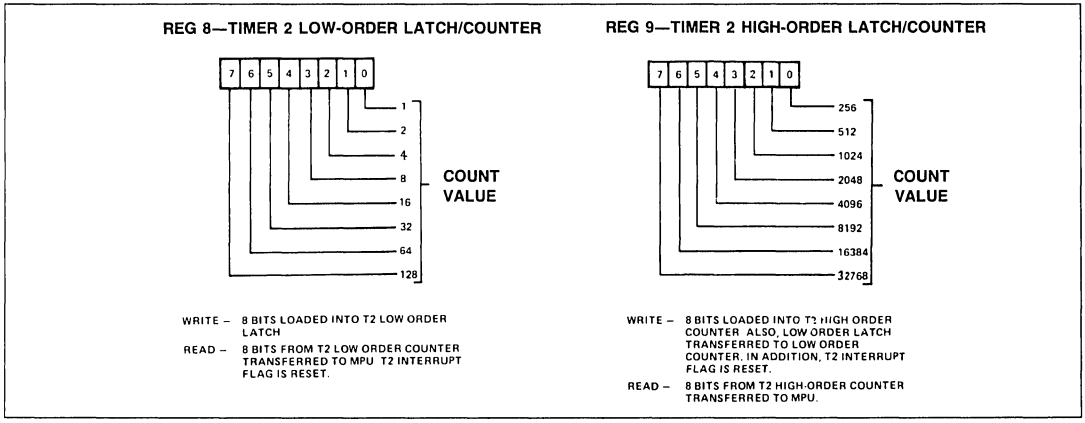


Figure 17. Timer 2 (T2) Latch/Counter Registers

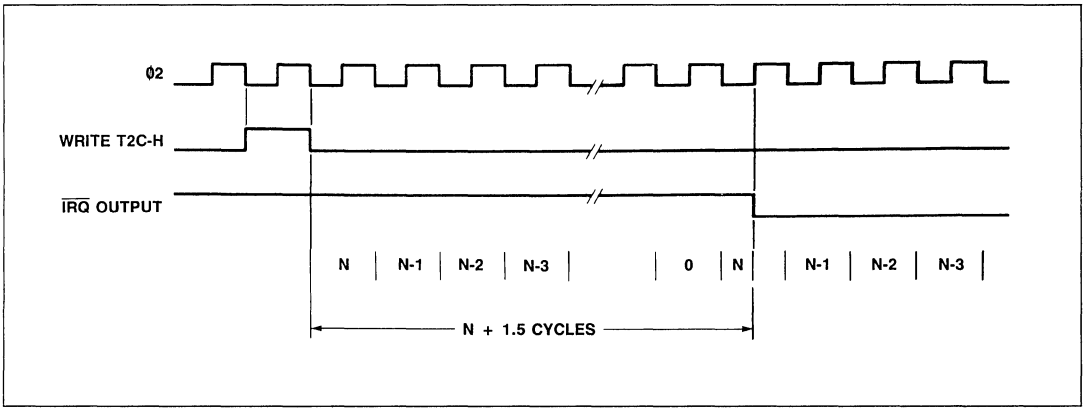


Figure 18. Timer 2 One-Shot Mode Timing

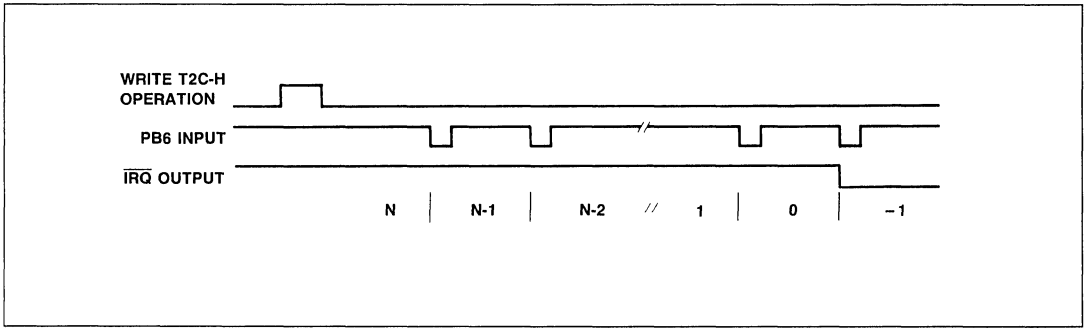


Figure 19. Timer 2 Pulse Counting Mode

SHIFT REGISTER OPERATION

The Shift Register (SR) performs serial data transfers into and out of the CB2 pin under control of an internal modulo-8 counter. Serial data transfer in and out of the Shift Register (SR) begin with the most significant bit (MSB) first. Shift pulses can be applied to the CB1 pin from an external source or, with the proper mode selection, shift pulses generated internally will appear on the CB1 pin for controlling external devices.

The control bits which select the various shift register operating modes are located in the Auxiliary Control Register. Figure 20 illustrates the configuration of the SR data bits and Figure 21 shows the SR control bits of the ACR.

SR Mode 0 — Shift Register Interrupt Disabled

Mode 0 disables the Shift Register interrupt. In this mode the microprocessor can write or read the SR and the SR will shift on each CB1 positive edge shifting in the value on CB2. In this mode the SR interrupt Flag is disabled (held to a logic 0).

SR Mode 1 — Shift In Under Control of T2

In mode 1, the shifting rate is controlled by the low order 8 bits of T2 (Figure 22). Shift pulses are generated on the CB1 pin to control shifting in external devices. The time between transitions of this output clock is a function of the system clock period and the contents of the low order T2 latch (N).

The shifting operation is triggered by the read or write of the SR if the SR flag is set in the IFR. Otherwise the first shift will occur at the next time-out of T2 after a read or write of the SR. The input data should change before the positive-going edge of CB1 clock pulse. This data is shifted into the shift register during the $\phi 2$ clock cycle following the positive-going edge of the CB1 clock pulse. The minimum CB1 positive pulse width must be one clock period. After 8 CB1 clock pulses, the shift register interrupt flag will set and $\overline{IRQ}$ will go low.

SR Mode 2 — Shift In Under $\phi 2$ Control

In mode 2, the shift rate is a direct function of the system clock frequency (Figure 23). CB1 becomes an output which generates shift pulses for controlling external devices. Timer 2 operates as an independent interval timer and has no effect on SR. The shifting operation is triggered by reading or writing the Shift Register. Data is shifted, first into bit 0 and is then shifted into the next higher order bit of the shift register on the trailing edge of each $\phi 2$ clock pulse. After 8 clock pulses, the shift register interrupt flag will be set, and the output clock pulses on CB1 will stop.

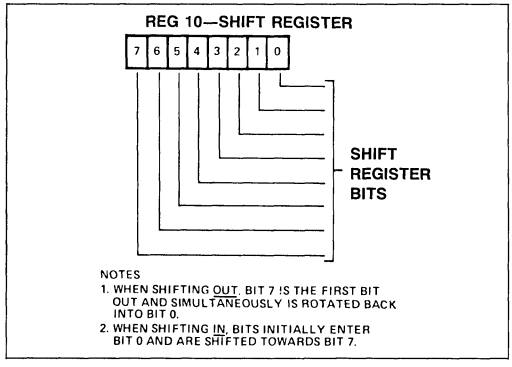
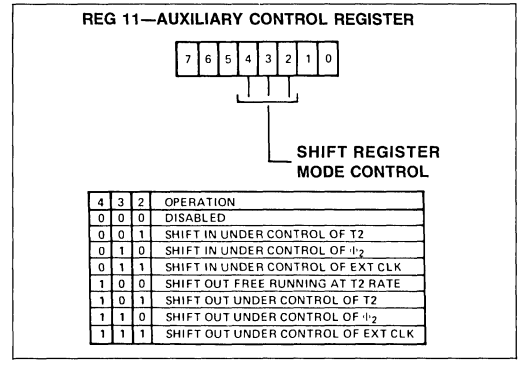


Figure 20. Shift Register



4	3	2	OPERATION
0	0	0	DISABLED
0	0	1	SHIFT IN UNDER CONTROL OF T2
0	1	0	SHIFT IN UNDER CONTROL OF $\phi 2$
0	1	1	SHIFT IN UNDER CONTROL OF EXT CLK
1	0	0	SHIFT OUT FREE RUNNING AT T2 RATE
1	0	1	SHIFT OUT UNDER CONTROL OF T2
1	1	0	SHIFT OUT UNDER CONTROL OF $\phi 2$
1	1	1	SHIFT OUT UNDER CONTROL OF EXT CLK

Figure 21. Shift Register Modes

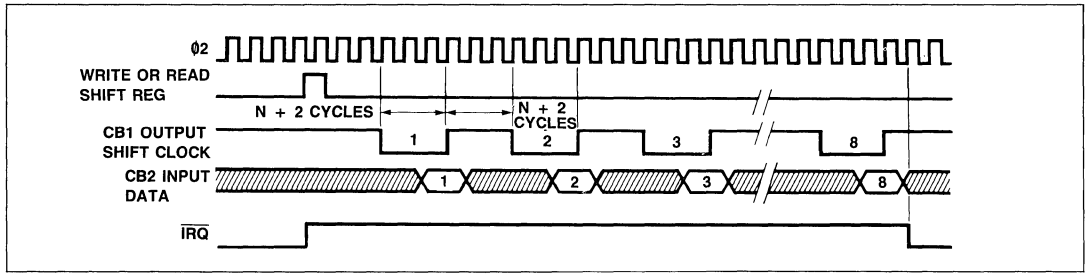


Figure 22. SR Mode 1 — Shift In Under T2 Control

SR Mode 3 — Shift In Under CB1 Control

In mode 3, external pin CB1 becomes an input (Figure 24). This allows an external device to load the shift register at its own pace. The shift register counter will interrupt the processor each time 8 bits have been shifted in. The shift register stops after 8 counts and must be reset to start again. Reading or writing the Shift Register resets the Interrupt Flag and initializes the SR counter to count another 8 pulses.

Note that the data is shifted during the first system clock cycle following the positive-going edge of the CB1 shift pulse. For this reason, data must be held stable during the first full cycle following CB1 going high. The minimum CB1 positive pulse width must be one clock period.

SR Mode 4 — Shift Out Under T2 Control (Free-Run)

Mode 4 is very similar to mode 1 in which the shifting rate is set by T2. However, in mode 4 the SR Counter does not stop the shifting operation (Figure 25). Since the Shift Register bit 7 (SR7) is recirculated back into bit 0, the 8 bits loaded into the shift register will be clocked onto CB2 repetitively. In this mode the shift register counter is disabled.

SR Mode 5 — Shift Out Under T2 Control

In mode 5, the shift rate is controlled by T2 (as in mode 1). The shifting operation is triggered by the read or write of the SR if the SR flag is set in the IFR (Figure 26). Otherwise the first shift will occur at the next time-out of T2 after a read or write of the SR. However, with each read or write of the shift register the SR Counter is reset and 8 bits are shifted onto CB2. At the same time, 8 shift pulses are generated on CB1 to control shifting in external devices. After the 8 shift pulses, the shifting is disabled, the SR Interrupt Flag is set and CB2 remains at the last data level.

2

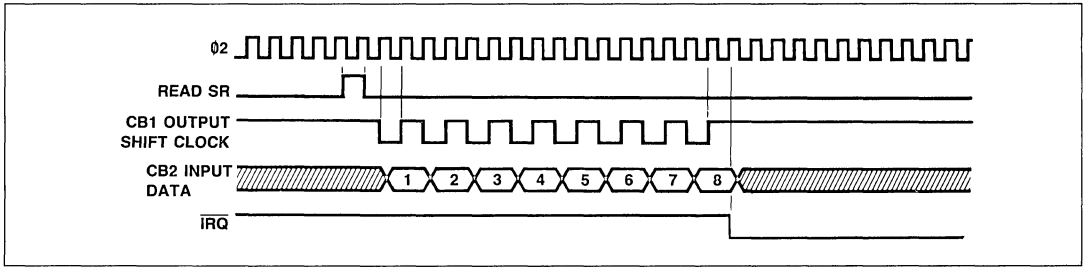


Figure 23. SR Mode 2 — Shift In Under Ø2 Control

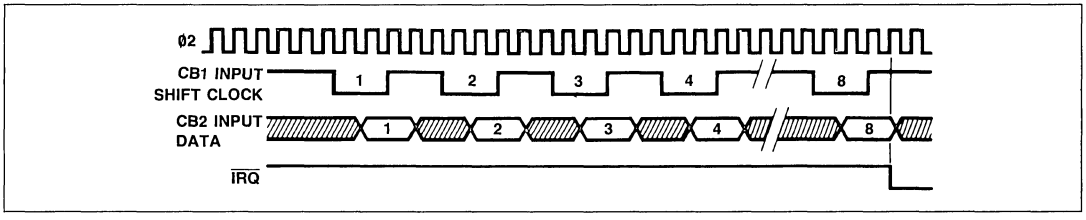


Figure 24. SR Mode 3 — Shift In Under CB1 Control

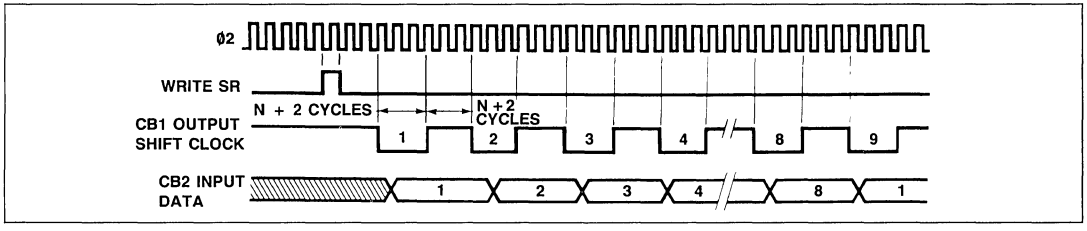


Figure 25. SR Mode 4 — Shift Out Under T2 Control (Free-Run)

SR Mode 6 — Shift Out Under Ø2 Control

In mode 6, the shift rate is controlled by the Ø2 system clock (Figure 27).

SR Mode 7 — Shift Out Under CB1 Control

In mode 7, shifting is controlled by pulses applied to the CB1 pin by an external device (Figure 28). The SR counter sets the SR Interrupt Flag each time it counts 8 pulses but it does not disable the shifting function. Each time the microprocessor, writes or reads the shift register, the SR Interrupt Flag is reset and the SR counter is initialized to begin counting the next 8 shift pulses on pin CB1. After 8 shift pulses, the Interrupt Flag is set. The microprocessor can then load the shift register with the next byte of data.

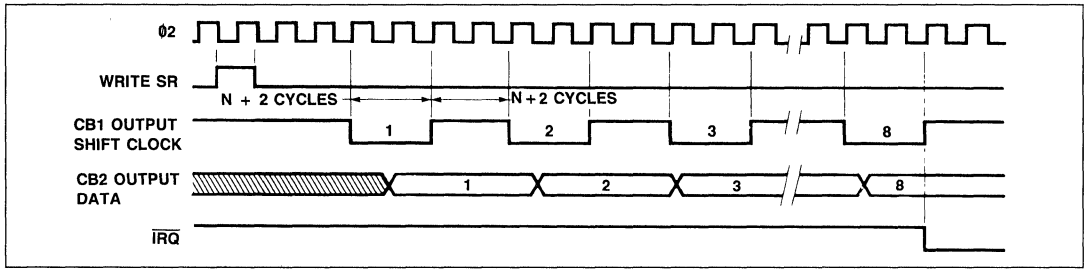


Figure 26. SR Mode 5 — Shift Out Under T2 Control

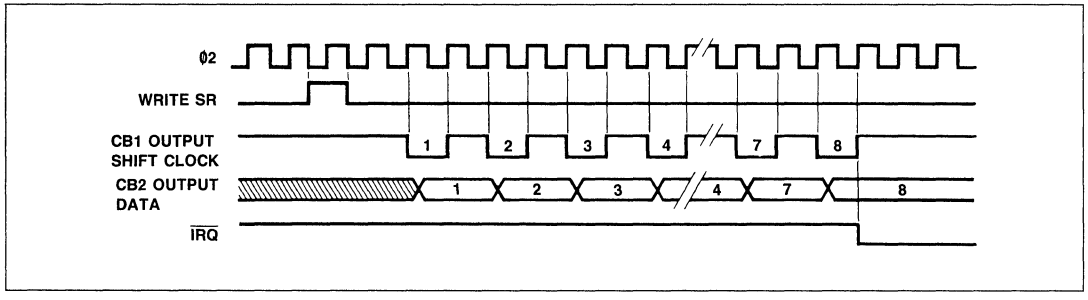


Figure 27. SR Mode 6 — Shift Out Under Ø2 Control

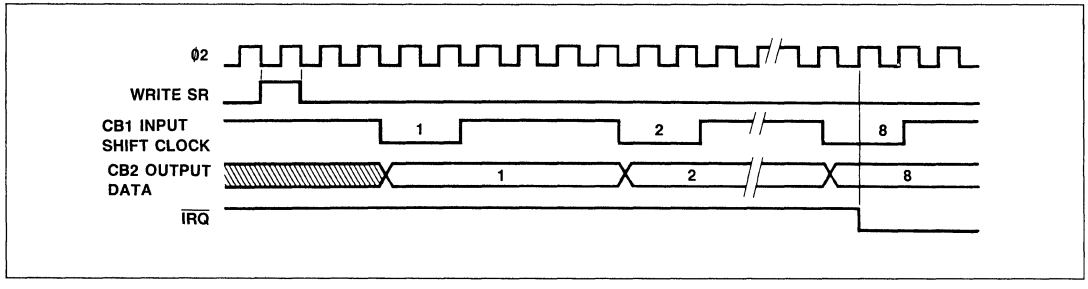


Figure 28. SR Mode 7 — Shift Out Under CB1 Control

INTERRUPT OPERATION

Controlling interrupts within the R6522 involves three principal operations. These are flagging the interrupts, enabling interrupts and signaling to the processor that an active interrupts exists within the chip. Interrupt flags are set in the Interrupt Flag Register (IFR) by conditions detected within the R6522 or on inputs to the R6522. These flags normally remain set until the interrupt has been serviced. To determine the source of an interrupt, the microprocessor must examine these flags in order, from highest to lowest priority.

Associated with each interrupt flag is an interrupt enable bit in the Interrupt Enable Register (IER). This can be set or cleared by the processor to enable interrupting the processor from the corresponding interrupt flag. If an interrupt flag is set to a logic 1 by an interrupting condition, and the corresponding interrupt enable bit is set to a 1, the Interrupt Request Output ($\overline{IRQ}$) will go low. $\overline{IRQ}$ is an "open-collector" output which can be "wire-OR'ed" with other devices in the system to interrupt the processor.

Interrupt Flag Register (IFR)

In the R6522, all the interrupt flags are contained in one register, i.e., the IFR (Figure 29). In addition, bit 7 of this register will be read as a logic 1 when an interrupt exists within the chip. This allows very convenient polling of several devices within a system to locate the source of an interrupt.

The Interrupt Flag Register (IFR) may be read directly by the processor. In addition, individual flag bits may be cleared by writing a "1" into the appropriate bit of the IFR. When the proper chip select and register signals are applied to the chip, the contents of this register are placed on the data bus. Bit 7 indicates the status of the $\overline{IRQ}$ output. This bit corresponds to the logic function: $\overline{IRQ}$ = IFR6 × IER6 + IFR5 × IER5 + IFR4 × IER4 + IFR3 × IER3 + IFR2 × IER2 + IFR1 × IER1 + IFR0 × IER0.

Note:

× = logic AND, + = Logic OR.

The IFR bit 7 is not a flag. Therefore, this bit is not directly cleared by writing a logic 1 into it. It can only be cleared by clearing all the flags in the register or by disabling all the active interrupts as discussed in the next section.

Interrupt Enable Register (IER)

For each interrupt flag in IFR, there is a corresponding bit in the Interrupt Enable Register (IER) (Figure 30). Individual bits in the IER can be set or cleared to facilitate controlling individual interrupts without affecting others. This is accomplished by writing to the (IER) after bit 7 set or cleared to, in turn, set or clear selected enable bits. If bit 7 of the data placed on the system data bus during this write operation is a 0, each 1 in bits 6 through 0 clears the corresponding bit in the Interrupt Enable Register. For each zero in bits 6 through 0, the corresponding bit is unaffected.

Selected bits in the IER can be set by writing to the IER with bit 7 in the data word set to a 1. In this case, each 1 in bits 6 through 0 will set the corresponding bit. For each zero, the corresponding bit will be unaffected. This individual control of the setting and clearing operations allows very convenient control of the interrupts during system operation.

In addition to setting and clearing IER bits, the contents of this register can be read at any time. Bit 7 will be read as a logic 1, however.

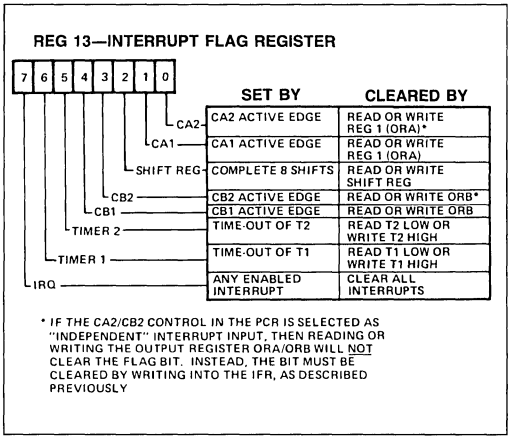


Figure 29. Interrupt Flag Register (IFR)

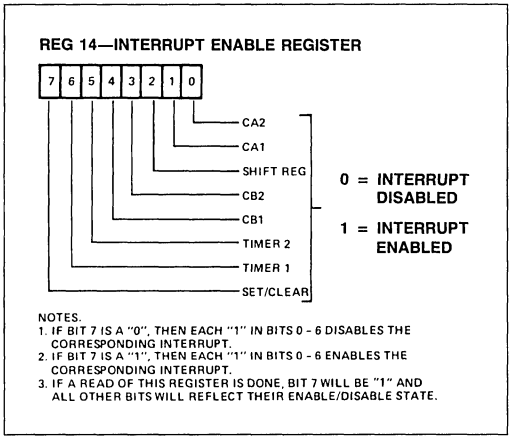


Figure 30. Interrupt Enable Register (IER)

PERIPHERAL INTERFACE CHARACTERISTICS

Symbol	Characteristic	Min.	Max.	Unit	Figure
t_r, t_f	Rise and Fall Time for CA1, CB1, CA2 and CB2 Input Signals	—	1.0	μs	—
t_{CA2}	Delay Time, Clock Negative Transition to CA2 Negative Transition (read handshake or pulse mode)	—	1.0	μs	31a, 31b
t_{RS1}	Delay Time, Clock Negative Transition to CA2 Positive Transition (pulse mode)	—	1.0	μs	31a
t_{RS2}	Delay Time, CA1 Active Transition to CA2 Positive Transition (handshake mode)	—	2.0	μs	31b
t_{WHS}	Delay Time, Clock Positive Transition to CA2 or CB2 Negative Transition (write handshake)	0.05	1.0	μs	31c, 31d
t_{DS}	Delay Time, Peripheral Data Valid to CB2 Negative Transition	0.20	1.5	μs	31c, 31d
t_{RS3}	Delay Time, Clock Positive Transition to CA2 or CB2 Positive Transition (pulse mode)	—	1.0	μs	31c
t_{RS4}	Delay Time, CA1 or CB1 Active Transition to CA2 or CB2 Positive Transition (handshake mode)	—	2.0	μs	31d
t_{21}	Delay Time Required from CA2 Output to CA1 Active Transition (handshake mode)	400	—	ns	31d
t_{IL}	Setup Time, Peripheral Data Valid to CA1 or CB1 Active Transition (input latching)	300	—	ns	31e
t_{AL}	CA1, CB1 Setup Prior to Transition to Arm Latch	300	—	ns	31e
t_{PDH}	Peripheral Data Hold After CA1, CB1 Transition	150	—	ns	31e
t_{SR1}	Shift-Out Delay Time — Time from ϕ_2 Falling Edge to CB2 Data Out	—	300	ns	31f
t_{SR2}	Shift-In Setup Time — Time from CB2 Data In to ϕ_2 Rising Edge	300	—	ns	31g
t_{SR3}	External Shift Clock (CB1) Setup Time Relative to ϕ_2 Trailing Edge	100	T_{CY}	ns	31g
t_{IPW}	Pulse Width — PB6 Input Pulse	2 × T_{CY}	—		31i
t_{ICW}	Pulse Width — CB1 Input Clock	2 × T_{CY}	—		31h
t_{IPS}	Pulse Spacing — PB6 Input Pulse	2 × T_{CY}	—		31i
t_{ICS}	Pulse Spacing — CB1 Input Pulse	2 × T_{CY}	—		31h

PERIPHERAL INTERFACE WAVEFORMS

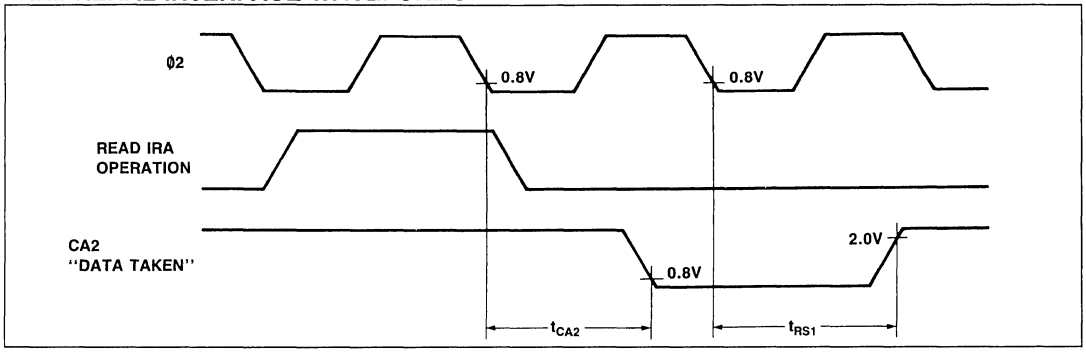


Figure 31a. CA2 Timing for Read Handshake, Pulse Mode

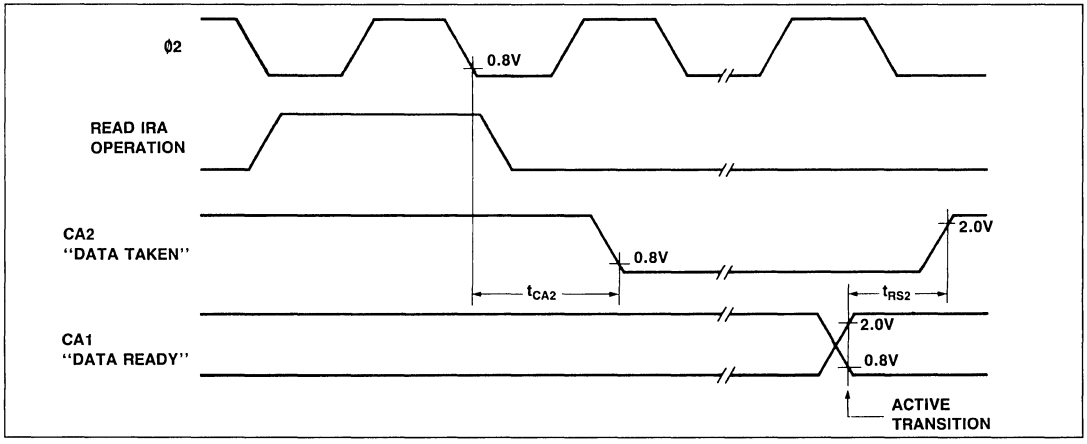


Figure 31b. CA2 Timing for Read Handshake, Handshake Mode

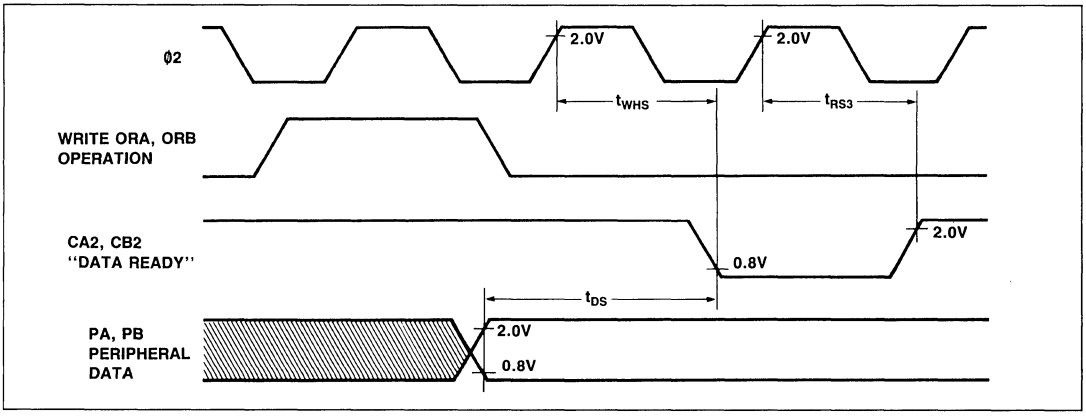


Figure 31c. CA2, CB2 Timing for Write Handshake, Pulse Mode

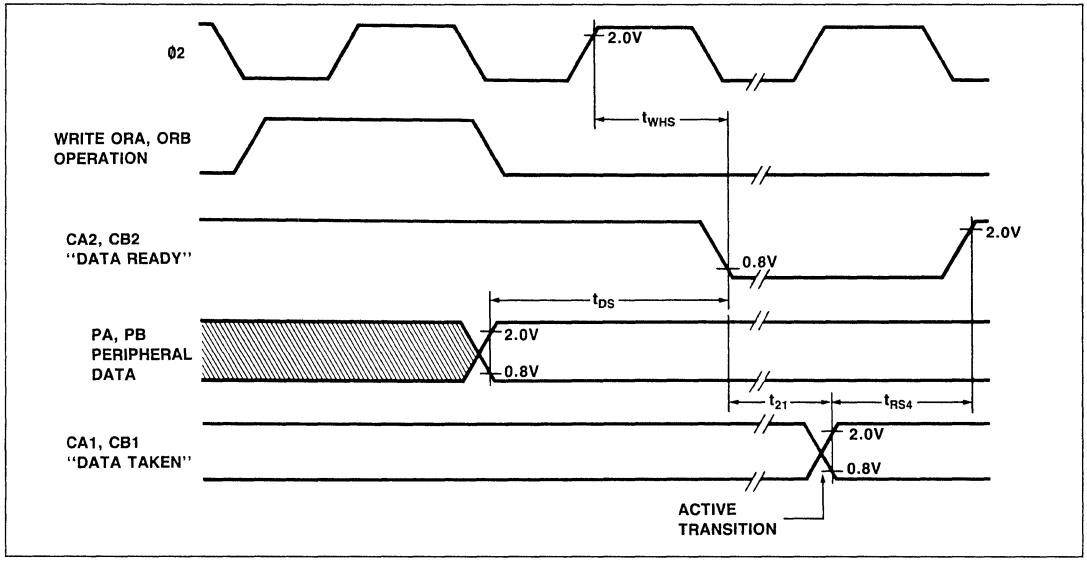


Figure 31d. CA2, CB2 Timing for Write Handshake, Handshake Mode

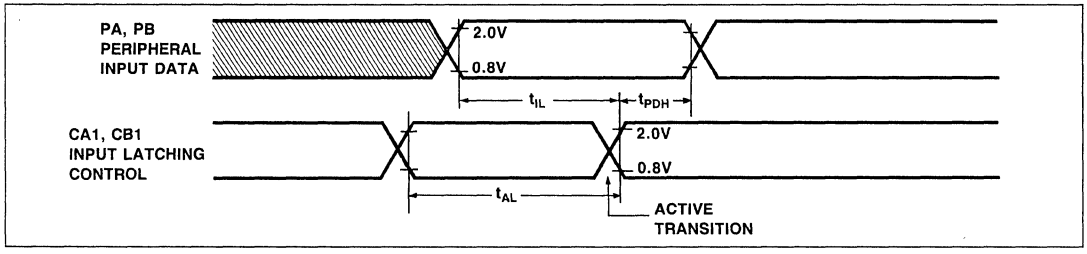


Figure 31e. Peripheral Data Input Latching Timing

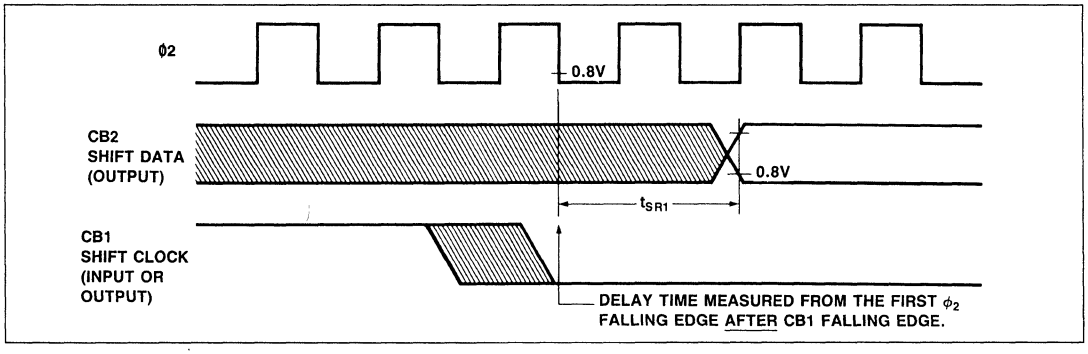


Figure 31f. Timing for Shift Out with Internal or External Shift Clocking

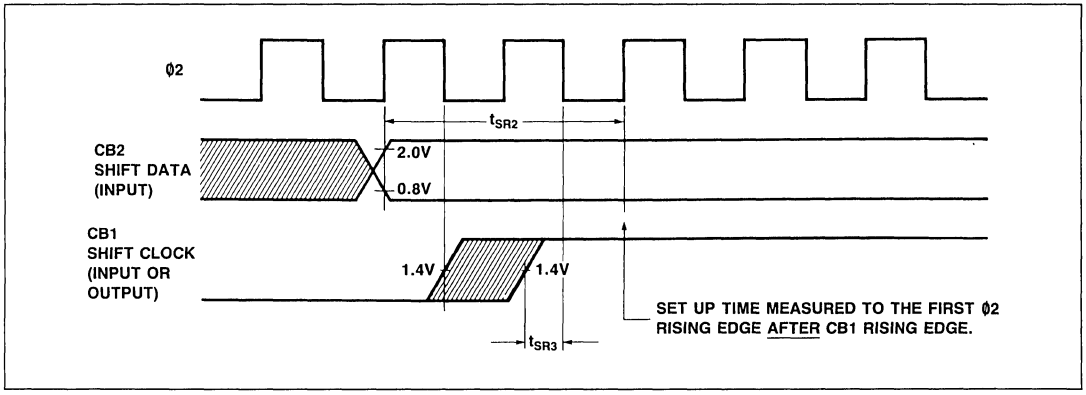


Figure 31g. Timing for Shift in with Internal or External Shift Clocking

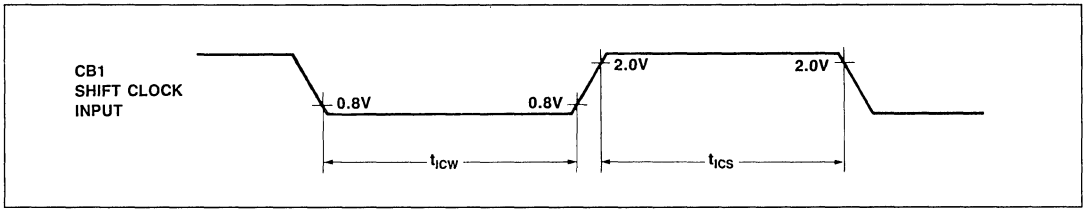


Figure 31h. External Shift Clock Timing

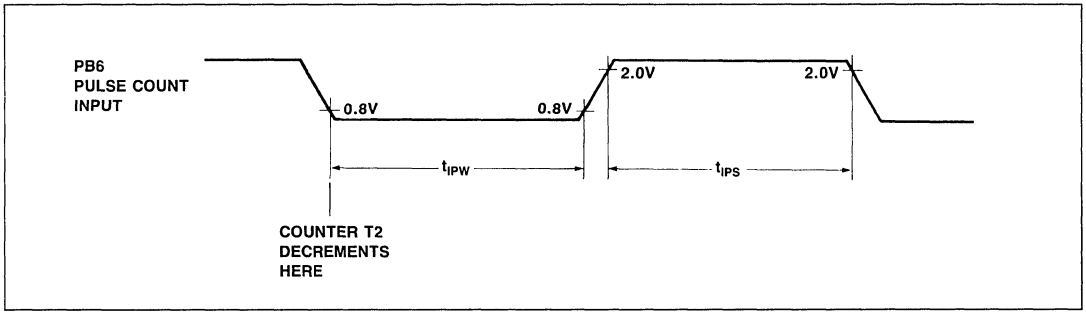
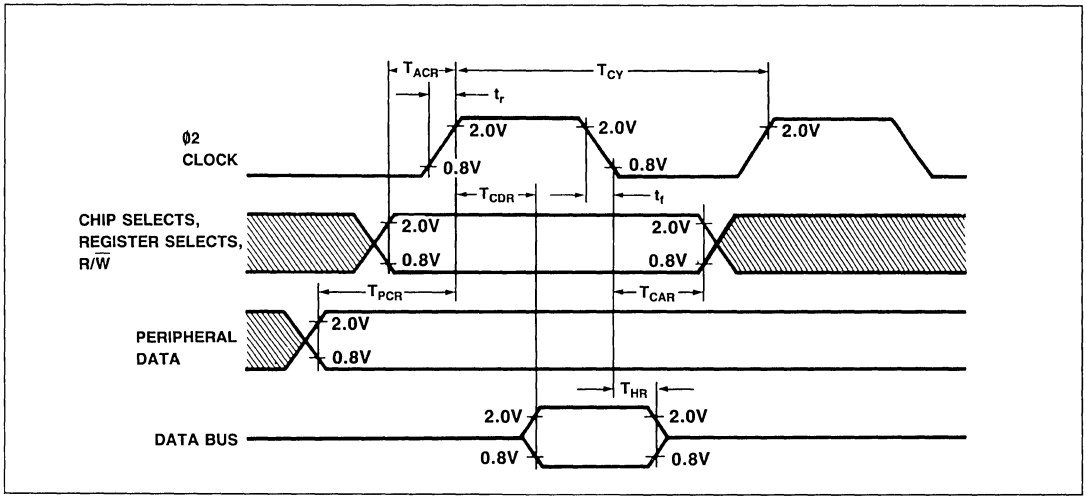


Figure 31i. Pulse Count Input Timing

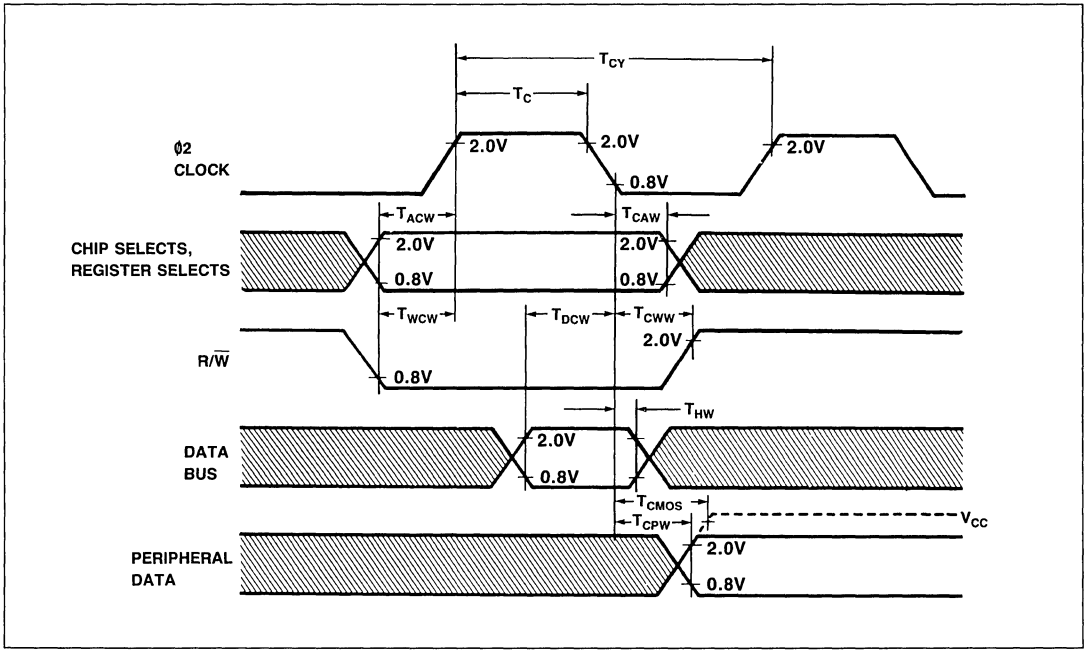
BUS TIMING CHARACTERISTICS

Parameter	Symbol	R6522 (1 MHz)		R6522A (2 MHz)		Unit
		Min.	Max.	Min.	Max.	
READ TIMING						
Cycle Time	T_{CY}	1	10	0.5	10	μs
Address Set-Up Time	T_{ACR}	180	—	90	—	ns
Address Hold Time	T_{CAR}	0	—	0	—	ns
Peripheral Data Set-Up Time	T_{PCR}	300	—	150	—	ns
Data Bus Delay Time	T_{CDR}	—	365	—	190	ns
Data Bus Hold Time	T_{HR}	10	—	10	—	ns
WRITE TIMING						
Cycle Time	T_{CY}	1	10	0.50	10	μs
Ø2 Pulse Width	T_C	470	—	235	—	ns
Address Set-Up Time	T_{ACW}	180	—	90	—	ns
Address Hold Time	T_{CAW}	0	—	0	—	ns
R/$\overline{W}$ Set-Up Time	T_{WCW}	180	—	90	—	ns
R/$\overline{W}$ Hold Time	T_{CWW}	0	—	0	—	ns
Data Bus Set-Up Time	T_{DCW}	200	—	90	—	ns
Data Bus Hold Time	T_{HW}	10	—	10	—	ns
Peripheral Data Delay Time	T_{CPW}	—	1.0	—	0.5	μs
Peripheral Data Delay Time to CMOS Levels	T_{CMOS}	—	2.0	—	1.0	μs
Note: t_R and t_F = 10 to 30 ns.						

BUS TIMING WAVEFORMS



Read Timing Waveforms



ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to +7.0	Vdc
Input Voltage	V_{IN}	−0.3 to +7.0	Vdc
Operating Temperature Commercial Industrial	T_A	 0 to +70 −40 to +85	 °C °C
Storage Temperature	T_{STG}	−55 to +150	°C

***NOTE:** Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the other sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING CONDITIONS

Parameter	Symbol	Value
Supply Voltage	V_{CC}	5V ±5%
Temperature Range Commercial	T_A	 0°C to 70°C

DC CHARACTERISTICS

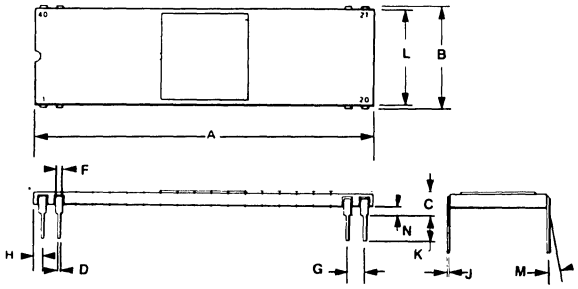
(V_{CC} = 5.0 Vdc ±5%, V_{SS} = 0, T_A = T_L to T_H, unless otherwise noted)

Parameter	Symbol	Min.	Typ.[3]	Max.	Unit	Test Conditions
Input High Voltage	V_{IH}	2.4	—	V_{CC}	V	
Input Low Voltage	V_{IL}	−0.3	—	0.4	V	
Input Leakage Current R/$\overline{W}$, $\overline{RES}$, RS0, RS1, RS2, RS3, CS1, $\overline{CS2}$, CA1, ϕ2	I_{IN}	—	±1	±2.5	μA	V_{IN} = 0V to 5.25V V_{CC} = 0V
Input Leakage Current for Three-State Off D0-D07	I_{TSI}	—	±2	±10	μA	V_{IN} = 0.4V to 2.4V V_{CC} = 5.25V
Input High Current PA0-PA7, CA2, PB0-PB7, CB1, CBS	I_{IH}	−100	−200	—	μA	V_{IN} = 2.4V V_{CC} = 5.25V
Input Low Current PA0-PA7, CA2, PB0-PB7, CB1, CB2	I_{IL}	—	−0.9	−1.8	mA	V_{IL} = 0.4V V_{CC} = 5.25V
Output High Voltage All outputs PB0-PB7, CB2 (Darlington Drive)	V_{OH}	 2.4 1.5	 — —	 — —	 V V	V_{CC} = 4.75V I_{LOAD} = −100 μA I_{LOAD} = −1.0 mA
Output Low Voltage	V_{OL}	—	—	0.4	V	V_{CC} = 4.75V I_{LOAD} = 1.6 mA
Output High Current (Sourcing) Logic PB0-PB7, CB2 (Darlington Drive)	I_{OH}	 −100 −1.0	 −1000 −2.5	 — −10	 μA mA	 V_{OH} = 2.4V V_{OH} = 1.5V
Output Low Current (Sinking)	I_{OL}	1.6	—	—	mA	V_{OL} = 0.4V
Output Leakage Current (Off State) $\overline{IRQ}$	I_{OFF}	—	4	±10	μA	V_{OH} = 2.4V V_{CC} = 5.25V
Power Dissipation	P_D	—	450	700	mW	
Input Capacitance R/$\overline{W}$, $\overline{RES}$, RS0, RS1, RS2, RS3, CS1, $\overline{CS2}$, D0-D7, PA0-PA7, CA1, CA2, PB0-PB7 CB1, CB2 ϕ2 Input	C_{IN}	 — — —	 — — —	 7 10 20	 pF pF pF	V_{CC} = 5.0V V_{IN} = 0V f = 1 MHz T_A = 25°C
Output Capacitance	C_{OUT}	—	—	10	pF	

Notes:
1. All units are direct current (DC) except for capacitance.
2. Negative sign indicates outward current flow, positive indicates inward flow.
3. Typical values shown for V_{CC} = 5.0V and T_A = 25°C.

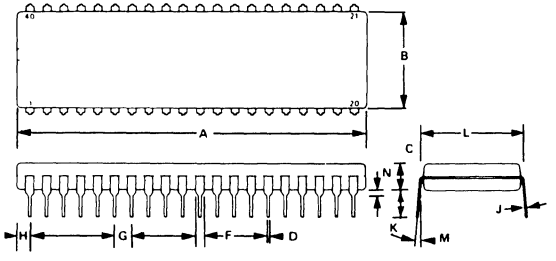
PACKAGE DIMENSIONS

40-PIN CERAMIC DIP



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	50 29	51 31	1.980	2 020
B	14 86	15 62	0.585	0 615
C	2 54	4 19	0 100	0 165
D	0.38	0 53	0 015	0.021
F	0.76	1 40	0 030	0 055
G	2.54 BSC		0.100 BSC	
H	0 76	1 78	0 030	0 070
J	0.20	0.33	0.008	0.013
K	2.54	4.19	0.100	0.165
L	14 60	15.37	0.575	0 605
M	0°	10°	0°	10°
N	0 51	1 52	0 020	0 060

40-PIN PLASTIC DIP



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	51 28	52.32	2 040	2 060
B	13 72	14 22	0 540	0 560
C	3.55	5 08	0 140	0 200
D	0.36	0 51	0 014	0.020
F	1 02	1 52	0.040	0 060
G	2 54 BSC		0.100 BSC	
H	1 65	2 16	0.065	0 085
J	0 20	0 30	0 008	0 012
K	3 05	3 56	0 120	0 140
L	15.24 BSC		0 600 BSC	
M	7°	10°	7°	10°
N	0.51	1 02	0.020	0 040

Rockwell

R6532
RAM-I/O-Timer (RIOT)

DESCRIPTION

The R6532 RAM-I/O-Timer (RIOT) integrates random access memory (RAM), parallel I/O data ports and timer functions into a single peripheral device which operates in conjunction with any CPU in the R6500 microprocessor family. It is comprised of a 128 × 8 static RAM, two software-controlled, 8-bit bidirectional data ports allowing direct interfacing between the microcomputer and peripheral devices, a software programmable interval timer, with interrupt, capable of timing in various intervals from 1 to 262,144 clock periods, and a programmable edge-detect circuit.

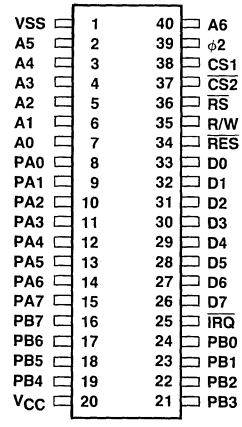
FEATURES

- 128 × 8 static RAM
- Two 8 bit bidirectional data ports
- Programmable interval timer with interrupt capability
- TTL & CMOS compatible peripheral lines
- One port has direct transistor drive capability
- Programmable edge-sensitive interrupt input
- 8 bit bidirectional data bus
- 6500/6800 bus compatible
- 1 MHz and 2 MHz parts available
- Single +5V power supply

ORDERING INFORMATION

Part Number: R6532 _ _ _

- Temperature Range:
  - Blank = 0°C to +70°C
  - E = −40°C to +85°C
- Package:
  - C = Ceramic DIP
  - P = Plastic DIP
- Frequency:
  - No Letter = 1 MHz
  - A = 2 MHz



R6532 Pin Configuration

INTERFACE SIGNALS

RESET ($\overline{RES}$)

During system initialization, a low $\overline{RES}$ input causes a zeroing of all four I/O registers. This in turn causes all I/O buses to act as inputs thus protecting external components from possible damage and erroneous data while the system is being configured under software control. The Data Bus Buffers are put into an OFF-STATE during Reset. Interrupt capability is disabled with the $\overline{RES}$ signal. The $\overline{RES}$ signal must be held low for at least two clock periods when reset is required.

READ/WRITE (R/$\overline{W}$)

The R/$\overline{W}$ signal is supplied by the microprocessor and controls the transfer of data to and from the R6532. A high on the R/$\overline{W}$ pin allows the processor to read (with proper addressing) the data supplied by the R6532. A low on the R/$\overline{W}$ pin allows a write (with proper addressing) to the R6532.

INTERRUPT REQUEST ($\overline{IRQ}$)

The $\overline{IRQ}$ pin is an interrupt pin from the interrupt control logic. The pin will be normally high with a low indicating an interrupt from the R6532. An external 3K pull-up resistor is required. The $\overline{IRQ}$ pin may be activated by a transition on PA7 or timeout of the interval timer.

DATA BUS (D0–D7)

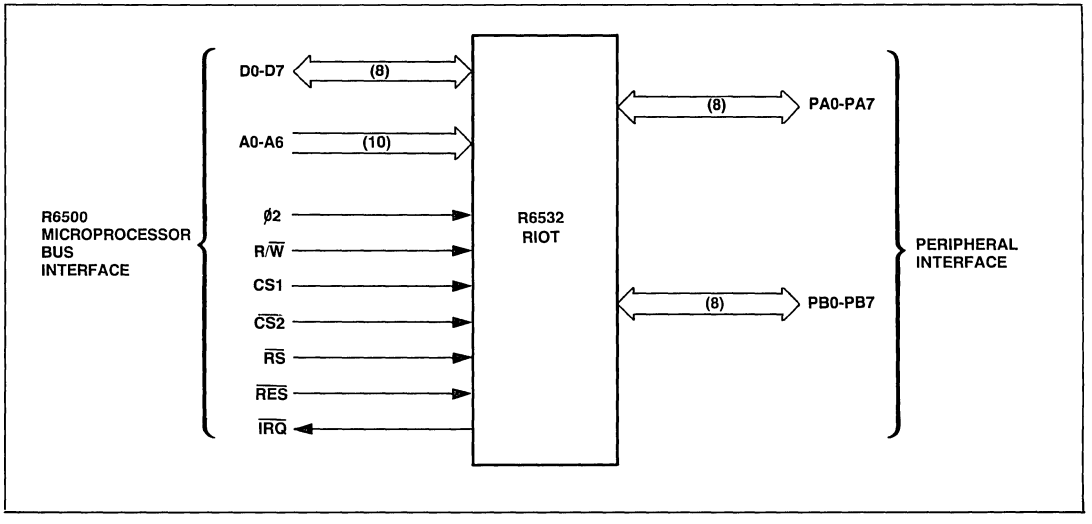
The R6532 has eight bidirectional data pins (D0–D7). These pins connect to the system's data lines and transfer data between the R6532 and the microprocessor data bus. The output buffers remain off, or tri-stated, except when the R6532 is selected for a Read operation.

ADDRESS LINES (A0–A6)

There are seven address pins (A0–A6). In addition, there is the $\overline{RAM\ SELECT}$ ($\overline{RS}$) pin. The pins A0–A6 and $\overline{RS}$ are always used as addressing pins. There are two additional pins which are used as CHIP SELECTS. They are pins CS1 and $\overline{CS2}$. Tables 1 and 2 identify the functions selected and registers addressed depending upon the address line and $\overline{RS}$ inputs in conjunction with the R/$\overline{W}$ level.

I/O PORTS (PA0–PA7, PB0–PB7)

The R6532 has 16 pins available for peripheral I/O operations. Each pin is individually software programmable to act as either an input or an output. The 16 pins are divided into two 8-bit ports, PA0–PA7 and PB0–PB7. (PA7 also has another use which is discussed later.) Each is set up as an input by writing a "0" into the corresponding bit of the data direction register. A "1" written into the data direction register causes its corresponding bit to be an output. When in the input mode, the peripheral output buffers are in the "1" state and the internal pull-up device acts as less than one TTL load to the peripheral data lines. On a Read operation, the microprocessor reads the peripheral pin. When the peripheral device gets information from the R6532 it receives data stored in the data register. The microprocessor reads valid pin information if the peripheral lines are greater than 2.0 volts for a "1" and less than 0.8 volt for a "0" as the peripheral pins are all TTL compatible. Pins PB0–PB7 are also capable of sourcing 3 ma at 1.5V, thus making them capable of Darlington drive.



RIOT Interface Signals

Table 1. Address Decoding

Operation	$\overline{RS}$	R/$\overline{W}$	A4	A3	A2	A1	A0
Write RAM	0	0	—	—	—	—	—
Read RAM	0	1	—	—	—	—	—
Write Output Reg A	1	0	—	—	0	0	0
Read Output Reg A	1	1	—	—	0	0	0
Write DDRA	1	0	—	—	0	0	1
Read DDRA	1	1	—	—	0	0	1
Write Output Reg B	1	0	—	—	0	1	0
Read Output Reg B	1	1	—	—	0	1	0
Write DDRB	1	0	—	—	0	1	1
Read DDRB	1	1	—	—	0	1	1
Write Timer							
÷1T	1	0	1	(a)	1	0	0
÷8T	1	0	1	(a)	1	0	1
÷64T	1	0	1	(a)	1	1	0
÷1024T	1	0	1	(a)	1	1	1
Read Timer	1	1	—	(a)	1	—	0
Read Interrupt Flag	1	1	—	—	1	—	1
Write Edge Detect Control	1	0	0	—	1	(b)	(c)

Notes:
— = Don't Care, "1" = High level (≥2.4V), "0" = Low level (≤0.4V)

(a) A3 = 0 to disable timer interrupt
A3 = 1 to enable timer interrupt

(b) A1 = 0 to disable PA7 interrupt
A1 = 1 to enable PA7 interrupt

(c) A0 = 0 for negative edge-detect
A0 = 1 for positive edge-detect

Table 2. Register Addressing

Start Address +	Register/Function	Start Address +	Register/Function
$0	DRA ('A' side data register)	$7	Write edge-detect control (positive edge-detece, enable interrupt)
$1	DDRA ('A' side data direction register)		
$2	DRB ('B' side data register)	$C	Read timer (enable interrupt)
$3	DDRB ('B' side data direction register)	$14	Write timer (divide by 1, disable interrupt)
$4	Read timer (disable interrupt)	$15	Write timer (divide by 8, disable interrupt)
$4	Write edge-detect control (negative edge-detect, disable interrupt)	$16	Write timer (divide by 64, disable interrupt)
		$17	Write timer (divide by 1024, disable interrupt)
$5	Read interrupt flag register (bit 7 = timer, bit 6 = PA7 edge-detect) Clear PA7 flag	$1C	Write timer (divide by 1, enable interrupt)
		$1D	Write timer (divide by 8, enable interrupt)
$5	Write edge-detect control (positive edge-detect, disable interrupt)	$1E	Write timer (divide by 64, enable interrupt)
		$1F	Write timer (divide by 1024, enable interrupt)
$6	Write edge-detect control (negative edge-detect, enable interrupt)		

INTERNAL ORGANIZATION

The R6532 is divided into four basic sections, RAM, I/O, Timer, and Interrupt Control. The RAM interfaces directly with the microprocessor through the system data bus and address lines. The I/O section consists of two 8-bit halves. Each half contains a Data Direction Register (DDR) and a Data Register (DR).

RAM—128 BYTES (1024 BITS)

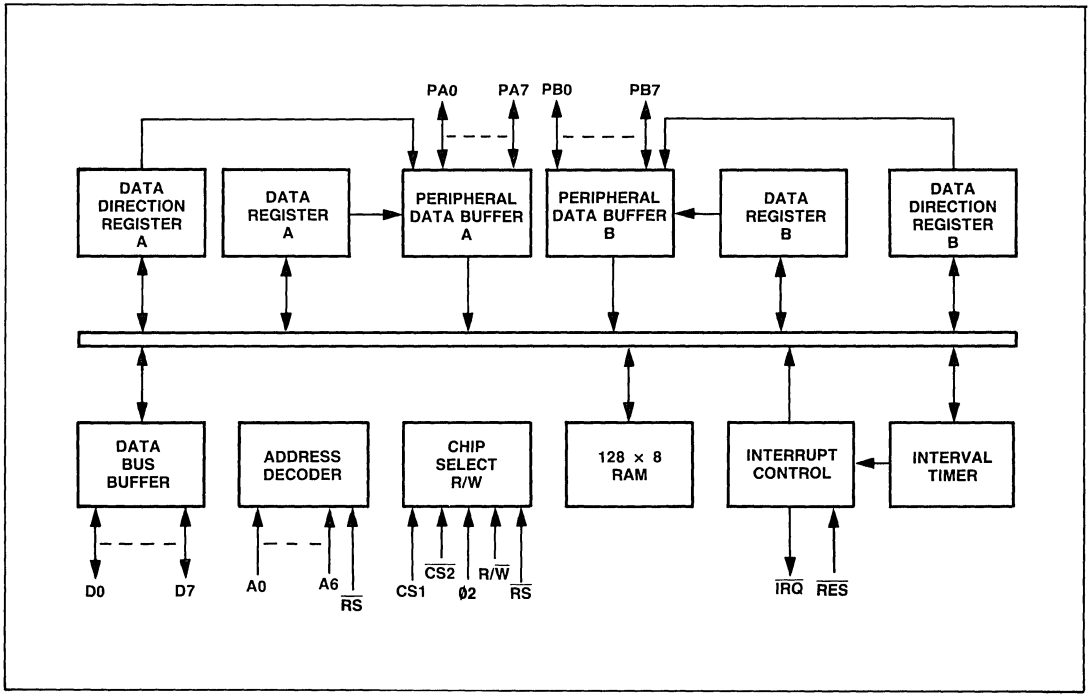
The 128 × 8 Read/Write Memory acts as a conventional static RAM and can be accessed from the microprocessor by selecting the chip (CS1 = high, $\overline{CS2}$ = low) and by setting $\overline{RS}$ low. Address lines A0 through A6 then select the desired byte of storage.

I/O PORTS AND REGISTERS

The I/O Ports consist of eight lines which can be individually programmed to act as either an input or an output. A logic zero in a bit of the Port A Data Direction Register (DDRA) causes the corresponding line of Port A to act as an input. A logic one causes the corresponding Port A line to act as an output. The voltage on any line programmed to be an output is determined by the corresponding bit in the Port A Data Register (DRA). Data is read directly from the data pins during any read operation. For any output pin, the data transferred into the processor will be the same as that contained in the Data Register if the voltage on the pin is allowed to go to 2.4V for a logic one. Note that for input lines, the processor can write into the corresponding bit of the Data Register. This will not affect the polarity on the pin until the corresponding bit of DDRA is set to a logic one to allow the I/O line to act as an output.

The operation of the Port B is exactly the same as the normal I/O operation of the Port A. Each of the eight lines can each be programmed to act as either an input or as an output by placing a 0 or a 1 into the Port B Data Direction register (DDRB). In the output mode, the voltage on a peripheral pin is controlled by the Port B Data Register (DRB).

The primary difference between Port A and the Port B is in the operation of the output buffers which drive these pins. The Port B output buffers are push-pull devices which are capable of sourcing 3 ma at 1.5V. This allows these pins to directly drive transistor switches. To assure that the microprocessor will read proper data on a "Read Port B" operation, logic in the R6532 allows the microprocessor to read the Output Register instead of reading the peripheral pin as on Port A.



R6532 Block Diagram

EDGE DETECTING WITH PA7

In addition to acting as a peripheral I/O line, the PA7 line can be used as an edge-detecting input. In this mode, an active transition sets the internal interrupt flag (bit 6 of the Interrupt Flag register). Setting the interrupt flag causes $\overline{IRQ}$ output to go low if the PA7 interrupt has been enabled.

Control of the PA7 edge detecting mode is accomplished by writing to one of four addresses. In this operation, A0 controls the polarity of the active transition and A1 acts to enable or disable interrupting of the processor. The data which is placed on the Data Bus during this operation is discarded and has no effect on the control of PA7.

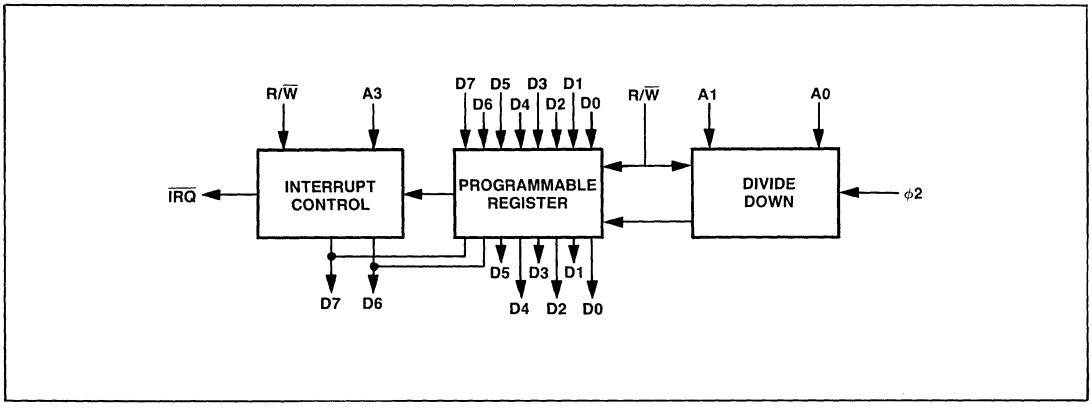
The PA7 interrupt flag is set on an active transition, even if the pin is being used as a normal input or as a peripheral control output. The flag is also set by an active transition if the PA7 interrupt is disabled. The reset signal ($\overline{RES}$) disables the PA7 interrupt and enables negative (high-to-low) edge detection on PA7. The PA7 edge detect logic can be set to detect either a positive or negative transition and to either enable or disable interrupt ($\overline{IRQ}$) generation upon detection.

During system initialization, the interrupt flag may inadvertently be set by an unexpected transition on the PA7. It is therefore recommended that the interrupt flag be cleared *before* enabling interrupting from PA7. To clear PA7 interrupt flag, simply read the interrupt Flag Register.

INTERVAL TIMER

The Timer section of the R6532 contains three basic parts: preliminary divide down register, programmable 8-bit register and interrupt logic.

The Timer can be programmed to count up to 255 time intervals. Each time interval can be either 1T, 8T, 64T or 1024T increments, where T is the system clock period. When a full count is reached, an interrupt flag is set to logic "1". After the interrupt flag is set the internal clock begins counting down at the system clock rate to a maximum of −255T. Thus, after the interrupt flag is set, a Read of the timer will tell how long since the flag was set up to a maximum of 255T.



Basic Elements of Interval Timer

INTERVAL TIMER EXAMPLE

The 8-bit microprocessor data bus transfers data to and from the Timer. If a count of 52 time intervals were to be counted, the pattern 0 0 1 1 0 1 0 0 would be put on the data bus and written into the divide by 1 Timer register.

At the same time that data is being written to the Timer, the counting intervals of 1, 8,64, 1024T are decoded from address lines A0 and A1. During a Read or Write Operation address line A3 controls the interrupt enable, i.e., A3 = 1 enables $\overline{IRQ}$, A3 = 0 disables $\overline{IRQ}$. When the time is read prior to the interrupt flag being set, the number of time intervals remaining will be read, i.e., 51, 50, 49, etc.

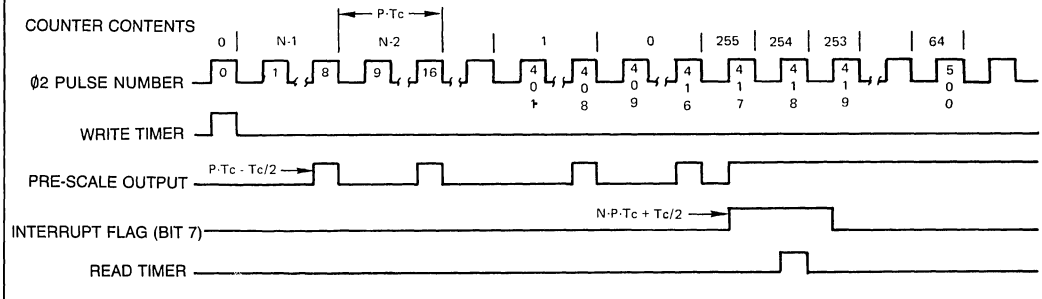
When the Timer has counted through 0 0 0 0 0 0 0 0 on the next count time an interrupt will occur and the counter will read 1 1 1 1 1 1 1 1. After the interrupt flag is set, the timer register decrements at a divide by "1" rate of the system clock. If the timer is read after the interrupt flag is set and a value of 1 1 1 0 0 1 0 0 is read, the time since interrupt is 27T. The value read is in two's complement, but remember that interrupt occurred on count number one. Therefore, we must subtract 1.

Value read = 1 1 1 0 0 1 0 0
Complement = 0 0 0 1 1 0 1 1
ADD 1 = 0 0 0 1 1 1 0 0 = 28 Equals two's complement of register
SUB 1 = 0 0 0 1 1 0 1 1 = 27

Thus, to arrive at the *total* elapsed time, merely do a two's complement add to the original time written into the timer. Again, assume time written as 0 0 1 1 0 1 0 0 (=52). With a divide by 8, total time to interrupt is (52 × 8) + 1 = 417T. Total elapsed time would be 416T + 27T = 443T, assuming the value read after interrupt was 1 1 1 0 0 1 0 0.

The interrupt flag will be reset whenever the Timer is accessed by a read or a write. However, the reading of the timer at the same time the interrupt occurs will not reset the interrupt flag. When the interrupt flags are read (D7 for the timer, D6 for the edge detect) data bus lines D0–D5 go to 0.

When reading the timer after an interrupt, A3 should be low so as to disable the $\overline{IRQ}$ pin. This is done so as to avoid future interrupts until after another Write timer operation.

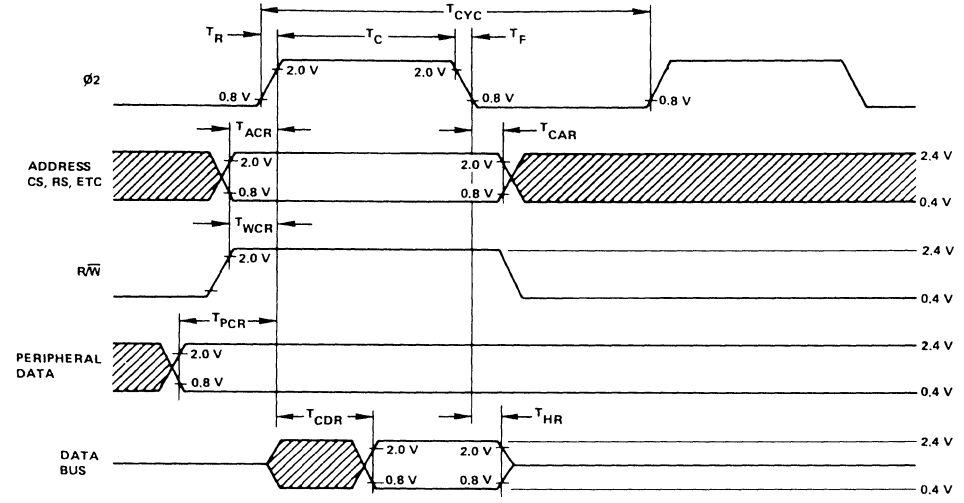


Notes:
Assume 52 Loaded into Timer with a divide by 8.
The Counter Contents and the Clock Pulse Numbers will coincide.
Prescale, P = 8.
Cycle Time, T_C = 1 μsec (for 1 MHz)
Count, N = 52

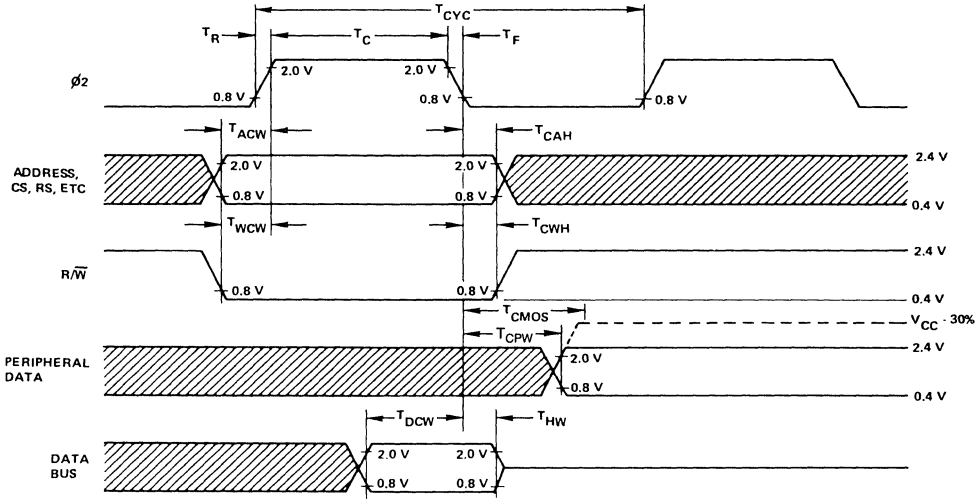
Interval Time Example Waveforms

BUS AND PERIPHERAL TIMING WAVEFORMS

READ TIMING



WRITE TIMING



AC CHARACTERISTICS

Characteristic	Symbol	R6532 (1 MHz) Min	R6532 (1 MHz) Max	R6532A (2 MHz) Min	R6532A (2 MHz) Max	Unit
Clock Cycle Time	T_{CYC}	1	10	0.5	10	μs
Clock Pulse Width	T_C	470	—	240	—	ns
Rise & Fall Times	T_R, T_F	—	25	—	15	ns

READ TIMING

Address Set Up Time	T_{ACR}	180	—	90	—	ns
Address Hold Time	T_{CAR}	0	—	0	—	ns
R/$\overline{W}$ Set Up Time	T_{WCR}	180	—	90	—	ns
Data Bus Delay Time	T_{CDR}	—	395	—	190	n
Data Bus Hold Time	T_{HR}	10	—	10	—	ns
Peripheral Data Set Up Time	T_{PCR}	300	—	150	—	ns

WRITE TIMING

Ø2 Cycle Time	T_{CYC}	1	10	0.5	10	μs
Ø2 Pulse Width	T_C	470	—	240	—	ns
Address Set Up Time	T_{ACW}	180	—	90	—	ns
Address Hold Time	T_{CAH}	0	—	0	—	ns
R/$\overline{W}$ Set Up Time	T_{WCW}	180	—	90	—	ns
R/$\overline{W}$ Hold Time	T_{CWH}	0	—	0	—	ns
Data Bus Set-Up Time	T_{DCW}	300	—	150	—	ns
Data Bus Hold Time	T_{HW}	10	—	10	—	ns
Peripheral Data Delay Time	T_{CPW}	—	1	—	0.5	μs
Peripheral Data Delay Time CMOS	T_{CMOS}	—	2	—	1	μs

MAXIMUM RATINGS*

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to +7.0	Vdc
Input Voltage	V_{IN}	−0.3 to +7.0	Vdc
Operating Temperature Commercial Industrial	T_A	 0 to +70 −40 to +85	 °C °C
Storage Temperature	T_{STG}	−55 to +150	°C

***NOTE:** Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the other sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

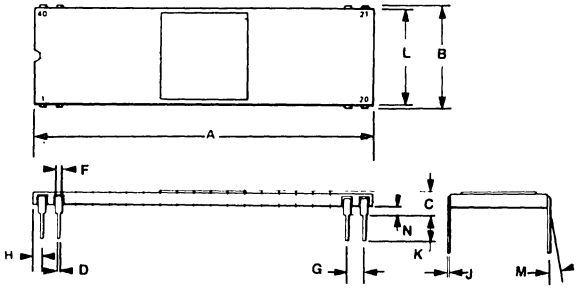
(V_{CC} = 5.0 ±5%, T_A = T_L to T_H unless otherwise noted)

Parameter	Symbol	Min	Max	Unit[1]	Test Conditions
Input High Voltage	V_{IH}	2.4	V_{CC}	V	
Input Low Voltage	V_{IL}	0	0.4	V	
Input Leakage Current: A0-A6, RS, R/$\overline{W}$, $\overline{RES}$, ø2, CS1,$\overline{CS2}$	I_{IN}	—	2.5	µA	V_{IN} = 5.25V V_{CC} = 0V
Input Leakage Current for Three-State Off D0-D7	I_{TSI}	—	±10	µA	V_{IN} = 0.4V to 2.4V
Input High Current PA0-PA7, PB0-PB7	I_{IH}	−100	—	µA	V_{IH} = 2.4V
Input Low Current PA0-PA7, PB0-PB7	I_{IL}	—	−1.6	mA	V_{IN} = 0.4V
Output High Voltage PA0-PA7, PB0-PB7 (TTL drive), D0-D7 PB0-PB7 (other than TTL drive, e.g., Darlington)	V_{OH}	 2.4 1.5	 — —	V	V_{CC} = 4.75V I_{LOAD} = −100 µA I_{LOAD} = 3 mA
Output Low Voltage D0-D7	V_{OL}	 —	 0.4	V	V_{CC} = 4.75V I_{LOAD} = 1.6 mA
Output High Current (Sourcing) PA0-PA7, PB0-PB7 (TTL drive), D0-D7 PB0-PB7 (other drive, e.g., Darlington)	I_{OH}	 −100 −3.0	 —	 µA mA	 V_{OH} = 2.4V V_{OH} = 1.5V
Output Low Current (Sinking) PA0-PA7, PB0-PB7	I_{OL}	1.6	—	mA	V_{OL} = 0.4V
Input Capacitance ø2 Other	 C_{CLK} C_{IN}	 — —	 30 10	 pF pF	V_{CC} = 5.0V V_{IN} = 0V f = 1 MHz T_A = 25°C
Output Capacitance	C_{OUT}	—	10	pF	
Power Dissipation	P_D	—	1000	mW	T_A = 0°C

Notes:
1. All units are direct current (DC).
2. Negative sign indicates outward current flow, positive indicates inward flow.

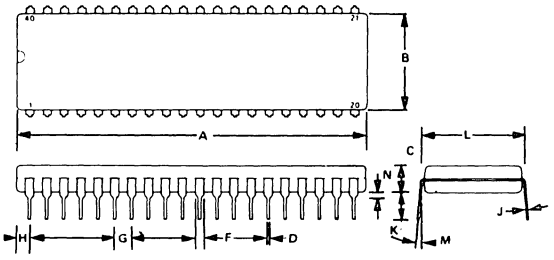
PACKAGE DIMENSIONS

40-PIN CERAMIC DIP



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	50.29	51.31	1 980	2.020
B	14.86	15 62	0.585	0.615
C	2.54	4.19	0 100	0.165
D	0 38	0.53	0.015	0.021
F	0.76	1.40	0.030	0.055
G	2 54 BSC		0 100 BSC	
H	0.76	1.78	0.030	0 070
J	0.20	0.33	0 008	0.013
K	2.54	4.19	0.100	0.165
L	14.60	15.37	0.575	0 605
M	0°	10°	0°	10°
N	0 51	1.52	0.020	0 060

40-PIN PLASTIC DIP



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	51.28	52.32	2.040	2.060
B	13.72	14 22	0.540	0.560
C	3.55	5 08	0.140	0.200
D	0.36	0.51	0.014	0 020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1 65	2.16	0 065	0.085
J	0.20	0 30	0 008	0.012
K	3 05	3.56	0.120	0.140
L	15.24 BSC		0 600 BSC	
M	7°	10°	7°	10°
N	0 51	1 02	0 020	0 040

Rockwell

R6545/R6545E
CRT Controller (CRTC)

DESCRIPTION

The R6545/R6545E CRT Controller (CRTC) interfaces an 8-bit microprocessor to CRT raster scan video displays, and adds an advanced CRT controller to the established and expanding line of R6500, R6500/* and R65C00 microprocessor, microcomputer and peripheral device products.

The R6545 and R6545E devices differ only in the character clock frequency (CCLK) specifications. The maximum CCLK frequency is 2.5 MHz for the R6545 and 3.7 MHz for the R6545E. Throughout this document, the nomenclature R6545 applies to both devices, unless specified otherwise.

The R6545 provides refresh memory addresses and character generator row addresses which allow up to 16K characters with 32 scan lines per character to be addressed. A major advantage of the R6545 is that the refresh memory may be addressed in either straight binary or by row/column.

Other functions in the R6545 include an internal cursor register which generates a cursor output when its contents are equal to the current refresh address. Programmable cursor start and end registers allow a cursor of up to the full character scan in height to be placed on any scan lines of the character. Variable cursor display blink rates are provided. A light pen strobe input allows capture of the current refresh address in an internal light pen register. The refresh address lines are configured to provide direct dynamic memory refresh.

All timing for the video refresh memory signals is derived from the character clock input (CCLK). Shift register, latch, and multiplex control signals (when needed) are provided by external high-speed timing. The mode control register allows noninterlaced video display modes at 50 or 60 Hz refresh rate. The internal status register may be used to monitor the R6545 operation. The $\overline{RES}$ input allows the CRTC-generated field rate to be dynamically-synchronized with line frequency jitter.

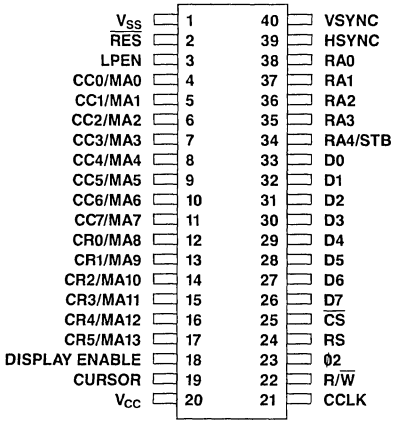
FEATURES

- Compatible with 8-bit microprocessors
- 3.7 MHz character clock operation (R6545E)
- 2.5 MHz character clock operation (R6545)
- Refresh RAM may be configured in row/column or straight binary addressing
- Alphanumeric and limited graphics capability
- Up and down scrolling by page, line, or character
- Programmable vertical sync width
- Fully programmable display (rows, columns, character matrix)
- Video display RAM may be configured as part of microprocessor memory field or independently slaved to R6545 (Transparent Addressing)
- Interlaced or non-interlaced scan
- 50/60 Hz refresh rate
- Fully programmable cursor
- Light pen register
- Addresses refresh RAM to 16K characters
- No external DMA required
- Internal status register
- 40-pin ceramic or plastic DIP
- Pin-compatible with MC6845R
- Single +5 ±5% Vdc power supply

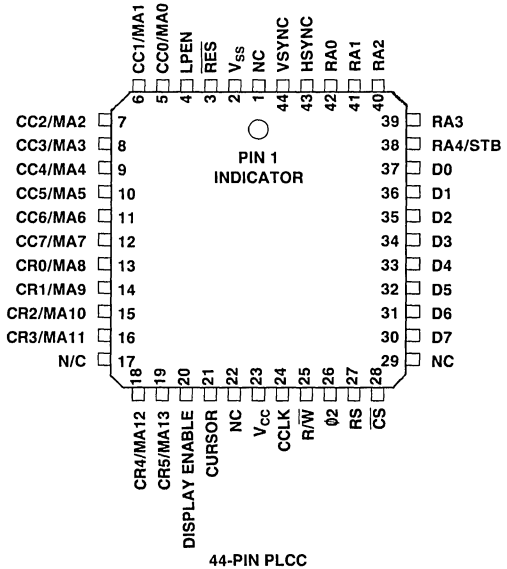
ORDERING INFORMATION

Part Number:
R6545 _ _ _ _

- Operating Temperature (T_L to T_H)
  - No Letters = 0°C to 70°C
  - E = −40°C to 85°C
- Package
  - P = 40-Pin Plastic DIP
  - C = 40-Pin Ceramic DIP
  - J = 44-Pin Plastic Leaded Chip Carrier (PLCC)
- Operating Frequency (Bus)
  - No Letter = 1 MHz
  - A = 2 MHz
- Character Clock Frequency (CCLK)
  - No Letter = 2.5 MHz
  - E = 3.7 MHz



40-PIN DIP



44-PIN PLCC

R6545/R6545E Pin Configuration

INTERFACE SIGNAL DESCRIPTION

Figure 1 illustrates the interface between the CPU, the R6545, and the video circuitry. Figure 2 shows typical timing waveforms at the video interface.

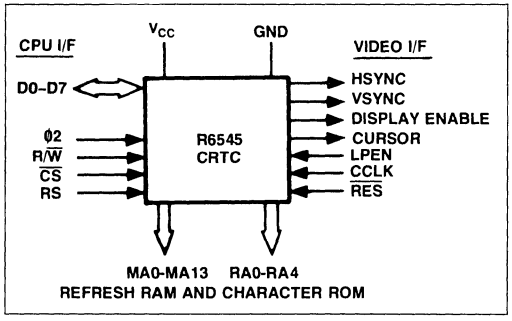


Figure 1. R6545 Interface Diagram

CPU INTERFACE

Ø2 (Phase 2 Clock)

The Phase 2 (Ø2) input clock triggers all data transfers between the system processor (CPU) and the R6545. Since there is no maximum limit to the allowable Ø2 clock time, it is not necessary for it to be a continuous clock. This capability permits the R6545 to be easily interfaced to non-6500 compatible microprocessors.

R/$\overline{W}$ (Read/Write)

The R/$\overline{W}$ input signal generated by the processor controls the direction of data transfers. A high on the R/$\overline{W}$ pin allows the processor to read the data supplied by the R6545, a low on the R/$\overline{W}$ pin allows data on data lines D0–D7 to be written into the R6545.

$\overline{CS}$ (Chip Select)

The Chip Select input is normally connected to the processor address bus either directly or through a decoder. The R6545 is selected when CS is low. Then, data may be written to, or read from, the R6545 depending on the state of RS and R/$\overline{W}$.

RS (Register Select)

The Register Select input allows access to internal registers. A low on this pin permits writing (R/$\overline{W}$ = low) into the Address Register and reading (R/$\overline{W}$ = high) from the Status Register. The Address Register selects the register accessed when RS is high.

D0–D7 (Data Bus)

The eight data lines (D0–D7) transfer data between the processor and the R6545. These lines are bidirectional and are normally high-impedance except during read cycles when the chip is selected ($\overline{CS}$ = low).

VIDEO INTERFACE

HSYNC (Horizontal Sync)

The HSYNC active-high output signal determines the start of the horizontal raster line. It may drive a CRT monitor directly or may be used for composite video generation. HSYNC time position and width are fully programmable.

VSYNC (Vertical Sync)

The VSYNC active-high output signal determines the start of the vertical frame. Like HSYNC, VSYNC may drive a CRT monitor or composite video generation circuits. VSYNC time position and width are both programmable.

DISPLAY ENABLE (Display Enable)

The DISPLAY ENABLE active-high output signal indicates when the R6545 is generating active display information. The number of horizontal display characters per row and the number of vertical display rows are both fully programmable and together generate the DISPLAY ENABLE signal. DISPLAY ENABLE may be delayed one character time by setting bit 4 of R8 to a 1.

CURSOR (Cursor Coincidence)

The CURSOR active-high output signal indicates when the scan coincides with the programmed cursor position. The cursor position is programmable to any character in the address field. Furthermore, within the character, the cursor may be programmed to be any block of scan lines, since the cursor start scan line and end scan line are both programmable. The cursor output may be delayed by one character time by setting Bit 5 of R8 to a 1.

LPEN (Light Pen Strobe)

The LPEN edge-sensitive input signal loads the internal Light Pen Register. A low-to-high transition activates LPEN.

CCLK (Clock)

The CCLK character timing clock input signal is the time base for all internal count/control functions.

$\overline{RES}$

The $\overline{RES}$ active-low input signal initializes all internal scan counter circuits. When $\overline{RES}$ is low, all internal counters stop and clear and all scan and video outputs go low; control registers are unaffected. $\overline{RES}$ must stay low for at least one CCLK period. All scan timing initiates when $\overline{RES}$ goes high. In this way, $\overline{RES}$ can synchronize display frame timing with line frequency. $\overline{RES}$ may also synchronize multiple CRTC's in horizontal and/or vertical split screen operation.

REFRESH RAM AND CHARACTER ROM INTERFACE

MA0-MA13 (Refresh RAM Address Lines)

These 14 active-high output signals address the refresh RAM for character storage and display operations. The starting scan address is fully programmable and the ending scan address is determined by the total number of characters displayed, which is also programmable, in terms of characters/line and lines/frame.

There are two selectable address modes for MA0-MA13:

In the straight binary mode (R8, Mode Control, bit 2 = 0), characters are stored in successive memory locations. Thus, the software design must translate row and column character coordinates into sequentially-numbered addresses for Refresh memory operations.

In the row/column mode (R8, Mode Control, bit 2 = 1), MA0-MA7 become column addresses CC0-CC7 and MA8-MA13 become row address CR0-CR5. In this case, the software manipulates characters in terms of row and column locations, but additional address compression circuits are needed to convert the CC0-CC7 and CR0-CR5 addresses into a memory-efficient binary address scheme.

RA0-RA4 (Raster Address Lines)

These five active-high output signals select each raster scan within an individual character row. The number of raster scan lines is programmable and determines the character height, including spaces between character rows.

The high-order line, RA4, is unique in that it can also function as a strobe output pin when the R6545 is programmed to operate in the "Transparent Address Mode." In this case the strobe is an active-high output and is true at the time the Refresh RAM updates address gates on to the address lines, MA0-MA13. In this way, updates and readouts of the Refresh RAM can be made under control of the R6545 with only a small amount of external circuitry.

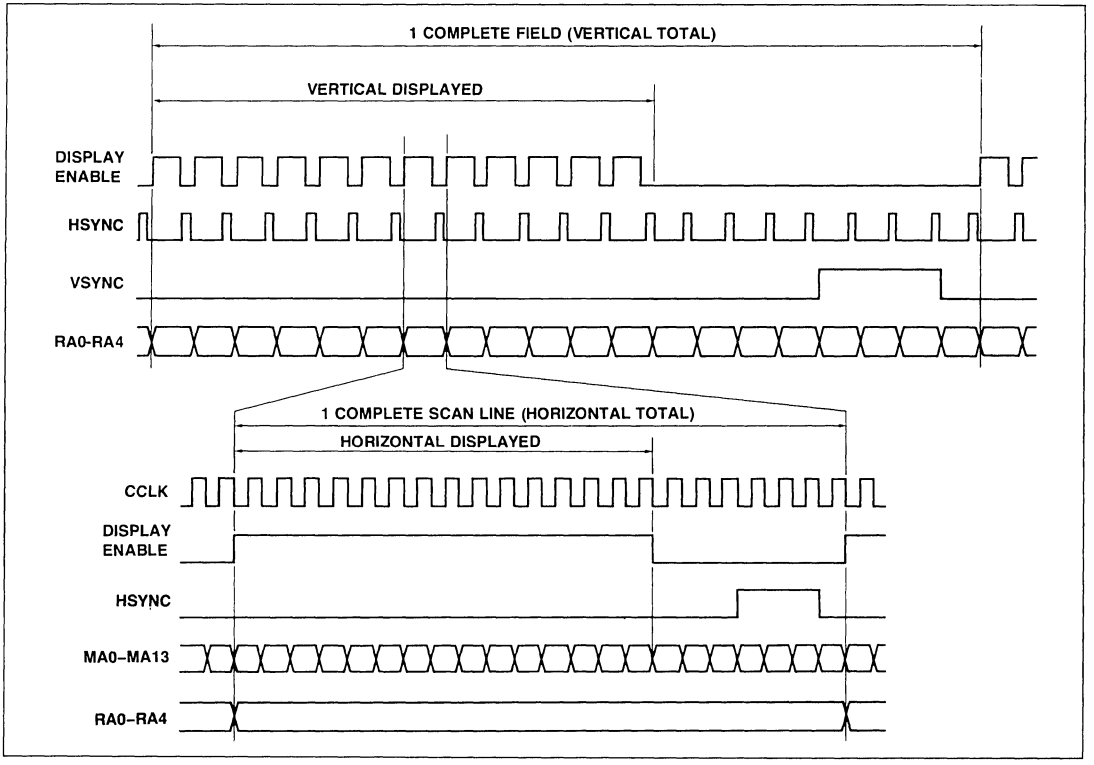


Figure 2. Vertical and Horizontal Timing

INTERNAL REGISTER DESCRIPTION

Table 1 summarizes the internal registers and indicates their address selection and read/write capabilities.

ADDRESS REGISTER

7	6	5	4	3	2	1	0
—	—	—	A_4	A_3	A_2	A_1	A_0

This 5-bit write-only register is used as a "pointer" to direct CRTC/CPU data transfers within the CRTC. It contains the number of the desired register (0–31). When RS is low, this register may be loaded; when RS is high, the selected register is the one whose identity is stored in this address register.

STATUS REGISTER (SR)

7	6	5	4	3	2	1	0
UR	LRF	VRT	—	—	—	—	—

This 3-bit register contains the status of the CRTC.

SR 7 — UR —Update Ready
- 0 Register R31 has been either read or written by the CPU.
- 1 An update strobe has occurred.

SR 6 — LRF —LPEN Register Full
- 0 Register R16 or R17 has been read by the CPU.
- 1 LPEN strobe has been received.

SR 5 — VRT —Vertical Re-Trace
- 0 Scan is not currently in the vertical re-trace time.
- 1 Scan is currently in its vertical re-trace time. NOTE: This bit goes to a 1 when vertical re-trace starts. It goes to a 0 five character clock times before vertical re-trace ends to ensure that critical timings for refresh RAM operations are met.

SR 4–0 —Not used.

Table 1. Internal Register Summary

		Address Reg.					Reg.					Register Bit							
$\overline{CS}$	RS	4	3	2	1	0	No.	Register Name	Stored Info.	RD	WR	7	6	5	4	3	2	1	0
1	—	—	—	—	—	—	—												
0	0	—	—	—	—	—	—	Address Reg.	Reg. No.		✓				A_4	A_3	A_2	A_1	A_0
0	0	—	—	—	—	—	—	Status Reg.		✓		UR	LRF	VRT					
0	1	0	0	0	0	0	R0	Horiz. Total	# Charac. – 1		✓	•	•	•	•	•	•	•	•
0	1	0	0	0	0	1	R1	Horiz. Displayed	# Charac.		✓	•	•	•	•	•	•	•	•
0	1	0	0	0	1	0	R2	Horiz. Sync Position	# Charac.		✓	•	•	•	•	•	•	•	•
0	1	0	0	0	1	1	R3	VSYNC, HSYNC Widths	# Scan Lines and # Char. Times		✓	V_3	V_2	V_1	V_0	H_3	H_2	H_1	H_0
0	1	0	0	1	0	0	R4	Vert. Total	# Charac. Row – 1		✓		•	•	•	•	•	•	•
0	1	0	0	1	0	1	R5	Vert. Total Adjust	# Scan LInes		✓				•	•	•	•	•
0	1	0	0	1	1	0	R6	Vert. Displayed	# Charac. Rows		✓		•	•	•	•	•	•	•
0	1	0	0	1	1	1	R7	Vert. Sync Position	# Charac. Rows		✓		•	•	•	•	•	•	•
0	1	0	1	0	0	0	R8	Mode Control			✓	UM	US	CSK	DES	RRA	RAD	IMC	
0	1	0	1	0	0	1	R9	Scan LInes	# Scan Lines – 1		✓				•	•	•	•	•
0	1	0	1	0	1	0	R10	Cursor Start	Scan Line No.		✓		B_1	B_0	•	•	•	•	•
0	1	0	1	0	1	1	R11	Cursor End	Scan Line No.		✓				•	•	•	•	•
0	1	0	1	1	0	0	R12	Display Start Addr (H)			✓			•	•	•	•	•	•
0	1	0	1	1	0	1	R13	Display Start Addr (L)			✓	•	•	•	•	•	•	•	•
0	1	0	1	1	1	0	R14	Cursor Position (H)		✓	✓			•	•	•	•	•	•
0	1	0	1	1	1	1	R15	Cursor Position (L)		✓	✓	•	•	•	•	•	•	•	•
0	1	1	0	0	0	0	R16	Light Pen Reg (H)		✓				•	•	•	•	•	•
0	1	1	0	0	0	1	R17	Light Pen Reg (L)		✓		•	•	•	•	•	•	•	•
0	1	1	0	0	1	0	R18	Update Address Reg (H)			✓			•	•	•	•	•	•
0	1	1	0	0	1	1	R19	Update Address Reg (L)			✓	•	•	•	•	•	•	•	•
0	1	1	1	1	1	1	R31	Dummy Location											

Notes: • Designates used bit in register
Designates unused bit in register. Reading this bit is always 0, except for R31, which does not drive the data bus.

R0—HORIZONTAL TOTAL CHARACTERS

7	6	5	4	3	2	1	0
NUMBER OF CHARACTERS – 1							

This 8-bit write-only register contains the total of displayed and non-displayed characters, minus one, per horizontal line. This register determines the frequency of HSYNC.

R1—HORIZONTAL DISPLAYED CHARACTERS

7	6	5	4	3	2	1	0
NUMBER OF CHARACTERS							

This 8-bit write-only register contains the number of displayed characters per horizontal line.

R2—HORIZONTAL SYNC POSITION

7	6	5	4	3	2	1	0
HORIZONTAL SYNC POSITION							

This 8-bit write-only register contains the position of HSYNC on the horizontal line, in terms of the character location number on the line. The position of the HSYNC determines the left to right location of the displayed text on the video screen. In this way, the side margins are adjusted.

R3—HORIZONTAL AND VERTICAL SYNC WIDTHS

7	6	5	4	3	2	1	0
V_3	V_2	V_1	V_0	H_3	H_2	H_1	H_0

This 8-bit write-only register contains the widths of both HSYNC and VSYNC as follows:

HVSW
7–4 VSYNC Pulse Width
The width of the vertical sync pulse (VSYNC) expressed as the number of scan lines. When bits 4–7 are all 0, VSYNC is 16 scan lines wide.

HVSW
3–0 HSYNC Pulse Width
The width of the horizontal sync pulse (HSYNC) expressed as the number of character clock times (CCLK). When bits 0–3 are all zero, HSYNC is 16 bit times wide.

Control of these parameters allows the R6545 to interface with a variety of CRT monitors, since the HSYNC and VSYNC timing signals may be accommodated without the use of external one shot timing.

R4—VERTICAL TOTAL ROWS

7	6	5	4	3	2	1	0
—	NO. OF CHAR. ROWS – 1						

The 7-bit Vertical Total Register contains the total number of character rows in a frame, minus one. This register, along with R5, determines the overall frame rate, which should be close to the line frequency to ensure flicker-free appearance. If the frame time is adjusted to be longer than the period of the line frequency, then $\overline{RES}$ may provide absolute synchronism.

R5—VERTICAL TOTAL LINE ADJUST

7	6	5	4	3	2	1	0
—	—	—	SCAN LINES				

The 5-bit write-only Vertical Total Line Adjust Register (R5) contains the number of additional scan lines needed to complete an entire frame scan and is intended as a fine adjustment for the video frame time.

R6—VERTICAL DISPLAYED ROWS

7	6	5	4	3	2	1	0
—	DISPLAYED CHAR. ROWS						

This 7-bit write-only register contains the number of displayed character rows in each frame. This determines the vertical size of the displayed text.

R7—VERTICAL SYNC POSITION

7	6	5	4	3	2	1	0
—	VERTICAL POSITION						

This 7-bit write-only register selects the character row time at which the vertical SYNC pulse occurs and, thus, positions the displayed text in the vertical direction.

R8—MODE CONTROL (MC)

7	6	5	4	3	2	1	0
UM(T)	US(T)	CSK	DES	RRA	RAD	IMC	

This 8-bit write-only register selects the operating modes of the R6545, as follows:

MC
7 UM(T)—Update/Read Mode (Transparent Mode)
0 Update occurs during horizontal and vertical blanking times with update strobe.
1 Update interleaves during Ø2 portion of cycle.

MC
6 US(T) —Update Strobe (Transparent Mode)
0 Pin 34 functions as memory address (RA4).
1 Pin 34 functions as update strobe (STB).

MC
5 CSK —Cursor Skew
0 No delay.
1 Delays Cursor one character time.

MC
4 DES —Display Enable Skew
0 No delay.
1 Display Enable delays one character time.

MC 3	RRA —Refresh RAM Access
0	Shared memory access
1	Transparent memory access

MC 2	RAD —Refresh RAM Addressing Mode
0	Straight binary addressing
1	Row/column addressing

MC1-MC0 IMC —Interlace Mode Control

MC 1	MC 0	Operation
X	0	Non-interlace
0	1	Interlace SYNC raster scan
1	1	Interlace SYNC and video raster scan

R9—ROW SCAN LINES

7	6	5	4	3	2	1	0
—	—	—	SCAN LINES −1				

This 5-bit write-only register contains the number of scan lines, minus one, per character row, including spacing.

R10—CURSOR START LINE

7	6	5	4	3	2	1	0
—	B_1	B_0	START SCAN LINE				

R11—CURSOR END LINE

7	6	5	4	3	2	1	0
—	—	—	END SCAN LINE				

These 5-bit write-only registers select the starting and ending scan lines for the cursor. In addition, bits 5 and 6 of R10 are used to select the cursor blink mode, as follows:

B_1	B_0	Cursor Operating Mode
0	0	Display Cursor Continuously
0	1	Blank Cursor
1	0	Blink cursor at 1/16 Field Rate
1	1	Blink Cursor at 1/32 Field Rate

A one character wide cursor can be controlled by storing values into the Cursor Start Line (R10) and Cursor End Line (R11) registers and into the Cursor Position Address High (R14) and Cursor Position Low (R15) registers.

R12—DISPLAY START ADDRESS HIGH

7	6	5	4	3	2	1	0
—	—	DISPLAY START ADDRESS HIGH					

R13—DISPLAY START ADDRESS LOW

7	6	5	4	3	2	1	0
DISPLAY START ADDRESS LOW							

These registers together form a 14-bit register whose contents are the memory address of the first character to be displayed (the character on the top left of the video display, as in Figure 4). Subsequent memory addresses are generated by the R6545 as a result of CCLK input pulses. Scrolling of the display is accomplished by changing R12 and R13 to the memory address of the first character of the first line of text to be displayed. Entire pages of text may be scrolled or changed as well via R12 and R13.

R14—CURSOR POSITION HIGH

7	6	5	4	3	2	1	0
—	—	CURSOR POSITION HIGH					

R15—CURSOR POSITION LOW

7	6	5	4	3	2	1	0
CURSOR POSITION LOW							

These registers together form a 14-bit register whose contents are the memory address of the current cursor position. When the video display scan counter (MA lines) matches the contents of this register, and when the scan line counter (RA lines) falls within the bounds set by R10 and R11, then the CURSOR output becomes active. Bit 5 of the Mode Control Register (R8) may be used to delay the CURSOR output by a full CCLK time to accommodate slow access memories.

The cursor is positioned on the screen by loading the Cursor Position Address High (R14) and Cursor Position Address Low (R15) registers with the desired refresh RAM address. The cursor can be positioned in any of the 16K character positions. Hardware paging and data scrolling is thus allowed without loss of cursor position. Figure 3 is an example of several cursor options.

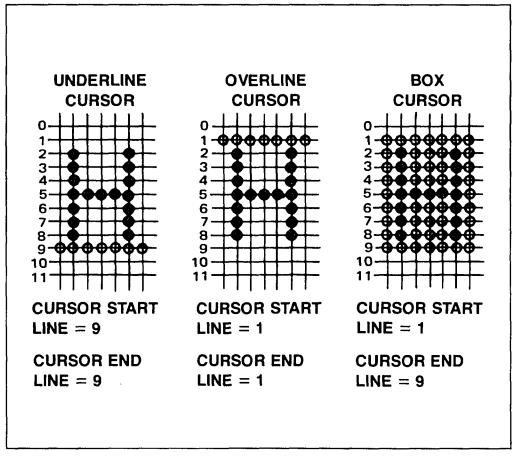


Figure 3. Cursor Display Scan Line Control Examples

R16—LIGHT PEN HIGH

7	6	5	4	3	2	1	0
—	—	LPEN HIGH					

R17—LIGHT PEN LOW

7	6	5	4	3	2	1	0
LPEN LOW							

These registers together form a 14-bit register whose contents are the light pen strobe position, in terms of the video display address at which the strobe occurred. When the LPEN input changes from low to high, then, on the next negative-going edge of CCLK, the contents of the internal scan counter is stored in registers R16 and R17.

R18—UPDATE ADDRESS HIGH

7	6	5	4	3	2	1	0
—	—	UPDATE ADDRESS HIGH					

R19—UPDATE ADDRESS LOW

7	6	5	4	3	2	1	0
UPDATE ADDRESS LOW							

These registers together comprise a 14-bit register whose contents are the memory address at which the next read or update will occur (for transparent address mode only). Whenever a read/update occurs, the update location automatically increments to allow for fast updates or readouts of consecutive character locations. The section on REFRESH RAM ADDRESSING describes this more fully.

R31—DUMMY LOCATION

7	6	5	4	3	2	1	0
—	—	—	—	—	—	—	—

This register does not store any data, but is required to detect transparent addressing updates. This is necessary to increment the Update Address Register and to set the Update Ready bit in the status register.

REGISTER FORMATS

Register pairs R12/R13, R14/R15, R16/R17, and R18/R19 are formatted in one of two ways:

(1) Straight binary, if register R8, bit 2 = 0
(2) Row/Column, if register R8, bit 2 = 1. In this case the low byte is the Character Column and the high byte is the Character Row.

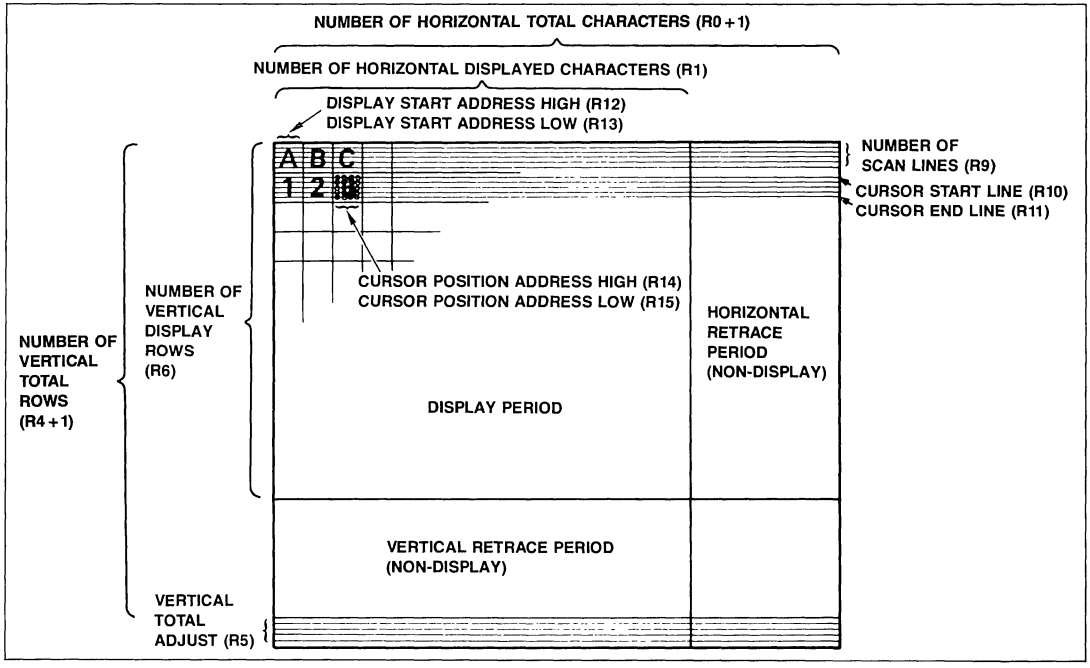


Figure 4. Video Display Format

DESCRIPTION OF OPERATION

VIDEO DISPLAY

Figure 4 indicates the relationship of the various program registers in the R6545 and the resulant video display.

Non-displayed areas of the Video Display are for horizontal and vertical retrace functions of the CRT monitor. The horizontal and vertical sync signals, HSYNC and VSYNC, are programmed to occur during these intervals and trigger the retrace in the CRT monitor. The pulse widths are constrained by the monitor requirements. The time position of the pulses may be adjusted to vary the display margins (left, right, top, and bottom).

REFRESH RAM ADDRESSING

There are two modes of addressing for the video display memory:

Shared Memory Mode (R8, BIT 3 = 0)

In this mode, the Refresh RAM address lines (MA0–MA13) directly reflect the contents of the internal refresh scan character counter. Multiplex control, to permit addressing and selection of the RAM by both the CPU and the CRTC, must be provided externally to the CRTC. In the Row/Column address mode, lines MA0–MA7 become character column addresses (CC0–CC7) and MA8–MA13 become character row addresses (CR0–CR5). Figure 5 illustrates the system configuration.

Transparent Memory Addressing (R8, BIT 3 = 1)

For this mode, the display RAM is not directly accessible by the CPU, but is controlled entirely by the R6545. All CPU accesses are made via the R6545 and a small amount of external circuitry. Figure 6 shows the system configuration for this approach.

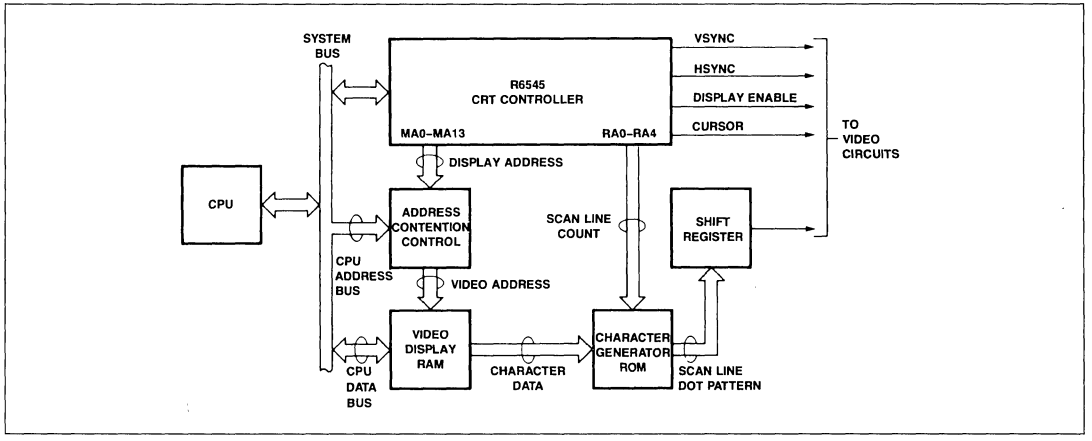


Figure 5. Shared Memory System Configuration

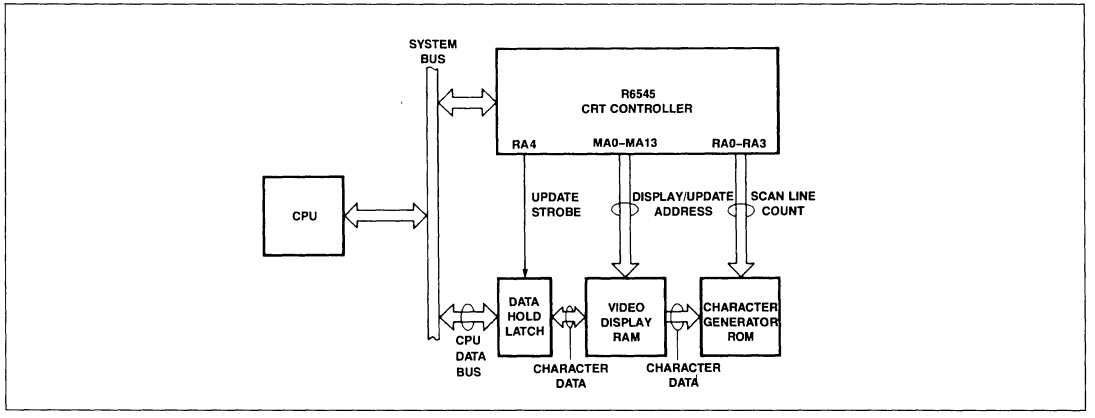


Figure 6. Transparent Memory Addressing System Configuration
(Data Hold Latch Needed for Horizontal/Vertical Blanking Updates, Only).

ADDRESSING MODES

Figure 7 illustrates the address sequence for both modes of the Refresh RAM address.

Row/Column

In this mode, the CRTC address lines (MA0–MA13) generate 8 column (MA0–MA7) and 6 row (MA8–MA13) addresses. Extra hardware is needed to compress this addressing into a straight binary sequence in order to conserve memory in the refresh RAM (register R8, bit 2 is a 1).

Binary

In this mode, the CRTC address lines are straight binary and no compression circuits are needed. However, software complexity increases since the CRT characters cannot be stored in terms of their row and column locations, but must be sequential (register R8, bit 2 is a 0).

USE OF DYNAMIC RAM FOR REFRESH MEMORY

The R6545 permits use of dynamic RAMS as storage devices for the Refresh RAM by continuing to increment memory addresses in the non-display intervals of the scan. This is a viable technique, since the Display Enable signal controls the actual video display blanking. Figure 7 illustrates Refresh RAM addressing for both row/column and binary addressing for 80 columns and 24 rows with 10 non-displayed columns and 10 non-displayed rows.

Note that the straight-binary mode has the advantage that all display memory addresses are stored in a continuous memory block, starting with address 0 and ending at 1919. The disadvantage with this method is that, if it is desired to change a displayed character location, the row and column identity of the location must be converted to its binary address before the memory may be written. The row/column mode, on the other hand, does not need to undergo this conversion. However, memory is not used as efficiently, since the memory addresses are not continuous, gaps exist. This requires that the system be equipped with more memory than actually used and this extra memory is wasted. Alternatively, address compression logic may be employed to translate the row/column format into a continuous address block.

The user selects whichever mode is best for the given application. The trade-offs between the modes are software versus hardware. Straight-binary mode minimizes hardware requirements and row/column minimizes software requirements.

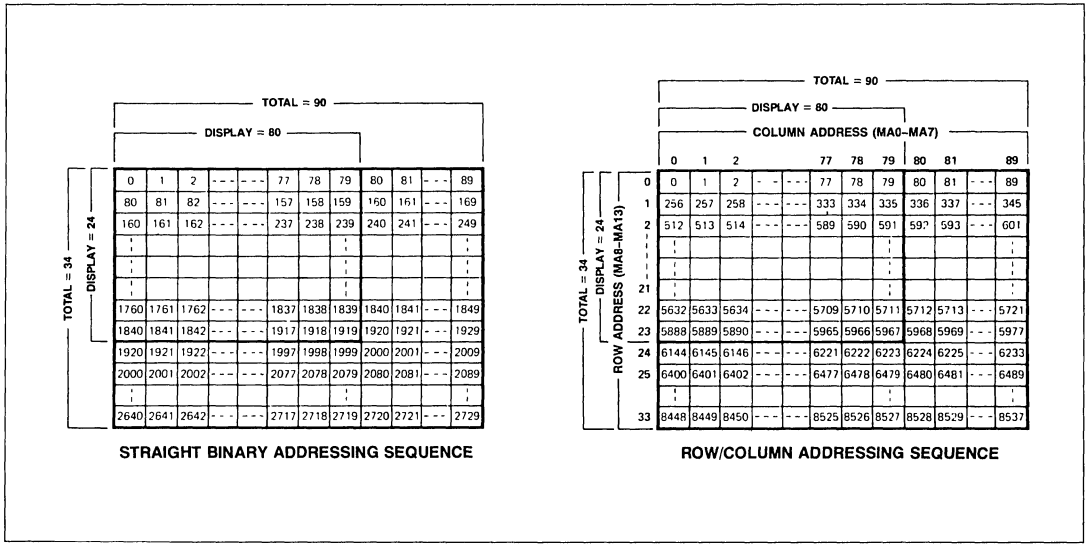


Figure 7. Display Address Sequences (with Start Address = 0) for 80 × 24 Example

MEMORY CONTENTION SCHEMES FOR SHARED MEMORY ADDRESSING

From the diagram of Figure 5, it is clear that both the R6545 and the system CPU must address the video display memory. The R6545 repetitively fetches character information to generate the video signals in order to keep the screen display active. The CPU occasionally accesses the memory to change the displayed information or to read out current data characters. Three ways of resolving this dual-contention requirement are apparent:

- **CPU Priority**

  In this technique, the address lines to the video display memory are normally driven by the R6545 unless the CPU needs access, in which case the CPU addresses immediately override those from the R6545 giving the CPU immediate access.

- **Ø1 and Ø2 Memory Interleaving**

  This method permits both the R6545 and the CPU to access the video display memory by time-sharing. During the Ø1 portion of each cycle (the time when Ø2 is low), the R6545 address outputs are gated to the video display memory. During Ø2 time, the CPU address lines are switched in. This way, both the R6545 and the CPU have unimpeded access to the memory. Figure 8 illustrates these timings.

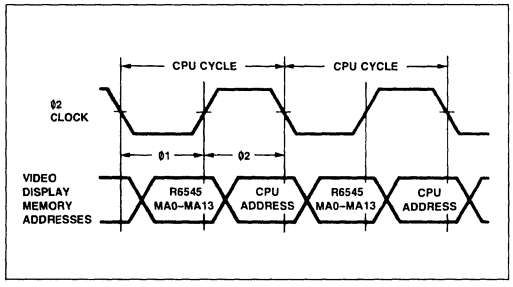


Figure 8. Ø1 and Ø2 Interleaving

- **Vertical Blanking**

  With this approach, the address circuitry is identical to the case for CPU Priority updates. The only difference is that the Vertical Retrace status bit (bit 5 of the Status Register) is used by the CPU so that access to the video display memory is only made during vertical blanking time (when bit 5 is a 1). In this way, no visible screen perturbations result. See Figure 10 for details.

TRANSPARENT MEMORY ADDRESSING

In this mode of operation, the video display memory address lines are not switched by contention circuits, but are generated by the R6545. In effect, the contention is handled by the R6545. As a result, the schemes for accomplishing CPU memory access are different:

- **Ø1 and Ø2 Interleaving**

  This mode is similar to the Interleave mode used with shared memory. In this case, however, the Ø2 address is generated from the Update Address Register (R18 and R19) in the R6545. The CPU loads the address to be accessed into R18/R19. This address is then gated onto the MA lines during Ø2. Figure 9 shows the timing.

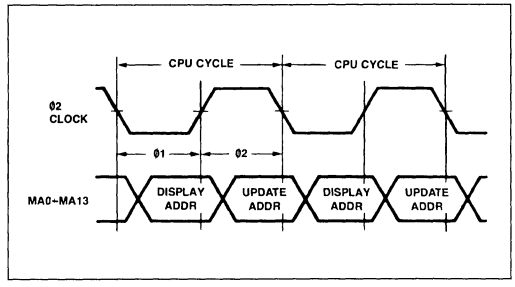


Figure 9. Ø1 and Ø2 Transparent Interleaving

- **Horizontal/Vertical Blanking**

  In this mode, the CPU loads the Update Address into R18 and R19. This address is gated onto the MA lines during horizontal or vertical blank times, so memory accesses do not interfere with the display appearance. Pin 34 can be programmed, by R8 bit 6, to function as an update strobe which signals the presence of an update address on the MA lines. Data hold latches are necessary to temporarily retain the character to be stored until the retrace time occurs. In this way, the system CPU is not halted waiting for the blanking time to arrive. Figure 11 illustrates the address and strobe timing for this mode.

CURSOR AND DISPLAY ENABLE SKEW CONTROL

Bits 4 and 5 of the Mode Control register (R8) are used to delay the Display Enable and Cursor outputs, respectively. Figure 12 illustrates the effect of the delays.

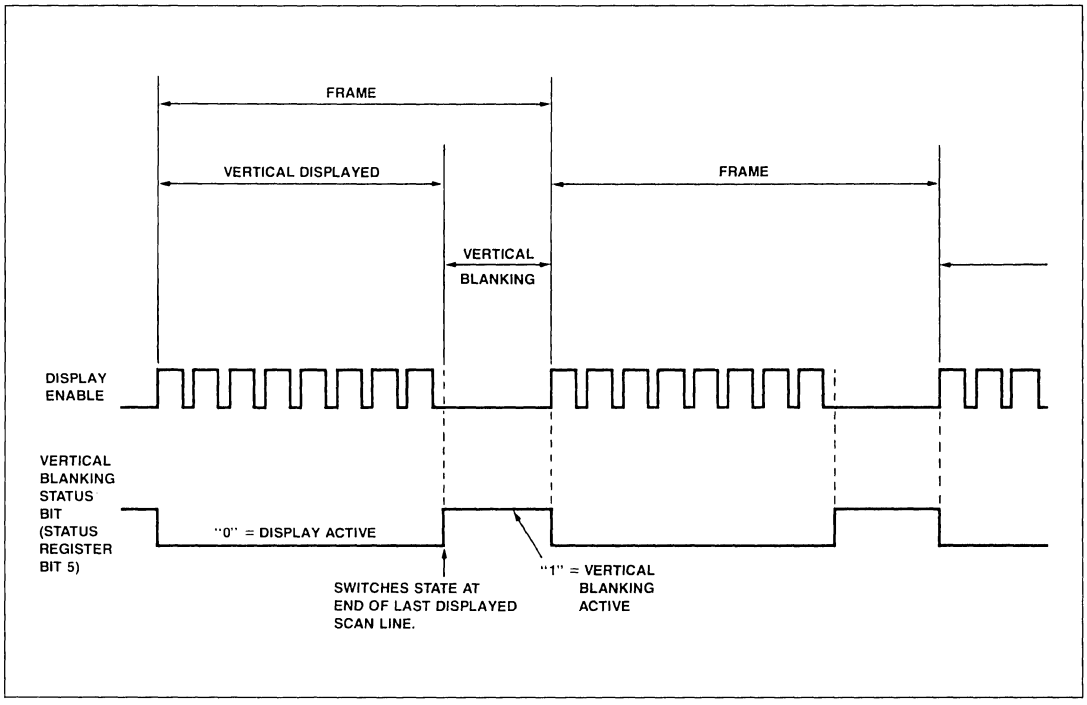


Figure 10. Operation of Vertical Blanking Status Bit

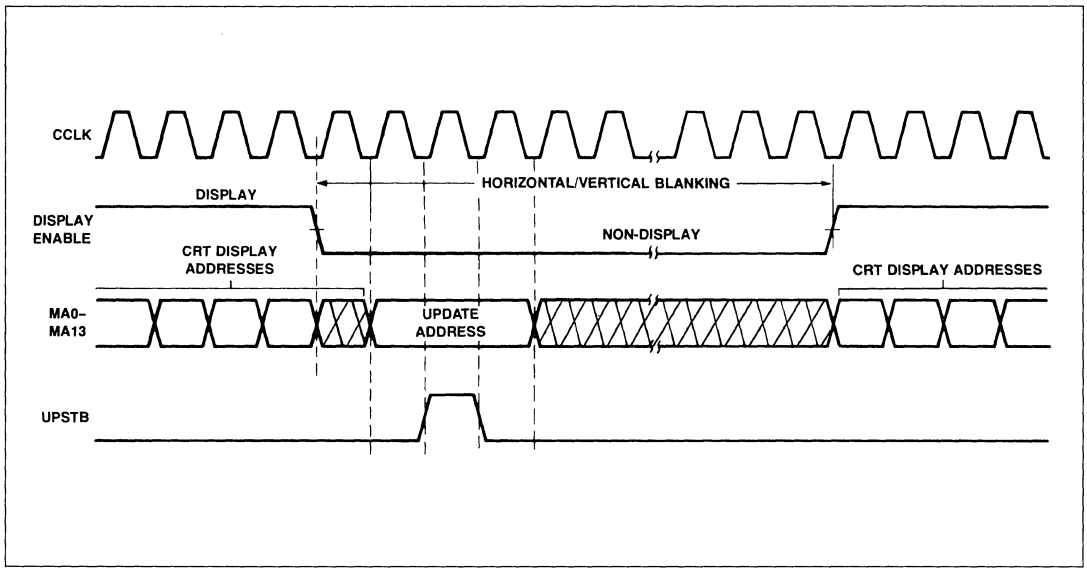


Figure 11. Retrace Update Timing

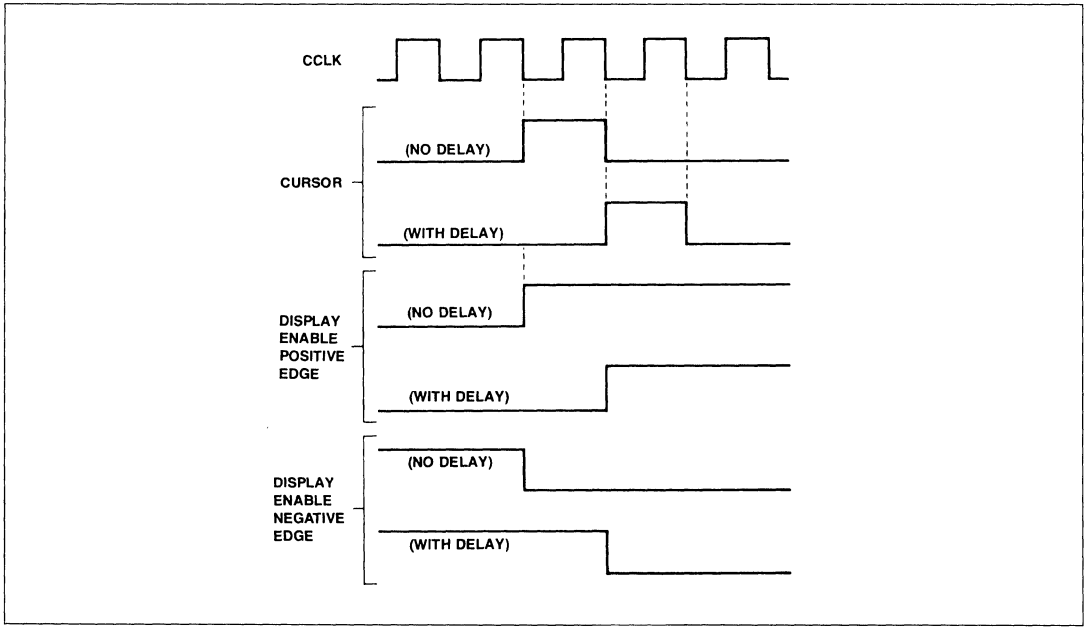


Figure 12. Cursor and Display Enable Skew

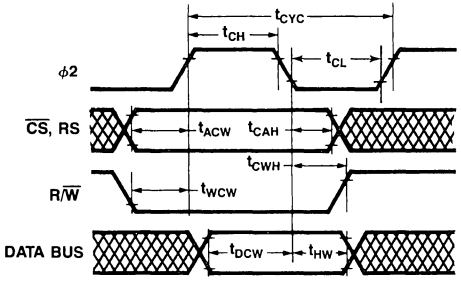
BUS WRITE TIMING CHARACTERISTICS (V_{CC} = 5.0V ± 5%, T_A = T_L to T_H, unless otherwise noted)

Symbol	Characteristic	1 MHz		2 MHz		Unit
		Min.	Max.	Min.	Max.	
t_{CYC}	Cycle Time	1.0	—	0.5	—	μs
t_{CH}	ϕ2 Pulse Width High	440	—	200	—	ns
t_{CL}	ϕ2 Pulse Width Low	420	—	190	—	ns
t_{ACW}	Address Set-Up Time	80	—	40	—	ns
t_{CAH}	Address Hold Time	0	—	0	—	ns
t_{WCW}	R/$\overline{W}$ Set-Up Time	80	—	40	—	ns
t_{CWH}	R/$\overline{W}$ Hold Time	0	—	0	—	ns
t_{DCW}	Data Bus Set-Up Time	165	—	60	—	ns
t_{HW}	Data Bus Hold Time	10	—	10	—	ns
(t_R and t_F = 10 to 30 ns)						

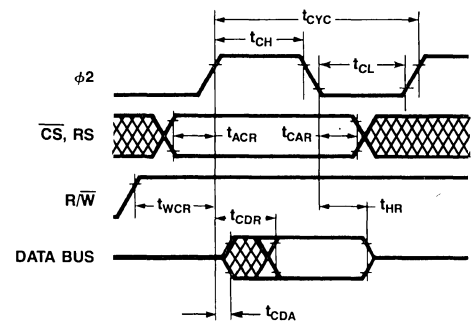
BUS READ TIMING CHARACTERISTICS (V_{CC} = 5.0V ± 5%, T_A = T_L to T_H, unless otherwise noted)

Symbol	Characteristic	1 MHz		2 MHz		Unit
		Min.	Max.	Min.	Max.	
t_{CYC}	Cycle Time	1.0	—	0.5	—	μs
t_{CH}	ϕ2 Pulse Width	440	—	200	—	ns
t_{CL}	ϕ2 Pulse Width Low	420	—	190	—	ns
t_{ACR}	Address Set-Up Time	80	—	40	—	ns
t_{CAR}	Address Hold Time	0	—	0	—	ns
t_{WCR}	R/$\overline{W}$ Set-Up Time	80	—	40	—	ns
t_{CDR}	Read Access Time (Valid Data)	—	290	—	150	ns
t_{HR}	Read Hold Time	10	—	10	—	ns
t_{CDA}	Data Bus Active Time (Invalid Data)	40	—	40	—	ns
(t_R and t_F = 10 to 30 ns)						

BUS WRITE TIMING WAVEFORMS



BUS READ TIMING WAVEFORMS

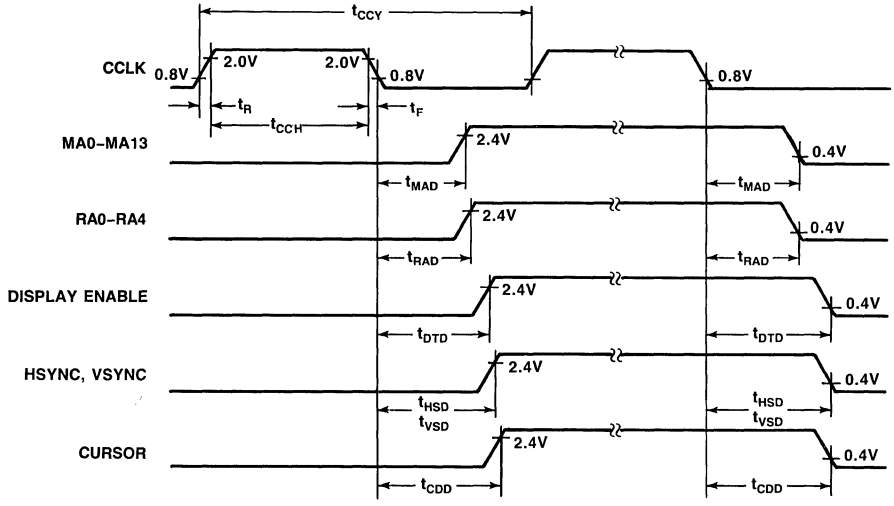


MEMORY AND VIDEO INTERFACE CHARACTERISTICS

(V_{CC} = 5.0V ± 5%, T_A = T_L to T_H, unless otherwise noted)

Symbol	Parameter	R6545			R6545E			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
t_{CCH}	Minimum Clock Pulse Width, High	200			130			ns
t_{CCY}	Clock Frequency			2.5			3.7	MHz
t_R, t_F	Rise and Fall Time for Clock Input			20			20	ns
t_{MAD}	Memory Address Delay Time		180	300		100	160	ns
t_{RAD}	Raster Address Delay Time		180	300		100	160	ns
t_{DTD}	Display Timing Delay Time		240	450		160	300	ns
t_{HSD}	Horizontal Sync Delay Time		240	450		160	300	ns
t_{VSD}	Vertical Sync Delay Time		240	450		160	300	ns
t_{CDD}	Cursor Display Timing Delay Time		240	450		160	300	ns

MEMORY AND VIDEO INTERFACE WAVEFORMS



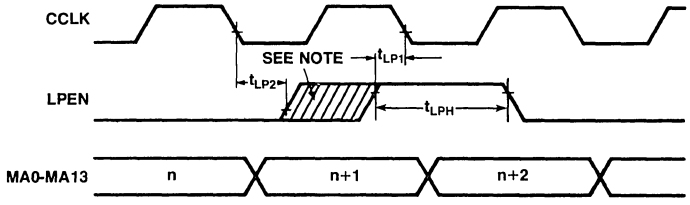
LIGHT PEN STROBE TIMING CHARACTERISTICS (For Reference Only)

Symbol	Characteristic	R6545		R6545A		Unit
		Min.	Max.	Min.	Max.	
t_{LPH}	LPEN Hold Time	150	—	100	—	ns
t_{LP1}	LPEN Setup Time	—	120	—	120	ns
t_{LP2}	CCLK to LPEN Delay	—	0	—	0	ns

Note: t_R, t_F = 20 ns (max)

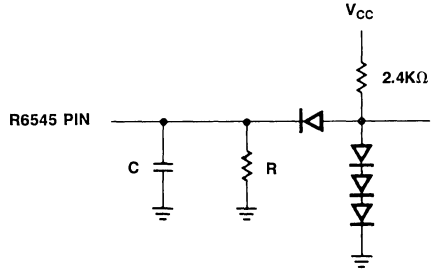
2

LIGHT PEN STROBE TIMING WAVEFORMS



NOTE: "Safe" time position for LPEN positive edge to cause address n+2 to load into Light Pen Register.
t_{LP2} and t_{LP1} are time positions causing uncertain results.

TEST LOAD



R = 11KΩ FOR D0-D7
= 24KΩ FOR ALL OTHER OUTPUTS
C = 130 pF TOTAL FOR D0-D7
= 30 pF ALL OTHER OUTPUTS

CRTC Register Comparison

REGISTER	MC6845R HD6845R	HD6845S	R6545-1	R6545/R6545E
GENERAL FUNCTIONS				
R0 HORIZONTAL TOT	TOT-1	TOT-1	TOT-1	TOT-1
R1 HORIZONAL DISP	ATUAL	ACTUAL	ACTUAL	ACTUAL
R2 HORIZONTAL SYNC	ACTUAL	ACTUAL	ACTUAL	ACTUAL
R3 HORIZ AND VERT SYNC WIDTH	HORIZONTAL	HORIZONTAL AND VERTICAL	HORIZONTAL AND VERTICAL	HORIZONTAL AND VERTICAL
R4 VERTICAL TOT	TOT-1	TOT-1	TOT-1	TOT-1
R5 VERTICAL TOT ADJ	ANY VALUE	ANY VALUE	ANY VALUE EXCEPT R5 = R9H• X	ANY VALUE
R6 VERTICAL DISP	ANY VALUE <R4	ANY VALUE <R4	ANY VALUE <R4	ANY VALUE <R4
R7 VERTICAL SYNC POS	ACTUAL	ACTUAL	ACTUAL	ACTUAL
R8 MODE REG BITS 0 and 1	INTERLACE MODE SELECT	INTERLACE MODE SELECT	—	INTERLACE MODE SELECT
BITS 2	—	—	ROW/COLUMN OR STRAIGHT BINARY ADDRESSING	ROW/COLUMN OR STRAIGHT BINARY ADDRESSING
BITS 3	—	—	SHARED OR TRANSPARENT ADDR	SHARED OR TRANSPARENT ADDR
BITS 4	—	DISPEN SKEW	DISPEN SKEW	DISPEN SKEW
BITS 5	—	DISPEN SKEW	CURSOR SKEW	CURSOR SKEW
BITS 6	—	CURSOR SKEW	RA4/UPSTB	RA4/UPSTB
BITS 7	—	CURSOR SKEW	TRANSPARENT MODE SELECT	TRANSPARENT MODE SELECT
R9 SCAN LINES	TOT-1	TOT-1	TOT-1	TOT-1
R10 CURSOR START	ACTUAL	ACTUAL	ACTUAL	ACTUAL
R11 CURSOR END	ACTUAL	ACTUAL	ACTUAL	ACTUAL
R12/R13 DISP ADDR	WRITE ONLY	READ/WRITE	WRITE ONLY	WRITE ONLY
R14/R15 CURSOR POS	WRITE ONLY	READ/WRITE	READ/WRITE	READ/WRITE
R16/R17 LPEN REG	READ ONLY	READ ONLY	READ ONLY	READ ONLY
R18/R19 UPDATE ADDR REG	N/A	N/A	TRANSPARENT MODE ONLY	TRANSPARENT MODE ONLY
R31 DUMMY REG	N/A	N/A	TRANSPARENT MODE ONLY	TRANSPARENT MODE ONLY
STATUS REG	NO	NO	YES	YES
INTERLACE SYNC				
R0	TOT-1 = ODD	TOT-1 = ODD	—	TOT-1 = ODD OR EVEN
R4 VERTICAL	TOT-1	TOT-2	—	TOT-1
R6 VERT DISP	TOT/2	TOT	—	TOT
R7 VERT SYNC	ACTUAL	ACTUAL	—	ACTUAL
R9 SCAN LINES	TOT-1 EVEN ONLY	TOT-2 ODD/EVEN	TOT-1 ODD/EVEN	TOT-1 ODD/EVEN
R10 CURSOR START R11 CURSOR END	BOTH ODD OR BOTH EVEN	ODD/EVEN ODD/EVEN	— —	ODD/EVEN ODD/EVEN
CHARACTER CLOCK FREQUENCY				
CCLK	2.5 MHz	3.7 MHz	2.5 MHz	3.7 MHz*

Notes: — = Does not apply * R6545 = 2.5 MHz R6545E = 3.7 MHz

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to +7.0	V
Input Voltage	V_{IN}	−0.3 to +7.0	V
Operating Temperature Range Commercial Industrial	T_A	 0 to +70 −40 to +85	°C
Storage Temperature	T_{STG}	−55 to +150	°C

***NOTE:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2

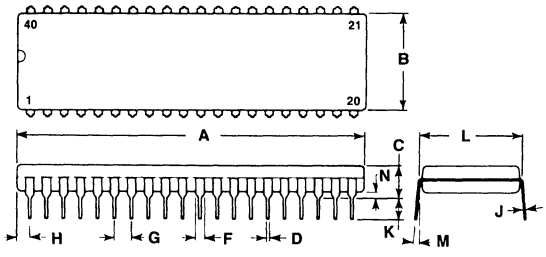
DC CHARACTERISTICS

(V_{CC} = 5.0V ±5%, T_A = T_L to T_H, unless otherwise noted)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Input High Voltage	V_{IH}	2.0		V_{CC}	V	
Input Low Voltage	V_{IL}	−0.3		0.8	V	
Input Leakage Ø2, R/$\overline{W}$, $\overline{RES}$, $\overline{CS}$, RS, LPEN, CCLK	I_{IN}	—		2.5	μA	
Three-State Input Leakage D0–D7	I_{TSI}	—		±10.0	μA	V_{IN} = 0.4V to 2.4V
Output High Voltage D0–D7 All other outputs	V_{OH}	2.4		—	V	 I_{LOAD} = 205 μA I_{LOAD} = 100 μA
Output Low Voltage	V_{OL}	—		0.4	V	I_{LOAD} = 1.6 mA
Input Capacitance Ø2, R/$\overline{W}$, $\overline{RES}$, $\overline{CS}$, RS, LPEN, CCLK D0–D7	C_{IN}	 — —		 10.0 12.5	pF	V_{IN} = 0V T_A = 25°C f = 1MHz
Output Capacitance	C_{OUT}	—		10.0	pF	
Power Dissipation Commercial Industrial	P_D	—	 350 350	 700 800	mW	V_{CC} = 5.25V

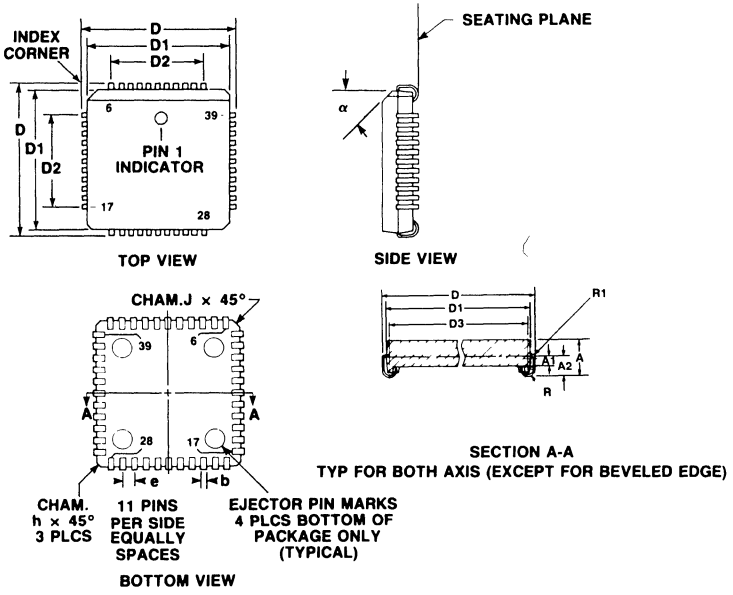
PACKAGE DIMENSIONS

40-PIN PLASTIC DIP



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	51.28	52.32	2.040	2.060
B	13.72	14.22	0.540	0.560
C	3.55	5.06	0.140	0.200
D	0.36	0.51	0.014	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.30	0.008	0.012
K	3.30	4.32	0.130	0.170
L	15.24 BSC		0.600 BSC	
M	7°	10°	7°	10°
N	0.51	1.02	0.020	0.040

44-PIN PLASTIC LEADED CHIP CARRIER (PLCC)



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.14	4.39	0.163	0.173
A1	1.37	1.47	0.054	0.058
A2	2.31	2.46	0.091	0.097
b	0.457 TYP		0.018 TYP	
D	17.45	17.60	0.687	0.693
D1	16.46	16.56	0.648	0.652
D2	12.62	12.78	0.497	0.503
D3	15.75 REF		0.620 REF	
e	1.27 BSC		0.050 BSC	
h	1.15 TYP		0.045 TYP	
J	0.25 TYP		0.010 TYP	
α	45° TYP		45° TYP	
R	0.89 TYP		0.035 TYP	
R1	0.25 TYP		0.010 TYP	

R6549
Color Video Display Generator (CVDG)

PRELIMINARY

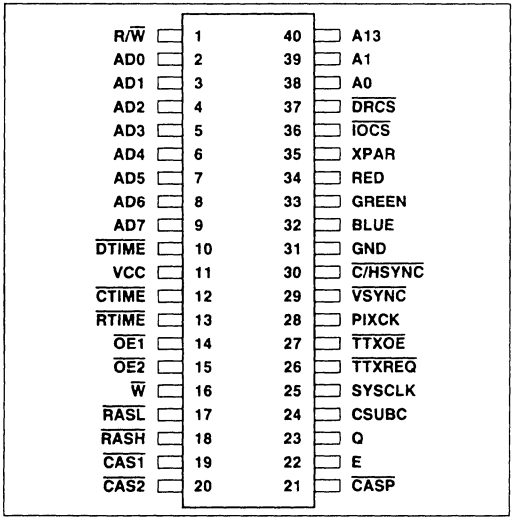
DESCRIPTION

The Rockwell R6549 Color Video Display Generator (CVDG) integrates video raster control; color lookup table (LUT) update and access; color generation and display refresh; teletext data DMA addressing, data routing and handshake; dynamic RAM (DRAM) control and refresh; and MPU/CVDG/DMA access to DRAM into a single device. Internal horizontal and vertical state machines generate video synchronization signals and control access of video color data from DRAM. A 16-entry color lookup table (LUT) supports 4-bit encoded color levels for red, green and blue (RGB) colors allowing 4096 color combinations to be generated. Each color code is converted to a 16-level analog signal by a dedicated DAC, combined with a blanking signal, and output in sync with a pixel clock.

Control registers allow MPU selection of CVDG operating mode and options while data registers allow MPU update of LUT data, current drawing pointer (CDP) graphics, Y scroll pointer and teletext pointer. The data registers can also be monitored by the MPU as can mode and raster scan status.

The R6549 is the first display generator to be designed exclusively in support of North American Presentation Level Protocol Syntax (NAPLPS) videotex (VTX) and teletext (TTX).

Replacing over 30 conventional MSI/LSI devices, the R6549 simplifies system design and layout, reduces printed circuit size, and minimizes required support circuits to speed system prototyping and greatly reduce both development and production costs.



R6549 CVDG Pin Assignments

FEATURES

- High performance video generator
  - 2:1 or 1:1 interlace
  - Analog red, green, blue (RGB) outputs
  - 16 levels per color plus blanking
  - 4096 color combinations
  - RS-170 sync and color subcarrier generation
  - 16 entry color look-up table (LUT)
  - RS-170 composite sync output with equalization and serration pulses
  - Internal/external video synchronization
  - Color subcarrier generation with line, field and pixel phase lock
  - Compatible with MC1377 color encoder
- Videotex (VTX)/Teletext (TTX) graphics
  - 256 x 210 x 4 bit-mapped video image buffer
  - Programmable border color
  - Transparent video overlay signal
  - Fast X CDP and Y CDP nibble or byte graphics I/O
  - NAPLPS X – Y origin with smooth Y vertical scroll
  - Fast horizontal drawing support with X auto increment byte write
- Dynamic RAM interface
  - Direct 48k-byte DRAM support, with auto inherent refresh for interfacing to six 16k x 4 DRAMS (4416-150 ns)
  - Supports three methods of DRAM access:
    - Video refresh 26.9k-byte DRAM—port or address mapped
    - Teletext/program 5.9k-byte DRAM—port or address mapped
    - Optional program 16k-byte DRAM extension—address mapped
  - Interleaving of MPU and CVDG DRAM access for uninterrupted read/write memory access without memory contention
  - On-chip refresh timing and control
- MPU Interface
  - Direct timing and cycle stealing for 1.4 MHz 68A09E MPU
  - Direct interface to R6512 CPU
- Teletext support
  - DMA interface and handshake to external NABTS teletext prefix processor
  - 5.72 Mbps effective data rate
  - 8k-byte teletext buffer DRAM interface

ORDERING INFORMATION

Part Number	Temperature Range
R6549 — Package: P = Plastic	0°C to 70°C

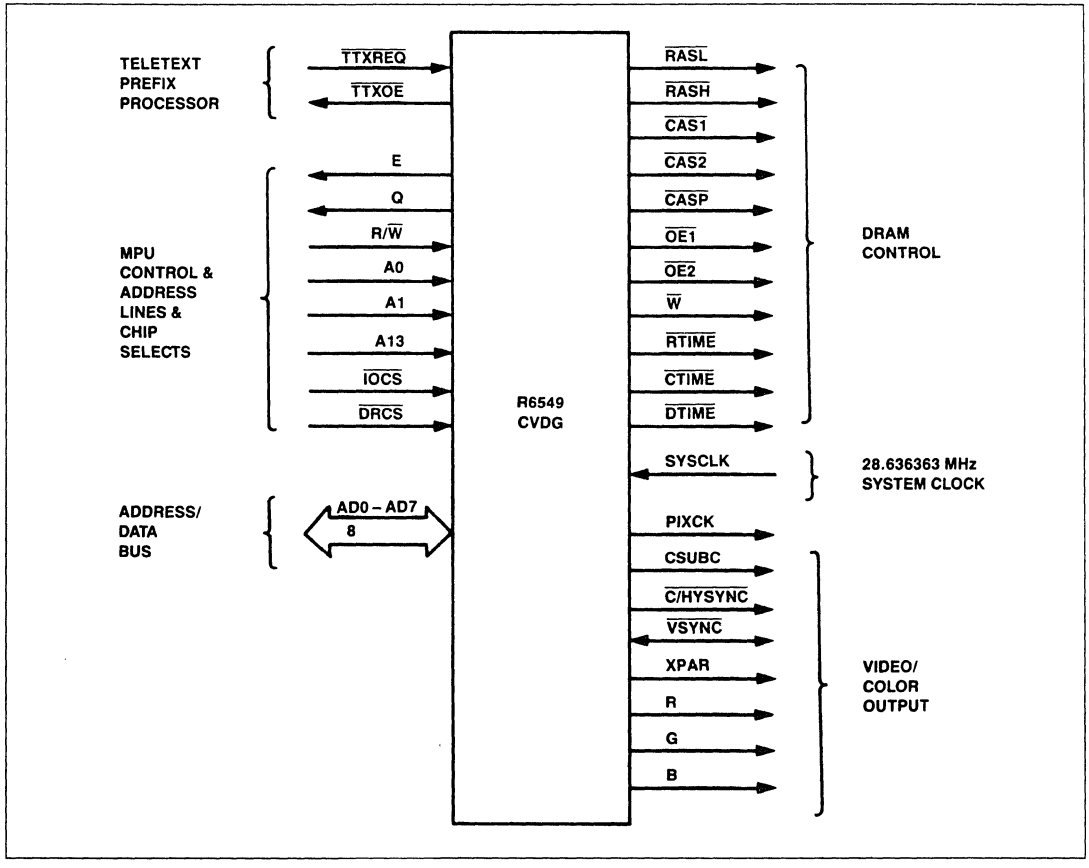


Figure 1. R6549 CVDG Interface Signals

PIN DESCRIPTION

Throughout this document signals are described logically using the terms active (or asserted) representing the true state, or inactive (or negated) representing the false state, regardless of whether the signal is active at a high or low voltage level.

The R6549 CVDG signals can be categorized into several different functional interfaces: MPU control and address bus, address/data (A/D) bus, DRAM control, color video output, teletext prefix processor and system clock input. Figure 1 identifies the signals within each group.

DMAC INTERFACE

$\overline{\text{TTXREQ}}$—Teletext DMA Request. An asynchronous falling edge-triggered request for direct memory access (DMA) transfer of data from a teletext prefix processor connected to the address/data (A/D) bus to DRAM. This TTL compatible input causes the CVDG to stop generating the E and Q clocks for one A/D bus cycle, output a 13-bit address (A0 – A12) to the DRAM during the processor portion of the A/D bus cycle, assert the $\overline{\text{TTXOE}}$ signal, and assert the $\overline{\text{W}}$ output to enable writing the data into DRAM.

$\overline{\text{TTXOE}}$—Teletext DMA Output Enable. An active LOW TTL compatible output pulse asserted within one A/D bus cycle after $\overline{\text{TTXREQ}}$ is asserted to acknowledge $\overline{\text{TTXREQ}}$ receipt and to enable data transfer from the teletext prefix processor onto the A/D bus (AD0 – AD7).

MPU CONTROL AND ADDRESS BUS

E—E Clock. A TTL compatible 1.43 MHz output clock that synchronizes data transfers over the MPU bus. This output drives the E clock input to the 6809E MPU. The E clock has special V_{OH} and V_{OL} output levels, V_{CC} – 0.5V and V_{SS} + 0.3V, respectively.

Q—Q Clock. A TTL compatible 1.43 MHz output clock that leads the E clock output for use by the 6809E.

R/$\overline{W}$—Read/Write. The TTL compatible Read/Write input controls the direction of data transfer between the MPU and the CVDG (HIGH = read from the CVDG; LOW = write to the CVDG). The R/$\overline{W}$ line should be connected to external data bus transceivers to also control the data direction between the MPU bus and the A/D bus.

A0, A1—MPU Address Line A0 and A1 Inputs. When $\overline{IOCS}$ is active, the encoded A0 and A1 inputs select the register in the CVDG to be accessed during a read or write operation (see Table 1). An exception is when A0 and A1 are both high during Mode 0, in which case DRAM is CDP accessed directly by the MPU at addresses generated by the CVDG.

When $\overline{DRCS}$ is active and program DRAM is selected (P = 1 in the DRAM Page Register), A0 is passed through the CVDG to drive the AD6 output during DRAM column address generation in the processor portion of the A/D bus cycle (see MPU DRAM Access Description).

A13—MPU Address Line A13 Input. When $\overline{DRCS}$ is active, A13 input HIGH causes program DRAM to be accessed ($\overline{CASP}$ asserted) during the processor portion of the A/D bus cycle independent of the P bit value in the DRAM Page Register. When program DRAM is selected in the DRAM Page Register (P = 1) or when A13 = 1, A13 is passed through the CVDG to drive the AD5 output during DRAM column address generation in the processor portion of the A/D bus cycle (see MPU DRAM Access Description).

$\overline{IOCS}$—I/O Chip Select. The active LOW, TTL compatible, $\overline{IOCS}$ input selects CVDG I/O port operation. The CVDG internal registers addressed by the A0 and A1 inputs are accessed as enabled by the mode selected in the Mode Register. Data direction is controlled by the R/$\overline{W}$ input as appropriate for each register and mode.

Table 1. CVDG Register Select Logic ($\overline{IOCS}$ = LOW)

A1	A0	Mode[1]	Read (R/$\overline{W}$ = H)	Write (R/$\overline{W}$ = L)
L	L	—	Status Register	Mode Register
L	H	0	X CDP Register	X CDP Register
H	L	0	Y CDP Register	Y CDP Register
H	H	0	DRAM[2]	DRAM[2]
H	H	1	—	LUT Address Register
H	H	2	LUT[3]	LUT Data Register
H	H	3	—	Switch Register
H	H	4	—	Y Scroll Register
H	L	5	TTX Pointer Register	TTX Pointer Register
H	H	6	—	DRAM Page Register

Notes:
1. The mode is selected in Mode Register.
2. DRAM is accessed directly by the MPU at DRAM addresses determined by the CVDG X CDP and Y CDP register contents.
3. The LUT is accessed as enabled and addressed in the LUT Address Register.

$\overline{DRCS}$—DRAM Chip Select. $\overline{DRCS}$ is a TTL compatible, active LOW, input that enables MPU access to the DRAM. $\overline{CTIME}$, $\overline{RTIME}$ and $\overline{DTIME}$ outputs are asserted by the CVDG at the proper times to enable external buffers which drive the MPU generated address onto the A/D bus and drive data between the MPU bus data lines and the A/D bus in the direction controlled by R/$\overline{W}$ (HIGH = read from DRAM; LOW = write to DRAM). Note that $\overline{DRCS}$ configurations are advanced and optional for many configurations.

ADDRESS/DATA BUS

AD0 – AD7—Address/Data Lines. Eight TTL compatible, bidirectional, multiplexed address/data lines (AD0 – AD7) interface the CVDG directly to the video/program DRAM, through external buffers to the MPU address bus (A1 – A12), and through external transceivers to the MPU data bus (D0 – D7). These lines transfer both address and data between the DRAM and the CVDG and between the MPU bus and the CVDG/DRAM during one 698 ns A/D bus cycle.

$\overline{RASL}$, $\overline{RASH}$—Row Address Strobe Low and High. TTL compatible outputs strobe the upper eight bits of the address on A/D bus lines AD0–AD7 into DRAM (as DRAM addresses A6–A13) on the falling edge. $\overline{RASL}$ strobes the address into the DRAM containing the lower four data bits (D0–D3) and $\overline{RASH}$ strobes the address into the DRAM containing the upper four data bits (D4–D7).

$\overline{CAS1}$, $\overline{CAS2}$, $\overline{CASP}$—Column Address Strobes 1, 2 and P. The TTL compatible CAS outputs strobe the six lower bits of the address on A/D bus lines (AD1–AD6) into DRAM (as DRAM addresses A0–A5) on the falling edge. $\overline{CAS1}$ and $\overline{CAS2}$ connect to the video DRAM containing the LUT addresses. Four 4-bit LUT addresses packed into two bytes are accessed during the video portion of each A/D bus cycle. $\overline{CAS1}$ strobes the DRAM containing the LUT addresses for the first two pixel positions while $\overline{CAS2}$ strobes the DRAM devices containing the LUT addresses for the second two pixel positions. $\overline{CASP}$ connects to the program DRAM containing the program instructions/data.

$\overline{OE1}$, $\overline{OE2}$—DRAM Output Enable. These active LOW, TTL compatible, outputs enable DRAM device data output lines during a read. $\overline{OE1}$ connects to the two video DRAM devices containing byte 1 (LUT addresses for pixels 1 and 2) and is asserted first during a video refresh cycle. $\overline{OE2}$ connects to the two DRAM devices containing byte 2 (LUT addresses for pixels 3 and 4) and is asserted following $\overline{OE1}$. $\overline{OE2}$ is also connected to the program DRAM devices and enables their data outputs during the processor portion of the A/D bus cycle.

$\overline{W}$—DRAM Write Enable. The TTL compatible, active LOW, $\overline{W}$ output strobes data from the A/D bus into DRAM during a write in the processor portion of the A/D bus cycle. $\overline{W}$ is held HIGH during a read from DRAM.

$\overline{RTIME}$—Row Address Time. The active LOW, TTL compatible, $\overline{RTIME}$ output enables DRAM row address lines from the MPU onto the A/D bus through external buffers when $\overline{DRCS}$ is active. (Required for $\overline{DRCS}$ configurations only.)

$\overline{CTIME}$—Column Address Time. The active LOW, TTL compatible, $\overline{CTIME}$ output enables DRAM column address lines from the MPU onto the A/D bus through external buffers when $\overline{DRCS}$ is active. (Required for $\overline{DRCS}$ configurations only.)

$\overline{\text{DTIME}}$—Data Time. The active LOW, TTL compatible, $\overline{\text{DTIME}}$ output enables data transfer between the MPU data bus and the A/D bus through external transceivers when $\overline{\text{DRCS}}$ or $\overline{\text{IOCS}}$ is active.

SYSTEM CLOCK

SYSCLK—System Clock. A clock input with a duty cycle of 40/60 to 50/50. The clock frequency should be 28.63636 MHz ±80 Hz for proper operation of the colorburst frequency. This input clock may be stopped in either state for up to 1 μs to allow for external digital phase lock techniques.

VIDEO/COLOR OUTPUTS

CSUBC—Color Subcarrier Clock Output. A TTL compatible 3.579545 MHz ± 10% color subcarrier clock. The clock rate complies with the North American Color Burst Clock Output Standard. The rate is the SYSCLK divided by eight and is phase keyed to the horizontal sync ($\overline{\text{HSYNC}}$) output on $\overline{\text{C/HSYNC}}$ (as either a component of $\overline{\text{CSYNC}}$ or pure $\overline{\text{HSYNC}}$). Vertical blanking interval (VBI) color gating by $\overline{\text{VSYNC}}$ must be done externally (since some modems require an uninterrupted 3.579 MHz clock).

When the color outputs are connected to an MC1377 color encoder, the CSUBC output can be connected to the MC1377 CLK input, typically through a 500 pF capacitor/150 μH inductor filter network.

$\overline{\text{C/HSYNC}}$—Composite/Horizontal Sync Output. Either a composite sync ($\overline{\text{CSYNC}}$) or a horizontal sync ($\overline{\text{HSYNC}}$) output at TTL levels, asserted "tips down", is selected by the External Sync (EXT) bit in the Switch Register.

In internal sync (EXT = 0), an RS-170 composite sync with full serration and equalization is output in either 2:1 or 1:1 interlace as selected by the 2:1 Interlace Select (S21) bit in the Switch Register (S21 = 1 for 2:1; S21 = 0 for 1:1).

In external sync (EXT = 1), a pure $\overline{\text{HSYNC}}$ is output in either normal or early timing as selected by the Normal Horizontal Sync (NHS) bit in the Switch Register. In normal timing (NHS = 1), a 15.7 kHz signal is output; in advance timing (NHS = 0), a 15.9 kHz stop clock signal is output.

When the color outputs are connected to an MC1377 color encoder, the $\overline{\text{C/HSYNC}}$ output can be connected directly to the MC1377 SYNC input pin.

$\overline{\text{VSYNC}}$—Vertical Sync Input/Output. A TTL compatible vertical sync ($\overline{\text{VSYNC}}$) input or output signal depending on the state of the External Sync (EXT) bit in the Switch Register (see Mode 3). $\overline{\text{VSYNC}}$ is an externally generated input at power up or when EXT = 1. $\overline{\text{VSYNC}}$ is an internally generated output when EXT = 0.

The $\overline{\text{VSYNC}}$ output can be used to disable the color subcarrier at the chroma modulator during VBI. Videotex decoders can also use $\overline{\text{VSYNC}}$ to interrupt the MPU at a 60 Hz rate for blink, task and timekeeping operations.

PIXCLK—Pixel Clock Output. A 5.7272 MHz pixel output clock running synchronously with the RGB color outputs.

R, G, B—Red, Green and Blue Color Outputs. Three separate color analog output voltages. Each output provides a 1.0 Vpp video signal at high impedance with a 1.8 Vdc offset. Each color level is controlled by a 4-bit color code accessed from the LUT for each pixel position. A digital-to-analog converter (DAC) converts the 4-bit code to one of 16 output voltage levels (black level = 1.875 Vdc; white level = 2.800 Vdc). The three outputs allow 4096 color level combinations. A composite blanking signal (1.800 Vdc) is included in each output.

The output signals include high frequency clock components which may require low pass filtering in some applications. The outputs can be connected to the R IN, G IN, and B IN inputs to a MC1377 color encoder through 15 μF (typical) AC coupling capacitors.

The color outputs, through external buffers, can also drive 75 ohm loads, e.g., the inputs to an RGB color monitor/TV.

XPAR—Transparent Output. A TTL compatible, active HIGH, output controlled by one bit in a 4-bit code (three bits are don't care) in the LUT. A LUT value of 1XXX in DRAM asserts XPAR (HIGH); LUT value of 0XXX in DRAM negates XPAR (LOW). This output can be used to indicate which video source to select. When XPAR output is HIGH, external video signals should be selected to display background video; when XPAR output is LOW, CVDG outputs should be selected to display graphics. The XPAR output is always HIGH during composite blanking to pass external vertical blanking interval (VBI) signals, external sync, color burst, etc.

POWER/GROUND

VCC—Primary Power. 5.0 Vdc.

VSS—Ground. Power and signal ground.

FUNCTIONAL DESCRIPTION

The R6549 CVDG operation is controlled by three free-running synchronous state machines with the following cycle rates:

Address/Data (A/D) Bus Cycle	698 ns/cycle (1.43 MHz)
Horizontal Raster Line Cycle	63.5 μs/cycle (15.74 kHz)*
Vertical Raster Frame Cycle	33.3 ms/cycle (30 Hz)

The CVDG also includes timing shift registers and sample flip-flops to generate internal and external timing signals; programmed logic arrays (PLAs) to perform I/O decoding, generate DRAM control signals and determine state machine outputs; registers to hold command/status and data; an internal 16-bit row/column bus in display X-Y coordinates; internal input and output 8-bit data busses; and input/output buffers to isolate internal circuits from external interfaces and to drive outputs. Figure 2 illustrates the main CVDG components.

*A 15.9 kHz stop-clock early sync is selectable.

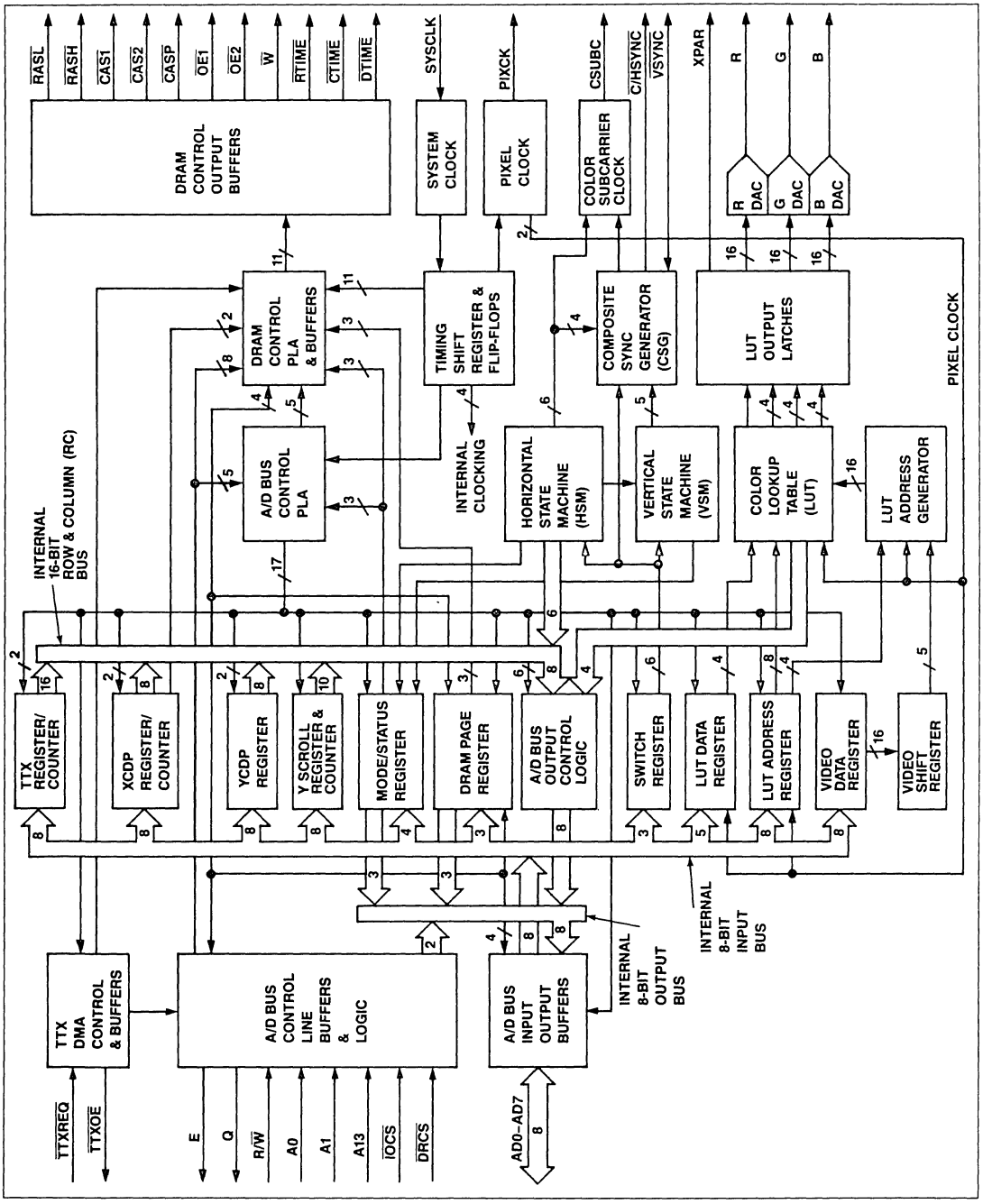


Figure 2. R6549 CVDG Block Diagram

SYSTEM TIMING

System Clock

Internal and output timing signals are derived from the 28.636363 MHz crystal frequency on the SYSCLK input pin. A two-phase non-overlapping 14.318181 MHz (SYSCLK/2) clock is generated to sequence high speed data transfer within the CVDG.

Timing Shift Register

The Timing Shift Register generates internal timing pulses as internal timing references at frequencies from 14.318 MHz down to 13.98 kHz. Flip-flops sample the various timing pulses to generate derivative timing reference signals for use by other CVDG circuits.

A two-phase non-overlapping 1.431818 MHz (SYSCLK/20) clock is generated for low speed sequencing within the CVDG and is also the external microprocessor bus and A/D bus timing reference. One phase of the 1.43 MHz clock drives the E clock output pin. A quadrature 1.431818 MHz clock leading the E clock is output on the Q output pin.

Pixel Clock

A 5.72 MHz pixel clock is output on the PIXCK output pin. Four pixel output clocks occur each 698 ns (one clock pulse coincident with each of the red, green and blue color level outputs and the transparent bit output for each pixel location).

VIDEO RASTER CONTROL

Horizontal Raster Line Cycle

An internal horizontal state machine (HSM) controls the horizontal raster line cycle. The HSM is incremented at the E clock rate, nominally every 698 ns. When normal horizontal sync timing is selected in the Switch Register (NHS = 1), 91 horizontal counts (HS0 – HS90), or states, comprise the 63.56 μs line raster. When early horizontal sync timing is selected (NHS = 0), typically to support external synchronization, 90 horizontal counts (HS0 – HS89) provide a 62.86 μs line raster. The first 64 counts clock the 256 displayed pixels (at four pixels per count). Figure 3 illustrates the horizontal and vertical raster count reference.

The HSM generates the horizontal raster timing pulses for internal logic and/or external output. These signals are the horizontal sync ($\overline{\text{HSYNC}}$), horizontal border and blanking, horizontal blanking, serration and equalization timing pulses.

The horizontal border and blanking pulse identifies the time that a border color is output (see LUT Data Register description) outside of the 256 pixel locations except during actual horizontal blanking. This signal is reported in bit 6 ($\overline{\text{HB}}$) of the Status Register.

An increment vertical count signal is also generated to increment the vertical state machine.

Vertical Raster Frame Cycle

An internal vertical state machine (VSM) controls the 33.3 ms vertical raster frame cycle. The VSM is incremented twice each horizontal raster line cycle. The VSM count (VS0 – VS523 or VS0 – VS524), or state, supports two frames per 30 ms vertical raster cycle. The upper count depends on the interlace mode (S21) switch position selected in the Switch Register. When 2:1 interlace mode is selected (S21 = 1), the upper VSM count supports a 262½ line frame. When 1:1 interlace is selected (S21 = 0), the upper VSM count supports a 262 line frame.

A VSM clear sign is normally generated when the VSM upper count is reached to restart the VSM at 0; however, when external sync is selected (EXT = 1) the VSM clear signal is generated from the external sync signal input on the $\overline{\text{VSYNC}}$ pin. Internal vertical state timing signals are generated for internal logic and/or external output. These signals include vertical sync ($\overline{\text{VSYNC}}$), vertical border and blanking, vertical blanking, and equalization enable pulses and the load Y scroll pointer time.

An internal vertical sync pulse, a vertical blanking pulse, and an equalization pulse are generated for combining with the $\overline{\text{HSYNC}}$ serration and equalization pulses when internal sync is selected (EXT = 0) to output composite sync on the $\overline{\text{C/HSYNC}}$ pin.

The vertical blanking pulse is also buffered and output on the $\overline{\text{VSYNC}}$ pin when internal sync is selected in the Switch Register (EXT = 0).

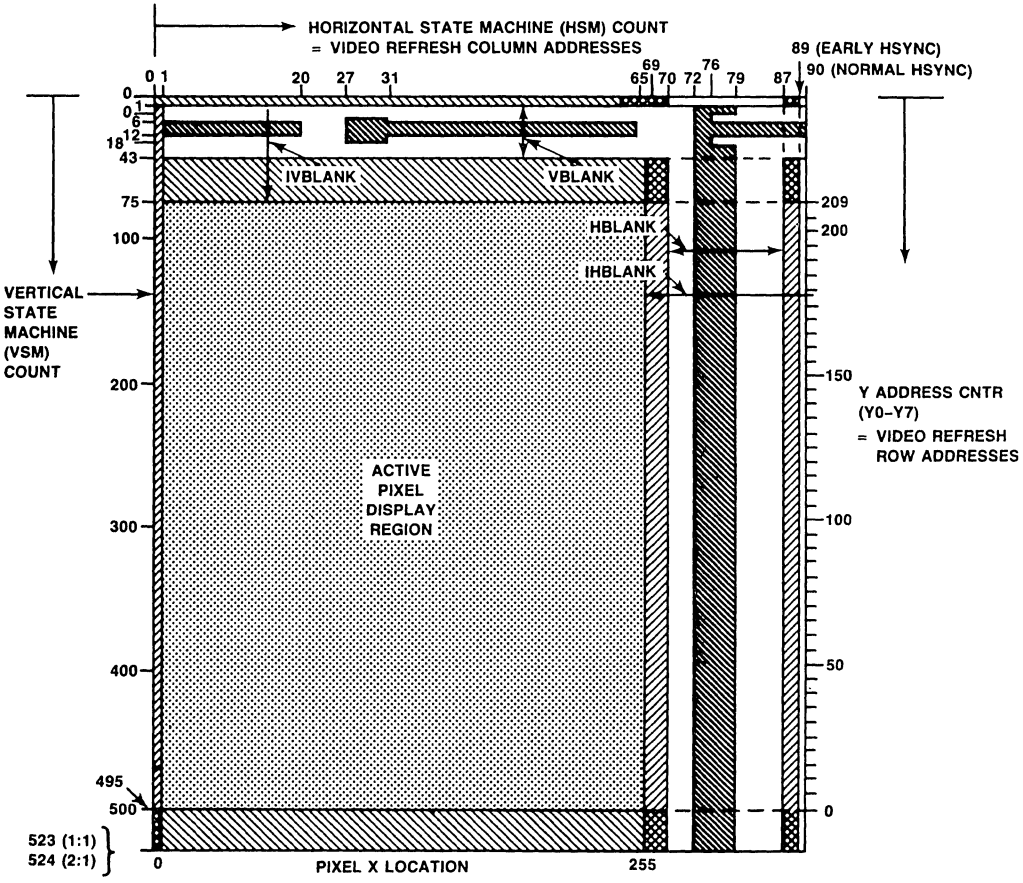
The internal vertical border and blanking pulse is generated and reported in bit 7 ($\overline{\text{VB}}$) of the Status Register. The pulse width is 3.302 ms for 2:1 interlace (S21 = 1) or 3.333 ms for 1:1 interlace (S21 = 0). This duration identifies the time the border color determined from the LUT Data Register is output, except during actual vertical blanking.

An internal load Y offset pointer signal is generated and routed to the Y Scroll Counter to cause the Y offset to load during the non-visible portion of the display raster.

Composite Sync and Color Subcarrier Clock Generation

$\overline{\text{HSYNC}}$ is output in one of two forms on the $\overline{\text{C/HSYNC}}$ pin depending upon the EXT bit state in the Switch Register. If internal sync is selected (EXT = 0), $\overline{\text{HSYNC}}$ is combined with horizontal blanking serration, equalization and vertical sync ($\overline{\text{VSYNC}}$) pulses to output as composite sync ($\overline{\text{CSYNC}}$). If external sync is selected (EXT = 1), the $\overline{\text{HSYNC}}$ signal is output on $\overline{\text{C/HSYNC}}$.

A 3.58 MHz color subcarrier clock (SYSCLK/8 and phase keyed to horizontal sync) is generated from composite sync and horizontal sync signals then is output on the CSUBC pin.



NOTES:
1. Vertical State Transition (HS28)
2. Vertical State Transition and $\overline{\text{HSYNC}}$ (HS73)
3. Symbol definitions:
   HBLANK = Horizontal Blanking
   IHBLANK = Horizontal Border and Blanking
   VBLANK = Vertical Blanking
   IVBLANK = Vertical Border and Blanking
   CBLANK = HBLANK + VBLANK = Composite Blanking
   ICBLANK = = IHBLANK + IVBLANK = Composite Borders and Blanking
4. Shading Legend:
   - Active Pixel Display Region
   - Right and Left Borders
   - Top and Bottom Borders
   - Blanking Region
   - Composite SYNC (CSYNC)

Figure 3. CVDG Video Raster Count Reference

ADDRESS/DATA BUS CONTROL

The Address/Data Bus state machine controls the operation of the 698 ns A/D bus cycle. The A/D bus cycle contains a 2-byte video data access cycle and a 1-byte I/O data access cycle (Figure 4). The addresses and data transferred on the A/D bus depend on the phase of the A/D bus cycle (i.e., the E clock level) and the type of operation in the I/O data access cycle. Table 2 identifies the source of the addresses for each type of DRAM access.

Video Data Access Cycle

The video data access cycle (also referred to as the video portion of the A/D bus cycle) occurs during the first half of the A/D bus cycle (when the E clock is LOW). Two bytes of video data (containing four LUT addresses corresponding to four pixel locations on the display) are read each cycle from DRAM at the DRAM address generated by the CVDG. The DRAM address is generated corresponding to the first of four pixel column locations in the horizontal raster and the pixel row location in the vertical raster. The video column (X) address of 0 to 64 is controlled by the horizontal state machine. The video row (Y) address of 209 to 0 is controlled by the Y Address Counter, which is in turn controlled by the vertical state machine and the Y Scroll Register. The two data bytes are loaded into the CVDG Video Data Register for subsequent serialization and LUT access (see the Pixel Color Generation description).

Up to 48k-bytes of Dynamic RAM (DRAM) can be connected to the A/D bus to store video data (LUT addresses) for video refresh, program instructions/data and received teletext data. The DRAM is segmented into six 8k-byte blocks with page selection of one block at a time during access (Figure 5). Four pages are required for video refresh (V00 – V11); three pages (V00, V01 and V10) hold video data exclusively, and one page (V11) holds video and program/teletext data. Two other pages hold program data. During the video data access cycle, and some modes of the I/O data access cycle, paging is handled automatically by the CVDG. The A13 and A0 input lines and the P, V1 and V0 bits in the CVDG DRAM Page Register select the page for MPU DRAM access during the I/O data access cycle (see MPU DRAM Access description).

I/O Data Access Cycle

The I/O data access cycle (also referred to as the processor portion of the A/D bus cycle) occurs during the second half of the A/D bus cycle (when E clock is HIGH). A/D bus address source and data source/destination depends upon CVDG chip select ($\overline{IOCS}$ and $\overline{DRCS}$) and Teletext Request ($\overline{TTXREQ}$) input levels, the selected CVDG mode, and the register select (A0 and A1) input levels. Refer to the description of each I/O access cycle function for details.

A/D Bus Control Line Buffers and Logic

The A/D Bus Control Line Buffers and Logic condition input and output A/D Bus control signals. Six input signals (R/$\overline{W}$, A0, A1, A13, $\overline{IOCS}$ and $\overline{DRCS}$) are buffered and routed to the DRAM Control PLA.

The E and Q output clocks are suppressed during a teletext DMA transfer. When $\overline{TTXREQ}$ input goes LOW, the Q and E clock outputs are held LOW to disable the clocks for one MPU bus cycle. In addition, the increment TTX address count goes HIGH to increment the modulo 32 TTX Counter. When $\overline{TTXREQ}$ goes HIGH at the completion of the DMA data transfer, the E and Q output clocks are enabled, the $\overline{TTXOE}$ output is negated (reset HIGH), and the increment TTX address count signal is reset.

Internal reset and initialization signals are generated when both $\overline{IOCS}$ and $\overline{DRCS}$ inputs are LOW for test purposes.

A/D Bus Control PLA

The A/D Bus Control PLA decodes CVDG and A/D Bus operation commands from buffered A/D bus control input signals and encoded mode bits in the Mode Register. Outputs from the PLA are buffered and routed to other circuits in the CVDG as internal enable signals.

A/D Bus Input/Output Buffers

The A/D Bus Input/Output Buffers isolate the internal CVDG data bus lines from the external A/D bus lines (AD0 – AD7). Input buffers continuously copy AD0 – AD7 onto the internal input data bus. Output buffers drive the states of the internal output data bus lines onto AD0 – AD7 when enabled by a CVDG output function and clocked by the 14.3 MHz internal clock. Two of these output buffers drive AD5 and AD6 during MPU DRAM access ($\overline{DRCS}$ = L) with the DRAM page signals, i.e., V0 and V1, respectively, or A13 and A0 inputs, respectively, depending on the state of the A13 input and the P bit in the DRAM Page Register.

A/D Bus Output Control Logic

The A/D Bus Output Control Logic drives data onto the internal output bus from the internal row and column bus lines, from the LUT, and from other internal CVDG circuits when enabled by outputs from the A/D Bus Control PLA.

DRAM Control PLA and Buffers

The DRAM Control PLA and Buffers generate and drive control and timing output signals to the DRAM; the row, column and data time output control signals for use by external line buffers and data line transceivers; and internal signals to control input/output data direction and to enable the internal row and column bus.

Timing pulses from the Timing Shift Registers; control signals from the Mode and Page registers, A/D Bus Control Buffers and Logic, and A/D Bus Control PLA; and control signals generated and derived from other sections of the CVDG are input to the PLA.

Output control states from the PLA are buffered and routed to external DRAM control signal pins ($\overline{RASL}$, $\overline{RASH}$, $\overline{CAS1}$, $\overline{CAS2}$, $\overline{CASP}$, $\overline{OE1}$, $\overline{OE2}$, and $\overline{W}$) and to external A/D bus control signal pins ($\overline{CTIME}$, $\overline{RTIME}$ and $\overline{DTIME}$). Other output signals are inverted and routed to internal logic.

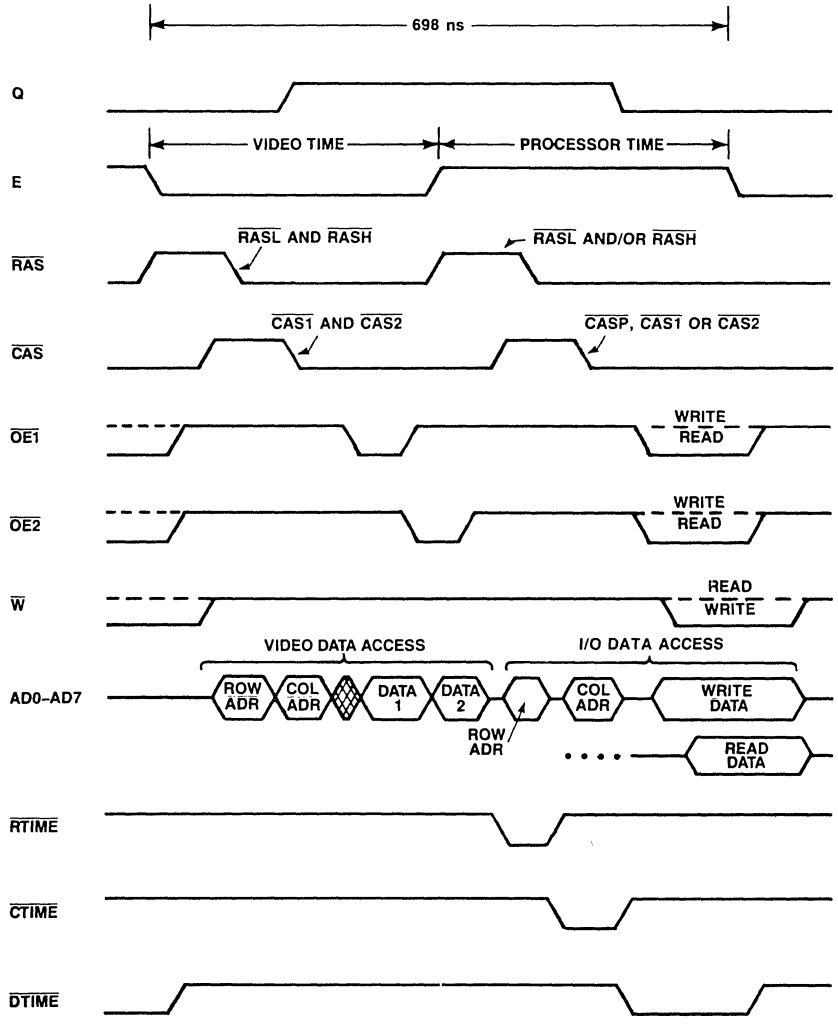


Figure 4. DRAM Address/Data (A/D) Bus Cycle

Table 2. Address/Data Bus Address Sources

DRAM Row/Column	—	CA5	CA4	CA3	CA2	CA1	CA0	—	RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0
CVDG Display Row/Column Bus	C7	C6	C5	C4	C3	C2	C1	C0	R7	R6	R5	R4	R3	R2	R1	R0
A/D Bus	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
Video Cycle[1]	0	V7	V6	V5	V4	V3	V2	0	V1	V0	H6	H5	H4	H3	H2	H1
Processor Cycle CDP Graphics[2] ($\overline{IOCS}$ = L, Mode 0)	X1[3]	Y7	Y6	Y5	Y4	Y3	Y2	X0[4]	Y1	Y0	X7	X6	X5	X4	X3	X2
MPU Video DRAM Access[5] ($\overline{DRCS}$ = L, P = 0)	A0[6]	V1[7]	V0[2]	A12	A11	A10	A9	0	A8	A7	A6	A5	A4	A3	A2	A1
MPU Program DRAM Access[8] ($\overline{DRCS}$ = L, P = 1)	0	A0[9]	A13[9]	A12	A11	A10	A9	0	A8	A7	A6	A5	A4	A3	A2	A1
Teletext DMA Access[10] ($\overline{TTXREQ}$ = L)	T0	1[11]	1[11]	T12	T11	T10	T9	0	T8	T7	T6	T5	T4	T3	T2	T1

Notes:

1. Video Cycle:
   H1 – H6 = HSM Output = 0 to 64 (= 0 to 255 pixel LUT addresses @ 4 addresses per access);
   V0 – V7 = Y Scroll Counter Output = 209 to 0
2. CDP Graphics:
   X0 – X7 = X CDP Register/Counter contents = 0 to 255;
   Y0 – Y7 = Y CDP Register contents = 0 to 255 (0 to 209 for displayable data)
3. X1 controls the $\overline{CAS1}$ and $\overline{CAS2}$ outputs:
   0 = Assert $\overline{CAS1}$
   1 = Assert $\overline{CAS2}$
4. X0 controls the $\overline{RASL}$ and $\overline{RASH}$ outputs:
   0 = Assert $\overline{RASL}$
   1 = Assert $\overline{RASH}$
5. MPU Video DRAM Access: A0 – A12 = MPU Address = 0 to 4096.
6. A0 input controls the $\overline{CAS1}$ and $\overline{CAS2}$ outputs:
   L = Assert $\overline{CAS1}$
   H = Assert $\overline{CAS2}$
7. V0 and V1 bits in the DRAM Page Register control assertion of AD6 and AD5 outputs, respectively:
   0 = Negate output
   1 = Assert output
8. MPU Program DRAM Access: A0 – A13 = MPU Address = 0 to 8192
9. A0 and A13 inputs control the AD6 and AD5 outputs, respectively:
   L = Negate output
   H = Assert output
10. Teletext Access:
    T1 – T4 = Modulo 32 counter incremented by each DMA byte transfer
    T5 – T12 = Teletext Pointer Register contents incremented by T1 – T4 overflow
11. AD6 and AD5 asserted to select program DRAM.

DRAM Page Register				Addr (Hex)	Addr (Dec)	Memory Page	Memory Function
A13	P	V1	V0				
				1FFF	8191		
1	1	X	X			Program 1 (A13 = 1)	
				0	0		PROGRAM
				1FFF	8191		
0	1	X	X			Program 0 (A13 = 0)	
				0	0		
				1FFF	8191		PROGRAM/ TELETEXT
0	0	1	1			Video 3 (V11)	
				0900	2304		
				08FF	2303	0,209 | 1,209	Note 2
				0	0		
				1FFF	8191		
0	0	1	0			Video 2 (V10)	
				0	0		
				1FFF	8191		VIDEO[1] DATA
0	0	0	1			Video 1 (V01)	
				0	0		
				1FFF	8191		
0	0	0	0			Video 0 (V00)	
				0	0	254,0 | 255,0	Note 2

Notes:

1. 26,880 bytes of video memory are required to support video refresh, i.e., to supply 53,760 4-bit LUT addresses in support of the 210 x 256 pixel display area. With 32,768 bytes supplied in four 4416 DRAM devices, 5888 bytes are available for general program/TTX message use in the upper part of video memory page 3 (V11).
2. Nibbles shown correspond to beginning and ending data for 210 x 256 pixel display area in X(column), Y(row) coordinates.

Figure 5. DRAM Memory Map

PIXEL COLOR GENERATION

LUT Address Generation

The 16-bit Video Data Register latches the four LUT addresses contained in the two data bytes acquired during the video data access cycle. Two 4-bit color lookup table (LUT) addresses are packed into each byte. The Video Shift Register serializes the four LUT addresses and transfers them one byte at a time to the LUT Address Generator. The LUT Address Generator latches the 4-bit coded LUT addresses from the Video Shift Register, converts the coded address to 16 binary signals and latches the binary address (0 – 15) for routing to the LUT.

LUT Operation

The color look-up table (LUT) is a 16 × 13 bit memory holding 16 entries of R, G and B color codes and corresponding transparent state (see Table 3). Each entry holds three 4-bit encoded color levels (0000 = lowest voltage level, 1111 = highest voltage level) and a 1-bit transparent state (0 = off, 1 = on). For each pixel location the three color level codes (R, G and B) are sampled from the LUT, latched and routed through three separate digital-to-analog converters. The transparent bit corresponding to each pixel location is also accessed from the LUT, latched, buffered and output on the $\overline{\text{XPAR}}$ pin.

Digital-To-Analog Conversion (DACs)

The 4-bit color code for each color (R, G and B) at a pixel position is converted to a corresponding analog voltage through a 16-level digital-to-analog converter (DAC). Four lines from the four color code lines and their four complements are decoded to one of 16 levels, sampled and latched. The latched outputs are in turn connected to the color output pin (R, G and B) through a voltage divider ladder network.

Table 3. LUT Structure

LUT ADDR	LUT FORMAT																
	XPAR[1]				GREEN[2]				BLUE[2]				RED[2]				
(HEX)	3	2	1	0	3	2	1	0	3	2	1	0	3	2	1	0	
F																	
E																	
D																	
C	0				0	0	0	0	0	1	0	0	0	1	1	1	Example 1[3]
B																	
A		NO															
9	1	ACTUAL			1	0	0	0	1	1	0	0	1	1	1	1	Example 2[4]
8		DATA															
7																	
6																	
5																	
4																	
3																	
2																	
1																	
0																	

Notes:

1. XPAR is a single bit in the LUT; the format shown corresponds to the LUT Data Register format:
   0XXX = XPAR output LOW
   1XXX = XPAR output HIGH

2. Color Data Level:
   0000 = lowest output voltage = 1.875 Vdc
   1111 = highest output voltage = 2.800 Vdc

3. Example 1—LUT Address C Data:
   XPAR output = LOW
   G output = 1.875 + 0 (0.0617) = 1.875 Vdc
   B output = 1.875 + 4 (0.0617) = 2.122 Vdc
   R output = 1.875 + 7 (0.0617) = 2.307 Vdc

4. Example 2—LUT Address 9 Data:
   XPAR output = HIGH
   G output = 1.875 + 8 (0.0617) = 2.369 Vdc
   B output = 1.875 + 12 (0.0617) = 2.615 Vdc
   R output = 1.875 + 15 (0.0617) = 2.800 Vdc

I/O DATA ACCESS CYCLE FUNCTIONS

The I/O access cycle operates in one of five ways:

1. CVDG Mode/Status Register Access (enabled by $\overline{IOCS}$ LOW)
2. CVDG Graphics Access (enabled by $\overline{IOCS}$ LOW)
3. CVDG Parameter I/O Access (enabled by $\overline{IOCS}$ LOW)
4. MPU DRAM I/O Access (enabled by $\overline{DRCS}$ LOW)
5. Teletext Byte DMA (enabled by $\overline{TTXREQ}$ LOW)

The basic type of I/O access cycle is determined by the chip select ($\overline{IOCS}$ or $\overline{DRCS}$) and Teletext Request ($\overline{TTXREQ}$) inputs. When neither of the chip select inputs are LOW, nor has a TTX DMA transfer been initiated by $\overline{TTXREQ}$ LOW, the I/O access cycle is idle with no data transfer occurring during the processor portion of the A/D bus cycle.

When $\overline{IOCS}$ is LOW, the register address inputs (A0 and A1) and the mode selected in the CVDG Mode Register define the specific CVDG I/O operation, i.e., Mode/Status Register Access, CVDG Graphics Access (Mode 0), or one of the six CVDG Parameter Access modes (Modes 1-6). Table 4 shows the CVDG registers accessible during the I/O access cycle and the bit assignments. When A1 and A0 are both HIGH, the register bits are defined with reference to a pseudo Data Register (DR). The actual internal CVDG register accessed depends on the selected mode (see Table 4). The bits are defined in the following text.

CVDG Mode/Status Register Access

When $\overline{IOCS}$ is LOW and the register address is zero (A0 and A1 inputs are both LOW), the Mode Register (MR) or the Status Register (SR) is accessed depending upon the R/$\overline{W}$ input level. When R/$\overline{W}$ is LOW, the Mode Register is written; when R/$\overline{W}$ is HIGH, the Status Register is read.

Table 4. CVDG Register Summary

Internal CVDG Register	Mode	Register Select Lines A1	Register Select Lines A0	R/W[4]	Register Bit No. 7	6	5	4	3	2	1	0	Reset[3]
Mode Register	—	0	0	W	—	—	—	—	S	M2	M1	M0	0F
Status Register	—	0	0	R	$\overline{VB}$	$\overline{HB}$	M2	M1	M0	P	V1	V0	— —
X CDP Register	0	0	1	R/W	X7	X6	X5	X4	X3	X2	X1	X0	00
Y CDP Register	0	1	0	R/W	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0	00
DRAM[1]	0	1	1	R/W	P3	P2	P1	P0	Q3	Q2	Q1	Q0	— —
LUT Address Register	1	1	1	W	XPE	RE	GE	BE	A3	A2	A1	A0	00
LUT[2]	2	1	1	R	—	—	—	—	D3	D2	D1	D0	— —
LUT Data Register	2	1	1	W	—	—	—	—	D3	D2	D1	D0	— —
Switch Register	3	1	1	W	NHS	S21	EXT	LS	TST	—	—	—	F8
Y Scroll Register	4	1	1	W	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0	00
TTX Pointer Register	5	1	0	R/W	A12	A11	A10	A9	A8	A7	A6	A5	00
DRAM Page Register	6	1	1	W	—	—	—	—	—	P	V1	V0	07

Notes:
1. The DRAM is directly accessed and not the CVDG.
2. Data is transferred from the LUT onto the A/D bus without going through the LUT Data Register.
3. Reset state upon power up.
4. R/W = Read/write (R = read only; W = write only; R/W = read or write).

Mode Register

The write-only Mode Register selects the CVDG mode for next read from, or write to, the CVDG. In addition, the Mode Register contains a submode flag applicable only to Mode 0. The Mode Register may be written at any time regardless of the current CVDG mode. The mode and submode bits are initialized to ones upon power up.

				Bit Position							
Register	A1	A0	R/W	7	6	5	4	3	2	1	0
Mode	0	0	W	—	—	—	—	S	M2	M1	M0

MR7–MR4 Not used (no effect)

MR3 CDP Submode Flag (S) — (Mode 0 only—see Mode 0 description)

0 Enable CDP Nibble Submode. Allows read/write of a single 4-bit pixel nibble in a byte.

1 Enable CDP Byte Submode. Allows read/write of two 4-bit pixel nibbles in a byte with automatic increment of the X CDP for faster storage of LUT addresses in DRAM.

MR2–MR0 CVDG Mode (M2–M0)

(M2)	(M1)	(M0)	
0	0	0	Mode 0 — Port CDP Graphics
0	0	1	Mode 1 — LUT Address
0	1	0	Mode 2 — LUT Data
0	1	1	Mode 3 — Switch Register
1	0	0	Mode 4 — Y Scroll Offset Register
1	0	1	Mode 5 — Teletext DMA Pointer
1	1	0	Mode 6 — Set DRAM Page
1	1	1	Not used — no effect

Note that the mode must be written into the Mode Register before the desired mode can be executed.

Status Register

The read-only Status Register reports the selected CVDG mode, the selected DRAM page and the status of the horizontal and vertical raster blanking signals. The Status Register may be read at anytime regardless of the CVDG mode.

The horizontal blanking ($\overline{HB}$) and vertical blanking ($\overline{VB}$) signals report the state of the video raster at the time of access. The states of these two signals can be used for 15 kHz poll-driven timing, vertical blanking interval (VBI) identification, LUT loading, etc. These blanking times reflect the non-pixel display time including the time actual horizontal and vertical blanking signals are generated (for inclusion in composite sync output).

				Bit Position							
Register	A1	A0	R/W	7	6	5	4	3	2	1	0
Status	0	0	R	$\overline{VB}$	$\overline{HB}$	M2	M1	M0	P	V1	V0

SR7 Vertical Blanking ($\overline{VB}$)

0 Vertical blanking is asserted.

1 Vertical blanking is not asserted.

SR6 Horizontal Blanking ($\overline{HB}$)

0 Horizontal blanking is asserted.

1 Horizontal blanking is not asserted.

SR5–SR3 Mode Selected (M2–M0)

Reports the current CVDG mode as selected in bits 2–0 of the Mode Register.

SR5 (M2)	SR4 (M1)	SR3 (M0)	
0	0	0	Mode 0 — Port CDP Graphics
0	0	1	Mode 1 — LUT Address
0	1	0	Mode 2 — LUT Data
0	1	1	Mode 3 — Switch Register
1	0	0	Mode 4 — Y Scroll Offset Register
1	0	1	Mode 5 — Teletext DMA Pointer
1	1	0	Mode 6 — DRAM Page
1	1	1	Not used — no effect

SR2–SR0 DRAM Page Selected (P, V1, V0)

Reports the current DRAM Page selected in bits 2–0 of the Page Register (see Mode 6 — Write DRAM Page). P is the program RAM page indicator. V0 and V1 are the video page indicators.

SR2 (P)	SR1 (V1)	SR0 (V0)	Selected DRAM Page
0	0	0	Video Page 0: 8k-byte video RAM
0	0	1	Video Page 1: 8k-byte video RAM
0	1	0	Video Page 2: 8k-byte video RAM
0	1	1	Video Page 3: 2.3k-byte video RAM; 5.9k-byte program RAM
1	0	0	Program Page: 16k-byte optional program RAM accessed via $\overline{DRCS}$ (additionally paged by A13 and A0 inputs)

Mode 0 — Port CDP Graphics

When $\overline{IOCS}$ is LOW and Mode 0 is selected in the Mode Register, the Port Current Drawing Pointer (CDP) Mode is active. In this mode display column and row addresses can be written to the CVDG Current Drawing Pointer (CDP) X and Y registers, respectively, and pixel data accessed in DRAM. This mode is primarily used to update LUT addresses (i.e., the CDPs) in the video pages of DRAM. These LUT addresses are the video data read from the DRAM by the CVDG during the video portion of the A/D bus cycle.

This mode can be used to write or read data in any of the four 8k-byte video pages of DRAM defined by the V0 and V1 bits in the CVDG DRAM Page Register. The first three pages (V00, V01 and V10) are used exclusively for video data. 2304 bytes (addresses 0–8FF) of the fourth page (V11) are used for video data while the rest of the DRAM can be used for program or teletext message storage.

In mode 0, the MPU writes the address of the data in display coordinates into the CVDG X CDP and Y CDP registers. The X CDP contains the pixel position in the horizontal axis (i.e., the display column number) and varies from 0 to 255 (hex FF). Each pixel data nibble corresponds to a location (0 to 15) in the color look-up table (LUT) from which the corresponding R, G and B color levels and transparent bit data are retrieved for color generation. The Y CDP contains the pixel position in the vertical axis (i.e., the display row number) and varies from 0 to 255 (hex FF). Only values of 0 to 209 are used by the CVDG during the video portion of the A/D bus cycle to access video data. Y addresses 210–255 identify DRAM address on video DRAM page V11 that can contain non-displayable data, i.e., program or teletext data.

The registers accessible (besides in Mode and Status registers) in this mode are:

				Bit Position							
Register	A1	A0	R/W	7	6	5	4	3	2	1	0
X CDP	0	1	R/W	X7	X6	X5	X4	X3	X2	X1	X0
Y CDP	1	0	R/W	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0
DRAM*	1	1	R/W	P3	P2	P1	P0	Q3	Q2	Q1	Q0
*Not CVDG Access											

The X CDP Register is accessed at register address 1 (A1 = 0 and A0 = 1) and the Y CDP Register is accessed at register address 2 (A1 = 1 and A0 = 0). When register address 3 (A1 = 1 and A0 = 1) is detected, the CVDG generates DRAM row and column addresses corresponding to the display coordinates loaded in the X CDP and Y CDP registers. Data is then written from the A/D bus to the DRAM (R/$\overline{W}$ = low) or read from the DRAM to the A/D bus (R/$\overline{W}$ = high).

There are two submodes in Mode 0 that allow accessing of DRAM data at either the nibble (4-bit) or byte (8-bit) level. The submode is selected by the S bit (bit 3) in the Mode Register:

S = 0 CDP Nibble Submode
S = 1 CDP Byte Submode

CDP Nibble Submode

The CDP Nibble Submode (S = 0) reads or writes DRAM data one nibble at a time. Eight bits of data corresponding to two 4-bit LUT addresses (P3–P0 and Q3–Q0) are on the A/D data bus, but only one nibble is read or written during each access.

When writing the data, the Q nibble should contain the same pixel data as the P nibble. Only one of the nibble values is strobed into DRAM according to the X0 value in the X CDP Register which enables the $\overline{RASL}$ or $\overline{RASH}$ signal to DRAM during the write. If X0 = 0, the Q nibble (data bits 3–0) is written into the DRAM (row address strobed by $\overline{RASL}$); if X0 = 1, the P nibble (data bits 7–4) is written into the DRAM (row address strobed by $\overline{RASH}$).

When reading the data, only one nibble is read depending on the state of X0 in the X CDP. If X0 = 0, the Q nibble is read (row address strobed by $\overline{RASL}$); if X0 = 1, the P nibble is read (row address strobed by $\overline{RASH}$).

Reading or writing the data in this submode has no effect on the X CDP or Y CDP register values.

CDP Byte Access Submode

The CDP Byte Submode (S = 1) reads or writes two 4-bit LUT addresses at a time (in one byte) with an automatic increment of the X CDP value in the X CDP Register during write. Each write of the DRAM data writes the eight data bits on AD0–AD7 into DRAM and increments the X CDP by two upon the completion of the write cycle. (The new X CDP count can be read from the X CDP Register at any time.) As writing of the data continues, the X CDP value eventually wraps around to zero and continues incrementing. The Y CDP Register value must be incremented by writing a new Y CDP value. The automatic increment of X CDP value allows fast horizontal drawing for filling of polygon and rectangle type shapes (i.e., no intervening X CDP update is required). Note that the filled boundaries must be addressed by the horizontal line software since the X0 value has no effect in this submode.

This feature is useful for fast non-modulo 210 Y scrolling with quick reads/writes interleaved by old/new Y address updates. Note that when S = 1 in the Mode Register, the X0 value has no effect (the P nibble corresponds to X0 = 1 and the Q nibble corresponds to X0 = 0).

Reading of the DRAM data in this submode does not effect the X CDP count.

CVDG PARAMETER I/O ACCESS

Six CVDG Parameter Access modes allow the MPU to load control parameters into CVDG internal registers. Two of the modes also allow the MPU to read the parameter values from registers. The exact mode and access is controlled by the selected mode in the Mode Register and the register select input lines (A1 and A0).

Mode 1 — LUT Address

In Mode 1, data written to register address 3 (A1 = 1 and A0 = 1) is loaded into the LUT Address Register. Four bits control LUT write and read and the other four bits contain the actual LUT address. Bits 7–4 (XPE, RE, GE and BE) enable writing into, or reading from, corresponding sections of the LUT (i.e., XPAR, R, G and B) during Mode 2 access. Bits 3–0 in the register contain the LUT address (0–15) accessed during Mode 2.

				Bit Position							
Register	A1	A0	R/W	7	6	5	4	3	2	1	0
LUT Address	1	1	W	XPE	RE	GE	BE	A3	A2	A1	A0

DR7 Transparent Enable (XPE)

0 Disable XPAR write or read
1 Enable XPAR write or read

DR6 Red Enable (RE)

0 Disable R write or read
1 Enable R write or read

DR5 Green Enable (GE)

0 Disable G write or read
1 Enable G write or read

DR4 Blue Enable (BE)

0 Disable B write or read
1 Enable B write or read

DR3-DR0 LUT Address (A3-A0)

DR3 (A3)	DR2 (A2)	DR1 (A1)	DR0 (A0)	
0	0	0	0	LUT address 0
0	0	0	1	LUT address 1
	.	.	.	
1	1	1	1	LUT address 15

The LUT address in the LUT Address Register, rather than the LUT addresses read from DRAM, is also used to lookup the color level code in the LUT during the active display time (border and/or pixel) in two circumstances:

1. Outside the 256 x 210 graphics area, i.e., to generate the border color. Note that programs loading the LUT during the vertical blanking interval (VBI) must restore the address of the border color in the LUT into the LUT Address Register prior to unblanking.
2. Within the 256 x 210 graphics area when the LS bit = 0 in the Switch Register.

Mode 2 — LUT Data

In Mode 2, LUT data (i.e., color levels and transparent state) written to, or read from, register address 3 (A1 = 1, A0 = 1) is loaded into, or read from the LUT at the LUT address contained in the LUT Address Register. Only the section (R, G, B and/or XPAR codes) of the LUT entry enabled by bits 7-4 in the LUT Address Register are accessed. Normally only one enable bit at a time is set to a 1. During a write, data will be written into each LUT section enabled. During a read, ambiguous data will be accessed if more than one enable bit is set.

The transparent state (XPAR) is only one bit (D3). The other three data bits (D2-D0) are don't care.

During a write, the data on the A/D bus is written into the CVDG LUT Data Register. The LUT Address Generator latches the 4-bit LUT address from the LUT Data Register rather than from the Video Shift Register. The LUT Address Generator then generates the 16-bit binary address for routing to the LUT. The LUT is loaded in a similar manner as described for pixel color generation.

During a read, data is transferred from the LUT directly to the A/D bus without going through the LUT Data Register. XPAR is not availabe for readback.

				Bit Position							
Register	A1	A0	R/W	7	6	5	4	3	2	1	0
LUT Data*	1	1	R/W	—	—	—	—	D3	D2	D1	D0

*During a read, data is transferred directly from LUT to A/D bus without going through LUT Data Register.

DR7-DR4 Not used (no effect)

DR3-DR0 Color Level Code or Transparent Bit State

D3	D2	D1	D0	R, G or B Color Output Level
0	0	0	0	Color output level 0
0	0	0	1	Color output level 1
		.		.
1	1	1		Color output level 15
D3	**D2**	**D1**	**D0**	**XPAR Output Level**
0	X	X	X	XPAR output LOW
1	X	X	X	XPAR output HIGH (X = no effect)

Mode 3 — Switch Register

In Mode 3, switch position data (represented by bit states) written to register address 3 (A1 = 1, A0 = 1) is loaded into the CVDG Switch Register. Three bits control video raster operation, one bit controls the LUT address access source, and one bit enables the CVDG test mode. All five bits are set to a 1 by power up.

				Bit Position							
Register	A1	A0	R/W	7	6	5	4	3	2	1	0
Switch	1	1	W	NHS	S21	EXT	LS	TST	—	—	—

DR7 Normal Horizontal Sync (NHS) Select

0 Early 15.9 kHz ($\overline{\text{HSYNC}}$) Output
1 Normal 15.7 kHz $\overline{\text{HSYNC}}$ Output

DR6 2:1 Interlace Select (S21)

0 1:1 interlace
1 2:1 interlace

DR5 External Sync Select (EXT)

0 Internal sync output on $\overline{\text{VSYNC}}$ ($\overline{\text{C/HSYNC}}$ output enabled.
1 External sync input on $\overline{\text{VSYNC}}$ ($\overline{\text{C/HSYNC}}$ output disabled)

DR4 LUT Address Select (LS)

0 Select the LUT Address Register as the LUT address source
1 Select Video Shift Register data as LUT address source

DR3 Test Mode Select (TST)

0 Normal mode; Vertical state machine (VSM) and Y address counter (YAC) run at normal rate
1 Test mode; VSM and YAC run at 1.413 MHz (used for factory test only)

Mode 4 — Y Scroll Register

In Mode 4, a Y scroll offset value written to register address 3 (A1 = 1, A0 = 1) is loaded into the Y Scroll Register. The Y scroll offset may vary from 0 to 209 (decimal). The value written defines the first horizontal row to be displayed at the top of the 256 x 210 graphics image area.

				Bit Position							
Register	A1	A0	R/W	7	6	5	4	3	2	1	0
Y Scroll	1	1	W	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0

DR7–DR0 Y Scroll Offset

0000000 Offset = 0
0000001 Offset = 1
. .
. .
. .
11010001 Offset = 209 (maximum allowed)

Mode 5 — Teletext DMA Pointer

In Mode 5, an 8-bit Teletext pointer written to register address 2 (A1 = 1, A0 = 0) is loaded into the TTX Pointer Register and Counter. The pointer, consisting of address bits A12–A5 specifies the starting address on a 32-byte boundary for the DMA transfer of teletext data into video page 3 of DRAM. During a teletext DMA data transfer, the Modulo 32 Teletext Counter is incremented by one upon each DMA byte transfer. The TTX Pointer Register is incremented by one every 32 bytes. The value of the Teletext Pointer can be read at any time in Mode 5.

				Bit Position							
Register	A1	A0	R/W	7	6	5	4	3	2	1	0
Teletext Pointer	1	0	R/W	A12	A11	A10	A9	A8	A7	A6	A5

The status of the P, V1 and V0 in the Mode/Status Register are unchanged during a Teletext DMA data transfer.

Mode 6 — Set DRAM Page

In Mode 6, data written to register address 3 (A1 = 1, A0 = 1) is loaded into the DRAM Page Register. The data contains a 3-bit DRAM page select code and five unused bits (don't care). These DRAM page select bits specify the 8k-byte DRAM page accessed during a MPU DRAM access ($\overline{DRCS}$ = low) when A13 input is LOW. The DRAM page bits can be read from the Status Register at any time.

				Bit Position							
Register	A1	A0	R/W	7	6	5	4	3	2	1	0
DRAM Page	1	1	W	—	—	—	—	—	P	V1	V0

DR7–DR3 Not Used (no effect)

DR2–DR0 Selected DRAM Page

DR2 (P)	DR1 (V1)	DR0 (V0)	
0	0	0	Video Page 0: 8k-byte video RAM
0	0	1	Video Page 1: 8k-byte video RAM
0	1	0	Video Page 2: 8k-byte video RAM
0	1	1	Video Page 3: 2.3k-byte video RAM; 5.9k-byte program RAM
1	0	0	Program Page 0: 16k-byte optional program RAM accessed via $\overline{DRCS}$ (additionally paged by A13 and A0 inputs)

MPU DRAM I/O ACCESS

When $\overline{DRCS}$ is LOW, the MPU directly accesses the DRAM in an address map manner. The MPU generates the DRAM row and column addresses (except for two column address lines which are driven by the CVDG). The CVDG drives the AD5 and AD6 lines during DRAM column address time and also outputs control signals ($\overline{RTIME}$, $\overline{CTIME}$ and $\overline{DTIME}$) to enable external A/D bus buffers. MPU address line A1–A8 are enabled onto A/D bus lines AD0–AD7, respectively, by $\overline{RTIME}$ to drive the DRAM row address. MPU address line A9–A12 are enabled onto A/D bus lines AD1–AD4, respectively, by $\overline{CTIME}$ to drive the DRAM column address. The CVDG drives AD5 and AD6 with one of two sets of signals during $\overline{CTIME}$. External bidirectional data line buffers are enabled by $\overline{DTIME}$ in the direction controlled by the MPU R/$\overline{W}$ output to transfer data between the MPU data bus lines D0–D7 and A/D bus lines AD0–AD7.

A13 input high causes program DRAM to be accessed during the processor portion of the A/D bus independent of the P bit value in the DRAM Page Register. $\overline{CASP}$ is asserted in response to the A13 HIGH to strobe the column address lines into program DRAM.

When A13 input is LOW, the section of DRAM accessed depends on the P bit value in the DRAM Page Register and the A0 input. If P = 0, video DRAM is accessed; $\overline{CAS1}$ is generated when A0 is LOW and $\overline{CAS2}$ is generated when A0 is HIGH. If P = 1, program DRAM is accessed since $\overline{CASP}$ is generated instead of $\overline{CAS1}$ or $\overline{CAS2}$ to strobe the DRAM column address.

The AD5 and AD6 outputs are driven by the CVDG during DRAM column address generation in the processor portion of the A/D bus cycle as controlled by the P bit in the DRAM Page Register. If video DRAM is selected (P = 0), the V0 and V1 bits in the DRAM Page Register are output on AD5 and AD6, respectively. If program DRAM is selected (P = 1), the A0 and A13 inputs are output on AD5 and AD6, respectively.

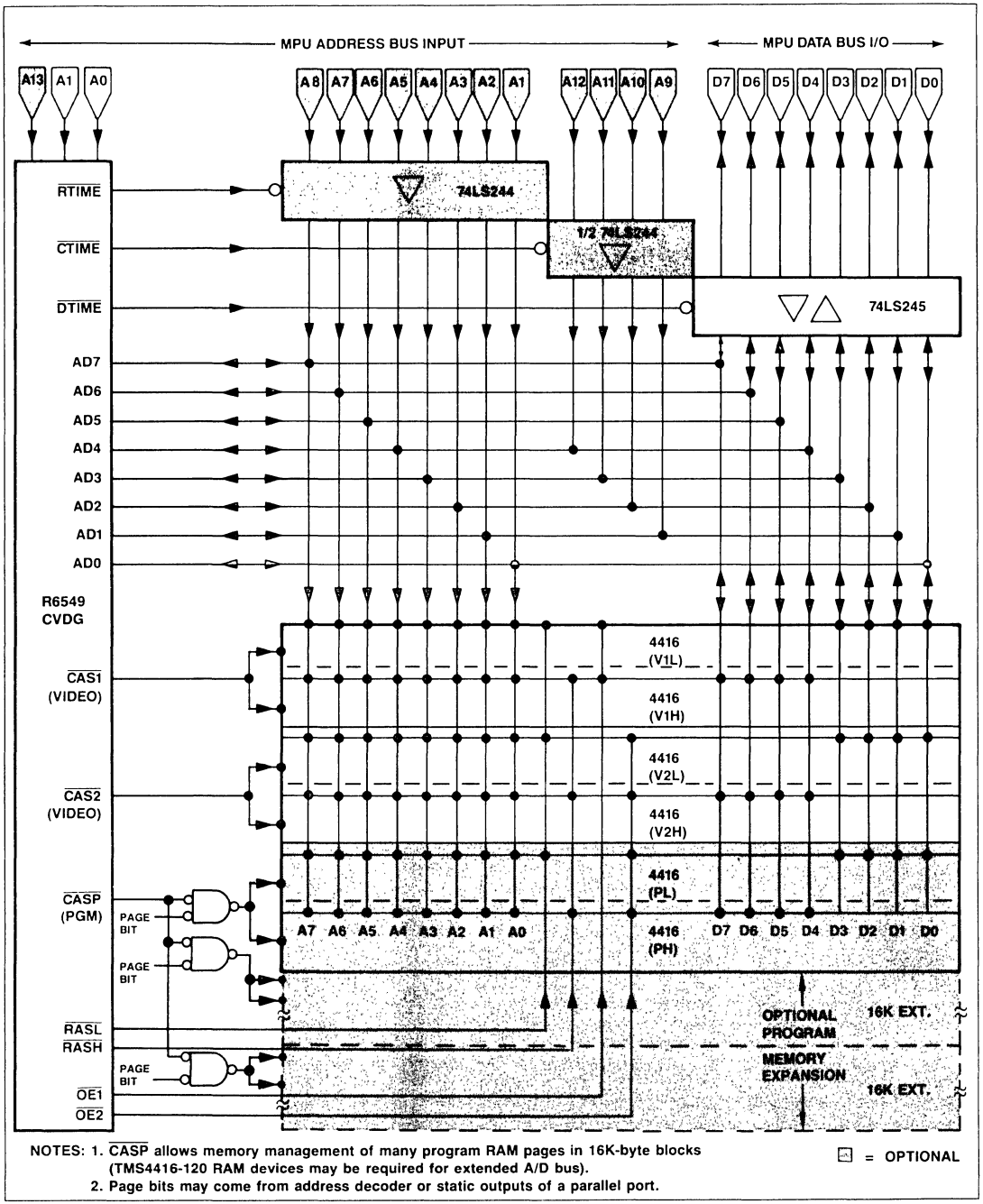
Note that the DRAM requires assertion of all three control signals for a valid access (i.e., $\overline{RAS}$, $\overline{CAS}$ and $\overline{OE}$ for a read and $\overline{RAS}$, $\overline{CAS}$ and $\overline{W}$ for a write). The CVDG sometimes outputs one or two of these signals but not all three control signals in "no access" situations.

TELETEXT DMA I/O ACCESS

Teletext data can be DMA transferred from a teletext prefix processor connected to the A/D bus to DRAM locations addressed by the CVDG. A 13-bit TTX Latch/Counter determines the DRAM address. The upper 8-bits of the TTX Counter is a latch. The value of the latch is defined by the TTX Pointer Register which can be loaded in Mode 5 by writing to register address 2 (A1 = 1 and A0 = 0). The TTX Pointer Register value therefore defines the TTX DMA starting address on a 32-byte boundary. The lower 5-bits of the TTX Latch/Counter is a modulo 32 counter. This counter increments by one after each TTX byte transfer. When the counter overflows (i.e., from 31 to 0) the upper count is incremented by one to increment the total address. The address is reset to zero during horizontal blanking. The upper count may be read from the TTX Pointer Register at any time in Mode 5.

TTX DMA transfer is initiated by asserting $\overline{\text{TTXREQ}}$ to the CVDG. The CVDG asserts TTX Output Enable ($\overline{\text{TTXOE}}$) to acknowledge $\overline{\text{TTXREQ}}$ receipt, suspends outputting the E and Q clocks for one cycle, outputs the 13-bit DRAM address and asserts DRAM Write Enable ($\overline{\text{W}}$) to enable writing into DRAM.

Note that DMA must be used only when the horizontal sync is genlocked to the external teletext raster.



NOTES: 1. $\overline{\text{CASP}}$ allows memory management of many program RAM pages in 16K-byte blocks (TMS4416-120 RAM devices may be required for extended A/D bus).
2. Page bits may come from address decoder or static outputs of a parallel port.

[ ] = OPTIONAL

Figure 6. CVDG Connection to A/D Bus and DRAM

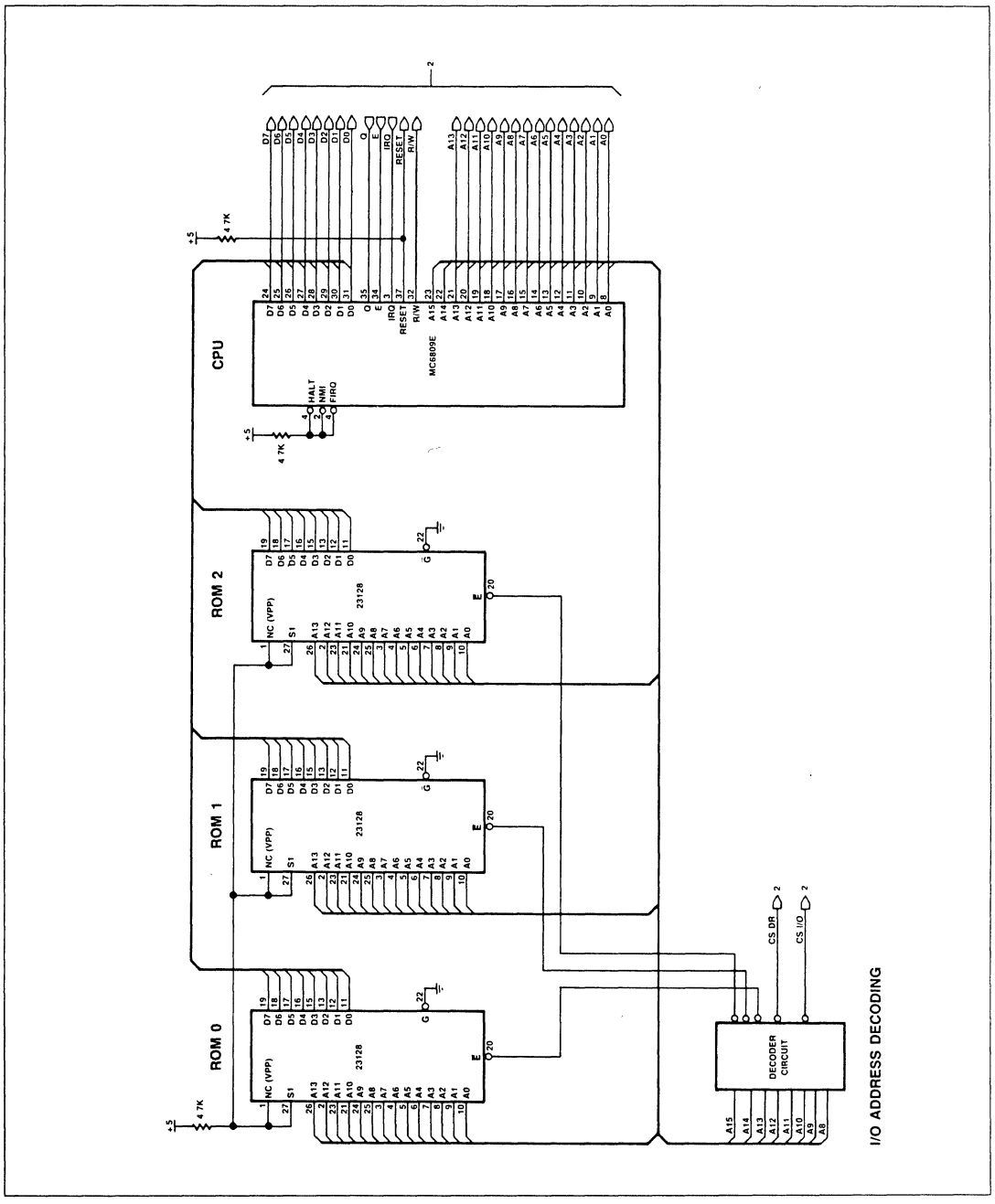


Figure 7. CVDG Application Schematic (Typical) (Sheet 1 of 2)

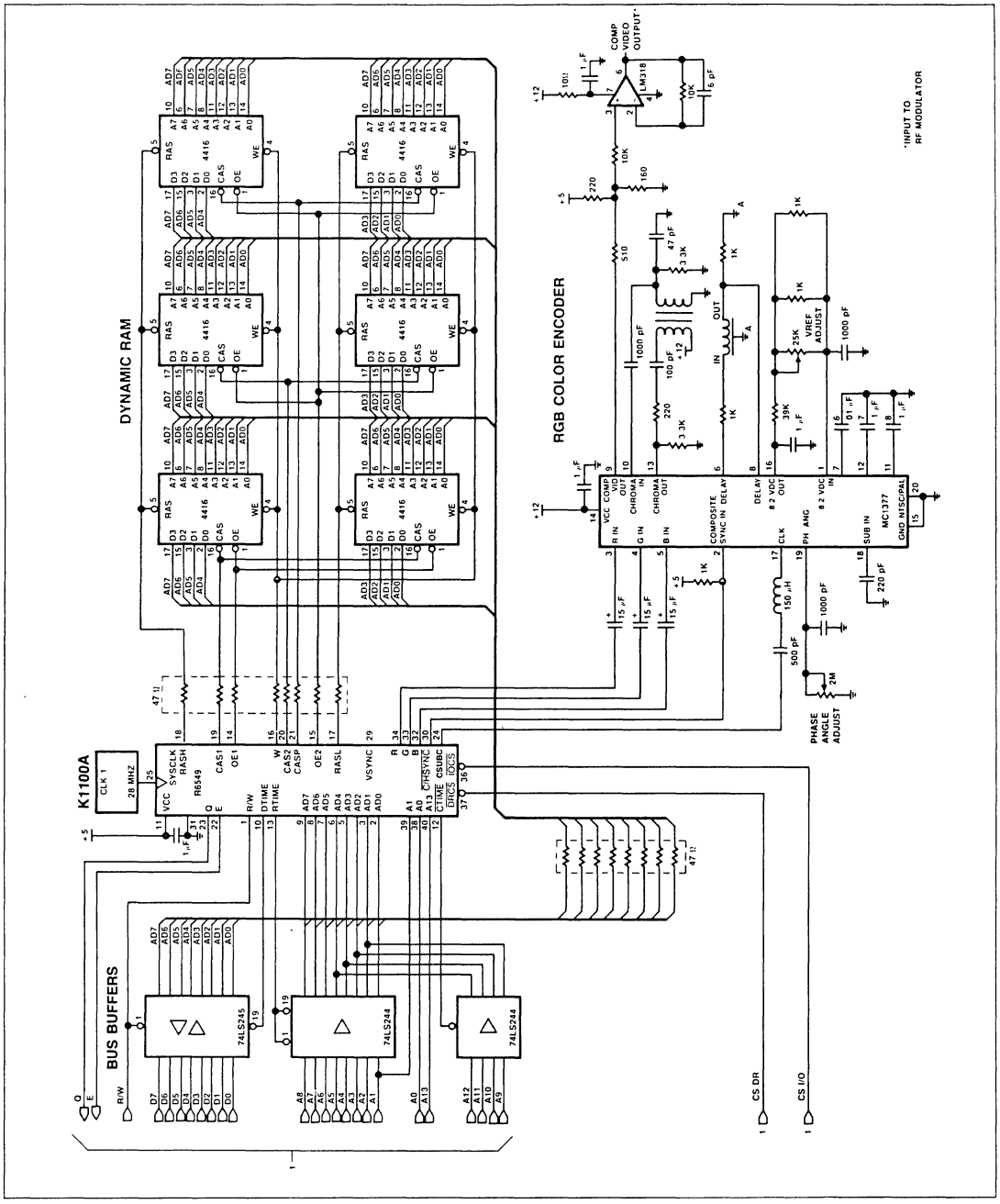


Figure 7. CVDG Application Schematic (Typical) (Sheet 2 of 2)

AC CHARACTERISTICS

(V_{CC} = 5.0V ±5%, V_{SS} = 0)

MPU CLOCK AND CONTROL LINE TIMING

Ref. Fig. 8 No.	Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
1	t_{ECYC}	E Cycle Time	700	698		ns	1
2	t_r, t_f	E and Q Rise and Fall		25		ns	
3	t_{ELEH}	E Low to E High		350		ns	
4	t_{EHEL}	E High to E Low		350		ns	
5	t_{ELQH}	E Low to Q Rising		175		ns	
6	t_{QHEH}	Q High to E Rising		175		ns	
7	t_{EHQL}	E High to Q Falling		175		ns	
8	t_{QLEL}	Q Low to E Falling		175		ns	
9	t_{SLEH}	Chip Select Low to E Rising (Setup)		70		ns	
10	t_{SHEH}	Chip Select High to E Rising (Hold)		0		ns	
11	t_{EHQV}	E High to Data Valid (Read)			240	ns	
12	t_{ELQZ}	E Low to Output High Z (Read)		10		ns	
13	t_{DVEL}	Data Valid to E Falling (Write)	100			ns	
14	t_{ELDZ}	E Falling to Data Invalid (Write)		30		ns	

Note:
1. Based on 28.636363 MHz SYSCLK input.

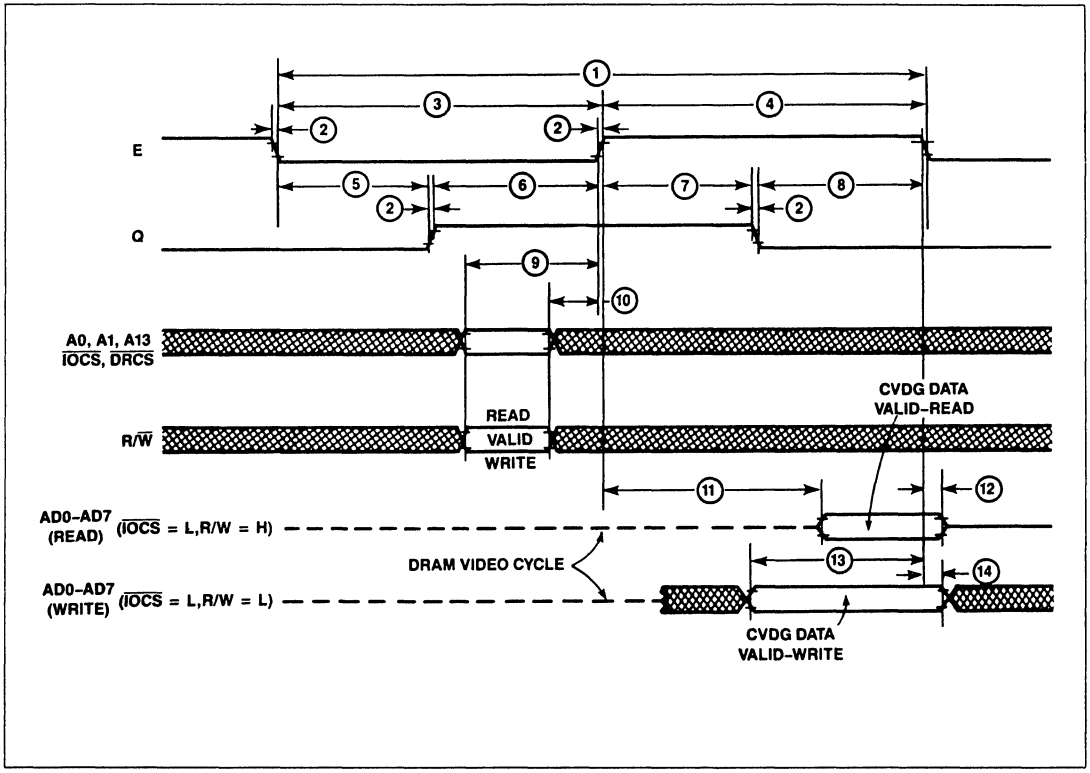


Figure 8. CVDG-MPU A/D Bus Timing Waveforms

DRAM TIMING — VIDEO ACCESS CYCLE

Ref. Fig. 9 No.	Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
1	t_{RLRTL}	$\overline{RAS}$ Low to $\overline{RTIME}$ Low (Delay)		315		ns	
2	t_{RTLRTH}	$\overline{RTIME}$ Low to $\overline{RTIME}$ High		70		ns	
3	t_{RLCTL}	$\overline{RAS}$ Low to $\overline{CTIME}$ Low (Delay)		35		ns	
4	t_{CTLCTH}	$\overline{CTIME}$ Low to $\overline{CTIME}$ High		87		ns	
5	t_{RLDTL}	$\overline{RAS}$ Low to $\overline{DTIME}$ Low (Delay)		122		ns	
6	t_{DTLDTH}	$\overline{DTIME}$ Low to $\overline{DTIME}$ High		157		ns	
7	t_{RC}	RAM Read/Write Cycle		350		ns	
8	t_{RP}	$\overline{RAS}$ High Width		105		ns	
9	t_{RAS}	$\overline{RAS}$ Low Width		245		ns	
10	t_{RCD}	$\overline{RAS}$ Low to $\overline{CAS}$ Low (Delay)		70		ns	
11	t_{CAS}	$\overline{CAS}$ Low Width		245		ns	
12	t_{CSH}	$\overline{RAS}$ Low to $\overline{CAS}$ Rising (Delay)		315		ns	
13	t_{RSH}	$\overline{CAS}$ Low to $\overline{RAS}$ Rising (Delay)		175		ns	
14	t_{CPN}	$\overline{CAS}$ High Width		105		ns	
15	t_{CRP}	$\overline{CAS}$ High to $\overline{RAS}$ Falling (Delay)		35		ns	
16	t_t	$\overline{RAS}$ and $\overline{CAS}$ Transition Times		5		ns	
17	t_{RCS}	Read Command Setup		105		ns	
18	t_{ASR}	Row Address Setup		35		ns	
19	t_{RAH}	Row Address Hold		35		ns	
20	t_{ASC}	Column Address Setup		35		ns	
21	t_{CAH}	Column Address Hold		70		ns	
22	t_{AR}	$\overline{RAS}$ Low to Column Hold		140		ns	
23	t_{RAC}	$\overline{RAS}$ Low to Data Valid (Setup)			150	ns	
24	t_{CAC}	$\overline{CAS}$ Low to Data Valid (Setup)			80	ns	
25	t_{RLG1L}	$\overline{RAS}$ Low to $\overline{OE1}$ Low (Delay)		140		ns	
26	t_{GLGHr}	$\overline{OE}$ Low to $\overline{OE}$ High		70		ns	
27	t_{OEA}	$\overline{OE}$ Low to Data Valid (Setup)	0		40	ns	
28	t_{OEZ}	$\overline{OE}$ High to Output High Z (Hold)	0		35	ns	
29	t_{RLG2L}	$\overline{RAS}$ Low to $\overline{OE2}$ Low (Delay)		210		ns	

DRAM TIMING — MPU DRAM ACCESS CYCLE

Ref. Fig. 9 No.	Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
30	t_{RRH}	Read Command Hold After $\overline{RAS}$ High		280		ns	
31	t_{RCH}	Read Command Hold After $\overline{CAS}$ High		210		ns	
33	t_{GLGH}	$\overline{OE1}$, $\overline{OE2}$ Low to $\overline{OE1}$, $\overline{OE2}$ High		140		ns	
36	t_{DS}	Data Setup		12		ns	
37	t_{WP}	$\overline{W}$ Low to $\overline{W}$ High		140		ns	
38	t_{DH}	Data Hold After $\overline{W}$ Low		70		ns	
39	t_{DHC}	Data Hold After $\overline{CAS}$ Low		175		ns	
40	t_{DHR}	Data Hold After $\overline{RAS}$ Low		245		ns	
41	t_{WCR}	Write Command Hold After $\overline{RAS}$ Low		315		ns	
42	t_{WCH}	Write Command Hold After $\overline{CASP}$ Low		245		ns	
43	t_{RWL}	Write Command Setup before $\overline{RAS}$ Rising		70		ns	
44	t_{CWL}	Write Command Setup before $\overline{CAS}$ Rising		140		ns	

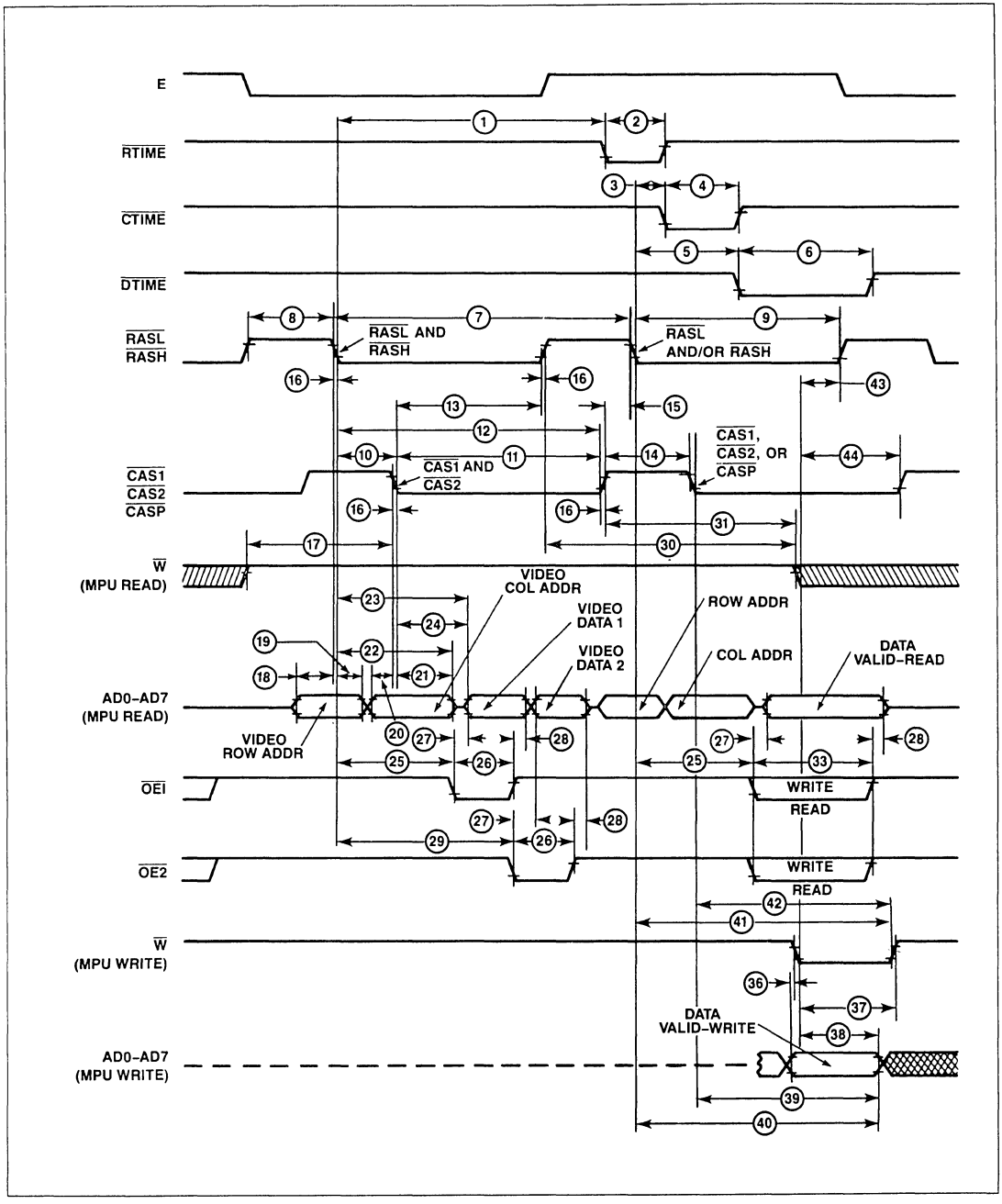


Figure 9. CVDG-DRAM A/D Bus Timing Waveforms

TELETEXT DMA CYCLE TIMING

Ref. Fig. 10 No.	Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
1	t_{RLEL}	$\overline{TTXREQ}$ Low to E Low (Setup)		80		ns	
2	t_{ELRH}	E Low to $\overline{TTXREQ}$ High (Hold)		10		ns	
3	t_{ELGL}	E Low to $\overline{TTXOE}$ Low		595		ns	
4	t_{GLGH}	$\overline{TTXOE}$ Low to $\overline{TTXOE}$ High		140		ns	

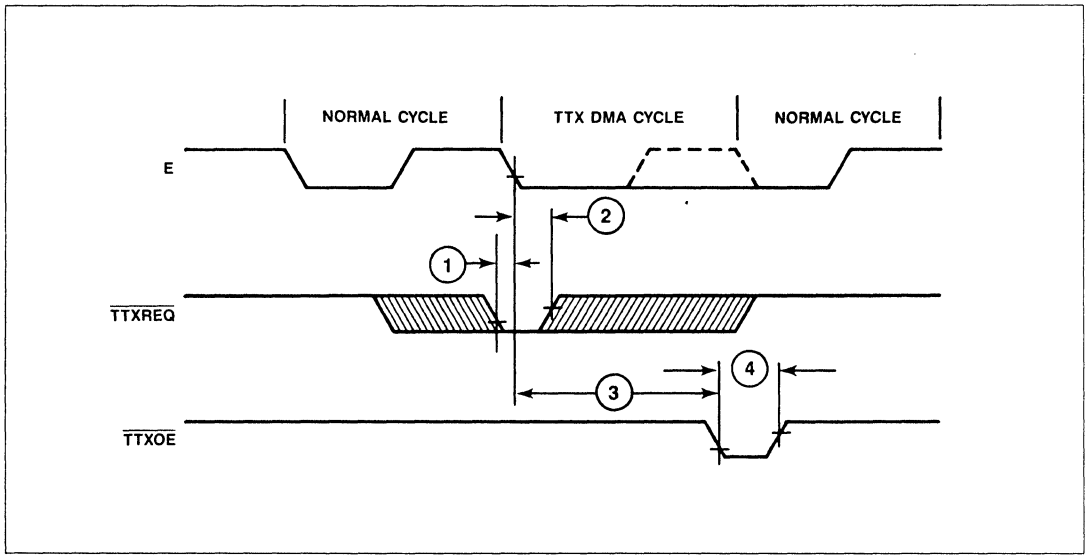


Figure 10. Teletext Prefix Processor — CVDG Timing Waveforms

HORIZONTAL VIDEO TIMING

Ref. Fig. 11 No.	Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
1		H Sync to Setup	9.3	9.4	9.5	μs	1
2		H Front Porch	1.4	1.5	1.6	μs	1
3		H Sync to XPAR	—	10.16	—	μs	2
4		XPAR Front Porch	—	2.79	—	μs	2
5		H Sync to Border 1	—	8.38	—	μs	2
6		H Sync to Graphics	—	12.57	—	μs	2
7		H Sync to Border 2	—	57.27	—	μs	2
8		Border Front Porch	—	2.79	—	μs	2
9		H Sync Tip	—	4.81	—	μs	2
10		H Period (Normal)	—	63.556	—	μs	2
11		H Period (Early)	—	62.857	—	μs	2

Notes: 1. RS-170A Specification (shown for reference only).
2. ±0.1μs; based on 28.636363 MHz SYSCLK input.

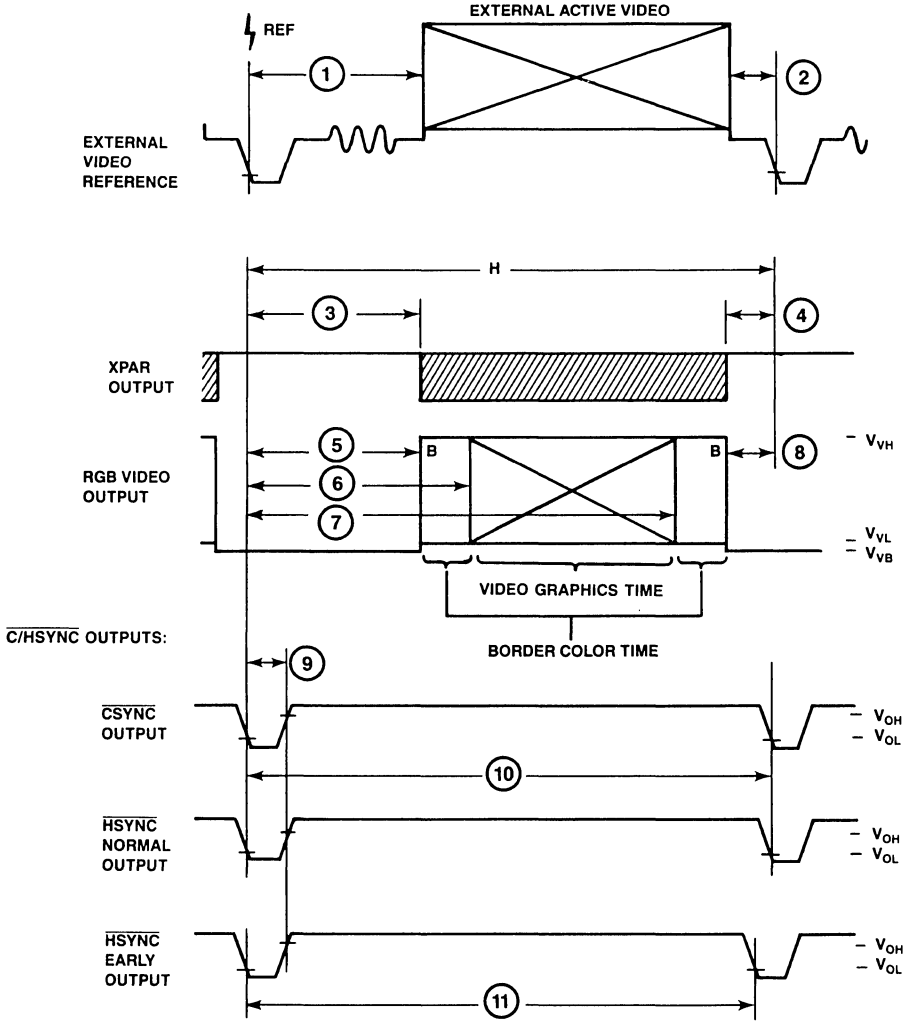
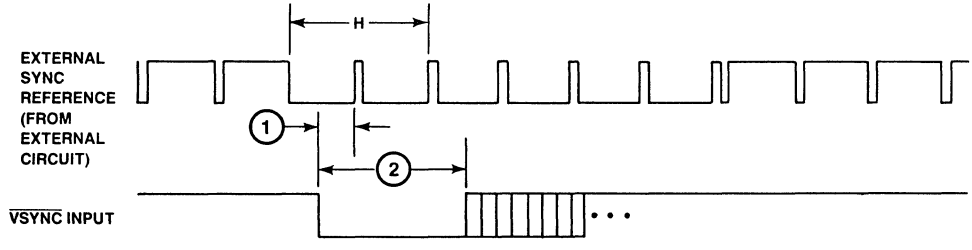


Figure 11. Horizontal Video Output Timing Waveforms

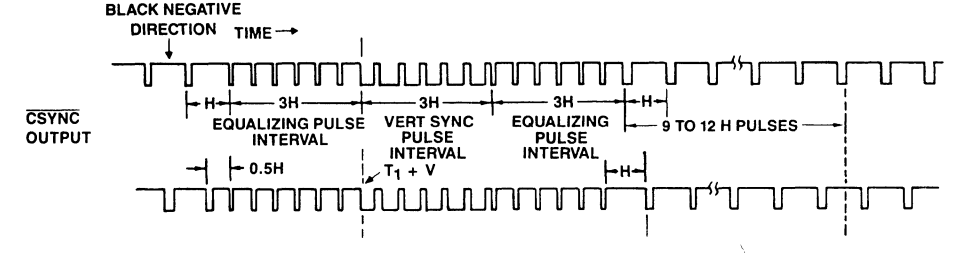
Vertical Cycle Timing

Ref. Fig. 12 No.	Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
1	V_{SU}	$\overline{VSYNC}$ Low Input to First Serration Setup	20	—	—	ns	3
2	V_H	$\overline{VSYNC}$ Low Input Pulse Duration	63.5	—	—	μs	3
—		$\overline{VSYNC}$ Low Output Pulse Duration (Burst Blank)	19	—	—	H	1
—		V Blank Duration	52	—	—	H	1
—		V Unblank to Graphics Duration (Top Border)	21	—	—	H	1
—		Graphics to V Blank Duration (Bottom Border)	31	—	—	H	1, 2

Notes: 1. H = $\overline{HSYNC}$ pulse width (63.5 μs)
2. 2:1 interlace mode.
3. Shown for reference only—not an R6549 requirement.



a. Vertical Synchronization



b. RS-170A Composite Sync VBI Timing Specifications

Figure 12. Vertical Cycle Waveforms—2:1 Interlace

TELETEXT DMA CYCLE TIMING

Ref. Fig. 13 No.	Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
1	t_{ELPL}	E Low to PIXCK High		0		ns	
2	t_{PHPL}	PIXCK High to PIXCK Low		70		ns	
3	t_{PLPH}	PIXCK Low to PIXCK High		105		ns	
4	t_{PCYC}	PIXCK Cycle		175		ns	

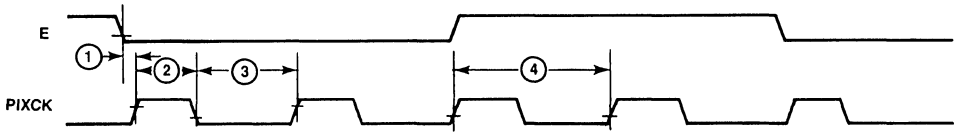


Figure 13. Video Output Waveforms

DC CHARACTERISTICS

(V_{CC} = 5.0V ±5%, V_{SS} = 0V, T_A = 0°C to 70°C, unless otherwise noted)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Input High Voltage					V	
SYSCLK	V_{IHC}	V_{CC} - 0.75	—	V_{CC}		
$\overline{IOCS}$, $\overline{DRCS}$, $\overline{TTXREQ}$, A0, A1, A13, R/$\overline{W}$, $\overline{VSYNC}$, AD0-AD7	V_{IH}	V_{SS} + 2.0	—	V_{CC}		
Input Low Voltage					V	
SYSCLK	V_{ILC}	V_{SS} - 0.3	—	V_{SS} + 0.4		
$\overline{IOCS}$, $\overline{DRCS}$, $\overline{TTXREQ}$, A0, A1, A13, R/$\overline{W}$ $\overline{VSYNC}$, AD0-AD7	V_{IL}	V_{SS} - 0.3	—	V_{SS} + 0.8		
Input Leakage Current	I_{IL}	—	—	±10	μA	V_{IN} = 0V to 5.25V V_{CC} = 0
Output High Voltage	V_{OH}				V	V_{CC} = 4.75V
E		V_{CC} - 0.75	—	—		I_{OH} = -0.14 mA Note 1
Q, $\overline{RTIME}$, $\overline{CTIME}$, $\overline{DTIME}$, $\overline{RASL}$, $\overline{RASH}$, $\overline{W}$ $\overline{CAS1}$, $\overline{CAS2}$, $\overline{CASP}$, $\overline{OE1}$, $\overline{OE2}$, $\overline{TTXOE}$, C/$\overline{HSYNC}$, $\overline{VSYNC}$, CSUBC, PIXCK, XPAR		V_{SS} + 2.4	—	—		I_{OH} = -80 μA Note 2
AD0-AD7		V_{SS} + 2.4	—	—		I_{OH} = -170 μA Note 3
Output Low Voltage	V_{OL}				V	V_{CC} = 4.75V
E		—	—	V_{SS} + 0.4		I_{OL} = 1.7 mA Note 1
Q, $\overline{RTIME}$, $\overline{CTIME}$, $\overline{DTIME}$, $\overline{RASL}$, $\overline{RASH}$, $\overline{W}$, $\overline{CAS1}$, $\overline{CAS2}$, $\overline{CASP}$, $\overline{OE1}$, $\overline{OE2}$, $\overline{TTXOE}$, C/$\overline{HSYNC}$, $\overline{VSYNC}$, CSUBC, PIXCK, XPAR		—	—	V_{SS} + 0.4		I_{OL} = 1.6 mA Note 2
AD0-AD7		—	—	V_{SS} + 0.4		I_{OL} = 3.0 mA Note 3
Output Leakage Current (Off-State) AD0-AD7	I_{OFF}	—	—	±20	μA	V_{IN} = 0 to 5.25V
Output High Voltage R, G, B	V_{VH}	—	+2.800	—	V	C_L = 30 pF R_L = 10K Ohms t_r/t_f = 50 ns
Output Low Voltage R, G, B	V_{VL}	—	+1.875	—	V	
Output Blanking Voltage R, G, B	V_{VB}	—	+1.800	—	V	
Input Capacitance[4]	C_{IN}				pF	V_{CC} = 5.0V, chip
SYSCLK		—	—	10		deselected, pin
$\overline{IOCS}$, $\overline{DRCS}$, $\overline{TTXREQ}$, A0, A1, A13, R/$\overline{W}$, $\overline{VSYNC}$, AD0-AD7		—	—	5		Under test at 0V, T_A = 25°C, f = 0.986 MHz (SYSCLK = 28.6363 MHz)

Notes:
1. Output Load: 1 TTL gate; C_L = 140 pF
2. Output Load: 1 TTL gate; C_L = 100 pF
3. Output Load: 6 DRAM, 2 LS244 buffers and 1 LS245 transceiver; C_L = 180 pF
4. This parameter is periodically sampled and is not 100% tested.

ABSOLUTE MAXIMUM RATINGS*

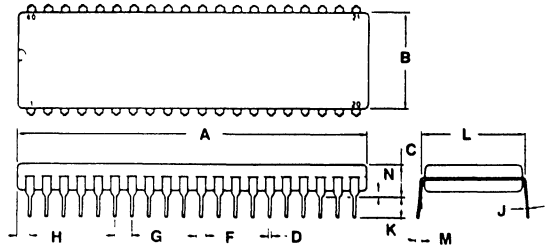
Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to +7.0	V
Input Voltages	V_{IN}	−0.3 to +7.0	V
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{STG}	−55 to +150	°C

***NOTE:** Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the other sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PACKAGE DIMENSIONS

2

40-PIN PLASTIC DIP



	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	51.28	52.32	2.040	2.060
B	13.72	14.22	0.540	0.560
C	3.55	5.08	0.140	0.200
D	0.36	0.51	0.014	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.30	0.008	0.012
K	3.05	3.56	0.120	0.140
L	15.24 BSC		0.600 BSC	
M	7°	10°	7°	10°
N	0.51	1.02	0.020	0.040

Rockwell

R6551
Asynchronous Communications Interface Adapter (ACIA)

DESCRIPTION

The Rockwell R6551 Asynchronous Communications Interface Adapter (ACIA) provides an easily implemented, program controlled interface between 8-bit microprocessor-based systems and serial communication data sets and modems.

The ACIA has an internal baud rate generator. This feature eliminates the need for multiple component support circuits, a crystal being the only other part required. The Transmitter baud rate can be selected under program control to be either 1 of 15 different rates from 50 to 19,200 baud, or at $^1/_{16}$ times an external clock rate. The Receiver baud rate may be selected under program control to be either the Transmitter rate, or at $^1/_{16}$ times an external clock rate. The ACIA has programmable word lengths of 5, 6, 7, or 8 bits; even, odd, or no parity; 1, 1½, or 2 stop bits.

The ACIA is designed for maximum programmed control from the microprocessor (MPU), to simplify hardware implementation. Three separate registers permit the MPU to easily select the R6551's operating modes and data checking parameters and determine operational status.

The Command Register controls parity, receiver echo mode, transmitter interrupt control, the state of the $\overline{RTS}$ line, receiver interrupt control, and the state of the $\overline{DTR}$ line.

The Control Register controls the number of stop bits, word length, receiver clock source, and baud rate.

The Status Register indicates the states of the $\overline{IRQ}$, $\overline{DSR}$, and $\overline{DCD}$ lines, Transmitter and Receiver Data Registers, and Overrun, Framing, and Parity Error conditions.

The Transmitter and Receiver Data Registers are used for temporary data storage by the ACIA Transmit and Receiver circuits.

ORDERING INFORMATION

Part No.: R6551___

- Temperature Range (T_L to T_H):
  - Blank = 0°C to +70°C
  - E = −40°C to +85°C
- Package:
  - C = Ceramic
  - P = Plastic
- Frequency Range:
  - No Letter = 1 MHz
  - A = 2 MHz

FEATURES

- Compatible with 8-bit microprocessors
- Full duplex operation with buffered receiver and transmitter
- Data set/modem control functions
- Internal baud rate generator with 15 programmable baud rates (50 to 19,200)
- Program-selectable internally or externally controlled receiver rate
- Programmable word lengths, number of stop bits, and parity bit generation and detection
- Programmable interrupt control
- Program reset
- Program-selectable serial echo mode
- Two chip selects
- 2 or 1 MHz operation
- 5.0 Vdc ± 5% supply requirements
- 28-pin plastic or ceramic DIP
- Full TTL compatibility
- Compatible with R6500, R6500/* and R65C00 microprocessors

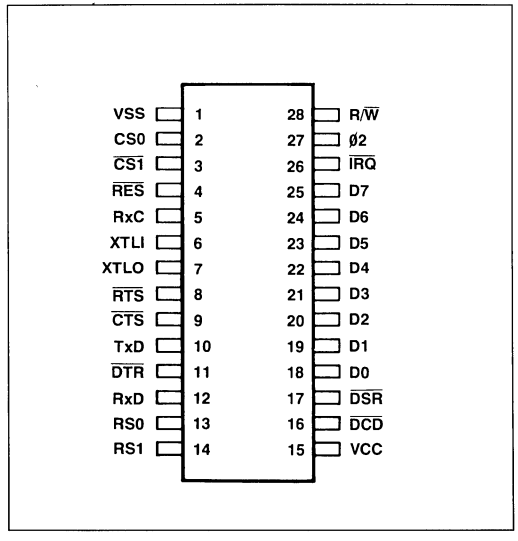


Figure 1. R6551 ACIA Pin Configuration

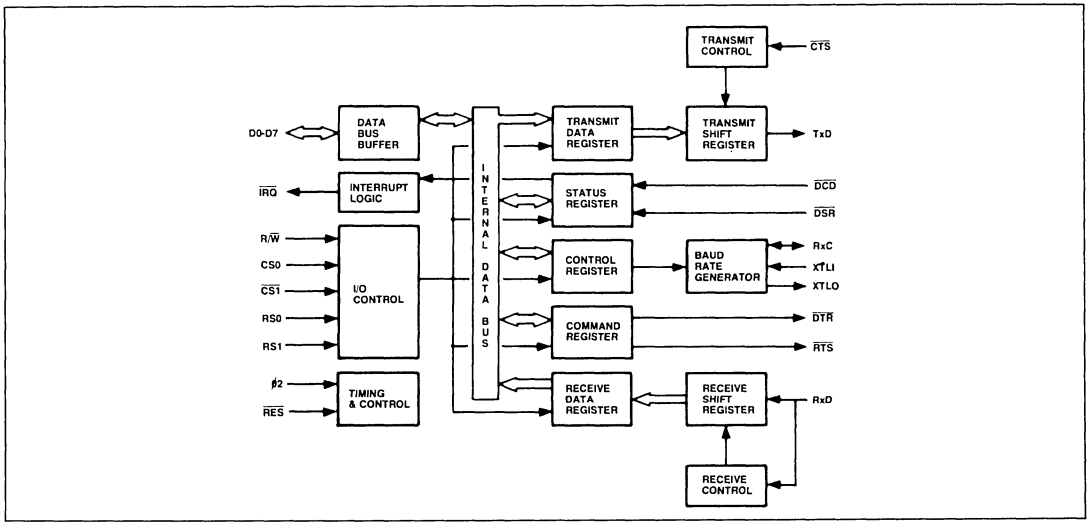


Figure 2. ACIA Internal Organization

FUNCTIONAL DESCRIPTION

A block diagram of the ACIA is presented in Figure 2. A description of each functional element of the device follows.

DATA BUS BUFFERS

The Data Bus Buffer interfaces the system data lines to the internal data bus. The Data Bus Buffer is bi-directional. When the R/$\overline{W}$ line is low and the chip is selected, the Data Bus Buffer writes the data from the system data lines to the ACIA internal data bus. When the R/$\overline{W}$ line is high and the chip is selected, the Data Bus Buffer drives the data from the internal data bus to the system data bus.

INTERRUPT LOGIC

The Interrupt Logic will cause the $\overline{IRQ}$ line to the microprocessor to go low when conditions are met that require the attention of the microprocessor. The conditions which can cause an interrupt will set bit 7 and the appropriate bit of bits 3 through 6 in the Status Register, if enabled. Bits 5 and 6 correspond to the Data Carrier Detect ($\overline{DCD}$) logic and the Data Set Ready ($\overline{DSR}$) logic. Bits 3 and 4 correspond to the Receiver Data Register full and the Transmitter Data Register empty conditions. These conditions can cause an interrupt request if enabled by the Command Register.

I/O CONTROL

The I/O Control Logic controls the selection of internal registers for a data transfer on the internal data bus and the direction of the transfer to or from the register.

The registers are selected by the Register Select (RS1, RS0) and Read/Write (R/$\overline{W}$) lines as described later in Table 1.

TIMING AND CONTROL

The Timing and Control logic controls the timing of data transfers on the internal data bus, the registers, the Data Bus Buffer, the microprocessor data bus, and the hardware reset.

Timing is controlled by the system ϕ2 clock input. The chip will perform data transfers to or from the microcomputer data bus during the ϕ2 high period when selected.

All registers will be initialized by the Timing and Control Logic when the Reset ($\overline{RES}$) line goes low. See the individual register description for the state of the registers following a hardware reset.

TRANSMITTER AND RECEIVER DATA REGISTERS

These registers are used as temporary data storage for the ACIA Transmit and Receive Circuits. Both the Transmitter and Receiver are selected by a Register Select 0 (RS0) and Register Select 1 (RS1) low condition. The Read/Write (R/$\overline{W}$) line determines which actually uses the internal data bus; the Transmitter Data Register is write only and the Receiver Data Register is read only.

Bit 0 is the first bit to be transmitted from the Transmitter Data Register (least significant bit first). The higher order bits follow in order. Unused bits in this register are "don't care".

The Receiver Data Register holds the first received data bit in bit 0 (least significant bit first). Unused high-order bits are "0". Parity bits are not contained in the Receiver Data Register. They are stripped off after being used for parity checking.

STATUS REGISTER

The Status Register indicates the state of interrupt conditions and other non-interrupt status information. The interrupt conditions are Data Set Ready and Data Carrier Detect transitions, Transmitter Data Register Empty and Receiver Data Register Full as reported in bits 6 through 3, respectively. If any of these bits are set, the Interrupt (IRQ) indicator (bit 7) is also set. Overrun, Framing Error, and Parity Error are also reported (bits 2 through 0 respectively).

7	6	5	4	3	2	1	0
IRQ	$\overline{DSR}$	$\overline{DCD}$	TDRE	RDRE	OVRN	FE	PE

Bit 7 **Interrupt (IRQ)**
0 No interrupt
1 Interrupt has occurred

Bit 6 **Data Set Ready ($\overline{DSR}$)**
0 $\overline{DSR}$ low (ready)
1 $\overline{DSR}$ high (not ready)

Bit 5 **Data Carrier Detect ($\overline{DCD}$)**
0 $\overline{DCD}$ low (detected)
1 $\overline{DCD}$ high (not detected)

Bit 4 **Transmitter Data Register Empty**
0 Not empty
1 Empty

Bit 3 **Receiver Data Register Full**
0 Not full
1 Full

Bit 2 **Overrun***
0 No overrun
1 Overrun has occurred

Bit 1 **Framing Error***
0 No framing error
1 Framing error detected

Bit 0 **Parity Error***
0 No parity error
1 Parity error detected

*No interrupt occurs for these conditions

Reset Initialization

7	6	5	4	3	2	1	0	
0	—	—	1	0	0	0	0	**Hardware reset**
—	—	—	—	—	0	—	—	**Program reset**

Parity Error (Bit 0), Framing Error (Bit 1), and Overrun (Bit 2)

None of these bits causes a processor interrupt to occur, but they are normally checked at the time the Receiver Data Register is read so that the validity of the data can be verified. These bits are self clearing (i.e., they are automatically cleared after a read of the Receiver Data Register).

Receiver Data Register Full (Bit 3)

This bit goes to a 1 when the ACIA transfers data from the Receiver Shift Register to the Receiver Data Register, and goes to a 0 (is cleared) when the processor reads the Receiver Data Register.

Transmitter Data Register Empty (Bit 4)

This bit goes to a 1 when the ACIA transfers data from the Transmitter Data Register to the Transmitter Shift Register, and goes to a 0 (is cleared) when the processor writes new data onto the Transmitter Data Register.

NOTE: There is a delay of approximately $\frac{1}{16}$ of a bit time after TDR becomes empty/full before this flag is updated.

Data Carrier Detect (Bit 5) and Data Set Ready (Bit 6)

These bits reflect the levels of the $\overline{DCD}$ and $\overline{DSR}$ inputs to the ACIA. A 0 indicates a low level (true condition) and a 1 indicates a high level (false). Whenever either of these inputs change state, an immediate processor interrupt (IRQ) occurs. When the interrupt occurs, the status bits indicate the levels of the inputs immediately after the change of state occurred. Subsequent level changes will not affect the status bits until after the Status Register has been interrogated by the processor. At that time, another interrupt will immediately occur and the status bits will reflect the new input levels. These bits are not automatically cleared (or reset) by an internal operation.

Interrupt (Bit 7)

This bit goes to a 1 whenever an interrupt condition occurs and goes to a 0 (is cleared) when the Status Register is read.

CONTROL REGISTER

The Control Register selects the desired baud rate, frequency source, word length, and the number of stop bits.

7	6	5	4	3	2	1	0
SBN	WL		RCS	SBR			
	WL1	WL0		SBR3	SBR2	SBR1	SBR0

Bit 7 — Stop Bit Number (SBN)

0	1 Stop bit
1	2 Stop bits
1	1½ Stop bits For WL = 5 and no parity
1	1 Stop bit For WL = 8 and parity

Bits 6-5 — Word Length (WL)

6	5	No. Bits
0	0	8
0	1	7
1	0	6
1	1	5

Bit 4 — Receiver Clock Source (RCS)

0	External receiver clock
1	Baud rate

Bits 3-0 — Selected Baud Rate (SBR)

3	2	1	0	Baud
0	0	0	0	16x External Clock
0	0	0	1	50
0	0	1	0	75
0	0	1	1	109.92
0	1	0	0	134.58
0	1	0	1	150
0	1	1	0	300
0	1	1	1	600
1	0	0	0	1200
1	0	0	1	1800
1	0	1	0	2400
1	0	1	1	3600
1	1	0	0	4800
1	1	0	1	7200
1	1	1	0	9600
1	1	1	1	19,200

Reset Initialization

7	6	5	4	3	2	1	0	
0	0	0	0	0	0	0	0	Hardware reset ($\overline{RES}$)
–	–	–	–	–	–	–	–	Program reset

Selected Baud Rate (Bits 0, 1, 2, 3)

These bits select the Transmitter baud rate, which can be at $^1/_{16}$ an external clock rate or one of 15 other rates controlled by the internal baud rate generator.

If the Receiver clock uses the same baud rate as the transmitter, then RxC becomes an output and can be used to slave other circuits to the ACIA. Figure 3 shows the Transmitter and Receiver layout.

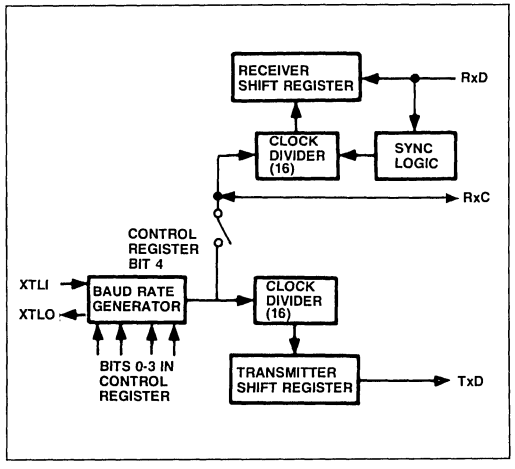


Figure 3. Transmitter/Receiver Clock Circuits

Receiver Clock Source (Bit 4)

This bit controls the clock source to the Receiver. A 0 causes the Receiver to operate at a baud rate of $^1/_{16}$ an external clock. A 1 causes the Receiver to operate at the same baud rate as is selected for the transmitter.

Word Length (Bits 5, 6)

These bits determine the word length to be used (5, 6, 7 or 8 bits).

Stop Bit Number (Bit 7)

This bit determines the number of stop bits used. A 0 always indicates one stop bit. A 1 indicates 1½ stop bits if the word length is 5 with no parity selected, 1 stop bit if the word length is 8 with parity selected, or 2 stop bits in all other configurations.

COMMAND REGISTER

The Command Register controls specific modes and functions.

7	6	5	4	3	2	1	0
PMC		PME	REM	TIC		IRD	DTR
PMC1	PMC0			TIC1	TIC0		

Bits 7-6 Parity Mode Control (PMC)

7	6	
0	0	Odd parity transmitted/received
0	1	Even parity transmitted/received
1	0	Mark parity bit transmitted Parity check disabled
1	1	Space parity bit transmitted Parity check disabled

Bit 5 Parity Mode Enabled (PME)

0	Parity mode disabled No parity bit generated Parity check disabled
1	Parity mode enabled

Bit 4 Receiver Echo Mode (REM)

0	Receiver normal mode
1	Receiver echo mode Bits 2 and 3 must also be zero for receiver echo mode, $\overline{RTS}$ will be low.

Bits 3-2 Transmitter Interrupt Control (TIC)

3	2	
0	0	$\overline{RTS}$ = High, transmitter disabled*
0	1	$\overline{RTS}$ = Low, transmit interrupt enabled
1	0	$\overline{RTS}$ = Low, tansmit interrupt disabled
1	1	$\overline{RTS}$ = Low, transmit interrupt disabled, transmit break on TxD**

Bit 1 Receiver Interrupt Request Disabled (IRD)

0	$\overline{IRQ}$ enabled (receiver)
1	$\overline{IRQ}$ disabled (receiver)

Bit 0 Data Terminal Ready (DTR)

0	Data terminal not ready ($\overline{DTR}$ high)*
1	Data terminal ready ($\overline{DTR}$ low)

NOTES

*The transmitter is disabled immediately. The receiver is disabled but will first complete receiving a byte in process of being received.

**A break is transmitted only after the end of a character stream. If the Transmit Data Register contains a character, the break is not transmitted.

Data Terminal Ready (Bit 0)

This bit enables all selected interrupts and controls the state of the Data Terminal Ready ($\overline{DTR}$) line. A 0 indicates the microcomputer system is not ready by setting the $\overline{DTR}$ line high. A 1 indicates the microcomputer system is ready by setting the $\overline{DTR}$ line low. $\overline{DTR}$ also enables and disables the transmitter and receiver.

Receiver Interrupt Control (Bit 1)

This bit disables the Receiver from generating an interrupt when set to a 1. The Receiver interrupt is enabled when this bit is set to a 0 and Bit 0 is set to a 1.

Transmitter Interrupt Control (Bits 2, 3)

These bits control the state of the Ready to Send ($\overline{RTS}$) line and the Transmitter interrupt.

Receiver Echo Mode (Bit 4)

A 1 enables the Receiver Echo Mode and a 0 disables the Receiver Echo Mode. When bit 4 is a 1 bits 2 and 3 must be 0. In the Receiver Echo Mode, the Transmitter returns each transmission received by the Receiver delayed by one-half bit time.

Parity Mode Enable (Bit 5)

This bit enables parity bit generation and checking. A 0 disables parity bit generation by the Transmitter and parity bit checking by the Receiver. A 1 bit enables generation and checking of parity bits.

Parity Mode Control (Bits 6, 7)

These bits determine the type of parity generated by the Transmitter, (even, odd, mark or space) and the type of parity check done by the Receiver (even, odd, or no check).

Reset Initialization

7	6	5	4	3	2	1	0	
0	0	0	0	0	0	0	0	**Hardware reset ($\overline{RES}$)**
–	–	–	0	0	0	0	0	**Program reset**

INTERFACE SIGNALS

Figure 4 shows the ACIA interface signals associated with the microprocessor and the modem.

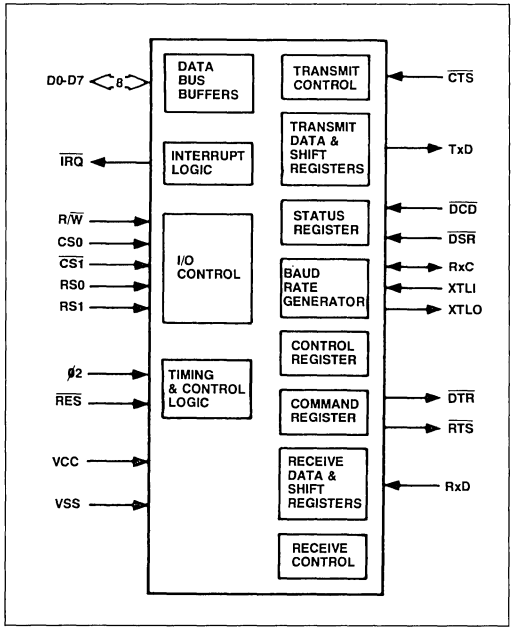


Figure 4. ACIA Interface Diagram

MICROPROCESSOR INTERFACE

Reset ($\overline{RES}$)

During system initialization a low on the $\overline{RES}$ input causes a hardware reset to occur. Upon reset, the Command Register and the Control Register are cleared (all bits set to 0). The Status Register is cleared with the exception of the indications of Data Set Ready and Data Carrier Detect, which are externally controlled by the $\overline{DSR}$ and $\overline{DCD}$ lines, and the transmitter Empty bit, which is set. $\overline{RES}$ must be held low for one ϕ2 clock cycle for a reset to occur.

Input Clock (ϕ2)

The input clock is the system ϕ2 clock and clocks all data transfers between the system microprocessor and the ACIA.

NOTE: The specified maximum cycle time for the signal on this input is 40 μs. This specification must be observed to prevent loss of data.

Read/Write (R/$\overline{W}$)

The R/$\overline{W}$ input, generated by the microprocessor controls the direction of data transfers. A high on the R/$\overline{W}$ pin allows the processor to read the data supplied by the ACIA, a low allows a write to the ACIA.

Interrupt Request ($\overline{IRQ}$)

The $\overline{IRQ}$ pin is an interrupt output from the interrupt control logic. It is an open drain output, permitting several devices to be connected to the commmon $\overline{IRQ}$ microprocessor input. Normally a high level, $\overline{IRQ}$ goes low when an interrupt occurs.

Data Bus (D0-D7)

The eight data line (D0-D7) pins transfer data between the processor and the ACIA. These lines are bi-directional and are normally high-impedance except during Read cycles when the ACIA is selected.

Chip Selects (CS0, $\overline{CS1}$)

The two chip select inputs are normally connected to the processor address lines either directly or through decoders. The ACIA is selected when CS0 is high and $\overline{CS1}$ is low. When the ACIA is selected, the internal registers are addressed in accordance with the register select lines (RS0, RS1).

Register Selects (RS0, RS1)

The two register select lines are normally connected to the processor address lines to allow the processor to select the various ACIA internal registers. Table 1 shows the internal register select decoding.

Table 1. ACIA Register Selection

RS1	RS0	Register Operation	
		R/$\overline{W}$ = Low	R/$\overline{W}$ = High
L	L	Write Transmit Data Register	Read Receiver Data Register
L	H	Programmed Reset (Data is "Don't Care")	Read Status Register
H	L	Write Command Register	Read Command Register
H	H	Write Control Register	Read Control Register

Only the Command and Control registers can be both read and written. The programmed Reset operation does not cause any data transfer, but is used to clear bits 4 through 0 in the Command register and bit 2 in the Status Register. The Control Register is unchanged by a programmed Reset. It should be noted that the programmed Reset is slightly different from the hardware Reset ($\overline{RES}$); refer to the register description.

ACIA/MODEM INTERFACE

Crystal Pins (XTLI, XTLO)

These pins are normally directly connected to a series mode external crystal (1.8432 MHz) to derive the various baud rates. Alternatively, an externally generated clock can drive the XTLI pin, in which case the XTLO pin must float. XTLI is the input pin for the transmit clock.

Transmit Data (TxD)

The TxD output line transfers serial nonreturn-to-zero (NRZ) data to the modem. The least significant bit (LSB) of the Transmit Data Register is the first data bit transmitted and the rate of data transmission is determined by the baud rate selected or by an external clock. This selection is made by programming the Control Register.

Receive Data (RxD)

The RxD input line transfers serial NRZ data into the ACIA from the modem, LSB first. The receiver data rate is determined by the programmed baud rate or by an externally generated receiver clock. The selection is made by programming the Control Register.

Receive Clock (RxC)

RxC is a bi-directional pin which is either the receiver 16x clock input or the receiver 16x clock output. The latter mode results if the internal baud rate generator is selected for receiver data clocking.

Request to Send ($\overline{RTS}$)

The $\overline{RTS}$ output pin controls the modem from the processor. The state of the $\overline{RTS}$ pin is determined by the contents of the Command Register.

Clear to Send ($\overline{CTS}$)

The $\overline{CTS}$ input pin controls the transmitter operation. The enable state is with $\overline{CTS}$ low. The transmitter is automatically disabled if $\overline{CTS}$ is high.

Data Terminal Ready ($\overline{DTR}$)

This output pin indicates the status of the ACIA to the modem. A low on $\overline{DTR}$ indicates the ACIA is enabled, a high indicates it is disabled. The processor controls this pin via bit 0 of the Command Register.

Data Set Ready ($\overline{DSR}$)

The $\overline{DSR}$ input pin indicates to the ACIA the status of the modem. A low indicates the "ready" state and a high, "not-ready."

Data Carrier Detect ($\overline{DCD}$)

The $\overline{DCD}$ input pin indicates to the ACIA the status of the carrier-detect output of the modem. A low indicates that the modem carrier signal is present and a high, that it is not.

TRANSMITTER AND RECEIVER OPERATION

Continuous Data Transmit

In the normal operating mode, the interrupt request output ($\overline{IRQ}$) signals when the ACIA is ready to accept the next data word to be transmitted. This interrupt occurs at the beginning of the Start Bit. When the processor reads the Status Register of the ACIA, the interrupt is cleared.

The processor must then identify that the Transmit Data Register is ready to be loaded and must then load it with the next data word. This must occur before the end of the Stop Bit, otherwise a continuous "MARK" will be transmitted. Figure 5 shows the continuous Data Transmit timing relationship.

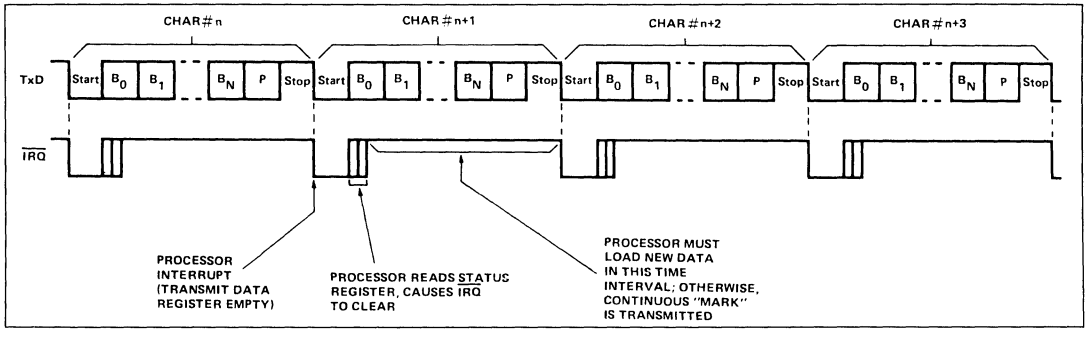


Figure 5. Continuous Data Transmit

Continuous Data Receive

Similar to the Continuous Data Transmit case, the normal operation of this mode is to assert $\overline{IRQ}$ when the ACIA has received a full data word. This occurs at about $^{9}/_{16}$ point through the Stop Bit. The processor must read the Status Register and read the data word before the next interrupt, otherwise the Overrun condition occurs. Figure 6 shows the continuous Data Receive Timing Relationship.

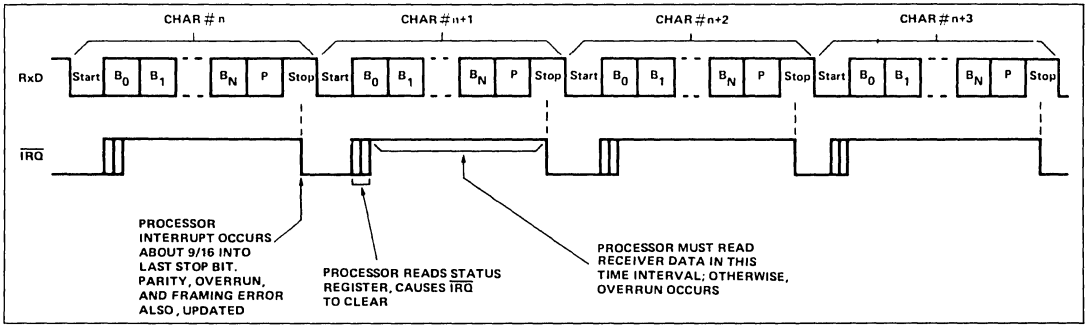


Figure 6. Continuous Data Receive

Transmit Data Register Not Loaded by Processor

If the processor is unable to load the Transmit Data Register in the allocated time, then the TxD line goes to the "MARK" condition until the data is loaded. $\overline{IRQ}$ interrupts continue to occur at the same rate as previously, except no data is transmitted. When the processor finally loads new data, a Start Bit immediately occurs, the data word transmission is started, and another interrupt is initiated, signaling for the next data word. Figure 7 shows the timing relationship for this mode of operation.

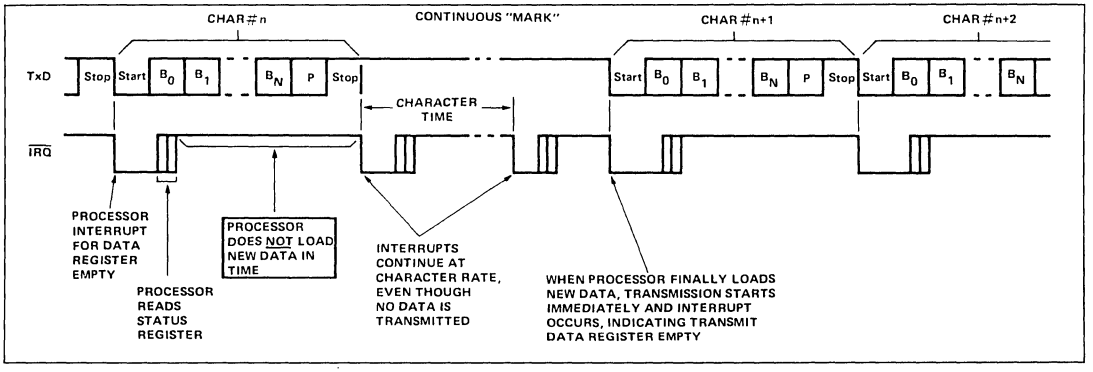


Figure 7. Transmit Data Register Not Loaded by Processor

Effect of $\overline{CTS}$ on Transmitter

$\overline{CTS}$ is the Clear-to-Send Signal generated by the modem. It is normally low (true state) but may go high in the event of some modem problems. When this occurs, the TxD line immediately goes to the "MARK" condition. Interrupts continue at the same rate, but the Status Register does not indicate that the Transmit Data Register is empty. Since there is no status bit for $\overline{CTS}$, the processor must deduce that $\overline{CTS}$ has gone to the FALSE (high) state. $\overline{CTS}$ is a transmit control line only, and has no effect on the R6551 Receiver Operation. Figure 8 shows the timing relationship for this operation.

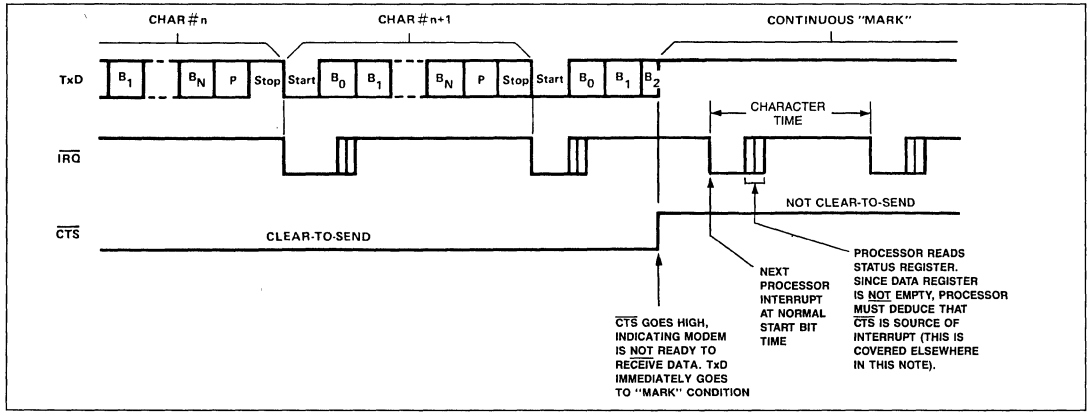


Figure 8. Effect of CTS on Transmitter

Effect of Overrun on Receiver

If the processor does not read the Receiver data Register in the allocated time, then, when the next interrupt occurs, the new data word is not transferred to the Receiver Data Register, but the Overrun status bit is set. Thus, the Data Register will contain the last valid data word received and all following data is lost. Figure 9 shows the timing relationship for this mode.

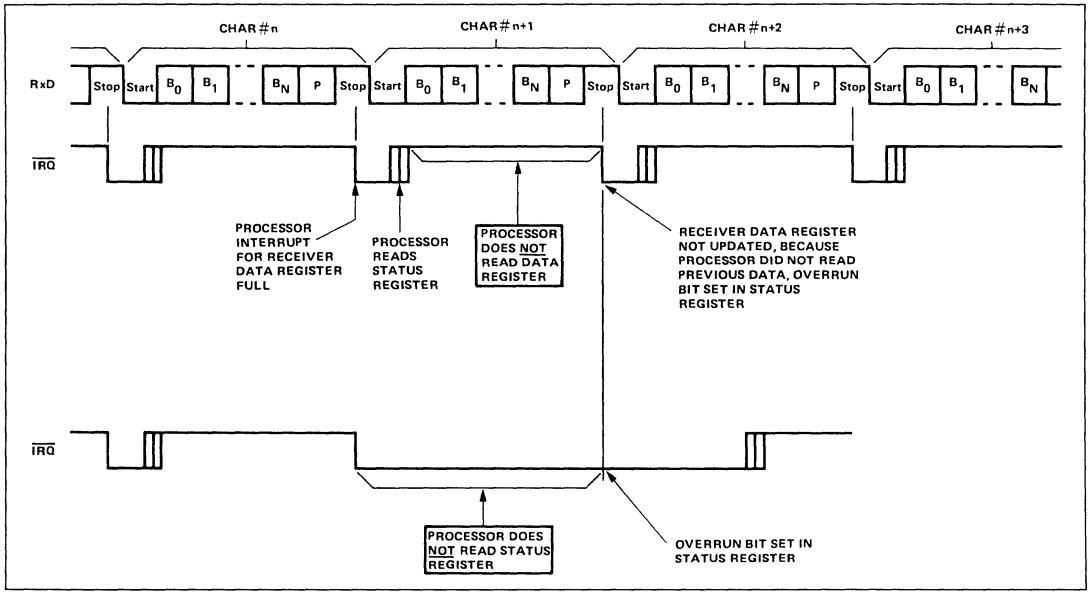


Figure 9. Effect of Overrun on Receiver

Echo Mode Timing

In Echo Mode, the TxD line re-transmits the data on the RxD line, delayed by ½ of the bit time, as shown in Figure 10.

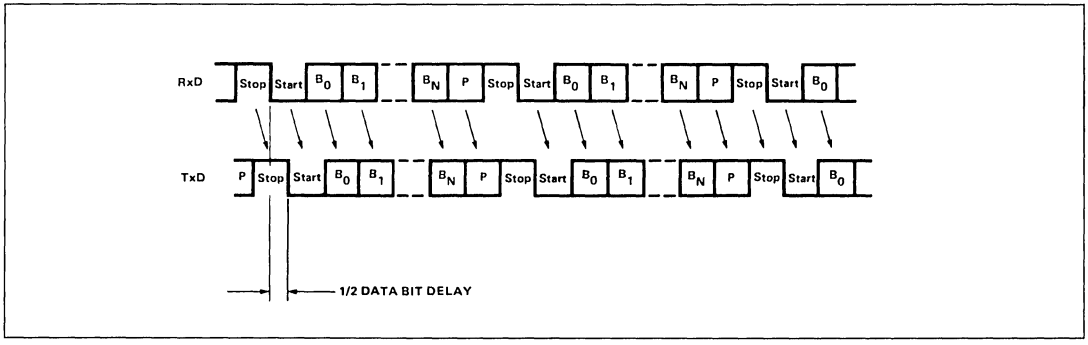


Figure 10. Echo Mode Timing

Effect of $\overline{CTS}$ on Echo Mode Operation

In Echo Mode, the Receiver operation is unaffected by $\overline{CTS}$, however, the Transmitter is affected when $\overline{CTS}$ goes high, i.e., the TxD line immediately goes to a continuous "MARK" condition. In this case, however, the Status Request indicates that the Receiver Data Register is full in response to an $\overline{IRQ}$, so the processor has no way of knowing that the Transmitter has ceased to echo. See Figure 11 for the timing relationship of this mode.

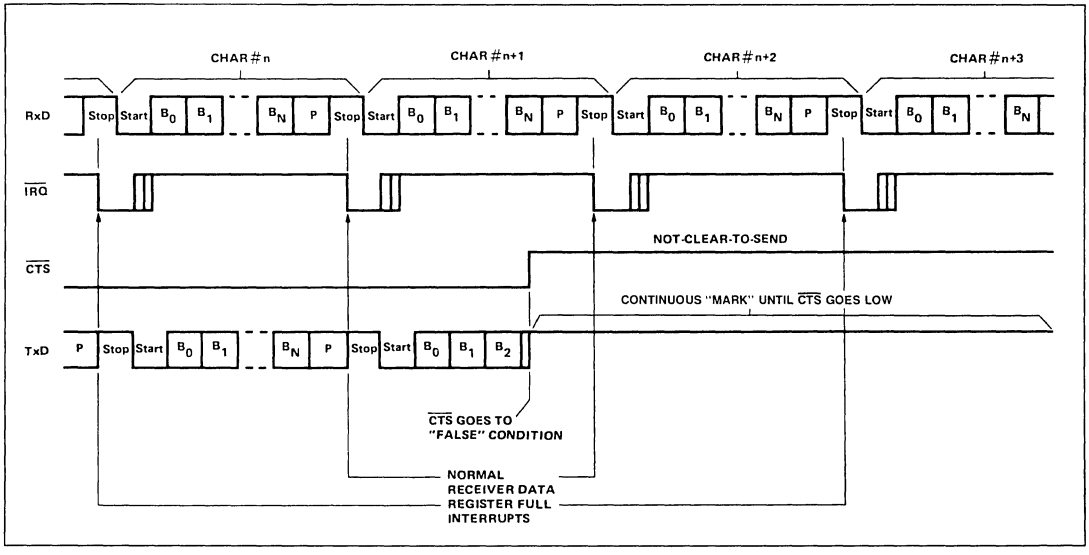


Figure 11. Effect of $\overline{CTS}$ on Echo Mode

Overrun in Echo Mode

If Overrun occurs in Echo Mode, the Receiver is affected the same way as a normal overrun in Receive Mode. For the re-transmitted data, when overrun occurs, the TxD line goes to the "MARK" condition until the first Start Bit after the Receiver Data Register is read by the processor. Figure 12 shows the timing relationship for this mode.

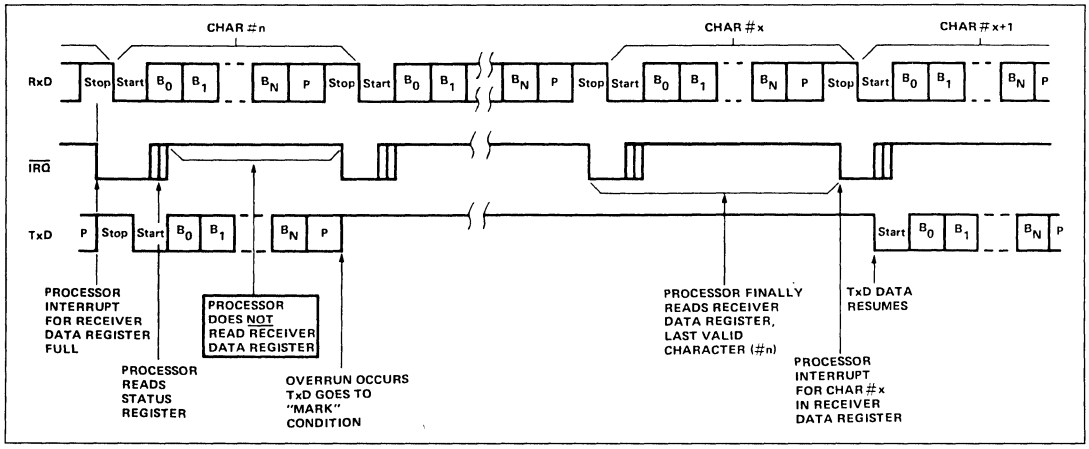


Figure 12. Overrun in Echo Mode

Framing Error

Framing Error is caused by the absence of Stop Bit(s) on received data. A Framing Error is indicated by the setting of bit 1 in the Status Register at the same time the Receiver Data Register Full bit is set, also in the Status Register. In response to IRQ, generated by RDRF, the Status Register can also be checked for the Framing Error. Subsequent data words are tested for Framing Error separately, so the status bit will always reflect the last data word received. See Figure 13 for Framing Error timing relationship.

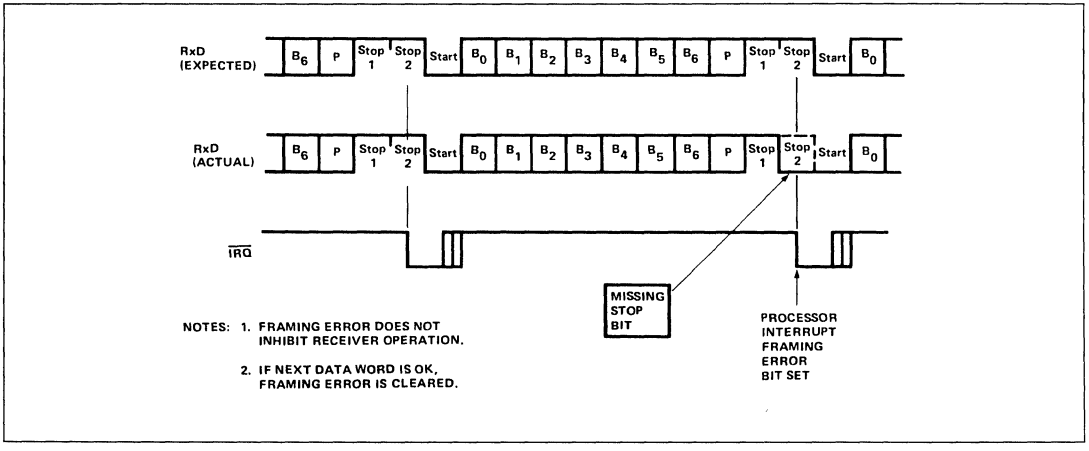


Figure 13. Framing Error

Effect of $\overline{DCD}$ on Receiver

$\overline{DCD}$ is a modem output indicating the status of the carrier-frequency-detection circuit of the modem. This line goes high for a loss of carrier. Normally, when this occurs, the modem will stop transmitting data some time later. The ACIA asserts $\overline{IRQ}$ whenever $\overline{DCD}$ changes state and indicates this condition via bit 5 in the Status Register.

Once such a change of state occurs, subsequent transitions will not cause interrupts or changes in the Status Register until the first interrupt is serviced. When the Status Register is read by the processor, the ACIA automatically checks the level of the $\overline{DCD}$ line, and if it has changed, another $\overline{IRQ}$ occurs (see Figure 14).

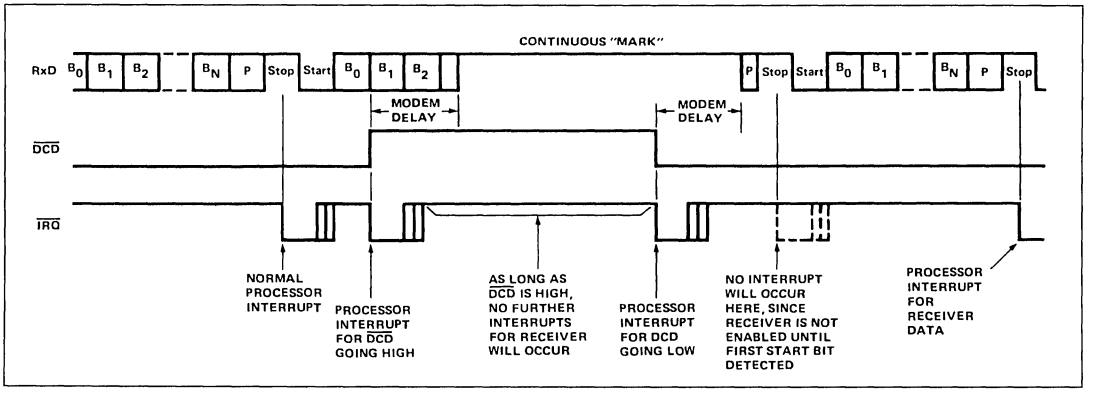


Figure 14. Effect of DCD on Receiver

Timing with 1½ Stop Bits

It is possible to select 1½ Stop Bits, but this occurs only for 5-bit data words with no parity bit. In this case, the $\overline{IRQ}$ asserted for Receiver Data Register Full occurs halfway through the trailing half-Stop Bit. Figure 15 shows the timing relationship for this mode.

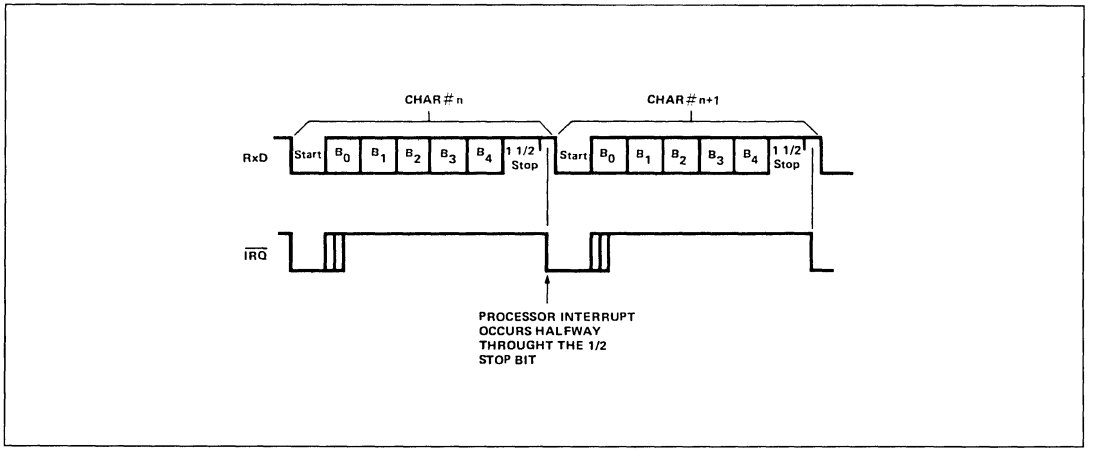


Figure 15. Timing with 1½ Stop Bits

Transmit Continuous "BREAK"

This mode is selected via the ACIA Command Register and causes the Transmitter to send continuous "BREAK" characters, beginning with the next character transmitted. At least one full "BREAK" character will be transmitted, even if the processor quickly re-programs the Command Register transmit mode. Later, when the Command Register is programmed back to normal transmit mode, an immediate Stop Bit will be generated and transmission will resume. Figure 16 shows the timing relationship for this mode.

Note

If, while operating in the Transmit Continuous "BREAK" mode, the $\overline{CTS}$ should go to a high, the TxD will be overridden by the $\overline{CTS}$ and will go to continuous "MARK" at the beginning of the next character transmitted after the $\overline{CTS}$ goes high.

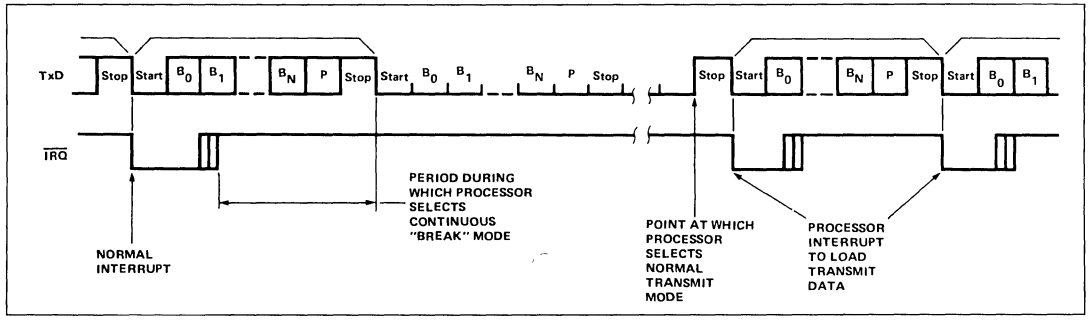


Figure 16. Transmit Continuous "BREAK"

Receive Continuous "BREAK"

In the event the modem transmits continuous "BREAK" characters, the ACIA will terminate receiving. Reception will resume only after a Stop Bit is encountered by the ACIA. Figure 17 shows the timing relationship for continuous "BREAK" characters.

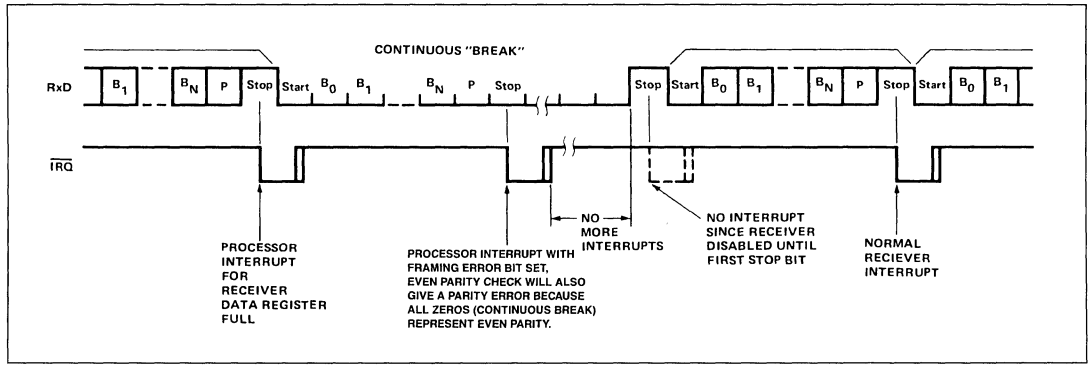


Figure 17. Receive Continuous "BREAK"

STATUS REGISTER OPERATION

Because of the special functions of the various status bits, there is a suggested sequence for checking them. When an interrupt occurs, the ACIA should be interrogated, as follows:

1. Read Status Register

   This operation automatically clears Bit 7 ($\overline{IRQ}$). Subsequent transitions on $\overline{DSR}$ and $\overline{DCD}$ will cause another interrupt.

2. Check IRQ (Bit 7) in the data read from the Status Register

   If not set, the interrupt source is not the ACIA.

3. Check $\overline{DCD}$ and $\overline{DSR}$

   These must be compared to their previous levels, which must have been saved by the processor. If they are both 0 (modem "on-line") and they are unchanged then the remaining bits must be checked.

4. Check RDRF (Bit 3)

   Check for Receiver Data Register Full.

5. Check Parity, Overrun, and Framing Error (Bits 0-2) if the Receiver Data Register is full.

6. Check TDRE (Bit 4)

   Check for Transmitter Data Register Empty.

7. If none of the above conditions exist, then $\overline{CTS}$ must have gone to the false (high) state.

PROGRAM RESET OPERATION

A program reset occurs when the processor performs a write operation to the ACIA with RS0 low and RS1 high. The program reset operates somewhat different from the hardware reset ($\overline{RES}$ pin) and is described as follows:

1. Internal registers are not completely cleared. Check register formats for the effect of a program reset on internal registers.

2. The $\overline{DTR}$ line goes high immediately.

3. Receiver and transmitter interrupts are disabled immediately. If $\overline{IRQ}$ is low when the reset occurs, it stays low until serviced, unless interrupt was caused by $\overline{DCD}$ or $\overline{DSR}$ transition.

4. $\overline{DCD}$ and $\overline{DSR}$ interrupts are disabled immediately. If $\overline{IRQ}$ is low and was caused by $\overline{DCD}$ or $\overline{DSR}$, then it goes high, also $\overline{DCD}$ and $\overline{DSR}$ status bits subsequently will follow the input lines, although no interrupt will occur.

5. Overrun cleared, if set.

MISCELLANEOUS

1. If Echo Mode is selected, $\overline{RTS}$ goes low.

2. If Bit 0 of Command Register ($\overline{DTR}$) is 0 (disabled), then:

   a) All interrupts are disabled, including those caused by $\overline{DCD}$ and $\overline{DSR}$ transitions.
   b) Transmitter is disabled immediately.
   c) Receiver is disabled, but a character currently being received will be completed first.

3. Odd parity occurs when the sum of all the 1 bits in the data word (including the parity bit) is odd.

4. In the receive mode, the received parity bit does not go into the Receiver Data Register, but generates parity error or no parity error for the Status Register.

5. Transmitter and Receiver may be in full operation simultaneously. This is "full-duplex" mode.

6. If the RxD line inadvertently goes low and then high right after a Stop Bit, the ACIA does not interpret this as a Start Bit, but samples the line again halfway into the bit time to determine if it is a true Start Bit or a false one. For false Start Bit detection, the ACIA does not begin to receive data, instead, only a true Start Bit initiates receiver operation.

7. $\overline{DCD}$ andd $\overline{DSR}$ transitions, although causing immediate processor interrupts, have no affect on transmitter operation. Data will continue to be sent, unless the processor forces transmitter to turn off. Since these are high-impedance inputs, they must not be permitted to float (un-connected). If unused, they must be terminated to GND.

CRYSTAL/CLOCK CONSIDERATIONS

CLOCK OSCILLATOR

The on-chip oscillator is designed for a series resonant crystal connected between XTLI and XTLO pins (Figure 18).

A series resonant crystal is specified by the series resistance (R_S) at its series resonant frequency. For proper oscillator operation, the selected series resonant crystal should have a series resistance less than 400 ohms.

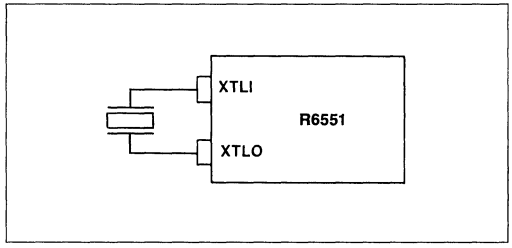


Figure 18. Internal Clock Connection

EXTERNAL CLOCK

The XTLI input may be used as an external clock input (Figure 19). For this implementation, a times 16 clock is input on XTLI and XTLO is left open.

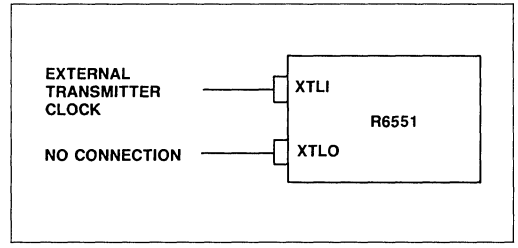


Figure 19. External Clock Connection

BAUD RATE GENERATION

DIVISORS

The internal counter/divider circuit generates appropriate divisors to produce standard baud rates when a 1.8432 MHz crystal is connected between XTLI and XTLO. Control Register bits 0-3 select the divisor for a particular bit rate as shown in Table 2.

GENERATING NON-STANDARD BAUD RATES

By using a different crystal, non-standard baud rates may be generated. These can be determined by:

$$\text{Baud Rate} = \frac{\text{Crystal Frequency}}{\text{Divisor}}$$

Furthermore, it is possible to drive the ACIA with an off-chip oscillator to achieve other baud rates. In this case, XTALI (pin 6) must be the clock input and XTALO (pin 7) must be a no-connect.

Table 2. Divisor Selection

Control Register Bits 3 2 1 0	Divisor Selected For The Internal Counter	Baud Rate Generated With 1.8432 MHz Crystal	Baud Rate Generated With a Crystal of Frequency (F)
0 0 0 0	No Divisor Selected	16 x External Clock at Pin RxC	16 x External Clock at Pin RxC
0 0 0 1	36,864	$1.8432 \times 10^6 / 36{,}864 = 50$	F / 36,864
0 0 1 0	24,576	$1.8432 \times 10^6 / 24{,}576 = 75$	F / 24,576
0 0 1 1	16,769	$1.8432 \times 10^6 / 16{,}769 = 109.92$	F / 16,769
0 1 0 0	13,704	$1.8432 \times 10^6 / 13{,}704 = 134.51$	F / 13,704
0 1 0 1	12,288	$1.8432 \times 10^6 / 12{,}288 = 150$	F / 12,288
0 1 1 0	6,144	$1.8432 \times 10^6 / 6{,}144 = 300$	F / 6,144
0 1 1 1	3,072	$1.8432 \times 10^6 / 3{,}072 = 600$	F / 3,072
1 0 0 0	1,536	$1.8432 \times 10^6 / 1{,}536 = 1{,}200$	F / 1,536
1 0 0 1	1,024	$1.8432 \times 10^6 / 1{,}024 = 1{,}800$	F / 1,024
1 0 1 0	768	$1.8432 \times 10^6 / 768 = 2{,}400$	F / 768
1 0 1 1	512	$1.8432 \times 10^6 / 512 = 3{,}600$	F / 512
1 1 0 0	384	$1.8432 \times 10^6 / 384 = 4{,}800$	F / 384
1 1 0 1	256	$1.8432 \times 10^6 / 256 = 7{,}200$	F / 256
1 1 1 0	192	$1.8432 \times 10^6 / 192 = 9{,}600$	F / 192
1 1 1 1	96	$1.8432 \times 10^6 / 96 = 19{,}200$	F / 96

DIAGNOSTIC LOOP-BACK OPERATING MODES

A simplified block diagram for a system incorporating an ACIA is shown in Figure 20.

It may be desirable to include in the system a facility for local loop-back testing.

In loop-back testing from the point of view of the processor, the Modem and Data Link must be effectively disconnected and the ACIA transmitter connected back to its own receiver, so that the processor can perform diagnostic checks on the system, excluding the actual data channel.

The ACIA does not contain automatic loop-back operating modes, but they may be implemented with the addition of a small amount of external circuitry. Figure 21 indicates the necessary logic to be used with the ACIA. The LLB line is the positive-true signal to enable local loop-back operation. Essentially, LLB = high does the following:

1. Disables outputs TxD, $\overline{DTR}$, and $\overline{RTS}$ (to Modem).
2. Disables outputs RxD, $\overline{DCD}$, $\overline{CTS}$, $\overline{DSR}$ (from Modem).
3. Connects transmitter outputs to respective receiver inputs (i.e. TxD to RxD, $\overline{DTR}$ to $\overline{DCD}$, $\overline{RTS}$ to $\overline{CTS}$).

LLB may be tied to a peripheral control pin (from an R6520 or R6522, for example) to provide processor control of local loop-back operation. In this way, the processor can easily perform local loop-back diagnostic testing.

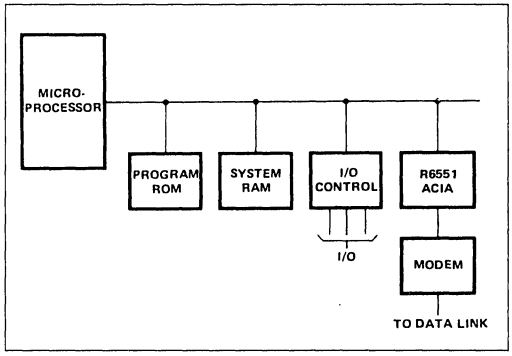


Figure 20. Simplified System Diagram

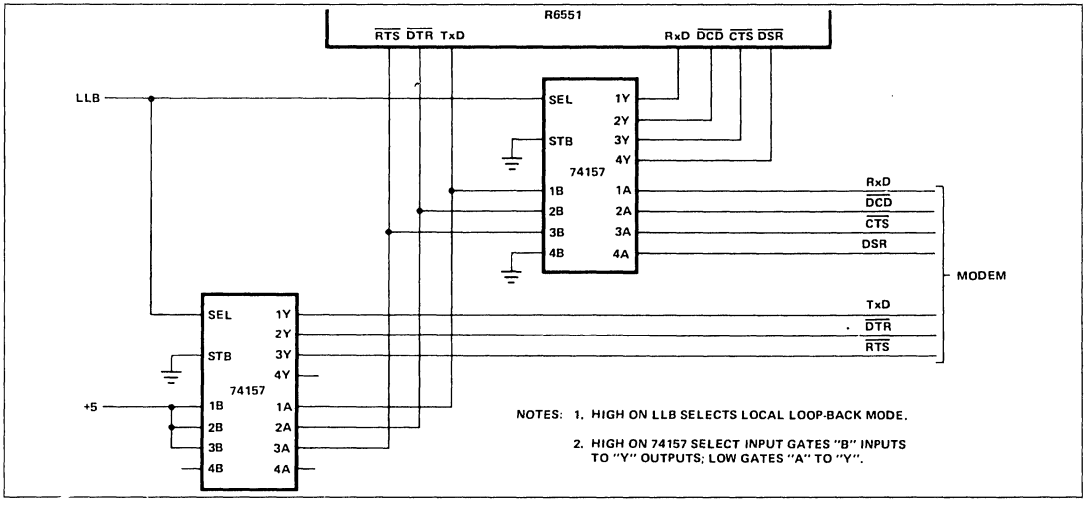


Figure 21. Loop-Back Circuit Schematic

READ TIMING DIAGRAM

Timing diagrams for transmit with external clock, receive with external clock, and $\overline{IRQ}$ generation are shown in Figures 22, 23 and 24, respectively. The corresponding timing characteristics are listed in the Table 3.

Table 3. Transmit/Receive Characteristics

Characteristic	Symbol	1 MHz		2 MHz		Unit
		Min	Max	Min	Max	
Transmit/Receive Clock Rate	t_{CCY}	400*	—	400*	—	ns
Transmit/Receive Clock High Time	t_{CH}	175	—	175	—	ns
Transmit/Receive Clock Low Time	t_{CL}	175	—	175	—	ns
XTLI to TxD Propagation Delay	t_{DD}	—	500	—	500	ns
RTS Propagation Delay	t_{DLY}	—	500	—	500	ns
$\overline{IRQ}$ Propagation Delay (Clear)	t_{IRQ}	—	500	—	500	ns
Load Capacitance $\overline{DTR}$, RTS TxD	C_L	 — —	 130 30	 — —	 130 30	 pF pF

Notes:
(t_R, t_F = 10 to 30 ns)

*The baud rate with external clocking is: Baud Rate = $\frac{1}{16 \times t_{CCY}}$

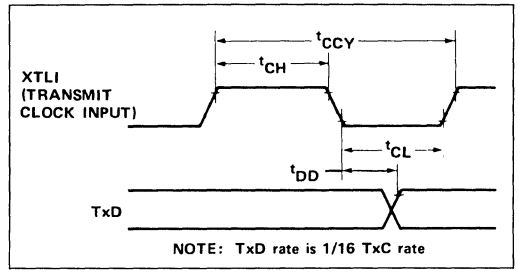


Figure 22. Transmit Timing with External Clock

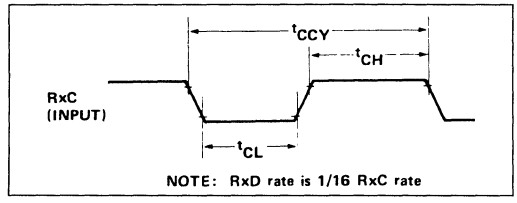


Figure 23. Receive External Clock Timing

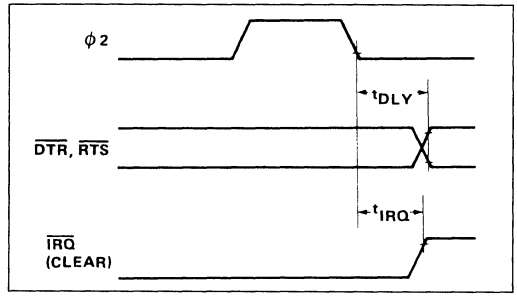


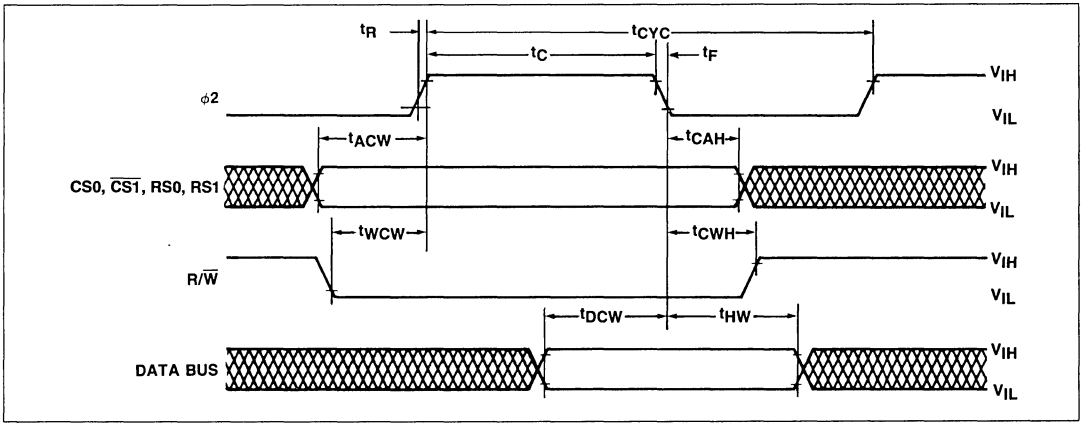
Figure 24. Interrupt and Output Timing

AC CHARACTERISTICS

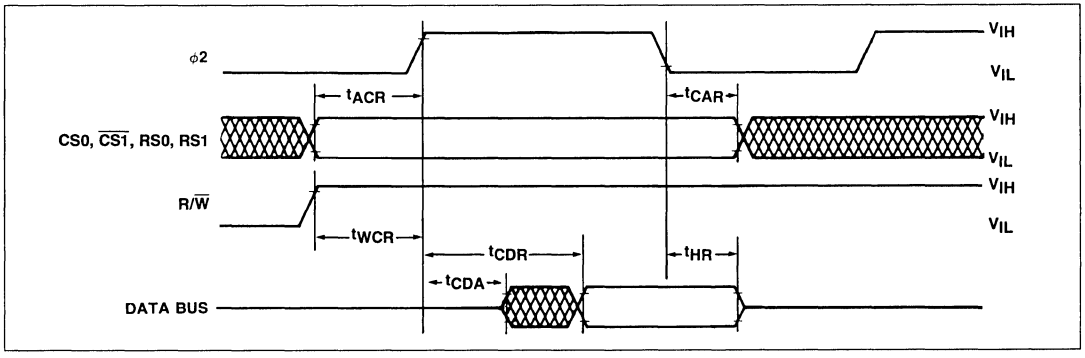
(V_{CC} = 5.0V ± 5%, V_{SS} = 0, T_A = T_L to T_H, unless otherwise noted)

Parameter	Symbol	1 MHz		2 MHz		Unit
		Min	Max	Min	Max	
Cycle Time	t_{CYC}	1.0	40	0.5	40	μs
Ø2 Pulse Width	t_C	400	—	200	—	ns
Address Set-Up Time	t_{ACW}, t_{ACR}	120	—	70	—	ns
Address Hold Time	t_{CAH}, t_{CAR}	0	—	0	—	ns
R/$\overline{W}$ Set-Up Time	t_{WCW}, t_{WCR}	120	—	70	—	ns
R/$\overline{W}$ Hold Time	t_{CWH}	0	—	0	—	ns
Data Bus Set-Up Time	t_{DCW}	150	—	60	—	ns
Data Bus Hold Time	t_{HW}	20	—	20	—	ns
Read Access Time (Valid Data)	t_{CDR}	—	200	—	150	ns
Read Hold Time	t_{HR}	20	—	20	—	ns
Bus Active Time (Invalid Data)	t_{CDA}	40	—	40	—	ns

Notes: 1. t_R and t_F = 10 to 30 ns.
2. D0-D7 load capacitance = 130 pF.
3. Timing measurements are referenced to/from a low of 0.8 volts and a high of 2.0 volts.



Write Timing Diagram



Read Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to +7.0	Vdc
Input Voltage	V_{IN}	−0.3 to V_{CC}	Vdc
Output Voltage	V_{OUT}	−0.3 to V_{CC}	Vdc
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{STG}	−55 to +150	°C

***NOTE:** Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in other sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING CONDITIONS

Parameter	Symbol	Value
Supply Voltage	V_{CC}	5V ±5%
Temperature Range Commercial Industrial	T_A	 0° to 70°C −40°C to +85°C

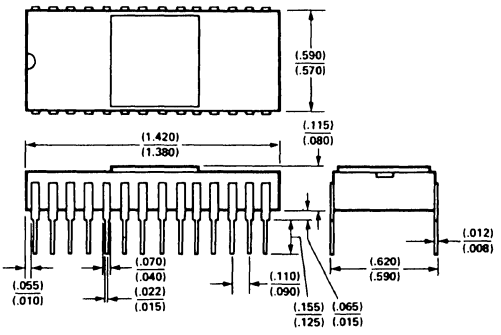
DC CHARACTERISTICS

(V_{CC} = 5.0V ± 5%, V_{SS} = 0, T_A = T_L to T_H, unless otherwise noted)

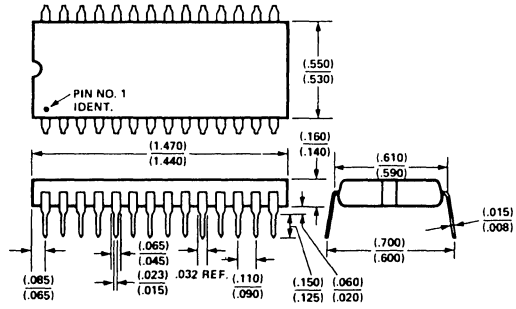
Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input High Voltage Except XTLI and XTLO XTLI and XTLO	V_{IH}	 2.0 2.4	 — —	 V_{CC} V_{CC}	V	
Input Low Voltage Except XTLI and XTLO XTLI and XTLO	V_{IL}	 V_{SS} V_{SS}	 — —	 0.8 0.4	V	
Input Leakage Current Ø2, R/W, RES, CS0, CS1, RS0, RS1, CTS, RxD, DCD, DSR	I_{IN}	—	—	2.5	μA	V_{IN} = 0V to 5V V_{CC} = 0V
Input Leakage Current for High Impedance (Three State Off) D0–D7	I_{TSI}	—	—	±10.0	μA	V_{IN} = 0.4V to 2.4V V_{CC} = 5.25V
Output High Voltage D0-D7, TxD, RxC, RTS, DTR	V_{OH}	2.4	—	—	V	I_{LOAD} = −100 μA V_{CC} = 4.75V
Output Low Voltage D0-D7, TxD, RxC, RTS, DTR, IRQ	V_{OL}	—	—	0.4	V	V_{CC} = 4.75V I_{LOAD} = 1.6 mA
Output High Current (Sourcing) D0-D7, TxD, RxC, RTS, DTR	I_{OH}	−100	—	—	μA	V_{OH} = 2.4V
Output Low Current (Sinking) D0-D7, TxD, RxC, RTS, DTR, IRQ	I_{OL}	1.6	—	—	mA	V_{OL} = 0.4V
Output Leakage Current (off state) IRQ	I_{OFF}	—	—	10.0	μA	V_{OUT} = 5V
Clock Capacitance (Ø2)	C_{CLK}	—	—	20	pF	V_{CC} = 5V V_{IN} = 0V f = 1 MHz T_A = 25°C
Input Capacitance except Ø2, XTLI, XTLO	C_{IN}	—	—	10	pF	
Output Capacitance	C_{OUT}	—	—	10	pF	
Power Dissipation	P_D	—	170	300	mW	T_A = 0°C

PACKAGE DIMENSIONS

28-PIN CERAMIC DIP



28-PIN PLASTIC DIP



2

Section 3
8-Bit Microcomputers

CMOS and NMOS 8-Bit Microcomputers
Highest Industry Performers

The R6500 single-chip CMOS and NMOS microcomputers provide high-speed and low CMOS power while being completely software compatible with the 8-bit multi-chip family. They let you move easily from a multi-chip to a single-chip solution when the application warrants. They also function as intelligent peripheral controllers. The R65C10, a CMOS version of the R6500/1, combines the low power of CMOS with advanced pipelining architecture to provide an efficient high-speed single-chip system solution.

Features of the microcomputer family include 1.5K to 4K bytes of ROM, 64 to 192 bytes of RAM, 23 to 56 I/O ports, multiple use counter/timers, serial communication channels, bit manipulation instructions, expansion bus, multiple bus interfaces, directly executable RAM with low power standby, and multiple interrupts — all from a single 5V power supply. They are also available in ROM-less versions, for large memory system applications and for developing and simulating products in prototype, with external memory.

And, the R65F11 and R65F12 even have all system software on the chip, including an operating system and high-level FORTH language. It is an extremely versatile microcomputer, and is available in three configurations to accommodate application programs to 48K.

FEATURE/MODELS	R6500/1	R6500/11	R6500/12	R6500/13	R6500/15	R65C10
• INSTRUCTION SPEED	1000ns	1000ns	1000ns	1000ns	1000ns	500ns
• ROM (x8)	2K	3K	3K	256	4K	2K
• RAM (x8)	64	192	192	192	192	64
• I/O LINES	32	32	56	32	32	32
• SERIAL COMM.	—	USART	USART	USART	UART	—
• 16-BIT COUNTERS	ONE	TWO	TWO	TWO	TWO	ONE
• EXPANSION BUS	—	16K	16K	65K	16K	—
• INTERRUPTS						
— EXTERNAL	5	6	6	6	6	5
— INTERNAL	1	4	4	4	4	1
• OPERATING POWER (mW)	750	800	800	800	800	40
• STANDBY (mW)	35*	12*	12*	12*	12*	12
• PACKAGE	40 DIP 44 PLCC	40 DIP 44 PLCC	64 QUIP 68 PLCC	64 QUIP 68 PLCC	40 DIP 44 PLCC	40 DIP 44 PLCC

* Standby RAM

Rockwell Microcomputers

Rockwell

R65C10
One-Chip Microcomputer

SECTION I
INTRODUCTION

SUMMARY

The Rockwell R65C10 microcomputer is a complete 8-bit computer fabricated on a single chip using an N-well silicon gate CMOS process. The R65C10 complements an industry standard line of R6500 and R65C00 microprocessors, R6500/* and R65C00/* microcomputers and compatible peripheral devices. The R65C10 has a wide range of microcomputer applications where high 8-bit performance, minimal chip count and low power consumption is required.

The R65C10 consists of a 6502 Central Processing Unit (CPU), 2048 bytes of mask programmable Read Only Memory (ROM), 64 bytes of Random Access Memory (RAM) and interface circuitry for peripheral devices. The parallel interface consists of four 8-bit ports including two edge detect lines. A 16-bit counter/timer with four selectable modes is also included.

The innovative architecture and the demonstrated high performance of the R65C02 CPU, as well as instruction simplicity, result in system cost-effectiveness and a wide range of computational power. These features make the R65C10 a leading candidate for low-power single-chip microcomputer applications.

Hardware enhancements of the R65C10 include a software-controlled system and/or counter/timer clock prescaler, and an ultra-low-power Stop mode.

This description assumes that the reader is familiar with the R6502 CPU programming capabilities as described in the R6500 Programming Manual (Order No. 202).

ORDERING INFORMATION

R65C10

- Temperature Range
  - No letter = 0°C to +70°C
  - E = −40°C to +85°C
- Operating Frequency (Internal Ø2 clock)
  - 1 = 1 MHz
  - 2 = 2 MHz
  - 3 = 3 MHz
  - 4 = 4 MHz
- Package
  - C = 40-pin CERDIP
  - P = 40-pin Plastic DIP
  - J = 44-pin Plastic Leaded Chip Carrier (PLCC)

FEATURES

- Single-chip microcomputer
- R6502 CPU instruction compatible
- 8-bit parallel processing
- Decimal or binary arithmetic
- Variable length stack
- True indexing capability
- 13 addressing modes
- Internal 1 MHz to 4 MHz clock with crystal or clock input
  - — Internal divide-by-2 network
  - — 2 MHz to 8 MHz crystal input
  - — 20 kHz to 8 MHz clock input
- Software-controllable prescaler
  - — Selectable system clock and timer clock prescaler or timer clock only prescaler
  - — Divide by 8, 32, 64, or 128 options
- Low-power oscillator Stop mode (cleared by $\overline{RES}$)
- 15 mW to 60 mW operating power (1 MHz to 4 MHz)
- 2K × 8 ROM on-chip
- 64 × 8 RAM on-chip
- 32 bidirectional TTL compatible I/O lines
  - — 1 positive edge-sensitive I/O line
  - — 1 negative edge-sensitive I/O line
- 1 bidirectional TTL compatible counter I/O line
- 16-bit buffered timer/counter with four modes
  - — Interval timer
  - — Pulse generator
  - — Event counter
  - — Pulse width measurement
- Three maskable interrupt requests (IRQ)
  - — 1 counter overflow
  - — 2 I/O edge detect
- $\overline{NMI}$ and $\overline{RES}$ inputs
- Available in 40-pin DIP and 44-pin PLCC packages
- +5V ±10% power

SECTION 2
INTERFACE DESCRIPTION

This section describes the interface requirements for the R65C10 single-chip microcomputer. An interface diagram for the R65C10 is shown in Figure 2-1. The R65C10 pin assignments are identified in Figure 2-2. The function of each pin of the R65C10 is explained in Table 2-1.

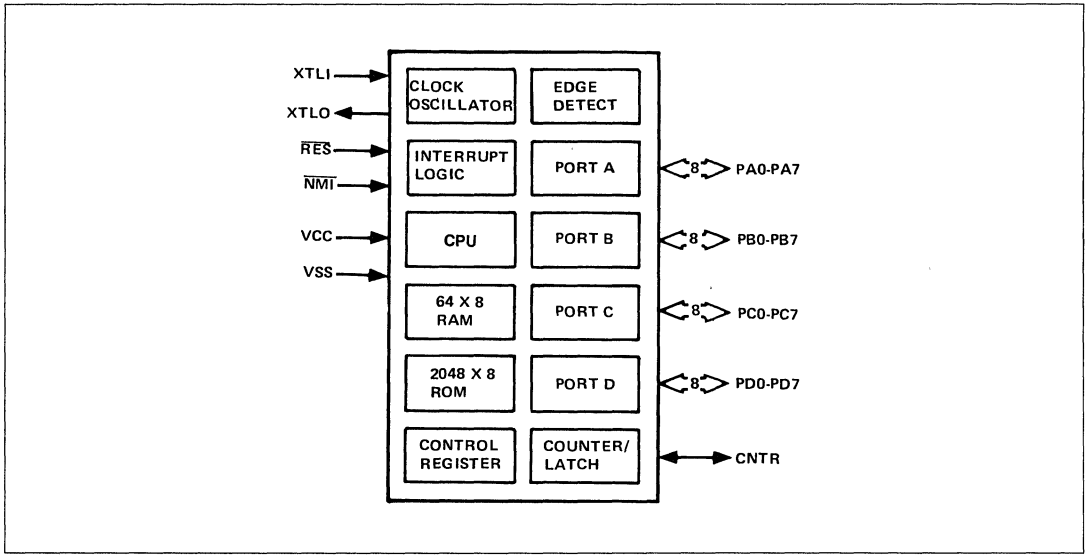


Figure 2-1. R65C10 Interface Diagram

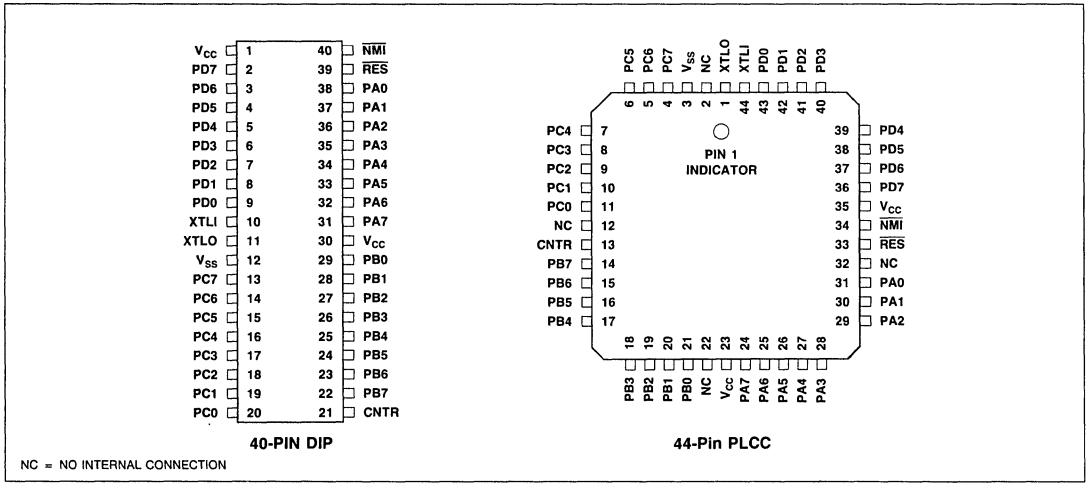


Figure 2-2. R65C10 Pin Assignments

Table 2-1. R65C10 Pin Description

Signal Name	I/O	Description
V_{CC}		**POWER**. +5 Vdc; must be connected to both pins.
V_{SS}		**GROUND**. Signal return and power ground (0V).
XTLI	I	**CRYSTAL INPUT**. The crystal or external clock input to the internal clock oscillator. The oscillator generates the internal master clock at the frequency of the input crystal/clock divided either by 1 or by 2 depending upon mask option. The system and counter/timer clocks are derived from the master clock under control of the Prescaler Control Register.
XTLO	O	**CRYSTAL OUTPUT**. The crystal output from the internal clock oscillator. XTLO should be left open when a clock is input at XTLI.
$\overline{RES}$	I	**RESET**. The active low $\overline{RES}$ input initializes the R65C10. This signal must not transition from low to high for at least eight cycles after V_{CC} reaches operating range and the internal oscillator has stabilized.
$\overline{NMI}$	I	**NON-MASKABLE INTERRUPT**. A negative-going edge on the $\overline{NMI}$ input interrupts the CPU.
PA0–PA7	I/O	**PORT A**. General purpose I/O Port A.
PB0–PB7	I/O	**PORT B**. General purpose I/O Port B.
PC0–PC7	I/O	**PORT C**. General purpose I/O Port C.
PD0–PD7	I/O	**PORT D**. General purpose I/O Port D.
		Four 8-bit ports used for either input or output. Each line consists of an active transistor to V_{SS} and an optional active pull-up to V_{CC} (see Section 4.3). The two lower bits of the Port A (PA0 and PA1) also serve as edge-detect inputs with maskable interrupts. PA0 detects a positive-going edge and PA1 detects a negative-going edge.
CNTR	I/O	**COUNTER**. This line is either an input to, or an output from, the counter. CNTR is an input in the event counter and pulse width measurement modes, and is an output in the pulse generator modes. It consists of an active transistor to V_{SS} and an optional active pull-up to V_{CC}.

SECTION 3
SYSTEM ARCHITECTURE

This section provides a functional description of the R65C10. A block diagram of the R65C10 is presented in Figure 3-1.

3.1 INDEX REGISTERS

There are two 8-bit index registers: X and Y. Either index register can be used as a base to modify the program counter contents and thus obtain a new address—the sum of the program counter contents and the index register contents.

When executing an instruction which specifies indexed addressing, the CPU fetches the op code and the address, and modifies the address from memory by adding the index register to it prior to loading or storing the value of memory.

3.2 STACK POINTER

The Stack Pointer is an 8-bit register. It is automatically incremented and decremented under control of the CPU to perform stack manipulation in response to program instructions, the $\overline{\text{NMI}}$ interrupt input or the internally generated IRQ interrupt. The Stack Pointer must be initialized by the user program. The JSR, BRK, RTI, and RTS instructions use the stack and the Stack Pointer. The stack is located in RAM from address 0 to address $3F (0 to 63 decimal).

3.3 ARITHMETIC AND LOGIC UNIT (ALU)

All arithmetic and logic operations take place in the ALU, including incrementing and decrementing internal registers (except the Program Counter). The ALU cannot store data for more than one cycle. If data is placed on the inputs to the ALU at the beginning of a cycle, the result is always gated into one of the storage registers or to memory during the next cycle.

Each bit of the ALU has two inputs. These inputs can be tied to various internal buses or to a logic 0; the ALU then generates the function (AND, OR, SUM, and so on) using the data on the two inputs.

3.4 ACCUMULATOR

The Accumulator is a general purpose 8-bit register that stores the results of most arithmetic and logic operations. In addition, the Accumulator usually contains one of the two data words used in these operations.

3.5 PROGRAM COUNTER

The 12-bit Program Counter provides the addresses that step the processor through sequential instructions in a program. Each time the processor fetches an instruction from the program memory, the lower (least significant) byte of the Program Counter (PCL) is placed on the eight low-order lines of the internal address bus and the higher (most significant) byte of the Program Counter (PCH) is placed on the four high-order lines of the internal address bus. The Program Counter is incremented each time an instruction or data is fetched from program memory.

3.6 INSTRUCTION REGISTER AND INSTRUCTION DECODE

Instructions are fetched from ROM or RAM and gated onto the internal data bus. These instructions are latched into the Instruction Register, then decoded along with timing and interrupt signals to generate control signals for the various registers.

3.7 PROCESSOR STATUS REGISTER (PSR)

The 8-bit Processor Status Register, shown in Figure 3-2, contains seven status flags. Some of these flags are controlled by the user program; others may be controlled both by the user program and the CPU. The R65C10 instruction set contains a number of conditional branch instructions which allow testing of these flags. Each of the seven processor status flags is described in the following paragraphs.

CARRY (C) BIT

The Carry (C) bit can be considered as the ninth bit of an arithmetic operation. It is set to logic 1 if a carry from the eighth bit has occurred, or cleared to logic 0 of no carry occurred, as the result of arithmetic operations.

The Carry bit may be set or cleared under program control by use of the Set Carry (SEC) or Clear Carry (CLC) instruction, respectively. Other operations which affect the Carry bit are ADC, ASL, CMP, CPX, CPY, LSR, PLP, ROL, ROR, RTI, and SBC.

ZERO (Z) BIT

The Zero (Z) bit is set to logic 1 by the CPU during any data movement or by any calculation which sets all eight bits of the result to zero. This bit is cleared to logic 0 when the resultant eight bits of a data movement or calculation operation are not all zero. The R65C10 instruction set contains no instruction to specifically set or clear the Zero bit. The Zero bit is, however, affected by the following instructions: ADC, AND, ASL, BIT, CMP, CPX, CPY, DEC, DEX, DEY, EOR, INC, INX, INY, LDA, LDX, LDY, LSR, ORA, PLA, PLP, ROL, ROR, RTI, SBC, TAX, TAY, TXA, TSX, and TYA.

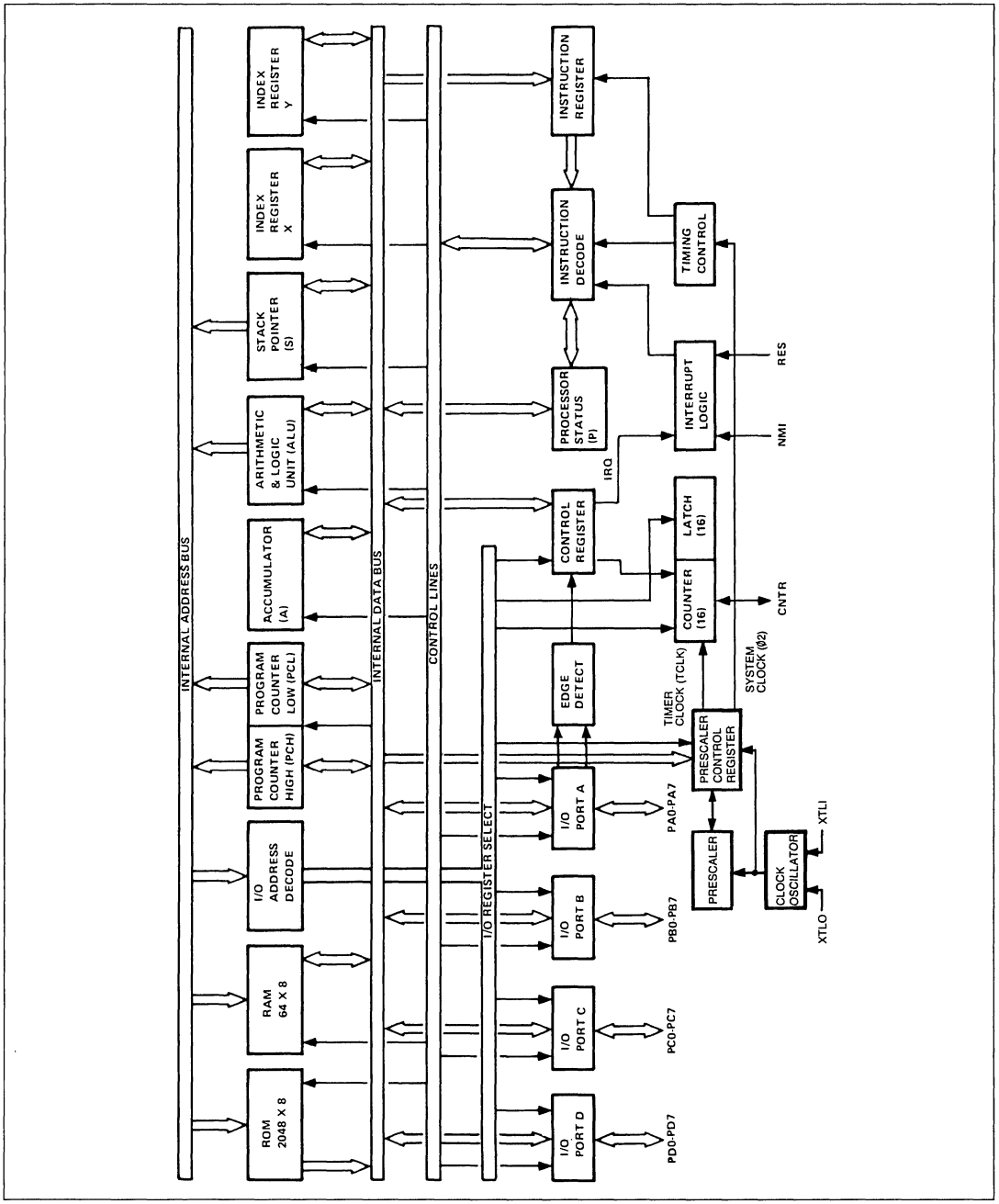
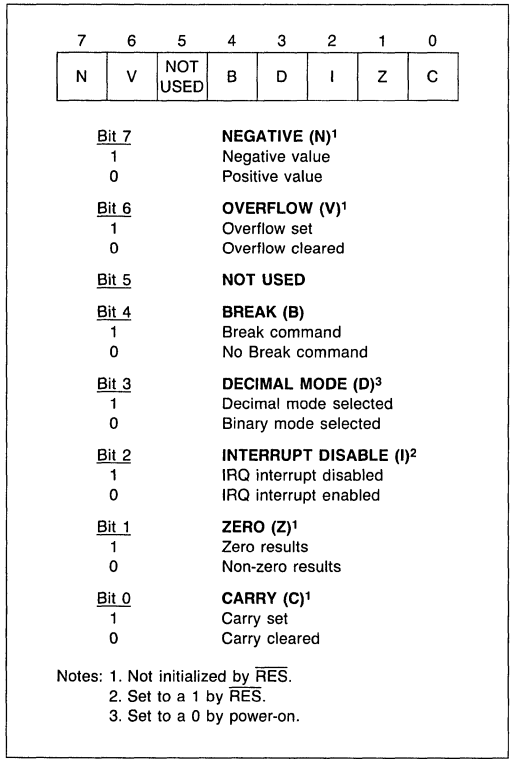


Figure 3-1. R65C10 Block Diagram



7	6	5	4	3	2	1	0
N	V	NOT USED	B	D	I	Z	C

Bit 7 — **NEGATIVE (N)[1]**
1 Negative value
0 Positive value

Bit 6 — **OVERFLOW (V)[1]**
1 Overflow set
0 Overflow cleared

Bit 5 — **NOT USED**

Bit 4 — **BREAK (B)**
1 Break command
0 No Break command

Bit 3 — **DECIMAL MODE (D)[3]**
1 Decimal mode selected
0 Binary mode selected

Bit 2 — **INTERRUPT DISABLE (I)[2]**
1 IRQ interrupt disabled
0 IRQ interrupt enabled

Bit 1 — **ZERO (Z)[1]**
1 Zero results
0 Non-zero results

Bit 0 — **CARRY (C)[1]**
1 Carry set
0 Carry cleared

Notes: 1. Not initialized by $\overline{RES}$.
2. Set to a 1 by $\overline{RES}$.
3. Set to a 0 by power-on.

Figure 3-2. Processor Status Register

INTERRUPT DISABLE (I) BIT

The Interrupt Disable (I) bit controls the servicing of the internal interrupt request (IRQ). If the I bit is reset to logic 0, the IRQ will be serviced. If the bit is set to logic 1, the IRQ will be ignored. The CPU will set the Interrupt Disable bit to logic 1 if NMI, an enabled IRQ interrupt or the $\overline{RES}$ signal is detected.

The I bit is restored by the Pull Processor Status from Stack (PLP) instruction, or as the result of executing a Return from Interrupt (RTI) instruction (provided the Interrupt Disable bit was cleared prior to the interrupt). The Interrupt Disable bit may be set or cleared under program control using a Set Interrupt Disable (SEI) or a Clear Interrupt Disable (CLI) instruction, respectively.

DECIMAL MODE (D) BIT

The Decimal Mode (D) bit controls the arithmetic mode of the CPU. When this bit is set to a logic 1, the adder operates as a decimal adder. When this bit is cleared to logic 0, the adder operates as a straight binary adder. The adder mode is controlled only by two instructions. The Set Decimal Mode (SED) instruction sets the D bit; the Clear Decimal Mode (CLD) instruction clears it. The PLP and RTI instructions also affect the Decimal Mode Bit. The Decimal Mode Bit is cleared upon power application and by $\overline{RES}$ thus establishing binary mode.

BREAK (B) BIT

The Break (B) bit indicates the condition which caused the IRQ service routine to be entered. If the IRQ service routine was entered because the CPU executed a BRK command, the B bit will be set to logic 1. If the IRQ routine was entered as the result of an IRQ occurring, the B bit will be cleared to logic 0. There are no instructions which can set or clear this bit.

OVERFLOW (V) BIT

The Overflow (V) bit indicates that the result of a signed, binary addition or subtraction operation is a value that cannot be contained in seven bits ($-128 \leq n \leq +127$). The indicator only has meaning when signed arithmetic (sign and seven magnitude bits) is performed. When the ADC or SBC instruction is performed, the V bit is set to logic 1 if the polarity of the sign bit (bit 7) is changed because the result exceeds +127 or −128; otherwise the V bit is cleared to logic 0. The V bit may also be cleared under program control by the Clear Overflow (CLV) instruction.

The Overflow bit may also be used with the BIT instruction. The BIT instruction, which may be used to sample interface devices, allows the Overflow bit to reflect the condition of Bit 6 in the sampled field. During a BIT instruction, the Overflow bit is set equal to the content of Bit 6 of the data tested with the BIT instruction. When used in this mode, the Overflow bit has nothing to do with signed arithmetic, but is just another sense bit for the CPU. Instructions which affect the V flag are ADC, BIT, CLV, PLP, RTI, and SBC.

NEGATIVE (N) BIT

The Negative (N) bit copies the arithmetic sign bit value resulting from a data movement or an arithmetic operation. If the sign bit is set, the resulting value of the data movement or arithmetic operation is negative and the N bit is a logic 1; if the sign bit is cleared, the result of the data movement or arithmetic operation is positive and the N bit is a logic 0. There are no instructions that set or clear the N bit since the N bit represents only the status of a result. The instructions that affect the state of the bit are: ADC, AND, ASL, BIT, CMP, CPX, CPY, DEC, DEX, DEY, EOR, INC, INX, INY, LDA, LDX, LDY, LSR, ORA, PLA, PLP, ROL, ROR, RTI, SBC, TAX, TAY, TSX, TXA, and TYA.

3.8 I/O ADDRESS DECODE

The internal memory, control registers, I/O ports, and Counter/Latch are memory mapped into the 4096-byte address space. The I/O Address Decode logic decodes the address from the internal address bus and routes enable signals to the appropriate functions. The memory map of the R65C10 is shown in Figure 3-3.

Parameter	Address Hex	Address Dec
IRQ Vector High	FFF	4095
IRQ Vector Low	FFE	4094
RES Vector High	FFD	4093
RES Vector Low	FFC	4092
NMI Vector High	FFB	4091
NMI Vector Low	FFA	4090
R65C10 User Program	FF9 : 800	4089 : 2048
Unassigned	7FF : 094	2047 : 148
Port D Direction Register (Write Only)[3]	093	147
Port C Direction Register (Write Only)[3]	092	146
Port B Direction Register (Write Only)[3]	091	145
Port A Direction Register (Write Only)[3]	090	144
Control Register (CR)	08F	143
Prescaler Control Register (PCR)	08E	142
Stop Mode (Write Only)[3]	08D	141
Unassigned	08C 08B	140 139
Clear PA1 Neg Edge Detected (Write Only)[1]	08A	138
Clear PA0 Pos Edge Detected (Write Only)[1]	089	137
Upper Latch and Transfer Latch to Counter, Clear Counter Overflow (Write Only)[2]	088	136
Lower Count, Clear Counter Overflow (Read Only)[2]	087	135
Upper Count (Read Only)	086	134
Lower Latch (Write Only)	085	133
Upper Latch (Write Only)	084	132
Port D (PD)	083	131
Port C (PC)	082	130
Port B (PB)	081	129
Port A (PA)	080	128
Unassigned	07F : 040	127 : 64
User RAM	03F : 000	63 : 0

Notes: 1. I/O command only; i.e., no stored data.
2. Clears Counter Overflow — Bit 7 in Control Register.
3. Mask option.

Figure 3-3. R65C10 Memory Map

3.9 2K x 8 ROM

The internal 2,048 x 8-bit Read Only Memory (ROM) usually contains the user's program instructions and other fixed constants. These program instructions and constants are mask-programmed during fabrication.

The ROM is mapped from $800 to $FFF.

3.10 64 x 8 RAM

The internal 64 x 8-bit Random Access Memory (RAM) contains the user program stack and is used for scratchpad memory during system operation. This RAM is completely static in operation and requires no clock or dynamic refresh. The data contained in RAM is read out nondestructively with the same polarity as the input data. In the event that execution stops, RAM data is retained until execution resumes.

The R65C10 RAM is assigned page zero memory address 0 to $03F.

3.11 CLOCK OSCILLATOR

The Clock Oscillator provides the basic timing signals used by the R65C10. The reference frequency is provided by an external source and can be from a crystal or clock input. The external frequency may vary from 2 MHz to 8 MHz for a parallel resonant crystal input or from 20 kHz to 8 MHz for a clock input. The external clock rate is divided by 2 or 1 to generate an internal master clock (MCLK) as shown in Figure 3-4. Selection of the input crystal/clock divide-by-2 or divide-by-1 is a mask option. The divide-by-2 option can be used with either a crystal or clock input. The divide-by-1 option can be used only with a clock input. The divide-by-2 option causes the R65C10 to operate at the same internal frequency as the R6500/1 or R6500/1E when connected to the same input clock frequency. MCLK may be prescaled by four different values under program control (discussed below).

The on-chip oscillator is designed for a parallel resonant crystal connected between XTLI and XTLO pins. The equivalent oscillator circuit is shown in Figure 3-5A.

A parallel resonant crystal is specified by its load capacitance and series resonant resistance. For proper oscillator operation, the load capacitance (C_L), series resistance (R_s) and the crystal resonant frequency (F) must meet the following two relations:

$$(C + 22) = 2C_L \quad \text{or} \quad C = 2C_L - 22$$

$$R_s \leq R_{smax} = \frac{2 \times 10^6}{(FC_L)^2}$$

where: F is in MHz; C and C_L are in pF; R is in ohms.

To select a parallel resonant crystal for the oscillator, first select the load capacitance from a crystal manufacturer's catalog. Next, calculate R_{smax} based on F and C_L. The selected crystal must have a R_s less than the R_{smax}.

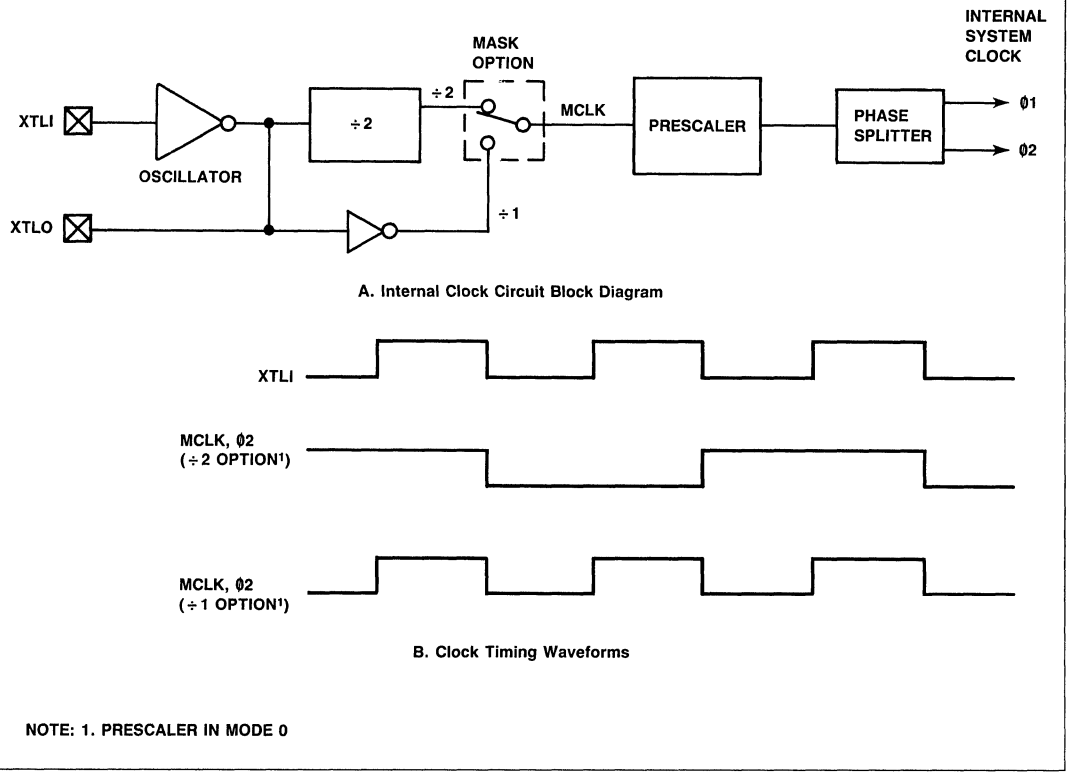


Figure 3-4. Internal System Clock Timing

For example, if C_L = 30 pF for a 4 MHz parallel resonant crystal, then

$C = (2 \times 30) - 22 = 38$ pF (Use standard value of 39 pF.)

(Note: C = Total shunt capacitance including that due to board layout.)

The series resistance of the crystal must be less than

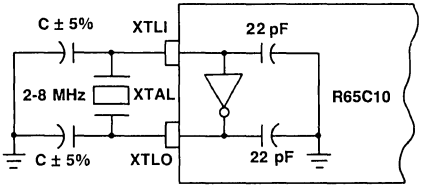
$$R_{smax} = \frac{2 \times 10^6}{(4 \times 30)^2} = 139 \text{ ohms}$$

The R65C10 internal oscillator and clock can be stopped under program control (Stop mode) and restarted by a $\overline{RES}$ input. The Stop mode is described in Section 4.

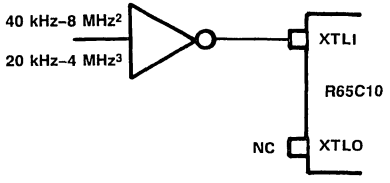
3.12 PRESCALER CONTROL

Clock prescaler mode and value selection is controlled by the Prescaler Control Register (PCR) at the address $08E (see Figure 3-6). The prescaler mode (PM) is determined by the value written to bits 0 and 1. The prescaler value (PV) is determined by the value written to bits 2 and 3. The system clock (Ø2) and timer clock (TCLK) rates are determined by the combination of selected prescaler mode and value. When prescaler mode 0 is selected, Ø2 and TCLK both run at the internal master clock (MCLK) rate regardless of the selected prescaler value. Ø2 runs at MCLK in prescaler modes 0 and 1 and at MCLK ÷ PV in prescaler mode 3. TCLK runs at MCLK in prescaler mode 0 and at MCLK ÷ PV in prescaler modes 1 and 3. Prescaler mode 2 is illegal and will cause indeterminate operation if selected.

The selected prescaler value is invoked in the cycle following the write or interrupt occurrence. Waveforms for five of these operations are illustrated in Figure 3-7.



A. Crystal Input



B. Clock Input

Notes:
1. Clock input divide-by-2 option must be selected.
2. Clock input divide-by-2 selected.
3. Clock input divide-by-1 selected.

Figure 3-5. Clock Oscillator Input Options

	7	6	5	4	3	2	1	0
ADDR $08E	NOT USED				V1	V0	M1	M0

Bits 3-2 Prescaler Value (PV) Select[1]

V1	V0	Prescale Value
0	0	Divide by 8
0	1	Divide by 32
1	0	Divide by 64
1	1	Divide by 128

Bits 1-0 Prescaler Mode (PM) Select[1]

M1	M0	Mode	System Clock (Ø2) Rate	Timer Clock (TCLK) Rate
0	0	0	MCLK	MCLK
0	1	1	MCLK	MCLK ÷ PV
1	0	2	N/A	N/A (Illegal Mode)
1	1	3	MCLK ÷ PV	MCLK ÷ PV

Note: 1. All bits are reset to 0 by $\overline{RES}$.

Figure 3-6. Prescaler Control Register

3.13 CONTROL REGISTER (CR)

The Control Register (CR), shown in Figure 3-8, is located at address $8F. The CR contains five control bits and three status bits. The control bits must be written to the Control Register. The status bits can be read, along with the previously written control bits, by reading the register. All control and status bits in the Control Register are cleared to 0 by the assertion of $\overline{RES}$. The signals controlled by and reported in the CR are described in the following paragraphs.

Bits 0 to 4 in the Control Register are control bits (Figure 3-8). The control signals are set by writing a 1 into the respective bit position, and cleared either by writing a 0 into the respective bit position or by assertion of $\overline{RES}$.

Bits 5 to 7 in the Control Register are status bits (Figure 3-8). The status bits are read-only information. Each status bit is set to a 1 by monitoring circuitry, and is cleared to a 0 either by writing to specific address or by assertion of $\overline{RES}$.

COUNTER MODE CONTROL 0 AND 1

Counter Mode Control signals CMC0 and CMC1 (bits 0 and 1) control the Counter operating modes. The modes of operation and the corresponding configuration of CMC0 and CMC1 are shown in Figure 3-8. These modes are selected by writing the appropriate bit values into the Counter Mode Control bits.

The Counter is reset to the Interval Timer mode (Mode 0) by assertion of $\overline{RES}$ (which causes 0s to be loaded into all bits of the Control Register).

PA1 INTERRUPT ENABLE BIT (A1IE)

If the PA1 Interrupt Enable bit (bit 2) is set to a 1, IRQ will occur when the PA1 Negative Edge Detected bit (bit 5) is set to a 1.

PA0 INTERRUPT ENABLE BIT (A0IE)

If the PA0 Interrupt Enable bit (bit 3) is set to a 1, IRQ will occur when the PA0 Positive Edge Detected bit (bit 6) is set to a 1.

COUNTER INTERRUPT ENABLE BIT (CIE)

If the Counter Interrupt Enable Bit (bit 4) is set to a 1, IRQ will occur when Counter Overflow (bit 7) is set to a 1.

PA1 NEGATIVE EDGE DETECTED BIT (A1ED)

The PA1 Negative Edge Detected bit (bit 5) is set to a 1 whenever a negative (falling) edge is detected on PA1. This bit is cleared to a 0 by writing to address $08A or by assertion of $\overline{RES}$.

The edge detecting circuitry is active regardless of whether PA1 is an input or is an output. When PA1 is used as an output, A1ED will be set when the negative edge is detected during a high-to-low transition. When PA1 is used as an input and the negative

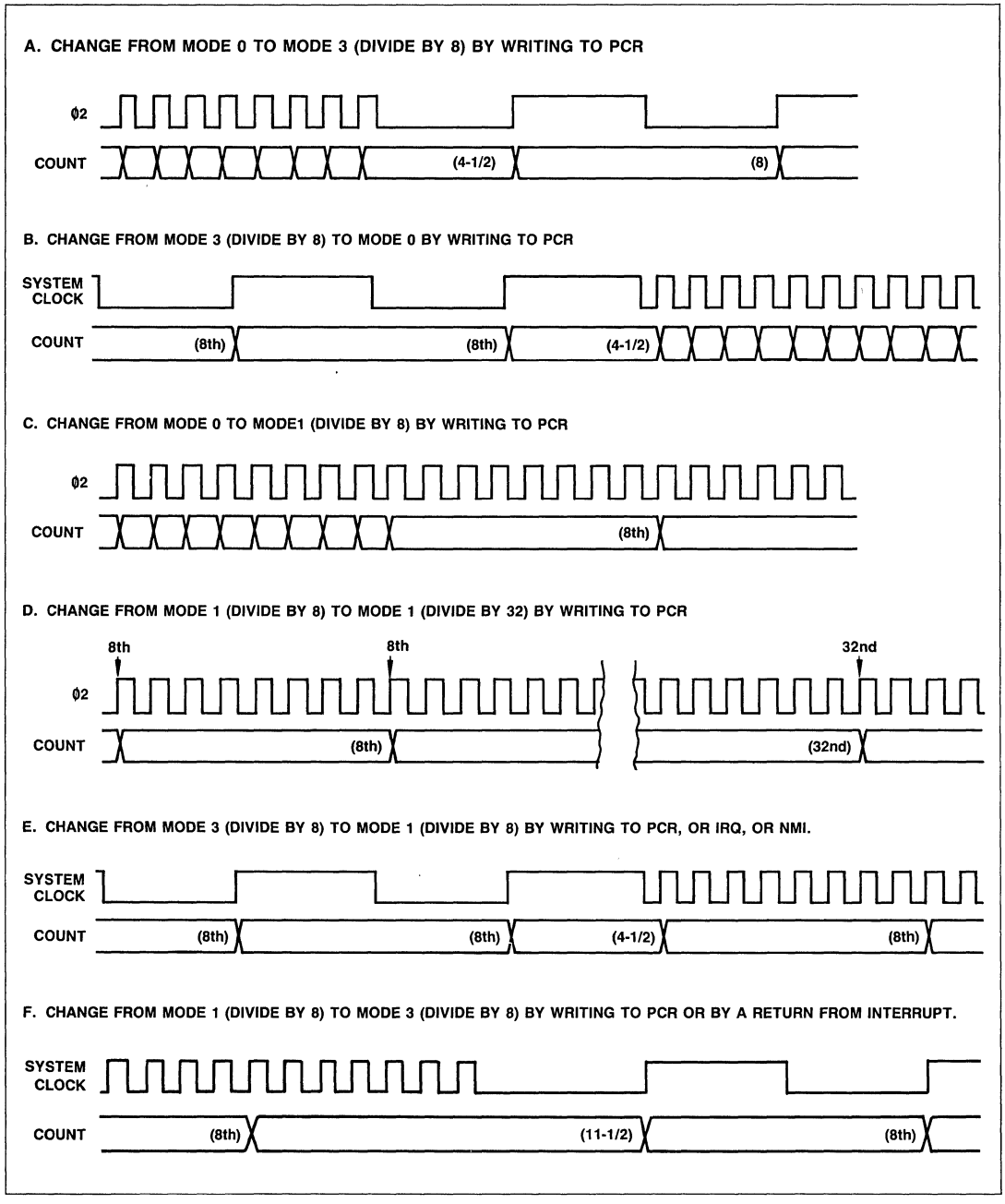


Figure 3-7. Prescaler Waveform Examples

	7	6	5	4	3	2	1	0
ADDR	INTERRUPT STATUS			INTERRUPT ENABLE			TIMER MODE	
$08F	TIMER	PA0	PA1	TIMER	PA0	PA1	CONTROL	

Bit 7 **COUNTER OVERFLOW (CTRO)[1]**
1 Counter overflow occurred
0 No counter overflow

Bit 6 **PA0 POSITIVE EDGE DETECT (A0ED)[1]**
1 PA0 positive edge detected
0 PA0 positive edge not detected

Bit 5 **PA1 NEGATIVE EDGE DETECT (A1ED)[1]**
1 PA1 negative edge detected
0 PA1 negative edge not detected

Bit 4 **COUNTER INTERRUPT ENABLE (CIE)[2]**
1 Enable counter interrupt
0 Disable counter interrupt

Bit 3 **PA0 INTERRUPT ENABLE (A0IE)[2]**
1 Enable PA0 interrupt
0 Disable PA0 interrupt

Bit 2 **PA1 INTERRUPT ENABLE (A1IE)[2]**
1 Enable PA1 interrupt
0 Disable PA1 interrupt

Bit 10 **COUNTER MODE CONTROL (CMC1 & CMC2)[2]**
0 0 Interval Timer
0 1 Pulse Generator
1 0 Event Counter
1 1 Pulse Width Measurement

Notes: 1. Read only.
2. Read/write.

Figure 3-8. Control Register

edge detecting circuitry is used, A1ED should be cleared by the user program upon initialization and upon completion of the PA1 Negative Edge Detected IRQ processing.

PA0 POSITIVE EDGE DETECTED BIT (A0ED)

The PA0 Positive Edge Detected bit (bit 6) is set to a 1 whenever a positive (rising) edge is detected on PA0. This bit is cleared to a 0 by writing to address $089 or by assertion of $\overline{RES}$.

The edge detecting circuitry is active regardless of whether PA0 is an input or is an output. When PA0 is used as an output, A0ED will be set when the positive edge is detected during a low-to-high transition. When PA0 is used as an input and the positive edge detecting circuitry is used, A0ED should be cleared by the user program upon initialization and upon completion of PA0 Positive Edge Detected IRQ processing.

COUNTER OVERFLOW BIT (CTRO)

The Counter Overflow bit (bit 7) is set to a 1 whenever the Counter overflow occurs in any of the four counter operating modes. Overflow occurs when the Counter is decremented one count from 0. This bit is cleared to a 0 by reading from address $087, writing to address $088, or by assertion of $\overline{RES}$.

The CTRO bit should be cleared by the user program upon initialization and upon completion of Counter Overflow IRQ interrupt processing.

When a Counter Overflow occurs, the Upper Count (UC) in address $086, and the Lower Count (LC) in address $087, are loaded with to the values contained in the Upper Latch (UL) in address $084, and in the Lower Latch (LL) in address $085, respectively.

3.14 PARALLEL INPUT/OUTPUT PORTS

The R65C10 provides four memory-mapped 8-bit Input/Output (I/O) ports: PA, PB, PC and PD. All 32 I/O lines of the four ports are completely bidirectional. All lines may be used either for input or output in any combination, i.e., there are no line grouping or port association restrictions. A mask option is available to select I/O port operation with or without direction registers. Table 3-1 lists the I/O port and edge detected bit reset addresses.

Table 3-1. I/O Port Addresses

Port/Function	Address
Port A Direction Register (Write Only)	$090
Port B Direction Register (Write Only)	$091
Port C Direction Register (Write Only)	$092
Port D Direction Register (Write Only)	$093
Port A Data Register (Read/Write)	$080
Port B Data Register (Read/Write)	$081
Port C Data Register (Read/Write)	$082
Port D Data Register (Read/Write)	$083
Clear PA0 Positive Edge Detected Bit (Write Only)	$089
Clear PA1 Negative Edge Detected Bit (Write Only)	$08A

I/O PORT OPERATION WITHOUT DIRECTION REGISTERS

If direction registers are *not* selected, the direction of the 32 I/O lines is controlled by writing to the four 8-bit port data registers located in page zero at addresses $80–$83 (see Figure 3-3). This arrangement provides quick programming access using simple 2-byte zero page address instructions. I/O handling is simplified since programming of direction registers is not required.

Inputs

Inputs are enabled by writing a 1 into all I/O port register bit positions that correspond to input lines. A low ($\leq$0.8 Vdc) input level causes a 0 to be read when a read instruction is issued to the port register. A high ($\geq$2.0 Vdc) input level causes a 1 to be read. Assertion of $\overline{RES}$ forces all bits in the I/O port registers to 1s, thus initially treating all I/O lines as inputs.

The status of the input lines can be interrogated at any time by reading the I/O port addresses. Note that this will return the actual status of the input lines, not the data written into the I/O port register.

Outputs

Outputs are controlled by writing the desired I/O line output states into the corresponding I/O port register bit positions.

A 1 will force a high (≥2.4 Vdc) output while a 0 will force a low (≤0.4 Vdc) output.

I/O PORT OPERATION WITH DIRECTION REGISTERS

If direction registers are selected, the direction of all 32 I/O lines is controlled by individual bits in four write-only I/O port direction registers. The direction registers for ports A, B, C and D are located at addresses $90, $91, $92 and $93, respectively. Setting a bit in a direction register to a 1 causes the corresponding I/O line to operate as an output; resetting the bit to a 0 causes the I/O line to be an input. Assertion of $\overline{RES}$ clears all direction register bits to 0s causing all I/O lines to initially be inputs.

Inputs

If an I/O line is an input, the state of the corresponding bit in the I/O port data register shows the input logic level: 1 = high; 0 = low.

Outputs

If an I/O line is an output, the state of the corresponding bit written to the port data register determines the output logic level: 1 = high; 0 = low.

EDGE DETECTION CAPABILITY

The Port A PA0 and PA1 circuitry has edge detection capability. Edges detected on these lines are reported in the Control Register and will cause an IRQ if enabled in the Control Register (see Section 3.14). The edge detect timing waveforms are illustrated in Figure 3-9.

PA0 Positive Edge Detection

In addition to its normal I/O function, an asynchronous positive (rising) edge signal can be detected on PA0. This occurrence will be reported in the PA0 Positive Edge Detected bit in the Control Register (CR6). CR6 is cleared by writing to address $089 or by assertion of $\overline{RES}$.

PA1 Negative Edge Detection

In addition to its normal I/O function, an asynchronous negative (falling) edge signal can be detected on PA1. This occurrence wil be reported in the PA1 Negative Edge Detected bit in the Control Register (CR5). CR5 is cleared by writing to address $08A or by assertion of $\overline{RES}$.

3.15 COUNTER/LATCH

GENERAL

The Counter/Latch consists of a 16-bit Counter, and a 16-bit Latch. The Counter resides in two 8-bit registers: address $086 contains the Upper Count value (bits 8–15 of the Counter) and address $087 contains the Lower Count value (bits 0–7 of the Counter). The Counter contains the count of either unscaled or prescaled Ø2 clock periods, or external events, depending on Counter mode selected in the Control Register and, for clock driven Counter modes, the Prescaler mode and value selected in the Prescaler Control Register. Table 3-2 lists the addresses associated with Counter/Latch operation.

Table 3-2. Counter/Latch Addresses

Function	Address
Write Upper Latch (Write Only)	$084
Write Lower Latch (Write Only)	$085
Read Upper Count (Read Only)	$086
Read Lower Count, Clear Timer Overflow (Read Only)	$087
Write Upper Latch and Transfer Latch to Counter, Clear Counter Overflow (Write Only)	$088

The Latch contains the Counter initialization value. The Latch resides in two 8-bit registers: address $084 contains the Upper Latch value (bits 8–15 of the Latch) and address $085 contains the Lower Latch value (bits 0–7 of the Latch). The 16-bit Latch can hold values from 0 to 65,535.

The latch registers can be loaded at any time by writing to the Upper Latch address ($084) and the Lower Latch address ($085). In each case, the contents of the Accumulator are copied into the applicable Latch register. The Upper Latch and Lower Latch

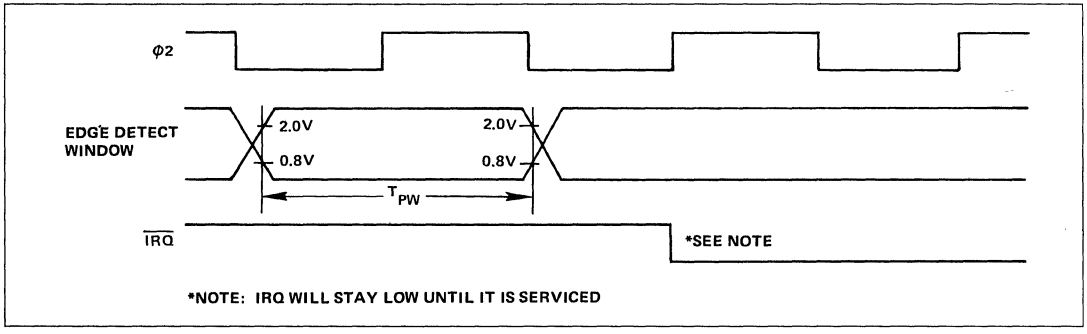


Figure 3-9. PA0 and PA1 Edge Detection Timing Waveforms

can be loaded independently; it is not required to load both registers at the same time, or sequentially. The Upper Latch can also be loaded by writing to address $088.

The Counter will also be initialized to the Latch value whenever the Counter overflows. When the Counter decrements from 0, the next Counter value will be the Latch value, not $FFFF.

Whenever the Counter overflows, the Counter Overflow status bit in the Control Register (CR7) is set to a 1. This bit is cleared whenever the lower eight bits of the Counter are read from address $087 or by writing to address $088.

COUNTER/TIMER MODES

The Counter operates in any of four modes. These modes are selected by the Counter Mode Control bits in the Control Register (see Table 3-3).

The Interval Timer, Pulse Generator, and Pulse Width Measurement modes are internally clocked modes. The Event Counter Mode counts the occurrences of an external event on the CNTR line.

Interval Timer (Mode 0)

In the Interval Timer mode, the Counter is initialized to the Latch value by either of two conditions:

1. When the Counter is decremented from 0, the next Counter value is the Latch value, not $FFFF.

2. When a write operation is performed to the Upper Latch and the Transfer Latch to Counter address ($088), the Counter is loaded with the Latch value. Note that the contents of the Accumulator are loaded into the Upper Latch before the Latch value is transferred to the Counter.

The Counter value is decremented at the timer clock (TCLK) rate. The 16-bit Counter can hold from 1 to 65,535 counts. For a 4 MHz internal Ø2 clock and no prescaler selected, the timer range is 0.25 μs to 16.384 ms. For a 4 MHz internal Ø2 clock and divide-by-128 prescaler selected, the timer range is 32 μs to 2.097 seconds.

When the Counter decrements from 0, the Counter Overflow bit in the Control Register (CR7) is set to a 1 at the next counter clock pulse. If the Counter Interrupt Enable bit (CR4) is also set, IRQ will occur. The Counter Overflow bit in the Control Register can be examined in the IRQ interrupt routine to determine that the IRQ was caused by the Counter overflow.

While the timer is operating in the Interval Timer mode, the Counter-Out/Event-In (CNTR) line is held in the high impedance state (output disabled).

A timing diagram of the Interval Timer mode is shown in Figure 3-10.

Pulse Generator Mode (Mode 1)

In the Pulse Generator mode, the CNTR line operates as a Counter-Out. When a write is performed to address $088 the CNTR output is initialized high. The Counter is decremented at the TCLK rate. The CNTR line toggles from low to high or from high to low whenever a Counter overflow occurs.

Either a symmetric or an asymmetric output waveform can be output on the CNTR line in this mode. The CNTR output is initialized to the high impedance state (output disabled) by assertion of $\overline{RES}$ since the Interval Timer mode is established by $\overline{RES}$.

Event Counter Mode (Mode 2)

In this mode, the CNTR line is used as an Event-In input, and the Counter will decrement with each rising edge detected on this line. The maximum rate at which this edge can be detected is one-half the system (Ø2) clock rate.

The Counter can count up to 65,535 occurrences before overflowing. As in the other modes, the Counter Overflow bit (CR7) is set to a 1 if the overflow occurs.

Figure 3-11 is a timing diagram of the Event Counter mode.

Pulse Width Measurement Mode (Mode 3)

This mode allows the accurate measurement of a low pulse duration on the CNTR line. In this mode, CNTR is used in the Event-In capacity. The Counter decrements at the TCLK rate as long as the CNTR line is held in the low state. The Counter is stopped when CNTR is in the high state.

If the CNTR pin is left disconnected, this mode may be selected to stop the Counter since the internal pull-up device (if present) will cause the CNTR input to be in the high ($\geq$2.0 volt) state.

A timing diagram for the Pulse Width Measurement mode is shown in Figure 3-12.

3.16 INTERRUPT LOGIC

Interrupt logic controls the sequencing of $\overline{RES}$ and the two interrupts: $\overline{NMI}$, and IRQ.

$\overline{RES}$ Sequencing

$\overline{RES}$ going from low-to-high causes the R65C/1 to set the Interrupt Disable bit in the Processor Status Register (bit 2) and to initiate RES vector fetch at address $FFC and $FFD to begin user program execution. All of the I/O ports (PA, PB, PC, and PD) and CNTR are forced to the high (logic 1) state. All bits of the Control Register are cleared to logic 0, causing the Interval Timer Counter Mode (Mode 0) to be selected and causing all interrupt enable bits to be reset. All Prescaler Control Register bits are also reset to 0 causing Prescaler Mode 0 to be selected.

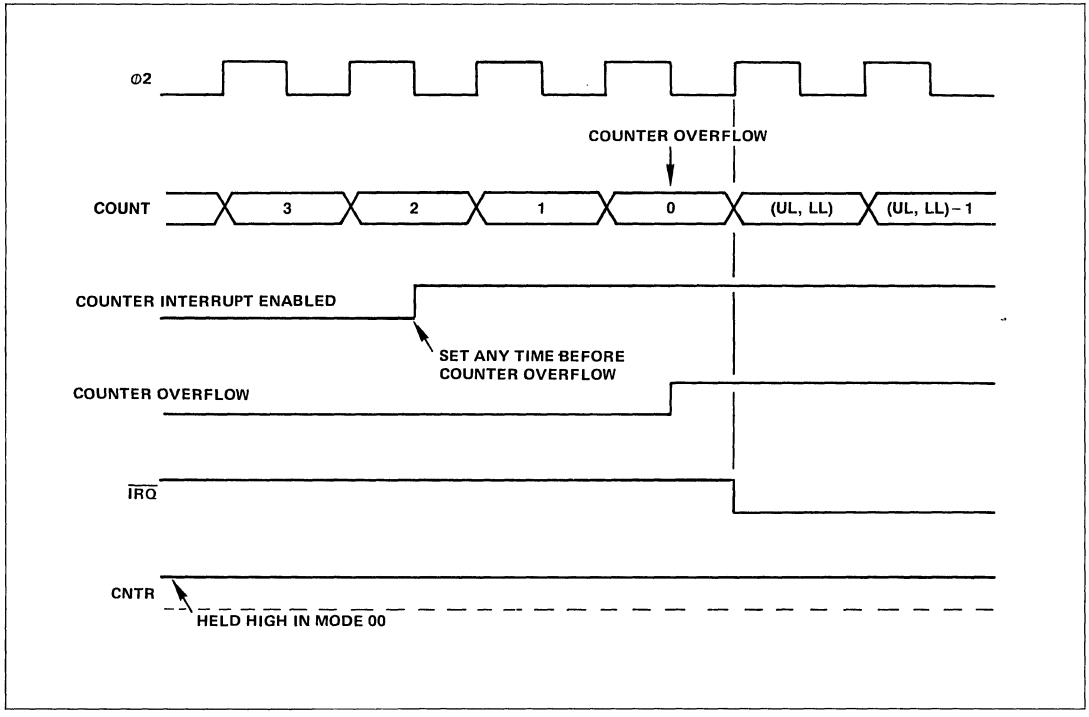


Figure 3-10. Interval Timer (Mode 0) Timing Waveforms

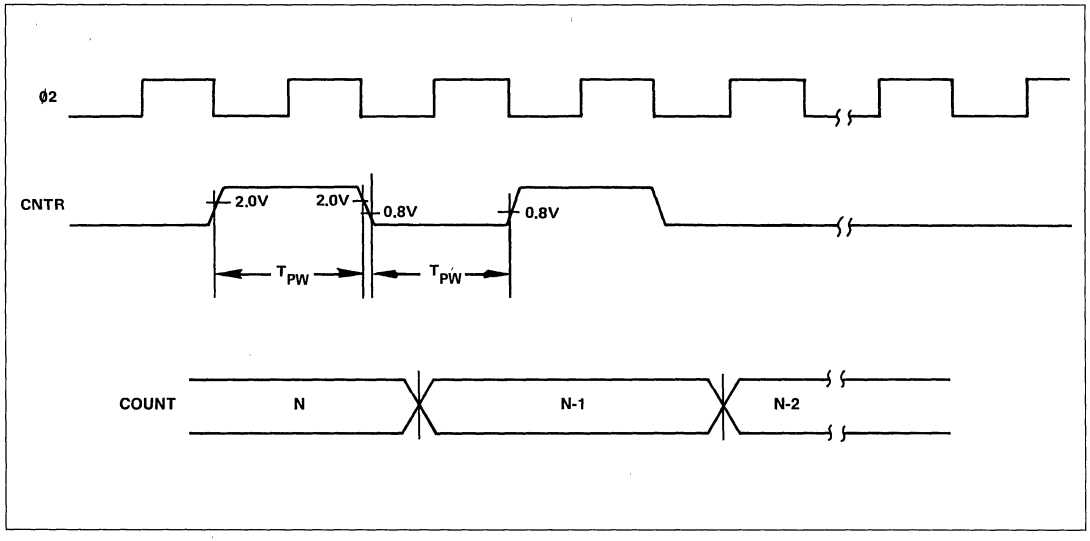


Figure 3-11. Event Counter (Mode 2) Timing Waveforms

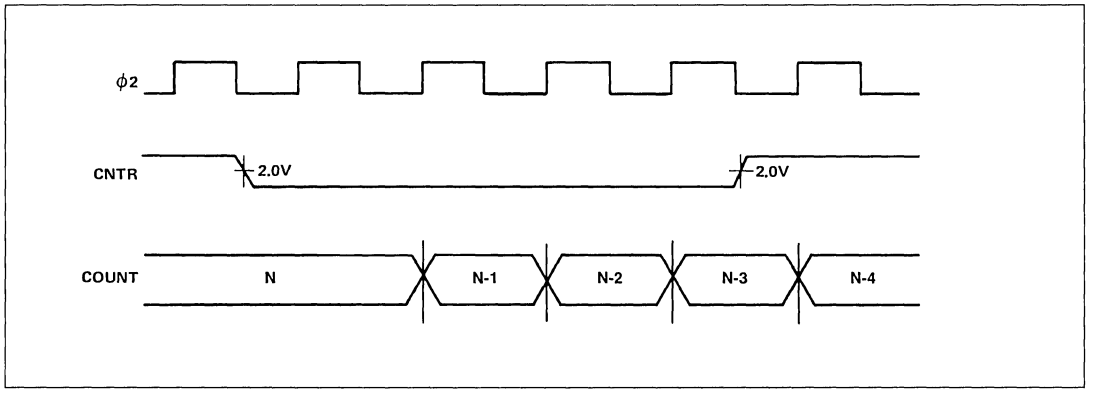


Figure 3-12. Pulse Width Measurement (Mode 3) Timing Waveforms

$\overline{\text{NMI}}$ Sequencing

At the first operation code fetch following the high-to-low transition of the $\overline{\text{NMI}}$ input, the interrupt logic forces execution of the Break (BRK) instruction and subsequent execution from the address vector stored at $FFA and $FFB. Simultaneous with the execution of the BRK instruction, the Interrupt Disable bit in the Processor Status Register is set to disable an IRQ and bit 1 in the Prescaler Control Register is cleared to select unscaled system clock. Bit 0 of the Prescaler Control Register is unaffected.

IRQ Sequencing

The internal IRQ can be generated by any or all of three possible conditions: Counter Overflow, a positive edge detected on PA0, or a negative edge detected on PA1. The IRQ in response to these conditions can be enabled or disabled by setting or resetting the appropriate interrupt enable bits in the Control Register.

The first IRQ condition is Counter Overflow. IRQ will occur whenever both the Counter Interrupt Enable (CR4) and the Counter Overflow (CR7) are logic 1.

The second IRQ condition is detection of a positive edge on PA0. IRQ will occur whenever both the PA0 Interrupt Enable (CR3) and the PA0 Positive Edge Detected (CR6) are logic 1.

The third IRQ condition is detection of a negative edge on PA1. IRQ will occur whenever both the PA1 Interrupt Enable (CR2) and the PA1 Negative Edge Detected (CR5) are logic 1.

Multiple simultaneous interrupts will cause the IRQ to remain active until all interrupting conditions have been serviced and cleared.

The IRQ interrupt occurs when bit 2 of the Process Status Register is clear (enabling an IRQ), an IRQ enable bit (bit 2, 3 or 4) in the Control Register is set, and the corresponding interrupt bit (bit 5, 6 or 7) in the Control Register is set. Upon IRQ interruption, the BRK instruction is forced and subsequent program execution begins from the address vector stored at $FFE and $FFF. Bit 2 of the Processor Status Register is set. Bit 1 in the Prescaler Control Register is cleared to select unscaled system ϕ2 clock. Bit 0 of the Prescaler Control Register is unaffected.

SECTION 4
POWER ON/OFF INITIALIZATION AND OTHER CONSIDERATIONS

This section describes power turn-on, stop mode and mask option considerations for the R65C10.

4.1 POWER-ON TIMING

After application of V_{CC} power to the R65C10, $\overline{RES}$ must be held low for at least eight $\phi 2$ clock cycles after V_{CC} reaches operating range and the internal clock oscillator has stabilized. This stabilization time is dependent upon the input V_{CC} voltage and performance of the crystal or clock input circuit. The clock oscillator output can be monitored on XTLO (Pin 11).

The power turn-on waveforms are illustrated in Figure 4-1.

4.2 STOP MODE

The Stop mode is an ultra-low-power mode in which the internal oscillator and clock is stopped. This mode is entered by writing to address $08D and is exited only when $\overline{RES}$ is asserted.

While in this mode, the R65C10 is dormant; however, the contents of RAM are preserved. Maximum power dissipation while in the Stop mode is under 4 mW. The oscillator stops with XTLO low.

A mask option is provided to inhibit Stop mode entry. This option is recommended if Stop mode is not used during operation.

4.3 MASK OPTIONS

Mask options are user selectable options permanently implemented when the R65C10 device is manufactured in response to a customer order. The options are to be specified on the R65C10 sheet in the R6500/* ROM Code Order Forms (Literature Order No. 2134). The options deal with three basic circuits:

- Input crystal/clock frequency divisor
- I/O port direction registers and internal pull-up resistors
- Stop mode enable/disable

Input Crystal/Clock Frequency Divisor

The input clock/crystal frequency divisor can be selected to be either 1 or 2 (see Section 3.11).

Direction Registers/Pull-up Resistors

Direction registers can be selected for controlling port input/output operation (see Section 3.14).

If direction registers are not used, then internal pull-up resistors can be optionally selected. In this case, pull-up resistors can be optionally included for 8-bit port groups only, i.e., not for individual I/O lines within an 8-bit port group. In addition, an internal pull-up for the CNTR line is selectable.

If direction registers are included, then internal pull-ups are not allowed.

Stop Mode Entry Enable

An option also exists to enable Stop mode use by writting to address 08D. (see Section 4.2).

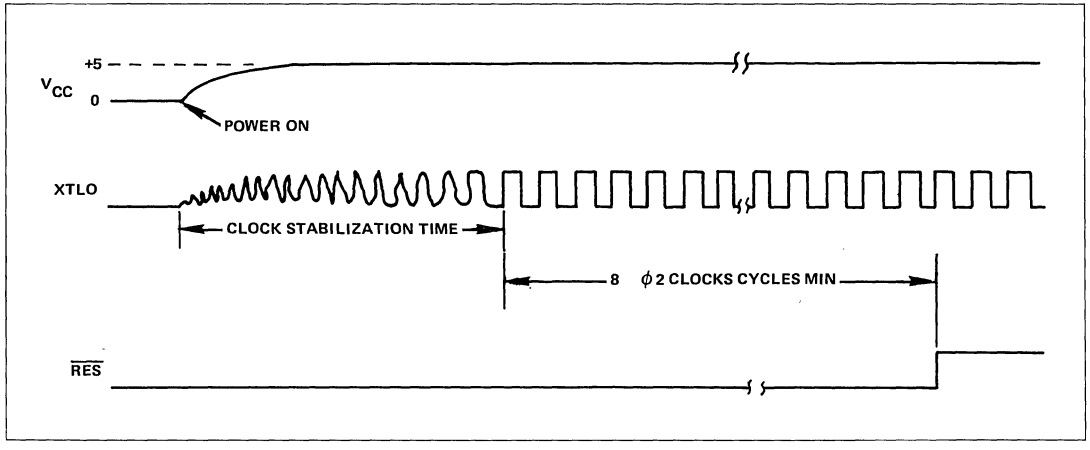


Figure 4-1. Power Turn-On Timing Detail

SECTION 5
SYSTEM SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to +7.0	Vdc
Input Voltage	V_{IN}	−0.3 to +7.0	Vdc
Storage Temperature	T_{STG}	−55 to +150	°C

***NOTE:** Stresses exceeding those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the other sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING CONDITIONS

Parameter	Symbol	Value
Supply Voltage	V_{CC}	5.0 Vdc ±10%
Operating Temperature (Ambient) Commercial Industrial	T_A	T_L to T_H 0°C to +70°C −40°C to +85°C

3

ELECTRICAL CHARACTERISTICS

(Over operating conditions unless otherwise noted)

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions
Input High Voltage All except $\overline{NMI}$ and $\overline{RES}$ $\overline{NMI}$, $\overline{RES}$	V_{IH}	 +2.0 +2.4	 — —	 V_{CC} V_{CC}	V	V_{CC} = 5.5V
Input Low Voltage	V_{IL}	—	—	+0.8	V	V_{CC} = 4.5V
Input Leakage Current $\overline{RES}$, $\overline{NMI}$	I_{IN}	—	—	±2.5	μA	V_{IN} = 0 to 5.0V
Output High Voltage	V_{OH}	+2.4	—	—	V	V_{CC} = 4.5V I_{LOAD} = −100 μA
Output Low Voltage	V_{OL}	—	—	+0.4	V	V_{CC} = 5.5V I_{LOAD} = 1.6 mA
Output High Current (Sourcing)	I_{OH}	−100	—	—	μA	V_{OUT} = 2.4V
Output Low Current (Sinking)	I_{OL}	1.6	—	—	mA	V_{OUT} = 0.4V
I/O Port Pull-Up Resistance PA0–PA7, PB0–PB7, PC0–PC7, PD0–PD7, CNTR	R_L	2.0	3.2	6.0	Kohm	
Input Capacitance XTLI, XTLO PA0–PA7, PB0–PB7, PC0–PC7, PD0–PD7, CNTR	C_{IN}	 — —	 — —	 25 7	pF	T_A = 25°C V_{IN} = 0V f = 2 MHz–4 MHz
Output Capacitance	C_{OUT}	—	—	50	pF	1 TTL load
Input Frequency (f) Crystal Clock Clock	f	 2.0 0.04 0.02	 — — —	 8.0 8.0 4.0	 MHz MHz MHz	 ÷2 selected ÷2 selected ÷1 selected
Power Dissipation Operating Stop Mode	P_D	 — —	 12 1.4	 14 1.6	 mW/MHz mW	V_{CC} = 5.5V Outputs High Frequency = unscaled ϕ2 clock No external clock input

Notes:
1. T_A = 25°C and V_{CC} = 5.0V.
2. Negative sign indicates outward current flow, positive indicates inward flow.

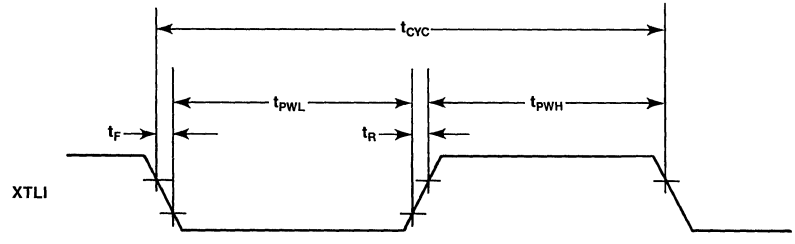
SWITCHING CHARACTERISTICS

(Over operating conditions unless otherwise noted)

Parameter	Mode	Symbol	1 MHz		2 MHz		3 MHz		4 MHz		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
XTLI Input Clock											
Cycle Time	÷2	t_{CYC}	0.500	25.0	0.250	25.0	0.166	25.0	0.125	25.0	μs
Pulse Width, Low	÷2	t_{PWL}	100		55		45		40		ns
Pulse Width, High	÷2	t_{PWH}	100		55		45		40		ns
Rise and Fall Time	÷2	t_R, t_F		60		25		20		15	ns
XTLI Input Clock											
Cycle Time	÷1	t_{CYC}	1.000	50.0	0.500	50.0	0.333	50.0	0.250	50.0	μs
Pulse Width, Low	÷1	t_{PWL}	450		225		145		110		ns
Pulse Width, High	÷1	t_{PWH}	450		225		145		110		ns
Rise and Fall Time	÷1	t_R, t_F		20		15		12		10	ns
Count and Edge Detect Pulse Width			1		1		1		1		Ø2 Period*

*Function of Prescaler

SWITCHING WAVEFORMS



APPENDIX A
R65C10 INSTRUCTION SET

This appendix summarizes the R65C10 instruction set. The basic instructions are listed alphabetically by standard mnemonic in Table A-1. The instruction operation codes (OP Codes) for all valid addressing modes are listed in Table A-2. Also listed in Table A-2 are the number of bytes and number of CPU cycles required in each addressing mode. The effect of instruction execution on the Processor Status Register is also shown.

A matrix of instructions and addressing modes arranged by operation code is shown in Table A-3. For detailed information about CPU instruction execution, consult the R6500 Programming Manual (Order No. 202).

Table A-4 summarizes the differences in operation between the R65C10 CPU and the R6502 CPU.

Table A-1. R65C10 Instruction Set Alphabetic Sequence

Mnemonic	Instruction	Mnemonic	Instruction
ADC	Add Memory to Accumulator with Carry	JMP	Jump to New Location
AND	"AND" Memory with Accumulator	JSR	Jump to New Location Saving Return Address
ASL	Shift Left One Bit (Memory or Accumulator)		
		LDA	Load Accumulator with Memory
		LDX	LOAD Index X with Memory
BCC	Branch on Carry Clear	LDY	Load Index Y with Memory
BCS	Branch on Carry Set	LSR	Shift One Bit Right (Memory or Accumulator)
BEQ	Branch on Result Zero		
BIT	Test Bits in Memory with Accumulator	NOP	No Operation
BMI	Branch on Result Minus	ORA	"OR" Memory with Accumulator
BNE	Branch on Result not Zero		
BPL	Branch on Result Plus	PHA	Push Accumulator on Stack
BRK	Force Break	PHP	Push Processor Status on Stack
BVC	Branch on Overflow Clear	PLA	Pull Accumulator from Stack
BVS	Branch on Overflow Set	PLP	Pull Processor Status from Stack
CLC	Clear Carry Flag	ROL	Rotate One Bit Left (Memory or Accumulator)
CLD	Clear Decimal Mode	ROR	Rotate One Bit Right (Memory or Accumulator)
CLI	Clear Interrupt Disable Bit	RTI	Return from Interrupt
CLV	Clear Overflow Flag	RTS	Return from Subroutine
CMP	Compare Memory and Accumulator		
CPX	Compare Memory and Index X	SBC	Subtract Memory from Accumulator with borrow
CPY	Compare Memory and Index Y	SEC	Set Carry Flag
		SED	Set Decimal Mode
		SEI	Set Interrupt Disable Status
DEC	Decrement Memory by One	STA	Store Accumulator in Memory
DEX	Decrement Index X by One	STX	Store Index X in Memory
DEY	Decrement Index Y by One	STY	Store Index Y in Memory
EOR	"Exclusive-Or" Memory with Accumulator	TAX	Transfer Accumulator to Index X
		TAY	Transfer Accumulator to Index Y
		TSX	Transfer Stack Pointer to Index X
INC	Increment Memory by One	TXA	Transfer Index X to Accumulator
INX	Increment Index X by One	TXS	Transfer Index X to Stack Register
INY	Increment Index Y by One	TYA	Transfer Index Y to Accumulator

Table A.2. R65C10 Instruction Set by Address Modes

		ADDRESSING MODES																																		PROCESSOR STATUS CODES	
		IMMEDIATE			ABSOLUTE			ZERO PAGE			ACCUM			IMPLIED			(IND. X)			(IND). Y			Z PAGE. X			ABS X			ABS. Y			RELATIVE			INDIRECT			Z PAGE. Y			7 6 5 4 3 2 1 0	
MNEMONIC	OPERATION	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	N V * B D I Z C	MNEMONIC
ADC	A + M + C → A (4) (1)	69	2	2	6D	4	3	65	3	2							61	6	2	71	5	2	75	4	2	7D	4	3	79	4	3								N V • • • • Z C	ADC
AND	A∧M → A (1)	29	2	2	2D	4	3	25	3	2							21	6	2	31	5	2	35	4	2	3D	4	3	39	4	3								N • • • • • Z •	AND
ASL	C ← [7 6 5 4 3 2 1 0] ← 0				0E	6	3	06	5	2	0A	2	1										16	6	2	1E	7	3											N • • • • • Z C	ASL
BCC	BRANCH ON C = 0 (2)																															90	2	2						• • • • • • • •	BCC
BCS	BRANCH ON C = 1 (2)																															B0	2	2						• • • • • • • •	BCS
BEQ	BRANCH ON Z = 1 (2)																															F0	2	2						• • • • • • • •	BEQ
BIT	A∧M				2C	4	3	24	3	2																														M_7 M_6 • • • • Z •	BIT
BMI	BRANCH ON N = 1 (2)																															30	2	2						• • • • • • • •	BMI
BNE	BRANCH ON Z = 0 (2)																															D0	2	2						• • • • • • • •	BNE
BPL	BRANCH ON N = 0 (2)																															10	2	2						• • • • • • • •	BPL
BRK	BREAK													00	7	1																								• • • 1 • 1 • •	BRK
BVC	BRANCH ON V = 0 (2)																															50	2	2						• • • • • • • •	BVC
BVS	BRANCH ON V = 1 (2)																															70	2	2						• • • • • • • •	BVS
CLC	0 → C													18	2	1																								• • • • • • • 0	CLC
CLD	0 → D													D8	2	1																								• • • • 0 • • •	CLD
CLI	0 → I													58	2	1																								• • • • • 0 • •	CLI
CLV	0 → V													B8	2	1																								• 0 • • • • • •	CLV
CMP	A − M (1)	C9	2	2	CD	4	3	C5	3	2							C1	6	2	D1	5	2	D5	4	2	DD	4	3	D9	4	3								N • • • • • Z C	CMP
CPX	X − M	E0	2	2	EC	4	3	E4	3	2																														N • • • • • Z C	CPX
CPY	Y − M	C0	2	2	CC	4	3	C4	3	2																														N • • • • • Z C	CPY
DEC	M − 1 → M				CE	6	3	C6	5	2													D6	6	2	DE	7	3											N • • • • • Z •	DEC
DEX	X − 1 → X													CA	2	1																								N • • • • • Z •	DEX
DEY	Y − 1 → Y													88	2	1																								N • • • • • Z •	DEY
EOR	A ∨ M → A (1)	49	2	2	4D	4	3	45	3	2							41	6	2	51	5	2	55	4	2	5D	4	3	59	4	3								N • • • • • Z •	EOR
INC	M + 1 → M				EE	6	3	E6	5	2													F6	6	2	FE	7	3											N • • • • • Z •	INC
INX	X + 1 → X													E8	2	1																								N • • • • • Z •	INX
INY	Y + 1 → Y													C8	2	1																								N • • • • • Z •	INY
JMP	JUMP TO NEW LOC				4C	3	3																												6C	5	3				• • • • • • • •	JMP
JSR	JUMP SUB				20	6	3																																		• • • • • • • •	JSR
LDA	M → A (1)	A9	2	2	AD	4	3	A5	3	2							A1	6	2	B1	5	2	B5	4	2	BD	4	3	B9	4	3								N • • • • • Z •	LDA
LDX	M → X (1)	A2	2	2	AE	4	3	A6	3	2																			BE	4	3							96	4	2	N • • • • • Z •	LDX
LDY	M → Y (1)	A0	2	2	AC	4	3	A4	3	2													B4	4	2	BC	4	3											N • • • • • Z •	LDY
LSR	0 → [7 6 5 4 3 2 1 0] → C				4E	6	3	46	5	2	4A	2	1										56	6	2	5E	7	3											0 • • • • • Z C	LSR
NOP	NO OPERATION													EA	2	1																								• • • • • • • •	NOP
ORA	A ∨ M → A (1)	09	2	2	0D	4	3	05	3	2							01	6	2	11	5	2	15	4	2	1D	4	3	19	4	3								N • • • • • Z •	ORA
PHA	A → Ms S − 1 → S													48	3	1																								• • • • • • • •	PHA
PHP	P → Ms S − 1 → S													08	3	1																								• • • • • • • •	PHP
PLA	S + 1 → S Ms → A													68	4	1																								N • • • • • Z •	PLA
PLP	S + 1 → S Ms → P													28	4	1																								(RESTORED)	PLP
ROL	[7 6 5 4 3 2 1 0] ← [C]				2E	6	3	26	5	2	2A	2	1										36	6	2	3E	7	3											N • • • • • Z C	ROL
ROR	[C] → [7 6 5 4 3 2 1 0]				6E	6	3	66	5	2	6A	2	1										76	6	2	7E	7	3											N • • • • • Z C	ROR
RTI	RTRN INT													40	6	1																								(RESTORED)	RTI
RTS	RTRN SUB													60	6	1																								• • • • • • • •	RTS
SBC	A − M − $\overline{C}$ • A (4) (1)	E9	2	2	ED	4	3	E5	3	2							E1	6	2	F1	5	2	F5	4	2	FD	4	3	F9	4	3								N V • • • • Z (3)	SBC
SEC	1 → C													38	2	1																								• • • • • • • 1	SEC
SED	1 → D													F8	2	1																								• • • • 1 • • •	SED
SEI	1 → I													78	2	1																								• • • • • 1 • •	SEI
STA	A → M				8D	4	3	85	3	2							81	6	2	91	6	2	95	4	2	9D	5	3	99	5	3								• • • • • • • •	STA
STX	X → M				8E	4	3	86	3	2																												96	4	2	• • • • • • • •	STX
STY	Y → M				8C	4	3	84	3	2													94	4	2															• • • • • • • •	STY
TAX	A → X													AA	2	1																								N • • • • • Z •	TAX
TAY	A → Y													A8	2	1																								N • • • • • Z •	TAY
TSX	S → X													BA	2	1																								N • • • • • Z •	TSX
TXA	X → A													8A	2	1																								N • • • • • Z •	TXA
TXS	X → S													9A	2	1																								• • • • • • • •	TXS
TYA	Y → A													98	2	1																								N • • • • • Z •	TYA

(1) ADD 1 to N IF PAGE BOUNDARY IS CROSSED
(2) ADD 1 TO N IF BRANCH OCCURS TO SAME PAGE
ADD 2 TO N IF BRANCH OCCURS TO DIFFERENT PAGE
(3) CARRY NOT = BORROW
(4) ADD 1 TO N IF IN DECIMAL MODE

X INDEX X
Y INDEX Y
A ACCUMULATOR
M MEMORY PER EFFECTIVE ADDRESS
Ms MEMORY PER STACK POINTER
+ ADD
− SUBTRACT
∧ AND
∨ OR
¥ EXCLUSIVE OR
M_7 MEMORY BIT 7
M_6 MEMORY BIT 6
n NO CYCLES
NO BYTES

Table A-3. R65C10 Instruction Set Operation Code Matrix

MSD \ LSD	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	BRK Implied 1 7	ORA (IND, X) 2 6				ORA ZP 2 3	ASL ZP 2 5		PHP Implied 1 3	ORA IMM 2 2	ASL Accum 1 2			ORA ABS 3 4	ASL ABS 3 6	
1	BPL Relative 2 2[b]	ORA (IND), Y 2 5[a]				ORA ZP, X 2 4	ASL ZP, X 2 6		CLC Implied 1 2	ORA ABS, Y 3 4[a]				ORA ABS, X 3 4[a]	ASL ABS, X 3 7	
2	JSR Absolute 3 6	AND (IND, X) 2 6			BIT ZP 2 3	AND ZP 2 3	ROL ZP 2 5		PLP Implied 1 4	AND IMM 2 2	ROL Accum 1 2		BIT ABS 3 4	AND ABS 3 4	ROL ABS 3 6	
3	BMI Relative 2 2[b]	AND (IND), Y 2 5[a]				AND ZP, X 2 4	ROL ZP, X 2 6		SEC Implied 1 2	AND ABS, Y 3 4[a]				AND ABS, X 3 4[a]	ROL ABS, X 3 7	
4	RTI Implied 1 6	EOR (IND, X) 2 6				EOR ZP 2 3	LSR ZP 2 5		PHA Implied 1 3	EOR IMM 2 2	LSR Accum 1 2		JMP ABS 3 3	EOR ABS 3 4	LSR ABS 3 6	
5	BVC Relative 2 2[b]	EOR (IND), Y 2 5[a]				EOR ZP, X 2 4	LSR ZP, X 2 6		CLI Implied 1 2	EOR ABS, Y 3 4[a]				EOR ABS, X 3 4[a]	LSR ABS, X 3 7	
6	RTS Implied 1 6	ADC (IND, X) 2 6[c]				ADC ZP 2 3[c]	ROR ZP 2 5		PLA Implied 1 4	ADC IMM 2 2[c]	ROR Accum 1 2		JMP Indirect 3 5	ADC ABS 3 4[c]	ROR ABS 3 6	
7	BVS Relative 2 2[b]	ADC (IND), Y 2 5[a,c]				ADC ZP, X 2 4[c]	ROR ZP, X 2 6		SEI Implied 1 2	ADC ABS, Y 3 4[a,c]				ADC ABS, X 3 4[a,c]	ROR ABS, X 3 7	
8		STA (IND, X) 2 6			STY ZP 2 3	STA ZP 2 3	STX ZP 2 3		DEY Implied 1 2		TXA Implied 1 2		STY ABS 3 4	STA ABS 3 4	STX ABS 3 4	
9	BCC Relative 2 2[b]	STA (IND), Y 2 6			STY ZP, X 2 4	STA ZP, X 2 4	STX ZP, Y 2 4		TYA Implied 1 2	STA ABS, Y 3 5	TXS Implied 1 2			STA ABS, X 3 5		
A	LDY IMM 2 2	LDA (IND, X) 2 6	LDX IMM 2 2		LDY ZP 2 3	LDA ZP 2 3	LDX ZP 2 3		TAY Implied 1 2	LDA IMM 2 2	TAX Implied 1 2		LDY ABS 3 4	LDA ABS 3 4	LDX ABS 3 4	
B	BCS Relative 2 2[b]	LDA (IND), Y 2 5[a]			LDY ZP, X 2 4	LDA ZP, X 2 4	LDX ZP, Y 2 4		CLV Implied 1 2	LDA ABS, Y 3 4[a]	TSX Implied 1 2		LDY ABS, X 3 4[a]	LDA ABS, X 3 4[a]	LDX ABS, Y 3 4[a]	
C	CPY IMM 2 2	CMP (IND, X) 2 6			CPY ZP 2 3	CMP ZP 2 3	DEC ZP 2 5		INY Implied 1 2	CMP IMM 2 2	DEX Implied 1 2		CPY ABS 3 4	CMP ABS 3 4	DEC ABS 3 6	
D	BNE Relative 2 2[b]	CMP (IND), Y 2 5[a]				CMP ZP, X 2 4	DEC ZP, X 2 6		CLD Implied 1 2	CMP ABS, Y 3 4[a]				CMP ABS, X 3 4[a]	DEC ABS, X 3 7	
E	CPX IMM 2 2	SBC (IND, X) 2 6[c]			CPX ZP 2 3	SBC ZP 2 3[c]	INC ZP 2 5		INX Implied 1 2	SBC IMM 2 2[c]	NOP Implied 1 2		CPX ABS 3 4	SBC ABS 3 4[c]	INC ABS 3 6	
F	BEQ Relative 2 2[b]	SBC (IND), Y 2 5[a,c]				SBC ZP, X 2 4[c]	INC ZP, X 2 6		SED Implied 1 2	SBC ABS, Y 3 4[a,c]				SBC ABS, X 3 4[a,c]	INC ABS, X 3 7	

NOTES:

[a]Add 1 to N if page boundary is crossed.

[b]Add 1 to N if branch occurs to same page; add 2 to N if branch occurs to different page.

[c]Add 1 to N if in decimal mode.

0	
0	BRK Implied 1 7

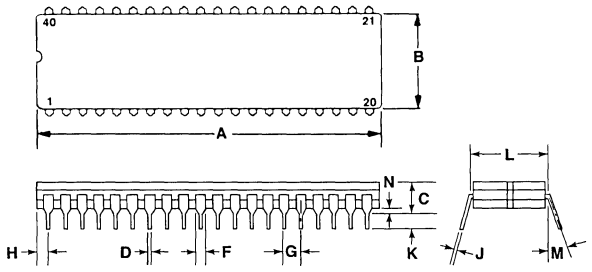
— OP Code
— Addressing Mode
— No. of Instruction Bytes (#); No. of Machine Cycles (n)

Table A-4. R65C10 Instruction Enhancements

Function	NMOS R6502 Microprocessor	CMOS R65C10 Microprocessor
Indexed addressing across page boundary.	Extra read of invalid address.	Extra read of last instruction byte.
Jump indirect, operand = XXFF.	Page address does not increment.	Page address increments and adds one additional cycle.
Read/modify/write instructions at effective address.	One read and two write cycles.	Two read and one write cycle.
Decimal flag.	Indeterminate after reset.	Initialized to binary mode (D = 0) after reset and interrupts.
Flags after decimal operation.	Invalid N, V and Z flags.	Valid flag adds one additional cycle.
Interrupt after fetch of BRK instruction.	Interrupt vector is loaded, BRK vector is ignored.	BRK is executed, then interrupt is executed.

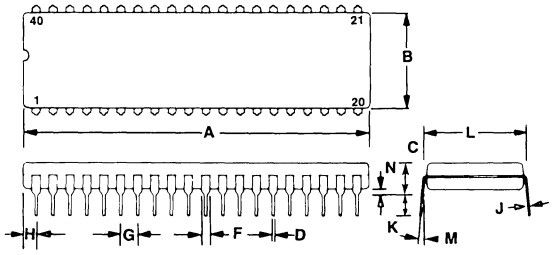
PACKAGE DIMENSIONS

40-PIN CERDIP



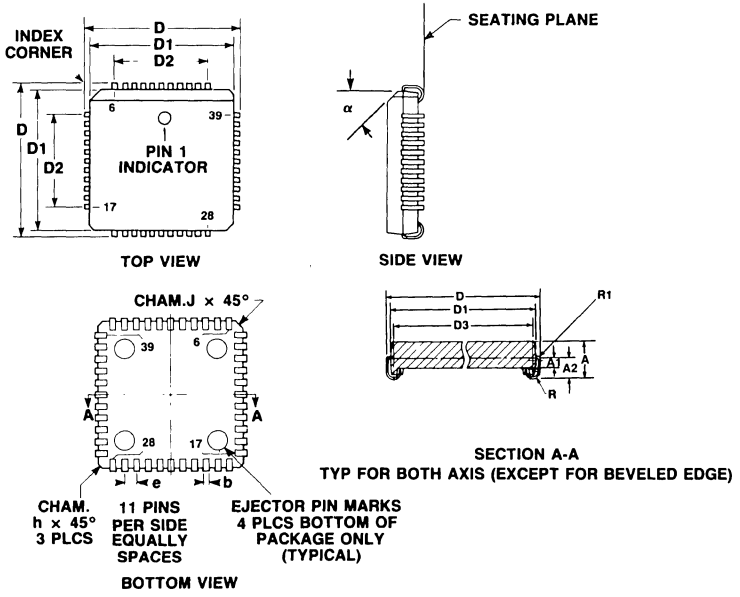
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	51 56	52 58	2.030	2.070
B	12.95	13.46	0.510	0.530
C	4 06	5 08	0 160	0.200
D	0 41	0.51	0.016	0 020
F	1.27	1.52	0.050	0.060
G	2.54 BSC		0.100 BSC	
H	1.78	2 29	0.070	0.090
J	0.20	0.30	0.008	0 012
K	3.05	4.06	0.120	0.160
L	15 24 BSC		0.600 BSC	
M	0°	10°	0°	10°
N	0.38	0.89	0.015	0.035

40-PIN PLASTIC DIP



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	51.82	52.32	2.040	2.060
B	13.46	13.97	0.530	0.550
C	3.56	5 08	0.140	0.200
D	0.38	0.53	0.015	0.021
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0 20	0.30	0.008	0.012
K	3.30	4.32	0.130	0.170
L	15.24 BSC		0.600 BSC	
M	7°	10°	7°	10°
N	0.51	1.02	0.020	0.040

44-PIN PLASTIC LEADED CHIP CARRIER (PLCC)



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.14	4.39	0.163	0.173
A1	1.37	1.47	0.054	0.058
A2	2.31	2 46	0.091	0.097
b	0.457 TYP		0.018 TYP	
D	17.45	17.60	0.687	0.693
D1	16.46	16.56	0 648	0.652
D2	12.62	12 78	0.497	0.503
D3	15.75 REF		0.620 REF	
e	1.27 BSC		0.050 BSC	
h	1.15 TYP		0.045 TYP	
J	0.25 TYP		0 010 TYP	
α	45° TYP		45° TYP	
R	0.89 TYP		0.035 TYP	
R1	0.25 TYP		0.010 TYP	

3

Rockwell

R6500/1
One-Chip Microcomputer

SECTION 1
INTRODUCTION

SUMMARY

The Rockwell R6500/1 microcomputer is a complete 8-bit computer fabricated on a single chip using an N-channel silicon gate MOS process. The R6500/1 complements an established and growing line of R6500 products and has a wide range of microcomputer applications.

The R6500/1 consists of an R6502 Central Processing Unit (CPU), 2048 bytes of Read Only Memory (ROM), 64 bytes of Random Access Memory (RAM) and interface circuitry for peripheral devices.

The innovative architecture and the demonstrated high performance of the R6502 CPU, as well as instruction simplicity, results in system cost-effectiveness and a wide range of computational power. These features make the R6500/1 a leading candidate for microcomputer applications.

To facilitate system and program development for the R6500/1, Rockwell has developed a 64-pin R6500/1E Emulator device, as well as a pin-compatible R6500/1EB Backpack Emulator device. For more information, refer to the data sheets for the R6500/1E (Order No. D51S) and the R6500/1EB (Order No. D60).

This product description is for the reader familiar with the R6502 CPU hardware and programming capabilities. A detailed description of the R6502 CPU hardware is included in the R6500 Microcomputer System Hardware Manual (Document Order No. 201). A description of the instruction capabilities of the R6502 CPU is contained in the R6500 Microcomputer Systems Programming Manual (Document Order No. 202).

ORDERING INFORMATION

Part Number:
R6500/1

- Temperature Range (T_L to T_H):
  - Blank = 0°C to +70°C
  - E = −40°C to +85°C
- Package
  - P = 40-Pin Plastic DIP
  - J = 44-Pin Plastic Leaded Chip Carrier (PLCC)
- Frequency
  - No Letter = 1 MHz
  - A = 2 MHz

FEATURES

- Single-chip microcomputer
- R6502 software compatible
- Eight-bit parallel processing
- Decimal or binary arithmetic
- Variable length stack
- True indexing capability
- Thirteen addressing modes
- 1 or 2 MHz clock operation, with the following options:
  - — External single clock input
  - — RC time base input
  - — Crystal time base input
- Single +5V power supply
- 500 mw operating power
- Separate power pin for RAM with standby power only 10% of operating power
- 2K x 8 ROM on chip
- 64 x 8 RAM on chip
- 40-pin DIP and 44-pin PLCC
- 64-pin R6500/1E Emulator part available, with 40 signals identical to production part
- 40-pin R6500/1EB Backback Emulator part available, pin compatible with an R6500/1
- Pipeline architecture
- 32 bidirectional TTL compatible I/O lines
  - — 1 positive edge sensitive I/O lines
  - — 1 negative edge sensitive I/O line
- 1 bidirectional TTL compatible counter I/O line
- 16-bit timer/counter
- Four timer/counter modes
  - — Internal timer
  - — Pulse generator
  - — Event counter
  - — Pulse width measurement
- Three maskable interrupts
  - — 1 counter overflow
  - — 2 I/O edge detect
- NMI and Reset interrupts

SECTION 2
INTERFACE REQUIREMENTS

This section describes the interface requirements for the R6500/1 single chip microcomputer. Figure 2-1 is the Interface Diagram for the R6500/1. Figure 2-2 shows the pin out configuration and Table 2-1 describes the function of each pin of the R6500/1.

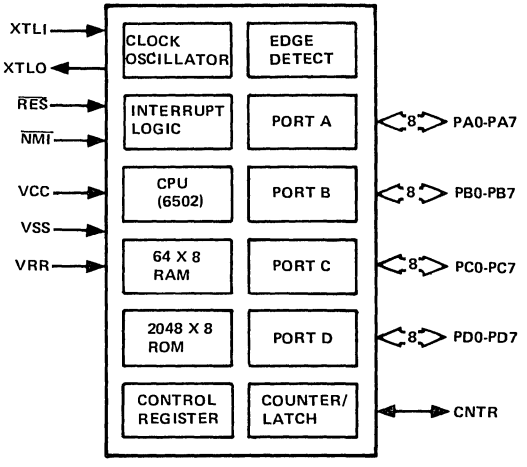


Figure 2-1. R6500/1 Interface Diagram

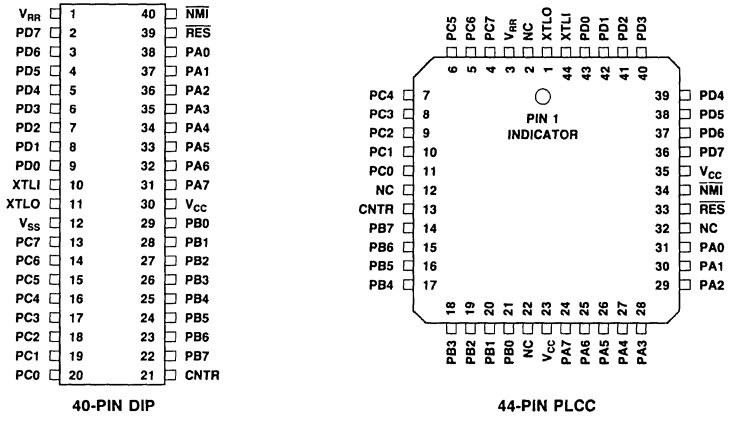


Figure 2-2. R6500/1 Pin Assignments

Table 2-1. R6500/1 Pin Description

Signal Name	I/O	Description
VCC		**Power.** Main power supply +5V.
VRR		**RAM Retention Power.** Separate power pin for RAM. In the event that VCC power is lost, this power retains RAM data +5V.
VSS		**Ground.** Signal and power ground (0V).
XTLI	I	**Crystal In.** Crystal or clock input for internal clock oscillator.
XTLO	O	**Crystal Out.** Crystal output from internal clock oscillator.
$\overline{RES}$	I	**Reset.** The Reset input is used to initialize the R6500/1. The signal must not transition from low to high for at least eight cycles after VCC reaches operating range and the internal oscillator has stabilized (see Section 5).
$\overline{NMI}$	I	**Non-Maskable Interrupt.** A negative going edge on the Non-Maskable Interrupt signal requests that a non-maskable interrupt be generated within the CPU.
PA0-PA7	I/O	**Port A.** General purpose I/O Port A.
PB0-PB7	I/O	**Port B.** General purpose I/O Port B.
PC0-PC7	I/O	**Port C.** General purpose I/O Port C.
PD0-PD7	I/O	**Port D.** General purpose I/O Port D.
		Four 8-bit ports used for either input/output. Each line consists of an active transistor to VSS and an optional passive pull-up to VCC. The two lower bits of the PA port (PA0-PA1) also serve as edge detect inputs with maskable interrupts.
CNTR	I/O	**Counter I/O.** This line is used as a Counter input/output line. CNTR is an input in the Event Counter and Pulse Width Measurement modes and is an output in the Interval Timer and Pulse Generator modes. It consists of an active transistor to VSS and an optional passive pull-up to VCC.

SECTION 3
SYSTEM ARCHITECTURE

This section provides a functional description of the R6500/1. A block diagram of the R6500/1 is presented in Figure 3-1.

3.1 INDEX REGISTERS

There are two 8-bit index registers, X and Y. Each index register can be used as a base to modify the address data program counter and thus obtain a new address — the sum of the program counter contents and the and the index register contents.

When executing an instruction which specifies indirect addressing, the CPU fetches the op code and the address, and modifies the address from memory by adding the index register to it prior to loading or storing the value of memory.

Indexing greatly simplifies many types of programs, especially those using data tables.

3.2 STACK POINTER

The Stack Pointer is an 8-bit register. It is automatically incremented and decremented under control of the microprocessor to perform stack manipulation in response to either user instructions or the interrupt lines $\overline{NMI}$ and $\overline{IRQ}$. The Stack Pointer must be initialized by the user program.

The stack allows simple implementation of multiple level interrupts, subroutine nesting and simplification of many types of data manipulation. The JSR, BRK, RTI and RTS instructions use the stack and Stack Pointer.

The stack can be envisioned as a deck of cards which may only be accessed from the top. The address of a memory location is stored (or "pushed") onto the stack. Each time data are to be pushed onto the stack, the Stack Pointer is placed on the Address Bus, data are written into the memory location addressed by the Stack Pointer, and the Stack Pointer is decremented by 1. Each time data are read (or "pulled") from the stack, the Stack Pointer is incremented by 1. The Stack Pointer is then placed on the Address Bus, and data are read from the memory location addressed by the Pointer.

3.3 ARITHMETIC AND LOGIC UNIT (ALU)

All arithmetic and logic operations take place in the ALU, including incrementing and decrementing internal registers

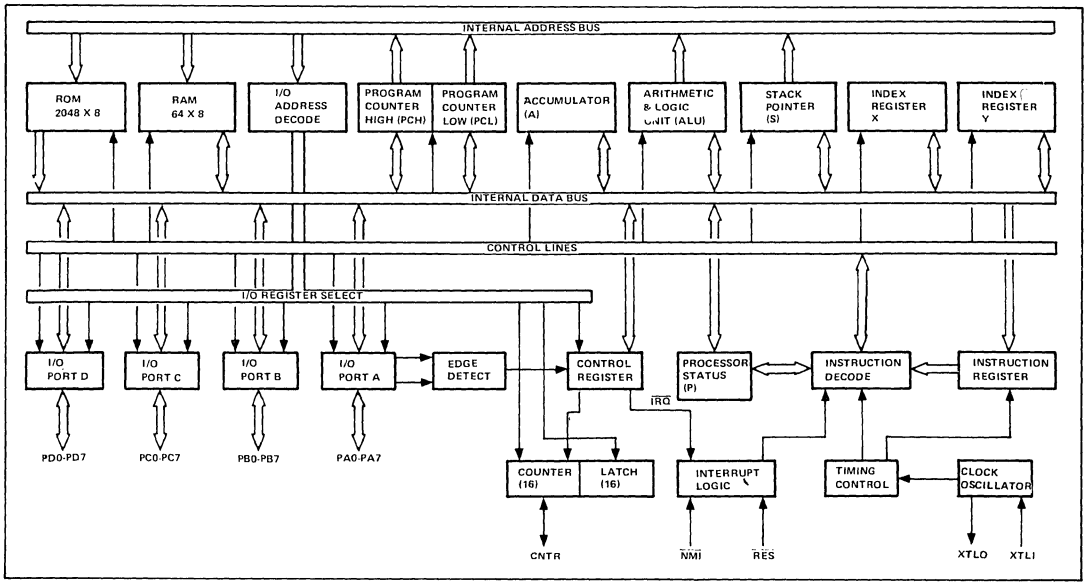


Figure 3-1. R6500/1 Block Diagram

(except the Program Counter). The ALU cannot store data for more than one cycle. If data are placed on the inputs to the ALU at the beginning of a cycle, the result is always gated into one of the storage registers or to external memory during the next cycle.

Each bit of the ALU has two inputs. These inputs can be tied to various internal buses or to a logic zero; the ALU then generates the function (AND, OR, SUM, and so on) using the data on the two inputs.

3.4 ACCUMULATOR

The accumulator is a general purpose 8-bit register that stores the results of most arithmetic and logic operations. In addition, the accumulator usually contains one of the two data words used in these operations.

3.5 PROGRAM COUNTER

The 12-bit Program Counter provides the addresses that are used to step the processor through sequential instructions in a program. Each time the processor fetches an instruction from program memory, the lower (least significant) byte of the Program Counter (PCL) is placed on the low-order bits of the Address Bus and the higher (most significant) byte of the Program Counter (PCH) is placed on the high-order 4 bits of the Address Bus. The Counter is incremented each time an instruction or data is fetched from program memory.

3.6 INSTRUCTION REGISTER AND INSTRUCTION DECODE

Instructions are fetched from ROM or RAM and gated onto the Internal Data Bus. These instructions are latched into the Instruction Register then decoded along with timing and interrupt signals to generate control signals for the various registers.

3.7 TIMING CONTROLS

The Timing Control Logic keeps track of the specific instruction cycle being executed. This logic is set to T0 each time an instruction fetch is executed and is advanced at the beginning of each Phase One clock pulse for as many cycles as are required to complete the instruction. Each data transfer which takes place between the registers is caused by decoding the contents of both the instruction register and timing control unit.

3.8 INTERRUPT LOGIC

Interrupt logic controls the sequencing of three interrupts; $\overline{RES}$, $\overline{NMI}$ and $\overline{IRQ}$. $\overline{IRQ}$ is generated by any one of three conditions: Counter Overflow, PA0 Positive Edge Detected, and PA1 Negative Edge Detected.

3.9 CLOCK OSCILLATOR

The Clock Oscillator provides the basic timing signals used by the R6500/1 CPU. The reference frequency is provided by an external source, and can be from a crystal or clock. The external frequency can vary from 200 kHz to 4 MHz. The internal Phase 2 ($\phi 2$) frequency is one-half the external reference frequency.

The on-chip oscillator is designed for a parallel resonant crystal connected between XTLI and XTLO pins. The equivalent oscillator circuit is shown in Figure 3-2.

A parallel resonant crystal is specified by its load capacitance and series resonant resistance. For proper oscillator operation, the load capacitance (C_L), series resistance (R_s) and the crystal resonant frequency (F) must meet the following two relations:

$$(C + 27) = 2C_L \quad \text{or} \quad C = 2C_L - 27$$

$$R_s \leq R_{smax} = \frac{2 \times 10^6}{(FC_L)^2}$$

where: F is in MHz; C and C_L are in pF; R is in ohms.

To select a parallel resonant crystal for the oscillator, first select the load capacitance from a crystal manufacturer's catalog. Next, calculate R_{smax} based on F and C_L. The selected crystal must have a R_s less than the R_{smax}.

For example, if C_L = 22 pF for a 4 MHz parallel resonant crystal, then

$$C = (2 \times 22) - 27 = 17 \text{ pF}$$
(use standard value, 18 pF)

The series resistance of the crystal must be less than

$$R_{smax} = \frac{2 \times 10^6}{(4 \times 22)^2} = 258 \text{ ohms}$$

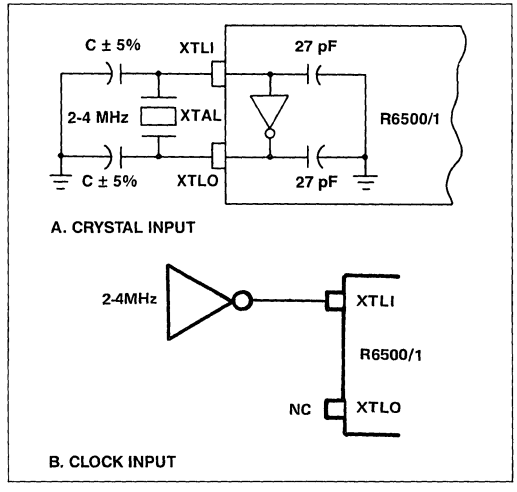


Figure 3-2. Clock Oscillator Input Options

3.10 PROCESSOR STATUS REGISTER

The 8-bit Processor Status Register, shown in Figure 3-3, contains seven status flags. Some of these flags are controlled by the user program; others may be controlled both by the user's program and the CPU. The R6500 instruction

set contains a number of conditional branch instructions which are designed to allow testing of these flags. Each of the eight processor status flags is described in the following sections.

3.10.1 CARRY BIT (C)

The Carry Bit (C) can be considered as the ninth bit of an arithmetic operation. It is set to logic 1 if a carry from the eighth bit has occurred or cleared to logic 0 if no carry occurred as the result of arithmetic operations.

The Carry Bit may be set or cleared under program control by use of the Set Carry (SEC) or Clear Carry (CLC) instruction, respectively. Other operations which affect the Carry Bit are ADC, ASL, CMP, CPX, CPY, LSR, PLP, ROL, ROR, RTI, and SBC.

3.10.2 ZERO BIT (Z)

The Zero Bit (Z) is set to logic 1 by the CPU during any data movement or calculation which sets all 8 bits of the result to zero. This bit is cleared to logic 0 when the resultant 8 bits of a data movement or calculation operation are not all zero. The R6500 instruction set contains no instruction to specifically set or clear the Zero Bit. The Zero Bit is, however, affected by the following instructions: ADC, AND, ASL, BIT, CMP, CPX, CPY, DEC, DEX, DEY, EOR, INC, INX, INY, LDA, LDX, LDY, LSR, ORA, PLA, PLP, ROL, ROR, RTI, SBC, TAX, TAY, TXA, TSX, and TYA.

3.10.3 INTERRUPT DISABLE BIT (I)

The Interrupt Disable Bit (I) is used to control the servicing of an interrupt request (IRQ). If the I Bit is reset to logic 0, the $\overline{IRQ}$ signal will be serviced. If the bit is set to logic 1, the $\overline{IRQ}$ signal will be ignored. The CPU will set the Interrupt Disable Bit to logic 1 if a RESET ($\overline{RES}$) or Non-Maskable Interrupt ($\overline{NMI}$) signal is detected.

The I bit is cleared by the Clear Interrupt (CLI) instruction, the Pull Processor Status from Stack (PLP) instruction, or as the result of executing a Return from Interrupt (RTI) instruction (providing the Interrupt Disable Bit was cleared prior to the interrupt). The Interrupt Disable Bit may be set or cleared under program control using a Set Interrupt Disable (SEI) or a Clear Interrupt Disable (CLI) instruction, respectively.

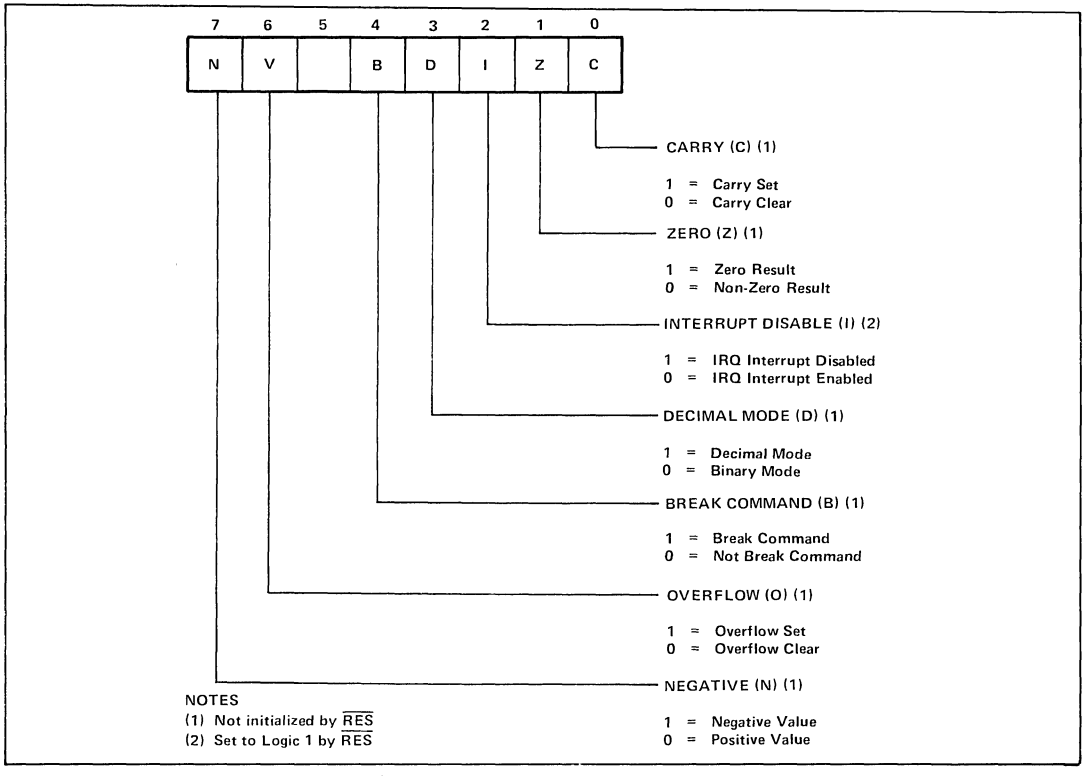


Figure 3-3. Processor Status Register

3.10.4 DECIMAL MODE BIT (D)

The Decimal Mode Bit (D), is used to control the arithmetic mode of the CPU. When this bit is set to logic 1, the adder operates as a decimal adder. When this bit is cleared to logic 0, the adder operates as a straight binary adder. The adder mode is controlled only by the programmer. The Set Decimal Mode (SED) instruction will set the D bit; the Clear Decimal Mode (CLD) instruction will clear it. The PLP and RTI instructions also effect the Decimal Mode Bit.

CAUTION

The Decimal Mode Bit will either set or clear in an unpredictable manner upon power application to R6500/1. This bit must be initialized to the desired state by the user program or erroneous results may occur.

3.10.5 BREAK BIT (B)

The Break Bit (B) is used to determine the condition which caused the $\overline{IRQ}$ service routine to be entered. If the $\overline{IRQ}$ service routine was entered because the CPU executed a BRK command, the Break Bit will be set to logic 1. If the $\overline{IRQ}$ routine was entered as the result of an $\overline{IRQ}$ signal being generated, the B bit will be cleared to logic 0. There are no instructions which can set or clear this bit.

3.10.6 OVERFLOW BIT (V)

The Overflow Bit (V) is used to indicate that the result of a signed, binary addition, or subtraction, operation is a value that cannot be contained in seven bits ($-128 \leq n \leq 127$). This indicator only has meaning when signed arithmetic (sign and seven magnitude bits) is performed. When the ADC or SBC instruction is performed, the Overflow Bit is set to logic 1 if the polarity of the sign bit (bit 7) is changed because the result exceeds +127 or -128; otherwise the bit is cleared to logic 0. The V bit may also be cleared by the programmer using a Clear Overflow (CLV) instruction.

The Overflow Bit may also be used with the BIT instruction. The BIT instruction which may be used to sample interface devices, allows the overflow flag to reflect the condition of bit 6 in the sampled field. Duriing a BIT instruction the Overflow Bit is set equal to the content of the bit 6 on the data tested with BIT instruction. When used in this mode, the overflow has nothing to do with signed arithmetic, but is just another sense bit for the microprocessor. Instructions which affect the V flag are ADC, BIT, CLV, PLP, RTI and SBC.

3.10.7 NEGATIVE BIT (N)

The Negative Bit (N) is used to indicate that the sign bit (bit 7), in the resulting value of a data movement or data arithmetic operation, is set to logic 1. If the sign bit is set to logic 1, the resulting value of the data movement or arithmetic operation is negative; if the sign bit is cleared, the result of the data movement or arithmetic operation s positive. There are no instructions that set or clear the Negative Bit since the Negative Bit represents only the status of a result. The instructions that effect the state of the Negative Bit are: ADC, AND, ASL, BIT, CMP, CPX, CPY, DEC, DEX, DEY, EOR, INC, INX, INY, LDA, LDX, LDY, LSR, ORA, PLA, PLP, ROL, ROR, RTI, SBC, TAX, TAY, TSX, TXA, and TYA.

3.11 2K × 8 ROM

The R6500/1 2048 byte × 8-bit Read Only Memory (ROM) usually contains the user's program instructions and other fixed constants. These program instructions and constants are mask-programmed into the ROM during fabrication of the R6500/1 device. The R6500/1 ROM is memory mapped from 800 to FFF.

3.12 64 × 8 RAM

The 64 byte × 8-bit Random Access Memory (RAM) contains the user program stack and is used for scratchpad memory during system operation. This RAM is completely static in operation and requires no clock or dynamic refresh. The data contained in RAM is read out nondestructively with the same polarity as the input data. A standby power pin, V_{RR} allows RAM memory to be maintained on 10% of the operating power. In the event that VCC power is lost and execution stops, this standby power retains RAM data until execution resumes.

In order to take advantage of zero page addressing capabilities, the R6500/1 RAM is assigned page zero memory address 0 to 03F.

3.13 CONTROL REGISTER

The Control Register (CR), shown in Figure 3-4, is located at address 08F. The CR contains five control signals and three status signals.

The control signals are summarized in Table 3-1. The control signals are set to logic 1 by writing logic 1 into the respective bit positions and cleared to logic 0 either by writing logic 0 into the respective bit position or by the occurrence of a $\overline{RES}$ signal.

Table 3-1. CR Control Signals

Control Signal Name	Bit Number
Counter Mode Control 0 (CMC0)	0
Counter Mode Control 1 (CMC1)	1
PA1 Interrupt Enabled (A1IE)	2
PA0 Interrupt Enabled (A0IE)	3
Counter Interrupt Enabled (CIE)	4

The three status signals are summarized in Table 3-2.

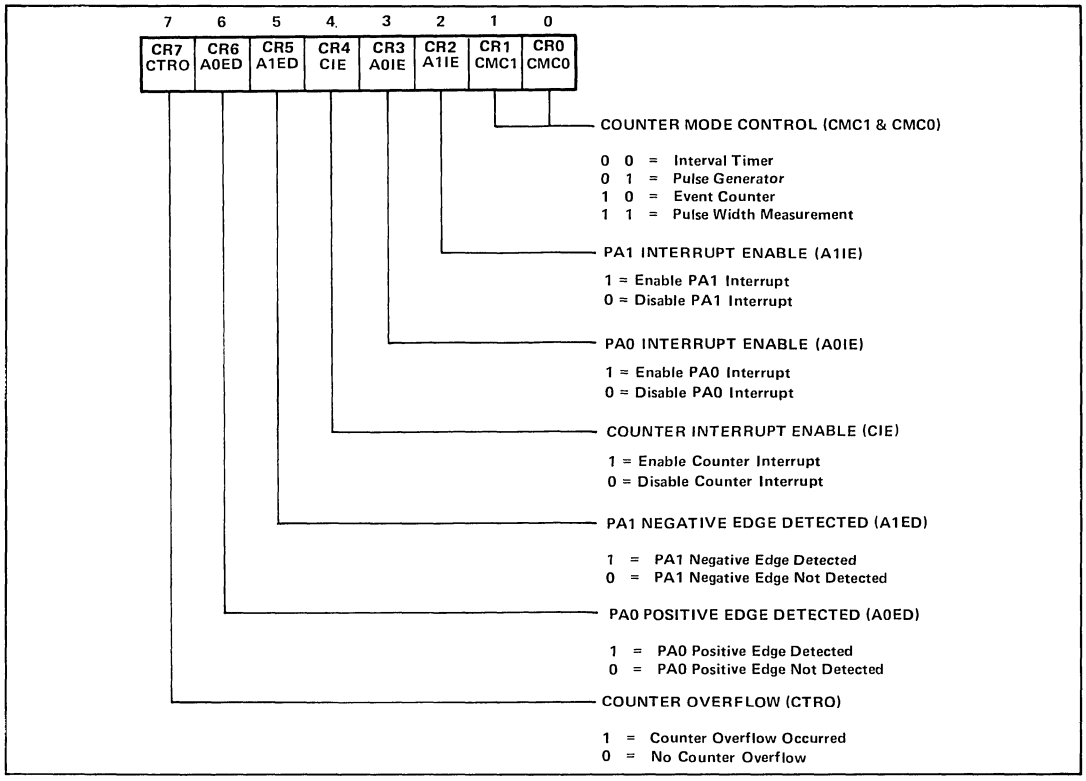


Figure 3-4. Control Register (CR)

Table 3-2. CR Status Signals

Status Signal Name	Bit Number
PA1 Negative Edge Detected (A1ED)	5
PA0 Positive Edge Detected (A0ED)	6
Counter Overflow (CTRO)	7

The status signals are read-only information. The status bits are set to logic 1 by hardware monitoring logic and cleared to logic 0 by the occurrence of $\overline{RES}$ signal or by specific address commands. Each of these signals is described in the following sections.

3.13.1 COUNTER MODE CONTROL 0 AND 1

Counter Mode Control signals CMC0 and CMC1 (bits 0 and 1) control the Counter operating modes. The modes of operation and the corresponding configuration of CMC0 and CMC1 are summarized in Table 3-3.

These modes are controlled by writing the appropriate bit values into the Counter Mode Control bits.

Table 3-3. Counter Mode Control Selection

CMC1 (Bit 1)	CMC0 (Bit 0)	Mode
0	0	Interval Timer
0	1	Pulse Generator
1	0	Event Counter
1	1	Pulse Width Measurement

The Counter is set to the Interval Timer Mode (00) when a $\overline{RES}$ signal is generated or if the user program stores logic 0 into Bits 0 and 1 of the Control Register. A complete description of each of the Counter modes is given in Section 3.14.1.

3.13.2 PA1 INTERRUPT ENABLE BIT (A1IE)

If the PA1 Interrupt Enable Bit (CR2) is set to logic 1, an $\overline{IRQ}$ interrupt request signal will be generated when the PA1 Negative Edge Detected Bit (CR5) is set.

3.13.3 PA0 INTERRUPT ENABLE BIT (A0IE)

If the PA0 Interrupt Enable Bit (CR3) is set to logic 1, the $\overline{IRQ}$ interrupt request signal will be generated when the PA0 Positive Edge Detected Bit (CR6) is set.

3.13.4 COUNTER INTERRUPT ENABLE BIT (CIE)

If the Counter Interrupt Enable Bit (CR4) is set to logic 1, the $\overline{IRQ}$ interrupt request signal will be generated when Counter Overflow (CR7) is set.

3.13.5 PA1 NEGATIVE EDGE DETECTED BIT (A1ED)

The PA1 Negative Edge Detected Bit (CR5) is set to logic 1 whenever a negative (falling) edge is detected on PA1. This bit is cleared to logic 0 by $\overline{RES}$ or by writing to address 08A.

The edge detecting circuitry is active when PA1 is used either as an input or as an output. When PA1 is used as an output, A1ED will be set when the negative edge is detected during a logical 1 to 0 transition.

When PA1 is used as an input and the negative edge detecting circuitry is used, A1ED should be cleared by the user program upon initialization and when the PA1 Negative Edge Detected $\overline{IRQ}$ processing is completed.

3.13.6 PA0 POSTIIVE EDGE DETECTED BIT (A0ED)

The PA0 Positive Edge Detected Bit (CR6) is set to logic 1 whenever a positive (rising) edge is detected on PA0. The bit is cleared to logic 0 by $\overline{RES}$ or by writing to address 089.

The edge detecting circuitry is active when PA0 is used either as an input or as an output. When PA0 is used as an output, A0ED will be set when the positive edge is detected during a logical 0 to 1 transition.

When PA0 is used as an input and the positive edge detecting circuitry is used, A0ED should be cleared by the user program upon initialization and upon completion of PA0 Positive Edge Detected $\overline{IRQ}$ processing.

3.13.7 COUNTER OVERFLOW BIT (CTRO)

The Counter Overflow Bit (CR7) is set to logic 1 whenever a counter overflow occurs in any of the four counter operating modes. Overflow occurs when the counter is decremented one count from 0000. This bit is cleared to logic 0 by $\overline{RES}$ or by reading from address 087 or writing to address 088.

This bit should be cleared by the user program upon initialization and upon completion of Counter Overflow $\overline{IRQ}$ interrupt processing.

When a Counter Overflow occurs, the Upper Count (UC) in address 086 and the Lower Count (LC) in address 087 are reset to the values contained in the Upper Latch (UL) in address 084 and in the Lower Latch (LL) in address 085, respectively. Therefore, it is important to load the Lower Latch value prior to executing the Write to Upper Latch and Transfer Latch to Counter (address 088) in order to prevent an unpredicted reoccurrence of Counter Overflow and, if enabled, an $\overline{IRQ}$ interrupt request.

3.14 COUNTER/LATCH

The Counter/Latch consists of a 16-bit Counter and a 16-bit Latch. The Counter resides in two 8-bit registers: address 086 contains the Upper Count value (bits 8-15 of the Counter) and address 087 contains the Lower Count value (bits 0-7 of the Counter). The Counter contains the count of either Ø2 clock periods or external events depending on which counter mode is selected in the Control Register (Section 3.13.1).

The Latch contains the Counter initialization value. The Latch resides in two 8-bit registers: address 084 contains the Upper Latch value (bits 8-15 of the Latch) and address 085 contains the Lower Latch value (bits 0-7 of the Latch). The 16-bit Latch can hold values from 0 to 65535.

The Latch registers can be loaded at any time by executing a write to the Upper Latch Address (084) and the Lower Latch Address (085). In each case, the contents of the Accumulator are copied into the applicable Latch register. The Upper Latch and Lower Latch can be loaded independently; it is not required to load both registers at the same time or sequentially. The Upper Latch can also be loaded by writing to address 088.

The Counter can be initialized at any time by writing to address 088. The contents of the Accumulator will be copied into the Upper Latch before the value in the Upper Latch is transferred to the Upper Counter.

The Counter will also be initialized to the Latch value whenever the Counter overflows. When the Counter decrements from 0000, the next Counter value will be the Latch value, not FFFF.

Whenever the Counter overflows, the Counter Overflow Bit (CR7) is set to logic 1. This bit is cleared whenever the lower eight bits of the counter are read from address 087 or by writing to address 088.

3.14.1 COUNTER MODES

The Counter operates in any of four modes. These modes are selected by the Counter Mode Control bits in the Control Register.

Mode	CMC1	CMC0
Interval Timer	0	0
Pulse Generator	0	1
Event Counter	1	0
Pulse Width Measurement	1	1

The Interval Timer, Pulse Generator, and Pulse Width Measurement Modes are ∅2 clock counter modes. The Event Counter Mode counts the occurrences of an external event on the CNTR line.

Interval Timer (Mode 0)

In the Interval Timer mode the Counter is initialized to the Latch value by either of two conditions:

1. When the Counter is decremented from 0000, the next Counter value is the Latch value (not FFFF).
2. When a write operation is performed to the Load Upper Latch and Transfer Latch to counter address (088), the Counter is loaded with the Latch value. Note that the contents of the Accumulator are loaded into the Upper Latch before the Latch value is transferred to the Counter.

The Counter value is decremented by one count at the ϕ2 clock rate. The 16-bit Counter can hold from 1 to 65535 counts. The Counter Timer capacity is therefore 1μs to 65.535ms at the 1 MHz ∅2 clock rate or 0.5μs to 32.768ms at the 2 MHz ϕ2 clock rate. Time intervals greater than the maximum Counter value can be easily measured by counting $\overline{IRQ}$ interrupt requests in the counter $\overline{IRQ}$ interrupt routine.

When the Counter decrements from 0000, the Counter Overflow (CR7) is set to logic 1 at the next ∅2 clock pulse. If the Counter Interrupt enable bit (CR4) is also set, an $\overline{IRQ}$ interrupt request will be generated. The Counter Overflow bit in the Control Register can be examined in the $\overline{IRQ}$ interrupt routine to determine that the $\overline{IRQ}$ was generated by the Counter Overflow.

While the timer is operating in the Interval Timer Mode, the Counter Out/Event line is held in the high (output disabled) state.

A timing diagram of the Interval Timer Mode is shown in Figure 3-5.

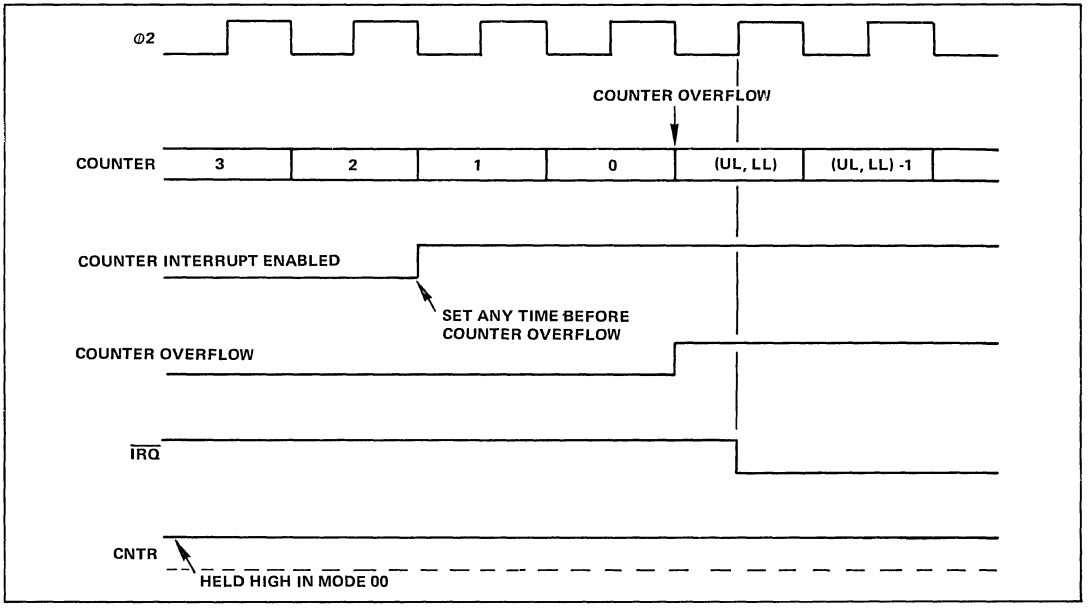


Figure 3-5. Interval Timer (Mode 0) Timing Diagram

Pulse Generator Mode (Mode 1)

In the Pulse Generator mode, the Counter Out/Event In line (CNTR) operates as a Counter Out. The CNTR line toggles from low to high or from high to low whenever a Counter Overflow occurs, or a write is performed to address 088.

Either a symmetric or asymmetric output waveform can be output on the CNTR line in this mode. The CNTR output is initialized high by a $\overline{RES}$ since the Interval Timer mode is established by $\overline{RES}$.

A one-shot waveform can be easily generated by changing from Mode 1 Pulse Generator to Mode 0 (Interval Timer) after only one occurrence of the output toggle condition.

Event Counter Mode (Mode 2)

In this mode the CNTR line is used as an Event Counter. The Counter will decrement with each rising edge detected on this line. The maximum rate at which this edge can be detected is one-half the Ø2 clock rate.

The Counter can count up to 65,535 occurrences before overflowing. As in the other modes, the Counter Overflow bit (CR7) is set to logic 1 if the overflow occurs.

Figure 3-6 is a timing diagram of the Event Counter Mode.

Pulse Width Measurement Mode (Mode 3)

This mode allows the accurate measurement of a low pulse duration on the CNTR line. In this mode, CNTR is used in the Event In capacity. The Counter decrements by one count at the Ø2 clock rate as long as the CNTR line is held in the low state. The Counter is stopped when CNTR is in the high state.

If the CNTR pin is left disconnected, this mode may be selected to stop the Counter since the internal pull-up device will cause the CNTR input to be in the high (>2.0V) state.

A timing diagram for the Pulse Width Measurement Mode is shown in Figure 3-7.

3.15 INPUT/OUTPUT PORTS

The R6500/1 provides four 8-bit Input/Output (I/O) ports (PA, PB, PC, PD). These 32 I/O lines are completely bidirectional. All lines may be used either for input or output in any combination; that is, there are no line grouping or port association restrictions.

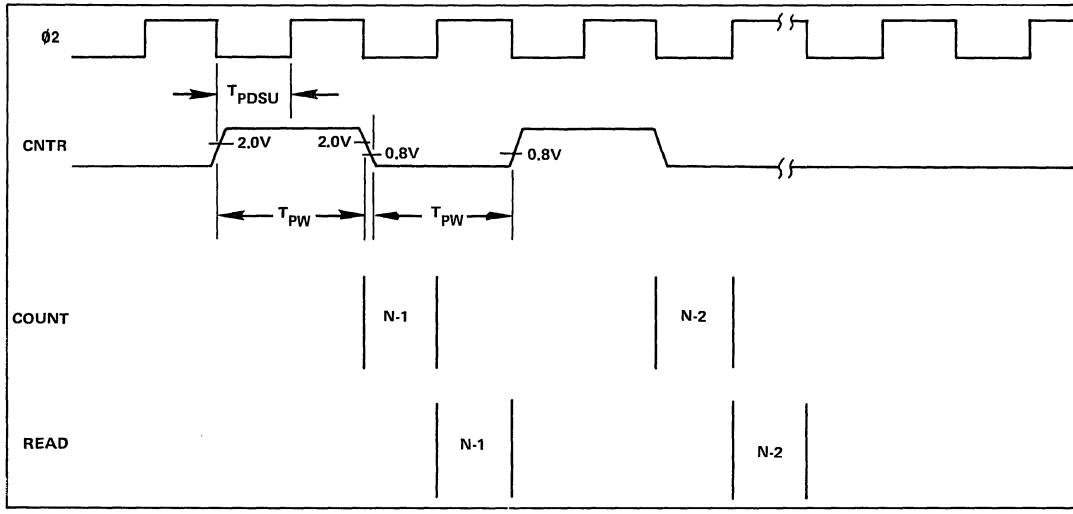


Figure 3-6. Event Counter Mode (Mode 2)

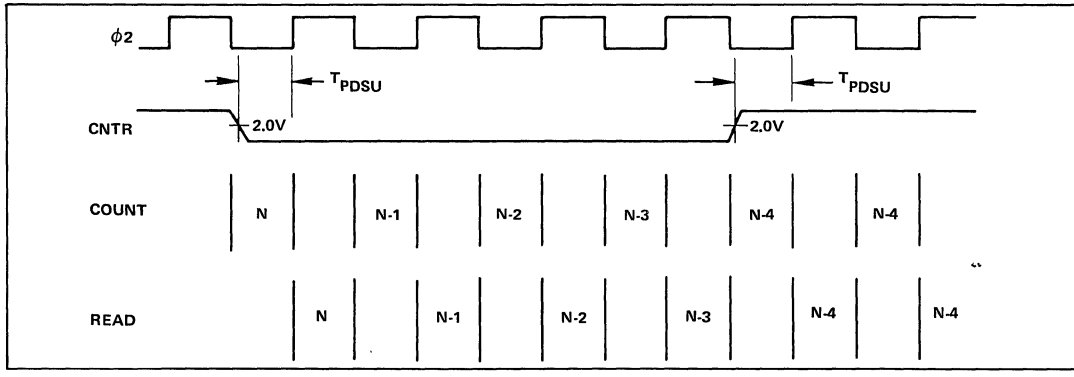


Figure 3-7. Pulse Width Measurement (Mode 3)

The direction of the 32 I/O lines are controlled by four 8-bit port registers located in page zero. This arrangement provides quick programming access using simple two-byte zero page address instructions. There are no direction registers associated with the I/O ports, which simplifies I/O handling. The I/O addresses are shown in Table 3-4.

Table 3-4. I/O Port Addresses

Port	Address
A	080
B	081
C	082
D	083

Figure 3-8 shows the I/O Port Timings.

3.15.1 INPUTS

Inputs are enabled by loading logic 1 into all I/O port register bit positions that are to correspond to I/O input lines. A low (<0.8V) input signal will cause a logic 0 to be read when a read instruction is issued to the port register. A high (>2.0V) input will cause a logic 1 to be read. An $\overline{RES}$ signal forces all I/O port registers to logic 1 thus initially treating all I/O lines as inputs.

The status of the input lines can be interrogated at any time by reading the I/O port addresses. Note that this will return the actual status of the input lines, not the data written into the I/O port registers.

3.15.2 OUTPUTS

Outputs are controlled by writing the desired I/O line output states into the corresponding I/O port register bit positions. A logic 1 will force a high (>2.4V) output while a logic 0 will force a low (<0.4V) output.

3.15.3 EDGE DETECTION CAPABILITY

Ports PA0 and PA1 have an edge detection capability. Figure 3-9 shows the edge detection timing.

PA0 Positive Edge Detecting Capability

In addition to its normal I/O function, PA0 will detect an asynchronous positive (rising) edge signal and set the PA0 Positive Edge Detected signal (CR6) to logic 1. The maximum rate at which this positive edge can be detected is one-half the ø2 clock rate.

If the PA0 Interrupt Enable Bit (CR3) is set, an $\overline{IRQ}$ interrupt request will also be generated. The PA0 Positive Edge Detected signal can be cleared by writing to address 089.

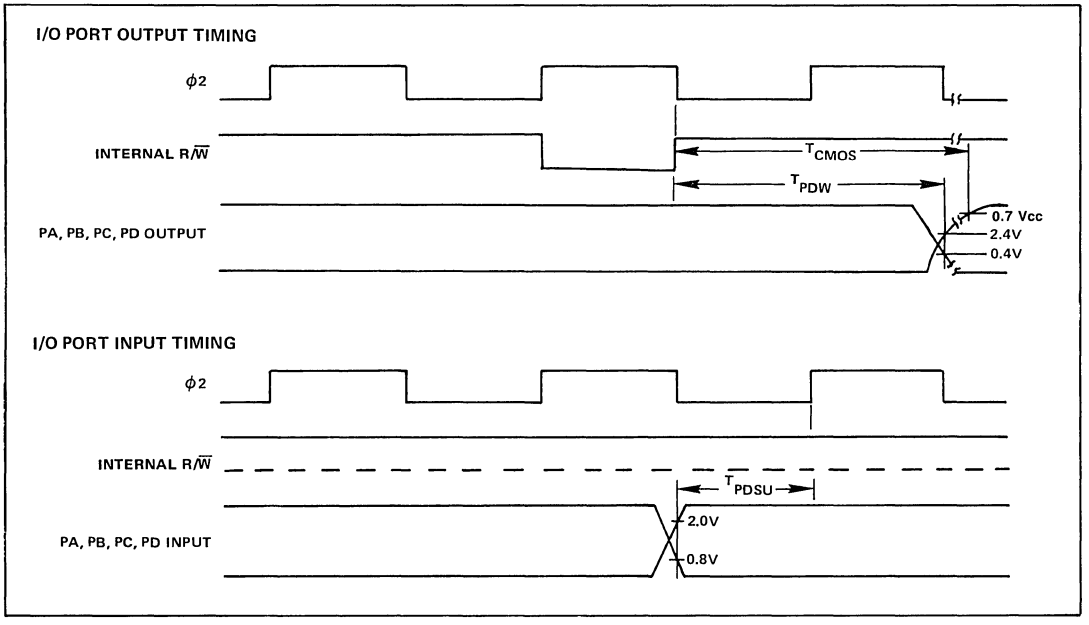


Figure 3-8. I/O Port Timing

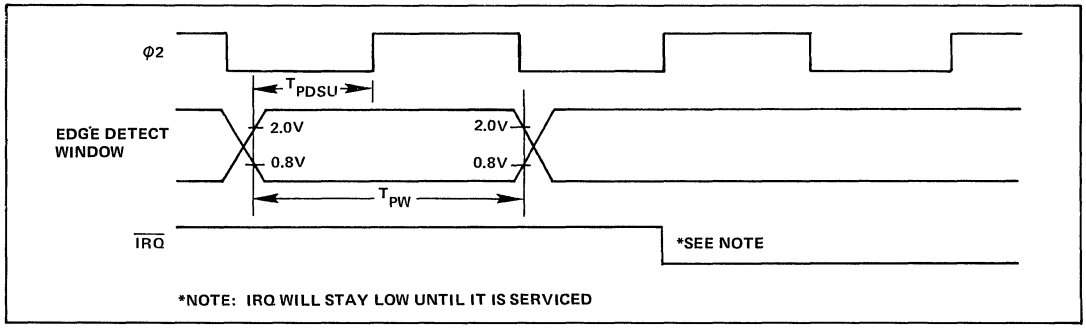


Figure 3-9. PA0 and PA1 Edge Detection Timing

PA1 Negative Edge Detecting Capability

In addition to its normal I/O function, PA1 will detect an asynchronous negative (falling) edge signal and set the PA1 Negative Edge Detected signal (CR5) to logic 1. The maximum rate at which this negative edge can be detected is one-half the ϕ2 clock rate.

If the PA1 Interrupt Enable signal (CR2) is set, an $\overline{IRQ}$ interrupt request will also be generated. The PA1 Negative Edge Detected signal may be cleared by writing to address 08A.

3.16 MASK OPTIONS

An option is provided to delete the internal pull-up resistance from PA, PB, PC and/or PD ports at mask time. This option is available for 8-bit port groups only, not for individual port lines. This option may by used to aid interface with CMOS drivers, or in order to interface with external pull-up devices.

An option is also provided to delete the internal pull-up resistance on the CNTR line.

SECTION 4
$\overline{\text{IRQ}}$ INTERRUPT REQUEST GENERATION

An $\overline{\text{IRQ}}$ interrupt request can be initiated by any or all of three possible sources. These sources are all capable of being enabled or disabled by the use of the appropriate interrupt enabled bits in the Control Register.

The first source of $\overline{\text{IRQ}}$ is Counter Overflow. The $\overline{\text{IRQ}}$ interrupt request will be driven low whenever both the Counter Interrupt Enable (CR4) and the Counter Overflow (CR7) are logic 1.

The second source of $\overline{\text{IRQ}}$ is detection of a positive edge on PA0. The $\overline{\text{IRQ}}$ inerrupt request will be driven low whenever both the PA0 Interrupt Enable (CR3) and the PA0 Positive Edge Detected (CR6) are logic 1.

The third source of $\overline{\text{IRQ}}$ is detection of a negative edge on PA1. The $\overline{\text{IRQ}}$ interrupt request will be driven low whenever both the PA1 Interrupt Enable (CR2) and the PA1 Negative Edge Detected (CR5) are logic 1.

Multiple simultaneous interrupts will cause the $\overline{\text{IRQ}}$ interrupt request to remain active until all interrupting conditions have been serviced and cleared.

CAUTION

If the same data, i.e., the same RAM, counter/latch or I/O addresses, are operated on asynchronously by a normal processing routine and by an interrupt service routine, care must be taken to prevent loss of data due to the interrupt routine altering the data during update of the data by the normal processing routine. This situation can be prevented by disabling the $\overline{\text{IRQ}}$ interrupt with the SEI instruction before starting the data update in the normal processing and then enabling the interrupt with the CLI instruction upon completion of data update.

SECTION 5
POWER ON/OFF CONSIDERATIONS

5.1 POWER-ON RESET

The occurrence of $\overline{RES}$ going from low to high will cause the R6500/1 to set the Interrupt Mask Bit — bit 2 of the Processor Status Register — and initiate a reset vector fetch at address FFE and FFF to begin user program execution. All of the I/O ports (PA, PB, PC, and PD) and CNTR will be forced to the high (logic 1) state. All bits of the Control Register will be cleared to logic 0 causing the Interval Timer counter mode (mode 00) to be selected and causing all interrupt enabled bits to be reset.

5.2 POWER ON/OFF TIMING

After application of VCC power to the R6500/1, $\overline{RES}$ must be held low for at least eight Ø2 clock cycles after VCC reaches operating range and the internal clock oscillator has stabilized. This stabilization time is dependent upon the input VCC voltage and performance of the crystal, clock, or RC network input circuit. The clock oscillator output can be monitored on XTLO (pin 11).

Figure 5-1 illustrates the power turn-on waveforms.

5.3 RAM DATA RETENTION — VRR REQUIREMENTS

For the RAM to retain data upon loss of VCC, VRR must be supplied within operating range and $\overline{RES}$ must be driven low at least eight Ø2 clock pulses before VCC falls out of operating range. $\overline{RES}$ must then be held low while VCC is out of operating range and until at least eight Ø2 clock cycles after VCC is again within operating range and the internal Ø2 oscillator is stabilzed. VRR must remain within VCC operation range during normal R6500/1 operation. When VCC is out of operating range, VRR must remain within the VRR retention range in order to retain data. Figure 5-2 shows typical waveforms.

5.4 RAM DATA RETENTION OPERATION

The requirement for R6500/1 RAM data retention and restart operation is application dependent. If R6500/1 RAM data retention is not required during loss of VCC, then VRR can be connected to the same power source as VCC. With this configuration a complete initialization of R6500/1 program variables in RAM is required upon VCC and VRR power application.

If the R6500/1 RAM is to retain data during loss of VCC, the following is required:

1. Connection of VCC and VRR to separate power supplies or to the same primary power supply with isolation diodes and battery or other backup power for VRR.
2. VCC power monitor hardware with power loss and cold/warm start indications to the R6500/1.
3 Power loss detection as well as cold and warm start initialization in the R6500/1 program.

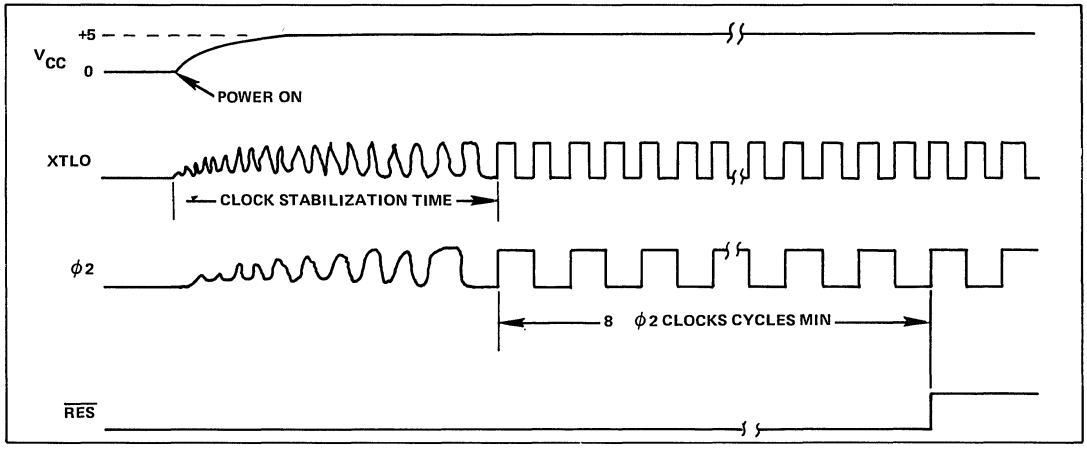
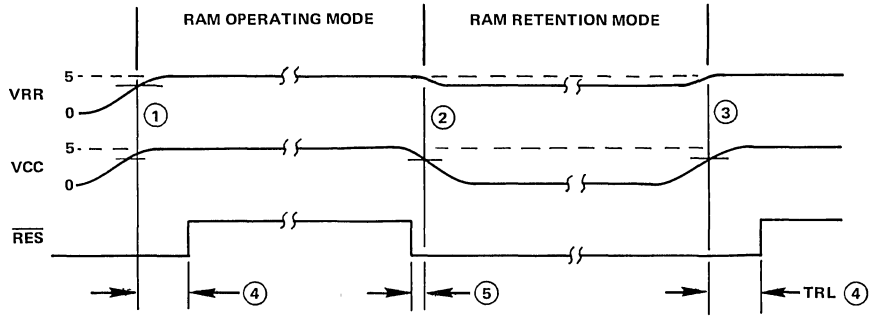


Figure 5-1. Power Turn-On Timing Detail



1. INITIAL APPLICATION OF VCC AND VRR.
2. LOSS OF VCC, RAM ON STANDBY POWER.
3. REAPPLICATION OF VCC.
4. ≥8 ϕ2 CLOCK PULSES AFTER ϕ2 OSCILLATOR STABILIZATION.
5. ≥8 ϕ2 CLOCK PULSES.

Figure 5-2. RAM Retention Mode Timing

The power monitor hardware must sense the loss of VCC power in sufficient time to allow the R6500/1 to save required CPU register data in RAM. The power loss indication line can be connected to the $\overline{\text{NMI}}$ interrupt input in order to cause an immediate R6500/1 interrupt upon power loss detection.

The power monitor hardware should also provide an indication of cold start (initial VCC and VRR power application) or warm start (VCC power re-application while VRR is retained on backup power) provided as input on a data I/O pin.

A level indication is sufficient. The R6500/1 program can then initialize all, or partial, program variables upon initialization then jump to any other starting address as required depending upon cold/warm start condition.

Upon power loss detection, the R6500/1 should save all required CPU register data in either the stack or dedicated RAM. The stack may be preferred if dedicated RAM is not available. If the program is to restart at the interrupted address, then all CPU registers must be saved, i.e., S, P, PC, A, X, and Y. The stack pointer must be saved in a dedicated RAM address. Note that processor status P and the program counter, PC, are already saved on the stack by the NMI interrupt R6500/1 hardware processing. If the warm start can be performed at a specific address, then the saving of the register data at power loss detection may not be required. Figure 5-3 shows top level flowcharts of typical power down and power-up processing.

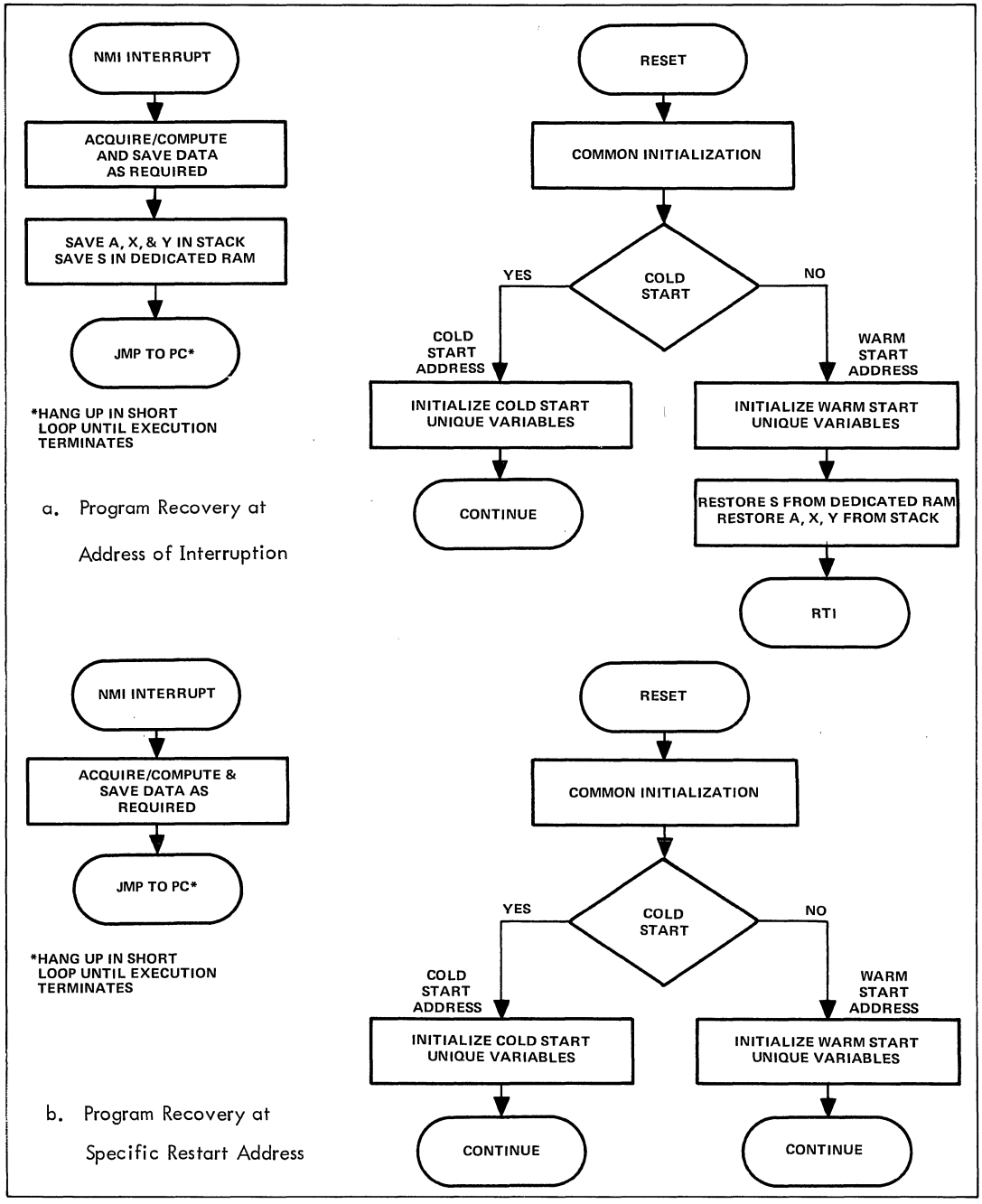
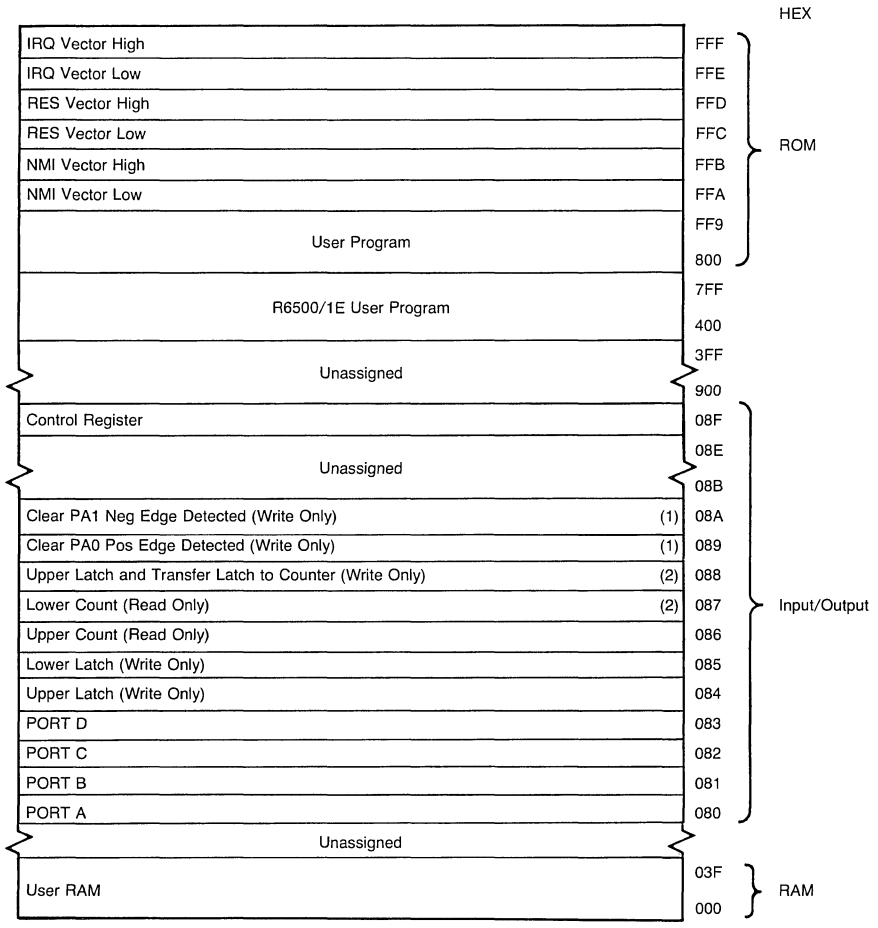


Figure 5-3. Typical R6500/1 Power Loss Recovery Flowcharts

APPENDIX A — SYSTEM MEMORY MAP



Notes:
(1) I/O command only; i.e., no stored data.
(2) Clears Counter Overflow — Bit 7 in Control Register.

APPENDIX B — R6500 INSTRUCTION SET

This appendix contains a summary of the R6500 instruction set. For detailed information, consult the R6500 Microcomputer System Programming Manual, Document Order No. 202.

B.1 INSTRUCTION SET IN ALPHABETIC SEQUENCE

Mnemonic	Description	Mnemonic	Description
ADC	Add Memory to Accumulator with Carry	LDA	Load Accumulator with Memory
AND	"AND" Memory with Accumulator	LDX	Load Index X with Memory
ASL	Shift Left One Bit (Memory or Accumulator)	LDY	Load Index Y with Memory
		LSR	Shift One Bit Right (Memory or Accumulator)
BCC	Branch on Carry Clear		
BCS	Branch on Carry Set	NOP	No Operation
BEQ	Branch on Result Zero		
BIT	Test Bits in Memory with Accumulator	ORA	"OR" Memory with Accumulator
BMI	Branch on Result Minus		
BNE	Branch on Result not Zero	PHA	Push Accumulator on Stack
BPL	Branch on Result Plus	PHP	Push Processor Status on Stack
BRK	Force Break	PLA	Pull Accumulator from Stack
BVC	Branch on Overflow Clear	PLP	Pull Processor Status from Stack
BVS	Branch on Overflow Set		
		ROL	Rotate One Bit Left (Memory or Accumulator)
CLC	Clear Carry Flag	ROR	Rotate One Bit Right (Memory or Accumulator)
CLD	Clear Decimal Mode	RTI	Return from Interrupt
CLI	Clear Interrupt Disable Bit	RTS	Return from Subroutine
CLV	Clear Overflow Flag		
CMP	Compare Memory and Accumulator	SBC	Subtract Memory from Accumulator with Borrow
CPX	Compare Memory and Index X	SEC	Set Carry Flag
CPY	Compare Memory and Index Y	SED	Set Decimal Mode
		SEI	Set Interrupt Disable Status
DEC	Decrement Memory by One	STA	Store Accumulator in Memory
DEX	Decrement Index X by One	STX	Store Index X in Memory
DEY	Decrement Index Y by One	STY	Store Index Y in Memory
EOR	"Exclusive-Or" Memory with Accumulator	TAX	Transfer Accumulator to Index X
		TAY	Transfer Accumulator to Index Y
INC	Increment Memory by One	TSX	Transfer Stack Pointer to Index X
INX	Increment Index X by One	TXA	Transfer Index X to Accumulator
INY	Increment Index Y by One	TXS	Transfer Index X to Stack Register
		TYA	Transfer Index Y to Accumulator
JMP	Jump to New Location		
JSR	Jump to New Location Saving Return Address		

B2. INSTRUCTION SET SUMMARY TABLE

INSTRUCTIONS		IMMEDIATE			ABSOLUTE			ZERO PAGE			ACCUM			IMPLIED			(IND, X)			(IND), Y			Z PAGE, X			ABS X			ABS, Y			RELATIVE			INDIRECT			Z PAGE, Y			PROCESSOR STATUS CODES	
MNEMONIC	OPERATION	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	7 6 5 4 3 2 1 0 N V * B D I Z C	MNEMONIC
ADC	A + M + C → A (4) (1)	69	2	2	6D	4	3	65	3	2							61	6	2	71	5	2	75	4	2	7D	4	3	79	4	3										N V • • • • Z C	ADC
AND	A∧M → A (1)	29	2	2	2D	4	3	25	3	2							21	6	2	31	5	2	35	4	2	3D	4	3	39	4	3										N • • • • • Z •	AND
ASL	C ← 7 … 0 ← 0				0E	6	3	06	5	2	0A	2	1										16	6	2	1E	7	3													N • • • • • Z C	ASL
BCC	BRANCH ON C = 0 (2)																															90	2	2								• • • • • • • •	BCC
BCS	BRANCH ON C = 1 (2)																															B0	2	2								• • • • • • • •	BCS
BEQ	BRANCH ON Z = 1 (2)																															F0	2	2								• • • • • • • •	BEQ
BIT	A∧M				2C	4	3	24	3	2																																M7 M6 • • • • Z •	BIT
BMI	BRANCH ON N = 1 (2)																															30	2	2								• • • • • • • •	BMI
BNE	BRANCH ON Z = 0 (2)																															D0	2	2								• • • • • • • •	BNE
BPL	BRANCH ON N = 0 (2)																															10	2	2								• • • • • • • •	BPL
BRK	BREAK													00	7	1																									• • • 1 • 1 • •	BRK
BVC	BRANCH ON V = 0 (2)																															50	2	2								• • • • • • • •	BVC
BVS	BRANCH ON V = 1 (2)																															70	2	2								• • • • • • • •	BVS
CLC	0 → C													18	2	1																									• • • • • • • 0	CLC
CLD	0 → D													D8	2	1																									• • • • 0 • • •	CLD
CLI	0 → I													58	2	1																									• • • • • 0 • •	CLI
CLV	0 → V													B8	2	1																									• 0 • • • • • •	CLV
CMP	A − M	C9	2	2	CD	4	3	C5	3	2							C1	6	2	D1	5	2	D5	4	2	DD	4	3	D9	4	3										N • • • • • Z C	CMP
CPX	X − M	E0	2	2	EC	4	3	E4	3	2																																N • • • • • Z C	CPX
CPY	Y − M	C0	2	2	CC	4	3	C4	3	2																																N • • • • • Z C	CPY
DEC	M − 1 → M				CE	6	3	C6	5	2													D6	6	2	DE	7	3													N • • • • • Z •	DEC
DEX	X − 1 → X													CA	2	1																									N • • • • • Z •	DEX
DEY	Y − 1 → Y													88	2	1																									N • • • • • Z •	DEY
EOR	A ∨ M → A (1)	49	2	2	4D	4	3	45	3	2							41	6	2	51	5	2	55	4	2	5D	4	3	59	4	3										N • • • • • Z •	EOR
INC	M + 1 → M				EE	6	3	E6	5	2													F6	6	2	FE	7	3													N • • • • • Z •	INC
INX	X + 1 → X													E8	2	1																									N • • • • • Z •	INX
INY	Y + 1 → Y													C8	2	1																									N • • • • • Z •	INY
JMP	JUMP TO NEW LOC				4C	3	3																												6C	5	3				• • • • • • • •	JMP
JSR	JUMP SUB				20	6	3																																			• • • • • • • •	JSR
LDA	M → A (1)	A9	2	2	AD	4	3	A5	3	2							A1	6	2	B1	5	2	B5	4	2	BD	4	3	B9	4	3										N • • • • • Z •	LDA
LDX	M → X (1)	A2	2	2	AE	4	3	A6	3	2																			BE	4	3							B6	4	2	N • • • • • Z •	LDX
LDY	M → Y (1)	A0	2	2	AC	4	3	A4	3	2													B4	4	2	BC	4	3													N • • • • • Z •	LDY
LSR	0 → 7 … 0 → C				4E	6	3	46	5	2	4A	2	1										56	6	2	5E	7	3													0 • • • • • Z C	LSR
NOP	NO OPERATION													EA	2	1																									• • • • • • • •	NOP
ORA	A ∨ M → A	09	2	2	0D	4	3	05	3	2							01	6	2	11	5	2	15	4	2	1D	4	3	19	4	3										N • • • • • Z •	ORA
PHA	A → Ms S − 1 → S													48	3	1																									• • • • • • • •	PHA
PHP	P → Ms S − 1 → S													08	3	1																									• • • • • • • •	PHP
PLA	S + 1 → S Ms → A													68	4	1																									N • • • • • Z •	PLA
PLP	S + 1 → S Ms → P													28	4	1																									(RESTORED)	PLP
ROL	7 … 0 ← C				2E	6	3	26	5	2	2A	2	1										36	6	2	3E	7	3													N • • • • • Z C	ROL
ROR	C → 7 … 0				6E	6	3	66	5	2	6A	2	1										76	6	2	7E	7	3													N • • • • • Z C	ROR
RTI	RTRN INT													40	6	1																									(RESTORED)	RTI
RTS	RTRN SUB													60	6	1																									• • • • • • • •	RTS
SBC	A − M − C̄ → A (1)	E9	2	2	ED	4	3	E5	3	2							E1	6	2	F1	5	2	F5	4	2	FD	4	3	F9	4	3										N V • • • • Z (3)	SBC
SEC	1 → C													38	2	1																									• • • • • • • 1	SEC
SED	1 → D													F8	2	1																									• • • • 1 • • •	SED
SEI	1 → I													78	2	1																									• • • • • 1 • •	SEI
STA	A → M				8D	4	3	85	3	2							81	6	2	91	6	2	95	4	2	9D	5	3	99	5	3										• • • • • • • •	STA
STX	X → M				8E	4	3	86	3	2																													96	4	2	• • • • • • • •	STX
STY	Y → M				8C	4	3	84	3	2													94	4	2																	• • • • • • • •	STY
TAX	A → X													AA	2	1																									N • • • • • Z •	TAX
TAY	A → Y													A8	2	1																									N • • • • • Z •	TAY
TSX	S → X													BA	2	1																									N • • • • • Z •	TSX
TXA	X → A													8A	2	1																									N • • • • • Z •	TXA
TXS	X → S													9A	2	1																									• • • • • • • •	TXS
TYA	Y → A													98	2	1																									N • • • • • Z •	TYA

(1) ADD 1 to N IF PAGE BOUNDARY IS CROSSED
(2) ADD 1 TO N IF BRANCH OCCURS TO SAME PAGE
ADD 2 TO N IF BRANCH OCCURS TO DIFFERENT PAGE
(3) CARRY NOT = BORROW
(4) IF IN DECIMAL MODE Z FLAG IS INVALID
ACCUMULATOR MUST BE CHECKED FOR ZERO RESULT

X	INDEX X	+	ADD	M_7	MEMORY BIT 7
Y	INDEX Y	−	SUBTRACT	M_6	MEMORY BIT 6
A	ACCUMULATOR	∧	AND	n	NO. CYCLES
M	MEMORY PER EFFECTIVE ADDRESS	∨	OR	#	NO. BYTES
Ms	MEMORY PER STACK POINTER	∨	EXCLUSIVE OR		

APPENDIX C — SYSTEM SPECIFICATIONS

MAXIMUM RATINGS*

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}, V_{RR}	−0.3 to +7.0	Vdc
Input Voltage	V_{IN}	−0.3 to +7.0	Vdc
Operating Temperature Commercial Industrial	T_A	T_L to T_H 0 to +70 −40 to +85	°C
Storage Temperature	T_{STG}	−55 to +150	°C

***NOTE:** Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in other sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

(V_{CC} = 5.0V ±10% for R6500/1, V_{CC} = 5.0V ±5% for R6500/1A, V_{RR} = V_{CC}; V_{SS} = 0V; T_A = 0° to 70°C, unless otherwise specified)

Parameter	Symbol	Min	Typ[1]	Max	Unit	Test Conditions
RAM Standby Voltage (Retention Mode)	V_{RR}	3.5	—	V_{CC}	V	
RAM Standby Current (Retention Mode) Commercial Industrial	I_{RR}	 — —	 10 12	 — —	mA	
Input High Voltage All Except XTLI XTLI	V_{IH}	 +2.0 +4.0	 — —	 V_{CC} V_{CC}	V	
Input Low Voltage	V_{IL}	−0.3	—	+0.8	V	
Input Leakage Current $\overline{RES}$, $\overline{NMI}$	I_{IN}	—	±1.0	±2.5	μA	V_{IN} = 0 to 5.0V
Input Low Current	I_{IL}	—	−1.0	−1.6	mA	V_{IL} = 0.4V
Output High Voltage	V_{OH}	+2.4	—	—	V	I_{LOAD} = −100 μA V_{CC} = 4.75V
Output High Voltage (CMOS)	V_{CMOS}	V_{CC} − 30%	—	—	V	V_{CC} = 4.75V
Output Low Voltage	V_{OL}	—	—	+0.4	V	V_{CC} = 4.75V I_{LOAD} = 1.6 mA
I/O Port Pull-Up Resistance PA0–PA7, PB0–PB7, PC0–PC7, PD0–PD7, CNTR	R_L	3.0	6.0	11.5	Kohm	
Output High Current (Sourcing)	I_{OH}	−100	—	—	μA	V_{OUT} = 2.4V
Output Low Current (Sinking)	I_{OL}	1.6	—	—	mA	V_{OUT} = 0.4V
Input Capacitance XTLI, XTLO PA, PB, PC, PD, CNTR	C_{IN}	 — —	 — —	 50 10	pF	T_A = 25°C V_{IN} = 0V f = 1.0 MHz
Output Capacitance (Three-State Off)	C_{OUT}	—	—	10	pF	T_A = 25°C V_{IN} = 0V f = 1.0 MHz
Power Dissipation (Outputs High)	P_D	—	600	990	mW	V_{CC} = +5.5V

Notes:
1. Typical values measured at T_A = 25°C and V_{CC} = 5.0V.
2. Negative sign indicates outward current flow, positive indicates inward flow.

AC CHARACTERISTICS

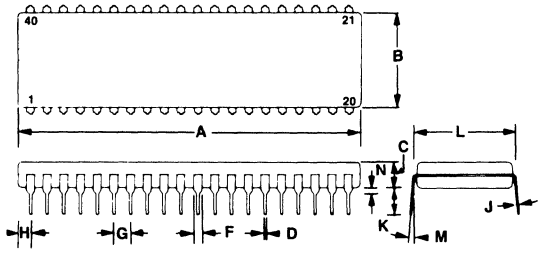
(V_{CC} = 5V ±10% for R6500/1, V_{CC} = 5V ±5% for R6500/1A)

Parameter	Symbol	1 MHz		2 MHz		Unit
		Min	Max	Min	Max	
XTLI Input Clock Cycle Time	T_{cyc}	0.500	5.0	0.250	5.0	µsec
Internal Write to Peripheral Data Valid (TTL)	T_{PDW}	1.0		0.5		µsec
Internal Write to Peripheral Data Valid (CMOS)	T_{CMOS}	2.0		1.0		µsec
Peripheral Data Setup Time	T_{PDSU}	400		200		nsec
Count and Edge Detect Pulse Width	T_{PW}	1.0		0.5		µsec

3

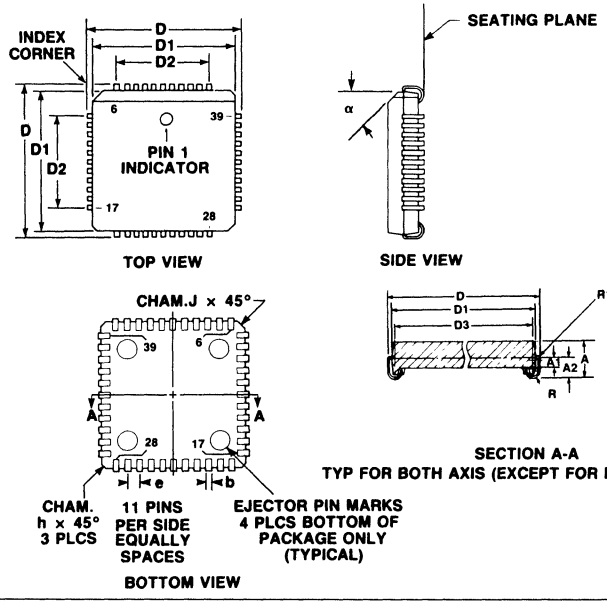
PACKAGE DIMENSIONS

40-PIN PLASTIC DIP



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	51 82	52 32	2 040	2.060
B	13 46	13.97	0 530	0.550
C	3 56	5.08	0 140	0 200
D	0 38	0.53	0 015	0.021
F	1.02	1.52	0.040	0.060
G	2 54 BSC		0.100 BSC	
H	1 65	2.16	0.065	0 085
J	0 20	0.30	0 008	0 012
K	3.30	4.32	0.130	0.170
L	15.24 BSC		0 600 BSC	
M	7°	10°	7°	10°
N	0 51	1.02	0.020	0.040

44-PIN PLASTIC LEADED CHIP CARRIER (PLCC)



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.14	4.39	0 163	0.173
A1	1.37	1 47	0.054	0.058
A2	2.31	2.46	0.091	0.097
b	0.457 TYP		0018 TYP	
D	17.45	17.60	0.687	0.693
D1	16.46	16.56	0.648	0.652
D2	12.62	12.78	0.497	0.503
D3	15.75 REF		0.620 REF	
e	1.27 BSC		0.050 BSC	
h	1.15 TYP		0.045 TYP	
J	0.25 TYP		0.010 TYP	
α	45° TYP		45° TYP	
R	0.89 TYP		0.035 TYP	
R1	0.25 TYP		0.010 TYP	

Rockwell

R6500/1E
Microprocessor Emulator Device

INTRODUCTION

The R6500/1E device provides all the features of the R6500/1 Microcomputer in a ROMless form suitable for use as an advanced microprocessor complete with 16-bit counter and 32 I/O lines, and an address and data bus for 4K of external memory.

To aid in designing R6500/1 microcomputer systems, it may also be used as an emulator device. Device architecture is basically the same as the R6500/1 except that the address, data, and associated control lines are routed off the chip for connection to an external memory.

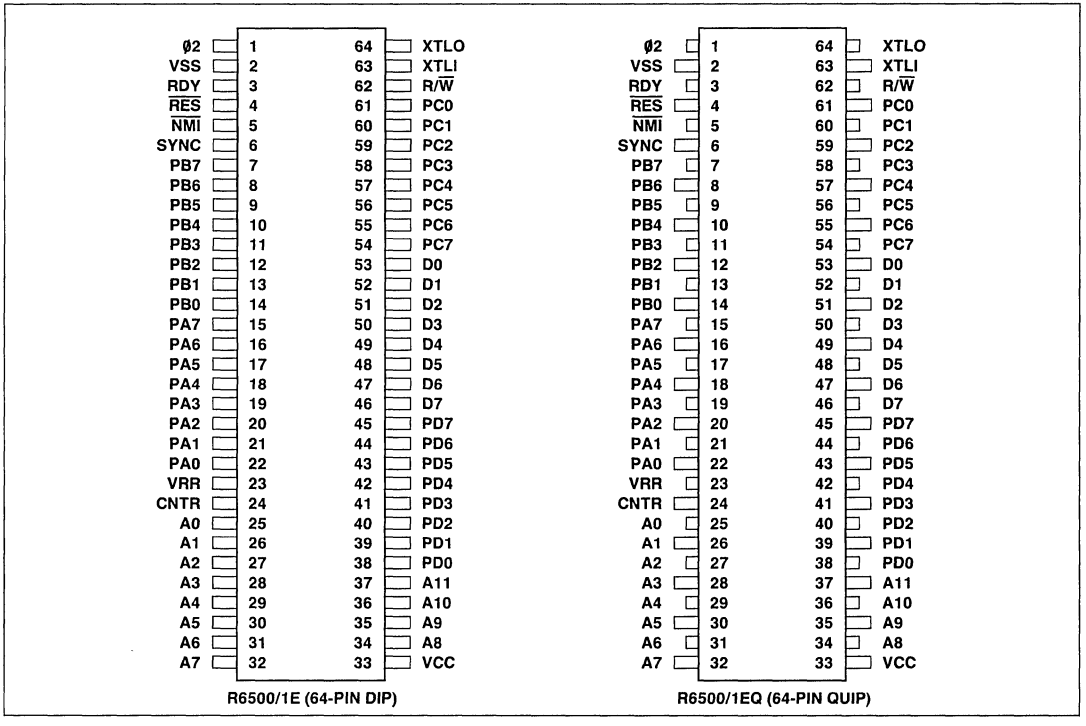
The functions and operation of the R6500/1E device are identical to the R6500/1 except for minor differences noted in this document. The R6500/1 Product Description (Order No. 212) contains a description of R6500/1 functions and interface signals.

The R6500/1E device is available in both 64-pin ceramic DIP (R6500/1EC) and 64-pin plastic QUIP (R6500/1EQ).

ORDERING INFORMATION

Part Number	Package Type	Frequency Option	Temperature Range
R6500/1EC	Ceramic	1 MHz	0°C to 70°C
R6500/1EAC	Ceramic	2 MHz	0°C to 70°C
R6500/1EQ	Plastic	1 MHz	0°C to 70°C
R6500/1EAQ	Plastic	2 MHz	0°C to 70°C

3



R6500/1E Pin Assignments

INTERFACE SIGNALS

All R6500/1 interface signals are available in the R6500/1E microcomputer plus the additional address (12), data (8), and control (4) lines required to extend the address bus and the data bus external to the device. The R6500/1E emulator unique interface signals are shown in Figure 1 and are described in Table 1. While the pin assignments are different in order to accommodate 64-pin DIP and QUIP packages, the interface characteristics of signals common to the R6500/1 are identical.

SYSTEM ARCHITECTURE

The architecture of the R6500/1E is identical to the R6500/1 with the following differences:

EXTERNAL ADDRESSING

ROM addressing is routed externally in the R6500/1E. The address range for internal ROM in the R6500/1 ($800-$FF9) is available externally for connection to ROM or RAM devices(s).

An additional 1024 bytes ($400-$7FF) are decoded for external memory access. Note that this address range can be used for debugging with the R6500/1E but cannot be used when the object code is transferred to masked ROM in an R6500/1 (which is restricted to $800-$FF9).

A memory map of the R6500/1E is shown in Figure 2.

INTERNAL I/O PORT PULL-UPS

The R6500/1E has the internal I/O and CNTR port pull-up resistors only. The option to delete the pull-up resistors is not available for the R6500/1E.

EARLIER I/O PORT INITIALIZATION

Ports A, B, C, D and the CNTR line in the R6500/1E are initialized to the logic high state two Ø2 clock cycles earlier than in the R6500/1. It is still required, however, that the $\overline{RES}$ line be held low for at least eight Ø2 clock cycles after VCC reaches operating range (Figure 3).

WRITE-ONLY MONITORING

The R6500/1E allows the user to monitor write operations to the internal RAM and I/O by routing those operations externally as well as internally. Read operations are not routed externally.

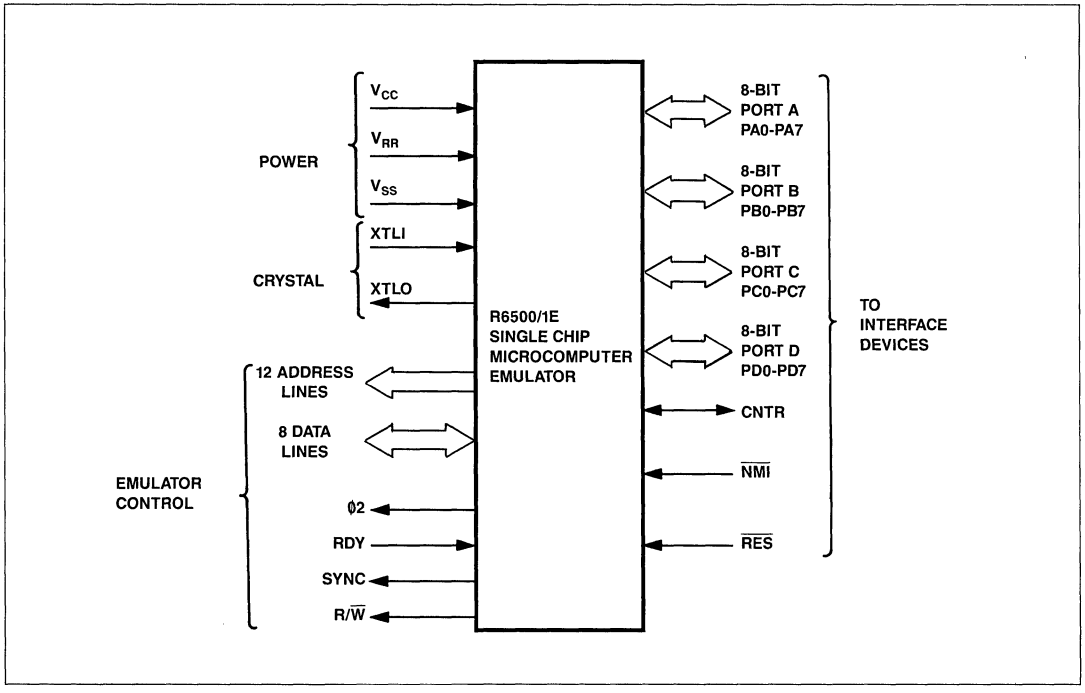


Figure 1. R6500/1E Emulator Interface Diagram

Table 1. R6500/1E Emulator Unique Signals Description

Signal Name	Pin No.	Description
R/$\overline{W}$	62	**Read/Write.** Read/Write allows the CPU to control the direction of data transfer between the R6500/1E Emulator CPU and external memory. This line is high when reading data from memory and is low when writing data to memory.
RDY	3	**Ready.** The Ready input delays execution of any cycle during which the RDY line is low. This allows the user to halt or single step the CPU on all cycles except write cycles. A negative transition to the low state during the ϕ2 clock low pulse will halt the CPU with the address lines containing the current address being fetched. If RDY is low during a write cycle, it is ignored until the following read operation. This condition will remain through a subsequent ϕ2 clock pulse in which the RDY line is low. This feature allows the CPU to interface with memories having slow access times, such as EPROMS used with the R6500/1E during prototype system development.
SYNC	6	**Sync.** The Sync signal is provided to identify cycles in which the CPU is performing OP CODE fetch. SYNC goes high during the ϕ2 clock low pulse of an OP CODE fetch and stays high for the remainder of that cycle. If the RDY line is pulled low during the ϕ2 clock low pulse in which SYNC went high, the CPU will halt in its current state and will remain in that state until the RDY line goes high. Using this technique, the SYNC signal can be used to control RDY to cause single instruction execution.
ϕ2	1	**Phase 2 (ϕ2) clock:** Data transfer takes place only during ϕ2 clock pulse high.
A0-A11	25-37	**Address Bus Lines.** The address bus buffers on the R6500/1E are push/pull type drivers capable of driging at least 130 pF and one standard TTL load. The address bus always contains known data. The addressing tgechnique involves putting an address on the address bus which is known to be either in program sequence, on the same page in program memory, or at a known point in memory. The I/O address commands are also placed on these lines.
D0-D7	53-46	**Data Bus Lines.** All transfers of instructions and data between the CPU and memory, I/O, and other interfacing circuitry take place on the bidirectional data bus lines. The buffers driving the data bus lines have full three-state capability. Each data bus pin is connected to an input and output buffer, with the output buffer remaining in the floating condition.

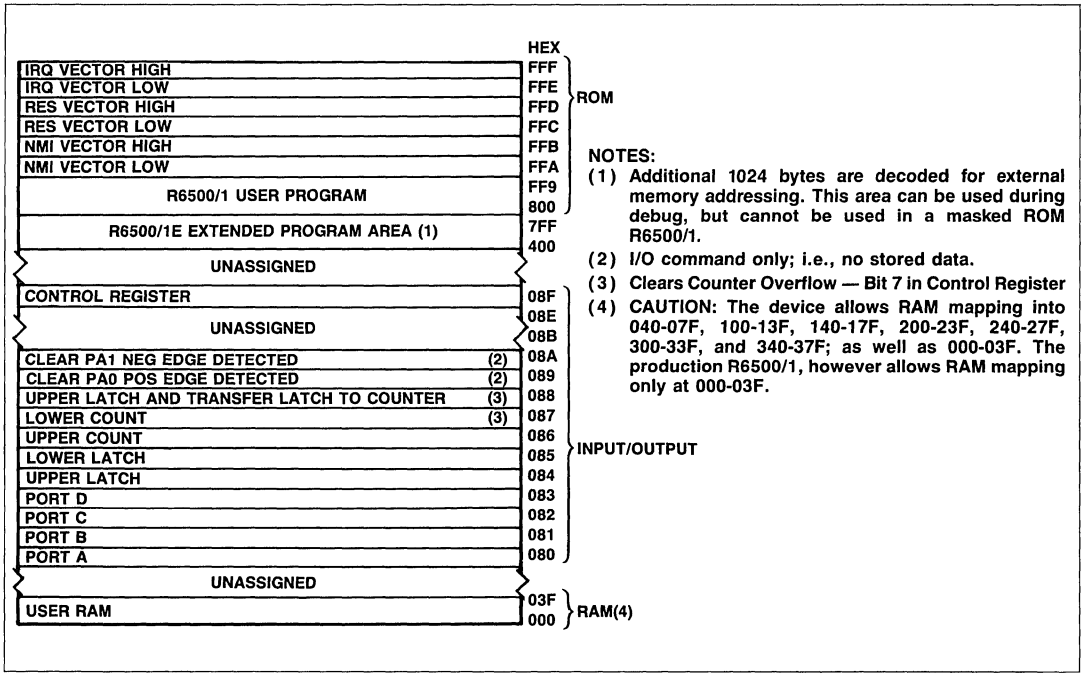


Figure 2. R6500/1E Memory Map

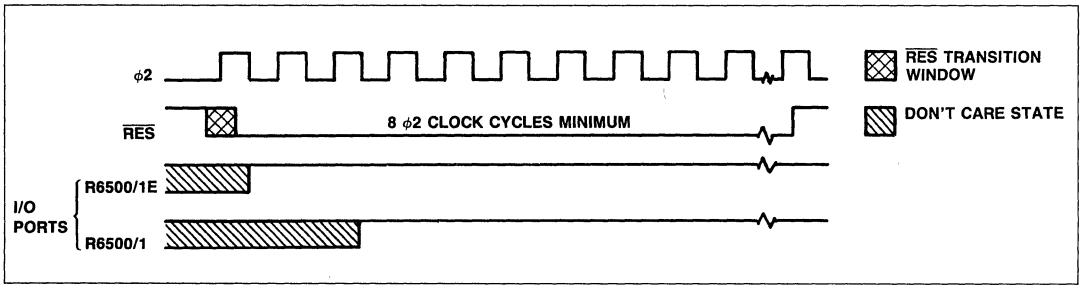


Figure 3. R6500/1E I/O Port Initialization

TYPICAL PROGRAM MEMORY INTERCONNECTIONS

Two typical connections between the R6500/1E and program memory (in this case, type 2716 and 2732 PROMS) are illustrated. Figure 4 shows a connection to a 2K 2716 PROM. Since the R6500/1 has a 2K ROM capacity, the contents of the PROM could be masked directly into the production R6500/1 ROM.

Figure 5 shows a connection to a 4K 2732 PROM. Only 3K bytes ($400-$FFF) are enabled. The upper 2K bytes correspond the production ROM space ($800-$FFF) in the R6500/1. The extra 1K ($400-$7FF) allows expanded or additional programs to be used during R6500/1 firmware development. The production program, however, must be reduced to 2K maximum ($800-$FFF) before masking into R6500/1 ROM.

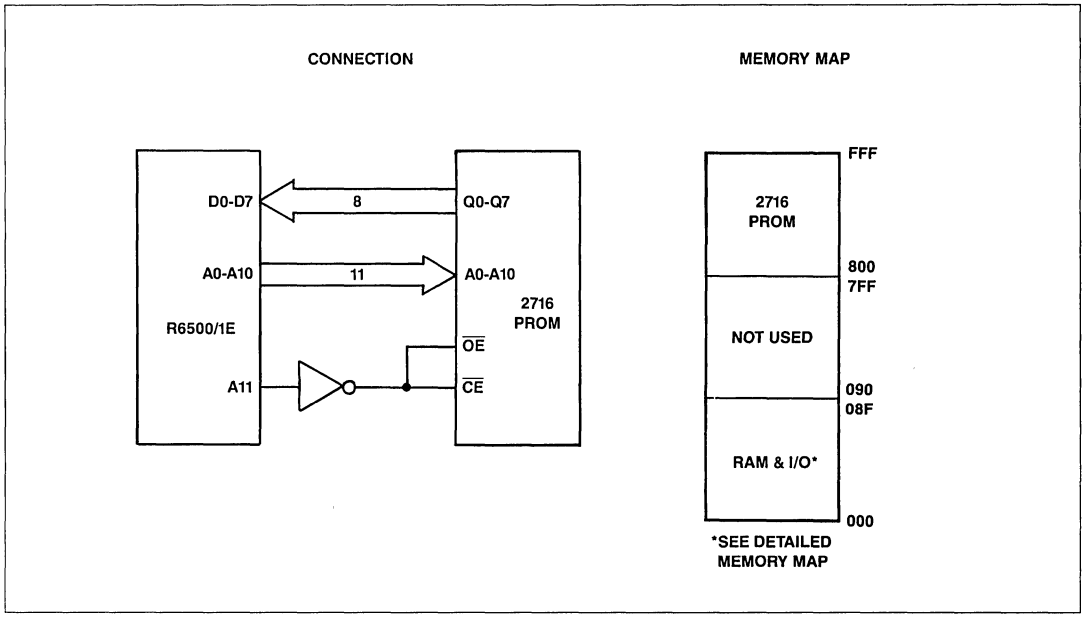


Figure 4. R6500/1E Connected to One 2716 PROM (2K Bytes)

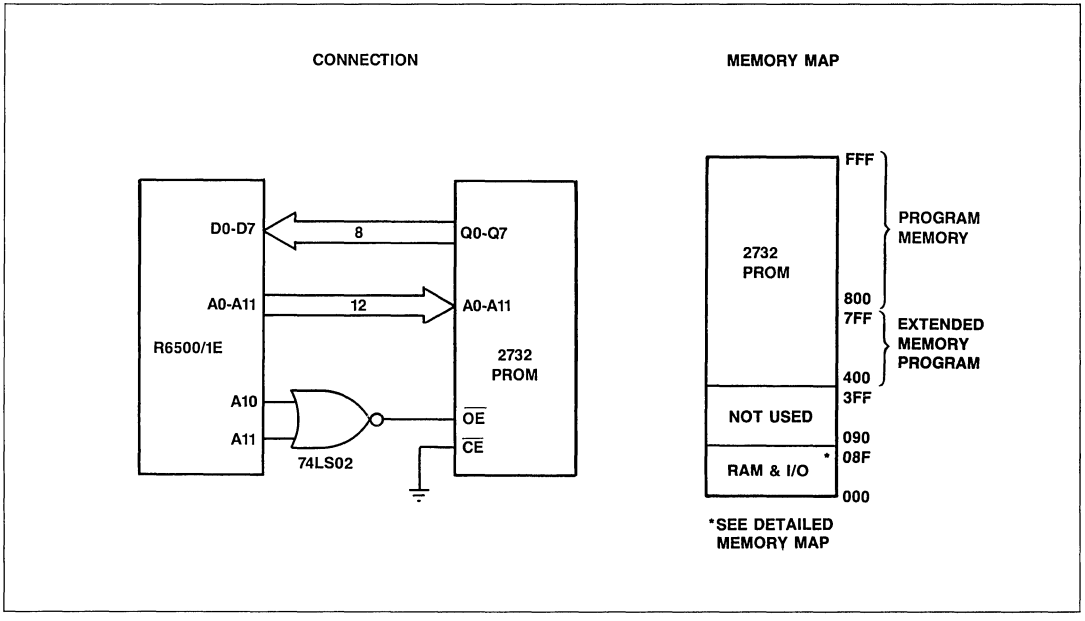


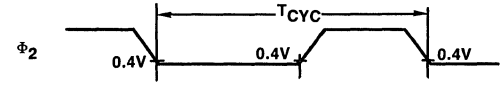
Figure 5. R6500/1E Connected to One 2732 PROM (3K Bytes)

DEVICE TIMING

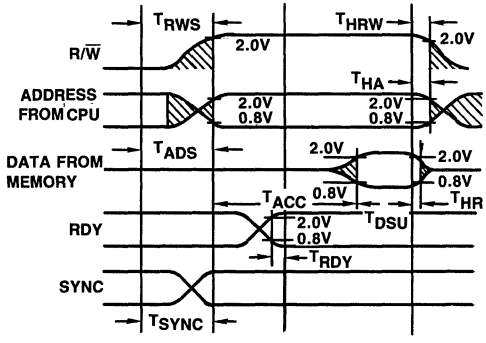
Signal	Symbol	1 MHz		2 MHz		Unit
		Min.	Max.	Min.	Max.	
R/$\overline{W}$ setup time from CPU	T_{RWS}		300		200	ns
Address setup time from CPU	T_{ADS}		300		200	ns
Memory read access time	T_{ACC}		525		225	ns
Data stabilization time	T_{DSU}	150		75		ns
Data hold time — Read	T_{HR}	10		10		ns
Data hold time — Write	T_{HW}	30		30		ns
Data delay time from CPU	T_{MDS}		200		150	ns
RDY setup time	T_{RDY}	100		50		ns
SYNC delay time from CPU	T_{SYNC}		350		175	ns
Address hold time	T_{HA}	30		30		ns
R/$\overline{W}$ hold time	T_{HRW}	30		30		ns
Cycle Time	T_{CYC}	1.0	10.0	0.5	10.0	μs

TIMING DIAGRAMS

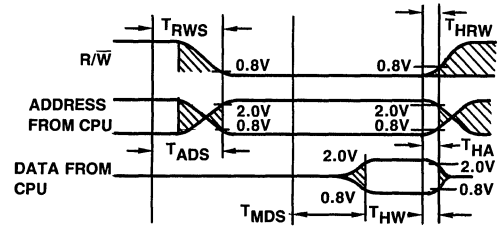
PHASE 2 (Φ2) TIMING REFERENCE



TIMING FOR READING FROM MEMORY



TIMING FOR WRITING TO MEMORY



MAXIMUM RATINGS*

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to +7.0	Vdc
Input Voltage	V_{IN}	−0.3 to +7.0	Vdc
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{STG}	−55 to +150	°C

***NOTE:** Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device atr these or any other conditions above those indicated in other sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

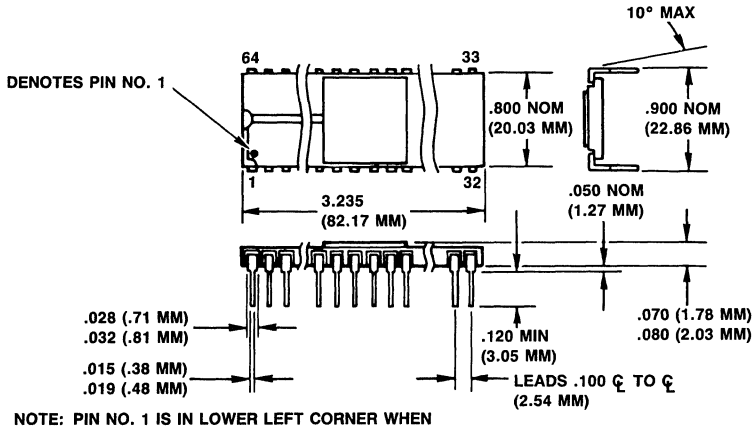
(V_{CC} = 5.0 ±5%, V_{SS} = 0, T_A = 0°C to 70°C unless otherwise specified)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Conditions
RAM Standby Voltage (Retention Mode)	V_{RR}	3.5	—	V_{CC}	V	
RAM Standby Current (Retention Mode)	I_{RR}	—	10	—	mA	
Input High Voltage	V_{IH}	+2.4	—	—	Vdc	
Input Low Voltage	V_{IL}	—	—	+0.8	Vdc	
Three-State (Off State) Input Current D0-D7	I_{TSI}	—	—	±10	μA	V_{IN} = 0.4 to 2.4V V_{CC} = 5.25V
Output High Voltage D0-D7, SYNC, A0-A11, R/$\overline{W}$, ϕ2	V_{OH}	+2.4	—	—	Vdc	I_{LOAD} = −100 μA V_{CC} = 4.75V
Output Low Voltage D0-D7, SYNC, A0-A11, R/$\overline{W}$, ϕ2	V_{OL}	—	—	+0.6	Vdc	I_{LOAD} = 1.6 μA V_{CC} = 4.75V
Power Dissipation (V_{CC} = 5.5V)	P_D	—	750	1200	μW	V_{CC} = 5.5V
Input Capacitance RDY, PA, PB, PC, PD, CNTR D0-D7 XTLI, XTLO	C_{IN}	 — — —	 — — —	 10 15 50	pF	 T_A = 25°C V_{IN} = 0 f = 1 MHz
Output Capacitance A0-A11, R/$\overline{W}$, SYNC ϕ2	 C_{OUT} $C_{ϕ2}$	 — —	 —	 12 80	 pF	
I/O Port Pull-up Resistance	R_L	3.0	6.0	11.5	kohm	

Notes:
1. Typical values measured at T_A = 25°C and V_{CC} = 5.0V.
2. Negative sign indicates outward current flow, positive indicates inward flow.

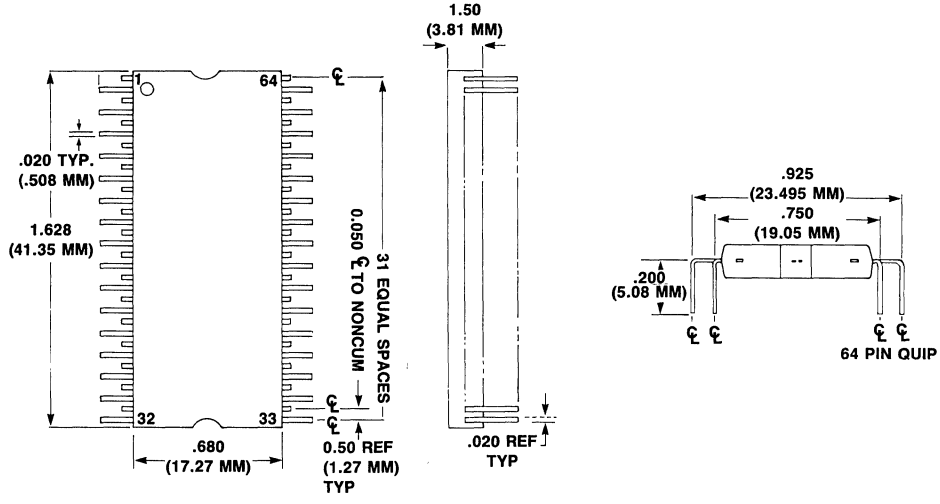
PACKAGE DIMENSIONS

R6500/1EC 64-PIN DIP CERAMIC



NOTE: PIN NO. 1 IS IN LOWER LEFT CORNER WHEN SYMBOLIZATION IS IN NORMAL ORIENTATION

R6500/1EQ 64-PIN QUIP PLASTIC



Rockwell

R6500/1EB and R6500/1EAB Backpack Emulator

INTRODUCTION

The Rockwell R6500/1EB and R6500/1EAB Backpack Emulator is the PROM prototyping version of the 8-bit, masked-ROM R6500/1 one-chip microcomputer. Like the R6500/1, the backpack device is totally upward/downward compatible with all members of the R6500/1 family. It is designed to accept standard 5-volt, 24-pin EPROMs or ROMs directly, in a socket on top of the Emulator. This packaging concept allows a standard EPROM to be easily removed, reprogrammed, then reinserted as often as desired.

The backpack devices have the same pinouts as the masked-ROM R6500/1 microcomputer. These 40 pins are functionally and operationally identical to the pins on the R6500/1, with some minor differences (described herein). The R6500/1 Microcomputer Product Description (Order No. 212) includes a description of the interface signals and their functions. Whereas the masked-ROM R6500/1 provides 2K bytes of read-only memory, the R6500/1EB will address 3K bytes of external program memory. This extra memory accommodates program patches, test programs or optional programs during breadboard and prototype development states.

FEATURES

- PROM version of the R6500/1
- Completely pin compatible with R6500/1 single-chip microcomputers
- Profile approaches 40-pin DIP of R6500/1
- Accepts 5-volt, 24-pin industry-standard EPROMs —4K memories—2732, 2732A (3K bytes addressable)
- Use as prototyping tool or for low volume production
- 3K bytes of memory capacity (4K memories)
- 64 × 8 static RAM
- Separate power pin for RAM
- Software compatibility with the R6500 family
- 32 bi-directional TTL compatible I/O lines (4 ports)
- 1 bi-directional TTL compatible counter I/O line
- 16-bit programmable counter/latch with four modes (interval timer, pulse generator, event counter, pulse width measurement)
- 5 interrupts (reset, non-maskable, two external edge sensitive, counter)
- Crystal or external time base
- Single +5V power supply

3

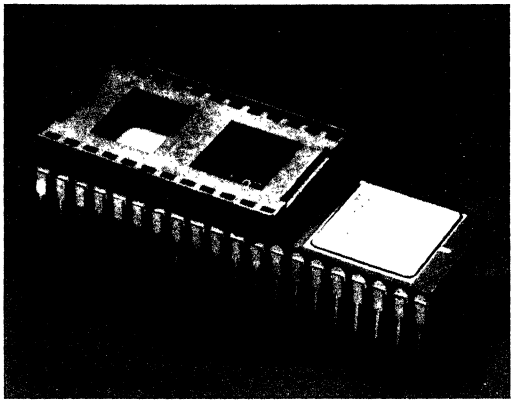
ORDERING INFORMATION

BACKPACK EMULATOR

Part Number	Memory Capacity	Compatible Memories	Temperature Range and Speed
R6500/1EB3	3K x 8	2732	0°C to 70°C 1 MHz
R6500/1EAB3	3K x 8	2732A (250 ns)	0°C to 70°C 2 MHz

SUPPORT PRODUCTS

Part Number	Description
RDC-3101	Low Cost Emulator (LCE)
RDC-3030	PROM Programmer Module
RDC-369	1- or 2-MHz R6500/1 Personality Module



R6500/1EB-R6500/1EAB Backpack Emulator

CONFIGURATION

The external memory must always occupy the upper 2K of available memory (addresses 800 through FFF) for implementation of interrupt vectors. See Memory Map. The Backpack Emulator provides a read block to the external memory where internal RAM or I/O are located in the same addresses as that occupied by external memory.

EXTERNAL FREQUENCY REFERENCE

The external frequency reference may be a crystal or a clock. The R6500/1EB and R6500/1EAB divide the input clock by two regardless of the source.

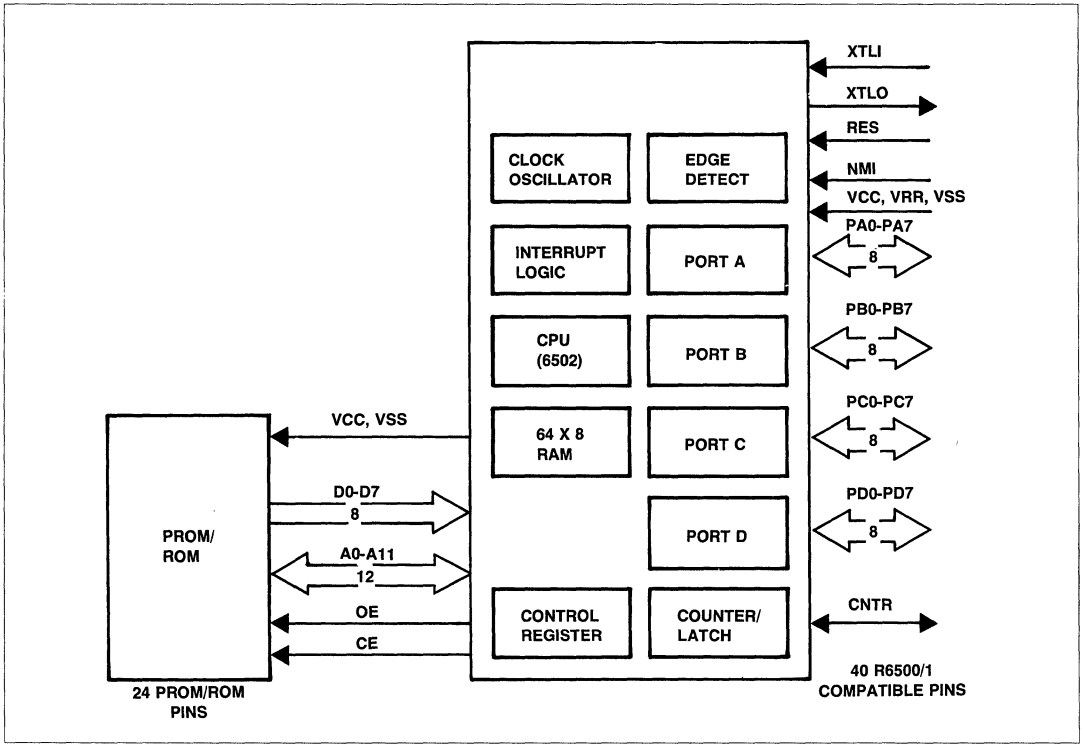
I/O PORT PULLUPS

The emulator devices have internal I/O port pullup resistors.

PRODUCT SUPPORT

The Backpack Emulator is just one of the products that Rockwell offers to facilitate system and program development for the R6500/1.

The Low Cost Emulator (LCE) with R6500/1 Personality Module supports both hardware and software development. Complete in-circuit user emulation with the R6500/1 Personality Module allows total system test and evaluation. With the optional PROM Programmer, the LCE can also be used to program EPROMs for the development activity. When PROM programs have been finalized, the PROM device can be sent to Rockwell for masking into the 2K ROM of the R6500/1.



R6500/1EB Interface Diagram

DETAILED MEMORY MAP

			HEX
PROM	IRQ VECTOR HIGH		FFF
	IRQ VECTOR LOW		FFE
	RES VECTOR HIGH		FFD
	RES VECTOR LOW		FFC
	NMI VECTOR HIGH		FFB
	NMI VECTOR LOW		FFA
	R6500/1 USER PROGRAM		FF9 400
PROM	R6500/1EB EXTENDED PROGRAM AREA (1)		3FF 400
NOT USED	UNASSIGNED		
I/O	CONTROL REGISTER		08F
	UNASSIGNED		08E 08B
	CLEAR PA1 NEG EDGE DETECTED	(2)	08A
	CLEAR PA0 POS EDGE DETECTED	(2)	089
	UPPER LATCH AND TRANSFER LATCH TO COUNTER	(3)	088
	LOWER COUNT	(3)	087
	UPPER COUNT		086
	LOWER LATCH		085
	UPPER LATCH		084
	PORT D		083
	PORT C		082
	PORT B		081
	PORT A		080
NOT USED	UNASSIGNED		03F
RAM	USER RAM		000

NOTES

(1) Additional 1024 bytes are decoded for external memory addressing by the Backpack Emulator Device. This area can be used during debug, but cannot be used in a masked ROM R6500/1.

(2) I/O command only; i.e., no stored data.

(3) Clears Counter Overflow—Bit 7 in Control Register

(4) CAUTION: The device allows RAM mapping into 040-07F, 100-13F, 140-17F, 200-23F, 240-27F, 300-33F, and 340-37F; as well as 000-03F. The production R6500/1, however allows RAM mapping only at 000-03F.

RAM MAPPING

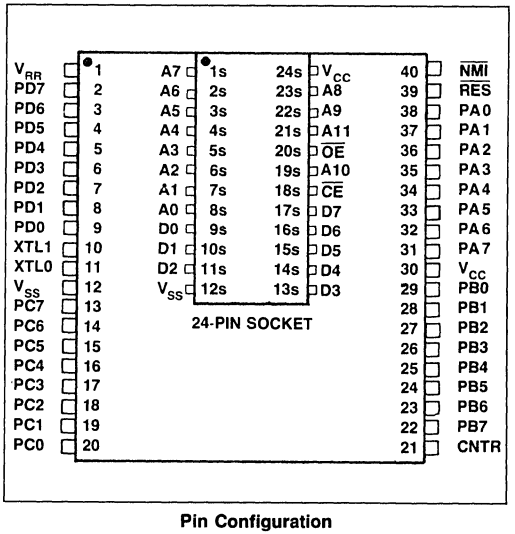
The Backpack Emulator allows RAM mapping into 040-07F, 100-13F, 140-17F, 200-23F, 240-27F, 300-33F and 340-37F, as well as 000-03F. The production R6500/1, however, allows RAM mapping only at 000-03F. This means that a write to location 40, for example, will write to location 0 in the Backpack Emulator, and to invalid RAM in the R6500/1 production part.

I/O PORT INITIALIZATION

Ports A, B, C, and D and the CNTR line in the Backpack Emulator are initialized to the logic high state two Ø2 clock cycles earlier than in the R6500/1. The $\overline{RES}$ line to the device must, however, still be held low for at least eight Ø2 clock cycles after V_{CC} reaches operating range. See timing diagram.

BACKPACK MEMORY SIGNAL DESCRIPTION

Signal Name	Pin No.	Description
D0-D7	9S-11S, 13S-17S	Data Bus Lines. All instruction and data transfers take place on the data bus lines. The buffers driving the data bus lines have full three-state capability. Each data bus pin is connected to an input and an output buffer, with the output buffer remaining in the floating condition.
A0-A9	1S-8S, 23S, 24S	Address Bus Lines. The address bus lines are buffered by push/pull type drivers that can drive one standard TTL load.
A10	19S	Address Bus Line 10. This address line has the same characteristics and functions as Lines A0-A9.
$\overline{CE}$	18S	$\overline{CE}$ is active when the address is 400-FFF. This line can drive one TTL load.
$\overline{OE}$	20S	Memory Enable Line. This signal provides the output enable for the memory to place information on the data bus lines. This signal is driven by the R/$\overline{W}$ signal from the CPU and then inverted by a standard TTL inverter, to form $\overline{OE}$.
V_{CC}	24S	Main Power Supply $5V. This pin is tied directly to pin 30 (V_{CC}).
A11	21S	Address Bus Line II. This pin is tied to A11. During backup power, power is supplied only to the RAM memory, and not to the PROMs.
V_{SS}	12S	Signal and Power Ground (zero volts). This pin is tied directly to pin 12 (V_{SS}).

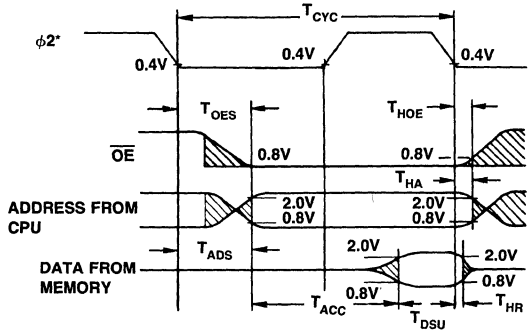


Pin Configuration

READ TIMING CHARACTERISTICS

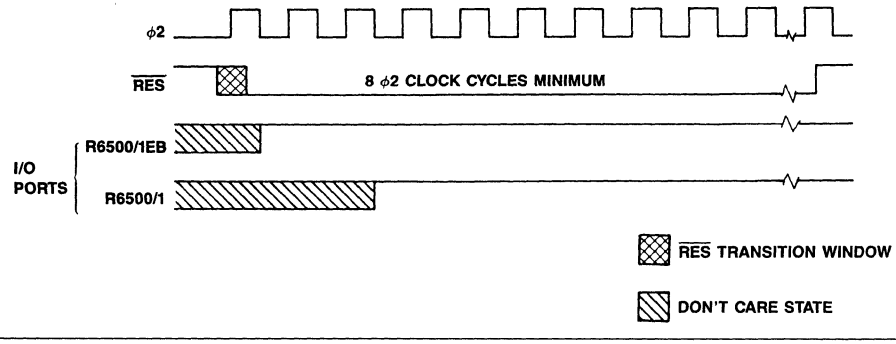
Signal	Symbol	1 MHz		2 MHz		Unit
		Min.	Max.	Min.	Max.	
$\overline{OE}$ setup time from CPU	T_{OES}	—	300	—	150	ns
Address setup time from CPU	T_{ADS}	—	300	—	150	ns
Memory read access time	T_{ACC}	—	525	—	250	ns
Data stabilization time	T_{DSU}	150	—	100	—	ns
Data hold time—Read	T_{HR}	10	—	10	—	ns
Address hold time	T_{HA}	30	—	30	—	ns
$\overline{OE}$ hold time	T_{HOE}	30	—	30	—	ns
Cycle Time	T_{CYC}	1.0	10.0	0.5	10.0	μs

READ TIMING WAVEFORMS



*ϕ2 IS SHOWN FOR REFERENCE ONLY AND IS NOT AVAILABLE EXTERNAL TO THE DEVICE.

I/O PORT INITIALIZATION TIMING



MAXIMUM RATINGS*

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to +7.0	Vdc
Input Voltage	V_{IN}	−0.3 to +7.0	Vdc
Operating Temperature Commercial	T_A	T_L to T_H 0 to +70	°C
Storage Temperature	T_{STG}	−55 to +150	°C

***NOTE:** Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in other sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

3

DC CHARACTERISTICS

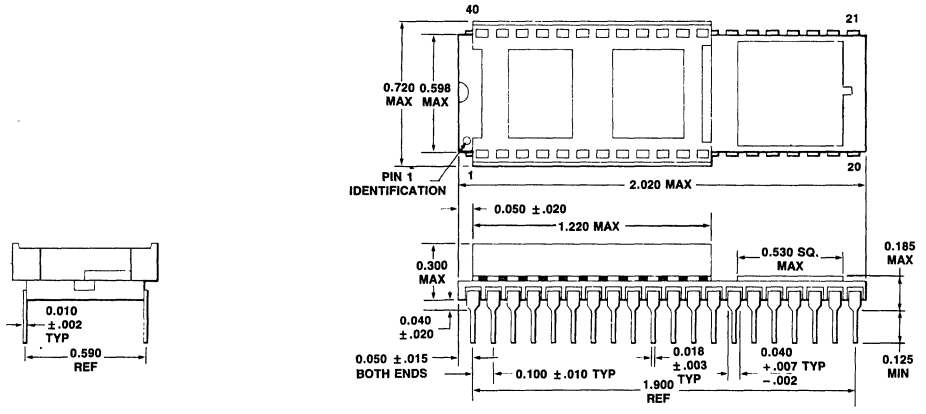
(V_{CC} = 5.0V ±5%, V_{SS} = 0V; T_A = 0° to 70°, unless otherwise specified)

Parameter	Symbol	Min	Typ[1]	Max	Unit	Test Conditions
Input High Voltage D0–D7	V_{IH}	+2.4	—	—	V	
Input Low Voltage D0–D7	V_{IL}	—	—	+0.8	V	
Input Leakage Current (Three-State Off) D0–D7	I_{IN}	—	—	±10.0	μA	V_{IN} = 0.4 to 2.4V V_{CC} = 5.25V
Output High Voltage (Except XTLO) D0–D7, A0–A11, $\overline{OE}$	V_{OH}	+2.4	—	—	V	I_{LOAD} = −100 μA V_{SS} = 4.75V
Output Low Voltage D0–D7, A0–A11, $\overline{OE}$	V_{OL}	—	—	+0.6	V	I_{LOAD} = 1.6 mA V_{SS} = 4.75V
I/O Port Pull-Up Resistance	R_L	3.0	6.0	11.5	Kohm	
Input Capacitance D0–D7	C_{IN}	—	—	15	pF	T_A = 25°C V_{IN} = 0V f = 1.0 MHz
Output Capacitance (Three-State Off) A0–A11	C_{OUT}	—	—	12	pF	T_A = 25°C V_{IN} = 0V f = 1.0 MHz
Power Dissipation (Less EPROM)	P_D	—	800	1300	mW	T_A = 0°C

Notes:
1. Typical values measured at T_A = 25°C and V_{CC} = 5.0V.
2. Negative sign indicates outward current flow, positive indicates inward flow.

PACKAGE DIMENSIONS

40-PIN BACKPACK



Rockwell

R6500/11, R6500/12 and R6500/15 One-Chip Microcomputers

3

SECTION 1 INTRODUCTION

1.1 FEATURES

- Enhanced 6502 CPU
  - —Four new bit manipulation instructions:
    - Set Memory Bit (SMB)
    - Reset Memory Bit (RMB)
    - Branch on Bit Set (BBS)
    - Branch on Bit Reset (BBR)
  - —Decimal and binary arithmetic modes
  - —13 addressing modes
  - —True indexing
- 3K-byte mask-programmable ROM (R6500/11, R6500/12)
- 4K-byte mask-programmable ROM (R6500/15)
- 192-byte static RAM
- 32 TTL-compatible I/O lines (R6500/11, R6500/15)
- 56 TTL-compatible I/O lines (R6500/12)
- One 8-bit port may be tri-stated under software control
- One 8-bit port with programmable latched input
- Two 16-bit programmable counter/timers, with latches
  - —Pulse width measurement
  - —Asymmetrical pulse generation
  - —Pulse generation
  - —Interval timer
  - —Event counter
  - —Retriggerable interval timer
- Serial port
  - —Full-duplex asynchronous operation mode
  - —Selectable 5- to 8-bit characters
  - —Wake-up feature
  - —Synchronous shift register mode
  - —Standard programmable bit rates, programmable up to 62.5K bits/sec @ 1 MHz
- Ten interrupts
  - —Four edge-sensitive lines; two positive, two negative
  - —Reset
  - —Non-maskable
  - —Two counter underflows
  - —Serial data received
  - —Serial data transmitted
- Bus expandable to 16K bytes of external memory
- Flexible clock circuitry
  - —2-MHz or 1-MHz internal operation
  - — Internal clock with external 2 MHz to 4 MHz series resonant XTAL at two or four times internal frequency
  - — External clock input divided by one, two or four
- 1 μs minimum instruction execution time @ 2 MHz
- NMOS-3 silicon gate, depletion load technology
- Single +5V power supply
- 12 mW stand-by power for 32 bytes of the 192-byte RAM
- 40-pin DIP (R6500/11 and R6500/15)
- 44-pin PLCC (R6500/11 and R6500/15)
- 64-pin QUIP (R6500/12)

1.2 SUMMARY

These Rockwell microcomputers are complete, high-performance 8-bit NMOS-3 microcomputers on a single chip, and are compatible with all members of the R6500 family.

The R6500/11 consists of an enhanced 6502 CPU, an internal clock oscillator, 3072 bytes of Read-Only Memory, 192 bytess of Random Access Memory (RAM) and versatile interface circuitry (Figure 1-1). The interface circuitry includes two 16-bit programmable timer/counters, 32 bidirectional input/output lines (including four edge-sensitive lines and input latching on one 8-bit port), a full-duplex serial I/O channel, ten interrupts and bus expandability.

The R6500/15 is identical to the R6500/11 except it has 4K of ROM.

The innovative architecture and the demonstrated high performance of the R6502 CPU, as well as instruction simplicity, results in system cost-effectiveness and a wide range of computational power. These features make either device a leading candidate for microcomputer applications.

The R6500/12 consists of all the features of the R6500/11 plus three additional I/O ports. It is packaged in a 64 pin QUIP.

To allow prototype circuit development, Rockwell offers a PROM-compatible 64-pin extended microprocessor device. This device, the R6511Q, provides all R6500/11 or R6500/15 interface lines, plus the address bus, data bus and control lines to interface with external memory. With the addition of external circuits it can also be used to emulate the R6500/12 (contact Rockwell sales offices listed on the back page for details).

A backpack emulator, the R65/11EB, is available for developing R6500/11 applications. No backpack part is available for the R6500/12.

The R6511Q may also be used as a CPU-RAM-I/O counter device in multichip systems.

Rockwell supports development of R6500/* single chip microcomputer applications with the Rockwell Design Center Low Cost Emulator (LCE) and R6500/* Personality Set. Program assembly can be performed on any user-provided computer using an assembler generating R6500/* machine code. The machine code can then be downloaded via an RS-232-C serial channel to the LCE for program debugging and in-circuit emulation. Complete in-circuit emulation with the R6500/* Personality Set allows total system test and evaluation. Refer to the RDC-3101/2 LCE and RDC-3XX R6500/* Personality Set data sheets, Order Nos. RDC17 and RDC06, respectively, for additional information.

This product description is for the reader familiar with the R6502 CPU hardware and programming capabilities. A detailed description of the R6502 CPU hardware is included in the R6500 Microcomputer System Hardware Manual (Order Number 201). A description of the instruction capabilities of the R6502 CPU is contained in the R6500 Microcomputer System Programming Manual (Order Number 202).

1.3 CUSTOMER OPTIONS

The R6500/11 microcomputer is available with the following customer specified mask options:

- Option 1 Crystal oscillator
- Option 2 Clock divide-by-2 or divide-by-4
- Option 3 Clock MASTER Mode or SLAVE Mode
- Option 4 Port A with or without internal pull-up resistors
- Option 5 Port B with or without internal pull-up resistors
- Option 6 Port C with or without internal pull-up resistors

All options should be specified on an R6500/11, /12 or /15 order form.

The R6500/12 is available with all of the above options plus:

- Option 7 Port F with or without internal pull-up resistors
- Option 8 Port G with or without internal pull-up resistors

Refer to the R6500/* ROM Code Order Forms (Order Number 2134) for detail option ordering information.

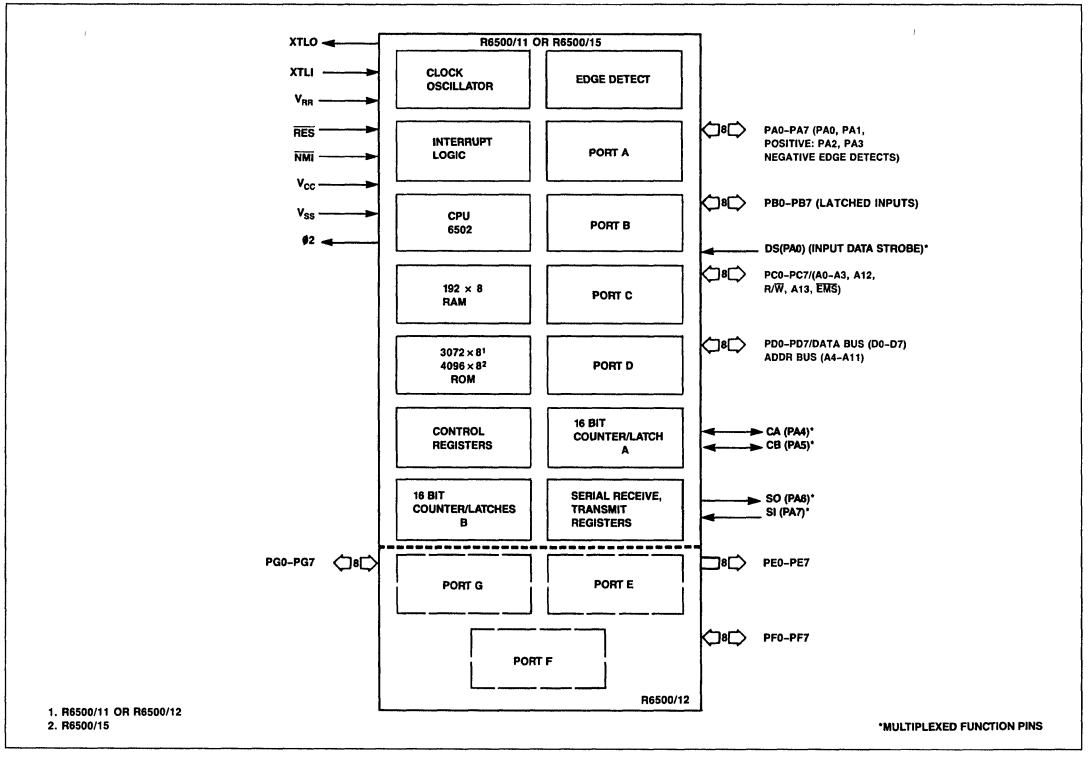


Figure 1-1. R6500/11, R6500/12 and R6500/15 Interface Signals

SECTION 2
INTERFACE REQUIREMENTS

This section describes the interface requirements for the single chip microcomputer devices. Figures 2-1 and 2-2 show the pin assignments and Table 2-1 describes the function of each pin. Figures 2-3 and 2-4 show the package dimensions.

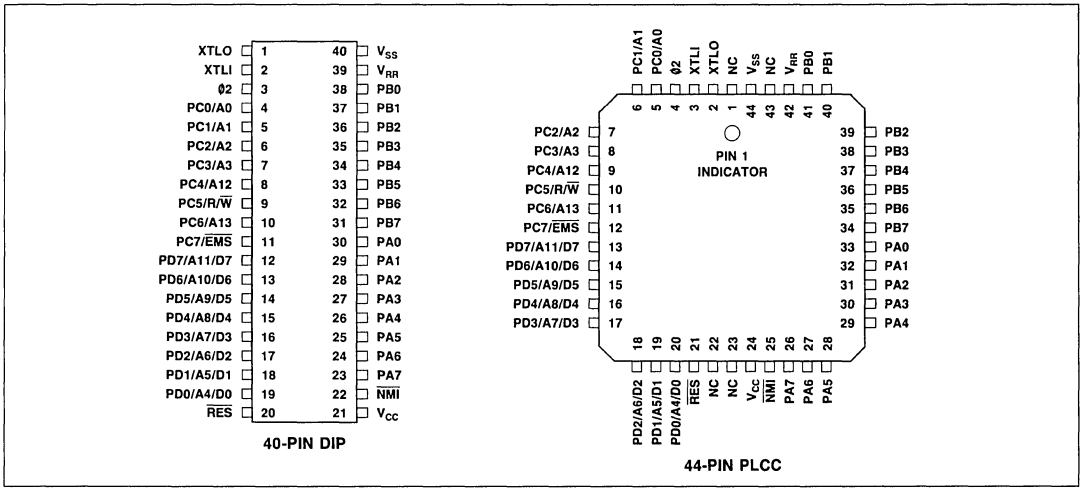


Figure 2-1. R6500/11 and R6500/15 Pin Assignments

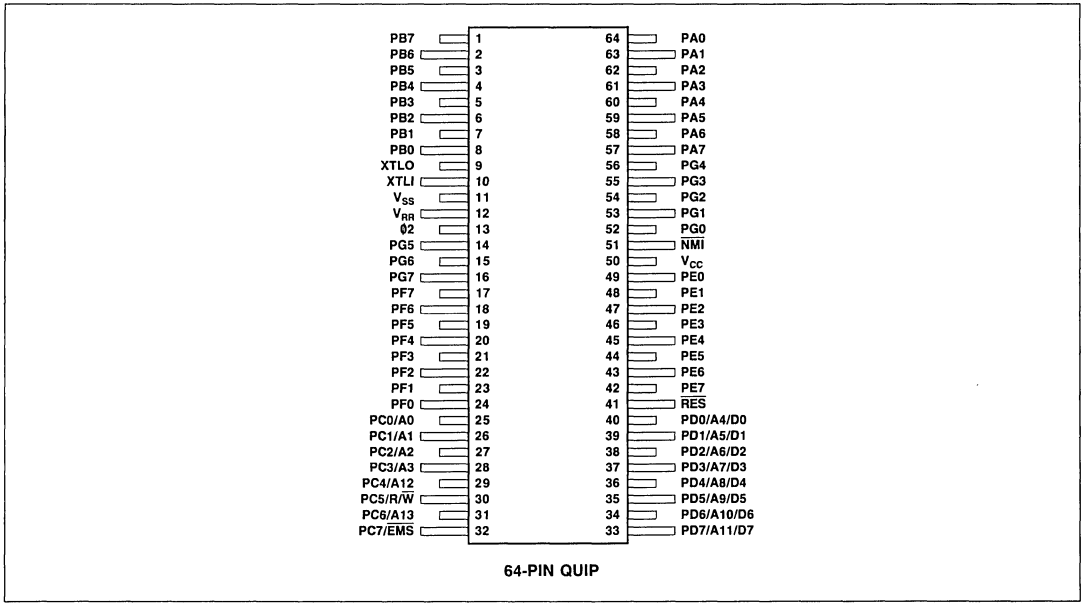
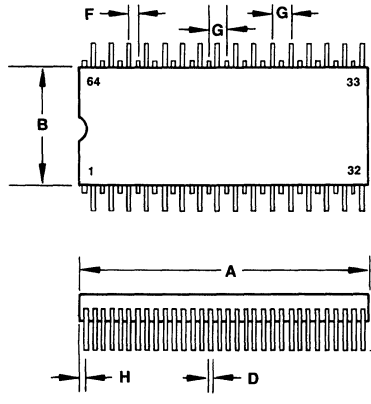


Figure 2-2. R6500/12 Pin Assignments

Table 2-1. Pin Descriptions

Signal Name	I/O Pin Number	Description
V_{CC}		Main power supply +5V.
V_{RR}		Separate power pin for RAM. In the event that V_{CC} power is lost, this power retains RAM data.
V_{SS}		Signal and power ground (0V).
XTLI	I	Crystal or clock input for internal clock oscillator. Also allows input of X1 clock signal if XTLO is connected to V_{SS} or X2 or X4 clock if XTLO is floated.
XTLO	O	Crystal output from internal clock oscillator.
$\overline{RES}$	I	The Reset input is used to initialize the device. This signal must not transition from low to high for at least eight cycles after V_{CC} reaches operating range and the internal oscillator is stabilized.
Ø2	I	Clock signal output at internal frequency.
$\overline{NMI}$	I	A negative going edge on the Non-Maskable interrupt signal requests that a non-maskable interrupt be generated within the CPU.
PA0–PA7 PB0–PB7 PC0–PC7 PD0–PD7	I/O I/O I/O I/O	Four 8-bit ports used for either input/output. Each line of Ports A, B and C consists of an active transistor to V_{SS} and an optional passive pull-up to V_{CC}. In the abbreviated or multiplexed modes of operation Port C has an active pull-up transistor. Port D functions as either an 8-bit input or 8-bit output port. It has active pull-up and pull-down transistors.
PE0–PE7 PF0–PF7 PG0–PG7	O I/O I/O	For the R6500/12, the 64-pin QUIP version, three additional ports (24 lines) are provided. Each line consists of an active transistor to V_{SS}. PF0–PF7 and PG0–PG7 are bidirectional, and an optional passive pull-up to V_{CC} is provided. PE0–PE7 is outputs only with an active pull-up. All ports will source 100 μamps at 2.4V except port E (PE0–PE7) which will source 1 mA at 1.5V.

64 PIN PLASTIC QUIP



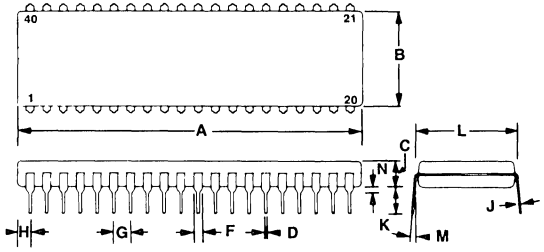
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	41.15	41.66	1.620	1.640
B	17.02	17.53	0.670	0.690
C	3.05	4.56	0.120	0.180
D	0.38	0.51	0.024	0.020
F	1.27 BSC		0.050 BSC	
G	2.54 BSC		0.100 BSC	
H	1.02	1.14	0.040	0.045
J	—	7°	—	7°
K	2.79	4.32	0.110	0.170
L	18.92	19.81	0.745	0.755
M	23.37	23.62	0.920	0.930

Figure 2-3. 64-PIN QUIP Dimensions

PACKAGE DIMENSIONS

40-PIN PLASTIC DIP

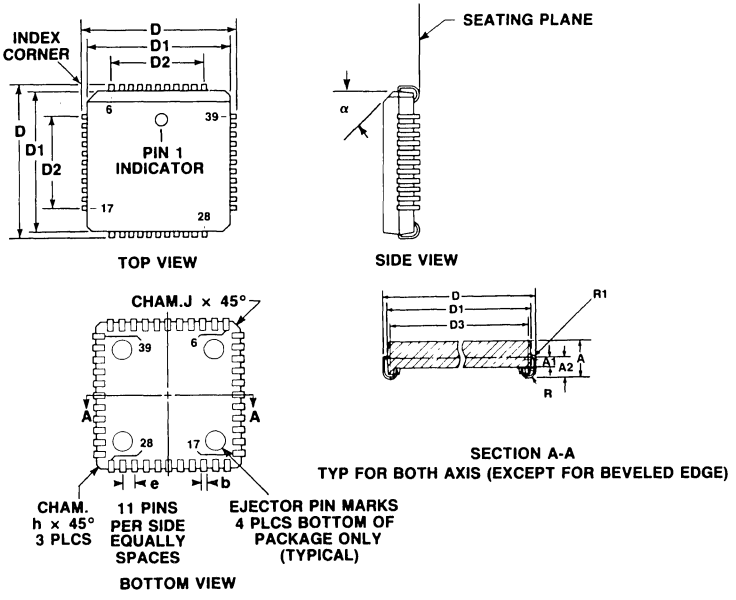
40-PIN PLASTIC DIP



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	51.82	52.32	2.040	2 060
B	13.46	13 97	0.530	0 550
C	3.56	5 08	0.140	0.200
D	0.38	0.53	0 015	0 021
F	1 02	1 52	0 040	0.060
G	2 54 BSC		0.100 BSC	
H	1 65	2 16	0.065	0 085
J	0 20	0.30	0.008	0.012
K	3.30	4.32	0.130	0.170
L	15 24 BSC		0 600 BSC	
M	7°	10°	7°	10°
N	0 51	1.02	0 020	0.040

3

44-PIN PLASTIC LEADED CHIP CARRIER (PLCC)



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.14	4.39	0.163	0.173
A1	1.37	1.47	0.054	0.058
A2	2.31	2.46	0.091	0 097
b	0.457 TYP		0.018 TYP	
D	17.45	17.60	0.687	0.693
D1	16.46	16 56	0.648	0.652
D2	12.62	12.78	0.497	0 503
D3	15.75 REF		0.620 REF	
e	1.27 BSC		0.050 BSC	
h	1.15 TYP		0.045 TYP	
J	0.25 TYP		0.010 TYP	
α	45° TYP		45° TYP	
R	0.89 TYP		0.035 TYP	
R1	0 25 TYP		0 010 TYP	

SECTION 3
SYSTEM ARCHITECTURE

This section provides a functional description of the devices. Functionally they consist of a CPU, both ROM and RAM memories, four 8-bit parallel I/O ports (seven in the 64-pin versions), a serial I/O port, dual counter/latch circuits, a mode control register, and an interrupt flag/enable dual register circuit. A block diagram of the system is shown in Figure 3-1.

NOTE

Throughout this document, unless specified otherwise, all memory or register address locations are specified in hexadecimal notation.

3.1 CPU LOGIC

The internal CPU is a standard 6502 configuration with an 8-bit Accumulator register, two 8-bit Index Registers (X and Y); an 8-bit Stack Pointer register, an ALU, a 16-bit Program Counter, and standard instruction register/decode and internal timing control logic.

3.1.1 Accumulator

The accumulator is a general purpose 8-bit register that stores the results of most arithmetic and logic operations. In addition, the accumulator usually contains one of the two data words used in these operations.

3.1.2 Index Registers

There are two 8-bit index registers, X and Y. Each index register can be used as a base to modify the address data program counter and thus obtain a new address—the sum of the program counter contents and the index register contents.

When executing an instruction which specifies indirect addressing, the CPU fetches the op code and the address, and modifies the address from memory by adding the index register to it prior to loading or storing the value of memory.

Indexing greatly simplifies many types of programs, especially those using data tables.

3.1.3 Stack Pointer

The Stack Pointer is an 8-bit register. It is automatically incremented and decremented under control of the microprocessor to perform stack manipulation in response to either user instructions, an internal $\overline{IRQ}$ interrupt, or the external interrupt line $\overline{NMI}$. The Stack Pointer must be initialized by the user program.

The stack allows simple implementation of multiple level interrupts, subroutine nesting and simplification of many types of data manipulation. The JSR, BRK, RTI and RTS instructions use the stack and Stack Pointer.

The stack can be envisioned as a deck of cards which may only be accessed from the top. The address of a memory location is stored (or "pushed") onto the stack. Each time data are to be pushed onto the stack, the Stack Pointer is placed on the Address Bus, data are written into the memory location addressed by the Stack Pointer, and the Stack Pointer is decremented by 1. Each time data are read (or "pulled") from the stack, the Stack Pointer is incremented by 1. The Stack Pointer is then placed on the Address Bus, and data are read from the memory location addressed by the Pointer.

The stack is located on zero page, i.e., memory locations 00FF-0040. After reset, which leaves the Stack Pointer indeterminate, normal usage calls for its initialization at 00FF.

3.1.4 Arithmetic And Logic Unit (ALU)

All arithmetic and logic operations take place in the ALU, including incrementing and decrementing internal registers (except the Program Counter). The ALU cannot store data for more than one cycle. If data are placed on the inputs to the ALU at the beginning of a cycle, the result is always gated into one of the storage registers or to external memory during the next cycle.

Each bit of the ALU has two inputs. These inputs can be tied to various internal buses or to a logic zero; the ALU then generates the function (AND, OR, SUM, and so on) using the data on the two inputs.

3.1.5 Program Counter

The 16-bit Program Counter provides the addresses that are used to step the processor through sequential instructions in a program. Each time the processor fetches an instruction from program memory, the lower (least significant) byte of the Program Counter (PCL) is placed on the low-order bits of the Address Bus and the higher (most significant) byte of the Program Counter (PCH) is placed on the high-order 8 bits of the Address Bus. The Counter is incremented each time an instruction or data is fetched from program memory.

3.1.6 Instruction Register and Instruction Decode

Instructions are fetched from ROM or RAM and gated onto the Internal Data Bus. These instructions are latched into the Instruction Register then decoded along with timing and interrupt signals to generate control signals for the various registers.

3.1.7 Timing Control

The Timing Control Logic keeps track of the specific instruction cycle being executed. This logic is set to T0 each time an instruction fetch is executed and is advanced at the beginning of each Phase One clock pulse for as many cycles as are required to complete the instruction. Each data transfer which takes place between the registers is caused by decoding the contents of both the instruction register and timing control unit.

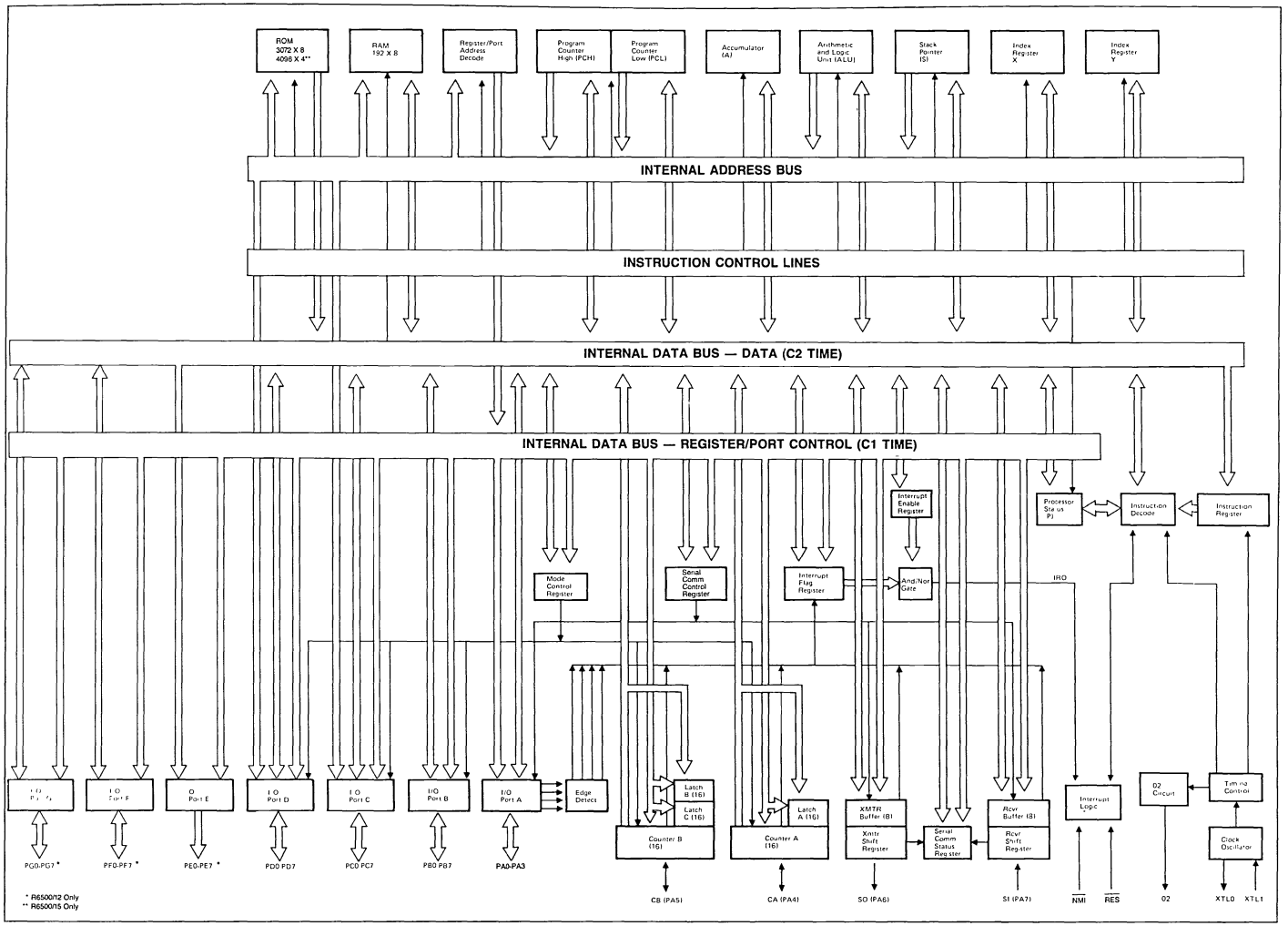


Figure 3-1. System Block Diagram

3.1.8 Interrupt Logic

Interrupt logic controls the sequencing of three interrupts; $\overline{RES}$, $\overline{NMI}$ and $\overline{IRQ}$. $\overline{IRQ}$ is generated by any one of eight conditions: 2 Counter Overflows, 2 Positive Edge Detects, 2 Negative Edge Detects, and 2 Serial Port Conditions.

3.2 NEW INSTRUCTIONS

In addition to the standard 6502 instruction set, four instructions have been added to the devices to simplify operations that previously required a read/modify/write operation. In order for these instructions to be equally applicable to any I/O ports, with or without mixed input and output functions, the I/O ports have been designed to read the contents of the specified port data register during the Read cycle of the read/modify/write operation, rather than I/O pins as in normal read cycles. The added instructions and their format are explained in the following subparagraphs. Refer to Appendix A for the Op Code mnemonic addressing matrix for these added instructions.

3.2.1 Set Memory Bit (SMB m, Addr.)

This instruction sets to "1" one of the 8-bit data field specified by the zero page address (memory or I/O port). The first byte of the instruction specifies the SMB operation and 1 of 8 bits to be set. The second byte of the instruction designates address (00-FF) of the byte or I/O port to be operated upon.

3.2.2 Reset Memory Bit (RMB m, Addr.)

This instruction is the same operation and format as SMB instruction except a reset to "0" of the bit results.

3.2.3 Branch On Bit Set Relative (BBS m, Addr, DEST)

This instruction tests one of 8 bits designated by a three bit immediate field within the first byte of the instruction. The second byte is used to designate the address of the byte to be tested within the zero page address range (memory or I/O ports). The third byte of the instruction is used to specify the 8 bit relative address to which the instruction branches if the bit tested is a "1". If the bit tested is not set, the next sequential instruction is executed.

3.2.4 Branch On Bit Reset Relative (BBR m, Addr, DEST)

This instruction is the same operation and format as the BBS instruction except that a branch takes place if the bit tested is a "0".

3.3 READ-ONLY-MEMORY (ROM)

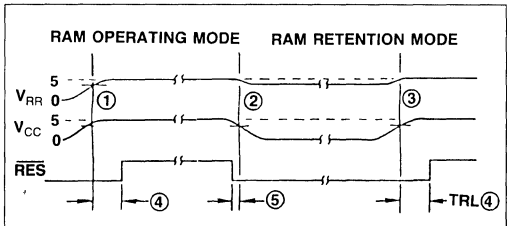
In the R6500/11 or R6500/12 the ROM consists of 3072 bytes (3K) of mask programmable memory with an address space from F400 to FFFF. ROM locations FFFA through FFFF are assigned for interrupt and reset vectors.

In the R6500/15 the ROM consists of 4096 bytes (4K) of mask programmable memory with an address space from F000 to FFFF. ROM locations FFFA through FFFF are assigned for interrupt and reset vectors.

3.4 RANDOM ACCESS MEMORY (RAM)

The RAM consists of 192 bytes of read/write memory with an assigned page zero address of 0040 through 00FF. The R6500/11 provides a separate power pin (V_{RR}) which may be used for standby power for 32 bytes located at 0040-005F. In the event of the loss of V_{CC} power, the lowest 32 bytes of RAM data will be retained if standby power is supplied to the V_{RR} pin. If the RAM data retention is not required then V_{RR} must be connected to V_{CC}. During operation V_{RR} must be at the V_{CC} level.

For the RAM to retain data upon loss of V_{CC}, V_{RR} must be supplied within operating range and $\overline{RES}$ must be driven low at least eight Ø2 clock pulses before V_{CC} falls out of operating range. $\overline{RES}$ must then be held low while V_{CC} is out of operating range and until at least eight Ø2 clock cycles after V_{CC} is again within operating range and the internal Ø2 oscillator is stabilized. V_{RR} must remain within V_{CC} operating range during normal operation. When V_{CC} is out of operating range, V_{RR} must remain within the V_{RR} retention range in order to retain data. Figure 3.2 shows typical waveforms.



1 INITIAL APPLICATION OF V_{CC} AND V_{RR}.
2 LOSS OF V_{CC}, RAM ON STANDBY POWER.
3 REAPPLICATION OF V_{CC}.
4 >8 Ø2 CLOCK PULSES AFTER OSCILLATOR STABILIZATION.
5 >8 Ø2 CLOCK PULSES.

Figure 3-2. Data Retention Timing

3.5 CLOCK OSCILLATOR

Customer selectable mask options are available for controlling the device timing. It can be ordered with a *crystal* oscillator, a *divide-by-2 or divide-by-4* countdown network and for *clock master mode or clock slave mode* operation.

Note:

For 2 MHz internal operations the divide-by-two option must be specified.

The on-chip oscillator is designed for a parallel resonant crystal connected between XTLI and XTLO pins. The equivalent oscillator circuit is shown in Figure 3-3a.

A parallel resonant crystal is specified by its load capacitance and series resonant resistance. For proper oscillator operation, the load capacitance (C_L), series resistance (R_s) and the crystal resonant frequency (F) must meet the following two relations:

$$(C + 27) = 2C_L \quad \text{or} \quad C = 2C_L - 27\ \text{pF}$$

$$R_s \leq R_{smax} = \frac{2 \times 10^6}{(FC_L)^2}$$

where: F is in MHz; C and C_L are in pF; R is in ohms.z

To select a parallel resonant crystal for the oscillator, first select the load capacitance from a crystal manufacturer's catalog. Next, calculate R_{smax} based on F and C_L. The selected crystal must have a R_s less than the R_{smax}.

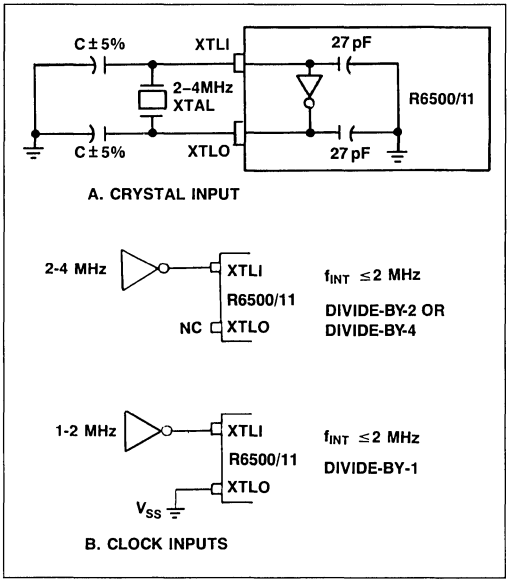


Figure 3-3. Clock Oscillator Input Options

For example, if C_L = 22 pF for a 4 MHz parallel resonant crystal, then

$$C = (2 \times 22) - 27 = 17\ \text{pF}$$
(use standard value of 18 pF)

The series resistance of the crystal must be less than

$$R_{smax} = \frac{2 \times 10^6}{(4 \times 22)^2} = 258\ \text{ohms}$$

Internal timing can also be controlled by driving the XTLI pin with an external frequency source. Figure 3-3b shows typical connections. If XTLO is left floating, the external source is divided by the internal countdown network. However, if XTLO is tied to V_{SS}, the internal countdown network is bypassed causing the chip to operate at the frequency of the external source.

The operation described above assumed a CLOCK MASTER MODE mask option. In this mode a frequence souce (crystal or external source) must be applied to the XTLI and XTLO pins. Ø2 is a buffered output signal which closely approximates the internal timing. When a common external source is used to drive multiple devices the internal timing between devices as well as their Ø2 outputs will be skewed in time. If skewing represents a system problem it can be avoided by the Master/Slave connection and options shown in Figure 3-4.

One device is operated in the CLOCK MASTER MODE and a second in the CLOCK SLAVE MODE. Mask options in the SLAVE unit convert the Ø2 signal into a clock input pin which is tightly coupled to the internal timing generator. As a result the internal timing of the MASTER and SLAVE units are synchronized with minimum skew. If the Ø2 signal to the SLAVE unit is inverted, the MASTER and SLAVE UNITS WILL OPERATE OUT OF PHASE. This approach allows the two devices to share external memory using cycle stealing techniques.

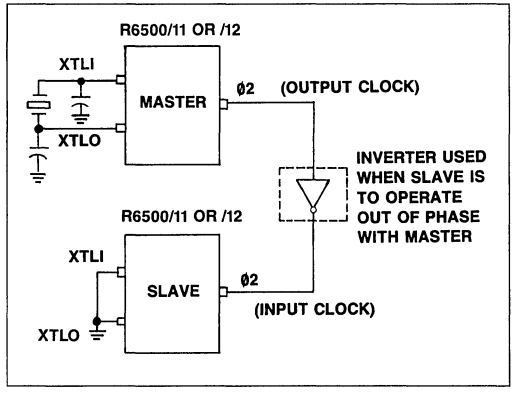


Figure 3-4. Master/Slave Connections

3.6 MODE CONTROL REGISTER (MCR)

The Mode Control Register contains control bits for the multifunction I/O ports and mode select bits for Counter A and Counter B. Its setting, along with the setting of the Serial Communications Control Register (SCCR), determines the basic configuration of the device in any application. Initializing this register is one of the first actions of any software program. The Mode Control Register bit assignment is shown in Figure 3-5.

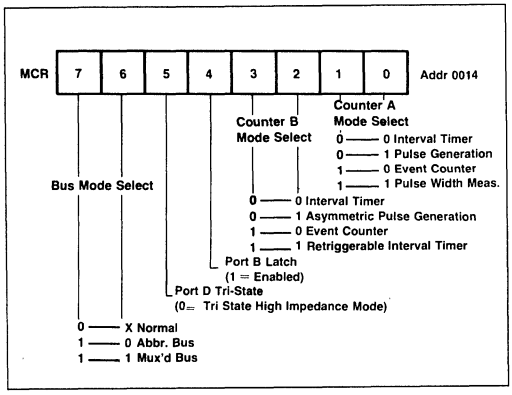


Figure 3-5. Mode Control Register

The use of Counter A Mode Select is shown in Section 6.1.

The use of Counter B Mode Select is shown in Section 6.2.

The use of Port B Latch Enable is shown in Section 4.4.

The use of Port D in Tri-State Enable is shown in Section 4.6.

The use of Bus Mode Select is shown in Section 4.5 and 4.6.

3.7 INTERRUPT FLAG REGISTER (IFR) AND INTERRUPT ENABLE REGISTER (IER)

An $\overline{IRQ}$ interrupt request can be initiated by any or all of eight possible sources. These sources are all capable of being enabled or disabled by the use of the appropriate interrupt enabled bits in the Interrupt Enable Register (IER). Multiple simultaneous interrupts will cause the $\overline{IRQ}$ interrupt request to remain active until all interrupting conditions have been serviced and cleared.

The Interrupt Flag Register contains the information that indicates which I/O or counter needs attention. The contents of the Interrupt Flag Register may be examined at any time by reading at address: 0011. Edge detect IFR bits may be cleared by executing a RMB instruction at address location 0010. The RMB X, (0010) instruction reads FF, modifies bit X to a "0", and writes the modified value at address location 0011. In this way IFR bits set to a "1" after the read cycle of a Read-Modify-Write instruction (such as RMB) are protected from being cleared. A logic "1" is ignored when writing to edge detect IFR bits.

Each IFR bit has a corresponding bit in the Interrupt Enable Register which can be set to a "1" by writing a "1" in the respective bit position at location 0012. Individual IER bits may be cleared by writing a "0" in the respective bit position, or by $\overline{RES}$. If set to a "1", an IRQ will be generated when the corresponding IFR bit becomes true. The Interrupt Flag Register and Interrupt Enable Register bit assignments are shown in Figure 3-6 and the functions of each bit are explained in Table 3-1.

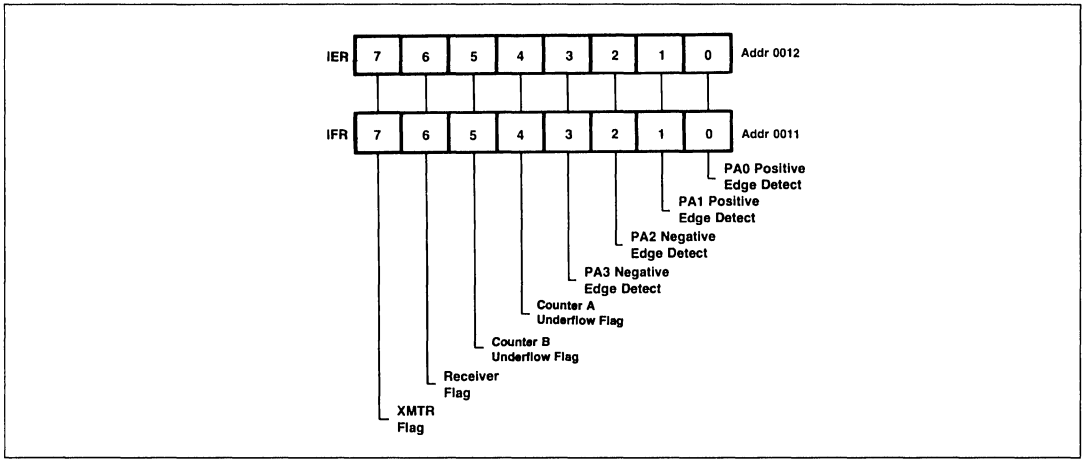


Figure 3-6. Interrupt Enable and Flag Registers

Table 3-1. Interrupt Flag Register Bit Codes

BIT CODE	FUNCTION
IFR 0:	PA0 Positive Edge Detect Flag—Set to a "1" when a positive going edge is detected on PA0. Cleared by RMB 0 (0010) instruction or by $\overline{RES}$.
IFR 1:	PA1 Positive Edge Detect Flag—Set to a 1 when a positive going edge is detected on PA1. Cleared by RMB 1 (0010) instruction or by $\overline{RES}$.
IFR 2:	PA2 Negative Edge Detect Flag—Set to a 1 when a negative going edge is detected on PA2. Cleared by RMB 2 (0010) instruction or by $\overline{RES}$.
IFR 3:	PA3 Negative Edge Detect Flag—Set to 1 when a negative going edge is detected on PA3. Cleared by RMB 3 (0010) instruction or by $\overline{RES}$.
IFR 4:	Counter A Underflow Flag—Set to a 1 when Counter A underflow occurs. Cleared by reading the Lower Counter A at location 0018, by writing to address location 001A, or by $\overline{RES}$.
IFR 5:	Counter B Underflow Flag—Set to a 1 when Counter B underflow occurs. Cleared by reading the Lower Counter B at location 001C, by writing to address location 001E, or by $\overline{RES}$.
IFR 6:	Receiver Interrupt Flag—Set to a 1 when any of the Serial Communication Status Register bits 0 through 3 is set to a 1. Cleared when the Receiver Status bits (SCSR 0-3) are cleared or by $\overline{RES}$.
IFR 7:	Transmitter Interrupt Flag—Set to a 1 when SCSR 6 is set to a 1 while SCSR 5 is a 0 or SCSR 7 is set to a 1. Cleared when the Transmitter Status bits (SCSR 6 & 7) are cleared or by $\overline{RES}$.

3.8 PROCESSOR STATUS REGISTER

The 8-bit Processor Status Register, shown in Figure 3-7, contains seven status flags. Some of these flags are controlled by the user program; others may be controlled both by the user's program and the CPU. The R6502 instruction set contains a number of conditional branch instructions which are designed to allow testing of these flags. Each of the eight processor status flags is described in the following sections.

3.8.1 Carry Bit (C)

The Carry Bit (C) can be considered as the ninth bit of an arithmetic operation. It is set to logic 1 if a carry from the eighth bit has occurred or cleared to logic 0 if no carry occurred as the result of arithmetic operations.

The Carry Bit may be set or cleared under program control by use of the Set Carry (SEC) or Clear Carry (CLC) instruction, respectively. Other operations which affect the Carry Bit are ADC, ASL, CMP, CPX, CPY, LSR, PLP, ROL, ROR, RTI, and SBC.

3.8.2 Zero Bit (Z)

The Zero Bit (Z) is set to logic 1 by the CPU during any data movement or calculation which sets all 8 bits of the result to zero. This bit is cleared to logic 0 when the resultant 8 bits of a data movement or calculation operation are not all zero. The R6500 instruction set contains no instruction to specifically set or clear the Zero Bit. The Zero Bit is, however, affected by the following instructions; ADC, AND, ASL, BIT, CMP, CPX, CPY, DEC, DEX, DEY, EOR, INC, INX, INY, LDA, LDX, LDY, LSR, ORA, PLA, PLP, ROL, ROR, RTI, SBC, TAX, TAY, TXA, TSX, and TYA.

3.8.3 Interrupt Disable Bit (I)

The Interrupt Disable Bit (I) is used to control the servicing of an interrupt request ($\overline{IRQ}$). If the I Bit is reset to logic 0, the $\overline{IRQ}$ signal will be serviced. If the bit is set to logic 1, the $\overline{IRQ}$ signal will be ignored. The CPU will set the Interrupt Disable Bit to logic 1 if a RESET ($\overline{RES}$), $\overline{IRQ}$, or Non-Maskable Interrupt ($\overline{NMI}$) signal is detected.

The I bit is cleared by the Clear Interrupt Mask Instruction (CLI) and is set by the Set Interrupt Mask Instruction (SEI). This bit is set by the BRK Instruction. The Return from Interrupt (RTI) and Pull Processor Status (PLP) instructions will also affect the I bit.

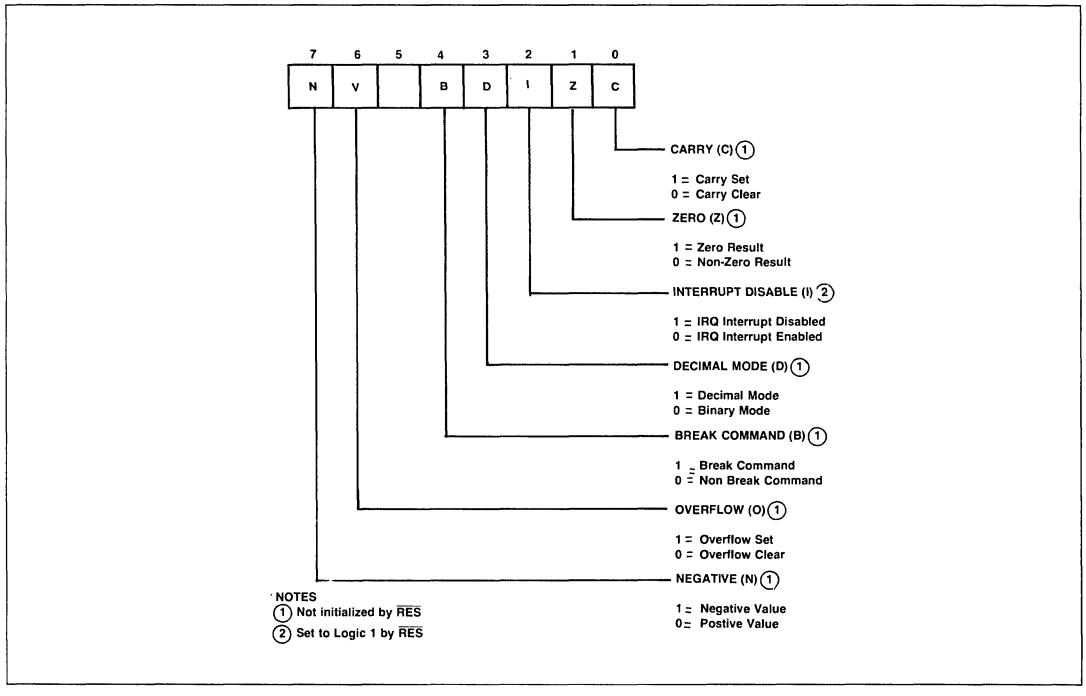


Figure 3-7. Processor Status Register

3.8.4 Decimal Mode Bit (D)

The Decimal Mode Bit (D), is used to control the arithmetic mode of the CPU. When this bit is set to logic 1, the adder operates as a decimal adder. When this bit is cleared to logic 0, the adder operates as a straight binary adder. The adder mode is controlled only by the programmer. The Set Decimal Mode (SED) instruction will set the D bit; the Clear Decimal Mode (CLD) instruction will clear it. The PLP and RTI instructions also effect the Decimal Mode Bit.

CAUTION

The Decimal Mode Bit will either set or clear in an unpredictable manner upon power application. This bit must be initialized to the desired state by the user program or erroneous results may occur.

3.8.5 Break Bit (B)

The Break Bit (B) is used to determine the condition which caused the $\overline{IRQ}$ service routine to be entered. If the $\overline{IRQ}$ service routine was entered because the CPU executed a BRK command, the Break Bit will be set to logic 1. If the $\overline{IRQ}$ routine was entered as the result of an $\overline{IRQ}$ signal being generated, the B bit will be cleared to logic 0. There are no instructions which can set or clear this bit.

3.8.6 Overflow Bit (V)

The Overflow Bit (V) is used to indicate that the result of a signed, binary addition, or subtraction, operation is a value that cannot be contained in seven bits ($-128 \leq n \leq 127$). This indicator only has meaning when signed arithmetic (sign and seven magnitude bits) is performed. When the ADC or SBC instruction is performed, the Overflow Bit is set to logic 1 if the polarity of the sign bit (bit 7) is changed because the result exceeds +127 or −128; otherwise the bit is cleared to logic 0. The V bit may also be cleared by the programmer using a Clear Overflow (CLV) instruction.

The Overflow Bit may also be used with the BIT instruction. The BIT instruction which may be used to sample interface devices, allows the overflow flag to reflect the condition of bit 6 in the sampled field. During a BIT instruction the Overflow Bit is set equal to the content of the bit 6 on the data tested with BIT instruction. When used in this mode, the overflow has nothing to do with signed arithmetic, but is just another sense bit for the microprocessor. Instructions which affect the V flag are ADC, BIT, CLV, PLP, RTI and SBC.

3.8.7 Negative Bit (N)

The Negative Bit (N) is used to indicate that the sign bit (bit 7), in the resulting value of a data movement or data arithmetic operation, is set to logic 1. If the sign bit is set to logic 1, the resulting value of the data movement or arithmetic operation is negative; if the sign bit is cleared, the result of the data movement or arithmetic operation is positive. There are no instructions that set or clear the Negative Bit since the Negative Bit represents only the status of a result. The instructions that effect the state of the Negative Bit are: ADC, AND, ASL, BIT, CMP, CPX, CPY, DEC, DEX, DEY, EOR, INC, INX, INY, LDA, LDX, LDY, LSR, ORA, PLA, PLP, ROL, ROR, RTI, SBC, TAX, TAY, TSX, TXA, and TYA.

SECTION 4
PARALLEL INPUT/OUTPUT PORTS

The R6500/11 or R6500/15 has 32 I/O lines grouped into four 8-bit ports (PA, PB, PC, and PD). Ports A through C may be used either for input or output individually or in groups of any combination. Port D may be used as all inputs or all outputs.

The R6500/12, a 64-pin QUIP device, has three additional ports: PE, PF and PG. PE is outputs only; PF and PG are bidirectional.

Multifunction I/O's such as Port A and Port C are protected from normal port I/O instructions when they are programmed to perform a multiplexed function.

Internal pull-up resistors (FET's with an impedance range of 3K ≤ Rpu ≤ 12K ohm) may be provided on all port pins except Port D and E as a mask option.

The direction of the I/O lines are controlled by four 8-bit port registers located in page zero. This arrangement provides quick programming access using simple two-byte zero page address instructions. There are no direction registers associated with the I/O ports, which simplifies I/O handling. The I/O addresses are shown in Table 4-1. Section E.6 shows the I/O Port Timing.

Table 4-1. I/O Port Addresses

Port	Address
A	0000
B	0001
C	0002
D	0003
E	0004
F	0005
G	0006

4.1 INPUTS

Inputs for Ports A, B, and C and also Ports F and G of the R6500/12 are enabled by loading logic 1 into all I/O port register bit positions that are to correspond to I/O input lines. A low (<0.8V) input signal will cause a logic 0 to be read when a read instruction is issued to the port register. A high (>2.0V) input will cause a logic 1 to be read. An RES signal forces all I/O port registers to logic 1 thus initially treating all I/O lines as inputs.

Port D may only be all inputs or all outputs. All inputs is selected by setting bit 5 of the Mode Control Register (MCR5) to a "0".

The status of the input lines can be interrogated at any time by reading the I/O port addresses. Note that this will return the actual status of the input lines, not the data written into the I/O port registers.

Read/Modify/Write instructions can be used to modify the operation of PA, PB, PC, & PD and also ports PF and PG of the R6500/12. During the Read cycle of a Read/Modify/Write instruction the Port I/O register is read. For all other read instructions the port input lines are read. Read/Modify/Write instructions are: ASL, DEC, INC, LSR, RMB, ROL, ROR, and SMB.

4.2 OUTPUTS

Outputs for Ports A thru D and Ports E thru G of the R6500/12 are controlled by writing the desired I/O line output states into the corresponding I/O port register bit positions. A logic 1 will force a high (>2.4V) output while a logic 0 will force a low (<0.4V) output.

Port D all outputs is selected by setting MCR5 to a "1".

Port E is always all outputs.

4.3 PORT A (PA)

Port A can be programmed via the Mode Control Register (MCR) and the Serial Communications Control Register (SCCR) as a standard parallel 8-bit, bit independent, I/O port or as serial channel I/O lines, counter I/O lines, or an input data strobe for the Port B input latch option. Table 4-2 tabulates the control and usage of Port A.

In addition to their normal I/O functions, PA0 and PA1 can detect positive going edges, and PA2 and PA3 can detect negative going edges. A proper transition on these pins will set a corresponding status bit in the IFR and generate an interrupt request if the respective Interrupt Enable Bit is set. The maximum rate at which an edge can be detected is one-half the 02 clock rate. Edge detection timing is shown in Section E.5.

Table 4-2. Port A Control & Usage

PA0 (2)	PA0 I/O		PORT B LATCH MODE	
	MCR4 = 0		MCR4 = 1	
	SIGNAL		SIGNAL	
	NAME	TYPE	NAME	TYPE
	PA0	I/O	PORT B LATCH STROBE	INPUT (1)
PA1 (2) **PA2 (3)** **PA3 (3)**	PA1–PA3 I/O			
	SIGNAL			
	NAME	TYPE		
	PA1 PA2 PA3	I/O I/O I/O		
PA4	PA4 I/O		COUNTER A I/O	
	MCR0 = 0 MCR1 = 0 SCCR7 = 0 RCVR S/R MODE = 0 (4) (5)		MCR0 = 1 MCR1 = 0 SCCR7 = 0 RCVR S/R MODE = 0 (4)	SCCR7 = 0 SCCR6 = 0 MCR1 = 1
	SIGNAL		SIGNAL	SIGNAL
	NAME	TYPE	NAME TYPE	NAME TYPE
	PA4	I/O	CNTA OUTPUT	CNTA INPUT (1)
	SERIAL I/O SHIFT REGISTER CLOCK			
	SCCR7 = 1 SCCR5 = 1		RCVR S/R MODE = 1 (4)	
	SIGNAL		SIGNAL	
	NAME	TYPE	NAME	TYPE
	XMTR CLOCK	OUTPUT	RCVR CLOCK	INPUT (1)
PA5	PA5 I/O		COUNTER B I/O	
	MCR3 = 0 MCR2 = 0		MCR3 = 0 MCR2 = 1	MCR3 = 1 MCR2 = X
	SIGNAL		SIGNAL	SIGNAL
	NAME	TYPE	NAME TYPE	NAME TYPE
	PA5	I/O	CNTB OUTPUT	CNTB INPUT (1)
PA6	PA6 I/O		SERIAL I/O XMTR OUTPUT	
	SCCR7 = 0		SCCR7 = 1	
	SIGNAL		SIGNAL	
	NAME	TYPE	NAME TYPE	
	PA6	I/O	XMTR OUTPUT	
PA7	PA7 I/O		SERIAL I/O RCVR INPUT	
	SCCR6 = 0		SCCR6 = 1	
	SIGNAL		SIGNAL	
	NAME	TYPE	NAME TYPE	
	PA7	I/O	RCVR INPUT (1)	

Notes:
(1) Hardware Buffer Float
(2) Positive Edge Detect
(3) Negative Edge Detect
(4) RCVR S/R Mode = 1 when SCCR6 • $\overline{\text{SCCR5}}$ • SCCR4 = 1
(5) For the following mode combinations PA4 is available as an input only pin:
$\overline{\text{SCCR7}}$•SCCR6•$\overline{\text{SCCR5}}$.MCR1
+$\overline{\text{SCCR7}}$•SCCR6•$\overline{\text{SCCR4}}$•MCR1
+SCCR7•$\overline{\text{SCCR6}}$•$\overline{\text{SCCR5}}$
+SCCR7•$\overline{\text{SCCR5}}$•$\overline{\text{SCCR4}}$•

4.4 PORT B (PB)

Port B can be programmed as an 8 bit, bit independent I/O port. It has a latched input capability which may be enabled or disabled via the Mode Control Register (MCR). Table 4-3 tabulates the control and usage of Port B. An Input Data Strobe signal must be provided thru PA0 when Port B is programmed to be used with latched input option. Input data latch timing for Port B is shown in Section E.5.

Table 4-3. Port B Control & Usage

Pin Name	I/O Mode MCR4 = 0 Signal Name	I/O Mode MCR4 = 0 Signal Type (1)	Latch Mode MCR4 = 1 (2) Signal Name	Latch Mode MCR4 = 1 (2) Signal Type
PB0	PB0	I/O	PB0	INPUT
PB1	PB1	I/O	PB1	INPUT
PB2	PB2	I/O	PB2	INPUT
PB3	PB3	I/O	PB3	INPUT
PB4	PB4	I/O	PB4	INPUT
PB5	PB5	I/O	PB5	INPUT
PB6	PB6	I/O	PB6	INPUT
PB7	PB7	I/O	PB7	INPUT

(1) Resistive pull-up, active buffer pull down
(2) Input data is stored in port B latch by PA0 pulse

4.5 PORT C (PC)

Port C can be programmed as an I/O port and in conjunction with Port D, as an abbreviated bus, or as a multiplexed bus. When used in the abbreviated or multiplexed bus modes, PC0-PC7 function as A0-A3, A12, R/W, A13, and $\overline{EMS}$, respectively, as shown in Table 4-4. $\overline{EMS}$ (External Memory Select) is asserted (low) whenever the internal processor accesses memory area between 0100 and 3FFF. (See Memory Map, Appendix B). The leading edge of $\overline{EMS}$ may be used to strobe the eight address lines multiplexed on Port D in the Multiplexed Bus Mode. See Appendix E.3 through E.5 for Port C timing.

4.6 PORT D (PD)

Port D can be programmed as an I/O Port, an 8-bit tri-state data bus, or as a multiplexed bus. Mode selection for Port D is made by the Mode Control Register (MCR). The Port D output drivers can be selected as tri-state drivers by setting bit 5 of the MCR to 0 (zero). Table 4-5 shows the necessary settings for the MCR to achieve the various modes for Port D. When Port D is selected to operate in the Abbreviated Mode PD0-PD7 serves as data register bits D0-D7. When Port D is selected to operate in the Multiplexed Mode data bits D0 through D7 are time multiplexed with address bits A4 through A11, respectively. Refer to the Memory Maps (Appendix C) for Abbreviated and Multiplexed memory assignments. See Appendix E.3 through E.5 for Port D timing.

4.7 PORT E, PORT F AND PORT G (PE, PF & PG R6500/12 ONLY

Port E only operates in the Output mode. It provides a Darlington output that can source current at the high (1) level. Port F and Port G operate identically and can be programmed as bidirectional I/O ports. They have standard output capability. See Appendix E.5 for Port E, F & Port G timing.

4.8 BUS MODES

In the Abbreviated Bus Mode, Port C and Port D are automatically transformed into an abbreviated address bus and control signals (Port C) and a bidirectional data bus (Port D). 64 Peripheral addresses can be selected. In general usage, these 64 addresses would be distributed to several external I/O devices such as R6522 and R6520, etc., each of which may contain more than one unique address.

In the Multiplexed Bus Mode, the operation is similar to the Abbreviated Mode except that a full 16K of external addresses are provided. Port C provides the lower addresses and control signals. Port D multiplexes functions. During the first half of the cycle it contains the remaining necessary 8 address bits for 16K; during the second half of the cycle it contains a bidirectional data bus. The address bits appearing on Port D must be latched into an external holding register. The leading edge of $\overline{EMS}$, which indicates that the bus function is active, may be used for this purpose.

MCR5 must be a logic 1 in the Abbreviated and Multiplexed Bus Modes.

Figures 4-1a through 4-1c show the possible configurations of the four bus modes.

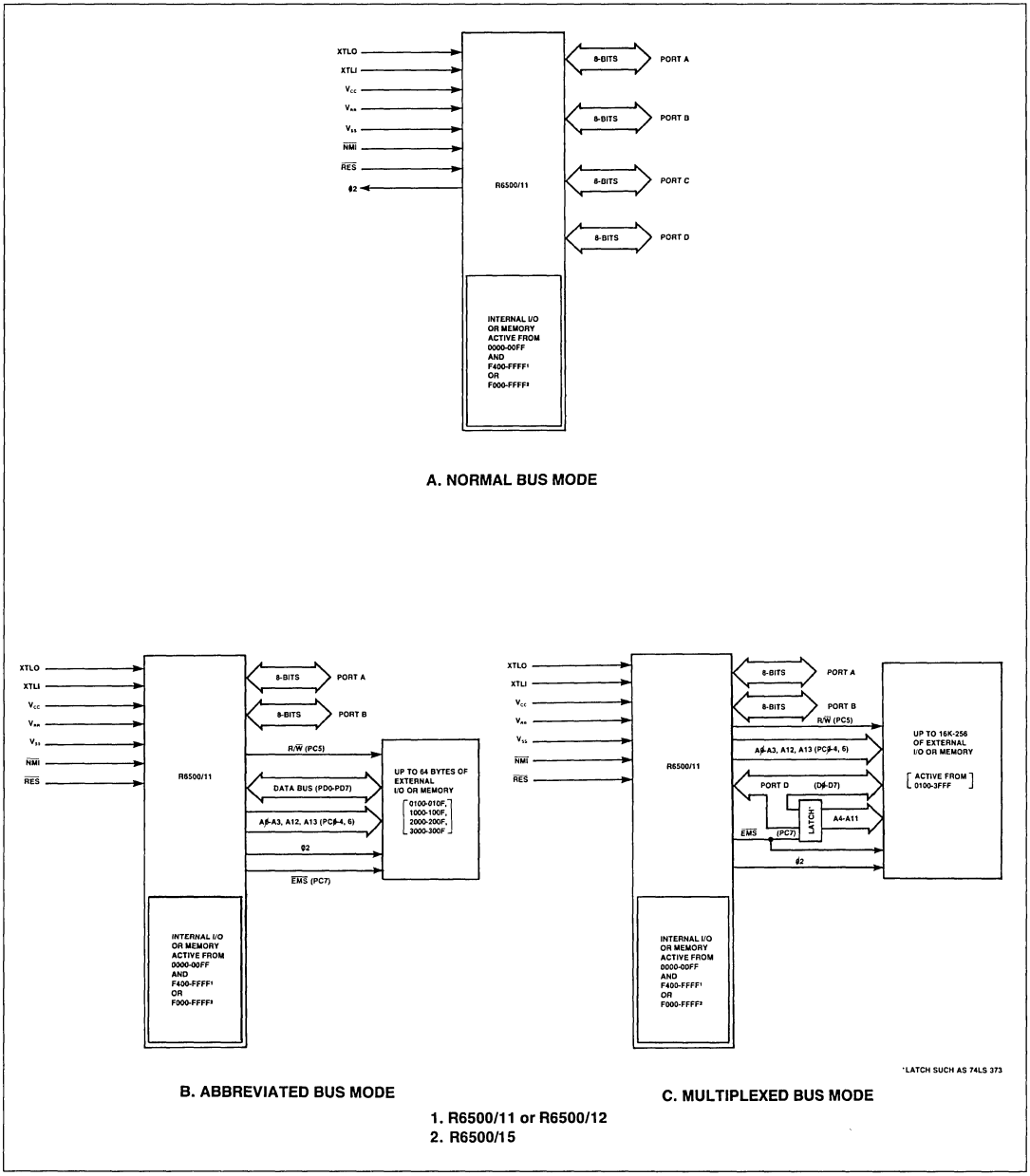


Figure 4-1. Bus Mode Configurations

Table 4-4. Port C Control and Usage

Pin Name	I/O Mode MCR7 = 0 MCR6 = X Signal Name	I/O Mode Type (1)	Abbreviated Mode MCR7 = 1 MCR6 = 0 Signal Name	Abbreviated Mode Type (2)	Multiplexed Mode MCR7 = 1 MCR6 = 1 Signal Name	Multiplexed Mode Type (2)
PC0	PC0	I/O	A0	OUTPUT	A0	OUTPUT
PC1	PC1	I/O	A1	OUTPUT	A1	OUTPUT
PC2	PC2	I/O	A2	OUTPUT	A2	OUTPUT
PC3	PC3	I/O	A3	OUTPUT	A3	OUTPUT
PC4	PC4	I/O	A12	OUTPUT	A12	OUTPUT
PC5	PC5	I/O	R/$\overline{W}$	OUTPUT	R/$\overline{W}$	OUTPUT
PC6	PC6	I/O	A13	OUTPUT	A13	OUTPUT
PC7	PC7	I/O	$\overline{EMS}$	OUTPUT	$\overline{EMS}$	OUTPUT

(1) Resistive Pull-Up, Active Buffer Pull-Down
(2) Active Buffer Pull-Up and Pull-Down

Table 4-5. Port D Control and Usage

Pin Name	I/O Modes MCR7 = 0 MCR6 = X MCR5 = 0 Signal Name	Type (1)	I/O Modes MCR7 = 0 MCR6 = X MCR5 = 1 Signal Name	Type (2)	Abbreviated Mode MCR7 = 1 MCR6 = 0 MCR5 = 1 Signal Name	Type (3)	Multiplexed Mode MCR7 = 1 MCR5 = 1 MCR5 = 1 Signal Phase 1 Name	Type (2)	Signal Phase 2 Name	Type (3)
PD0	PD0	INPUT	PD0	OUTPUT	DATA0	I/O	A4	OUTPUT	DATA0	I/O
PD1	PD1	INPUT	PD1	OUTPUT	DATA1	I/O	A5	OUTPUT	DATA1	I/O
PD2	PD2	INPUT	PD2	OUTPUT	DATA2	I/O	A6	OUTPUT	DATA2	I/O
PD3	PD3	INPUT	PD3	OUTPUT	DATA3	I/O	A7	OUTPUT	DATA3	I/O
PD4	PD4	INPUT	PD4	OUTPUT	DATA4	I/O	A8	OUTPUT	DATA4	I/O
PD5	PD5	INPUT	PD5	OUTPUT	DATA5	I/O	A9	OUTPUT	DATA5	I/O
PD6	PD6	INPUT	PD6	OUTPUT	DATA6	I/O	A10	OUTPUT	DATA6	I/O
PD7	PD7	INPUT	PD7	OUTPUT	DATA7	I/O	A11	OUTPUT	DATA7	I/O

(1) Tri-State Buffer is in High Impedance Mode
(2) Tri-State Buffer is in Active Mode
(3) Tri-State Buffer is in Active Mode Only During the Phase 2 Portion of a Write Cycle

SECTION 5
SERIAL INPUT/OUTPUT CHANNEL

The device provides a full duplex Serial I/O channel with programmable bit rates and operating modes. The serial I/O functions are controlled by the Serial Communication Control Register (SCCR). The SCCR bit assignment is shown in Figure 5-1. The serial bit rate is determined by Counter A for all modes except the Receiver Shift Register (RCVR S/R) mode for which an external shift clock must be provided. The maximum data rate using the internal clock is 62.5K bits per second (@ $\phi 2$ = 1 MHz). The transmitter (XMTR) and receiver (RCVR) can be independently programmed to operate in different modes and can be independently enabled or disabled.

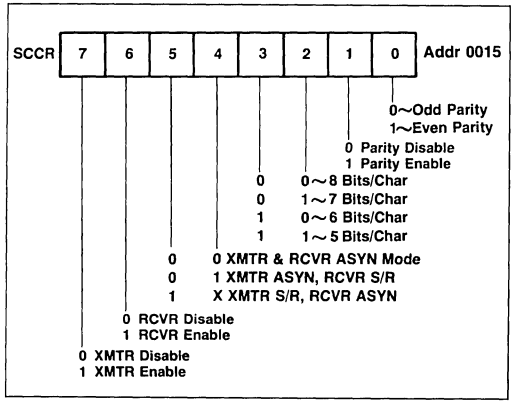


Figure 5-1. Serial Communication Control Register

Except for the Receiver Shift Register Mode (RCVR S/R), all XMTR and RCVR bit rates will occur at one sixteenth of the Counter A interval timer rate. Counter A is forced into an interval timer mode whenever the serial I/O is enabled in a mode requiring an internal clock.

Whenever Counter A is required as a timing source it must be loaded with the hexadecimal code that selects the data rate for the serial I/O Port. Refer to Counter A (paragraph 6.1) for a table of hexadecimal values to represent the desired data rate.

5.1 TRANSMITTER OPERATION (XTMR)

The XTMR operation and the transmitter related control/status functions are enabled by bit 7 of the Serial Communications Control Register (SCCR). The transmitter, when in the Asynchronous (ASYN) mode, automatically adds a start bit, one or two stop bits, and, when enabled, a parity bit to the transmitted data. A word of transmitted data (in asynchronous parity mode) can have 5, 6, 7, or 8 bits of data. The nine data modes are in Figure 5-2. When parity is disabled, the 5, 6, 7 or 8 bits of data are terminated with two stop bits.

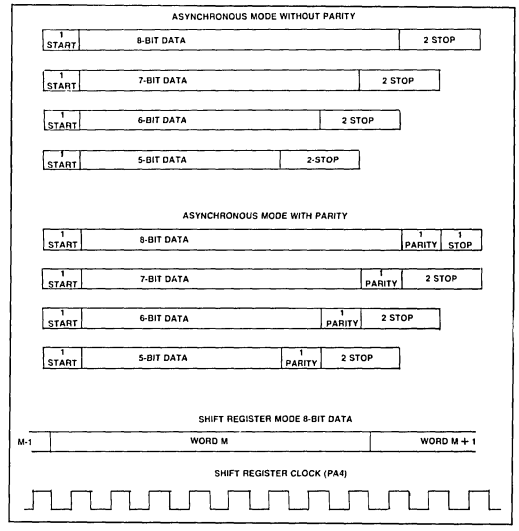


Figure 5-2. Transmitted Data Modes

In the S/R mode, eight data bits are always shifted out. Bits/character and parity control bits are ignored. The serial data is shifted out via the SO output (PA6) and the shift clock is available at the CA (PA4) pin. When the transmitter underruns in the S/R mode the SO output and shift clock are held in a high state.

The XMTR Interrupt Flag bit (IFR7) is controlled by Serial Communication Status Register bits SCSR5, SCSR6 and SCSR7.

$$IFR7 = SCSR6\ (\overline{SCSR5} + SCSR7)$$

5.2 RECEIVER OPERATION (RCVR)

The receiver and its selected control and status functions are enabled when SCCR-6 is set to a "1." In the ASYN mode, data format must have a start bit, appropriate number of data bits, a parity bit (if enabled) and one stop bit. Refer to paragraph 5.1 for a diagram of bit allocations. The receiver bit period is divided into 8 sub-intervals for internal synchronization. The receiver bit stream is synchronized by the start bit and a strobe signal is generated at the approximate center of each incoming bit. Refer to Figure 5-3 for ASYN Receive Data Timing. The character assembly process does not start if the start bit signal is less than one-half the bit time after a low level is detected on the Receive Data Input. Framing error, over-run, and parity error conditions or a RCVR Data Register Full will set the appropriate status bits, and any of the above conditions will cause an Interrupt Request if the Receiver Interrupt Enable bit is set to logic 1.

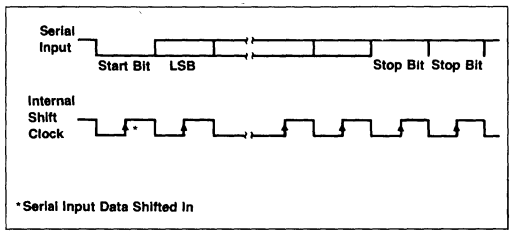


Figure 5-3. ASYN Receive Data Timing

In the S/R mode, an external shift clock must be provided at CA (PA4) pin along with 8 bits of serial data (LSB first) at the SI input (PA7). The maximum data rate using an external shift clock is one-eighth the internal clock rate. Refer to Figure 5-4 for S/R Mode Timing.

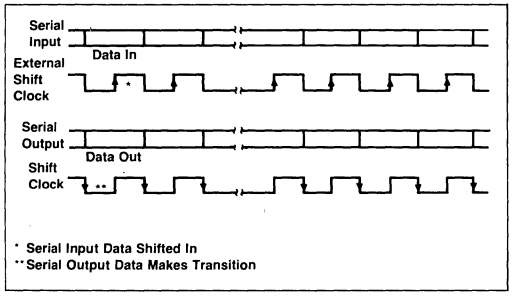


Figure 5-4. S/R Mode Timing

A RCVR interrupt (IFR6) is generated whenever any of SCSR0-3 are true.

5.3 SERIAL COMMUNICATION STATUS REGISTER (SCSR)

The Serial Communication Status Register (SCSR) holds information on various communication error conditions, status of the transmitter and receiver data registers, a transmitter end-of-transmission condition, and a receiver idle line condition (Wake-Up Feature). The SCSR bit assignment is shown in Figure 5-5. Bit assignments and functions of the SCSR are as follows:

SCSR0: *Receiver Data Register Full*—Set to a logic 1 when a character is transferred from the Receiver Shift Register to the Receiver Data Register. This bit is cleared by reading the Receiver Data Register, or by $\overline{RES}$ and is disabled if SCCR6 = 0. The SCSR 0 bit will not be set to a logic 1 if the received data contains an error condition, instead, a corresponding error bit will be set to a logic 1.

SCSR1: *Over-Run Error*—Set to a logic 1 when a new character is transferred from the Receiver Shift Register, with the last character still in the Receiver Data Register. This bit is cleared by reading the Receiver Data Register, or by $\overline{RES}$.

SCSR2: *Parity Error*—Set to logic 1 when the RCVR is in the ASYN Mode, Parity Enable bit is set, and the received data has a parity error. This bit is cleared by reading the Receiver Data Register or by $\overline{RES}$.

SCSR3: *Framing Error*—Set to a logic 1 when the received data contains a zero bit after the last data or parity bit in the stop bit slot. Cleared by reading the Receiver Data Register or by $\overline{RES}$. (ASYN Mode only).

SCSR4: *Wake-Up*—Set to a logic 1 by writing a "1" in bit 4 of address: 0016. The Wake-Up bit is cleared by $\overline{RES}$ or when the receiver detects a string of ten consecutive 1's. When the Wake-Up bit is set SCSR0 through SCSR3 are inhibited.

SCSR5: *End of Transmission*—Set to a logic 1 by writing a "1" in bit position 5 of address: 0016. The End of Transmission bit is cleared by $\overline{RES}$ or upon writing a new data word into the Transmitter Data Register. When the End-of-Transmission bit is true the Transmitter Register Empty bit is disabled until a Transmitter Under-Run occurs.

SCSR6: *Transmitter Data Register Empty*—Set to a logic 1 when the contents of the Transmitter Data Register is transferred to the Transmitter Shift Register. Cleared upon writing new data into the Transmit Data Register. This bit is initialized to a logic 1 by $\overline{RES}$.

SCSR7: *Transmitter Under-Run*—Set to a logic 1 when the last data bit is transmitted if the transmitter is in a S/R Mode or when the last stop bit is transmitted if the XMTR is in the ASYN Mode while the Transmitter Data Register Empty Bit is set. Cleared by a transfer of new data into the Transmitter Shift Register, or by $\overline{RES}$.

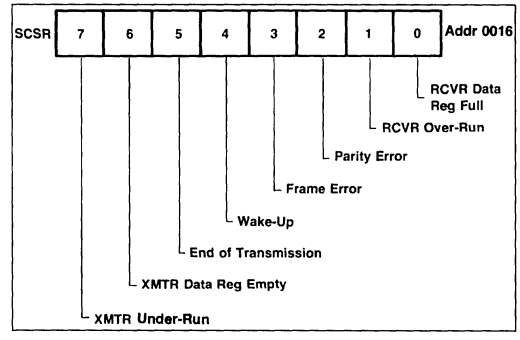


Figure 5-5. SCSR Bit Allocation

5.4 WAKE-UP FEATURE

In a multi-distributed microprocessor or microcomputer applications, a destination address is usually included at the beginning of the message. The Wake-Up Feature allows non-selected CPU's to ignore the remainder of the message until the beginning of the next message by setting the Wake-Up bit. As long as the Wake-Up flag is true, the Receiver Data Register Full Flag remains false. The Wake-Up bit is automatically cleared when the receiver detects a string of eleven consecutive 1's which indicates an idle transmit line. When the next byte is received, the Receiver Data Register Full Flag signals the CPU to wake-up and read the received data.

SECTION 6
COUNTER/TIMERS

The device contains two 16-bit counters (Counter A and Counter B) and three 16-bit latches associated with the counters. Counter A has one 16-bit latch and Counter B has two 16-bit latches. Each counter can be independently programmed to operate in one of four modes:

Counter A	Counter B
• Pulse width measurement	• Retriggerable Interval Counter
• Pulse Generation	• Asymmetrical Pulse Generation
• Interval Timer	• Interval Timer
• Event Counter	• Event Counter

Operating modes of Counter A and Counter B are controlled by the Mode Control Register. All counting begins at the initialization value and decrements. When modes are selected requiring a counter input/output line, PA4 is automatically selected for Counter A and PA5 is automatically selected for Counter B (see Table 4.2).

6.1 COUNTER A

Counter A consists of a 16-bit counter and a 16-bit latch organized as follows: Lower Counter A (LCA), Upper Counter A (UCA), Lower Latch A (LLA), and Upper Latch A (ULA). The counter contains the count of either ϕ2 clock pulses or external events, depending on the counter mode selected. The contents of Counter A may be read any time by executing a read at location 0019 for the Upper Counter A and at location 001A or location 0018 for the Lower Counter A. A read at location 0018 also clears the Counter A Underflow Flag (IFR4).

The 16-bit latch contains the counter initialization value, and can be loaded at any time by executing a write to the Upper Latch A at location 0019 and the Lower Latch A at location 0018. In either case, the contents of the accumulator are copied into the applicable latch register.

Counter A can be started at any time by writing to address: 001A. The contents of the accumulator will be copied into the Upper Latch A before the contents of the 16-bit latch are transferred to Counter A. Counter A is set to the latch value whenever Counter A underflows. When Counter A decrements from 0000 the next counter value will be the latch value, not FFFF, and the Counter A Underflow Flag (IFR 4) will be set to "1". This bit may be cleared by reading the Lower Counter A at location 0018, by writing to address location 001A, or by $\overline{RES}$.

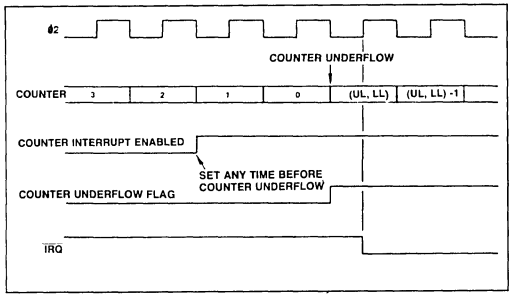


Figure 6-1. Interval Timer Timing Diagram

Counter A operates in any of four modes. These modes are selected by the Counter A Mode Control bits in the Control Register.

MCR1 (bit 1)	MCR0 (bit 0)	Mode
0	0	Interval Timer
0	1	Pulse Generation
1	0	Event Counter
1	1	Pulse Width Measurement

The Interval Timer, Pulse Generation, and Pulse Width Measurement Modes are ϕ2 clock counter modes. The Event Counter Mode counts the occurrences of an external event on the CNTR line.

The Counter is set to the Interval Timer Mode (00) when a $\overline{RES}$ signal is generated.

6.1.1 Interval Timer

In the Interval Timer mode the Counter is initialized to the Latch value by either of two conditions:

1. When the Counter is decremented from 0000, the next Counter value is the Latch value (not FFFF).

2. When a write operation is performed to the Load Upper Latch and Transfer Latch to Counter address 001A, the Counter is loaded with the Latch value. Note that the contents of the Accumulator are loaded into the Upper Latch before the Latch value is transferred to the Counter.

The Counter value is decremented by one count at the ϕ2 clock rate. The 16-bit Counter can hold from 1 to 65535 counts. The Counter Timer capacity is therefore 1 μs to 65.535 ms at the 1 MHz ϕ2 clock rate or 0.5 μs to 32.767 ms at the 2 MHz ϕ2 clock rate. Time intervals greater than the maximum Counter value can be easily measured by counting $\overline{IRQ}$ interrupt requests in the counter $\overline{IRQ}$ interrupt routine.

When Counter A decrements from 0000, the Counter A Underflow (IFR4) is set to logic 1. If the Counter A Interrupt Enable Bit (IER4) is also set, an $\overline{IRQ}$ interrupt request will be generated. The Counter A Underflow bit in the Interrupt Flag Register can be examined in the $\overline{IRQ}$ interrupt routine to determine that the $\overline{IRQ}$ was generated by the Counter A Underflow.

While the timer is operating in the Interval Timer Mode, PA4 operates as a PA I/O bit.

A timing diagram of the Interval Timer Mode is shown in Figure 6-1.

6.1.2 Pulse Generation Mode

In the Pulse Generation mode, the CA line operates as a Counter Output. The line toggles from low to high or from high to low whenever a Counter A Underflow occurs, or a write is performed to address 001A.

The normal output waveform is a symmetrical square-wave. The CA output is initialized high when entering the mode and transitions low when writing to 001A.

Asymmetric waveforms can be generated if the value of the latch is changed after each counter underflow.

A one-shot waveform can be generated by changing from Pulse Generation to Interval Timer mode after only one occurrence of the output toggle condition.

6.1.3 Event Counter Mode

In this mode the CA is used as an Event Input line, and the Counter will decrement with each rising edge detected on this line. The maximum rate at which this edge can be detected is one-half the ϕ2 clock rate.

The Counter can count up to 65,535 occurrences before underflowing. As in the other modes, the Counter A Underflow bit (IER4) is set to logic 1 if the underflow occurs.

Figure 6.2 is a timing diagram of the Event Counter Mode.

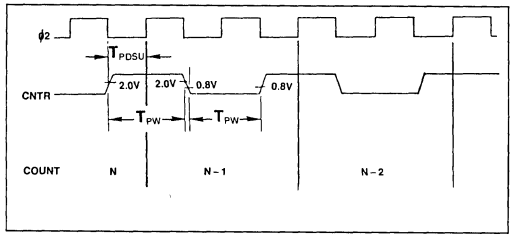


Figure 6-2. Event Counter Mode

6.1.4 Pulse Width Measurement Mode

This mode allows the accurate measurement of a low pulse duration on the CA line. The Counter decrements by one count at the ϕ2 clock rate as long as the CA line is held in the low state. The Counter is stopped when CA is in the high state.

The Counter A underflow flag will be set only when the count in the timer reaches zero. Upon reaching zero the timer will be loaded with the latch value and continue counting down as long as the CA pin is held low. After the counter is stopped by a high level on CA, the count will hold as long as CA remains high. Any further low levels on CA will again cause the counter to count down from its present value. The state of the CA line can be determined by testing the state of PA4.

A timing diagram for the Pulse Width Measurement Mode is shown in Figure 6.3.

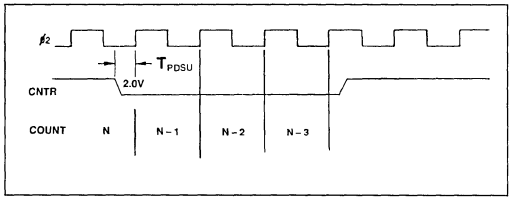


Figure 6-3. Pulse Width Measurement

6.1.5 Serial I/O Data Rate Generation

Counter A also provides clock timing for the Serial I/O which establishes the data rate for the Serial I/O port. When the Serial I/O is enabled, Counter A is forced to operate at the internal clock rate. Counter A is not required for the RCVR S/R mode. The Counter I/O (PA4) may also be required to support the Serial I/O (see Table 4-2).

Table 6-1 identifies the values to be loaded in Counter A for selecting standard data rates with a ϕ2 clock rate of 1 MHz and 2 MHz. Although Table 6-1 identifies only the more common data rates, any data rate from 1 to 62.5K bps can be selected by using the formula:

$$N = \frac{\phi 2}{16 \times bps} - 1$$

where

- N = decimal value to be loaded into Counter A using its hexadecimal equivalent.
- ϕ2 = the clock frequency (1 MHz or 2 MHz)
- bps = the desired data rate.

NOTE

In Table 6-1 you will notice that the standard data rate and the actual data rate may be slightly different. Transmitter and receiver errors of 1.5% or less are acceptable. A revised clock rate is included in Table 6-1 for those baud rates which fall outside this limit.

Table 6-1. Counter A Values for Baud Rate Selection

Standard Baud Rate	Hexadecimal Value		Actual Baud Rate At		Clock Rate Needed To Get Standard Baud Rate	
	1 MHz	2 MHz	1 MHz	2 MHz	1 MHz	2 MHz
50	04E1	09C3	50.00	50.00	1.0000	2.0000
75	0340	0682	75.03	74.99	1.0000	2.0000
110	0237	046F	110.04	110.04	1.0000	2.0000
150	01A0	0340	149.88	150.06	1.0000	2.0000
300	00CF	01A0	300.48	299.76	1.0000	2.0000
600	0067	00CF	600.96	600.96	1.0000	2.0000
1200	0033	0067	1201.92	1201.92	1.0000	2.0000
2400	0019	0033	2403.85	2403.85	1.0000	2.0000
3600	0010	0021	3676.47	3676.47	0.9792	1.9584
4800	000C	0019	4807.69	4807.69	1.0000	2.0000
7200	0008	0010	6944.44	7352.94	1.0368	1.9584
9600	0006	000C	8928.57	9615.38	1.0752	2.0000

6.2 COUNTER B

Counter B consists of a 16-bit counter and two 16-bit latches organized as follows: Lower Counter B (LCB), Upper Counter B (UCB), Lower Latch B (LLB), Upper Latch B (ULB), Lower Latch C (LLC), and Upper Latch C (ULC). Latch C is used only in the asymmetrical pulse generation mode. The counter contains the count of either Ø2 clock pulses or external events depending on the counter mode selected. The contents of Counter B may be read any time by executing a read at location 001D for the Upper Counter B and at location 001E or 001C for the Lower Counter B. A read at location 001C also clears the Counter B Underflow Flag.

Latch B contains the counter initialization value, and can be loaded at any time by executing a write to the Upper Latch B at location 001D and the Lower Latch B at location 001C. In each case, the contents of the accumulator are copied into the applicable latch register.

Counter B can be initialized at any time by writing to address: 001E. The contents of the accumulator is copied into the Upper Latch B before the value in the 16-bit Latch B is transferred to Counter B. Counter B will also be set to the latch value and the Counter B Underflow Flag bit (IFR5) will be set to a "1" whenever Counter B underflows by decrementing from 0000.

IFR 5 may be cleared by reading the Lower Counter B at location 001C, by writing to address location 001E, or by $\overline{RES}$.

Counter B operates in the same manner as Counter A in the Interval Timer and Event Counter modes. The Pulse Width Measurement Mode is replaced by the Retriggerable Interval Timer mode and the Pulse Generation mode is replaced by the Asymmetrical Pulse Generation Mode.

6.2.1 Retriggerable Interval Timer Mode

When operating in the Retriggerable Interval Timer mode, Counter B is initialized to the latch value by writing to address 001E, by a Counter B underflow, or whenever a positive edge occurs on the CB pin (PA5). The Counter B interrupt flag will be set if the counter underflows before a positive edge occurs on the CB line. Figure 6-4 illustrates the operation.

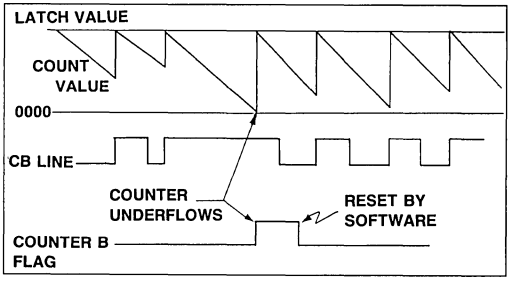


Figure 6-4. Counter B Retriggerable Interval Timer Mode

6.2.2 Asymmetrical Pulse Generation Mode

Counter B has a special Asymmetrical Pulse Generation Mode whereby a pulse train with programmable pulse width and period can be generated without the processor intervention once the latch values are initialized.

In this mode, the 16-bit Latch B is initialized with a value which corresponds to the duration between pulses (referred to as D in the following descriptions). The 16-bit Latch C is initialized with a value which corresponds to the desired pulse width (referred to as P in the following descriptions). The initialization sequence for Latch B and C and the starting of a counting sequence are as follows:

1. The lower 8 bits of P are loaded into LLB by writing to address 001C, and the upper 8 bits of P are loaded into ULB and the full 16 bits are transferred to Latch C by writing to address location 001D. At this point both Latch B and Latch C contain the value of P.

2. The lower 8 bits of D are loaded into LLB by writing to address 001C, and the upper 8 bits of D are loaded into ULB by writing to address location 001E. Writing to address location 001E also causes the contents of the 16-bit Latch B to be downloaded into the Counter B and causes the CB output to go low as shown in Figure 6-5.

3. When the Counter B underflow occurs the contents of the Latch C is loaded into the Counter B, and the CB output toggles to a high level and stays high until another underflow occurs. Latch B is then down-loaded and the CB output toggles to a low level repeating the whole process.

SECTION 7
POWER ON/INITIALIZATION CONSIDERATIONS

7.1 POWER-ON TIMING

After applications of V_{CC} and V_{RR} power to the device, $\overline{RES}$ must be held low for at least eight Ø2 clock cycles after V_{CC} reaches operating range and the interal oscillator has stabilized. This stabilization time is dependent upon the input V_{CC} voltage and performance of the internal oscillator. The clock can be monitored at Ø2 (pin 3). Figure 7-1 illustrates the power turn-on waveforms. Clock stabilization time is typically 20 ms.

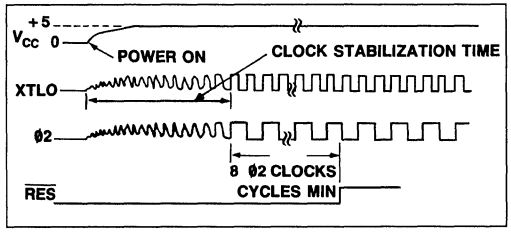


Figure 7-1. Power Turn-on Timing Detail

7.2 POWER-ON RESET

The occurrence of $\overline{RES}$ going from low to high will cause the device to set the Interrupt Mask Bit — bit 2 of the Processor Status Register — and initiate a reset vector fetch at address FFFC and FFFD to begin user program execution. All of the I/O ports (PA, PB, PC, PD) will be forced to the high (logic 1) state. All bits of the Control Register will be cleared to logic 0 causing the Interval Timers counter mode (mode 00) to be selected and causing all interrupt enabled bits to be reset.

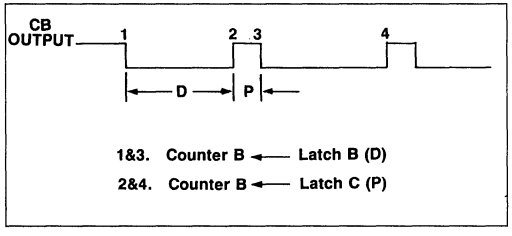


Figure 6-5. Counter B Pulse Generation

7.3 RESET ($\overline{RES}$) CONDITIONING

When $\overline{RES}$ is driven from low to high the device is put in a reset state causing the registers and I/O ports to be configured as shown in Table 7-1. All RAM and other CPU registers will initialize in a random, non-repeatable data pattern.

Table 7.1 $\overline{RES}$ Initialization of I/O Ports and Registers

	Add. (Hex.)	Bit No. 7	6	5	4	3	2	1	0
Registers									
Processor Status	—	—	—	—	—	—	1	—	—
Int. Flag (IFR)	11	0	0	0	0	0	0	0	0
Int. Enable (IER)	12	0	0	0	0	0	0	0	0
Mode Control (MCR)	14	0	0	0	0	0	0	0	0
Ser. Com. Control (SCCR)	15	0	0	0	0	0	0	0	0
Ser. Com. Status (SCSR)	16	0	1	0	0	0	0	0	0
Ports									
PA Latch	0	1	1	1	1	1	1	1	1
PB Latch	1	1	1	1	1	1	1	1	1
PC Latch	2	1	1	1	1	1	1	1	1
PD Latch	3	1	1	1	1	1	1	1	1

7.4 INITIALIZATION

Any initialization process for the device should include a $\overline{RES}$, as indicated in the preceding paragraphs. After stabilization of the internal clock (if a power on situation) an initialization subroutine should be executed to perform (as a minimum) the following functions:

1. The Stack Pointer should be set
2. Clear or Set Decimal Mode
3. Set or Clear Carry Flag
4. Set up Mode Controls as required
5. Clear Interrupts

A typical initialization subroutine could be as follows:

LDX	Load stack pointer starting address into X Register
TXS	Transfer X Register value to Stack Pointer
CLD	Clear Decimal Mode
SEC	Set Carry Flag
. . . .	Set-up Mode Control and
. . . .	special function
. . . .	registers as required
CLI	Clear Interrupts

APPENDIX A
ENHANCED R6502 INSTRUCTION SET

This appendix summarizes the R6500/11. R6500/12 and R6500/15 instruction set. For detailed information, consult the R6500 Microcomputer System Programming Manual (Order No. 202). Four new bit access instructions are added to enhance the standard 6502 instruction set.

Table A.1 R6500/11, R6500/12 and R6500/15 Instruction Set in Alphabetic Sequence

Mnemonic	Instruction	Mnemonic	Instruction
ADC	Add Memory to Accumulator with Carry	LDA	Load Accumulator with Memory
AND	"AND" Memory with Accumulator	LDX	Load Index X with Memory
ASL	Shift Left One Bit (Memory or Accumulator)	LDY	Load Index Y with Memory
		LSR	Shift One Bit Right (Memory or Accumulator)
*BBR	Branch on Bit Reset Relative		
*BBS	Branch on Bit Set Relative		
BCC	Branch on Carry Clear	NOP	No Operation
BCS	Branch on Carry Set		
BEQ	Branch on Result Zero	ORA	"OR" Memory with Accumulator
BIT	Test Bits in Memory with Accumulator		
BMI	Branch on Result Minus	PHA	Push Accumulator on Stack
BNE	Branch on Result not Zero	PHP	Push Processor Status on Stack
BPL	Branch on Result Plus	PLA	Pull Accumulator from Stack
BRK	Force Break	PLP	Pull Processor Status from Stack
BVC	Branch on Overflow Clear		
BVS	Branch on Overflow Set	*RMB	Reset Memory Bit
		ROL	Rotate One Bit Left (Memory or Accumulator)
CLC	Clear Carry Flag		
CLD	Clear Decimal Mode	ROR	Rotate One Bit Right (Memory or Accumulator)
CLI	Clear Interrupt Disable Bit		
CLV	Clear Overflow Flag	RTI	Return from Interrupt
CMP	Compare Memory and Accumulator	RTS	Return from Subroutine
CPX	Compare Memory and Index X		
CPY	Compare Memory and Index Y	SBC	Subtract Memory from Accumulator with Borrow
DEC	Decrement Memory by One	SEC	Set Carry Flag
DEX	Decrement Index X by One	SED	Set Decimal Mode
DEY	Decrement Index Y by One	SEI	Set Interrupt Disable Status
		*SMB	Set Memory Bit
EOR	"Exclusive-Or" Memory with Accumulator	STA	Store Accumulator in Memory
		STX	Store Index X in Memory
		STY	Store Index Y in Memory
INC	Increment Memory by One		
INX	Increment Index X by One	TAX	Transfer Accumulator to Index X
INY	Increment Index X by One	TAY	Transfer Accumulator to Index Y
		TSX	Transfer Stack Pointer to Index X
JMP	Jump to New Location	TXA	Transfer Index X to Accumulator
JSR	Jump to New Location Saving Return Address	TXS	Transfer Index X to Stack Register
		TYA	Transfer Index Y to Accumulator

Notes:
* Instructions added to this standard 6502 instruction set.

Table A.2 R6500/11, R6500/12 and R6500/15 Instruction Set Summary

INSTRUCTIONS		IMMEDIATE			ABSOLUTE			ZERO PAGE			ACCUM.			IMPLIED		
MNEMONIC	OPERATION	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#
ADC	A · M · C→A (4)(1)	69	2	2	6D	4	3	65	3	2						
AND	A M→A (1)	29	2	2	2D	4	3	25	3	2						
ASL	C← [7 0] ←0				0E	6	3	06	5	2	0A	2	1			
BBR[#(0-7)]	Branch on M_6=0 (5)(2)															
BBS[#(0-7)]	Branch on M_6=1 (5)(2)															
BCC	Branch on C=0 (2)															
BCS	Branch on C=1 (2)															
BEQ	Branch on Z=1 (2)															
BIT	A∧M				2C	4	3	24	3	2						
BMI	Branch on N=1 (2)															
BNE	Branch on Z=0 (2)															
BPL	Branch on N=0 (2)															
BRK	Break													00	7	1
BVC	Branch on V=0 (2)															
BVS	Branch on V=1 (2)															
CLC	0→C													18	2	1
CLD	0→D													D8	2	1
CLI	0→I													58	2	1
CLV	0→V													B8	2	1
CMP	A M (1)	C9	2	2	CD	4	3	C5	3	2						
CPX	X M	E0	2	2	EC	4	3	E4	3	2						
CPY	Y M	C0	2	2	CC	4	3	C4	3	2						
DEC	M 1→M				CE	6	3	C6	5	2						
DEX	X 1→X													CA	2	1
DEY	Y 1→Y													88	2	1
EOR	A∀M→A (1)	49	2	2	4D	4	3	45	3	2						
INC	M 1→M				EE	6	3	E6								
INX	X · 1→X													EB	2	1
INY	Y · 1→Y													C8	2	1
JMP	Jump to New Loc				4C	3	3									
JSR	Jump Sub				20	6	3									
LDA	M→A (1)	A9	2	2	AD	4	3	A5	3	2						
LDX	M→X (1)	A2	2	2	AE	4	3	A6	3	2						
LDY	M→Y (1)	A0	2	2	AC	4	3	A4	3	2						
LSR	0→ [7 0] →C				4E	6	3	46	5	2	4A	2	1			
NOP	No Operation													EA	2	1
ORA	AVM→A (1)	09	2	2	0D	4	3	05	3	2						
PHA	A→Ms S 1→S													48	3	1
PHP	P→Ms S 1→S													08	3	1
PLA	S 1→S Ms→A													68	4	1
PLP	S · 1→S Ms→P													28	4	1
RMB[#(0-7)]	0→M_b (5)															
ROL	[7 0] ← [C] (rotate)				2E	6	3	26	5	2	2A	2	1			
ROR	[C] → [7 0] (rotate)				6E	6	3	66	5	2	6A	2	1			
RTI	Rtrn Int													40	6	1
RTS	Rtrn Sub													60	6	1
SBC	A M C→A (1)	E9	2	2	ED	4	3	E5	3	2						
SEC	1→C													38	2	1
SED	1→D													F8	2	1
SEI	1→T													78	2	1
SMB[#(0-7)]	1→M_b (5)															
STA	A→M				8D	4	3	85	3	2						
STX	X→M				8E	4	3	86	3	2						
STY	Y→M				8C	4	3	84	3	2						
TAX	A→X													AA	2	1
TAY	A→Y													A8	2	1
TSX	S→X													BA	2	1
TXA	X→A													8A	2	1
TXS	X→S													9A	2	1
TYA	Y→A													98	2	1

MNEMONIC	(IND, X)			(IND), Y			Z. PAGE, X			ABS, X			ABS, Y			RELATIVE			INDIRECT			Z. PAGE, Y		
	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#
ADC	61	6	2	71	5	2	75	4	2	7D	4	3	79	4	3									
AND	21	6	2	31	5	2	35	4	2	3D	4	3	39	4	3									
ASL							16	6	2	1E	7	3												
BBR[#(0-7)]																								
BBS[#(0-7)]																								
BCC																90	2	2						
BCS																B0	2	2						
BEQ																F0	2	2						
BIT																								
BMI																30	2	2						
BNE																D0	2	2						
BPL																10	2	2						
BRK																								
BVC																50	2	2						
BVS																70	2	2						
CLC																								
CLD																								
CLI																								
CLV																								
CMP	C1	6	2	D1	5	2	D5	4	2	DD	4	3	D9	4	3									
CPX																								
CPY																								
DEC							D6	6	2	DE	7	3												
DEX																								
DEY																								
EOR	41	6	2	51	5	2	55	4	2	5D	4	3	59	4	3									
INC							F6	6	2	FE	7	3												
INX																								
INY																								
JMP																			6C	5	3			
JSR																								
LDA	A1	6	2	B1	5	2	B5	4	2	BD	4	3	B9	4	3									
LDX													BE	4	3							B6	4	2
LDY							B4	4	2	BC	4	3												
LSR							56	6	2	5E	7	3												
NOP																								
ORA	01	6	2	11	5	2	15	4	2	1D	4	3	19	4	3									
PHA																								
PHP																								
PLA																								
PLP																								
RMB[#(0-7)]																								
ROL							36	6	2	3E	7	3												
ROR							76	6	2	7E	7	3												
RTI																								
RTS																								
SBC	E1	6	2	F1	5	2	F5	4	2	FD	4	3	F9	4	3									
SEC																								
SED																								
SEI																								
SMB[#(0-7)]																								
STA	81	6	2	91	6	2	95	4	2	9D	5	3	[illegible]	5	3									
STX																						96	4	2
STY							94	4	2															
TAX																								
TAY																								
TSX																								
TXA																								
TXS																								
TYA																								

MNEMONIC	BIT ADDRESSING (OP BY BIT #)								PROCESSOR STATUS CODES							
									7	6	5	4	3	2	1	0
	0	1	2	3	4	5	6	7	N	V	•	B	D	I	Z	C
ADC									N	V	•	•	•	•	Z	C
AND									N	•	•	•	•	•	Z	•
ASL									N	•	•	•	•	•	Z	C
BBR[#(0-7)]	0F	1F	2F	3F	4F	5F	6F	7F	•	•	•	•	•	•	•	•
BBS[#(0-7)]	8F	9F	AF	BF	CF	DF	EF	FF	•	•	•	•	•	•	•	•
BCC									•	•	•	•	•	•	•	•
BCS									•	•	•	•	•	•	•	•
BEQ									•	•	•	•	•	•	•	•
BIT									M_7	M_6	•	•	•	•	Z	•
BMI									•	•	•	•	•	•	•	•
BNE									•	•	•	•	•	•	•	•
BPL									•	•	•	•	•	•	•	•
BRK									•	•	•	1	•	1	•	•
BVC									•	•	•	•	•	•	•	•
BVS									•	•	•	•	•	•	•	•
CLC									•	•	•	•	•	•	•	0
CLD									•	•	•	•	0	•	•	•
CLI									•	•	•	•	•	0	•	•
CLV									•	0	•	•	•	•	•	•
CMP									N	•	•	•	•	•	Z	C
CPX									N	•	•	•	•	•	Z	C
CPY									N	•	•	•	•	•	Z	C
DEC									N	•	•	•	•	•	Z	•
DEX									N	•	•	•	•	•	Z	•
DEY									N	•	•	•	•	•	Z	•
EOR									N	•	•	•	•	•	Z	•
INC									N	•	•	•	•	•	Z	•
INX									N	•	•	•	•	•	Z	•
INY									N	•	•	•	•	•	Z	•
JMP									•	•	•	•	•	•	•	•
JSR									•	•	•	•	•	•	•	•
LDA									N	•	•	•	•	•	Z	•
LDX									N	•	•	•	•	•	Z	•
LDY									N	•	•	•	•	•	Z	•
LSR									0	•	•	•	•	•	Z	C
NOP									•	•	•	•	•	•	•	•
ORA									N	•	•	•	•	•	Z	•
PHA									•	•	•	•	•	•	•	•
PHP									•	•	•	•	•	•	•	•
PLA									N	•	•	•	•	•	Z	•
PLP									(Restored)							
RMB[#(0-7)]	07	17	27	37	47	57	67	77	•	•	•	•	•	•	•	•
ROL									N	•	•	•	•	•	Z	C
ROR									N	•	•	•	•	•	Z	C
RTI									(Restored)							
RTS									•	•	•	•	•	•	•	•
SBC									N	V	•	•	•	•	Z	(3)
SEC									•	•	•	•	•	•	•	1
SED									•	•	•	•	1	•	•	•
SEI									•	•	•	•	•	1	•	•
SMB[#(0-7)]	87	97	A7	B7	C7	D7	E7	F7	•	•	•	•	•	•	•	•
STA									•	•	•	•	•	•	•	•
STX									•	•	•	•	•	•	•	•
STY									•	•	•	•	•	•	•	•
TAX									N	•	•	•	•	•	Z	•
TAY									N	•	•	•	•	•	Z	•
TSX									N	•	•	•	•	•	Z	•
TXA									N	•	•	•	•	•	Z	•
TXS									•	•	•	•	•	•	•	•
TYA									N	•	•	•	•	•	Z	•

NOTES

1. Add 1 to N if page boundary is crossed
2. Add 1 to N if branch occurs to same page
   Add 2 to N if branch occurs to different page
3. Carry not = Borrow
4. If in decimal mode Z flag is invalid
   accumulator must be checked on zero result
5. Effects 8-bit data field of the specified zero page address

LEGEND

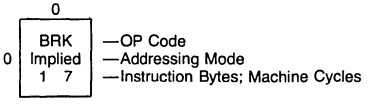
X = Index X
Y = Index Y
A = Accumulator
M = Memory per effective address
M_s = Memory per stack pointer
M_b = Selecter zero page memory bit
M_7 = Memory Bit 7
M_6 = Memory Bit 6
• = Add
– = Subtract
∧ = And
V = Or
∀ = Exclusive Or
n = Number of cycles
# = Number of Bytes

Table A.3 R6500/11, R6500/12 and R6500/15 Instruction Operation Code Matrix

MSD	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	MSD
	LSD																
0	BRK Implied 1 7	ORA (IND, X) 2 6				ORA ZP 2 3	ASL ZP 2 5	RMB0 ZP 2 5	PHP Implied 1 3	ORA IMM 2 2	ASL Accum 1 2			ORA ABS 3 4	ASL ABS 3 6	BBR0 ZP 3 5**	0
1	BPL Relative 2 2**	ORA (IND), Y 2 5*				ORA ZP, X 2 4	ASL ZP, X 2 6	RMB1 ZP 2 5	CLC Implied 1 2	ORA ABS, Y 3 4*				ORA ABS, X 3 4*	ASL ABS, X 3 7	BBR1 ZP 3 5**	1
2	JSR Absolute 3 6	AND (IND, X) 2 6			BIT ZP 2 3	AND ZP 2 3	ROL ZP 2 5	RMB2 ZP 2 5	PLP Implied 1 4	AND IMM 2 2	ROL Accum 1 2		BIT ABS 3 4	AND ABS 3 4	ROL ABS 3 6	BBR2 ZP 3 5**	2
3	BMI Relative 2 2**	AND (IND, Y) 2 5*				AND ZP, X 2 4	ROL ZP, X 2 6	RMB3 ZP 2 5	SEC Implied 1 2	AND ABS, Y 3 4*				AND ABS, X 3 4*	ROL ABS, X 3 7	BBR3 ZP 3 5**	3
4	RTI Implied 1 6	EOR (IND, X) 2 6				EOR ZP 2 3	LSR ZP 2 5	RMB4 ZP 2 5	PHA Implied 1 3	EOR IMM 2 2	LSR Accum 1 2		JMP ABS 3 3	EOR ABS 3 4	LSR ABS 3 6	BBR4 ZP 3 5**	4
5	BVC Relative 2 2**	EOR (IND), Y 2 5*				EOR ZP, X 2 4	LSR ZP, X 2 6	RMB5 ZP 2 5	CLI Implied 1 2	EOR ABS, Y 3 4*				EOR ABS, X 3 4*	LSR ABS, X 3 7	BBR5 ZP 3 5**	5
6	RTS Implied 1 6	ADC (IND, X) 2 6				ADC ZP 2 3	ROR ZP 2 5	RMB6 ZP 2 5	PLA Implied 1 4	ADC IMM 2 2	ROR Accum 1 2		JMP Indirect 3 5	ADC ABS 3 4	ROR ABS 3 6	BBR6 ZP 3 5**	6
7	BVS Relative 2 2**	ADC (IND, Y) 2 5*				ADC ZP, X 2 4	ROR ZP, X 2 6	RMB7 ZP 2 5	SEI Implied 1 2	ADC ABS, Y 3 4*				ADC ABS, X 3 4*	ROR ABS, X 3 7	BBR7 ZP 3 5**	7
8		STA (IND, X) 2 6			STY ZP 2 3	STA ZP 2 3	STX ZP 2 3	SMB0 ZP 2 5	DEY Implied 1 2		TXA Implied 1 2		STY ABS 3 4	STA ABS 3 4	STX ABS 3 4	BBS0 ZP 3 5**	8
9	BCC Relative 2 2**	STA (IND, Y) 2 6			STY ZP, X 2 4	STA ZP, X 2 4	STX ZP, Y 2 4	SMB1 ZP 2 5	TYA Implied 1 2	STA ABS, Y 3 5	TXS Implied 1 2			STA ABS, X 3 5		BBS1 ZP 3 5**	9
A	LDY IMM 2 2	LDA (IND, X) 2 6	LDX IMM 2 2		LDY ZP 2 3	LDA ZP 2 3	LDX ZP 2 3	SMB2 ZP 2 5	TAY Implied 1 2	LDA IMM 2 2	TAX Implied 1 2		LDY ABS 3 4	LDA ABS 3 4	LDX ABS 3 4	BBS2 ZP 3 5**	A
B	BCS Relative 2 2**	LDA (IND), Y 2 5*			LDY ZP, X 2 4	LDA ZP, X 2 4	LDX ZP, Y 2 4	SMB3 ZP 2 5	CLV Implied 1 2	LDA ABS, Y 3 4*	TSX Implied 1 2		LDY ABS, X 3 4*	LDA ABS, X 3 4*	LDX ABS, Y 3 4*	BBS3 ZP 3 5**	B
C	CPY IMM 2 2	CMP (IND, X) 2 6			CPY ZP 2 3	CMP ZP 2 3	DEC ZP 2 5	SMB4 ZP 2 5	INY Implied 1 2	CMP IMM 2 2	DEX Implied 1 2		CPY ABS 3 4	CMP ABS 3 4	DEC ABS 3 6	BBS4 ZP 3 5**	C
D	BNE Relative 2 2**	CMP (IND), Y 2 5*				CMP ZP, X 2 4	DEC ZP, X 2 6	SMB5 ZP 2 5	CLD Implied 1 2	CMP ABS, Y 3 4*				CMP ABS, X 3 4*	DEC ABS, X 3 7	BBS5 ZP 3 5**	D
E	CPX IMM 2 2	SBC (IND, X) 2 6			CPX ZP 2 3	SBC ZP 2 3	INC ZP 2 5	SMB6 ZP 2 5	INX Implied 1 2	SBC IMM 2 2	NOP Implied 1 2		CPX ABS 3 4	SBC ABS 3 4	INC ABS 3 6	BBS6 ZP 3 5**	E
F	BEQ Relative 2 2**	SBC (IND), Y 2 5*				SBC ZP, X 2 4	INC ZP, X 2 6	SMB7 ZP 2 5	SED Implied 1 2	SBC ABS, Y 3 4*				SBC ABS, X 3 4*	INC ABS, X 3 7	BBS7 ZP 3 5**	F
	0	1	2	3	4	5	6	7 LSD	8	9	A	B	C	D	E	F	

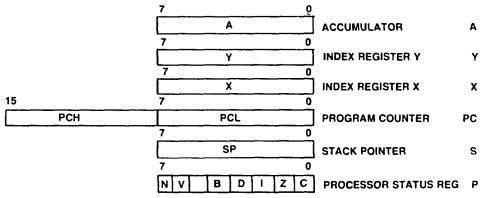
MSD = Most Significant Digit
LSD = Least Significant Digit

*Add 1 to N if page boundary is crossed.
**Add 1 to N if branch occurs to same page;
add 2 to N if branch occurs to different page.

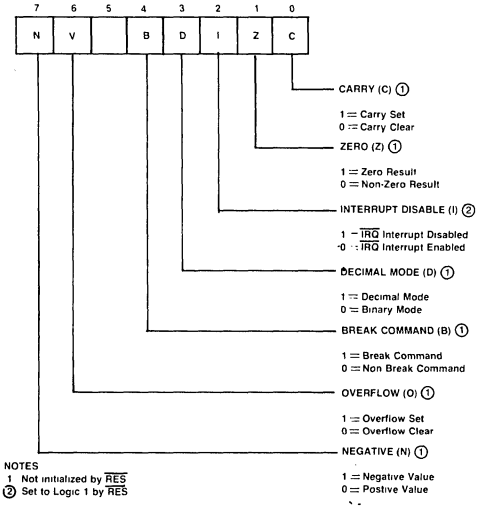


3

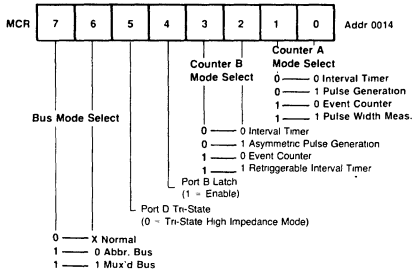
APPENDIX B
KEY REGISTER SUMMARY



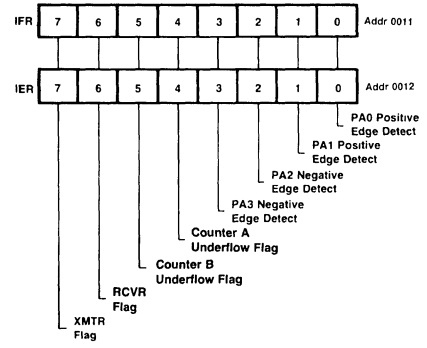
CPU Registers



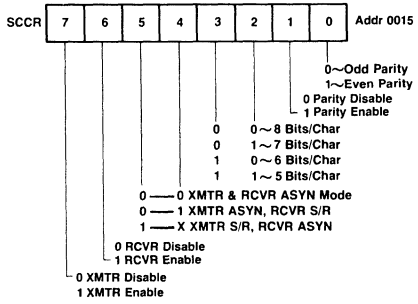
Processor Status Register



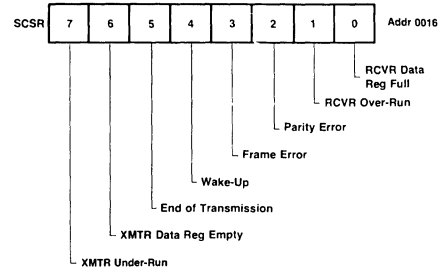
Mode Control Register



Interrupt Enable and Flag Registers



Serial Communications Control Register



Serial Communications Status Register

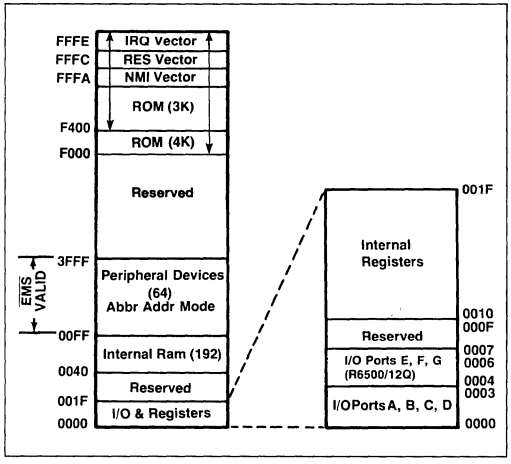
APPENDIX C
ADDRESS ASSIGNMENTS/MEMORY MAPS/PIN FUNCTIONS

C.1 I/O AND INTERNAL REGISTER ADDRESSES

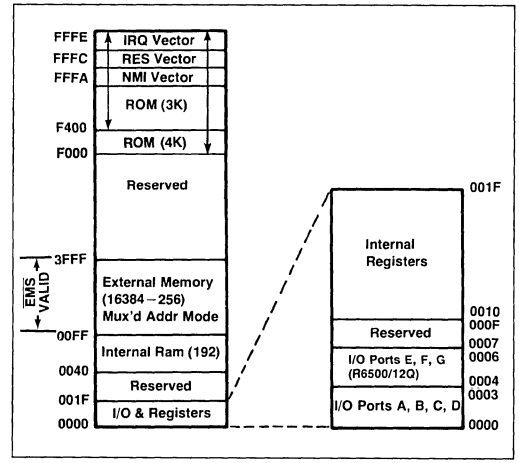
ADDRESS (HEX)	READ	WRITE
001F	— —	— —
1E	Lower Counter B	Upper Latch B, Cntr B←Latch B, CLR Flag
1D	Upper Counter B	Upper Latch B, Latch C←Latch B
1C	Lower Counter B, CLR Flag	Lower Latch B.
1B	— —	— —
1A	Lower Counter A	Upper Latch A, Cntr A←Latch A, CLR Flag
19	Upper Counter A	Upper Latch A
18	Lower Counter A, CLR Flag	Lower Latch A
17	Serial Receiver Data Register	Serial Transmitter Data Register
16	Serial Comm. Status Register	Serial Comm. Status Reg. Bits 4 & 5 only
15	Serial Comm. Control Register	Serial Comm. Control Register
14	Mode Control Register	Mode Control Register
13	— —	— —
12	Interrupt Enable Register	Interrupt Enable Register
11	Interrupt Flag Register	— —
0010	Read FF	Clear Int Flag (Bits 0-3 only, Write 0's only)
0F	— —	— —
0E	— —	— —
0D	— —	— —
0C	— —	— —
0B	— —	— —
0A	— —	— —
09	— —	— —
08	— —	— —
07	— —	— —
06	Port G*	Port G*
05	Port F*	Port F*
04	Port E*	Port E*
03	Port D	Port D
02	Port C	Port C
01	Port B	Port B
0000	Port A	Port A

NOTE *R6500/12Q only.

C.2 ABBREVIATED MODE MEMORY MAP



C.3 MULTIPLEXED MODE MEMORY MAP



C.4 MULTIPLE FUNCTION PIN ASSIGNMENTS—PORT C AND PORT D

PIN NUMBER	I/O PORT FUNCTION	ABBREVIATED PORT FUNCTION	MULTIPLEXED PORT FUNCTION
4	PC0	A0	A0
5	PC1	A1	A1
6	PC2	A2	A2
7	PC3	A3	A3
8	PC4	A12	A12
9	PC5	R/$\overline{W}$	R/$\overline{W}$
10	PC6	A13	A13
11	PC7	$\overline{EMS}$	$\overline{EMS}$
19	PD0	D0	A4/D0
18	PD1	D1	A5/D1
17	PD2	D2	A6/D2
16	PD3	D3	A7/D3
15	PD4	D4	A8/D4
14	PD5	D5	A9/D5
13	PD6	D6	A10/D6
12	PD7	D7	A11/D7

APPENDIX D
ELECTRICAL SPECIFICATIONS

MAXIMUM RATINGS*

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC} & V_{RR}	−0.3 to +7.0	Vdc
Input Voltage	V_{IN}	−0.3 to +7.0	Vdc
Operating Temperature Commercial Industrial	T_A	T_L to T_H 0 to +70 −40 to +85	°C
Storage Temperature	T_{STG}	−55 to +150	°C

***NOTE:** Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in other sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

3

DC CHARACTERISTICS

(V_{CC} = 5.0V ±5%, V_{RR} = V_{CC}; V_{SS} = 0V; T_A = 0° to 70°, unless otherwise specified)

Parameter	Symbol	Min.	Typ.[1]	Max.	Unit	Test Conditions
RAM Standby Voltage (Retention Mode)	V_{RR}	3.0		V_{CC}	V	
RAM Standby Current (Retention Mode) Commercial Industrial	I_{RR}	 — —	 4 5.2	 — —	mA	T_A = 25°C
Input High Voltage All Except XTLI and ϕ2 in Slave Option XTLI and ϕ2 in Slave Option	V_{IH}	 +2.0 +4.0	 — —	 V_{CC} V_{CC}	V	
Input Low Voltage	V_{IL}	−0.3	—	+0.8	V	
Input Leakage Current $\overline{RES}$, $\overline{NMI}$	I_{IN}	—	—	±10.0	μA	V_{IN} = 0 to 5.0V
Input Low Current PA, PB, PC, PD, PF[3], and PG[3]	I_{IL}	—	−1.0	−1.6	mA	V_{IL} = 0.4 V
Output High Voltage (Except XTLO)	V_{OH}	+2.4	—	V_{CC}	V	I_{LOAD} = −100 μA
Darlington Current Drive, PE[3]	I_{OH}	−1.0	—	—	mA	V_{OH} = 1.5V
Output Low Voltage	V_{OL}	—	—	+0.4	V	I_{LOAD} = 1.6 mA
I/O Port Pull-Up Resistance PA0 – PA7, PB0 – PB7, PC0 – PC7, PF0 – PF7[3] & PG0 – PG7[3]	R_L	3.0	6.0	11.5	Kohm	
Output Leakage Current (Three-State Off)	I_{OUT}	—	—	±10	μA	
Input Capacitance XTLI, XTLO PA, PB, PC, PD, PF[3], PG[3]	C_{IN}	 — —	 — —	 50 10	pF	T_A = 25°C V_{IN} = 0V f = 1.0 MHz
Output Capacitance (Three-State Off)	C_{OUT}	—	—	10	pF	T_A = 25°C V_{IN} = 0V f = 1.0 MHz
Power Dissipation (Outputs High)	P_D	—	—	1000	mW	T_A = 0°C

Notes:
1. Typical values measured at T_A = 25°C and V_{CC} = 5.0V.
2. Negative sign indicates outward current flow, positive indicates inward flow.
3. R6500/12Q only.

APPENDIX E
TIMING REQUIREMENTS AND CHARACTERISTICS

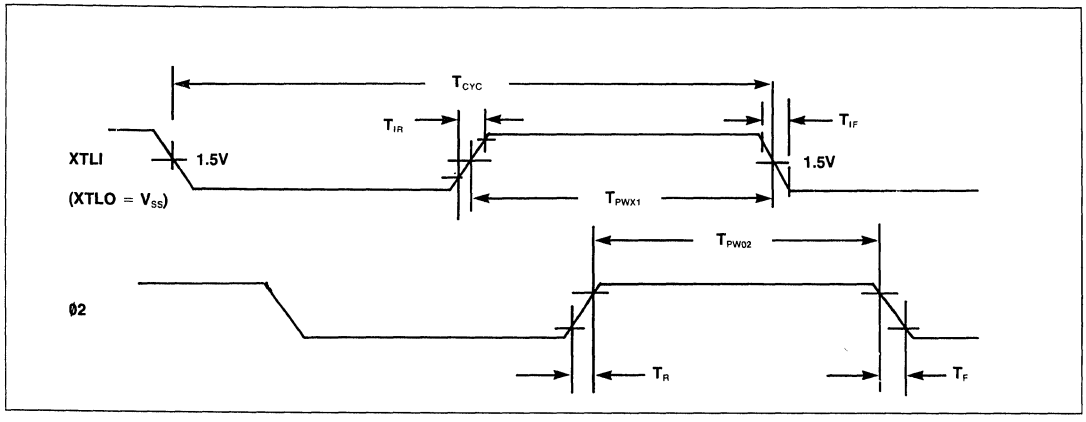
E.1 GENERAL NOTES

1. V_{CC} = 5V ±5%, 0°C ≤ TA ≤ 70°C
2. A valid V_{CC} – $\overline{RES}$ sequence is required before proper operation is achieved.
3. All timing reference levels are 0.8V and 2.0V, unless otherwise specified.
4. All time units are nanoseconds, unless otherwise specified.
5. All capacitive loading is 130pF maximum, except as noted below:

PA, PB	— 50pF maximum
PC (I/O Modes Only)	— 50pF maximum
PC (A_{BB} and Mux Mode)	— 130pF maximum
PC6, PC7 (Full Address Mode)	— 130pF maximum

E.2 CLOCK TIMING

Symbol	Parameter	1 MHz		2 MHz		Units
		Min	Max	Min	Max	
T_{CYC}	Cycle Time	1.0	10	0.5	10	μs
T_{PWX1}	XTLI Input Clock Pulse Width XTLO = VSS	500 ±25	—	250 ±10	—	ns
T_{PW02}	Output Clock Pulse Width at Minimum T_{CYC}	T_{PWX1}	T_{PWX1} +0 −25	T_{PWX1}	T_{PWX1} +0 −20	ns
T_R, T_F	Output Clock Rise, Fall Time	—	25	—	15	ns
T_{IR}, T_{IF}	Input Clock Rise Fall Time	—	10	—	10	ns



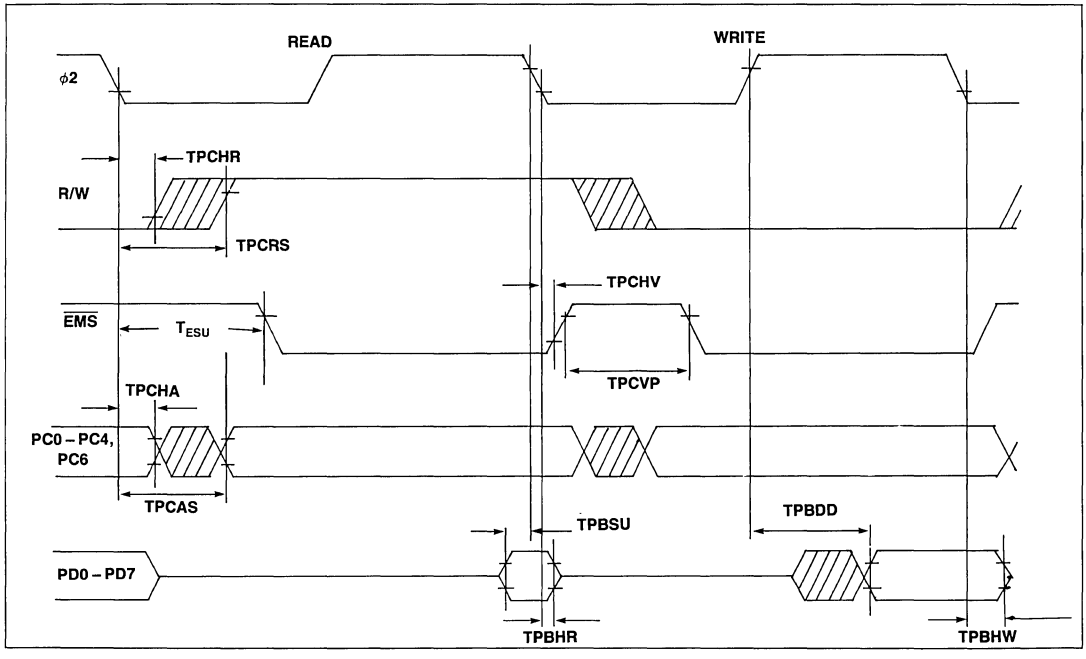
E.3 ABBREVIATED MODE TIMING—PC AND PD

(MCR 5 = 1, MCR 6 = 0, MCR 7 = 1)

Symbol	Parameter	1 MHz		2 MHz		Units
		Min	Max	Min	Max	
T_{PCRS}	(PC5) R/W Setup Time	—	225	—	140	ns
T_{PCAS}	(PC0–PC4, PC6) Address Setup Time	—	225	—	140	ns
T_{PBSU}	(PD) Data Setup Time	50	—	35	—	ns
T_{PBHR}	(PD) Data Read Hold Time	10	—	10	—	ns
T_{PBHW}	(PD) Data Write Hold Time	30	—	30	—	ns
T_{PBDD}	(PD) Data Output Delay	—	175	—	150	ns
T_{PCHA}	(PC0–PC4, PC6) Address Hold Time	30	—	30	—	ns
T_{PCHR}	(PC5) R/W Hold Time	30	—	30	—	ns
T_{PCHV}	(PC7) $\overline{EMS}$ Hold Time	10	—	10	—	ns
T_{ESU}	(PC7) $\overline{EMS}$ Setup Time	—	350	—	210	ns
T_{PCVP}	(PC7) $\overline{EMS}$ Stabilization Time	30	—	30	—	ns

NOTE 1: Values assume PC0–PC4, PC6 and PC7 have the same capacitive load.

E.3.1 Abbreviated Mode Timing Diagram



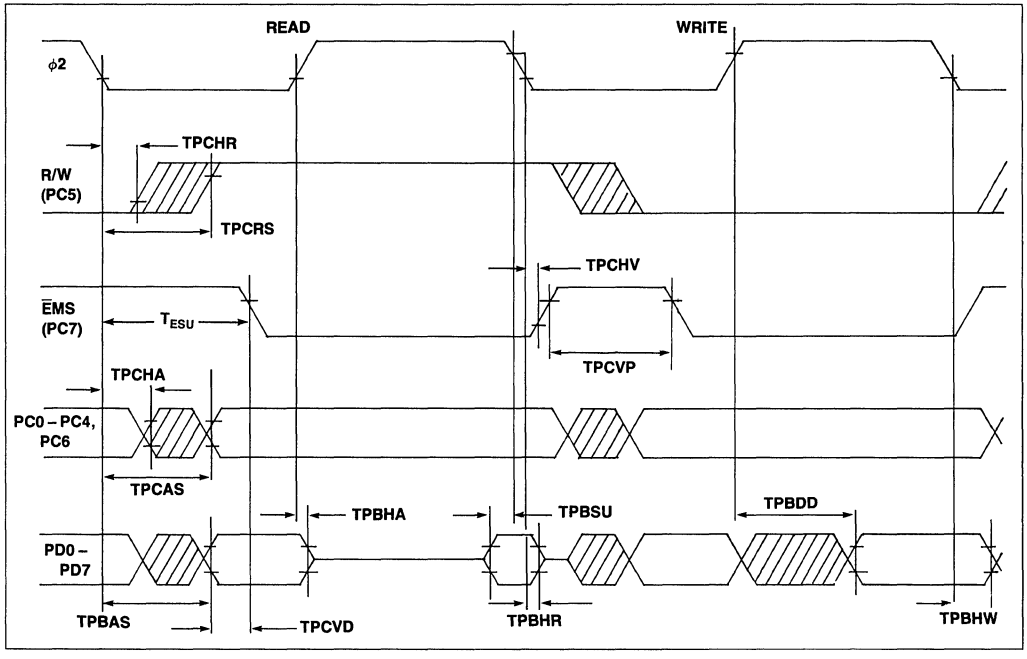
E.4 MULTIPLEXED MODE TIMING—PC AND PD

(MCR 5 = 1, MCR 6 = 1, MCR 7 = 1)

Symbol	Parameter	1 MHz		2 MHz		Units
		Min	Max	Min	Max	
T_{PCRS}	(PC5) R/W Setup Time	—	225	—	140	ns
T_{PCAS}	(PC0–PC4, PC6) Address Setup Time	—	225	—	140	ns
T_{PBAS}	(PD) Address Setup Time	—	225	—	140	ns
T_{PBSU}	(PD) Data Setup Time	50	—	35	—	ns
T_{PBHR}	(PD) Data Read Hold Time	10	—	10	—	ns
T_{PBHW}	(PD) Data Write Hold Time	30	—	30	—	ns
T_{PBDD}	(PD) Data Output Delay	—	175	—	150	ns
T_{PCHA}	(PC0–PC4, PC6) Address Hold Time	30	—	30	—	ns
T_{PBHA}	(PD) Address Hold Time	10	100	10	80	ns
T_{PCHR}	(PC5) R/W Hold Time	30	—	30	—	ns
T_{PCHV}	(PC7) $\overline{EMS}$ Hold Time	10	—	10	—	ns
T_{PCVD}(1)	(PC7) Address to $\overline{EMS}$ Delay Time	30	—	30	—	ns
T_{PCVP}	(PC7) $\overline{EMS}$ Stabilization Time	30	—	30	—	ns
T_{ESU}	(PC7) $\overline{EMS}$ Setup Time	—	350	—	210	ns

NOTE 1: Values assume PD0–PD7 and PC7 have the same capacitive load.

E.4.1 Multiplex Mode Timing Diagram

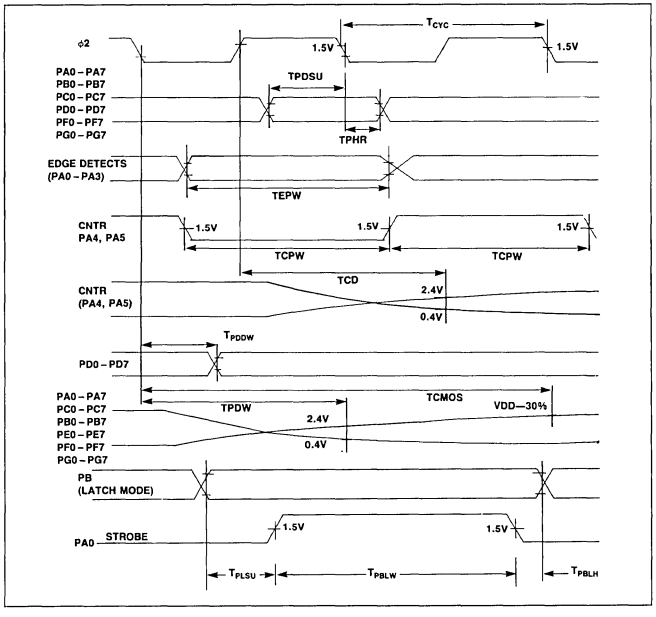


E.5 I/O, EDGE DETECT, COUNTERS, AND SERIAL I/O TIMING

Symbol	Parameter	1 MHz Min	1 MHz Max	2 MHz Min	2 MHz Max	Units
	Internal Write to Peripheral Data Valid					ns
T_{PDW}(1)	PA, PB, PC, PE, PF, PG, TTL	—	500	—	500	
T_{CMOS}(1)	PA, PB, PC, PE, PF, PG, CMOS	—	1000	—	1000	
T_{PDDW}	PD	—	175	—	150	
	Peripheral Data Setup Time					ns
T_{PDSU}	PA, PB, PC, PF, PG	200	—	200	—	
T_{PDSU}	PD	50	—	50	—	
	Peripheral Data Hold Time					ns
T_{PHR}	PA, PB, PC, PF, PG	75	—	75	—	
T_{PHR}	PD	10	—	10	—	
T_{EPW}	PA0–PA3 Edge Detect Pulse Width	T_{CYC}	—	T_{CYC}	—	ns
	Counters A and B					ns
T_{CPW}	PA4, PA5 Input Pulse Width	T_{CYC}	—	T_{CYC}	—	
T_{CD}(1)	PA4, PA5, Output Delay	—	500	—	500	
	Port B Latch Mode					ns
T_{PBLW}	PA0 Strobe Pulse Width	T_{CYC}	—	T_{CYC}	—	
T_{PLSU}	PB Data Setup Time	175	—	150	—	
T_{PBLH}	PB Data Hold Time	30	—	30		
	Serial I/O					ns
T_{PDW}(1)	PA6 XMTR TTL	—	500	—	500	
T_{CMOS}(1)	PA6 XMTR CMOS	—	1000	—	1000	
T_{CPW}	PA4 RCVR S/R Clock Width	4 T_{CYC}	—	4 T_{CYC}	—	
T_{PDW}(1)	PA4 XMTR Clock—S/R Mode (TTL)	—	500	—	500	
T_{CMOS}(1)	PA4 XMTR Clock—S/R Mode (CMOS)	—	1000	—	1000	

NOTE 1: Maximum Load Capacitance: 50pF Passive Pull-Up Required.

E.5.1 I/O, Edge Detect, Counter, and Serial I/O Timing



3

Rockwell

R65/11EB and R65/11EAB Backpack Emulator

INTRODUCTION

The Rockwell R65/11EB and R65/11EAB Backpack Emulator are PROM prototyping versions of the 8-bit, masked-ROM R6500/11 and R6500/15 one-chip microcomputers. Like the R6500/11, the backpack device is totally upward/downward compatible with all members of the R6500/11 family. It is designed to accept standard 5-volt, 24-pin EPROMs or ROMs directly, in a socket on top of the Emulator. This packaging concept allows a standard EPROM to be easily removed, re-programmed, then reinserted as often as desired.

The backpack devices have the same pinouts as the masked-ROM R6500/11 and R6500/15 microcomputers. These 40 pins are functionally and operationally identical to the pins on the R6500/11. The R6500/11 Microcomputer Product Description (Order No. 2119) includes a description of the interface signals and their functions. Whereas the masked-ROM R6500/11 provides 3K bytes of read-only memory, the R65/11EB will address 4K bytes of external program memory. This extra memory accommodates program patches, test programs or optional programs during breadboard and prototype development states.

FEATURES

- PROM version of the R6500/11 and R6500/15
- Completely pin compatible with R6500/11 single-chip microcomputers
- Profile approaches 40-pin DIP of R6500/11
- Accepts 5 volt, 24-pin industry-standard EMPROMS—4K memories—2732, 2732A (4K bytes addressable)
- Use as prototyping tool or for low volume production
- 4K bytes of memory capacity
- 192 x 8 static RAM
- Separate power pin for 32 bytes of RAM
- Software compatibility with the R6500 family
- 32 bi-directional TTL compatible I/O lines (4 ports)
- Two 16-bit programmable counter/latches with six modes (interval timer, pulse generator, event counter, pulse width measurement, asymmetrical pulse generator, and retriggerable interval timer)
- 10 interrupts (reset, non-maskable, four external edge sensitive, 2 counters, serial data received, serial data transmitted)
- Crystal or external time base
- Single +5V power supply

Note: R6500/11 describes both R6500/11 and R6500/15.

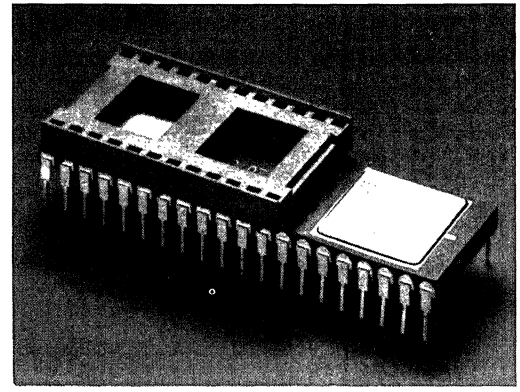
ORDERING INFORMATION

BACKPACK EMULATOR

Part Number	Memory Capacity	Compatible Memories	Temperature Range and Speed
R65/11EB	4K x 8	2732	0°C to 70°C 1 MHz
R65/11EAB	4K x 8	2732A	0°C to 70°C 2 MHz

SUPPORT PRODUCTS

Part Number	Description
RDC-3101	Low Cost Emulator (LCE) Development System
RDC-3030	LCE PROM Programmer Module
RDC-309	1 or 2-MHz R6500/11 Personality Module



R65/11EB Backpack Emulator

CONFIGURATIONS

The Backpack Emulator is available in two different versions, to accommodate 1 MHz and 2 MHz speeds. Both versions provide 192 bytes of RAM and I/O, as well as 24 signals to support the external memory "backpack" socket.

The emulator will relocate the EPROM address space to FXXX (see Memory Map). EPROM addresses FFA through FFF must contain the interrupt vectors.

EXTERNAL FREQUENCY REFERENCE

The external frequency reference may be a crystal or a clock. The R65/11EB and R65/11EAB divide the input clock by two regardless of the source.

I/O PORT PULLUPS

The devices have internal I/O port pull-up resistors on ports A, B, & C. Port D has push-pull drivers.

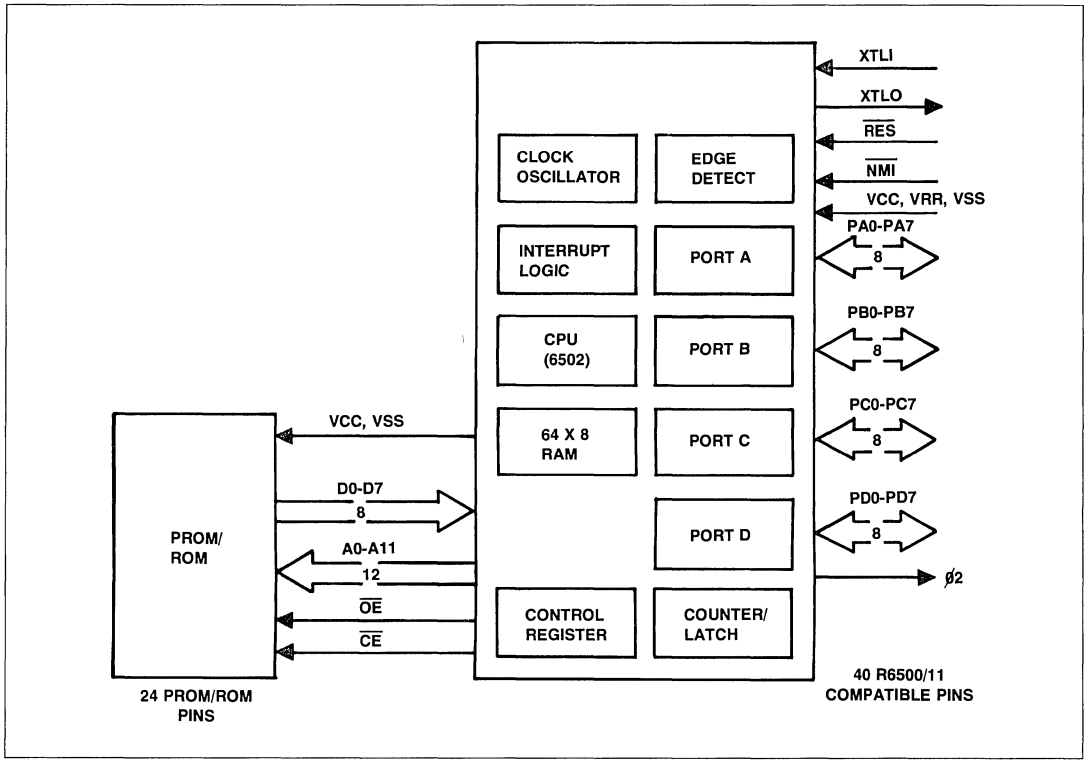
MODE CONTROL REGISTER

Bit 6 of the MODE CONTROL REGISTER (MCR6) must be set to 1 if Bit 7 (MCR7) is set to ϕ. (R65/11EB and R65/11EAB only).

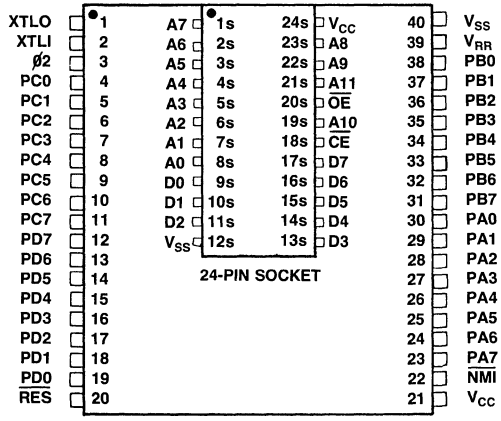
PRODUCT SUPPORT

The Backpack Emulator is just one of the products that Rockwell offers to facilitate system and program development for the R6500/11.

The Low Cost Emulator (LCE) Development System with R6500/11 Personality Module supports both hardware and software development. Complete in-circuit user emulation with the R6500/11 Personality Module allows total system test and evaluation. With the optional PROM Programmer, the LCE can also be used to program EPROMs for the development activity. When PROM programs have been finalized, the PROM device can be sent to Rockwell for masking into the 3K ROM of the R6500/11 or the 4K ROM of the R6500/15.



R65/11EB Interface Diagram



Pin Configuration

BACKPACK MEMORY SIGNAL DESCRIPTION

Signal Name	Pin No.	Description
D0–D7	9S–11S, 13S–17S	Data Bus Lines. All instruction and data transfers take place on the data bus lines. The buffers driving the data bus lines have full three-state capability. Each data bus pin is connected to an input and an output buffer, with the output buffer remaining in the floating condition.
A0–A7 A8, A9 A10 A11	1S–8A, 23S, 24S 19S 21S	Address Bus Lines. The address bus lines are buffered by push/pull type drivers that can drive one standard TTL load.
$\overline{CE}$	18S	Chip Enable. $\overline{CE}$ is active when the address is 8000-FFFF. This line can drive one TTL load.
$\overline{OE}$	20S	Memory Enable Line. This signal provides the output enable for the memory to place information on the data bus lines. This signal is driven by an inverted R/$\overline{W}$ signal from the CPU. It can drive 1 TTL load.
V_{CC}	24S	Main Power Supply +5V. This pin is tied directly to pin 21 (V_{CC}).
V_{SS}	12S	Signal and Power Ground (zero volts). This pin is tied directly to pin 40 (V_{SS}).

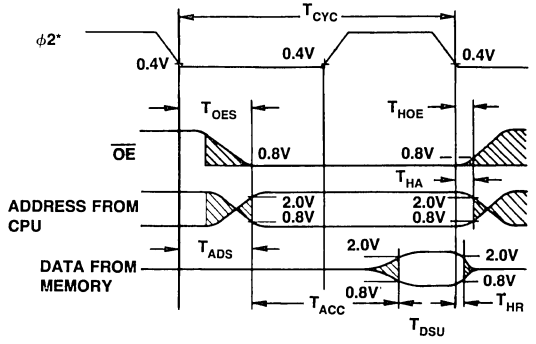
I/O AND INTERNAL REGISTER ADDRESSES

Address (Hex)	Read	Write
001F	— —	— —
1E	Lower Counter B	Upper Latch B, Cntr B←Latch B, CLR Flag
1D	Upper Counter B	Upper Latch B, Latch C←Latch B
1C	Lower Counter B, CLR Flag	Lower Latch B
1B	— —	— —
1A	Lower Counter A	Upper Latch A, Cntr A←Latch A, CLR Flag
19	Upper Counter A	Upper Latch A
18	Lower Conter A, CLR Flag	Lower Latch A
17	Serial Receiver Data Register	Serial Transmitter Data Register
16	Serial Comm. Status Register	Serial Comm. Status Reg. Bits 4 & 5 only
15	Serial Comm. Control Register	Serial Comm. Control Register
14	Mode Control Register	Mode Control Register
13	— —	— —
12	Interrupt Enable Register	Interrupt Enable Register
11	Interrupt Flag Register	— —
0010	Read FF	Clear Int Flag (Bits 0-3 only, Write 0's only)
04 thru 0F	— —	— —
03	Port D	Port D
02	Port C	Port C
01	Port B	Port B
0000	Port A	Port A

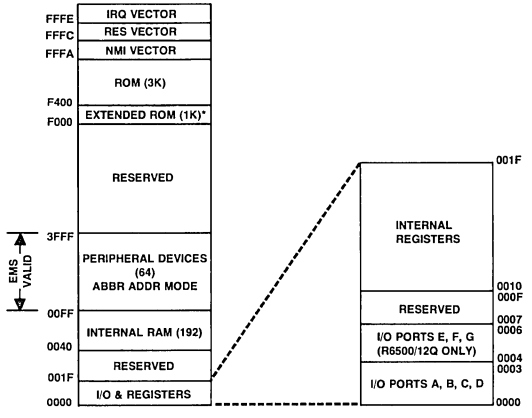
READ TIMING CHARACTERISTICS

Signal	Symbol	1 MHz		2 MHz		Unit
		Min.	Max.	Min.	Max.	
$\overline{OE}$ and $\overline{CE}$ setup time from CPU	T_{OES}	—	225	—	140	ns
Address setup time from CPU	T_{ADS}	—	150	—	75	ns
Memory read access time	T_{ACC}	—	700	—	315	ns
Data set up time	T_{DSU}	50	—	35	—	ns
Data hold time—Read	T_{HR}	10	—	10	—	ns
Address hold time	T_{HA}	30	—	30	—	ns
$\overline{OE}$ and $\overline{CE}$ hold time	T_{HOE}	30	—	30	—	ns
Cycle Time	T_{CYC}	1.0	10.0	0.5	10.0	μs

READ TIMING WAVEFORMS

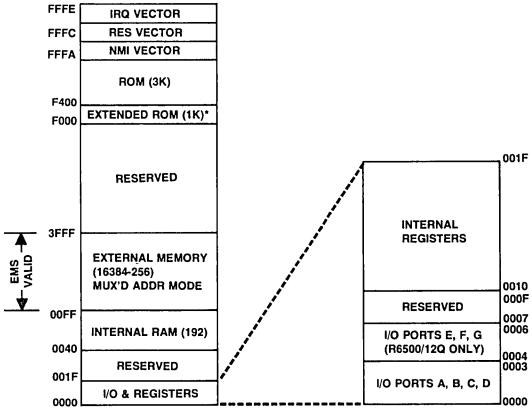


ABBREVIATED MODE MEMORY MAP



*NOT AVAILABLE FOR MASKED ROM R6500/11.

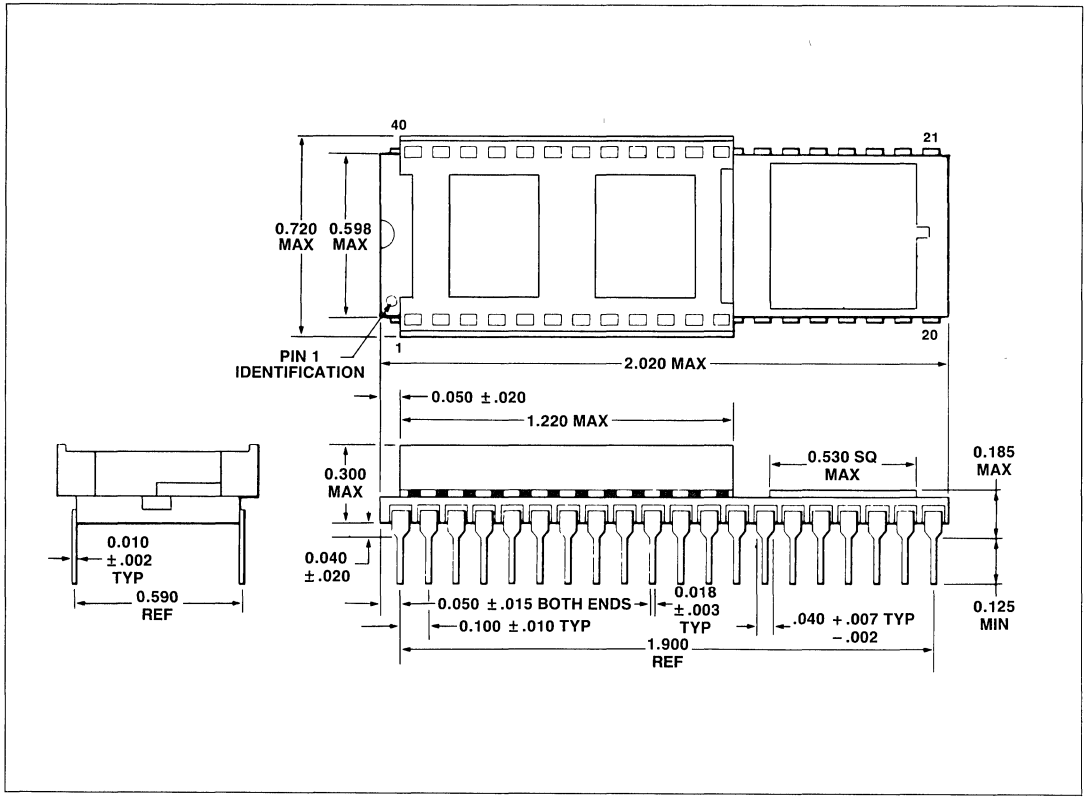
MULTIPLEXED MODE MEMORY MAP



ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ± 5%, V_{SS} = 0, T_A = 0°C to 70°C, unless otherwise stated)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Conditions
Input High Threshold Voltage D0-D7	V_{IHT}	+2.0	—	—	Vdc	
Input Low Threshold Voltage D0-D7	V_{ILT}	—	—	+0.8	Vdc	
Three-State (Off State) Input Current D0-D7	I_{TSI}	—	—	±10	μA	V_{CC} = 5.25V V_{IN} = 0.4V to 2.4V
Output High Voltage D0-D7, A0-A11, $\overline{OE}$, $\overline{CE}$	V_{OH}	+2.4	—	—	Vdc	V_{CC} = 4.75V I_{LOAD} = 100μA
Output Low Voltage D0-D7, A0-A11 $\overline{OE}$, $\overline{CE}$	V_{OL}	—	—	+0.4	Vdc	V_{CC} = 4.75V I_{LOAD} = 1.6mA
Power Dissipation (less EPROM)	P_D	—	0.80	1.20	W	
Output Capacitance (High Impendance State) D0-D7	C_{OUT}	—	—	10	pF	T_A = 25°C V_{IN} = 0V f = 1 MHz
Input Capacitance	C_{IN}	—	—	10	pF	
I/O Port Pull-up Resistance	R_L	3.0	6.0	11.5	kohm	



40-Pin Backpack Package

Rockwell

R6501
One-Chip Microprocessor

SECTION 1
INTRODUCTION

SUMMARY

The Rockwell R6501 is a complete, high performance 8-bit NMOS-3 microcomputer on a single chip and is compatible with all members of the R6500 family.

The R6501 consists of an enhanced 6502 CPU, an internal clock oscillator, 192 bytes of Random Access Memory (RAM), and versatile interface circuitry. The interface circuitry includes two-16-bit programmable timer/counters, 32 bidirectional input/output lines (including four edge-sensitive lines and input latching on one 8-bit port), a full-duplex serial I/O channel, ten interrupts, and bus expandability.

The innovative architecture and the demonstrated high performance of the R6502 CPU, as well as instruction simplicity, results in system cost-effectiveness and a wide range of computational power. These features make the R6501 a leading candidate for microcomputer application.

Rockwell supports development of the R6501 with the Low Cost Emulator (LCE) Development System and the R6500/* Family of Personality Modules. Complete in-circuit emulation with the R6500/* Family of Personality Modules allows total system test and evaluation.

This product description assumes that the reader is familiar with the R6502 CPU hardware and programming capabilities. A detailed description of the R6502 CPU hardware is included in the R6500 Microcomputer System Hardware Manual (Document Order No. 201). A description of the instruction capabilities of the R6502 CPU is contained in the R6500 Microcomputer System Programming Manual (Document Order No. 202).

ORDERING INFORMATION

Part Number:
R6501

Temperature Range (T_L to T_H):
- No Letter = 0°C to 70°C (Commercial)
- E = −40°C to +85°C (Industrial)

Package
- J = 68-Pin Plastic Leaded Chip Carrier (PLCC)
- Q = 64-Pin Plastic QUIP

Frequency
- No Letter = 1 MHz Operation
- A = 2 MHz Operation

FEATURES

- Enhanced 6502 CPU
  - —Four new bit manipulation instructions
    - Set Memory Bit (SMB)
    - Reset Memory Bit (RMB)
    - Branch on Bit Set (BBS)
    - Branch on Bit Reset (BBR)
  - —Decimal and binary arithmetic modes
  - —13 addressing modes
  - —True indexing
- 192-byte static RAM
- 32 bidirectional, TTL-compatible I/O lines (four ports)
  - —One 8-bit port may be tri-stated under software control
  - —One 8-bit port may have latched inputs under software control
  - —Internal pull-up resistors on parts PA, PB, and PC
- Two 16-bit programmable counter/timers, with latches
  - —Pulse width measurement
  - —Asymmetrical pulse generation
  - —Pulse generation
  - —Interval timer
  - —Event counter
  - —Retriggerable interval timer
- Serial port
  - —Full-duplex asynchronous operation mode
  - —Selectable 5- to 8-bit characters
  - —Wake-up feature
  - —Synchronous shift register mode
  - —Standard programmable bit rates programmable up to 62.5K bits/sec @ 1 MHz
- Ten interrupts
  - —Four edge-sensitive lines; two positive, two negative
  - —Reset and non-maskable interrupt
  - —Two counter underflows
  - —Serial data received and serial data transmitted
- Bus expandable to 64K bytes of external memory
- Flexible clock circuitry
  - —2 MHz (R6501A) or 1 MHz (R6501) internal operation
  - —Crystal or clock input
- 1 μs minimum instruction execution time at 2 MHz
- Single +5V power supply
- 12 mW stand-by power for 32 bytes of the 192-byte RAM
- Available in 64-pin plastic QUIP and 68-pin PLCC packages

3

SECTION 2
INTERFACE REQUIREMENTS

This section describes the interface requirements for the R6501. Figure 2-1 and 2-2 show the Interface Diagram and the pin out configuration for both devices. Table 2-1 describes the function of each pin. Figure 3-1 has a detailed block diagram of the R6501 ports which illustrates the internal function of the device.

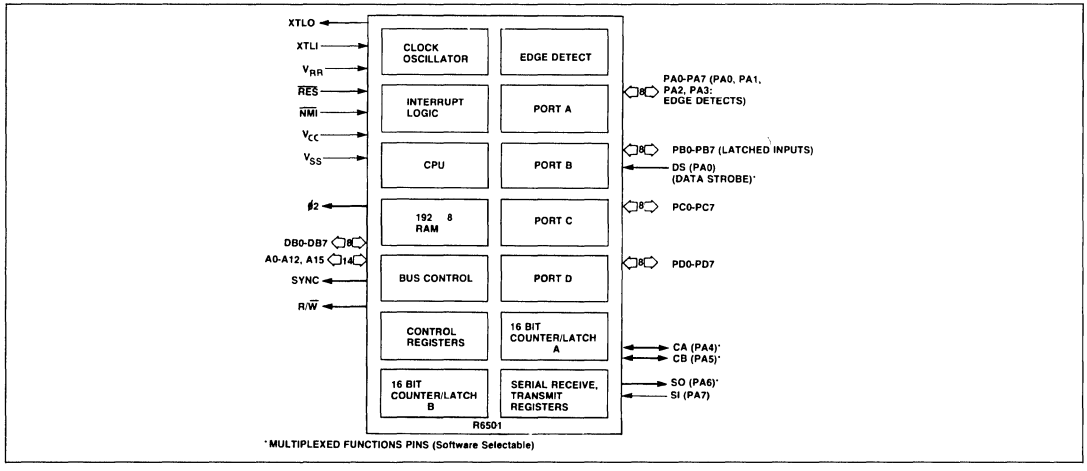
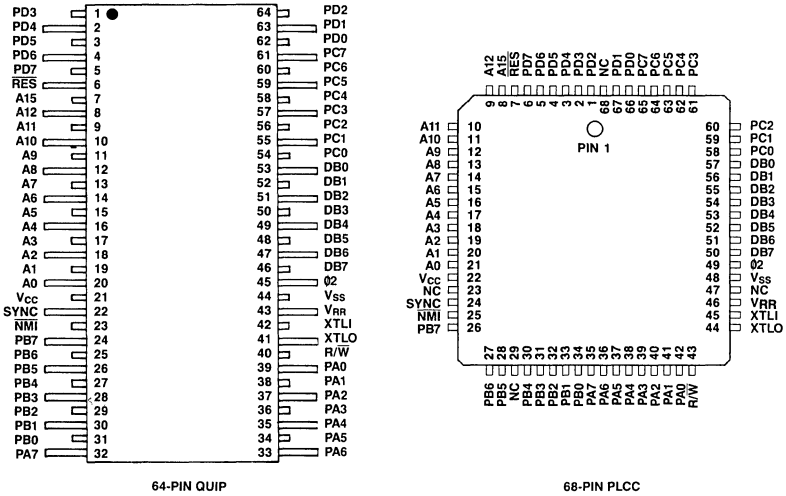


Figure 2-1. R6501 Interface Diagram



Note: "NC" means no connection is to be made to this pin.

Figure 2-2. R6501 Pin Assignments

Table 2-1. R6501 Pin Descriptions

Signal Name	I/O	Pin No. 64-Pin QUIP	Pin No. 68-Pin PLCC	Description
V_{CC}	I	21	22	**POWER.** Main power supply. +5V.
V_{RR}	I	43	46	**RAM RETENTION POWER.** Separate power pin for RAM. In the event that V_{CC} power is off, this power retains RAM data. +5V.
V_{SS}		44	48	**GROUND.** Signal and power ground (0V).
XTLI	I	42	45	**CRYSTAL IN.** Crystal or clock input for internal clock oscillator. Allows input of X1 clock signal if XTLO is connected to V_{SS}, or of X4 (R6501) or X2 (R6501A) clock if XTLO is floated.
XTLO	O	41	44	**CRYSTAL OUT.** Crystal output from internal clock oscillator.
$\overline{RES}$	I	6	7	**RESET.** The Reset input is used to initialize the device. This signal must not transition from low to high for at least eight cycles after V_{CC} reaches operating range and the internal oscillator has stabilized.
ø2	O	45	49	**PHASE 2 CLOCK.** Clock signal output at internal frequency.
$\overline{NMI}$	I	23	25	**NON-MASKABLE INTERRUPT.** A negative going edge on the Non-Maskable Interrupt signal requests that a non-maskable interrupt be generated with the CPU.
PA0-PA7	I/O	39-32	42-35	**PORT A.** General purpose I/O Port A.
PB0-PB7	I/O	31-24	34-30, 28-26	**PORT B.** General purpose I/O Port B.
PC0-PC7	I/O	54-61	58-65	**PORT C.** General purpose I/O Port C.
PD0-PD7	I/O	62-64, 1-5	66, 67, 1-6	**PORT D.** General purpose I/O Port D. Four 8-bit ports used for either input/output. Each line of Ports A, B and C consists of an active transistor to V_{SS} and a passive pull-up to V_{CC}. Port D functions as either an 8-bit input or an 8-bit output port. It has active pull-up and pull-down transistors.
A0-A12, A15	O	20-8,7	21-9, 8	**ADDRESS LINES.** Fourteen address lines used to address a complete 65K external address space. Note: A13 and A14 are sourced through PC6 and PC7 when in the Full Address Mode.
DB0-DB7	I/O	53-46	57-50	**DATA LINES.** Eight bidirectional data bus lines used to transmit data to and from external memory.
SYNC	O	22	24	**SYNC.** SYNC is a positive going signal for the full clock cycle whenever the CPU is performing an OP CODE fetch.
R/$\overline{W}$	O	40	43	**READ/$\overline{WRITE}$.** Controls the direction of data transfer between the CPU and the external 65K address space. The signal is high when reading and low when writing.

3

SECTION 3
SYSTEM ARCHITECTURE

This section provides a functional description of the R6501. Functionally the R6501 consists of a CPU, RAM, four 8-bit parallel I/O ports, a serial I/O port, dual counter/latch circuits, a mode control register, and an interrupt flag/enable dual register circuit. a block diagram of the system is shown in Figure 3-1.

NOTE

Throughout this document, unless specified otherwise, all memory or register address locations are specified in hexadecimal notation.

3.1 CPU LOGIC

The R6501 internal CPU is a standard 6502 configuration with an 8-bit Accumulator register, two 8-bit Index Registers (X and Y); an 8-bit Stack Pointer register, an ALU, a 16-bit Program Counter, and standard instruction register/decode and internal timing control logic.

3.1.1 Accumulator

The accumulator is a general purpose 8-bit register that stores the results of most arithmetic and logic operations. In addition, the accumulator usually contains one of the two data words used in these operations.

3.1.2 Index Registers

There are two 8-bit index registers, X and Y. Each index register can be used as a base to modify the address data program counter and thus obtain a new address—the sum of the program counter contents and the index register contents.

When executing an instruction which specifies indirect addressing, the CPU fetches the op code and the address and modifies the address from memory by adding the index register to it prior to loading or storing the value of memory.

Indexing greatly simplifies many types of programs, especially those using data tables.

3.1.3 Stack Pointer

The Stack Pointer is an 8-bit register. It is automatically incremented and decremented under control of the microprocessor to perform stack manipulation in response to either user instructions, an internal $\overline{IRQ}$ interrupt, or the external interrupt line $\overline{NMI}$. The Stack Pointer must be initialized by the user program.

The stack allows simple implementation of multiple level interrupts, subroutine nesting and simplification of many types of data manipulation. The JSR, BRK, RTI and RTS instructions use the stack and Stack Pointer.

The stack can be envisioned as a deck of cards which may be accessed only from the top. The address of a memory location is stored (or "pushed") onto the stack. Each time data are to be pushed onto the stack, the Stack Pointer is placed on the Address Bus, data are written into the memory location addressed by the Stack Pointer, and the Stack Pointer is decremented by 1. Each time data are read (or "pulled") from the stack, the Stack Pointer is incremented by 1. The Stack Pointer is then placed on the Address Bus and data are read from the memory location addressed by the Pointer.

The stack is located on zero page, i.e., memory locations 00FF-0040. After reset, which leaves the Stack Pointer indeterminate, normal usage calls for its initialization at 00FF.

3.1.4 Arithmetic And Logic Unit (ALU)

All arithmetic and logic operations take place in the ALU, including incrementing and decrementing internal registers (except the Program Counter). The ALU cannot store data for more than one cycle. If data are placed on the inputs to the ALU at the beginning of a cycle, the result is always gated into one of the storage registers or to external memory during the next cycle.

Each bit of the ALU has two inputs. These inputs can be tied to various internal buses or to a logic zero; the ALU then generates the function (AND, OR, SUM, and so on) using the data on the two inputs.

3.1.5 Program Counter

The 16-bit Program Counter provides the addresses that are used to step the processor through sequential instructions in a program. Each time the processor fetches an instruction from program memory, the lower (least significant) byte of the Program Counter (PCL) is placed on the low-order bits of the Address Bus and the higher (most significant) byte of the Program Counter (PCH) is placed on the high-order 8 bits of the Address Bus. The Counter is incremented each time an instruction or data is fetched from program memory.

3.1.6 Instruction Register and Instruction Decode

Instructions are fetched from ROM or RAM and gated onto the Internal Data Bus. These instructions are latched into the Instruction Register, then decoded along with timing and interrupt signals to generate control signals for the various registers.

3.1.7 Timing Control

The Timing Control Logic keeps track of the specific instruction cycle being executed. This logic is set to T0 each time an instruction fetch is executed and is advanced at the beginning of each Phase One clock pulse for as many cycles as are required to complete the instruction. Each data transfer which takes place between the registers is caused by decoding the contents of both the instruction register and timing control unit.

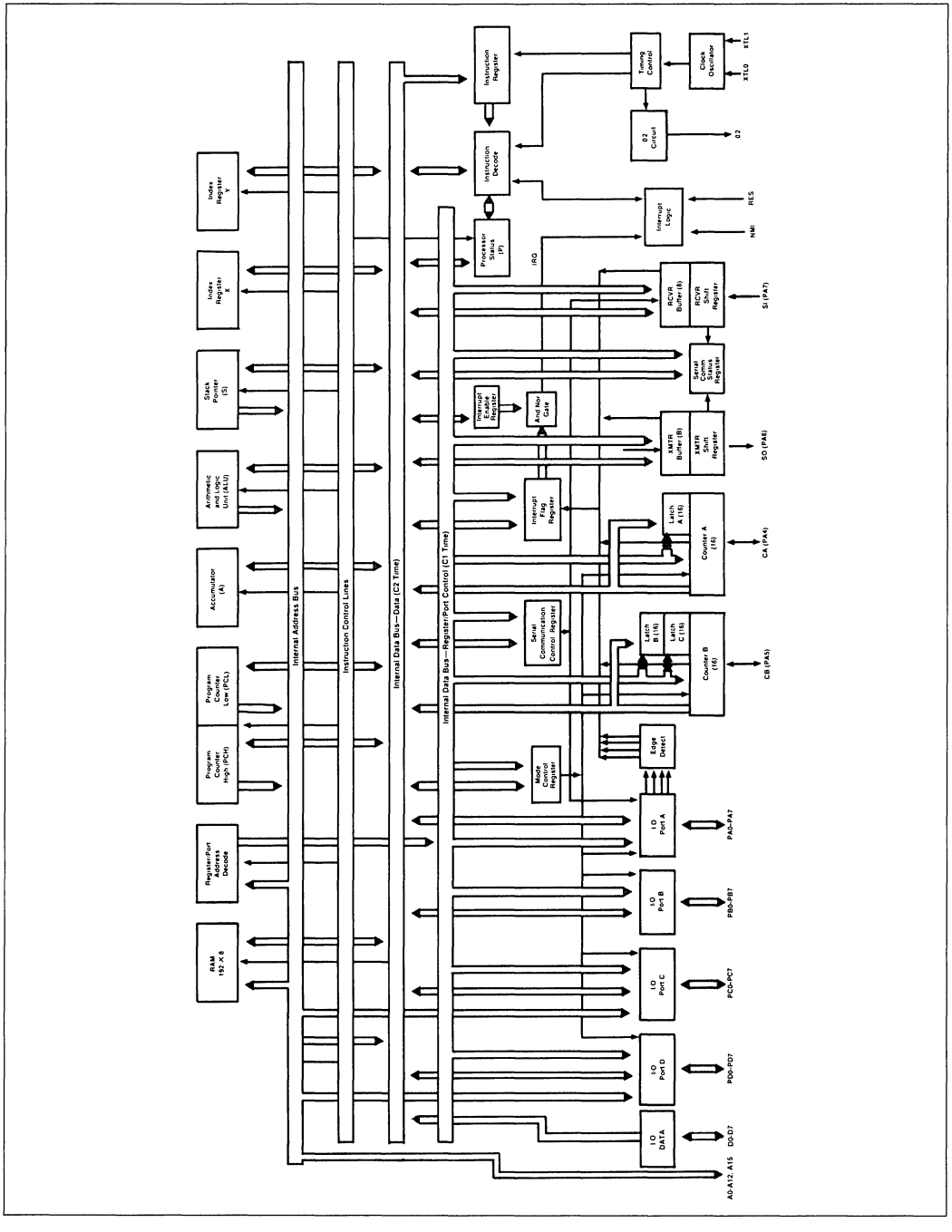


Figure 3-1. Detailed Block Diagram

3

3.1.8 Interrupt Logic

Interrupt logic controls the sequencing of three interrupts; $\overline{RES}$, $\overline{NMI}$ and $\overline{IRQ}$. $\overline{IRQ}$ is generated by any one of eight conditions: 2 Counter Overflows, 2 Positive Edge Detects, 2 Negative Edge Detects, and 2 Serial Port Conditions.

3.2 NEW INSTRUCTIONS

In addition to the standard R6502 instruction set, four new bit manipulation instructions have been added to the R6501. The added instructions and their format are explained in the following paragraphs. Refer to Appendix A for the Op Code mnemonic addressing matrix for these added instructions. The four added instructions do not impact the CPU processor status register.

3.2.1 Set Memory Bit SMB m, Addr.)

This instruction sets to "1" one of the 8-bit data field specified by the zero page address (memory or I/O port). The first byte of the instruction specifies the SMB operation and one of eight bits to be set. The second byte of the instruction designates address (0-255) of the byte to be operated upon.

3.2.2 Reset Memory Bit (RMB m, Addr.)

This instruction is the same operation and format as SMB instruction except a reset to "0" of the bit results.

3.2.3 Branch On Bit Set Relative (BBS m, Addr, DEST)

This instruction tests one of eight bits designated by a 3-bit immediate field within the first byte of the instruction. The second byte is used to designate the address of the byte to be tested within the zero page address range (memory or I/O ports). The third byte of the instruction is used to specify the 8-bit relative address to which the instruction branches if the bit tested is a "1". If the bit tested is not set, the next sequential instruction is executed.

3.2.4 Branch On Bit Reset Relative (BBR m, Addr, DEST)

This instruction is the same operation and format as the BBS instruction except that a branch takes place if the bit tested is a "0".

3.3 READ-ONLY-MEMORY (ROM)

The R6501 has no ROM and its Reset vector is at FFFC.

3.4 RANDOM ACCESS MEMORY (RAM)

The RAM consists of 192 bytes of read/write memory with an assigned page zero address of 0040 through 00FF. The R6501 provides a separate power pin (V_{RR}) which may be used for standby power for 32 bytes located at 0040-005F. In the event of the loss of V_{CC} power, the lowest 32 bytes of RAM data will be retained if standby power is supplied to the V_{RR} pin. If the RAM data retention is not required then V_{RR} must be connected to V_{CC}. During operation V_{RR} must be at the V_{CC} level.

For the RAM to retain data upon loss of V_{CC}, V_{RR} must be supplied within operating range and $\overline{RES}$ must be driven low at least eight $\phi 2$ clock pulses before V_{CC} falls out of operating range. $\overline{RES}$ must then be held low while V_{CC} is out of operating range and until at least eight $\phi 2$ clock cycles after V_{CC} is again within operating range and the internal $\phi 2$ oscillator is stabilized. V_{RR} must remain within V_{CC} operating range during normal operation. When V_{CC} is out of operating range, V_{RR} must remain within the V_{RR} retention range in order to retain data. Figure 3.2 shows typical waveforms.

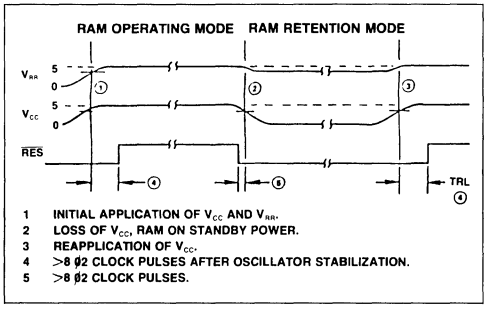


Figure 3-2. Data Retention Timing

3.5 CLOCK OSCILLATOR

The R6501 has been configured for a crystal oscillator, a countdown network, and for Master Mode Operation.

A reference frequency can be generated with the on-chip oscillator using either an external crystal or an external oscillator. The oscillator reference frequency passes through an internal countdown network to obtain the internal operating frequency.

The on-chip oscillator is designed for a parallel resonant crystal connected between XTLI and XTLO pins. The equivalent oscillator circuit is shown in Figure 3-3a.

A parallel resonant crystal is specified by its load capacitance and series resonant resistance. For proper oscillator operation, the load capacitance (C_L), series resistance (R_s) and the crystal resonant frequency (F) must meet the following two relations:

$$(C + 27) = 2C_L \quad \text{or} \quad C = 2C_L - 27 \text{ pF}$$

$$R_s \leq R_{smax} = \frac{2 \times 10^6}{(FC_L)^2}$$

where: F is in MHz; C and C_L are in pF; R is in ohms.

To select a parallel resonant crystal for the oscillator, first select the load capacitance from a crystal manufacturer's catalog. Next, calculate R_{smax} based on F and C_L. The selected crystal must have a R_s less than the R_{smax}.

For example, if C_L = 22 pF for a 4 MHz parallel resonant crystal, then

$$C = (2 \times 22) - 27 = 17 \text{ pF (use standard value of 18 pF)}$$

The series resistance of the crystal must be less than

$$R_{smax} = \frac{2 \times 10^6}{(4 \times 22)^2} = 258 \text{ ohms}$$

Internal timing can also be controlled by driving the XTLI pin with an external frequency source. Figure 3-3b shows typical connections. If XTLO is left floating, the external source is divided by the internal countdown network. However, if XTLO is tied to V_{SS}, the internal countdown network is bypassed causing the chip to operate at the frequency of the external source.

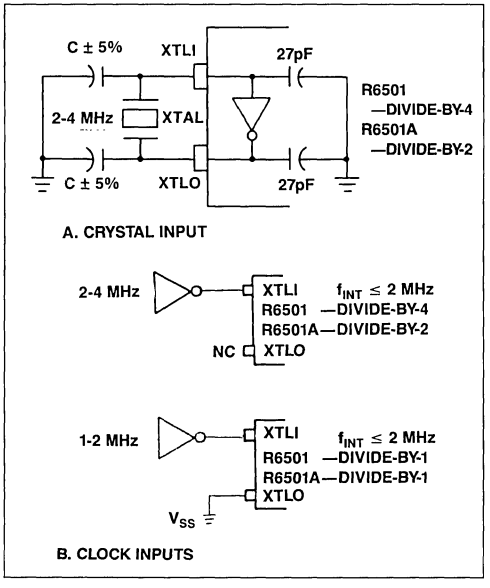


Figure 3-3. Clock Oscillator Input Options

3.6 MODE CONTROL REGISTER (MCR)

The Mode Control Register contains control bits for the multifunction I/O ports and mode select bits for Counter A and Counter B. Its setting, along with the setting of the Serial Communications Control Register (SCCR), determines the basic configuration of the R6501 in any application. Initializing this register is one of the first actions of any software program. The Mode control Register bit assignment is shown in Figure 3-4.

3.7 INTERRUPT FLAG REGISTER (IFR) AND INTERRUPT ENABLE REGISTER (IER)

An $\overline{IRQ}$ interrupt request can be initiated by any or all of eight possible sources. These sources are all capable of being enabled or disabled by the use of the appropriate interrupt enabled bits in the Interrupt Enable Register (IER). Multiple simultaneous interrupts cause the $\overline{IRQ}$ interrupt request to remain active until all interrupting conditions have been serviced and cleared.

The Interrupt Flag Register contains the information that indicates which I/O or counter needs attention. The contents of the Interrupt Flag Register may be examined at any time by reading at address: 0011. Edge detect IFR bits may be cleared by executing a RMB instruction at address location 0010. The RMB X, (0010) instruction reads FF, modifies bit X to a "0", and writes the modified value at address location 0011. In this way IFR bits set to a "1" after the read cycle of a Read-Modify-Write instruction (such as RMB) are protected from being cleared. A logic "1" is ignored when writing to edge detect IFR bits.

Each IFR bit has a corresponding bit in the Interrupt Enable Register which can be set to a "1" by writing a "1" in the respective bit position at location 0012. Individual IER bits may be cleared by writing a "0" in the respective bit position, or by $\overline{RES}$. If set to a "1", an IRQ will be generated when the corresponding IFR bit becomes true. The Interrupt Flag Register and Interrupt Enable Register bit assignments are shown in Figure 3-5 and the functions of each bit are explained in Table 3-1.

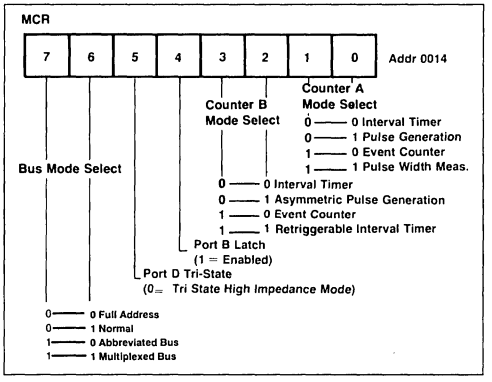


Figure 3-4. Mode Control Register

The use of Counter A Mode Select is shown in Section 6.1.

The use of Counter B Mode Select is shown in Section 6.2.

The use of Port B Latch Enable is shown in Section 4.4

The use of Port D in Tri-State Enable is shown in Section 4.6.

The use of Bus Mode Select is shown in Section 4.5 and 4.6.

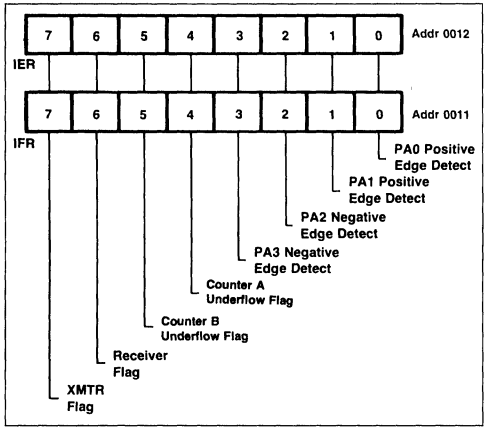


Figure 3-5. Interrupt Enable and Flag Registers

3.8 PROCESSOR STATUS REGISTER

The 8-bit Processor Status Register, shown in Figure 3-6, contains seven status flags. Some of these flags are controlled by the user program; others may be controlled both by the user's program and the CPU. The R6502 instruction set contains a number of conditional branch instructions which are designed to allow testing of these flags. Each of the eight processor status flags is described in the following sections.

3.8.1 Carry Bit (C)

The Carry Bit (C) can be considered as the ninth bit of an arithmetic operation. It is set to logic 1 if a carry from the eighth bit has occurred or cleared to logic 0 if no carry occurred as the result of arithmetic operations.

The Carry Bit may be set or cleared under program control by use of the Set Carry (SEC) or Clear Carry (CLC) instruction, respectively. Other operations which affect the Carry Bit are ADC, ASL, CMP, CPX, CPY, LSR, PLP, ROL, ROR, RTI, and SBC.

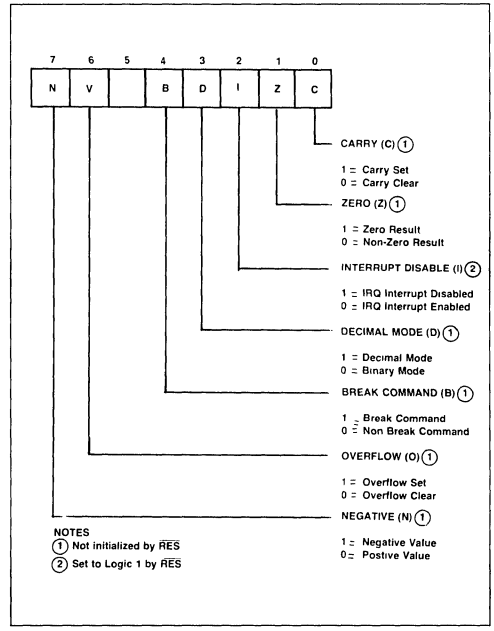


Figure 3-6. Processor Status Register

Table 3-1. Interrupt Flag Register Bit Codes

Bit Code	Function
IFR 0:	PA0 Positive Edge Detect Flag—Set to a "1" when a positive going edge is detected on PA0. Cleared by RMB O (0010) instruction or by $\overline{RES}$.
IFR 1:	PA1 Positive Edge Detect Flag—Set to a 1 when a positive going edge is detected on PA1. Cleared by RMB 1 (0010) instruction or by $\overline{RES}$.
IFR 2:	PA2 Negative Edge Detect Flag—Set to a 1 when a negative going edge is detected on PA2. Cleared by RMB 2 (0010) instruction or by $\overline{RES}$.
IFR 3:	PA3 Negative Edge Detect Flag—Set to 1 when a negative going edge is detected on PA3. Cleared by RMB 3 (0010) instruction or by $\overline{RES}$.
IFR 4:	Counter A Underflow Flag—Set to a 1 when Counter A underflow occurs. Cleared by reading the Lower Counter A at location 0018, by writing to address location 001A, or by $\overline{RES}$.
IFR 5:	Counter B Underflow Flag—Set to a 1 when Counter B underflow occurs. Cleared by reading the Lower Counter B at location 001C, by writing to address location 001E, or by $\overline{RES}$.
IFR 6:	Receiver Interrupt Flag—Set to a 1 when any of the Serial Communication Status Register bits 0 through 3 is set to a 1. Cleared when the Receiver Status bits (SCSR 0-3) are cleared or by $\overline{RES}$.
IFR 7:	Transmitter Interrupt Flag—Set to a 1 when SCSR 6 is set to a 1 while SCSR 5 is a 0 or SCSR 7 is set to a 1. Cleared when the Transmitter Status bits (SCSR 6 & 7) are cleared or by $\overline{RES}$.

3.8.2 Zero Bit (Z)

The Zero Bit (Z) is set to logic 1 by the CPU during any data movement or calculation which sets all 8 bits of the result to zero. This bit is cleared to logic 0 when the resultant 8 bits of a data movement or calculation operation are not all zero. The R6500 instruction set contains no instruction to specifically set or clear the Zero Bit. The Zero Bit is, however, affected by the following instructions; ADC, AND, ASL, BIT, CMP, CPX, CPY, DEC, DEX, DEY, EOR, INC, INX, INY, LDA, LDX, LDY, LSR, ORA, PLA, PLP, ROL, ROR, RTI, SBC, TAX, TAY, TXA, TSX, and TYA.

3.8.3 Interrupt Disable Bit (I)

The Interrupt Disable Bit (I) is used to control the servicing of an interrupt request ($\overline{IRQ}$). If the I Bit is reset to logic 0, the $\overline{IRQ}$ signal will be serviced. If the bit is set to logic 1, the $\overline{IRQ}$ signal will be ignored. The CPU will set the Interrupt Disable Bit to logic 1 if a RESET ($\overline{RES}$), $\overline{IRQ}$, or Non-Maskable Interrupt ($\overline{NMI}$) signal is detected.

The I bit is cleared by the Clear Interrupt Mask Instruction (CLI) and is set by the Set Interrupt Mask Instruction (SEI). This bit is set by the BRK Instruction. The Return from Interrupt (RTI) and Pull Processor Status (PLP) instructions will also affect the I bit.

3.8.4 Decimal Mode Bit (D)

The Decimal Mode Bit (D) is used to control the arithmetic mode of the CPU. When this bit is set to logic 1, the adder operates as a decimal adder. When this bit cleared to logic 0, the adder operates as a staight binary adder. The adder mode is controlled only by the programmer. The Set Decimal Mode (SED) instruction will set the D bit; the Clear Decimal Mode (CLD) instruction clears it. The PLP and RTI instructions also affect the Decimal Mode Bit.

CAUTION

The Decimal Mode Bit will either set or clear in an unpredictable manner upon power application. This bit must be initialized to the desired state by the user program or erroneous results may occur.

3.8.5 Break Bit (B)

The Break Bit (B) is used to determine the condition which caused the $\overline{IRQ}$ service routine to be entered. If the $\overline{IRQ}$ service routine was entered because the CPU executed a BRK command, the Break Bit will be set to logic 1. If the $\overline{IRQ}$ routine was entered as the result of an $\overline{IRQ}$ signal being generated, the B bit will be cleared to logic 0. There are no instructions which can set or clear this bit.

3.8.6 Overflow Bit (V)

The Overflow Bit (V) is used to indicate that the result of a signed, binary addition, or subtraction, operation is a value that cannot be contained in seven bits ($-128 \leq n \leq 127$). This indicator only has meaning when signed arithmetic (sign and seven magnitude bits) is performed. When the ADC or SBC instruction is performed, the Overflow Bit is set to logic 1 if the polarity of the sign bit (bit 7) is changed because the result exceeds +127 or −128; otherwise the bit is cleared to logic 0. The V bit may also be cleared by the programmer using a Clear Overflow (CLV) instruction.

The Overflow Bit may also be used with the BIT instruction. The BIT instruction—which may be used to sample interface devices—allows the overflow flag to reflect the condition of bit 6 in the sampled field. During a BIT instruction the Overflow Bit is set equal to the content of the bit 6 on the data tested with BIT instruction. When used in this mode, the overflow has nothing to do with signed arithmetic, but is just another sense bit for the microprocessor. Instructions affecting the V flag are ADC, BIT, CLV, PLP, RTI and SBC.

3.8.7 Negative Bit (N)

The Negative Bit (N) is used to indicate that the sign bit (bit 7) in the resulting value of a data movement or data arithmetic operation is set to logic 1. If the sign bit is set to logic 1, the resulting value of the data movement or arithmetic operation is negative; if the sign bit is cleared, the result of the data movement or arithmetic operation is positive. There are no instructions that set or clear the Negative Bit since the Negative Bit represents only the status of a result. The instructions that effect the state of the Negative Bit are: ADC, AND, ASL, BIT, CMP, CPX, CPY, DEC, DEX, DEY, EOR, INC, INX, INY, LDA, LDX, LDY, LSR, ORA, PLA, PLP, ROL, ROR, RTI, SBC, TAX, TAY, TSX, TXA, and TYA.

SECTION 4
PARALLEL INPUT/OUTPUT PORTS & BUS MODES

The devices have 32 I/O lines grouped into four 8-bit ports (PA, PB, PC, and PD). Ports A through C may be used either for input or output individually or in groups of any combination. Port D may be used as all inputs or all outputs.

Multifunction I/O's such as Port A and Port C are protected from normal port I/O instructions when they are programmed to perform a multiplexed function.

Internal pull-up resistors (FET's with an impedance range of $3K \leq R_L \leq 12K$ ohm) are provided on all port pins except Port D.

The direction of the 32 I/O lines is controlled by four 8-bit port registers located in page zero. This arrangement provides quick programming access using simple two-byte zero page address instructions. There are no direction registers associated with the I/O ports, thus simplifying I/O handling. The I/O addresses are shown in Table 4-1. Appendix E.4 shows the I/O Port Timing.

Table 4-1. I/O Port Addresses

Port	Address
A	0000
B	0001
C	0002
D	0003

4.1 INPUTS

Inputs for Ports A, B, and C are enabled by loading logic 1 into all I/O port register bit positions that are to correspond to I/O input lines. A low (<0.8V) input signal will cause a logic 0 to be read when a read instruction is issued to the port register. A high (>2.0V) input will cause a logic 1 to be read. An $\overline{RES}$ signal forces all I/O port registers to logic 1 thus initially treating all I/O lines as inputs.

Port D may only be all inputs or all outputs. All inputs is selected by setting bit 5 of the Mode Control Register (MCR5) to a "0".

The status of the input lines can be interrogated at any time by reading the I/O port addresses. Note that this will return the actual status of the input lines, not the data written into the I/O port registers.

Read/Modify/Write instructions can be used to modify the operation of PA, PB, PC, & PD. During the Read cycle of a Read/Modify/Write instruction the Port I/O register is read. For all other read instructions the port input lines are read. Read/Modify/Write instructions are: ASL, DEC, INC, LSR, RMB, ROL, ROR, and SMB.

4.2 OUTPUTS

Outputs for Ports A thru D are controlled by writing the desired I/O line output states into the corresponding I/O port register bit positions. A logic 1 will force a high (>2.4V) output while a logic 0 will force a low (<0.4V) output.

Port D all outputs is selected by setting MCR5 to a "1".

4.3 Port A (PA)

Port A can be programmed via the Mode Control Register (MCR) and the Serial Communications Control Register (SCCR) as a standard parallel 8-bit, bit independent, I/O port or as serial channel I/O lines, counter I/O lines, or an input data strobe for the Port B input latch option. Table 4-2 tabulates the control and usage of Port A.

In addition to their normal I/O functions, PA0 and PA1 can detect positive going edges and PA2 and PA3 can detect negative going edges. A proper transition on these pins will set a corresponding status bit in the IFR and generate an interrupt request if the respective Interrupt Enable Bit is set. The maximum rate at which an edge can be detected is one-half the $\phi 2$ clock rate. Edge detection timing is shown in Appendix E.3.

Table 4-2. Port A Control and Usage

PA0 (2)	PA0 I/O		PORT B LATCH MODE	
	MCR4 = 0		MCR4 = 1	
	SIGNAL		SIGNAL	
	NAME	TYPE	NAME	TYPE
	PA0	I/O	PORT B LATCH STROBE	INPUT (1)

PA1 (2) **PA2 (3)** **PA3 (3)**	PA1-PA3 I/O	
	SIGNAL	
	NAME	TYPE
	PA1 PA2 PA3	I/O I/O I/O

PA4	PA4 I/O		COUNTER A I/O			
	MCR0 = 0 MCR1 = 0 SCCR7 = 0 RCVR S/R MODE = 0 (4) (5)		MCR0 = 1 MCR1 = 0 SCCR7 = 0 RCVR S/R MODE = 0 (4)		SCCR7 = 0 SCCR6 = 0 MCR1 = 1	
	SIGNAL		SIGNAL		SIGNAL	
	NAME	TYPE	NAME	TYPE	NAME	TYPE
	PA4	I/O	CNTA	OUTPUT	CNTA	INPUT (1)
	SERIAL I/O SHIFT REGISTER CLOCK					
	SCCR7 = 1 SCCR5 = 1			RCVR S/R MODE = 1 (4)		
	SIGNAL			SIGNAL		
	NAME	TYPE		NAME	TYPE	
	XMTR CLOCK	OUTPUT		RCVR CLOCK	INPUT (1)	

PA5	PA5 I/O		COUNTER B I/O			
	MCR3 = 0 MCR2 = 0		MCR3 = 0 MCR2 = 1		MCR3 = 1 MCR2 = X	
	SIGNAL		SIGNAL		SIGNAL	
	NAME	TYPE	NAME	TYPE	NAME	TYPE
	PA5	I/O	CNTB	OUTPUT	CNTB	INPUT (1)

PA6	PA6 I/O		SERIAL I/O XMTR OUTPUT	
	SCCR7 = 0		SCCR7 = 1	
	SIGNAL		SIGNAL	
	NAME	TYPE	NAME	TYPE
	PA6	I/O	XMTR	OUTPUT

PA7	PA7 I/O		SERIAL I/O RCVR INPUT	
	SCCR6 = 0		SCCR6 = 1	
	SIGNAL		SIGNAL	
	NAME	TYPE	NAME	TYPE
	PA7	I/O	RCVR	INPUT (1)

(1) HARDWARE BUFFER FLOAT
(2) POSITIVE EDGE DETECT
(3) NEGATIVE EDGE DETECT
(4) RCVR S/R MODE = 1 WHEN SCCR6 · $\overline{\text{SCCR5}}$ · SCCR4 = 1
(5) For the following mode combinations PA4 is available as an Input Only pin:
$\overline{\text{SCCR7}}$•SCCR6•$\overline{\text{SCCR5}}$•MCR1
+ $\overline{\text{SCCR7}}$•$\overline{\text{SCCR6}}$•$\overline{\text{SCCR4}}$•MCR1
+ SCCR7•$\overline{\text{SCCR6}}$•$\overline{\text{SCCR5}}$
+ SCCR7•$\overline{\text{SCCR5}}$•$\overline{\text{SCCR4}}$•

4.4 PORT B (PB)

Port B can be programmed as an 8-bit, bit-independent I/O port. It has a latched input capability which may be enabled or disabled via the Mode Control Register (MCR). Table 4-3 tabulates the control and usage of Port B. An Input Data Strobe signal must be provided thru PA0 when Port B is programmed to be used with latched input option. Input data latch timing for Port B is shown in Appendix E.5.

Table 4-3. Port B Control & Usage

		I/O Mode		Latch Mode	
		MCR4 = 0		MCR4 = 1 (2)	
		Signal		Signal	
Pin #	Pin Name	Name	Type (1)	Name	Type
31	PB0	PB0	I/O	PB0	INPUT
30	PB1	PB1	I/O	PB1	INPUT
29	PB2	PB2	I/O	PB2	INPUT
28	PB3	PB3	I/O	PB3	INPUT
27	PB4	PB4	I/O	PB4	INPUT
26	PB5	PB5	I/O	PB5	INPUT
25	PB6	PB6	I/O	PB6	INPUT
24	PB7	PB7	I/O	PB7	INPUT

(1) Resistive Pull-Up, Active Buffer Pull-Down
(2) Input data is stored in Port B latch by PA0 Pulse

4.5 PORT C (PC)

Port C can be programmed as an I/O port, as part of the full address bus, and, in conjunction with Port D, as an abbreviated bus, or as a multiplexed bus. When operating in the Full Address Mode PC6 and PC7 serve as A13 and A14 with PC0-PC5 operating as normal I/O pins. When used in the abbreviated or multiplexed bus modes, PC0-PC7 function as A0-A3, A12, R/W, A13, and $\overline{EMS}$, respectively, as shown in Table 4-4. $\overline{EMS}$ (External Memory Select) is asserted (low) whenever the internal processor accesses memory area between 0100 and 3FFF. (See Memory Map, Appendix B). The leading edge of $\overline{EMS}$ may be used to strobe the eight address lines multiplexed on Port D in the Multiplexed Bus Mode. See Appendices E.3 through E.5 for Port C timing.

4.6 PORT D (PD)

Port D can be programmed as an I/O Port, an 8-bit tri-state data bus, or as a multiplexed bus. Mode selection for Port D is made by the Mode Control Register (MCR). The Port D output drivers can be selected as tri-state drivers by setting bit 5 of the MCR to 1 (one). Table 4-5 shows the necessary settings for the MCR to achieve the various modes for Port D. When Port D is selected to operate in the Abbreviated Mode PD0–PD7 serves as data register bits D0–D7. When Port D is selected to operate in the Multiplexed Mode data bits D0 through D7 are time multiplexed with address bits A4 through A11, respectively. Refer to the Memory Maps (Appendix C) for Abbreviated and Multiplexed memory assignments. See Appendices E.3 through E.5 for Port D timing.

4.7 BUS MODES

A special attribute of Port C and Port D is their capability to be configured via the Mode Control Register (see Section 3.6) into four different modes.

In the Full Address Mode, the separate address and data bus are used in conjunction with PC6 and PC7, which automatically provide A13 and A14. The remaining ports perform the normal I/O function.

In the I/O Bus Mode all ports serve as I/O. The address and data bus are still functional but without A13 and A14. Since the internal RAM and registers are in the 00XX location, A15 can be used for chip select and A0–A12 used for selecting 8K of external memory.

In the Abbreviated Bus Mode, the address and data lines can be used as in the I/O Bus Mode to emulate the R6500/11. Port C and Port D are automatically transformed into an abbreviated address bus and control signals (Port C) and a bidirectional data bus (Port D). 64 Peripheral addresses can be selected. In general usage, these 64 addresses would be distributed to several external I/O devices such as R6522 and R6520, etc., each of which may contain more than one unique address.

In the Multiplexed Bus Mode, the operation is similar to the Abbreviated Mode except that a full 16K of external addresses are provided. Port C provides the lower addresses and control signals. Port D multiplexes functions. During the first half of the cycle it contains the remaining necessary 8 address bits for 16K; during the second half of the cycle it contains a bidirectional data bus. The address bits appearing on Port D must be latched into an external holding register. The leading edge of $\overline{EMS}$ which indicates that the bus function is active, may be used for this purpose.

MCR5 must be a logic 1 in the Abbreviated and Multiplexed Bus Modes.

Figures 4-1a through 4-1d show the possible configurations of the four bus modes. Figure 4-2 shows a memory map of the part as a function of the Bus Mode and further shows which adddresses are active or inactive on each of the three possible buses.

Table 4-4. Port C Control & Usage

	Full Address Mode		Normal Mode		Abbreviated Mode		Multiplexed Mode	
	MCR7 = 0 MCR6 = 0		MCR7 = 0 MCR6 = 1		MCR7 = 1 MCR6 = 0		MCR7 = 1 MCR6 = 1	
	Signal		Signal		Signal		Signal	
Pin Name	Name	Type	Name	Type (1)	Type Name	(2)	Type Name	(2)
PC0	PC0	I/O (1)	PC0	I/O	A0	OUTPUT	A0	OUTPUT
PC1	PC1	I/O (1)	PC1	I/O	A1	OUTPUT	A1	OUTPUT
PC2	PC2	I/O (1)	PC2	I/O	A2	OUTPUT	A2	OUTPUT
PC3	PC3	I/O (1)	PC3	I/O	A3	OUTPUT	A3	OUTPUT
PC4	PC4	I/O (1)	PC4	I/O	A12	OUTPUT	A12	OUTPUT
PC5	PC5	I/O (1)	PC5	I/O	R/W	OUTPUT	R/W	OUTPUT
PC6	A13	OUTPUT (2)	PC6	I/O	A13	OUTPUT	A13	OUTPUT
PC7	A14	OUTPUT (2)	PC7	I/O	EMS	OUTPUT	EMS	OUTPUT

(1) Resistive Pull-Up, Active Buffer Pull-Down
(2) Active Buffer Pull-Up and Pull-Down

3

Table 4-5. Port D Control & Usage

	Normal Mode				Abbreviated Mode		Multiplexed Mode			
	MCR7 = 0 MCR6 = X MCR5 = 0		MCR7 = 0 MCR6 = X MCR5 = 1		MCR7 = 1 MCR6 = 0 MCR5 = 1		MCR7 = 1 MCR6 = 1 MCR5 = 1			
	Signal		Signal		Signal		Signal		Signal	
							ϕ2 Low		ϕ2 High	
Pin Name	Name	Type (1)	Name	Type (2)	Name	Type (3)	Name	Type (2)	Name	Type (3)
PD0	PD0	INPUT	PD0	OUTPUT	DATA0	I/O	A4	OUTPUT	DATA0	I/O
PD1	PD1	INPUT	PD1	OUTPUT	DATA1	I/O	A5	OUTPUT	DATA1	I/O
PD2	PD2	INPUT	PD2	OUTPUT	DATA2	I/O	A6	OUTPUT	DATA2	I/O
PD3	PD3	INPUT	PD3	OUTPUT	DATA3	I/O	A7	OUTPUT	DATA3	I/O
PD4	PD4	INPUT	PD4	OUTPUT	DATA4	I/O	A8	OUTPUT	DATA4	I/O
PD5	PD5	INPUT	PD5	OUTPUT	DATA5	I/O	A9	OUTPUT	DATA5	I/O
PD6	PD6	INPUT	PD6	OUTPUT	DATA6	I/O	A10	OUTPUT	DATA6	I/O
PD7	PD7	INPUT	PD7	OUTPUT	DATA7	I/O	A11	OUTPUT	DATA7	I/O

(1) Tri-State Buffer is in High Impedance Mode
(2) Tri-State Buffer is in Active Mode
(3) Tri-State Buffer is in Active Mode only during the phase 2 portion of a Write Cycle

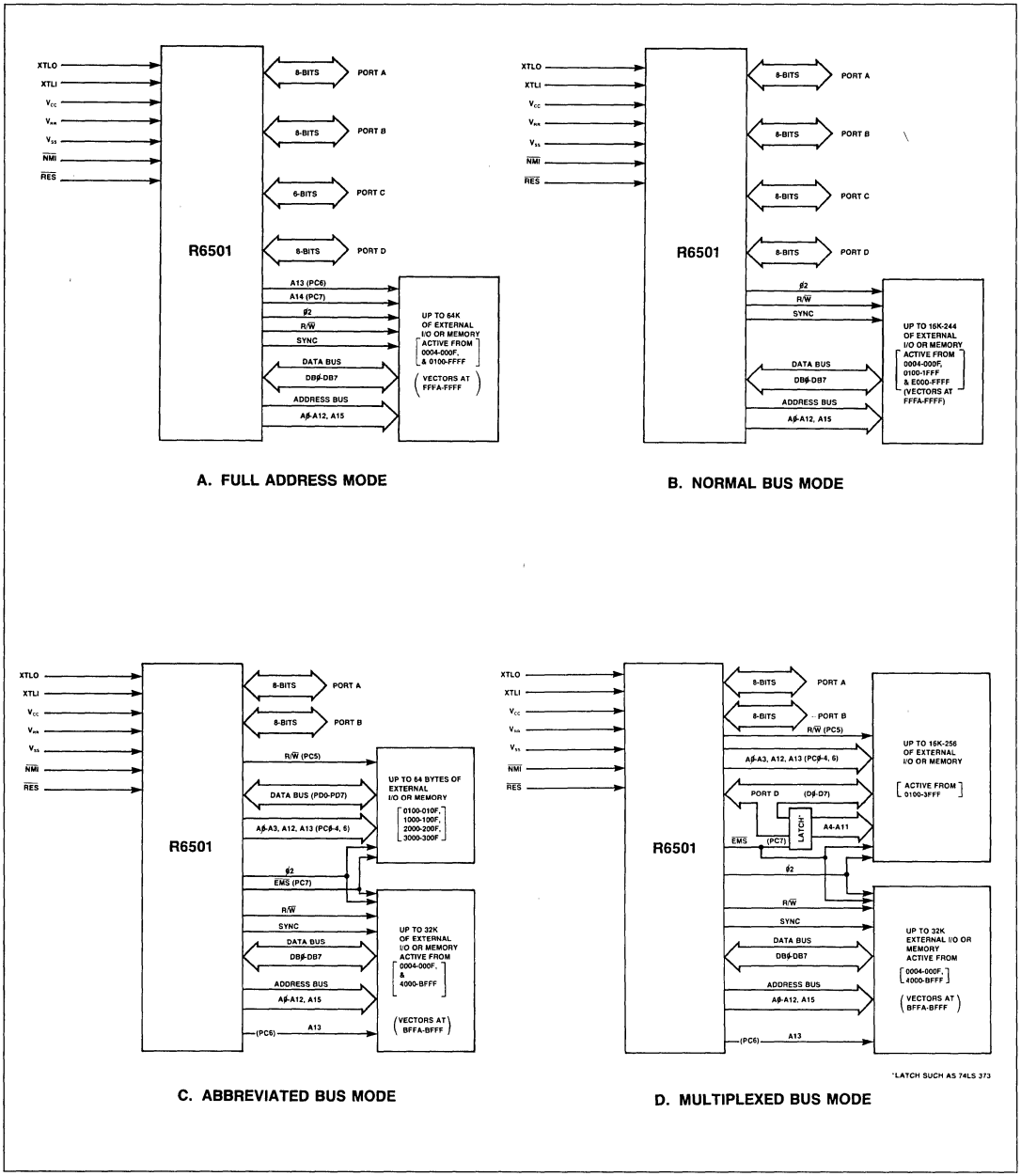


Figure 4-1. R6501 Bus Mode Configurations

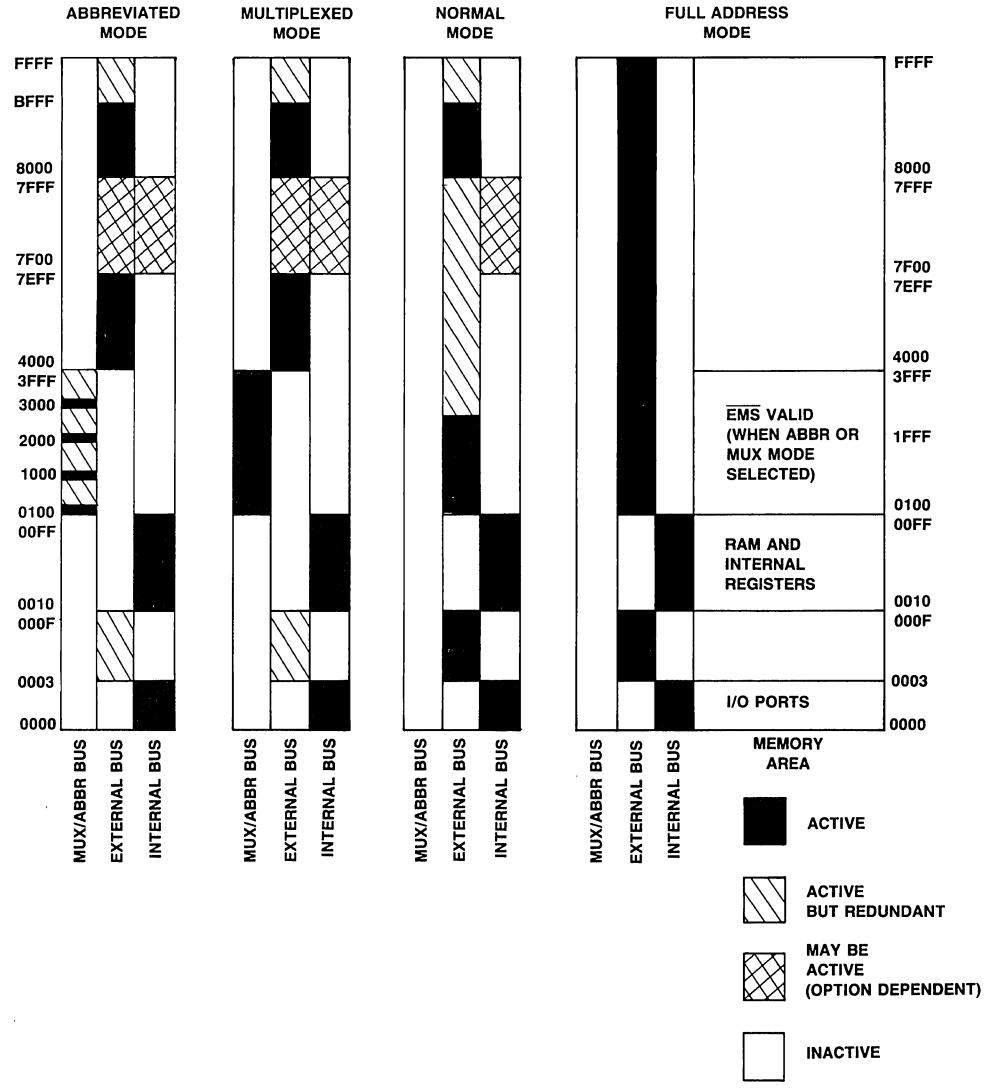


Figure 4-2. R6501 Memory Map

SECTION 5
SERIAL INPUT/OUTPUT CHANNEL

The device provides a full duplex Serial I/O channel with programmable bit rates and operating modes. The serial I/O functions are controlled by the Serial Communication Control Register (SCCR). The SCCR bit assignment is shown in Figure 5-1. The serial bit rate is determined by Counter A for all modes except the Receiver Shift Register (RCVR S/R) mode for which an external shift clock must be provided. The maximum data rate using the internal clock is 62.5K bits per second (at $\phi 2$ = 1 MHZ). The transmitter (XMTR) and receiver (RCVR) can be independently programmed to operate in different modes and can be independently enabled or disabled.

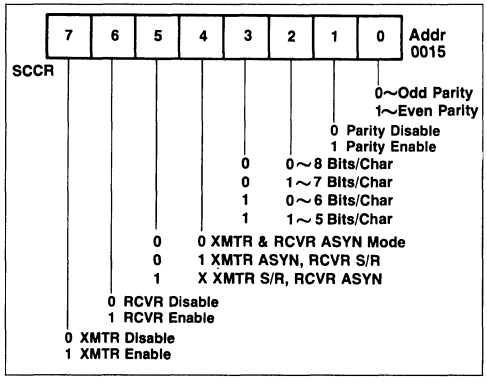


Figure 5-1. Serial Communication Control Register

Except for the Receiver Shift Register Mode (RCVR S/R), all XMTR and RCVR bit rates will occur at one sixteenth of the Counter A interval timer rate. Counter A is forced into an interval timer mode whenever the serial I/O is enabled in a mode requiring an internal clock.

Whenever Counter A is required as a timing source it must be loaded with the hexadecimal code that selects the data rate for the serial I/O Port. Refer to Counter A (paragraph 6.1) for a table of hexadecimal values to represent the desired data rate.

5.1 TRANSMITTER OPERATION (XTMR)

The XTMR operation and the transmitter related control/status functions are enabled by bit 7 of the Serial Communications Control Register (SCCR). The transmitter, when in the Asynchronous (ASYN) mode, automatically adds a start bit, one or two stop bits, and, when enabled, a parity bit to the transmitted data. A word of transmitted data (in asynchronous parity mode) can have 5, 6, 7, or 8 bits of data. The nine data modes are shown in Figure 5-2. When parity is disabled, the 5, 6, 7 or 8 bits of data are terminated with two stop bits.

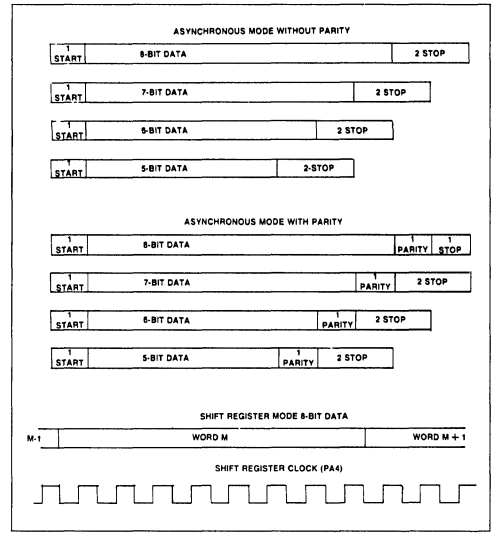


Figure 5-2. SIO Data Modes

In the S/R mode, eight data bits are always shifted out. Bits/character and parity control bits are ignored. The serial data is shifted out via the SO output (PA6) and the shift clock is available at the CA (PA4) pin. When the transmitter underruns in the S/R mode the SO output and shift clock are held in a high state.

The XMTR Interrupt Flag bit (IFR7) is controlled by Serial Communication Status Register bits SCSR5, SCSR6 and SCSR7.

$$IFR7 = SCSR6\ (\overline{SCSR5} + SCSR7)$$

5.2 RECEIVER OPERATION (RCVR)

The receiver and its selected control and status functions are enabled when SCCR-6 is set to a "1." In the ASYN mode, data format must have a start bit, the appropriate number of data bits, a parity bit (if enabled), and one stop bit. Refer to paragraph 5.1 for a diagram of bit allocations. The receiver bit period is divided into 8 sub-intervals for internal synchronization. The receiver bit stream is synchronized by the start bit and a strobe signal is generated at the approximate center of each incoming bit. Refer to Figure 5-3 for ASYN Receive Data Timing. The character assembly process does not start if the start bit signal is less than one-half the bit time after a low level is detected on the Receive Data Input. Framing error, over-run, and parity error conditions or a RCVR Data Register Full will set the appropriate status bits. Any of the above conditions will cause an Interrupt Request if the Receiver Interrupt Enable bit is set to logic 1.

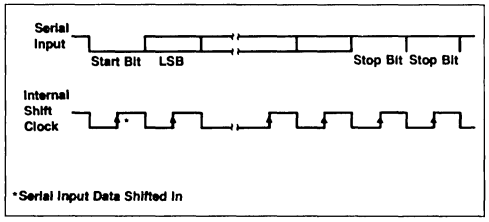


Figure 5-3. ASYN Receive Data Timing

In the S/R mode, an external shift clock must be provided at CA (PA4) pin along with 8 bits of serial data (LSB first) at the SI input (PA7). The maximum data rate using an external shift clock is one-eighth the internal clock rate. Refer to Figure 5-4 for S/R Mode Timing.

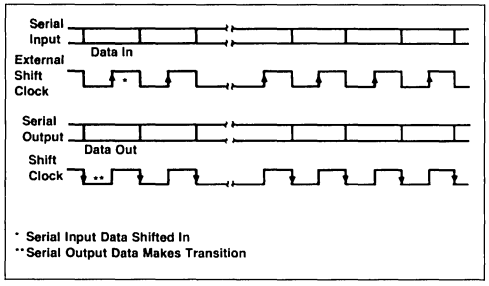


Figure 5-4. S/R Mode Timing

A RCVR interrupt (IFR6) is generated whenever any of SCSR0-3 are true.

5.3 SERIAL COMMUNICATION STATUS REGISTER (SCSR)

The Serial Communication Status Register (SCSR) holds information on various communication error conditions, status of the transmitter and receiver data registers, a transmitter end-of-transmission condition, and a receiver idle line condition (Wake-Up Feature). The SCSR bit assignment is shown in Figure 5-5. Bit assignments and functions of the SCSR are as follows:

SCSR 0: *Receiver Data Register Full*—Set to a logic 1 when a character is transferred from the Receiver Shift Register to the Receiver Data Register. This bit is cleared by reading the Receiver Data Register, or by $\overline{RES}$ and is disabled if SCCR 6 = 0. The SCSR 0 bit will not be set to a logic 1 if the received data contains an error condition; instead, a corresponding error bit will be set to a logic 1.

SCSR 1: *Over-Run Error*—Set to a logic 1 when a new character is transferred from the Receiver Shift Register with the last character still in the Receiver Data Register. This bit is cleared by reading the Receiver Data Register or by $\overline{RES}$.

SCSR 2: *Parity Error*—Set to logic 1 when the RCVR is in the ASYN Mode, Parity Enable bit is set, and the received data has a parity error. This bit is cleared by reading the Receiver Data Register or by $\overline{RES}$.

SCSR 3: *Framing Error*—Set to a logic 1 when the received data contains a zero bit after the last data or parity bit in the stop bit slot. Cleared by reading the Receiver Data Register or by $\overline{RES}$ (ASYN Mode only).

SCSR 4: *Wake-Up*—Set to a logic 1 by writing a "1" in bit 4 of address: 0016. The Wake-Up bit is cleared by $\overline{RES}$ or when the receiver detects a string of ten consecutive 1's. When the Wake-Up bit is set SCSR0 through SCSR3 are inhibited.

SCSR 5: *End of Transmission*—Set to a logic 1 by writing a "1" in bit position 5 of address: 0016. The End of Transmission bit is cleared by $\overline{RES}$ or upon writing a new data word into the Transmitter Data Register. When the End-of-Transmission bit is true the Transmitter Register Empty bit is disabled until a Transmitter Under-Run occurs.

SCSR 6: *Transmitter Data Register Empty*—Set to a logic 1 when the contents of the Transmitter Data Register are transferred to the Transmitter Shift Register. Cleared upon writing new data into the Transmit Data Register. This bit is initialized to a logic 1 by $\overline{RES}$.

SCSR 7: *Transmitter Under-Run*—Set to a logic 1 when the last data bit is transmitted if the transmitter is in a S/R Mode or when the last stop bit is transmitted if the XMTR is in the ASYN Mode while the Transmitter Data Register Empty Bit is set. Cleared by a transfer of new data into the Transmitter Shift Register or by $\overline{RES}$.

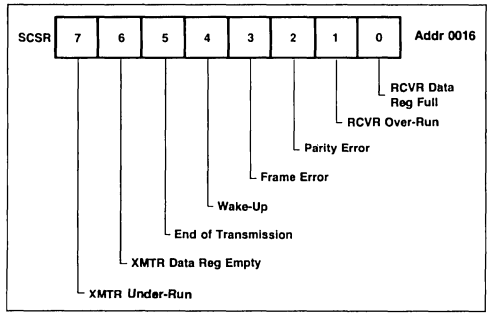


Figure 5-5. SCSR Bit Allocations

5.4 WAKE-UP FEATURE

In a multi-distributed microprocessor or microcomputer applications, a destination address is usually included at the beginning of the message. The Wake-Up Feature allows non-selected CPU's to ignore the remainder of the message until the beginning of the next message by setting the Wake-Up bit. As long as the Wake-Up flag is true, the Receiver Data Register Full Flag remains false. The Wake-Up bit is automatically cleared when the receiver detects a string of eleven consecutive 1's which indicates an idle transmit line. When the next byte is received, the Receiver Data Register Full Flag signals the CPU to wake-up and read the received data.

SECTION 6
COUNTER/TIMERS

The device contains two 16-bit counters (Counter A and Counter B) and three 16-bit latches associated with the counters. Counter A has one 16-bit latch and Counter B has two 16-bit latches. Each counter can be independently programmed to operate in one of four modes:

Counter A	Counter B
• Pulse width measurement	• Retriggerable Interval Counter
• Pulse Generation	• Asymmetrical Pulse Generation
• Interval Timer	• Interval Timer
• Event Counter	• Event Counter

Operating modes of Counter A and Counter B are controlled by the Mode Control Register. All counting begins at the initialization value and decrements. When modes are selected requiring a counter input/output line, PA4 is automatically selected for Counter A and PA5 is automatically selected for Counter B (see Table 4.2).

6.1 COUNTER A

Counter A consists of a 16-bit counter and a 16-bit latch organized as follows: Lower Counter A (LCA), Upper Counter A (UCA), Lower Latch A (LLA), and Upper Latch A (ULA). The counter contains the count of either $\phi 2$ clock pulses or external events, depending on the counter mode selected. The contents of Counter A may be read any time by executing a read at location 0019 for the Upper Counter A and at location 001A or location 0018 for the Lower Counter A. A read at location 0018 also clears the Counter A Underflow Flag (IFR4).

The 16-bit latch contains the counter initialization value and can be loaded at any time by executing a write to the Upper Latch A at location 0019 and the Lower Latch A at location 0018. In either case, the contents of the accumulator are copied into the applicable latch register.

Counter A can be started at any time by writing to address: 001A. The contents of the accumulator will be copied into the Upper Latch A before the contents of the 16-bit latch are transferred to Counter A. Counter A is set to the latch value whenever Counter A underflows. When Counter A decrements from 0000 the next counter value will be the latch value—not FFFF—and the Counter A Underflow Flag (IFR 4) will be set to "1". This bit may be cleared by reading the Lower Counter A at location 0018, by writing to address location 001A, or by $\overline{RES}$.

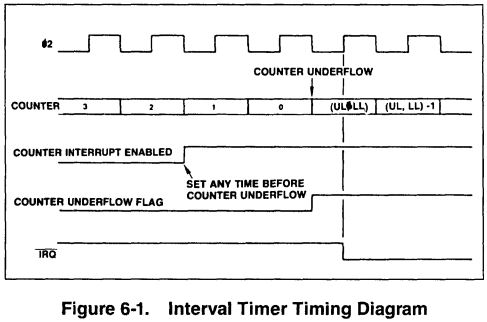


Figure 6-1. Interval Timer Timing Diagram

Counter A operates in any of four modes. These modes are selected by the Counter A Mode Control bits in the Control Register.

MCR1 (bit 1)	MCR0 (bit 0)	Mode
0	0	Interval Timer
0	1	Pulse Generation
1	0	Event Counter
1	1	Pulse Width Measurement

The Interval Timer, Pulse Generation, and Pulse Width Measurement Modes are $\phi 2$ clock counter modes. The Event Counter Mode counts the occurrences of an external event on the CNTR line.

The Counter is set to the Interval Timer Mode (00) when a $\overline{RES}$ signal is generated.

6.1.1 Interval Timer

In the Interval Timer mode the Counter is initialized to the Latch value by either of two conditions:

1. When the Counter is decremented from 0000, the next Counter value is the Latch value (not FFFF).

2. When a write operation is performed to the Load Upper Latch and Transfer Latch to Counter address 001A, the Counter is loaded with the Latch value. Note that the contents of the Accumulator are loaded into the Upper Latch before the Latch value is transferred to the Counter.

The Counter value is decremented by one count at the 02 clock rate. The 16-bit Counter can hold from 1 to 65535 counts. The Counter Timer capacity is therefore 1μs to 65,535 ms at the 1 MHz $\phi 2$ clock rate or 0.5 μs to 32.767 ms at the 2 MHz $\phi 2$ clock rate. Time intervals greater than the maximum Counter value can be easily measured by counting $\overline{IRQ}$ interrupt requests in the counter $\overline{IRQ}$ interrupt routine.

When Counter A decrements from 0000, the Counter A Underflow (IFR4) is set to logic 1. If the Counter A Interrupt Enable Bit (IER4) is also set, an $\overline{IRQ}$ interrupt request will be generated. The Counter A Underflow bit in the Interrupt Flag Register can be examined in the $\overline{IRQ}$ interrupt routine to determine that the $\overline{IRQ}$ was generated by the Counter A Underflow.

While the timer is operating in the Interval Timer Mode, PA4 operates as a PA I/O bit.

A timing diagram of the Interval Timer Mode is shown in Figure 6-1.

6.1.2 Pulse Generation Mode

In the Pulse Generation mode, the CA line operates as a Counter Output. The line toggles from low to high or from high to low whenever a Counter A Underflow occurs or a write is performed to address 001A.

The normal output waveform is a symmetrical square-wave. The CA output is initialized high when entering the mode and transitions low when writing to 001A.

Asymmetric waveforms can be generated if the value of the latch is changed after each counter underflow.

A one-shot waveform can be generated by changing from Pulse Generation to Interval Timer mode after only one occurrence of the output toggle condition.

6.1.3 Event Counter Mode

In this mode the CA is used as an Event Input line, and the Counter will decrement with each rising edge detected on this line. The maximum rate at which this edge can be detected is one-half the $\phi 2$ clock rate.

The Counter can count up to 65,535 occurrences before underflowing. As in the other modes, the Counter A Underflow bit (IER4) is set to logic 1 if the underflow occurs.

Figure 6.2 is a timing diagram of the Event Counter Mode.

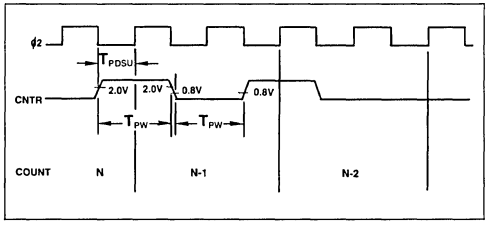


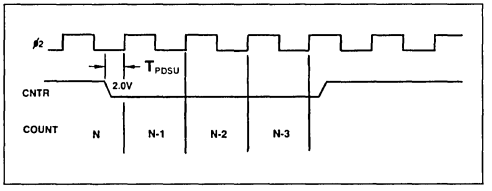
Figure 6-2. Event Counter Mode

6.1.4 Pulse Width Measurement Mode

This mode allows the accurate measurement of a low pulse duration on the CA line. The Counter decrements by one count at the $\phi 2$ clock rate as long as the CA line is held in the low state. The Counter is stopped when CA is in the high state.

The Counter A underflow flag will be set only when the count in the timer reaches zero. Upon reaching zero the timer will be loaded with the latch value and continue counting down as long as the CA pin is held low. After the counter is stopped by a high level on CA, the count will hold as long as CA remains high. Any further low levels on CA will again cause the counter to count down from its present value. The state of the CA line can be determined by testing the state of PA4.

A timing diagram for the Pulse Width Measurement Mode is shown in Figure 6.3.



6-3. Pulse Width Measurement

6.1.5 Serial I/O Data Rate Generation

Counter A also provides clock timing for the Serial I/O which establishes the data rate for the Serial I/O port. When the Serial I/O is enabled, Counter A is forced to operate at the internal clock rate. Counter A is not required for the RCVR S/R mode. The Counter I/O (PA4) may also be required to support the Serial I/O (see Table 4-2).

Table 6-1 identifies the values to be loaded in Counter A for selecting standard data rates with a $\phi 2$ clock rate of 1 MHz and 2 MHz. Although Table 6-1 identifies only the more common data rates, any data rate from 1 to 62.5K bps can be selected by using the formula:

$$N = \frac{\phi 2}{16 \times bps} - 1$$

where

N = decimal value to be loaded into Counter A using its hexadecimal equivalent.
$\phi 2$ = the clock frequency (1 MHz or 2 MHz)
bps = the desired data rate.

NOTE

In Table 6-1 you will notice that the standard data rate and the actual data rate may be slightly different. Transmitter and receiver errors of 1.5% or less are acceptable. A revised clock rate is included in Table 6-1 for those baud rates which fall outside this limit.

Table 6-1. Counter A Values for Baud Rate Selection

STANDARD BAUD RATE	HEXADECIMAL VALUE		03 ACTUAL BAUD RATE AT		CLOCK RATE NEEDED TO GET STANDARD BAUD RATE	
	1 MHz	2 MHz	1 MHz	2 MHz	1 MHz	2 MHz
50	04E1	09C3	50.00	50.00	1.0000	2.0000
75	0340	0682	75.03	74.99	1.0000	2.0000
110	0237	046F	110.04	110.04	1.0000	2.0000
150	01A0	0340	149.88	150.06	1.0000	2.0000
300	00CF	01A0	300.48	299.76	1.0000	2.0000
600	0067	00CF	600.96	600.96	1.0000	2.0000
1200	0033	0067	1201.92	1201.92	1.0000	2.0000
2400	0019	0033	2403.85	2403.85	1.0000	2.0000
3600	0010	0021	3676.47	3676.47	0.9792	1.9584
4800	000C	0019	4807.69	4807.69	1.0000	2.0000
7200	0008	0010	6944.44	7352.94	1.0368	1.9584
9600	0006	000C	8928.57	9615.38	1.0752	2.0000

6.2 COUNTER B

Counter B consists of a 16-bit counter and two 16-bit latches organized as follows: Lower Counter B (LCB), Upper Counter B (UCB), Lower Latch B (LLB), Upper Latch B (ULB), Lower Latch C (LLC), and Upper Latch C (ULC). Latch C is used only in the asymmetrical pulse generation mode. The counter contains the count of either Ø2 clock pulses or external events depending on the counter mode selected. The contents of Counter B may be read any time by executing a Read at location 001D for the Upper Counter B and at location 001E or 001C for the Lower Counter B. A Read at location 001C also clears the Counter B Underflow Flag.

Latch B contains the counter initialization value and can be loaded at any time by executing a Write to the Upper Latch B at location 001D and the Lower Latch B at location 001C. In each case, the contents of the accumulator are copied into the applicable latch register.

Counter B can be initialized at any time by writing to address: 001E. The contents of the accumulator is copied into the Upper Latch B before the value in the 16-bit Latch B is transferred to Counter B. Counter B will also be set to the latch value and the Counter B Underflow Flag bit (IFR5) will be set to a "1" whenever Counter B underflows by decrementing from 0000.

IFR 5 may be cleared by reading the Lower Counter B at location 001C, by writing to address location 001E, or by $\overline{RES}$.

Counter B operates in the same manner as Counter A in the Interval Timer and Event Counter modes. The Pulse Width Measurement Mode is replaced by the Retriggerable Interval Timer mode and the Pulse Generation mode is replaced by the Asymmetrical Pulse Generation Mode. Mode Control Register bits MCR2 and MCR3 select the four Counter B modes in a similar manner and coding as MCR0 and MCR1 select the modes of Counter A.

6.2.1 Retriggerable Interval Timer Mode

When operating in the Retriggerable Interval Timer mode, Counter B is initialized to the latch value by writing to address 001E, by a Counter B underflow, or whenever a positive edge occurs on the CB pin (PA5). The Counter B interrupt flag will be set if the counter underflows before a positive edge occurs on the CB line. Figure 6-4 illustrates the operation.

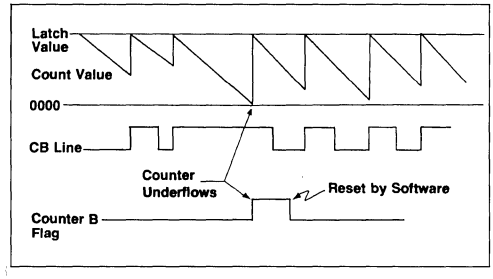


Figure 6-4. Counter B Retriggerable Interval Timer Mode

6.2.2 Asymmetrical Pulse Generation Mode

Counter B has a special Asymmetrical Pulse Generation Mode whereby a pulse train with programmable pulse width and period can be generated without the processor intervention once the latch values are initialized.

In this mode, the 16-bit Latch B is initialized with a value which corresponds to the duration between pulses (referred to as D in the following descriptions). The 16-bit Latch C is initialized with a value corresponding to the desired pulse width (referred to as P in the following descriptions). The initialization sequence for Latch B and C and the starting of a counting sequence are as follows:

1. The lower 8 bits of P are loaded into LLB by writing to address 001C; the upper 8 bits of P are loaded into ULB and the full 16 bits are transferred to Latch C by writing to address location 001D. At this point both Latch B and Latch C contain the value of P.

2. The lower 8 bits of D are loaded into LLB by writing to address 001C; the upper 8 bits of D are loaded into ULB by writing to address location 001E. Writing to address location 001E also causes the contents of the 16-bit Latch B to be downloaded into the Counter B and the CB output to go low as shown in Figure 6-5.

3. When Counter B underflow occurs the contents of the Latch C are loaded into the Counter B and the CB output toggles to a high level, staying high until another underflow occurs. Latch B is then down-loaded and the CB output toggles to a low level repeating the whole process.

SECTION 7
POWER ON/INITIALIZATION CONSIDERATIONS

7.1 POWER ON TIMING

After application of V_{CC} and V_{RR} power to the device, $\overline{RES}$ must be held low for at least eight $\phi 2$ clock cycles after V_{CC} reaches operating range and the internal oscillator has stabilized. This stabilization time is dependent upon the input V_{CC} voltage and performance of the internal oscillator. The clock can be monitored at $\phi 2$ (pin 3). Figure 7-1 illustrates the power turn-on waveforms. Clock stabilization time is typically 20 ms.

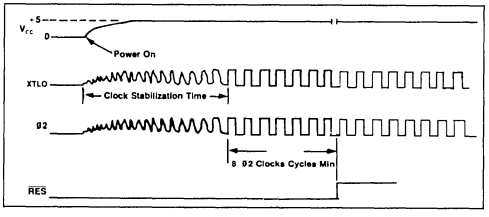


Figure 7-1. Power Turn-On Timing Detail

7.2 POWER-ON RESET

When $\overline{RES}$ goes from low to high, the device sets the Interrupt Mask Bit—bit 2 of the Processor Status Register—and initiates a reset vector fetch at address FFFC and FFFD to begin user program execution. All of the I/O ports (PA, PB, PC, PD) will be forced to the high (logic 1) state. All bits of the Control Register will be cleared to logic 0 causing the Interval Timers counter mode (mode 00) to be selected and all interrupt enabled bits to be reset.

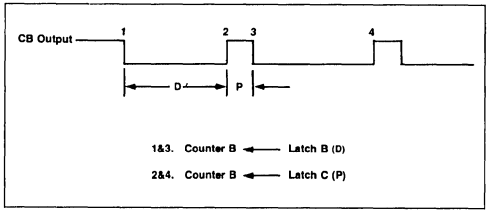


Figure 6-5. Counter B Pulse Generation

7.3 RESET ($\overline{RES}$) CONDITIONING

When $\overline{RES}$ is driven from low to high the device is put in a reset state causing the registers and I/O ports to be configured as shown in Table 7-1.

Table 7-1. $\overline{RES}$ Initialization of I/O Ports and Registers

	7	6	5	4	3	2	1	0
REGISTERS								
Processor Status	—	—	—	—	—	1	—	—
Mode Control (MCR)	0	0	0	0	0	0	0	0
Int. Enable (IER)	0	0	0	0	0	0	0	0
Int. Flag (IFR)	0	0	0	0	0	0	0	0
Ser. Com. Control (SCCR)	0	0	0	0	0	0	0	0
Ser. Com. Status (SCSR)	0	1	0	0	0	0	0	0
PORTS								
PA Latch	1	1	1	1	1	1	1	1
PB Latch	1	1	1	1	1	1	1	1
PC Latch	1	1	1	1	1	1	1	1
PD Latch	1	1	1	1	1	1	1	1

All RAM and other CPU registers will initialize in a random, non-repeatable data pattern.

7.4 INITIALIZATION

Any initialization process for the device should include a $\overline{RES}$, as indicated in the preceeding paragraphs. After stabilization of the internal clock (if a power on situation) an initialization routine should be executed to perform (as a minimum) the following functions:

1. The Stack Pointer should be set
2. Clear or Set Decimal Mode
3. Set or Clear Carry Flag
4. Set up Mode Controls as required
5. Clear Interrupts

A typical initialization subroutine could be as follows:

```
LDX     Load stack pointer starting address into
        X Register
TXS     Transfer X Register value to Stack Pointer
CLD     Clear Decimal Mode
SEC     Set Carry Flag
. . . .  Set-up Mode Control and
. . . .  special function registers
. . . .  and clear RAM as required
CLI     Clear Interrupts
```

3

APPENDIX A
ENHANCED R6502 INSTRUCTION SET

This appendix contains a summary of the Enhanced R6502 instruction set. For detailed information, consult the R6502 Microcomputer System Programming Manual, (Order No. 202). The four instructions notated with a * are added instructions to enhance the standard 6502 instruction set.

A.1 INSTRUCTION SET IN ALPHABETIC SEQUENCE

Mnemonic	Description	Mnemonic	Description
ADC	Add Memory to Accumulator with Carry	LDA	Load Accumulator with Memory
AND	"AND" Memory with Accumulator	LDX	Load Index X with Memory
ASL	Shift Left One Bit (Memory or Accumulator)	LDY	Load Index Y with Memory
		LSR	Shift One Bit Right (Memory or Accumulator)
*BBR	Branch on Bit Reset Relative		
*BBS	Branch on Bit Set Relative	NOP	No Operation
BCC	Branch on Carry Clear		
BCS	Branch on Carry Set	ORA	"OR" Memory with Accumulator
BEQ	Branch on Result Zero		
BIT	Test Bits in Memory with Accumulator		
BMI	Branch on Result Minus	PHA	Push Accumulator on Stack
BNE	Branch on Result not Zero	PHP	Push Processor Status on Stack
BPL	Branch on Result Plus	PLA	Pull Accumulator from Stack
BRK	Force Break	PLP	Pull Processor Status from Stack
BVC	Branch on Overflow Clear		
BVS	Branch on Overflow Set	*RMB	Reset Memory Bit
		ROL	Rotate One Bit Left (Memory or Accumulator)
CLC	Clear Carry Flag	ROR	Rotate One Bit Right (Memory or Accumulator)
CLD	Clear Decimal Mode	RTI	Return from Interrupt
CLI	Clear Interrupt Disable Bit	RTS	Return from Subroutine
CLV	Clear Overflow Flag		
CMP	Compare Memory and Accumulator		
CPX	Compare Memory and Index X	SBC	Subtract Memory from Accumulator with Borrow
CPY	Compare Memory and Index Y	SEC	Set Carry Flag
		SED	Set Decimal Mode
DEC	Decrement Memory by One	SEI	Set Interrupt Disable Status
DEX	Decrement Index X by One	*SMB	Set Memory Bit
DEY	Decrement Index Y by One	STA	Store Accumulator in Memory
		STX	Store Index X in Memory
EOR	"Exclusive-Or" Memory with Accumulator	STY	Store Index Y in Memory
INC	Increment Memory by One	TAX	Transfer Accumulator to Index X
INX	Increment Index X by One	TAY	Transfer Accumulator to Index Y
INY	Increment Index Y by One	TSX	Transfer Stack Pointer to Index X
		TXA	Transfer Index X to Accumulator
JMP	Jump to New Location	TXS	Transfer Index X to Stack Register
JSR	Jump to New Location Saving Return Address	TYA	Transfer Index Y to Accumulator

A.2 R6501 INSTRUCTION SET SUMMARY TABLE

ADDRESSING MODES (part 1)

MNEMONIC	OPERATION	IMMEDIATE			ABSOLUTE			ZERO PAGE			ACCUM.			IMPLIED			(IND, X)			(IND), Y		
		OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#
ADC	A + M + C→A (4)(1)	69	2	2	6D	4	3	65	3	2							61	6	2	71	5	2
AND	A M→A (1)	29	2	2	2D	4	3	25	3	2							21	6	2	31	5	2
ASL	C← [7 0] ←0				0E	6	3	06	5	2	0A	2	1									
BBR[#(0-7)]	Branch on M_b = 0 (5)(2)																					
BBS[#(0-7)]	Branch on M_b = 1 (5)(2)																					
BCC	Branch on C = 0 (2)																					
BCS	Branch on C = 1 (2)																					
BEQ	Branch on Z = 1 (2)																					
BIT	A ∧ M				2C	4	3	24	3	2												
BMI	Branch on N = 1 (2)																					
BNE	Branch on Z = 0 (2)																					
BPL	Branch on N = 0 (2)																					
BRK	Break													00	7	1						
BVC	Branch on V = 0 (2)																					
BVS	Branch on V = 1 (2)																					
CLC	0→C													18	2	1						
CLD	0→D													D8	2	1						
CLI	0→I													58	2	1						
CLV	0→V													B8	2	1						
CMP	A M (1)	C9	2	2	CD	4	3	C5	3	2							C1	6	2	D1	5	2
CPX	X M	E0	2	2	EC	4	3	E4	3	2												
CPY	Y M	C0	2	2	CC	4	3	C4	3	2												
DEC	M 1→M				CE	6	3	C6	5	2												
DEX	X 1→X													CA	2	1						
DEY	Y 1→Y													88	2	1						
EOR	A∀M→A (1)	49	2	2	4D	4	3	45	3	2							41	6	2	51	5	2
INC	M + 1→M				EE	6	3	E6														
INX	X + 1→X													EB	2	1						
INY	Y + 1→Y													C8	2	1						
JMP	Jump to New Loc				4C	3	3															
JSR	Jump Sub				20	6	3															
LDA	M→A (1)	A9	2	2	AD	4	3	A5	3	2							A1	6	2	B1	5	2
LDX	M→X (1)	A2	2	2	AE	4	3	A6	3	2												
LDY	M→Y (1)	A0	2	2	AC	4	3	A4	3	2												
LSR	0→ [7 0] → C				4E	6	3	46	5	2	4A	2	1									
NOP	No Operation													EA	2	1						
ORA	AVM→A (1)	09	2	2	0D	4	3	05	3	2							01	6	2	11	5	2
PHA	A→Ms S − 1→S													48	3	1						
PHP	P→Ms S − 1→S													08	3	1						
PLA	S + 1→S Ms→A													68	4	1						
PLP	S + 1→S Ms→P													28	4	1						
RMB[#(0-7)]	0→M_b (5)																					
ROL	[7 0]←[C]				2E	6	3	26	5	2	2A	2	1									
ROR	[C]→[7 0]				6E	6	3	66	5	2	6A	2	1									
RTI	Rtrn Int													40	6	1						
RTS	Rtrn Sub													60	6	1						
SBC	A − M − C→A (1)	E9	2	2	ED	4	3	E5	3	2							E1	6	2	F1	5	2
SEC	1→C													38	2	1						
SED	1→D													F8	2	1						
SEI	1→T													78	2	1						
SMB[#(0-7)]	1→M_b (5)																					
STA	A→M				8D	4	3	85	3	2							81	6	2	91	6	2
STX	X→M				8E	4	3	86	3	2												
STY	Y→M				8C	4	3	84	3	2												
TAX	A→X													AA	2	1						
TAY	A→Y													A8	2	1						
TSX	S→X													BA	2	1						
TXA	X→A													8A	2	1						
TXS	X→S													9A	2	1						
TYA	Y→A													98	2	1						

ADDRESSING MODES (part 2) and PROCESSOR STATUS CODES

MNEMONIC	Z. PAGE, X			ABS, X			ABS, Y			RELATIVE			INDIRECT			Z. PAGE, Y			BIT ADDRESSING (OP BY BIT #)								PROCESSOR STATUS CODES 7 6 5 4 3 2 1 0
	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	0	1	2	3	4	5	6	7	N V · B D I Z C
ADC	75	4	2	7D	4	3	79	4	3																		N V · · · · Z C
AND	35	4	2	3D	4	3	39	4	3																		N · · · · · Z ·
ASL	16	6	2	1E	7	3																					N · · · · · Z C
BBR[#(0-7)]																			0F	1F	2F	3F	4F	5F	6F	7F	· · · · · · · ·
BBS[#(0-7)]																			8F	9F	AF	BF	CF	DF	EF	FF	· · · · · · · ·
BCC										90	2	2															· · · · · · · ·
BCS										B0	2	2															· · · · · · · ·
BEQ										F0	2	2															· · · · · · · ·
BIT																											M_7 M_6 · · · · Z ·
BMI										30	2	2															· · · · · · · ·
BNE										D0	2	2															· · · · · · · ·
BPL										10	2	2															· · · · · · · ·
BRK																											· · · 1 · 1 · ·
BVC										50	2	2															· · · · · · · ·
BVS										70	2	2															· · · · · · · ·
CLC																											· · · · · · · 0
CLD																											· · · · 0 · · ·
CLI																											· · · · · 0 · ·
CLV																											· 0 · · · · · ·
CMP	D5	4	2	DD	4	3	D9	4	3																		N · · · · · Z C
CPX																											N · · · · · Z C
CPY																											N · · · · · Z C
DEC	D6	6	2	DE	7	3																					N · · · · · Z ·
DEX																											N · · · · · Z ·
DEY																											N · · · · · Z ·
EOR	55	4	2	5D	4	3	59	4	3																		N · · · · · Z ·
INC	F6	6	2	FE	7	3																					N · · · · · Z ·
INX																											N · · · · · Z ·
INY																											N · · · · · Z ·
JMP													6C	5	3												· · · · · · · ·
JSR																											· · · · · · · ·
LDA	B5	4	2	BD	4	3	B9	4	3																		N · · · · · Z ·
LDX							BE	4	3							B6	4	2									N · · · · · Z ·
LDY	B4	4	2	BC	4	3																					N · · · · · Z ·
LSR	56	6	2	5E	7	3																					0 · · · · · Z C
NOP																											· · · · · · · ·
ORA	15	4	2	1D	4	3	19	4	3																		N · · · · · Z ·
PHA																											· · · · · · · ·
PHP																											· · · · · · · ·
PLA																											N · · · · · Z ·
PLP																											(Restored)
RMB[#(0-7)]																			07	17	27	37	47	57	67	77	· · · · · · · ·
ROL	36	6	2	3E	7	3																					N · · · · · Z C
ROR	76	6	2	7E	7	3																					N · · · · · Z C
RTI																											(Restored)
RTS																											· · · · · · · ·
SBC	F5	4	2	FD	4	3	F9	4	3																		N V · · · · Z (3)
SEC																											· · · · · · · 1
SED																											· · · · 1 · · ·
SEI																											· · · · · 1 · ·
SMB[#(0-7)]																			87	97	A7	B7	C7	D7	E7	F7	· · · · · · · ·
STA	95	4	2	9D	5	3	[illegible]	5	3																		· · · · · · · ·
STX																96	4	2									· · · · · · · ·
STY	94	4	2																								· · · · · · · ·
TAX																											N · · · · · Z ·
TAY																											N · · · · · Z ·
TSX																											N · · · · · Z ·
TXA																											N · · · · · Z ·
TXS																											· · · · · · · ·
TYA																											N · · · · · Z ·

NOTES

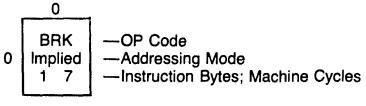
1. Add 1 to N if page boundary is crossed
2. Add 1 to N if branch occurs to same page
   Add 2 to N if branch occurs to different page
3. Carry not = Borrow
4. If in decimal mode Z flag is invalid
   accumulator must be checked on zero result.
5. Effects 8-bit data field of the specified zero page address.

LEGEND

- X = Index X
- Y = Index Y
- A = Accumulator
- M = Memory per effective address
- M_s = Memory per stack pointer
- M_b = Selecter zero page memory bit
- M_7 = Memory Bit 7
- M_6 = Memory Bit 6
- • = Add
- – = Subtract
- ∧ = And
- V = Or
- ∀ = Exclusive Or
- n = Number of cycles
- # = Number of Bytes

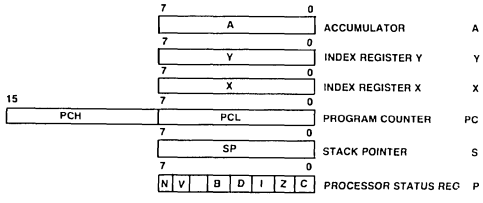
A.3 INSTRUCTION CODE MATRIX

MSD \ LSD	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	MSD
0	BRK Implied 1 7	ORA (IND, X) 2 6				ORA ZP 2 3	ASL ZP 2 5	RMB0 ZP 2 5	PHP Implied 1 3	ORA IMM 2 2	ASL Accum 1 2			ORA ABS 3 4	ASL ABS 3 6	BBR0 ZP 3 5**	0
1	BPL Relative 2 2**	ORA (IND), Y 2 5*				ORA ZP, X 2 4	ASL ZP, X 2 6	RMB1 ZP 2 5	CLC Implied 1 2	ORA ABS, Y 3 4*				ORA ABS, X 3 4*	ASL ABS, X 3 7	BBR1 ZP 3 5**	1
2	JSR Absolute 3 6	AND (IND, X) 2 6			BIT ZP 2 3	AND ZP 2 3	ROL ZP 2 5	RMB2 ZP 2 5	PLP Implied 1 4	AND IMM 2 2	ROL Accum 1 2		BIT ABS 3 4	AND ABS 3 4	ROL ABS 3 6	BBR2 ZP 3 5**	2
3	BMI Relative 2 2**	AND (IND, Y) 2 5*				AND ZP, X 2 4	ROL ZP, X 2 6	RMB3 ZP 2 5	SEC Implied 1 2	AND ABS, Y 3 4*				AND ABS, X 3 4*	ROL ABS, X 3 7	BBR3 ZP 3 5**	3
4	RTI Implied 1 6	EOR (IND, X) 2 6				EOR ZP 2 3	LSR ZP 2 5	RMB4 ZP 2 5	PHA Implied 1 3	EOR IMM 2 2	LSR Accum 1 2		JMP ABS 3 3	EOR ABS 3 4	LSR ABS 3 6	BBR4 ZP 3 5**	4
5	BVC Relative 2 2**	EOR (IND), Y 2 5*				EOR ZP, X 2 4	LSR ZP, X 2 6	RMB5 ZP 2 5	CLI Implied 1 2	EOR ABS, Y 3 4*				EOR ABS, X 3 4*	LSR ABS, X 3 7	BBR5 ZP 3 5**	5
6	RTS Implied 1 6	ADC (IND, X) 2 6				ADC ZP 2 3	ROR ZP 2 5	RMB6 ZP 2 5	PLA Implied 1 4	ADC IMM 2 2	ROR Accum 1 2		JMP Indirect 3 5	ADC ABS 3 4	ROR ABS 3 6	BBR6 ZP 3 5**	6
7	BVS Relative 2 2**	ADC (IND, Y) 2 5*				ADC ZP, X 2 4	ROR ZP, X 2 6	RMB7 ZP 2 5	SEI Implied 1 2	ADC ABS, Y 3 4*				ADC ABS, X 3 4*	ROR ABS, X 3 7	BBR7 ZP 3 5**	7
8		STA (IND, X) 2 6			STY ZP 2 3	STA ZP 2 3	STX ZP 2 3	SMB0 ZP 2 5	DEY Implied 1 2		TXA Implied 1 2		STY ABS 3 4	STA ABS 3 4	STX ABS 3 4	BBS0 ZP 3 5**	8
9	BCC Relative 2 2**	STA (IND, Y) 2 6			STY ZP, X 2 4	STA ZP, X 2 4	STX ZP, Y 2 4	SMB1 ZP 2 5	TYA Implied 1 2	STA ABS, Y 3 5	TXS Implied 1 2			STA ABS, X 3 5		BBS1 ZP 3 5**	9
A	LDY IMM 2 2	LDA (IND, X) 2 6	LDX IMM 2 2		LDY ZP 2 3	LDA ZP 2 3	LDX ZP 2 3	SMB2 ZP 2 5	TAY Implied 1 2	LDA IMM 2 2	TAX Implied 1 2		LDY ABS 3 4	LDA ABS 3 4	LDX ABS 3 4	BBS2 ZP 3 5**	A
B	BCS Relative 2 2**	LDA (IND), Y 2 5*			LDY ZP, X 2 4	LDA ZP, X 2 4	LDX ZP, Y 2 4	SMB3 ZP 2 5	CLV Implied 1 2	LDA ABS, Y 3 4*	TSX Implied 1 2		LDY ABS, X 3 4*	LDA ABS, X 3 4*	LDX ABS, Y 3 4*	BBS3 ZP 3 5**	B
C	CPY IMM 2 2	CMP (IND, X) 2 6			CPY ZP 2 3	CMP ZP 2 3	DEC ZP 2 5	SMB4 ZP 2 5	INY Implied 1 2	CMP IMM 2 2	DEX Implied 1 2		CPY ABS 3 4	CMP ABS 3 4	DEC ABS 3 6	BBS4 ZP 3 5**	C
D	BNE Relative 2 2**	CMP (IND), Y 2 5*				CMP ZP, X 2 4	DEC ZP, X 2 6	SMB5 ZP 2 5	CLD Implied 1 2	CMP ABS, Y 3 4*				CMP ABS, X 3 4*	DEC ABS, X 3 7	BBS5 ZP 3 5**	D
E	CPX IMM 2 2	SBC (IND, X) 2 6			CPX ZP 2 3	SBC ZP 2 3	INC ZP 2 5	SMB6 ZP 2 5	INX Implied 1 2	SBC IMM 2 2	NOP Implied 1 2		CPX ABS 3 4	SBC ABS 3 4	INC ABS 3 6	BBS6 ZP 3 5**	E
F	BEQ Relative 2 2**	SBC (IND), Y 2 5*				SBC ZP, X 2 4	INC ZP, X 2 6	SMB7 ZP 2 5	SED Implied 1 2	SBC ABS, Y 3 4*				SBC ABS, X 3 4*	INC ABS, X 3 7	BBS7 ZP 3 5**	F
	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	

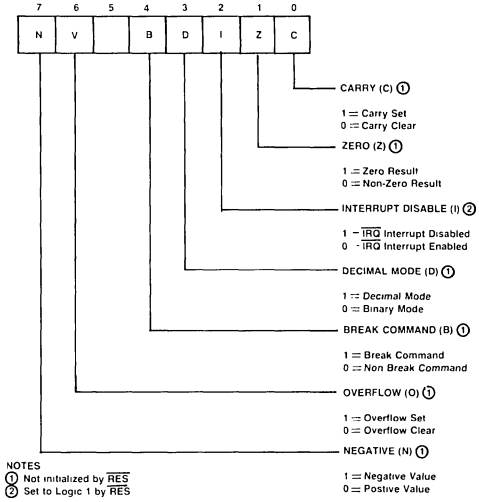


*Add 1 to N if page boundary is crossed.
**Add 1 to N if branch occurs to same page;
add 2 to N if branch occurs to different page.

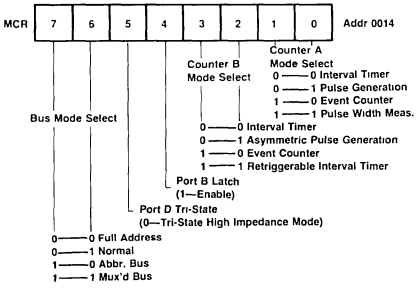
APPENDIX B
KEY REGISTER SUMMARY



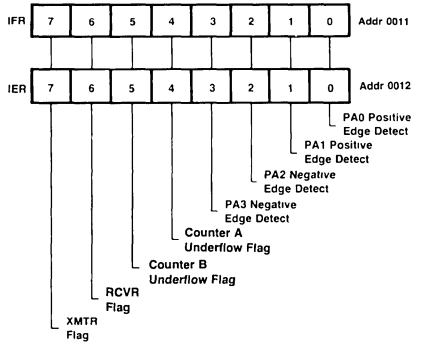
CPU Registers



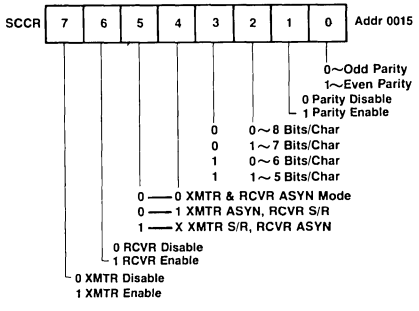
Processor Status Register



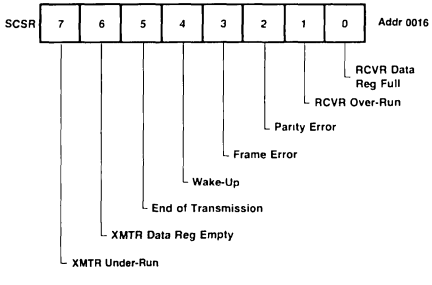
Mode Control Register



Interrupt Enable and Flag Registers



Serial Communications Control Register



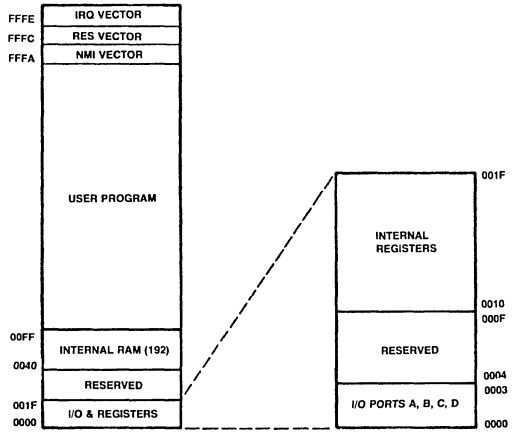
Serial Communications Status Register

APPENDIX C
ADDRESS ASSIGNMENTS/MEMORY MAPS/PIN FUNCTIONS

C.1 I/O AND INTERNAL REGISTER ADDRESSES

ADDRESS (HEX)	READ	WRITE
001F	— —	— —
1E	Lower Counter B	Upper Latch B, Cntr B←Latch B, CLR Flag
1D	Upper Counter B	Upper Latch B, Latch C←Latch B
1C	Lower Counter B, CLR Flag	Lower Latch B.
1B	— —	— —
1A	Lower Counter A	Upper Latch A, Cntr A←Latch A, CLR Flag
19	Upper Counter A	Upper Latch A
18	Lower Counter A, CLR Flag	Lower Latch A
17	Serial Receiver Data Register	Serial Transmitter Data Register
16	Serial Comm. Status Register	Serial Comm. Status Reg. Bits 4 & 5 only
15	Serial Comm. Control Register	Serial Comm. Control Register
14	Mode Control Register	Mode Control Register
13	— —	— —
12	Interrupt Enable Register	Interrupt Enable Register
11	Interrupt Flag Register	— —
0010	Read FF	Clear Int Flag (Bits 0-3 only, Write 0's only)
0F	**RESERVED**	
0E		
0D	These addresses are reserved and are used by the CPU during Read and Write operation over the external Data Bus (D0-D7).	
0C		
0B		
0A		
09		
08		
07		
06		
05		
04		
03	Port D	Port D
02	Port C	Port C
01	Port B	Port B
0000	Port A	Port A

C.2 FULL ADDRESS MODE MEMORY MAP—R6501



C.3 MULTIPLE FUNCTION PIN ASSIGNMENTS—PORT C AND PORT D

FULL ADDRESS MODE	I/O PORT FUNCTION	ABBREV	MUX
PC0	PC0	A0	A0
PC1	PC1	A1	A1
PC2	PC2	A2	A2
PC3	PC3	A3	A3
PC4	PC4	A12	A12
PC5	PC5	R/W	R/W
A13	PC6	A13	A13
A14	PC7	EMS	EMS
PD0	PD0	D0	A4/D0
PD1	PD1	D1	A5/D1
PD2	PD2	D2	A6/D2
PD3	PD3	D3	A7/D3
PD4	PD4	D4	A8/D4
PD5	PD5	D5	A9/D5
PD6	PD6	D6	A10/D6
PD7	PD7	D7	A11/D7

APPENDIX D
ELECTRICAL SPECIFICATIONS

MAXIMUM RATINGS*

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC} & V_{RR}	−0.3 to +7.0	Vdc
Input Voltage	V_{IN}	−0.3 to +7.0	Vdc
Operating Temperature Range, Commercial Industrial	T_A	T_L to T_H 0 to +70 −40 to +85	°C
Storage Temperature Range	T_{STG}	−55 to +150	°C

*NOTE: Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the other sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

(V_{CC} = 5.0V ±5%, V_{RR} = V_{CC}; V_{SS} = 0V; T_A = T_L to T_H, unless otherwise specified)

Parameter	Symbol	Min	Typ[1]	Max	Unit	Test Conditions
RAM Standby Voltage (Retention Mode)	V_{RR}	3.0		V_{CC}	V	
RAM Standby Current (Retention Mode)	I_{RR}	—	4	—	mA	T_A = 25°C
Input High Voltage All Except XTLI XTLI	V_{IH}	 +2.0 +4.0	 — —	 V_{CC} V_{CC}	V	
Input Low Voltage	V_{IL}	−0.3	—	+0.8	V	
Input Leakage Current $\overline{RES}$, $\overline{NMI}$	I_{IN}	—	—	±10.0	μA	V_{IN} = 0 to 5.0V
Input Low Current PA, PB, PC, PD	I_{IL}	—	−1.0	−1.6	mA	V_{IL} = 0.4V
Output High Voltage (Except XTLO)	V_{OH}	+2.4	—	V_{CC}	V	I_{LOAD} = −100 μA
Output Low Voltage	V_{OL}	—	—	+0.4	V	I_{LOAD} = 1.6 mA
I/O Port Pull-Up Resistance PA0–PA7, PB0–PB7, PC0–PC7	R_L	3.0	6.0	11.5	Kohm	
Output Leakage Current (Three-State Off)	I_{OUT}	—	—	±10	μA	
Input Capacitance XTLI, XTLO All Others	C_{IN}	 — —	 — —	 50 10	pF	T_A = 25°C V_{IN} = 0V f = 1.0 MHz
Output Capacitance (Three-State Off)	C_{OUT}	—	—	10	pF	T_A = 25°C V_{IN} = 0V f = 1.0 MHz
Power Dissipation (Outputs High)	P_D	—	750	1100	mW	T_A = 0°C

Notes:
1. Typical values measured at T_A = 25°C and V_{CC} = 5.0V.
2. Negative sign indicates outward current flow, positive indicates inward flow.

APPENDIX E
TIMING REQUIREMENTS AND CHARACTERISTICS

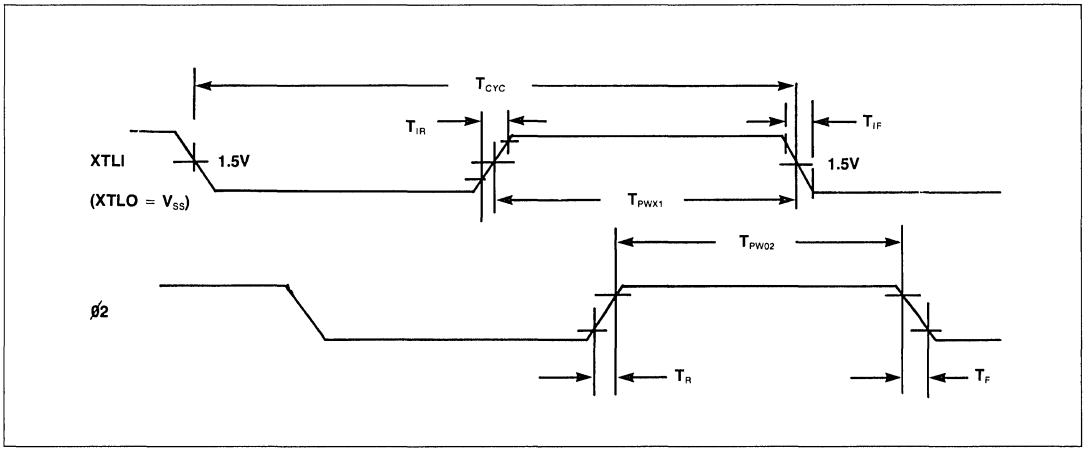
E.1 GENERAL NOTES

1. V_{CC} = 5V ±5%, 0°C ≤ TA ≤ 70°C
2. A valid V_{CC} – $\overline{RES}$ sequence is required before proper operation is achieved.
3. All timing reference levels are 0.8V and 2.0V, unless otherwise specified.
4. All time units are nanoseconds, unless otherwise specified.
5. All capacitive loading is 130pf maximum, except as noted below:

PA, PB	— 50pF maximum
PC (I/O Modes Only)	— 50pF maximum
PC (ABB and Mux Mode)	— 130pF maximum
PC6, PC7 (Full Address Mode)	— 130pF maximum

E.2 CLOCK TIMING

SYMBOL	PARAMETER	1 MHz		2 MHz	
		MIN	MAX	MIN	MAX
T_{CYC}	Cycle Time	1000	10 μs	500	10 μs
T_{PWX1}	XTLI Input Clock Pulse Width XTLO = VSS	500 ± 25	—	250 ± 10	—
T_{PW02}	Output Clock Pulse Width at Minimum T_{CYC}	T_{PWX1}	T_{PWX1} ± 25	T_{PWX1}	T_{PWX1} ± 20
T_R, T_F	Output Clock Rise, Fall Time	—	25	—	15
T_{IR}, T_{IF}	Input Clock Rise, Fall Time	—	10	—	10

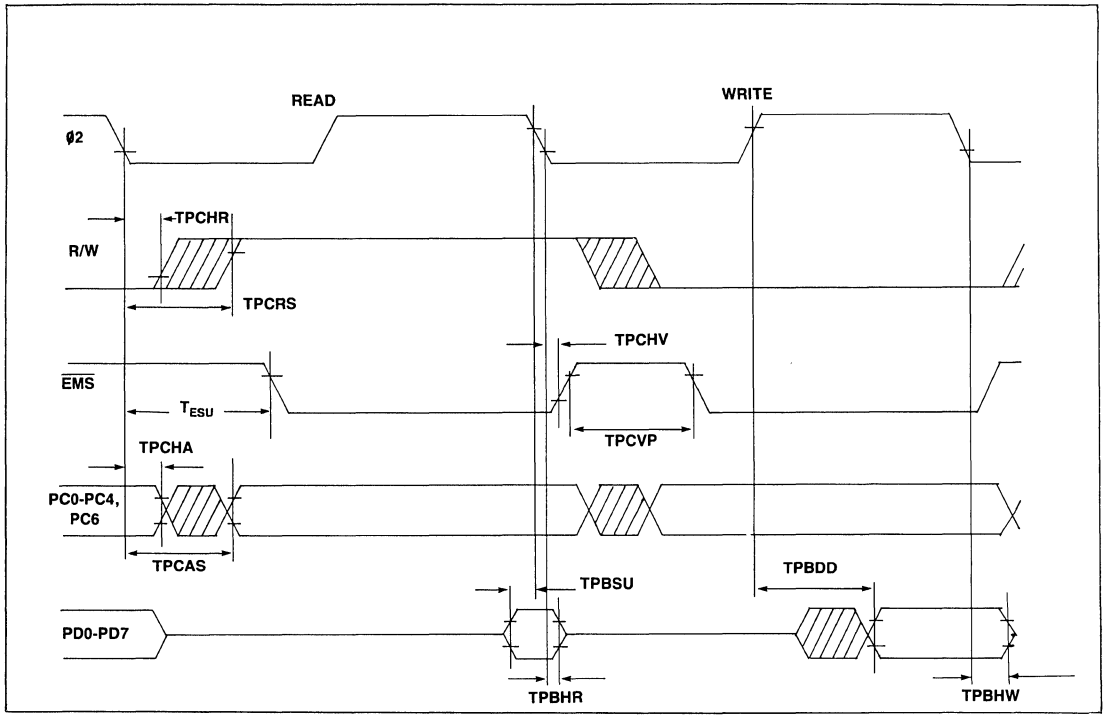


E.3 ABBREVIATED MODE TIMING—PC AND PD

(MCR 5 = 1, MCR 6 = 0, MCR 7 = 1)

SYMBOL	PARAMETER	1 MHz		2 MHz	
		MIN	MAX	MIN	MAX
T_{PCRS}	(PC5) R/W Setup Time	—	225	—	140
T_{PCAS}	(PC0-PC4, PC6) Address Setup Time	—	225	—	140
T_{PBSU}	(PD) Data Setup Time	50	—	35	—
T_{PBHR}	(PD) Data Read Hold Time	10	—	10	—
T_{PBHW}	(PD) Data Write Hold Time	30	—	30	—
T_{PBDD}	(PD) Data Output Delay	—	175	—	150
T_{PCHA}	(PC0-PC4, PC6) Address Hold Time	30	—	30	—
T_{PCHR}	(PC5) R/W Hold Time	30	—	30	—
T_{PCHV}	(PC7) $\overline{EMS}$ Hold Time	10	—	10	—
T_{PCVP}	(PC7) $\overline{EMS}$ Stabilization Time	30	—	30	—
T_{ESU}	$\overline{EMS}$ Setup Time	—	350	—	210

E.3.1 Abbreviated Mode Timing Diagram



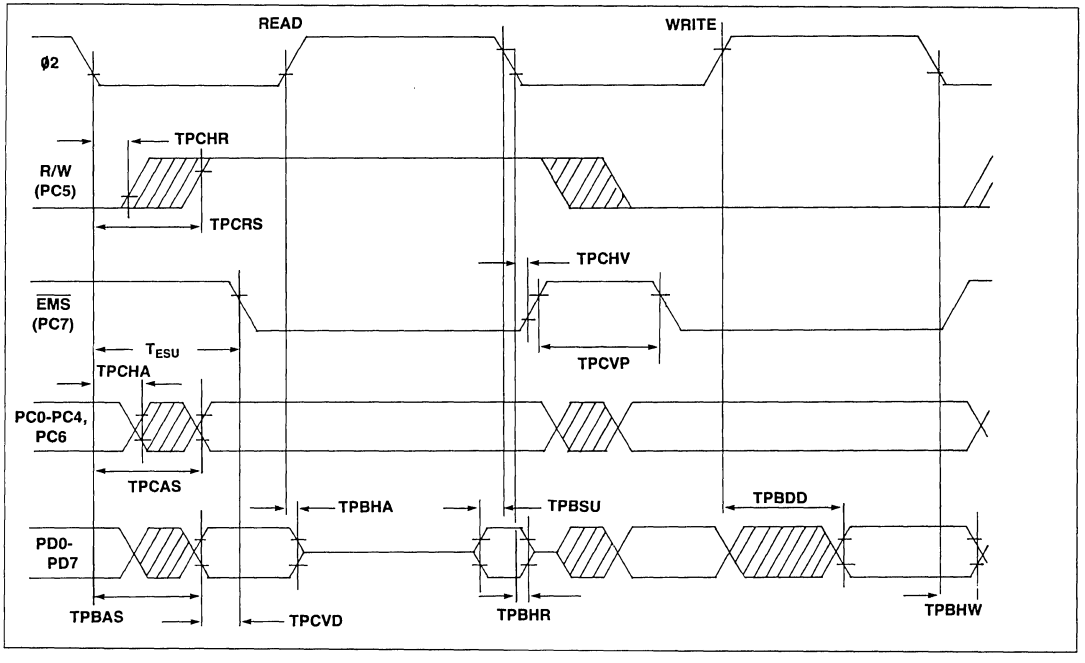
E.4 MULTIPLEXED MODE TIMING—PC AND PD

(MCR 5 = 1, MCR 6 = 1, MCR 7 = 1)

SYMBOL	PARAMETER	1 MHz		2 MHz	
		MIN	MAX	MIN	MAX
T_{PCRS}	(PC5) R/W Setup Time	—	225	—	140
T_{PCAS}	(PC0-PC4, PC6) Address Setup Time	—	225	—	140
T_{PBAS}	(PD) Address Setup Time	—	225	—	140
T_{PBSU}	(PD) Data Setup Time	50	—	35	—
T_{PBHR}	(PD) Data Read Hold Time	10	—	10	—
T_{PBHW}	(PD) Data Write Hold Time	30	—	30	—
T_{PBDD}	(PD) Data Output Delay	—	175	—	150
T_{PCHA}	(PC0-PC4, PC6) Address Hold Time	30	—	30	—
T_{PBHA}	(PD) Address Hold Time	10	100	10	80
T_{PCHR}	(PC5) R/W Hold Time	30	—	30	—
T_{PCHV}	(PC7) $\overline{EMS}$ Hold Time	10	—	10	—
T_{PCVD}[1]	(PC7) Address to $\overline{EMS}$ Delay Time	30		30	
T_{PCVP}	(PC7) $\overline{EMS}$ Stabilization Time	30	—	30	—
T_{ESU}	$\overline{EMS}$ Setup Time	—	350	—	210

NOTE 1: Values assume PC0-PC4, PC6 and PC7 have the same capacitive load.

E.4.1 Multiplex Mode Timing Diagram

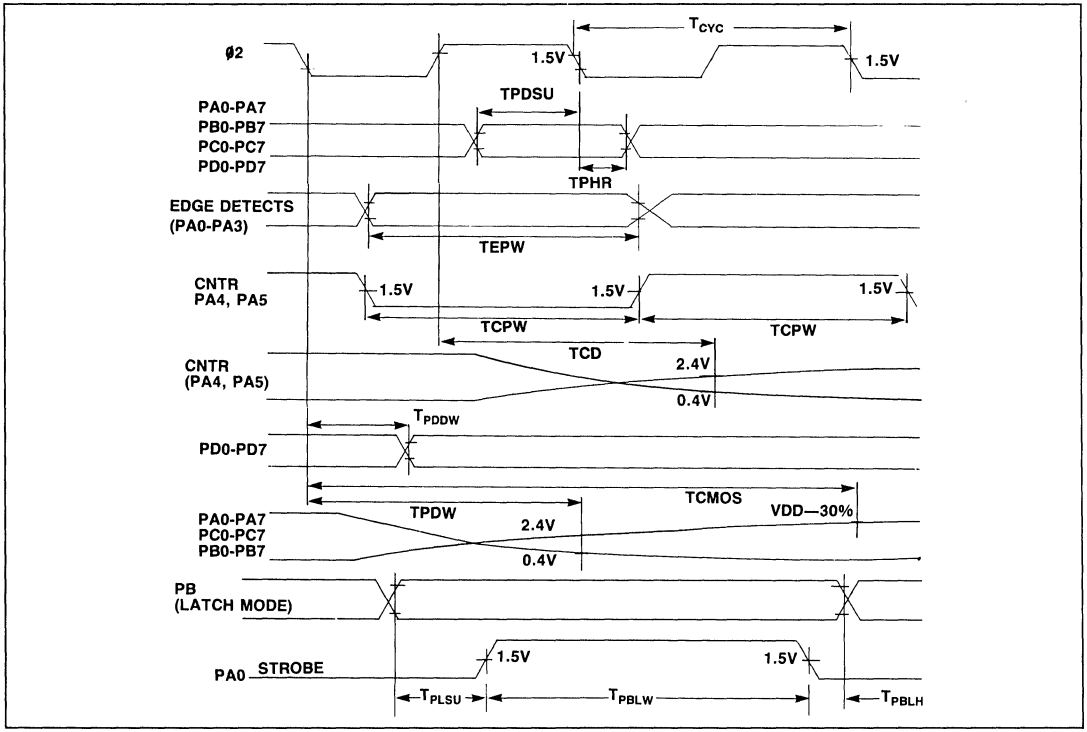


E.5 I/O, EDGE DETECT, COUNTERS, AND SERIAL I/O TIMING

SYMBOL	PARAMETER	1 MHz		2 MHz	
		MIN	MAX	MIN	MAX
	Internal Write to Peripheral Data Valid				
T_{PDW}(1)	PA, PB, PC TTL	—	500	—	500
T_{CMOS}(1)	PA, PB, PC CMOS	—	1000	—	1000
T_{PDDW}	PD	—	175	—	150
	Peripheral Data Setup Time				
T_{PDSU}	PA, PB, PC	200	—	200	—
T_{PDSU}	PD	50	—	50	—
	Peripheral Data Hold Time				
T_{PHR}	PA, PB, PC	75	—	75	—
T_{PHR}	PD	10	—	10	—
T_{EPW}	PA0-PA3 Edge Detect Pulse Width	T_{CYC}	—	T_{CYC}	—
	Counters A and B				
T_{CPW}	PA4, PA5 Input Pulse Width	T_{CYC}	—	T_{CYC}	—
T_{CD}(1)	PA4, PA5 Output Delay	—	500	—	500
	Port B Latch Mode				
T_{PBLW}	PA0 Strobe Pulse Width	T_{CYC}	—	T_{CYC}	—
T_{PLSU}	PB Data Setup Time	175	—	150	—
T_{PBLH}	PB Data Hold Time	30	—	30	—
	Serial I/O				
T_{PDW}(1)	PA6 XMTR TTL	—	500	—	500
T_{CMOS}(1)	PA6 XMTR CMOS	—	1000	—	1000
T_{CPW}	PA4 RCVR S/R Clock Width	4 T_{CYC}	—	4 T_{CYC}	—
T_{PDW}(1)	PA4 XMTR Clock—S/R Mode (TTL)	—	500	—	500
T_{CMOS}(1)	PA4 XMTR Clock—S/R Mode (CMOS)	—	1000	—	1000

NOTE 1: Maximum Load Capacitance: 50pF
Passive Pull-Up Required

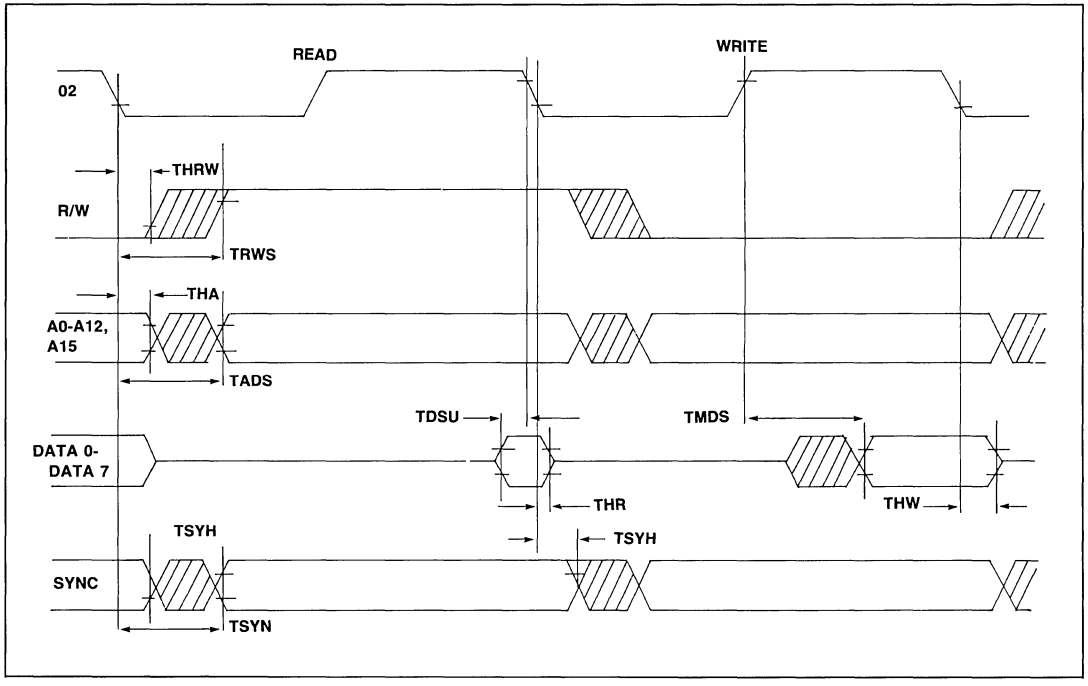
E.5.1 I/O, Edge Detect, Counter, and Serial I/O Timing



E.6 MICROPROCESSOR TIMING (D0-D7, A0-A12, A15, SYNC, R/W)

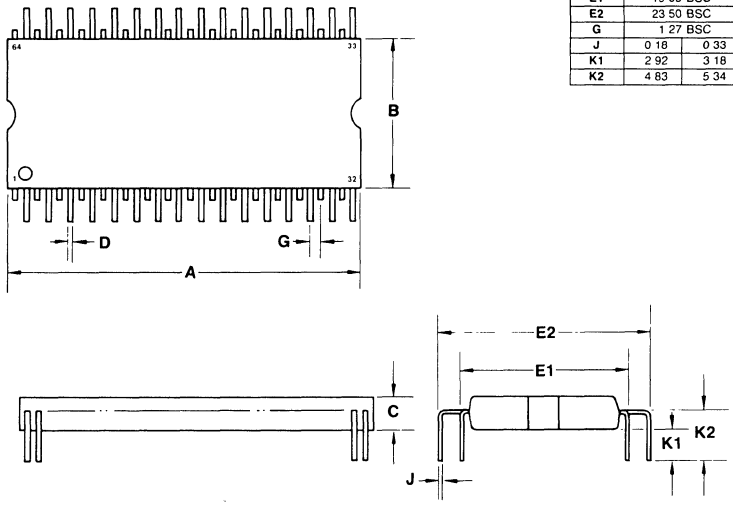
SYMBOL	PARAMETER	1 MHz		2 MHz	
		MIN	MAX	MIN	MAX
T_{RWS}	R/W Setup Time	—	225	—	140
T_{ADS}	A0-A12, A15 Setup Time	—	150	—	75
T_{DSU}	D0-D7 Data Setup Time	50	—	35	—
T_{HR}	D0-D7 Read Hold Time	10	—	10	—
T_{HW}	D0-D7 Write Hold Time	30	—	30	—
T_{MOS}	D0-D7 Write Output Delay	—	175	—	130
T_{SYN}	SYNC Setup	—	225	—	175
T_{HA}	A0-A12, A15 Hold Time	30	—	30	—
T_{HRW}	R/W Hold Time	30	—	30	—
T_{ACC}	External Memory Access Time $T_{ACC} = T_{CYC} - T_F - T_{ADS} - T_{DSU}$	—	T_{ACC}	—	T_{ACC}
T_{SYH}	SYNC Hold Time	30	—	30	—

E.6.1 Microprocessor Timing Diagram

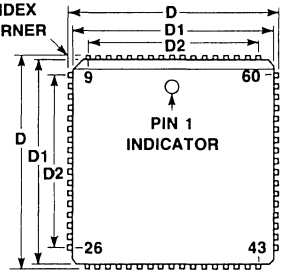


64-PIN PLASTIC QUAD IN-LINE PACKAGE (QUIP)

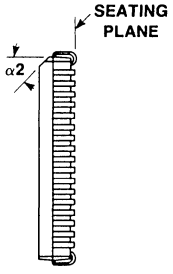
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	41 10	41 61	1 618	1 638
B	17 02	17.23	0 670	0 690
C	3 56	4 58	0 140	0 180
D	0 48	0 56	0 018	0 022
E1	19 05 BSC		0 750 BSC	
E2	23 50 BSC		0 925 BSC	
G	1 27 BSC		0 050 BSC	
J	0 18	0 33	0 007	0 013
K1	2 92	3 18	0 115	0 125
K2	4 83	5 34	0 190	0 210



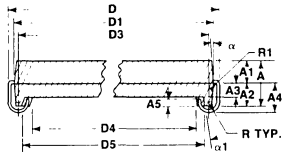
68-PIN PLASTIC CHIP CARRIER (PCC)



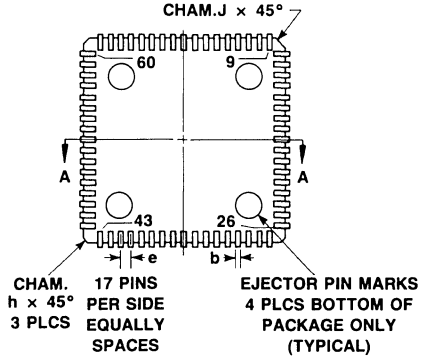
TOP VIEW



SIDE VIEW



SECTION A-A
TYP FOR BOTH AXIS (EXCEPT FOR BEVELED EDGE)



BOTTOM VIEW

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	3.683	3.785	.145	.149
A1	1.829	1.930	.072	.076
A2	1.803	1.905	.071	.075
A3	1.372	1.473	.054	.058
A4	2.311	2.464	.091	.097
A5	0.203	0.305	.008	.012
b	0.457 TYP		.018 TYP	
D	25.02	25.27	.985	.995
D1	24.00	24.26	.945	.955
D2	20.19	20.45	.795	.805
D3	23.24	23.50	.915	.925
D4	20.96	21.21	.825	.835
D5	22.23	22.48	.875	.885
e	1.27 BSC		.050 BSC	
h	0.254 TYP		.010 TYP	
J	1.143 TYP		.045 TYP	
α	4° TYP		4° TYP	
α1	10° TYP		10° TYP	
α2	45° TYP		45° TYP	
R	0.889 TYP		.035 TYP	
R1	0.254 TYP		.010 TYP	

3

Rockwell

R6511Q One-Chip Microprocessor and R6500/13 One-Chip Microcomputer

SECTION 1 INTRODUCTION

1.1 FEATURES

- Enhanced 6502 CPU
  - —Four new bit manipulation instructions
    - Set Memory Bit (SMB)
    - Reset Memory Bit (RMB)
    - Branch on Bit Set (BBS)
    - Branch on Bit Reset (BBR)
  - —Decimal and binary arithmetic modes
  - —13 addressing modes
  - —True indexing
- 256-byte mask-programmable ROM or no ROM*
- 192-byte static RAM
- 32 bidirectional, TTL-compatible I/O lines (four ports)
- One 8-bit port may be tri-stated under software control
- One 8-bit port may have latched inputs under software control
- Two 16-bit programmable counter/timers, with latches
  - —Pulse width measurement
  - —Asymmetrical pulse generation
  - —Pulse generation
  - —Interval timer
  - —Event counter
  - —Retriggerable interval timer
- Serial port
  - —Full-duplex asynchronous operation mode
  - —Selectable 5- to 8-bit characters
  - —Wake-up feature
  - —Synchronous shift register mode
  - —Standard programmable bit rates programmable up to 62.5K bits/sec @ 1 MHz
- Ten interrupts
  - —Four edge-sensitive lines; two positive, two negative
  - —Reset
  - —Non-maskable
  - —Two counter underflows
  - —Serial data received
  - —Serial data transmitted
- Bus expandable to 64K bytes of external memory

*R6511Q has no ROM.

- Flexible clock circuitry
  - —2-MHz or 1-MHz internal operation
  - —Internal clock with external XTAL at two or four times internal frequency
  - —External clock input divided by one, two or four
- 1μs minimum instruction execution time @ 2 MHz
- NMOS-3 silicon gate, depletion load technology
- Single +5V power supply
- 12 mW stand-by power for 32 bytes of the 192-byte RAM
- 64-pin QUIP

NOTE

This document uses the term R6500/13 to describe both parts. See section 1.3 for a description of the options available when using the R6500/13 and the fixed features of the R6511Q.

1.2 SUMMARY

The Rockwell R6500/13 is a complete, high-performance 8-bit NMOS-3 microcomputer on a single chip and is compatible with all members of the R6500 family.

The R6500/13 consists of an enhanced 6502 CPU, an internal clock oscillator, an optional 256 bytes of Read-Only Memory, 192 bytes of Random Access Memory (RAM) and versatile interface circuitry. The interface circuitry includes two 16-bit programmable timer/counters, 32 bidirectional input/output lines (including four edge-sensitive lines and input latching on one 8-bit port), a full-duplex serial I/O channel, ten interrupts and bus expandability.

The innovative architecture and the demonstrated high performance of the R6502 CPU, as well as instruction simplicity, results in system cost-effectiveness and a wide range of computational power. These features make the R6500/13 a leading candidate for microcomputer applications.

The R6511Q contains all the features of the R6500/13 except it has no ROM and is thus intended as a high feature microprocessor with full 65K address bus.

To allow prototype circuit development, Rockwell offers a PROM-compatible 64-pin extended microprocessor device. This device, the R6511Q, provides all R6500/11 interface lines, plus the address bus, data bus and control lines to interface with external memory. The R6511Q also can be used to emulate the R6500/13. With the addition of external circuits it can also emulate the R6500/12.

Rockwell supports development of the R6500/13 with the Low Cost Emulator (LCE) Development System and the R6500/* Family of Personality Modules. Complete in-circuit emulation with the R6500/* Family of Personality Modules allows total system test and evaluation.

This product description assumes that the reader is familiar with the R6502 CPU hardware and programming capabilities. A detailed description of the R6502 CPU hardware is included in the R6500 Microcomputer System Hardware Manual (Document Number 29650N31). A description of the instruction capabilities of the R6502 CPU is contained in the R6500 Microcomputer System Programming Manual (Document Number 29650N30).

1.3 CUSTOMER OPTIONS

The R6500/13 microcomputer is available with the following customer specified mask options.

- Option 1 Crystal or RC oscillator
- Option 2 Clock divide by 2 or 4
- Option 3 Clock MASTER Mode or SLAVE Mode
- Option 4 with or without a 256 byte ROM
- Option 5 Reset Vector at FFFC or 7FFF
- Option 6 Port A with or without internal pull-up resistors
- Option 7 Port B with or without internal pull-up resistors
- Option 8 Port C with or without internal pull-up resistors

All options should be specified on an R6500/13 order form.

The R6511Q has no customer specified mask options. It has the following characteristics.

- Crystal Oscillator
- Clock Divide by 2
- Clock MASTER Mode
- Without ROM
- Reset Vector at FFFC
- No internal pull-up resistors on any Port (PA, PB, or PC)

3

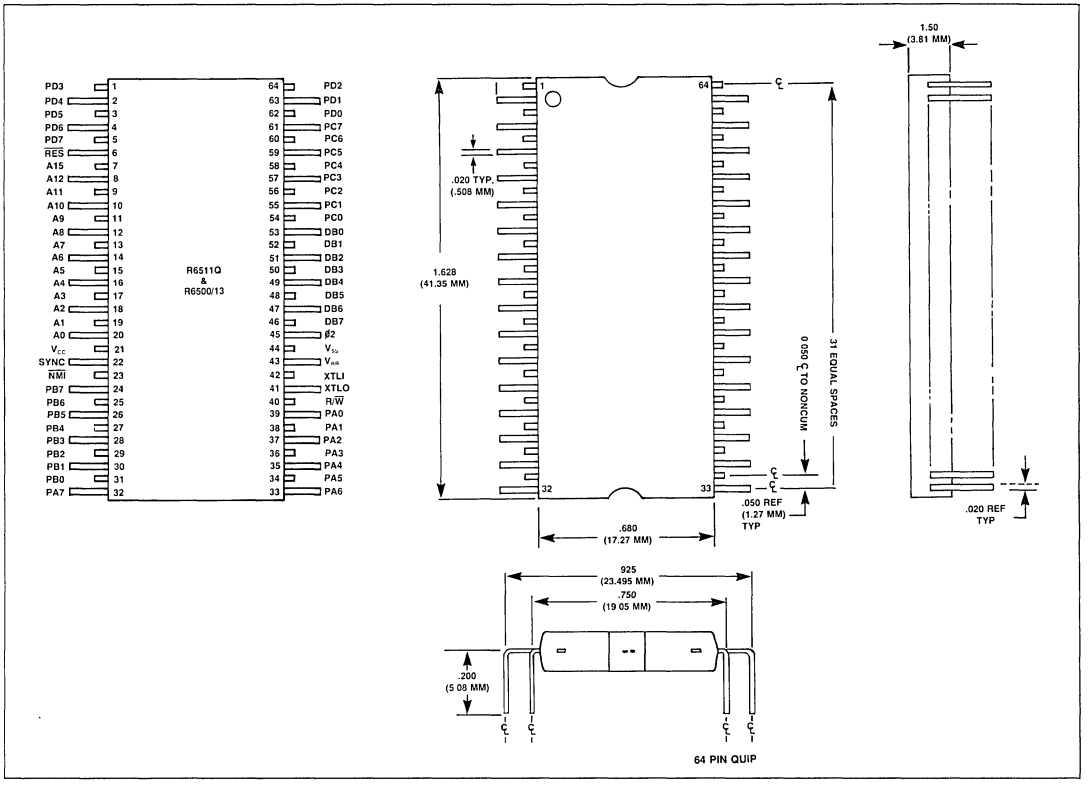


Figure 2-1. Mechanical Outline & Pin Out Configuration

SECTION 2
INTERFACE REQUIREMENTS

This section describes the interface requirements for the R6511Q and R6500/13. Figure 2-1 and 2-2 show the Interface Diagram and the pin out configuration for both devices. Table 2-1 describes the function of each pin. Figure 3-1 has a detailed block diagram of the R6500/13 ports which illustrates the internal function of the device.

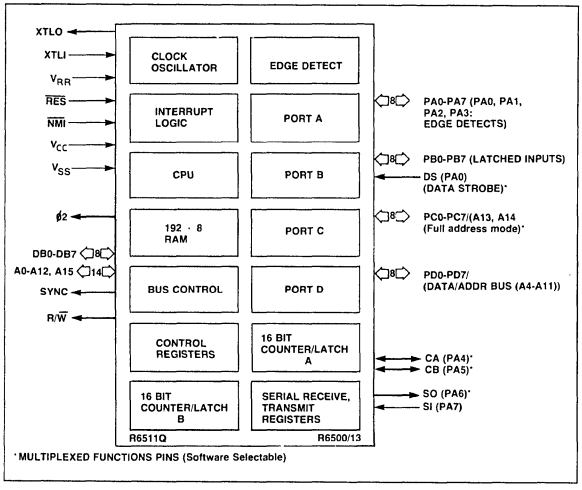


Figure 2-2. Interface Diagram

Table 2-1. R6500/13 Pin Descriptions

Signal Name	Pin No.	Description
V_{CC}	21	Main power supply +5V
V_{RR}	43	Separate power pin for RAM. In the event that V_{CC} power is off, this power retains RAM data.
V_{SS}	44	Signal and power ground (0V)
XTLI	42	Crystal or clock input for internal clock oscillator. Also allows input of X1 clock signal if XTLO is connected to V_{SS}, or X2 or X4 clock if XTLO is floated.
XTLO	41	Crystal output from internal clock oscillator.
$\overline{RES}$	6	The Reset input is used to initialize the device. This signal must not transition from low to high for at least eight cycles after V_{CC} reaches operating range and the internal oscillator has stabilized.
$\phi 2$	45	Clock signal output at internal frequency.
$\overline{NMI}$	23	A negative going edge on the Non-Maskable Interrupt signal requests that a non-maskable interrupt be generated with the CPU.
PA0-PA7 PB0-PB7 PC0-PC7 PD0-PD7	39-32 31-24 54-61 62-64, 1-5	Four 8-bit ports used for either input/output. Each line of Ports A, B and C consists of an active transistor to V_{SS} and an optional passive pull-up to V_{CC}. In the abbreviated or multiplexed modes of operation Port C has an active pull-up transistor. Port D functions as either an 8-bit input or 8-bit output port. It has active pull-up and pull-down transistors.
A0-A12, A15	20-7	Fourteen address lines used to address a complete 65K external address space. Note: A13 & A14 are sourced through PC6 & PC7 when in the Full Address Mode.
DB0-DB7	53-46	Eight bidirectional data bus lines used to transmit data to and from external memory.
SYNC	22	SYNC is a positive going signal for the full clock cycle whenever the CPU is performing an OP CODE fetch.
R/$\overline{W}$	40	Controls the direction of data transfer between the CPU and the external 65K address space. The signal is high when reading and low when writing.

SECTION 3
SYSTEM ARCHITECTURE

This section provides a functional description of the R6500/13. Functionally the R6500/13 consists of a CPU, both RAM and optional ROM memories, four 8-bit parallel I/O ports, a serial I/O port, dual counter/latch circuits, a mode control register, and an interrupt flag/enable dual register circuit. A block diagram of the system is shown in Figure 3-1.

NOTE

Throughout this document, unless specified otherwise, all memory or register address locations are specified in hexadecimal notation.

3.1 CPU LOGIC

The R6500/13 internal CPU is a standard 6502 configuration with an 8-bit Accumulator register, two 8-bit Index Registers (X and Y); an 8-bit Stack Pointer register, an ALU, a 16-bit Program Counter, and standard instruction register/decode and internal timing control logic.

3.1.1 Accumulator

The accumulator is a general purpose 8-bit register that stores the results of most arithmetic and logic operations. In addition, the accumulator usually contains one of the two data words used in these operations.

3.1.2 Index Registers

There are two 8-bit index registers, X and Y. Each index register can be used as a base to modify the address data program counter and thus obtain a new address—the sum of the program counter contents and the index register contents.

When executing an instruction which specifies indirect addressing, the CPU fetches the op code and the address and modifies the address from memory by adding the index register to it prior to loading or storing the value of memory.

Indexing greatly simplifies many types of programs, especially those using data tables.

3.1.3 Stack Pointer

The Stack Pointer is an 8-bit register. It is automatically incremented and decremented under control of the microprocessor to perform stack manipulation in response to either user instructions, an internal $\overline{IRQ}$ interrupt, or the external interrupt line $\overline{NMI}$. The Stack Pointer must be initialized by the user program.

The stack allows simple implementation of multiple level interrupts, subroutine nesting and simplification of many types of data manipulation. The JSR, BRK, RTI and RTS instructions use the stack and Stack Pointer.

The stack can be envisioned as a deck of cards which may be accessed only from the top. The address of a memory location is stored (or "pushed") onto the stack. Each time data are to be pushed onto the stack, the Stack Pointer is placed on the Address Bus, data are written into the memory location addressed by the Stack Pointer, and the Stack Pointer is decremented by 1. Each time data are read (or "pulled") from the stack, the Stack Pointer is incremented by 1. The Stack Pointer is then placed on the Address Bus and data are read from the memory location addressed by the Pointer.

The stack is located on zero page, i.e., memory locations 00FF-0040. After reset, which leaves the Stack Pointer indeterminate, normal usage calls for its initialization at 00FF.

3.1.4 Arithmetic And Logic Unit (ALU)

All arithmetic and logic operations take place in the ALU, including incrementing and decrementing internal registers (except the Program Counter). The ALU cannot store data for more than one cycle. If data are placed on the inputs to the ALU at the beginning of a cycle, the result is always gated into one of the storage registers or to external memory during the next cycle.

Each bit of the ALU has two inputs. These inputs can be tied to various internal buses or to a logic zero; the ALU then generates the function (AND, OR, SUM, and so on) using the data on the two inputs.

3.1.5 Program Counter

The 16-bit Program Counter provides the addresses that are used to step the processor through sequential instructions in a program. Each time the processor fetches an instruction from program memory, the lower (least significant) byte of the Program Counter (PCL) is placed on the low-order bits of the Address Bus and the higher (most significant) byte of the Program Counter (PCH) is placed on the high-order 8 bits of the Address Bus. The Counter is incremented each time an instruction or data is fetched from program memory.

3.1.6 Instruction Register and Instruction Decode

Instructions are fetched from ROM or RAM and gated onto the Internal Data Bus. These instructions are latched into the Instruction Register, then decoded along with timing and interrupt signals to generate control signals for the various registers.

3.1.7 Timing Control

The Timing Control Logic keeps track of the specific instruction cycle being executed. This logic is set to T0 each time an instruction fetch is executed and is advanced at the beginning of each Phase One clock pulse for as many cycles as are required to complete the instruction. Each data transfer which takes place between the registers is caused by decoding the contents of both the instruction register and timing control unit.

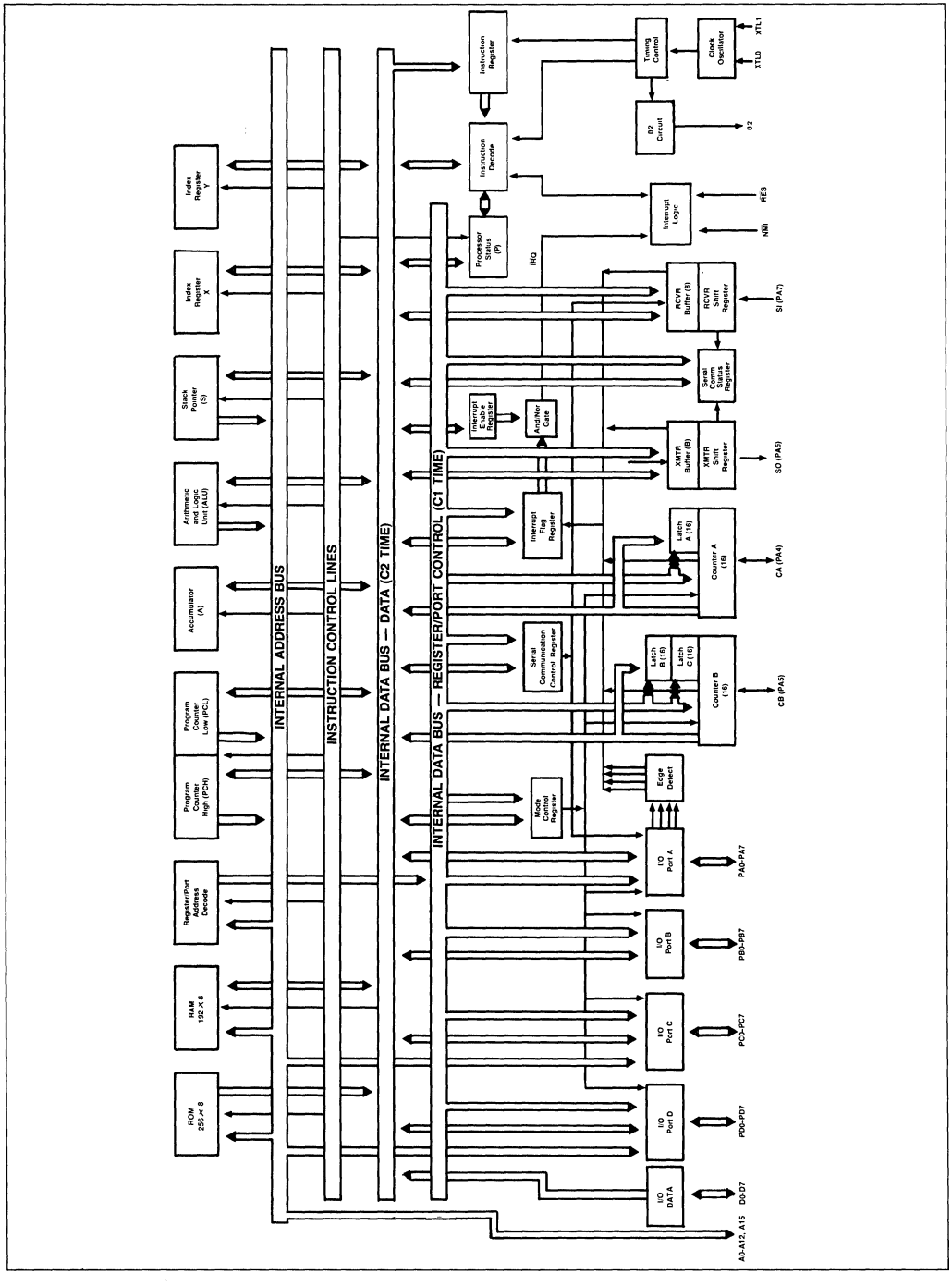


Figure 3-1. Detailed Block Diagram

3.1.8 Interrupt Logic

Interrupt logic controls the sequencing of three interrupts; $\overline{RES}$, $\overline{NMI}$ and $\overline{IRQ}$. $\overline{IRQ}$ is generated by any one of eight conditions: 2 Counter Overflows, 2 Positive Edge Detects, 2 Negative Edge Detects, and 2 Serial Port Conditions.

3.2 NEW INSTRUCTIONS

In addition to the standard R6502 instruction set, four new bit manipulation instructions have been added to the R6500/13. The added instructions and their format are explained in the following paragraphs. Refer to Appendix A for the Op Code mnemonic addressing matrix for these added instructions. The four added instructions do not impact the CPU processor status register.

3.2.1 Set Memory Bit (SMB m, Addr.)

This instruction sets to "1" one of the 8-bit data field specified by the zero page address (memory or I/O port). The first byte of the instruction specifies the SMB operation and one of eight bits to be set. The second byte of the instruction designates address (0-255) of the byte to be operated upon.

3.2.2 Reset Memory Bit (RMB m, Addr.)

This instruction is the same operation and format as SMB instruction except a reset to "0" of the bit results.

3.2.3 Branch On Bit Set Relative (BBS m, Addr, DEST)

This instruction tests one of eight bits designated by a 3-bit immediate field within the first byte of the instruction. The second byte is used to designate the address of the byte to be tested within the zero page address range (memory or I/O ports). The third byte of the instruction is used to specify the 8-bit relative address to which the instruction branches if the bit tested is a "1". If the bit tested is not set, the next sequential instruction is executed.

3.2.4 Branch On Bit Reset Relative (BBR m, Addr, DEST)

This instruction is the same operation and format as the BBS instruction except that a branch takes place if the bit tested is a "0".

3.3 READ-ONLY-MEMORY (ROM)

The optional ROM consists of 256 bytes mask programmable memory with an address space from 7F00 to 7FFF. ROM locations FFFA to FFFF are assigned for interrupt vectors. The reset vector can be optionally at 7FFE or FFFC.

The R6511Q has no ROM and its Reset vector is at FFFC.

3.4 RANDOM ACCESS MEMORY (RAM)

The RAM consists of 192 bytes of read/write memory with an assigned page zero address of 0040 through 00FF. The R6500/13 provides a separate power pin (V_{RR}) which may be used for standby power for 32 bytes located at 0040-005F. In the event of the loss of V_{CC} power, the lowest 32 bytes of RAM data will be retained if standby power is supplied to the V_{RR} pin. If the RAM data retention is not required then V_{RR} must be connected to V_{CC}. During operation V_{RR} must be at the V_{CC} level.

For the RAM to retain data upon loss of V_{CC}, V_{RR} must be supplied within operating range and $\overline{RES}$ must be driven low at least eight Ø2 clock pulses before V_{CC} falls out of operating range. $\overline{RES}$ must then be held low while V_{CC} is out of operating range and until at least eight Ø2 clock cycles after V_{CC} is again within operating range and the internal Ø2 oscillator is stabilized. V_{RR} must remain within V_{CC} operating range during normal operation. When V_{CC} is out of operating range, V_{RR} must remain within the V_{RR} retention range in order to retain data. Figure 3.2 shows typical waveforms.

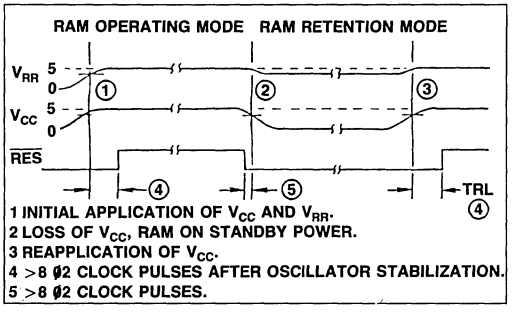


Figure 3-2. Data Retention Timing

3.5 CLOCK OSCILLATOR

The R6511Q has been configured for a crystal oscillator, a divide by 2 countdown network, and for Master Mode Operation.

Three customer selectable mask options are available for controlling the R6500/13 timing. The R6500/13 can be ordered with a *crystal* oscillator, a *divide by 2 or divide by 4* countdown network and for *clock master mode or clock slave mode* operation.

For 2MHz interval operation the divide-by-2 options must be specified.

The on-chip oscillator is designed for a parallel resonant crystal connected between XTLI and XTLO pins. The equivalent oscillator circuit is shown in Figure 3-3.

A parallel resonant crystal is specified by its load capacitance and series resonant resistance. For proper oscillator operation, the load capacitance (C_L), series resistance (R_S) and the crystal resonant frequency (F) must meet the following two relations:

$$(C + 27) = 2C_L \quad \text{or} \quad C = 2C_L - 27 \text{ pF}$$

$$R_S \leq R_{Smax} = \frac{2 \times 10^6}{(FC_L)^2}$$

where: F is in MHz; C and C_L are in pF; R is in ohms.

To select a parallel resonant crystal for the oscillator, first select the load capacitance from a Crystal Manufacturer's catalog. Next, calculate R_{Smax} based on F and C_L. The selected crystal must have a R_S less than the R_{Smax}.

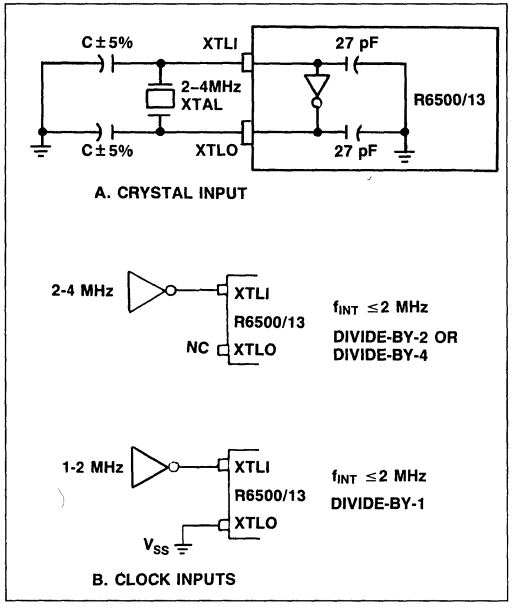


Figure 3-3. Clock Oscillator Input Options

For example, if C_L = 22 pF for a 4 MHz parallel resonant crystal, then

$$C = (2 \times 22) - 27 = 17 \text{ pF}$$
(use standard value of 18 pF)

The series resistance of the crystal must be less than

$$R_{Smax} = \frac{2 \times 10^6}{(4 \times 22)^2} = 258 \text{ ohms}$$

Internal timing can also be controlled by driving the XTLI pin with an external frequency source. Figure 3-3b shows typical connections. If XTLO is left floating, the external source is divided by the internal countdown network. However, if XTLO is tied to V_{SS}, the internal countdown network is bypassed causing the chip to operate at the frequency of the external source.

The operation described above assumed a CLOCK MASTER MODE mask option. In this mode a frequence source (crystal or external source) must be applied to the XTLI and XTLO pins.

Ø2 is a buffered output signal which closely approximates the interal timing. When a common external source is used to drive multiple devices the internal timing between devices as well as their Ø2 outputs will be skewed in time. If skewing represents a system problem it can be avoided by the Master/Slave connection and options shown in Figure 3-4.

One R6500/13 is operated in the CLOCK MASTER MODE and a second in the CLOCK SLAVE MODE. Mask options in the SLAVE unit convert to Ø2 signal into a clock input pin which is tightly coupled to the internal timing generator. As a result the internal timing of the MASTER and SLAVE units are synchronized with minimum skew. If the Ø2 signal to the SLAVE unit is inverted, the MASTER and SLAVE UNITS WILL OPERATE OUT OF PHASE. This approach allows the two devices to share external memory using cycle stealing techniques.

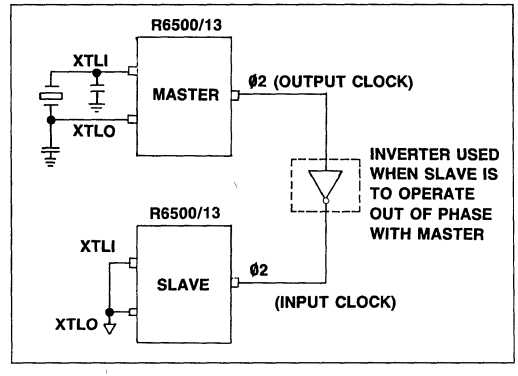


Figure 3-4. Master/Slave Connections

3.6 MODE CONTROL REGISTER (MCR)

The Mode Control Register contains control bits for the multifunction I/O ports and mode select bits for Counter A and Counter B. Its setting, along with the setting of the Serial Communications Control Register (SCCR), determines the basic configuration of the R6500/13 in any application. Initializing this register is one of the first actions of any software program. The Mode Control Register bit assignment is shown in Figure 3-5.

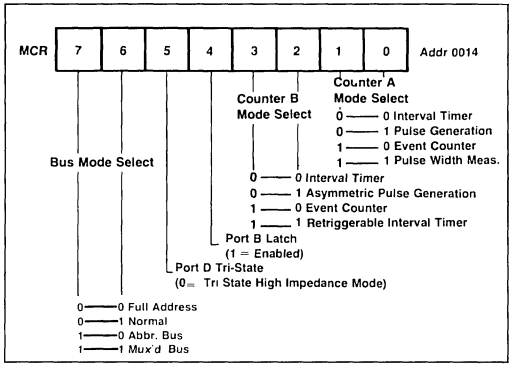


Figure 3-5. Mode Control Register

The use of Counter A Mode Select is shown in Section 6.1.

The use of Counter B Mode Select is shown in Section 6.2.

The use of Port B Latch Enable is shown in Section 4.4.

The use of Port D in Tri-State Enable is shown in Section 4.6.

The use of Bus Mode Select is shown in Section 4.5 and 4.6.

3.7 INTERRUPT FLAG REGISTER (IFR) AND INTERRUPT ENABLE REGISTER (IER)

An $\overline{IRQ}$ interrupt request can be initiated by any or all of eight possible sources. These sources are all capable of being enabled or disabled by the use of the appropriate interrupt enabled bits in the Interrupt Enable Register (IER). Multiple simultaneous interrupts cause the $\overline{IRQ}$ interrupt request to remain active until all interrupting conditions have been serviced and cleared.

The Interrupt Flag Register contains the information that indicates which I/O or counter needs attention. The contents of the Interrupt Flag Register may be examined at any time by reading at address: 0011. Edge detect IFR bits may be cleared by executing a RMB instruction at address location 0010. The RMB X, (0010) instruction reads FF, modifies bit X to a "0", and writes the modified value at address location 0011. In this way IFR bits set to a "1" after the read cycle of a Read-Modify-Write instruction (such as RMB) are protected from being cleared. A logic "1" is ignored when writing to edge detect IFR bits.

Each IFR bit has a corresponding bit in the Interrupt Enable Register which can be set to a "1" by writing a "1" in the respective bit position at location 0012. Individual IER bits may be cleared by writing a "0" in the respective bit position, or by $\overline{RES}$. If set to a "1", an IRQ will be generated when the corresponding IFR bit becomes true. The Interrupt Flag Register and Interrupt Enable Register bit assignments are shown in Figure 3-6 and the functions of each bit are explained in Table 3-1.

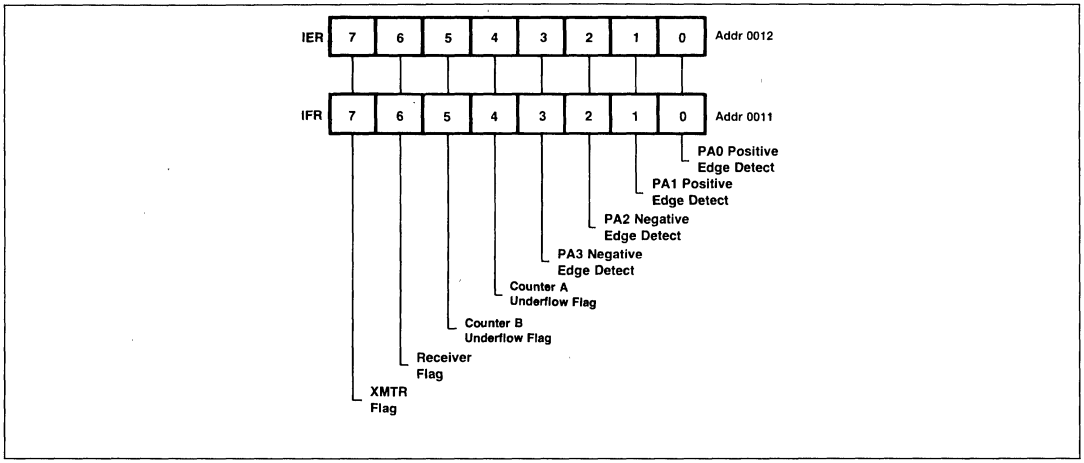


Figure 3-6. Interrupt Enable and Flag Registers

Table 3-1. Interrupt Flag Register Bit Codes

Bit Code	Function
IFR 0:	PA0 Positive Edge Detect Flag—Set to a "1" when a positive going edge is detected on PA0. Cleared by RMB O (0010) instruction or by $\overline{RES}$.
IFR 1:	PA1 Positive Edge Detect Flag—Set to a 1 when a positive going edge is detected on PA1. Cleared by RMB 1 (0010) instruction or by $\overline{RES}$.
IFR 2:	PA2 Negative Edge Detect Flag—Set to a 1 when a negative going edge is detected on PA2. Cleared by RMB 2 (0010) instruction or by $\overline{RES}$.
IFR 3:	PA3 Negative Edge Detect Flag—Set to 1 when a negative going edge is detected on PA3. Cleared by RMB 3 (0010) instruction or by $\overline{RES}$.
IFR 4:	Counter A Underflow Flag—Set to a 1 when Counter A underflow occurs. Cleared by reading the Lower Counter A at location 0018, by writing to address location 001A, or by $\overline{RES}$.
IFR 5:	Counter B Underflow Flag—Set to a 1 when Counter B underflow occurs. Cleared by reading the Lower Counter B at location 001C, by writing to address location 001E, or by $\overline{RES}$.
IFR 6:	Receiver Interrupt Flag—Set to a 1 when any of the Serial Communication Status Register bits 0 through 3 is set to a 1. Cleared when the Receiver Status bits (SCSR 0-3) are cleared or by $\overline{RES}$.
IFR 7:	Transmitter Interrupt Flag—Set to a 1 when SCSR 6 is set to a 1 while SCSR 5 is a 0 or SCSR 7 is set to a 1. Cleared when the Transmitter Status bits (SCSR 6 & 7) are cleared or by $\overline{RES}$.

3.8 PROCESSOR STATUS REGISTER

The 8-bit Processor Status Register, shown in Figure 3-7, contains seven status flags. Some of these flags are controlled by the user program; others may be controlled both by the user's program and the CPU. The R6502 instruction set contains a number of conditional branch instructions which are designed to allow testing of these flags. Each of the eight processor status flags is described in the following sections.

3.8.1 Carry Bit (C)

The Carry Bit (C) can be considered as the ninth bit of an arithmetic operation. It is set to logic 1 if a carry from the eighth bit has occurred or cleared to logic 0 if no carry occurred as the result of arithmetic operations.

The Carry Bit may be set or cleared under program control by use of the Set Carry (SEC) or Clear Carry (CLC) instruction, respectively. Other operations which affect the Carry Bit are ADC, ASL, CMP, CPX, CPY, LSR, PLP, ROL, ROR, RTI, and SBC.

3.8.2 Zero Bit (Z)

The Zero Bit (Z) is set to logic 1 by the CPU during any data movement or calculation which sets all 8 bits of the result to zero. This bit is cleared to logic 0 when the resultant 8 bits of a data movement or calculation operation are not all zero. The R6500 instruction set contains no instruction to specifically set or clear the Zero Bit. The Zero Bit is, however, affected by the following instructions; ADC, AND, ASL, BIT, CMP, CPX, CPY, DEC, DEX, DEY, EOR, INC, INX, INY, LDA, LDX, LDY, LSR, ORA, PLA, PLP, ROL, ROR, RTI, SBC, TAX, TAY, TXA, TSX, and TYA.

3.8.3 Interrupt Disable Bit (I)

The Interrupt Disable Bit (I) is used to control the servicing of an interrupt request ($\overline{IRQ}$). If the I Bit is reset to logic 0, the $\overline{IRQ}$ signal will be serviced. If the bit is set to logic 1, the $\overline{IRQ}$ signal will be ignored. The CPU will set the Interrupt Disable Bit to logic 1 if a RESET ($\overline{RES}$), $\overline{IRQ}$, or Non-Maskable Interrupt ($\overline{NMI}$) signal is detected.

The I bit is cleared by the Clear Interrupt Mask Instruction (CLI) and is set by the Set Interrupt Mask Instruction (SEI). This bit is set by the BRK Instruction. The Return from Interrupt (RTI) and Pull Processor Status (PLP) instructions will also affect the I bit.

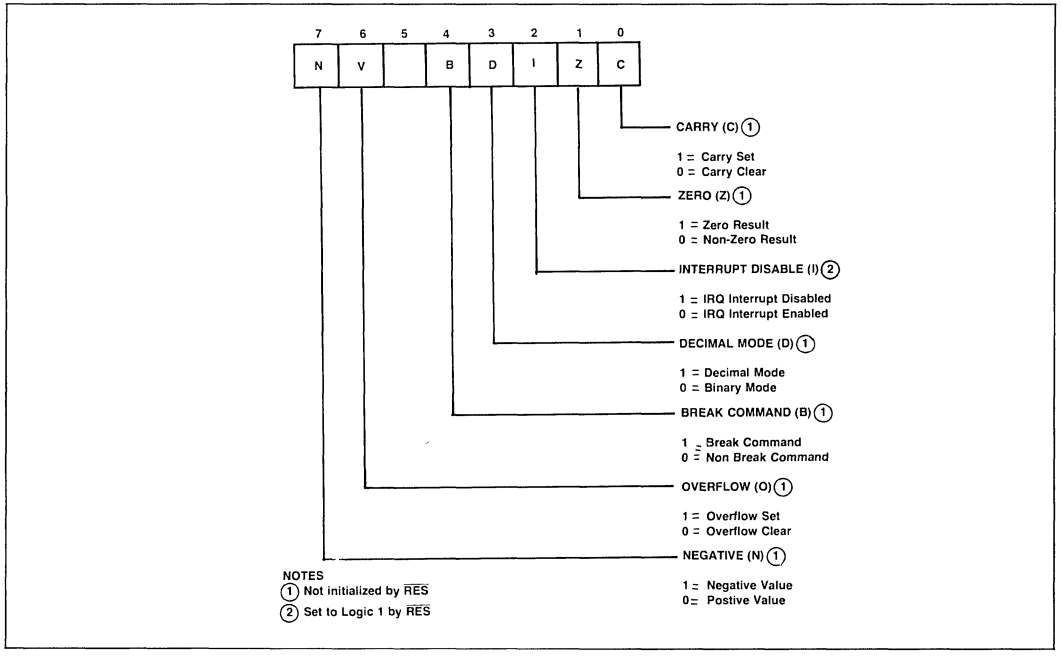


Figure 3-7. Processor Status Register

3.8.4 Decimal Mode Bit (D)

The Decimal Mode Bit (D) is used to control the arithmetic mode of the CPU. When this bit is set to logic 1, the adder operates as a decimal adder. When this bit is cleared to logic 0, the adder operates as a straight binary adder. The adder mode is controlled only by the programmer. The Set Decimal Mode (SED) instruction will set the D bit; the Clear Decimal Mode (CLD) instruction clears it. The PLP and RTI instructions also affect the Decimal Mode Bit.

CAUTION

The Decimal Mode Bit will either set or clear in an unpredictable manner upon power application. This bit must be initialized to the desired state by the user program or erroneous results may occur.

3.8.5 Break Bit (B)

The Break Bit (B) is used to determine the condition which caused the $\overline{IRQ}$ service routine to be entered. If the $\overline{IRQ}$ service routine was entered because the CPU executed a BRK command, the Break Bit will be set to logic 1. If the $\overline{IRQ}$ routine was entered as the result of an $\overline{IRQ}$ signal being generated, the B bit will be cleared to logic 0. There are no instructions which can set or clear this bit.

3.8.6 Overflow Bit (V)

The Overflow Bit (V) is used to indicate that the result of a signed, binary addition, or subtraction, operation is a value that cannot be contained in seven bits ($-128 \leq n \leq 127$). This indicator only has meaning when signed arithmetic (sign and seven magnitude bits) is performed. When the ADC or SBC instruction is performed, the Overflow Bit is set to logic 1 if the polarity of the sign bit (bit 7) is changed because the result exceeds +127 or −128; otherwise the bit is cleared to logic 0. The V bit may also be cleared by the programmer using a Clear Overflow (CLV) instruction.

The Overflow Bit may also be used with the BIT instruction. The BIT instruction—which may be used to sample interface devices—allows the overflow flag to reflect the condition of bit 6 in the sampled field. During a BIT instruction the Overflow Bit is set equal to the content of the bit 6 on the data tested with BIT instruction. When used in this mode, the overflow has nothing to do with signed arithmetic, but is just another sense bit for the microprocessor. Instructions affecting the V flag are ADC, BIT, CLV, PLP, RTI and SBC.

3.8.7 Negative Bit (N)

The Negative Bit (N) is used to indicate that the sign bit (bit 7) in the resulting value of a data movement or data arithmetic operation is set to logic 1. If the sign bit is set to logic 1, the resulting value of the data movement or arithmetic operation is negative; if the sign bit is cleared, the result of the data movement or arithmetic operation is positive. There are no instructions that set or clear the Negative Bit since the Negative Bit represents only the status of a result. The instructions that effect the state of the Negative Bit are: ADC, AND, ASL, BIT, CMP, CPX, CPY, DEC, DEX, DEY, EOR, INC, INX, INY, LDA, LDX, LDY, LSR, ORA, PLA, PLP, ROL, ROR, RTI, SBC, TAX, TAY, TSX, TXA, and TYA.

SECTION 4
PARALLEL INPUT/OUTPUT PORTS & BUS MODES

The devices have 32 I/O lines grouped into four 8-bit ports (PA, PB, PC, and PD). Ports A through C may be used either for input or output individually or in groups of any combination. Port D may be used as all inputs or all outputs.

Multifunction I/O's such as Port A and Port C are protected from normal port I/O instructions when they are programmed to perform a multiplexed function.

Internal pull-up resistors (FET's with an impedance range of $3K \leq R_L \leq 12K$ ohm) are optional on all port pins except Port D (R6500/13 only).

The direction of the 32 I/O lines are controlled by four 8-bit port registers located in page zero. This arrangement provides quick programming access using simple two-byte zero page address instructions. There are no direction registers associated with the I/O ports, thus simplifying I/O handling. The I/O addresses are shown in Table 4-1. Appendix E.6 shows the I/O Port Timing.

Table 4-1. I/O Port Addresses

Port	Address
A	0000
B	0001
C	0002
D	0003

4.1 INPUTS

Inputs for Ports A, B, and C are enabled by loading logic 1 into all I/O port register bit positions that are to correspond to I/O input lines. A low (<0.8V) input signal will cause a logic 0 to be read when a read instruction is issued to the port register. A high (>2.0V) input will cause a logic 1 to be read. An $\overline{RES}$ signal forces all I/O port registers to logic 1 thus initially treating all I/O lines as inputs.

Port D may only be all inputs or all outputs. All inputs is selected by setting bit 5 of the Mode Control Register (MCR5) to a "0".

The status of the input lines can be interrogated at any time by reading the I/O port addresses. Note that this will return the actual status of the input lines, not the data written into the I/O port registers.

Read/Modify/Write instructions can be used to modify the operation of PA, PB, PC, & PD. During the Read cycle of a Read/Modify/Write instruction the Port I/O register is read. For all other read instructions the port input lines are read. Read/Modify/Write instructions are: ASL, DEC, INC, LSR, RMB, ROL, ROR, and SMB.

4.2 OUTPUTS

Outputs for Ports A thru D are controlled by writing the desired I/O line output states into the corresponding I/O port register bit positions. A logic 1 will force a high (>2.4V) output while a logic 0 will force a low (<0.4V) output.

Port D all outputs is selected by setting MCR5 to a "1".

4.3 Port A (PA)

Port A can be programmed via the Mode Control Register (MCR) and the Serial Communications Control Register (SCCR) as a standard parallel 8-bit, bit independent, I/O port or as serial channel I/O lines, counter I/O lines, or an input data strobe for the Port B input latch option. Table 4-2 tabulates the control and usage of Port A.

In addition to their normal I/O functions, PA0 and PA1 can detect positive going edges and PA2 and PA3 can detect negative going edges. A proper transition on these pins will set a corresponding status bit in the IFR and generate an interrupt request if the respective Interrupt Enable Bit is set. The maximum rate at which an edge can be detected is one-half the $\emptyset 2$ clock rate. Edge detection timing is shown in Appendix E.5.

Table 4-2. Port A Control & Usage

PA0 (2) PIN 39

PA0 I/O		PORT B LATCH MODE	
MCR4 = 0		MCR4 = 1	
SIGNAL		SIGNAL	
NAME	TYPE	NAME	TYPE
PA0	I/O	PORT B LATCH STROBE	INPUT (1)

PA1 (2) PIN 38
PA2 (3) PIN 37
PA3 (3) PIN 36

PA1-PA3 I/O	
SIGNAL	
NAME	TYPE
PA1 PA2 PA3	I/O I/O I/O

PA4 PIN 35

PA4 I/O		COUNTER A I/O			
MCR0 = 0 MCR1 = 0 SCCR7 = 0 RCVR S/R MODE = 0 (4) (5)		MCR0 = 1 MCR1 = 0 SCCR7 = 0 RCVR S/R MODE = 0 (4)		SCCR7 = 0 SCCR6 = 0 MCR1 = 1	
SIGNAL		SIGNAL		SIGNAL	
NAME	TYPE	NAME	TYPE	NAME	TYPE
PA4	I/O	CNTA	OUTPUT	CNTA	INPUT (1)

SERIAL I/O SHIFT REGISTER CLOCK			
SCCR7 = 1 SCCR5 = 1		RCVR S/R MODE = 1 (4)	
SIGNAL		SIGNAL	
NAME	TYPE	NAME	TYPE
XMTR CLOCK	OUTPUT	RCVR CLOCK	INPUT (1)

PA5 PIN 34

PA5 I/O		COUNTER B I/O			
MCR3 = 0 MCR2 = 0		MCR3 = 0 MCR2 = 1		MCR3 = 1 MCR2 = X	
SIGNAL		SIGNAL		SIGNAL	
NAME	TYPE	NAME	TYPE	NAME	TYPE
PA5	I/O	CNTB	OUTPUT	CNTB	INPUT (1)

PA6 PIN 33

PA6 I/O		SERIAL I/O XMTR OUTPUT	
SCCR7 = 0		SCCR7 = 1	
SIGNAL		SIGNAL	
NAME	TYPE	NAME	TYPE
PA6	I/O	XMTR	OUTPUT

PA7 PIN 32

PA7 I/O		SERIAL I/O RCVR INPUT	
SCCR6 = 0		SCCR6 = 1	
SIGNAL		SIGNAL	
NAME	TYPE	NAME	TYPE
PA7	I/O	RCVR	INPUT (1)

(1) Hardware Buffer Float
(2) Positive Edge Detect
(3) Negative Edge Detect
(4) RCVR S/R Mode = 1 when SCCR6 • $\overline{\text{SCCR5}}$ • SCCR4 = 1
(5) For the following mode combinations PA4 is available as an input only pin:
SCCR7•SCCR6•SCCR5•MCR1
+ SCCR7•SCCR6•7SCCR4•MCR1
+ SCCR7•SCCR6•SCCR5
+ SCCR7•SCCR5C•SCCR4.

4.4 PORT B (PB)

Port B can be programmed as an 8-bit, bit-independent I/O port. It has a latched input capability which may be enabled or disabled via the Mode Control Register (MCR). Table 4-3 tabulates the control and usage of Port B. An Input Data Strobe signal must be provided thru PA0 when Port B is programmed to be used with latched input option. Input data latch timing for Port B is shown in Appendix E.5.

Table 4-3. Port B Control & Usage

		I/O Mode		Latch Mode	
		MCR4 = 0		MCR4 = 1 (2)	
		Signal		Signal	
Pin #	Pin Name	Name	Type (1)	Name	Type
31	PB0	PB0	I/O	PB0	INPUT
30	PB1	PB1	I/O	PB1	INPUT
29	PB2	PB2	I/O	PB2	INPUT
28	PB3	PB3	I/O	PB3	INPUT
27	PB4	PB4	I/O	PB4	INPUT
26	PB5	PB5	I/O	PB5	INPUT
25	PB6	PB6	I/O	PB6	INPUT
24	PB7	PB7	I/O	PB7	INPUT

(1) Resistive Pull-Up, Active Buffer Pull-Down
(2) Input data is stored in Port B latch by PA0 Pulse

4.5 PORT C (PC)

Port C can be programmed as an I/O port, as part of the full address bus, and, in conjunction with Port D, as an abbreviated bus, or as a multiplexed bus. When operating in the Full Address Mode PC6 and PC7 serve as A13 and A14 with PC0-PC5 operating as normal I/O pins. When used in the abbreviated or multiplexed bus modes, PC0-PC7 function as A0-A3, A12, R/W, A13, and $\overline{EMS}$, respectively, as shown in Table 4-4. $\overline{EMS}$ (External Memory Select) is asserted (low) whenever the internal processor accesses memory area between 0100 and 3FFF. (See Memory Map, Appendix B). The leading edge of $\overline{EMS}$ may be used to strobe the eight address lines multiplexed on Port D in the Multiplexed Bus Mode. See Appendices E.3 through E.5 for Port C timing.

4.6 PORT D (PD)

Port D can be programmed as an I/O Port, an 8-bit tri-state data bus, or as a multiplexed bus. Mode selection for Port D is made by the Mode Control Register (MCR). The Port D output drivers can be selected as tri-state drivers by setting bit 5 of the MCR to 1 (one). Table 4-5 shows the necessary settings for the MCR to achieve the various modes for Port D. When Port D is selected to operate in the Abbreviated Mode PD0–PD7 serves as data register bits D0–D7. When Port D is selected to operate in the Multiplexed Mode data bits D0 through D7 are time multiplexed with address bits A4 through A11, respectively. Refer to the Memory Maps (Appendix C) for Abbreviated and Multiplexed memory assignments. See Appendices E.3 through E.5 for Port D timing.

4.7 BUS MODES

A special attribute of Port C and Port D is their capability to be configured via the Mode Control Register (see Section 3.6) into four different modes.

In the Full Address Mode, the separate address and data bus are used in conjunction with PC6 and PC7, which automatically provide A13 and A14. The remaining ports perform the normal I/O function.

In the I/O Bus Mode all ports serve as I/O. The address and data bus are still functional but without A13 and A14. Since the internal RAM and registers are in the 00XX location, A15 can be used for chip select and A0–A12 used for selecting 8K of external memory. Thus, the device can be used to emulate the R6500/11 in the Normal Bus Mode.

In the Abbreviated Bus Mode, the address and data lines can be used as in the I/O Bus Mode to emulate the R6500/11. Port C and Port D are automatically transformed into an abbreviated address bus and control signals (Port C) and a bidirectional data bus (Port D). 64 Peripheral addresses can be selected. In general usage, these 64 addresses would be distributed to several external I/O devices such as R6522 and R6520, etc., each of which may contain more than one unique address.

In the Multiplexed Bus Mode, the operation is similar to the Abbreviated Mode except that a full 16K of external addresses are provided. Port C provides the lower addresses and control signals. Port D multiplexes functions. During the first half of the cycle it contains the remaining necessary 8 address bits for 16K; during the second half of the cycle it contains a bidirectional data bus. The address bits appearing on Port D must be latched into an external holding register. The leading edge of $\overline{EMS}$, which indicates that the bus function is active, may be used for this purpose.

MCR5 must be a logic 1 in the Abbreviated and Multiplexed Bus Modes.

Figures 4-1a through 4-1d show the possible configurations of the four bus modes. Figure 4-2 shows a memory map of the part as a function of the Bus Mode and further shows which adddresses are active or inactive on each of the three possible buses.

Table 4-4. Port C Control & Usage

		Full Address Mode		Normal Mode		Abbreviated Mode		Multiplexed Mode	
		MCR7 = 0 MCR6 = 0		MCR7 = 0 MCR6 = 1		MCR7 = 1 MCR6 = 0		MCR7 = 1 MCR6 = 1	
		Signal		Signal		Signal		Signal	
Pin #	Pin Name	Name	Type	Name	Type (1)	Name	Type (2)	Name	Type (2)
54	PC0	PC0	I/O (1)	PC0	I/O	A0	OUTPUT	A0	OUTPUT
55	PC1	PC1	I/O (1)	PC1	I/O	A1	OUTPUT	A1	OUTPUT
56	PC2	PC2	I/O (1)	PC2	I/O	A2	OUTPUT	A2	OUTPUT
57	PC3	PC3	I/O (1)	PC3	I/O	A3	OUTPUT	A3	OUTPUT
58	PC4	PC4	I/O (1)	PC4	I/O	A12	OUTPUT	A12	OUTPUT
59	PC5	PC5	I/O (1)	PC5	I/O	$\overline{RW}$	OUTPUT	$\overline{RW}$	OUTPUT
60	PC6	A13	OUTPUT (2)	PC6	I/O	A13	OUTPUT	A13	OUTPUT
61	PC7	A14	OUTPUT (2)	PC7	I/O	$\overline{EMS}$	OUTPUT	$\overline{EMS}$	OUTPUT

(1) Resistive Pull-Up, Active Buffer Pull-Down
(2) Active Buffer Pull-Up and Pull-Down

Table 4-5. Port D Control & Usage

		Normal Modes				Abbreviated Mode		Multiplexed Mode			
		MCR7 = 0 MCR6 = X MCR5 = 0		MCR7 = 0 MCR6 = X MCR5 = 1		MCR7 = 1 MCR6 = 0 MCR5 = 1		MCR7 = 1 MCR6 = 1 MCR5 = 1			
		Signal		Signal		Signal		Signal		Signal	
								ø2 Low		ø2 High	
Pin #	Pin Name	Name	Type (1)	Name	Type (2)	Name	Type (3)	Name	Type (2)	Name	Type (3)
62	PD0	PD0	INPUT	PD0	OUTPUT	DATA0	I/O	A4	OUTPUT	DATA0	I/O
63	PD1	PD1	INPUT	PD1	OUTPUT	DATA1	I/O	A5	OUTPUT	DATA1	I/O
64	PD2	PD2	INPUT	PD2	OUTPUT	DATA2	I/O	A6	OUTPUT	DATA2	I/O
1	PD3	PD3	INPUT	PD3	OUTPUT	DATA3	I/O	A7	OUTPUT	DATA3	I/O
2	PD4	PD4	INPUT	PD4	OUTPUT	DATA4	I/O	A8	OUTPUT	DATA4	I/O
3	PD5	PD5	INPUT	PD5	OUTPUT	DATA5	I/O	A9	OUTPUT	DATA5	I/O
4	PD6	PD6	INPUT	PD6	OUTPUT	DATA6	I/O	A10	OUTPUT	DATA6	I/O
5	PD7	PD7	INPUT	PD7	OUTPUT	DATA7	I/O	A11	OUTPUT	DATA7	I/O

(1) Tri-State Buffer is in High Impedance Mode
(2) Tri-State Buffer is in Active Mode
(3) Tri-State Buffer is in Active Mode only during the phase 2 portion of a Write Cycle

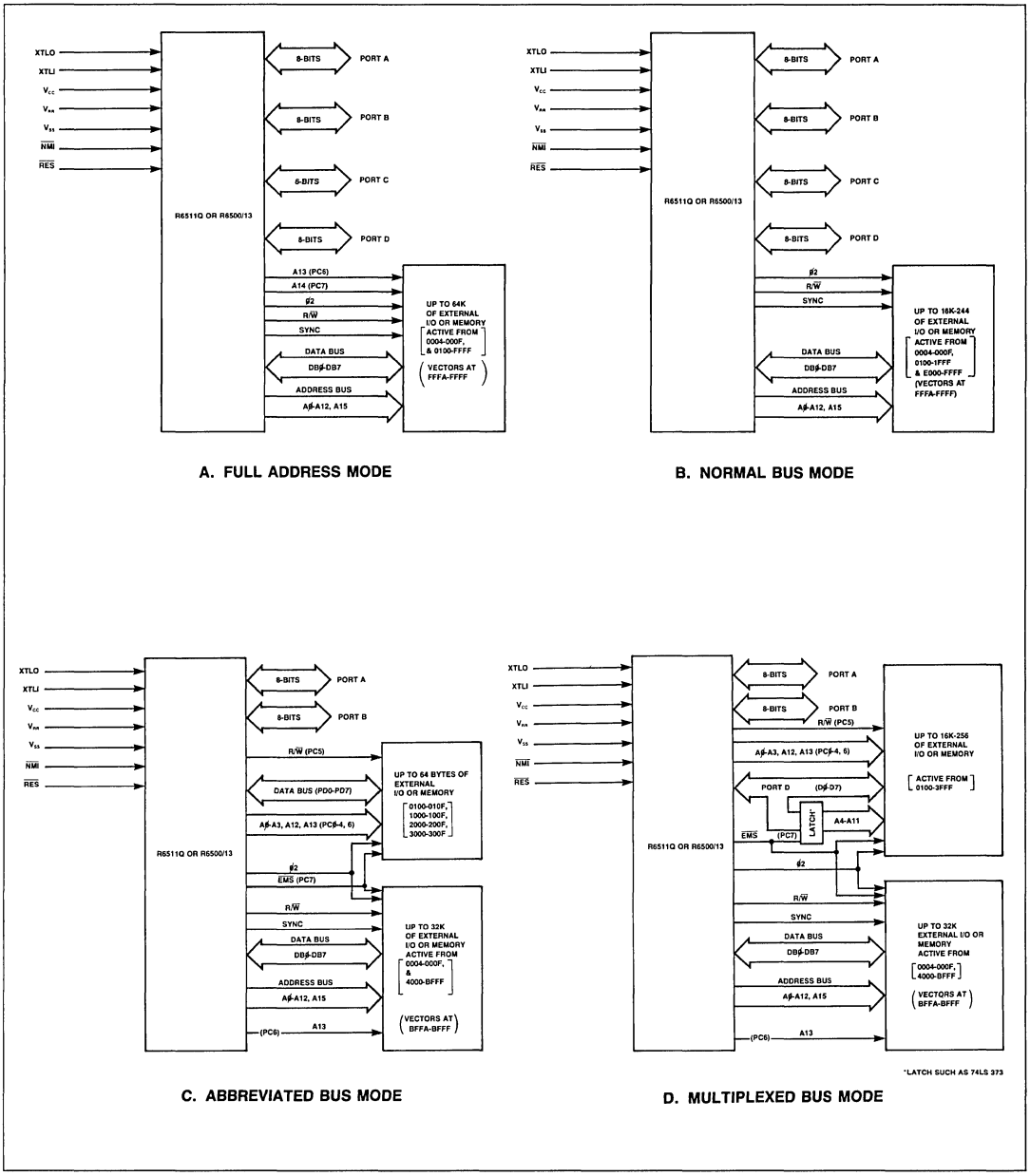


Figure 4-1. Bus Mode Configurations

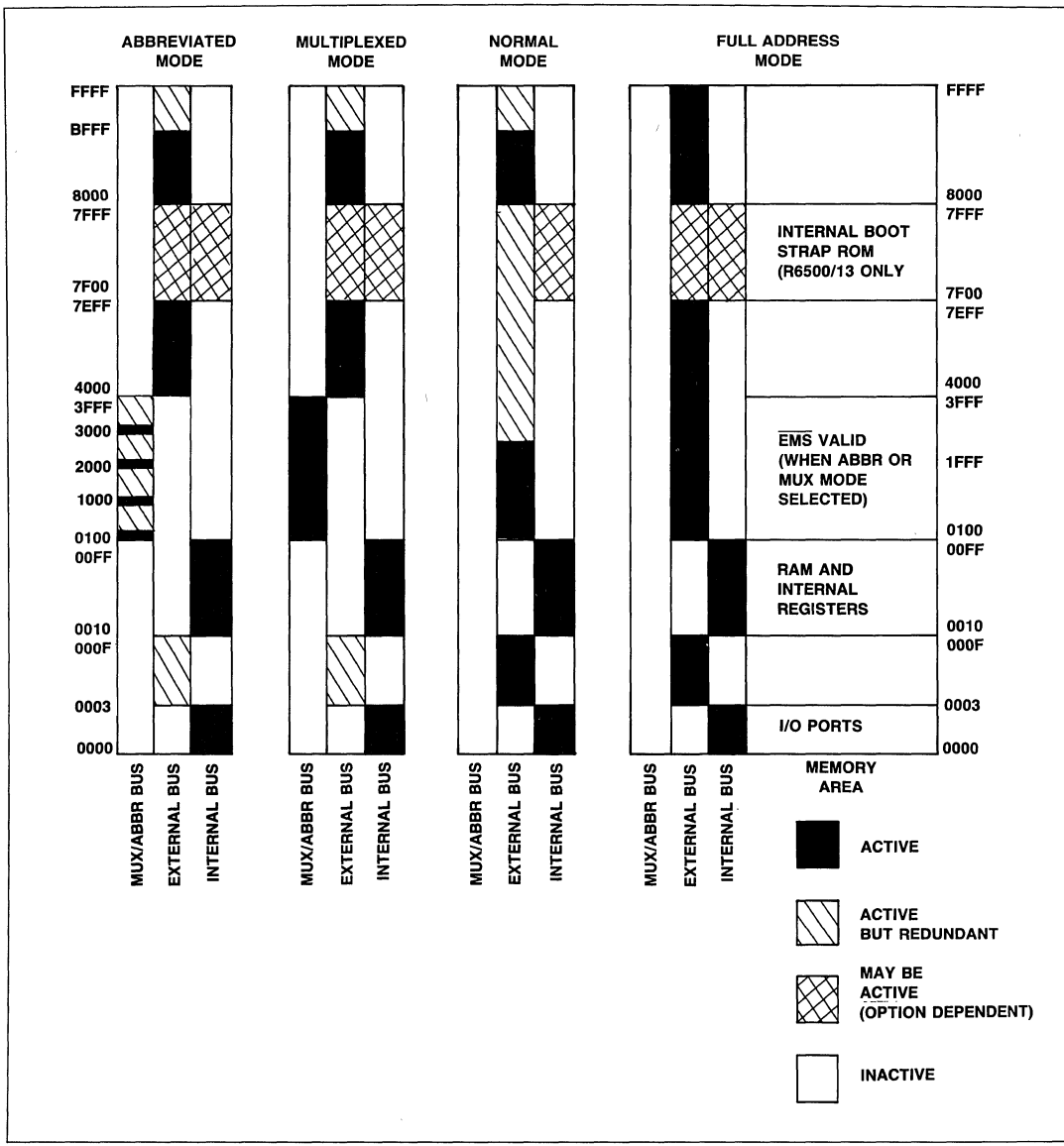


Figure 4-2. Memory Map

SECTION 5
SERIAL INPUT/OUTPUT CHANNEL

The device provides a full duplex Serial I/O channel with programmable bit rates and operating modes. The serial I/O functions are controlled by the Serial Communication Control Register (SCCR). The SCCR bit assignment is shown in Figure 5-1. The serial bit rate is determined by Counter A for all modes except the Receiver Shift Register (RCVR S/R) mode for which an external shift clock must be provided. The maximum data rate using the internal clock is 62.5K bits per second (at $\phi 2$ = 1 MHZ). The transmitter (XMTR) and receiver (RCVR) can be independently programmed to operate in different modes and can be independently enabled or disabled.

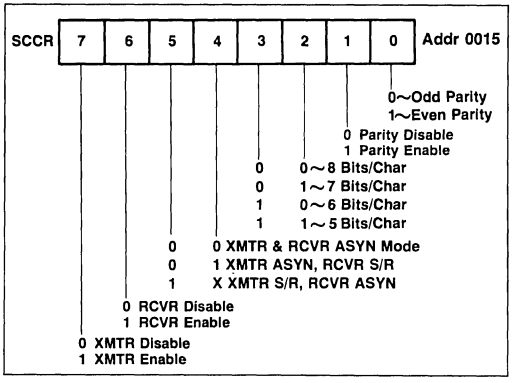


Figure 5-1. Serial Communication Control Register

Except for the Receiver Shift Register Mode (RCVR S/R), all XMTR and RCVR bit rates will occur at one sixteenth of the Counter A interval timer rate. Counter A is forced into an interval timer mode whenever the serial I/O is enabled in a mode requiring an internal clock.

Whenever Counter A is required as a timing source it must be loaded with the hexadecimal code that selects the data rate for the serial I/O Port. Refer to Counter A (paragraph 6.1) for a table of hexadecimal values to represent the desired data rate.

5.1 TRANSMITTER OPERATION (XTMR)

The XTMR operation and the transmitter related control/status functions are enabled by bit 7 of the Serial Communications Control Register (SCCR). The transmitter, when in the Asynchronous (ASYN) mode, automatically adds a start bit, one or two stop bits, and, when enabled, a parity bit to the transmitted data. A word of transmitted data (in asynchronous parity mode) can have 5, 6, 7, or 8 bits of data. The nine data modes are shown in Figure 5-2. When parity is disabled, the 5, 6, 7 or 8 bits of data are terminated with two stop bits.

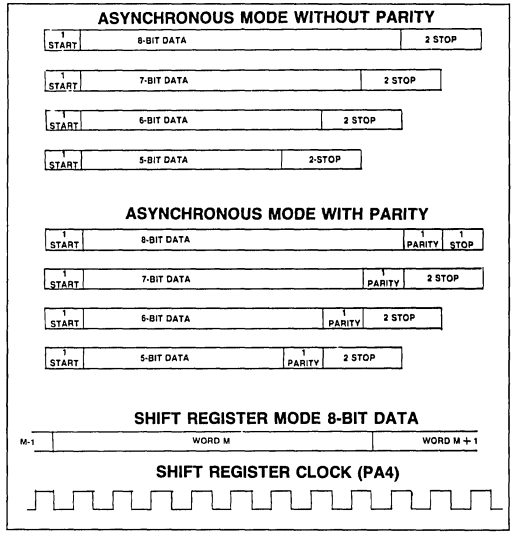


Figure 5-2. SIO Data Modes

In the S/R mode, eight data bits are always shifted out. Bits/character and parity control bits are ignored. The serial data is shifted out via the SO output (PA6) and the shift clock is available at the CA (PA4) pin. When the transmitter underruns in the S/R mode the SO output and shift clock are held in a high state.

The XMTR Interrupt Flag bit (IFR7) is controlled by Serial Communication Status Register bits SCSR5, SCSR6 and SCSR7.

$$IFR7 = SCSR6\ (\overline{SCSR5} + SCSR7)$$

5.2 RECEIVER OPERATION (RCVR)

The receiver and its selected control and status functions are enabled when SCCR-6 is set to a "1." In the ASYN mode, data format must have a start bit, the appropriate number of data bits, a parity bit (if enabled), and one stop bit. Refer to paragraph 5.1 for a diagram of bit allocations. The receiver bit period is divided into 8 sub-intervals for internal synchronization. The receiver bit stream is synchronized by the start bit and a strobe signal is generated at the approximate center of each incoming bit. Refer to Figure 5-3 for ASYN Receive Data Timing. The character assembly process does not start if the start bit signal is less than one-half the bit time after a low level is detected on the Receive Data Input. Framing error, over-run, and parity error conditions or a RCVR Data Register Full will set the appropriate status bits. Any of the above conditions will cause an Interrupt Request if the Receiver Interrupt Enable bit is set to logic 1.

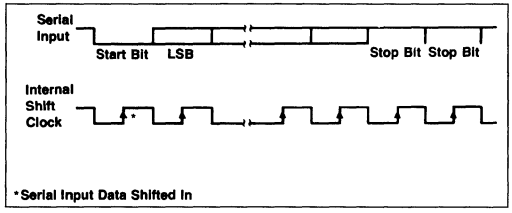


Figure 5-3. ASYN Receive Data Timing

In the S/R mode, an external shift clock must be provided at CA (PA4) pin along with 8 bits of serial data (LSB first) at the SI input (PA7). The maximum data rate using an external shift clock is one-eighth the internal clock rate. Refer to Figure 5-4 for S/R Mode Timing.

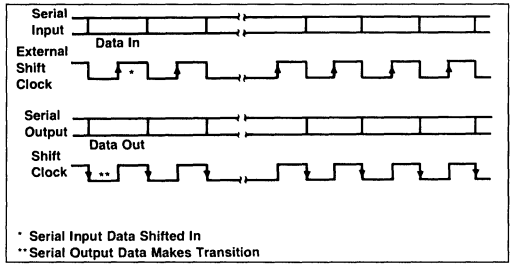


Figure 5-4. S/R Mode Timing

A RCVR interrupt (IFR6) is generated whenever any of SCSR0-3 are true.

5.3 SERIAL COMMUNICATION STATUS REGISTER (SCSR)

The Serial Communication Status Register (SCSR) holds information on various communication error conditions, status of the transmitter and receiver data registers, a transmitter end-of-transmission condition, and a receiver idle line condition (Wake-Up Feature). The SCSR bit assignment is shown in Figure 5-5. Bit assignments and functions of the SCSR are as follows:

SCSR 0: *Receiver Data Register Full*—Set to a logic 1 when a character is transferred from the Receiver Shift Register to the Receiver Data Register. This bit is cleared by reading the Receiver Data Register, or by $\overline{RES}$ and is disabled if SCCR 6 = 0. The SCSR 0 bit will not be set to a logic 1 if the received data contains an error condition; instead, a corresponding error bit will be set to a logic 1.

SCSR 1: *Over-Run Error*—Set to a logic 1 when a new character is transferred from the Receiver Shift Register with the last character still in the Receiver Data Register. This bit is cleared by reading the Receiver Data Register or by $\overline{RES}$.

SCSR 2: *Parity Error*—Set to logic 1 when the RCVR is in the ASYN Mode, Parity Enable bit is set, and the received data has a parity error. This bit is cleared by reading the Receiver Data Register or by $\overline{RES}$.

SCSR 3: *Framing Error*—Set to a logic 1 when the received data contains a zero bit after the last data or parity bit in the stop bit slot. Cleared by reading the Receiver Data Register or by $\overline{RES}$ (ASYN Mode only).

SCSR 4: *Wake-Up*—Set to a logic 1 by writing a "1" in bit 4 of address: 0016. The Wake-Up bit is cleared by $\overline{RES}$ or when the receiver detects a string of ten consecutive 1's. When the Wake-Up bit is set SCSR0 through SCSR3 are inhibited.

SCSR 5: *End of Transmission*—Set to a logic 1 by writing a "1" in bit position 5 of address: 0016. The End of Transmission bit is cleared by $\overline{RES}$ or upon writing a new data word into the Transmitter Data Register. When the End-of-Transmission bit is true the Transmitter Register Empty bit is disabled until a Transmitter Under-Run occurs.

SCSR 6: *Transmitter Data Register Empty*—Set to a logic 1 when the contents of the Transmitter Data Register are transferred to the Transmitter Shift Register. Cleared upon writing new data into the Transmit Data Register. This bit is initialized to a logic 1 by $\overline{RES}$.

SCSR 7: *Transmitter Under-Run*—Set to a logic 1 when the last data bit is transmitted if the transmitter is in a S/R Mode or when the last stop bit is transmitted if the XMTR is in the ASYN Mode while the Transmitter Data Register Empty Bit is set. Cleared by a transfer of new data into the Transmitter Shift Register or by $\overline{RES}$.

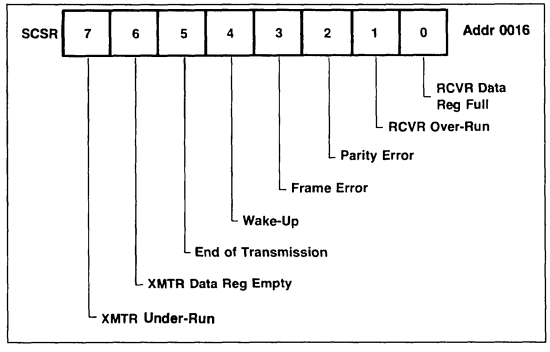


Figure 5-5. SCSR Bit Allocations

5.4 WAKE-UP FEATURE

In a multi-distributed microprocessor or microcomputer applications, a destination address is usually included at the beginning of the message. The Wake-Up Feature allows non-selected CPU's to ignore the remainder of the message until the beginning of the next message by setting the Wake-Up bit. As long as the Wake-Up flag is true, the Receiver Data Register Full Flag remains false. The Wake-Up bit is automatically cleared when the receiver detects a string of 11 consecutive 1's which indicates an idle transmit line. When the next byte is received, the Receiver Data Register Full Flag signals the CPU to wake-up and read the received data.

SECTION 6
COUNTER/TIMERS

The device contains two 16-bit counters (Counter A and Counter B) and three 16-bit latches associated with the counters. Counter A has one 16-bit latch and Counter B has two 16-bit latches. Each counter can be independently programmed to operate in one of four modes:

Counter A	Counter B
• Pulse width measurement	• Retriggerable Interval Counter
• Pulse Generation	• Asymmetrical Pulse Generation
• Interval Timer	• Interval Timer
• Event Counter	• Event Counter

Operating modes of Counter A and Counter B are controlled by the Mode Control Register. All counting begins at the initialization value and decrements. When modes are selected requiring a counter input/output line, PA4 is automatically selected for Counter A and PA5 is automatically selected for Counter B (see Table 4.2).

6.1 COUNTER A

Counter A consists of a 16-bit counter and a 16-bit latch organized as follows: Lower Counter A (LCA), Upper Counter A (UCA), Lower Latch A (LLA), and Upper Latch A (ULA). The counter contains the count of either Ø2 clock pulses or external events, depending on the counter mode selected. The contents of Counter A may be read any time by executing a read at location 0019 for the Upper Counter A and at location 001A or location 0018 for the Lower Counter A. A read at location 0018 also clears the Counter A Underflow Flag (IFR4).

The 16-bit latch contains the counter initialization value and can be loaded at any time by executing a write to the Upper Latch A at location 0019 and the Lower Latch A at location 0018. In either case, the contents of the accumulator are copied into the applicable latch register.

Counter A can be started at any time by writing to address: 001A. The contents of the accumulator will be copied into the Upper Latch A before the contents of the 16-bit latch are transferred to Counter A. Counter A is set to the latch value whenever Counter A underflows. When Counter A decrements from 0000 the next counter value will be the latch value—not FFFF—and the Counter A Underflow Flag (IFR 4) will be set to "1". This bit may be cleared by reading the Lower Counter A at location 0018, by writing to address location 001A, or by $\overline{RES}$.

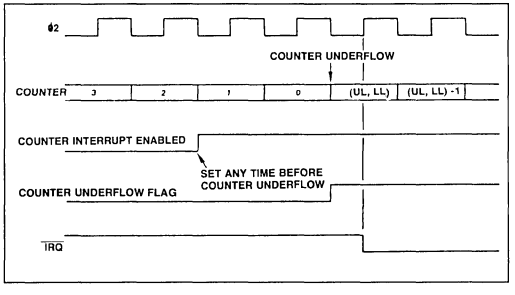


Figure 6-1. Interval Timer Timing Diagram

Counter A operates in any of four modes. These modes are selected by the Counter A Mode Control bits in the Control Register.

MCR1 (bit 1)	MCR0 (bit 0)	Mode
0	0	Interval Timer
0	1	Pulse Generation
1	0	Event Counter
1	1	Pulse Width Measurement

The Interval Timer, Pulse Generation, and Pulse Width Measurement Modes are Ø2 clock counter modes. The Event Counter Mode counts the occurrences of an external event on the CNTR line.

The Counter is set to the Interval Timer Mode (00) when a $\overline{RES}$ signal is generated.

6.1.1 Interval Timer

In the Interval Timer mode the Counter is initialized to the Latch value by either of two conditions:

1. When the Counter is decremented from 0000, the next Counter value is the Latch value (not FFFF).

2. When a write operation is performed to the Load Upper Latch and Transfer Latch to Counter address 001A, the Counter is loaded with the Latch value. Note that the contents of the Accumulator are loaded into the Upper Latch before the Latch value is transferred to the Counter.

The Counter value is decremented by one count at the 02 clock rate. The 16-bit Counter can hold from 1 to 65535 counts. The Counter Timer capacity is therefore 1μs to 65,535 ms at the 1 MHz Ø2 clock rate or 0.5 μs to 32.767 ms at the 2 MHz Ø2 clock rate. Time intervals greater than the maximum Counter value can be easily measured by counting $\overline{IRQ}$ interrupt requests in the counter $\overline{IRQ}$ interrupt routine.

When Counter A decrements from 0000, the Counter A Underflow (IFR4) is set to logic 1. If the Counter A Interrupt Enable Bit (IER4) is also set, an $\overline{IRQ}$ interrupt request will be generated. The Counter A Underflow bit in the Interrupt Flag Register can be examined in the $\overline{IRQ}$ interrupt routine to determine that the $\overline{IRQ}$ was generated by the Counter A Underflow.

While the timer is operating in the Interval Timer Mode, PA4 operates as a PA I/O bit.

A timing diagram of the Interval Timer Mode is shown in Figure 6-1.

6.1.2 Pulse Generation Mode

In the Pulse Generation mode, the CA line operates as a Counter Output. The line toggles from low to high or from high to low whenever a Counter A Underflow occurs or a write is performed to address 001A.

The normal output waveform is a symmetrical square-wave. The CA output is initialized high when entering the mode and transitions low when writing to 001A.

Asymmetric waveforms can be generated if the value of the latch is changed after each counter underflow.

A one-shot waveform can be generated by changing from Pulse Generation to Interval Timer mode after only one occurrence of the output toggle condition.

6.1.3 Event Counter Mode

In this mode the CA is used as an Event Input line, and the Counter will decrement with each rising edge detected on this line. The maximum rate at which this edge can be detected is one-half the $\phi 2$ clock rate.

The Counter can count up to 65,535 occurrences before underflowing. As in the other modes, the Counter A Underflow bit (IER4) is set to logic 1 if the underflow occurs.

Figure 6.2 is a timing diagram of the Event Counter Mode.

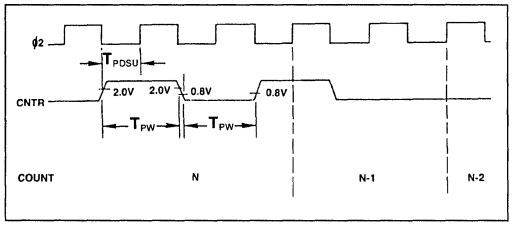


Figure 6-2. Event Counter Mode

6.1.4 Pulse Width Measurement Mode

This mode allows the accurate measurement of a low pulse duration on the CA line. The Counter decrements by one count at the $\phi 2$ clock rate as long as the CA line is held in the low state. The Counter is stopped when CA is in the high state.

The Counter A underflow flag will be set only when the count in the timer reaches zero. Upon reaching zero the timer will be loaded with the latch value and continue counting down as long as the CA pin is held low. After the counter is stopped by a high level on CA, the count will hold as long as CA remains high. Any further low levels on CA will again cause the counter to count down from its present value. The state of the CA line can be determined by testing the state of PA4.

A timing diagram for the Pulse Width Measurement Mode is shown in Figure 6.3.

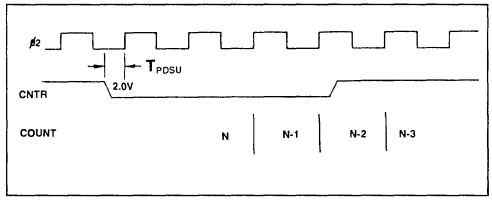


Figure 6-3. Pulse Width Measurement

6.1.5 Serial I/O Data Rate Generation

Counter A also provides clock timing for the Serial I/O which establishes the data rate for the Serial I/O port. When the Serial I/O is enabled, Counter A is forced to operate at the internal clock rate. Counter A is not required for the RCVR S/R mode. The Counter I/O (PA4) may also be required to support the Serial I/O (see Table 4-2).

Table 6-1 identifies the values to be loaded in Counter A for selecting standard data rates with a $\phi 2$ clock rate of 1 MHz and 2 MHz. Although Table 6-1 identifies only the more common data rates, any data rate from 1 to 62.5K bps can be selected by using the formula:

$$N = \frac{\phi 2}{16 \times \text{bps}} - 1$$

where

- N = decimal value to be loaded into Counter A using its hexadecimal equivalent.
- $\phi 2$ = the clock frequency (1 MHz or 2 MHz)
- bps = the desired data rate.

NOTE

In Table 6-1 you will notice that the standard data rate and the actual data rate may be slightly different. Transmitter and receiver errors of 1.5% or less are acceptable. A revised clock rate is included in Table 6-1 for those baud rates which fall outside this limit.

Table 6-1. Counter A Values for Baud Rate Selection

Standard Baud Rate	Hexadecimal Value		Actual Baud Rate At		Clock Rate Needed To Get Standard Baud Rate	
	1 MHz	2 MHz	1 MHz	2 MHz	1 MHz	2 MHz
50	04E1	09C3	50.00	50.00	1.0000	2.0000
75	0340	0682	75.03	74.99	1.0000	2.0000
110	0237	046F	110.04	110.04	1.0000	2.0000
150	01A0	0340	149.88	150.06	1.0000	2.0000
300	00CF	01A0	300.48	299.76	1.0000	2.0000
600	0067	00CF	600.96	600.96	1.0000	2.0000
1200	0033	0067	1201.92	1201.92	1.0000	2.0000
2400	0019	0033	2403.85	2403.85	1.0000	2.0000
3600	0010	0021	3676.47	3676.47	0.9792	1.9584
4800	000C	0019	4807.69	4807.69	1.0000	2.0000
7200	0008	0010	6944.44	7352.94	1.0368	1.9584
9600	0006	000C	8928.57	9615.38	1.0752	2.0000

6.2 COUNTER B

Counter B consists of a 16-bit counter and two 16-bit latches organized as follows: Lower Counter B (LCB), Upper Counter B (UCB), Lower Latch B (LLB), Upper Latch B (ULB), Lower Latch C (LLC), and Upper Latch C (ULC). Latch C is used only in the asymmetrical pulse generation mode. The counter contains the count of either Ø2 clock pulses or external events depending on the counter mode selected. The contents of Counter B may be read any time by executing a Read at location 001D for the Upper Counter B and at location 001E or 001C for the Lower Counter B. A Read at location 001C also clears the Counter B Underflow Flag.

Latch B contains the counter initialization value and can be loaded at any time by executing a Write to the Upper Latch B at location 001D and the Lower Latch B at location 001C. In each case, the contents of the accumulator are copied into the applicable latch register.

Counter B can be initialized at any time by writing to address: 001E. The contents of the accumulator is copied into the Upper Latch B before the value in the 16-bit Latch B is transferred to Counter B. Counter B will also be set to the latch value and the Counter B Underflow Flag bit (IFR5) will be set to a "1" whenever Counter B underflows by decrementing from 0000.

IFR 5 may be cleared by reading the Lower Counter B at location 001C, by writing to address location 001E, or by $\overline{RES}$.

Counter B operates in the same manner as Counter A in the Interval Timer and Event Counter modes. The Pulse Width Measurement Mode is replaced by the Retriggerable Interval Timer mode and the Pulse Generation mode is replaced by the Asymmetrical Pulse Generation Mode. Mode Control Register bits MCR2 and MCR3 select the four Counter B modes in a similar manner and coding as MCR0 and MCR1 select the modes of Counter A.

6.2.1 Retriggerable Interval Timer Mode

When operating in the Retriggerable Interval Timer mode, Counter B is initialized to the latch value by writing to address 001E, by a Counter B underflow, or whenever a positive edge occurs on the CB pin (PA5). The Counter B interrupt flag will be set if the counter underflows before a positive edge occurs on the CB line. Figure 6-4 illustrates the operation.

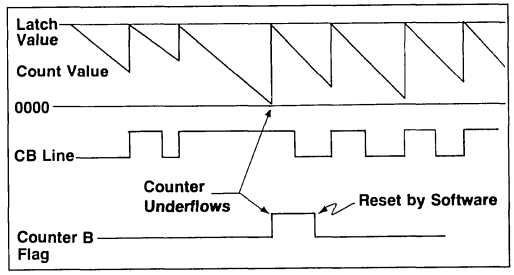


Figure 6-4. Counter B. Retriggerable Interval Timer Mode

6.2.2 Asymmetrical Pulse Generation Mode

Counter B has a special Asymmetrical Pulse Generation Mode whereby a pulse train with programmable pulse width and period can be generated without the processor intervention once the latch values are initialized.

In this mode, the 16-bit Latch B is initialized with a value which corresponds to the duration between pulses (referred to as D in the following descriptions). The 16-bit Latch C is initialized with a value corresponding to the desired pulse width (referred to as P in the following descriptions). The initialization sequence for Latch B and C and the starting of a counting sequence are as follows:

1. The lower 8 bits of P are loaded into LLB by writing to address 001C; the upper 8 bits of P are loaded into ULB and the full 16 bits are transferred to Latch C by writing to address location 001D. At this point both Latch B and Latch C contain the value of P.

2. The lower 8 bits of D are loaded into LLB by writing to address 001C; the upper 8 bits of D are loaded into ULB by writing to address location 001E. Writing to address location 001E also causes the contents of the 16-bit Latch B to be downloaded into the Counter B and the CB output to go low as shown in Figure 6-5.

3. When Counter B underflow occurs the contents of the Latch C are loaded into the Counter B and the CB output toggles to a high level, staying high until another underflow occurs. Latch B is then down-loaded and the CB output toggles to a low level repeating the whole process.

SECTION 7
POWER ON/INITIALIZATION CONSIDERATIONS

7.1 POWER ON TIMING

After application of V_{CC} and V_{RR} power to the device, $\overline{RES}$ must be held low for at least eight $\phi 2$ clock cycles after V_{CC} reaches operating range and the internal oscillator has stabilized. This stabilization time is dependent upon the input V_{CC} voltage and performance of the internal oscillator. The clock can be monitored at $\phi 2$ (pin 3). Figure 7-1 illustrates the power turn-on waveforms. Clock stabilization time is typically 20 ms.

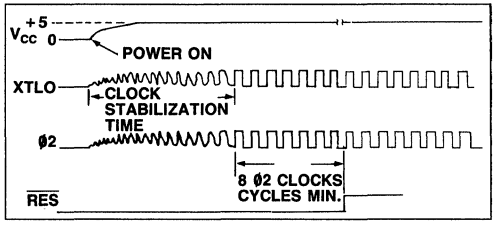


Figure 7-1. Power Turn-On Timing Detail

7.2 POWER-ON RESET

When $\overline{RES}$ goes from low to high, the device sets the Interrupt Mask Bit—bit 2 of the Processor Status Register—and initiates a reset vector fetch at address FFFC and FFFD (or optionally 7FFE and 7FFF) to begin user program execution. All of the I/O ports (PA, PB, PC, PD) will be forced to the high (logic 1) state. All bits of the Control Register will be cleared to logic 0 causing the Interval Timers counter mode (mode 00) to be selected and all interrupt enabled bits to be reset.

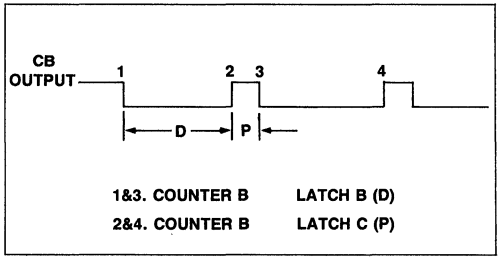


Figure 6-5. Counter B Pulse Generation

7.3 RESET ($\overline{RES}$) CONDITIONING

When $\overline{RES}$ is driven from low to high the device is put in a reset state causing the registers and I/O ports to be configured as shown in Table 7-1.

Table 7-1. $\overline{RES}$ Initialization of I/O Ports and Registers

Bit No.	7	6	5	4	3	2	1	0
REGISTERS								
Processor Status	—	—	—	—	—	1	—	—
Mode Control (MCR)	0	0	0	0	0	0	0	0
Int. Enable (IER)	0	0	0	0	0	0	0	0
Int. Flag (IFR)	0	0	0	0	0	0	0	0
Ser. Com. Control (SCCR)	0	0	0	0	0	0	0	0
Ser. Com. Status (SCSR)	0	1	0	0	0	0	0	0
PORTS								
PA Latch	1	1	1	1	1	1	1	1
PB Latch	1	1	1	1	1	1	1	1
PC Latch	1	1	1	1	1	1	1	1
PD Latch	1	1	1	1	1	1	1	1

All RAM and other CPU registers will initialize in a random, non-repeatable data pattern.

7.4 INITIALIZATION

Any initialization process for the device should include a $\overline{RES}$, as indicated in the preceeding paragraphs. After stabilization of the internal clock (if a power on situation) an initialization subroutine should be executed to perform (as a minimum) the following functions:

1. The Stack Pointer should be set
2. Clear or Set Decimal Mode
3. Set or Clear Carry Flag
4. Set up Mode Controls as required
5. Clear Interrupts

A typical initialization subroutine could be as follows:

```
LDX     Load stack pointer starting address into
        X Register
TXS     Transfer X Register value to Stack Pointer
CLD     Clear Decimal Mode
SEC     Set Carry Flag
. . . .
. . . .  Set-up Mode Control and
. . . .  special function registers
. . . .  and clear RAM as required
CLI     Clear Interrupts
```

APPENDIX A
ENHANCED R6502 INSTRUCTION SET

This appendix contains a summary of the Enhanced R6502 instruction set. For detailed information, consult the R6502 Microcomputer System Programming Manual, Document 29650 N30. The four instructions notated with a * are added instructions to enhance the standard 6502 instruction set.

A.1 INSTRUCTION SET IN ALPHABETIC SEQUENCE

Mnemonic	Instruction	Mnemonic	Instruction
ADC	Add Memory to Accumulator with Carry	LDA	Load Accumulator with Memory
AND	"AND" Memory with Accumulator	LDX	Load Index X with Memory
ASL	Shift Left One Bit (Memory or Accumulator)	LDY	Load Index Y with Memory
		LSR	Shift One Bit Right (Memory or Accumulator)
*BBR	Branch on Bit Reset Relative		
*BBS	Branch on Bit Set Relative		
BCC	Branch on Carry Clear	NOP	No Operation
BCS	Branch on Carry Set		
BEQ	Branch on Result Zero	ORA	"OR" Memory with Accumulator
BIT	Test Bits in Memory with Accumulator		
BMI	Branch on Result Minus	PHA	Push Accumulator on Stack
BNE	Branch on Result not Zero	PHP	Push Processor Status on Stack
BPL	Branch on Result Plus	PLA	Pull Accumulator from Stack
BRK	Force Break	PLP	Pull Processor Status from Stack
BVC	Branch on Overflow Clear		
BVS	Branch on Overflow Set	*RMB	Reset Memory Bit
		ROL	Rotate One Bit Left (Memory or Accumulator)
CLC	Clear Carry Flag		
CLD	Clear Decimal Mode	ROR	Rotate One Bit Right (Memory or Accumulator)
CLI	Clear Interrupt Disable Bit		
CLV	Clear Overflow Flag	RTI	Return from Interrupt
CMP	Compare Memory and Accumulator	RTS	Return from Subroutine
CPX	Compare Memory and Index X		
CPY	Compare Memory and Index Y	SBC	Subtract Memory from Accumulator with Borrow
DEC	Decrement Memory by One	SEC	Set Carry Flag
DEX	Decrement Index X by One	SED	Set Decimal Mode
DEY	Decrement Index Y by One	SEI	Set Interrupt Disable Status
		*SMB	Set Memory Bit
EOR	"Exclusive-Or" Memory with Accumulator	STA	Store Accumulator in Memory
		STX	Store Index X in Memory
		STY	Store Index Y in Memory
INC	Increment Memory by One		
INX	Increment Index X by One	TAX	Transfer Accumulator to Index X
INY	Increment Index X by One	TAY	Transfer Accumulator to Index Y
		TSX	Transfer Stack Pointer to Index X
JMP	Jump to New Location	TXA	Transfer Index X to Accumulator
JSR	Jump to New Location Saving Return Address	TXS	Transfer Index X to Stack Register
		TYA	Transfer Index Y to Accumulator

A.2 R6511Q AND R6500/13 INSTRUCTION SET SUMMARY TABLE

ADDRESSING MODES

MNEMONIC	OPERATION	IMMEDIATE			ABSOLUTE			ZERO PAGE			ACCUM.			IMPLIED			(IND, X)			(IND), Y			Z. PAGE, X			ABS, X			ABS, Y			RELATIVE			INDIRECT			Z. PAGE, Y			BIT ADDRESSING (OP BY BIT #)								PROCESSOR STATUS CODES 7 6 5 4 3 2 1 0
		OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	0	1	2	3	4	5	6	7	N V • B D I Z C
ADC	A + M + C→A (4)(1)	69	2	2	6D	4	3	65	3	2							61	6	2	71	5	2	75	4	2	7D	4	3	79	4	3																		N V • • • • Z C
AND	A M→A (1)	29	2	2	2D	4	3	25	3	2							21	6	2	31	5	2	35	4	2	3D	4	3	39	4	3																		N • • • • • Z •
ASL	C← [7 0] ←0				0E	6	3	06	5	2	0A	2	1										16	6	2	1E	7	3																					N • • • • • Z C
BBR[#(0-7)]	Branch on M_6 = 0 (5)(2)																																								0F	1F	2F	3F	4F	5F	6F	7F	• • • • • • • •
BBS[#(0-7)]	Branch on M_6 = 1 (5)(2)																																								8F	9F	AF	BF	CF	DF	EF	FF	• • • • • • • •
BCC	Branch on C = 0 (2)																															90	2	2															• • • • • • • •
BCS	Branch on C = 1 (2)																															B0	2	2															• • • • • • • •
BEQ	Branch on Z = 1 (2)																															F0	2	2															• • • • • • • •
BIT	A∧M				2C	4	3	24	3	2																																							M_7 M_6 • • • • Z •
BMI	Branch on N = 1 (2)																															30	2	2															• • • • • • • •
BNE	Branch on Z = 0 (2)																															D0	2	2															• • • • • • • •
BPL	Branch on N = 0 (2)																															10	2	2															• • • • • • • •
BRK	Break (See Fig 1)													00	7	1																																	• • • 1 • 1 • •
BVC	Branch on V = 0 (2)																															50	2	2															• • • • • • • •
BVS	Branch on V = 1 (2)																															70	2	2															• • • • • • • •
CLC	0→C													18	2	1																																	• • • • • • • 0
CLD	0→D													D8	2	1																																	• • • • 0 • • •
CLI	0→I													58	2	1																																	• • • • • 0 • •
CLV	0→V													B8	2	1																																	• 0 • • • • • •
CMP	A M (1)	C9	2	2	CD	4	3	C5	3	2							C1	6	2	D1	5	2	D5	4	2	DD	4	3	D9	4	3																		N • • • • • Z C
CPX	X M	E0	2	2	EC	4	3	E4	3	2																																							N • • • • • Z C
CPY	Y M	C0	2	2	CC	4	3	C4	3	2																																							N • • • • • Z C
DEC	M 1→M				CE	6	3	C6	5	2													D6	6	2	DE	7	3																					N • • • • • Z •
DEX	X 1→X													CA	2	1																																	N • • • • • Z •
DEY	Y 1→Y													88	2	1																																	N • • • • • Z •
EOR	A⊻M→A (1)	49	2	2	4D	4	3	45	3	2							41	6	2	51	5	2	55	4	2	5D	4	3	59	4	3																		N • • • • • Z •
INC	M + 1→M				EE	6	3	E6															F6	6	2	FE	7	3																					N • • • • • Z •
INX	X + 1→X													EB	2	1																																	N • • • • • Z •
INY	Y + 1→Y													C8	2	1																																	N • • • • • Z •
JMP	Jump to New Loc				4C	3	3																												6C	5	3												• • • • • • • •
JSR	Jump Sub (See Fig 2)				20	6	3																																										• • • • • • • •
LDA	M→A (1)	A9	2	2	AD	4	3	A5	3	2							A1	6	2	B1	5	2	B5	4	2	BD	4	3	B9	4	3																		N • • • • • Z •
LDX	M→X (1)	A2	2	2	AE	4	3	A6	3	2																			BE	4	3							B6	4	2									N • • • • • Z •
LDY	M→Y (1)	A0	2	2	AC	4	3	A4	3	2													B4	4	2	BC	4	3																					N • • • • • Z •
LSR	0→ [7 0] →C				4E	6	3	46	5	2	4A	2	1										56	6	2	5E	7	3																					0 • • • • • Z C
NOP	No Operation													EA	2	1																																	• • • • • • • •
ORA	A∨M→A (1)	09	2	2	0D	4	3	05	3	2							01	6	2	11	5	2	15	4	2	1D	4	3	19	4	3																		N • • • • • Z •
PHA	A→Ms S 1→S													48	3	1																																	• • • • • • • •
PHP	P→Ms S 1→S													08	3	1																																	• • • • • • • •
PLA	S + 1→S Ms→A													68	4	1																																	N • • • • • Z •
PLP	S + 1→S Ms→P													28	4	1																																	(Restored)
RMB[#(0-7)]	0→M_b (5)																																								07	17	27	37	47	57	67	77	• • • • • • • •
ROL	[7 0]←[C]				2E	6	3	26	5	2	2A	2	1										36	6	2	3E	7	3																					N • • • • • Z C
ROR	[C]→[7 0]				6E	6	3	66	5	2	6A	2	1										76	6	2	7E	7	3																					N • • • • • Z C
RTI	Rtrn Int (See Fig 1)													40	6	1																																	(Restored)
RTS	Rtrn Sub (See Fig 2)													60	6	1																																	• • • • • • • •
SBC	A - M - C→A (1)	E9	2	2	ED	4	3	E5	3	2							E1	6	2	F1	5	2	F5	4	2	FD	4	3	F9	4	3																		N V • • • • Z (3)
SEC	1→C													38	2	1																																	• • • • • • • 1
SED	1→D													F8	2	1																																	• • • • 1 • • •
SEI	1→T													78	2	1																																	• • • • • 1 • •
SMB[#(0-7)]	1→M_b (5)																																								87	97	A7	B7	C7	D7	E7	F7	• • • • • • • •
STA	A→M				8D	4	3	85	3	2							81	6	2	91	6	2	95	4	2	9D	5	3	[illegible]	5	3																		• • • • • • • •
STX	X→M				8E	4	3	86	3	2																												96	4	2									• • • • • • • •
STY	Y→M				8C	4	3	84	3	2													94	4	2																								• • • • • • • •
TAX	A→X													AA	2	1																																	N • • • • • Z •
TAY	A→Y													A8	2	1																																	N • • • • • Z •
TSX	S→X													BA	2	1																																	N • • • • • Z •
TXA	X→A													8A	2	1																																	N • • • • • Z •
TXS	X→S													9A	2	1																																	• • • • • • • •
TYA	Y→A													98	2	1																																	N • • • • • Z •

NOTES

1. Add 1 to N if page boundary is crossed
2. Add 1 to N if branch occurs to same page
   Add 2 to N if branch occurs to different page
3. Carry not = Borrow
4. If in decimal mode Z flag is invalid
   accumulator must be checked on zero result.
5. Effects 8-bit data field of the specified zero page address.

LEGEND

- X = Index X
- Y = Index Y
- A = Accumulator
- M = Memory per effective address
- M_s = Memory per stack pointer
- M_b = Selecter zero page memory bit
- M_7 = Memory Bit 7
- M_6 = Memory Bit 6
- • = Add
- − = Subtract
- ∧ = And
- ∨ = Or
- ⊻ = Exclusive Or
- n = Number of cycles
- # = Number of Bytes

A.3 INSTRUCTION CODE MATRIX

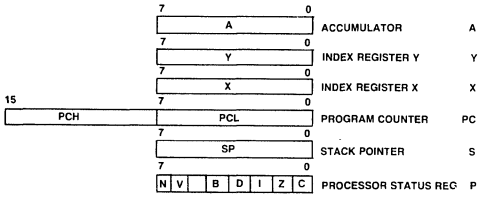
MSD \ LSD	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	MSD
0	BRK Implied 1 7	ORA (IND, X) 2 6				ORA ZP 2 3	ASL ZP 2 5	RMB0 ZP 2 5	PHP Implied 1 3	ORA IMM 2 2	ASL Accum 1 2			ORA ABS 3 4	ASL ABS 3 6	BBR0 ZP 3 5**	0
1	BPL Relative 2 2**	ORA (IND), Y 2 5*				ORA ZP, X 2 4	ASL ZP, X 2 6	RMB1 ZP 2 5	CLC Implied 1 2	ORA ABS, Y 3 4*				ORA ABS, X 3 4*	ASL ABS, X 3 7	BBR1 ZP 3 5**	1
2	JSR Absolute 3 6	AND (IND, X) 2 6			BIT ZP 2 3	AND ZP 2 3	ROL ZP 2 5	RMB2 ZP 2 5	PLP Implied 1 4	AND IMM 2 2	ROL Accum 1 2		BIT ABS 3 4	AND ABS 3 4	ROL ABS 3 6	BBR2 ZP 3 5**	2
3	BMI Relative 2 2**	AND (IND, Y) 2 5*				AND ZP, X 2 4	ROL ZP, X 2 6	RMB3 ZP 2 5	SEC Implied 1 2	AND ABS, Y 3 4*				AND ABS, X 3 4*	ROL ABS, X 3 7	BBR3 ZP 3 5**	3
4	RTI Implied 1 6	EOR (IND, X) 2 6				EOR ZP 2 3	LSR ZP 2 5	RMB4 ZP 2 5	PHA Implied 1 3	EOR IMM 2 2	LSR Accum 1 2		JMP ABS 3 3	EOR ABS 3 4	LSR ABS 3 6	BBR4 ZP 3 5**	4
5	BVC Relative 2 2**	EOR (IND), Y 2 5*				EOR ZP, X 2 4	LSR ZP, X 2 6	RMB5 ZP 2 5	CLI Implied 1 2	EOR ABS, Y 3 4*				EOR ABS, X 3 4*	LSR ABS, X 3 7	BBR5 ZP 3 5**	5
6	RTS Implied 1 6	ADC (IND, X) 2 6				ADC ZP 2 3	ROR ZP 2 5	RMB6 ZP 2 5	PLA Implied 1 4	ADC IMM 2 2	ROR Accum 1 2		JMP Indirect 3 5	ADC ABS 3 4	ROR ABS 3 6	BBR6 ZP 3 5**	6
7	BVS Relative 2 2**	ADC (IND, Y) 2 5*				ADC ZP, X 2 4	ROR ZP, X 2 6	RMB7 ZP 2 5	SEI Implied 1 2	ADC ABS, Y 3 4*				ADC ABS, X 3 4*	ROR ABS, X 3 7	BBR7 ZP 3 5**	7
8		STA (IND, X) 2 6			STY ZP 2 3	STA ZP 2 3	STX ZP 2 3	SMB0 ZP 2 5	DEY Implied 1 2		TXA Implied 1 2		STY ABS 3 4	STA ABS 3 4	STX ABS 3 4	BBS0 ZP 3 5**	8
9	BCC Relative 2 2**	STA (IND, Y) 2 6			STY ZP, X 2 4	STA ZP, X 2 4	STX ZP, Y 2 4	SMB1 ZP 2 5	TYA Implied 1 2	STA ABS, Y 3 5	TXS Implied 1 2			STA ABS, X 3 5		BBS1 ZP 3 5**	9
A	LDY IMM 2 2	LDA (IND, X) 2 6	LDX IMM 2 2		LDY ZP 2 3	LDA ZP 2 3	LDX ZP 2 3	SMB2 ZP 2 5	TAY Implied 1 2	LDA IMM 2 2	TAX Implied 1 2		LDY ABS 3 4	LDA ABS 3 4	LDX ABS 3 4	BBS2 ZP 3 5**	A
B	BCS Relative 2 2**	LDA (IND), Y 2 5*			LDY ZP, X 2 4	LDA ZP, X 2 4	LDX ZP, Y 2 4	SMB3 ZP 2 5	CLV Implied 1 2	LDA ABS, Y 3 4*	TSX Implied 1 2		LDY ABS, X 3 4*	LDA ABS, X 3 4*	LDX ABS, Y 3 4*	BBS3 ZP 3 5**	B
C	CPY IMM 2 2	CMP (IND, X) 2 6			CPY ZP 2 3	CMP ZP 2 3	DEC ZP 2 5	SMB4 ZP 2 5	INY Implied 1 2	CMP IMM 2 2	DEX Implied 1 2		CPY ABS 3 4	CMP ABS 3 4	DEC ABS 3 6	BBS4 ZP 3 5**	C
D	BNE Relative 2 2**	CMP (IND), Y 2 5*				CMP ZP, X 2 4	DEC ZP, X 2 6	SMB5 ZP 2 5	CLD Implied 1 2	CMP ABS, Y 3 4*				CMP ABS, X 3 4*	DEC ABS, X 3 7	BBS5 ZP 3 5**	D
E	CPX IMM 2 2	SBC (IND, X) 2 6			CPX ZP 2 3	SBC ZP 2 3	INC ZP 2 5	SMB6 ZP 2 5	INX Implied 1 2	SBC IMM 2 2	NOP Implied 1 2		CPX ABS 3 4	SBC ABS 3 4	INC ABS 3 6	BBS6 ZP 3 5**	E
F	BEQ Relative 2 2**	SBC (IND), Y 2 5*				SBC ZP, X 2 4	INC ZP, X 2 6	SMB7 ZP 2 5	SED Implied 1 2	SBC ABS, Y 3 4*				SBC ABS, X 3 4*	INC ABS, X 3 7	BBS7 ZP 3 5**	F
	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	

0

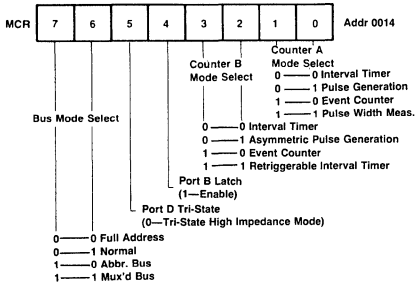
BRK	—OP Code
0 Implied	—Addressing Mode
1 7	—Instruction Bytes; Machine Cycles

*Add 1 to N if page boundary is crossed.
**Add 1 to N if branch occurs to same page;
add 2 to N if branch occurs to different page.

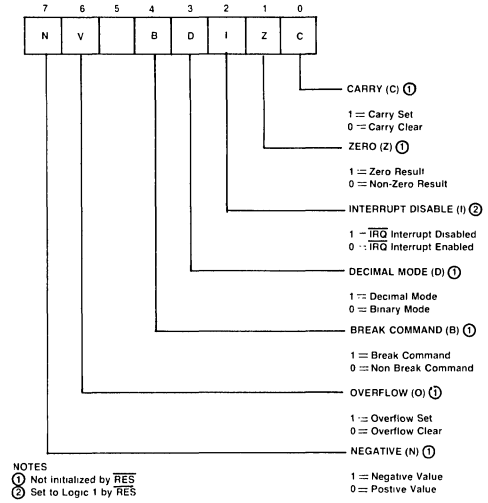
APPENDIX B
KEY REGISTER SUMMARY



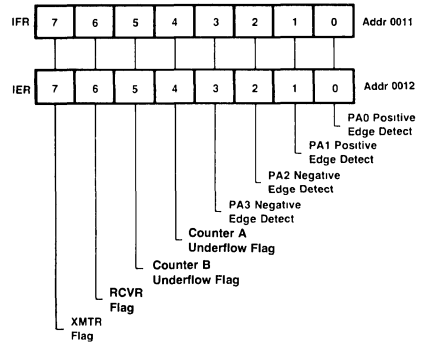
CPU Registers



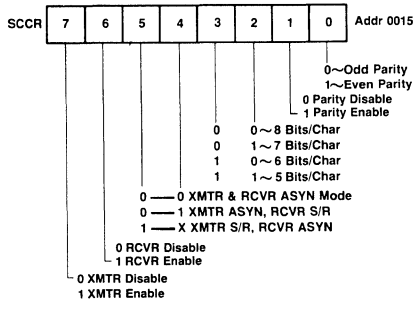
Mode Control Register



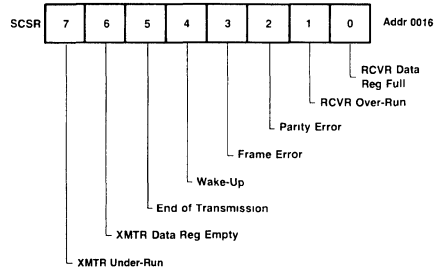
Processor Status Register



Interrupt Enable and Flag Registers



Serial Communications Control Register



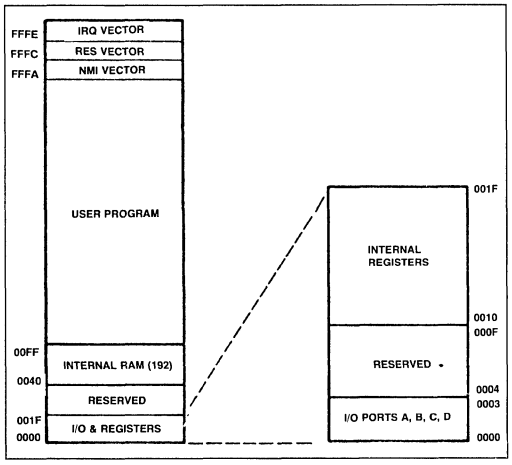
Serial Communications Status Register

APPENDIX C
ADDRESS ASSIGNMENTS/MEMORY MAPS/PIN FUNCTIONS

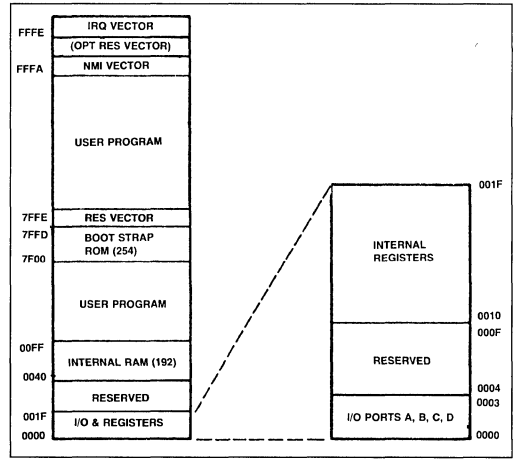
C.1 I/O AND INTERNAL REGISTER ADDRESSES

ADDRESS (HEX)	READ	WRITE
001F	— —	— —
1E	Lower Counter B	Upper Latch B, Cntr B←Latch B, CLR Flag
1D	Upper Counter B	Upper Latch B, Latch C←Latch B
1C	Lower Counter B, CLR Flag	Lower Latch B.
1B	— —	— —
1A	Lower Counter A	Upper Latch A, Cntr A←Latch A, CLR Flag
19	Upper Counter A	Upper Latch A
18	Lower Counter A, CLR Flag	Lower Latch A
17	Serial Receiver Data Register	Serial Transmitter Data Register
16	Serial Comm. Status Register	Serial Comm. Status Reg. Bits 4 & 5 only
15	Serial Comm. Control Register	Serial Comm. Control Register
14	Mode Control Register	Mode Control Register
13	— —	— —
12	Interrupt Enable Register	Interrupt Enable Register
11	Interrupt Flag Register	— —
0010	Read FF	Clear Int Flag (Bits 0-3 only, Write 0's only)
0F	**RESERVED**	
0E		
0D	These addresses are reserved and are used by the CPU during Read and Write operation over the external Data Bus (D0-D7).	
0C		
0B		
0A		
09		
08		
07		
06		
05		
04		
03	Port D	Port D
02	Port C	Port C
01	Port B	Port B
0000	Port A	Port A

C.2 FULL ADDRESS MODE MEMORY MAP R6511Q OR R6500/13



C.3 FULL ADDRESS MODE MEMORY MAP R6500/13 ONLY



C.4 MULTIPLE FUNCTION PIN ASSIGNMENTS—PORT C AND PORT D

PIN NUMBER	FULL ADDRESS MODE	I/O PORT FUNCTION	ABBREVIATED PORT FUNCTION	MULTIPLEXED PORT FUNCTION
54	PC0	PC0	A0	A0
55	PC1	PC1	A1	A1
56	PC2	PC2	A2	A2
57	PC3	PC3	A3	A3
58	PC4	PC4	A12	A12
59	PC5	PC5	R/W	R/W
60	A13	PC6	A13	A13
61	A14	PC7	EMS	EMS
62	PD0	PD0	D0	A4/D0
63	PD1	PD1	D1	A5/D1
64	PD2	PD2	D2	A6/D2
1	PD3	PD3	D3	A7/D3
2	PD4	PD4	D4	A8/D4
3	PD5	PD5	D5	A9/D5
4	PD6	PD6	D6	A10/D6
5	PD7	PD7	D7	A11/D7

APPENDIX D
ELECTRICAL SPECIFICATIONS

MAXIMUM RATINGS*

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC} & V_{RR}	−0.3 to +7.0	Vdc
Input Voltage	V_{IN}	−0.3 to +7.0	Vdc
Operating Temperature Commercial Industrial	T_A	T_L to T_H 0 to +70 −40 to +85	°C
Storage Temperature	T_{STG}	−55 to +150	°C

***NOTE:** Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the other sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

3

DC CHARACTERISTICS

(V_{CC} = 5.0V ±5%, V_{RR} = V_{CC}; V_{SS} = 0V; T_A = 0° to 70°, unless otherwise specified)

Parameter	Symbol	Min	Typ[1]	Max	Unit	Test Conditions
RAM Standby Voltage (Retention Mode)	V_{RR}	3.0		V_{CC}	V	
RAM Standby Current (Retention Mode) Commercial Industrial	I_{RR}	 — —	 4 5.2	 — —	mA	T_A = 25°C
Input High Voltage All Except XTLI and ∅2 in Slave Option XTLI and ∅2 in Slave Option	V_{IH}	 +2.0 +4.0	 — —	 V_{CC} V_{CC}	V	
Input Low Voltage	V_{IL}	−0.3	—	+0.8	V	
Input Leakage Current $\overline{RES}$, $\overline{NMI}$	I_{IN}	—	—	±10.0	μA	V_{IN} = 0 to 5.0V
Input Low Current PA, PB, PC, PD	I_{IL}	—	−1.0	−1.6	mA	V_{IL} = 0.4V
Output High Voltage (Except XTLO)	V_{OH}	+2.4	—	V_{CC}	V	I_{LOAD} = −100 μA
Output Low Voltage	V_{OL}	—	—	+0.4	V	I_{LOAD} = 1.6 mA
I/O Port Pull-Up Resistance PA0–PA7, PB0–PB7, PC0–PC7	R_L	3.0	6.0	11.5	Kohm	
Output Leakage Current (Three-State Off)	I_{OUT}	—	—	±10	μA	
Input Capacitance XTLI, XTLO All Others	C_{IN}	 — —	 — —	 50 10	pF	T_A = 25°C V_{IN} = 0V f = 1.0 MHz
Output Capacitance (Three-State Off)	C_{OUT}	—	—	10	pF	T_A = 25°C V_{IN} = 0V f = 1.0 MHz
Power Dissipation (Outputs High) Commercial Industrial	P_D	— — —	 750 —	 1100 1200	mW	T_A = 0°C

Notes:
1. Typical values measured at T_A = 25°C and V_{CC} = 5.0V.
2. Negative sign indicates outward current flow, positive indicates inward flow.

APPENDIX E
TIMING REQUIREMENTS AND CHARACTERISTICS

E.1 GENERAL NOTES

1. V_{CC} = 5V ±5%, 0°C ≤ TA ≤ 70°C

2. A valid $V_{CC}/\overline{RES}$ sequence is required before proper operation is achieved.

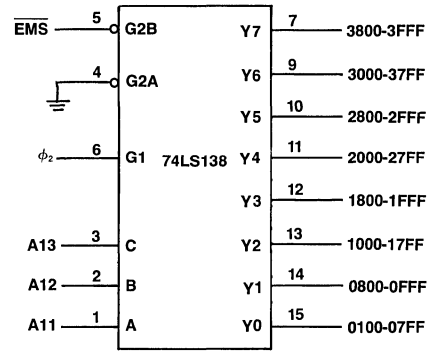
3. All timing reference levels are 0.8V and 2.0V, unless otherwise specified.

4. All time units are nanoseconds, unless otherwise specified.

5. All capacitive loading is 130pf maximum, except as noted below:

PA, PB	—	50pf maximum
PC (I/O Modes Only)	—	50pf maximum
PC (ABB and Mux Mode)	—	130pf maximum
PC6, PC7 (Full Address Mode)	—	130pf maximum

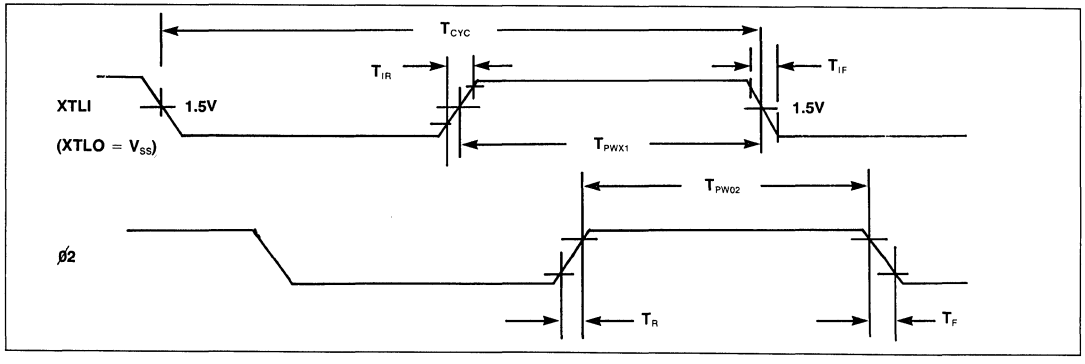
6. Example of External Chip Select (Multiplexed Bus)



Note that *both* $\overline{EMS}$ and Phase 2 (ϕ_2) must be used to correctly enable the chip selects in the multiplexed or abbreviated bus modes.

E.2 CLOCK TIMING

SYMBOL	PARAMETER	1 MHz		2 MHz	
		MIN	MAX	MIN	MAX
T_{CYC}	Cycle Time	1000	10 μs	500	10 μs
T_{PWX1}	XTLI Input Clock Pulse Width XTLO = VSS	500 ± 25	—	250 ± 10	—
T_{PW02}	Output Clock Pulse Width at Minimum T_{CYC}	T_{PWX1}	T_{PWX1} ± 25	T_{PWX1}	T_{PWX1} ± 20
T_R, T_F	Output Clock Rise, Fall Time	—	25	—	15
T_{IR}, T_{IF}	Input Clock Rise, Fall Time	—	10	—	10

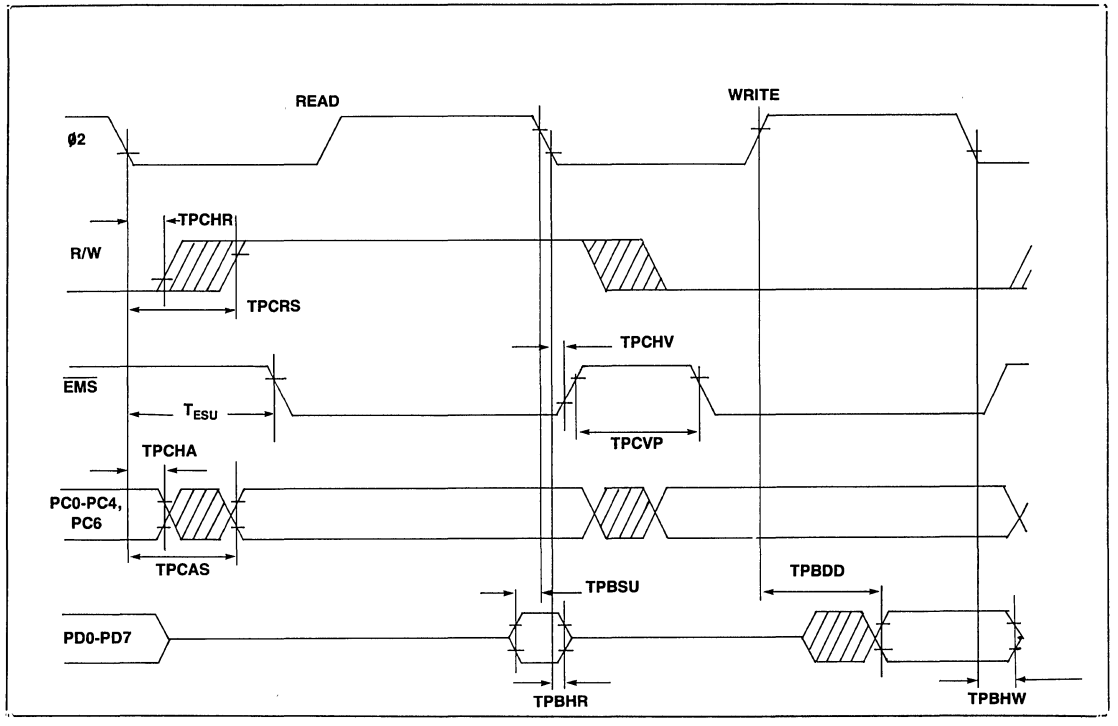


E.3 ABBREVIATED MODE TIMING—PC AND PD

(MCR 5 = 1, MCR 6 = 0, MCR 7 = 1)

SYMBOL	PARAMETER	1 MHz		2 MHz	
		MIN	MAX	MIN	MAX
T_{PCRS}	(PC5) R/W Setup Time	—	225	—	140
T_{PCAS}	(PC0-PC4, PC6) Address Setup Time	—	225	—	140
T_{PBSU}	(PD) Data Setup Time	50	—	35	—
T_{PBHR}	(PD) Data Read Hold Time	10	—	10	—
T_{PBHW}	(PD) Data Write Hold Time	30	—	30	—
T_{PBDD}	(PD) Data Output Delay	—	175	—	150
T_{PCHA}	(PC0-PC4, PC6) Address Hold Time	30	—	30	—
T_{PCHR}	(PC5) R/W Hold Time	30	—	30	—
T_{PCHV}	(PC7) $\overline{EMS}$ Hold Time	10	—	10	—
T_{PCVP}	(PC7) $\overline{EMS}$ Stabilization Time	30	—	30	—
T_{ESU}	$\overline{EMS}$ Setup Time	—	350	—	210

E.3.1 Abbreviated Mode Timing Diagram



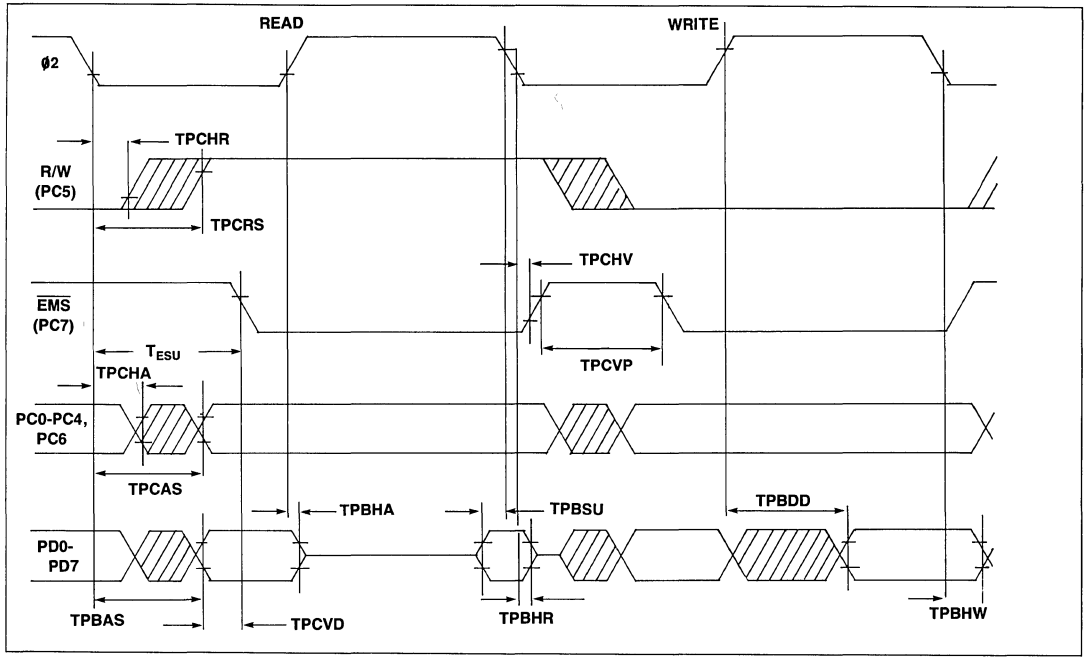
E.4 MULTIPLEXED MODE TIMING—PC AND PD

(MCR 5 = 1, MCR 6 = 1, MCR 7 = 1)

SYMBOL	PARAMETER	1 MHz		2 MHz	
		MIN	MAX	MIN	MAX
T_{PCRS}	(PC5) R/W Setup Time	—	225	—	140
T_{PCAS}	(PC0-PC4, PC6) Address Setup Time	—	225	—	140
T_{PBAS}	(PD) Address Setup Time	—	225	—	140
T_{PBSU}	(PD) Data Setup Time	50	—	35	—
T_{PBHR}	(PD) Data Read Hold Time	10	—	10	—
T_{PBHW}	(PD) Data Write Hold Time	30	—	30	—
T_{PBDD}	(PD) Data Output Delay	—	175	—	150
T_{PCHA}	(PC0-PC4, PC6) Address Hold Time	30	—	30	—
T_{PBHA}	(PD) Address Hold Time	10	100	10	80
T_{PCHR}	(PC5) R/W Hold Time	30	—	30	—
T_{PCHV}	(PC7) $\overline{EMS}$ Hold Time	10	—	10	—
T_{PCVD}(1)	(PC7) Address to $\overline{EMS}$ Delay Time	30		30	
T_{PCVP}	(PC7) $\overline{EMS}$ Stabilization Time	30	—	30	—
T_{ESU}	$\overline{EMS}$ Setup Time	—	350	—	210

NOTE 1: Values assume PC0-PC4, PC6 and PC7 have the same capacitive load.

E.4.1 Multiplex Mode Timing Diagram

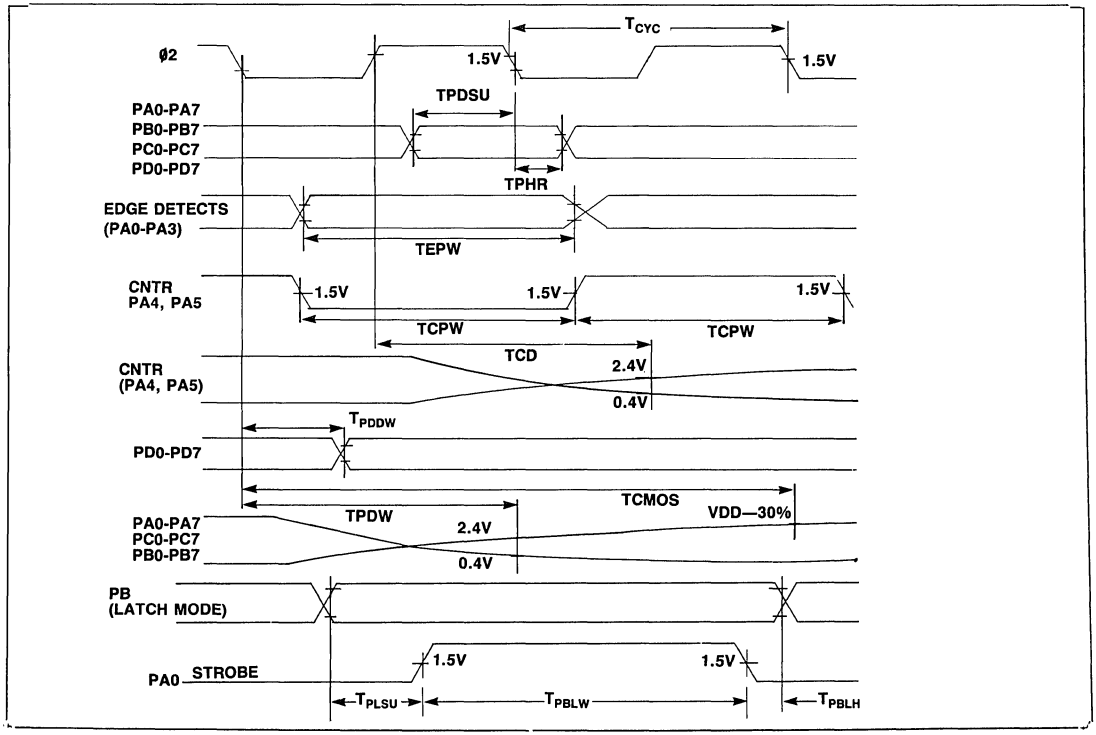


E.5 I/O, EDGE DETECT, COUNTERS, AND SERIAL I/O TIMING

SYMBOL	PARAMETER	1 MHz		2 MHz	
		MIN	MAX	MIN	MAX
	Internal Write to Peripheral Data Valid				
T_{PDW}(1)	PA, PB, PC TTL	—	500	—	500
T_{CMOS}(1)	PA, PB, PC CMOS	—	1000	—	1000
T_{PDDW}	PD	—	175	—	150
	Peripheral Data Setup Time				
T_{PDSU}	PA, PB, PC	200	—	200	—
T_{PDSU}	PD	50	—	50	—
	Peripheral Data Hold Time				
T_{PHR}	PA, PB, PC	75	—	75	—
T_{PHR}	PD	10	—	10	—
T_{EPW}	PA0–PA3 Edge Detect Pulse Width	T_{CYC}	—	T_{CYC}	—
	Counters A and B				
T_{CPW}	PA4, PA5 Input Pulse Width	T_{CYC}	—	T_{CYC}	—
T_{CD}(1)	PA4, PA5 Output Delay	—	500	—	500
	Port B Latch Mode				
T_{PBLW}	PA0 Strobe Pulse Width	T_{CYC}	—	T_{CYC}	—
T_{PLSU}	PB Data Setup Time	175	—	150	—
T_{PBLH}	PB Data Hold Time	30	—	30	—
	Serial I/0				
T_{PDW}(1)	PA6 XMTR TTL	—	500	—	500
T_{CMOS}(1)	PA6 XMTR CMOS	—	1000	—	1000
T_{CPW}	PA4 RCVR S/R Clock Width	4 T_{CYC}	—	4 T_{CYC}	—
T_{PDW}(1)	PA4 XMTR Clock—S/R Mode (TTL)	—	500	—	500
T_{CMOS}(1)	PA4 XMTR Clock—S/R Mode (CMOS)	—	1000	—	1000

NOTE 1: Maximum Load Capacitance: 50pF
Passive Pull-Up Required

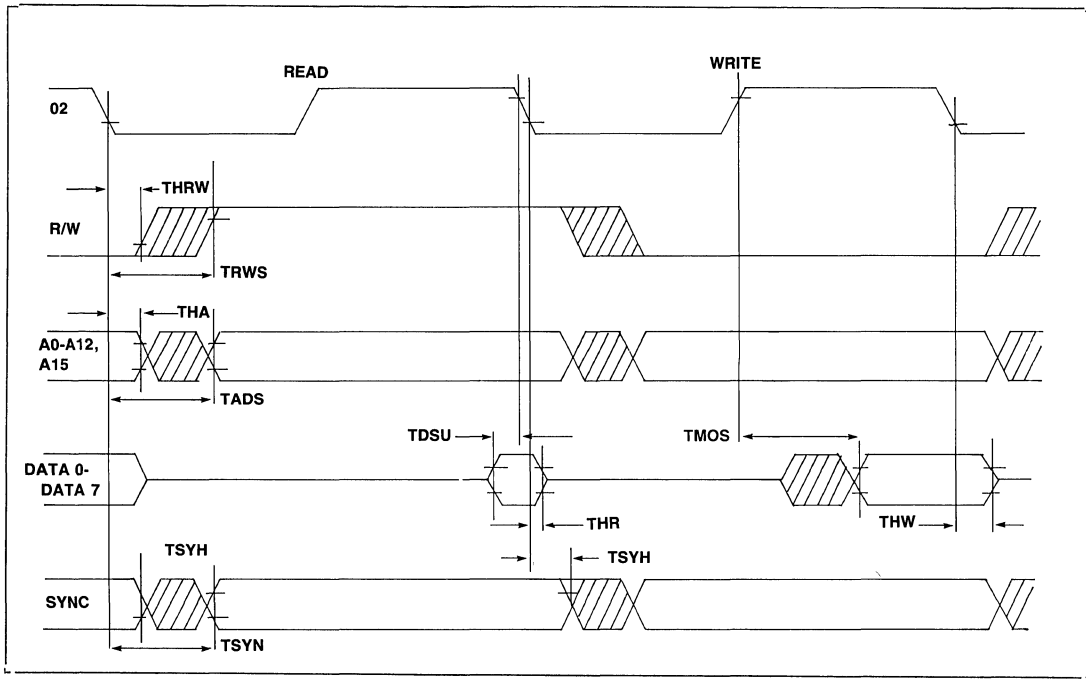
E.5.1 I/O, Edge Detect, Counter, and Serial I/O Timing



E.6 MICROPROCESSOR TIMING (D0-D7, A0-A12, A15, SYNC, R/W)

SYMBOL	PARAMETER	1 MHz		2 MHz	
		MIN	MAX	MIN	MAX
T_{RWS}	R/W Setup Time	—	225	—	140
T_{ADS}	A0-A12, A15 Setup Time	—	150	—	75
T_{DSU}	D0-D7 Data Setup Time	50	—	35	—
T_{HR}	D0-D7 Read Hold Time	10	—	10	—
T_{HW}	D0-D7 Write Hold Time	30	—	30	—
T_{MOS}	D0-D7 Write Output Delay	—	175	—	130
T_{SYN}	SYNC Setup	—	225	—	175
T_{HA}	A0-A12, A15 Hold Time	30	—	30	—
T_{HRW}	R/W Hold Time	30	—	30	—
T_{ACC}	External Memory Access Time $T_{ACC} = T_{CYC} - T_F - T_{ADS} - T_{DSU}$	—	T_{ACC}	—	T_{ACC}
T_{SYH}	SYNC Hold Time	30	—	30	—

E.6.1 Microprocessor Timing Diagram



Rockwell

R6518
One-Chip Microprocessor

INTRODUCTION

FEATURES

- Enhanced 6502 CPU
  - — Four new bit manipulation instructions:
    - Set Memory Bit (SMB)
    - Reset Memory Bit (RMB)
    - Branch on Bit Set (BBS)
    - Branch on Bit Reset (BBR)
  - — Decimal and binary arithmetic modes
  - — 13 addressing modes
  - — True indexing
- 192-byte static RAM
- 16 TTL-compatible I/O lines
- One 8-bit port with programmable latched input
- Two 16-bit programmable counter/timers, with latches
  - — Pulse width measurement
  - — Asymmetrical pulse generation
  - — Pulse generation
  - — Interval timer
  - — Event counter
  - — Retriggerable interval timer
- Serial port
  - — Full-duplex asynchronous operation mode
  - — Selectable 5- to 8-bit characters
  - — Wake-up feature
  - — Synchronous shift register mode
  - — Standard programmable bit rates, programmable up to 62.5K bits/sec @ 1 MHz
- Ten interrupts
  - — Four edge-sensitive lines; two positive, two negative
  - — Reset
  - — Non-maskable
  - — Two counter underflows
  - — Serial data received
  - — Serial data transmitted
- 16K bytes of external memory addressing
- Flexible clock circuitry
  - — 2 MHz or 1 MHz internal operation
  - — Internal clock with external 2 MHz to 4 MHz series resonant XTAL at two times internal frequency
  - — External clock input divided by one or two
- 1 μs minimum instruction execution time @ 2 MHz
- NMOS-3 silicon gate, depletion load technology
- Single +5V power supply
- 12 mW stand-by power for 32 bytes of the 192-byte RAM
- 40-pin DIP
- 44-pin PLCC

SUMMARY

The Rockwell R6518 one-chip microprocessor is a complete 8-bit microcomputer on a single VLSI chip with the exception of external user-provided application ROM. The R6518 interfaces with up to 16K bytes of external memory via a multiplexed address/data bus.

The R6518 consists of an enhanced R6502 CPU, an internal clock oscillator, 192 bytes of Random Access Memory (RAM) and versatile interface circuitry. The interface circuitry includes two 16-bit programmable timer/counters, 16 bidirectional input/output lines (including four edge-sensitive lines and input latching on one 8-bit port), a full-duplex serial I/O channel, ten interrupts and 16K of external address space.

The innovative architecture and the demonstrated high performance of the R6502 CPU, as well as instruction simplicity, results in system cost-effectiveness and a wide range of computational power. These features make this device a leading candidate for microprocessor applications.

Rockwell supports development of R6500/* single-chip microcomputer applications with the Rockwell Design Center Low Cost Emulator (LCE) and R6500/* Personality Set. Program assembly can be performed on any user-provided computer using an assembler generating R6500/* machine code. The machine code can then be downloaded via an RS-232-C serial channel to the LCE for program debugging and in-circuit emulation. Refer to the RDC-3101/2 LCE and RDC-3XX R6500/* Personality Set data sheets, Order No.s RDC17 and RDC06, respectively, for detailed information.

This product description is for the reader familiar with the R6502 CPU hardware and programming capabilities. A detailed description of the R6502 CPU hardware is included in the R6500 Microcomputer System Hardware Manual (Order No. 201). A description of the instruction capabilities of the R6502 CPU is contained in the R6500 Microcomputer System Programming Manual (Order No. 202).

CUSTOMER OPTIONS

The R6518 is available in 1 MHz (no suffix letter) or 2 MHz (A suffix) versions.

ORDERING INFORMATION

Part Number:
R6518

Temperature Range (T_L to T_H):
Blank = 0°C to +70°C
E = −40°C to +85°C

Package
C = 40-Pin Ceramic DIP
P = 40-Pin Plastic DIP
J = 44-Pin Plastic Leaded Chip Carrier (PLCC)

Frequency
1 = 1 MHz
A = 2 MHz

INTERFACE

This section presents the interface requirements for the R6518 single-chip microprocessor. Figure 1 is the Interface Diagram, Figure 2 shows the pin configurations and Table 1 describes the function of each pin. A detailed block diagram of the device and its internal function is illustrated in Figure 3. Package dimensions are illustrated in the last section.

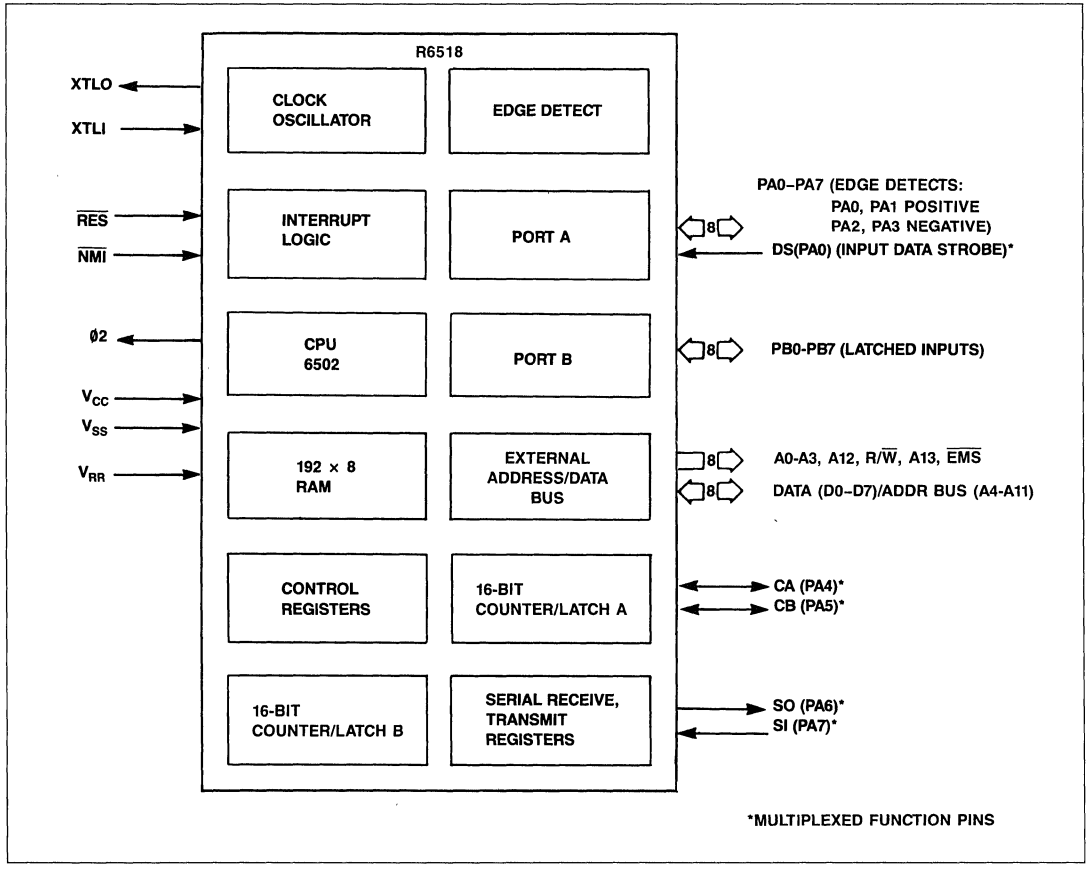
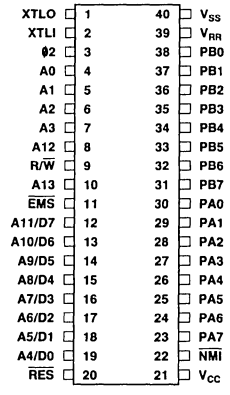
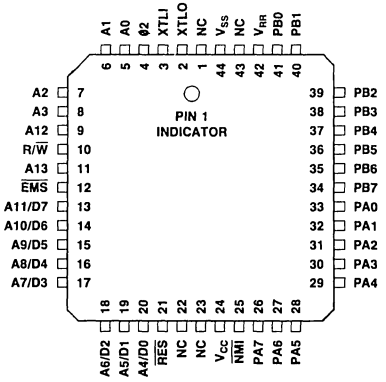


Figure 1. Interface Diagram



40-PIN DIP



44-PIN PLCC

Figure 2. R6518 Pin Assignments

Table 1. Pin Description

Signal Name	Pin Number DIP	Pin Number PLCC	Description
V_{CC}	21	24	Main power supply +5V
V_{RR}	39	42	Separate power pin for RAM. In the event that V_{CC} power is lost, this power retains 32 bytes of RAM Data.
V_{SS}	40	44	Signal and power ground (0V)
XTLI	2	3	Crystal or clock input for internal clock oscillator. Also allows input of X1 clock signal if XTLO is connected to V_{SS}, or X2 clock if XTLO is floated.
XTLO	1	2	Crystal output from internal clock oscillator.
$\overline{RES}$	20	21	The Reset input is used to initialize the device. This signal must not transition from low to high for at least eight cycles after V_{CC} reaches operating range and the internal oscillator is stabilized.
ϕ2	3	4	Clock signal output at internal frequency.
$\overline{NMI}$	22	25	A negative going edge on the Non-Maskable Interrupt signal requests that a non-maskable interrupt be generated within the CPU.
PA0-PA7 PB0-PB7	30-23 38-31	33-26 41-34	Two 8-bit ports used for either input/output. Each line of Ports A and B consists of an active transistor to V_{SS} and a passive pull-up to V_{CC}.
A0-A3, A12, R/$\overline{W}$ A13, & $\overline{EMS}$	4-11	5-12	The address and timing pins have an active transistor to V_{SS} and a passive pull-up to V_{CC}.
A4-A11/D0-D7	19-12	20-13	These multiplexed address/data pins have active pull-up and pull-down transistors.
NC	—	1,22 23,43	No connection. These pins should be left open.

SYSTEM ARCHITECTURE

This section provides a functional description of the R6518. Functionally it consists of a CPU, RAM memory, two 8-bit parallel I/O ports, a serial I/O port, dual counter/latch circuits, a mode control register, and an interrupt flag/enable dual register circuit. A block diagram of the system is shown in Figure 3.

NOTE

Throughout this document, unless specified otherwise, all memory or register address locations are specified in hexadecimal notation.

CPU LOGIC

The internal CPU is a standard 6502 configuration with an 8-bit Accumulator register, two 8-bit index registers (X and Y); an 8-bit Stack Pointer register, an ALU, a 16-bit Program Counter, and standard instruction register/decode and internal timing control logic.

ACCUMULATOR

The Accumulator is a general purpose 8-bit register that stores the results of most arithmetic and logic operations. In addition, the Accumulator usually contains one of the two data words used in these operations.

INDEX REGISTERS

There are two 8-bit index registers, X and Y. Each index register can be used as a base to modify the address data program counter and thus obtain a new address—the sum of the program counter contents and the index register contents.

When executing an instruction which specifies indirect addressing, the CPU fetches the op code and the address, and modifies the address from memory by adding the index register to it prior to loading or storing the value of memory.

Indexing greatly simplifies many types of programs, especially those using data tables.

STACK POINTER

The Stack Pointer is an 8-bit register. It is automatically incremented and decremented under control of the microprocessor to perform stack manipulation in response to either user instructions, an internal $\overline{IRQ}$ interrupt, or the external interrupt line $\overline{NMI}$. The Stack Pointer must be initialized by the user program.

The stack allows simple implementation of multiple level interrupts, subroutine nesting and simplification of many types of data manipulation. The JSR, BRK, RTI and RTS instructions use the stack and Stack Pointer.

The stack can be envisioned as a deck of cards which may only be accessed from the top. The address of a memory location is stored (or "pushed") onto the stack. Each time data are to be pushed onto the stack, the Stack Pointer is placed on the Address Bus, data are written into the memory location addressed by the Stack Pointer, and the Stack Pointer is decremented by 1. Each time data are read (or "pulled") from the stack, the Stack Pointer is incremented by 1. The Stack Pointer is then placed on the Address Bus, and data are read from the memory location addressed by the Pointer.

The stack is located on zero page, i.e., memory locations 00FF-0040. After reset, which leaves the Stack Pointer indeterminate, normal usage calls for its initialization at 00FF.

ARITHMETIC AND LOGIC UNIT (ALU)

All arithmetic and logic operations take place in the ALU, including incrementing and decrementing internal registers (except the Program Counter). The ALU cannot store data for more than one cycle. If data are placed on the inputs to the ALU at the beginning of a cycle, the result is always gated into one of the storage registers or to external memory during the next cycle.

Each bit of the ALU has two inputs. These inputs can be tied to various internal buses or to a logic zero; the ALU then generates the function (AND, OR, SUM, and so on) using the data on the two inputs.

PROGRAM COUNTER

The 16-bit Program Counter provides the addresses that are used to step the processor through sequential instructions in a program. Each time the processor fetches an instruction from program memory, the lower (least significant) byte of the Program Counter (PCL) is placed on the low-order bits of the Address Bus and the higher (most significant) byte of the Program Counter (PCH) is placed on the high-order 8 bits of the Address Bus. The Counter is incremented each time an instruction or data is fetched from program memory.

INSTRUCTION REGISTER AND INSTRUCTION DECODE

Instructions are fetched from ROM or RAM and gated onto the Internal Data Bus. These instructions are latched into the Instruction Register then decoded along with timing and interrupt signals to generate control signals for the various registers.

TIMING CONTROL

The Timing Control Logic keeps track of the specific instruction cycle being executed. This logic is set to T0 each time an instruction fetch is executed and is advanced at the beginning of each Phase One clock pulse for as many cycles as are required to complete the instruction. Each data transfer which takes place between the registers is caused by decoding the contents of both the instruction register and timing control unit.

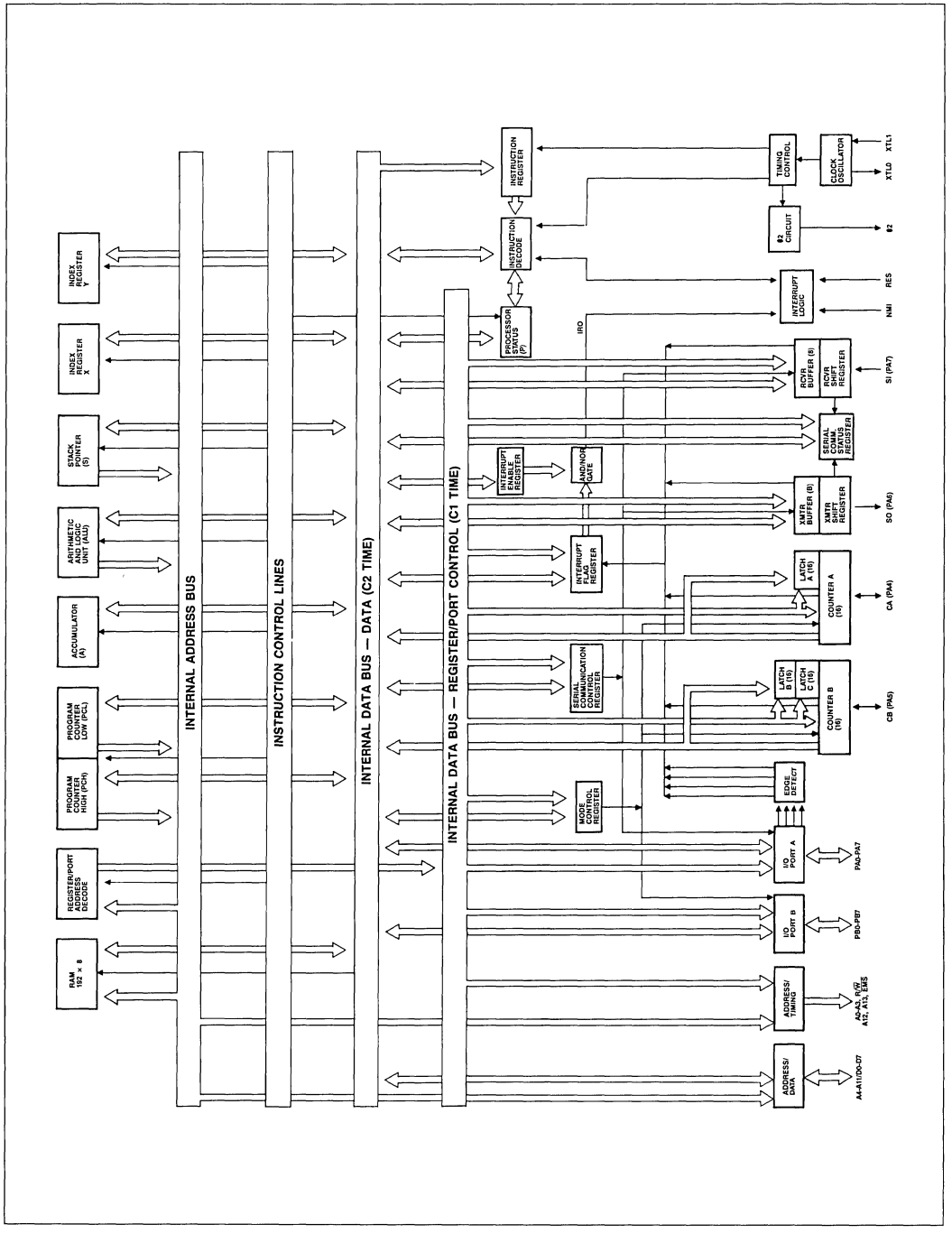


Figure 3. System Block Diagram

INTERRUPT LOGIC

Interrupt logic controls the sequencing of three interrupts; $\overline{RES}$, $\overline{NMI}$ and $\overline{IRQ}$. $\overline{IRQ}$ is generated by any one of eight conditions: 2 Counter Overflows, 2 Positive Edge Detects, 2 Negative Edge Detects, and 2 Serial Port Conditions.

The R6518 requires that 3-byte JMP instructions for $\overline{NMI}$, $\overline{RES}$ and $\overline{IRQ}$ be programmed in user-provided external ROM at hex locations 3FF7, 3FFA and 3FFD, respectively. These instructions must jump to the first instruction of the respective reset or interrupt handler routine. Terminate the interrupt handler routines as normal with an RTI. See Power-On Reset for details of $\overline{RES}$ internal initialization.

NEW INSTRUCTIONS

In addition to the standard 6502 instruction set, four instructions have been added to the device to simplify operations that previously required a read/modify/write operation. In order for these instructions to be equally applicable to either I/O port, with or without mixed input and output functions, the I/O ports have been designed to read the contents of the specified port data register during the Read cycle of the read/modify/write operation, rather than I/O pins as in normal read cycles. The added instructions and their format are explained in the following subparagraphs. Refer to Appendix A for the Op Code mnemonic addressing matrix for these added instructions.

SET MEMORY BIT (SMB m, ADDR.)

This instruction sets to "1" one of the 8 bits specified by the zero page address (memory or I/O port). The first byte of the instruction specifies the SMB operation and 1 of 8 bits to be set. The second byte of the instruction designates address (00-FF) of the byte or I/O port to be operated upon.

RESET MEMORY BIT (RMB m, ADDR.)

This instruction is the same in operation and format as the SMB instruction except that a reset to "0" of the bit results.

BRANCH ON BIT SET RELATIVE (BBS m, ADDR, DEST)

This instruction tests one of 8 bits designated by a three bit immediate field within the first byte of the instruction. The second byte is used to designate the address of the byte to be tested within the zero page address range (memory or I/O ports). The third byte of the instruction is used to specify the 8 bit relative address to which the instruction branches if the bit tested is a "1". If the bit tested is not set, the next sequential instruction is executed.

BRANCH ON BIT RESET RELATIVE (BBR m, ADDR, DEST)

This instruction is the same in operation and format as the BBS instruction except that a branch takes place if the bit tested is a "0".

READ ONLY MEMORY (ROM)

This device has no internal application ROM. Up to 16K of external memory can be attached via the 16 address/data and timing pins.

RANDOM ACCESS MEMORY (RAM)

The RAM consists of 192 bytes of read/write memory with an assigned page zero address of 0040 through 00FF. The R6518 provides a separate power pin (V_{RR}) which may be used for standby power for 32 bytes located at 0040-005F. In the event of the loss of V_{CC} power, the lowest 32 bytes of RAM data will be retained if standby power is supplied to the V_{RR} pin. If the RAM data retention is not required then V_{RR} must be connected to V_{CC}. During operation V_{RR} must be at the V_{CC} level.

For the RAM to retain data upon loss of V_{CC}, V_{RR} must be supplied within operating range and $\overline{RES}$ must be driven low at least eight Ø2 clock pulses before V_{CC} falls out of operating range. $\overline{RES}$ must then be held low while V_{CC} is out of operating range and until at least eight Ø2 clock cycles after V_{CC} is again within operating range and the internal Ø2 oscillator is stabilized. V_{RR} must remain within V_{CC} operating range during normal operation. When V_{CC} is out of operating range, V_{RR} must remain within the V_{RR} retention range in order to retain data. Figure 4 shows typical waveforms.

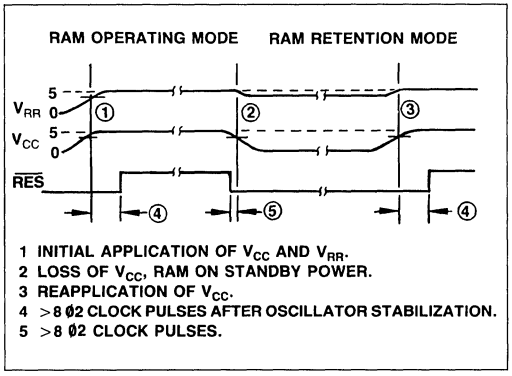


Figure 4. Data Retention Timing

CLOCK OSCILLATOR

A reference frequency can be generated with the on-chip oscillator using an external crystal. The oscillator reference frequency passes through an internal countdown network (divide by 2) to obtain the internal operating frequency (see Figure 5a). The on-chip oscillator is designed for a parallel resonant crystal connected between XTLI and XTLO pins. The equivalent oscillator circuit is shown in Figure 5.

A parallel resonant crystal is specified by its load capacitance and series resonant resistance. For proper oscillator operation, the load capacitance (C_L), series resistance (R_s) and the crystal resonant frequency (F) must meet the following two relations:

$$(C + 27) = 2C_L \quad \text{or} \quad C = 2C_L - 27\ \text{pF}$$

$$R_s \leq R_{smax} = \frac{2 \times 10^6}{(FC_L)^2}$$

where: F is in MHz; C_L is in pF; and R is in ohms.

To select a parallel resonant crystal for the oscillator, first select the load capacitance from a crystal manufacturer's catalog. Next, calculate R_{smax} based on F and C_L. The selected crystal must have a R_s less than the R_{smax}.

For example, if C_L = 22 pF for a 4 MHz parallel resonant crystal, then

$$C = (2 \times 22) - 27 = 17 \text{ pF}$$
(use standard value of 18 pF)

The series resistance of the crystal must be less than

$$R_{smax} = \frac{2 \times 10^6}{(4 \times 22)^2} = 258 \text{ ohms}$$

Internal timing can also be controlled by driving the XTLI pin with an external frequency source. Figure 5b shows typical connections. If XTLO is left floating, the external source is divided by the internal countdown network. However, if XTLO is tied to V_{SS}, the internal countdown network is bypassed causing the chip to operate at the frequency of the external source.

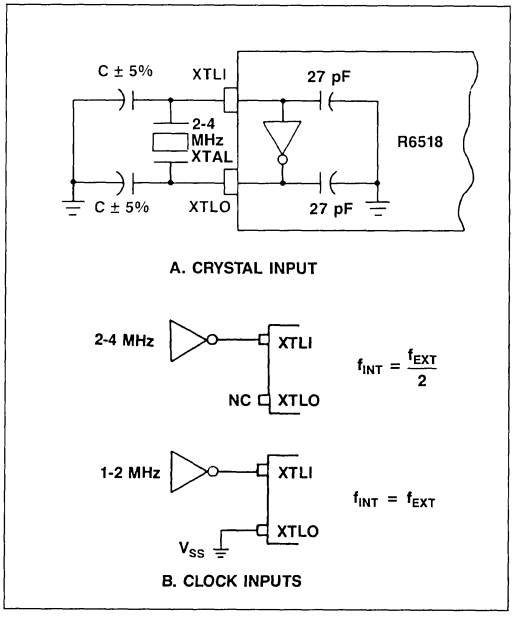


Figure 5. Clock Oscillator Input Options

MODE CONTROL REGISTER (MCR)

The Mode Control Register contains a control bit for Port B and mode select bits for Counter A and Counter B. Its setting, along with the setting of the Serial Communications Control Register (SCCR), determines the basic configuration of the device in any application. Initializing this register is one of the first actions of any software program. MCR bits 7, 6, 5 must remain 1s in order for external memory referencing to be enabled. The Mode Control Register bit assignment is shown in Figure 6.

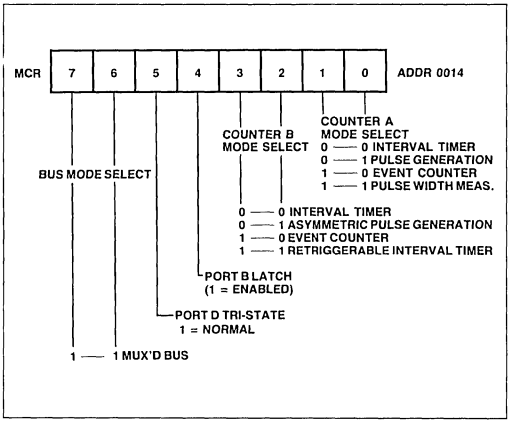


Figure 6. Mode Control Register

The use of Counter A Mode Select is shown in Section "Counter A".

The use of Counter B Mode Select is shown in Section "Counter B".

The use of Port B Latch Enable is shown in Section "Port B (PB)".

INTERRUPT FLAG REGISTER (IFR) AND INTERRUPT ENABLE REGISTER (IER)

An $\overline{IRQ}$ interrupt request can be initialized by any or all of eight possible sources. These sources are all capable of being enabled or disabled by the use of the appropriate interrupt enabled bits in the Interrupt Enable Register (IER). Multiple simultaneous interrupts will cause the $\overline{IRQ}$ interrupt request to remain active until all interrupting conditions have been serviced and cleared.

The Interrupt Flag Register contains the information that indicates which I/O or counter needs attention. The contents of the Interrupt Flag Register may be examined at any time by reading at address: 0011. Edge detect IFR bits may be cleared by executing a RMB instruction at address location 0010. The RMB X, (0010) instruction reads FF, modifies bit X to a "0", and writes the modified value at address location 0011. In this way IFR bits set to a "1" after the read cycle of a Read-Modify-Write instruction (such as RMB) are protected from being cleared. A logic "1" is ignored when writing to edge detect IFR bits.

Each IFR bit has a corresponding bit in the Interrupt Enable Register which can be set to a "1" by writing a "1" in the respective bit position at location 0012. Individual IER bits may be cleared by writing a "0" in the respective bit position, or by $\overline{RES}$. If set to a "1", an IRQ will be generated when the corresponding IFR bit becomes true. The Interrupt Flag Register and Interrupt Enable Register bit assignments are shown in Figure 7 and the functions of each bit are explained in Table 2.

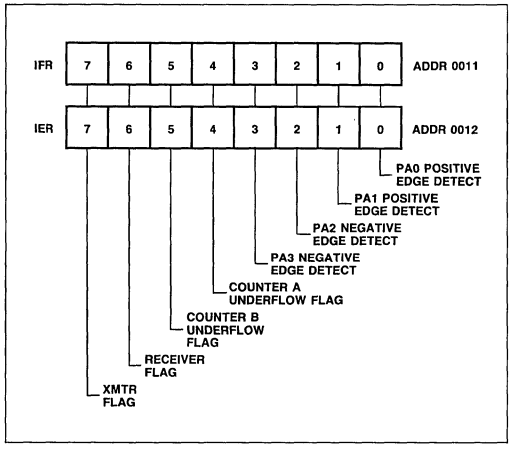


Figure 7. Interrupt Enable and Flag Registers

PROCESSOR STATUS REGISTER

The 8-bit Processor Status Register, shown in Figure 8 contains seven status flags. Some of these flags are controlled by the user program; others may be controlled both by the user's program and the CPU. The R6502 instruction set contains a number of conditional branch instructions which are designed to allow testing of these flags. Each of the eight processor status flags is described in the following sections.

CARRY BIT (C)

The Carry Bit (C) can be considered as the ninth bit of an arithmetic operation. It is set to logic 1 if a carry from the eighth bit has occurred or cleared to logic 0 if no carry occurred as the result of arithmetic operations.

The Carry Bit may be set or cleared under program control by use of the Set Carry (SEC) or Clear Carry (CLC) instruction, respectively. Other operations which affect the Carry Bit are ADC, ASL, CMP, CPX, CPY, LSR, PLP, ROL, ROR, RTI, and SBC.

Table 2. Interrupt Flag Register Bit Codes

Bit Code	Function
IFR 0:	PA0 Positive Edge Detect Flag—Set to a "1" when a positive going edge is detected on PA0. Cleared by RMB 0 (0010) instruction or by $\overline{RES}$.
IFR 1:	PA1 Positive Edge Detect Flag—Set to a 1 when a positive going edge is detected on PA1. Cleared by RMB 1 (0010) instruction or by $\overline{RES}$.
IFR 2:	PA2 Negative Edge Detect Flag—Set to a 1 when a negative going edge is detected on PA2. Cleared by RMB 2 (0010) instruction or by $\overline{RES}$.
IFR 3:	PA3 Negative Edge Detect Flag—Set to 1 when a negative going edge is detected on PA3. Cleared by RMB 3 (0010) instruction or by $\overline{RES}$.
IFR 4:	Counter A Underflow Flag—Set to a 1 when Counter A underflow occurs. Cleared by reading the Lower Counter A at location 0018, by writing to address location 001A, or by $\overline{RES}$.
IFR 5:	Counter B Underflow Flag—Set to a 1 when Counter B underflow occurs. Cleared by reading the Lower Counter B at location 001C, by writing to address location 001E, or by $\overline{RES}$.
IFR 6:	Receiver Interrupt Flag—Set to a 1 when any of the Serial Communication Status Register bits 0 through 3 is set to a 1. Cleared when the Receiver Status bits (SCSR0-3) are cleared or by $\overline{RES}$.
IRF 7:	Transmitter Interrupt Flag—Set to a 1 when SCSR6 is set to a 1 while SCSR5 is a 0 or SCSR7 is set to a 1. Cleared when the Transmitter Status bits (SCSR6 & 7) are cleared or by $\overline{RES}$.

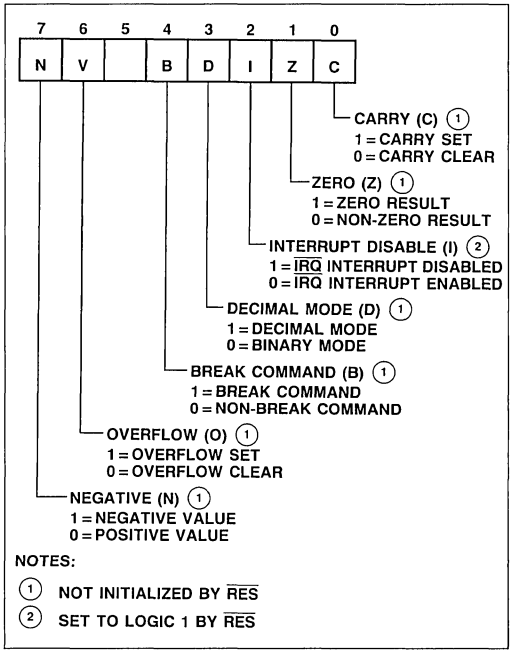


Figure 8. Processor Status Register

ZERO BIT (Z)

The Zero Bit (Z) is set to logic 1 by the CPU during any data movement or calculation which sets all 8 bits of the result to zero. This bit is cleared to logic 0 when the resultant 8 bits of a data movement or calculation operation are not all zero. The R6500 instruction set contains no instruction to specifically set or clear the Zero Bit. The Zero Bit is, however, affected by the following instructions; ADC, AND, ASL, BIT, CMP, CPX, CPY, DEC, DEX, DEY, EOR, INC, INX, INY, LDA, LDX, LDY, LSR, ORA, PLA, PLP, ROL, ROR, RTI, SBC, TAX, TAY, TXA, TSX, and TYA.

INTERRUPT DISABLE BIT (I)

The Interrupt Disable Bit (I) is used to control the servicing of an interrupt request ($\overline{IRQ}$). If the I Bit is reset to logic 0, the $\overline{IRQ}$ signal will be serviced. If the bit is set to logic 1, the $\overline{IRQ}$ signal will be ignored. The CPU will set the Interrupt Disable Bit to logic 1 if a RESET ($\overline{RES}$), $\overline{IRQ}$, or Non-Maskable Interrupt ($\overline{NMI}$) signal is detected.

The I bit is cleared by the Clear Interrupt Mask Instruction (CLI) and is set by the Set Interrupt Mask Instruction (SEI). This bit is set by the BRK Instruction. The Return from Interrupt (RTI) and Pull Processor Status (PLP) instructions will also affect the I bit.

DECIMAL MODE BIT (D)

The Decimal Mode Bit (D), is used to control the arithmetic mode of the CPU. When this bit is set to logic 1, the adder operates as a decimal adder. When this bit is cleared to logic 0, the adder operates as a straight binary adder. The adder mode is controlled only by the programmer. The Set Decimal Mode (SED) instruction will set the D bit; the Clear Decimal Mode (CLD) instruction will clear it. The PLP and RTI instructions also effect the Decimal Mode Bit.

CAUTION

The Decimal Mode Bit will either set or clear in an unpredictable manner upon power application. This bit must be initialized to the desired state by the user program or erroneous results may occur.

BREAK BIT (B)

The Break Bit (B) is used to determine the condition which caused the $\overline{IRQ}$ service routine to be entered. If the $\overline{IRQ}$ service routine was entered because the CPU executed a BRK command, the Break Bit will be set to logic 1. If the $\overline{IRQ}$ routine was entered as the result of an $\overline{IRQ}$ signal being generated, the B bit will be cleared to logic 0. There are no instructions which can set or clear this bit.

OVERFLOW BIT (V)

The Overflow Bit (V) is used to indicate that the result of a signed, binary addition, or subtraction, operation is a value that cannot be contained in seven bits ($-128 \leq n \leq 127$).

This indicator only has meaning when signed arithmetic (sign and seven magnitude bits) is performed. When the ADC or SBC instruction is performed, the Overflow Bit is set to logic 1 if the polarity of the sign bit (bit 7) is changed because the result exceeds +127 or −128; otherwise the bit is cleared to logic 0. The V bit may also be cleared by the programmer using a Clear Overflow (CLV) instruction.

The Overflow Bit may also be used with the BIT instruction. The BIT instruction which may be used to sample interface devices, allows the overflow flag to reflect the condition of bit 6 in the sampled field. During a BIT instruction the Overflow Bit is set equal to the content of the bit 6 on the data tested with BIT instruction. When used in this mode, the overflow has nothing to do with signed arithmetic, but is just another sense bit for the microprocessor. Instructions which affect the V flag are ADC, BIT, CLV, PLP, RTI and SBC.

NEGATIVE BIT (N)

The Negative Bit (N) is used to indicate that the sign bit (bit 7), in the resulting value of a data movement or data arithmetic operation, is set to logic 1. If the sign bit is set to logic 1, the resulting value of the data movement or arithmetic operation is negative; if the sign bit is cleared, the result of the data movement or arithmetic operation is positive. There are no instructions that set or clear the Negative Bit since the Negative Bit represents only the status of a result. The instructions that effect the state of the Negative Bit are: ADC, AND, ASL, BIT, CMP, CPX, CPY, DEC, DEX, DEY, EOR, INC, INX, INY, LDA, LDX, LDY, LSR, ORA, PLA, PLP, ROL, ROR, RTI, SBC, TAX, TAY, TSX, TXA, AND TYA.

PARALLEL INPUT/OUTPUT PORTS

The R6518 has 16 I/O lines grouped into two 8-bit ports (PA, PB). Ports A and B may be used either for input or output individually or in groups of any combination.

Multifunction I/O's in Port A are protected from normal port I/O instructions when they are programmed to perform a multiplexed function.

Internal pull-up resistors (FET's with an impedance range of 3K ≤ Rpu ≤ 12K ohm) are provided on all port pins.

The direction of the I/O lines are controlled by 8-bit port registers located in page zero. This arrangement provides quick programming access using simple two-byte zero page address instructions. There are no direction registers associated with the I/O ports, which simplifies I/O handling. The I/O addresses are shown in Table 3. I/O Port Timing is shown on page 29.

Table 3. I/O Port Addresses

Port	Address
A	0000
B	0001

INPUTS

Inputs for Ports A and B are enabled by loading logic 1 into all I/O port register bit positions that are to correspond to I/O input lines. A low (<0.8V) input signal will cause a logic 0 to be read when a read instruction is issued to the port register. A high (>2.0V) input will cause a logic 1 to be read. An $\overline{RES}$ signal forces both I/O port registers to logic 1 thus initially treating all I/O lines as inputs.

The status of the input lines can be interrogated at any time by reading the I/O port addresses. Note that this will return the actual status of the input lines, not the data written into the I/O port registers.

Ready/Modify/Write instructions can be used to modify the operation of PA and PB. During the Read cycle of a Read/Modify/Write instruction the Port I/O register is read. For all other read instructions the port input lines are read. Read/Modify/Write instructions are: ASL, DEC, INC, LSR, RMB, ROL, ROR, and SMB.

OUTPUTS

Outputs for Ports A and B are controlled by writing the desired I/O line output states into the corresponding I/O port register bit positions. A logic 1 will force a high (>2.4V) output while a logic 0 will force a low (<0.4V) output.

PORT A (PA)

Port A can be programmed via the Mode Control Register (MCR) and the Serial Communications Control Register (SCCR) as a standard parallel 8-bit, bit independent, I/O port or as serial channel I/O lines, counter I/O lines, or an input data strobe for the Port B input latch option. Table 4 tabulates the control and usage of Port A.

In addition to their normal I/O functions, PA0 and PA1 can detect positive going edges, and PA2 and PA3 can detect negative going edges. A proper transition on these pins will set a corresponding status bit in the IFR and generate an interrupt request if the respective Interrupt Enable Bit is set. The maximum rate at which an edge can be detected is one-half the phase 2 (Ø2) clock rate. Edge detection timing is shown on page 29.

PORT B (PB)

Port B can be programmed as an 8 bit, bit independent I/O port. It has a latched input capability which may be enabled or disabled via the Mode Control Register (MCR). Table 5 tabulates the control and usage of Port B. An Input Data Strobe signal must be provided through PA0 when Port B is programmed to be used with latched input option. Input data latch timing for Port B is shown on page 29.

Table 5. Port B Control & Usage

Pin Name	I/O Mode		Latch Mode	
	MCR4 = 0		MCR4 = 1 (2)	
	Signal		Signal	
	Name	Type (1)	Name	Type
PB0	PB0	I/O	PB0	INPUT
PB1	PB1	I/O	PB1	INPUT
PB2	PB2	I/O	PB2	INPUT
PB3	PB3	I/O	PB3	INPUT
PB4	PB4	I/O	PB4	INPUT
PB5	PB5	I/O	PB5	INPUT
PB6	PB6	I/O	PB6	INPUT
PB7	PB7	I/O	PB7	INPUT

(1) Resistive pull-up, active buffer pull down
(2) Input data is stored in port B latch by PA0 pulse

Table 4. Port A Control & Usage

	PA0 I/O		PORT B LATCH MODE			
	MCR4 = 0		MCR4 = 1			
	SIGNAL		SIGNAL			
	NAME	TYPE	NAME	TYPE		
PA0 (2)	PA0	I/O	PORT B LATCH STROBE	INPUT (1)		
PA1 (2)	PA1-PA3 I/O					
	SIGNAL					
PA2 (3)	NAME	TYPE				
PA3 (3)	PA1 PA2 PA3	I/O I/O I/O				
PA4	PA4 I/O		COUNTER A I/O			
	MCR0 = 0 MCR1 = 0 SCCR7 = 0 RCVR S/R MODE = 0 (4) (5)		MCR0 = 1 MCR1 = 0 SCCR7 = 0 RCVR S/R MODE = 0 (4)		SCCR7 = 0 SCCR6 = 0 MCR1 = 1	
	SIGNAL		SIGNAL		SIGNAL	
	NAME	TYPE	NAME	TYPE	NAME	TYPE
	PA4	I/O	CNTA	OUTPUT	CNTA	INPUT (1)
	SERIAL I/O SHIFT REGISTER CLOCK					
	SCCR7 = 1 SCCR5 = 1		RCVR S/R MODE = 1 (4)			
	SIGNAL		SIGNAL			
	NAME	TYPE	NAME	TYPE		
	XMTR CLOCK	OUTPUT	RCVR CLOCK	INPUT (1)		
PA5	PA5 I/O		COUNTER B I/O			
	MCR3 = 0 MCR2 = 0		MCR3 = 0 MCR2 = 1		MCR3 = 1 MCR2 = X	
	SIGNAL		SIGNAL		SIGNAL	
	NAME	TYPE	NAME	TYPE	NAME	TYPE
	PA5	I/O	CNTB	OUTPUT	CNTB	INPUT (1)
PA6	PA6 I/O		SERIAL I/O XMTR OUTPUT			
	SCCR7 = 0		SCCR7 = 1			
	SIGNAL		SIGNAL			
	NAME	TYPE	NAME	TYPE		
	PA6	I/O	XMTR	OUTPUT		
PA7	PA7 I/O		SERIAL I/O RCVR INPUT			
	SCCR6 = 0		SCCR6 = 1			
	SIGNAL		SIGNAL			
	NAME	TYPE	NAME	TYPE		
	PA7	I/O	RCVR	INPUT (1)		

Notes:
(1) Hardware Buffer Float
(2) Positive Edge Detect
(3) Negative Edge Detect
(4) RCVR S/R Mode = 1 when SCCR6 • $\overline{SCCR5}$ • SCCR4 = 1
(5) For the following mode combinations PA4 is available as an input only pin:
$\overline{SCCR7}$•SCCR6•SCCR5.MCR1
+ $\overline{SCCR7}$•SCCR6•$\overline{SCCR4}$•MCR1
+ SCCR7•$\overline{SCCR6}$•$\overline{SCCR5}$
+ SCCR7•$\overline{SCCR5}$•$\overline{SCCR4}$•

SERIAL INPUT/OUTPUT CHANNEL

The device provides a full duplex Serial I/O channel with programmable bit rates and operating modes. The serial I/O functions are controlled by the Serial Communication Control Register (SCCR). The SCCR bit assignment is shown in Figure 9. The serial bit rate is determined by Counter A for all modes except the Receiver Shift Register (RCVR S/R) mode for which an external shift clock must be provided. The maximum data rate using the internal clock is 62.5K bits per second (@ Ø2 = 1 MHz). The transmitter (XMTR) and receiver (RCVR) can be independently programmed to operate in different modes and can be independently enabled or disabled.

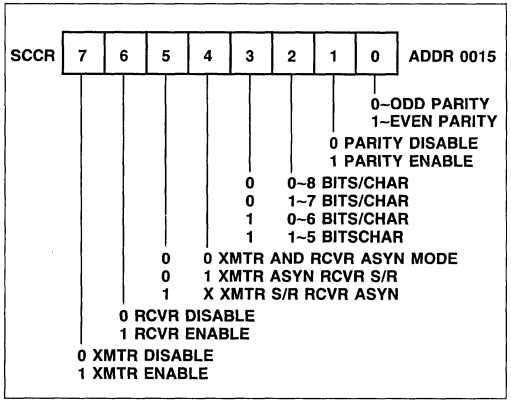


Figure 9. Serial Communication Control Register

Except for the Receiver Shift Register Mode (RCVR S/R), all XMTR and RCVR bit rates will occur at one sixteenth of the Counter A interval timer rate. Counter A is forced into an interval timer mode whenever the serial I/O is enabled in a mode requiring an internal clock.

Whenever Counter A is required as a timing source it must be loaded with the hexadecimal code that selects the data rate for the serial I/O Port. Refer to Section "Counter A," Table 6 for hexadecimal values to represent the desired data rate.

TRANSMITTER OPERATION (XTMR)

The XTMR operation and the transmitter related control/status functions are enabled by bit 7 of the Serial Communications Control Register (SCCR). The transmitter, when in the Asynchronous (ASYN) mode, automatically adds a start bit, one or two stop bits, and when enabled, a parity bit to the transmitted data. A word of transmitted data (in asynchronous parity mode) can have 5-, 6-, 7-, or 8-bits of data. The nine data modes are in Figure 10. When parity is disabled, the 5-, 6-, 7- or 8-bits of data are terminated with two stop bits.

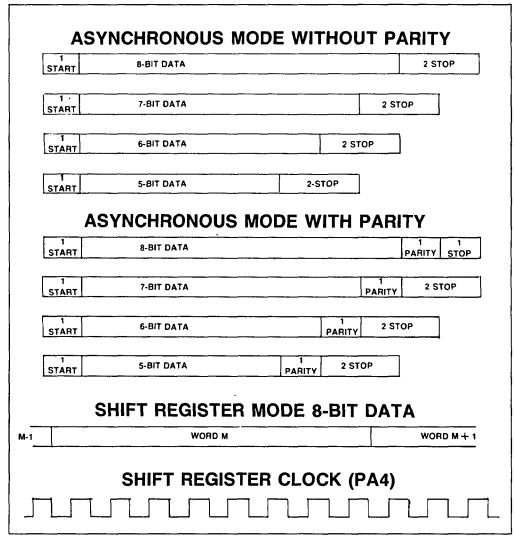


Figure 10. Transmitter Data Modes

In the S/R mode, eight data bits are always shifted out. Bits/character and parity control bits are ignored. The serial data is shifted out via the SO output (PA6) and the shift clock is available at the CA (PA4) pin. When the transmitter under-runs in the S/R mode the SO output and shift clock are held in a high state.

The XMTR Interrupt Flag bit (IFR7) is controlled by Serial Communication Status Register bits SCSR5, SCSR6 and SCSR7.

$$IFR7 = SCSR6\ (\overline{SCSR5} + SCSR7)$$

RECEIVER OPERATION (RCVR)

The receiver and its selected control and status functions are enabled when SCCR6 is set to a "1". In the ASYN mode, data format must have a start bit, appropriate number of data bits, a parity bit (if enabled) and one stop bit. Refer to Figure 10 for a diagram of bit allocations. The receiver bit period is divided into 8 sub-intervals for internal synchronization. The receiver bit stream is synchronized by the start bit and a strobe signal is generated at the appropriate center of each incoming bit. Refer to Figure 11 for ASYN Receive Data Timing. The character assembly process does not start if the start bit signal is less than one-half bit time after a low level is detected on the Receive Data Input. Framing error, over-run, and parity error conditions or a RCVR Data Register Full will set the appropriate status bits, and any of the above conditions will cause an Interrupt Request if the Receiver Interrupt Enable bit is set to logic 1.

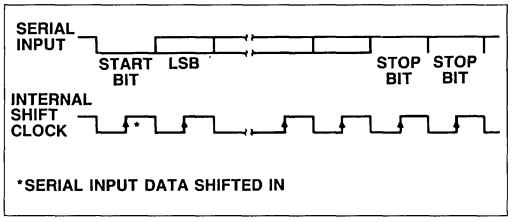


Figure 11. ASYN Receive Data Timing

In the S/R mode, an external shift clock must be provided at CA (PA4) pin along with 8 bits of serial data (LSB first) at the SI input (PA7). The maximum data rate using an external shift clock is one-eighth the internal clock rate. Refer to Figure 12 for S/R Mode Timing.

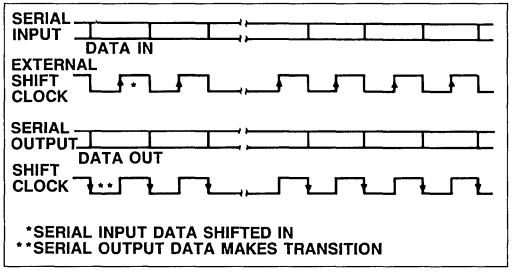


Figure 12. S/R Mode Timing

A RCVR interrupt (IFR6) is generated whenever any of SCSR0-3 are true.

SERIAL COMMUNICATION STATUS REGISTER (SCSR)

The Serial Communication Status Register (SCSR) holds information on various communication error conditions, status of the transmitter and receiver data registers, a transmitter end-of-transmission condition, and a receiver idle line condition (Wake-Up Feature). The SCSR bit assignment is shown in Figure 13. SCSR bit assignments and functions are:

SCSR0: ***Receiver Data Register Full***—Set to a logic 1 when a character is transferred from the Receiver Shift Register to the Receiver Data Register. This bit is cleared by reading the Receiver Data Register, or by $\overline{RES}$ and is disabled if SCCR6 = 0. The SCSR0 bit will not be set to a logic 1 if the received data contains an error condition, instead, a corresponding error bit will be set to a logic 1.

SCSR1: ***Over-Run Error***—Set to a logic 1 when a new character is transferred from the Receiver Shift Register, with the last character still in the Receiver Data Register. This bit is cleared by reading the Receiver Data Register, or by $\overline{RES}$.

SCSR2: ***Parity Error***—Set to a logic 1 when the RCVR is in the ASYN Mode, Parity Enable bit is set, and the received data has a parity error. This bit is cleared by reading the Receiver Data Register or by $\overline{RES}$.

SCSR3: ***Framing Error***—Set to a logic 1 when the received data contains a zero bit after the last data or parity bit in the stop bit slot. Cleared by reading the Receiver Data Register or by $\overline{RES}$. (ASYN Mode only).

SCSR4: ***Wake-Up***—Set to a logic 1 by writing a "1" in bit 4 of address: 0016. The Wake-Up bit is cleared by $\overline{RES}$ or when the receiver detects a string of ten consecutive 1s. When the Wake-Up bit is set SCSR0 through SCSR3 are inhibited.

SCSR5: ***End of Transmission***—Set to a logic 1 by writing a "1" in bit position 5 of address: 0016. The End of Transmission bit is cleared by $\overline{RES}$ or upon writing a new data word into the Transmitter Data Register. When the End-of-Transmission bit is true the Transmitter Data Register Empty bit is disabled until a Transmitter Under-Run occurs.

SCSR6: ***Transmitter Data Register Empty***—Set to a logic 1 when the contents of the Transmitter Data Register are transferred to the Transmitter Shift Register. Cleared upon writing new data into the Transmit Data Register. This bit is initialized to a logic 1 by $\overline{RES}$.

SCSR7: ***Transmitter Under-Run***—Set to a logic 1 when the last data bit is transmitted if the transmitter is in a S/R Mode or when the last stop bit is transmitted if the XMTR is in the ASYN Mode while the Transmitter Data Register Empty Bit is set. Cleared by a transfer of new data into the Transmitter Shift Register, or by $\overline{RES}$.

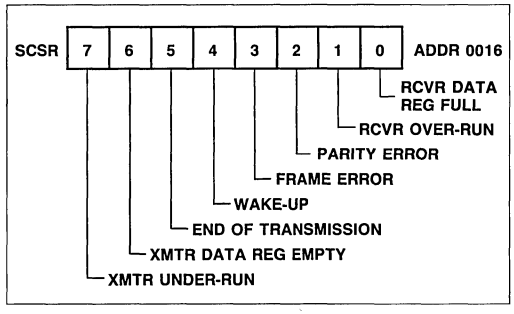


Figure 13. SCSR Bit Allocation

WAKE-UP FEATURE

In multi-distributed microprocessor or microcomputer applications, a destination address is usually included at the beginning of the message. The Wake-Up Feature allows non-selected CPU's to ignore the remainder of the message until the beginning of the next message by setting the Wake-Up bit. As long as the Wake-Up flag is true, the Receiver Data Register Full Flag remains false. The Wake-Up bit is automatically cleared when the receiver detects a string of ten consecutive 1s which indicates an idle transmit line. When the next byte is received, the Receiver Data Register Full Flag signals the CPU to wake-up and read the received data.

COUNTER/TIMERS

The device contains two 16-bit counters (Counter A and Counter B) and three 16-bit latches associated with the counters. Counter A has one 16-bit latch and Counter B has two 16-bit latches. Each counter can be independently programmed to operate in one of four modes:

Counter A	Counter B
• Pulse width measurement	• Retriggerable Interval Counter
• Pulse Generation	• Asymmetrical Pulse Generation
• Interval Timer	• Interval Timer
• Event Counter	• Event Counter

Operating modes of Counter A and Counter B are controlled by the Mode Control Register. All counting begins at the initialization value and decrements. When modes are selected requiring a counter input/output line, PA4 is automatically selected for Counter A and PA5 is automatically selected for Counter B (see Table 4).

COUNTER A

Counter A consists of a 16-bit counter and a 16-bit latch organized as follows: Lower Counter A (LCA), Upper Counter A (UCA), Lower Latch A (LLA), and Upper Latch A (ULA). The counter contains the count of either Ø2 clock pulses or external events, depending on the counter mode selected. The contents of Counter A may be read any time by executing a read at location 0019 for the Upper Counter A and at location 001A or location 0018 for the Lower Counter A. A read at location 0018 also clears the Counter A Underflow Flag (IFR4).

The 16-bit latch contains the counter initialization value, and can be loaded at any time by executing a write to the Upper Latch A at location 0019 and the Lower Latch A at location 0018. In either case, the contents of the accumulator are copied into the applicable latch register.

Counter A can be started at any time by writing to address: 001A. The contents of the accumulator will be copied into the Upper Latch A before the contents of the 16-bit latch are transferred to Counter A. Counter A is set to the latch value whenever Counter A underflows. When Counter A decrements from 0000 the next counter value will be the latch value, not FFFF, and the Counter A Underflow Flag (1FR 4) will be set to "1". This bit may be cleared by reading the Lower Counter A at location 0018, by writing to address location 001A, or by $\overline{RES}$.

Counter A operates in any of four modes. These modes are selected by the Counter A Mode Select bits in the Mode Control Register.

MCR1 (bit 1)	MCR0 (bit 0)	Mode
0	0	Interval Timer
0	1	Pulse Generation
1	0	Event Counter
1	1	Pulse Width Measurement

The Interval Timer, Pulse Generation, and Pulse Width Measurement Modes are Ø2 clock counter modes. The Event Counter Mode counts the occurrences of an external event on the CNTR line.

The Counter is set to the Interval Timer Mode (00) when a $\overline{RES}$ signal is generated.

INTERVAL TIMER

In the Interval Timer mode the Counter is initialized to the Latch value by either of two conditions:

1. When the Counter is decremented from 0000, the next Counter value is the Latch value (not FFFF).

2. When a write operation is performed to the Load Upper Latch and Transfer Latch to Counter address 001A, the Counter is loaded with the Latch value. Note that the contents of the Accumulator are loaded into the Upper Latch before the Latch value is transferred to the Counter.

The Counter value is decremented by one count at the Ø2 clock rate. The 16-bit Counter can hold from 1 to 65535 counts. The Counter Timer capacity is therefore 1 μs to 65.535 ms at the 1 MHz Ø2 clock rate or 0.5 μs to 32.7675 ms at the 2 MHz Ø2 clock rate. Time intervals greater than the maximum Counter value can be easily measured by counting $\overline{IRQ}$ interrupt requests in the counter $\overline{IRQ}$ interrupt routine.

When Counter A decrements from 0000, the Counter A Underflow (IFR4) is set to logic 1. If the Counter A Interrupt Enable Bit (IER4) is also set, an $\overline{IRQ}$ interrupt request will be generated. The Counter A Underflow bit in the Interrupt Flag Register can be examined in the $\overline{IRQ}$ interrupt routine to determine that the $\overline{IRQ}$ was generated by the Counter A Underflow.

While the timer is operating in the Interval Timer Mode, PA4 operates as a PA I/O bit.

A timing diagram of the Interval Timer mode is shown in Figure 14.

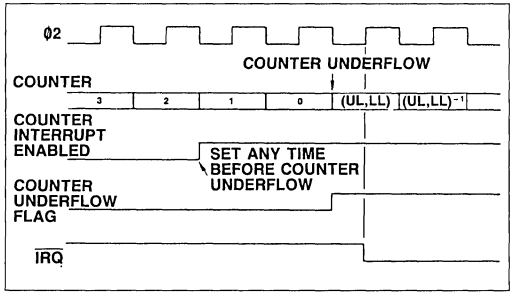


Figure 14. Interval Timer Timing Diagram

PULSE GENERATION MODE

In the Pulse Generation mode, the CA line operates as a Counter Output. The line toggles from low to high or from high to low whenever a Counter A Underflow occurs, or a write is performed to address 001A.

The normal output wave form is a symmetrical square-wave. The CA output is initialized high when entering the mode and transitions low when writing to 001A.

Asymmetric waveforms can be generated if the value of the latch is changed after each counter underflow.

A one-shot waveform can be generated by changing from Pulse Generation to Interval Timer mode after only one occurrence of the output toggle condition.

EVENT COUNTER MODE

In this mode the CA is used as an Event Input line, and the Counter will decrement with each rising edge detected on this line. The maximum rate at which this edge can be detected is one-half the Ø2 clock rate (Figure 15).

The Counter can count up to 65,535 occurrences before underflowing. As in the other modes, the Counter A Underflow bit (IER4) is set to logic 1 if the underflow occurs.

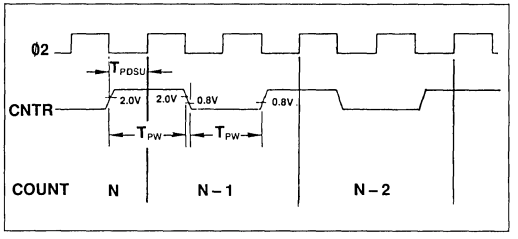


Figure 15. Event Counter Mode Timing

PULSE WIDTH MEASUREMENT MODE

This mode allows the accurate measurement of a low pulse duration on the CA line. The Counter decrements by one count at the Ø2 clock rate as long as the CA line is held in the low state. The Counter is stopped when CA is in the high state.

The Counter A underflow flag will be set only when the count in the timer reaches zero. Upon reaching zero the timer will be loaded with the latch value and continue counting down as long as the CA pin is held low. After the counter is stopped by a high level on CA, the count will hold as long as CA remains high. Any further low levels on CA will again cause the counter to count down from its present value. The state of the CA line can be determined by testing the state of PA4 (Figure 16).

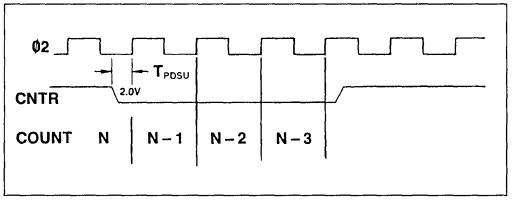


Figure 16. Pulse Width Measurement Timing

SERIAL I/O DATA RATE GENERATION

Counter A also provdes clock timing for the Serial I/O which establishes the data rate for the Serial I/O port. When the Serial I/O is enabled, Counter A is forced to operate at the internal clock rate. Counter A is not required for the RCVR S/R mode. The Counter I/O (PA4) may also be required to support the Serial I/O (see Table 4).

Table 6 identifies the values to be loaded in Counter A for selecting standard data rates with a Ø2 clock rate of 1 MHz and 2 MHz. Although Table 6 identifies only the more common data rates, any data rate from 1 to 62.5K bps can be selected by using the formula:

$$N = \frac{Ø2}{16 \times bps} - 1$$

where

N = decimal value to be loaded into Counter A using its hexadecimal equivalent
Ø2 = the clock frequency (1 MHz or 2 MHz)
bps = the desired data rate.

NOTE

In Table 6 you will notice that the standard data rate and the actual data rate may be slightly different. Transmitter and receiver errors of 1.5% or less are acceptable. A revised clock rate is included in Table 6 for those baud rates which fall outside this limit.

Table 6. Counter A Values for Baud Rate Selection

Standard Baud Rate	Hexadecimal Value		Actual Baud Rate At		Clock Rate Needed to Get Standard Baud Rate	
	1 MHz	2 MHz	1 MHz	2 MHz	1 MHz	2 MHz
50	04E1	09C3	50.00	50.00	1.0000	2.0000
75	0340	0682	75.03	74.99	1.0000	2.0000
110	0237	046F	110.04	110.04	1.0000	2.0000
150	01A0	0340	149.88	150.06	1.0000	2.0000
300	00CF	01A0	300.48	299.76	1.0000	2.0000
600	0067	00CF	600.96	600.96	1.0000	2.0000
1200	0033	0067	1201.92	1201.92	1.0000	2.0000
2400	0019	0033	2403.85	2403.85	1.0000	2.0000
3600	0010	0021	3676.47	3676.47	0.9792	1.9584
4800	000C	0019	4807.69	4807.69	1.0000	2.0000
7200	0008	0010	6944.44	7352.94	1.0368	1.9584
9600	0006	000C	8928.57	9615.38	1.0752	2.0000

COUNTER B

Counter B consists of a 16-bit counter and two 16-bit latches organized as follows: Lower Counter B (LCB), Upper Counter B (UCB), Lower Latch B (LLB), Upper Latch B (ULB), Lower Latch C (LLC), and Upper Latch C (ULC). Latch C is used only in the asymmetrical pulse generation mode. The counter contains the count of either ∅2 clock pulses or external events depending on the counter mode selected. The contents of Counter B may be read any time by executing a read at location 001D for the Upper Counter B and at location 001E or 001C for the Lower Counter B. A read at location 001C also clears the Counter B Underflow Flag.

Latch B contains the counter initialization value, and can be loaded at any time by executing a write to the Upper Latch B at location 001D and the Lower Latch B at location 001C. In each case, the contents of the accumulator are copied into the applicable latch register.

Counter B can be initialized at any time by writing to address: 001E. The contents of the accumulator is copied into the Upper Latch B before the value in the 16-bit Latch B is transferred to Counter B. Counter B will also be set to the latch value and the Counter B Underflow Flag bit (IFR5) will be set to a "1" whenever Counter B underflows by decrementing from 0000.

IFR 5 may be cleared by reading the Lower Counter B at location 001C, by writing to address location 001E, or by $\overline{RES}$.

Counter B operates in the same manner as Counter A in the Interval Timer and Event Counter modes. The Pulse Width Measurement Mode is replaced by the Retriggerable Interval Timer Mode and the Pulse Generation mode is replaced by the Asymmetrical Pulse Generation Mode.

RETRIGGERABLE INTERVAL TIMER MODE

When operating in the Retriggerable Interval Timer mode, Counter B is initialized to the latch value by writing to address 001E, by a Counter B underflow, or whenever a positive edge occurs on the CB pin (PA5). The Counter B interrupt flag will be set if the counter underflows before a positive edge occurs on the CB line. Figure 17 illustrates the operation of this timer mode.

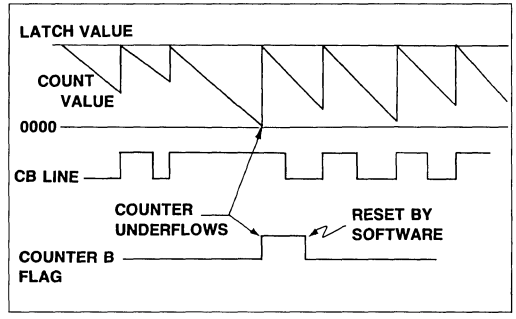


Figure 17. Counter B Retriggerable Interval Timer Mode

ASYMMETRICAL PULSE GENERATION MODE

Counter B has a special Asymmetrical Pulse Generation Mode whereby a pulse train with programmable pulse width and period can be generated without the processor intervention once the latch values are initialized.

In this mode, the 16-bit Latch B is initialized with a value which corresponds to the duration between pulses (referred to as D in the following descriptions). The 16-bit Latch C is initialized with a value which corresponds to the desired pulse width (referred to as P in the following descriptions). The initialization sequence for Latch B and C and the starting of a counting sequence are as follows:

1. The lower 8 bits of P are loaded into LLB by writing to address 001C, and the upper 8 bits of P are loaded into ULB and the full 16 bits are transferred to Latch C by writing to address location 001D. At this point both Latch B and Latch C contain the value of P.
2. The lower 8 bits of D are loaded into LLB by writing to address 001C, and the upper 8 bits of D are loaded into ULB by writing to address location 001E. Writing to address location 001E also causes the contents of the 16-bit Latch B to be downloaded into the Counter B and causes the CB output to go low as shown in Figure 18.
3. When the Counter B underflow occurs the contents of the Latch C is loaded into the Counter B, and the CB output toggles to a high level and stays high until another underflow occurs. Latch B is then down-loaded and the CB output toggles to a low level repeating the whole process.

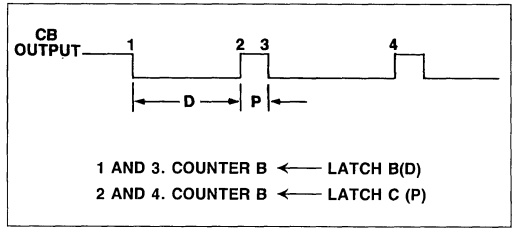


Figure 18. Counter B Pulse Generation

POWER-ON/INITIALIZATION CONSIDERATIONS

POWER-ON TIMING

After applications of V_{CC} and V_{RR} power to the device, $\overline{RES}$ must be held low for at least eight Ø2 clock cycles after V_{CC} reaches operating range and the internal oscillator has stabilized. This stabilization time is dependent upon the input V_{CC} voltage and performance of the internal oscillator. The clock can be monitored at Ø2 (pin 3). Figure 19 illustrates the power turn-on waveforms. Clock stabilization time is typically 20 ms.

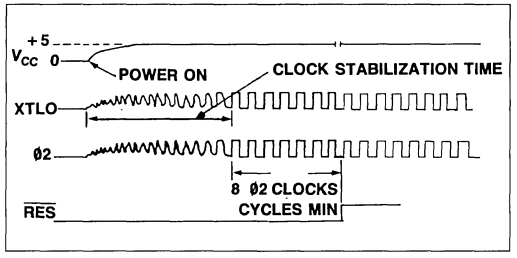


Figure 19. Power Turn-on Timing Detail

POWER-ON RESET

The occurrence of $\overline{RES}$ going from low to high will cause the device to set the Interrupt Mask Bit — bit 2 of the Processor Status Register. Both I/O ports (PA, PB) will be forced to the high (logic 1) state. An internal initialization sequence lasting 16 clock cycles is then performed which sets bits 5–7 of the Mode Control Register to logic 1, thus enabling external user memory (Multiplexed Bus Mode). The remaining bits of the Control Register will be cleared to logic 0 causing the Interval Timers counter mode (mode 00) to be selected and causing all interrupt enabled bits to be reset.

RESET ($\overline{RES}$) CONDITIONING

When $\overline{RES}$ is driven from low to high the device is put in a reset state causing the registers and I/O ports to be configured as shown in Table 7.

Table 7. $\overline{RES}$ Initialization of I/O Ports and Registers

	7	6	5	4	3	2	1	0
Registers								
Processor Status	—	—	—	—	0	1	—	—
Mode Control (MCR)	1	1	1	0	0	0	0	0
Int. Enable (IER)	0	0	0	0	0	0	0	0
Int. Flag (IFR)	0	0	0	0	0	0	0	0
Ser. Com. Control (SCCR)	0	0	0	0	0	0	0	0
Ser. Com. Status (SCSR)	0	1	0	0	0	0	0	0
Ports								
PA Latch	1	1	1	1	1	1	1	1
PB Latch	1	1	1	1	1	1	1	1

All RAM and other CPU registers will initialize in a random, non-repeatable data pattern.

INITIALIZATION

Any initialization process for the device should include a $\overline{RES}$, as indicated in the preceding paragraphs. After stabilization of the internal clock (if a power-on situation) an initialization subroutine should be executed to perform (as a minimum) the following functions:

1. The Stack Pointer should be set
2. Clear or Set Decimal Mode
3. Set or Clear Carry Flag
4. Set up Mode Controls as required
5. Clear Interrupts

A typical initialization subroutine could be as follows:

```
LDX     Load stack pointer starting address into X Register
TXS     Transfer X Register value to Stack Pointer
CLD     Clear Decimal Mode
SEC     Set Carry Flag
. . . .  Set-up Mode Control and
. . . .  special function
. . . .  registers as required
CLI     Clear Interrupts
```

ENHANCED R6502 INSTRUCTION SET

The following table contains a summary of the R6502 instruction set. For detailed information, consult the R6502 Microcomputer System Programming Manual, Order No. 202. The four instructions notated with a * are added instructions to enhance the standard 6502 instruction set.

Instruction Set In Alphabetic Sequence

Mnemonic	Description	Mnemonic	Description
ADC	Add Memory to Accumulator with Carry	LDA	Load Accumulator with Memory
AND	"AND" Memory with Accumulator	LDX	Load Index X with Memory
ASL	Shift Left One Bit (Memory or Accumulator)	LDY	Load Index Y with Memory
		LSR	Shift One Bit Right (Memory or (Accumulator)
*BBR	Branch on Bit Reset Relative		
*BBS	Branch on Bit Set Relative		
BCC	Branch on Carry Clear	NOP	No Operation
BCS	Branch on Carry Set		
BEQ	Branch on Result Zero	ORA	"OR" Memory with Accumulator
BIT	Test Bits in Memory with Accumulator		
BMI	Branch on Result Minus	PHA	Push Accumulator on Stack
BNE	Branch on Result not Zero	PHP	Push Processor Status on Stack
BPL	Branch on Result Plus	PLA	Pull Accumulator from Stack
BRK	Force Break	PLP	Pull Processor Status from Stack
BVC	Branch on Overflow Clear		
BVS	Branch on Overflow Set	*RMB	Reset Memory Bit
		ROL	Rotate One Bit Left (Memory or Accumulator)
CLC	Clear Carry Flag	ROR	Rotate One Bit Right (Memory or Accumulator)
CLD	Clear Decimal Mode	RTI	Return from Interrupt
CLI	Clear Interrupt Disable Bit	RTS	Return from Subroutine
CLV	Clear Overflow Flag		
CMP	Compare Memory and Accumulator		
CPX	Compare Memory and Index X		
CPY	Compare Memory and Index Y	SBC	Subtract Memory from Accumulator with Borrow
		SEC	Set Carry Flag
DEC	Decrement Memory by One	SED	Set Decimal Mode
DEX	Decrement Index X by One	SEI	Set Interrupt Disable Status
DEY	Decrement Index Y by One	*SMB	Set Memory Bit
		STA	Store Accumulator in Memory
		STX	Store Index X in Memory
EOR	"Exclusive-Or" Memory with Accumulator	STY	Store Index Y in Memory
INC	Increment Memory by One		
INX	Increment Index X by One	TAX	Transfer Accumulator to Index X
INY	Increment Index Y by One	TAY	Transfer Accumulator to Index Y
		TSX	Transfer Stack Pointer to Index X
		TXA	Transfer Index X to Accumulator
JMP	Jump to New Location	TXS	Transfer Index X to Stack Register
JSR	Jump to New Location Saving Return Address	TYA	Transfer Index Y to Accumulator

INSTRUCTIONS

MNEMONIC	OPERATION	IMMEDIATE OP	n	#	ABSOLUTE OP	n	#	ZERO PAGE OP	n	#	ACCUM. OP	n	#	IMPLIED OP	n	#
ADC	A · M · C→A (4)(1)	69	2	2	6D	4	3	65	3	2						
AND	A M→A (1)	29	2	2	2D	4	3	25	3	2						
ASL	C← [7 0] ←0				0E	6	3	06	5	2	0A	2	1			
BBR[#(0-7)]	Branch on $M_b = 0$ (5)(2)															
BBS[#(0-7)]	Branch on $M_b = 1$ (5)(2)															
BCC	Branch on C = 0 (2)															
BCS	Branch on C = 1 (2)															
BEQ	Branch on Z = 1 (2)															
BIT	A∧M				2C	4	3	24	3	2						
BMI	Branch on N = 1 (2)															
BNE	Branch on Z = 0 (2)															
BPL	Branch on N = 0 (2)															
BRK	Break													00	7	1
BVC	Branch on V = 0 (2)															
BVS	Branch on V = 1 (2)															
CLC	0→C													18	2	1
CLD	0→D													D8	2	1
CLI	0→I													58	2	1
CLV	0→V													B8	2	1
CMP	A M (1)	C9	2	2	CD	4	3	C5	3	2						
CPX	X M	E0	2	2	EC	4	3	E4	3	2						
CPY	Y M	C0	2	2	CC	4	3	C4	3	2						
DEC	M 1→M				CE	6	3	C6	5	2						
DEX	X 1→X													CA	2	1
DEY	Y 1→Y													88	2	1
EOR	A∀M→A (1)	49	2	2	4D	4	3	45	3	2						
INC	M · 1→M				EE	6	3	E6								
INX	X · 1→X													EB	2	1
INY	Y · 1→Y													C8	2	1
JMP	Jump to New Loc				4C	3	3									
JSR	Jump Sub				20	6	3									
LDA	M→A (1)	A9	2	2	AD	4	3	A5	3	2						
LDX	M→X (1)	A2	2	2	AE	4	3	A6	3	2						
LDY	M→Y (1)	A0	2	2	AC	4	3	A4	3	2						
LSR	0→ [7 0] → C				4E	6	3	46	5	2	4A	2	1			
NOP	No Operation													EA	2	1
ORA	AVM→A (1)	09	2	2	0D	4	3	05	3	2						
PHA	A→Ms S 1→S													48	3	1
PHP	P→Ms S 1→S													08	3	1
PLA	S · 1→S Ms→A													68	4	1
PLP	S · 1→S Ms→P													28	4	1
RMB[#(0-7)]	0→M_b (5)															
ROL	←[7 0]←[C]←				2E	6	3	26	5	2	2A	2	1			
ROR	→[C]→[7 0]→				6E	6	3	66	5	2	6A	2	1			
RTI	Rtrn Int													40	6	1
RTS	Rtrn Sub													60	6	1
SBC	A - M - C→A (1)	E9	2	2	ED	4	3	E5	3	2						
SEC	1→C													38	2	1
SED	1→D													F8	2	1
SEI	1→T													78	2	1
SMB[#(0-7)]	1→M_b (5)															
STA	A→M				8D	4	3	85	3	2						
STX	X→M				8E	4	3	86	3	2						
STY	Y→M				8C	4	3	84	3	2						
TAX	A→X													AA	2	1
TAY	A→Y													A8	2	1
TSX	S→X													BA	2	1
TXA	X→A													8A	2	1
TXS	X→S													9A	2	1
TYA	Y→A													98	2	1

MNEMONIC	(IND, X) OP	n	#	(IND), Y OP	n	#	Z. PAGE, X OP	n	#	ABS, X OP	n	#	ABS, Y OP	n	#	RELATIVE OP	n	#	INDIRECT OP	n	#	Z. PAGE, Y OP	n	#
ADC	61	6	2	71	5	2	75	4	2	7D	4	3	79	4	3									
AND	21	6	2	31	5	2	35	4	2	3D	4	3	39	4	3									
ASL							16	6	2	1E	7	3												
BBR[#(0-7)]																								
BBS[#(0-7)]																								
BCC																90	2	2						
BCS																B0	2	2						
BEQ																F0	2	2						
BIT																								
BMI																30	2	2						
BNE																D0	2	2						
BPL																10	2	2						
BRK																								
BVC																50	2	2						
BVS																70	2	2						
CLC																								
CLD																								
CLI																								
CLV																								
CMP	C1	6	2	D1	5	2	D5	4	2	DD	4	3	D9	4	3									
CPX																								
CPY																								
DEC							D6	6	2	DE	7	3												
DEX																								
DEY																								
EOR	41	6	2	51	5	2	55	4	2	5D	4	3	59	4	3									
INC							F6	6	2	FE	7	3												
INX																								
INY																								
JMP																			6C	5	3			
JSR																								
LDA	A1	6	2	B1	5	2	B5	4	2	BD	4	3	B9	4	3									
LDX													BE	4	3							B6	4	2
LDY							B4	4	2	BC	4	3												
LSR							56	6	2	5E	7	3												
NOP																								
ORA	01	6	2	11	5	2	15	4	2	1D	4	3	19	4	3									
PHA																								
PHP																								
PLA																								
PLP																								
RMB[#(0-7)]																								
ROL							36	6	2	3E	7	3												
ROR							76	6	2	7E	7	3												
RTI																								
RTS																								
SBC	E1	6	2	F1	5	2	F5	4	2	FD	4	3	F9	4	3									
SEC																								
SED																								
SEI																								
SMB[#(0-7)]																								
STA	81	6	2	91	6	2	95	4	2	9D	5	3	99	5	3									
STX																						96	4	2
STY							94	4	2															
TAX																								
TAY																								
TSX																								
TXA																								
TXS																								
TYA																								

MNEMONIC	BIT ADDRESSING (OP BY BIT #) 0	1	2	3	4	5	6	7	PROCESSOR STATUS CODES 7 N	6 V	5 •	4 B	3 D	2 I	1 Z	0 C
ADC									N	V	•	•	•	•	Z	C
AND									N	•	•	•	•	•	Z	•
ASL									N	•	•	•	•	•	Z	C
BBR[#(0-7)]	0F	1F	2F	3F	4F	5F	6F	7F	•	•	•	•	•	•	•	•
BBS[#(0-7)]	8F	9F	AF	BF	CF	DF	EF	FF	•	•	•	•	•	•	•	•
BCC									•	•	•	•	•	•	•	•
BCS									•	•	•	•	•	•	•	•
BEQ									•	•	•	•	•	•	•	•
BIT									M	M_6	•	•	•	•	Z	•
BMI									•	•	•	•	•	•	•	•
BNE									•	•	•	•	•	•	•	•
BPL									•	•	•	•	•	•	•	•
BRK									•	•	•	1	•	1	•	•
BVC									•	•	•	•	•	•	•	•
BVS									•	•	•	•	•	•	•	•
CLC									•	•	•	•	•	•	•	0
CLD									•	•	•	•	0	•	•	•
CLI									•	•	•	•	•	0	•	•
CLV									•	0	•	•	•	•	•	•
CMP									N	•	•	•	•	•	Z	C
CPX									N	•	•	•	•	•	Z	C
CPY									N	•	•	•	•	•	Z	C
DEC									N	•	•	•	•	•	Z	•
DEX									N	•	•	•	•	•	Z	•
DEY									N	•	•	•	•	•	Z	•
EOR									N	•	•	•	•	•	Z	•
INC									N	•	•	•	•	•	Z	•
INX									N	•	•	•	•	•	Z	•
INY									N	•	•	•	•	•	Z	•
JMP									•	•	•	•	•	•	•	•
JSR									•	•	•	•	•	•	•	•
LDA									N	•	•	•	•	•	Z	•
LDX									N	•	•	•	•	•	Z	•
LDY									N	•	•	•	•	•	Z	•
LSR									0	•	•	•	•	•	Z	C
NOP									•	•	•	•	•	•	•	•
ORA									N	•	•	•	•	•	Z	•
PHA									•	•	•	•	•	•	•	•
PHP									•	•	•	•	•	•	•	•
PLA									N	•	•	•	•	•	Z	•
PLP									(Restored)							
RMB[#(0-7)]	07	17	27	37	47	57	67	77	•	•	•	•	•	•	•	•
ROL									N	•	•	•	•	•	Z	C
ROR									N	•	•	•	•	•	Z	C
RTI									(Restored)							
RTS									•	•	•	•	•	•	•	•
SBC									N	V	•	•	•	•	Z	(3)
SEC									•	•	•	•	•	•	•	1
SED									•	•	•	•	1	•	•	•
SEI									•	•	•	•	•	1	•	•
SMB[#(0-7)]	87	97	A7	B7	C7	D7	E7	F7	•	•	•	•	•	•	•	•
STA									•	•	•	•	•	•	•	•
STX									•	•	•	•	•	•	•	•
STY									•	•	•	•	•	•	•	•
TAX									N	•	•	•	•	•	Z	•
TAY									N	•	•	•	•	•	Z	•
TSX									N	•	•	•	•	•	Z	•
TXA									N	•	•	•	•	•	Z	•
TXS									•	•	•	•	•	•	•	•
TYA									N	•	•	•	•	•	Z	•

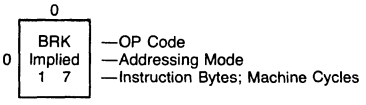
NOTES

1. Add 1 to N if page boundary is crossed
2. Add 1 to N if branch occurs to same page
   Add 2 to N if branch occurs to different page
3. Carry not = Borrow
4. If in decimal mode Z flag is invalid
   accumulator must be checked on zero result.
5. Effects 8-bit data field of the specified zero page address.

LEGEND

- X = Index X
- Y = Index Y
- A = Accumulator
- M = Memory per effective address
- M_s = Memory per stack pointer
- M_b = Selecter zero page memory bit
- M_7 = Memory Bit 7
- M_6 = Memory Bit 6
- • = Add
- – = Subtract
- ∧ = And
- V = Or
- ∀ = Exclusive Or
- n = Number of cycles
- # = Number of Bytes

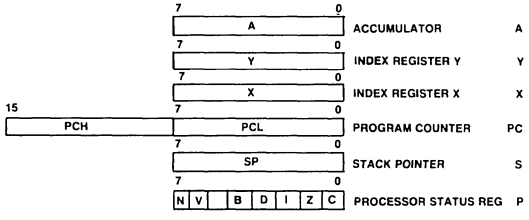
INSTRUCTION CODE MATRIX



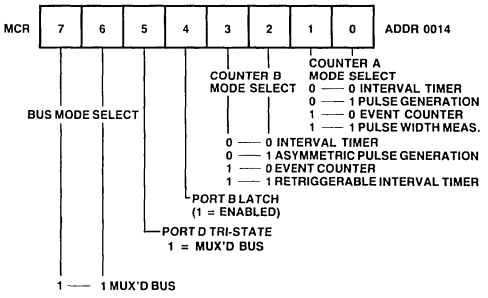
MSD \ LSD	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	MSD
0	BRK Implied 1 7	ORA (IND, X) 2 6				ORA ZP 2 3	ASL ZP 2 5	RMB0 ZP 2 5	PHP Implied 1 3	ORA IMM 2 2	ASL Accum 1 2			ORA ABS 3 4	ASL ABS 3 6	BBR0 ZP 3 5**	0
1	BPL Relative 2 2**	ORA (IND), Y 2 5*				ORA ZP, X 2 4	ASL ZP, X 2 6	RMB1 ZP 2 5	CLC Implied 1 2	ORA ABS, Y 3 4*				ORA ABS, X 3 4*	ASL ABS, X 3 7	BBR1 ZP 3 5**	1
2	JSR Absolute 3 6	AND (IND, X) 2 6			BIT ZP 2 3	AND ZP 2 3	ROL ZP 2 5	RMB2 ZP 2 5	PLP Implied 1 4	AND IMM 2 2	ROL Accum 1 2		BIT ABS 3 4	AND ABS 3 4	ROL ABS 3 6	BBR2 ZP 3 5**	2
3	BMI Relative 2 2**	AND (IND, Y) 2 5*				AND ZP, X 2 4	ROL ZP, X 2 6	RMB3 ZP 2 5	SEC Implied 1 2	AND ABS, Y 3 4*				AND ABS, X 3 4*	ROL ABS, X 3 7	BBR3 ZP 3 5**	3
4	RTI Implied 1 6	EOR (IND, X) 2 6				EOR ZP 2 3	LSR ZP 2 5	RMB4 ZP 2 5	PHA Implied 1 3	EOR IMM 2 2	LSR Accum 1 2		JMP ABS 3 3	EOR ABS 3 4	LSR ABS 3 6	BBR4 ZP 3 5**	4
5	BVC Relative 2 2**	EOR (IND), Y 2 5*				EOR ZP, X 2 4	LSR ZP, X 2 6	RMB5 ZP 2 5	CLI Implied 1 2	EOR ABS, Y 3 4*				EOR ABS, X 3 4*	LSR ABS, X 3 7	BBR5 ZP 3 5**	5
6	RTS Implied 1 6	ADC (IND, X) 2 6				ADC ZP 2 3	ROR ZP 2 5	RMB6 ZP 2 5	PLA Implied 1 4	ADC IMM 2 2	ROR Accum 1 2		JMP Indirect 3 5	ADC ABS 3 4	ROR ABS 3 6	BBR6 ZP 3 5**	6
7	BVS Relative 2 2**	ADC (IND, Y) 2 5*				ADC ZP, X 2 4	ROR ZP, X 2 6	RMB7 ZP 2 5	SEI Implied 1 2	ADC ABS, Y 3 4*				ADC ABS, X 3 4*	ROR ABS, X 3 7	BBR7 ZP 3 5**	7
8		STA (IND, X) 2 6			STY ZP 2 3	STA ZP 2 3	STX ZP 2 3	SMB0 ZP 2 5	DEY Implied 1 2		TXA Implied 1 2		STY ABS 3 4	STA ABS 3 4	STX ABS 3 4	BBS0 ZP 3 5**	8
9	BCC Relative 2 2**	STA (IND, Y) 2 6			STY ZP, X 2 4	STA ZP, X 2 4	STX ZP, Y 2 4	SMB1 ZP 2 5	TYA Implied 1 2	STA ABS, Y 3 5	TXS Implied 1 2			STA ABS, X 3 5		BBS1 ZP 3 5**	9
A	LDY IMM 2 2	LDA (IND, X) 2 6	LDX IMM 2 2		LDY ZP 2 3	LDA ZP 2 3	LDX ZP 2 3	SMB2 ZP 2 5	TAY Implied 1 2	LDA IMM 2 2	TAX Implied 1 2		LDY ABS 3 4	LDA ABS 3 4	LDX ABS 3 4	BBS2 ZP 3 5**	A
B	BCS Relative 2 2**	LDA (IND), Y 2 5*			LDY ZP, X 2 4	LDA ZP, X 2 4	LDX ZP, Y 2 4	SMB3 ZP 2 5	CLV Implied 1 2	LDA ABS, Y 3 4*	TSX Implied 1 2		LDY ABS, X 3 4*	LDA ABS, X 3 4*	LDX ABS, Y 3 4*	BBS3 ZP 3 5**	B
C	CPY IMM 2 2	CMP (IND, X) 2 6			CPY ZP 2 3	CMP ZP 2 3	DEC ZP 2 5	SMB4 ZP 2 5	INY Implied 1 2	CMP IMM 2 2	DEX Implied 1 2		CPY ABS 3 4	CMP ABS 3 4	DEC ABS 3 6	BBS4 ZP 3 5**	C
D	BNE Relative 2 2**	CMP (IND), Y 2 5*				CMP ZP, X 2 4	DEC ZP, X 2 6	SMB5 ZP 2 5	CLD Implied 1 2	CMP ABS, Y 3 4*				CMP ABS, X 3 4*	DEC ABS, X 3 7	BBS5 ZP 3 5**	D
E	CPX IMM 2 2	SBC (IND, X) 2 6			CPX ZP 2 3	SBC ZP 2 3	INC ZP 2 5	SMB6 ZP 2 5	INX Implied 1 2	SBC IMM 2 2	NOP Implied 1 2		CPX ABS 3 4	SBC ABS 3 4	INC ABS 3 6	BBS6 ZP 3 5**	E
F	BEQ Relative 2 2**	SBC (IND), Y 2 5*				SBC ZP, X 2 4	INC ZP, X 2 6	SMB7 ZP 2 5	SED Implied 1 2	SBC ABS, Y 3 4*				SBC ABS, X 3 4*	INC ABS, X 3 7	BBS7 ZP 3 5**	F
	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	

*Add 1 to N if page boundary is crossed.
**Add 1 to N if branch occurs to same page;
add 2 to N if branch occurs to different page.

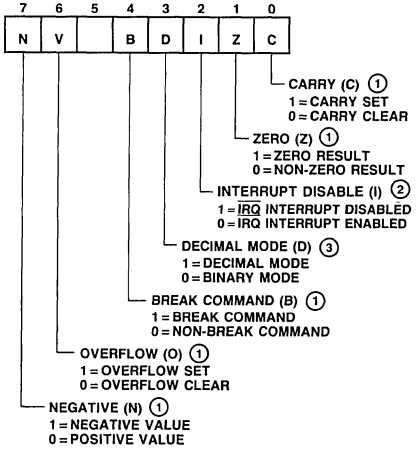
KEY REGISTER SUMMARY



CPU Registers



Mode Control Register



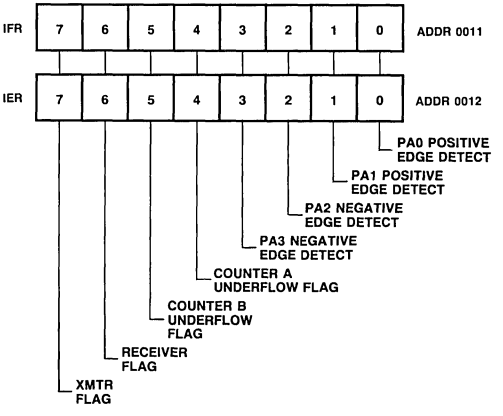
NOTES:

(1) NOT INITIALIZED BY $\overline{RES}$

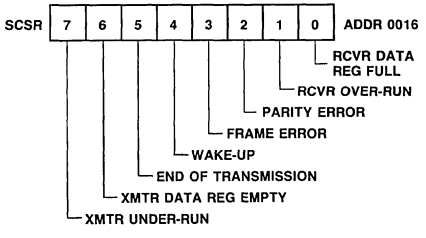
(3) SET TO LOGIC 1 BY $\overline{RES}$

(3) SET TO LOGIC 0 BY $\overline{RES}$

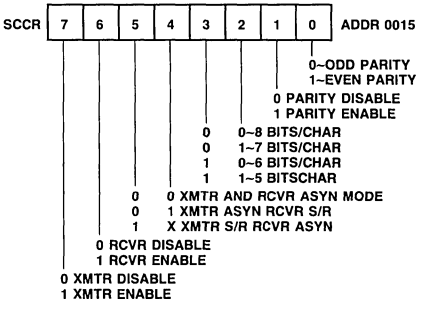
Processor Status Register



Interrupt Enable and Flag Registers



Serial Communications Status Register



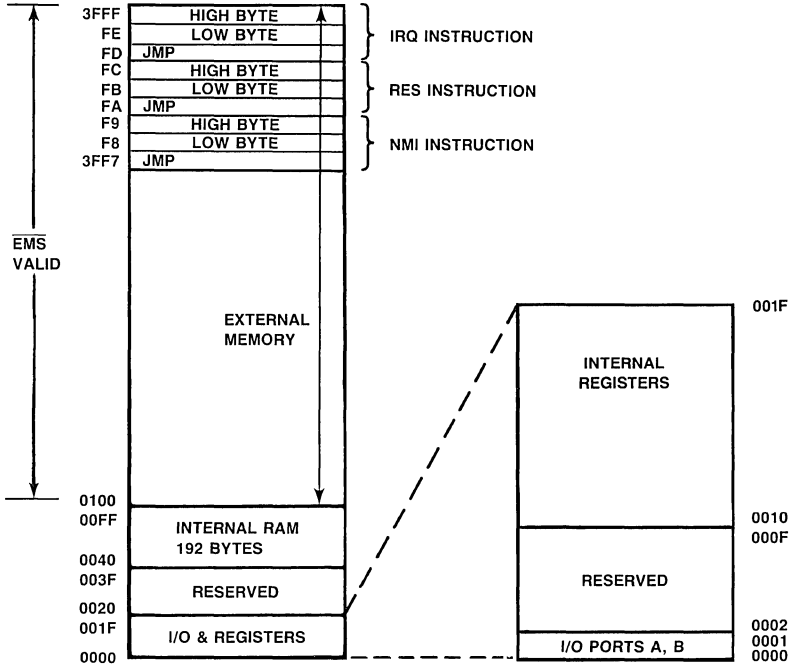
Serial Communications Control Register

ADDRESS ASSIGNMENTS AND MEMORY MAPS

I/O AND INTERNAL REGISTER ADDRESS

ADDRESS (HEX)	READ	WRITE
001F	—	—
1E	Lower Counter B	Upper Latch B, Cntr B ←Latch B, CLR Flag
1D	Upper Counter B	Upper Latch B, Latch C ←Latch B
1C	Lower Counter B, CLR Flag	Lower Latch B.
1B	—	—
1A	Lower Counter A	Upper Latch A, Cntr A ←Latch A, CLR Flag
19	Upper Counter A	Upper Latch A
18	Lower Counter A, CLR Flag	Lower Latch A
17	Serial Receiver Data Register	Serial Transmitter Data Register
16	Serial Comm. Status Register	Serial Comm. Status Reg. Bits 4 & 5 only
15	Serial Comm. Control Register	Serial Comm. Control Register
14	Mode Control Register	Mode Control Register
13	—	—
12	Interrupt Enable Register	Interrupt Enable Register
11	Interrupt Flag Register	—
0010	Read FF	Clear Int Flag (Bits 0–3 only, Write 0's only)
0F	—	—
0E	—	—
0D	—	—
0C	—	—
0B	—	—
0A	—	—
09	—	—
08	—	—
07	—	—
06	—	—
05	—	—
04	—	—
03	—	—
02	—	—
01	Port B	Port B
0000	Port A	Port A

MULTIPLEXED MODE MEMORY MAP



ELECTRICAL SPECIFICATIONS

MAXIMUM RATINGS*

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC} & V_{RR}	−0.3 to +7.0	Vdc
Input Voltage	V_{IN}	−0.3 to +7.0	Vdc
Operating Temperature Commercial	T_A	0 to +70	°C
Storage Temperature	T_{STG}	−55 to +150	°C

***NOTE:** Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in other sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

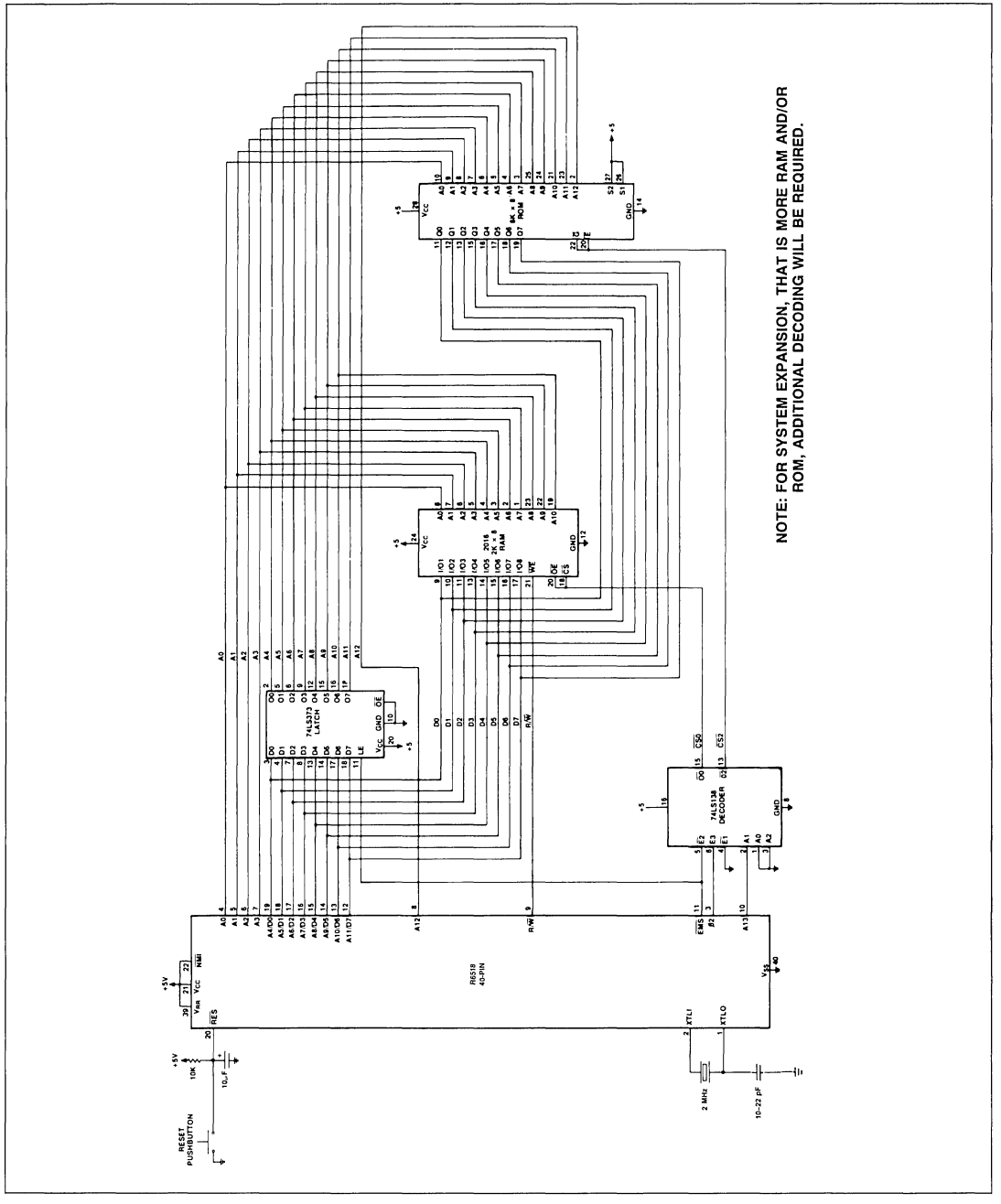
DC CHARACTERISTICS

(V_{CC} = 5V ±5%, V_{RR} = V_{CC}, V_{SS} = 0, T_A = 0 to 70°C except as noted)

Parameter	Symbol	Min	Typ.	Max.	Unit
Power Dissipation (Outputs High) Commercial @ 0°C	P_D	—		1000	mW
RAM Standby Voltage (Retention Mode)	V_{RR}	3.0	—	V_{CC}	Vdc
RAM Standby Current (Retention Mode) Commercial @ 25°C	I_{RR}	—	4	—	mAdc
Input High Voltage	V_{IH}	+2.0	—	V_{CC}	Vdc
Input High Voltage (XTLI)	V_{IH}	+4.0	—	V_{CC}	Vdc
Input Low Voltage	V_{IL}	−0.3	—	+0.8	Vdc
Input Leakage Current ($\overline{RES}$, $\overline{NMI}$) V_{in} = 0 to 5.0 Vdc	I_{IN}			±10.0	μAdc
Input Low Current PA, PB, and Address/Data (V_{IL} = 0.4 Vdc)	I_{IL}	—	−1.0	−1.6	mAdc
Output High Voltage (Except XTLO) (I_{LOAD} = 100 μAdc)	V_{OH}	+2.4	—	V_{CC}	Vdc
Output Low Voltage (I_{LOAD} = 1.6 mAdc)	V_{OL}	—	—	+0.4	Vdc
Input Capacitance (V_{in} = 0V, T_A = 25°C, f = 1.0 MHz)	C_{in}				pF
PA, PB		—	—	10	
XTLI, XTLO		—	—	50	
I/O Port Pull-Up Resistance A0–A3, D0–D7; $\overline{EMS}$, R/$\overline{W}$ PA0–PA7, PB0–PB7	R_L	3.0	6.0	11.5	KΩ
Output Capacitance V_{IN} = 0V, T_A = 25°C, f = 1.0 MHz	C_{OUT}	—	—	10	pF

Note: Negative sign indicates outward current flow, positive indicates inward flow.

TYPICAL MEMORY HOOKUP



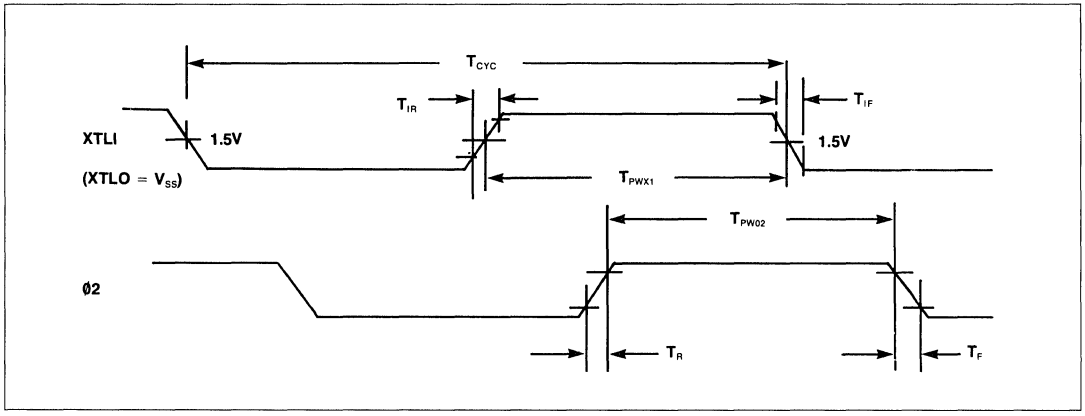
TIMING REQUIREMENTS AND CHARACTERISTICS

GENERAL NOTES

1. V_{CC} = 5V ±5%, 0°C ≤ TA ≤ 70°C
2. A valid V_{CC} – $\overline{RES}$ sequence is required before proper operation is achieved.
3. All timing reference levels are 0.8V and 2.0V, unless otherwise specified.
4. All time units are nanoseconds, unless otherwise specified.
5. All capacitive loading is 130 pF maximum, except for Ports A and B which are 50 pF maximum.

CLOCK TIMING

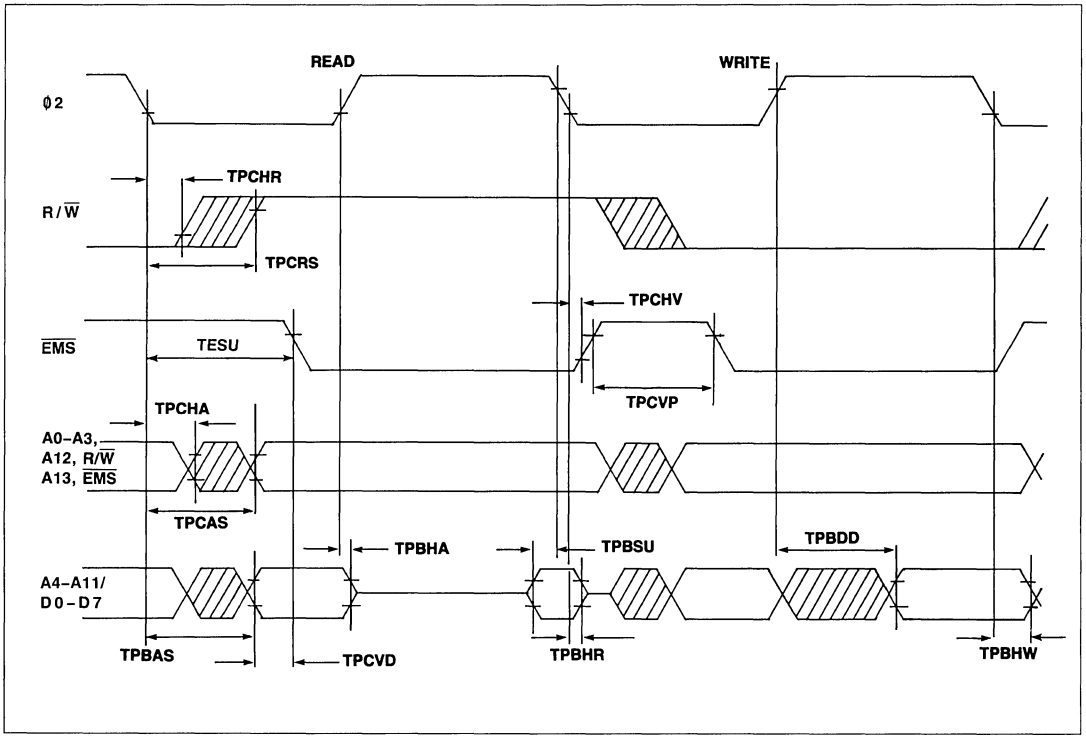
Symbol	Parameter	1 MHz		2 MHz		Unit
		Min	Max	Min	Max	
T_{CYC}	Cycle Time	1	10	0.5	10	μs
T_{PWX1}	XTLI Input Clock Pulse Width (XTLO = VSS)	500 ±25	—	250 ±10	—	ns
T_{PW02}	Output Clock Pulse Width at Minimum T_{CYC}	T_{PWX1} +0 −25	T_{PWX1}	T_{PWX1} +0 −20	T_{PWX1}	ns
T_R, T_F	Output Clock Rise Fall Time	—	25	—	15	ns
T_{IR}, T_{IF}	Input Clock Rise, Fall Time	—	10	—	10	ns



ADDRESS/DATA TIMING

Symbol	Parameter	1 MHz		2 MHz		Units
		Min	Max	Min	Max	
T_{PCRS}	R/W Setup Time	—	225	—	140	ns
T_{PCAS}	Address Setup Time	—	225	—	140	ns
T_{PBAS}	Address Setup Time	—	225	—	140	ns
T_{PBSU}	Data Setup Time	50	—	35	—	ns
T_{PBHR}	Data Read Hold Time	10	—	10	—	ns
T_{PBHW}	Data Write Hold Time	30	—	30	—	ns
T_{PBDD}	Data Output Delay	—	175	—	150	ns
T_{PCHA}	Address Hold Time	30	—	30	—	ns
T_{PBHA}	Address Hold Time	10	100	10	80	ns
T_{PCHR}	R/W Hold Time	30	—	30	—	ns
T_{PCHV}	$\overline{EMS}$ Hold Time	10	—	10	—	ns
T_{PCVD}(1)	Address to $\overline{EMS}$ Delay Time	30	—	30	—	ns
T_{PCVP}	$\overline{EMS}$ Stabilization Time	30	—	30	—	ns
T_{ESU}	$\overline{EMS}$ Setup Time	—	350	—	210	ns

Note 1: Values assume Address and $\overline{EMS}$ have the same capacitive load.

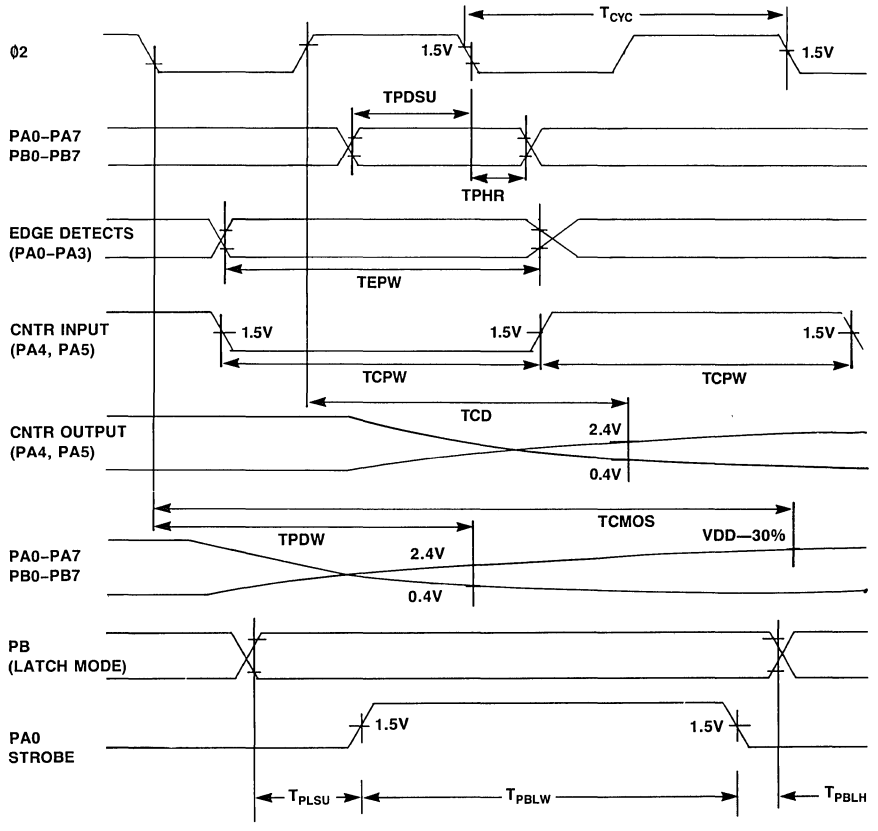


I/O, EDGE DETECT, COUNTERS, AND SERIAL I/O TIMING

Symbol	Parameter	1 MHz		2 MHz	
		Min	Max	Min	Max
	Internal Write to Peripheral Data Valid				
T_{PDW}(1)	PA, PB, TTL	—	500	—	500
T_{CMOS}(1)	PA, PB, CMOS	—	1000	—	1000
	Peripheral Data Setup Time				
T_{PDSU}	PA, PB	200	—	200	—
	Peripheral Data Hold Time				
T_{PHR}	PA, PB	75	—	75	—
T_{EPW}	PA0–PA3 Edge Detect Pulse Width	T_{CYC}	—	T_{CYC}	—
	Counters A and B				
T_{CPW}	PA4, PA5 Input Pulse Width	T_{CYC}	—	T_{CYC}	—
T_{CD}(1)	PA4, PA5 Output Delay	—	500	—	500
	Port B Latch Mode				
T_{PBLW}	PA0 Strobe Pulse Width	T_{CYC}	—	T_{CYC}	—
T_{PLSU}	PB Data Setup Time	175	—	150	—
T_{PBLH}	PB Data Hold Time	30	—	30	—
	Serial I/O				
T_{PDW}(1)	PA6 XMTR TTL	—	500	—	500
T_{CMOS}(1)	PA6 XMTR CMOS	—	1000	—	1000
T_{CPW}	PA4 RCVR S/R Clock Width	4 T_{CYC}	—	4 T_{CYC}	—
T_{PDW}(1)	PA4 XMTR Clock—S/R Mode (TTL)	—	500	—	500
T_{CMOS}(1)	PA4 XMTR Clock—S/R Mode (CMOS)	—	1000	—	1000

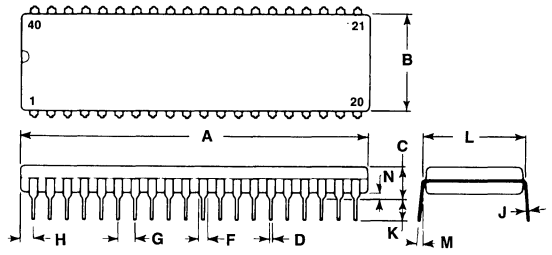
Notes: 1. Maximum load capacitance: 50 pF; passive pull-up required.
2. All times are in nanoseconds.

I/O, EDGE DETECT, COUNTER, AND SERIAL I/O TIMING



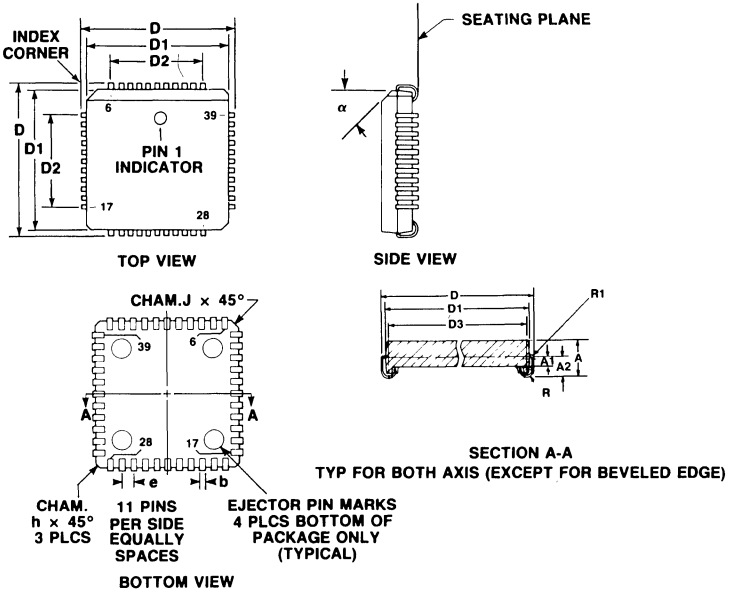
PACKAGE DIMENSIONS

40-PIN PLASTIC DIP



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	51.28	52.32	2.040	2.060
B	13 72	14.22	0.540	0.560
C	3.55	5.06	0 140	0 200
D	0.36	0.51	0.014	0 020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0 30	0.008	0 012
K	3.30	4.32	0.130	0.170
L	15.24 BSC		0.600 BSC	
M	7°	10°	7°	10°
N	0.51	1 02	0.020	0.040

44-PIN PLASTIC LEADED CHIP CARRIER (PLCC)



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4 14	4.39	0.163	0 173
A1	1 37	1.47	0 054	0 058
A2	2.31	2 46	0 091	0 097
b	0 457 TYP		0 018 TYP	
D	17 45	17 60	0 687	0 693
D1	16 46	16.56	0.648	0 652
D2	12 62	12 78	0 497	0 503
D3	15.75 REF		0.620 REF	
e	1 27 BSC		0 050 BSC	
h	1 15 TYP		0 045 TYP	
J	0.25 TYP		0 010 TYP	
α	45° TYP		45° TYP	
R	0 89 TYP		0.035 TYP	
R1	0 25 TYP		0 010 TYP	

Rockwell

R65F11 and R65F12 FORTH Based Microcomputers

SECTION 1 INTRODUCTION

1.1 FEATURES

- FORTH kernel in ROM
- Enhanced 6502 CPU
  - —Four new bit manipulation instructions:
    - Set Memory Bit (SMB)
    - Reset Memory Bit (RMB)
    - Branch on Bit Set (BBS)
    - Branch on Bit Reset (BBR)
  - —Decimal and binary arithmetic modes
  - —13 addressing modes
  - —True indexing
- 192-byte static RAM
- 16 bidirectional, TTL-compatible I/O lines (two ports, R65F11) or 40 bidirectional, TTL-compatible I/O lines (five ports, R65F12)
- One 8-bit port with programmable latched input
- Two 16-bit programmable counter/timers, with latches
  - —Pulse width measurement
  - —Asymmetrical pulse generation
  - —Pulse generation
  - —Interval timer
  - —Event counter
  - —Retriggerable interval timer
- Serial port
  - —Full-duplex asynchronous operation mode
  - —Selectable 5- to 8-bit characters
  - —Wake-up feature
  - —Synchronous shift register mode
  - —Standard programmable bit rates, programmable up to 62.5K bits/sec
- Ten interrupts
  - —Four edge-sensitive lines; two positive, two negative
  - —Reset
  - —Non-maskable
  - —Two counter
  - —Serial data received
  - —Serial data transmitted
- Expandable to 16K bytes of external memory
- Flexible clock circuitry
  - —2-MHz or 1-MHz internal operation
  - —Internal clock with external XTAL at two times internal frequency
  - —External clock input divided by one or two
- 1 μs minimum instruction execution time @ 2 MHz
- NMOS silicon gate, depletion load technology
- Single +5V power supply
- 12 mW standby power for 32 bytes of the 192-byte RAM
- 40-pin DIP (R65F11)
- 64-pin QUIP (R65F12) has three additional 8-bit I/O ports to provide a total of 40 I/O lines.

1.2 SUMMARY

The Rockwell R65F11 and R65F12 are complete, high-performance 8-bit NMOS single chip microcomputers, and are compatible with all members of the R6500 family.

The kernel of the high level Rockwell Single Chip RSC-FORTH language is contained in the preprogrammed ROM of the R65F11 and R65F12. RSC-FORTH is based on the popular fig-FORTH model with extensions. All of the run time functions of RSC-FORTH are contained in the ROM, including 16- and 32-bit mathematical, logical and stack manipulation, plus memory and input/output operators. The RSC-FORTH Operating System allows an external user program written in RSC-FORTH or Assembly Language to be executed from external EPROM, or development of such a program under the control of the R65FR1 RSC-FORTH Development ROM. Other development ROM's can also be accommodated.

The R65F11 and R65F12 consist of an enhanced 6502 CPU, an internal clock oscillator, 192 bytes of Random Access Memory (RAM) and versatile interface circuitry. The interface circuitry includes two 16-bit programmable timer/counters, 16 bidirectional input/output lines (including four edge-sensitive lines and input latching on one 8-bit port), a full-duplex serial I/O channel, ten interrupts and bus expandability.

The innovative architecture and the demonstrated high performance of the R6502 CPU, as well as instruction simplicity, results in system cost-effectiveness and a wide range of

computational power. These features in combination with the FORTH high level operating system make the R65F11 and R65F12 ideal for microcomputer applications.

For systems requiring additional I/O ports, the 64-pin QUIP version, the R65F12, provides three additional 8-bit ports.

A complete RSC-FORTH development system can be created with three MOS parts: the R65F11, one RAM chip and the R65FR1 Development ROM.

This product description is for the reader familiar with the R6502 CPU hardware and programming capabilities. A detailed description of the R6502 CPU hardware is included in the R6500 Microcomputer System Hardware Manual (Order Number 201). A description of the instruction capabilites of the R6502 CPU is contained in the R6500 Microcomputer System Programming Manual (Order Number 202).

1.3 ORDERING INFORMATION

Part No.	Description
R65F11P	40-Pin FORTH Based Microcomputer at 1 MHz
R65F11AP	40-Pin FORTH Based Microcomputer at 2 MHz
R65F12Q	64-Pin FORTH Based Microcomputer at 1 MHz
R65F12AQ	64-Pin FORTH Based Microcomputer at 2 MHz
R65FR1P	FORTH Development ROM for R65F11 or R65F12
R65FR2P	FORTH Development ROM for expanded capacity
R65FK2P	FORTH Kernel ROM for expanded capacity development
R65FR3P	FORTH Development ROM for R6501Q
R65FK3P	FORTH Kernel ROM for R6501Q
Order No.	**Description**
2148	FORTH Based Microcomputer User's Manual*

Note:
*Included with R65FR1.

SECTION 2
INTERFACE REQUIREMENTS

This section describes the interface requirements for the R65F11 and R65F12 single chip microcomputers. Figure 2-1 is the Interface Diagram for the R65F11 and R65F12, Figure 2-2 shows the pin out configuration and Table 2-1 describes the function of each pin of the R65F11 and R65F12. Figure 3-1 is a detailed block diagram.

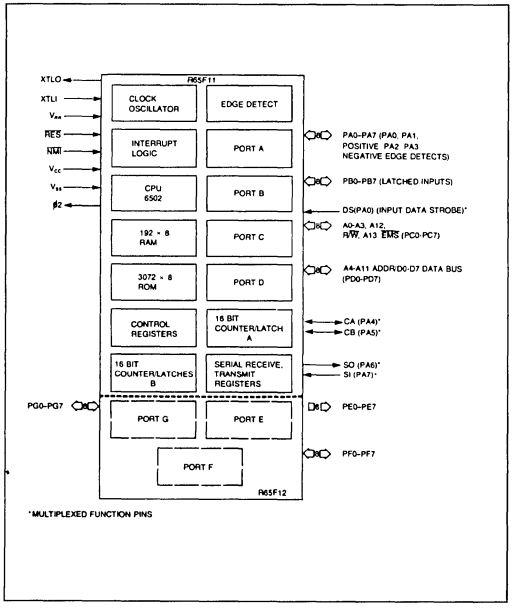
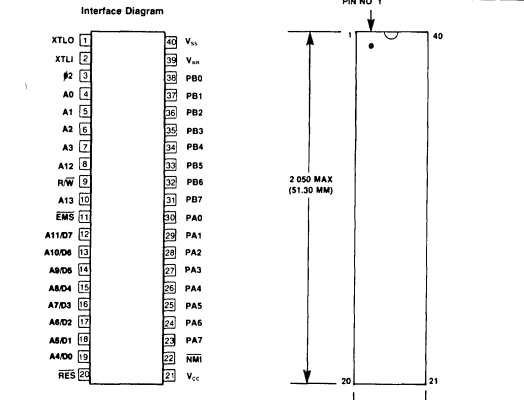


Figure 2-1. R65F11 and R65F12 Interface Diagram

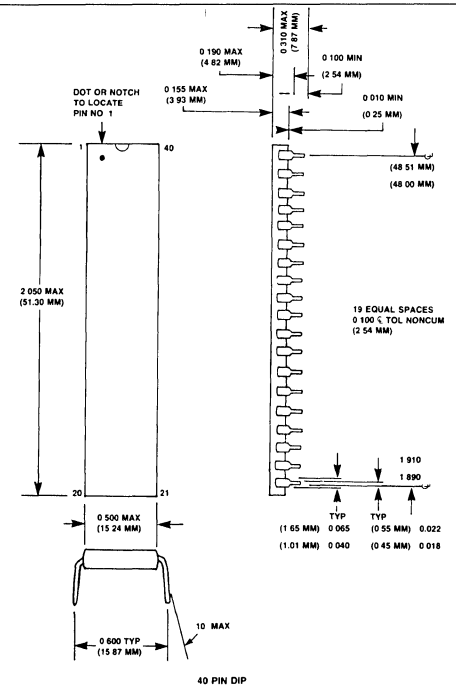
Table 2-1. R65F11 and R65F12 Pin Descriptions

Signal Name	Pin No. R65F11	Pin No. R65F12	Description
V_{CC}	21	50	Main power supply +5V
V_{RR}	39	12	Separate power pin for RAM. In the event that V_{CC} power is lost, this power retains RAM data.
V_{SS}	40	11	Signal and power ground (0V)
XTLI	2	10	Crystal or clock input for internal clock oscillator. Also allows input of X1 clock signal if XTLO is connected to V_{SS}, or X2 or X4 clock if XTLO is floated.
XTLO	1	9	Crystal output from internal clock oscillator.
$\overline{RES}$	20	41	The Reset input is used to initialize the R65F11. This signal must not transition from low to high for at least eight cycles after V_{CC} reaches operating range and the internal oscillator has stabilized.
$\phi 2$	3	13	Clock signal output at internal frequency.
$\overline{NMI}$	22	51	A negative going edge on the Non-Maskable Interrupt signal requests that a non-maskable interrupt be generated within the CPU.
PA0-PA7 PB0-PB7	30-23 38-31	64-57 8-1	Two 8-bit ports used for either input/output. Each line of Ports A and B consist of an active transistor to V_{SS} and a passive pull-up to V_{CC}.
PC0-PC7 A0-A3 A12, R/$\overline{W}$ A13, $\overline{EMS}$	4-11	25-32	Port C has an active pull-up transistor. Port D has active pull-up and pull-down transistors. Ports C and D lines form the external multiplexed address and data bus to allow external memory addressing.
PD0-PD7 A4-A11 D0-D7	19-12	40-33	
PE0-PE7 PF0-PF7 PG0-PG4 PG5-PG7		49-42 24-17 52-56, 14-16	On the R65F12, Port E may be used for output only. Ports F and G are similar to Ports A and B in construction and may be used for inputs or outputs.

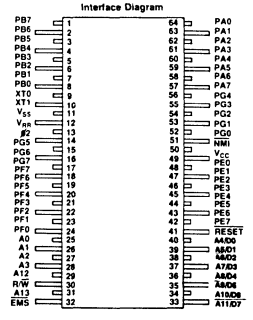
3



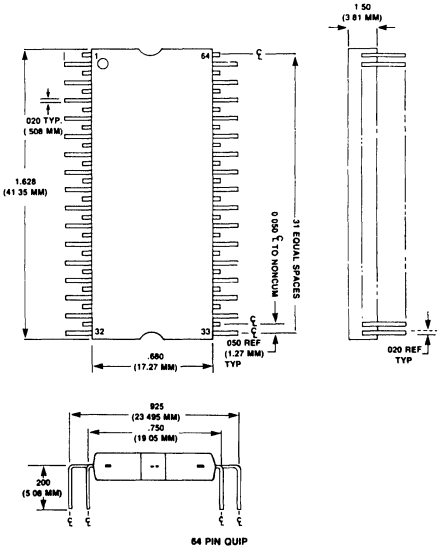
R65F11 Pin Out Designation



R65F11 Dimensional Outline



R65F12 Pin Out Designation



R65F12 Dimensional Outline

Figure 2-2. Pin Out Configuration

SECTION 3
SYSTEM ARCHITECTURE

This section provides a functional description of the R65F11 and R65F12. Functionally the R65F11 consists of a CPU, RAM memory, two 8-bit parallel I/O ports (five in the 64-pin R65F12), a serial I/O port, dual counter/latch circuits, a mode control register, an interrupt flag/enable dual register circuit, and an internal Operating System. The kernel of FORTH in ROM complements the system hardware. A block diagram of the system is shown in Figure 3-1.

NOTE

Throughout this document, unless specified otherwise, all memory or register address locations are specified in hexadecimal notation.

3.1 CPU LOGIC

The R65F11 internal CPU is a standard 6502 configuration with an 8-bit Accumulator register, two 8-bit Index Registers (X and Y); an 8-bit Stack Pointer register, and ALU, a 16-bit Program Counter, and standard instruction register/decode and internal timing control logic.

3.1.1 Accumulator

The accumulator is a general purpose 8-bit register that stores the results of most arithmetic and logic operations. In addition, the accumulator usually contains one of the two data words used in these operations.

3.1.2 Index Registers

There are two 8-bit index registers, X and Y. Each index register can be used as a base to modify the address data program counter and thus obtain a new address—the sum of the program counter contents and the index register contents.

When executing an instruction which specifies indirect addressing, the CPU fetches the op code and the address, and modifies the address from memory by adding the index register to it prior to loading or storing the value of memory.

Indexing greatly simplifies many types of programs, especially those using data tables.

3.1.3 Stack Pointer

The Stack Pointer is an 8-bit register. It is automatically incremented and decremented under control of the microprocessor to perform stack manipulation in response to either user instructions, an internal $\overline{IRQ}$ interrupt, or the external interrupt line $\overline{NMI}$. The Stack Pointer must be initialized by the user program.

The stack allows simple implementation of multiple level interrupts, subroutine nesting and simplification of many types of data manipulation. The JSR, BRK, RTI and RTS instructions use the stack and Stack Pointer.

The stack can be envisioned as a deck of cards which may only be accessed from the top. The address of a memory location is stored (or "pushed") onto the stack. Each time data are to be pushed onto the stack, the Stack Pointer is placed on the Address Bus, data are written into the memory location addressed by the Stack Pointer, and the Stack Pointer is decremented by 1. Each time data are read (or "pulled") from the stack, the Stack Pointer is incremented by 1. The Stack Pointer is then placed on the Address Bus, and data are read from the memory location addressed by the Pointer.

The stack is located on zero page, i.e., memory locations 00FF-0040. After reset, which leaves the Stack Pointer indeterminate, normal usage calls for its initialization at 00FF.

3.1.4 Processor Status Register

The 8-bit Processor Status Register contains seven status flags. Some of these flags are controlled by the user program; others may be controlled both by the user's program and the CPU. The R6500 instruction set contains a number of conditional branch instructions which are designed to allow testing of these flags. See Appendix B for details.

3.1.5 Program Counter

The 16-bit Program Counter provides the addresses that are used to step the processor through sequential instructions in a program. Each time the processor fetches an instruction from program memory, the lower (least significant) byte of the Program Counter (PCL) is placed on the low-order bits of the Address Bus and the higher (most significant) byte of the Program Counter (PCH) is placed on the high-order 8 bits of the Address Bus. The Counter is incremented each time an instruction or data is fetched from program memory.

3.1.6 Arithmetic And Logic Unit (ALU)

Each bit of the ALU has two inputs. These inputs can be tied to various internal buses or to a logic zero; the ALU then generates the function (AND, OR, SUM, and so on) using the data on the two inputs.

3.1.7 Instruction Register and Instruction Decode

Instructions are fetched from ROM or RAM and gated onto the Internal Data Bus. These instructions are latched into the Instruction Register then decoded along with timing and interrupt signals to generate control signals for the various registers.

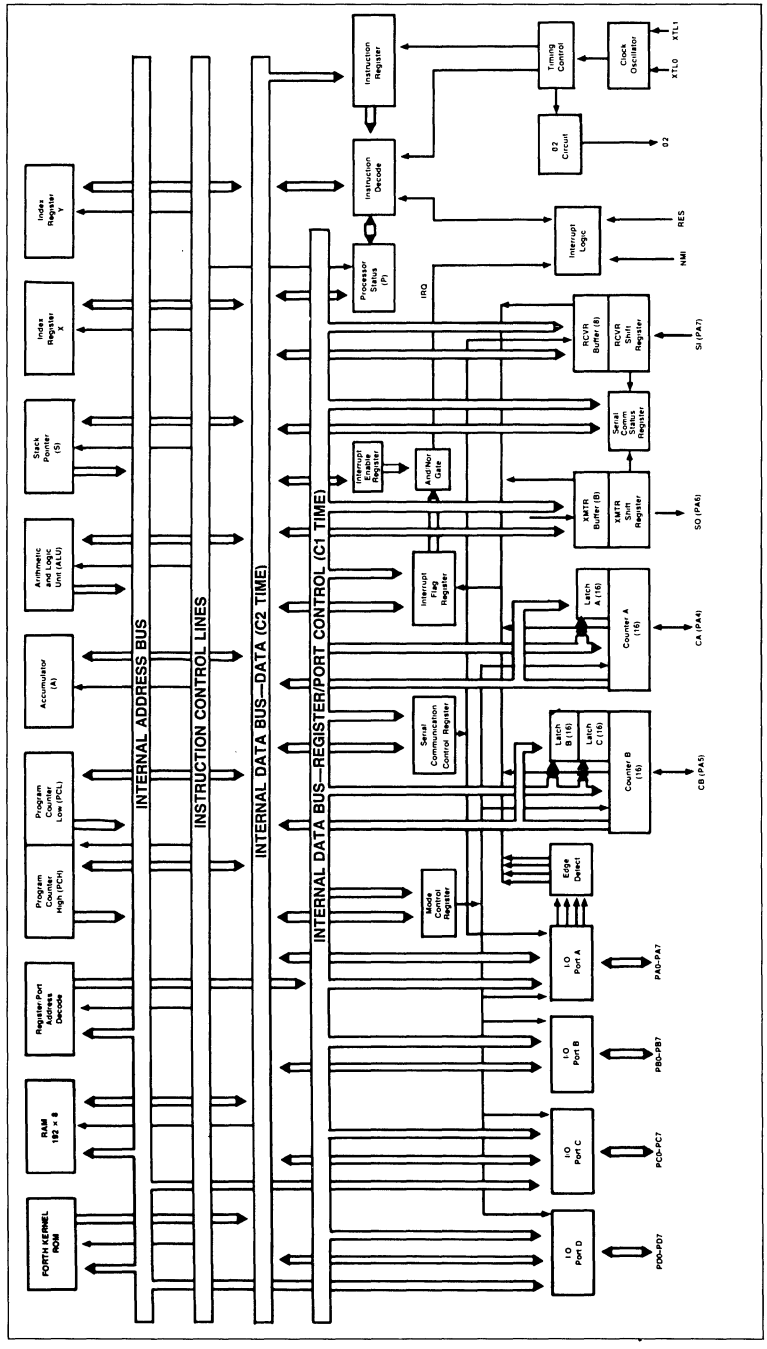


Figure 3-1. Detailed Block Diagram

3.1.8 Timing Control

The Timing Control Logic keeps track of the specific instruction cycle being executed. This logic is set to T0 each time an instruction fetch is executed and is advanced at the beginning of each Phase One clock pulse for as many cycles as are required to complete the instruction. Each data transfer which takes place between the registers is caused by decoding the contents of both the instruction register and timing control unit.

3.1.9 Interrupt Logic

Interrupt logic controls the sequencing of three interrupts; $\overline{RES}$, $\overline{NMI}$ and $\overline{IRQ}$. $\overline{IRQ}$ is generated by any one of eight conditions: 2 Counter Overflows, 2 Positive Edge Detects, 2 Negative Edge Detects, and 2 Serial Port Conditions.

3.2 CPU INSTRUCTION SET

The machine code instruction set of the R65F11 and R65F12 microcomputers are based on the popular R6500 microprocessor set. They contain all the instructions in the standard R6502 set, with the addition of the four new bit instructions added to the R6511 processor family. Refer to Appendix A for the Op Code mnemonics addressing matrix for details on these instructions.

3.3 READ-ONLY-MEMORY (ROM)

The ROM consists of preprogrammed memory with an address space from F400 to FFFF. It contains the run time kernel of the high level language Rockwell Single Chip FORTH. There are 133 included functions stored in the ROM. Codes are in the format of a two byte code field, which identifies the interpreter assigned to execute that word, followed by a variable length Parameter Field, which contains the instructions and data used by that interpreter according to the programmed intention of that definition. See Appendix D for a complete list of the names of all included words. All words needed for support of the run time operation of dedicated applications programs are included. The RSC-FORTH Operating System is also part of the ROM code and is entered upon Reset. This Operating System allow the R65F11 and R65F12 to auto start a user program written in either RSC-FORTH or Assembly Language or enter a Development ROM if one is present. If no auto start program is found, an attempt will be made to boot an operating program from floppy disk.

3.4 RANDOM ACCESS MEMORY (RAM)

The RAM consists of 192 bytes of read/write memory with an assigned page zero address of 0040 through 00FF. The R65F11 and R65F12 provide a separate power pin (V_{RR}) which may be used for standby power for 32 bytes located at 0040-005F. In the event of the loss of V_{CC} power, the lowest 32 bytes of RAM data will be retained if standby power is supplied to the V_{RR} pin. If the RAM data retention is not required then V_{RR} must be connected to V_{CC}. During operation V_{RR} must be at the V_{CC} level.

For the RAM to retain data upon loss of V_{CC}, V_{RR} must be supplied within operating range and $\overline{RES}$ must be driven low at least eight Ø2 clock pulses before V_{CC} falls out of operating range. $\overline{RES}$ must then be held low while V_{CC} is out of operating range and until at least eight Ø2 clock cycles after V_{CC} is again within operating range and the internal Ø2 oscillator is stabilized. V_{RR} must remain within V_{CC} operating range during normal operation. When V_{CC} is out of operating range, V_{RR} must remain within the V_{RR} retention range in order to retain data. Figure 3-2 shows typical waveforms.

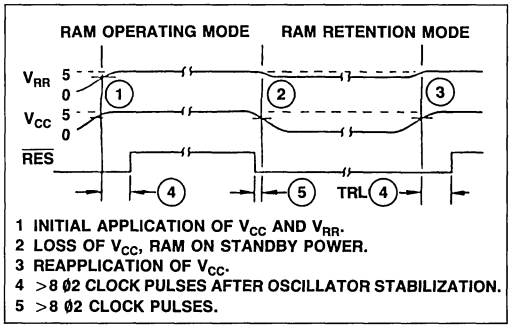


Figure 3-2. Data Retention Timing

3.5 CLOCK OSCILLATOR

A reference frequency can be generated with the on-chip oscillator using an external crystal. The oscillator reference frequency passes through an internal countdown network (divide by 2) to obtain the internal operating frequency.

The on-chip oscillator is designed for a parallel resonant crystal connected between XTLI and XTLO pins. The equivalent oscillator circuit is shown in Figure 3-3a.

A parallel resonant crystal is specified by its load capacitance and series resonant resistance. For proper oscillator operation, the load capacitance (C_L), series resistance (R_s) and the crystal resonant frequency (F) must meet the following two relations:

$$(C + 27) = 2C_L \quad \text{or} \quad C = 2C_L - 27 \text{ pF}$$

$$R_s \leq R_{smax} = \frac{2 \times 10^6}{(FC_L)^2} \quad F \text{ in MHz; } C_L \text{ in pF}$$

To select a parallel resonant crystal for the oscillator, first select the load capacitance from a Crystal Manufacturer's catalog. Next, calculate R_{smax} based on F and C_L. The selected crystal must have a R_s less than the R_{smax}.

For example, if C_L = 22 pF for a 4 MHz parallel resonant crystal, then

$$C = (2 \times 22) - 27 = 17 \text{ pF}$$
(use standard value, 18 pF)

The series resistance of the crystal must be less than

$$R_{smax} = \frac{2 \times 10^6}{(4 \times 22)^2} = 258 \text{ ohms}$$

Internal timing can also be controlled by driving the XTLI pin with an external frequency source. Figure 3-3b shows typical connections. If XTLO is left floating, the external source is divided by the internal countdown network. However, if XTLO is tied to V_{SS}, the internal coundown network is bypassed casuing the chip to operate at the freqency of the external source.

The R65F11 and R65F12 operate in the CLOCK MASTER mode. In this mode a frequence source (crystal or external source) must be applied to the XTLI and XTLO pins.

Ø2 is a buffered output signal which closely approximates the internal timing. When a common external source is used to drive multiple devices the internal timing between devices as well as their Ø2 outputs will be skewed in time. If skewing represents a system problem it can be avoided by the Master/Slave connection and options shown in Figure 3-4.

The R65F11 and R65F12 is operated in the CLOCK MASTER MODE. A second processor could be operated in the CLOCK SLAVE MODE. Mask options in the SLAVE unit convert the Ø2 signal into a clock input pin which is tightly coupled to the internal timing generator. As a result, the internal timing of the MASTER and SLAVE units are synchronized with minimum skew. If the Ø2 signal to the SLAVE unit is inverted, the MASTER and SLAVE UNITS WILL OPERATE OUT OF PHASE. This approach allows the two devices to share external memory using cycle stealing techniques.

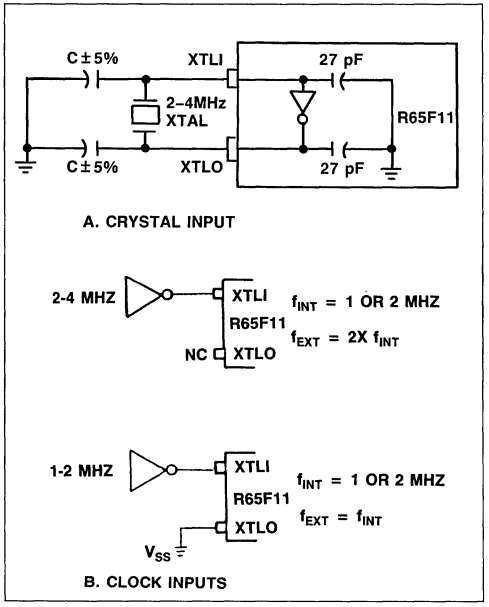


Figure 3-3. Clock Oscillator Input Options

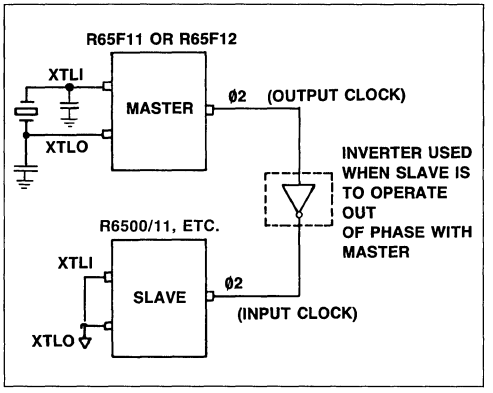


Figure 3-4. Master/Slave Connections

3.6 MODE CONTROL REGISTER (MCR)

The Mode Control Register contains bits for the multifunction I/O ports and mode select bits for Counter A and Counter B. Its setting, along with the setting of the Serial Communications Control Register (SCCR), determines the basic configuration of the R65F11 and R65F12 in any application. The Model Control Register bit assignment is shown in Figure 3-5. MCR Bits 7, 6, 5 must remain 1's in order for external memory referencing to be enabled.

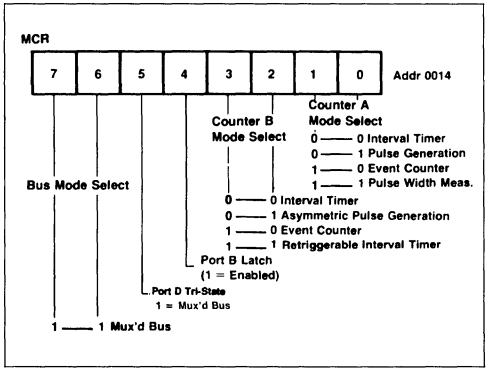


Figure 3-5. Mode Control Register

The use of Counter A Mode Select is shown in Section 6.1.

The use of Counter B Mode Select is shown in Section 6.2.

The use of Port B Latch Enable is shown in Section 4.4.

3.7 INTERRUPT FLAG REGISTER (IFR) AND INTERRUPT ENABLE REGISTER (IER)

An $\overline{IRQ}$ interrupt request can be initiated by any or all of eight possible sources. These sources are all capable of being enabled or disabled by the use of the appropriate interrupt enabled bits in the Interrupt Enable Register (IER). Multiple simultaneous interrupts will cause the $\overline{IRQ}$ interrupt request to remain active until all interrupting conditions have been serviced and cleared.

The Interrupt Flag Register contains the information that indicates which I/O or counter needs attention. The contents of the Interrupt Flag Register may be examined at any time by reading at address: 0011. Edge detect IFR bits may be cleared in low level code by executing a RMB instruction at address location 0010. The RMB X, (0010) instruction reads FF, modifies bit X to a "0", and writes the modified value at address location 0011. In this way IFR bits set to a "1" after the read cycle of a Read-Modify-Write instruction (such as RMB) are protected from being cleared. A logic "1" is ignored when writing to edge detect IFR bits.

Each IFR bit has a corresponding bit in the Interrupt Enable Register which can be set to a "1" by writing a "1" in the respective bit position at location 0012. Individual IER bits may be cleared by writing a "0" in the respective bit position, or by $\overline{RES}$. If set to a "1", an IRQ will be generated when the corresponding IFR bit becomes true. The Interrupt Flag Register and Interrupt Enable Register bit assignments are shown in Figure 3-6 and the functions of each bit are explained in Table 3-1.

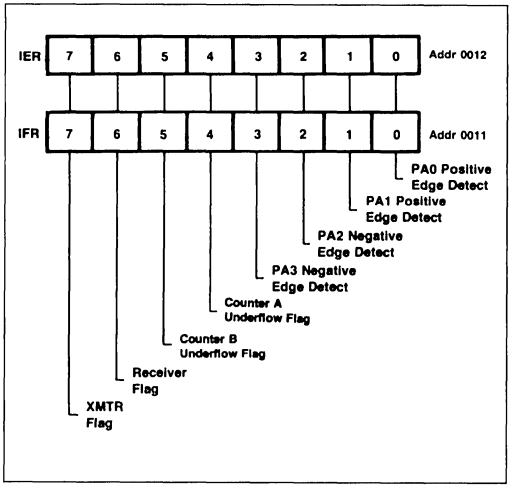


Figure 3-6. Interrupt Enable and Flag Registers

Table 3-1. Interrupt Flag Register Bit Codes

Bit Code	Function
IFR 0:	PA0 Positive Edge Detect Flag—Set to a "1" when a positive going edge is detected on PA0. Cleared by RMB 0 (0010) instruction or by $\overline{RES}$.
IFR 1:	PA1 Positive Edge Detect Flag—Set to a 1 when a positive going edge is detected on PA1. Cleared by RMB 1 (0010) instruction or by $\overline{RES}$.
IFR 2:	PA2 Negative Edge Detect Flag—Set to a 1 when a negative going edge is detected on PA2. Cleared by RMB 2 (0010) instruction or by $\overline{RES}$.
IFR 3:	PA3 Negative Edge Detect Flag—Set to 1 when a negative going edge is detected on PA3. Cleared by RMB 3 (0010) instruction or by $\overline{RES}$.
IFR 4:	Counter A Underflow Flag—Set to a 1 when Counter A underflow occurs. Cleared by reading the Lower Counter A at location 0018, by writing to address location 001A, or by $\overline{RES}$.
IFR 5:	Counter B Underflow Flag—Set to a 1 when Counter B underflow occurs. Cleared by reading the Lower Counter B at location 001C, by writing to address location 001E, or by $\overline{RES}$.
IFR 6:	Receiver Interrupt Flag—Set to a 1 when any of the Serial Communication Status Register bits 0 through 3 is set to a 1. Cleared when the Receiver Status bits (SCSR 0-3) are cleared or by $\overline{RES}$.
IFR 7:	Transmitter Interrupt Flag—Set to a 1 when SCSR 6 is set to a 1 while SCSR 5 is a 0 or SCSR 7 is set to a 1. Cleared when the Transmitter Status bits (SCSR 6 & 7) are cleared or by $\overline{RES}$.

3.8 OPERATING SYSTEM

The system startup function, COLD, is executed upon Reset. COLD, a high level FORTH word, forms the basis of the RSC Operating System. Upon reset this function initializes the R65F11 or R65F12 registers to establish the external 16K byte memory map and disable all interrupt sources. It also sets up the serial channel for 1200 baud (assuming a 1 MHz internal clock) asynchronous transmission (seven bits, parity disabled). The internal FORTH structure "W" is prepared for use and the low level input/output vectors are forced to point to the system serial channel routines. The FORTH User Area Pointer, UP, is assigned the value 0300 Hex.

A test is made of the variable CLD/WRM in memory location 030E. If this contains a value other than A55A Hex a cold reset is assumed. In this case, the low level IRQ vector, IRQVEC; the low level NMI Vector, NMIVEC, and the high level interrupt vector, INTVEC, are all forced to point to the system reset routine. This prevents an unintentionally generated interrupt from crashing the system. System variables TIB, RO, SO, UC/L, UPAD, UR/W and BASE are also initialized to their default values.

Whether a warm or cold reset, the memory map is then searched at every 1K byte boundary starting at location 0400 Hex. The first two bytes at each boundary are checked against an A55A Hex bit pattern. This pattern indicates that an auto start program is installed. The next two bytes are assumed to point to the Parameter Field of the high level RSC-FORTH word to be executed upon reset. This may be the main function of a user defined program or the start up routine of a Development ROM. Figure 3-7 details proper alignment.

If no auto start ROM is found, the Operating System turns control over to a program that issues a "NO ROM" message to the systems terminal via the serial channel and attempts to boot a program from disk. A floppy disk controller, compatible with the WD1793 type, is assumed to be present at address 0100 Hex. The first half of Track 0 Sector 1 is loaded from a double density boot diskette into RAM starting at address 005F. When successfully loaded execution will be turned over to this boot program.

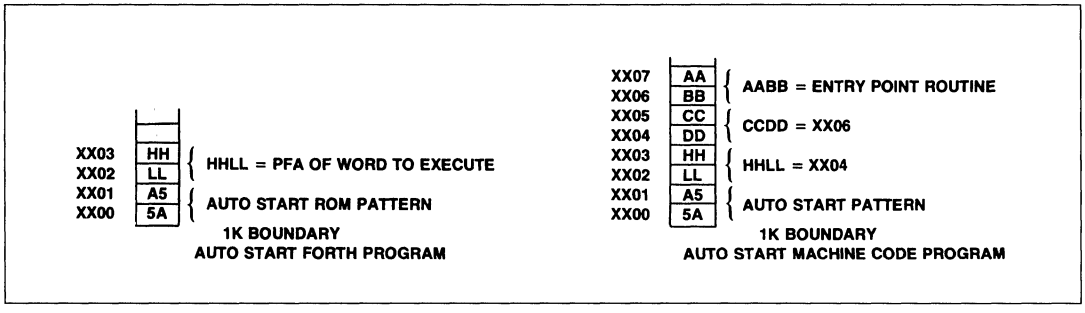


Figure 3-7. Auto Start ROM

SECTION 4
PARALLEL INPUT/OUTPUT PORTS

The R65F11 has 16 I/O lines grouped into two 8-bit ports (PA, PB) and 16 lines programmed as an Address/Data bus (PC & PD). Ports A and B may be used either for input or output individually or in groups of any combination. The R65F12 has 24 additional port lines grouped into three 8-bit ports (PE, PF, PG).

Multifunction I/O's such as Port A are protected from normal port I/O instructions when they are programmed to perform a multiplexed function.

Internal pull-up resistors (FET's with an impedance range of 3K ≤ Rpu ≤ 12K ohm) are provided on all port pins.

The direction of the I/O lines are controlled by 8-bit port registers located in page zero. This arrangement provides quick programming access using simple two-byte zero page address instructions. There are no direction registers associated with the I/O ports, which simplifies I/O handling. The I/O addresses are shown in Table 4-1.

Table 4-1. I/O Port Addresses

Port	Address
A	0000
B	0001
E	0004
F	0005
G	0006

Appendix F.4 shows the I/O Port Timing.

4.1 INPUTS

Inputs for Ports A and B are enabled by loading logic 1 into all I/O port register bit positions that are to correspond to I/O input lines. A low (<0.8V) input signal will cause a logic 0 to be read when a read instruction is issued to the port register. A high (>2.0V) input will cause a logic 1 to be read. An $\overline{RES}$ signal forces all I/O port registers to logic 1 thus initially treating all I/O lines as inputs.

The status of the input lines can be interrogated at any time by reading the I/O port addresses. Note that this will return the actual status of the input lines, not the data written into the I/O port registers.

Read/Modify/Write instructions can be used to modify the operation of PA and PB. During the Read cycle of a Read/Modify/Write instruction the Port I/O register is read. For all other read instructions the port input lines are read. Read/Modify/Write instructions are: ASL, DEC, INC, LSR, RMB, ROL, ROR, and SMB.

4.2 OUTPUTS

Outputs for Ports A and B are controlled by writing the desired I/O line output states into the corresponding I/O port register bit positions. A logic 1 will force a high (>2.4V) output while a logic 0 will force a low (<0.4V) output.

4.3 PORT A (PA)

Port A can be programmed via the Mode Control Register (MCR) and the Serial Communications Control Register (SCCR) as a standard parallel 8-bit, bit independent, I/O port or as serial channel I/O lines, counter I/O lines, or an input data strobe for the Port B input latch option. Table 4-3 tabulates the control and usage of Port A.

In addition to their normal I/O functions, PA0 and PA1 can detect positive going edges, and PA2 and PA3 can detect negative going edges. A proper transition on these pins will set a corresponding status bit in the IFR and generate an interrupt request if the respective Interrupt Enable Bit is set. The maximum rate at which an edge can be detected is one-half the ∅2 clock rate. Edge detection timing is shown in Appendix F.4.

4.4 PORT B (PB)

Port B can be programmed as an 8 bit, bit independent I/O port. It has a latched input capability which may be enabled or disabled via the Mode Control Register (MCR). Table 4-2 tabulates the control and usage of Port B. An Input Data Strobe signal must be provided thru PA0 when Port B is programmed to be used with latched input option. Input data latch timing for Port B is shown in Appendix F.4.

Table 4-2. Port B Control & Usage

Pin No. R65F11	Pin No. R65F12	I/O Mode MCR4 = 0 Signal Name	I/O Mode MCR4 = 0 Signal Type (1)	Latch Mode MCR4 = 1 (2) Signal Name	Latch Mode MCR4 = 1 (2) Signal Type
38	8	PB0	I/O	PB0	INPUT
37	7	PB1	I/O	PB1	INPUT
36	6	PB2	I/O	PB2	INPUT
35	5	PB3	I/O	PB3	INPUT
34	4	PB4	I/O	PB4	INPUT
33	3	PB5	I/O	PB5	INPUT
32	2	PB6	I/O	PB6	INPUT
31	1	PB7	I/O	PB7	INPUT

(1) Resistive pull-up, active buffer pull down
(2) Input data is stored in port B latch by PA0 pulse

Table 4-3. Port A Control and Usage

R65F11/R65F12 PORT[5]	PA0 I/O		PORT B LATCH MODE	
	MCR4 = 0		MCR4 = 1	
	SIGNAL		SIGNAL	
	NAME	TYPE	NAME	TYPE
PA0[2]	PA0	I/O	PORT B LATCH STROBE	INPUT[1]

	PA1-PA3 I/O	
	SIGNAL	
	NAME	TYPE
PA1[2] PA2[3] PA3[3]	PA1 PA2 PA3	I/O I/O I/O

	PA4 I/O		COUNTER A I/O			
PA4	MCR0 = 0 MCR1 = 0 SCCR7 = 0 RCVR S/R MODE = 0[4] [6]		MCR0 = 1 MSR1 = 0 SCCR7 = 0 RCVR S/R MODE = 0[4]		SCCR7 = 0 SCCR6 = 0 MCR1 = 1	
	SIGNAL		SIGNAL		SIGNAL	
	NAME	TYPE	NAME	TYPE	NAME	TYPE
	PA4	I/O	CNTA	OUTPUT	CNTA	INPUT (1)
	SERIAL I/O SHIFT REGISTER CLOCK					
	SCCR7 = 1 SCCR5 = 1		RCVR S/R MODE = 1[4]			
	SIGNAL		SIGNAL			
	NAME	TYPE	NAME	TYPE		
	XMTR CLOCK	OUTPUT	RCVR CLOCK	INPUT (1)		

	PA5 I/O		COUNTER B I/O			
PA5	MCR3 = 0 MCR2 = 0		MCR3 = 0 MCR2 = 1		MCR3 = 1 MCR2 = X	
	SIGNAL		SIGNAL		SIGNAL	
	NAME	TYPE	NAME	TYPE	NAME	TYPE
	PA5	I/O	CNTB	OUTPUT	CNTB	INPUT (1)

	PA6 I/O		SERIAL I/O XMTR OUTPUT	
PA6	SCCR7 = 0		SCCR7 = 1	
	SIGNAL		SIGNAL	
	NAME	TYPE	NAME	TYPE
	PA6	I/O	XMTR	OUTPUT

	PA7 I/O		SERIAL I/O RCVR INPUT	
PA7	SCCR6 = 0		SCCR6 = 1	
	SIGNAL		SIGNAL	
	NAME	TYPE	NAME	TYPE
	PA7	I/O	RCVR	INPUT (1)

(1) HARDWARE BUFFER FLOAT
(2) POSITIVE EDGE DETECT
(3) NEGATIVE EDGE DETECT
(4) RCVR S/R MODE = 1 WHEN SCCR6 • SCCR5 • SCCR4 = 1
(5) APPLIES TO EITHER R65F11 OR R65F12 PORT (SEE PIN DIAGRAM)
(6) FOR THE FOLLOWING MODE COMBINATIONS PA4 IS AVAILABLE AS AN INPUT ONLY PIN:
$\overline{SCCR7} \cdot \overline{SCCR6} \cdot SCCR5 \cdot \overline{MCR1} + \overline{SCCR7} \cdot SCCR6 \cdot \overline{SCCR4} \cdot MCR1 + SCCR7 \cdot \overline{SCCR6} \cdot \overline{SCCR5} + SCCR7 \cdot \overline{SCCR5} \cdot \overline{SCCR4}$

4.5 PORT C (PC)

Port C is preprogrammed as part of the Address/Data bus. PC0-PC7 function as A0-A3, A12, R/W, A13, and $\overline{EMS}$, respectively, as shown in Table 4-4. $\overline{EMS}$ (External Memory Select) is asserted (low) whenever the internal processor accesses memory area between 0100 and 3FFF. (See Memory Map, Appendix C). The leading edge of $\overline{EMS}$ may be used to strobe the eight address lines multiplexed on Port D. See Appendix F.3 for Port C timing.

4.6 PORT D (PD)

Port D is also preprogrammed as part of the Address/Data bus. Data bits D0 through D7 are time multiplexed with address bits A4 through A11, respectively. Refer to the Memory Maps (Appendix C) for Multiplexed memory assignments. See Appendix F.3 for Port D timing.

4.7 PORT E (PE), PORT F (PF), PORT G (PG)

Ports E, F and G are available on the R65F12 only. Port E can only be used as outputs. Port F and Port G can be used for inputs or outputs and are similar to Port A and Port B in operation.

Table 4-4. Port C Control and Usage

R65F11/ R65F12 Port	Multiplexed Mode MCR7 = 1 MCR6 = 1 Signal Name	Signal Type (1)
PC0	A0	OUTPUT
PC1	A1	OUTPUT
PC2	A2	OUTPUT
PC3	A3	OUTPUT
PC4	A12	OUTPUT
PC5	R/W	OUTPUT
PC6	A13	OUTPUT
PC7	EMS	OUTPUT

Table 4-5. Port D Control and Usage

R65F11/ R65F12 Port	Multiplexed Mode MCR7 = 1 MCR6 = 1 MCR5 = 1 Signal Phase 1 Name	Signal Phase 1 Type (2)	Signal Phase 2 Name	Signal Phase 2 Type (3)
PD0	A4	OUTPUT	DATA0	I/O
PD1	A5	OUTPUT	DATA1	I/O
PD2	A6	OUTPUT	DATA2	I/O
PD3	A7	OUTPUT	DATA3	I/O
PD4	A8	OUTPUT	DATA4	I/O
PD5	A9	OUTPUT	DATA5	I/O
PD6	A10	OUTPUT	DATA6	I/O
PD7	A11	OUTPUT	DATA7	I/O

(1) Active Buffer Pull-up and Pull-Down
(2) Tri-State Buffer is in Active Mode
(3) Tri-State Buffer is in Active Mode only during the Phase 2 Portion of a Write Cycle

SECTION 5
SERIAL INPUT/OUTPUT CHANNEL

The R65F11 and R65F12 Microcomputers provide a full duplex Serial I/O channel with programmable bit rates and operating modes. The serial I/O functions are controlled by the Serial Communication Control Register (SCCR). The SCCR bit assignment is shown in Figure 5-1. The serial bit rate is determined by Counter A for all modes except the Receiver Shift Register (RCVR S/R) mode for which an external shift clock must be provided. The maximum data rate using the internal clock is 62.5K bits per second (@ Ø2 = 1 MHZ). The transmitter (XMTR) and receiver (RCVR) can be independently programmed to operate in different modes and can be independently enabled or disabled.

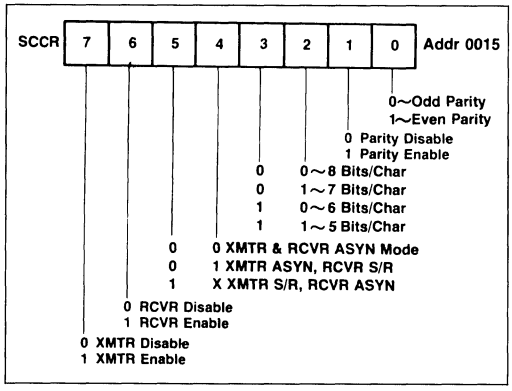


Figure 5-1. Serial Communication Control Register

Except for the Receiver Shift Register Mode (RCVR S/R), all XMTR and RCVR bit rates will occur at one sixteenth of the Counter A interval timer rate. Counter A is forced into an interval timer mode whenever the serial I/O is enabled in a mode requiring an internal clock.

Whenever Counter A is required as a timing source it must be loaded with the hexadecimal code that selects the data rate for the serial I/O Port. Refer to Counter A (paragraph 6.1) for a table of hexadecimal values to represent the desired data rate.

5.1 TRANSMITTER OPERATION (XTMR)

The XTMR operation and the transmitter related control/status functions are enabled by bit 7 of the Serial Communications Control Register (SCCR). The transmitter, when in the Asynchronous (ASYN) mode, automatically adds a start bit, one or two stop bits, and, when enabled, a parity bit to the transmitted data. A word of transmitted data (in asynchronous parity mode) can have 5, 6, 7, or 8 bits of data. The nine data modes are shown below. When parity is disabled, the 5, 6, 7 or 8 bits of data are terminated with two stop bits.

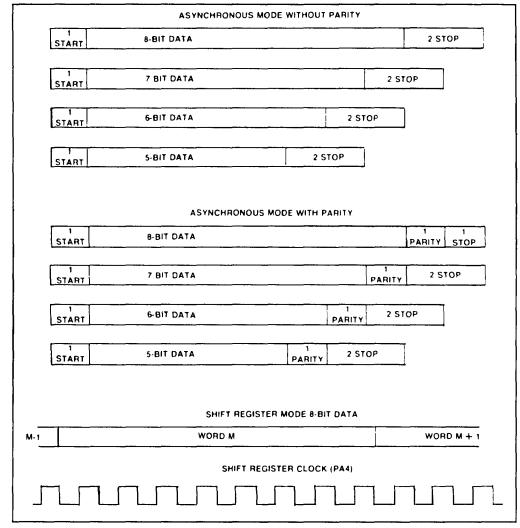


Figure 5-2. Bit Allocations

In the S/R mode, eight data bits are always shifted out. Bits/character and parity control bits are ignored. The serial data is shifted out via the SO output (PA6) and the shift clock is available at the CA (PA4) pin. When the transmitter underruns in the S/R mode the SO output and shift clock are held in a high state.

The XMTR Interrupt Flag bit (IFR7) is controlled by Serial Communication Status Register bits SCCR5, SCCR6 and SCCR7.

$$IFR7 = SCSR6\ (\overline{SCCR5} + SCCR7)$$

5.2 RECEIVER OPERATION (RCVR)

The receiver and its selected control and status functions are enabled when SCCR-6 is set to a "1." In the ASYN mode, data format must have a start bit, appropriate number of data bits, a parity bit (if enabled) and one stop bit. Refer to Figure 5-2 for a diagram of bit allocations. The receiver bit period is divided into 8 sub-intervals for internal synchronization. The receiver bit stream is synchronized by the start bit and a strobe signal is generated at the approximate center of each incoming bit. Refer to Figure 5-3 for ASYN Receive Data Timing. The character assembly process does not start if the start bit signal is less than one-half the bit time after a low level is detected on the Receive Data Input. Framing error, over-run, and parity error conditions or a RCVR Data Register Full will set the appropriate status bits, and any of the above conditions will cause an Interrupt Request if the Receiver Interrupt Enable bit is set to logic 1.

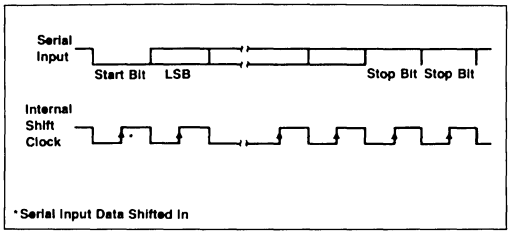


Figure 5-3. ASYN Receive Data Timing

In the S/R mode, an external shift clock must be provided at CA (PA4) pin along with 8 bits of serial data (LSB first) at the SI input (PA7). The maximum data rate using an external shift clock is one-eighth the internal clock rate. Refer to Figure 5-4 for S/R Mode Timing.

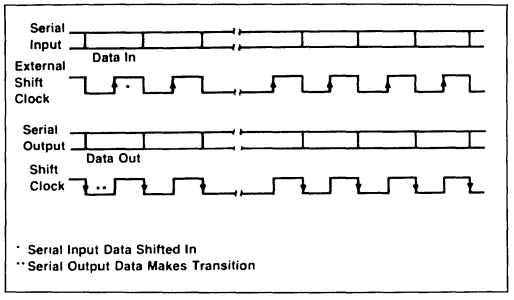


Figure 5-4. S/R Mode Timing

A RCVR interrupt (IFR6) is generated whenever any of SCSR0-3 are true.

5.3 SERIAL COMMUNICATION STATUS REGISTER (SCSR)

The Serial Communication Status Register (SCSR) holds information on various communication error conditions, status of the transmitter and receiver data registers, a transmitter end-of-transmission condition, and a receiver idle line condition (Wake-Up Feature). The SCSR bit assignment is shown in Figure 5-5. Bit assignments and functions of the SCSR are as follows:

SCSR 0: *Receiver Data Register Full*—Set to a logic 1 when a character is transferred from the Receiver Shift Register to the Receiver Data Register. This bit is cleared by reading the Receiver Data Register, or by $\overline{RES}$ and is disabled if SCCR 6 = 0. The SCSR 0 bit will not be set to a logic 1 if the received data contains an error condition, however, a corresponding error bit will be set to a logic 1 instead.

SCSR 1: *Over-Run Error*—Set to a logic 1 when a new character is transferred from the Receiver Shift Register, with the last character still in the Receiver Data Register. This bit is cleared by reading the Receiver Data Register, or by $\overline{RES}$.

SCSR 2: *Parity Error*—Set to logic 1 when the RCVR is in the ASYN Mode, Parity Enable bit is set, and the received data has a parity error. This bit is cleared by reading the Receiver Data Register or by $\overline{RES}$.

SCSR 3: *Framing Error*—Set to a logic 1 when the received data contains a zero bit after the last data or parity bit in the stop bit slot. Cleared by reading the Receiver Data Register or by $\overline{RES}$. (ASYN Mode only).

SCSR 4: *Wake-Up*—Set to a logic 1 by writing a "1" in bit 4 of address: 0016. The Wake-Up bit is cleared by $\overline{RES}$ or when the receiver detects a string of ten consecutive 1's. When the Wake-Up bit is set SCSR0 through SCSR3 are inhibited.

SCSR 5: *End of Transmission*—Set to a logic 1 by writing a "1" in bit position 5 of address: 0016. The End of Transmission bit is cleared by $\overline{RES}$ or upon writing a new data word into the Transmitter Data Register. When the End-of-Transmission bit is true the Transmitter Register Empty bit is disabled until a Transmitter Under-Run occurs.

SCSR 6: *Transmitter Data Register Empty*—Set to a logic 1 when the contents of the Transmitter Data Register is transferred to the Transmitter Shift Register. Cleared upon writing new data into the Transmit Data Register. This bit is initialized to a logic 1 by $\overline{RES}$.

SCSR 7: *Transmitter Under-Run*—Set to a logic 1 when the last data bit is transmitted if the transmitter is in a S/R Mode or when the last stop bit is transmitted if the XMTR is in the ASYN Mode while the Transmitter Data Register Empty Bit is set. Cleared by a transfer of new data into the Transmitter Shift Register, or by $\overline{RES}$.

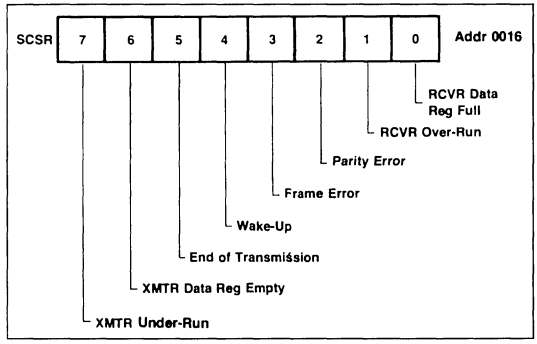


Figure 5-5. SCSR Bit Allocations

5.4 WAKE-UP FEATURE

In a multi-distributed microprocessor or microcomputer applications, a destination address is usually included at the beginning of the message. The Wake-Up Feature allows non-selected CPU's to ignore the remainder of the message until the beginning of the next message by setting the Wake-Up bit. As long as the Wake-Up flag is true, the Receiver Data Register Full Flag remains false. The Wake-Up bit is automatically cleared when the receiver detects a string of ten consecutive 1's which indicates an idle transmit line. When the next byte is received, the Receiver Data Register Full Flag signals the CPU to wake-up and read the received data.

SECTION 6
COUNTER/TIMERS

The R65F11 and R65F12 Microcomputers contain two 16-bit counters (Counter A and Counter B) and three 16-bit latches associated with the counters. Counter A has one 16-bit latch and Counter B has two 16-bit latches. Each counter can be independently programmed to operate in one of four modes:

Counter A	Counter B
• Pulse width measurement	• Retriggerable Interval Counter
• Pulse Generation	• Asymmetrical Pulse Generation
• Interval Timer	• Interval Timer
• Event Counter	• Event Counter

Operating modes of Counter A and Counter B are controlled by the Mode Control Register. All counting begins at the initialization value and decrements. When modes are selected requiring a counter input/output line, PA4 is automatically selected for Counter A and PA5 is automatically selected for Counter B (see Table 4.2).

6.1 COUNTER A

Counter A consists of a 16-bit counter and a 16-bit latch organized as follows: Lower Counter A (LCA), Upper Counter A (UCA), Lower Latch A (LLA), and Upper Latch A (ULA). The counter contains the count of either Ø2 clock pulses or external events, depending on the counter mode selected. The contents of Counter A may be read any time by executing a read at location 0019 for the Upper Counter A and at location 001A or location 0018 for the Lower Counter A. A read at location 0018 also clears the Counter A Underflow Flag (IFR4).

The 16-bit latch contains the counter initialization value, and can be loaded at any time by executing a write to the Upper Latch A at location 0019 and the Lower Latch A at location 0018. In either case, the contents of the accumulator are copied into the applicable latch register.

Counter A can be started at any time by writing to address: 001A. The contents of the accumulator will be copied into the Upper Latch A before the contents of the 16-bit latch are transferred to Counter A. Counter A is set to the latch value whenever Counter A underflows. When Counter A decrements from 0000 the next counter value will be the latch value, not FFFF, and the Counter A Underflow Flag (IFR 4) will be set to "1". This bit may be cleared by reading the Lower Counter A at location 0018, by writing to address location 001A, or by $\overline{RES}$.

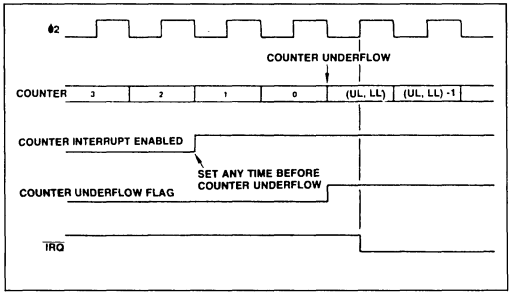


Figure 6-1. Interval Timer Timing Diagram

Counter A operates in any of four modes. These modes are selected by the Counter A Mode Control bits in the Control Register. See Table 6-1.

Table 6-1. Counter A Control Bits

MCR1 (bit 1)	MCR0 (bit 0)	Mode
0	0	Interval Timer
0	1	Pulse Generation
1	0	Event Counter
1	1	Pulse Width Measurement

The Interval Timer, Pulse Generation, and Pulse Width Measurement Modes are Ø2 clock counter modes. The Event Counter Mode counts the occurrences of an external event on the CNTR line.

The Counter is set to the Interval Timer Mode (00) when a $\overline{RES}$ signal is generated.

6.1.1 Interval Timer

In the Interval Timer mode the Counter is initialized to the Latch value by either of two conditions:-

1. When the Counter is decremented from 0000, the next Counter value is the Latch value (not FFFF).

2. When a write operation is performed to the Load Upper Latch and Transfer Latch to Counter address 001A, the Counter is loaded with the Latch value. Note that the contents of the Accumulator are loaded into the Upper Latch before the Latch value is transferred to the Counter.

The Counter value is decremented by one count at the Ø2 clock rate. The 16-bit Counter can hold from 1 to 65535 counts. The Counter Timer capacity is therefore 1μs to 65 535 ms at the 1 MHz Ø2 clock rate or 0.5 μs to 32.767 ms at the 2 MHz Ø2 clock rate. Time intervals greater than the maximum Counter value can be easily measured by counting $\overline{IRQ}$ interrupt requests in the counter $\overline{IRQ}$ interrupt routine.

When Counter A decrements from 0000, the Counter A Underflow (IFR4) is set to logic 1. If the Counter A Interrupt Enable Bit (IER4) is also set, an $\overline{IRQ}$ interrupt request will be generated. The Counter A Underflow bit in the Interrupt Flag Register can be examined in the $\overline{IRQ}$ interrupt routine to determine that the $\overline{IRQ}$ was generated by the Counter A Underflow.

While the timer is operating in the Interval Timer Mode, PA4 operates as a PA I/O bit.

A timing diagram of the Interval Timer Mode is shown in Figure 6-1.

6.1.2 Pulse Generation Mode

In the Pulse Generation mode, the CA line operates as a Counter Output. The line toggles from low to high or from high to low whenever a Counter A Underflow occurs, or a write is performed to address 001A.

The normal output waveform is a symmetrical square-wave. The CA output is initialized high when entering the mode and transitions low when writing to 001A.

Asymmetric waveforms can be generated if the value of the latch is changed after each counter underflow.

A one-shot waveform can be generated by changing from Pulse Generation to Interval Timer mode after only one occurrence of the output toggle condition.

6.1.3 Event Counter Mode

In this mode the CA is used as an Event Input line, and the Counter will decrement with each rising edge detected on this line. The maximum rate at which this edge can be detected is one-half the ϕ2 clock rate.

The Counter can count up to 65,535 occurrences before underflowing. As in the other modes, the Counter A Underflow bit (IER4) is set to logic 1 if the underflow occurs.

Figure 6.2 is a timing diagram of the Event Counter Mode.

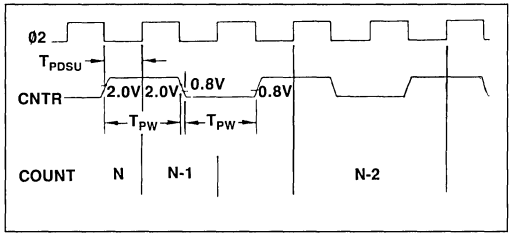


Figure 6-2. Event Counter Mode

6.1.4 Pulse Width Measurement Mode

This mode allows the accurate measurement of a low pulse duration on the CA line. The Counter decrements by one count at the ϕ2 clock rate as long as the CA line is held in the low state. The Counter is stopped when CA is in the high state.

The Counter A underflow flag will be set only when the count in the timer reaches zero. Upon reaching zero the timer will be loaded with the latch value and continue counting down as long as the CA pin is held low. After the counter is stopped by a high level on CA, the count will hold as long as CA remains high. Any further low levels on CA will again cause the counter to count down from its present value. The state of the CA line can be determined by testing the state of PA4.

A timing diagram for the Pulse Width Measurement Mode is shown in Figure 6-3.

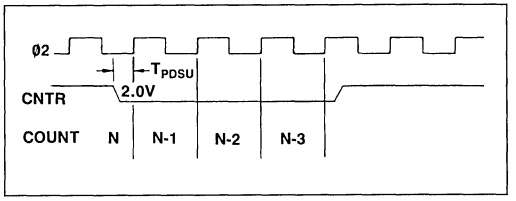


Figure 6-3. Pulse Width Measurement

6.1.5 Serial I/O Data Rate Generation

Counter A also provides clock timing for the Serial I/O which establishes the data rate for the Serial I/O port. When the Serial I/O is enabled, Counter A is forced to operate at the internal clock rate. Counter A is not required for the RCVR S/R mode. The Counter I/O (PA4) may also be required to support the Serial I/O (see Table 4-2).

Table 6-2 identifies the values to be loaded in Counter A for selecting standard data rates with a ϕ2 clock rate of 1 MHz and 2 MHz. Although Table 6-2 identifies only the more common data rates, any data rate from 1 to 62.5K bps can be selected by using the formula:

$$N = \frac{\phi 2}{16 \times bps} - 1$$

where

N = decimal value to be loaded into Counter A using its hexadecimal equivalent.
ϕ2 = the clock frequency (1 MHz or 2 MHz)
bps = the desired data rate.

NOTE

In Table 6-2 you will notice that the standard data rate and the actual data rate may be slightly different. Transmitter and receiver errors of 1.5% or less are acceptable. A revised clock rate is included in Table 6-2 for those baud rates which fall outside this limit.

Table 6-2. Counter A Values for Baud Rate Selection

Standard Baud Rate	Hexadecimal Value		Actual Baud Rate At		Clock Rate Needed To Get Standard Baud Rate	
	1 MHz	2 MHz	1 MHz	2 MHz	1 MHz	2 MHz
50	04E1	09C3	50.00	50.00	1.0000	2.0000
75	0340	0682	75.03	74.99	1.0000	2.0000
110	0237	046F	110.04	110.04	1.0000	2.0000
150	01A0	0340	149.88	150.06	1.0000	2.0000
300	00CF	01A0	300.48	299.76	1.0000	2.0000
600	0067	00CF	600.96	600.96	1.0000	2.0000
1200	0033	0067	1201.92	1201.92	1.0000	2.0000
2400	0019	0033	2403.85	2403.85	1.0000	2.0000
3600	0010	0021	3676.47	3676.47	0.9792	1.9584
4800	000C	0019	4807.69	4807.69	1.0000	2.0000
7200	0008	0010	6944.44	7352.94	1.0368	1.9584
9600	0006	000C	8928.57	9615.38	1.0752	2.0000

6.2 COUNTER B

Counter B consists of a 16-bit counter and two 16-bit latches organized as follows: Lower Counter B (LCB), Upper Counter B (UCB), Lower Latch B (LLB), Upper Latch B (ULB), Lower Latch C (LLC), and Upper Latch C (ULC). Latch C is used only in the asymmetrical pulse generation mode. The counter contains the count of either Ø2 clock pulses or external events depending on the counter mode selected. The contents of Counter B may be read any time by executing a read at location 001D for the Upper Counter B and at location 001E or 001C for the Lower Counter B. A read at location 001C also clears the Counter B Underflow Flag.

Latch B contains the counter initialization value, and can be loaded at any time by executing a write to the Upper Latch B at location 001D and the Lower Latch B at location 001C. In each case, the contents of the accumulator are copied into the applicable latch register.

Counter B can be initialized at any time by writing to address: 001E. The contents of the accumulator is copied into the Upper Latch B before the value in the 16-bit Latch B is transferred to Counter B. Counter B will also be set to the latch value and the Counter B Underflow Flag bit (IFR5) will be set to a "1" whenever Counter B underflows by decrementing from 0000.

IFR 5 may be cleared by reading the Lower Counter B at location 001C, by writing to address location 001E, or by $\overline{RES}$.

Counter B operates in the same manner as Counter A in the Interval Timer and Event Counter modes. The Pulse Width Measurement Mode is replaced by the Retriggerable Interval Timer mode and the Pulse Generation mode is replaced by the Asymmetrical Pulse Generation Mode.

6.2.1 Retriggerable Interval Timer Mode

When operating in the Retriggerable Interval Timer mode, Counter B is initialized to the latch value by writing to address 001E, by a Counter B underflow, or whenever a positive edge occurs on the CB pin (PA5). The Counter B interrupt flag will be set if the counter underflows before a positive edge occurs on the CB line. Figure 6-4 illustrates the operation.

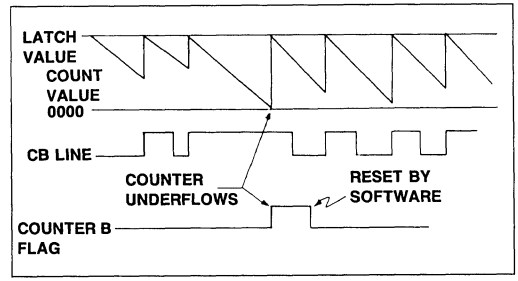


Figure 6-4. Counter B. Retriggerable Interval Timer Mode

6.2.2 Asymmetrical Pulse Generation Mode

Counter B has a special Asymmetrical Pulse Generation Mode whereby a pulse train with programmable pulse width and period can be generated without the processor intervention once the latch values are initialized.

In this mode, the 16-bit Latch B is initialized with a value which corresponds to the duration between pulses (referred to as D in the following descriptions). The 16-bit Latch C is initialized with a value which corresponds to the desired pulse width (referred to as P in the following descriptions). The initialization sequence for Latch B and C and the starting of a counting sequence are as follows:

1. The lower 8 bits of P are loaded into LLB by writing to address 001C, and the upper 8 bits of P are loaded into ULB and the full 16 bits are transferred to Latch C by writing to address location 001D. At this point both Latch B and Latch C contain the value of P.
2. The lower 8 bits of D are loaded into LLB by writing to address 001C, and the upper 8 bits of D are loaded into ULB by writing to address location 001E. Writing to address location 001E also causes the contents of the 16-bit Latch B to be downloaded into the Counter B and causes the CB output to go low as shown in Figure 6-5.
3. When the Counter B underflow occurs the contents of the Latch C is loaded into the Counter B, and the CB output toggles to a high level and stays high until another underflow occurs. Latch B is then down-loaded and the CB output toggles to a low level repeating the whole process.

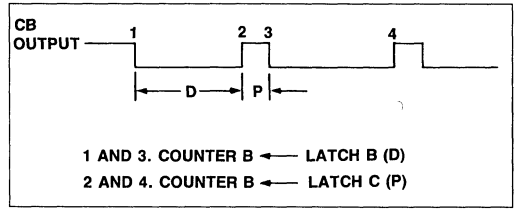


Figure 6-5. Counter B Pulse Generation

SECTION 7
POWER ON/INITIALIZATION CONSIDERATIONS

7.1 POWER-ON-RESET

The occurrence of $\overline{RES}$ going from low to high will cause the R65F11 or R65F12 to reset and enter the RSC-FORTH Operating System. As was described in Section 3.8, upon reset certain system variables will be initialized. See Appendix C.4 for a list of these variables names, locations and contents. The external memory map will be searched for an auto start ROM.

A bit pattern of A55A at a 1K byte page boundary indicates that an auto start program follows. The next two bytes are assumed to be a pointer to the high level RSC-FORTH word that is the entry point to that program. Auto start programs is written in assembly language, rather than RSC-FORTH, a series of indirect pointers as shown in 3-7 can be used to initiate program execution.

7.2 POWER ON TIMING

After application of V_{CC} and V_{RR} power to the R65F11 or R65F12, $\overline{RES}$ must be held low for at least eight $\phi 2$ clock cycles after V_{CC} reaches operating range and the internal oscillator has stabilized. This stabilization time is dependent upon the input V_{CC} voltage and performance of the internal oscillator. The clock can be monitored at $\phi 2$ (pin 3). Figure 7-1 illustrates the power turn-on waveforms. Clock stabilization time is typically 20 ms.

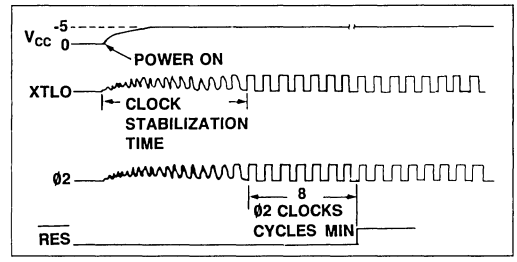


Figure 7-1. Power Turn-On Timing Detail

7.3 RESET ($\overline{RES}$) CONDITIONING

When $\overline{RES}$ is driven from low to high the R65F11 or R65F12 is put in a reset state. The registers and I/O ports are configured as shown in Table 7-1 when the external ROM is autostarted.

Table 7-1. RES Initialization of I/O Ports and Registers

	7	6	5	4	3	2	1	0
REGISTERS								
Mode Control (MCR)	1	1	1	0	0	0	0	0
Int. Enable (IER)	0	0	0	0	0	0	0	0
Int. Flag (IFR)	0	0	0	0	0	0	0	0
Ser. Com. Control (SCCR)	1	1	0	0	0	1	0	0
Ser. Com. Status (SCSR)	0	1	0	0	0	0	0	0
PORTS								
PA Latch	1	1	1	1	1	1	1	1
PB Latch	1	1	1	1	1	1	1	1

APPENDIX A
R65F11 AND R65F12 INSTRUCTION SET

This appendix contains a summary of the R6500 instruction set. For detailed information, consult the R6500 Microcomputer System Programming Manual, Document 29650 N30. The four instructions notated with a * are added instructions for the R65F11 and R65F12 which are not part of the standard 6502 instruction set.

A.1 INSTRUCTION SET IN ALPHABETIC SEQUENCE

Mnemonic	Instruction	Mnemonic	Instruction
ADC	Add Memory to Accumulator with Carry	LDA	Load Accumulator with Memory
AND	"AND" Memory with Accumulator	LDX	Load Index X with Memory
ASL	Shift Left One Bit (Memory or Accumulator)	LDY	Load Index Y with Memory
		LSR	Shift One Bit Right (Memory or Accumulator)
*BBR	Branch on Bit Reset Relative		
*BBS	Branch on Bit Set Relative		
BCC	Branch on Carry Clear	NOP	No Operation
BCS	Branch on Carry Set		
BEQ	Branch on Result Zero	ORA	"OR" Memory with Accumulator
BIT	Test Bits in Memory with Accumulator		
BMI	Branch on Result Minus	PHA	Push Accumulator on Stack
BNE	Branch on Result not Zero	PHP	Push Processor Status on Stack
BPL	Branch on Result Plus	PLA	Pull Accumulator from Stack
BRK	Force Break	PLP	Pull Processor Status from Stack
BVC	Branch on Overflow Clear		
BVS	Branch on Overflow Set	*RMB	Reset Memory Bit
		ROL	Rotate One Bit Left (Memory or Accumulator)
CLC	Clear Carry Flag		
CLD	Clear Decimal Mode	ROR	Rotate One Bit Right (Memory or Accumulator)
CLI	Clear Interrupt Disable Bit		
CLV	Clear Overflow Flag	RTI	Return from Interrupt
CMP	Compare Memory and Accumulator	RTS	Return from Subroutine
CPX	Compare Memory and Index X		
CPY	Compare Memory and Index Y	SBC	Subtract Memory from Accumulator with Borrow
DEC	Decrement Memory by One	SEC	Set Carry Flag
DEX	Decrement Index X by One	SED	Set Decimal Mode
DEY	Decrement Index Y by One	SEI	Set Interrupt Disable Status
		*SMB	Set Memory Bit
EOR	"Exclusive-Or" Memory with Accumulator	STA	Store Accumulator in Memory
		STX	Store Index X in Memory
		STY	Store Index Y in Memory
INC	Increment Memory by One		
INX	Increment Index X by One	TAX	Transfer Accumulator to Index X
INY	Increment Index Y by One	TAY	Transfer Accumulator to Index Y
		TSX	Transfer Stack Pointer to Index X
JMP	Jump to New Location	TXA	Transfer Index X to Accumulator
JSR	Jump to New Location Saving Return Address	TXS	Transfer Index X to Stack Register
		TYA	Transfer Index Y to Accumulator

A.2 R65F11 AND R65F12 INSTRUCTION SET SUMMARY TABLE

R65F11 AND R65F12 ADDRESS MODES

INSTRUCTIONS		IMMEDIATE			ABSOLUTE			ZERO PAGE			ACCUM.			IMPLIED			(IND, X)			(IND), Y			Z. PAGE, X			ABS, X			ABS, Y			RELATIVE			INDIRECT			Z. PAGE, Y			BIT ADDRESSING (OP BY BIT #)								PROCESSOR STATUS CODES 7 6 5 4 3 2 1 0
MNEMONIC	OPERATION	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	0	1	2	3	4	5	6	7	N V · B D I Z C
ADC	A · M · C→A (4)(1)	69	2	2	6D	4	3	65	3	2							61	6	2	71	5	2	75	4	2	7D	4	3	79	4	3																		N V · · · · Z C
AND	A M→A (1)	29	2	2	2D	4	3	25	3	2							21	6	2	31	5	2	35	4	2	3D	4	3	39	4	3																		N · · · · · Z ·
ASL	C← [7 0] ←0				0E	6	3	06	5	2	0A	2	1										16	6	2	1E	7	3																					N · · · · · Z C
BBR[#(0-7)]	Branch on M_b = 0 (5)(2)																																								0F	1F	2F	3F	4F	5F	6F	7F	· · · · · · · ·
BBS[#(0-7)]	Branch on M_b = 1 (5)(2)																																								8F	9F	AF	BF	CF	DF	EF	FF	· · · · · · · ·
BCC	Branch on C = 0 (2)																															90	2	2																· · · · · · · ·
BCS	Branch on C = 1 (2)																															B0	2	2																· · · · · · · ·
BEQ	Branch on Z = 1 (2)																															F0	2	2																· · · · · · · ·
BIT	A ∧ M				2C	4	3	24	3	2																																								M M, · · · · Z ·
BMI	Branch on N = 1 (2)																															30	2	2																· · · · · · · ·
BNE	Branch on Z = 0 (2)																															D0	2	2																· · · · · · · ·
BPL	Branch on N = 0 (2)																															10	2	2																· · · · · · · ·
BRK	Break													00	7	1																																		· · · 1 · 1 · ·
BVC	Branch on V = 0 (2)																															50	2	2																· · · · · · · ·
BVS	Branch on V = 1 (2)																															70	2	2																· · · · · · · ·
CLC	0→C													18	2	1																																		· · · · · · · 0
CLD	0→D													D8	2	1																																		· · · · 0 · · ·
CLI	0→I													58	2	1																																		· · · · · 0 · ·
CLV	0→V													B8	2	1																																		· 0 · · · · · ·
CMP	A M (1)	C9	2	2	CD	4	3	C5	3	2							C1	6	2	D1	5	2	D5	4	2	DD	4	3	D9	4	3																		N · · · · · Z C
CPX	X M	E0	2	2	EC	4	3	E4	3	2																																								N · · · · · Z C
CPY	Y M	C0	2	2	CC	4	3	C4	3	2																																								N · · · · · Z C
DEC	M 1→M				CE	6	3	C6	5	2													D6	6	2	DE	7	3																					N · · · · · Z ·
DEX	X 1→X													CA	2	1																																		N · · · · · Z ·
DEY	Y 1→Y													88	2	1																																		N · · · · · Z ·
EOR	A⊻M→A (1)	49	2	2	4D	4	3	45	3	2							41	6	2	51	5	2	55	4	2	5D	4	3	59	4	3																		N · · · · · Z ·
INC	M · 1→M				EE	6	3	E6															F6	6	2	FE	7	3																					N · · · · · Z ·
INX	X · 1→X													E8	2	1																																		N · · · · · Z ·
INY	Y · 1→Y													C8	2	1																																		N · · · · · Z ·
JMP	Jump to New Loc				4C	3	3																												6C	5	3													· · · · · · · ·
JSR	Jump Sub				20	6	3																																											· · · · · · · ·
LDA	M→A (1)	A9	2	2	AD	4	3	A5	3	2							A1	6	2	B1	5	2	B5	4	2	BD	4	3	B9	4	3																		N · · · · · Z ·
LDX	M→X (1)	A2	2	2	AE	4	3	A6	3	2																			BE	4	3							B6	4	2									N · · · · · Z ·
LDY	M→Y (1)	A0	2	2	AC	4	3	A4	3	2													B4	4	2	BC	4	3																					N · · · · · Z ·
LSR	0→ [7 0] → C				4E	6	3	46	5	2	4A	2	1										56	6	2	5E	7	3																					0 · · · · · Z C
NOP	No Operation													EA	2	1																																		· · · · · · · ·
ORA	AVM→A (1)	09	2	2	0D	4	3	05	3	2							01	6	2	11	5	2	15	4	2	1D	4	3	19	4	3																		N · · · · · Z ·
PHA	A→Ms S 1→S													48	3	1																																		· · · · · · · ·
PHP	P→Ms S 1→S													08	3	1																																		· · · · · · · ·
PLA	S · 1→S Ms→A													68	4	1																																		N · · · · · Z ·
PLP	S · 1→S Ms→P													28	4	1																																		(Restored)
RMB[#(0-7)]	0→M_b (5)																																								07	17	27	37	47	57	67	77	· · · · · · · ·
ROL	[7 0] ← [C]				2E	6	3	26	5	2	2A	2	1										36	6	2	3E	7	3																					N · · · · · Z C
ROR	[C] → [7 0]				6E	6	3	66	5	2	6A	2	1										76	6	2	7E	7	3																					N · · · · · Z C
RTI	Rtrn Int													40	6	1																																		(Restored)
RTS	Rtrn Sub													60	6	1																																		· · · · · · · ·
SBC	A M C→A (1) (4)	E9	2	[illegible]	ED	4	3	E5	3	2							E1	6	2	F1	5	2	F5	4	2	FD	4	3	F9	4	3																		N V · · · · Z (3)
SEC	1→C													38	2	1																																		· · · · · · · 1
SED	1→D													F8	2	1																																		· · · · 1 · · ·
SEI	1→T													78	2	1																																		· · · · · 1 · ·
SMB[#(0-7)]	1→M_b (5)																																								87	97	A7	B7	C7	D7	E7	F7	· · · · · · · ·
STA	A→M				8D	4	3	85	3	2							81	6	2	91	6	2	95	4	2	9D	5	3	[illegible]	5	3																		· · · · · · · ·
STX	X→M				8E	4	3	86	3	2																												96	4	2									· · · · · · · ·
STY	Y→M				8C	4	3	84	3	2													94	4	2																								· · · · · · · ·
TAX	A→X													AA	2	1																																		N · · · · · Z ·
TAY	A→Y													A8	2	1																																		N · · · · · Z ·
TSX	S→X													BA	2	1																																		N · · · · · Z ·
TXA	X→A													8A	2	1																																		N · · · · · Z ·
TXS	X→S													9A	2	1																																		· · · · · · · ·
TYA	Y→A													98	2	1																																		N · · · · · Z ·

NOTES

1. Add 1 to N if page boundary is crossed
2. Add 1 to N if branch occurs to same page
   Add 2 to N if branch occurs to different page
3. Carry not = Borrow
4. If in decimal mode Z flag is invalid
   accumulator must be checked on zero result
5. Effects 8-bit data field of the specified zero page address

LEGEND

X = Index X
Y = Index Y
A = Accumulator
M = Memory per effective address
M_s = Memory per stack pointer
M_b = Selecter zero page memory bit
M_7 = Memory Bit 7
M_6 = Memory Bit 6
· = Add
– = Subtract
∧ = And
V = Or
⊻ = Exclusive Or
n = Number of cycles
# = Number of Bytes

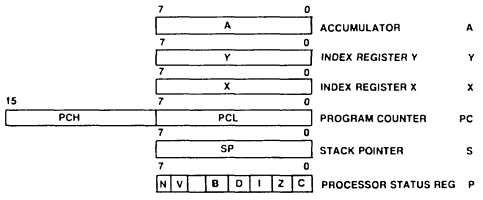
A.3 INSTRUCTION CODE MATRIX

MSD \ LSD	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	MSD
0	BRK Implied 1 7	ORA (IND, X) 2 6				ORA ZP 2 3	ASL ZP 2 5	RMB0 ZP 2 5	PHP Implied 1 3	ORA IMM 2 2	ASL Accum 1 2			ORA ABS 3 4	ASL ABS 3 6	BBR0 ZP 3 5**	0
1	BPL Relative 2 2**	ORA (IND), Y 2 5*				ORA ZP, X 2 4	ASL ZP, X 2 6	RMB1 ZP 2 5	CLC Implied 1 2	ORA ABS, Y 3 4*				ORA ABS, X 3 4*	ASL ABS, X 3 7	BBR1 ZP 3 5**	1
2	JSR Absolute 3 6	AND (IND, X) 2 6			BIT ZP 2 3	AND ZP 2 3	ROL ZP 2 5	RMB2 ZP 2 5	PLP Implied 1 4	AND IMM 2 2	ROL Accum 1 2		BIT ABS 3 4	AND ABS 3 4	ROL ABS 3 6	BBR2 ZP 3 5**	2
3	BMI Relative 2 2**	AND (IND, Y) 2 5*				AND ZP, X 2 4	ROL ZP, X 2 6	RMB3 ZP 2 5	SEC Implied 1 2	AND ABS, Y 3 4*				AND ABS, X 3 4*	ROL ABS, X 3 7	BBR3 ZP 3 5**	3
4	RTI Implied 1 6	EOR (IND, X) 2 6				EOR ZP 2 3	LSR ZP 2 5	RMB4 ZP 2 5	PHA Implied 1 3	EOR IMM 2 2	LSR Accum 1 2		JMP ABS 3 3	EOR ABS 3 4	LSR ABS 3 6	BBR4 ZP 3 5**	4
5	BVC Relative 2 2**	EOR (IND), Y 2 5*				EOR ZP, X 2 4	LSR ZP, X 2 6	RMB5 ZP 2 5	CLI Implied 1 2	EOR ABS, Y 3 4*				EOR ABS, X 3 4*	LSR ABS, X 3 7	BBR5 ZP 3 5**	5
6	RTS Implied 1 6	ADC (IND, X) 2 6				ADC ZP 2 3	ROR ZP 2 5	RMB6 ZP 2 5	PLA Implied 1 4	ADC IMM 2 2	ROR Accum 1 2		JMP Indirect 3 5	ADC ABS 3 4	ROR ABS 3 6	BBR6 ZP 3 5**	6
7	BVS Relative 2 2**	ADC (IND, Y) 2 5*				ADC ZP, X 2 4	ROR ZP, X 2 6	RMB7 ZP 2 5	SEI Implied 1 2	ADC ABS, Y 3 4*				ADC ABS, X 3 4*	ROR ABS, X 3 7	BBR7 ZP 3 5**	7
8		STA (IND, X) 2 6			STY ZP 2 3	STA ZP 2 3	STX ZP 2 3	SMB0 ZP 2 5	DEY Implied 1 2		TXA Implied 1 2		STY ABS 3 4	STA ABS 3 4	STX ABS 3 4	BBS0 ZP 3 5**	8
9	BCC Relative 2 2**	STA (IND, Y) 2 6			STY ZP, X 2 4	STA ZP, X 2 4	STX ZP, Y 2 4	SMB1 ZP 2 5	TYA Implied 1 2	STA ABS, Y 3 5	TXS Implied 1 2			STA ABS, X 3 5		BBS1 ZP 3 5**	9
A	LDY IMM 2 2	LDA (IND, X) 2 6	LDX IMM 2 2		LDY ZP 2 3	LDA ZP 2 3	LDX ZP 2 3	SMB2 ZP 2 5	TAY Implied 1 2	LDA IMM 2 2	TAX Implied 1 2		LDY ABS 3 4	LDA ABS 3 4	LDX ABS 3 4	BBS2 ZP 3 5**	A
B	BCS Relative 2 2**	LDA (IND), Y 2 5*			LDY. ZP, X 2 4	LDA ZP, X 2 4	LDX ZP, Y 2 4	SMB3 ZP 2 5	CLV Implied 1 2	LDA ABS, Y 3 4*	TSX Implied 1 2		LDY ABS, X 3 4*	LDA ABS, X 3 4*	LDX ABS, Y 3 4*	BBS3 ZP 3 5**	B
C	CPY IMM 2 2	CMP (IND, X) 2 6			CPY ZP 2 3	CMP ZP 2 3	DEC ZP 2 5	SMB4 ZP 2 5	INY Implied 1 2	CMP IMM 2 2	DEX Implied 1 2		CPY ABS 3 4	CMP ABS 3 4	DEC ABS 3 6	BBS4 ZP 3 5**	C
D	BNE Relative 2 2**	CMP (IND), Y 2 5*				CMP ZP, X 2 4	DEC ZP, X 2 6	SMB5 ZP 2 5	CLD Implied 1 2	CMP ABS, Y 3 4*				CMP ABS, X 3 4*	DEC ABS, X 3 7	BBS5 ZP 3 5**	D
E	CPX IMM 2 2	SBC (IND, X) 2 6			CPX ZP 2 3	SBC ZP 2 3	INC ZP 2 5	SMB6 ZP 2 5	INX Implied 1 2	SBC IMM 2 2	NOP Implied 1 2		CPX ABS 3 4	SBC ABS 3 4	INC ABS 3 6	BBS6 ZP 3 5**	E
F	BEQ Relative 2 2**	SBC (IND), Y 2 5*				SBC ZP, X 2 4	INC ZP, X 2 6	SMB7 ZP 2 5	SED Implied 1 2	SBC ABS, Y 3 4*				SBC ABS, X 3 4*	INC ABS, X 3 7	BBS7 ZP 3 5**	F
	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	

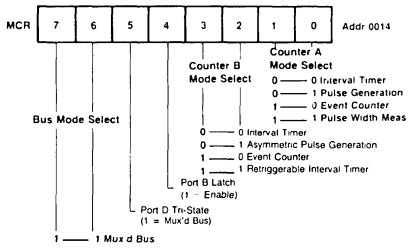
0	0
BRK Implied 1 7	—OP Code —Addressing Mode —Instruction Bytes; Machine Cycles

*Add 1 to N if page boundary is crossed.
**Add 1 to N if branch occurs to same page;
add 2 to N if branch occurs to different page.

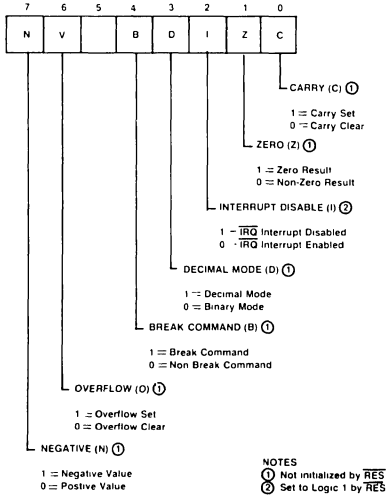
APPENDIX B
KEY REGISTER SUMMARY



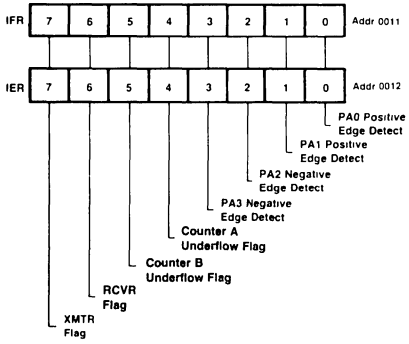
CPU Registers



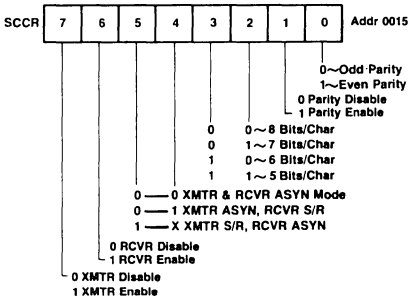
Mode Control Register



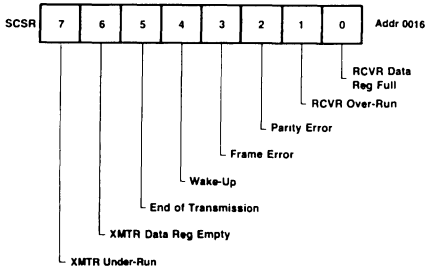
Processor Status Register



Interrupt Enable and Flag Registers



Serial Communications Control Register



Serial Communications Status Register

APPENDIX C
ADDRESS ASSIGNMENTS/MEMORY MAPS/PIN FUNCTIONS

C.1 I/O AND INTERNAL REGISTER ADDRESSES

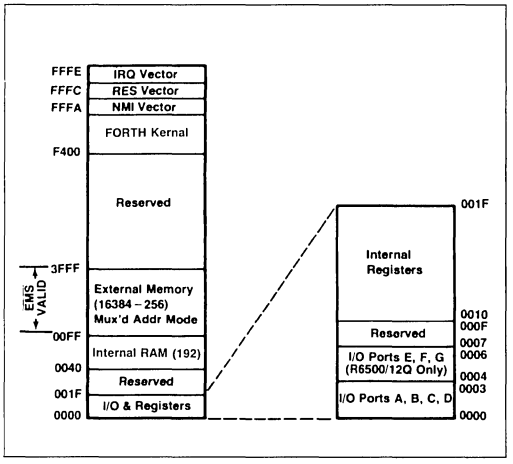
ADDRESS (HEX)	READ	WRITE
001F	— —	— —
1E	Lower Counter B	Upper Latch B, Cntr B←Latch B, CLR Flag
1D	Upper Counter B	Upper Latch B, Latch C←Latch B
1C	Lower Counter B, CLR Flag	Lower Latch B.
1B	— —	— —
1A	Lower Counter A	Upper Latch A, Cntr A←Latch A, CLR Flag
19	Upper Counter A	Upper Latch A
18	Lower Counter A, CLR Flag	Lower Latch A
17	Serial Receiver Data Register	Serial Transmitter Data Register
16	Serial Comm. Status Register	Serial Comm. Status Reg. Bits 4 & 5 only
15	Serial Comm. Control Register	Serial Comm. Control Register
14	Mode Control Register	Mode Control Register
13	— —	— —
12	Interrupt Enable Register	Interrupt Enable Register
11	Interrupt Flag Register	— —
10	Read FF	Clear Int Flag (Bits 0-3 only, Write 0's only)
0F	— —	— —
0E	— —	— —
0D	— —	— —
0C	— —	— —
0B	— —	— —
0A	— —	— —
09	— —	— —
08	— —	— —
07	— —	— —
06	Port G*	Port G*
05	Port F*	Port F*
04	Port E*	Port E*
03	— —	— —
02	— —	— —
01	Port B	Port B
0000	Port A	Port A

NOTE: *R65F12 Only

C.2 MULTIPLE FUNCTION PIN ASSIGNMENTS— PORT C AND PORT D

PIN NUMBER		I/O PORT FUNCTION	MULTIPLEXED PORT
R65F11	R65F12	REPLACED	FUNCTION
4	25	PC0	A0
5	26	PC1	A1
6	27	PC2	A2
7	28	PC3	A3
8	29	PC4	A12
9	30	PC5	R/W
10	31	PC6	A13
11	32	PC7	EMS
19	40	PD0	A4/D0
18	39	PD1	A5/D1
17	38	PD2	A6/D2
16	37	PD3	A7/D3
15	36	PD4	A8/D4
14	35	PD5	A9/D5
13	34	PD6	A10/D6
12	33	PD7	A11/D7

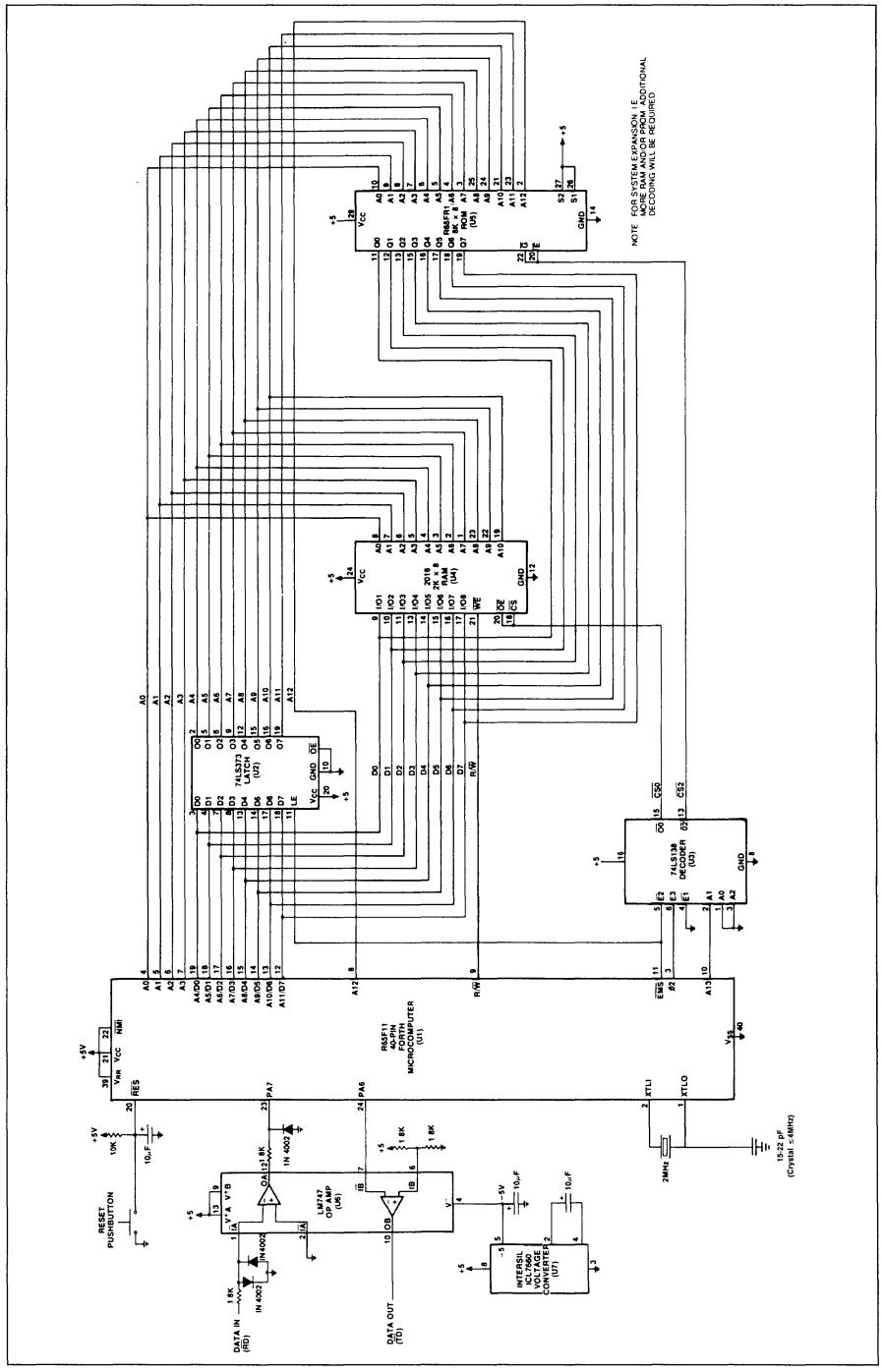
C.3 MULTIPLEXED MODE MEMORY MAP



C.4 SYSTEM VARIABLES IN RAM

ADDRESS	NAME	COLD START VALUE	WARM START VALUE
0040	IRQVEC	(COLD)	—
0042	NMIVEC	(COLD)	—
0044	UKEY	(INK)	(INK)
0046	UEMIT	(OUT)	(OUT)
0048	UP	0300	0300
004A	INTFLG	00	00
004B	(W-1)	6C	6C
004C	W	—	—
004E	IP	—	—
0050	(N-1)	—	—
0051	N	—	—
0059	XSAVE	—	—
005B	INTVEC	(COLD)	—
005D	TOS	—	—
0300	TIB	0380	0380
0302	R0	00FF	00FF
0304	S0	00C2	00C2
0306	UC/L	0050	—
0308	UPAD	037E	—
030A	UR/W	(DISK)	—
030C	BASE	0010	—
030E	CLD/WRM	—	—
0310	IN	—	—
0312	DPL	—	—
0314	HLD	—	—
0316	DISKNO	—	—
0318	CURCYL	—	—
031C	B/SIDE	—	—

APPENDIX D
TYPICAL MINIMUM HOOKUP



APPENDIX E
ELECTRICAL SPECIFICATIONS

MAXIMUM RATINGS*

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC} & V_{RR}	−0.3 to +7.0	Vdc
Input Voltage	V_{IN}	−0.3 to +7.0	Vdc
Operating Temperature Range, Commercial	T_A	T_L to T_H 0 to +70	°C
Storage Temperature	T_{STG}	−55 to +150	°C

***NOTE:** Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the other sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

3

DC CHARACTERISTICS

(V_{CC} = 5.0V ±5%, V_{RR} = V_{CC}; V_{SS} = 0V; T_A = 0° to 70°, unless otherwise specified)

Parameter	Symbol	Min	Typ[1]	Max	Unit	Test Conditions
RAM Standby Voltage (Retention Mode)	V_{RR}	3.0		V_{CC}	V	
RAM Standby Current (Retention Mode)	I_{RR}	—	4	—	mA	T_A = 25°C
Input High Voltage All Except XTLI XTLI	V_{IH}	 +2.0 +4.0	 — —	 V_{CC} V_{CC}	V	
Input Low Voltage	V_{IL}	−0.3	—	+0.8	V	
Input Leakage Current $\overline{RES}$, $\overline{NMI}$	I_{IN}	—	—	±10.0	μA	V_{IN} = 0 to 5.0V
Input Low Current PA, PB, PC, PD, PF[3], PG[3]	I_{IL}	—	−1.0	−1.6	mA	V_{IL} = 0.4V
Output High Voltage (Except XTLO)	V_{OH}	+2.4	—	V_{CC}	V	I_{LOAD} = −100 μA
Output Low Voltage	V_{OL}	—	—	+0.4	V	I_{LOAD} = 1.6 mA
I/O Port Pull-Up Resistance PA0–PA7, PB0–PB7, PC0–PC7, PF0–PF7[3], PG0–PG7[3]	R_L	3.0	6.0	11.5	Kohm	
Output Leakage Current (Three-State Off)	I_{OUT}	—	—	±10	μA	
Darlington Current Drive PE[3]	I_{OH}	−1.0	—	—	mA	V_{OUT} = 1.5V
Input Capacitance XTLI, XTLO All Others	C_{IN}	 — —	 — —	 50 10	pF	T_A = 25°C V_{IN} = 0V f = 1.0 MHz
Output Capacitance (Three-State Off)	C_{OUT}	—	—	10	pF	T_A = 25°C V_{IN} = 0V f = 1.0 MHz
Power Dissipation (Outputs High)	P_D	—		1000	mW	T_A = 25°C

Notes:
1. Typical values measured at T_A = 25°C and V_{CC} = 5.0V.
2. Negative sign indicates outward current flow, positive indicates inward flow.
3. R65F12 only.

APPENDIX F
TIMING REQUIREMENTS AND CHARACTERISTICS

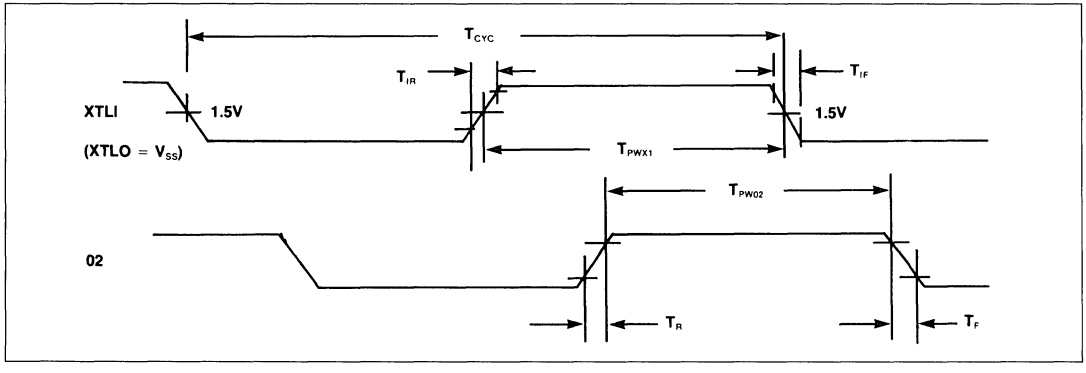
F.1 GENERAL NOTES

1. V_{CC} = 5V ± 5%, 0°C ≤ TA ≤ 70°C
2. A valid V_{CC} – RES sequence is required before proper operation is achieved.
3. All timing reference levels are 0.8V and 2.0V, unless otherwise specified.
4. All time units are nanoseconds, unless otherwise specified.
5. All capacitive loading is 130pf maximum, except as noted below:

   PA, PB, PE, PF, PG — 50pf maximum

F.2 CLOCK TIMING

SYMBOL	PARAMETER	1 MHz		2 MHz	
		MIN	MAX	MIN	MAX
T_{CYC}	Cycle Time	1000	10 μs	500	10 μs
T_{PWX1}	XTLI Input Clock Pulse Width XTLO = VSS	500 ± 25	—	250 ± 10	—
T_{PW02}	Output Clock Pulse Width at Minimum T_{CYC}	T_{PWX1}	T_{PWX1} ± 25	T_{PWX1}	T_{PWX1} ± 20
T_R, T_F	Output Clock Rise, Fall Time	—	25	—	15
T_{IR}, T_{IF}	Input Clock Rise, Fall Time	—	10	—	10



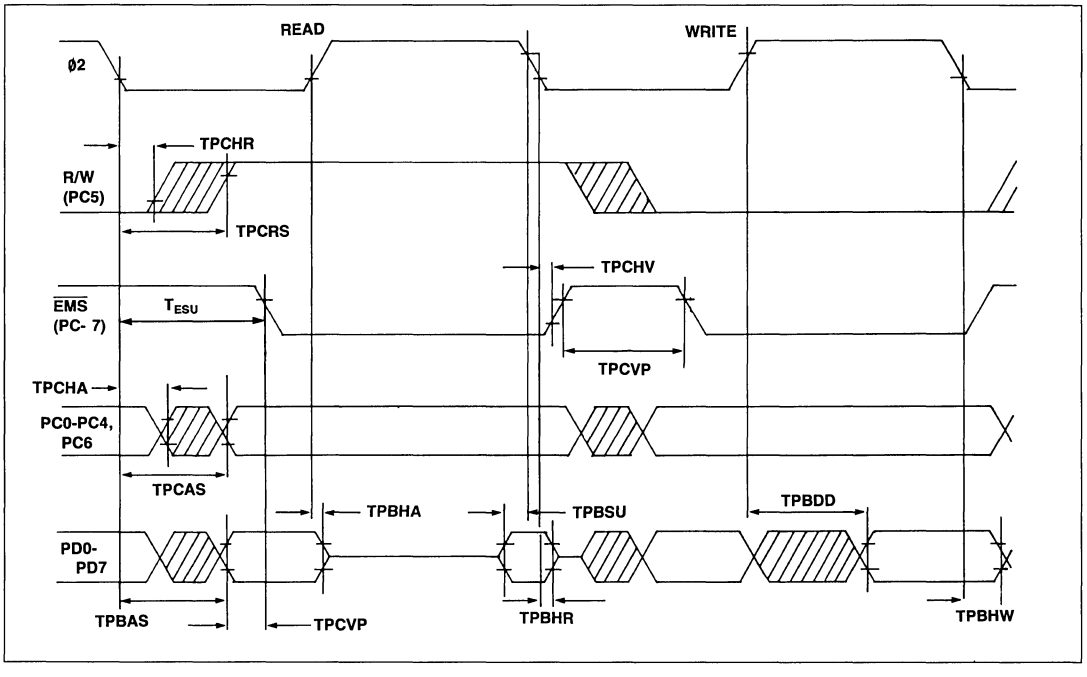
F.3 MULTIPLEXED MODE TIMING—PC AND PD

(MCR 5 = 1, MCR 6 = 1, MCR 7 = 1)

SYMBOL	PARAMETER	1 MHz		2 MHz	
		MIN	MAX	MIN	MAX
T_{PCRS}	(PC5) R/W Setup Time	—	225	—	140
T_{PCAS}	(PC0-PC4, PC6) Address Setup Time	—	225	—	140
T_{PBAS}	(PD) Address Setup Time	—	225	—	140
T_{PBSU}	(PD) Data Setup Time	50	—	35	—
T_{PBHR}	(PD) Data Read Hold Time	10	—	10	—
T_{PBHW}	(PD) Data Write Hold Time	30	—	30	—
T_{PBDD}	(PD) Data Output Delay	—	175	—	150
T_{PCHA}	(PC0-PC4, PC6) Address Hold Time	30	—	30	—
T_{PBHA}	(PD) Address Hold Time	10	100	10	80
T_{PCHR}	(PC5) R/W Hold Time	30	—	30	—
T_{PCHV}	(PC7) EMS Hold Time	10	—	10	—
T_{PCVD} (1)	(PC7) Address to EMS Delay Time	30	—	30	—
T_{PCVP}	(PC7) EMS Stabilization Time	30	—	30	—
T_{ESU}	$\overline{EMS}$ Set Up Time	—	350	—	210

NOTE 1: Values assume PC0-PC4, PC6 and PC7 have the same capacitive load.

F.3.1 Multiplex Mode Timing Diagram

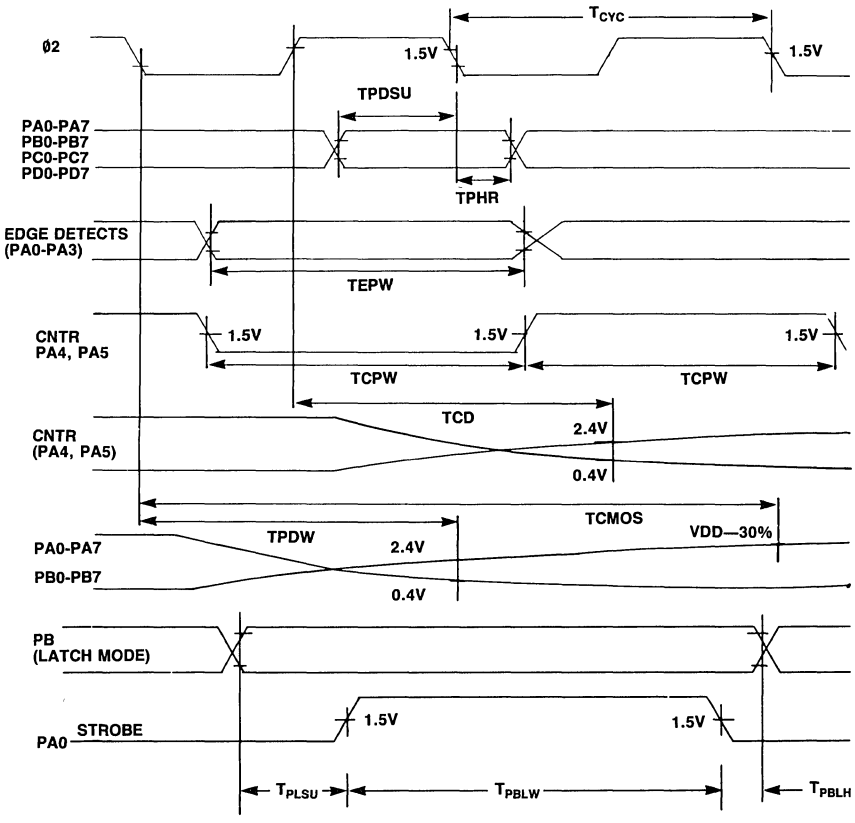


F.4 I/O, EDGE DETECT, COUNTERS, AND SERIAL I/O TIMING

SYMBOL	PARAMETER	1 MHz		2 MHz	
		MIN	MAX	MIN	MAX
	Internal Write to Peripheral Data Valid				
T_{PDW}[1]	PA, PB TTL	—	500	—	500
T_{CMOS}[1]	PA, PB CMOS	—	1000	—	1000
	Peripheral Data Setup Time				
T_{PDSU}	PA, PB	200	—	200	—
	Peripheral Data Hold Time				
T_{PHR}	PA, PB	75	—	75	—
T_{EPW}	PA0-PA3 Edge Detect Pulse Width	T_{CYC}	—	T_{CYC}	—
	Counters A and B				
T_{CPW}	PA4, PA5 Input Pulse Width	T_{CYC}	—	T_{CYC}	—
T_{CD}[1]	PA4, PA5 Output Delay	—	500	—	500
	Port B Latch Mode				
T_{PBLW}	PA0 Strobe Pulse Width	T_{CYC}	—	T_{CYC}	—
T_{PLSU}	PB Data Setup Time	175	—	150	—
T_{PBLH}	PB Data Hold Time	30	—	30	—
	Serial I/O				
T_{PDW}[1]	PA6 XMTR TTL	—	500	—	500
T_{CMOS}[1]	PA6 XMTR CMOS	—	1000	—	1000
T_{CPW}	PA4 RCVR S/R Clock Width	4 T_{CYC}	—	4 T_{CYC}	—
T_{PDW}[1]	PA4 XMTR Clock—S/R Mode (TTL)	—	500	—	500
T_{CMOS}[1]	PA4 XMTR Clock—S/R Mode (CMOS)	—	1000	—	1000

NOTE 1: Maximum Load Capacitance: 50pF Passive Pull-Up Required.

F.4.1 I/O Edge Detect, Counter, and Serial I/O Timing



APPENDIX G
INCLUDED FORTH FUNCTIONS IN ROM

BANKEXECUTE	BANKEEC!	BANKC@	BANKC!
EEC!	•	.R	D.
?	#S	#	SIGN
D.R	<#	SPACES	SEEK
#>	DWRITE	DREAD	SELECT
INIT	M/MOD	*/	*/MOD
DISK	/	/MOD	*
MOD	M*	MAX	MIN
M/	ABS	D+-	+-
DABS	COLD	(NUMBER)	HOLD
S->D	ERASE	FILL	QUERY
BLANKS	(.")	-TRAILING	TYPE
EXPECT	DECIMAL	HEX	-DUP
COUNT	PICK	ROT	>
SPACE	U<	=	-
<	1-	2+	1+
2-	C/L	HLD	DPL
PAD	CLD/WRM	BASE	UR/W
IN	UC/L	R0	S0
UPAD	BL	4	3
TIB	1	0	C!
2	C@	@	TOGGLE
!	BOUNDS	2DUP	DUP
+!	2DROP	DROP	OVER
SWAP	NEGATE	D+	+
DNEGATE	0=	R	R>
0<	LEAVE	;S	RP@
>R	SP!	SP@	XOR
RP!	AND	U/	U*
OR	CR	?TERMINAL	KEY
CMOVE	ENCLOSE	(FIND)	DIGIT
EMIT	(+LOOP)	(LOOP)	0BRANCH
(DO)	EXECUTE	CLIT	LIT
BRANCH			

Rockwell

R65FRx and R65FKx RSC FORTH Development and Kernel ROMS

INTRODUCTION

The Rockwell Single Chip (RSC) FORTH System can be configured using the R65F11, R65F12 microcomputers or the R6501Q ROM-less microcomputer. One of these microcomputers, when used in conjunction with a development ROM and a FORTH kernel ROM, provide the designer with maximum flexibility when developing FORTH applications.

RSC-FORTH is based on the popular fig-FORTH model with extensions. The R65F11 and R65F12 both have the kernel of the high level Rockwell Single Chip RSC-FORTH language contained in the preprogrammed ROM. The R65FK2 and R65FK3 Kernel ROMs are preprogrammed ROMs for use with the R6501Q when developing larger applications requiring more memory and I/O line support. All of the run time functions of the RSC-FORTH are contained in these ROMs, including 16- and 32-bit mathematical, logical and stack manipulation, plus memory and input/output operators. The RSC-FORTH Operating System allows an external user program written in RSC-FORTH or Assembly Language to be executed from external EPROM, or development of such a program under the control of the R65FR1, R65FR2 or R65FR3 RSC-FORTH Development ROMs.

This document describes five different RSC-FORTH system configurations using the development and kernel ROMs.

ORDERING INFORMATION

Part No.	Description
R65FR1P	FORTH Development ROM for R65F11 or R65F12
R65FR2P	FORTH Development ROM for R6501Q
R65FR3P	FORTH Development ROM for R6501Q
R65FK2P	FORTH Kernel ROM for R6501Q
R65FK3P	FORTH Kernel ROM for R6501Q
R65F11P	40-Pin FORTH Based Microcomputer at 1 MHz
R65F11AP	40-Pin FORTH Based Microcomputer at 2 MHz
R65F12Q	64-Pin FORTH Based Microcomputer at 1 MHz
R65F12AQ	64-Pin FORTH Based Microcomputer at 2 MHz
R6501Q	64-Pin One-Chip Microprocessor at 1 MHz
R6501AQ	64-Pin One-Chip Microprocessor at 2 MHz
Order No.	**Description**
2145	R6501Q One-Chip Microprocessor Product Description
2146	R65F11 and R65F12 FORTH Based Microcomputer Product Description
2148	RSC-FORTH User's Manual
2162	Application Note: A Low-Cost Development Module for the R65F11 FORTH Microcomputer

FEATURES

- R65FR1 FORTH Development ROM
  - —8K ROM
  - —Addressable from $2000 through $3FFF in FORTH development configuration memory map
  - —R65F11 and R65F12 compatible
  - —Operates in the R65F11/F12 FORTH development configuration
- R65FR2 FORTH Development ROM
  - —8K ROM
  - —Addressable from $4000 through $5FFF in the FORTH development configuration memory map
  - —R6501Q compatible for use in emulation of the R65F11/F12 FORTH development configuration
- R65FR3 FORTH Development ROM
  - —8K ROM
  - —Addressable from $C000 through $DFFF in the FORTH development configuration memory map
  - —Operates in the R6501Q FORTH development configuration
- R65FK2 FORTH Kernel ROM
  - —4K ROM
  - —Addressable from $F400 through $FFFF in the FORTH development configuration memory map
  - —R6501Q compatible for use in the emulation of the R65F11/F12 FORTH development configuration
  - —Replaces the FORTH kernel contained in the R65F11 and R65F12 microcomputers during development
- R65FK3 FORTH Kernel ROM
  - —4K ROM
  - —Addressable from $F400 through $FFFF in the FORTH development and production configuration memory maps
  - —R6501Q compatible
  - —Operates in the R6501Q FORTH development and production configurations

RSC-FORTH SYSTEM CONFIGURATIONS

The three configurations of the RSC-FORTH System are identified by the CPU-Development ROM combinations listed below:

RSC-FORTH System Configurations

CPU	Kernel ROM	Development ROM	RSC Configuration
R65F11	none	R65FR1	1
R65F12	none	R65FR1	1
R6501Q	R65FK2	R65FR2	2
R6501Q	R65FK3	R65FR3	3

RSC-FORTH CONFIGURATION 1 (R65FR1)

R65F11/R65F12 DEVELOPMENT AND PRODUCTION

The RSC-FORTH Configuration 1 provides the designer with a FORTH development and application environment at a minimal cost. The application program is developed using an R65F11 or R65F12 microcomputer, an R65FR1 Development ROM and external RAM. Up to 8K bytes of RAM space is available using this configuration. However, Configuration 1 is limited to 5K or less bytes of RAM during development. This is the result of allocating 2K bytes of RAM for disk buffers and at least 1K bytes of RAM for the "Program heads". The program heads are contained in a dictionary containing the Name (NFA), Link Field Address (LFA) and the Parameter Field Address Pointer (PFA). This dictionary is a list of FORTH word words and user-defined FORTH words used in the development of a FORTH program and is not present during the execution of the FORTH program.

Although programs may reside in the upper 8K bytes of memory area, normally filled by the R65FR1 Development ROM, it is difficult to develop code for that area using this configuration of the RSC-FORTH System.

The difference in using the R65F11 or the R65F12 is in the number of I/O lines available to the user. The R65F11 supports 16 I/O lines, the R65F12 supports 40 I/O lines.

Figure 1 shows the development and production configurations for the R65F11/F12. Configurations 1A and 1B list the features, memory maps, and the relationship of the R65F11 and R65F12 to the R65FR1 Development ROM in the development and production environment.

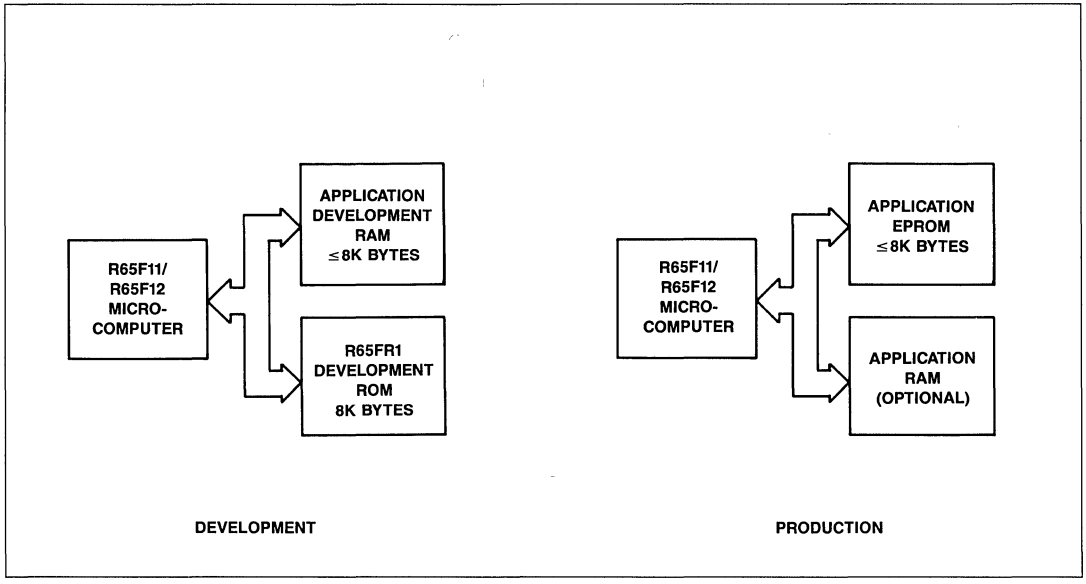


Figure 1. R65FR1 Configuration 1 Block Diagram

CONFIGURATION 1A CONSIDERATIONS

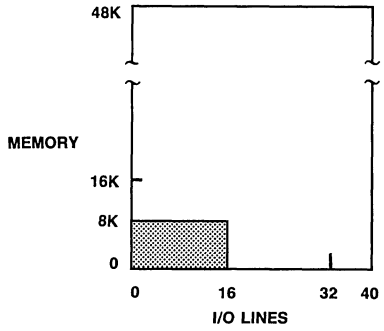
Features
- 8K Bytes of User Memory
- 16 I/O Lines

Device Configuration

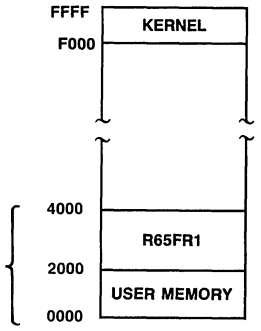
	DEVELOPMENT	PRODUCTION
R65F11 Microcomputer	✓	✓
R65FR1 Development ROM	✓	

User Memory—I/O Resource Matrix

User memory may be a mix of ROM, EEROM, UVPROM or RAM.



Memory Map



CONFIGURATION 1B CONSIDERATIONS

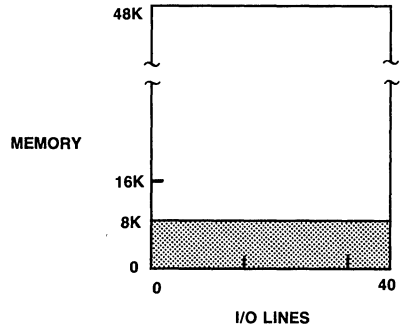
Features
- 8K Bytes of User Memory
- 40 I/O Lines

Device Configuration

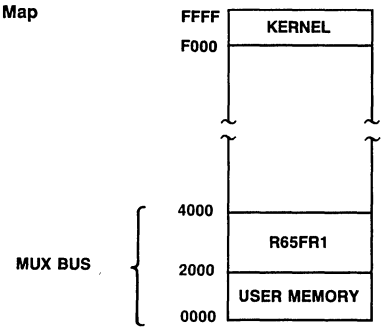
	DEVELOPMENT	PRODUCTION
R65F12 Microcomputer	✓	✓
R65FR1 Development ROM	✓	

User Memory—I/O Resource Matrix

User memory may be a mix of ROM, EEROM, UVPROM or RAM.



Memory Map



3

RSC-FORTH CONFIGURATION 2 (R65FR2, R65FK2)

R6501Q DEVELOPMENT AND R65F11/F12 PRODUCTION

The RSC-FORTH Configuration 2 provides the designer with the capability of using the full 16K bytes of external address space of the R65F11 and R65F12.

The R6501Q ROM-less microprocessor, when used with the R65FK2 Kernel ROM and the R65FR2 Development ROM, emulates the operation of the R65F11/F12. Because of the greater address space of the R6501Q, the R65FR2 Development ROM can be relocated to address $4000 and the disk buffers and HEADS program to $6000. This expands the available user memory space to 16K bytes, $0000 through $3FFF.

Using this configuration, the application program can be developed using the R6501Q and then later installed in an R65F11 or R65F12 microcomputer without modification.

Figure 2 shows the development and production configuration for the R6501Q. Configurations 2A and 2B list the features, memory maps, and the relationship of the R6501Q to the R65FR2 Development ROM and R65FK2 Kernel ROM in the development and production environment. Figure 3 is a schematic of the R6501Q, R65FR2, R65FK2 development setup designed to plug into a 40 pin socket in place of the R65F11.

Note: Ports E, F and G of the R65F12 are not present on the R6501Q and must be emulated by external TTL logic. Contact Rockwell for further information.

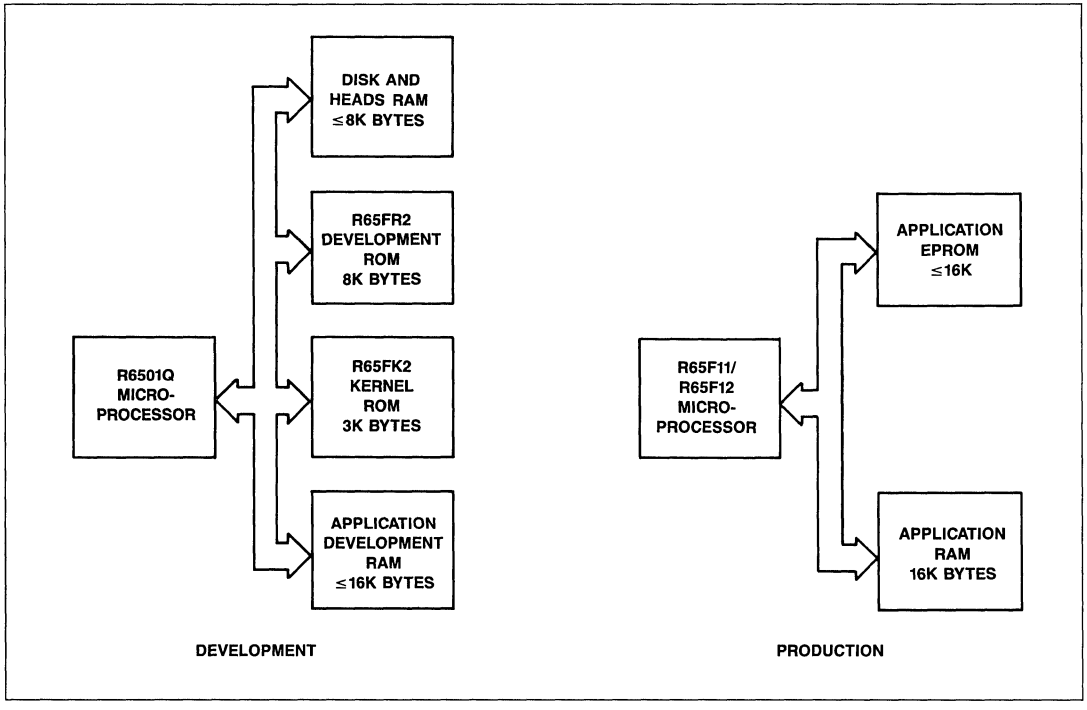


Figure 2. R65FR2 and R65FK2 Configuration 2 Block Diagrams

CONFIGURATION 2A CONSIDERATIONS

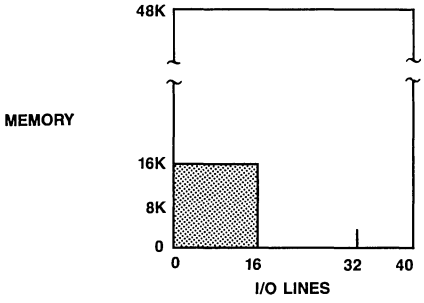
Features
- 16K Bytes of User "Headerless" Memory
- 16 I/O Lines

Device Configuration

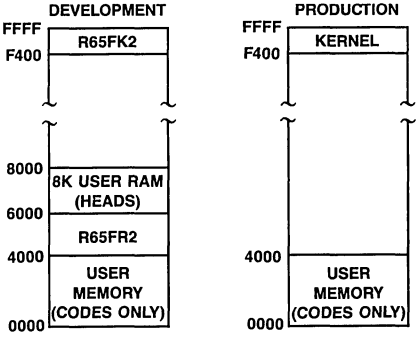
	DEVELOPMENT	PRODUCTION
R65F11 Microcomputer		✓
R6501Q Microprocessor	✓	
R65FR2 Development ROM	✓	
R65FK2 Kernel ROM	✓	

Memory—I/O Matrix

If floppy disk is used in the application, space for the disk buffers must be allocated in memory from $0500 through $3FFF or $6000 through $7FFF. User memory can be a mix of ROM, EEROM, UVROM or RAM.



Memory Maps



CONFIGURATION 2B CONSIDERATIONS

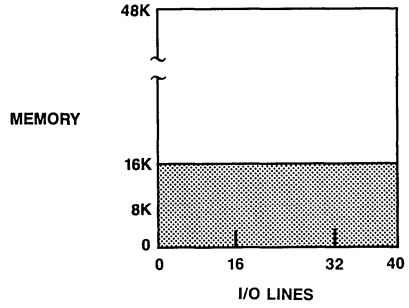
Features
- 16K Bytes of User "Headerless" Memory
- 40 I/O Lines

Device Configuration

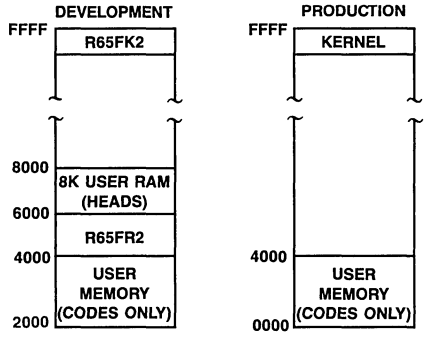
	DEVELOPMENT	PRODUCTION
R65F12 Microcomputer		✓
R6501Q Microprocessor	✓	
R65FR2 Development ROM	✓	
R65FK2 Kernel ROM	✓	

Memory—I/O Matrix

If floppy disk is used in the application, space for the disk buffers must be allocated in memory $0000 through $3FFF. User memory can be a mix of ROM, EEROM, UVROM or RAM.



Memory Maps



3

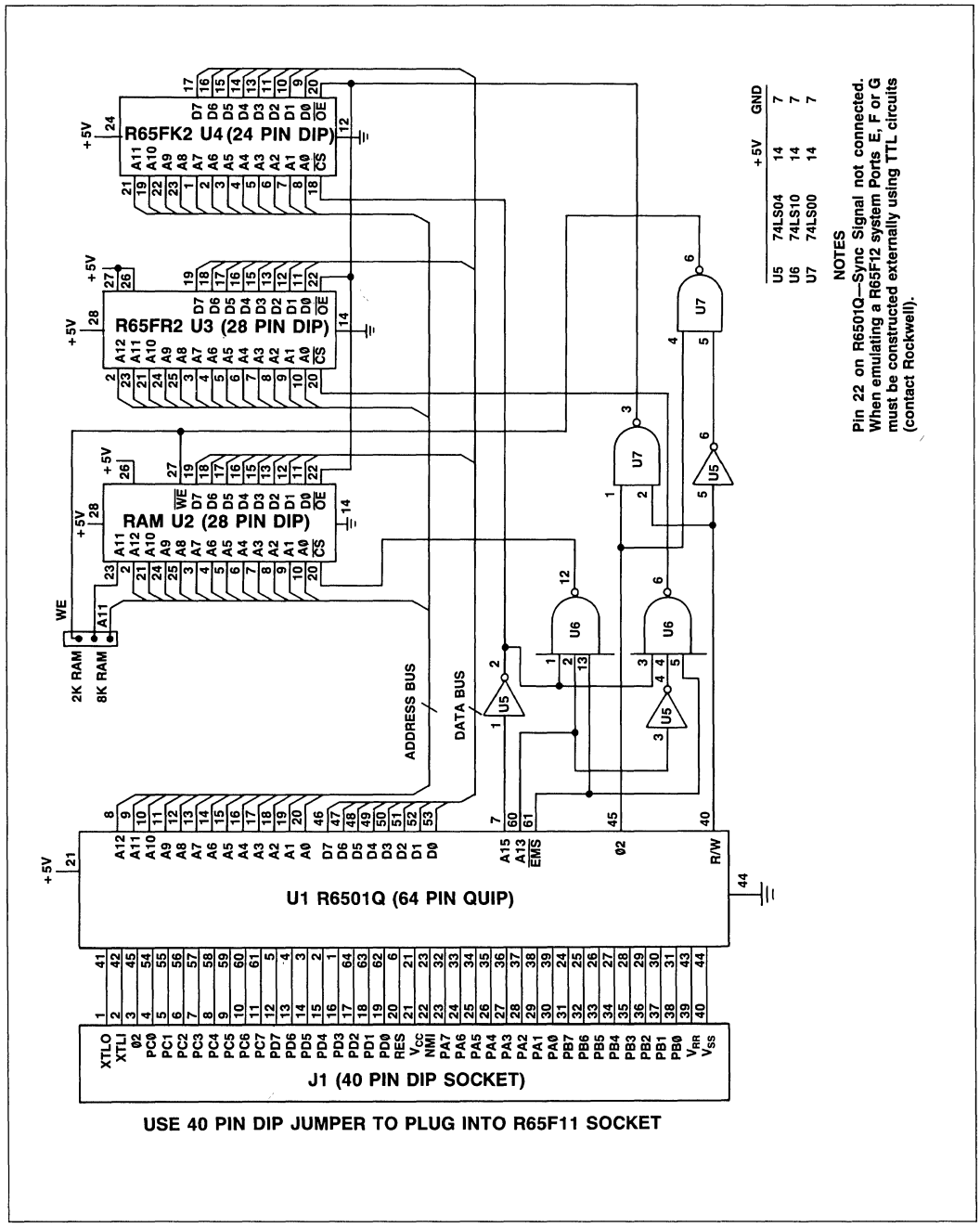


Figure 3. R6501Q, R65FR2 and R65K2 Application Configuration Schematic

RSC-FORTH CONFIGURATION 3 (R65FR3, R65FK3)

R6501Q BASED SYSTEM DEVELOPMENT AND PRODUCTION

The RSC-FORTH Configuration 3 is designed for those applications which require a larger amount of ROM or RAM space than the R65F11 or R65F12 can provide.

In the development configuration, the user is provided with up to 48K bytes of memory. The user memory is located from $0000 through $BFFF. The program heads will use some of this area but the user will still have considerably more memory space available then in the previous configurations.

The production configuration provides up to 56K bytes of user memory. This is due to the fact that the R65FR3 Development ROM, used in the development configuration, is not required in the production configuration and releases the 8K bytes of memory space. This memory is located at $C000 through $DFFF.

Figure 4 shows the development and production configurations for the R6501Q. Configuration 3 lists the features, memory maps, and the relationship of the R6501Q to the R65FR3 Development ROM and the R65FK3 Kernel ROM in the development and production environment.

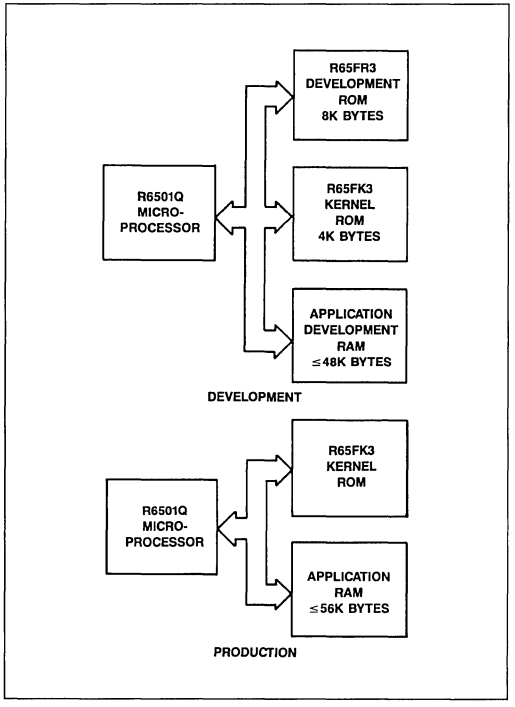


Figure 4. R65FR3 and R65FK3 Configuration 3 Block Diagrams

CONFIGURATION 3 CONSIDERATIONS

Features

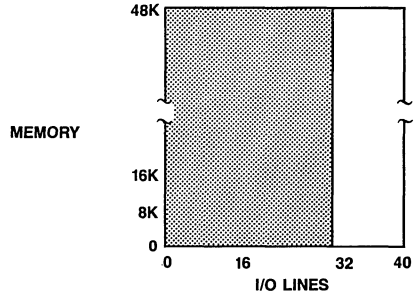
- R6501Q w/FORTH
- 48K Bytes of User Memory
- 30 I/O Lines

Device Configuration

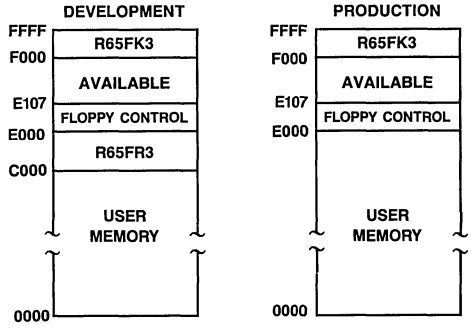
	DEVELOPMENT	PRODUCTION
R6501Q Microcomputer	✓	✓
R65FK3 Development ROM	✓	
R65FR3 Kernel ROM	✓	✓

User Memory—I/O Resource Matrix

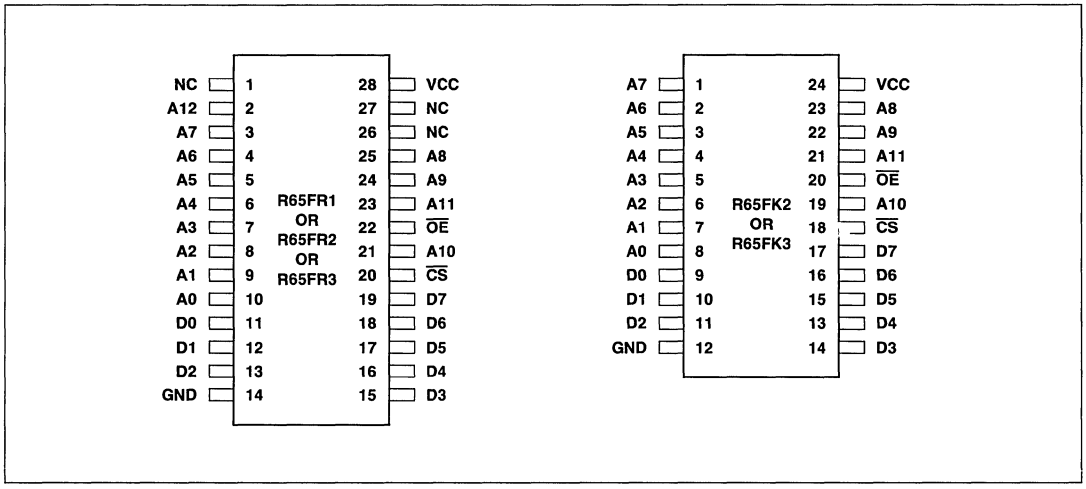
All ports act as I/O ports. Memory is on the bus. PC6 & PC7 (I/O lines) are assigned to memory. User memory can be a mix of ROM, EEROM, UVPROM or RAM.



Memory Maps



Note: Chip select for the Floppy Disk Controller should be at $E000-$E006 and at $E100-$E106 for this configuration.



RSC-FORTH ROM Pin Assignments

ABSOLUTE MAXIMUM RATINGS*

R65FR1, R65FR2, R65FR3, R65FK2, R65FK3

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.5 to +7.0	V
Input Voltage	V_{IN}	−0.5 to +7.0	V
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature	T_{ST}	−65 to +150	°C
Power Dissipation	P_D	1.0	W

***NOTE:** Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device atr these or any other conditions above those indicated in the other sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING CONDITIONS

Parameter	Range
V_{CC} Power Supply	5.0V ± 5%
Operating Temperature	0°C to 70°

3

D.C. CHARACTERISTICS

V_{CC} = 5.0V ± 5%, T_A = 0°C to +70°C (unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
V_{OH}	Output High Voltage R65FRx R65FKx	2.4	—	V_{CC}	V	V_{CC} = 4.75V I_{OH} = −400 μA I_{OH} = −240 μA
V_{OL}	Output Low Voltage R65FRx R65FKx	—	—	0.4	V	V_{CC} = 4.75V I_{OL} = 3.3 mA I_{OL} = 2.1 mA
V_{IH}	Input High Voltage	2.0	—	V_{CC}	V	
V_{IL}	Input Low Voltage	−0.5	—	0.8	V	
I_{LI}	Input Load Current	—	—	10	μA	V_{CC} = 5.25V, OV ≤ V_{IN} 5.25V
I_{LO}	Output Leakage Current	—	—	±10	μA	Chip Deselected, V_{CC} = 5.25V, V_{OUT} = +0.4V to V_{CC}
I_{CC}	Power Supply Current R65FRx R65FKx	 — —	 25 80	 55 135	 mA mA	V_{CC} = 5.25V @ 0°C
C_I	Input Capacitance	—	—	7	pF	V_{CC} = 5.0V, Chip Deselected, pin under test at 0V
C_O	Output Capacitance	—	—	10	pF	V_{CC} = 5.0V, Chip Deselected, pin under test at 0V

Section 4
16-Bit Microprocessors and Peripherals

4

16-Bit Microprocessor and Peripherals Meeting System Communications Needs

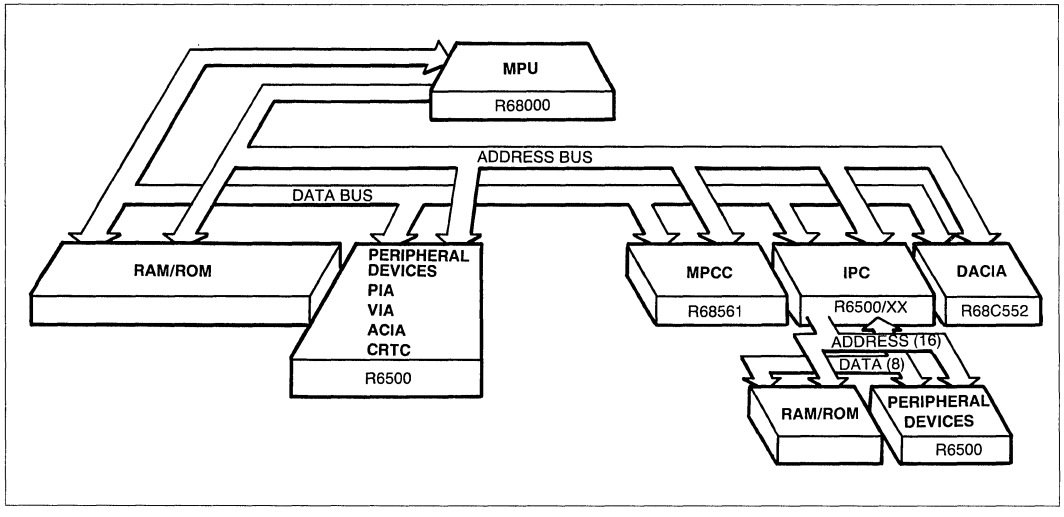
Rockwell peripherals give a designer the communication control elements for the 68000 processor. They allow you to design functional systems utilizing all the speed and data handling potential of the 16-bit 68000 family.

These peripherals consist of the Rockwell designed Multi-Protocol Communications Controller and the Dual Asynchronous Interface Adapter — each a significant "first" that eliminates "glue parts" between a CPU and peripherals.

The R68561 Multi-Protocol Communications Controller (MPCC) is one of the highest throughput communications devices ever commercially made. It operates up to 4 Mbits/sec and supports all major communication protocols. It is available to work with either a 16-bit or 8-bit bus and can be adapted to function with essentially any of today's more common busses.

The R68C552 Dual Asynchronous Interface Adapter (DACIA) provides an easily implemented, programmed controlled interface between 16-bit microprocessor-based systems and serial communication data sets and modems. This device is the first CMOS ACIA in the industry.

Rockwell lets you build efficient and economical 16-bit systems through families of 16-bit and 8-bit peripherals, all compatible. No other company offers you more.

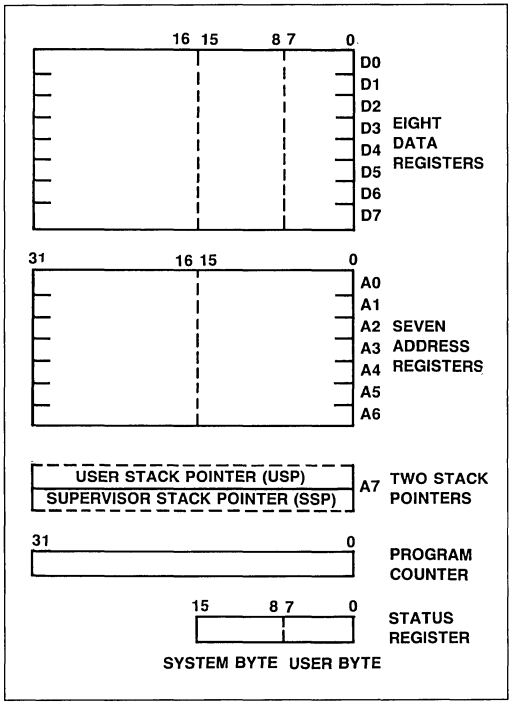


R68000/R6500 Peripheral Migration

R68000
16-Bit Microprocessing Unit (MPU)

DESCRIPTION

The R68000 microprocessor is designed for high performance where operational computation and versatility is required. The R68000 provides powerful mass-memory handling capability and architectural features designed to fit the broad range of 16-bit needs. The Rockwell family of 16-bit products also includes a wide range of peripherals that will allow complete system design and manufacture.



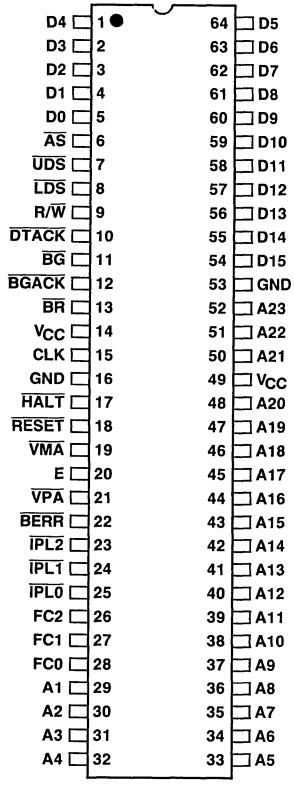
R68000 Registers

The R68000 offers seventeen 32-bit registers in addition to the 32-bit program counter and a 16-bit status register. The first eight registers (D0-D7) are used as data registers for byte (8-bit), word (16-bit), and long word (32-bit) data operations. The second set of seven registers (A0-A6) and the system stack pointer may be used as software stack pointers and base address registers. In addition, these registers may be used for word and long word address operations. All 17 registers may be used as index registers.

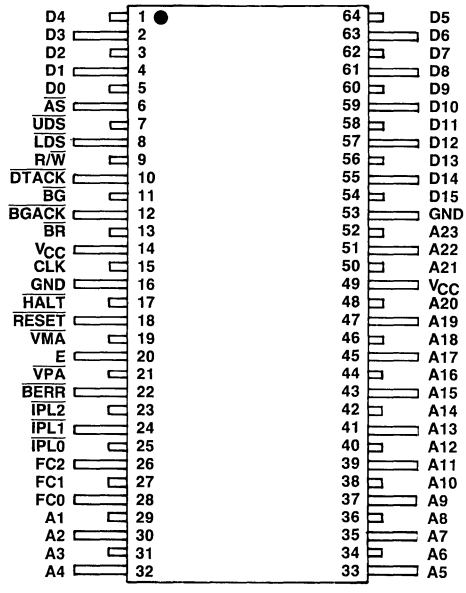
FEATURES

- 16M byte (8M word) Linear Addressing Range
- 14 Operand Addressing Modes
- 56 Powerful Instruction Types
- Instruction Set Supports Structured High-Level Languages
- Pipelining Instruction Execution
- 32-Bit Program Counter
- 16-Bit Data Bus
- 23-Line Address Bus
- 32-Bit Data and Address Registers Including:
  - — Eight General Purpose Data Registers
  - — Seven Address Registers
  - — Two Stack Pointers (User, Supervisory)
- All 17 Registers Can Be Index Registers
- Memory Mapped Peripheral Devices
- Vector Generated Exception Processing
- Seven Unique Autovectors for Interrupt Service Routines
- Trace Mode for Software Debugging
- Operations Occur on Five Main Data Types
  - — Bit
  - — BCD
  - — Byte
  - — Word
  - — Long Word
- Asynchronous and Synchronous Peripheral Interface Capability
- Many Peripheral Chips Available
  - R68560/R68561 Multi-Protocol Communications Controller (MPCC)
  - — R68802 Local Network Controller (LNET)
  - — R68C552 Dual Asynchronous Communications Interface Adapter (DACIA)
- Up to 12.5 MHz Input Clock
- +5 VDC Power Supply

4



R68000C/P Pin Assignments—64-Pin DIP*



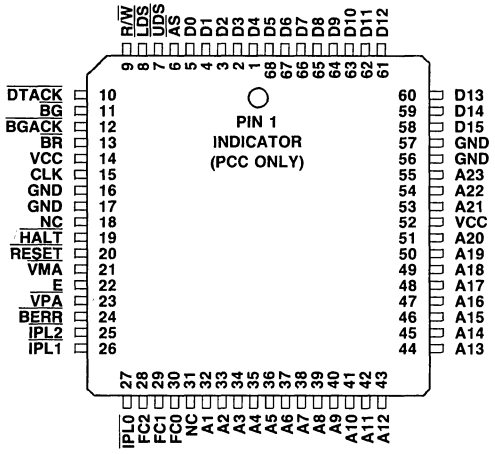
R68000Q Pin Assignments—64-Pin QUIP*

ORDERING INFORMATION

Part Number:

R68000

- Temperature Range (T_L to T_H) and Screening/Burn-in
  - Blank = 0°C to 70°C
  - M = −55°C to 125°C
  - R = −55°C to 125°C and burned-in 168 hours
  - B = −55°C to 125°C and screened to MIL-STD 883B
- Frequency
  - 6 = 6 MHz
  - 8 = 8 MHz
  - 10 = 10 MHz
  - 12 = 12.5 MHz
- Package
  - C = 64-Pin Ceramic DIP
  - P = 64-Pin Plastic DIP
  - Q = 64-Pin Plastic QUIP
  - J = 64-Pin Plastic Leaded Chip Carrier (PCC)
  - L = 64-Pin Leadless Ceramic Chip Carrier (LCCC)



R68000J/L Pin Assignments—68-Pin PCC and LCC*

*Pin Assignment package outlines are not actual size (refer to PACKAGE DIMENSIONS on pages 56–59).

SIGNAL DESCRIPTION

The following paragraphs briefly describe the input and output signals and also reference (if applicable) other paragraphs that contain more detail about the function being performed. Bus operation during the various machine cycles and operations is also discussed. The input and output signals can be functionally organized into the groups shown in Figure 1.

Note

The terms assertion and negation are used to avoid confusion when dealing with a mixture of "active-low" and "active-high" signals. The terms assert, or assertion, indicates that a signal is active, or true, independent of whether that voltage is low or high. The term negate, or negation, indicates that a signal is inactive or false.

ADDRESS BUS (A1 THROUGH A23). This 23-bit, unidirectional, three-state bus can address eight megawords of data. It provides the address for bus operation during all cycles except interrupt cycles. During interrupt cycles, address lines A1, A2, and A3 encode the interrupt level to be serviced while address lines A4 through A23 are all set high.

DATA BUS (D0 THROUGH D15). This 16-bit, bidirectional, three-state bus is the general purpose data path. It transfers and accepts data in either word or byte length. During an interrupt acknowledge cycle, an external device supplies the vector number on data lines D0-D7.

ASYNCHRONOUS BUS CONTROL. Asynchronous data transfers are handled using the following control signals: address strobe, read/write, upper and lower data strobes, and data transfer acknowlege. These signals are explained in the following paragraphs.

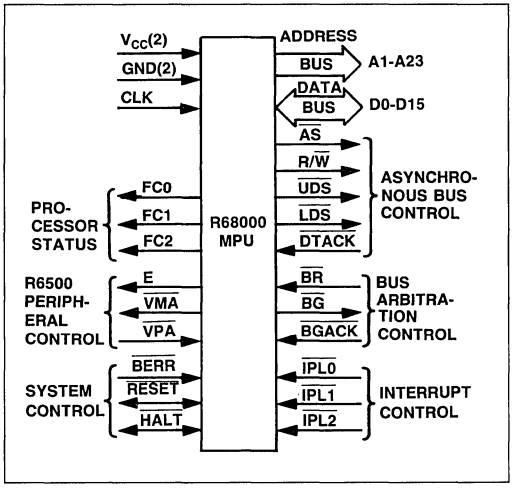


Figure 1. Input and Output Signals

Address Strobe (AS). The AS output indicates that there is a valid address on the address bus.

Read/Write (R/W). The R/W output defines the data bus transfer as a read or write cycle. The R/W signal also works in conjunction with the upper and lower data strobes as explained in the following paragraph.

Upper and Lower Data Strobes (UDS, LDS). The UDS and LDS outputs control the data on the data bus, as shown in Table 1. When the R/W line is high, the processor reads from the data bus as indicated. When the R/W line is low, the processor writes to the data bus as shown.

Data Transfer Acknowledge (DTACK). The DTACK input indicates that the data transfer is completed. When the processor recognizes DTACK during a read cycle, data is latched and the bus cycle terminated. When DTACK is recognized during a write cycle, the bus cycle terminates. Refer to **ASYNCHRONOUS VERSUS SYNCHRONOUS OPERATION.**

BUS ARBITRATION CONTROL. These three signals form a bus arbitration circuit to determine which device will be the bus master device.

Bus Request (BR). The BR input indicates to the processor that some other device desires to become the bus master. This input can be externally ORed with all other devices that could be bus masters.

Bus Grant (BG). The BG output indicates to all other potential bus master devices that the processor will release bus control at the end of the current bus cycle.

Bus Grant Acknowledge (BGACK). The BGACK input indicates that some other device has become the bus master. This signal cannot be asserted until the following four conditions are met:

1. a bus grant (BG) has been received,
2. address strobe (AS) is inactive which indicates that the processor is not using the bus

Table 1. Data Strobe Control of Data Bus

UDS	LDS	R/W	D8-D15	D0-D7
High	High	—	No valid data	No valid data
Low	Low	High	Valid data bits 8-15	Valid data bits 0-7
High	Low	High	No valid data	Valid data bits 0-7
Low	High	High	Valid data bits 8-15	No valid data
Low	Low	Low	Valid data bits 8-15	Valid data bits 0-7
High	Low	Low	Valid data bits 0-7*	Valid data bits 0-7
Low	High	Low	Valid data bits 8-15	Valid data bits 8-15*

*These conditions are a result of current implementation and may not appear on future devices.

3. data transfer acknowledge ($\overline{DTACK}$) is inactive which indicates that neither memory nor peripherals are using the bus, and
4. bus grant acknowledge ($\overline{BGACK}$) is inactive which indicates that no other device is still claiming bus mastership.

INTERRUPT CONTROL ($\overline{IPL0}$, $\overline{IPL1}$, $\overline{IPL2}$). These input pins indicate the encoded priority level of the device requesting an interrupt. Level seven is the highest priority while level zero indicates that no interrupts are requested. Level seven cannot be masked. $\overline{IPL0}$ is the least significant bit while $\overline{IPL2}$ is the most significant bit. To insure an interrupt is recognized, the interrupt control lines ($\overline{IPLX}$) must remain stable until the processor signals interrupt acknowledge (FC0, FC1, and FC2 all high).

SYSTEM CONTROL. The system control inputs either reset or halt the processor or indicate to the processor that bus errors have occurred. The three system control inputs are explained in the following paragraphs.

Bus Error ($\overline{BERR}$). The $\overline{BERR}$ input informs the processor that a problem exists with the cycle currently being executed. Problems may be a result of:
1. nonresponding devices,
2. interrupt vector number acquisition failure,
3. illegal access request as determined by a memory management unit, or
4. other application dependent errors.

The Bus Error ($\overline{BERR}$) signal interacts with the $\overline{HALT}$ signal to determine if exception processing should be performed or the current bus cycle should be retried.

Refer to BUS ERROR AND HALT OPERATION paragraph for additional information about the interaction of the bus error and halt signals.

Reset ($\overline{RESET}$). This bidirectional signal line acts to reset (initiate a system initialization sequence) the processor and system in response to an external reset signal. An internally generated reset (result of a RESET instruction) resets all external devices while not affecting the internal state of the processor. A total system reset (processor and external devices) is the result of external $\overline{HALT}$ and $\overline{RESET}$ signals applied simultaneously. Refer to RESET OPERATION paragraph for additional information.

Halt ($\overline{HALT}$). The bidirectional $\overline{HALT}$ line, when driven by an external device, will cause the processor to stop at the completion of the current bus cycle. Halting the processor using $\overline{HALT}$ causes all control signals to go inactive and all three-state lines to go to their high-impedance state. Refer to BUS ERROR AND HALT OPERATION paragraph for additional information about the interaction between the $\overline{HALT}$ and $\overline{BERR}$ signals.

When the processor has stopped executing instructions, such as in a double bus fault condition, the $\overline{HALT}$ line is driven by the processor to indicate to external devices that the processor has stopped. Refer to paragaph on Double Bus Faults.

R6500 PERIPHERAL CONTROL. These control signals are used to allow the interfacing of synchronous R6500 peripheral devices with the asynchronous R68000. These signals are explained in the following paragraphs.

Enable (E). The E output signal is the standard enable signal ($\emptyset 2$ clock) common to all R6500 type peripheral devices. The period for this output is ten R68000 clock periods (six clocks low; four clocks high). Enable is generated by an internal ring counter which may come up in any state (i.e., at power on, it is impossible to guarantee phase relationship of E to CLK). E is a free-running clock and runs regardless of the state of the bus on the MPU.

Valid Peripheral Address ($\overline{VPA}$). The $\overline{VPA}$ input indicates that the device or region addressed is a R6500 family device and that data transfer should be synchronized with the enable (E) signal. This input also indicates that the processor should use automatic vectoring for an interrupt. Refer to INTERFACE WITH R6500 PERIPHERALS.

Valid Memory Address ($\overline{VMA}$). The $\overline{VMA}$ output indicates to R6500 peripheral devices that there is a valid address on the address bus and that the processor is synchronized to enable. This signal only responds to a valid peripheral address ($\overline{VPA}$) input which indicates that the peripheral is a R6500 family device.

PROCESSOR STATUS (FC0, FC1, FC2). These function code outputs indicate the state (user or supervisor) and the cycle type currently being executed, as shown in Table 2. The information indicated by the function code outputs is valid whenever address strobe ($\overline{AS}$) is active.

CLOCK (CLK). The clock input is a TTL-compatible signal that is internally buffered for development of the internal clocks needed by the processor. The clock input should not be gated off at any time and the clock signal must conform to minimum and maximum pulse width times.

SIGNAL SUMMARY. Table 3 summarizes all the signals discussed in the previous paragraphs.

Table 2. Function Code Outputs

FC2	FC1	FC0	Cycle Type
Low	Low	Low	(Undefined, Reserved)
Low	Low	High	User Data
Low	High	Low	User Program
Low	High	High	(Undefined, Reserved)
High	Low	Low	(Undefined, Reserved)
High	Low	High	Supervisor Data
High	High	Low	Supervisor Program
High	High	High	Interrupt Acknowledge

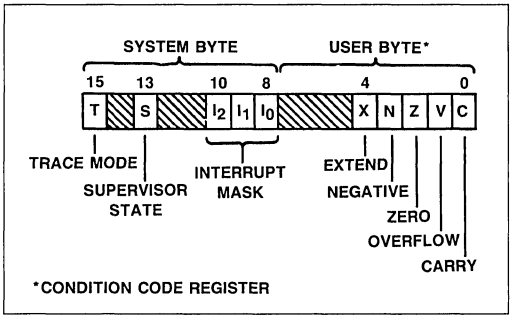
Table 3. Signal Summary

Signal Name	Mnemonic	Input/Output	Active State	Hi-Z	
				On $\overline{HALT}$	On $\overline{BGACK}$
Address Bus	A1-A23	Output	High	Yes	Yes
Data Bus	D0-D15	Input/Output	High	Yes	Yes
Address Strobe	$\overline{AS}$	Output	Low	No	Yes
Read/Write	R/$\overline{W}$	Output	Read-High Write-Low	No	Yes
Upper and Lower Data Strobes	$\overline{UDS}$, $\overline{LDS}$	Output	Low	No	Yes
Data Transfer Acknowledge	$\overline{DTACK}$	Input	Low	No	No
Bus Request	$\overline{BR}$	Input	Low	No	No
Bus Grant	$\overline{BG}$	Output	Low	No	No
Bus Grant Acknowledge	$\overline{BGACK}$	Input	Low	No	No
Interrupt Priority Level	$\overline{IPL0}$, $\overline{IPL1}$, $\overline{IPL2}$	Input	Low	No	No
Bus Error	$\overline{BERR}$	Input	Low	No	No
Reset	$\overline{RESET}$	Input/Output	Low	No*	No*
Halt	$\overline{HALT}$	Input/Output	Low	No*	No*
Enable	E	Output	High	No	No
Valid Memory Address	$\overline{VMA}$	Output	Low	No	Yes
Valid Peripheral Address	$\overline{VPA}$	Input	Low	No	No
Function Code Output	FC0, FC1, FC2	Output	High	No	Yes
Clock	CLK	Input	High	No	No
Power Input	V_{CC}	Input	—	—	—
Ground	GND	Input	—	—	—

*Open drain.

REGISTER DESCRIPTION AND DATA ORGANIZATION

STATUS REGISTER. The status register contains the eight level interrupt mask as well as the condition codes; extend (X), negative (N), zero (Z), overflow (V), and carry (C). Additional status bits indicate that the processor is in a trace (T) mode and/or in a supervisor (S) state.



Status Register

OPERAND SIZE

Operand sizes are defined as follows: a byte equals 8 bits, a word equals 16 bits, and a long word equals 32 bits. The operand size for each instruction is either explicitly encoded in the instruction or implicitly defined by the instruction operation. Implicit instructions support some subset of all three sizes.

DATA ORGANIZATION IN REGISTERS

The eight data registers support data operands of 1, 8, 16, or 32 bits. The seven address registers together with the active stack pointer support address operands of 32 bits.

DATA REGISTERS. Each data register is 32 bits wide. Byte operands occupy the low order 8 bits, word operands the low order 16 bits, and long word operands the entire 32 bits. The least significant bit is addressed as bit zero; the most significant bit is addressed as bit 31. When a data register is used as either a source or destination operand, only the appropriate low-order portion is changed; the remaining high order portion is neither used nor changed.

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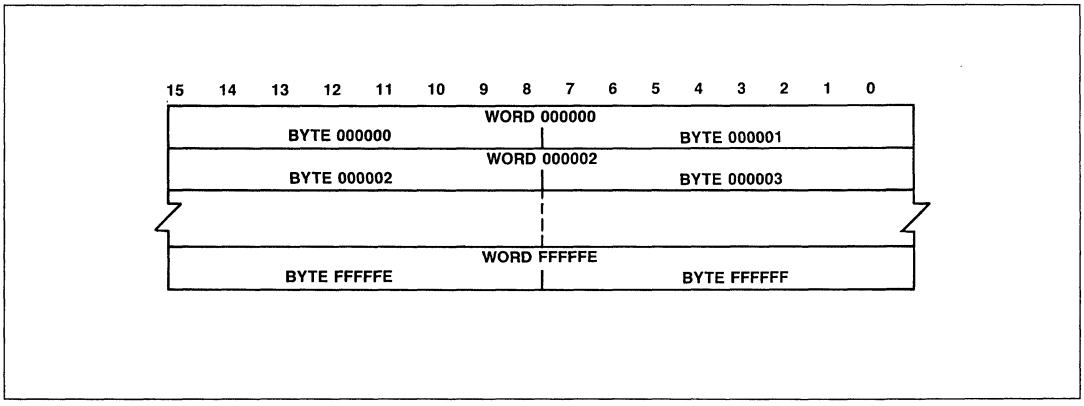


Figure 2. Word Organization In Memory

ADDRESS REGISTERS. Each address register and the stack pointer is 32 bits wide and holds a full 32-bit address. Address registers do not support byte sized operands. Therefore, when an address register is used as a source operand, either the low order word or the entire long word operand is used depending upon the operation size. When an address register is used as the destination operand, the entire register is affected regardless of the operation size. If the operation size is word, any other operands are sign extended to 32 bits before the operation is performed.

DATA ORGANIZATION IN MEMORY

Bytes are individually addressable with the high order byte having an even address the same as the word, as shown in Figure 2. The low order byte has an odd address that is one higher than the word address. Instructions and multi-byte data are accessed only on word (even byte) boundaries. If a long word datum is located at address n (n even), then the second word of that datum is located at address n + 2.

The data types supported by the R68000 are: bit data, integer data of 8, 16, or 32 bits, 32-bit addresses and binary coded decimal data. Each of these data types is put in memory, as shown in Figure 3. The numbers indicate the order in which data is accessed from the processor.

BUS OPERATION

The following paragraphs explain control signal and bus operation during data transfer operations, bus arbitration, bus error and halt conditions, and reset operation.

DATA TRANSFER OPERATIONS. Transfer of data between devices involves the following signals:

- Address Bus A1 through A23
- Data Bus D0 through D15
- Control Signals

The address and data buses are separate parallel buses which transfer data using an asynchronous bus structure. In all cycles, the bus master assumes responsibility for deskewing all signals it issues at both the start and end of a cycle. In addition, the bus master is responsible for deskewing the acknowledge and data signals from the slave device.

The following paragraphs explain the read, write, and read-modify-write cycles. The indivisible read-modify-write cycle is the method used by the R68000 for interlocked multiprocessor communications.

Read Cycle. During a read cycle, the processor receives data from memory or a peripheral device. The processor reads bytes of data in all cases, and for a word (or double word) operation, the processor reads both upper and lower bytes simultaneously by asserting both upper and lower data strobes. When the instruction specifies byte operation, the processor uses an internal AO bit to determine which byte to read and then issues the data strobe required for that byte. When the AO bit equals zero, the upper data strobe is issued, and when the AO bit equals one, the lower data strobe is issued. The processor correctly positions the received data internally.

A word read cycle flow chart is given in Figure 4. A byte read cycle flow chart is given in Figure 5. Read cycle timing is given in Figure 6. Figure 7 details word and byte read cycle operations.

Write Cycle. During a write cycle, the processor sends bytes of data to memory or a peripheral device. If the instruction specifies a word operation, the processor writes both bytes. When the instruction specifies a byte operation, the processor uses an internal AO bit to determine which byte to write and then issues the data strobe required for that byte. When the AO bit equals zero, the upper data strobe is issued and when the AO bit equals one, the lower data strobe is issued. A word write cycle flow chart is given in Figure 8. A byte write cycle flow chart is given in Figure 9. Write cycle timing is given in Figure 6. Figure 10 details word and byte write cycle operation.

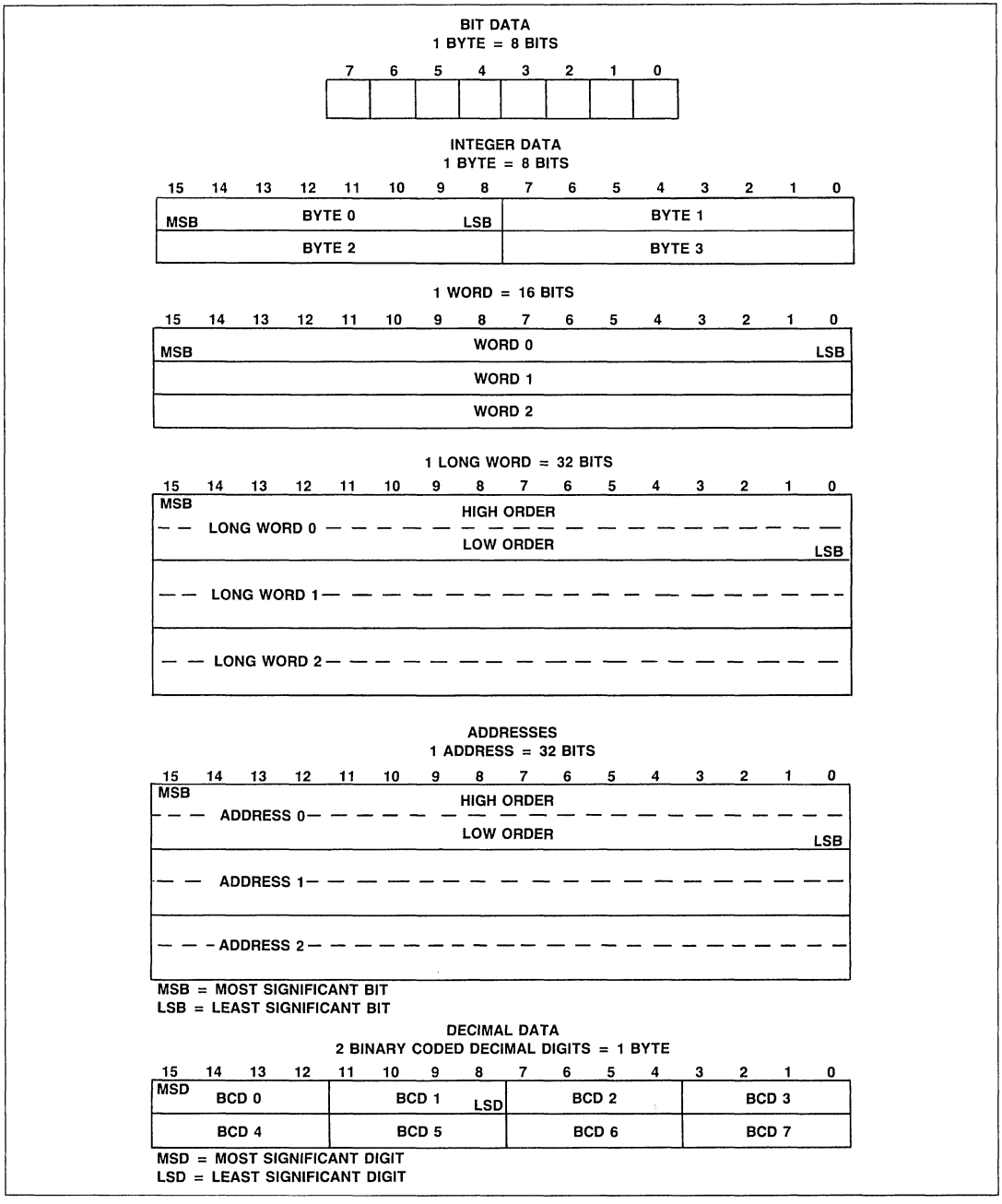


Figure 3. Data Organization In Memory

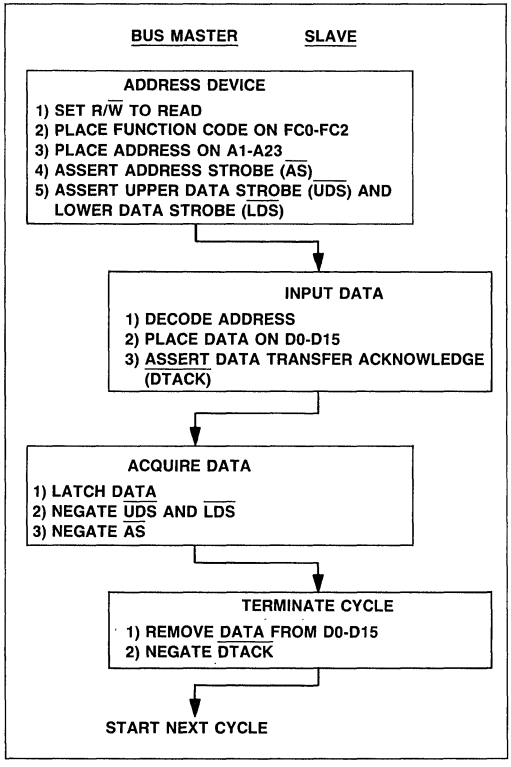


Figure 4. Word Read Cycle Flow Chart

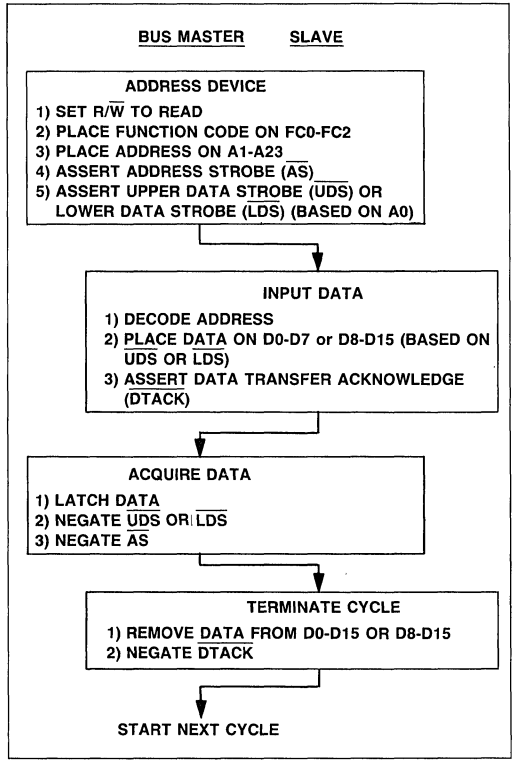


Figure 5. Byte Read Cycle Flow Chart

Read-Modify-Write Cycle. The read-modify-write cycle performs a read, modifies the data in the arithmetic-logic unit, and writes the data back to the same address. In the R68000 this cycle is indivisible in that the address strobe is asserted throughout the entire cycle. The test and set (TAS) instruction uses this cycle to provide meaningful communication between processors in a multiple processor environment. TAS is the only instruction that uses the read-modify-write cycles. Since the test and set instruction only operates on bytes, all read-modify-write cycles are byte operations. A read-modify-write cycle flow chart is given in Figure 11 and a timing diagram is given in Figure 12.

BUS ARBITRATION. Bus arbitration is a technique used by master-type devices to request, be granted, and acknowledge bus mastership. In its simplest form, it consists of:

1. asserting a bus mastership request,
2. receiving a grant that the bus is available at the end of the current cycle, and
3. acknowledging that mastership has been assumed.

Figure 13 is a flow chart showing the detail involved in a request from a single device. Figure 14 is a timing diagram for the same operation. This technique allows processing of bus requests during data transfer cycles.

The timing diagram shows that the bus request is negated at the time that an acknowledge is asserted. This is true for a system consisting of the processor and one device capable of bus mastership. However, in systems having a number of devices capable of bus mastership, the bus request line from each device is ORed to the processor. In this system, it is easy to see that there could be more than one bus request being made. The timing diagram shows that the bus grant signals negate a few clock cycles after the transition of the acknowledge (BGACK) signal.

However, if the bus requests are still pending, the processor will assert another bus grant within a few clock cycles after negation. This additional assertion of bus grant allows external arbitration circuitry to select the next bus master before the current bus master has completed its requirements. The following paragraphs provide additional information about the three steps in the arbitration process.

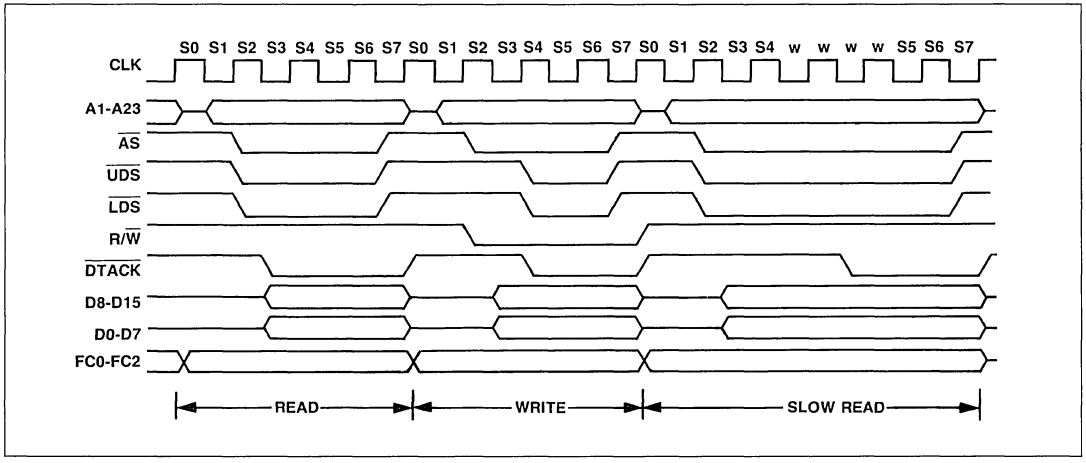


Figure 6. Read and Write Cycle Timing Diagram

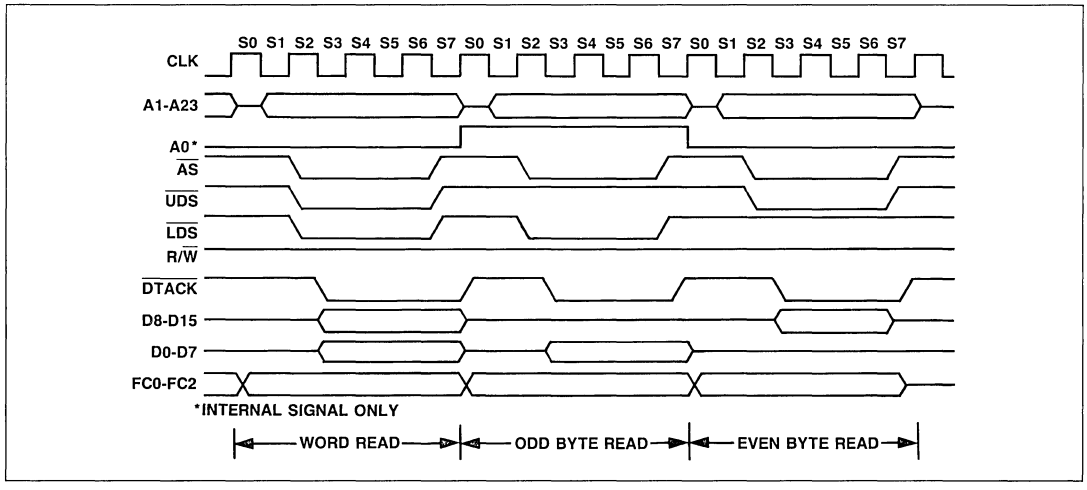


Figure 7. Word and Byte Read Cycle Timing Diagram

Requesting the Bus. External devices capable of becoming bus masters request the bus by asserting the bus request ($\overline{BR}$) signal. This ORed signal (although it need not be constructed from open collector devices) indicates to the processor that some external device requires control of the external bus. The processor, at a lower bus priority level than the external device, will relinquish the bus after it has completed the last bus cycle it has started. If no acknowledge is received before the bus request signal goes inactive, the processor will continue processing when it detects that the bus request is inactive. This allows ordinary processing to continue if the arbitration circuitry inadvertently responded to noise.

Receiving the Bus Grant. Normally the processor asserts bus grant ($\overline{BG}$) as soon as possible after internal synchronization. The only exception occurs when the processor has made an internal decision to execute the next bus cycle but has not progressed far enough into the cycle to have asserted the address strobe ($\overline{AS}$) signal. In this case, bus grant will not be asserted until one clock after address strobe is asserted to indicate to external devices that a bus cycle is being executed.

The bus grant signal may be routed through a daisy-chained network or through a specific priority-encoded network. The processor is not affected by the external method of arbitration as long as the protocol is obeyed.

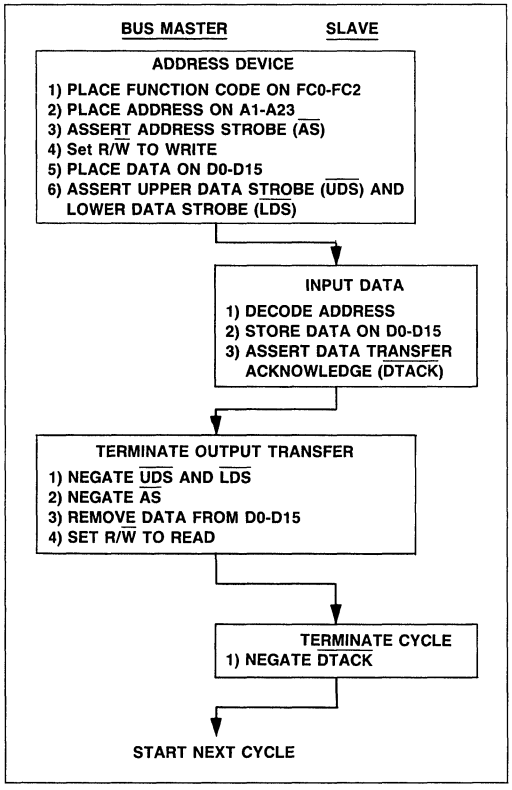


Figure 8. Word Write Cycle Flow Chart

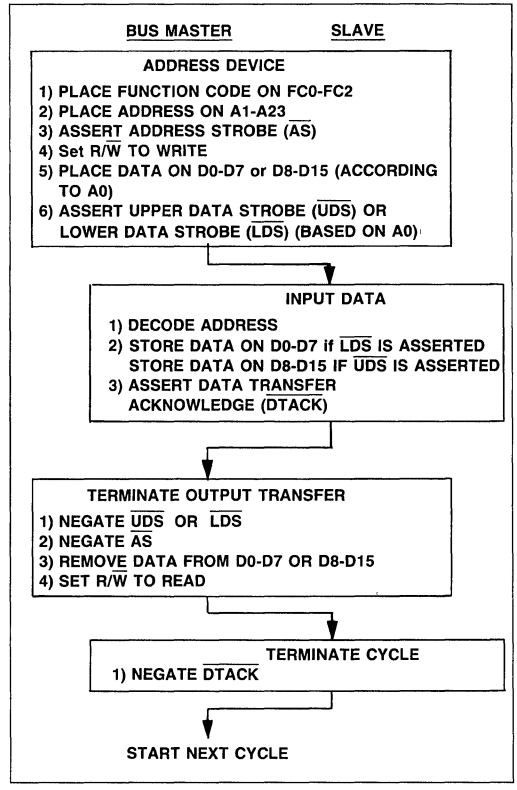


Figure 9. Byte Write Cycle Flow Chart

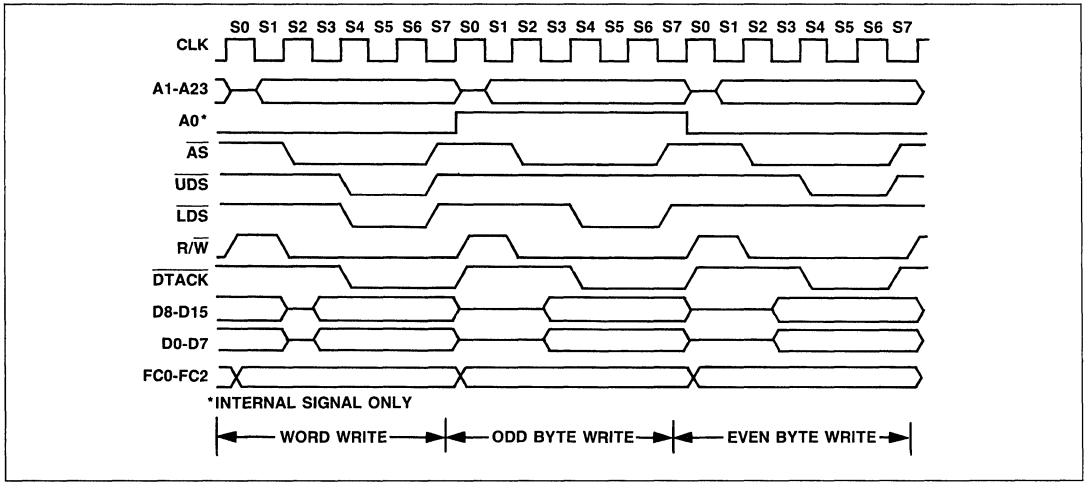


Figure 10. Word and Byte Write Cycle Timing Diagram

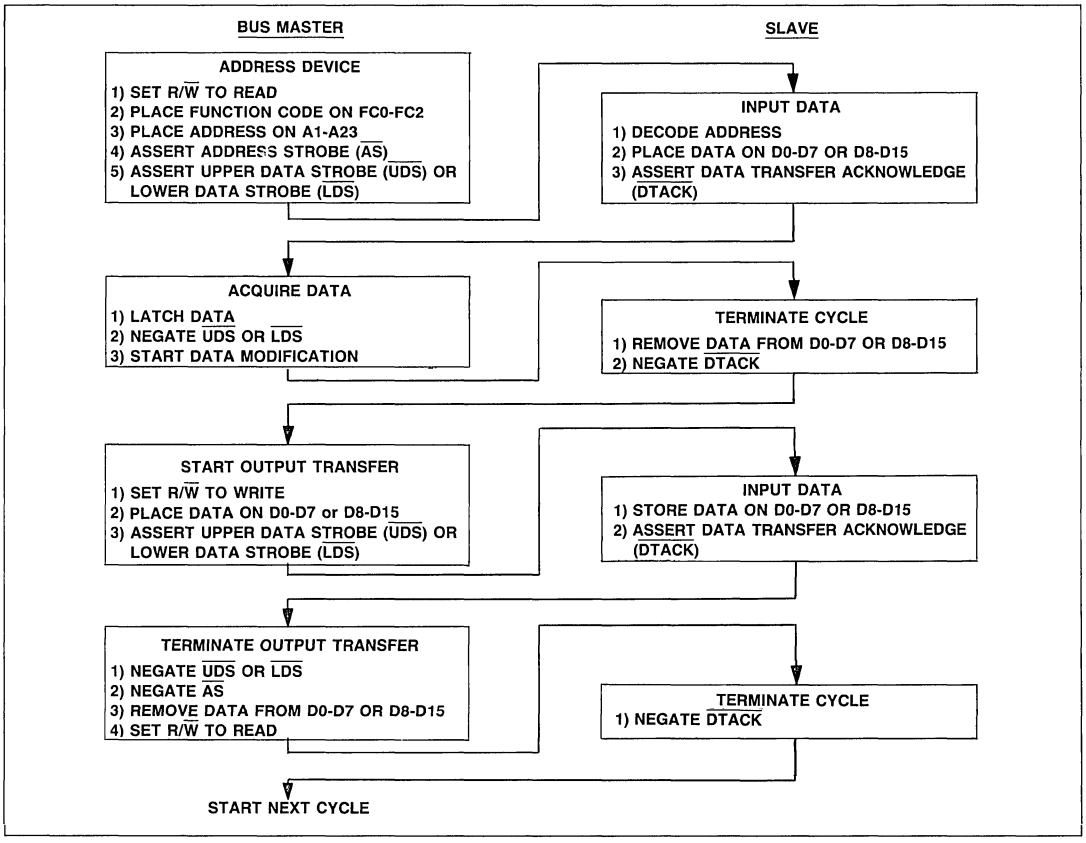


Figure 11. Read-Modify-Write Cycle Flow Chart

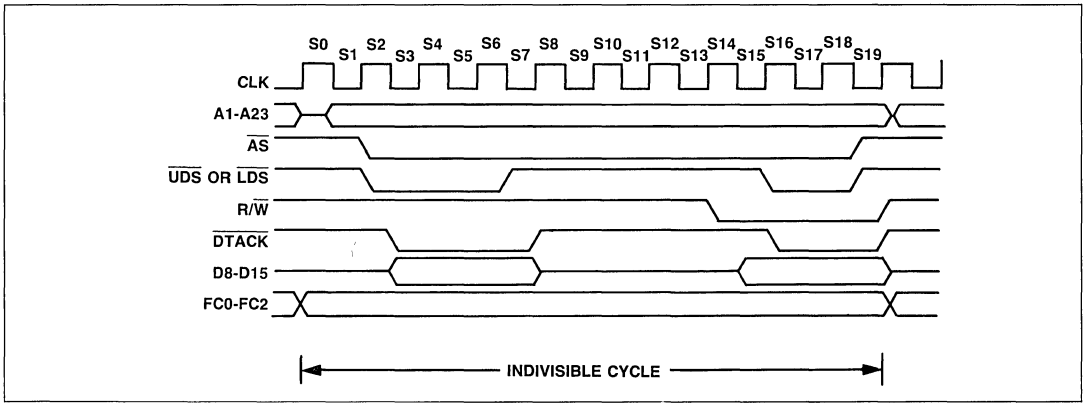


Figure 12. Read-Modify-Write Cycle Timing Diagram

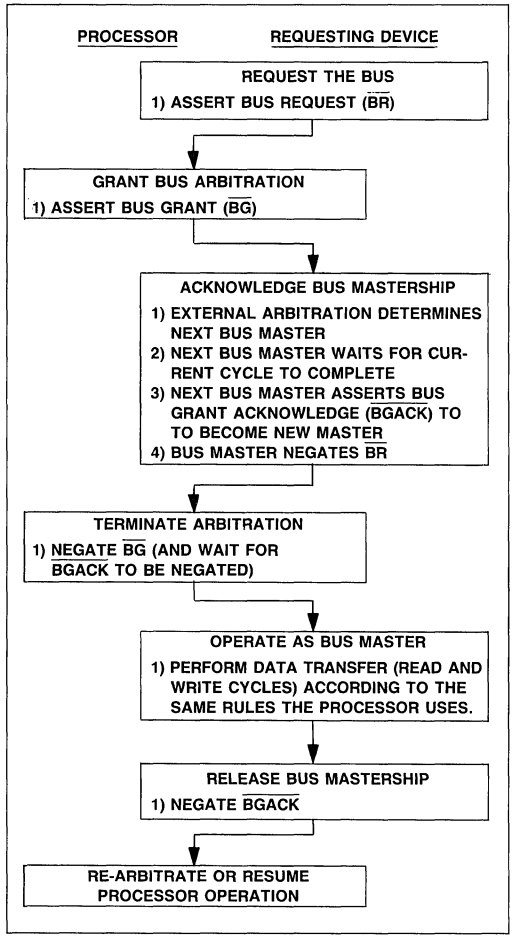


Figure 13. Bus Arbitration Cycle Flow Chart

Acknowledgment of Mastership. Upon receiving a bus grant ($\overline{BG}$), the requesting device waits until address strobe ($\overline{AS}$), data transfer acknowledge ($\overline{DTACK}$), and bus grant acknowledge ($\overline{BGACK}$) are negated before issuing its own $\overline{BGACK}$. The negation of the address strobe indicates that the previous master has completed its cycle, while the negation of bus grant acknowledge indicates that the previous master has released the bus. (If address strobe is asserted no device is allowed to "break into" a cycle.) The negation of data transfer acknowledge indicates the previous slave has terminated its connection to the previous master. In some applications data transfer acknowledge may not be required. In this case the devices would use the address strobe. When bus grant acknowledge is issued the device is bus master. Only after the bus cycle(s) is (are) completed should bus grant acknowledge be negated to terminate bus mastership.

The bus request from the granted device should be dropped after bus grant acknowledge is asserted. If a bus request is still pending, another bus grant will be asserted within a few clocks of the negation of bus grant. Refer to Bus Arbitration Control section. The processor does not perform any external bus cycles before it reasserts bus grant.

BUS ARBITRATION CONTROL. The bus arbitration control unit in the R68000 is implemented with a finite state machine. A state diagram of this machine is shown in Figure 15. All asynchronous signals to the R68000 are synchronized before being used internally. This synchronization is accomplished in a maximum of one cycle of the system clock, assuming that the asynchronous input setup time (#47) has been met (see Figure 16). The input signal is sampled on the falling edge of the clock and is valid internally after the next falling edge. If $\overline{BR}$ and $\overline{BGACK}$ meet the asynchronous set-up time tASI (#47), then tBGKBR (#37A) can be ignored. If $\overline{BR}$ and $\overline{BGACK}$ are asserted asynchronously with respect to the clock, $\overline{BGACK}$ has to be asserted before $\overline{BR}$ is negated.

As shown in Figure 15, input signals labeled R and A are internally synchronized on the bus request and bus grant acknowledge pins respectively. The bus grant output is labeled G and the internal three-state control signal T. If T is true, the address, data, and control buses are placed in a high-impedance state when $\overline{AS}$ is negated. All signals are shown in positive logic (active high) regardless of their true active voltage level.

State changes (valid outputs) occur on the next rising clock edge after the internal signal is valid.

A timing diagram of the bus arbitration sequence during a processor bus cycle is shown in Figure 17. The bus arbitration sequence while the bus is inactive (i.e., executing internal operations such as a multiply instruction) is shown in Figure 18.

If a bus request ($\overline{BR}$) is made at a time when the MPU has already begun a bus cycle but $\overline{AS}$ has not been asserted (bus state S0), $\overline{BG}$ will not be asserted on the next rising edge. Instead $\overline{BG}$ will be delayed until the second rising edge following its internal assertion. This sequence is shown in Figure 19.

BUS ERROR AND HALT OPERATION. In a bus architecture that requires a handshake from an external device, the possibility exists that the handshake might not occur. Since different systems will require a different maximum response time, a bus error input is provided.

External circuitry must be used to determine the duration between address strobe and data transfer acknowledge before issuing a bus error signal. When a bus error signal is received, the processor has two options: initiate a bus error exception sequence or try running the bus cycle again.

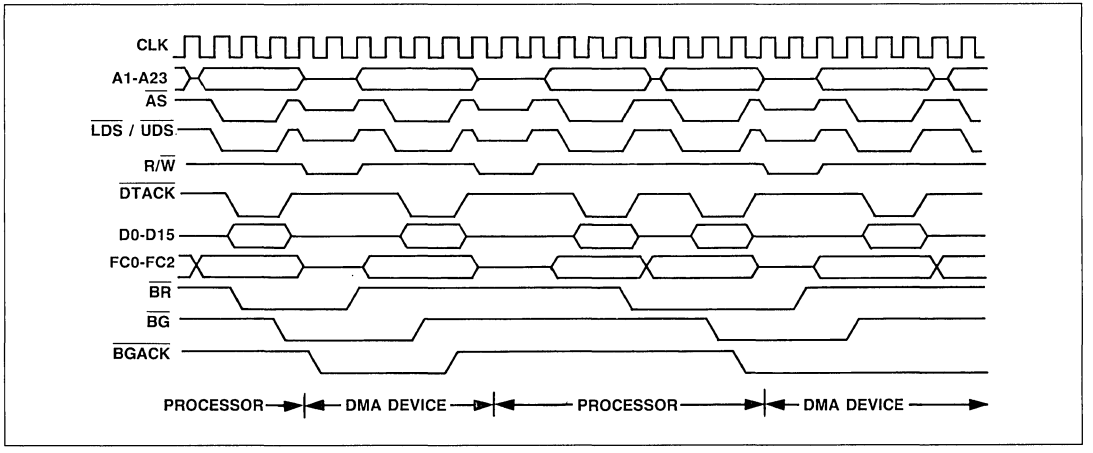
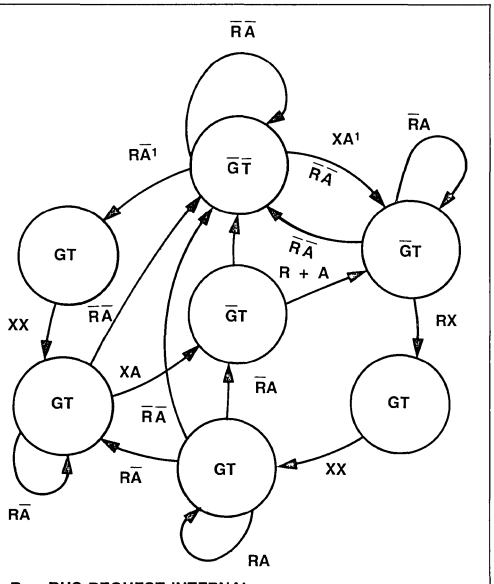


Figure 14. Bus Arbitration Cycle Timing Diagram



R = BUS REQUEST INTERNAL
A = BUS GRANT ACKNOWLEDGE INTERNAL
G = BUS GRANT
T = THREE-STATE CONTROL TO BUS CONTROL LOGIC[2]
X = DON'T CARE

1. STATE MACHINE WILL NOT CHANGE STATE IF BUS IS IN S0 OR S1. REFER TO BUS ARBITRATION CONTROL FOR ADDITIONAL INFORMATION.
2. THE ADDRESS BUS WILL BE PLACED IN THE HIGH IMPEDANCE STATE IF T IS ASSERTED AND AS NEGATED.

Figure 15. State Diagram of R68000 Bus Arbitration Unit

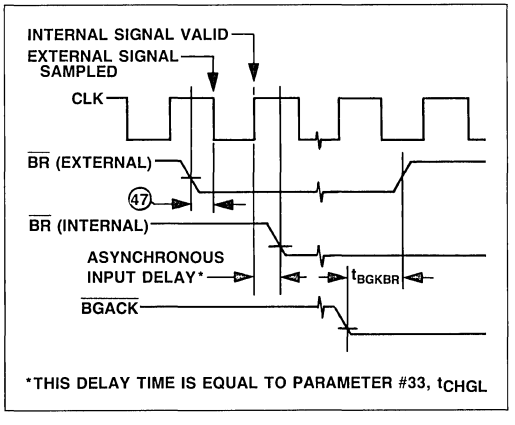


Figure 16. Timing Relationship of External Asynchronous Inputs to Internal Signals

Bus Error Operation. When BERR is asserted, the current bus cycle is terminated. If BERR is asserted before the falling edge of S2, AS will be negated in S7 in either a read or write cycle. As long as BERR remains asserted, the data and address buses will be in the high-impedance state. When BERR is negated, the processor will begin stacking for exception processing. Figure 20 is a timing diagram for the exception sequence. The sequence is composed of the following elements:

1. stacking the program counter and status register,
2. stacking the error information,
3. reading the bus error vector table entry, and
4. executing the bus error handler routine.

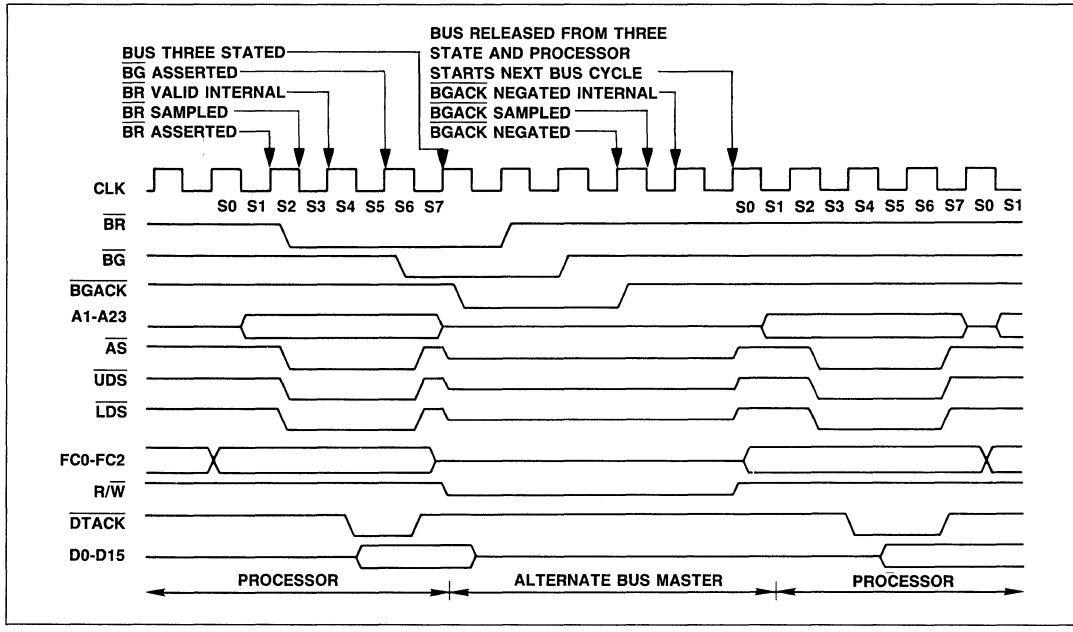


Figure 17. Bus Arbitration During Processor Bus Cycle

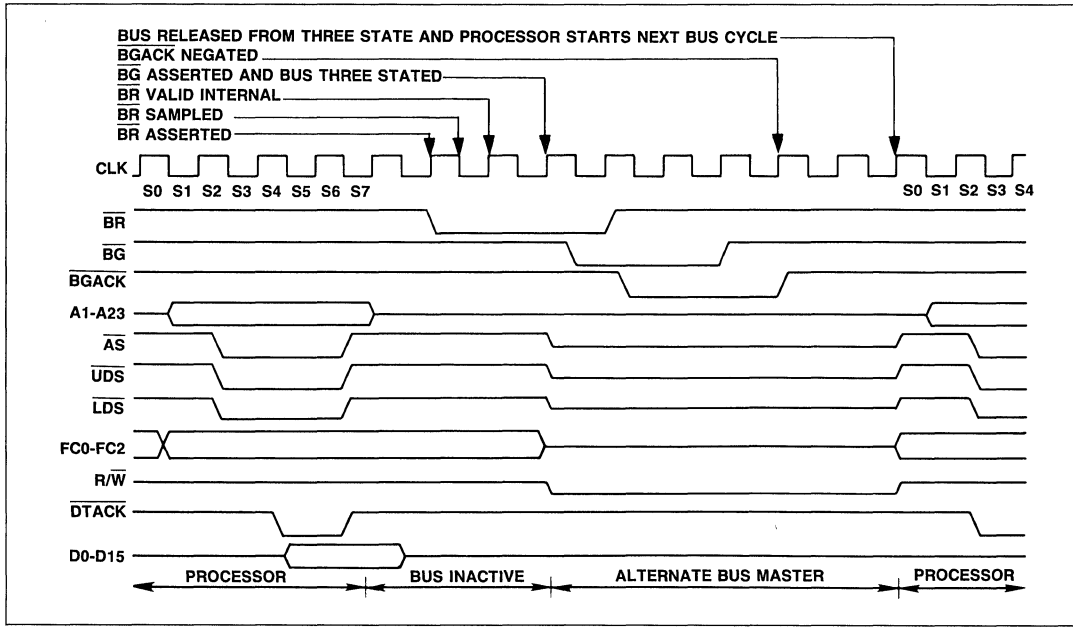


Figure 18. Bus Arbitration with Bus Inactive

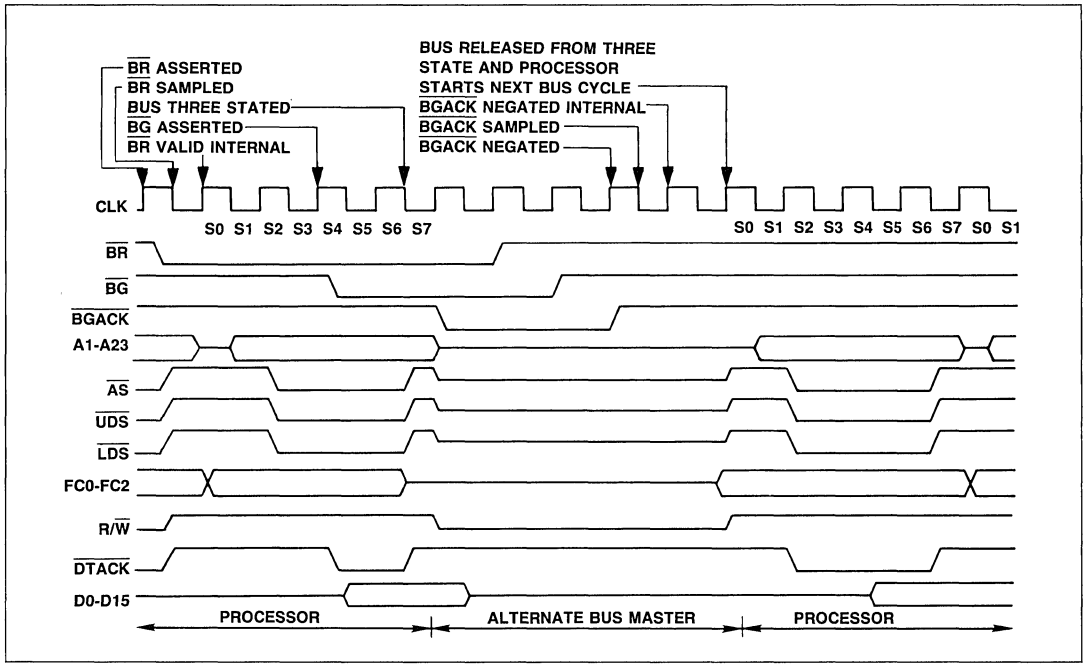


Figure 19. Bus Arbitration During Processor Bus Cycle Special Case

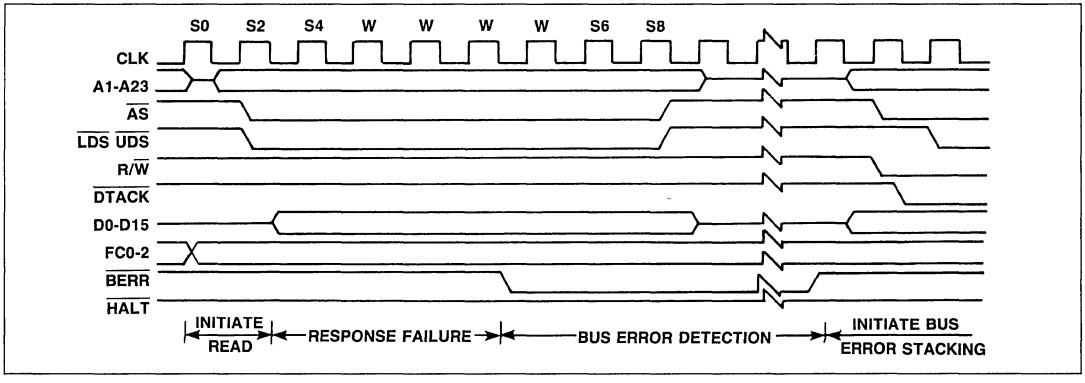


Figure 20. Bus Error Timing Diagram

The stacking of the program counter and the status register is identical to the interrupt sequence. Several additional items are stacked when a bus error occurs. These items are used to determine the nature of the error and correct it, if possible. The bus error vector is vector number two located at address $000008. The processor loads the new program counter from this location. A software bus error handler routine is then executed by the processor. Refer to EXCEPTION PROCESSING for additional information.

Re-Running the Bus Cycle. When, during a bus cycle, the processor receives a BERR, and HALT is being driven by an external device, the processor enters the re-run sequence. Figure 21 is a timing diagram for re-running the bus cycle.

The processor terminates the bus cycle, then puts the address and data output lines in the high-impedance state. The processor remains "halted" and will not run another bus cycle until external logic negates HALT. Then the processor will re-run the previous bus cycle using the same address, the same function codes, the same data (for a write operation), and the same controls. BERR should be negated at least one clock cycle before HALT is negated.

Note

The processor will not re-run a read-modify-write cycle. This restriction is made to guarantee that the entire cycle runs correctly and that the write operation of a Test-and-Set operation is performed without ever releasing AS. If BERR and HALT are asserted during a read-modify-write bus cycle, a bus error operation results.

Halt Operation with No Bus Error. The HALT input signal to the R68000 performs a Halt/Run/Single-Step function in a similar fashion to the R6500 halt functions. When the HALT signal is constantly active the processor "halts" (does nothing) and when the HALT signal is constantly inactive the processor "runs" (does something).

The single-step mode, derived from correctly timed transitions on the HALT signal input, forces the processor to execute a single bus-cycle by entering the "run" mode until the processor starts a bus cycle then changing to the "halt" mode. Thus, the single-step mode allows the user to proceed through (and therefore debug) processor operations one bus cycle at a time.

Figure 22 details the timing required for correct single-step operations. Some care must be exercised to avoid harmful interactions between BERR and HALT when using the single cycle mode as a debugging tool. This is also true of interactions between the HALT and RESET lines since these can reset the machine.

When the processor completes a bus cycle after recognizing that HALT is active, most three-state signals are put in the high-impedance state. These include:

1. address lines, and
2. data lines.

This is required for correct performance of the re-run bus cycle operation.

Honoring the halt request has no effect on bus arbitration. Only the bus arbitration function removes the control signals from the bus.

Total debugging flexibility is derived from the software debugging package, the halt function, and the hardware trace capability. These processor capabilities allow the hardware debugger to trace single bus cycles or single instructions at a time.

Double Bus Faults. When a bus error exception occurs, the processor will attempt to stack several words containing information about the state of the machine. If a bus error exception occurs during the stacking operation, there have been two bus errors in a row, or a double bus fault. A double bus fault causes the processor to halt. Once a bus error exception has occurred, any bus error exception occurring before the execution of the next instruction constitutes a double bus fault.

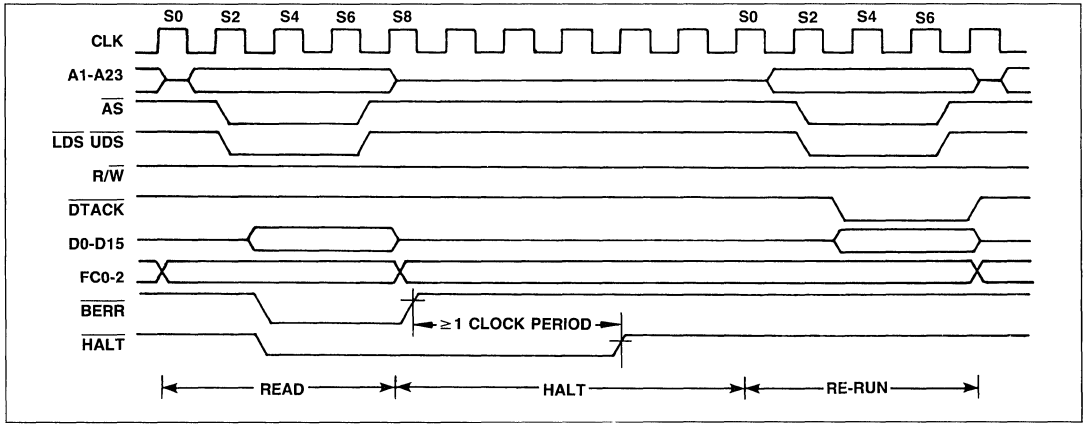


Figure 21. Re-Run Bus Cycle Timing Diagram

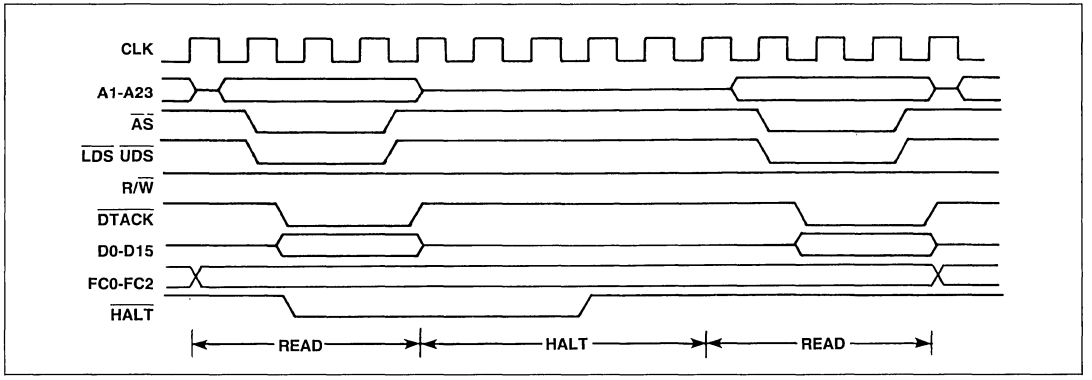


Figure 22. Halt Signal Timing Waveforms

Note that a bus cycle which is re-run does not constitute a bus error exception, and does not contribute to a double bus fault. This means that as long as the external hardware requests it, the processor will continue to re-run the same bus cycle.

The bus error (BERR) pin also has an effect on processor operation after the processor receives an external reset input. The processor reads the vector table after a reset to determine the address to start program execution. If a bus error occurs while reading the vector table (or at any time before the first instruction is executed), the processor reacts as if a double bus fault has occurred and it halts. Only an external reset will start a halted processor.

RESET OPERATION. The reset signal is a bidirectional signal that allows either the processor or an external signal to reset the system. Figure 23 is a timing diagram for reset operations. Both HALT and RESET must be applied to ensure total reset of the processor.

When the RESET and HALT are driven by an external device the entire system, including the processor, is reset. The processor responds by reading the reset vector table entry (vector number zero, address $000000) and loading into the supervisor stack pointer (SSP). Vector table entry number one at address $000004 is read next and loaded into the program counter. The processor initializes the status register to an interrupt level of seven, with no other register being affected.

Execution of the RESET instruction drives the reset pin low for 124 clock periods. In this case, the processor is trying to reset the rest of the system. The internal state of the processor, including the processor's internal registers and the status register, is unaffected by the execution of a RESET instruction. All external devices connected to the reset line will be reset at the completion of the RESET instruction.

Asserting RESET and HALT for 10 clock cycles will cause a processor reset, except when Vcc is initially applied to the processor. In this case, an external reset must be applied for 100 milliseconds.

THE RELATIONSHIP OF DTACK, BERR, AND HALT

In order to properly control termination of a bus cycle for a re-run or a bus error condition, DTACK, BERR, and HALT should be asserted and negated on the rising edge of R68000 clock. This will assure that when two signals are asserted simultaneously, the required setup time (#47) for both of them will be met during the same bus state.

This, or some equivalent precaution, should be designed external to the R68000. Parameter #48 is intended to ensure this operation in a totally asynchronous system, and may be ignored if the above conditions are met.

The preferred bus cycle terminations may be summarized as follows (case numbers refer to Table 4):

Normal Termination: DTACK occurs first (case 1).

Halt Termination: HALT is asserted at same time, or precedes DTACK (no BERR) cases 2 and 3.

Bus Error Termination: BERR is asserted in lieu of, at same time, or preceding DTACK (case 4); BERR negated at same time, or after DTACK.

Re-Run Termination: HALT and BERR asserted in lieu of, at the same time, or before DTACK (cases 6 and 7); HALT must be negated at least one cycle after BERR. (Case 5 indicates BERR may precede HALT which allows fully asynchronous assertion).

Table 4 details the resulting bus cycle termination under various combinations of control signal sequences. The negation of these same control signals under several conditions is shown in Table 5. (DTACK is assumed to be negated normally in all cases; for best results, both DTACK and BERR should be negated when address strobe is negated).

Example A: A system uses a watch-dog timer to terminate accesses to unpopulated address space. The timer asserts DTACK and BERR simultaneously after timeout (case 4).

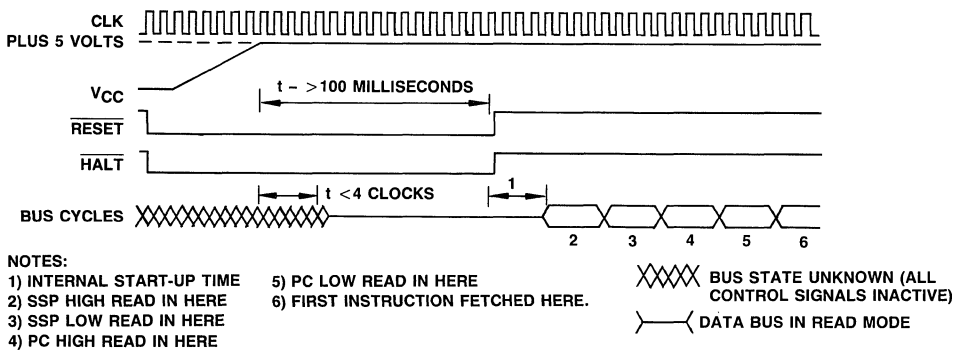


Figure 23. Reset Operation Timing Diagram

Example B: A system uses error detection on RAM contents. Designer may (a) delay DTACK until data verified, and return BERR and HALT simultaneously to re-run error cycle (case 6), or if valid, return DTACK (case 1); (b) delay DTACK until data verified and return BERR at same time as DTACK if data in error (case 4).

ASYNCHRONOUS VERSUS SYNCHRONOUS OPERATION

Asynchronous Operation

To achieve clock frequency independence at a system level, the R68000 can be used in an asynchronous manner. This entails using only the bus handshake lines (AS, UDS, LDS, DTACK, BERR, HALT, and VPA) to control the data transfer. Using this method, AS signals the start of a bus cycle and the data strobes are used as a condition for valid data on a write cycle. The slave device (memory or peripheral) then responds by placing the requested data on the data bus for a read cycle or latching data on a write cycle and asserting the data transfer acknowledge signal (DTACK) to terminate the bus cycle. If no slave reponds or the access is invalid, external control logic asserts the BERR, or BERR and HALT, signal to abort or rerun the bus cycle.

The DTACK signal is allowed to be asserted before the data from a slave device is valid on a read cycle. The length of time that DTACK may precede data is given as parameter #31 (See Figure 45) and it must be met in any asynchronous system to insure that valid data is latched into the processor. Notice that there is no maximum time specified from the assertion of AS to the assertion of DTACK. This is because the MPU will insert wait cycles of one clock period each until DTACK is recognized.

The BERR signal is allowed to be asserted after the DTACK signal is asserted. BERR must be asserted within the time given as parameter #48 after DTACK is asserted in any asynchronous system to insure proper operation. If this maximum delay time is violated, the processor may exhibit erratic behavior.

Synchronous Operation

To allow for those systems which use the system clock as a signal to generate DTACK and other asynchronous inputs, the asynchronous inputs setup time is given as parameter #47. If this setup is met on an input, such as DTACK, the processor is guaranteed to recognize that signal on the next falling edge of the system clock. However, the converse is not true—if the input signal does not meet the setup time it is not guaranteed not to be recognized. In addition, if DTACK is recognized on a falling edge, valid data will be latched into the processor (on a read cycle) on the next falling edge provided that the data meets the setup time given as parameter #27. Given this, parameter #31 may be ignored. Note that if DTACK is asserted, with the required setup time, before the falling edge of S4, no wait states will be incurred and the bus cycle will run at its maximum speed of four clock periods.

In order to assure proper operation in a synchronous system when BERR is asserted after DTACK, the following conditions must be met. Within one clock cycle after DTACK was recognized, BERR must meet the setup time parameter #27A prior to the falling edge of the next clock. The setup time is critical to proper operation, and the R68000 may exhibit erratic behavior if it is violated.

Note

During an active bus cycle, VPA and BERR are sampled on every falling edge of the clock starting with S0. DTACK is sampled on every falling edge of the clock starting with S4 and data is latched on the falling edge of S6 during a read. The bus cycle will then be terminated in S7 except when BERR is asserted in the absence of DTACK, in which case it will terminate one clock cycle later in S9.

Table 4. $\overline{\text{DTACK}}$, $\overline{\text{BERR}}$, $\overline{\text{HALT}}$ Assertion Results

Case No.	Control Signal	Asserted on Rising Edge of State		Result
		N	N + 2	
1	$\overline{\text{DTACK}}$ $\overline{\text{BERR}}$ $\overline{\text{HALT}}$	A NA NA	S X X	Normal cycle terminate and continue.
2	$\overline{\text{DTACK}}$ $\overline{\text{BERR}}$ $\overline{\text{HALT}}$	A NA A	S X S	Normal cycle terminate and halt. Continue when $\overline{\text{HALT}}$ removed.
3	$\overline{\text{DTACK}}$ $\overline{\text{BERR}}$ $\overline{\text{HALT}}$	NA NA A	A NA S	Normal cycle terminate and halt. Continue when $\overline{\text{HALT}}$ removed.
4	$\overline{\text{DTACK}}$ $\overline{\text{BERR}}$ $\overline{\text{HALT}}$	X A NA	X S NA	Terminate and take bus error trap.
5	$\overline{\text{DTACK}}$ $\overline{\text{BERR}}$ $\overline{\text{HALT}}$	NA A NA	X S A	Terminate and re-run.
6	$\overline{\text{DTACK}}$ $\overline{\text{BERR}}$ $\overline{\text{HALT}}$	X A A	X S S	Terminate and re-run when $\overline{\text{HALT}}$ removed.
7	$\overline{\text{DTACK}}$ $\overline{\text{BERR}}$ $\overline{\text{HALT}}$	NA NA A	X A S	Terminate and re-run when $\overline{\text{HALT}}$ removed.

Legend:
N — the number of the current even bus state (e.g., S4, S6, etc.)
A — signal is asserted in this bus state
NA — signal is not asserted in this state
X — don't care
S — signal was asserted in previous state and remains asserted in this state

Table 5. $\overline{\text{BERR}}$ AND $\overline{\text{HALT}}$ Negation Results

Conditions of Termination in Table 4-4	Control Signal	Negated on Rising Edge of State			Results — Next Cycle
		N		N + 2	
Bus Error	$\overline{\text{BERR}}$ $\overline{\text{HALT}}$	● ●	or or	● ●	Takes bus error trap.
Re-run	$\overline{\text{BERR}}$ $\overline{\text{HALT}}$	● ●	or	●	Illegal sequence; usually traps to vector number 0.
Re-run	$\overline{\text{BERR}}$ $\overline{\text{HALT}}$	●		● ●	Re-runs the bus cycle.
Normal	$\overline{\text{BERR}}$ $\overline{\text{HALT}}$	● ●	or	●	May lengthen next cycle.
Normal	$\overline{\text{BERR}}$ $\overline{\text{HALT}}$	●	or	● none	If next cycle is started it will be terminated as a bus error.

● = Signal is negated in this bus state.

PROCESSING STATES

The following paragraphs describe the actions of the R68000 which are outside the normal processing associated with the execution of instructions. The functions of the bits in the supervisor portion of the status register are covered: the supervisor/user bit, the trace enable bit, and the processor interrupt priority mask. The sequence of memory references and actions taken by the processor on exception conditions are detailed.

The R68000 is always in one of three processing states: normal, exception, or halted. The normal processing state associated with instruction execution; the memory references are to fetch instructions and operands, and to store results. A special case of the normal state is the stopped state which the processor enters when a STOP instruction is executed. In this state, no further references are made.

The exception processing state is associated with interrupts, trap instructions, tracing and other exceptional conditions. The exception may be internally generated by an instruction or by an unusual condition arising during the execution of an instruction. Externally, exception processing can be forced by an interrupt, by a bus error, or by a reset. Exception processing is designed to provide an efficient context switch so that the processor may handle unusual conditions.

The halted processing state is an indication of a catastrophic hardware failure. For example, if during the exception processing of a bus error another bus error occurs, the processor assumes that the system is unusable and halts. Only an external reset can restart a halted processor. Note that a processor in the stopped state is not in the halted state, nor vice versa.

PRIVILEGE STATES

The processor operates in one of two states of privilege: the "user" state or the "supervisor" state. The privilege state determines legal operations. It is used to choose between the supervisor stack pointer and the user stack pointer in instruction references, and by the external memory management device to control and translate accesses.

The privilege state is a mechanism for providing security in a computer system by allowing most programs to execute in user state. In this state, the accesses are controlled, and the effects on other parts of the system are limited. Programs should access only their own code and data areas, and ought to be restricted from accessing information.

The operating system which executes in the supervisor state, has access to all resources and performs the overhead tasks for the user state programs.

SUPERVISOR STATE. The supervisor state is the higher state of privilege. For instruction execution, the supervisor state is determined by asserting (high) the S-bit of the status register. All instructions can be executed in the supervisor state. The bus cycles generated by instructions executed in the supervisor state are classified as supervisor references. While the processor is in the supervisor privilege state, those instructions which use either the system stack pointer implicitly or address register seven explicitly access the supervisor stack pointer.

All exception processing is done in the supervisor state, regardless of the setting of the S-bit. The bus cycles generated during exception processing are classified as supervisor references. All stacking operations during exception processing use the supervisor stack pointer.

USER STATE. The user state is the lower state of privilege. For instruction execution, the user state is determined by negating (low) the S-bit of the status register.

Most instructions execute the same in user state as in the supervisor state. However, some instructions which have important system effects are made privileged. User programs are not permitted to execute the STOP instruction, or the RESET instruction. To ensure that a user program cannot enter the supervisor state except in a controlled manner, the instructions which modify the whole state register are priviled. To aid in debugging programs which are to be used as operating systems, the move to user stack pointer (MOVE to USP) and move from user stack pointer (MOVE from USP) instructions are also privileged.

The bus cycles generated by an instruction executed in user state are classified as user state references. This allows an external memory management device to translate the address and to control access to protected portions of the address space. While the processor is in user privilege state, those instructions which use either the system stack pointer implicitly or address register seven explicitly, access the user stack pointer.

PRIVILEGE STATE CHANGES. Once the processor is in the user state and executing instructions, only exception processing can change the privilege state. During exception processing, the current setting of the S-bit of the status register is saved and the S-bit is asserted, putting the processing in the supervisor state. Therefore, when instruction execution resumes to process the exception, the processor is in the supervisor privilege state.

REFERENCE CLASSIFICATION. When the processor makes a reference, it classifies the kind of reference being made by using the encoding on the three function code output lines. This allows external translation of addresses, control of access, and differentiation of special processor states, such as interrupt acknowledge. Table 6 lists the classification of references.

Table 6. Reference Classification

Function Code Output			
FC2	FC1	FC0	Reference Class
0	0	0	(Unassigned)
0	0	1	User Data
0	1	0	User Program
0	1	1	(Unassigned)
1	0	0	(Unassigned)
1	0	1	Supervisor Data
1	1	0	Supervisor Program
1	1	1	Interrupt Acknowledge

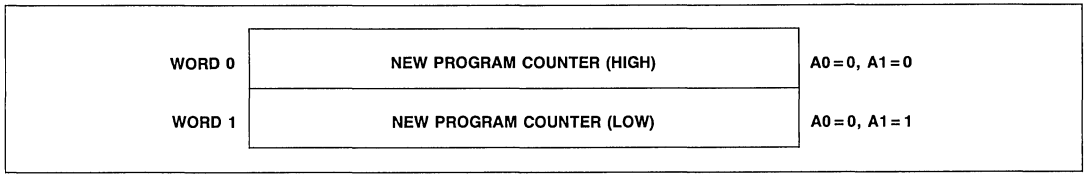


Figure 24. Exception Vector Format

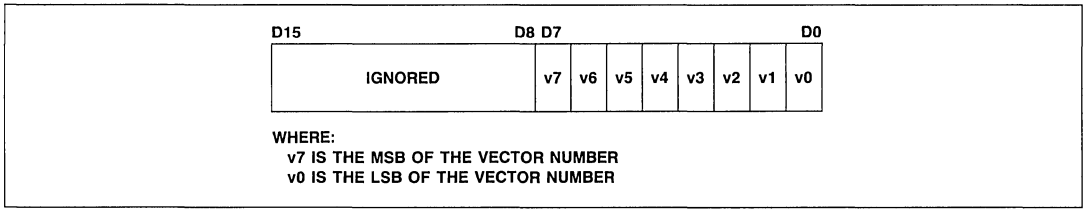


Figure 25. Peripheral Vector Number Format

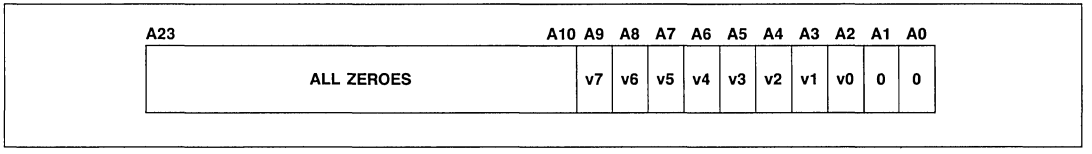


Figure 26. Address Translated From 8-Bit Vector Number

EXCEPTION PROCESSING

Before discussing the details of interrupts, traps, and tracing, a general description of exception processing is in order. The processing of an exception occurs in four steps, with variations for different exception causes. During the first step, a temporary copy of the status register is made, and the status register is set for exception processing. In the second step the exception vector is determined, and the third step is the saving of the current processor contents. In the fourth step a new context is obtained, and the processor switches to instruction processing.

EXCEPTION VECTORS. Exception vectors are memory locations from which the processor fetches the address of a routine which will handle that exception. All exception vectors are two words in length (Figure 24), except for the reset vector, which is four words. All exception vectors lie in the supervisor data space, except for the reset vector which is in the supervisor program space. A vector number is an eight-bit number which, when multipled by four, gives the address of an exception vector. Vector numbers are generated internally or externally, depending on the cause of the exception. In the case of interrupts, during the interrupt acknowledge bus cycle, a peripheral provides an 8-bit vector number (Figure 25) to the processor on data bus lines D0 through D7. The processor translates the vector number into a full 24-bit address, as shown in Figure 26. The memory layout for exception vectors is given in Table 7.

As shown in Table 7, the memory layout is 512 words long (1024 bytes). It starts at address 0 and proceeds through address 1023. This provides 255 unique vectors; some of these are reserved for TRAPS and other system functions. Of the 255, there are 192 reserved for user interrupt vectors. However, there is no protection on the first 64 entries, so user interrupt vectors may overlap at the discretion of the systems designer.

KINDS OF EXCEPTIONS. Exceptions can be generated either internally or externally. Externally generated exceptions include interrupts ($\overline{IRQ}$), bus error ($\overline{BERR}$), and reset ($\overline{RESET}$) requests. Interrupts are requests from peripheral devices for processor action while $\overline{BERR}$ and $\overline{RESET}$ inputs are used for access control and processor restart. Internally generated exceptions come from instructions, from address errors, or from tracing. The trap (TRAP), trap on overflow (TRAPV), check register against bounds (CHK) and divide (DIV) instructions can all generate exceptions as part of their instruction execution. In addition, illegal instructions, word fetches from odd addresses and privilege violations cause exceptions. Tracing behaves like a very high priority, internally generated interrupt after each instruction execution.

EXCEPTION PROCESSING SEQUENCE. Exception processing occurs in four identifiable steps. In the first step, an internal copy is made of the status register. After the copy is made, the S-bit is asserted, putting the processor into the supervisor privilege state. Also, the T-bit is negated which will allow the exception handler to execute unhindered by tracing. For the reset and interrupt exceptions, the interrupt priority mask is also updated.

Table 7. Exception Vector Assignment

Vector Number(s)	Address			Assignment
	Dec	Hex	Space	
0	0	000	SP	Reset: Initial SSP
—	4	004	SP	Reset: Initial PC
2	8	008	SD	Bus Error
3	12	00C	SD	Address Error
4	16	010	SD	Illegal Instruction
5	20	014	SD	Zero Divide
6	24	018	SD	CHK Instruction
7	28	01C	SD	TRAPV Instruction
8	32	020	SD	Privilege Violation
9	36	024	SD	Trace
10	40	028	SD	Line 1010 Emulator
11	44	02C	SD	Line 1111 Emulator
12*	48	030	SD	(Unassigned, reserved)
13*	52	034	SD	(Unassigned, reserved)
14*	56	038	SD	(Unassigned, reserved)
15	60	03C	SD	Uninitialized Interrupt Vector
16-23*	64	04C	SD	(Unassigned, reserved)
	95	05F		—
24	96	060	SD	Spurious Interrupt
25	100	064	SD	Level 1 Interrupt Autovector
26	104	068	SD	Level 2 Interrupt Autovector
27	108	06C	SD	Level 3 Interrupt Autovector
28	112	070	SD	Level 4 Interrupt Autovector
29	116	074	SD	Level 5 Interrupt Autovector
30	120	078	SD	Level 6 Interrupt Autovector
31	124	07C	SD	Level 7 Interrupt Autovector
32-47	128	080	SD	TRAP Instruction Vectors
	191	0BF		—
48-63*	192	0C0	SD	(Unassigned, reserved)
	255	0FF		—
64-255	256	100	SD	User Interrupt Vectors
	1023	3FF		—

*Vector numbers 12, 13, 14, 16 through 23, and 48 through 63 are reserved for future enhancements. No user peripheral devices should be assigned these numbers.

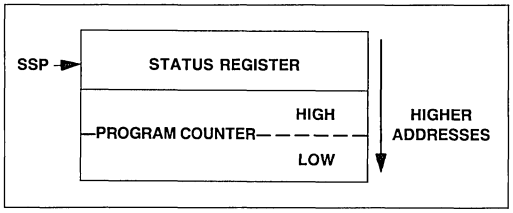


Figure 27. Exception Stack Order (Groups 1 and 2)

In the second step, the vector number of the exception is determined. For interrupts, the vector number is obtained by a processor fetch, classified as an interrupt acknowledge. For all other exceptions, internal logic provides the vector number. This vector number is then used to generate the address of the exception vector.

The third step is to save the current processor status except for the reset exception. The current program counter value and the saved copy of the status register are stacked using the supervisor stack pointer as shown in Figure 27. The program counter value stacked usually points to the next unexecuted instruction; however, for bus error and address error, the value stacked for the program counter is unpredictable, and may be incremented from the address of the instruction which caused the error. Additional information defining the current context is stacked for the bus error and address error exceptions.

The last step is the same for all exceptions. The new program counter value is fetched from the exception vector. The processor then resumes instruction execution. The instruction at the address given in the exception vector is fetched, and normal instruction decoding and execution is started.

MULTIPLE EXCEPTIONS. These paragraphs describe the processing which occurs when multiple exceptions arise simultaneously. Exceptions can be grouped according to their occurrence and priority. The Group 0 exceptions are reset, bus error, and address error. These exceptions cause the instruction currently being executed to be aborted, and the exception processing to commence within two clock cycles. The Group 1 exceptions are trace and interrupt, as well as the privilege violations and illegal instructions. These exceptions allow the current instruction to execute to completion, but preempt the execution of the next instruction by forcing exception processing to occur (privilege violations and illegal instructions are detected when they are the next instruction to be executed). The Group 2 exceptions occur as part of the normal processing of instructions. The TRAP, TRAPV, CHK, and zero divide exceptions are in this group. For these exceptions, the normal execution of an instruction may lead to exception processing.

Group 0 exceptions have highest priority, while Group 2 exceptions have lowest priority. Within Group 0, reset has highest priority, followed by address error and then bus error. Within Group 1, trace has priority over external interrupts, which in turn takes priority over illegal instruction and privilege violation. Since only one instruction can be executed at a time, there is no priority relation within Group 2.

Table 8. Exception Grouping and Priority

Group	Exception	Processing
0	Reset Address Error Bus Error	Exception processing begins within two clock cycles.
1	Trace Interrupt Illegal Instruction Privilege Violation	Exception processing begins before the next instruction.
2	TRAP, TRAPV, CHK, Zero Divide	Exception processing is started by normal instruction execution

The priority relation between two exceptions determines which is taken first if the conditions for both arise simultaneously. Therefore, if a bus error occurs during a TRAP instruction, the bus error takes precedence, and the TRAP instruction processing is aborted. In another example, if an interrupt request occurs during the execution of an instruction while the T-bit is asserted, the trace exception has priority, and is processed first. Before instruction processing resumes, however, the interrupt exception is also processed, and instruction processing commences finally in the interrupt handler routine. Table 8 gives a summary of exception grouping and priority.

4

EXCEPTION PROCESSING DETAILED DISCUSSION

Exceptions have a number of sources, and each exception has a unique processing sequence. The following paragraphs detail the sources of exceptions, how each arises, and how each is processed.

RESET. The reset input provides the highest exception level. The processing of the reset signal is designed for system initiation, and recovery from catastrophic failure. Any processing in progress at the time of the reset is aborted and cannot be recovered. The processor is forced into the supervisor state and the trace state is forced off. The processor interrupt priority mask is set at level seven. The vector number is internally generated to reference the reset exception vector at location 0 in the supervisor program space. Because no assumptions can be made about the validity of register contents, in particular the supervisor stack pointer, neither the program counter nor the status register is saved. The address contained in the first two words of the reset exception vector is fetched as the initial supervisor stack pointer, and the address in the last two words of the reset exception vector is fetched as the initial program counter. Finally, instruction execution is started at the address in the program counter. The powerup/restart code should be pointed to by the initial program counter.

The RESET instruction does not cause loading of the reset vector, but does assert the reset line to reset external devices. This allows the software to reset the system to a known state and then continue processing with the next instruction.

INTERRUPTS. Seven levels of interrupt priorities are provided. Devices may be chained externally within interrupt priority levels, allowing an unlimited number of peripheral devices to interrupt the processor. Interrupt priority levels are numbered from one to seven, level seven being the highest priority. The status register contains a three-bit mask which indicates the current processor priority. Interrupts are inhibited for all priority levels less than or equal to the current processor priority.

An interrupt request is made to the processor by encoding the interrupt request level on the interrupt request lines; a zero indicates no interrupt request. Interrupt requests arriving at the processor do not face immediate exception processing, but are made pending. Pending interrupts are detected between instruction executions. If the priority of the pending interrupt is lower than or equal to the current processor priority, execution continues with the next instruction and the interrupt exception processing is postponed. (The recognition of level seven is slightly different, as explained in a following paragraph.)

If the priority of the pending interrupt is greater than the current processor priority, the exception processing sequence is started. First a copy of the status register is saved, and the privilege state is set to supervisor, then tracing is suppressed, and the processor priority level is set to the level of the interrupt being acknowledged. The processor fetches the vector number from the interrupting device, classifying the reference as an interrupt acknowledge and displaying the level number of the interrupt being acknowledged on the address bus. If external logic requests an automatic vectoring, the processor internally generates a vector number which is determined by the interrupt level number. If external logic indicates a bus error, the interrupt is taken to be spurious, and the generated vector number references the spurious interrupt vector. The processor then proceeds with the usual exception processing, saving the program counter and status register on the supervisor stack. The saved value of the program counter is the address of the instruction which would have been executed had the interrupt not been present. The content of the interrupt vector whose vector number was previously obtained is fetched and loaded into the program counter, and normal instruction execution commences in the interrupt handling routine. A flow chart for the interrupt acknowledge sequence is given in Figure 28, a timing diagram is given in Figure 29, and the interrupt exception timing sequence is shown in Figure 30.

Priority level seven is a special case. Level seven interrupts cannot be inhibited by the interrupt priority mask, thus providing a "non-maskable interrupt" capability. An interrupt is generated each time the interrupt request level changes from some lower level to level seven. Note that a level seven interrupt may still be caused by the level comparison if the request level is a seven and the processor priority is set to a lower level by an instruction.

UNINITIALIZED INTERRUPT. An interrupting device asserts $\overline{VPA}$ or provides an interrupt vector during an interrupt acknowledge cycle to the R68000. If the vector register has not been initialized, the responding R68000 Family peripheral will provide vector 15, the uninitialized interrupt vector. This provides a uniform way to recover from a programming error.

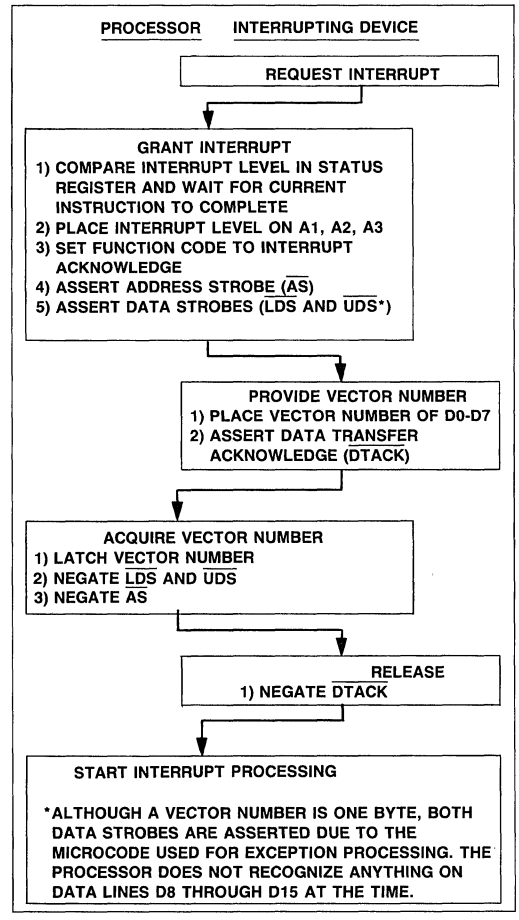


Figure 28. Interrupt Acknowledge Sequence Flow Chart

SPURIOUS INTERRUPT. If during the interrupt acknowledge cycle no device responds by asserting $\overline{DTACK}$ or $\overline{VPA}$, the bus error line should be asserted to terminate the vector acquisition. The processor separates the processing of this error from bus error by fetching the spurious interrupt vector instead of the bus error vector. The processor then proceeds with the usual exception processing.

INSTRUCTION TRAPS. Traps are exceptions caused by instructions. They arise either from processor recognition of abnormal conditions during instruction execution, or from use of instructions whose normal behavior is trapping.

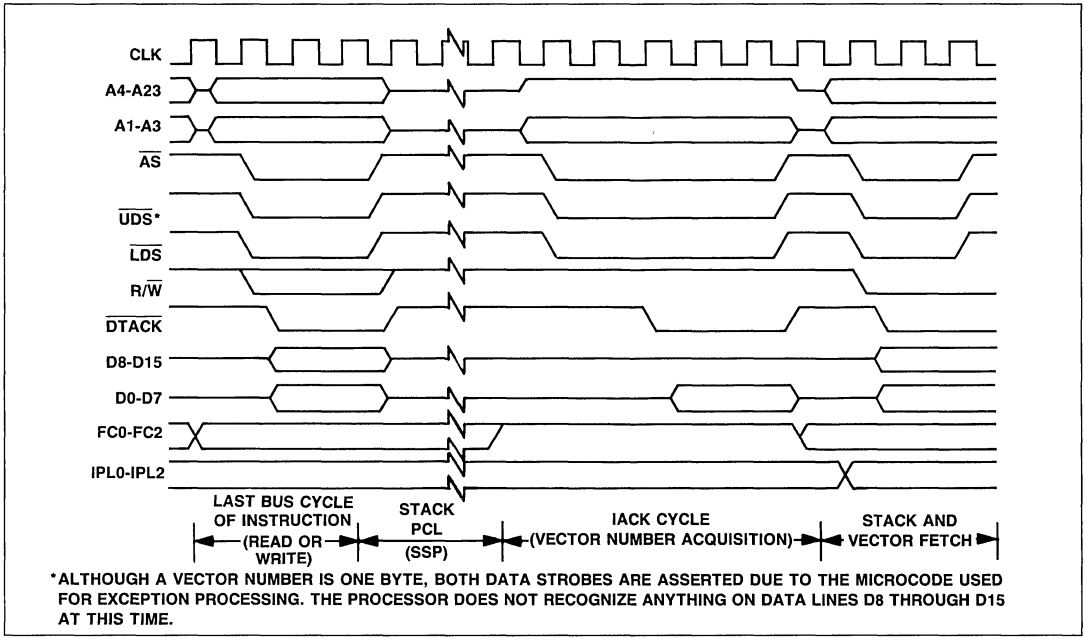


Figure 29. Interrupt Acknowledge Sequence Timing Diagram

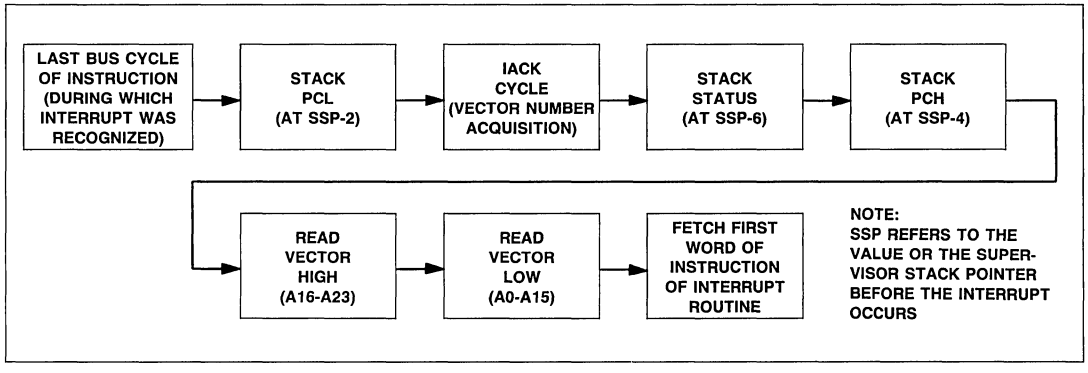


Figure 30. Interrupt Exception Timing Sequence

Some instructions are used specifically to generate traps. The TRAP instruction always forces an exception, and is useful for implementing system calls for user programs. The TRAPV and CHK instructions force an exception if the user program detects a runtime error, which may be an arithmetic overflow or a subscript out of bounds.

The signed divide (DIVS) and unsigned divide (DIVU) instructions will force an exception if a division operation is attempted with a divisor of zero.

ILLEGAL AND UNIMPLEMENTED INSTRUCTIONS. Illegal instruction refers to any of the word bit patterns which are not the bit pattern of the first word of a legal instruction. During instruction execution, if such an instruction is fetched, an illegal instruction exception occurs. Rockwell reserves the right to define instructions whose opcodes may be any of the illegal instructions. Three bit patterns will always force an illegal instruction trap on all R68000 Family compatible microprocessors. They are: $4AFA, $4AFB, and $4AFC. Two of the patterns, $4AFA and $4AFB, are reserved for Rockwell system products. The third pattern, $4AFC, is reserved for customer use.

Word patterns with bits 15 through 12 equaling 1010 or 1111 are distinguished as unimplemented instructions and separate exception vectors are given to these patterns to permit efficient emulation. This facility allows the operating system to detect program errors, or to emulate unimplemented instructions in software.

PRIVILEGE VIOLATIONS. In order to provide system security, various instructions are privileged. An attempt to execute one of the privileged instructions while in the user state will cause an exception. The privileged instructions are:

STOP	AND Immediate to SR
RESET	EOR Immediate to SR
RTE	OR Immediate to SR
MOVE USP	MOVE to SR

TRACING. To aid in program development, the R68000 includes a facility to allow instruction by instruction tracing. In the trace state, after each instruction is executed an exeception is forced, allowing a debugging program to monitor the execution of the program under test.

The trace facility uses the T-bit in the supervisor portion of the status register. If the T-bit is negated (off), tracing is disabled, and instruction execution proceeds from instruction to instruction as normal. If the T-bit is asserted (on) at the beginning of the execution of an instruction, a trace exception will be generated after the execution of that instruction is completed. If the instruction is not executed, either because an interrupt is taken, or the instruction is illegal or privileged, the trace exception does not occur. The trace exception also does not occur if the instruction is aborted by a reset, bus error, or address error exception. If the instruction is indeed executed and an interrupt is pending on completion, the trace exception is processed before the interrupt exception. If, during the execution of the instruction, an exception is forced by that instruction, the forced exception is processed before the trace exception.

As an extreme illustration of the above rules, consider the arrival of an interrupt during the execution of a TRAP instruction while tracing is enabled. First the trap exception is processed, then the trace exception, and finally the interrupt exception. Instruction execution resumes in the interrupt handler routine.

BUS ERROR. Bus error exceptions occur when the external logic requests that a bus error be processed by an exception. The current bus cycle which the processor is making is then aborted. Whether the processor was doing instruction or exception processing, that processing is terminated, and the processor immediately begins exception processing.

Exception processing for bus error follows the usual sequence of steps. The status register is copied, the supervisor state is entered, and the trace state is turned off. The vector number is generated to refer to the bus error vector. Since the processor was not between instructions when the bus error exception request was made, the context of the processor is more detailed. To save more of this context, additional information is saved on the supervisor stack. The program counter and the copy of the status register are of course saved. The value saved for the program counter is advanced by some amount, two to ten bytes beyond the address of the first word of the instruction which made the reference causing the bus error. If the bus error occurred during the fetch of the next instruction, the saved program counter has a value in the vicinity of the current instruction, even if the current instruction is a branch, a jump, or a return instruction. Besides the usual information, the processor saves its internal copy of the first word of the instruction being processed, and the address which was being accessed by the aborted bus cycle. Specific information about the access is also saved: whether it was a read or a write, whether the processor was processing an instruction or not, and the classification displayed on the function code outputs when the bus error occurred. The processor is processing an instruction if in the normal state or processing a Group 2 exception; the processor is not processing an instruction when processing a Group 0 or a Group 1 exception. Figure 31 illustates how the information is organized on the supervisor stack. Although this information is not sufficient to effect full recovery from the bus error, it does allow software diagnosis. Finally, the processor commences instruction processing at the address contained in the vector. It is the responsibility of the error handler routine to clean up the stack and determine where to continue execution.

If a bus error occurs during the exception processing for a bus error, address error, or reset, the processor is halted, and all processing ceases. This simplifies the detection of catastrophic system failure, since the processor removes itself from the system rather than destroy all memory contents. Only the $\overline{\text{RESET}}$ pin can restart a halted processor.

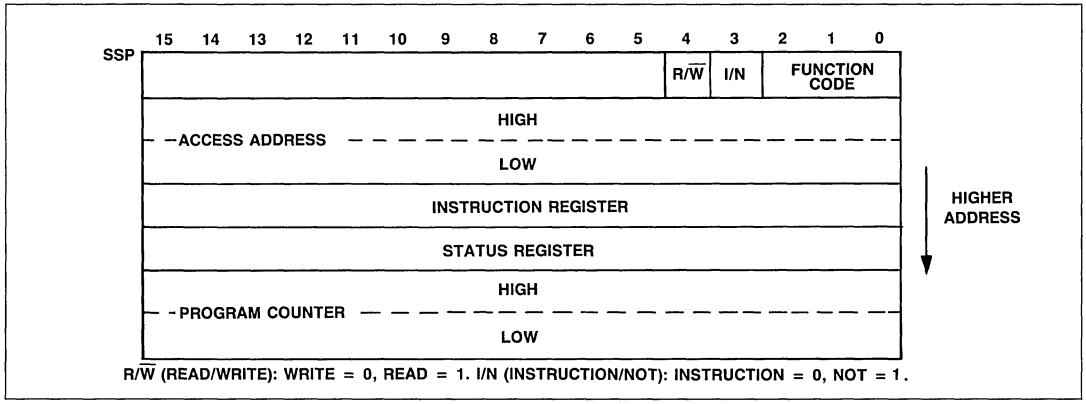


Figure 31. Supervisor Stack Order (Group 0)

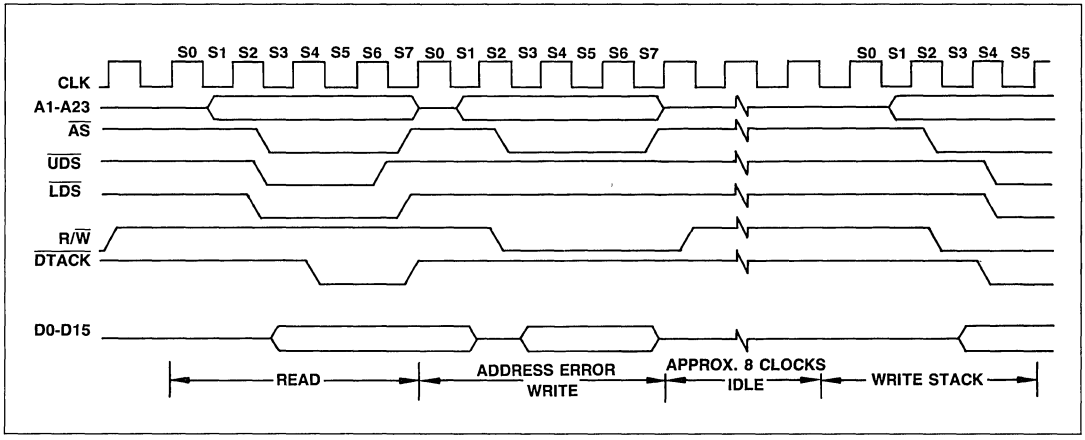


Figure 32. Address Error Timing

ADDRESS ERROR. Address error exceptions occur when the processor attempts to access a word or a long word operand or an instruction at an odd address. The effect is much like an internally generated bus error, so that the bus cycle is aborted, and the processor ceases whatever processing it is currently doing and begins exception processing. After exception processing commences, the sequence is the same as that for bus error including the information that is stacked, except that the vector number refers to the address error vector instead. Likewise, if an address error occurs during the exception processing for a bus error, address error, or reset, the processor is halted. As shown in Figure 32, an address error will execute a short bus cycle followed by an exception processing.

INTERFACE WITH R6500 PERIPHERALS

Rockwell's line of R6500 peripherals are directly compatible with the R68000. Some of these devices that are particularly useful are:

- R6520 Peripheral Interface Adapter (PIA)
- R6522 Versatile Interface Adapter (VIA)
- R6545 CRT Controller (CRTC)
- R6551 Asynchronous Communication Interface Adapter (ACIA)

To interface the synchronous R6500 peripherals with the asynchronous R68000, the processor modifies its bus cycle to meet the R6500 cycle requirements whenever an R6500 device address is detected. This is possible since both processors use memory mapped I/O. Figure 33 is a flow chart of the interface operation between the processor and R6500 devices. 6800 peripherals are also compatible with the R68000 processor.

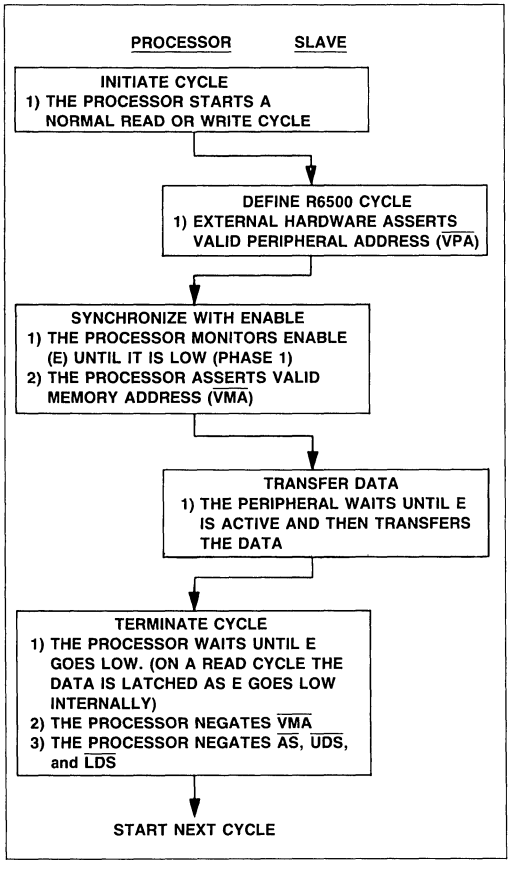


Figure 33. R6500 Interfacing Flow Chart

DATA TRANSFER OPERATION

Three signals on the processor provide the R6500 interface. They are: enable (E), valid memory address ($\overline{VMA}$), and valid Peripheral address ($\overline{VPA}$). Enable corresponds to the E or Ø2 signal in existing R6500 systems. The bus frequency is one tenth of the incoming R68000 clock frequency. The timing of E allows 1 MHz peripherals to be used with an 8 MHz R68000. Enable has a 60/40 duty cycle; that is, it is low for six input clocks and high for four input clocks. This duty cycle allows the processor to do successive $\overline{VPA}$ accesses on successive E pulses.

Figures 34 and 35 give a general R6500 to R68000 interface timing, while Figures 36 and 37 detail the specific timing parameters involved in the interface. At state zero (S0) in the cycle, the address bus is in the high-impedance state. A function code is asserted on the function code output lines. One-half clock later, in state 1, the address bus is released from the high-impedance state.

During state 2, the address strobe ($\overline{AS}$) is asserted to indicate that there is a valid address on the address bus. If the bus cycle is a read cycle, the upper and/or lower data strobes are also asserted in state 2. If the bus cycle is a write cycle, the read/write (R/$\overline{W}$) signal is switched to a low (write) during state 2. One-half clock later, in state 3, the write data is placed on the data bus, and in state 4 the data strobes are issued to indicate valid data on the data bus. The processor now inserts wait states until it recognizes the assertion of $\overline{VPA}$.

The $\overline{VPA}$ input signals the processor that the address on the bus is the address of an R6500 device (or an area reserved for R6500 devices) and that the bus should conform to the Ø2 transfer characteristics of the R6500 bus. Valid peripheral address ($\overline{VPA}$) is derived by decoding the address bus, conditioned by address strobe ($\overline{AS}$). Chip select for the R6500 peripherals should be derived by decoding the address bus conditioned by $\overline{VMA}$.

After the recognition of $\overline{VPA}$, the processor assures that the Enable (E) is low, by waiting if necessary, and subsequently asserts $\overline{VMA}$. Valid memory address is then used as part of the chip select equation of the peripheral. This ensures that the R6500 peripherals are selected and deselected at the correct time. The peripheral now runs its cycle during the high portion of the E signal. Figures 34 and 35 depict the best and worst case R6500 cycle timing. This cycle length is dependent strictly upon when $\overline{VPA}$ is asserted in relationship the E clock.

If we assume that external circuitry asserts $\overline{VPA}$ as soon as possible after the assertion of $\overline{AS}$, then $\overline{VPA}$ will be recognized as being asserted on the falling edge of S4. In this case, no "extra" wait cycles will be inserted prior to the recognition of $\overline{VPA}$ assertion and only the wait cycles inserted to synchronize with the E clock will determine the total length of the cycle. In any case, the synchronization delay will be some integral number of clock cycles within the following two extremes:

1. Best Case—$\overline{VPA}$ is recognized as being asserted on the falling edge three clock cycles before E rises (or three clock cycles after E falls).

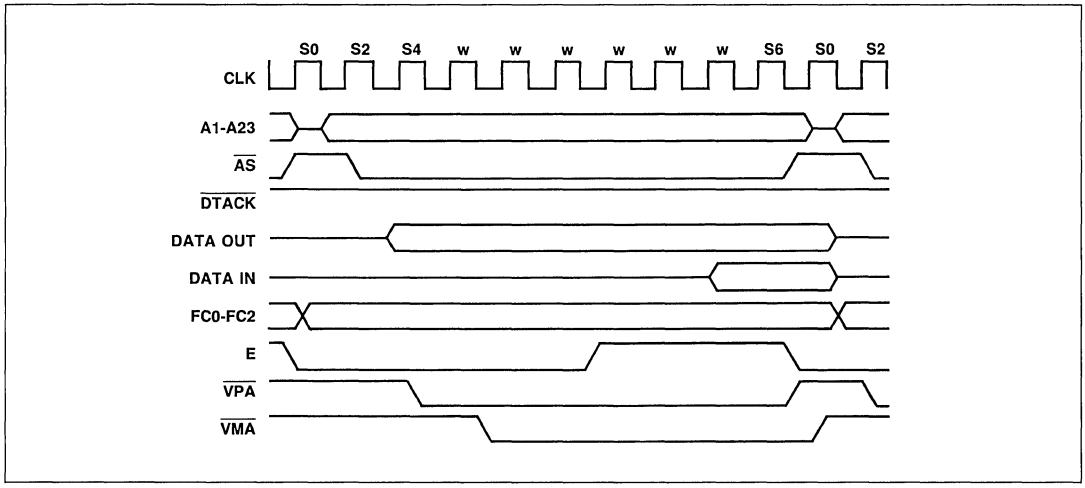


Figure 34. R68000 to R6500 Peripheral Timing—Best Case

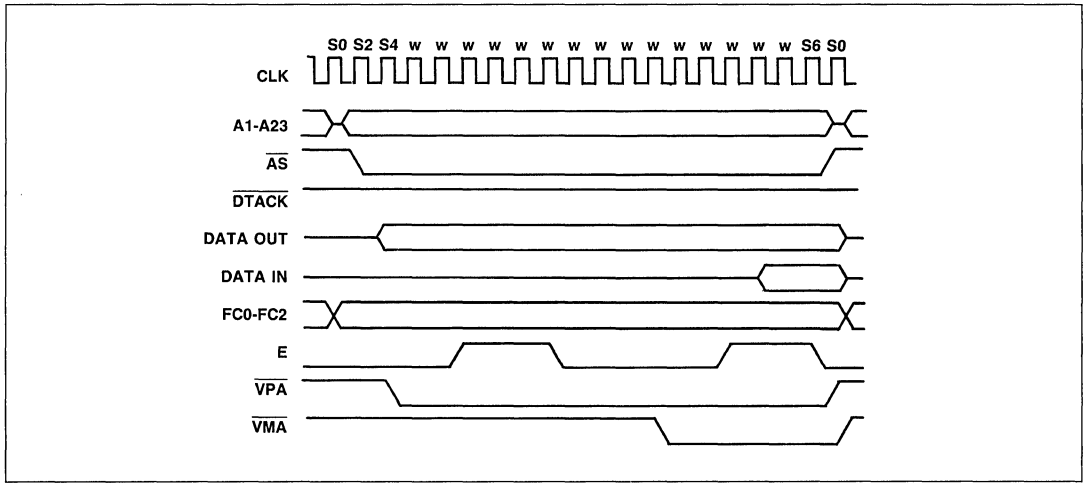
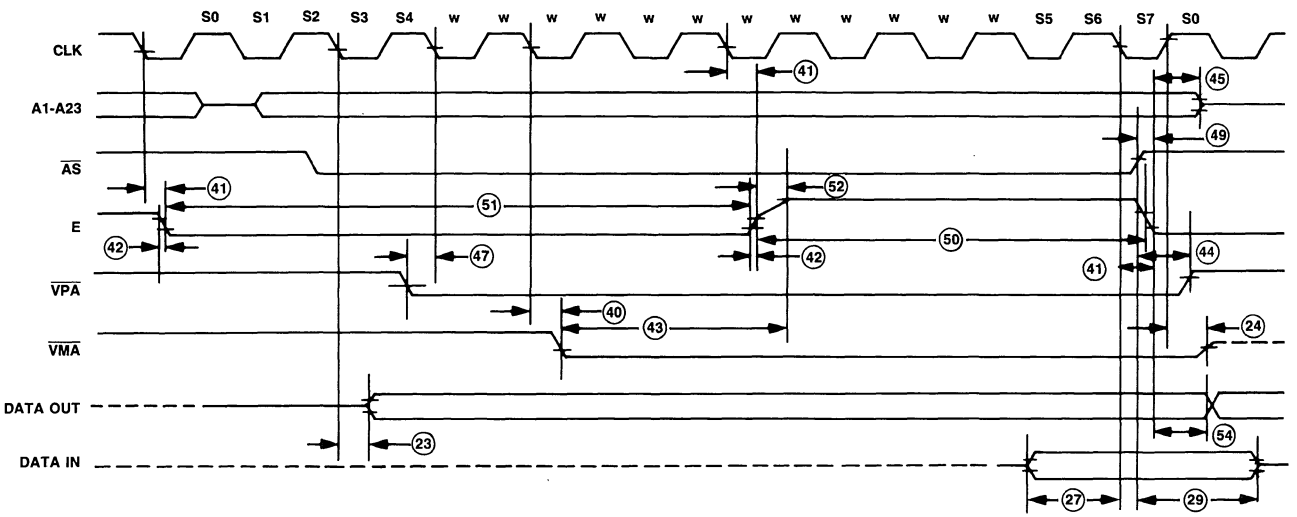


Figure 35. R68000 to R6500 Peripheral Timing—Worst Case



NOTES:
THIS FIGURE REPRESENTS THE BEST CASE R6500 TIMING WHERE $\overline{VPA}$ FALLS BEFORE THE THIRD SYSTEM CLOCK CYCLE AFTER THE FALLING EDGE OF E.

THIS TIMING DIAGRAM IS INCLUDED FOR THOSE WHO WISH TO DESIGN THEIR OWN CIRCUIT TO GENERATE $\overline{VMA}$ IT SHOWS THE BEST CASE POSSIBLY ATTAINABLE.

Figure 36. R6500 Timing—Best Case

2. Worst Case—$\overline{VPA}$ is recognized as being asserted on the falling edge two clock cycles before E rises (or four clock cycles after E falls).

Near the end of a read cycle, the processor latches the peripheral's data in state 6. For all cycles, the processor negates the address and data strobes one half clock cycle later in state 7, and the Enable signal goes low at this time. Another half clock later, the address bus is put in the high-impedance state. Upon write cycle completion, the data bus is put in the high-impedance state and the read/write signal is switched high. The peripheral logic must remove $\overline{VPA}$ within one clock after address strobe is negated.

$\overline{DTACK}$ should not be asserted while $\overline{VPA}$ is asserted. Note that the R68000 $\overline{VMA}$ is active low. This allows the processor to put its buses in the high-impedance state on DMA requests without inadvertently selecting peripherals.

INTERRUPT OPERATION

During an interrupt acknowledge cycle while the processor is fetching the vector, if $\overline{VPA}$ is asserted, the R68000 will assert $\overline{VMA}$ and complete a normal R6500 read cycle as shown in Figure 38. The processor will then use an internally generated vector, called an autovector, that is a function of the interrupt being served. The seven autovectors are vector numbers 25 through 31 (decimal).

Autovectors operate in the same fashion as (but are not restricted to) the R6500 interrupt sequence. The basic difference is that there are six normal interrupt vectors and one NMI type vector. As with both the R6500 and the R68000's normal vectored interrupt, the interrupt service routine can be located anywhere in the address space. This is due to the fact that while the vector numbers are fixed, the contents of the vector table entries are assigned by the user.

Since $\overline{VMA}$ is asserted during autovectoring, the R6500 peripheral address decoding should prevent unintended accesses.

DATA TYPES AND ADDRESSING MODES

Five basic data types are supported. These data types are:

Bits
BCD Digits (4-bits)
Bytes (8-bits)
Word (16-bits)
Long Words (32-bits)

In addition, operations on other data types such as memory addresses, status word data, etc., are provided for in the instruction set.

The 14 addressing modes, shown in Table 9, include six basic types:

Register Direct
Register Indirect
Absolute
Program Counter Relative
Implied
Immediate

Included in the register indirect addressing modes is the capability to do postincrementing, predecrementing, offsetting and indexing. Program counter relative mode can also be modified via indexing and offsetting.

Table 9. Addressing Modes

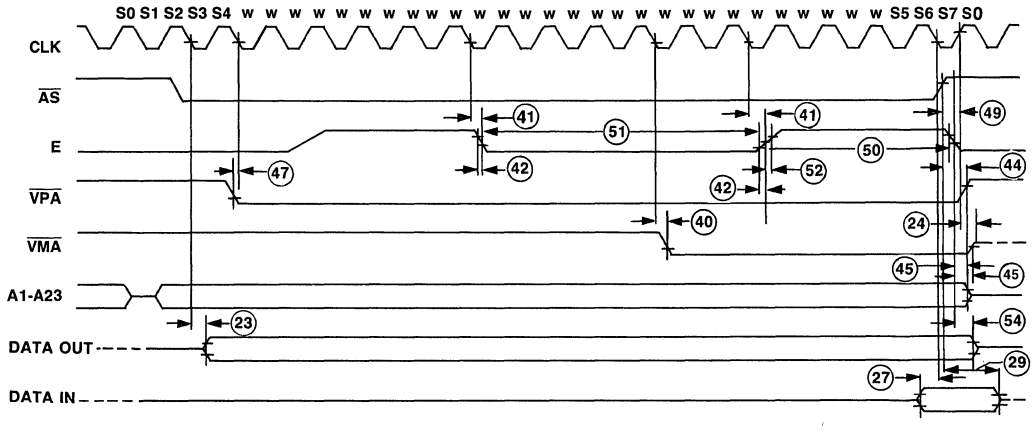
Mode	Generation
Register Direct Addressing	
Data Register Direct	EA = Dn
Address Register Direct	EA = An
Absolute Data Addressing	
Absolute Short	EA = (Next Word)
Absolute Long	EA = (Next Two Words)
Program Counter Relative Addressing	
Relative with Offset	EA = (PC) + d_{16}
Relative with Index and Offset	EA = (PC) + (Xn) + d_8
Register Indirect Addressing	
Register Indirect	EA = (An)
Postincrement Register Indirect	EA = (An), An ← An + N
Predecrement Register Indirect	An ← An − N, EA = (An)
Register Indirect with Offset	EA = (An) + d_{16}
Indexed Register Indirect with Offset	EA = (An) + (Xn) + d_8
Immediate Data Addressing	
Immediate	DATA = Next Word(s)
Quick Immediate	Inherent Data
Implied Addressing	
Implied Register	EA = SR, USP, SP, PC

NOTES:

EA = Effective Address
An = Address Register
Dn = Data Register
Xn = Address or Data Register used as Index Register
SR = Status Register
PC = Program Counter
( ) = Contents of
d_8 = Eight-bit Offset (displacement)
d_{16} = Sixteen-bit Offset (displacement)
N = 1 for Byte, 2 for Words and 4 for Long Word. If An is the stack pointer and the operand size is byte, N = 2 to keep the stack pointer on a word boundry.
← = Replaces

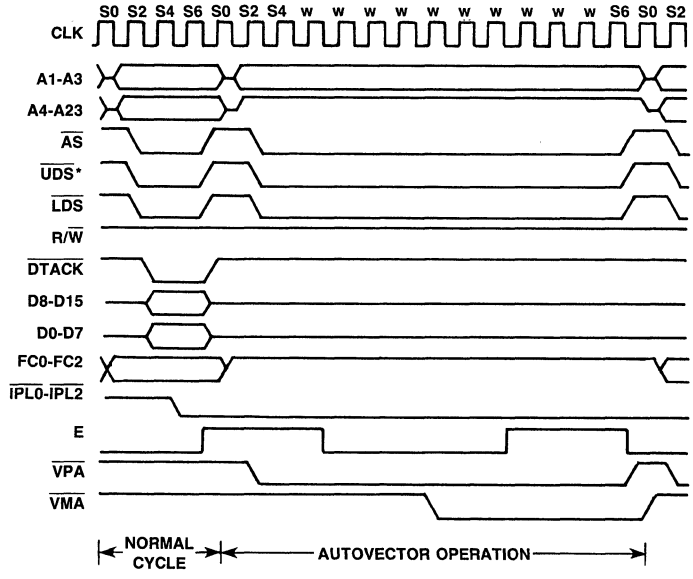
INSTRUCTION SET OVERVIEW

The R68000 instruction set is shown in Table 10. Some additional instructions are variations, or subsets, of these and they appear in Table 11. Special emphasis has been given to the instruction set's support of structured high-level languages to facilitate ease of programming. Each instruction, with few exceptions, operates on bytes, words, and long words and most instructions can use any of the 14 addressing modes. Combining instruction types, data types, and addressing modes, over 1000 useful instructions are provided. These instructions include signed and unsigned multiply and divide, "quick" arithmetic operations. BCD arithmetic and expanded operations (through traps).



NOTE: THIS TIMING DIAGRAM IS INCLUDED FOR THOSE WHO WISH TO DESIGN THEIR OWN CIRCUIT TO GENERATE VMA. IT SHOWS THE WORST CASE POSSIBLY ATTAINABLE.

Figure 37. RC68000 to R6500 Peripheral Timing Diagram — Worst Case



*ALTHOUGH A VECTOR NUMBER IS ONE BYTE, BOTH DATA STROBES ARE ASSERTED DUE TO THE MICROCODE USED FOR EXCEPTION PROCESSING. THE PROCESSOR DOES NOT RECOGNIZE ANYTHING ON DATA LINES D8 THROUGH D15 AT THIS TIME.

Figure 38. Autovector Operation Timing Diagram

Table 10. Instruction Set Summary

Mnemonic	Description
ADBC	Add Decimal with Extend
ADD	Add
AND	Logical And
ASL	Arithmetic Shift Left
ASR	Arithmetic Shift Right
B_{CC}	Branch Conditionally
BCHG	Bit Test and Change
BCLR	Bit Test and Clear
BRA	Branch Always
BSET	Bit Test and Set
BSR	Branch to Subroutine
BTST	Bit Test
CHK	Check Register Against Bounds
CLR	Clear Operand
CMP	Compare
DB_{CC}	Test Condition, Decrement and Branch
DIVS	Signed Divide
DIVU	Unsigned Divide
EOR	Exclusive Or
EXG	Exchange Registers
EXT	Sign Extend
JMP	Jump
JSR	Jump to Subroutine
LEA	Load Effective Address
LINK	Link Stack
LSL	Logical Shift Left
LSR	Logical Shift Right
MOVE	Move
MULS	Signed Multiply
MULU	Unsigned Multiply
NBCD	Negate Decimal with Extend
NEG	Negate
NOP	No Operation
NOT	One's Complement
OR	Logical Or
PEA	Push Effective Address
RESET	Reset External Devices
ROL	Rotate Left without Extend
ROR	Rotate Right without Extend
ROXL	Rotate Left with Extend
ROXR	Rotate Right with Extend
RTE	Return from Exception
RTR	Return and Restore
RTS	Return from Subroutine
SBCD	Subtract Decimal with Extend
S_{CC}	Set Conditional
STOP	Stop
SUB	Subtract
SWAP	Swap Data Register Halves
TAS	Test and Set Operand
TRAP	Trap
TRAPV	Trap on Overflow
TST	Test
UNLK	Unlink

4

Table 11. Variations of Instruction Types

Instruction Type	Variation	Description
ADD	**ADD**	Add
	ADDA	Add Address
	ADDQ	Add Quick
	ADDI	Add Immediate
	ADDX	Add with Extend
AND	**AND**	Logical And
	ANDI	And Immediate
	ANDI to CCR	And Immediate to Condition Codes
	ANDI to SR	And Immediate to Status Register
CMP	**CMP**	Compare
	CMPA	Compare Address
	CMPM	Compare Memory
	CMPI	Compare Immediate
EOR	**EOR**	Exclusive Or
	EORI	Exclusive Or Immediate
	EORI to CCR	Exclusive Or Immediate to Condition Codes
	EORI to SR	Exclusive Or Immediate to Status Register
MOVE	**MOVE**	Move
	MOVEA	Move Address
	MOVEM	Move Multiple Registers
	MOVEP	Move Peripheral Data
	MOVEQ	Move Quick
	MOVE from SR	Move from Status Register
	MOVE to SR	Move to Status Register
	MOVE to CCR	Move to Condition Codes
	MOVE USP	Move User Stack Pointer
NEG	**NEG**	Negate
	NEGX	Negate with Extend
OR	**OR**	Logical Or
	ORI	Or Immediate
	ORI to CCR	Or Immediate to Condition Codes
	ORI to SR	Or Immediate to Status Register
SUB	**SUB**	Subtract
	SUBA	Subtract Address
	SUBI	Subtract Immediate
	SUBQ	Subtract Quick
	SUBX	Subtract with Extend

The following paragraphs contain an overview of the form and structure of the R68000 instruction set. The instructions form a set of tools that include all the machine functions to perform the following operations:

Data Movement
Integer Arithmetic
Logical
Shift and Rotate
Bit Manipulation
Binary Coded Decimal
Program Control
System Control

The complete range of instruction capabilities combined with the flexible addressing modes described previously provide a very flexible base for program development.

ADDRESSING

Instructions for the R68000 contain two kinds of information: the type of function to be performed, and the location of the operand(s) on which to perform that function. The methods used to locate (address) the operand(s) are explained in the following paragraphs.

Instructions specify an operand location in one of three ways:

Register Specification — the number of the register is given in the register field of the instruction.

Effective Address — use of the different effective address modes.

Implicit Reference — the definition of certain instructions implies the use of specific registers.

DATA MOVEMENT OPERATIONS

The move (MOVE) instruction provides a means for data acquisition (transfer and storage). The move instruction and the effective addressing modes allow both address and data manipulation. Data move instructions allow byte, word, and long word operands to be transferred from memory to memory, memory to register, register to memory, and register to register. Address move instructions allow word and long word operand transfers and ensure that only legal address manipulations are executed. In addition to the general move instruction there are several special data movement instructions: move multiple registers (MOVEM), move peripheral data (MOVEP), exchange registers (EXG), load effective address (LEA), push effective address (PEA), link stack (LINK), unlink stack (UNLK), and move quick (MOVEQ). Table 12 summarizes the data movement operations.

Table 12. Data Movement Operations

Instruction	Operand Size	Operation
EXG	32	Rx↔Ry
LEA	32	EA→ An
LINK	—	An →– (SP) SP →An SP + displacement →SP
MOVE	8, 16, 32	s →d
MOVEM	16, 32	(EA) →An, Dn An, Dn →EA
MOVEP	16, 32	(EA) →Dn Dn →(EA)
MOVEQ	8	#xxx →Dn
PEA	32	EA →– (SP)
SWAP	32	Dn[31:16]↔Dn[15:0]
UNLK	—	An →Sp (SP) + →An

NOTES:
s = source, d = destination, [ ] = bit number, –( ) = indirect with predecrement, ( )+ = indirect with postdecrement, # = immediate data

INTEGER ARITHMETIC OPERATIONS

The arithmetic operators include the four basic operations of add (ADD), subtract (SUB), multiply (MUL), and divide (DIV) as well as arithmetic compare (CMP), clear (CLR), and negate (NEG). The add and subtract instructions are available for both address and data operations, and with data operations accepting all operand sizes. Address operations are limited to legal address size operands (16 or 32 bits). Data, address, and memory compare operations are also available. The clear and negate instructions may be used on all sizes of data operands.

The multiply and divide operations are available for signed and unsigned operands using word multiply to produce a long word product, and a long word dividend with word divisor to produce a word quotient with a word remainder.

Multiprecision and mixed size arithmetic can be accomplished using a set of extended instructions. These instructions are: add extended (ADDX), subtract extended (SUBX), sign extend (EXT), and negate binary with extend (NEGX).

A text operand (TST) instruction that sets the condition codes as a result of a compare of the operand with zero is available. Test and set (TAS) is a synchronization instruction useful in multiprocessor systems. Table 13 summrizes the integer arithmetic operations.

INSTRUCTION FORMAT

Instructions, as shown in Figure 39, vary from one to five words in length. The first word of the instruction, called the operation word, specifies the length of the instruction and the operation to be performed. The remaining words further specify the operands. These words are either immediate operands or extensions to the effective address mode specified in the operation word.

Table 13. Integer Arithmetic Operations

Instruction	Operand Size	Operation
ADD	8, 16, 32	Dn + (EA) → Dn
		(EA) + Dn → (EA)
		(EA) + #xxx → (EA)
	16, 32	An + (EA) → An
ADDX	8, 16, 32	Dx + Dy + X → Dx
	16, 32	−(Ax) + −(Ay) + X → (Ax)
CLR	8, 16, 32	0 → EA
CMP	8, 16, 32	Dn − (EA)
		(EA) − #xxx
		(Ax)+ − (Ay)+
	16, 32	An − (EA)
DIVS	32 ÷ 16	Dn ÷ (EA) → Dn
DIVU	32 ÷ 16	Dn ÷ (EA) → Dn
EXT	8 → 16	$(Dn)_8 \rightarrow Dn_{16}$
	16 → 32	$(Dn)_{16} \rightarrow Dn_{32}$
MULS	16 × 16 → 32	Dn × (EA) → Dn
MULU	16 × 16 → 32	Dn × (EA) → Dn
NEG	8, 16, 32	0 − (EA) → (EA)
NEGX	8, 16, 32	0 − (EA) − X → (EA)
SUB	8, 16, 32	Dn − (EA) → Dn
		(EA) − Dn → (EA)
		(EA) − #xxx → (EA)
	16, 32	An − (EA) → An
SUBX	8, 16, 32	Dx − Dy − X → Dx
		−(Ax) − −(Ay) − X → (Ax)
TAS	8	[EA] − 0, 1 → EA[7]
TST	8, 16, 32	(EA) − 0

NOTES:
[ ] = bit number
−( ) = indirect with predecrement
( )+ = indirect with postdecrement
= immediate data

PROGRAM/DATA REFERENCES

The R68000 separates memory references into two classes: program references, and data references. Program references reference that section of memory that contains the program being executed. Data references refer to that section of memory that contains data. Operand reads are from the data space, except in the case of the program counter relative addressing mode. All operand writes are to the data space.

REGISTER SPECIFICATION

The register field within an instruction specifies the register to be used. Other fields within the instruction specify whether the register selected is an address or data register and how the register is to be used.

EFFECTIVE ADDRESS

Most instructions specify the location of an operand by using the effective address field in the operation word. For example, Figure 40 shows the general format of the single effective address instruction operation word. The effective address is composed of two 3-bit fields: the mode field, and the register field. The value in the mode field selects the different address modes. The register field contains the number of a register.

The effective address field may require additional information to fully specify the operand. This additional information, called the effective address extension, is contained in the following word or words and is considered part of the instruction, as shown in Figure 39. The effective address modes are grouped into three categories: register direct, memory addressing, and special.

REGISTER DIRECT MODES. These effective addressing modes specify that the operand is in one of the 16 multifunction registers.

Data Register Direct. The operand is in the data register specified by the effective address register field.

Address Register Direct. The operand is in the address register specified by the effective address register field.

MEMORY ADDRESS MODES. These effective addressing modes specify that the operand is in memory and provide the specific address of that operand.

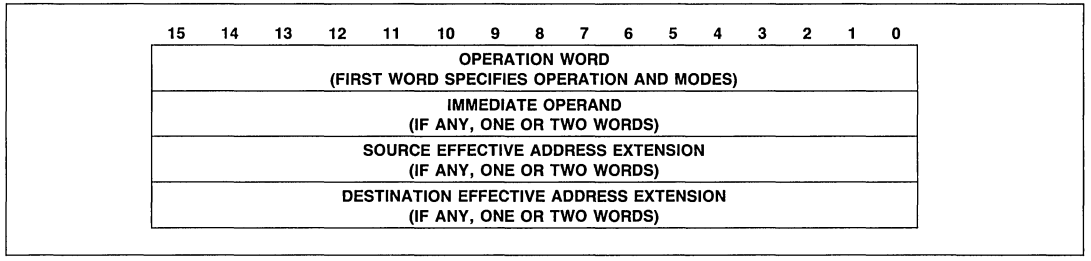


Figure 39. Instruction Format

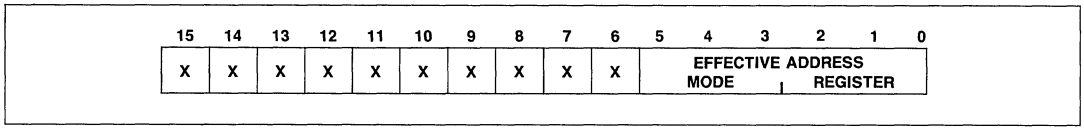


Figure 40. Single-Effective-Address Instruction Operation Word General Format

Address Register Indirect. The address of the operand is in the address register specified by the register field. The reference is classified as a data reference with the exception of the jump and jump to subroutine instructions.

Address Register Indirect With Postincrement. The address of the operand is in the address register specified by the register field. After the operand address is used, it is incremented by one, two or four depending upon whether the size of the operand is byte, word, or long word. If the address register is the stack pointer and the operand size is byte, the address is incremented by two rather than one to keep the stack pointer on a word boundary. The reference classifies as a data reference.

Address Register Indirect With Predecrement. The address of the operand is in the address register specified by the register field. Before the operand address is used, it is decremented by one, two, or four depending upon whether the operand size is byte, word, or long word. If the address register is the stack pointer and the operand size is byte, the address is decremented by two rather than one to keep the stack pointer on a word boundary. The reference is classified as a data reference.

Address Register Indirect with Displacement. This address mode requires one word of extension. The address of the operand is the sum of the address in the address register and the sign-extended 16-bit displacement integer in the extension word. The reference classifies as a data reference with the exception of the jump to subroutine instructions.

Address Register Indirect With Index. This address mode requires one word of extension. The address of the operand sums the addresses in the address register, the sign-extended displacement integer in the low order eight bits of the extension word, and the contents of the index register. The reference is classified as a data reference with the exception of the jump and jump to subroutine instructions.

SPECIAL ADDRESS MODE. The special address modes use the effective address register field to specify the special addressing mode instead of a register number.

Absolute Short Address. This address mode requires one word of extension. The address of the operand is the extension word. The 16-bit address is sign extended before it is used. The reference classifies as a data reference with the exception of the jump and jump to subroutine instructions.

Absolute Long Address. This address mode requires two words of extension. The address of the operand is developed by the concatenation of the extension words. The high-order part of the address is the first extension word; the low-order part of the address is the second extension word. The reference classifies as a data reference with the exception of the jump and jump to subroutine instructions.

Program Counter With Displacement. This address mode requires one word of extension. The address of the operand sums the addresses in the program counter and the sign-extended 16-bit displacement integer in the extension word. The value in the program counter is the address of the extension word. The reference classifies as a program reference.

Program Counter With Index. This address mode requires one word of extension. This address sums the addresses in the program counter, the sign-extended displacement integer in the lower eight bits of the extension word, and the contents of the index register. The value in the program counter is the address of the extension word. This reference classifies as a program reference.

Immediate Data. This address mode requires either one or two words of extension depending on the size of the operation.

Byte Operation	— operand is low order byte of extension word
Word Operation	— operand is extension word
Long Word Operation	— operand is in the two extension words, high-order 16 bits are in the first extension word, low-order 16 bits are in the second extension word.

IMPLICIT REFERENCE

Some instructions make implicit reference to the program counter (PC), the system stack pointer (SP), the supervisor stack pointer (SSP), the user stack pointer (USP), or the status register (SR).

A selected set of instructions may reference the status register by means of the effective address field. These are:

ANDI to CCR
ANDI to SR
EORI to CCR
EORI to SR
MOVE to CCR
MOVE to SR
MOVE from SR
ORI to CCR
ORI to SR

EFFECTIVE ADDRESS ENCODING SUMMARY

Table 14 summarizes the effective addressing modes discussed in the previous paragraphs.

Table 14. Effective Address Encoding Summary

Addressing Mode	Mode	Register
Data Register Direct	000	register number
Address Register Direct	001	register number
Address Register Indirect	010	register number
Address Register Indirect with Postincrement	011	register number
Address Register Indirect with Predecrement	100	register number
Address Register Indirect with Displacement	101	register number
Address Register Indirect with Index	110	register number
Absolute Short	111	000
Absolute Long	111	001
Program Counter with Displacement	111	010
Program Counter with Index	111	011
Immediate	111	100

SYSTEM STACK. The system stack is used implicitly by many instructions; user stacks and queues may be created and maintained through the addressing modes. Address register seven (A7) is the system stack pointer (SP). The system stack pointer is either the supervisor stack pointer (SSP) or the user stack pointer (USP), depending on the state of the S-bit in the status register. If the S-bit indicates supervisor state (High), SSP is the active system stack pointer, and the USP cannot be referenced as an address register. If the S-bit indicates user state (Low), the USP is the active system stack pointer, and the SSP cannot be referenced. Each system stack fills from high memory to low memory.

LOGICAL OPERATIONS

Logical operation instructions AND, OR, EOR, and NOT are available for all sizes of integer data operands. A similar set of immediate instructions (ANDI, ORI, and EORI) provide these logical operations with all sizes of immediate data. Table 15 summarizes the logical operations.

SHIFT AND ROTATE OPERATIONS

Shift operations in both directions are provided by arithmetic instructions ASR and ASL and logical shift instructions LSR and LSL. The rotate instructions (with and without extend) available are ROXR, ROXL, ROR, and ROL. All shift and rotate operations can be performed in either registers or memory. Register shifts and rotates support all operand sizes and allow a shift count specified in a data register.

Table 15. Logical Operations

Instruction	Operand Size	Operation
AND	8, 16, 32	DnΛ(EA) →Dn (EA)ΛDn →(EA) (EA)Λ#xxx →(EA)
OR	8, 16, 32	Dn ν (EA) →Dn (EA) ν Dn →(EA) (EA) ν #xxx →(EA)
EOR	8, 16, 32	(EA) ⊕ Dy →(EA) (EA) ⊕ #xxx →(EA)
NOT	8, 16, 32	~ (EA) →(EA)

NOTES:
~ = invert
# = immediate data
Λ = logical AND
ν = logical OR
⊕ = logical exclusive OR

Memory shifts and rotates are for word operands only and allow only single-bit shifts or rotates.

Table 16 summarizes the shift and rotate operations.

BIT MANIPULATION OPERATIONS

The following instructions provide bit manipulation operations: bit test (BTST), bit test and set (BSET), bit test and clear (BCLR), and bit test and change (BCHG). Table 17 is a summary of the bit manipulation operations. (Bit 2 of the status register is Z.)

Table 16. Shift and Rotate Operations

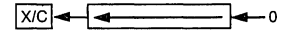
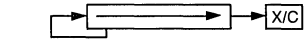
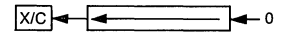
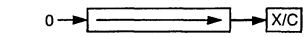
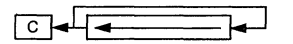
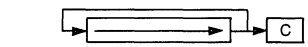
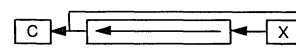
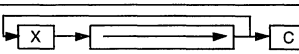
Instruction	Operand Size	Operation
ASL	8, 16, 32	
ASR	8, 16, 32	
LSL	8, 16, 32	
LSR	8, 16, 32	
ROL	8, 16, 32	
ROR	8, 16, 32	
ROXL	8, 16, 32	
ROXR	8, 16, 32	

Table 17. Bit Manipulation Operations

Instruction	Operand Size	Operation
BTST	8, 32	~ bit of (EA) →Z
BSET	8, 32	~ bit of (EA) →Z 1 →bit of EA
BCLR	8, 32	~ bit of (EA) →Z 0 →bit of EA
BCHG	8, 32	~ bit of (EA) →Z ~ bit of (EA) →bit of EA
NOTE: ~ = invert		

BINARY CODED DECIMAL OPERATIONS

The following instructions accomplish multiprecision arithmetic operations on binary coded decimal numbers: add decimal with extend (ABCD), subtract decimal with extend (SBCD), and negate decimal with extend (NBCD). Table 18 summarizes the binary coded decimal operations.

PROGRAM CONTROL OPERATIONS

Program control operations implementation requires a series of conditional and unconditional branch instructions and return instructions. These instructions are summarized in Table 19.

The conditional instructions provide setting and branching for the following conditions:

CC — carry clear
CS — carry set
EQ — equal
F — never true
GE — greater or equal
GT — greater than
HI — high
LE — less or equal
LS — low or same
LT — less than
MI — minus
NE — not equal
PL — plus
T — always true
VC — no overflow
VS — overflow

Table 18. Binary Coded Decimal Operations

Instruction	Operand Size	Operation
ABCD	8	$Dx_{10} + Dy_{10} + X \rightarrow Dx$ $-(Ax)_{10} + -(Ay)_{10} + x \rightarrow (Ax)$
SBCD	8	$Dx_{10} - Dy_{10} - X \rightarrow Dx$ $-(Ax)_{10} - -(Ay)_{10} - X \rightarrow (Ax)$
NBCD	8	$0 - (EA)_{10} - X \rightarrow (EA)$
NOTE: −( ) = indirect with predecrement		

Table 19. Program Control Operations

Instruction	Operation
Conditional	
B_{CC}	Branch conditionally (14 conditions) 8- and 16-bit displacement
DB_{CC}	Test condition, decrement, branch 16-bit displacement
S_{CC}	Set byte conditionally (16 conditions)
Unconditional	
BRA	Branch always 8- and 16-bit displacement
BSR	Branch to subroutine 8- and 16-bit displacement
JMP	Jump
JSR	Jump to subroutine
Returns	
RTR	Return and restore condition codes
RTS	Return from subroutine

SYSTEM CONTROL OPERATIONS

System control operations are accomplished by using privileged instructions, trap generating instructions, and instructions that use or modify the status register. These instructions are summarized in Table 20.

INSTRUCTION SET

The following paragraphs provide information about the addressing categories and instruction set of the R68000.

ADDRESSING CATEGORIES

Effective address modes may be categorized by the ways in which they may be used. The following classifications will be used in the instructions definitions.

Data — If an effective address mode may be used to refer to data operands, it is considered a data addressing effective address mode.

Memory — If an effective address mode may be used to refer to memory operands, it is considered a memory addressing effective address mode.

Alterable — If an effective address mode may be used to refer to alterable (writeable) operands, it is considered an alterable addressing effective address mode.

Control — If an effective address mode may be used to refer to memory operands without an associated size, it is considered control addressing effective address mode.

Table 21 shows the various categories to which each of the effective address modes belong. Table 22 is the instruction set summary.

Table 20. System Control Operations

Instruction	Operation
Privileged	
ANDI to SR	Logical AND to Status Register
EORI to SR	Logical EOR to Status Register
MOVE EA to SR	Load New Status Register
MOVE USP	Move User Stack Pointer
ORI to SR	Logical OR to Status Register
RESET	Reset External Devices
RTE	Return from Exception
STOP	Stop Program Execution
Trap Generating	
CHK	Check Data Register Against Upper Bounds
TRAP	Trap
TRAPV	Trap on Overflow
Status Register	
ANDI to CCR	Logical AND to Condition Codes
EORI to CCR	Logical EOR to Condition Codes
MOVE EA to CCR	Load New Condition Codes
MOVE SR to EA	Store Status Register
ORI to CCR	Logical OR to Condition Codes

The status register addressing mode is not permitted unless it is explicitly mentioned as a legal addressing mode.

These categories may be combined, so that additional, more restrictive, classifications may be defined. For example, the instruction descriptions use such classifications as alterable memory or data alterable. The former refers to those addressing modes which are both alterable and memory addresses, and the latter refers to addressing modes which are both data and alterable.

INSTRUCTION PREFETCH

The R68000 uses a two-word tightly-coupled instruction prefetch mechanism to enhance performance. This mechanism is described in terms of the microcode operations involved. If the execution of an instruction is defined to begin when the microroutine for that instruction is entered, some features of the prefetch mechanism can be described.

1) When execution of an instruction begins, the operation word and the word following have already been fetched. The operation word is in the instruction decoder.
2) In the case of multi-word instructions, as each additional word of the instruction is used internally, a fetch is made to the instruction stream to replace it.
3) The last fetch from the instruction stream is made when the operation word is discarded and decoding is started on the next instruction.
4) If the instruction is a single-word instruction causing a branch, the second word is not used. But because this word is fetched by the preceding instruction, it is impossible to avoid this superfluous fetch.
5) In the case of an interrupt or trace exception, both words are not used.
6) The program counter usually points to the last word fetched from the instruction stream.

INSTRUCTION EXECUTION TIMES

The following paragraphs contain listings of the instruction execution times in terms of external clock (CLK) periods. In this timing data, it is assumed that both memory read and write cycle times are four clock periods. Any wait states caused by a longer memory cycle must be added to the total instruction time. The number of bus read and write cycles for each instruction is enclosed in parenthesis following the execution periods and is shown as (r/w) where r is the number of read cycles and w is the number of write cycles.

Table 21. Effective Addressing Mode Categories

Effective Address Modes	Mode	Register	Addressing Categories			
			Data	Memory	Control	Alterable
Dn	000	Register Number	X	—	—	X
An	001	Register Number	—	—	—	X
(An)	010	Register Number	X	X	X	X
(An)+	011	Register Number	X	X	—	X
–(An)	100	Register Number	X	X	—	X
d(An)	101	Register Number	X	X	X	X
d(An, ix)	110	Register Number	X	X	X	X
xxx.W	111	000	X	X	X	X
xxx.L	111	001	X	X	X	X
d(PC)	111	010	X	X	X	—
d(PC, ix)	111	011	X	X	X	—
#xxx	111	X	X	X	—	—

Table 22. Instruction Set

Mnemonic	Description	Operation	Condition Codes				
			X	N	Z	V	C
ABCD	Add Decimal with Extend	$(Destination)_{10} + (Source)_{10} + X \rightarrow$ Destination	*	U	*	U	*
ADD	Add Binary	(Destination) + (Source) → Destination	*	*	*	*	*
ADDA	Add Address	(Destination) + (Source) → Destination	—	—	—	—	—
ADDI	Add Immediate	(Destination) + Immediate Data → Destination	*	*	*	*	*
ADDQ	Add Quick	(Destination) + Immediate Data → Destination	*	*	*	*	*
ADDX	Add Extended	(Destination) + (Source) + X → Destination	*	*	*	*	*
AND	AND Logical	(Destination) Λ (Source) → Destination	—	*	*	0	0
ANDI	AND Immediate	(Destination) Λ Immediate Data → Destination	—	*	*	0	0
ANDI to CCR	AND Immediate to Condition Codes	(Source) Λ CCR → CCR	*	*	*	*	*
ANDI to SR	AND Immediate to Status Register	(Source) Λ SR → SR	*	*	*	*	*
ASL, ASR	Arithmetic Shift	(Destination) Shifted by <count> → Destination	*	*	*	*	*
B_{CC}	Branch Conditionally	If CC then PC + d → PC	—	—	—	—	—
BCHG	Test a Bit and Change	~ (<bit number>) OF Destination → Z ~ (<bit number>) OF Destination → <bit number> OF Destination	—	—	*	—	—
BCLR	Test a Bit and Clear	~ (<bit number>) OF Destination → Z 0 → <bit number> → OF Destination	—	—	*	—	—
BRA	Branch Always	PC + d → PC	—	—	—	—	—
BSET	Test a Bit and Set	~ (<bit number>) OF Destination → Z 1 → <bit number> OF Destination	—	—	*	—	—
BSR	Branch to Subroutine	PC → (SP); PC + d → PC	—	—	—	—	—
BTST	Test a Bit	~ (<bit number>) OF Destination → Z	—	—	*	—	—
CHK	Check Register Against Bounds	If Dn <0 or Dn> (<ea>) then TRAP	—	*	U	U	U
CLR	Clear and Operand	0 → Destination	—	0	1	0	0
CMP	Compare	(Destination) – (Source)	—	*	*	*	*
CMPA	Compare Address	(Destination) – (Source)	—	*	*	*	*
CMPI	Compare Immediate	(Destination) – Immediate Data	—	*	*	*	*
CMPM	Compare Memory	(Destination) – (Source)	—	*	*	*	*
DB_{CC}	Test Condition, Decrement and Branch	If ~ CC then Dn – 1 → Dn; if Dn ≠ – 1 then PC + d → PC	—	—	—	—	—
DIVS	Signed Divide	(Destination)/(Source) → Destination	—	*	*	*	0
DIVU	Unsigned Divide	(Destination)/(Source) → Destination	—	*	*	*	0
EOR	Exclusive OR Logical	(Destination) ⊕ (Source) → Destination	—	*	*	0	0
EORI	Exclusive OR Immediate	(Destination) ⊕ Immediate Data → Destination	—	*	*	0	0
EORI to CCR	Exclusive OR Immediate to Condition Codes	(Source) ⊕ CCR → CCR	*	*	*	*	*

NOTES:

Λ = logical AND
ν = logical OR
⊕ = logical exclusive OR
~ = logical complement

* = affected
— = unaffected
0 = cleared
1 = set
U = undefined

Table 22. Instruction Set (Continued)

Mnemonic	Description	Operation	Condition Codes				
			X	N	Z	V	C
EORI to SR	Exclusive OR Immediate to Status Register	(Source) ⊕ SR → SR	*	*	*	*	*
EXG	Exchange Register	Rx ↔ Ry	—	—	—	—	—
EXT	Sign Extend	(Destination) Sign-Extended → Destination	—	*	*	0	0
JMP	Jump	Destination → PC	—	—	—	—	—
JSR	Jump to Subroutine	PC → – (SP); Destination → PC	—	—	—	—	—
LEA	Load Effective Address	<ea> → An	—	—	—	—	—
LINK	Link and Allocate	An → (SP); SP → An; SP + Displacement → SP	—	—	—	—	—
LSL, LSR	Logical Shift	(Destination) Shifted by <count> → Destination	*	*	*	0	*
MOVE	Move Data from Source to Destination	(Source) → Destination	—	*	*	0	0
MOVE to CCR	Move to Condition Code	(Source) → CCR	*	*	*	*	*
MOVE to SR	Move to the Status Register	(Source) → SR	*	*	*	*	*
MOVE from SR	Move from the Status Register	SR → Destination	—	—	—	—	—
MOVE USP	Move User Stack Pointer	USP → An; An → USP	—	—	—	—	—
MOVEA	Move Address	(Source) → Destination	—	—	—	—	—
MOVEM	Move Multiple Registers	Register → Destination (Source) → Registers	—	—	—	—	—
MOVEP	Move Peripheral Data	(Source) → Destination	—	—	—	—	—
MOVEQ	Move Quick	Immediate Data → Destination	—	*	*	0	0
MULS	Signed Multiply	(Destination)X(Source) → Destination	—	*	*	0	0
MULU	Unsigned Multiply	(Destination)X(Source) → Destination	—	*	*	0	0
NBCD	Negate Decimal with Extend	0 – (Destination)$_{10}$ – X → Destination	*	U	*	U	*
NEG	Negate	0 – (Destination) → Destination	*	*	*	*	*
NEGX	Negate with Extend	0 – (Destination) – X → Destination	*	*	*	*	*
NOP	No Operation	—	—	—	—	—	—
NOT	Logical Complement	~ (Destination) → Destination	—	*	*	0	0
OR	Inclusive OR Logical	(Destination) ∨ (Source) → Destination	—	*	*	0	0
ORI	Inclusive OR Immediate	(Destination) ∨ Immediate Data → Destination	—	*	*	0	0
ORI to CCR	Inclusive OR Immediate to Condition Codes	(Source) ∨ CCR → CCR	*	*	*	*	*
ORI to SR	Inclusive OR Immediate to Status Register	(Source) ∨ SR → SR	*	*	*	*	*
PEA	Push Effective Address	<ea> → – (SP)	—	—	—	—	—
RESET	Reset External Device	—	—	—	—	—	—
ROL, ROR	Rotate (Without Extend)	(Destination) Rotated by <count> → Destination	—	*	*	0	*

NOTES:

Λ = logical AND
∨ = logical OR
⊕ = logical exclusive OR
~ = logical complement

* = affected
— = unaffected
0 = cleared
1 = set
U = undefined

4

Table 22. Instruction Set (Continued)

Mnemonic	Description	Operation	Condition Codes				
			X	N	Z	V	C
ROXL, ROXR	Rotate with Extend	(Destination) Rotated by <count> →Destination	*	*	*	0	*
RTE	Return from Exception	(SP) + →SR; (SP) + →PC	*	*	*	*	*
RTR	Return and Restore Condition Codes	(SP) + →CC; (SP) + →PC	*	*	*	*	*
RTS	Return from Subroutine	(SP) + →PC	—	—	—	—	—
SBCD	Subtract Decimal with Extend	$(Destination)_{10}$ − $(Source)_{10}$ − X →Destination	*	U	*	U	*
S_{CC}	Set According to Condition	If CC then 1's →Destination else 0's →Destination	—	—	—	—	—
STOP	Load Status Register and Stop	Immediate Data →SR; STOP	*	*	*	*	*
SUB	Subtract Binary	(Destination) − (Source) →Destination	*	*	*	*	*
SUBA	Subtract Address	(Destination) − (Source) →Destination	—	—	—	—	—
SUBI	Subtract Immediate	(Destination) − Immediate Data →Destination	*	*	*	*	*
SUBQ	Subtract Quick	(Destination) − Immediate Data →Destination	*	*	*	*	*
SUBX	Subtract with Extend	(Destination) − (Source) − X →Destination	*	*	*	*	*
SWAP	Swap Register Halves	Register [31:16]↔Register [15:0]	—	*	*	0	0
TAS	Test and Set an Operand	(Destination) Tested →CC; 1 →[7] OF Destination	—	*	*	0	0
TRAP	Trap	PC →− (SSP); SR →− (SSP); (Vector) →PC	—	—	—	—	—
TRAPV	Trap on Overflow	If ν then TRAP	—	—	—	—	—
TST	Test and Operand	(Destination) Tested →CC	—	*	*	0	0
UNLK	Unlink	An →SP; (SP) + →An	—	—	—	—	—

NOTES:

[ ]	= bit number	*	= affected
Λ	= logical AND	—	= unaffected
ν	= logical OR	0	= cleared
$\oplus$	= logical exclusive OR	1	= set
~	= logical complement	U	= undefined

Note

The number of periods includes instruction fetch and all applicable operand fetches and stores.

EFFECTIVE ADDRESS OPERAND CALCULATION TIMING

Table 23 lists the number of clock periods required to compute an instruction's effective address. It includes fetching of any extension words, the address computation, and fetching of the memory operand. The number of bus read and write cycles is shown in parenthesis as (r/w). Note there are no write cycles involved in processing the effective address.

MOVE INSTRUCTION CLOCK PERIODS

Tables 24 and 25 indicate the number of clock periods for the move instruction. This data includes instruction fetch, operand reads, and operand writes. The number of bus read and write cycles is shown in parenthesis as (r/w).

STANDARD INSTRUCTION CLOCK PERIODS

The number of clock periods shown in Table 26 delineate the time required to perform the operations, store the results, and read the next instruction. The number of bus read and write cycles is shown in parenthesis as (r/w). The number of clock periods and the number of read and write cycles must be added respectively to those of the effective address calculation where indicated.

In Table 26, the headings have the following meanings: An = address register operand, Dn = data register operand, ea = an operand specified by an effective address, and M = memory effective address operand.

IMMEDIATE INSTRUCTION CLOCK PERIODS

The number of clock periods shown in Table 27 includes the time to fetch immediate operands, perform the operations, store the results, and read the next operation. The number of bus read and write cycles is shown in parenthesis as (r/w). The number

Table 23. Effective Address Calculation Timing

Addressing Mode		Byte, Word	Long
	Register		
Dn	Data Register Direct	**0**(0/0)	**0**(0/0)
An	Address Register Direct	**0**(0/0)	**0**(0/0)
	Memory		
(An)	Address Register Indirect	**4**(1/0)	**8**(2/0)
(An)+	Address Register Indirect with Postincrement	**4**(1/0)	**8**(2/0)
−(An)	Address Register Indirect with Predecrement	**6**(1/0)	**10**(2/0)
d(An)	Address Register Indirect with Displacement	**8**(2/0)	**12**(3/0)
d(An, ix)*	Address Register Indirect with Index	**10**(2/0)	**14**(3/0)
xxx.W	Absolute Short	**8**(2/0)	**12**(3/0)
xxx.L	Absolute Long	**12**(3/0)	**16**(4/0)
d(PC)	Program Counter with Displacement	**8**(2/0)	**12**(3/0)
d(PC, ix)*	Program Counter with Index	**10**(2/0)	**14**(3/0)
#xxx	Immediate	**4**(1/0)	**8**(2/0)

*The size of the index register (ix) does not affect execution time.

Table 24. Move Byte and Word Instruction Clock Periods

Source	Destination								
	Dn	**An**	**(An)**	**(An)+**	**−(An)**	**d(An)**	**d(An, ix)***	**xxx.W**	**xxx.L**
Dn	**4**(1/0)	**4**(1/0)	**8**(1/1)	**8**(1/1)	**8**(1/1)	**12**(2/1)	**14**(2/1)	**12**(2/1)	**16**(3/1)
An	**4**(1/0)	**4**(1/0)	**8**(1/1)	**8**(1/1)	**8**(1/1)	**12**(2/1)	**14**(2/1)	**12**(2/1)	**16**(3/1)
(An)	**8**(2/0)	**8**(2/0)	**12**(2/1)	**12**(2/1)	**12**(2/1)	**16**(3/1)	**18**(3/1)	**16**(3/1)	**20**(4/1)
(An)+	**8**(2/0)	**8**(2/0)	**12**(2/1)	**12**(2/1)	**12**(2/1)	**16**(3/1)	**18**(3/1)	**16**(3/1)	**20**(4/1)
−(An)	**10**(2/0)	**10**(2/0)	**14**(2/1)	**14**(2/1)	**14**(2/1)	**18**(3/1)	**20**(3/1)	**18**(3/1)	**22**(4/1)
d(An)	**12**(3/0)	**12**(3/0)	**16**(3/1)	**16**(3/1)	**16**(3/1)	**20**(4/1)	**22**(4/1)	**20**(4/1)	**24**(5/1)
d(An, ix)*	**14**(3/0)	**14**(3/0)	**18**(3/1)	**18**(3/1)	**18**(3/1)	**22**(4/1)	**24**(4/1)	**22**(4/1)	**26**(5/1)
xxx.W	**12**(3/0)	**12**(3/0)	**16**(3/1)	**16**(3/1)	**16**(3/1)	**20**(4/1)	**22**(4/1)	**20**(4/1)	**24**(5/1)
xxx.L	**16**(4/0)	**16**(4/0)	**20**(4/1)	**20**(4/1)	**20**(4/1)	**24**(5/1)	**26**(5/1)	**24**(5/1)	**28**(6/1)
d(PC)	**12**(3/0)	**12**(3/0)	**16**(3/1)	**16**(3/1)	**16**(3/1)	**20**(4/1)	**22**(4/1)	**20**(4/1)	**24**(5/1)
d(PC, ix)*	**14**(3/0)	**14**(3/0)	**18**(3/1)	**18**(3/1)	**18**(3/1)	**22**(4/1)	**24**(4/1)	**22**(4/1)	**26**(5/1)
#xxx	**8**(2/0)	**8**(2/0)	**12**(2/1)	**12**(2/1)	**12**(2/1)	**16**(3/1)	**18**(3/1)	**16**(3/1)	**20**(4/1)

*The size of the index register (ix) does not affect execution time.

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of clock periods and the number of read and write cycles must be added respectively to those of the effective adress calculation where indicated.

In Table 27, the headings have the following meanings: # = immediate operand, Dn = data register operand, An = address register operand, M = memory operand, and SR = status register.

SINGLE OPERAND INSTRUCTION CLOCK PERIODS

Table 28 indicates the number of clock periods for the single operand instructions. The number of bus read and write cycles is shown in parenthesis as (r/w). The number of clock periods and the number of read and write cycles must be added respectively to those of the effective address calculation where indicated.

Table 25. Move Long Instruction Clock Periods

Source	Destination								
	Dn	An	(An)	(An)+	–(An)	d(An)	d(An, ix)*	xxx.W	xxx.L
Dn	4(1/0)	4(1/0)	12(1/2)	12(1/2)	12(1/2)	16(2/2)	18(2/2)	16(2/2)	20(3/2)
An	4(1/0)	4(1/0)	12(1/2)	12(1/2)	12(1/2)	16(2/2)	18(2/2)	16(2/2)	20(3/2)
(An)	12(3/0)	12(3/0)	20(3/2)	20(3/2)	20(3/2)	24(4/2)	26(4/2)	24(4/2)	28(5/2)
(An)+	12(3/0)	12(3/0)	20(3/2)	20(3/2)	20(3/2)	24(4/2)	26(4/2)	24(4/2)	28(5/2)
–(An)	14(3/0)	14(3/0)	22(3/2)	22(3/2)	22(3/2)	26(4/2)	28(4/2)	26(4/2)	30(5/2)
d(An)	16(4/0)	16(4/0)	24(4/2)	24(4/2)	24(4/2)	28(5/2)	30(5/2)	28(5/2)	32(6/2)
d(An, ix)*	18(4/0)	18(4/0)	26(4/2)	26(4/2)	26(4/2)	30(5/2)	32(5/2)	30(5/2)	34(6/2)
xxx.W	16(4/0)	16(4/0)	24(4/2)	24(4/2)	24(4/2)	28(5/2)	30(5/2)	28(5/2)	32(6/2)
xxx.L	20(5/0)	20(5/0)	28(5/2)	28(5/2)	28(5/2)	32(6/2)	34(6/2)	32(6/2)	36(7/2)
d(PC)	16(4/0)	16(4/0)	24(4/2)	24(4/2)	24(4/2)	28(5/2)	30(5/2)	28(5/2)	32(5/2)
d(PC, ix)*	18(4/0)	18(4/0)	26(4/2)	26(4/2)	26(4/2)	30(5/2)	32(5/2)	30(5/2)	34(6/2)
#xxx	12(3/0)	12(3/0)	20(3/2)	20(3/2)	20(3/2)	24(4/2)	26(4/2)	24(4/2)	28(5/2)

*The size of the index register (ix) does not affect execution time.

Table 26. Standard Instruction Clock Periods

Instruction	Size	op<ea>, An†	op<ea>, Dn	op Dn, <M>
ADD	Byte, Word	8(1/0)+	4(1/0)+	8(1/1)+
	Long	6(1/0)+**	6(1/0)+**	12(1/2)+
AND	Byte, Word	—	4(1/0)+	8(1/1)+
	Long	—	6(1/0)+**	12(1/2)+
CMP	Byte, Word	6(1/0)+	4(1/0)+	—
	Long	6(1/0)+	6(1/0)+	—
DIVS	—	—	158(1/0)+*	—
DIVU	—	—	140(1/0)+*	—
EOR	Byte, Word	—	4(1/0)***	8(1/1)+
	Long	—	8(1/0)***	12(1/2)+
MULS	—	—	70(1/0)+*	—
MULU	—	—	70(1/0)+*	—
OR	Byte, Word	—	4(1/0)+	8(1/1)+
	Long	—	6(1/0)+**	12(1/2)+
SUB	Byte, Word	8(1/0)+	4(1/0)+	8(1/1)+
	Long	6(1/0)+**	6(1/0)+**	12(1/2)+

NOTES:
+ add effective address calculation time
† word or long only
* indicates maximum value
** The base time of six clock periods is increased to eight if the effective address mode is register direct or immediate (effective address time should also be added).
*** Only available effective address mode is data register direct
DIVS, DIVU The divide algorithm used by the R68000 provides less than 10% difference between the best and worst case timings.
MULS, MULU The multiply algorithm requires 38 + 2n clocks where n is defined as:
MULU: n = the number of ones in each <ea>
MULU: n = concatanate the <ea> with a zero as the LSB; n is the resultant number of 10 or 01 patterns in the 17-bit source; i.e., worst case happens when the source is $5555.

Table 27. Immediate Instruction Clock Periods

Instruction	Size	op #, Dn	op #, An	op #, M
ADDI	Byte, Word	8(2/0)	—	12(2/1)+
	Long	16(3/0)	—	20(3/2)+
ADDQ	Byte, Word	4(1/0)	8(1/0)*	8(1/1)+
	Long	8(1/0)	8(1/0)	12(1/2)+
ANDI	Byte, Word	8(2/0)	—	12(2/1)+
	Long	16(3/0)	—	20(3/1)+
CMPI	Byte, Word	8(2/0)	—	8(2/0)+
	Long	14(3/0)	—	12(3/0)+
EORI	Byte, Word	8(2/0)	—	12(2/1)+
	Long	16(3/0)	—	20(3/2)+
MOVEQ	Long	4(1/0)	—	—
ORI	Byte, Word	8(2/0)	—	12(2/1)+
	Long	16(3/0)	—	20(3/2)+
SUBI	Byte, Word	8(2/0)	—	12(2/1)+
	Long	16(3/0)	—	20(3/2)+
SUBQ	Byte, Word	4(1/0)	8(1/0)*	8(1/1)+
	Long	8(1/0)	8(1/0)	12(1/2)+

+ add effective address calculation time
* word only

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Table 28. Single Operand Instruction Clock Periods

Instruction	Size	Register	Memory
CLR	Byte, Word	4(1/0)	8(1/1)+
	Long	6(1/0)	12(1/2)+
NBCD	Byte	6(1/0)	8(1/1)+
NEG	Byte, Word	4(1/0)	8(1/1)+
	Long	6(1/0)	12(1/2)+
NEGX	Byte, Word	4(1/0)	8(1/1)+
	Long	6(1/0)	12(1/2)+
NOT	Byte, Word	4(1/0)	8(1/1)+
	Long	6(1/0)	12(1/2)+
Scc	Byte, False	4(1/0)	8(1/1)+
	Byte, True	6(1/0)	8(1/1)+
TAS	Byte	4(1/0)	10(1/1)+
TST	Byte, Word	4(1/0)	4(1/0)+
	Long	4(1/0)	4(1/0)+

+ add effective address calculation time

SHIFT/ROTATE INSTRUCTION CLOCK PERIODS

Table 29 delineates the number of clock periods for the shift and rotate instructions. The number of bus read and write cycles is shown in parenthesis as: (r/w). The number of clock periods and the number of read and write cycles must be added respectively to those of the effective address calculation where indicated.

BIT MANIPULATION INSTRUCTION CLOCK PERIODS

Table 30 indicates the number of clock periods required for the bit manipulation instructions. The number of bus read and write cycles is shown in parenthesis as: (r/w). The number of clock periods and the number of read and write cycles must be added respectively to those of the effective address calculation where indicated.

CONDITIONAL INSTRUCTION CLOCK PERIODS

Table 31 delineates the number of clock periods required for the conditional instructions. The number of bus read and write cycles is indicated in parenthesis as: (r/w). The number of clock periods and the number of read and write cycles must be added respectively to those of the effective address calculation where indicated.

JMP, JSR, LEA, PWA, MOVEM INSTRUCTION CLOCK PERIODS

Table 32 indicates the number of clock periods required for the jump, jump to subroutine, load effective address, push effective address, and move multiple registers instructions. The number of bus read and write cycles is shown in parenthesis as: (r/w).

Table 29. Shift/Rotate Instruction Clock Periods

Instruction	Size	Register	Memory
ASR, ASL	Byte, Word	**6** + **2n**(1/0)	**8**(1/1) +
	Long	**8** + **2n**(1/0)	—
LSR, LSL	Byte, Word	**6** + **2n**(1/0)	**8**(1/1) +
	Long	**8** + **2n**(1/0)	—
ROR, ROL	Byte, Word	**6** + **2n**(1/0)	**8**(1/1) +
	Long	**8** + **2n**(1/0)	—
ROXR, ROXL	Byte, Word	**6** + **2n**(1/0)	**8**(1/1) +
	Long	**8** + **2n**(1/0)	—

+ add effective address calculation time
n is shift or rotate count

Table 30. Bit Manipulation Instruction Clock Periods

Instruction	Size	Dynamic		Static	
		Register	Memory	Register	Memory
BCHG	Byte	—	**8**(1/1) +	—	**12**(2/1) +
	Long	**8**(1/0)*	—	**12**(2/0)*	—
BCLR	Byte	—	**8**(1/1) +	—	**12**(2/1) +
	Long	**10**(1/0)*	—	**14**(2/0)*	—
BSET	Byte	—	**8**(1/1) +	—	**12**(2/1) +
	Long	**8**(1/0)*	—	**12**(2/0)*	—
BTST	Byte	—	**4**(1/0) +	—	**8**(2/0) +
	Long	**6**(1/0)	—	**10**(2/0)	—

+ add effective address calculation time
* indicates maximum value

Table 31. Conditional Instruction Clock Periods

Instruction	Displacement	Branch Taken	Branch Not Taken
B_{CC}	Byte	10(2/0)	8(1/0)
	Word	10(2/0)	12(2/0)
BRA	Byte	10(2/0)	—
	Word	10(2/0)	—
BSR	Byte	18(2/2)	—
	Word	18(2/2)	—
DB_{CC}	CC true	—	12(2/0)
	CC false	10(2/0)	14(3/0)

Table 32. JMP, JSR, LEA, PEA, MOVEM INSTRUCTION CLOCK PERIODS

Instr	Size	(An)	(An)+	−(An)	d(An)	d(An, ix)* +	xxx.W	xxx.L	d(PC)	d(PC, ix)*
JMP	—	8(2/0)	—	—	10(2/0)	14(3/0)	10(2/0)	12(3/0)	10(2/0)	14(3/0)
JSR	—	16(2/2)	—	—	18(2/2)	22(2/2)	18(2/2)	20(3/2)	18(2/2)	22(2/2)
LEA	—	4(1/0)	—	—	8(2/0)	12(2/0)	8(2/0)	12(3/0)	8(2/0)	12(2/0)
PEA	—	12(1/2)	—	—	16(2/2)	20(2/2)	16(2/2)	20(3/2)	16(2/2)	20(2/2)
MOVEM M → R	Word	12 + 4n (3 + n/0)	12 + 4n (3 + n/0)	—	16 + 4n (4 + n/0)	18 +4n (4 + n/0)	16 + 4n (4 + n/0)	20 + 4n (5 + n/0)	16 + 4n (4 + n/0)	18 + 4n (4 + n/0)
	Long	12 + 8n (3 + 2n/0)	12 + 8n (3 + 2n/0)	—	16 + 8n (4 + 2n/0)	18 + 8n (4 + 2n/0)	16 + 8n (4 + 2n/0)	20 + 8n (5 + 2n/0)	16 + 8n (4 + 2n/0)	18 + 8n (4 + 2n/0)
MOVEM R → M	Word	8 + 4n (2/n)	—	8 + 4n (2/n)	12 + 4n (3/n)	14 + 4n (3/n)	12 + 4n (3/n)	16 + 4n (4/n)	— —	— —
	Long	8 + 8n (2/2n)	— —	8 + 8n (2/2n)	12 + 8n (3/2n)	14 + 8n (3/2n)	12 + 8n (3/2n)	16 + 8n (4/2n)	— —	— —

n is the number of registers to move
* The size of the index register (ix) does not affect the instruction's execution time

MULTI-PRECISION INSTRUCTION CLOCK PERIODS

Table 33 delineates the number of clock periods for the multi-precision instructions. The number of clock periods includes the time to fetch both operands, perform the operations, store the results, and read the next instructions. The number of read and write cycles is shown in parenthesis as: (r/w).

In Table 33, the headings have the following meanings: Dn = data register operand and M = memory operand.

Table 33. Multi-Precision Instruction Clock Periods

Instruction	Size	op Dn, Dn	op M, M
ADDX	Byte, Word	4(1/0)	18(3/1)
	Long	8(1/0)	30(5/2)
CMPM	Byte, Word	—	12(3/0)
	Long	—	20(5/0)
SUBX	Byte, Word	4(1/0)	18(3/1)
	Long	8(1/0)	30(5/2)
ABCD	Byte	6(1/0)	18(3/1)
SBCD	Byte	6(1/0)	18(3/1)

MISCELLANEOUS INSTRUCTION CLOCK PERIODS

Table 34 and 35 indicate the number of clock periods for the following miscellaneous instructions. The number of bus read and write cycles is shown in parenthesis as: (r/w). The number of clock periods plus the number of read and write cycles must be added to those of the effective address calculation where indicated.

EXCEPTION PROCESSING CLOCK PERIODS

Table 36 delineates the number of clock periods for exception processing. The number of clock periods includes the time for all stacking, the vector fetch, and the fetch of the first instruction of the handler routine. The number of bus read and write cycles is shown in parenthesis as (r/w).

Table 34. Miscellaneous Instruction Clock Periods

Instruction	Size	Register	Memory	Instruction	Size	Register	Memory
ANDI to CCR	Byte	**20**(3/0)	—	LINK	—	**16**(2/2)	—
ANDI to SR	Word	**20**(3/0)	—	MOVE from USP	—	**4**(1/0)	—
CHK	—	**10**(1/0)+	—	MOVE to USP	—	**4**(1/0)	—
EORI to CCR	Byte	**20**(3/0)	—	NOP	—	**4**(1/0)	—
EORI to SR	Word	**20**(3/0)	—	RESET	—	**132**(1/0)	—
ORI to CCR	Byte	**20**(3/0)	—	RTE	—	**20**(5/0)	—
ORI to SR	Word	**20**(3/0)	—	RTR	—	**20**(5/0)	—
MOVE from SR	—	**6**(1/0)	**8**(1/1)+	RTS	—	**16**(4/0)	—
MOVE to CCR	—	**12**(2/0)	**12**(2/0)+	STOP	—	**4**(0/0)	—
MOVE to SR	—	**12**(2/0)	**12**(2/0)+	SWAP	—	**4**(1/0)	—
EXG	—	**6**(1/0)	—	TRAPV	—	**4**(1/0)	—
EXT	Word	**4**(1/0)	—	UNLK	—	**12**(3/0)	—
	Long	**4**(1/0)	—				
+ add effective address calculation time							

Table 35. Move Peripheral Instruction Execution Times

Instruction	Size	Register→Memory	Memory→Register
MOVEP	Word	**16**(2/2)	**16**(4/0)
	Long	**24**(2/4)	**24**(6/0)

Table 36. Exception Processing Clock Periods

Exception	Periods
Address Error	**50**(4/7)
Bus Error	**50**(4/7)
CHK Instruction	**44**(5/4)+
Divide by Zero	**42**(5/4)
Illegal Instruction	**34**(4/3)
Interrupt	**44**(5/3)*
Privilege Violation	**34**(4/3)
$\overline{\text{RESET}}$**	**40**(6/0)
Trace	**34**(4/3)
TRAP Instruction	**38**(4/4)
TRAPV Instruction	**34**(4/3)

\+ add effective address calculation time
* The interrupt acknowledge cycle is assumed to take four clock periods.
** Indicates the time from when $\overline{\text{RESET}}$ and $\overline{\text{HALT}}$ are first sampled as negated to when instruction execution starts.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to +7.0	V
Input Voltage	V_{IN}	−0.3 to +7.0	V
Operating Temperature Range	T_A	T_L to T_H*	°C
Storage Temperature	T_{STG}	−65 to +150	°C
*See ordering information			

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Thermal Resistance	θ_{JA}		
64-Pin Ceramic		30	°C/W
64-Pin Plastic Dip		55 ±5	°C/W

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{CC}.

POWER CONSIDERATIONS

The average chip-junction temperature, T_J, in °C can be obtained from:

$$T_J = T_A + (P_D \cdot \theta_{JA}) \quad (1)$$

Where:

$T_A \equiv$ Ambient Temperature, °C

$\theta_{JA} \equiv$ Package Thermal Resistance, Junction-to-Ambient, °C/W

$P_D \equiv P_{INT} + P_{I/O}$

$P_{INT} \equiv I_{CC} \cdot V_{CC}$, Watts—Chip Internal Power

$P_{I/O} \equiv$ Power Dissipation on Input and Output Pins—User Determined

For most applications $P_{I/O} \ll P_{INT}$ and can be neglected.

An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = K \div (T_J + 273°C) \quad (2)$$

Solving equations 1 and 2 for K gives:

$$K = P_D \cdot (T_A + 273°C) + \theta_{JA} \cdot P_D^2 \quad (3)$$

Where K is a constant pertaining to the particular part. K can be determined from equation 3 by measuring P_D (at equilibrium) for a known T_A. Using this value of K the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A.

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DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0 Vdc ±5%, V_{SS} = 0 Vdc, T_A = T_L to T_H °C. See Figures 41, 42, and 43.)

Characteristic	Symbol	Min	Max	Unit	Test Conditions
Input High Voltage	V_{IH}	2.0	V_{CC}	V	
Input Low Voltage	V_{IL}	V_{SS} − 0.3	0.8	V	
Input Leakage Current	I_{IN}				
$\overline{BERR}$, $\overline{BGACK}$, $\overline{BR}$, $\overline{DTACK}$, CLK, $\overline{IPL0}$–$\overline{IPL2}$, $\overline{VPA}$		—	2.5	μA	V_{IN} = 5.25
$\overline{HALT}$, $\overline{RESET}$		—	20	μA	V_{CC} = OV
Three-State (Off State) Input Current	I_{TSI}	—	20	μA	
$\overline{AS}$, A1–A23, D0–D15, FC0–FC2, $\overline{LDS}$, R/$\overline{W}$, $\overline{UDS}$, $\overline{VMA}$					V_{IN} = 0.4V to 2.4V V_{CC} = 5.25V
Output High Voltage	V_{OH}				
E*		V_{CC} − 0.75	—	V	V_{CC} = 4.75V
E, $\overline{AS}$, A1–A23, $\overline{BG}$, D0–D15, FC0–FC2, $\overline{LDS}$, R/$\overline{W}$, $\overline{UDS}$, $\overline{VMA}$		2.4	—	V	I_{OH} = −400 μA
Output Low Voltage	V_{OL}				V_{CC} = 4.75V
$\overline{HALT}$		—	0.5	V	(I_{OL} = 1.6 mA)
$\overline{BG}$, FC0–FC2, A1–A23		—	0.5	V	(I_{OL} = 3.2 mA)
$\overline{RESET}$		—	0.5	V	(I_{OL} = 5.0 mA)
$\overline{AS}$, D0–D15, $\overline{LDS}$, R/$\overline{W}$ $\overline{UDS}$, $\overline{VMA}$, E		—	0.5	V	(I_{OL} = 5.3 mA)
Power Dissipation	P_D***	—	1.5	W	
Input Capacitance	C_{IN}	—	20.0	pF	V_{CC} = 5.0V, V_{IN} = OV f = 1 MHz, T_A = 25°C

*With external pullup resistor of 1.1 kΩ

**Capacitance is periodically sampled rather than 100% tested.

***During normal operation instantaneous V_{CC} current requirements may be as high as 1.5A.

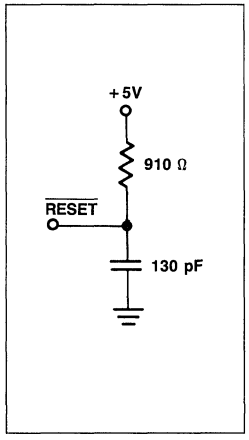


Figure 41. $\overline{\text{RESET}}$ Test Load

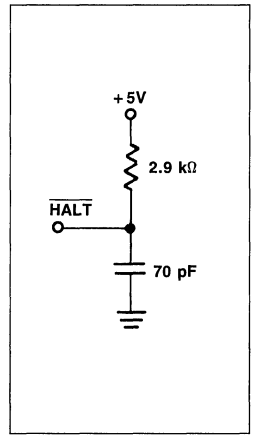


Figure 42. $\overline{\text{HALT}}$ Test Load

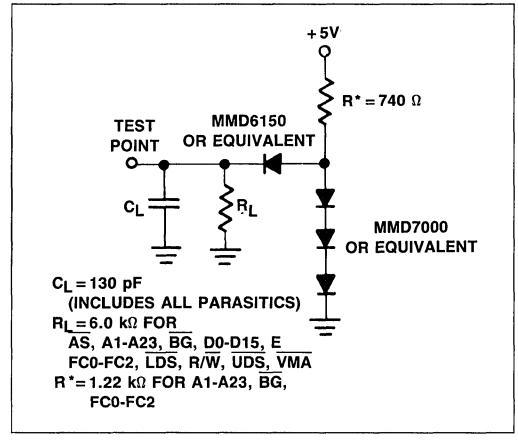


Figure 43. Test Loads

CLOCK TIMING (See Figure 44)

Characteristic	Symbol	4 MHz		6 MHz		8 MHz		10 MHz		12.5 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Frequency of Operation	F	2.0	4.0	2.0	6.0	2.0	8.0	2.0	10.0	4.0	12.5	MHz
Cycle Time	t_{cyc}	250	500	167	500	125	500	100	500	80	250	ns
Clock Pulse Width	t_{CL} t_{CH}	115 115	250 250	75 75	250 250	55 55	250 250	45 45	250 250	35 35	125 125	ns
Rise and Fall Times	t_{Cr} t_{Cf}	— —	10 10	— —	10 10	— —	10 10	— —	10 10	— —	5 5	ns

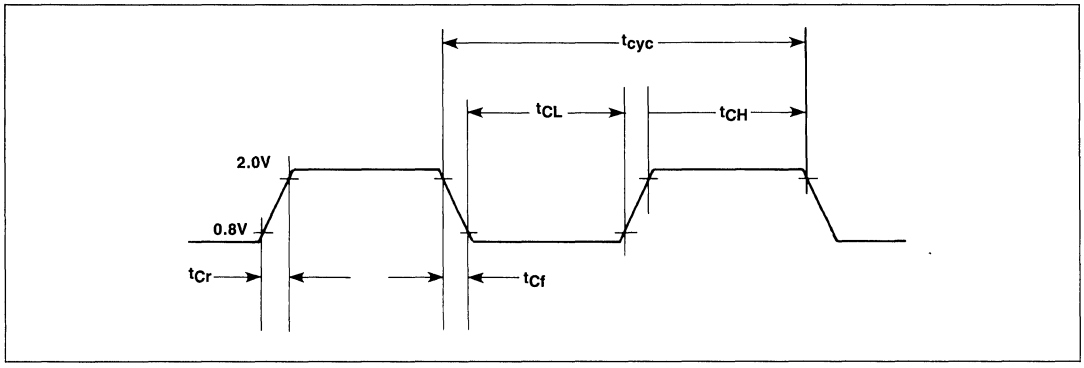


Figure 44. Input Clock Waveform

AC ELECTRICAL SPECIFICATIONS — READ AND WRITE CYCLES

(V_{CC} = 5.0 Vdc ±5%, V_{SS} = 0 Vdc; $T_A = T_L$ to T_H, see Figures 45 and 46)

Num.	Characteristic	Symbol	4 MHz		6 MHz		8 MHz		10 MHz		12.5 MHz		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
1	Clock Period	t_{cyc}	250	500	167	500	125	500	100	500	80	250	ns
2	Clock Width Low	t_{CL}	115	250	75	250	55	250	45	250	35	125	ns
3	Clock Width High	t_{CH}	115	250	75	250	55	250	45	250	35	125	ns
4	Clock Fall Time	t_{Cf}	—	10	—	10	—	10	—	10	—	5	ns
5	Clock Rise Time	t_{Cr}	—	10	—	10	—	10	—	10	—	5	ns
6	Clock Low to Address	t_{CLAV}	—	90	—	80	—	70	—	60	—	55	ns
6A	Clock High to FC Valid	t_{CHFCV}	—	90	—	80	—	70	—	60	—	55	ns
7	Clock High to Address Data High Impedance (Maximum)	t_{CHAZx}	—	120	—	100	—	80	—	70	—	60	ns
8	Clock High to Address/FC Invalid (Minimum)	t_{CHAZn}	0	—	0	—	0	—	0	—	0	—	ns
9[1]	Clock High to $\overline{AS}$, $\overline{DS}$ Low (Maximum)	t_{CHSLx}	—	80	—	70	—	60	—	55	—	55	ns
10	Clock High to $\overline{AS}$, $\overline{DS}$ Low (Minimum)	t_{CHSLn}	0	—	0	—	0	—	0	—	0	—	ns
11[2]	Address to $\overline{AS}$, $\overline{DS}$ (Read) Low/$\overline{AS}$ Write	t_{AVSL}	55	—	35	—	30	—	20	—	0	—	ns
11A[2]	FC Valid to $\overline{AS}$, $\overline{DS}$ (Read) Low/$\overline{AS}$ Write	t_{FCVSL}	80	—	70	—	60	—	50	—	40	—	ns
12[1]	Clock Low to $\overline{AS}$, $\overline{DS}$ High	t_{CLSH}	—	90	—	80	—	70	—	55	—	50	ns
13[2]	$\overline{AS}$, $\overline{DS}$ High to Address/FC Invalid	t_{SHAZ}	60	—	40	—	30	—	20	—	10	—	ns
14[2]	$\overline{AS}$, $\overline{DS}$ Width Low (Read)/$\overline{AS}$ Write	t_{SL}	535	—	337	—	240	—	195	—	160	—	ns
14A[2]	$\overline{DS}$ Width Low (Write)	t_{DWPW}	285	—	170	—	115	—	95	—	80	—	ns
15[2]	$\overline{AS}$, $\overline{DS}$ Width High	t_{SH}	285	—	180	—	150	—	105	—	65	—	ns
16	Clock High to $\overline{AS}$, $\overline{DS}$ High	t_{CHSZ}	—	120	—	100	—	80	—	70	—	60	ns
17[2]	$\overline{AS}$, $\overline{DS}$ High to R/$\overline{W}$ High	t_{SHRH}	60	—	50	—	40	—	20	—	10	—	ns
18[1]	Clock High to R/$\overline{W}$ High (Maximum)	t_{CHRHx}	—	90	—	80	—	70	—	60	—	60	ns
19	Clock High to R/$\overline{W}$ High (Minimum)	t_{CHRHn}	0	—	0	—	0	—	0	—	0	—	ns
20[1]	Clock High to R/$\overline{W}$ Low	t_{CHRL}	—	90	—	80	—	70	—	60	—	60	ns
20A[6]	$\overline{AS}$ Low to R/$\overline{W}$ Valid	t_{ASRV}	—	20	—	20	—	20	—	20	—	20	ns
21[2]	Address Valid to R/$\overline{W}$ Low	t_{AVRL}	45	—	25	—	20	—	0	—	0	—	ns
21A[2]	FC Valid to R/$\overline{W}$ Low	t_{FCVRL}	80	—	70	—	60	—	50	—	30	—	ns
22[2]	R/$\overline{W}$ Low to $\overline{DS}$ Low (Write)	t_{RLSL}	200	—	140	—	80	—	50	—	30	—	ns
23	Clock Low to Data Out Valid	t_{CLDO}	—	90	—	80	—	70	—	55	—	55	ns
24	Clock High to R/$\overline{W}$, $\overline{VMA}$ High Impedance	t_{CHRZ}	—	120	—	100	—	80	—	70	—	60	ns
25[2]	$\overline{DS}$ High to Data Out Invalid	t_{SHDO}	60	—	40	—	30	—	20	—	15	—	ns
26[2]	Data Out Valid to $\overline{DS}$ Low (Write)	t_{DOSL}	55	—	35	—	30	—	20	—	15	—	ns
27[5]	Data In to Clock Low (Setup Time)	t_{DICL}	30	—	25	—	15	—	10	—	10	—	ns
27A	Late $\overline{BERR}$ Low to Clock Low (Setup Time)	t_{BELCL}	45	—	45	—	45	—	45	—	45	—	ns
28[2]	$\overline{AS}$, $\overline{DS}$ High to $\overline{DTACK}$ High	t_{SHDAH}	0	490	0	325	0	245	0	190	0	150	ns

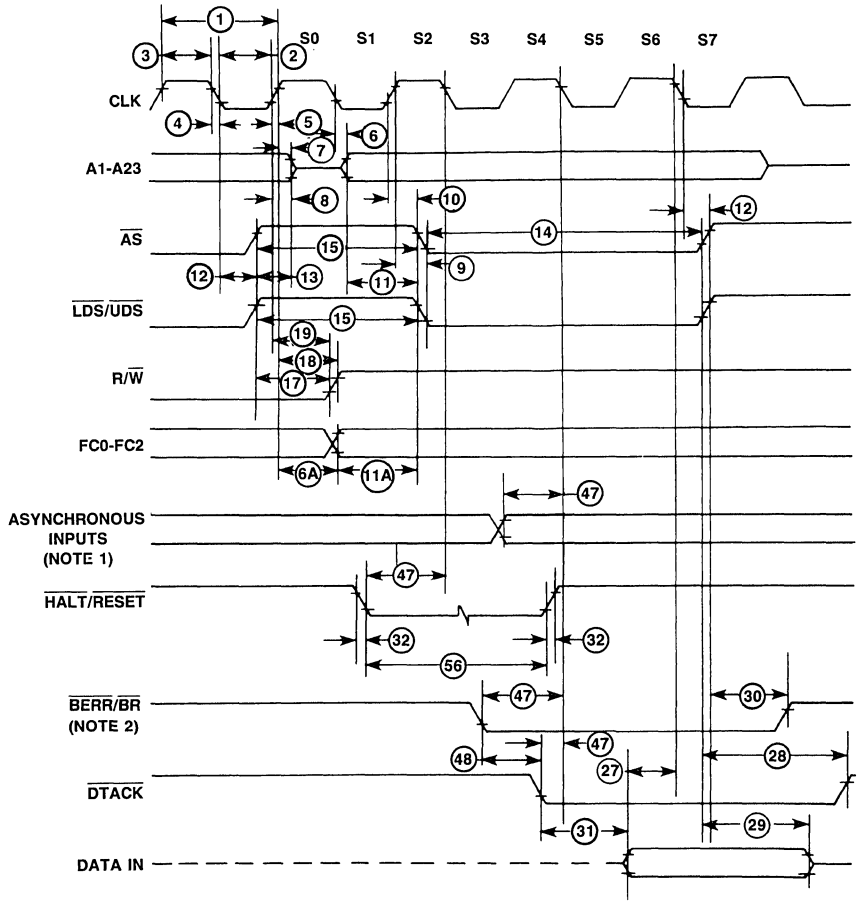
4

AC ELECTRICAL SPECIFICATIONS — READ AND WRITE CYCLES (CONTINUED)

Num.	Characteristic	Symbol	4 MHz		6 MHz		8 MHz		10 MHz		12.5 MHz		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
29	$\overline{DS}$ High to Data Invalid (Hold Time)	t_{SHDI}	0	—	0	—	0	—	0	—	0	—	ns
30	$\overline{AS}$, $\overline{DS}$ High to $\overline{BERR}$ High	t_{SHBEH}	0	—	0	—	0	—	0	—	0	—	ns
31[2,5]	$\overline{DTACK}$ Low to Data In (Setup Time)	t_{DALDI}	—	180	—	120	—	90	—	65	—	50	ns
32	$\overline{HALT}$ and $\overline{RESET}$ Input Transition Time	$t_{RHr,f}$	0	200	0	200	0	200	0	200	0	200	ns
33	Clock High to $\overline{BG}$ Low	t_{CHGL}	—	90	—	80	—	70	—	60	—	50	ns
34	Clock High to $\overline{BG}$ High	t_{CHGH}	—	90	—	80	—	70	—	60	—	50	ns
35	$\overline{BR}$ Low to $\overline{BG}$ Low	t_{BRLGL}	1.5	3.5	1.5	3.5	1.5	3.5	1.5	3.5	1.5	3.5	Clk. Per.
36	$\overline{BR}$ High to $\overline{BG}$ High	t_{BRHGH}	1.5	3.5	1.5	3.5	1.5	3.5	1.5	3.5	1.5	3.5	Clk. Per.
37	$\overline{BGACK}$ Low to $\overline{BG}$ High	t_{GALGH}	1.5	3.0	1.5	3.0	1.5	3.0	1.5	3.0	1.5	3.0	Clk. Per.
37A	$\overline{BGACK}$ Low to $\overline{BR}$ High (to Prevent Rearbitration)	t_{BGKBR}	30	—	25	—	20	—	20	—	20	—	ns
38	$\overline{BG}$ Low to Bus High Impedance (with $\overline{AS}$ High)	t_{GLZ}	—	120	—	100	—	80	—	70	—	60	ns
39	$\overline{BG}$ Width High	t_{GH}	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	Clk. Per.
40	Clock Low to $\overline{VMA}$ Low	t_{CLVML}	—	90	—	80	—	70	—	70	—	70	ns
41	Clock Low to E Transition	t_{CLC}	—	100	—	85	—	70	—	55	—	45	ns
42	E Output Rise and Fall Time	$t_{Er,f}$	—	25	—	25	—	25	—	25	—	25	ns
43	$\overline{VMA}$ Low to E High	t_{VMLEH}	325	—	240	—	200	—	150	—	90	—	ns
44	$\overline{AS}$, $\overline{DS}$ High to $\overline{VPA}$ High	t_{SHVPH}	0	240	0	160	0	120	0	90	0	70	ns
45	E Low to Address/$\overline{VMA}$/FC Invalid	t_{ELAI}	55	—	35	—	30	—	10	—	10	—	ns
46	$\overline{BGACK}$ Width	t_{BGL}	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	Clk. Per.
47[5]	Asynchronous Input Setup Time	t_{ASI}	30	—	25	—	20	—	20	—	20	—	ns
48[3,5]	$\overline{BERR}$ Low to $\overline{DTACK}$ Low	t_{BELDAL}	30	—	25	—	20	—	20	—	20	—	ns
49	E Low to $\overline{AS}$, $\overline{DS}$ Invalid	t_{ELSI}	−80	—	−80	—	−80	—	−80	—	−80	—	ns
50	E Width High	t_{EH}	900	—	600	—	450	—	350	—	280	—	ns
51	E Width Low	t_{EL}	1400	—	900	—	700	—	550	—	440	—	ns
52	E Extended Rise Time	t_{CIEHX}	—	80	—	80	—	80	—	80	—	80	ns
53	Data Hold from Clock High	t_{CHDO}	0	—	0	—	0	—	0	—	0	—	ns
54	Data Hold from E Low (Write)	t_{ELDOZ}	60	—	40	—	30	—	20	—	15	—	ns
55	R/$\overline{W}$ to Data Bus Impedance Change	t_{RLDO}	55	—	35	—	30	—	20	—	10	—	ns
56[4]	$\overline{HALT}$/$\overline{RESET}$ Pulse Width	t_{HRPW}	10	—	10	—	10	—	10	—	10	—	Clk. Per.

Notes:

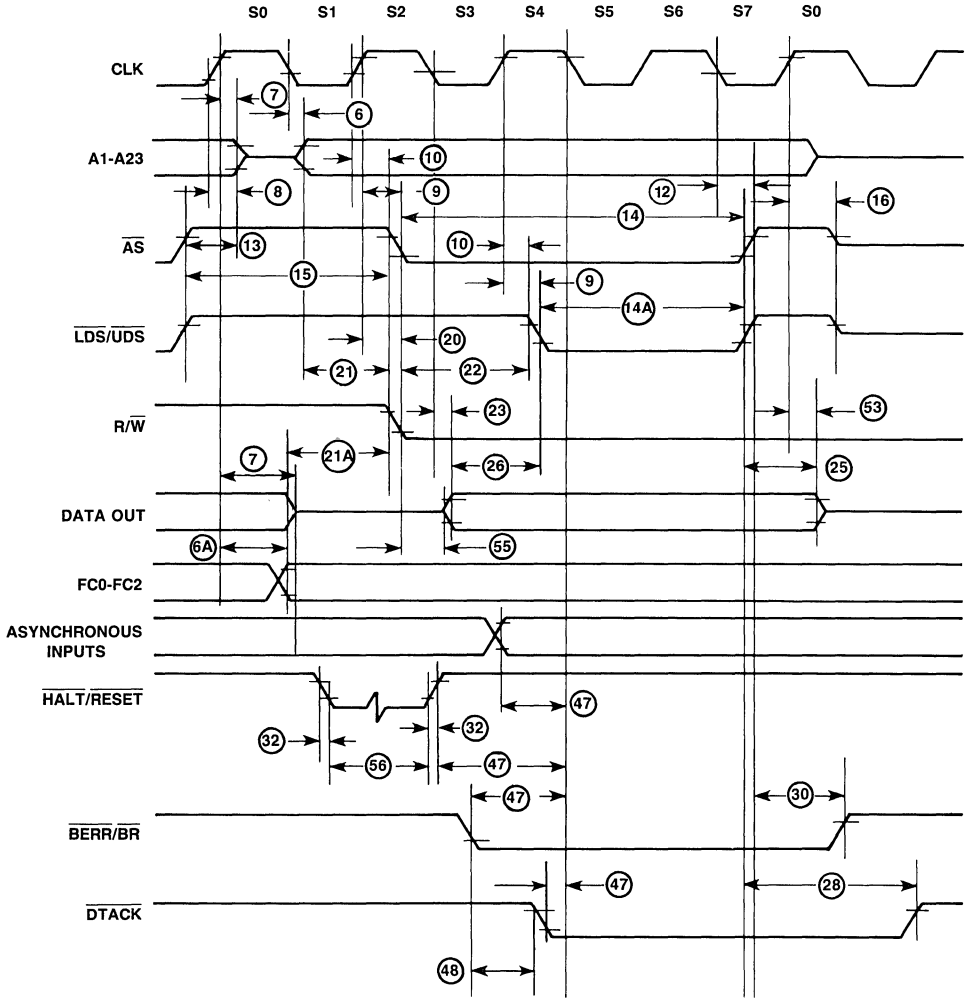
1. For a loading capacitance of less than or equal to 50 picofarads, subtract 5 nanoseconds from the value given in these columns.
2. Actual value depends on clock period.
3. If #47 is satisfied for both $\overline{DTACK}$ and $\overline{BERR}$, #48 may be 0 nanoseconds.
4. For power up, the MPU must be held in $\overline{RESET}$ state for 100 ms to stabilize all on-chip circuitry. After the system is powered up, #56 refers to the minimum pulse width required to reset the system.
5. If the asynchronous setup time (#47) requirements are satisfied the $\overline{DTACK}$ low-to-data setup time (#31) requirement can be ignored. The data must only satisfy the data-in clock-low setup time (#27) for the following cycle.
6. When $\overline{AS}$ and R/$\overline{W}$ are equally loaded (±20%), subtract 10 nanoseconds from the value given in these columns.



NOTES:

1. SETUP TIME FOR THE ASYNCHRONOUS INPUTS BGACK, IPL0-IPL2, AND VPA GUARANTEES THEIR RECOGNITION AT THE NEXT FALLING EDGE OF THE CLOCK.
2. BR NEEDS FALL AT THIS TIME ONLY IN ORDER TO INSURE BEING RECOGNIZED AT THE END OF THIS BUS CYCLE.
3. TIMING MEASUREMENTS ARE REFERENCED TO AND FROM A LOW VOLTAGE OF 0.8 VOLTS AND A HIGH VOLTAGE OF 2.0 VOLTS, UNLESS OTHERWISE NOTED.

Figure 45. Read Cycle Timing



NOTES:
1. BECAUSE OF LOADING VARIATIONS, R/$\overline{W}$ MAY BE VALID AFTER $\overline{AS}$ EVEN THOUGH BOTH ARE INITIATED BY THE RISING EDGE OF S2 (SPECIFICATION 20A).
2. TIMING MEASUREMENTS ARE REFERENCED TO AND FROM A LOW VOLTAGE OF 0.8 VOLTS AND A HIGH VOLTAGE OF 2.0 VOLTS, UNLESS OTHERWISE NOTED.

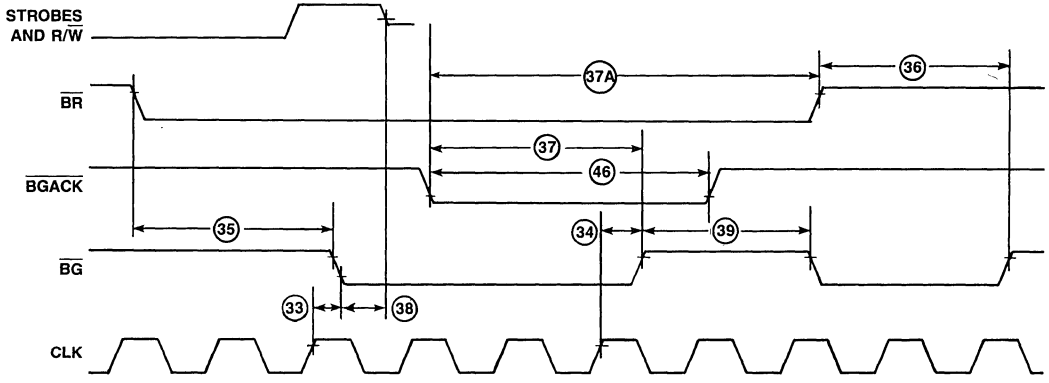
Figure 46. Write Cycle Timing

AC ELECTRICAL SPECIFICATIONS — BUS ARBITRATION

(V_{CC} = 5.0 Vdc ±5%, V_{SS} = 0 Vdc, T_A = T_L to T_H °C. See Figure 47.)

Num.	Characteristic	Symbol	4 MHz		6 MHz		8 MHz		10 MHz		12.5 MHz		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
33	Clock High to $\overline{BG}$ Low	t_{CHGL}	—	90	—	80	—	70	—	60	—	50	ns
34	Clock High to $\overline{BG}$ High	t_{CHGH}	—	90	—	80	—	70	—	60	—	50	ns
35	$\overline{BR}$ Low to $\overline{BG}$ Low	t_{BRLGL}	1.5	3.5	1.5	3.5	1.5	3.5	1.5	3.5	1.5	3.5	Clk. Per.
36	$\overline{BR}$ High to $\overline{BG}$ High	t_{BRHGH}	1.5	3.5	1.5	3.5	1.5	3.5	1.5	3.5	1.5	3.5	Clk. Per.
37	$\overline{BGACK}$ Low to $\overline{BG}$ High	t_{GALGH}	1.5	3.0	1.5	3.0	1.5	3.0	1.5	3.0	1.5	3.0	Clk. Per.
37A	$\overline{BGACK}$ Low to $\overline{BR}$ High (to Prevent Rearbitration)	t_{BGKBR}	30	—	25	—	20	—	20	—	20	—	ns
38	$\overline{BG}$ Low to Bus High Impedance (with $\overline{AS}$ High)	t_{GLZ}	—	120	—	100	—	80	—	70	—	60	ns
39	$\overline{BG}$ Width High	t_{GH}	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	Clk. Per.
46	$\overline{BGACK}$ Width	t_{BGL}	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	Clk. Per.

THESE WAVEFORMS SHOULD ONLY BE REFERENCED IN REGARD TO THE EDGE-TO-EDGE MEASUREMENT OF THE TIMING SPECIFICATIONS. THEY ARE NOT INTENDED AS A FUNCTIONAL DESCRIPTION OF THE INPUT AND OUTPUT SIGNALS. REFER TO OTHER FUNCTIONAL DESCRIPTIONS AND THEIR RELATED DIAGRAMS FOR DEVICE OPERATION.



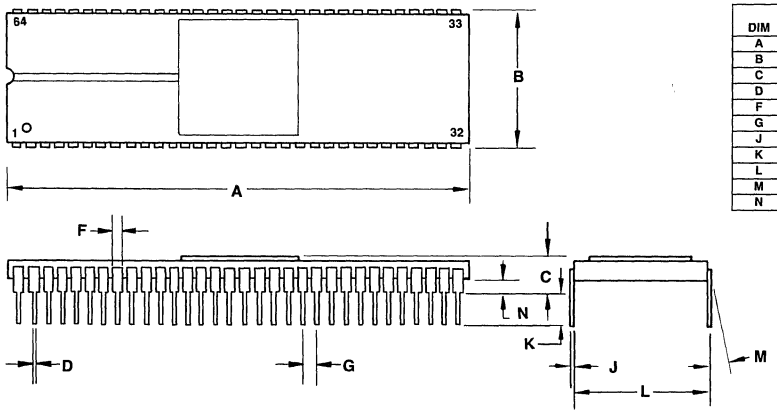
NOTES:

1. SETUP TIME FOR THE ASYNCHRONOUS INPUTS $\overline{BERR}$, $\overline{BGACK}$, $\overline{BR}$, $\overline{DTACK}$, $\overline{IPL0}$-$\overline{IPL2}$, AND $\overline{VPA}$ GUARANTEES THEIR RECOGNITION AT THE NEXT FALLING EDGE OF THE CLOCK.
2. WAVEFORM MEASUREMENTS FOR ALL INPUTS AND OUTPUTS ARE SPECIFIED AT: LOGIC HIGH = 2.0 VOLTS, LOGIC LOW = 0.8 VOLTS

Figure 47. AC ELECTRICAL Waveforms — Bus Arbitration

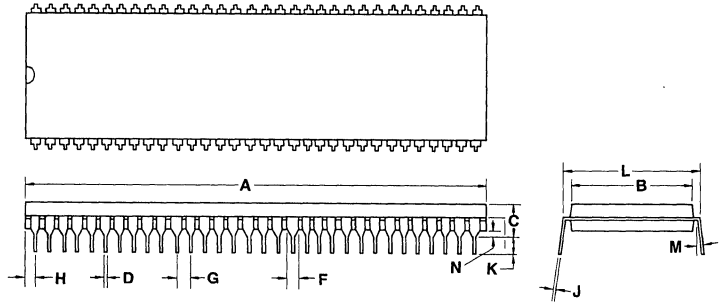
PACKAGE DIMENSIONS

64-PIN CERAMIC DUAL IN-LINE PACKAGE (DIP)



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	80.52	82.04	3.170	3.230
B	22.25	22.96	0.876	0.904
C	3.05	4.32	0.120	0.170
D	0.38	0.53	0.015	0 021
F	0.76	1.40	0.030	0.055
G	2.54 BSC		0.100 BSC	
J	0.20	0.33	0 008	0.013
K	2.54	4.19	0.100	0.165
L	22.61	23.11	0.890	0.910
M	—	10°	—	10°
N	1.02	1.52	0.040	0.060

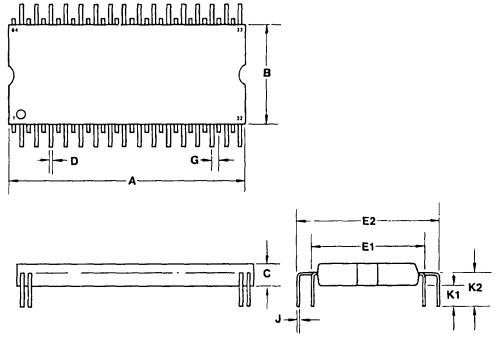
64-PIN PLASTIC DUAL IN-LINE PACKAGE (DIP)



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	81.15	81.91	3.195	3.225
B	20.07	20.57	0.790	0.810
C	4.32	4.82	0 170	0.190
D	0.38	0.58	0.015	0.023
F	1.42	1.62	0.056	0.064
G	2.54 BSC		0.100 BSC	
H	1.15	1.65	0.045	0.065
J	0.20	0.30	0.008	0 012
K	3.05	3.55	0.120	0.140
L	22.71	23.01	0.894	0.906
M	0	10	0	10
N	0.51	1.01	0.020	0.040

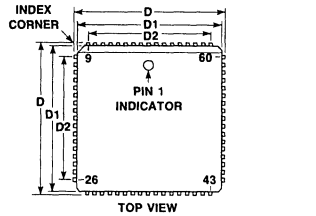
64-PIN PLASTIC QUAD IN-LINE PACKAGE (QUIP)

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	41.10	41.61	1.618	1.638
B	17.02	17 23	0 670	0.690
C	3 56	4.58	0.140	0.180
D	0 48	0.56	0 018	0 022
E1	19.05 BSC		0.750 BSC	
E2	23.50 BSC		0.925 BSC	
G	1.27 BSC		0.050 BSC	
J	0.18	0.33	0.007	0.013
K1	2.92	3.18	0.115	0.125
K2	4 83	5.34	0.190	0 210

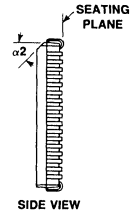


4

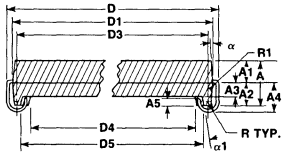
68-PIN PLASTIC CHIP CARRIER (PCC)



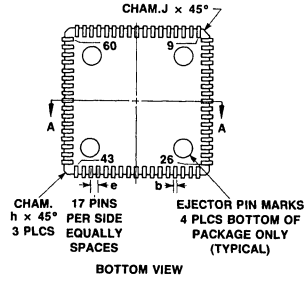
TOP VIEW



SIDE VIEW



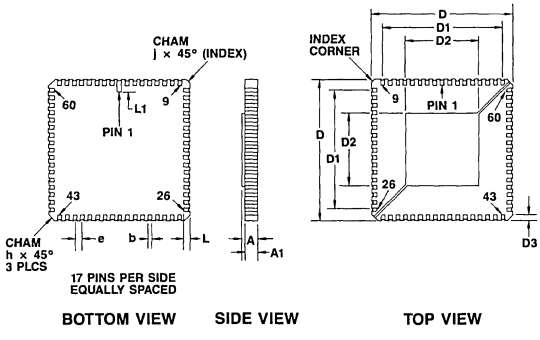
SECTION A-A
TYP FOR BOTH AXIS (EXCEPT FOR BEVELED EDGE)



BOTTOM VIEW

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	3.683	3.785	.145	.149
A1	1.829	1.930	.072	.076
A2	1.803	1.905	.071	.075
A3	1.372	1.473	.054	.058
A4	2.311	2.464	.091	.097
A5	0.203	0.305	.008	.012
b	0.457 TYP		.018 TYP	
D	25.02	25.27	.985	.995
D1	24.00	24.26	.945	.955
D2	20.19	20.45	.795	.805
D3	23.24	23.50	.915	.925
D4	20.96	21.21	.825	.835
D5	22.23	22.48	.875	.885
e	1.27 BSC		.050 BSC	
h	0.254 TYP		.010 TYP	
J	1.143 TYP		.045 TYP	
α	4° TYP		4° TYP	
α1	10° TYP		10° TYP	
α2	45° TYP		45° TYP	
R	0.889 TYP		.035 TYP	
R1	0.254 TYP		.010 TYP	

68-PIN CERAMIC CHIP CARRIER (LCC)



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.65	1.91	0.065	0.075
A1	1.40	1.65	0.055	0.065
b	0.51	0.76	0.020	0.030
D	23.83	24.43	0.938	0.962
D1	20.12	20.52	0.792	0.808
D2	12.45	12.70	0.490	0.500
D3	1.27 REF		0.050 REF	
e	1.27 BSC		0.050 BSC	
h	1.02 REF		0.040 REF	
j	0.51 REF		0.020 REF	
L	1.27 REF		0.050 REF	
L1	1.96	2.36	0.077	0.093

4

Rockwell

R68C552
Dual Asynchronous Communications Interface Adapter (DACIA)

PRELIMINARY

DESCRIPTION

The Rockwell CMOS R68C552 Dual Asynchronous Communications Interface Adapter (DACIA) provides an easily implemented, program controlled two-channel interface between 16-bit microprocessor-based systems and serial communication data sets and modems.

The DACIA is designed for maximum programmed control from the microprocessor (MPU) to simplify hardware implementation. Dual sets of registers allow independent control and monitoring of each channel.

Transmitter and Receiver bit rates may be controlled by an internal baud rate generator or external times 16 clocks. The baud rate generator accepts either a crystal or a clock input, and provides 15 programmable baud rates. When a 3.6864 MHz crystal is used, the baud rates range from 50 bps to 38,400 bps.

The DACIA may be programmed to transmit and receive frames having word lengths of 5, 6, 7 or 8 bits; even, odd, space, mark or no parity; and 1 or 2 stop bits.

A Compare Register, and the ability to detect address frames, facilitate address recognition in a multidrop mode.

FEATURES

- Low power CMOS N-well silicon gate technology
- Two independent full duplex channels with buffered receivers and transmitters.
- Data set/modem control functions
- Internal baud rate generator with 15 programmable baud rates (50 bps to 38,400 bps)
- Program-selectable internally or externally controlled receiver and transmitter bit rates
- Programmable word lengths, number of stop bits, and parity bit generation and detection
- Programmable interrupt control
- Edge detect for $\overline{DCD}$, $\overline{DSR}$, and $\overline{CTS}$
- Program-selectable echo mode for each channel
- Compare Register
- Address/Data frame recognition
- 5.0 Vdc ±5% supply requirements
- 40-pin plastic or ceramic DIP or 44-pin PLCC
- Full TTL or CMOS input/output compatibility
- Compatible with R68000 microprocessors

ORDERING INFORMATION

Part Number:
R68C552

Temperature Range (T_L to T_H):
Blank = 0°C to +70°C
E = −40°C to +85°C

Package:
C = 40-Pin Ceramic DIP
P = 40-Pin Plastic DIP
J = 44-Pin Plastic Leaded Chip Carrier (PLCC)

INTERFACE SIGNALS

The DACIA is available in a 40-pin DIP or a 44-pin PLCC. Figure 1 shows the pin assignments for each package. The DACIA interface signals are shown in Figure 2. Table 1 contains a description of each signal.

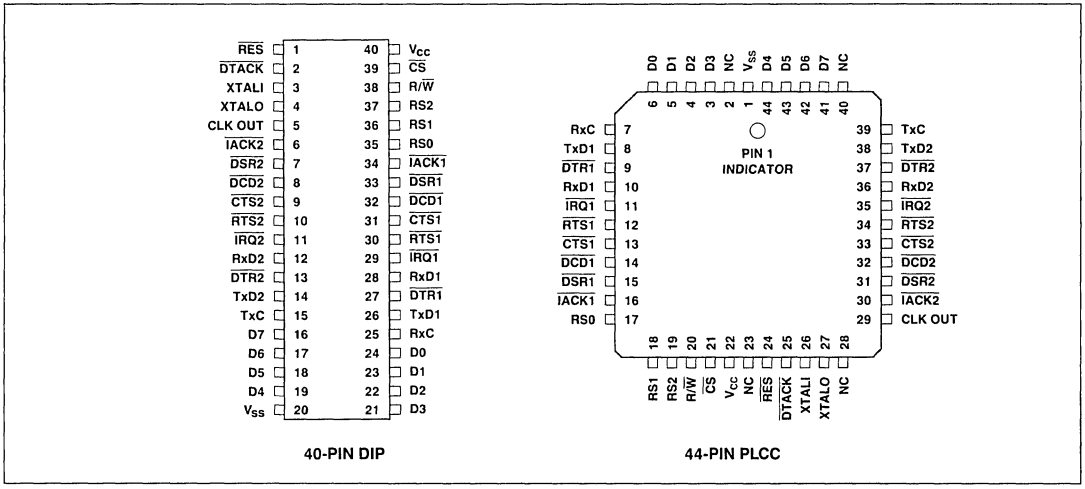


Figure 1. R68C552 Pin Assignments

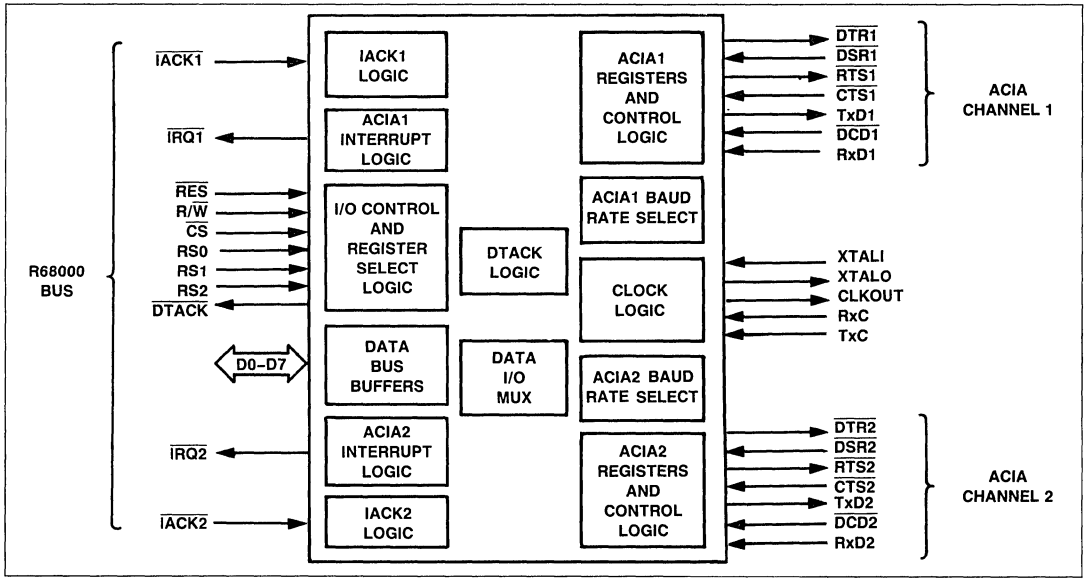


Figure 2. R68C552 DACIA Interface Signals

Table 1. DACIA Interface Signal Definitions

Signal	Pin No. DIP	Pin No. PLCC	I/O	Name/Description
Host Interface				
$\overline{RES}$	1	24	I	**Reset.** Active low input controlling the reset function. This signal must be driven low for a minimum of 4 μs for a valid reset to occur. It is driven high during normal operation.
R/$\overline{W}$	38	20	I	**Read/Write.** Input controlling the direction of data transfer. It is driven low during write cycles, and is driven high at all other times.
$\overline{CS}$	39	21	I	**Chip Select.** Active low input enabling data transfers between the host CPU and the DACIA. The DACIA latches register selects and the R/$\overline{W}$ input on the falling edge of $\overline{CS}$. It latches input data on the rising edge of $\overline{CS}$.
RS0-RS3	35-37	17-19	I	**Register Select.** Three inputs controlling access to the DACIA internal registers. Table 3 lists the coding for each register.
D0-D3 D4-D7	24-21 19-16	6-3 44-41	I/O	**Data Bus.** Eight bidirectional lines used to transfer data between the host and the DACIA. These lines output data during READ cycles when $\overline{CS}$ is low and they output the interrupt vector during INTERRUPT ACKNOWLEDGE cycles when $\overline{IACK1}$ or $\overline{IACK2}$ is low. At all other times, they are in the high impedence state.
$\overline{DTACK}$	2	25	O	**Data Transfer Acknowledge.** Active low open drain output generated in response to $\overline{CS}$, $\overline{IACK1}$ and $\overline{IACK2}$ during asynchronous data transfers. $\overline{DTACK}$ goes to the high impedence state when $\overline{CS}$, $\overline{IACK1}$ and $\overline{IACK2}$ are high.
$\overline{IRQ1}$ $\overline{IRQ2}$	29 11	11 35	O	**Interrupt Request.** Two active low, open-drain outputs from the interrupt control logic. These outputs are normally high. An $\overline{IRQ}$ line goes low when one of the flags of the associated ISR is set if the corresponding enable bit is set in the IER.
$\overline{IACK1}$ $\overline{IACK2}$	34 6	16 30	I	**Interrupt Acknowledge.** Two active low inputs indicating that an INTERRUPT ACKNOWLEDGE cycle is in progress. When an $\overline{IACK}$ goes low, the DACIA places the interrupt vector for the associated channel on the data bus and issues $\overline{DTACK}$.
Clock Interface				
XTALI XTALO	3 4	26 27	I O	**Crystal Input/Output.** One input and one output through which the reference signal for the internal clock oscillator is supplied. A parallel resonant crystal may be connected across the pins or a clock may be input at XTALI. When a clock is used, XTALO must be left open.
CLK OUT	5	29	O	**Clock Out.** A buffered output from the internal clock oscillator which is in phase with XTALI. This output may be used to drive the XTALI input of another DACIA. Therefore, several DACIA chips may be driven with one crystal.
RxC	25	7	I	**Receiver Clock.** Input for external 16x receiver clock.
TxC	15	39	I	**Transmitter Clock.** Input for external 16x transmitter clock.
Serial Channel Interface				
$\overline{DTR1}$ $\overline{DTR2}$	27 13	9 37	O	**Data Terminal Ready.** Two general purpose outputs which are set high upon reset. The output level is programmed by setting the appropriate bit in the associated Format Register (FR) high or low. The state of each $\overline{DTR}$ line is reflected by the $\overline{DTR}$ LVL bit in the associated Control Status Register (CSR).
$\overline{DSR1}$ $\overline{DSR2}$	33 7	15 31	I	**Data Set Ready.** Two general purpose inputs. An active transition sets the $\overline{DSR}$T bit in the Interrupt Enable Register (ISR). The $\overline{DSR}$ LVL bit in the associated CSR reflects the current state of a $\overline{DSR}$ line.
$\overline{RTS1}$ $\overline{RTS2}$	30 10	12 34	O	**Request To Send.** Two general purpose outputs which are set high upon reset. The output level is programmed by setting the appropriate bit in the associated FR high or low. The state of an $\overline{RTS}$ line is reflected by the $\overline{RTS}$ LVL bit in the associated CSR.
$\overline{CTS1}$ $\overline{CTS2}$	31 9	13 33	I	**Clear To Send.** The $\overline{CTS}$ control line inputs allow handshaking by the transmitters. When $\overline{CTS}$ is low, the data is transmitted continuously. When $\overline{CTS}$ is high, the Transmit Data Register Empty bit (TDRE) in the associated ISR is not set. The word presently in the Transmit Shift Register is sent normally. Any active transition on a $\overline{CTS}$ line sets the $\overline{CTS}$T bit in the appropriate ISR. The $\overline{CTS}$ LVL bit in the associated CSR reflects the current state of $\overline{CTS}$.
TxD1 TxD2	26 14	8 38	O	**Transmit Data.** The TxD outputs transfer serial non-return to zero (NRZ) data to the data communications equipment (DCE). The data is transferred, LSB first, at a rate determined by the baud rate generator or external clock.
$\overline{DCD1}$ $\overline{DCD2}$	32 8	14 32	I	**Data Carrier Detect.** Two general purpose inputs. An active transition sets the $\overline{DCD}$T bit in the appropriate ISR. The $\overline{DCD}$ LVL bit in the associated CSR reflects the current state of a $\overline{DCD}$ line.
RxD1 RxD2	28 12	10 36	I	**Receive Data.** The RxD inputs transfer serial NRZ data into the DACIA from the DCE, LSB first. The receiver baud rate is determined by the baud rate generator or external clock.
Power				
VCC	40	22	I	**DC Power Input.** 5.0V ± 5%.
VSS	20	1	I	**Power and Signal Reference.**

FUNCTIONAL DESCRIPTION

Figure 3 is a block diagram of the DACIA which consists of two asynchronous communications interface adapters with common microprocessor interface control logic and data bus buffers. The individual functional elements of the DACIA are described in the following paragraphs.

RESET LOGIC

The Reset Logic sets various internal registers, status bits and control lines to a known state. The $\overline{RES}$ input must be driven low for a minimum of 4 μs for a valid reset to occur. At this time, the IERs are set to $80, the RDRs and ACRs are cleared, and the compare mode is disabled. Also, the $\overline{DTR}$ and $\overline{RTS}$ outputs are driven high and the $\overline{CTS}$, $\overline{DCD}$ and $\overline{DSR}$ transition detect flags are cleared. No other bits are affected.

DATA BUS BUFFER

The Data Bus Buffer is a bidirectional interface between the data lines and the internal data bus. The state of the Data Bus Buffer is controlled by the I/O Control Logic and the Interrupt Logic. Table 2 summarizes the Data Bus Buffer states.

I/O CONTROL LOGIC

The I/O Control Logic controls data transfers between the Internal Registers and the Data Bus Buffer. Internal Register selection is determined by the Register Select inputs as shown in Table 3. When R/$\overline{W}$ is high and $\overline{CS}$ is low, data from the selected register is transferred from the internal data bus to the data lines and $\overline{DTACK}$ is asserted. When $\overline{CS}$ is high, the DACIA is deselected if the $\overline{IACK}$ inputs are high and the data lines are tri-stated.

INTERRUPT LOGIC

The interrupt logic causes the $\overline{IRQ}$ lines ($\overline{IRQ1}$ or $\overline{IRQ2}$) to go low when conditions are met that require the attention of the MPU. There are two registers (the Interrupt Enable Register and the Interrupt Status Register) involved in the control of interrupts in the DACIA. Corresponding bits in both registers must be set to cause an $\overline{IRQ}$.

When an $\overline{IACK}$ input goes low in response to an $\overline{IRQ}$, the following occurs if $\overline{CS}$ and R/$\overline{W}$ are high: D0 goes low if the $\overline{IRQ}$ is generated by TDR empty or RDR full. D0 goes high for all other interrupt sources. TDRE and RDRF interrupts have priority over all other interrupt sources. D1 goes low when the interrupt request is from Channel 1. It goes high if the $\overline{IRQ}$ is from Channel 2. D2 through D7 outputs the Interrupt Vector Number stored in bits 2 through 7 of the Auxiliary Control Register. $\overline{DTACK}$ is asserted.

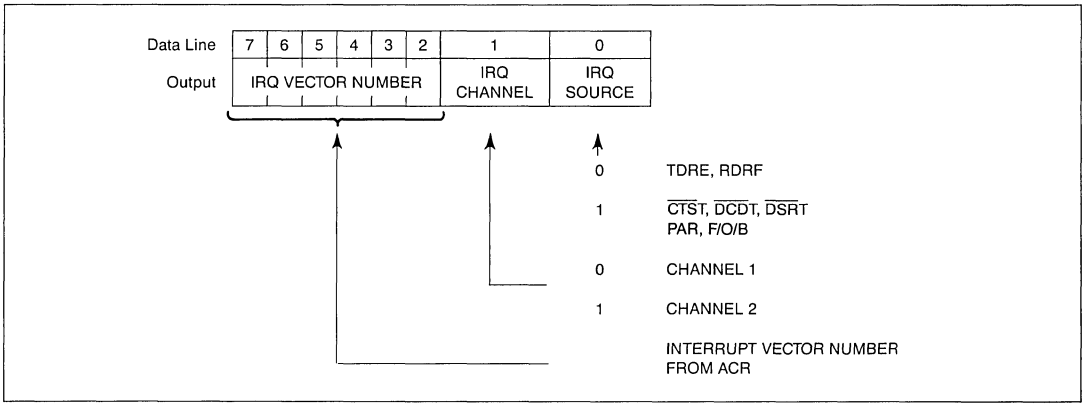
CLOCK OSCILLATOR LOGIC

The internal clock oscillator supplies the time base for the baud rate generator. The oscillator can be driven by a crystal or an external clock.

The baud rate generator may be disabled by connecting XTALI to ground and leaving XTALO open. When this is done, a transmitter times 16 clock must be input at TxC, a receiver times 16 clock must be input at RxC and the Control Registers must be programmed to select TxC and RxC clocks.

Table 2. Data Bus Buffer Summary

Control Signals				Data Bus Buffer State
R/$\overline{W}$	$\overline{CS}$	$\overline{IACK1}$	$\overline{IACK2}$	
L	L	L	L	Illegal Mode — Tri-State
L	L	L	H	Illegal Mode — Tri-State
L	L	H	L	Illegal Mode — Tri-State
L	L	H	H	Write Mode — Tri-State
L	H	L	L	Illegal Mode — Tri-State
L	H	L	H	Illegal Mode — Tri-State
L	H	H	L	Illegal Mode — Tri-State
L	H	H	H	Tri-State
H	L	L	L	Illegal Mode — Output $0F
H	L	L	H	Illegal Mode — Output $0F
H	L	H	L	Illegal Mode — Output $0F
H	L	H	H	Read Mode — Output Data
H	H	L	L	Illegal Mode — Output $0F
H	H	L	H	Output IRQ Vector 1
H	H	H	L	Output IRQ Vector 2
H	H	H	H	Tri-State



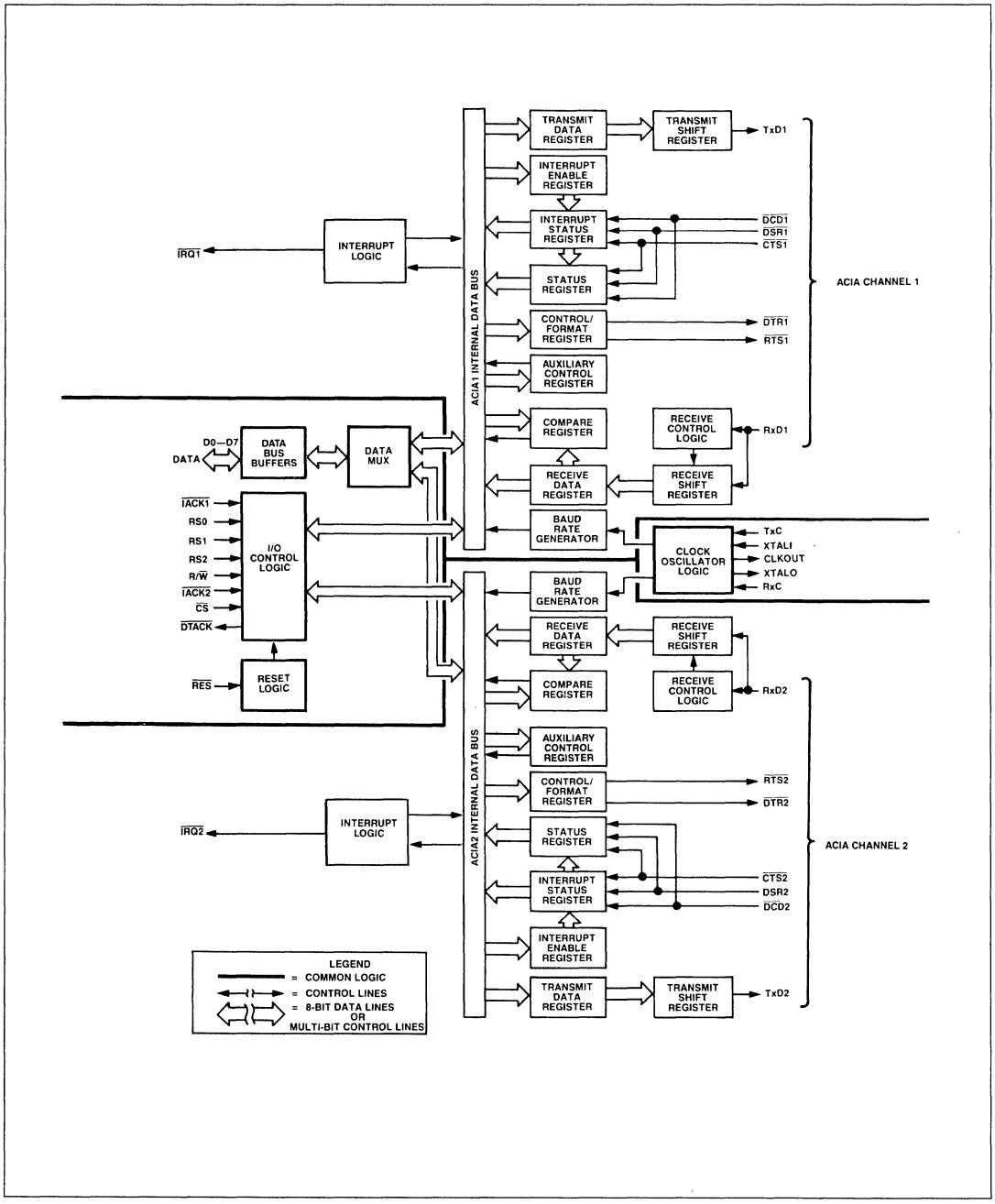


Figure 3. DACIA Block Diagram

Table 3. DACIA Register Selection

Register Select Lines				Register Accessed			
				Write		Read	
HEX	RS2	RS1	RS0	Symbol	Name	Symbol	Name
0	L	L	L	IER1	Interrupt Enable Register 1	ISR1	Interrupt Status Register 1
1	L	L	H	CR1	Control Register 1[1]	CSR1	Control Status Register 1
				FR1	Format Register 1[2]		
2	L	H	L	CDR1	Compare Data Register 1[3]		Not Used
				ACR1	Auxiliary Control Register 1[4]		
3	L	H	H	TDR1	Transmit Data Register 1	RDR1	Receive Data Register 1
4	H	L	L	IER2	Interrupt Enable Register 2	ISR2	Interrupt Status Register 2
5	H	L	H	CR2	Control Register 2[1]	CSR2	Control Status Register 2
				FR2	Format Register 2[2]		
6	H	H	L	CDR2	Compare Data Register 2[3]		Not Used
				ACR2	Auxiliary Control Register 2[4]		
7	H	H	H	TDR2	Transmit Data Register 2	RDR2	Receive Data Register 2

Notes:
1. D7 must be set low to write to the Control Registers.
2. D7 must be set high to write to the Format Registers.
3. Control Register bit 6 must be set to 0 to access the Compare Register.
4. Control Register bit 6 must be set to 1 to access the Auxiliary Control Register.

SERIAL DATA CHANNELS

Two independent serial data channels are available for the full duplex (simultaneous transmit and receive) transfer of asynchronous frames. Separate internal registers are provided for each channel for the selection of frame parameters (number of bits per character, parity options, etc.), status flags, interrupt control and handshake. The asynchronous frame format is shown in Figure 4.

Transmit data from the host system is loaded into the Transmit Data Register. From there, it is transferred to the Transmit Shift Register where it is shifted, LSB first, onto the TxD line. All transmissions begin with a start bit and end with the user selected number of stop bits. A parity bit is transmitted before the stop bit(s) if parity is enabled.

Receive data is shifted into the Receive Shift Register from the associated RxD line. Start and stop bits are stripped from the frame and the data is transferred to the Receive Data Register. Parity bits may be discarded or stored in the ISR.

Five I/O lines are provided for each channel for handshake with the data communications equipment (DCE). Four of these signals ($\overline{RTS}$, $\overline{DTR}$, $\overline{DSR}$ and $\overline{DCD}$) are general purpose inputs or outputs. The fifth signal, $\overline{CTS}$, enables/disables the transmitter. When $\overline{CTS}$ is high and the Transmit Shift Register is empty, the transmitter (except for Echo Mode) is inhibited. When $\overline{CTS}$ is low, the transmitter is enabled.

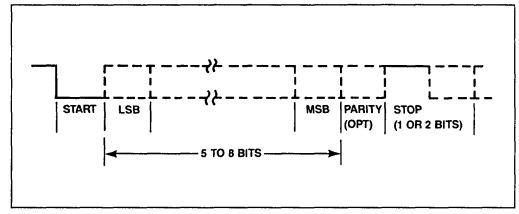


Figure 4. Asynchronous Frame Format

INTERNAL REGISTERS

The DACIA contains ten control registers and four status registers in addition to the transmit and receive registers. The Control Registers provide for control of frame parameters, baud rate, interrupt generation, handshake lines, transmission and reception. The status registers provide status information on transmit and receive registers, error conditions and interrupt sources. Table 4 summarizes the bit definitions of these registers. A detailed description follows.

Table 4. Register Formats

Register Select (Hex)	Register	R/$\overline{W}$	Bit 7	6	5	4	3	2	1	0	Reset Value 76543210
0 4	ISR1 ISR2	R	ANY BIT SET	TDRE	$\overline{CTS}$T	$\overline{DCD}$T	$\overline{DSR}$T	PAR	F/O/B	RDRF	1 - 00000 -
0 4	IER1 IER2	W	CLR/SET BITS	TDRE IE	$\overline{CTS}$T IE	$\overline{DCD}$T IE	$\overline{DSR}$T IE	PAR IE	F/O/B IE	RDRF IE	- 0000000
1 5	CSR1 CSR2	R	FE	TUR	$\overline{CTS}$ LVL	$\overline{DCD}$ LVL	$\overline{DSR}$ LVL	BRK	$\overline{DTR}$ LVL	$\overline{RTS}$ LVL	1 - - - - 011
1 5	CR1 CR2	W	0	CDR/ ACR	STOP BITS	ECHO	BIT RATE SEL				0 - - - - - - -
1 5	FR1 FR2	W	1	DATA BITS		PAR SEL		PAR EN	$\overline{DTR}$ CNTL	$\overline{RTS}$ CNTL	1 - - - - - - -
2 6	CDR1 CDR2	W (CR6 = 0)	COMPARE DATA								- - - - - - - -
2 6	ACR1 ARC2	W (CR6 = 1)	IRQ VECTOR NUMBER						TRNS BRK	PAR ERR/ST	- - - - - - 00
3 7	RDR1 RDR2	R	RECEIVE DATA REGISTER								00000000
3 7	TDR1 TDR2	W	TRANSMIT DATA REGISTER								- - - - - - - -

INTERRUPT STATUS REGISTERS (ISR1, ISR2)

The Interrupt Status Registers are read-only registers indicating the status of each interrupt source. Bits 6 through 0 are set when the indicated $\overline{IRQ}$ condition has occurred. Bit 7 is set to a 1 when any $\overline{IRQ}$ source bit is set, or if Echo Mode is disabled, when $\overline{CTS}$ is high.

7	6	5	4	3	2	1	0
ANY BIT SET	TDRE	$\overline{CTST}$	$\overline{DCDT}$	$\overline{DSRT}$	PAR	F/O/B	RDRF

Address = 0,4 Reset Value = 1 - 00000 -

Bit 7 **Any Bit Set**
1 Any bit (6 through 0) has been set to a 1 or $\overline{CTS}$ is high with echo disabled
0 No bits have been set to a 1 or echo is enabled

Bit 6 **Transmit Data Register Empty (TDRE)**
1 Transmit Data Register is empty and $\overline{CTS}$ is low
0 Transmit Data Register is full or $\overline{CTS}$ is high

Bit 5 **Transition On $\overline{CTS}$ Line ($\overline{CTST}$)**
1 A positive or negative transition has occurred on $\overline{CTS}$
0 No transition has occurred on $\overline{CTS}$, or ISR has been Read

Bit 4 **Transition On $\overline{DCD}$ Line ($\overline{DCDT}$)**
1 A positive or negative transition has occurred on $\overline{DCD}$
0 No transition has occurred on $\overline{DCD}$, or ISR has been Read

Bit 3 **Transition On $\overline{DSR}$ Line ($\overline{DSRT}$)**
1 A positive or negative transition has occurred on $\overline{DSR}$
0 No transition has occurred on $\overline{DSR}$, or ISR has been Read

Bit 2 **Parity Status (PAR)**
ACR bit 0 = 0
1 A parity error has occurred in received data
0 No parity error has occurred, or the Receive Data Register (RDR) has been Read
ACR bit 0 = 1
1 Parity bit = 1
0 Parity bit = 0

Bit 1 **Frame Error, Overrun, Break**
1 A framing error, receive overrun, or receive break has occurred or has been detected
0 No error, overrun, break has occurred or RDR has been Read

Bit 0 **Receive Data Register Full (RDRF)**
1 Receive Data Register is full
0 Receive Data Register is empty

INTERRUPT ENABLE REGISTERS (IER1, IER2)

The Interrupt Enable Registers are write-only registers that enable/disable the $\overline{IRQ}$ sources. $\overline{IRQ}$ sources are enabled by writing to an IER with bit 7 set to a 1 and the bit for every $\overline{IRQ}$ source to be enabled set to a 1. $\overline{IRQ}$ sources are disabled by writing to an IER with bit 7 reset to a 0 and the bit for every source to be disabled set to a 1. Any source bit reset to 0 is unaffected and remains in its original state. Thus, writing $7F to an IER disables all of that channel's interrupts and writing an $FF to an IER enables all of that channel's interrupts.

7	6	5	4	3	2	1	0
SET BITS	TDRE IE	$\overline{CTST}$ IE	$\overline{DCDT}$ IE	$\overline{DSRT}$ IE	PAR IE	F/O/B IE	RDRF IE

Address = 0,4 Reset Value = - 0000000

Bit 7 **Enable/Disable**
1 Enable selected IRQ source
0 Disable selected IRQ source

Bits 0-6
1 Select for enable/disable
0 No change

CONTROL STATUS REGISTERS (CSR1, CSR2)

The Control Status Registers are read-only registers that provide I/O status and error condition information. A CSR is normally read after an IRQ has occurred to determine the exact cause of the interrupt condition.

7	6	5	4	3	2	1	0
FE	TUR	$\overline{CTS}$ LVL	$\overline{DCD}$ LVL	$\overline{DSR}$ LVL	BRK	$\overline{DTR}$ LVL	$\overline{RTS}$ LVL

Address = 1,5 Reset Value = 1 - - - - 011

Bit 7 **Framing Error (FE)**
1 A framing error occurred in receive data
0 No framing error occurred, or the RDR was read

Bit 6 **Transmitter Underrun (TUR)**
1 Transmit Shift Register is empty and TDRE is set
0 Transmitter Shift Register is not empty

Bit 5 **$\overline{CTS}$ Level ($\overline{CTS}$ LVL)**
1 $\overline{CTS}$ line is high
0 $\overline{CTS}$ line is low

Bit 4 **$\overline{DCD}$ Level ($\overline{DCD}$ LVL)**
1 $\overline{DCD}$ line is high
0 $\overline{DCD}$ line is low

Bit 3 **$\overline{DSR}$ Level ($\overline{DSR}$ LVL)**
1 $\overline{DSR}$ line is high
0 $\overline{DSR}$ line is low

Bit 2 **Receive Break (BRK)**
1 A Receive Break has occurred
0 No Receive Break occurred, or RDR was read

Bit 1 **$\overline{DTR}$ Level ($\overline{DTR}$ LVL)**
1 $\overline{DTR}$ line is high
0 $\overline{DTR}$ line is low

Bit 0 **$\overline{RTS}$ Level ($\overline{RTS}$ LVL)**
1 $\overline{RTS}$ line is high
0 $\overline{RTS}$ line is low

CONTROL REGISTERS (CR1, CR2)

The Control Registers are write-only registers. They control access to the Auxiliary Control Register and the Compare Data Register. They select the number of stop bits, control Echo Mode, and select the data rate.

(Accessed when Bit 7 = 0)

7	6	5	4	3 2 1 0
0	CDR/ACR	STOP BITS	ECHO	BAUD RATE SEL

Address = 1,5 Reset Value = 0 - - - - - - -

Bit 7 **Control or Format Register**
0 Access Control Register

Bit 6 **CDR/ACR**
1 Access the Auxiliary Control Register (ACR)
0 Access the Compare Data Register (CDR)

Bit 5 **Number of Stop Bits Per Character**
1 Two stop bits
0 One stop bit

Bit 4 **Echo Mode Selection**
1 Echo Mode enabled
0 Echo Mode disabled

Bits 3-0 **Baud Rate Selection**

3	2	1	0	(bits per second with 3.6864 MHz crystal)
0	0	0	0	50
0	0	0	1	109.2
0	0	1	0	134.58
0	0	1	1	150
0	1	0	0	300
0	1	0	1	600
0	1	1	0	1200
0	1	1	1	1800
1	0	0	0	2400
1	0	0	1	3600
1	0	1	0	4800
1	0	1	1	7200
1	1	0	0	9600
1	1	0	1	19200
1	1	1	0	38400
1	1	1	1	External TxC and RxC X16 Clocks

FORMAT REGISTERS (FR1, FR2)

The Format Registers are write-only registers. They select the number of data bits per character and parity generation/checking options. They also control $\overline{RTS}$ and $\overline{DTR}$.

(Accessed when Bit 7 = 1)

7	6 5	4 3	2	1	0
1	DATA BITS	PAR SEL	PAR EN	$\overline{DTR}$ CNTL	$\overline{RTS}$ CNTL

Address = 1,5 Reset Value = 1 - - - - - - -

Bit 7 **Control or Format Register**
1 Access Format Register

Bits 6-5 **Number of Data Bits Per Character**

6	5	
0	0	5
0	1	6
1	0	7
1	1	8

Bits 4-3 **Parity Mode Selection**

4	3	
0	0	Odd Parity
0	1	Even Parity
1	0	Mark in Parity bit
1	1	Space in Parity bit

Bit 2 **Parity Enable**
1 Parity as specified by bits 4-3
0 No Parity

Bit 1 **$\overline{DTR}$ Control**
1 Set $\overline{DTR}$ high
0 Set $\overline{DTR}$ low

Bit 0 **$\overline{RTS}$ Control**
1 Set $\overline{RTS}$ high
0 Set $\overline{RTS}$ low

COMPARE DATA REGISTERS (CDR1, CDR2)

The Compare Data Registers are write-only registers which can be accessed when CR bit 6 = 0. By writing a value into the CDR, the DACIA is put in the compare mode. In this mode, setting of the RDRF bit is inhibited until a character is received which matches the value in the CDR. The next character is then received and the RDRF bit is set. The receiver will now operate normally until the CDR is again loaded.

(Control Register bit 6 = 0)

7	6	5	4	3	2	1	0
COMPARE DATA							

Address = 2,6 Reset Value = --------

AUXILIARY CONTROL REGISTERS (ACR1, ACR2)

The Auxiliary Control Registers are write-only registers. Bits 7-2 hold the user selected interrupt vector number to be output on data lines 7-2 during interrupt acknowledge. Bit 1 causes the transmitter to transmit a BREAK. Bit 0 determines whether parity error or the parity bit is displayed in ISR bit 2.

(Control Register bit 6 = 1)

7	6	5	4	3	2	1	0
IRQ VECTOR ADDRESS						TRNS BRK	PAR ERR/ST

Address = 2,6 Reset Value = ------00

Bits 7-2	IRQ Vector Address
Bit 1	**Transmit Break (TRNS BRK)**
1	Transmit continuous Break
0	Normal transmission
Bit 0	**Parity Error/State (PAR ERR/ST)**
1	Send value of parity bit to ISR bit 2 (Address Recognition mode)
0	Send Parity Error status to ISR bit 2

RECEIVE DATA REGISTERS (RDR1, RDR2)

The Receive Data Registers are read-only registers which are loaded with the received data character of each frame. Start bits, stop bits and parity bits are stripped off of incoming frames before the data is transferred from the Receive Shift Register to the Receive Data Register. For characters of less than eight bits, the unused bits are the high order bits which are set to 0.

MSB **LSB**

7	6	5	4	3	2	1	0
RECEIVE DATA							

Address = 3,7 Reset Value = 00000000

TRANSMIT DATA REGISTERS (TDR1, TDR2)

The Transmit Data Registers are write-only registers which are loaded from the CPU with data to be transmitted. For data characters of less than eight bits, the unused bits are the high order bits which are "don't care".

MSB **LSB**

7	6	5	4	3	2	1	0
TRANSMIT DATA							

Address = 3,7 Reset Value = --------

OPERATION

TERMINATION OF UNUSED INPUTS

Noise on floating inputs can affect chip operation. All unused inputs must be terminated. If unused, $\overline{IACK1}$ and $\overline{IACK2}$ must be tied high. If the baud rate generator is bypassed, XTALI must be connected to ground (XTALO is an output and must be left open). If the external clock mode is not used, RxC and TxC may be tied either to +5V or to ground. If the handshake inputs are not needed, the $\overline{CTS}$ inputs should be tied low to enable the transmitters. The $\overline{DCD}$ and $\overline{DSR}$ inputs may either be tied high or low.

RESET INITIALIZATION

During power on initialization, all readable registers should be read to assure that the status registers are initialized. Specifically, the RDRF bit of the Interrupt Status Registers is not initialized by reset. The Receiver Data Registers must be read to clear this bit.

BAUD RATE CLOCK OPTIONS

The receiver and transmitter clocks may be supplied either by the internal Baud Rate Generator or by user supplied external clocks. Both channels may use the same clock source or one may use the Baud Rate Generator and the other channel external clocks. If both channels use the Baud Rate Generator, each channel may have a different bit rate. The options are shown in Figure 5.

An internal clock oscillator supplies the time base for the Baud Rate Generator. The oscillator can be driven by a crystal or an external clock.

If the on-chip oscillator is driven by a crystal, a parallel resonant crystal is connected between the XTALI and XTALO pins. The equivalent oscillator circuit is shown in Figure 6.

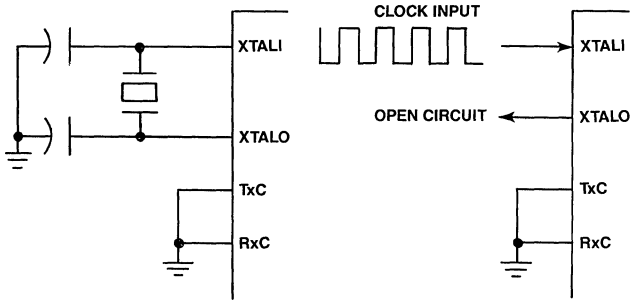
A parallel resonant crystal is specified by its load capacitance and series resonant resistance. For proper oscillator operation, the load capacitance (C_L), series resistance (R_s) and the crystal resonant frequency (F) must meet the following two relations:

$$(C + 2) = 2C_L \quad \text{or} \quad C = 2C_L - 2$$

$$R_s \leq R_{smax} = \frac{2 \times 10^6}{(FC_L)^2}$$

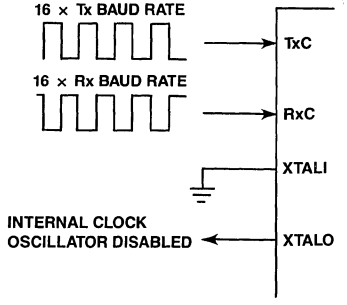
where: F is in MHz; C and C_L are in pF; R is in ohms.

To select a parallel resonant crystal for the oscillator, first select the load capacitance from a crystal manufacturer's catalog. Next, calculate R_{smax} based on F and C_L. The selected crystal must have a R_s less than the R_{smax}.



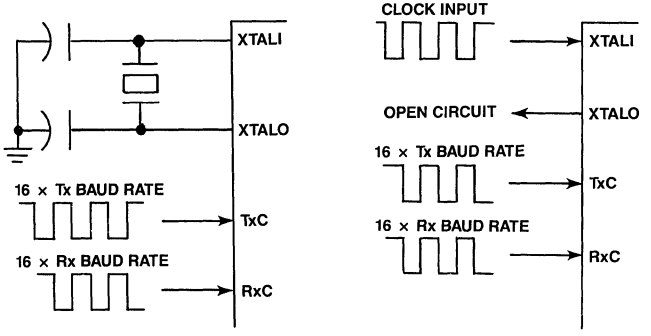
- Baud rate determined by XTALI frequency and 1 of 15 divisors selected in CR1 and CR2. CR1 and CR2 must not be set to all ones.
- Channel 1 baud rate may be different from channel 2 baud rate.
- Receiver baud rate must be the same as transmitter baud rate.

A. Both Channels Use Internal Baud Rate Generator



- Transmitter baud rate 1/16 TxC input frequency.
- Receiver baud rate 1/16 RxC input frequency.
- Channel 1 baud rate is the same as channel 2 baud rate.
- Receiver baud rate may be different from transmitter baud rate.
- Bits 3-0 of CR1 and CR2 must be set to all ones.

B. Both Channels Use External Clocks



- Channel 1 baud rate may be different from channel 2 baud rate.
- Transmitter baud rate may be different from receiver baud rate on channel using external clock.

C. One Channel Uses Internal Baud Rate Generator;
One Channel Uses External Clocks

Figure 5. Baud Rate Clock Options

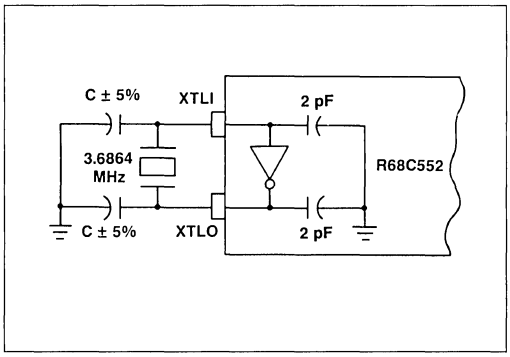


Figure 6.

For example, if C_L = 22 pF for a 3.6864 MHz parallel resonant crystal, then

$C = (2 \times 22) - 2 = 42$ pF (use standard value of 43 pF)

The series resistance of the crystal must be less than

$$R_{smax} = \frac{2 \times 10^6}{(3.6864 \times 22)^2} = 304 \text{ ohms}$$

If the on-chip oscillator is driven by an external clock, the clock is input at XTALI and XTALO is left open.

An internal counter/divider circuit divides the frequency input at XTALI by the divisor selected in bits 3 through 0 of the Control Registers. Table 5 lists the divisors that may be selected and shows the bit rates generated with a 3.6864 MHz crystal or clock input. Other bit rates may be generated by changing the clock or crystal frequency. However, the input frequency must not exceed 4 MHz.

For external clock operation, a transmitter times 16 clock must be supplied at TxC and a receiver times 16 clock must be input at RxC. Since there are separate receiver and transmitter clock inputs, the receiver data rate may be different from the transmitter data rate.

4

Table 5. Baud Rate Generator Divisor Selection

Control Register Bits				Divisor Selected For The Internal Counter	Baud Rate Generated With 3.6864 MHz Crystal or Clock	Baud Rate Generated* With a Crystal or Clock of Frequency (f)
3	2	1	0			
0	0	0	0	73,728	$(3.6864 \times 10^6)/73,728 = 50$	f/73,728
0	0	0	1	33,538	$(3.6864 \times 10^6)/33,538 = 109.92$	f/33,538
0	0	1	0	27,408	$(3.6864 \times 10^6)/27,408 = 134.58$	f/27,408
0	0	1	1	24,576	$(3.6864 \times 10^6)/24,576 = 150$	f/24,576
0	1	0	0	12,288	$(3.6864 \times 10^6)/12,288 = 300$	f/12,288
0	1	0	1	6,144	$(3.6864 \times 10^6)/6,144 = 600$	f/6,144
0	1	1	0	3,072	$(3.6864 \times 10^6)/3,072 = 1,200$	f/3,072
0	1	1	1	2,048	$(3.6864 \times 10^6)/2,048 = 1,800$	f/2,048
1	0	0	0	1,536	$(3.6864 \times 10^6)/1,536 = 2,400$	f/1,536
1	0	0	1	1,024	$(3.6864 \times 10^6)/1,024 = 3,600$	f/1,024
1	0	1	0	768	$(3.6864 \times 10^6)/768 = 4,800$	f/768
1	0	1	1	512	$(3.6864 \times 10^6)/512 = 7,200$	f/512
1	1	0	0	384	$(3.6864 \times 10^6)/384 = 9,600$	f/384
1	1	0	1	192	$(3.6864 \times 10^6)/192 = 19,200$	f/192
1	1	1	0	96	$(3.6864 \times 10^6)/96 = 38,400$	f/96
1	1	1	1	16	Transmitter Baud Rate = TxC/16	Receiver Baud Rate = RxC/16

*Baud Rate = $\frac{\text{Frequency}}{\text{Divisor}}$

CONTINUOUS DATA TRANSMIT

In the normal operating mode, the TDRE bit in the ISR signals the MPU that the DACIA is ready to accept the next data word. An $\overline{IRQ}$ occurs if the corresponding TDRE IRQ enable bit is set in the IER. The TDRE bit is set at the beginning of the start bit. When the MPU writes a word to the TDR the TDRE bit is cleared. In order to maintain continuous transmission the TDR must be loaded before the stop bit(s) are ended. Figure 7 shows the relationship between $\overline{IRQ}$ and TxD for the Continuous Data Transmit mode.

CAUTION:

When the Baud Rate Generator is the clock source, writing to the Format or Control Register of a channel with an active transmitter can result in loss of data. Do not write to the Control or Format Register when the transmitter is shifting out data. This precaution does not apply to channels using the external clock option, i.e., TxC.

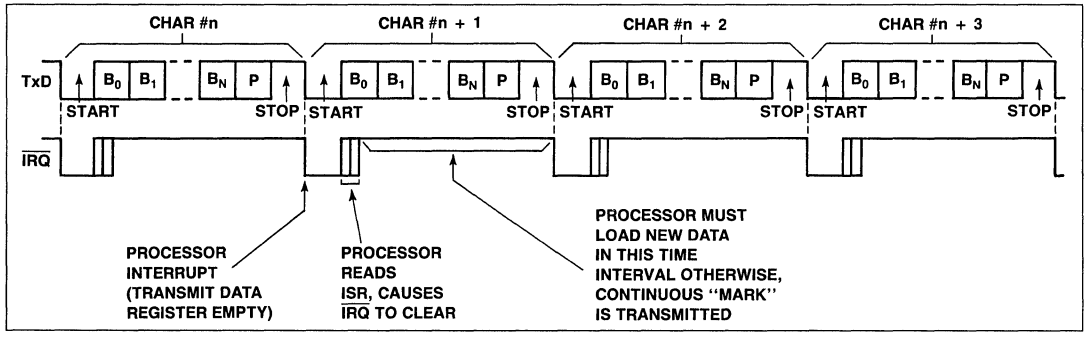


Figure 7. Continuous Data Transmit

TRANSMIT UNDERRUN CONDITION

If the MPU is unable to load the TDR before the last stop bit is sent, the TxD line goes to the MARK condition and the underrun flag (TUR) is set. This condition persists until the TDR is loaded with a new word. Figure 8 shows the relation between $\overline{IRQ}$ and TxD for the Transmit Underrun Condition.

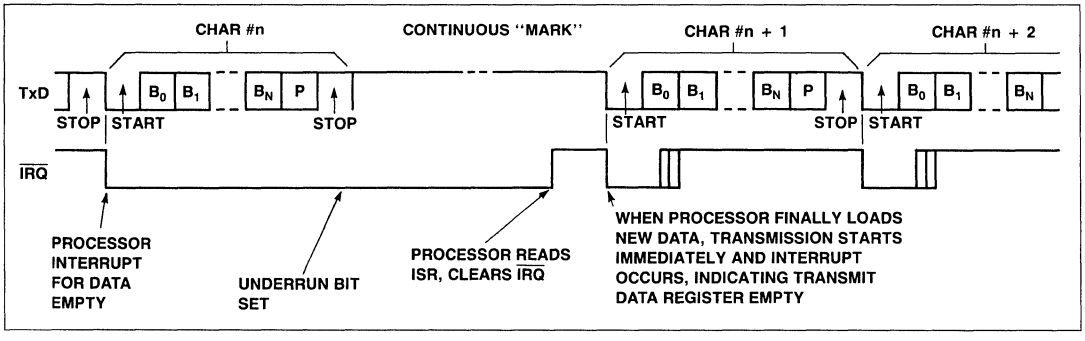


Figure 8. Transmit Underrun Condition Relationship

TRANSMIT BREAK CHARACTER

A BREAK may be transmitted by setting bit 1 of the ACR (Transmit Break bit) to a 1. The BREAK is transmitted after the character in the Transmit Shift Register is sent. If there is a character in the Transmit Data Register, it will be transmitted after the BREAK is terminated. The Transmit Break bit must remain set for at least one character time to assure that a proper BREAK is transmitted. If the Transmit Break bit is cleared before one character time of BREAK has been transmitted, the BREAK will be terminated after one character time has elapsed. If the Transmit Break bit is cleared after one character time of BREAK has been transmitted, the BREAK will be terminated immediately. Figure 9 shows the relationship of TxD, $\overline{IRQ}$ and ACR bit 1 for various BREAK options.

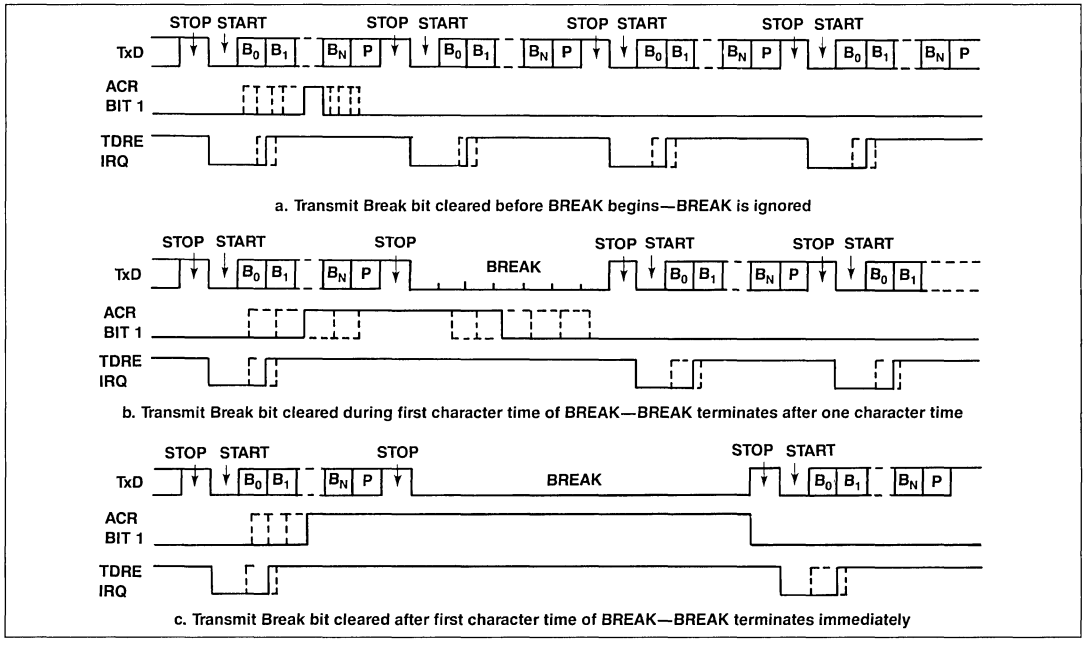


Figure 9. Transmit BREAK

EFFECTS OF $\overline{CTS}$ ON TRANSMITTER

The $\overline{CTS}$ control line controls the transmission of data or the handshaking of data to a "busy" device (such as a printer). When the $\overline{CTS}$ line is low, the transmitter operates normally. A high condition inhibits the TDRE bit in the ISR from becoming set. Transmission of the word currently in the shift register is completed but any word in the TDR is held until $\overline{CTS}$ goes low.

Any transition on $\overline{CTS}$ sets bit 5 ($\overline{CTST}$) of the ISR. A high on $\overline{CTS}$ forces bit 6 (TDRE) of the ISR to a 0. Bit 7 of the ISR also goes to a 1 when $\overline{CTS}$ is high, if Echo Mode is disabled. Thus, when the ISR is $80, it means that $\overline{CTS}$ is high and no interrupt source requires service. A processor interrupt will not be generated under these circumstances, but an ISR polling routine should accommodate this.

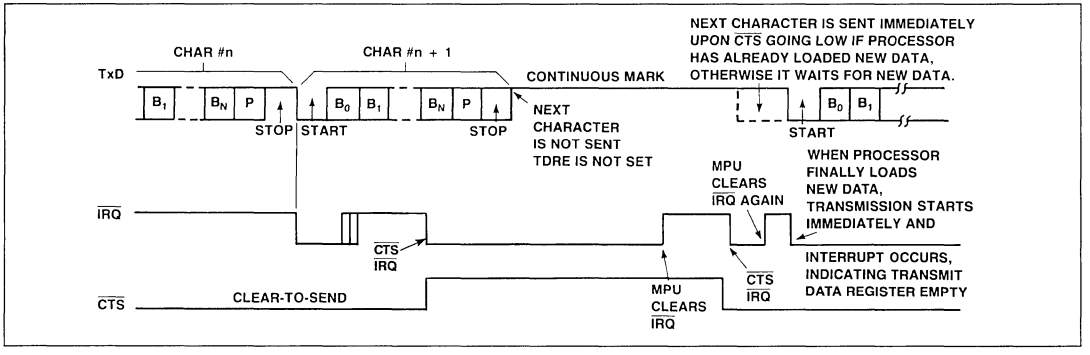


Figure 10. Effects of $\overline{CTS}$ on Transmitter

ECHO MODE TIMING

In the Echo Mode, the TxD line re-transmits the data received on the RxD line, delayed by 1/2 of a bit time. An internal underrun mode must occur before Echo Mode will start transmitting. In normal transmit mode if TDRE occurs (indicating end of data) an underflow flag would be set and continuous Mark transmitted. If Echo is initiated, the underflow flag will not be set at end of data and continuous Mark will not be transmitted. Figure 11 shows the relationship of RxD and TxD for Echo Mode.

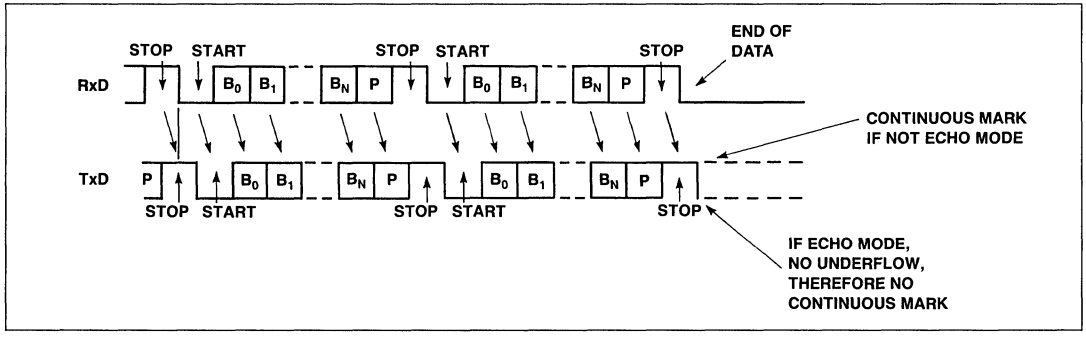


Figure 11. Echo Mode Timing

CONTINUOUS DATA RECEIVE

The normal receive mode sets the RDRF bit in the ISR when the DACIA channel has received a full data word. This occurs at about the 9/16 point through the stop bit. The processor must read the RDR before the next stop bit, or an overrun error occurs. Figure 12 shows the relationship between $\overline{IRQ}$ and RxD for the continuous Data Receive mode.

CAUTION:

When the Baud Rate Generator is the clock source, writing to the Control or Format Registers of a channel with an active receiver can result in loss of data. Do not write to the Control or Format Registers when the receiver is shifting in data. This precaution is not necessary on channels using the external clock option, i.e., RxC.

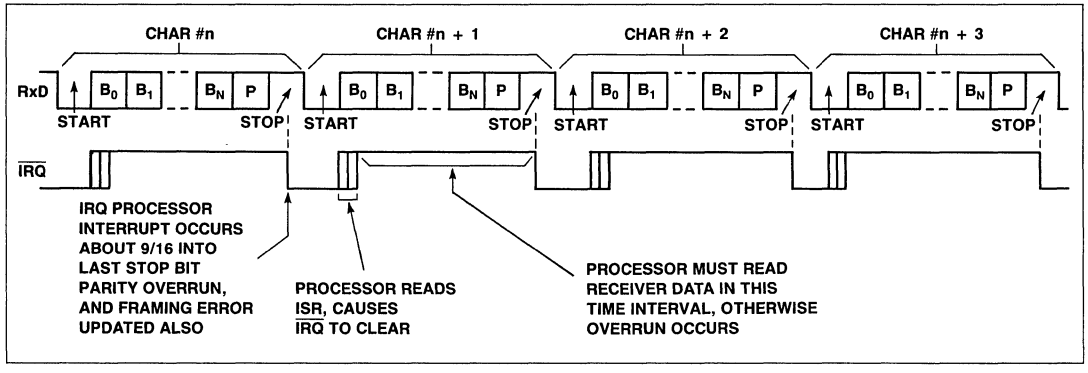


Figure 12. Continuous Data Receive

EFFECTS OF OVERRUN ON RECEIVER

If the processor does not read the RDR before the stop bit of the next word, an overrun error occurs, the overrun bit is set in the ISR, and the new data word is not transferred to the RDR. The RDR contains the last word not read by the MPU and all following data is lost. The receiver will return to normal operation when the RDR is read. Figure 13 shows the relationship of $\overline{IRQ}$ and RxD when overrun occurs.

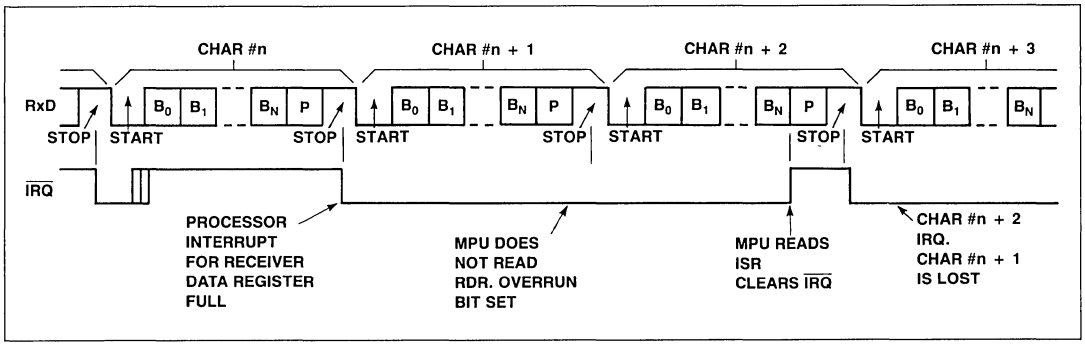


Figure 13. Effects of Overrun on Receiver

RECEIVE BREAK CHARACTER

In the event that a Break character is received by the receiver, the Break bit is set. The receiver does not set the RDRF bit and remains in this state until a stop bit is received. At this time the next character is to be received normally. Figure 14 shows the relationship of $\overline{IRQ}$ and RxD for a Receive Break Character.

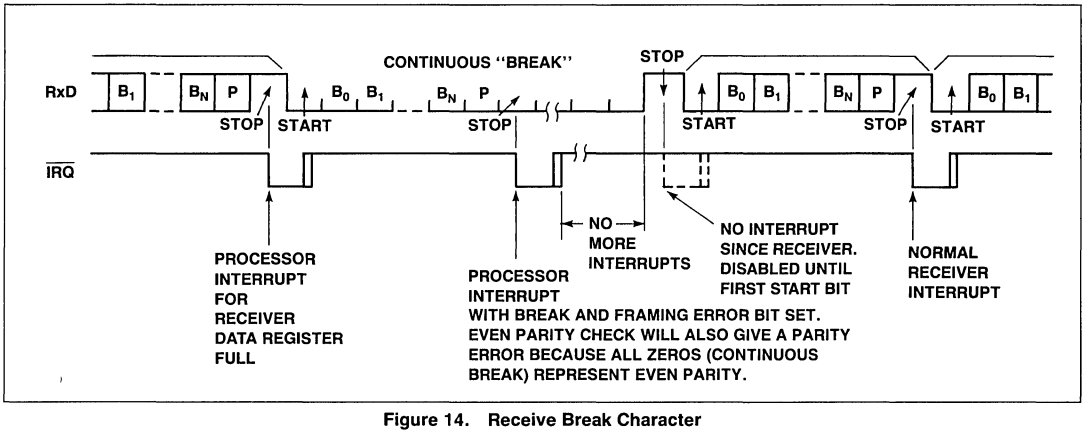


Figure 14. Receive Break Character

FRAMING ERROR

Framing error is caused by the absence of stop bit(s) on received data. The framing error bit is set when the RDRF bit is set. Subsequent data words are tested separately, so the status bit always reflects the last data word received. Figure 15 shows the relationship of $\overline{IRQ}$ and RxD when a framing error occurs.

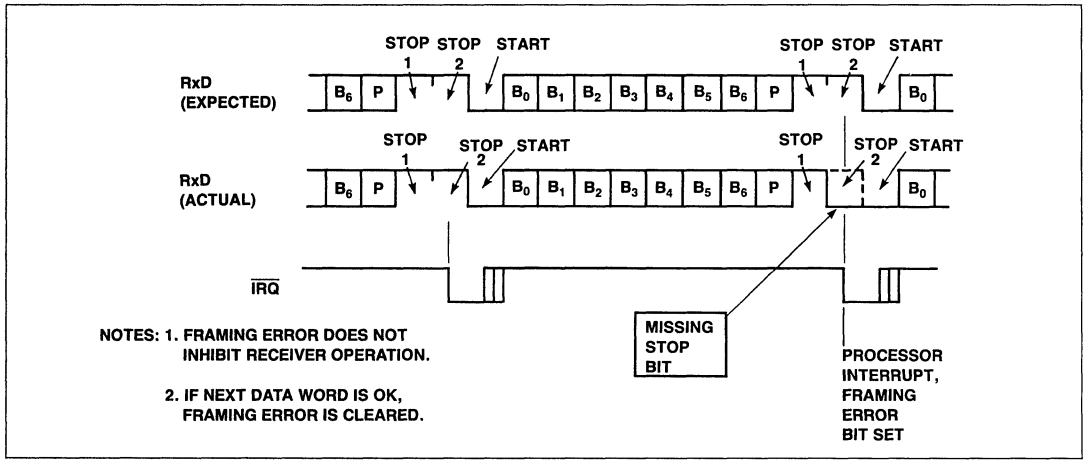


Figure 15. Framing Error

PARITY ERROR DETECT/ADDRESS FRAME RECOGNITION

The Parity Status bit (ISR bit 2) may be programmed to indicate parity errors (ACR bit 0 = 0) or to display the parity bit received (ACR bit 0 = 1).

In applications where parity checking is used, one of the parity checking modes is enabled by setting bits 2, 3 and 4 of the Format Register to the desired option and bit 0 of the Auxiliary Control Register is reset to 0. Then, when the RDRF bit (bit 0) is set in the ISR, the PAR bit (bit 2) will be set when a parity error is detected.

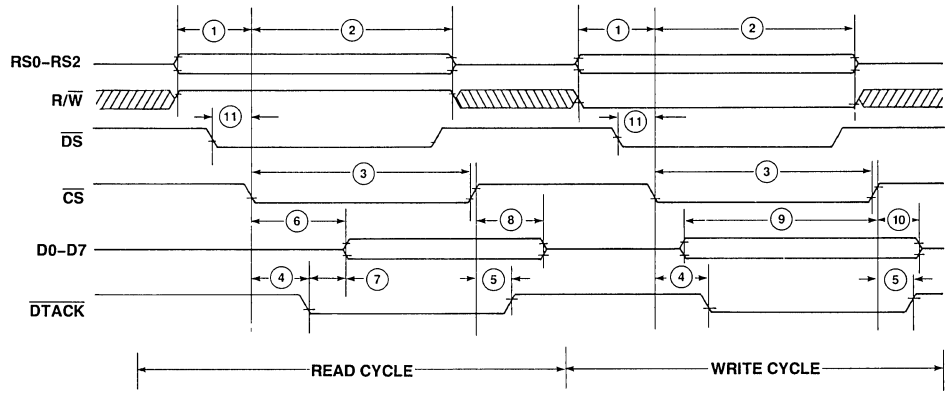
In multi-drop applications, the parity bit is used as an address/data flag. It is set to 1 for address frames and is 0 on data frames. For this type of operation, bit 0 of the ACR is set to a 1 and bits 2, 3 and 4 of the FR select a parity checking mode. Then, ISR bit 2 will be set to a 1 by incoming address frames and it will be a 0 on data frames.

COMPARE MODE

The Compare Mode is automatically enabled, i.e., the channel is put to sleep, whenever data is written to the Compare Data Register. NOTE: Bit 6 of the Control Register must be set to 0 to enable access to the Compare Data Register. When the channel is in the compare mode, the RDRF bit (bit 0 of the ISR) is forced to a 0. Upon receipt of a matching character, normal receiver operation resumes and the RDRF bit (bit 0 of the ISR) will be set upon receipt of the *next* character.

SPECIFICATIONS

DACIA READ/WRITE WAVEFORMS

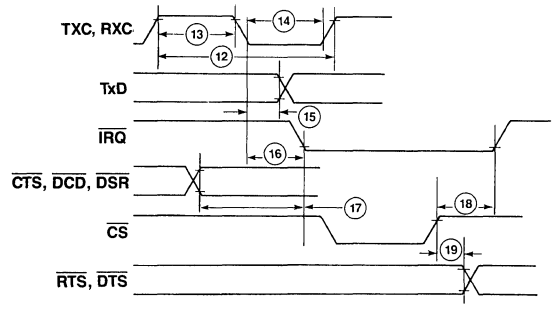


DACIA READ/WRITE CYCLE TIMING

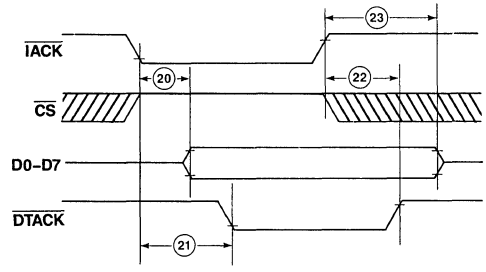
(V_{CC} = 5 Vdc ±5%, V_{SS} = 0 Vdc, T_A = T_L to T_H, unless otherwise noted)

Number	Characteristic	Symbol	Min.	Typ.	Max.	Unit
1	R/$\overline{W}$, RS0-RS2 Valid to $\overline{CS}$ Low (Setup)	T_{RSU}	0		—	ns
2	$\overline{CS}$ Low to R/$\overline{W}$, RS0-RS2 Invalid (Hold)	T_{RH}	45		—	ns
3	$\overline{CS}$ Pulse Width	T_{CP}	210		—	ns
4	$\overline{CS}$ Low to $\overline{DTACK}$ Low	T_{CTL}		160	320	ns
5	$\overline{CS}$ High to $\overline{DTACK}$ High	T_{CTH}		200		ns
6	$\overline{CS}$ Low to Data Valid (Read)	T_{CDV}	—		210	ns
7	$\overline{DTACK}$ Low to Data Valid (Read)	T_{TDV}		90		ns
8	$\overline{CS}$ High to Data Invalid (Read)	T_{CDR}	10		50	ns
9	Data Valid to $\overline{CS}$ High (Write, Setup)	T_{DSU}	20		—	ns
10	$\overline{CS}$ High to Data Invalid (Write Hold)	T_{CDW}	30		—	ns
11	$\overline{DS}$ Low to $\overline{CS}$ Low (Delay for $\overline{CS}$ derived from Data Strobe)	T_{DSC}		20		ns

DACIA TRANSMIT/RECEIVER WAVEFORMS



DACIA INTERRUPT ACKNOWLEDGE WAVEFORMS



TRANSMIT/RECEIVE AND INTERRUPT ACKNOWLEDGE TIMING

(V_{CC} = 5 Vdc ± 5%, V_{SS} = 0 Vdc, T_A = T_L to T_H, unless otherwise noted)

Number	Characteristic	Symbol	Min.	Max.	Unit
TRANSMIT/RECEIVE TIMING					
12	Transmit/Receive Clock Rate	t_{CY}	250	—	ns
13	Transmit/Receive Clock High	t_{CH}	100	—	ns
14	Transmit/Receive Clock Low	t_{CL}	100	—	ns
15	TxC, RxC to TxD Propagation Delay	t_{DD}	—	285	ns
16	TxC, RxC to $\overline{IRQ}$ Propagation Delay	t_{DI}	—	250	ns
17	$\overline{CTS}$, $\overline{DCD}$, $\overline{DSR}$ Valid to $\overline{IRQ}$ Low	t_{CTI}	—	150	ns
18	$\overline{IRQ}$ Propagation Delay (Clear)	t_{IRQ}	—	150	ns
19	$\overline{RTS}$, $\overline{DTR}$ Propagation Delay	t_{DLY}	—	150	ns
INTERRUPT ACKNOWLEDGE TIMING					
20	$\overline{IACK}$ Low to Data Valid	t_{IDV}	—	210	ns
21	$\overline{IACK}$ Low to $\overline{DTACK}$ Low	t_{ITL}	0	—	ns
22	$\overline{IACK}$ High to $\overline{DTACK}$ High	t_{ITH}	0	—	ns
23	$\overline{IACK}$ High to Data Invalid	t_{IDZ}	10	30	ns

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to +7.0	Vdc
Input Voltage	V_{IN}	−0.3 to V_{CC} +0.3	Vdc
Output Voltage	V_{OUT}	−0.3 to V_{CC} +0.3	Vdc
Operating Temperature Commercial Industrial	T_A	 0 to +70 −40 to +85	°C
Storage Temperature	T_{STG}	−55 to +150	°C

*NOTE: Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in other sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING CONDITIONS

Parameter	Symbol	Value
Supply Voltage	V_{CC}	5V ± 5%
Temperature Range Commercial Industrial	T_A	 0 to 70°C −40°C to +85°C

DC CHARACTERISTICS

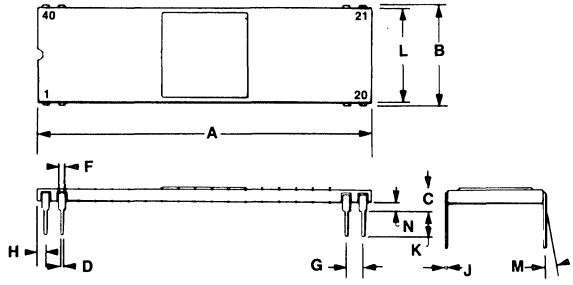
(V_{CC} = 5.0 V ±5%, V_{SS} = 0, T_A = T_L to T_H, unless otherwise noted)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input High Voltage Except XTALI and XTALO XTALI and XTALO	V_{IH}	 +2.0 +2.4	 — —	 V_{CC} + 0.3 V_{CC} + 0.3	V	
Input Low Voltage Except XTALI and XTALO XTALI and XTALO	V_{IL}	 −0.3 −0.3	 — —	 +0.8 +0.4	V	
Input Leakage Current R/$\overline{W}$, $\overline{RES}$, RS0, RS1, RS2, RxD, $\overline{CTS}$, $\overline{DCD}$, $\overline{DSR}$, RxC, TxC, $\overline{CS}$, $\overline{IACK}$	I_{IN}	—	10	50	μA	V_{IN} = 0V to 5.0V V_{CC} = 5.25V
Input Leakage Current for Three-State Off D0–D7	I_{TSI}	—	±2	10	μA	V_{IN} = 0.4V to 2.4V V_{CC} = 5.25V
Output High Voltage D0–D7, TxD, CLK OUT, RTS, DTR	V_{OH}	+2.4	—	—	V	V_{CC} = 4.75V I_{LOAD} = −100 μA
Output Low Voltage D0–D7, TxD, CLK OUT, RTS, DTR	V_{OL}	—	—	+0.4	V	V_{CC} = 4.75V I_{LOAD} = 1.6 mA
Output Leakage Current (Off State) $\overline{IRQ}$, $\overline{DTACK}$	I_{OFF}	—	±2	±10	μA	V_{CC} = 5.25V V_{OUT} = 0 to 2.4V
Power Dissipation	P_D	—	—	10	mW/MHz	
Input Capacitance Except XTALI and XTALO XTALI and XTALO	C_{IN}	 — —	 — —	 5 10	 pF pF	V_{CC} = 5.0V V_{IN} = 0V f = 2 MHz T_A = 25°C
Output Capacitance	C_{OUT}	—		10	pF	

Notes:
1. All units are direct current (dc) except for capacitance.
2. Negative sign indicates outward current flow, positive indicates inward flow.
3. Typical values are shown for V_{CC} = 5.0V and T_A = 25°C.

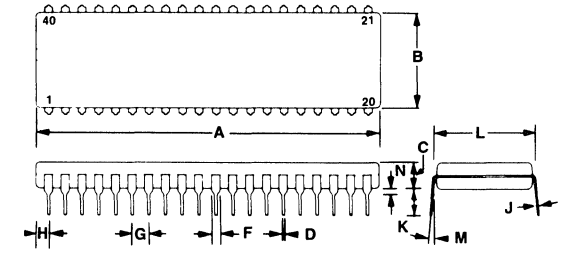
PACKAGE DIMENSIONS

40-PIN CERAMIC DIP



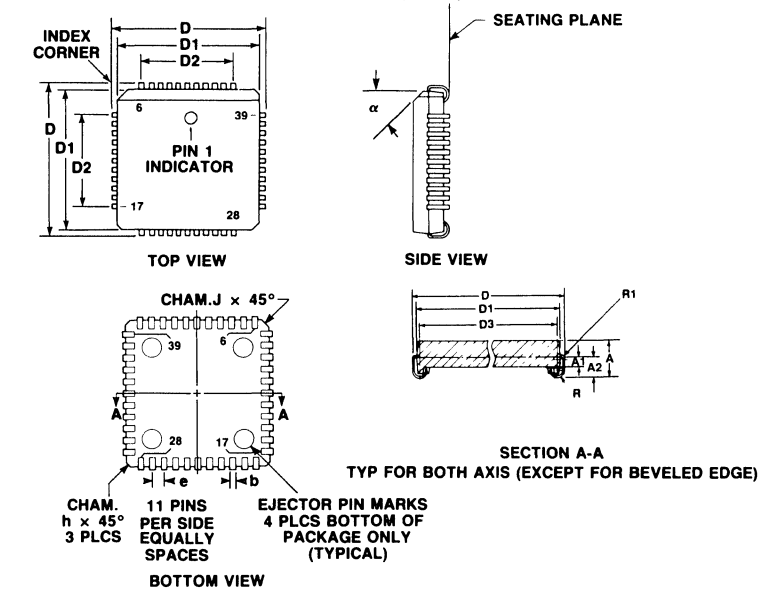
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	50.29	51.31	1.980	2.020
B	15.11	15.88	0 595	0.625
C	2.54	4 19	0.100	0.165
D	0 38	0.53	0 015	0.021
F	0 76	1.27	0.030	0.050
G	2.54 BSC		0.100 BSC	
H	0.76	1.78	0 030	0.070
J	0 20	0.33	0.008	0.013
K	2 54	4.19	0 100	0 165
L	14.60	15.37	0 575	0.605
M	0°	10°	0°	10°
N	0 51	1.52	0.020	0 060

40-PIN PLASTIC DIP



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	51 82	52.32	2.040	2.060
B	13 46	13.97	0 530	0.550
C	3.56	5 08	0.140	0.200
D	0.38	0.53	0.015	0.021
F	1 02	1.52	0.040	0 060
G	2.54 BSC		0 100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.30	0.008	0.012
K	3.30	4.32	0.130	0.170
L	15.24 BSC		0.600 BSC	
M	7°	10°	7°	10°
N	0.51	1.02	0.020	0.040

44-PIN PLASTIC LEADED CHIP CARRIER (PLCC)



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4 14	4 39	0.163	0.173
A1	1.37	1.47	0.054	0.058
A2	2.31	2.46	0.091	0.097
b	0.457 TYP		0.018 TYP	
D	17.45	17.60	0.687	0.693
D1	16.46	16.56	0.648	0.652
D2	12.62	12.78	0.497	0.503
D3	15.75 REF		0.620 REF	
e	1.27 BSC		0.050 BSC	
h	1.15 TYP		0.045 TYP	
J	0.25 TYP		0.010 TYP	
α	45° TYP		45° TYP	
R	0.89 TYP		0.035 TYP	
R1	0.25 TYP		0.010 TYP	

Rockwell

R68560, R68561 Multi-Protocol Communications Controller (MPCC)

DESCRIPTION

The R68560, R68561 Multi-Protocol Communications Controller (MPCC) interfaces a single serial communications channel to a 68008/68000 microcomputer-based system using either asynchronous or synchronous protocol. High speed bit rate, automatic formatting, low overhead programming, eight character buffering, two channel DMA interface and three separate interrupt vector numbers optimize MPCC performance to take full advantage of the 68008/68000 processing capabilities and asynchronous bus structure.

In synchronous operation, the MPCC supports bit-oriented protocols (BOP), such as SDLC/HDLC, and character-oriented protocols (COP), such as IBM Bisync (BSC) in either ASCII or EBCDIC coding. Formatting, synchronizing, validation and error detection is performed automatically in accordance with protocol requirements and selected options. Asynchronous (ASYNC) and isochronous (ISOC) modes are also supported. In addition, modem interface handshake signals are available for general use.

Control, status and data are transferred between the MPCC and the microcomputer bus via 22 directly addressable registers and a DMA interface. Two first-in first-out (FIFO) registers, addressable through separate receiver and transmitter data registers, each buffer up to eight characters at a time to allow more MPU processing time to service data received or to be transmitted and to maximize bus throughput, especially during DMA operation. The two-channel Direct Memory Access (DMA) interface operates with the MC68440/MC68450 DMA Controllers. Three prioritized interrupt vector numbers separately support receiver, transmitter and modem interface operation.

An on-chip oscillator drives the internal baud rate generator (BRG) and an external clock output with an 8 MHz input crystal or clock frequency. The BRG, in conjunction with two selectable prescalers and 16-bit programmable divisor, provides a data bit rate of DC to 4 MHz.

The 48-pin R68561 supports word-length (16-bit) operation when connected to the 68000 16-bit asynchronous bus, as well as byte-length (8-bit) operation when connected to the 68008 8-bit bus. The 40-pin R68560 supports byte-length operation on the 68008 bus.

FEATURES

- Full duplex synchronous/asynchronous receiver and transmitter
- Implements IBM Binary Synchronous Communications (BSC) in two coding formats: ASCII and EBCDIC
- Supports other synchronous character-oriented protocols (COP), such as six-bit BSC, X3.28k, ISO IS1745, ECMA-16, etc.
- Supports synchronous bit oriented protocols (BOP), such as SDLC, HDLC, X.25, etc.
- Asynchronous and isochronous modes
- Modem handshake interface
- High speed serial data rate (DC to 4 MHz)
- Internal oscillator and baud rate generator with programmable data rate
- Crystal or TTL level clock input and buffered clock output (8 MHz)
- Direct interface to 68008/68000 asynchronous bus
- Eight-character receiver and transmitter buffer registers
- 22 directly addressable registers for flexible option selection, complete status reporting, and data transfer
- Three separate programmable interrupt vector numbers for receiver, transmitter and serial interface
- Maskable interrupt conditions for receiver, transmitter and serial interface
- Programmable microprocessor bus data transfer; polled, interrupt and two-channel DMA transfer compatible with MC68440/MC68450
- Clock control register for receiver clock divisor and receiver and transmitter clock routing
- Selectable full/half duplex, autoecho and local loop-back modes
- Selectable parity (enable, odd, even) and CRC (control field enable, CRC-16, CCITT V.41, VRC/LRC)

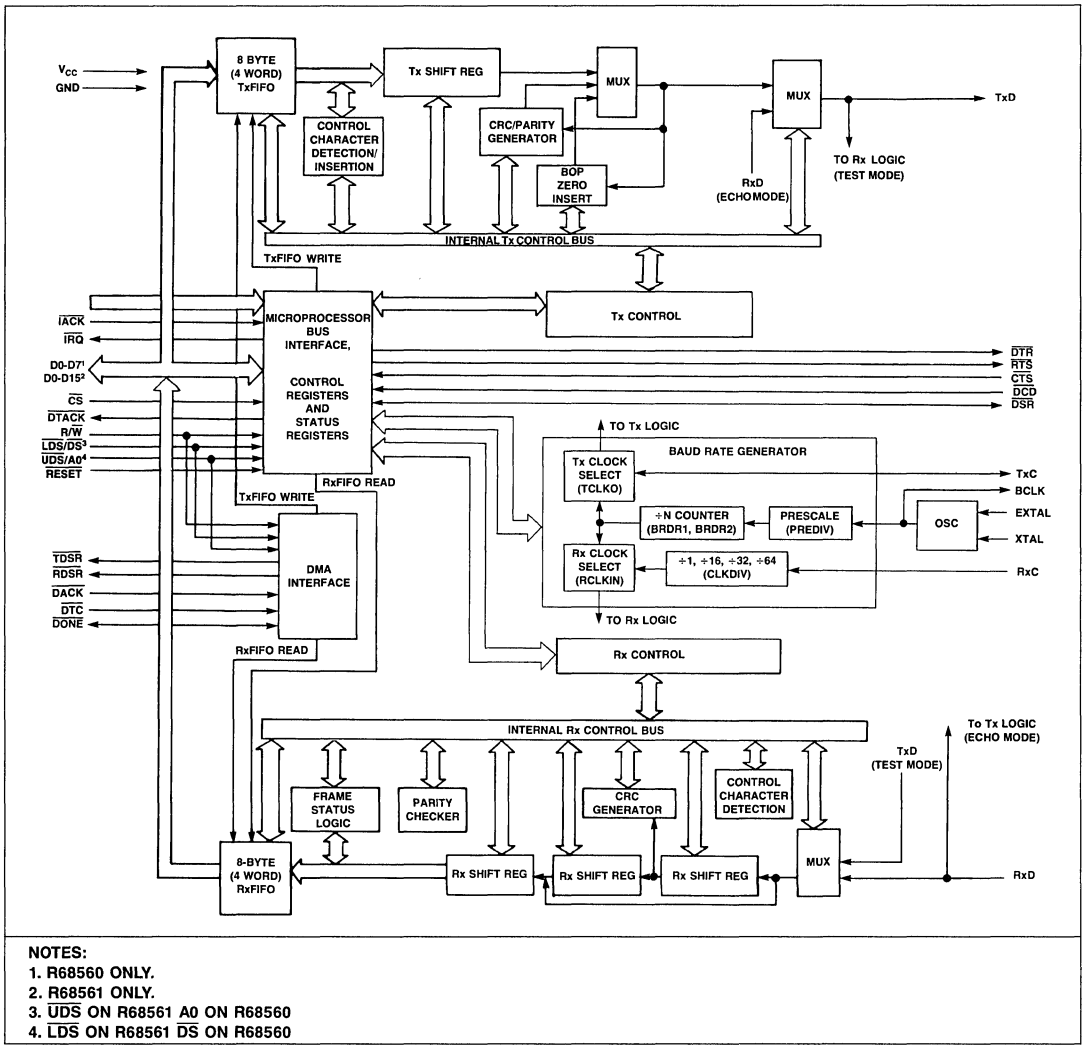
ORDERING INFORMATION

Part Number	Frequency	Temperature Range
R6856	4 MHz	0°C to 70°C

Package: C = Ceramic
P = Plastic

Number of pins: 0 = 40
1 = 48

4



NOTES:
1. **R68560 ONLY.**
2. **R68561 ONLY.**
3. **$\overline{UDS}$ ON R68561 A0 ON R68560**
4. **$\overline{LDS}$ ON R68561 $\overline{DS}$ ON R68560**

Figure 1. MPCC Block Diagram

PIN DESCRIPTION

Throughout the document, signals are presented using the terms active and inactive or asserted and negated independently of whether the signal is active in the high-voltage state or low-voltage state. (The active state of each logic pin is described below.) Active low signals are denoted by a superscript bar. For example, R/$\overline{W}$ indicates write is active low and read is active high.

Note: The R68561 interface is described for word mode operation only and the R68560 interface is described for byte mode operation only.

A1–A4—Address Lines. A1–A4 are active high inputs used in conjunction with the $\overline{CS}$ input to access the internal registers. The address map for these registers is shown in Table 1.

D0–D15—Data Lines. The bidirectional data lines transfer data between the MPCC and the MPU, memory or other peripheral device. D0–D15 are used when connected to the 16-bit 68000 bus and operating in the MPCC word mode. D0–D7 are used when connected to the 16-bit 68000 bus or the 8-bit 68008 bus and operating in the MPCC byte mode. The data bus is three-stated when $\overline{CS}$ is inactive. (See exceptions in DMA mode.)

$\overline{CS}$—Chip Select. $\overline{CS}$ low selects the MPCC for programmed transfers with the host. The MPCC is deselected when the $\overline{CS}$ input is inactive in non-DMA mode. $\overline{CS}$ must be decoded from the address bus and gated with address strobe ($\overline{AS}$).

R/$\overline{W}$—Read/Write. R/$\overline{W}$ controls the direction of data flow through the bidirectional data bus by indicating that the current bus cycle is a read (high) or write (low) cycle.

$\overline{DTACK}$—Data Transfer Acknowledge. $\overline{DTACK}$ is an active low output that signals the completion of the bus cycle. During read or interrupt acknowledge cycles, $\overline{DTACK}$ is asserted by the MPCC after data has been provided on the data bus; during write cycles it is asserted after data has been accepted at the data bus. $\overline{DTACK}$ is driven high after assertion prior to being tri-stated. A holding resistor is required to maintain $\overline{DTACK}$ high between bus cycles.

$\overline{DS}$—Data Strobe (R68560). During a write (R/$\overline{W}$ low), the $\overline{DS}$ positive transition latches data on data bus lines D0–D7 into the MPCC. During a read (R/$\overline{W}$ high), $\overline{DS}$ low enables data from the MPCC to data bus lines D0–D7.

$\overline{LDS}$—Lower Data Strobe (R68561). During a write (R/$\overline{W}$ low), the positive transition latches data on the data bus lines D0–D7 (and on D8–D15 if $\overline{UDS}$ is low) into the MPCC. During a read (R/$\overline{W}$ high), $\overline{LDS}$ low enables data from the MPCC to D0–D7 (and to D8–D15 if $\overline{UDS}$ is low).

A0—Address Line A0 (R68560). When interfacing to an 8-bit data bus system such as the 68008, address line A0 is used to access an internal register. A0 = 0 defines an even register and A0 = 1 defines an odd register. See Table 1b.

$\overline{UDS}$—Upper Data Strobe (R68561). When interfacing to a 16-bit data bus system such as the 68000, a low on control bus signal $\overline{UDS}$ enables access to the upper data byte on D8–D15. A high on $\overline{UDS}$ disables access to D8–D15. Data is latched and enabled in conjunction with $\overline{LDS}$.

$\overline{IRQ}$—Interrupt Request. The active low $\overline{IRQ}$ output requests interrupt service by the MPU. $\overline{IRQ}$ is driven high after assertion prior to being tri-stated.

$\overline{IACK}$—Interrupt Acknowledge. The active low $\overline{IACK}$ input indicates that the current bus cycle is an interrupt acknowledge cycle. When $\overline{IACK}$ is asserted the MPCC places an interrupt vector on the lower byte (D0–D7) of the data bus.

$\overline{TDSR}$—Transmitter Data Service Request. When Transmitter DMA mode is active, the low $\overline{TDSR}$ output requests DMA service.

$\overline{RDSR}$—Receiver Data Service Request. When receiver DMA mode is active, the low $\overline{RDSR}$ output requests DMA service.

$\overline{DACK}$—DMA Acknowledge. The $\overline{DACK}$ low input indicates that the data bus has been acquired by the DMAC and that the requested bus cycle is beginning.

$\overline{DTC}$—Data Transfer Complete. On a 68000 bus, the $\overline{DTC}$ low input indicates that a DMA data transfer was completed with no bus conflicts. $\overline{DTC}$ in response to a $\overline{RDSR}$ indicates that the data has been successfully stored in memory. $\overline{DTC}$ in response to a $\overline{TDSR}$ indicates that the data is present on the data bus for strobing into the MPCC. If not used, this input should be connected to ground.

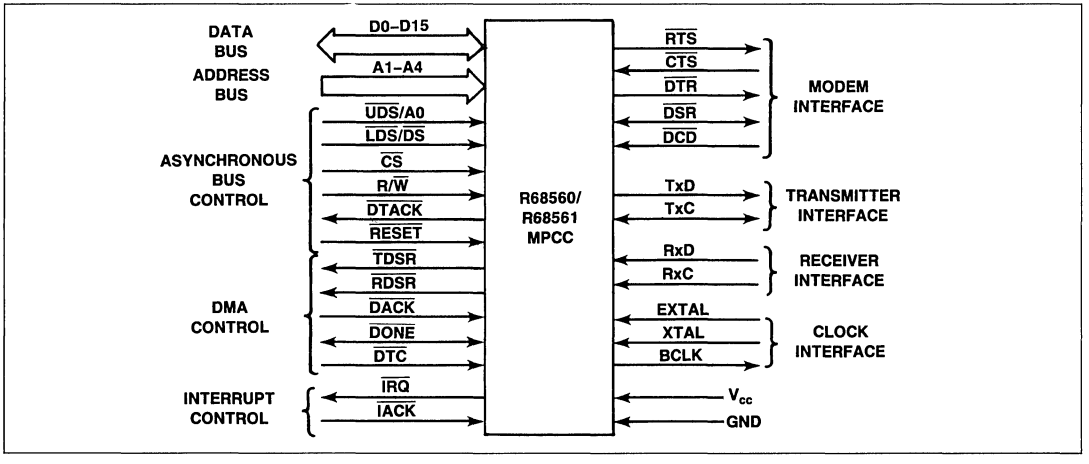


Figure 2. MPCC Input and Output Signals

$\overline{\text{DONE}}$—Done. $\overline{\text{DONE}}$ is a bidirectional active low signal. The $\overline{\text{DONE}}$ signal is asserted by the DMAC when the DMA transfer count is exhausted and there is no more data to be transferred, or asserted by the MPCC when the status byte following the last character of a frame (block) is being transferred in response to a $\overline{\text{RDSR}}$. The $\overline{\text{DONE}}$ signal asserted by the DMAC in response to a $\overline{\text{TDSR}}$ will be stored to track with the data byte (lower byte for word transfer) through the TxFIFO.

$\overline{\text{RESET}}$—Reset. $\overline{\text{RESET}}$ is an active low, high impedance input that initializes all MPCC functions. $\overline{\text{RESET}}$ must be asserted for at least 500 ns to initialize the MPCC.

$\overline{\text{DTR}}$—Data Terminal Ready. The $\overline{\text{DTR}}$ active low output is general purpose in nature, and is controlled by the DTRLVL bit in the Serial Interface Control Register (SICR).

$\overline{\text{RTS}}$—Request to Send. The $\overline{\text{RTS}}$ active low output is general purpose in nature, and is controlled by the RTSLVL bit in the SICR.

$\overline{\text{CTS}}$—Clear to Send. The $\overline{\text{CTS}}$ active low input positive transition and level are reported in the CTST and CTSLVL bits in the Serial Interface Status Register (SISR), respectively.

$\overline{\text{DSR}}$—Data Set Ready. The $\overline{\text{DSR}}$ active low input negative transition and level are reported in the DSRT and DSRLVL bits in the SISR, respectively. $\overline{\text{DSR}}$ is also an output for RSYN.

$\overline{\text{DCD}}$—Data Carrier Detect. The $\overline{\text{DCD}}$ active low input positive transition and level are reported in the DCDT and DCDLVL bits in the the SISR, respectively.

TxD—Transmitted Data. The MPCC transmits serial data on the TxD output. The TxD output changes on the negative going edge of TxC.

RxD—Received Data. The MPCC receives serial data on the RxD input. The RxD input is shifted into the receiver with the negative going edge of RxC.

TxC—Transmitter Clock. TxC can be programmed to be an input or an output. When TxC is selected to be an input, the transmitter clock must be provided externally. When TxC is programmed to be an output, a clock is generated by the MPCC's internal baud rate generator.

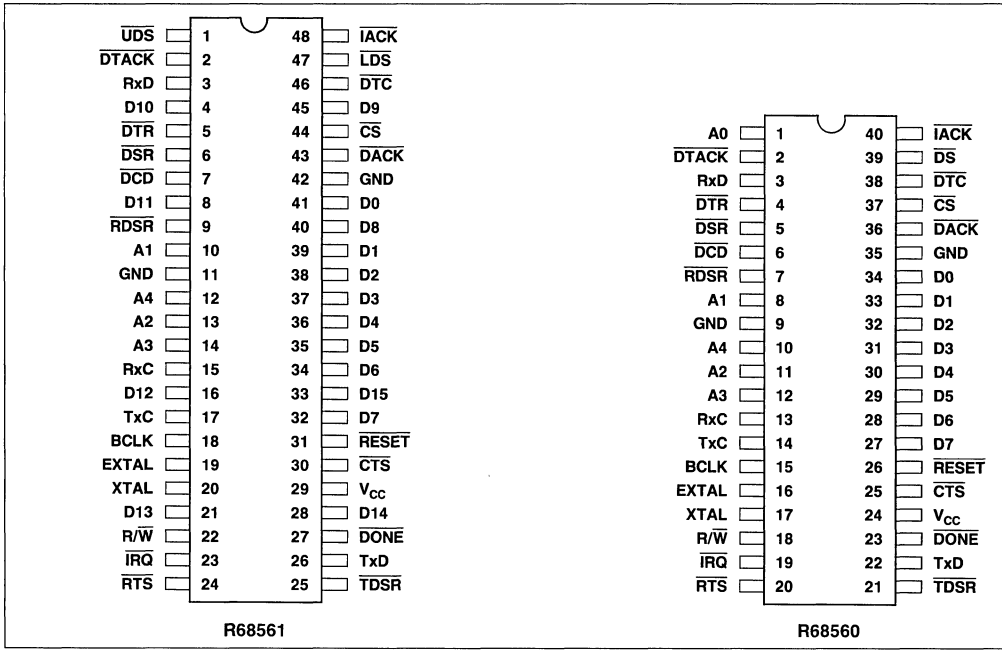
RxC—Receiver Clock. RxC provides the MPCC receiver with received data timing information.

EXTAL—Crystal/External Clock Input.
XTAL Crystal Return. EXTAL and XTAL connect a 20 kHz to 8.064 MHz parallel resonant external crystal to the MPCC internal oscillator (see CLOCK OSCILLATOR). The pin EXTAL may also be used as a TTL level input to supply DC to 8 MHz reference timing from an external clock source. XTAL must be tied to ground when applying an external clock to the EXTAL input.

BCLK—Buffered Clock. BCLK is the internal oscillator buffered output available to other MPCC devices eliminating the need for additional crystals.

V_{CC}—Power. 5V ±5%.

GND—Ground. Ground (V_{SS}).



Pin Configuration

MPCC REGISTERS

Twenty-two registers control and monitor the MPCC operation. The registers and their addresses are identified in Table 1a (R68561 operation in word mode) and in Table 1b (R68560 operation in byte mode). When the R68561 is operated in the word mode, two registers are read or written at a time starting at an even boundary. When the R68560 is operated in the byte mode, each register is explicitly addressed based on A0.

Table 2 summarizes the MPCC register bit assignments and their access. A read from an unassigned location results in a read from a "null register." A null register returns all ones for data and results in a normal bus cycle. Unused bits of a defined register are read as zeros unless otherwise noted.

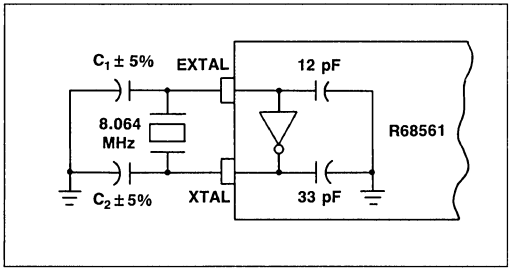
Table 1a. R68561 Accessible Registers (Word Mode)

Register(s)		R/W	Addr (Hex.)	Address Lines A4 A3 A2 A1
15 — (Odd Registers) — 8	7 — (Even Registers) — 0			
Receiver Control Register (RCR)	Receiver Status Register (RSR)	R/W	00	0 0 0 0
Receiver Data Register (RDR)—16 bits[1]		R	02	0 0 0 1
Receiver Interrupt Enable Register (RIER)	Receiver Interrupt Vector Number Register (RIVNR)	R/W	04	0 0 1 0
Transmitter Control Register (TCR)	Transmitter Status Register (TSR)	R/W	08	0 1 0 0
Transmitter Data Register (TDR)—16 bits[2]		W	0A	0 1 0 1
Transmitter Interrupt Enable Register (TIER)	Transmitter Interrupt Vector Number Register (TIVNR)	R/W	0C	0 1 1 0
Serial Interface Control Register (SICR)	Serial Interface Status Register (SISR)	R/W	10	1 0 0 0
Reserved[3]	Reserved[3]	R/W	12	1 0 0 1
Serial Interrupt Enable Register (SIER)	Serial Interrupt Vector Number Register (SIVNR)	R/W	14	1 0 1 0
Protocol Select Register 2 (PSR2)	Protocol Select Register (PSR1)	R/W	18	1 1 0 0
Address Register 2 (AR2)	Address Register 1 (AR1)	R/W	1A	1 1 0 1
Baud Rate Divider Register 2 (BRDR2)	Baud Rate Divider Register 1 (BRDR1)	R/W	1C	1 1 1 0
Error Control Register (ECR)	Clock Control Register (CCR)	R/W	1E	1 1 1 1

Notes:
1. Accessible register of the four word RxFIFO. The data is not initialized, however, $\overline{RES}$ resets the RxFIFO pointer to the start of the first word.
2. Accessible register of the four word TxFIFO. The data is not initialized, however, $\overline{RES}$ resets the TxFIFO pointer to the start of the first word.
3. Reserved registers may contain random bit values.

CLOCK OSCILLATOR

An on-chip oscillator is designed for a parallel resonant crystal connected between XTLI and XTLO pins. The equivalent oscillator circuit is shown in the figure below.



A parallel resonant crystal is specified by its load capacitance and series resonant resistance. For proper oscillator operation, the load capacitance (C_L), series resistance (R_s) and the crystal resonant frequency (F) must meet the following two relations:

$$C_1 = 2C_L - 12 \text{ pF}$$

$$C_2 = 2C_L - 33 \text{ pF}$$

$$R_s \ / \ R_{smax} = \frac{2 \times 10^6}{(FC_L)^2}$$

where: F is in MHz; C and C_L are in pF; R is in ohms.

To select a parallel resonant crystal for the oscillator, first select the load capacitance from a crystal manufacturer's catalog. Next, calculate R_{smax} based on F and C_L. The selected crystal must have a R_s less than the R_{smax}.

For example, if C_L = 20 pF for an 8.064 MHz parallel resonant crystal, then

C_1 = 40 − 12 = 28 pF (Use standard value of 27 pF.)

C_2 = 40 − 33 = 7 pF (Use standard value of 6.8 pF.)

Note: C_X = Total Shunt Capacitance including that due to board layout.

The series resistance of the crystal must be less than

$$R_{smax} = \frac{2 \times 10^6}{(8.064 \times 20)^2} = 77 \text{ ohms}$$

Table 1b. R68560 Accessible Registers (Byte Mode)

Register(s)	R/W	Addr (Hex.)	Address Lines A4	A3	A2	A1	A0
7 0							
Receiver Status Register (RSR)	R/W	00	0	0	0	0	0
Receiver Control Register (RCR)	R/W	01	0	0	0	0	1
Receiver Data Register (RDR)—8 bits[1]	R	02	0	0	0	1	0
Reserved[3]		03	0	0	0	1	1
Receiver Interrupt Vector Number Register (RIVNR)	R/W	04	0	0	1	0	0
Receiver Interrupt Enable Register (RIER)	R/W	05	0	0	1	0	1
Transmitter Status Register (TSR)	R/W	08	0	1	0	0	0
Transmitter Control Register (TCR)	R/W	09	0	1	0	0	1
Transmitter Data Register (TDR)[2]—8 bits	W	0A	0	1	0	1	0
Reserved[3]		0B	0	1	0	1	1
Transmitter Interrupt Vector Number Register (TIVNR)	R/W	0C	0	1	1	0	0
Transmitter Interrupt Enable Register (TIER)	R/W	0D	0	1	1	0	1
Serial Interface Status Register (SISR)	R/W	10	1	0	0	0	0
Serial Interface Control Register (SICR)	R/W	11	1	0	0	0	1
Reserved[3]		12	1	0	0	1	0
Reserved[3]		13	1	0	0	1	1
Serial Interrupt Vector Number Register (SIVNR)	R/W	14	1	0	1	0	0
Serial Interrupt Enable Register (SIER)	R/W	15	1	0	1	0	1
Protocol Select Register 1 (PSR1)	R/W	18	1	1	0	0	0
Protocol Select Register 2 (PSR2)	R/W	19	1	1	0	0	1
Address Register 1 (AR1)	R/W	1A	1	1	0	1	0
Address Register 2 (AR2)	R/W	1B	1	1	0	1	1
Baud Rate Divider Register 1 (BRDR1)	R/W	1C	1	1	1	0	0
Baud Rate Divider Register 2 (BRDR2)	R/W	1D	1	1	1	0	1
Clock Control Register (CCR)	R/W	1E	1	1	1	1	0
Error Control Register (ECR)	R/W	1F	1	1	1	1	1

Notes:
1. Accessible register of the eight byte RxFIFO. The data is not initialized, however, $\overline{RES}$ resets the RxFIFO pointer to the start of the first byte.
2. Accessible register of the eight byte TxFIFO. The data is not initialized, however, $\overline{RES}$ resets the TxFIFO pointer to the start of the first byte.
3. Reserved registers may contain random bit values.

Table 2. MPCC Register Bit Assignments

R/W Access	Bit Number 7	6	5	4	3	2	1	0	Reset(1) Value	
R/W	RDA	EOF	0	C/PERR	FRERR	ROVRN	RA/B	RIDLE	00	Receiver Status Register (RSR)
R/W	0	RDSREN	DONEEN	RSYNEN	STRSYN	0	RABTEN	RRES	01	Receiver Control Register (RCR)
R	RECEIVER DATA (RxFIFO)[2]								— —	Receiver Data Register (RDR)
R/W	RECEIVER INTERRUPT VECTOR NUMBER (RIVN)								0F	Receiver Interrupt Vector Number Register (RIVNR)
R/W	RDA IE	EOF IE	0	C/PERR IE	FRERR IE	ROVRN IE	RA/B IE	0	00	Receiver Interrupt Enable Register (RIER)
R/W	TDRA	TFC	0	0	0	TUNRN	TFERR	0	80	Transmitter Status Register (TSR)
R/W	TEN	TDSREN	TICS	THW	TLAST	TSYN	TABT	TRES	01	Transmitter Control Register (TCR)
W	TRANSMITTER DATA (TxFIFO)[2]								— —	Transmitter Data Register (TDR)
R/W	TRANSMITTER INTERRUPT VECTOR NUMBER (TIVN)								0F	Transmitter Interrupt Vector Number Register (TIVNR)
R/W	TDRA IE	TFC IE	0	0	0	TUNRN IE	TFERR IE	0	00	Transmitter Interrupt Enable Register (TIER)
R/W	CTST	DSRT	DCDT	CTSLVL	DSRLVL	DCDLVL	0	0	00	Serial Interface Status Register (SISR)
R/W	RTSLVL	DTRLVL	0	0	0	ECHO	TEST	0	00	Serial Interface Control Register (SICR)
	RANDOM BIT VALUES									(reserved)
	RANDOM BIT VALUES									(reserved)
R/W	SERIAL INTERRUPT VECTOR NUMBER (SIVN)								0F	Serial Interrupt Vector Number Register (SIVNR)
R/W	CTS IE	DSR IE	DCD IE	0	0	0	0	0	00	Serial Interrupt Enable Register (SIER)
R/W	0	0	0	0	0	0	CTLEX	ADDEX	00	Protocol Select Register 1 (PSR1)
R/W	WD/BYT	STOP BIT SEL		CHAR LEN SEL		PROTOCOL SEL			00	Protocol Select Register 2 (PSR2)
		SB2	SB1	CL2	CL1	PS3	PS2	PS1		
R/W	BOP ADDRESS/BSC & COP PAD								00	Address Register 1 (AR1)
R/W	BOP ADDRESS/BSC & COP SYN								00	Address Register 2 (AR2)
R/W	BAUD RATE DIVIDER (LSH)								01	Baud Rate Divider Register 1 (BRDR1)
R/W	BAUD RATE DIVIDER (MSH)								00	Baud Rate Divider Register 2 (BRDR2)
R/W	0	0	0	PSCDIV	TCLKO	RCLKIN	CLK DIV		00	Clock Control Register (CCR)
							CK2	CK1		
R/W	PAREN	ODDPAR	0	0	CFCRC	CRCPRE	CRC SEL		04	Error Control Register (ECR)
							CR2	CR1		

Notes:
1. RESET = Register contents upon power up or $\overline{\text{RESET}}$.
2. 16-bits for R68561 (word mode); 8-bits for R68560 (byte mode).

REGISTER DEFINITIONS

RECEIVER REGISTERS

Receiver Status Register (RSR)

7	6	5	4	3	2	1	0
RDA	EOF	0	C/PERR	FRERR	ROVRN	RA/B	RIDLE

Address = 00 Reset Value = $00

The Receiver Status Register (RSR) contains the status of the receiver including error conditions. Status bits are cleared by writing a 1 into respective positions, by writing a 1 into the RCR RRES bit or by $\overline{\text{RESET}}$. If an EOF, C/PERR, or FRERR is set in the RSR, the data reflecting the error (the next byte or word in the RxFIFO) must be read prior to resetting the corresponding status bit in the RSR. The $\overline{\text{IRQ}}$ output is asserted if any of the conditions reported by the status bits occur and the corresponding interrupt enable bit in the RIER is set.

The RSR format is the same as the frame status format (see below) except as noted.

RSR
7 RDA —Receiver Data Available. (RSR only).
0 The FxFIFO is empty (i.e., no received data is available).
1 RDA is set and an interrupt issued (if enabled) when the RxFIFO has 1 to 8 bytes, or 1 to 4 words, of data in it.

RDA Reset — RDA cannot be cleared or reset in software. It is initialized to 0 upon hardware reset and remains 0 if no data has been received. It is set to a 1 and an interrupt issued when a data byte/word is loaded to the RxFIFO with the negative edge of RxC coincident with the first bit of the next byte transmitted. It is automatically reset to 0 when the last byte/word is read from the RxFIFO by the host through RDR.

RSR
6 EOF —End of Frame. (BOP and BSC)
0 No end of frame has been detected.
1 The closing flag (BOP) or pad (BSC) has been detected. EOF is loaded in the RxFIFO along with the FSB with which it is associated. The EOF is loaded into the RSR and the interrupt issued, if enabled, (when the RxFIFO read pointer is positioned at the FSB) with the trailing edge of $\overline{\text{LDS}}$.

EOF Reset — The byte/word containing the FSB must be read from the RxFIFO before resetting the EOF bit. Then EOF may be reset by writing a 1 to RSR6.

RSR
5 RHW —Receive Half Word. (Frame Status only)*
0 The last word of the frame contains data on the upper half (D8–D15) and frame status on the lower half (D0–D7) of the data bus.
1 The lower half of the data bus (D0–D7) contains the frame status but the upper half (D8–D15) is blank or invalid.

*See Frame Status (RSR) on next page.

RSR
4 C/PERR —CRC/Parity Error.
0 No CRC or parity error detected.
1 CRC error detected (BOP, BSC) or parity error detected (ASYNC, ISOC and COP). The C/PERR bit is loaded into the RxFIFO with the negative-going RxC edge, along with the byte or word with which it is associated. For ASYNC, ISOCH or COP protocols, this is with the byte/word containing a parity error. For BOP or BSC, it is loaded to RxFIFO (after the CRC check) with the FSB. C/PERR is loaded into the RSR and the interrupt issued (when the read pointer is positioned at the FSB) with the trailing edge of $\overline{\text{LDS}}$.

C/PERR Reset — The byte/word containing the FSB must be read from the RxFIFO before resetting the C/PERR bit. Then it may be reset by writing a 1 to RSR4.

RSR
3 FRERR —Frame Error.
0 No frame error detected.
1 FRERR is set for receiver overrun, flag detected off boundary (BOP), or frame error (ASYNC, ISOCH). For receiver overrun, the FRERR bit is set in the RxFIFO with the last byte when the overrun is detected.

For BOP, a minimum message size is an opening flag, one address byte and one control byte. If the closing flag is detected before the control byte is sent, a short frame is indicated and a frame error results. For address extension, multi-address bytes may be received before the control byte is expected. The FRERR bit is latched in RxFIFO with the negative-going edge of RxC with the last address byte received upon detection of the flag off boundary. FRERR is loaded into the RSR and the interrupt issued when the read pointer is positioned at the FSB with the trailing edge of $\overline{\text{LDS}}$.

In ASYNC or ISOCH, a FRERR bit set indicates that the stop bit was detected off boundary (too early or too late for the number of bits expected by the setting of PSR2-3 and PSR2-4) or it was not the correct width (as expected by the setting of PSR2-6 and PSR2-5).

FRERR Reset — The byte/word containing the FSB must be read from the RxFIFO before resetting the C/PERR bit. The C/PERR bit may then be reset by writing a 1 to RSR3.

RSR
2 ROVRN —Receiver Overrun.
0 No receiver overrun detected.
1 Receiver overrun detected. Data is loaded into the RxFIFO on byte boundaries with the negative-going edge of RxC coincident with the first bit of the subsequent data being received. When the eighth byte, or fourth word, of data has been written into RxFIFO without any data being read out, the RxFIFO is full and the incremented write pointer "catches up" with the read pointer. The next attempt to write data to RxFIFO causes ROVRN bit to be loaded to the RSR and the interrupt issued (if enabled). The data in the RxFIFO is not affected, but new received data is lost.

ROVRN Reset — The ROVRN bit is not self-clearing when data is read from the RxFIFO, but may be reset by writing a 1 to RSR2.

RSR
1 RA/B —Receiver Abort/Break.
0 Normal Operation.
1 (BOP) When an ABORT (seven 1s) is detected after the opening flag, the RA/B bit is set in the RSR and an interrupt issued (if enabled). This bit is latched with the negative edge of RxC after the seventh 1 bit is detected. (NOTE: Because the previous byte can end in zero to five 1 bits, the abort could be recognized in the next byte as early as two to seven 1 bits.)

(BSC) When ENQ is detected in a block of text data, the RA/B bit is set in the RSR and the interrupt issued (if enabled) with the next negative edge of the RxC clock.

RA/B Reset — The RA/B bit is reset by writing a 1 to RSR1.

RSR
0 RIDLE —Receiver Idle. (BOP only).
0 Receiver is not idle.
1 15 or more 1s have been detected. The RIDLE bit is set in RSR with the negative edge of the next RxC after 15 consecutive 1s have been detected.

RIDLE Reset — The RIDLE is reset by writing a 1 to RSR0. (NOTE: The RIDLE bit will set again in 15 clock cycles if RxD is still in the idle condition.)

*Frame Status (RSR)

7	6	5	4	3	2	1	0
0	EOF	RHW	C/PERR	FRERR	ROVRN	RA/B	0

For the BSC and BOP protocols which have defined message blocks or frames, a "frame status" byte will be loaded into the RxFIFO following the last data byte of each block. The frame status contains all the status contained within the RSR with the exception of RDA and RIDLE. But, in addition to the RSR contents, the frame status byte has a RHW status in bit 5 which indicates either an even or odd boundary (applicable to word mode only).

If the MPCC is in word mode and the last data byte was on an even byte boundary (i.e., there was an even number of bytes in the message), a blank byte will be loaded into the RxFIFO prior to loading the frame status byte in order to force the "frame status" byte and the next frame to be on an even boundary. When RHW = 0, the last word of the frame contains data on the upper half and status on the lower half of the data bus. If RHW = 1, the lower half of the bus contains status but the upper half is a blank or invalid byte.

In the byte mode, the status byte will always immediately follow the last data byte of the block/frame (see Figure 3). The EOF status in the RSR is then set when the byte/word containing the frame status is the next byte/word to be read from the RxFIFO.

In the receiver DMA mode, when the EOF status in the RSR is set, DONE is asserted to the DMAC. Thus the last byte accessed by the DMAC is always a status byte, which the processor may read to check the validity of entire frame.

Receiver Control Register (RCR)

7	6	5	4	3	2	1	0
—	RDSREN	DONEEN	RSYNEN	STRSYN	0	RABEN	RRES

Address = 01 Reset value = $01

The Receiver Control Register (RCR) selects receiver control options.

RCR
7 —Not used.

RCR
6 RDSREN —Receiver Data Service Request Enable.
0 Disable receiver DMA mode.
1 Enable receiver DMA mode.

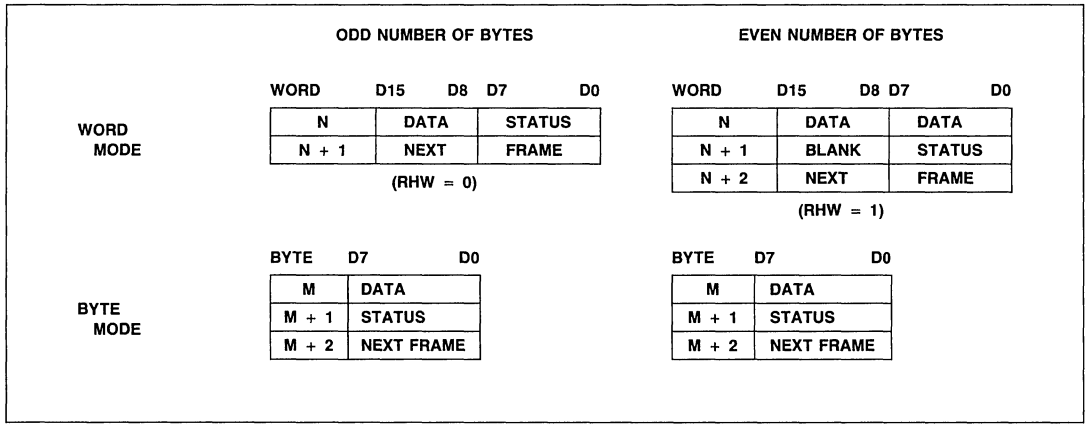


Figure 3. BSC/BOP Block/Frame Status Location

RCR
5 **DONEEN —$\overline{\text{DONE}}$ Output Enable.**
0 Disable $\overline{\text{DONE}}$ output.
1 Enable $\overline{\text{DONE}}$ output. (When the receiver is in the DMA mode, i.e., RDSREN = 1).

RCR
4 **RSYNEN —RSYNEN Output Enable.** Selects the DSR signal input or the RSYN SYNC signal output on the $\overline{\text{DSR}}$ pin.
0 Input DSR on $\overline{\text{DSR}}$.
1 Output RSYN on $\overline{\text{DSR}}$.

RCR
3 **STRSYN —Strip SYN Character (COP only).**
0 Do not strip SYN character.
1 Strip SYN character.

RCR
2 **MUST BE ZERO**
0

RCR
1 **RABTEN —Receiver Abort Enable (BOP only).**
0 Do not abort frame upon error detection.
1 Abort frame upon RxFIFO overrun (ROVRN bit = 1 in the RSR) or CFCRC error detection (C/PERR bit = 1 in the RSR). If either error occurs, the MPCC ignores the remainder of the current frame and searches for the beginning of the next frame. (EOF is set upon abort).

RCR
0 **RRES —Receiver Reset Command.**
0 Enable normal receiver operation.
1 Reset receiver. Resets the receiver section including the RxFIFO and the RSR (but not the RCR). RRES is set by $\overline{\text{RESET}}$ or by writing a 1 into this bit and must be cleared by writing a 0 into this bit. RRES requires clearing after $\overline{\text{RESET}}$.

Receiver Data Register (RDR)

R68561 (Word Mode)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSB			Byte 1				LSB	MSB			Byte 0				LSB

Address = 02

R68560 (Byte Mode)

7	6	5	4	3	2	1	0
MSB			Byte 0				LSB

Address = 02

The receiver has an 8-byte (or 4-word) First In First Out (FIFO) register file (RxFIFO) where received data are stored before being transferred to the bus. The received data is transferred out of the RxFIFO via the RDR in 8-bit bytes or 16-bit words depending on the WD/BYT bit setting in PSR2. When the RxFIFO has a data byte/word ready to be transferred, the RDA status bit in the RSR is set to 1.

Receiver Interrupt Vector Number Register (RIVNR)

7	6	5	4	3	2	1	0
Receiver Interrupt Vector Number (RIVN)							

Address = 04 Reset value = $0F

If a receiver interrupt condition occurs (as reported by status bits in the RSR that correspond to interrupt enable bits in the RIER) and the corresponding bit is set in the RIER, $\overline{\text{IRQ}}$ output is asserted to request MPU receiver interrupt service. When the $\overline{\text{IACK}}$ input is asserted from the bus, the Receiver Interrupt Vector Number (RIVN) from the Receiver Interrupt Vector Number Register (RIVNR) is placed on the data bus.

Receiver Interrupt Enable Register (RIER)

7	6	5	4	3	2	1	0
RDA IE	EOF IE	0	C/PERR IE	FRERR IE	ROVRN IE	RA/B IE	0

Address = 05 Reset value = $00

The Receiver Interrupt Enable Register (RIER) contains interrupt enable bits for the Receiver Status Register (RSR). When enabled, the $\overline{\text{IRQ}}$ output is asserted when the corresponding condition is detected and reported in the RSR.

RIER
7 **RDA IE —Receiver Data Available Interrupt Enable.**
0 Disable RDA Interrupt.
1 Enable RDA Interrupt.

RIER
6 **EOF IE —End of Frame Interrupt Enable.**
0 Disable EOF Interrupt.
1 Enable EOF Interrupt.

RIER
5 **—Not used.**

RIER
4 **C/PERR IE —CRC/Parity Error Interrupt Enable.**
0 Disable C/PERR Interrupt.
1 Enable C/PERR Interrupt.

RIER
3 **FRERR IE —Frame Error Interrupt Enable.**
0 Disable FRERR Interrupt.
1 Enable FRERR Interrupt.

RIER
2 **ROVRN IE —Receiver Overrun Interrupt Enable.**
0 Disable ROVRN Interrupt.
1 Enable ROVRN Interrupt.

RIER
1 **RA/B IE —Receiver Abort/Break Interrupt Enable.**
0 Disable RA/B Interrupt.
1 Enable RA/B Interrupt.

RIER
0 **—Not used.**

TRANSMITTER REGISTERS

Transmitter Status Register (TSR)

7	6	5	4	3	2	1	0
TDRA	TFC	0	0	0	TUNRN	TFERR	0

Address = 08 Reset value = $80

The Transmitter Status Register (TSR) contains the transmitter status including error conditions. The transmitter status bits are cleared by writing a 1 into their respective positions, by writing a 1 into the TCR TRES bit, or by $\overline{\text{RESET}}$. The $\overline{\text{IRQ}}$ output is asserted if any of the conditions reported by the status bits occur and the corresponding interrupt enable bit in the TIER is set.

TSR
7 TDRA —Transmitter Data Register Available.
0 The TxFIFO is full.
1 The TxFIFO is available to be loaded via the TDR (1 to 8 bytes, or 1 to 4 words).

TDRA Reset — TDRA cannot be reset by the host in normal operation. It initializes to a 1 upon hardware or software reset of the MPCC. TDRA is not dependent on the serial clock.

TSR
6 TFC —Transmitted Frame Complete. (BOP, BSC and COP only).
0 (All) Frame not complete.
1 (BOP) Closing flag or ABORT has been transmitted. The TFC bit is set and the interrupt issued (if enabled) with the negative edge of TxC coincident with the end of the last bit of the flag. When TABT is set in TCR1, an ABORT is transmitted immediately but TFC is not issued until after the closing flag or 8 bits of the MARK idle condition after the TxFIFO is flushed of all current data bytes.

(BSC) Trailing pad has been transmitted. TFC bit set and/or interrupt issued with negative edge of TxC coincident with the end of the last bit of the trailing pad.

(COP) Last byte has been transmitted (TLAST set in TCR3). TFC bit set and/or interrupt issued with negative edge of the TxC coincident with the end of the last bit of the last byte.

TFC Reset — One full cycle of the serial clock (TxC) must elapse before the TFC bit can be reset by writing a 1 to TSR6.

TSR
5-3 —Not used.

TSR
2 TUNRN —Transmitter Underrun (BOP, BSC and COP only).
0 No TxFIFO underrun has occurred.
1 An empty TxFIFO was accessed for data. (BOP) Underrun is treated as an ABORT in that eight consecutive 1s are transmitted followed by the idle condition of MARK or FLAG.

(BSC, COP) Underrun causes SYN characters to be transmitted until new data is available in the TxFIFO. The TUNRN bit is set in TSR2 and the interrupt issued with the positive edge of the TxC coincident with the eighth bit of data prior to the ABORT in BOP or to SYN in BSC or COP.

TUNRN Reset — One full cycle of the serial clock (TxC) must elapse before the TUNRN bit can be reset by writing a 1 to TSR2.

TSR
1 TFERR —Transmit Frame Error (BOP only).
0 No frame error has occurred.
1 A short frame condition exists in that no control field is transmitted. (TLAST was issued early with an address byte.) TFERR bit is set and the interrupt issued with the positive edge of TxC coincident with the end of the last bit of the byte causing the error.

TFERR Reset — One full cycle of the serial clock (TxC) must elapse before TFERR bit can be reset by writing a 1 to TSR1.

Transmitter Control Register (TCR)

7	6	5	4	3	2	1	0
TEN	TDSREN	TICS	THW	TLAST	TSYN	TABT	TRES

Address = 09 Reset value = $01

The Transmitter Control Register (TCR) selects transmitter control function.

TCR
7 TEN —Transmitter Enable.
0 Disable transmitter. TxD output is idled. The TxFIFO may be loaded while the transmitter is disabled.
1 Enable transmitter.

TCR
6 TDSREN —Transmitter Data Service Request Enable.
0 Disable transmitter DMA mode.
1 Enable transmitter DMA mode.

TCR
5 TICS —Transmitter Idle Character Select. Selects the idle character to be transmitted when the transmitter is in an active idle mode (transmitter enabled or disabled).
0 Mark Idle (TxD output is held high).
1 Content of AR2 (BSC and COP), BREAK condition (ASYNC and ISOC), or FLAG character (BOP).

TCR
4 THW —Transmit Half Word. (R68561, word mode only). This bit is used when the frame or block ends on an odd boundary in conjunction with the TLAST bit and indicates that the last word in the TxFIFO contains valid data in the upper byte only. This bit must always be 0 in byte mode (R68560).
0 Transmit full word (16 bits) from the TxFIFO.
1 Transmit upper byte (8 bits) from the TxFIFO.

TCR
3 TLAST —Transmit Last Character (BOP, BSC and COP only).
0 The next character is not the last character in a frame or block.
1 The next character to be written into the TDR is the last character of the message. The TLAST bit automatically returns to a 0 when the associated word/byte is written to the TxFIFO. If the transmitter DMA mode is enabled, TLAST is set to a 1 by $\overline{DONE}$ from the DMAC. In this case the character written into the TDR in the current cycle is the last character.

TCR
2 TSYN —Transmit SYN (BSC and COP only).
0 Do not transmit SYN characters.
1 Transmit SYN characters. Causes a pair of SYN characters to be transmitted immediately following the current character. If BSC transparent mode is active, a DLE SYN sequence is transmitted. The TSYN bit automatically returns to a 0 when the SYN character is loaded into the Transmitter Shift Register.

TCR
1 TABT —Transmit ABORT (BOP only).
0 Enable normal transmitter operation.
1 Causes an abort by sending eight consecutive 1's. A data word/byte must be loaded into the TxFIFO after setting this bit in order to complete the command. The TABT bit clears automatically when the subsequent data word/byte is loaded into the TxFIFO.

TCR
0 TRES —Transmitter Reset Command.
0 Enable normal transmitter operation.
1 Reset transmitter. Clears the transmitter section including the TxFIFO and the TSR (but not the TCR). The TxD output is held in "Mark" condition. TRES is set by $\overline{RESET}$ or by writing a 1 into this bit and is cleared by writing a 0 into this bit. TRES requires clearing after $\overline{RESET}$.

Transmit Data Register (TDR)

R68561 (Word Mode)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSB				Byte 1			LSB	MSB			Byte 0				LSB

Address = 0A

R68560 (Byte Mode)

7	6	5	4	3	2	1	0
MSB			Byte 0				LSB

Address = 0A

The transmitter has an 8-byte (or 4-word) FIFO register file (TxFIFO). Data to be transmitted is transferred from the bus into the TxFIFO via the TDR in 8-bit bytes or 16-bit words depending on the WD/BYT bit setting in PSR2. The TDRA status bit in the TSR is set to 1 when the TxFIFO is ready to accept another data word/byte.

Transmitter Interrupt Vector Number Register (TIVNR)

7	6	5	4	3	2	1	0
Transmitter Interrupt Vector Number (TIVN)							

Address = 0C Reset value = $0F

If a transmitter interrupt condition occurs (as reported by status bits in the TSR that correspond to interrupt enable bits in the TIER) and the corresponding bit in the TIER is set, the $\overline{IRQ}$ output is asserted to request MPU transmitter interrupt service. When the $\overline{IACK}$ input is asserted from the bus, the Transmitter Interrupt Vector Number (TIVN) from the Transmitter Interrupt Vector Number Register (TIVNR) is placed on the data bus.

Transmitter Interrupt Enable Register (TIER)

7	6	5	4	3	2	1	0
TDRA IE	TFC IE	0	0	0	TUNRN IE	TFERR IE	—

Address = 0D Reset value = $00

The Transmitter Interrupt Enable Register (TIER) contains interrupt enable bits for the Transmitter Status Register. When enabled, the $\overline{IRQ}$ output is asserted when the corresponding condition is detected and reported in the TSR.

TIER
7 TDRA IE —Transmitter Data Register (TDR) Available Interrupt Enable.
0 Disable TDRA Interrupt.
1 Enable TDRA Interrupt.

TIER
6 TFC IE —Transmit Frame Complete (TFC) Interrupt Enable.
0 Disable TFC Interrupt.
1 Enable TFC Interrupt.

TIER
5-3 —Not used.

TIER
2 TUNRN IE —Transmitter Underrun (TUNRN) Interrupt Enable.
0 Disable TUNRN Interrupt.
1 Enable TUNRN Interrupt.

TIER
1 TFERR IE —Transmit Frame Error (TFERR) Interrupt Enable.
0 Disable TFERR Interrupt.
1 Enable TFERR Interrupt.

TIER
0 —Not used.

SERIAL INTERFACE REGISTERS

Serial Interface Status Register (SISR)

7	6	5	4	3	2	1	0
CTST	DSRT	DCDT	CTSLVL	DSRLVL	DCDLVL	0	0

Address = 10 Reset value = $00

The Serial Interface Status Register (SISR) contains the serial interface status information. The transition status bits (CTST, DSRT and DCDT) are cleared by writing a 1 into their respective positions, or by RESET. The level status bits (CTSLVL, DSRLVL and DCDLVL) reflect the state of their respective inputs and cannot be cleared internally. The IRQ output is asserted if any of the conditions reported by the transition status bits occur and the corresponding interrupt enable bit in the SIER is set.

SISR
7 CTST —Clear to Send Transition Status.
0 The input on CTS has not transitioned positive.
1 The input on CTS has transitioned positive from active to inactive. To detect this transition, RTS must be active (low) and the transmitter must be enabled (TRES in TCR0 = 0). The CTST bit is set in SISR7 and an interrupt issued (if enabled) with the negative edge of TxC.

CTST Reset — A negative transition of the serial clock (TxC) must occur after the CTS input goes high before the CTST bit can be reset by writing a 1 to SISR7.

SISR
6 DSRT —Data Set Ready Transition Status.
0 The input on DSR has not transitioned negative.
1 The input on DSR has transitioned negative from inactive to active. The DSRT bit is set in SISR7 and an interrupt issued (if enabled) with the negative edge of RxC. The receiver must be enabled (RRES in RCR0 = 0).

DSRT Reset — A negative transition of the serial clock (RxC) must occur after the DSR input goes high before the DSRT bit can be reset by writing a 1 to SISR6.

SISR
5 DCDT —Data Carrier Detect Transition Status.
0 The input on DCD has not transitioned positive.
1 The input on DCD has transitioned positive from active to inactive. The DCDT bit is set in SISR5 and an interrupt issued (if enabled) with the negative edge of RxC. The receiver must be enabled (RRES in RCR0 = 0).

DCDT Reset — A negative transition of the serial clock (RxC) must occur after the DCD input goes high before the DCDT bit can be reset by writing a 1 to SISR5.

SISR
4 CTSLVL —Clear to Send Level.
0 The input on CTS is negated (high, inactive).
1 The input on CTS is asserted (low, active).

CRSLVL Reset — The CTSLVL bit in SISR4 follows the state of the input to CTS and cannot be reset internally.

SISR
3 DSRLVL —Data Set Ready Level.
0 The input on DSR is negated (high, inactive).
1 The input on DSR is asserted (low, active).

DSRLVL Reset — The DSRLVL bit in SISR3 follows the state of the input to DSR and cannot be reset internally.

SISR
2 DCDLVL —Data Carrier Detect Level.
0 The input on DCD is negated (high, inactive).
1 The input on DCD is asserted (low, active).

DCDLVL Reset — The DCDLVL bit in SISR2 follows the state of the input to DCD and cannot be reset internally.

SISR
1-0 —Not used.

Serial Interface Control Register (SICR)

7	6	5	4	3	2	1	0
RTSLVL	DTRLVL	0	0	0	ECHO	TEST	0

Address = 11 Reset value = $00

The Serial Interface Control Register (SICR) controls various serial interface signals and test functions.

SICR
7 RTSLVL —Request to Send Level.
0 Negate RTS output (high).
1 Assert RTS output (low).

NOTE

In BOP, BSC, or COP, when the RTSLVL bit is cleared in the middle of data transmission, the RTS output remains asserted until the end of the current frame or block has been transmitted. In ASYNC or ISOC, the RTS output is negated when the TxFIFO is empty. If the transmitter is idling when the RTSLVL bit is reset, the RTS output is negated within two bit times.

SICR
6 DTRLVL —Data Terminal Ready Level.
0 Negate DTR output (high).
1 Assert DTR output (low).

SICR
5-3 —Not used. These bits are initialized to 0 by RESET and must not be set to 1.

SICR
2 ECHO —Echo Mode Enable.
0 Disable Echo mode (enable normal operation).
1 Enable Echo mode. Received data (RxD) is routed back through the transmitter to TxD. The contents of the TxFIFO is undisturbed. This mode may be used for remote test purposes.

SICR
1 TEST —Self-test Enable.
0 Disable self-test (enable normal operation).
1 Enable self-test. The transmitted data (TxD) and clock (TxC) are routed back through to the receiver through RxD and RxC, respectively (DCD and CTS are ignored). This "loopback" self-test may be used for all protocols. RxC is external and CCR bits 2 and 3 must be a 1.

SICR
0 MUST BE ZERO
0

Serial Interrupt Vector Number Register (SIVNR)

7	6	5	4	3	2	1	0
Serial Interrupt Vector Number (SIVN)							

Address = 14 Reset value = $0F

If a serial interface interrupt condition occurs (as reported by status bits in the SISR that correspond to interrupt enable bits in the SIER) and the corresponding bit in the SIER is set, the $\overline{IRQ}$ output is asserted to request MPU serial interface interrupt service. When the $\overline{IACK}$ input is asserted from the bus, the Serial Interrupt Vector Number (SIVN) from the Serial Interrupt Vector Number Register (SIVNR) is placed on the data bus.

Serial Interrupt Enable Register (SIER)

7	6	5	4	3	2	1	0
CTS IE	DSR IE	DCD IE	0	0	0	0	0

Address = 15 Reset value = $00

The Serial Interrupt Enable Register (SIER) contains interrupt enable bits for the Serial Interface Status Register. When an interrupt enable bit is set, the $\overline{IRQ}$ output is asserted when the corresponding condition occurs as reported in the SISR.

SIER
7 **CTS IE —Clear to Send (CTS) Interrupt Enable.**
0 Disable CTS Interrupt.
1 Enable CTS Interrupt.

SIER
6 **DSR IE —Data Set Ready (DSR) Interrupt Enable.**
0 Disable DSR Interrupt.
1 Enable DSR Interrupt.

SIER
5 **DCD IE —Data Carrier Detect (DCD) Interrupt Enable.**
0 Disable DCD Interrupt.
1 Enable DCD Interrupt.

SIER
4-0 **—Not used.**

GLOBAL REGISTERS

The global registers contain command information applying to different modes of operation and protocols. After changing global register data, TRES in the TCR and RRES in the RCR should be set then cleared prior to performing normal mode processing.

Protocol Select Register 1 (PSR1)

7	6	5	4	3	2	1	0
0	0	0	0	0	0	CTLEX	ADDEX

Address = 18 Reset value = $00

Protocol Select Register 1 (PSR1) selects BOP protocol related options.

PSR1
7-2 **—Not used.**

PSR1
1 **CTLEX —Control Field Extend (BOP only).**
0 Select 8-bit control field.
1 Select 16-bit control field.

PSR1
0 **ADDEX —Address Extend (BOP only).**
0 Disable address extension. All eight bits of the address byte are utilized for addressing.
1 Enable address extension. When bit 0 in the address byte is a 0 the address field is extended by one byte. An exception to the address field extension occurs when the first address byte is all 0's (null address).

Protocol Select Register 2 (PSR2)

7	6	5	4	3	2	1	0
WD/BYT	STOP BIT SEL		CHAR LEN SEL		PROTOCOL SEL		
	SB2	SB1	CL2	CL1	PS3	PS2	PS1

Address = 19 Reset value = $00

Protocol Select Register 2 (PSR2) selects protocols, character size, the number of stop bits, and word/byte mode.

PSR2
7 **WD/BYT —Data Bus Word/Byte Mode.**
0 Select byte mode. Selects the number of data bits to be transferred from the RxFIFO and the registers to the data bus and to be transferred from the data bus to the TxFIFO and the registers. The MPCC is initialized by $\overline{RESET}$ to the byte mode.
1 Select word mode. For operation with the 16-bit bus, select the word mode by sending $80 on D7–D0 to address $19 prior to transferring subsequent data between the MPCC and the data bus.

PSR2
6-5 **STOP BIT SEL —Number of Stop Bits Select.** Selects the number of stop bits transmitted at the end of the data bits in ASYNC and ISOC modes.

6 SB2	5 SB1	No. of Stop Bits ASYNC	ISOC
0	0	1	1
0	1	1-1/2	2
1	0	2	2

PSR2

4-3 CHAR LEN SEL —Character Length Select. Selects the character length except in BOP and BSC where the character length is always eight bits. Parity is not included in the character length.

4 CL2	3 CL1	Character Length
0	0	5 bits
0	1	6 bits
1	0	7 bits
1	1	8 bits

PSR2

2-0 PROTOCOL SEL—Protocol Select. Selects protocol and defines the protocol dependent control bits.

2 PS3	1 PS2	0 PS1	Protocol
0	0	0	BOP (Primary)
0	0	1	BOP (Secondary)
0	1	0	Reserved
0	1	1	COP
1	0	0	BSC EBCDIC
1	0	1	BSC ASCII
1	1	0	ASYNC
1	1	1	ISOC

Address Register 1 (AR1) Address

7	6	5	4	3	2	1	0
BOP ADDRESS/BSC & COP PAD							

Address = 1A Reset value = $00

Address Register 2 (AR2)

7	6	5	4	3	2	1	0
BSC & COP SYN							

Address = 1B Reset value = $00

The protocol selected in PSR2 (BOP, BSC and COP only) determines the function of the two 8-bit Address Registers (AR1 and AR2). As a secondary station in BOP, the contents of AR1 is used for address matching. In BSC and COP, AR1 and AR2 contain programmable leading PAD and programmable SYN characters, respectively.

Address Register (AR) Contents

Protocol Selected	AR1	AR2
BOP (Primary)	X	X
BOP (Secondary)	Address	X
BSC EBCDIC	Leading PAD	SYN
BSC ASCII	Leading PAD	SYN
COP	Leading PAD	SYN
*X = Not used		

Baud Rate Divider Register 1 (BRDR1)

7	6	5	4	3	2	1	0
BAUD RATE DIVIDER (LSH)							

Address = 1C Reset value = $01

Baud Rate Divider Register 2 (BRDR2)

7	6	5	4	3	2	1	0
BAUD RATE DIVIDER (MSH)							

Address = 1D Reset value = $00

The two 8-bit Baud Rate Divider Registers (BRDR1 and BRDR2) hold the divisor of the Baud Rate Divider circuit. BRDR1 contains the least significant half (LSH) and BRDR2 contains the most significant half (MSH), With an 8.064 MHz EXTAL input, standard bit rates can be selected using the combination of Prescaler Divider (in the CCR) and Baud Rate Divider values shown in Table 3. For isochronous or synchronous protocols, the Baud Rate Divider value must be multiplied by two for the same Prescaler Divider value.

The Baud Rate Divider (BRD) value can be computed for other crystal frequency, prescaler divider and desired baud rate values as follows:

$$BRD = \frac{\text{Crystal Frequency}}{\text{(Prescaler Divider) (Baud Rate) (K)}}$$

where: K = 1 for isochronous or synchronous
2 for asynchronous

Clock Control Register (CCR)

7	6	5	4	3	2	1	0
0	0	0	PSCDIV	TCLKO	RCLKIN	CLK DIV	
						CK2	CK1

Address = 1E Reset value = $00

The CCR selects various clock options.

CCR
7-5 —Not used.

CCR
4 PSCDIV —Prescaler Divider. The Prescaler Divider network reduces the external/oscillator frequency to a value for use by the internal Baud Rate Generator.
0 Divide by 2.
1 Divide by 3.

CCR
3 TCLKO —Transmitter Clock Output Select.
0 Select TxC to be an input.
1 Select TxC to be an output. (1X clock)

Table 3. Standard Baud Selection (8.064 MHz Crystal)

Desired Baud Rate (Bit Rate)	Prescaler Divider		Baud Rate Divider					
			Asynchronous			Isochronous and Synchronous		
				Hexadecimal Value			Hexadecimal Value	
	Decimal Value	PSCDIV (0 to 1)	Decimal Value	BRDR2 (MSH)	BRDR1 (LSH)	Decimal Value	BRDR2 (MSH)	BRDR1 (LSH)
50	3	1	26,880	69	00	53,760	D2	00
75	2	0	26,880	69	00	53,760	D2	00
110	3	1	12,218	2F	BA	24,436	5F	74
135	2	0	14,933	3A	55	29,866	74	AA
150	3	1	8,960	23	00	17,920	46	00
300	2	0	6,720	1A	40	13,440	34	80
1200	3	1	1,120	04	60	2,240	08	C0
1800	2	0	1,120	04	60	2,240	08	C0
2400	2	0	840	03	48	1,680	06	90
3600	2	0	560	02	30	1,120	04	60
4800	3	1	280	01	18	560	02	30
7200	2	0	280	01	18	560	02	30
9600	3	1	140	00	8C	280	01	18
19200	3	1	70	00	46	140	00	8C
38400	3	1	35	00	23	70	00	46

CCR
2 RCLKIN —Receiver Clock Internal Select (ASYNC only).
0 Select External RxC.
1 Select Internal RxC.

CCR
1-0 CLK DIV —External Receiver Clock Divider. Selects the divider of the external RxC to determine the receiver data rate.

CK2	CK1	Divider	
0	0	1	(ISOC)
0	1	16	(ASYNC) only
1	0	32	
1	1	64	

Error Control Register (ECR)

7	6	5	4	3	2	1	0
PAREN	ODDPAR	—	—	CFCRC	CRCPRE	CRCSEL	
						CR2	CR1

Address = 1F Reset value = $04

The Error Control Register (ECR) selects the error detection method used by the MPCC.

ECR
7 PAREN —Parity Enable. (ASYNC, ISOC and COP only).
0 Disable parity generation/checking.
1 Enable parity generation/checking.

ECR
6 ODDPAR —Odd/Even Parity Select (Effective only when PAREN = 1).
0 Generate/check even parity.
1 Generate/check odd parity.

ECR
5-4 —Not used.

ECR
3 CFCRC —Control Field CRC Enable. (BOP Only)
0 Disable control field CRC.
1 Enables an intermediate CRC remainder to be appended after the address/control field in transmitted BOP frames and checked in received frames. The CRC generator is reset after control field CRC calculation.

ECR
2 CRCPRE —CRC Generator Preset Select. (BOP, BSC Only)
0 Preset CRC Generator to 0. (For BSC)
1 Preset CRC Generator to 1 and transmit the 1's complement of the resulting remainder. (For BOP)

ECR
1-0 CRCSEL —CRC Polynomial Select. Selects one of the RC polynominals.

1 CR2	0 CR1	Polynominal
0	0	$x^{16}+x^{12}+x^5+1$ (CCITT V.41) (BOP)
0	1	$x^{16}+x^{15}+x^2+1$ (CRC-16) (BSC)
1	0	x^8+1 (VRC/LRC)* (BSC, ASCII, non-transparent)
1	1	Not used.

*VRC: Odd-parity check is performed on each character including the LRC character.

INPUT/OUTPUT FUNCTIONS

MPU INTERFACE

Transfer of data between the MPCC and the system bus involves the following signals:

	R68561	R68560
Address Lines	A1–A4	A0–A4
Data Lines	D0–D15	D0–D7
Read/Write	R/$\overline{W}$	R/$\overline{W}$
Data Transfer Acknowledge	$\overline{DTACK}$	$\overline{DTACK}$
Chip Select	$\overline{CS}$	$\overline{CS}$
Data Strobes	$\overline{UDS}$ and $\overline{LDS}$	$\overline{DS}$

Figures 10 and 11 show typical interface connections.

Read/Write Operation

The R/$\overline{W}$ input controls the direction of data flow on the data bus. $\overline{CS}$ (Chip Select) enables the MPCC for access to the internal registers and other operations. When $\overline{CS}$ is asserted, the data I/O buffer acts as an output driver during a read operation and as an input buffer during a write operation. $\overline{CS}$ must be decoded from the address bus and gated with address strobe ($\overline{AS}$).

When the R68561 is connected to the 16-bit bus for operation in the word mode (WD/BYT = 1 in the PSR2), address lines A1–A4 select the internal register(s) (the 8-bit control/status registers are accesed two at a time and the 16-bit data registers are accessed on even address boundaries). When the MPCC is selected ($\overline{CS}$ low) during a read (R/$\overline{W}$ high), 16 bits of register data are placed on the data bus when the data strobes ($\overline{LDS}$ and $\overline{UDS}$) are asserted. $\overline{LDS}$ strobes the eight data bits from the even numbered registers to the lower data bus lines (D0–D7) and $\overline{UDS}$ strobes the eight data bits from the odd numbered registers to the upper data bus lines (D8–D15). The MPCC asserts Data Transfer Acknowledge ($\overline{DTACK}$) prior to placing data on the data bus. Conversely, when the MPCC is selected ($\overline{CS}$ low) during a write (R/$\overline{W}$ low) $\overline{LDS}$ and $\overline{UDS}$ strobe data from the D0–D7 and D8–D15 data bus lines into the addressed even and odd numbered registers, respectively, and the MPCC asserts $\overline{DTACK}$. $\overline{DTACK}$ is negated when $\overline{CS}$ is negated. Figures 12 and 13 show the read and write timing relationships.

When the R68560 is connected to the 8-bit bus for operation in the byte mode (WD/BYT = 0 in the PSR2), address lines A0–A4 select one internal 8-bit register. When the MPCC is selected ($\overline{CS}$ low) during a read (R/$\overline{W}$ high), eight bits of register data are placed on data bus lines D0–D7 when the data strobe ($\overline{DS}$) is asserted. When the MPCC is selected ($\overline{CS}$ low) for a write (R/$\overline{W}$ low), $\overline{DS}$ strobes data from the D0–D7 data lines into the selected register.

DMA INTERFACE

The MPCC is capable of providing DMA data transfers at up to 2 Mbytes per second when used with the MC68440 or MC68450 DMAC in the single address mode. Based on 4 Mb/s serial data rate and 5 bits/character, the maximum DMA required transfer rate is 800 Kbytes per second.

The MPCC has separate DMA enable bits for the transmitter and receiver, each of which requires a DMA channel. Both the transmitter and receiver data are implicitly addressed (TDR or RDR) therefore addressing of the data register is not required before data may be transferred. Communication between the MPCC and the DMAC is accomplished by a two-signal request/acknowledge handshake. Since the MPCC has only one acknowledge input ($\overline{DACK}$) for its two DMA request lines, an external OR function must be provided to combine the two DMA acknowledge signals. The MPCC uses the R/$\overline{W}$ input to distinguish between the Transmitter Data Service Request ($\overline{TDSR}$ acknowledge and the Receiver Data Service Request ($\overline{RDSR}$) acknowledge.

Receiver DMA Mode

The receiver DMA mode is enabled when the RDSREN bit in the RCR is set to 1. When data is available in the RxFIFO, Receiver Data Service Request ($\overline{RDSR}$) is asserted for one receiver clock period (BOP and BSC) to initiate the MPCC to memory DMA transfer. For asynchronous operation, $\overline{RDSR}$ is asserted for 2–3 periods of the system clock depending on prescale factor. The next $\overline{RDSR}$ cycle may be initiated as soon as the current $\overline{RDSR}$ cycle is completed (i.e., a full sequence of $\overline{DACK}$, $\overline{DS}$, and $\overline{DTC}$).

In response to $\overline{RDSR}$ assertion, the DMAC sets the R/$\overline{W}$ line to write, asserts the memory address, address strobe, and DMA acknowledge. The MPCC outputs data from the RxFIFO to the data bus and the DMAC asserts the data strobes. The memory latches the data and asserts $\overline{DTACK}$ to complete the data transfer. The DMAC asserts $\overline{DTC}$ to indicate to the MPCC that data transfer is complete. Figure 14 shows the timing relationships for the receiver DMA mode.

$\overline{RDSR}$ is inhibited when either RDSREN is reset to 0 or RRES is set to 1 (both in the RCR), or when $\overline{RESET}$ is asserted.

Transmitter DMA Mode

The transmitter DMA mode is enabled when the TDSREN bit in the TCR is set to 1. When the TxFIFO is available, Transmitter Data Service Request ($\overline{TDSR}$) is asserted for one transmitter clock period to initiate the memory to MPCC DMA transfer. For asynchronous operation, $\overline{TDSR}$ is asserted for a period of one-half the transmitter baud rate. The next $\overline{TDSR}$ cycle may be initiated as soon as the current $\overline{TDSR}$ cycle is completed.

In the transmitter DMA mode, the TxFIFO Is implicitly addressed. That is, when the transfer is from memory to the TxFIFO, only the memory is addressed. In response to $\overline{TDSR}$ assertion, the DMAC sets the R/$\overline{W}$ line to read, asserts the memory address, the address strobe, the data strobes and DMA acknowledge. The memory places data on the data bus and asserts $\overline{DTACK}$. Data is valid at this time and will remain valid until the data strobes are negated. The DMAC asserts $\overline{DTC}$ to indicate to the MPCC that data is available. The MPCC loads the data into the TxFIFO on the negation (rising edge) of $\overline{DS}$ and the transfer is complete. When a TxFIFO underrun occurs, the TUNRN bit is set in TSR2, the interrupt is issued, and the ABORT sequence is entered (eight consecutive 1s are transmitted). The next word/byte in TxFIFO clears the ABORT bit and the idle mode is entered. When a transmission is aborted, it is expected that the interrupt will allow the host system to decide the next course of action; probably to reset the DMAC and retransmit the message. A timing diagram for the transmitter DMA Mode is shown in Figure 15.

$\overline{TDSR}$ is inhibited when either TDSREN is reset to 0 or TRES is set to 1 (both in the TCR), or when $\overline{RESET}$ is asserted.

$\overline{\text{DONE}}$ Signal

When the DMA transfer count is exhausted in transmitter DMA mode, the DMAC asserts $\overline{\text{DONE}}$ which sets the TLAST bit in the TCR to indicate that the last word/byte has been transferred. In the receiver DMA mode of operation, $\overline{\text{DONE}}$ is issued by the MPCC on an MPCC-to-memory transfer when the last byte/word is being transferred from the RxFIFO to the data bus (if DONEEN bit is set in RCR5). In the byte mode, this is the Frame Status Byte (FSB). In the word mode, this is the last data byte and FSB (for an odd number of data byte transfers) or FSB and blank (for an even number of data byte transfers).

$\overline{\text{DONE}}$ is asserted as a result of the FSB being transferred and not as a result of the error conditions. The EOF, C/PERR and FRERR are addendum bits in the RxFIFO which are written to FIFO when they occur and follow the data through the FIFO. The frame is aborted upon overrun or error detection if RCR1 = 1.

CAUTION

$\overline{\text{DONE}}$ is reasserted with each occurrence of $\overline{\text{DACK}}$ until EOF is cleared in the RSR.

INTERRUPTS

If an interrupt generating status occurs and the interrupt is enabled, the MPCC asserts the $\overline{\text{IRQ}}$ output. Upon receiving $\overline{\text{IACK}}$ for the pending interrupt request, the MPCC places an interrupt vector on D0-D7 data bus and asserts $\overline{\text{DTACK}}$.

The MPCC has three vector registers: Receiver Interrupt Vector Number Register (RIVNR), Transmitter Interrupt Vector Number Register (TIVN), and Serial Interrupt Vector Number Register (SIVNR). The receiver interrupt has priority over the transmitter interrupt, and the transmitter interrupt has priority over the serial interface interrupt. For example, if a pending interrupt request has been generated simultaneously by the receiver and the transmitter, the Receiver Interrupt Vector Number (RIVN) is placed on D0-D7 when acknowledged by the MPU. Upon completion of the first interrupt request cycle (which clears the receiver interrupt), $\overline{\text{IRQ}}$ will remain low to start the transmitter interrupt cycle. $\overline{\text{IRQ}}$ is negated by clearing all bits set in a status register that could have caused the interrupt.

CAUTION

A higher priority interrupt occuring while $\overline{\text{IACK}}$ is low during transfer of a lower priority interrupt vector to the MPU will cause the lower priority interrupt vector on the data bus to be invalid if there are any 1's in the higher priority interrupt vector in the same bit poositions as any 0's in the lower priority interrupt vector. To prevent this problem from occuring, ensure that the higher priority interrupt vectors contain 1's only in bit positions where there are 1's in the lower priority interrupt vectors, e.g.:

Vector	Vector Value (Hex)	Vector Value (Binary)
Receiver Interrupt Vector Number (RIVN)	44	01000100
Transmitter Interrupt Vector Number (TIVN)	4C	01001100
Serial Interrupt Vector Number (SIVN)	5C	01011100

A timing diagram for the interrupt acknowledge sequence is shown in Figure 16.

SERIAL INTERFACE

The MPCC is a high speed, high performance device supporting the more popular bit and character oriented data protocols. The lower speed asynchronous (ASYNC) and isochronous (ISOCH) modes are also supported. An on-chip clock oscillator and baud rate generator provide an output data clock at a frequency of DC to a 4 MHz.. The clock can also be used in the ASYNC mode to provide a receive clock for the incoming data. The serial interface consists of the following signals:

$\overline{\text{RTS}}$ (Request to Send) Output

The $\overline{\text{RTS}}$ output to the DCE is controlled by the RTSLVL bit in the SICR inn conjunction with the state of the transmitter section. When the RTSLVL bit is set to 1, the $\overline{\text{RTS}}$ output is asserted. When the RTSLVL bit is reset to 0 (no sooner than one full cycle of TxC after transmission has started), the $\overline{\text{RTS}}$ output remains asserted until the TxFIFO becomes empty, or the end of the message (or frame), complete with CRC code (if any), closing flag, and one full cycle of idle has been transmitted. $\overline{\text{RTS}}$ also is negated when the RTSLVL bit is reset during transmitter idle, or when the $\overline{\text{RESET}}$ input is asserted.

$\overline{\text{CTS}}$ (Clear to Send) Input

The CTS input signal is normally generated by the DCE to indicate whether or not the data set is ready to receive data. The CTST bit in the SISR reflects the transition status of the $\overline{\text{CTS}}$ input while the CTSLVL bit in the SISR reflects the current level. A positive transition on the $\overline{\text{CTS}}$ pin asserts $\overline{\text{IRQ}}$ if the CTS IE bit in the SIER is set. The $\overline{\text{CTS}}$ input in an inactive state disables the start of transmission of each frame.

$\overline{\text{DCD}}$ (Data Carrier Detect) Input

The $\overline{\text{DCD}}$ input signal is normally gnerated by the DCE and indicates that the DCE is receiving a data carrier signal suitable for demodulation. The DCDT bit in the SISR reports the transition status of the $\overline{\text{DCD}}$ input while the DCDLVL bit in the SISR contains the current level. A positive transition on the $\overline{\text{DCD}}$ pin asserts the $\overline{\text{IRQ}}$ output if the DCD IE bit in the SIER is set. A negated $\overline{\text{DCD}}$ input disables the start of the receiver but does not stop the operation of an incoming message already in progress.

$\overline{DSR}$ (Data Set Ready) Input/RSYN Output

The DSRT input from the DCE indicates the status of the local set. The DSRT bit in the SISR contains the transition status of the $\overline{DSR}$ input while the DSRLVL bit in the SISR reports the current level. A negative transition on the $\overline{DSR}$ pin asserts the $\overline{IRQ}$ output if the DSR IE bit in the SIER is set.

The $\overline{DSR}$ pin is used as an output for RSYN when enabled by a 1 in RSR4 (RSYNEN = 1). DSR output low indicates detection of a SYN (non-transparent) in BSC or COP protocols or DLE-SYN pair (transparent) in BSC protocol. It is asserted as a negative-going pulse one-bit time after the end of the SYN byte and lasts for one full serial clock cycle before being reset.

In BOP protocol, RSYN is asserted as a result of address match at the beginning of a frame. It is asserted one bit time after the end of the address byte(s) if an address match is made, and lasts for one full serial clock cycle.

$\overline{DTR}$ (Data Terminal Ready) Output

The $\overline{DTR}$ output is general purpose in nature and can be used to control switching of the DCE. The $\overline{DTR}$ output is controlled by the DTRLVL bit in the SICR.

TxC (Transmitter Clock) Input/Output

The transmitter clock (TxC) may be programmed to be input or an output. When the TCLKO control bit in the CCR is set to a 1, the TxC pin becomes an output and provides the DCE with a clock whose frequency is determined by the internal baud rate generator. When the TCKLO control bit is reset, TxC is an input and the transmitter shift timing must be provided exernally. The TxD output changes state on the negative-going edge of the transmitter clock. In the asynchronous mode when TCLKO = 0 in the CCR, the TxC input frequency must be two times the desired baud rate.

TxD (Transmitted Data) Output

The serial data transmitted from the MPCC is coded in NRZ data format. The first byte of a message transmitted out of the R68561 MPCC is the even byte of the 68000 bus (D8–D15). It is transmitted least significant bit (LSB) first.

RxC (Receiver Clock) Input

The receiver latches data on the negative transition of the RxC.

RxD (Received Data) Input

The serial data received by the MPCC is in NRZ data format. The first byte received in the MPCC RXFIFO is output to the 68000 bus on (D8–D15).

Serial Interface Timing

The timing for the serial interface clock and data lines is shown in Figure 18. The MPCC supports high speed synchronous operation. As shown, the TxD output changes with the negative-going edge of TxC and the received data on RxD is latched on the negative edge of RxC. This assures high speed two-way operation between two MPCCs connected as shown in Figure 17.

For low speed operation between the MPCC and a modem or RS-232C Data Communications Equipment (DCE), an inverter can be used in the TxC output lines as shown in Figure 17. RS-232 and RS-423 (covering serial data interface up to 100K baud) require that data be centered ±25% about the negative-going edge of the RxC. This criteria is met for frequencies up to 1.25 MHz using the inverter. Use of the inverter also allows MPCC to MPCC operation up to 2.17 MHz.

SERIAL COMMUNICATION MODES AND PROTOCOLS

ASYNCHRONOUS AND ISOCHRONOUS MODES

Asynchronous and isochronous data are transferred in frames. Each frame consists of a start bit, 5 to 8 data bits plus optional even or odd parity, and 1, 1½, or 2 stop bits. The data character is transmitted with the least significant bit (LSB) first. The data line is normally held high (MARK) between frames, however, a BREAK (minimum of one frame length for which the line is held low) is used for control purposes. Figure 4 illustrates the frame format supported by the MPCC.

Asynchronous Receive

In the asynchronous (ASYNC) mode, data reception on RxD occurs in three phases: (1) detection of the start bit and bit synchronization, (2) character assembly and optional parity check, and (3) stop bit detection. The receiver bit stream may be synchronized by the internal baud rate generator clock or by an external clock on RxC. When RCLKIN in the CCR is set to 0, an external clock with a frequency of 16, 32, or 64 times the data rate establishes the data bit midpoint and maintains bit synchronization. The character assembly process does not start if the start bit is less than one-half bit time. Framing and parity errors are detected and buffered along with the character on which errors occurred. They are passed on to the RxFIFO and set appropriate status bits in the RSR when the character with an error reaches the last RxFIFO register where it is ready to be transferred onto the data bus via the RDR.

Isochronous Receive

In the isochronous (ISOC) mode, a times 1 clock on RxC is required with the data on RxD and the serial data bit is latched on the falling edge of each clock pulse. The requirement for the detection of a valid start bit, or the beginning of a break, is satisfied by the detection of a high-to-low transition on the serial data input line. Error detection and status indication are the same as the asynchronous mode.

Asynchronous and Isochronous Transmit

In asynchronous and isochronous transmit modes, output data transmission on TxD begins with the start bit. This is followed by the data character which is transmitted LSB first. If parity generation is enabled, the parity bit is transmitted after the MSB of the character. Each frame is terminated with 1, 1½ or 2 stop bits as selected by PSR2 bits 5 and 6.

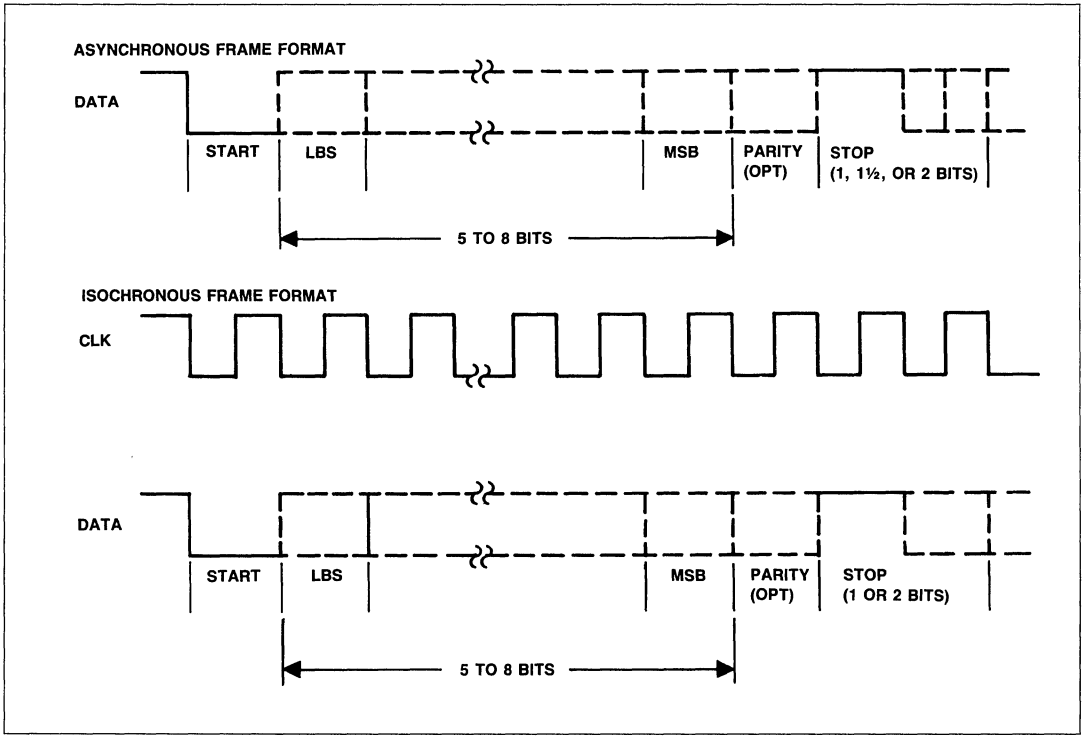


Figure 4. Asynchronous and Isochronous Frame Format

SYNCHRONOUS MODES

In synchronous modes, a times one clock is provided along with the data. Serial output data is shifted out and input data is latched on the falling edge of the clock.

BIT ORIENTED PROTOCOLS (BOP)

In bit oriented protocols (BOP), messages (data) are transmitted and received in frames. Each frame contains an opening flag, address field, control field, frame check sequence, and a closing flag. A frame may also contain an information field. (See Figure 5).

The opening flag is a special character whose bit pattern is 01111110. It marks the frame boundaries and is the interframe fill character. The address field of a frame contains the address of the secondary station which is receiving or responding to a command. The address field may be one or more bytes long. The address field can be extended by setting the ADDEX bit to a 1 in PSR1. In this case, the address field will be extended until the occurrence of an address byte with a 1 in bit 0. The first byte of the address field is automatically checked when the MPCC is programmed to be a secondary station in BOP. An automatic check for global (11111111) or null (00000000) address is also made. The control field of one or two bytes is transparent to the MPCC and sent directly to the host without interpretation.

The optional information field consists of 8-bit characters. Cyclic redundancy checking is used for error detection and the CRC remainder resulting from the calculation is transmitted as the frame check sequence field. For BOP, the polynomial $X^{16} + X^{12} + X^5 + 1$ (CRC-CCITT) should be used, i.e., selected in the CRC SEL bits in the ECR. The registers representing the CRC-CCITT polynomial are generally preset to all 1s, and the 1s complement of the resulting remainder is transmitted. (See X.25 Recommendation.)

FLAG 01111110	ADDRESS 1 OR N BYTES	CONTROL 1 OR 2 BYTES	INFORMATION N BYTES (OPTIONAL)	FCS 2 BYTES	FLAG 01111110

Figure 5. Bit Oriented Protocol (BOP) Frame Format

Zero insertion/deletion is employed to prevent valid frame data from being confused with the special characters. A 0 is inserted by the transmitter after every fifth consecutive 1 in the data stream. These inserted zeros are removed by the receiver to restore the data to its original form. The inserted zeros are not included in the CRC calculation.

The end of the frame is determined by the detection of the closing Flag special character which is the same is the opening Flag.

With the control options offered by the MPCC, commonly used bit oriented protocols such as SDLC, HDLC and X.25 standards can be supported. Figure 6 compares the requirements of these options.

BOP Receiver Operation

In BOP, the receiver starts assembling characters and accumulating CRC immediately after the detection of a Flag. The receiver also continues to search for additional Flag, or Abort, characters on a bit-by-bit basis. Zero deletion is implemented in the Receiver Shift Register after the Flag detection logic and before the CRC circuitry. The receiver recognizes the shared flag (the closing flag for one frame serves as the opening flag for the next frame) and the shared zero (the ending 0 of a closing flag serves as the beginning 0 of an opening flag forming the pattern "011111101111110."

Character assembly and CRC accumulation are stopped when a closing Flag or Abort is detected. The CRC accumulation includes all the characters between the opening Flag and the closing Flag. The contents of the CRC register are checked at the close of a frame and the C/PERR bit in the RSR is updated. The FCS and the Flag are not passed on to the RxFIFO.

If the Flag is a closing flag, checks for short frame (no control field) and CRC error conditions are made and the appropriate status is updated. When an Abort (seven 1s) is detected, the remaining frame is discarded and the RA/B bit is set in the RSR. When a link idle (15 or more consecutive 1s) is detected, the RIDLE status bit is set in the RSR. The zeros that have been inserted to distinguish data from special characters are detected and deleted from the data stream before characters are assembled. The MPCC programmed as a secondary station provides automatic address matching of the first byte. If there is no address match, or if null address is received, the receiver ignores the remainder of the frame by searching for the Flag. If there is a match, the address bytes are transferred to the RxFIFO as they are assembled.

For the control field, one or two bytes are assembled and passed on to the RxFIFO depending on the state of the extended control field bit.

If the CFCRC bit in the ECR is set to 1, an intermediate CRC check will be made after the address and control field. The Frame Check Sequence is still calculated over the remainder of the frame.

BOP Transmitter Operation

In BOP, the TxFIFO can be preloaded through the TDR while the transmitter is disabled (TEN = 0 in the TCR). When the transmitter is enabled (TEN = 1 in the TCR), the leading Flag is automatically sent prior to transmitting data from the TxFIFO. The TDRA bit is set to 1 in the TSR as long as TxFIFO is not full. If an underrun occurs, the TUNRN bit in the TSR is set to a 1 and an Abort (11111111) is transmitted followed by continuous Flags or marks until a new sequence is initiated.

The TLAST bit in the TCR must be set prior to loading the last character of the message to signal the transmitter to append the two-byte Frame Check Sequence (FCS) following the last character. If the transmitter DMA mode is selected (the TDSREN bit set to 1 in the TCR) the TLAST bit is set by the $\overline{\text{DONE}}$ signal from the DMAC.

A message may be terminated at any time by setting the TABT bit in the TCR to 1. This causes the transmitter to send an Abort character followed by the remainder of the current frame data in the TxFIFO.

The serial data from the Transmitter Shift Register is continuously monitored for five consecutive 1s, and a 0 is inserted in the data stream each time this condition occurs (excluding Flag and Abort characters).

CRC accumulation begins with the first non-Flag character and includes all subsequent characters. The CRC remainder is transmitted as the FCS following the last data character. If the CTLCRC bit in the ECR is set to 1, an intermediate CRC remainder is appended after the Address and Control field. The final Frame Check Sequence is calculated over the balance of the frame.

IBM SDLC FRAME FORMAT

FLAG 01111110	ADDRESS 1 BYTE	CONTROL 1 BYTE	INFORMATION N BYTES	FCS 2 BYTES	FLAG 01111110

HDLC FRAME FORMAT

FLAG 01111110	ADDRESS N BYTES	CONTROL 1 OR 2 BYTES	INFORMATION N BYTES	FCS 2 BYTES	FLAG 01111110

Figure 6. Bit Oriented Protocols

LEADING PAD 1 BYTE (AR1)	SYN 1 BYTE (AR2)	SYN 1 BYTE (AR2)	BODY	BCC	TRAILING PAD 11111111

Figure 7. BSC Block Format

BISYNC (BSC)

The structure of messages utilizing the IBM Binary Synchronous Communications (BSC) protocol, commonly called Bisync, is shown in Figure 7. The MPCC can process both transparent and nontransparent messages using either the EBCDIC or the ASCII codes. The CRC-16 polynomial should be selected by setting the appropriate CRCSEL bits in the ECR for both transparent and non-transparent EBCDIC and for transparent ASCII coded messages. VRC/LRC should be selected for non-transparent ASCII coded messages. BSC messages are formatted using defined data-link control characters. Data-link control characters generated and recognized by the MPCC are listed in Table 4.

Table 4. BSC Control Sequences—Inclusion in CRC Accumulation

ASCII			EBCDIC		
Command	**Byte 1**	**Byte 2**	**Command**	**Byte 1**	**Byte 2**
SYN	16*	—	SYN	32*	—
SOH	01	—	SOH	01	—
STX	02	—	STX	02	—
ETB	17	—	EOB (ETB)	26	—
ETX	03	—	ETX	03	—
ENQ	05	—	ENQ	2D	—
DLE	10	—	DLE	10	—
ITB	1F	—	ITB	1F	—
EOT	04	—	EOT	37	—
ACK N*	10	30-37	ACK 0	10	70
NAK	15	—	ACK 1	10	61
WACK	10	3B	NAK	3D	—
RVI	10	3C	WACK	10	6B
			RVI	10	7C

Note: *Programmable

A heading is a block of data starting with an SOH and containing one or more characters that are used for message control (e.g., message identification, routing, and priority). The SOH initiates the block-check-character (BCC) accumulation, but is not included in the accumulation. The heading is terminated by STX when it is part of a block containing both heading and text. A block containing only a heading is terminated with an ITB or an ETB followed by the BCC. Only the first SOH or STX in a transmission block following a line turnaround causes the BCC to reset. All succeeding STX or SOH characters are included in the BCC. This permits the entire transmission (excluding the first SOH or STX) to be block-checked.

The text data is transmitted in complete units called messages, which are initiated by STX and concluded with ETX. A message can be subdivided into smaller blocks for ease in processing and more efficient error control. Each block starts with STX and ends with ETB (except for the last block of a message, which ends with ETX). A single transmission can contain any number of blocks (ending with ETB) or messages (ending with ETX). An EOT following the last ETX block indicates a normal end of transmission. Message blocking without line turnaround can be accomplished by using ITB (see the Additional Data Link Capabilities section, IBM GA 27-3004-2).

Two modes of data transfers are used in BSC. In non-transparent mode, data link control characters may not appear as text data. In transparent mode, each control character is preceded by a data link escape (DLE) character to differentiate it from the text data. Table 5 indicates which control characters are excluded in the CRC generation. All characters not shown in the table are included in the CRC generation. Figure 8 shows various formats for Control/Response Blocks and Heading and Text Blocks.

Table 5. Transparent Mode BSC Control Sequences — Inclusion in CRC Accumulation

Character of Sequence	Included in CRC Accumulation	
	Yes	**No**
TSYN	—	DLESYN
TSOH	—	DLESOH
TSTX*	—	DLESTX
TETB	ETB	DLE
TETX	ETX	DLE
TDLE	(DLE)DLE	DLE(DLE)

*If not preceded within the same block by transparent heading information.

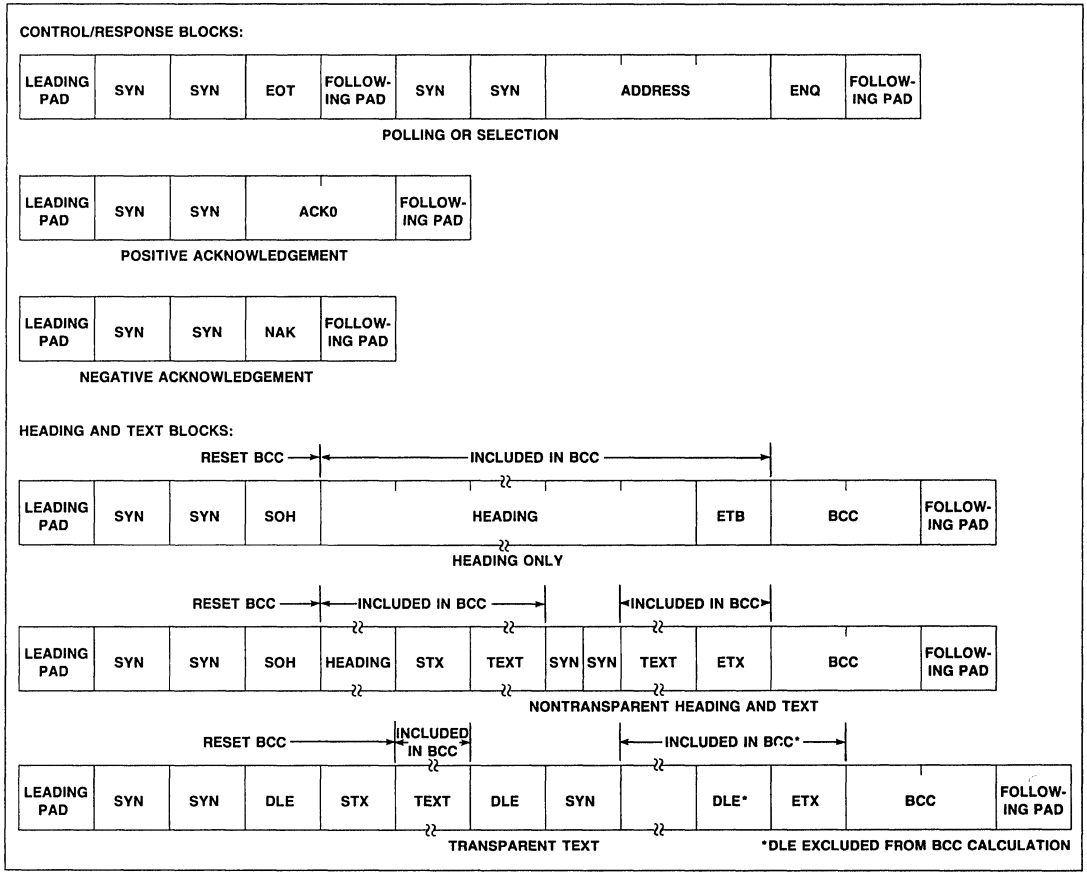


Figure 8. BSC Message Format Examples

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BSC Receiver Operation

Character length defaults to eight bits in BSC mode. When ASCII is selected, the eighth bit is used for parity provided that VRC/LRC polynomial is selected. Character assembly starts after the receipt of two consecutive SYN characters. Serial data bits are shifted through the Receiver Shift Register into the Serial-to-Parallel Register and transferred to the RxFIFO. The RDA status bit in the RSR is set to 1 each time data is transferred to the RxFIFO. The SYN character pairs in non-transparent mode and DLE-SYN pairs in transparent mode are discarded.

The receiver starts each block in the non-transparent mode. It switches to transparent mode if a block begins with a DLE-SOH or DLE-STX pair. The receiver remains in transparent mode until a DLE-ITB, DLE-ETB, DLE-ETX or DLE-ENQ pair is received. BCC accumulation begins after an opening SOH, STX, or DLE-STX. SYN characters in non-transparent mode or DLE-SYN pairs in transparent mode are excluded from the BCC accumulation. The first DLE of a DLE-DLE sequence is not included in the BCC accumulation and is discarded. The BCC is checked after receipt of an ITB, ETB, or ETX in non-transparent mode or DLE-ITB, DLE-ETB, DLE-ETX in transparent mode. If a CRC error is detected, the C/PERR and EOF bits in the RSR are set to 1. If no error is detected only the EOF bit is set. If the closing character was an ITB, BCC accumulation and character assembly starts again on the first character following the BCC.

BSC Transmitter Operation

BSC transmission begins with the sending of an opening pad (PAD) and two sync (SYN) characters. These characters are programmable and stored in AR1(PAD) and AR2(SYN). The first SOH or STX initiates the block-check-character (BCC) accumulation. An initial SOH or STX is not included in the BCC accumulation. Should an underrun condition occur, the content of AR2 (normally SYN character) is transmitted until new characters become available. The message is terminated by the transmission of the BCC followed by a closing pad when an ETB, ITB, or ETX is fetched from the TxFIFO. The closing PAD is generated by the MPCC.

In transparent mode, the BCC accumulation is initiated by DLE-STX and is terminated by the sequences DLE-ETX, DLE-ETB, or DLE-ITB. See Table 5 for character sequence and inclusion in CRC accumulation. If an underrun occurs, DLE-SYN characters will be transmitted until new characters are available in the TxFIFO. ETB, ETX, ITB, or ENQ with a TLAST tag is treated as a control character and the MPCC automatically inserts a DLE immediately preceding these characters. DLE-ETB, DLE-ETX, DLE-ITB, or DLE-ENQ terminates a block of transparent text, and returns the data link to normal mode. BCC generation is not used for messages beginning with characters other than SOH, STX, DLE-SOH, or DLE-STX. On all message types, if the TSYN bit is set to 1 in the TCR, a SYN-SYN (DLE-SYN sequence on transparent messages) sequence is transmitted before the next character is fetched from the TxFIFO.

CHARACTER ORIENTED PROTOCOLS

The character oriented protocol (COP) option uses the format shown in Figure 9. It may be used for various character oriented protocols with 5-8 bit character sizes and optional parity checking. The input data is checked on a bit-by-bit basis for a pair of consecutive SYN characters to establish character synchronization. These SYN characters are discarded after detection. The PAD and SYN characters may be 5-8 bits long and are user programmable as stored in AR1 and AR2, respectively.

If parity checking is enabled the characters assembled after character sync are checked for parity errors. If STRSYN is set in the RCR, all SYN characters detected within the message will be discarded and will not be passed on to the RxFIFO. If STRSYN is reset, SYNs detected within the message will be treated as data.

DMA CONSIDERATIONS

When the R68561, in the word mode, is used with a DMAC, high throughput of bit-oriented protocols is achieved. However, problems can arise when trying to DMA byte-oriented data in the word mode.

BOP and BSC have well-defined message boundaries and the MPCC can detect the end of message, determine if there is an odd (single) byte at the end of a message, and so inform the host MPU by setting the Received Half Word (RHW) bit in the Frame Status byte.

In byte-oriented protocols (such as ASYNC and COP) there is no defined message length. In the word mode, received bytes are grouped in pairs. In the byte mode, each byte is available through the RxFIFO as it is received. Thus, the MPCC in the word mode has no way of knowing when an odd (single) byte has been received at an end of a transmission to be passed onto the host MPU. In the word mode received bytes are grouped in pairs. In the byte mode each byte is available through the FIFO as it is received.

For transmission of data by the MPCC in the word mode, the MPCC provides a Transmit Half Word (THW) bit in the Transmit Control Register. When set, this bit informs the MPCC that the last word in the TxFIFO (marked by setting the TLAST bit with $\overline{\text{DONE}}$) contains only the upper byte as valid data. However, the currently available DMACs have no method to inform the MPCC that the last word of the message contains a single byte and MPU intervention is necessary.

To handle byte-oriented protocols with DMAC, an R68561 in the byte mode or the R68560 (byte mode only) should be used.

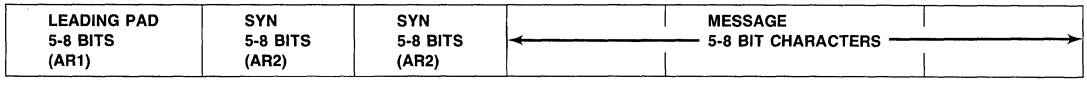
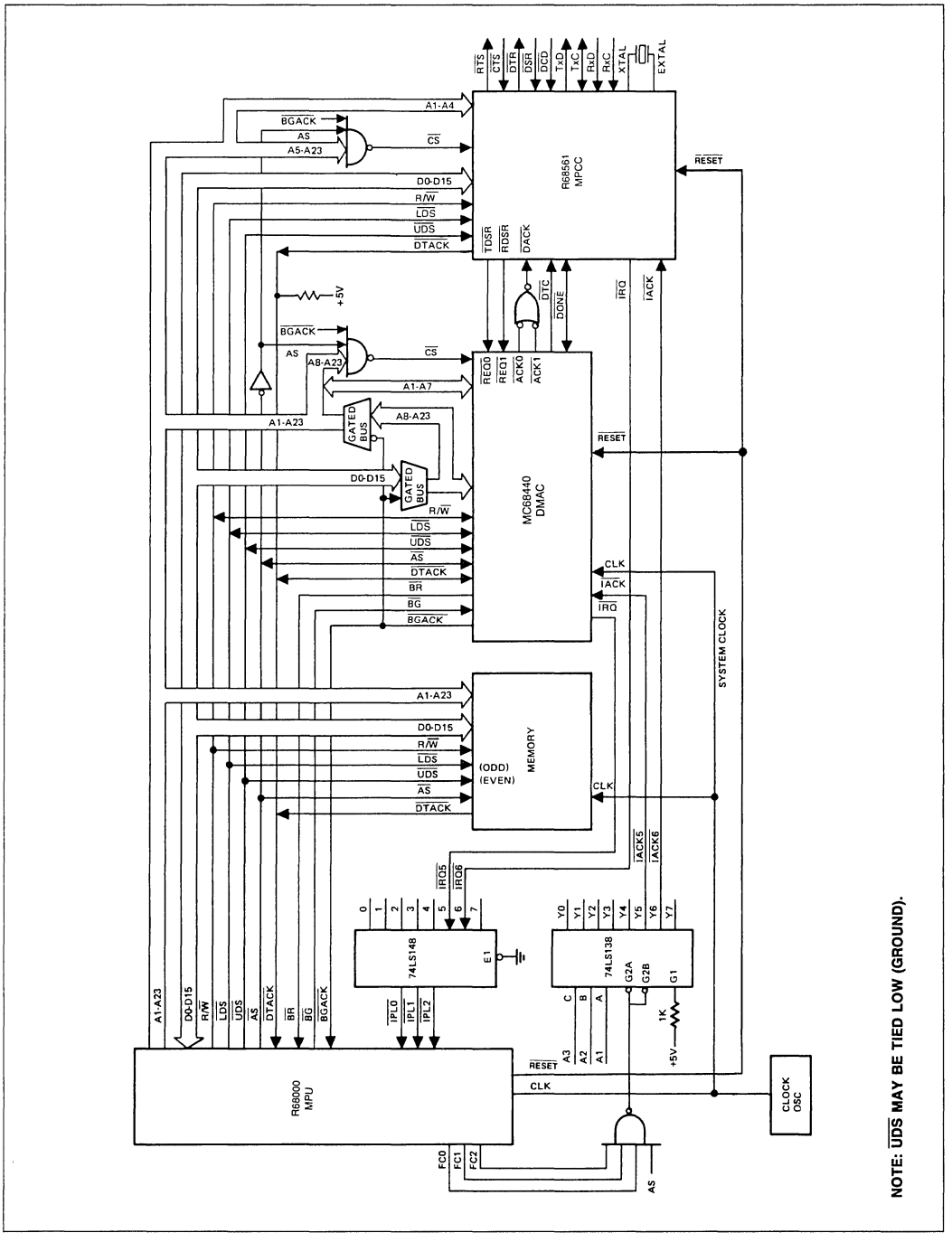


Figure 9. Character Oriented Protocol Format



NOTE: $\overline{UDS}$ MAY BE TIED LOW (GROUND).

Figure 10. Typical Interface to 68000-Based System

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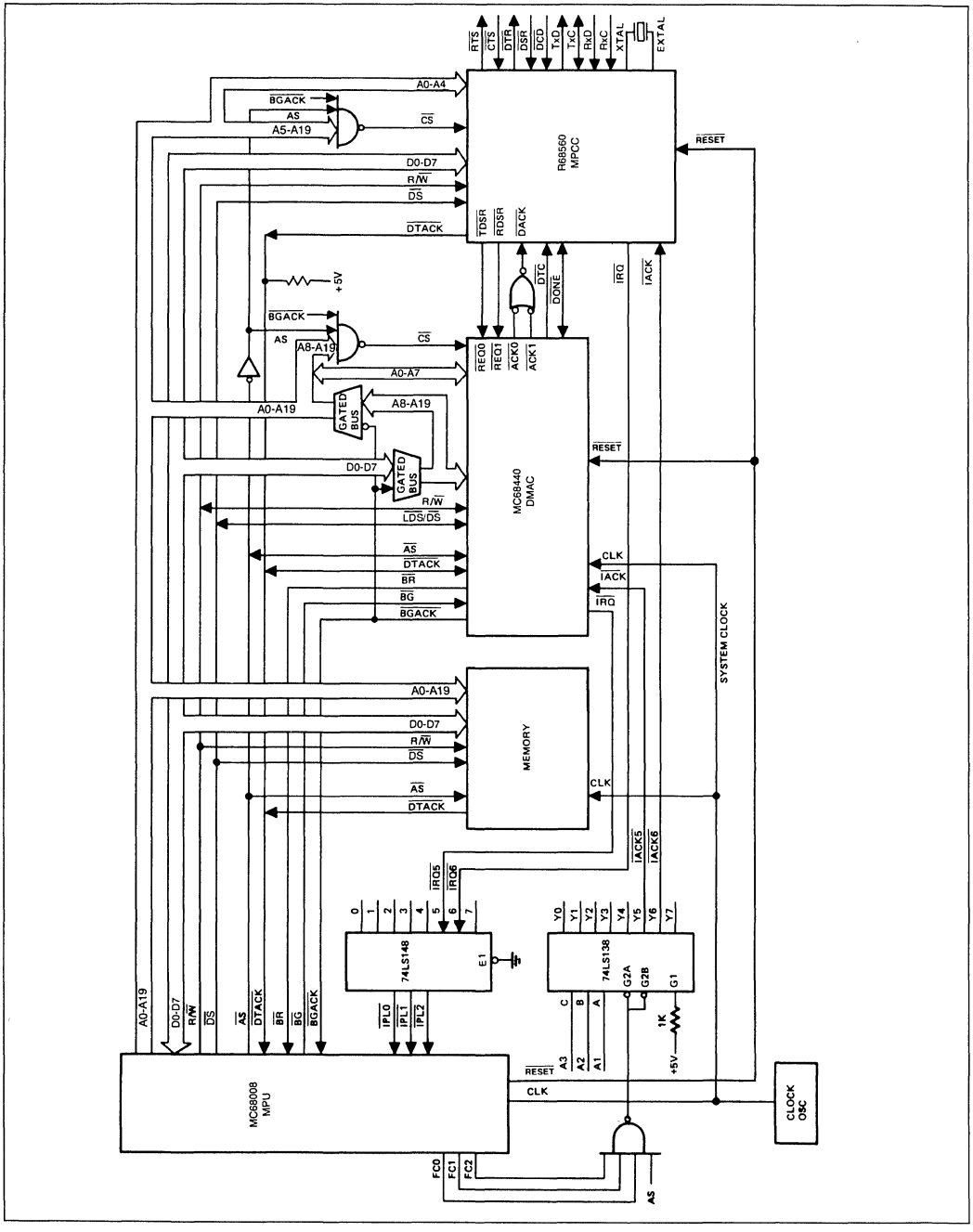
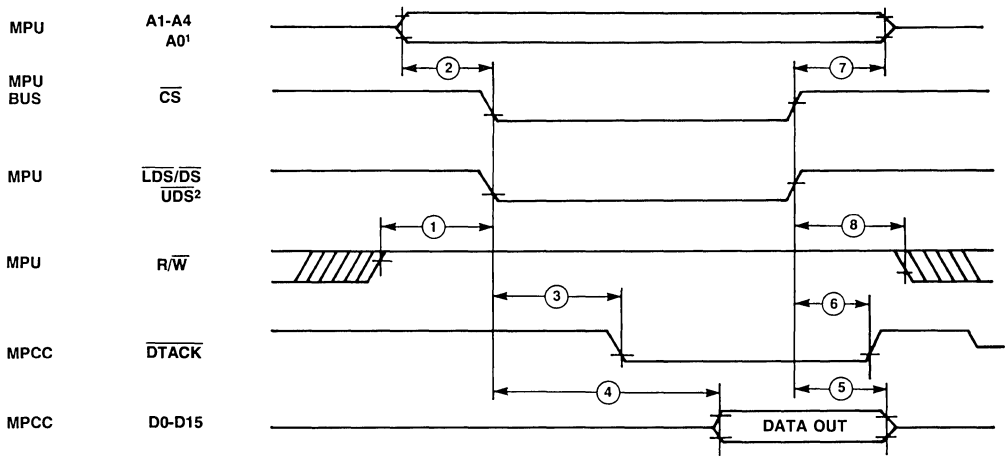
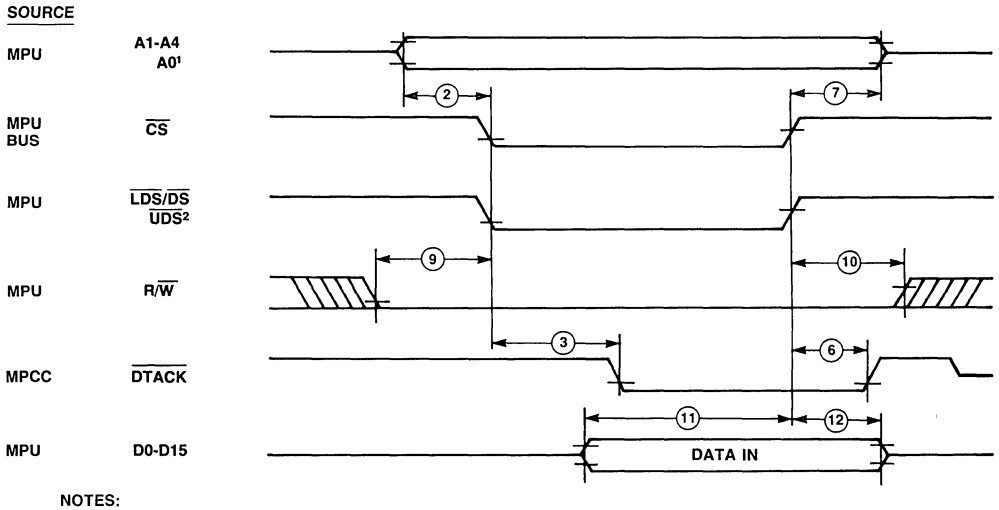


Figure 11. Typical Interface to 68008-Based System



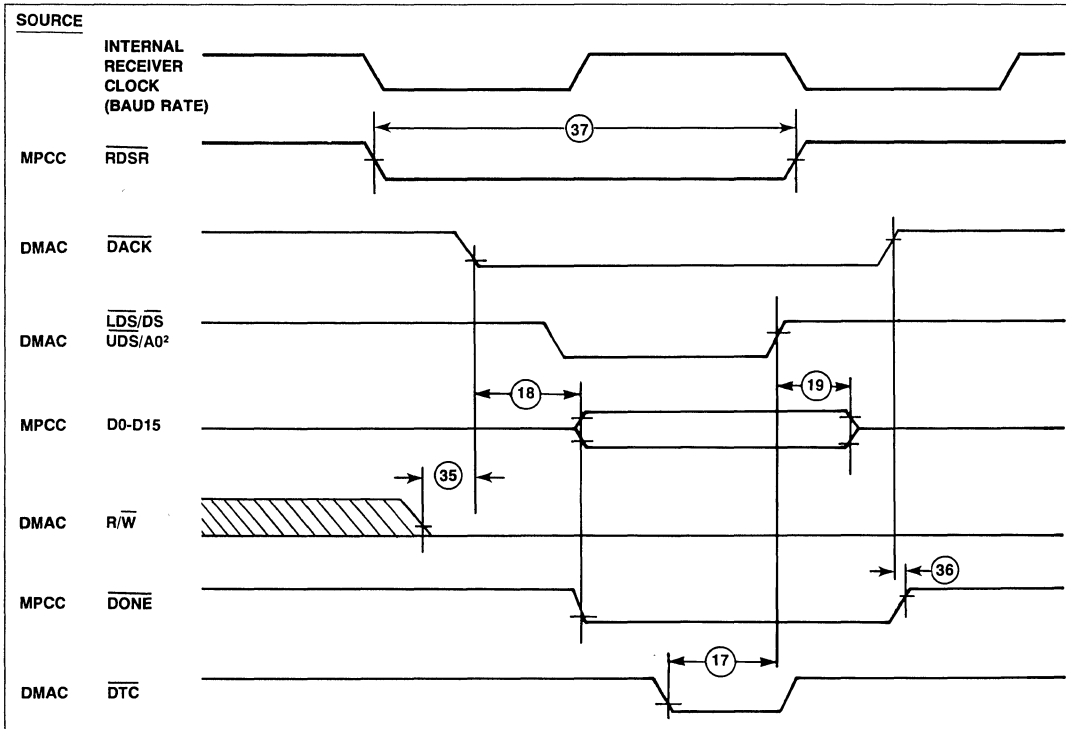
NOTES:
1. BYTE MODE WHEN CONNECTED TO A0 ON 68008 BUS.
2. WORD MODE WHEN CONNECTED TO UDS ON 68000 BUS.
3. TIMING MEASUREMENTS ARE REFERENCED TO AND FROM A LOW VOLTAGE OF 0.8 VOLTS AND A HIGH VOLTAGE OF 2.0 VOLTS, UNLESS OTHERWISE NOTED.
4. SEE ADDITIONAL NOTES ON PAGE 32.

Figure 12. MPCC Read Cycle Timing



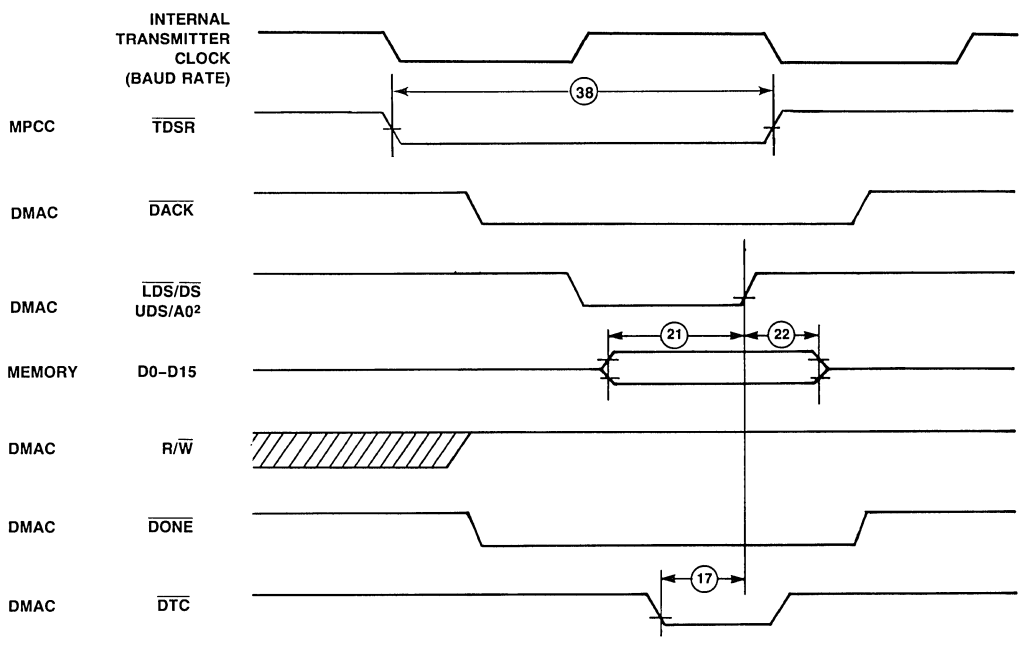
NOTES:
1. BYTE MODE WHEN CONNECTED TO A0 ON 68008 BUS.
2. WORD MODE WHEN CONNECTED TO UDS ON 68000 BUS.
3. TIMING MEASUREMENTS ARE REFERENCED TO AND FROM A LOW VOLTAGE OF 0.8 VOLTS AND A HIGH VOLTAGE OF 2.0 VOLTS, UNLESS OTHERWISE NOTED.
4. SEE ADDITIONAL NOTES ON PAGE 32.

Figure 13. MPCC Write Cycle Timing



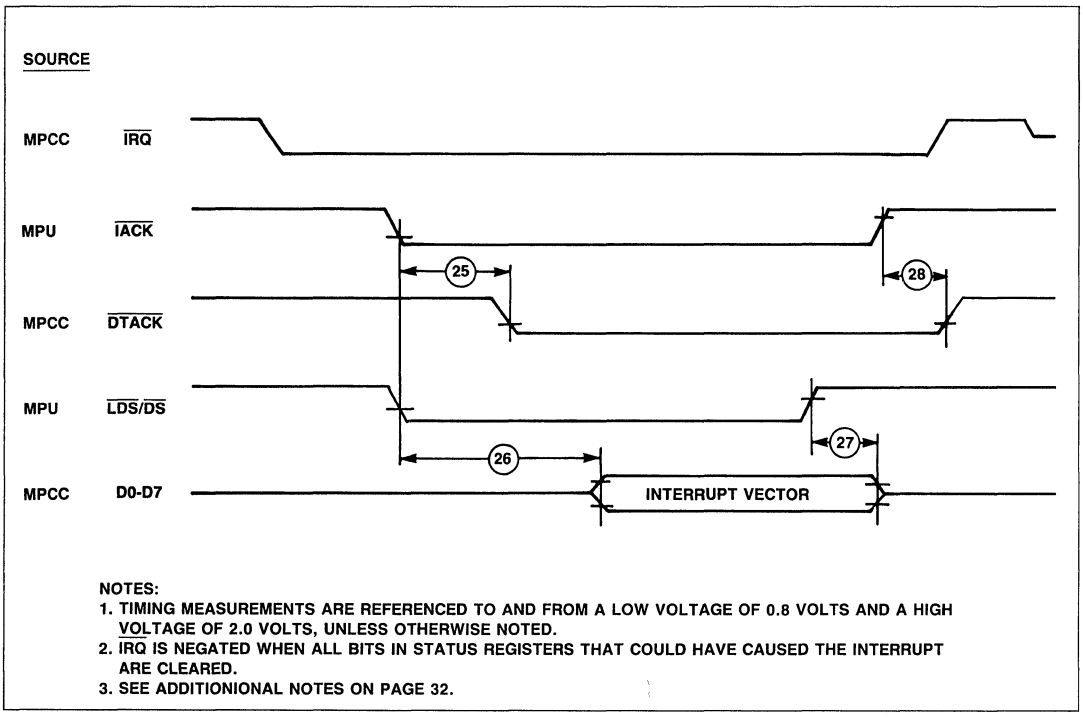
NOTES:
1. TIMING MEASUREMENTS ARE REFERENCED TO AND FROM A LOW VOLTAGE OF 0.8 VOLTS AND A HIGH VOLTAGE OF 2.0 VOLTS UNLESS OTHERWISE NOTED.
2. WORD MODE ONLY.
3. SEE ADDITIONAL NOTES ON PAGE 32.

Figure 14. MPCC to Memory DMA Transfer Cycle Timing (Receiver DMA Mode)



NOTES:
1. TIMING MEASUREMENTS ARE REFERENCED TO AND FROM A LOW VOLTAGE OF 0.8 VOLTS AND A HIGH VOLTAGE OF 2.0 VOLTS UNLESS OTHERWISE NOTED.
2. WORD MODE ONLY.
3. SEE ADDITIONAL NOTES ON PAGE 32.

Figure 15. Memory to MPCC DMA Transfer Cycle Timing (Transmitter DMA Mode)



NOTES:
1. TIMING MEASUREMENTS ARE REFERENCED TO AND FROM A LOW VOLTAGE OF 0.8 VOLTS AND A HIGH VOLTAGE OF 2.0 VOLTS, UNLESS OTHERWISE NOTED.
2. IRQ IS NEGATED WHEN ALL BITS IN STATUS REGISTERS THAT COULD HAVE CAUSED THE INTERRUPT ARE CLEARED.
3. SEE ADDITIONIONAL NOTES ON PAGE 32.

Figure 16. Interrupt Request Cycle Timing

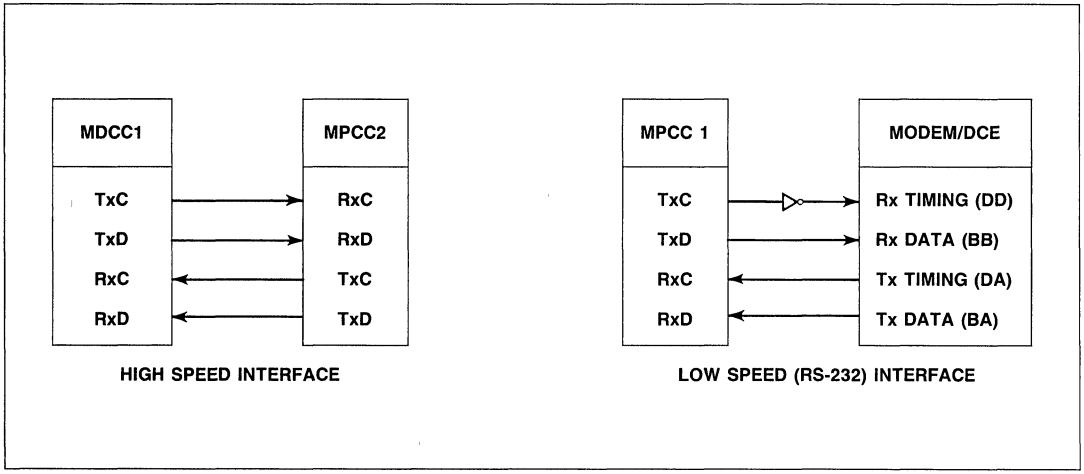


Figure 17. Serial Interface

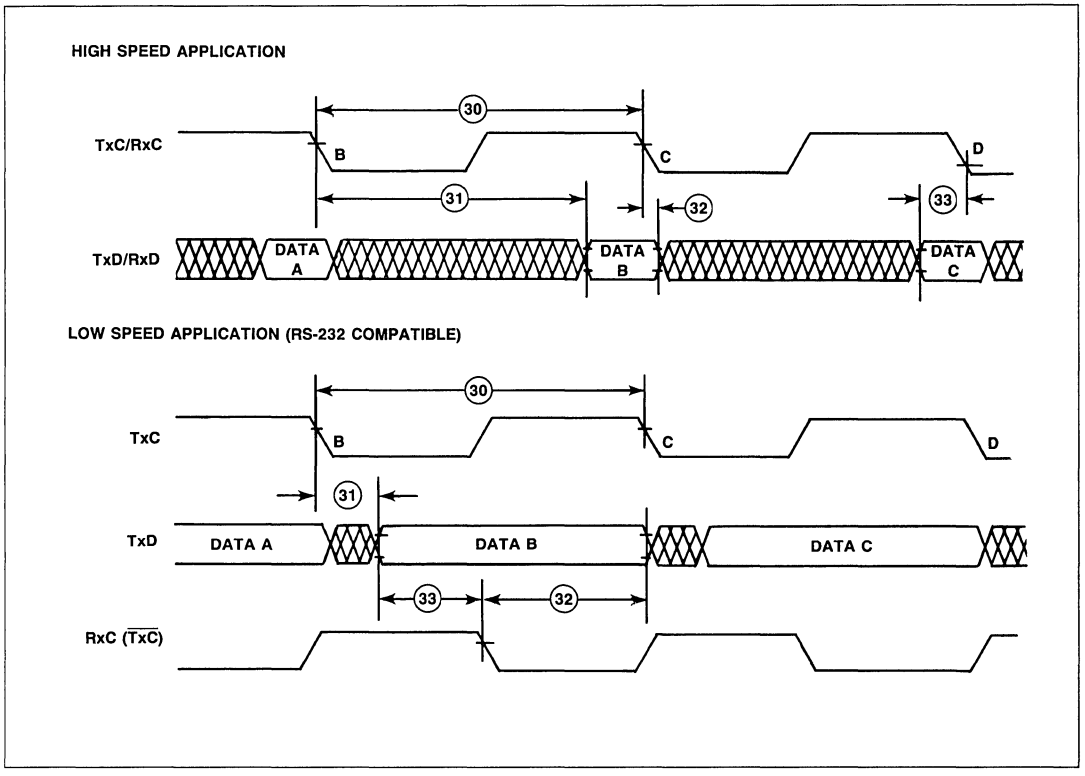


Figure 18. Serial Interface Timing

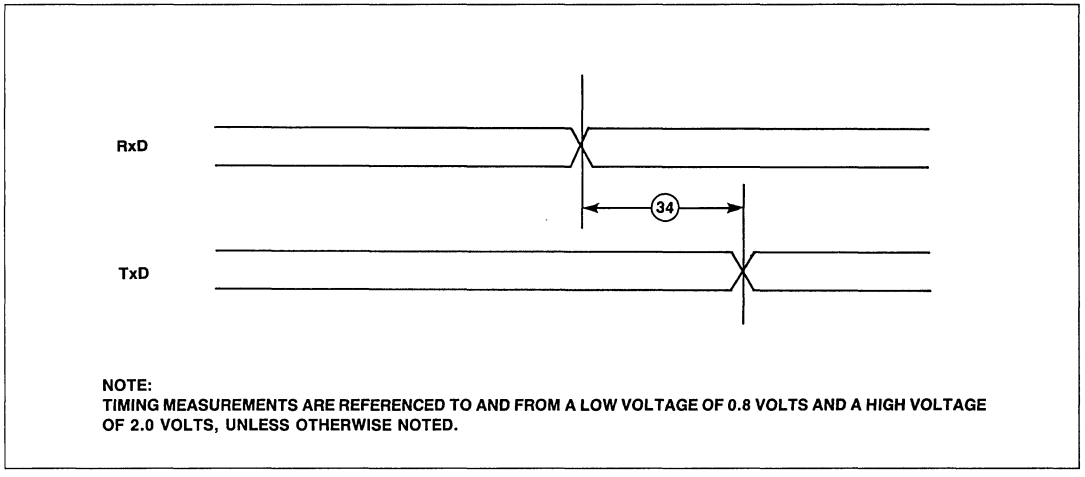


Figure 19. Serial Interface Echo Mode Timing

AC CHARACTERISTICS

(V_{CC} = 5.0 Vdc ±5%, V_{SS} = 0 Vdc, T_A = 0°C to 70°C)

Number	Parameter	Symbol	Min	Max	Unit
1	R/$\overline{W}$ High to $\overline{CS}$, $\overline{DS}$ Low	t_{RHSL}	0	—	ns
2	Address Valid to CS, $\overline{DS}$ Low	t_{AVSL}	30	—	ns
3[1]	$\overline{CS}$ Low to $\overline{DTACK}$ Low	t_{CLDAL}	0	60	ns
4[1]	$\overline{CS}$, $\overline{DS}$ Low to Data Valid	t_{SLDV}	0	140	ns
5	$\overline{DS}$ High to Data Invalid	t_{SHDXR}	10	150	ns
6	$\overline{DS}$ High to $\overline{DTACK}$ High	t_{SHDAT}	0	40	ns
7	$\overline{DS}$ High to Address Invalid	t_{SHAI}	20	—	ns
8	$\overline{CS}$, $\overline{DS}$ High to R/$\overline{W}$ Low	t_{SHRL}	20	—	ns
9	R/$\overline{W}$ Low to $\overline{CS}$, $\overline{DS}$ Low	t_{RLSL}	0	—	ns
10	$\overline{CS}$ High, $\overline{DS}$ High to R/$\overline{W}$ High	t_{SHRH}	20	—	ns
11	Data Valid to $\overline{CS}$, $\overline{DS}$ High	t_{DVSH}	60	—	ns
12	$\overline{CS}$, $\overline{DS}$ High to Data Invalid	t_{SHDXW}	0	—	ns
17	$\overline{DTC}$ Low to $\overline{DS}$ High	t_{CLSH}	60	—	ns
18	$\overline{DACK}$ Low to Data Valid, $\overline{DONE}$ Low	t_{ALDV}	0	140	ns
19	$\overline{DS}$ High to Data Invalid	t_{SHDXDR}	10	150	ns
21	Data Valid to $\overline{DS}$ High	t_{DVSH}	60	—	ns
22	$\overline{DS}$ High to Data Invalid	t_{SHDXDW}	0	—	ns
25	$\overline{IACK}$ Low to $\overline{DTACK}$ Low	t_{IALAL}	0	40	ns
26	$\overline{IACK}$, $\overline{DS}$ Low to Data Valid	t_{IALDV}	0	140	ns
27	$\overline{DS}$ High to Data Invalid	t_{ISHDI}	10	150	ns
28	$\overline{IACK}$ High to $\overline{DTACK}$ High	t_{IAHDAT}	0	40	ns
30	RxC and TxC Period	t_{CP}	248	—	ns
31	TxC Low to TxD Delay	t_{TCLTD}	0	200	ns
32	RxC Low to RxD Transition (Hold)	t_{RCLRD}	0	—	ns
33	RxD Transition to RxC Low (Setup)	t_{RDRCL}	30	—	ns
34	RxD to TxD Delay (Echo Mode)	t_{RDTD}	—	200	ns
35	R/$\overline{W}$ Low to $\overline{DACK}$ Low (Setup)	t_{RLAL}	0	—	ns
36	$\overline{DACK}$ High to $\overline{DONE}$ High	t_{AHDH}	0	—	ns
37[2, 3]	$\overline{RDSR}$ Pulse Width	t_{RPW}	1	—	clock period
38[2, 4]	$\overline{TDSR}$ Pulse Width	t_{TPW}	1	—	clock period

Notes:
1. For read cycle timing, the MPCC asserts $\overline{DTACK}$ within the MPU S4 clock low setup time requirement and establishes valid data (Data In) within the MPU S6 clock low setup time requirement.
2. For synchronous protocols, this is one full serial clock period of RxC for $\overline{RDSR}$ and TxC for $\overline{TDSR}$.
3. For asynchronous protocols, $\overline{RDSR}$ is asserted for two system clock periods for a prescale factor of 2 and for three system clock periods for a prescale factor of 3.
4. For asynchronous protocols, $\overline{TDSR}$ is asserted for a period of one-half the baud rate.

*NOTES TO FIGURES 12–16.

Address, $\overline{LDS}$, $\overline{UDS}$ and R/$\overline{W}$ are signals generated by the 68000 MPU and its bus timing prevails. $\overline{CS}$ is derived with external logic from the address bus and generally an Address Strobe ($\overline{AS}$) signal from the MPU. It will naturally be delayed somewhat from the $\overline{AS}$ signal. The active read or write cycle timing in the MPCC is during the summation of the active signal time, i.e., the last active signal starts the timing sequence. For an MPCC read cycle, for example, the data out parameter (t_{SLDV}, item 4) will be available 0 to 140 ns from the falling edge of $\overline{CS}$ or $\overline{LDS}$ whichever is active last. The data out parameter (t_{SHDXR}, item 5) will remain valid for 0–150 ns after the negation of $\overline{CS}$ or $\overline{LDS}$, whichever is negated first.

The minimum pulse widths for $\overline{CS}$, $\overline{LDS}$, $\overline{UDS}$, $\overline{DACK}$, $\overline{IACK}$ and $\overline{DTC}$ are not specified since they are system dependent and relate to system clock timing. For example, it is apparent that the minimum active time for "AND" condition of $\overline{CS}$ and $\overline{LDS}$ is 140 ns (t_{SLDV}, item 4) plus the setup time of the Data In to the receiving device if $\overline{LDS}$ high is used to strobe the data in. These same factors hold true for $\overline{UDS}$, $\overline{DACK}$ and $\overline{IACK}$. If $\overline{DTC}$ is used it must be true a minimum of 60 ns before the rising edge of $\overline{LDS}$ and thus this is the minimum pulse width. It may be connected to ground.

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to +7.0	V
Input Voltage	V_{IN}	−0.3 to +7.0	V
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature	T_{STG}	−55 to +150	°C

***NOTE:** Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in other sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL CHARACTERISTICS

Parameter	Symbol	Value	Rating
Thermal Resistance	θ_{JA}		°C/W
Ceramic		50	
Plastic		68	

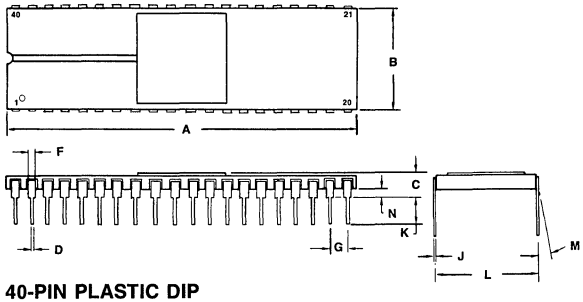
DC CHARACTERISTICS

(V_{CC} = 5.0 Vdc ±5%, V_{SS} = 0 Vdc, T_A = 0°C to 70°C unless otherwise noted)

Parameter	Symbol	Min	Max	Unit	Test Conditions
Input High Voltage All Inputs	V_{IH}	2.0	V_{CC}	V	
Input Low Voltage All Inputs	V_{IL}	−0.3	+0.8	V	
Input Leakage Current R/$\overline{W}$, $\overline{RESET}$, $\overline{CS}$, A1-A4	I_{IN}	—	10.0	μA	V_{IN} = 0 to 5.25V V_{CC} = 5.25V
Three-State (Off State) Input Current $\overline{IRQ}$, $\overline{DTACK}$, D0-D15	T_{TSI}	—	10.0	μA	V_{IN} = 0.4 to 2.4V V_{CC} = 5.25V
Output High Voltage $\overline{RDSR}$, $\overline{TDSR}$, $\overline{IRQ}$, $\overline{DTACK}$, D0-D15, $\overline{DSR}$, $\overline{DTR}$, $\overline{RTS}$, TxD, TxC	V_{OH}	V_{SS} + 2.4	—	V	V_{CC} = 4.75V I_{LOAD} = −400 μA C_{LOAD} = 130 pF
BCLK	V_{OH}	V_{SS} + 2.4	—	V	V_{CC} = 4.75V I_{LOAD} = 0 C_{LOAD} = 30 pF
Output Low Voltage $\overline{RDSR}$, $\overline{TDSR}$, $\overline{IRQ}$, $\overline{DTACK}$ D0-D15, $\overline{DSR}$, $\overline{DTR}$, $\overline{RTS}$, TxD, TxC, BCLK,	V_{OL}	—	0.5	V	V_{CC} = 4.75V I_{LOAD} = 3.2 mA
$\overline{DONE}$	V_{OL}	—	0.5	V	V_{CC} = 4.75V I_{LOAD} = 8.8 mA
Internal Power Dissipation	P_{INT}	—	1	W	T_A = 25°C
Input Capacitance	C_{IN}	—	13	pF	V_{IN} = 0V T_A = 25°C f = 1 MHz

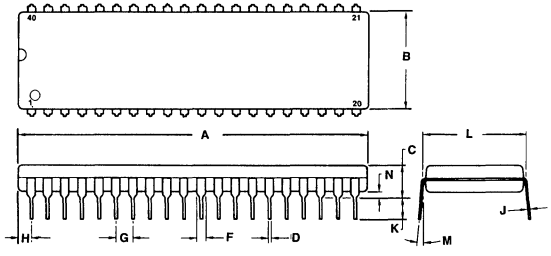
PACKAGE DIMENSIONS — 40-PIN DIP

40-PIN CERAMIC DIP



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	50.29	51.31	1.980	2.020
B	14.73	15.24	0.580	0.600
C	3.30	4.32	0.130	0.170
D	0.38	0.53	0.015	0.021
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
J	0.20	0.30	0.008	0.012
K	2.54	4.06	0.100	0.160
L	14.99	15.49	0.590	0.610
M	0°	10°	0°	10°
N	1.02	1.52	0.040	0.060

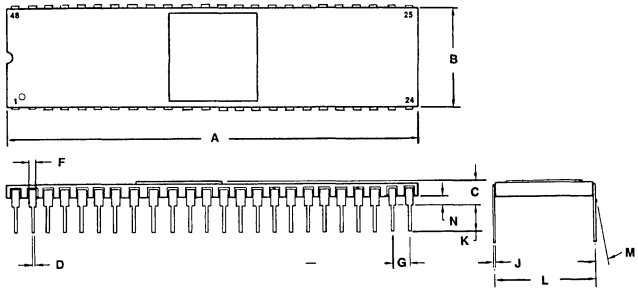
40-PIN PLASTIC DIP



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	51.82	52.32	2.040	2.060
B	13.72	14.22	0.540	0.560
C	4.06	5.08	0.160	0.200
D	0.38	0.53	0.015	0.021
F	1.14	1.40	0.045	0.055
G	2.54 BSC		0.100 BSC	
H	1.40	1.91	0.055	0.075
J	0.20	0.30	0.008	0.012
K	3.30	4.32	0.130	0.170
L	14.48	16.00	0.570	0.630
M	0°	10°	0°	10°
N	0.51	1.02	0.020	0.040

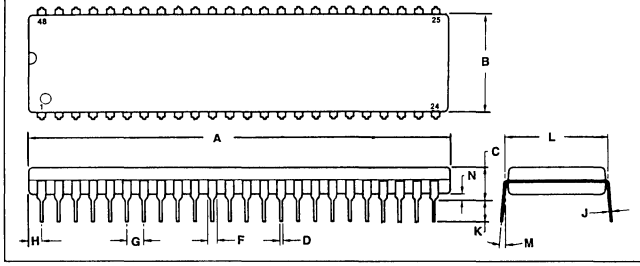
PACKAGE DIMENSIONS — 48-PIN DIP

48-PIN CERAMIC DIP



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	60.35	61.57	2.376	2.424
B	14.73	15.24	0.580	0.600
C	3.30	4.32	0.130	0.170
D	0.38	0.53	0.015	0.021
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
J	0.20	0.30	0.008	0.012
K	2.54	4.06	0.100	0.160
L	14.99	15.49	0.590	0.610
M	0°	10°	0°	10°
N	1.02	1.52	0.040	0.060

48-PIN PLASTIC DIP



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	60.83	61.85	2.395	2.435
B	13.72	14.22	0.540	0.560
C	4.06	5.08	0.160	0.200
D	0.38	0.53	0.015	0.021
F	1.14	1.40	0.045	0.055
G	2.54 BSC		0.100 BSC	
H	1.40	1.91	0.055	0.075
J	0.20	0.30	0.008	0.012
K	3.30	4.32	0.130	0.170
L	14.48	16.00	0.570	0.630
M	0°	10°	0°	10°
N	0.51	1.02	0.020	0.040

4

Section 5
Intelligent Display Controllers

Rockwell

10937 and 10957
Alphanumeric Display Controller

DESCRIPTION

The 10937 and 10957 Alphanumeric Display Controllers, two of the Rockwell Intelligent Display Controller products, are MOS/LSI general purpose display controllers designed to interface to segmented displays (vacuum fluorescent, or LED).

The 10937 or 10957 will drive displays with up to 16 characters with 14 or 16 segments plus a decimal point and comma tail. Segment decoding within each device provides for the ASCII character set (upper case only). No external drive circuitry is required for displays that operate on 20 ma of drive current up to 50 volts. A 16 x 64-bit segment decoder provides internal ASCII character set decoding for the display.

The 10937 and 10957 are identical with the exception that the 10957 has two additional decodings for the decimal point and comma tail.

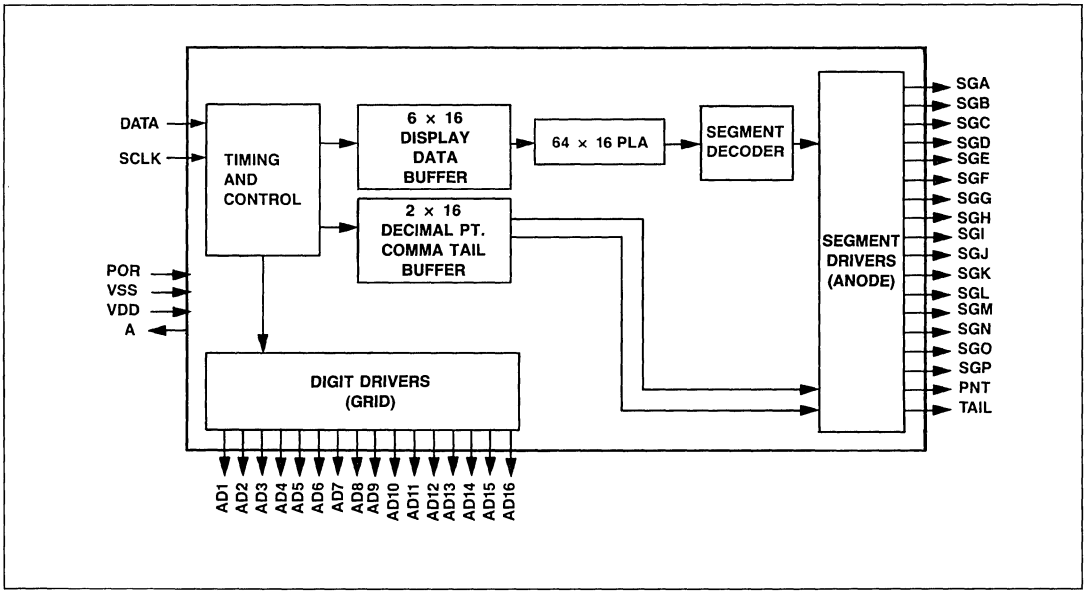
FEATURES

- 16 character display driver with decimal point and comma tail
- 14 or 16 segment drivers
- Up to 66 kHz data rate
- Direct digit drive of 20 ma at 50 volts
- Supports vacuum fluorescent, or LED displays
- 64 x 16-bit PLA provides segment decoding for ASCII character set (all caps only)
- Serial data input for 8-bit display and control data words.
- 40-Pin DIP

ORDERING INFORMATION

Part Number	Package Type	Drive Voltage	Temperature Range (°C)
109X7P-40	Plastic	40V	0 to +70
109X7P-50	Plastic	50V	0 to +70
109X7PE-40	Plastic	40V	−40 to +85
109X7PE-50	Plastic	50V	−40 to +85

Note: X = 3 or 5



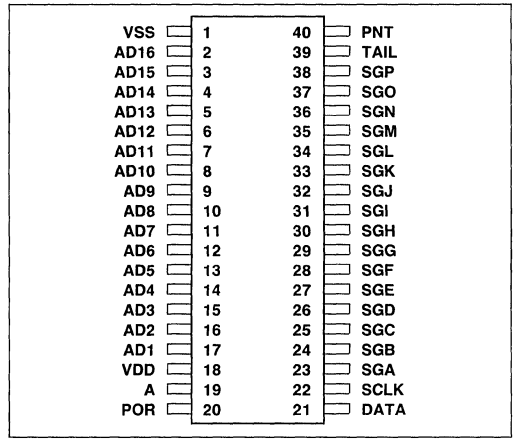
10937 and 10957 Block Diagram

5

INTERFACE DESCRIPTION

Pin Functions

Signal Name	Pin No.	Function
VSS	1	Power and signal reference
AD16–AD1	2–17	Digits 16 through 1 driver outputs
VDD	18	DC power connection
A	19	A clock output used for testing
POR	20	Power-on reset input
DATA	21	Serial data input
SCLK	22	Serial data clock input
SGA–SGP	23–38	Segments A through P driver outputs
TAIL	39	Comma tail driver output
PNT	40	Decimal point driver output



Pin Configuration

SPECIFICATIONS

MAXIMUM RATINGS*

All voltages are specified relative to V_{SS}.

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{DD}	+0.3	−20	V
Input Voltage	V_{IN}	+0.3	−20	V
Output Voltage	V_{OUT}	+0.3	−50	V
Operating Current	I_{DD}		7	mA
Output Current Digits	I_{SD}		20	mA
Output Current Segments	I_{SS}		10	mA
Operating Temperature				
Commercial	T_C	0	+70	°C
Industrial	T_I	−40	+85	°C
Storage Temperature	T_{STG}	−55	+125	°C
Input Capacitance	C_{IN}		5	pF
Output Capacitance	C_{OUT}		10	pF

***NOTE:** Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

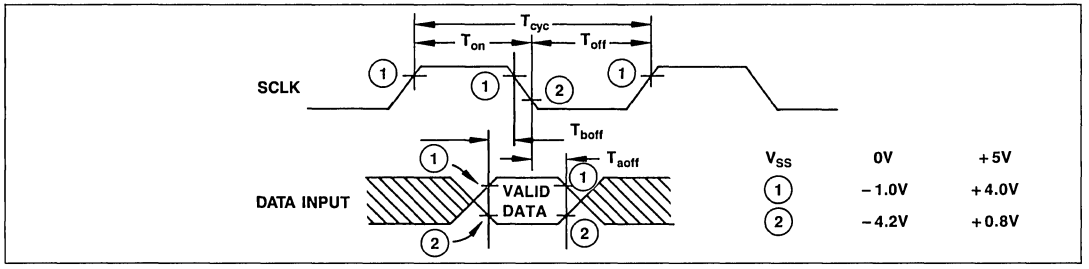
DC CHARACTERISTICS

Parameter	Limits (V_{SS} = 0) Min.	Typ.	Max.	Limits (V_{SS} = +5V) Min.	Typ.	Max.	Conditions	Unit
Supply Voltage (V_{DD})	−16.5	−15.0	−13.5	−11.5	−10.0	−8.5		V
Power dissipation		40	100		40	100		mW
Input DATA, SCLK,								V
Logic "1"	−1.0		+0.3	+4.0		+5.3		V
Logic "0"	V_{DD}		−4.2	V_{DD}		+0.8		
Input POR								
Logic "1"	−3.0		+0.3	+2.0		+5.3		
Logic "0"	V_{DD}		−10.0	V_{DD}		−5.0		
Output Digit and Segment Strobes								
Driver On								
Commercial			−1.5			+3.5	At 10 mA	V
Industrial			−1.7			+3.3		V
Driver Off 109X7-40			−40			−35	Actual value determined by external circuit	V
Driver Off 109X7-50			−50			−45		V
Output Leakage			10			10	Per driver when driver is off	μA
Input Leakage			10			10		μA

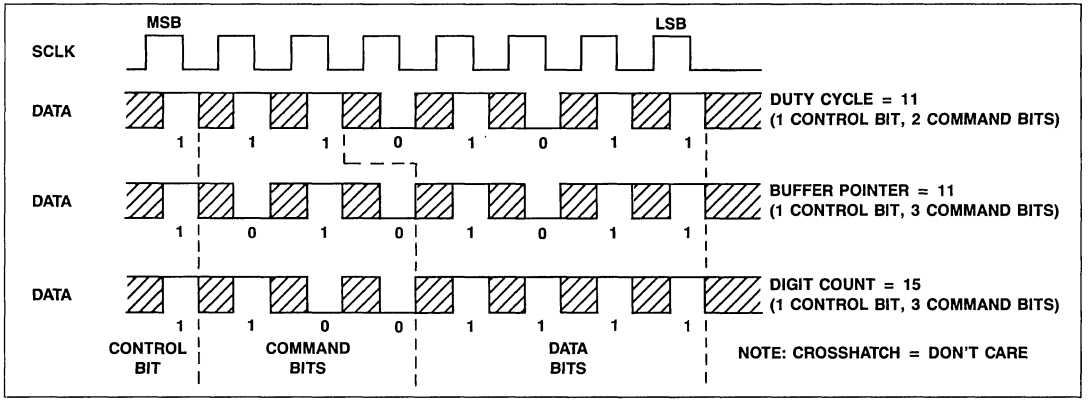
Notes: All outputs require pulldown resistors. X = 3 or 5 depending on device.

AC CHARACTERISTICS

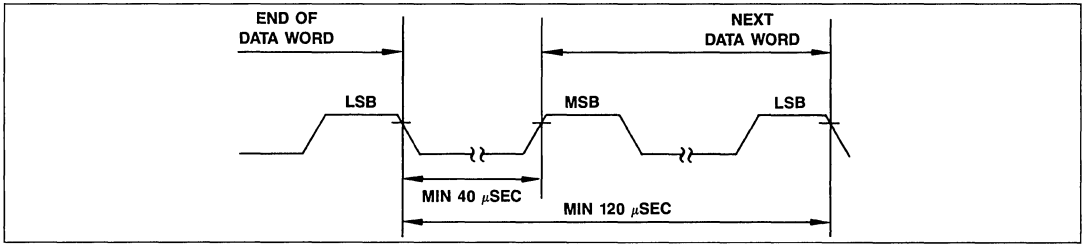
Parameter	Symbol	Min	Typ	Max	Unit
SCLK Clock					
On Time	T_{on}	1.0		20.0	μs
Off Time	T_{off}	1.0			μs
Data Input Sample Time					
Before SCLK Clock Off	T_{boff}	200			ns
After SCLK Clock Off	T_{aoff}	100			ns



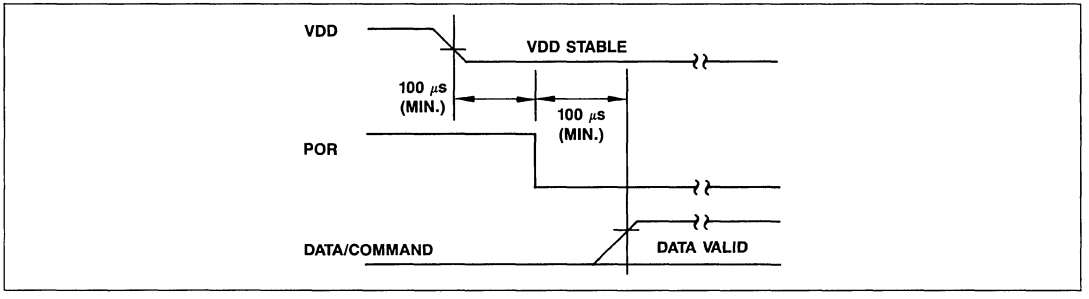
SCLK and Serial Data Timing



SCLK and Serial Data (Control Word) Examples



Data Word LSB/MSB Timing



Power-On Reset Timing

FUNCTIONAL DESCRIPTION

The 10937 or 10957 is a general purpose display controller for multiplexed, segmented displays with up to 16 character positions and 14 or 16 segments, plus decimal point and comma tail. No external drive circuitry is needed for displays requiring up to 20 ma of drive current up to 50 volts. All timing signals required to control the display are generated in the 10937 or 10957 device without any refresh input from the host processor.

Input data is loaded into the Display Data Buffer via the Serial Data Input (Data) channel. Internal timing and control blocks synchronize the segment and digit output signals to provide the proper timing for the multiplexing operation. A 16 x 64-bit PLA is provided for segment decoding for the full ASCII character set (upper case only).

Input data is loaded into the 10937 or 10957 ADC as a series of 8-bit words with the most significant bit (MSB), bit 7, first. If bit 7 of any word loaded is a logic 1 (this bit is referred to as the control bit C), the loaded word is a control data word. If the C bit of any word is a logic 0, the loaded word is a display data word. The following paragraphs describe the format and functions of these control and display data words.

INPUT CONTROL DATA WORDS

When the C-Bit (bit 7) of the 8-bit input word is a logic 1, bits 5 and 6 are decoded into one of four control commands while data associated with the command are extracted from bits 0 – 4 (see Table 1). The four control codes perform the following display functions:

- Load the Display Data Buffer pointer,
- Load the Digit Counter,
- Load the Duty Cycle register,
- Enable the Test Mode.

Table 1 lists the control codes and their functions.

Buffer Pointer Control

The Buffer Pointer Control code allows the Display Data Buffer pointer to be set to any digit position so that individual characters may be modified. The Buffer Pointer is loaded with a decimal equivalent value 2 less than the desired value (i.e., to point to the digit controlled by AD6 of the display, a value of 4 is entered). See Table 2 for a complete list of the Buffer Pointer values.

Table 2. Buffer Pointer Control Codes

Hex Code	Pointer Value	Character Controlled By
A0	0	AD2
A1	1	AD3
A2	2	AD4
A3	3	AD5
A4	4	AD6
A5	5	AD7
A6	6	AD8
A7	7	AD9
A8	8	AD10
A9	9	AD11
AA	10	AD12
AB	11	AD13
AC	12	AD14
AD	13	AD15
AE	14	AD16
AF	15	AD1

Digit Counter Control

The Digit Counter Control code is normally used only during initialization routines to define the number of character positions to be controlled. This code maximizes the duty cycle for any display. If 16 characters are to be controlled, enter a value of 0 (zero). Otherwise, enter the value desired.

Duty Cycle Control

The Duty Cycle Control code is used to turn the display on and off, and to adjust display brightness. As shown in the block diagram, the time slot for each character is 32 clock cycles. The segment and digit drivers for each character are on for a maximum of 31 cycles with a 1 cycle inter-digit off-time. The Duty Cycle Control code contains a 5-bit numeric field which modifies the on-time for the driver outputs from 0 to 31 cycles. A duty cycle of 0 puts both the segment and digit drivers into the off state.

Test Mode Enable

The Test Mode Enable code is a device test function only. If executed, it will lock the device in the Test Mode. Once locked in, the device can only be removed from Test Mode by performing a power-on reset.

If this mode is activated, the digit time is reduced from 32 to 4 clock cycles to speed up the output driver sequencing time for ease in testing.

INPUT DISPLAY DATA WORDS

Display data words are loaded as 8-bit ASCII format codes. The 64 codes available (with the C-bit set to 0 to indicate a display data word) are shown in Table 3 with their corresponding ASCII characters.

Table 1. Control Data Words

8-Bit Control Word		Function
C-Bit (Bit 7)	7-Bit Code (Bits 6 – 0)	
1	010NNNN(1)	BUFFER POINTER CONTROL (Position of character to be changed)
1	100NNNN(1)	DIGIT COUNTER CONTROL (Number of characters to be output)
1	11NNNNN(2)	DUTY CYCLE CONTROL (On/off and brightness control)
1	00NNNNN(3)	TEST MODE ENABLE (Not a user function)

Notes: 1. NNNN is a 4-bit binary value representing the digit number to be loaded.
2. NNNNN is a 5-bit binary value representing the number of clock cycles each digit is on.
3. This code is a device test function only. If executed it will lock the device in the test mode. Once locked in, the device can only be removed from Test Mode by performing a power-on reset.

Sixteen display data words must be entered to completely load the Display Data Buffer. The Buffer Pointer is automatically incremented before each data word is stored in the Display Buffer except for decimal point and comma words. These do not cause the Buffer Pointer to increment and thus are always associated with the previous character entered. To select the next character position to be loaded out of the normal sequence, use the Buffer Pointer Control command before entering the display data word. It is not necessary to use the Buffer Pointer Control command to cycle back to position 1 when less than 16 character positions are being used.

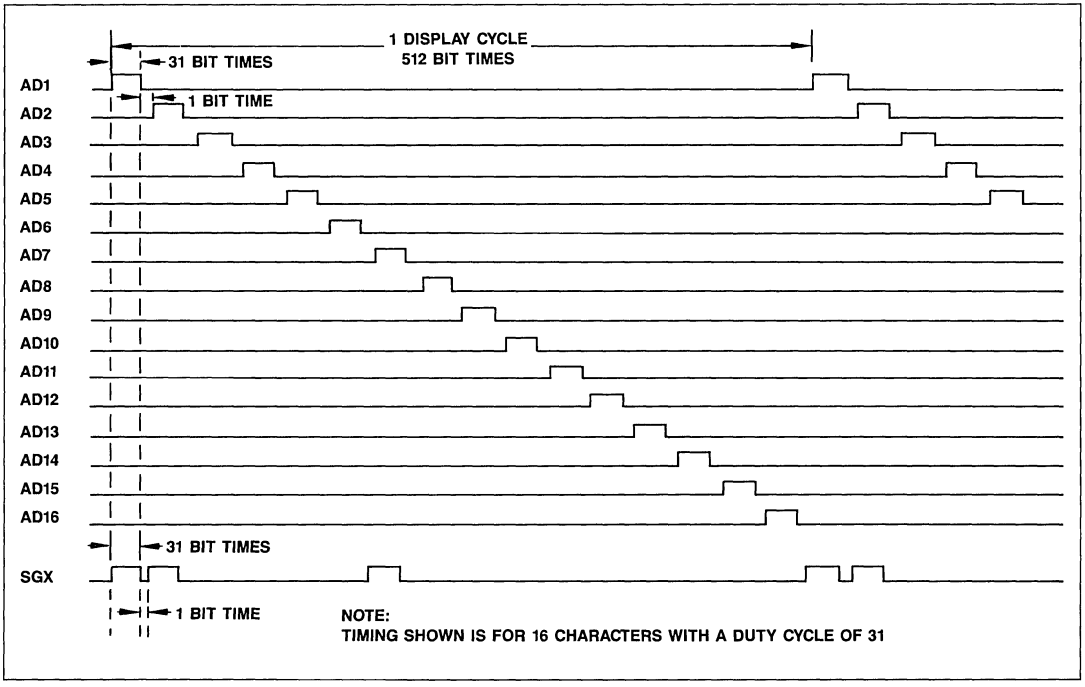


Figure 1. Display Scan Timing Diagram (Duty Cycle)

Table 3. Character Assignments for Display Data Words

DATA WORD		CHARACTER	DATA WORD		CHARACTER	DATA WORD		CHARACTER	DATA WORD		CHARACTER
BINARY	HEX		BINARY	HEX		BINARY	HEX		BINARY	HEX	
0X000000	00	@	0X010000	10	P	0X100000	20		0X110000	30	0
0X000001	01	A	0X010001	11	Q	0X100001	21	!	0X110001	31	1
0X000010	02	B	0X010010	12	R	0X100010	22	"	0X110010	32	2
0X000011	03	C	0X010011	13	S	0X100011	23	#	0X110011	33	3
0X000100	04	D	0X010100	14	T	0X100100	24	$	0X110100	34	4
0X000101	05	E	0X010101	15	U	0X100101	25	%	0X110101	35	5
0X000110	06	F	0X010110	16	V	0X100110	26	&	0X110110	36	6
0X000111	07	G	0X010111	17	W	0X100111	27	'	0X110111	37	7
0X001000	08	H	0X011000	18	X	0X101000	28	(	0X111000	38	8
0X001001	09	I	0X011001	19	Y	0X101001	29	)	0X111001	39	9
0X001010	0A	J	0X011010	1A	Z	0X101010	2A	*	0X111010	3A	:
0X001011	0B	K	0X011011	1B	[	0X101011	2B	+	0X111011	3B	;
0X001100	0C	L	0X011100	1C	/	0X101100	2C	'	0X111100	3C	<
0X001101	0D	M	0X011101	1D	]	0X101101	2D	—	0X111101	3D	=
0X001110	0E	N	0X011110	1E	∧	0X101110	2E	•	0X111110	3E	>
0X001111	0F	O	0X011111	1F	-	0X101111	2F	\	0X111111	3F	?

Note: X means this bit (bit 7) is a "don't care" bit except for PNT and TAIL on 10957 only. The hex codes shown assume bit 7 is a zero.

POWER-ON RESET (POR)

The Power-On Reset (POR) initializes the internal circuits of the 10937 or 10957 ADC when power (V_{DD}) is applied. The following conditions are established after a Power-On Reset:

a. The Digit Drivers (AD1 – AD16) are in the off state (floating).
b. The Segment Drivers (SGA – SGP) are in the off state (floating). This includes PNT and Tail.
c. The Duty Cycle is set to 0.
d. The Digit Counter is set to 16 (a bit code value of 0).
e. The Buffer Pointer points to the character controlled by AD1.

DIGIT DRIVERS (AD1–AD16)

The sixteen Digit Drivers (AD1 – AD16) are used to select each of the display digits sequentially during a refresh scan. Display segments will be illuminated when both the Digit Drivers and Segment Drivers for a particular character are energized simultaneously. The timing characteristics of both the digits and segments are shown in Figure 1. See POR for the Power-On Reset state of these drivers.

Table 4. Comparison of 10957 with 10937

Input Data	10937 Character	10957 Character
2C	;	;
2E	.	.
6C	;	.
6E	.	

SEGMENT DRIVERS (SGA–SGP)

Sixteen (16) Segment Drivers are provided (SGA – SGP), plus the decimal point (PNT) and comma tail (TAIL). The segment outputs are internally decoded from the 8-bit characters in the Display Data Buffer by means of a 64 x 16-bit PLA. The Segment Driver Allocations are shown in Figure 2. Data codes and their corresponding segment patterns are shown in Figure 3. Timing characteristics for the segment outputs are shown in Figure 1. See POR for the Power-On Reset state of these drivers.

NOTE

For 14-segment displays, SGA is used for the top segment and SGF is used for the bottom segment. SGB and SGE can be floated.

TYPICAL SYSTEM HOOK-UP

Figure 4 shows the 10937 or 10957 as it would be connected to a V-F display when driven by a host system. E_K is determined by the V-F display specifications and R_C is selected to provide proper biasing current for zeners. Pull down resistors R_A and R_G are determined by the interconnection capacitance between the device and the display.

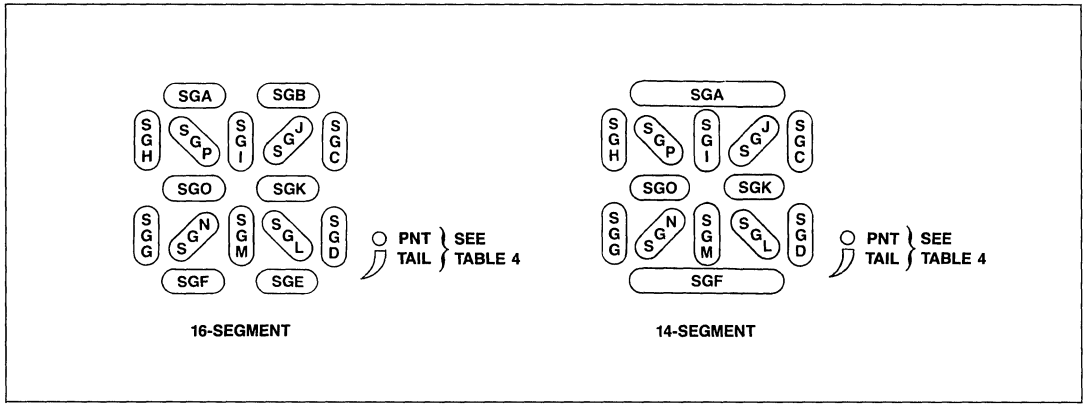
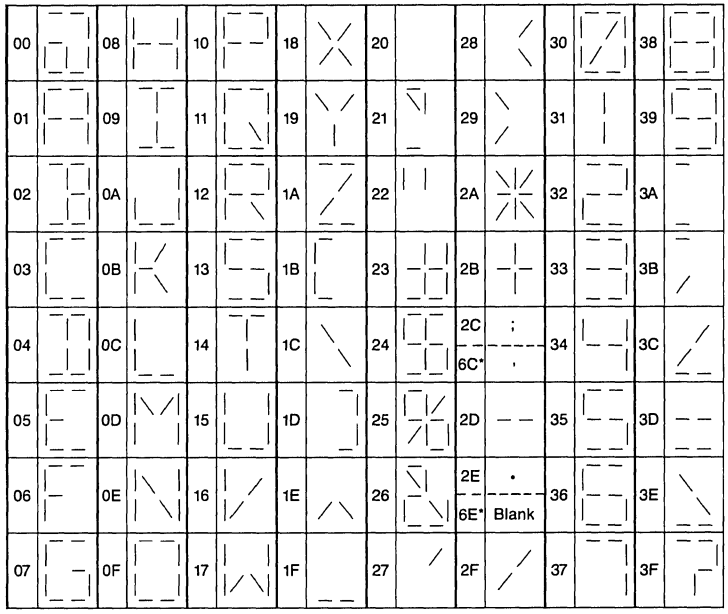
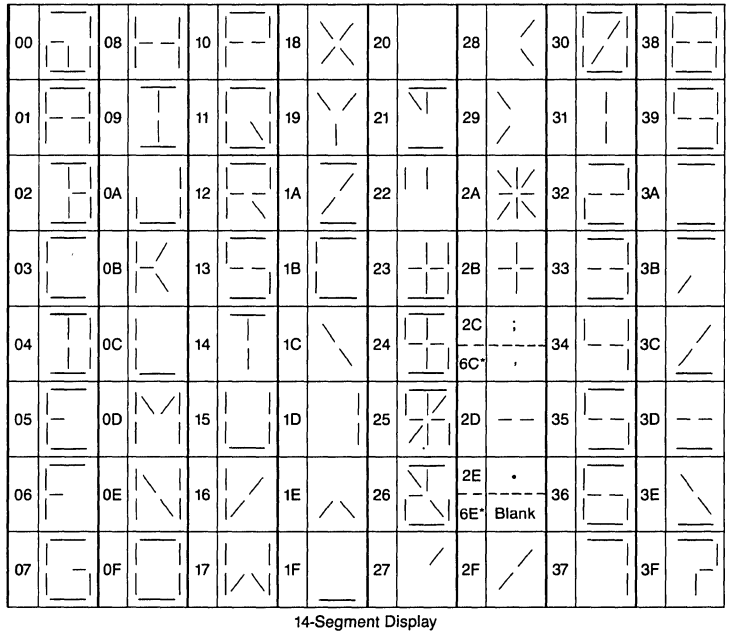


Figure 2. Segment Driver Allocations



16-Segment Display



14-Segment Display

Notes: Bit 7 of the data byte is a "don't care" bit except for PNT and TAIL on 10957. Data byte hex codes shown assume bit 7 is a zero.
* = 10957 only.

Figure 3. Display Segment Driver Character Patterns

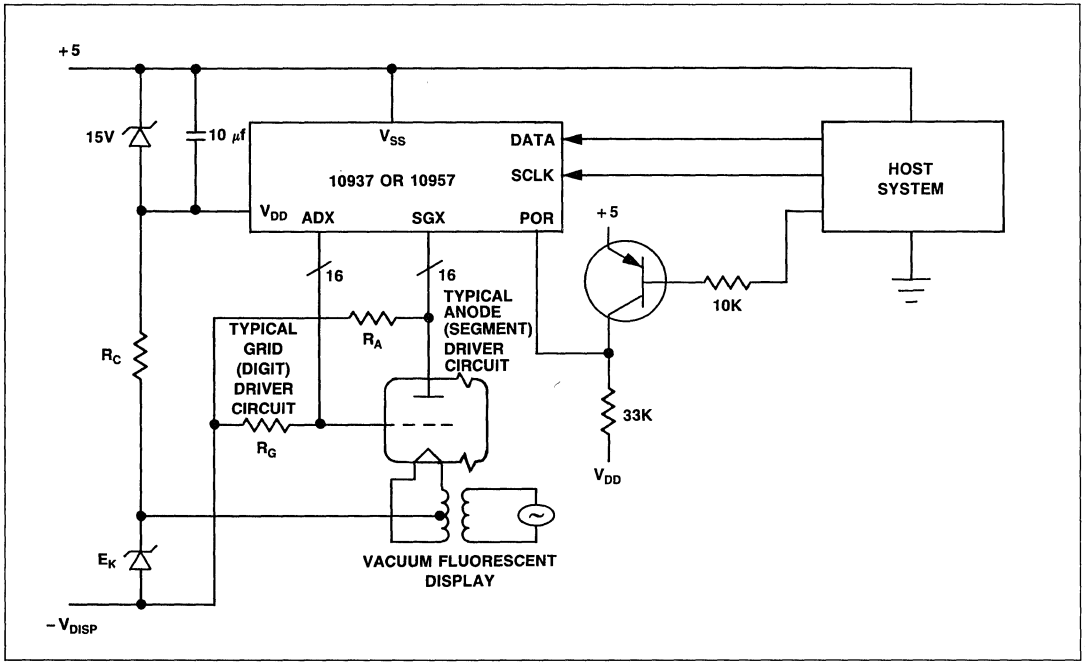


Figure 4. Partial System Schematic

Rockwell

10938 and 10939
Dot Matrix Display Controller

DESCRIPTION

The Rockwell 10938 and 10939 Dot Matrix Display Controller is a two-chip MOS/LSI general purpose display controller system designed to interface to dot matrix displays (vacuum-fluorescent or LED).

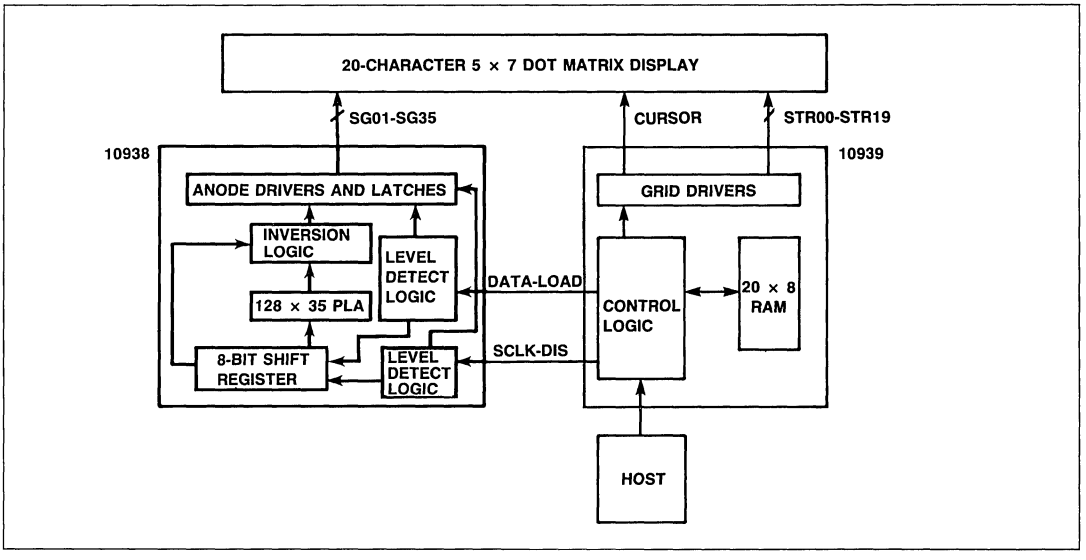
The two-chip set will drive displays with up to 35 anodes (dots) and up to 20 grids (characters) plus a cursor. The chips can be cascaded to drive larger displays of as many as 80 characters. An internal PLA-type decoder provides character decoding and dot pattern generation for the full 96-character ASCII set and an additional 32 special characters.

FEATURES

- 20-character display driver cascadable to 80
- Standard 5 x 7 character font.
- Separate cursor driver output
- Direct drive capability for vacuum-fluorescent displays
- 128 x 35 PLA provides segment decoding for full 96-character ASCII set, plus 32 special characters
- Serial or parallel data input for 8-bit display and control characters
- Brightness, refresh rate, and display mode controls
- 40-pin DIP

ORDERING INFORMATION

Part Number	Package Type	Temperature Range (°C)
10938P	Plastic	0 to +70
10938PE	Plastic	−40 to +85
10939P	Plastic	0 to +70
10939PE	Plastic	−40 to +85

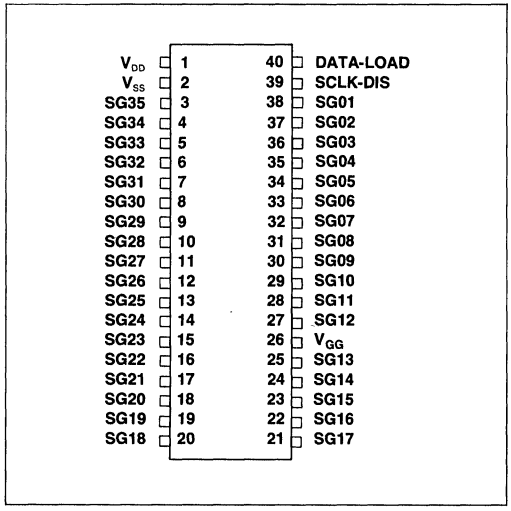


Block Diagram of 10938 and 10939

INTERFACE DESCRIPTION

10938 Pin Functions

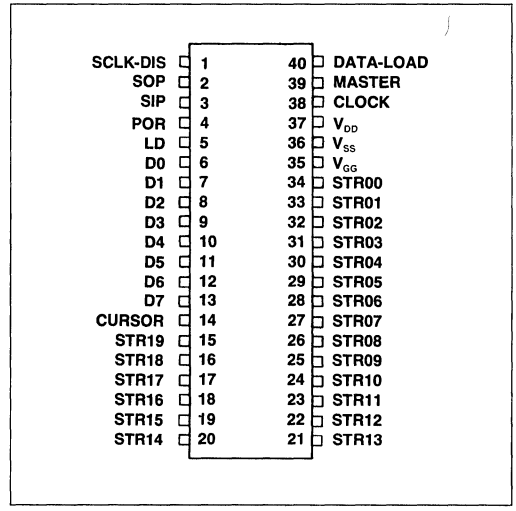
Signal Name	Pin No.	Function
V_{SS}	2	Power and signal reference
SG01-SG35	3-25, 27-38	Anode driver outputs
SCLK-DIS	39	Serial data shift clock
DATA-LOAD	40	Serial data output/latch control
V_{DD}	1	DC Power
V_{GG}	26	Display voltage



10938 Pin Configuration

10939 Pin Functions

Signal Name	Pin No.	Function
V_{SS}	36	Power and signal reference
V_{DD}	37	DC Power
CLOCK	38	Synchronization Clock
CURSOR	14	Cursor drive output
MASTER	39	Master/Slave Mode control
SIP	3	Sync Input
SOP	2	Sync Output
D0-D7	6-13	Serial or parallel data input
LD	5	Input data strobe
POR	4	Power-on reset
SCLK-DIS	1	Serial data shift clock
DATA-LOAD	40	Serial data output/latch control
STR00-STR19	15-34	Grid Driver Outputs
V_{GG}	35	Display voltage



10939 Pin Configuration

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS*

Voltages are referenced to V_{SS}

Parameter	Symbol	Value	Unit
Operating Temperature			
Commercial	Tc	0 to +70	°C
Industrial	Ti	−40 to +85	°C
Storage Temperature		−55 to +125	°C
Operating Voltage	V_{DD}	−22 to −18	Vdc
Operating Display Voltage	V_{GG}	−50	Vdc

***NOTE:** Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in other sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

All voltages referenced to V_{SS}

Parameter	Notes	Symbol	Min	Typ	Max	Unit
Input D0-D7, LD, SIP	2					
Logic "1"		V_{IH}	−1.2		+0.3	V
Logic "0"		V_{IL}	V_{DD}		−4.2	V
Input POR	2					
Logic "1"		V_{IHPO}	−3.0		+0.3	V
Logic "0"		V_{ILPO}	V_{DD}		−10.0	V
Output SOP	2					
Logic "1"		V_{OHSY}	−1.2		V_{SS}	V
Logic "0"		V_{OLSY}	V_{DD}		−4.2	V
Output Grids, Cursor, and Anodes	1					
Logic "1" (I_{load} = 10 mA 10939, 2 mA 10938)		V_{OH}	−1.5		V_{SS}	V
Logic "0" (I_{load} = 0 mA)		V_{OL}	V_{GG}		0.95 × V_{GG}	V

Notes: 1. Designates characteristics for both 10938 and 10939.
2. Designates characteristics for 10939.

OPERATING CURRENTS

Parameter	Maximum		Typical	Unit
	Industrial **TA = −40°C** **V_{DD} = −22 Vdc** **V_{GG} = −50 Vdc**	**Commercial** **TA = 0°C** **V_{DD} = −22 Vdc** **V_{GG} = −50 Vdc**	**TA = 25°C** **V_{DD} = −20 Vdc** **V_{GG} = −50 Vdc**	
10938[1]				
I_{DD}	4.5	3.6	3.2	mA
I_{GG}	11.2	9.0	8.0	mA
10939 (master)[2]				
I_{DD}	13.6	10.9	6.0	mA
I_{GG}	1.0	0.8	0.5	mA
10939 (slave)[2]				
I_{DD}	9.1	7.3	4.0	mA
I_{GG}	1.0	0.8	0.5	mA

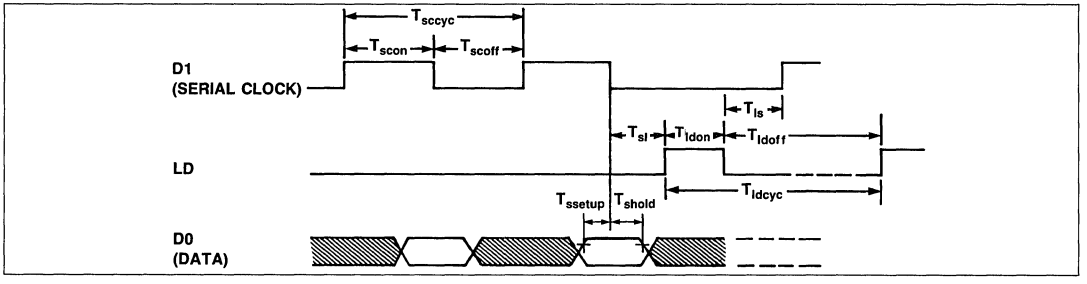
Notes:
1. The 10938 has 35 internal drivers which are brought out. I_{GG} is proportional to the number of drivers on. The values given are for all 35 drivers on. Divide I_{GG} shown by 35 to determine I_{GG} for one driver.
2. The 10939 will never have more than two drivers on at any one time; one grid driver and the cursor. The values shown are for two drivers on with 100% duty cycle.

5

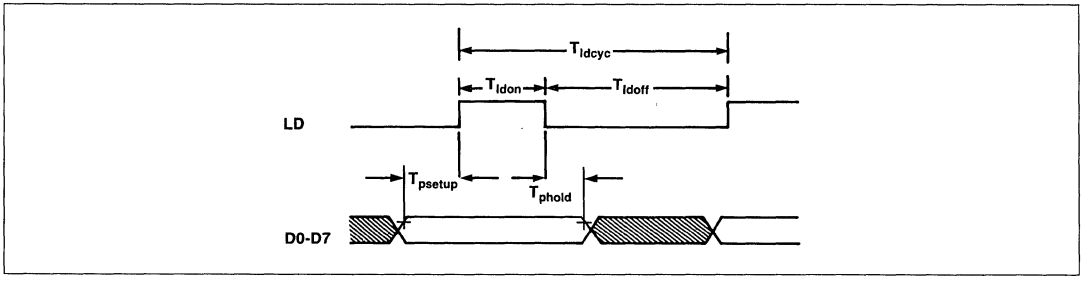
AC CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Unit
GENERAL INTERFACE TIMING					
Data Load (LD)					
On Time	T_{ldon}	1.0			µs
Off time	T_{ldoff}				
Commercial		40.0			µs
Industrial		44.5			µs
Cycle Time	T_{ldcyc}				
Commerical		60.0			µs
Industrial		66.7			µs
SERIAL INTERFACE TIMING					
Serial Clock (D1)					
On Time	T_{scon}	1.0		20.0	µs
Off Time	T_{scoff}	1.0			µs
Cycle Time	T_{sccyc}	2.0			µs
Serial Clock (D0)					
Set-up Time	T_{ssetup}	400			ns
Hold Time	T_{shold}	400			ns
Serial Clock to LD Time	T_{sl}	1.0			µs
LD to Serial Clock	T_{ls}	1.0			µs
PARALLEL INTERFACE TIMING					
Parallel Data (D0–D7)					
Set-up Time	T_{psetup}	0			ns
Hold Time	T_{phold}	200			ns

TIMING WAVEFORMS



Serial Interface Timing Waveforms



Parallel Interface Timing Waveforms

FUNCTIONAL DESCRIPTION

Once the display buffer has been loaded from the host processor, the 10938/10939 system generates all timing signals required to control the display.

Input data is loaded into the Display Data Buffer as a series of 8-bit words via the Serial or Parallel Data Input channel on the 10939. Internal timing and control logic synchronize the digit output signals with the Serial Data and Load signals to the 10938 to provide the proper timing for the multiplexing operation. A 128 x 35 bit PLA is provided for decoding the full 96 character ASCII set, plus 32 special characters.

The parallel data input mode is implemented by toggling any of data lines D2–D7 after POR has gone low. Once the parallel data load mode has been implemented, a power-on reset procedure must be performed to return to serial data load mode. Parallel data transfer is accomplished by putting the command or display data on the data lines, then pulsing the LD line. The load cycle time must be at least 60 μs with the LD line set high for at least one μs and held low for at least 40 μs.

The serial data input mode is implemented during the power-on reset procedure. In those systems using serial mode, ports D2–D7 should be tied low to prevent the inadvertent implementation of the parallel load mode. Serial data bytes are shifted into a data buffer MSB first on line D0 using line D1 as the serial clock. The last eight bits clocked in are latched into the display controller by a pulse on the LD line. The cycle time for each data bit is 2 μs and the load time for each byte is 60 μs.

Input data may be Control or Display data. The following paragraphs describe the format and functions of these control and display data words.

CONTROL DATA WORDS

Control data words are used to select the operating parameters of the display controller. They must be preceded by a Control Prefix word (0000 0001, hexadecimal 01) to be distinguished from Display Data words.

Buffer Pointer Control

The Buffer Pointer Control code sets the Display Data Buffer pointer. The lower 5 bits of the code are loaded into the buffer pointer (see Table 2).

Table 1. Control Word Assignments

Hex Value	Function
00	Not used
01	Load 01 into Data Buffer
02	Not used
03	Not used
04	Not used
05	Set digit time to 16 cycles per grid
06	Set digit time to 32 cycles per grid
07	Set digit time to 64 cycles per grid
08	Enable Normal Display Mode (MSB in data words is used for cursor control only)
09	Enable Blank Mode (data words with MSB = 1 will be blanked and cursor will be on)
0A	Enable Inverse Mode (data words with MSB = 1 will be "inversed" and cursor will be on)
0B	Not used
0C	Not used
0D	Not used
0E	Start Display Refresh Cycle (use only once after reset)
0F	Not used
10–3F	Not used
40–7F	Load Duty Cycle Register with lower 6 bits (0–63)
80–9F	Load Digit Counter (80 = 32, 81 = 1, 82 = 2, etc.)
A0–BF	Not used
C0–D3	Load Buffer Pointer Register with lower 5 bits
E0–FF	Not used

Table 2. Buffer Pointer Control Codes

Code Value	Pointer Value	Character Position
C0	00	0
C1	01	1
C2	02	2
C3	03	3
C4	04	4
C5	05	5
C6	06	6
C7	07	7
C8	08	8
C9	09	9
CA	0A	10
CB	0B	11
CC	0C	12
CD	0D	13
CE	0E	14
CF	0F	15
D0	10	16
D1	11	17
D2	12	18
D3	13	19

Note:
DO NOT USE CHARACTER POSITIONS 20–31 (CODES D4–DF)

5

Digit Counter Control

The Digit Counter Control code defines the number of character positions (grids) to be controlled. This code is normally used only during initialization routines, but it may also be used in conjunction with the Duty Cycle Control code to extend the range of brightness control (see Table 3).

Duty Cycle Control

The Duty Cycle Control code turns the display on and off, adjusts display brightness, and modifies display timing. The time slot for each character is 16, 32, or 64 cycles as selected by the Digit Time Control codes (see Table 1). The anode and grid drivers for each character are on for a maximum of 13, 29, or 61 cycles with a 3 cycle inter-digit off-time. The lower 6 bits of the Duty Cycle Control code are loaded into the Duty Cycle Register. Resultant duty cycles are shown in Table 4.

Table 3. Digit Counter Control Codes

Code	Digit Counter Value	No. of Grids Controlled
80	00	32
81	01	1
82	02	2
83	03	3
84	04	4
85	05	5
86	06	6
87	07	7
88	08	8
89	09	9
8A	0A	10
8B	0B	11
8C	0C	12
8D	0D	13
8E	0E	14
8F	0F	15
90	10	16
91	11	17
92	12	18
93	13	19
94	14	20
95	15	21
96	16	22
97	17	23
98	18	24
99	19	25
9A	1A	26
9B	1B	27
9C	1C	28
9D	1D	29
9E	1E	30
9F	1F	31

Digit Time Select

The Digit Time Select code sets the total time for each character during the refresh cycle. Three values can be set using the three codes shown in Table 1. The default value set at power-on is 64 cycles per grid. For displays with 40 or more characters, or under conditions where the display can be subjected to quick movements during viewing (e.g. portable or vehicle-mounted applications), it may be necessary to increase the refresh rate by selecting 16 or 32 cycles per grid with the appropriate control code.

Table 4. Duty Cycle Control Codes

	Digit Time = 16		Digit Time = 32		Digit Time = 64	
Code	On	Off	On	Off	On	Off
40	—	16	—	32	—	64
41	—	16	—	32	—	64
42	—	16	—	32	—	64
43	1	15	1	31	1	63
44	2	14	2	30	2	62
45	3	13	3	29	3	61
46	4	12	4	28	4	60
47	5	11	5	27	5	59
48	6	10	6	26	6	58
49	7	9	7	25	7	57
4A	8	8	8	24	8	56
4B	9	7	9	23	9	55
4C	10	6	10	22	10	54
4D	11	5	11	21	11	53
4E	12	4	12	20	12	52
4F	13	3	13	19	13	51
50	13	3	14	18	14	50
51	13	3	15	17	15	49
52	13	3	16	16	16	48
53	13	3	17	15	17	47
•	•	•	•	•	•	•
•	•	•	•	•	•	•
•	•	•	•	•	•	•
5B	13	3	25	7	25	39
5C	13	3	26	6	26	38
5D	13	3	27	5	27	37
5E	13	3	28	4	28	36
5F	13	3	29	3	29	35
60	13	3	29	3	30	34
61	13	3	29	3	31	33
62	13	3	29	3	32	32
•	•	•	•	•	•	•
•	•	•	•	•	•	•
•	•	•	•	•	•	•
7C	13	3	29	3	58	6
7D	13	3	29	3	59	5
7E	13	3	29	3	60	4
7F	13	3	29	3	61	3

Display Mode Select

Each ASCII character is represented by the lower seven bits of the 8-bit value loaded into the 10939. The eighth (most significant) bit controls the cursor (see Cursor Control). This bit is known as the data byte control bit. If either Blank or Inverse mode is selected, a "0" in this bit causes a normal character display, while "1" selects either Blank or Inverse mode, depending on which mode is enabled. Three control codes are provided (see Table 1) to enable Blank Mode, Inverse Mode, or Normal Display Mode.

In the Blank mode, any character with the MSB = "1" will be blanked. In the Inverse mode, it will be displayed with all segment driver outputs inverted. On video displays, this is referred to as "Inverse Video" format. These controls allow individual characters or groups of characters to be blinked or blanked by simply changing the mode without changing the data in the Display Buffer.

Cursor Control

The data byte control bit (MSB 8), besides selecting Blank, Inverse, or Normal mode, also controls the cursor output which is enabled on all characters with the MSB equal to one. Therefore, when the Normal mode is enabled and the MSB of the data byte is set to a one, the normal character is displayed with the cursor on. When the Blank mode is enabled and the MSB is set to a one, the character is blanked but the cursor is on. If Inverse mode is enabled and the MSB is set to a one, the inverse character is displayed and the cursor is on but not inversed.

Start Refresh

At power on, the 10939 is held in an internal halt mode. The normal display refresh sequence starts upon receipt of a Start Refresh control code. This is particularly useful for synchronizing systems using more than one 10939. Only the Master 10939 in a multi-chip system will recognize the Start Refresh code. The Master starts the Slave(s) at the appropriate time, using the SOP signal.

INPUT DISPLAY DATA WORDS

Display data words are loaded as 8-bit codes. The eighth (most significant) bit specifies normal (0) or blank/inverse (1) display mode, depending on the blank/inverse mode selection (see Control data words 09 and 0A in Table 1). This bit also controls the cursor.

Twenty display data words must be entered to completely load the Display Data Buffer. The Buffer Pointer automatically increments after each data word is stored in the buffer. To select a character position to be loaded out of sequence, use the Buffer Pointer control code. The Buffer Pointer will automatically reset to character position 0 when its value is equal to the programmed Digit Count.

POWER-ON RESET

The Power-On Reset (POR) initializes the internal circuits of the 10939. This is normally accomplished when power (V_{DD}) is applied. The following conditions are established by application of POR:

a. The Grid Drivers (STR00–STR19) on the 10939 are in the off state.
b. The Anode Drivers (SG01–SG35) on the 10938 are in the off state.
c. The Duty Cycle is set to 0.
d. The Digit Counter is set to 32.
e. The Buffer Pointer is set to 0.
f. The Digit time is set to 64.
g. The Normal display mode is set.
h. DATA-LOAD is set to high impedance state.
i. SCLK-DIS is set to V_{OL} to disable the anode drivers in the 10938.
j. SOP is set to V_{OL} to disable the sync pulse.

NOTE:

1. When the POR signal is removed, SCLK-DIS is set to the high impedance state.
2. During the initial rise time of V_{DD} at power turn-on, the magnitude of V_{GG} should not exceed the magnitude of V_{DD}.

GRID (DIGIT) DRIVERS (STR00–STR19) PLUS CURSOR

The 20 Digit Drivers select each of the display character positions sequentially during a refresh scan. Display dots will be illuminated when both the Digit Drivers and Dot Drivers for a particular character are energized simultaneously. The cursor segment is generated by the 10939, but its timing characteristics are identical to the anode timing generated by the 10938.

ANODE (DOT) DRIVERS (SG01–SG35)

35 Dot Drivers are provided in the 10938. The output states for each character pattern are internally decoded from the 8-bit characters received from the 10939 by means of a 128 × 35-bit PLA. Data codes and the corresponding patterns are shown in Figure 1. Figure 2 shows the Dot Driver (SG01–SG35) assignments as they relate to the 5 × 7 dot matrix patterns.

TYPICAL SYSTEM HOOKUPS

Figure 3 shows a 10938 and 10939 in a parallel interface with the host system driving a 20 character display. Figure 4 shows a 10938 and a 10939 in a serial interface with the host system driving a 20 character display. Figure 5 shows a 10938 and two 10939's in a parallel interface with the host system driving a 40 character display.

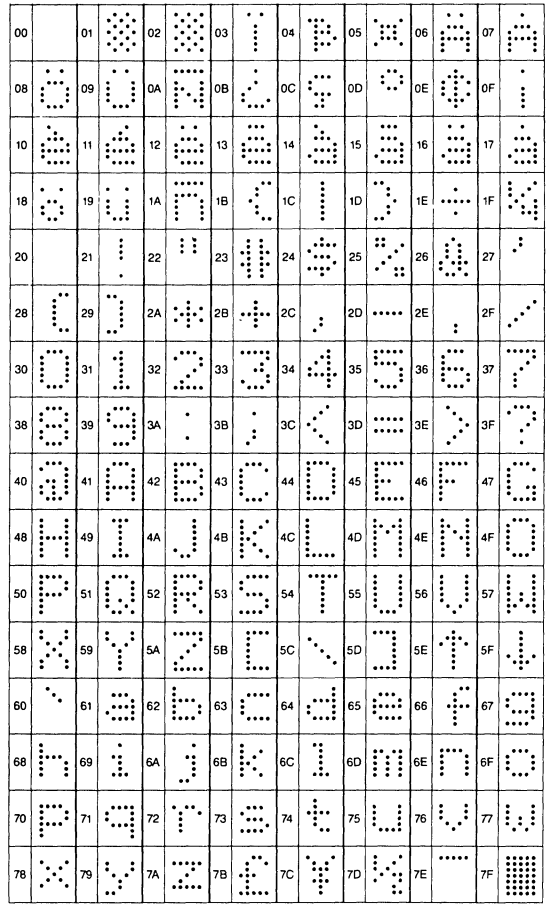


Figure 1. 5 x 7 Dot Matrix PLA Patterns

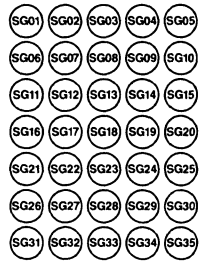


Figure 2. Anode (Dot) Driver Assignments

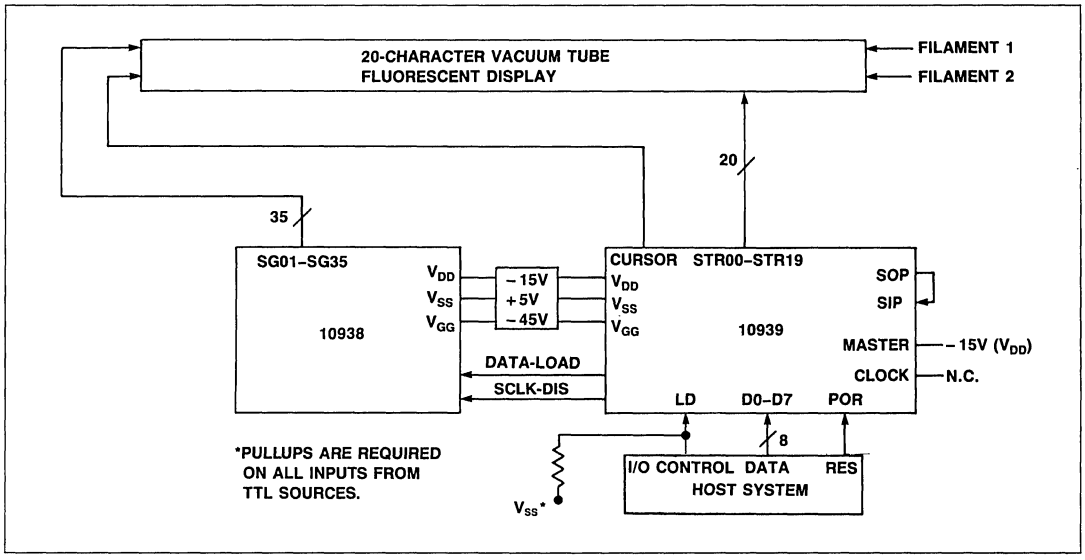


Figure 3. Typical Display System with Parallel Interface to Host System

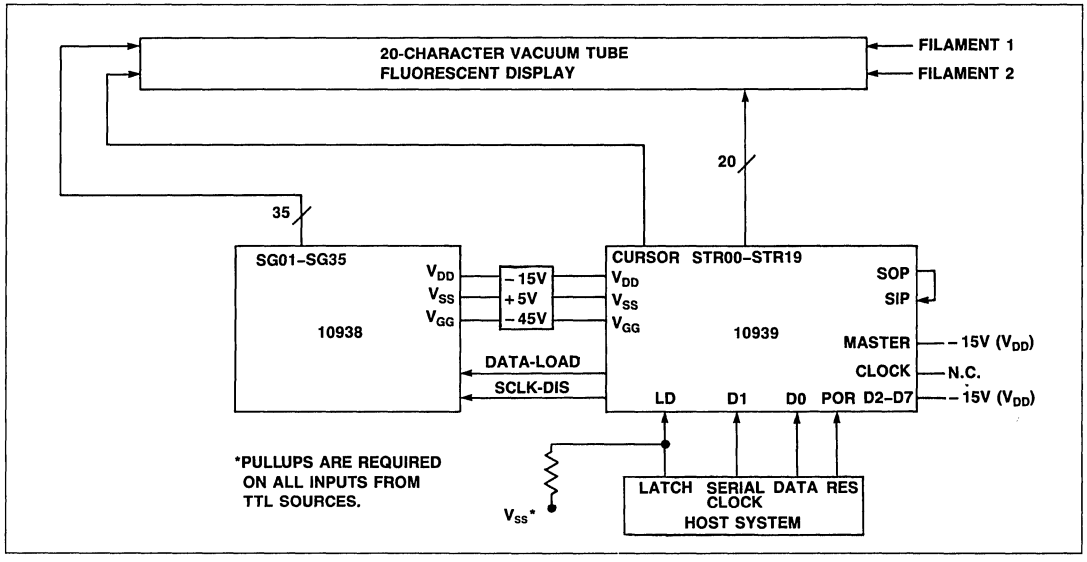


Figure 4. Typical Display System with Serial Interface to Host System

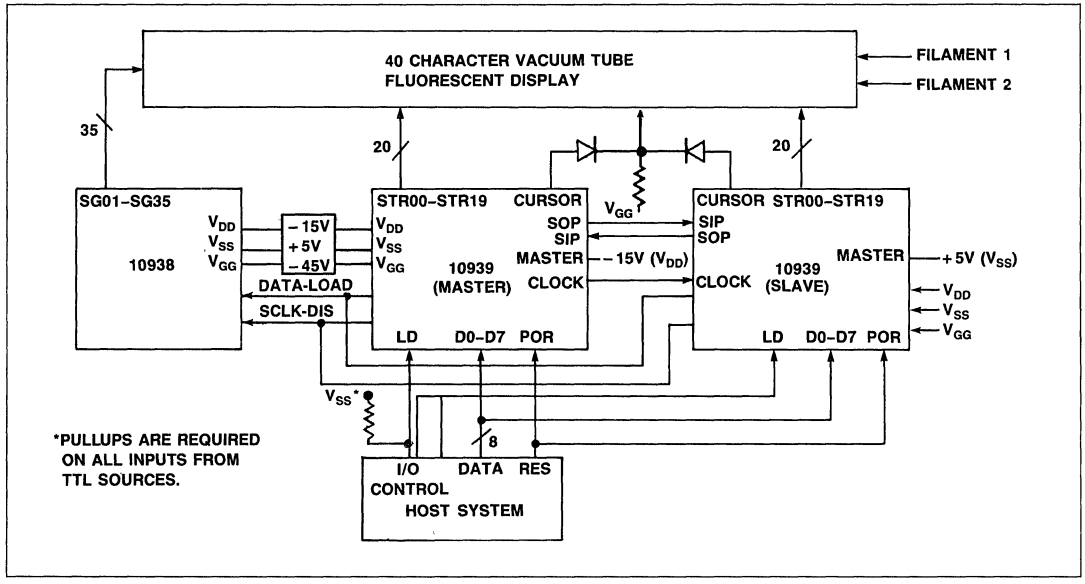


Figure 5. Typical Display System with Parallel Interface to Host and Two 10939 Devices

Rockwell

10939, 10942, and 10943 Dot Matrix Display Controller

DESCRIPTION

The Rockwell 10939, 10942, and 10943 Dot Matrix Display Controller is a three-chip MOS/LSI general purpose display controller system designed to interface to dot matrix displays (vacuum-fluorescent or LED).

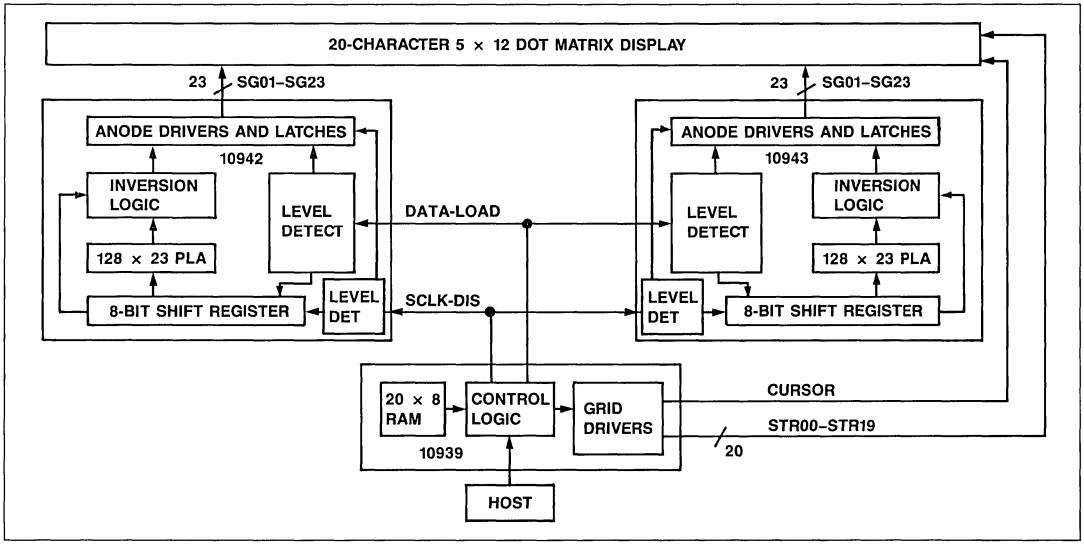
The three-chip set will drive displays with up to 46 anodes (dots) and up to 20 grids (characters) plus a cursor. The chips can be cascaded to drive larger displays of up to 80 characters. An internal PLA-type decoder provides character decoding and dot pattern generation for the full 96-character ASCII set and an additional 32 special characters.

FEATURES

- 20-character display driver cascadable to 80 characters
- Standard 5 x 12 character font
- Separate cursor driver output
- Two 128 x 23 PLAs provide decoding for full 96-character ASCII set plus 32 special characters
- Serial or parallel data input for 8-bit display and control characters
- Brightness, refresh rate, and display mode controls
- 10939 provided in 40-pin DIP
- 10942 and 10943 provided in 28-pin DIP

ORDERING INFORMATION

Part Number	Package Type	Temperature Range (°C)
10939P	Plastic	0 to +70
10939PE	Plastic	−40 to +85
10942P	Plastic	0 to +70
10942PE	Plastic	−40 to +85
10943P	Plastic	0 to +70
10943PE	Plastic	−40 to +85

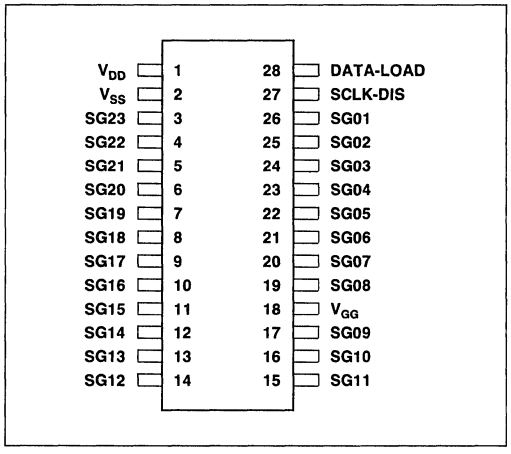


Block Diagram of 10939, 10942, 10943

INTERFACE DESCRIPTION

10942 and 10943 Pin Functions

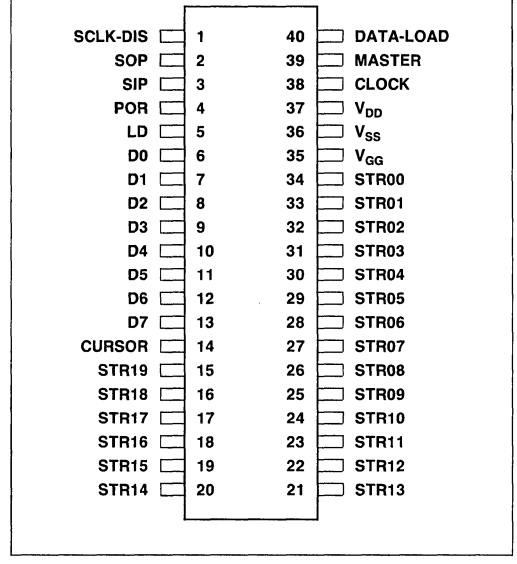
Signal Name	Pin No.	Function
V_{DD}	1	DC Power
V_{SS}	2	Power and signal reference
SG01–SG23	3–17, 19–26	Anode (Dot) driver outputs
V_{GG}	18	Display voltage
SCLK-DIS	27	Serial data shift clock
DATA-LOAD	28	Serial data output/latch control



10942 and 10943 Pin Configurations

10939 Pin Functions

Signal Name	Pin No.	Function
V_{SS}	36	Power and signal reference
V_{DD}	37	DC Power
CLOCK	38	Synchronization Clock
CURSOR	14	Cursor driver output
MASTER	39	Master/Slave Mode control
SIP	3	Sync Input
SOP	2	Sync Output
D0–D7	6–13	Serial or parallel data input
LD	5	Input data strobe
POR	4	Power-on reset
SCLK-DIS	1	Serial data shift clock
DATA-LOAD	40	Serial data output/latch control
STR00–STR19	15–34	Digit (grid) driver outputs
V_{GG}	35	Display voltage



10939 Pin Configurations

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS*

Voltages are referenced to V_{SS}, where V_{SS} = +5 Vdc

Parameter	Symbol	Value	Unit
Operating Temperature	T_A		
Commercial		0 to +70	°C
Industrial		−40 to +85	°C
Storage Temperature	T_S	−55 to +125	°C
Operating Voltage	V_{DD}	−22 to −18 −20 typical	Vdc
Operating Display Voltage	V_{GG}	−50	Vdc

***NOTE:** Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the other sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

(V_{DD} = −18.0 to −22 Vdc, V_{SS} = 0 Vdc, unless otherwise noted. All voltages referenced to V_{SS}.)

Parameter	Symbol	Min.	Typical	Max.	Unit
10942 and 10943					
Output Anodes (Dots)					
Logic "1" (I_{LOAD} = 2 mA)	V_{OH}	−1.5		V_{SS}	V
Logic "0" (I_{LOAD} = 0 mA)	V_{OL}	V_{GG}		0.95 × V_{GG}	V
10939					
Input D0–D7, LD, SIP					
Logic "1"	V_{IH}	−1.2		+0.3	V
Logic "0"	V_{IL}	V_{DD}		−4.2	V
Input POR					
Logic "1"	V_{IHPO}	−3.0		+0.3	V
Logic "0"	V_{ILPO}	V_{DD}		−10.0	V
Output SOP					
Logic "1"	V_{OHSY}	−1.2		V_{SS}	V
Logic "0"	V_{OLSY}	V_{DD}		−4.2	V
Output Digits, Cursor					
Logic "1" (I_{LOAD} = 10 mA)	V_{OH}	−1.5		V_{SS}	V
Logic "0" (I_{LOAD} = 0 mA)	V_{OL}	V_{GG}		0.95 × V_{GG}	V

Note: TA = 0°C to +70°C (commercial) or −40°C to +85°C (industrial), unless otherwise noted.

OPERATING CURRENTS

Parameter	Maximum		Typical	Unit
	Industrial TA = −40°C V_{DD} = −22 Vdc V_{GG} = −50 Vdc	**Commercial** TA = 0°C V_{DD} = −22 Vdc V_{GG} = −50 Vdc	TA = 25°C V_{DD} = −20 Vdc V_{GG} = −50 Vdc	
10942 or 10943				
I_{DD}	4.5	3.6	3.2	mA
I_{GG}[1]	7.4	5.9	5.3	mA
10939 (master)				
I_{DD}	13.6	10.9	6.0	mA
I_{GG}[2]	1.0	0.8	0.5	mA
10939 (slave)				
I_{DD}	9.1	7.3	4.0	mA
I_{GG}[2]	1.0	0.8	0.5	mA

Notes:
1. The 10942 and 10943 each have 23 driver outputs. I_{GG} is proportional to the number of drivers on. The values given are for all 23 drivers on. Divide I_{GG} shown by 23 to determine I_{GG} for one driver. Multiply I_{GG} by 2 to find total current requirements for all drivers on for both devices.
2. The 10939 will never have more than two drivers on at any one time; one grid driver and the cursor. The values shown are for two drivers on with 100% duty cycle.

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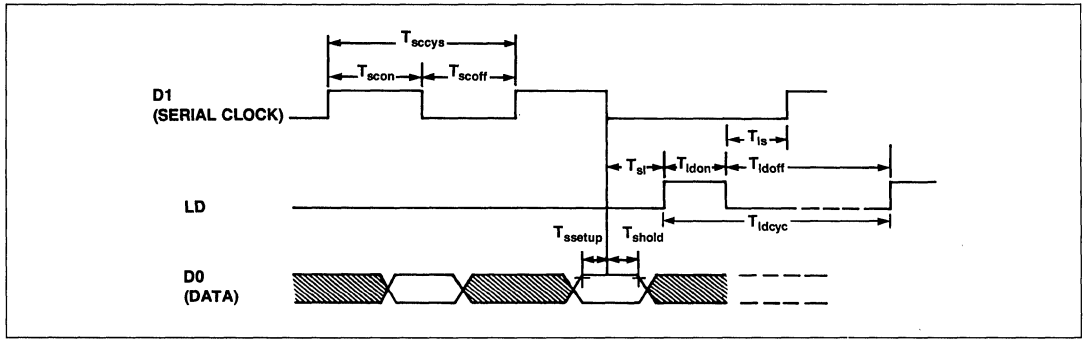
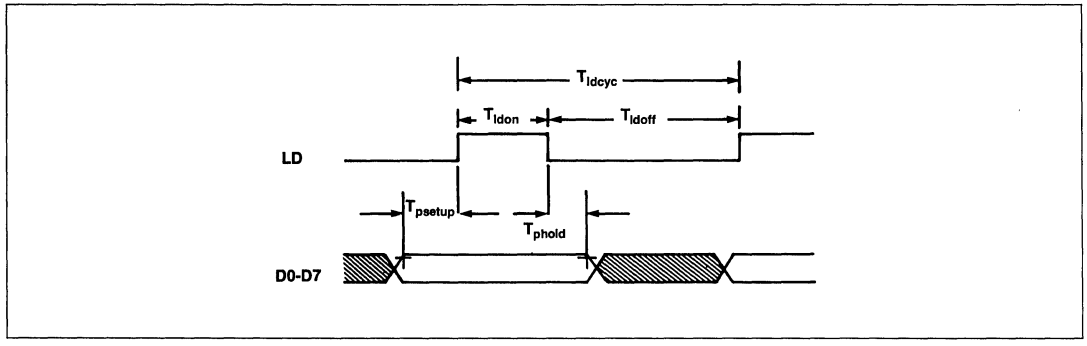
AC CHARACTERISTICS

Parameter	Symbol	Min.	Typical	Max.	Unit
Data Load (LD)					
On Time	T_{ldon}	1.0			µs
Off Time	T_{ldoff}				
Commercial		40.0			µs
Industrial		44.5			µs
Cycle Time	T_{ldcyc}				
Commercial		60.0			µs
Industrial		66.7			µs
SERIAL INTERFACE TIMING					
Serial Clock (D1)					
On Time	T_{scon}	1.0		20.0	µs
Off Time	T_{scoff}	1.0			µs
Cycle Time	T_{sccyc}	2.0			µs
Serial Data (D0)					
Set-up time	T_{ssetup}	400			ns
Hold Time	T_{shold}	400			ns
Serial Clock to LD Time	T_{sl}	1.0			µs
LD to Serial Clock	T_{ls}	1.0			µs
PARALLEL INTERFACE TIMING					
Parallel Data (D0–D7)					
Set-up Time	T_{psetup}	0			ns
Hold Time	T_{phold}	200			ns

TIMING WAVEFORMS



Serial Interface Timing Waveforms



Parallel Interface Timing Waveforms

FUNCTIONAL DESCRIPTION

Once the display buffer has been loaded from the host processor, the 10939, 10942, and 10943 system generates all timing signals required to control the display.

Input data is loaded into the Display Data Buffer as a series of 8-bit words via the Serial or Parallel Data Input channel on the 10939. Internal timing and control logic synchronize the digit output signals with the Serial Data and Load signals to the 10942/10943 to provide the proper timing for the multiplexing operation. Two 128 × 23 bit PLAs, one in the 10942 and the other in the 10943, decode the full 96-character ASCII set plus 32 special characters.

The parallel data input mode is implemented by toggling any of data lines D2–D7 after POR has gone low. Once the parallel data load mode has been implemented, a power-on reset procedure must be performed to return to serial data load mode. Parallel data transfer is accomplished by putting the command or display data on the data lines, then pulsing the LD line. The load cycle time must be at least 60 μs with the LD line set high for at least one μs and held low for at least 40 μs.

The serial data input mode is implemented during the power-on reset procedure. In those systems using serial mode, ports D2–D7 should be tied low to prevent the inadvertent implementation of the parallel load mode. Serial data bytes are shifted into a data buffer MSB first on line D0 using line D1 as the serial clock. The last eight bits clocked in are latched into the display controller by a pulse on the LD line. The cycle time for each data bit is 2 μs and the load time for each byte is 60 μs.

Input data may be Control or Display data. The following paragraphs describe the format and functions of these control and display data words.

CONTROL DATA WORDS

Control data words are used to select the operating parameters of the display controller. They must be preceded by a control prefix word (0000 0001, hexadecimal 01) to be distinguished from display data words.

Buffer Pointer Control

The Buffer Pointer Control code sets the Display Data Buffer pointer. The lower 5 bits of the code are loaded into the buffer pointer (see Table 2).

Digit Counter Control

The Digit Counter Control code defines the number of character positions (grids) to be controlled. This code is normally used only during initialization routines, but it may also be used in conjunction with the Duty Cycle Control code to extend the range of brightness control (see Table 3).

Duty Cycle Control

The Duty Cycle Control code is used to turn the display on and off, to adjust display brightness, or to modify display timing. The time slot for each character is 16, 32, or 64 cycles as selected by the Digit Time Control codes (see Table 1). The segment and digit drivers for each character are on for a maximum of 13, 29, or 61 cycles with a 3 cycle inter-digit off-time. The lower 6 bits of the Duty Cycle Control code are loaded into the Duty Cycle Register. Resultant duty cycles are shown in Table 4.

Table 1. Control Word Assignments

Hex Value	Function
00	Not Used
01	Load 01 into Data Buffer
02	Not used
03	Not used
04	Not used
05	Set Digit Time to 16 cycles per grid
06	Set Digit Time to 32 cycles per grid
07	Set Digit Time to 64 cycles per grid
08	Enable Normal Display Mode (MSB in data words is ignored
09	Enable Blank Mode (data words with MSB = 1 will be blanked)
0A	Enable Inverse Mode (data words with MSB = 1 will be "inversed")
0B	Not used
0C	Not used
0D	Not used
0E	Start Display Refresh Cycle (use only once after reset)
0F	Not used
10–3F	Not used
40–7F	Load Duty Cycle Register
80–9F	Load Digit Counter (80 = 32, 81 = 1, 82 = 2, etc.)
A0–BF	Not used
C0–DF	Load Buffer Pointer Register with lower 5 bits
E0–FF	Not used

Table 2. Buffer Pointer Control Codes

Code Value	Pointer Value	Character Position
C0	00	0
C1	01	1
C2	02	2
C3	03	3
C4	04	4
C5	05	5
C6	06	6
C7	07	7
C8	08	8
C9	09	9
CA	0A	10
CB	0B	11
CC	0C	12
CD	0D	13
CE	0E	14
CF	0F	15
D0	10	16
D1	11	17
D2	12	18
D3	13	19

Note: Do not use character positions 20–31 (Codes D4-DF).

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Table 3. Digit Counter Control Codes

Code	Digit Counter Value	No. of Grids Controlled
80	00	32
81	01	1
82	02	2
83	03	3
84	04	4
85	05	5
86	06	6
87	07	7
88	08	8
89	09	9
8A	0A	10
8B	0B	11
8C	0C	12
8D	0D	13
8E	0E	14
8F	0F	15
90	10	16
91	11	17
92	12	18
93	13	19
94	14	20
95	15	21
96	16	22
97	17	23
98	18	24
99	19	25
9A	1A	26
9B	1B	27
9C	1C	28
9D	1D	29
9E	1E	30
9F	1F	31

Digit Time Select

The Digit Time Select code sets the total time for each character during the refresh cycle. Three values can be set using the three codes shown in Table 1. The default value set at power-on is 64 cycles per grid. For displays with 40 or more characters,or under conditions where the display can be subjected to quick movements during viewing (e.g. portable or vehicle-mounted applications), it may be necessary to increase the refresh rate by selecting 16 or 32 cycles per grid with the appropriate control code.

Display Mode Select

Each ASCII character is represented by the lower seven bits of the 8-bit value loaded into the 10939. The eighth (most significant) bit is used to turn the cursor (see Cursor Control) on in Normal display mode. If either Blank or Inverse mode is selected, a "0" in this bit causes a normal character display mode, while a "1" selects either Blank or Inverse mode, depending on which mode is enabled. Three control codes are provided (see Table 1) to enable Blank Mode, Inverse Mode, or Normal Display Mode.

In the Blank mode, any character with the MSB = "1" will be blanked. In the Inverse mode, it will be displayed with all segment driver outputs inverted. On video displays, this is referred to as "Inverse Video" format. These controls allow individual characters or groups of characters to be blinked or blanked by simply changing the mode without changing the data in the Display Buffer.

Table 4. Duty Cycle Control Codes

	Digit Time = 16		Digit Time = 32		Digit Time = 64	
Code	On	Off	On	Off	On	Off
40	—	16	—	32	—	64
41	—	16	—	32	—	64
42	—	16	—	32	—	64
43	1	15	1	31	1	63
44	2	14	2	30	2	62
45	3	13	3	29	3	61
46	4	12	4	28	4	60
47	5	11	5	27	5	59
48	6	10	6	26	6	58
49	7	9	7	26	7	57
4A	8	8	8	24	8	56
4B	9	7	9	23	9	55
4C	10	6	10	22	10	54
4D	11	5	11	21	11	53
4E	12	4	12	20	12	52
4F	13	3	13	19	13	51
50	13	3	14	18	14	50
51	13	3	15	17	15	49
52	13	3	16	16	16	48
53	13	3	17	15	17	47
.	.	.	.	.	.	.
.	.	.	.	.	.	.
.	.	.	.	.	.	.
5B	13	3	25	7	25	39
5C	13	3	26	6	26	38
5D	13	3	27	5	27	37
5E	13	3	28	4	28	36
5F	13	3	29	3	29	35
60	13	3	29	3	30	34
61	13	3	29	3	31	33
62	13	3	29	3	32	32
.	.	.	.	.	.	.
.	.	.	.	.	.	.
.	.	.	.	.	.	.
7C	13	3	29	3	58	6
7D	13	3	29	3	59	5
7E	13	3	29	3	60	4
7F	13	3	29	3	61	3

Cursor Control

The data byte control (MSB 8), besides selecting Blank, Inverse, or Normal mode, also controls the cursor output which is enabled on all characters with the MSB equal to one. Therefore, when the Normal mode is enabled and the MSB of the data byte is set to a one, the normal character is displayed with the cursor on. When the Blank mode is enabled and the MSB is set to a one, the character is blanked but the cursor is on. If Inverse mode is enabled and the MSB is set to a one, the inverse character is displayed, and the cursor is on but not inversed.

Start Refresh

At power on, the 10939 is held in an internal halt mode. The normal display refresh sequence starts upon receipt of a Start Refresh control code. This is particularly useful for synchronizing systems using more than one 10939. Only the Master 10939 in a multi-chip system will recognize the Start Refresh code. The Master starts the Slave(s) at the appropriate time, using the SOP signal.

INPUT DISPLAY DATA WORDS

Display data words are loaded as 8-bit codes. The eighth (most significant) bit is a dual purpose bit. This bit specifies normal (0) or blank/inverse (1) display mode, depending on the blank/inverse mode selection (see control data words 09 and 0A in Table 1). It also controls the cursor output from the 10939; on (1) or off (0). Note, that this bit always controls the cursor no matter what display mode is selected.

Twenty display data words must be entered to completely load the Display Data Buffer. The Buffer Pointer automatically increments after each data word is stored in the buffer. To select a character position to be loaded out of sequence, use the Buffer Pointer Control code command. The Buffer Pointer will automatically reset to character position 0 when its value is equal to the programmed Digit Count.

DIGIT GRID DRIVERS (STR00–STR19) PLUS CURSOR

The 20 Digit Drivers select each of the display character positions sequentially during a refresh scan. Display dots are illuminated when both the Digit Drivers and Anode (Dot) Drivers for a particular character are energized simultaneously. The Cursor output is generated by the 10939, but its timing characteristics are identical to the 46 segment outputs generated by the 10942 and the 10943.

ANODE (DOT) DRIVERS (SG01–SG23)

A total of 46 Dot Drivers are provided by the 10942 and the 10943. The output states for each ASCII charcter pattern are internally decoded from the 8-bit characters received from the 10939 by means of two 128 × 23-bit PLAs, one in the 10942 and the other in the 10943. Figure 1 shows the dot matrix drivers (SG01–SG23) as they relate to the 10942 and 10943. Data codes and the corresponding character patterns are also shown in Figure 1.

POWER-ON RESET

The Power-On Reset (POR) initializes the internal circuits of the 10939. This is normally accomplished when power (V_{DD}) is applied. The following conditions are established by the application of POR:

a. The Grid Drivers (STR00–STR19) on the 10939 are in the off state.
b. The Anode Drivers, SG01–SG23 on the 10942 and SG01–SG23 on the 10943, are in the off state.
c. The Duty Cycle is set to 0.
d. The Digit Counter is set to 32.
e. The Buffer Pointer is set to 0.
f. The Digit time is set to 64.
g. The Normal display mode is set.
h. DATA-LOAD is set to high impedance state.
i. SCLK-DIS is set to V_{OL} to disable the anode drivers in the 10942 and 10943.
j. SOP is set to V_{OL} to disable the sync pulse.

NOTE:

1. When th POR signal is removed, SCLK-DIS is set to the high impedance state.
2. During the initial rise time of V_{DD} at power turn-on, the magnitude of V_{GG} should not exceed the magnitude of V_{DD}.

TYPICAL SYSTEM HOOKUPS

Figure 2 shows a 10939, 10942, and a 10943 in a parallel interface with the host system driving a 20-character display. Figure 3 shows a 10939, 10942, and a 10943 in a serial interface with the host system driving a 20-character display. Figure 4 shows two 10939s, a 10942, and a 10943 in a parallel interface with the host system driving a 40-character display.

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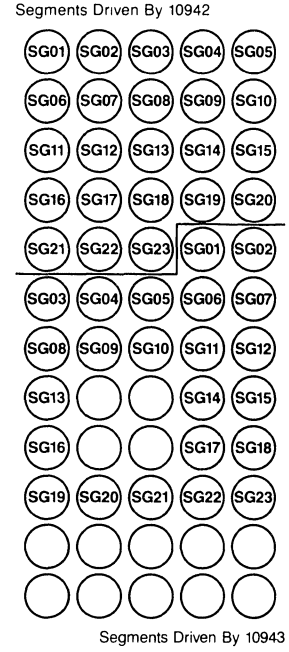
Input Data	Character	Input Data	Character	Input Data	Character	Input Data	Character	Input Data	Character	Input Data	Character	Input Data	Character	Input Data	Character
00		01		02		03		04		05		06		07	
08		09		0A		0B		0C		0D		0E		0F	
10		11		12		13		14		15		16		17	
18		19		1A		1B		1C		1D		1E		1F	
20		21		22		23		24		25		26		27	
28		29		2A		2B		2C		2D		2E		2F	
30		31		32		33		34		35		36		37	
38		39		3A		3B		3C		3D		3E		3F	
40		41		42		43		44		45		46		47	
48		49		4A		4B		4C		4D		4E		4F	
50		51		52		53		54		55		56		57	
58		59		5A		5B		5C		5D		5E		5F	
60		61		62		63		64		65		66		67	
68		69		6A		6B		6C		6D		6E		6F	
70		71		72		73		74		75		76		77	
78		79		7A		7B		7C		7D		7E		7F	



10942 and 10943 Driver Assignments

Figure 1. 5 × 12 Dot Matrix PLA Patterns and Driver Assignments

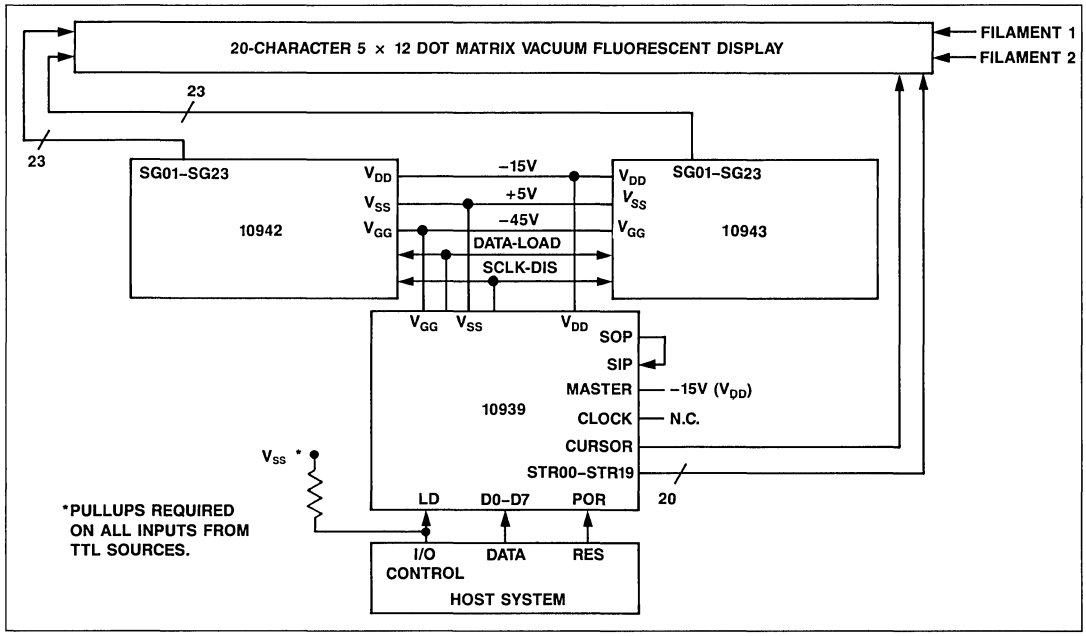


Figure 2. Typical Display System with Parallel Interface to Host System

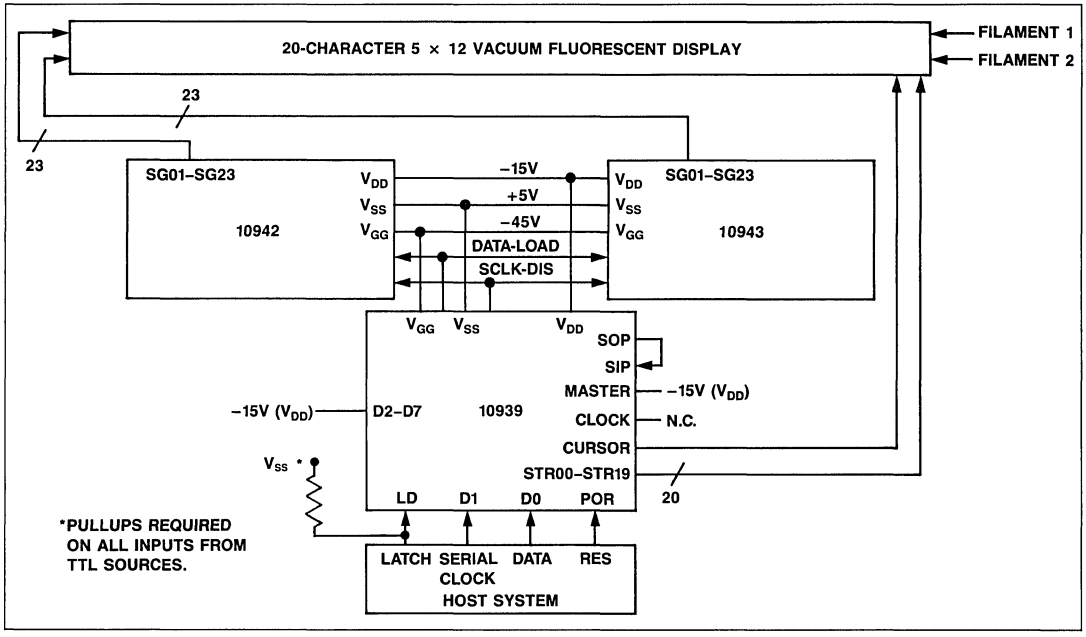


Figure 4. Typical Display System with Serial Interface to Host System

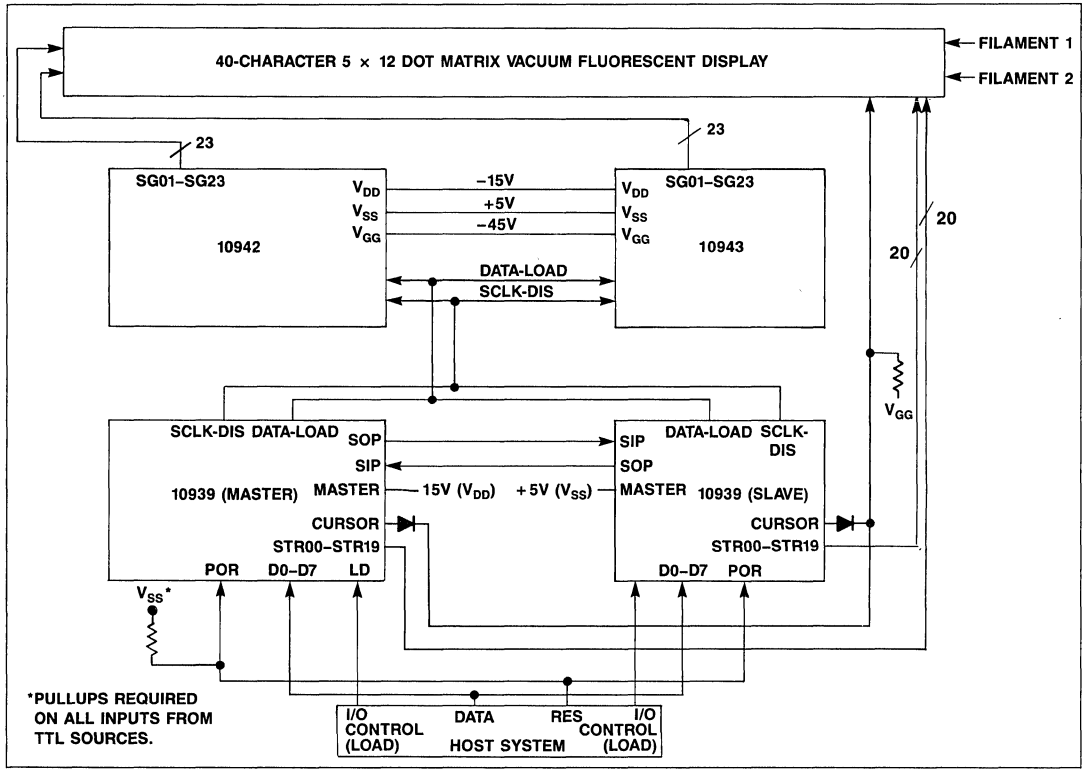


Figure 4. Typical Display System with Parallel Interface to Host and Two 10939 Devices

Rockwell

10941 and 10939 Alphanumeric and Bargraph Display Controller

DESCRIPTION

The Rockwell 10939 and 10941 Alphanumeric and Bargraph Display Controller is a two-chip MOS/LSI general purpose display controller system designed to interface with bargraph and segmented displays (vacuum-fluorescent or LED).

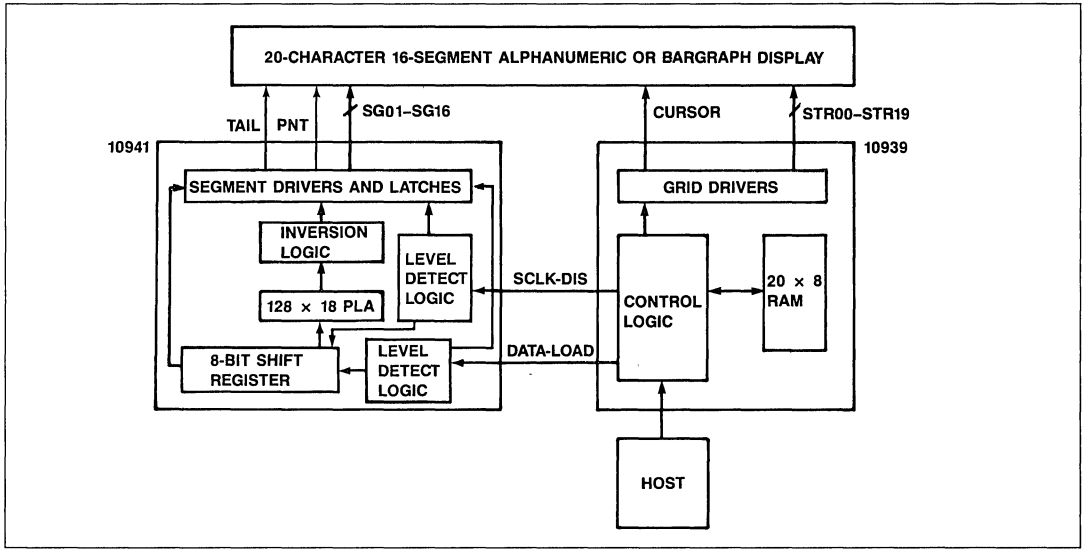
The two-chip set will drive displays with up to 16 segments (plus decimal point and comma tail) and up to 20 grids (characters) plus a cursor. The chips can be cascaded to drive larger displays of 80 characters. Segment decoding for ASCII characters and bargraph patterns is accomplished through an internal PLA.

FEATURES

- 20-character display driver cascadable to 80 characters
- Direct drive capability for vacuum-fluorescent displays
- 128 x 18 PLA provides segment decoding for ASCII characters (all caps only) and bargraph patterns
- Serial or parallel data input for 8-bit display and control characters
- Brightness, refresh rate, and display mode controls
- Separate cursor driver output
- 10939—40-pin DIP package
- 10941—24-pin DIP package

ORDERING INFORMATION

Part Number	Package Type	Temperature Range (°C)
10941P	Plastic	0 to +70
10941PE	Plastic	−40 to +85
10939P	Plastic	0 to +70
10939PE	Plastic	−40 to +85

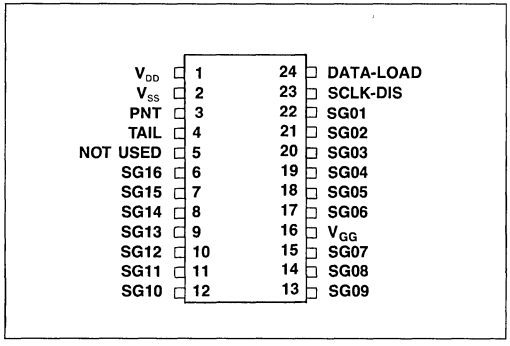


Block Diagram of 10941 and 10939

INTERFACE DESCRIPTION

10941 Pin Functions

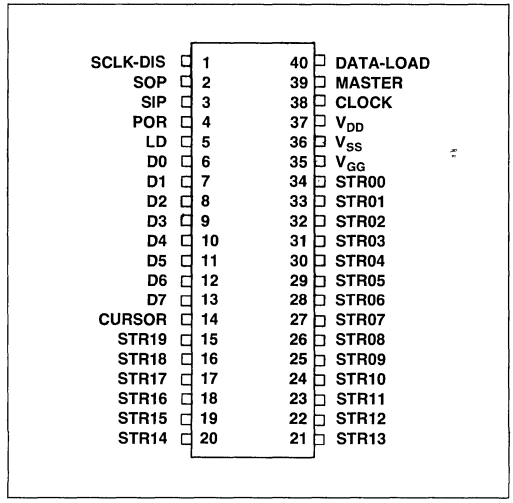
Signal Name	Pin No.	Function
V_{SS}	2	Power and signal reference
SG01-SG16	6-15, 17-22	Segment driver outputs
SCLK-DIS	23	Serial data shift clock
DATA-LOAD	24	Serial data output/latch control
PNT	4	Decimal Point driver output
TAIL	5	Comma Tail driver output
V_{DD}	1	DC Power
V_{GG}	16	Display voltage



10941 Pin Configuration

10939 Pin Functions

Signal Name	Pin No.	Function
V_{SS}	36	Power and signal reference
V_{DD}	37	DC Power
CLOCK	38	Synchronization Clock
CURSOR	14	Cursor driver output
MASTER	39	Master/Slave Mode control
SIP	3	Sync Input
SOP	2	Sync Output
D0-D7	6-13	Serial or parallel data input
LD	5	Input data strobe
POR	4	Power-on reset
SCLK-DIS	1	Serial data shift clock
DATA-LOAD	40	Serial data output/latch control
STR00-STR19	15-34	Grid Driver Outputs
V_{GG}	35	Display voltage



10939 Pin Configuration

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS*

Voltages are referenced to V_{SS}

Parameter	Symbol	Value	Unit
Operating Temperature			
Commercial		0 to +70	°C
Industrial	Tc	−40 to +85	°C
Storage Temperature	Ti	−55 to +125	°C
Operating Voltage	V_{DD}	−22 to −18 −20 (typical)	Vdc
Operating Display Voltage	V_{GG}	−50	Vdc

***NOTE:** Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in other sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

All voltages referenced to V_{SS}

Parameter	Symbol	Min	Typ	Max	Unit
10941					
Output Segments					
Logic "1" (I_{load} = 2 mA)	V_{OH}	−1.5		V_{SS}	V
Logic "1" (I_{LOAD} = 0 mA)	V_{OL}	V_{GG}		0.95 × V_{GG}	V
10939					
Input D0-D7, LD, SIP					
Logic "1"	V_{IH}	−1.2		+0.3	V
Logic "0"	V_{IL}	V_{DD}		−4.2	V
Input POR					
Logic "1"	V_{IHPO}	−3.0		+0.3	V
Logic "0"	V_{ILPO}	V_{DD}		−10.0	V
Output SOP					
Logic "1"	V_{OHSY}	−1.2		V_{SS}	V
Logic "0"	V_{OLSY}	V_{DD}		−4.2	V
Output Digits, Cursor					
Logic "1" (I_{load} = 10 mA)	V_{OH}	−1.5		V_{SS}	V
Logic "0" (I_{load} = 0 mA)	V_{OL}	V_{GG}		0.95 × V_{GG}	V

OPERATING CURRENTS

Parameter	Notes	Maximum		Typical	Unit
		Industrial TA = −40°C V_{DD} = −22 Vdc V_{GG} = −50 Vdc	Commercial TA = 0°C V_{DD} = −22 Vdc V_{GG} = −50 Vdc	TA = 25°C V_{DD} = −20 Vdc V_{GG} = −50 Vdc	
10941					
I_{DD}	1	4.5	3.6	3.2	mA
I_{GG}		5.7	4.6	4.1	mA
10939 (master)					
I_{DD}	2	13.6	10.9	6.0	mA
I_{GG}		1.0	0.8	0.5	mA
10939 (slave)					
I_{DD}	2	9.1	7.3	4.0	mA
I_{GG}		1.0	0.8	0.5	mA

Notes:

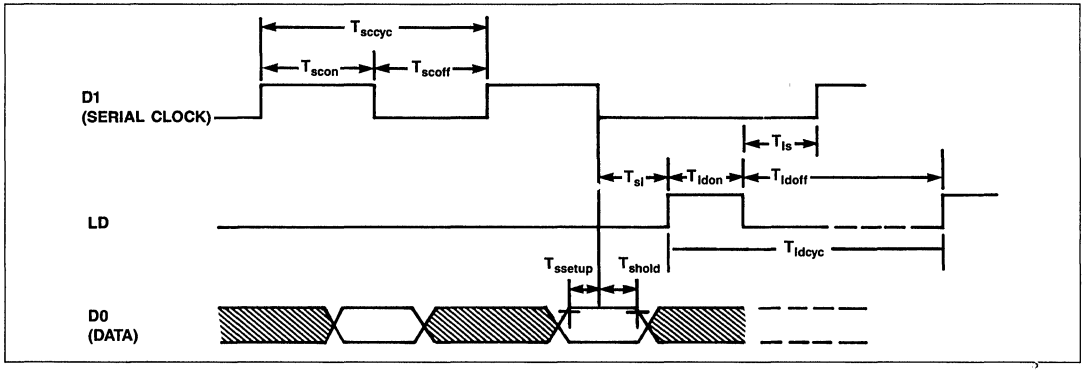
1. The 10941 has 18 internal drivers which are brought out. I_{GG} is proportional to the number of drivers on. The values given are for all 18 drivers on. Divide I_{GG} shown by 18 to determine I_{GG} for one driver.
2. The 10939 will never have more than two drivers on at any one time; one grid driver and the cursor. The values shown are for two drivers on with 100% duty cycle.

5

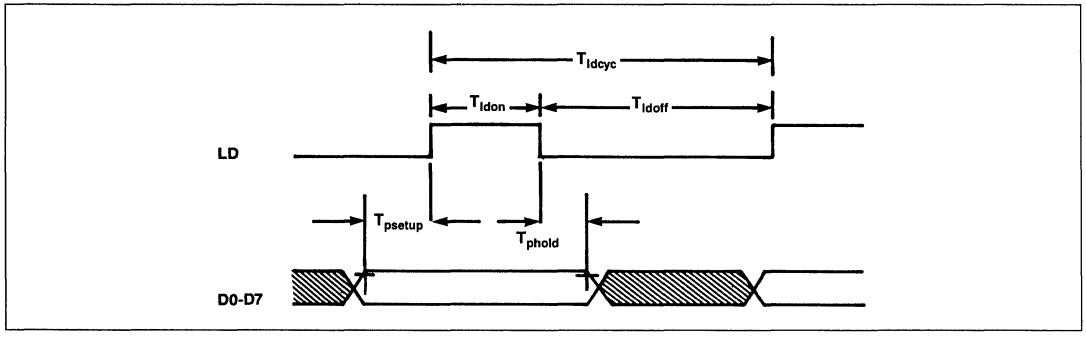
AC CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Unit
GENERAL INTERFACE TIMING					
Data Load (LD)					
On Time	T_{ldon}	1.0			µs
Off time	T_{ldoff}				
Commercial		40.0			µs
Industrial		44.5			µs
Cycle Time	T_{ldcyc}				
Commerical		60.0			µs
Industrial		66.7			µs
SERIAL INTERFACE TIMING					
Serial Clock (D1)					
On Time	T_{scon}	1.0		20.0	µs
Off Time	T_{scoff}	1.0			µs
Cycle Time	T_{sccyc}	2.0			µs
Serial Data (D0)					
Set-up Time	T_{ssetup}	400			ns
Hold Time	T_{shold}	400			ns
Serial Clock to LD Time	T_{sl}	1.0			µs
LD to Serial Clock	T_{ls}	1.0			µs
PARALLEL INTERFACE TIMING					
Parallel Data (D0–D7)					
Set-up Time	T_{psetup}	0			ns
Hold Time	T_{phold}	200			ns

TIMING WAVEFORMS



Serial Interface Timing Waveforms



Parallel Interface Timing Waveforms

FUNCTIONAL DESCRIPTION

Once the display buffer has been loaded from the host processor, the 10941/10939 system generates all timing signals required to control the display.

Input data is loaded into the Display Data Buffer as a series of 8-bit words via the Serial or Parallel Data Input channel on the 10939. Internal timing and control logic synchronize the digit output signals with the Serial Data and Load signals to the 10941 to provide the proper timing for the multiplexing operation. A 128 x 18 bit PLA is provided for decoding the character set and bargraph codes.

The parallel data input mode is implemented by toggling any of data lines D2–D7 after POR has gone low. Once the parallel data load mode has been implemented, a power-on reset procedure must be performed to return to serial data load mode. Parallel data transfer is accomplished by putting the command or display data on the data lines, then pulsing the LD line. The load cycle time must be at least 60 μs with the LD line set high for at least one μs and held low for at least 40 μs.

The serial data input mode is implemented during the power-on reset procedure. In those systems using serial mode, ports D2–D7 should be tied low to prevent the inadvertent implementation of the parallel load mode. Serial data bytes are shifted into a data buffer MSB first on line D0 using line D1 as the serial clock. The last eight bits clocked in are latched into the display controller by a pulse on the LD line. The cycle time for each data bit is 2 μs and the load time for each byte is 60 μs.

Input data may be Control or Display data. The following paragraphs describe the format and functions of these control and display data words.

CONTROL DATA WORDS

Control data words are used to select the operating parameters of the display controller. They must be preceded by a Control Prefix word (0000 0001, hexadecimal 01) to be distinguished from Display Data words. Table 1 shows the Control Word code assignments and functions.

Buffer Pointer Control

The Buffer Pointer Control code sets the Display Data Buffer pointer. The lower 5 bits of the code are loaded into the buffer pointer (see Table 2).

Table 1. Control Word Assignments

Hex Value	Function
00	Not used
01	Load 01 into Data Buffer
02	Not used
03	Not used
04	Not used
05	Set digit time to 16 cycles per grid
06	Set digit time to 32 cycles per grid
07	Set digit time to 64 cycles per grid
08	Enable Normal Display Mode (MSB in data words is cursor control only)
09	Enable Blank Mode (data words with MSB = 1 will be blanked and cursor will be on)
0A	Enable Inverse Mode (data words with MSB = 1 will be "inversed" and cursor will be on)
0B	Not used
0C	Not used
0D	Not used
0E	Start Display Refresh Cycle (use only once after reset)
0F	Not used
10–3F	Not used
40–7F	Load Duty Cycle Register with lower 6 bits (0–63)
80–9F	Load Digit Counter (80 = 32, 81 = 1, 82 = 2, etc.)
A0–BF	Not used
C0–DF	Load Buffer Pointer Register with lower 5 bits
E0–FF	Not used

Table 2. Buffer Pointer Control Codes

Code Value	Pointer Value	Character Position
C0	00	0
C1	01	1
C2	02	2
C3	03	3
C4	04	4
C5	05	5
C6	06	6
C7	07	7
C8	08	8
C9	09	9
CA	0A	10
CB	0B	11
CC	0C	12
CD	0D	13
CE	0E	14
CF	0F	15
D0	10	16
D1	11	17
D2	12	18
D3	13	19

Note:
DO NOT USE CHARACTER POSITIONS 20–31 (Codes D4–DF).

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Digit Counter Control

The Digit Counter Control code defines the number of character positions (grids) to be controlled. This code is normally used only during initialization routines, but it may also be used in conjunction with the Load Duty Cycle control code to extend the range of brightness control (see Table 3).

Duty Cycle Control

The Duty Cycle Control code turns the display on and off, adjusts display brightness, or modifies display timing. The time slot for each character is 16, 32, or 64 cycles as selected by the Digit Time Control codes (see Table 1). The segment and digit drivers for each character are on for a maximum of 13, 29, or 61 cycles with a 3 cycle inter-digit off-time. The lower 6 bits of the Duty Cycle Control code are loaded into the Duty Cycle Register. Resultant duty cycles are shown in Table 4.

Digit Time Select

The Digit Time Select code sets the total time for each character during the refresh cycle. Three values can be set using the three codes shown in Table 1. The default value set at power-on is 64 cycles per grid. For displays with 40 or more characters, or under conditions where the display can be subjected to quick movements during viewing (e.g. portable or vehicle-mounted applications), it may be necessary to increase the refresh rate by selecting 16 or 32 cycles per grid with the appropriate control code.

Table 3. Digit Counter Control Codes

Code	Digit Counter Value	No. of Grids Controlled
80	00	32
81	01	1
82	02	2
83	03	3
84	04	4
85	05	5
86	06	6
87	07	7
88	08	8
89	09	9
8A	0A	10
8B	0B	11
8C	0C	12
8D	0D	13
8E	0E	14
8F	0F	15
90	10	16
91	11	17
92	12	18
93	13	19
94	14	20
95	15	21
96	16	22
97	17	23
98	18	24
99	19	25
9A	1A	26
9B	1B	27
9C	1C	28
9D	1D	29
9E	1E	30
9F	1F	31

Display Mode Select

Each ASCII character is represented by the lower seven bits of the 8-bit value loaded into the 10939. The eighth (most significant) bit controls the cursor (see Cursor Control). This bit is known as the data byte control bit. If either Blank or Inverse mode is selected, a "0" in this bit causes a normal character display, while a "1" selects either Blank or Inverse mode, depending on which mode is enabled. Three control codes are provided (see Table 1) to enable Blank Mode, Inverse Mode, or Normal Display mode.

Table 4. Duty Cycle Control Codes

	Digit Time = 16		Digit Time = 32		Digit Time = 64	
Code	On	Off	On	Off	On	Off
40	—	16	—	32	—	64
41	—	16	—	32	—	64
42	—	16	—	32	—	64
43	1	15	1	31	1	63
44	2	14	2	30	2	62
45	3	13	3	29	3	61
46	4	12	4	28	4	60
47	5	11	5	27	5	59
48	6	10	6	26	6	58
49	7	9	7	25	7	57
4A	8	8	8	24	8	56
4B	9	7	9	23	9	55
4C	10	6	10	22	10	54
4D	11	5	11	21	11	53
4E	12	4	12	20	12	52
4F	13	3	13	19	13	51
50	13	3	14	18	14	50
51	13	3	15	17	15	49
52	13	3	16	16	16	48
53	13	3	17	15	17	47
.	.	.	.	.	.	.
.	.	.	.	.	.	.
.	.	.	.	.	.	.
5B	13	3	25	7	25	39
5C	13	3	26	6	26	38
5D	13	3	27	5	27	37
5E	13	3	28	4	28	36
5F	13	3	29	3	29	35
60	13	3	29	3	30	34
61	13	3	29	3	31	33
62	13	3	29	3	32	32
.	.	.	.	.	.	.
.	.	.	.	.	.	.
.	.	.	.	.	.	.
7C	13	3	29	3	58	6
7D	13	3	29	3	59	5
7E	13	3	29	3	60	4
7F	13	3	29	3	61	3

In the Blank mode, any character with the MSB = "1" will be blanked. In the Inverse mode, it will be displayed with all segment driver outputs inverted. On video displays, this is referred to as "Inverse Video" format. These controls allow individual characters or groups of characters to be blinked or blanked by simply changing the mode without changing the data in the Display Buffer.

Cursor Control

The data byte control bit (MSB 8), besides selecting Blank, Inverse, or Normal mode, also controls the cursor output which is enabled on all characters with the MSB equal to one. Therefore, when the Normal mode is enabled and the MSB of the data byte is set to a one, the normal character is displayed with the cursor on. When the Blank mode is enabled and the MSB is set to a one, the character is blanked but the cursor is on. If Inverse mode is enabled and the MSB is set to a one, the inverse character is displayed and the cursor is on but not inversed.

Start Refresh

At power on, the 10939 is held in an internal halt mode. The normal display refresh sequence starts upon receipt of a Start Refresh control code. This is particularly useful for synchronizing systems using more than one 10939. Only the Master 10939 in a multi-chip system will recognize the Start Refresh code. The Master starts the Slave(s) at the appropriate time, using the SOP signal.

INPUT DISPLAY DATA WORDS

Display data words are loaded as 8-bit codes. The eighth (most significant) bit specifies normal (0) or blank/inverse (1) display mode, depending on the blank/inverse mode selection (see Control data words 09 and 0A in Table 1). This bit also controls the cursor.

Twenty display data words must be entered to completely load the Display Data Buffer. The Buffer Pointer automatically increments after each data word is stored in the buffer. To select a character position to be loaded out of sequence, use the Buffer Pointer control code. The Buffer Pointer will automatically reset to character position 0 when its value is equal to the programmed Digit Count.

POWER-ON RESET

The Power-On Reset (POR) initializes the internal circuits of the 10939. This is normally accomplished when power (V_{DD}) is applied. The following conditions are established by application of POR:

a. The Grid Drivers (STR00–STR19) on the 10939 are in the off state.
b. The Segment Drivers (SG01–SG16) on the 10941 are in the off state.
c. The Duty Cycle is set to 0.
d. The Digit Counter is set to 32.
e. The Buffer Pointer is set to 0.
f. The Digit time is set to 64.
g. The Normal display mode is set.
h. DATA-LOAD is set to high impedance state.
i. SCLK-DIS is set to V_{OL} to disable the anode drivers in the 10941.
j. SOP is set to V_{OL} to disable the sync pulse.

Note:
1. When the POR signal is removed, SCLK-DIS is set to the high impedance state.
2. During the initial rise time of V_{DD} at power turn-on, the magnitude of V_{GG} should not exceed the magnitude of V_{DD}.

DIGIT (GRID) DRIVERS (STR00–STR19) PLUS CURSOR

The 20 Digit (Grid) Drivers select each of the display character positions sequentially during a refresh scan. Display segments are illuminated when both the Digit Drivers and Segment Drivers for a particular character are energized simultaneously. The Cursor segment is generated by the 10939, but its timing characteristics are identical to the 16 segments generated by the 10941.

SEGMENT (ANODE) DRIVERS (SG01–SG16, PNT, TAIL)

Eighteen Segment (Anode) Drivers are provided in the 10941. The output states for each character pattern and each bargraph pattern are internally decoded from the 8-bit characters received from the 10939 by means of a 128 x 18-bit PLA. Data codes and the corresponding segment patterns are shown in Figure 1. Data codes and the corresponding bargraph patterns are shown in Figure 2.

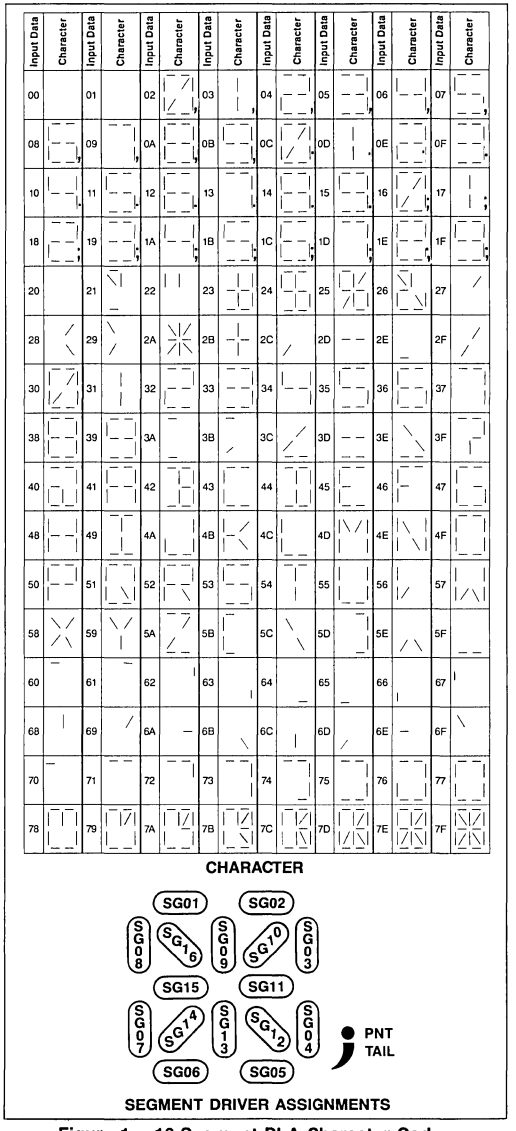

Figure 1. 16-Segment PLA Character Codes

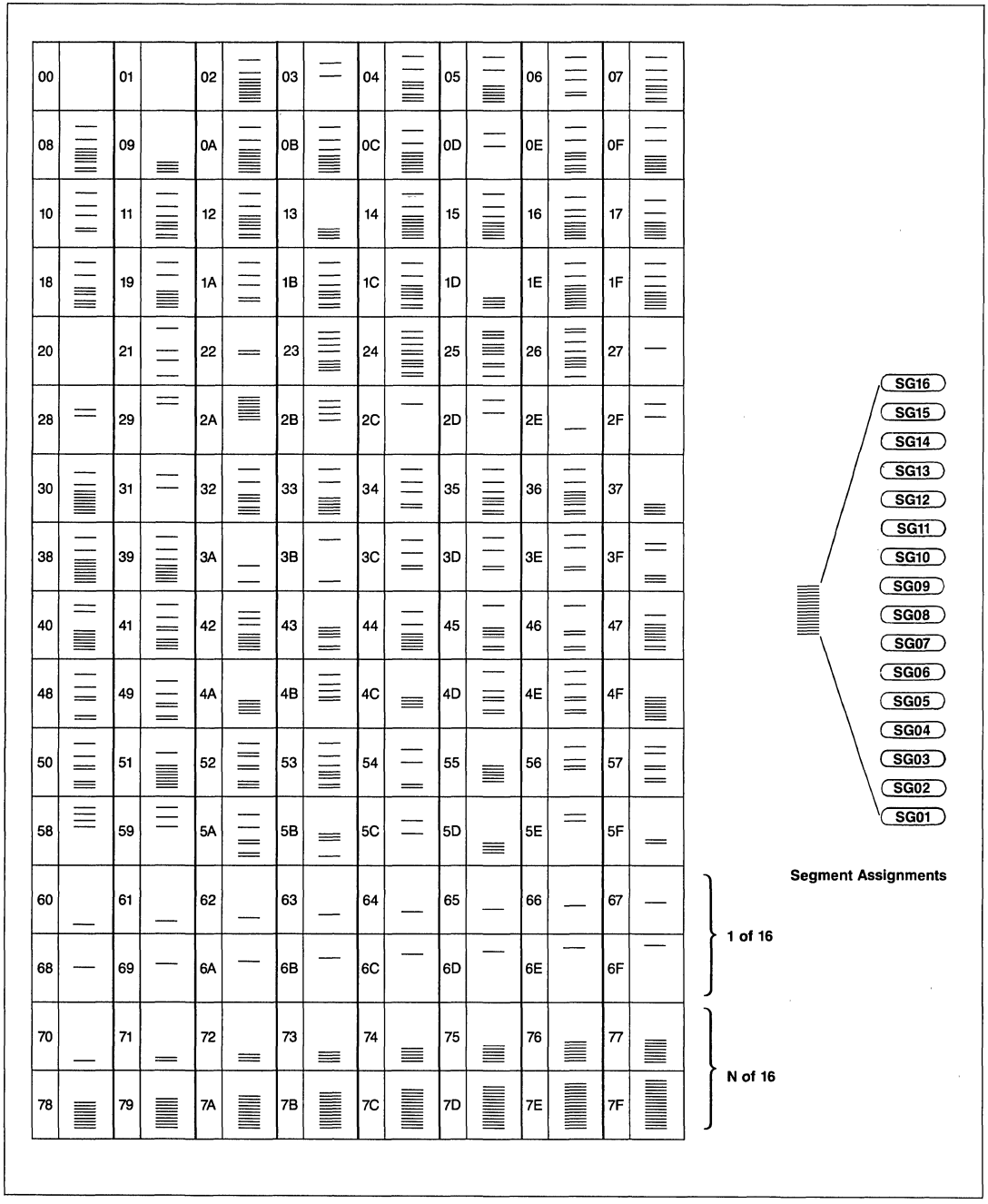

Figure 2. 16-Segment BarGraph Codes

TYPICAL SYSTEM HOOKUPS

Figure 3 shows a 10941 and 10939 in a parallel interface with the host system driving a 20 character display. Figure 4 shows a 10941 and a 10939 in a serial interface with the host system driving a 20 character display. Figure 5 shows a 10941 and two 10939's in a parallel interface with the host system driving a 40 character display.

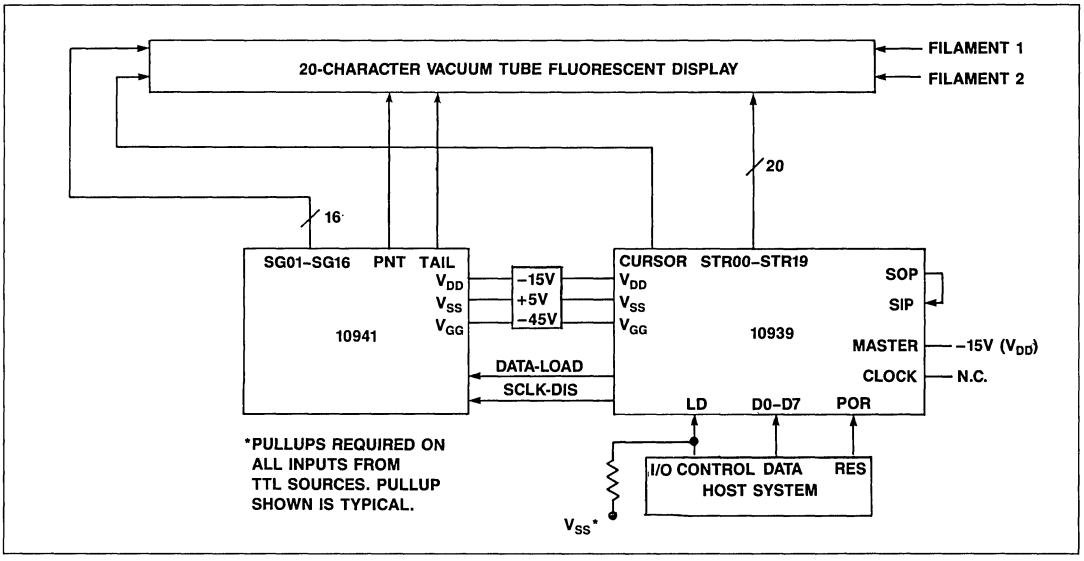

Figure 3. Typical Display System with Parallel Interface to Host System

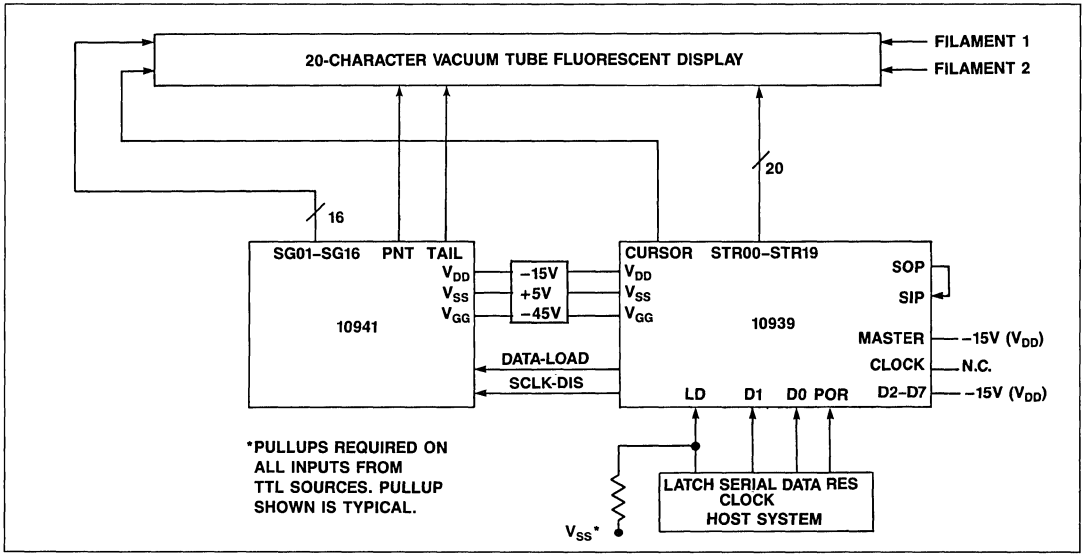

Figure 4. Typical Display System with Serial Interface to Host System

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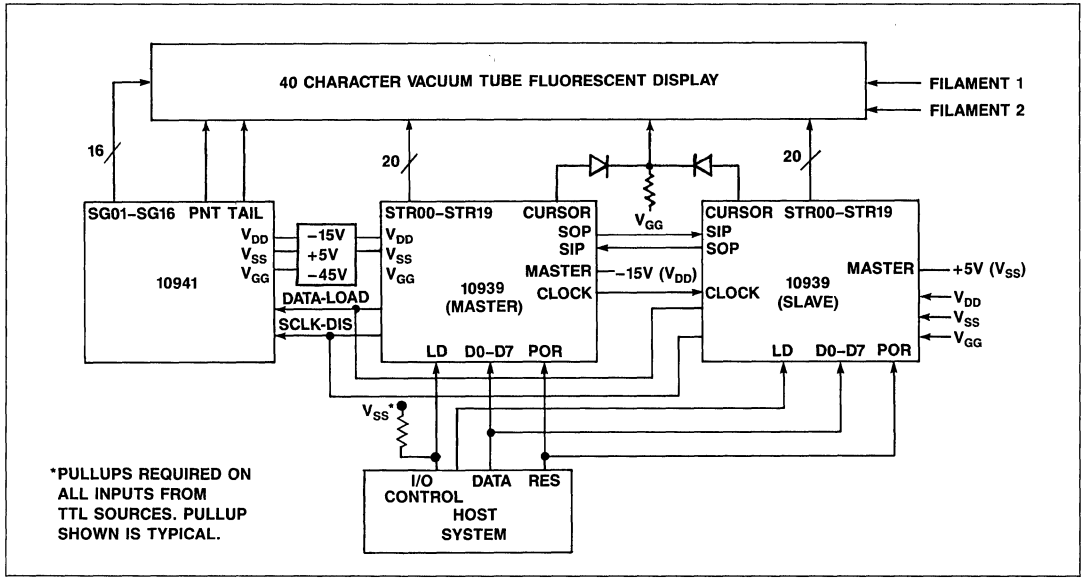

Figure 5. Typical Display System with Parallel Interface to Host and Two 10939 Devices

Rockwell

10951
Bargraph and Numeric Display Controller

DESCRIPTION

The Rockwell 10951 Bargraph and Numeric Display Controller is an LSI general purpose display controller designed to interface to bargraph and numeric displays (vacuum fluorescent or LED).

The 10951 will drive 16-segment bargraph or seven-segment plus comma and decimal numeric displays with up to 16 display positions. The controller accepts command and data input words on a clocked serial input line. Commands control the on/off duty cycle, starting character position and number of characters to display. Encoded data words display bargraph position (single segment or increasing bar length), numbers, comma, decimal and selected upper and lower case letters. No external drive circuitry is required for displays that operate on 20 mA of drive current up to 50 volts. A 64 x 16-bit segment decoder provides character set decoding for the display.

ORDERING INFORMATION

Part Number	Package Type	Drive Voltage	Temperature Range (°C)
10951P-40	Plastic	40V	0 to +70
10951P-50	Plastic	50V	0 to +70
10951PE-40	Plastic	40V	−40 to +85
10951PE-50	Plastic	50V	−40 to +85

FEATURES

- 16 segment drivers plus decimal point and comma tail drivers
- 16 digit drivers
- Up to 66 kHz data rate
- Direct digit drive of 20 mA for up to 50 volt displays
- Supports vacuum fluorescent or LED displays
- Serial data input for 8-bit display and control data words
- 64 x 16-bit PLA provides data decoding driving
  - — Any 1 of 16 bargraph segments
  - — 1 to 16 bargraph segments
  - — Ten seven-segment numeric characters (0–9)
  - — Comma and decimal
  - — Eight upper and lower case seven-segment characters
- Command functions
  - — Duty cycle adjust
  - — Character position select
  - — Number of characters
- 40-Pin DIP package

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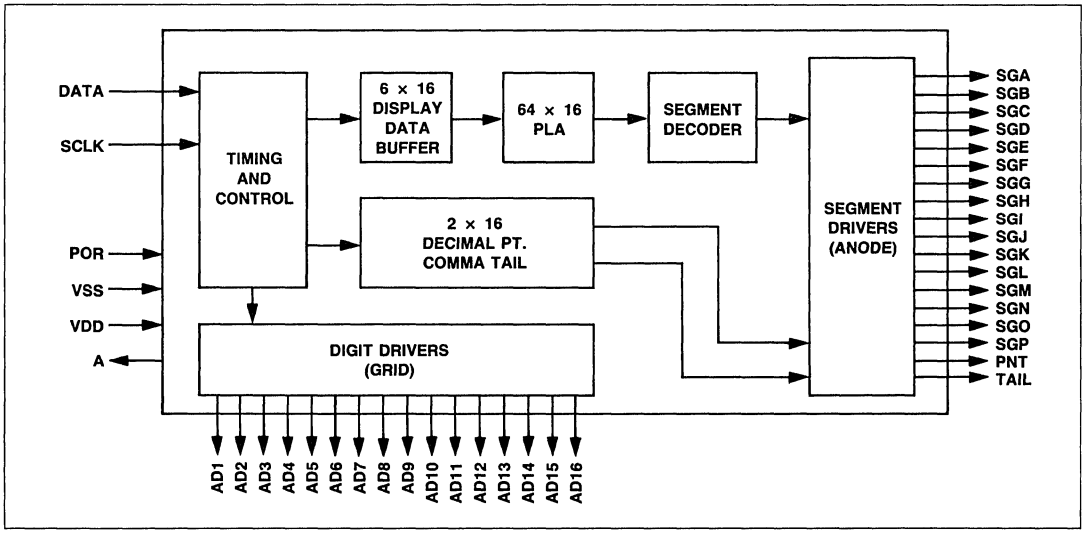
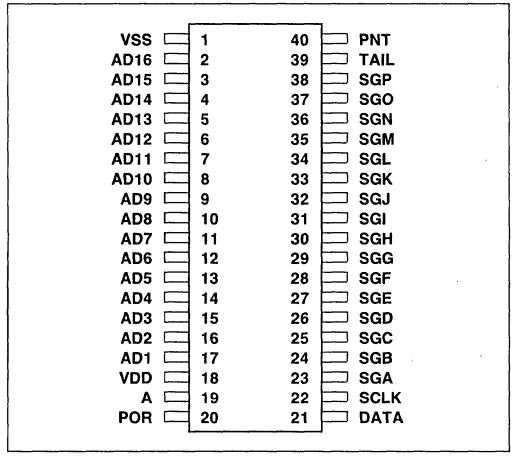


10951 Block Diagram

INTERFACE DESCRIPTION

10951 Pin Functions

Signal Name	Pin No.	Function
V_{SS}	1	Power and signal reference
AD16–AD1	2–17	Digits 16 through 1 driver outputs
V_{DD}	18	DC power connection
A	19	A clock output used for testing
POR	20	Power-on reset input
DATA	21	Serial data input
SCLK	22	Serial data clock input
SGA–SGP	23–38	Segments A through P driver outputs
TAIL	39	Comma tail driver output
PNT	40	Decimal point driver output



10951 Pin Configuration

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS*

All voltages are specified relative to V_{SS}.

Parameter	Symbol	Value	Unit
Supply Voltage	V_{DD}	+0.3 to −20	V
Operating Current	I_{DD}	7	mA
Input Voltage	V_{IN}	+0.3 to −20	V
Output Voltage	V_{OUT}	+0.3 to −50	V
Output Current Digits	I_D	20	mA
Output Current Segments	I_S	10	mA
Operating Temperature			
Commercial	T_C	0 to +70	°C
Industrial	T_I	−40 to +85	°C
Storage Temperature	T_{STG}	−55 to +125	°C
Input Capacitance	C_{IN}	5	pF
Output Capacitance	C_{OUT}	10	pF

***NOTE:** Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the other sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

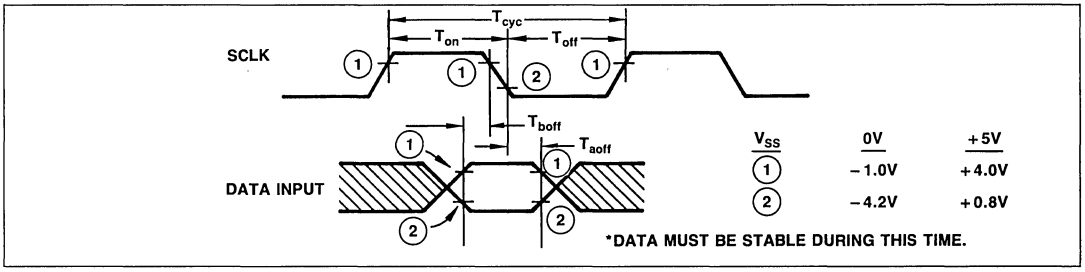
DC CHARACTERISTICS

Parameter	Limits (V_{SS} = 0) Min	Typ	Max	Limits (V_{SS} = +5V) Min	Typ	Max	Conditions	Unit
Supply Voltage (V_{DD})	−16.5	−15.0	−13.5	−11.5	−10.0	−8.5		V
Power Dissipation		40	100		40	100		mW
Input DATA,SCLK,								
Logic "1"	−1.0		+0.3	+4.0		+5.3		V
Logic "0"	V_{DD}		−4.2	V_{DD}		+0.8		
Input POR								
Logic "1"	−3.0		+0.3	+2.0		+5.3		
Logic "0"	V_{DD}		−10.0	V_{DD}		−5.0		
Output Digit and Segment Strobes Driver On								
Commercial			−1.5			+3.5	At 10 mA	V
Industrial			−1.7			+3.3		V
Driver Off 10951-40	−40		−35	−35		−30	Actual value determined by external circuit	V
Driver Off 10951-50	−50		−45	−45		−40		V
Output Leakage			10			10	Per driver at driver off	μA
Input Leakage			10			10		μA

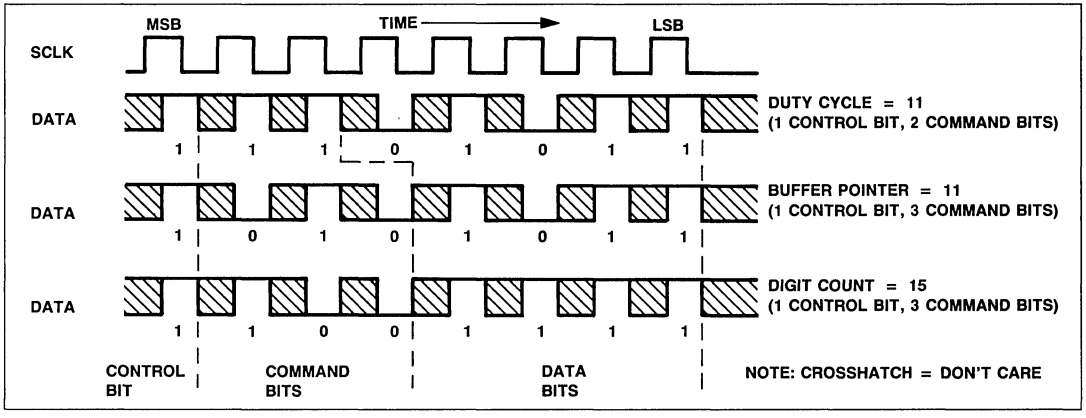
Note: All outputs require Pulldown Resistors.

AC CHARACTERISTICS

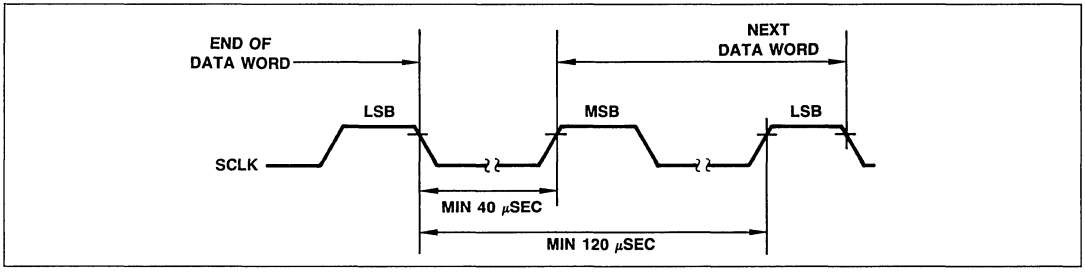
Parameter	Symbol	Min	Typ	Max	Unit
SCLK Clock					
On Time	T_{on}	1.0		20.0	μs
On Time	T_{off}	1.0			μs
Data Input Sample Time					
Before SCLK Clock Off	T_{boff}	200			ns
After SCLK Clock Off	T_{aoff}	100			ns



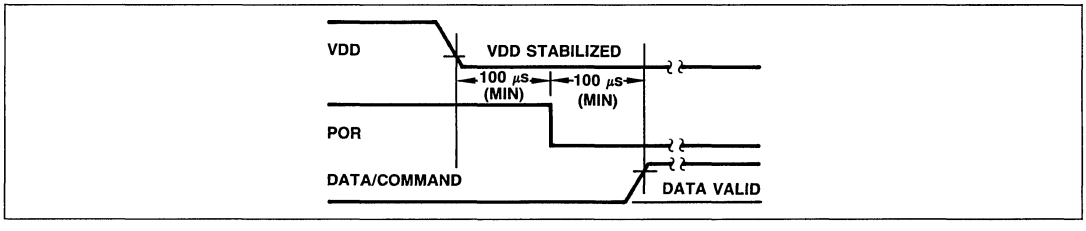
SCLK and Serial Data Timing



SCLK and Serial Data (Control Word) Examples



Data Word LSB/MSB Timing



Power-On Reset

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FUNCTIONAL DESCRIPTION

The 10951 receives commands and data on a serial input line clocked externally by a separate clock input line. The controller decodes the commands from control data words, decodes the data words in accordance with an internal 64 x 16-bit programmable logic array (PLA) and turns on and off segment and digit output drivers. The segment output patterns are controlled by the decoded data words while the digit output and segment output timing are controlled by the decoded control words. All timing signals required to control the display are generated in the 10951 device without any refresh input from the host processor.

Input data is loaded into the Display Data Buffer via the Serial Data Input (Data) channel. Internal timing and control blocks synchronize the segment and digit output signals to provide the proper timing for the multiplexing operation. The 16 x 64 PLA decodes 8-bit data words to drive the 16 segment, comma and decimal point drivers. The decoded data words will drive 16 segments to display bargaph patterns (single segment and multiple segment for increasing length displays) or seven-segment patterns to display numbers, selected upper and lower case letters, comma and decimal point.

Input data is loaded into the 10951 as a series of 8-bit words with the most significant bit (MSB), bit 7, first. If the MSB is a logic 1 (this bit is referred to as the control bit C), the loaded word is a control data word. If the C bit of any word is a logic 0, the loaded word is a display data word. The following paragraphs describe the format and functions of these control and display data words.

INPUT CONTROL DATA WORDS

When the C-Bit (bit 7) of the 8-bit input word is a logic 1, bits 5 and 6 are decoded into one of four control commands while data associated with the command are extracted from bits 0–4. There are four control codes which perform the following display functions:

- Load the Display Data Buffer pointer,
- Load the Digit Counter,
- Load the Duty Cycle register,
- Enable the Test Mode.

Table 1 lists the control codes and their functions.

Buffer Pointer Control

The Buffer Pointer Control code allows the Display Data Buffer pointer to be set to any digit position so that individual characters may be modified. The Buffer Pointer is loaded with a decimal equivalent value 2 less than the desired value (i.e., to point to the digit controlled by AD6 of the display, a value of 4 is entered). See Table 2 for a complete list of the Buffer Pointer values.

Digit Counter Control

The Digit Counter Control code is normally used only during initialization routines to define the number of character positions to be controlled. This code maximizes the duty cycle for any display. If 16 characters are to be controlled, enter a value of 0 (zero). Otherwise, enter the value desired.

Duty Cycle Control

The Duty Cycle Control code is used to turn the display on and off, and to adjust display brightness. As shown in the block diagram, the time slot for each character is 32 clock cycles. The segment and digit drivers for each character are on for a maximum of 31 cycles with a 1 cycle inter-digit off-time. The Duty Cycle Control code contains a 5-bit numeric field which modifies the on-time for the driver outputs from 0 to 31 cycles. A duty cycle of 0 puts both the segment and digit drivers into the off state. Figure 1 shows the timing characteristics for the segment outputs.

Test Mode Enable

The Test Mode Enable code is a device test function only. If executed, it will lock the device in the Test Mode. This mode can be disabled only by performing a power-on reset.

If this mode is activated, the digit time is reduced from 32 to 4 clock cycles to speed up the output driver sequencing time for ease in testing.

Table 1. Control Data Words

8-Bit Control Word		Function
C-Bit	7-Bit Code	
1	010NNNN[1]	Buffer Pointer Control (Position of character to be changed)
1	100NNNN[1]	Digit Counter Control (Number of characters to be output)
1	11NNNNN[2]	Duty Cycle Control (On/off and brightness control)
1	00NNNNN[3]	Test Mode Enable (Not a user function)

Note:
1. NNNN is a 4-bit binary value representing the digit number to be loaded.
2. NNNNN is a 5-bit binary value representing the number of clock cycles each digit is on.
3. This code is a device test function only. If executed it will lock the device in the Test Mode. Test Mode can be disabled only by performing a power-on reset.

Table 2. Buffer Pointer Control Codes

Hex Code	Pointer Value	Character Controlled By
A0	0	AD2
A1	1	AD3
A2	2	AD4
A3	3	AD5
A4	4	AD6
A5	5	AD7
A6	6	AD8
A7	7	AD9
A8	8	AD10
A9	9	AD11
AA	10	AD12
AB	11	AD13
AC	12	AD14
AD	13	AD15
AE	14	AD16
AF	15	AD1

INPUT DISPLAY DATA WORDS

Display data words are loaded as 8-bit format codes. There are 64 codes available (with the C-bit set to 0 to indicate a display data word).

Sixteen display data words must be entered to completely load the Display Data Buffer. The Buffer Pointer is automatically incremented before each data word is stored in the Display Buffer except for decimal point and comma words. The decimal point and comma words do not cause the Buffer Pointer to increment and thus are always associated with the previous character entered. To enter a character position out of the normal sequence, use the Buffer Pointer control command before entering the display data word. It is not necessary to use the Buffer Pointer control command to cycle back to position 1 when less than 16 character positions are being used (Digit Counter $\neq$ 0).

DIGIT DRIVERS (AD1–AD16)

The sixteen Digit Drivers (AD1 – AD16) are used to select each of the display digits sequentially during a refresh scan. Display segments will be illuminated when both the Digit Drivers and Segment Drivers for a particular character are energized simultaneously. The timing characteristics of both the digits and segments are shown in Figure 1. See POR for the Power-On Reset state of these drivers.

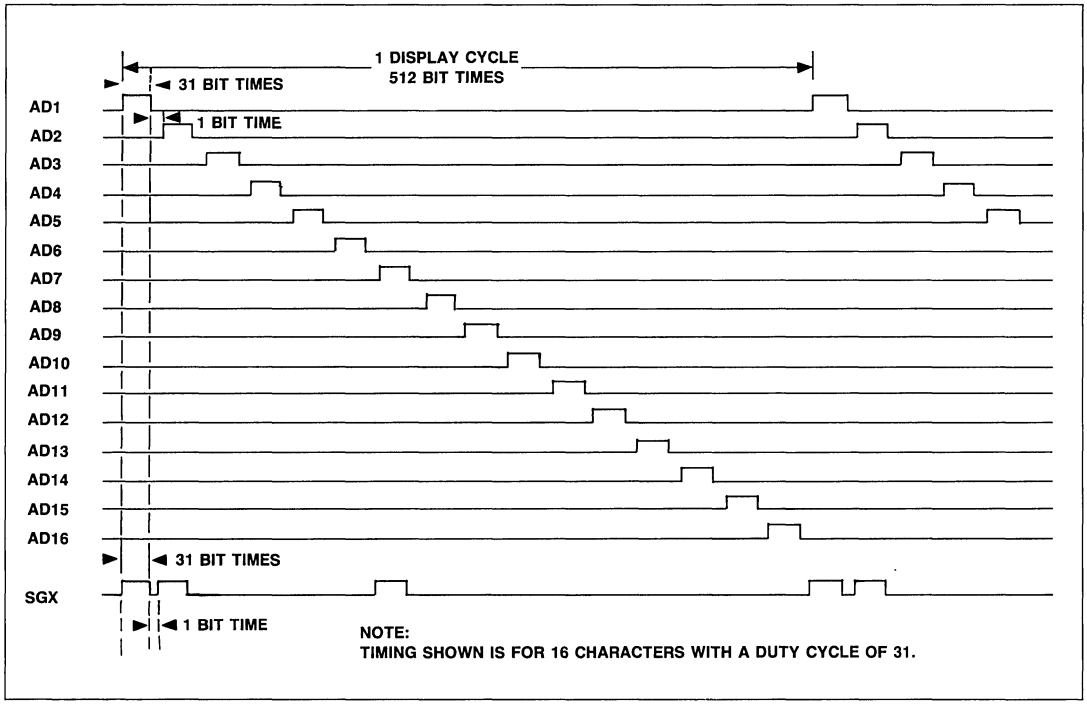


Figure 1. Display Scan Timing Diagram (Duty Cycle)

POWER-ON RESET (POR)

The Power-On Reset (POR) initializes the internal circuits of the 10951 when power (V_{DD}) is applied. The following conditions are established after a Power-On Reset:

a. The Digit Drivers (AD1-AD16) are in the off state (floating).
b. The Segment Drivers (SGA-SGP) are in the off state (floating). This includes PNT and TAIL.
c. The Duty Cycle is set to 0.
d. The Digit Counter is set to 16 (a bit code value of 0).
e. The Buffer Pointer points to the character controlled by AD1.

SEGMENT DRIVERS (SGA–SGP)

Sixteen (16) Segment Drivers are provided (SGA-SGP), plus the decimal point (PNT) and comma tail (TAIL). The segment, PNT and TAIL outputs are internally decoded from the 8-bit characters in the Display Data Buffer by means of a 64 x 16-bit PLA. The driver allocations for the 16-segment bargraph display and the seven-segment alphanumeric character plus comma and decimal point are shown in Figure 2. The input codes associated with seven-segment alphanumeric, comma and decimal point display are also shown in Figure 2. The complete set of 8-bit codes for the bargraph and alphanumeric display is shown in Table 3. Note that only segment drivers SGA-SGG are used to drive the seven-segment characters. Segment drivers SGH-SGP may be used for other purposes as decoded in accordance with Table 3. Figure 3 shows the total allocation of the 16-segment drivers as they would appear on a 7-segment display or a 16-segment bargraph display. Timing characteristics for the segment outputs are shown in Figure 1. See POR for the Power-On Reset state of these drivers.

TYPICAL SYSTEM HOOK-UP

Figure 4 shows the 10951 as it would be connected to a V-F display when driven by a host system. E_K is determined by the V-F display specifications and R_C is selected to provide proper biasing current for zeners. Pull down resistors R_A and R_G are determined by the interconnection capacitance between the 10951 and the display.

Table 3. 10951 Data Codes

Input Code								Function	Segment Driver Output Patterns (1 = On)																
7	6	5	4	3	2	1	0		SGA	SGB	SGC	SGD	SGE	SGF	SGG	SGH	SGI	SGJ	SGK	SGL	SGM	SGN	SGO	SGP	PNT	TAIL
0	X	0	0	0	0	0	0	Segment A On	1																	
0	X	0	0	0	0	0	1	Segment B On		1																
0	X	0	0	0	0	1	0	Segment C On			1															
0	X	0	0	0	0	1	1	Segment D On				1														
0	X	0	0	0	1	0	0	Segment E On					1													
0	X	0	0	0	1	0	1	Segment F On						1												
0	X	0	0	0	1	1	0	Segment G On							1											
0	X	0	0	0	1	1	1	Segment H On								1										
0	X	0	0	1	0	0	0	Segment I On									1									
0	X	0	0	1	0	0	1	Segment J On										1								
0	X	0	0	1	0	1	0	Segment K On											1							
0	X	0	0	1	0	1	1	Segment L On												1						
0	X	0	0	1	1	0	0	Segment M On													1					
0	X	0	0	1	1	0	1	Segment N On														1				
0	X	0	0	1	1	1	0	Segment O On															1			
0	X	0	0	1	1	1	1	Segment P On																1		
0	X	0	1	0	0	0	0	Segment A On	1																	
0	X	0	1	0	0	0	1	Segments A&B On	1	1																
0	X	0	1	0	0	1	0	Segment A-C On	1	1	1															
0	X	0	1	0	0	1	1	Segment A-D On	1	1	1	1														
0	X	0	1	0	1	0	0	Segment A-E On	1	1	1	1	1													
0	X	0	1	0	1	0	1	Segment A-F On	1	1	1	1	1	1												
0	X	0	1	0	1	1	0	Segment A-G On	1	1	1	1	1	1	1											
0	X	0	1	0	1	1	1	Segment A-H On	1	1	1	1	1	1	1	1										
0	X	0	1	1	0	0	0	Segment A-I On	1	1	1	1	1	1	1	1	1									
0	X	0	1	1	0	0	1	Segment A-J On	1	1	1	1	1	1	1	1	1	1								
0	X	0	1	1	0	1	0	Segment A-K On	1	1	1	1	1	1	1	1	1	1	1							
0	X	0	1	1	0	1	1	Segment A-L On	1	1	1	1	1	1	1	1	1	1	1	1						
0	X	0	1	1	1	0	0	Segment A-M On	1	1	1	1	1	1	1	1	1	1	1	1	1					
0	X	0	1	1	1	0	1	Segment A-N On	1	1	1	1	1	1	1	1	1	1	1	1	1	1				
0	X	0	1	1	1	1	0	Segment A-O On	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1			
0	X	0	1	1	1	1	1	Segment A-P On	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1		
0	X	1	0	0	0	0	0	Number 0	1	1	1	1	1	1		1	1	1	1	1						
0	X	1	0	0	0	0	1	Number 1		1	1					1	1	1	1	1						
0	X	1	0	0	0	1	0	Number 2	1	1		1	1		1	1	1	1	1	1						
0	X	1	0	0	0	1	1	Number 3	1	1	1	1			1	1	1	1	1	1						
0	X	1	0	0	1	0	0	Number 4		1	1			1	1	1	1	1	1	1						
0	X	1	0	0	1	0	1	Number 5	1		1	1		1	1	1	1	1	1	1						
0	X	1	0	0	1	1	0	Number 6	1		1	1	1	1	1	1	1	1	1	1						
0	X	1	0	0	1	1	1	Number 7	1	1	1			1	1	1	1	1	1	1						
0	X	1	0	1	0	0	0	Number 8	1	1	1	1	1	1	1	1	1	1	1	1						
0	X	1	0	1	0	0	1	Number 9	1	1	1	1		1	1	1	1	1	1	1						
0	X	1	0	1	0	1	0	Letter P	1	1			1	1	1						1	1	1	1		
0	X	1	0	1	0	1	1	Letter L				1	1	1							1	1	1	1		
0	X	1	0	1	1	0	0	Semicolon								1	1	1	1	1					1*	1*
0	X	1	0	1	1	0	1	Blank								1	1	1	1	1						
0	X	1	0	1	1	1	0	Decimal													1	1	1	1	1**	
0	X	1	0	1	1	1	1	Blank													1	1	1	1		
0	X	1	1	0	0	0	0	Number 0	1	1	1	1	1	1							1	1	1	1		
0	X	1	1	0	0	0	1	Number 1		1	1										1	1	1	1		
0	X	1	1	0	0	1	0	Number 2	1	1		1	1		1						1	1	1	1		
0	X	1	1	0	0	1	1	Number 3	1	1	1	1			1						1	1	1	1		
0	X	1	1	0	1	0	0	Number 4		1	1			1	1						1	1	1	1		
0	X	1	1	0	1	0	1	Number 5	1		1	1		1	1						1	1	1	1		
0	X	1	1	0	1	1	0	Number 6	1		1	1	1	1	1						1	1	1	1		
0	X	1	1	0	1	1	1	Number 7	1	1	1			1							1	1	1	1		
0	X	1	1	1	0	0	0	Number 8	1	1	1	1	1	1	1						1	1	1	1		
0	X	1	1	1	0	0	1	Number 9	1	1	1	1		1	1						1	1	1	1		
0	X	1	1	1	0	1	0	Letter A	1	1	1		1	1	1						1	1	1	1		
0	X	1	1	1	0	1	1	Letter b			1	1	1	1	1						1	1	1	1		
0	X	1	1	1	1	0	0	Letter C	1			1	1	1							1	1	1	1		
0	X	1	1	1	1	0	1	Letter d		1	1	1	1		1						1	1	1	1		
0	X	1	1	1	1	1	0	Letter E	1			1	1	1	1						1	1	1	1		
0	X	1	1	1	1	1	1	Letter F	1				1	1	1						1	1	1	1		

Any 1 of 16 Segments

Bargraph Codes

1 to 16 Segments

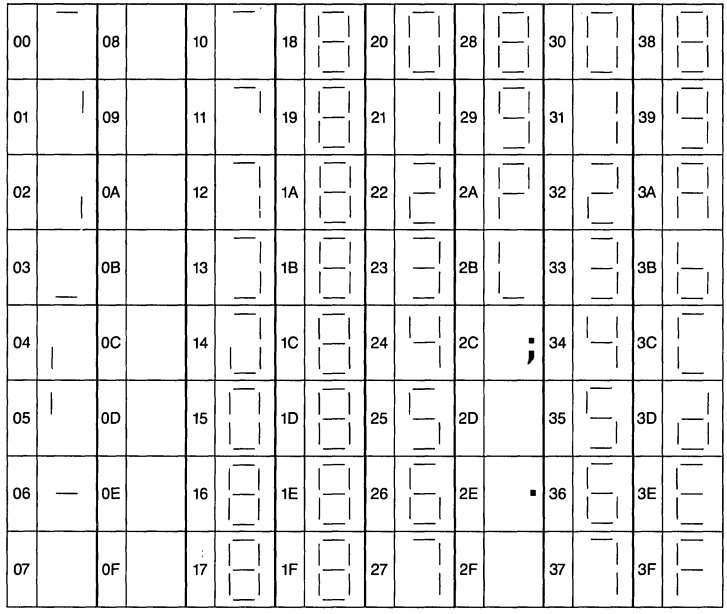
Alphanumeric and Special Codes

Notes:

* Sets comma and decimal outputs for last character entered.

** Sets decimal output for last character entered.

5



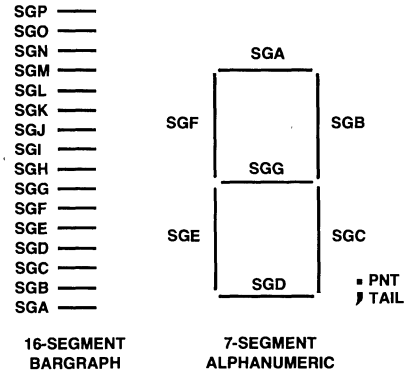


Figure 2. Segment Allocation and 7-Segment Alphanumeric Codes

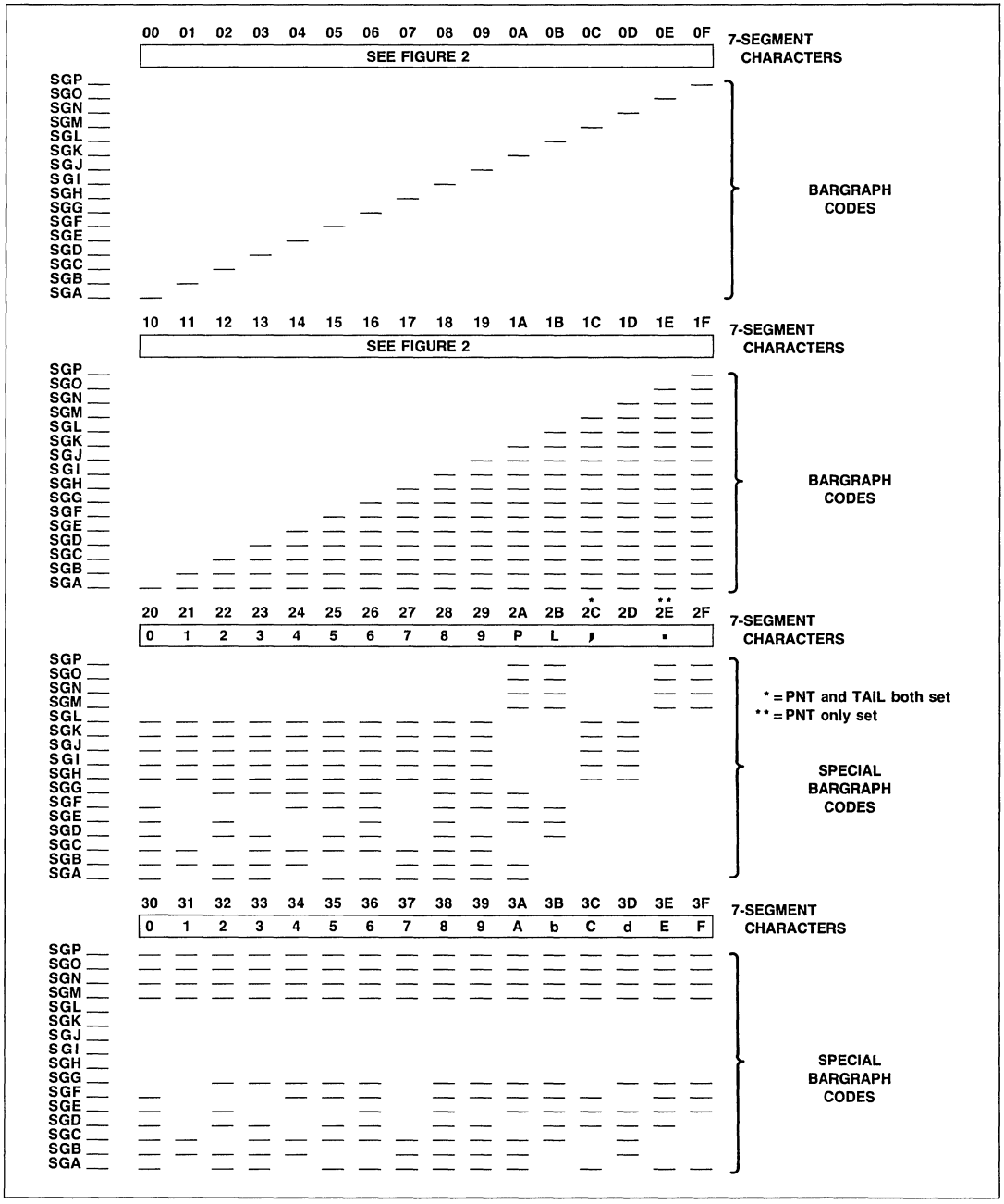


Figure 3. Total Character Allocation for Bargraph or 7-Segment Displays

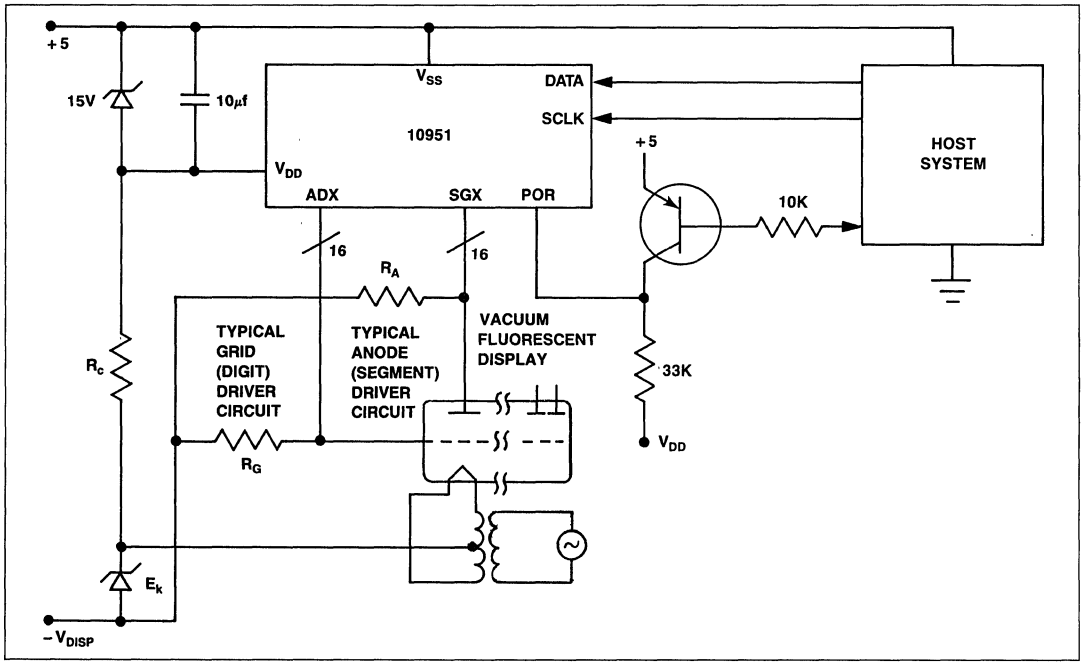


Figure 4. Partial System Schematic

Rockwell

10955
Segmented Display Controller/Driver

DESCRIPTION

The 10955 Segmented Display/Driver is a MOS/LSI device capable of directly driving both the grids and anodes of multiplexed vacuum-fluorescent segmented displays. All timing circuits (including a clock generator) required to control the display drivers are contained within the device. The 10955 can drive segmented displays with 8 or 16 grids (characters) and 8, 16, or 24 anodes (segments). A serial interface allows for a host microprocessor to transmit commands and display data to the 10955 directly.

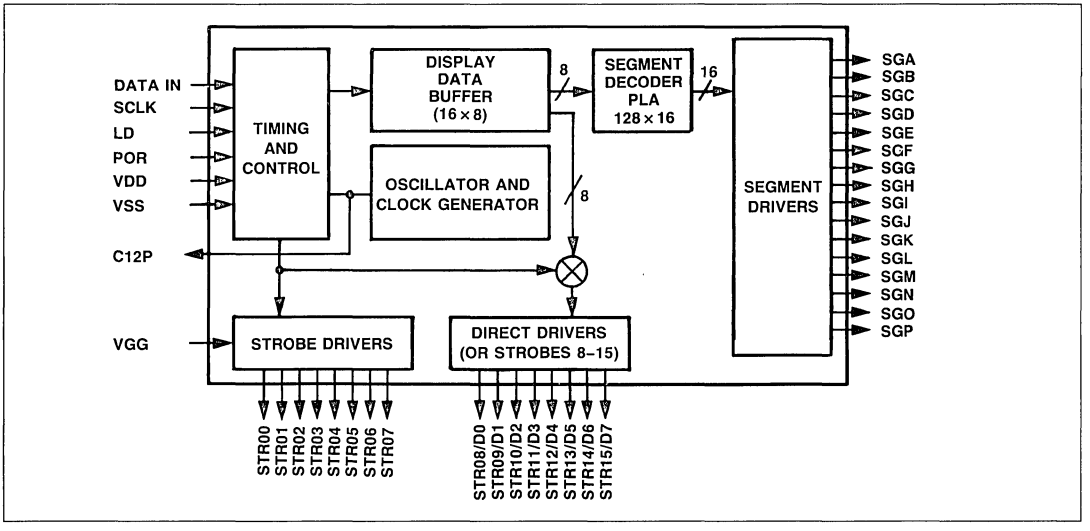
A 128 x 16 bit PLA provides coding for both 16-segment and 14-segment alphanumeric ASCII code character sets (all caps only). The PLA is divided into lower 64 and upper 64 code sets. Only one set can be selected at a time. In lower set mode the 16-segment display characters are selected. In upper set mode the 14-segment display characters are selected. The PLA can also be bypassed so that data words from the host microprocessor are loaded directly into segment drivers without decoding by the PLA. This mode is especially useful for creating special display patterns such as bar graph displays. Bypass mode is limited to eight drivers per data word.

FEATURES

- 8- or 16-character display driver
- 8-, 16-, or 24-segment drivers
- Average data rate 66 kHz
- Single character burst rate 500 kHz
- Direct digit drive of 20 ma for up to 40 or 50 volt vacuum-fluorescent serial displays
- 128 x 16-bit PLA provides 16- or 14-segment alpha-numeric character set
- Internal clock generator circuit
- Serial host interface
- PLA bypass mode
- 40-pin DIP

ORDERING INFORMATION

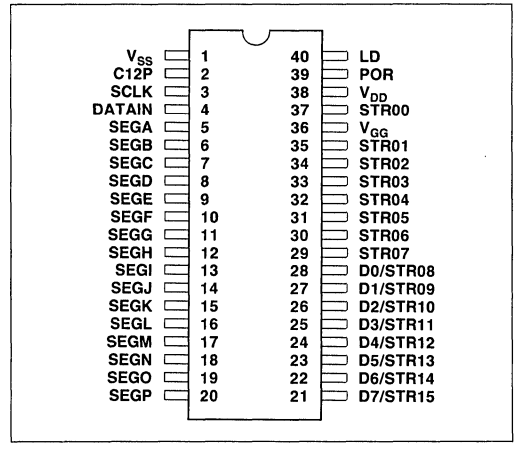
Part Number	Package Type	Drive Voltage	Temperature Range (°C)
10955P-40	Plastic	40V	0 to +70
10955P-50	Plastic	50V	0 to +70
10955PE-40	Plastic	40V	−40 to +85
10955PE-50	Plastic	50V	−40 to +85



10955 Block Diagram

INTERFACE DESCRIPTION

Signal Name	Pin No.	Function
V_{SS}	1	Power and signal reference
C12P	2	Test clock—factory test
SCLK	3	Serial input data clock
DATAIN	4	Serial data input
SEGA-SEGP	5–20	Segments A through P driver outputs
D7/STR15–D0/STR08	21–28	Direct segment outputs or strobe outputs
STR07–STR00	29–35, 37	Strobe outputs
V_{GG}	36	Display voltage
V_{DD}	38	Logic supply voltage
POR	39	Power on reset
LD	40	Data Load Strobe



10955 Pin Configuration

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS*

All voltages are specified relative to V_{SS}.

Parameter	Symbol	Value	Unit
Supply Voltage	V_{DD}	+0.3 to −25	V
Operating Current	I_{DD}	8	mA
Input Voltage	V_{IN}	+0.3 to −25	V
Display Voltage	V_{GG}	+0.3 to −50	V
Operating Temperature			
Commercial	T_C	0 to +70	°C
Industrial	T_I	−40 to +85	°C
Storage Temperature	T_{STG}	−55 to +125	°C
Input Capacitance	C_{IN}	5	pF
Output Capacitance	C_{OUT}	10	pF

***Note:** Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the other sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

(V_{DD} = −18.0 to −22.0 Vdc, V_{SS} = 0 Vdc, TA = 0°C to +70°C (commercial) or −40°C to +85°C (industrial), unless otherwise noted. All voltages referenced to V_{SS}.)

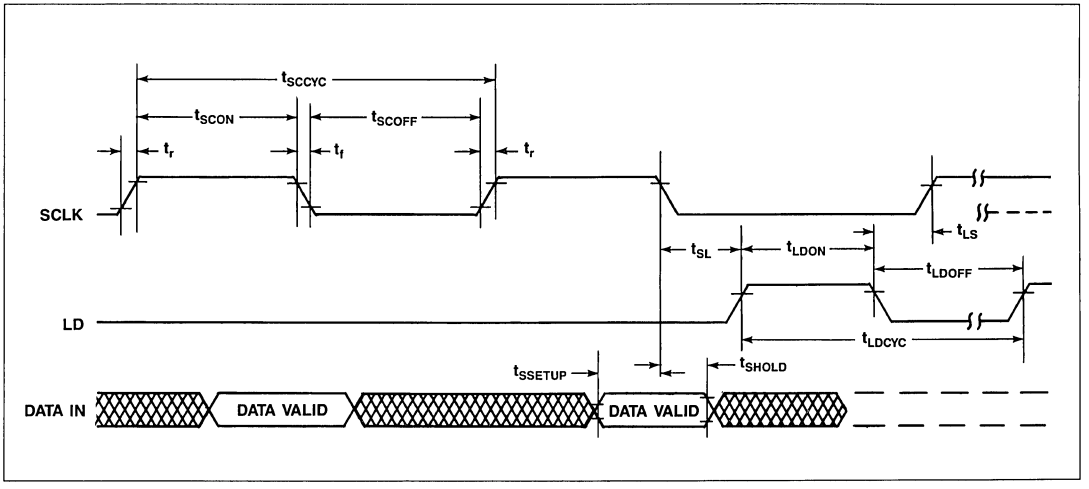
Parameter	Symbol	Min.[4]	Typical[3]	Max.[4]	Unit
Operating Current, Logic	I_{DD}				mA
Commercial		—	3.2	6.4	
Industrial		—	4.0	8.0	
Operating Current Display	I_{GG}				
1 strobe plus 24 segments @ V_{OH}					
Commercial		—	—	6.5	mA
Industrial		—	—	8.0	mA
1 strobe plus 16 segments @ V_{OH}					
Commercial		—	—	4.3	mA
Industrial		—	—	5.3	mA
All display drivers					
@ V_{GG} and 85°C		—	—	320	μA
Display Voltage	V_{GG}				V
10955-40		−40.0	—	—	
10955-50		−50.0	—	—	
Input Leakage (at −20V)	I_{IL}	—	—	10	μA
Input (DATAIN, LD, SCLK)					V
Logic "1"	V_{IH}	−1.2	−0.5	+0.3	
Logic "0"	V_{IL}	V_{DD}	−6.0	−4.2	
Input POR					V
Logic "1"	V_{IHPO}	−3.0	—	+0.3	
Logic "0"	V_{ILPO}	V_{DD}	−12.0	−10.0	
Output (C12P)					V
Logic "1"	V_{OHSY}	−0.7	—	+0.3	
Logic "0"[1]	V_{OLSY}	V_{DD}		—	
Output (Strobe STR00–07, D0–D7, SGA–SGP)					V
Logic "1" (I_{Load} = 10 mA)	V_{OH}	−1.5	−1.0	V_{SS}	
Logic "1" (I_{Load} = 20 mA)[2]	V_{OH}	—	−2.0	V_{SS}	
Logic "0" (I_{Load} = 0 mA)	V_{OL}	V_{GG}	0.5 + V_{GG}	0.95 × V_{GG}	

Notes:
1. Open drain driver. Requires external pull-down resistor for testing only.
2. STR00–STR07 only (also for D0–D7 when used as character drivers)
3. Typical measured at V_{DD} = 20.0V and Y_A = 25°C.
4. Max. values are most positive limits. Min. values are most negative limits.

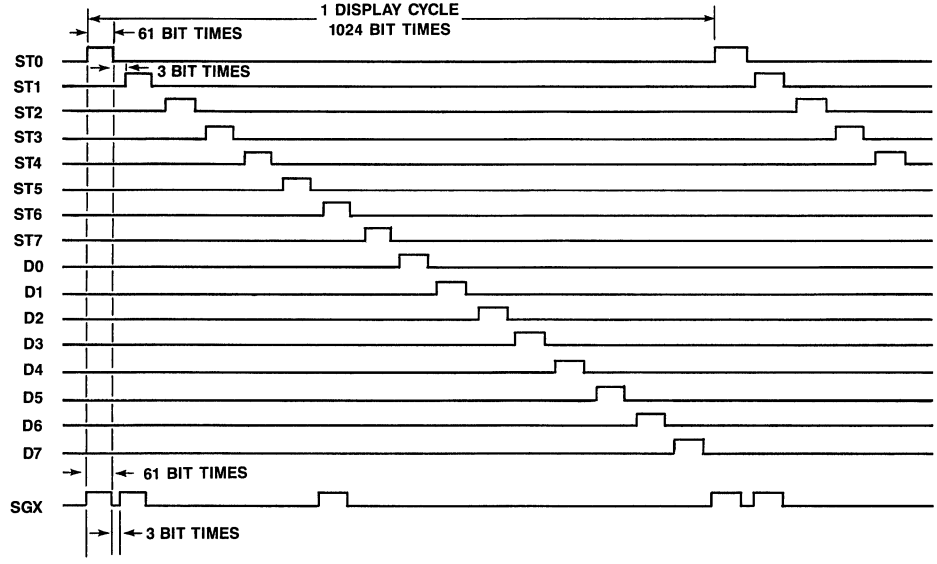
AC CHARACTERISTICS

Characteristic	Symbol	Min.	Max.	Unit
Clock Timing Cycle Time	t_{CYC}			
Commercial		6.66	23.0	usec
Industrial		5.88	24.0	usec
HOST INTERFACE TIMING				
Serial Clock (SCLK)				
On Time	t_{SCON}	1.2	40.0	usec
Off Time	t_{SCOFF}	1.0	—	usec
Cycle Time	t_{SCCYC}	2.2	—	usec
Serial Data (DATAIN)				
Set-up Time	t_{SSETUP}	400	—	nsec
Hold Time	t_{SHOLD}	400	—	nsec
Serial Clock to LD Time	t_{SL}	600	—	nsec
LD to Serial Clock	t_{LS}	400	—	nsec
Data Load (LD)				
On Time	t_{LDON}	1.0	—	usec
Off Time (Commercial	t_{LDOFF}	46.0	—	usec
Off Time (Industrial)	t_{LDOFF}	48.0	—	usec
Cycle Time (Commercial)	t_{LDCYC}	69.0	—	usec
Cycle Time (Industrial)	t_{LDCYC}	72.0	—	usec

Note:
t_r and t_f = rise and fall time of clocking signals which are 10 to 30 nsec.



Serial Interface Timing Waveforms



Notes:
1. t_{CYC} = 2 bit times.
2. Timing shown is for 16 characters with a duty cycle of 61.

Display Scan Timing Diagram

FUNCTIONAL DESCRIPTION

All timing signals required to control the display are generated by the 10955 device after the display buffer and control registers have been loaded from the host processor. In the following functional description, refer to the 10955 block diagram.

Input data is loaded into the Display Data Buffer via the serial data input channel. Internal timing and control logic synchronize the digit output signals with the segment output signals to provide the proper timing for the multiplexing operation. The segment decoding is performed in a 128 x 16 PLA character code set.

CHARACTER DRIVERS (STR00-STR07)

The eight character (grid) drivers are used to select the display character positions sequentially during a refresh scan. Display characters are illuminated when the character driver for a particular character position and the segment (anode) drivers are energized simultaneously.

DISCRETE DRIVERS (D0-D7)

The function of these eight drivers depends on the display mode. In some modes these drivers act as segment (anode) drivers loaded directly from the Data Buffer (RAM). In other modes these drivers are used as extra character (grid) drivers (STR8-STR15). See Display Modes for further discussion of these driver functions.

SEGMENT DRIVERS (SGA-SGP)

Depending on the display mode, the sixteen segment drivers are loaded through an 8 x 16 PLA decoder or directly from the Data Buffer RAM.

SYSTEM CLOCK

Each 10955 device has its own on-board oscillator and clock generator.

POWER-ON RESET

The Power-On Reset (POR) input initializes the internal circuits of the 10955. This is normally performed when power (VDD) is applied. The following conditions are established by application of POR:

a. The grid and anode drivers (STR00-STR07, D0-D7, and SGA-SGP) are in the off state.

b. Duty Cycle register is set to zero.
c. The Digit Counter is set to 32 digits.
d. The Buffer Pointer is set to zero.
e. The Digit Time is set to 64.
f. The PLA Bypass/Sixteen Digit display mode is set.

At power on, the 10955 is held in an internal halt mode. This allows the host system to load the control registers and the data buffer without flashing invalid data on the display.

During the initial rise time of VDD at power turn-on, the magnitude of VGG should not exceed the magnitude of VDD.

HOST SYSTEM INTERFACE

Input data is loaded into the 10955 via a serial data input channel as a series of nine-bit words.

After nine bits of data (with the most significant bit first) have been shifted into the data buffer, a pulse on the LD signal loads the data into an internal buffer and informs the 10955 that a new data word is available. After the LD pulse, a new data word may be shifted in while the 10955 is processing the first word.

The following sections describe the format and functions of the input words which may contain either control data or display data.

Display Data Words

Display data words are loaded as nine bit codes. The lower eight bits (7-0) are data. The ninth bit (the most significant) is always a zero (0).

Sixteen display data words must be entered to completely load the Display Data Buffer. The Buffer Pointer is automatically incremented after each data word is stored in the buffer. The Buffer Pointer will automatically reset to character position 0 when its value is equal to the programmed digit count value. The Buffer Pointer may be set to any desired value with the Buffer Pointer Control Word. This permits arbitrary loading of the Display Data Buffer.

Control Words

Control words are distinguished from display words by the fact that the most significant bit is always a one. Control words and their functions are defined below.

8	7	6	5	4	3	2	1	0	BIT
			DATA						DUTY CYCLE, DIGIT COUNT, BUFFER POINTER
1	CODE			PLA MODE		CONFIG.	DIGIT TIME		← CONTROL REGISTER
	0	1	X	X	X	X	X	X	DUTY CYCLE CONTROL
	1	0	0	X	X	X	X	X	DIGIT COUNT CONTROL
	1	1	0	0	X	X	X	X	BUFFER POINTER CONTROL
	0	0	0	X	X	X	X	X	CONTROL REGISTER
									(5 bits coded as shown below)
	0	0	0	X	X	Y	0	0	64 cycles per grid
	0	0	0	X	X	Y	0	1	16 cycles per grid
	0	0	0	X	X	Y	1	0	32 cycles per grid
	0	0	0	X	X	Y	1	1	8 cycles per grid
	0	0	0	X	X	0	Z	Z	16 digit configuration
	0	0	0	X	X	1	Z	Z	8 digit and two output
	0	0	0	0	0	Y	Z	Z	PLA bypass
	0	0	0	0	1	Y	Z	Z	Reserved for upgrade
	0	0	0	1	0	Y	Z	Z	Lower 64 PLA (64U)
	0	0	0	1	1	Y	Z	Z	Lower 64 PLA (64L)

5

Buffer Pointer

The Buffer Pointer Control code sets the Display Data Buffer Pointer. The five least significant bits of the code are loaded into the Buffer Pointer to select the character position as shown in Table 1.

Table 1. Load Buffer Pointer Codes

Load Code Value	Pointer Value	Character Position Selected
C0	00	0
C1	01	1
C2	02	2
C3	03	3
C4	04	4
C5	05	5
C6	06	6
C7	07	7
C8	08	8
C9	09	9
CA	0A	10
CB	0B	11
CC	0C	12
CD	0D	13
CE	0E	14
CF	0F	15

Note: D0–DF (Not Used)

Digit Count Control

The Digit Count Control command defines the number of character positions (grids) to be controlled. This code is normally used only during initialization routines, but it may also be used in conjunction with the Duty Cycle Control code to extend the range of brightness control. Strobing begins at character position 0 and proceeds thru the last position specified. If more than 16 grids are selected (17–32), extra time slots are generated for these phantom strobes. When the phantom strobes are active, strobes 0 through 15 are off so the displayed data is not affected although the duty cycle is decreased as each phantom strobe is added. The code, digit count value, and number of grids controlled by the Digit Counter are shown in Table 2.

Table 2. Load Digit Counter Control Codes

Code	Digit Counter Value	No. of Grids Controlled
80	00	32
81	01	1
82	02	2
83	03	3
84	04	4
85	05	5
86	06	6
87	07	7
88	08	8
89	09	9
8A	0A	10
8B	0B	11
8C	0C	12
8D	0D	13
8E	0E	14
8F	0F	15
90	10	16
91	11	17
92	12	18
93	13	19
94	14	20
95	15	21
96	16	22
97	17	23
98	18	24
99	19	25
9A	1A	26
9B	1B	27
9C	1C	28
9D	1D	29
9E	1E	30
9F	1F	31

Duty Cycle

The Duty Cycle Control code is used to turn on and off the display, to adjust display brightness, or to modify display timing. The time slot for each character is 8, 16, 32, or 64 internal cycles (an internal cycle = 1/2 t_{CYC} as selected by the Digit Time codes in the control register. The segment and digit drivers for each character may be turned on for a maximum of 5, 13, 29, or 61 cycles with a 3 cycle mandatory inter-digit off time. The lower six bits of the Duty Cycle Control code are loaded into the Duty Cycle Register. Resultant duty cycles (on-times and off-times) are shown in Table 3.

Table 3. Duty Cycle Control Codes

	Digit Time = 8		Digit Time = 16		Digit Time = 32		Digit Time = 64	
Code	On	Off	On	Off	On	Off	On	Off
40	—	8	—	16	—	32	—	64
41	—	8	—	16	—	32	—	64
42	—	8	—	16	—	32	—	64
43	1	7	1	15	1	31	1	63
44	2	6	2	14	2	30	2	62
45	3	5	3	13	3	29	3	61
46	4	4	4	12	4	28	4	60
47	5	3	5	11	5	27	5	59
48	5	3	6	10	6	26	6	58
49	5	3	7	9	7	25	7	57
4A	5	3	8	8	8	24	8	56
4B	5	3	9	7	9	23	9	55
4C	5	3	10	6	10	22	10	54
4D	5	3	11	5	11	21	11	53
4E	5	3	12	4	12	20	12	52
4F	5	3	13	3	13	19	13	51
50	5	3	13	3	14	18	14	50
51	5	3	13	3	15	17	15	49
52	5	3	13	3	16	16	16	48
53	5	3	13	3	17	15	17	47
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
5B	5	3	13	3	25	7	25	39
5C	5	3	13	3	26	6	26	38
5D	5	3	13	3	27	5	27	37
5E	5	3	13	3	28	4	28	36
5F	5	3	13	3	29	3	29	35
60	5	3	13	3	29	3	30	34
61	5	3	13	3	29	3	31	33
62	5	3	13	3	29	3	32	32
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
7C	5	3	13	3	29	3	58	6
7D	5	3	13	3	29	3	59	5
7E	5	3	13	3	29	3	60	4
7F	5	3	13	3	29	3	61	3

Control Register

There is a 5-bit control register, which can be loaded by the control word, 000XXYZZ. The lower 5 bits of this control word are loaded into the control register.

The least significant two bits of the control register set the total Digit Time for each character during the refresh cycle. Four values can be set using the codes, 8, 16, 32, or 64 cycles per grid. The default value set at power-on is 64 cycles per grid. Under conditions where the display can be subjected to quick movements during viewing (e.g. portable or vehicle mounted applications) it may be necessary to increase the refresh rate by selecting 8, 16 or 32 cycles per grid with the appropriate control codes.

The middle bit of the 5 bit control register determines the sixteen digit or eight digit configurations. The two most significant bits select one of the four PLA Modes.

DISPLAY MODES

The 10955 can operate in any of eight display modes which control the maximum number of active strobes and segments and the manner in which the RAM Data Buffer is decoded onto the segment drivers.

16 Digit Configuration

If the third bit of the control register is zero or is reset by the POR signal, the 16 digit configuration is selected. In this case, a maximum of 16 segments and 16 strobes are provided. The 16 words in the RAM Data Buffer correspond to the 16 strobes. The 8 data bits of each word are sent to the PLA for decode.

8 Digit Configuration

If the third bit of the control register is a one, the 10955 is configured into the 8 digit mode. In this case, a maximum of 8 strobes and 24 segments are allowed. The 8-bit words in the RAM Data Buffer are grouped into 8 word pairs which correspond to strobes STR0–STR7: 0-1, 2-3, 4-5, 6-7, 8-9, 10-11, 12-13, and 14-15. The data in the even-numbered word of each pair is loaded into the direct-output segment drivers (D0–D7). The data in the odd-numbered word of each pair is decoded in the segment PLA decoder before being loaded into the 16-segment output drivers (SGA–SGP).

PLA Bypass Mode

If both of the most significant bits of the control register are zero, the PLA Bypass Mode is selected. In this mode, the PLA is bypassed. Each data word is loaded directly into the segment drivers without being decoded by the PLA. Since there are only 8 data bits but 16 drivers, each data bit is loaded into two adjacent drivers which can be connected externally to provide twice the current drive of an individual driver. The data bits/segments selection allocation is as follows:

Data bit	7	6	5	4	3	2	1	0
Segments	O,P	M,N	K,L	I,J	G,H	E,F	C,D	A,B

Upper 64 PLA Mode (64U)

In this mode (bit 5 = 1, bit 4 = 0) the Upper 64 out of the 128 codes are used, (i.e., 64 to 127). Since 64 codes can be specified by a 6-bit word, the most significant two bits of the 8-bit word from the RAM are not used. However, the most significant two bits of the display data are brought out directly to SEGO and SEGP outputs. Therefore, the 64 codes can be decoded to the 16-segment outputs, or only 14-segment outputs leaving two for direct output from the RAM.

Lower 64 PLA Mode (64L)

This mode (bit 5 = 1, bit 4 = 1) is similar to the Upper 64 PLA Mode, but only the lower 64 codes (0–63) out of the 128 codes are used. The 64L and 64U PLA modes allow two independent sets of 64 codes to be programmed into one chip. In running the display, only one set can be selected at a time.

Fourth PLA Mode

A fourth PLA mode is reserved for future expansion of the 10955. This code (bit 5 = 0, bit 4 = 1) should not be used. Selecting this PLA mode may result in non-defined characters appearing on the display.

PLA CHARACTER SET CODES

Figure 1 shows the 16-segment and 14-segment driver assignments for the corresponding segmented displays. Figure 2 shows the 16-segment and 14-segment PLA character set patterns coded into the 10955.

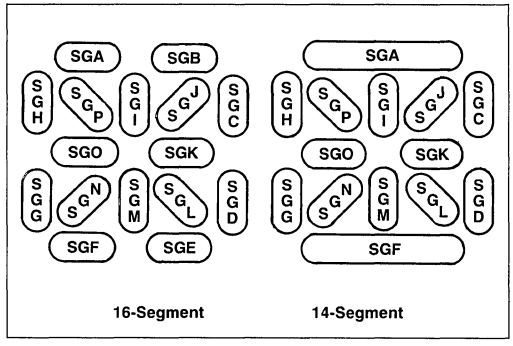
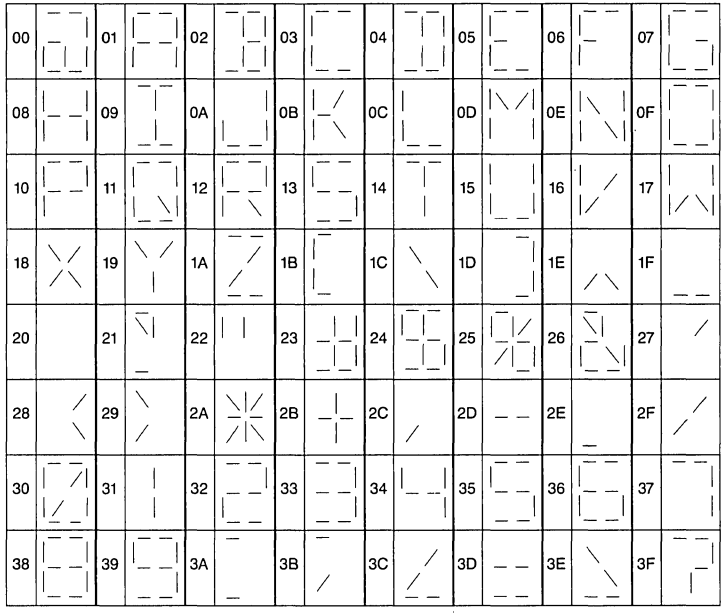
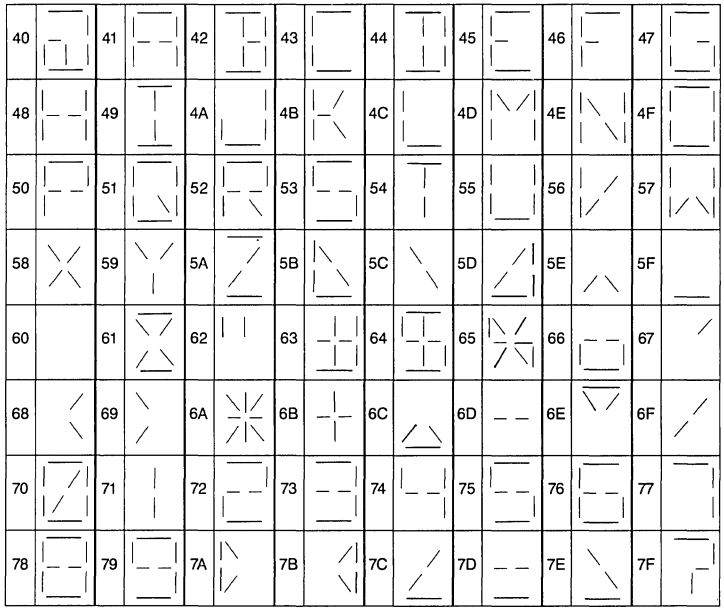


Figure 1. Segment Driver Assignments



16-Segment PLA Patterns

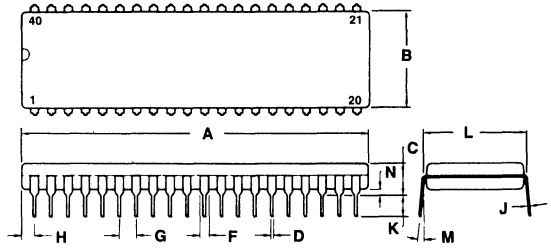


14-Segment PLA Patterns

Figure 2. 16- and 14-Segment PLA Character Sets

PACKAGE DIMENSIONS

40-PIN PLASTIC DIP



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	51.28	52.32	2.040	2.060
B	13.72	14.22	0.540	0.560
C	3.55	5.08	0.140	0.200
D	0.36	0.51	0.014	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.30	0.008	0.012
K	3.30	4.32	0.130	0.170
L	15.24 BSC		0.600 BSC	
M	7°	10°	7°	10°
N	0.51	1.02	0.020	0.040

Section 6
Application Notes

Low-Cost Crystal Oscillator for Clock Input

PURPOSE

This application note describes a low cost oscillator circuit which will produce the basic input frequency required by the clock generator circuits in the Rockwell R65XX series microprocessors. This circuit can be constructed around either of two readily-available, low cost crystals. Both crystals are approximately the same cost, depending on source and quantities. These crystals, identified in the table below, may be obtained from Electro Dynamics, 5625 Foxridge Drive, Shawnee Mission, Kansas 66201, by ordering Part No. 333R05-001 (3.579 MHz) or 59672 (4.19 MHz).

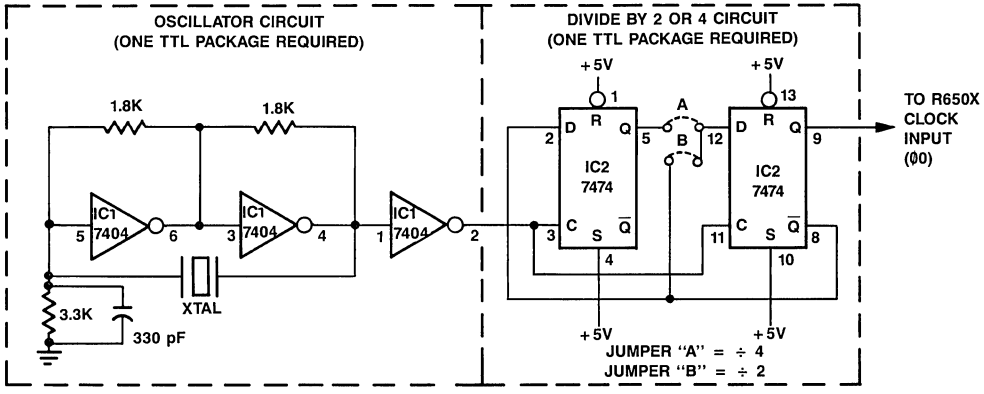
The oscillator output frequency is divided by 2 or by 4 to provide any of the frequency options shown in the table. By trading off the slight deviation in frequency from the standard 1 MHz or 2 MHz clock with cost, this approach can reduce the cost of the oscillator circuit to less than $2.00 each in quantity buys.

Crystal		Output Frequency (MHz)	
Primary Use	**Frequency**	**Divided By 2**	**Divided By 4**
Color TV P/N 333R05-001	3.579545 MHz	1.7897	0.894886
Automotive Clock P/N 59672	4.194304 MHz	2.097152	1.048576

DESCRIPTION

The clock input frequency generator shown in the schematic consists of an oscillator circuit requiring one IC and a divide by 2 or by 4 circuit which also requires only one IC. The output of this circuit is applied to the (ϕ0) input of the R650X microcomputer clock generator circuit.

The oscillator circuit uses three of the six drivers in a standard 7404 and a crystal to produce an output. The oscillator output is input to a standard 7474 and the frequency is divided by either 2 or 4 depending on the jumper connections (A or B), as shown in the schematic.



Clock Input Frequency Generator

Rockwell

R6500/R6532
Timer Interrupt Precautions

PURPOSE

The R6532 is a RAM, I/O, timer (RIOT) combination device. The timer is an on-board count-down circuit and may be programmed to cause interrupts to the R6502 microprocessor. The timer interrupt is enabled by simply addressing the R6532 with the necessary selects and address bits. It is *not* necessary to load any internal registers to enable the interrupt, only to address the device.

The R6502 (or one of its 28-pin versions) microprocessor can inadvertently cause addressing of the R6532 (or other devices with a timer) during start-up or RESET operations. When $\overline{RES}$ is driven low, the R6502 and R6532 are initialized to known internal states. When $\overline{RES}$ goes high, however, the start-up procedure is initiated and the first two cycles contain arbitrary or random addresses on the bus. Table 1 illustrates the cycles immediately following $\overline{RES}$ going high.

In most cases, this is normally not a problem, since the occurrence of $\overline{RES}$ causes the R6502 $\overline{IRQ}$ interrupt to be disabled. However, if the R6532 interrupt output is connected to the $\overline{NMI}$ (Non-Maskable Interrupt) input of the R6502 and the R6532 timer interrupt is inadvertently enabled during start-up, a timer interrupt may occur before the processor has executed its system initialization procedure. The possibility of all these things happening is somewhat remote, but can be a potential problem.

DESCRIPTION

There are several solutions to this problem:

1. Use the $\overline{IRQ}$ interrupt input of the R6502, instead of $\overline{NMI}$. In this way, the $\overline{IRQ}$ interrupt is automatically disabled by $\overline{RES}$ and the R6532 timer interrupt cannot occur.

2. Use separate $\overline{RES}$ signals for the R6502 and the R6532. In order to avoid the first two cycles of the start-up (wherein the addresses are unpredictable), it is necessary to hold the $\overline{RES}$ to the 6532 low *after* the $\overline{RES}$ to the R6502 goes high. This is illustrated in Figure 1.

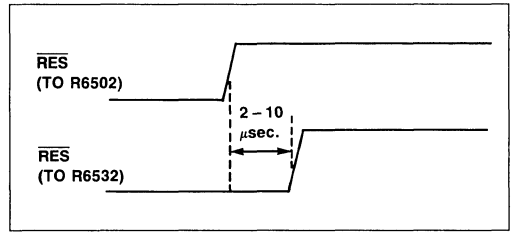


Figure 1. Delayed Reset to R6532

Table 1. Start-Up Cycle

Cycles	Address Bus	Data Bus	External Operation	Internal Operation
1	?	?	Don't Care	Hold during Reset
2	? + 1	?	Don't Care	First Start State
3	0100 + SP	?	Don't Care	Second Start State
4	0100 + SP – 1	?	Don't Care	Third Start State
5	0100 + SP – 2	?	Don't Care	Fourth Start State
6	FFFC	Start PCL	Fetch First Vector	
7	FFFD	Start PCH	Fetch Second Vector	Hold PCL
8	PCH PCL	First OP CODE	Load First OP CODE	

3. Gate the R6532 $\overline{IRQ}$ output to the R6502 $\overline{NMI}$ input with a circuit which is enabled by the initialization routine of the processor. Figure 2 shows a possible configuration, with the gate enabled only when the processor does a write operation with A15 high. Note that this scheme essentially allows disabling of the $\overline{NMI}$ in the R6502.

There are likely to be many other solutions to this problem. These ideas are intended to provide some simple ones and to provoke thought for others from the reader.

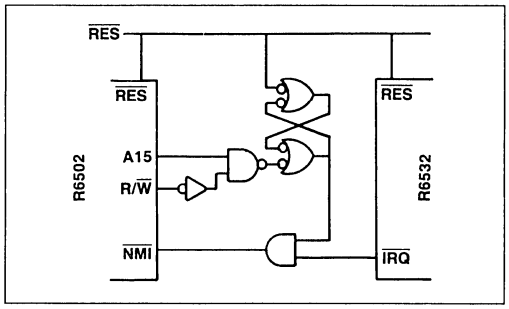


Figure 2. Scheme for Gating to the NMI Input

Rockwell

A Dot Matrix Controller System Design Using the 10938/10939 Display Drivers and R6500/1EB Microcomputer

by Terry Christensen and Tal Klaus,
Semiconductor Products Division, Newport Beach, California

INTRODUCTION

The Rockwell 10938 and 10939 Dot Matrix Display Controller is a two-chip MOS/LSI general purpose display controller system designed to interface a host processor to dot matrix displays (vacuum-fluorescent or LED).

This application note describes how this chip set can be used to drive a 40 character 5 × 7 dot matrix vacuum-fluorescent display. For demonstration purposes, a Futaba 40-SD-41Z display is used and a Rockwell R6500/1EB Backpack Emulator serves as the host. With appropriate adjustments to the power supplies, the interfacing technique described is valid for all similar displays and any host processor. Since the display has 40 grids, two 10939s are required.

The two chip set will drive displays containing up to 35 anodes (dots or segments) and 20 grids (characters).

The 10938 controls the anodes. It contains the anode drivers and a PLA-type decoder programmed to generate the 5 × 7 dot patterns for the full 96 character ASCII set. A similar device, the 10941, is programmed to generate the ASCII character set for 16 segment displays as well as bar graph patterns. The anode driver chips may be driven in parallel to generate patterns for more than 35 dots. An example of this is the 10942/10943 anode driver set which is programmed to generate patterns for 5 × 12 dot matrix displays.

The 10939 controls the grids. In addition to 20 grid drivers, it contains a cursor driver, a 20 character display data buffer, logic to control grid timing and display refresh, and the host interface logic. These devices may be cascaded to drive displays with as many as 80 grids. Since the 10939 performs the grid strobing and display refresh functions, the host processor need only define the operating parameters (such as duty cycle and character count) and update the display message.

The hardware section of this document describes the demonstration system and explains the operation of the display controller chip set. The software section describes several methods of controlling the display drivers and the display output.

DESCRIPTION OF HARDWARE

The simplicity of the hardware to drive the display is shown in the Figure 1 schematic and is presented in three sections: the host processor, the display drivers and the power supply.

Host Processor

The host processor for this application is a Rockwell R6500/1EB Backpack Emulator which is the PROM prototyping version of the masked-ROM R6500/1 Single Chip NMOS Microcomputer. The R6500/1EB is totally upward/downward compatible with all members of the R6500 family. It is designed to accept standard 5-volt 24-pin PROMs, EPROMs or ROMs directly in a socket on top of the emulator which simplifies program development. A 2 MHz crystal provides the timing reference for the generation of a 1 MHz internal clock. Reset to the emulator is supplied during power on while the RC circuit is charging. The system can be reset at other times by the push button switch.

Data may be transferred from a host processor to the display controller in either a parallel or a serial mode. In this application, parallel data is sent from port B of the emulator chip to the 10939 data ports. Emulator lines PC0 and PC1 control the load lines of the 10939s. Line PD0 on the emulator chip controls the reset circuit that drives the POR lines of the 10939s. This places the reset of the display controllers under software control. A level translator circuit converts the 0 to +5V TTL levels of the host to the +5V to −15V levels of the display controller devices.

Display Control

The display driver chip set interfaces directly with the vacuum fluorescent display tube. The selected display tube has a 5 × 12 dot matrix. For this demonstration, rows one through seven are connected to the 10938 anode drivers to serve as a 5 × 7 dot matrix. The dots of row nine are connected together to form a cursor and the anodes of rows 8, 10, 11 and 12 are unused.

The two 10939 devices are connected in daisy-chain fashion. Each 10939 device has its own on-board oscillator and clock generator. However, when more than one 10939 is used in a system, the same clock must be used for all devices. The MASTER pin on the 10939 device which is to supply the system clock must be connected to VDD, but on the other 10939 device, the slave, the MASTER pin is connected to VSS. These connections activate the oscillator on the master 10939 and cause a three-level four-state signal to be output on the CLOCK output. The oscillator on the slave 10939 is deactivated. The internal clock generators on both the master and slave devices use the signal on the CLOCK pin as an input. This minimizes the skew between master and slave devices.

As shown in the schematic, for this application, the master 10939 controls the left half of the display and the slave controls the right half. Strobe 0 (STR00) controls the left most digit (MSB) and strobe 19 (STR19) controls the right most digit (LSB) of

each half of the display. The cursor outputs are diode ORed to prevent ghosting and they are pulled down to VGG to provide a normally off signal to the display.

A two line synchronization port (SOP and SIP) insures that only one 10939 device at a time drives the display. When one 10939 outputs its last character, it emits a pulse on SOP. The next 10939 receives this pulse on its SIP input and starts its display cycle. This sequence continues through all of the 10939's in a chain. The SOP of the last 10939 is connected back to the SIP of the first 10939 to start another cycle. The limit to the number of 10939's in the chain is determined by: 1) the load on the clock output on the master 10939, and 2) the display refresh requirements. The synchronization signal propagates during the last character time of its own 10939 and thus does not require any extra time before the first character of the next 10939. The duty cycles of all the 10939's in the chain must be the same.

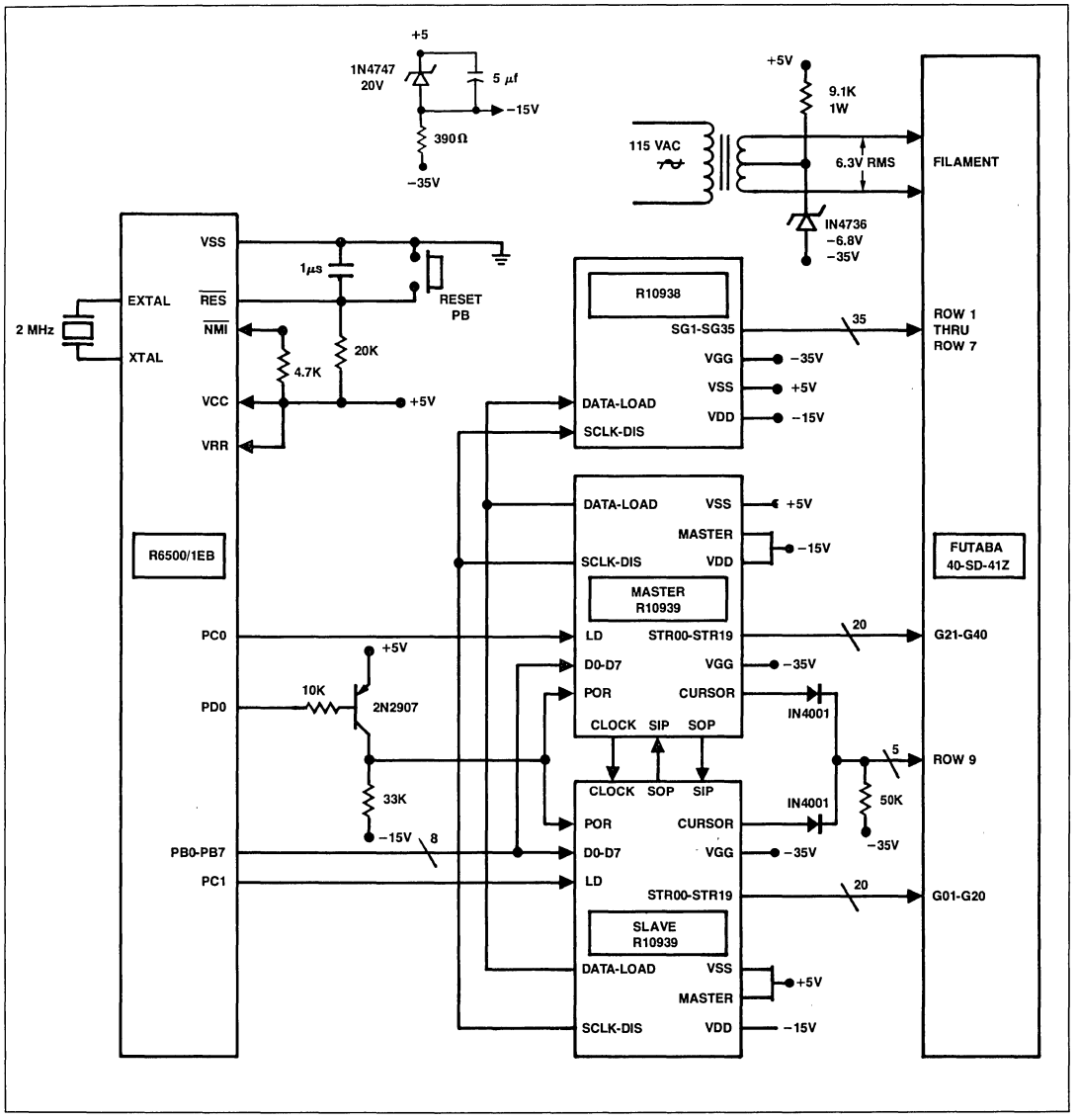


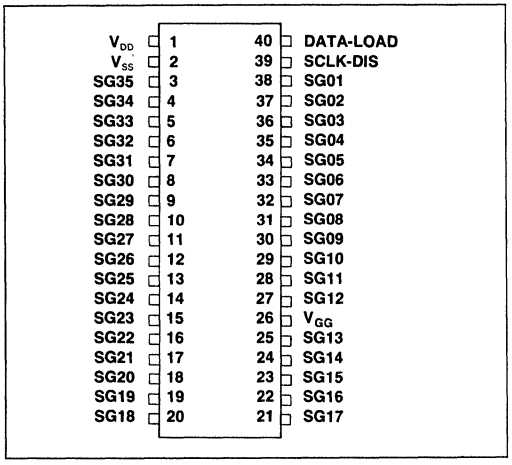
Figure 1. Display System Schematic

Display data and timing is output to the 10938 device via a two line serial port consisting of the SCLKDIS and DATALOAD pins. In order to minimize the number of package pins, these outputs are multiplexed, three-level, four-state drivers.

The SCLKDIS signal is composed of the shift clock which shifts new data into the 10938 device and a disable signal which sets all of the 10938 display output drivers to the display off state. The DATALOAD signal is composed of serial 8-bit ASCII data and a load signal to transfer the new data from the 10938 input buffer through the PLA to the display driver outputs. The ASCII data is output with the most significant bit first.

10938 Pin Functions

Signal Name	Pin No.	Function
V_{SS}	2	Power and signal reference
SG01-SG35	3-25, 27-38	Anode driver outputs
SCLK-DIS	39	Serial data shift
DATA-LOAD	40	Serial data output/latch control
V_{DD}	1	DC Power
V_{GG}	26	Pull down driver voltage



10938 Pin Configuration

10939 Pin Functions

Signal Name	Pin No.	Function
V_{SS}	36	Power and signal reference
V_{DD}	37	DC Power
CLOCK	38	Synchronization Clock
CURSOR	14	Cursor drive output
MASTER	39	Master/Slave Mode control
SIP	3	Sync Input
SOP	2	Sync Output
D0-D7	6-13	Serial or parallel data input
LD	5	Inputn data strobe
POR	4	Power-on reset
SCLK-DIS	1	Serial data shift clock
DATA-LOAD	40	Serial data output/latch control
STR00-STR19	15-34	Grid Drive Outputs
V_{GG}	35	Pull down driver voltage

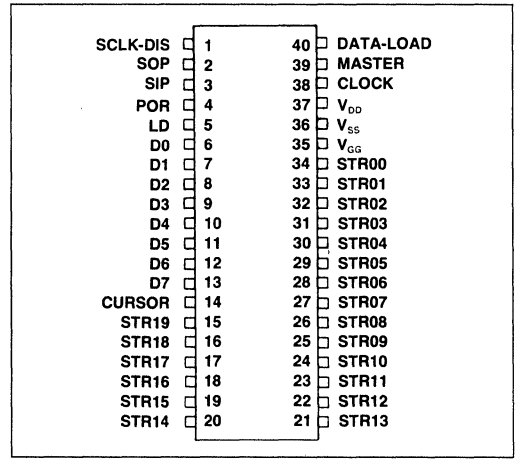
Power Supply

The power for this application is derived from two linear power supplies for VSS (+5 Vdc) and VGG (−35 Vdc). A third level for VDD (−15 Vdc) is obtained from a zener reference between VSS and VGG. Power requirements at room temperature (25°C) are as follows:

VSS +5 ±0.5 Vdc @ 40 ma
VDD −15 ±1.5 Vdc @ 12 ma
VGG −35 ±3.5 Vdc @ 16 ma

These levels are for worst case operation, i.e., with all 35 dots ON. For normal alphanumeric display characters, the VGG power to the 10938 is reduced by 50 percent for a total of about 11 ma. At 0°C operation, the power requirement would increase about 20 percent.

In addition to the dc levels for the IC devices, the vacuum-fluorescent display tube also requires an ac filament voltage. The filament power for the Futaba 40-SD-41 display tube is typically 6.3 Vac at 150 ma. This is driven from a center-tapped transformer and biased at 6.8 V above VGG with a zener diode as shown in Figure 2.



10939 Pin Configuration

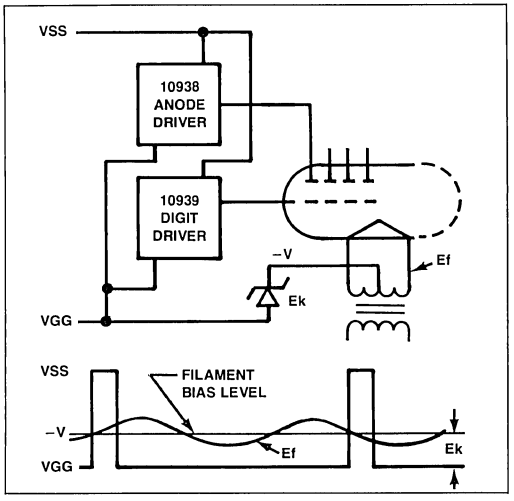


Figure 2. Basic Drive Circuit

DISPLAY OPERATION

At power on, the 10939 is placed in an internal host mode with reset from the R6500/1EB. This allows the host system to load the control registers and the data buffer without flashing "garbage" on the display. The normal display refresh sequence is started upon receipt of a START REFRESH control code. Only the master 10939 in a multi-chip system will recognize the START REFRESH code. The master will start the slave(s) at the appropriate time by using the SOP signal.

During the initial rise time of VDD at power turn-on, the magnitude of VGG should not exceed the magnitude of VDD.

Data bytes may be loaded into a 10939 in either a serial or a parallel data load mode. At power-on reset, the device is set to serial load mode. The parallel load mode is implemented when any of the six data input lines D2-D7 is raised to VSS (TTL logic "1"). After the parallel load mode has been implemented, the chip must be reset to return to serial load mode.

When using serial data load mode exclusively, it is recommended that input lines D2-D7 be externally tied to VDD to prevent inadvertent implementation of the parallel load mode. The data line D0 is used for data input, and the serial clock is input on D1. After eight bits of data (with the most significant bit first) have been shifted into the data buffer, a pulse on the LD signal loads the data into an internal buffer and informs the 10939 that a new data word is available. After the LD pulse, a new data word may be shifted in while the 10939 is processing the first word.

In parallel mode, data bytes are loaded into the 10939 by loading the data onto D0-D7, then pulsing the LD input. Before sending data to the chip, implement the parallel load mode by toggling the data lines. This will not be effective unless it is done after POR has gone low.

In this application, the data lines for both 10939s are controlled by emulator port B. The LD lines determine which device accepts the output data.

SOFTWARE

The subroutines of this section control the display in the previously described system. Included are examples of display driver initialization, data transfer to the display drivers and display scrolling. The routines are written in 6502 Assembly language and assume 1 MHz operation. With minor modifications, they may be used for a system having a display with a different grid count.

The following definitions are used throughout:

```
        CONSTANTS

MRS     = $02       MASTER 10939
SLV     = $01       SLAVE 10939
ALL     = $03       BOTH 10939'S

DUT     = $5A       DUTY CYCLE = 24/32
DT      = $06       DIGIT TIME = 32
CC      = $94       CHARACTER COUNT = 20

          RAM

          * = $0
HOLD      * = * +1  LOAD LINE SELECT

      BIT 1 = MASTER 10939 (UPPER 1/2 OF DISPLAY)
      BIT 0 = SLAVE 10939 (LOWER 1/2 OF DISPLAY)

KNTR    * = * +1    COUNTER FOR # OF DIGITS TO OUTPUT
KNT2    * = * +1    COUNTER FOR DISPLAY ROTATION
DATA    * = * +1    DATA TO BE OUTPUT TO 10939'S
SDATA   * = * +1    TEMP REG FOR SERIAL OUTPUT
PNTR    * = * +2    TABLE POINTER
BPNT    * = * +2    2ND POINTER FOR DISPLAY ROTATION
TEMP    * = * +1    SCRATCH PAD
WAITER  * = * +1    DELAY LOOP COUNTER

          I/O

PBIO    = $081      DISP DATA LINES
PCIO    = $082      DISP LOAD LINES

      BIT 0 = SLAVE (RIGHT OR LOWER)
      BIT 1 = MASTER (LEFT OR UPPER)

PDIO    = $083      DISP DRIVER CNTL LINES

      BIT 0 = POR

LLATCH  = $085      LOWER LATCH
ULATCH  = $088      L U LTCH, XFR 2 CNTR, CLR FLG
CR      = $08F      CONTROL REGISTER
```

DISPLAY DRIVER CONTROL WORDS

Control Word Assignments

Hex Value	Function
01	Load 01 into Data Buffer
05	Set digit time to 16 cycles per grid
06	Set digit time to 32 cycles per grid
07	Set digit time to 64 cycles per grid
08	Enable Normal Display Mode (MSB in data word is used for cursor control only)
09	Enable Blank Mode (data words with MSB = 1 will be blanked and cursor will be on)
0A	Enable Inverse Mode (data words with MSB = 1 will be "inversed" and cursor will be on)
0E	Start Display Refresh Cycle (use only once after reset)
40-7F	Load Duty Cycle Register with lower 6 bits (0-63)
80-9F	Load Digit Counter (80=32, 81=1, 82=2, etc.)
C0-D3	Load Buffer Pointer Register with lower 5 bits

Duty Cycle Control Codes

	Digit Time = 16		Digit Time = 32		Digit Time = 64	
Code	On	Off	On	Off	On	Off
40	—	16	—	32	—	64
41	—	16	—	32	—	64
42	—	16	—	32	—	64
43	1	15	1	31	1	63
44	2	14	2	30	2	62
45	3	13	3	29	3	61
46	4	12	4	28	4	60
47	5	11	5	27	5	59
48	6	10	6	26	6	58
49	7	9	7	26	7	57
4A	8	8	8	24	8	56
4B	9	7	9	23	9	55
4C	10	6	10	22	10	54
4D	11	5	11	21	11	53
4E	12	4	12	20	12	52
4F	13	3	13	19	13	51
50	13	3	14	18	14	50
51	13	3	15	17	15	49
52	13	3	16	16	16	48
53	13	3	17	15	17	47
.	.	.	.	.	.	.
.	.	.	.	.	.	.
.	.	.	.	.	.	.
5B	13	3	25	7	25	39
5C	13	3	26	6	26	38
5D	13	3	27	5	27	37
5E	13	3	28	4	28	36
5F	13	3	29	3	29	35
60	13	3	29	3	30	34
61	13	3	29	3	31	33
62	13	3	29	3	32	32
.	.	.	.	.	.	.
.	.	.	.	.	.	.
.	.	.	.	.	.	.
7C	13	3	29	3	58	6
7D	13	3	29	3	59	5
7E	13	3	29	3	60	4
7F	13	3	29	3	61	3

Buffer Pointer Control Codes

Code Value	Pointer Value	Character Position
C0	00	0
C1	01	1
C2	02	2
C3	03	3
C4	04	4
C5	05	5
C6	06	6
C7	07	7
C8	08	8
C9	09	9
CA	0A	10
CB	0B	11
CC	0C	12
CD	0D	13
CE	0E	14
CF	0F	15
D0	10	16
D1	11	17
D2	12	18
D3	13	19

Load Digit Counter Codes

Code	Digit Counter Value	No. of Grids Controlled
80	00	32
81	01	1
82	02	2
83	03	3
84	04	4
85	05	5
86	06	6
87	07	7
88	08	8
89	09	9
8A	0A	10
8B	0B	11
8C	0C	12
8D	0D	13
8E	0E	14
8F	0F	15
90	10	16
91	11	17
92	12	18
93	13	19
94	14	20
95	15	21
96	16	22
97	17	23
98	18	24
99	19	25
9A	1A	26
9B	1B	27
9C	1C	28
9D	1D	29
9E	1E	30
9F	1F	31

Delay Loops

Delay loops DELAY and WATE0 will be frequently referenced. They are used to control the display driver data load cycle time and to set display update and scrolling speed.

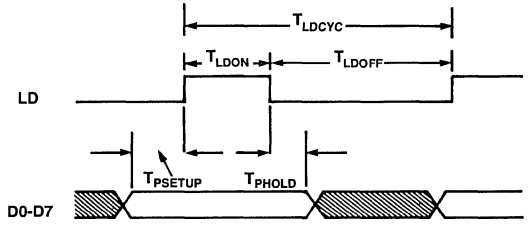
Y * 50MS DELAY LOOP

```
DELAY   LDY   #$03        WAIT 150 MS (3 * 50MS)
DLAY0   LDA   #<50000     LOAD COUNTER WITH 50000
        STA   LLATCH
DLAY1   LDA   #>50000     TO GET 50 MS DELAY
        STA   ULATCH
DLAY2   LDA   CR
        BPL   DLAY2
        DEY
        BNE   DLAY1
        RTS
```

SHORT DELAY LOOP
WAIT (17+10 * (ACC+1))US

```
WATE0   LDA   #$00        WAIT 27US
WATE    STA   WAITER      STORE LOOP COUNTER
WATE1   NOP
        DEC   WAITER
        BPL   WATE1
        RTS
```

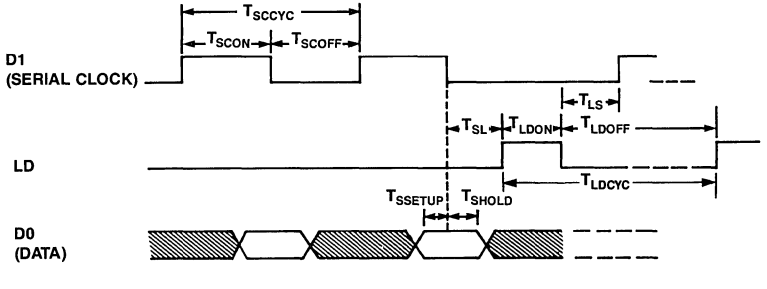
TIMING WAVEFORMS



40 μsec* ≤ T_{LDOFF}
1 μsec ≤ T_{LDON}
0 ≤ T_{PSETUP}
1 μsec ≤ T_{PHOLD}
60 μsec* ≤ T_{LDCYC}

*FOR INDUSTRIAL RATED PARTS SUBSTITUTE 44.5 FOR 40
66.7 FOR 60

Parallel Interface Timing Waveforms

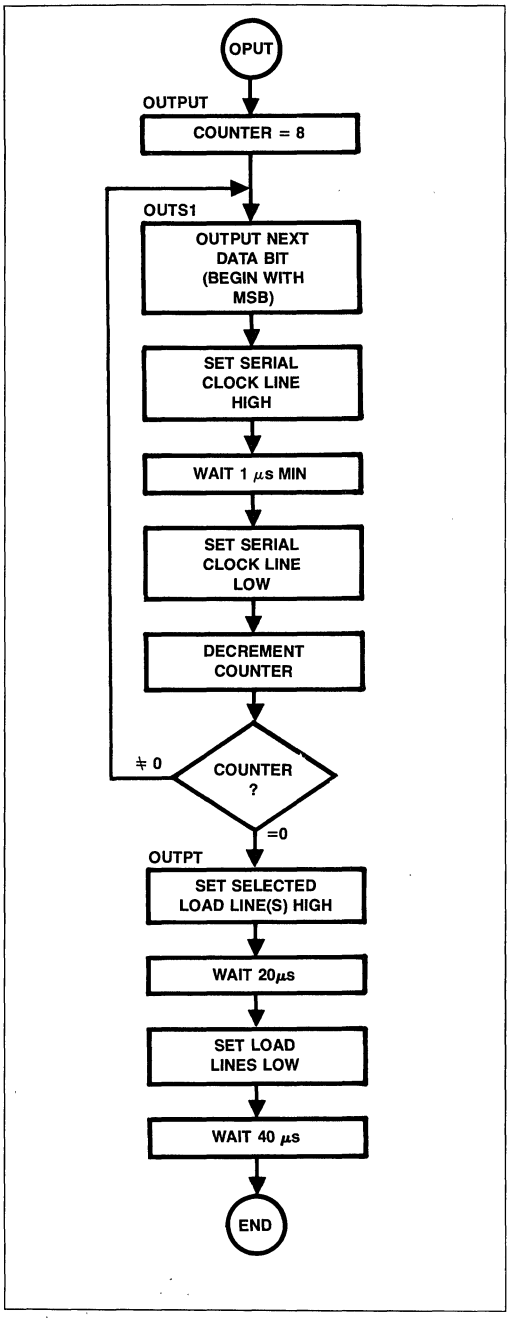


2 μsec ≤ T_{SCCYC}
1 μsec ≤ T_{SCON} ≤ 20 μsec
1 μsec ≤ T_{SCOFF}
1 μsec ≤ T_{SSETUP}
1 μsec ≤ T_{SHOLD}
1 μsec ≤ T_{LDON}
40 μsec* ≤ T_{LDOFF}
60 μsec* ≤ T_{LDCYC}
1 μsec ≤ T_{LS}
1 μsec ≤ T_{SL}

*FOR INDUSTRIAL RATED PARTS SUBSTITUTE 44.5 FOR 40
66.7 FOR 60

Serial Interface Timing Waveforms

6

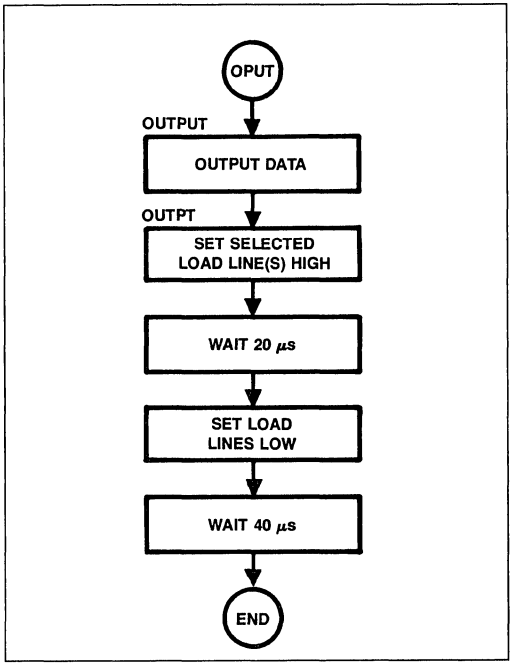


Flowchart: Serial Data Transfer to Display Controllers

Output A Character—Serial

This version of OPUT performs a serial data transfer from the host system to the selected 10939(s). Load line timing is the same for serial data transfer as it is for parallel data transfer. Serial data is shifted into each 10939 most significant bit first. It is not necessary to reload character data between load line pulses so a string of identical characters (when blanking the display for example) may be loaded by successively pulsing the load line.

```
        OUTPUT A CHARACTER

        SERIAL OUTPUT MSB FIRST
            HOLD = LOAD LINE(S)
            ACC OR DATA = DATA

OPUT    STA  DATA      WHEN DATA IN ACC
OUTPUT  LDX  #$08      INIT COUNTER
        LDA  DATA      FETCH DATA
        STA  SDATA

OUTS1   ROL  SDATA     DATA BIT TO C
        LDA  #$01      INIT ACC

    BIT 1 = SERIAL CLOCK LINE
    BIT 0 = DATA BIT

        ROL  A         DATA & SER CLK IN ACC
        STA  PBIO      OUTPUT DATA, TURN ON SER CLK
        AND  #01
        STA  PBIO      TURN OFF SER CLK
        DEX
        BNE  OUTS1     OUTPUT NEXT BIT

        ROL  SDATA     RESTORE CARRY

OUTPT   LDA  HOLD      SET LOAD LINE(S) HI
        STA  PCIO
        JSR  WATE0     WAIT 20 US
        LDA  #00       SET LOAD LINE(S) LO
        STA  PCIO
        LDA  #02       WAIT 40 US
        JSR  WATE
        RTS
```

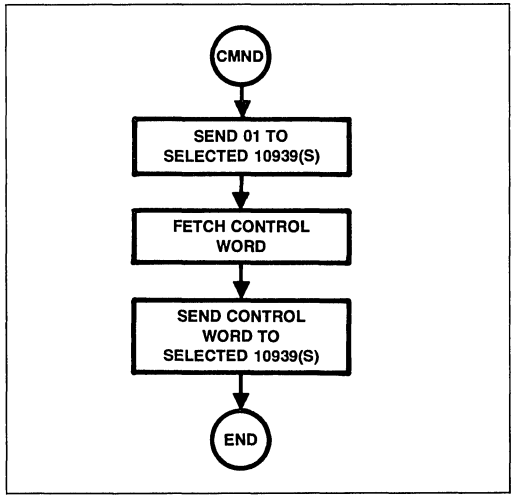


Flowchart: Parallel Data Transfer to Display Controllers

Output A Character—Parallel

This version of subroutine OPUT performs a parallel data transfer from the host system to one or both of the 10939's. Note that this subroutine contains two time delays. These are used to adjust the load line off and load cycle times. Also, it contains two entry points. OPUT is used when the output data is in the accumulator and OUTPUT is used, when the output data has been stored in RAM location DATA.

```
    OUTPUT A CHARACTER

    PARALLEL OUTPUT
       HOLD = LOAD LINE(S)
       ACC OR DATA = DATA

OPUT    STA   DATA        WHEN DATA IN ACC
OUTPUT  LDA   DATA        FETCH DATA
        STA   PBIO        OUTPUT DATA

OUTPT   LDA   HOLD        SET LOAD LINE(S) HI
        STA   PCIO
        JSR   WATE0       WAIT 20 US
        LDA   #00         SET LOAD LINE(S) LO
        STA   PCIO
        LDA   #02         WAIT 40 US
        JSR   WATE
        RTS
```



Flowchart: Send a Control Word to Display Controllers

Send A Control Word

CMND sends a control word from the host system to the selected 10939(s). The accumulator is loaded with the control word prior to the transfer to this subroutine.

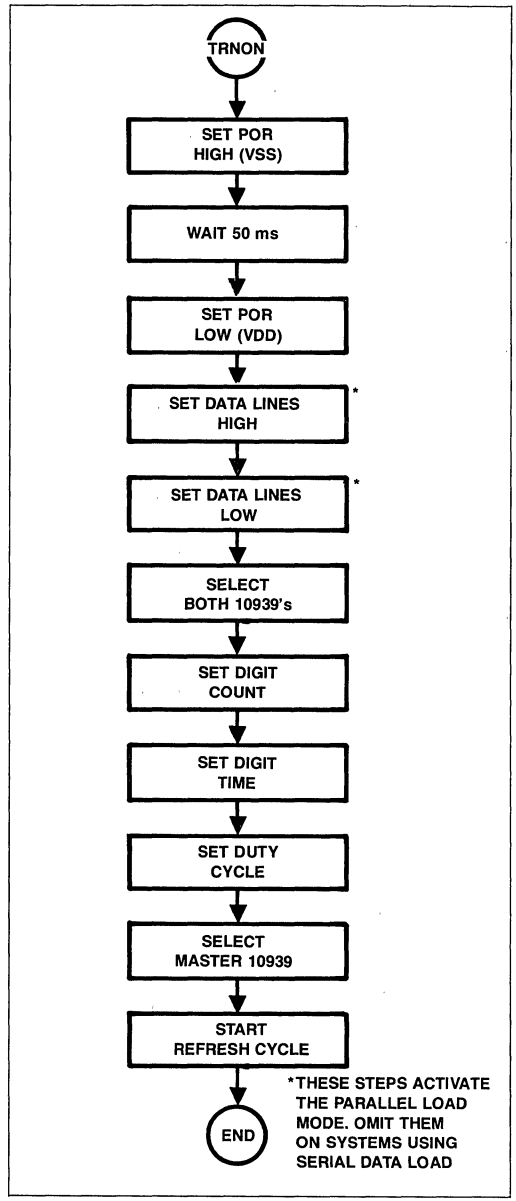
```
    SEND A COMMAND
       ACC = COMMAND

CMND    PHA
        LDA  #$01      PREPARE DISPLAY DRIVER
        JSR  OPUT      FOR CONTROL WORD
        PLA
        JSR  OPUT      SEND CNTL WORD
        RTS
```

6

Initialize Display Drivers

TRNON is an example of an initialization routine.

```
        SET UP DISPLAY CONTROLLER

TRNON LDA  #$00
      STA  PDIO     DISABLE 10939'S
      STA  PCIO     SET LOAD LINES LOW
      STA  PBIO     SET DATA LINES LOW

      LDY  #$01     WAIT 50 MS
      JSR  DLAY0

      LDA  #$01     RELEASE POR
      STA  PDIO

      LDY  #$01     WAIT 50 MS
      JSR  DLAY0

      LDA  #$FF     * PARALLEL DATA LOAD ONLY
      STA  PBIO     * PULSE DATA LINES
      LDA  #$00     *
      STA  PBIO     * PARALLEL DATA LOAD ONLY

TRN1  LDA  #ALL     SET DISPLAY CONTROLLER PARAMS
      STA  HOLD     ADDRESS BOTH 10939'S
      LDA  #CC      DIGIT COUNT = 20
      JSR  CMND
      LDA  #DT      DIGIT TIME = 32 CYC/CHAR
      JSR  CMND
      LDA  #DUT     DUTY CYCLE = 24/32
      JSR  CMND

      LDA  #MRS     LOAD MASTER ONLY
      STA  HOLD
      LDA  #$0E     START REFRESH CYCLE
      JMP  CMND     (RETURN VIA CMND)
```

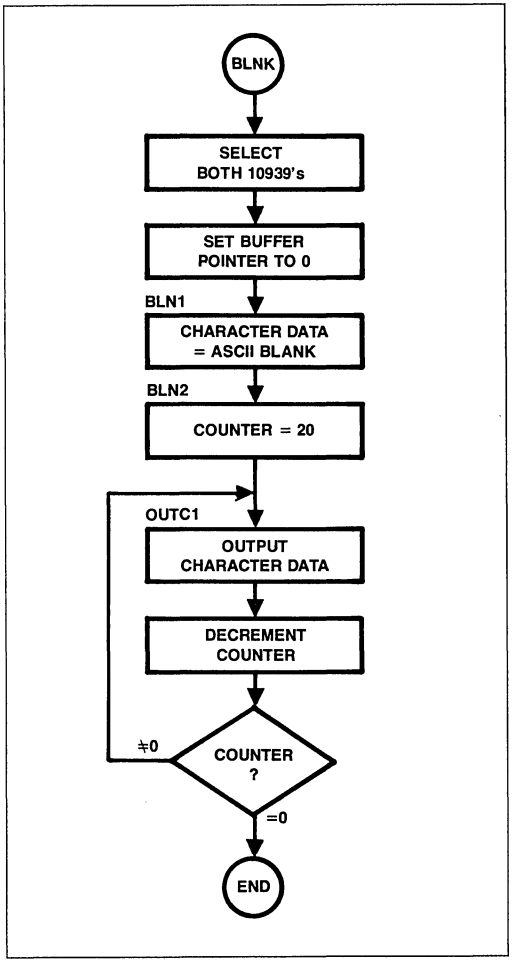


Flowchart: Display Controller Initialization

BLANK The Display

BLNK is a routine which fills the display buffers with blanks. By preloading HOLD, DATA and KNTR, then entering the routine at location OUTC, it can be used to display a string of constants.

```
     BLANK DISPLAY

BLNK   LDA  #ALL          ADDRESS BOTH 10939'S
       STA  HOLD
       LDA  #$C0          SET BUFFER POINTER TO ZERO
       JSR  CMND
BLN1   LDA  #$20          ASCII BLANK
BLN11  STA  DATA
BLN2   LDA  #$14          OUTPUT 20 DIGITS
       STA  KNTR
       BNE  OUTC1

     OUTPUT A CONSTANT
       ACC = DATA
       KNTR = # DIGITS (MAX=20)

OUTC   STA  DATA          SAVE DATA
OUTC1  JSR  OUTPUT        SEND IT
       DEC  KNTR
       BNE  OUTC1
       RTS
```



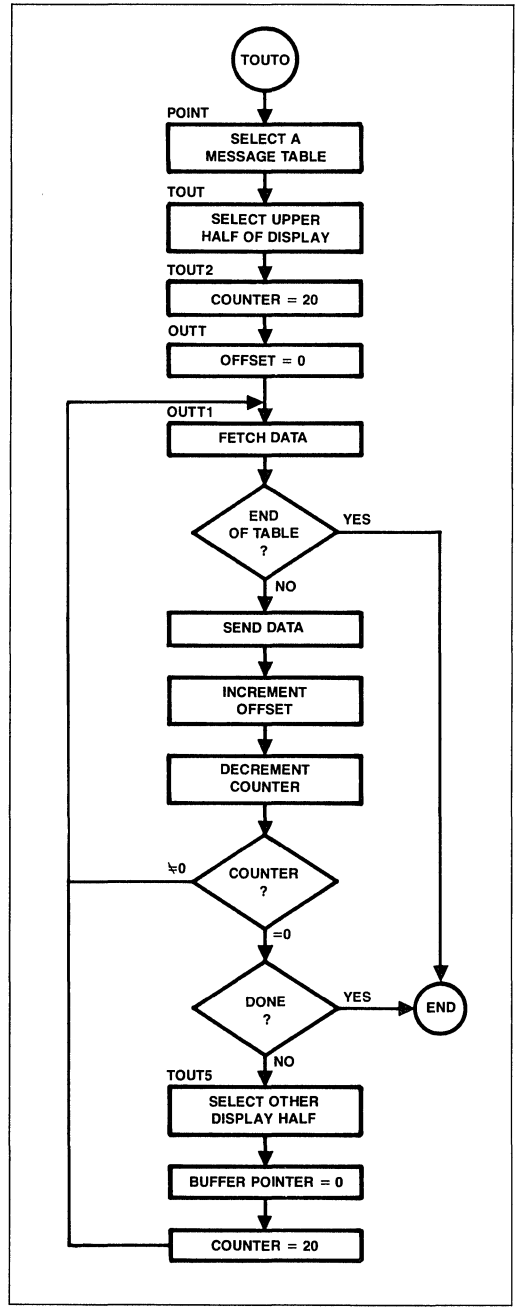
Flowchart: Blank the Display

6

Load A Message

TOUT0 loads the display with data from a table stored in RAM or ROM. Locations PNTR and PNTR+1 contain the address of the first byte of data to be fetched from the table. KNTR is preloaded with the number of characters to load. $FF is defined as an end of table flag so the execution of the routine can be terminated either by the count down of KNTR or the detection of the end of a table.

```
        OUTPUT FROM TABLE

              BUFFER POINTER MUST BE PRELOADED
              WHEN USING ENTRY POINTS BEFORE
              TOUT5

TOUT0   JSR   POINT          SET UP POINTER

TOUT    LDA   #MRS          SELECT MASTER
TOUT1   STA   HOLD
TOUT2   LDA   #$14          20 CHARS MAX
TOUT3   STA   KNTR
TOUT4   JSR   OUTT          SEND IT

TOUT5   LDA   #$03          SELECT THE OTHER 10939
        EOR   HOLD
TOUT7   STA   HOLD
        LDA   #$C0          BUFF PNTR = 0
        JSR   CMND
        LDA   #$14          20 CHARS MAX
TOUT8   STA   KNTR
        JMP   OUTT1         SEND IT

OUTT    LDY   #$00          INITIALIZE COUNTER
OUTT1   LDA   (PNTR),Y      FETCH DATA
        CMP   #$FF          END OF TABLE ?
        BEQ   OUTT2         YES
        JSR   OPUT          NO: SEND IT
        INY                 POINT TO NEXT TBL LOCN
        DEC   KNTR          COUNT DONE ?
        BNE   OUTT1         NO
OUTT2   RTS                 YES: EXIT

        LOAD TABLE POINTER
        X = OFFSET FOR POINTER TABLE

POINT   LDA   MESS,X        FETCH ADDRESS FROM
                              POINTER TABLE
        STA   PNTR          TRANSFER TO POINTER
                              REGISTER
        LDA   MESS+1,X
        STA   PNTR+1
        RTS
```



Flowchart: Display with Table Data

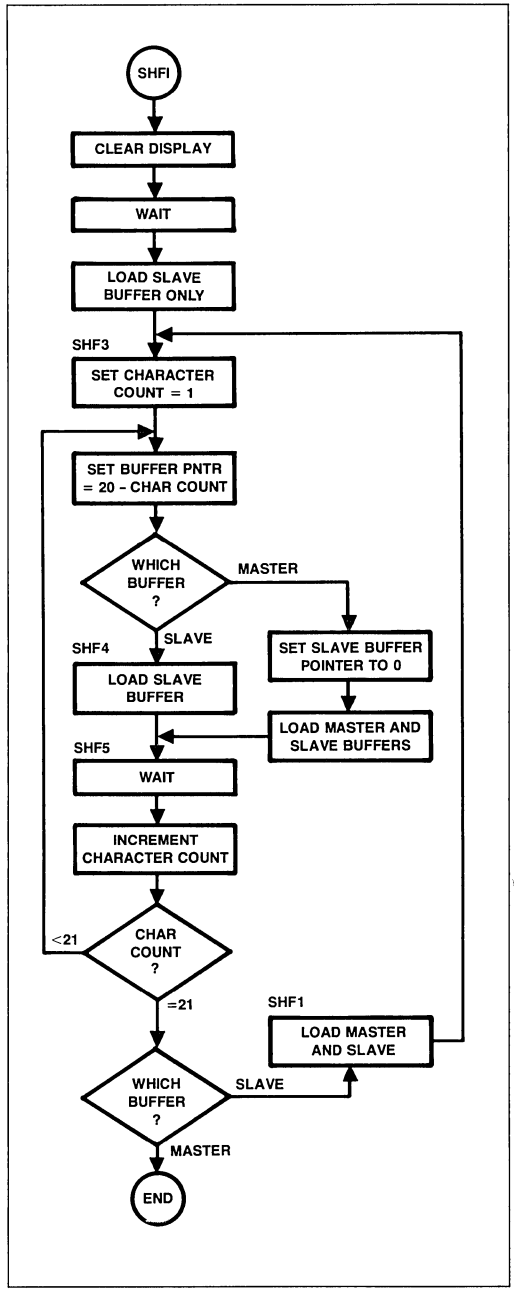
Message Scroll

The next three subroutines are used for scrolling messages across the display. SHFI clears the display then shifts in a message. SHFTO shifts a message across the display and ROTR is a loop which repeatedly rotates a message through the display. These routines may be used separately or combined to create various effects.

Scroll In A Message

SHFI blanks the display then shifts in a table message. The embedded transfers to delay loops are used to control the shifting speed.

```
        CLEAR DISPLAY
        SHIFT IN TABLE MESSAGE RIGHT TO LEFT
        EXIT WHEN MSD MASTER HOLDS FIRST
        CHARACTER OF TABLE

SHFI    JSR   POINT    SET UP TABLE POINTER
        JSR   BLNK     BLANK DISPLAY
        JSR   DELAY    WAIT

        LDA   #SLV     START WITH SLAVE ONLY
        BNE   SHF2
SHF1    LDA   #MRS     LOAD MASTER & SLAVE
SHF2    STA   HOLD

        LDA   #01      START WITH ONE DIGIT
        STA   KNT2     SAVE # OF DIGITS
SHF3    STA   KNTR

        SEC            SET BUFFER PNTR = 20 - #
                         DIGITS
        LDA   #$14
        SBC   KNT2
        ORA   #$C0
        JSR   CMND

        LDA   HOLD     HOLD DOUBLES AS A FLAG
        CMP   #MRS
        BNE   SHF4

        JSR   TOUT4    OUTPT TO MSTR & SLV
        JSR   SHFT2    ADD A SPACE IF END OF TABLE
        LDA   #MRS     SET UP FOR NEXT PASS
        STA   HOLD
        JMP   SHF5

SHF4    JSR   OUTT     OUTPT TO SLAVE ONLY
        JSR   SHFT2    ADD A SPACE IF END OF TABLE
SHF5    JSR   DELAY    WAIT

        INC   KNT2     ADD ANOTHER DIGIT
        LDA   KNT2
        CMP   #$15
        BNE   SHF3
        LDA   #SLV     BUFFER LOADED: WHICH ONE ?
        CMP   HOLD
        BEQ   SHF1     SLAVE LDED, ADD MSTR
        RTS            MSTR & SLV LOADED: EXIT
```

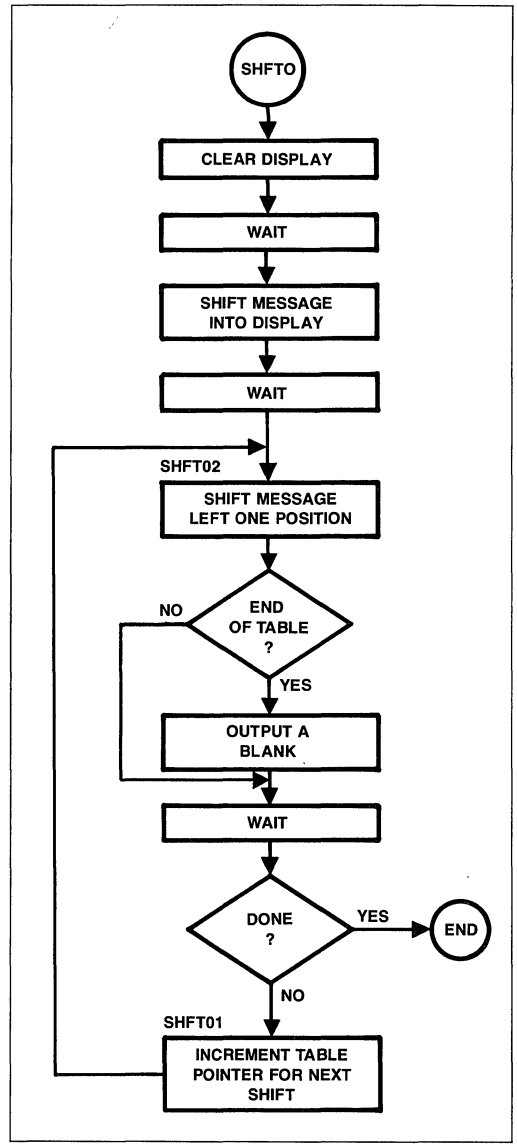


Flowchart: Display Clear and Message Shift In

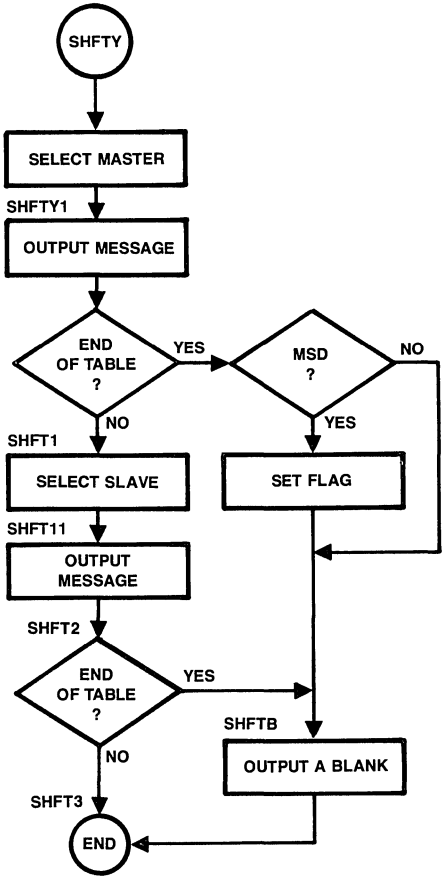
Scroll A Message Across the Display

SHFTO blanks the display, shifts in a table message then shifts the message out of the display while simultaneously shifting in blanks.

```
        SHIFT TABLE MESSAGE ACROSS DISPLAY

SHFTO   JSR  SHFI     BLANK DISPLAY, SHIFT IN MESSAGE
SHFTO2  JSR  SHFTY    SHIFT LEFT 1 DIGIT
        JSR  DELAY    WAIT
        BCC  SHFTO1
        RTS           DONE ON C=1

SHFTO1  INC  PNTR     ADJ PNTR 4 NEXT SHIFT
        BNE  SHFTO2
        INC  PNTR+1
        BCC  SHFTO2

        SHIFT TABLE MESSAGE LEFT ONE
        DIGIT. OUTPUT A BLANK IF END
        OF TABLE IS DETECTED.

SHFTY   LDY  #00      INITIALIZE POINTER OFFSET
        LDA  #MRS     SELECT MASTER
SHFTY1  JSR  TOUT7    OUTPUT MESSAGE
        LDA  KNTR     END OF TABLE ?
        BEQ  SHFT1    NO
        CMP  #$14     YES
        CLC
        BNE  SHFTB    SET C=1 IF END OF TABLE
        SEC           DETECTED AT MSD OF MASTER.
        BEQ  SHFTB    OUTPUT A BLANK

SHFT1   LDA  #SLV     SELECT SLAVE
SHFT11  JSR  TOUT7    OUTPUT MESSAGE
        CLC
SHFT2   LDA  KNTR     END OF TABLE ?
        BEQ  SHFT3    NO: EXIT

SHFTB   STA  TEMP     YES: SVE XIT CNTR VALUE
        LDA  #01      FOR ROTR THEN
        STA  KNTR     OUTPUT A BLANK
        LDA  #$20
        JSR  OUTC
SHFT3   RTS
```



Flowchart: Shift Message Across Display

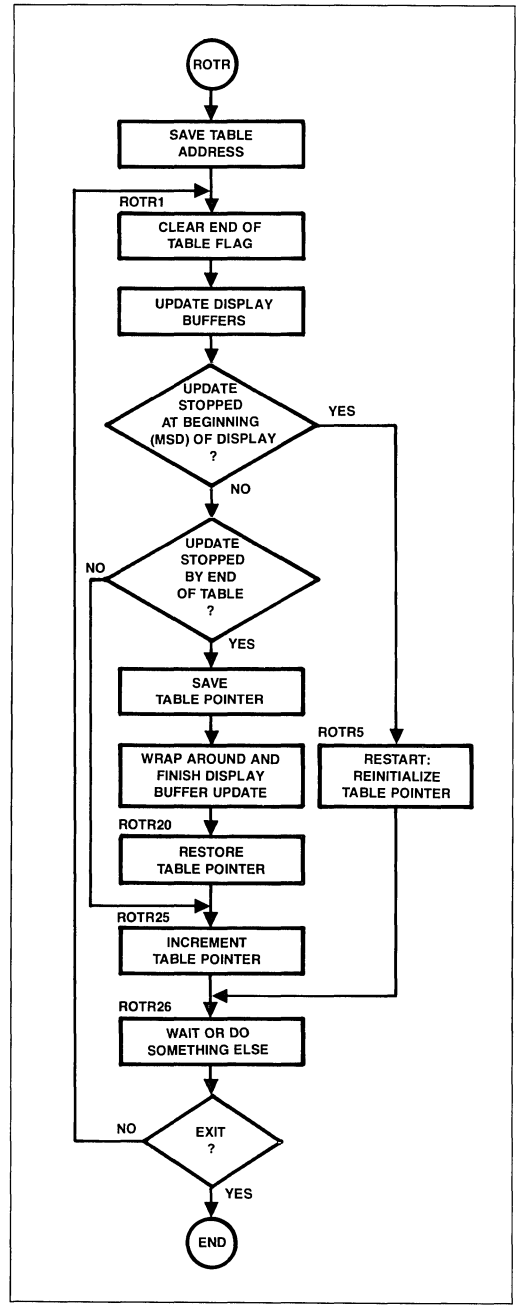


Flowchart: Shift Message Left One Position

Rotate A Message—Continuous Loop

ROTR rotates a message on the display.

```
        ROTATE A TABLE MESSAGE—CONTINUOUS LOOP
          MESSAGE MUST BE ≥ 20 CHARACTERS

ROTR    JSR  SHFI      SHIFT IN MESSAGE
        LDA  PNTR      SAVE TBL ADDRSS FOR WRAP
        STA  BPNT      AROUND
        LDA  PNTR+1
        STA  BPNT+1

ROTR1   LDA  #00       TEMP IS CNTR VALUE 4 WRAP
                         AROUND
        STA  TEMP      TEMP≠0=TBL END DETECTED
        JSR  SHFTY     SHIFT LEFT ONE DIGIT
        BCS  ROTR5     TBL END IN MSD DISP ?
        LDA  #00       NO: TABLE END DETECTED ?
        CMP  TEMP
        BEQ  ROTR25    NO

        LDA  PNTR      TABLE END: WRAP AROUND
        PHA            SAVE TAIL POINTER ON STACK
        LDA  PNTR+1
        PHA
        LDA  BPNT      FETCH 1ST BYTE PNTR
        STA  PNTR
        LDA  BPNT+1
        STA  PNTR+1
        DEC  TEMP      SHFTY ADDED BLNK: ADJ CNTR
        BNE  ROTR10
        LDA  #MRS      COUNT DONE—WHICH HALF ?
        CMP  HOLD
        BNE  ROTR20    LOWER: SET UP 4 NEXT SHIFT
        JSR  SHFT1     UPPER: DO LOWER
        JMP  ROTR20    SET UP 4 NEXT SHIFT

ROTR5   LDA  BPNT      TBL END IN MSD DISP
        STA  PNTR      RESET PNTR
        LDA  BPNT+1
        STA  PNTR+1
        JMP  ROTR26    DO NEXT SHIFT

ROTR10  LDA  TEMP      COUNT NOT DONE
        STA  KNTR      RESET COUNTER
        LDA  #MRS      WHICH HALF ?
        CMP  HOLD
        BNE  ROTR15
        JSR  TOUT4     UP: FINISH UP, DO LOW
        JMP  ROTR20

ROTR15  JSR  OUTT      LOWER: FINISH LOWER

ROTR20  PLA            RECLAIM TAIL POINTER
        STA  PNTR+1
        PLA
        STA  PNTR

ROTR25  INC  PNTR      INCREMENT TABLE
        BNE  ROTR26    POINTER FOR
        INC  PNTR+1    NEXT SHIFT

ROTR26  JSR  DELAY     WAIT

      [ADD EXIT SEQUENCE HERE]

        JMP  ROTR1     DO NEXT SHIFT
```



Flowchart: Rotate Message

For further product information, refer to the following documents:

Order Number	Document Title
D96	10938 and 10930 Dot Matrix Display Controller Data Sheet
D60	R6500/1EB Backpack Emulator Data Sheet
D51	R6500/1 One-Chip Microcomputer Data Sheet
D51S	R6500/1E Emulator Device Data Sheet Supplement
212	R6500/1 One-Chip Microcomputer Product Description
2175	Intelligent Display Controller Designer's Notes

Rockwell

Intelligent Display Controller Designer's Notes

by Terry Christensen and Tal Klaus,
Semiconductor Products Division, Newport Beach, California

DESCRIPTION

The Rockwell Intelligent Display Controller family of products is designed to interface host processors to various types of vacuum fluorescent displays. In addition to providing the display drive signals, these products perform character decoding, grid timing and display refresh functions. Included in the family are a series of single chip display controllers, a series of anode decoder/drivers and a grid controller/driver.

Figure 1 is a block diagram of the single chip display controller. The products of this series contain 18 anode drivers and 16 grid drivers. Commands and data are input through a serial data port. A 64 x 16-bit mask programmable PLA provides character decoding. A 16 x 8-bit data buffer holds character data. Commands for brightness control, data buffer control and test mode enable are available.

Two PLA patterns are provided as standard products. One, the 10937 provides ASCII to 16 segment decoding. The other, the 10951 provides 7 segment numeric and 16 segment bargraph decoding. Both of these products feature decimal point and tail control. Also available is the 10957 which is a 10937 modified to provide greater decimal and tail control.

The block diagram of Figure 2 shows a typical host and display interface for a single chip display controller.

Grid controller/drivers are combined with anode decoder/drivers to create multi-chip display controllers. As shown in the block diagram of Figure 3, the grid controller/driver (10939) accepts commands and data from the host system, sends data and timing information to the anode decoder/driver, and controls a cursor output in addition to controlling the display grids. Commands for brightness control, buffer control, and blank and inverse display modes are available. These commands and the character data may be input to the 10939 through either a serial or a parallel data port. Each 10939 can drive up to 20 grids and store the related character data for automatic refresh. With the synchronization logic provided, as many as four 10939's can be daisy chained together to drive 80 character displays as shown in Figure 4.

The anode decoder/driver can drive up to 35 anodes. Data input from the grid controller/driver are decoded in a 128 character mask

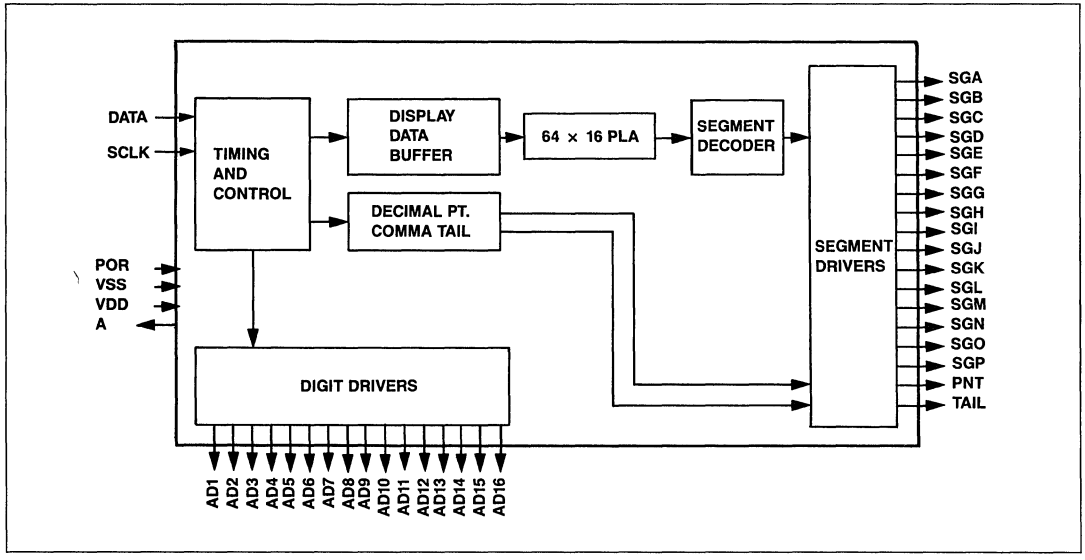


Figure 1. Single Chip Display Controller Block Diagram

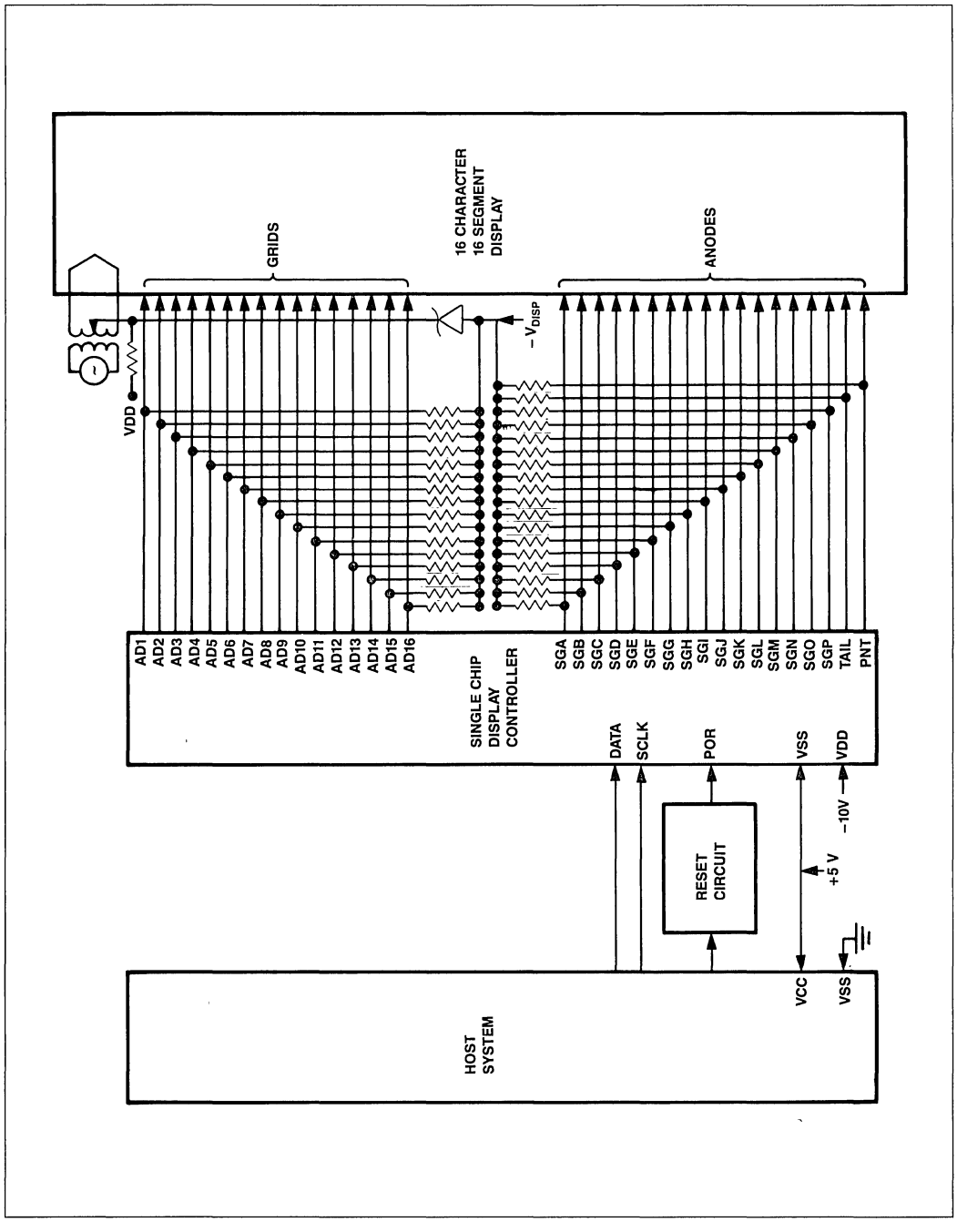


Figure 2: 16 Character 16 Segment Display Driven by Single-Chip Display Controller

6

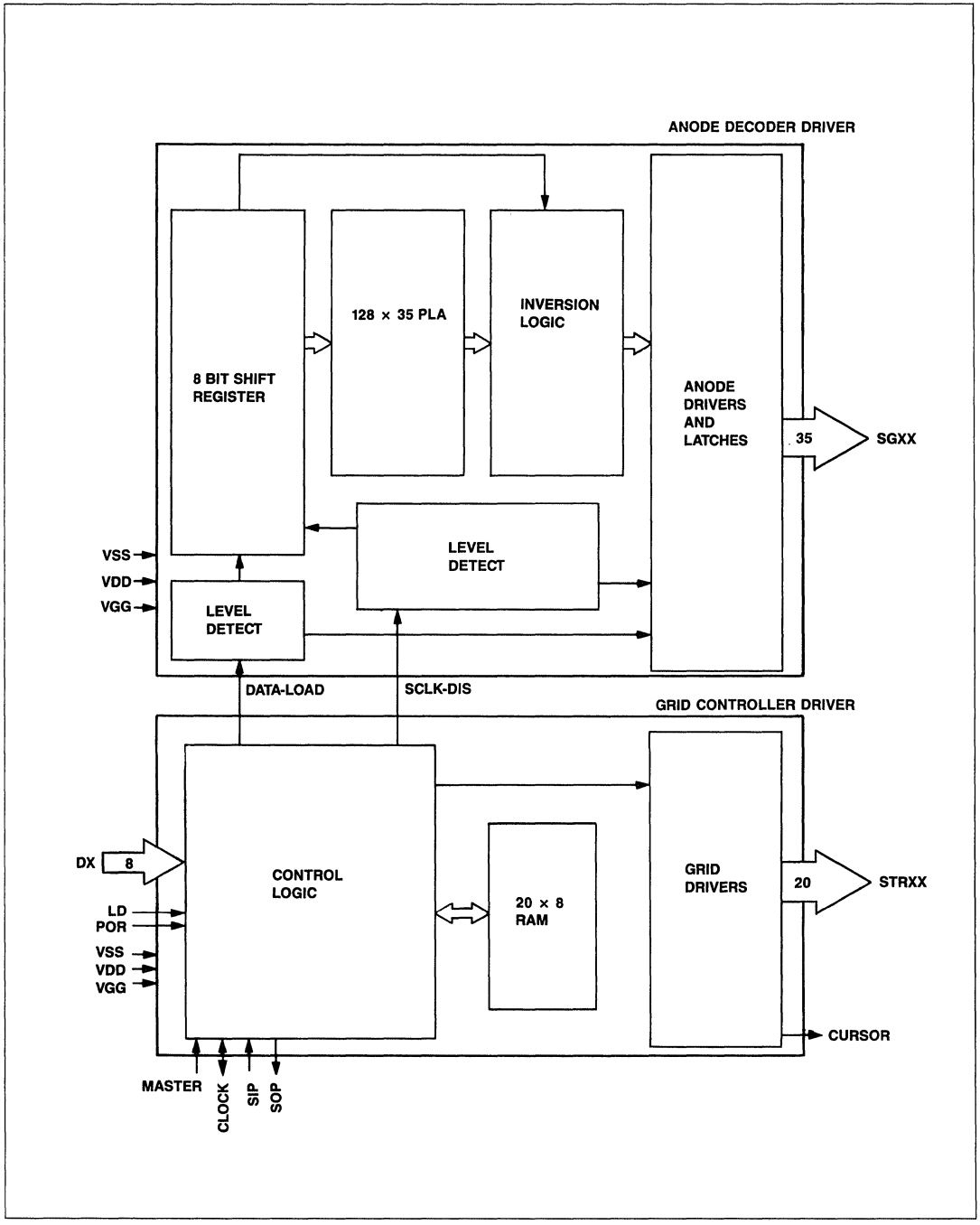


Figure 3. Multi-Chip Display Controller Block Diagram

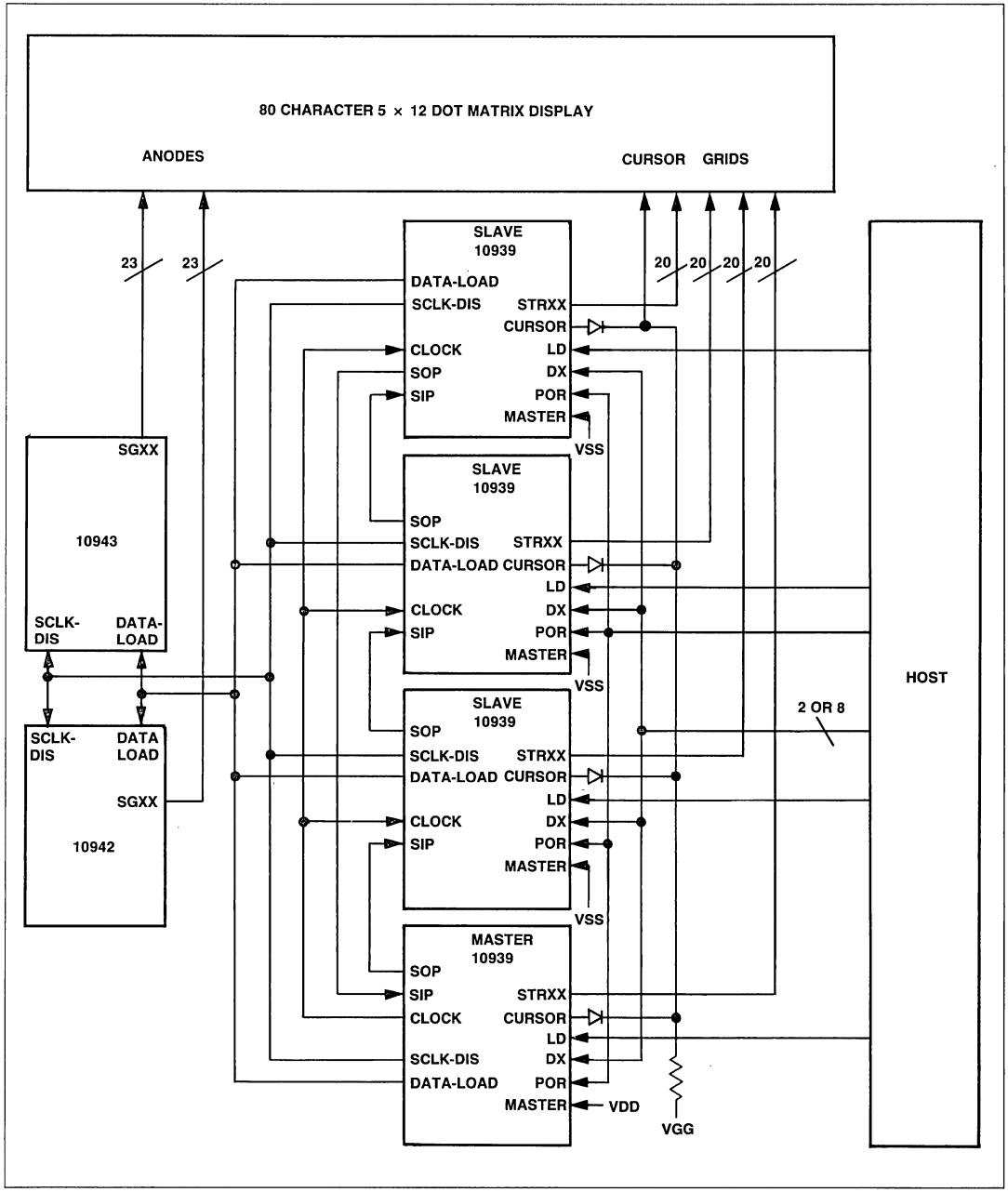


Figure 4. Block Diagram of 80 Character 5 x 12 Dot Matrix Display Driven by Multi-Chip Display Controller

programmable PLA to determine which anodes to activate. Several anode drivers may be driven as shown in Figure 4 to produce characters from more than 35 anodes.

Four PLA patterns are produced as standard products. The 10938 provides ASCII to 5 x 7 dot matrix decoding. The 10941 generates 16 segment ASCII and bargraph patterns. The 10942 and 10943 are used together to generate 5 x 12 dot matrix ASCII characters.

Tables 1 and 2 compare the features of the display controller products.

Typical applications for the intelligent display controller family include: automotive instrument clusters, interactive terminals, typewriters, telecommunications products, industrial automation, appliances, hand-held computers and instrumentation systems.

Although intended for vacuum fluorescent displays, users are finding these intelligent controllers are cost effective for use with gas discharge, LED and incandescent displays even though buffering is required.

By providing a simple interface both with the host computer and the associated display, the intelligent controller family provides significant advantages over other approaches. The benefits of Rockwell's intelligent display controller approach are: reduction of operating time required of the host computer, less display overhead electronics, simplified system design, less board real estate for the display control function, reduced power and cooling, lower overall installed cost and lower maintenance costs.

This can be seen from the following comparison. Several techniques can be used to drive a 20 character, 5 x 7 dot matrix, vacuum fluorescent display. One way is to use two 10-bit shift register latched drivers to drive the grids and five 8-bit latched drivers to drive the anodes as shown in Figure 5. This configuration uses 19 outputs from the host system for display control. The host system must perform the grid timing and character to dot conversion. Because of this, the host system must service the display every character cycle.

An efficient alternate method is to use the 10938/10939 chip set as shown in Figure 6. With this configuration, 4 or 10 outputs from the host system and a simple reset circuit are needed to drive the display controller. At initialization, the host loads operating parameters into the display controller. Then the display buffer is loaded with the ASCII code of the characters to be displayed. After that the host accesses the display controller only when display characters or operating parameters need to be changed. The display controller performs the grid timing and ASCII to dot conversion functions.

Table 1. Comparison of Single Chip Display Controller Features

Features	10937	10951	10957
PLA Size	64	64	64
Font	16 Segment Alphanumeric Decimal Point Comma	7 Segment Numeric Decimal Point Comma 16 Segment Bargraph	16 Segment Alphanumeric Decimal Point Comma
Anode Drivers			
Type	Open-Drain	Open-Drain	Open-Drain
Number	18	18	18
Current Limit (mA)	10	10	10
Grid Drivers			
Type	Open-Drain	Open-Drain	Open-Drain
Number	16	16	16
Current Limit (mA)	20	20	20
Host Interface	Serial	Serial	Serial
Control Options	Duty Cycle Character Count Buffer Pointer Test Mode	Duty Cycle Character Count Buffer Pointer Test Mode	Duty Cycle Character Count Buffer Pointer Test Mode
Power Supply Limits			
VDD(V)	−15 ± 1.5	−15 ± 1.5	−15 ± 1.5
VGG(V)	to −50	to −50	to −50
Package	40 Pin Dip	40 Pin Dip	40 Pin Dip
Other	2 Decimal and Tail Commands	2 Decimal and Tail Commands	4 Decimal and Tail Commands

Table 2. Comparison of Multi-Chip Display Controller Features

Features	Grid Drivers	Anode Drivers			
	10939	10938	10941	10942	10943
PLA Size		128	128	128	128
Font		5 x 7 Dot Matrix Alphanumeric	16 Segment Alphanumeric and Bargraph	Top Half 5 X 12 Dot Matrix Alphanumeric	Bottom Half 5 x 12 Dot Matrix Alphanumeric
Grid Drivers					
Type	Push-Pull				
Number	20				
Current Limit (mA)	10				
Anode Drivers					
Type		Push-Pull	Push-Pull	Push-Pull	Push-Pull
Number		35	18	23	23
Current Limit (mA)		2	2	2	2
Host Interface	Serial or Parallel	Via 10939	Via 10939	Via 10939	Via 10939
Control Options	Digit Time Duty Cycle Character Count Buffer Pointer Blank Mode Inverse Mode Start Refresh				
Power Supply Limits					
VDD(V)	−20±2.0	−20±2.0	−20±2.0	−20±2.0	−20±2.0
VGG(V)	to −50	to −50	to −50	to −50	to −50
Package	40 Pin Dip	40 Pin Dip	24 Pin Dip	28 Pin Dip	28 Pin Dip
Other	Cursor Driver Cascadable		Decimal Point Driver Comma Driver		

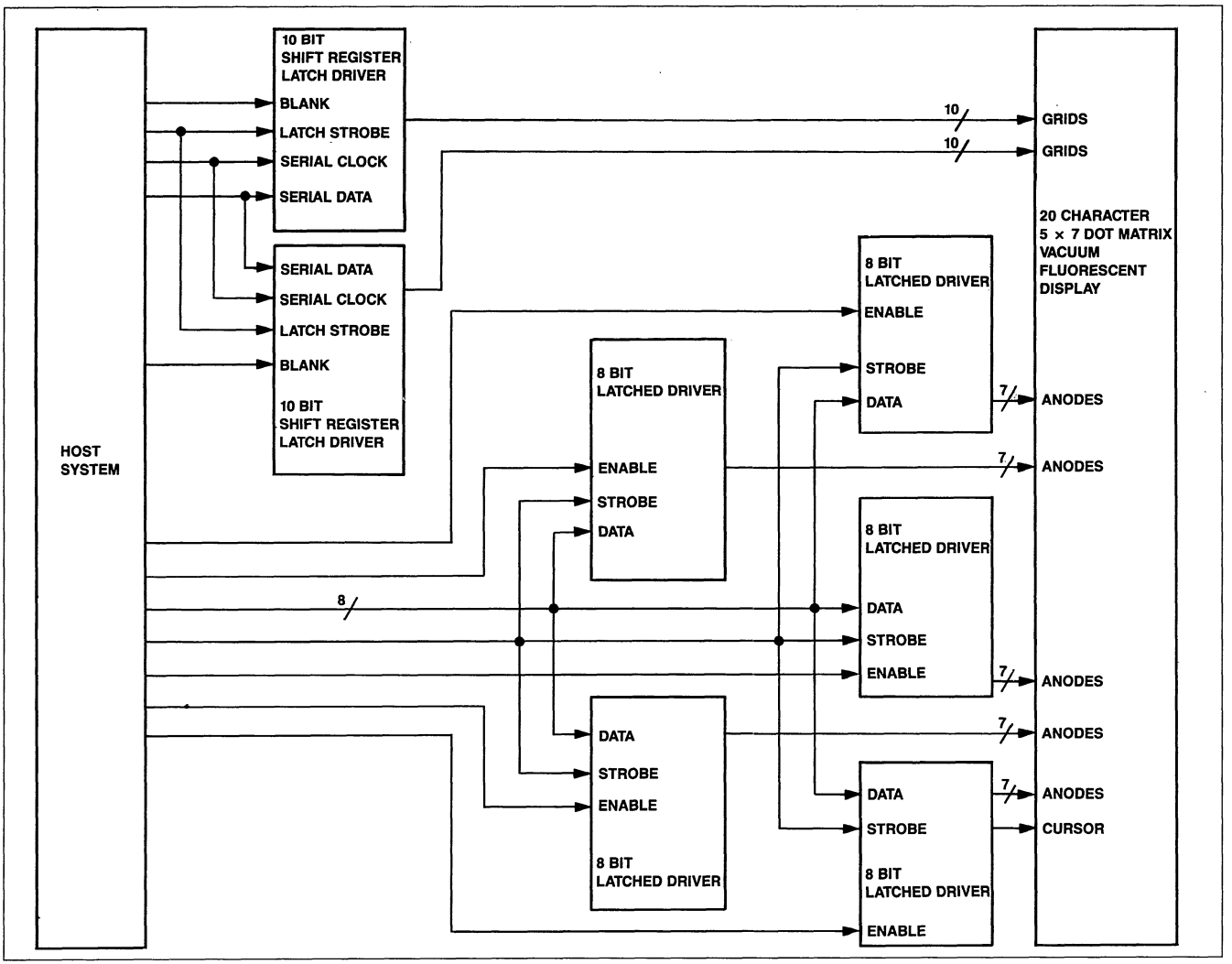


Figure 5. 20 Character 5 x 7 Dot Matrix Display Driven by Latched Drivers

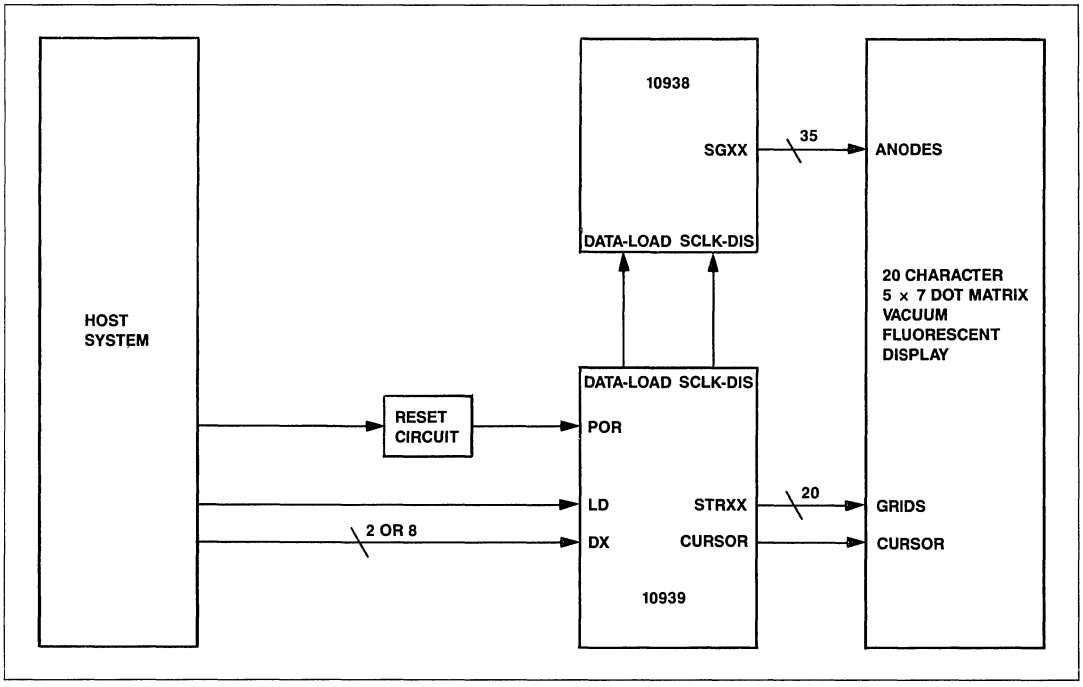


Figure 6. 20 Character 5 x 7 Dot Matrix Display Driven by Multi-Chip Display Controller

HOST-DISPLAY CONTROLLER INTERFACE

These devices contain circuitry to protect the inputs against damage due to high static voltages. However, it is advised that normal precautions be taken to avoid application of any voltage beyond the maximum rated limits. All inputs are TTL compatible although pullup (to VSS) resistors may be required in certain applications.

CONTROL OF SINGLE CHIP DISPLAY CONTROLLERS

Commands and display data are clocked into the single chip display controller from the host serially with the DATA and SCLK inputs. Input data is shifted in as serial bytes, MSB first. Each bit is latched in on the falling edge of the SCLK pulse. The SCLK signal must remain high from one to 20 μs and low at least one μs for each bit. There must be a 40 μs gap, with SCLK held low, between each byte. It is recommended that the display controller be reset periodically to assure bit synchronization. Figure 7 contains a summary of the data transfer timing requirements and a flow chart of the data transfer procedure.

The MSB of the input byte is called the control bit. The state of this bit determines the function of the input data. If the control bit is a one, the input data is a command or control word. If the control bit is a zero, the input byte is display data.

The single chip display controller recognizes four types of commands which are summarized in Table 3. The Buffer Pointer Control command sets the display data buffer pointer to the desired digit position. This enables easy modification of any individual character. When the command is executed, the buffer pointer is loaded with two less than the value of the controlling strobe line. Thus, to set the buffer pointer to the anode data for the character controlled by AD8, the command $A6_{16}$ is sent to the display controller.

The Digit Counter Control command sets the number of strobe lines to be activated on the display controller. It is normally used during initialization to define the number of characters to be controlled. In some cases it may also be used to adjust display brightness. This is discussed in the section describing display control techniques. The four least significant bits of the command byte determine the number of strobes to be activated. A command code of $C0_{16}$ enables all 16 strobes. Otherwise, the number in the lower half of the command is the number of active digits.

Display brightness and display on/off are controlled by the Duty Cycle Control command. The internal clock of the display controller runs at 100 KHz $\pm$50%. 32 clock cycles are allotted each active strobe. One of these 32 cycles is an inter-digit off time.

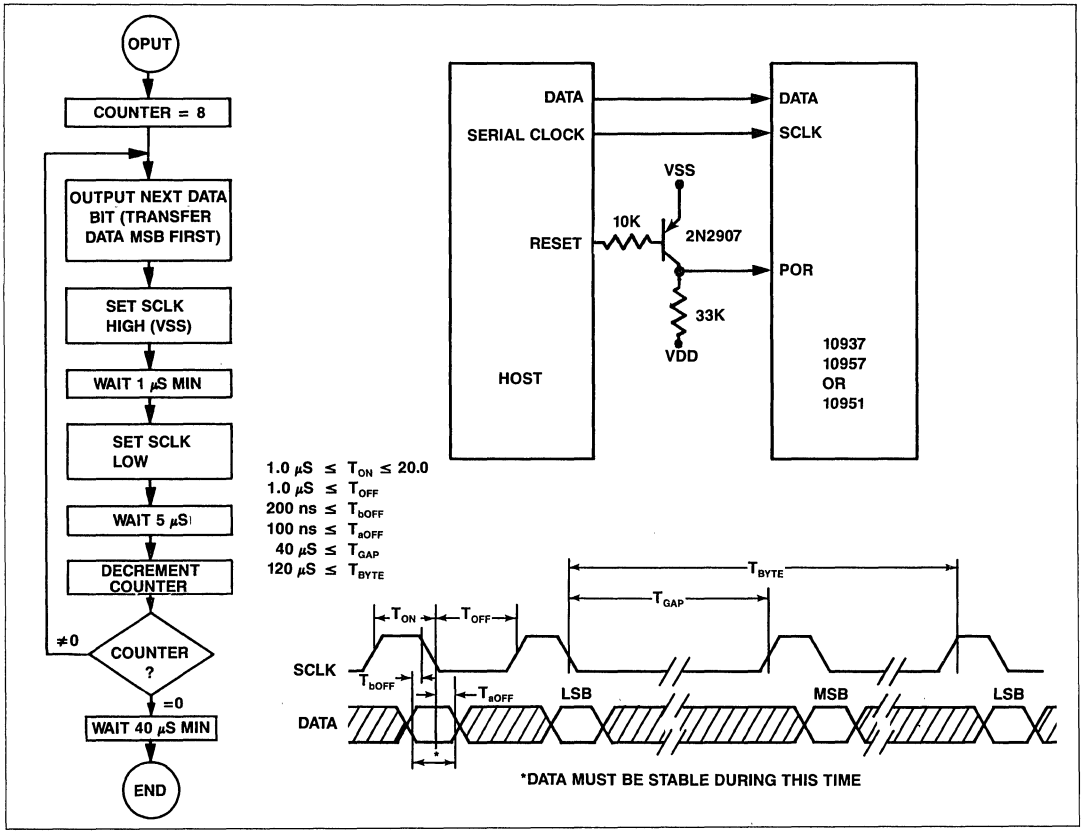


Figure 7. Data Transfer to Single-Chip Display Controller

The Duty Cycle Control command is used to select the number of the remaining 31 clock cycles a strobe is on. The number of "on" cycles is the five least significant bits of the command byte.

The fourth command type is a Test Mode Enable. When this mode is activated, the digit time is reduced from 32 to 4 clock cycles. After the test mode has been entered, a power-on reset sequence must be performed to resume normal operation.

CONTROL OF MULTI-CHIP DISPLAY CONTROLLERS

In systems using the multi-chip display controller, commands and display data are sent from the host to the 10939(s) through the data (D0-D7) and LD lines. Either a parallel or a serial data input mode may be used.

The parallel data input mode is implemented by toggling any of data lines D2-D7 after POR has gone low. Once the parallel data load mode has been implemented, a power-on reset procedure must be performed to return to serial data load mode. Parallel data transfer is accomplished, as shown in Figure 8, by putting the command or display data on the data lines, then pulsing the LD line. The load cycle time must be at least 60 μs with the LD line set high for at least one μs and held low for at least 40 μs.

The serial data input mode is implemented during the power-on reset procedure. In those systems using serial mode, ports D2-D7 should be tied low to prevent the inadvertent implementation of the parallel load mode. Serial data bytes are shifted into a data buffer MSB first on line D0 using line D1 as the serial clock. The last eight bits clocked in are latched into the display controller by a pulse on the LD line. As shown in Figure 9, the cycle time for each data bit is 2 μs and the load time for each byte is 60 μs.

The 10939's may be cascaded together to drive displays having more than 20 characters. As many as four 10939's can be daisy chained as shown in Figures 4 and 14 to control up to 80 characters.

Each 10939 has its own on-chip oscillator and a clock generator operating at approximately 100 kHz. When more than one 10939 is used in a system, the same clock must be used for all the

Table 3. Single Chip Command Summary

Control Word Assignment

Hex Code	Function
80-9F	Enter Test Mode
A0-AF	Load Buffer Pointer
C0-CF	Load Digit Counter
E0-FF	Load Duty Cycle

Duty Cycle Control Codes

Hex Code	On Cycles	Off Cycles
E0	0	32
E1	1	31
E2	2	30
E3	3	29
E4	4	28
E5	5	27
E6	6	26
E7	7	25
E8	8	24
E9	9	23
EA	10	22
EB	11	21
EC	12	20
ED	13	19
EE	14	18
EF	15	17
F0	16	16
F1	17	15
F2	18	14
F3	19	13
F4	20	12
F5	21	11
F6	22	10
F7	23	9
F8	24	8
F9	25	7
FA	26	6
FB	27	5
FC	28	4
FD	29	3
FE	30	2
FF	31	1

Digit Counter Control Codes

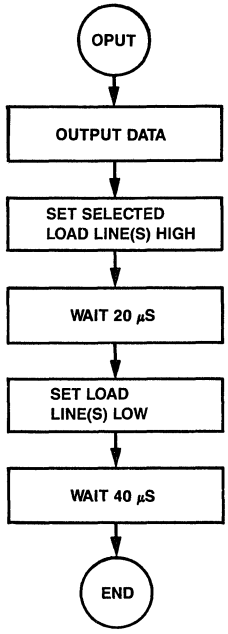
Hex Code	Hex Digit Counter Value	Number of Digits Controlled
C0	0	16
C1	1	1
C2	2	2
C3	3	3
C4	4	4
C5	5	5
C6	6	6
C7	7	7
C8	8	8
C9	9	9
CA	A	10
CB	B	11
CC	C	12
CD	D	13
CE	E	14
CF	F	15

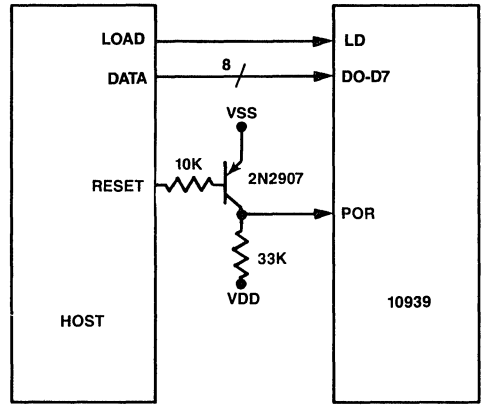
Buffer Pointer Control Codes

Hex Code	Pointer Value	Character Controlled By
A0	0	AD2
A1	1	AD3
A2	2	AD4
A3	3	AD5
A4	4	AD6
A5	5	AD7
A6	6	AD8
A7	7	AD9
A8	8	AD10
A9	9	AD11
AA	10	AD12
AB	11	AD13
AC	12	AD14
AD	13	AD15
AE	14	AD16
AF	15	AD1

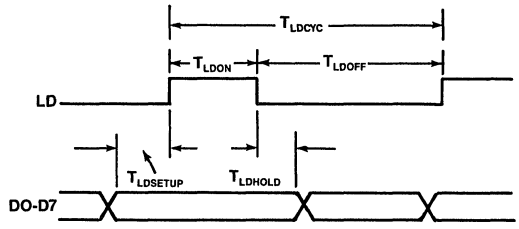
devices. To do this, one 10939 is designated the master by connecting its MASTER pin to VDD. This activates the oscillator on that device and causes a three-level four-state signal to be output on the CLOCK pin. The MASTER pin on the remaining, i.e., slave, devices is connected to VSS. This deactivates the oscillators on these devices so that the master's CLOCK output can be input on the slaves' CLOCK pins.

A two line synchronization port (SOP and SIP) ensures that only one 10939 device at a time drives the display. When one 10939 outputs its last character, it emits a pulse on its SOP. The next 10939 receives this pulse on its SIP input and starts its display cycle. This sequence continues through all of the 10939's in a chain. The SOP of the last 10939 is connected back to the SIP of the first 10939 to start another cycle. The limit to the number of 10939's in the chain is determined by: 1) the load on the clock output of the master 10939, and 2) the display refresh requirements. The synchronization signal propagates during the last character time of its own 10939 and thus does not require any extra time before the first character of the next 10939. The duty cycles of all the 10939's in the chain must be the same.





PARALLEL INTERFACE TIMING WAVEFORMS



40 μSEC* ≤ T_{LDOFF}
1 μSEC ≤ T_{LDON}
0 ≤ $T_{LDSETUP}$
1 μSEC ≤ T_{LDHOLD}
60 μSEC* ≤ T_{LDCYC}

*FOR INDUSTRIAL RATED PARTS SUBSTITUTE 44.5 FOR 40
66.7 FOR 60

Figure 8. Parallel Data Transfer to 10939

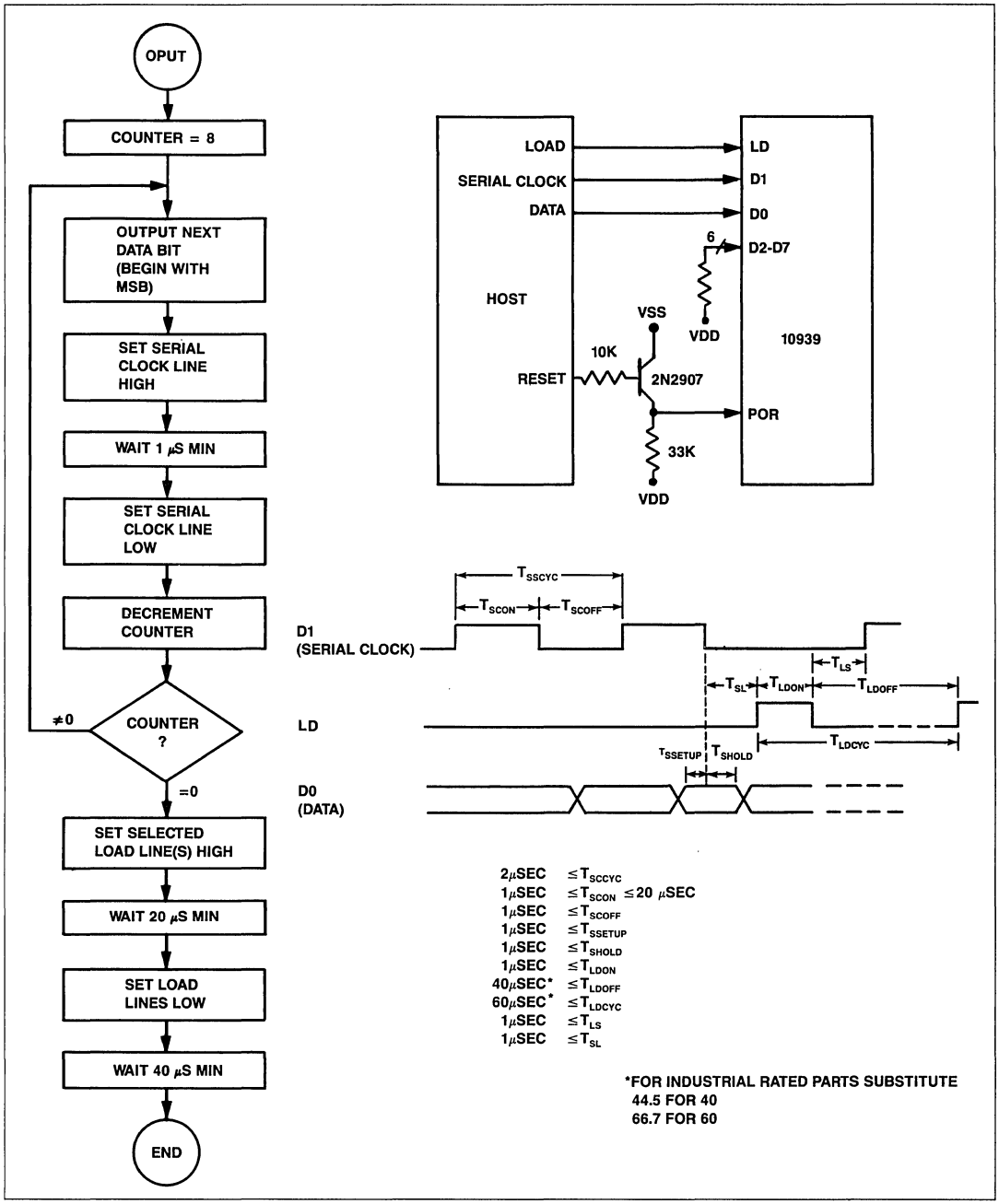


Figure 9. Serial Data Transfer to 10939

The data pattern 01_{16} is a control prefix byte. When this byte is transmitted to a 10939, it indicates that the next byte is a command. Several command types, listed in Table 4 are recognized by the 10939.

One of these, the Digit Time Select, determines the amount of time allotted to each character during the refresh cycle. Three options are available. These are 16, 32 or 64 half clock cycles per character. A clock cycle is one cycle of the internal clock of the master 10939 of the system.

The Duty Cycle Select is another command type. This determines the number of clock cycles a digit driver is on during its character time. Three half clock cycles of each character time are used as an inter-digit off time so the selectable duty cycle range is zero to digit time minus three.

A third command type is the Digit Count Select. This determines the number of character positions to be controlled. Note that a digit count greater than the actual number of characters can be selected. This is a feature that can be used to extend the display cycle time and thus expand the range of brightness control since adding phantom characters causes a proportionate reduction of display brightness.

The 10939 contains a 20 character data buffer which holds the anode data for each digit. A buffer pointer, which can be set on command, allows direct access to the data for each character.

The multi-chip display controllers may be operated in three command selectable display modes. These are the normal, inverse and blank modes. When the inverse mode is enabled, selected characters will be inverted. The anodes that would be enabled in normal mode are disabled and the anodes that would be disabled in normal mode are enabled. When the blank mode is enabled, selected characters will be blanked.

The MSB of the data byte is a control bit which determines which characters are selected for a particular display mode. Characters for which this bit is a zero will be displayed in the normal mode.

The data byte control bit also controls the cursor output. The cursor output will be enabled on all characters with the MSB equal to one. So when normal mode is enabled and the MSB of the data byte is set, the normal character will be displayed with the cursor on. When blank mode is enabled and the MSB equals one, the character will be blanked and the cursor will be on.

Two commands remain. One is the Start Refresh Command. At power on, 10939s are placed in an internal halt mode. The normal display refresh sequence starts when a master 10939 receives this start refresh command.

The final command is the command to load 01_{16} into the data buffer. This byte signifies that a command follows. When the command is also 01_{16}, it means that 01_{16} is data.

Display data and timing (Figure 10) are output to the anode decoder/driver via a two line serial port consisting of the SCLK-DIS and DATA-LOAD PINS. In order to minimize the number of package pins, these outputs are multiplexed, three-level, four-state drivers.

The SCLK-DIS signal is composed of the shift clock which shifts new data into the anode decoder/driver and a disable signal which sets all of the anode drivers to the display off state. The DATA-LOAD signal is composed of serial 8-bit data and a load signal to transfer the new data from the 10938 input buffer through the PLA to the display driver outputs. The data is output with the most significant bit first.

The anode decoder/driver devices can drive a maximum of 35 anodes. For displays having more than 35 anodes per character, such as the 5×12 dot matrix example of Figure 4, two or more anode decoder/drivers may be connected in parallel.

POWER-ON RESET AND INITIALIZATION

The power-on reset (POR) input controls the initialization of the internal circuits of the display controllers. Chip reset is achieved by setting the POR input high (VSS), waiting a minimum of 100 μs then setting the POR input low. After another delay of at least 100 μs, commands and data may be sent to the display controllers. On a cold start, POR should be held high for at least 100 μs after VDD stabilizes. Figure 11 contains examples of circuits that can be used to control this input while Figure 12 contains cold start timing diagrams.

A power-on reset establishes the following default conditions on the single chip display controllers:

a. The grid drivers (ADXX) are off (floating).
b. The anode drivers (SGX, PNT, TAIL) are off (floating).
c. Duty cycle is set to zero.
d. Digit Count is set to 16.
e. The buffer pointer selects the character controlled by AD1.
f. The display data buffer is filled with zeros.

When performing chip initialization it is recommended that a sequence such as that of Figure 13 be followed. In this sequence, the digit count is adjusted and the display data buffer is loaded before the duty cycle is set. This prevents the flashing of random data on the display.

A power-on reset establishes the following default conditions on the multi-chip display controller.

a. The Grid Drivers (STRXX) are off.
b. Duty Cycle is set to zero.
c. Digit Count is set to 32.
d. The Buffer Pointer is set to zero.
e. Digit Time is set to 64 cycles per character.
f. Normal display mode is selected.
g. The DATA-LOAD output is set to the high impedance state.
h. SCLK-DIS is set to Vol to disable the anode drivers. When the POR signal is removed, SCLK-DIS is set to the high impedance state.
i. SOP is set to Vol to disable the synchronization pulse.
j. The 10939(s) is (are) placed in an internal halt mode. This allows the host system to load the control registers and the data buffer without flashing "garbage" on the display. The normal display refresh sequence is started upon receipt of a START REFRESH control code. Only the master 10939 in a multi-chip system will recognize the START REFRESH code. The slave(s) will be started by the master at the appropriate time, using the SOP signal.

Table 4. Multi-Chip Command Summary

Control Word Assignments

Hex Code	Function
01	Load 01 into Data Buffer
05	Set digit time to 16 cycles per grid
06	Set digit time to 32 cycles per grid
07	Set digit time to 64 cycles per grid
08	Enable Normal Display Mode (MSB in data words is ignored)
09	Enable Blank Mode (data words with MSB = 1 will be blanked)
0A	Enable Inverse Mode (data words with MSB = 1 will be "inversed")
0E	Start Display Refresh Cycle (use only once after reset)
40-7F	Load Duty Cycle Register with lower 6 bits (0-63)
80-9F	Load Digit Counter (80 = 32, 81 = 1, 82 = 2, etc.)
C0-DF	Load Buffer Pointer Register with lower 5 bits

Duty Cycle Control Codes

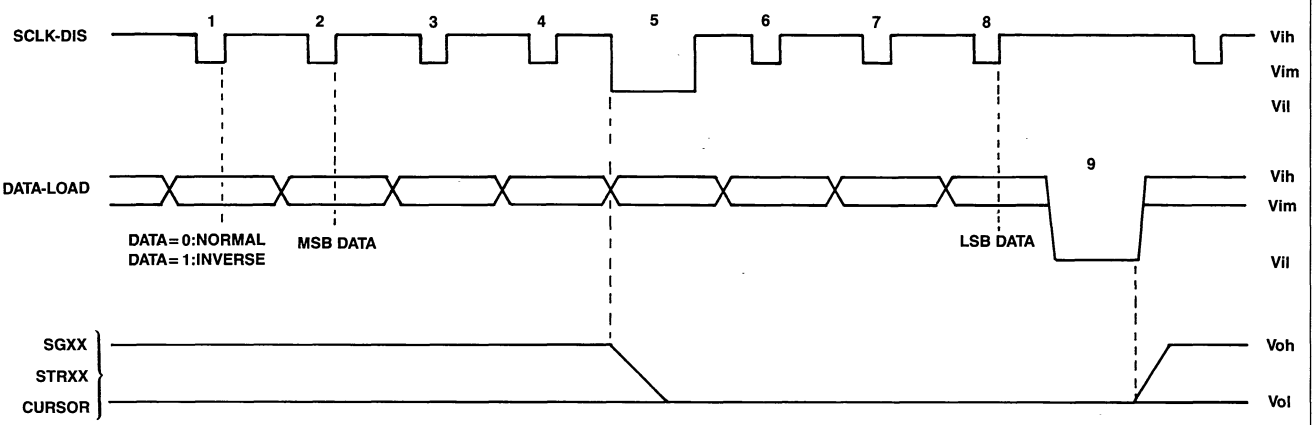
Hex Code	Digit Time = 16		Digit Time = 32		Digit Time = 64	
	On	Off	On	Off	On	Off
40	—	16	—	32	—	64
41	—	16	—	32	—	64
42	—	16	—	32	—	64
43	1	15	1	31	1	63
44	2	14	2	30	2	62
45	3	13	3	29	3	61
46	4	12	4	28	4	60
47	5	11	5	27	5	59
48	6	10	6	26	6	58
49	7	9	7	25	7	57
4A	8	8	8	24	8	56
4B	9	7	9	23	9	55
4C	10	6	10	22	10	54
4D	11	5	11	21	11	53
4E	12	4	12	20	12	52
4F	13	3	13	19	13	51
50	13	3	14	18	14	50
51	"	"	15	17	15	49
.	.	.	.	.	.	.
.	.	.	.	.	.	.
.	.	.	.	.	.	.
5D	"	"	27	5	27	37
5E	"	"	28	4	28	36
5F	"	"	29	3	29	35
60	"	"	29	3	30	34
61	"	"	"	"	31	33
.	.	.	.	.	.	.
.	.	.	.	.	.	.
.	.	.	.	.	.	.
7C	"	"	"	"	58	6
7D	"	"	"	"	59	5
7E	"	"	"	"	60	4
7F	"	"	"	"	61	3

Digit Counter Control Codes

Hex Code	Digit Counter Value	No. of Grids Controlled
80	00	32
81	01	1
82	02	2
83	03	3
84	04	4
85	05	5
86	06	6
87	07	7
88	08	8
89	09	9
8A	0A	10
8B	0B	11
8C	0C	12
8D	0D	13
8E	0E	14
8F	0F	15
90	10	16
91	11	17
92	12	18
93	13	19
94	14	20
95	15	21
96	16	22
97	17	23
98	18	24
99	19	25
9A	1A	26
9B	1B	27
9C	1C	28
9D	1D	29
9E	1E	30
9F	1F	31

Buffer Pointer Control Codes

Hex Code	Pointer Value	Character Controlled By
C0	00	STR00
C1	01	STR01
C2	02	STR02
C3	03	STR03
C4	04	STR04
C5	05	STR05
C6	06	STR06
C7	07	STR07
C8	08	STR08
C9	09	STR09
CA	0A	STR10
CB	0B	STR11
CC	0C	STR12
CD	0D	STR13
CE	0E	STR14
CF	0F	STR15
D0	10	STR16
D1	11	STR17
D2	12	STR18
D3	13	STR19



SHIFT PULSES ARE MARKED 1 THROUGH 8. DATA IS LATCHED ON THE POSITIVE TRANSITION OF SCLK-DIS. IF THE DATA INPUT DURING CLOCK PULSE 1 IS A LOGIC 1, THE SEGMENT OUTPUTS ARE COMPLEMENTED TO PROVIDE AN INVERSE CHARACTER. THE MOST SIGNIFICANT BIT OF THE CHARACTER CODE IS INPUT DURING CLOCK PULSE 2 AND THE LEAST SIGNIFICANT BIT DURING CLOCK PULSE 8.

THE DRIVERS ARE DISABLED AFTER THE NEGATIVE TRANSITION (Vih to Vil) OF THE DISABLE PULSE (CLOCK PULSE 5 IN THE EXAMPLE). THE DRIVERS CHANGE TO THEIR NEW VALUES AFTER THE POSITVE TRANSITION OF THE LOAD PULSE (MARKED 9).

Figure 10. Data Transfer from Grid Driver to Anode Driver

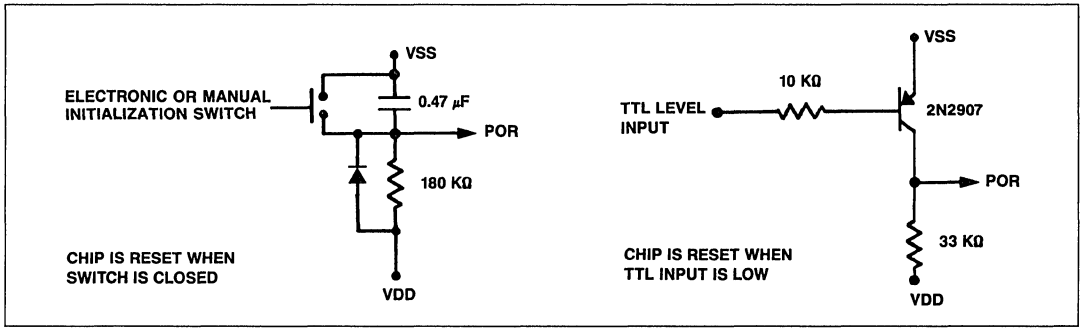


Figure 11. Power On/Reset Control Circuits

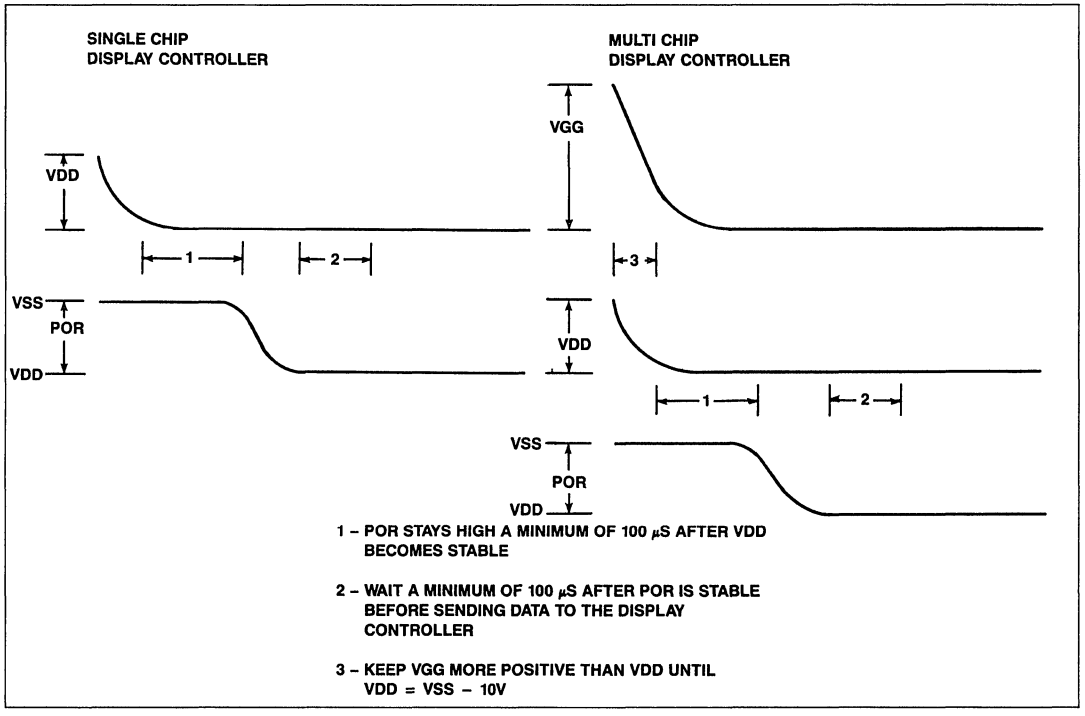


Figure 12. Power On/Reset Timing

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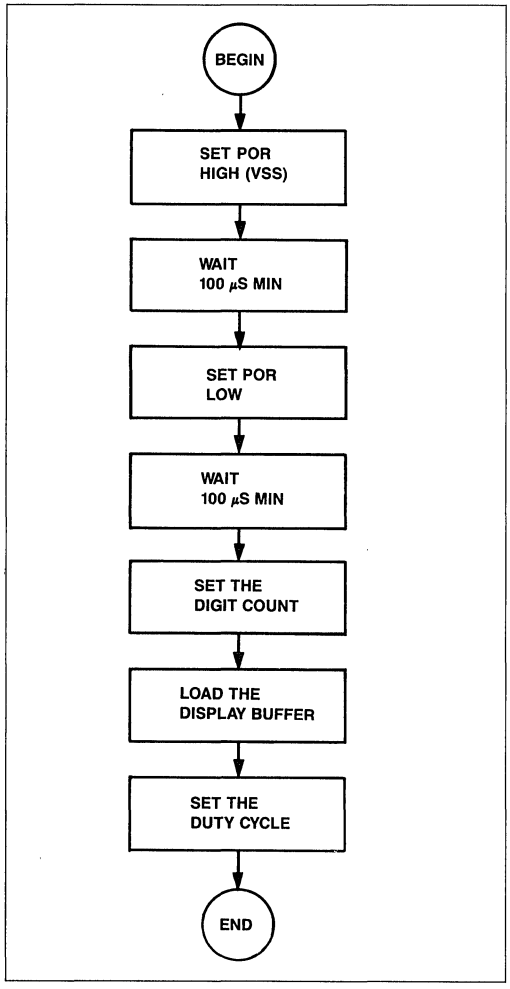


Figure 13. Single Chip Display Controller Initialization

Figure 14 is an example of an initialization sequence for the multi-chip display controller. In systems using parallel data loading, one or more of data lines D2 through D7 should be toggled before sending data to the 10939. Digit time should be set before the duty cycle is selected. To prevent the flashing of random data on the display, the display data buffer should be loaded before the start refresh cycle command is given.

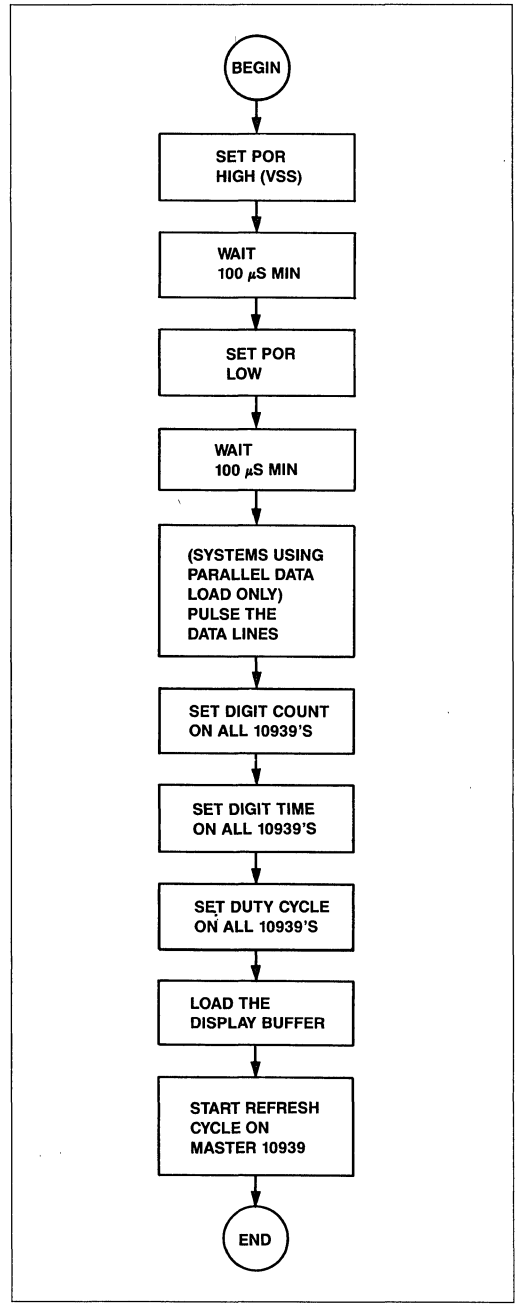


Figure 14. Multi-Chip Display Controller Initialization

CONTROLLER DISPLAY INTERFACE

DISPLAY INTERFACE OF SINGLE CHIP DISPLAY CONTROLLER

The single chip display controllers can drive up to 16 digits and 18 segments. These are open drain drivers so external pull down resistors must be supplied. The total capacitance on an output and the display duty cycle determine the resistor values to use. To prevent ghosting, the RC time constant of an output must be less than the interdigit off time. However, the resistor value should be as large as possible to maximize the portion of the driver current going to the display. Thus $R \leq T_{off}/C_{eff}$, where T_{off} is the interdigit off time and C_{eff} is the total capacitance on the driver. For VF displays, this value is usually between 30 kΩ and 50 kΩ.

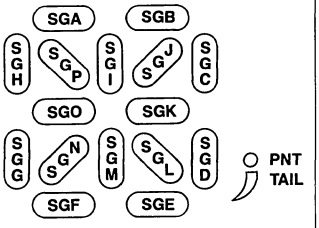
Each segment driver can source up to 10 mA and each digit driver can source up to 20 mA. Operating the chips beyond these limits can reduce chip life time. Both 40 and 50 volt versions of the single chip display controller are available as standard products.

Two PLA patterns are offered as standard products. One of them, part number 10937, displays 16 segment upper case ASCII characters plus decimal and tail. It can also be used for 14 segment ASCII and 7 segment numeric displays. The 14 and 16 segment driver assignments and character patterns are listed in Tables 5 and 6. Part number 10951 generates 7 segment numeric and 16 segment bargraph codes. Tables 7 and 8 contain the segment assignments and patterns generated by this device.

Table 5. 16 Segment PLA Patterns

Input Data	Character	Input Data	Character	Input Data	Character	Input Data	Character	Input Data	Character	Input Data	Character	Input Data	Character	Input Data	Character
00		08		10		18		20		28		30		38	
01		09		11		19		21		29		31		39	
02		0A		12		1A		22		2A		32		3A	
03		0B		13		1B		23		2B		33		3B	
04		0C		14		1C		24		2C	;	34		3C	
05		0D		15		1D		25		2D	–	35		3D	
06		0E		16		1E		26		2E	.	36		3E	
07		0F		17		1F		27		2F	/	37		3F	

Bit 7 of the data byte is a don't care
Table input data is for bit 7 equal to zero

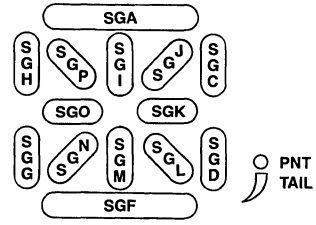


10937 Driver Assignments

Table 6. 14 Segment PLA Patterns

Input Data	Character	Input Data	Character	Input Data	Character	Input Data	Character	Input Data	Character	Input Data	Character	Input Data	Character	Input Data	Character
00		08		10		18		20		28		30		38	
01		09		11		19		21		29		31		39	
02		0A		12		1A		22		2A		32		3A	
03		0B		13		1B		23		2B		33		3B	
04		0C		14		1C		24		2C	;	34		3C	
05		0D		15		1D		25		2D	– –	35		3D	– –
06		0E		16		1E		26		2E	.	36		3E	
07		0F		17		1F		27		2F		37		3F	

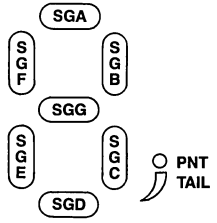
Bit 7 of the data byte is a don't care
Table input data is for bit 7 equal to zero



10937 Driver Assignments

Table 7. 7 Segment PLA Patterns

Input Data	Character	Input Data	Character	Input Data	Character	Input Data	Character
20	[1]	28	[1]	30	[2]	38	[2]
21	[1]	29	[1]	31	[2]	39	[2]
22	[1]	2A	[2]	32	[2]	3A	[2]
23	[1]	2B	[2]	33	[2]	3B	[2]
24	[1]	2C	;	34	[2]	3C	[2]
25	[1]	2D	[1]	35	[2]	3D	[2]
26	[1]	2E	.	36	[2]	3E	[2]
27	[1]	2F	[2]	37	[2]	3F	[2]



10951 Driver Assignments

Bit 7 of the data byte is a don't care
Table input data is for bit 7 equal to zero

[1]Segment drivers SGH, SGI, SGJ, SGK, SGL are enabled when these codes are used.
[2]Segment drivers SGM, SGN, SGO, SGP are enabled when these codes are used.

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Table 8. 16 Segment Bargraph Patterns

Input Data	Character	Input Data	Character	Input Data	Character	Input Data	Character
00		08		10		18	
01		09		11		19	
02		0A		12		1A	
03		0B		13		1B	
04		0C		14		1C	
05		0D		15		1D	
06		0E		16		1E	
07		0F		17		1F	

Bit 7 of the data byte is a don't care
Table input data is for bit 7 equal to zero

10951 Driver Assignments

A modified version of the 10937, part number 10957, offers expanded decimal and comma control. To provide this, two of the 10937 data codes have been redefined. Table 9 lists the unique 10957 codes and compares the 10957 with the 10937.

The single chip display controllers were not designed for paralleled or cascaded operation. The multi-chip display controller should be used for displays having more than 16 digits or more than 18 segments per character.

Table 9. Comparison of 10957 with 10937

Input Data	10937 Character	10957 Character
2C	;	;
2E	.	.
6C	;	,
6E	.	

DISPLAY INTERFACE OF MULTI-CHIP DISPLAY CONTROLLERS

Multi-chip display controllers are constructed from various combinations of anode decoder/drivers and grid controller/drivers.

The anode decoder/drivers can each drive a maximum of 35 dots or segments. Each driver can carry a 2 mA load and no external pull downs are required. The devices may be driven in parallel to generate patterns of more than 35 dots. An example of this is the 5 ×12 dot matrix block diagram of Figure 4.

Display data codes and timing information are sent from a 10939 or other source to the anode decoder/drivers serially on the DATA-LOAD and SCLK-DIS lines. An on-board 128 character PLA decodes the data bytes to determine which drivers to enable. Standard PLA patterns are available for three character fonts. The 10938, listed in Table 10, generates 5 × 7 dot matrix patterns. The 10941, listed in Tables 11 and 12, generates 16 segment and bargraph patterns. It also features separate decimal and comma drivers. This PLA may also be used for 14 segment and 7 segment displays. The 10942 and 10943 are combined to produce the 5 × 12 dot matrix patterns shown in Table 13.

Each grid controller/driver, i.e. 10939, can drive 20 digits and a cursor. These are push-pull drivers which can source 10 mA each. The 10939s may be cascaded, as shown in Figure 4, to drive displays of more than 20 characters. They may be connected in parallel, as shown in Figure 15, to drive multi-line displays having shared grids. In this configuration, the grid drivers may be wired ORed if additional grid current is required. However, when this is done, diodes and pull down resistors must be used as they are used with the cursor outputs. Alternatively, external drivers may be added. The total number of 10939s that may be connected together is limited by the duty cycle requirements of the display and the load on the master 10939 clock output. Typically, this limit is four 10939s but more may be added if the clock output load is kept below 50 pF.

In addition to the grid drivers, each 10939 contains a cursor output to drive the cursor segment present on some displays. This output is activated when the MSB of the data byte for a particular digit is a one.

USE OF EXTERNAL DRIVERS WITH INTELLIGENT DISPLAY CONTROLLERS

If external drivers are added, the devices of the Intelligent Display Controller product line can be used to control displays which operate beyond the range of the display controllers' internal drivers. This applies to LED, Gas Discharge and certain VF displays.

An example of this is shown in Figure 16. Here the 10941/10939 chip set is used to control a 16 segment LED display. The display consists of two Hewlett Packard HDSP-6508s. These are 16 segment GaAsP red LEDs. They are common cathode configured and mounted in an 8-character package. The 10939 strobe outputs are connected to 600 mA inverting drivers which control the cathodes. The 10941 segment outputs are connected to 500 mA sourcing drivers which control the anodes. A 47Ω current limiting resistor is also supplied to each anode.

DISPLAY CONTROL TECHNIQUES

DIGIT STROBING

The display controller strobe lines are activated sequentially starting with STR00 (AD1 on single chip controllers) and ending with the highest strobe enabled by the character count select commands. After the last strobe in the chain has completed its cycle, the process repeats. The strobe drivers may be connected to strobe a display from right to left, or from left to right, depending on the system requirements. In most cases this will be determined by board layout or software constraints.

BRIGHTNESS CONTROL

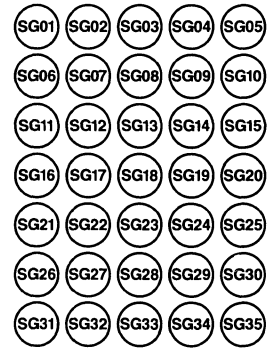
In certain applications, particularly in situations where the environmental light level varies, the display brightness must be varied from time to time. This can be done by varying the duty cycle and by adding and deleting fictitious digits.

For example, suppose a 10937 is used to control a 7-digit alphanumeric display. Assume that the maximum progammable duty cycle, i.e. each strobe ON 31 clock cycles, is used when ambient light levels are high. Then the display brightness can be decreased by decreasing the duty cycle. Display dimming from maximum to minimum brightness will be achieved in 31 steps with a 3.22 percent decrease from full brightness at each step.

At lower light levels it may be desirable to decrease the display brightness in smaller steps. This can be done by using fictitious digits. In this example, after the display has been dimmed to approximately 20 percent of full brightness, i.e. duty cycle value as been decreased from 31 to 7, the character count is increased from 7 to 16. At the same time, the duty cycle number is changed from 7 to 14. Display dimming then proceeds by successively reducing the duty cycle. However, now the brightness is reduced about 1.4 percent with each step.

Table 10. 5 x 7 Dot Matrix PLA Patterns

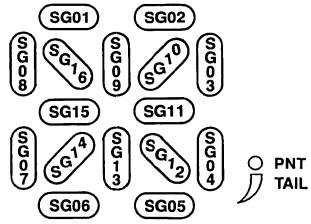
Input Data	Character	Input Data	Character	Input Data	Character	Input Data	Character	Input Data	Character	Input Data	Character	Input Data	Character	Input Data	Character
00		01		02		03		04		05		06		07	
08		09		0A		0B		0C		0D		0E		0F	
10		11		12		13		14		15		16		17	
18		19		1A		1B		1C		1D		1E		1F	
20		21		22		23		24		25		26		27	
28		29		2A		2B		2C		2D		2E		2F	
30		31		32		33		34		35		36		37	
38		39		3A		3B		3C		3D		3E		3F	
40		41		42		43		44		45		46		47	
48		49		4A		4B		4C		4D		4E		4F	
50		51		52		53		54		55		56		57	
58		59		5A		5B		5C		5D		5E		5F	
60		61		62		63		64		65		66		67	
68		69		6A		6B		6C		6D		6E		6F	
70		71		72		73		74		75		76		77	
78		79		7A		7B		7C		7D		7E		7F	



10938 Driver Assignments

Table 11. 16 Segment PLA Patterns

Input Data	Character	Input Data	Character	Input Data	Character	Input Data	Character	Input Data	Character	Input Data	Character	Input Data	Character	Input Data	Character
00		01		02		03		04		05		06		07	
08		09		0A		0B		0C		0D		0E		0F	
10		11		12		13		14		15		16		17	
18		19		1A		1B		1C		1D		1E		1F	
20		21		22		23		24		25		26		27	
28		29		2A		2B		2C		2D		2E		2F	
30		31		32		33		34		35		36		37	
38		39		3A		3B		3C		3D		3E		3F	
40		41		42		43		44		45		46		47	
48		49		4A		4B		4C		4D		4E		4F	
50		51		52		53		54		55		56		57	
58		59		5A		5B		5C		5D		5E		5F	



10941 Driver Assignments

Table 12. 16 Segment Bargraph Patterns

Input Data	Character	Input Data	Character	Input Data	Character	Input Data	Character	Input Data	Character	Input Data	Character	Input Data	Character	Input Data	Character
60		61		62		63		64		65		66		67	
68		69		6A		6B		6C		6D		6E		6F	
70		71		72		73		74		75		76		77	
78		79		7A		7B		7C		7D		7E		7F	

10941 Driver Assignments

Table 13. 5 x 12 Dot Matrix PLA Patterns

Input Data	Character	Input Data	Character	Input Data	Character	Input Data	Character	Input Data	Character	Input Data	Character	Input Data	Character	Input Data	Character
00		01		02		03		04		05		06		07	
08		09		0A		0B		0C		0D		0E		0F	
10		11		12		13		14		15		16		17	
18		19		1A		1B		1C		1D		1E		1F	
20		21		22		23		24		25		26		27	
28		29		2A		2B		2C		2D		2E		2F	
30		31		32		33		34		35		36		37	
38		39		3A		3B		3C		3D		3E		3F	
40		41		42		43		44		45		46		47	
48		49		4A		4B		4C		4D		4E		4F	
50		51		52		53		54		55		56		57	
58		59		5A		5B		5C		5D		5E		5F	
60		61		62		63		64		65		66		67	
68		69		6A		6B		6C		6D		6E		6F	
70		71		72		73		74		75		76		77	
78		79		7A		7B		7C		7D		7E		7F	

Segments Driven By 10942

SG01	SG02	SG03	SG04	SG05
SG06	SG07	SG08	SG09	SG10
SG11	SG12	SG13	SG14	SG15
SG16	SG17	SG18	SG19	SG20
SG21	SG22	SG23	SG01	SG02
SG03	SG04	SG05	SG06	SG07
SG08	SG09	SG10	SG11	SG12
SG13			SG14	SG15
SG16			SG17	SG18
SG19	SG20	SG21	SG22	SG23

Segments Driven By 10943

10942 and 10943 Driver Assignments

6

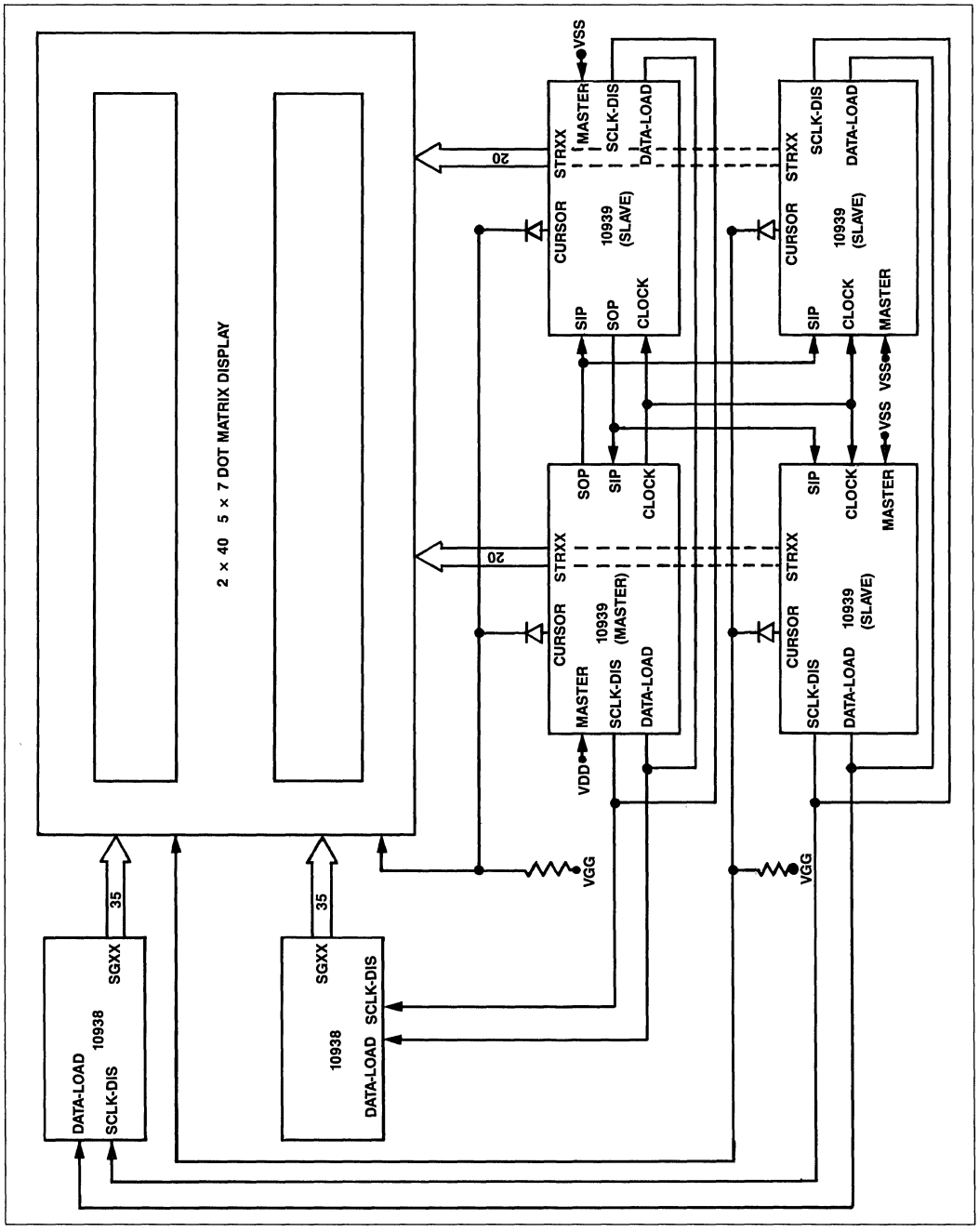


Figure 15. Driving a Two Line Display with a 10938 and a 10939

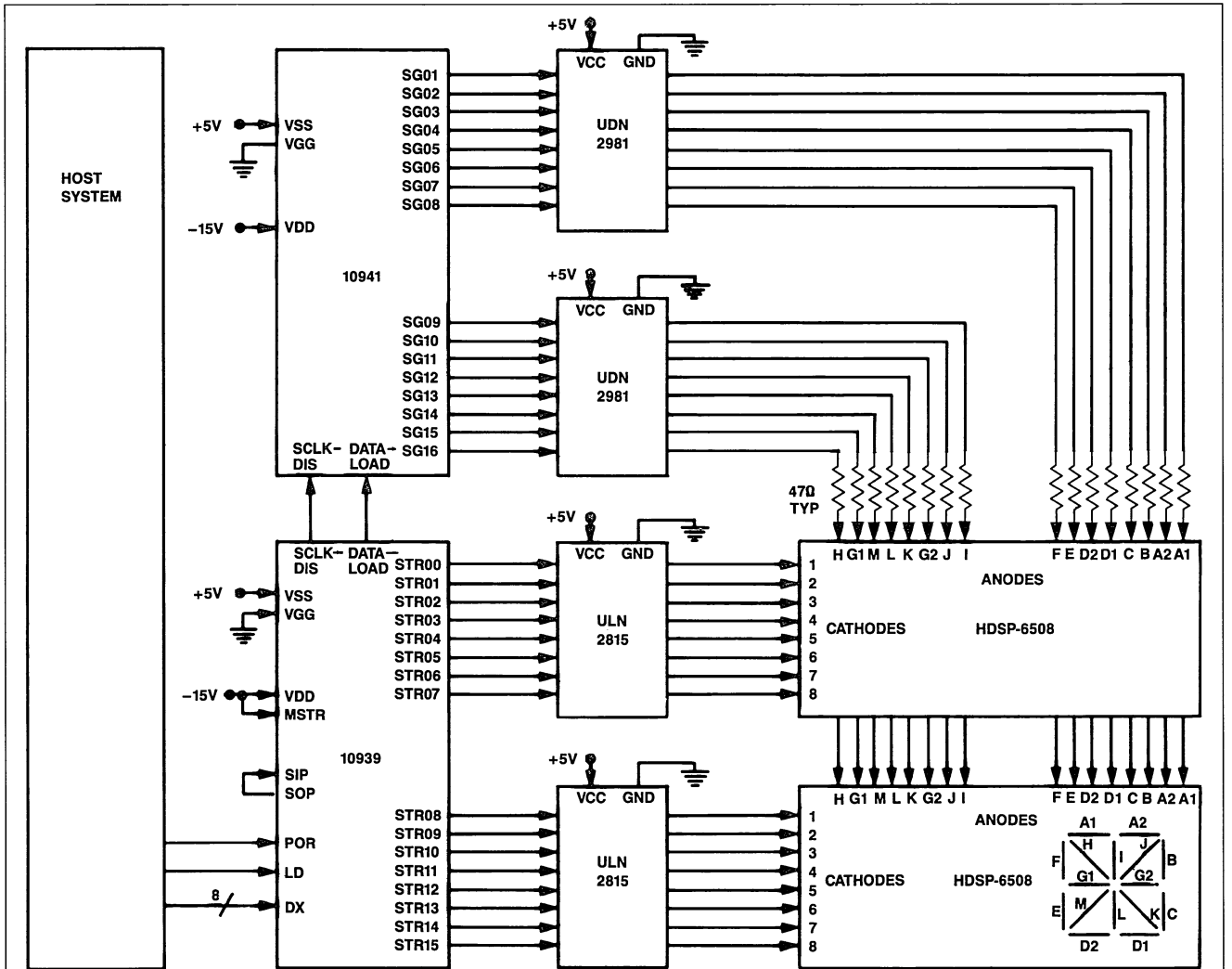


Figure 16. Driving an LED Display with a 10941 and a 10939

DISPLAY BLANKING

The intelligent display controllers may use several methods to blank displays. One method is to load the display buffer with blanks. A second method is to set the duty cycle to zero.

A third method of display blanking is available on multi-chip display controllers. This is the use of blank mode. When this mode is to be used, the display data buffer is loaded with data having the most significant bit set to a one. Then the display is blanked by enabling the blank mode. This feature is especially useful when only selected characters are to be blanked.

POWER REQUIREMENTS

INTRODUCTION

This section discusses some of the factors involved in determining power requirements of typical vacuum fluorescent display systems. It discusses the display tube construction and operation, the controller types and power requirements, and the factors which affect power dissipation. Examples of power calculations are given for several display configurations.

DISPLAY TUBE OPERATION

To be able to determine the power requirements for a display system it would be helpful to have a basic understanding of how a vacuum fluorescent tube is constructed and operates.

Construction

The vacuum fluorescent display tube contains three basic elements in an evacuated tube. These are the filament cathode, control grid and anode. The directly heated cathode, nearest the glass viewing surface, is a metal filament covered with an oxide coating and is thin enough not to cause viewing interference. The control grid is a wire mesh also thin enough not to cause viewing interference. The anodes are formed of a fluorescent material coating on insulating bases to form alpha-numeric, bargraph or dot matrix segments.

Operation

Thermionic emission by the cathode results at the relatively low temperatures of 650°C to 700°C. When positive voltages (with respect to the cathode) are applied to the grid (Ec) and anode (Eb), the electrons are accelerated toward them. The fine mesh construction of the grid allows most of the electrons to pass through it to the phosphor on the positive anodes. The collision of electrons on the phosphor causes light to be emitted in the blue-green spectrum.

When no voltage is applied to the grid (same potential as the cathode) some of the electrons still get through to the positive anode. To cut off all electron flow to the anode, a negative voltage with respect to the cathode is applied to the grid. This is called the grid cutoff voltage (Ecco). When the anode voltage is open or lower than the cathode voltage almost no electrons reach the phosphor and those few that do have insufficient energy to cause light emission. This is known as the plate (anode) cutoff voltage (Ebco). The negative potential cutoff voltages are normally both the same level and are generated by providing a positive cathode bias (EK).

The basic principle of operation is shown in Figure 17. Three anode segments are shown in the vacuum tube. If anode voltage Eb is applied through switches S_1 and S_3 with S_2 open, for example, currents Ia1 and Ia3 flow to their respective anodes to cause light emission.

By increasing the number of anode segments to seven and arranging them to form numerals, digits from 0 to 9 can be indicated. More anode segments are added to provide the popular 14 or 16 segment alpha-numeric characters. Dot matrix configurations lend themselves to more versatile character generation and are generally a matrix of 5 × 7 dots (35 anodes) or 5 × 12 dots (60 anodes) as shown in Figure 18.

Providing the same pattern of anodes (character) behind multiple grids and time multiplexing the "ON" signal to each grid allows multi-character displays to be constructed in a single tube as shown in Figure 19. As each grid in a multi-character display tube is turned on (positive pulse applied) the appropriate anodes are also driven positive to form the desired character at that position.

Electrical Considerations

A major feature of any display device is the readability of the characters and this relates directly to luminance or brightness of the device. Luminance is affected by factors such as filament, grid and anode voltages, as well as duty cycle, phosphor response and temperature.

The filament voltage (Ef) is selected carefully to produce a filament temperature near 700°C. Thermionic emission increases rapidly with filament temperature up to about 600°C where it levels off. The filament voltage is selected by the tube manufacturer to work in this saturation region of about 650°C to 700°C. If the filament temperature is too high (high Ef), the overheating causes a brightness slump due to evaporation of the oxide. A too low filament temperature operates on the steep part of the emission curve and brightness variation becomes large and unstable with slight voltage variations. The filament voltage should not be used to vary luminance.

Another factor of filament voltage affects the brightness in multi-character displays. Using dc voltage for the filament produces a linearly distributed bias voltage across the filament element resulting in a non-uniform display brightness. The filament voltage is specified therefore by the manufacturer as ac; either 60 Hz or a higher frequency pulse from a dc-to-ac converter. The filament bias voltage is normally applied to the center tap of the filament transformer as discussed later.

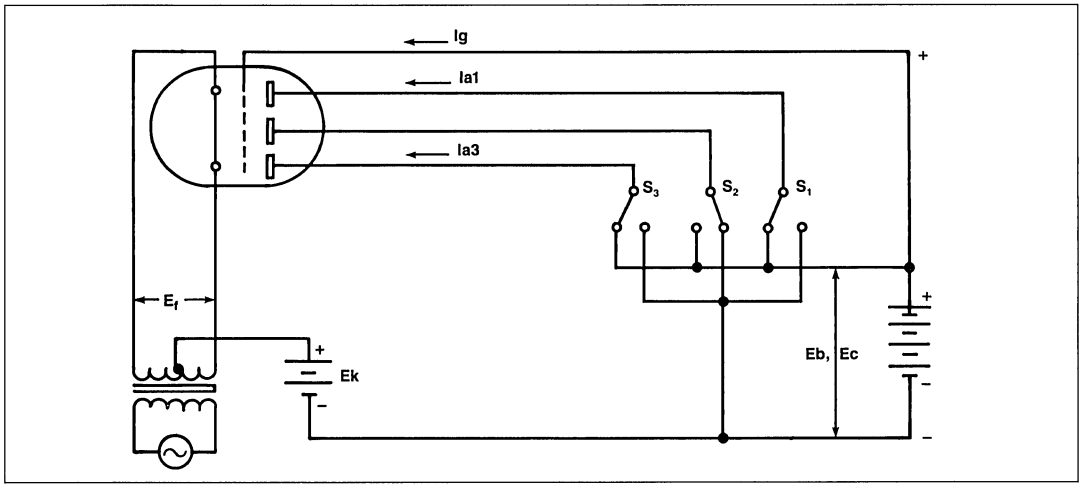


Figure 17. Basic Operation

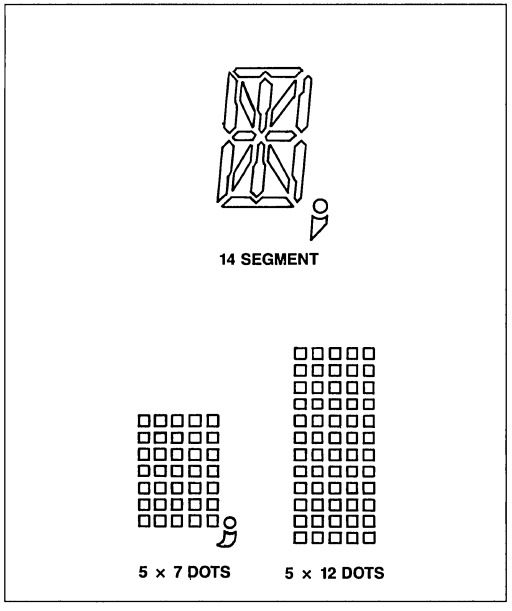


Figure 18. Characters

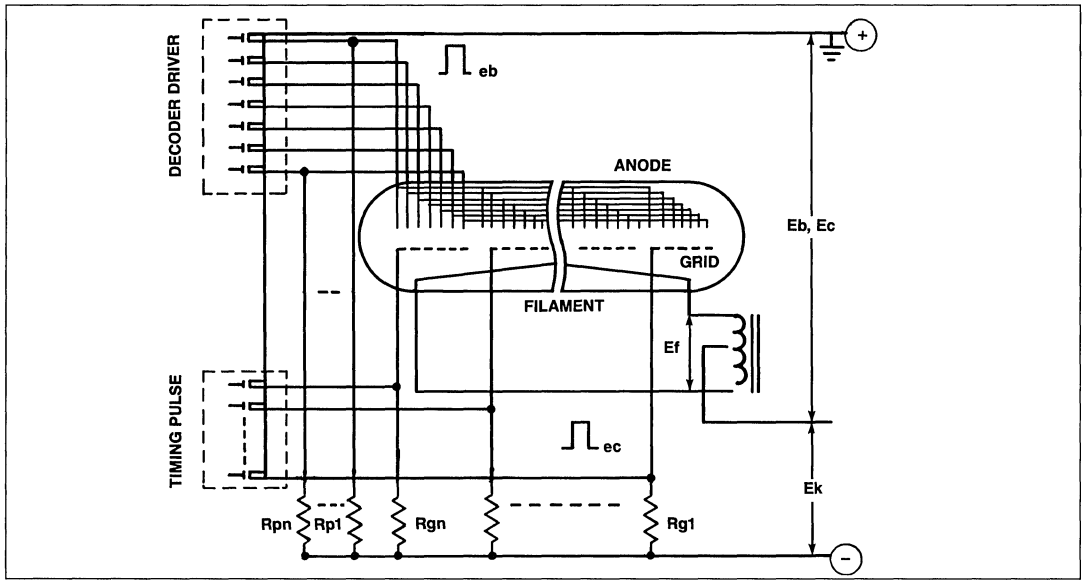


Figure 19. Basic Dynamic Drive Circuit

Brightness is also affected by the level of the grid and anode voltage (currents). To obtain an acceptable brightness level using a dc voltage on the grid or anode takes far less voltage than when the element is pulsed as shown in the graph of Figure 20. However, by multiplexing this pulse to many characters (grids) a large power savings is realized. The relationship of luminance to grid and anode voltage is given by the expression:

$$L = K * (ebc)^{2.5} * \left(\frac{tp}{Tr}\right)$$

where: L = Luminance
K = a constant depending on tube type
ebc = grid and anode voltage, where eb = ec
tp/Tr = pulse duty cycle

From the above equation it can be seen that the duty cycle of the pulse has a bearing on the brightness of the display. When a pulse voltage is applied to the device a time lag is seen between the pulse application and the brightness response of the fluorescent material due to the internal impedance of the tube itself. Figure 21 indicates that this time lag is about 8 μs in both rise time and fall time. It is recommended by display manufacturers that blanking (no positive voltage to any grid) of about 20 μs be provided

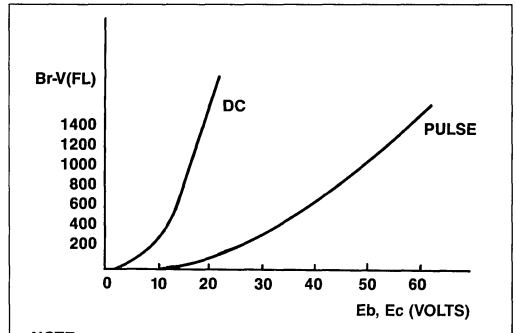


Figure 20. Anode Grid Voltage—Brightness Characteristics (DC and Pulse)

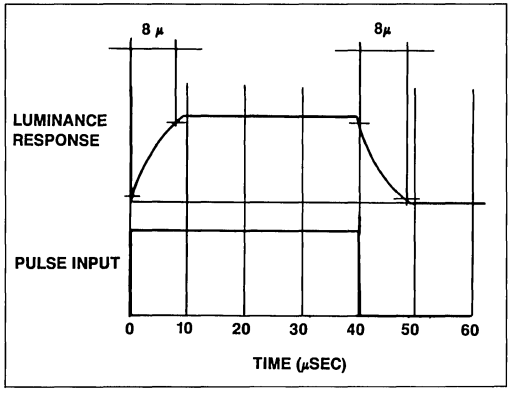


Figure 21. Pulse Response of Phosphor

between the multiplexed digit pulses to assure that the response time lag and extraneous noise does not cause undesirable character illumination. Note that brightness will be constant when duty factor is constant regardless of pulse width except that brightness will deteriorate when the pulse width nears 8 μs or less. Figure 22 shows the relationship of adjacent multiplexed grid pulses with the blanking separation.

Because the fluorescent material has semiconductor properties the luminance is also affected by ambient temperature as shown in Figure 23. Most display tube manufacturers recommend operation between −10°C to +55°C.

Controller Power Requirements

As shown previously, the Rockwell display controllers are of three types: grid/anode controllers with open drain drivers, and grid controllers and anode controllers with push-pull drivers. The power requirements for these controllers will be covered in this section. The factors which affect the power dissipation will also be discussed: these include voltage variations, temperature affects, and the display load requirements such as tube type and characters being driven.

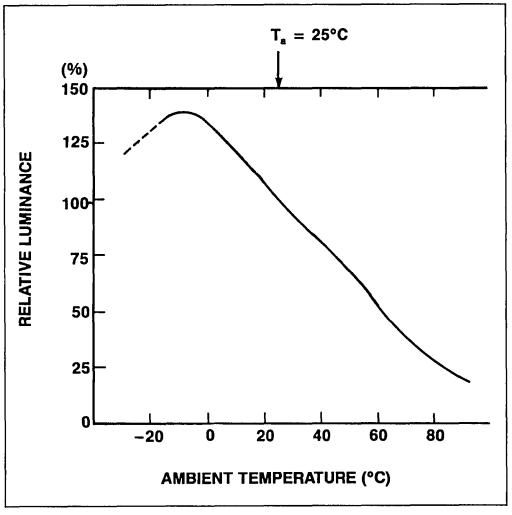


Figure 23. Ambient Temperature Effect

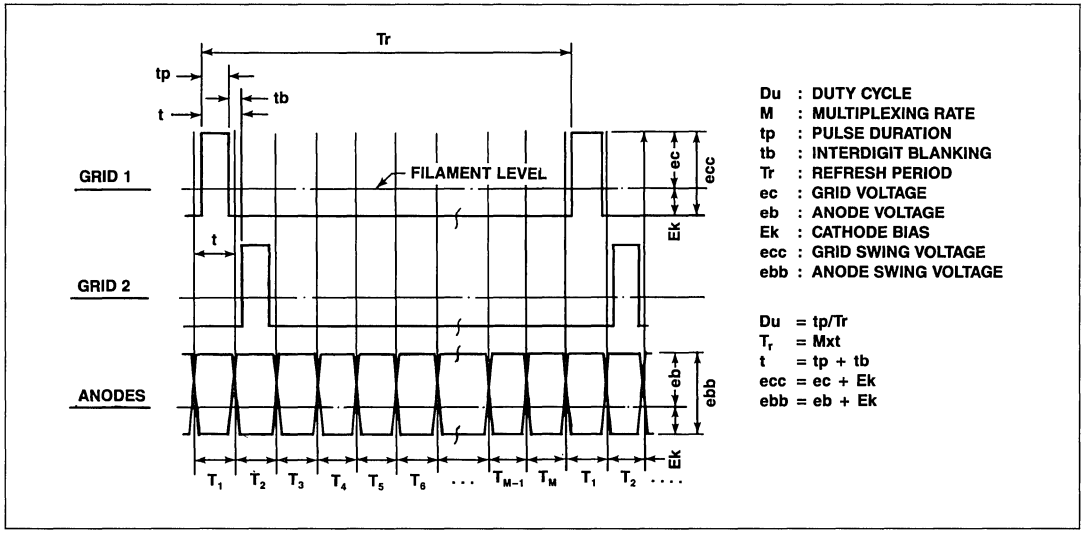
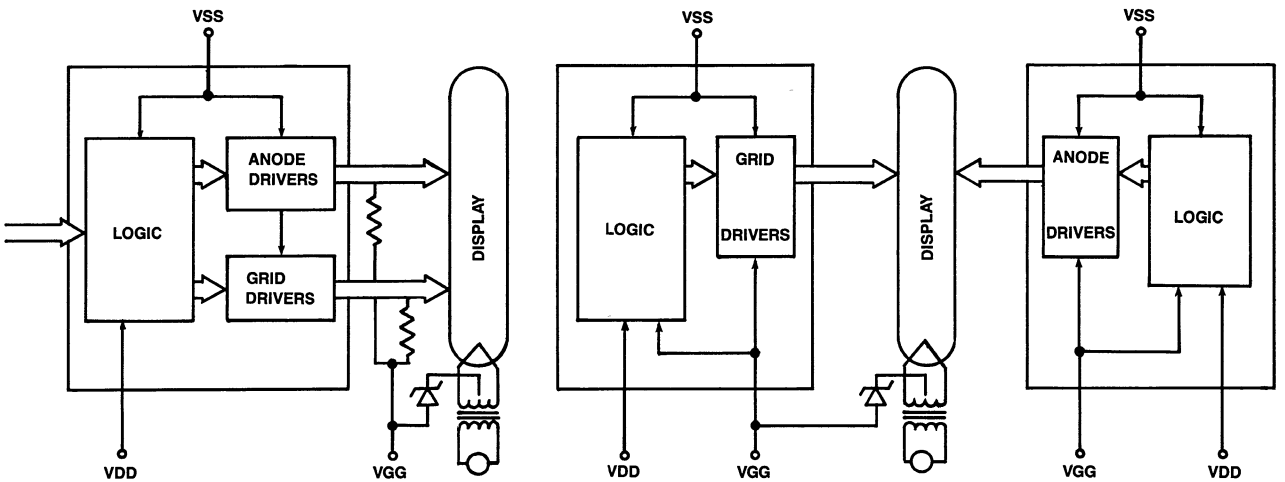


Figure 22. Relationship of Adjacent Multiplexed Grid Pulses with Blanking Separation



DEVICE TYPE: DRIVER TYPE: PART NUMBER:	GRID/ANODE CONTROLLER OPEN-DRAIN 10937, 10951, 10957	GRID CONTROLLER PUSH-PULL 10939	ANODE CONTROLLER PUSH-PULL 10938, 10941, 10942, 10943
VDD MAX Idd AT 25°C ΔIdd/Vdc	−15 ±1.5 Vdc 2.12 mA 0.057 mA/Vdc	−20 ±2 Vdc 4.0 mA Slave, 6.0 mA Master 0.025 mA/Vdc	−20 ±2 Vdc 3.2 mA 0.015 mA/Vdc
VGG MAX Igg AT 25°C ΔIgg/Vdc		−50 Vdc 0.5 mA NEGLIGIBLE	−50 Vdc 8 mA 0.15 mA/Vdc

Figure 24. Display Controller Architecture

Device Power Requirements

Figure 24 shows the three basic types of Rockwell display controller devices. They have open-drain or push-pull drivers which are shown schematically in Figure 25.

Vdd power is used in all three device types for the logic section. Worst case dissipation is at Vdd max (−16.5 Vdc for the open-drain device and −22 Vdc for the push-pull devices) and at the lowest temperature (0°C for the commercial range and −40°C for the industrial range). Idd varies as a function of applied voltage and temperature.

Vgg power is dissipated in the push-pull driver devices when an output grid or anode driver is ON (pulled to Vss). Most of the dissipation is in the logic pre-drivers but a small amount is also used in the driver itself. At worst case, with Vgg at −50 Vdc and a temperature of −40°C, the maximum drain for each ON grid driver is 25 mW or 0.5 mA/driver. As an example, since only one grid driver and the cursor driver can be ON at the same time, the maximum Igg load of the 10939 device is 1.0 mA. The maximum drain for each ON anode driver is 16 mW or .32 mA per driver, so the maximum Igg load of the anode controller with all 35 anode drivers ON would be 11.2 mA. Igg varies not only as a function of the number of drivers ON, but also as a function of applied voltage and temperature.

Effects of Voltage Variations

The effects of supply voltage variations on current drains are shown in Figure 26. As Vdd supply voltage increases the current also increases at rates from approximately 0.015 mA/Vdc to almost 0.06 mA/Vdc depending on device type. Igg also increases as Vgg increases for the push-pull driver devices as shown for the 1094X anode driver devices.

Effects of Temperature Variation

As previously stated, the worst case supply current is at the lowest temperature extremes. The power dissipation in the controller device for both Vdd and Vgg generally follow the curve shown in Figure 27. The curve is defined by the equation below and is normalized to +25°C:

$$\frac{K'}{Ko'} = \left(\frac{T}{To}\right)^m$$

Where K′ = K factor at new temperature, T
Ko′ = K factor at To (25°C)
T = New temperature, in Kelvin
To = Initial temperature (25°C = 298°K)
m = Exponent, dependent on device materials

Display Load Variations

Current is drawn from the Vgg supply due to the display grid or anode load itself. This load is a function of the display tube and may be any load up to the maximum allowed by the device driver. I_{load} (max) for the grid, cursor, point and tail drivers is 20 mA for the single chip controllers and 10 mA for the grid controller drivers. The maximum load on the segment drivers of the single chip controllers is 10 mA and the maximum load of the anode drivers is 2 mA each. Each tube type is different and actual current requirements must be taken from the manufacturers display tube specifications. This power is dissipated in the display tube rather than in the controller device and is also dependent on the number of grids or anodes that are driven ON.

Character Load Variations

The total device power required is dependent on the number of grids or anodes being driven ON at any particular moment. The grids are driven ON sequentially in a multiplexed fashion so that only one grid is ever enabled at any time. The anodes are driven individually to form different characters in both the segmented and dot matrix displays. The anode driver devices are designed with up to 35 output drivers available as shown in Table 14. However, not every driver is used to form characters in each application.

Table 14 shows the dot patterns of the 128 character font for the 10938 anode driver device. Except for the inverse mode in which all the dot patterns are reversed, and character 7F which has all anodes ON; the worst case dot pattern is letter "B" which has 20 anodes ON. If, for example, a particular application requires only alpha-numeric characters displayed, the peak drive current required for the load would be only 57 percent of the worst case load. With a display tube requiring a maximum load of 2 mA for each dot anode, the total Igg current required would be (35 × 2 mA × 0.57) 39.9 mA for the display tube and (35 × 0.32 mA × 0.57) 6.4 mA for the 10938 drivers. The average current would be (35 × 2 mA × 0.384) 27 mA for the display tube and (35 × 0.32 × 0.384) 4.3 mA for the 10938 drivers. Note, however, that the actual predominance or frequency of use of each character has to be considered to obtain a realistic average current over a given time period. Table 15 lists the average ratios of anodes ON per total anodes for the various anode driver devices.

DISPLAY SYSTEM POWER CONSIDERATIONS

The controller device power is not the only power that has to be considered in deriving display system power requirements. Also to be considered are the power for the host microprocessor and the display tube load.

Typical Power Flow

The microprocessor is normally a bipolar or MOS device requiring +5 vdc for its power source. In such a display system the Vss return for the control devices is returned to the +5 vdc Vcc as shown in Figure 28. Vdd is a negative supply, referenced to Vss, to supply the logic sections of the controller device. Vgg is a negative voltage to supply anode and grid current through the controller output switches to the display tube. Ek is a positive level voltage referenced to Vgg for cathode bias (to the center tap of the filament transformer). The filament voltage is an ac 60 cycle voltage supplied through a step down transformer or a dc-dc converter output which supplies a chopped high frequency square wave.

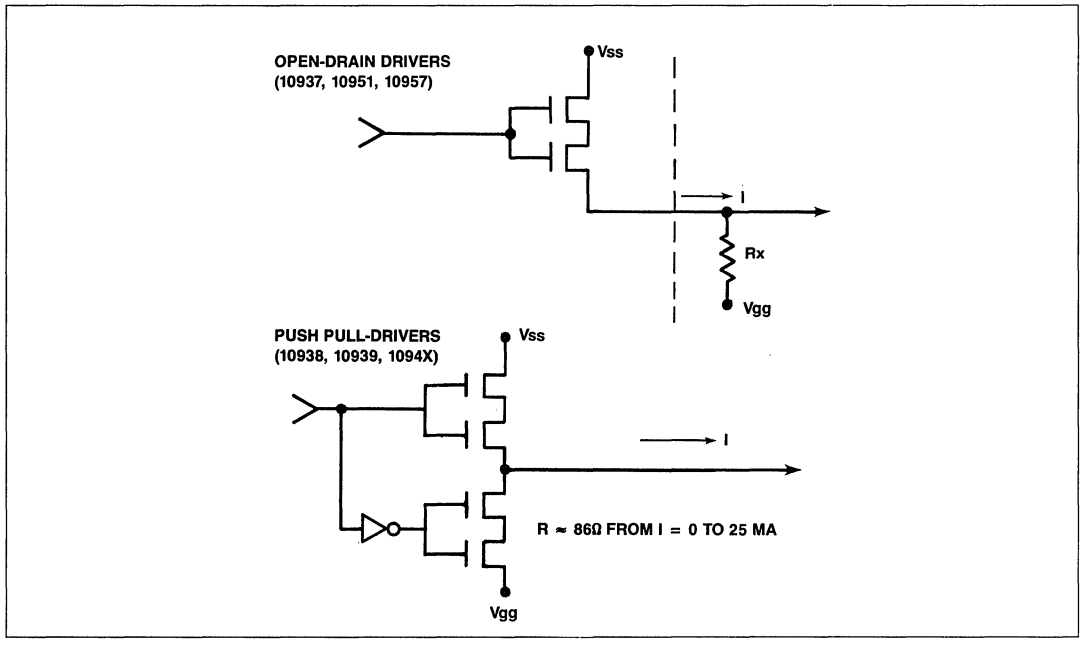


Figure 25. Controller Drive Circuits

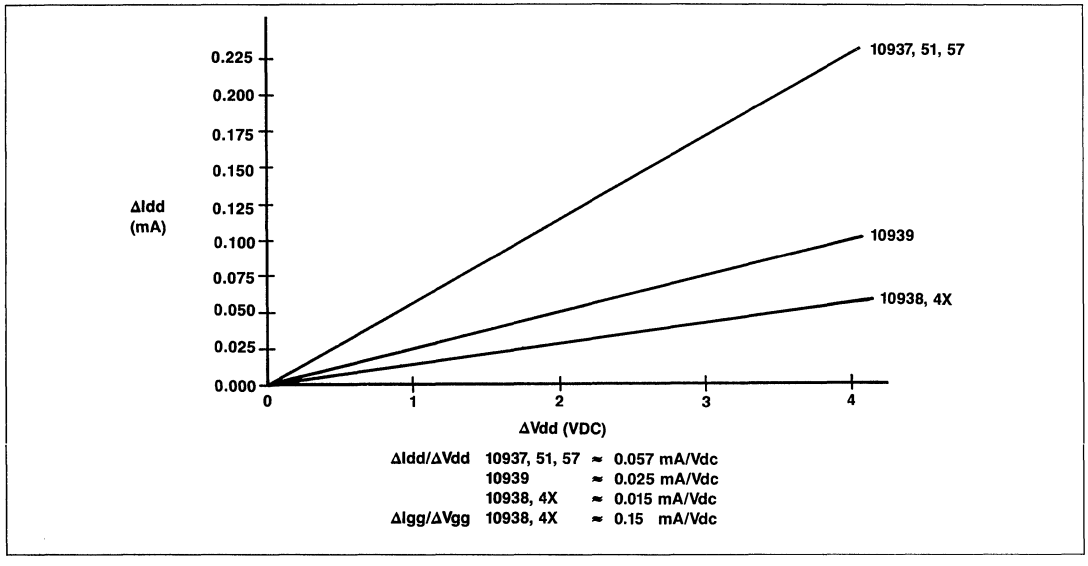
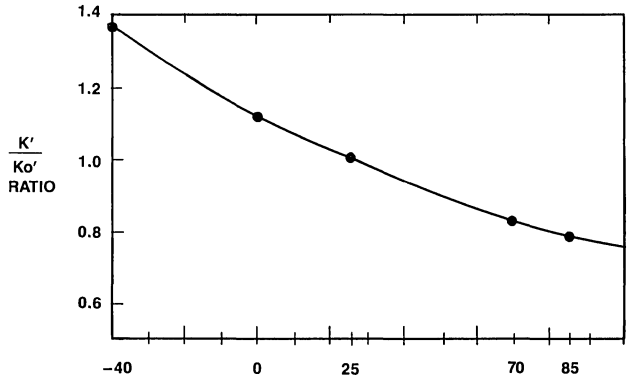


Figure 26. Effects of Voltage Variation, ΔIdd/ΔVdd (at 25°C)



Temp (°C)	–40	0	+25	+70	+85
K′/Ko′ RATIO	1.38	1.1	1.0	0.83	0.78

Figure 27. Effects of Temperature Variations

Table 14. 10938 Dot Patterns

#Anodes ON	Character	#Anodes ON	Character	#Anodes ON	Character	#Anodes ON	Character	#Anodes ON	Character	#Anodes ON	Character	#Anodes ON	Character	#Anodes ON	Character
0		17		18		7		14		12		16		15	
14		13		18		9		11		8		16		5	
17		17		17		18		16		17		16		15	
10		11		17		9		7		9		7		15	
0		5		6		18		15		13		16		3	
9		9		11		9		3		5		2		5	
16		10		14		15		14		17		16		11	
17		16		2		4		7		10		7		9	
18		18		20		13		18		17		13		16	
17		11		9		14		11		17		17		16	
15		17		18		15		11		15		13		18	
13		10		15		13		5		13		11		11	
3		14		14		11		14		15		11		17	
12		8		8		11		9		16		12		12	
14		14		8		12		10		12		9		12	
9		10		13		15		13		14		5		35	

Character(s)	# Anodes ON	% Anodes ON
1 Letter "B"	20.0	57.1
2 Avg of all Numeric	14.1	40.0
3 Avg of all Alpha Caps	14.9	42.6
4 Avg of all Alpha Lowercase	11.7	33.4
5 Avg of items 2 & 3	14.7	41.9
6 Avg of items 2 thru 4	13.4	38.4
7 Avg of all characters	12.4	35.4

Table 15. Character Anodes ON Summary

Character(s) Display Type	% Anodes On			
	10937, 10957	10938	10941**	10942/43
• Total Anodes	16	35	16	46
• Worst Case Digit(s)*	$,%,0	B	$,%,0,8	B
Anodes ON	10	20	10	20
% Anodes ON	63.0	57.1	62.5	43.5
• Numeric (Avg, %)	46.0	40.0	46.3	31.1
• Alpha all caps (Avg, %)	39.0	42.6	38.9	32.4
• Alpha lower case (Avg, %)	—	33.4	—	26.9
• Alpha Caps — Numeric (Avg, %)	41.0	41.9	41.0	32.1
• Alpha — Numeric (Avg, %)	41.0	38.4	41.0	29.9
• All Characters (Avg, %)	24	35.4	37.0	27.2

*Excluding inverse and all dots ON pattern.
** Excluding bargraph

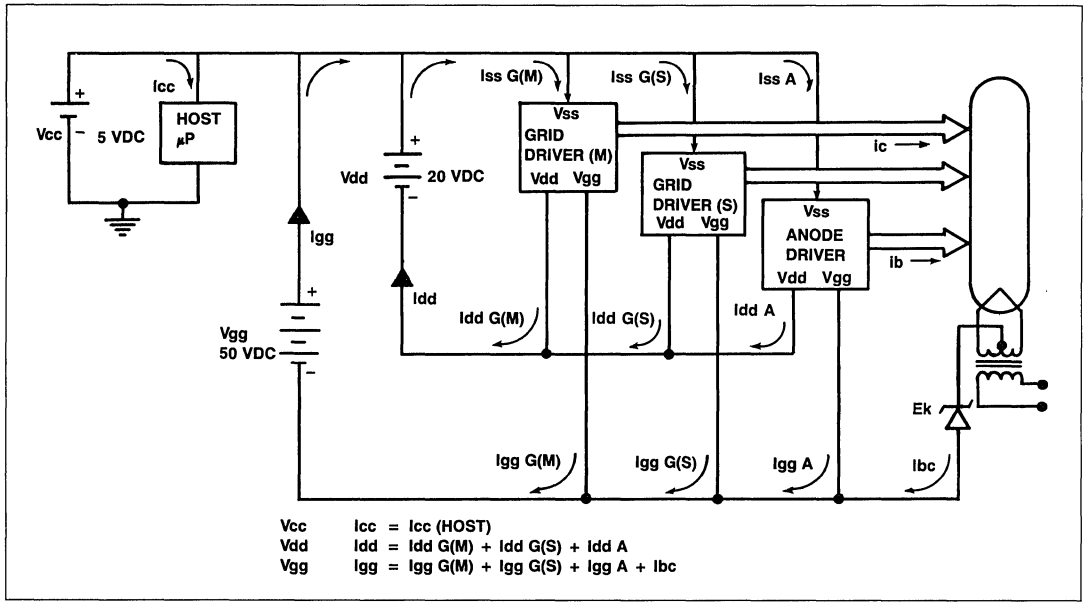


Figure 28. Typical Display System Power Flow

Example 1: 20-Character Display

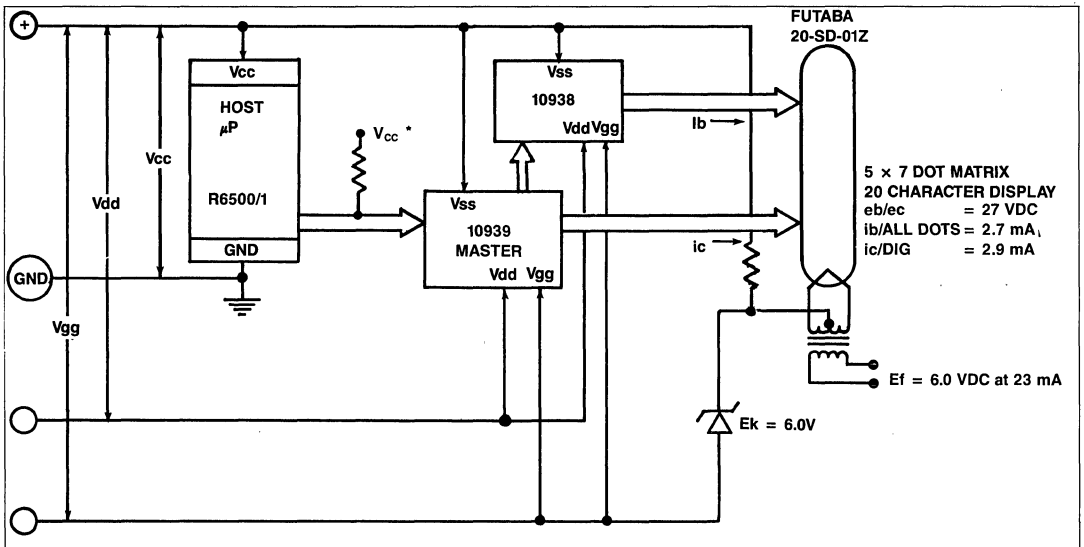
Figure 29 shows a 5 x 7 dot matrix 20-character display tube being driven by a 10938 anode driver and a 10939 grid driver and controlled by an R6500/1 microprocessor. Five voltage levels are required including the ac filament voltage of 6 Vac @ 23 mA typically.

The other voltages are:

Vcc of +5 Vdc referenced to Gnd for the microprocessor
Vdd of −20 Vdc referenced to Vss for the driver devices
Vgg of −33 Vdc referenced to Vss for the driver devices
Ek of +6 Vdc referenced to Vgg for the display tube cathode

As discussed before, Vgg is determined by the sum of eb/ec and Ek. Ek bias above Vgg is normally provided by a zener diode reference. The ac filament voltage, Ek and eb/ec are specified by the display tube manufacturer.

The Vcc current requirement is typically 100 mA at +25°C. The Vdd current requirements from Figure 24 are 6 mA for the 10939 grid driver and 3.2 mA for the 10938 anode driver. Vgg current from Figure 24 is .25 mA for the 10939 and 8 mA for the 10938, however, this is at a Vgg of −50 Vdc. At −33 Vdc the 10938 current reduces at a rate of 0.15 mA/Vdc for a total of [8−(0.15)(17)] 5.5 mA. Other Igg components from the display tube characteristics include the anode drive of 2.7 mA/all dots ON, and the grid drive of 2.9 mA. This total Igg current of 11.3 mA is representative of all 35 dots on continuously.



	(1) 10939 GRID DRIVE	(1) 10938 ANODE DRIVE	DISPLAY TUBE ib	DISPLAY TUBE ic	TOTAL (mA)
AT 25°C, TYPICAL					
• Idd (AT −20 VDC)	6.0	3.2	—	—	9.2
• Igg (AT −33 VDC)					
ALL DOTS "ON"	0.2	5.5	2.7	2.9	11.3
ALPHA NUMERIC ONLY	0.2	2.1	1.1	2.9	6.3
PEAK, LETTER "B"	0.2	3.1	1.5	2.9	7.7
AT −40°C W.C.					
• Idd (AT −22 VDC)	13.6	4.5	—	—	18.1
• Igg (AT −36 VDC)					
ALL DOTS "ON"	0.5	8.2	3.7	4.0	16.4

Figure 29. 20 Character Display Example

For display operation of alphanumerics only, with an average of 38.4 percent of the dots ON as shown in Table 15, anode drive currents reduce to a total Igg of 6.3 mA. Peak Igg for the letter "B" increases anode drive current to 57 percent of all dots for a total of 7.7 mA.

Worst case power dissipation is also shown in Figure 29. This is at maximum voltage excursions and a temperature of −40°C. (Keep in mind, however, that most VF display tubes are recommended for operation down to only about −10°C to −20°C.) Idd at −22 Vdc increases by 0.03 mA for the 10938 (as shown in Figure 24) to 3.23 mA. Figure 27 shows that a factor of 1.38 is used to determine Idd or Igg at −40°C so that the total Idd becomes (3.23 • 1.38) 4.5 mA. Igg for the 10938 becomes [(5.5 mA + 0.15 mA/Vdc • 3 Vdc) 1.38] 8.2 mA. The same procedure is used to determine the grid driver current requirements. Igg is assumed to increase by 50 percent worst case. The tube currents ib and ic are assumed to increase by 20 percent as temperature decreases from +25°C to −20°C and voltage increases to maximum which is worst case for VF display tubes.

Note in these examples that the cursor drive requirements for the 10939 and display tube have not been included and would have to be added to the totals when used.

Example 2: 40-Character Display

Figure 30 shows how the 10939 controller devices are cascaded to control the 40-character display tube. The 10942/43 devices are used in parallel to provide an expanded font capability for a 5 × 12 dot matrix.

The current requirements for this system are determined in the same way as in Example 1. Note that when two 10939s are used, the logic current (Idd) is the sum of a master and one slave but the grid drive current (Igg) remains the same. This is because in a master-slave configuration only one grid is enabled at any given moment giving a constant Igg and ic load of a single grid.

For this example Vgg is −50 Vdc (eb/ec of 41 Vdc and Ek of 9 Vdc) for an Igg of .25 mA for the grid drivers. However, only 23 of the 35 drivers are used in the anode driver bringing the total to 5.25 mA/device. For totally alphanumeric applications the anode currents reduce to 30 percent of all dots ON and the peak currents for letter "B" reduce to 43.5 percent of full ON.

The worst case power dissipation at voltage and temperature extremes are calculated in the same way as in Example 1.

Example 3: Two-line by 40-Character Display

Figure 31 is an example of a more advanced display system. The major difference between this example and Example 2 is that two grids are enabled at the same time (one in each line) and therefore the grid drive current and Ic are doubled.

Power Source

The power source for the display systems can be derived from standard power supplies, custom designs, or DC-DC converters.

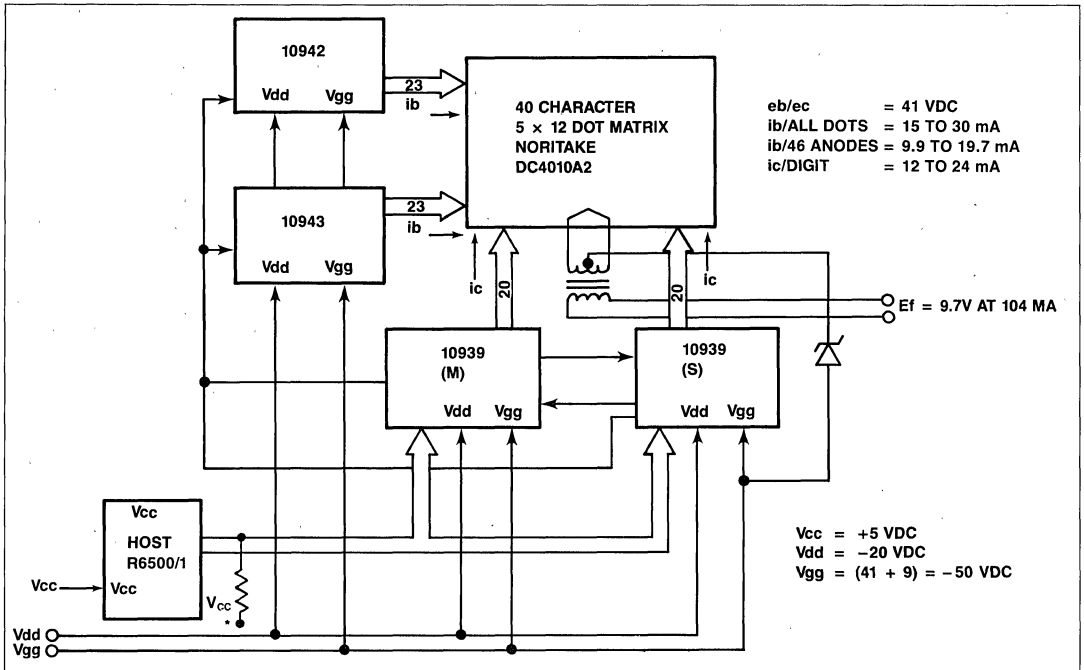
Four separate standard supplies could be used to furnish the four dc voltages required for Example 1 as shown in Figure 32. This is expensive, however, and the proper voltage levels are not really "standard" in most cases, and therefore not readily available. Tracking of the power supplies upon power turn-on and turn-off could also be a problem. The structure of the PMOS display driver devices is such that Vgg should not be more negative than Vdd unless Vdd is at −10 Vdc or greater; otherwise, damage to the output drivers is possible. If the 40 Vdc Vgg supply has much faster response than the 20 Vdc Vdd supply in Figure 32, this problem could exist.

Figure 33 shows how the voltages could be derived using only two standard supplies and zener diodes for the other levels. Using a zener diode to generate Vdd from the Vgg supply level assures that the Vdd and Vgg levels "track" all the way to Vdd. This is also shown in Figure 33. Another zener is used to generate the Ek bias voltage above Vgg for the filament transformer center tap.

DC-DC converters are also available that have been designed specifically to provide the power requirements for particular display tube types available in the marketplace. As shown in Figure 34, these converters normally oscillate the low voltage dc input through a step-up transformer and then rectify and filter the high frequency square wave to provide the desired output voltage. A dc feedback is applied to the input oscillator transistor to adjust the oscillation duty cycle and thus provide a constant voltage output. To provide multiple dc output levels (such as for Vdd and Vgg) multi-turn secondary transformer taps and rectifier filter sections are included in the design. See Reference 3 for addresses of DC-DC converter vendors.

FOOTPRINTS

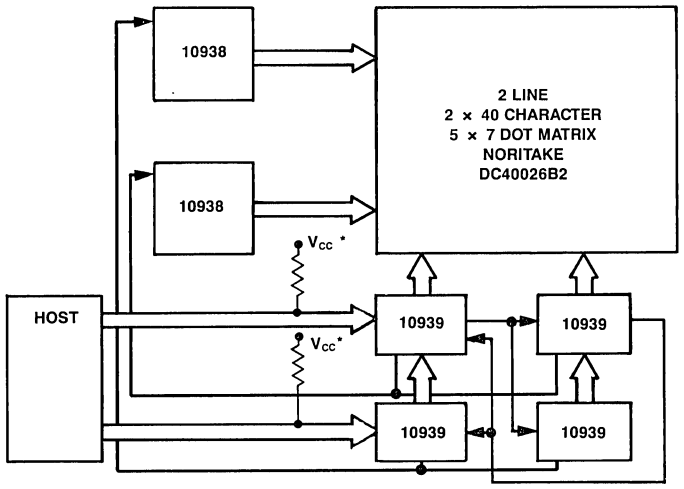
Figure 35 contains the pin configurations of all the products of the Intelligent Display Controller family.



*PULLUPS REQUIRED ON ALL INPUTS FROM TTL SOURCES

	(2) 10939 GRID DRIVE		(1) 10942 (1) 10943 ANODE DRIVE	DISPLAY TUBE ib	DISPLAY TUBE ic	TOTAL (mA)
AT 25°C, TYPICAL	M	S				
• Idd (AT −20 VDC)	6.0	4.0	6.4	—	—	16.4
• Igg (AT −50 VDC)						
ALL DOTS "ON"		0.3	10.5	15.0	12.0	37.8
ALPHA NUMERIC ONLY		0.3	3.2	4.5	12.0	20.0
PEAK, LETTER "B"		0.3	4.6	9.4	12.0	25.3
AT −40°C W.C.						
• Idd (AT −22 VDC)	13.6	9.1	8.9	—	—	31.6
• Igg (AT −55 VDC)						
ALL DOTS "ON"		0.5	14.5	18.0	14.4	47.4

Figure 30. 40 Character Display Example



eb/ec = 42 VDC
Ek = 8 VDC
ib/ALL DOTS = 7.5 to 15 mA
ic/DIGIT = 15 to 25 mA
Ef = 9 VAC AT 15 mA

(SEE FIGURE 15 FOR TYPICAL INTERCONNECTIONS.)

	(4) 10939 GRID DRIVE		(2) 10938 ANODE DRIVE	DISPLAY TUBE ib	DISPLAY TUBE ic	TOTAL (mA)
AT 25°C, TYPICAL	M	(3) S				
• Idd (AT −20 VDC)	6.0	12.0	6.4	—	—	22.4
• Igg (AT −50 VDC)						
ALL DOTS "ON"		0.5	16.0	15.0	30.0	61.5
ALPHA NUMERIC ONLY		0.5	6.2	5.8	30.0	42.5
PEAK, LETTER "B"		0.5	9.2	8.6	30.0	48.3
AT −40°C W.C.						
• Idd (AT −22 VDC)	13.6	27.3	9.0	—	—	49.9
• Igg (AT −55 VDC)						
ALL DOTS "ON"		1.0	22.4	18.0	36.0	77.4

*PULLUPS REQUIRED ON ALL INPUTS FROM TTL SOURCES

Figure 31. Advanced Display System Example

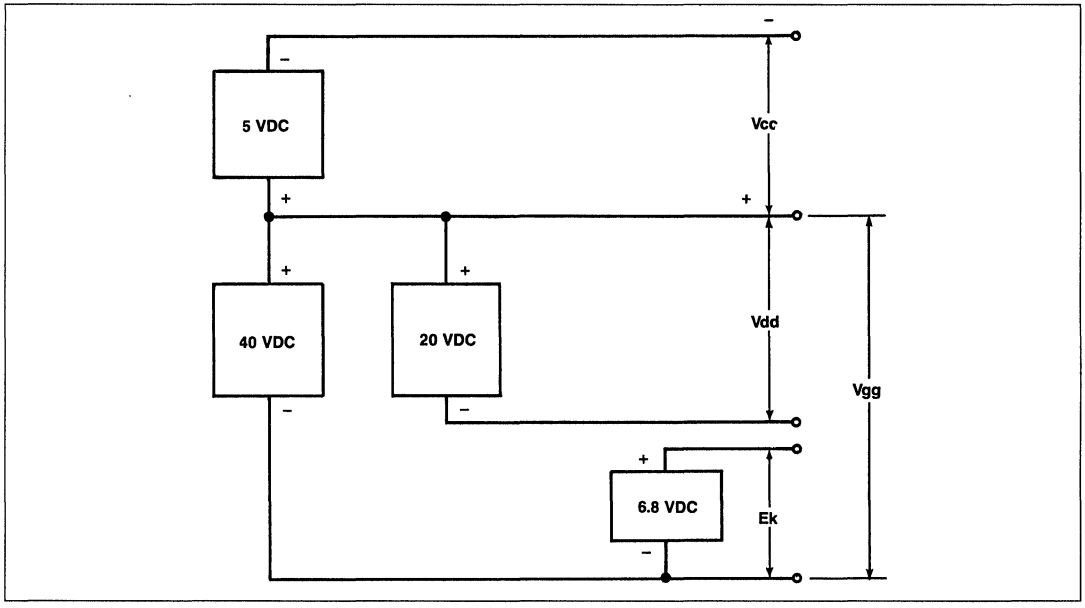


Figure 32. Standard Power Supply Source

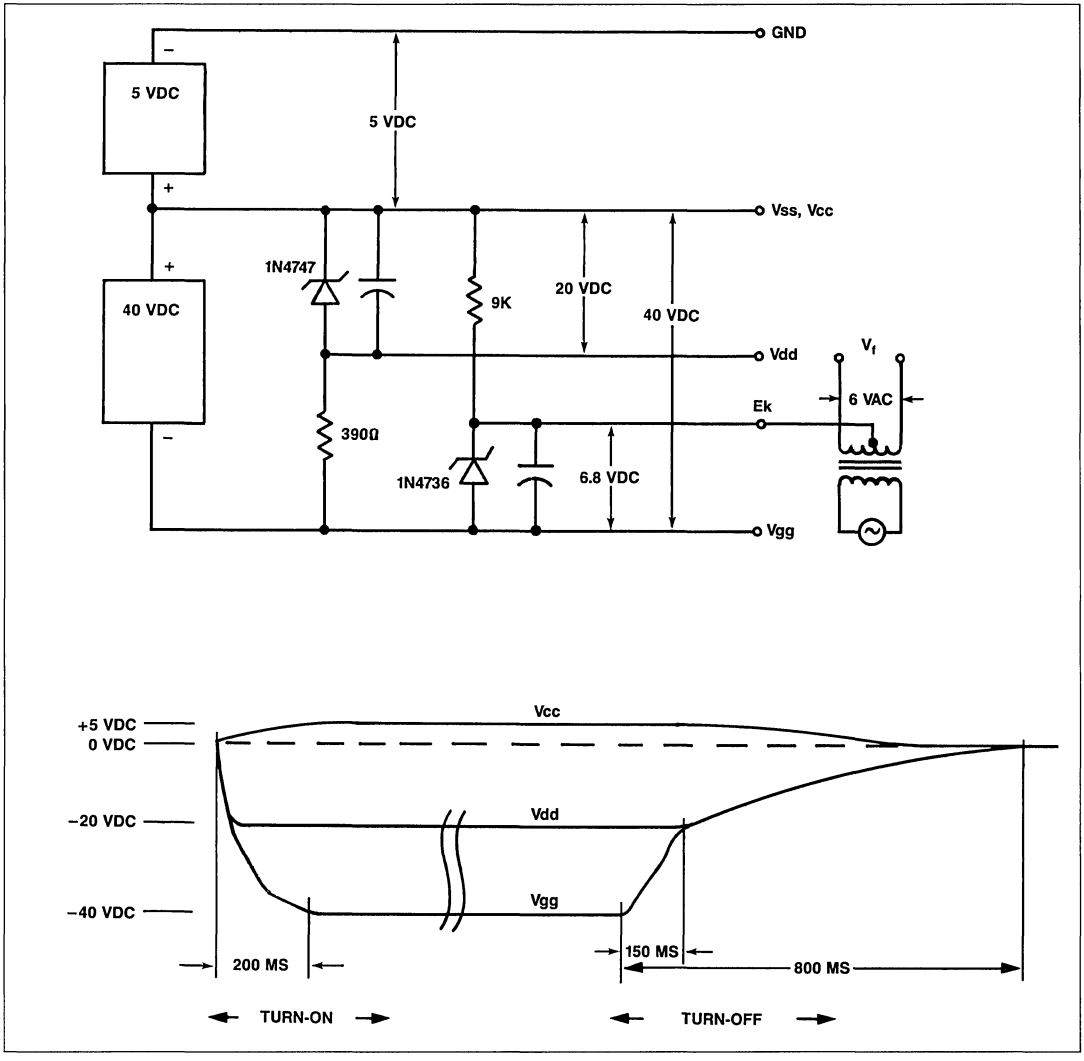


Figure 33. Modified Power Supply Source

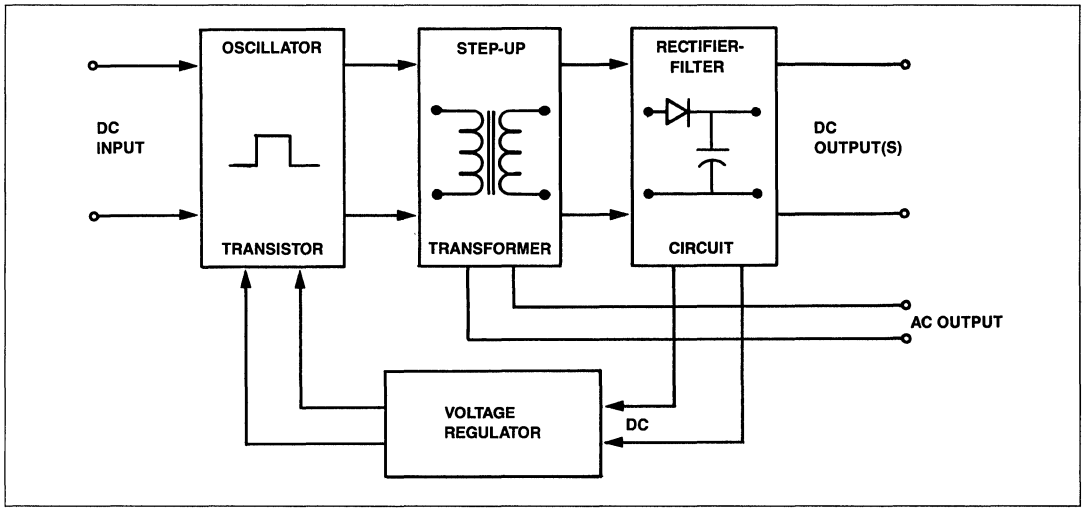
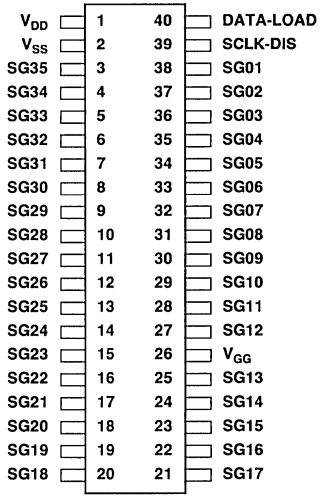


Figure 34. DC-DC Converter Power Source



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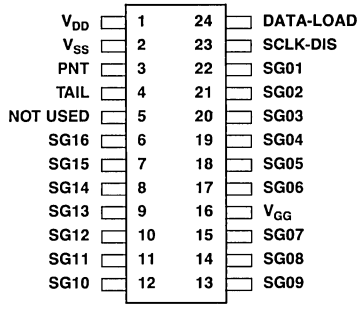
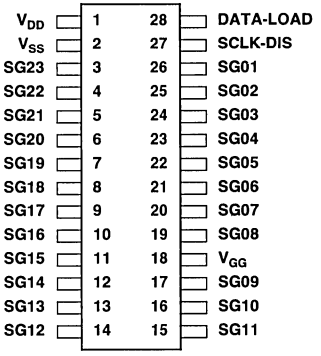
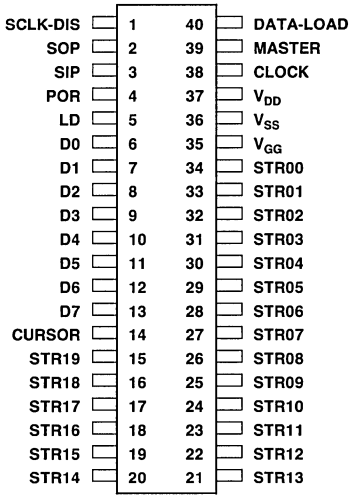
Multi-Chip Display Controller



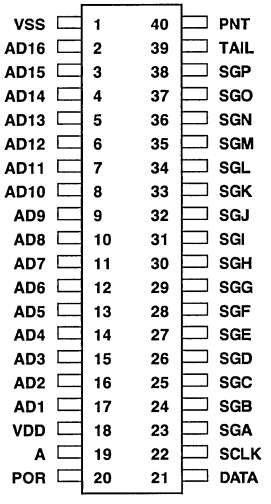
10941
Anode Driver
Multi-Chip Display Controller



10942 and 10943
Anode Driver
Multi-Chip Display Controller



10939
Grid Driver
Multi-Chip Display Controller



10937, 10951 and 10957
Single Chip Display Controller

Figure 35. Pin Configurations of Intelligent Display Controllers

REFERENCES

1. Application Notes
   - A Dot Matrix Controller System Design using the 10938/10939 Display Drivers and R6500/1EB Microcomputer," Rockwell International, APP Note Order No. 2163, P.O. Box C, Newport Beach, CA 92660.
   - "Vacuum Fluorescent Display," Application Notes AP-01 through AP-05. Noritake Electronics (See Reference 2.)

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TWX: 910 950-0077

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Anaheim, CA 92807
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(818) 407-4100

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Costa Mesa, CA 92626
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(818) 459-5500

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1012
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1182
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