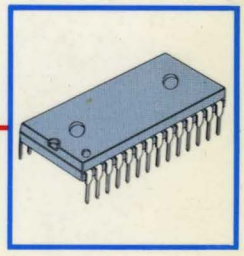
SAMSUNG

Data Book

MPR

(Microprocessor Peripheral)

1990



SAMSUNG
DATA BOOK LIST

I. Semiconductor Product Guide

II. Transistor Data Book

- Vol. 1: Small Signal TR
- Vol. 2: Bipolar Power TR
- Vol. 3: TR Pellet

III. Linear IC Data Book

- Vol. 1: Audio/CDP/Toy
- Vol. 2: Video
- Vol. 3: Telecom
- Vol. 4: Industrial
- Vol. 5: Data Converter IC

IV. CMOS Consumer IC Data Book

V. High Speed CMOS Logic Data Book

VI. MOS Memory Data Book

VII. SFET Data Book

VIII. MPR Data Book

IX. CPL Data Book

X. Dot Matrix Data Book

MICROPROCESSOR PERIPHERAL

Data Book

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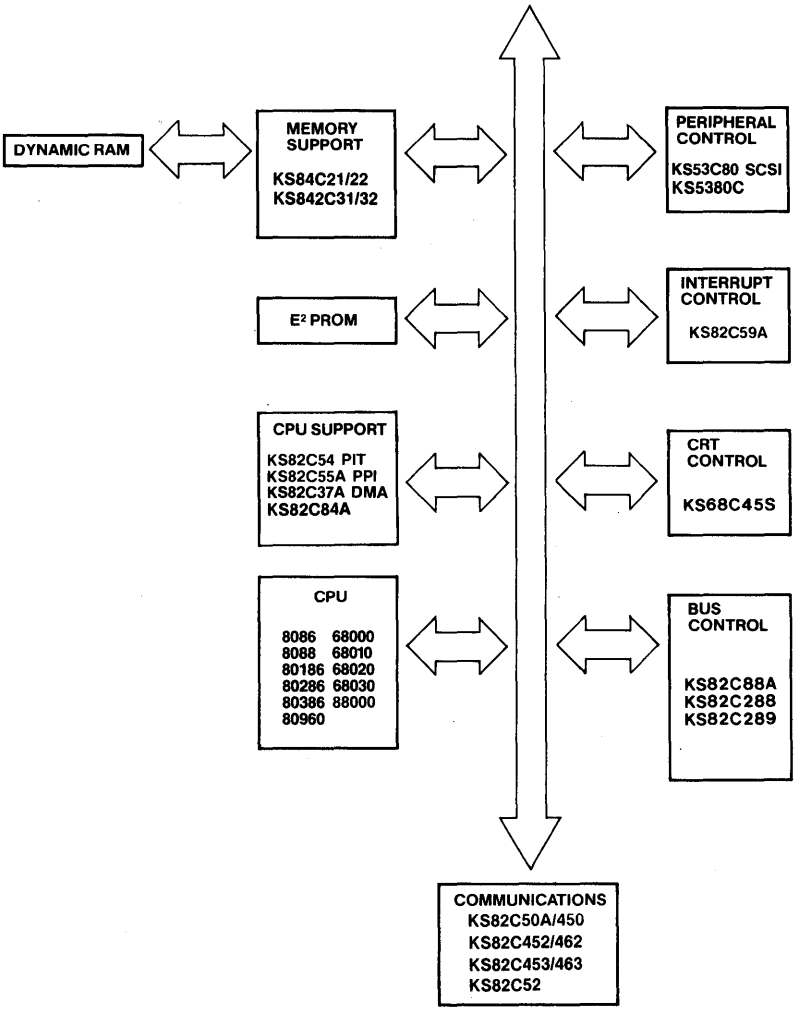
OVERVIEW

Samsung microprocessor peripherals provide a complete solution to increasing complex and performance-oriented applications environment. Standard functions in high performance CMOS technology reduce designers time-to-market by shortening design, testing and debug activities.

At Samsungs world class manufacturing facilities in Korea and San Jose, product reliability and failure rates are carefully monitored. This emphasis on manufacturing products of the highest quality and reliability translates into higher system reliability, reduced down time and reduced repair costs.

Our advanced CMOS technology,CSPIIA, provides performance levels to match today's high speed microprocessors. CSPIIA features dual-layer metal, single-layer poly, and features sizes down to 2μ drawn. This 11 mask process results in cost-effective manufacturing to produce high performance CMOS building blocks at competitive prices. Figure 1 summarizes microprocessor support from Samsung peripheral products.

SAMSUNG'S TOTAL SYSTEM SOLUTION



ALPHA NUMERIC INDEX

CROSS REFERENCE GUIDE

AMD	SAMSUNG
AM5380	KS53C80
D8237A D8237A-4 D8237A-5	KS82C37A-5 KS82C37A-5 KS82C37A-5
D82C54-8 D82C54-10	KS82C54-8 KS82C54-10
D8255A-2 D8255A-3	KS82C55A-5 KS82C55A-5
D8259A-5 D8259A-8	KS82C59A-8 KS82C59A-8
D8284A-8 D8284A-10	KS82C84A-8 KS82C84A-10
D8288-5	KS82C8A-5

HARRIS	SAMSUNG
82C37A-5 82C37A-8	KS82C37A-5 KS82C37A-8
82C52	KS82C52
82C54-8	KS82C54-8
82C55A-5 82C55A-8	KS82C55A-5 KS82C55A-8
82C59A-5 82C59A-8	KS82C59A-8 KS82C59A-8
82C84A-8	KS82C84A-8
82C88-5 82C88-8	KS82C88A-5 KS82C88A-8

INTEL	SAMSUNG
82C37A 82C37A-4 82C37A-5	KS82C37A-5 KS82C37A-5 KS82C37A-5
8255A 8255A-5	KS82C55A-5 KS82C55A-5
82C54A	KS82C54-8
82C55A-8 82C55A-8	KS82C55A-8 KS82C55A-8
82C59A 82C59A-2 82C59A-8	KS82C59A-8 KS82C59A-8 KS82C59A-8
82C84 82C84A 82C84A-1	KS82C84A-5 KS82C84A-8 KS82C84A-10
82C88 8288	KS82C88A-8 KS82C88A-8

LOGIC DEVICES	SAMSUNG
L5380 L53C80	KS5380C KS53C80

MITSUBISHI	SAMSUNG
82C37A-4 82C37A-5	KS82C37A-5 KS82C37A-5
82C54-6 82C54-8	KS82C54-8 KS82C54-8
82C55A-5 82C55A-8	KS82C55A-5 KS82C55A-8
82C59A-5 82C59A-8	KS82C59A-8 KS82C59A-8

NCR	SAMSUNG
5380	KS53C80

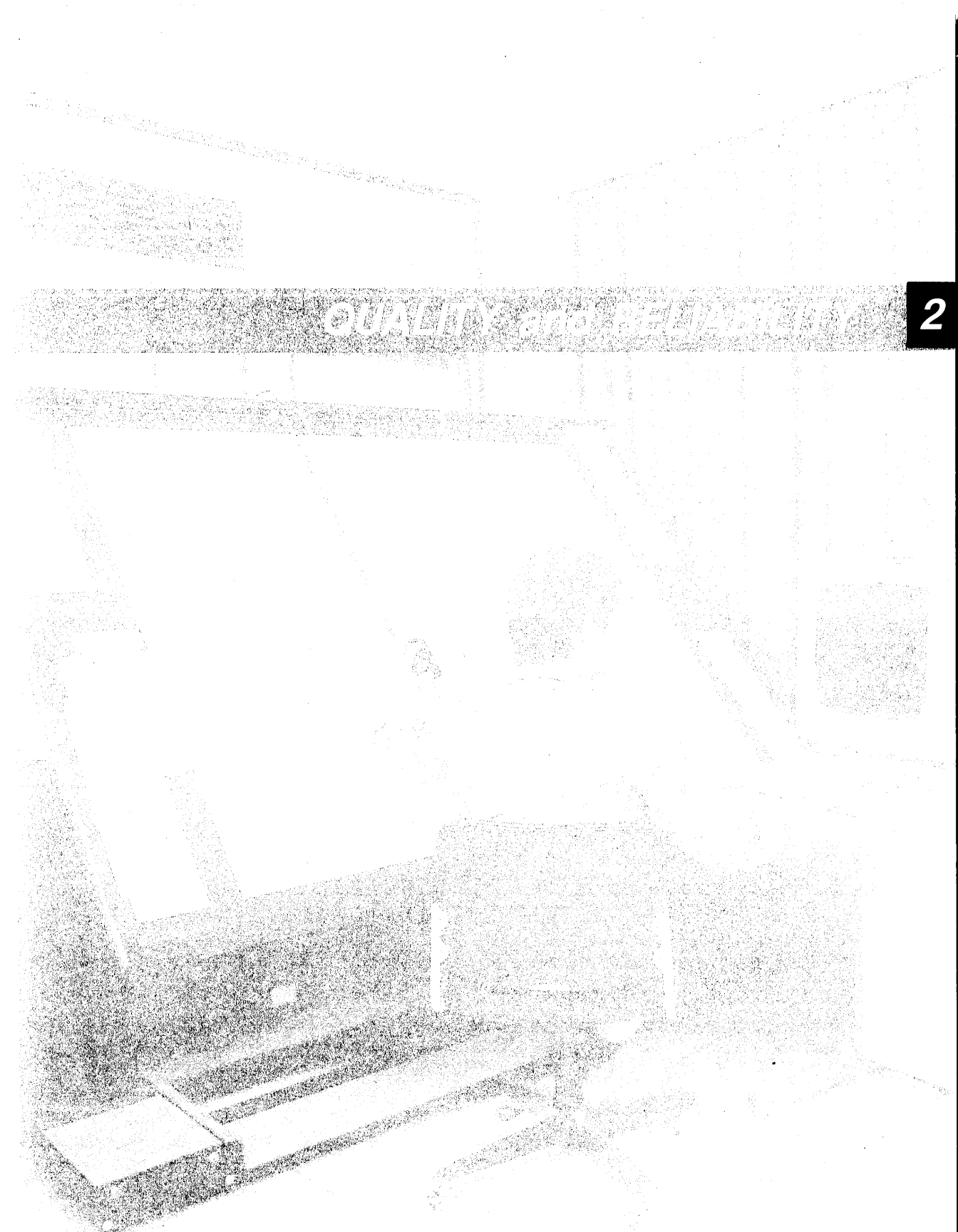
NEC	SAMSUNG
82C37A-5	KS82C37A-5
82C54-8	KS82C54-8
82C55A-8	KS82C55A-8
82C59A-8	KS82C59A-8
82C84A-8	KS82C84A-8
82C88-8	KS82C88A-8

OKI	SAMSUNG
M82C37A-5	KS82C37A-5
M82C54-8 M82C54-10	KS82C54-8 KS82C54-10
M82C55A-8	KS82C55A-8
M82C59A-5 M82C59A-8	KS82C59A-8 KS82C59A-8
M82C84A-5 M82C84A-8	KS82C84A-5 KS82C84A-8
M82C88-5 M82C88-8	KS82C88A-5 KS82C88A-8

UMC	SAMSUNG
UM8237A-3 UM8237A-4 UM8237A-5	KS8237A-5 KS82C37A-5 KS82C37A-5
UM8250A UM8250B	KS82C50A KS82C50A
UM8254-2	KS82C54-8
UM8255A	KS82C55A-5
UM8259A-5	KS82C59A-8
UM82C84AE-8 UM82C84AE-10	KS82C84A-8 KS82C84A-10
UM82C88-5	KS82C88A-5

QUALITY STANDARDS

2



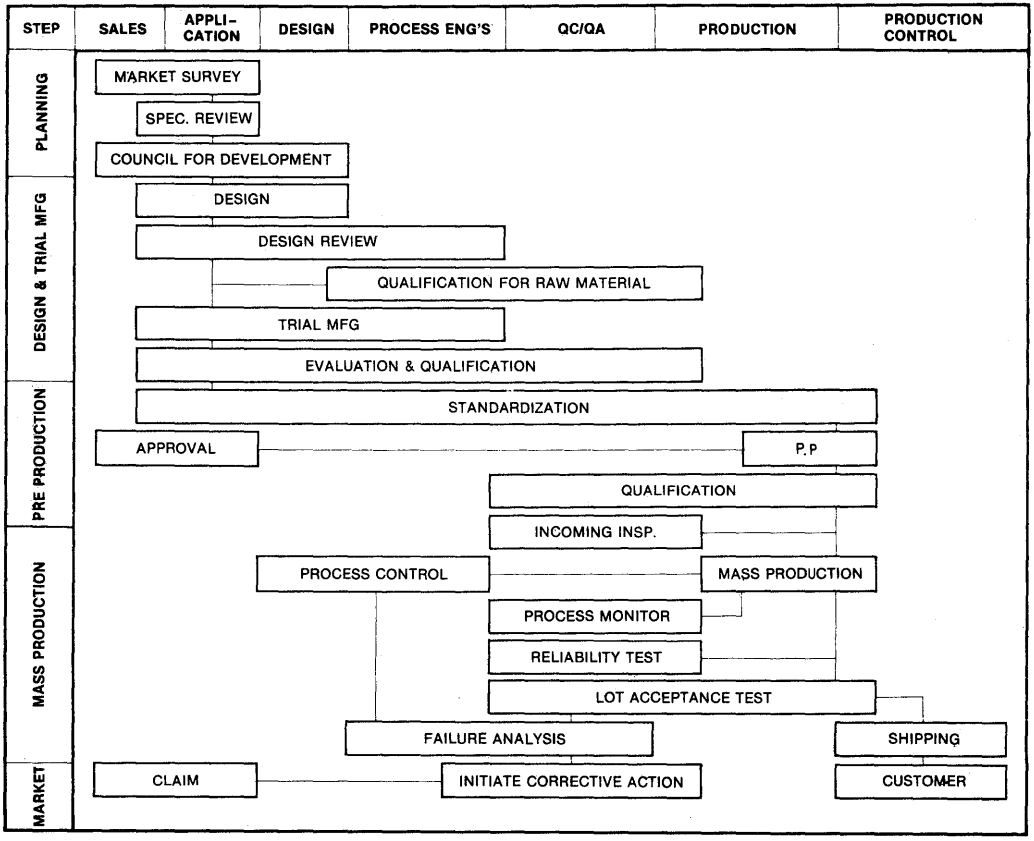
1. INTRODUCTION

SEC has been providing a wide variety of semiconductor products to the world since 1974. Since this time, extensive in-sights have been gained to create methods which most effectively result in reliable products. The worldwide customers of SEC have encouraged and helped develop the existing manufacturing and quality philosophy that is a way of life for SEC management and it's employees. This philosophy dictates the need for a zero defect environment through out SEC's processes leading ultimately to total customer satisfaction. By developing and using methods of Statistical Process Control and Statistical Quality Control, SEC has made great strides in improving product quality & reliability. The direct result of these improvements has been reduced product DPM (Defects Per Million) to levels below customer requirements. SEC's repeated ability to exceed requirements for customer's "Dock to Stock" programs and our commitment to all our customers needs, has made SEC the company to watch as we move ahead into the 1990's and beyond.

SEC's MPR products are among the most reliable in the industry. SEC has always made a commitment to achieve the highest possible quality, reliability, and customer satisfaction with its products. Extensive qualification, monitor and outgoing programs are used to scrutinize product quality and reliability. Stringent controls are applied to every wafer fabrication and assembly lot to achieve reproducibility, and therefore maintain product reliability.

In this chapter, the quality and reliability programs established at SEC will be discussed. In addition, a description of reliability theory, reliability tests and various support efforts provides a broad framework from which to comprehend SEC quality and reliability.

To better understand the Quality Department's role in product development and manufacturing, a detailed diagram is listed below. As can be noted, Quality Engineering is involved in all phases, save that of initial product planning.

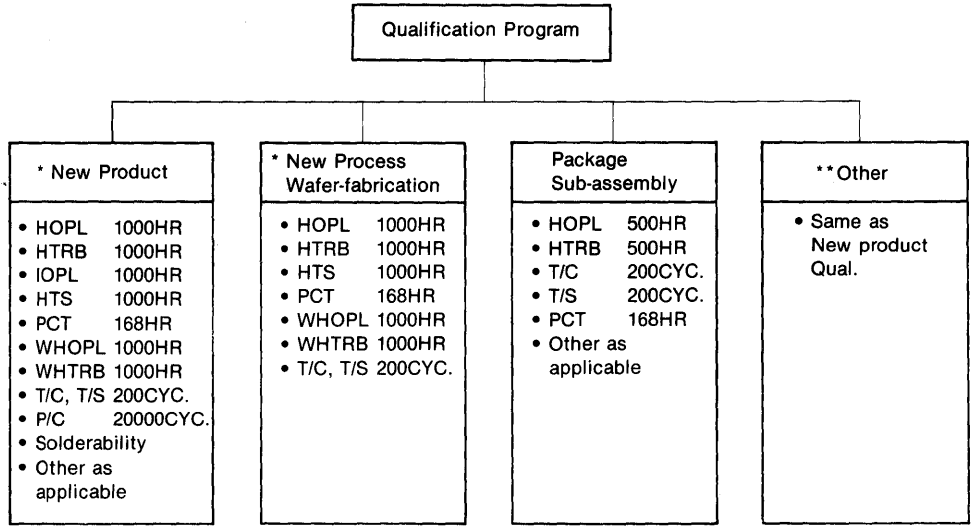


Quality Assurance During Development

2. QUALITY & RELIABILITY PROGRAM

2.1 QUALIFICATION

Procedures to qualify devices are listed below. There are both general and product-specific requirements. Procedures are detailed for new products, die-only qualifications, and package-only qualifications. The latter two are for products and/or packages already qualified, but where there is room for further product optimization.



*Testing time for each test items depends on the grade (group) of devices. (see the device group list 2.1 2))

** Design, Equipment, Material(s), etc....

1) PROCESS DEVELOPMENT QUALIFICATION

Purpose: To investigate the change of a process parameter and then apply it to a production process by reliability testing of a process which has been newly developed.

New Process, Wafer Fabrication Qualification

No	Test Item	Test Condition	Package	
			L-IC	Discrete
1	High Temperature Operating Life (HOPL)	$T_a = T_{opr}(max)$ $V_{CC} = V_{CC}(max)$ STATIC, DYNAMIC 1000HRS	YES	—
2	High Temperature Reverse Bias (HTRB)	$T_a = T_j(max)$ $V_{CB} = 0.8 \times V_{CBO}$ 1000HRS	—	YES
3	High Temperature Storage (HTS)	$T_a = T_j(max)$ 1000HRS	YES	YES
4	Pressure Cooker Test (PCT)	$T_a = 121°C \pm 2°C$ RH = 100% 15 PSIG 168HRS	YES	YES
5	Wet High Temperature Operating Life (WHOPL)	$T_a = 85°C$, RH = 85% $V_{CC} = V_{CC}(min)$ 1000HRS	YES	—
6	Wet High Temperature Reverse Bias (WHTRB)	$T_a = 85°C$, RH = 85% $V_{CB} = 0.8 \times V_{CBO}$ 1000HRS	—	YES
7	Thermal Shock (T/S)	$-65°C \rightleftarrows 150°C$ (Liquid) 5min, <10sec, 5min 200 cycles	YES	YES
8	Temperature Cycle (T/C)	$-65°C \rightleftarrows 150°C$ (Air) 10min, 10min 200 Cycles	YES	YES

When the results of a reliability test are good, the process characteristics good and the yield level is satisfied, the process can be applied to production. If there are any problems found in a process after it has been applied to production, the problem will be investigated in detail and the process will be revised. Once the process has been revised and approved it will again be applied to production.

2) PRODUCT DEVELOPMENT QUALIFICATION

Purpose: To develop a stable and uniform product that satisfies the customer's requirements for quality by using the exact reliability test specification called out for the new product.

Products are grouped according to the importance of their application.

Group 1	Group 2	Group 3
1. A/D, D/A Converter 2. IC for LCD 3. IC for PC 4. ASIC Master 5. Codec 6. MPR 7. IC for Exchange 8. New Products	1. Transistor 2. Regulator/OP AMP 3. IC for Telephone 4. Comparator/Timer 5. MICOM 6. Audio/Video IC 7. General Mos IC	1. ASIC Opinion Product 2. Toy/Melody IC 3. MICOM family 4. Products Except Group 1, Group 2 Products

New Product Qualification Test Items

No.	Test Item	Test Condition	Part		Reference Method	Note
			L-IC	Discrete		
1	High Temperature Reverse Bias (HTRB)	$Ta = T_j(max)$ $V_{CB} = 0.8 \times V_{CBO}$ 1000HRS	—	YES		
2	High Temperature Operating Life (HOPL)	$Ta = T_{opr}(max)$ $V_{CC} = V_{CC}(max)$ Static, Dynamic 1000HRS	YES	—	MIL-STD-883 1005	
3	High Temperature Storage (HTS)	$Ta = T_{stg}(max)$ 1000HRS	YES	YES		
4	Operating Life (OPL)	$Ta = 25°C$ $P_C = P_C(max)$ 1000HRS	—	YES	MIL-STD-750 1026.3	For Small-Signal Device
5	Intermittent OPL (IOPL)	$Ta = 25°C$ $P_C = P_C(max)$ 2min/2min On/Off 1000HRS	—	YES	MIL-STD-750 1036.3	
6	Power Cycle (P/C)	$\Delta T_j = 125°C$ 120Sec/120Sec On/Off 10000CYC.	YES	YES		For PWR TR, PWR IC
7	Pressure Cooker Test (PCT)	$Ta = 121°C \pm 2°C$ RH = 100% 15PSIG 168HRS	YES	YES		
8	Wet High Temperature Reverse Bias (WHTRB)	$Ta = 85°C$, RH = 85% $V_{CB} = 0.8 \times V_{CBO}$ 1000HRS	—	YES		
9	Wet High Temperature Operating Life (WHOPL)	$Ta = 85°C$, RH = 85% $V_{CC} = V_{CC}(min)$ Pdmin 1000HRS	YES	—		
10	Thermal Shock (T/S) (Liquid)	$-65°C \leftrightarrow 150°C$ 5min, <10Sec, 5min 200 Cycles	YES	YES	MIL-STD-883 1011	
11	Temperature Cycle (T/C) (Air)	$-65°C \leftrightarrow 150°C$ 10min, 10min 200 Cycles	YES	YES	MIL-STD-883 1011	
12	Solder Heat Resistance (S/H)	$Ta = 260°C \pm 5°C$ $t = 10 \pm 2$Sec	YES	YES	MIL-STD-750 2031.1	
13	Solderability	$Ta = 245°C \pm 5°C$ $t = 5 \pm 0.5$sec Reject is >10% uncovered surface	YES	YES	MIL-STD-883 2003	
14	Salt Atmosphere	$Ta = 35°C$, 5% NaCl 24HRS	YES	YES	MIL-STD-883 1009A	

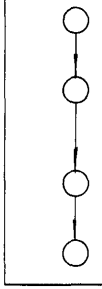
New Products Qualification Test Item (Continued)

No.	Test Item	Test Condition	Part		Reference Method	Note
			L-IC	Discrete		
15	Mechanical Shock	1500G, 0.5ms 3 Times Each direction of X, Y and Z Axis	YES	YES	MIL-STD-750 2016	For Hermetic
16	Vibration	20G, 3 Axis f = 20 to 2000 cps for 4 min, 4 cycles	YES	YES	MIL-STD-883 2007	For Hermetic
17	Constant Acceleration	2000G X,Y,Z Axis 1min for each Axis	YES	YES	MIL-STD-883 2001	For Hermetic
18	ESD (Human Body Model)	R = 1.5kΩ C = 100pF 5 Discharge V ≥ ± 1000V	YES	YES	MIL-STD-883 3015	
19	Latch-up Test		YES	—	—	For CMOS
20	Fine Leak Gross Leak	Helium Fluoro Carbon	YES	YES	MIL-STD-883 1014	For Hermetic

Note) • SOT-23, TO-92S PKG: PCT-48HR

3) PACKAGE DEVELOPMENT QUALIFICATION

Purpose: Whenever a new package type is developed, it must meet the specifications for devices that have been qualified and have maintained certain specified quality levels before the new package type may be applied to production.

Flow	Contents	Remarks
	Beginning of PKG development	Select representative device for product group (proceed at least 2 lots)
	Ass'y Qual	• Push Test • MPT • Die Thick • Dimension • Bond Pull • X-Ray • Lead Torque • Solderability
	Reliability Qual	• HTRB (TR) • PCT • Vibration • HOPL (IC) • LTS • M/S • T/C • S/H • Const
	Approvement of Qual	• New PKG Development will be approved when Rel qual is good for 500HR.

Package Sub-Assembly Qualification Test Items

No.	Test Item	Test Condition	Package		Notes
			Plastic	Hermetic	
1	High Temperature Reverse Bias (HTRB)	$Ta = T_j(max)$ $V_{CB} = 0.8 \times V_{CBO}$ 500HRS	YES	YES	For Discrete
2	High Temperature Operating Life (HOPL)	$Ta = T_{opr}(max)$ $V_{CC} = V_{CC}(max)$ Static, Dynamic, 500HRS	YES	YES	For IC
3	Temperature Cycle (T/C)	$-65°C \rightleftarrows 25°C \rightleftarrows 150°C$ 10min, 5min, 10min 200 CYCLES	YES	YES	
4	Pressure Cooker Test (PCT)	$Ta = 121°C \pm 2°C$ RH = 100%, 15PSIG 168HRS	YES	—	
5	Thermal Shock (T/S)	$-65°C \rightleftarrows 150°C$ (Liquid) 5min, < 10sec, 5min 200 CYCLES	YES	YES	
6	Solder Heat Resistance (S/H)	$260°C \pm 5°C$ 10 ± 1 sec Once without Flux	YES	YES	
7	Vibration (Variable-Frequency)	100 ~ 2000 ~ 100Hz 20G, 5min, 5Times, X, Y, Z	—	YES	For Discrete, others as applicable
8	Mechanical Shock (M/S)	1500G, 0.5ms 3 Times, X, Y, Z	—	YES	same as above
9	Constant Acceleration	20000G X, Y, Z Axis 1 min for each Axis	—	YES	same as above

4) CHANGE QUALIFICATIONS:

Purpose: To apply changes to production processes and designs by evaluating the quality levels for those processes and designs of devices in production.

Classification		Change
Design		Change of more than 1EA MASK for the product in production.
Process	Ass'y	• D/A • Coating • W/B • Mold
	Diffusion	• Diffusion/Photo/Etch, etc. • Metalization • Passivation

Procedure: Issuance of EIN for the change → Review of initial characteristics → Reliability test → Issuance of ECN (register of specification) → Application for production. Evaluation level: LTPD 10% (1/2)

2.2 MONITOR PROGRAM

1) ON GOING PROCESS CONTROL

All parameters of each process are controlled by SPC (Statistical Process Control). All resultant SPC data is gathered by computers and recorded automatically. Trends of each parameter are plotted on control charts by the computer and corrective actions are immediately taken whenever a parameter goes "out-of-control" beyond the control limits.
Whenever a parameter goes "out-of-control" in a process, engineers involved with that particular process have meetings to decide the disposition of those lots that were effected by the out-of-control process and corrective actions are implemented. In the case of critical defects, all lots are scrapped by MRB (Material Review Board).
As the key item of ongoing process control, Cp or Cpk value is controlled by computer for each process. The UCL and LCL for each process is then determined by the computer generated Cp or Cpk value. Cp or Cpk values are continually upgraded to insure the stabilization of process and a QIP (quality improvement plan) is made out to drive defects down to zero.
Process capabilities of each process are totaled and analyzed and those results of analysis are reflected on the QIP. The stabilization and maximization of process capabilities are driven by SPC.

2) PRODUCT RELIABILITY MONITOR

The reliability monitor program begins where the qualification program ends, at the start-up of limited production. Everything that is subject to qualification is considered subject to the monitor program. Generally, the product to be used for reliability monitors is gathered from each fab lot each month, where the product selected is representative of:

1) each fab process technology
2) each generic product type
3) each package technology
4) each subassembly plant

The product is shipped directly to the appropriate Q & R group, which puts the product through a series of electrical, mechanical, thermal, and environmental tests that usually are identical to those used initially for qualifying the product. Most tests are of short duration, but some may extend out to thousands of hours. Each month the test results are evaluated and problems, should they exist, identified.
Each monitor failure is analyzed. If a problem is detected where the failure rate is greater than that considered acceptable, or a reliability problem is suspected, a Material Review Board (MRB) is called. This meeting is attended by appropriate Q & R personnel, scheduling personnel, engineering, and any other affected group.
This group reviews the data, decides on disposition of the affected material, decides on appropriate corrective action, and basically controls the problem or issue until it is satisfactorily resolved.

3) FINAL QUALITY ASSURANCE PROGRAM

After the completion of the entire manufacturing process a sample of each lot is pulled and the data sheet verification test is repeated. This final verification objective is to ensure that test system to test system variations are not compromising the quality, and that inadvertent system or handling problems have not occurred.

4) ENVIRONMENT MONITOR

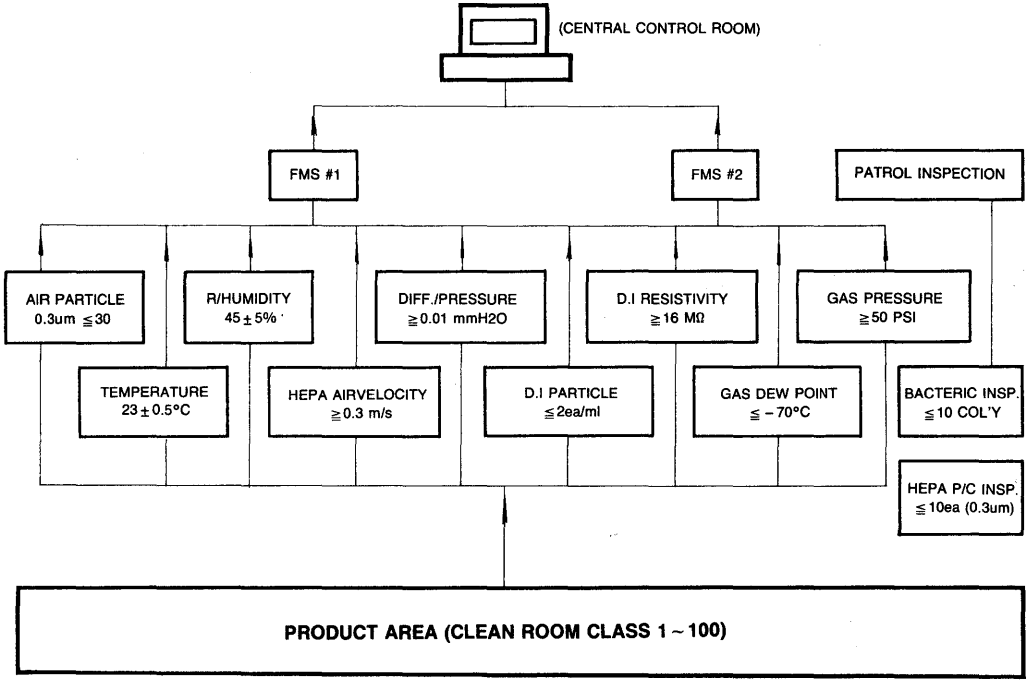
• **Instruments**

- F.M.S #1 (HIAC/ROYCO System 1 Set)
- F.M.S #2 (P.M.S System 1 Set)
- Control Particle Monitoring System (2 Set)

— On line monitoring system (Central control room)

- Portable Particle Counter, Sensors

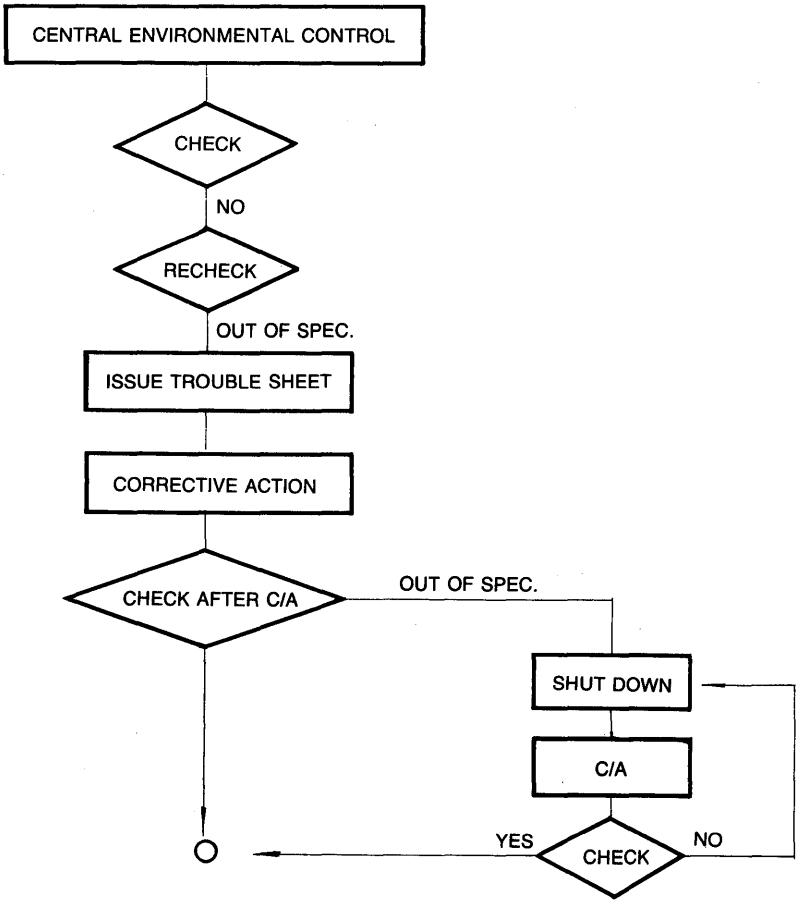
• **Block Diagram**



• **Environment Monitor**

Item	Frequency
1. Particle (Air, D-I Water)	5 min
2. Temperature, Relative Humidity	5 min
3. D.I Resistivity	5 min
4. Differential Pressure	5 min
5. HEPA Air Velocity	5 min
6. Gas (H_2, O_2, N_2, Air) Dew Point	5 min
7. Gas Pressure	5 min
8. HEPA Filter Particle	All HEPAs/1 room/Day
9. D-I Bacteria Main Lot	Weekly
10. D-I Bacteria Using Lot	Monthly

Corrective Action Requirement



2.3 QUALITY CONFORMANCE PROGRAM

1) DESCRIPTION

SEC has established a comprehensive reliability program to monitor and ensure the ongoing reliability of the MPR family. This program involves not only reliability data collection and analysis on existing parts, but also rigorous in-line quality controls for all products.
Listed below are details of tests performed to ensure that manufactured product continues to meet SEC's stringent quality standards. In line quality controls are reviewed extensively in later sections.
The tests run by the quality department are accelerated tests, serving to model "real world" applications through boosted temperature, voltage, and/or humidities. Accelerated conditions are used to derive device knowledge through means quicker than that of typical application situations. These acceierated conditions are then used to assess differing failure rate mechanisms that correlate directly with ambient conditions. Following are summaries of various stresses (and their conditions) run by SEC on Linear IC products.

2) HIGH TEMPERATURE OPERATING LIFE TEST (HOPL)

($T_j = 125°C$, $V_{CC} = V_{CC}$ max, static)

High temperature operating life test is performed to measure actual field reliability. Life tests of 1000HR to 2000HR durations are used to accelerate failure mechanisms by operating the device at an elevated ambient temperature (125°C). Data obtained from this test are used to predict product infant mortality, early life, and random failure rates. Data are translated to standard operating temperatures via failure analysis to determine the activation energy of each of the observed failures, using the Arrhenius relationship as previously discussed.

3) WET HIGH TEMPERATURE OPERATING LIFE TEST (WHOPL)

($Ta = 85°C$, R.H. = 85%, $V_{CC} = V_{CC}$ opt, static)

Wet high temperature operating life test is performed to evaluate the moisture resistance characteristics of plastic encapsulated components. Long time testing is performed under static bias conditions at 85°C/85 percent relative humidity with nominal voltages. To maximize metal corrosion, the biasing configuration utilizes low power levels.

4) INTERMITTENT OPERATING LIFE (IOPL)

(Pmax, 25°C, 2min on/2 min off)

This test is normally applied to scrutinize die bond thermal fatigue. A stressed device undergoes an "ON" cycle, where there is thermal heating due to power dissipation, and an "OFF " cycle, where there is thermal cooling due to lack of inputted power. Die attach (between die and package) and bond attach (between wire and die) are the critical areas of concern.

5) HIGH TEMPERATURE STORAGE TEST (HTS)

($Ta = 125°C$, UNBIASED)

High temperature storage is a test in which devices are subjected to elevated temperatures with no applied bias. The test is used to detect mechanical instabilities such as bond integrity, and process wearout mechanisms.

6) PRESSURE COOKER TEST (PCT)

(121°C, 15PSIG, 100% R.H., UNBIASED)

The pressure cooker test checks for resistance to moisture penetration. A highly pressurized vessel is used to force water (thereby promoting corrosion) into packaged devices located within the vessel.

7) TEMPERATURE CYCLING (T/C)

(−65°C to +150°C, AIR, UNBIASED)

This stess uses a chamber with alternating temperatures of −65°C and +150°C (air ambient) to thermally cycle devices within it. No bias is applied. The cycling checks for mechanical integrity of the packaged device, in particular bond wires and die attach, along with metal/polysilicon microcracks.

8) THERMAL SHOCK (T/S)

(−65°C to +150°C, LIQUID, UNBIASED)

This stress uses a chamber with alternating temperatures of −65°C to +150°C (liquid ambient) to thermally cycle devices within it. No bias is applied. The cycling is very rapid, and primarily checks for die/package compatibility.

9) RESISTANCE TO SOLDER HEAT

(UNBIASED, 260°C, 10 sec)

Solder Heat Resistance is performed to establish that devices can withstand the thermal effects of solder dip, soldering iron, or solder wave operations.

10) MECHANICAL SHOCK

(UNBIASED, 1500g, Pulse = 0.5msec)

This test determines the suitability of a device to be used in equipment where mechanical "shocks" may occur. Such shocks result from sudden or abrupt changes produced by rough (non-standard) handling, transportation, or field operations.

11) VARIABLE FREQUENCY VIBRATION

(UNBIASED, Range = 100 to 2000Hz)

Variable Frequency Vibration is done to model the effects of differential vibration in the specified range. Die attach and bonding integrity are particularly stressed, testing the mechanical soundness of device packaging.

12) CONSTANT ACCELERATION

(UNBIASED, 10kg to 20kg)

This is an accelerated test designed to indicate types or modes of structural and mechanical weaknesses not necessarily detectable in Mechanical Shock and Variable Frequency Vibration stressing.

13) RELATIVE STRESS COMPARISONS

Many stresses are run at SEC on many different devices. Through both theoretical and actual results, it was clearly determined which stresses were most effective. Also established were the stresses which weren't fully effective.

Comparisons have been made on the basis of defects able to be determined, efficiency in detection, and cost. For the reader's benefit, SEC provides the results of its conclusions on the following pages.

3. CUSTOMER SUPPORT SYSTEM

3.1 INTRODUCTION

Manufacturing companies have developed customer support systems for the purpose of uniting communications. Through these communications pass the information and knowledge required to satisfy the customers needs in areas such as quality and reliability, customer claims, customer training, field service technical issues, pricing or availability and above all, trust. Open lines of communication establishes thorough trust between the customer and vendor and are essential for such programs as dock-to-stock in order to achieve the ultimate in customer/vendor relations. SEC, in its commitment to customer satisfaction, has installed within its organization a support system that is designed to produce the open lines of communication between all facets of relations for both the customer and SEC.

3.2 POLICY

SEC has developed within its organization, a customer support system. SEC's policy requires that this system be manned with the proper personnel that are thoroughly trained in the areas that each represent and are dedicated to opening and maintaining lines of communication with the customer. Technical data used by SEC to support the customer must be up to date and always available for use by the customer (privileged or confidential information maybe excluded). Customer training is provided to the customer by only the most knowledgeable SEC personnel. SEC will provide customer field service in the form of periodic goodwill visits to customer sites or specialized problem solving services as required. Process change notification procedures as well as safety standards are also strictly adhered to.

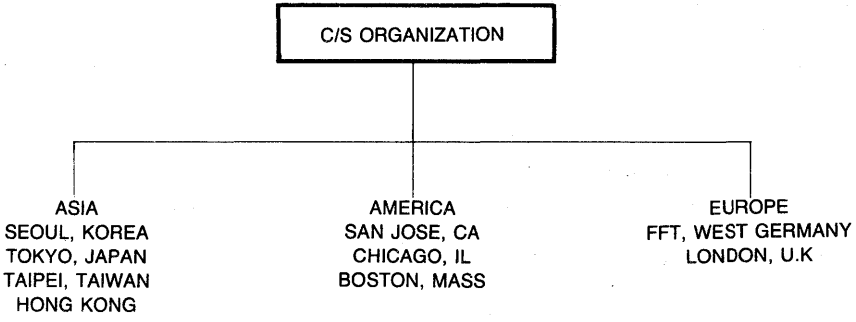
3.3 CUSTOMER SUPPORT SYSTEM

1) QUALITY ASSURANCE SERVICE

SEC has felt the need to reorganize its current Quality Assurance Sections in order to better service our customers. From this new organizational change, a new QA section was born. This new QA section, known as QA Section 3, was developed specifically for the customer. The customer service team in QA3, was organized to respond prombtly to customers quality requirements. The purpose of this team is to form a more responsive communication channel between plant R & D, the sales department and the customer. Customers will achieve satisfaction with our company's products by use of the newly organized customer service system. This service system is openly available to customers for comments concerning problems or opinions about SEC's devices. An 800 number is published on the inside of the handbooks cover.

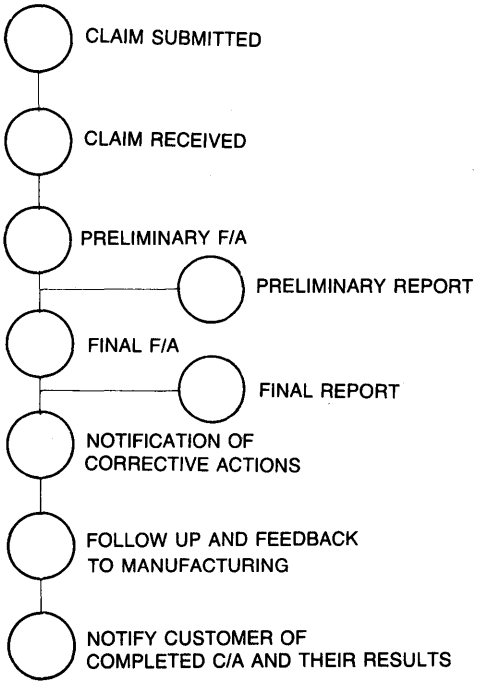
2) CUSTOMER SERVICE TEAM

The following organizational chart illustrates the world-wide base that the customer service team of SEC has established. Maintaining continuity between all of SEC's worldwide customer service teams is accomplished through the use of a newly installed computer network which allows constant communication between all teams.



3) CUSTOMER CLAIM SUPPORT SYSTEM

Information from the field concerning quality is an essential factor for the improvement of product quality. Equally important, is the investigation of field failures. Timely feedback of the results from the analysis is required to better service customers properly. This data also serves as a direct guide to the improvement of reliability and quality for both SEC and our customers.
The flowchart below demonstrates the process in which SEC currently follows for customer claims.



4) CUSTOMER TRAINING SYSTEM

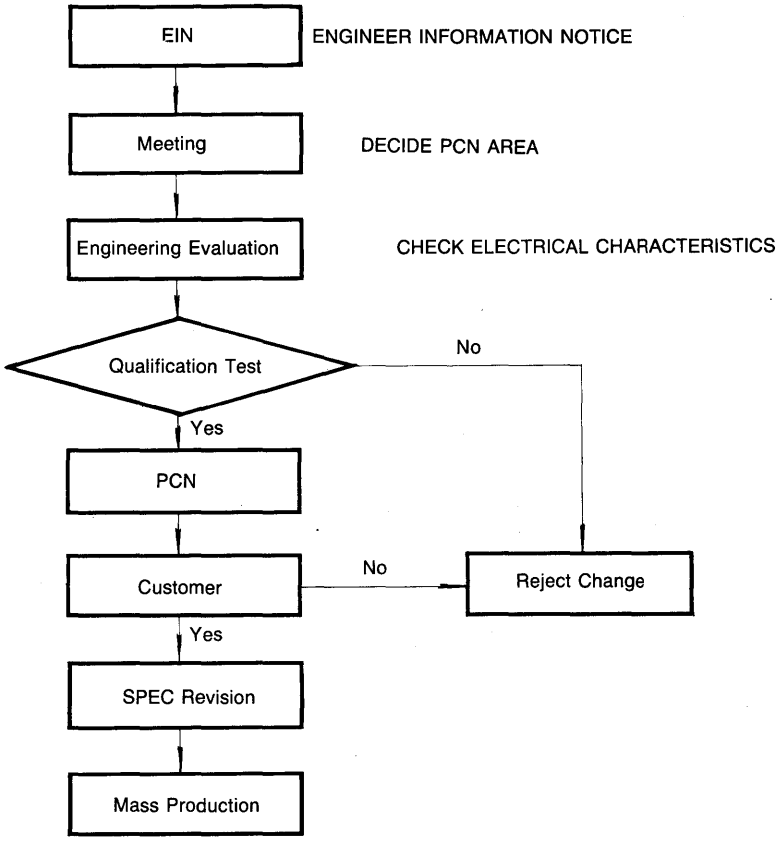
SEC has recently established a training team for the purpose of teaching SEC's customers the methods currently used by SEC to insure the product quality and reliability at the customers site. SEC offers this training in the form of group seminars or presentations and when requested or deemed necessary, individualized training is offered. In some cases, the training will take place at the customers site at the customers convenience while in other cases, SEC will extend on invitation to the customer to visit our manufacturing site.

5) CUSTOMER FIELD SERVICE

SEC has developed field service teams that are devoted to making customer contact when there aren't any problems. In other words, SEC is interested in making periodic goodwill visits. The visiting team would be comprised of those managers and engineers that are involved with the product types that the customer currently uses. The main goal of this team is to establish customer trust through communication.

3.4 PROCESS CHANGE NOTIFICATION SYSTEM (PCN)

Changes in a process are sometimes required to produce a higher quality product at a lower price. These changes can include new or different types of material, new or modified designs and new or different processes. SEC has developed a PCN procedure that is followed whenever a major or critical change is to be considered for any process. The idea behind the PCN is to allow change to a process by submitting the planned change for qualification by SEC engineering and then presenting the PCN to the customer for final approval. By following this procedure, the customer is assured that no major or critical change will occur to the process without the customers consent.



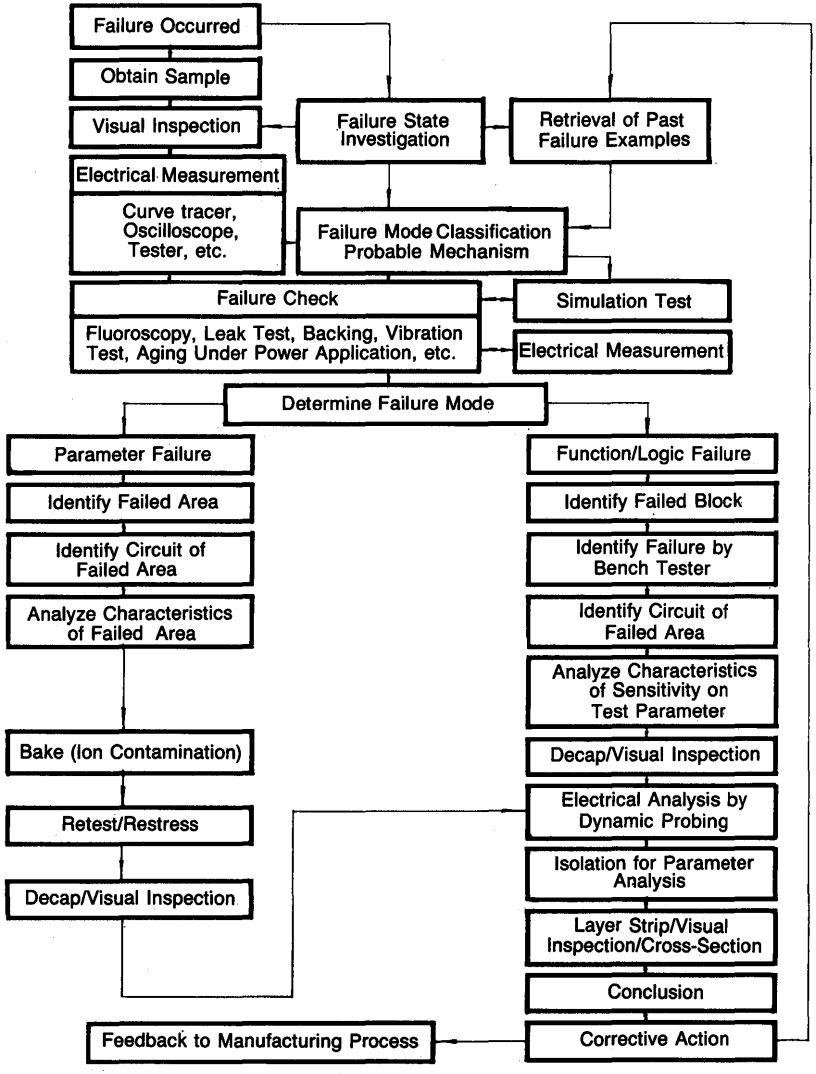
3.5 SAFETY STANDARDS

Most customers express the desire to use only products which have been manufactured with materials that meet the safety specifications of the Underwriters Laboratories. SEC has chosen to adhere to the specifications called out in the UL standard 94 by purchasing and using only those plastic materials that conform to this standard. UL 94 tests for a number of different flammability conditions that effect the plastic material used in semiconductor devices including horizontal burning, vertical burning and flame spread.

4. FAILURE ANALYSIS

4.1 PROCEDURE

A general failure analysis procedure is shown below. The method demonstrated in the flow chart applies to all rejects. However, each analysis is specific unto itself, so that a completely exhaustive analytical flow is impossible for the limits of this manual. Specific instances and examples of interest are provided later in the chapter. Also included in this section is a typical day-by-day accounting of a failure analysis in progress. A two-week turnaround is the objective, with greater than 90% of analysis lasting equal to or less than this duration. A sample analysis plan and report are attached at the conclusion of this section.



Failure Analysis Procedure Flow Chart

Applicable Comments for the above flow chart are made below.

1) DETERMINATION OF FAILURE MODE

The basic failure mode shall be determined with data from computer and bench testing. As a defect can represent various electrical failure modes, it is critical to determine the most basic failure mode. (For example, a V_{OL}/V_{OH} parameter failure may be also analyzed as a functional failure. However, it is very important to determine V_{OL}/V_{OH} as the basic failure mode.)

2) IDENTIFICATION AND ANALYSIS OF FAILED CIRCUIT AREA

Correlation shall be derived with general (macroscopic) failure phenomenon through circuit interpretation of the failed area.

3) SENSITIVITY OF TEST

Parametric value of failed sample shall be determined through adjusting DC and AC parameters, temperature range, etc.

4) ION CONTAMINATION

For a sample assumed to have an inversion phenomenon caused by ionic contamination, characteristics shall be identified by conducting a Ta = 150°C, 24 hour cure and repeating test/restress.
Contamination of a specific layer shall be determined by stripping each layer.

5) DECAPSULATION

There are 5 decap methods with respective merits and demerits. The appropriate method must be utilized on the basis of the characteristics and potential cause for each failure.

6) ISOLATION AND DYNAMIC PROBING

It is essential to isolate the probable failing part of the circuit for its electrical failure mode. Without isolation, exact detection of a failed part can not be accurately accomplished as an electrical failure mode has an influence on other parts of the circuit.

7) LAYER STRIPPING

Each layer strip should meet specification requirements with respect to time. It should never be the case that chemical attack is mistaken for causing the failure of a part.

8) GENERATION OF ACTIVATION ENERGY

Accelerated life testing requires generation of actual activation energies based upon establishing a definitive failure mode. This generation has a great effect in determining the acceleration factor of Arrehenius' model.

9) CORRECTIVE ACTION

Failure analysis is fully completed only by establishing a future plan and corrective action, which are taken to resolve a problem and prevent its recurrence.

4.2 Failure Modes and Mechanisms

1) Failure mechanisms for devices vary widely. They are caused by both front-end (wafer) and back-end (assembly) processing. To classify problems and their instigations, the table listed below is provided.

Items and Causes of Failure Modes

Item	Type of Failure	Failure Mode	Cause
Wire Bonding	Wire Disconnection	Open	Incomplete Manufacture or Misuse
	Wire Short	Short	
	Purple Plague	Open, High Resistance	
	Bond Detaching	Open, High Resistance	
	Misplaced Bonding, Loose Contact	Open, High Resistance Short	
	Improper Bond Shape Erroneous Bonding	Open, High Resistance Open, High Resistance	Incomplete Manufacture
Junction Region	Destruction by Surge	Low Breakdown Voltage, Short, Open	Incomplete Manufacture or Misuse
	Hot Spot		
Case	Lead Disconnection	Open, High Resistance	Same as above
	Lead Short	Short, High Leakage	
Seal	Incomplete Seal	Breakdown Voltage Deterioration, High Leakage	Same as above
	Enclosed High Humidity Gas		
	Contamination of Surface		
	Dust and Dirt	Short, Low Breakdown Voltage Large Leakage	
Metallization	High Current Density	Open, Short	Misuse
	Electromigration	Open, High Resistance	
	Scratch	Open, Short	Incomplete Manufacture
	Insufficient Thickness Excessive Etching	Open, High Resistance	
	Contamination, Dust and Dirt	Open, High Resistance	Incomplete Manufacture or Misuse
	Poor Wiring and Element Connection		
Chip Mounting	Chip Crack	Open, Short	Same as above
	Chip Detaching	Open, Short, High Thermal Resistance	
Oxidized Film	Pinhole, Crack	Low Breakdown Voltage, Short	Incomplete Manufacture
	Insufficiently Oxidized Film Thickness	Low Breakdown Voltage	
Surface Treatment	Channel Formation	Low Breakdown Voltage High Leakage	Same as above
	Contamination		
Mask	Insufficient Photoresist	Low Breakdown Voltage Short, Open, High Leakage	Same as above
	Mask Misalignment		
Material and Diffusion	Improper Impurity Density	Same as above	Same as above

2) Standard product reliability tests can naturally generate failures. Here, in this section, a table is given which lists tests and their associated rejects. Each test has a specific purpose, and if there exists a particular product weakness, a given test will expose it. In this manner, by knowing a test and it's function, a clear determination can be made as to the relevance of a failure for that particular test.

Reliability Tests and Associated Failure Modes

	Failure Cause	Diffusion	Oxide	Metalization	Wire Bonding	Package Environment	Package Seal	Lead Fatigue	Solderability	Mark	Die bonding
Item	Test Condition	•Contamination •Crystal Defect •Photoresist Reject	•Contamination •Pin Hole •Crack •Thickness Unstable	•Conpos. •Scratch •Void •Open	•Interface •Corrosion •Misbonding •Wire Open •Chemical Interface	•Conductive ions •Inadequate •Environments	•Sealing Reject	•Conpos.	•Marking	•Themal Reject	Resistance Reject •Crack •Chip Position Reject
T/C	−65°C→150°C 200 Cycles		0	0	0		0				0
T/S	−65°C→125°C 200 Cycles		0	0	0		0				0
Moisture Resistance	90-98%R.H./65°C3HRS 80-98%R.H./25°C8HRS 90-98%R.H./65°C3HRS 10 Cycles		0	0	0	0	0				
Vibration Fatigue	20G-3 Axis Orientation f=20 to 2000 cpe for 4 min. 4 cycles				0	0					0
Constant Acceleration	Pulse Duration: 0.1-1m sec Shock pulse: 0.5-3Kg				0						0
Mechanical Shock	1500g, 0.5ns Each Direction of X, Y and Z Axis				0						0
Lead Integrity	W=227g 90°C 3 times						0				
Marking	Isoprophylalcohol									0	
Solderability	Ta=230° 5 Sec. Once With Flux								0		
Salt Spray	Ta=35°C, 5% NaCl				0				0		
OPL	Individual Spec	0	0	0	0	0					0
IOPL	Individual Spec	0	0	0	0	0					0
HTRB	Individual Spec	0	0	0	0	0					0
HTS	Individual Spec		0		0	0			0		
WHTS	80°C, 90% RH 85°C, 85% RH		0	0			0	0	0		
WHTRB	85°C, 85% RH Bias	0	0	0	0	0	0	0	0		0

3) An anomalous manufacturing step can manifest itself in many ways with respect to product reliability. The chart below depicts process steps, the types of rejects they can generate, and the way to defect such failures. Of course, there are numerous QC and Production checks along all stages of the manufacturing process. However, a semiconductor product typically involves so many operations it's nearly impossible to detect all potential reliability hazards. Thus, there are final electrical and visual tests, reliability tests, and statistical analyses which are run prior to product releasal. The chart below speaks to the electrical, visual, and reliability tests.

Failure Mechanisms of Integrated Circuits

Process Step Affecting Reliability	Failure Mechanism	Failure Mode	Failure Detection Method
Wafer Fabrication	Dislocation and Stacking Fault	Degradation of Function Characteristics	Electrical Test Operation Life
	Non-Uniform Resistivity	Unpredictable Characteristic Values	Electrical Test
	Surface Abnormalities	Improper Electrical Characteristics, Short and Open	Electrical Test Operation Test
	Cracks, Chips, Scratches (Usually Caused During Handling)	Open and Short	Electrical Test Visual Inspection (Before Seal) Temperature Cycling
	Contamination	Degradation of Junction Characteristics	Visual Inspection (Before Seal), Temperature Cycling, High Temperature Storage, Reverse Bias
Passivation	Cracks and Pin Holes	Shorts, Low Breakdown Voltage	Temperature Cycling High Temperature Storage High-Voltage Test, Operation Life Visual Inspection (Before Seal)
	Non-Uniformity of Film Thickness	Low Breakdown Voltage Increase of Leakage Current in Oxide Film	Same as Above
Mask	Scratch, Crack, Scar of Photo Mask	Open, Short	Visual Inspection (Before Seal), Electrical Test
	Misalignment	Open, Short	Same as Above
	Abnormality of Photo-Resist Pattern (Line-Width, Space, Pin Hole)	Degradation of Characteristics Due to Parameter Drift Open, Short	Same as Above
Etching	Improper Elimination of Oxide Film	Open, Short, Intermittent Failure	Visual Inspection (Before Seal) Electrical Test Operation Life
	Under-Cut	Short or Open in Metallization	Visual Inspection (Before Seal) Electrical Test

Failure Mechanisms of Integrated Circuits (Continued)

Process Step Affecting Reliability	Failure Mechanism	Failure Mode	Failure Detection Method
Etching	Spotting (Smear) Inhomogeneous Etching	Latent Short	Visual Inspection (Before Seal) Temperature Cycle, High Temperature Storage Operation Life
	Contamination (Photo Resist, Residue of Chemical Substance)	Low Breakdown Voltage Increase of Leak Current	Same as Above Reverse Bias
Diffusion	Improper Control of Doping Profile	Performance Degradation Caused by Instability and Fault	High Temperature Storage Temperature Cycling Operation Life Electrical Test
Metallization	Scratched and Smeared Metallization (Caused During Handling)	Open and Short	Visual Inspection (Before Seal) Temperature Cycling Operation Life
	Thin Metallization Due to Insufficient Deposition or Oxide Film Step	Open or High Impedance Internal Connection	Electrical Test Operation Life Temperature Cycle
	Oxid Film Contamination Material Incompatibility	Open Metallization Caused by Poor Adhesion	High Temperature Storage Temperature Cycling Operation Life Test
	Corrosion (Residue of Chemical Substance)	Open Metallization	Visual Inspection (Before Seal), High Temperature Storage Temperature Cycle, Operation Life
	Displacement Contaminated Contact	High Contact Resistance, Open	Visual Inspection (Before Seal), Electrical Test, High Temperature Storage Temperature Cycle, Operation Life
	Improper Temperature and Period for Metallization	Peeled Metallization Poor Adhesion Short	Electrical Test High Temperature Storage Temperature Cycle Operation Life
Die Separation	Cracks and Chips Caused by Improper Dicing	Open	Visual Inspection (Before Seal) Temperature Cycling Thermal Shock Vibration Shock

Failure Mechanisms of Integrated Circuits (Continued)

Process Step Affecting Reliability	Failure Mechanism	Failure Mode	Failure Detection Method
Die Bonding	Void Between Header and Die	Degradation Due to Overheating	Radiography, Operation Life Constant Acceleration Shock, Vibration
	Over-Spreading of Eutectic Solder	Short, Intermittent Short	Visual Inspection (Before Seal), Radiography, Vibration Shock
	Poor Bonding of Die to Header	Die Crack and Lifting	Visual Inspection (Before Sealing), Constant Acceleration, Shock, Vibration
	Mismatching of Materials	Crack or Peeling of Die	Temperature Cycling High Temperature Storage Constant Acceleration
Wire Bonding	Poor Bonding Strength	Open Wire, Open, Lifting Vibration Shock	Constant Acceleration
	Mismatched Material and Contaminated Bonding Pad	Lead Bond Peeling	Temperature Cycling High Temperature Storage Constant Acceleration Shock, Vibration
	Formation of Intermetallic Plague	Open Bonding	High temperature storage, Temperature Cycling. Constant Acceleration Shock, Vibration
	Insufficient Bonding Area or Spacing	Open Bonding Short	Operation Life Test, Constant Acceleration, Shock Vibration, Visual Inspection (Before Seal)
	Improper Bonding Arrangement	Open, Short	Visual Inspection (Before Seal) Electrical Test
	Die Cracks or Chips	Open, Shock	Visual Inspection (Before Seal) High Temperature Storage Temperature Cycling Constant Acceleration, Shock Vibration
	Excessive Loop or Sag in Wire	Short to the Case, Substrate or other Parts of the Leads	Visual Inspection (Before Seal), Radiography, Constant Acceleration, Vibration
	Crack, Scratch, or Scar on Lead	Wire Disconnection Causing Open, Short	Visual Inspection (Before Seal), Constant Acceleration, Shock Vibration

Failure Mechanisms of Integrated Circuits (Continued)

Process Step Affecting Reliability	Failure Mechanism	Failure Mode	Failure Detection Method
	Insufficent Elimination of Tail Wire	Short, Intermittent Short	Same as Above Radiography
Sealing	Incomplete Hermetic Seal	Performance Degradation, Shorts and Opens Caused by Chemical Corrosion and Moisture	Fine Leak, Gross Leak
	Bad Atmosphere in Package	Performance Degradation Due to Inversion Layer Channeling	Operation Life Reverse Bias, High Temp. Storage, Temperature Cycling
	Bending or Breaking of the External Lead	Open	Visual Inspection, Lead Fatique
	Crack or Void in Seal Glass	Short or Open in Metallization Due to Leak	Seal, Electrical Test High Temperature Storage Temperature Cycling High Voltage Test
	Migration on Seal between Outer Lead and Metal Case	Intermittent Short	Low Voltage Test
	Electro-Conducting Particles Floating in Package	Same as Above	Constant Acceleration, Vibration Radiography
	Mismarking	Inoperable	Electrical Test

4) Equipment

A listing of important equipment used for failure analysis is shown below in tabular from, SEC's committment to comprehensive analysis of all relevant rejects necessarily implies a usefulness for key analytical instruments. Constant efforts are made to both use and modify equipment to meet specialized investigations. However, only standard equipment, not a listing of hybrids (for confidential development purposes), is listed below.

Equipment for failure analysis

Category	Item	Application
Visual	1. Stereo Microscope	Use for visual inspection
	2. SEM (Scanning Electron Microscope)	Use to inspect the surface or cross-section of a device at high magnification. Through voltage contrast techniques, it is possible to analyze voltage levels while the device is operating
	3. Infrared Microscope	Using the infrared radiation emitted by a functioning device, a thermal map can be produced.
	4. X-Ray	Use to inspect the bonding wire of encapsulated devices.
	5. Metallugical Microscope	Inspect interconnects, contacts, bonds
	6. Radiographic Scope	Inspect bond wires, die attach

Equipment for failure analysis (Continued)

Category	Item	Application
Elemental Analysis	1. Auger Electron Spectrometer (AES)	Used to detect and analyze contamination on the surface of a die
	2. EDX Spectrometer	Used with SEM to analyze elements present in a device. This is done by measuring the energy distribution of X-rays produced by the interaction of primary electrons and the sample.
	3. Differential Interference Microscope	Used for elemental analysis
	4. Electron Probe Micro Analyzer (EPMA)	Used for current analysis
	5. Ion Micro Mass Analyzer (IMMA)	Spectral analysis of chemical constituents
	6. Surface Eveness Micrometer	Measures planarity
	7. Differential Scanning Calorimeter (DSC)	Permits the analysis of glasses and polymers-especially encapsulation resins-through the measurement of reaction heat
	8. Thermo Gravimetric Analyser	Used to determine the thermal stability of polymers and glasses by measuring variations in mass with temperature.
	9. Plasma Etcher	Used to open devices encapsulated in epoxy resins, to remove silicon nitride, and to remove thin oxide films
	10. Transmission Electron Microscope (TEM)	Used for elemental analysis and high resolution surface on spectron
	11. Surface Tunneling Microscope (STM)	Used for elemental analysis
	12. Electron Spectrometry for Chemical Analysis (ESCA)	Used for elemental analysis
	13. Secondary Ion Mass Spectroscope	Used for elemental analysis
Decapsulation System	1. Grinding Machines 2. Angle Lapping 3. Evaporation 4. Diamond Cutter (Cross Section Cutter) 5. Molding System 6. Jet-Etching System 7. Etching Solution 8. Hot Plates 9. Ventilation Hoods	Used to decapsulate devices, to cut the cross section of die, to remove a surface layer.

Equipment for failure analysis (Continued)

Category	Item	Application
Electrical Test	1. Curve Tracer 2. TR, IC, MOS Tester 3. ESD Simulator 4. LCR Meter 5. DC-Analyzer 6. Noise Tester 7. Logic State Analyzer 8. Manipulator Probe Ssytem 9. Electron Beam Tester 10. Hot Electron Analyzer 11. I.R Scope	Used to measure electrical characteristic of devices, to establish the cause of failure.
Stress Test	1. Temperature Probe System 2. Constant Temperature Oven 3. Ovenn for Oper Life Test 4. Humidity Oven 5. Vibration System	Used to stress or cure the failed devices to identify a failure mechanism. This is a very important tool for analyzing degradation phenomena and intermittent failures.

Methods and Equipment for Failure Analysis

Item	Contents of Inspection	Equipment for Analysis
External Visual Check	• Condition of Lead, Plating, Soldering, Welding Area • Mark, Date Code • Package damage • Solderability • Sealing	Stereo-Optical-Scope x 40 Optical Microscope x 100 Helium Leak Detector Gross Leak Detector (Using Fluorocarbon)
Electrical Test	• DC Parameter, AC Parameter Test • Function Test • Margin Test of Voltage and Temp. • Diode Characteristics between Each Pin • Disconnection, Short Circuit and / or Electrical Characteristic detected by the above Inspection	IC Tester Curve Tracer (HP4145) Oscilloscope DC Power Supply Oscillator (Sine Wave Pulse) Heat-Gun, Cooling Gas Spray Thermo-Spot
Radiography	• Internal Structure of Device is Checked Non-Destructively	Soft X-Ray
Decapping	• Internal Structure is observed after decapping	Metal Cutting Scissors, Nippers Cap opener, plastic etcher, Hot plate, Drill, HNO_3
Internal Visual Check	• Detection of Defective Spot on the Chip Surface • Detection of Discrepancy of Internal Connection (Metallization, Wire Bond -ing, Etc.) • Electrical Characteristics are Checked by Mechanical Prober • Detection of Hot Spot • Existence of Foreign Material	Optical Microscope Micro-Prober SEM Laser Cutter Infrared Micro Scanner Thermal Plotter Infrared Microscope
Internal Structure Analysis	• Cross Sectional Analysis of Chips to Observe Diffusion Layer of Oxide Film • Analysis of Metallic Elements • Removing of Over-Coating Glass and Aluminum Metallization	Optical Microscope SEM, MAX, AES, SAM, IMA Spectrometer Micro-Prober
Simulation Test	• Operational Test on Actual Equipment	Actual Electronic Equipment

4.3 FAILURE MODE EFFECT ANALYSIS (FMEA)

Failure Mode Effect Analysis is a method used for checking if measures are taken against every possible failure in the design, the manufacturing process, the operating method, etc. For this analysis, factors such as design, manufacturing process, packaging, and operating method are divided into small units, and its functions are clearly defined. All possible failure modes are listed for each item, its effect on the product and the cause of each failure is examined. Each item is then evaluated to clarify the corrective actionto be taken.
Table shows an example of FMEA in the manufacturing process of plastic encapsulated MOS LSI. The incident column pertaining to the Evaluation Points show the failure rate; Effectiveness column shows the impact of the effect by the failure of the product, device, or system; and Detectability shows the rate of detection of the failure. These are individually graded on the basis of ten points. The result is then evaluated by multiplying the points. The larger value indicates the importance of the item. A counterplan for each item is then specified and action taken.

Manufacturing Process FMEA Example (Plastic Encapsulated Products)

Process Name (Process Function)	Failure Mode	Failure Effect	Failure Cause	Counterplan
Al metallization	Improper thickness Lack of Al wiring Breakage defect	Electromigration open circuit	Operator's mis-handling, dirt/foreign matter attachment, poor adjustment of equipment	Improvement and adjustment of written working process, dust control of clean room, SEM test in the process
Glassivation	Lack of glassivation film, failure film thickness	Increased leak current, improper operation	Dirt/foreign matter attachment, operator's mishandling	Dust control of clean room, improvement and adjustment of written working process
Visual Inspection	Scratch, die crack, dirt, spot, residual resist	Open circuit, increased junction leak current	Mishandling of wafer, Misclearning of water	Improvement and adjustment of written working process
Assembly Process Die Selection	Die crack	Increased junction leak current, improper operation	Poor adjustment of equipment, operator's mishandling	Corrective action to device control operator, improvement and adjustment of written working process
Die Bonding	Die crack Die floating	Open circuit, increased junction leak current, improper operation	Operator's mishandling temperature too low	Corrective action to device control operator, improvement and adjustment of written working process, visual inspection
Wire Bonding	Open bonding, improper bonding position, shorted bonding wire	Open circuit, short circuit	Poor bonding strength, operator's mishandling, poor adjustment of equipment, looped bonding wire, shape defact	Improvement and adjustment of written working process, corrective action to device control operator, visual inspection

Manufacturing Process FMEA Example (Plastic Encapsulated Products) (Continued)

Process Name (Process Function)	Failure Mode	Failure Effect	Failure Cause	Counterplan
Sealing (Resin)	Open bonding wire, shorted bonding wire, package crack, corrosion	Open circuit, short circuit, defective appearance	Poor adjustment of equipment, insufficient cure	Ditto
Lead Surface Treatment (plating)	Poor metal-plating thickness, dirt	Poor soldering, poor contact	Operator's mishandling poor adjustment of equipment, insufficient cleaning	Adjustment of written working process, corrective action to control operator
Lead Formation	Abnormal shape, broken lead	Failure inserting in the printed substrate poor operation	Operator's mishandling poor adjustment of equipment	Ditto
Marking	Marking error illegible marking	Operating destruction	Operator's mishandling insufficient cure	Improvement and adjustment of written working process

1. KS53C80/KS5380C
2. KS68C45S
3. KS82C37A
4. KS82C450/50A
5. KS82C52
6. KS82C54
7. KS82C55A
8. KS82C59A
9. KS82C84A
10. KS82C88A
11. KS82C288
12. KS82C289
13. KS82C411
14. KS82C452/462
15. KS84C21/22
16. KS84C31/32

PRODUCT INDEX

PRODUCT FEATURES

- **Directly drives the SCSI bus**
- **Supports asynchronous operation, with data transfer rates of 1.5 or 3.0 megabytes per second**
- **Supports arbitration, selection/reselection**
- **Supports initiator and target roles**
- **Low-power CMOS technology**
- **Generates parity**

Processor Interface

- **Supports DMA or programmed I/O**
- **Generates optional interrupts**
- **Supports DMA transfers—normal mode or block mode**
- **Supports memory or I/O mapped interface**
- **Interfaces directly with the CPU**

PRODUCT OVERVIEW

The KS53C80 is a CMOS SCSI controller, designed to provide an interface between a central processing unit, and the physical layer of the Small Computer System Interface (SCSI) bus, as defined by the ANSI X3T9.2 committee. The device can function as both target and initiator, and can be used in host port, host adapter and formatter modes.

The KS53C80 looks like a peripheral device to the microprocessor. It has internal registers, addressed by the CPU as memory mapped I/O ports. By means of these registers, the KS53C80 controls the interface between the CPU and the SCSI bus, with a minimum of intervention from the processor. Figure 1 shows a functional block diagram of the device.

If the KS53C80 detects errors on the SCSI bus, it generates an interrupt to the CPU. The chip also supports direct memory access (DMA), in normal or block mode, providing an easy interface with DMA controllers.

With the high current open collector output driver, the KS53C80 can sink 48mA at 0.5V. The device can thus be connected directly to the SCSI bus. Additional ground lines increase noise immunity, and reduce ground bouncing.

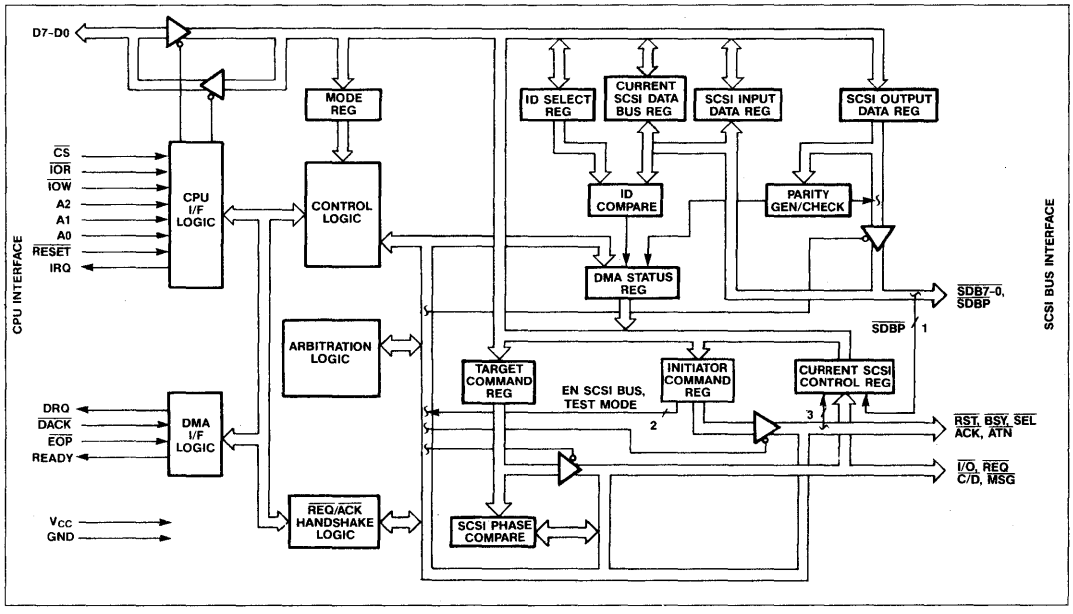


Figure 1. Functional Block Diagram of KS53C80

CMOS VERSUS NMOS FEATURES

The Samsung CMOS KS53C80 has a number of enhancements that differentiate it from NMOS devices. These differences are described below.

- Prevents Additional $\overline{ACK}$ Occurrences

  At the end of process, when a valid $\overline{EOP}$ is received, the NMOS device sets the end of DMA status bit and stops additional DMA requests (DRQs). This means that additional data transmitted without phase change may be lost. The KS53C80 inhibits $\overline{ACK}$ until the device is instructed to continue by a write operation to the Start DMA Initiator Receive register.

- Faster $\overline{REQ}$/$\overline{ACK}$ Transition Times

  The KS53C80 achieves faster response times. This is partly a function of the intrinsically faster CMOS cells, but can also be attributed to design features of this particular device, such as the cell-placement priority for the handshaking signals ($\overline{REQ}$ and $\overline{ACK}$), and the increased number of ground lines that minimize the noise factors.

- No Spurious $\overline{RST}$ Interrupt

  The KS53C80 has an internal 30μA pull up on the $\overline{RST}$ signal. This prevents an unwanted interrupt that can be caused by a floating condition on the input of the $\overline{RST}$ signal when it is not terminated on the SCSI bus.

- Verification of True End of DMA Send Operations

  The Samsung KS53C80 uses bit 7 of the Target Command Register to indicate that the last byte of the DMA transfer has actually been sent to the SCSI bus. The NMOS device does not have this feature, and if $\overline{EOP}$ is applied on the last byte, the END OF DMA status bit indicates only that the last byte has been received, and there is nothing to indicate whether this byte has been placed on the SCSI bus.

- Faster Transfer Rates

  There are two versions of the KS53C80. The slower version (1.5 megabytes per second) is the same as the N5380 NMOS device. The fast version is twice as efficient (3.0 megabytes per second).

INTERFACE SPECIFICATIONS

The KS53C80 SCSI Bus Controller is available in two packages: the first, shown in Figure 2 is a 44-pin PLCC (plastic leaded chip carrier) device. The second, shown in Figure 3 is a 48-pin DIP device.

Table 1 shows detailed pin allocations for the PLCC device, while Table 2 shows the DIP version. Table 3 provides the input/output signal definitions for the SCSI bus interface, and Table 4 for the CPU interface.

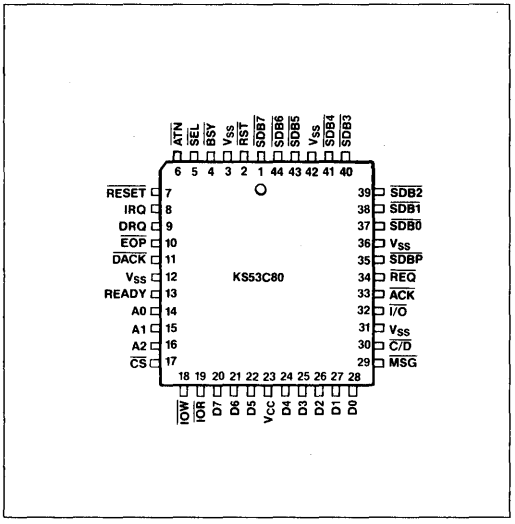


Figure 2. Physical Layout of the KS53C80 SCSI Bus Controller (PLCC Version)

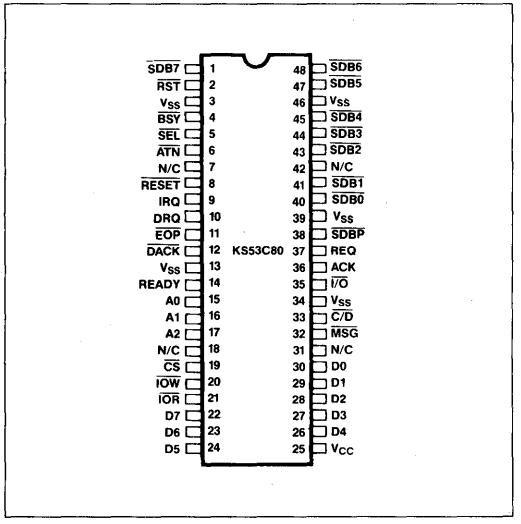


Figure 3. Physical Layout of the KS53C80 SCSI Bus Controller (DIP-48 Version)

Table 1. KS53C80 Pin Allocations PLCC Version.

Pin No.	Signal Abbrev.	Signal Name
1	$\overline{SDB7}$	Data Bit 7 (SCSI)
2	$\overline{RST}$	Reset
3	V_{SS}	V_{SS}
4	$\overline{BSY}$	Busy
5	$\overline{SEL}$	Select
6	$\overline{ATN}$	Attention
7	$\overline{RESET}$	Reset
8	IRQ	Interrupt Request
9	DRQ	DMA Request
10	$\overline{EOP}$	End of Process
11	$\overline{DACK}$	DMA Acknowledge
12	V_{SS}	V_{SS}
13	READY	Ready
14	A0	Address 0
15	A1	Address 1
16	A2	Address 2
17	$\overline{CS}$	Chip Select
18	$\overline{IOW}$	I/O Write
19	$\overline{IOR}$	I/O Read
20	D7	Data 7 (CPU)
21	D6	Data 6 (CPU)
22	D5	Data 5 (CPU)
23	V_{CC}	V_{CC}
24	D4	Data 4 (CPU)
25	D3	Data 3 (CPU)
26	D2	Data 2 (CPU)
27	D1	Data 1 (CPU)
28	D0	Data 0 (CPU)
29	$\overline{MSG}$	Message
30	$\overline{C}$/D	Control/Data
31	V_{SS}	V_{SS}
32	$\overline{I}$/O	Input/Output
33	$\overline{ACK}$	Acknowledge
34	$\overline{REQ}$	Request
35	$\overline{SDBP}$	Data Bit Parity (SCSI)
36	V_{SS}	V_{SS}
37	$\overline{SDB0}$	Data Bit 0 (SCSI)
38	$\overline{SDB1}$	Data Bit 1 (SCSI)
39	$\overline{SDB2}$	Data Bit 2 (SCSI)
40	$\overline{SDB3}$	Data Bit 3 (SCSI)
41	$\overline{SDB4}$	Data Bit 4 (SCSI)
42	V_{SS}	V_{SS}
43	$\overline{SDB5}$	Data Bit 5 (SCSI)
44	$\overline{SDB6}$	Data Bit 6 (SCSI)

Table 2. KS53C80 Pin Allocations DIP Version

Pin No.	Signal Abbrev.	Signal Name
1	$\overline{SDB7}$	Data Bit 7 (SCSI)
2	$\overline{RST}$	Reset
3	V_{SS}	V_{SS}
4	$\overline{BSY}$	Busy
5	$\overline{SEL}$	Select
6	$\overline{ATN}$	Attention
7	N/C	Not Connected
8	$\overline{RESET}$	Reset
9	IRQ	Interrupt Request
10	DRQ	DMA Request
11	$\overline{EOP}$	End of Process
12	$\overline{DACK}$	DMA Acknowledge
13	V_{SS}	V_{SS}
14	READY	Ready
15	A0	Address 0
16	A1	Address 1
17	A2	Address 2
18	N/C	Not Connected
19	$\overline{CS}$	Chip Select
20	$\overline{IOW}$	I/O Write
21	$\overline{IOR}$	I/O Read
22	D7	Data 7 (CPU)
23	D6	Data 6 (CPU)
24	D5	Data 5 (CPU)
25	V_{CC}	V_{CC}
26	D4	Data 4 (CPU)
27	D3	Data 3 (CPU)
28	D2	Data 2 (CPU)
29	D1	Data 1 (CPU)
30	D0	Data 0 (CPU)
31	N/C	Not Connected
32	$\overline{MSG}$	Message
33	$\overline{C}$/D	Control/Data
34	V_{SS}	V_{SS}
35	$\overline{I}$/O	Input/Output
36	$\overline{ACK}$	Acknowledge
37	$\overline{REQ}$	Request
38	$\overline{SDBP}$	Data Bit Parity (SCSI)
39	V_{SS}	V_{SS}
40	$\overline{SDB0}$	Data Bit 0 (SCSI)
41	$\overline{SDB1}$	Data Bit 1 (SCSI)
42	N/C	Not Connected
43	$\overline{SDB2}$	Data Bit 2 (SCSI)
44	$\overline{SDB3}$	Data Bit 3 (SCSI)
45	$\overline{SDB4}$	Data Bit 4 (SCSI)
46	V_{SS}	V_{SS}
47	$\overline{SDB5}$	Data Bit 5 (SCSI)
48	$\overline{SDB6}$	Data Bit 6 (SCSI)

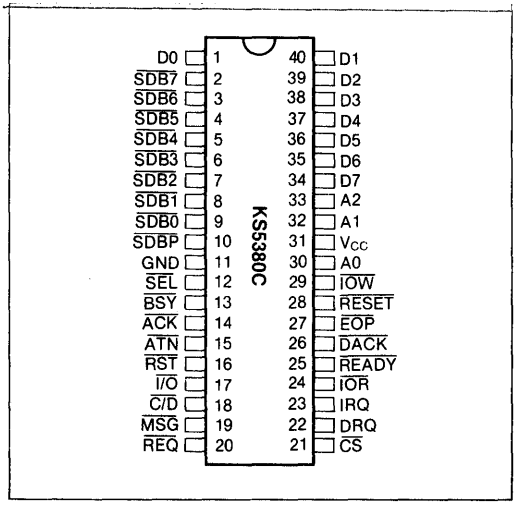


Figure 4. Physical Layout of the KS5380C SCSI Bus Controller (DIP-40 Version)

Table 3. KS5380C Pin Allocation DIP Version.

Pin No.	Signal Abbrev.	Signal Name
1	D0	Data 0 (CPU)
2	$\overline{SDB7}$	Data Bit 7 (SCSI)
3	$\overline{SDB6}$	Data Bit 6 (SCSI)
4	$\overline{SDB5}$	Data Bit 5 (SCSI)
5	$\overline{SDB4}$	Data Bit 4 (SCSI)
6	$\overline{SDB3}$	Data Bit 3 (SCSI)
7	$\overline{SDB2}$	Data Bit 2 (SCSI)
8	$\overline{SDB1}$	Data Bit 1 (SCSI)
9	$\overline{SDB0}$	Data Bit 0 (SCSI)
10	$\overline{SDBP}$	Data Bit Parity (SCSI)
11	V_{SS}	V_{SS}
12	$\overline{SEL}$	Select
13	$\overline{BSY}$	Busy
14	$\overline{ACK}$	Acknowledge
15	$\overline{ATN}$	Attention
16	$\overline{RST}$	Reset
17	$\overline{I/O}$	Input/Output
18	$\overline{C/D}$	Control/Data
19	$\overline{MSG}$	Message
20	$\overline{REQ}$	Request

Pin No.	Signal Abbrev.	Signal Name
21	$\overline{CS}$	Chip Select
22	DRQ	DMA Request
23	IRQ	Interrupt Request
24	$\overline{IOR}$	I/O Read
25	READY	Ready
26	$\overline{DACK}$	DMA Acknowledge
27	$\overline{EOP}$	End of Process
28	$\overline{RESET}$	Reset
29	$\overline{IOW}$	I/O Write
30	A0	Address 0
31	V_{CC}	V_{CC}
32	A1	Address 1
33	A2	Address 2
34	D7	Data 7 (CPU)
35	D6	Data 6 (CPU)
36	D5	Data 5 (CPU)
37	D4	Data 4 (CPU)
38	D3	Data 3 (CPU)
39	D2	Data 2 (CPU)
40	D1	Data 1 (CPU)

Table 3. Interface Signal Definitions—SCSI Bus

Note: I indicates that the signal is an input to the KS53C80 chip. O indicates that the signal is an output from the KS53C80 chip.

Symbol	Type	Description
$\overline{SDB0\text{-}7}$	I/O	**Data Bits 0-7:** Eight-bit bidirectional data bus. $\overline{SDB7}$ is the most significant bit, and has highest priority during arbitration.
$\overline{SDBP}$	I/O	**Data Bit Parity:** This bit is used for parity checking. The bit is always generated when sending information, but parity checking when receiving is optional. Data parity is odd (the number of ones, including parity, is odd). Parity is not valid during arbitration.
$\overline{SEL}$	I/O	**Select:** This bit is used by the initiator to select a target or by the target to reselect an initiator.
$\overline{BSY}$	I/O	**Busy:** Indicates that the SCSI bus is being used, and may be driven by both the target and the initiator.
$\overline{ACK}$	I/O	**Acknowledge:** $\overline{ACK}$ is asserted by the initiator during information transfer, in response to the assertion of $\overline{REQ}$ by the target. $\overline{ACK}$ is deasserted after $\overline{REQ}$ becomes inactive.
$\overline{ATN}$	I/O	**Attention:** This signal is driven by the initiator after successful selection of the target.
$\overline{RST}$	I/O	**Reset:** This input indicates a reset condition on the SCSI bus.
$\overline{I/O}$	I/O	**Input/Output:** This signal indicates the direction of data flow on the SCSI bus, and is controlled by the target. When asserted, the data is transferred to the initiator. When deasserted, data is transferred to the target. The signal also distinguishes between the selection and reselection phases.
$\overline{C/D}$	I/O	**Control/Data:** This signal is controlled by the target, and indicates that data ($C/\overline{D}$ deasserted) or control phase.
$\overline{REQ}$	I/O	**Request:** Controlled by the target, $\overline{REQ}$ is asserted by the target to begin the handshake associated with data transfer. $\overline{REQ}$ is deasserted on receipt of $\overline{ACK}$ from the initiator. Data is latched on the falling edge of $\overline{REQ}$ for the initiator data receive operation.

Table 4. Interface Signal Definitions—CPU Bus

Symbol	Type	Description
D0-7	I/O	**Data 0-7:** This is an eight-bit bidirectional, tri-state data bus between the KS53C80 and the CPU (microprocessor). D7 is the most significant bit.
$\overline{CS}$	I	**Chip Select:** This input from the CPU enables reading or writing of the internal register selected by address inputs A0-2.
DRQ	O	**DMA Request:** This signal is sent from the KS53C80 to the DMA controller, or the CPU, and requests a direct memory access (DMA) operation. It occurs only when the DMA Mode bit is set in the MODE Register. DRQ is cleared when $\overline{DACK}$ is asserted.
IRQ	O	**Interrupt Request:** Flags the CPU that one of the interrupt conditions has been met. This includes SCSI bus fault conditions, and events requiring CPU intervention.
READY	O	**Ready:** This signal is transferred from the KS53C80 to the CPU. It controls the speed of block mode DMA transfer and must be enabled by the CPU. It indicates that the chip is ready to send or receive data, and remains low (inactive) until the last byte has been sent, or until the DMA mode bit has been reset.
$\overline{DACK}$	I	**DMA Acknowledge:** This input resets DRQ and, in conjunction with $\overline{IOR}$ or $\overline{IOW}$, selects the data register to be accessed for the read or write operation. $\overline{CS}$ must be high.
$\overline{EOP}$	I	**End of Process:** This input is sent to the KS53C80 by the CPU or DMA controller, to terminate the DMA transfer. If it is asserted during a DMA cycle, the byte being processed is sent, but no further bytes are requested. The KS53C80 can automatically generate an interrupt in response to receiving $\overline{EOP}$.
A0-2	I	**Address 0-2:** These inputs from the CPU select one of eight internal registers in the KS53C80, in conjunction with $\overline{IOR}$, $\overline{IOW}$ and $\overline{CS}$.
$\overline{IOR}$	I	**Input/Output Read:** This signal is sent from the CPU, and initiates a read operation in the register selected by A0-2 and $\overline{CS}$.
$\overline{IOW}$	I	**Input/Output Write:** This signal is sent from the CPU, and initiates a write operation in the register selected by A0-2 and $\overline{CS}$.
$\overline{RESET}$	I	**Reset:** This input clears all registers. It does not force the SCSI signal $\overline{RST}$ to become active, and thus affects only the local KS53C80.

REGISTERS

The KS53C80 is made up of eight physical registers, that are configured and addressed as 16 registers. The controlling CPU can read from or write to these registers to monitor and initiate SCSI bus activities.

There are four groups of registers:

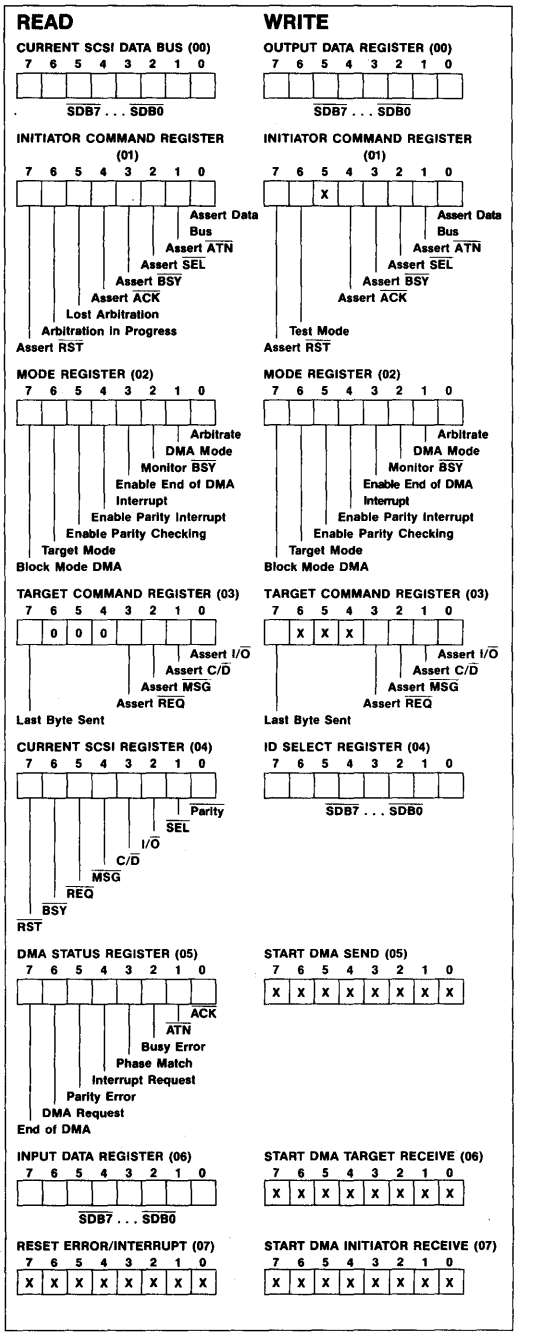
- Three **data registers**: Input Data Register, Output Data Register, and the Current SCSI Data Register.
- Three **control registers**: Mode Register, and Initiator Command Register, Target Command Register.
- Three **miscellaneous registers**: Current SCSI Bus Status Register, ID Select Register, Reset Error/ Interrupts Register.
- Four **DMA registers**: Start DMA Send Register, Start DMA Target Receive Register, Start DMA Initiator Receive Register, DMA Status Register.

Registers are selected by the address inputs, A0-2, when $\overline{CS}$ is asserted. A read operation is initiated by $\overline{IOR}$ and a write operation by $\overline{IOW}$, so that $\overline{IOR}$ and $\overline{IOW}$ act as virtual functional address bits. Table 5 shows the register addresses, and indicates the functions performed by each register. Table 6 is a register reference chart.

Table 5. Register Addresses

A2	A1	A0	Reg.	Register Name	Operation
1	1	1	7	Start DMA Initiator Receive	Write
1	1	1	7	Reset Error/Interrupt	Read
1	1	0	6	Start DMA Target Receive	Write
1	1	0	6	Input Data	Read
1	0	1	5	Start DMA Send	Write
1	0	1	5	DMA Status	Read
1	0	0	4	ID Select	Write
1	0	0	4	Current SCSI Control	Read
0	1	1	3	Target Command	Read/Write
0	1	0	2	Mode	Read/Write
0	0	1	1	Initiator Command	Read/Write
0	0	0	0	Current SCSI Data	Read
0	0	0	0	Output Data	Write

Table 6. Register Reference Chart



Note: X = Don't Care

Data Registers

Data registers are used to transfer data to and from the SCSI bus and the microprocessor bus.

Input Data Register—6 (Read Only)

FUNCTION:

Holds data received from the SCSI bus during a DMA operation. As an option, parity may be checked when the register is loaded.

When this register is functioning as a read-only input data register, data are latched into the register under the following conditions:

- $\overline{ACK}$ goes low — DMA target receive operation.
- $\overline{REQ}$ goes low — DMA initiator operation.
- DMA MODE bit is set.

The register can be read by asserting $\overline{IOR}$ and $\overline{DACK}$ at the same time or by a CPU read operation of address location 6. Note that $\overline{DACK}$ and $\overline{CS}$ must never be active simultaneously.

REGISTER CONFIGURATION

7	6	5	4	3	2	1	0
X	X	X	X	X	X	X	X
$\overline{SDB7}$	$\overline{SDB6}$	$\overline{SDB5}$	$\overline{SDB4}$	$\overline{SDB3}$	$\overline{SDB2}$	$\overline{SDB1}$	$\overline{SDB0}$

Output Data Register—0 (Write Only)

FUNCTION:

Used for sending information to the SCSI bus. It is used to assert the ID bits during the arbitration and selection phases. Data is sent to the register using a normal write operation, or by asserting $\overline{IOW}$ and $\overline{DACK}$ at the same time, under DMA control, irrespective of Address and $\overline{CS}$. In I/O operation, this register is written when $\overline{IOW}$ is asserted, A0-2 = 000, and $\overline{CS}$ = 0.

REGISTER CONFIGURATION

7	6	5	4	3	2	1	0
X	X	X	X	X	X	X	X
$\overline{SDB7}$	$\overline{SDB6}$	$\overline{SDB5}$	$\overline{SDB4}$	$\overline{SDB3}$	$\overline{SDB2}$	$\overline{SDB1}$	$\overline{SDB0}$

Current SCSI Data Register—0 (Read Only)

FUNCTION:

Enables the microprocessor to read the active SCSI data bus of any time. Used during programmed I/O data read, or arbitration. The SCSI bus data are not latched.

A read operation of this register is initiated when $\overline{CS}$ is low, and address 0 (A0-2 = 000) is sent from the CPU. $\overline{IOR}$ must be low to enable the read. This register is also read during arbitration to determine whether devices with higher priority are also arbitrating.

If parity checking is enabled, the SCSI bus parity is checked at the beginning of the read cycle. Parity error checking is not guaranteed during arbitration.

REGISTER CONFIGURATION

7	6	5	4	3	2	1	0
X	X	X	X	X	X	X	X
$\overline{SDB7}$	$\overline{SDB6}$	$\overline{SDB5}$	$\overline{SDB4}$	$\overline{SDB3}$	$\overline{SDB2}$	$\overline{SDB1}$	$\overline{SDB0}$

Control Registers

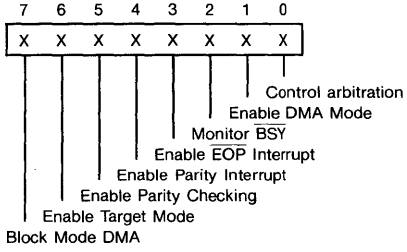
These registers store the control signals that govern the operation of the CPU and SCSI buses.

Mode Register—2 (Read/Write)

FUNCTION:

Controls the operating modes of the chip, deciding whether the chip is to function as initiator or target; whether DMA transfers are to be used; and whether interrupts are to be generated for a number of error conditions. The register is set during a write operation ($\overline{IOW}$ = 0), and may be sampled during a read operation ($\overline{IOR}$ = 0), to check the value of the internal control bits.

REGISTER CONFIGURATION



BIT 7—BLOCK MODE DMA

This bit must be used in conjunction with Bit 1 (DMA Mode)

Normal DMA Mode

BLOCK MODE DMA = 0 and DMA MODE bit = 1: The DMA handshake is the normal interlocked handshake. The rising edge of $\overline{DACK}$ indicates the end of each byte transfer.

Block DMA Mode

BLOCK MODE DMA = 1 and DMA MODE bit = 1: $\overline{DACK}$ is allowed to remain active during DMA operation, and READY can be used to request the next data transfer. The trailing edge of $\overline{IOW}$ or $\overline{IOR}$ indicates the end of each byte transfer.

This mode is compatible with the KS82C37 DMA Controller.

BIT 6—TARGET MODE

TARGET MODE = 1: $\overline{C/D}$, $\overline{I/O}$, $\overline{MSG}$ and $\overline{REQ}$ are asserted on the SCSI bus, and the chip acts as the SCSI device target.

TARGET MODE = 0: $\overline{ATN}$, $\overline{ACK}$ are asserted on the SCSI bus, and the device acts as the SCSI device initiator.

BIT 5 - PARITY CHECK

PARITY CHECK = 1: Parity error is saved in the parity error latch whenever data is received under DMA control, or read out from the Current SCSI Data Register (0).

The state of the parity bit can be determined by reading the DMA status register (5), and can be reset by reading the Reset Error/Interrupt Register (7).

PARITY CHECK = 0: Parity error is not saved in the parity error latch.

BIT 4—ENABLE PARITY INTERRUPT

ENABLE INTERRUPT PARITY = 1: If a parity error is detected when this bit is set, and if PARITY CHECK is set, an interrupt (IRQ) is generated.

ENABLE INTERRUPT PARITY = 0: Disabled.

BIT 3—$\overline{EOP}$ INTERRUPT

INTERRUPT $\overline{EOP}$ = 1: If this bit is set, an interrupt is generated when the DMA controller asserts $\overline{EOP}$. $\overline{EOP}$ is valid in conjunction with either $\overline{IOR}$, $\overline{IOW}$ and $\overline{DTACK}$.

INTERRUPT $\overline{EOP}$ = 0: Disabled.

BIT 2—BUSY MONITOR

BUSY MONITOR = 1: If $\overline{BSY}$ unexpectedly goes inactive for longer than 400 ns, but less than 1200ns, an interrupt is generated. This causes the lower six bits of the Initiator Command Register to be reset (0), and all signals are disabled on the SCSI bus until the Busy Error bit is reset. This feature allows the CPU to respond if the SCSI bus becomes available.

BUSY MONITOR = 0: Busy Monitor is disabled, and no interrupt is generated.

BIT 1—DMA MODE

DMA MODE = 1: If this bit is set, the KS53C80 is in DMA Mode, and the internal state machine controls $\overline{ACK}$, $\overline{REQ}$ and the CPU signals DRQ and READY automatically. ASSERT DATA BUS (register 1, bit 0) must be active for all DMA transfers. TARGET MODE (Register 2, bit 6), must be active (1) for a write operation to port 6, and inactive (0) for a write operation to port 7 (initiator role). $\overline{BSY}$ must be active when this bit is set.

DMA Mode is not reset when $\overline{EOP}$ is received, but must be reset by the CPU. However, $\overline{EOP}$ automatically inhibits additional DMA cycles.

DMA MODE = 0: Stops all DMA transfers.

BIT 0—ARBITRATION

ARBITRATION = 1: Starts the arbitration process. Before this bit is set, the Output Data Register (0) should contain the correct SCSI device ID. The KS53C80 waits for the SCSI bus to be free before starting arbitration. The status of the arbitration phase can be checked by reading bit 5 and 6 in Register 1: Arbitration in Progress (bit 6), Lost Arbitration (bit 5).

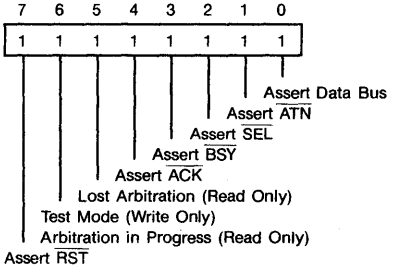
ARBITRATION = 0: Disabled

Initiator Command Register—1 (Read or Write)

FUNCTION:

Asserts and monitors certain initiator SCSI bus signals, and monitors bus arbitration.

REGISTER CONFIGURATION



BIT 7 - ASSERT RESET

ASSERT RESET = 1: $\overline{RST}$ is asserted on the SCSI bus, initializing all devices on the bus to the reset condition. IRQ goes active (high) indicating a SCSI reset. This interrupt cannot be disabled by masking it out. All control registers and logic are reset to '0' except the $\overline{RST}$ bit itself, and the Test Mode bit (Register 1, bit 6).

ASSERT RESET = 0: a). $\overline{RST}$ is disabled. b). External RESET may have been used.

BIT 6—ARBITRATION IN PROGRESS (Read Only)

ARBITRATION IN PROGRESS = 1: The arbitration bit is set, provided that the ARBITRATE bit (Register 2, bit 6) is also set. It indicates that the KS53C80 has detected a bus free phase, and is currently arbitrating for the bus. Resetting the ARBITRATE bit also resets ARBITRATION IN PROGRESS.

BIT 6—TEST MODE (Write Only)

TEST MODE = 1: When this bit is set, all output drivers, including SCSI and CPU signals are tristated. All writable registers can be accessed during Test Mode.

This function is used only during testing. When the bit is reset, the KS53C80 returns to normal operation. It can be reset by CPU signal RESET. It is not affected by RST on the SCSI bus, or by ASSERT RST bit in the Initiator Command Register.

BIT 5—LOST ARBITRATION (Read Only)

LOST ARBITRATION = 1: When this bit is asserted, it indicates that the KS53C80 has arbitrated for the bus, and detected that another device on the bus, with higher priority, has asserted the SEL line. The ARBITRATE bit (Register 2, bit 2) must be active at this time.

BIT 4—ASSERT ACK

ASSERT ACK = 1: When this bit is set, ACK is asserted on the SCSI bus. The TARGET MODE bit (Register 2, bit 6) must be reset at this time, indicating that the KS53C80 is the initiator.

BIT 3—ASSERT BSY

ASSERT BSY = 1: BSY is asserted on the SCSI bus. This only signifies that the process of selection or reselection has been completed.

BIT 2—ASSERT SEL

ASSERT SEL = 1: SEL is asserted on the SCSI bus. SEL is normally asserted after a successful arbitration.

ASSERT SEL = 0: Resetting this bit deasserts the SEL line.

BIT 1—ASSERT ATN

ASSERT ATN = 1: If the KS53C80 is the initiator (TARGET Mode bit, Register 2, bit 6 reset), ASSERT ATN asserts the ATN line to request a message out phase.

BIT 0—ASSERT DATA BUS

ASSERT DATA BUS = 1: If this bit is set, the open drain drives of SDB0-7 and the parity bit (Output Data Register) are enabled. Data and parity are asserted on the SCSI bus. For this to occur, the following conditions must exist:

- The phase signals (I/O, MSG, C/D) agree with ASSERT I/O, ASSERT C/D, and ASSERT MSG in the Target Command Register, meaning that there is no phase mismatch.
- The I/O is inactive, which means the output is to the target.
- TARGET MODE is inactive.

When the KS53C80 operates as target, the TARGET Mode bit must be set, and the outputs are asserted unconditionally. During arbitration, ASSERT DATA BUS bit has no influence.

Target Command Register—3 (Read/Write)

FUNCTION:

This register controls and monitors the SCSI information transfer phases.

The functions and the conditions governing the functions of this register differ, depending upon whether the KS53C80 is acting as initiator or target.

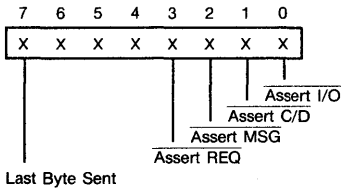
Initiator (Read):

The Target Command Register allows the target to monitor and set/reset the SCSI lines REQ, MSG, C/D and I/O. In addition, reading a '1' in bit 7 signals that the last byte has been send to the SCSI bus during a DMA write operation.

Target (Write):

When the device is in Target Mode, the register enables the CPU to control the SCSI bus information transfer phase asserted by the target.

REGISTER CONFIGURATION



BIT 7—LAST BYTE SENT

LAST BYTE SENT = 1: This bit is set to indicate that the last byte in a DMA transfer has been sent to the SCSI bus.

BITS 6-4—NOT USED

BIT 3—$\overline{\text{ASSERT REQ}}$

$\overline{\text{ASSERT REQ}}$ = 1: $\overline{\text{REQ}}$ is asserted. Note that the $\overline{\text{REQ}}$ line is asserted only if the KS53C80 is in Target Mode (Register 2 bit 6 is set.)

$\overline{\text{ASSERT REQ}}$ = 0: $\overline{\text{REQ}}$ is deasserted.

BITS 2-0—$\overline{\text{ASSERT REQ}}$, $\overline{\text{ASSERT MSG}}$, $\overline{\text{ASSERT C/D}}$

These bits are encoded to control a variety of SCSI bus functions.

$\overline{\text{MSG}}$	$\overline{\text{C/D}}$	$\overline{\text{I/O}}$	Phase	Direction I(nitiator) ⇄ T(arget)
0	0	0	Data Out	I → T
1	0	0	Unspecified	
0	1	0	Command Transfer	I → T
1	1	0	Message Out	I → T
0	0	1	Data In	I ← T
1	0	1	Unspecified	
0	1	1	Status	I ← T
1	1	1	Message In	I ← T

$\overline{\text{I/O}}$ controls the bidirectional SCSI bus, and decides whether it is to function as an input or output bus to the KS53C80. When $\overline{\text{I/O}}$ is high, the SCSI bus functions as an input bus to the chip. When $\overline{\text{I/O}}$ is low (active) it is an output bus from the chip. The $\overline{\text{I/O}}$ line is asserted only if the Target Mode bit is set.

$\overline{\text{C/D}}$ determines whether control information or data is transferred on the bus. When $\overline{\text{C/D}}$ is high, control information is transferred on the bus. When $\overline{\text{C/D}}$ is low (active) data is transferred on the bus.

$\overline{\text{MSG}}$ selects between Message and Status or Command transfers on the bus. When it is high, status or commands are transferred. When $\overline{\text{MSG}}$ is low (active) messages are transferred.

When the KS53C80 is connected as Initiator and the DMA mode bit is true, a phase mismatch interrupt is generated when $\overline{\text{REQ}}$ goes active and the phase lines $\overline{\text{I/O}}$, $\overline{\text{C/D}}$ and $\overline{\text{MSG}}$ are in different state than the appropriate bit in the Target command register.

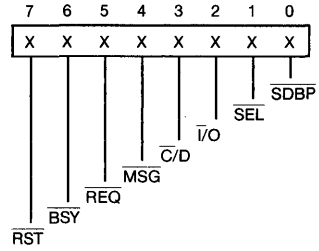
Miscellaneous Registers

Current SCSI Bus Control Register—4 (Read Only)

FUNCTION:

This register is used to monitor seven SCSI bus control signals, and the data parity bit. The SCSI control lines are not latched. The CPU may sample the register to determine the current bus phase, or poll $\overline{\text{REQ}}$ to see if a data transfer is pending. Note that the SCSI signals are true (low) if the appropriate bit is set in the register.

REGISTER CONFIGURATION



BIT 7—$\overline{\text{RST}}$

$\overline{\text{RST}}$ = 1: SCSI bus is in a reset condition.
$\overline{\text{RST}}$ = 0: SCSI bus in not reset.

BIT 6—$\overline{\text{BSY}}$

$\overline{\text{BSY}}$ = 1: SCSI bus is being used.
$\overline{\text{BSY}}$ = 0: SCSI bus is free.

BIT 5—$\overline{\text{REQ}}$

$\overline{\text{REQ}}$ = 1: Indicates a request for a $\overline{\text{REQ}}/\overline{\text{ACK}}$ data transfer has been received by the KS53C80.
$\overline{\text{REQ}}$ = 0: $\overline{\text{REQ}}$ is inactive.

BIT 4—$\overline{\text{MSG}}$

$\overline{\text{MSG}}$ = 1: The bus transfer is in the message phase.
$\overline{\text{MSG}}$ = 0: The bus is not in message phase.

BIT 3—$\overline{\text{C/D}}$

$\overline{\text{C/D}}$ = 1: Data is on the bus.
$\overline{\text{C/D}}$ = 0: Control signals are on the bus.

BIT 2—$\overline{\text{I/O}}$

$\overline{\text{I/O}}$ = 1: Data is being transferred to the initiator.
$\overline{\text{I/O}}$ = 0: The bus is active as an input bus.

BIT 1—$\overline{SEL}$

$\overline{SEL}$ = 1: The initiator has selected a target, or a target has reselected an initiator.
$\overline{SEL}$ = 0: The device is not selected.

BIT 0—$\overline{SDBP}$

$\overline{SDBP}$ = 1/0: Indicates state of parity bit.

Note that parity is odd, so $\overline{SDBP}$ is set high or low, (depending upon the state of the eight data bits), to force an odd number of ones, including the parity bit.

ID Select Register—4 (Write Only)

FUNCTION:

Monitors a single device ID if selection or reselection is being attempted. An ID number is given to each SCSI device in a system, by assigning one bit of the ID register. If an ID match is found while a bus-free condition exists, $\overline{BSY}$ false and $\overline{SEL}$ is active, the KS53C80 will generate an interrupt to indicate a selection or reselection.

Parity is checked in the selected device if ENABLE PARITY CHECKING is appropriately set (active).

REGISTER CONFIGURATION

7	6	5	4	3	2	1	0
X	X	X	X	X	X	X	X
SDB7	SDB6	SDB5	SDB4	SDB3	SDB2	SDB1	SDB0

Reset Error/Interrupt Register—7 (Read Only)

FUNCTION:

This is a dummy register. When the register is read, the following actions take place:

- Reset Interrupt Request (IRQ) signal.
- Interrupt Latch request bit reset in Register 5.
- Busy Error is reset in Register 5.
- Parity Error is reset in Register 5.

REGISTER CONFIGURATION

7	6	5	4	3	2	1	0
X	X	X	X	X	X	X	X

DMA Registers

Three write-only registers initiate all DMA activity. The following Mode bits must be set appropriately, before a write operation is performed in any of these registers. Data (D0-7) are not valid and are meaningless when a write operation is being performed in one of the DMA registers.

Target Mode	DMA Mode	Block* Mode DMA	Register Selected
X	1	1/0	Start DMA Send
1	1	1/0	Start DMA Target Receive
0	1	1/0	Start DMA Initiator Receive

* This bit is set (1) to enable Block Mode DMA transfer. If it is 0, a normal DMA transfer is initiated.

Start DMA Send Register—5 (Write Only)

FUNCTION:

Initiates a DMA send from the DMA to the SCSI bus, during either a Target or an Initiator operation. The DMA MODE bit (Register 2, bit 1) must be set prior to starting a DMA operation.

REGISTER CONFIGURATION

7	6	5	4	3	2	1	0
X	X	X	X	X	X	X	X

Start DMA Target Receive Register—6 (Write Only)

FUNCTION:

Initiates a DMA receive from the SCSI bus to the DMA, during Target mode only. Both the DMA Mode bit (Register 2, bit 1) and the TARGET Mode bit (Register 2, bit 6) must be set.

REGISTER CONFIGURATION

7	6	5	4	3	2	1	0
X	X	X	X	X	X	X	X

Start DMA Initiator Receive Register—7 (Write Only)

FUNCTION:

Initiates a DMA receive from the SCSI bus to the DMA, during Initiator mode only. The DMA Mode Bit (Register 2, bit 1) must be set, and the TARGET Mode Bit (Register 2, bit 6) must be reset prior to this operation.

REGISTER CONFIGURATION

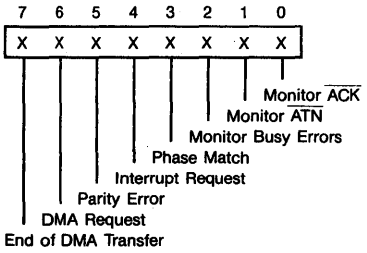
7	6	5	4	3	2	1	0
X	X	X	X	X	X	X	X

DMA Status Register—5 (Read Only)

FUNCTION:

Monitors the control signals not found in the Current SCSI Bus Status Register (ATN, ACK), and six status bits.

REGISTER CONFIGURATION



BIT 7—END OF DMA TRANSFER

END OF DMA TRANSFER = 1: This bit is set only if a valid EOP has been received: DACK, EOP and either the read initiate (IOR) or write initiate (IOW) signals are active at the same time. REQ and ACK should be monitored to make sure that the last byte has actually been transferred, since EOP may go active while the last byte is being sent to the Output Data Register.

This bit is reset by whenever the DMA MODE bit is reset in the Mode Register. This may occur when the busy condition is lost. Therefore, the DMA STATUS Register should be read before resetting the ASSERT BSY bit (Register 1, bit 3), at the conclusion of the DMA transfer.

BIT 6—DMA REQUEST

DMA REQUEST = 1: Permits the CPU to read the output pin DRQ.

The bit is cleared by resetting the DMA MODE bit in the Mode Register, or by asserting DACK and IOW for DMA send (write) operations, and DACK and IOR for DMA read operations. It is not reset if a Phase Mismatch Interrupt Occurs

BIT 5—PARITY ERROR

PARITY ERROR = 1: Indicates that a parity error has occurred during device selection, or during receipt of data.

It can be set only when the ENABLE PARITY CHECK bit is active. It is cleared by reading the RESET PARITY/ INTERRUPT Register (7).

BIT 4—INTERRUPT REQUEST ACTIVE

INTERRUPT REQUEST ACTIVE = 1/0: Indicates the current state of the IRQ output.

The bit is cleared by reading the Reset Parity/Interrupt Register.

BIT 3—PHASE MATCH

PHASE MATCH = 1: When active, it indicates whether the lower three bits of the Target Command Register match the Current SCSI bus signals, MSG, C/D, I/O. This bit must be set before data is transferred on the SCSI bus. The bit is updated constantly, to reflect the current status. It is used by the initiator. (SCSI signals MSG, C/D and I/O indicate the current transfer phases.)

BIT 2—BUSY ERROR

BUSY ERROR = 1: Indicates the loss of the BSY signal. It is set if MONITOR BUSY is active (1) and BSY goes inactive for at least the bus-settle period of 400ns. When this bit is set, SCSI outputs are disabled, and DMA MODE is reset.

BIT 1—MONITOR ATN

MONITOR ATN = 1/0: Indicates the condition of the SCSI bus control signal ATN. This bit is monitored by the CPU.

BIT 0—MONITOR ACK

MONITOR ACK = 1/0: Indicates the state of the SCSI bus control signal ACK. This bit is monitored by the target device.

DATA TRANSFER MODES

The KS53C80 controls data transfer between SCSI bus devices. It supports four operating modes:

- Programmed Input/Output (I/O) transfer
- Normal Direct Memory Access (DMA) transfer
- Block DMA transfer
- Pseudo DMA transfer.

Programmed I/O Transfer

This transfer mode is used to transfer small data blocks, such as control, message or status.

To start an initiator send operation, bits C/D, I/O and MSG in the Target Command Register are set to enable control or data to be placed on the bus; to enable the SCSI bus as an input or an output device; and to determine whether the transfer is a message or non-message transfer.

For an operation to start, there must be a phase match; ASSERT DATA BUS must be active, and the I/O signal must be inactive. The handshake signals REQ and ACK are monitored and asserted individually, by reading the CPU and writing the appropriate register bits.

The data to be transferred is loaded into the Output Data Register (0). The processor waits until REQ is asserted (Register 4, bit 5), and then looks for a Phase Match. If there is an appropriate match, ASSERT ACK is asserted, to complete the handshake. The CPU samples REQ until it becomes inactive, indicating that the request for transfer has been met. At that point, ASSERT ACK is reset.

Normal DMA Transfer

DMA transfers are generally used to transfer large blocks of data. The DMA Mode bit must be set, and the BLOCK Mode bit must be reset.

To initiate a DMA transfer the KS53C80 generates a DMA request (DRQ) to transfer a byte to or from the DMA Controller. This DRQ is output to the DMA Controller. The DMA Controller acknowledges receipt, with the DACK handshaking signal, and asserts either IOR or IOW, to enable a read or a write operation, respectively. DRQ is terminated when DACK goes active, and DACK is terminated at the end of the minimum pulse width for IOR or IOW. This procedure is followed for each byte transferred. Note that DACK must not be active while CS is active.

DMA Block Transfer

To increase transfer rate, an external DMA device, such as the KS82C37 can go into block mode transfer, and perform sequential DMA transfers, without giving up the bus to the CPU. Block mode transfers are supported for both Target and Initiator roles. In this mode, the BLOCK Mode bit must be set.

At the start of the transfer, DRQ is asserted, as for normal transfer. DACK is then asserted, to acknowledge request, and remains active during the entire transfer. While DACK is active, the CPU cannot gain access to the system bus. IOR or IOW is asserted, to initiate the read or write operation. When the read or write initiate is terminated, READY goes active, indicating that the KS53C80 is ready for another data transfer. READY is used to insert wait states in a read or write cycle as long as READY is low.

To get the best performance in block mode, the DMA logic may optionally use the normal DMA mode DRQ-DACK handshaking.

Block Mode transfers end when IOR or IOW goes inactive. This means that another transfer can be initiated, without waiting for DACK, thus increasing the data throughput rate.

READY will be false (low) whenever the Input Data Register (R6) or the byte in the Output Data Register (R0) is not sent to the SCSI data bus.

Care must be taken when using READY as a DMA request signal. If a phase mismatch error occurs during transfer, READY will remain inactive and INT will be asserted. In this instance, the control has to given back from the DMA Controller to the CPU so that the interrupt can be received.

Emulated DMA Mode Transfer During I/O Transfers

To improve performance during I/O transfers, and avoid continually monitoring and asserting REQ and ACK, the system may be set up to emulate DMA mode during I/O transfers.

The KS53C80 operates in DMA mode, and uses the CPU to generate the DMA handshake signals. DRQ is then monitored by polling the DMA REQ bit (6) in the DMA Status Register (5); by sampling the signal through an external IO port; or by using it to generate a CPU interrupt.

When DRQ is detected, the CPU can proceed with a DMA read or write transfer. External decoding is used to generate the appropriate IOR, IOW and DACK signals. Since external logic is often needed to generate CS, the designer can take advantage of the same logic to generate DACK at no extra cost.

Halting DMA Operation

The DMA operation may be halted in a number of ways, as described below.

Using the EOP Signal

To halt DMA operation, EOP is asserted for the required minimum time while IOR or IOW and DACK are simultaneously active. If EOP goes active and neither IOR or IOW is active, an interrupt is generated, but the DMA transfer continues.

The $\overline{EOP}$ signal does not reset the DMA MODE bit, so provisions must be made to do this. In addition, since $\overline{EOP}$ may go active during the last byte sent to the Output Data Register, the $\overline{REQ}$ and $\overline{ACK}$ signals should be monitored to make sure that the last byte has actually been sent. In addition, LAST BYTE SEND (Register 3, bit 7) can be monitored. Note that this bit is not implemented in all 5380-type SCSI controllers.

Bus Phase Mismatch Interrupt

Bus phase mismatch halts a DMA transfer. This method can be used if the KS53C80 is operating as an initiator. It prevents recognition of $\overline{REQ}$, and disables all the SCSI data and parity drivers. If $\overline{REQ}$ becomes active, an interrupt will be generated. The DMA transfer is stopped, however the DMA MODE bit must be reset by the CPU or by a valid $\overline{EOP}$ signal.

Resetting the DMA MODE Bit

A DMA mode transfer may be terminated at any time by resetting the DMA MODE bit. This bit should also be reset if the operation was halted by $\overline{EOP}$ or by a phase mismatch interrupt.

If the DMA MODE bit is used instead of $\overline{EOP}$ during a Target role operation, the time when the bit is reset is critical, and in most instances, it is easier to use $\overline{EOP}$ when the device is in Target Mode. If the KS53C80 is receiving data as the target device, DMA MODE should be reset when the last DRQ is received, and before $\overline{DACK}$ is asserted. Otherwise, an additional $\overline{REQ}$ will occur. When DMA MODE is reset, DRQ is terminated. However, the last byte received will remain in the Input Data Register, and may be obtained either by performing a normal CPU read operation, or by cycling $\overline{DACK}$ and $\overline{IOR}$.

The DMA MODE bit must be set before writing to any of the Start DMA registers for subsequent bus phases.

INTERRUPTS

The KS53C80 generates an interrupt signal (IRQ) which it sends to the processor when a task has been completed or if an abnormal operating condition is detected. The following occurrences will cause IRQ to be asserted:

- The KS53C80 is selected or reselected
- The operation is completed and $\overline{EOP}$ is asserted during a DMA transfer
- The SCSI bus is disconnected and the $\overline{BSY}$ signal is lost
- A parity error is detected
- The SCSI bus is reset
- There is a SCSI bus phase mismatch.

When the CPU receives an interrupt (IRQ), it reads the DMA Status Register and the Current SCSI Bus Status Register, to determine what was the cause of the interrupt.

IRQ is reset by writing to the Reset Error/Interrupt Register (7), or by driving $\overline{RESET}$ active to implement an external reset.

Selection/Reselection Interrupt

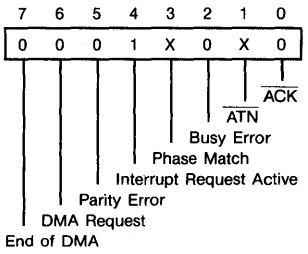
A select interrupt occurs when the select signal ($\overline{SEL}$) is active; the device ID is valid, and the SCSI bus is not busy ($\overline{BSY}$ inactive for a bus-settle delay of at least 400 nanoseconds). If I/$\overline{O}$ is active, this is considered to be a reselect interrupt.

ID status is decided by a match in the ID Select Register (4). A single-bit match is adequate to enable the interrupt. SCSI bus protocol requires that not more than two devices be active during the selection process. The Current SCSI Data Register (0) is read to make sure that this condition is met.

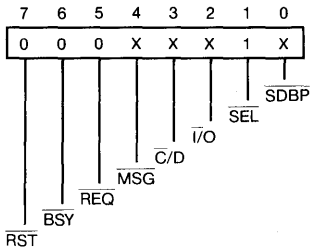
If parity checking is supported, parity is also expected to be good during the selection phase. So if ENABLE PARITY BIT (Register 2, bit 5) is set, the PARITY ERROR bit should be sampled to make sure that there is no parity error.

The appropriate settings for the DMA Status Register and Current SCSI Bus Register during a selection/ reselection interrupt are shown below.

DMA Status Register—5 Read Only



Current SCSI Bus Status Register—4 Read Only



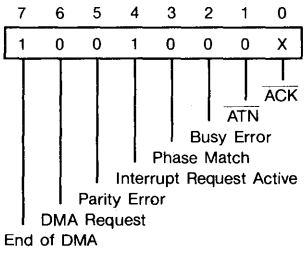
The select interrupt is disabled by writing all zeros into the ID Select Register (4)

End of Process (EOP) Interrupt

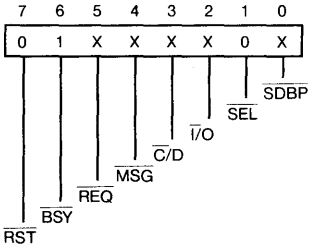
An end of process signal (EOP) occurring during a DMA transfer (DMA MODE active), sets the END OF DMA status bit (Register 5, bit 7) and generates an interrupt. ENABLE EOP INTERRUPT bit (Register 2, bit 3) is set. EOP is not recognized unless EOP, DACK and either IOR or IOW are concurrently active time. DMA transfers will still occur if EOP is asserted.

The appropriate settings for the DMA Status Register and the Current SCSI Bus Status Register during an EOP interrupt, are shown below.

DMA Status Register—5 Read Only



Current SCSI Bus Status Register—4 Read Only



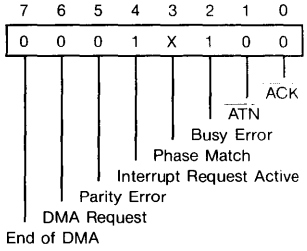
This interrupt is disabled by resetting the ENABLE EOP INTERRUPT bit.

Loss of Busy Interrupt

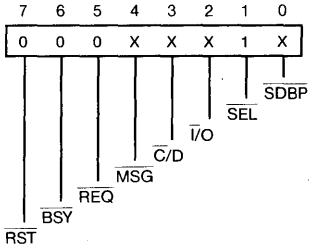
This interrupt is generated if the BSY signal goes false (indicating disconnection of the SCSI bus) for at least a bus-settle delay period of 400 nanoseconds.

The appropriate settings for the DMA Status Register and the Current SCSI Bus Status Register during a loss of BSY interrupt, are shown below.

DMA Status Register—5 Read Only



Current SCSI Bus Status Register—4 Read Only



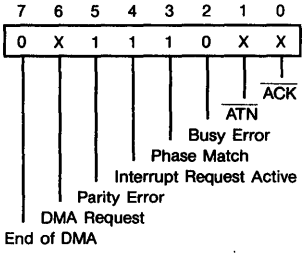
The Loss of Busy Interrupt is disabled by resetting the MONITOR BUSY bit.

Parity/Error Interrupt

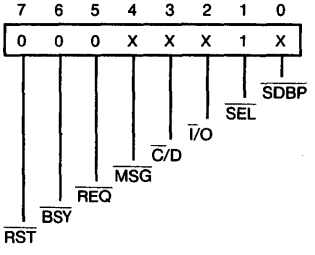
Parity status is checked by reading the Current SCSI Data Register. If the PARITY ERROR bit is set, an interrupt will be generated, provided that the ENABLE PARITY CHECK bit (5) and ENABLE PARITY INTERRUPT bit (Register 2, bit 4) are set in the Mode Register (Register 2, bit 5). The parity checking feature can be used without generating a parity error interrupt if the ENABLE PARITY CHECK bit is disabled.

The appropriate settings for the DMA Status Register and the Current SCSI Bus Status Register during Parity Error interrupt, are shown below.

DMA Status Register—5 Read Only



Current SCSI Bus Status Register—4 Read Only

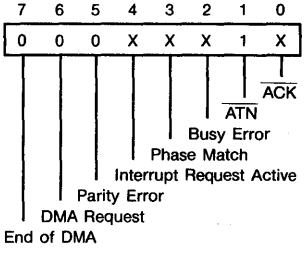


SCSI Bus Reset Interrupt

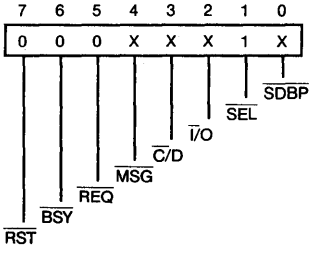
RST going active generates the SCSI Bus Reset Interrupt. After a bus clear delay of 800 nanoseconds, the KS53C80 releases all bus signals. This type of interrupt may also be generated by setting ASSERT RST (Register 1, bit 7). Since RST is not latched in the Current SCSI Bus Status Register, this bit may not be set when the register is read. The reset status may then be decided by default.

The appropriate settings for the DMA Status Register and the Current SCSI Bus Status Register during SCSI Bus Reset interrupt, are shown below.

DMA Status Register—5 Read Only



Current SCSI Bus Status Register—4 Read Only



This interrupt may not be disabled.

SCSI Bus Phase Mismatch Interrupt

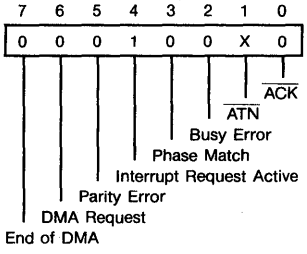
The SCSI bus phases are controlled by I/O, C/D and MSG. These signals are constantly compared with corresponding bits in the Target Command Register (ASSERT I/O, ASSERT C/D, ASSERT MSG). The results of the comparison are stored in DMA Status Register (PHASE MATCH).

If a phase mismatch is detected during a DMA transfer (DMA MODE active) when REQ is active, an interrupt is generated. REQ is not recognized during a phase mismatch, and the KS53C80 is disconnected from the SCSI bus during an initiator send operation. SDB0-7 cannot be driven, even if ASSERT DATA BUS is active.

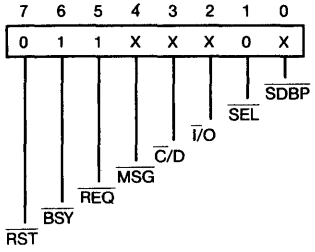
This interrupt is significant only when the device is acting as initiator. It may occur in Target mode, if another device is driving the phase lines to a different state.

The appropriate settings for the DMA Status Register and the Current SCSI Bus Status Register during Bus Phase Mismatch interrupt, are shown below.

DMA Status Register—5 Read Only



Current SCSI Bus Status Register—4 Read Only



The bus phase mismatch interrupt is disabled by resetting the DMA MODE bit.

RESETS CONDITIONS

There are three ways in which the KS53C80 can be reset.

Chip Reset

The chip is reset when the RESET input from the processor goes active and remains active for a minimum time. The chip is initialized, and all internal registers and control logic are cleared. This signal does not reset the SCSI bus.

SCSI Bus Reset (RST) Received

The RST input from the SCSI bus generates an interrupt (IRQ), and resets all internal logic and registers in the chip, with the exception of the IRQ latch, and the ASSERT RST bit 7 in the Initiator Command Register.

SCSI Bus Reset (RST) Issued

RST may also go active on the SCSI bus if the CPU sets ASSERT RST (bit 7) in the Initiator Command Register. RST clears all internal logic and registers, as described above, with the exception of IRQ and ASSERT RST. RST generated in this way remains active until either ASSERT RST is reset, or until a chip reset is initiated.

DC CHARACTERISTICS

This section provides the DC power characteristics for the KS53C80 SCSI Controller.

Absolute Maximum Ratings

Supply Voltage ..... -0.5V to 7.0V
Input Voltage ..... 0V to 5.5V
Output Voltage ..... 0V to V_{CC}
Storage Temperature ..... -65°C to 150°C

Power Requirements

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{CC}	Supply Voltage		4.5	5.0	5.5	V
I_{DD}*	Supply Current		—	10	20	mA
T_A	Ambient Temperature		0.0	25	70	°C

* All input pins should not be floating.

Input Requirements

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{IH}	Input High Level		2.0	—	5.25	V
V_{IL}	Input Low Level		-0.3	—	0.8	V
SCSI Bus						
I_{IH}	Input High Level	V_{IH} = 5.5V	—	—	50	μA
I_{IL}	Input Low Level	V_{IL} = 0V	—	—	-50	μA
Other Pins						
I_{IH}	Input High Level	V_{IH} = 5.5V	—	—	10	μA
I_{IL}	Input Low Level	V_{IL} = 0V	—	—	-10	μA

Output Requirements

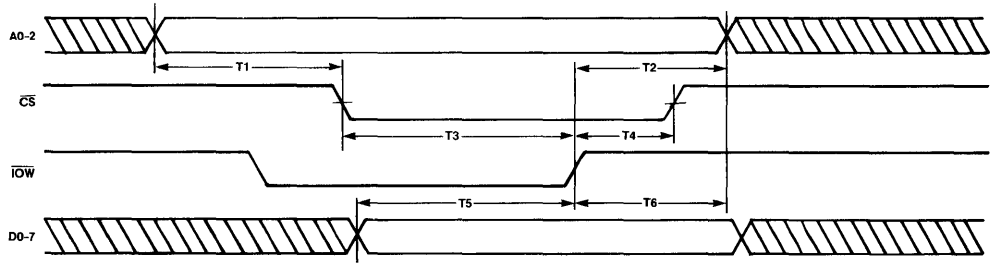
Symbol	Parameter	Condition	Min	Typ	Max	Unit
SCSI Bus						
V_{OL}	Output High Level	V_{CC} = Min., I_{OL} = 48.0mA	—	—	0.5	V
Other Pins						
V_{OH}	Output High Level	V_{SS} = Min., I_{OH} = -3.0mA	2.4	—	—	V
V_{OL}	Output Low Level	V_{SS} = Min., I_{OL} = 7.0mA	—	—	0.5	V

AC SWITCHING CHARACTERISTICS

Figures 4 through 12 provide switching characteristics for a number of typical KS53C80 operations:

- Figure 4. CPU Write Cycle Timing
- Figure 5. CPU Read Cycle Timing
- Figure 6. DMA Read (Block Mode) Target Receive Timing
- Figure 7. DMA Write (Block Mode) Target Send Timing
- Figure 8. DMA Read (Non-Block Mode) Target Receive Timing
- Figure 9. DMA Write (Non-Block Mode) Target Send Timing
- Figure 10. DMA Read (Non-Block Mode) Initiator Receive Timing
- Figure 11. DMA Write (Non-Block Mode) Initiator Send Timing
- Figure 12. Arbitration Timing
- Figure 13. Reset Timing

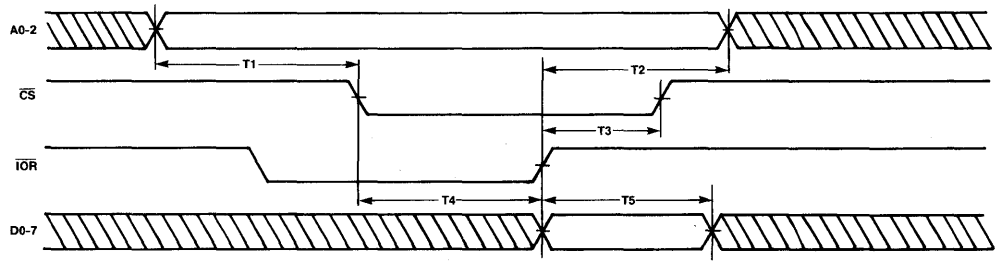
Figure 4. CPU Write Cycle Timing



Name	Description	1.5M/sec Min	1.5M/sec Typ	1.5M/sec Max	3.0M/sec Min	3.0M/sec Typ	3.0M/sec Max	Units
T1	Address Setup to Write Enable	20			10			ns
T2	Address Hold from End Write Enable	20			10			ns
T3	Write Enable Width	70			35			ns
T4	Chip Select Hold from End of $\overline{IOW}$	0			0			ns
T5	Data Setup to End of Write Enable	50			20			ns
T6	Data Hold Time from End of $\overline{IOW}$	30			10			ns

Note: Write enable is the occurrence of $\overline{CS}$ and $\overline{IOW}$.

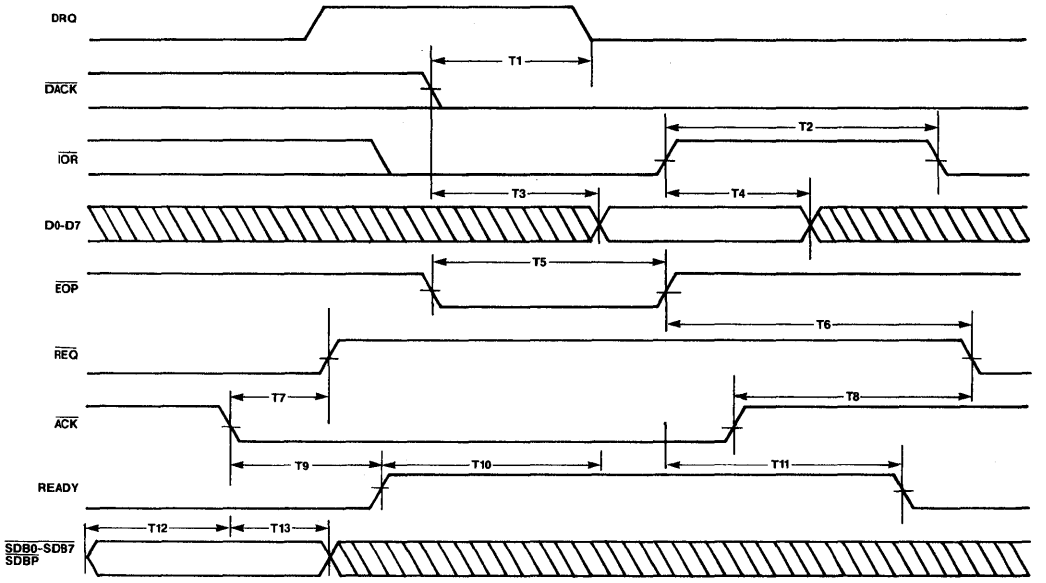
Figure 5. CPU Read Cycle Timing



Name	Description	1.5M/sec Min	1.5M/sec Typ	1.5M/sec Max	3.0M/sec Min	3.0M/sec Typ	3.0M/sec Max	Units
T1	Address Setup to Read Enable	20			10			ns
T2	Address Hold from End Read Enable	20			10			ns
T3	Chip Select Hold from End of $\overline{IOR}$	0			0			ns
T4	Data Access Time from Read Enable			130			65	ns
T5	Data Hold Time from End of $\overline{IOR}$	20			10			ns

Note: Read enable is the occurrence of $\overline{CS}$ and $\overline{IOR}$.

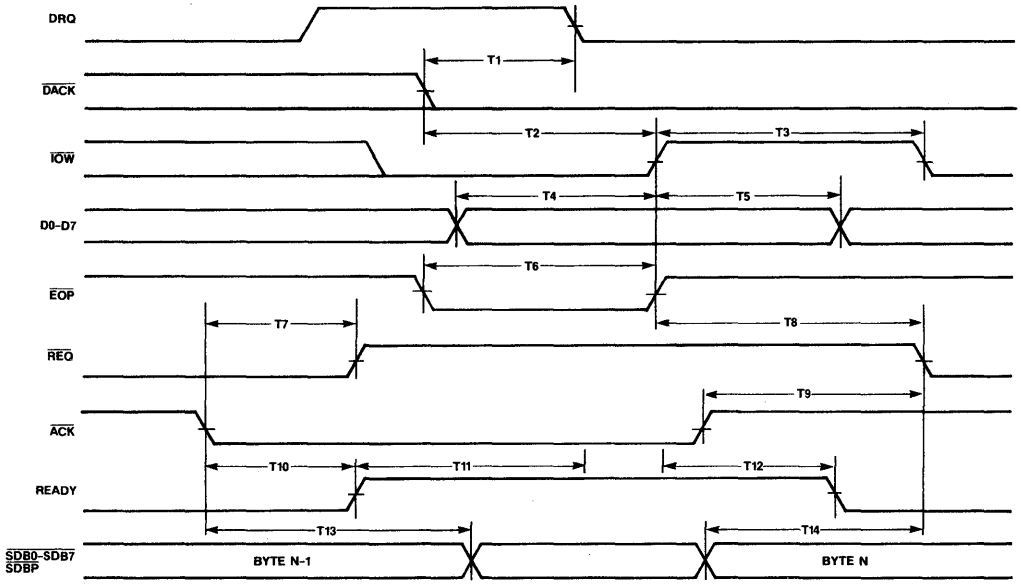
Figure 6. DMA Read (Block Mode) Target Receive Timing



Name	Description	1.5M/sec			3.0M/sec			Units
		Min	Typ	Max	Min	Typ	Max	
T1	DRQ False from DACK True			130			60	ns
T2	IOR Recovery Time	120			60			ns
T3	Data Access Time from Read Enable		100	110			50	ns
T4	Data Hold Time from End of IOR	20			10			ns
T5	Width of EOP Pulse	100			50			ns
T6	IOR False to REQ True (ACK False)			190			70	ns
T7	ACK True to REQ False			125			50	ns
T8	ACK False to REQ True (IOR False)			170			70	ns
T9	ACK True to READY True			140			60	ns
T10	READY True to Valid CPU Data			50			20	ns
T11	IOR False to READY False	20	125	140			70	ns
T12	SCSI DATA Setup Time to ACK True	20			10			ns
T13	SCSI DATA Hold Time from ACK True	50			20			ns

Note: DACK, IOR, and EOP = 1, for at least T5 for EOP pulse recognition. Read enable is DACK and IOR occurrence.

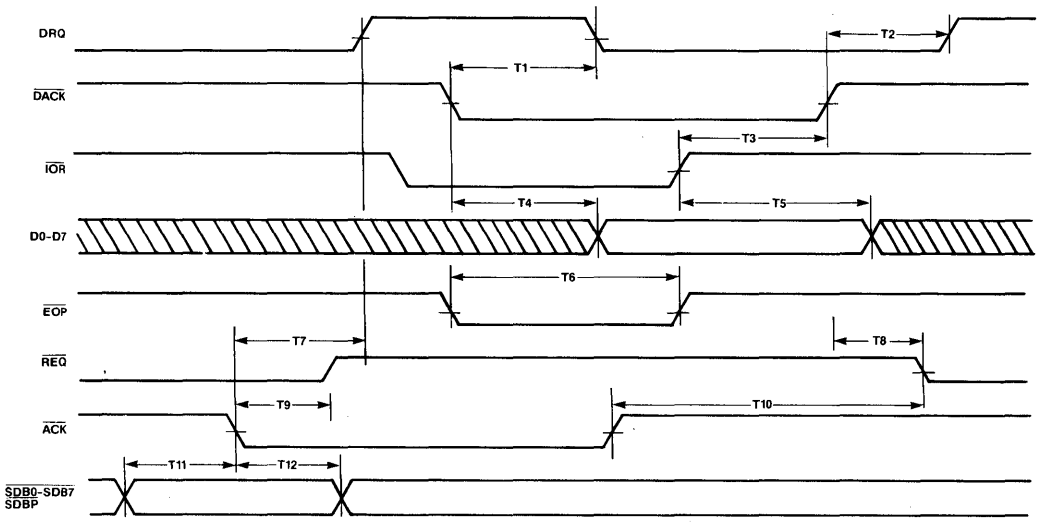
Figure 7. DMA Write (Block Mode) Target Send Timing



Name	Description	1.5M/sec			3.0M/sec			Units
		Min	Typ	Max	Min	Typ	Max	
T1	DRQ False from DACK True	100		130			60	ns
T2	Write Enable Width	100			50			ns
T3	Write Recovery Time	120			60			ns
T4	Data Setup to End of Write Enable	50			20			ns
T5	Data Hold Time from End of IOW	40			20			ns
T6	Width of EOP Pulse	100			50			ns
T7	ACK True to REQ False			125			60	ns
T8	REQ from End of IOW (ACK False)			180			100	ns
T9	REQ from End of ACK (IOW False)			170			90	ns
T10	ACK True to READY True			140			70	ns
T11	READY True to IOW False	70			30			ns
T12	IOW False to READY False	20	130	140			70	ns
T13	DATA Hold Time from ACK True	40			20			ns
T14	Data Setup to REQ True	60			30			ns

Note: DACK, IOW, and EOP = 1, for at least T6 for EOP pulse recognition. Write enable is DACK and IOW occurrence.

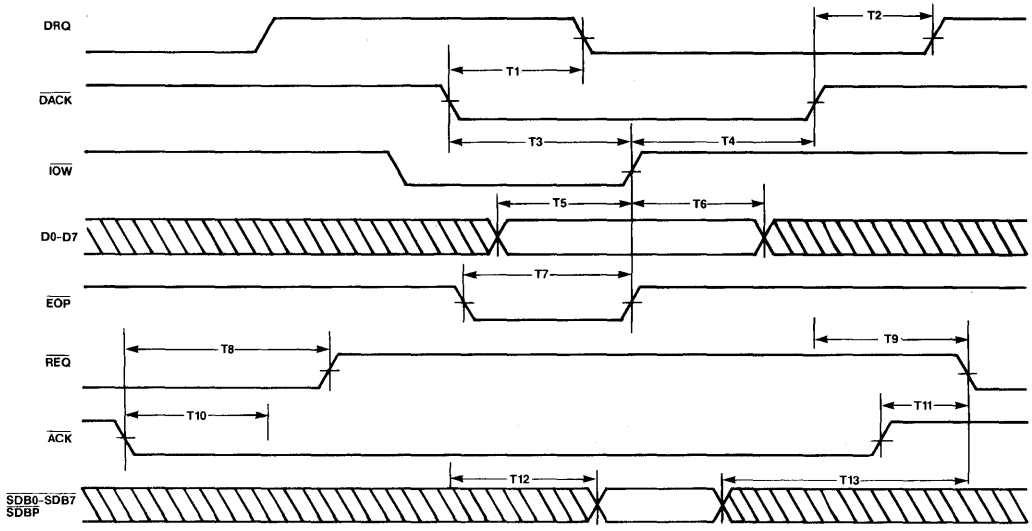
Figure 8. DMA Read (Non-Block Mode) Target Receive Timing



Name	Description	1.5M/sec			3.0M/sec			Units
		Min	Typ	Max	Min	Typ	Max	
T1	DRQ False from DACK and IOR True			130			60	ns
T2	DACK False to DRQ True	30			20			ns
T3	DACK Hold Time from End of IOR	0			0			ns
T4	Data Access Time from Read Enable (IOR and DACK Low)			115			60	ns
T5	Data Hold Time from End of IOR	20			10			ns
T6	Width of EOP Pulse	100			50			ns
T7	ACK True to DRQ True			110			60	ns
T8	DACK False to REQ True (ACK False)			150			70	ns
T9	ACK True to REQ False			125			60	ns
T10	ACK False to REQ True (DACK False)			150			70	ns
T11	SCSI DATA Setup Time to ACK	20			10			ns
T12	SCSI DATA Hold Time from ACK	50			20			ns

Note: DACK, IOR, and EOP = 1, for at least T6 for EOP pulse recognition. Write enable is DACK and IOR occurrence.

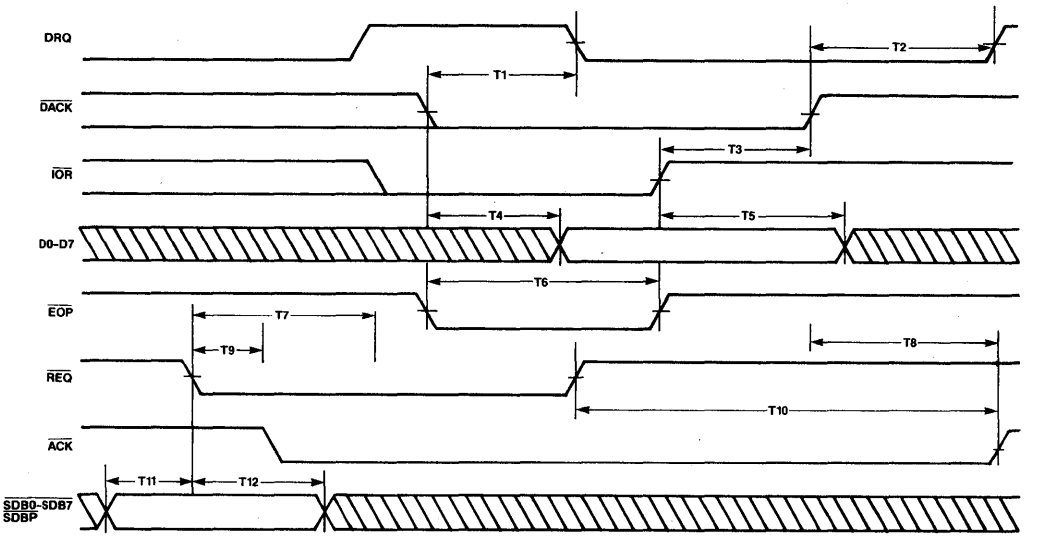
Figure 9. DMA Write (Non-Block Mode) Target Send Timing



Name	Description	1.5M/sec			3.0M/sec			Units
		Min	Typ	Max	Min	Typ	Max	
T1	DRQ False from DACK True			130			60	ns
T2	DACK False to DRQ True	30			20			ns
T3	Write Enable Width	100			50			ns
T4	DACK Hold from End of IOW	0			0			ns
T5	Data Setup to End of Write Enable	50			20			ns
T6	Data Hold Time from End of IOW	40			20			ns
T7	Width of EOP Pulse	100			50			ns
T8	ACK True to REQ False			125			60	ns
T9	REQ from End of DACK (ACK False)			150			70	ns
T10	ACK True to DRQ True			110			50	ns
T11	REQ from End of ACK (DACK False)			150			70	ns
T12	SCSI DATA Hold Time from Write Enable	15			10			ns
T13	SCSI DATA Setup to REQ True	60			30			ns

Note: DACK, IOW, and EOP = 1, for at least T7 for EOP pulse recognition. Write enable is DACK and IOW occurrence.

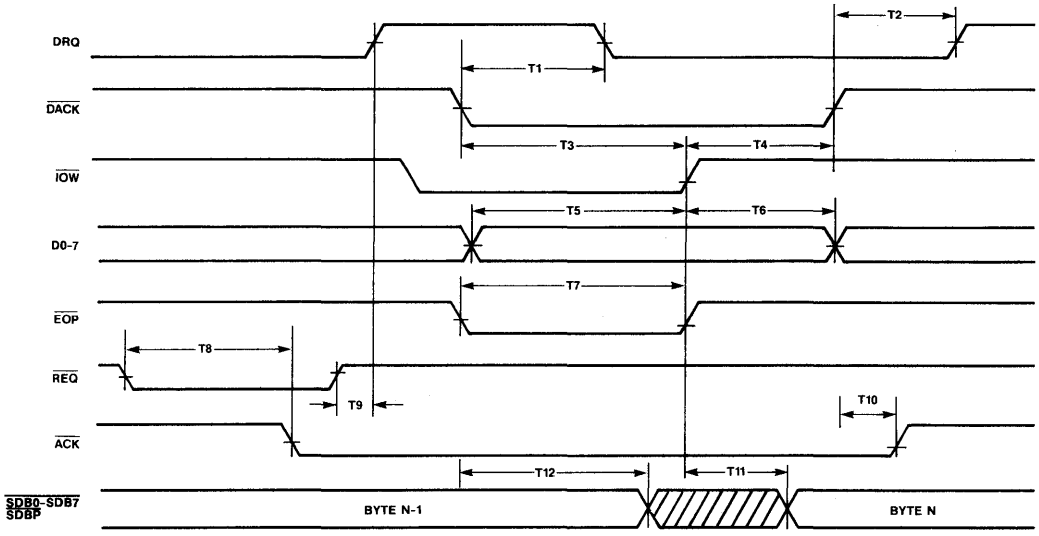
Figure 10. DMA Read (Non-Block Mode) Initiator Receive Timing



Name	Description	1.5M/sec			3.0M/sec			Units
		Min	Typ	Max	Min	Typ	Max	
T1	DRQ False from $\overline{DACK}$ True			130			60	ns
T2	$\overline{DACK}$ and $\overline{IOR}$ False to $\overline{DRQ}$ True	30			20			ns
T3	$\overline{DACK}$ Hold Time from End of $\overline{IOR}$	0			0			ns
T4	Data Access Time from Read Enable			115			60	ns
T5	Data Hold Time from End of $\overline{IOR}$	20			10			ns
T6	Width of $\overline{EOP}$ Pulse	100			50			ns
T7	$\overline{REQ}$ True to DRQ True			150			70	ns
T8	$\overline{DACK}$ False to $\overline{ACK}$ ($\overline{REQ}$ False)			160			80	ns
T9	$\overline{REQ}$ True to $\overline{ACK}$ True			160			80	ns
T10	$\overline{REQ}$ False to $\overline{ACK}$ False ($\overline{DACK}$ False)			140			70	ns
T11	SCSI DATA Setup Time to $\overline{REQ}$	20			10			ns
T12	SCSI DATA Hold Time from $\overline{REQ}$	50			20			ns

Note: $\overline{DACK}$, $\overline{IOR}$, and $\overline{EOP}$ = 1, for at least T6 for $\overline{EOP}$ pulse recognition. Write enable is $\overline{DACK}$ and $\overline{IOR}$ occurrence.

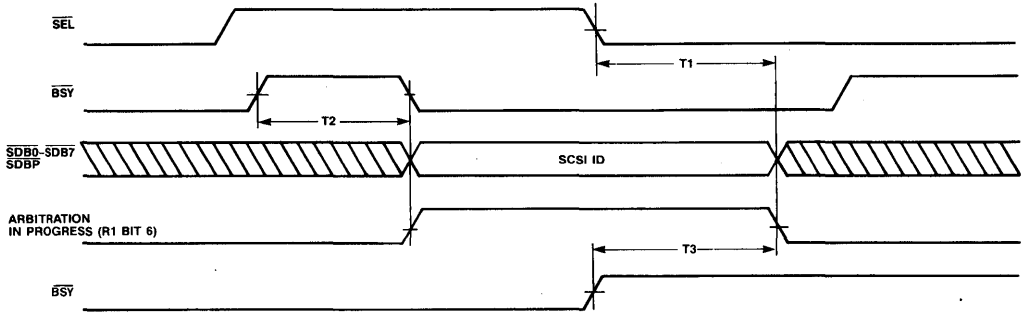
Figure 11. DMA Write (Non-Block Mode) Initiator Send Timing



Name	Description	1.5M/sec			3.0M/sec			Units
		Min	Typ	Max	Min	Typ	Max	
T1	DRQ False from DACK True			130			60	ns
T2	DACK False to DRQ True	30			20			ns
T3	Write Enable Width	100			50			ns
T4	DACK Hold from End of IOW	0			0			ns
T5	Data Setup to End or Write Enable	50			20			ns
T6	Data Hold Time from End of IOW	40			20			ns
T7	Width of EOP Pulse	100			50			ns
T8	REQ True to ACK True			160			80	ns
T9	REQ False to DRQ True			110			50	ns
T10	DACK False to ACK False			150			70	ns
T11	IOW False to Valid SCSI Data			100			50	ns
T12	DATA Hold Time from Write Enable	15			10			ns

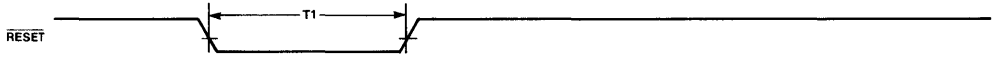
Note: DACK, IOW, and EOP = 1, for at least T7 for EOP pulse recognition. Write enable is DACK and IOW occurence.

Figure 12. Arbitration Timing



Name	Description	1.5M/sec			3.0M/sec			Units
		Min	Typ	Max	Min	Typ	Max	
T1	SCSI Bus Clear from SEL True			0.6			0.6	μs
T2	ARBITRATE Start from BSY False	1.2		2.2	1.2		2.2	μs
T3	SCSI Bus Clear from BSY False	0.4		1.1	0.4		1.1	μs

Figure 13. Reset Timing



Name	Description	1.5M/sec			3.0M/sec			Units
		Min	Typ	Max	Min	Typ	Max	
T1	Minimum Width of Reset	100			50			ns

PACKAGING

The Samsung KS53C80 SCSI controller is available in two packages. Figure 13 shows the dimensions of the 44-pin PLCC package. Figure 14 shows the dimensions of the 48-pin DIP package.

Figure 14. KS53C80 44-Pin PLCC Package

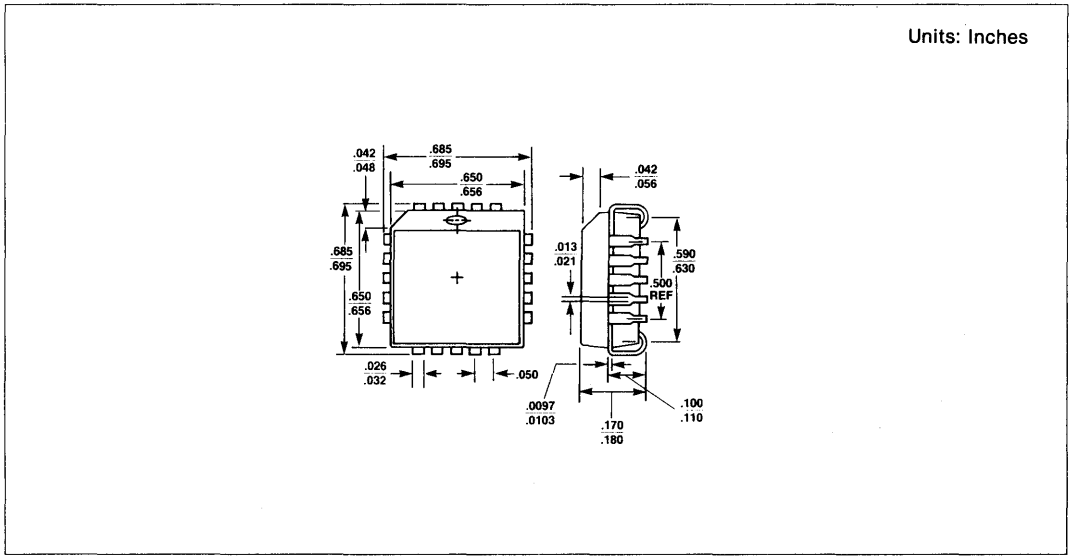
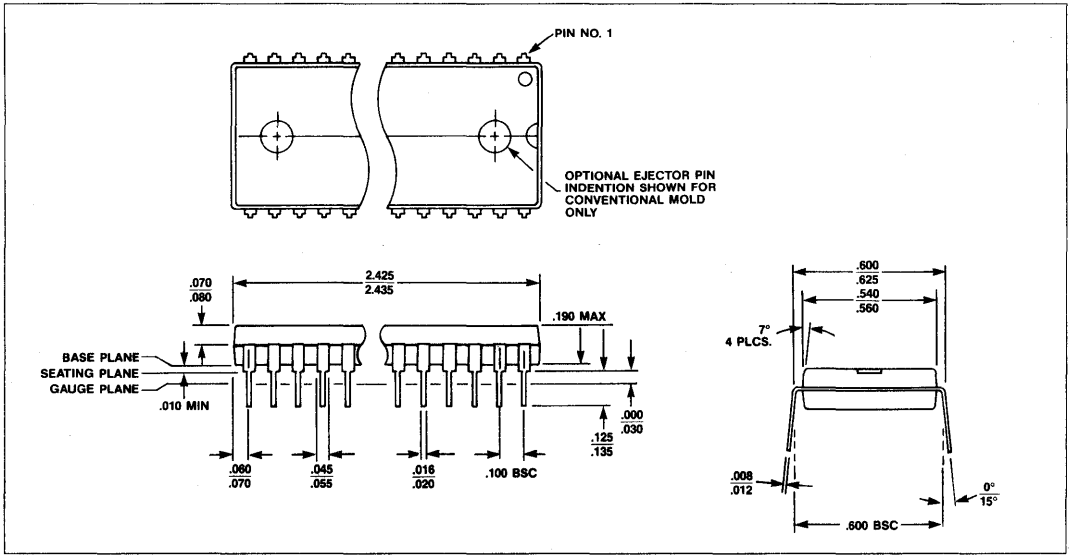


Figure 15. KS53C80 48-Pin DIP Package



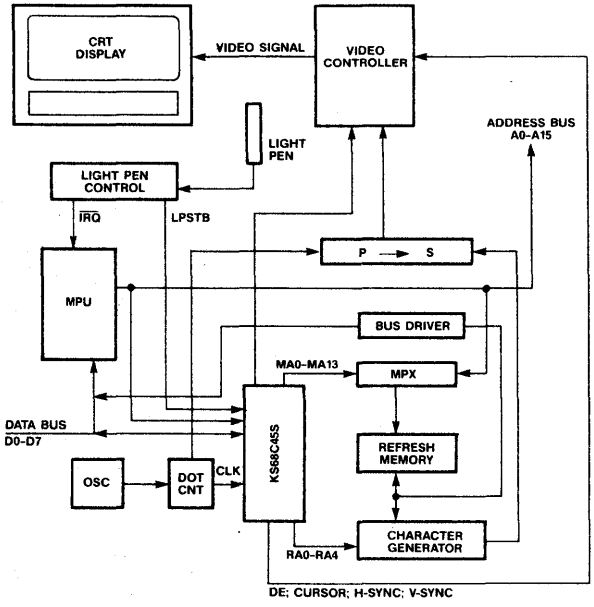
KS68C45S

CRT CONTROLLER

FEATURES/BENEFITS

- **Programmable:**
  - **— Number of characters displayed**
  - **— Interlace or non-interlace scan modes**
  - **— Cursor format and blink rate**
  - **— Cursor skew**
  - **— Horizontal and vertical SYNC signal**
  - **— Display timing**
- **3.7 or 6 MHz display operation**
- **Bufferless line refresh**
- **No DMA required**
- **Built-in light-pen detection function**
- **Supports paging and scrolling by page, line, or character**
- **TTL-compatible low-power CMOS**
- **512K address space for graphic systems**
- **16K refresh memory for character or semi-graphic displays**
- **Single +5V power supply**

Figure 1. System Block Diagram



DESCRIPTION

The KS68C45S CRT Controller (CRTC) provides an interface for computers to raster-scan type CRT displays. The Controller's data and control lines are fully compatible with the 6800 MPU. The Controller generates timing signals necessary for the raster-scan type CRT display based on specifications programmed into the Controller's registers.

Because it is programmable, the CRT Controller is capable of a wide-range of CRT display-types from small character displays up to raster-type full-graphic displays as well as large, limited-graphic displays.

Figure 2a: KS68C45S 44-Pin PLCC

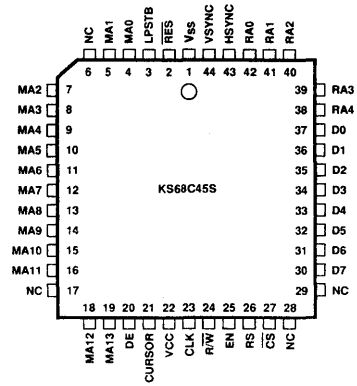


Figure 2b: KS68C45S Pin DIP

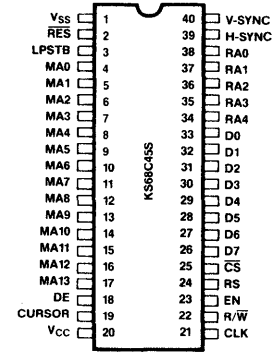


Table 1: KS68C45S Signal Descriptions

The CRTC provides 13 signals to the MPU and 25 interface signals to the CRT display.

Symbol	Type	Name and Function
Processor Interface		
D_0-D_7	I/O	**Bi-directional Data Lines:** Used for data transfer between the CRTC and MPU. Outputs of the data bus are 3-state buffers that remain in the high-impedance state unless the MPU performs a CRTC read operation.
EN	I	**Enable:** Input which enables the data bus input/output buffers and clocks data to and from the CRTC. This signal is usually derived from the processor clock. The HIGH-to-LOW transition is the active edge.
$\overline{CS}$	I	**Chip Select:** Input which selects the CRTC, when LOW, to read or write to the internal register file. This signal should only be active when there is a valid stable address being decoded from the processor.
RS	I	**Register Select:** Input used to access internal registers. A LOW on this pin allows writes into the Address Register and allows reads from the Status Register. When HIGH, the data register is selected. The contents of the Address Register = the identity of the register accessed when RS is high.
R/$\overline{W}$	I	**Read/Write:** Input which determines whether the internal register file is written to (LOW) or read from (HIGH).
$\overline{RES}$	I	**Reset:** When LOW, forces the CRTC into the following status: 1) All counters in the CRTC are cleared and the device stops the display operation. 2) All outputs go LOW. Control registers in the CRTC are not affected, and remain unchanged. This signal has the following restrictions for usage: 1) $\overline{RES}$ is effective only when Light-Pen Strobe (LPSTB) is LOW. 2) The CRTC starts the display operation immediately after $\overline{RES}$ goes HIGH. Display Enable (DE) and the cursor are not active until after the first frame has been displayed. The $\overline{RES}$ input and the LPSTB input are encoded as shown:

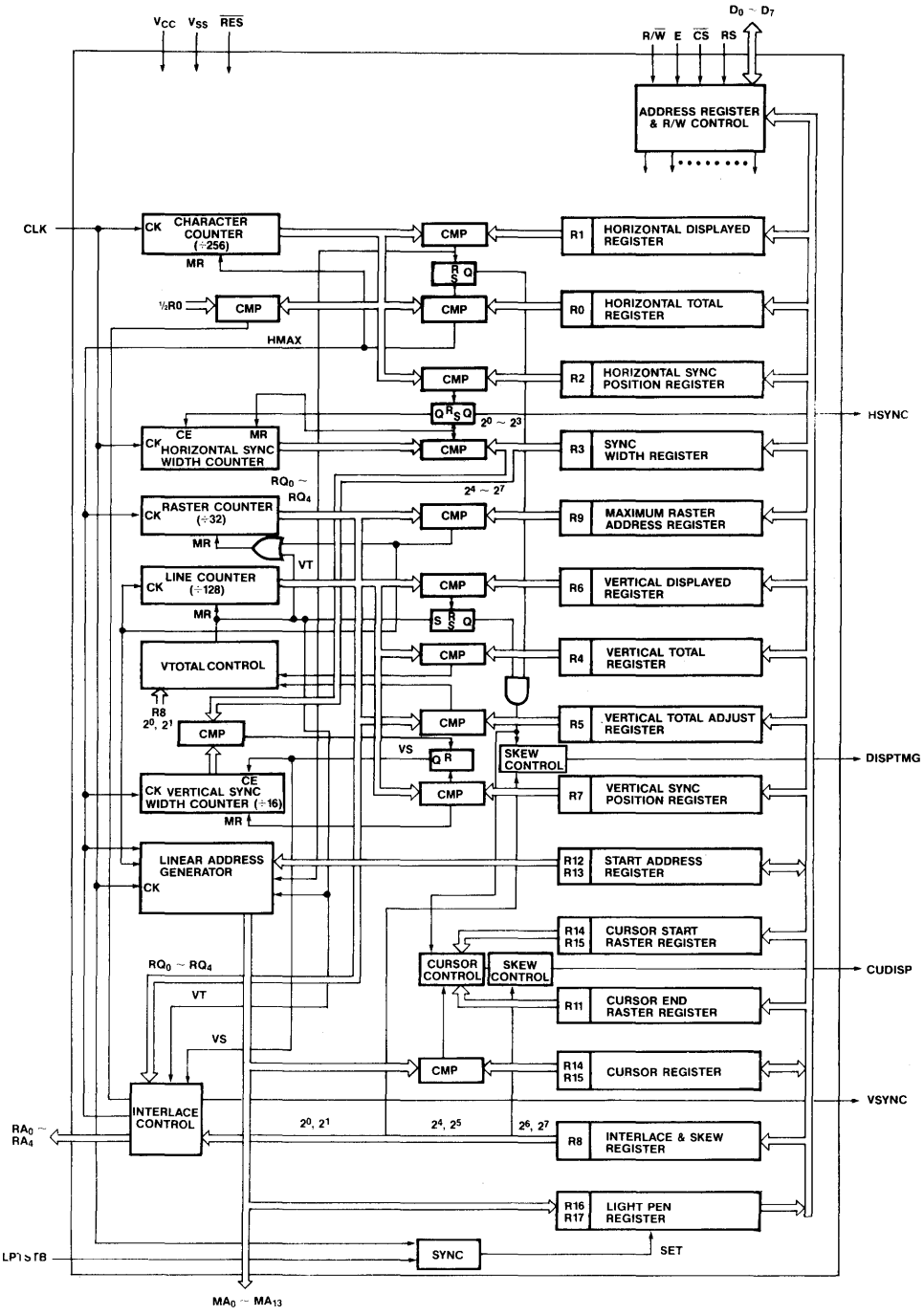
$\overline{RES}$	LPSTB	Operating Mode
0	0	Reset
0	1	Test Mode
1	0	Normal Mode
1	1	Normal Mode

After $\overline{RES}$ has gone LOW (and LPSTB = 0), MA_0-MA_{13} and RA_0-RA_4 will be driven low on the falling edge of CLK. $\overline{RES}$ must remain low for at least one cycle of the character clock (CLK).

Table 1: KS68C45S Signal Descriptions (Continued)

Symbol	Type	Name and Function
Internal Signals to the CRT Display		
CLK	I	**Character Clock:** A standard clock input signal which defines character timing for the CRTC display operation. This signal is normally derived from the external dot-timing logic.
H-SYNC	O	**Horizontal Sync:** Provides horizontal synchronization for the display device.
V-SYNC	O	**Vertical Sync:** Provides vertical synchronization for the display device.
DE	O	**Display Enable:** Defines the display period in horizontal and vertical raster scanning. When HIGH, this signal enables the video signal.
MA_0-MA_{13}	O	**Refresh Memory Address 0-13:** Used to address up to 16K-words of frame buffer for character storage and display refresh operations. The starting scan address is fully programmable and the ending scan address is determined by the total number of characters displayed, which is also programmable in terms of characters/line and lines/frame. The buffer can support up to 8 pages at 2000 characters per page.
RA_0-RA_4	O	**Raster Address 0-4:** Selects the raster of the character generator or graphic-pattern generator.
CURSOR	O	**Cursor:** Used to display the cursor on the CRT screen. This output is inhibited while DE is LOW. This output is normally mixed with the video signal. The cursor may be programmed to any character in the address field. Within the character, the cursor may be programmed to be any block of scan lines, since the start-scan line and the end-scan line are both programmable.
LPSTB	I	**Light Pen Strobe:** Edge-sensitive input which accepts a strobe pulse detected by the light-pen control circuit. When this signal is activated, the refresh memory address (MA_0-MA_{13}) is stored in the 14-bit light-pen register. Software must correct the stored refresh-memory address for the delay time of the display device, light pen, and light-pen control circuits.
V_{CC}		5V ± 5%.
V_{SS}		Ground.

Figure 3. CRTC Block Diagram



REGISTER DESCRIPTION

Table 2: Internal Registers Assignment

		Address Register										Data Bit							
CS	RS	4	3	2	1	0	Register #	Register Name	Program Unit	Read	Write	7	6	5	4	3	2	1	0
1	X	X	X	X	X	X			—	—	—								
0	0	X	X	X	X	X	AR	Address Register	—	X	O								
0	1	0	0	0	0	0	R0	Horizontal Total*	Character	X	O								
0	1	0	0	0	0	1	R1	Horizontal Displayed	Character	X	O								
0	1	0	0	0	1	0	R2	Horizontal Sync* Position	Character	X	O								
0	1	0	0	0	1	1	R3	Sync Width	Vertical-Raster, Horizontal-Character	X	O	wv3	wv2	wv1	wv0	wh3	wh2	wh1	wh0
0	1	0	0	1	0	0	R4	Vertical Total*	Line	X	O								
0	1	0	0	1	0	1	R5	Vertical Total Adjust	Raster	X	O								
0	1	0	0	1	1	0	R6	Vertical Displayed	Line	X	O								
0	1	0	0	1	1	1	R7	Vertical Sync* Position	Line	X	O								
0	1	0	1	0	0	0	R8	Interlace & Skew	—	X	O	C1	C0	D1	D0			V	S
0	1	0	1	0	0	1	R9	Maximum Raster Address	Raster	X	O								
0	1	0	1	0	1	0	R10	Cursor Start Raster	Raster	X	O		B	P					
0	1	0	1	0	1	1	R11	Cursor End Raster	Raster	X	O								
0	1	0	1	1	0	0	R12	Start Address (H)	—	O	O								
0	1	0	1	1	0	1	R13	Start Address (L)	—	O	O								
0	1	0	1	1	1	0	R14	Cursor (H)	—	O	O								
0	1	0	1	1	1	1	R15	Cursor (L)	—	O	O								
0	1	1	0	0	0	0	R16	Light Pen (H)	—	O	X								
0	1	1	0	0	0	1	R17	Light Pen (L)	—	O	X								

Notes:

1. The Registers marked *: (Written Value) = (Specified Value) - 1
2. Written Value of R9 is mentioned below.
   1) Non-interlace Mode
      Interlace Sync Mode (Written Value Nr) = (Specified Value) - 1
   2) Interlace Sync & Video Mode
      (Written Value Nr) = (Specified Value) - 2
3. C0 and C1 specify skew of CUDISP output signal.
   D0 and D1 specify skew of DISPTMG output signal.
   When S is "1", V specifies video mode. S specifies the Interlace Sync Mode.
4. B specifies the cursor blink. P specifies the cursor blink period.
5. wv0 ~ wv3 specify the pulse width of Vertical Sync Signal.
   wh0 ~ wh3 specify the pulse width of Horizontal Sync Signal.
6. R0 is ordinally programmed to be odd number in interlace mode.
7. O: Yes, X; No
8. The X bits are don't care.

FUNCTIONAL DESCRIPTION

The KS68C45S CRT Controller consists of programmable horizontal and vertical timing generators, a programmable linear address register, programmable cursor logic, a light-pen capture register, and control circuitry for interface to a processor bus.

All CRTC timing is derived from the CLK, usually the output of an external dot-race counter. Coincidence circuits continuously compare counter contents to the contents of the programmable register file, R_0–R_{17}. For horizontal timing generation, comparisons result in: 1) horizontal synch pulse (H-SYNC) of a frequency, position, and width determined by the registers; and 2) horizontal display signal of a frequency, position, and duration determined by the registers.

The horizontal counter produces H clock which drives the scan-line counter and vertical control. The contents of the raster counter are continuously compared to the maximum scan-line address register. A coincidence resets the raster counter and clocks the vertical counter.

Comparisons of vertical counter contents and vertical registers result in: 1) vertical sync pulse (V-SYNC) of a frequency and position determined by the registers; and, 2) vertical display signal of a frequency and position determined by the registers.

The vertical control logic has two other functions:

1) To generate row selects, RA_0–RA_4, from the raster counter for the corresponding interface or non-interlace modes.
2) To extend the number of scan lines in the vertical total by the amount programmed in the vertical-total adjust register.

The linear address generator is driven by the CLK and locates the relative positions of characters in memory with their positions on the screen. Fourteen lines, MA_0–MA_{13}, are available for addressing four pages of 4K characters each, eight pages of 2K characters each, or any combination totalling 16K characters. The linear address generator repeats the same sequence of addresses for each scan line of a character row.

The cursor logic determines the cursor location, size, and clock rate on the screen. These features are all programmable.

The light-pen strobe going HIGH causes the current contents of the address counter to be latched in the light-pen register. The contents of the light-pen register are subsequently read by the processor.

Internal CRT Controller registers are programmed by the processor through the data bus, D_0–D_7, and the control signals: R/$\overline{W}$, $\overline{CS}$, RS, and EN.

OPERATIONAL DESCRIPTION

Control Modes

There are four control modes:

1) Non-interlace Mode
2) Interlace Sync Mode
3) Interlace Sync and Video Mode (even)
4) Interlace Sync and Video Mode (odd)

Non-Interlace Mode

In Non-Interlace Mode each field is scanned twice, and addresses RA_0–RA_4 are counted up one, from zero.

Interlace Sync Mode

In Interlace Sync Mode, the raster address in the even and odd fields is the same as that addressed in the Non-Interlace Mode. One character pattern is displayed in both fields, but, the displayed position of that character is 1/2 the raster space down from its position in the even field.

Interlace Sync and Video Mode (even)

TRN (total number of rasters) is programmed to be even. An even-field is output by even raster-addressing.

Interlace Sync and Video Mode (odd)

TRN is programmed to be odd. An odd-field is output by odd raster-addressing. Odd and even addresses are reversed to the odd and even lines in each field. This reversal creates a more stable interlace display than when TRN is programmed even.

Cursor Control

Start and end values are programmed to the raster register and must meet the condition Cursor Start $\leq$ Cursor End $\leq$ Maximum raster address register.

Internal Registers

Internal registers are:

Register Symbol	Register Name
AR	Address Register
R_0	Horizontal Total Register
R_1	Horizontal Displayed Register
R_2	Horizontal Sync Position Register
R_3	Sync Width Register
R_4	Vertical Total Register
R_5	Vertical Total Adjust Register
R_6	Vertical Displayed Register
R_7	Vertical Sync Position Register
R_8	Interlace and Skew Register
R_9	Maximum Raster Address Register
R_{10}	Cursor Start Raster Register
R_{11}	Cursor End Raster Register
R_{12}, R_{13}	Start Address Register
R_{14}, R_{15}	Cursor Register
R_{16}, R_{17}	Light Pen Register

Table 3: Functional Description of Internal Registers

AR — Address Register

A 5-bit register used to select the internal control registers (R_0-R_{17}). This register is the address of one of the control registers. In order to access the control registers, the address of the control register must be written to the Address Register. (Programming data from binary 8 to binary 13 into the Address Register produces no results.)

To select AR, RS and $\overline{CS}$ must equal 0.

R_0 — Horizontal Total Register

An 8-bit register used to program the total number of horizontal characters per line. This number must include the retrace period and is programmed according to the CRT specification. If N is the total number of characters, N-1 is programmed to this register. N must be even for the Interlace Mode.

R_1 — Horizontal Displayed Register

An 8-bit register used to program the number of horizontal displayed characters per line. Any number less than the total number of horizontal characters can be programmed.

R_2 — Horizontal Sync Position Register

An 8-bit register used to program the horizontal sync position as a multiple of the character clock period. Any number less than the total horizontal number can be programmed. If H is the character number of the horizontal sync position, H-1 is programmed to this register.

The value of this register determines the optimum horizontal position. The display position on the CRT screen moves to the left if the programmed value of this register is increased. The display position on the CRT screen moves to the right if the programmed value of this register is decreased.

R_3 — Sync Width Register

7							0
V	V	V	V	H	H	H	H

An 8-bit register used to program the horizontal and vertical sync pulse width. The horizontal sync (H-SYNC) width is programmed to the least-significant 4 bits of R_3 as multiples of the character clock period. Zero cannot be programmed. The vertical sync (V-SYNC) is programmed to the most-significant 4 bits of R_3 as multiples of the raster period. If 0 is programmed in the most-significant 4 bits, a raster period of 16 (16H) is specified.

Table 4: Raster Scan Mode

Raster Scan Mode (2^1, 2^0)	V	S
Non-Interlace Mode	0 1	0 0
Interlace Sync Mode	0	1
Interlace Sync & Video Mode	1	1

R_4 — Vertical Total Register

A 7-bit register used to program the total number of lines per frame, including the vertical retrace period. This register must be programmed according to the CRT specification. If L is the total number of lines, L-1 is programmed to this register.

R_5 — Vertical Total Adjust Register

A 5-bit register used to program the optimum number to adjust the total number of rasters per field. This register is also used to decide the vertical deflection frequency.

R_6 — Vertical Displayed Register

A 7-bit register used to program the number of displayed character rows on the CRT screen. Any number less than the total number of vertical characters can be programmed.

R_7 — Vertical Sync Position Register

A 7-bit register used to program the vertical sync position on the screen as multiples of the horizontal character line period. Any number less than the total number of vertical characters can be programmed. If V is the character number of the vertical sync position, V-1 is programmed to this register.

If the programmed value of this register is decreased, the display position is moved down on the CRT screen. If the programmed value of this register is increased, the display position is moved up on the screen.

Table 5: Pulse Width of Vertical Sync Signal

Vertical Sync Signal

Pulse Width	VSW 2^7	2^6	2^5	2^4
16H	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1

H: Raster Period

Table 6: Pulse Width of Horizontal Sync Signal

Horizontal Sync Signal

Pulse Width	HSW 2^3	2^2	2^1	2^0
—	0	0	0	0
1 CH	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1

CH: Character Clock Period
HSW = 0 cannot be used

R_8 — Interlace and Skew Register

7							0
C1	C0	D1	D0			V	S

An 8-bit register used to program the raster scan mode, the skew of CURSOR, and Display Enable (DE).

In Table 7, bits 4 and 5 specify DE output delay (skew). Bits 6 and 7 specify CURSOR output delay (skew) in two characters, starting from 0. If 3 is programmed to these bits, the signal is not output.
Bits 2 and 3 are not used.
Bits 0 and 1 (V, S) specify scan modes.

Table 7: DE and Cursor Skew

DE Skew (2^5, 2^4)	D0	D1
Non-skew	0	0
One-character skew	1	0
Two-character skew	0	1
Non-output	1	1
Cursor Skew Bits (2^7, 2^6)	**C0**	**C1**
Non-skew	0	0
One-character skew	1	0
Two-character skew	0	1
Non-output	1	1

R_9 — Maximum Raster Address Register

A 5-bit register used to program the maximum raster address and to define the total number of rasters per character, including line space.

In Interlace Sync Mode where TNR equals the Total Number of Rasters, TNR equals 5. Where Nr equals the raster number and equals the programmed value, Nr equals 4. Where X equals TNR, X - 1 is programmed.

In Non-interlace Mode, TNR = 5, Nr = 4, X - 2 is programmed.

In Interlace and Video Mode, TNR = 5, Nr = 3, X - 1 is programmed.

R_{10} — Cursor Start Raster Register

A 7-bit register. The cursor start raster address is programmed in the least-significant 5 bits. The cursor display mode is programmed to the most-significant 2 bits.

Table 8: Cursor Display Mode

Cursor Display Mode (2^6, 2^5)	B	P
Non-blink	0	0
Cursor Non-display	0	1
Blink 16 Field Period	1	0
Blink 32 Field Period	1	1

R_{11} — Cursor End Raster Register

A 5-bit register used to program the cursor end raster address.

R_{12}, R_{13} — Start Address Register

The two registers form a single 16-bit register used to program the first address to be read out of refresh memory, and used to program for paging and scrolling. The most significant two bits of R_{12} are always 0.

R_{14}, R_{15} — Cursor Register (Read/Write)

The two registers form a single 16-bit register used to store the cursor location. The most significant two bits of R_{14} are always 0.

R_{16}, R_{17} — Light-Pen Register (Read Only)

The two registers form a single 16-bit register used to store the detected address of the light pen. The most significant two bits of R_{16} are always 0.

Table 9: Programmed Values into the Registers

Register Name	Register	Value
Horizontal Total Horizontal Displayed Horizontal Sync Position	R0 R1 R2	Nht Nhd Nhsp
Sync Width	R3	Nvsw, Nhsw
Vertical Total Vertical Total Adjust Vertical Displayed Vertical Sync Position	R4 R5 R6 R7	Nvt Nadj Nvd Nvsp
Interlace & Skew Max. Raster Address	R8 R9	 Nr
Cursor Start Raster Cursor End Raster	R10 R11	
Start Address (H) Start Address (L)	R12 R13	0 0
Cursor (H) Cursor (L)	R14 R15	
Light Pen (H) Light Pen (L)	R16 R17	

Table 10: Raster Address Output

No. of Rasters in a Line		Odd Field	Even Field
Even		Odd Address	Even Address
Odd	Odd Line	Even Address	Odd Address
	Even Line	Odd Address	Even Address

Restrictions on Internal Register Programming

$0 \leq Nhsp \leq Nht$
$0 \leq Nvsp \leq Nvt$ (see note 1)
$0 < Nhd < Nht + 1 \leq 256$
$0 < Nvd < Nvt + 1 \leq 128$
$0 \leq Ncs \leq Nce \leq Nr$ (for Non-interlace and Interlace Sync Modes)
$0 \leq Ncs \leq Nce \leq Nr + 1$ (for Interlace Sync and Video Mode)
$2 \leq Nr \leq 30$ (Interlace Sync and Video Mode)
$3 \leq Nht$ (not for Non-Interlace Mode)
$5 \leq Nht$ (Non-interlace Mode only)

Notes:
1. The pulse width is changed ±1/2 the raster time when the vertical sync signal extends over two fields in the Interlace Mode.
2. Ncs = Cursor start, Nce = Cursor end

Figure 4: Video Signal and Character Display

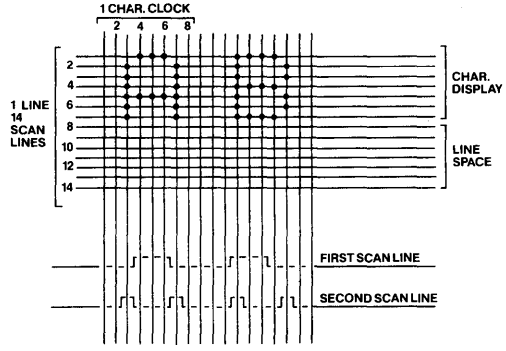
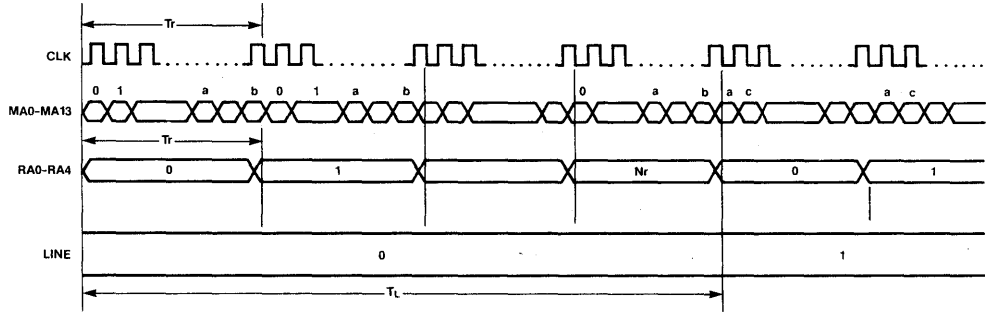


Figure 5: Raster Line Period Timing Chart



Notes:
Tr = Raster Period
T_L = Line Period = (Nr + 1) * Tr
a = Nhd
b = Nht
c = Nhd + 1
Nr = Max. Raster Address

Figure 6: CRT Screen Format

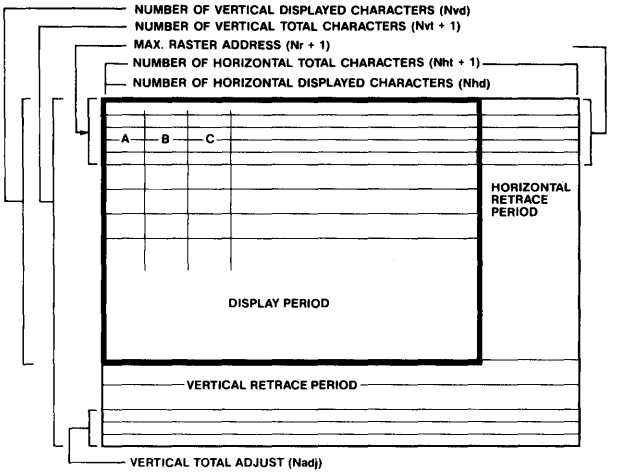
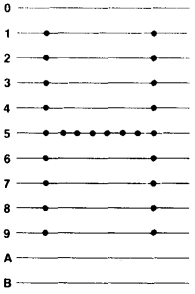
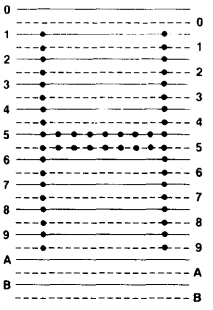


Figure 7: Raster Scan Display

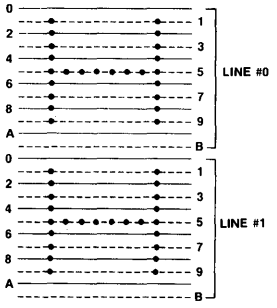
Non-Interlace Mode



Interlace Sync Mode

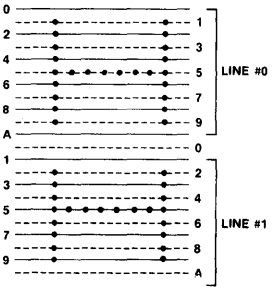


Interlace Sync & Video Mode



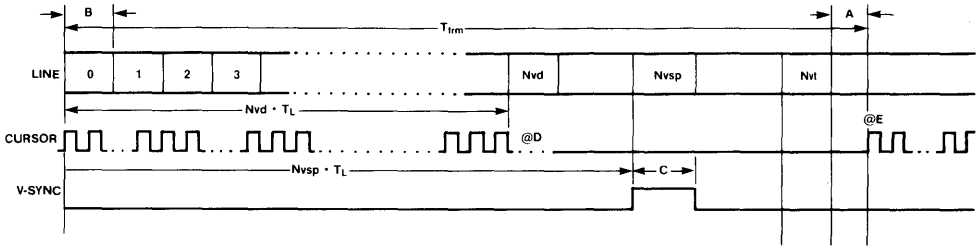
Total number of rasters in a line is even.

Interlace Sync & Video Mode



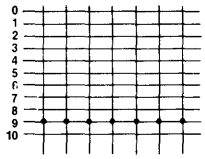
Total number of rasters in a line is odd.

Figure 8: Vertical Timing Chart

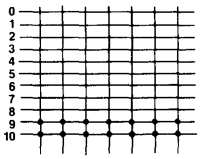


Note:
Nvd = Number of vertical displayed characters
Nvsp = Vertical sync position
Nvt = Number of vertical total characters
Tadj = Nadj · Tr = Fine adjustment period of frame
Tvsw = Nvsw · Tr = Vertical sync pulse width
T_{frm} = (Nvt + 1) · T_L + Tadj = Frame period
A = T_{adj}
B = T_L
@D = See Fig. 9a for the expansion of this region
@E = See Fig. 9b for the expansion of this region

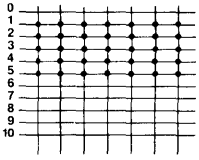
Figure 9: Cursor Control



Cursor Start Address = 9
Cursor End Address = 9



Cursor Start Address = 9
Cursor End Address = 10



Cursor Start Address = 1
Cursor End Address = 5

Figure 10:

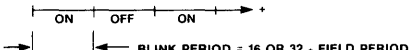
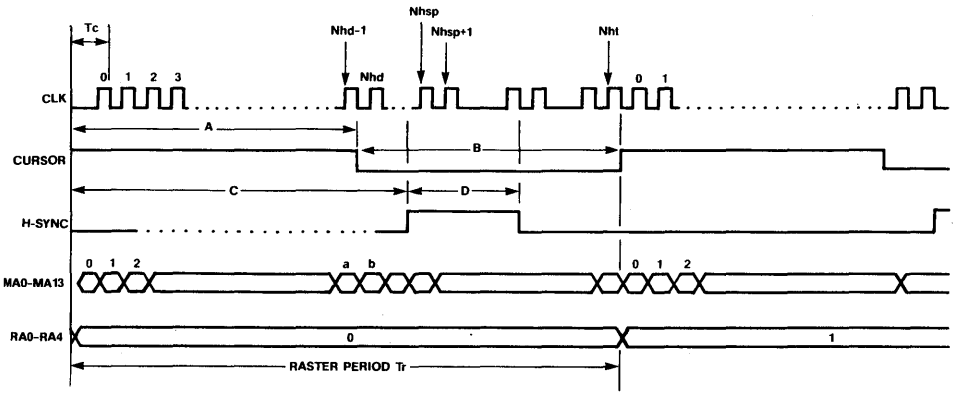
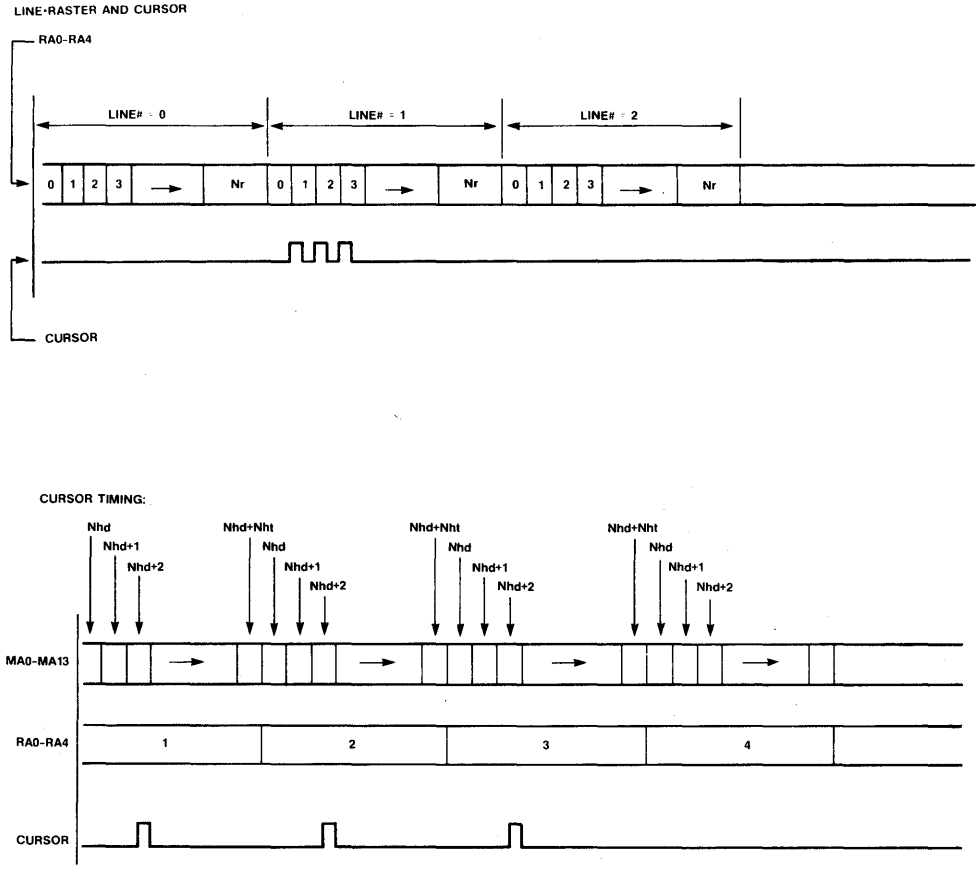


Figure 11: Horizontal Timing Chart



Notes:
Tc = Character clock period
A = Horizontal display period Nht - Tc
B = Horizontal Retrace Period
C = Nhsp * Tc
D = Nhsw * Tc
a = Nhd - 1
b = Nhd
Nhd = Number of Horizontal Displayed Characters
Nhsp = Horizontal Sync Position
Nht = Number of Horizontal Total Characters
Tr = Raster Period = (Nht + 1) * Tc

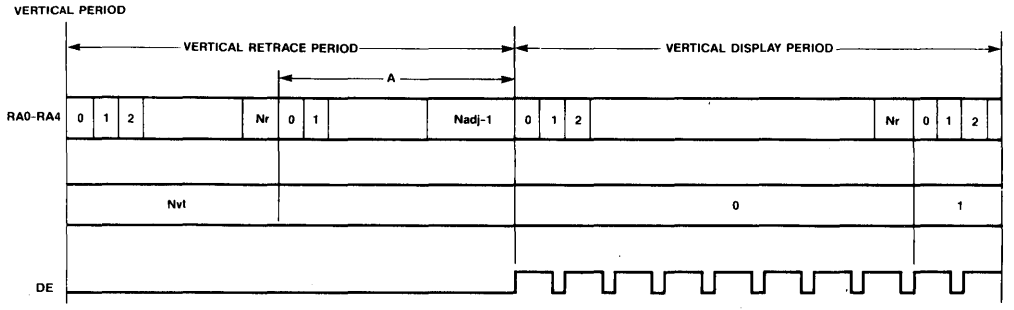
Figure 12a: Cursor Timing



Note:
The following are programmed in Cursor Display Mode:
Cursor Start: Raster Register = 1. Cursor End: Raster Register = 3
Cursor Register = Nhd + 2

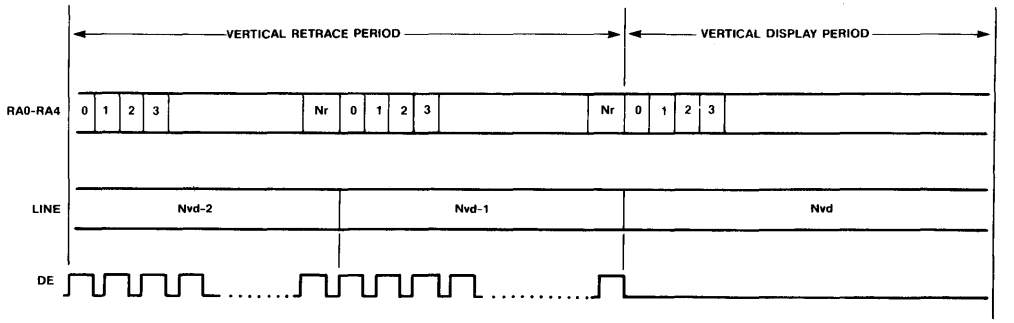
In Blink mode: When field period is 16 or 32 time period, it is changed into display or non-display mode.

Figure 12b: Fine Adjustment Period of Frame



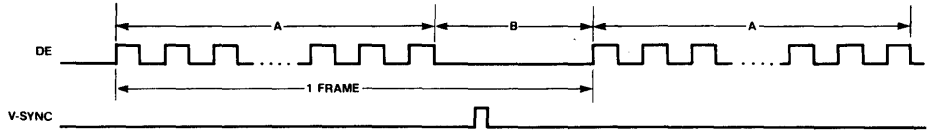
Note:
A = Fine adjustment period of Frame Period.
Tadj = Nadj * Tr

Figure 13a: Switching from Vertical Period to Vertical Retrace Period



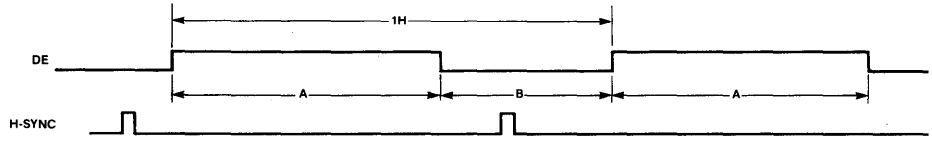
Notes:
A = Fine adjustment period of Frame Period.
Tadj = Nadj * Tr

Figure 13b: V-Sync Timing Chart



Notes:
A = Vertical Display Period
B = Vertical Retrace Period

Figure 13c: H-Sync Timing Chart



Notes:
A = Horizontal Display Period
B = Horizontal Retrace Period

Figure 14: Refresh Memory Addressing (MA0–MA13) Stage Chart

	HORIZONTAL DISPLAY (1 CHAR.)				HORIZONTAL RETRACE PERIOD (NON DISPLAY)		
0 [0 ↓ Nr]	0 ↓↓ 0	1 ↓↓ 1	→	Nhd-1 ↓↓ Nhd-1	Nhd ↓↓ Nhd	→	Nht ↓↓ Nht
1 [0 ↓ Nr]	Nhd ↓↓ Nhd	Nhd+1 ↓↓ Nhd+1	→	2•Nhd-1 ↓↓ 2•Nhd-1	2•Nhd ↓↓ 2•Nhd	→	Nhd+Nht ↓↓ Nhd+Nht
2 [0 ↓ Nr]	2•Nhd ↓↓ 2•Nhd	2•Nhd+1 ↓↓ 2•Nhd+1	→	3•Nhd-1 ↓↓ 3•Nhd-1	3•Nhd ↓↓ 3•Nhd	→	2Nhd+Nht ↓↓ 2Nhd+Nht
↓	↓	↓		↓	↓		↓
Nvd-1 [0 ↓ Nr]	(Nvd-1)Nhd ↓↓ (Nvd-1)Nhd	(Nvd-1)Nhd+1 ↓↓ (Nvd-1)Nhd+1	→	Nvd•Nhd-1 ↓↓ Nvd•Nhd-1	Nvd•Nhd ↓↓ Nvd•Nhd	→	(Nvd-1)Nhd+Nht ↓↓ (Nvd-1)Nhd+Nht
Nvd [0 ↓ Nr]	Nvd•Nhd ↓↓ Nvd•Nhd	Nvd•Nhd+1 ↓↓ Nvd•Nhd+1	→	(Nvd+1)Nhd-1 ↓↓ (Nvd+1)Nhd-1	(Nvd+1)Nhd ↓↓ (Nvd+1)Nhd	→	Nvd•Nhd+Nht ↓↓ Nvd•Nhd+Nht
Nvt [0 ↓ Nr]	Nvt•Nhd ↓↓ Nvt•Nhd	Nvt•Nhd+1 ↓↓ Nvt•Nhd+1	→	(Nvt+1)Nhd-1 ↓↓ (Nvt+1)Nhd-1	(Nvt+1)Nhd ↓↓ (Nvt+1)Nhd	→	Nvt•Nhd+Nht ↓↓ Nvt•Nhd+Nht
0 ↓ Nadj-1	(Nvt+1)Nhd ↓↓ (Nvt+1)Nhd	(Nvt+1)Nhd+1 ↓↓ (Nvt+1)Nhd+1	→	(Nvt+2)Nhd-1 ↓↓ (Nvt+2)Nhd-1	(Nvt+2)Nhd ↓↓ (Nvt+2)Nhd	→	(Nvt+2)Nhd+Nht ↓↓ (Nvt+2)Nhd+Nht

Notes:
0 — Nr; 0 — Nadj = Raster Address
0, 1, 2 — Nvd-1 = Line Number
0 — Nvd-1 = Vertical Display Period
Nvd — Nadj-1 = Vertical Display Period
Thick line square indicates valid refresh memory address (0 → Nvd•Nhd-1). Refer to Cursor Timing.

Table 11: DC Characteristics

V_{CC} = 5.0V ± 5%, V_{SS} = 0V, T_A = -20°C to 75°C

Item	Symbol	Test Condition	Min	Typ	Max	Unit
Input High Voltage	V_{IH}		2.0	—	V_{CC}	V
Input Low Voltage	V_{IL}		-0.3	—	0.8	V
Input Leakage Current	I_{IN}	V_{IN}[(a)] = 0V - 5.25V	-2.5	—	2.5	μA
3-State Input Current (Off-State)	I_{TSI}	V_{IN} = 0.4V - 2.4V V_{CC}[(b)] = 5.25V	-10	—	10	μA
Output High Voltage	V_{OH}	I_{LOAD}[(b)] = -205μA I_{LOAD}[(c)] = -100μA	2.4	—	—	V
Output Low Voltage	V_{OL}	I_{LOAD} = 1.6mA	—	—	0.4	V
Input Capacitance	C_{IN}	V_{IN} = 0V F = 1.0MHz, T_A = 25°C—	— —	— 10.0	12.5[(c)] pF	pF
Output Capacitance	C_{OUT}	V_{IN} = 0V F = 1.0MHz, T_A = 25°C	—	—	10.0	pF
Power Dissipation	P_D		—	600	1000	mW

Typical Condition: T_A = 25°C, V_{CC} = 5.0V

Note:
(a) = Except D0-D7
(b) = D0-D7
(c) = Other Inputs

Table 12: AC Characteristics

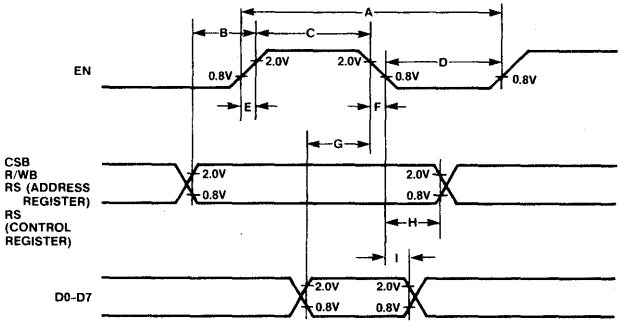
Item	Symbol	Test Condition	3.7 MHz			6 MHz			Unit
			Min	Typ	Max	Min	Typ	Max	
CRTC Timing									
Light Pen Strobe Pulse Width	PW_{LPH}		60	—	—	60	—	—	ns
Light Pen Strobe	T_{LPD1}		—	—	70	—	—	70	ns
Uncertain Time of Acceptance	T_{LPD2}		—	—	0	—	—	0	ns
Raster Address Delay Time	T_{RAD}		—	—	160	—	—	105	ns
Memory Address Delay Time	T_{MAD}		—	—	160	—	—	105	ns
DE Delay Time	T_{DTD}		—	—	250	—	—	165	ns
CURSOR Delay Time	T_{CDD}		—	—	250	—	—	165	ns
V-SYNC Delay Time	T_{VSD}		—	—	250	—	—	165	ns
Horizontal Sync Delay Time	T_{HSD}		—	—	200	—	—	132	ns
Rise and Fall Time for CLK Input	T_{CR}, T_{CF}		—	—	20	—	—	14	ns
Clock Low Pulse Width	PW_{CL}		130	—	—	86	—	—	ns
Clock High Pulse Width	PW_{CH}		130	—	—	86	—	—	ns
Clock Cycle Time	T_{CYC}		270	—	—	178	—	—	ns

Table 12: AC Characteristics (Continued)

Item	Symbol	Test Condition	3.7 MHz			6 MHz			Unit
			Min	Typ	Max	Min	Typ	Max	
MPU Write Timing									
Enable Cycle Time	T_{CYCE}		1.0	—	—	0.375	—	—	μs
Enable High Pulse Width	PW_{EH}		0.45	—	—	0.165	—	—	μs
Enable Low Pulse Width	PW_{EL}		0.40	—	—	0.158	—	—	μs
Enable Rise and Fall Time	T_{ER}, T_{EF}		—	—	25	—	—	15	ns
Address Setup Time	T_{AS}		140	—	—	30	—	—	ns
Data Setup Time	T_{DSW}		195	—	—	45	—	—	ns
Data Hold Time	T_H		10	—	—	10	—	—	ns
Address Hold Time	T_{AH}		10	—	—	10	—	—	ns
MPU Read Timings									
Enable Cycle Time	T_{CYCE}		1.0	—	—	0.375	—	—	μs
Enable High Pulse Width	PW_{EH}		0.45	—	—	0.165	—	—	μs
Enable Low Pulse Width	PW_{EL}		0.40	—	—	0.158	—	—	μs
Enable Rise and Fall Time	T_{ER}, T_{EF}		—	—	25	—	—	15	ns
Address Setup Time	T_{AS}		140	—	—	30	—	—	ns
Enable Data Delay	T_{DDR}		—	—	320	—	—	90	ns
Data Hold Time	T_H		10	—	—	10	—	—	ns
Address Hold Time	T_{AH}		10	—	—	10	—	—	ns
Data Access Time	T_{ACC}		—	—	460	—	—	120	ns

V_{CC} = 5V ± 5%, T_A = -20°C to 75°C

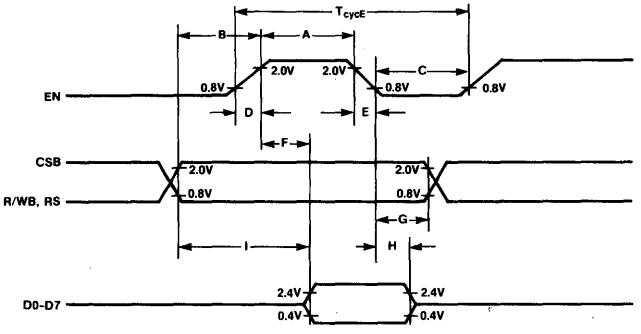
Figure 15: Write Timing Sequence



Notes:

A = T_{cycE}
B = T_{AS}
C = PW_{EH}
D = PW_{EL}
E = T_{Er}
F = T_{Ef}
G = T_{DSW}
H = T_{AH}
I = T_H

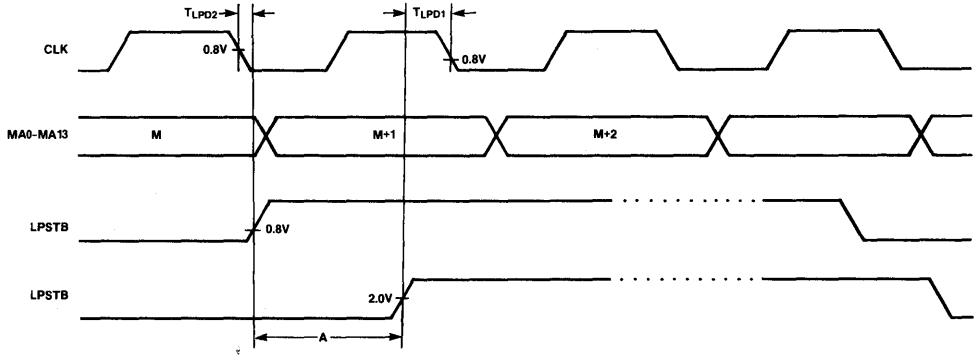
Figure 16: Read Sequence



Notes:

A = PW_{EH}	D = T_{Er}	G = T_{AH}
B = T_{AS}	E = T_{Ef}	H = T_H
C = PW_{EL}	F = T_{DDR}	I = T_{ACC}

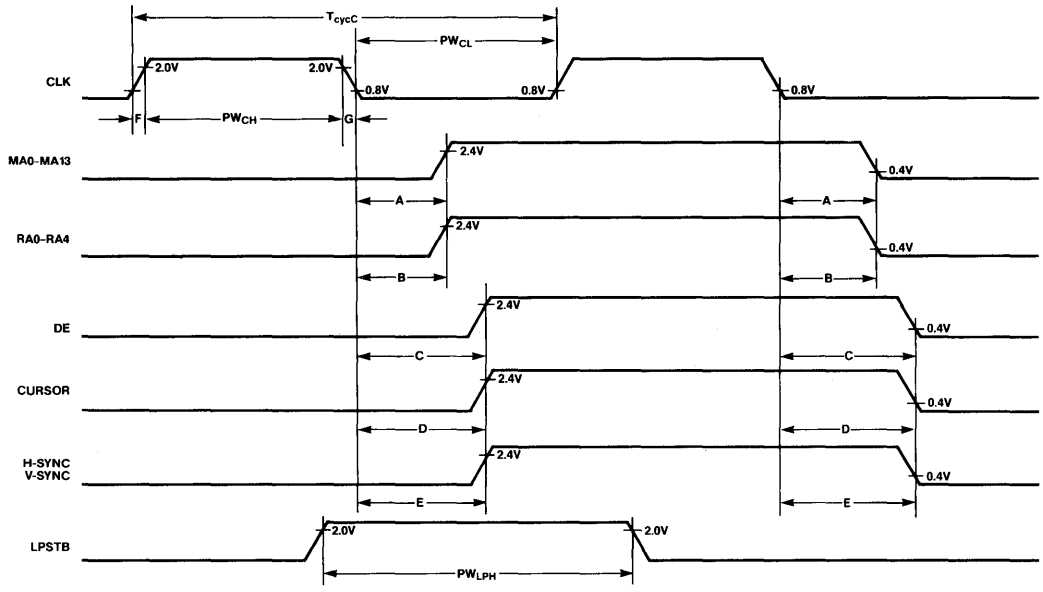
Figure 17: CLK, MA0-MA13, and LPSTB Timing



Note:

A — Sets Refresh Memory Address (M+2) into the light pen registers.

Figure 18: CRTC Timing Chart



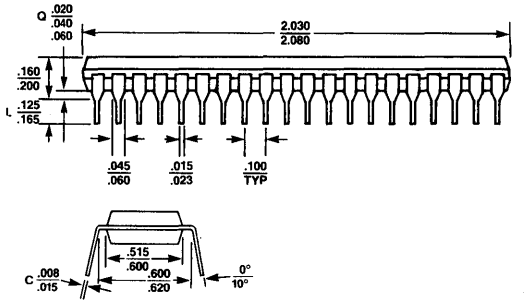
Notes:

A = T_{MAD}
B = T_{RAD}
C = T_{DTD}
D = T_{CDD}
E = T_{HSD}
F = T_{CR}
G = T_{CF}

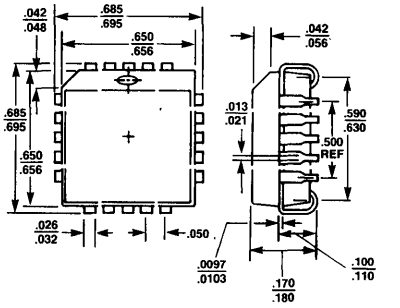
PACKAGE DIMENSIONS

Units: Inches

40-pin DIP



44-pin PLCC



ORDERING INFORMATION AND PRODUCT CODE

KS 68C45S X X X

SAMSUNG SEMICONDUCTOR

Part Number

Speed
-4 3.7MHz
-6 6MHz

Packaging
P — Plastic DIP
L — Plastic Leaded Chip Carrier (PLCC)

Temperature
C — Commercial (0°C to +70°C)
I — Industrial (-40°C to +85°C)

SAMSUNG products are designated by a Product Code. When ordering, please refer to products by their full code. For unusual, and/or specific packaging or processing requirements not covered by the standard product line, please contact the SAMSUNG MOS Product Group.

KS82C37A

PROGRAMMABLE DMA CONTROLLER

FEATURES/BENEFITS

- **Pin and functional compatibility with the industry standard 8237/8237A**
- **High Speed — 5MHz, 8MHz and 10MHz versions available**
- **Four independent maskable DMA channels with autoinitialize capability**
- **Independent polarity control for DREQ and DACK signals**
- **Address increment or decrement selection**
- **Cascadable to any number of channels**
- **Memory-to-memory transfer**
- **Fixed or rotating DMA request priority**
- **Low power CMOS implementation**
- **TTL input/output compatibility**
- **8080/85, 8086/88, 80186/286/386 compatible**

DESCRIPTION

The KS82C37A is a high performance, programmable Direct Memory Access (DMA) controller offering pin-for-pin functional compatibility with the industry standard 8237/8237A. It features four channels, each independently programmable, and is cascadable to any number of channels. Each channel can be programmed to autoinitialize following DMA termination.

In addition, the KS82C37A supports both memory-to-memory transfer capability and memory block initialization, as well as a programmable transfer mode.

The KS82C37A is manufactured using a proven CMOS technology to produce a powerful, reliable product. It is designed to improve system performance by allowing external devices to transfer data directly from the system memory. High speed and very low power consumption make it an attractive addition in portable systems or systems with low power standby modes.

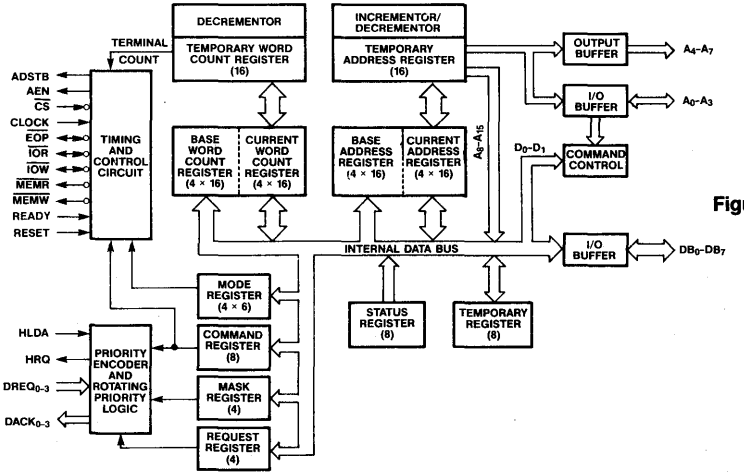


Figure 1: KS82C37A Block Diagram

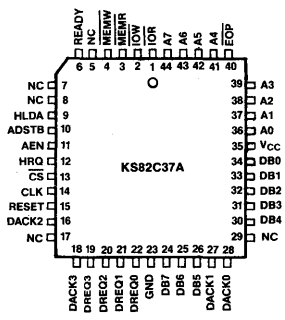


Figure 2: 44 Pin PLCC Configuration

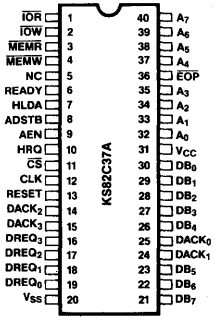


Figure 3: 40 Pin DIP

Table 1a: 40-Pin DIP Pin Assignment

Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name
1	$\overline{IOR}$	8	ADSTB	15	$DACK_3$	22	DB_6	29	DB_1	36	$\overline{EOP}$
2	$\overline{IOW}$	9	AEN	16	$DREQ_3$	23	DB_5	30	DB_0	37	A_4
3	$\overline{MEMR}$	10	HRQ	17	$DREQ_2$	24	$DACK_1$	31	V_{CC}	38	A_5
4	$\overline{MEMW}$	11	$\overline{CS}$	18	$DREQ_1$	25	$DACK_0$	32	A_0	39	A_6
5	N.C.	12	CLK	19	$DREQ_0$	26	DB_4	33	A_1	40	A_7
6	READY	13	RESET	20	V_{SS}	27	DB_3	34	A_2		
7	HLDA	14	$DACK_2$	21	DB_7	28	DB_2	35	A_3		

Table 1b: 44-Pin PLCC Pin Assignment

Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name
1	$\overline{IOR}$	9	HLDA	17	N.C.	25	DB_6	33	DB_1	41	A_4
2	$\overline{IOW}$	10	ADSTB	18	$DACK_3$	26	DB_5	24	DB_0	42	A_5
3	$\overline{MEMR}$	11	AEN	19	$DREQ_3$	27	$DACK_1$	35	V_{CC}	43	A_6
4	$\overline{MEMW}$	12	HRQ	20	$DREQ_2$	28	$DACK_0$	36	A_0	44	A_7
5	N.C.	13	$\overline{CS}$	21	$DREQ_1$	23	N.C.	27	A_1		
6	READY	14	CLK	22	$DREQ_0$	30	DB_4	38	A_2		
7	N.C.	15	RESET	23	V_{SS}	31	DB_3	39	A_3		
8	N.C.	16	DACK2	24	DB_7	32	DB_2	40	$\overline{EOP}$		

Table 2: Pin Descriptions

Symbol	Type	Name and Function
A_{0-3}	I/O	**Low Address Bus:** Bi-directional, 3-state signals. The 4 least significant address lines. *Idle Cycle (Inputs).* Addresses the KS82C37A control register to be loaded or read. *Active Cycle (Outputs).* Lower 4 bits of the transfer address.
A_{4-7}	O	**High Address Bus:** 3-state output signals. The 4 most significant address lines representing the upper 4 bits of the transfer address. Enabled during DMA service only.
ADSTB	O	**Address Strobe:** Active HIGH output signal to control latching of the upper address byte. Drives the strobe input of external transparent octal latches. During block operations, ADSTB is activated only if the upper address byte needs updating, eliminating S_1 states and accelerating operation.
AEN	O	**Address Enable:** Active HIGH output signal to enable the 8-bit latch containing the higher order address byte onto the system address bus. During DMA transfers, it can disable other system bus drivers.
CLK	I	**Clock Input:** Generates timing signals to control internal operations and data transfer rate. Input can be driven from DC to maximum frequency. CLK may be stopped in Active or Idle Cycle for standby operation.

Table 2: Pin Descriptions (Continued)

Symbol	Type	Name and Function
$\overline{CS}$	I	**Chip Select:** Active LOW input signal to select the KS82C37A as an I/O device (Idle Cycle) for CPU communication on the data bus.
$DACK_{0-3}$	O	**DMA Acknowledge:** Individual channel active LOW (RESET) or HIGH output lines. Informs a peripheral that the requested DMA transfer has been granted.
DB_{0-7}	I/O	**Data Bus:** Bi-directional 3-state data lines connected to the system data bus. *Idle Cycle.* During I/O Read (Program condition), outputs are enabled and contents of KS82C37A internal registers are read by the CPU. In I/O Write, outputs are disabled and data from the data bus are written into the registers. *Active Cycle.* The upper byte of the transfer address is output to the data bus during DMA I/O device-to-memory transfers. In memory-to-memory transfers, data is read into the KS82C37A Temporary Register from data bus inputs during the read-from-memory transfer, and written to the new memory location by data bus outputs during the write-to-memory transfer.
$DREQ_{0-3}$	I	**DMA Request:** Asynchronous DMA service request input lines from I/O devices. DMA service is requested by activation of the channel from a specific device. DREQ must be maintained until DACK (service acknowledge) is activated. *I/O Device Priority.* Order of service is programmable. Priority may be fixed (descending order from channel 0 or rotating (most recent channel served gets the lowest priority).
$\overline{EOP}$	I/O	**End of Process:** Active Low bi-directional 3-state signal. The KS82C37A terminates DMA service when $\overline{EOP}$ is activated. *Internal $\overline{EOP}$ (Output).* $\overline{EOP}$ is activated when the word count for any channel turns over from 0000(H) to FFFF(H) and a TC pulse is generated. In memory-to-memory transfer, service is terminated when TC for channel 1 occurs. *External $\overline{EOP}$ (Input).* An external $\overline{EOP}$ signal pulling $\overline{EOP}$ LOW terminates active DMA service. An $\overline{EOP}$ signal also resets the DMA request. If autoinitialize is enabled, the base registers are written to the current register of the channel. If the channel is not programmed for autoinitialize, the mask bit (Mask Register) and TC bit (Status Register) are set for the currently active channel. The mask bit is not changed if the channel is set for autoinitialize. Since $\overline{EOP}$ is driven by an *open drain transistor* on-chip, it should be maintained HIGH with a pull-up resistor in order to avoid erroneous $\overline{EOP}$ inputs.
HLDA	I	**Hold Acknowledge:** Active HIGH input signal from the CPU, following an HRQ. Notifies the KS82C73A that the CPU has released control of the system buses.
HRQ	O	**Hold Request:** Active HIGH output signal to the CPU. Requests control of the system buses. HRQ is issued following a request for DMA service (DREQ) from a peripheral, and is acknowledged by the HLDA signal.
$\overline{IOR}$	I/O	**$\overline{IOR}$ Read:** Active LOW bi-directional, 3-state signal. *Idle Cycle.* CPU input control signal for reading the Control Registers. *Active Cycle.* Output control signal to read data from a peripheral device during a DMA cycle.
$\overline{IOW}$	I/O	**$\overline{IOW}$ Write:** Active LOW bi-directional, 3-state signal. *Idle Cycle.* CPU input control signal for loading information into the KS82C37A. *Active Cycle.* Output control signal to load data to a peripheral device during a DMA cycle.

Table 2: Pin Descriptions (Continued)

Symbol	Type	Name and Function
$\overline{MEMR}$	O	**Memory Read:** Active LOW 3-state output signal. KS82C37A reads data from a selected memory address during a DMA read or memory-to-memory transfer.
$\overline{MEMW}$	O	**Memory Write:** Active LOW 3-state output signal. KS82C37A writes data to a selected memory address during a DMA write or memory-to-memory transfer.
READY	I	**Ready:** A LOW ready signal extends the memory read and write pulse widths from the KS82C37A to accommodate slow I/O peripherals or memories. Transition must not be made during the specified setup/hold time.
RESET	I	**Reset:** Active HIGH asynchronous input signal. Clears the Command, Status, Request and Temporary Register, the Mode Register Counter, and the First/Last Flip-Flop. The Mask Register is set to ignore DMA requests. The KS82C37 is in Idle Cycle following Reset.
V_{CC}	—	**Power:** 5V ± 10% DC supply.
V_{SS}	—	**Ground:** 0V

FUNCTIONAL DESCRIPTION

The KS82C37A DMA controller is a state-driven address and control signal generator designed to accelerate data transfer in systems moving data from an I/O device to memory, or a block memory to an I/O device. Data transfer is direct, bypassing storage in a temporary register.

The KS82C37A also mediates memory-to-memory block transfers and will move data from a single location to a memory block. Temporary storage of data is required, but the transfer rate is significantly faster than CPU processes. The device provides operating modes to carry out both single byte transfers and memory block transfers, allowing it to control data movement with software transparency. An operational flowchart of the KS82C37A is shown in Figure 3.

The organization of the KS82C37A is outlined in the block diagram. It is composed of three logic blocks, a series of internal registers and a counter selection. The logic blocks include the Timing and Control and Priority Encoder circuits.

The Timing Control block generates internal timing signals from the clock input and produces external control signals.

Command Control decodes incoming instructions from the CPU, and the Priority Encoder block regulates DMA channel priority.

The internal registers hold internal states and instruction from the CPU. Addresses and word counts are computed in the counter section.

OPERATIONAL DESCRIPTION

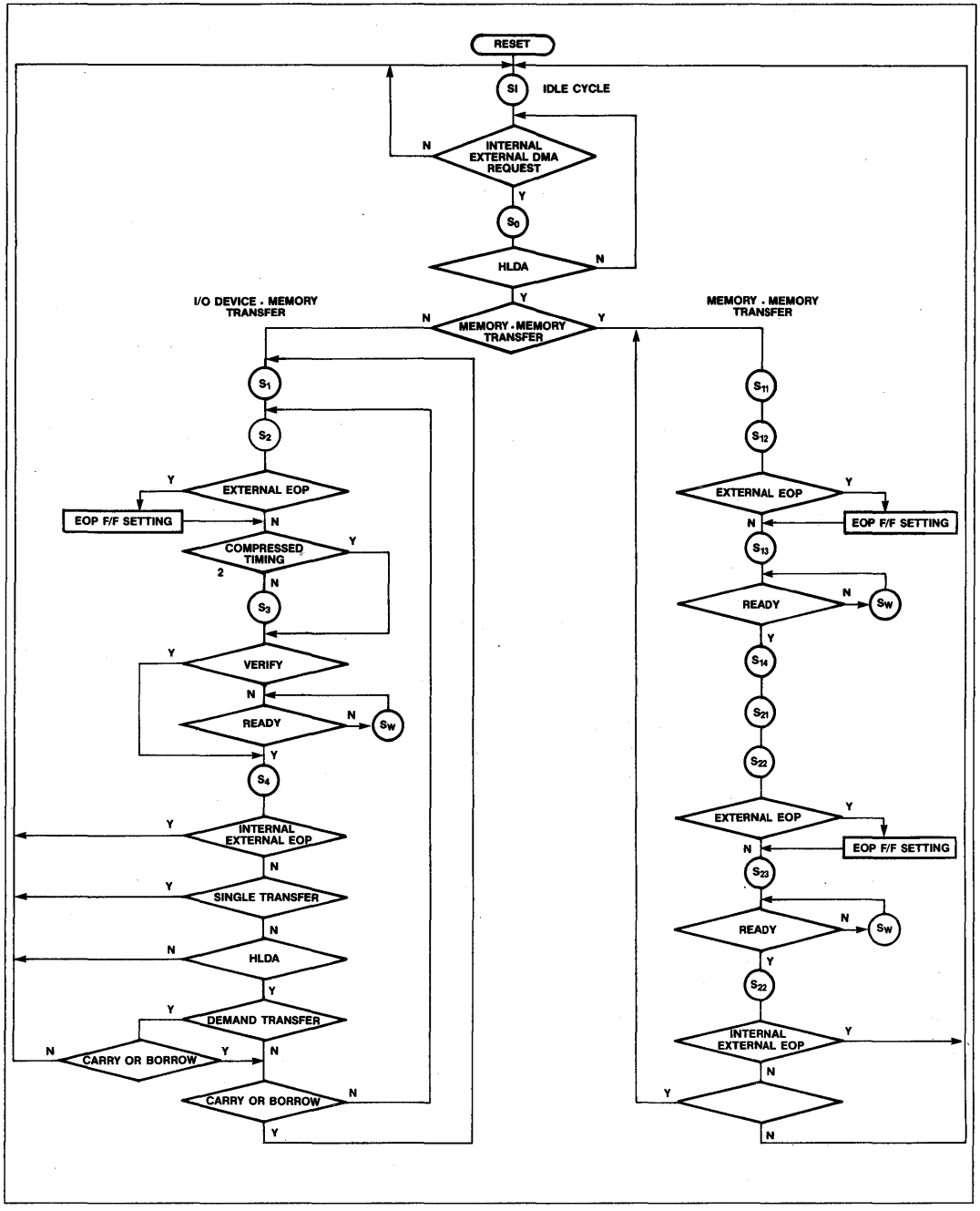
DMA Operation

In a system, the KS82C37A address and control outputs and data bus pins are usually connected in parallel with the system buses with an external latch required for the upper address byte. When inactive, the controller's outputs are in a high impedance state. When activated by a DMA request (and bus control has been relinquished by the host), the KS82C37A drives the buses and generates the control signals to perform the data transfer. The operation performed by activating one of the four DMA request inputs has previously been programmed into the controller via the Command Mode Address, and Word Count Registers.

For example, if a block of data is to be transferred from RAM to an I/O device, the starting address of the data is loaded into the KS82C37A current and Base Address Registers for a particular channel, and the length of the block is loaded into that channel's Word Count Register. The corresponding Mode Register is programmed for a memory-to-I/O operation (read transfer), and various options are selected by the Command Register and other Mode Register bits. The channel's mask bit is cleared to enable recognition of a DMA request (DREQ). The DREQ can be generated by a hardware signal or by a Software Command.

Once initiated, the block DMA transfer proceeds as the controller outputs the data address, simultaneous $\overline{MEMR}$ and $\overline{IOW}$ pulses, then selects an I/O device via the DMA acknowledge (DACK) outputs. The data byte flows directly from the RAM to the I/O device. After each byte

Figure 3: Operational Flowchart



is transferred, the address is automatically incremented (or decremented) and the Word Count is decremented. The operation is then repeated for the next byte. The controller stops transferring data when the Word Count Register underflows, or an external EOP is applied.

To better understand KS82C37A operation, consider the states generated by each clock cycle. The DMA controller operates in two major cycles, active and idle. After being programmed, the controller is normally idle until a DMA request occurs on an unmasked channel, or a software request is given. The KS82C37A then requests control of the system buses and enters the active cycle. The active cycle is composed of several internal states, depending on the options that have been selected and the type of operation that has been requested.

When performing I/O-to-memory or memory-to-I/O DMA the KS82C37A can enter seven distinct states, each composed of one full clock period. State 1 (S_1) is the idle state. It is entered when the KS82C37A has no valid DMA requests pending, at the end of a transfer sequence, or when a Reset or Master Clear occurs. While in S_1, the DMA controller is inactive, though it may be in the process of being programmed by the processor (Program Condition).

State 0 (S_0) is the first state of a DMA service. The KS82C37A has requested a hold but the processor has not yet returned an acknowledge. The KS82C37A may still be programmed until it has received HLDA from the CPU. An acknowledge from the CPU will signal that DMA transfers may begin. S_1, S_2, S_3, and S_4 are the working states of the DMA service. If more time is needed to complete a transfer than is available with normal timing, wait states (S_W) can be inserted prior to the execution of the S_4 cycle by use of the Ready line on the KS82C37A.

Note that the data is transferred directly from the I/O device to memory (or vice versa) with $\overline{IOR}$ and $\overline{MEMW}$ (or $\overline{MEMR}$ and $\overline{IOW}$) being active at the same time. The data is neither read into nor driven out of the KS82C37A in I/O-to-memory or memory-to-I/O transfers.

Table 3: Memory-to-Memory Transfer States

Transfer States	State Numbers	Notes
Read-from-Memory	S_{11}, S_{12} S_{13}, S_{14}	Memory-to-Memory transfers require 8 states per transfer. 4 states for the Read-from-Memory portion, and 4 Write-to-Memory states to complete the transfer.
Write-to-Memory	S_{21}, S_{22} S_{23}, S_{24}	

The KS82C37A can enter eight distinct states when performing memory-to-memory DMA, each composed of one full clock period. Four states are required for the read-from-memory step, and four for the write-to-memory operations. Data bytes in transit are stored in the Temporary register.

Idle Cycle

When none of the channels are requesting service, the KS82C37A enters the Idle cycle and performs S_1 states. In this cycle, the KS82C37A samples the DREQ lines on the falling edge of every clock cycle to determine if any channel is requesting a DMA service.

Note that DMA requests will be ignored in standby operation where the clock has been stopped. The device will respond to a $\overline{CS}$ (chip select), in case of an attempt by the microprocessor to write or read the internal registers of the KS82C37A. When $\overline{CS}$ is low and HLDA is low, the KS82C37A enters the Program Condition. The CPU can then establish, change or inspect the internal definition of the part by reading or writing the internal registers.

The KS82C37A may be programmed with the clock stopped, provided HLDA is low and at least one rising clock edge occurred after HLDA was driven low, so the controller is in an S_1 state. Address lines A_0 - A_3 are inputs to the device and select which registers are read or written. The $\overline{IOR}$ and $\overline{IOW}$ lines are used to select and time the read or write operations.

Due to the number and size of the internal registers, an internal flip-flop is used to generate an additional address bit. This bit is used to determine the upper or lower byte of the 16-bit Address and Word Count Registers. The flip-flop is reset by a Master Clear or Reset. Separate software commands can also set or reset this flip-flop.

Special software commands can be executed by the KS82C37A in the Program Condition. These commands are decoded as sets of addresses with $\overline{CS}$, $\overline{IOR}$, $\overline{IOW}$, and do not make use of the data bus. The commands include: Set and Clear First/Last Flip-Flop, Master Clear, Clear Mode Register Counter, and Clear Mask Register.

Active Cycle

When the KS82C37A is in the Idle cycle, and a software requests or an unmasked channel requests a DMA service, the device outputs an HRQ to the microprocessor and enters the Active cycle. It is in this cycle that the DMA service will take place, in one of the four modes described below:

Single Transfer Mode

In Single Transfer Mode, the device is programmed to make one transfer only. The Word Count is decremented and the address decremented or incremented following each transfer. When the Word Count rolls over from zero to FFFFH, a terminal count bit in the status register is set, an $\overline{EOP}$ pulse is generated, and the channel autoinitializes if this option has been selected. If not programmed to Autoinitialize, the mask bit is set, along with the TC bit and an $\overline{EOP}$ pulse is generated.

DREQ must be held active until DACK becomes active. If DREQ is held active throughout the single transfer, HRQ goes inactive and releases the bus to the system. It again goes active and, upon receipt of a new HLDA, another single transfer is performed, unless a higher priority channel takes over. In 8080A, 8085A, or 8088/86 systems, this ensures one full machine cycle execution between DMA transfers. Details of the timing between the KS82C37A and other bus control protocols depends upon the characteristics of the microprocessor involved.

Block Transfer Mode

In Block Transfer Mode, the KS82C37A is activated by DREQ or software request and continues making data transfers during the service until a TC, caused by word count going to FFFFH, or an external End of Process ($\overline{EOP}$) is encountered. DREQ need only be held active until DACK becomes active. Again, Autoinitialization occurs at the end of the service if the channel has been programmed for that option.

Demand Transfer Mode

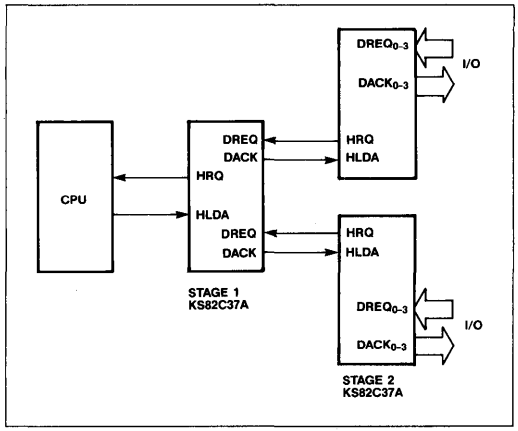
In Demand Transfer Mode the KS82C37A continues making transfers until a TC or an external $\overline{EOP}$ is encountered, or until DREQ goes inactive. Thus, transfers continue until the I/O device has exhausted its data capacity. When the I/O device has caught up, DMA service is reestablished by means of a DREQ. In the interim between services when the microprocessor is allowed to operate, the intermediate values of address and word count are stored in the KS82C37A Current Address and Current Word Count registers.

Higher priority channels may intervene in the demand process, once DREQ has gone inactive. Only an $\overline{EOP}$ can cause an Autoinitialization at the end of the service. The $\overline{EOP}$ is generated either by TC or by an external signal.

Cascade Mode

This mode is used to cascade more than one KS82C37A for simple system expansion. The HRQ and HLDA signals from additional KS82C37A devices are connected

Figure 4: Cascaded KS82C37As



to the DREQ and DACK signals respectively of a channel for the initial KS82C37A. This allows the DMA requests of the additional devices to propagate through the priority network circuitry of the preceding device. The priority chain is preserved and the new device must wait for its turn to acknowledge requests. Since the cascade channel of the initial KS82C37A is used only for setting the priority of additional devices, it does not output an address or control signals of its own. These could conflict with the outputs of the active channel in the extra devices.

The KS82C37A will respond to DREQ and generate DACK but all other outputs except HRQ will be disabled. An external $\overline{EOP}$ will be ignored by the initial device, but will have the usual effect on the added device.

Figure 4 shows two additional devices cascaded with an initial device and using two of the initial device's channels. This forms a two-level DMA system. More KS82C37As could be added at the second level by using the remaining channels of the first level. Additional devices can also be added by cascading into the channels of the second level devices, forming a third level.

When programming cascaded controllers, start with the first level device (the one closet to the microprocessor). After Reset, the DACK outputs are programmed to be active low and are held in the high state. If they are used to drive HLDA directly, the second level device(s) cannot be programmed until DACK polarity is selected as active high on the initial device. In addition, the initial device's mask bits funciton normally on cascaded channels, so they may be used to inhibit second-level services.

Transfer Types

Each of the three active transfer modes can perform three different types of transfers. These are Read, Write and Verify. Write transfers move data from an I/O device to the memory by activating $\overline{MEMW}$ and $\overline{IOR}$. Read transfers move data from memory to an I/O device by activating $\overline{MEMR}$ and $\overline{IOW}$ (refer to Table 4).

Verify transfers are pseudo-transfers. The KS82C37A operates like Read or Write transfers, generating addresses and responding to $\overline{EOP}$, etc., however the memory and I/O control lines all remain inactive. Verify mode is not allowed for memory-to-memory operation. Note that Ready is ignored during verify transfers.

Autoinitialize

By programming a bit in the mode register, a channel may be set up as an Autoinitialize channel. During Autoinitialization, the original values of the Current Address and Current Word Count Registers are automatically restored from the Base Address and Base Word Count Registers of that channel following $\overline{EOP}$. The Base Registers are loaded at the same time as the Current Registers by the microprocessor and remain unchanged throughout the DMA service. The mask bit is not set when the channel is in Autoinitialize. Following Autoinitialization, the channel is ready to perform another DMA service, without CPU intervention, as soon as a valid DREQ is detected, or software request is made.

Memory-to-Memory

The KS82C37A incorporates a memory-to-memory transfer feature, to perform block moves of data from one memory address space to another with minimum of program effort and time. Programming bit 0 in the Command Register selects channels 0 and 1 to operate as memory-to-memory transfer channels.

The transfer is initiated by setting the software or hardware DREQ for channel 0. The KS82C37A requests a DMA service in the normal manner. When HLDA goes high, the device, using four-state transfers in Block Transfer mode, reads data from the memory. The channel 0 Current Address Register is the source for the address used and is decremented or incremented in the normal manner. The data byte read from the memory is stored in the KS82C37A internal Temporary Register. Another four-state transfer moves the data to memory using the address in the channel 1 Current Address Register. The Current Address is incremented or decremented in the normal manner, and the channel 1 Current Word Count is decremented.

When the word count of channel 1 goes to FFFFH, a TC is generated, causing an $\overline{EOP}$ output which terminates the service. When Channel 0 word count decrements to FFFFH the channel 0 TC bit in the status register is not set nor is an $\overline{EOP}$ generated in this mode. However, channel 0 is Autoinitialized, if that option has been selected.

Table 4: I/O-Memory Transfer States*

Operational State	Description	Notes
S_1	AEN High Low Order Bits: A_0 - A_7 High Order Bits: DB_0 - DB_7 ADSTB High DACK Active	S_1 state is omitted if there is no change in the 8 high order bit transfer address during demand and block mode transfers.
S_2	$\overline{IOR}$ Low or $\overline{MEMR}$ goes Low	S_2 State (and S_3) are I/O or memory I/O timing control states.
S_3	$\overline{IOW}$ Low or $\overline{MEMW}$ goes Low	S_3 is omitted when compressed timing is used.
S_4	$\overline{IOR}$ High $\overline{IOW}$ High $\overline{MEMR}$ High $\overline{MEMW}$ High Word Count Register Decremented by 1 Address Register Incremented (or Decremented) by 1	S_4 state completes the DMA transfer of one word.

* In I/O memory transfers, data is transferred directly without being handled by the KS82C37A.

If full Autoinitialization for a memory-to-memory operation is desired, the channel 0 and channel 1 word counts must be set to the same value before the transfer begins. Otherwise, should channel 0 underflow before channel 1, it Autoinitializes and sets the data source address back to the beginning of the block. Should the channel 1 word count underflow before channel 0, the memory-to-memory DMA service terminates, and channel 1 Autoinitializes but not channel 0.

In memory-to-memory mode, Channel 0 may be programmed to retain the same address for all transfers, allowing a single byte to be written to an entire block of memory. This channel 0 Address Hold feature is selected by bit 1 in the command register.

The KS82C37A responds to external $\overline{EOP}$ signals during memory-to-memory transfers, but only relinquishes the system buses after the transfer is complete (i.e. after an S_{24} state). Data comparators in block search schemes may use this input to terminate the service when a match is found. The timing of memory-to-memory transfers is found in Figure 14b. Memory-to-memory operations can be detected as an active AEN with no DACK outputs.

Priority

The KS82C37A has two types of priority encoding available as software selectable options. The first is Fixed Priority which fixes the channels in priority order based upon the descending value of their numbers. The channel with the lowest priority is 3 followed by 2, 1 and the highest priority channel, 0. After a channel has been recognized for service, the other channels are prevented from interfering with the service until it is completed.

The second scheme is Rotating Priority. The last channel to get service becomes the lowest priority channel with the others rotated accordingly. The next lower channel from the channel serviced has highest priority on the following request: Priority rotates every time control of the system buses is returned to the CPU.

With Rotating Priority in a single chip DMA system, any device requesting service is guaranteed to be recognized after no more than three higher priority services have occurred. Thus any one channel is prevented from monopolizing the system.

Note that regardless of which priority scheme is chosen, priority is evaluated every time a HLDA is returned to the KS82C37A.

Compressed Timing

In order to achieve even greater throughput where system characteristics permit, the KS82C37A can compress the transfer time to two clock cycles. From Figure 3, it can be seen that state S_3 is used to extend the access time of the read pulse. By removing state S_3, the read pulse width is made equal to the write pulse width and a transfer consists only of state S_2 to change the address and state S_4 to perform the read/write. S_1 states will still occur when A_8 - A_{15} need updating (see Address Generation). Timing for compressed transfers is found in Figure 3. $\overline{EOP}$ will be output in S_2 if compressed timing is selected. Compressed timing is not allowed for memory-to-memory transfers.

Table 5: Priority Decision Modes

Priority Mode		Fixed	Rotating			
Service Terminated Channel		—	CH_0	CH_1	CH_2	CH_3
Order of Priority or next DMA	Highest	CH_0	CH_1	CH_2	CH_3	CH_0
		CH_1	CH_2	CH_3	CH_0	CH_1
		CH_2	CH_3	CH_0	CH_1	CH_2
	Lowest	CH_3	CH_0	CH_1	CH_2	CH_3

Address Generation

In order to reduce the pin count, the KS82C37A multiplexes the eight higher order address bits on the data lines. State S_1 is used to output the higher order address bits to an external latch from which they may be placed on the address bus. The falling edge of Address Strobe (ADSTB) is used to load these bits from the data lines to the latch. Address Enable (AEN) is used to enable the bits onto the address bus through a three-state enable. Lower order address bits are output by the KS82C37A directly. Lines A_0 - A_7 should be connected to the address bus. The timing diagram of Figure 3 shows the time relationships between CLK, AEN, ADSTB, DB_0 - DB_7 and A_0 - A_7.

During Block and Demand Transfer mode service, which include multiple transfers, the addresses generated will be sequential. For many transfers the data held in the external address latch will remain the same. This data need only change when a carry or borrow from A_7 to A_8 takes place in the normal sequence of addresses. To save time and speed transfers, the KS82C37A executes the S_1 states only when updating of A_8 - A_{15} in the latch is necessary. This means for long services, S_1 states and ADSTB may occur only once every 256 transfers, a saving of 255 clock cycles for each 256 transfers.

External EOP Operation

The $\overline{EOP}$ pin is bidirectional and open drain, and can be driven by external signals to terminate DMA operation. It is important to note that the KS82C37A will not accept external $\overline{EOP}$ signals when it is in an S_I (Idle) state. The controller must be active to latch external $\overline{EOP}$. Once

latched, the external $\overline{EOP}$ will be acted upon during the next S_2 state, unless the KS82C37A enters an idle state first. In the latter case, the latched $\overline{EOP}$ is cleared. External $\overline{EOP}$ pulses that occur between active DMA transfers in demand mode are not recognized, since the KS82C37A is in an S_1 state.

INTERNAL REGISTERS

The KS82C37A contains 27 registers that are used internally for control and temporary data storage. These registers are listed in Table 6 below, and described in the subsections following.

Base Address and Base Word Count Registers

Each of the four (4) channels has a pair of Base Address and Base Word Count Registers. These 16-bit registers store the original value of their associated current registers. During Autoinitialize these values are used to restore the current registers to their original values.

The base registers are written simultaneously with their corresponding current register (in 8-bit bytes) by the microprocessor when in the Program Condition. These registers cannot be read by the microprocessor.

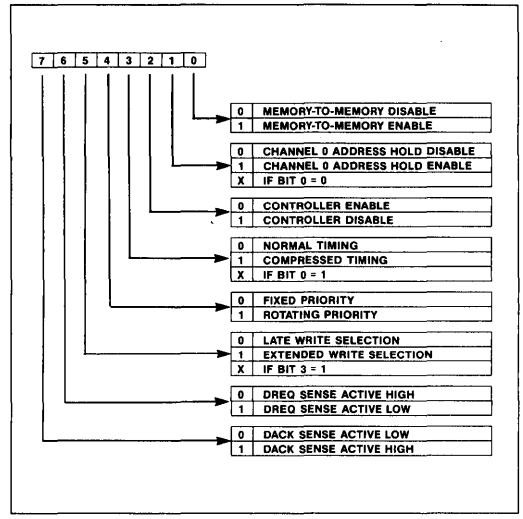
Table 6: Internal Registers

Name	Number	Size
Base Address Registers	4	16-Bit
Base Word Count Registers	4	16-Bit
Command Register	1	8-Bit
Current Address Registers	4	16-Bit
Current Word Count Registers	4	16-Bit
Mask Register	1	4-Bit
Mode Registers	4	6-Bit
Request Register	1	4-Bit
Status Register	1	8-Bit
Temporary Address Register	1	16-Bit
Temporary Register	1	8-Bit
Temporary Word Count Register	1	16-Bit

Command Register

The operation of the KS82C37A is controlled by the 8-bit Command Register. It is programmed by the microprocessor and is cleared by a Reset or a Master Clear instruction. Figure 5 lists the function of the command bits, while Table 7 contains the Read and Write addresses.

Figure 5: Command Register



Current Address Register

Each of the channels has a 16-bit Current Address register. This register holds the value of the address used during DMA transfers. The address is automatically incremented or decremented after each transfer, with the values of the address stored in the Current Address register during the transfer.

This register is written or read by the microprocessor in successive 8-bit bytes. It may also be reinitialized (by an Autoinitialize) back to its original value, where an Autoinitialize takes place only after an $\overline{EOP}$.

In memory-to-memory mode, the channel 0 current address register can be prevented from incrementing or decrementing by setting the address hold bit in the command register.

Current Word Register

Each of the channels also has a 16-bit Current Word Count register which is used to determine the number of transfers to be performed. The actual number of transfers is one more than the number programmed in the Current Word Count register (i.e. programming a count of 100 will result in 101 transfers). The word count is decremented after each transfer, and when the value in the register goes from zero to FFFFH, a terminal count (TC) is generated.

This register is loaded or read in successive 8-bit bytes by the microprocessor in the Program Condition.

Following the end of a DMA service it may also be reinitialized by an Autoinitialization back to its original value. Autoinitialization can occur only after an $\overline{EOP}$ or TC. If not Autoinitialized, this register will have a count of FFFFH after TC.

Mask Register

Each of the channels has associated with it one mask bit in the 4-bit Mask register which can be set to disable an incoming DREQ. Each mask bit is set when its associated channel produces an $\overline{EOP}$ if the channel is not programmed to Autoinitialize. Each Mask register bit may also be set or cleared separately or simultaneously under software control.

The entire register is also set by a Reset or Master Clear. This disables all hardware DMA requests until a clear Mask register instruction allows them to occur. The instruction to separately set or clear the mask bits is similar in form to that used with the Request register. Refer to the Figure 6 and Table 7 for details.

When reading the mask register, bits 4-7 will always read as logical ones, and bits 0-3 will display the mask bits of channel 0-3, respectively. The 4 bits of the mask register may be cleared simultaneously by using the Clear Mask Register command (see software commands section).

Figure 6: Mask Register

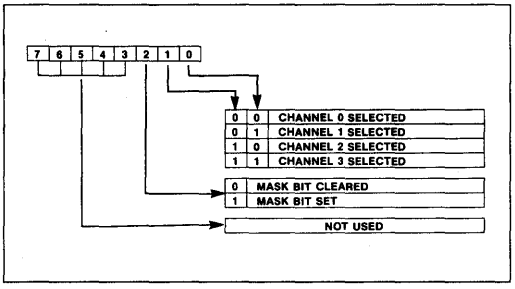
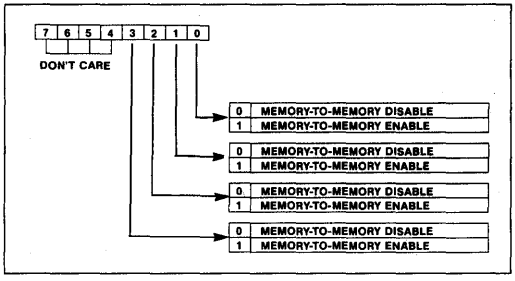


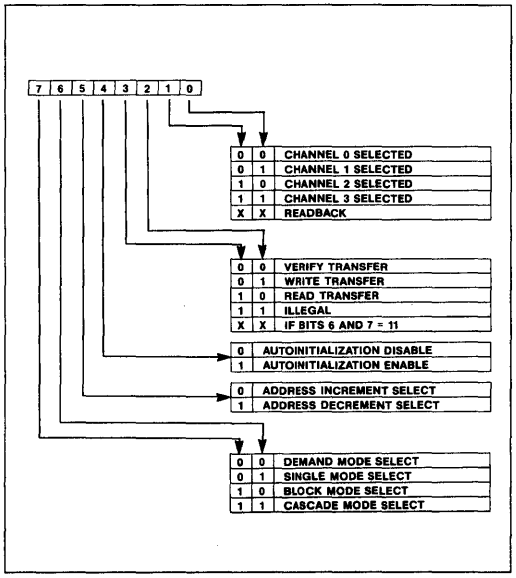
Figure 7: All Four Size Bits of the Mask Register May Also Be Written with a Simple Command



Mode Register

Each of the channels has a 6-bit mode register associated with it. When this register is being written to by the microprocessor in the Program Condition, bits 0 and 1 determine which channel Mode register is to be written. When the processor reads a mode register, bits 0 and 1 are both ones. See Figure 8 and Table 7 for mode register functions and addresses.

Figure 8: Mode Register

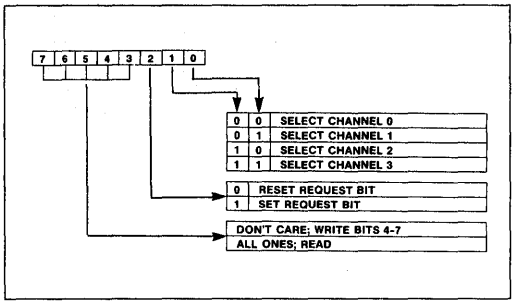


Request Register

The KS82C37A responds to requests for DMA service initiated by the software and by a DREQ. Each channel has a non-maskable request bit associated with it in the 4-bit Request Register. These are subject to prioritization by the priority Encoder network with each bit set or reset separately under software control. To set or reset a bit, the software loads the proper form of the data word. The entire register is cleared by a Reset. See Table 7 for register address coding, and Figure 9 for request register format.

A software request for DMA operation can be made in block or single modes. For memory-to-memory transfers, the software request for channel 0 should be set. When reading the request register, bits 4-7 will always read as ones, and bits 0-3 will display the request bits of channels 0-3 respectively.

Figure 9: Request Register



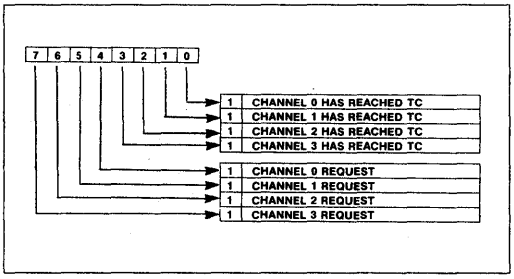
Status Register

The KS82C37A Status register can be read by the microprocessor. It contains information about which channels have reached a terminal count and which channels have pending DMA requests.

Bits 0-3 are set every time a TC is reached by that channel or an external $\overline{EOP}$ is applied. These bits are cleared upon Reset, Master Clear, and on each Status Read.

Bits 4-7 are set whenever their corresponding channel is requesting service, regardless of the mask bit state. If the mask bits are set, software can poll the status register to determine which channels have DREQs, and selectively clear a mask bit, thus allowing user defined service priority. Status bits 4-7 are updated while the clock is high, and latched on the falling edge. Status Bits 4-7 are cleared upon Reset or Master Clear.

Figure 10: Status Register



Temporary Register

The Temporary Register is used to hold data during memory-to-memory transfers. When the transfers are completed, the last word moved can be read by the microprocessor.

Note that the Temporary Register always contains the last byte transferred in the previous memory-to-memory operation, unless cleared by a Reset or Master Clear.

Figure 11: Definition of Register Codes

Register	Operation	SIGNALS						
		$\overline{CS}$	$\overline{IOR}$	$\overline{IOW}$	A_3	A_2	A_1	A_0
Command	Write	0	1	0	1	0	0	0
Mode	Write	0	1	0	1	0	1	1
Request	Write	0	1	0	1	0	0	1
Mask	Set/Reset	0	1	0	1	0	1	0
Mask	Write	0	1	0	1	1	1	1
Temporary	Read	0	0	1	1	1	0	1
Status	Read	0	0	1	1	0	0	0

PROGRAMMING

The KS82C37A accepts programming from the host processor any time that HLDA is inactive, and at least one rising clock edge has occurred after HLDA has gone low. It is necessary for the host processor to ensure that programming and HLDA are mutually exclusive.

Note that a problem can occur if a DMA request occurs on an unmasked channel while the KS82C37A is being programmed. For example: Where the CPU is starting to re-program the two byte address register of channel 1 when channel 1 receives a DMA request: If the KS82C37A is enabled (bit 2 in the Command register is set to 0), and channel 1 is unmasked, then a DMA service will occur after only one byte of the Address register has been reprogrammed. This condition can be avoided by disabling the controller (bit 2 in the Command register is set to 1) or masking the channel before programming any of its registers. Once the programming is complete, the controller can be enabled or the channel unmasked.

Software Commands

There are special software commands which can be executed by reading or writing to the KS82C37A. These commands do not depend on the specific data pattern on the data bus, but are activated by the I/O operation itself.

The KS82C37A Software Commands are summarized below:

Clear First/Last Flip-Flop

This command is executed prior to writing or reading new Address or Word Count information to the KS82C37A. This initializes the flip-flop to a known state so that subsequent accesses to register contents by the micro processor will address upper and lower bytes in the correct sequence.

Table 7: Software Command Codes and Register Codes

Operation	A_3	A_2	A_1	A_0	$\overline{IOR}$	$\overline{IOW}$
Read Status Register	1	0	0	0	0	1
Write Command Register	1	0	0	0	1	0
Read Request Register	1	0	0	1	0	1
Write Request Register	1	0	0	1	1	0
Read Command Register	1	0	1	0	0	1
Write Single Bit Mask	1	0	1	0	1	0
Read Mode Register	1	0	1	1	0	1
Write Mode Register	1	0	1	1	1	0
Set Byte Pointer F/F	1	1	0	0	0	1
CLR Byte Pointer F/F	1	1	0	0	1	0
Read Temporary Register	1	1	0	1	0	1
Master Clear	1	1	0	1	1	0
CLR Mode Register Counter	1	1	1	0	0	1
CLR Mask Register	1	1	1	0	1	0
Read All Mask Bits	1	1	1	1	0	1
Write All Mask Bits	1	1	1	1	1	0

Set First/Last Flip-Flop

This command will set the flip-flop to first select the high byte first on read and write operations to Address and Word Count Registers.

Master Clear

This software instruction has the same effect as the hardware Reset. The Command, Status, Request, and Temporary Registers, and Internal First/Last Flip-Flop and Mode Register counter are cleared and the Mask Register is set. The device then enters the Idle cycle.

Clear Mode Register

This command clears the mask bits of all four channels, enabling them to accept DMA requests.

Clear Mode Register Counter

Since only one address location is available for reading Mode Registers, an internal two-bit counter is included to select Mode Registers during read operations.

To read the Mode Registers, first execute the Clear Mode Register Counter Command, then do consecutive reads until the desired channel is read. Read order is channel 0 first, channel 3 last. The lower two bits on all Mode Registers will read as ones.

APPLICATIONS

Figure 12 shows an application for a DMA system utilizing the KS82C37A DMA controller and an 80C88 microprocessor. The KS82C37A DMA controller is used here to improve system performance by allowing an I/O device to transfer data directly to or from the system memory.

Components

The system clock is generated by the KS82C84A clock driver and is inverted to meet the clock high and low times required by the KS82C37A DMA controller. The four OR gates are used to support an 80C88 microprocessor in minimum mode by producing the control signals used by the processor to access memory or I/O. A decoder is used to generate the chip select for the DMA controller and memory.

Since the most significant bits of the address are output on the address/data bus, an octal latch is used to demultiplex the address. Hold Acknowledge (HLDA) and Address Enable (AEN) are ORed together to insure that the DMA controller does not encounter bus contention with the microprocessor.

Operation

A DMA request (DREQ) is generated by the I/O device. After receiving the DMA request, the DMA controller issues a Hold Request (HRQ) to the microprocessor. The system buses are not released to the DMA controller until a Hold Acknowledge signal is returned to the DMA controller from the 80C88 processor. After the Hold Acknowledge has been received, addresses and control signals are generated by the DMA controller to accomplish the DMA transfers. Data is transferred directly from the I/O device to memory (or vice versa) with $\overline{IOR}$ and $\overline{MEMW}$ (or $\overline{MEMR}$ and $\overline{IOW}$) being active. Recall that data is not read into or driven out of the DMA controller in I/O-to-memory or memory-to-I/O data transfers.

Table 8: Word Count and Address Register Command Codes

Channel	Register	Operation	SIGNALS							Internal Flip-Flop	Data Bus DB_0-DB_7
			$\overline{CS}$	$\overline{IOR}$	$\overline{IOW}$	A_3	A_2	A_1	A_0		
0	Base and Current Address	Write	0	1	0	0	0	0	0	0	A_0 - A_7
			0	1	0	0	0	0	0	1	A_8 - A_{15}
	Current Address	Read	0	0	1	0	0	0	0	0	A_0 - A_7
			0	0	1	0	0	0	0	1	A_8 - A_{15}
	Base and Current Word Count	Write	0	1	0	0	0	0	1	0	W_0 - W_7
			0	1	0	0	0	0	1	1	W_8 - W_{15}
	Current Word Count	Read	0	0	1	0	0	0	1	0	W_0 - W_7
			0	0	1	0	0	0	1	1	W_8 - W_{15}
1	Base and Current Address	Write	0	1	0	0	0	1	0	0	A_0 - A_7
			0	1	0	0	0	1	0	1	A_8 - A_{15}
	Current Address	Read	0	0	1	0	0	1	0	0	A_0 - A_7
			0	0	1	0	0	1	0	1	A_8 - A_{15}
	Base and Current Word Count	Write	0	1	0	0	0	1	1	0	W_0 - W_7
			0	1	0	0	0	1	1	1	W_8 - W_{15}
	Current Word Count	Read	0	0	1	0	0	1	1	0	W_0 - W_7
			0	0	1	0	0	1	1	1	W_8 - W_{15}
2	Base and Current Address	Write	0	1	0	0	1	0	0	0	A_0 - A_7
			0	1	0	0	1	0	0	1	A_8 - A_{15}
	Current Address	Read	0	0	1	0	1	0	0	0	A_0 - A_7
			0	0	1	0	1	0	0	1	A_8 - A_{15}
	Base and Current Word Count	Write	0	1	0	0	1	0	1	0	W_0 - W_7
			0	1	0	0	1	0	1	1	W_8 - W_{15}
	Current Word Count	Read	0	0	1	0	1	0	1	0	W_0 - W_7
			0	0	1	0	1	0	1	1	W_8 - W_{15}
3	Base and Current Address	Write	0	1	0	0	1	1	0	0	A_0 - A_7
			0	1	0	0	1	1	0	1	A_8 - A_{15}
	Current Address	Read	0	0	1	0	1	1	0	0	A_0 - A_7
			0	0	1	0	1	1	0	1	A_8 - A_{15}
	Base and Current Word Count	Write	0	1	0	0	1	1	1	0	W_0 - W_7
			0	1	0	0	1	1	1	1	W_8 - W_{15}
	Current Word Count	Read	0	0	1	0	1	1	1	0	W_0 - W_7
			0	0	1	0	1	1	1	1	W_8 - W_{15}

Figure 12: Application for DMA System

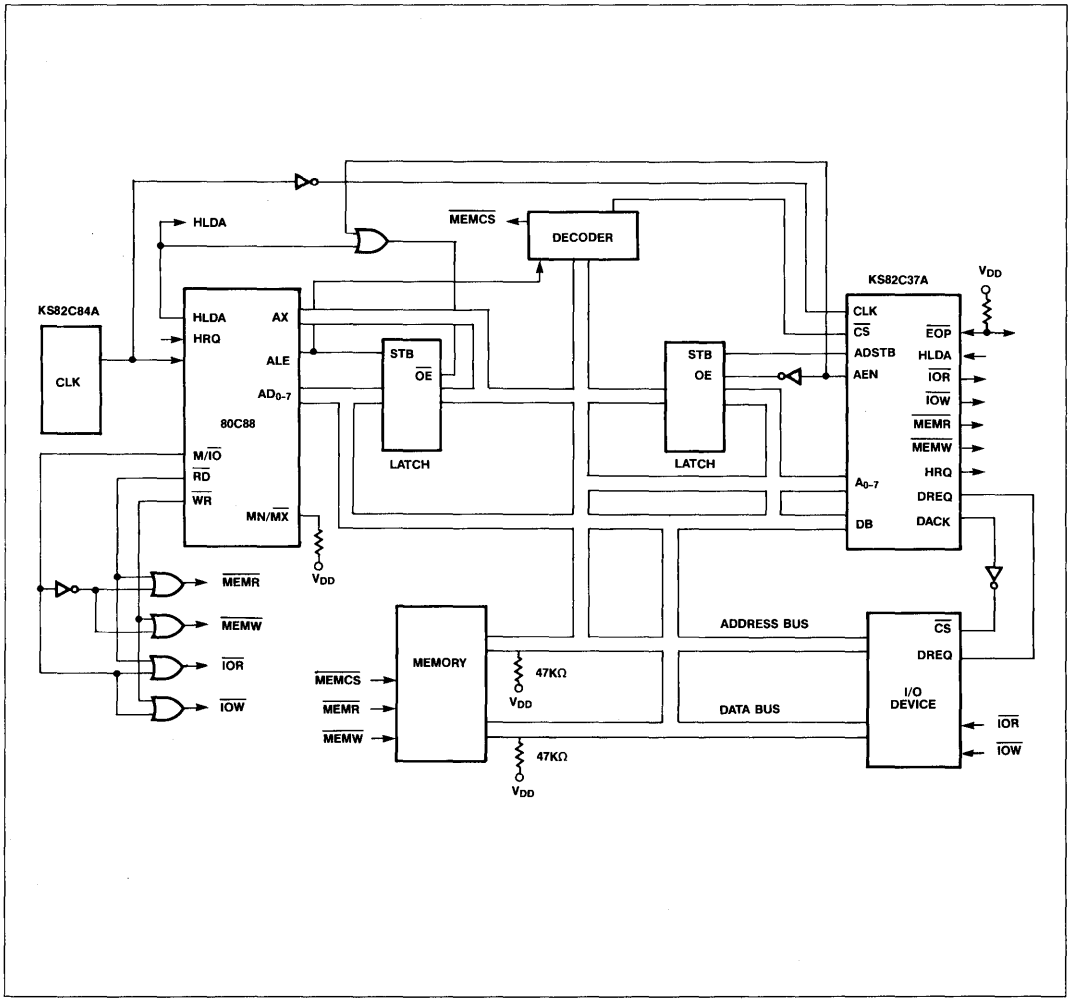


Table 9: Recommended Operating Conditions

DC Supply Voltage		+4.0V to +6.0V
Operating Temperature Range	Commercial	0°C to 70°C
	Industrial	-40°C to +85°C

Table 10: Absolute Maximum Ratings

DC Supply Voltage	+7.0V
Input, Output or I/O Voltage Applied	V_{SS} - 0.5V to V_{CC} + 0.5V
Storage Temperature Range	-65°C to +150°C
Maximum Package Power Dissipation	1W

Note: Stresses beyond those listed above may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 11: Capacitance (T_A = 25°C, V_{CC} = 0V, V_{IN} = +5V or V_{SS})

Symbol	Parameter	Test Conditions	Typ	Units
$C_{I/O}$	I/O Capacitance	FREQ = 1MHz Unmeasured Pins Returned to V_{SS}	20	pF
C_{IN}	Input Capacitance		5	pF
C_{OUT}	Output Capacitance		15	pF

Table 12: DC Characteristics (T_A = 0°C to 70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V)

Symbol	Parameter	Test Conditions	Limits		Units
			Min	Max	
I_{DD}	Operating Power Supply Current	V_{CC} = 5.5V V_{IN} = V_{CC} or V_{SS} Outputs Open	—	2.0	mA/MHz
I_{DDSB}	Standby Power Supply Current	V_{CC} = 5.5V V_{IN} = V_{CC} or V_{SS} Outputs Open	—	100	μA
I_{IL}	Input Leakage Current for Unidirectionals	$0V \leq V_{IN} \leq V_{CC}$	-1.0	+1.0	μA
I_{ILIO}	Input Leakage Current for Bidirectionals	$0V \leq V_{IN} \leq V_{CC}$	-10.0	+10.0	μA
I_{OL}	Output Leakage Current	$0V \leq V_{OUT} \leq V_{CC}$	-10.0	+10.0	μA
V_{IH}	Logical One Input Voltage		2.0	—	V
V_{IL}	Logical Zero Input Voltage		—	0.8	V
V_{OH}	Output High Voltage	I_{OH} = -2.5mA I_{OH} = -100μA	2.4 V_{CC} - 0.4	— —	V V
V_{OL}	Output Low Voltage	I_{OL} = +3.2mA	—	0.4	V

Notes:
1. Input timing parameters assume rise and fall transition times of 20ns or less.
2. The net $\overline{IOW}$ or $\overline{MEMW}$ pulse width for a normal write will be t_{CY} - 100ns, and for an extended write will be 2 · t_{CY} - 100ns. The net $\overline{IOR}$ or $\overline{MEMR}$ pulse width for a normal read will be 2 · t_{CY} - 50ns and for a compressed read will be t_{CY} - 50ns.
3. DREQ should be held active until DACK is returned.
4. DREQ and DACK signals may be active HIGH or active LOW. The timing diagrams assume active HIGH.
5. Successive read and/or write operations by the external processor to program or examine the controller must be timed to allow at least 100ns (KS82C37A-10) and 200ns (KS82C37A-5) as recovery time between active read or write pulses.
6. $\overline{EOP}$ is an open drain output, and requires a pullup resistor to V_{CC}.
7. Pin 5 can be either tied to V_{DD}, or left unconnected.

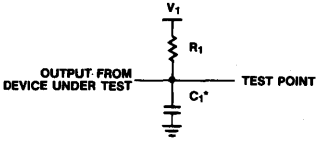
Table 13: AC Characteristics, DMA (Master) Mode (T_A = 0 to 70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V)

Symbol	Parameter	Limits (5MHz)		Limits (8MHz)		Limits (10MHz)		Units
		Min	Max	Min	Max	Min	Max	
t_{AEL}	AEN HIGH from CLK LOW (S_1) Delay Time	—	175	—	105	—	90	ns
t_{AET}	AEN LOW from CLK HIGH (S_1) Delay Time	—	130	—	80	—	80	ns
t_{AFAB}	ADR Active to Float Delay from CLK HIGH	—	90	—	55	—	55	ns
t_{AFC}	$\overline{READ}$ or $\overline{WRITE}$ Float Delay from CLK HIGH	—	120	—	75	—	75	ns
t_{AFDB}	DB Active to Float Delay from CLK HIGH	—	170	—	135	—	100	ns
t_{AHR}	ADR from $\overline{READ}$ HIGH Hold Time	t_{CY}-100	—	t_{CY}-75	—	t_{CY}-75	—	ns
t_{AHS}	DB from ADSTB LOW Hold Time	30	—	25	—	20	—	ns
t_{AHW}	ADR from $\overline{WRITE}$ HIGH Hold Time	t_{CY}-50	—	t_{CY}-50	—	t_{CY}-50	—	ns
t_{AK}	DACK Valid from CLK LOW Delay Time	—	170	—	105	—	90	ns
	$\overline{EOP}$ HIGH from CLK HIGH Delay Time	—	170	—	105	—	90	ns
	$\overline{EOP}$ LOW from CLK HIGH Delay Time	—	100	—	60	—	60	ns
t_{ASM}	ADR Stable from CLK HIGH	—	110	—	60	—	60	ns
t_{ASS}	DB to ADSTB LOW Setup Time	100	—	85	—	75	—	ns
t_{CH}	CLK HIGH Time	70	—	55	—	45	—	ns
t_{CL}	CLK LOW Time	70	—	50	—	45	—	ns
t_{CY}	CLK Cycle Time	200	—	125	—	100	—	ns
t_{DCL}	CLK HIGH to $\overline{READ}$ or $\overline{WRITE}$ LOW Delay	—	190	—	120	—	90	ns
t_{DCTR}	$\overline{READ}$ HIGH from CLK HIGH (S_1) Delay Time	—	190	—	115	—	95	ns
t_{DCTW}	$\overline{WRITE}$ HIGH from CLK HIGH (S_1) Delay Time	—	130	—	80	—	80	ns
t_{DQ1}	HRQ Valid from CLK HIGH Delay Time	—	120	—	75	—	75	ns
t_{DQ2}	HRQ Valid from CLK HIGH Delay Time	—	120	—	75	—	75	ns
t_{EPS}	$\overline{EOP}$ LOW from CLK LOW Setup Time	40	—	25	—	25	—	ns
t_{EPW}	$\overline{EOP}$ Pulse Width (ext. $\overline{EOP}$)	220	—	135	—	80	—	ns
t_{FAAB}	ADR Float to Active Delay from CLK HIGH	—	110	—	60	—	60	ns
t_{FAC}	$\overline{READ}$ or $\overline{WRITE}$ Active from CLK HIGH	—	150	—	90	—	90	ns
t_{FADB}	DB Float to Active Delay from CLK HIGH	—	110	—	60	—	60	ns
t_{HS}	HLDA Valid to CLK HIGH Setup Time	75	—	45	—	45	—	ns
t_{IDH}	Input Data from $\overline{MEMR}$ HIGH Hold Time	0	—	0	—	0	—	ns
t_{IDS}	Input Data to $\overline{MEMR}$ HIGH Setup Time	155	—	90	—	80	—	ns
t_{ODH}	Output Data from $\overline{MEMW}$ HIGH Hold Time	15	—	15	—	15	—	ns
t_{ODV}	Output Data Valid to $\overline{MEMW}$ HIGH	125	—	85	—	65	—	ns
t_{QS}	DREQ to CLK LOW (S_1, S_4) Setup Time	0	—	0	—	0	—	ns
t_{RH}	CLK to READY LOW Hold Time	20	—	20	—	10	—	ns
t_{RS}	READY to CLK LOW Setup Time	60	—	35	—	35	—	ns
t_{STL}	ADSTB HIGH from CLK HIGH Delay Time	—	80	—	50	—	50	ns
t_{STT}	ADSTB LOW from CLK HIGH Delay Time	—	90	—	90	—	90	ns

Table 14: AC Characteristics, Peripheral (Slave) Mode (T_A = 0 to 70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V)

Symbol	Parameter	Limits (5MHz)		Limits (8MHz)		Limits (10MHz)		Units
		Min	Max	Min	Max	Min	Max	
t_{AR}	ADR Valid or $\overline{CS}$ LOW to $\overline{READ}$ LOW	10	—	10	—	0	—	ns
t_{AW}	ADR Valid to $\overline{WRITE}$ HIGH Setup Time	130	—	100	—	60	—	ns
t_{CW}	$\overline{CS}$ LOW to $\overline{WRITE}$ HIGH Setup Time	130	—	100	—	85	—	ns
t_{DW}	Data Valid to $\overline{WRITE}$ HIGH Setup Time	130	—	100	—	90	—	ns
t_{RA}	ADR or $\overline{CS}$ Hold from $\overline{READ}$ HIGH	0	—	0	—	0	—	ns
t_{RDE}	Data Access from $\overline{READ}$	—	140	—	120	—	95	ns
t_{RDF}	DB Float Delay from $\overline{READ}$ HIGH	0	70	0	70	0	70	ns
t_{RSTD}	Power Supply HIGH to RESET LOW Setup Time	500	—	500	—	500	—	ns
t_{RSTS}	RESET to First $\overline{IOWR}$	$2 \cdot t_{CY}$	—	$2 \cdot t_{CY}$	—	$2 \cdot t_{CY}$	—	ns
t_{RSTW}	RESET Pulse Width	300	—	200	—	100	—	ns
t_{RW}	I/O Read Width	200	—	155	—	120	—	ns
t_{WA}	ADR from $\overline{WRITE}$ HIGH Hold Time	0	—	0	—	0	—	ns
t_{WC}	$\overline{CS}$ HIGH from $\overline{WRITE}$ HIGH Hold Time	0	—	0	—	0	—	ns
t_{WD}	Data from $\overline{WRITE}$ HIGH Hold Time	10	—	10	—	10	—	ns
t_{WWS}	$\overline{WRITE}$ Width	150	—	100	—	90	—	ns

Figure 13: AC Test Circuits



PINS	V_1	R_1	C_1
All Outputs Except $\overline{EOP}$	1.7V	520Ω	100pF
$\overline{EOP}$	V_{CC}	1.6KΩ	50pF

Figure 14: AC Testing Input, Output Waveforms

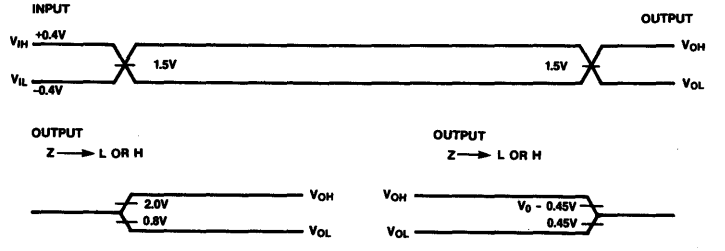
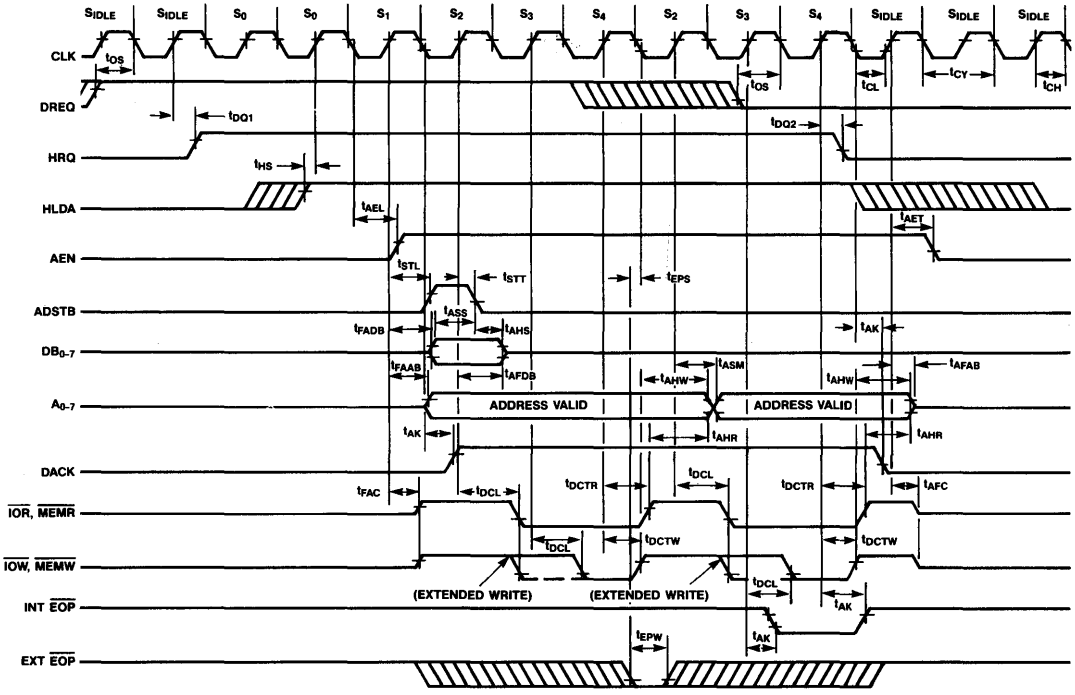
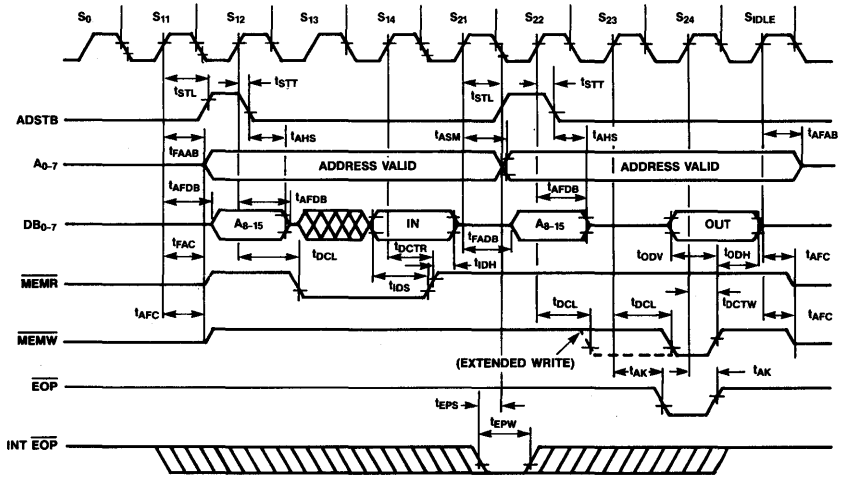


Figure 15: Timing Diagrams (Master Mode)

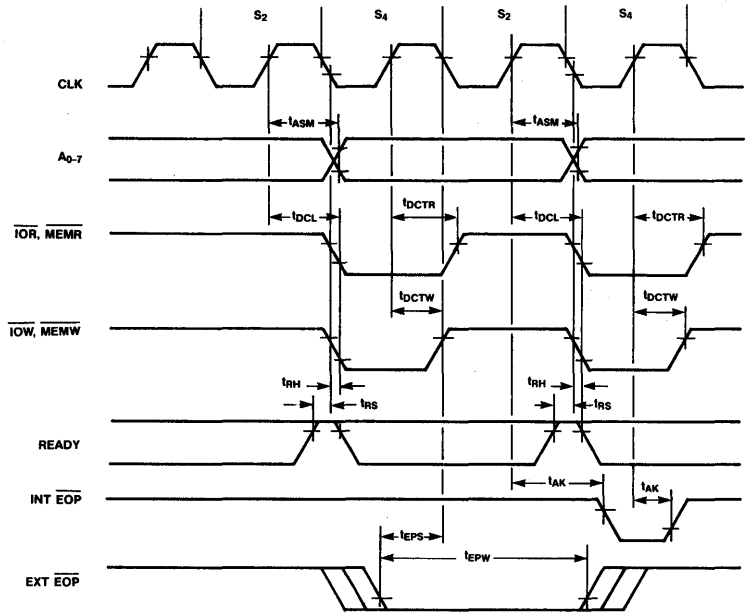
a) DMA Transfer Timing



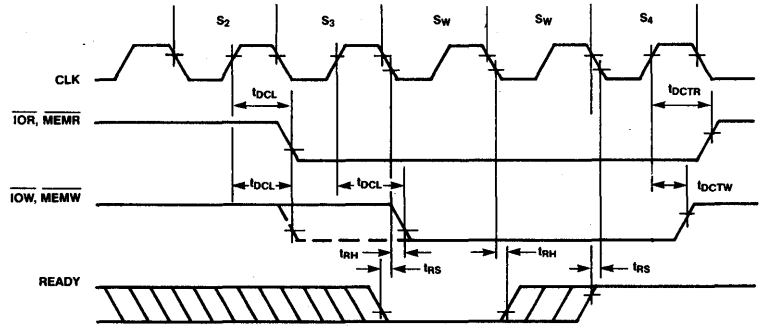
b) Memory-to-Memory Transfer Timing



c) Compressed Transfer Timing



d) Ready Timing



e) Reset Timing

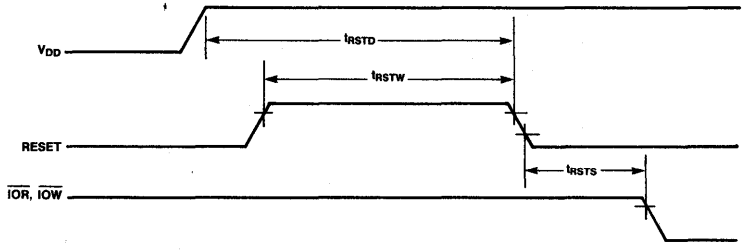
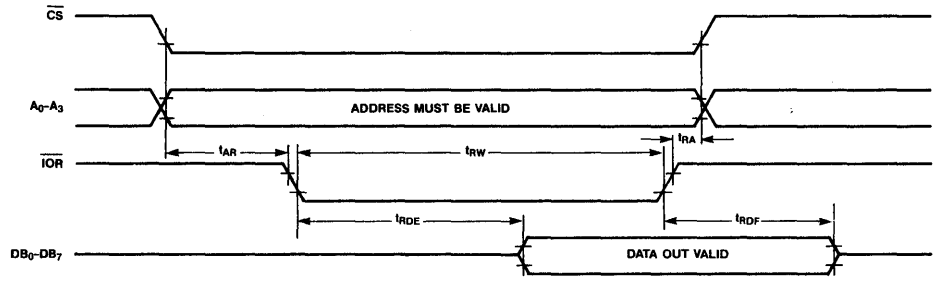
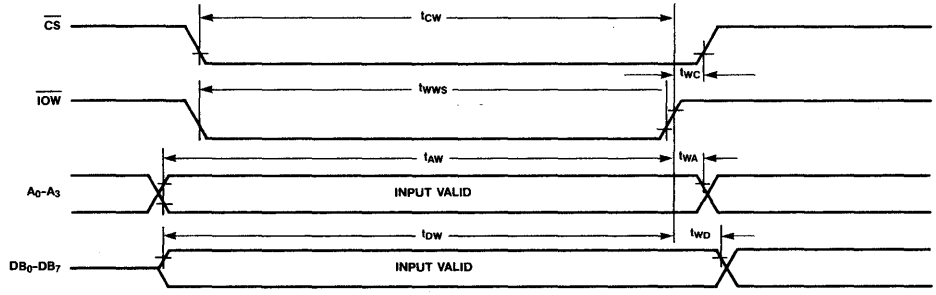


Figure 16: Timing Diagrams (Slave Mode)

a) Slave Mode Read Timing

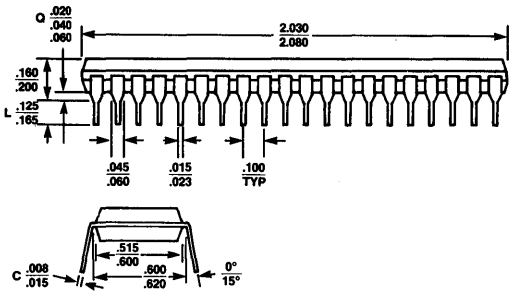


b) Slave Mode Write Timing

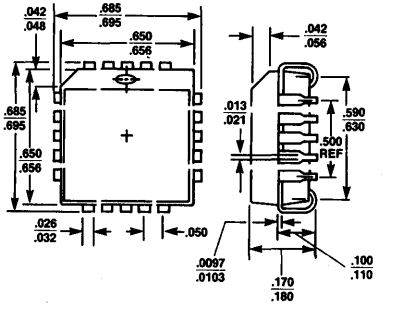


PACKAGE DIMENSIONS

Units: Inches



Plastic Package



44 Pin PLCC

ORDERING INFORMATION & PRODUCT CODE DIMENSIONS

KS 82C37A X X X

SAMSUNG SEMICONDUCTOR

Part Number

Speed
-5 5MHz
-8 8MHz
-10 10MHz

Packaging
P — Plastic DIP
L — Plastic Leaded Chip Carrier (PLCC)

Temperature
C — Commercial (0°C to +70°C)
I — Industrial (-40°C to +85°C)

SAMSUNG products are designated by a Product Code. When ordering, please refer to products by their full code. For unusual, and/or specific packaging or processing requirements not covered by the standard product line, please contact the SAMSUNG MOS Products Group.

FEATURES

- **Single Chip UART/BRG**
- **DC to 10 MHz Operation (DC to 625K Baud)**
- **Crystal or External Clock Input**
- **On Chip Baud Rate Generator 1 to 65535 Divisor Generates 16x Clock**
- **Prioritized Interrupt Mode**
- **Fully TTL/CMOS Compatible**
- **Microprocessor Bus Oriented Interface**
- **Easily interfaces to most popular μ-processors**
- **Low Power CMOS Implementation (1 mA/MHz Typ)**
- **Modem Interface**
- **Line Break Generation and Detection**
- **Loopback Mode**
- **Double Buffered Transmitter and Receiver**
- **Single 5V Supply**

DESCRIPTION

The KS82C450 is an improved specification version of the KS82C50A Asynchronous Communications Element (ACE). Functionally, the KS82C450 is equivalent to the KS82C50A..

The KS82C450/KS82C50A are functionally equivalent to their NMOS counterparts, except that they are fabricated in CMOS.

The 82C50A Asynchronous Communications Element (ACE) is a high performance programmable Universal Asynchronous Receiver/Transmitter (UART) and Baud Rate Generator (BRG) on a single chip. The device supports data rates from DC to 625K baud (0 - 10 MHz clock).

The ACE receiver circuitry converts start, data, stop and parity bits into a parallel data word. The transmitter circuitry converts a parallel data word into serial form and appends the start, parity and stop bits. The word length is programmable to 5, 6, 7 or 8 data bits. Stop bit selection provides a choice of 1, 1.5 or 2 stop bits.

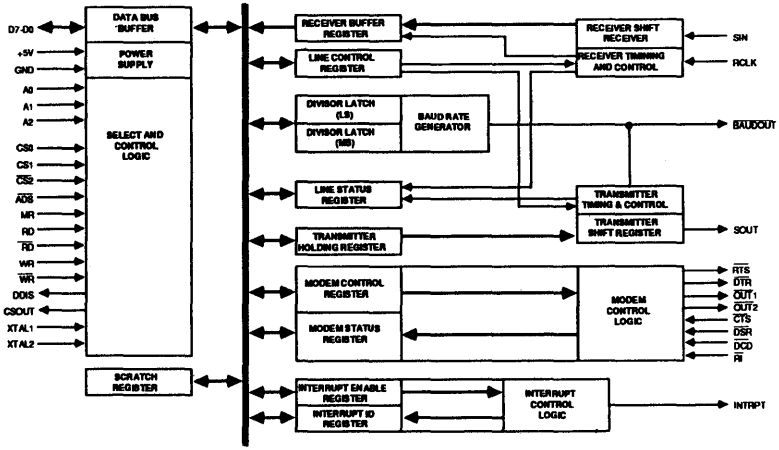


Figure 1 : BLOCK DIAGRAM OF KS82C450/KS82C50A

DESCRIPTION (Continued)

The Baud Rate Generator divides the clock by a divisor programmable from 1 to $2^{16}-1$ to provide standard RS-232C baud rates when using any one of three industry standard baud rate crystals (1.8432 MHz, 2.4576 MHz or 3.072 MHz). The BAUDOUT programmable clock output provides a buffered oscillator or a 16x (16 times the data rate) baud rate clock for general purpose system use.

To meet the system requirements of a CPU interfacing to an asynchronous channel, the modem control signals RTS, CTS, DSR, DTR, RI, DCD are provided. Inputs and outputs have been designed with full TTL/CMOS compatability in order to facilitate mixed TTL/NMOS/CMOS system design.

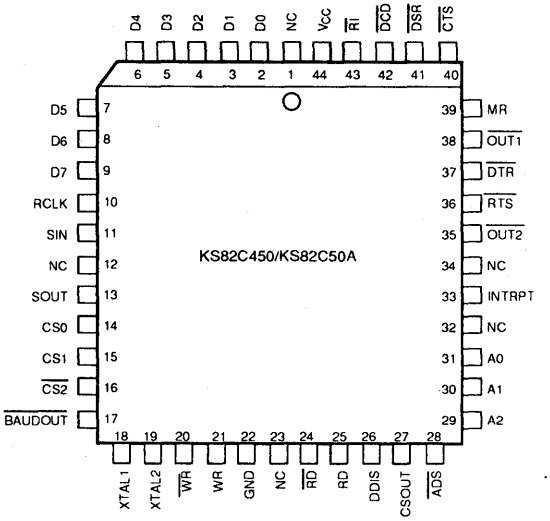


Figure 2a : PLCC CONFIGURATION

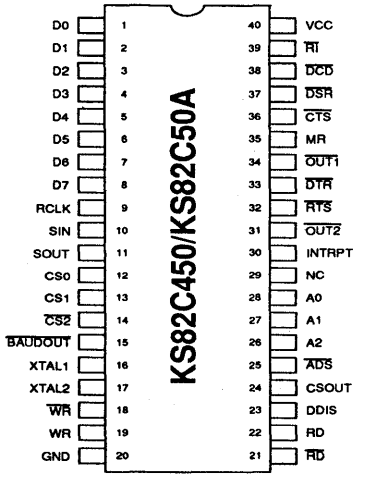


Figure 2b : 40-PIN DIP CONFIGURATION

Table 1 : PIN DESCRIPTIONS

Symbol	Pin(s)	Type	Name and Function
$\overline{RD}$, RD	22, 21	I	Read, Read: $\overline{RD}$, RD are read inputs which cause the KS82C450/KS82C50A to output data to the data bus (D_0 - D_7). The data output depends upon the register selected by the address inputs A_0, A_1 and A_2. The chip select inputs CS0, CS1 and $\overline{CS2}$ enable the RD, RD inputs. Only an active $\overline{RD}$ or RD, not both, is used to receive data from the KS82C450/KS82C50A during a read operation. If RD is used as the read input, $\overline{RD}$ should be tied high. If $\overline{RD}$ is used as the active read input, RD should be tied low.
$\overline{WR}$, WR	19,18	I	Write, Write:$\overline{WR}$, WR are write inputs which cause data from the data bus (D_0 - D_7) to be input to the KS82C450/KS82C50A. The data input depends upon the register selected by the address inputs A_0, A_1 and A_2. The chip select inputs CS_0, CS_1 and $\overline{CS_2}$ enable the $\overline{WR}$, WR inputs. Only an active $\overline{WR}$ or WR, not both, is used to transmit data to the KS82C450/KS82C50A during a write operation. If WR is used as the write input, $\overline{WR}$ should be tied high. If $\overline{WR}$ is used as the write input, WR must be tied low.
D_0 - D_7	1 - 8	I/O	Data Bus: The Data Bus provides eight, 3-state input/output lines for the transfer of data, control and status information between the KS82C450/KS82C50A and the CPU. For character formats of less than 8 bits, D7, D6 and D5 are *don't cares* for data write operations and zero for data read operations. These lines are normally in a high impedance state except during read operations. D0 is the Least Significant Bit (LSB) and is the first serial data bit to be received or transmitted.
A_0, A_1, A_2	28, 27,26	I	Register Select: The address lines select the internal registers during CPU bus operations.
$XTAL_1$, $XTAL_2$	16, 17	I, O	Crystal/Clock: Crystal connections for the internal Baud Rate Generator. XTAL1 can also be used as an external clock input, in which case XTAL2 should be left open.
SOUT	11	O	Serial Data Output: Serial data ouputput from the KS82C450/KS82C50A transmitter circuitry. A Mark (1) is a logic one (high) and Space (0) is a logic zero (low). SOUT is held in the Mark condition when the transmitter is disabled, MR is true, the Transmitter Register is empty, or when in the Loop Mode. SOUT is not affected by the CTS input.
V_{SS}	20	-	Ground: Power supply ground, 0V
$\overline{CTS}$	36	I	Clear to Send: An active low signal, the logical state of the $\overline{CTS}$ pin is reflected in the CTS bit of the (MSR) Modem Status Register (CTS is bit 4 of the MSR, written MSR[4]). A change of state in the $\overline{CTS}$ pin since the previous reading of the MSR causes the setting of DCTS (MSR[0]) of the Modem Status Register. When $\overline{CTS}$ is active (low), the modem is indicating that data on SOUT can be transmitted on the communications link. If $\overline{CTS}$ pin goes inactive (high), the KS82C450/KS82C50A should not be allowed to transmit data out of SOUT. $\overline{CTS}$ pin does not affect Loop Mode operation.
$\overline{DSR}$	37	I	Data Set Ready: An active low signal, the logical state of the $\overline{DSR}$ pin is reflected in MSR[5] of the Modem Status Register. DDSR (MSR[1]) indicates whether the DSR pin has changed state since the previous reading of the MSR. When the $\overline{DSR}$ pin is active (low), the modem is indicating that it is ready to exchange data with the KS82C450/KS82C50A, while the $\overline{DSR}$ pin inactive (high) indicates that the modem is not ready for data exchange. The active condition indicates only the condition of the local Data Communications Equipment (DCE), and does not imply that a data circuit has been established with remote equipment.

Table 1 : PIN DESCRIPTIONS con't

Symbol	Pin(s)	Type	Name and Function
$\overline{DTR}$	33	O	Data Terminal Ready: An active low signal, the $\overline{DTR}$ pin can be set (low) by writing a logic one to MCR[0]. Modem Control Register bit 0. This signal is cleared (high) by writing a logic zero to the DTR bit (MCR[0]) or whenever a MR active (high) is applied to the KS82C450/KS82C50A. When active (low), $\overline{DTR}$ pin indicates to the DCE that the KS82C450/KS82C50A is ready to receive data. In some instances, DTR pin is used as a power on indicator. The inactive (high) state causes the DCE to disconnect the modem from the telecommunications circuit.
$\overline{RTS}$	32	O	Request to Send: An active low signal, $\overline{RTS}$ is an output used to enable the modem. The $\overline{RTS}$ pin is set low by writing a logic one to MCR[1] bit 1 of the Modem Control Register. The $\overline{RTS}$ pin is reset high by Master Reset. When active, the RTS pin indicates to the DCE that the KS82C450/KS82C50A has data ready to transmit. In half duplex operations, RTS is used to control the direction of the line.
$\overline{BAUDOUT}$	15	O	$\overline{BAUDOUT}$: This active low output signal is a 16x clock out used for the transmitter section (16x = 16 times the data rate). The $\overline{BAUDOUT}$ clock rate is equal to the reference oscillator frequency divided by the specified divisor in the Baud Rate Generator Divisor Latches DLL and DLM. $\overline{BAUDOUT}$ may be used by the receiver section by tying this output to RCLK.
$\overline{OUT1}$	34	O	Output 1: This is an active low general purpose output that can be programmed active (low) by setting MCR[2] (OUT1) of the Modem Control Register to a high level. The $\overline{OUT1}$ pin is set high by Master Reset. The $\overline{OUT1}$ pin is inactive (high) during loop mode operation.
$\overline{OUT2}$	31	O	Output 2: This a an active low general purpose output that can be programmed active (low) by setting MCR[3] (OUT2) of the Modem Control Register to a high level. The $\overline{OUT2}$ pin is set high by Master Reset. The $\overline{OUT2}$ signal is inactive (high) during loop mode operation.
$\overline{RI}$	39	I	Ring Indicator: When low, $\overline{RI}$ indicates that a telephone ringing signal has been received by the modem or data set. The $\overline{RI}$ signal is a modem control input whose condition is tested by reading MSR[6] (RI). The Modem Status Register output TERI (MSR[2]) indicates whether the $\overline{RI}$ input has changed from a low to high since the previous reading of the MSR. If the interrupt is enabled (IER[3] = 1) and $\overline{RI}$ changes from a high to low, an interrupt is generated. The active (low) state of $\overline{RI}$ indicates that the DCE is receiving a ringing signal. $\overline{RI}$ will appear active for approximately the same length of time as the active segment of the ringing cycle. The inactive state of RI will occur during the inactive segments of the ringing cycle, or when ringing is not detected by the DCE. This circuit is not disabled by the inactive condition of $\overline{DTR}$.
$\overline{DCD}$	38	I	Data Carrier Detect: When active (low), $\overline{DCD}$ indicates that the data carrier has been detected by the modem or data set. $\overline{DCD}$ is a modem input whose condition can be tested by the CPU by reading MSR[7] (DCD) of the Modem Status Register, MSR[3] (DDCD) of the Modem Status Register indicates whether the $\overline{DCD}$ input has changed since the previous reading of the MSR. $\overline{DCD}$ has no effect on the receiver. If the DCD changes state with the modem status interrupt enabled, an interrupt is generated. When $\overline{DCD}$ is active (low), the received line signal from the remote terminal is within the limits specified by the DCE manufacturer. The inactive (high) signal indicates that the signal is not within the specified limits, or is not present.

Table 1 : PIN DESCRIPTIONS con't

Symbol	Pin(s)	Type	Name and Function
MR	35	I	Master Reset: The MR input forces the KS82C450/KS82C50A into an idle mode in which all serial data activities are suspended. The Modem Control Register (MCR) along with its associated outputs are cleared. The Line Status Register (LSR) is cleared except for the THRE and TEMT bits, which are set. The KS82C450/ KS82C50A remains in an idle state until programmed to resume serial data activities. The MR input is a TTL compatible Schmitt trigger.
INTRPT	30	O	Interrupt Request: The INTRPT output goes active (high) when one of the following interrupts has an active (high) condition and is enabled by the Interrupt Enable Register: Receiver Error flag; Received Data Available; Transmitter Holding Register Empty; and Modem Status. The INTRPT is reset low upon appropriate service or a MR operation.
SIN	10	I	Serial Data Input: The SIN input is the serial data input from the communication line or modem to the KS82C450/KS82C50A receiver circuits. A Mark (1) is high, and a Space (0) is low. Data inputs on SIN are disabled when operating in the loop mode.
V_{DD}	40	-	Power Supply: +5V ±10% DC Supply. A 0.1 μA decoupling capacitor from V_{DD} (pin 40) to V_{SS} (pin 20) is recommended.
CS0, CS1, $\overline{CS2}$	12, 13, 14	I	Chip Select: The Chip Select inputs act as enable signals for the write ($\overline{WR}$, WR) and read ($\overline{RD}$, RD) input signals. The Chip select inputs are latched by the $\overline{ADS}$ input.
NC	29	-	Do Not Connect
CSOUT	24	O	Chip Select Out: When active (high), this pin indicates that the chip has been selected by active CS0, CS1 and $\overline{CS2}$ inputs. No data trasfer can be initiated until CSOUT is a logic one, active (high).
DDIS	23	O	Driver Disable: This output is inactive (low) when the CPU is reading data from the KS82C450/KS82C50A. An active (high) DDIS output can be used to disable an external transceiver when the CPU is reading data.
$\overline{ADS}$	25	I	$\overline{Address\ Strobe}$: When active (low), $\overline{ADS}$ latches the Register Select (A0, A1 and A2) and Chip Select (CS0, CS1 and $\overline{CS2}$) inputs. An active $\overline{ADS}$ is required when the Register Select pins are not stable for the duration of the read or write operation, multiplexed mode. If not required, the $\overline{ADS}$ input should be tied low, non-multiplexed mode.
RCLK	9	I	Receiver Clock: This input is the 16x Baud Rate Clock for the receiver section of the KS82C450/KS82C50A. This input may be provided from the BAUDOUT output or an external clock.

Table 2a : AC CHARACTERISTICS: (T_A=0°C to +70°C, V_{CC}=5.0V ±10%)

Symbol	Parameter	Test Conditions	*KS82C450		KS82C50A		Units
			Min	Max	Min	Max	
tADS	Address strobe width		60	-	90	-	ns
tAS	Address Setup time		60	-	90	-	ns
tAH	Address Hold Time		0	-	0	-	ns
tCS	Chip Select Setup Time		60	-	90	-	ns
tCH	Chip Select Hold Time		0	-	0	-	ns
tDIW	$\overline{RD}$/RD Strobe Width		125	-	175	-	ns
tRC	Read Cycle Delay		175	-	500	-	ns
RC	Read Cycle = tAR* + tDIW + tRC		360	-	755	-	ns
tDD	RD/$\overline{RD}$ to Driver Disable Delay	@100 pF loading ***	-	60	-	75	ns
tDDD	Delaly from $\overline{RD}$/RD to Data	@100 pF loading***	-	125	-	175	ns
tHZ	$\overline{RD}$, RD to Floating Data delay	@100 pF loading***	0	100	100	-	ns
tDOW	$\overline{WR}$/WR Strobe Width		100	-	175	-	ns
tWC	Write Cycle Delay		200	-	500	-	ns
WC	Write Cycle = tAW + tDOW + tWC		360	-	755	-	ns
tDS	Data Setup Time		40	-	90	-	ns
tDH	Data Hold Time		40	-	60	-	ns
tCSC*	Chip Select Output Delay from Select	@100 pF loading*	-	100	-	125	ns
tRA*	Address hold time from $\overline{RD}$, RD		20	-	20	-	ns
tRCS*	Chip Selct Hold Time from $\overline{RD}$/RD		20	-	20	-	ns
tAR*	$\overline{RD}$, RD Delay from Address		60	-	80	-	ns
tCSR*	$\overline{RD}$/RD Delay from Chip Select		50	-	80	-	ns
tWA*	Address Hold Time from $\overline{WR}$/WR		20	-	20	-	ns
tWCS*	Chip select hold time from $\overline{WR}$, WR		20	-	20	-	ns
tAW*	$\overline{WR}$/WR Delay from Address		60	-	80	-	ns
tCSW*	$\overline{WR}$/WR Delay from Select		50	-	80	-	ns
tMRW	Master Reset Pulse Width		5	-	10	-	μs
tXH	Duration of Clock High Pulse	External Clock (3.1 MHz Max.)	140	-	140	-	ns
tXL	Duration of Clock Low Pulse	External Clock (3.1 MHz Max.)	140	-	140	-	ns

*: Preliminary

Table 2a : AC CHARACTERISTICS (Continued): (T_A=0°C to +70°C, V_{CC}=5.0V ±10%)

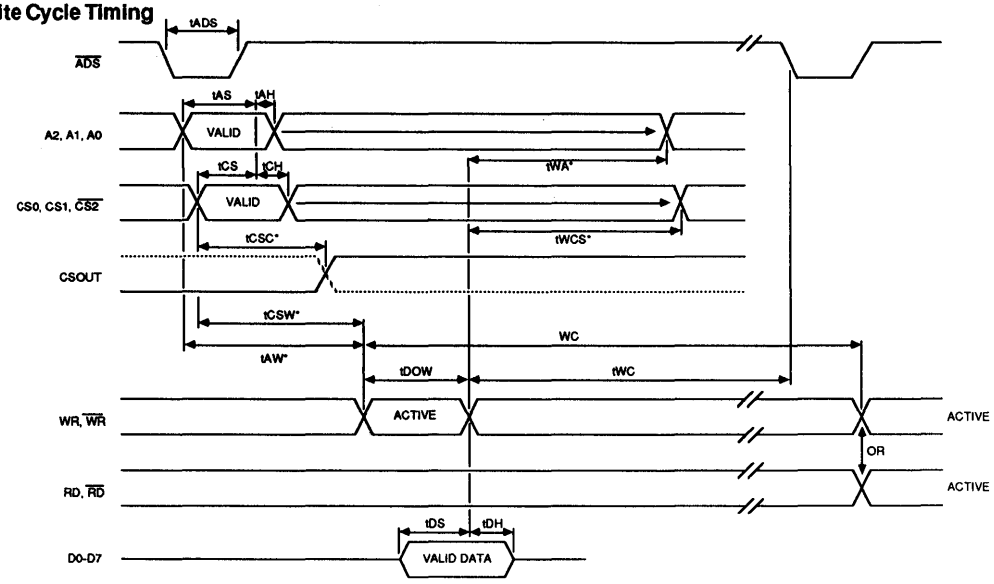
Symbol	Parameter	Test Conditions	*KS82C450		KS82C50A		Units
			Min	Max	Min	Max	
Baud Generator							
N	Baud Divisor		1	2^{16}-1	1	2^{16}-1	-
tBLD	Baud Output Negative Edge Delay	100 pF Load	-	125	-	250	ns
tBHD	Baud Output Positive Edge Delay	100 pF Load	-	125	-	250	ns
tLW	Baud Output Down Time	fX = 2MHz, ÷ 2, 100 pF Load	425	-	425		ns
tHW	Baud Output Up Time	fX = 3 MHz, ÷ 3, 100 pF Load	330	-	330	-	ns
Receiver							
tSCD	Delay from RCLK to Sample Time		-	2	-	2	µs
tSINT	Delay from Stop to Set Interrupt			1		1	RCLK**
tRINT	Delay from $\overline{RD}$/RD (RD RBR/RD LSR) to Reset Interrupt	100 pF Load		1		1	µs
Transmitter							
tHR	Delay from $\overline{WR}$/WR (WR THR) to Reset Interrupt	100 pF Load	-	175	-	1000	ns
tIRS	Delay from Initial INTR Reset to Transmit Start		24	40	24	40	RCLK Cycles
tSI	Delay from Initial Write to Interrupt (Note 1)		16	48	16	48	RCLK Cycles
tSTI	Delay from Stop to Interrupt (THRE)			8		8	RCLK Cycles**
tIR	Delay from $\overline{RD}$/RD (RD IIR) to to Reset Interrupt (THRE)	100 pF Load	-	250	-	1000	ns
Modem Control							
tMDO	Delay from $\overline{WR}$/WR (WR MCR) to Output	100 pF Load	-	200	-	1000	ns
tSIM	Delay to Set Interrupt from MODEM Input	100 pF Load		250	-	1000	ns
tRIM	Delay to Reset Interrupt from $\overline{RD}$/RD (RD MSR)	100 pF Load	-	250	-	1000	ns

*Applicable only when $\overline{ADS}$ is tied low.
**RCLK is equal to t_{XH} and t_{XL}.
***Charge and discharge time is determined by V_{OL}, V_{OH} and the external loading.

* Note: Preliminary

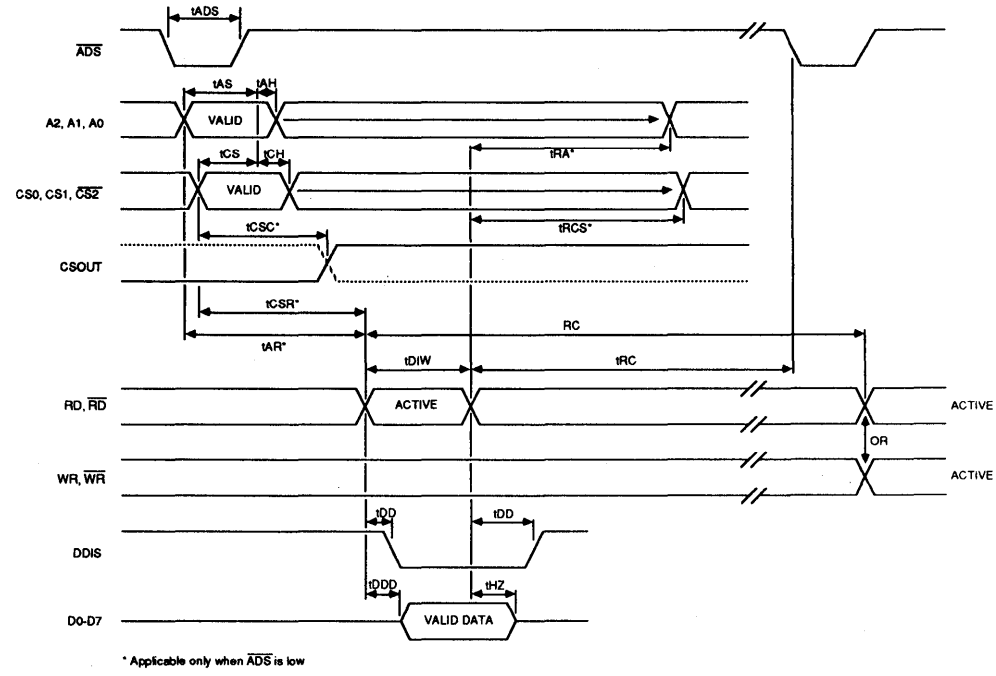
Figure 3 : TIMING DIAGRAMS

a) Write Cycle Timing



* Applicable only when ADS is low

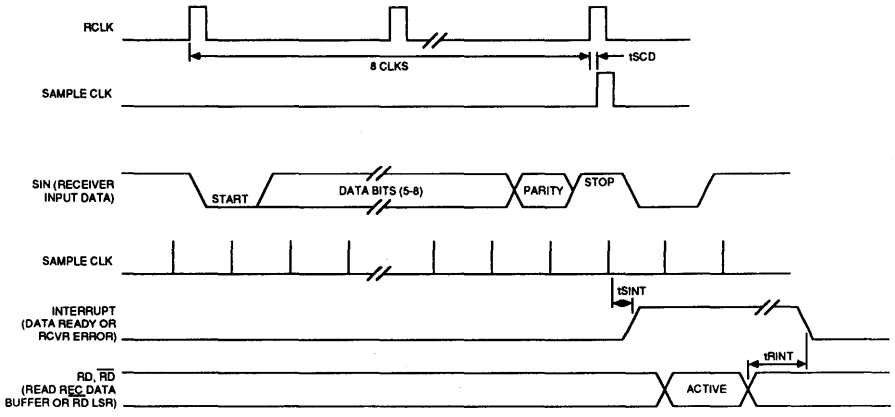
b) Read Cycle Timing



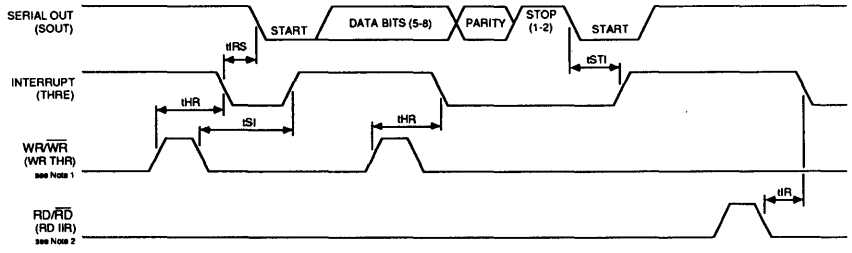
* Applicable only when ADS is low

Figure 3 : TIMING DIAGRAMS con't

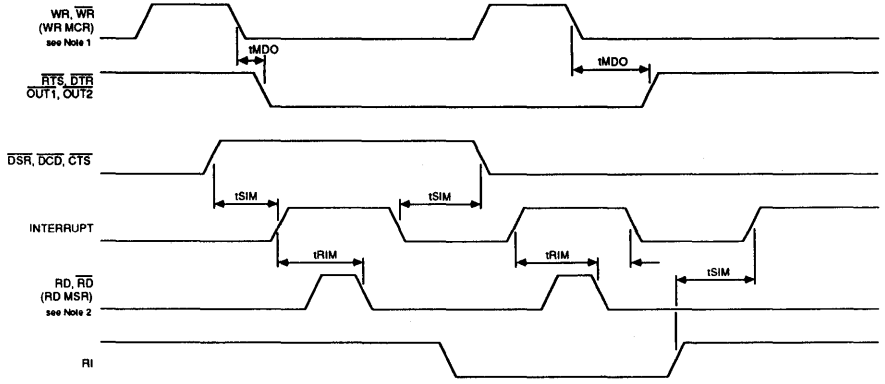
c) Receiver Timing



d) Transmitter Timing



e) Modem Controls Timing



Notes: 1. See Write Cycle Timing
2. See Read Cycle Timing

Figure 3 : TIMING DIAGRAMS con't

f) $\overline{\text{BAUDOUT}}$ Timing

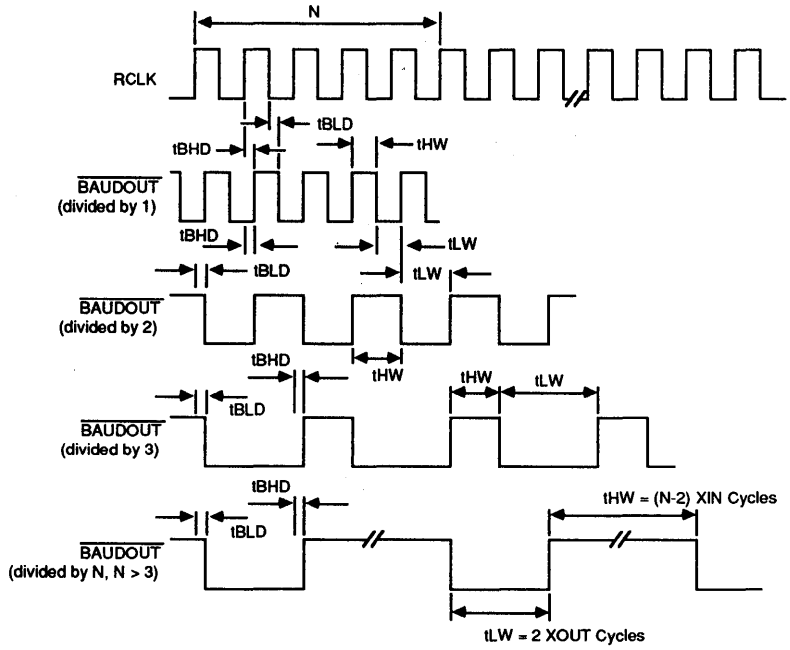


Table 3 : CAPACITANCE (TA=25°C, VDD=VSS=0V, VIN=+5V or VSS)

Symbol	Parameter	Test Conditions	Typical Values	Units
CIN	Input capacitance	Freq = 1 MHz	15	pF
COUT	Output capacitance	Unmeasured pins	15	pF
CI/O	I/O capacitance	returned to VSS	20	pF

Table 4 : OPERATING CONDITIONS

Operating Voltage Range	+4.5V to +5.5V
Operating Temperature Range	
Commercial	0°C to +70°C
Industrial	-40°C to +85°C

Table 5 : ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+8.0 Volts
Input, Output or I/O Voltage Applied	GND -0.5V to V_{CC} +0.5V
Storage Temperature Range	-65°C to +150°C
Maximum Package Power Dissipation	1 Watt
Junction Temperature	+150°C
Lead Temperature (Soldering, 10 seconds)	+260°C
θjc	12°C/W (Cerdip), 17°C/W (LCC)
θja	36°C/W (Cerdip), 41°C/W (LCC)

Table 6 : DC CHARACTERISTICS (T_A=0°C to +70°C, V_{CC}=5.0V ±10%)

Symbol	Parameter	Test Conditions	Limits		Units
			Min	Max	
VIH	Logical one input voltage		2.0	-	V
VIL	Logical zero input voltage		-	0.8	V
VTH	Schmitt trigger logic one input voltage	MR input	2.0	-	V
VTL	Schmitt trigger logic zero input voltage	MR input	-	0.8	V
VIH (CLK)	Logical one clock voltage	External Clock	2.0	V_{CC}	V
VIL (CLK)	Logical zero clock voltage	External Clock	-	0.8	V
VOH	Output high voltage	IOH=-2.5 mA	3.0	-	V
		IOH=-100 μA	V_{CC}-0.4	-	V
VOL	Output low voltage	IOL=+2.5 mA	-	0.4	V
II	Input leakage current	V_{IN}=V_{CC} or GND	-1.0	+1.0	μA
IO	Input/output leakage current	V_{OUT}=V_{CC} or GND	-10.0	+10.0	μA
ICCOP	Operating power supply current	External Clock, Freq=2.4576 MHz, V_{CC}=5.5V, V_{IN}=V_{CC} or GND, Outputs open	-	6	mA
ICCSB	Standby supply current	V_{CC}=5.5V, V_{IN}=V_{CC} or GND, Outputs open		100	μA

REGISTERS

The three types of internal registers in the KS82C450/KS82C50A used in the operation of the device are control, status and data registers. The control registers are the Bit Rate Select Register DLL and DLM, Line Control Register, Interrupt Enable Register and the Modem Control registers, while the status registers are the Line Status Registers and the Modem Status Register. The data registers are the Receiver Buffer Register and Transmitter Holding Register. The Address, Read and Write inputs are used in conjunction with the Divisor Latch Access Bit in the Line Control Register (LCR[7]) to select the register to be written or read (see Table 7). Individual bits within these registers are referred to by the register mnemonic and the bit number in square brackets. An example, LCR[7] refers to Line Control Register Bit 7.

The Transmitter Holding Register and Receiver Buffer Register are data registers holding from 5 to 8 data bits. If less than eight data bits are transmitted, data is right justified to the LSB. Bit 0 of a data word is always the first serial data bit received and transmitted. The KS82C450/KS82C50A data registers are double buffered so that read and write operations can be performed at the same time the UART is performing the parallel to serial and serial to parallel conversion. This provides the microprocessor with increased flexibility in its read and write timing.

Table 7 : ACCESSING KS82C450/KS82C50A INTERNAL REGISTERS

Mnemonic	Register	DLAB	A2	A1	A0
RBR	Receiver Buffer Register (read only)	0	0	0	0
THR	Transmitter Holding Register (write only)	0	0	0	0
IER	Interrupt Enable Register	0	0	0	1
IIR	Interrupt Identification Register (read only)	X	0	1	0
LCR	Line Control Register	X	0	1	1
MCR	Modem Control Register	X	1	0	0
LSR	Line Status Register	X	1	0	1
MSR	Modem Status Register	X	1	1	0
SCR	Scratch Register	X	1	1	1
DLL	Divisor Latch (LSB)	1	0	0	0
DLM	Divisor Latch (MSB)	1	0	0	1

Notes: 1. X = Don't Care
2. 0 = Logic Low
3. 1 = Logic High

Line Control Register (LCR)

The format of the data character is controlled by the Line Control Register. The contents of the LCR may be read, eliminating the need for separate storage of the line characteristics in system memory. The contents of the LCR are described in Table 8.

LCR[0] and LCR[1] word length select bit 0, word length select bit 1: The number of bits in each transmitted or received serial character is programmed per Table 9.

LCR[2] Stop Bit Select: LCR[2] specifies the number of stop bits in each transmitted character. If LCR[2] is a logic zero, one stop bit is generated in the transmitted data. If LCR[2] is a logic one when a 5-bit word length is selected, 1.5 stop bits are generated. If LCR[2] is a logic one when either a 6-, 7- or 8-bit word length is selected, two stop bits are generated. The receiver checks the first stop-bit only, regardless of the number of stop bits selected.

LCR[3] Parity Enable: When LCR[3] is high, a parity bit between the last data word bit and stop bit is generated and checked.

LCR[4] Even Parity Select: When parity is enabled (LCR[3]=1), LCR[4]=0 selects odd parity, and LCR[4]=1 selects even parity.

LCR[5] Stick Parity: When LCR[3, 4 and 5] are logic one the Parity bit is transmitted and checked as a logic zero. If LCR[3 and 5] are one and LCR[4] is a logic zero then the parity bits is transmitted and checked as a logic one. If LCR[5] is a logic zero Stick Parity is disabled.

LCR[6] Break Control: When LCR[6] is set to logic one, the serial output (SOUT) is forced to the spacing (logic zero) state. The break is disabled by setting LCR[6] to a logic zero. The Break Control bit acts only on SOUT and has no effect on the transmitter logic. Break Control enables the CPU to alert a terminal in a computer communications system. If the following sequence is used, no erroneous or extraneous characters will be transmitted because of the break.

1. Load an all 0s pad character in response to THRE.
2. Set break in response to the next THRE.
3. Wait for the transmitter to be idle, (TTEMT=1), and clear break when normal transmission has to be restored.

During the break, the transmitter can be used as a character timer to accurately establish the break duration.

LCR[7] Divisor Latch Access Bit (DLAB): LCR[7] must be set high (logic one) to access the Divisor Latches DLL and DLM of the Baud Rate Generator during a read or write operation. LCR[7] must be input low to access the Receiver Buffer, the Transmitter Holding Register, or the Interrupt Enable Register.

Table 8 : LCR BIT DEFINITIONS

Bit Number	Function
0	Word Length Select Bit 0 (WLS0)
1	Word Length Select Bit 1 (WLS1)
2	Stop Bit Select (STB)
3	Parity Enable (EN)
4	Even Parity Select (EPS)
5	Stick Parity
6	Set Break
7	Divisor Latch Access Bit (DLAB)

Table 9 : LCR WORD LENGTH SELECTION

LCR[1]	LCR[2]	Word Length
0	0	5 Bits
0	1	6 Bits
1	0	7 Bits
1	1	8 Bits

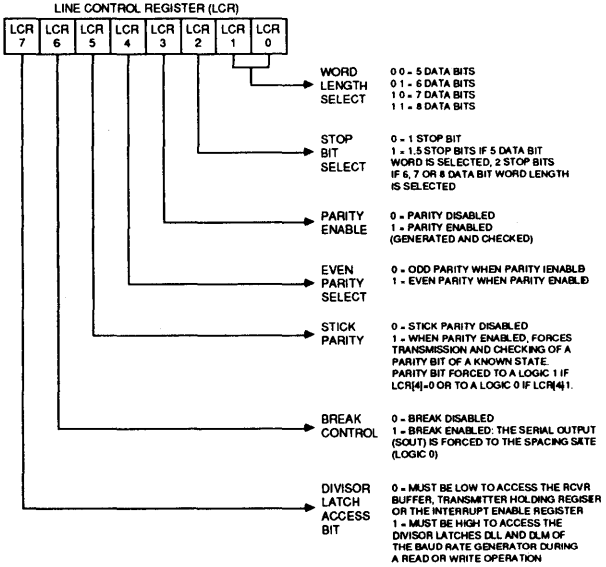


Figure 4 : LINE CONTROL REGISTER

Line Status Register (LSR)

The LSR is a single register that provides status indications. The LSR is usually the first register read by the CPU to determine the cause of an interrupt or to poll the status of the KS82C450/KS82C50A.

Three error flags OE, FE and PE provide the status of any error conditions detected in the receiver circuity. During reception of the stop bits, the error flags are set high by an error condition. The error flags are not reset by the absence of an error condition in the next received character. The flags reflect the last charater only if no overrun occurred. The Overrun Error (OE) indicates that a character in the Receiver Buffer Register has been overwritten by a character from the Receiver Shift Register before being read by the CPU. The character is lost. Framing Error (FE) indicates that the last character received contained incorrect (low) stop bits. This is caused by the absence of the required stop bit or by a stop bit too short to be detected. Parity Error (PE) indicates that the last character received contained a parity error based on the programmed and calculated parity of the received character.

The Break Interrupt (BI) status bit indicates that the last character received was a break character. A break character is an invalid data character, with the entire character, including parity and stop bits, logic zero.

The Transmitter Holding Register Empty (THRE) bit indicates that the THR register is empty and ready to receive another character. The Transmission Shift Register Empty (TEMT) bit indicates that the Transmitter Shift Register is empty, and the KS82C450/KS82C50A has completed transmission of the last character. If the interrupt is enabled (IER[1]), an active THRE causes an interrupt (INTRPT).

The Data Ready (DR) bit indicates that the RBR has been loaded with a received character (included Break) and that the CPU may access this data.

Reading LSR clears LSR[1] - LSR[4], (OE, PE, FE and BI).

The contents of the Line Status Register are indicated in Table 10, and are described below.

LSR[0] Data Ready (DR): Data Ready is set high when an incoming character has been received and transferred into the Receiver Buffer Register. LSR[0] is reset low by a CPU read of the data in the Receiver Buffer Register.

LSR[1] Overrun Error (OE): Overrun Error indicates that data in the Receiver Buffer Register was not read by the CPU before the next character was transferred into the Receiver Buffer Register, overwriting the previous character. The OE indicator is reset whenever the CPU reads the contents of the Line Status Register.

LSR[2] Parity Error (PE): PE indicates that the received data character does not have the correct even or odd parity, as selected by the Even Parity Select bit (LCR[4]). The PE bit is set high upon detection of a parity error, and is reset low when the CPU reads the contents of the LSR.

LSR[3] Framing Error (FE): FE indicates that the received character did not have a valid stop bit. LSR[3] is set high when the stop bit following the last data bit or parity bit is detected as a zero bit (spacing level). The FE indicator is reset low when the CPU reads the contents of the LSR.

LSR[4] Break Interrupt (BI): BI is set high when the received data input is held in the spacing (logic zero) state for longer than a full word transmission time (start bit+data bits+parity+stop bits). The BI indicator is reset when the CPU reads the contents of the Line Status Register.

LSR[1] – LSR[4] are the error conditions that produce a Receiver Line Status interrupt (priority 1 interrupt in the Interrupt Identification Register (IIR)) when any of the conditions are detected. This interrupt is enabled by setting IER[2]=1 in the Interrupt Enable Register.

LSR[5] Transmitter Holding Register Empty (THRE): THRE indicates that the KS82C450/KS82C50A is ready to accept a new character for transmission. The THRE bit is set high when a character is transferred from the Transmitter Holding Register into the Transmitter Shift Register. LSR[5] is reset low when the CPU loads the Transmitter Holding Register. LSR[5] is not reset by a CPU read of the LSR.

When the THRE interrupt is enabled (IER[1]=1), THRE causes a priority 3 interrupt in the IIR. If THRE is the interrupt source indicated in IIR, INTRPT is cleared by a read of the IIR.

LSR[6] Transmitter Empty (TEMT): TEMT is set high when the Transmitter Holding Register (THR) and the Transmitter Shift Register (TSR) are both empty. LSR[6] is reset low when a character is loaded into the THR and remains low until the character is trasferred out of SOUT. TEMT is not reset low by a CPU read of the LSR.

LSR[7]: This bit is permanently set to logic zero.

Table 10 : LSR BIT DEFINITIONS

Bit Number	Function	Logic 1	Logic 0
0	Data Ready (DR)	Ready	Not Ready
1	Overrun Error (OE)	Error	No Error
2	Parity Error (PE)	Error	No Error
3	Framing Error (FE)	Error	No Error
4	Break Interrupt (BI)	Break	No Break
5	Transmitter Holding Register Empty (THRE)	Empty	Not Empty
6	Transmitter Empty (TEMT)	Empty	Not Empty
7	Not Used		

Modem Control Register (MCR)

The MCR controls the interface with the modem or data set as described below. The MCR can be written and read. The RTS, DTR, OUT1 and OUT2 outputs are directly controlled by their control bits in this register. A high input asserts a low (true) at the output pins.

MCR[0]: When MCR[0] is set high, the DTR output is forced low. When MCR[0] is reset low, the DTR output is forced high. The DTR output of the KS82C450/KS82C50A may be input into an EIA inverting line driver as the 1488 to obtain the proper polarity input at the modem or data set.

MCR[1]: When MCR[1] is set high, the RTS output is forced low. When MCR[1] is reset low, the RTS output is forced high. The RTS output of the KS82C450/KS82C50A may be input into an EIA inverting line driver as the 1488 to obtain the proper polarity input at the modem or data set.

MCR[2]: When MCR[2] is set high, the OUT1 output is forced low. When MCR[2] is reset low, the OUT1 output is forced high. OUT1 is a user designated output.

MCR[3]: When MCR[3] is set high, the OUT2 output is forced low. When MCR[3] is reset low, the OUT2 output is forced high. OUT2 is a user designated output.

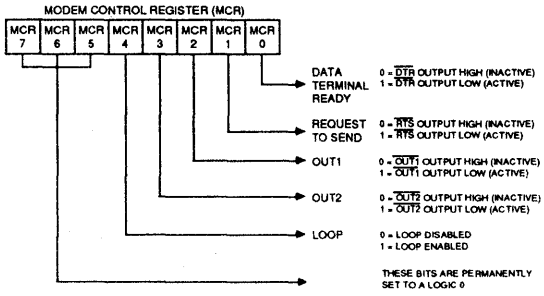


Figure 5 : MODEM CONTROL REGISTER

MCR[4]: MCR[4] provides a local loopback feature for diagnostic testing of the KS82C450/KS82C50A. When MCR[4] is set high. Serial Output (SOUT) is set to the marking (logic one) state, and the receiverr data input Serial Input (SIN) is disconnected. The output of the Transmitter Shift Register is looped back into the Receiver Shift Register input. The four modem control inputs (CTS, DSR, DCD and RI) are disconnected. The four modem control outputs (DTR, RTS, OUT1 and OUT2) are internally connected to the four modem control inputs. The modem control output pins are forced to their inactive state (high). In the diagnostic mode, data transmitted is immediately received. This allows the CPU to verify KS82C450/KS82C50A transmit and receive data paths .

In the diagnostic mode, the receiver and transmitter interrupts are fully operational. The modem control interrupts are also operational, but the interrupt sources are now the lower four bits of the MCR instead of the four modem control inputs. The interrupts are still controlled by the Interrupt Enable Register.

MCR[5] – MCR[7]: Bits are permanently set to logic zero.

Table 11 : MCR BIT DEFINITIONS

Bit Number	Function	Logic 1	Logic 0
0	Data Terminal Ready (DTR)	DTR Output Low	DTR Output High
1	Request to Send (RTS)	RTS Output Low	RTS Output High
2	OUT1	OUT1 Output Low	OUT1 Output High
3	OUT2	OUT2 Output Low	OUT2 Output High
4	LOOP	LOOP Enabled	LOOP Disabled
5	0		
6	0		
7	0		

Modem Status Register (MSR)

The MSR provides the CPU with status of the modem input lines from the modem or peripheral device. The MSR allows the CPU to read the modem signal inputs by accessing the data bus interface of the KS82C450/KS82C50A. In addition to the current status information, four bits of the MSR indicate whether the modem inputs have changed since the last reading of the MSR. The delta status bits are set high when a control input from the modem changes state, and reset low when the CPU reads the MSR.

The modem input lines are CTS (pin 36), DSR (pin 37), RI (pin 39) and DCD (pin 38). MSR[4] – MSR[7] are status indications of these lines. The status indications follow the status of the input lines. If the modem status interrupt in the Interrupt Enable Register is enabled (IER[3]), a change of state in a modem input signals will be reflected by the modem status bits in the IIR register and an interrupt (INTRPT) is generated. The MSR is a priority 4 interrupt. The contents of the Modem Status Register are described in Table 12.

Note that the state (high or low) of the status bits are inverted versions of the actual input pins.

MSR[0] Delta Clear to Send (DCTS): DCTS indicates that the $\overline{CTS}$ input (pin 36) to the KS82C450/KS82C50A has changed state since the last time it was read by the CPU.

MSR[1] Delta Data Set Ready (DDSR): DDSR indicates that the $\overline{DSR}$ input (pin 37) to the KS82C450/KS82C50A has changed state since the last time it was read by the CPU.

MSR[2] Trailing Edge of Ring Indicator (TERI): TERI indicates that the $\overline{RI}$ input (pin 39) to the KS82C450/KS82C50A has changed state (L→H) since the last time it was read by the CPU.

MSR[3] Delta Data Carrier Detect (DDCD): DDCD indicates that the $\overline{DCD}$ input (pin 38) to the KS82C450/KS82C50A has changed state since the last time it was read by the CPU.

MSR[4] Clear to Send (CTS): CTS is the status of the $\overline{CTS}$ input (pin 36) from the modem indicating to the KS82C450/KS82C50A that the modem is ready to receive data from the transmitter output (SOUT). If the KS82C450/KS82C50A is in the loop mode (MCR[4]=1), MSR[4] is equivalent to RTS in the MCR.

MSR[5] Data Set Ready (DSR): DSR is a status of the $\overline{DSR}$ input (pin 37) from the modem to the KS82C450/KS82C50A which indicates that the modem is ready to provide received data to the receiver circuitry. If KS82C450/KS82C50A is in the loop mode (MCR[4]=1), MSR[5] is equivalent to DTR in the MCR.

MSR[6] Ring Indicator (RI): RI indicates the status of the RI input (pin 39). If the KS82C450/KS82C50A is in the loop mode (MCR[4]=1), MSR[6] is equivalent to OUT1 in the MCR.

MSR[7] Data Carrier Detect (DCD): DCD indicates the status of the Data Carrier Detect ($\overline{DCD}$) input (pin 38). If the KS82C450/KS82C50A is in the loop mode (MCR[4]=1), MSR[4] is equivalent to OUT2 of the MCR.

The modem status inputs (RI, DCD, DSR and CTS) reflect the modem input lines with any change of status. Reading the MSR register well clear the delta modem status indications but has no effect on the status bits. The status bits reflect the state of the input pins regardless of the mask control signals. If a DCTS, DDSR, TERI or DDCD are true and a state change occurs during a read operation ($\overline{RD}$,RD), the state change is not indicated in the MSR. If DCTS, DDSR, TERI or DDCD are false and a state change occurs during a read operation, the state change is indicated after the read operation.

For LSR and MSR, the setting of status bits is inhibited during status register read ($\overline{RD}$,RD) operations. If a status condition is generated during a read ($\overline{RD}$,RD) operation, the status bit is not set until the trailing edge of the read ($\overline{RD}$,RD).

If a status bit is set during a read ($\overline{RD}$,RD) operation, and the same status condition occurs, that status bit will be cleared at the trailing edge of the read ($\overline{RD}$,RD) instead of being set again.

Baud Rate Select Register (BRSR)

The KS82C450/KS82C50A contains a programmable Baud Rate Generator (BRG) that divides the clock (DC to 10 MHz) by any divisor from 1 to $2^{16}-1$ (see BRG description). The output frequency of the BRG is 16x the data rate:

Divisor # = Frequency Input ÷ (Baud Rate x 16)

Two 8-bit registers store the divisor in 16-bit binary format. These Divisor Latch registers must be loaded during initialization. On loading either of the Divisor Latches, a 16-bit Baud counter is immediately loaded, preventing long counts on initial load.

Sample Divisor Number Calculation:

Given:	Desired Baud Rate 1200 Baud
	Frequency Input 1.8432 MHz
Formula:	Divisor # = Frequency Input ÷ (Baud Rate x 16)
	Divisor # = 1843200 ÷ (1200 x 16)
Answer:	Divisor # = 96 = 60_{HEX} → DLL = 01100000
	DLM = 00000000
Check:	The Divisor #96 will divide the input frequency 1.8432 MHz down to 19200 which is 16 times the desired baud rate.

Table 12 : MSR BIT DEFINITIONS

Bit Number	Function
0	Delta Clear to Send (DCTS)
1	Delta Data Set Ready (DDSR)
2	Trailing Edge of Ring Indicator (TERI)
3	Delta Data Carrier Detect (DDCD)
4	Clear to Send (CTS)
5	Data Set Ready (DSR)
6	Ring Indicator (RI)
7	Data Carrier Detect (DCD)

Table 13: DIVISOR LATCH BIT DEFINITIONS

Least Significant Bit		Most Significant Bit	
Bit Number	Function	Bit Number	Function
0	DLL[0]	8	DLM[0]
1	DLL[1]	9	DLM[1]
2	DLL[2]	10	DLM[2]
3	DLL[3]	11	DLM[3]
4	DLL[4]	12	DLM[4]
5	DLL[5]	13	DLM[5]
6	DLL[6]	14	DLM[6]
7	DLL[7]	15	DLM[7]

Receiver Buffer Register (RBR)

The receiver circuitry in the KS82C450/KS82C50A is programmable for 5, 6, 7 or 8 data bits per character. For words of less than 8 bits, the data is right justified to the least significant bit (LSB = Data Bit 0, RBR[0]). Data Bit 0 of a data word (RBR[0]) is the first data bit received. The unused bits in a character less than 8 bits are output low to the parallel output by the KS82C450/KS82C50A.

Received data at the SIN input pin is shifted into the Receiver Shift Register by the 16x clock provided at the RCLK input. This clock is synchronized to the incoming data based on the position of the start bit. When a complete character is shifted into the Receiver Shift Register, the assembled data bits are parallel loaded into the Receiver Buffer Register. The DR flag in the LSR register is set.

Double buffering of the received data permits continuous reception of data without losing received data. While the Receiver Shift Register is shifting a new character into the KS82C450/KS82C50A, the Receiver Buffer Register is holding a previously received character for the CPU to read. Failure to read the data in the RBR before complete reception of the next character result in the loss of the data in the Receiver Register. The OE flag in the LSR register indicates the overrun condition.

Transmitter Holding Register (THR)

The Transmitter Holding Register (THR) holds parallel data from the data bus (D0 – D7) until the Transmitter Shift Register is empty and ready to accept a new character for transmission. The transmitter and receiver word length and number stop bits are the same. If the character is less than eight bits, unused bits at the microprocessor data bus are ignored by the transmitter.

Data Bit 0 (THR[0]) is the first serial data bit transmitted. The THRE flag (LSR[5]) reflects the THR status, the TEMT flag (LSR[5]) indicates if both THR and TSR are empty.

Table 14 : RBR BIT DEFINITIONS

Bit Number	Function
0	Data - RBR[0]
1	Data - RBR[1]
2	Data - RBR[2]
3	Data - RBR[3]
4	Data - RBR[4]
5	Data - RBR[5]
6	Data - RBR[6]
7	Data - RBR[7]

Table 15 : THR BIT DEFINITIONS

Bit Number	Function
0	Data - THR[0]
1	Data - THR[1]
2	Data - THR[2]
3	Data - THR[3]
4	Data - THR[4]
5	Data - THR[5]
6	Data - THR[6]
7	Data - THR[7]

Scratchpad Register (SCR)

This 8-bit Read/Write register has no effect on the KS82C450/KS82C50A. It is intended as a scratchpad register to be used by the programmer to hold data temporarily.

Table 16 : SCR BIT DEFINITIONS

Bit Number	Function
0	Data - SCR[0]
1	Data - SCR[1]
2	Data - SCR[2]
3	Data - SCR[3]
4	Data - SCR[4]
5	Data - SCR[5]
6	Data - SCR[6]
7	Data - SCR[7]

INTERRUPT STRUCTURE

Interrupt Identification Register (IIR)

The KS82C450/KS82C50A has interrupt capability for interfacing to current microprocessors. In order to minimize software overhead during data character transfers, the KS82C450/KS82C50A prioritizes interrupts into four levels:

- Receiver Line Status (priority 1)
- Received Data Ready (priority 2)
- Transmitter Holding Register Empty (priority 3)
- Modem Status (priority 4)

Information indicating that a prioritized interrupt is pending and the type of interrupt is stored in the Interrupt Identification Register (IIR). When addressed during chip select time, the IIR indicates the highest priority interrupt pending. No other interrupts are acknowledged until the interrupt is serviced by the CPU. The contents of the IIR are indicated in Table 17 and are described below.

IIR[0]: IIR[0] can be used in either a hardwired prioritized or polled environment to indicate if an interrupt is pending. When IIR[0] is low, an interrupt is pending, and IIR contents may be used as a pointer to the appropriate interrupt service routine. When is high, no interrupt is pending.

IIR[1] and IIR[2]: IIR[1] and IIR[2] are used to identify the highest priority interrupt pending as indicated in Table 17.

IIR[3] – IIR[7]: These five bits of the IIR are logic zero.

Interrupt Enable Register (IER)

The Interrupt Enable Register (IER) is a Write register used to independently enable the four KS82C450/KS82C50A interrupts which activate the interrupt (INTRPT) output. All interrupts are disabled by resetting IER[0] – IER[3] of the Interrupt Enable Register. Interrupts are enabled by setting the appropriate bits of the IER high. Disabling the interrupt system inhibits the Interrupt Identification Register and the active (high) INTRPT output. All other system functions operate in their normal manner, including the setting of the Line Status and Modem Status Registers. The contents of the Interrupt Enable Register are indicated in Table 18 and are described below.

IER[0]: When programmed high (IER[0] = Logic 1), IER[0] enables Received Data Available interrupt.

IER[1]: When programmed high (IER[1] = Logic 1), IER[1] enables the Transmitter Holding Register Empty interrupt.

IER[2]: When programmed high (IER[2] = Logic 1), IER[2] enables the Receiver Line Status interrupt.

IER[3]: Wehn programmed high (IER[3] = Logic 1), IER[3] enables the Modem Status interrupt.

IER[4] – IER[7]: These four bits of the IER are logic zero.

Table 17 : INTERRUPT IDENTIFICATION REGISTER

Interrupt Identification				Interrupt Set and Reset Functions		
Bit 2	Bit 1	Bit 0	Priority Level	Interrupt Flag	Interrupt Source	Interrupt Reset Control
X	X	1		None	None	
1	1	0	First	Receiver Line Status	OE, PE, FE or BI	LSR Read
1	0	0	Second	Received Data Available	Receiver Data Available	RBR Read
0	1	0	Third	THRE	THRE	IIR Read if THRE is interrupt source or THR Write
0	0	0	Fourth	Modem Status	$\overline{CTS}$, $\overline{DSR}$, $\overline{RI}$, $\overline{DCD}$	MSR Read

Note: X - Don't Care

Table 18 : REGISTER SUMMARY

Register Mnemonic	Register Bit Number							
	Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
RBR (Read Only)	Data Bit 7 (MSB)	Data Bit 6	Data Bit 5	Data Bit 4	Data Bit 3	Data Bit 2	Data Bit 1	Data Bit 0 (LSB)[1]
THR (Write Only)	Data Bit 7	Data Bit 6	Data Bit 5	Data Bit 4	Data Bit 3	Data Bit 2	Data Bit 1	Data Bit 0
DLL	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DLM	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
IER	0	0	0	0	EDSSI (Enable Modem Status Interrupt)	ELSI (Enable Receiver Line Status Interrupt)	ETBEI (Enable Transmitter Holding Register Empty Interrupt)	ERBFI (Enable Received Data Available Interrupt)
IIR (Read Only)	0	0	0	0	0	Interrupt ID Bit 1	Interrupt ID Bit 0	'0' - if Interrupt Pending
LCR	DLAB (Divisor Latch Access Bit)	Set Break	Stick Parity	EPS (Even Parity Select)	PEN (Parity Enable)	STB (Number of Stop Bits)	WLSB1 (Word Length Select) Bit 1	WLSB0 (Word Length Select) Bit 0
MCR	0	0	0	LOOP	OUT2	OUT1	RTS (Request to Send)	DTR (Data Terminal Ready)
LSR	0	TEMT (Transmitter Empty)	THRE (Transmitter Holding Register Empty)	BI (Break Interrupt)	FE (Framing Error)	PE (Parity Error)	OE (Overrun Error)	DR (Data Ready)
MSR	DCD (Data Carrier Detect)	RI (Ring Indicator)	DSR (Data Set Ready)	CTS (Clear to Send)	DDCD (Delta Data Carrier Detect)	TERI (Trailing Edge Ring Indicator)	DDSR (Delta Data Set Ready)	DCTS (Delta Clear to Send)
SCR	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

Note: 1. LSB, Data Bit 0 is the first bit transmitted or received

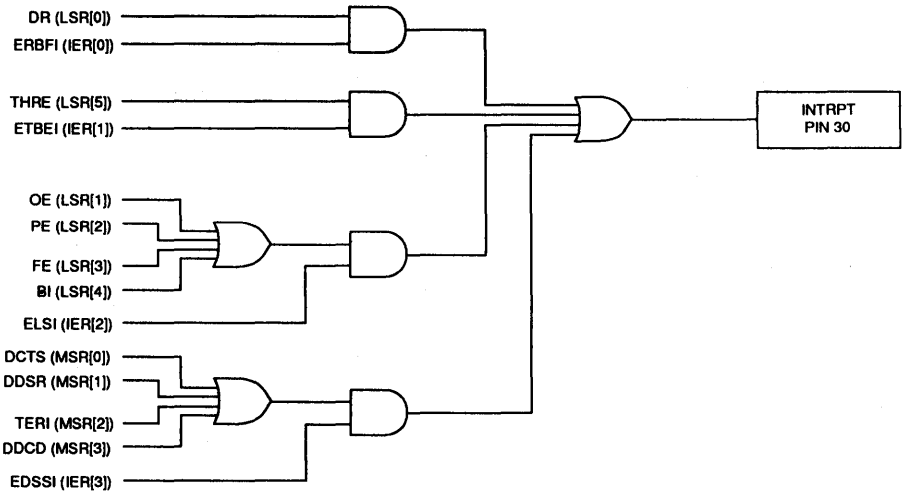


Figure 6: KS82C450/82C50A INTERRUPT CONTROL STRUCTURE

Transmitter

The serial transmitter section consists of a Transmitter Holding Register (THR). Transmitter Shift Register (TSR) and associated control logic. The Transmitter Holding Register Empty (THRE) and Transmitter Shift Register Empty (TEMT) are two bits in the Line Status Register which indicate the status of THR and TSR. To transmit a 5 - 8 bit word, the word is written through D0 - D7 to the THR. The microprocessor should perform a write operation only if THRE is high. The THRE is set high when the word is automatically transferred from the THR to the TSR during the transmission of the start bit.

When the transmitter is idle, both THRE and TEMT are high. The first word written causes THRE to be reset to zero. After completion of the transfer, THRE returns high. TEMT remains low for at least the duration of the transmission of the data word. If a second character is transmitted to the THR, the THRE is reset low. Since the data word cannot be transferred from the THR to the TSR until the TSR is empty, THRE remains low until the TSR has completed transmission of the word. When the last word has been transmitted out of the TSR, TEMT is set high. THRE is set high one THR to TSR transfer time later.

Receiver

Serial asynchronous data is input into the SIN pin. The idle state of the line providing the input into SIN is high. A start bit detect circuit continually searches for a H → L transition from the idle state. When a transition is detected, a counter is reset, and counts the 16x clock to $7^1/_2$, which is the center of the start bit. The start bit is valid if the SIN is still low at the mid bit sample of the start bit. The start bit is verified to prevent the receiver from assembling an incorrect data character due to a low going noise spike on the SIN input.

The Line Control Register determines the number of data bits in a character (LCR[0], LCR[1]), number of stop bits LCR[2], if parity is used LCR[3], and the polarity of parity LCR[4]. Status information for the receiver is provided in the Line Status Register. When a character is transferred from the Receiver Shift Register to the Receiver Buffer Register, the Data Received indication in LSR[0] is set high. The CPU reads the Receiver Buffer Register through D0 - D7. Thes read resets LSR[0]. If D0 - D7 are not read prior to a new character transfer from the RSR to RBR, the overrun error status indication is set in LSR[1]. The parity check tests for even or odd parity on the parity bit, which precedes the first stop bit. If there is a parity error, the parity error is set in LSR[2]. There is circuitry which tests whether the stop bit is high. If it is not, a framing error indication is generated in LSR[3].

The center of the start bit is defined as clock count $7^1/_2$. If data into the SIN is a symmetrical square wave, the data cell centers will occur within ±3.125% of the actual center, giving an error margin of 46.875%. The start bit can begin as much as one 16x clock cycle prior to being detected.

Baud Rate Generator (BRG)

The BRG generates the clocking for the UART function, at standard ANSI/CCITT bit rates. The oscillator driving the BRG may be provided with an external crystal to the XTAL1 and XTAL2 pins, or an external clock into XTAL1. In either case, a buffered clock output, BAUDOUT is provided for other system clocking. If two KS82C450/KS82C50As are used on the same board, one can use a crystal, with the buffered clock output routed directly to XTAL1 of the other KS82C450/KS82C50A.

The data rate is determined by the Divisor Latch registers DLL and DLM and the external frequency or crystal input, with the BAUDOUT providing an output 16x the data rate. The bit rate is selected by programming the two divisor latches, Divisor Latch Most Significant Byte and Divisor Latch Least Significant Byte. Setting DLL=1 and DLM=0 selects the divisor to divide by 1 (divide by 1 gives maximum baud rate for a given input frequency at XTAL1). The on-chip oscillator is optimized for a 10MHz crystal.

The BRG can use any of three different popular crystals to provide standard baud rates. The frequency of these three common crystals on the market are 1.8432MHz, 2.4576MHz and 3.072MHz. With these standard crystals, standard bit rates from 50 to 38.5 kbps are available. The following tables illustrate the divisors needed to obtain standard rates using these three crystal frequencies.

Table 19 : BAUD RATES WITH 1.8432 MHZ CRYSTAL

Desired Baud Rate	Divisor Used to Generate 16 x Clock	Percentage Error Difference Between Desired and Actual
50	2304	-
75	1536	-
110	1047	0.026
134.5	857	0.058
150	768	-
300	384	-
600	192	-
1200	96	-
1800	64	-
2000	58	0.69
2400	48	-
3600	32	-
4800	24	-
7200	16	-
9600	12	-
19200	6	-
38400	3	-
56000	2	2.86

Table 20 : BAUD RATES WITH 2.4576 MHZ CRYSTAL

Desired Baud Rate	Divisor Used to Generate 16 x Clock	Percentage Error Difference Between Desired and Actual
50	3072	-
75	2048	-
110	1396	0.026
134.5	1142	0.0007
150	1024	-
300	512	-
600	256	-
1200	128	-
1800	85	0.392
2000	77	0.260
2400	64	-
3600	43	0.775
4800	32	-
7200	21	1.587
9600	16	-
19200	8	-
38400	4	-

Table 21 : BAUD RATES WITH 3.072 MHZ CRYSTAL

Desired Baud Rate	Divisor Used to Generate 16 x Clock	Percentage Error Difference Between Desired and Actual
50	3840	-
75	2560	-
110	1745	0.026
134.5	1428	0.034
150	1280	-
300	640	-
600	320	-
1200	160	-
1800	107	0.312
2000	96	-
2400	80	-
3600	53	0.628
4800	40	-
7200	27	1.23
9600	20	-
19200	10	-
38400	5	-

Reset

After powerup, the KS82C450/KS82C50A Master Reset schmitt trigger input (MR) should be held high for TMRW ns to reset the KS82C450/KS82C50A circuits to an idle mode unitl initialization. A high on MR causes the following:

- Initializes the transmitter and receiver internal clock counters.
- Clears the Line Status Register (LSR), except for Transmitter Shift Register Empty (TEMT) and Transmit Holding Register Empty (THRE), which are set. The Modem Control Register (MCR) and Line Control Register (LCR) are also cleared. All of the discrete lines, memory elements and miscellaneous logic associated with these register bits are also cleared or turned off. The Divisor Latches, Receiver Buffer Register, Transmitter Buffer Register are not effected.

Following removal of the reset condition (MR low), the KS82C450/KS82C50A remains in the idle mode until programmed.

A hardware reset of the KS82C450/KS82C50A sets the THRE and TEMT status bit in the LSR. When interrupts are subsequently enabled, an interrupt occurs due to THRE.

A summary of the effect of a Master Reset on the KS82C450/KS82C50A is given in Table 22.

Table 22 : RESET OPERATIONS

Register/Signal	Reset Control	Reset
Interrupt Enable Register	Master Reset	All Bits Low (0-3 forced, 4-7 permanent)
Interrupt Identification Register	Master Reset	Bit 0 is High, Bits 1 and 2 Low Bits 3-7 Permanently Low
Line Control Register	Master Reset	All Bits Low
MODEM Control Register	Master Reset	All Bits Low
Line Status Register	Master Reset	Bits 5 and 6 High, all other Bits Low
MODEM Status Register	Master Reset	Bits 0-3 Low, Bits 4-7 Input Signal
SOUT	Master Reset	High
Interrupt (RCVR Errors)	Read LSR/MR	Low
Interrupt (RCVR Data Ready)	Read RBR/MR	Low
Interrupt (THRE)	Read IIR, Write THR/MR	Low
Interrupt (Modem Status Changes)	Read MSR/MR	Low
$\overline{OUT2}$	Master Reset	High
$\overline{RTS}$	Master Reset	High
$\overline{DTR}$	Master Reset	High
$\overline{OUT1}$	Master Reset	High

PROGRAMMING

The KS82C450/KS82C50A is programmed by the control registers LCR, IER, DLL, DLM and MCR. These control words define the character length, number of stop bits, parity, baud rate and modem interface.

While the Control registers can be written in any order, the IER should be written to last because it controls the interrupt enables. Once the KS82C450/KS82C50A is programmed and operational, these registers can be updated any time the KS82C450/KS82C50A is not transmitting or receiving data.

The control signals required to access KS82C450/KS82C50A internal registers are shown below.

Software Reset

A software reset of the KS82C450/KS82C50A is a useful method for returning to a completely known state without a system reset. Such a reset consists of writing to the LCR, Divisor Latches and MCR registers. The LSR and RBR registers should be read prior to enabling interrupts in order to clear out any residual data or status bits which may be invalid for subsequent operation.

Crystal Operation

The KS82C450/KS82C50A crystal oscillator circuitry is designed to operate with a fundamental mode, parallel resonant crystal. Table 23 shows the required crystal parameters and crystal circuit configuration, respectively.

When using an external clock source, the XTAL1 input is driven and the XTAL2 output is left open. Power consumption when using an external clock is typically 50% of that required when using a crystal. This is due to the sinusoidal nature of the drive circuitry when using a crystal.

The maximum frequency of the KS82C450/KS82C50A is 10 MHz with an external clock or a crystal attached to XTAL1 and XTAL2. Using the external clock or crystal, and a divide by one divisor, the maximum BAUDOUT is 10 MHz and the maximum data rate is 625 kbps.

Table 23 : TYPICAL CRYSTAL OSCILLATOR CIRCUIT

Parameter	
Frequency	1.0 to 10 MHz
Type of Operation	Parallel resonant, Fundamental mode
Load Capacitance (C_L)	20 or 32 pF (typical)
R_{SERIES} (Max)	100 (f = 10 MHz, C_L = 32 pF) 200 (f = 10 MHz, C_L = 20 pF)

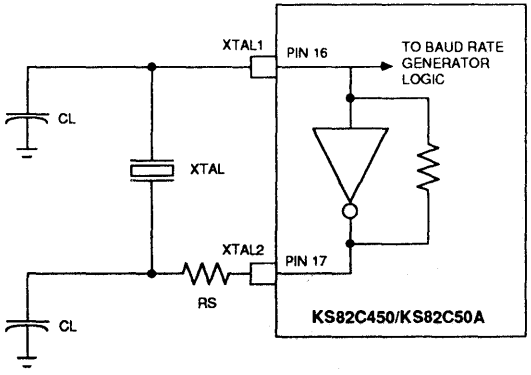


Figure 7 : CRYSTAL OSCILLATOR CIRCUIT

PACKAGE DIMENSIONS

Units: Inches

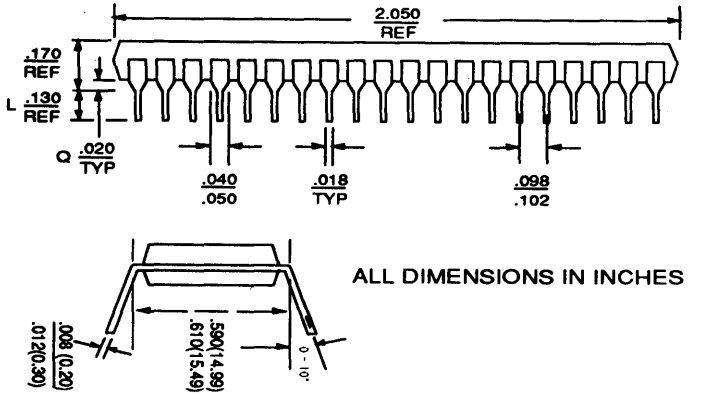


Figure 8 : PLASTIC PACKAGING

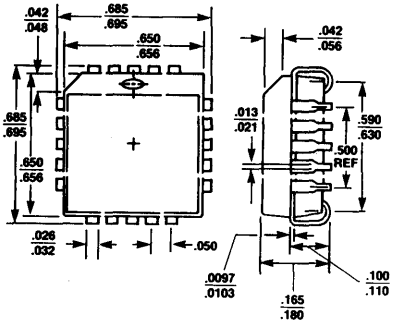
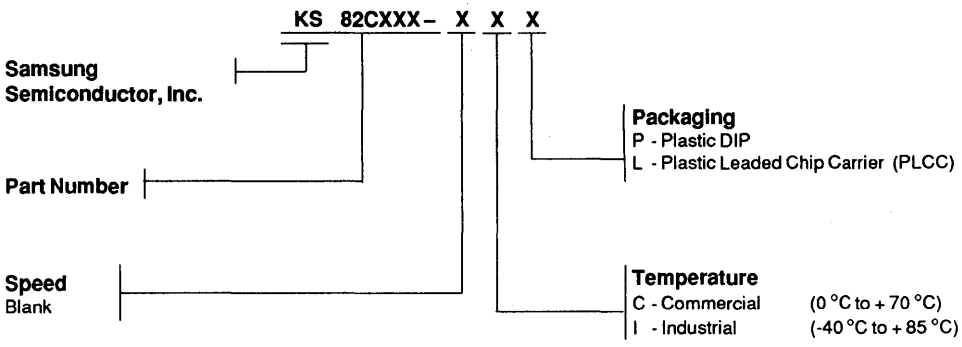


Figure 9 : PLCC PACKAGING

ORDERING INFORMATION and PRODUCT CODE



Samsung Semiconductor products are designated by a Product Code. When ordering, refer to products by their full code. For unusual, and/or specific packaging or processing requirements not covered by the standard product line, please contact the *Samsung Microprocessor Peripherals Product Group.*

FEATURES

- **Pin and functional compatibility with the industry standard 8252**
- **TTL input/output compatibility**
- **Low power CMOS implementation**
- **High speed - DC to 16 MHz operation**
- **Single chip UART/BRG**
- **Crystal or external clock input**
- **On chip baud rate generator featuring 72 selectable baud rates**
- **Interrupt mode with mask capability**
- **Microprocessor bus oriented interface**
- **Line break generation and detection**
- **Loopback and echo modes**
- **Fully static operation**

DESCRIPTION

The KS82C52 is a high performance, single chip programmable Universal Asynchronous Receiver/Transmitter (UART) and Baud Rate Generator (BRG). The Baud Rate Generator can be programmed for one of 72 different baud rates using a single industry standard crystal or external frequency source. A programmable buffered clock output is available and can be programmed to provide either a buffered oscillator or 16X baud rate clock for general purpose system usage.

The KS82C52 features full TTL/CMOS compatibility, allowing it to be designed into mixed TTL/NMOS/CMOS system environments. Its high speed and high performance make it ideally suited for aerospace and defense applications, while a very low power consumption suits it to portable systems and systems with low power standby modes.

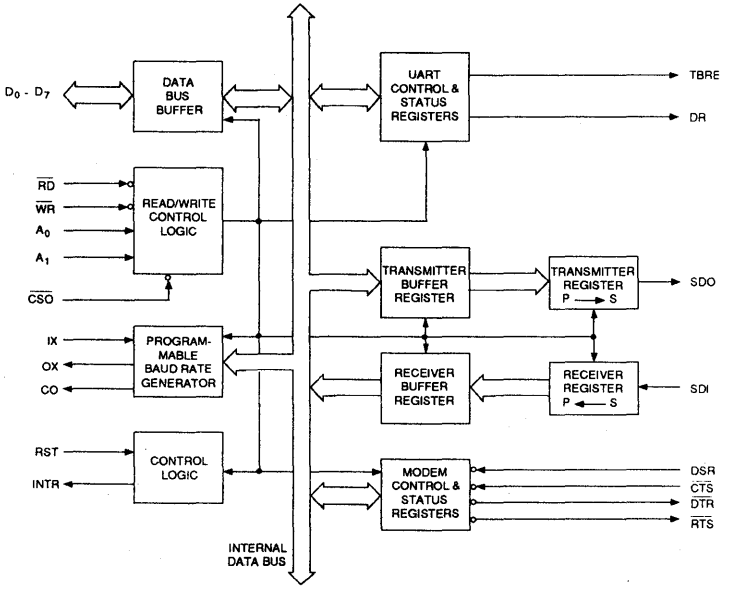


Figure 1 : KS82C52 BLOCK DIAGRAM

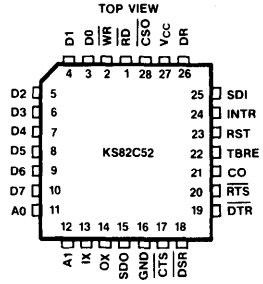


Figure 2 a: PLCC CONFIGURATION

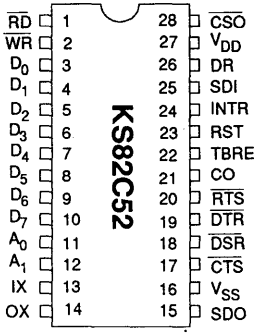


Figure 2 b: 28-PIN DIP CONFIGURATION

Table 1 : PIN DESCRIPTIONS

Symbol	Pin(s) 28-Pin DIP	Type	Name and Function
A_0, A_1	11, 12	I	**Address Inputs:** The address lines select the various internal registers during CPU bus operations.
CO	21	O	**Clock Out:** This output is user programmable to provide either a buffered IX output or a buffered Baud Rate Generator (16x) clock output. The buffered IX (Crystal or external clock source) output is provided when the Baud Rate Select Register (BRSR) bit 7 is set to a zero. Writing a logic one to BRSR bit 7 causes the CO output to provide a buffered version of the internal Baud Rate Generator clock which operates at sixteen times the programmed baud rate.
$\overline{CSO}$	28	I	**Chip Select:** The chip select input acts as an enable signals for the $\overline{RD}$ and $\overline{WR}$ input signals.
$\overline{CTS}$	17	I	**Clear to Send:** The logical state of the $\overline{CTS}$ line is reflected in the $\overline{CTS}$ bit of the Modem Status Register. Any change of state in $\overline{CTS}$ causes INTR to be set true when INTEN and MIEN are true. A false level on $\overline{CTS}$ will inhibit transmission of data on the SDO output and will hold SDO in the Mark (high) state. If $\overline{CTS}$ goes false during transmission, the current character being transmitted will be completed. $\overline{CTS}$ does not affect Loop Mode operation.
D_0 - D_7	3 - 10	I/0	**Data Bits 0 - 7:** The Data Bus provides eight, 3-state input/output lines for the transfer of data, control and status information between the KS82C52 and the CPU. For character formats of less than 8 bits, the corresponding D_7, D_6 and D_5 are considered *don't cares* for data *write* operations and are 0 for data *read* operations. These lines are normally in a high impedance state except during read operations. D_0 is the Least Significant Bit (LSB) and is the first serial data bit to be received or transmitted.
DR	26	O	**Data Ready:** A true level indicates that a character has been received, transferred to the RBR and is ready for transfer to the CPU. DR is reset on a data READ of the Receiver Buffer Register (RBR) or when RST is true.
$\overline{DSR}$	18	I	**Data Set Ready:** The logical state of the $\overline{DSR}$ line is reflected in the Modem Status Register. Any change of state of $\overline{DSR}$ will cause INTR to be set if INTEN and MIEN are true. The state of this signal does not affect any other circuitry within the KS82C52.
$\overline{DTR}$	19	O	**Data Terminal Ready:** The $\overline{DTR}$ signal can be set *low* by writing a logic 1 to the appropriate bit in the Modem Control Register (MCR). This signal is cleared *high* by writing a logic 0 to the $\overline{DTR}$ bit in the MCR or whenever a RST (high) is applied to the KS82C52.
INTR	24	O	**Interrupt Request:** The INTR output is enabled by the INTEN bit in the Modem Control Register (MCR). The MIEN bit selectively enables modem status changes to provide an input to the INTR logic. Figure 15 shows the overall relationship of these interrupt control signals.
IX, OX	13, 14	I/O	**Crystal/Clock:** Crystal connections for the internal Baud Rate Generator. IX can also be used as an external clock input in which case OX should be left open.
$\overline{RD}$	1	I	**Read:** The $\overline{RD}$ input causes the KS82C52 to output data to the data bus (D_0 - D_7). The data output depends upon the state of the address inputs (A_0, A_1). $\overline{CSO}$ enables the RD input.
RST	23	I	**Reset:** The RST input forces the KS82C52 into an *Idle* mode in which a serial data activities are suspended. The Modem Control Register (MCR) along with its associated outputs are cleared. The UART Status Register (USR) is cleared except for the TBRE and TC bits, which are set. The KS82C52 remains in an *Idle* state until programmed to resume serial data activities. The RST input is a Schmitt trigger input.
$\overline{RTS}$	20	O	**Request to Send:** The $\overline{RTS}$ signal can be set *low* by writing a logic 1 to the appropriate bit in the MCR. This signal is cleared *high* by writing a logic 0 to the $\overline{RTS}$ bit in the MCR or whenever a reset RST (high) is applied to the KS82C52.

Table 1 : PIN DESCRIPTIONS con't

Symbol	Pin(s) 28-Pin DIP	Type	Name and Function
SDI	25	I	**Serial Data Input:** Serial data input to the KS82C52 receiver circuits. A Mark (1) is high, and a Space (0) is *low*. Data inputs on SDI are disabled when operating in the loop mode or when RST is true.
SDO	15	O	**Serial Data Output:** Serial data output from the KS82C52 transmitter circuitry. A Mark (1) is a logic one (*high*) and Space (0) is a logic zero (*low*). SDO is held in the Mark condition when the transmitter is disabled, when $\overline{CTS}$ is false, RST is true, when the Transmitter Register is empty, or when in the Loop Mode.
TBRE	22	O	**Transmitter Buffer Register Empty:** The TBRE output is set *high* whenever the Transmitter Buffer Register (TBR) has transferred its data to the Transmitter Register. Application of a reset (RST) to the KS82C52 will also set the TBRE output. TBRE is cleared *low* whenever data is written to the TBR.
V_{CC}	27		**Power:** 5V ± 10% DC Supply

FUNCTIONAL DESCRIPTION

The KS82C52 UART contains a programmable baud rate generator that provides clocking for the transmitter and receiver circuits. The clock output, CO, is a buffered version of either the clock input (IX) to the device or a clock rate that is 16 x the actual baud rate generated.

The transmitter is used for sending serial data out through the SDO pin. The Transmitter Buffer Register accepts 5- to 8-bit wide parallel data from the data bus and transfers it to the Transmitter Register which then shifts the data out serially through the SDO pin. This form of double buffering technique allows continuous data flow transmission.

The receiver accepts serial data via the SDI pin and converts it to parallel form for the system CPU to read. Data is received serially into the Receiver Shift Register from the SDI pin, then sent to the Receiver Buffer Register for access by the CPU. The receiver also detects parity errors, overrun errors, frame errors and break characters.

The Modem Control and Status block provides the means for communicating with the modem or data set. The Modem Control Register is used to select one of four modes of communication: normal mode, loop mode, echo mode and transmit break. The Modem Control Register defines which interrupts will be enabled and will also set the modem control output lines, $\overline{RTS}$ and $\overline{DTR}$. The Modem Status Register keeps track of any changes in the modem control inputs lines, $\overline{CTS}$ and $\overline{DSR}$, as well as allowing the CPU to read their inputs.

The format of the data character being transmitted (eg: number of data bits, parity control and the number of stop bits) is controlled by the UART Control Register. Changes in the status of the device at any given time is reflected in the UART Status Register.

Operating Modes

Normal Mode: Configures the KS82C52 for normal full or half-duplex communications. Data will not be looped back in any form between the serial data input pin and the serial data output pin (see Figure 3a).

Transmit Break: This mode of operation causes the transmitter to transmit break characters only. A break character is composed of all logical zeros for the start, data, parity and stop bits.

Echo Mode: When selected, echo mode causes the KS82C52 to re-transmit data received on the SDI pin out to the SDO pin. In this mode of operation, any data written to the Transmitter Buffer Register will not be sent out on the SDO pin (Figure 3b).

Loop Test Mode: This mode internally re-directs data that would normally be transmitted back to the receiver circuitry. The transmitted data will not appear at the SDO pin. Aiso, data that is received on the SDI pin will be ignored by the device. This mode of operation is useful for performing self test(s) on the device (Figure 3c).

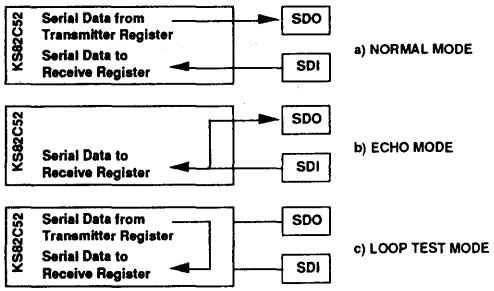


Figure 3 : OPERATING MODES

Table 2 : RECOMMENDED OPERATING CONDITIONS

Operating Voltage Range		+4 V to +7 V
Operating Temperature Range	Commercial	0 °C to +70 °C

Table 3 : ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage (V_{CC})	+8.0 V
Input (V_{IN}) or I/O Voltage Applied	V_{SS} - 0.5 V to V_{DD} + 0.5 V
Output (V_{OUT}) Voltage Applied	V_{SS} - 0.5 V to V_{DD} + 0.5 V
Maximum Power Dissipation	1 Watt
Storage Temperature	-65 °C to +150 °C

Stresses beyond those listed above may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 4 : DC CHARACTERISTICS (T_A = 0 to 70 °C, V_{CC} = 5V ± 10%, V_{SS} = 0V)

Symbol	Parameter	Test Conditions	Limits		Units
			Min	Max	
I_{DD}	Operating Power Supply Current	External Clock F = 2.45576 MHz V_{DD} = 5.5 V, V_{IN} = V_{DD} or V_{SS} Outputs Open		3	mA
I_{IL}	Input Leakage Current	V_{IN} = V_{DD} or V_{SS} on input pins	- 1.0	+1.0	µA
I_{OL}	I/O Leakage Current	V_{OUT} = V_{DD} or V_{SS} on 3-state pins	-10.0	+10.0	µA
V_{IH}	Input HIGH Voltage		2.0		V
V_{IH} (CLK)	Input HIGH Voltage Clock	External Clock	V_{DD} - 0.5		V
V_{IL}	Input LOW Voltage			0.8	V
V_{IL} (CLK)	Input LOW Voltage Clock	External Clock		V_{SS} + 0.5	V
V_{OH}	Output HIGH Voltage	I_{OH} = -2.5 mA	3.0		V
		I_{OH} = -100 µA	V_{DD} - 0.4		
V_{OL}	Output LOW Voltage	I_{OL} = +2.5 mA		0.4	V
V_{TH}	Schmitt Trigger Input HIGH Voltage	Reset Input	V_{DD} - 0.5		V
V_{TL}	Schmitt Trigger Input LOW Voltage	Reset Input		V_{SS} + 0.5	V

I_{DD} is typically ≤ 1 ma/MHz

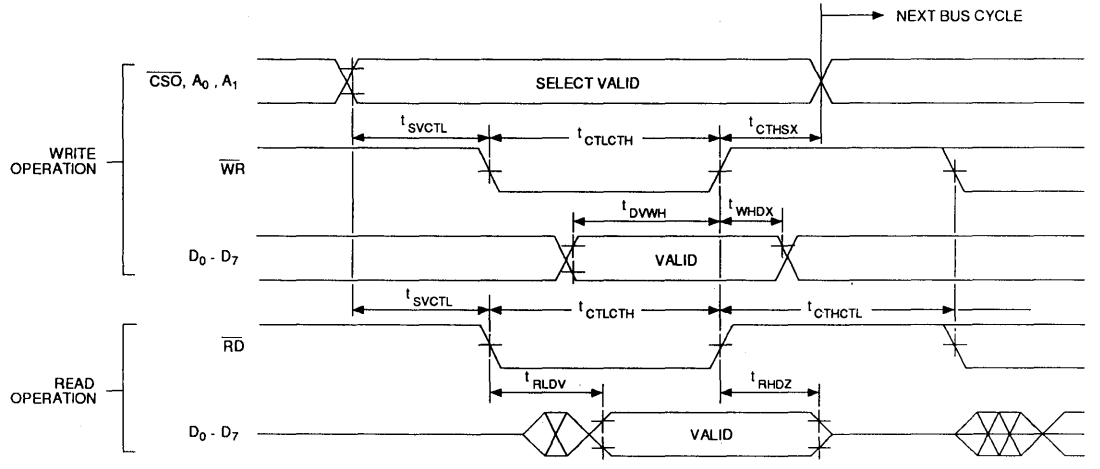
Table 5 : AC CHARACTERISTICS (T_A = 0 to 70 °C, V_{DD} = 5V ± 10%, V_{SS} = 0V)

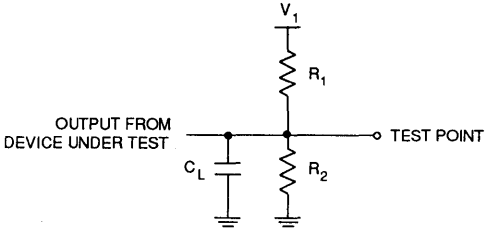
Symbol	Parameter	Test Conditions	Limits (16 MHz)		Units
			Min	Max	
FC	Clock Frequency	$t_{CHCL} + t_{CLCH}$ must be ≥ 62.5 ns	0	16	MHz
t_{CHCL}	Clock High Time		25		ns
t_{CLCH}	Clock Low Time		25		ns
t_{CTHCTL}	Control Disable to Control Enable		100		ns
t_{CTHSX}	Select Hold From Control Trailing Edge		50		ns
t_{CTLCTH}	Control Pulse Width	Control Consists of $\overline{RD}$ or $\overline{WR}$	150		ns
t_{DVWH}	Data Setup Time		50		ns
t_{FCO}	Clock Output Fall Time	C_L = 50 pf		15	ns
t_{RCO}	Clock Output Rise Time	C_L = 50 pf		15	ns
t_{RHDZ}	Read Disable	2	0	60	ns
t_{RLDV}	Read Low to Data Valid	1		120	ns
T_R/T_F	IX Input Rise/Fall Time (External Clock)	tx ≤ 1/6FC or 50 ns, whichever is smaller		tx	ns
t_{SVCTL}	Select Setup to Control Leading Edge		30		ns
t_{WHDX}	Data Hold Time		20		ns

Table 6 : CAPACITANCE (T_A = 0 to 70 °C, V_{DD} = 5V ± 10%, V_{SS} = 0V)

Symbol	Parameter	Test Conditions	Limits		Units
			Min	Max	
C_{IN}	Input Capacitance	Freq = 1 MHz		10	pF
$C_{I/O}$	I/O Capacitance	Unmeasured pins are		20	pF
C_{OUT}	Output Capacitance	returned to V_{SS} (GND)		15	pF

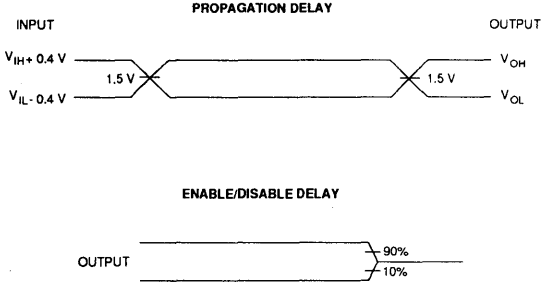
Figure 4 : BUS OPERATION TIMING DIAGRAM





	TEST CONDITION	V_1	R_1	R_2	C_L
1	Propagation Delay	1.7 V	520	∞	100 pF
2	Disable Delay	V_{DD}	5 K	5 K	50 pF

Figure 5 : AC TEST CIRCUITS



A.C. Testing: All input signals must switch between V_{IL} 0.4 V and V_{IH} + 0.4 V TR and TF must be ≤ 15 ns.

Figure 6 : AC TESTING I/O WAVEFORM

PROGRAMMING INSTRUCTIONS

Reset

During and after power-up, the KS82C52 Reset input (RST) should be held high for at least two IX clock cycles in order to initialize and drive the KS82C52 circuits to an idle mode until proper programming can be done. A high on RST causes the following events to occur:

- Resets the internal Baud Rate Generator (BRG) circuits, clock counters and bit counters. The Baud Rate Select Register (BRSR) is not affected.
- Clears the UART Status Register (USR) except for Transmission Complete (TC) and Transmit Buffer Register Empty (TBRE) which are set. The Modem Control Register (MCR) is also cleared. All of the discrete lines, memory elements and miscellaneous logic associated with these register bits are also cleared or turned off. Note that the UART Control Register (UCR) is not affected.

Following removal of the reset condition (RST = low), the KS82C52 remains in the idle mode until programmed to its desired system configuration.

Control Words

The complete functional definition of the KS82C52 is programmed by the systems software. A set of control words (UCR, BRSR and MCR) must be sent out by the CPU to initialize the KS82C52 to support the desired communication format. These control words will program the character length, number of stop bits, even/odd/no parity, baud rate etc. Once programmed, the KS82C52 is ready to perform its communication functions.

The control registers can be written to in any order. However, the MCR should be written to last because it controls the interrupt enables, modem control outputs and the receiver enable bit. Once the KS82C52 is programmed and operational, these registers can be updated any time the KS82C52 is not immediately transmitting or receiving data.

Table 7 : CONTROL SIGNALS

$\overline{CSO}$	A_1	A_0	$\overline{WR}$	$\overline{RD}$	Operation
0	0	0	0	1	Data Bus⇒Transmitter Buffer Register (TBR)
0	0	0	1	0	Receiver Buffer Register (RBR)⇒Data Bus
0	0	1	0	1	Data Bus⇒UART Control Register (UCR)
0	0	1	1	0	UART Status Register⇒Data Bus
0	1	0	0	1	Data Bus⇒ Modem Control Register (MCR)
0	1	0	1	0	Modem Control Register (MCR)⇒Data Bus
0	1	1	0	1	Data Bus⇒Bit Rate Select Register (BRSR)
0	1	1	1	0	Modem Status Register (MSR) ⇒Data Bus

Table 7 shows the control signals required to access the KS82C52 internal registers.

UART Control Register (UCR)

The UCR is a write only register which configures the UART transmitter and receiver circuits. Data bits D_7 and D_6 are not used but should always be set to a logic zero (0) in order to ensure software compatibility with future product upgrades. During the Echo Mode, the transmitter always repeats the received word and parity, even when the UCR is programmed with different or no parity.

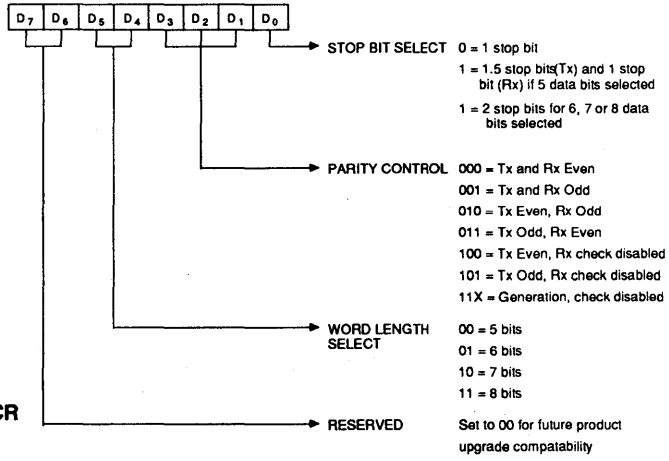


Figure 7 : UCR

Baud Rate Select Register (BRSR)

The KS82C52 is designed to operate with a single crystal or external clock driving the IX input pin. The Baud Rate Select Register is used to select the divide ratio (one of 72) for the internal Baud Rate Generator circuitry. The internal circuitry is separated into two separate counters, a Prescaler and a Divisor Select. The Prescaler can be set to any one of four division rates: ÷ 1, ÷ 3, ÷ 4 or ÷ 5.

The prescaler design has been optimized to provide standard baud rates using any one of three popular crystals. Using one of these system clock frequencies: 1.8432 MHz, 2.4576 MHz or 3.072 MHz and Prescaler divide ratios of ÷ 3, ÷ 4, or ÷ 5 respectively, the Prescaler output will provide a constant 614.4 KHz. When this frequency is further divided by the Divisor Select counter, any of the standard baud rates from 50 Baud to 38.4 KBaud can be selected (Table 8). Non-standard baud rates up to 1 Mbaud can be selected using different input frequencies (crystal or external frequency input up to 16 MHz) and/or different Prescaler and Divisor Select ratios.

Regardless of the baud rate, the baud rate generator provides a clock which is 16 times the desired baud rate. For example, in order to operate at a 1 Mbaud data rate, a 16 MHz crystal, a Prescale rate of ÷ 1, and a Divisor Select rate of *external is* used. This provides a 16 MHz clock as the output of the Baud Rate Generator to the Transmitter and Receiver circuits.

The CO select bit in the BRSR determines if the buffered version of the external frequency input (IX input) or the Baud Rate Generator output (16x baud rate clock) is output on the CO output. The Baud Rate Generator output is always a 50% nominal duty cycle except when *external* is selected and the Prescaler is set to ÷ 3 or ÷ 5.

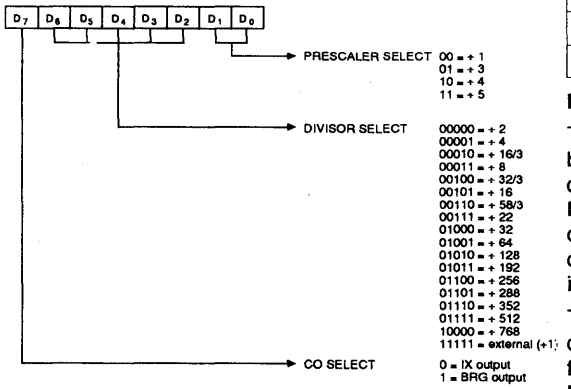


Figure 8 : BRSR

Table 8 : BAUD RATE DIVISORS

Baud Rate	Divisor
38.4 K	external
19.2 K	2
9600	4
7200	16/3
4800	8
3600	32/3
2400	16
2000	58/3
1800	22
1200	32
600	64
300	128
200	192
150	256
134.5*	288
110*	352
75	512
50	768

Note: These baud rates are based upon the following input frequency/Prescale divisor combinations:

1.8432 MHz and Prescale = ÷ 3
2.4576 MHz and Prescale = ÷ 4
3.072 MHz and Prescale = ÷ 5

*All baud rates are exact except for those in Table 9.

Table 9 : BAUD RATE % ERROR

Baud Rate	Actual	Percent Error
2000	1986.2	0.69%
134.5	133.33	0.87%
110	109.71	0.26%

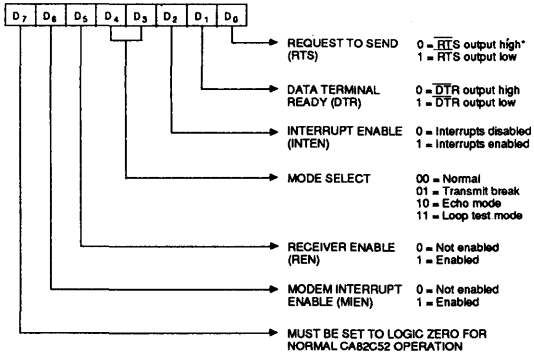
Modem Control Register

The MCR is a general purpose control register which can be written to and read from. The RTS and DTR outputs are directly controlled by their associated bits in this register. Note that a logic one asserts a true logic level (low) at these output pins. The Interrupt Enable (INTEN) bit is the overall control for the INTR output pin. When INTEN is false, INTR is held false (low).

The Operating Mode bits configure the KS82C52 into one of four possible modes. "Normal" configures the KS82C52 for normal full or half duplex communications. "Transmit Break" enables the transmitter to only transmit break

characters (Start, Data and Stop bits are all logic zero). The Echo Mode causes any data that is received on the SDI input pin to be re-transmitted on the SDO output pin. Note that this output is a buffered version of the data seen on the SDI input and is not a resychronized output. Also note that normal UART transmission via the Transmitter Register is disabled when operating in the Echo mode (Figure 10). The Loop Test Mode internally routes transmitted data to the receiver circuitry for the purpose of self test. The transmit data is disabled from the SDO output pin. The Receiver Enable (REN) bit gates off the input to the receiver circuitry when in the false state.

Modem Interrupt Enable will permit any change in modem status line inputs (CTS, DSR) to cause an interrupt when this bit is enabled. Bit D_7 must always be written to with a logic zero to ensure correct KS82C52 operation.



* See Modem Status Register description for a description of register flag images with respect to output pins.

Figure 9 : MCR

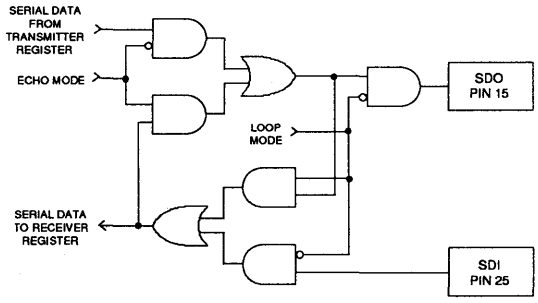


Figure 10 : LOOP AND ECHO MODE FUNCTIONALITY

UART Status Register (USR)

The USR provides a single register that the controlling system can examine to determine if errors have occurred or if other status changes in the KS82C52 require attention. For this reason, the USR is usually the first register read by the CPU to determine the cause of an interrupt or to poll the status of the KS82C52.

Three error flags OE, FE and PE report the status of any error conditions detected in the receiver circuitry. These error flags are updated with every character received during reception of the stop bits. The Overrun Error (OE) indicates that a character in the Receiver Register has been received and cannot be transferred to the Receiver Buffer Register (RBR) because the RBR was not read by the CPU. Framing Error (FE) indicates that the last character received contained improper stop bits. This could be caused by the absence of the required stop bit(s) or by a stop bit(s) that was too short to be properly detected. Parity Error (PE) indicates that the last character received contained a parity error based on the programmed parity of the receiver and the calculated parity of the received character data and parity bits.

The Received Break (RBRK) status bit indicates that the last character received was a break character. A break character would be considered to be an invalid data character in that the entire character including parity and stop bits are a logic zero.

The Modem Status bit is set whenever a transition is detected on any of the modem input lines (CTS or DSR). A subsequent read of the Modem Status Register will show the state of these two signals. Assertion of this bit will cause an interrupt (INTR) to be generated if the MIEN and INTEN bits in the MCR register are enabled.

The Transmission Complete (TC) bit indicates that both the TBR and Transmitter Registers are empty and the KS82C52 has completed transmission of the last character it was commanded to transmit. The assertion of this bit will cause an interrupt (INTR) if the INTEN bit in the MCR register is true.

The Transmitter Buffer Register Empty (TBRE) bit indicates that the TBR register is empty and ready to receive another character.

The Data Ready (DR) bit indicates that the RBR has been loaded with a received character (including Break) and that the CPU may access this data.

Assertion of the TBRE or DR bits do not affect the INTR logic and associated INTR output pin since the KS82C52 has been designed to provide separate requests via the DR and TBRE output pins. If a single interrupt for any status change in the KS82C52 is desired this can be accomplished by "ORing" DR, TBRE and INTR together.

Reading the USR clears all of the status bits in the USR register but does not affect associated output pins.

Modem Status Register (MSR)

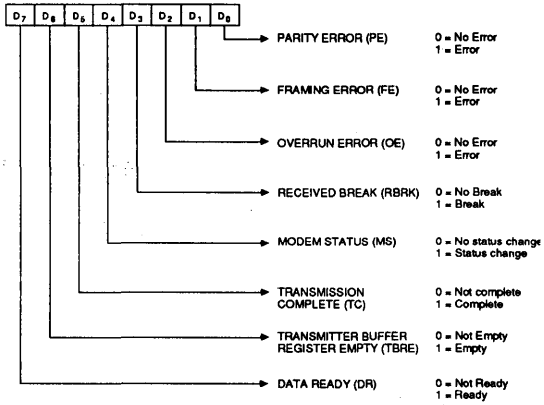


Figure 11 : USR

The MSR allows the CPU to read the modem signal inputs by accessing the data bus interface of the KS82C52. Like all of the register images of external pins in the KS82C52, true logic levels are represented by a high (1) signal level. By following this consistent definition, the system software need not be concerned with whether external signals are high or low true. In particular, the modem signal inputs are low true, thus a 0 (true assertion) at a modem input pin is represented by a 1 (true) in the MSR.

Any change of state in any modem input signals will set the Modem Status (MS) bit in the USR register. When this happens, an interrupt (INTR) will be generated if the MIEN and INTEN bits of the MCR are enabled.

The Data Set Ready (DSR) input is a status indicator from the modem to the KS82C52 which indicates that the modem is ready to provide received data to the KS82C52 receiver circuitry.

Clear to Send (CTS) is both a status and control signal from the modem that tells the KS82C52 that the modem is ready to receive transmit data from the KS82C52 transmitter output (SDO). A high (false) level on this input will inhibit the KS82C52 from beginning transmission and if asserted in the middle of a transmission will only permit the KS82C52 to finish transmission of the current character.

Receiver Buffer Register (RBR)

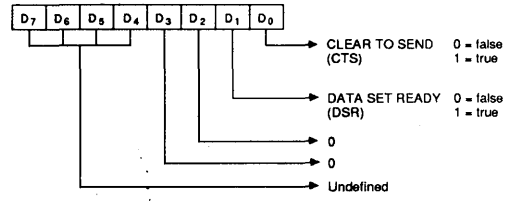
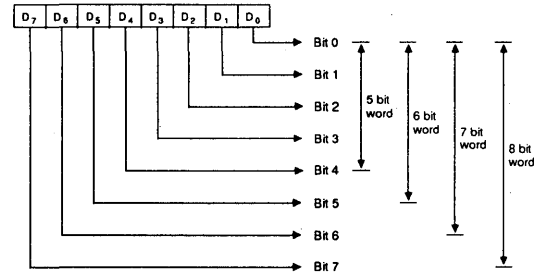


Figure 12 : MSR

The receiver circuitry in the KS82C52 is programmable for 5, 6, 7 or 8 data bits per character. For words of less than 8 bits, the data is right justified to the Least Significant Bit (LSB = D_0). Bit D_0 of a data word is always the first data bit received. The unused bits in a less than 8 bit word, at the parallel interface, are set to a logic zero (0) by the KS82C52.

Received data at the SDI input pin is shifted into the Receiver Register by an internal 1 x clock which has been synchronized to the incoming data based on the position of the start bit. When a complete character has been shifted into the Receiver Register, the assembled data bits are parallel loaded into the Receiver Buffer Register. Both the DR output pin and DR flag in the USR register are set. This double buffering of the received data permits continuous reception of data without losing any of the received data.

While the Receiver Register is shifting a new character into the KS82C52, the Receiver Buffer Register is holding a previously received character for the system CPU to read. Failure to read the data in the RBR before complete reception of the next character can result in the loss of the data in the Receiver Register. The OE flag in the USR register indicates the overrun condition.



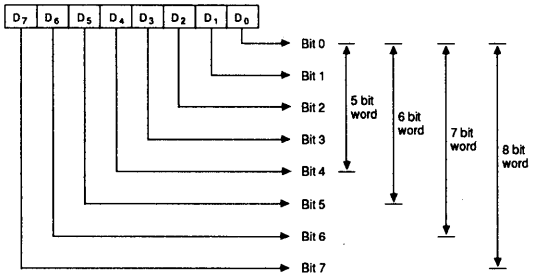
Note: The LSB, Bit 0 is the first serial data bit received.

Figure 13 : RBR

Transmitter Buffer Register (TBR)

The Transmitter Buffer Register (TBR) accepts parallel data from the data bus (D_0-D_7) and holds it until the Transmitter Register is empty and ready to accept a new character for transmission. The transmitter always has the same word length and number of stop bits as the receiver. For words of less than 8 bits the unused bits at the microprocessor data bus are ignored by the transmitter.

Bit 0, which corresponds to D_0 at the data bus, is always the first serial data bit transmitted. Provision is made for the transmitter parity to be the same or different from the receiver. The TBRE output pin and flag (USR register) reflect the status of the TBR. The TC flag (USR register) indicates when both the TBR and TR are empty.



Note: The LSB, Bit 0 is the first serial data bit transmitted.

Figure 14 : TBR

INTERRUPT STRUCTURE

The KS82C52 has provisions for software masking of interrupts generated for the INTR output pin. Two control bits in the MCR register, MIEN and INTEN, control modem status interrupts and overall KS82C52 interrupts respectively. Figure 15 illustrates the logical control function provided by these signals.

The modem status inputs ($\overline{DSR}$ and $\overline{CTS}$) will trigger the edge detection circuitry with any change of status. Reading the MSR register will clear the detect circuit but has no effect on the status bits themselves. These status bits always reflect the state of the input pins regardless of the mask control signals. Note that the state (high or low) of the status bits are inverted versions of the actual input pins.

The edge detection circuits for the USR register signals will trigger only for a positive edge (true assertion) of these status bits. Reading the USR register not only clears the edge detect circuit but also clears (sets to 0) all of the status bits. The output pins associated with these status bits are not affected by reading the USR register.

A hardware reset of the KS82C52 sets the TC status bit in the USR. When interrupts are subsequently enabled an interrupt can occur due to the fact that the positive edge detection circuitry in the interrupt logic has detected the setting of the TC bit. If this interrupt is not desired the USR should be read prior to enabling interrupts. This action resets the positive edge detection circuitry in the interrupt control logic (Figure 15).

Note: For USR and MSR, the setting of status bits is inhibited during status register READ operations. If a status condition is generated during a READ operation, the status bit is not set until the trailing edge of the RD pulse.

If the bit was already set at the time of the READ operation, and the same status condition occurs, that status bit will be cleared at the trailing edge of the RD pulse instead of being set again.

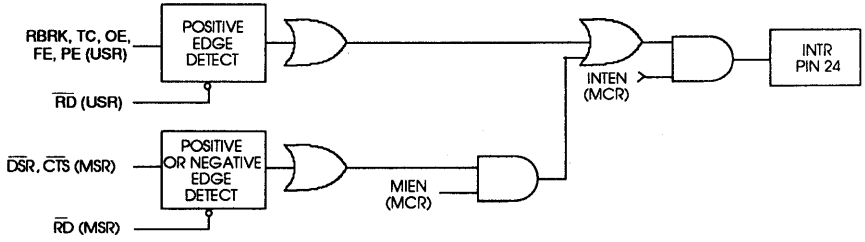


Figure 15 : INTERRUPT STRUCTURE

SOFTWARE RESET

A software reset of the KS82C52 is a useful method for returning to a completely known state without exercising a complete system reset. Such a reset would consist of writing to the UCR, BRSR and MCR registers. The USR and RBR registers should be read prior to enabling interrupts in order to clear out any residual data or status bits which may be invalid for subsequent operation.

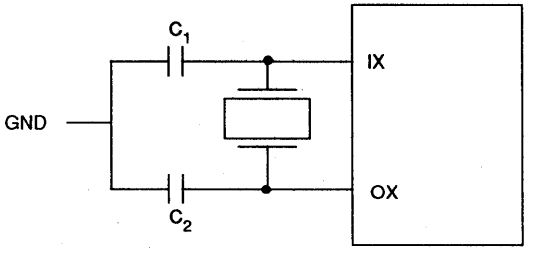
CRYSTAL OPERATION

The KS82C52 crystal oscillator circuitry is designed to operate with a fundamental mode, parallel resonant crystal. To summarize, Table 10 and Figure 16 show the required crystal parameters and crystal circuit configuration respectively.

When using an external clock source, the IX input is driven and the OX output is left open. Power consumption when using an external clock is typically 50% of that required when using a crystal. This is due to the sinusoidal nature of the drive circuitry when using a crystal.

Table 10 : CRYSTAL SPECIFICATIONS

Parameter	Typical Crystal Specs
Frequency	1.0 to 16 MHz
Type of Operation	Parallel resonant, Fundamental mode
Load Capacitance (C_L)	20 or 32 pF (typ.)
R_{series} (Max.)	100 Ω (f = 16 MHz, C_L = 32 pF) 200 Ω (f = 16 MHz, C_L = 20 pF)



* C1 = C2 = 20 pf for C_L = 20 pf
* C1 = C2 = 47 pf for C_L = 32 pf

Figure 16 : TYPICAL CRYSTAL CIRCUIT

APPLICATIONS

The following example (Figure 17) shows the interface for an KS82C52 in an 80C86 system.
Use of the Samsung Interrupt Controller (KS82C59A) is optional and necessary only if an interrupt driven system is desired.

By using the Samsung KS82C84A clock generator, the system can be built with a single crystal providing both the processor clock and the clock for the 82C52. The 82C52 has special divider circuitry which is designed to supply industry standard baud rates with a 2.4576 MHz input frequency. Using a 15 MHz crystal as shown, results in less than a 2% frequency error which is adequate for many applications. For more precise baud rate requirements, a 14.7456 MHz crystal will drive the 80C86 at 4.9 MHz and provide the 82C52 with the standard baud rate input frequency of 2.4576 MHz. If baud rates above 156 Kbaud are desired, the OSC output can be used instead of the PCLK (+6) output for asynchronous baud rates up to 1 Mbaud.

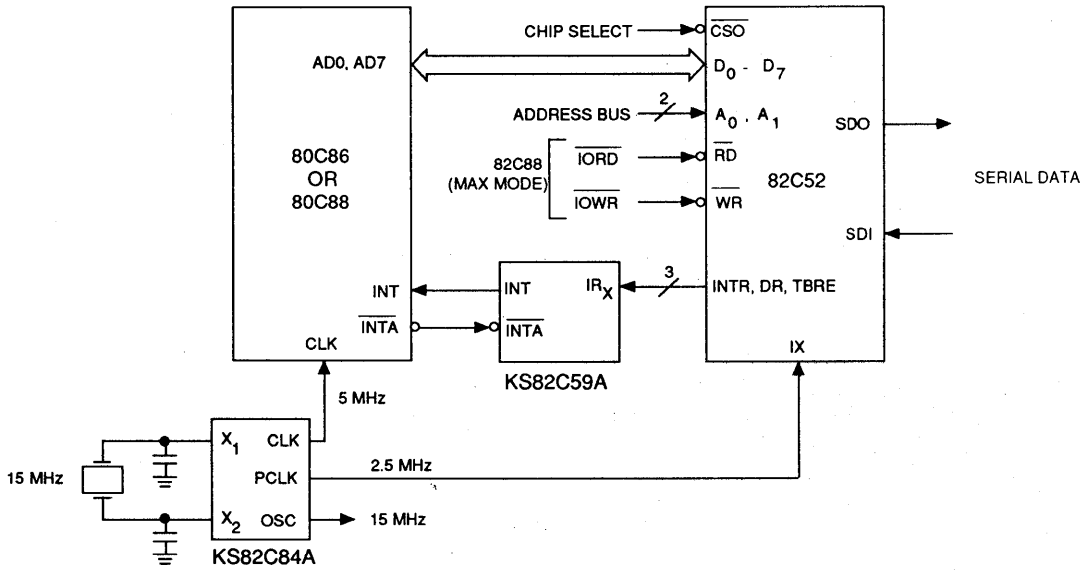


Figure 17 : 80C86/KS82C52 INTERFACE

PACKAGE DIMENSIONS

Units: Inches

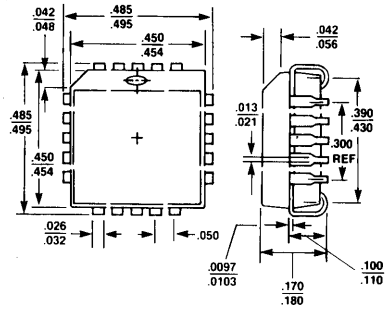


Figure 17 : PLCC PACKAGING

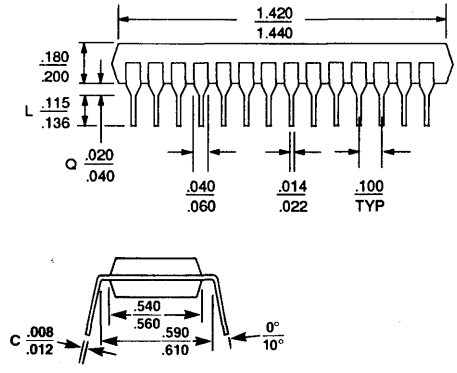
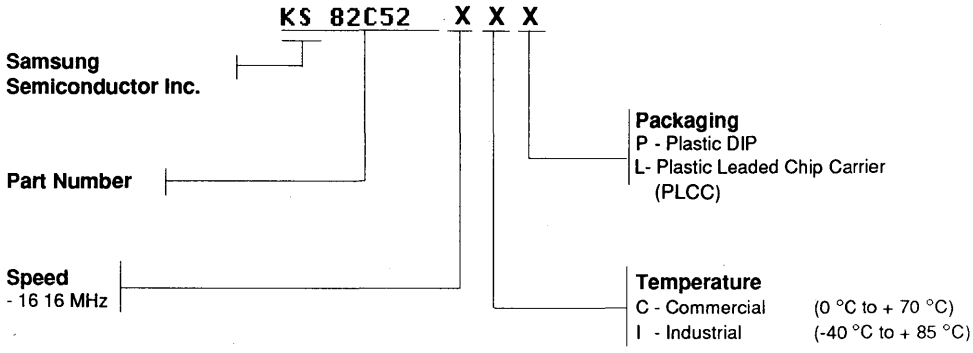


Figure 18 : PLASTIC PACKAGING

ORDERING INFORMATION



Samsung products are designated by a Product Code. When ordering, refer to products by their full code. For unusual, and/or specific packaging or processing requirements not covered by the standard product line, contact the *Samsung Microprocessor Peripherals Product Marketing.*

KS82C54

PROGRAMMABLE INTERVAL TIMER

FEATURES/BENEFITS

- **A high performance device featuring pin and functional compatibility with the industry standard 8254**
- **High Speed — 8MHz and 10MHz versions**
- **Low power CMOS implementation**
- **TTL input/output compatibility**
- **Compatible with 8080/85, 8086/88, 80286/386 and 680X0μP families**
- **Fully static operation**
- **Three independent 16 bit counters**
- **Six programmable counter modes**
- **Status read-back command**
- **Binary or BCD counting**

DESCRIPTION

The KS82C54 is a counter/timer device that includes complete pin and functional compatibility with the industry standard 8254. Designed for fast 10MHz operation, it has three independently programmable 16 bit counters and six programmable counter modes. Counting can be performed in both binary and BCD formats.

The KS82C54 offers a very flexible, hardware solution to the generation of accurate time delays in microprocessor systems. A general purpose, multi-timing element, it can be used to implement event counters, elapsed time indicators, waveform generators plus a host of other functions.

The low power consumption of the KS82C54 makes it ideally suited to portable systems or those with low power standby modes. It is manufactured using proven CMOS process technology to produce a solid, reliable product.

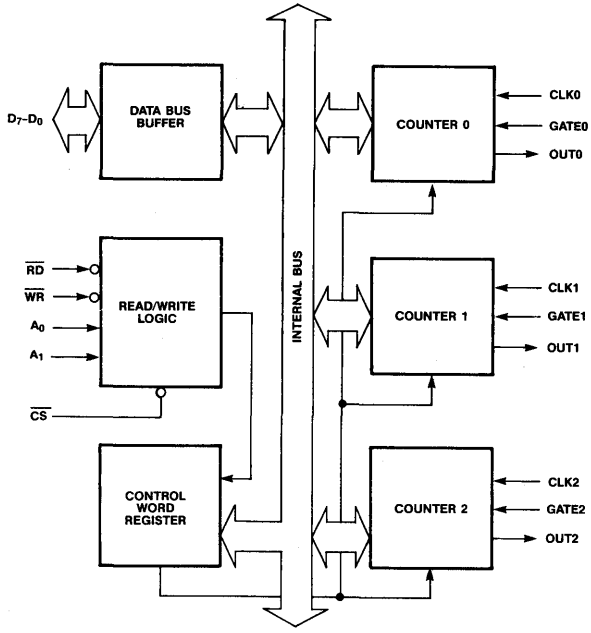


Figure 2: KS82C54 Block Diagram

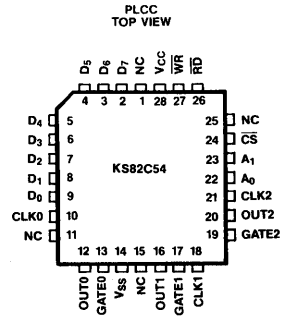


Figure 1a: Plastic Leaded Chip Carrier

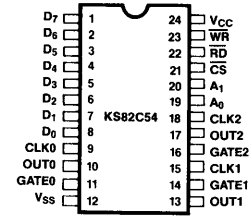


Figure 1b: 24-Pin Configuration

Table 1a: 28-Pin PLCC Pin Assignment

Pin #	I/O	Pin Name	Pin #	I/O	Pin Name
1	—	NC	15	—	NC
2	I/O	D_7	16	O	OUT1
3	I/O	D_6	17	I	GATE1
4	I/O	D_5	18	I	CLK1
5	I/O	D_4	19	I	GATE2
6	I/O	D_3	20	O	OUT2
7	I/O	D_2	21	I	CLK2
8	I/O	D_1	22	I	A_0
9	I/O	D_0	23	I	A_1
10	I	CLK0	24	I	$\overline{CS}$
11	—	NC	25	—	NC
12	O	OUT0	26	I	$\overline{RD}$
13	I	GATE0	27	I	$\overline{WR}$
14	—	V_{SS}	28	—	V_{CC}

Table 1b: 24-Pin DIP Pin Assignment

Pin #	I/O	Pin Name	Pin #	I/O	Pin Name
1	I/O	D_7	13	O	OUT1
2	I/O	D_6	14	I	GATE1
3	I/O	D_5	15	I	CLK1
4	I/O	D_4	16	I	GATE2
5	I/O	D_3	17	O	OUT2
6	I/O	D_2	18	I	CLK2
7	I/O	D_1	19	I	A_0
8	I/O	D_0	20	I	A_1
9	I	CLK0	21	I	$\overline{CS}$
10	O	OUT0	22	I	$\overline{RD}$
11	I	GATE0	23	I	$\overline{WR}$
12	—	V_{SS}	24	—	V_{CC}

3

Table 2: Pin Descriptions

Symbol	Type	Name and Function
A_0, A_1	I	**Address:** These two address pins are used to select the Control Word Register (for read or write operations), or one of the three counters. They are normally connected to the system address bus.
$\overline{CS}$	I	**Chip Select:** Active LOW control signal to enable the KS82C54 to respond to RD and WR signals. If CS is not LOW, RD and WR are ignored.
D_7 - D_0	I/O	**Data:** Bi-directional 3-state data bus lines, connected to system data bus.
CLK0	I	**Clock 0:** Clock input of Counter 0.
CLK1	I	**Clock 1:** Clock input of Counter 1.
CLK2	I	**Clock 2:** Clock input of Counter 2.
GATE0	I	**Gate 0:** Gate input of Counter 0.
GATE1	I	**Gate 1:** Gate input of Counter 1.

A_1	A_0	Selects
0	0	Counter 0
0	0	Counter 1
0	1	Counter 2
1	1	Control Word Register

Table 2: Pin Descriptions (Continued)

Symbol	Type	Name and Function
GATE2	I	**Gate 2:** Gate input of Counter 2.
OUT0	O	**Output 0:** Output of Counter 0.
OUT1	O	**Output 1:** Output of Counter 1.
OUT2	O	**Output 2:** Output of Counter 2.
$\overline{RD}$	I	**Read Control:** Active LOW control signal used to enable the KS82C54 for read operations by the CPU.
$\overline{WR}$	I	**Write Control:** Active LOW control signal used to enable the KS82C54 to be written to by the CPU.
V_{CC}	—	**Power:** 5V ± 10% DC Supply.
V_{SS}	—	**Ground:** 0V.

FUNCTIONAL DESCRIPTION

The KS82C54 is a versatile programmable interval timer/counter designed for use in high speed 8, 16 and 32-bit microprocessor systems. It provides a means of generating accurate time delays in hardware that is fully software configurable. It can be treated as an array of I/O ports, with minimal software overhead.

The internal structure of the KS82C54 is illustrated in the block diagram of Figure 2. Major functional blocks include a data bus buffer, read/write logic, control word register, and three programmable counters.

Data bus Buffer Block

The 8-bit, 3-state data bus buffer provides controllable, bidirectional interface between the KS82C54 and the microprocessor system bus.

Read/Write Logic Block

The read/write logic block generates internal control signals for the different functional blocks using address and control information obtained from the system. The active LOW signals: $\overline{CS}$, $\overline{RD}$ and $\overline{WR}$ are used to select the KS82C54 for operation, read a counter, and write to a counter (or the control word register) respectively. $\overline{CS}$ must be LOW for $\overline{RD}$ or $\overline{WR}$ to be recognized. Note that $\overline{RD}$ and $\overline{WR}$ must not be active at the same time.

The inputs A_0 and A_1 are used to select the Control Word Register, or one of the three counters that is to be written to or read from (see Table 4). A_0 and A_1 connect directly to the corresponding signals of the microprocessor address bus, while $\overline{CS}$ is derived from the address bus using either a linear select method, or an address decoder device.

Control Word Register

The Control Word Register is a write only register that is selected by the read/write logic block when A_0 and A_1 = 1. When $\overline{CS}$ and $\overline{WR}$ are LOW, data is written into the KS82C54 Control Word Register from the CPU via the data bus buffer. Control word data is interpreted as a number of different commands which are used to program the various device functions. For example, status information is available with the Read-Back Command. These are discussed further in the section on programming.

Counter Blocks

The KS82C54 contains three identical, independent counter blocks. Each counter provides the same functions, but can be programmed to operate in different modes relative to each other. A typical KS82C54 counter is illustrated in Figure 3, and contains the following functional elements: control logic, counter, output latches, count registers and status register.

The Control Logic provides the interface between the Counter Element, the program instructions contained in the Control Word Register and the external signals CLKn, GATEn and OUTn. It also keeps the Status Register information current, controls the access of OL and CR to the internal data bus, and the loading of CE from the CR registers.

The Counter Element (shown in the Figure 3 as CE, for Counting Element) is a 16-bit presettable synchronous down counter.

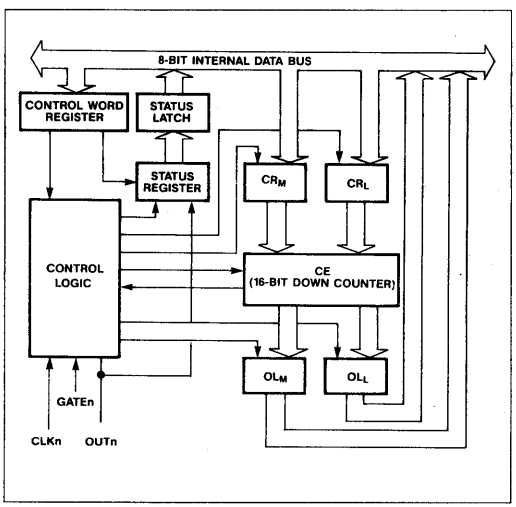
The Output Latches (shown as OL_M and OL_L) provide a mechanism whereby the CPU can read the current contents of the CE. These two 8-bit latches (M for most significant byte and L for least significant byte) together form a 16-bit latch capable of holding the complete content of the CE. Note that this arrangement is also used for communicating 16-bit values over the 8-bit internal data bus.

During normal operation, the contents of OL track with the contents of CE. When a Counter Latch Command is issued by the CPU to a particular counter, its OL latches the current value of CE so that it can be read by the CPU (the CE cannot be read directly). OL then returns to tracking with CE. Note that only one latch (OL_M followed by OL_L) at a time is enabled by the counter's control logic.

The Count Registers (shown as CR_M and CR_L) behave as input latches to the CE, and provide a mechanism whereby the initial count value can be downloaded from the CPU to the CE. Similar in operation to OL, CR is controlled by the counter control logic. When a two byte initial count is to be downloaded, it is transferred one byte at a time across the internal KS82C54 data bus to the appropriate register (CR_M if the most significant byte, CR_L otherwise). CE is loaded by transferring both bytes simultaneously from CR. Note that CR is the interface between CE and the data bus, since CE cannot be accessed directly.

Both CR_M and CR_L are cleared automatically when the counter is programmed and a new initial count is to be written. Thus, regardless of the counter's previous programming, both CR bytes will be initialized to a known zero state. This is important in the case where one byte counts are programmed (either most significant or least significant byte), so that the unused byte is always zero, and won't corrupt the initial count value loaded into CE.

Figure 3: Block Diagram of a Counter



The Status Register and Status Latch is used to hold the current contents of the Control Word Register and the status of the output and null count flag (see section on Programming). The contents of the Status Register must be latched to become available to the data bus, where they can be read by the CPU.

Note that the Control Word Register is also shown in the Counter block diagram. While not a part of the Counter Element, its contents determine the functional operation of the counter, including mode selection programmed.

OPERATIONAL DESCRIPTION

The following operations are common to all modes.

Control Word: When a Control Word is written to a Counter, all Control Logic is Reset, and OUT is initialized to a known state. No CLK pulses are needed.

Gate: The GATE input is always sampled on the rising edge of CLK. In modes 0, 2, 3, and 4 the GATE input is level sensitive, and the logic level is sampled on the rising edge of CLK. In modes 1, 2, 3, and 5 the GATE input is rising-edge sensitive. In these modes, a rising edge of GATE (trigger) sets an edge-sensitive flip-flop in the Counter. This flip-flop is sampled on the next rising edge of CLK, then is immediately reset. In this way, a trigger will be detected no matter when it occurs and a high logic level does not have to be maintained until the next CLK pulse. A summary is given in Table 5.

Note that in Modes 2 and 3, the GATE input is both edge-and level-sensitive. If a CLK source other than the system clock is used in modes 2 and 3, GATE should be pulsed immediately after the $\overline{WR}$ for a new count value.

Counter: New Counts are loaded, with the largest possible initial COUNT being 0; (equivalent to 2^{16} for binary counting and 10^4 for BCD counting, as in Table 3)

Counters decremented on the falling edge of CLK do not stop when they reach zero. In Modes 0, 1, 4, and 5 the Counters wrap around to the highest count (either FFFF hex for binary counting or 9999 for BCD counting), then continue counting. Modes 2 and 3 are periodic; the Counters reload themselves with the initial count, then continue counting from there.

Table 3: MIN and MAX Initial Counts

Mode	Minimum Count	Maximum Count*
0	1	0
1	1	0
2	2	0
3	2	0
4	1	0
5	1	0

* 0 is equivalent to 2^{16} for binary counting and 10^4 for BCD counting.

Table 4: Read/Write Operations Summary

$\overline{CS}$	$\overline{RD}$	$\overline{WR}$	A_1	A_0	
0	1	0	0	0	Write into Counter 0
0	1	0	0	1	Write into Counter 1
0	1	0	1	0	Write into Counter 2
0	1	0	1	1	Write Control Word
0	0	1	0	0	Read from Counter 0
0	0	1	0	1	Read from Counter 1
0	0	1	1	0	Read from Counter 2
0	0	1	1	1	No-Operation (3-State)
1	X	X	X	X	No-Operation (3-State)
0	1	1	X	X	No-Operation (3-State)

If both the Count and Status Registers of a counter are latched, the first read operation of that counter will return the latched status, regardless of which was latched first. The next one or two reads (the counter can be programmed for one or two type counts) will return the latched count. Subsequent reads will return an unlatched count. Read and write operations are summarized in Table 4.

PROGRAMMING THE KS82C54

The KS82C54 is programmed by writing a Control Word into the Control Word Register (selected by A_0, A'1, 1') and an initial count to the Counter to be written into. A_0 and A_1 are used to select the appropriate Counter. The format of the count depends on the Control Word used.

Write Operation

As mentioned previously, programming of the KS82C54 is performed in two steps:

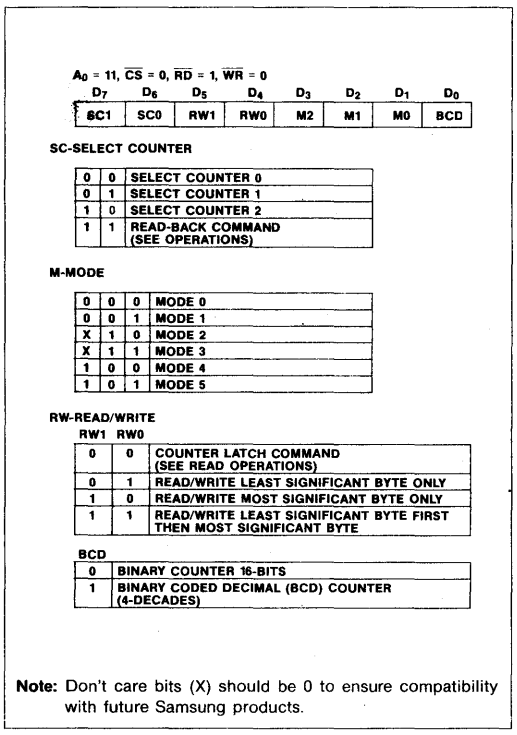
- Each counter requires a Control Word before the initial count can be written into the selected Counter.
- The initial count must follow the convention in the Control Word for the particular Counter; i.e., LSB or MSB only or LSB and then MSB.

The instruction sequence has to be followed as shown above, however, the sequence of programming the Counter can be random, since every Counter has its associated Control Word Register. A new initial count may be written to the Counter without rewriting the Control Word for that Counter. Of course, the new count must follow the programmed count format.

Table 5: Gate Pin Operations Summary

Signal Status Modes	Low, or Going Low	Rising	High
0	—	• Disables counting	• Enables counting
1	—	• Initiates counting • Resets output after next clock	—
2	• Disables counting • Sets output immediately high	• Initiates counting	• Enables counting
3	• Disables counting • Sets output immediately high	• Initiates counting	• Enables counting
4	• Disables counting	—	• Enables counting
5	—	• Initiates counting	—

Figure 4: Control Word Format



A_0 = 11, $\overline{CS}$ = 0, $\overline{RD}$ = 1, $\overline{WR}$ = 0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
SC1	SC0	RW1	RW0	M2	M1	M0	BCD

SC-SELECT COUNTER

0	0	SELECT COUNTER 0
0	1	SELECT COUNTER 1
1	0	SELECT COUNTER 2
1	1	READ-BACK COMMAND (SEE OPERATIONS)

M-MODE

0	0	0	MODE 0
0	0	1	MODE 1
X	1	0	MODE 2
X	1	1	MODE 3
1	0	0	MODE 4
1	0	1	MODE 5

RW-READ/WRITE

RW1	RW0	
0	0	COUNTER LATCH COMMAND (SEE READ OPERATIONS)
0	1	READ/WRITE LEAST SIGNIFICANT BYTE ONLY
1	0	READ/WRITE MOST SIGNIFICANT BYTE ONLY
1	1	READ/WRITE LEAST SIGNIFICANT BYTE FIRST THEN MOST SIGNIFICANT BYTE

BCD

0	BINARY COUNTER 16-BITS
1	BINARY CODED DECIMAL (BCD) COUNTER (4-DECADES)

Note: Don't care bits (X) should be 0 to ensure compatibility with future Samsung products.

If a Counter is programmed as a 16 bit counter, the Control Register should not be accessed between writing the first and second byte count. Otherwise, the Counter will be loaded incorrectly.

Read Operation

There are three methods of reading the Counters:

- by a simple read operation
- by a Counter Latch Command
- by a Read-Back Command

The first method is performed just by performing a read of the desired Counter Register. The value read is the current status and may be changing if the CLK input is not inhibited.

Counter Latch Command

This method of reading the Counter requires a write command to the Control Word Register of the Counter selected by SC0 and SC1 in the Control Word and RW0 and RW1 = '0'. See Figure 5. The selected counter output will be latched in the OL latch of the Counter at the time the Control Word is received and is held until it is read by the CPU or the Counter is reprogrammed. The OL latch is then loaded according to the Counter Element. This allows reading the Counter at any time without affecting counting. More than one Latch Command may be issued since all counter blocks are built identical. Latching the count by the Latch Command does not influence the programmed Mode of the Counter. Multiple successive Latch Commands do not overwrite the value latched at the first Latch Command. Only a read of the OL or reprogramming of the Counter will alter the latched Counter value. It is also important that two read commands have to be issued if the Counter is programmed as a 16 bit counter. A program may not transfer commands between the two read cycles. Otherwise, an incorrect count value will be read.

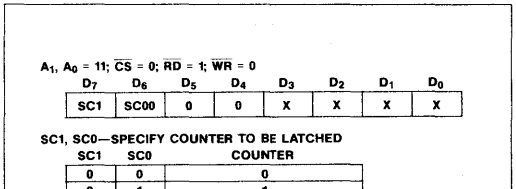
Read-Back Command

A third method of reading the count value requires issuing a Read-Back Command prior to the read operation. See Figure 6. If the $\overline{COUNT}$ bit is set, the appropriate count values of the Counter selected by CNT0, 1, 2 are latched. The status of the Counter are latched if the STATUS bit is '1'. Multiple counters may be selected.

The Counter Status format is shown in Figure 7. D0 to D5 contain the Mode of the counter as programmed by the last Control Word.

D6 (Null Count) indicate when the last Count Register (CR) has been loaded into the Counting Element (CE). See also Mode Definition.

Figure 5: Counter Latching Command Format



A_1, A_0 = 11; $\overline{CS}$ = 0; $\overline{RD}$ = 1; $\overline{WR}$ = 0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
SC1	SC00	0	0	X	X	X	X

SC1, SC0—SPECIFY COUNTER TO BE LATCHED

SC1	SC0	COUNTER
0	0	0
0	1	1
1	0	1
1	1	READ-BACK COMMAND

D5, D4-00 DESIGNATED COUNTER LATCH COMMAND
X — DON'T CARE

Note: Don't care bits (X) should be 0 to ensure compatibility with future Samsung products.

'1' After a write to the Word Control Register (Note 1)
'1' After a write to the Counter Register (CR) (Note 2)
'0' After a new count is loaded into the Count Element (CR → CE).

Note 1: Only the Counter specified by the Control Word is affected.
Note 2: If the Counter is programmed for two byte counts, the $\overline{COUNT}$ bit goes to '1' after the second byte is written.

The output OUT of the selected counter can be read by D7 (OUTPUT) of the Status byte. If both $\overline{COUNT}$ and $\overline{STATUS}$ has been selected, the first read operation of that Counter will return the latched status and the next one or two read will return the latched count. Subsequent reads return unlatched counts.

Figure 6: Read-Back Command Format

A_1, A_0 = 22; $\overline{CS}$ = 0; $\overline{RD}$ = 1; $\overline{WR}$ = 0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	1	$\overline{COUNT}$	$\overline{STATUS}$	CNT2	CNT1	CNT0	0

D_5 : 0 = Latch count of selected conter(s)
D_4 : 0 = Latch status of selected counter(s)
D_3 : 1 = Select Counter 2
D_2 : 1 = Select Counter 1
D_1 : 1 = Select Counter 0
D_0 : Reserved for future expansion; Must be 0

Figure 7: Status Byte

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
OUTPUT	NULL COUNT	RW1	RW0	M2	M1	M0	BCD

D_7 : 1 = OUT Pin is 1
0 = OUT Pin is 0
D_6 : 0 = OUT Pin is 0
0 = Count Available for Reading
D_5-D_0 : Counter Programmed Mode (See Figure 4)

MODE DEFINITIONS

The following terms are useful in describing the operation of the KS82C84.

- CLK pulse: A rising edge, followed by a falling edge, of a Counter's CLK input.
- Trigger: A rising edge of a Counter's GATE input.
- Counter loading: Transfer of a count from the CR to the CE (see Functional Description)

Mode 0: Interrupt on Terminal Count

Mode 0 is typically used for event counting. After the Control Word is written, OUT is set low, and remains low until the Counter reaches zero. OUT then goes high and remains high until a new count or a new Mode 0 Control Word is written into the Counter.

GATE = 1 enables counting while GATE = 0 disables counting. GATE has no effect on OUT.

After a Control Word and initial count are written to a Counter, the initial count is loaded on the next CLK pulse. Since this CLK pulse does not decrement the count, OUT does not go high until N + 1 CLK pulses after the initial count is written (where N is the initial count value).

If a new count is written to the Counter, it is loaded on the next CLK pulse and counting continues from the new count. If a two-byte count is written, the following happens:

1. Writing the first byte disables counting. OUT is set low immediately (no clock pulse required).
2. Writing the second byte allows the new count to be loaded on the next CLK pulse.

This allows the counting sequence to be synchronized by software. Again, OUT does not go high until N + 1 CLK pulses after the new count of N is written.

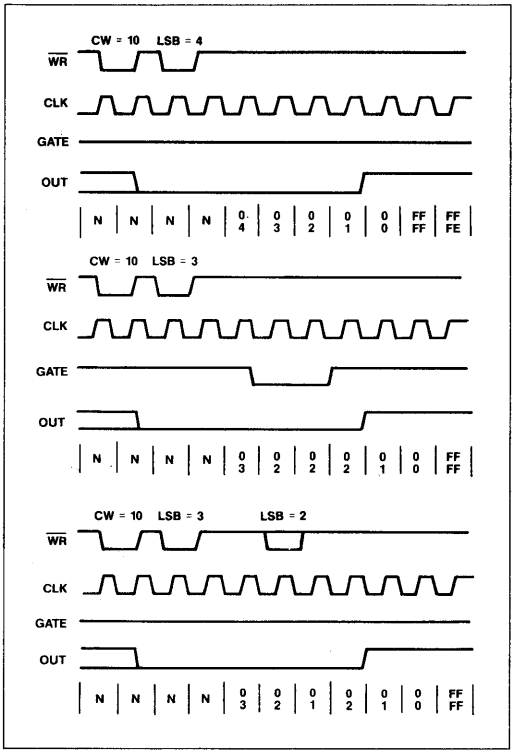
If an initial count is written while GATE = 0, it will still be loaded on the next CLK pulse. When GATE goes high, OUT will go high N CLK pulses later. A CLK pulse is not required to load the Counter as this has already been done.

Mode 1: Hardware Retriggerable One-Shot

OUT is initially high. To begin the one-shot pulse, OUT goes low on the CLK pulse following a trigger and remains low until the Counter reaches zero. OUT then goes high and remains high until the CLK pulse following the next trigger.

After a Control Word and intial count have been written, the Counter is armed. A trigger causes the Counter to be loaded and OUT to be set low on the next CLK pulse, starting the one-shot pulse. An initial count of N results in a one-shot pulse N CLK cycles long. Since the one-shot is retriggerable, OUT remains low for N CLK pulses after any trigger. The one-shot pulse can be repeated without rewriting the same count into the counter. GATE has no effect on OUT.

Figure 8: Mode 0 Timing



Notes: These conventions apply to all mode timing diagrams:

1. Counters are programmed for binary (not BCD) counting and for reading/writing least significant byte (LSB) only.
2. The counter is always selected ($\overline{CS}$ always low).
3. CW stands for Control Word; CW = 10 means a control word of 10, hex is written to the counter.
4. LSB is the Least Significant Byte of count.
5. Numbers below diagrams are count values. The lower number is the least significant byte. The upper number is the most significant byte. Since the counter is programmed to read/write only, the most significant byte cannot be read.
6. N stands for an undefined count. Vertical lines show transitions between count values.

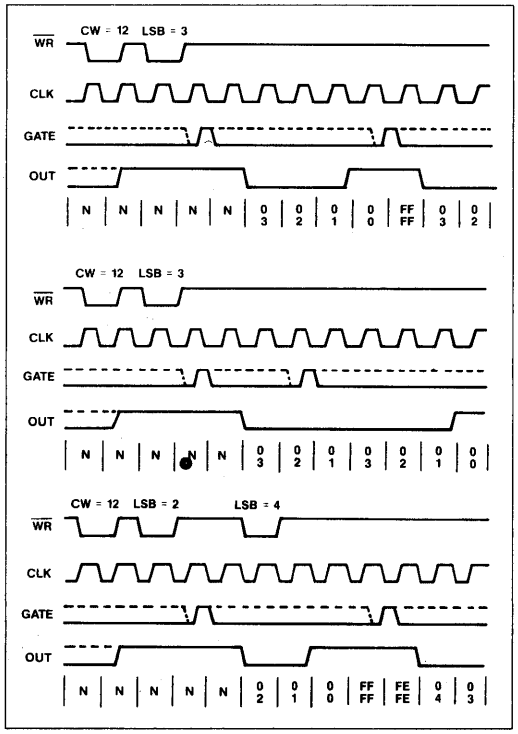
If a new count is written to the Counter during a one-shot pulse, the current one-shot is not affected unless the Counter is retriggered. In this case, the new count is loaded into the Counter and the one-shot pulse continues for the duration of the count.

Mode 2: Rate Generator

This mode functions like a divide-by-N counter and is typically used for generating Real Time Clock Interrupts. OUT is initially high. When the initial count has decremented to 1, OUT goes low for one CLK pulse, then high again. The Counter reloads the initial count and the process is repeated. Mode 2 is periodic, with the same sequence repeated indefinitely. For an initial count of N, the sequence repeats every N CLK cycles.

GATE = 1 enables counting; GATE = 0 disables counting. If GATE goes low during an output pulse, OUT is set high immediately. A trigger reloads the initial count into the Counter on the next CLK pulse; OUT goes low N CLK pulses after the trigger. Thus the GATE input can be used to synchronize the Counter.

Figure 9: Mode 1 Timing



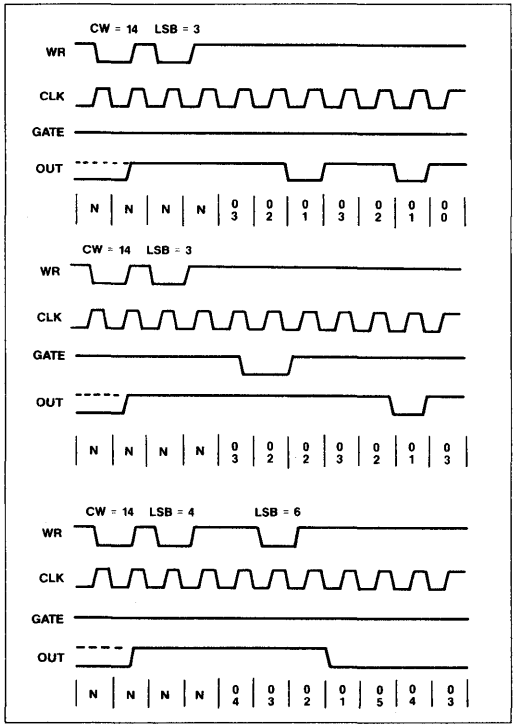
After a Control Word and intial count have been written, the Counter is loaded on the next CLK pulse. OUT goes low N CLK pulses after the initial count is written, which allows the Counter to be synchronized by software.

Writing a new count while counting does not affect the current counting sequence. If a trigger is received after a new count is written but before the end of the current period, the Counter is loaded with the new count on the next CLK pulse and counting continues from the new count. Otherwise, the new count is loaded at the end of the current counting cycle. In Mode 2, a COUNT of 1 is illegal.

Mode 3: Square Wave Mode

Mode 3 is typically used for Baud rate generation, and is similar to Mode 2 except for the duty cycle of OUT. OUT is initially high. When half the initial count has expired, OUT goes low for the remainder of the count. Mode 3 is also periodic, with the sequence above repeated indefinitely. An initial count of N results in a square wave with a period of N CLK cycles.

Figure 10: Mode 2 Timing



Note: A gate transition should not occur one clock cycle prior to reaching the terminal count (TC).

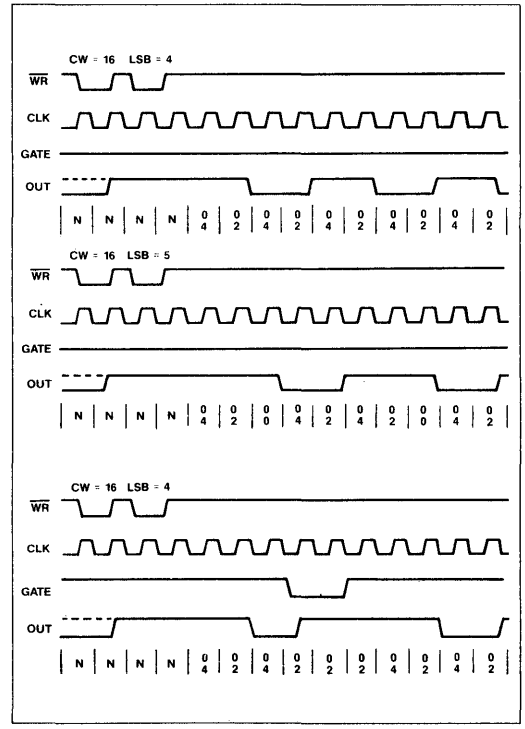
GATE = 1 enables counting; GATE = 0 disables counting. If GATE goes low while OUT is low, OUT is set high immediately (no CLK pulse is needed). A trigger reloads the Counter with the initial count on the next CLK pulse. Thus the GATE input can be used to synchronize the Counter.

The Counter is loaded on the next CLK pulse after a Control Word and initial count have been written. This allows the Counter to be synchronized by software.

Writing a new count while counting does not affect the current counting sequence. If a trigger is received after writing a new count but before the end of the current half-cycle of the square wave, the Counter is loaded with the new count on the next CLK pulse and counting continues from the new count. Otherwise, the new count is loaded at the end of the current half-cycle.

Mode 3 is implemented as follows according to whether the initial count value is even or odd:

Figure 11: Mode 3 Timing

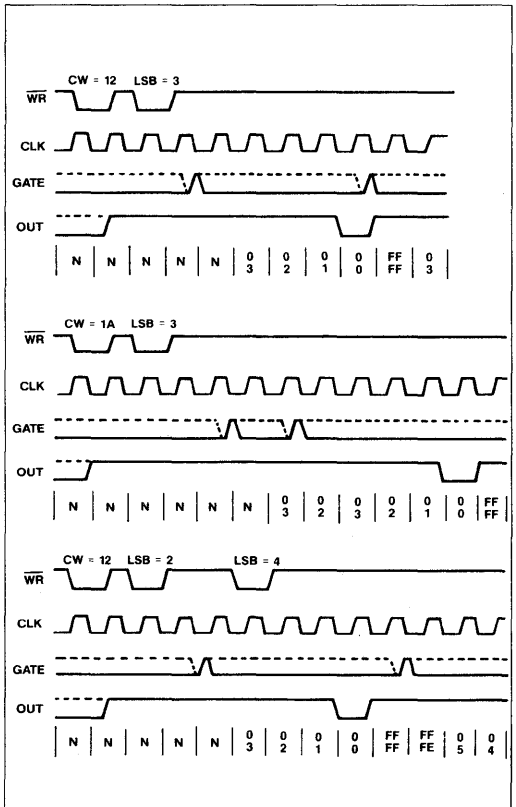


Note: A gate transition should not occur one clock cycle prior to reaching the terminal count (TC).

Even counts: OUT is initially high. The initial count is loaded on one CLK pulse and then decremented by two on succeeding CLK pulses. When the count expires, OUT goes low and the counter is reloaded with the initial count. The above process is repeated indefinitely.

Odd counts: OUT is initially high. The initial count minus one (to given an even number) is loaded on one CLK pulse and then decremented by two on succeeding CLK pulses. One CLK pulse after the count expires, OUT goes low and the Counter is reloaded with the initial count minus one. Succeeding CLK pulses decrement the count by two. When the count expires, OUT goes high again and the Counter is reloaded with the initial count minus one. The above process is repeated indefinitely. So for odd counts, OUT is high for (N + 1)/2 counts and low for (N - 1)/2 counts.

Figure 12: Mode 4 Timing



Mode 4: Software Triggered Strobe

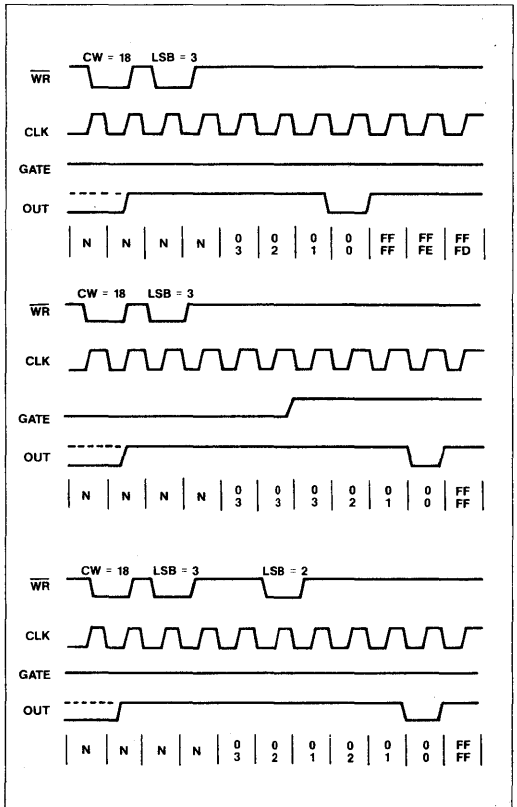
OUT is initially high. When the initial count expires, OUT goes low for one CLK pulse and then goes high again. The counting sequence is triggered by writing the initial count.

GATE = 1 enables counting; GATE = 0 disables counting. GATE has no effect on OUT.

The Counter is loaded on the next CLK pulse after a Control Word and initial count have been written. This CLK pulse does not decrement the count, so for an initial count of N, OUT does not strobe low until N + 1 CLK pulses after the initial count is written.

If a new count is written during counting, it is loaded on the next CLK pulse and counting continues from the new count. If a two-byte count is written, the following events occur:

Figure 13: Mode 5 Timing



1. Writing the first byte has no effect on counting.
2. Writing the second byte allows the new count to be loaded on the next CLK pulse.

This allows the sequence to be retriggered by software. OUT strobes low N + 1 CLK pulses after the new count of N is written.

Mode 5:
HARDWARE TRIGGERED strobe (Retriggerable).

OUT is initially high. Counting is triggered by a rising edge of GATE. When the initial count has expired, OUT goes low for one CLK pulse, then goes high again.

After a Control Word and initial count has been written, the counter is loaded on the first CLK pulse following a trigger. This CLK pulse does not decrement the count, so, given an initial count of N, OUT does not strobe low until N + 1 CLK pulses after a trigger.

A trigger causes the Counter to be loaded with the initial count on the next CLK pulse. The counting sequence is retriggerable, so OUT will not go low until N + 1 CLK pulses after any trigger. GATE has no effect on OUT.

If a new count is written during counting, the current counting sequence will not be affected. If a trigger occurs after the new count is written, but before the current count expires, the Counter will be loaded with the new count on the next CLK pulse and counting will continue from there.

Table 6: Recommended Operating Conditions

DC Supply Voltage		+4.0V to +6.0V
Operating Temperature Range	Commercial	0°C to 70°C
	Industrial	-40°C to +85°C

Table 7: Absolute Maximum Ratings

DC Supply Voltage	+7.0V
Input, Output or I/O Voltage Applied	V_{SS} - 0.5V to V_{CC} + 0.5V
Storage Temperature Range	-65°C to +150°C
Maximum Package Power Dissipation	1W

Note: Stresses beyond those listed above may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

3

Table 8: Capacitance (T_A = 25°C, V_{CC} = 0V, V_{IN} = +5V or V_{SS})

Symbol	Parameter	Test Conditions	Typ	Units
$C_{I/O}$	I/O Capacitance	FREQ = 1MHz Unmeasured Pins Returned to V_{SS}	20	pF
C_{IN}	Input Capacitance		10	pF
C_{OUT}	Output Capacitance		20	pF

Table 9: DC Characteristics (T_A = 0°C to 70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V)

Symbol	Parameter	Test Conditions	Limits		Units
			Min	Max	
I_{CC}	V_{CC} Supply Current		—	20	mA
I_{CCSB}	Standby Supply Current		—	10	μA
I_{IL}	Input Load Current	V_{IN} = V_{CC} to 0V	—	±20	μA
I_{OFL}	Output Float Leakage	V_{OUT} = V_{CC} to 0.45V	—	±10	μA
V_{IH}	Input High Voltage		2.0	V_{CC}+0.5V	V
V_{IL}	Input Low Voltage		-0.5	0.8	V
V_{OH}	Output High Voltage	I_{OH} = -400μA I_{OH} = -2.5mA	3.0 2.4	— —	V V
V_{OL}	Output Low Voltage	I_{OL} = 2.5mA	—	0.4	V

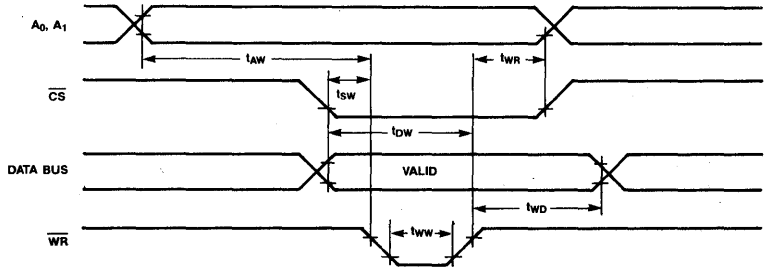
Table 10: AC Characteristics (T_A = 0°C to 70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V) Bus Parameters[1]

Symbol	Parameter	Test Conditions	Limits (8MHz)		Limits (10MHz)		Units
			Min	Max	Min	Max	
t_{AD}	Data delay from address		—	220	—	185	ns
t_{AR}	Address stable before $\overline{RD}$↓		45	—	30	—	ns
t_{AW}	Address stable before $\overline{WR}$		0	—	0	—	ns
t_{CL}	CLK setup for count latch		-40	45	-40	40	ns
t_{CLK}	Clock period		125	DC	100	DC	ns
t_{DF}	$\overline{RD}$↑ to data floating		5	90	5	65	ns
t_{DW}	Data setup time before $\overline{WR}$↑		120	—	95	—	ns
t_F	Clock fall time		—	25	—	25	ns
t_{GH}	Gate hold time after CLK↑	Note 2	50	—	50	—	ns
t_{GL}	Gate width low		50	—	50	—	ns
t_{GS}	Gate setup time to CLK↑		50	—	40	—	ns
t_{GW}	Gate width high		50	—	50	—	ns
t_{OD}	Output delay from CLK↓		—	150	—	100	ns
t_{ODG}	Output delay from GATE↓		—	120	—	100	ns
t_{PWH}	High pulse width	Note 3	60	—	30	—	ns
t_{PWL}	Low pulse width	Note 3	60	—	50	—	ns
t_R	Clock rise time		—	25	—	25	ns
t_{RA}	Address hold time after $\overline{RD}$↑		0	—	0	—	ns
t_{RD}	Data delay from $\overline{RD}$↓		—	120	—	85	ns
t_{RR}	$\overline{RD}$ pulse width		150	—	95	—	ns
t_{RV}	Command recovery time		200	—	165	—	ns
t_{SR}	$\overline{CS}$ stable before $\overline{RD}$↓		0	—	0	—	ns
t_{SW}	$\overline{CS}$ stable before $\overline{WR}$↓		0	—	0	—	ns
t_{WA}	Address hold time $\overline{WR}$↑		0	—	0	—	ns
t_{WC}	CLK delay for loading		0	55	0	55	ns
t_{WD}	Data hold time after $\overline{WR}$↑		0	—	0	—	ns
t_{WG}	Gate delay for sampling		-5	50	-5	40	ns
t_{WO}	OUT delay from Mode Write		—	260	—	240	ns
t_{WW}	$\overline{WR}$ pulse width		150	—	95	—	ns

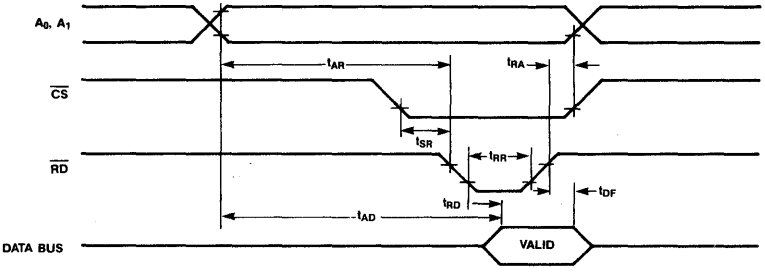
Notes:
1. AC timings measured at V_{OH} = 2.0V, V_{OL} = 0.8V.
2. In modes 1 and 5, triggers are sampled on each rising clock edge. A second trigger within 120ns of the rising clock edge may not be detected (70ns for KS82C54-10).
3. Low-going glitches that violate t_{PWH}, t_{PWL} may cause errors requiring counter reprogramming.

Figure 14: Timing Diagrams

a) Write Timing

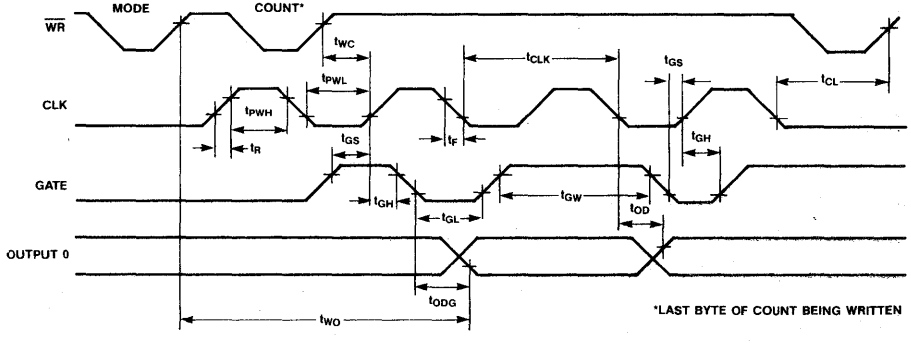


b) Read Timing



c) Recover Timing

d) Clock and Gate Timing



PACKAGE DIMENSIONS

Units: Inches

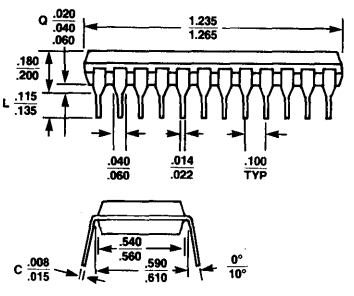


Figure 15: Plastic Package

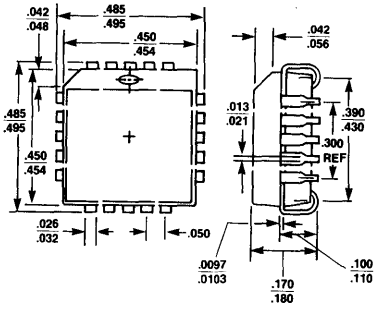


Figure 16: PLCC Package

ORDERING INFORMATION & PRODUCT CODE

KS 82C54 X X X

SAMSUNG SEMICONDUCTOR

Part Number

Speed
-8 8MHz
-10 10MHz

Packaging
P — Plastic DIP
L — Plastic Leaded Chip Carrier (PLCC)

Temperature
C — Commercial (0°C to +70°C)
I — Industrial (–40°C to +85°C)

SAMSUNG products are designated by a Product Code. When ordering, please refer to products by their full code. For unusual, and/or specific packaging or processing requirements not covered by the standard product line, please contact the SAMSUNG MOS Products Group.

KS82C55A

PROGRAMMABLE PERIPHERAL INTERFACE

FEATURES/BENEFITS

- **Pin and functional compatibility with the industry standard 8255A**
- **Provides support for 8080/85, 8086/8 and 80186 286/386**
- **Very high speed — 5MHz, 8MHz and 10MHz version**
- **Low power CMOS implementation**
- **TTL input/output compatibility**
- **24 programmable I/O pins**
- **Direct bit set/reset capability**
- **Bidirectional bus operation**
- **Enhanced control word read capability**
- **Bus-hold circuitry on all I/O ports eliminates pull-up resistors**

DESCRIPTION

The KS82C55A Programmable Peripheral Interface is a high performance CMOS device offering pin for pin functional compatibility with the industry standard 8255A. It includes 24 I/O pins which may be individually programmed in 2 groups of 12 and used in 3 major modes of operation. Bus hold circuitry on all I/O ports together with TTL compatibility over the full temperature range eliminates the need for pull-up resistors.

The KS82C55A is a general purpose programmable I/O device designed for use with many different microprocessors. Also makes it an attractive addition in portable systems or systems with low power standby modes.

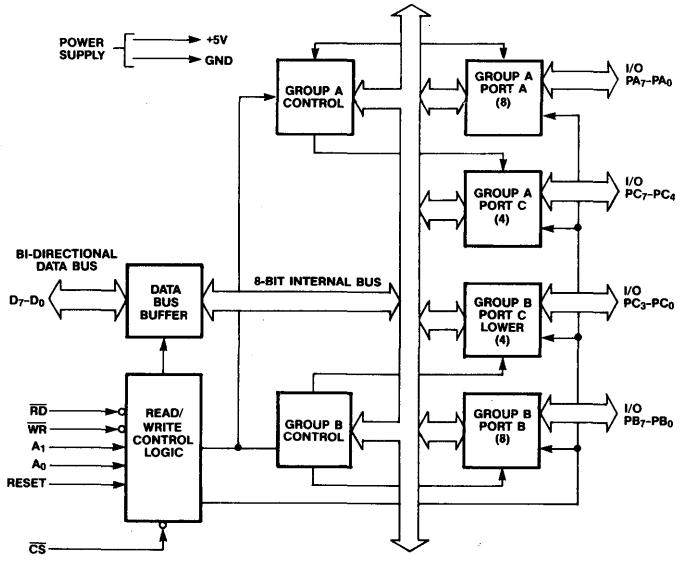


Figure 2: KS82C55A Block Diagram

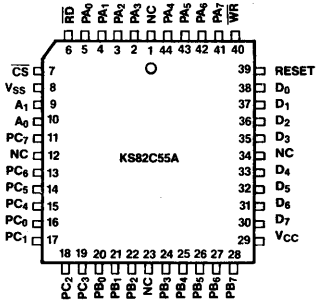


Figure 1a: 44-Pin PLCC Configuration

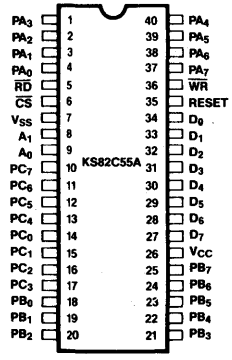


Figure 1b: 40-Pin DIP Configuration

Table 1a: 44-Pin PLCC Pin Assignment

Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name
1	NC	9	A_1	17	PC_1	25	PB_4	33	D_4	41	PA_7
2	PA_3	10	A_0	18	PC_2	26	PB_5	34	NC	42	PA_6
3	PA_2	11	PC_7	19	PC_3	27	PB_6	35	D_3	43	PA_5
4	PA_1	12	NC	20	PB_0	28	PB_7	36	D_2	44	PA_4
5	PA_0	13	PC_6	21	PB_1	29	V_{CC}	37	D_1		
6	$\overline{RD}$	14	PC_5	22	PB_2	30	D_7	38	D_0		
7	$\overline{CS}$	15	PC_4	23	NC	31	D_6	39	RESET		
8	V_{SS}	16	PC_0	24	PB_3	32	D_5	40	$\overline{WR}$		

Table 1b: 40-Pin DIP Pin Assignment

Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name
1	PA_3	8	A_1	15	PC_1	22	PB_4	29	D_5	36	$\overline{WR}$
2	PA_2	9	A_0	16	PC_2	23	PB_5	30	D_4	37	PA_7
3	PA_1	10	PC_7	17	PC_3	24	PB_6	31	D_3	38	PA_6
4	PA_0	11	PC_6	18	PB_0	25	PB_7	32	D_2	39	PA_5
5	$\overline{RD}$	12	PC_5	19	PB_1	26	V_{CC}	33	D_1	40	PA_4
6	$\overline{CS}$	13	PC_4	20	PB_2	27	D_7	34	D_0		
7	V_{SS}	14	PC_0	21	PB_3	28	D_6	35	RESET		

FUNCTIONAL DESCRIPTION

General

The KS82C55A is a programmable peripheral interface device designed for use in high speed, low power microcomputer systems. It is a general purpose I/O component which functions to interface peripheral equipment to the microcomputer system bus. The functional configuration of the KS82C55A is programmed by the system software such that no external logic is necessary to interface peripheral devices.

Data Bus Buffer

This 3-state bidirectional 8-bit buffer is used to interface the KS82C55A to the system data bus. Data is transmitted or received by the buffer upon execution of input or output instructions by the CPU. The data bus buffer also transfers control words and status information.

Read/Write and Control Logic

This block manages all of the internal and external transfers of both Data and Control or Status Words. It accepts inputs from the CPU Address and Control buses and issues commands to both of the Control Groups.

Group A and Group B Controls

The functional configuration of each port is programmed by the system software. The CPU outputs a Control Word to the KS82C55A. The Control Word contains information such as code, bit set, bit reset, etc., that initializes the functional configuration of the KS82C55A.

Each of the Control blocks (Group A and Group B) accepts commands from the Read/Write Control Logic, receives Control Words from the internal data bus and issues the proper commands to its associated ports.

- Control Group A - Port A and Port C upper (C_7-C_4)
- Control Group B - Port B and Port C lower (C_3-C_0)

Table 2: Pin Descriptions

<table>
<tr><th>Symbol</th><th>Type</th><th>Name and Function</th></tr>
<tr><td>A_0, A_1</td><td>I</td><td>Address: These input signals in conjunction with $\overline{RD}$ and $\overline{WR}$, control the selection of one of the three ports or the Control Word Registers.
<table>
<tr><th>A_1</th><th>A_0</th><th>$\overline{RD}$</th><th>$\overline{WR}$</th><th>$\overline{CS}$</th><th>Input Operation (Read)</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>Port A - Data Bus</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>Port B - Data Bus</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>Port C - Data Bus</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>Control Word - Data Bus</td></tr>
</table>
<table>
<tr><th>A_1</th><th>A_0</th><th>$\overline{RD}$</th><th>$\overline{WR}$</th><th>$\overline{CS}$</th><th>Output Operation (Write)</th></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>Data Bus - Port A</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>Data Bus - Port B</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>Data Bus - Port C</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>Data Bus - Control</td></tr>
</table>
<table>
<tr><th>A_1</th><th>A_0</th><th>$\overline{RD}$</th><th>$\overline{WR}$</th><th>$\overline{CS}$</th><th>Disable Function</th></tr>
<tr><td>X</td><td>X</td><td>X</td><td>X</td><td>1</td><td>Data Bus - 3-State</td></tr>
<tr><td>X</td><td>X</td><td>1</td><td>1</td><td>0</td><td>Data Bus - 3-State</td></tr>
</table></td></tr>
<tr><td>$\overline{CS}$</td><td>I</td><td>Chip Select: A low on this input enables the KS82C55A to respond to $\overline{RD}$ and $\overline{WR}$ signals. $\overline{RD}$ and $\overline{WR}$ are ignored otherwise.</td></tr>
<tr><td>D_{0-7}</td><td>I/O</td><td>Data Bus: Bi-directional, 3-state data bus lines, connected to system data bus.</td></tr>
<tr><td>PA_{0-7}</td><td>I/O</td><td>Port A, Pins 0-7: An 8-bit data output latch/buffer and an 8-bit data input buffer.</td></tr>
<tr><td>PB_{0-7}</td><td>I/O</td><td>Port B, Pins 0-7: An 8-bit data output latch/buffer and an 8-bit data input buffer.</td></tr>
<tr><td>PC_{0-3}</td><td>I/O</td><td>Port C, Pins 0-3: Lower nibble of an 8-bit data output latch/buffer and an 8-bit data input buffer (no latch for input). This port can be divided into two 4-bit ports under the mode control. Each 4-bit port contains a 4-bit latch and it can be used for the control signal outputs and status signal inputs in conjunction with ports A and B.</td></tr>
<tr><td>PC_{4-7}</td><td>I/O</td><td>Port C, Pins 4-7: Upper nibble of Port C.</td></tr>
<tr><td>$\overline{RD}$</td><td>I</td><td>Read Control: This input is low during CPU read operations.</td></tr>
<tr><td>$\overline{WR}$</td><td>I</td><td>Write Control: This input is low during CPU write operations.</td></tr>
<tr><td>RESET</td><td>I</td><td>Reset: A high on this input clears the control register and all ports are set to the input mode.</td></tr>
<tr><td>V_{CC}</td><td>—</td><td>Power: 5V ± 10% DC Supply.</td></tr>
<tr><td>V_{SS}</td><td>—</td><td>Ground: 0V.</td></tr>
</table>

The Control Word Register can be both written and read as shown in the address decode table in the pin descriptions (Table 2). The Control Word format for both read and write operations is shown in Figure 8. Bit D_7 will always be a logic ONE when the Control Word is read, as this implies control word mode information.

Ports A, B, and C

The KS82C55A contains three 8-bit ports (A, B, and C). All three ports can be configured in a wide variety of functional characteristics by the system software, but each also has its own special features.

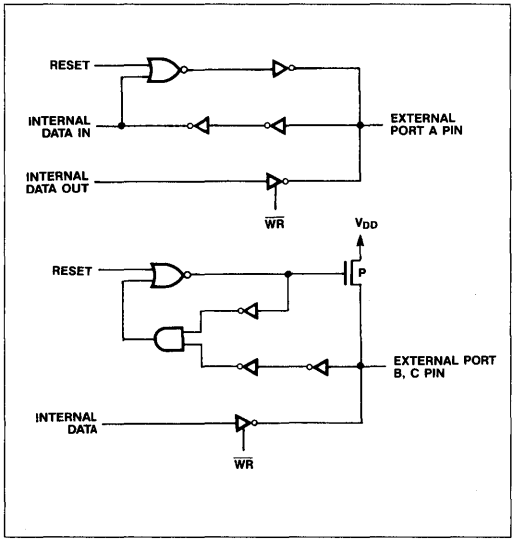
Port A: One 8-bit data output buffer and one 8-bit input buffer. Both pull-up and pull-down bus-hold devices are present on Port A.

Port B: One 8-bit data output buffer and one 8-bit data input buffer. Only pull-up bus-hold devices are present on Port B.

Port C: One 8-bit data output buffer and one 8-bit data input buffer (no latch for input). Port C can be divided into two 4-bit ports under the mode control. Each 4-bit port contains a 4-bit latch and it can be used for the control signal outputs and status signal inputs in conjunction with ports A and B. Only pull-up bus-hold devices are present on Port C.

See Figure 3 for the bus-hold circuit configuration for Ports A, B, and C.

Figure 3: Port A, B, C, Bus-Hold Configuration



OPERATIONAL DESCRIPTION

Mode Selection

There are three basic modes of operation that can be selected by the system software:

- Mode 0 - Basic Input/Output
- Mode 1 - Strobed Input/Output
- Mode 2 - Bidirectional Bus

When the Reset input goes high, all ports will be set to the input mode with all 24 port lines held at a logic one level by the internal bus hold devices. After the reset is removed, no additional initialization is required for the KS82C55A to remain in the input mode. No pull-up or pull-down devices are required. During execution, any of the other modes may be selected by using a single output instruction. This allows a single KS82C55A to service a variety of peripheral devices with a simple software maintenance routine.

The modes for Port A and Port B can be separately defined, while Port C is divided into two portions as required by the Port A and Port B definitions. All of the output registers, including the status flip-flops, will be reset whenever the mode is changed. Modes may be combined such that their functional definition can be tailored to almost any I/O structure. For example, Group B can be programmed in Mode 0 to monitor simple switch closings or display computational results, and Group A could be programmed in Mode 1 to monitor a keyboard or tape reader on an interrupt-driven basis.

Single Bit Set/Reset Feature

Any of the eight bits of Port C can be Set or Reset using a single output instruction. This feature reduces the software requirements in control-based applications.

When Port C is being used as status/control for Port A or B, these bits can be set or reset by using the Bit Set/Reset operation as if they were data output ports.

Interrupt Control Functions

When the KS82C55A is operating in Mode 1 or Mode 2, control signals are provided for use as interrupt request inputs to the CPU. The interrupt request signals, generated from Port C, can be inhibited or enabled by setting or resetting the associated INTE flip-flop using the Bit Set/Reset function of Port C.

This function allows the Programmer to Enable or Disable a specific I/O device to interrupt the CPU without affecting any other device in the interrupt structure.

Figure 4: Mode Definitions & Bus Interface

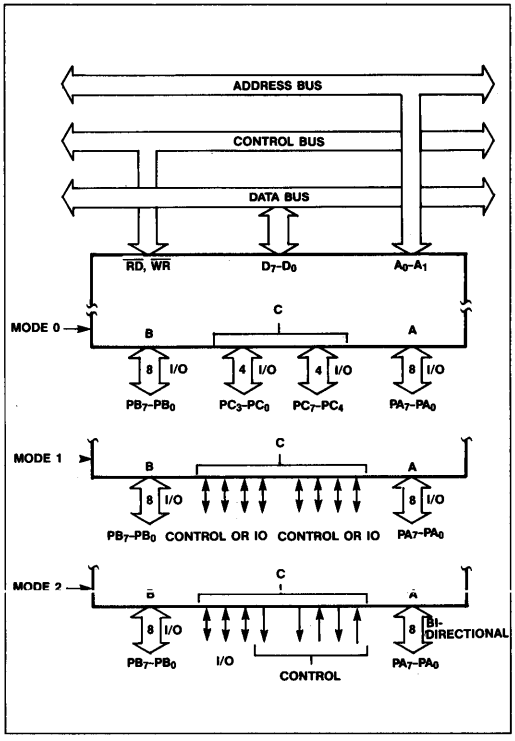
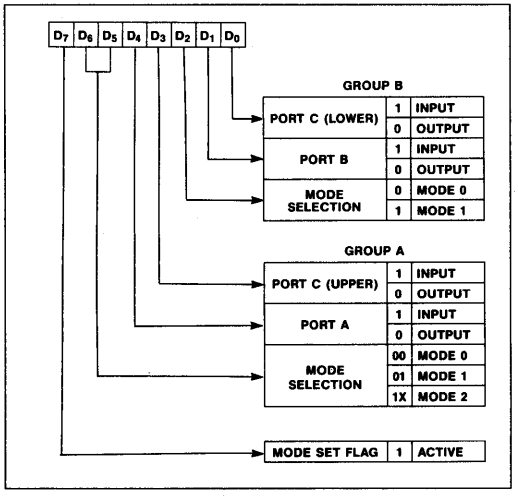


Figure 5: Mode Definition Format



INTE Flip-Flop Definition:

(Bit-Set) - INTE is Set - Interrupt enable
(Bit-Reset) - INTE is Reset - Interrupt disable

Note: All mask flip-flops are automatically reset during mode selection and device reset.

Mode 0 (Basic Input/Output)

This mode provides simple input and output operations for each of the three ports. No handshaking is required. Data is simply written to or read from a specified port.

Mode 0 Basic Functional Definitions:

- Two 8-bit ports and two 4-bit ports
- Any port can be input or output
- Outputs are latched
- Inputs are not latched
- 16 different Input/Output configurations are possible in this mode.

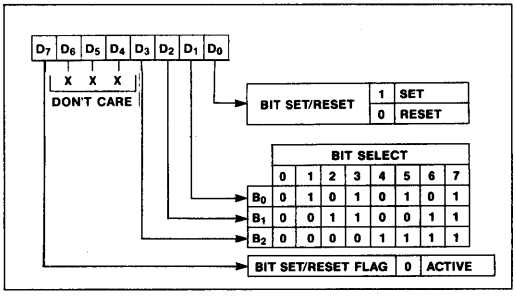
Mode 1 (Strobed Input/Output)

This mode transfers I/O data to or from a specified port in conjunction with strobes or handshaking signals. In Mode 1, Port A and Port B use the lines on Port C to generate or accept these handshaking signals.

Mode 1 Basic Functional Definitions:

- Two Groups (Group A and Group B).
- Each group contains one 8-bit data port and one 4-bit control/data port.
- The 8-bit data port can be either input or output. Both inputs and outputs are latched.
- The 4-bit port is used for control and status of the 8-bit data port.

Figure 6: Bit Set/Reset Format

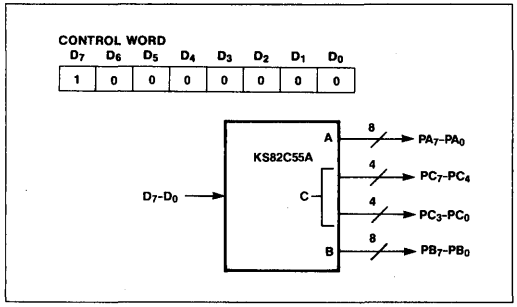


Input Control Signal Definitions

$\overline{STB}$ (Strobe Input): A LOW on this input loads data into the input latch.

IBF (Input Buffer Full F/F): A HIGH on this output indicates that the data has been loaded into the input latch. IBF is set by the STB input being LOW and is RESET by the rising edge of the $\overline{RD}$ input.

Figure 7: Mode 0 Configuration



INTR (Interrupt Request): A HIGH on this output can be used to interrupt the CPU when an input device is requesting service. INTR is set by the $\overline{STB}$ being a ONE, IBF is a ONE, and INTE is a ONE. It is RESET by the falling edge of $\overline{RD}$. This procedure allows an input device to request service from the CPU by simply strobing its data into the Port.

INTE A: Controlled by bit Set/Reset of PC_4.

INTE B: Controlled by bit Set/Reset of PC_2.

Output Control Signal Definition

OBF (Output Buffer Full F/F): The OBF output will go LOW to indicate that the CPU has written data out to the specified port. The OBF F/F will be set by the rising edge of the $\overline{WR}$ input and reset by the ACK input being low.

ACK (Acknowledge Input): A LOW on this input informs the KS82C55A that the data from Port A or Port B has been accepted. (i.e., a response from the peripheral device indicating that it has received the data output by the CPU).

Table 3: Mode 0 Port Definition

Control Word #	Control Word Bits								Port Direction			
		Group A				Group B			Group A		Group B	
	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	PA_7-PA_0	PC_7-PC_4	PC_3-PC_0	PB_7-PB_0
0	1	0	0	0	0	0	0	0	OUTPUT	OUTPUT	OUTPUT	OUTPUT
1	1	0	0	0	0	0	0	1	OUTPUT	OUTPUT	INPUT	OUTPUT
2	1	0	0	0	0	0	1	0	OUTPUT	OUTPUT	OUTPUT	INPUT
3	1	0	0	0	0	0	1	1	OUTPUT	OUTPUT	INPUT	INPUT
4	1	0	0	0	1	0	0	0	OUTPUT	INPUT	OUTPUT	OUTPUT
5	1	0	0	0	1	0	0	1	OUTPUT	INPUT	INPUT	OUTPUT
6	1	0	0	0	1	0	1	0	OUTPUT	INPUT	OUTPUT	INPUT
7	1	0	0	0	1	0	1	1	OUTPUT	INPUT	INPUT	INPUT
8	1	0	0	1	0	0	0	0	INPUT	OUTPUT	OUTPUT	OUTPUT
9	1	0	0	1	0	0	0	1	INPUT	OUTPUT	INPUT	OUTPUT
10	1	0	0	1	0	0	1	0	INPUT	OUTPUT	OUTPUT	INPUT
11	1	0	0	1	0	0	1	1	INPUT	OUTPUT	INPUT	INPUT
12	1	0	0	1	1	0	0	0	INPUT	INPUT	OUTPUT	OUTPUT
13	1	0	0	1	1	0	0	1	INPUT	INPUT	INPUT	OUTPUT
14	1	0	0	1	1	0	1	0	INPUT	INPUT	OUTPUT	INPUT
15	1	0	0	1	1	0	1	1	INPUT	INPUT	INPUT	INPUT

INTR (Interrupt Request): A HIGH on this output can be used to interrupt the CPU when an output device has accepted data transmitted by the CPU. INTR is set when $\overline{ACK}$ is a ONE, $\overline{OBF}$ is a ONE and INTE is a ONE. It is Reset by the falling edge of $\overline{WR}$.

INTE A: Controlled by bit Set/Reset of PC_4.

INTE B: Controlled by bit Set/Reset of PC_2.

Mode 2 (Strobed Bidirectional Bus I/O)

This mode provides a means for communicating with a peripheral device on a single 8-bit bus to facilitate both transmitting and receiving of data (bi-directional bus I/O). Handshaking signals maintain proper bus flow discipline in a similar manner to Mode 1. Interrupt generation and enable/disable functions are also available.

Mode 2 Basic Functional Definitions:

- Used in Group A only.
- One 8-Bit, bi-directional bus port (Port A) and a 5-bit control port (Port C).
- Both inputs and outputs are latched.
- The 5-bit control port (Port C) is used for control and status of the 8-bit, bi-directional bus port (Port A).

Bidirectional Bus I/O Control Signal Definition

INTR (Interrupt Request): A HIGH on this output can be used to interrupt the CPU for input or output operations.

Output Operations

$\overline{OBF}$ (Output Buffer Full): The $\overline{OBF}$ output will go LOW to indicate that the CPU has written data into Port A.

$\overline{ACK}$ (Acknowledge): A LOW on this input enables the 3-state output buffer of Port A to send out the data. Otherwise, the output buffer will be in the high impedance state.

INTE1 (The INTE Flip-Flop Associated with OBF): Controlled by bit Set/Reset of PC_6.

Input Operations

$\overline{STB}$ (Strobe Input): A LOW on this input loads data into the input latch.

IBF (Input Buffer Full F/F): A HIGH on this output indicates that data has been loaded into the input latch.

INTE2 (The INTE Flip-Flop Associated with IBF): Controlled by bit Set/Reset of PC_4.

Figure 8: Mode 1 Input

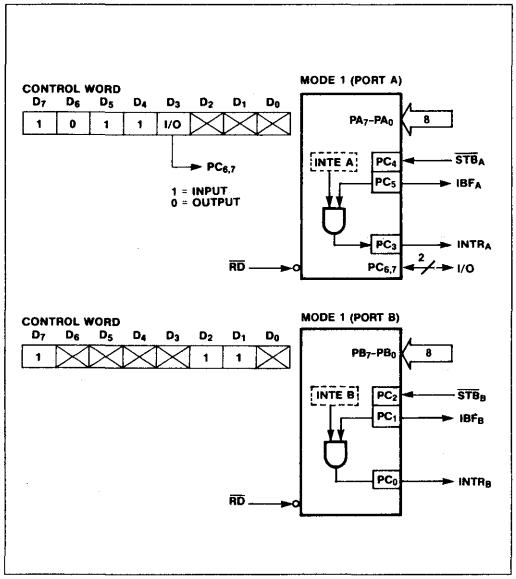
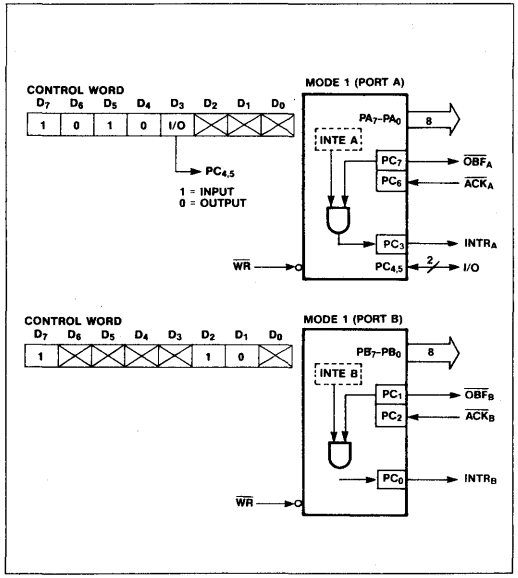


Figure 9: Mode 1 Output



Special Mode Combination Considerations

Several combinations of modes are possible. For any combination, some or all of the Port C lines are used for control or status. The remaining bits are either inputs or outputs as defined by a Set Mode command.

The state of all the Port C lines, except the $\overline{ACK}$ and $\overline{STB}$ lines, will be placed on the data bus during a read of Port C. In place of the $\overline{ACK}$ and $\overline{STB}$ line states, flag status will appear on the data bus in the PC_2, PC_4, and PC_6 bit positions as shown in Table 4.

Through a Write Port C command, only the Port C pins programmed as outputs in a Mode 0 group can be written. No other pins can be affected by a Write Port C command, and the interrupt enable flags cannot be accessed. The Set/Reset Port C Bit command must be used to write to any Port C output programmed as an output in a Mode 1 group or to change an interrupt enable flag.

With a Set/Reset Port C Bit command, any Port C line programmed as an output (including INTR, IBF and $\overline{OBF}$) can be written, or an interrupt enable flag can be set or reset. Port C lines programmed as inputs, including $\overline{ACK}$ and $\overline{STB}$ lines, are not affected by a Set/Reset Port C Bit command. Writing to the corresponding Port C bit positions of the $\overline{ACK}$ and $\overline{STB}$ lines with the Set/Reset Port C Bit command will affect the Group A and Group B interrupt enable flags (see Table 5).

Current Drive Capability

Any output on Port A, B or C can sink or source 2.5mA. Thus the KS82C55A can directly drive Darlington type drivers and high-voltage displays that require such sink or source current.

Reading Port C Status

In Mode 0, Port C transfers data to or from the peripheral device. When the KS82C55A is in Modes 1 or 2, Port C generates or accepts handshaking signals with the peripheral device. Reading Port C allows the programmer to test or verify the status of each peripheral device and change the program flow accordingly.

There is not special instruction to read the status information from Port C. This function is performed by executing a normal read operations of Port C.

Figure 10: Combinations of Mode 1

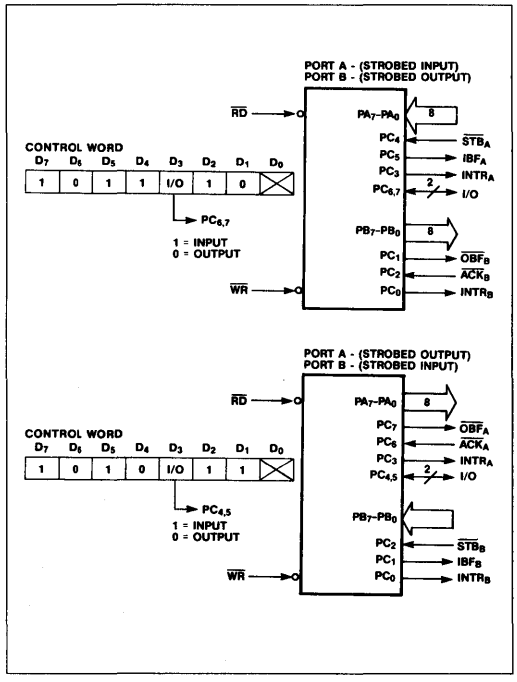


Figure 11: Mode Control Word

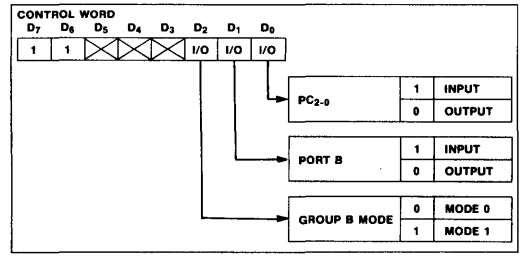


Figure 12: Mode 2

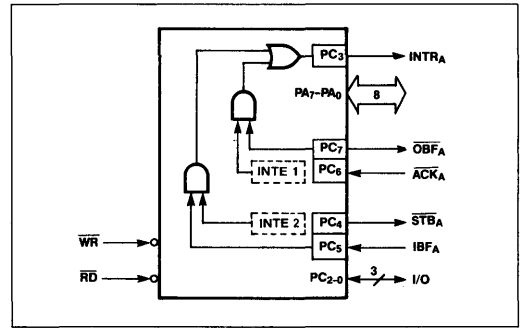


Figure 13: Mode 1/4 Combinations

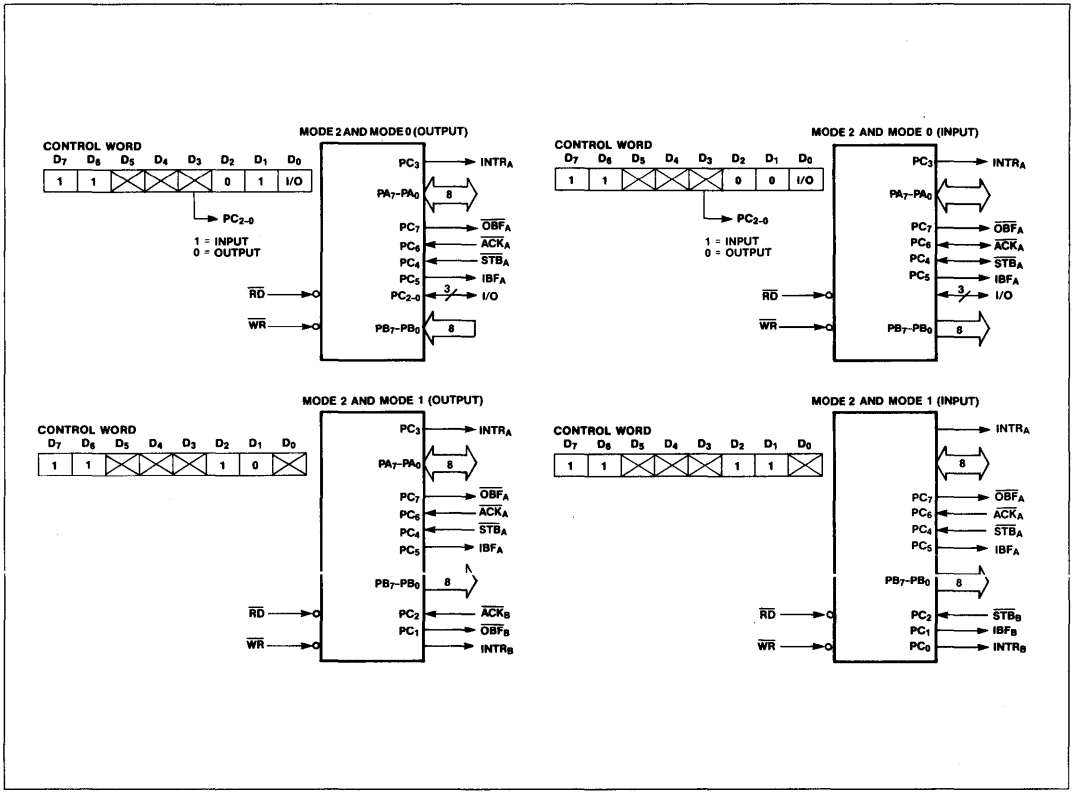


Figure 14: Mode 1 Status Word Format

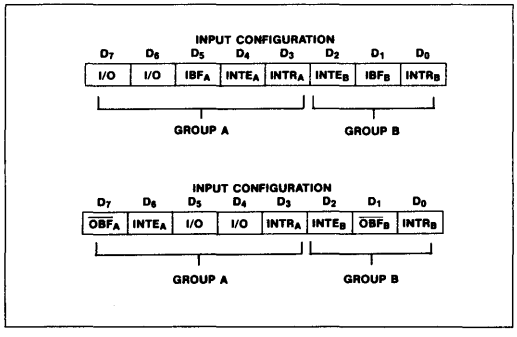


Figure 15: Mode 2 Status Word Format

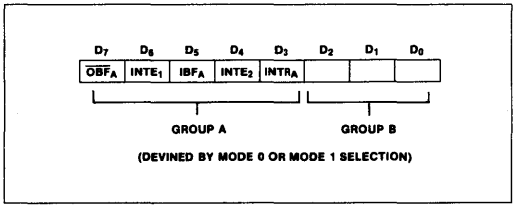


Table 4: Mode Definition Summary

PORT		MODE 0	MODE 1				MODE 2
PORT A	PA_0 PA_1 PA_2 PA_3 PA_4 PA_5 PA_6 PA_7	All IN or All OUT	All IN or All OUT				All BIDIRECTIONAL
PORT B	PB_0 PB_1 PB_2 PB_3 PB_4 PB_5 PB_6 PB_7	All IN or All OUT	All IN or All OUT				MODE 0 or MODE 1 only
			A IN, B IN	A IN, B OUT	A OUT, B IN	A OUT, B OUT	
PORT C	PC_0	All IN	$INTR_B$	$INTR_B$	$INTR_B$	$INTR_B$	I/O
	PC_1	or	IBF_B	OBF_B	IBF_B	OBF_B	I/O
	PC_2	All OUT	STB_B	ACK_B	STB_B	ACK_B	I/O
	PC_3		$INTR_A$	$INTR_A$	$INTR_A$	$INTR_A$	$INTR_A$
	PC_4	All IN	STB_A	STB_A	I/O	I/O	STB_A
	PC_5	or	IBF_A	IBF_A	I/O	I/O	IBF_A
	PC_6	All OUT	I/O	I/O	ACK_A	ACK_A	ACK_A
	PC_7		I/O	I/O	OBF_A	OBF_A	OBF_A

Table 5: Interrupt Enable Flags in Modes 1 and 2

Interrupt Enable Flag	Position	Alternate Port C Pin Signal (Mode)
$INTE_B$	PC_2	$\overline{ACK}_B$ (Output Mode 1) or STB_B (Input Mode 1)
$INTE_{A2}$	PC_4	$\overline{STB}_A$ (Input Mode 1 or Mode 2)
$INTE_{A1}$	PC_6	$\overline{ACK}_A$ (Output Mode 1 or Mode 2)

APPLICATIONS

The KS82C55A is a very powerful device for interfacing peripheral equipment to the microcomputer system. It is flexible enough to interface almost any I/O device without the need for additional external logic.

Each peripheral device in a microcomputer system usually has a service routine associated with it. The routine manages the software interface between the device and the CPU. The functional definition of the KS82C55A is programmed by the I/O service routine and becomes an extension of the system software. By examining the interface characteristics of the I/O device for both data transfer and timing, and matching this information to the examples and tables in the Operational Description, a Control Word can easily be developed to intialize the KS82C55A to exactly fit the application. Figures 16 through 22 illustrate a few examples of typical KS82C55A applications.

Figure 16: Keyboard and Display Interface

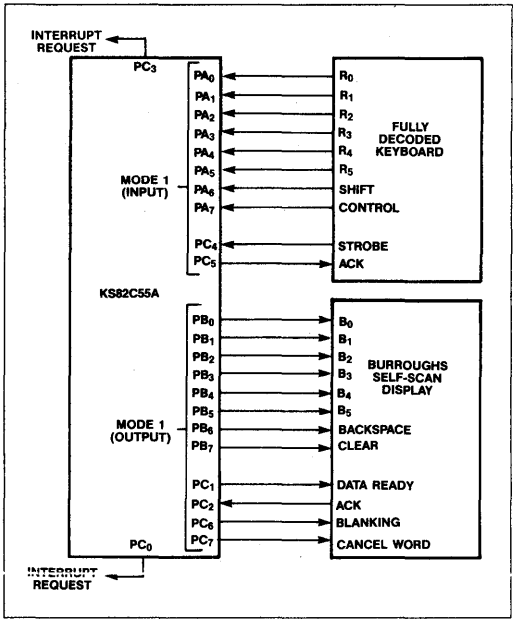


Figure 17: Printer Interface

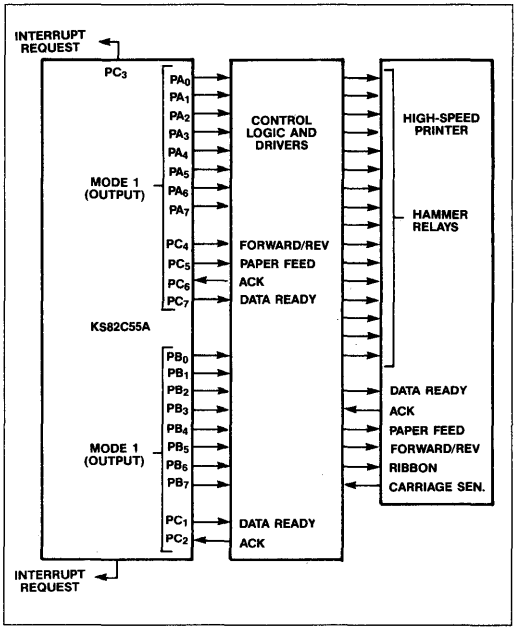


Figure 18: Keyboard and Terminal Address Interface

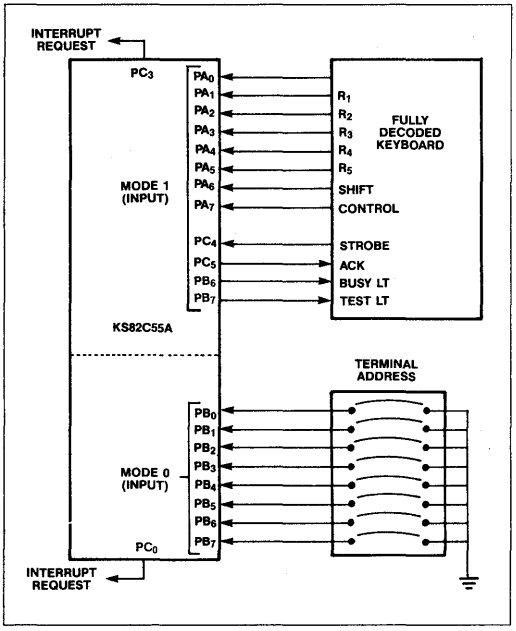


Figure 19: D/A, A/D

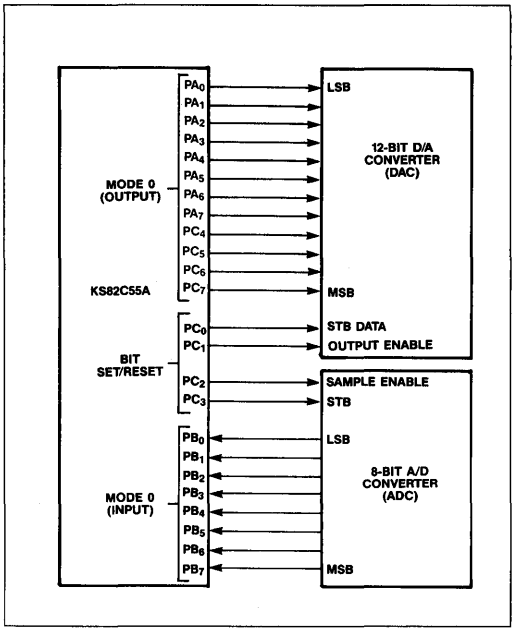


Figure 20: Basic Floppy Disc Interface

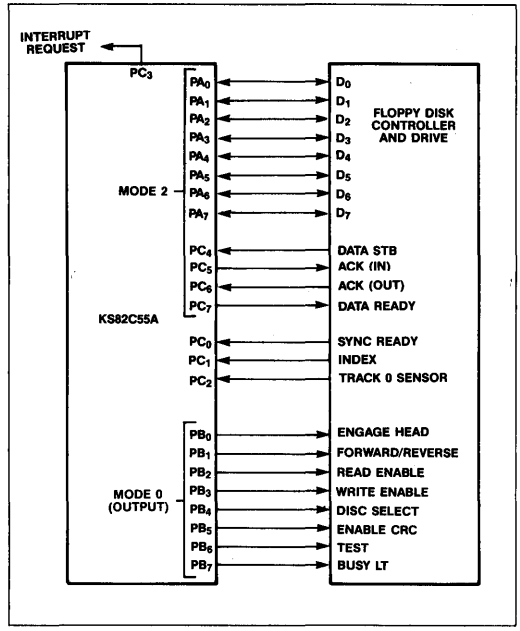


Figure 21: Basic CRT Controller Interface

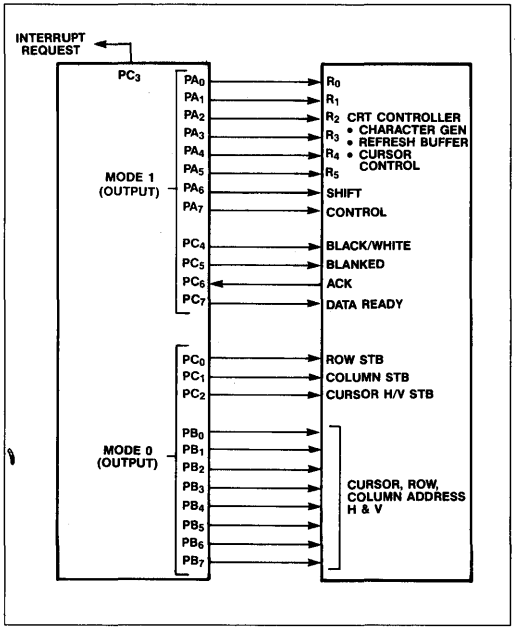


Figure 22: Machine Tool Controller

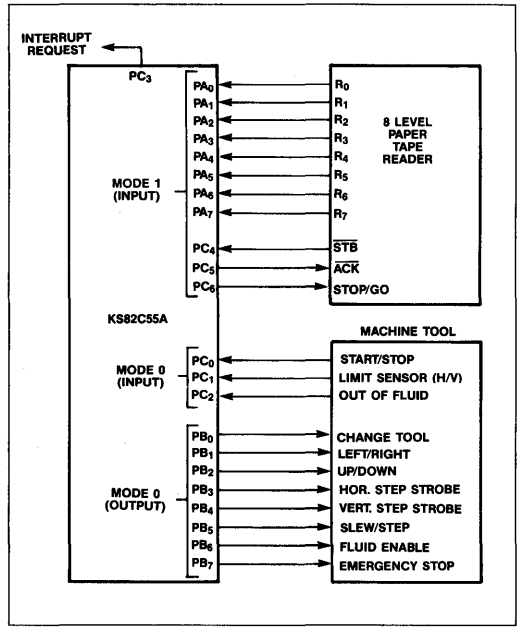


Table 6: Recommended Operating Conditions

DC Supply Voltage		+4.0V to +6.0V
Operating Temperature Range	Commercial	0°C to 70°C
	Industrial	-40°C to +85°C

Table 7: Absolute Maximum Ratings

DC Supply Voltage	+7.0V
Input, Output or I/O Voltage Applied	V_{SS} - 0.5V to V_{CC} + 0.5V
Storage Temperature Range	-65°C to +150°C
Maximum Package Power Dissipation	1W

Note: Stresses beyond those listed above may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 8: Capacitance (T_A = 25°C, V_{CC} = 0V, V_{IN} = +5V or V_{SS})

Symbol	Parameter	Test Conditions	Typ	Units
$C_{I/O}$	I/O Capacitance	Unmeasured Pins Returned to V_{SS}	20	pF
C_{IN}	Input Capacitance		10	pF

Table 9: DC Characteristics (T_A = 0°C to 70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V)

Symbol	Parameter	Test Conditions	Limits		Unit
			Min	Max	
I_{CC}	V_{CC} Supply Current	(Note 3)		10	mA
I_{CCSB}	V_{CC} Supply Current-Standby	V_{CC} = 5.5V, V_{IN} = V_{CC} or V_{SS} Port Conditions: If I/P = Open/High — O/P = Open Only With Data Bus = High/Low — CS = High — Reset = Low Pure Inputs = Low/High		10	μA
I_{DAR}	Darlington Drive Current	Ports A, B, C R_{EXT} = 750Ω, V_{EXT} = 1.5V	±2.5		mA
I_{IL}	Input Leakage Current	V_{IN} = V_{CC} to 0V (Note 1)		±1	μA
I_{OFL}	Output Float Leakage Current	V_{IN} = V_{CC} to 0V (Note 2)		±10	μA
I_{PHH}	Port Hold High Leakage Current	V_{OUT} = 3.0V (Ports A, B, C)	-50	-300	μA
I_{PHHO}	Port Hold High Overdrive Current	V_{OUT} = 3.0V	+350		μA
I_{PHL}	Port Hold Low Leakage Current	V_{OUT} = 1.0V (Port A Only)	+50	+300	μA
I_{PHLO}	Port Hold Low Overdrive Current	V_{OUT} = 0.8V	-350		μA
V_{IH}	Input High Voltage		2.0	V_{CC}	V
V_{IL}	Input Low Voltage		-0.5	0.8	V
V_{OH}	Output High Voltage	I_{OH} = -2.5mA I_{OH} = -100μA	3.0 V_{CC} - 0.4		V V
V_{OL}	Output LOW Voltage	I_{OL} = 2.5mA		0.4	V

Notes: 1. Pins A1, A0, $\overline{CS}$, $\overline{WR}$, $\overline{RD}$, Reset. 2. Data Bus; Ports B, C. 3. Outputs Open.

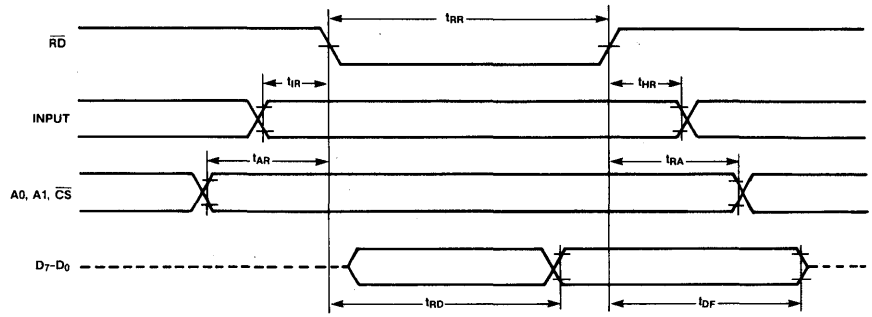
Table 10: AC Characteristics (T_A = 0°C to 70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V)

Symbol	Parameter	Test Conditions	Limits (8MHz)		Limits (10MHz)		Units
			Min	Max	Min	Max	
t_{AD}	$\overline{ACK}$ = 0 to Output			175		125	ns
t_{AIT}	$\overline{ACK}$ = 1 to INTR = 1			150		100	ns
t_{AK}	$\overline{ACK}$ Pulse Width		200		100		ns
t_{AOB}	$\overline{ACK}$ = 0 to $\overline{OBF}$ = 1			150		100	ns
t_{AR}	Address Strobe Before $\overline{RD}$↓		0		0		ns
t_{AW}	Address Strobe Before $\overline{WR}$↓		0		0		ns
t_{DF}	$\overline{RD}$ ≠ Data Floating $\overline{RD}$↑ to Data Floating		10	75	10	75	ns
t_{DW}	Data Setup Time Before $\overline{WR}$↑		100		50		ns
t_{HR}	Peripheral Data After $\overline{RD}$		0		0		ns
t_{IR}	Peripheral Data Before $\overline{RD}$		0		0		ns
t_{KD}	$\overline{ACK}$ = 1 to Output Float		20	250	20	175	ns
t_{PH}	Peripheral Data After $\overline{STB}$ High		50		40		ns
t_{PS}	Peripheral Data Before $\overline{STB}$ High		20		20		ns
t_{RA}	Address Hold Time After $\overline{RD}$↑		0		0		ns
t_{RD}	Data Delay from $\overline{RD}$↓			120		95	ns
t_{RES}	Reset Pulse Width	See Note 2	500		400		ns
t_{RIB}	$\overline{RD}$ = 1 to IBF = 0			150		120	ns
t_{RIT}	$\overline{RD}$ = 0 to INTR = 0			200		160	ns
t_{RR}	$\overline{RD}$ Pulse Width		150		100		ns
t_{RV}	Recovery Time Between $\overline{RD}$/$\overline{WR}$		200		100		ns
t_{SIB}	$\overline{STB}$ = 0 to IBF = 1			150		100	ns
t_{SIT}	$\overline{STB}$ = 1 to INTR = 1			150		100	ns
t_{ST}	$\overline{STB}$ Pulse Width		100		50		ns
t_{WA}	Address Hold Time After $\overline{WR}$↑	Ports A & B Port C	20 20		10 10		ns ns
t_{WB}	$\overline{WR}$ = 1 to Output			350		150	ns
t_{WD}	Data Hold Time After $\overline{WR}$↑	Ports A & B Port C	30 30		20 20		ns ns
t_{WIT}	$\overline{WR}$ = 0 to INTR = 0	See Note 1		200		160	ns
t_{WOB}	$\overline{WR}$ = 1 to $\overline{OBF}$ = 0			150		120	ns
t_{WW}	$\overline{WR}$ Pulse Width		100		70		ns

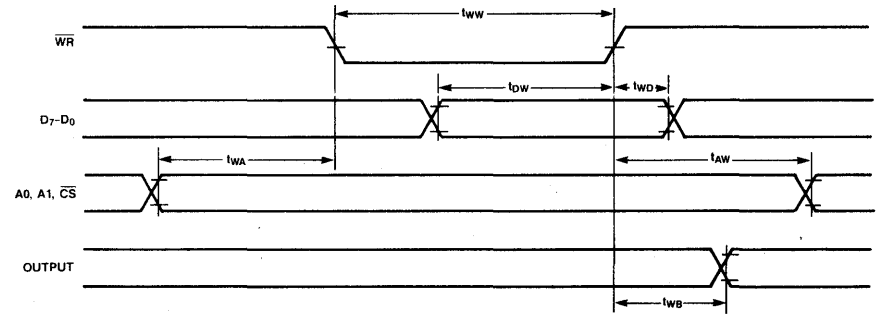
Notes: 1. INTR↑ may occur as early as $\overline{WR}$↓.
2. Width of initial Reset pulse after power on must be at least 50μsec. Subsequent Reset pulses may be 500ns minimum.

Figure 23: Timing Diagrams

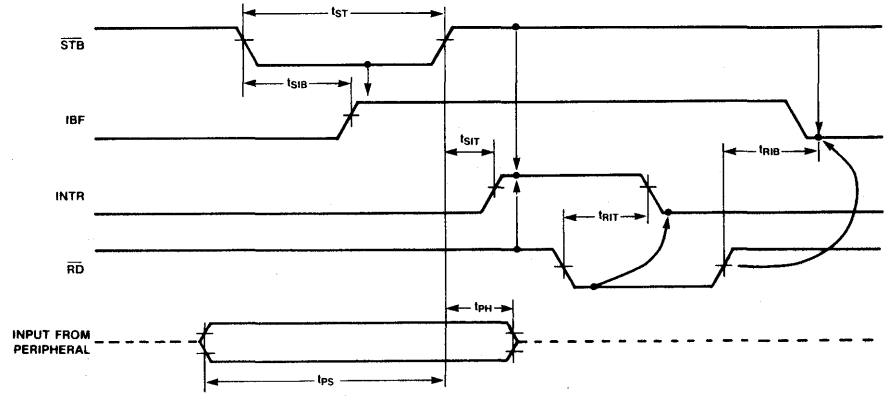
a) Mode 0 (Basic Input)



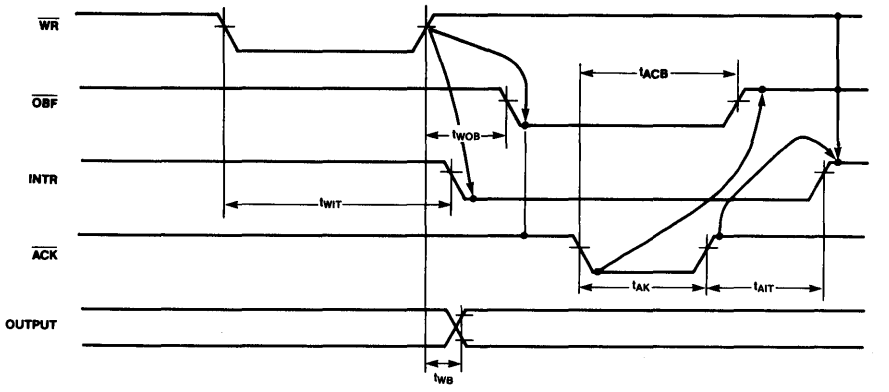
b) Mode 0 (Basic Output)



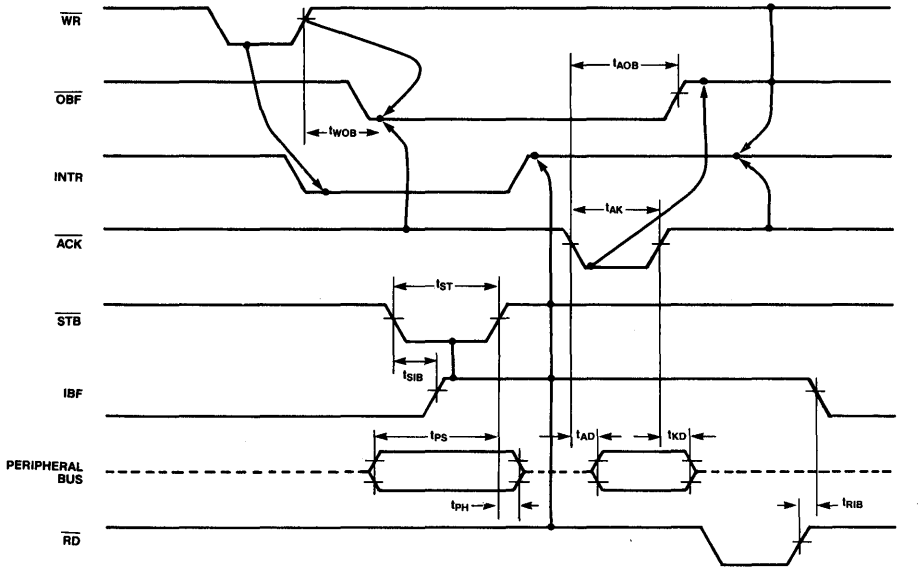
c) Mode 1 (Strobed Input)



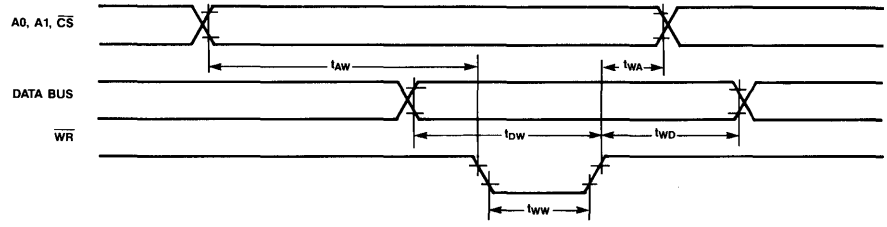
d) Mode 1 (Strobed Output)



e) Mode 2 (Bidirectional)



f) Write Timing



g) Read Timing

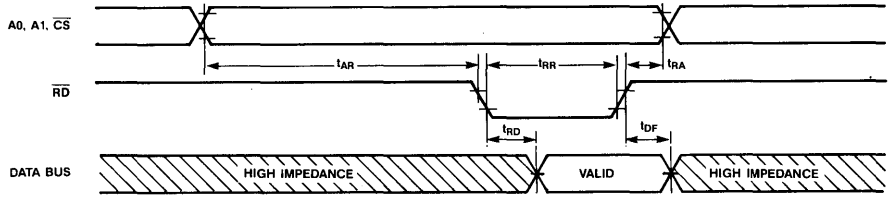
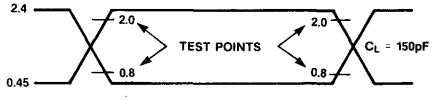
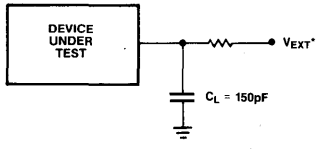


Figure 24: AC Testing I/O Waveform



A.C. Testing Inputs are driven at 2.4V for a logic 1 and 0.45V for a logic 0. Timing measurements are made at 2.0V for a logic 1 and 0.8V for logic 0.

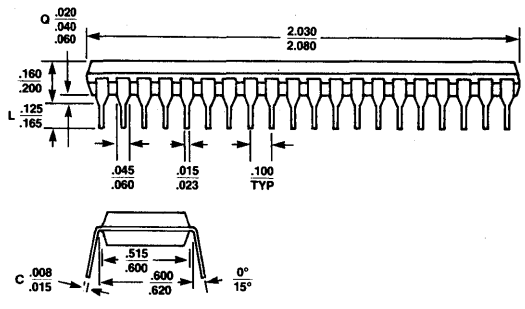
Figure 25: AC Testing Load Circuit



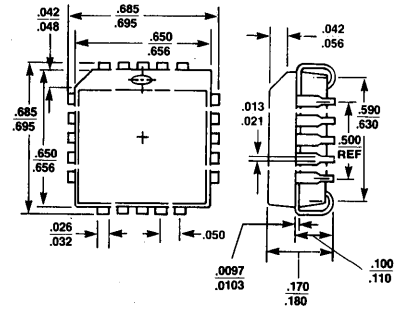
* V_{EXT} is set at various voltages during testing to guarantee the specification. C_L includes jig capacitance.

PACKAGE DIMENSIONS

Units: Inches



Plastic Package



PLCC Package

ORDERING INFORMATION & PRODUCT CODE DIMENSIONS

KS 82C55A X X X

SAMSUNG SEMICONDUCTOR

Part Number

Speed
-8 8MHz
-10 10MHz

Packaging
P — Plastic DIP
L — Plastic Leaded Chip Carrier (PLCC)

Temperature
C — Commercial (0°C to +70°C)
I — Industrial (-40°C to +85°C)

SAMSUNG products are designated by a Product Code. When ordering, please refer to products by their full code. For unusual, and/or specific packaging or processing requirements not covered by the standard product line, please contact the SAMSUNG MOS Products Group.

KS82C59A

PROGRAMMABLE INTERRUPT CONTROLLER

FEATURES

- **Pin and functional compatibility with the industry standard 8259/8259A**
- **TTL input/output compatibility**
- **Low power CMOS implementation**
- **Compatible with 8080/85, 8086/88, 80286/386 and 68000 family microprocessor systems**
- **Eight level priority controller**
- **Expandable to 64 levels**
- **Programmable interrupt modes, with each interrupt maskable**
- **Edge- or level-triggered interrupt request inputs**
- **Polling operation**
- **Fully static design**

DESCRIPTION

The KS82C59A is a high performance, completely programmable interrupt controller. It can process eight interrupt request inputs, assigning a priority level to each one, and is cascadable up to 64 interrupt requests. Individual interrupting sources are maskable. Its two modes of operation (Call and Vector) allow it to be used with a wide variety of microprocessors.

Featuring fully static, very high speed operation, the KS82C59A is designed to relieve the system CPU from polling in a multi-level priority interrupt system. Its very low power consumption makes it useful in portable systems and systems with low power standby modes.

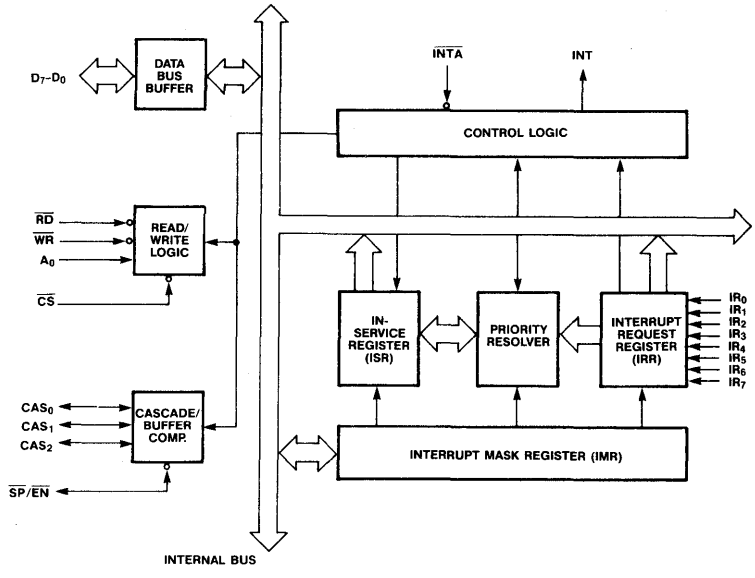


Figure 1: Block Diagram of KS82C59A

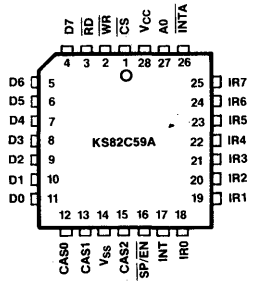


Figure 2a: 28-Lead PLCC

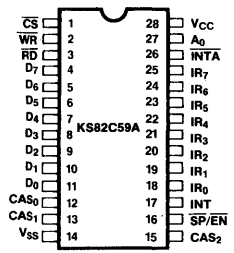


Figure 2b: Pin Configuration

Table 1: Pin Descriptions

Symbol	Pin (28-Pin DIP)	Type	Name and Function
A_0	27	I	**A_0 Address Line:** This signal acts in conjunction with the $\overline{CS}$, $\overline{WR}$ and $\overline{RD}$ signals. It is used by the KS82C59A to decipher various Command Words written by the CPU, and Status information read by the CPU. It is typically connected to the CPU-A_0 address line.
CAS_{0-2}	12, 13, 15	I/O	**Cascade Line:** These signals are outputs for the master KS82C59A, and inputs for slaved KS82C59As. The CAS lines are used as a private bus by a KS82C59A master to control a multiple KS82C59A system structure.
$\overline{CS}$	1	I	**Chip Select:** An active LOW signal used to enable $\overline{RD}$ and $\overline{WR}$ communication between the CPU and the KS82C59A. Note that $\overline{INTA}$ functions are independent of $\overline{CS}$.
D_7-D_0	4-11	I/O	**Data Bus:** Bidirectional, 3-state, 8-bit data bus for the transfer of control, status and interrupt vector information.
INT	17	O	**Interrupt:** This signal goes HIGH when a valid interrupt request is asserted. It is used to interrupt the CPU, thus, it is connected to the CPU's interrupt pin.
$\overline{INTA}$	26	I	**Interrupt Acknowledge:** Signal used to enable the KS82C59A interrupt vector data onto the data bus by a sequence of interrupt acknowledge pulses issued by the CPU.
IR_{0-7}	18-25	I	**Interrupt Requests:** Asynchronous input signals. An interrupt request is executed by raising an IR input (LOW to HIGH), and holding it HIGH until it is acknowledged (Edge Triggered Mode), or just by a HIGH level on an IR input (Level Triggered Mode).
$\overline{RD}$	3	I	**Read:** Active LOW signal used to enable the KS82C59A to output status information onto the data bus for the CPU.
$\overline{SP}/\overline{EN}$	16	I/O	**Slave Program/Enable Buffer:** Active LOW, dual function control signal. When in the *Buffered Mode* its can be used as an output to control buffer transceivers ($\overline{EN}$). When not in the buffered mode it is used as an input to designate a master (SP = 1) or a slave (SP = 0).
V_{CC}	28	—	**Power:** 5V ± 10% DC Supply.
V_{SS}	14	—	**Ground:** 0V.
$\overline{WR}$	2	I	**Write:** Active LOW signal used to enable the KS82C59A to accept command words from the CPU.

FUNCTIONAL DESCRIPTION

The KS82C59A Programmable Interrupt Controller is designed for use in interrupt-driven micro-computer systems. Acting as an overall peripherals manager, its functions include:

- Accepting interrupt requests from assorted peripheral devices
- Determining which is the highest priority
- Establishing whether or not the new interrupt is of a higher priority than any interrupt which might be currently being serviced, and if so,
- Issuing an interrupt to the CPU
- Then providing the CPU with the *interrupt service routine* address of the interrupting peripheral

Each peripheral device usually has a specific interrupt service routine which is particular to its operational or functional requirements within the system. The KS82C59A can be programmed to hold a pointer to the service routine addresses associated with each of the peripheral devices under its control. Thus when a peripheral interrupt is passed through to the CPU, the KS82C59A can set the CPU Program Counter to the interrupt service routine required. These *pointers* (or vectors) are addresses in a vector table.

The KS82C59A is intended to run in one of two major operational modes, according to the type of CPU being used in the system. The *CALL Mode* is used for 8085 type microprocessor systems, while the *VECTOR Mode* is reserved for those systems using more sophisticated processors such as the 8088/86, 80286/386 or 68000 family.

In either mode, the KS82C59A can manage up to eight interrupt request levels individually, with a maximum capability of up to 64 interrupt request levels when cascaded with other KS82C59As. A selection of priority modes is also available such that interrupt requests can be processed in a number of different ways to meet the requirements of a varity of system configurations.

Priority modes can be changed or reconfigured dynamically at any time during system operation using the operation command words (OCWs), allowing the overall interrupt structure to be defined for a complete system. Note that the KS82C59A is programmed by the system software *as an I/O peripheral.*

The major functional components of the KS82C59A are laid out in the block diagram of Figure 1. Vector data and device programming information are transferred from the system bus to the KS82C59A via the 3-state, bi-directional Data Bus Buffer which is connected to the internal bus of the controller. Control data between the KS82C59A and the CPU, and between master and slave KS82C59A devices, is managed by one of three functional blocks:

- The Read/Write Control block processes CPU-initiated reads and writes to the KS82C59A registers
- The Control Logic block receives and generates the signals that control the sequence of events during an interrupt
- The Cascade Control block is used to operate a private bus (CAS_0-CAS_2) connecting a master and up to 8 slave KS82C59As.

Programming data passed over the system bus is saved in the initialization and Command Word Registers. Note that the contents of these registers cannot be read back by the CPU.

Peripheral interrupt requests (IR_0-IR_7) are handled by the functional blocks comprising the Interrupt Request Register (IRR), the Interrupt Mask Register (IMR), the In-Service Register (ISR) and the Priority Decision Logic block. Interrupt requests are received at the IRR, the IMR masks those interrupts which cannot be accepted by the KS82C59A, and the ISR shows those interrupt priority levels which are being serviced. These three registers can all be read by the CPU under software control. The Priority Decision Logic block determines which interrupt will be processed next according to a variety of indicators which include the current priority, mode status, current interrupt mask and interrupt service status.

The actual operation of the KS82C59A and its many modes are described in the section following device specifications and characteristics.

OPERATIONAL DESCRIPTION

The KS82C59A is designed to operate in one of two mutually exclusive modes, selected according to the type of system processor used: **Call Mode** for 8080/85 type processors, and **Vector Mode** for 8088/86 and 80286/386 type processors. The major difference between

these two modes is the way in which interrupt service routine address data is passed to the system CPU. Unless specifically programmed to the contrary, the KS82C59A defaults to the CALL Mode of operation, (see section on Programming).

Call Mode

In CALL mode, the *interrupt service routine address* is passed in two steps, in response to three Interrupt Acknowledge ($\overline{INTA}$) signals sent by the CPU to the KS82C59A. In a system containing a single Interrupt Controller, the sequence of steps to respond to a peripheral interrupt request is outlined below, and shown graphically in Figure 4. The itnerrupt service routine addresses are loaded into the KS82C59A during the initialization procedures.

Step	Event Sequence
1	One or more interrupt request lines (IR_0-IR_7) are raised HIGH, setting corresponding IRR bits.
2	The requests are evaluated by the KS82C59A, and if their priority is high enough, and if they are not masked, the INT signal is sent to the CPU.
3	The CPU acknowledges the INT with an interrupt acknowledge ($\overline{INTA}$).
4	On receipt of the first $\overline{INTA}$, the KS82C59A sets the highest priority ISR bit, and resets the corresponding IRR bit. In addition, the KS82C59A sends a CALL instruction 0CDH) to the CPU via the data bus.
5	The CALL instruction causes the CPU to send two more $\overline{INTA}$ signals to the KS82C59A.
6	On receipt of the second $\overline{INTA}$ signal, the KS82C59A sends the low order 8-bit address byte to the CPU via the data bus. On receipt of the third $\overline{INTA}$, the high order address byte is sent to the CPU.
7	This completes the 3-byte CALL instruction procedure. The ISR bit is reset at the end of the interrupt sequence by EOI command, except in the Automatic EOI mode, where the ISR bit is reset automatically at the end of the third $\overline{INTA}$.

Vector Mode

In VECTOR mode, the interrupt service routine address is calculated by the CPU from a one byte *interrupt vector* supplied by the KS82C59A. The significant bits T_{7-3} of the interrupt vectors are loaded into the KS82C59A during the initialization procedures.

Note that no data is transferred by the KS82C59A to the CPU at the first $\overline{INTA}$ signal (the KS82C59A data bus buffers are disabled). It is similar to the CALL mode in that this cycle is used for internal operations that freeze the state of the interrupts for priority resolution and leaves the data bus buffers disabled or, in cascaded mode: to issue the interrupt code on the cascade lines (CAS_{0-2}).

The sequence of steps that occur to respond to a peripheral interrupt request in Vector mode are outlined below and illustrated in Figure 7.

Step	Event Sequence
1	One or more interrupt request lines (IR_0-IR_7) are raised HIGH, setting corresponding IRR bits.
2	The requests are evaluated by the KS82C59A, and if their priority is high enough, and if they are not masked, an INT signal is sent to the CPU.
3	The CPU acknowledges the INT with an interrupt acknowledge ($\overline{INTA}$).
4	Upon receipt of the first $\overline{INTA}$ signal from the CPU, the KS82C59A sets the highest priority ISR bit and resets the corresponding IRR bit. The KS82C59A data bus buffer is *not* active during this cycle (high impedance state).
5	Upon receipt of the second $\overline{INTA}$ signal generated by the CPU, the KS82C59A sends an 8-bit *interrupt vector* to the CPU via the data bus.
6	This completes the 1-byte VECTOR mode procedure. In the Automatic End-of-Interrupt (AEOI) mode, the ISR bit is reset at the end of the second $\overline{INTA}$. In EOI mode, the ISR bit remains set until an appropriate EOI command is received at the end of the interrupt sequence.

The interrupt sequence procedures, when several KS82C59As are cascaded together, is shown for both CALL and VECTOR modes in Figures 5 and 8, respectively.

Figure 4: CALL Mode Operation (Single KS82C59A Systems)

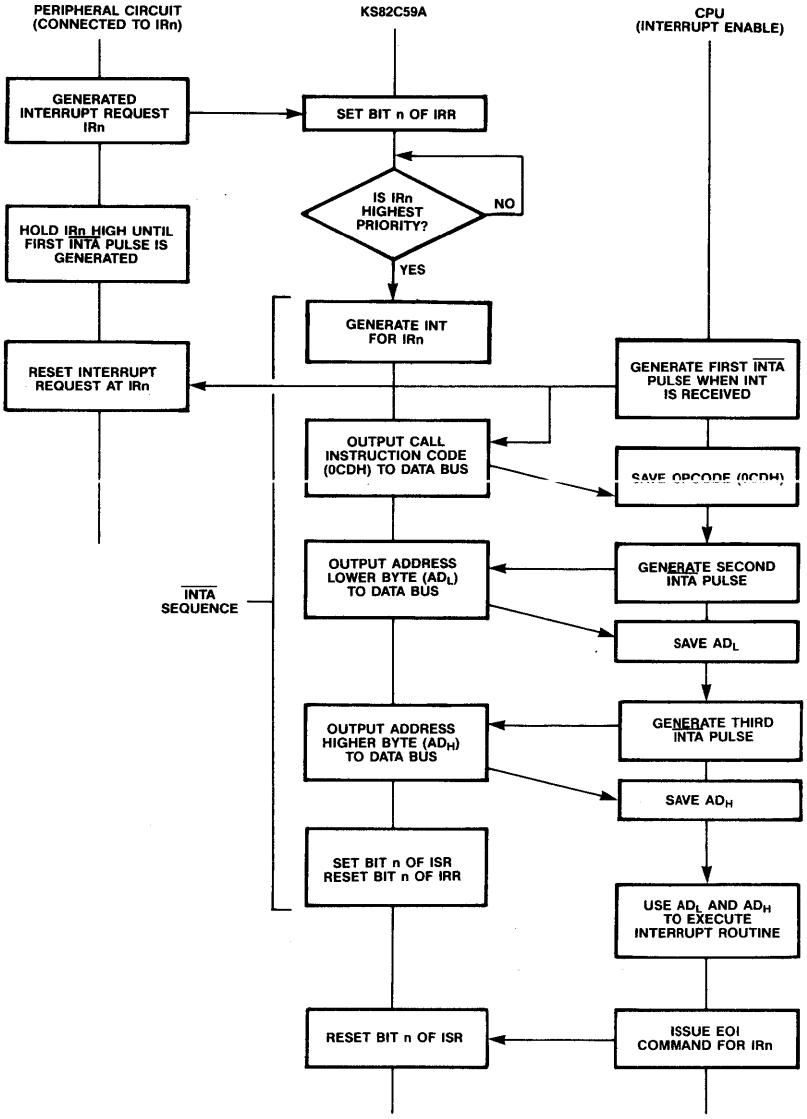


Figure 5: CALL Mode Operation (Cascaded KS82C59A Systems)

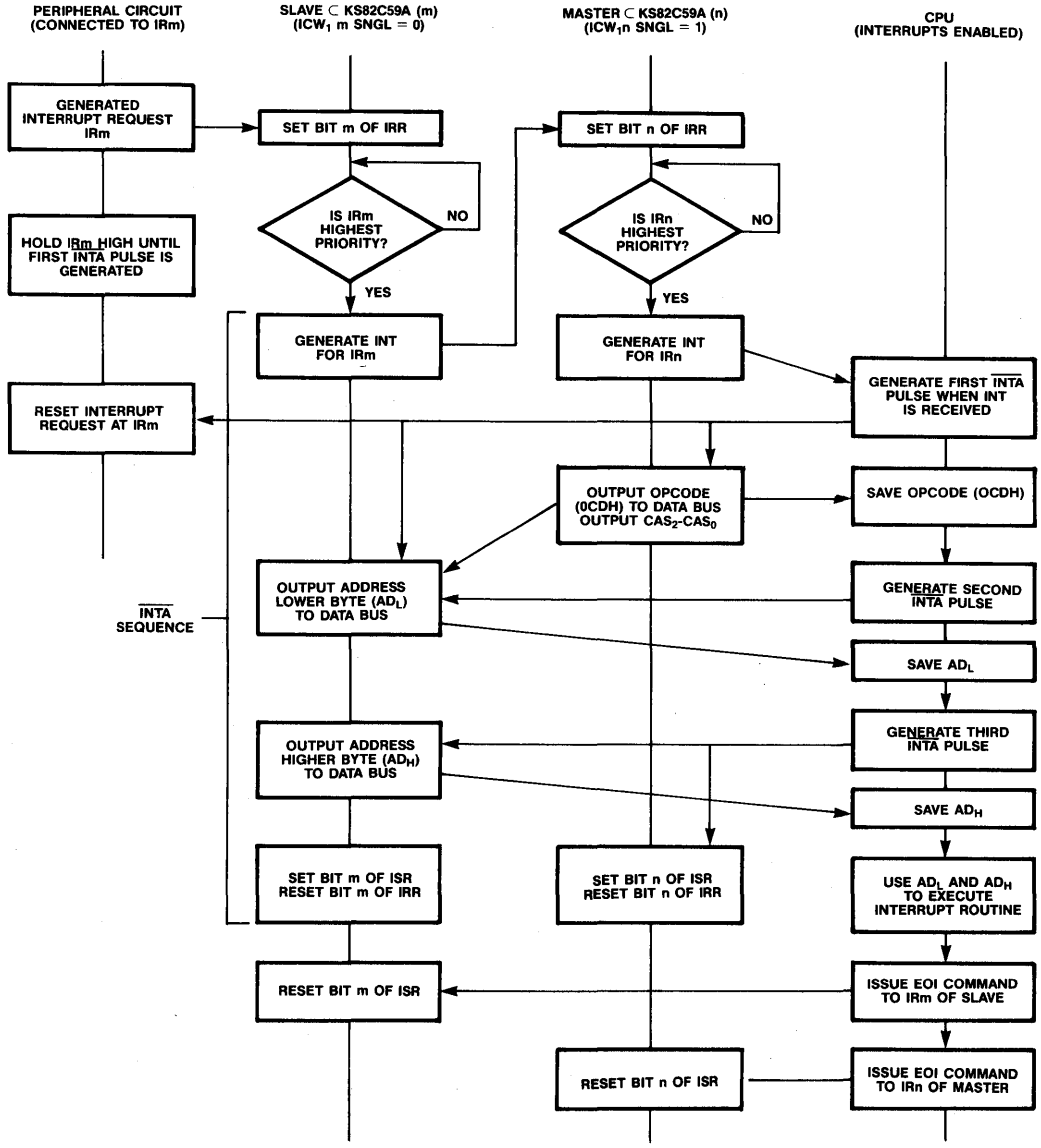


Figure 6: CALL Mode Address Byte Sequence

CONTENTS OF FIRST INTERRUPT VECTOR BYTE

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
CALL CODE	1	1	0	0	1	1	0	1

The lower address of the appropriate service routine is enabled onto the data bus during the second INTA pulse.

When the *Interval = 4*, bits A_5-A_7 are programmed, and A_0-A_4 are inserted automatically by the KS82C59A.

When the *Interval = 8*, bits A_6 and A_7 only are programmed, with A_0-A_5 inserted automatically by the KS82C59A.

CONTENTS OF SECOND INTERRUPT VECTOR BYTE

IR	INTERVAL = 4							
	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
7	A_7	A_6	A_5	1	1	1	0	0
6	A_7	A_6	A_5	1	1	0	0	0
5	A_7	A_6	A_5	1	0	1	0	0
4	A_7	A_6	A_5	1	0	0	0	0
3	A_7	A_6	A_5	0	1	1	0	0
2	A_7	A_6	A_5	0	1	0	0	0
1	A_7	A_6	A_5	0	0	1	0	0
0	A_7	A_6	A_5	0	0	0	0	0

IR	INTERVAL = 8							
	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
7	A_7	A_6	1	1	1	0	0	0
6	A_7	A_6	1	1	0	0	0	0
5	A_7	A_6	1	0	1	0	0	0
4	A_7	A_6	1	0	0	0	0	0
3	A_7	A_6	0	1	1	0	0	0
2	A_7	A_6	0	1	0	0	0	0
1	A_7	A_6	0	0	1	0	0	0
0	A_7	A_6	0	0	0	0	0	0

During the third INTA pulse, the higher address of the appropriate service routine is enabled onto the bus. This address was initially programmed as byte 2 of the initialization sequence (A_8-A_{15}).

CONTENTS OF THIRD INTERRUPT VECTOR BYTE

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8

Figure 7: Vector Mode Operation (Single KS82C59A Systems)

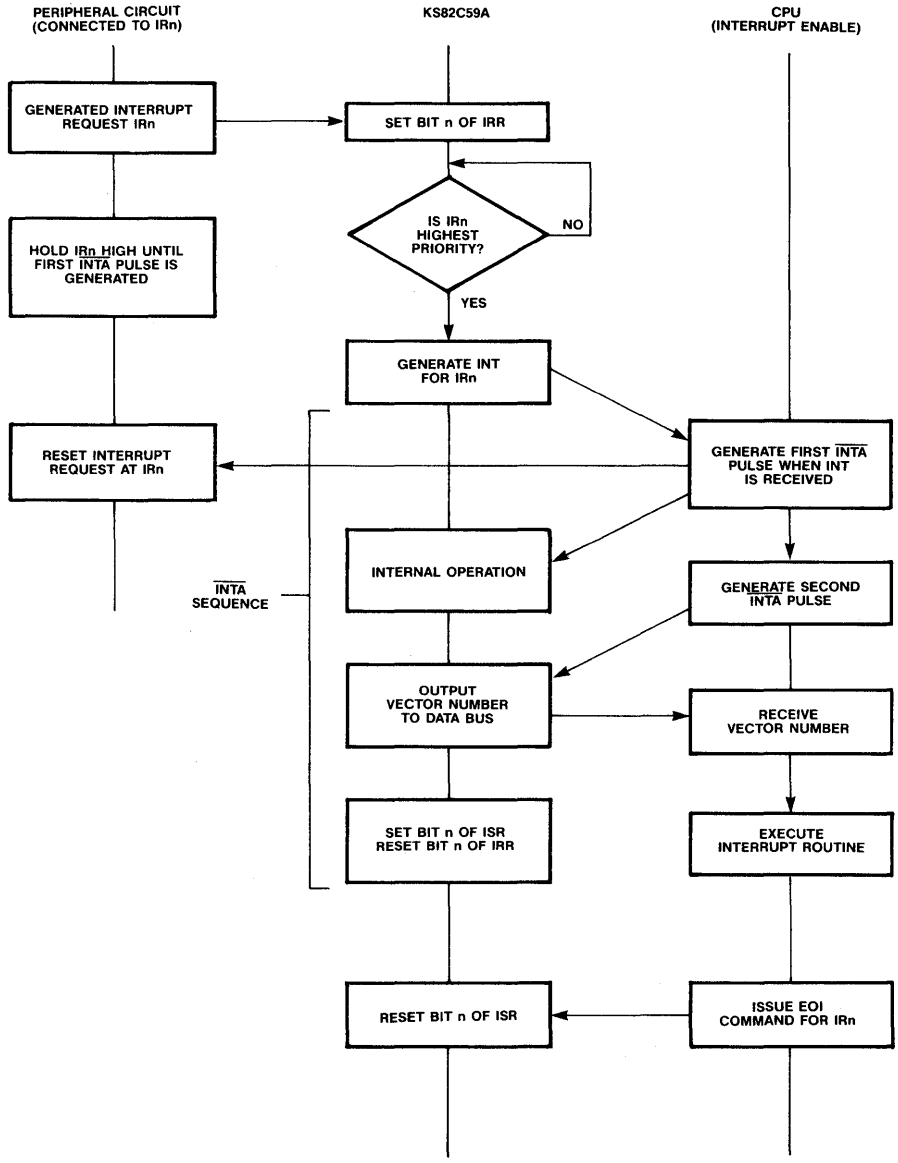


Figure 8: Vector Mode Operation (Cascaded KS82C59A Systems)

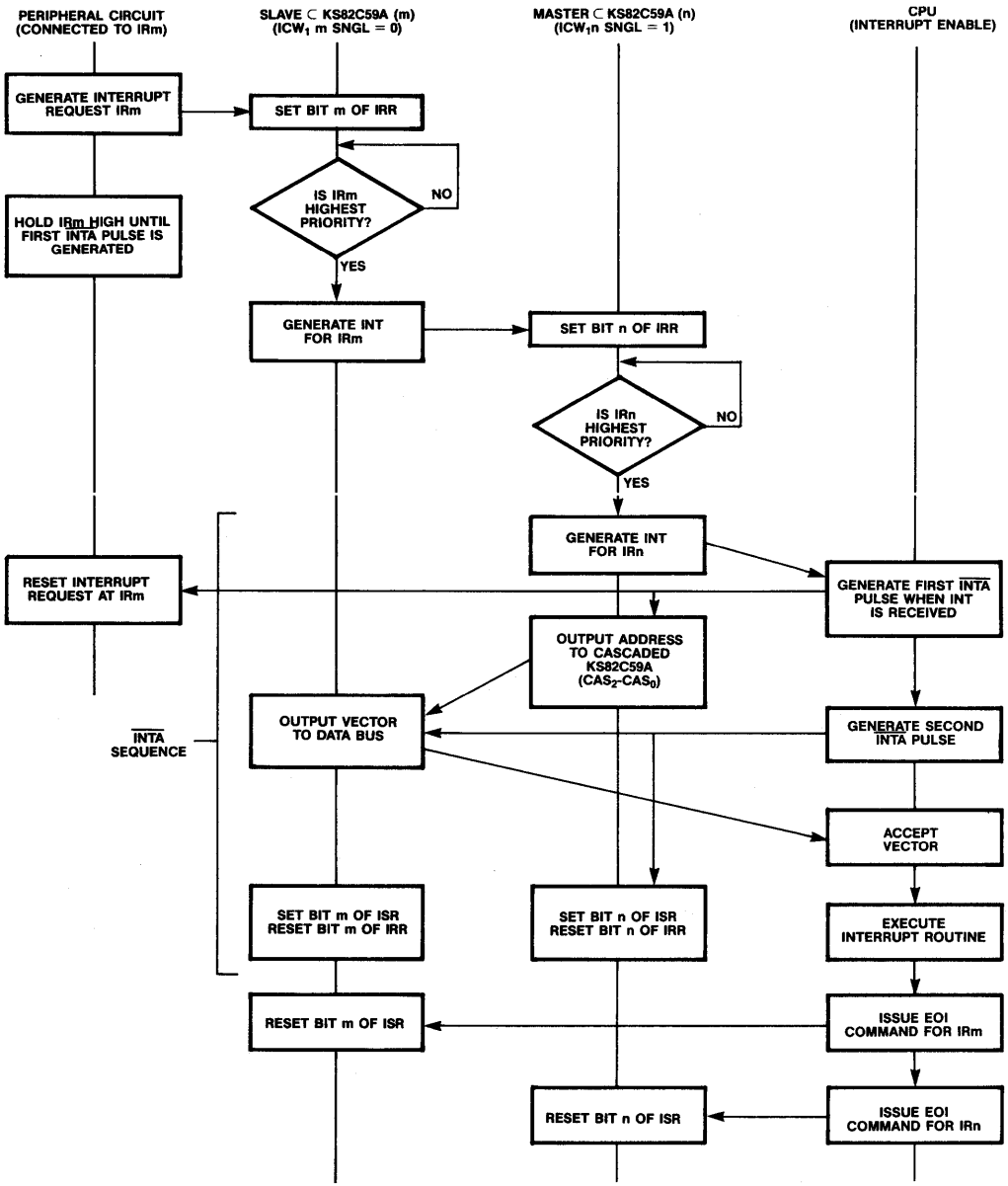


Figure 9: Vector Mode Address Byte

CONTENTS OF FIRST INTERRUPT VECTOR BYTE 8086, 8088, 80286 MODE

IR	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
7	T_7	T_6	T_5	T_4	T_3	1	1	1
6	T_7	T_6	T_5	T_4	T_3	1	1	0
5	T_7	T_6	T_5	T_4	T_3	1	0	1
4	T_7	T_6	T_5	T_4	T_3	1	0	0
3	T_7	T_6	T_5	T_4	T_3	0	1	1
2	T_7	T_6	T_5	T_4	T_3	0	1	0
1	T_7	T_6	T_5	T_4	T_3	0	0	1
0	T_7	T_6	T_5	T_4	T_3	0	0	0

The value T_7 to T_3 is programmed during byte 2 of the initialization (ICW_2).

During the second INTA pulse, the interrupt vector of the appropriate service routine is enabled onto the bus. The low order three bits are supplied by the KS82C59A according to the IR input causing the interrupt.

REGISTERS

The KS82C59A contains a number of registers, used to keep track of interrupts which are being serviced, or pending, as well as those which are masked. These registers are described in Table 7. They can be written to using the *command word* structure, or in the case of IRR, are set by external peripheral devices requesting interrupt service. The contents of all registers can be read by the CPU for status updates (see Table 9).

Table 7: KS82C59A Registers

Symbol	Name	Function
IMR	Interrupt Mask Register	An 8-bit wide register that contains the interrupt request lines which are masked.
IRR	Interrupt Request Register	An 8-bit wide register that contains the levels requesting an interrupt to be acknowledged. The highest request level is reset from the IRR when an interrupt is acknowledged, (not affected by IMR).
ISR	In-Service Register	An 8-bit wide register that contains the priority levels which are being serviced. The ISR is updated when an *End of Interrupt* Command (EOI) is received.

Table 8: Register Read/Write Operations

Operations			Bit Programming			
KS82C59A	CPU	Other Conditions	$\overline{CS}$	$\overline{RD}$	$\overline{WR}$	A_0
IRR to Data Bus ISR to Data Bus	IRR Read ISR Read	IRR set by OCW_3 ISR set by OCW_3	0	0	1	0
Polling data to Data Bus	Polling	Polling data is read instead of IRR and ISR				
IMR to Data Bus	IMR Read		0	0	1	1
Data Bus to ICW_1 Reg. Data Bus to OCW_2 Reg. Data Bus to OCW_3 Reg.	ICW_1 Write OCW_2 Write OCW_3 Write	Set ICW_1 (D_4 = 1) Set OCW_2 (D_4, D_3 = 0) Set OCW_3 (D_4 = 0, D_3 = 1)	0	1	0	0
Data Bus to ICW_2 Reg. Data Bus to ICW_3 Reg. Data Bus to ICW_4 Reg.	ICW_2 Write ICW_3 Write ICW_4 Write	Refer to section on Control Words for ICW_2–ICW_4 writing procedure	0	1	0	1
Data Bus to IMR	OCW_1 Write	After initialization				
Data Bus set to High Impedance State			0 1	1 X	1 X	X X
Illegal State			0	0	0	X

PROGRAMMING COMMANDS

The KS82C59A is initialized and programmed with special command words issued by the CPU. These commands fall into two major categories: *Initialization Command Words* (ICW_1–ICW_4), and *Operational Command Words* (OCW_1–OCW_3). Initialization commands are used to bring the KS82C59A to a known state when the system is first activated, or after a system restart.

Operational commands are used once the KS82C59A is in operation (and *after* it has been initialized), to set, or alter specific interrupt program modes. The format and use of these two command types is described below.

INITIALIZATION COMMANDS

The KS82C59A is initialized by a sequence of 2 to 4 command words (ICWs), where the actual number of commands sent depends on the system configuration, and the initial operating modes to be programmed. Note that *each* KS82C59A in the system *must* be initialized before operations begin in earnest (Figure 11).

The initialization sequence is started when the CPU sends $A_0 = 0$ and ICW_1 with $D_4 = 1$ (Figure 10). During initialization, the events below occur automatically:

- Edge sense circuit is reset. Thus, after initialization, an interrupt request must make a LOW-to-HIGH transition to be recognized.
- IMR is cleared (Interrupts enabled).
- The priority of IR_7 is set to 7 (the lowest priority).
- Special Mask Mode is reset.
- Status read is set to IRR.
- If SNGL bit of $ICW_1 = 1$, then no ICW_3 will be issued.
- If IC_4 bit of $ICW_1 = 0$, then functions selected in ICW_4 are reset: Non-buffered Mode, no Automatic EOI, Call Mode operation.
- If $IC_4 = 1$, then KS82C59A will expect ICW_4.

Bit Definitions (ICW_1, ICW_2)

- IC_4 — Set if ICW_4 is to be issued. This bit *must* be set for systems operating in Vector Mode.
- SNGL — Set if this KS82C59A is not cascaded to other KS82C59As in the system (ICW_3 not issued). When KS82C59As are cascaded, SNGL is reset and ICW_3 is issued.
- ADI — CALL Address Interval. If ADI = 1, then interval = 4. If ADI = 0, then interval = 8.
- LTIM — Level Trigger Mode. If LTIM = 1, edge detect logic on the IR inputs is disabled, and the KS82C59A operates in level triggered mode.
- A_{5-15} — Service routine *Page Starting Address* (Call Mode). In a single KS82C59A system, the 8 interrupt request levels generate CALLs to 8 equally spaced locations in memory. These are spaced at intervals of either 4 or 8 memory locations according to the ADI value. Thus, the vector tables associated with each KS82C59A in the system occupy pages of 32 or 64 byte, respectively.

  Bits A_0–A_4 are automatically inserted to give an address length of 2 bytes (A_0–A_{15}).

  Note that the 8-byte interval is compatible with KS80C85B restart instructions.
- A_{11-15} — Service routine *Vector Address Byte*. In the vector mode, bits A_{11}–A_{15} are inserted in the five most significant places of the vector byte. The three least significant bits are inserted by the KS82C59A according to the interrupt request level. The ADI (Address Interval) and A_5–A_{10} bits are ignored.

Bit Definitions (ICW_3)

This word is read only when SNGL = 0 in ICW_1 (cascading is used).

- **Master Mode:** Sent to the master KS82C59A, each bit of ICW_3 represents a potential slave device connected to an IR input. If a slave exists, the corresponding bit in ICW_3 is set. Where a slave is not attached to an IR input of the master, the corresponding bit is reset.

  In operation, the master outputs byte 1 of the interrupt sequence to the bus, then enables the appropriate slave (via the cascade bus CAS_{0-2}) to output bytes 2 and 3 (Call Mode) or byte 2 only (Vector Mode).
- **Slave Mode:** When sent to a slave KS82C59A, bits ID_{0-2} contain the slave address on the cascade bus. Each slave device in the system *must* be initialized with a unique address. Remaining bits are not used.

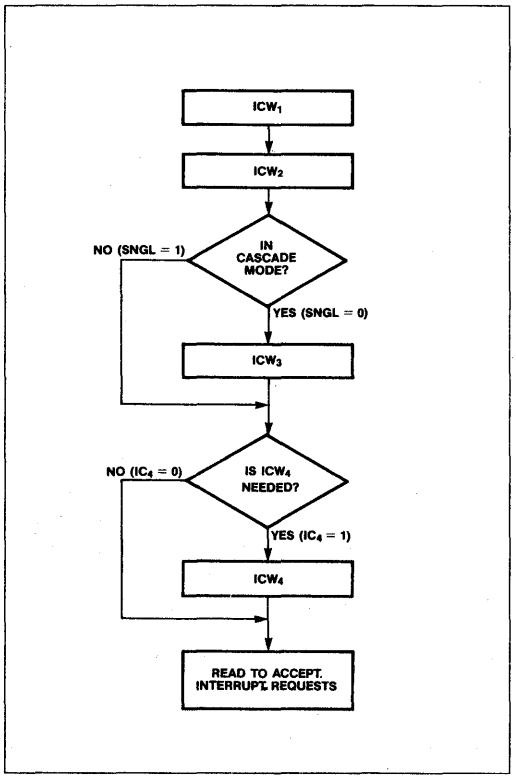
  In operation, the slave compares the cascade input to its 3-bit address and if they match, outputs byte 2 and 3 (Call Mode), or byte 2 only (Vector Mode) to the bus.

Bit Definitions (ICW_4)

This word is used only when bit IC_4 in ICW_1 is set. Note that only five bits are used.

- μPM Microprocessor System Mode: μPM = 0 for Call Mode, μPM = 1 for Vector Mode.
- AEOI This bit is set if the *Automatic End of Interrupt Mode* is to be programmed.
- M/S When the Buffered Mode is selected, the M/$\overline{S}$ bit is used to determine the master/slave programming. That is: M/$\overline{S}$ = 1 indicates the device is a master, while M/$\overline{S}$ = 0 indicates a slave. If the BUF bit is not set, M/$\overline{S}$ is not used.
- BUF The Buffered Mode is programmed by setting BUF = 1. In buffered mode, the output pin $\overline{SP}/\overline{EN}$ becomes an enable output, and the M/S bit determines whether the device is a master or a slave.
- SFNM Special Fully Nested Mode is programmed by setting SFNM = 1.

Figure 10: Initialization Flow Chart



OPERATIONAL COMMANDS

Once the KS82C59A has been initialized, it can accept and process interrupt requests received on its IR input lines. Interrupts are processed according to the modes programmed during the initialization process. A number of commands, sent to the KS82C59A from the CPU, allow the programmed modes or the interrupt request priorities to be changed *on the fly* during operation. These commands are described below (and Figure 12):

Bit Definitions (OCW_1)

OCW_1 is used to set and clear mask bits in the IMR, thus enabling or disabling specific IR inputs. In the *Special Mask Mode*, the ISR is also masked.

- M_{0-7} Bits M_{0-7} correspond to the 8 IR inputs. If bit M_n = 1, the IR_n input is disabled. If M_n = 0, the IR_n input is enabled.

Bit Definitions (OCW_2)

OCW_2 is used to program the different End of Interrupt (EOI) Modes, and alter the interrupt request priorities.

- L_{0-2} These bits determine the interrupt level to be acted upon when bit SL = 1 (active).
- EOI The End of Interrupt command is issued by the CPU, rather than by the KS82C59A (in automatic EOI mode). Note that this bit is used in conjunction with bits R and SL to control the interrupt priority assignments and rotations.
- SL Set Interrupt Level bit. This lowest priority interrupt is assigned to the IR input corresponding to the octal value of L_{0-2}.
- R This bit determines if interrupt priority rotation is in effect. R = 1 indicates priorities will be rotated, perhaps combined with other modes.

Bit Definitions (OCW_3)

OCW_3 is used to program the Special Mask Mode, the Polling Mode, and select internal registers to be read by the CPU.

- RIS If RIS = 1, select ISR. IF RIS = 0, select IRR.
- RR Read Register bit. If RR = 1, output the contents of the register selected by bit RIS onto the bus. The register selection is retained, so OCW_3 does not have to be reissued in order to read the same register again.

- P — If P = 1, the Polling Mode is selected for this KS82C59A. In this mode the CPU will poll for new interrupt requests, rather than having the KS82C59A actively set the CPU *INT* input.
- SMM — If *Special Mask Mode* is enabled (ESMM = 1), then SMM = 1 programs the special mask mode, and SMM = 0 clears the special mask mode.
- ESMM — If ESMM = 1, then the special mask mode is enabled, and can be set or reset by the SMM bit. If ESMM = 0, the special mask mode is disabled and SMM is ignored.

OPERATIONAL MODES

The KS82C59A can be programmed to operate in a number of different modes which are summarized and described below. Depending on the mode, some are set during initialization, and some during operation.

Mode	Location Set	
Buffer Mode	BUF, M/S	(ICW_4)
Cascaded Mode	SNGL	(ICW_1)
• Master Mode	S_{0-7}	(ICW_3)
• Slave Mode	ID_{0-2}	(ICW_3)
End of Interrupt (EOI) Modes	EOI	(OCW_2)
• Automatic EOI Mode	AEOI	(ICW_4)
• Non-specific EOI	EOI, SL, R	(OCW_2)
• Specific EOI	EOI, SL, R	(OCW_2)
Nested Modes		
• Fully Nested Mode	default mode	
• Special Fully Nested Mode	SFNM	(ICW_4)
	AEOI	(ICW_4)
Polling Mode	P	(OCW_3)
Rotation Modes		
• Automatic Rotation Mode	R, SL, EOI	(OCW_2)
• Specific Rotation Mode	R, SL, L_{0-2}	(OCW_2)
Special Mask Mode	ESMM, SMM	(OCW_3)
System Modes		
• CALL Mode	μPM	(ICW_4)
• VECTOR Mode	μPM	(ICW_4)
	IC_4	(ICW_1)
Trigger Modes		
• Edge Triggered Mode	LTIM	(ICW_1)
• Level Triggered Mode	LTIM	(ICW_1)

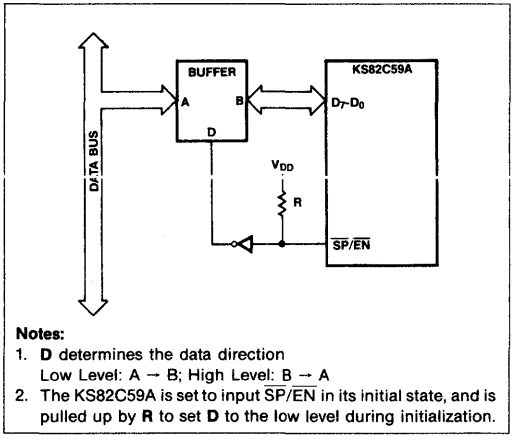
Buffer Mode

In larger systems the KS82C59A may be required to drive the data bus through a buffer. To handle this situation, the *Buffer Mode* is programmed during initialization (using the BUF and M/S bits in ICW_4).

When in buffer mode, $\overline{SP}/\overline{EN}$ is used to enable the data bus buffers, and determine the direction of data flow through the buffer (Figure 13). This signal is active when the output ports of the KS82C59A are activated.

Note that when *cascaded* KS82C59As are required to be used in the buffer mode, the master/slave selection is done using the M/S bit of ICW_4, (and SNGL bit of ICW_1 is set to 1). M/S is set to 1 for the master mode and 0 for the slave mode.

Figure 13: Buffer Mode



Notes:
1. **D** determines the data direction
   Low Level: A → B; High Level: B → A
2. The KS82C59A is set to input $\overline{SP}/\overline{EN}$ in its initial state, and is pulled up by **R** to set **D** to the low level during initialization.

Cascaded Mode

In systems that contain more than 8 priority interrupt levels, several KS82C59A devices can be easily cascaded together to handle a maximum of 64 interrupt levels. In a cascaded configuration, one KS82C59A serves as a *master*, controlling up to 8 *slaves* (able to handle 8 interrupts each). The master selects the slaves via the cascade local bus (CAS_{0-2}), enabling the corresponding slave to output the interrupt service routine address (or vector) following each of the second and third $\overline{INTA}$ signals (second $\overline{INTA}$ signal only in Vector mode). At the end of the interrupt cycle, the EOI command must be issued *twice*, one for the master, and one for the appropriate slave.

Figure 11. Initialization Command Word Format

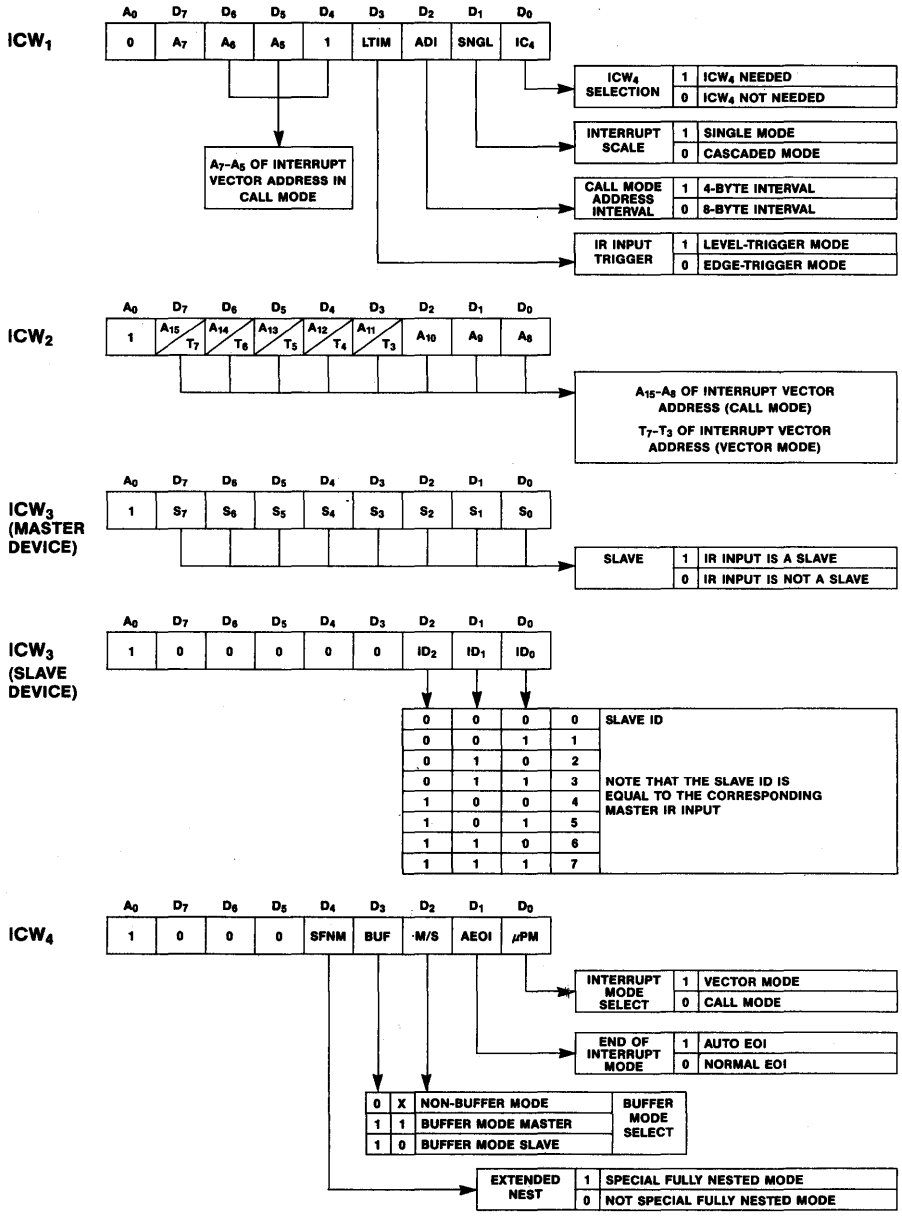
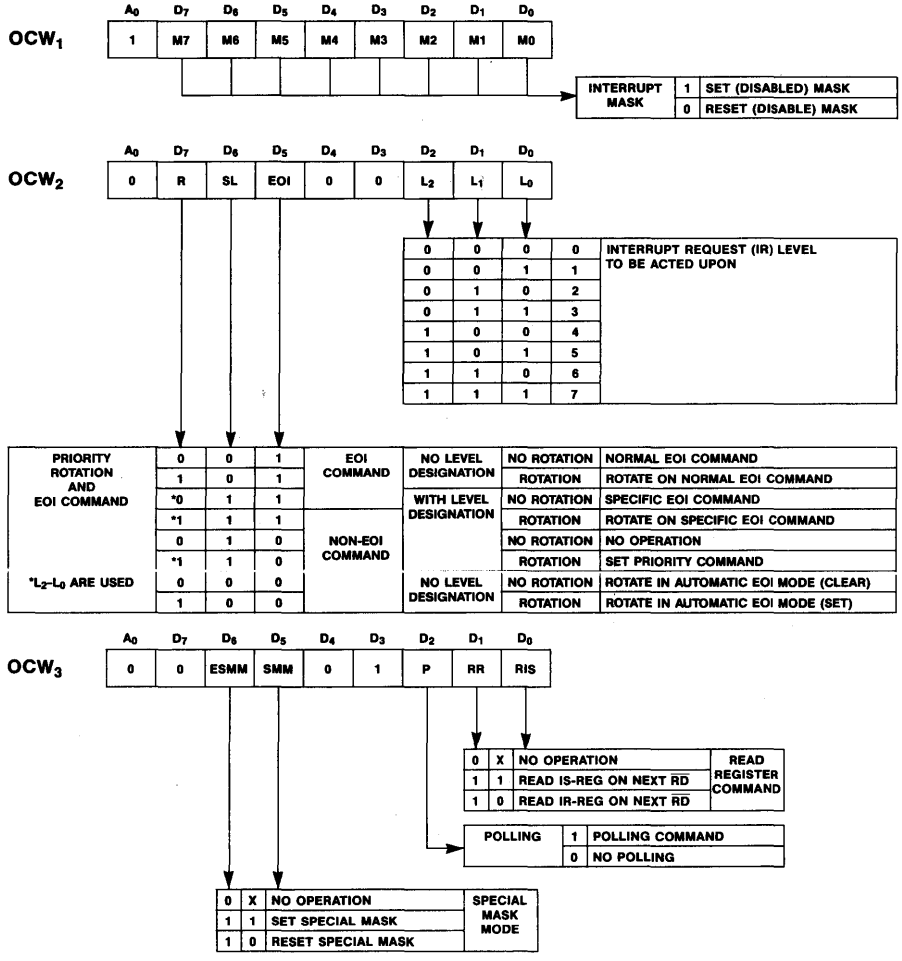


Figure 12. Operation Command Word Format



The CAS_{0-2} bus lines are normally held in a LOW state, and activated only for slave inputs (non-slave inputs to the master do not affect the cascade bus). The slave address will be held on the cascade bus from the trailing edge of the first $\overline{INTA}$ signal to the trailing edge of the last $\overline{INTA}$ signal (either second or third depending on the system mode).

Within the system, each slave can be programmed to operate in a different mode (except AEOI), independently of other slave devices. The interrupt output (INT) of each slave is tied to one of the interrupt request lines (IR_{0-7}) of the master device. Unused IR pins on the master device can be connected to other peripheral devices (as in the single standalone mode of operation), or left unconnected.

Note that an address decoder is required to activate the chip select ($\overline{CS}$) input of each KS82C59A in the system.

Master Mode

A KS82C59A operating in the *Master Mode* can be controlling both peripheral interrupts as well as other KS82C59A slave devices. Since both types of interrupts are connected to the IR_{0-7} pins, it is necessary to differentiate between the two. This is accomplished in the initialization control word (ICW_3) sent out to the master. ICW_3 sets the S_n bits corresponding to IR_n pins connected to slaves equal to one (1), while S_m bits corresponding to IR_m pins connected to peripheral inputs are reset to zero (0).

Peripheral interrupt requests to IR_m pins (S_m = 0) are handled by the master as if it were operating singly. That is, the CAS line remain LOW, and the master provides the interrupt or vector as required.

Slave interrupt requests to IR_n pins (S_n = 1) are handled as follows: the master sends an interrupt to the CPU if the slave requesting the interrupt has priority. If so, the master outputs the slave address *n* to the CAS bus on the first $\overline{INTA}$ signal, then lets the slave complete the remainder of the interrupt cycle. Note that two EOI commands are required to terminate the sequence, one each for the master and slave.

Slave Mode

When a slave KS82C59A receives a peripheral interrupt request, and it has no higher interrupt requests pending, the slave sends an interrupt request to the master via its INT output. This interrupt request is passed by the master to the CPU, which then initiates the interrupt cycle, in turn causing the master to output the slave's address on the CAS bus. Each slave in the system continuously monitors the CAS bus, comparing the addresses thereon until a match is found with its own address. When the slave initiating the interrupt request finds an address match, it completes the interrupt sequence as though it were a single KS82C59A.

Note: Since the master holds the CAS bus LOW (corresponding to CAS address 0) when processing peripheral interrupt requests, address 0 should not be used as a slave address unless the system contains the full complement of 8 slaves.

End of Interrupt (EOI) Modes

The *EOI Modes* are used to terminate teh *request* for *interrupt service* sequence, update the ISR register and alter the interrupt priorities. The EOI mode selected depends on the *nesting mode* currently programmed. The options are discussed below:

Automatic EOI (AEOI) Mode

In *AEOI Mode*, the ISR bit corresponding to the interrupt is set and reset automatically during the final $\overline{INTA}$ signal. This means that the CPU does not have to issue an EOI command at the end of the interrupt routine.

Caution is urged in using AEOI however, as the ISR does not save the *routine currently in service* in this mode. Thus, unless the interrupts are disabled by the interrupt service routine, a stack overflow situation can result from newly generated interrupts (which bypass the priority structure), or from level triggered interrupts.

The Automatic EOI mode is programmed by setting the AEOI bit in ICW_4.

Non-specific (Normal) EOI Mode

When the KS82C59A is operated in the *Fully Nested Mode*, it can easily determine which ISR bit is to be reset at the conclusion of an interrupt sequence. In this case, the non-specific EOI command is used to reset the highest priority level selected from the interrupts in service, (the valid assumption is made that the last interrupt level acknowledged and serviced necessarily corresponds to the highest priority ISR bit set).

A *Non-specific EOI Mode* is selected via OCW_2, where EOI = 1, SL = 0 and R = 0. Refer to Figure 14a, c.

Specific EOI Mode

The *Specific EOI Mode* is required when the fully nested (normal) mode is not used, and the KS82C59A is unable to determine the last interrupt level acknowledged (such as might be encountered if the *Special Mask Mode* is programmed). The Specific EOI command identifies the ISR bit (interrupt level) to be reset using bits L_{0-2} of OCW_2, which also has the following bit settings: EOI = 1, SL = 1 and R = 0. Refer to Figure 14b, d.

Figure 14: EOI Commands

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
OCW_2	0	0	1	0	0	X	X	X

a) Non-specific EOI Command

OCW_2	0	1	1	0	0	L_2	L_1	L_0

b) Specific EOI Command

OCW_2	1	0	1	0	0	X	X	X

c) Rotate on Non-specific EOI Command

OCW_2	1	1	1	0	0	L_2	L_1	L_0

d) Rotate on Specific Command

Mask Modes

The *Mask Modes* are used to selectively enable or disable interrupt requests. This is distinct from the automatic disabling of an interrupt which is in effect while a request from the same interrupt is being serviced.

Normal Mask Mode

Interrupt request lines IR_{0-7} can be individually masked in the Interrupt Mask Register (IMR), using OCW_1. Each bit in IMR masks one interrupt request line if it is set, with no effect on the other interrupt request lines. Bit 0 masks IR_0, bit 1 masks IR_1 etc.

Special Mask Mode

The *Special Mask Mode* is used to dynamically alter the interrupt priority structure under software control during program execution. In this mode, when a mask bit is set in OCW_1, it disables further interrupts at that level, and enables interrupts from all other levels that are not masked. This includes those interrupts which are lower (as well as higher) in priority.

The *Special Mask Mode* is set by ESMM = 1 and SMM = 1 in OCW_3. To clear this mode, the CPU must issue another OCW_3 with ESMM = 1 and SMM = 0. Setting ESMM = 0 alone has no effect. To correctly enter the *Special Mask Mode*, use the following procedure:

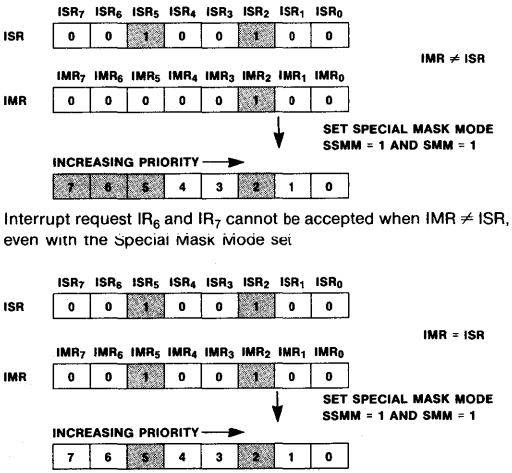
1. CPU reads the ISR
2. CPU writes the ISR data from (1) to the IMR (OCW_1)
3. CPU selects *Special Mask Mode* by issuing OCW_3 with ESMM = 1 and SMM = 1.

This procedure ensures that all interrupt requests not currently in service will be enabled.

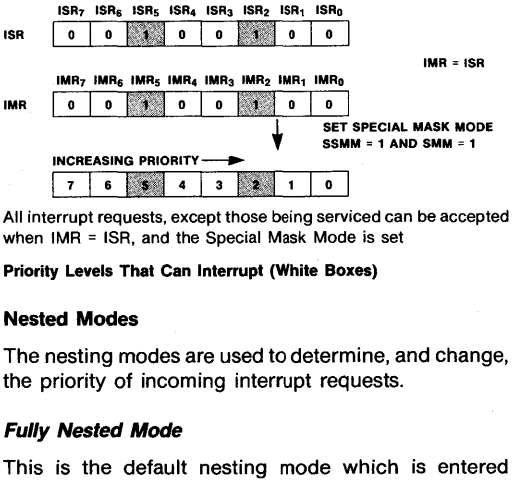
Note that if IMR is not set equal to ISR when *Special Mask Mode* is selected, bits which may be set in the ISR will be ignored. If a corresponding bit is not set in IMR, that interrupt request may be serviced, causing all interrupts of lower priority to be effectively disabled. This is illustrated in Figure 15.

When the *Special Mask Mode* is selected, the *Specific EOI Mode* must be used to terminate the interrupt sequence, so the CPU can explicitly specify which ISR bit is to be reset.

Figure 15: Special Mask Mode



Interrupt request IR_6 and IR_7 cannot be accepted when IMR ≠ ISR, even with the Special Mask Mode set



All interrupt requests, except those being serviced can be accepted when IMR = ISR, and the Special Mask Mode is set

Priority Levels That Can Interrupt (White Boxes)

Nested Modes

The nesting modes are used to determine, and change, the priority of incoming interrupt requests.

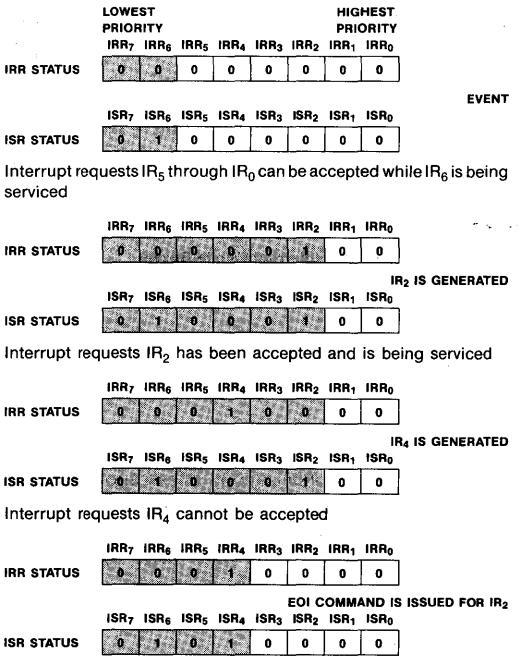
Fully Nested Mode

This is the default nesting mode which is entered automatically after initialization, unless another mode has been programmed. In the *Fully Nested Mode*, the interrupt request priorities are set in descending order from 0 to 7. That is; IR_0 is the highest priority interrupt, IR_7 the lowest.

When an interrupt is acknowledged, the highest priority request is selected, the corresponding ISR bit is set, and the service routine address information is output to the data bus. The ISR bit is reset by the EOI command from the CPU, or automatically if *AEOI Mode* is programmed, at the completion of the interrupt sequence. While the ISR bit is set, all interrupt requests of equal or lower priority are inhibited. Interrupt requests of higher priority will generate an interrupt to the CPU, but whether or not these will be acknowledged depends on the system software. Interrupt priorities can be altered in this mode using one of the *Rotation Modes*.

Note that fully nested interrupt priorities are not necessarily preserved in those systems containing cascaded KS82C59As, as it is possible for interrupts of higher priority than the one being serviced to be ignored. This situation occurs when a slave accepts a peripheral interrupt request (and passes the request to the master). When the master accepts the request, it locks out further interrupts from that slave. Should an interrupt of higher priority come in to the same slave, it will not be recognized until the interrupt being serviced has completed processing. To preserve interrupt priorities in this situation, use the *Special Fully Nested Mode*.

Figure 16: Fully Nested Mode



Special Fully Nested Mode

This mode is very similar to the *Fully Nested Mode*, but is used in systems with cascaded KS82C59's, so as to preserve the interrupt priorities within each slave, as well as within the master. The *Special Fully Nested Mode* is programmed by setting the SFNM bit in the ICW_4 word in both the master and the slave during initialization. This allows interrupt requests of a higher level than the one being serviced to be accepted by the master from the same slave. That is, the slave is not locked out from the priority logic in the master, and higher priority interrupts within the slave will be recognized by the master, which will generate an interrupt to the CPU.

Caution should be exercised in this mode during the End Of Interrupt processing. It is essential that the system software check whether or not the interrupt just serviced was the *only* one from that slave. After the first non-specific EOI has been issued to the slave, the CPU should read the slave's ISR and check that no other bits are set (ISR = 0). Only if the slave ISR is zero, *can a non-specific EOI be sent to the master to complete the interrupt sequence*. If bits are set in the slave ISR, no EOI should be sent to the master.

Polling Mode

The *Polling Mode* is used to bypass the KS82C59A Interrupt control logic in favour of PCU software control over interrupt request processing. This allows systems to be built up with more than one master KS82C59A, and consequently, the sytem can contain more than 64 interrupt priority levels (since each master can handle 64 levels individually). In this case, the CPU polls each master looking for the highest priority interrupt request within the realm of each master.

In the *Polling Mode*, the INT outputs of the KS82C59A masters, and the INT input of the CPU are disabled. Interrupt service to individual peripheral devices is accomplished by system software using the *Poll Command* (Bit 'P' = 1 in OCW_3). When a poll command has been issued, the KS82C59A waits for the CPU to perform a register read. This read is treated by the KS82C59A as an interrupt acknowledge, and it sets the appropriate ISR bit and determines the priority level if there is an interrupt request pending. It then outputs the polling data byte onto the data bus (see Figure 17), including the binary code of the highest priority level requesting service. The CPU then processes the interrupt according to the polling data read, terminating the interrupt sequence with an EOI. Interrupt is frozen from WR to RD.

Figure 17: Poll Command

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
OCW_3	INT	0	0	0	0	W_2	W_1	W_0

Notes:
1. W_0-W_2 is binary code of highest priority level requesting service.
2. **INT** is equal to one (1) if there is an interrupt.

Rotation Modes

The different *Rotation Modes* allow the interrupt request priorities to be changed either automatically, or under software control. This is particularly useful for situations where there are a number of equal priority devices, or where a particular application may call for a specific priority change.

Automatic Rotation Mode

The *Automatic Rotation Mode* is recommended where there are a number of equal priority devices. In this mode the device is assigned the lowest priority immediately after it has had an interrupt request serviced. Its priority is subsequently increased as other devices have their interrupt requests serviced, and are then rotated to the bottom of the priority list. In the worst case, a device would have to wait for a maximum of seven other device interrupts of equal priority to be serviced *once*, before it was serviced. The effect of rotation on interrupt priority is illustrated in Figure 18.

Automatic Rotation can be activated in one of two ways, both using the command word OCW_2, and both combined with EOI modes:

- Rotation in Non-specific EOI Mode (R = 1, SL = 0 and EOI = 1)
- Rotation in Automatic EOI Mode (R = 1, SL = 0 and EOI = 0). This mode must be cleared by the CPU (accomplished by sending OCW_2 with: R = 0, SL = 0 and EOI = 1.

Specific Rotation Mode

The Specific Rotation Mode provides a mechanism to arbitrarily change interrupt priority assignments. This is accomplished by programming the lowest priority interrupt request line (specified by bits L_{0-2} in OCW_2), thereby fixing the other priorities. That is, if IR_4 is programmed as the lowest priority device, then IR_5 will have the highest priority.

Caution: because this change in priority levels is different from the normal *Fully Nested Mode*, it is *essential* that the user manage the interrupt nesting via the system software.

Specific rotation can be activated in one of two ways, both using the command word OCW_2:

- The *Set Priority* command is issued in OCW_2 with: R = 1, SL = 1 and L_{0-2} equal to the binary code of the lowest priority device.
- As part of the *Specific EOI Mode*, with OCW_2, (Rotate on Specific EOI command) values: R = 1, SL = 1, EOI = 1 and L_{0-2} equal to the binary priority level code of the lowest priority device. When the specific EOI is issued by the CPU, the KS82C59A resets the ISR bit designated by bits L_{0-2} in OCW_2, then rotates the priorities so that the interrupt just reset becomes the lowest priority.

Figure 18: Effect of Rotation

	ISR_7	ISR_6	ISR_5	ISR_4	ISR_3	ISR_2	ISR_1	ISR_0
ISR STATUS	0	1	0	1	0	0	0	0
	LOWEST PRIORITY							HIGHEST PRIORITY
PRIORITY STATUS	7	6	5	4	3	2	1	0

BEFORE ROTATE: IR_4 is the highest priority requiring service

AFTER ROTATE: IR_4 was serviced, all other priorities have been rotated correspondingly

	ISR_7	ISR_6	ISR_5	ISR_4	ISR_3	ISR_2	ISR_1	ISR_0
ISR STATUS	0	1	0	0	0	0	0	0
	HIGHEST PRIORITY							LOWEST PRIORITY
PRIORITY STATUS	2	1	0	7	6	5	4	3

Figure 18: Rotation Commands

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
OCW_2	1	0	0	0	0	X	X	X

a) Rotate in Automatic EOI Mode (Set)

OCW_2	0	0	0	0	0	X	X	X

b) Rotate in Automatic EOI Mode (Reset)

OCW_2	1	0	1	0	0	X	X	X

c) Rotate on Non-specific EOI Command

OCW_2	1	1	1	0	0	L_2	L_1	L_0

d) Rotate on Specific Command

OCW_2	1	1	0	0	0	L_2	L_1	L_0

e) Set Priority Command (Specific Rotation)

System Modes

The KS82C59A *must* operate in the system mode that corresponds to the processor type used in the system. *Call Mode* is used for 8085 type systems (and features an interrupt cycle controlled by three $\overline{INTA}$ signals), while *Vector Mode* is used for more sophisticated 8088/86 and 80286/386 type systems (and features an interrupt cycle controlled by only two $\overline{INTA}$ signals). These modes are described in more detail back in the Operational Description section.

Trigger Modes

In the KS82C59A, the interrupt request lines (IR_{0-7}) can be programmed for either edge or level triggering sensitivity, with the requirement that all IR lines must be in the same mode. That is, all edge triggered, or all level triggered. Figure 21 illustrates the priority cell diagram which shows a conceptual circuit of the level sensitive and edge sensitive input circuitry of the IR lines.

Note that to ensure a valid interrupt request is registered by the KS82C59A, it is essential that the IR input remain HIGH until after the first $\overline{INTA}$ has been received. In both modes, if the IR input goes LOW before this time, the interrupt will be registered as a *default* IR_7 regardless of which IR input initiated the interrupt request. This *default* IR_7 can be used to detect (and subsequently ignore) spurious interrupt signals such as those caused by glitches or noise on the IR input lines. The technique is described below:

- If the IR_7 input is not used, it can be assigned solely to intercepting spurious interrupt requests, invoking a simple service routine that contains a return only, thus effectively ignoring the interrupt.
- If IR_7 is used for a peripheral interrupt, a default IR_7 is detected with the extra step of reading the ISR. A normal IR_7 interrupt causes the corresponding bit to be set in the ISR, while a default IR_7 interrupt does not. It is necessary that the system software keep track of whether or not the IR_7 service routine has been entered. In the event that another IR_7 interrupt occurs before servicing is complete, it will be a default IR_7 interrupt (and should be ignored).

Edge Triggered Mode

Programmed by setting the LTIM bit in ICW_1: LTIM = 0 for *low-to-high-transition* edge triggering. An interrupt request is detected by a rising edge on an IR line. The IR line must remain HIGH until after the falling edge of the first $\overline{INTA}$ signal has been received from the CPU. This is required to latch the corresponding IRR bit. It is recommended that the IR line be kept HIGH to help filter out noise spikes that might cause spurious interrupts. To send the next interrupt request, temporarily lower the IR line, then raise it.

Level Triggered Mode

Programmed by setting the LTIM bit in ICW_1: LTIM = 1 for level triggering. An interrupt request is detected by a HIGH level on an IR line. This HIGH level must be maintained until the falling edge of the first $\overline{INTA}$ signal (as in the edge-triggered mode), to ensure the appropriate IRR bit is set. However, in the level triggered mode, interrupts are requested *as long as* the IR line remains HIGH. Thus, care should be exercised so as to prevent a stack overflow condition in the CPU.

Figure 20: Trigger Mode Timing

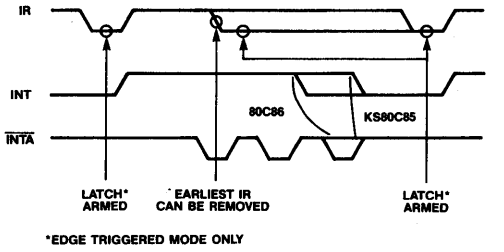
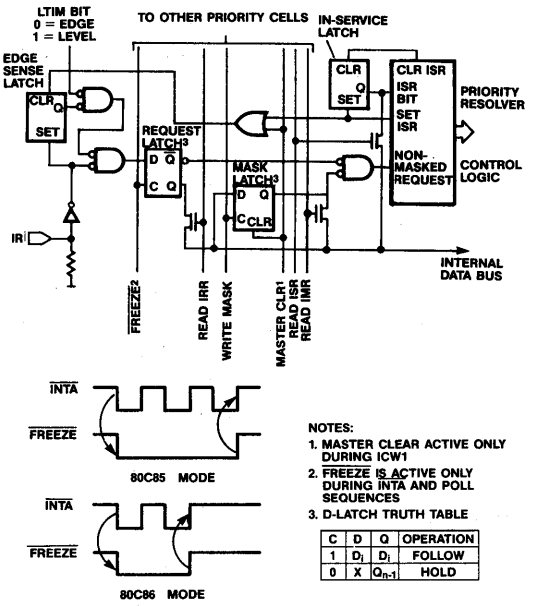


Figure 21: Priority Cell Structure



NOTES:
1. MASTER CLEAR ACTIVE ONLY DURING ICW1
2. FREEZE IS ACTIVE ONLY DURING INTA AND POLL SEQUENCES
3. D-LATCH TRUTH TABLE

C	D	Q	OPERATION
1	D_i	D_i	FOLLOW
0	X	Q_{n-1}	HOLD

APPLICATION DIAGRAMS

Figure 22: KS82C59A in Standard System Configuration

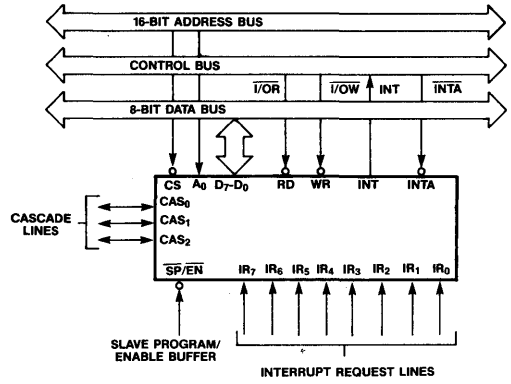
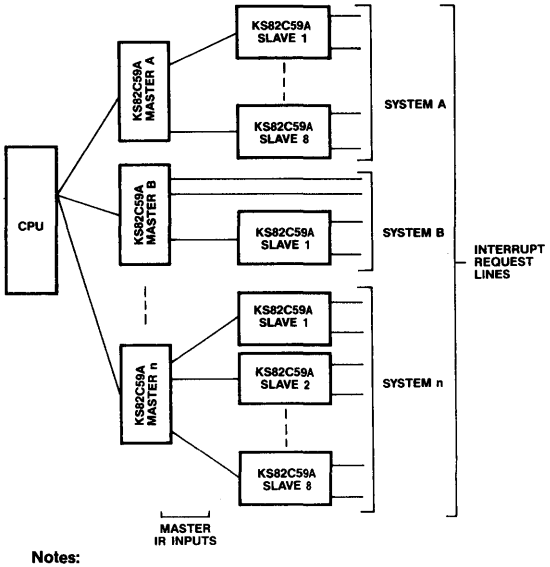


Figure 24: Multiple KS82C59A Masters in a Polled System



Notes:
1. Master KS82C59As in Poll Mode
2. Maximum of 64 Inputs per System
3. Total Capacity Limited by CPU

Figure 23: Multiple KS82C59As in a Cascaded System

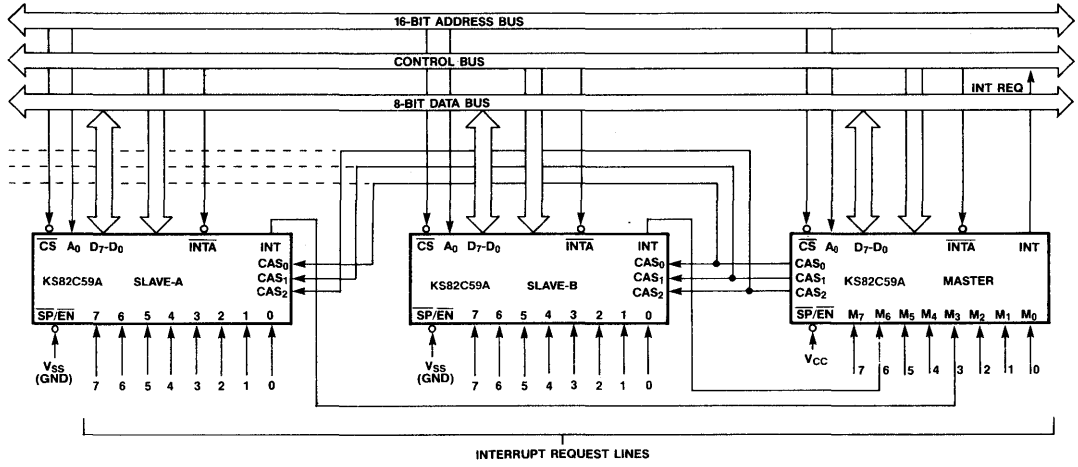


Table 5: Recommended Operating Conditions

DC Supply Voltage		+4.0V to +6.0V
Operating Temperature Ranges	Commercial	0°C to 70°C
	Industrial	-40°C to +85°C

Table 6: Absolute Maximum Ratings

DC Supply Voltage	-0.5 to +7.0V
Input, Output or I/O Voltage Applied	V_{SS} - 0.5V to V_{CC} + 0.5V
Storage Temperature Range	-65°C to +150°C
Maximum Package Power Dissipation	1W

Note: Stresses beyond those listed above may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 7: Capacitance (T_A = 25°C, V_{CC} = 0V, V_{IN} = +5V or V_{SS})

Symbol	Parameter	Test Conditions	Typ	Units
$C_{I/O}$	I/O Capacitance	FREQ = 1MHz Unmeasured Pins Returned to V_{SS}	20	pF
C_{IN}	Input Capacitance		7	pF
C_{OUT}	Output Capacitance		15	pF

Table 8: DC Characteristics (T_A = 0°C to 70°C, V_{CC} = 5V ± 10%)

Symbol	Parameter	Test Conditions	Limits		Unit
			Min	Max	
I_{CC}	V_{CC} Supply Current	V_{IN} = 0V/V_{CC}, C_L = 0pF	—	1	mA/MHz
I_{CCSB}	Standby Power Supply Current	CS = V_{CC}, IR = V_{CC} V_{IL} = 0V, V_{IH} - V_{CC}	—	10	μA
I_{LI}	Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}	-1.0	+1.0	μA
I_{LIR}	IR Input Load Current	V_{IN} = 0V V_{IN} = V_{CC}, All temp ranges	— —	-300 10	μA μA
I_{LOL}	Output Leakage Current	0V ≤ V_{OUT} ≤ V_{CC}	-10.0	+10.0	μA
V_{IH}	Input HIGH Voltage		2.2	V_{CC} + 0.5	V
V_{IL}	Input LOW Voltage		-0.5	0.8	V
V_{OH}	Output HIGH Voltage	I_{OH} = -2.5mA I_{OH} = -100μA	3.0 V_{CC} - 0.4	— —	V V
V_{OL}	Output LOW Voltage	I_{OL} = +2.5mA	—	0.4	V

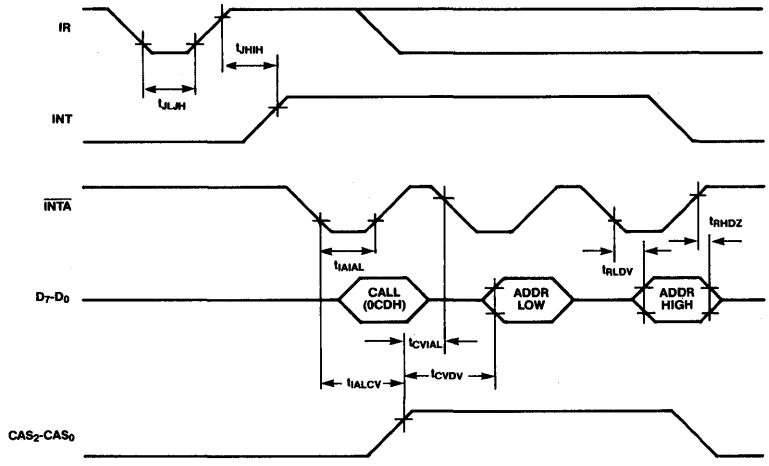
Table 9: AC Characteristics (T_A = 0°C to 70°C, V_{CC} = 5V ± 10%)

Symbol	Parameter	Test Conditions	Limits (8MHz)		Limits (10MHz)		Units
			Min	Max	Min	Max	
t_{AHDV}	Data Valid from Stable Address		—	200	—	160	ns
t_{AHRL}	A_0/$\overline{CS}$ Setup to $\overline{RD}$/$\overline{INTA}$↓		10	—	10	—	ns
t_{AHWL}	A_0/$\overline{CS}$ Setup to $\overline{WR}$↓		0	—	0	—	ns
t_{CHCL}	End of Command to next Command (Not same command type) End of $\overline{INTA}$ Sequence to Next $\overline{INTA}$ sequence (same as T_{RV2})	Note 1	200	—	160	—	ns
t_{CVDV}	Cascade Valid to Valid Data	Slave, C_L = 100pF	—	200	—	130	ns
t_{CVIAL}	Cascade Setup to Second or Third $\overline{INTA}$↓ (Slave only)	Slave	40	—	30	—	ns
t_{DVWH}	Data Setup to $\overline{WR}$↑		160	—	100	—	ns
t_{IAIAH}	$\overline{INTA}$ Pulse Width HIGH	$\overline{INTA}$ Sequence	160	—	100	—	ns
t_{IAIAL}	$\overline{INTA}$ Pulse Width LOW		160	—	100	—	ns
t_{IALCV}	Cascade Valid from First $\overline{INTA}$↓ (Master Only)	Master, C_L = 100pF	—	260	—	160	ns
t_{JHIH}	Interrupt Output Delay	C_L = 100pF	—	200	—	120	ns
t_{JLJH}	Interrupt Request Width (LOW)	Note 2	100	—	100	—	ns
t_{RHAX}	A_0/$\overline{CS}$ Hold After $\overline{RD}$/$\overline{INTA}$↑		0	—	0	—	ns
t_{RHDZ}	Data Float After $\overline{RD}$/$\overline{INTA}$↑	C_L = 100pF	10	85	10	65	ns
t_{RHEH}	Enable Inactive from $\overline{RD}$↑ or $\overline{INTA}$↑		—	50	—	50	ns
t_{RHRL}	End of $\overline{RD}$ to next $\overline{RD}$ End of $\overline{INTA}$ to next $\overline{INTA}$ within $\overline{INTA}$ sequence only		160	—	100	—	ns
t_{RLDV}	Data Valid from $\overline{RD}$/$\overline{INTA}$↓	C_L = 100pF	—	120	—	95	ns
t_{RLEL}	Enable Active from $\overline{RD}$↓ or $\overline{INTA}$↓		—	100	—	70	ns
t_{RLRH}	$\overline{RD}$ Pulse Width		160	—	100	—	ns
t_{RV1}	Command Recovery Time	Note 3	200	—	160	—	ns
t_{RV2}	$\overline{INTA}$ Recovery Time	Note 4	200	—	160	—	ns
t_{WHAX}	A_0/$\overline{CS}$ Hold After $\overline{WR}$↑		0	—	0	—	ns
t_{WHDX}	Data Hold After $\overline{WR}$↑		0	—	0	—	ns
t_{WHWL}	End of $\overline{WR}$ to next $\overline{WR}$		160	—	100	—	ns
t_{WLWH}	$\overline{WR}$ Pulse Width		160	—	100	—	ns

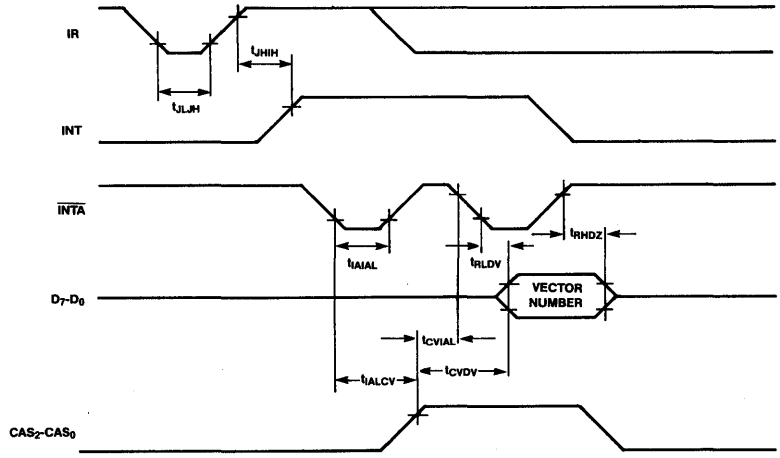
Notes:
1. The time to move $\overline{INTA}$ to/from command (read/write).
2. The time to clear the input latch in edge-triggered mode.
3. The time to move from read to write operation.
4. The time to move to the next $\overline{INTA}$ operation.

Figure 25: Timing Diagrams

a) Interrupt Cycle (CALL Mode)

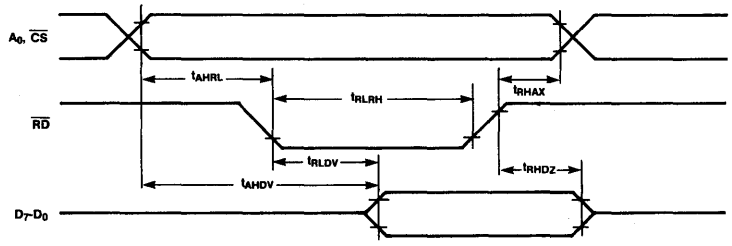


b) Interrupt Cycle (VECTOR Mode)

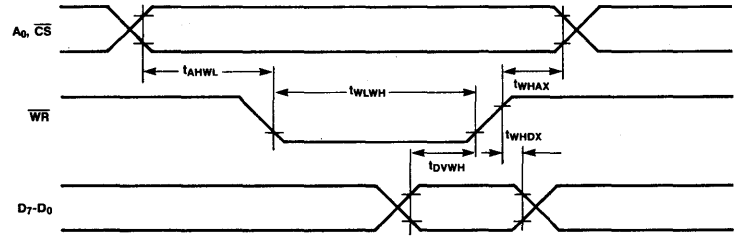


Note that **IR** input should remain at a high level until the leading edge of the first $\overline{INTA}$ pulse.

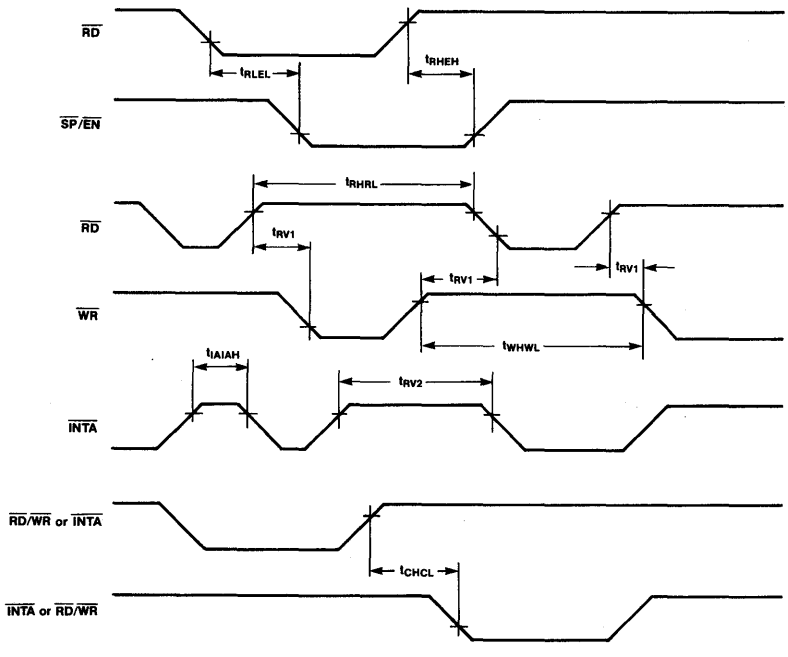
c) Read Cycle



d) Write Cycle



e) Other Timing



PACKAGE DIMENSIONS

Figure 26: Plastic Packaging DIP-28

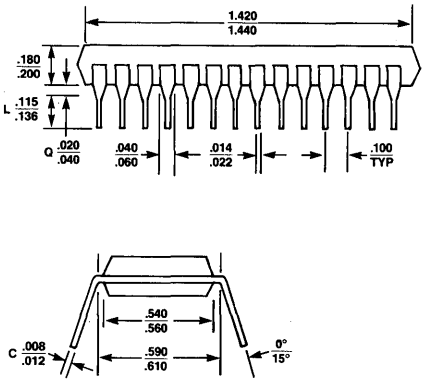
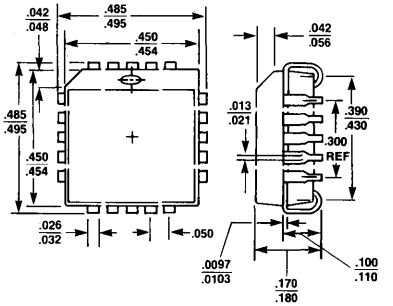
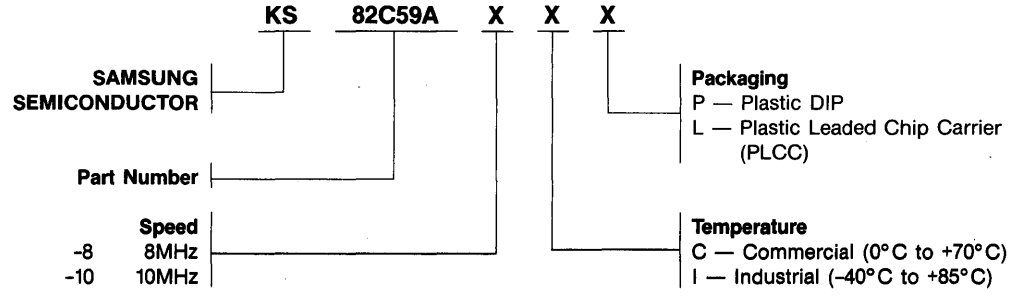


Figure 27: PLCC-28 Package

Units: Inches



ORDERING INFORMATION AND PRODUCT CODE



SAMSUNG products are designated by a Product Code. When ordering, please refer to products by their full code. For unusual, and/or specific packaging or processing requirements not covered by the standard product line, please contact the SAMSUNG MOS Product Group.

KS82C84A

CLOCK GENERATOR AND DRIVER

FEATURES

- **Pin and functional compatibility with the industry standard 82C84/82C84A**
- **Very high speed — 8 and 10MHz**
- **Low power CMOS implementation**
- **TTL input/output compatibility**
- **5V ± 10% power supply**
- **Provides Local READY and Multibus™ READY Synchronization**
- **Generates System Reset Output from Schmitt Trigger Input**
- **Capable of Clock Synchronization with other 8284As**
- **Uses a Crystal or a TTL signal for frequency source**

DESCRIPTION

The KS82C84A is a high performance, single chip clock generator/driver for the 8088/86 type processors, offering pin-for-pin functional compatibility with the industry standard 8284/8284A. It features a crystal-controlled oscillator, a divide-by-three counter, complete Multibus™ Ready synchronization, and reset logic.

The KS82C84A is manufactured using CMOS technology. Its very low power consumption also makes it suitable for portable systems and systems with low power standby modes.

3

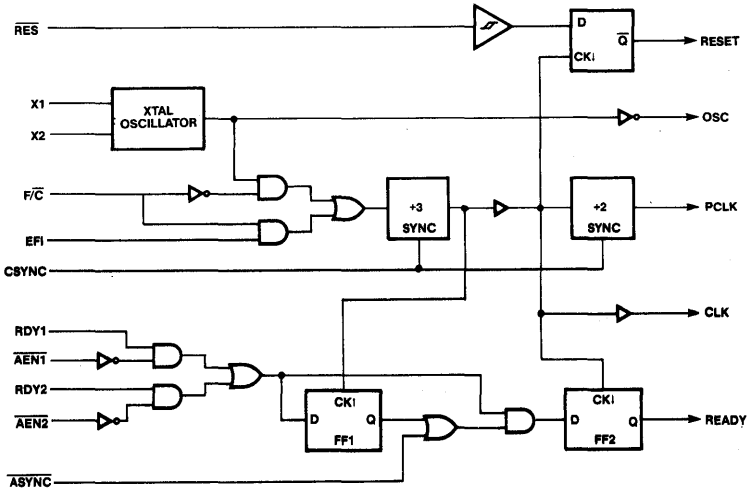


Figure 2: KS82C84A Block Diagram

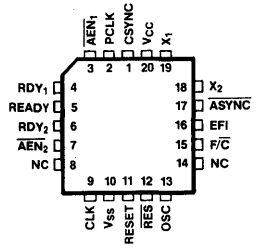


Figure 1a: 20-Pin PLCC Configuration

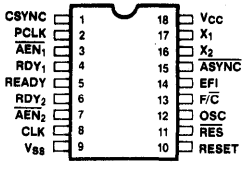


Figure 1b: 18-Pin DIP Configuration

Multibus is a trademark of Intel

Table 1a: 20-Pin PLCC Pin Assignment

Pin #	I/O	Pin Name	Pin #	I/O	Pin Name
1	I	CSYNC	11	O	RESET
2	O	PCLK	12	I	$\overline{RES}$
3	I	$\overline{AEN1}$	13	O	OSC
4	I	RDY1	14	—	NC
5	O	READY	15	I	F/$\overline{C}$
6	I	RDY2	16	I	EFI
7	I	$\overline{AEN2}$	17	I	$\overline{ASYNC}$
8	—	NC	18	I	X2
9	O	CLK	19	I	X1
10	—	V_{SS}	20	—	V_{CC}

Table 1b: 18-Pin DIP Pin Assignment

Pin #	I/O	Pin Name	Pin #	I/O	Pin Name
1	I	CSYNC	10	O	RESET
2	I	PCLK	11	O	$\overline{RES}$
3	I	$\overline{AEN1}$	12	O	OSC
4	O	RDY1	13	O	F/$\overline{C}$
5	O	READY	14	I	EFI
6	I	RDY2	15	O	$\overline{ASYNC}$
7	O	$\overline{AEN2}$	16	O	X2
8	O	CLK	17	I	X1
9	—	V_{SS}	18	—	V_{CC}

Table 2: Pin Descriptions

Symbol	Type	Name and Function
$\overline{AEN1}$, $\overline{AEN2}$	I	**Address Enable:** $\overline{AEN}$ is an active LOW signal which qualifies its respective Bus Ready Signal. $\overline{AEN1}$ validates RDY1 while $\overline{AEN2}$ validates RDY2. Two $\overline{AEN}$ signal inputs are useful in system configurations with two multi-master System Buses. In non-multi-master configurations the $\overline{AEN}$ signal inputs are tied true (LOW).
$\overline{ASYNC}$	I	**Ready Synchronization Select:** $\overline{ASYNC}$ defines the synchronization mode of the READY logic. When $\overline{ASYNC}$ is LOW, two stages of READY synchronization are provided. When HIGH or open a single stage of READY synchronization is provided.
CLK	O	**Processor Clock:** CLK is used by the processor and all devices which connect directly to the processor's local bus. CLK has an output frequency of 1/3 the crystal or EFI input frequency and a 1/3 duty cycle. An output HIGH of 4.5 volts (V_{CC} = 5V) is provided to drive MOS devices.
CSYNC	I	**Clock Synchronization:** CSYNC is an active HIGH signal which allows multiple 8284As to be synchronized to provide clocks that are in phase. When CSYNC is HIGH the internal counters are reset. When CSYNC goes LOW the internal counters are allowed to resume counting. CSYNC must be externally synchronized to EFI. When using the internal oscillator, CSYNC should be hardwired to ground.
EFI	I	**External Frequency:** When F/$\overline{C}$ is strapped HIGH, CLK is generated from the input frequency appearing on this pin. This input signal is a square wave 3x the frequency of the desired CLK output. EFI should be connected to V_{CC} or V_{SS} if F/$\overline{C}$ is LOW.
F/$\overline{C}$	I	**Frequency/Crystal Select:** F/$\overline{C}$ is a strapping option. When strapped LOW, F/$\overline{C}$ permits the processor clock to be generated by the crystal. When strapped HIGH, CLK is generated form the EFI input.
OSC	O	**Oscillator Output:** OSC is the TTL level output of the internal oscillator circuitry. Its frequency is equal to that of the crystal.
PCLK	O	**Peripheral Clock:** PCLK is a TTL level peripheral clock signal whose output frequency is 1/2 that of CLK and has a 50% duty cycle.

Table 2: Pin Descriptions (Continued)

Symbol	Type	Name and Function
RDY1, RDY2	I	**Bus Ready:** (Transfer Complete) RDY is an active HIGH signal which indicates that data from a device located on the system data bus has been received, or is available. RDY1 is qualified by $\overline{AEN1}$ while RDY2 is qualified by $\overline{AEN2}$.
READY	O	**Ready:** READY is an active HIGH signal which is synchronized to the RDY signal input. READY is cleared after the guaranteed hold time to the processor has been met.
$\overline{RES}$	I	**Reset In:** $\overline{RES}$ is an active LOW signal used to generate RESET. The KS82C84A provides a Schmitt trigger input so that an RC connection can be used to establish the power-up reset of proper duration.
RESET	O	**Reset:** RESET is an active HIGH signal which is used to reset the 8086 family processors. Its timing characteristics are determined by $\overline{RES}$.
X1, X2	I	**Crystal In:** X1 and X2 are the pins to which a crystal is attached. The crystal frequency is 3x the desired processor clock frequency. (If no crystal is attached, then X1 should be tied to V_{CC} or V_{SS} and X2 should be left open.)
V_{CC}	—	**Power:** 5V ± 10% DC Supply.
V_{SS}	—	**Ground:** 0V.

FUNCTIONAL DESCRIPTION

Oscillator

The oscillator of the KS82C84A is designed for use with an external parallel resonant, fundamental mode crystal from which the basic operating frequency is derived.

The crystal frequency should be selected to be 3X the required CPU clock frequency. X1 and X2 are the two crystal inputs. For the most stable operation of OSC, two capacitors (C1 = C2), as shown in the waveform figures, are recommended. The output of the oscillator is buffered and brought out on OSC so that other system timing signals can be derived from this stable, crystal-controlled source.

Capacitors C1, C2 are chosen such that their combined capacitance:

$$CT = \frac{C1 \cdot C2}{C1 + C2} \text{ (Including Stray Capacitance)}$$

matches the load capacitance as specified by the crystal manufacturer. This insures operation within the frequency tolerance specified by the crystal manufacturer.

Clock Generator

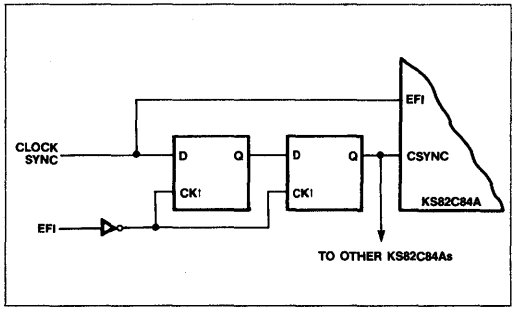
The clock generator consists of a synchronous divide-by-three counter with a special clear input that inhibits the counting. This clear input (CSYNC) allows the output clock to be synchronized with an external event (such as another KS82C84A clock). The ASYNC input to the EFI clock external to the KS82C84A is synchronized using two Schottky flip-flops. The counter output is a 33% duty cycle clock at one-third the input frequency.

The F/$\overline{C}$ input is a strapping pin that selects either the crystal oscillator or the EFI input as the clock for the ÷3 counter. If the EFI input is selected as the clock source, the oscillator section can be used independently for another clock source with output taken from OSC.

Clock Outputs

The CLK output is a 33% duty cycle clock driver designed to drive the 8088/86 processors directly. PCLK is a TTL level peripheral clock signal with a frequency of 1/2 CLK, and a 50% duty cycle.

Figure 3: CSYNC Synchronization



Reset Logic

The reset logic provides a Schmitt trigger input ($\overline{RES}$) and a synchronizing flip-flop to generate the reset timing. The reset signal is synchronized to the falling edge of CLK. Utilizing this function, a simple RC network can be used to provide a power-on reset.

READY Synchronization

Two READY Inputs (RDY1, RDY2) are provided to accommodate two multi-master system buses. Each input has a qualifier ($\overline{AEN1}$ and $\overline{AEN2}$, respectively). The $\overline{AEN}$ signals validate their respective RDY signals. If a multi-master system is not being used, the $\overline{AEN}$ pin should be tied LOW.

Synchronization is required for all asynchronous active-going edges of either RDY input to guarantee that the RDY setup and hold times are met. Inactive-going edges of RDY in normally ready systems do not require synchronization, but must satisfy RDY setup and hold.

The $\overline{ASYNC}$ input defines two modes of READY synchronization operation: When $\overline{ASYNC}$ is LOW, two stages of synchronization are provided for active READY input signals. Positive-going asynchronous READY inputs are first synchronized to flip-flop one at the rising edge of CLK, and then synchronized to flip-flop two at the next falling edge of CLK, after which the READY output goes active (HIGH). Negative-going asynchronous READY inputs are synchronized directly to flip-flop two at the falling edge of CLK, after which the READY output goes inactive. This mode of operation is intended for asynchronous (normally not ready) devices in the system which cannot be guaranteed by design to meet the required RDY setup timing, t_{R1VCL}, on each bus cycle.

When $\overline{ASYNC}$ is HIGH or open, the first READY flip-flop is bypassed in the READY synchronization logic. READY inputs are synchronized by flip-flop two on the falling edge of CLK before they are presented to the processor. This mode is available for synchronous devices that can be guaranteed to meet the required RDY setup time.

$\overline{ASYNC}$ can change at every bus cycle to set the correct synchronization mode for each device in the system.

Table 3: Recommended Operating Conditions

DC Supply Voltage		+4.0V to +6.0V
Operating Temperature Range	Commercial	0°C to 70°C
	Industrial	-40°C to +85°C

Table 4: Absolute Maximum Ratings

DC Supply Voltage	+7.0V
Input, Output or I/O Voltage Applied	V_{SS} - 0.5V to V_{CC} + 0.5V
Storage Temperature Range	-65°C to +150°C
Maximum Package Power Dissipation	1W

Note: Stresses beyond those listed above may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 5: DC Characteristics (T_A = 0°C to 70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V)

Symbol	Parameter		Test Conditions	Limits Min	Limits Max	Unit
C_{IN}	Input Capacitance		freq = 1MHz		7	pF
I_{CC}	Operating Supply Current:	5MHz	15MHz xtal, C_L = 0		10	mA
		10MHz	30MHz xtal, C_L = 0		40	mA
I_{CCS}	Standby Supply Current (Note 1)				100	μA
I_{LI}	Input Leakage Current: (Note 2)	ASYNC Only	ASYNC = V_{CC}		10	μA
			ASYNC = V_{SS}		-130	μA
		All Other Pins	$0V \leq V_{IN} \leq V_{CC}$		±1.0	μA
V_{IH}	Input HIGH Voltage			2.2	V_{CC} + 0.5	V
V_{IHR}	Reset Input HIGH Voltage			$0.6V_{CC}$		V
V_{IHR}-V_{ILR}	RES Input Hysteresis			0.25		V
V_{IL}	Input LOW Voltage				0.8	V
V_{OH}	Output HIGH Voltage		CLK: I_{OH} = -4mA Others: I_{OH} = -2.5mA	V_{CC}-0.4		V
V_{OL}	Output LOW Voltage		CLK: I_{OL} = 4mA Others: I_{OL} = 2.5mA		0.4	V

Notes:
1. V_{IH}, F/$\overline{C}$ X1 ≥ V_{CC} - 0.2V; V_{IL} X2 ≤ 0.2V; $\overline{ASYNC}$ = V_{CC} or $\overline{ASYNC}$ = Open.
2. An internal pull-up resistor is implemented on the $\overline{ASYNC}$ input.

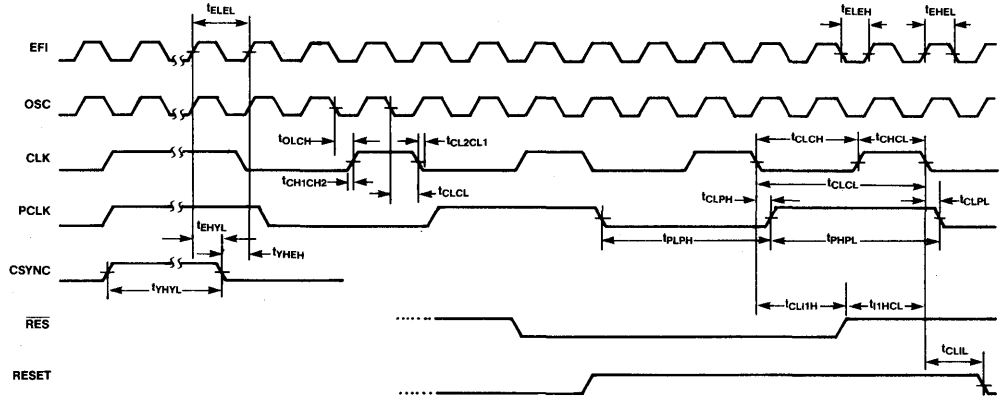
Table 6: AC Characteristics, DMA (Master) Mode (T_A = 0°C to 70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V)

Symbol	Parameter	Test Conditions	Limits (8MHz)		Limits (10MHz)		Units
			Min	Max	Min	Max	
t_{A1VR1V}	$\overline{AEN1}$, $\overline{AEN2}$ Setup to RDY1, RDY2		15		15		ns
t_{AYVCL}	$\overline{ASYNC}$ Setup to CLK		50		50		ns
t_{CH1CH2} t_{CL2CL1}	CLK Rise or Fall Time	1.0V to 3.5V		10		10	ns
t_{CHCL}	CLK HIGH Time		$^1/_3t_{CLCL}$+2		$^1/_3t_{CLCL}$+2		ns
t_{CLA1X}	$\overline{AEN1}$, $\overline{AEN2}$ Hold to CLK		0		0		ns
t_{CLAYX}	$\overline{ASYNC}$ Hold to CLK		0		0		ns
t_{CLCH}	CLK LOW Time		$^2/_3t_{CLCL}$-15		$^2/_3t_{CLCL}$-15		ns
t_{CLCL}	CLK Cycle Period		125		100		ns
t_{CLI1H}	$\overline{RES}$ Hold to CLK	(Note 2)	10		10		ns
t_{CLIL}	CLK to Reset Delay			40		40	ns
t_{CLR1X}	RDY1, RDY2 Hold to CLK		0		0		ns
t_{CLPH}	CLK to PCLK HIGH Delay			22		22	ns
t_{CLPL}	CLK to PCLK LOW Delay			22		22	ns
t_{EHEL}	External Frequency HIGH Time	90%-90% V_{IN}	13		13		ns
t_{EHYL}	CSYNC Hold to EFI		10		10		ns
t_{ELEH}	External Frequency LOW Time	10%-10% V_{IN}	13		13		ns
t_{ELEL}	EFI Period	(Note 1)	36		33		ns
t_{I1HCL}	$\overline{RES}$ Setup to CLK	(Note 2)	65		65		ns
t_{IHIL}	Input Fall Time	(Note 1)		15		15	ns
t_{ILIH}	Input Rise Time	(Note 1)		15		15	ns
t_{OLCH}	OSC to CLK HIGH Delay		-5	22	-5	22	ns
t_{OLCL}	OSC to CLK LOW Delay		2	35	2	35	ns
t_{OLOH}	Output Rise Time (except CLK)	From 0.8V to 2.0V		15		15	ns
t_{OHOL}	Output Fall Time (except CLK)	From 2.0V to 0.8V		15		15	ns
t_{PHPL}	PCLK HIGH Time		t_{CLCL}-20		t_{CLCL}-20		ns
t_{PLPH}	PCLK LOW Time		t_{CLCL}-20		t_{CLCL}-20		ns
t_{R1VCH}	RDY1, RDY2 Active Setup to CLK	$\overline{ASYNC}$ = LOW	35		35		ns
t_{R1VCL}	RDY1, RDY2 Active Setup to CLK	$\overline{ASYNC}$ = HIGH	35		35		ns
t_{RYHCH}	Ready Active to CLK	(Note 3)	$^2/_3t_{CLCL}$-15		$^2/_3t_{CLCL}$-15		ns
t_{RYLCL}	Ready Inactive to CLK	(Note 4)	-8		-8		ns
t_{YHEH}	CSYNC Setup to EFI		20		20		ns
t_{YHYL}	CSYNC Width		2·t_{ELEL}		2·t_{ELEL}		ns
	XTAL Frequency		2.4	25	2.4	30	MHz

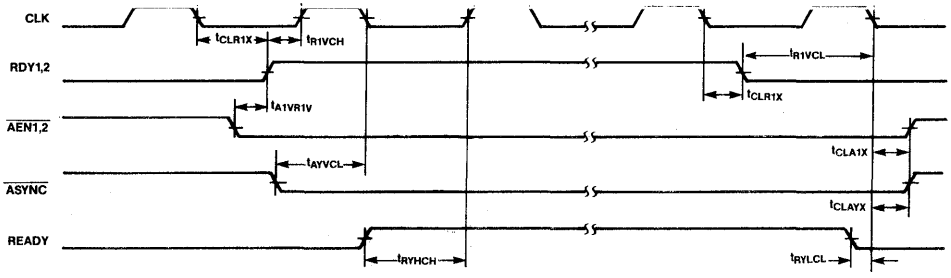
Notes:
1. Transition between V_{IL} (Max) - 0.4V and V_{IH} (Min) + 0.4V.
2. Setup and hold necessary only to guarantee recognition at next clock.
3. Applies only to T_3 and T_W states.
4. Applies only to T_2 states.

Figure 4: Timing Diagrams

a) Clocks and Reset Signals



b) Ready Signals (for Asynchronous Devices)



c) Ready Signals (for Synchronous Devices)

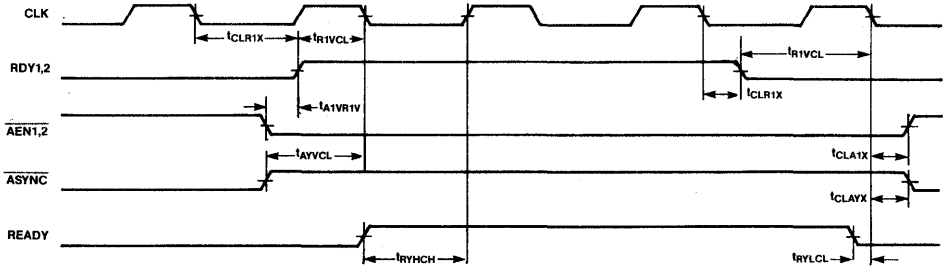
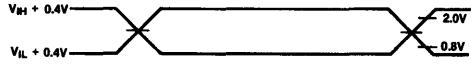
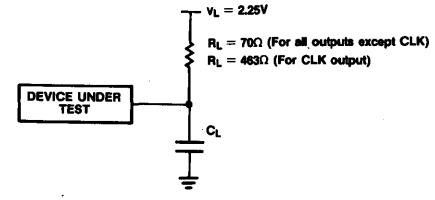


Figure 5: AC Testing I/O Waveform



A.C. Testing: All input signals must switch between 0.45V and 2.4V. T_{RISE} and T_{FALL} must be ≤ 15ns. All timing measurements are made at 0.8V and 2.0V.

Figure 6: AC Testing Loading Circuit



C_L = 100pF for CLK
C_L = 10pF for READY
C_L includes probe and jig capacitance

Figure 7: Clock High & Low Time (Using X1, X2)

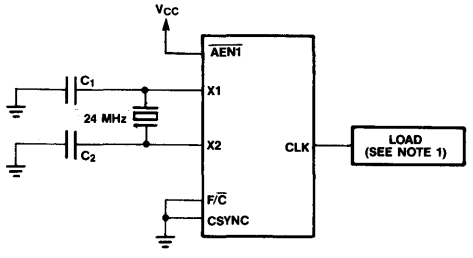


Figure 8: Clock High & Low Time (Using EFI)

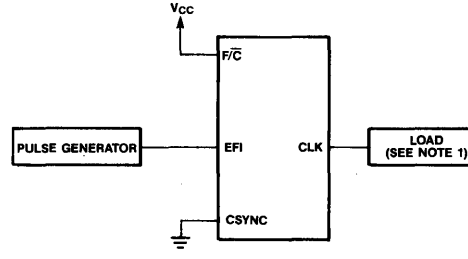


Figure 9: Ready to Clock (Using X1, X2)

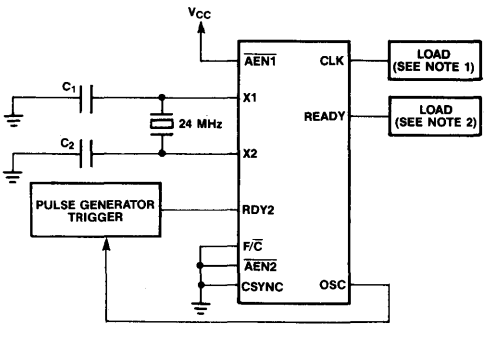
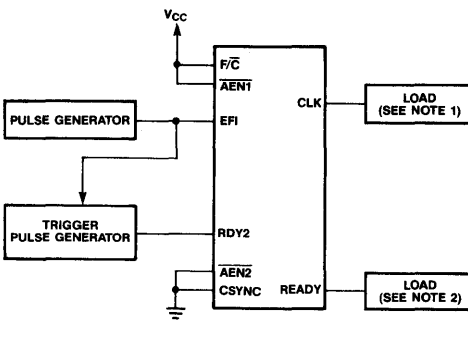


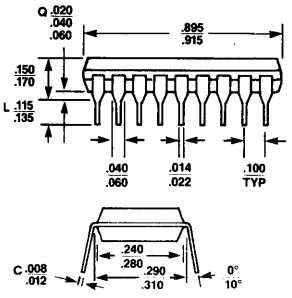
Figure 10: Ready to Clock (Using EFI)



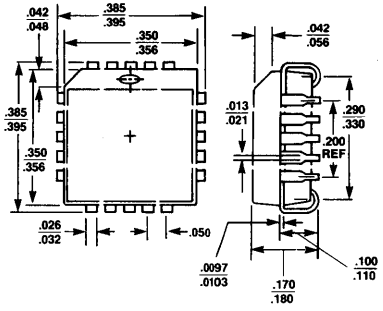
Notes: 1. C_L = 100pF
2. C_L = 30pF

PACKAGE DIMENSIONS

Units: Inches



Plastic Package



PLCC Package

ORDERING INFORMATION AND PRODUCT CODE

KS 82C84A X X X

SAMSUNG SEMICONDUCTOR

Part Number

Speed
-8 8MHz
-10 10MHz

Packaging
P — Plastic DIP
L — Plastic Leaded Chip Carrier (PLCC)

Temperature
C — Commercial (0°C to +70°C)
I — Industrial (-40°C to +85°C)

SAMSUNG products are designated by a Product Code. When ordering, please refer to products by their full code. For unusual, and/or specific packaging or processing requirements not covered by the standard product line, please contact the SAMSUNG MOS Product Group.

KS82C88A

MICROPROCESSOR BUS CONTROLLER

FEATURES/BENEFITS

- **Pin and functional compatibility with the Industry standard 8288**
- **Very high speed — 8MHz and 10MHz**
- **Low power CMOS implementation**
- **Bipolar drive capability**
- **TTL I/O compatibility**
- **3-state command output drivers**
- **Configurable for use with an I/O bus**
- **Facilitates interface to one or two multi-master buses**

DESCRIPTION

The KS82C88A Bus Controller is a 20-pin CMOS component which includes command and control timing generation as well as a bipolar bus drive capability while optimizing system performance. A strapping option on the bus controller configures it for use with a multi-master system bus and separate I/O bus.

The KS82C88A is manufactured using advanced CMOS technology. Fully static, with very high speed operation, the KS82C88A is designed for use in medium-to-large 8088/86 microprocessor systems.

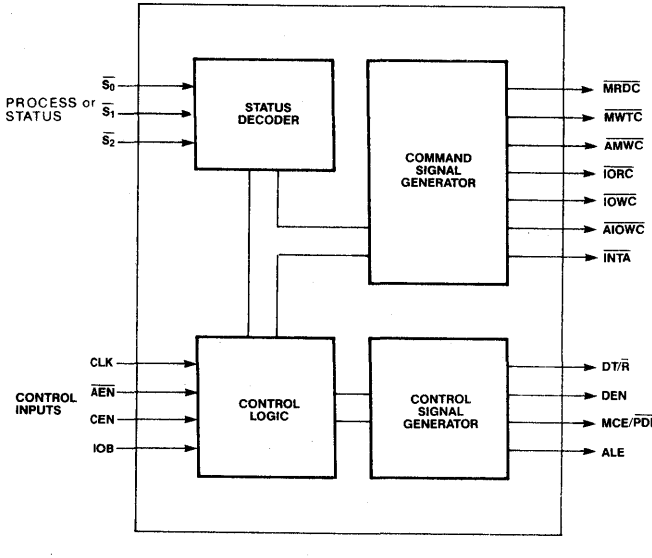


Figure 2: KS82C88 Block Diagram

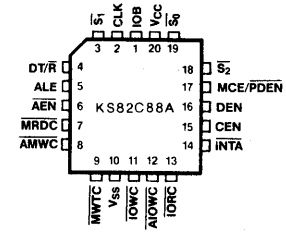


Figure 1a: 20-Pin PLCC Configuration

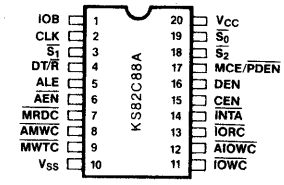


Figure 1b: 20-Pin DIP Configuration

Table 1a: PLCC Pin Assignment

Pin #	I/O	Pin Name	Pin #	I/O	Pin Name
1	I	IOB	11	O	$\overline{IOWC}$
2	I	CLK	12	O	$\overline{AIOWC}$
3	I	$\overline{S_1}$	13	O	$\overline{IORC}$
4	O	DT/$\overline{R}$	14	O	$\overline{INTA}$
5	O	ALE	15	I	CEN
6	I	$\overline{AEN}$	16	O	DEN
7	O	$\overline{MRDC}$	17	O	MCE/$\overline{PDEN}$
8	O	$\overline{AMWC}$	18	I	$\overline{S_2}$
9	O	$\overline{MWTC}$	19	I	$\overline{S_0}$
10	—	V_{SS}	20	—	V_{CC}

Table 1b: 20-Pin DIP Pin Assignment

Pin #	I/O	Pin Name	Pin #	I/O	Pin Name
1	I	IOB	11	O	$\overline{IOWC}$
2	I	CLK	12	O	$\overline{AIOWC}$
3	I	$\overline{S_1}$	13	O	$\overline{IORC}$
4	O	DT/$\overline{R}$	14	O	$\overline{INTA}$
5	O	ALE	15	I	CEN
6	I	$\overline{AEN}$	16	O	DEN
7	O	$\overline{MRDC}$	17	O	MCE/$\overline{PDEN}$
8	O	$\overline{AMWC}$	18	I	$\overline{S_2}$
9	O	$\overline{MWTC}$	19	I	$\overline{S_0}$
10	—	V_{SS}	20	—	V_{CC}

Table 2: Pin Descriptions

Symbol	Type	Name and Function
$\overline{AEN}$	I	**Address Enable:** $\overline{AEN}$ enables the KS82C88 command outputs at least t_{AELCV} (Table 4) after it becomes active (LOW). When $\overline{AEN}$ goes inactive, the command output drivers are immediately 3-stated. $\overline{AEN}$ does not affect the I/O command lines if the KS82C88 is in the I/O Bus mode (IOB tied HIGH).
$\overline{AIOWC}$	O	**Advanced I/O Write Command:** The $\overline{AIOWC}$ issues an I/O Write command earlier in the machine cycle to give I/O devices an early indication of a write instruction. Its timing is the same as a read command signal. This signal is active LOW.
ALE	O	**Address Latch Enable:** This signal serves to strobe an address into the address latches. It is active HIGH and latching occurs on the falling (HIGH to LOW) transition. ALE is intended for use with transparent D type latches.
$\overline{AMWC}$	O	**Advanced Memory Write Command:** This active LOW signal is used to issue a memory write command earlier in the machine cycle to give memory devices an early indication of a write instruction. Its timing is the same as a read command signal.
CEN	I	**Command Enable:** When LOW all KS82C88 command outputs, and the control outputs DEN and $\overline{PDEN}$ are forced to the inactive state. When HIGH, these outputs are enabled.
CLK	I	**Clock:** This clock signal from the KS82C88 clock generator is used to determine when command and control signals are generated.
DEN	O	**Data Enable:** This active HIGH signal enables data transceivers onto either the local or system data bus.
DT/$\overline{R}$	O	**Data Transmit/Receive:** This signal establishes the direction of data flow through the transceivers. HIGH indicates Transmit (write to I/O or memory), LOW indicates Receive (Read).
$\overline{INTA}$	O	**Interrupt Acknowledge:** This active LOW signal tells an interrupting device that its interrupt has been acknowledged and that it should drive vector information onto the data bus.
IOB	I	**Input/Output Bus Mode:** When IOB is strapped HIGH the KS82C88 functions in the I/O Bus mode. When strapped LOW, the KS82C88 functions in the System Bus mode. (See sections on I/O Bus and System Bus modes)

Table 2: Pin Descriptions (Continued)

Symbol	Type	Name and Function
$\overline{IORC}$	O	**I/O Read Command:** This active LOW signal instructs an I/O device to drive its data onto the data bus.
$\overline{IOWC}$	O	**I/O Write Command:** This active LOW signal instructs an I/O device to read the data on the data bus.
MCE/$\overline{PDEN}$	O	**MCE (IOB is tied LOW):** Master Cascade Enable occurs during an interrupt sequence and serves to read a Cascade Address from a master PIC (Priority Interrupt Controller) onto the data bus. The MCE signal is active HIGH. **$\overline{PDEN}$ (IOB is tied HIGH):** Peripheral Data Enable enables the data bus transceiver for the I/O bus that DEN performs.
$\overline{MRDC}$	O	**Memory Read Command:** This active LOW signal instructs the memory to drive its data onto the data bus.
$\overline{MWTC}$	O	**Memory Write Command:** This active LOW signal instructs the memory to record the data present on the data bus.
$\overline{S}_0$, $\overline{S}_1$, $\overline{S}_2$	I	**Status Input Pins:** These are status input pins from 8088/86/89 processors. The KS82C88 decodes these inputs to generate command and control signals at the appropriate time. These pins are HIGH when not in use. Internal pull-up resistors hold these lines HIGH when no other driving source is present.
V_{CC}	—	**Power:** 5V ± 10% DC Supply.
V_{SS}	—	**Ground:** 0V.

FUNCTIONAL DESCRIPTION

Command and Control Logic

The KS82C88A decodes the status line signals ($\overline{S}_0$, $\overline{S}_1$, $\overline{S}_2$) common to the 8086/88/89 processors to determine what command is to be issued, (Table 3).

Table 3: KS82C88A Commands

$\overline{S}_2$	$\overline{S}_1$	$\overline{S}_0$	Processor State	8288A Command
0	0	0	Interrupt Acknowledge	$\overline{INTA}$
0	0	1	Read I/O Port	$\overline{IORC}$
0	1	0	Write I/O Port	$\overline{IOWC}$, $\overline{AIOWC}$
0	1	1	Halt	None
1	0	0	Code Access	$\overline{MRDC}$
1	0	1	Read Memory	$\overline{MRDC}$
1	1	0	Write Memory	$\overline{MWTC}$, $\overline{AMWC}$
1	1	1	Passive	None

Operating Modes

The KS82C88A can be operated in one of two modes, I/O Bus Mode or System Bus Mode according to the system hardware configuration.

I/O Bus Mode: *(IOB Strapped HIGH)*

In the I/O Bus (IOB) mode the I/O command lines ($\overline{IORC}$, $\overline{IOWC}$, $\overline{AIOWC}$, $\overline{INTA}$) are always enabled (not dependent on $\overline{AEN}$). When an I/O command is initiated by the processor, the KS82C88A immediately activates the command lines using $\overline{PDEN}$ and DT/$\overline{R}$ control the I/O bus transceiver. Since no arbitration is present, the I/O command lines should not be used to control the sytem bus in this mode. This mode allows one KS82C88A to handle two external buses. No waiting is involved when the CPU wants to gain access to the I/O bus. Normal memory access requires a Bus Ready signal ($\overline{AEN}$ LOW) before proceeding. The IOB mode is aimed at applications where I/O or peripherals dedicated to one processor exist in a multi-processor system.

System Bus Mode: *(IOB Strapped LOW)*

In this mode no commands are issued until t_{AELCV} (Table 4) after the $\overline{AEN}$ Line is activated (LOW). This mode assumes that bus arbitration logic will inform the bus controller (on the $\overline{AEN}$ line) when the bus is free for use. Both memory and I/O commands wait for bus arbitration. This mode is used when only one bus exists, and both I/O and memory are shared by more than one processor.

Table 4: Command Outputs

$\overline{MRDC}$	Memory Read Command
$\overline{MWTC}$	Memory Write Command
$\overline{IORC}$	I/O Read Command
$\overline{IOWC}$	I/O Write Command
$\overline{AMWC}$	Advanced Memory Write Command
$\overline{AIOWC}$	Advanced I/O Write Command
$\overline{INTA}$	Interrupt Acknowledge

Command Outputs

Advanced write commands prevent the processor from entering unnecessary wait states. They are available to initiate write procedures early in the machine cycle.

$\overline{INTA}$ (Interrupt Acknowledge) acts as an I/O read during an interrupt cycle. $\overline{INTA}$ informs an interrupting device that it should place service vectors onto the data bus.

Control Outputs

KS82C88A control outputs include Data Enable (DEN), Data Transmit/Receive (DT/$\overline{R}$) and Master Cascade Enable/Peripheral Data Enable (MCE/$\overline{PDEN}$). DEN determines when the external bus should be enabled onto the local bus and DT/$\overline{R}$ determines the direction of data transfer. These two signals are usually connected to the transceiver chip select and direction pins.

MCE/$\overline{PDEN}$ alters its function with the operating mode. In the IOB mode, the $\overline{PDEN}$ signal serves as a dedicated data enable signal for the I/O or Peripheral System Bus.

In the System Bus Mode, MCE is used during interrupt acknowledge cycles. Two interrupt acknowledge cycles occur back to back during interrupt sequences, with no data or address transfers during the first cycle. Thus logic should be provided to mask off MCE. Just before the second cycle, MCE gates a master Priority Interrupt Controller's (PIC) cascade address onto the processor's local bus where ALE strobes it into the address latches. On the leading edge of the second interrupt cycle, the addressed slave PIC gates an interrupt vector onto the system data bus where it is read by the processor.

If the system contains only one PIC, MCE is not used and the second Interrupt Acknowledge signal gates the interrupt vector onto the processor bus.

Address Latch Enable (ALE) and Halt

ALE occurs every machine cycle and strobes the current address into the address latches. ALE also strobes $\overline{S_0}$, $\overline{S_1}$, $\overline{S_2}$ into a latch for halt state decoding.

Command Enable (CEN)

CEN is a command qualifier for the KS82C88A. If CEN is HIGH, the KS82C88A functions normally, and all command lines are held in their inactive state (note 3-state). This feature can be used to implement memory partitioning and to eliminate address conflicts between system bus and resident bus devices.

Table 5: Recommended Operating Conditions

DC Supply Voltage		+4.0V to +6.0V
Operating Temperature Range	Commercial	0°C to 70°C
	Industrial	-40°C to +85°C

Table 6: Absolute Maximum Ratings

DC Supply Voltage	+7.0V
Input, Output or I/O Voltage Applied	V_{SS}-0.5V to V_{CC}+0.5V
Storage Temperature Range	-65°C to +150°C
Maximum Package Power Dissipation	1W

Note: Stresses beyond those listed above may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 7: DC Characteristics (T_A = 0°C to 70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V)

Symbol	Parameter		Test Conditions	Limits Min	Limits Max	Units
C_{IN}	Input Capacitance		Freq. = 1MHz Unmeasured pins at V_{SS}		5	pF
C_{OUT}	Output Capacitance				15	pF
I_{BHH}	Input Leakage Current (Bus Hold High)		V_{IN} = 2.0V (Notes 3, 4)	-50	-300	μA
I_{BHHO}	Bus Hold High Overdrive		(Notes 3, 5)	-600		μA
I_{CC}	Operating Supply Current		V_{IN} = V_{CC} or V_{SS}, V_{CC} = 5.5V Outputs Unloaded, Freq 5MHz		5	mA
I_{CCS}	Standby Supply Current		V_{IN} = V_{CC} or V_{SS}, V_{CC} = 5.5V Outputs Unloaded		100	μA
I_{LI}	Input Leakage Current		0V ≤ V_{IN} ≤ V_{CC} (Notes 1, 2)		±10	μA
I_{LO}	Output Leakage Current		0V ≤ V_{OUT} ≤ V_{CC}		±10	μA
V_{CH}	V_{IH} for Clock, $\overline{S}_0$, $\overline{S}_1$, $\overline{S}_2$			3.0	V_{CC}+0.3	V
V_{CL}	V_{IL} for Clock, $\overline{S}_0$, $\overline{S}_1$, $\overline{S}_2$				0.2V_{CC}	V
V_{IH}	Input High Voltage			2.2	V_{CC}+0.3	V
V_{IL}	Input Low Voltage			-0.3	0.8	V
V_{OH}	Output High Voltage	Command Outputs	I_{OH} = -5mA I_{OH} = -1mA	3.7 3.7		V V
		Control Outputs	I_{OH} = -4mA I_{OH} = -2.5mA	3.0 V_{CC}-0.4		V V
V_{OL}	Output LOW Voltage		I_{OL} = 12mA I_{OL} = 8mA		0.45 0.44	V V

Notes: 1. Except $\overline{S}_0$, $\overline{S}_1$, $\overline{S}_2$.
2. During input leakage test, maximum input rise and fall time should be 15ns between V_{CC} and V_{SS}.
3. $\overline{S}_0$, $\overline{S}_1$, $\overline{S}_2$ only.
4. Raise inputs to V_{CC}, then lower to 2.0V.
5. An external driver must sink at least I_{BHHO} to toggle a status line from HIGH to LOW.

Table 8: AC Characteristics, (T_A = 0°C to 70°C, V_{DD} = 5V ± 10%, V_{SS} = 0V)

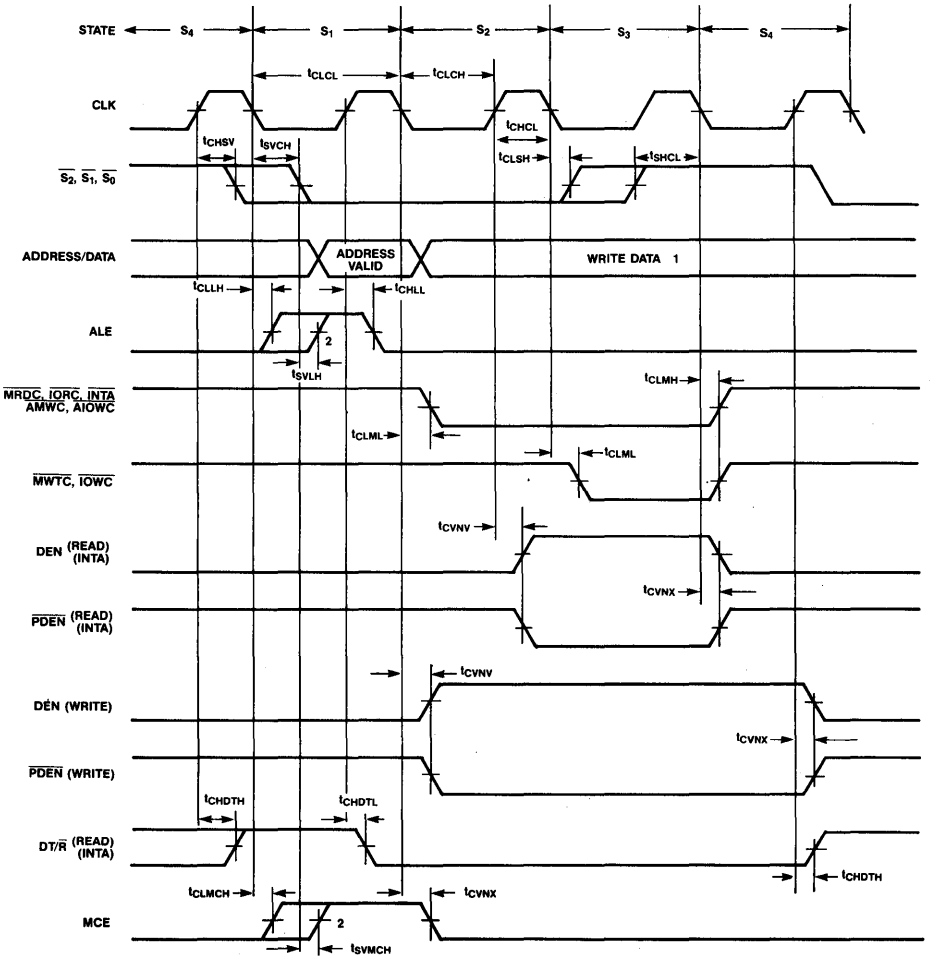
Symbol	Parameter	Test Conditions	Limits (8MHz)		Limits (10MHz)		Units
			Min	Max	Min	Max	
t_{AEHCZ}	Command Disable Time	D (Note 2)		40		40	ns
t_{AELCH}	Command Enable Time	C (Note 1)		40		40	ns
t_{AELCV}	Enable Delay Time	B	100	250	100	200	ns
t_{AEVNV}	$\overline{AEN}$ to DEN	A		25		20	ns
t_{CELRH}	CEN to Command	B		t_{CLML}+10		t_{CLML}	ns
t_{CEVNV}	CEN to DEN, $\overline{PDEN}$	A		25		25	ns
t_{CHCL}	CLK High Time		40		30		ns
t_{CHDTH}	Direction Control Inactive Delay	A		30		30	ns
t_{CHDTL}	Direction Control Active Delay	A		50		50	ns
t_{CHLL}	ALE Inactive Delay	A (Note 3)	2	25	2	15	ns
t_{CHSV}	Status Inactive Hold Time		10		10		ns
t_{CLCH}	CLK Low Time		66		50		ns
t_{CLCL}	CLK Cycle Period		125		100		ns
t_{CLLH}	ALE Active Delay (from CLK)	A		20		20	ns
t_{CLMCH}	MCE Active Delay (from CLK)	A		25		20	ns
t_{CLMH}	Command Inactive Delay	B	2	35	2	35	ns
t_{CLML}	Command Active Delay	B	5	35	5	35	ns
t_{CLSH}	Status Active Hold Time		10		10		ns
t_{CVNV}	Control Active Delay	A	2	45	2	45	ns
t_{CVNX}	Control Inactive Delay	A	5	45	5	45	ns
t_{MHNL}	Command Inactive to DEN Low Delay	Command: B, DEN: E	t_{CLCH}-5		t_{CLCH}-5		ns
t_{OHOL}	Output, Fall Time	From 2.0V to 0.8V		15		20	ns
t_{OLOH}	Output, Rise Time	From 0.8V to 2.0V		15		12	ns
t_{SHCL}	Status Inactive Setup Time		35		35		ns
t_{SVCH}	Status Active Setup Time		35		35		ns
t_{SVLH}	ALE Active Delay (from Status)	A		20		20	ns
t_{SVMCH}	MCE Active Delay (from Status)	A		30		20	ns

Refer to Figure 5 for Test Conditions Definition Table.

Notes: 1. t_{AELCH} measurement is between 1.5V and 2.5V.
2. t_{AEHCZ} measured at 0.5V change in V_{OUT}.
3. In 5MHz 80C86/88 systems, minimum ALE HIGH time = t_{CLCL} - (t_{CHSV}(max) + t_{SVLH}) + t_{CHLL}(min) = 74ns.

Figure 3: Timing Diagrams

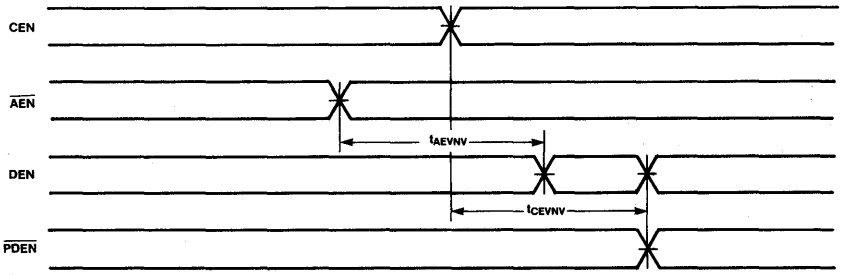
a) Read/Write Timing



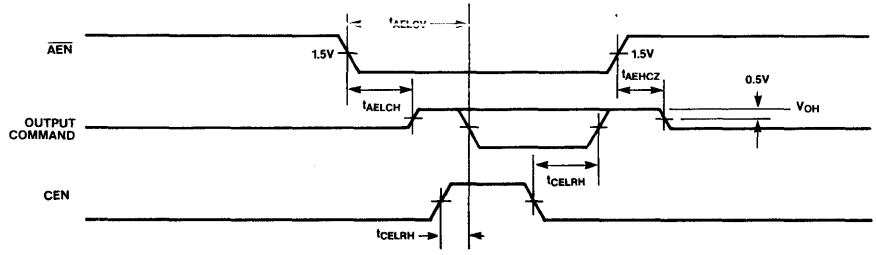
Notes: 1. Address/Data bus is shown only for reference purposes.
2. Leading edge of ALE and MCE is determined by the falling edge of CLK or STATUS going active, whichever occurs last.

Figure 3: Timing Diagrams (Continued)

b) DEN, PDEN Qualification Timing

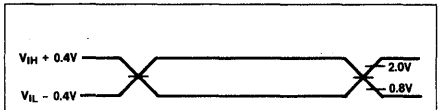


c) Address Enable Timing (3-State Enable/Disable)



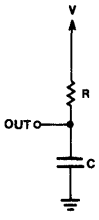
Note: CEN must be LOW or valid prior to S_2 to prevent the command from being generated.

Figure 4: AC Testing I/O Waveform



AC Testing: Inputs are driven at V_{IH} + 0.4V for a logic "1", and V_{IL} - 0.4V for a logic "0". The clock is driven at 3.9V and 0.4V. Timing measurements are made at 2.0V and 0.8V. Input rise and fall times should be ≤15ns measured between 0.8V and 2.0V.

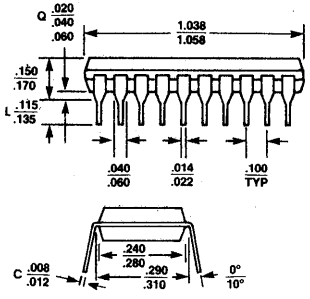
Figure 5: Test Load Circuits 3-State Command Output Test Load



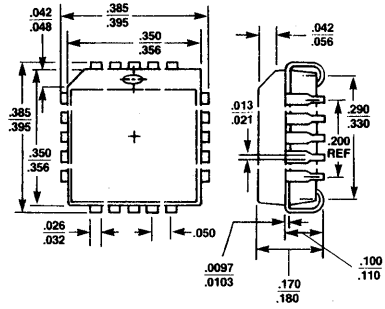
Test Condition	I_{OH}	I_{OL}	V (V)	R (Ω)	C (pF)
A	-4.0mA	+8.0mA	2.13	220	80
B	-8.0mA	+20.0mA	2.29	91	300
C	-8.0mA	—	1.5	187	300
D	-8.0mA	—	1.5	187	50
E	-1.0μA	+1.0μA	2.13	870K	30

PACKAGE DIMENSIONS

Units: Inches



Plastic Package



PLCC Package

ORDERING INFORMATION & PRODUCT CODE

KS 82C88A X X X

SAMSUNG SEMICONDUCTOR

Part Number

Speed
-8 8MHz
-10 10MHz

Packaging
P — Plastic DIP
L — Plastic Leaded Chip Carrier (PLCC)

Temperature
C — Commercial (0°C to +70°C)
I — Industrial (-40°C to +85°C)

SAMSUNG products are designated by a Product Code. When ordering, please refer to products by their full code. For unusual, and/or specific packaging or processing requirements not covered by the standard product line, please contact the SAMSUNG MOS Products Group.

FEATURES/BENEFITS

- **Provides commands and control for local and system bus in 80286-based machines**
- **Flexible command timing**
- **Works with KS82C289 Bus Arbiter and KS82C284 Clock Generator**
- **Optional IEEE-796 (Multibus®) compatible timing**
- **10, 12.5 MHz versions**
- **Supports high-speed, non-Multibus systems**
- **Control drivers with 16 mA I_{OL} and 3-state command drivers with 32 mA I_{OL}**
- **Single +5V supply**
- **Low-power CMOS**
- **20-lead PLCC or plastic DIP**

DESCRIPTION

The 20-pin CMOS KS82C288 controls buses in 80286-based computer systems. The Bus Controller provides command and control outputs with flexible timing options. Separate outputs are used for memory and I/O devices. The data bus is controlled with separate direction-control and data-enable signals.

Using a strapping option, the KS82C288 can be used for either Multibus-compatible bus cycles or high-speed bus cycles.

3

Figure 1. Block Diagram of KS82C288

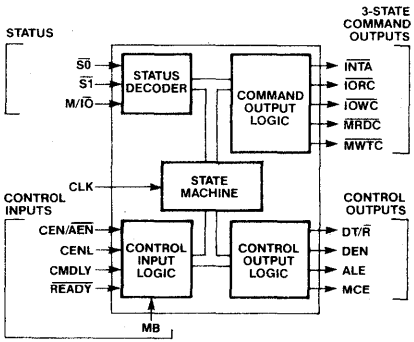


Figure 2a. KS82C288 PLCC Pin Diagram

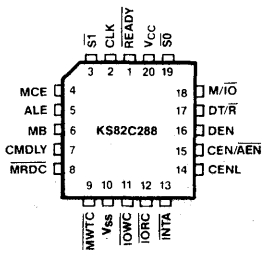


Figure 2b. KS82C288 DIP Pin Diagram

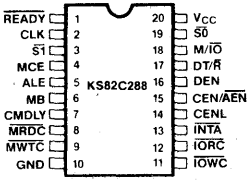


Table 1: KS82C288 Interface Signal Descriptions

Symbol	Type	Name and Function
CLK	I	**System Clock:** Provides the basic timing control for the KS82C288 in an 80286-based system. Its frequency is twice the internal processor clock frequency. The falling edge of CLK establishes when inputs are sampled and command and control outputs change.
$\overline{S0}$, $\overline{S1}$	I	**Status Signal 0, Status Signal 1:** These are bus cycle status signals that, along with M/$\overline{IO}$, start a bus signal and define the type of bus cycle. These signals are active LOW. A bus cycle is started when either $\overline{S0}$ or $\overline{S1}$ is sampled LOW at the falling edge of CLK. Setup and hold times must be met for these signals to operate properly. There are eight bus cycles defined by $\overline{S0}$, $\overline{S1}$, and M/$\overline{IO}$, as described below: **80286 Bus Cycles** M/$\overline{IO}$ | $\overline{S1}$ | $\overline{S0}$ | Type of Bus Cycle 0 | 0 | 0 | Interrupt Acknowledge 0 | 0 | 1 | I/O Read 0 | 1 | 0 | I/O Write 0 | 1 | 1 | None; Idle 1 | 0 | 0 | Halt, or Shutdown 1 | 0 | 1 | Memory Read 1 | 1 | 0 | Memory Write 1 | 1 | 1 | None; Idle
M/$\overline{IO}$	I	**Memory or I/O Select:** This signal determines whether the current bus cycle is in the memory space or in the I/O space. When LOW, the current bus cycle is in the I/O space. When HIGH, the current bus cycle is in the memory space. Setup and hold times must be met for proper operation.
MB	I	**Multibus Mode Select:** Determines the timing of the command and control outputs. When HIGH, the bus controller operates with Multibus I-compatible timings. When LOW, the bus controller optimizes the command and control output timing for short bus cycles. The function of the CEN/$\overline{AEN}$ pin is selected by this signal. This input is typically a strapping option and is not dynamically changed.
CENL	I	**Command Enable Latched:** A bus controller select signal which allows the Bus Controller to respond to the current bus cycle being initiated. CENL is an active-HIGH input latched internally at the end of each T_S cycle. CENL is used to select the appropriate bus controller for each bus cycle in a system where the CPU has more than one bus it can use. To select this KS82C288 for all transfers, connect CENL to V_{CC}. No control inputs affect CENL. Setup and hold times must be met for proper operation.
CMDLY	I	**Command Delay:** CMDLY allows the start of a command to be delayed. If sampled HIGH (active), the command output is not activated and CMDLY is again sampled at the next CLK cycle. When sampled LOW, the selected command is enabled. If $\overline{READY}$ is detected LOW before the command output is activated, the KS82C288 will terminate the bus cycle, even if no command was issued. If no delays are required before starting a command, CMDLY should be connected to GND. This input has no effect on KS82C288 control outputs. Setup and hold times must be satisfied for proper operation.

Table 1: KS82C288 Interface Signal Descriptions (Continued)

Symbol	Type	Name and Function
$\overline{READY}$	I	**Ready:** Indicates the end of the current bus cycle. Multibus I-mode requires at least one wait state to allow the command outputs to become active. $\overline{READY}$ must be active (LOW) during reset to force the KS82C288 into an idle state. Setup and hold times must be satisfied for proper operation. The KS82C284 Clock Generator drives $\overline{READY}$ LOW during RESET.
CEN/$\overline{AEN}$	I	**Command Enable, Address Enable:** Controls the command and DEN outputs of the KS82C288. CEN/$\overline{AEN}$ inputs may be asynchronous to CLK. Setup and hold times must be satisfied to assure a guaranteed response to synchronous inputs. When MB is HIGH, CEN/$\overline{AEN}$ has the $\overline{AEN}$ function. Active LOW, $\overline{AEN}$ indicates that the CPU has been granted the use of a shared bus and the bus controller command outputs may exit 3-state OFF and become inactive (HIGH). $\overline{AEN}$ HIGH indicates that the CPU does not have control of the shared bus and forces the command outputs into 3-state OFF and DEN inactive (LOW). When MB is LOW, this input has the CEN function. CEN is unlatched active HIGH input which allows the Bus Controller to activate its command and DEN outputs. With MB LOW, CEN LOW forces the command and DEN outputs inactive but does not tristate them. This input may be connected to V_{CC} or to GND.
ALE	O	**Address Latch Enable:** This signal controls the address latches used to hold an address stable during a bus cycle. ALE will not be issued for the halt bus cycle and is not affected by any of the control inputs.
MCE	O	**Master Cascade Enable:** Signals that a cascade address from a master KS82C59A interrupt controller may be placed onto the CPU address bus for latching by the address latches under ALE control. The CPU's address bus may then be used to broadcast the cascade address to slave interrupt controllers so only one of them will respond to the interrupt acknowledge cycle. MCE is only active during interrupt acknowledge cycles and is not affected by any control input. Using MCE to enable cascade address drivers requires latches which save the cascade address on the falling edge of ALE.
DEN	O	**Data Enable:** Controls when the data transceivers connected to the local data bus are enabled. DEN is delayed for write cycles in the Multibus I-mode.
DT/$\overline{R}$	O	**Data Transmit/Receive:** Establishes the direction of data flow to or from the local data bus. When HIGH, this control output indicates that a write bus cycle is being performed. When LOW, a read bus cycle is being performed. DEN is always inactive when DT/$\overline{R}$ changes states. This output is HIGH when no bus cycle is active. DT/$\overline{R}$ is not affected by any of the control inputs.
$\overline{IOWC}$	O	**I/O Write Command:** Instructs and I/O device to read the data on the data bus. The MB and CMDLY inputs control when this output becomes active. $\overline{READY}$ controls when this output becomes inactive.
$\overline{IORC}$	O	**I/O Read Comand:** Instructs an I/O device to place data onto the data bus. The MB and CMDLY inputs control when this output becomes active. $\overline{READY}$ controls when this output becomes inactive.
$\overline{MWTC}$	O	**Memory Write Command:** Instructs a memory device to read the data on the data bus. The MB and CMDLY inputs control when this output becomes active. $\overline{READY}$ controls when it becomes inactive.

Table 1: KS82C288 Interface Signal Descriptions (Continued)

Symbol	Type	Name and Function
$\overline{MRDC}$	O	**Memory Read Command:** Instructs the memory device to place data onto the data bus. The MB and CMDLY inputs control when this output becomes active. $\overline{READY}$ controls when it becomes inactive.
$\overline{INTA}$	O	**Interrupt Acknowledge:** Tells an interrupting device that its interrupt request is being acknowledged. The MB and CMDLY inputs control when this output becomes active. $\overline{READY}$ controls when it becomes inactive.
V_{CC}	—	5V ± 5%.
GND	—	Ground.

Table 2. Command and Control Outputs for Each Type of Bus Cycle

Type of Bus Cycle	M/$\overline{IO}$	$\overline{S1}$	$\overline{S0}$	Command Activated	DT/$\overline{R}$ State	ALE, DEN Issued?	MCE Issued?
Interrupt Acknowledge	0	0	0	$\overline{INTA}$	LOW	Yes	Yes
I/O Read	0	0	1	$\overline{IORC}$	LOW	Yes	No
I/O Write	0	1	0	$\overline{IOWC}$	HIGH	Yes	No
None; Idle	0	1	1	None	HIGH	No	No
Halt/Shutdown	1	0	0	None	HIGH	No	No
Memory Read	1	0	1	$\overline{MRDC}$	LOW	Yes	No
Memory Write	1	1	0	$\overline{MWTC}$	HIGH	Yes	No
None; Idle	1	1	1	None	HIGH	No	No

FUNCTIONAL DESCRIPTION

The KS82C288 Bus Controller provides 80286-based systems with address latch control, data transceiver control, and standard level-type command outputs. The Bus Controller can drive either IEEE-796 Multibus I buses or non-IEEE-796 buses. Command outputs have sufficient drive capabilities for large TTL buses.

A special Multibus I mode is provided to satisfy the address/data setup and hold time requirements of the IEEE-796 Standard.

Command timing may be tailored to special needs through the Bus Controller's $\overline{CMDLY}$ input (to determine the start of a command) and $\overline{READY}$ (to determine the end of a command).

Connection to multiple buses is supported with a latched enable input (CENL). An external address decoder can determine which, if any, Bus Controller should be enabled for the bus cycle. The CENL input is latched to allow the address decoder to take advantage of pipelined timing on the 80286 local bus.

Buses shared by several Bus Controllers are supported. The KS82C288's $\overline{AEN}$ input prevents the Bus Controller from driving the shared-bus command and data signals except when enabled by an external bus arbiter such as the KS82C289.

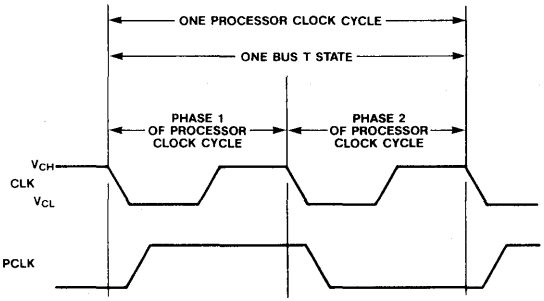
Data transceivers for all the buses are controlled by separate DEN and DT/$\overline{R}$ outputs. Bus contention is eliminated by disabling DEN before changing DT/$\overline{R}$. DEN timing allows enough time for tri-state bus-drivers to enter 3-state OFF before allowing other drivers onto the same bus.

CPU refers to any 80286 processor or 80286 support component which may become an 80286 bus master and thereby drive the KS82C288 status inputs $\overline{S0}$, $\overline{S1}$, and M/$\overline{IO}$.

OPERATIONAL DESCRIPTION

Any CPU driving the local bus uses and internal clock which is one half the frequency of the system clock (CLK). One 80286 processor bus cycle is equal to one bus T-state (see Figure 3). The local bus master informs the Bus Controller of its internal clock phase when it asserts the status signals. Status signals are always asserted at the beginning of Phase 1 of the local bus master's internal clock.

Figure 3. CLK Relationship to the Processor Clock and Bus T-States



KS82C288 Bus States

The KS82C288 has three bus states (see Figure 4). The three bus states are: Idle (T_I), Status (T_S), and Command (T_C). Each bus state is two CLK cycles long.

The T_I bus state occurs when no bus cycle is currently active on the 80286 local bus. This state may be repeated indefinitely. When control of the local bus is being passed between masters, the bus remains in the T_I state.

KS82C288 Bus Cycles

The $\overline{S0}$ and $\overline{S1}$ inputs from the master processor signal the start of a bus cycle. When either input goes LOW, a bus cycle is started. The T_S bus state is defined to be the two CLK cycles during which either $\overline{S0}$ or $\overline{S1}$ are active (see Figure 5). These inputs are sampled by the KS82C288 at every falling edge of CLK. When either $\overline{S0}$ or $\overline{S1}$ are sampled LOW, the next CLK cycle is considered the second phase of the internal CPU clock cycle.

The local bus enters the T_C bus state after the T_S state. The shortest bus cycle may have one T_S state and one T_C state. Longer bus cycles are formed by repeating the T_C state after the T_S state. A repeated T_C bus state is called a wait state.

The $\overline{READY}$ input determines whether the current T_C bus state will be repeated. The $\overline{READY}$ input has the same timing and effect for all bus cycles. $\overline{READY}$ is sampled at the end of each T_C bus state to see if it is active. If sampled HIGH, the T_C bus state is repeated to insert a wait state. Control and command outputs do not change during wait states.

When $\overline{READY}$ is sampled LOW, the current bus cycle is terminated.

The Bus Controller may enter the T_S bus state directly from T_C if the status lines are sampled active (LOW) at the next falling edge of CLK.

Figure 4. KS82C288 Bus States

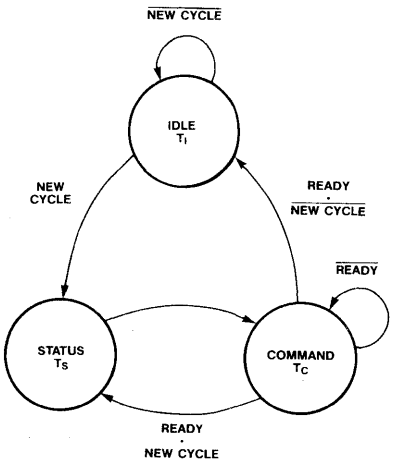
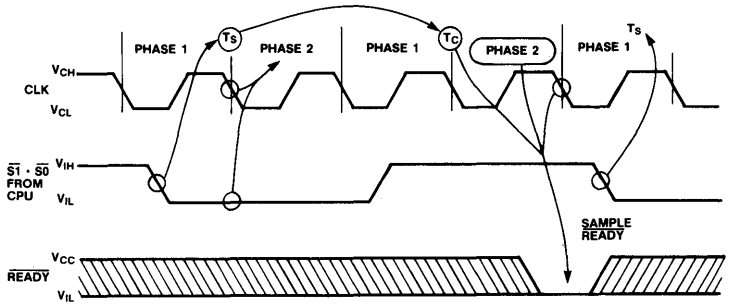


Figure 5. Bus Cycle Definition



Figures 6 through 10 show the basic command and control output timing for read and write bus cycles including the basic idle-read-idle and idle-write-idle bus cycles. Halt bus cycles are not shown because they activate no outputs.

The signal label CMD represents the appropriate command output for the bus cycle.

For figures 6 through 10, the CMDLY input is connected to GND and CENL is connected to V_{CC}. The effects of CENL and CMDLY are described in the section on control inputs.

Figures 6, 7, and 8 show non-Multibus I cycles. MB is connected to GND and CEN is connected to V_{CC} in non-Multibus cycles. Figure 6 shows a read cycle with no wait states while figure 7 shows a write cycle with one wait state. The READY input is shown to illustrate how wait states are added.

Figure 6. Idle-Read-Idle Bus Cycles with MB = 0

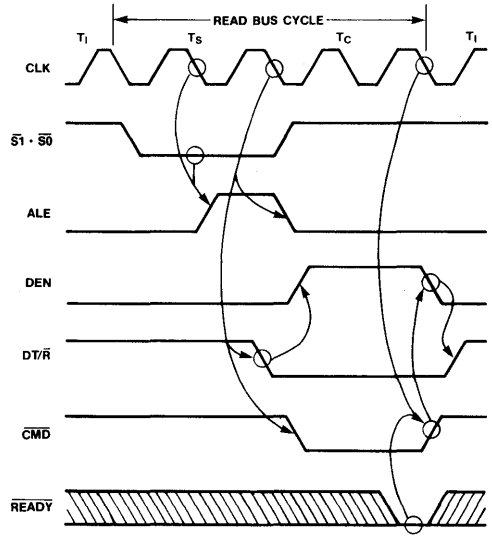


Figure 7. Idle-Write-Idle Bus Cycles with MB = 0

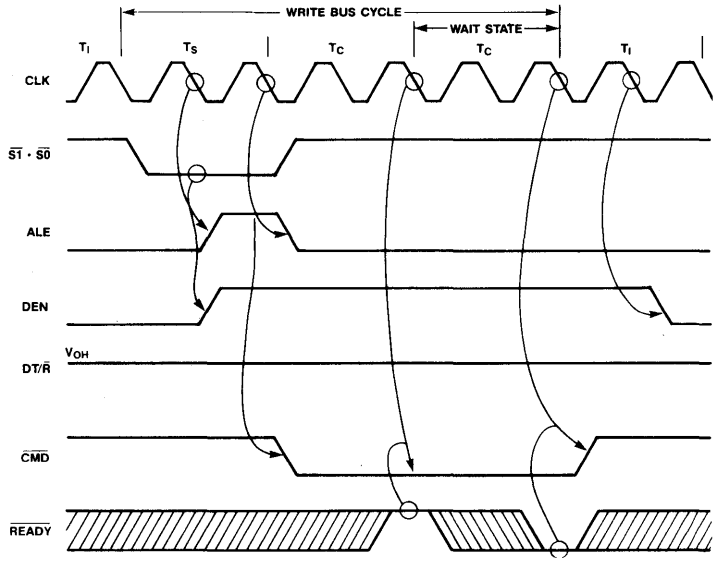
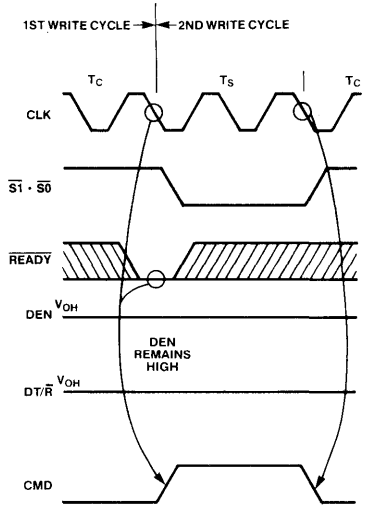


Figure 8. Write-Write Bus Cycles with MB = 0



Bus cycles can occur back-to-back with no T_I bus states between T_C and T_S. Back-to-back cycles do not affect the timing of the command and control outputs. Command and control outputs always match the states shown for the same clock edge (within T_S, T_C) or falling bus state of a bus cycle.

A special case in control timing occurs for back-to-back write cycles when MB = 0 (non-Multibus mode). In this case, DT/$\overline{R}$ and DEN remain HIGH between the bus cycles (see Figure 8). The command and ALE output timings do not change.

Figures 9 and 10 show a Multibus cycle (MB = 1). AEN and CMDLY are connected to GND. The effects of CMDLY and $\overline{AEN}$ are described in the section on control inputs. Figure 9 shows a read cycle with one wait state and Figure 10 shows a write cycle with two wait states. The second wait state of the write cycle is not required and is shown only for example. The $\overline{READY}$ input shows how wait states are added.

Figure 9. Idle-Read-Idle Bus Cycles with 1 Wait State and with MB = 1

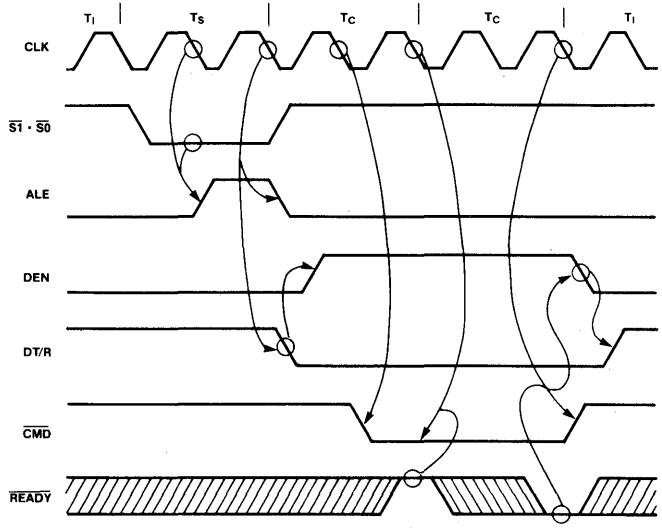
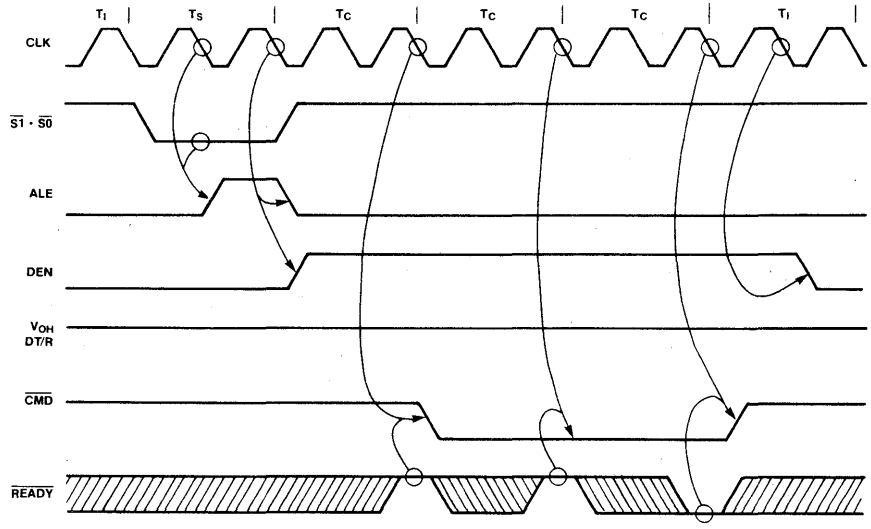


Figure 10. Idle-Write-Idle Bus Cycles with 2 Wait States in Multibus Mode (MB = 1)



The MB control input affects the timing of the command and DEN outputs. These outputs are automatically delayed in Multibus 1 mode to satisfy three requirements:

1) 50 ns minimum setup time for valid address before any command output becomes active
2) 50 ns minimum setup time for valid write data before any write command output becomes active
3) 65 ns maximum time from when any read command becomes inactive until the slave's read data drivers reach 3-state OFF.

Three signal transitions are delayed by MB = 1:

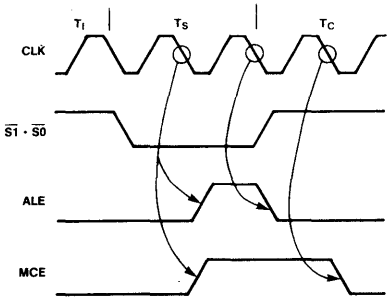
1) The HIGH-to-LOW transition of the read command outputs ($\overline{IORC}$, $\overline{MRDC}$, and $\overline{INTA}$) are delayed by one CLK cycle
2) The HIGH-to-LOW transition of the write command outputs ($\overline{IOWC}$ and $\overline{MWTC}$) are delayed by two CLK cycles.
3) The LOW-to-HIGH transition of DEN for write cycles is delayed one CLK cycle.

Back-to-back bus cycles with MB = 1 do not change the timing of any of the command or control outputs. DEN always becomes inactive between bus cycles with MB = 1.

ALE will be issued during the second half of T_S for any bus cycle except for a halt (shutdown) bus cycle. ALE becomes inactive at the end of T_S to allow latching the address to keep it stable during the entire bus cycle. The address outputs may change during Phase 2 of any T_C bus state. ALE is not affected by any control input.

Figure 11 shows how MCE is timed during Interrupt Acknowledge ($\overline{INTA}$) bus cycles. MCE is one CLK cycle longer than ALE to hold the cascade address from a master KS82C59A Programmable Interrupt Controller valid after the falling edge of ALE. With the exception of the MCE control output, an $\overline{INTA}$ bus cycle is identical in timing to a read bus cycle. MCE is not affected by any control input.

Figure 11. MCE Operation for an $\overline{INTA}$ Bus Cycle



Control Inputs

The control inputs (CENL, CMDLY, $\overline{READY}$, CEN/$\overline{AEN}$) can alter the basic timing of command outputs, allow interfacing to multiple buses, and share a bus between different masters. In many 80286-based systems, each CPU has more than one bus which may be used to perform a bus cycle. Normally, a CPU will have only one Bus Controller active for each bus cycle. Some buses may be shared by more than one CPU, as in Multibus configurations, requiring only one of them to use the bus at a time.

Systems with multiple and shared buses use two control input signals from the KS82C288 bus controller, CENL and $\overline{AEN}$ (see figure 12). CENL enables the Bus Controller to control the current bus cycle. The $\overline{AEN}$ input prevents a bus controller from driving its command outputs. $\overline{AEN}$ HIGH means that another bus controller may be driving the shared bus.

Figure 12 shows two buses: a local bus and a Multibus I. Only one bus is used for each CPU bus cycle. The CENL inputs of the Bus Controller select which bus controller is to perform the bus cycle. An address decoder determines which bus to use for each bus cycle. The Bus Controller connected to the shared Multibus I must be selected by CENL and be given access to the Multibus I by $\overline{AEN}$ before it will begin a Multibus I operation.

CENL must be sampled HIGH at the end of the bus state (see waveforms) to allow the bus controller to activate its command and control outputs. If sampled LOW, the commands and DEN will not go active and DT/$\overline{R}$ will remain HIGH. In this situation, the Bus Controller will ignore the CMDLY, CEN, and $\overline{READY}$ inputs until another bus cycle is started via $\overline{S0}$ and $\overline{S1}$. Since an address decoder is commonly used to identify which bus is required for each bus cycle, CENL is latched internally, so the input does not have to be latched.

The CENL input can affect the DEN control output. When MB = 0, DEN normally becomes active during Phase 2 of T_S in write bus cycles. This transition occurs before CENL is sampled. If CENL is sampled LOW, then the DEN output will be forced LOW during T_C as shown in the timing waveforms.

When MB = 1, CEN/$\overline{AEN}$ becomes $\overline{AEN}$. $\overline{AEN}$ controls when the Bus Controller command outputs enter and exit 3-state OFF. $\overline{AEN}$ should be driven by a Multibus I type bus arbiter such as the KS82C289, which assures only one bus controller is driving the shared bus at any one time.

When $\overline{AEN}$ makes a LOW-to-HIGH transition, the command outputs immediately enter 3-state OFF and DEN is forced inactive. An inactive DEN should force the local data transceivers connected to the shared data bus into 3-state OFF (see figure 12). The LOW-to-HIGH transition of $\overline{AEN}$ should occur during T_I or T_S bus states.

The HIGH-to-LOW transition of $\overline{AEN}$ signals that the Bus Controller may now drive the shared bus command signals. Since a bus cycle may be active or be in the process of starting, $\overline{AEN}$ can become active during any T-state. $\overline{AEN}$ LOW immediately allows DEN to go to the appropriate state. Three CLK edges later, the command outputs will go active (see timing waveforms). The Multibus I requires this delay for the address and data to be valid on the bus before the command becomes active.

When MB = 0 (non-Multibus mode), CEN/$\overline{AEN}$ becomes CEN. CEN is an asynchronous input which immediately affects the command and DEN outputs. When CEN makes a HIGH-to-LOW transition, the commands and DEN are immediately forced inactive. When CEN makes a LOW-to-HIGH transition, the commands and DEN outputs immediately go to the appropriate state (see timing waveforms). $\overline{READY}$ must still become active to terminate a bus cycle if CEN remains LOW for a selected bus controller (CENL was latched HIGH).

Some memory or I/O systems may require more address or write data setup time than provided by the basic command output timing. To provide flexible command timing, the CMDLY input can delay the activation of command outputs. The CMDLY input must be sampled LOW to activate the command outputs. CMDLY does not affect the control outputs ALE, MCE, DEN, and DT/$\overline{R}$.

CMDLY is first sampled on the falling edge of the CLK ending T_S. If sampled HIGH, the command output is not activated, and CMDLY is again sampled on the next falling edge of CLK. Once sampled LOW, the proper command output becomes active immediately if MB = 0. If MB = 1, the proper command goes active no earlier than shown in figures 9 and 10.

$\overline{READY}$ can terminate a bus cycle before CMDLY allows a command to be issued. When $\overline{READY}$ does terminate a bus cycle before CMDLY allows a command to be issued, no commands are issued and the bus controller deactivates DEN and DT/$\overline{R}$ in the same manner as if a command had been issued.

Waveforms

The waveforms show the timing relationships of inputs and outputs. They do not show all possible transitions of all signals in all modes. Instead, all signal timing relationships are shown through general cases. Special cases are shown when necessary. Most functional descriptions of the KS82C288 are provided in figures 5 through 11, but the waveforms also provide some functional descriptions of the KS82C288.

To find the timing specification for a signal transition in a particular mode, first look for a special case in the waveforms. If no special case applies, then use a timing specification for the same or related function in another mode.

Figure 12. System Use of $\overline{AEN}$ and CENL

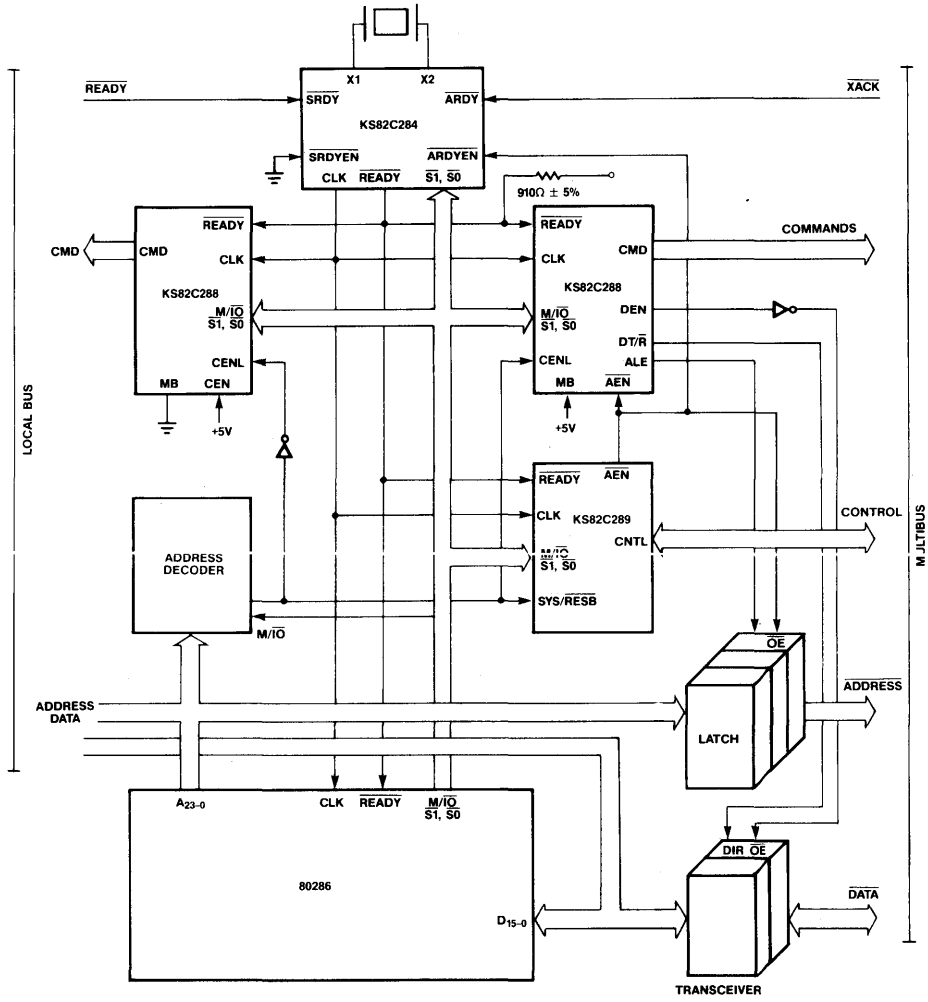


Table 3: Recommended Operating Conditions

DC Supply Voltage		+4.0V to +6.0V
Operating Temperature Range	Commercial	0°C to 70°C
	Industrial	-40°C to +85°C

Table 4: Absolute Maximum Ratings

DC Supply Voltage	+7.0V
Input, Output or I/O Voltage Applied	V_{SS}-0.5V to V_{CC}+0.5V
Storage Temperature Range	-65°C to +150°C
Maximum Package Power Dissipation	1W

Note: Stresses beyond those listed above may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 5: DC Characteristics (T_A = 0°C to 70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V)

Symbol	Parameter	Test Conditions	Min	Max	Units
V_{IL}	Input LOW Voltage		-0.5	0.8	V
V_{IH}	Input HIGH Voltage		2.0	V_{CC} + 0.5	V
V_{ILC}	CLK Input LOW Voltage		-0.5	0.6	V
V_{IHC}	CLK Input HIGH Voltage		3.8	V_{CC} + 0.5	V
V_{OL}	Output LOW Voltage				
	Command Outputs	I_{OL} = 32 mA (Note 1)		0.45	V
	Control Outputs	I_{OL} = 16 mA (Note 2)		0.45	V
V_{OH}	Output HIGH Voltage				
	Command Outputs	I_{OH} = -5 mA (Note 1)	2.4		V
		I_{OH} = -1 mA (Note 1)	V_{CC} - 0.5		V
	Control Outputs	I_{OH} = -1 mA (Note 2)	2.4		V
		I_{OH} = -0.2 mA (Note 2)	V_{CC} - 0.5		V
I_{IL}	Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}		±10	μA
I_{LO}	Output Leakage Current	0.45V ≤ V_{OUT} ≤ V_{CC}		±10	μA
I_{CC}	Power Supply Current			75	mA
I_{CCS}	Power Supply Current (Static)	(Note 3)		1	mA
C_{CLK}	CLK Input Capacitance	F_C = 1 MHz		12	pF
C_I	Input Capacitance	F_C = 1 MHz		10	pF
C_O	Input/Output Capacitance	F_C = 1 MHz		20	pF

* T_A is guaranteed from 0°C to +70°C as long as T_{CASE} is not exceeded.

Notes:

1. Command Outputs are $\overline{INTA}$, $\overline{IORC}$, $\overline{IOWC}$, $\overline{MRDC}$ and $\overline{MWRC}$.
2. Control Outputs are DT/$\overline{R}$, $\overline{DEN}$, ALE and MCE.
3. Tested while outputs are unloaded, and inputs at V_{CC} or V_{SS}.

Table 6: AC Characteristics (T_A = 0°C to 70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V)

Symbol	Parameter	Test Condition	8 MHz		10 MHz		12.5 MHz		16 MHz (Preliminary)		Unit
			-8 Min	-8 Max	-10 Min	-10 Max	-12 Min	-12 Max	-16 Min	-16 Max	
1	CLK Period		62	250	50	250	40	250	62	250	ns
2	CLK HIGH Time	at 3.6V	20		16		13		10		ns
3	CLK LOW Time	at 1.0V	15		12		11		9		ns
4	CLK Rise Time	1.0V to 3.6V		10		8		8		6	ns
5	CLK Fall Time	3.6V to 1.0V		10		8		8		6	ns
6	M/$\overline{IO}$ and Status Setup Time		22		18		15		12		ns
7	M/$\overline{IO}$ and Status Hold Time		1		1		1		1		ns
8	CENL Setup Time		20		15		15		15		ns
9	CENL Hold Time		1		1		1		1		ns
10	$\overline{READY}$ Setup Time		38		26		18		14		ns
11	$\overline{READY}$ Hold Time		25		25		20		16		ns
12	CMDLY Setup Time		20		15		15		12		ns
13	CMDLY Hold Time		1		1		1		1		ns
14	$\overline{AEN}$ Setup Time	(Note 3)	20		15		15		12		ns
15	$\overline{AEN}$ Hold Time	(Note 3)	0		0		0		0		ns
16	ALE, MCE Active Delay from CLK	(Note 4)	3	20	3	16	3	16	3	13	ns
17	ALE, MCE Inactive Delay from CLK	(Note 4)		25		19		19		15	ns
18	DEN (Write) Inactive from CENL	(Note 4)		35		23		23		18	ns
19	DT/$\overline{R}$ LOW from CLK	(Note 4)		25		23		23		18	ns
20	DEN (Read) Active from DT/$\overline{R}$	(Note 4)	5	35	5	21	5	21	5	17	ns
21	DEN (Read) Inactive Delay from CLK	(Note 4)	3	35	3	21	3	19	3	15	ns
22	DT/$\overline{R}$ HIGH from DEN Inactive	(Note 4)	5	35	5	20	5	18	5	14	ns
23	DEN (Write) Active Delay from CLK	(Note 4)		30		23		23		18	ns
24	DEN (Write) Inactive Delay from CLK	(Note 4)	3	30	3	19	3	19	3	15	ns
25	DEN Inactive from CEN	(Note 4)		35		25		25		20	ns
26	DEN Active from CEN	(Note 4)		30		24		24		19	ns
27	DT/$\overline{R}$ HIGH from CLK (when CEN = LOW)	(Note 4)		35		25		25		20	ns
28	DEN Active from $\overline{AEN}$	(Note 4)		30		26		26		20	ns

Table 6: AC Characteristics (T_A = 0°C to 70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V) (Continued)

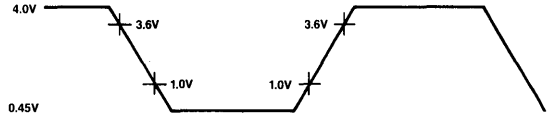
Symbol	Parameter	Test Condition	8 MHz		10 MHz		12.5 MHz		16 MHz (Preliminary)		Unit
			-8 Min	-8 Max	-10 Min	-10 Max	-12 Min	-12 Max	-16 Min	-16 Max	
29	$\overline{CMD}$ Active Delay from CLK	(Note 5)	3	25	3	21	3	21	3	17	ns
30	$\overline{CMD}$ Inactive Delay from CLK	(Note 5)	5	20	5	20	5	20	5	16	ns
31	$\overline{CMD}$ Active from CEN	(Note 5)		25		25		25		20	ns
32	$\overline{CMD}$ Inactive from CEN	(Note 5)		25		25		25		20	ns
33	$\overline{CMD}$ Inactive Enable from $\overline{AEN}$	(Note 5)		40		40		40		35	ns
34	$\overline{CMD}$ Float Delay from $\overline{AEN}$	(Note 6)		40		40		40		35	ns
35	MB Setup Time		20		20		20		20		ns
36	MB Hold Time		0		0		0		0		ns
37	Command Inactive Enable from MB↓	(Note 5)		40		40		40		35	ns
38	Command Float Time from MB↑	(Note 6)		40		40		40		35	ns
39	DEN Inactive from MB↑	(Note 4)		30		26		26		20	ns
40	DEN Active from MB↓	(Note 4)		30		30		30		24	ns

*T_A is guaranteed from 0°C to +70°C as long as T_{CASE} is not exceeded.

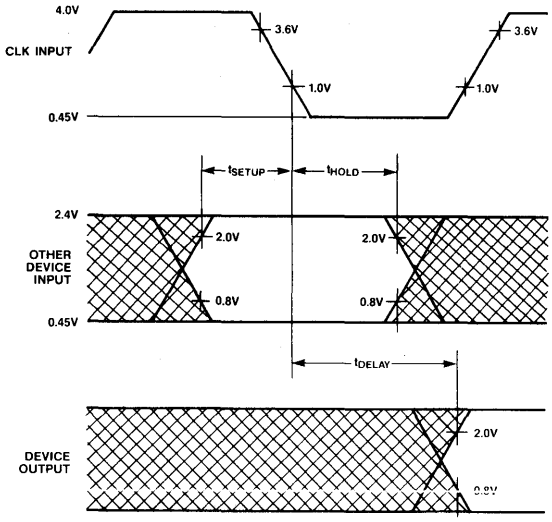
Notes:

3. $\overline{AEN}$ is an asynchronous input. This specification is for testing purposes only, to assure recognition at a specific CLK edge.
4. Control output load: CL = 150 pF.
5. Command output load: CL = 300 pF.
6. Float condition occurs when output current is less than I_{LO} in magnitude.
7. AC Drive and Measurement Points — CLK Input
8. AC Setup, Hold and Delay Time Measurement — General
9. AC Test Loading on Outputs

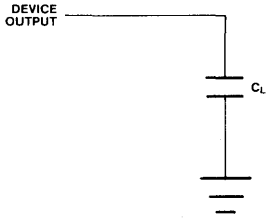
Note 7: AC Drive and Measurement Points — CLK Input



Note 8: AC Setup, Hold and Delay Time Measurement — General

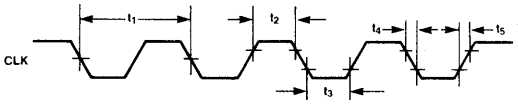


Note 9: AC Test Loading on Outputs

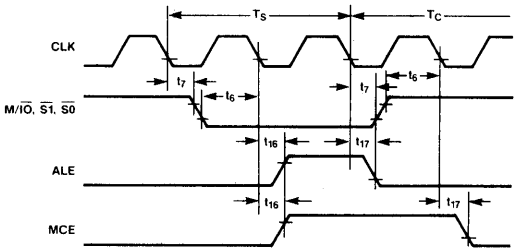


WAVEFORMS

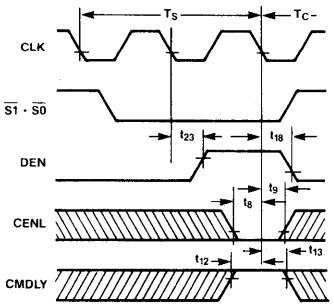
CLK Characteristics



Status, ALE, MCE Characteristics

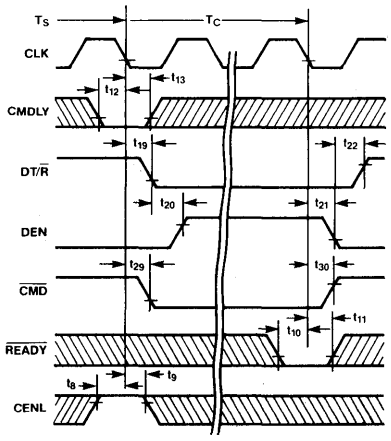


CENL, CMDLY, DEN Characteristics with MB = 0 and CEN = 1 During Write Cycle

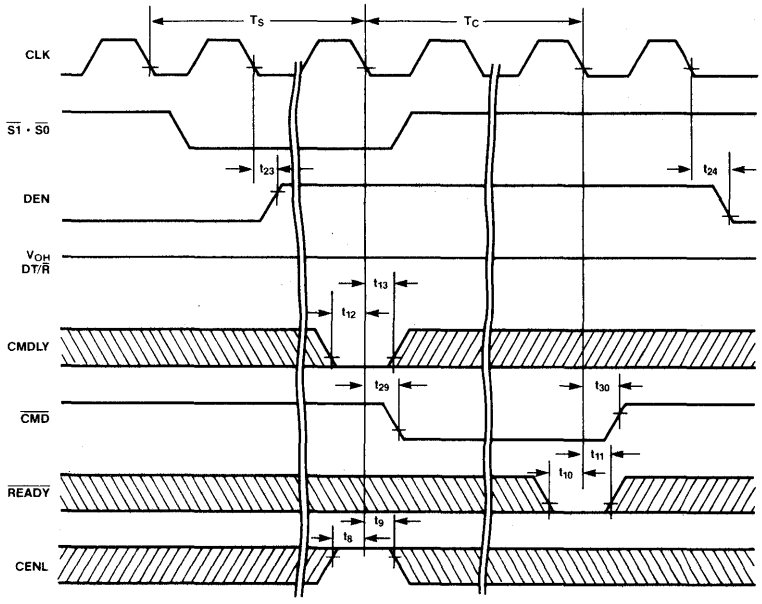


WAVEFORMS (Continued)

Read Cycle Characteristics with MB = 0 and CEN = 1

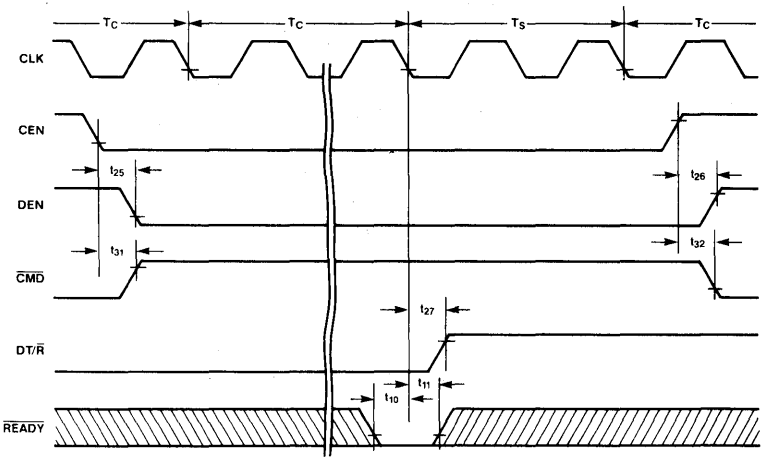


Write Cycle Characteristics with MB = 0 and CEN = 1

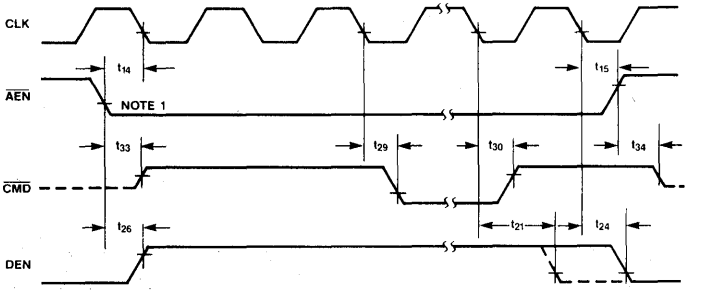


WAVEFORMS (Continued)

CEN Characteristics with MB = 0



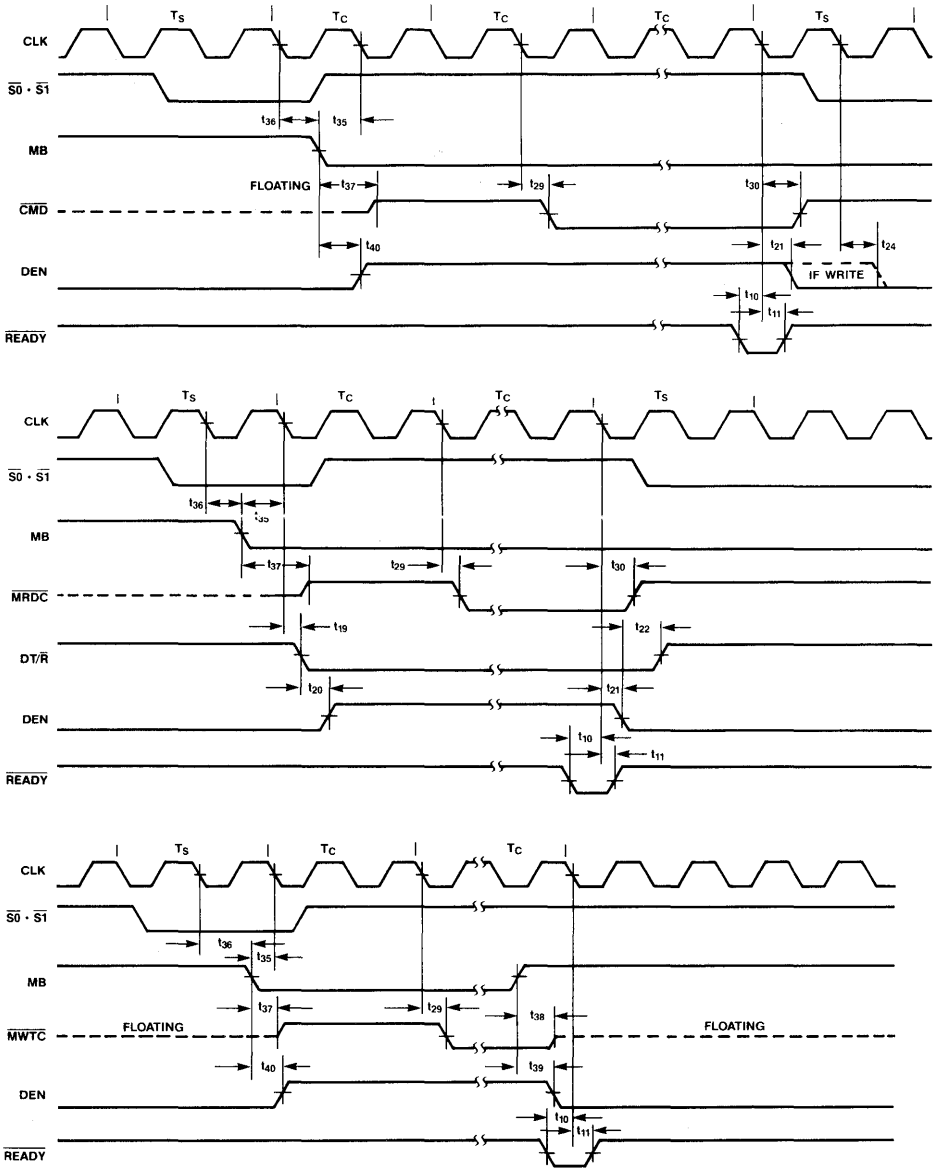
$\overline{AEN}$ Characteristics with MB = 1



Note:
1. AEN is an asynchronous input. AEN setup and hold time is specified to guarantee the response shown in the waveforms.

WAVEFORMS (Continued)

MB Characteristics with $\overline{AEN}$/CEN = High

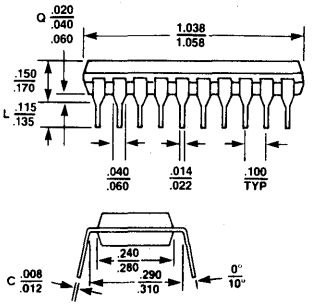


Note:

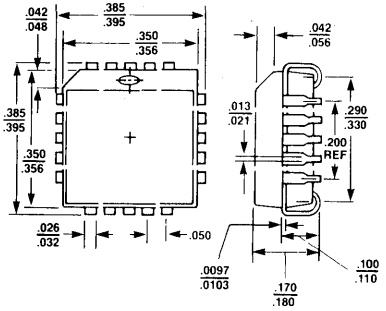
1. MB is an asynchronous input. MB setup and hold times specified to guarantee the response shown in the waveforms.
2. If the setup time, t35, is met two clock cycles will occur before CMD becomes active after the falling edge of MB.

PACKAGE DIMENSIONS

Units: Inches



20-Pin DIP



20-Pin PLCC

ORDERING INFORMATION AND PRODUCT CODE

KS 82C288 X X X

SAMSUNG SEMICONDUCTOR

Part Number

Speed

-8.0	8.0MHz
-10.0	10.0MHz
-12.5	12.5MHz

Packaging

P — Plastic DIP

L — Plastic Leaded Chip Carrier (PLCC)

Temperature

C — Commercial (0°C to +70°C)

I — Industrial (-40°C to +85°C)

SAMSUNG products are designated by a Product Code. When ordering, please refer to products by their full code. For unusual, and/or specific packaging or processing requirements not covered by the standard product line, please contact the SAMSUNG MOS Product Group.

KS82C289

BUS ARBITER

FEATURES/BENEFITS

- **Supports serial, parallel, and rotating priority resolving schemes**
- **Three modes of bus release operation**
- **Supports multi-master system bus arbitration protocol**
- **Compatible with IEEE 796 (MULTIBUS™) Standard**
- **Available in 20-pin plastic DIP**
- **8, 10, 12.5 MHz versions**
- **Low power CMOS**

DESCRIPTION

The Samsung KS82C289 20-pin CMOS Bus Arbiter signals to request, possess, and release the system bus. External logic determines which bus cycle requires the system bus and sets the priority of requests for control of the system bus.

The KS82C289 has processor-interface and Multibus state machines which support bus request and bus release logic.

The KS82C289 Bus Arbiter requires a Bus Controller, Clock Generator, and processor (bus master) to interface to the Multi-master System Bus.

3

Figure 1. KS82C289 Block Diagram

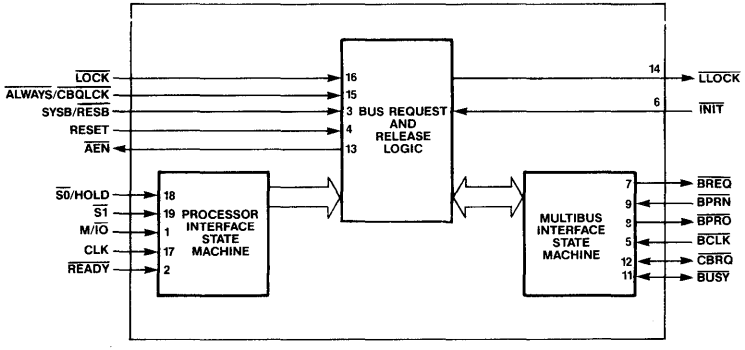


Figure 2a: 20-pin PLCC Configuration

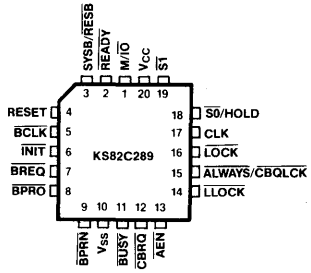


Figure 2b: 20-pin DIP Configuration

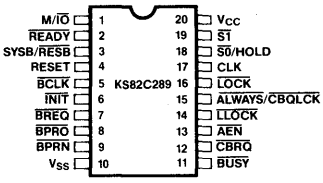


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Table 1. KS82C289 Pin Allocations in a 20-pin Plastic DIP

Note on Conventions: A bar over the signal name is used to denote an active low signal (S0). Active high signals are shown with no bar (HOLD).

Pin No.	Signal Abbrev.	Signal Name
1	M/$\overline{IO}$	Memory or I/O Select
2	$\overline{READY}$	Ready
3	SYSB/$\overline{RESB}$	System Bus/Resident Bus
4	RESET	Reset
5	$\overline{BCLK}$	Bus Clock
6	$\overline{INIT}$	Initialize
7	$\overline{BREQ}$	Bus Request
8	$\overline{BPRO}$	Bus Priority Out
9	$\overline{BPRN}$	Bus Priority In
10	V_{SS}	Ground

Pin No.	Signal Abbrev.	Signal Name
11	$\overline{BUSY}$	Busy
12	$\overline{CBRQ}$	Common Bus Request
13	$\overline{AEN}$	Address Enable
14	$\overline{LLOCK}$	Level Lock
15	$\overline{ALWAYS}$/ $\overline{CBQLCK}$	Always Release/Common Bus Request Clock
16	$\overline{LOCK}$	Lock
17	CLK	System Clock
18	$\overline{S0}$/HOLD	Status Input S0/Hold
19	$\overline{S1}$	Status Input S1
20	V_{CC}	VCC

Table 2. KS82C289 Signal Descriptions

Note: I indicates that the signal is an input to the KS82C289 chip. O indicates that the signal is an output from the KS82C289 chip.

Symbol	Type	Description
CLK	I	**System Clock:** Receives the CLK signal from the clock generator as a timing reference. The processor interface state machine (see Figure 1) is synchronous to the falling edge of CLK.
$\overline{S0}$/HOLD	I	**Status Input S0 or Hold:** Becomes active if $\overline{S0}$ is received from the processor or HOLD is received from the bus master. HOLD is selected if the $\overline{S0}$/HOLD pin is high at the falling edge of the processor RESET. $\overline{S0}$ is selected if $\overline{S0}$/HOLD pin is low at the falling edge of the processor reset.
$\overline{S1}$, M/$\overline{IO}$	I	**Status Input 1, Memory or Input/Output Select:** $\overline{S0}$, $\overline{S1}$, and M/$\overline{IO}$ are the status input signals from the processor. These inputs are decoded, along with $\overline{S0}$/HOLD, to start a bus request or to release the bus. If either $\overline{S1}$ or $\overline{S0}$ is low at the falling edge of the clock, a bus cycle is started. Bus Cycle Status Encoding

M/$\overline{IO}$	$\overline{S0}$	$\overline{S0}$/HOLD	Type of Bus Cycle
0	0	0	Interrupt acknowledge
0	0	1	I/O Read
0	1	0	I/O Write
0	1	1	None; bus idle
1	0	0	Halt or shutdown
1	0	1	Memory read
1	1	0	Memory write
1	1	1	None; bus idle

SYSB/$\overline{RESB}$	I	**System Bus/Resident Bus:** Decides when the multi-master system bus is needed for the current bus cycle. If SYSB/$\overline{RESB}$ is high at the end of the T_S bus state, the arbiter will request or retain the multi-master system bus. SYSB/$\overline{RESB}$ is sampled at every falling edge of the CLK which starts at the end of the T_S bus state until the bus cycle is finished by the $\overline{READY}$ signal or SYSB/$\overline{RESB}$ becomes high (inactive).
$\overline{READY}$	I	**Ready:** Indicates the end of the bus cycle if $\overline{READY}$ is low (active). The processor does not require the $\overline{READY}$ signal to end the bus cycle.
$\overline{LOCK}$	I	**Lock:** If $\overline{LOCK}$ is active (low), the arbiter is prevented from releasing the multi-master system bus to any other arbiters having higher priority. $\overline{LOCK}$ is sampled at the end of every bus state.

Table 2. KS82C289 Signal Descriptions (Continued)

Symbol	Type	Description
$\overline{\text{ALWAYS}}$	I	**Always Release:** Must be programmed during the falling edge of the processor reset by setting this pin low. Arbiter will release the multi-master system bus after each bus transfer cycle. Arbiter will be in the Always Release mode until reprogrammed.
$\overline{\text{CBQLCK}}$	I	**Common Bus Request Lock:** Is programmed if this pin is set high during the falling edge of the processor reset. $\overline{\text{CBQLCK}}$ is active on and prevents the arbiter from releasing the multi-master system bus to any other arbiters.
$\overline{\text{INIT}}$	I	**Initialize:** If $\overline{\text{INIT}}$ is low (active), all the arbiters on the multi-master system bus are reset. Releases the multi-master system bus but, pending a bus request, it cannot be cleared. Hence, arbiters can regain the multi-master system bus immediately, if necessary. $\overline{\text{INIT}}$ is not synchronous to CLK. **Note:** $\overline{\text{LLOCK}}$ (Level Lock) is not affected by this signal.
RESET	I	**Reset:** If RESET is high (active), $\overline{\text{BREQ}}$, $\overline{\text{BUSY}}$, and $\overline{\text{AEN}}$ are cleared and become inactive. RESET will also stop any current bus cycle without waiting for it to end. The bus cycle terminated by RESET will not be completed when RESET becomes inactive.
$\overline{\text{BCLK}}$	I	**Bus Clock:** $\overline{\text{BCLK}}$ is the multi-master system bus clock. All of the multi-master bus interface signals are synchronized to $\overline{\text{BCLK}}$. $\overline{\text{BCLK}}$ may not be synchronous to CLK. The multi-master system bus interface state machine (see Figure 1) is asynchronous to the falling edge of $\overline{\text{BCLK}}$.
$\overline{\text{BREQ}}$	O	**Bus Request:** The arbiter keeps the $\overline{\text{BREQ}}$ low (active) until it releases the multi-master system bus. $\overline{\text{BREQ}}$ is essential in the rotating and parallel priority resolving technique.
$\overline{\text{BPRN}}$	I	**Bus Priority In:** When low (active), this arbiter has the highest priority. When high, another arbiter with higher priority is requesting the multi-master system bus.
$\overline{\text{CBRQ}}$	I/O	**Common Bus Request:** An open-drain input/output which requires an external pull-up resistor. As an input: Another arbiter is requesting the multi-master system bus. It is enabled by the $\overline{\text{CBRQ}}$. As an output: This arbiter is requesting the multi-master system bus. When $\overline{\text{BREQ}}$ (Bus Request) is issued, the $\overline{\text{CBRQ}}$ is pulled low. When the arbiter gains the multi-master system bus, the $\overline{\text{CBRQ}}$ is released.
$\overline{\text{BPRO}}$	O	**Bus Priority Out:** $\overline{\text{BPRO}}$ low (active) is used for the serial priority technique. $\overline{\text{BPRO}}$ is connected to the $\overline{\text{BPRN}}$ (Bus Priority In) of the immediately lower priority to decide the status of the priority for that arbiter.
$\overline{\text{LLOCK}}$	O	**Level Lock:** $\overline{\text{LLOCK}}$ cannot be cleared by the $\overline{\text{INIT}}$, but can be cleared by RESET. When buffered with a tri-state buffer enabled by the $\overline{\text{AEN}}$ (Address Enable), $\overline{\text{LLOCK}}$ can be used as a multi-master system bus lock. $\overline{\text{LLOCK}}$ is active low and it is decoded from the processor LOCK.

Table 2. KS82C289 Signal Descriptions (Continued)

Symbol	Type	Description
$\overline{AEN}$	O	**Address Enable:** Connected to the clock generator, bus controller, and the processor's address latches. When low (active), can be used as Hold ACK (Hold Acknowledge) to a bus master. When high, indicates to the bus master that the arbiter has released the system bus. $\overline{AEN}$ becomes active relative to $\overline{BCLK}$ (Bus Clock). $\overline{AEN}$ becomes inactive relative to $\overline{CLK}$ (System Clock).
$\overline{BUSY}$	I/O	**Busy:** An open-drain input/output which requires an external pull-up resistor. As an input: Low (active) indicates that the multi-master system bus is in use. As an output: When high, indicates that this arbiter has taken control of the multi-master system bus.
V_{SS}	—	**Ground.**
V_{CC}	—	+5 volts supply voltage.

OPERATIONAL DESCRIPTION

Arbitration Between Bus Masters

The KS82C289 Bus Arbiter is a priority controlling device which allows the multi-master system bus to be used for multi-processing. Both higher and lower priority bus masters are allowed to gain the system bus, depending on the release mode. Ordinarily, the higher priority master acquires the system bus immediately after any lower priority master finishes its present cycle. Therefore, at the end of each transfer cycle, the Arbiter can keep the system bus or release it depending on the bus arbitration inputs, arbiter strapping options, and the processor state.

Releasing the Multi-Master System Bus

The Bus Arbiter can retain or release control of the multi-master system bus following every transfer cycle. There are three modes in which the Arbiter can release the multi-master system bus.

These three modes cannot release the multi-master system bus if the cycles are LOCKed.

Mode 1

Always Release Mode

Figure 3. Always Release Mode

Releases the multi-master system bus at the end of each transfer cycle. Mode 1 must be programmed at the falling edge of the processor RESET.

Mode 2

Releases the multi-master system bus if either condition, below, is met:

a) a lower priority bus master demands the bus by pulling CBRQ low.

b) BPRN = 1, which indicates that the higher priority bus master is asking for the multi-master system bus.

Mode 3

Mode 3 is the same as Mode 2, only $\overline{CBRQ}$ has no effect.

Gaining Control of the Multi-Master System Bus

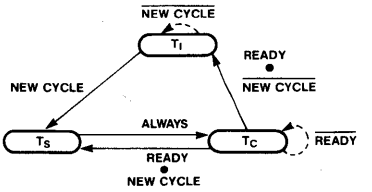
The $\overline{CBRQ}$ signal indicates whether or not another Arbiter wishes to gain control of the multi-master system bus. To perform this function, $\overline{CBRQ}$ must be connected to all other Arbiter $\overline{CBRQ}$ pins. Therefore, if any Bus Arbiter activates the $\overline{CBRQ}$ pin, it will pull down the $\overline{CBRQ}$ line to low.

Besides the $\overline{CBRQ}$ line, only the $\overline{BPRN}$ indicates if other, higher-priority, masters are requesting the bus.

A lower priority master can gain the bus in between the bus master's transfer cycles if the bus master has terminated its use of the bus. Then the bus must gain $\overline{BCLK}$ again at the beginning of the next transfer cycle.

This requires two $\overline{BCLK}$ periods if no other master demands the bus. This step of giving up and getting back the bus is wasteful and unnecessary. To bypass this problem $\overline{CBRQ}$ is useful. The Bus Arbiter does not need to release the bus if the $\overline{CBRQ}$ is not asserted. This alleviates the inefficient delay of getting back the multi-master system bus.

Figure 4. Bus States and the $\overline{READY}$ Signal



Bus States

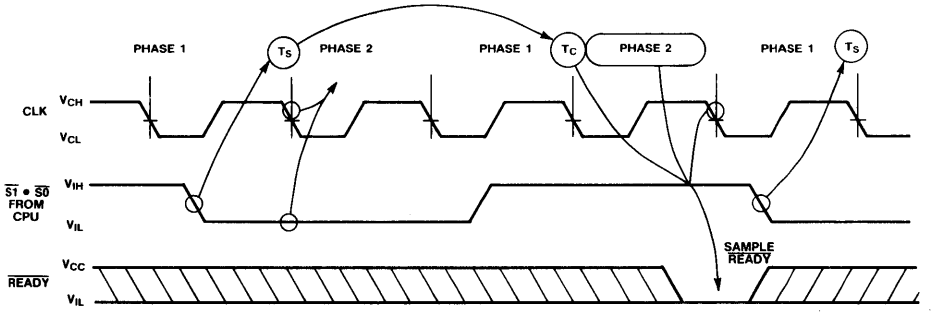
The Bus Arbiter has three processor bus states:

a) T_I (Idle)
b) T_S (Status)
c) T_C (Command)

Each bus cycle is two CLK cycles long.

Internal CPU processor clock phases correspond to the bus state phases.

Figure 5. 80286 Bus Cycle Definition (without wait states)



Bus Cycles

The $\overline{S1}$ and $\overline{S0}$ status inputs are sampled only at the falling edge of the CLK. $\overline{S1}$ and $\overline{S0}$ indicate the start of the bus cycle by going active (low).

The arbiter enters the T_S state if either the $\overline{S1}$ or $\overline{S0}$ is active (low) during the two CLK cycles.

The arbiter enters the T_C state after T_S is exited.

The shortest bus cycle is one T_S and one T_C. The longest bus cycle is one T_S followed by multiple T_C states. A repeated T_C bus state is referred to as a wait state.

The $\overline{READY}$ input determines whether the current T_C is to be repeated. It is sampled at the end of every T_C state if it is high. If it is high (1), then the T_C is repeated. When $\overline{READY}$ is sampled low, the current bus cycle is aborted.

If the $\overline{S1}$ and $\overline{S0}$ status lines are low at the next falling edge of the CLK, then the Bus Arbiter enters the T_S state immediately after the current bus cycle is aborted.

If none of the status lines are sampled active (low) at the next falling edge of the CLK, then the Bus Arbiter enters the T_I state. T_I is repeated until the status lines are sampled active (low).

Bus Masters

MULTIBUS protocols allow multiple processing elements to share access to common system resources. When a common system resource such as the system bus is "BUSY", local processors must wait for access.

The Bus Arbiter sets priorities and schedules access to the multi-master system bus. The bus arbiter supplies access to the system bus depending upon the release mode and the higher or lower priority of each bus master.

When the bus arbiter is used, higher priority bus masters access the system bus before lower priority bus masters or when the current lower priority bus master completes its transfer cycle. Lower priority bus masters access the system bus when there are no higher priority bus masters or when the proper surrender conditions exist.

The bus arbiter arranges scheduling and access transparently to the bus master.

The bus arbiter retains or releases the system bus at the end of each transfer cycle. The processor state, bus arbitration inputs, and arbiter strapping options are the factors used by the bus arbiter to determine release status. Refer to section "Release Modes" for more specific information.

Establishing Priority

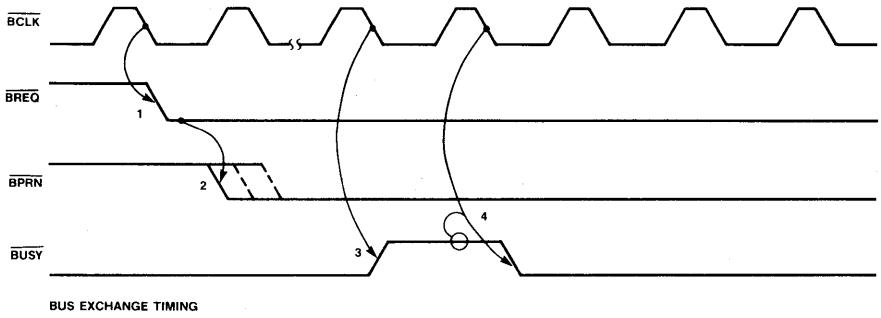
The Bus Arbiter establishes the priority level of the bus masters that are competing for access to a multi-master bus. To do this, the bus arbiter uses parallel, serial, and rotating techniques. Each of these techniques assumes that at any point in time, one bus master has priority over all other bus masters.

The highest priority arbiter is the arbiter with a $\overline{BPRN}$ input (low). The arbiter with the highest priority cannot access the system bus until the system bus is released from its current transaction.

When the system bus completes its current transaction, the present bus owner releases $\overline{BUSY}$. $\overline{BUSY}$ is an active-low 'Wired-OR' MULTIBUS signal which indicates that the system bus is inactive. This signal is sent to every bus arbiter in the system.

When the arbiter with the highest priority ($\overline{BPRN}$ low) receives the $\overline{BUSY}$ signal, it seizes the system bus by pulling $\overline{BUSY}$ (low). Figure 6 is a graphic representation of the Bus Exchange Timing.

Figure 6. Bus Exchange Timing for the MULTIBUS®



A multi-master bus request is initiated when two conditions occur. 1) a processor signals the status for memory read, memory write, I/O read, I/O write, or interrupt acknowledge. 2) an SYSB/$\overline{RESB}$ (high) at the end of T_S.

An interrupt acknowledge cycle does not always require the MULTIBUS each time the status input indicates. To determine when to request the MULTIBUS, the arbiter uses external logic, through the SYSB/$\overline{RESB}$ input.

When the arbiter samples SYSB/$\overline{RESB}$, and it is (high), the MULTIBUS is requested. When the arbiter samples SYSB/$\overline{RESB}$ and it is not (high), the arbiter continues to sample SYSB/$\overline{RESB}$ until either SYSB/$\overline{RESB}$ is (high) or the bus cycle is terminated. The arbiter does not request the MULTIBUS if the bus cycle is completed before SYSB/$\overline{RESB}$ returns (high). Figure 7 is an example of an SYSB/$\overline{RESB}$ sampled repeatedly.

The bus arbiter generates and uses only one $\overline{BREQ}$ from the time it requests the system bus through the entire time it has access to the system bus. The bus arbiter does not generate a separate $\overline{BREQ}$ for each bus cycle. All multi-master system bus requests using $\overline{BREQ}$ are synchronized to the system bus clock, $\overline{BCLK}$.

Parallel Priority Technique

In order to use the parallel technique for determining bus master priority, each bus arbiter on the multi-master system bus must have its own bus request line ($\overline{BREQ}$). Figure 8 is a representation of the parallel technique.

Each $\overline{BREQ}$ line is fed into a priority encoder. The encoder generates the binary address of the active $\overline{BREQ}$ line with the highest priority. Then a decoder uses the binary address to identify the $\overline{BPRN}$ line corresponding to the requesting bus arbiter with the highest priority. The $\overline{BPRO}$ output is not used with the parallel priority resolving technique.

When an arbiter receives the highest priority, $\overline{BPRN}$ (low) and the system bus is released, the arbiter's associated bus master is allowed onto the multi-master system.

The only limiting factor, for the number of bus masters that can be handled by the parallel technique, is the external circuitry. The external circuitry must be able to resolve the bus priorities within one $\overline{BCLK}$ period. Otherwise the parallel priority resolving technique can be used for any number of bus masters.

Serial Priority Technique

The serial priority technique does not require external circuitry. The arbiters are connected in a daisy chain fashion. The highest priority arbiter has its $\overline{BPRO}$ output connected to the $\overline{BPRN}$ input of the next lower priority arbiter. That next lower arbiter has its $\overline{BPRO}$ output connected to the $\overline{BPRN}$ input of the next lower priority arbiter after itself, etc. Figure 9 is a representation of serial technique connection.

This technique establishes a fixed position of priority. The highest priority bus arbiter has its $\overline{BPRN}$ tied (low), ensuring that it always receives highest priority when it requests the system bus. Figure 10 illustrates serial priority bus behavior.

A lower priority arbiter receives temporary higher priority status from the fixed higher priority arbiter. When the arbiter with the higher priority is not accessing or requesting the system bus, it asserts its $\overline{BPRO}$ signal (low). This asserts the $\overline{BPRN}$ signal of the fixed lower priority arbiter, allowing it to have the highest priority, temporarily.

When its $\overline{BPRO}$ goes inactive, a fixed higher priority arbiter retrieves its priority status from a fixed lower priority arbiter. The $\overline{BPRO}$ of an arbiter becomes inactive when it either requests access to the system bus or when its $\overline{BPRN}$ goes inactive because the $\overline{BPRO}$ from the next higher arbiter goes inactive. This allows for a trickle down effect from fixed higher priority arbiters down to the fixed lowest priority arbiter.

$\overline{BREQ}$ output is not used for the serial technique.

The number of bus arbiters connected in serial for priority resolution is limited by propagation delay between $\overline{BPRN}$ and $\overline{BPRO}$, 18ns, because priority must be established within one $\overline{BCLK}$ period. Therefore the maximum number of bus arbiters equals $\overline{BCLK}$ period divided by $\overline{BPRN}$ to $\overline{BPRO}$ delay.

$$\text{number of bus arbiters} = \frac{\overline{BCLK}\text{ period}}{\overline{BPRN}\text{ to }\overline{BPRO}\text{ delay}}$$

Figure 7. Bus Request Timing During an Interrupt Acknowledge Cycle

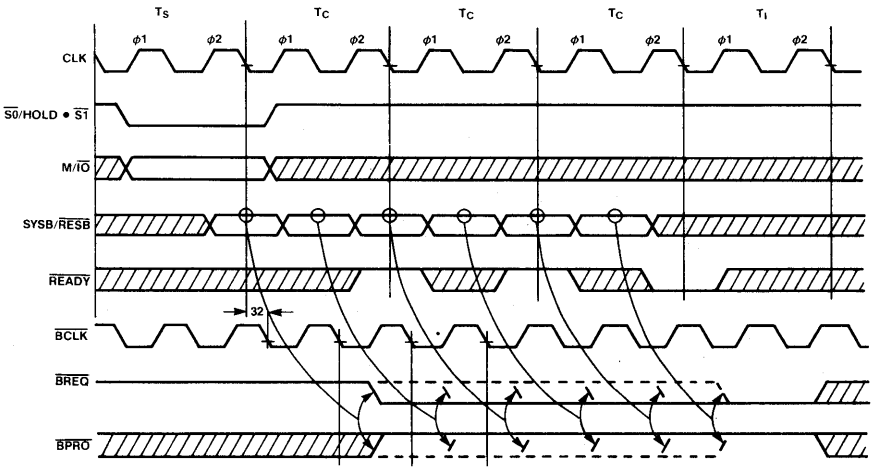


Figure 8. Parallel Priority Resolving Technique

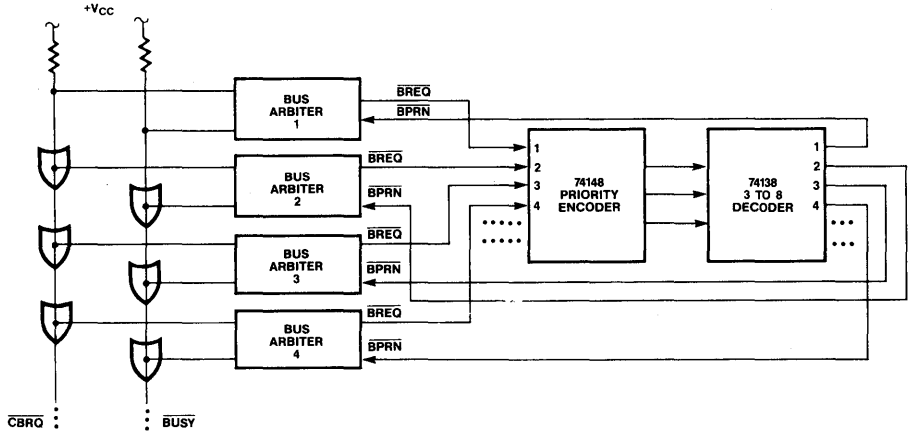


Figure 9. Connections for Serial Priority Resolving Technique

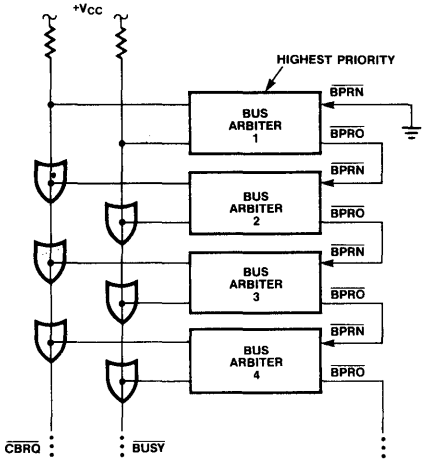
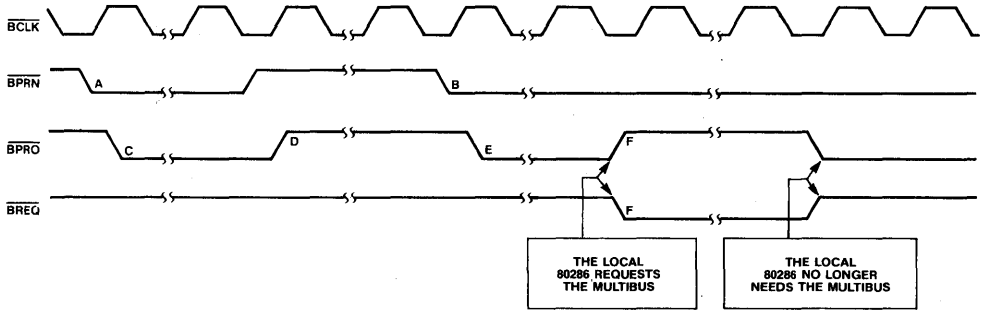


Figure 10. Serial Priority Bus Behavior



Note: Events A through F described above.

Rotating Priority Technique

The rotating priority technique requires external circuitry, similar to the parallel priority technique. The rotating technique assigns and re-assigns priority to the arbiters dynamically.

The priority encoder used in the rotating technique is a more complex circuit than the one used in the parallel technique. The circuit rotates priority between requesting arbiters. This provides each arbiter with an equal chance to use the multi-master system bus over a specified amount of time.

Choosing a Priority Technique

Each priority technique, parallel, serial, and rotating provides a trade-off between using complex external circuitry and allowing equal access to the system bus by each bus master.

The parallel priority technique does not require extensive external logic circuits, does allow for re-assignment of priority status for each bus master, and can accommodate a relatively large number of bus masters.

The serial priority technique does not require any external logic circuits but has fixed priority settings assigned to each bus master and can accommodate a limited number of bus masters.

The rotating priority technique does requires more complicated external logic circuits but does provide equal access between each of the bus masters and the system bus.

Releasing the MULTIBUS

The bus arbiter can either release or retain control of the system bus after the completion of a data transfer cycle on the MULTIBUS. Whether the bus arbiter releases control of the system bus depends upon the release mode selected and the priority settings in effect for the release mode selected.

There are three release modes. Table 3 describes the release modes and the mode settings which enable release of the system bus.

Table 3. Release Modes

Release Mode	Acceptable Release Conditions
Mode 1	The bus arbiter always releases the bus at the end of the transfer cycle.
Mode 2	The bus arbiter retains the system bus until: • a higher-priority bus master requests the system bus. This drives the BPRN (high) • a lower priority bus master requests the system by pulling CBRQ (low)
Mode 3	The bus arbiter retains the system bus until: • a higher priority bus master requests the system bus. This drives the BPRN (high) • CBRQ (low) is ignored **Note:** If the cycles are LOCKed, the bus arbiter does not release the system bus, even if the mode release conditions are met.

The arbiter will surrender the MULTIBUS after each complete transfer cycle if the "Always Release" mode 1 is programmed.

If the "Always Release" mode 1 is not programmed, the arbiter will not surrender the MULTIBUS until one of the following occur:

- the processor enters a halt state
- the arbiter is forced off because the $\overline{\text{BPRN}}$ becomes (high) and mode 2 or mode 3 is programmed into the arbiter
- the arbiter is forced off because a common bus request $\overline{\text{CBRQ}}$ input is enabled and mode 2 is programmed into the arbiter

$\overline{\text{CBRQ}}$ reduces bus exchanges. The present bus master retains the sytem bus as long as $\overline{\text{CBRQ}}$ is (high). $\overline{\text{CBRQ}}$ remains (high) until another master requests the system bus.

$\overline{\text{BPRN}}$ indicates if a bus master of higher priority is requesting the system bus. It does not indicate if a bus master of lower priority is requesting the system bus.

In order to allow lower priority bus masters access to the system bus, bus masters must release the system bus at the end of each transfer cycle and re-establish priority to access the system bus again and wait for a current transfer cycle opening. This release, re-establishing priority and re-accessing can take approximately two $\overline{\text{BCLK}}$ periods.

$\overline{\text{CBRQ}}$ eliminates unnecessary releasing of a bus master from the system bus. When a bus master requires the system bus it must assert $\overline{\text{CBRQ}}$ (low). If $\overline{\text{CBRQ}}$ remains (high), the current bus master does not have to release the system bus at the end of each transfer cycle.

$\overline{\text{LOCK}}$ overrides any of the release mode options. As long as $\overline{\text{LOCK}}$ is asserted, the arbiter will not release control of the MULTIBUS to any other requesting bus master.

$\overline{\text{INIT}}$ or RESET signals cause the arbiter to surrender the MULTIBUS. The release mode and arbiter input status are ignored.

The three bus release modes operate the same irregardless of the type of microprocessor used.

Choosing a Release Mode

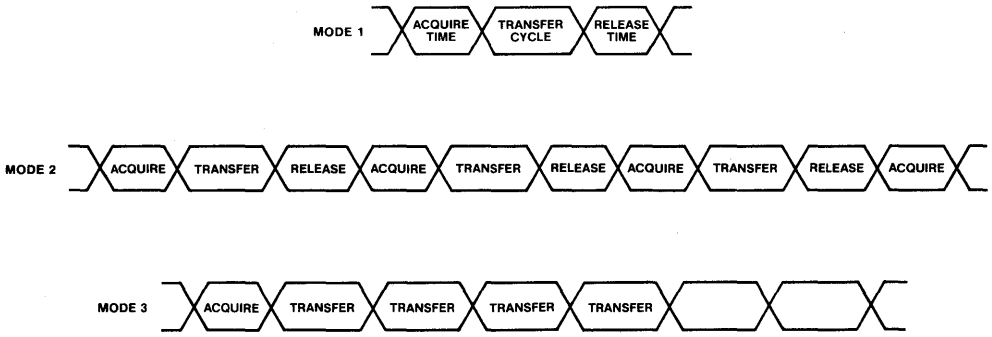
The release mode affects subsystem bus utilization and the system as a whole. The acquire and release times specified for each of the release modes impacts the system bus efficiency. Figure 11 illustrates the differences caused the release and acquisition times for each release mode.

Mode 1 requires a request and release phase for every transfer cycle. This allows lower priority bus masters to access the system bus, but it reduces the overall bus efficiency.

Modes 2 and 3 let the bus master retain the system bus for multiple transfer cycles. A bus master releases the system bus when it is forced off by another bus master's request.

Each release mode allows the designer to optimize the system use of the MULTIBUS.

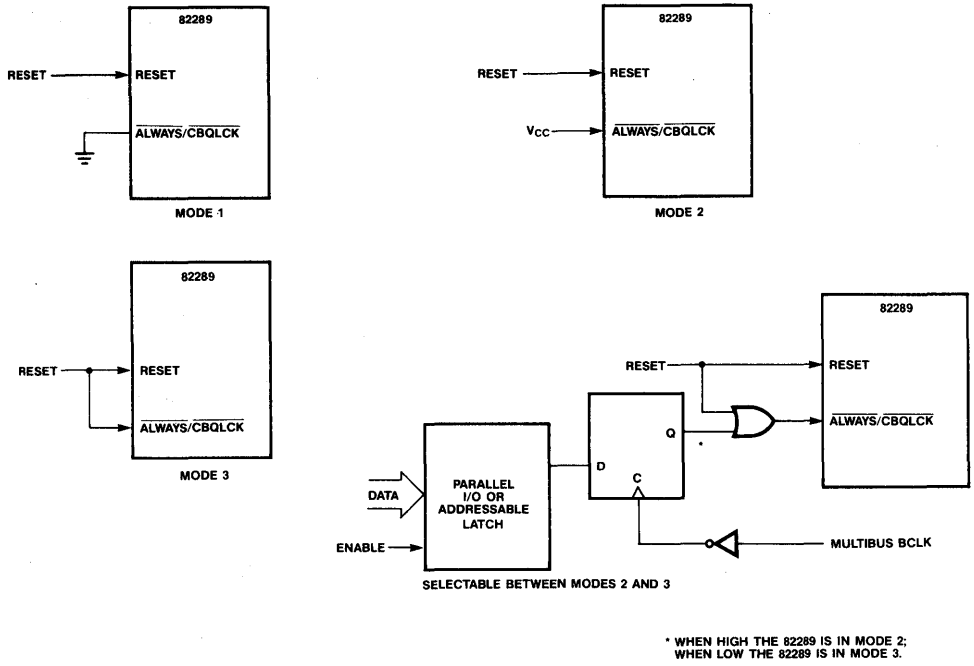
Figure 11. Effects of Bus Release Mode on Bus Efficiency



Configuring Release

The bus arbiter does not require any additional hardware to configure in any of the three release modes. In addition, the processor can be configured to switch between mode 2 and mode 3 by software control. This requires that a parallel port or addressable latch is used to drive the ALWAYS/CBQLCK input pin of the processor. Figure 12 illustrates the three release mode configurations.

Figure 12. 82289 Release Mode Configurations



LOCK and LLOCK

The three modes of releasing the multi-master system bus can be nulled by the LOCK input. But, LOCK will not surrender control of the multi-master system bus to any other Arbiter. The Bus Arbiter will surrender the multi-master system bus if RESET or INIT becomes active. RESET and INIT are independent of the states of the Arbiter inputs or the current release mode.

The LOCK signal can be asserted to the bus arbiter synchronous with the CLK and independent of the three release modes to prevent the release of the multi-master system bus to other bus masters regardless of their order of priority.

The LLOCK output signal can be asserted at all the bus cycles that are LOCKed. LLOCK is 1 if LOCK is 1, and 0 if LOCK is 0. Once LLOCK is active, it will wait until the end of the current transfer cycle before becoming inactive.

RESET and Initialization (INIT)

INIT (active low) is an asynchronous signal from the multi-master system bus. BREQ, BUSY, and AEN are cleared and become inactive when INIT is active (low). The Bus Arbiter will not clear any pending bus request from other bus masters while INIT is active. INIT can interrupt an active bus cycle, but, it will not prevent the Arbiter from requesting the multi-master system bus when it becomes inactive and completing the bus cycle.

RESET (active high) is synchronous to the CLK and can be synchronous to the processor. BREQ, BUSY, and AEN are cleared and become inactive when RESET is asserted. Also, RESET will clear the LLOCK signal and clear any pending bus request, unlike the INIT signal. RESET will stop any current bus cycle without waiting for the cycle to end. And, the bus cycle terminated by RESET will not be completed after the RESET becomes inactive.

DC ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Storage Temperature ..... -65°C to +150°C
Ambient Temperature Under Bias ..... 0°C to 70°C
Case Temperature ..... 0°C to 85°C

Note: Operation at absolute maximum ratings may cause permanent damage to the device.

Table 4. DC Electrical Characteristics

Symbol	Parameter	Condition	Min	Max	Units
V_{IL}	Input Low Voltage			0.8	V
V_{IH}	Input High Voltage		2.0		V
V_{ILC}	CLK Input Low Voltage			0.6	V
V_{IHC}	CLK Input High Voltage		3.0	V_{CC}	V
V_{OL}	Output Low Voltage: $\overline{BUSY}$, $\overline{CBRQ}$, $\overline{BPRO}$ $\overline{BPRO}$, $\overline{BREQ}$, AEN $\overline{LLOCK}$	 I_{OL} = 32 mA I_{OL} = 16 mA I_{OL} = 5 mA		 0.45 0.45 0.45	 V V V
V_{OH}	Output High Voltage	I_{OH} = 400 μA	2.4		V
I_{LI}	Input Leakage Current	$V_{SS} < V_{IN} < V_{CC}$		+1	μA
I_O	Output Leakage Current	$V_{OUT} = V_{SS}$ or V_{CC}		+10	μA
I_{CC1}	Quiescent Current	CLK, $V_{IN} - V_{CC}$ or V_{SS}		+10	μA
I_{CC2}	Supply Current			+80	mA
C_{CLK}	CLK, $\overline{BCLK}$ Input Capacitance	FC = 1 MHz		12	pF
C_{IN}	Input Capacitance	FC = 1 MHz		10	pF
C_O	Input/Output Capacitance	FC = 1 MHz		20	pF

AC SWITCHING CHARACTERISTICS

Table 5. KS82C289 AC Switching Characteristics

No.	Parameter	Test Conditions	8.0 MHz		10.0 MHz		12.5 MHz		Units
			Min	Max	Min	Max	Min	Max	
01	CLK Cycle Period		60	BCLK+50	50	BCLK+50	40	BCLK+50	ns
02	CLK Low Time	at 1.0V	15	230	15	230	10		ns
03	CLK High Time	at 3.6V	20	235	15	230	12		ns
04	CLK Rise/Fall Time	1 to 3.6V		10		10		9	ns
05	$\overline{BCLK}$ Cycle Time		100		100		100	∞	ns
06	$\overline{BCLK}$ High/Low Time		30		25		20		ns

Table 5. KS82C289 AC Switching Characteristics (Continued)

No.	Parameter	Test Conditions	8.0 MHz		10.0 MHz		12.5 MHz		Units
			Min	Max	Min	Max	Min	Max	
07	$\overline{S0}$/HOLD, $\overline{S1}$, M/$\overline{IO}$ Setup Time		22		15		13		ns
08	$\overline{S0}$/HOLD, $\overline{S1}$, M/$\overline{IO}$ Hold Time		1		1		1		ns
09	$\overline{READY}$ Setup Time		38		30		24		ns
10	$\overline{READY}$ Hold Time		25		20		16		ns
11	$\overline{LOCK}$, SYSB/$\overline{RESB}$ Setup Time		20		15		12		ns
12	$\overline{LOCK}$, SYSB/$\overline{RESB}$ Hold Time		1		1		1		ns
13	RESET Setup Time		20		15		12		ns
14	RESET Hold Time		1		1		1		ns
15	RESET Active Pulse Width		16		16		16		CLKs
16	$\overline{INIT}$ Setup Time	Note 2	45		45		45		ns
17	$\overline{INIT}$ Hold Time	Note 2	1		1		1		ns
18	$\overline{INIT}$ Active Pulse Width		$3(t_1)+(t_{14})$		$3(t_1)+(t_{14})$		$3(t_1)+(t_{14})$		ns
19	$\overline{BUSY}$, $\overline{BPRN}$, $\overline{CBRQ}$, CBQCLK/$\overline{ALWAYS}$ Hold Time to $\overline{BCLK}$ or (RESET)		20		18		15		ns
20	$\overline{BUSY}$, $\overline{BPRN}$, $\overline{CBRQ}$, CBQCLK/$\overline{ALWAYS}$ Hold Time to $\overline{BCLK}$ or (RESET)		1		1		1		ns
21	$\overline{BCLK}$ to $\overline{BREQ}$ Delay	C = 60 pF		30		30		25	ns
22	$\overline{BCLK}$ to $\overline{BPRO}$ Delay	C = 60 pF		35		35		28	ns
23	$\overline{BPRN}$ to $\overline{BPRO}$ Delay	C = 60 pF		25		25		20	ns
24	$\overline{BCLK}$ to $\overline{BUSY}$ Active Delay	C = 300 pF	1	60	1	60	1	50	ns
25	$\overline{BCLK}$ to $\overline{BUSY}$ Float Delay	Note 1		35		35		28	ns
26	$\overline{BCLK}$ to $\overline{CBRQ}$ Active Delay	C = 300 pF		55		55		45	ns
27	$\overline{BCLK}$ to $\overline{CBRQ}$ Float Delay	Note 1		35		35		28	ns
28	$\overline{BCLK}$ to $\overline{AEN}$ Active Delay	C = 150 pF	1	25		25	1	20	ns
29	CLK to $\overline{AEN}$ Inactive Delay	C = 150 pF	3	25		25	3	20	ns
30	CLK to $\overline{LLOCK}$ Delay	C = 50 pF		20		20		16	ns
31	RESET to $\overline{LLOCK}$ Delay	Note 2		35		35		28	ns
32	CLK to $\overline{BCLK}$ Setup Time	Note 3	38		38		35		ns

T_A = 0°C to 70°C
T_{CASE} = 0°C to 85°C
V_{CC} = 5V ± 5%

Notes: AC timing is referenced to 0.8V and 2.0V points.
1. When $I_O < I_{LO}$, float condition occurs.
2. CLK and $\overline{BCLK}$ are asynchronous to each other in actual use. But, this specification is required for component testing.
3. $\overline{INIT}$ is asynchronous to CLK and to $\overline{BCLK}$ during actual use. But, this specification is required for component testing.

Figure 13. AC Drive and Measurement Points CLK Input (BCLK Input)

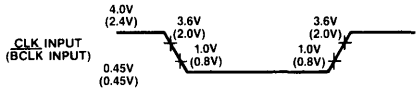


Figure 14. AC Setup, Hold and Delay Time Measurement

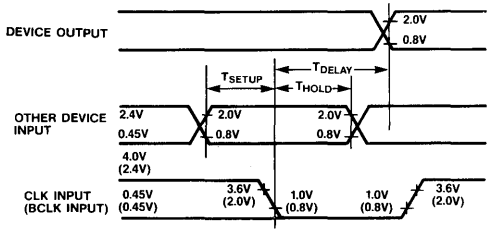
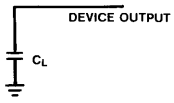


Figure 15. AC Test Loading on Outputs



WAVEFORMS

The following waveforms, Figures 16 through 24, contain examples of general cases of the timing relationships of the inputs and the outputs. These figures do not represent all the possible input and output transitions of all signals in all modes.

Refer to the identified special cases or a timing specification for the same or related function in another mode for examples of specific transitions.

The bus arbiter serves as an interface between the iAPX subsystem and MULTIBUS. The iAPX 286 subsystem operates synchronously to the CLK signal. The MULTIBUS operates synchronous to the BCLK signal.

CLK and BCLK operate asynchronously to each other and at different frequencies. The relative phase and frequency of CLK and BCLK at the time the input is sensed effects the exact clock period where a synchronous input to one clock will cause a synchronous response in the other clock.

The CLK period cannot be too long, relative to the BCLK period, t_1 greater than t_5 + 50ns, in order to maintain proper MULTIBUS arbitration. If the CLK period is too long relative to the BCLK period, another arbiter could gain control of the system bus before the current arbiter releases AEN synchronous to its CLK.

The AEN release is synchronous to the fall of the CLK edge after the processor cycle ends. The BREQ and BUSY releases are synchronous to the fall of the BCLK after the processor cycle ends.

However, all 286 speed selections are MULTIBUS compatible because any CLK frequency greater than 6.66 MHz, processor speeds greater than 3.33 MHz, avoids conflict with 10 MHz BCLKs.

Figure 16. MULTIBUS® Acquisition and Always-Release Operation

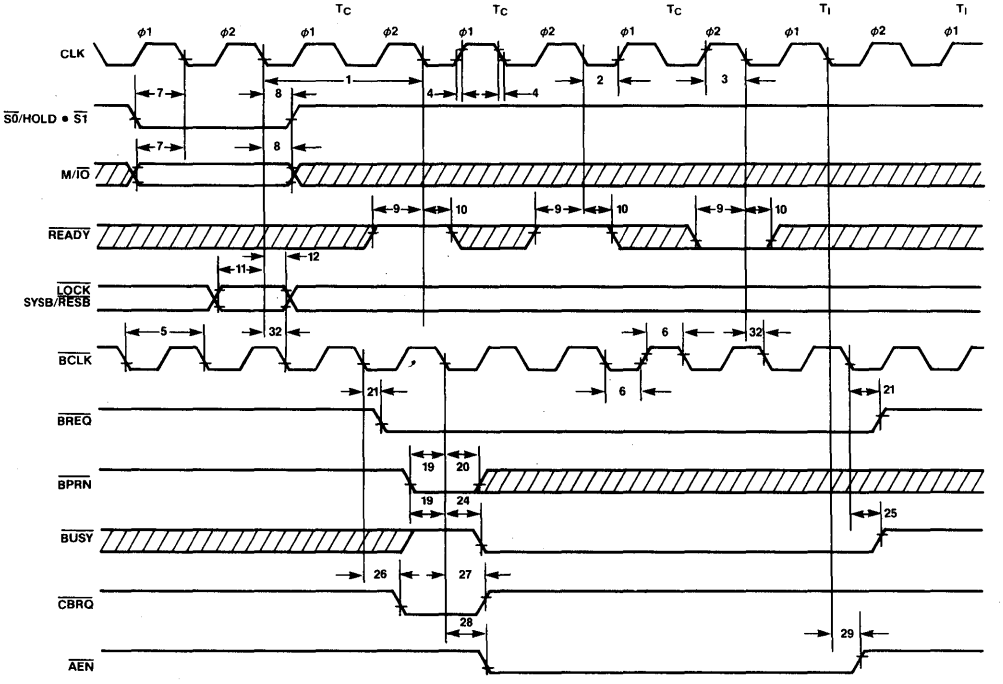


Figure 17. MULTIBUS® Release due to $\overline{\text{BPRN}}$ Inactive

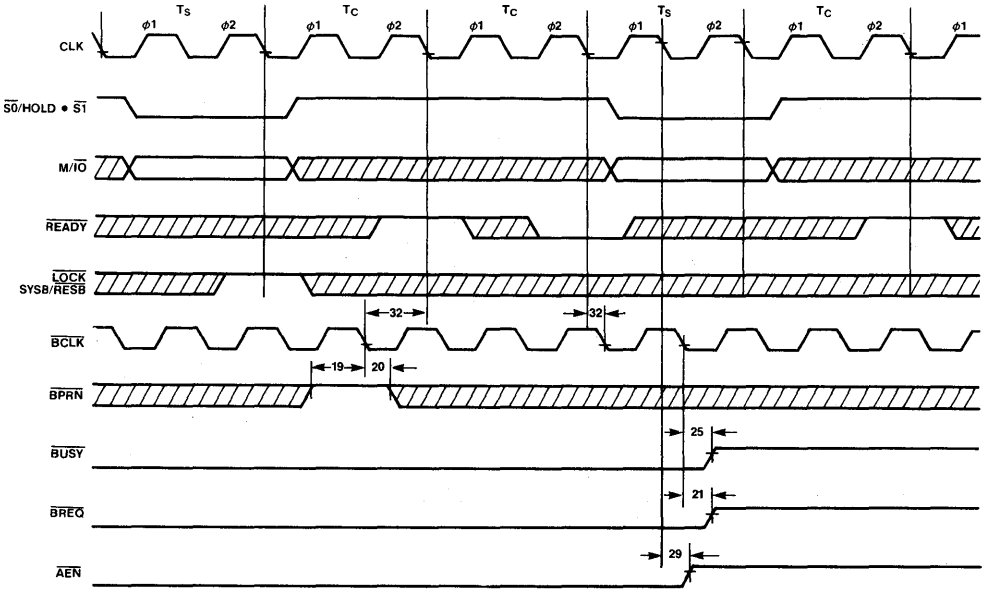


Figure 18. MULTIBUS® Release due to $\overline{CBRQ}$ Active

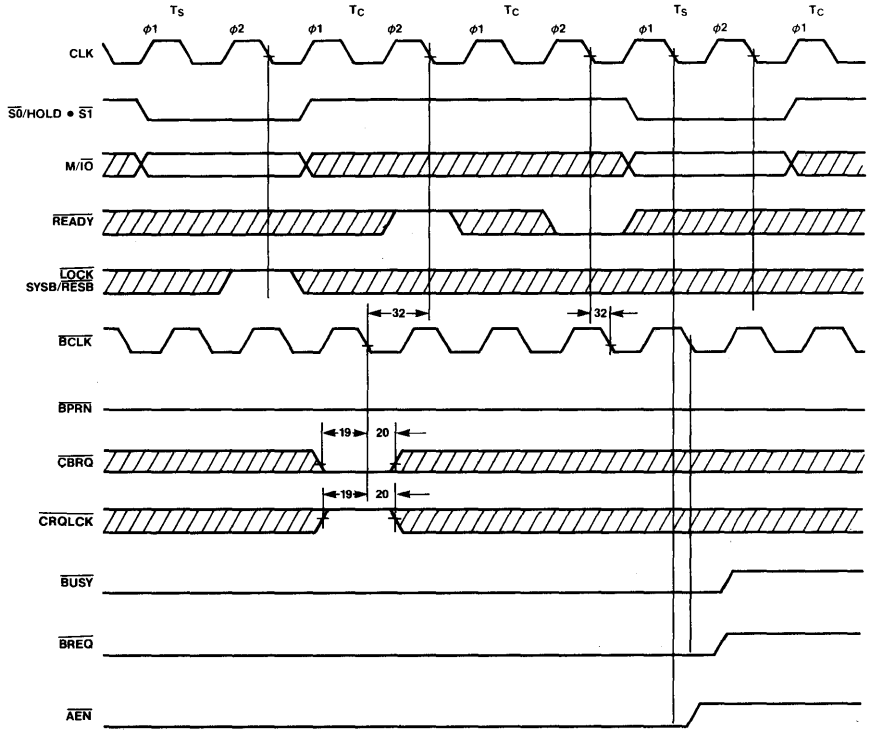


Figure 19. MULTIBUS® Acquisition During 80286 INTA Cycles

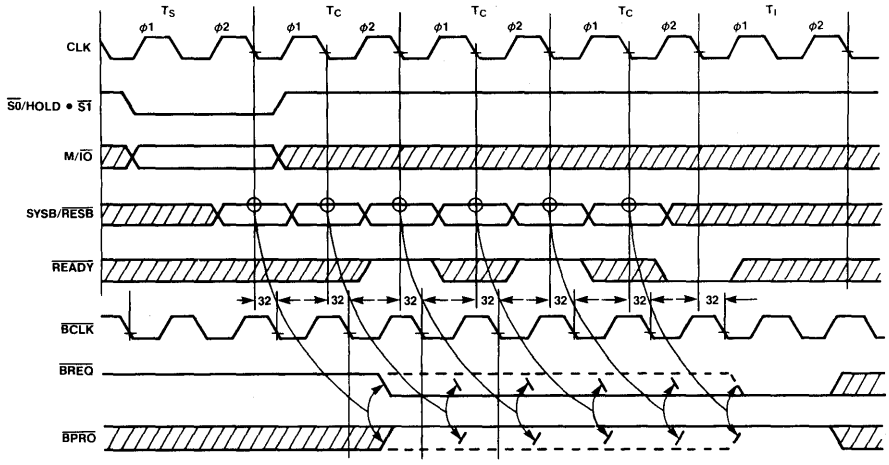


Figure 20. $\overline{BPRN}$ to $\overline{BPRO}$ Timing Relationship

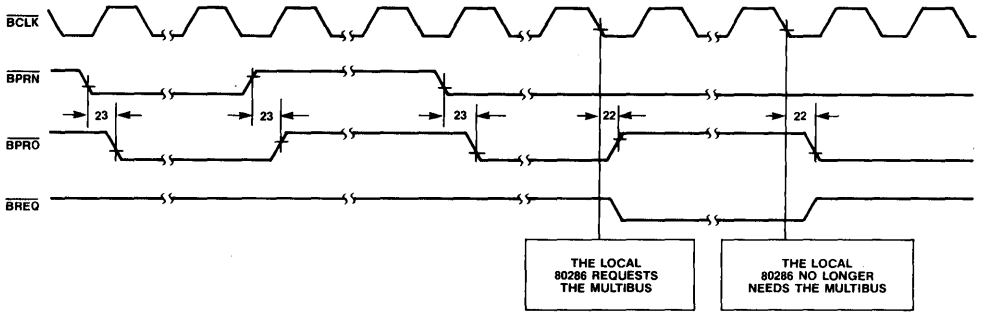


Figure 21. 80286 $\overline{LOCK}$ and 82289 $\overline{LLOCK}$ Relationship

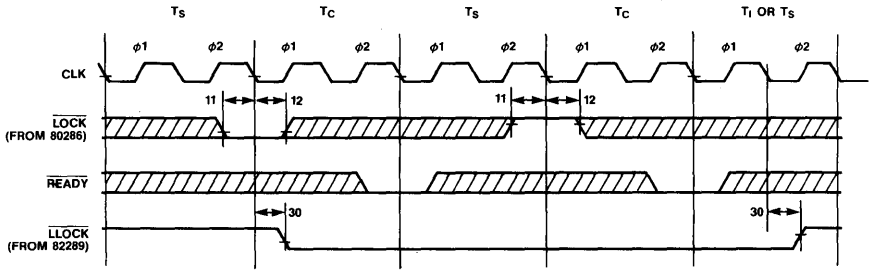


Figure 22. RESET Active Pulse

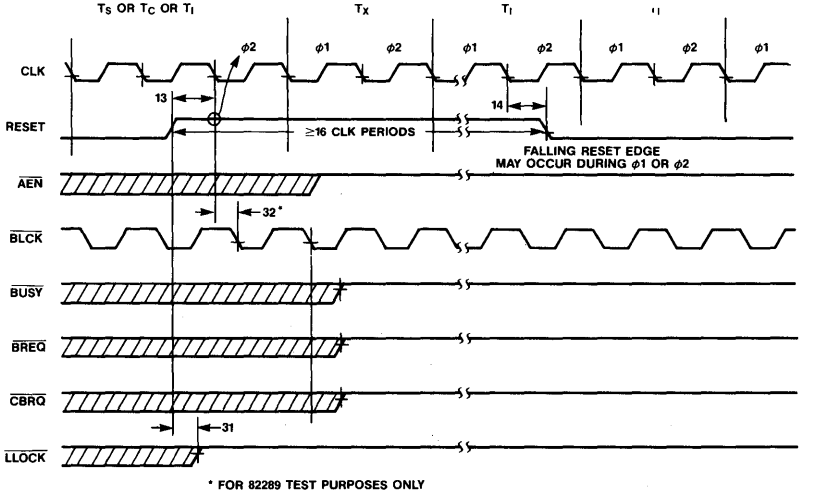


Figure 23. $\overline{INIT}$ Active Pulse

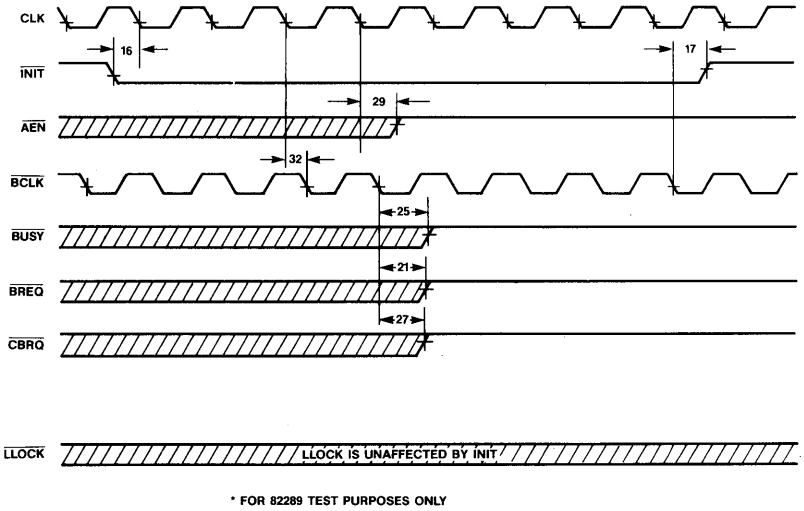
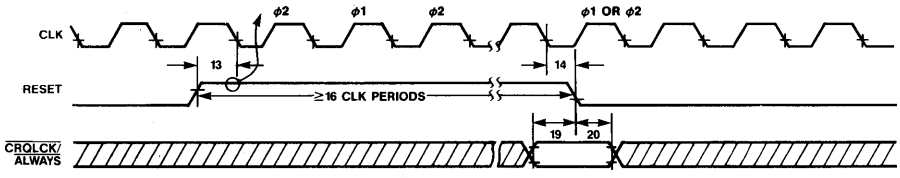


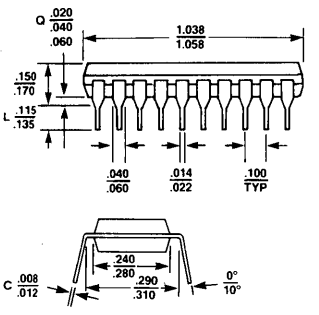
Figure 24. Programming the Always-Release/Common-Bus-Request-Release Option



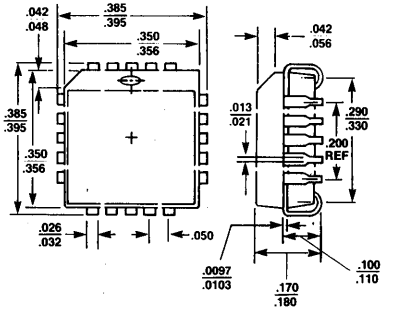
PACKAGE DIMENSIONS

Units: Inches

20-pin DIP



20-pin PLCC



ORDERING INFORMATION AND PRODUCT CODE

KS 82C289 X X X

SAMSUNG SEMICONDUCTOR

Part Number

Speed

-8.0	8.0MHz
-10.0	10.0MHz
-12.5	12.5MHz

Packaging

P — Plastic DIP

L — Plastic Leaded Chip Carrier (PLCC)

Temperature

C — Commercial (0°C to +70°C)

I — Industrial (-40°C to +85°C)

SAMSUNG products are designated by a Product Code. When ordering, please refer to products by their full code. For unusual, and/or specific packaging or processing requirements not covered by the standard product line, please contact the SAMSUNG MOS Product Group.

FEATURES

- **Fully IBM PC parallel port compatible**
- **Completely TTL compatible I/O**
- **Bidirectional I/O port**
- **H/W or S/W controllable I/O**
- **User controllable interrupt request**
- **Minimum components required**
- **On-chip 20 MHz oscillator**
- **High speed CMOS process**
- **40 Pin DIP**

GENERAL DESCRIPTION

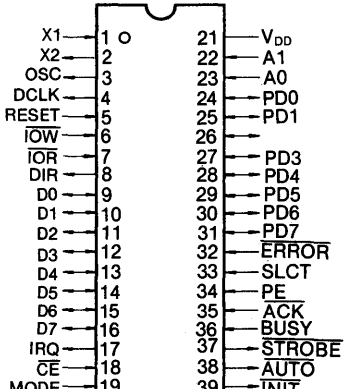
KS82C411 Parallel I/O Interface is a 40 pin DIP custom LSI which provides parallel port interface between IBM PC and printer with minimum external components. It can be used to communicate with an industry standard parallel printer such as IBM parallel printer or Centronics compatible one.

It contains all parts of IBM printer adapter without I/O device select logic, and performs the same function as that.

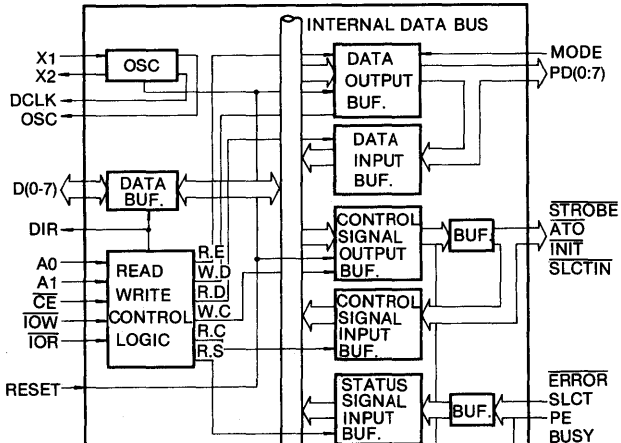
The outputs of KS82C411 fabricated by high speed CMOS process, are TTL compatible which can source 4mA and can sink 12mA each.

The KS82C411 also can be used to design monochrome display interface or RS-232C interface board with its on chip-oscillator. The on-chip oscillator and it's divided by 10 output can offer the baud rate clock of the RS-232C interface or the dot clock of the monochrome display interface.

PIN DIAGRAM



BLOCK DIAGRAM



PIN DESCRIPTION

I : Input O : output B : bidirection S : source

Pin No.	Symbol	Name	Type	Pin Function
1 2	X1 X2	Crystal in Crystal out	I O	X1, X2 are the pins to which a crystal (whose frequency is between 1.5 MHz and 20 MHz) is attached.
3	CLK	Clock out	O	Oscillator out.
4	DCLK	Divided CLK	O	Clock output whose frequency is one tenth that of CLK.
5	RESET	Reset in	I	Active high clears date and control registers.
6	$\overline{IOW}$	I/O write	I	Active low enables the CPU to write data or control words to the chip.
7	$\overline{IOR}$	I/O read	I	Active low enables the chip to send data, control words or pinter status to the CPU.
8	DIR	Direction	O	It is active high only when $\overline{CE}$ and $\overline{IOR}$ are activated. It indicates the direction of data transfer between CPU and KS82C411. When activated, the chip sends data, control words or printer status to the CPU.
9-16	D0-7	Data	I/O	The bidirectional 8-bit data bus is connected to the system data bus. The CPU transmits or receives data/control words through the data bus. The CPU also receives status from printer.
17	IRQ	Interrupt request	O	It is an interrupt request output pin, which is the inverted $\overline{ACK}$ signal only when it is internally enabled. It is enabled by writing D4 = 1 in the printr control register. When RESET is activated it is disabled remaining high impedance.
18	$\overline{CE}$	Chip enable	I	When $\overline{CE}$ = O, it enables the data transfers between CPU and the chip.
19	MODE	Mode select	I	MODE = 1: The chip is in read only mode the parallel I/O port. MODE = 0: If b5 of Control Word Register (CWR) is '1', CPU can read external data from parallel port. If b5 of CWR is '0', CPU can read back the parallel port which was last written to it.
20	V_{SS}	Ground		Ground pin
21	$\overline{SLCTIN}$	Select in	O	Active low allows data entry into the printer.
22	$\overline{INIT}$	Initiate	O	Active low clears the printer buffer.
23	AUTO	Auto feed	O	When it is low, the printer is feed automatically one line after printing.
24	$\overline{STROBE}$	Data strobe	O	Active low writes data into the printer.
25	BUSY	Busy state	I	A high indicates that the printer can not receive data during either case: • In data entry • In printer error status • Under printing • Under processing of paper feed • In off-line status
26	$\overline{ACK}$	Acknowledge	I	A low indicates that data bus has been received and that the printer is ready to accept other data. The CPU can read this status in D6 by the "Read Status" command.

PIN DESCRIPTION (Continued)

I : input O : output B : bidirection S : source

Pin No.	Symbol	Name	Type	Pin Function
27	PE	Paper end	I	It is a output pin from the printer. A high indicates that the printer is out of paper. The CPU can read this status in D5 by the "Read Status" command.
28	SLCT	Printer	I	It is always high unless the selected printer power is down. The CPU can read this status in D4 by the "Read Status" command.
29	$\overline{ERROR}$	Error status	I	It is a output pin from the printer. Active low indicates the printer is in either status. • Paper end status • Off-line status • Other abnormall motor operation The CPU can read this status in D3 by the "Read Status" command.
30-37	PD7-0	Printer data bus	I/O	Printer data port. This port is cleard by RESET. These output pins send out the dat to the printer by the CPU "Write Data" command. They are compatible with the TTL logic Level. The CPU con also "Read back" these data which the CPU last wrote by the "Read Data" command.
38-39	A0,A1	Address A0 Address A1	I	These two address lines are used to decode the five command registers with $\overline{IOR}$, $\overline{IOW}$, $\overline{CE}$.
40	V_{DD}	Power supply		+5 Volt power supply.

FUNCTION DESCRIPTION

The printer deiver responds to five I/O instructions: two outputs and three inputs. The output instructions transfer data into 2 latches, one is the dat latch, the other is the printer control signal latch. The two of three input instructions allow the processor to read or read-back the contents of the above two latches. The last one allows the processor to read the real time status of a printer.

A description of each instruction follows:

(1) Write data to the printer port.

During write operation, the data on the system data bus are latched in at the rising edge of $\overline{IOW}$, and is put on the printer data bus (PD0-PD7).

The write operation when the MODE pin is high, is discarded. The write operation when the MODE pin is low and internal RDEN is high (read external data mode), will reset the RDEN to the low level, and outputs the data through the PD(0-7) pins.

The printer data latch is cleared by RESET.

(2) Read data on the printer port.

The read operation can be determined to the MODE pin and b5 of control word register.

They are as follows:

Mode	b5 of CWR	Function
1	X	Read external data without the state of RDEN.
0	1	Read external data.
0	0	Read back the printer port written (The same function as IBM Printer Adapter)

FUNCTION DESCRIPTION (Continued)

(3) Write control word to the printer.

This instruction causes the latch to capture the six least significant bits of the data bus. These control signals are shown below.

Data bus	b7	b6	b5	b4	b3	b2	b1	b0
Control signal	—	—	RDEN	IRQEN	SLCTIN*	$\overline{INIT}$	AUTO*	STROBE*

Note: b3, b1, b0 data are inverted at the output pins $\overline{SLCTIN}$, $\overline{AUTO}$, $\overline{STROBE}$ respectively.

If b4 (IRQEN) = 1, KS82C411 will interrupt the PROCESSOR ON THE CONDITION THAT ACK pin transits high to low.

If b5 (RDEN) = 1, printer data pins are disabled. And CPU can read external data through Printer data pins.

If b5 = 0, Printer data pins are enabled. CPU can read back the exact values that was previously written to the printer port.

(4) Read control word from printer.

During read operation of the processor, the latched printer control signals is sent back to CPU data bus. They are as follows:

Data bus	b7	b6	b5	b4	b3	b2	b1	b0
Control signal	1	1	RDEN	IRQEN	SLCTIN*	$\overline{INIT}$	AUTO*	STROBE*

Note: The unused pins (b7, b6) are fixed to "1" on system data bus.

The states of $\overline{SLCTIN}$, $\overline{AUTO}$, $\overline{STROBE}$ pins are inverted on system data bus.

(5) Read status from the printer

During read operation of the processor, the real time printer status signals on the pin 25-29 are transfered to the Processor.

Data bus	b7	b6	b5	b4	b3	b2	b1	b0
Status word	$\overline{BUSY}$*	$\overline{ACK}$	PE	SLCT	$\overline{ERROR}$	1	1	1

Note: The BUSY state is inverted on system data bus.

The unused bits (b2, b1, b0) are fixed to "1" on system data bus.

(6) Reset operation

When $\overline{RESET} = 1$,

$\overline{STROBE} = 1$, $\overline{AUTO} = 1$, $\overline{INT} = 0$, $\overline{SLCTIN} = 1$, IRQEN = 0, AND RDEN = 0.

$\overline{CE}$	A1	A0	$\overline{IOR}$	$\overline{IOW}$	Selected command
1	X	X	X	X	Not selected
0	0	0	0	1	Read data
0	0	0	1	0	Write data
0	0	1	0	1	Read status
0	0	1	1	0	Invalid
0	1	0	0	1	Read control
0	1	0	1	0	Write control
0	1	1	0	1	Invalid
0	1	1	1	0	Invalid

ELECTERICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Characteristics	Symbol	Ratings	Unit
Supply voltage range	V_{DD}	−0.5 to +7.0	V
Operating temperature	T_{OP}	−40 to +85	Deg
Storage temperature	T_{STG}	−65 to −150	Deg

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect reliability.

D.C. CHARACTERISTICS (Temp = 25 Deg, V_{DD} = 5V Unless otherwise specified.)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power supply	V_{DD}		4.5	5.0	5.5	V
Input high voltage 1	VIH1	V_{DD} = 5V +/− 5% (PIN 1)	4.0	—	—	V
Input low voltage 1	VIL1	V_{DD} = 5V +/− 5% (PIN 1)	—	—	1.0	V
Input high voltage 2	VIH2	V_{DD} = 5V +/− 5% (Other inputs)	2.0	—	—	V
Input low voltage 2	VIL2	V_{DD} = 5V +/− 5% (Other inputs)	—	—	0.8	V
Output high voltage	VOH	IOH = −4mA (PIN 3,4,8) (D0-7, PD0-7)	3.5	—	—	V
Output low voltage	VOL	IOL − 5mA (PIN 2,3,4,8) IOL = 8mA (PIN 21-24) IOL = 12mA (D0-7, PD0-7)	—	—	0.45	V
Input current	IIN	VIN = 0V-V_{DD} MAX (Except Pin 1)	−1.5	—	1.5	μA
Output floating leackage current	IFL	VIN = 0V-V_{DD} MAX (IRQ, D0-7)	−10	—	10	μA
Static supply current	IDD	V_{DD} = max, No load (CE = X1 = V_{DD})	—	10	20	μA
Dynamic current	IDD	V_{DD} = 5V 20MHz osc	—	20	25	mA

Note: Pin 21-24 are the open drains with internal pull-up resisters of 2.7 KΩ

A.C. CHARACTERISTICS

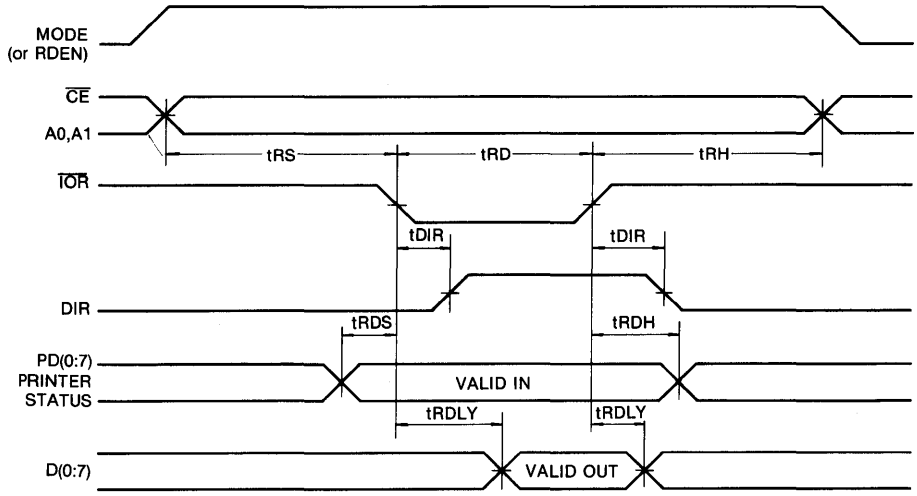
Parameter	Symbol	Max.	Min.	Unit
Chip select setting time	tWS	—	0	ns
Chip select holding time	tWH	—	20	ns
Write pluse width	tWR	—	200	ns
Data setting time on D0-7	tWDS	—	70	ns
Data hold time on D0-7	tWDH	—	30	ns
Data delay from IOW to PD0-7	tWDLY	70	—	ns
Chip select setting time	tRS	—	0	ns
Chip select holding time	tRH	—	20	ns
Read pluse width	tRD	—	200	ns
Delay time from IOR to DIR	tDIR	20	—	ns

ELECTERICAL CHARACTERISTICS (Continued)

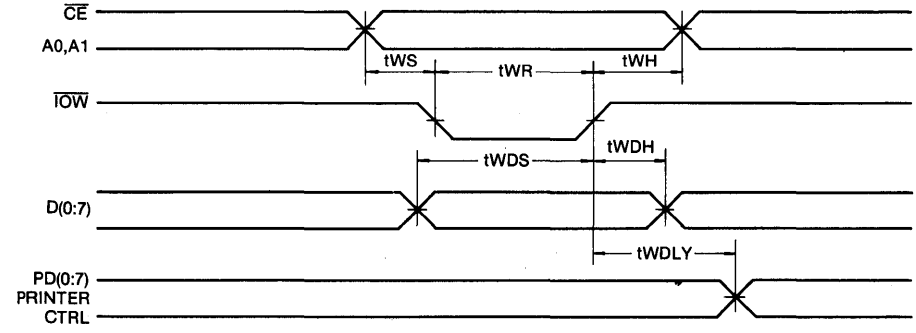
Parameter	Symbol	Max.	Min.	Unit
Data setting time on PD0-7	tRDS	—	0	ns
Data holding time on PD0-7	tRDH	—	0	ns
Data delay from IOR to D0-7	tRDLY	70	—	ns
Delay time from ACK to IRQ	tID	40	—	ns
Reset pulse width	tRST	—	50	ns
Output signal setting time after RESET	tRSC	50	—	ns
DCLK delay time after CLK	tDCLK	20	—	ns
Output disable time	tIDIS	50	—	ns
Output enable time	tIEN	50	—	ns

TIMING DIAGRAMS

READ OPERATION

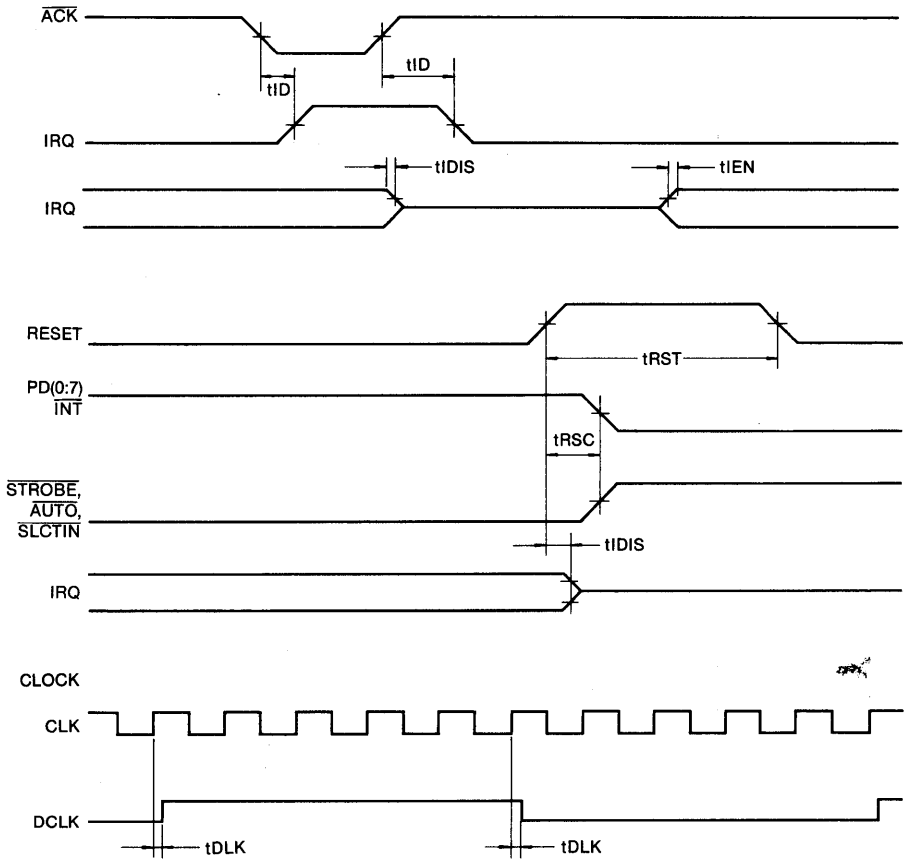


WRITE OPERATION

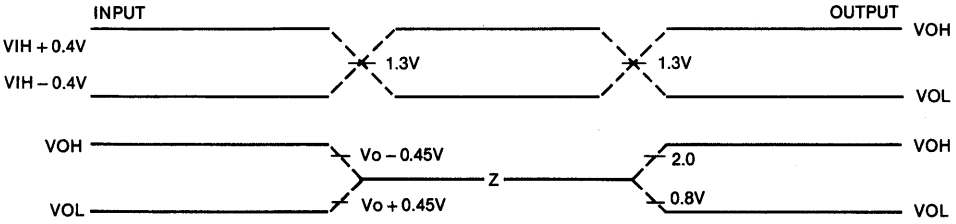


TIMING DIAGRAMS (Continued)

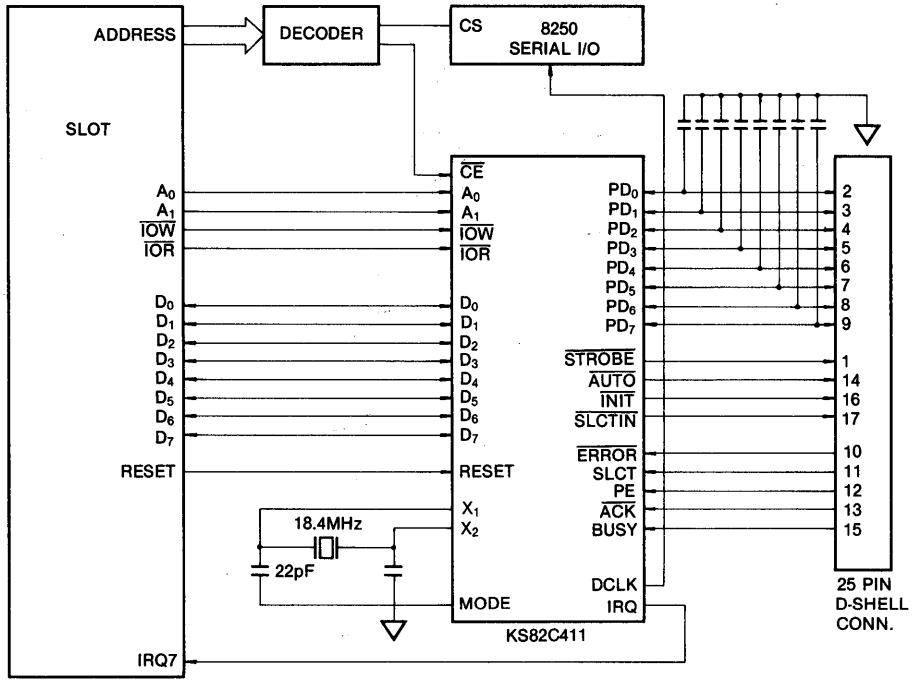
INTERRUPT AND RESET



AC TESTING INPUT/OUTPUT WAVEFORMS



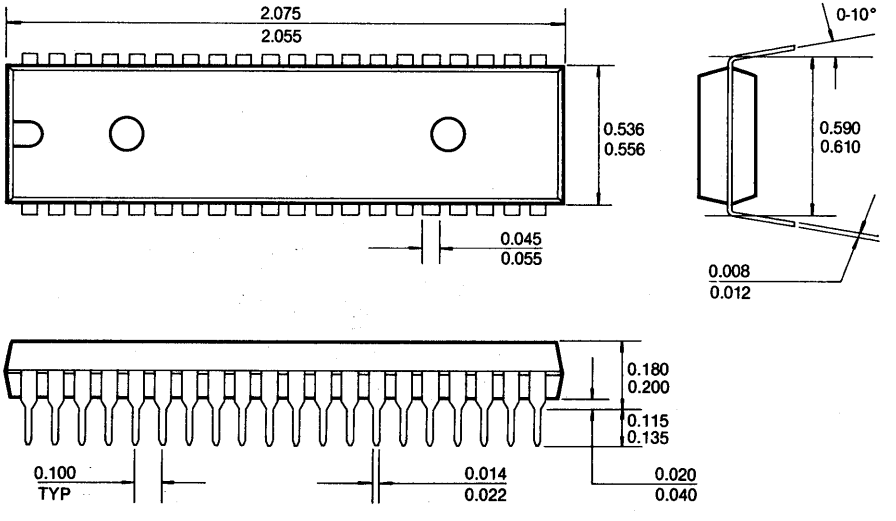
TYPICAL APPLICATION



PACKAGE DIMENSIONS

40 PIN PLASTIC DUAL IN LINE PACKAGE

Units: Inches



FEATURES

- **IBM PC/AT-compatible**
- **Dual-channel version of KS82C450 (campatible VL 16C450)**
- **Centronix printer interface**
- **Programmable serial interface characteristics for each channel**
- **Independent control on each channel**
- **Individual modem control signals for each channel**
- **Three-state TTL drive on each channel**

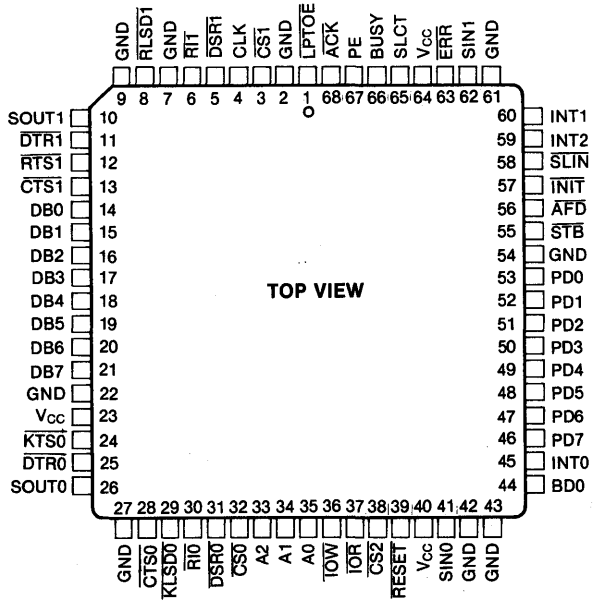
GENERAL DESCRIPTION

The KS82C452 is a parallel and dual asynchronous communications element (ACE). The device serves two UARTs simultaneously in microcomputer or microprocessor based systems. Each UART performs serial-to-parallel conversion on data characters received from peripheral devices or modems, and parallel-to-serial conversion on data characters transmitted by the CPU. The complete status of each UART of the dual ACE can be read at any time during functional operation by the CPU.

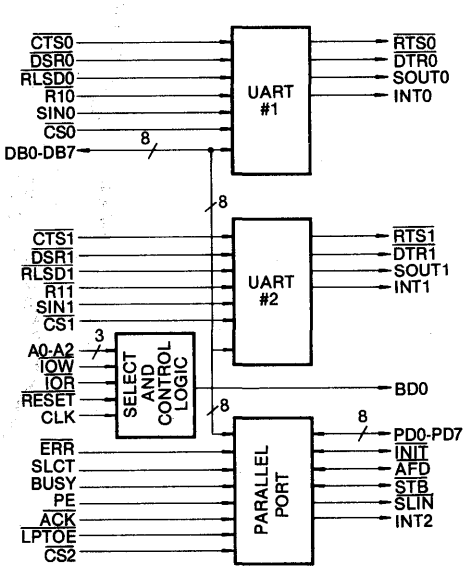
The information obtained includes the type and condition of the transfer operations being performed, and error conditions. Also, the KS82C452 provides the user with a fully birdirectional parallel data port that fully supports the parallel Centronics type printer.

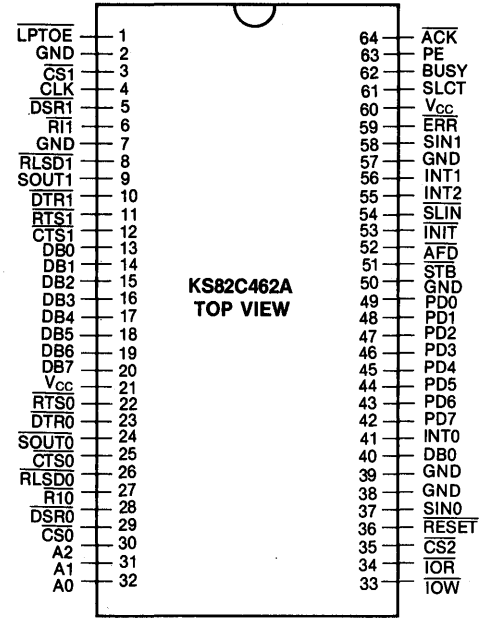
This device provides IBM PC/AT compatible computers with a simple device to serve the three system ports. The KS82C452 is, implemented using advanced CMOS technology and packaged in 68-pin PLCC 64 SDIP package.

PIN DIAGRAM



BLOCK DIAGRAM





* SAMSUNG KS82C462 is a 64 SDIP type of KS82C452.

Table KS82C452A Pin Allocations.

Pin No.	Pin Name	Pin No.	Pin Name
1	$\overline{LPTOE}$	18	DB4
2	GND	19	DB5
3	$\overline{CS1}$	20	DB6
4	CLK	21	DB7
5	$\overline{DSR1}$	22	GND
6	$\overline{RI1}$	23	UDD
7	GND	24	$\overline{RTS0}$
8	$\overline{RLSD1}$	25	$\overline{DTR0}$
9	GND	26	SOUT0
10	SOUT1	27	GND
11	$\overline{DTR1}$	28	$\overline{CTS0}$
12	$\overline{RTS1}$	29	$\overline{RLSD0}$
13	$\overline{CTS1}$	30	$\overline{RI0}$
14	DB0	31	$\overline{DSR0}$
15	DB1	32	$\overline{CS0}$
16	DB2	33	A2
17	DB3	34	A1

Pin No.	Pin Name	Pin No.	Pin Name
35	A0	52	PD1
36	$\overline{IOW}$	53	PD0
37	$\overline{IOR}$	54	GND
38	$\overline{CS2}$	55	$\overline{STB}$
39	$\overline{RESET}$	56	$\overline{AFD}$
40	V_{DD}	57	$\overline{INIT}$
41	SIN0	58	$\overline{SLIN}$
42	GND	59	INT2
43	GND	60	INT1
44	BD0	61	GND
45	INT0	62	SIN1
46	PD7	63	$\overline{ERR}$
47	PD6	64	V_{DD}
48	PD5	65	SLCT
49	PD4	66	BUSY
50	PD3	67	PE
51	PD2	68	$\overline{ACK}$

Table KS82C462A Pin Allocations.

Pin No.	Pin Name	Pin No.	Pin Name
1	$\overline{LPTOE}$	18	DB5
2	GND	19	DB6
3	$\overline{CS1}$	20	DB7
4	CLK	21	V_{DD}
5	$\overline{DSR1}$	22	$\overline{RTS0}$
6	$\overline{RI1}$	23	$\overline{DTR0}$
7	GND	24	$\overline{SOUT0}$
8	$\overline{RLSD1}$	25	$\overline{CTS0}$
9	SOUT1	26	$\overline{RLSD0}$
10	$\overline{DTR1}$	27	$\overline{RI0}$
11	$\overline{RTS1}$	28	$\overline{DSR0}$
12	$\overline{CTS1}$	29	$\overline{CS0}$
13	DB0	30	A2
14	DB1	31	A1
15	DB2	32	A0
16	DB3	33	$\overline{IOW}$
17	DB4	34	$\overline{IOK}$

Pin No.	Pin Name	Pin No.	Pin Name
35	$\overline{CS2}$	52	$\overline{AFD}$
36	$\overline{RESET}$	53	$\overline{INIT}$
37	SIN0	54	$\overline{SLIN}$
38	GND	55	INT2
39	GND	56	INT1
40	DB0	57	GND
41	INT0	58	SIN1
42	PD7	59	$\overline{ERR}$
43	PD6	60	V_{DD}
44	PD5	61	SLCT
45	PD4	62	BUSY
46	PD3	63	PE
47	PD2	64	$\overline{ACK}$
48	PD1	65	
49	PD0	66	
50	GND	67	
51	$\overline{STB}$	68	

PIN DESCRIPTIONS

I : input O : output B : bidirection S : source

Type	Pin Name	Pin Function
I	$\overline{LPTOE}$	Parallel Data Output Enable — When low, this signal enables the Write Data Register to the PD_0-PD_7 lines. A high puts the $\overline{PD_0}$-$\overline{PD_7}$ lines in the high-impedance state allowing them to be used as inputs. $\overline{LPTOE}$ is usually tied low for line printer operation.
S	GND	Ground (0V) — All pins must be tied to ground for proper operation.
I	$\overline{CS1}$ $\overline{CS0}$ CS2	Chip Selects — Each Chip Select Input acts as an enable for the write and read signals for the serial channels 0 ($\overline{CS0}$) and 1 ($\overline{CS1}$), $\overline{CS2}$ enables the signals to the printer port.
I	CLK	Clock Input — The external clock input to the baud rate divisor of each UART.
I	$\overline{DSR1}$ $\overline{DSR0}$	Data Set Ready Inputs — The logical state of the DSR pins is reflected in MSR(5) of its associated Modem Status Register, DDSR [MSR(1)] indicates whether the associated DSR pin has changed state since the previous reading of the MSR. When a DSR pin is low, its modem is indicating that it is ready to exchange data with the associated UART.
I	$\overline{RI1}$ $\overline{R10}$	Ring Indicator Inputs — When low RI indicates that a telephone ringing signal has been received by the modem or data set. The $\overline{RI}$ signal is a modem control input whose condition is tested by reading MSR(6) (RI) of each UART. The Modem Status Register output TERI [MSR(2)] indicates whether the RI input has changed from high to low since the previous reading of the MSR. If the interrupt is enabled [IER(3) = 1] and RI changes from a high to low, an interrupt is generated.

PIN DESCRIPTIONS (Continued)

I : input O : output B : bidirection S : source

Type	Pin Name	Pin Function
O	$\overline{RLSD1}$ $\overline{RLSD0}$	Receive Line Signal Detect — When low, the $\overline{RLSD}$ output indicates that the data carrier has been detected by the modem or data set. $\overline{RLSD}$ is a modem input whose condition can be tested by the CPU by reading MSR(7) (RLSD) of the Modem Status Registers. MSR(3) (DRLSD) of the Modem Status Register indicates whether the $\overline{RLSD}$ input has changed since the previous reading of the MSR. $\overline{RLSD}$ has no effect on the receiver. If the $\overline{RLSD}$ changes state with the modem status interrupt enabled, an interrupt occurs.
O	SOUT1 SOUT0	Serial Data Outputs — These lines are the serial data outputs from the UART's transmitter circuitry. A mark (1) is a logic "one" (high) and space (0) is a logic "zero" (low). Each SOUT is held in the mark condition when the transmitter is disabled. Reset is true, the Transmiter Register is empty, or when in the Loop Mode.
O	$\overline{DTR1}$ $\overline{DTR0}$	Data Terminal Ready Lines — Each $\overline{DTR}$ pin can be set (low) by writing a logic 1 to MCR (0), Modem Control Register bit 0 of its associated UART. This signal is cleared (high) by writing a logic 0 to the $\overline{DTR}$ bit [MCR(0)] or whenever a reset occurs. When active (low), the DTR pin indicates to the DCE that its UART is ready to receive data.
O	$\overline{RTS1}$ $\overline{RTS0}$	Request to Send Outputs — The $\overline{RTS}$ signal is an output on each UART used to enable the modem. An $\overline{RTS}$ pin is set low by writing a logic 1 to MCR(1) bit 1 of its UART's Modem Control Register. Both $\overline{RTS}$ pins are reset high by Reset. A low on the $\overline{RTS}$ pin indicates to the DCE that its UART has data ready to transmit. In half duplex operations. $\overline{RTS}$ is used to control the direction of the line.
I	$\overline{CTS1}$ $\overline{CTS0}$	Clear to Send Inputs — The logical state of each $\overline{CTS}$ pin is reflected in the $\overline{CTS}$ bit of the (MSR) Modem Status Register [$\overline{CTS}$ is bit 4 of the MSR, written MSR (4)] of each UART. A change of state in either $\overline{CTS}$ pin since the previous reading of the associated MSR causes the setting of DCTS [MSR(0)] of each Modem Status Register. When a $\overline{CTS}$ pin is low, the modem is indicating that data on the associated SOUT can be transmitted.
I/O	DB0-DB7	Data Bits DB0-DB7 — The Data Bus provides eight three-state I/O lines for the transfer of data, control and status information between the KS82C452 and the CPU. These lines are normally in a high-impedance state except during read operation. D0 is the least significant bit (LSB) and is the first serial data bit to be received or transmitted.
S	VCC	Power Supply — The power supply requirement is $5V \pm 5\%$.
I	A2 A1 A0	Address Lines A0-A2 — The address lines select the internal registers during CPU bus operations.
I	$\overline{IOW}$	Input/Output Write Strobe — This is an active low input which causes data from the data bus (DB_0-DB_7 to be input to either UART or to the parallel port. The data input depends upon the register selected by the address inputs A0, A1, A2. The chip select inputs ($\overline{CS0}$, $\overline{CS1}$, and $\overline{CS2}$) enable UART #1, UART #2, and the parallel port (respectively).
I	$\overline{IOR}$	Input/Output Read Strobe — This is an ative low input which cause the selected channel to output data to the data bus DB_0-DB_7). The data output depends upon the register selected by the address inputs. A0, A1, A2. Chip Select 0 ($\overline{CS0}$) selects UART #1, Chip Select 1 ($\overline{CS1}$) selects UART #2, and Chip Select 2 ($\overline{CS2}$) selects the line printer port.

PIN DESCRIPTIONS (Continued)

I : input O : output B : bidirection S : source

Type	Pin Name	Pin Function
I	$\overline{\text{RESET}}$	$\overline{\text{Reset}}$ — When low, the reset input forces the KS82C452 into an idle mode in which all serial data activities are suspended. The Modem Control Register (MCR) along with its associated outputs are cleared. The Line Status Register (LSR) is cleared except for the THRE and TEMT bits, which are set. All functions of the device remain in an idle state until programmed to resume serial data activities.
I	SIN0 SIN1	Serial Data Inputs — The serial data inputs move information from the communication line or modem to the KS82C452 receiver circuits. A mark (1) is high, and a space (0) is low. Data on serial data inputs is disabled when operating in the loop mode.
O	BDO	Bus Buffer Output — This active high output is asserted when either serial channel or the parallel port is read. This output can be used to control the system bus driver device (74LS245).
O	INT0 INT1	Serial Channel Interrupts — Each three-state, serial channel interupt output (enabled by bit 3 of the MCR) goes active (high) when one of the following interrupts has an active (high) condition and is enabled by the Interrupt Enable Register of its associated channel: Receiver Error flag, Reeceived Data Available, Transmitter Holding Register Empty, and Modem Status. The interrupt is reset low upon appropriate service or a reset operation.
I/O	PD7-PD0	Parallel Data Bits (0-7) — These eight lines provide a byte-wide input or output port to the system. The eight lines are held in a high-impedance state when $\overline{\text{LPTOE}}$ is held in the high state.
I/O	$\overline{\text{STB}}$	Line Printer Strobe — This open-drain line provides communication between the KS82C452 and the line printer. When it is active low, it provides the line printer with a signal to latch the data currently on the parallel port.
I/O	$\overline{\text{AFD}}$	Line Printer Autofeed — This open-drain line provides the line printer with an active low signal when continuous form paper is to be autofed to the printer.
I/O	$\overline{\text{INIT}}$	Line Printer Initialize — This open-drain line provides the line printer with a signal that allows the line printer initialization routine to be started.
I/O	$\overline{\text{SLIN}}$	Line Printer Select — This open-drain line selects the printer when it is active low.
O	INT2	Printer Port Interrupt — This signal is an ative high, three-state output, generated by the positive transition of $\overline{\text{ACK}}$. It is enabled by bit 4 of the Write Control Register.
I	$\overline{\text{ERROR}}$	Line Printer Error — This is an input line from the line printer. The line printer reports an error by holding this line low during the error condition.
I	SLCT	Line Printer Selected — This is an input line from the line printer that goes high when the line printer has been selected.
I	BUSY	Line Printer Busy — This is an input line from the line printer that goes high when the line printer is not ready to accept data.
I	PE	Line Printer Paper Empty — This is an input line from the line printer that goes high when the printer runs out of paper.
I	$\overline{\text{ACK}}$	Line Printer Acknowledge — This input goes low to indicate a successful data transfer has taken place. It generates a printer port interrupt during its positive transition.

ABSOLUTE MAXIMUM RATINGS

Item	Range	Conditions
Ambient Operating Temperature	−10°C to + 70°C	Stresses above those listed may cause permanent damage to the device. These are stress ratings only, functional operation of this device at these or any other conditions above those indicated in this data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
Storage Temperature	−65°C to + 150°C	
Supply Voltage to Ground Potential	−0.5V to V_{CC} + 0.3	
Applied Output Voltage	−0.5V to V_{CC} + 0.3V	
Applied Input Voltage	−0.5V to + 7.0V	
Power Dissipation	550mW	

DC CHARACTERISTICS: (TA = 0 to + 70°C, V_{CC} = 5V ± 5%)

Symbol	Parameter	Min.	Max.	Units	Conditions
VILX	Clock Input Low Voltage	−0.5	0.8	V	
VIHX	Clock Input High Voltage	2.0	V_{CC}	V	
VIL	Input Low Voltage	−0.5	0.8	V	
VIH	Input High Voltage	2.0	V_{CC}	V	
VOL	Output Low Voltage		0.4	V	IOL = 4.0 mA on DB0-DB7 IOL = 12 mA on PD0-PD7 IOL = 10 mA on $\overline{INIT}$, $\overline{AFD}$, $\overline{STB}$, and $\overline{SLIN}$ (see note 1) IOL = 2.0 mA on all other outputs
VOH	Output High Voltage	2.4		V	IOH = −0.4 mA on DB0-DB7 IOH = −2.0 mA on PD0-PD7 IOH = −0.2 mA on $\overline{INIT}$, $\overline{AFD}$, $\overline{STB}$, and $\overline{SLIN}$ IOH = −0.2 mA on all other outputs
ICC	Power Supply Current		50	mA	V_{CC} = 5.25 V, No loads on SIN0, 1; $\overline{DSR0}$, 1; $\overline{RLSD0}$, 1; $\overline{CTS0}$, 1, $\overline{R10}$, $\overline{R11}$ = 2.0V. Other inputs = 0.8V, Baud rate generator = 4 MHz. Baud rate = 56K
IIL	Input Leakage		± 10	μA	V_{CC} = 5.25 V, GND = 0V All other pins floating
ICL	Clock Leakage		± 10	μA	V_{IN} = 0 V, 2.25V
IOZ	3-State Leakage		± 20	μA	V_{CC} = 5.25 V, BND = 0V V_{OUT} = 0 V, 5.25V 1) Chip deselected 2) Chip and write mode selected
VIL(RES)	Reset Schmitt VIL		0.8	V	
VIH(RES)	Reset Schmitt V_{IH}	2.0		V	

Note 1. $\overline{INIT}$, $\overline{AFD}$, $\overline{STB}$, and $\overline{SLIN}$ are open collector output pins that each have an internal pull-up resistor (2.5 kΩ-3.5 kΩ) to V_{CC}. This will generate a maximum of 2.0 mA of internal IOL. In addition to this internal current, each pin will sink at least 10 mA, while maintaining the VOL specification of 0.4 V Max.

AC CHARACTERISTICS $T_A = 0°C$ to $+ 70°C$, $V_{CC} = 5V \pm 5\%$ (Notes 1,5)

Symbol	Parameter	Min.	Max.	Units	Conditions
tDIW	IOR Strobe Width	125		ns	
RC	Read Cycle	360		ns	
tDDD	Delay from $\overline{IOR}$ to Data		125	ns	100 pF Load
tHZ	$\overline{IOR}$ Floating Data Delay	0	100	ns	100 pF Load, Note 4
tDOW	$\overline{IOW}$ Strobe Width	100		ns	
WC	Write Cycle	360		ns	
tDS	Data Setup Time	40		ns	
tDH	Data Hold Time	40		ns	
tRA	Address Hold Time from $\overline{IOR}$	20		ns	Note 2
tRCS	Chip Select Hold Time from $\overline{IOR}$	20		ns	Note 2
tAR	$\overline{IOR}$ Delay from Address	60		ns	Note 2
tCSR	$\overline{IOR}$ Delay from Chip Select	50		ns	Note 2
tWA	Address Hold Time from $\overline{IOW}$	20		ns	Note 2
tWCS	Chip Select Hold Time from $\overline{IOW}$	20		ns	Note 2
tAW	$\overline{IOW}$ Delay from Address	60		ns	Note 2
tCSW	$\overline{IOW}$ Delay from Select	50		ns	Note 2
tRW	Rest Pulse Width	5		μs	
tXH	Duraton of Clock High Pulse	140		ns	External Clock
tXL	Duration of Clock Low Pulse	140		ns	External Clock
Transmitter					
tHR1	Delay from Rising Edge of $\overline{IOW}$ (WR THR) To Reset Interrput		175	ns	100 pF Load
tIRS	Delay from Initial INTR Reset to Transmit Start		16	CLK	Note 3
tSI	Delay from Initial Write to Interrupt	8	24	CLK	Note 3
tSTI	Delay from Stop to Interrupt (THRE)		8	CLK	Note 3
tIR	Delay from $\overline{IOR}$ (RD IIR) to Reset Interrupt (THRE)		250	ns	100 pF Load
Modem Control					
tMDO	Delay from $\overline{IOW}$ (WR MCR) to Output		250	ns	100 pF Load
tSIM	Delay to Set Interrupt from MODEM Input		250	ns	100 pF Load
tRIM	Delay to Reset Interrupt from-$\overline{IOR}$ (RS MSR)		250	ns	38 pF Load
Receiver					
tSINT	Delay from Stop to Set Interput		1	CLK	Note 3
tRINT	Delay from $\overline{IOR}$ (RD RBR/RDLSR) to Reset Interrupt		1	μs	100 pF Load

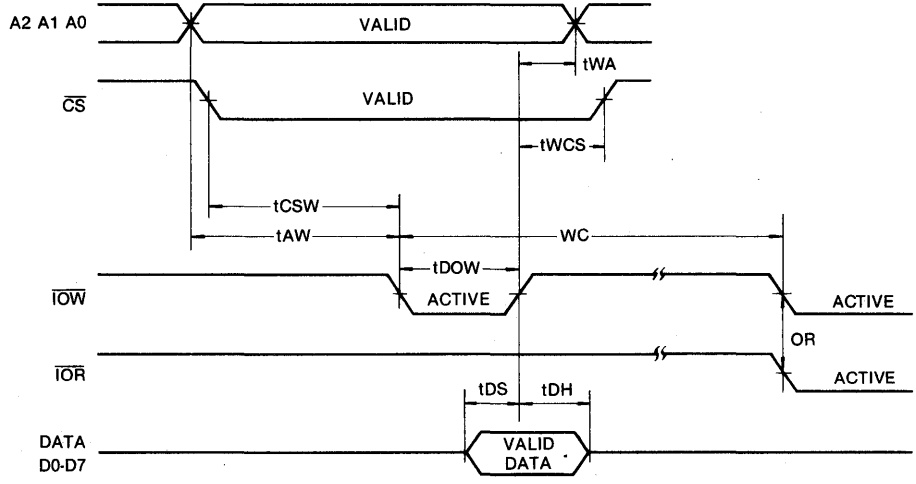
AC CHARACTERISTICS (Continued)

Symbol	Parameter	Min.	Max.	Units	Conditions
Parallel Port					
tDT	Date Time	1		μs	
tSB	Strobe Time	1	500	μs	
tAD	Acknowledge Delay (Busy Start to Acknowledge)			μs	Defined by Printer
tAKD	Acknowledge Delay (Busy End to Acknowledge)			μs	Defined by Printer
tAK	Acknowledge Duration Time			μs	Defined by Printer
tBSY	Busy Duration Time			μs	Defined by Printer
tBSD	Busy Delay Time			μs	Defined by Printer

Notes: 1. All timing specifications apply to pins on both serial channels (e.g. RI refers to both RI0 and RI1).
2. The internal address strobe is always active. 3. RCLK = tXH and tXL.
4. Charge and discharge time is determined by VOL, VOH and the external loading.
5. All timings are referenced to valid 0 and valid 1. (see AC TEST POINTS).
6. RCLK is internally derived from the internal-BAUDOUT signal.

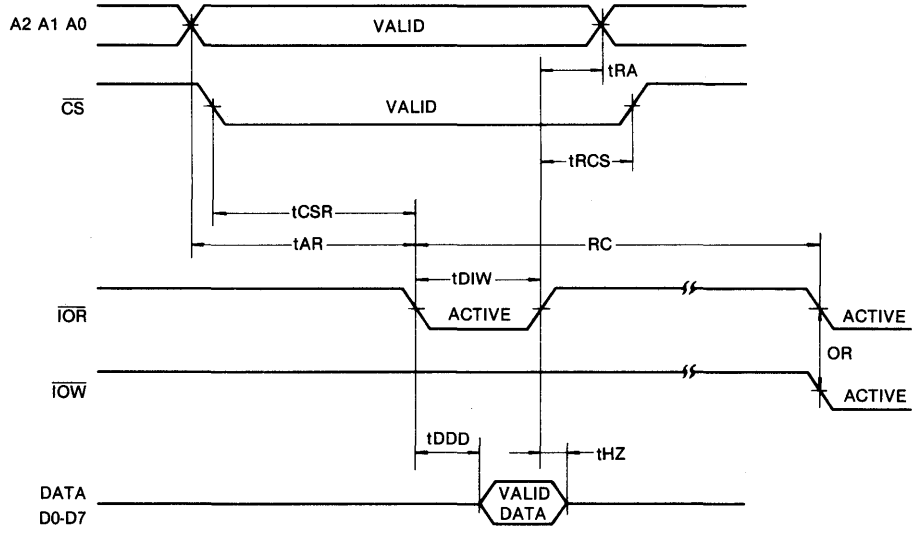
TIMING DIAGRAM

WRITE CYCLE TIMING

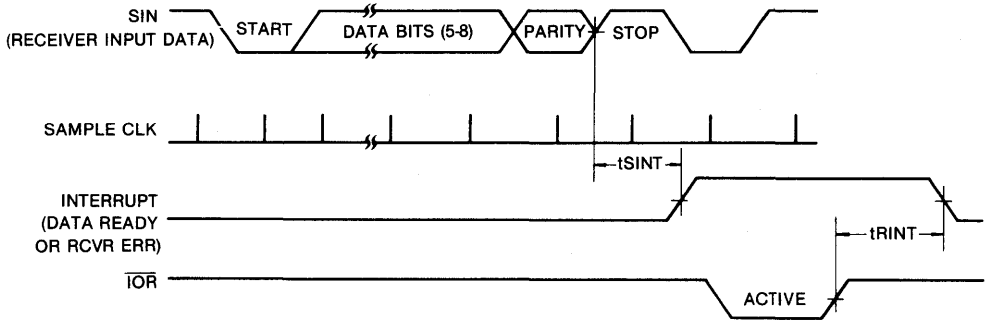


TIMING DIAGRAM (Continued)

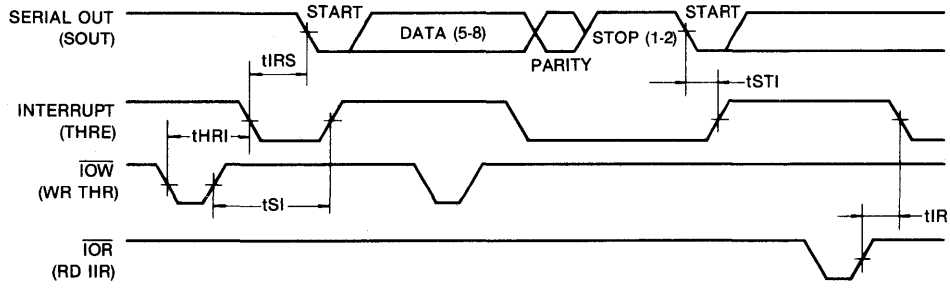
READ CYCLE TIMING



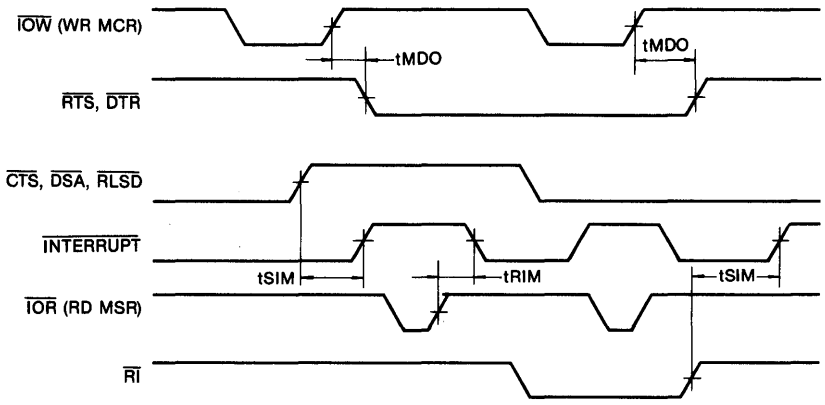
RECEIVER TIMING



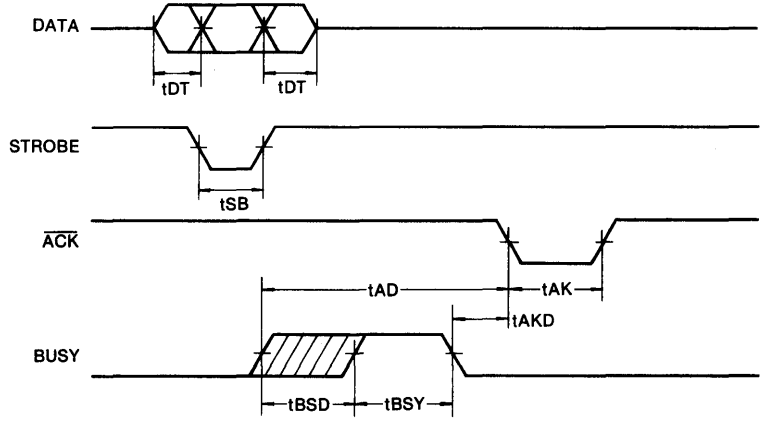
TRANSMITTER TIMING



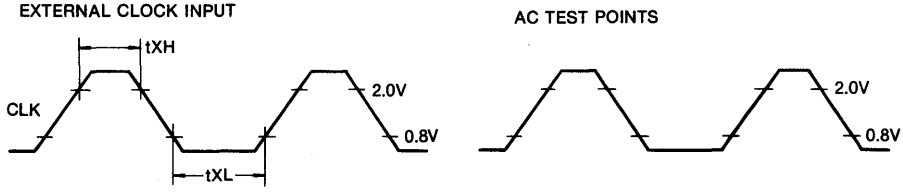
MODEM TIMING



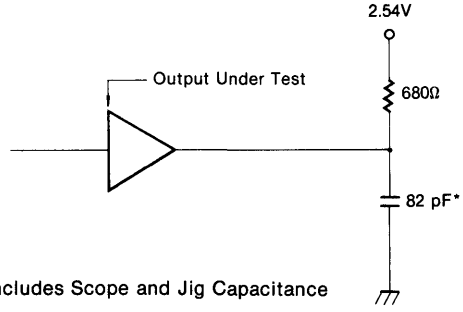
PARALLEL PORT TIMING



AC TESTING INPUT/OUTPUT WAVEFORMS



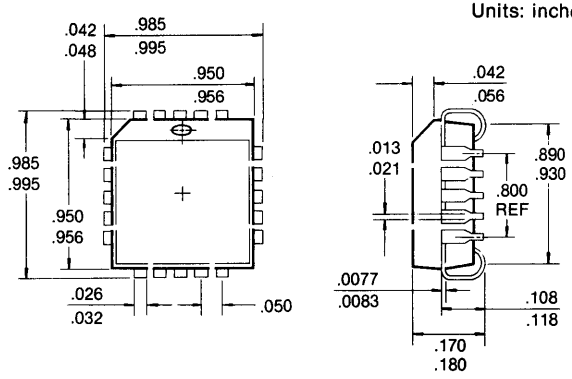
TEST CIRCUT



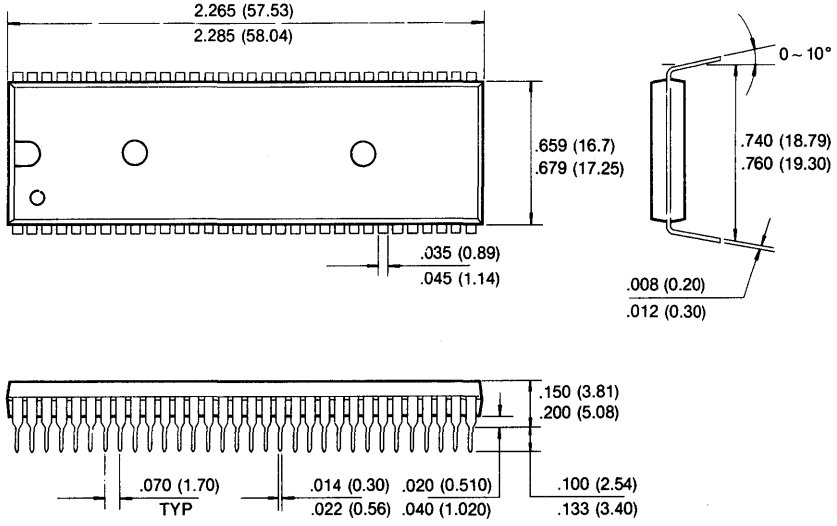
PACKAGE DIMENSIONS

68-PIN PLCC PACKAGE

Units: inches (millimeters)



64-PIN DUAL IN LINE PACKAGE SHRINK TYPE



FEATURES

- **Direct drive for 256K, 1Mbit and 4Mbit DRAMs**
- **Page, nibble and static column accesses**
- **Fast burst access**
- **Interleaved or non-interleaved accesses to maximize system performance**
- **Programmable or mask-programmed versions**
- **Programmable refresh operations**
- **Staggered and burst refresh**
- **Refresh operations virtually transparent to the CPU**
- **Programmable wait states**
- **Byte operation with four independent $\overline{CAS}$ outputs**
- **Easy interface to all major microprocessors**
- **Built in delay line**
- **Synchronous and asynchronous operation**
- **On-chip capacitive load drivers**
- **Can be used with 25MHz clock**
- **CMOS technology for low power consumption**
- **TTL-compatible inputs**
- **68-pin PLCC package (KS84C21)**
- **84-pin PLCC package (KS84C22)**

PRODUCT OVERVIEW

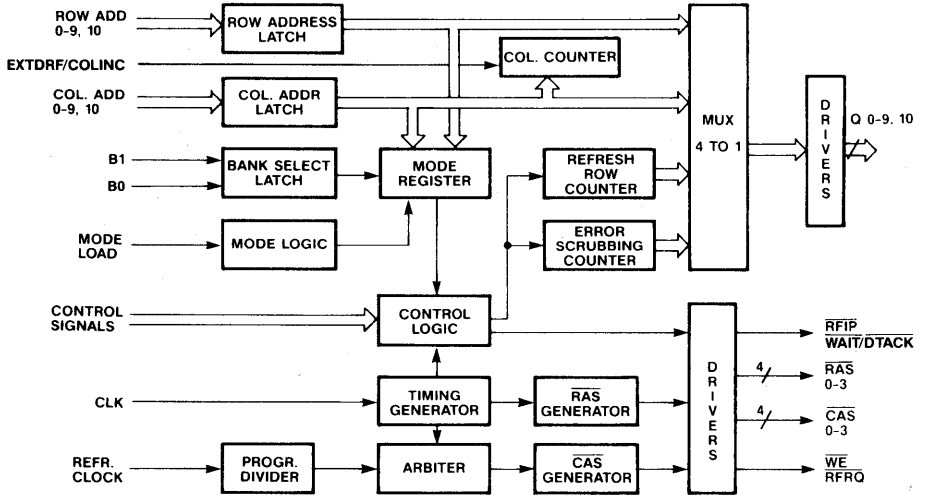
The Samsung KS84C21 and KS84C22 are high performance dynamic RAM (DRAM) controllers. They simplify the interface between the microprocessor and the DRAM array, while also significantly reducing the required design time. The KS84C21 supports the 256K DRAM and the 1MBit DRAM, while the KS84C22 supports the 256K DRAM, 1MBit DRAM and 4MBit DRAM.

Both devices are available in either externally programmable or masked programmable versions. The externally programmable version is an economic and flexible design solution for small-scale applications and prototyping. A 23-bit programmable Mode Register allows the selection of various options and features, including synchronous or asynchronous operation; interleaved or non-interleaved operation; burst or non-burst access; insertion of Wait States into the CPU cycle; a variety of refresh options; as well as the ability to fine tune the control signals.

A mask-programmed version of the chip offers the same Mode Register options. However, the chip is programmed at the factory to customer specifications. This version offers maximum system reliability and eliminates the need for external logic.

Both chips have a drive capability of 500pF, sufficient to drive memory arrays of up to 88 DRAMs under worst case conditions. Figure 1 shows a block diagram of the dynamic RAM controller.

Figure 1. KS84C21/C22 Block Diagram



INTERFACE SPECIFICATIONS

The Dynamic Ram Controller is available in two packages. The KS84C21, shown in Figure 2, is a 68-pin device and supports the 256K DRAM and 1Mbit DRAM. The KS84C22, shown in Figure 3, is an 84-pin device designed for use with the 256K DRAM, 1Mbit DRAM and 4Mbit DRAM.

Figure 2. Pin Configuration of the KS84C21 DRAM Controller

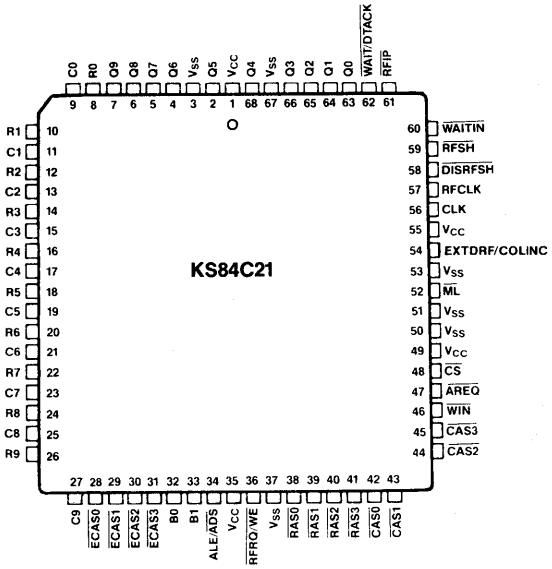


Figure 3. Pin Configuration of the KS84C22 DRAM Controller

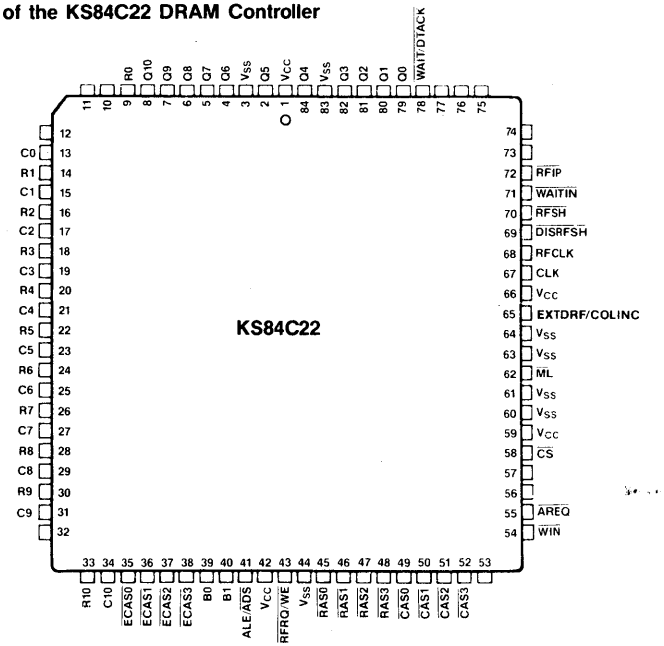


Table 1 shows detailed pin allocations for the KS84C21, while Table 2 shows the KS84C22. Table 3 provides the input/output signal definitions.

Note on Conventions:
A bar over the signal name is used to denote an active low signal ($\overline{ADS}$). Active high signals are shown with no bar (ALE).

Table 1. KS84C21 Pin Allocations

Pin No.	Signal Abbrev.	Signal Name
1	V_{CC}	V_{CC}
2	Q5	Multiplexed Address 5
3	V_{SS}	V_{SS}
4	Q6	Multiplexed Address 6
5	Q7	Multiplexed Address 7
6	Q8	Multiplexed Address 8
7	Q9	Multiplexed Address 9
8	R0	Row Address 0
9	C0	Column Address 0
10	R1	Row Address 1
11	C1	Column Address 1
12	R2	Row Address 2
13	C2	Column Address 2
14	R3	Row Address 3
15	C3	Column Address 3
16	R4	Row Address 4
17	C4	Column Address 4
18	R5	Row Address 5
19	C5	Column Address 5
20	R6	Row Address 6
21	C6	Column Address 6
22	R7	Row Address 7
23	C7	Column Address 7
24	R8	Row Address 8
25	C8	Column Address 8
26	R9	Row Address 9
27	C9	Column Address 9
28	$\overline{ECAS0}$	Enable $\overline{CAS0}$
29	$\overline{ECAS1}$	Enable $\overline{CAS1}$
30	$\overline{ECAS2}$	Enable $\overline{CAS2}$
31	$\overline{ECAS3}$	Enable $\overline{CAS3}$
32	B0	Bank Select 0
33	B1	Bank Select 1
34	ALE/$\overline{ADS}$	Address Latch Enable/ Address Strobe
35	V_{CC}	V_{CC}
36	$\overline{RFRQ/WE}$	Refresh Request/Write Enable
37	V_{SS}	V_{SS}
38	$\overline{RAS0}$	Row Address Strobe 0
39	$\overline{RAS1}$	Row Address Strobe 1
40	$\overline{RAS2}$	Row Address Strobe 2
41	$\overline{RAS3}$	Row Address Strobe 3
42	$\overline{CAS0}$	Column Address Strobe 0
43	$\overline{CAS1}$	Column Address Strobe 1
44	$\overline{CAS2}$	Column Address Strobe 2
45	$\overline{CAS3}$	Column Address Strobe 3
46	$\overline{WIN}$	Write Enable Input
47	$\overline{AREQ}$	Access Request
48	$\overline{CS}$	Chip Select
49	V_{CC}	V_{CC}
50	V_{SS}	V_{SS}
51	V_{SS}	V_{SS}
52	$\overline{ML}$	Mode Load
53	V_{SS}	V_{SS}
54	EXTDRF/ COLINC	External Refresh/ Column Increment
55	V_{CC}	V_{CC}
56	CLK	Clock
57	RFCLK	Refresh Clock
58	$\overline{DISRFSH}$	Disable Internal Refresh
59	$\overline{RFSH}$	External Refresh Request
60	$\overline{WAITIN}$	Add Wait State
61	$\overline{RFIP}$	Refresh in Progress
62	$\overline{WAIT}/\overline{DTACK}$	Wait/Data Transfer Acknowledge
63	Q0	Multiplexed Address 0
64	Q1	Multiplexed Address 1
65	Q2	Multiplexed Address 2
66	Q3	Multiplexed Address 3
67	V_{SS}	V_{SS}
68	Q4	Multiplexed Address 4

Table 2. KS84C22 Pin Allocations

Pin No.	Signal Abbrev.	Signal Name
1	V_{CC}	V_{CC}
2	Q5	Multiplexed Address 5
3	V_{SS}	V_{SS}
4	Q6	Multiplexed Address 6
5	Q7	Multiplexed Address 7
6	Q8	Multiplexed Address 8
7	Q9	Multiplexed Address 9
8	Q10	Multiplexed Address 10
9	R0	Row Address 0
10	—	N.C.
11	—	N.C.
12	—	N.C.
13	C0	Column Address 0
14	R1	Row Address 1
15	C1	Column Address 1
16	R2	Row Address 2
17	C2	Column Address 2
18	R3	Row Address 3
19	C3	Column Address 3
20	R4	Row Address 4
21	C4	Column Address 4
22	R5	Row Address 5
23	C5	Column Address 5
24	R6	Row Address 6
25	C6	Column Address 6
26	R7	Row Address 7
27	C7	Column Address 7
28	R8	Row Address 8
29	C8	Column Address 8
30	R9	Row Address 9
31	C9	Column Address 9
32	—	N.C.
33	R10	Row Address 10
34	C10	Column Address 10
35	$\overline{ECAS0}$	Enable $\overline{CAS0}$
36	$\overline{ECAS1}$	Enable $\overline{CAS1}$
37	$\overline{ECAS2}$	Enable $\overline{CAS2}$
38	$\overline{ECAS3}$	Enable $\overline{CAS3}$
39	B0	Bank Select 0
40	B1	Bank Select 1
41	ALE/$\overline{ADS}$	Address Latch Enable/ Address Strobe
42	V_{CC}	V_{CC}
43	$\overline{RFRQ/WE}$	Refresh Request/Write Enable
44	V_{SS}	V_{SS}
45	$\overline{RAS0}$	Row Address Strobe 0
46	$\overline{RAS1}$	Row Address Strobe 1
47	$\overline{RAS2}$	Row Address Strobe 2
48	$\overline{RAS3}$	Row Address Strobe 3
49	$\overline{CAS0}$	Column Address Strobe 0
50	$\overline{CAS1}$	Column Address Strobe 1
51	$\overline{CAS2}$	Column Address Strobe 2
52	$\overline{CAS3}$	Column Address Strobe 3
53	—	N.C.
54	$\overline{WIN}$	Write Enable Input
55	$\overline{AREQ}$	Access Request
56	—	N.C.
57	—	N.C.
58	$\overline{CS}$	Chip Select
59	V_{CC}	V_{CC}
60	V_{SS}	V_{SS}
61	V_{SS}	V_{SS}
62	$\overline{ML}$	Mode Load
63	V_{SS}	V_{SS}
64	V_{SS}	V_{SS}
65	EXTDRF/ COLINC	Extend Refresh/ Column Increment
66	V_{CC}	V_{CC}
67	CLK	Clock
68	RFCLK	Refresh Clock
69	$\overline{DISRFSH}$	Disable Internal Refresh
70	$\overline{RFSH}$	External Refresh Request
71	$\overline{WAITIN}$	Add Wait State
72	$\overline{RFIP}$	Refresh in Progress
73	—	N.C.
74	—	N.C.
75	—	N.C.
76	—	N.C.
77	—	N.C.
78	$\overline{WAIT/DTACK}$	Wait/Data Transfer Acknowledge
79	Q0	Multiplexed Address 0
80	Q1	Multiplexed Address 1
81	Q2	Multiplexed Address 2
82	Q3	Multiplexed Address 3
83	V_{SS}	V_{SS}
84	Q4	Multiplexed Address 4

Table 3. Interface Signal Definitions

Note: I indicates an input signal. O indicates an output signal. Timing notations (t12) etc. are referenced to the timing diagrams at the end of the product description.

Symbol	Type	Description
$\overline{ADS}$/ALE	I	**Address Strobe/Address Latch Enable:** This input latches row, column and bank addresses, and initiates DRAM access. Addresses are strobed independently of $\overline{CS}$, however $\overline{CS}$ must be low to initiate an access. While $\overline{ADS}$ or ALE is high, the on-chip row address latches are transparent to the input. The column address can be strobed into the column counter by ALE/$\overline{ADS}$ while $\overline{CS}$ is high. In Mode 0: This input functions as address latch enable ALE. In Mode 1: This input is active low, and functions as address strobe signal. The falling edge of $\overline{ADS}$ also starts an access, if $\overline{CS}$ is low for the set-up time t_{12}. (Mode is selected by Bit B1 in the Mode Register. See PROGRAMMING THE KS84C21/C22.)
$\overline{AREQ}$	I	**Access Request:** This input terminates an access. In non-interleave mode: it brings $\overline{RAS}$ high. $\overline{CAS}$ depends on how $\overline{ECAS0}$ is programmed. In interleave mode: it brings $\overline{CAS}$ and $\overline{RAS}$ high.
B0, B1	I	**Bank Select:** These inputs are bank addresses, and allow one, two or four memory banks to be selected. Selection depends upon how C4, C5 and C6 in the Mode Register are set.
C0-9, 10	I	**Column Address Inputs:** These column address bits are usually connected to the high order address bits of the microprocessor. They select columns in the DRAM cell configuration.
$\overline{CAS0-3}$	O	**Column Address Strobe:** These inputs strobe the column address. They go low after the programmed Column Address Set-up time of 0 or 10ns.
CLK	I	**Clock:** This is the system clock. It is used for bus arbitration and timing purposes. Synchronous access requests must be synchronized with the system clock. The duty cycle is significant if 1/2T Wait State is programmed.
$\overline{CS}$	I	**Chip Select:** The $\overline{CS}$ input must be low to enable a DRAM access. Row, column and bank address are strobed independently of $\overline{CS}$. There is a pre-access setup time. In Mode 0 this is the rising edge of CLK, and in Mode 1 the falling edge of $\overline{ADS}$.*
EXTDRF/ COLINC	I	**Extend Refresh/Column Increment:** This input has two functions. During a DRAM access, toggling COLINC increments the latched column address, which can be used to access incremental memory locations within a row. During refresh, EXTDRF extends a refresh cycle, to allow a read-modify-write cycle to be performed in a system with error correction. See ERROR SCRUBBING.
$\overline{DISRFSH}$	I	**Disable Internal Refresh:** When low, this input disables Internal Refresh.
$\overline{ECAS0-3}$	I	**Enable $\overline{CAS0-3}$:** These inputs are used to enable or disable individual $\overline{CAS}$ outputs, or delay $\overline{CAS}$ from going low. They are useful when accessing bytes, nibbles or pages. $\overline{ECAS0}$ also programs output $\overline{WE}$ ($\overline{RFRQ}$), and sets the trailing edge of $\overline{CAS}$.

*Note: $\overline{CS}$ must be low until $\overline{AREQ}$ terminates the access in Mode 0

Table 3. Interface Signal Definitions (Continued)

Symbol	Type	Description
$\overline{ML}$	I	**Mode Load:** This input latches the row, column, $\overline{ECAS0}$, and bank address inputs into the Mode Register.
Q0-9, 10	O	**Address Outputs:** These outputs are the multiplexed address bits (R0-10, C0-10). They access the memory for read, write and refresh operations. The output load may be as high as 500pF.
R0-9, 10	I	**Row Address Inputs:** These address inputs are usually connected to the low order address bits of the microprocessor. They select rows in the DRAM cell configuration.
$\overline{RAS0-3}$	O	**Row Address Strobe:** These row address strobe signals are used to strobe the row addresses into the DRAM.
RFCLK	I	**Refresh Clock:** This input determines the timing of the refresh cycles for the DRAMs. It should be a multiple of 2MHz. It is divided according to bits C0, 1, 2, and C3 in the Mode Register, so that the refresh cycles occur at 15μs or 13μs intervals. **Note:** The Refresh Clock should be derived from or driven by the CLK source.
$\overline{RFIP}$	O	**Refresh in Progress:** This output indicates that a refresh cycle is in progress. $\overline{RFIP}$ goes low one CLK cycle prior to the start of a refresh cycle.
$\overline{RFSH}$	I	**External Refresh Request:** Refresh cycles can be requested externally by driving the $\overline{RFSH}$ signal low.
$\overline{WAITIN}$	I	**Add Wait State:** If this input is low, one or two extra Wait States will be added to the access cycle at an external event, e.g. memory read.
$\overline{WAIT/DTACK}$	O	**Wait/Data Transfer Acknowledge:** This output inserts Wait States into CPU access cycles. The output is controlled by bits R2, R3, R4, R5 and R7, in the Mode Register.
$\overline{WE/RFRQ}$	O	**Write Enable/Refresh Request:** After Power up reset and in interleave mode, this output functions as refresh request. In non-interleave mode it can be programmed to function as the $\overline{WE}$ output if $\overline{ECAS0}$ is low in the Mode Register.
$\overline{WIN}$	I	**Write Enable Input:** This input controls the $\overline{WE}$ output, and delays $\overline{CAS}$, if programmed to do so by bit C9 in the Mode Register.

KS84C21/22 OPERATION

Introduction

The KS84C21/22 support both synchronous and asynchronous operations; interleaved or non-interleaved accesses; burst and non-burst accesses, and a variety of refresh operations. They generate all the signals required to control these various functions, by means of the Mode Register. (See PROGRAMMING THE KS84C21/22.) Timing characteristics for typical operations are shown under AC SWITCHING CHARACTERISTICS.

Reset

Power Up Reset

The KS84C21/22 on-chip power-up reset logic generates a reset pulse:

- At power up;
- If V_{CC} falls well below +3.0V, and reaches V_{CC} min. (Short spikes below the minimum V_{CC} will not reset the chip. However, correct functionality is guaranteed only within the operating conditions.)

When the chip is reset, all internal flip-flops, counters, and the Mode register are reset, and the output lines are inactive: $\overline{RAS0}$-3, $\overline{CAS0}$-3, $\overline{WAIT}$ ($\overline{DTACK}$), $\overline{RFIP}$, $\overline{WE}$ ($\overline{RFRQ}$) are high, while Q0-9, 10 are low. Note that there are no tri-state buffers on any of the outputs.

The chip does not need any time to synchronize after power up, it is operable after 200 microseconds, as required by most DRAMs.

After power-up reset, the Mode Register must be reprogrammed in the programmable version of the chip.

External Reset

The Mode Load signal ($\overline{ML}$) can also be used to reset the chip. When $\overline{ML}$ is driven low, all counters and flip-flops are reset, and the Mode Register is enabled to receive the mode bit inputs.

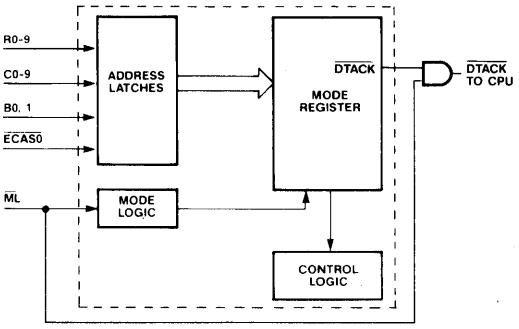
Programming the KS84C21/22

The KS84C21/22 has a Mode Register that can be programmed by the user, or mask-programmed at the factory. The outputs from the register control the internal program modes.

Mode Register

Figure 4 shows data flow to and from the Mode Register.

Figure 4. Mode Register Data Flow



The Mode Register receives inputs from the CPU on the address lines: Row addresses R0-9, Column addresses C0-9, and Bank addresses B0, B1 and $\overline{ECAS0}$. These bits are loaded into the Register when Mode Load ($\overline{ML}$) goes low. Alternatively, the Mode Register may be programmed by initiating a 'dummy' access, as shown in the Mode Load Timing Characteristics (Figure 11, AC Switching Characteristics). $\overline{ML}$, $\overline{CS}$ and $\overline{AREQ}$ are asserted, the addresses are loaded into the Mode Register on the falling edge of $\overline{AREQ}$, while $\overline{ML}$ and $\overline{CS}$ are low, or when $\overline{ML}$ goes high (whichever occurs first). $\overline{DTACK}$ is not asserted during a "dummy" access and must be generated externally to terminate the access.

It is necessary to program the chip after power up, and before using it in normal operation. The inputs to the register are encoded to control a variety of functions, as shown in Table 4. Note that inputs R10 and C10 of the KS84C22 do not program the Mode Register.

Note: Make sure that the CPU is not in a indefinite Wait State when loading the Mode Register by a dummy access.

The 84C21/22 are set for error scrubbing after power up or reset by $\overline{ML}$ low. A "1" on the EXTDRF input will extend the refresh cycle if the device has not been programmed before the first refresh occurs.

Table 4. Programming the Mode Register

ADDRESS LATCH

B0 allows the user to decide whether address inputs should be latched by $\overline{ADS}$/ALE, or whether the address latches should be permanently transparent and merely allow passage of the address inputs.

B0	
0	Address bits latched.
1	Address latches transparent.

ACCESS MODES

B1 allows the user to select either synchronous or asynchronous access modes.

In Mode 0 (synchronous), access is controlled by the system clock, and the access $\overline{RAS}$ is initiated on the rising edge of the first clock input after ALE goes high. $\overline{AREQ}$ is used to terminate the $\overline{RAS}$ cycle.

In Mode 1 (asynchronous), the falling edge of $\overline{ADS}$ initiates an access immediately, and the rising edge of $\overline{AREQ}$ terminates $\overline{RAS}$.

B1	
0	Access Mode 0 (synchronous)
1	Access Mode 1 (asynchronous)

ENABLE COLUMN ADDRESS STROBE

$\overline{ECAS0}$ Controls the $\overline{CAS}$ outputs. Only one $\overline{ECAS}$ Mode Register.

$\overline{ECAS0}$	
0	$\overline{CAS}$n outputs are negated with $\overline{AREQ}$ in non-interleave mode. $\overline{WE}$ output is selected.
1	$\overline{CAS}$n outputs can be held low until the rising edge of CLK, after $\overline{RAS}$ is deasserted in non-interleave mode. $\overline{RFRQ}$ is selected.

$\overline{RAS}$ LOW AND $\overline{RAS}$ PRECHARGE TIME

R0, R1 These bits control the period of time that $\overline{RAS}$ is low during refresh operations, and also determine the guaranteed $\overline{RAS}$ precharge time. The time interval shown (T) is equivalent to one Clock (CLK) cycle. $\overline{RAS}$ precharge is the minimum number of CLK cycles. The actual precharge time can be longer.

R0	R1	$\overline{RAS}$ Low Time	$\overline{RAS}$ Precharge Time
0	0	2T	1T
0	1	2T	2T
1	0	3T	2T
1	1	4T	3T

Table 4. Programming the Mode Register (Continued)

WAIT OR DTACK GENERATION FOR NON-BURST MODE ACCESSES

R2, R3, R7

These bits control the WAIT or DTACK generation modes for non-burst accesses. Bit R7 is set to select either WAIT or DTACK type of output. The time interval shown (T) is equal to one Clock cycle.

R7	R2	R3	WAIT High from Access RAS Low. Non-delayed Access	WAIT High from Access RAS Low, After Delayed Access	DTACK Low from RAS Low
0	0	0	No wait states	0T	—
0	0	1	No wait states	1/2T	—
0	1	0	1/2T	1/2T	—
0	1	1	1T	1T	—
1	0	0	—	—	0T
1	0	1	—	—	1/2T
1	1	0	—	—	1T
1	1	1	—	—	1-1/2T

WAIT OR DTACK GENERATION FOR BURST MODE ACCESSES

R4, R5

R4 and R5 Control WAIT or DTACK generation modes during burst mode accesses.

R4	R5	Condition	
0	0	No wait states.	WAIT stays high and DTACK stays low from previous access.
0	1	1/2T.	WAIT goes high on the falling edge of the next CLK after ECASn goes low. (DTACK goes low)
1	0	1T.	WAIT goes high on the rising edge of the next CLK. DTACK goes low one CLK cycle after CAS.
1	1	0T.	WAIT (DTACK) follows CAS.

ADDS WAIT STATE

R6

R6 adds wait states to the current access if WAITIN is low.

R6	Condition
0	Hold WAIT low (DTACK high) for one extra clock period.
1	Hold WAIT low (DTACK high) for two extra clock periods.

Table 4. Programming the Mode Register (Continued)

INTERLEAVING

R8

R8 Determines whether the DRAM is accessed in interleaved or non-interleaved mode.

In interleaved mode, the row addresses are multiplexed to the DRAM controller address outputs, after the column addresses have been held for a sufficient time (35ns minimum) after $\overline{CAS}$ has gone low.

In non-interleaved mode, the column addresses are held on the DRAM controller address outputs until $\overline{CAS}$ goes high.

R8	
0	Interleaved mode
1	Non-interleaved mode

STAGGERED REFRESH OPERATIONS

R9

R9 determines whether the refresh operation is standard, or staggered.

During a standard refresh cycle, all $\overline{RAS}$ outputs will be asserted and deasserted at the same time.

In staggered refresh operations, the $\overline{RAS}$ outputs will go low in sequence, at one clock intervals. One or two $\overline{RAS}$ outputs are selected at a time, depending upon the $\overline{RAS}/\overline{CAS}$ configuration selected by the setting of C4-C6. There is no error scrubbing during this type of refresh.

R9	
0	Standard refresh
1	Staggered refresh

RFCLK DIVIDER

C0, C1, C2

These bits allow the user to select the divider for the refresh clock input (RFCLK), from which the internal REFRESH clock is generated. Select divider such that the result is an approximately 2MHz clock (REFRESH).

C0	C1	C2	
0	0	0	Divide by 10
0	0	1	Divide by 6
0	1	0	Divide by 8
0	1	1	Divide by 4
1	0	0	Divide by 9
1	0	1	Divide by 5
1	1	0	Divide by 7
1	1	1	Divide by 3

Table 4. Programming the Mode Register (Continued)

REFRESH CLOCK DIVIDER

C3

C3 allows the user to divide the internal refresh clock (REFRESH), to get the required refresh cycle time.

C3	
0	Divide by 30. Divides the internal REFRESH clock (usually 2MHz) by 30, to produce a refresh clock period every 15 microseconds.
1	Divide by 26. Divides the internal REFRESH clock (usually 2MHz) by 26, to produce a refresh clock period every 13 microseconds.

$\overline{RAS}$ AND $\overline{CAS}$ CONFIGURATIONS

C4, C5, C6

These bits, in conjunction with B0 and B1 control the $\overline{RAS}$ and $\overline{CAS}$ configurations. There are four $\overline{RAS}$ and four $\overline{CAS}$ outputs, that can be grouped so that each $\overline{RAS}$ and $\overline{CAS}$ will drive one fourth of the array, regardless of whether the array is arranged in 1, 2 or 4 banks. The setting of these bits also determines whether error scrubbing and interleaving can be supported.

C4	C5	C6	$\overline{RAS}$ and $\overline{CAS}$ Configuration Modes	Error* Scrubbing	Support Interleaving
0	0	0	$\overline{RAS}$0-3 are brought low during an access. $\overline{CAS}$0-3 are all selected during an access but only those enabled by the corresponding $\overline{ECAS}$ can go low. B0 and B1 are not used.	Yes	No
0	0	1	$\overline{RAS}$ groups are selected by B1. B0 is not used. All $\overline{CAS}$ outputs are selected, making this mode useful for byte writing via $\overline{ECAS}$0-3 inputs and the $\overline{CAS}$0-3 outputs.	No	No
0	1	0	$\overline{RAS}$, $\overline{CAS}$ pairs selected by B0 and B1. A particular $\overline{CAS}$ cannot go low unless its $\overline{ECAS}$ is also low.	Yes	Yes
0	1	1	$\overline{RAS}$n is selected by B0 and B1. $\overline{CAS}$ outputs are selected with the corresponding $\overline{ECAS}$ input, making this mode useful for byte writing via $\overline{ECAS}$0-3 inputs and the $\overline{CAS}$0-3 outputs.	No	No
1	0	0	$\overline{RAS}$, $\overline{CAS}$ groups selected by B1. A particular $\overline{CAS}$ cannot go low unless its $\overline{ECAS}$ is also low.	Yes	Yes

B1	B0	
0	—	$\overline{RAS}$0, 1
1	—	$\overline{RAS}$2,3

B1	B0	
0	0	$\overline{RAS}$0 and $\overline{CAS}$0
0	1	$\overline{RAS}$1 and $\overline{CAS}$1
1	0	$\overline{RAS}$2 and $\overline{CAS}$2
1	1	$\overline{RAS}$3 and $\overline{CAS}$3

B1	B0	
0	0	$\overline{RAS}$0
0	1	$\overline{RAS}$1
1	0	$\overline{RAS}$2
1	1	$\overline{RAS}$3

B1	B0	
0	—	$\overline{RAS}$0, 1 and $\overline{CAS}$0, 1
1	—	$\overline{RAS}$2, 3 and $\overline{CAS}$2, 3

Table 4. Programming the Mode Register (Continued)

RAS AND CAS CONFIGURATIONS (Continued)

C4	C5	C6	RAS and CAS Configuration Modes	Error* Scrubbing	Support Interleaving
1	0	1	RAS, CAS groups are selected by B1. A particular CAS cannot go low unless its ECAS is also low.	No	Yes
1	1	0	RAS0-3 and CAS0-3 are all selected during an access. This mode is useful for byte writing via ECAS0-3 inputs and the CAS0-3 outputs. B0 and B1 are not used.	No	No
1	1	1	RASn and CASn are selected by B0 and B1. A particular CAS cannot go low unless its ECAS is also low.	No	Yes

B1	B0	
0	—	RAS0, 1 and CAS0, 1
1	—	RAS2, 3 and CAS2, 3

B1	B0	
0	0	RAS0 and CAS0
0	1	RAS1 and CAS1
1	0	RAS2 and CAS2
1	1	RAS3 and CAS3

***Note:** Internal refresh only.

COLUMN ADDRESS SETUP TIME SELECTION

C7 allows the user to select a minimum guaranteed setup time (t_{ASC}) for the column address inputs.

C7	
0	Selects 10ns setup time.
1	Selects 0ns setup time.

ROW ADDRESS HOLD TIME SELECTION

C8 allows the user to select a minimum guaranteed hold time (t_{RAH}) for the row address inputs.

C8	
0	Selects 25ns hold time.
1	Selects 15ns hold time.

DELAY CAS DURING WRITE ACCESSES

C9 allows the user to delay CAS during write operations. If no delay is selected, CAS is treated in the same way for read and write operations. If delay is selected, CAS is delayed for one rising clock edge after RAS goes low.

C9	
0	No delay.
1	Delay selected.

Standard Access Operations

The versatile KS84C21/C22 chips support a variety of DRAM operations. They enable read and write accesses, in synchronous or asynchronous mode, with or without interleaving, and in burst or non-burst mode. Typical operations are illustrated in the timing diagrams at the end of this Product Description.

Operating Features

DRAM performance is optimized under the control of the KS84C21/C22, as a function of the special operating features designed into the chips. This section describes some of the features that enhance DRAM performance.

Controlling Precharge Time

The precharge time of the DRAM, or the time the chip takes to stabilize between accesses, negatively impacts the overall access speed of the memory devices. Since the DRAM performance is generally trailing CPU throughput time, the DRAM controller can play an important role in improving overall system performance.

$\overline{RAS}$ Low and $\overline{RAS}$ Precharge Time. $\overline{RAS}$ precharge time can be programmed using bits R0 and R1 in the Mode Register. The precharge time is guaranteed during access and refresh. $\overline{RAS}$ low and $\overline{RAS}$ precharge times are counted by the rising edges of the CLK input. Each bank of memory devices has its own precharge counter. This is an important feature, since the KS84C21/C22 allows memory interleaving of 2 or 4 memory banks.

$\overline{AREQ}$ must go high at t_{C22} with respect to the rising edge of the CLK input, to be counted as 1T of the programmed precharge time. An access will start with the following CLK edge that is programmed by R0, 1.

The KS84C21/C22 inserts Wait States as required, to keep the CPU and DRAM interactions in step. The system designer is responsible, however, for making sure that the appropriate numbers of Wait States are inserted to keep $\overline{RAS}$ low for the period of time required by the DRAM specification.

$\overline{CAS}$ Precharge Time. The $\overline{ECASn}$ input controls $\overline{CAS}$ precharge time during a burst access. The $\overline{CASn}$ output is a direct function of the $\overline{ECASn}$ input. The KS84C21/C22 does not monitor precharge time t_{CP} or t_{NCP} in a page or nibble access.

Access Features

The KS84C21/C22 enables a number of types of DRAM access, that either enhance DRAM performance, or increase the DRAM's flexibility in specific applications.

Static Column Access. With this type of access, a specific memory row is accessed, and the column addresses to that row are incremented with COLINC, enabling sequential accesses, without invoking a succession of $\overline{RAS}$ and $\overline{CAS}$ signals.

Access to Random. Column address can be accomplished by strobing the new column address with a high/low transition on ALE/$\overline{ADS}$ input while $\overline{CS}$ is high. Note that the page comparator is not built in.

Page Access. The KS84C21/22 DRC is capable of performing random column accesses within a page when used with page or static column mode DRAMs. When used in this mode, $\overline{AREQ}$ remains asserted from the opening access in order to keep $\overline{RAS}$ asserted. In Mode 1, the new column address is strobed onto the DRAM address bus on the falling edge of $\overline{ADS}$. $\overline{CS}$ must be negated before the falling edge of $\overline{ADS}$ in order to keep the DRC from strobing a new row address onto the bus and performing another opening access. In Mode 0, $\overline{CS}$ must be negated before the rising edge of CLK after ALE is pulsed high.

When used in this mode, the user is responsible for insuring that the DRAM's maximum $\overline{RAS}$ low time and minimum $\overline{CAS}$ precharge time is not violated. Since the DRC will not perform a refresh until $\overline{AREQ}$ negates $\overline{RAS}$, it is suggested that $\overline{RFRQ}$ be monitored in order to negate $\overline{AREQ}$ when an internal refresh request is pending.

For such applications as frame buffer, or printer buffer, the KS84C21/C22 support fast page accesses, in which a specific row is accessed, and incremental column addresses within that row are accessed sequentially. The built in column counter provides the column address. If the row changes, a new access must be initiated with $\overline{ADS}$/ALE.

Access to Random. Column address can be accomplished by strobing the new column address with a high/low transition on ALE/$\overline{ADS}$ input while $\overline{CS}$ is high. Note that the page comparator is not built in.

Memory Interleaving. Performance is similarly enhanced if consecutive accesses are made to different memory banks by hiding the precharge time in the access of subsequent access cycle. The KS84C21/C22 supports access to up to 88 DRAMs, arranged in up to four banks, each containing 16 memory devices for data and 6 for error correction. The bank address bits, B0 and B1 are the least significant bits, as seen by the CPU. The KS84C21/C22 ensures that the DRAM will be precharged for the programmed number of CLK cycles by inserting Wait States. The precharge counter, as programmed by

R0 and R1, keeps track of the CLK inputs, and after reaching the programmed number, the rising edge of the next CLK input is used to complete the current cycle. The precharge counter starts with the rising edge of the first CLK input (which is counted as 1T) that occurs after the low-to-high transition of $\overline{AREQ}$. There is a required setup time to the rising edge of CLK of t_{C22}.

Delay $\overline{CAS}$

An early write cycle to a DRAM is useful if the input data is not stable at the falling edge of $\overline{WE}$, or if bidirectional data buffers are used. With this sort of access, $\overline{WE}$ goes low before $\overline{CAS}$ is low. The column address bits and data are stored in the DRAM latches on the falling edge of $\overline{CAS}$. The data output buffer of the DRAM is tri-stated during the entire $\overline{RAS}$ cycle.

To achieve an early write cycle, the $\overline{CAS}$ output of the KS84C21/C22 can be delayed one CLK cycle, if bit C9 of the Mode Register is set appropriately. $\overline{CAS}$ will go low t_{C24} after the rising edge of CLK. If $\overline{CAS}$ has been delayed in this way, and requires further delay, this can be done by holding ECASn high, which prevents $\overline{CAS}$ from going low.

Conversely, a late write access may be required, in which $\overline{WE}$ is asserted after $\overline{CAS}$. In this case, the column address bits are latched into the DRAMs on the falling edge of $\overline{CAS}$ and the input data is latched on the falling edge of $\overline{WE}$.

Wait States

Wait states are required when a relatively slow DRAM is operating with a fast CPU. The KS84C21/C22 generates the $\overline{WAIT}$ signal, and sends it back to the CPU instructing it to insert a Wait. This means that the CPU will not look for data prematurely, and during a Refresh operation, an access is deferred. Bit R7 of the Mode Register must be set to '0' to instigate this feature.

If the Wait state is not selected, the KS84C21/C22 generates a handshaking signal, $\overline{DTACK}$, which is returned to the CPU to acknowledge transfer of data.

Refresh Operations

The KS84C21/22 provide a number of refresh options, as described below.

Automatic Internal Refresh

Internal refresh is generated by an internal refresh counter, which keeps track of the refresh intervals, and also supplies the row address bits required to refresh the memory area. (Internal refresh is a $\overline{RAS}$-only operation.) The refresh period is selected by bits C0, C1, C2 and C3 of the Mode Register.

The refresh period for most DRAMs is 15 microseconds. This means that the one megabit DRAM has to be refreshed every eight milliseconds, during which time, 512 rows must be accessed. This calls for a 9-bit refresh counter. The KS84C21 has a 10-bit counter, and the C22 has an 11-bit counter. The extra bits are used for error scrubbing over the whole address range.

If a refresh is requested by the on-chip Refresh counter, while an access is in progress, that access is finished before the refresh cycle is initiated. The next access is deferred until the refresh cycle is complete. The wait logic automatically inserts Wait States.

Internal refresh is possible in both interleaved and non-interleaved modes.

Automatic Internal Staggered Refresh

Staggered refresh, during which the $\overline{RAS}$ signals are staggered at one CLK intervals, can be selected by appropriately setting bit R9 in the Mode Register. This type of cycle allows the memory area to be refreshed with minimum switching current.

External Controlled Refresh

Refresh operations can be controlled externally and can be either 'all $\overline{RAS}$' or staggered. As for internal refresh, the row address bits are supplied by the on-chip refresh counter.

Internal refresh must be disabled by driving $\overline{DISRFSH}$ low. $\overline{RFSH}$ must go low at setup time t_{R1}.

Refresh Request Divider

The refresh request divider (derived from the programmable divider) asserts the $\overline{RFRQ}$ output, if internal or external refresh has been selected by $\overline{DISRFSH}$.

Clearing the Refresh Counter (Row Address)

The refresh counter is cleared by driving $\overline{DISRFSH}$ high and $\overline{RFSH}$ low, with a setup time of t_{R1} to the rising edge of CLK. This procedure does not invoke a refresh of the DRAM.

Error Scrubbing

In a system with error correction, transparent error scrubbing is one method of increasing data integrity. A full access is performed during refresh, during which data and ECC bits are continuously updated and checked, and random bit errors corrected. The error scrubbing option is selected by appropriately setting bits C4, C5 and C6 of the Mode Register.

When the KS84C21/22 are programmed for error scrubbing, a complete memory access is performed during the refresh cycle. The 10- or 11-bit internal scrubbing counter provides the column address bits, and the 10- or 11-bit refresh counter provides the row address bits. Error scrubbing is done by word, not by byte.

If the error correction circuitry detects an error, the error is corrected by writing the corrected word to the DRAM by means of the read-modify-write operation. (The data is read and checked during the read portion, and modified/corrected data is written back during the write portion.)

To enable this type of cycle, EXTDRF must be asserted while $\overline{RAS}$ is low. $\overline{RAS}$ and $\overline{CAS}$ remain low until the rising edge of the next CLK, after EXTDRF has gone low again.

Although the KS84C21/22 control the error scrubbing, they do not provide the error correction circuitry.

Access Modes

The KS84C21/22 support both synchronous and asynchronous operations. The user can select the mode most suited to the microprocessor with which the DRAM is interfacing, by means of bit B1 in the Mode Register.

Mode 0 — Synchronous Access

Mode 0 is selected when B1 = 0. To initiate a Mode 0 operation, ALE must pulse high t_{02} before the rising edge of the clock input (CLK). Provided that the chip select signal ($\overline{CS}$) has been established at t_{01} before the rising edge of the next CLK input, access will start on the rising edge of that CLK. $\overline{CS}$ must stay asserted until $\overline{AREQ}$ terminates the access.

Since ALE is high, the address latch is transparent to the address inputs, and, if the chip is programmed in Address Latch Mode (B0 = 0), the latch stores the address bits that were present one setup time (t_{06}) before the high-to-low transition of ALE. If the chip is not in Latch Mode (B0 = 1), the address inputs have to meet the setup time of t_{05} to the rising edge of CLK, to make sure that the row address bits are on the Q output when row address strobe ($\overline{RAS}$) is asserted.

Mode 1 — Asynchronous Access

Mode 1 is selected when B1 = 1. To initiate a Mode 1 operation, $\overline{CS}$ must be low for t_{12} before $\overline{ADS}$ goes low. If the chip is programmed in Address Latch Mode, the address latch, which is transparent to address inputs while $\overline{ADS}$ is high, stores the address that was present one set up time t_{14} before the high-to-low transition of the $\overline{ADS}$ signal.

Interleaving

The KS84C21/22 support both interleaved and non-interleaved memory operation. Interleaving is controlled by the R8 input to the Mode Register.

Interleaving

With R8 set at 0, the chip supports interleaved accessing of the DRAM. This is a way of reducing access cycle time. In interleaved mode, access cycles (read or write) are overlapped, so that before an access cycle is completed in one memory bank location, another access may be started in a different memory bank. Since the precharge time of most DRAMs is between 80 and 100 nanoseconds (about the same length as t_{RAS}), interleaving can save up to 50% of cycle time. $\overline{AREQ}$ may be deasserted before the column address hold time.

Memory accesses can only be overlapped in physically separated banks of memory, and may occur during precharge time. The column address hold time is assured by the DRC.

Interleaving can take place in either Mode 0 or Mode 1.

Non-Interleaving

When R8 is set at 1, the chip does not support interleaving. The address lines from the microprocessor are connected to the Row (R), Column (C), and Bank (B) inputs of the KS84C21. B0 and B1 (bank address bits) may be connected to the most significant or the least significant address bits.

Access starts in Mode 0 if ALE pulses high t_{02} before the edge of the CLK input. In Mode 1, access starts when $\overline{CS}$ remains low for t_{12} before the falling edge of $\overline{ADS}$. In both cases, access is terminated when $\overline{AREQ}$ goes high, terminating $\overline{RAS}$. $\overline{CAS}$ goes high or stays low until the rising edge of the next CLK, as programmed by ECAS0.

DC ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

DC Supply Voltage 7V
Temperature Under Bias ..... 0°C + 70°C
Storage Temperature ..... -65°C to 150°C
All Input and Output Voltage ..... V_{SS} - 0.5V to +7V
Power Dissipation at 25MHz 0.6W
E.S.D. 2000V

Note: If the device is used beyond the maximum rating, permanent damage may occur. Operation should be limited to those conditions specified under DC Electrical Characteristics.

DC Electrical Characteristics (T_A = 0°C to +70°C, V_{CC} = 4.5V to 5.5V, V_{SS} = 0V)

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IH}	Input High Voltage	Tested with limited Test pattern	2.0		V_{CC}+0.5	V
V_{IL}	Input Low Voltage	Tested with limited Test pattern	-0.5		0.8	V
V_{OH1}	Q and $\overline{WE}$ Outputs	I_{OH} = -10mA	2.4			V
V_{OL1}	Q and $\overline{WE}$ Outputs	I_{OL} = 10mA			0.5	V
V_{OH2}	All outputs except Q and $\overline{WE}$	I_{OH} = -3mA	2.4			V
V_{OL2}	All outputs except Q and $\overline{WE}$	I_{OL} = 3mA			0.5	V
I_{IN}	Input Leakage Current	V_{IN} = V_{CC} or V_{SS}			±10	μA
I_{ILML}	$\overline{ML}$ Input Current	V_{IN} = V_{SS}			200	μA
I_{CC1}	Quiescent Current	CLK at 25MHz Inputs Inactive			15	mA
I_{CC2}	Supply Current	Inputs Active (I load = 0)		50	95	mA
C_{IN}	Input Capacitance	f_{IN} at 1MHz		5	10	pF

AC SWITCHING CHARACTERISTICS

Figure 5 shows a typical test circuit, while Figure 6 shows the output drive levels. Figures 7 through 14 provide switching characteristics for a number of typical KS84C21/C22 operations:

- Figure 7. Mode 0 Interleave
- Figure 8. Mode 0 Wait State, Non-Interleave
- Figure 9. Mode 1 Interleave, Address Latch
- Figure 10. Burst Access, Page Mode
- Figure 11. Non-Interleave, Delay $\overline{CAS}$
- Figure 12. Mode Load
- Figure 13. CLK, RFCLK Timing
- Figure 14. Internal Refresh
- Figure 15. Refresh and Extend Refresh
- Figure 16. Staggered Refresh

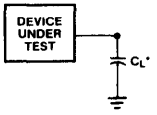
Unless otherwise stated V_{CC} = 4.5V to 5.5V, $0 < T_A < 70°C$

Load Capacitance: Q0-Q9, Q10 C_L = 380pF
$\overline{WE}$ C_L = 500pF
$\overline{RAS0-3}$, $\overline{CAS0-3}$ C_L = 125pF
All other Outputs C_L = 50pF

All minimum and maximum values are measured in nanoseconds.

CAPACITIVE LOAD SWITCHING

Figure 5. Switching Test Circuit



*t_{PD} SPECIFIED AT C_L = 380pF ALL Q OUTPUTS
C_L = 125pF $\overline{RAS}$ AND $\overline{CAS}$ OUTPUTS
C_L = 500pF $\overline{WE}$ OUTPUT

TYPICAL SWITCHING CHARACTERISTICS

Figure 6a. Output Drive Levels

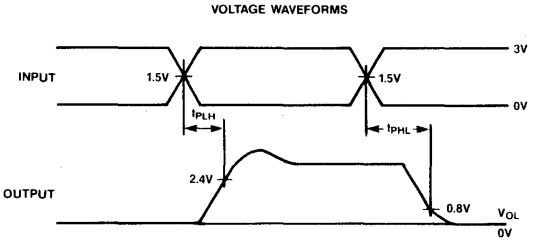
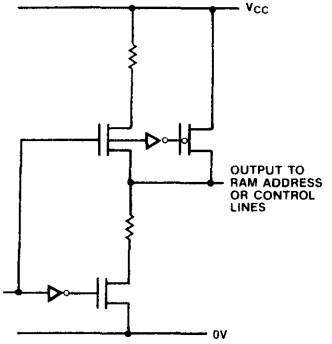


Figure 6b. Simplified Output Driver Schematic

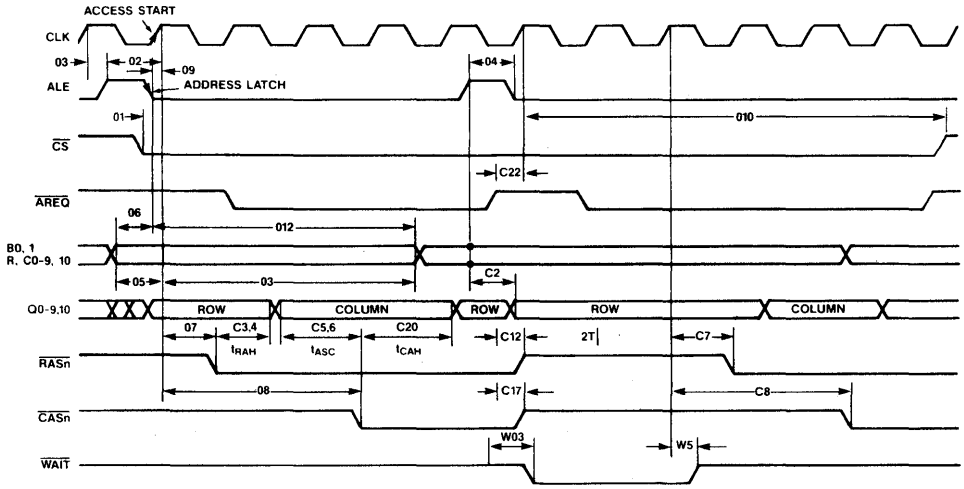


AC Testing inputs are driven at 3.0V for a logic "1" and 0.0V for a logic "0". Timing measurements are made at 2.4V for a logic "1" and 0.8V for a logic "0" at the outputs.

Maximum Propagation Delay Change vs Load Capacitance

$\overline{RAS}$ = 1ns/14pF (between 50pF . . . 250pF)
$\overline{CAS}$ = 1ns/8 pF (between 50pF . . . 250pF)
Q = 1ns/20pF (between 150pF . . . 500pF)

Figure 7. Mode 0 Interleave



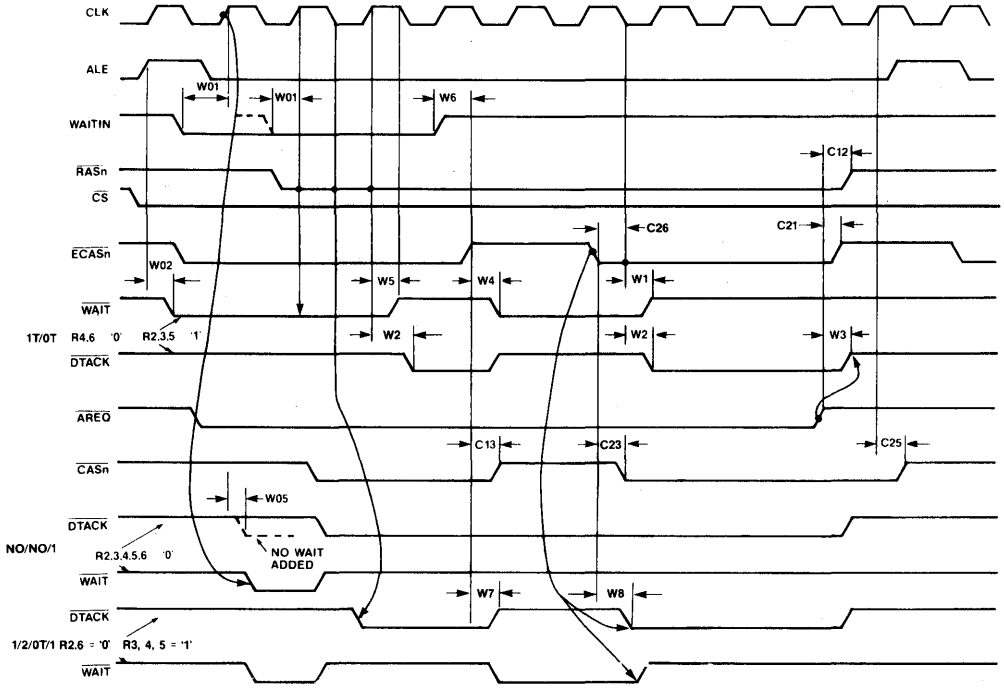
No.	Parameter	Min	Max
01	$\overline{CS}$ Low to CLK Rising Edge	5	
02	ALE High to CLK Rising Edge	5	1T**
03	ALE Negated from CLK High	0	
04	ALE Pulse Width	10	
05	Address Set-up to CLK Rising Edge not using the On-Chip Address Latch	20	
06	Address Set-up to ALE Falling Edge using the On-Chip Address Latch	2	
07	CLK Rising Edge to $\overline{RAS}$ Low	12	33
08	CLK Rising Edge to $\overline{CAS}$ Low (non-delayed access)		
a	t_{RAH} = 15ns, t_{ASC} = 0ns	45	85
b	t_{RAH} = 15ns, t_{ASC} = 10ns	55	95
c	t_{RAH} = 25ns, t_{ASC} = 0ns	55	95
d	t_{RAH} = 25ns, t_{ASC} = 10ns	65	105
010	$\overline{CS}$ Low After Access Start	*	
012	Address Hold Time from ALE falling edge using the On-Chip Address Latch	8	

* $\overline{CS}$ must be asserted until $\overline{AREQ}$ terminates the access (mode 0 only)

** 02_{MAX} = ½T if Mode 0 and WAIT output programmed

No.	Parameter	Min	Max
C3	Row Address Hold Time, t_{RAH} = 15ns	15	
C4	Row Address Hold Time, t_{RAH} = 25ns	25	
C5	Column Address Set-up Time t_{ASC} = 0ns	0	
C6	Column Address Set-up Time t_{ASC} = 10ns	10	
C7	CLK Rising Edge to $\overline{RAS}$ active after delayed access	12	33
C8	CLK Rising Edge to $\overline{CAS}$ active after delayed access		
a	t_{RAH} = 15ns, t_{ASC} = 0ns	45	85
b	t_{RAH} = 15ns, t_{ASC} = 10ns	55	95
c	t_{RAH} = 25ns, t_{ASC} = 0ns	55	95
d	t_{RAH} = 25ns, t_{ASC} = 10ns	65	105
C12	$\overline{AREQ}$ High to $\overline{RAS}$ High	12	35
C17	$\overline{AREQ}$ High to $\overline{CASn}$ High	12	40
C20	Column Address Hold Time in Interleave	35	
C22	$\overline{AREQ}$ High to CLK Rising Edge to recognized as 1T of $\overline{RAS}$ precharge	15	1T
W03	$\overline{CS}$ Low to $\overline{WAIT}$ Low		25
W5	CLK Rising Edge to $\overline{WAIT}$ High		30

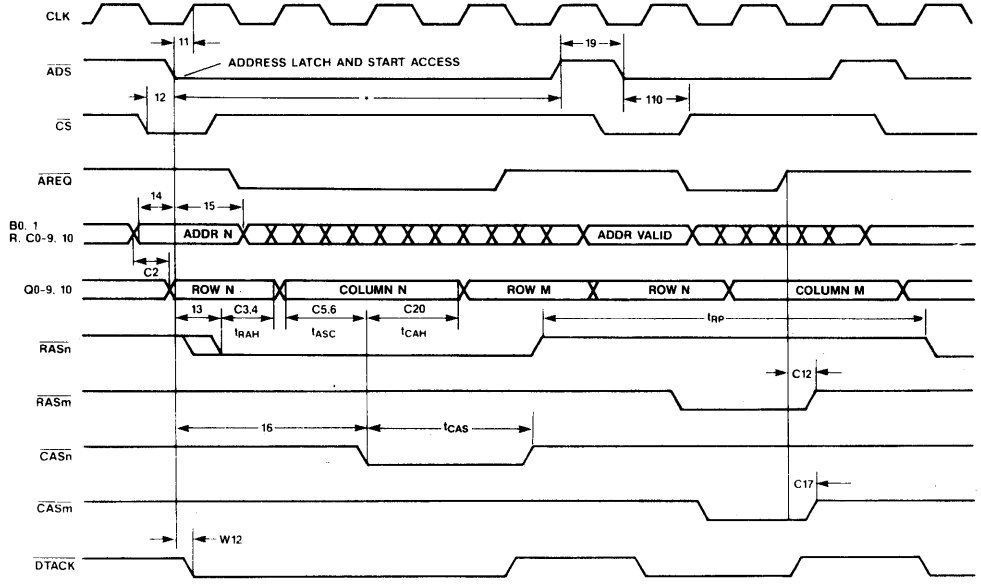
Figure 8. Mode 0, Wait State, Non-Interleave



No.	Parameter	Min	Max
C12	$\overline{AREQ}$ High to $\overline{RAS}$ High	12	35
C13a	$\overline{ECASn}$ High to $\overline{CASn}$ High	7	25
C13b	$\overline{ECASn}$ Low to $\overline{CASn}$ Low	7	25
C21	$\overline{AREQ}$ Rising Edge to $\overline{ECAS}$ Rising Edge in order not to start a Wait State	20	
C25	CLK Rising Edge to $\overline{CASn}$ High if $\overline{ECASn}$ low at AREQ Rising Edge (if Delay Programmed by ECAS0)	12	40
C26a	$\overline{ECAS}$ Asserted (setup time) to CLK Rising Edge	20	
C26b	$\overline{ECAS}$ Asserted (setup time) to CLK Falling Edge	20	

No.	Parameter	Min	Max
W01	$\overline{WAITIN}$ Low to CLK Rising Edge to Add Wait State (s) if no Wait State is programmed	5	
W02	ALE Rising Edge to $\overline{WAIT}$ Low ($\overline{CS}$ must be Low)		35
W1	CLK to $\overline{WAIT}$ High		30
W2	CLK to $\overline{DTACK}$ Low	12	33
W3	$\overline{AREQ}$ Rising Edge to $\overline{DTACK}$ High	5	25
W4	$\overline{ECAS}$ Rising Edge to $\overline{WAIT}$ Low		30
W5	CLK Rising Edge to $\overline{WAIT}$ High		30
W05	CLK High to $\overline{DTACK}$ Low 0T Programmed	12	35
W6	$\overline{WAITIN}$ Low to $\overline{ECAS}$ Rising Edge to Add Wait State(s)	12	
W7	$\overline{ECAS}$ High to $\overline{DTACK}$ High during Burst Access	6	35
W8	$\overline{ECAS}$ low to $\overline{DTACK}$ Low during Burst Access (0T programmed)	6	35

Figure 9. Mode 1, Interleave, Address Latch

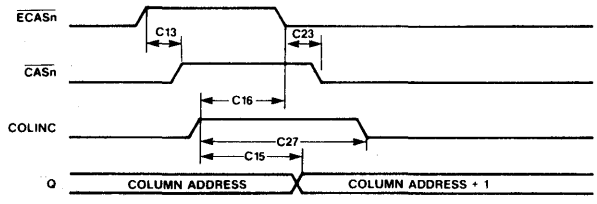


* 11a AND 11b MAY BE IGNORED IF 0T IS PROGRAMMED AND WAITIN IS NEGATED.

No.	Parameter	Min	Max
C1	R input to Q output while ALE is high	15	40
C2	Address to Q output	15	40
C3	Row Address Hold Time, t_{RAH} = 15ns	15	
C4	Row Address Hold Time, t_{RAH} = 25ns	25	
C5	Column Address Set-up Time t_{ASC} = 0ns	0	
C6	Column Address Set-up Time t_{ASC} = 10ns	10	
C12	$\overline{AREQ}$ High to $\overline{RAS}$ High	12	35
C17	$\overline{AREQ}$ High to $\overline{CAS}$ High	12	40
C20	Column Address Hold Time in Interleave	35	
W12	$\overline{ADS}$ Low to $\overline{DTACK}$ Low 0T from $\overline{RAS}$ Programmed R2, 3 = '0', R7 = '1'	14	35

No.	Parameter	Min	Max
11a	1T programmed or 0T programmed and $\overline{WAITIN}$ asserted	18	
11b	$\overline{ADS}$ Low to CLK, ½T or 1½T programmed	18	
12	$\overline{CS}$ to $\overline{ADS}$ Low Set-up Time	8	
13	$\overline{ADS}$ Falling Edge to $\overline{RAS}$ Low during an Access	10	30
14	Address Set-up to $\overline{ADS}$ Falling Edge	10	
15	Address Hold after $\overline{ADS}$ Falling Edge using the On-Chip Address Latch	8	
16	$\overline{ADS}$ Low to $\overline{CAS}$ Low C9 = '0' (not delayed access)		
a	t_{RAH} = 15ns, t_{ASC} = 0ns	45	85
b	t_{RAH} = 15ns, t_{ASC} = 10ns	55	95
c	t_{RAH} = 25ns, t_{ASC} = 0ns	55	95
d	t_{RAH} = 25ns, t_{ASC} = 10ns	60	105
19	$\overline{ADS}$ High Pulse Width	10	
110	$\overline{CS}$ Low After Access Start	20	

Figure 10. Burst Access — Page Mode

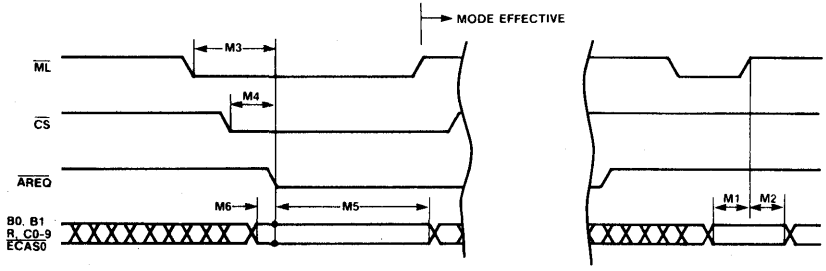


No.	Parameter	Min	Max
C13	$\overline{ECASn}$ High to $\overline{CASn}$ High	7	25
C15	COLINC Rising Edge to Column Address Output	22	40

No.	Parameter	Min	Max
C16	COLINC High Set-up to $\overline{ECASn}$ Low	20	
C23	$\overline{ECASn}$ Low to $\overline{CAS}$ Low	7	25
C27	COLINC Pulse Width	20	

Figure 11a. Mode Load
Load Mode Register with Fake Access

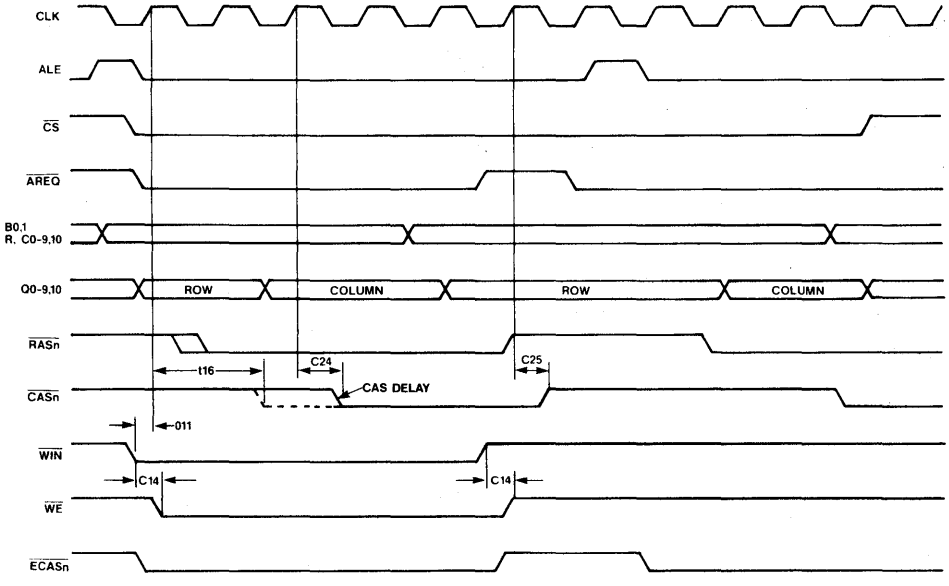
Figure 11b. Mode Load
Load Mode Register with $\overline{ML}$



No.	Parameter	Min	Max
M1	Mode Address Set-up Time	6	
M2	Mode Address Hold Time	5	
M3	$\overline{ML}$ asserted to $\overline{AREQ}$ asserted	10	

No.	Parameter	Min	Max
M4	$\overline{CS}$ asserted to $\overline{AREQ}$ asserted	5	
M5	Mode Address Hold Time from $\overline{AREQ}$ Low	10	
M6	Mode Address Set-up Time to $\overline{AREQ}$ Low	5	

Figure 12. Non-Interleave — Delay $\overline{CAS}$



No.	Parameter	Min	Max
011	$\overline{WIN}$ low to CLK Rising Edge to delay $\overline{CAS}$ (C9 = '1')	0	
C14	$\overline{WIN}$ to $\overline{WE}$	15	40
C24	CLK Rising Edge to $\overline{CAS}$ Low if delayed by $\overline{WIN}$	10	32
C25	CLK Rising Edge to $\overline{CASn}$ High if $\overline{ECASn}$ Low at $\overline{AREQ}$ (if delay programmed by $\overline{ECAS0}$)	12	40

No.	Parameter	Min	Max
C18	CLK High	15	
C18a	CLK Low	15	
C19	CLK Period	40	
C28	RFCLK High	15	
C28a	RFCLK Low	15	
C29	RFCLK Period	40	
C30	$\overline{ADS}$ Hold Time for RFCLK Rising Edge	20	
C31	$\overline{ADS}$ Setup Time for RFCLK Rising Edge	5	

Figure 13. CLK, RFCLK, $\overline{ADS}$ Timing

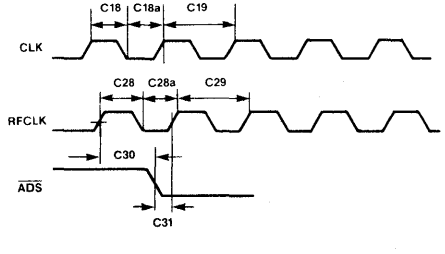
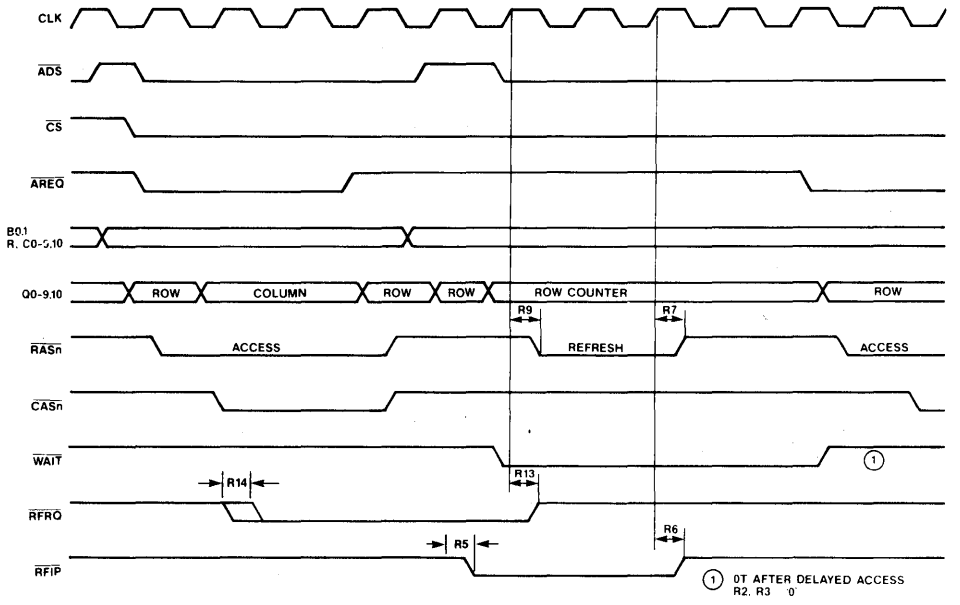
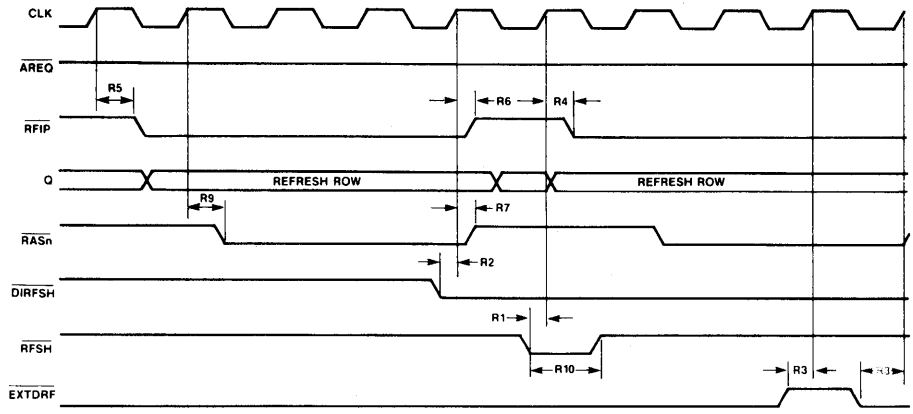


Figure 14. Internal Refresh — Interleave Access



No.	Parameter	Min	Max
R5	CLK High to $\overline{\text{RFIP}}$ Low		35
R6	CLK Rising Edge to $\overline{\text{RFIP}}$ High		35
R7	CLK Rising Edge to Refresh $\overline{\text{RAS}}$ Ending	10	33
R9	CLK Rising Edge to Refresh $\overline{\text{RAS}}$ Starting	10	33
R13	CLK Rising Edge to $\overline{\text{RFRQ}}$ High		40
R14	CLK Rising Edge $\overline{\text{RFRQ}}$ Low		40

Figure 15. Refresh and Extended Refresh



No.	Parameter	Min	Max
R1	$\overline{RFSH}$ Low Set-up to CLK Rising Edge	10	
R2	DISRFSH Low Set-up to CLK Rising Edge	10	
R3	EXTDRF Set-up to CLK Rising Edge	10	
R5	CLK Rising Edge to $\overline{RFIP}$ Low		35

No.	Parameter	Min	Max
R6	CLK Rising Edge to $\overline{RFIP}$ High		35
R7	CLK Rising Edge to Refresh $\overline{RAS}$ Ending	10	33
R9	CLK Rising Edge to Refresh $\overline{RAS}$ Starting	10	33
R10	$\overline{RFSH}$ Low Pulse Width	18	

Figure 16. Staggered Refresh

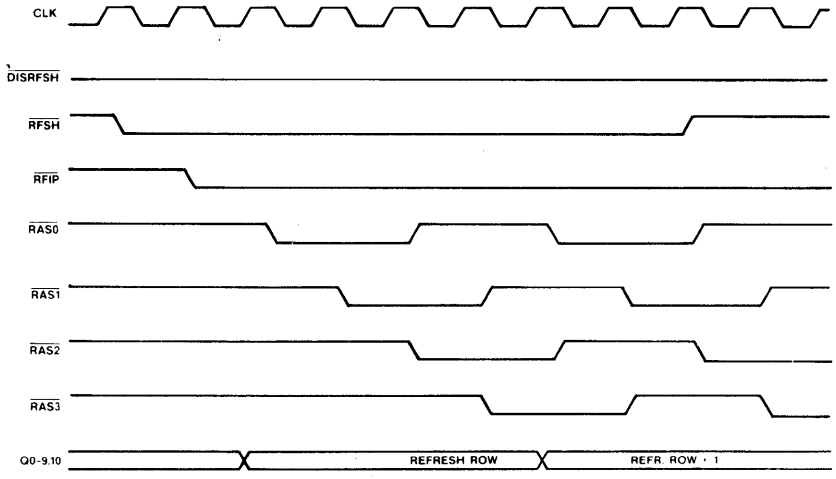
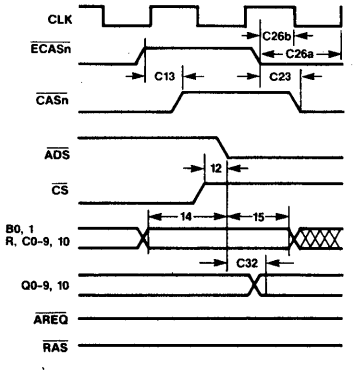


Figure 17. Random Page Mode Access



No.	Parameter	Min	Max
C32	$\overline{ADS}$ Asserted to Column Address Valid		35

NOTES ON TIMING CHARACTERISTICS

This section provides notes on timing characteristics for the following operations:

- Interleaving (Figures 7, 9 and 14)
- Two consecutive accesses to the same bank
- Refresh (Figures 14, 15 and 16)
- Wait States (Figure 8)

Interleaving

Relevant Mode Bits

R8	Interleave/non-interleave mode
C4, 5, 6	Select Interleave 2, 4, 5, or 7
B0	Address latch mode
B1	Access Modes
C7	Column Address Setup Time
C8	Row Address Hold Time
R0, 1	RAS Precharge Time

External Signal Inputs

$\overline{CS}$ — This input enables the access cycle.
Mode 0: It must be low for t_{01} before the rising edge of CLK. $\overline{CS}$ must stay low until $\overline{AREQ}$ goes high.
Mode 1: It must be low t_{12} before the falling edge of $\overline{ADS}$.

$\overline{ADS}$ — Mode 1: This input latches the address during asynchronous accesses. The falling edge must occur t_{11} before the rising edge of CLK. It may go high after $\overline{AREQ}$ was low for one CLK period. The address of the R, C and B inputs is latched at the falling edge of $\overline{ADS}$, if bit B0 in the Mode Register is '0'. While $\overline{ADS}$ is high, the row address latches are transparent to the input. The column address is not transparent.

ALE — Mode 0: This input latches the address during synchronous accesses. The rising edge must occur t_{02} before the rising edge of the next CLK input which starts an access. This is also true if the on-chip address latch is programmed in fall-through mode (bit B0 in the Mode Register is '1').

$\overline{AREQ}$ — This input ends the active time of $\overline{RAS}$ and $\overline{CAS}$. It may go low with $\overline{ADS}$ or some time later. $\overline{AREQ}$ has to be high t_{C22} before the rising edge of CLK in order to be recognized as 1T of precharge time.

$\overline{RASn}$ and $\overline{CASn}$ go high at the rising edge of $\overline{AREQ}$, independently of $\overline{ADS}$. Example: If $\overline{RAS3}$ followed by $\overline{RAS1}$ has been invoked, $\overline{RAS3}$ goes high with the first rising edge of $\overline{AREQ}$ and $\overline{RAS1}$ with the second.

If $\overline{ECAS}$ is set "1" then $\overline{CAS}$ goes high with the rising edge of CLK.

$\overline{RAS}$ Precharge time: If two consecutive access cycles address the same bank, i.e. the two least significant bits do not change, the precharge time t_{RP} is met by invoking Wait States.

$\overline{ECASn}$ — $\overline{ECASn}$ must be toggled to invoke a burst access while $\overline{RASn}$ is low.

$\overline{CAS}$ precharge time: The $\overline{CAS}$ precharge time during burst access must be controlled by the $\overline{ECAS}$ inputs. KS84C21/22 do not monitor the duration of $\overline{CAS}$.

R, C, B0, B1 — Mode 0: Address inputs must be stable t_{05} before CLK goes high if the address latches are fall through, and t_{06} if the address bits are latched. The address hold time is t_{03} or t_{12}.

Mode 1: Address inputs must be stable for a setup time of t_{14a} and t_{14b} before $\overline{ADS}$ goes low. The address hold time is t_{15a} and t_{15b} for latched and unlatched address bits.

Note: To meet the address hold time requirements, the KS84C21/22 guarantee that the column address is turned on for 35ns. If an access is initiated before the column address is turned on, the column address may change, since the address latches are transparent while ADS or ALE is high.

***External Signal Inputs** (Continued)*

B0, B1 — These two inputs should be connected to the two least significant address bits. B0 and B1 select one of the memory banks, depending upon the setting of bits C4, C5 and C6 in the Mode Register. Set-up and hold times are as described for the address inputs.

Signal Outputs

Q-Row — The Q outputs are the multiplexed address outputs. The row address is on the Q-outputs after the propagation delay time t_{C2}. The row address appears after a Column Address Hold time of 35ns minimum (interleave mode only).

$\overline{\text{RASn}}$ — The row address is guaranteed to be stable when $\overline{\text{RAS}}$ goes low. $\overline{\text{RASn}}$ stays low as long as $\overline{\text{AREQ}}$ is low and then stays high for the programmed number of CLK cycles. If required, Wait States are requested by the output $\overline{\text{WAIT}}$ or $\overline{\text{DTACK}}$.

$\overline{\text{CASn}}$ — This output goes low after t_{16}, guaranteeing the programmed Column Address Set-up time of 0ns or 10ns and the Row Address Hold time of 15ns or 25ns.

Q-Coln — After the Row Address Hold time has elapsed, the column address is multiplexed to the Q outputs. After the Column Address Hold time of min. 35ns, the row address will again be on the output (interleave mode only).

$\overline{\text{WE/RFRQ}}$ — This output signal is asserted when an internal or external refresh is requested. In interleave mode, the $\overline{\text{WE}}$ input to the DRAMs must be controlled by external logic.

Two Consecutive Accesses to the Same Bank

External Signal Inputs

$\overline{\text{AREQ}}$ — $\overline{\text{AREQ}}$ must go high to end the access in progress, before a pending access can be executed.

$\overline{\text{ADS}}$/ALE — An access may be started while $\overline{\text{AREQ}}$ is high or low. This means that $\overline{\text{ADS}}$ or ALE may go low while $\overline{\text{CAS}}$ is active.

Signal Outputs

$\overline{\text{WAIT}}$ or $\overline{\text{DTACK}}$ — This output is asserted when the same bank is accessed in two consecutive cycles, and/or the $\overline{\text{RASn}}$ precharge time for the current access is less than the programmed precharge time. The $\overline{\text{WAIT}}$ output if programmed, is asserted immediately when the KS84C21/C22 detects that the bank did not change and the DRAM was not precharged.

$\overline{\text{RASn}}$ — These outputs go high with the rising edge of $\overline{\text{AREQ}}$, and remain high for the number of CLK cycles programmed by R0 and R1 in the Mode Register. After the precharge time has elapsed, a pending access is executed on the rising edge of the CLK that ended the precharge time. These conditions are true for both Mode 0 and Mode 1.

Refresh

Relevant Mode Bits

R0, R1 — $\overline{\text{RAS}}$ low time during refresh and $\overline{\text{RAS}}$ precharge time.
R9 — Staggered refresh
C0-3 — Refresh clock divider
C4-6 — Select 0, 2, 4 is error scrubbing during refresh

External Signal Inputs

$\overline{\text{ECAS0}}$ — If $\overline{\text{ECAS0}}$ is set low in the Mode Register, the output $\overline{\text{WE/RFRQ}}$ becomes $\overline{\text{WE}}$. If $\overline{\text{ECAS0}}$ is high at this time, $\overline{\text{WE/RFRQ}}$ will function as refresh request. However, in interleave mode, this output is always $\overline{\text{RFRQ}}$.

***External Signal Inputs** (Continued)*

$\overline{\text{DISRFSH}}$	When high, this signal enables internal refresh, and when low, externally controlled refresh. External refresh can also be invoked by the $\overline{\text{RFSH}}$ input.
$\overline{\text{RFSH}}$	Must stay high for internally controlled refresh cycles. If $\overline{\text{DISRFSH}}$ is low, the $\overline{\text{RFSH}}$ input controls the number of refresh cycles performed, depending on how long it stays low. One refresh cycle is performed if $\overline{\text{RFSH}}$ is low for a minimum of one CLK period, and then goes high t_{R1} before the rising edge of the CLK input that ends the refresh operation. The Refresh Counter can be cleared with $\overline{\text{DISRFSH}}$ high and $\overline{\text{RFSH}}$ low with the set-up time t_{21} to CLK rising edge.
COLINC/ EXTDRF	If error scrubbing has been chosen and this input goes high while $\overline{\text{RAS}}$ is low, the refresh cycle in progress is extended to allow a read-modify-write cycle for error correction. $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ remain low until the rising edge of the next CLK input after EXTDRF has gone low again.

Signal Outputs

$\overline{\text{RFIP}}$	This signal goes low one CLK period before $\overline{\text{RAS}}$ goes low, and goes high on the rising edge of the CLK that ends the $\overline{\text{RAS}}$ active cycle.
$\overline{\text{WAIT}}$/$\overline{\text{DTACK}}$	If an access is requested during the refresh period, this access is deferred by inserting Wait States until refresh is complete.
$\overline{\text{WE}}$ or $\overline{\text{RFRQ}}$	This output becomes $\overline{\text{RFRQ}}$ in interleave mode. If $\overline{\text{RFRQ}}$ programmed to do so by $\overline{\text{ECAS0}}$, it becomes $\overline{\text{RFRQ}}$ in non-interleave mode. $\overline{\text{RFRQ}}$ goes low when an internal refresh request occurs, and goes high when the refresh $\overline{\text{RAS}}$ is asserted. $\overline{\text{RFRQ}}$ is activated regardless of internally or externally controlled refresh.
$\overline{\text{RASn}}$	This signal goes low after the precharge time of the access in progress, to start the refresh operation. It is toggled high and low for the number of CLK cycles programmed by R0 and R1 in the Mode Register. All $\overline{\text{RAS}}$ inputs go low at the same time, or are staggered at one CLK intervals (Figure 16) if a staggered refresh is programmed by Mode bit R9. The refresh counter (controlled either internally or externally) is incremented at every refresh, on the rising edge of $\overline{\text{RAS3}}$.

Wait States

Relevant Mode Bits

R2, R3	Wait during non-burst access
R4, R5	Add Wait State(s) to the current access if $\overline{\text{WAITIN}}$ is low.
R7	Select $\overline{\text{WAIT}}$ or $\overline{\text{DTACK}}$.

External Signal Inputs

ALE	Mode 0: $\overline{\text{WAIT}}$ goes low after the rising edge of ALE, if $\overline{\text{CS}}$ is low. If $\overline{\text{CS}}$ is high when ALE goes high, then the $\overline{\text{WAIT}}$ output will not be asserted until $\overline{\text{CS}}$ enables the access.
$\overline{\text{ADS}}$	Mode 1: Wait State starts if an access is initiated by $\overline{\text{ADS}}$ going low, provided that $\overline{\text{CS}}$ is low at set up time t_{12}.
$\overline{\text{AREQ}}$	If this input goes high, $\overline{\text{DTACK}}$ goes high after a maximum interval of t_{W3}.
$\overline{\text{ECASn}}$	During a non-burst access, $\overline{\text{ECAS}}$ inputs are normally low, unless $\overline{\text{CASn}}$ is delayed from going low. During burst access, the rising edge of $\overline{\text{ECASn}}$ starts a Wait State while $\overline{\text{AREQ}}$ is low. The Wait State is terminated as programmed by R4 and R5 in the Mode Register. $\overline{\text{ECASn}}$ must stay low t_{C21} after $\overline{\text{AREQ}}$ goes high. This ensures that no further Wait State is inserted.

***External Signal Inputs** (Continued)*

$\overline{WAITIN}$ Keeping this signal low allows Wait States to be inserted at particular external events, such as read instructions, or into a portion of memory that requires additional Wait States. $\overline{WAITIN}$ can be deasserted one CLK period before $\overline{WAIT}$ ends and $\overline{DTACK}$ starts. The active time of $\overline{WAIT}$ or $\overline{DTACK}$ is prolonged by one or two CLK cycles. $\overline{WAITIN}$ must be low for a setup time of t_{W01} in Mode 0, and t_{W11} in Mode 1, and must stay low for a minimum of one CLK period before the Wait State ends.

Signal Outputs

$\overline{WAIT}/\overline{DTACK}$ This output is either $\overline{WAIT}$ or $\overline{DTACK}$, depending on the setting of R7 in the Mode Register. $\overline{WAIT}$ goes low and $\overline{DTACK}$ stays high for the programmed number of Wait States. Wait States are inserted if necessary to meet the $\overline{RAS}$ precharge time, or to delay access.

There is a precharge counter for every bank. If the $\overline{RAS}$ precharge time has not elapsed at the expected number of CLK cycles, $\overline{WAIT}$ output goes low, or $\overline{DTACK}$ stays high, to instruct the CPU to insert Wait States until the precharge time has elapsed.

Wait During Non-Burst Access

The first access of any memory cycle is always a non-burst access.

$\overline{WAIT}$ Mode 0: $\overline{WAIT}$ goes low after t_{W02} and stays low for the programmed number of clock periods after $\overline{RAS}$ goes low. $\overline{CS}$ must meet the set-up time before the rising edge of CLK. $\overline{WAIT}$ is delayed from going low until $\overline{CS}$ goes low. It stays high if zero Wait states are programmed. If $\overline{WAITIN}$ goes low at t_{W01} before the rising edge of CLK, one or two extra Wait States are inserted, depending upon the setting of R6 in the Mode Register.

Mode 1: $\overline{WAIT}$ goes low after the '$\overline{CS}$ set up time to $\overline{ADS}$ low' of t_{W13}, and stays low for the programmed number of Wait States after $\overline{RAS}$ goes low. It stays high if zero Wait States are programmed. If $\overline{WAITIN}$ goes low t_{W11} before the falling edge of $\overline{ADS}$, one or two extra Wait States are inserted. $\overline{WAIT}$ does not go low when $\overline{ADS}$ goes low, if an access does not start (that is if $\overline{CS}$ is high.)

$\overline{DTACK}$ Mode 0: $\overline{DTACK}$ stays high for the programmed number of clock cycles of $\overline{RAS}$ goes low. It switches to high a maximum interval of t_{W3} after $\overline{AREQ}$ goes high. If $\overline{WAITIN}$ goes low t_{W01} before the rising edge of the CLK which starts the access, $\overline{DTACK}$ stays high for one or two extra CLK cycles, depending upon the setting of bit R6 in the Mode Register.

Mode 1: $\overline{DTACK}$ stays high for the programmed number of CLK cycles after $\overline{RAS}$ goes low. It goes high t_{W3} after $\overline{AREQ}$ goes high. If $\overline{WAITIN}$ goes low t_{W11} before the rising edge of CLK, $\overline{DTACK}$ will stay high for one or two additional CLK cycles, depending upon the setting of bit R6 in the Mode Register.

PACKAGE DIMENSIONS

The Samsung KS84CXX DRAM Controllers are available in two packages. The KS84C21 68-Pin PLCC package is shown in Figure 18, while the 84-Pin version is shown in Figure 19.

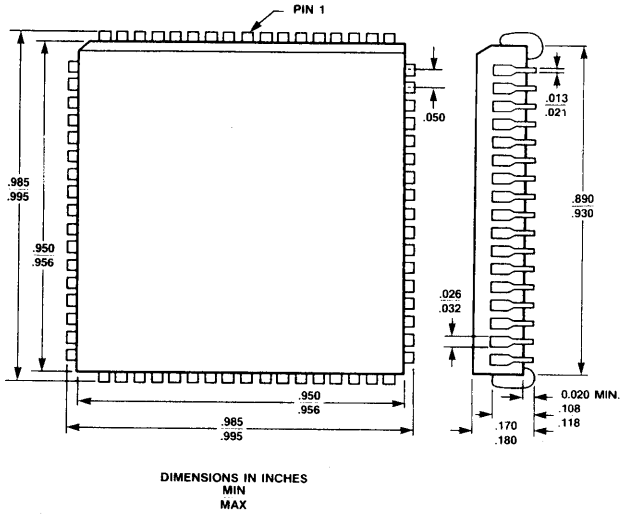


Figure 18. 68-Pin PLCC Package

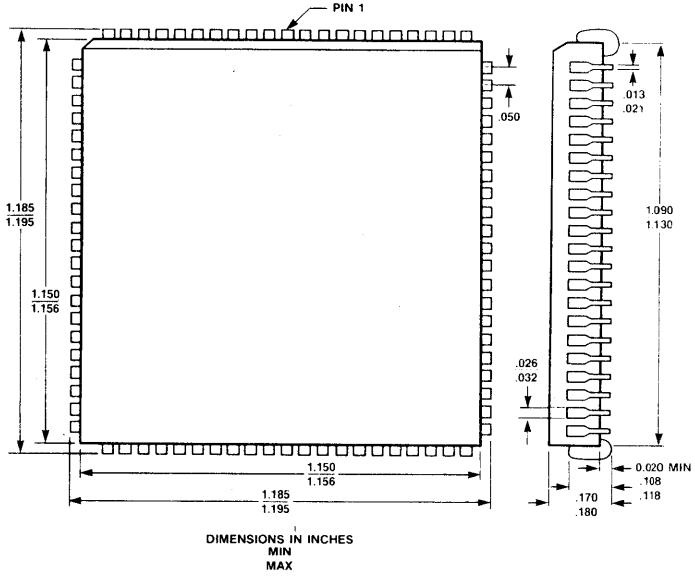
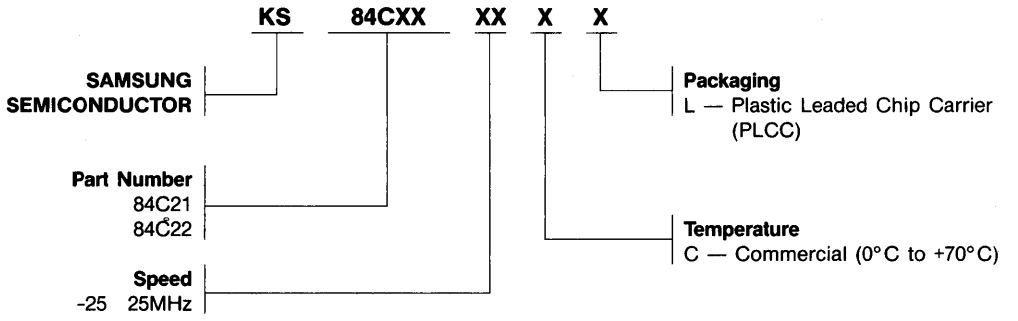


Figure 19. 84-Pin PLCC Package

ORDERING INFORMATION AND PRODUCT CODE



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FEATURES

- **33 MHz operation**
- **Easy interface to Motorola CPUs**
- **68040/68030 burst mode operation**
- **i486 burst mode operation**
- **Page, static column and nibble mode accesses**
- **Interleaved and non-interleaved accesses**
- **Synchronous and asynchronous operation**
- **Direct drive for 256K, 1Mbit and 4Mbit DRAMs**
- **High capacitive load, slew rate controlled drivers**
- **Page switch detection logic**
- **Built in precision delay line**
- **Four independent $\overline{RAS}$ and $\overline{CAS}$ outputs**
- **Programmable wait state generation logic**
- **Staggered and burst refresh**
- **Error scrubbing during refresh**
- **CMOS technology for low power consumption**
- **TTL compatible inputs**
- **68-pin PLCC package (KS84C31)**
- **84-pin PLCC package (KS84C32)**

PRODUCT OVERVIEW

The Samsung KS84C31 and KS84C32 are high performance dynamic RAM (DRAM) controllers. They simplify the interface between the microprocessor and the DRAM array, while also significantly reducing the required design time. The KS84C31 supports 256K and 1 MBit DRAMs, while the KS84C32 supports 256K, 1 Mbit and 4 MBit DRAMs.

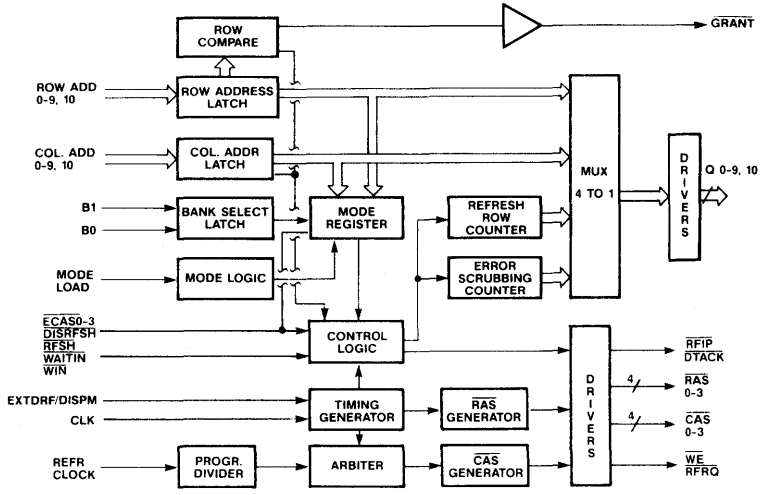
Both devices are functionally enhanced versions of their KS84C21/22 counterparts. They are available in either user programmable or mask programmed versions.

The MC68030™, MC68040™ and i486™ microprocessors are supported by special programming modes specifically tailored to their bus operations.

The user programmable version is an economical and flexible design solution. The 26-bit programmable Mode Register allows the selection of various options and features.

3

Figure 1. KS84C31/32 Block Diagram



™ MC68030, MC68040 are registered trademarks of Motorola, Inc.
™ i486 is a registered trademark of Intel, Inc.

A mask programmed version, useful for large production runs, offers the same Mode Register options however, the chip is programmed at the factory to the customer's specifications.

Both chips have a drive capability of 380 pf, sufficient to drive large memory arrays. Several hundred DRAMs may be driven if damping resistors are used to control ground bounce.

Figure 1 shows a block diagram of the chips.

INTRODUCTION

The KS84C31/32 are Dynamic Ram Controllers (hereafter referred to as DRCs) which are built upon the proven KS84C21/22 architecture with enhancements that improve memory access time and make it especially suitable for cache based memory systems. The DRC contains all of the advanced features of its predecessor including the capabilities of address latches, refresh counter, refresh clock, address multiplexor, precision delay line, refresh/access arbitration logic, high capacitive output drivers and on-chip damping resistors. A programmable system interface allows any manufacturer's CPU or cache controller to be interfaced to DRAM arrays up to 64 Mbytes in size.

The incorporation of on-chip page detection logic enables the DRC to support random accesses within a page for use with page and static column mode DRAMs. A 2-bit wrap around column counter may be used during burst accesses. On-chip $\overline{RAS}$ timeout circuitry enables the DRC to maintain an active $\overline{RAS}$ signal while EPROM or I/O is referenced, greatly improving system performance in embedded control applications and during data transfers between memory and I/O.

The MC68030, MC68040 and i486 burst cache fill accesses are supported. The special 68030 programming mode supports a burst memory access which doubles the 68030's cache hit ratio when compared against memory controllers that inhibit bursting.

The user programmable version of the DRC must be programmed after power up before the DRAM array is referenced. The DRC is programmed through the address bus.

There are two methods of programming the chip. The first method, Mode Load , is performed by first asserting the mode load ($\overline{ML}$) signal and presenting the programming selection on the row, column, bank and $\overline{ECAS}$ inputs. The programming selection is loaded into the Mode Register when $\overline{ML}$ is negated.

The second method, Fake Access, is performed by first asserting $\overline{ML}$, then performing a chip selected access. The programming value present on the address bus when $\overline{AREQ}$ is asserted is loaded into the Mode Register. The DRC then asserts the appropriate control signals to terminate the chip selected access.

If the production version of the target board will be using the mask programmed version of the part, laser programmed LCC versions are availible for prototyping from Samsung.

The DRC supports two access modes, synchronous (Access Mode 0) and asynchronous (Access Mode 1). To access the DRAM in Mode 0, the address latch enable (ALE) signal is asserted. $\overline{RAS}$ will be asserted on the next rising clock edge. To access the DRAM in Mode 1, the address strobe ($\overline{ADS}$) signal is asserted causing $\overline{RAS}$ to be asserted immediately.

The KS84C31/32 DRC offers four refreshing control modes:

1) internal automatic refreshing

2) internal automatic burst refreshing

3) externally controlled/burst refreshing

4) refresh request/acknowledge refreshing

When using internal automatic refreshing, the DRC's refresh request clock generates internal refresh requests. The DRC arbitrates between refresh requests and accesses. If an access is not currently in progress, the DRC will assert the refresh in progress signal ($\overline{RFIP}$). The refresh will start on the next rising clock edge. If an access had been in progress, the refresh would be delayed until the access is terminated.

Internal automatic burst refreshing is available when the DRC is programmed for use with page mode or static column DRAMs. After the refresh request clock has generated the fifth internal refresh request, the DRC will arbitrate between the refresh request and any accesses in progress. The DRC will assert $\overline{RFIP}$ and perform a five refresh burst.

To use externally controlled burst/refreshing, the internally requested refreshes are disabled by asserting the disable refresh ($\overline{DISFRSH}$) signal. A refresh can now be requested externally by asserting the refresh ($\overline{RFSH}$) signal. The DRC will arbitrate between accesses and external refresh requests, assert $\overline{RFIP}$ and perform the refresh.

When refresh request/acknowledge refreshing is used, the DRC broadcasts the internal refresh request by asserting the refresh request ($\overline{RFRQ}$) signal. External circuitry can determine when to enable the refresh by asserting $\overline{RFSH}$. When $\overline{RFSH}$ is asserted, the DRC will perform an externally controlled/burst refresh.

Figure 2a. Pin Configuration of the KS84C31 DRAM Controller

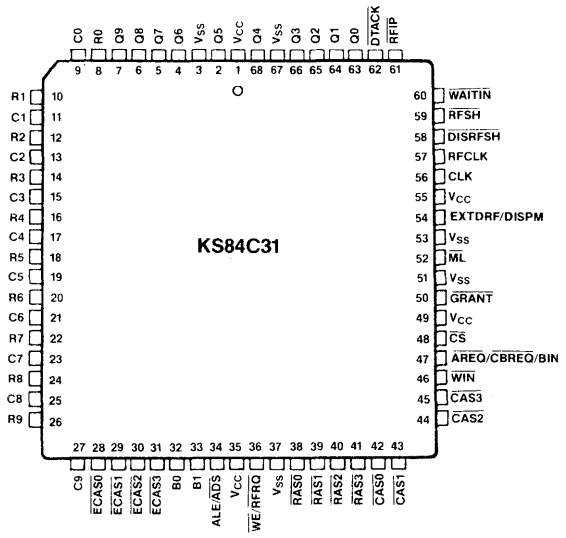
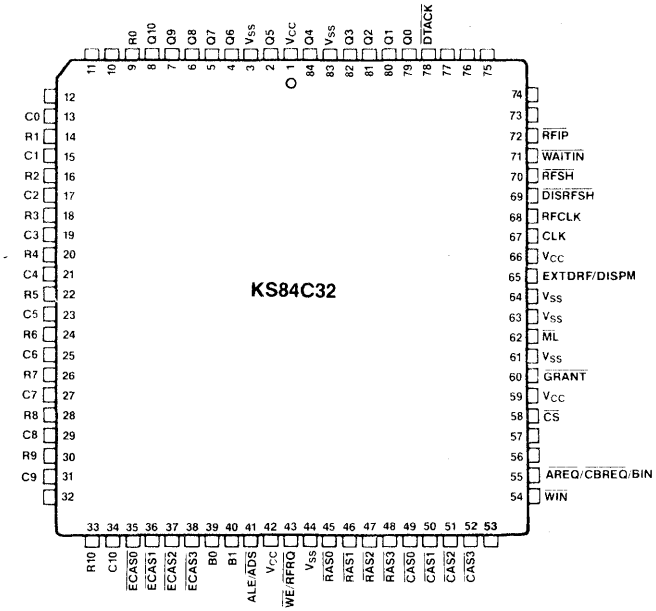


Figure 2b. Pin Configuration of the KS84C32 DRAM Controller



The DRC supports three types of refreshing

1) $\overline{RAS}$ Only

2) Staggered $\overline{RAS}$ Only

3) $\overline{RAS}$ Only with Error Scrubbing

In a $\overline{RAS}$ only refresh, all the $\overline{RAS}$ outputs will be asserted and negated at once. In a staggered $\overline{RAS}$ only refresh, the $\overline{RAS}$ outputs will be asserted one rising clock edge apart. Error scrubbing is the same as $\overline{RAS}$ only refresh except that a $\overline{CAS}$ and column address will be asserted during refresh, allowing the system to run the data through an error detection/correction chip and write it back to memory if an error has occured.

The DRC provides wait state support through its $\overline{DTACK}$ and $\overline{GRANT}$ output signals. Both signals may be used during Modes 0 and 1. $\overline{DTACK}$ is asserted by the on-chip wait state logic after a pre-programmed number of clock cycles to terminate the access. $\overline{GRANT}$ is asserted by the DRC to inform external circuitry that the DRC has begun an access. $\overline{DTACK}$ can be dynamically delayed by asserting the $\overline{WAITIN}$ input.

When a page miss is detected, the DRC will insert wait states during the access and precharge the memory.

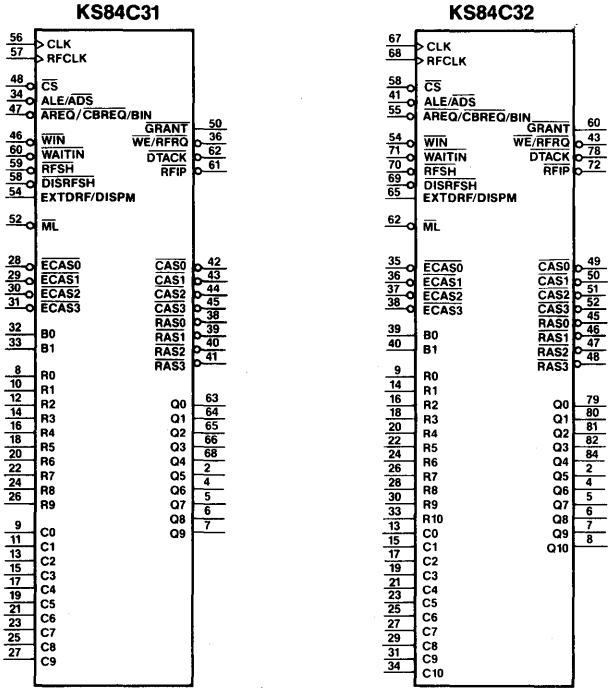
The DRC has address latches, used to latch the row, column, and bank address inputs. The latches may also be used in fall through mode, even when the DRC is programmed for page mode operation. (The page address is latched in a separate page register).

The $\overline{RAS}$ and $\overline{CAS}$ drivers can be configured to drive a 1, 2, 3 or 4 bank memory array up to 36 bits in width (32 data, 4 parity). The $\overline{CAS}$ enable ($\overline{ECAS}$) signals can then be used to selectively enable the $\overline{CAS}$ drivers for byte writing without requiring external logic. The DRC contains internal logic that ensures that the $\overline{CAS}$ outputs will not be asserted in case of a page miss, thus preventing spurious data writes to an incorrect page.

When configuring the DRC for more than one bank, memory interleaving can be used. The DRC can perform 2 or 4 way interleaving to eliminate wait states due to $\overline{RAS}$ precharge time.

The Dynamic Ram Controller is available in two packages. The KS84C31, shown in Figure 2a, is available in a 68 pin PLCC and supports 256K and 1 Mbit DRAMs. The KS84C32, shown in Figure 2b, is available in an 84 pin PLCC and supports 256K, 1 Mbit and 4 Mbit DRAMs. The logic symbols are shown in Figure 3.

Figure 3. Logic Symbol



Tables 1 and 2 show detailed pin allocations for the KS84C31 and KS84C32, respectively.

Table 1. KS84C31 Pin Allocations

Pin No.	Signal Abbrev.	Signal Name
1	V_{CC}	V_{CC}
2	Q5	Multiplexed Address 5
3	V_{SS}	V_{SS}
4	Q6	Multiplexed Address 6
5	Q7	Multiplexed Address 7
6	Q8	Multiplexed Address 8
7	Q9	Multiplexed Address 9
8	R0	Row Address 0
9	C0	Column Address 0
10	R1	Row Address 1
11	C1	Column Address 1
12	R2	Row Address 2
13	C2	Column Address 2
14	R3	Row Address 3
15	C3	Column Address 3
16	R4	Row Address 4
17	C4	Column Address 4
18	R5	Row Address 5
19	C5	Column Address 5
20	R6	Row Address 6
21	C6	Column Address 6
22	R7	Row Address 7
23	C7	Column Address 7
24	R8	Row Address 8
25	C8	Column Address 8
26	R9	Row Address 9
27	C9	Column Address 9
28	$\overline{ECAS0}$	Enable $\overline{CAS0}$
29	$\overline{ECAS1}$	Enable $\overline{CAS1}$
30	$\overline{ECAS2}$	Enable $\overline{CAS2}$
31	$\overline{ECAS3}$	Enable $\overline{CAS3}$
32	B0	Bank Select 0
33	B1	Bank Select 1
34	ALE/$\overline{ADS}$	Address Latch Enable/ Address Strobe
35	V_{CC}	V_{CC}
36	$\overline{RFRQ/WE}$	Refresh Request/Write Enable
37	V_{SS}	V_{SS}
38	$\overline{RAS0}$	Row Address Strobe 0
39	$\overline{RAS1}$	Row Address Strobe 1
40	$\overline{RAS2}$	Row Address Strobe 2
41	$\overline{RAS3}$	Row Address Strobe 3
42	$\overline{CAS0}$	Column Address Strobe 0
43	$\overline{CAS1}$	Column Address Strobe 1
44	$\overline{CAS2}$	Column Address Strobe 2
45	$\overline{CAS3}$	Column Address Strobe 3
46	$\overline{WIN}$	Write Enable Input
47	$\overline{AREQ}$	Access Request
	$\overline{CBREQ}$	Cache Burst Request
	BIN	Burst Inhibit
48	$\overline{CS}$	Chip Select
49	V_{CC}	V_{CC}
50	$\overline{GRANT}$	Access Grant
51	V_{SS}	V_{SS}
52	$\overline{ML}$	Mode Load
53	V_{SS}	V_{SS}
54	EXTDRF	Extend Refresh
	DISPM	Disable Page Mode
55	V_{CC}	V_{CC}
56	CLK	Clock
57	RFCLK	Refresh Clock
58	$\overline{DISRFSH}$	Disable Internal Refresh
59	$\overline{RFSH}$	External Refresh Request
60	$\overline{WAITIN}$	Add Wait State
61	$\overline{RFIP}$	Refresh in Progress
62	$\overline{DTACK}$	Data Transfer Acknowledge
63	Q0	Multiplexed Address 0
64	Q1	Multiplexed Address 1
65	Q2	Multiplexed Address 2
66	Q3	Multiplexed Address 3
67	V_{SS}	V_{SS}
68	Q4	Multiplexed Address 4

Table 2. KS84C32 Pin Allocations

Pin No.	Signal Abbrev.	Signal Name
1	V_{CC}	V_{CC}
2	Q5	Multiplexed Address 5
3	V_{SS}	V_{SS}
4	Q6	Multiplexed Address 6
5	Q7	Multiplexed Address 7
6	Q8	Multiplexed Address 8
7	Q9	Multiplexed Address 9
8	Q10	Multiplexed Address 10
9	R0	Row Address 0
10	—	N.C.
11	—	N.C.
12	—	N.C.
13	C0	Column Address 0
14	R1	Row Address 1
15	C1	Column Address 1
16	R2	Row Address 2
17	C2	Column Address 2
18	R3	Row Address 3
19	C3	Column Address 3
20	R4	Row Address 4
21	C4	Column Address 4
22	R5	Row Address 5
23	C5	Column Address 5
24	R6	Row Address 6
25	C6	Column Address 6
26	R7	Row Address 7
27	C7	Column Address 7
28	R8	Row Address 8
29	C8	Column Address 8
30	R9	Row Address 9
31	C9	Column Address 9
32	—	N.C.
33	R10	Row Address 10
34	C10	Column Address 10
35	$\overline{ECAS0}$	Enable $\overline{CAS0}$
36	$\overline{ECAS1}$	Enable $\overline{CAS1}$
37	$\overline{ECAS2}$	Enable $\overline{CAS2}$
38	$\overline{ECAS3}$	Enable $\overline{CAS3}$
39	B0	Bank Select 0
40	B1	Bank Select 1
41	ALE/$\overline{ADS}$	Address Latch Enable/ Address Strobe
42	V_{CC}	V_{CC}
43	$\overline{RFRQ/WE}$	Refresh Request/Write Enable
44	V_{SS}	V_{SS}
45	$\overline{RAS0}$	Row Address Strobe 0
46	$\overline{RAS1}$	Row Address Strobe 1
47	$\overline{RAS2}$	Row Address Strobe 2
48	$\overline{RAS3}$	Row Address Strobe 3
49	$\overline{CAS0}$	Column Address Strobe 0
50	$\overline{CAS1}$	Column Address Strobe 1
51	$\overline{CAS2}$	Column Address Strobe 2
52	$\overline{CAS3}$	Column Address Strobe 3
53	—	N.C.
54	$\overline{WIN}$	Write Enable Input
55	$\overline{AREQ}$	Access Request
	$\overline{CBREQ}$	Cache Burst Request
	BIN	Burst Inhibit
56	—	N.C.
57	—	N.C.
58	$\overline{CS}$	Chip Select
59	V_{CC}	V_{CC}
60	$\overline{GRANT}$	Access Grant
61	V_{SS}	V_{SS}
62	$\overline{ML}$	Mode Load
63	V_{SS}	V_{SS}
64	V_{SS}	V_{SS}
65	EXTDRF	Extend Refresh
	DISPM	Disable Page Mode
66	V_{CC}	V_{CC}
67	CLK	Clock
68	RFCLK	Refresh Clock
69	$\overline{DISRFSH}$	Disable Internal Refresh
70	$\overline{RFSH}$	External Refresh Request
71	$\overline{WAITIN}$	Add Wait State
72	$\overline{RFIP}$	Refresh in Progress
73	—	N.C.
74	—	N.C.
75	—	N.C.
76	—	N.C.
77	—	N.C.
78	$\overline{DTACK}$	Data Transfer Acknowledge
79	Q0	Multiplexed Address 0
80	Q1	Multiplexed Address 1
81	Q2	Multiplexed Address 2
82	Q3	Multiplexed Address 3
83	V_{SS}	V_{SS}
84	Q4	Multiplexed Address 4

Table 3. Interface Signal Descriptions

Symbol	Type	Descriptions
Access Signals		
$\overline{ADS}$ (ALE)	I	**Address Strobe (Address Latch Enable)**: This input latches row, column and bank addresses, and initiates the DRAM access. $\overline{ADS}$ (ALE) must be invoked for every non-burst access. $\overline{ADS}$ (ALE) need only be invoked for the opening cycle of a burst access when used with microprocessors that only assert $\overline{ADS}$ (ALE) during the opening cycle. In Access Mode 0, this input functions as Address Latch Enable (ALE). In Access Mode 1, this input functions as Address Strobe ($\overline{ADS}$).
$\overline{CS}$	I	**Chip Select**: The $\overline{CS}$ input must be active to enable a DRAM access. $\overline{CS}$ must enable every non-burst access. $\overline{CS}$ need only be invoked for the opening cycle of a burst access when used with microprocessors that only assert $\overline{ADS}$ (ALE) during the opening access.
$\overline{AREQ}$ ($\overline{CBREQ}$) (BIN)	I	**Access Request (Cache Burst Request) (Burst Inhibit)**: This input terminates an access. $\overline{AREQ}$: In Single Access Mode, this input functions as Access Request. It brings $\overline{RAS}$ and $\overline{CAS}$ high to terminate the access. In Page Access Mode, $\overline{AREQ}$ only brings $\overline{CAS}$ high. $\overline{CBREQ}$: In 68030 Burst Mode, this signal functions as Cache Burst Request. $\overline{CBREQ}$ is sampled on the rising edge of CLK that negates $\overline{DTACK}$. Directly compatible with the MC68030's $\overline{CBREQ}$ signal, it controls the termination of the DRC's burst access. It brings $\overline{RAS}$ and $\overline{CAS}$ high to terminate the burst when programmed for use with nibble mode DRAMs. When programmed for use with page and static column mode DRAMs, only $\overline{CAS}$ is brought high. BIN: When programmed for 68040 Burst Mode, this signal functions as Burst Inhibit. Burst Inhibit is sampled on the rising edge of CLK that negates $\overline{DTACK}$. BIN prevents the DRC from bursting if the CPU aborts the burst or is performing a single access. It brings $\overline{RAS}$ and $\overline{CAS}$ high to terminate the burst when programmed for use with nibble mode DRAMs. When programmed for use with page and static column mode DRAMs, only $\overline{CAS}$ is brought high.
$\overline{DTACK}$	O	**Data Transfer Acknowledge**: This output is asserted to terminate the CPU access. In Single Access Mode and Page Mode, it is negated when the access is terminated by $\overline{AREQ}$. In both burst modes, $\overline{DTACK}$ is negated on the first rising clock edge after it has been asserted.
$\overline{WAITIN}$	I	**Wait State Insert**: This input is used to dynamically add wait states during a bus cycle. If R6=0 during programming, $\overline{WAITIN}$ is used to add one wait state during the access. $\overline{WAITIN}$ is sampled once during the access, when $\overline{DTACK}$ is to be asserted by the DRC. $\overline{DTACK}$ will remain negated for one more rising CLK edge if $\overline{DTACK}$ is rising edge triggered or one more falling CLK edge if $\overline{DTACK}$ is falling edge trigered. $\overline{WAITIN}$ will not be sampled again, until the next access. If R6=1 during programming, $\overline{WAITIN}$ may be used to defer $\overline{DTACK}$ indefinitely. $\overline{WAITIN}$ is sampled at the access start. If $\overline{WAITIN}$ is inactive, the DRC will assert $\overline{DTACK}$ after the programmed number of CLK edges. If $\overline{WAITIN}$ was active, the $\overline{DTACK}$ CLK edge count is deferred. $\overline{WAITIN}$ will be continually sampled on the rising edge of CLK if $\overline{DTACK}$ is rising edge triggered or on the falling edge of CLK if $\overline{DTACK}$ is falling edge triggered. Once $\overline{WAITIN}$ is negated, the DRC will assert $\overline{DTACK}$ after the programmed number of CLK edges and will not sample $\overline{WAITIN}$ again until the next access.

Table 3. Interface Signal Descriptions (Continued)

Symbol	Type	Descriptions
Access Signals (Continued)		
$\overline{GRANT}$	O	**Access Grant**: This output is asserted only when $\overline{RAS}$ is asserted for a DRAM access. It is asserted at the beginning of an access to indicate that the access has begun. If an access is deferred due to a refresh cycle, page miss, or to satisfy $\overline{RAS}$ precharge time, $\overline{GRANT}$ will not be asserted until the access has begun. $\overline{GRANT}$ will remain asserted until the access $\overline{RAS}$ is negated.
Address, R/$\overline{W}$ and Programming Signals		
C0-9,10	I	**Column Address Inputs**: These address bits are connected to the CPU's address bus. When the DRC is programmed for use with page mode or static column DRAMs, they should be connected to the low order address bits.
R0-9,10	I	**Row Address Inputs**: Theses address bits are connected to the CPU's address bus. When the DRC is programmed for use with page or static column mode DRAMs, they should be connected to the higher order address bits.
B0, B1	I	**Bank Select**: These inputs select the memory bank to be addressed. Up to four banks are supported by the DRC.
$\overline{ECAS0\text{-}3}$	I	**Enable** $\overline{CAS0\text{-}3}$: These inputs are used to enable or disable individual $\overline{CAS}$ outputs when accessing bytes, words or doublewords. They can also be used to delay the falling edge of $\overline{CAS}$.
$\overline{WIN}$	I	**Write Enable Input**: This input controls the Write Enable ($\overline{WE}$) output. If programmed to do so, it also delays the falling edge of $\overline{CAS}$ by one rising CLK edge during page hits and one CLK period during burst accesses. It does not delay the falling edge of $\overline{CAS}$ in Single Access Mode or the opening cycle of a burst access that results in a page miss. When the leading edge of $\overline{CAS}$ is delayed by $\overline{WIN}$, one wait state is automatically added to the access cycle. $\overline{WIN}$ is sampled when a burst or page hit access starts in all operating modes and also on the rising edge of CLK that negates $\overline{DTACK}$ when the DRC is bursting.
$\overline{ML}$	I	**Mode Load**: This input strobes the row, column, bank and $\overline{ECAS0\text{-}3}$ inputs into the Mode Register.
DRAM Control Signals		
Q0-9,10	O	**Address Outputs**: These outputs are the multiplexed address bits (R0-10, C0-10). They access the memory for read, write and refresh operations. The output loading is rated at 380 pF.
$\overline{RAS0\text{-}3}$	O	**Row Address Strobe**: These output signals are used to strobe the row address into the DRAM.
$\overline{CAS0\text{-}3}$	O	**Column Address Strobe**:These output signals are used to strobe the column address into the DRAM.
$\overline{WE}$ ($\overline{RFRQ}$)	O	**Write Enable (Refresh Request)**: After power up and when the DRC is programmed for interleaved operation, this output functions as Refresh Request. When the DRC is not programmed for interleaved operation, this output may be programmed as Write Enable or Refresh Request. When programmed as $\overline{WE}$, this output is controlled by the $\overline{WIN}$ input. The output loading is rated at 500 pF. When programmed as $\overline{RFRQ}$, the DRC asserts this output whenever a refresh request has been generated by the internal refresh interval timer. $\overline{RFRQ}$ is negated when the refresh begins.

Table 3. Interface Signal Descriptions (Continued)

Symbol	Type	Descriptions
Refresh Control Signals		
EXTDRF (DISPM)	I	**Extend Refresh (Disable Page Mode)**: When the DRC is programmed to support error scrubbing, this pin is time multiplexed. During refresh, this input extends the refresh cycle to allow a read-modify-write cycle to be performed in a system with error scrubbing. During accesses, this pin is used to terminate $\overline{RAS}$ when the DRC is programmed for use with page mode DRAMs. When the DRC is not programmed to support error scrubbing, this pin only functions as Disable Page Mode and does not affect refresh cycles.
$\overline{DISRFSH}$	I	**Disable Internal Refresh**: This input prevents the DRC from performing internally requested refreshes. This signal could be asserted to prevent the DRC from performing refreshes during DMA transfers, while the CPU is executing time critical code or if refreshes are going to be controlled externally.
$\overline{RFIP}$	O	**Refresh In Progress**: This output indicates that a refresh cycle is in progress. $\overline{RFIP}$ is asserted one clock cycle prior to the start of a refresh cycle.
$\overline{RFSH}$	I	**External Refresh**: Refresh requests can be generated externally by asserting this input when $\overline{DISRFSH}$ is low.
Clock Inputs		
CLK	I	**Sytem Clock**: This input should be connected to the system bus clock. It is used for access arbitration and timing.
RFCLK	I	**Refresh Clock**: This input determines the interval between internally requested refreshes. Ideally, it should be a multiple of 2 MHz. It is divided internally, according to the value in the Mode Register, so that refresh requests are generated at 15 µs or 13 µs intervals.

ACCESS START and TERMINATION MODES

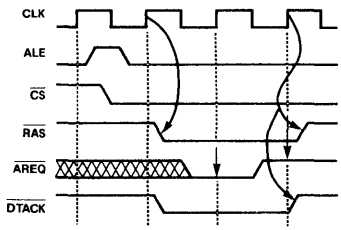
The KS84C31/32 supports both synchronous and asynchronous access modes. The user selects the mode best suited to the microprocessor by programming bit B1 of the Mode Register.

Mode 0 - Synchronous Access Start and Termination

Mode 0 is selected when B1 = 0 during programming. To initiate a Mode 0 access, ALE is pulsed high and a valid $\overline{CS}$ signal is asserted before the input clock's (CLK) rising edge. The access will start on the rising edge of CLK as shown in Figure 4, provided that the ALE and $\overline{CS}$ setup times were observed, the $\overline{RAS}$ precharge time was met and a refresh was not currently in progress. If the $\overline{RAS}$ precharge time was not met from the previous access or a refresh was in progress, the DRC will wait until these events have taken place before asserting $\overline{RAS}$ on the rising edge of CLK.

The DRC will begin sampling $\overline{AREQ}$ on the rising edge of CLK after $\overline{DTACK}$ is asserted. The access will continue until $\overline{AREQ}$ is negated.

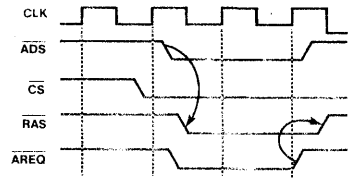
Figure 4. Synchronous Access Start and Termination



Mode 1- Asynchronous Access Start and Termination

Mode 1 is selected when B1 = 1 during programming. To initiate a Mode 1 access, $\overline{CS}$ is asserted, followed by $\overline{ADS}$. The access will start when $\overline{ADS}$ is asserted as shown in Figure 5, provided that the $\overline{RAS}$ precharge time was met and a refresh was not currently in progress. If the $\overline{RAS}$ precharge time was not met from the previous access or a refresh was in progress, the DRC will wait until these events have taken place before asserting $\overline{RAS}$ on the rising edge of CLK. The access will be terminated when $\overline{AREQ}$ is negated.

Figure 5. Asynchronous Access Start and Termination



OPERATING MODES

The KS84C31/32 may be programmed to operate in several different modes, depending on the CPU characteristics and type of DRAM used. The Single Access Mode is recommended for use in slower speed systems in which there is no advantage to be gained from a $\overline{CAS}$ only access and where the $\overline{RAS}$ precharge time is hidden between back to back accesses. For higher performance systems, Page Mode operation is provided and may be used with page or static column DRAMs. Two versions of burst mode operation, 68030 Burst Mode and 68040 Burst Mode are provided to support CPUs that are capable of performing burst accesses. Both burst modes may be used with nibble, page or static column DRAMs.

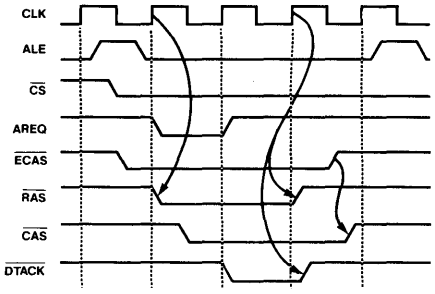
Interleaved Access Mode can provide a performance advantage when used in systems that support address pipelining. The user selects the operating mode best suited to the system's requirements by programming bits R8 and $\overline{ECAS1\text{-}3}$ in the Mode Load Register.

Single Access Mode

Single Access Mode is selected when R8, $\overline{ECAS1}$, $\overline{ECAS2}$, $\overline{ECAS3}$ =1, 0,0,0 during programming. The access is initiated by two signals, $\overline{ADS}$(ALE) and $\overline{CS}$, and is terminated by one signal, $\overline{AREQ}$. Both $\overline{RAS}$ and $\overline{DTACK}$ are negated when the access is terminated.

The user has the option of negating $\overline{CAS}$ when the access is terminated or up to one clock period later. If $\overline{ECAS0}$ = 0 during programming, $\overline{CAS}$ will be negated with $\overline{RAS}$ and $\overline{DTACK}$. If $\overline{ECAS0}$ = 1 during programming, $\overline{CAS}$ will remain asserted until the next rising CLK edge or the rising edge of $\overline{ECAS}$, whichever occurs first . This allows the DRAM to continue to drive the data bus while $\overline{RAS}$ is precharging. See Figure 6.

Figure 6. Single Access Mode with Synchronous Access Start and Extended $\overline{CAS}$



Page Mode Access

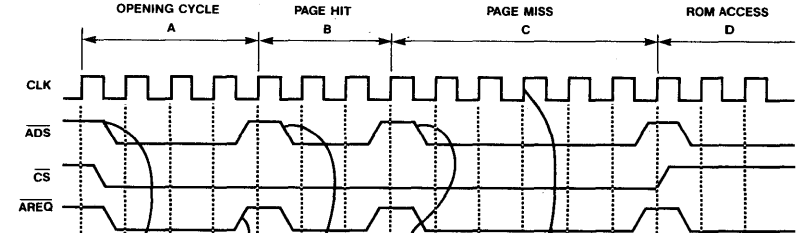
Page Mode is selected when R8, $\overline{ECAS1}$, $\overline{ECAS2}$, $\overline{ECAS3}$ =1, 0,1,0 during programming. Page Mode allows the CPU to access random columns within a page without having to pay the penalties associated with $\overline{RAS}$ access and precharge time. Both page and static column mode DRAMs may be used. It is very similar in operation to the Single Access Mode, with only two notable exceptions:

1) Only $\overline{CAS}$ and $\overline{DTACK}$ are negated when $\overline{AREQ}$ terminates the access.
2) The DRC maintains $\overline{RAS}$ low even when the CPU is not accessing DRAM.

On-chip page detection logic detects page hits and misses. The DRC's on-chip wait state logic delays the assertion of $\overline{DTACK}$ in case of a page miss to allow for $\overline{RAS}$ precharge and $\overline{RAS}$ access time. An external signal, $\overline{GRANT}$, is asserted to indicate to external circuitry when the access has begun.

Several Page Mode accesses are shown in Figure 7. Access A occurred after a refresh cycle. The access was not delayed due to $\overline{RAS}$ precharge since the CPU initiated the access after the $\overline{RAS}$ was already precharged. Access B is a page hit. Access C is a page miss. Access D is an access to a memory location other than DRAM.

Figure 7. Page Mode Accesses



When programmed for Page Mode operation ($\overline{ECAS2}$ = 1), the DRC maintains $\overline{RAS}$ and $\overline{GRANT}$ low for 5 internal refresh requests (75 µs). After the 5th internal refresh request, both signals will be negated when $\overline{AREQ}$ terminates the access. The DRC will then perform a 5 refresh burst.

Certain applications may require that, at certain times, the DRAM is precharged prior to an access start. Since it is impossible to ensure that a given access will result in a page hit, and if the penalty of a page miss is intolerable, DISPM may be used to negate $\overline{RAS}$ when an access is completed.

If DISPM is asserted when there is no access or refresh in progress, $\overline{RAS}$ is negated immediately. If DISPM is asserted during an access, $\overline{AREQ}$ will negate both $\overline{RAS}$ and $\overline{CAS}$ when the access is completed. The DRC will continue to function as though it were programmed for Single Access Mode operation as long as DISPM is asserted. After DISPM is negated, all pending refreshes (up to 5) will be performed in a burst refresh.

When the DRC is not programmed to support error scrubbing, DISPM has no effect on $\overline{RAS}$ during refreshes. When the DRC is programmed to support error scrubbing, DISPM is time multiplexed with EXTDRF. EXTDRF will cause the refresh $\overline{RAS}$ to be extended when it is sampled active on the rising edge of CLK that was programmed to negate $\overline{RAS}$.

Burst Mode Accesses

In order to support high performance CPUs that can perform up to 4 memory accesses in a single burst, the KS84C31/32 is capable of performing 4 accesses when provided with the starting address of the burst. The DRC supports two forms of burst mode operation. When programmed for 68040 Burst Mode, $\overline{CAS}$ is asserted on the falling edge of CLK and is negated on the rising edge of CLK. This mode should be used when the data is to be sampled on the rising edge of CLK such as with the MC68040 and i486 CPUs. To accomodate CPU's that sample data on the falling edge of CLK, such as the MC68030, 68030 Burst Mode should be used. In 68030 Burst Mode, $\overline{CAS}$ is asserted on the rising edge of CLK and is negated on the falling edge of CLK.

The user has the choice of using nibble, page or static column DRAMs in both burst modes. An on-chip address counter may be used while bursting, if desired. The 2-bit address counter wraps around to support CPU's that wrap around when filling their cache lines. The user can choose when to increment the address counter depending on whether page or static column DRAMs are used. The DRC's burst access can be terminated early if the CPU is performing a single access or aborts the burst.

When programmed for use with page or static column mode DRAMs ($\overline{ECAS2}$ = 1), the DRC maintains $\overline{RAS}$ and $\overline{GRANT}$ low for 5 internal refresh requests (75 µs). After the 5th internal refresh request, both signals will be negated when the access is completed. The DRC will then perform a 5 refresh burst.

If DISPM is asserted during an access, both $\overline{RAS}$ and $\overline{CAS}$ are negated when the access is completed. The DRC will continue to function as though it were programmed for use with nibble mode DRAMs ($\overline{ECAS2}$ = 0) as long as DISPM is asserted. After DISPM is negated, all pending refreshes (up to 5) will be performed in a burst refresh.

The on-chip address counter is enabled when the address latches are programmed to latch the address on the falling edge of $\overline{ADS}$(ALE). If the latches are transparent, the counter is disabled. When the latches are transparent, external circuitry may be used to provide a new column address to the DRC to take advantage of the DRC's address drivers.

If the on-chip address counter is used, the user needs to select when the counter is incremented. If static column DRAMs are used, R6 = 0 should be programmed. If page mode DRAMs are used, R6 = 1 may be programmed. When R6 = 0, the column address will be incremented when $\overline{CAS}$ is negated. When R6 = 1, the column address is incremented before the access is completed, on the CLK edge that asserts $\overline{DTACK}$.

The $\overline{CAS}$ strobe is negated when the DRAM access is completed, even when static column DRAMs are used. This is done for two reasons:

1) To insure that data is not strobed into the incorrect page if a page miss occurs during a write access.
2) To retain flexibility of DRC operating modes.

Since the $\overline{CAS}$ propagtion delay and precharge time is matched to the DRC's column address increment propagation delay, there is no performance penalty associated with bringing $\overline{CAS}$ high.

68040 Burst Access Mode

68040 Burst Mode operation is selected when R8, $\overline{ECAS1}$, $\overline{ECAS3}$ =1, 0,1 during programming. If nibble mode DRAMs are used, $\overline{ECAS2}$ = 0 should be programmed, and $\overline{RAS}$ will be terminated when the burst is aborted or completed. If page or static column mode DRAMs are used, $\overline{ECAS2}$ = 1 may be programmed, and $\overline{RAS}$ will remain low.

When programmed for 68040 Burst Mode, $\overline{CAS}$ is always negated by the same rising CLK edge that negates $\overline{DTACK}$. $\overline{CAS}$ is always asserted on the next falling CLK edge unless the DRC has completed the burst or if the burst was aborted.

The DRC's burst can be aborted by asserting the DRC's Burst Inhibit (BIN) input. BIN is sampled on the rising edge of CLK that negates $\overline{CAS}$ and $\overline{DTACK}$, and if asserted, the burst is aborted. Once aborted, the next access must be initiated with $\overline{ADS}$(ALE) and $\overline{CS}$.

Two 68040 Burst Mode accesses, using nibble mode DRAMs are shown in Figure 8. During the first access, the DRC is allowed to complete the burst normally. The second access was deferred due to $\overline{RAS}$ precharge. The burst was aborted during the second access by asserting BIN.

Figures 9 and 10 show the same accesses with static column and page mode DRAMS, respectively. In the case of Figures 9 and 10, the $\overline{RAS}$ precharge is due to a page miss.

Figure 8. 68040 Burst Mode Access with Nibble Mode DRAMs ($\overline{ECAS2}$ = 0 During Programming)

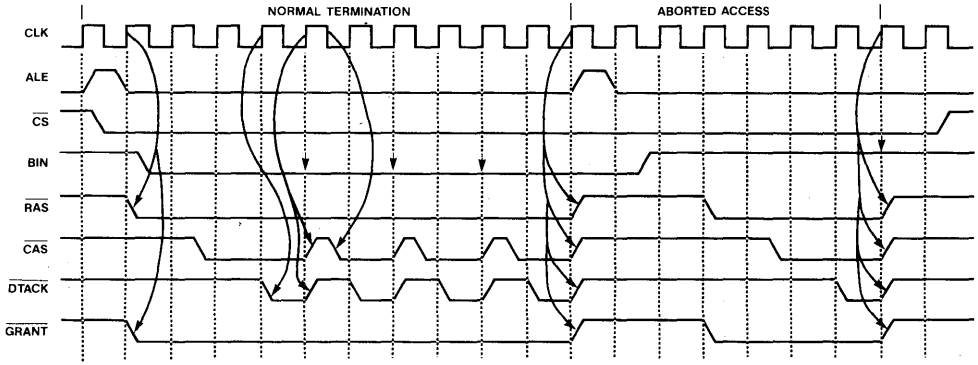


Figure 9. Burst Mode Access with Static Column DRAMs ($\overline{ECAS2}$ = 1, R6 = 0 During Programming)

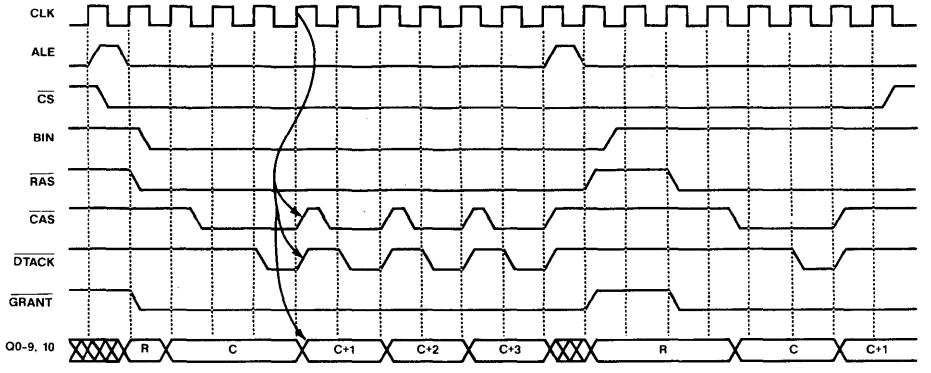
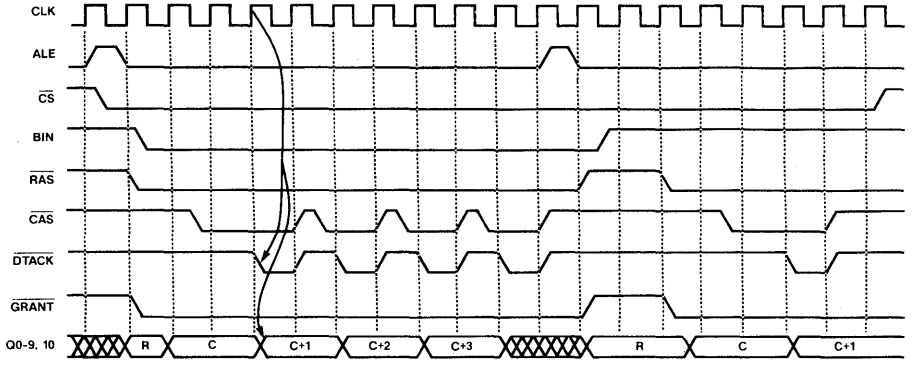


Figure 10. Burst Mode Access with Page Mode DRAMs ($\overline{ECAS2}$ = 1, R6 = 1 During Programming)



68030 Burst Access Mode

The MC68030's synchronous burst cache fill operation is supported by programming the DRC for 68030 Burst Mode operation. 68030 Burst Mode operation is very similar to 68040 Burst Mode operation, with only two notable exceptions:

1) $\overline{CAS}$ is asserted on the rising edge of CLK and negated on the falling edge.
2) The handshake input $\overline{CBREQ}$ is provided and is sampled on the rising edge of CLK that negates $\overline{DTACK}$.

The DRC's $\overline{DTACK}$ output drives the MC68030's $\overline{STERM}$ and $\overline{CBACK}$ inputs.

68030 Burst Mode operation is selected when R8, $\overline{ECAS1}$, $\overline{ECAS3}$ =1, 1, 0 during programming. If nibble mode DRAMs are used, $\overline{ECAS2}$ = 0 should be programmed, and $\overline{RAS}$ will be negated when the burst is aborted or completed. If page or static column mode DRAMs are used, $\overline{ECAS2}$ = 1 may be programmed, and $\overline{RAS}$ will remain low.

Two 68030 Burst Mode accesses, using nibble mode DRAMs are shown in Figure 11. During the first access, the DRC is allowed to complete the burst normally. The second access was deferred due to $\overline{RAS}$ precharge. The burst was aborted during the second access by negating $\overline{CBREQ}$.

Figures 12 and 13 show the same accesses with static column and page mode DRAMS, respectively. In the case of Figures 12 and 13, the $\overline{RAS}$ precharge is due to a page miss.

Figure 11. 68030 Burst Mode Access with Nibble Mode DRAMs ($\overline{ECAS2}$ = 0 During Programming)

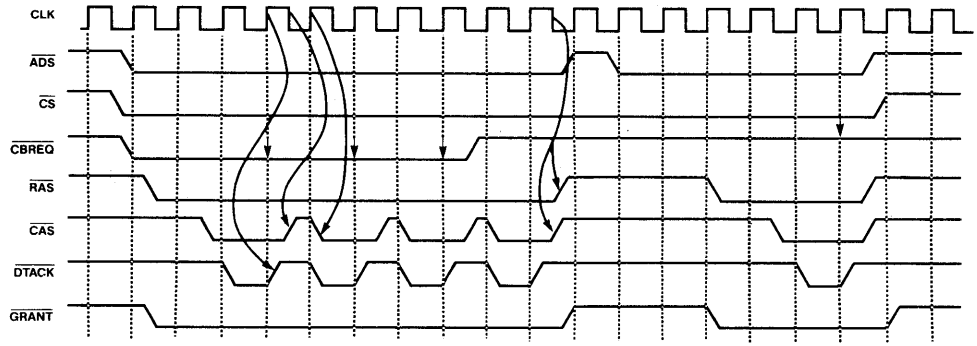


Figure 12. 68030 Burst Mode with Static Column DRAM ($\overline{ECAS2}$ = 1, R6 = 0 During Programming)

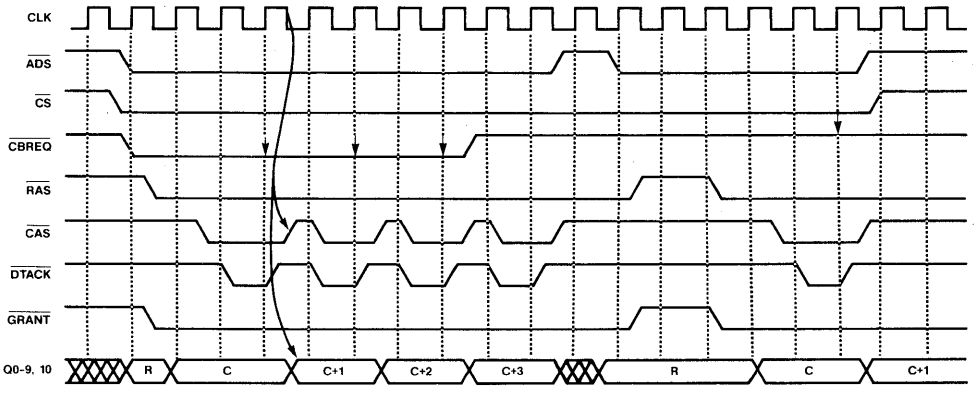
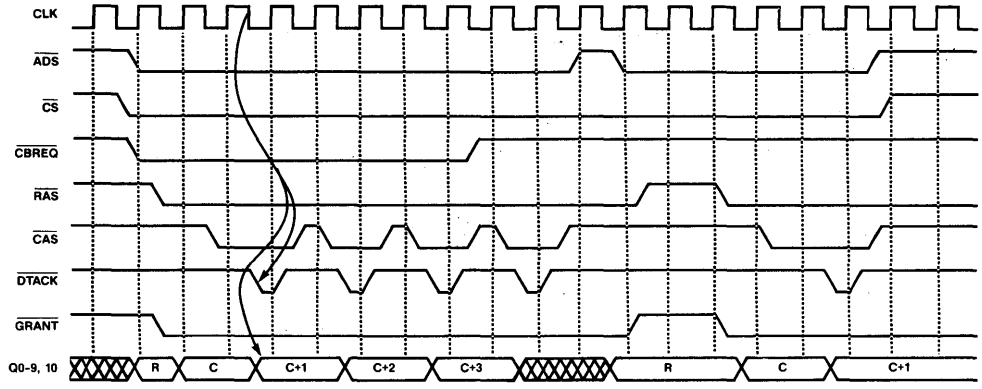


Figure 13. 68030 Burst Mode with Page Mode DRAMs ($\overline{ECAS2}$ = 1, R6 = 1 During Programming)



Interleaved Access Modes

The KS84C31/32 supports 2 or 4 way interleaved accesses between memory banks. By interleaving accesses between memory banks, performance degradation due to $\overline{RAS}$ precharge time is minimized. Interleaved Access Mode, may be used in systems that support address pipelining. The DRC is programmed for Interleaved Access Mode by programming R8, $\overline{ECAS1}$, $\overline{ECAS2}$, $\overline{ECAS3}$ = 0,0,0,0. When programmed for Interleaved Access Mode, and the next access is to a different bank of memory than the current access, the DRC will supply the next row address after the column address hold time is satisfied for the current access (25 ns min). $\overline{RAS}$ will be asserted for the next access when ALE is pulsed (Mode 0) or on the falling edge of $\overline{ADS}$ (Mode 1).

Interleaved Access Mode operation is shown in Figure 14. Back-to-back memory accesses are interleaved between two memory banks. Memory addresses A and C appear in bank 0; Memory address B appears in bank 1.

Interleaved Access Mode should not be used in conjunction with page or burst mode operation. However, the $\overline{RAS}$ precharge time is hidden in these modes if consecutive accesses hit different banks. Only one CLK of precharge will be incurred when switching banks. The programmed number of precharge clock cycles will be observed if consecutive access hit the same memory bank.

Wait State Support

Wait states are required when a relatively slow DRAM is operating with a fast CPU. Wait states allow the CPU's bus cycle to be extended by one or more CPU clock periods. The KS84C31/32 will insert wait states during the CPU's DRAM bus access in order to:

a) insert the desired number of wait states during the access,

b) delay the access until the refresh in progress is complete, or

c) delay the access to guarantee $\overline{RAS}$ precharge time.

The DRC generates two output signals to support the insertion of wait states. $\overline{GRANT}$ is asserted to inform external logic that the DRC has begun an access. $\overline{DTACK}$ is asserted to terminate the access. An input signal, $\overline{WAITIN}$, is provided to allow the user to add wait states dynamically during the access.

$\overline{GRANT}$ mimics the operation of $\overline{RAS}$ during an access. Like $\overline{RAS}$, it is asserted synchronous to CLK in Mode 0 and asynchronous to CLK in Mode 1 and remains active until $\overline{RAS}$ is negated. In case of a page miss, both $\overline{GRANT}$ and $\overline{RAS}$ will remain negated for at least 1T so that $\overline{GRANT}$ may be sampled by external circuitry to determine if a page miss has occured. $\overline{GRANT}$ is deasserted during refresh operations.

$\overline{DTACK}$ may be programmed (via R7) to be asserted on the rising or falling CLK edge. The number of CLK edges that $\overline{DTACK}$ is delayed, is programmable. $\overline{DTACK}$ is controlled by programming bits R2 and R3 for any access during which $\overline{RAS}$ is initially asserted (i.e. single accesses, page misses, etc). Programming bits R4 and R5 control $\overline{DTACK}$ during page hits and while bursting.

Figures 15 and 16 show how $\overline{DTACK}$ behaves in Mode 0 and 1 accesses during which $\overline{RAS}$ is initially asserted. Figures 17 and 18 shows how $\overline{DTACK}$ behaves during page hits.

Figure 14. 2-Way Interleaved Access Mode Operation ($\overline{ECAS0}$ = 1 During Programming)

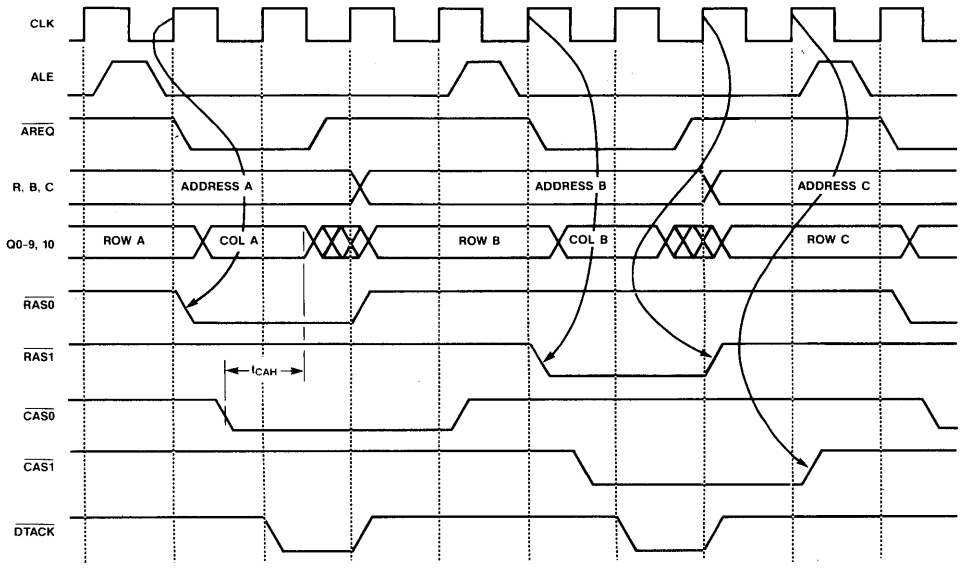


Figure 15. $\overline{DTACK}$ During Mode 0 Accesses, $\overline{RAS}$ Initially Asserted

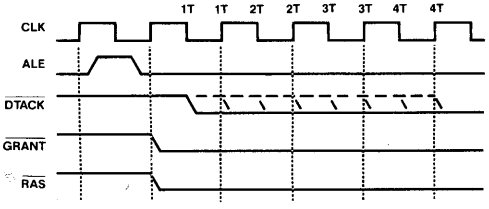


Figure 16. $\overline{DTACK}$ During Mode 1 Accesses, $\overline{RAS}$ Initially Asserted

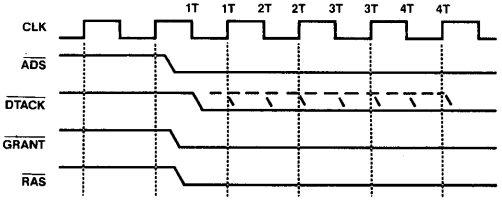


Figure 17. $\overline{DTACK}$ During Mode 0 Page Hits

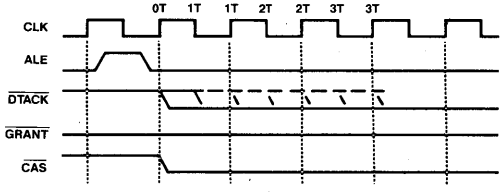
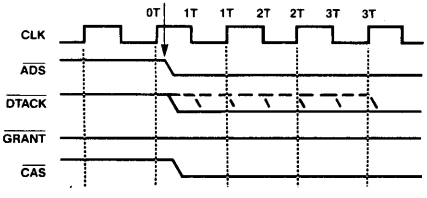


Figure 18. $\overline{DTACK}$ During Mode 1 Page Hits



When used in 68040 Burst Mode or 68030 Burst Mode, the DRC should not be programmed for 0T operation for page hits and subsequent burst cycles. This will not impact memory performance, since the opening cycle of a burst access would be expected to have at least one wait state. Regardless of when $\overline{DTACK}$ is asserted, it is always negated on the next rising CLK edge in both burst modes, as shown in Figures 19 and 20.

Figure 19. $\overline{DTACK}$ While Bursting 68040 in Burst Mode

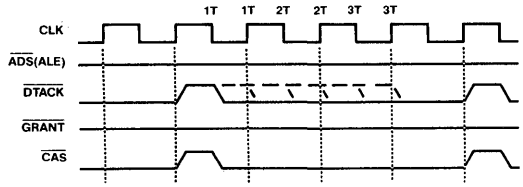
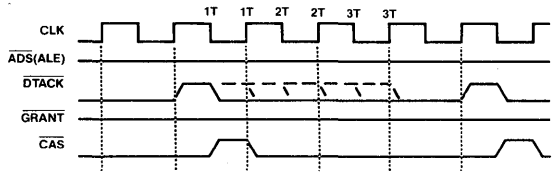


Figure 20. $\overline{DTACK}$ While Bursting in 68030 Burst Mode



If nibble mode DRAMs are used ($\overline{ECAS2}$ = 0), $\overline{GRANT}$ will be negated when the burst has been aborted or completed; It remains asserted if page or static column mode DRAMs are used ($\overline{ECAS2}$ = 1).

Any access may be extended on the fly by asserting the $\overline{WAITIN}$ input. If R6 = 0 during programming, $\overline{WAITIN}$ is used to add one wait state during the access as shown in Figure 21. $\overline{WAITIN}$ is sampled once during the access, when $\overline{DTACK}$ is to be asserted by the DRC. $\overline{DTACK}$ will remain negated for one more rising CLK edge if $\overline{DTACK}$ is rising edge triggered or one more falling CLK edge if $\overline{DTACK}$ is falling edge trigered. $\overline{WAITIN}$ will not be sampled again, until the next access.

If R6 = 1 during programming, $\overline{WAITIN}$ may be used to defer $\overline{DTACK}$ indefinitely as shown in Figure 22. $\overline{WAITIN}$ is first sampled on:

- The falling edge of $\overline{ADS}$ (Mode 1)
- The first rising edge CLK after ALE is pulsed high (Mode 0)
- The CLK edge that negates $\overline{DTACK}$ while bursting

If $\overline{WAITIN}$ is inactive, the DRC will assert $\overline{DTACK}$ after the programmed number of CLK edges. If $\overline{WAITIN}$ was active, the $\overline{DTACK}$ CLK edge count is deferred. $\overline{WAITIN}$ will be continually sampled on the rising edge of CLK if $\overline{DTACK}$ is rising edge triggered or on the falling edge of CLK if $\overline{DTACK}$ is falling edge triggered. Once $\overline{WAITIN}$ is negated, the DRC will assert $\overline{DTACK}$ after the programmed number of CLK edges and will not sample $\overline{WAITIN}$ again until the next access.

Programming bit R6 also determines when the column address is incremented in both burst modes. If R6 = 0 during programming, the column address is incremented when $\overline{CAS}$ is negated. If R6 = 1 during programming, the column address is incremented when $\overline{DTACK}$ is asserted.

Figure 21 shows a 68030 Burst Mode burst cycle. The DRC has been programmed to assert $\overline{DTACK}$ on the second falling CLK edge after $\overline{CAS}$ is asserted. $\overline{DTACK}$ was held negated for 1 extra CLK period due to $\overline{WAITIN}$. Since R6 = 0, the column address is incremented when $\overline{CAS}$ is negated for use with static column DRAMs.

Figure 21. WAITIN, R6 = 0 During Programming

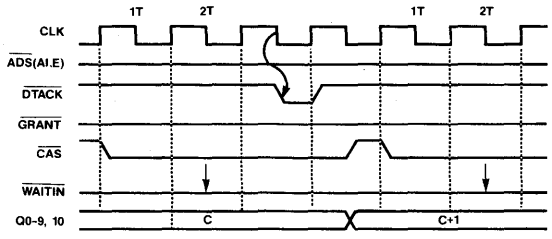
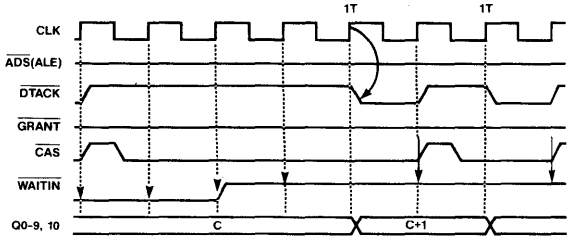


Figure 22 shows two 68040 Burst Mode burst cycles. The DRC has been programmed to assert DTACK on the first rising CLK edge after CAS is asserted. In the first cycle, WAITIN was sampled active on the clock edge that negated DTACK. DTACK is rising edge triggered, so WAITIN is continually sampled on rising CLK edges until it is negated. Since the DRC was programmed to assert DTACK one rising CLK edge after CAS was asserted, DTACK is asserted one rising CLK edge after WAITIN is negated. Since WAITIN is negated during the second burst cycle, DTACK is asserted on the first rising CLK edge after CAS is asserted.

Since R6 = 1, the column address is incremented when DTACK is asserted.

Figure 22. WAITIN, R6 = 1 During Programming



REFRESH OPERATIONS

The DRC supports four refresh control mode options:

1) internal automatic refreshing

2) internal automatic burst refreshing

3) externally controlled/burst refreshing

4) refresh request/acknowledge burst refreshing

With each of the control modes above, RAS only refresh, staggered RAS only refresh, or error scrubbing with RAS only refresh may be performed.

Three inputs, extend refresh (EXTDRF), refresh (RFSH) and disable refresh (DISRFSH), along with two outputs, refresh in progress (RFIP) and refresh request (RFRQ) are associated with refreshing.

DISRFSH and RFSH are used in the externally controlled/burst refresh mode and the refresh request/acknowledge mode. External circuitry asserts DISRFSH to inhibit internally requested refreshes and requests refreshes by asserting RFSH.

$\overline{RFRQ}$ is used in the refresh request/acknowledge mode. The DRC asserts $\overline{RFRQ}$ to request a refresh cycle but will not perform the refresh until external circuitry acknowledges the request by asserting $\overline{RFSH}$ as long as $\overline{DISRFSH}$ is asserted.

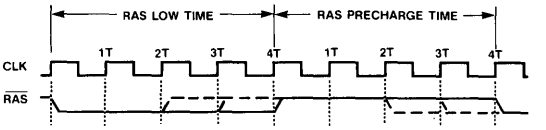
$\overline{RFIP}$ is used in all refresh modes. The DRC asserts $\overline{RFIP}$ to indicate to external circuitry that a refresh is in progress.

EXTDRF is used when the DRC is programmed for error scrubbing. External circuitry asserts EXTDRF to extend the refresh cycle.

The internal refresh row counter will be incremented automatically, regardless of the refresh control mode used. The refresh address counter will be incremented once all of the refresh RASs have been negated. The refresh counter may be reset by asserting $\overline{RFSH}$ while $\overline{DISRFSH}$ is high.

In every combination of refresh control mode and type, the DRC will assert the refresh RASs for a programmed number of CLK periods. CLK edges for $\overline{RAS}$ low time during refresh and $\overline{RAS}$ precharge time are counted as shown in Figure 23.

Figure 23. $\overline{RAS}$ Low and Precharge Time



REFRESH CONTROL MODES

Automatic Internal Refresh

The DRC has an internal refresh clock to generate internal refresh requests. An internal refresh request is generated every period of the refresh clock. $\overline{RFRQ}$ is pulsed once every period of the refresh clock. The refresh clock period is programmed according to the value of address bits C0-C3. The internal refresh request will generate an automatic internal refresh as long as a DRAM access is not currently in progress and the $\overline{RAS}$ precharge time has been met. If a DRAM access is in progress when the refresh timer requests a refresh, the on-chip arbitration logic will allow the access to finish before the refresh is initiated. The next DRAM access is deferred until the refresh cycle is complete.

The refresh period for most DRAMs is 15 µs. This means that a 1 Mbit DRAM has to be refreshed every 8 ms, during which time, 512 rows must be accessed. This requires a 9-bit row address refresh counter. The KS84C31 has a 10-bit counter and the KS84C32, an 11-bit counter. The extra bits are used for error scrubbing over the entire address range.

Automatic internal refresh is possible in Single Access, Interleaved Access and both burst modes. When the DRC is operated in Page Mode or either burst mode with page or static column mode DRAMs, an enhanced version of automatic internal refreshing is available as shown in the next section.

$\overline{DISRFSH}$ must be negated to enable automatic internal refreshes.

Automatic Internal Burst Refreshing

The $\overline{RAS}$ pulse width, t_{RASP} and t_{RASC}, of most page and static column DRAMs is limited to 100 us. The DRC takes advantage of this characteristic by supporting automatic internal burst refreshing. When operating in automatic internal burst refresh control mode, the DRC will perform a 5-refresh burst after the 5th internal refresh request (approximately every 75 us) instead of performing a refresh after every internal request, as in the automatic internal refresh control mode.

$\overline{DISRFSH}$ must be negated to enable automatic internal burst refreshes. However, if $\overline{DISRFSH}$ is asserted for any reason, all pending refreshes (up to 5) will be performed when $\overline{DISRFSH}$ is again negated. While $\overline{DISRFSH}$ is asserted, no internal refresh requests will accumulate.

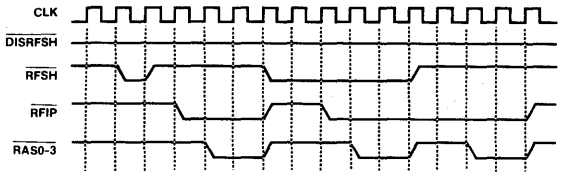
Externally Controlled/Burst Refresh

When using externally controlled/burst refresh, internally generated refresh requests are ignored. Instead, external circuitry is used to pulse the refresh ($\overline{RFSH}$) signal low to generate a refresh request. The refresh cycle will take place on the next positive edge of CLK. If a DRAM access is in progress or the $\overline{RAS}$ precharge time has not been satisfied, the refresh will be delayed. This means that the

access $\overline{RAS}$ must be negated with DISPM if $\overline{ECAS2}$ = 1 is programmed in order to precharge $\overline{RAS}$ before the refresh can take place. If $\overline{RFSH}$ is asserted when the refresh $\overline{RAS}$ is negated, $\overline{RFIP}$ will remain asserted and another refresh cycle will be performed after $\overline{RAS}$ has been precharged.

Figure 24 shows how $\overline{DISRFSH}$ and $\overline{RFSH}$ are used to control single and burst refreshes. The DRC is performing a $\overline{RAS}$ only refresh under external control and has been programmed to assert the refresh $\overline{RAS}$ for 2T and to precharge $\overline{RAS}$ for 2T.

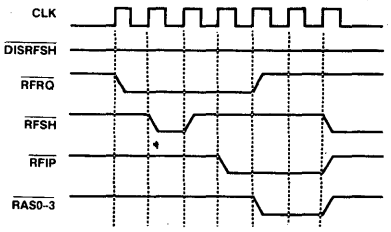
Figure 24. Externally Controlled/Burst Refresh



Refresh Request/Acknowledge Burst Refreshing

In this refresh control mode, internally generated refresh requests are ignored by the DRC. Instead, external circuitry monitors the the DRC's $\overline{RFRQ}$ output and generates a refresh request at the appropriate time by pulsing $\overline{RFSH}$. The refresh is then performed as shown in Figure 25.

Figure 25. Refresh Request/Acknowledge Refresh



REFRESH TYPES

The DRC supports three types of refreshing:

1) $\overline{RAS}$ only

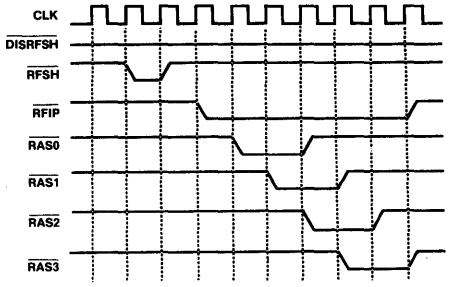
2) Staggered $\overline{RAS}$ only

3) $\overline{RAS}$ only with Error Scrubbing

Each refreshing type may by controlled by any refresh control mode. The DRC asserts all RASs at the same time when performing $\overline{RAS}$ only refreshing as shown in Figure 24. The DRC asserts each $\overline{RAS}$ at one CLK intervals when performing staggered $\overline{RAS}$ only refreshing as shown in Figure 26a. C4, C5, C6 has to be programmed as shown.

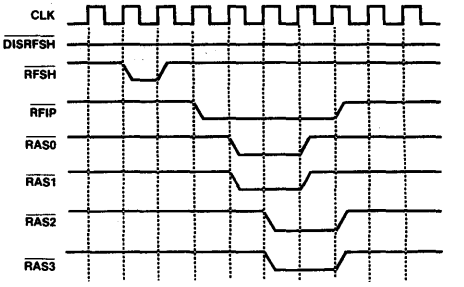
Two $\overline{RAS}$ lines will be asserted at a time if C4, C5, C6 is programmed as shown in Figure 26b.

Figure 26a. Staggered $\overline{RAS}$ Only Refreshing



C4	C5	C6
0	1	1
1	1	0
1	1	1

Figure 26b. Staggered $\overline{RAS}$ Only Refreshing



C4	C5	C6
0	0	1
1	0	1

RESET

The KS84C31/32 on-chip power-up reset logic generates a reset pulse:

- At power up
- If V_{CC} falls well below 3V and reaches V_{CC} min.

When the chip is reset, the Mode Register (with the exception of bit C6, which is set) and all internal counters are reset. All of the output signals are inactive; $\overline{RAS0\text{-}3}$, $\overline{CAS0\text{-}3}$, $\overline{DTACK}$, $\overline{RFIP}$, $\overline{WE}$, $\overline{RFRQ}$ and $\overline{GRANT}$ are high while Q0-9,10 are low.

After power-up, the DRC is operable after 200 μs and the Mode Register can be programmed if the programmable version of the chip is being used.

The Moad Load signal ($\overline{ML}$) can be used to reset the chip at any time after power-up. When $\overline{ML}$ is driven low, all internal counters are reset and the Mode Register is enabled to receive the mode bit inputs.

The internal refresh interval counter may be reset at any time by asserting $\overline{RFSH}$ while $\overline{DISRFSH}$ is high.

PROGRAMMING THE KS84C31/32

The KS84C31/32 has a Mode Register that can be programmed by the user or mask programmed at the factory. The Mode Register controls the internal operating modes of the DRC.

The DRC is programmed via the system's address bus, not the data bus. The Mode Register receives inputs from the CPU on address lines R0-9 and C0-9, the bank select lines B0 and B1, and the $\overline{CAS}$ enable lines $\overline{ECAS0\text{-}3}$. The Mode Register is enabled by the falling edge of $\overline{ML}$. The inputs are then strobed in on the rising edge of $\overline{ML}$ as show in Figure 27.

Alternatively, the Mode Register may be programmed by initiating a "fake" access as shown in Figure 28. When programmed in this fashion, $\overline{ML}$ and $\overline{CS}$ are asserted, followed by $\overline{AREQ}$. The programming inputs are strobed into the Moad Load Register on the falling edge of $\overline{AREQ}$. $\overline{DTACK}$ is asserted on the falling edge of $\overline{AREQ}$ to terminate the bus access and is negated by the rising edge of $\overline{ML}$ or $\overline{AREQ}$ (whichever occurs first).

Figure 27. Mode Load Only Programming

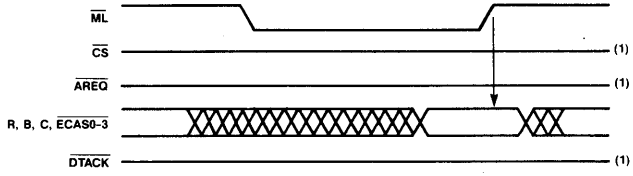


Figure 28. Fake Access Programming

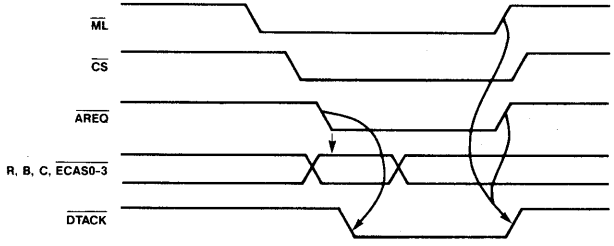


Table 4. Programming the Mode Register

OPERATING MODES

R8, $\overline{ECAS1\text{-}3}$

These bits program the DRCs operating mode. The user has the choice of Single Access Mode, Interleaved Access Mode, Page Access Mode, 68040 Burst Access Mode with nibble or page mode or 68030 Burst Access Mode with nibble or page mode.

R8	$\overline{ECAS1}$	$\overline{ECAS2}$	$\overline{ECAS3}$	Operating Mode
1	0	0	0	Single Access Mode
1	0	1	0	Page Access Mode
1	0	0	1	68040 Burst Access Mode with Nibble Mode
1	0	1	1	68040 Burst Access Mode with Page/Static Column Mode
1	1	0	0	68030 Burst Access Mode with Nibble Mode
1	1	1	0	68030 Burst Access Mode with Page/Static Column Mode
0	0	0	0	Interleaved Access Mode

ADDRESS LATCH/AUTOMATIC COLUMN INCREMENT WHILE BURSTING

B0

B0 allows the user to specify whether the on-chip latches should latch the address inputs on the falling edge of $\overline{ADS}$(ALE) or whether they should remain tranparent. If $\overline{ECAS2}$ = 1 during programming (page or static column mode DRAMs are being used), then the row address is always latched by the on-chip page detect logic regardless of how B0 is programmed.

The user also specifies whether the DRC automatically increments the column address while bursting or if external circuitry is required to change the column address. If B0 = 0 during programming, then the column address is automatically incremented while bursting. If B0 = 1, the address latches will remain tranparent, disabling the automatic column increment.

B0		Automatic Column Increment
0	Address Bits Latched	Enabled
1	Address Latches Transparent	Disabled

ACCESS START AND TERMINATION MODES

B1

B1 allows the user to specify either synchronous or asynchronous access start and termination modes.

A synchronous (Mode 0) access is controlled by the system clock. The access is initiated on the first rising CLK edge after ALE goes high. $\overline{AREQ}$ is sampled on rising CLK edges and terminates the access when it is asserted.

An asynchronous (Mode1) access is initiated immediately by the falling edge of $\overline{ADS}$ and is immediately terminated by the rising edge of $\overline{AREQ}$.

B1	
0	Mode 0
1	Mode 1

Table 4. Programming the Mode Register (Continued)

$\overline{RAS}$ LOW AND $\overline{RAS}$ PRECHARGE TIME

R0, R1

These bits control the time that $\overline{RAS}$ is low during refresh operations and also determine the $\overline{RAS}$ precharge time. The time interval shown (T) is equivalent to one rising CLK edge. The user should take into account $\overline{RAS}$ rise and fall time when programming these bits.

R0	R1	$\overline{RAS}$ Low Time	$\overline{RAS}$ Precharge Time
0	0	2T	2T
0	1	2T	3T
1	1	3T	3T
1	1	4T	4T

$\overline{DTACK}$ GENERATION FOR ACCESSES THAT INITIALY ASSERT $\overline{RAS}$

R2, R3

These bits control $\overline{DTACK}$ generation for any access during which $\overline{RAS}$ is initiated. R2 and R3 determine the number of CLK edges that $\overline{DTACK}$ remains negated under the following conditions:

- All accesses when the DRC is programmed for Single or Interleaved Access Modes
- During page misses and deferred accesses when the DRC is programmed for Page Mode
- During the opening cycle of a burst access when the DRC is programmed for 68040 Burst or 68030 Burst Access Modes when nibble mode is used or if a page miss occurs during the opening access when page mode is used.

The time interval shown (T) refers to one rising or falling CLK edge. Bit R7 determines whether $\overline{DTACK}$ is asserted on rising or falling CLK edges.

R2	R3	$\overline{DTACK}$ Low From Access Start
0	0	1T
0	1	2T
1	0	3T
1	1	4T

$\overline{DTACK}$ GENERATION FOR PAGE HITS AND BURST ACCESSES

R4, R5

These bits control $\overline{DTACK}$ generation for any access during which only $\overline{CAS}$ is initiated. R4 and R5 determine the number of CLK edges that $\overline{DTACK}$ remains negated under the following conditions:

- During page hits when the DRC is programmed for Page Mode
- During the opening cycle of a burst access that results in a page hit when the DRC is programmed for 68040 Burst or 68030 Burst Access Modes and page mode is used.
- While Bursting

The time interval shown (T) refers to one rising or falling CLK edge. Bit R7 determines whether $\overline{DTACK}$ is asserted on rising or falling CLK edges.

R4	R5	$\overline{DTACK}$ Low From Access Start
0	0	0T
0	1	1T
1	0	2T
1	1	3T

Table 4. Programming the Mode Register (Continued)

PROGRAMMING $\overline{\text{WAITIN}}$ FOR WAIT STATE INSERTION AND COLUMN INCREMENT

R6

R6 controls the functionality of $\overline{\text{WAITIN}}$ in all operating modes. It also determines when the column address will be incremented when the DRC is operated in 68040 Burst and 68030 Burst Modes.

R6	$\overline{\text{WAITIN}}$ Functionality	Column Address Increment
0	Add 1 wait state if active.	Increment when $\overline{\text{CAS}}$ is negated
1	Continually add wait states.	Increment when $\overline{\text{DTACK}}$ is asserted

PROGRAMMING $\overline{\text{DTACK}}$ FOR RISING OR FALLING CLK EDGES

R7

This bit controls whether $\overline{\text{DTACK}}$ is asserted (and $\overline{\text{WAITIN}}$ is sampled) on rising or falling CLK edges.

R7	$\overline{\text{DTACK}}$
0	Rising Edge Triggered
1	Falling Edge Triggered

STAGGERED REFRESH OPTIONS

R9

R9 determines whether the refresh operation is $\overline{\text{RAS}}$ Only or Staggered $\overline{\text{RAS}}$ Only. During a $\overline{\text{RAS}}$ Only refresh cycle, all $\overline{\text{RAS}}$ outputs are asserted and negated at the same time. In a Staggered $\overline{\text{RAS}}$ Only refresh cycle, the $\overline{\text{RAS}}$ outputs will go low in sequence, at one clock intervals. One or two $\overline{\text{RAS}}$ outputs are selected at a time, depending on the $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ configuration selected by C4-C6.

Error scrubbing is not supported when Staggered $\overline{\text{RAS}}$ Only refresh is programmed.

R9	
0	$\overline{\text{RAS}}$ Only Refresh
1	Staggered $\overline{\text{RAS}}$ Only Refresh

RFCLK DIVISOR

C0, C1, C2

These bits allow the user to select the divisor for the refresh clock (RFCLK) input, from which the internal refresh clock is generated. Select the divisor such that the internal refresh clock frequency is approximately 2 MHz.

C0	C1	C2	Divisor
0	0	0	10
0	0	1	6
0	1	0	8
0	1	1	4
1	0	0	9
1	0	1	5
1	1	0	7
1	1	1	3

Table 4. Programming the Mode Register (Continued)

INTERNAL REFRESH CLOCK DIVISOR

C3 allows the user to divide the internal refresh clock to achieve the desired interval between internally generated refresh requests.

C3	Divisor	Refresh Interval if Internal Refresh Clock Freqency is 2 MHz
0	30	15 μs
1	26	13 μs

$\overline{RAS}$ AND $\overline{CAS}$ CONFIGURATIONS

C4, C5, C6: These bits control the $\overline{RAS}$ and $\overline{CAS}$ configurations. There are 4 $\overline{RAS}$ and 4 $\overline{CAS}$ outputs. They can always be grouped such that each $\overline{RAS}$ and $\overline{CAS}$ will drive one fourth of the memory array, regardless of whether the array is arranged in 1, 2 or 4 banks. The setting of these bits also determines whether error scrubbing and Interleaved Access Mode can be supported.

C4	C5	C6	$\overline{RAS}$ and Configuration Modes	Error Scrubbing	Interleaved Access Mode
0	0	0	$\overline{RAS}$0–3 are brought low during an access. $\overline{CAS}$0–3 are all selected during an access but only those enabled by the corresponding $\overline{ECAS}$ can go low. B0 and B1 are not used.	Yes	No
0	0	1	$\overline{RAS}$ pairs are selected by B1. $\overline{CAS}$0–3 are all selected during an access but only those enabled by the corresponding $\overline{ECAS}$ can go low.	No	No
0	1	0	$\overline{RAS}$, $\overline{CAS}$ pairs are selected by B0 and B1. A selected $\overline{CAS}$ will go low only if enabled by its corresponding $\overline{ECAS}$.	Yes	Yes
0	1	1	$\overline{RAS}$ is selected by B0 and B1. $\overline{CAS}$0–3 are all selected during an access but only those enabled by the corresonding $\overline{ECAS}$ can go low.	No	No
1	0	0	$\overline{RAS}$, $\overline{CAS}$ pairs are selected by B1. A selected $\overline{CAS}$ will go low only if enabled by its corresponding $\overline{ECAS}$.	Yes	Yes
1	0	1	$\overline{RAS}$, $\overline{CAS}$ pairs are selected by B1. A selected $\overline{CAS}$ will go low only if enabled by its corresponding $\overline{ECAS}$.	No	Yes
1	1	0	$\overline{RAS}$0–3 are brought low during an access. $\overline{CAS}$0–3 are all selected during an access but only those enabled by the corresponding $\overline{ECAS}$ can go low. B0 and B1 are not used.	No	No

B1	B0	
0	X	$\overline{RAS}$0, 1
1	X	$\overline{RAS}$2, 3

B1	B0	
0	0	$\overline{RAS}$0, $\overline{CAS}$0
0	1	$\overline{RAS}$1, $\overline{CAS}$1
1	0	$\overline{RAS}$2, $\overline{CAS}$2
1	1	$\overline{RAS}$3, $\overline{CAS}$3

B1	B0	
0	0	$\overline{RAS}$0
0	1	$\overline{RAS}$1
1	0	$\overline{RAS}$2
1	1	$\overline{RAS}$3

B1	B0	
0	X	$\overline{RAS}$0, 1 and $\overline{CAS}$0, 1
1	X	$\overline{RAS}$2, 3 and $\overline{CAS}$2, 3

B1	B0	
0	X	$\overline{RAS}$0, 1 and $\overline{CAS}$0, 1
1	X	$\overline{RAS}$2, 3 and $\overline{CAS}$2, 3

Table 4. Programming the Mode Register (Continued)

$\overline{RAS}$ AND $\overline{CAS}$ CONFIGURATIONS (Continued)

C4	C5	C6	$\overline{RAS}$ and Configuration Modes	Error Scrubbing	Interleaved Access Mode
1	1	1	$\overline{RAS}$ pairs are selected by B0 and B1. A selected $\overline{CAS}$ will go low only if enabled by its corresponding $\overline{ECAS}$.	No	Yes

B1	B0	
0	0	$\overline{RAS0}$, $\overline{CAS0}$
0	1	$\overline{RAS1}$, $\overline{CAS1}$
1	0	$\overline{RAS2}$, $\overline{CAS2}$
1	1	$\overline{RAS3}$, $\overline{CAS3}$

COLUMN ADDRESS SETUP TIME

C7 allows the user to specify the minimum guaranteed column address setup time (t_{ASC}).

C7	t_{ASC}
0	10 ns
1	0 ns

ROW ADDRESS HOLD TIME

C8 allows the user to specify the minimum guaranteed row address hold time (t_{RAH}).

C8	t_{RAH}
0	20 ns
1	12 ns

DELAY $\overline{CAS}$ DURING WRITE ACCESSES

C9 allows the user to delay $\overline{CAS}$ during write operations that result in page hits or that occur during a burst cycle. This option allows the user to insure that the data is valid at the DRAM before $\overline{CAS}$ is asserted. Since the $\overline{CAS}$ delay would most likely require an additional wait state during the write access, $\overline{DTACK}$ may be automatically delayed.

During Mode 1 page hits, if DELAY $\overline{CAS}$ is selected, $\overline{CAS}$ will be asserted on the first CLK rising edge after $\overline{ADS}$ is asserted. If $\overline{DTACK}$ was programmed for 0T operation, $\overline{DTACK}$ will be asserted on the same CLK rising edge that asserted CAS. If $\overline{DTACK}$ was programmed for 1T, 2T or 3T operation, the DRC will begin counting CLK edges after $\overline{CAS}$ is asserted.

During Mode 0 page hits, if DELAY $\overline{CAS}$ is selected, the assertion of both $\overline{CAS}$ and $\overline{DTACK}$ will be delayed one complete CLK period.

During burst accesses, if DELAY $\overline{CAS}$ is selected, the assertion of both $\overline{CAS}$ and $\overline{DTACK}$ will be delayed one complete CLK period.

C9	
0	No Delay
1	Delay $\overline{CAS}$

EXTEND $\overline{CAS}$ AND SPECIFY $\overline{WE}$ OR $\overline{RFRQ}$

$\overline{ECAS0}$ allows the user to specify whether $\overline{CAS}$ is extended when the DRC is programmed for Single Access Mode. This option allows the user to begin precharging $\overline{RAS}$ before the access is completed. $\overline{ECAS0}$ also specifies whether the $\overline{WE}$($\overline{RFRQ}$) pin functions as Write Enable or Refresh Request

$\overline{ECAS0}$		
0	$\overline{CAS}$ is negated by $\overline{AREQ}$.	Specify $\overline{WE}$
1	$\overline{CAS}$ remains asserted until the next rising CLK edge after $\overline{RAS}$ is negated.	Specify $\overline{RFRQ}$

DC ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

DC Supply Voltage 7V
Temperature Under Bias ..... 0°C + 70°C
Storage Temperature ..... -65°C to 150°C

All Input and Output Voltage ..... V_{SS} - 0.5V to +7V
Power Dissipation at 33MHz 0.7W
E.S.D. 2000V

Note: If the device is used beyond the maximum rating, permanent damage may occur. Operation should be limited to those conditions specified under DC Electrical Characteristics.

DC Electrical Characteristics (T_A = 0°C to +70°C, V_{CC} = 4.75V to 5.25V, V_{SS} = 0V)

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IH}	Input High Voltage	Tested with limited Test pattern	2.0		V_{CC}+0.5	V
V_{IL}	Input Low Voltage	Tested with limited Test pattern	-0.5		0.8	V
V_{OH1}	Q and $\overline{WE}$ Outputs	I_{OH} = -3mA	2.4			V
V_{OL1}	Q and $\overline{WE}$ Outputs	I_{OL} = 10mA			0.5	V
V_{OH2}	All outputs except Q and $\overline{WE}$	I_{OH} = -1mA	2.4			V
V_{OL2}	All outputs except Q and $\overline{WE}$	I_{OL} = 3mA			0.5	V
I_{IN}	Input Leakage Current	V_{IN} = V_{CC} or V_{SS}			±10	μA
I_{ILML}	$\overline{ML}$ Input Current	V_{IN} = V_{SS}			200	μA
I_{CC1}	Quiescent Current	CLK at 33MHz Inputs Inactive			25	mA
I_{CC2}	Supply Current	Inputs Active (I load = 0)		65	125	mA
C_{IN}	Input Capacitance	f_{IN} at 1MHz		5	10	pF

AC SWITCHING CHARACTERISTICS

Figure 29 shows a typical test circuit, while Figure 30 shows the output drive levels. Figures 32 through 52 provide switching characteristics for a number of typical KS84C31/32 operations:

Unless otherwise stated V_{CC} = 4.75V to 5.25V, $0 < T_A < 70°C$

Load Capacitance: Q0-Q9, Q10 C_L = 380pF
$\overline{WE}$ C_L = 500pF
$\overline{RAS0-3}$, $\overline{CAS0-3}$ C_L = 125pF
All other Outputs C_L = 50pF

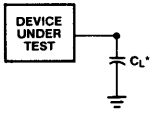
All minimum and maximum values are measured in nanoseconds.

Propagation delay variance vs. load capacitance:

$\overline{RAS}$, $\overline{CAS}$ 5ns/100pF rise time
3ns/100pF fall time
Q0-Q9, Q10 4ns/100pF rise time
3ns/100pF fall time

CAPACITIVE LOAD SWITCHING

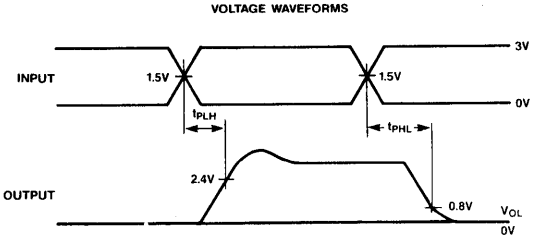
Figure 29. Switching Test Circuit



*t_{PD} SPECIFIED AT C_L = 380pF ALL Q OUTPUTS
C_L = 125pF $\overline{RAS}$ AND $\overline{CAS}$ OUTPUTS
C_L = 500pF $\overline{WE}$ OUTPUTS
C_L = 50pF ALL OTHER OUTPUTS

TYPICAL SWITCHING CHARACTERISTICS

Figure 30. Output Drive Levels



AC Testing inputs are driven at 3.0V for a logic "1" and 0.0V for a logic "0". Timing measurements are made at 2.4V for a logic "1" and 0.8V for a logic "0" at the outputs.

Figure 31. Simplified Output Driver Schematic

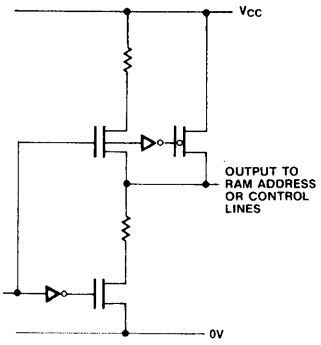


Figure 32. CLK, RFCLK Timing

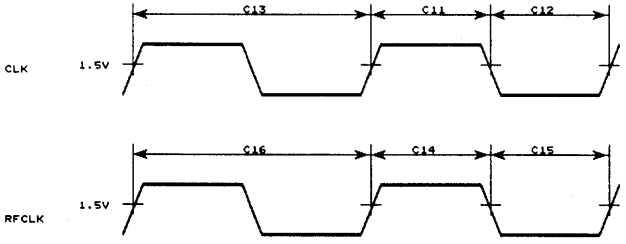


Figure 33. Single Access Mode Mode 0

MODE SETTING		
R0	0	2T tRP
R1	0	
R2	0	2T NON BURST
R3	1	
R4	X	
R5	X	
R6	X	
R7	1	CLK RISING EDGE
R8	0	INTERLEAVE
R9	X	
C0	X	
C1	X	
C2	X	
C3	X	
C4	0	RAS/CAS PAIRS
C5	1	
C6	0	
C7	X	
C8	X	
C9	X	
B0	0	ADDRESS LATCH
B1	0	SYN MODE 0
ECAS0	0	
ECAS1	0	
ECAS2	0	
ECAS3	0	

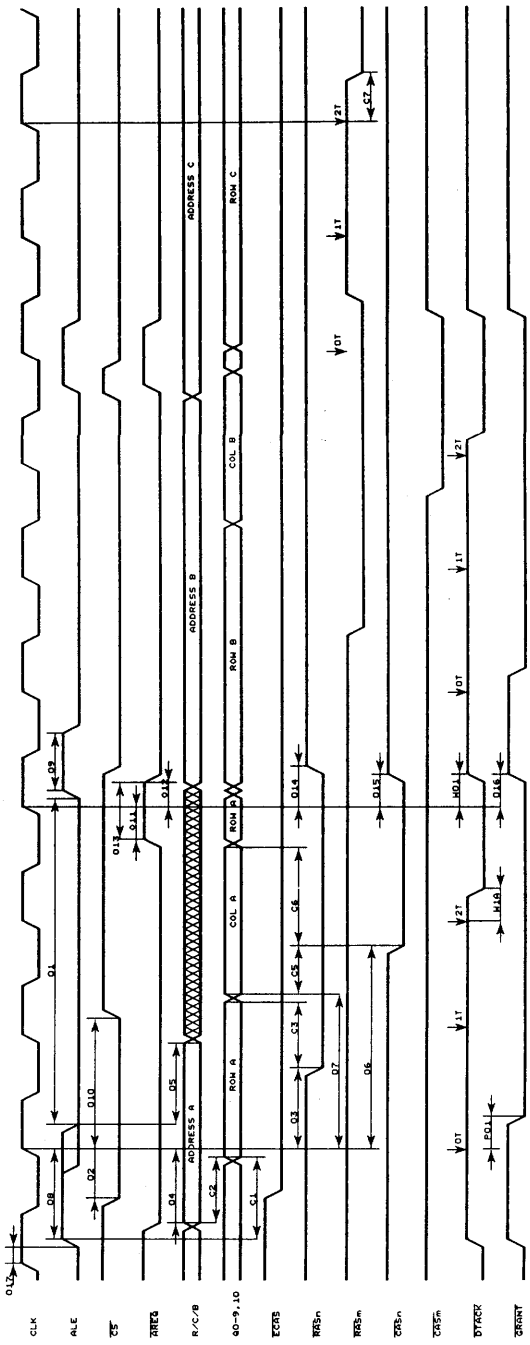


Figure 34. Single Access Mode Mode 1

MODE SETTING		
R0	0	2T tRP
R1	0	
R2	0	2T NON BURST
R3	1	
R4	X	
R5	X	
R6	X	
R7	1	CLK RISING EDGE
R8	0	INTERLEAVE
R9	X	
C0	X	
C1	X	
C2	X	
C3	X	
C4	0	RAS/CAS PAIRS
C5	1	
C6	0	
C7	X	
C8	X	
C9	X	
B0	0	ADDRESS LATCH
B1	1	ASYN MODE 1
ECAS0	0/1	CAS DELAY
ECAS1	0	
ECAS2	0	
ECAS3	0	

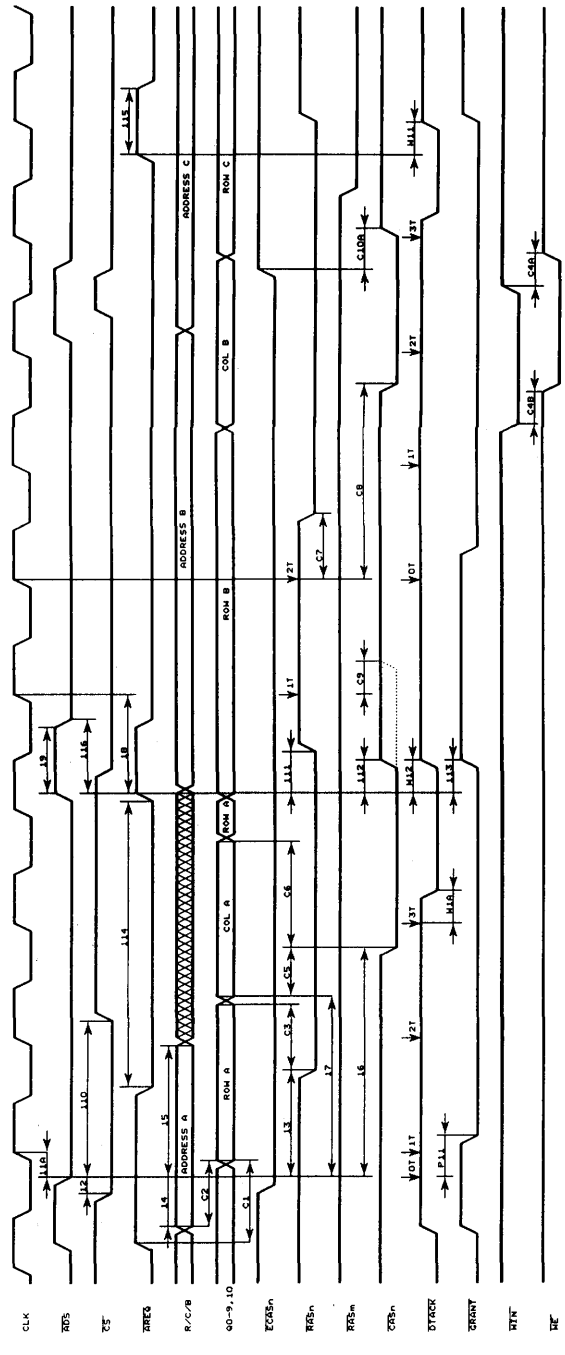


Figure 35. Page Access Mode Mode 0

MODE SETTING		
R0	0	2T tRP
R1	0	
R2	0	1T NON BURST
R3	0	
R4	0	1T BURST
R5	1	
R6	0	ADD 1T
R7	0/1	CLK RISING/FALL
R8	1	NON INTERL.
R9	X	
C0	X	
C1	X	
C2	X	
C3	X	
C4	0	RAS/CAS PAIRS
C5	1	
C6	0	
C7	X	
C8	X	
C9	X	
B0	X	
B1	0	SYN MODE 0
ECAS0	0	
ECAS1	0	
ECAS2	1	PAGE MODE
ECAS3	0	

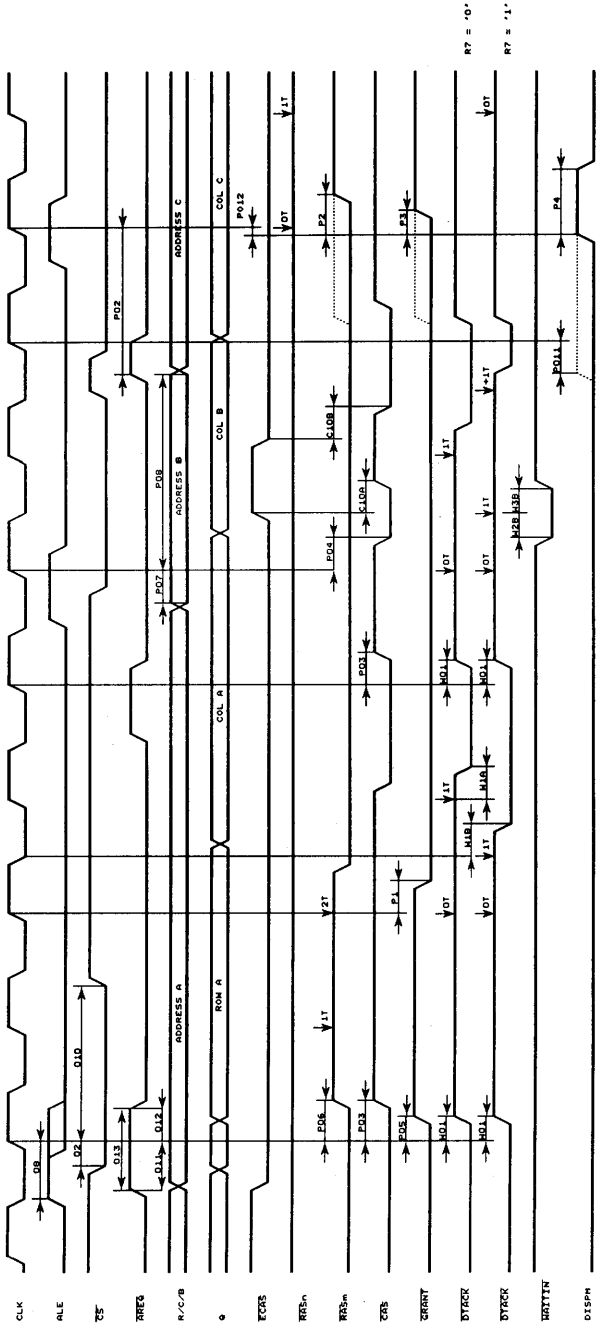


Figure 36. Page Access Mode Mode 1

MODE SETTING		
R0	0	2T tRP
R1	0	
R2	0	2T NON BURST
R3	1	
R4	0	1T BURST
R5	1	
R6	X	
R7	0	CLK RISING EDGE
R8	1	NON INTERL.
R9	X	
C0	X	
C1	X	
C2	X	
C3	X	
C4	0	RAS/CAS PAIRS
C5	1	
C6	0	
C7	X	
C8	X	
C9	1	DELAY CAS (MIN)
B0	X	
B1	1	ASYN MODE 1
ECAS0	0	
ECAS1	0	
ECAS2	1	PAGE MODE
ECAS3	0	

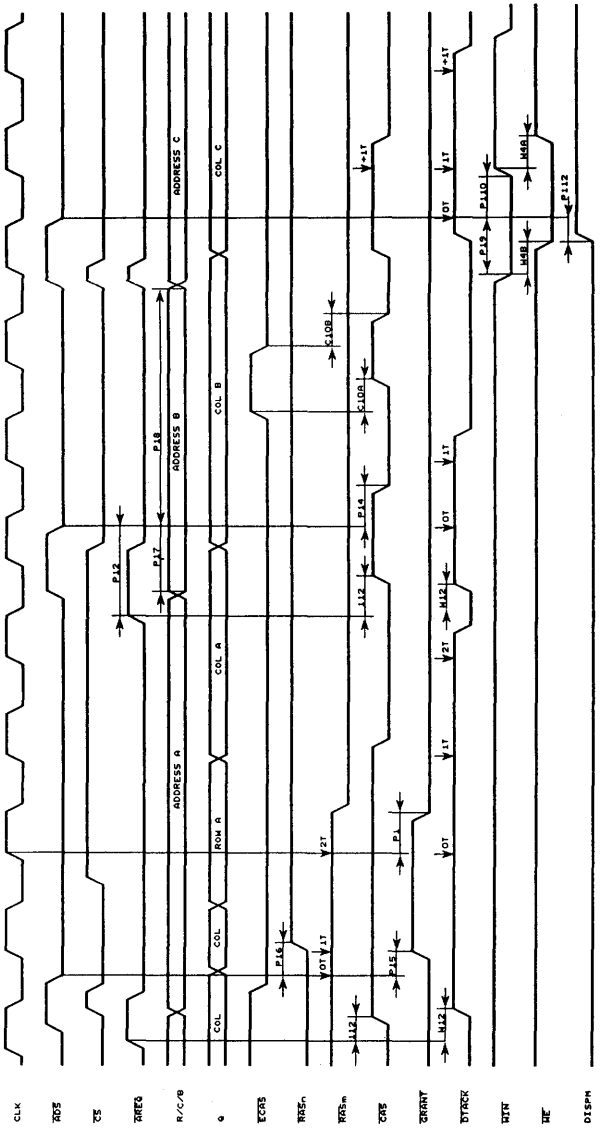


Figure 37. 68030 Burst Access Mode with Nibble Mode DRAMs

MODE SETTING		
R0	0	2T tRP
R1	0	
R2	0	2T NON BURST
R3	1	
R4	0	1T BURST
R5	1	
R6	0	ADD 1T
R7	0	CLK RISING EDGE
R8	1	NON INTERL.
R9	X	
C0	X	
C1	X	
C2	X	
C3	X	
C4	0	RAS/CAS PAIRS
C5	1	
C6	0	
C7	X	
C8	X	
C9	X	
R0	X	
R1	1	ASYN MODE 1
ECAS0	0	
ECAS1	1	68030 MODE
ECAS2	0	
ECAS3	0	

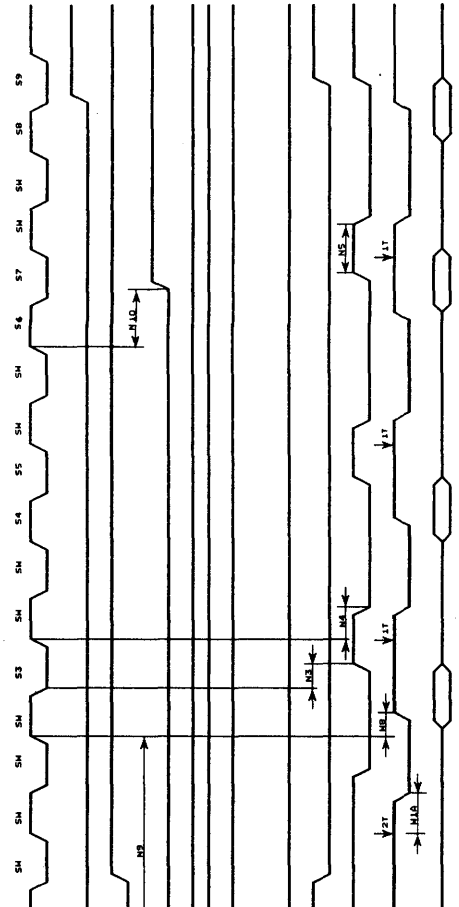


Figure 38. 68030 Burst Access Mode with Page Mode DRAMs

MODE SETTING		
R0	0	2T tRP
R1	0	
R2	0	1T NON BURST
R3	0	
R4	0	1T BURST
R5	1	
R6	1	DEFER DTACK
R7	0	CLK RISING EDGE
R8	1	NON INTERL.
R9	X	
C0	X	
C1	X	
C2	X	
C3	X	
C4	0	RAS/CAS PAIRS
C5	1	
C6	0	
C7	X	
C8	X	
C9	X	
B0	X	
B1	1	ASYN MODE 1
ECAS0	0	
ECAS1	1	68030 MODE
ECAS2	1	PAGE MODE
ECAS3	0	

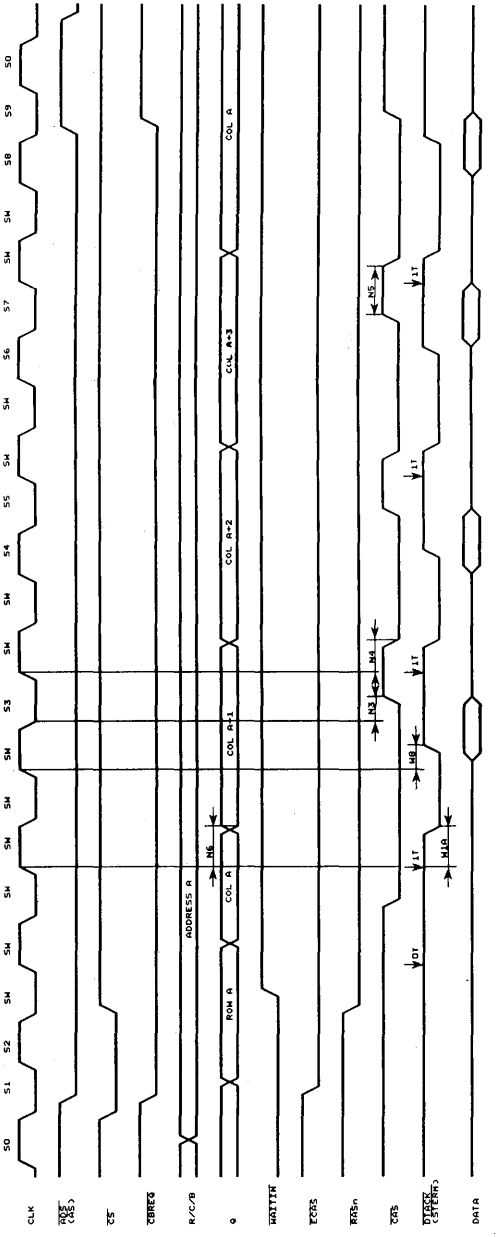


Figure 39. Burst Access Mode with Page Mode DRAMs (68040, 80486) Mode 1

MODE SETTING		
R0	0	2T tRP
R1	0	
R2	0	1T NON BURST
R3	0	
R4	0	1T BURST
R5	1	
R6	1	DEFER DTACK
R7	0	CLK RISING EDGE
R8	1	NON INTERL.
R9	X	
C0	X	
C1	X	
C2	X	
C3	X	
C4	0	RAS/CAS PAIRS
C5	1	
C6	0	
C7	X	
C8	X	
C9	1	DELAY CAS (MIN)
B0	0	ADDRESS LATCH
B1	1	ASYN MODE 1
ECAS0	0	
ECAS1	0	
ECAS2	1	PAGE MODE
ECAS3	1	BURST MODE

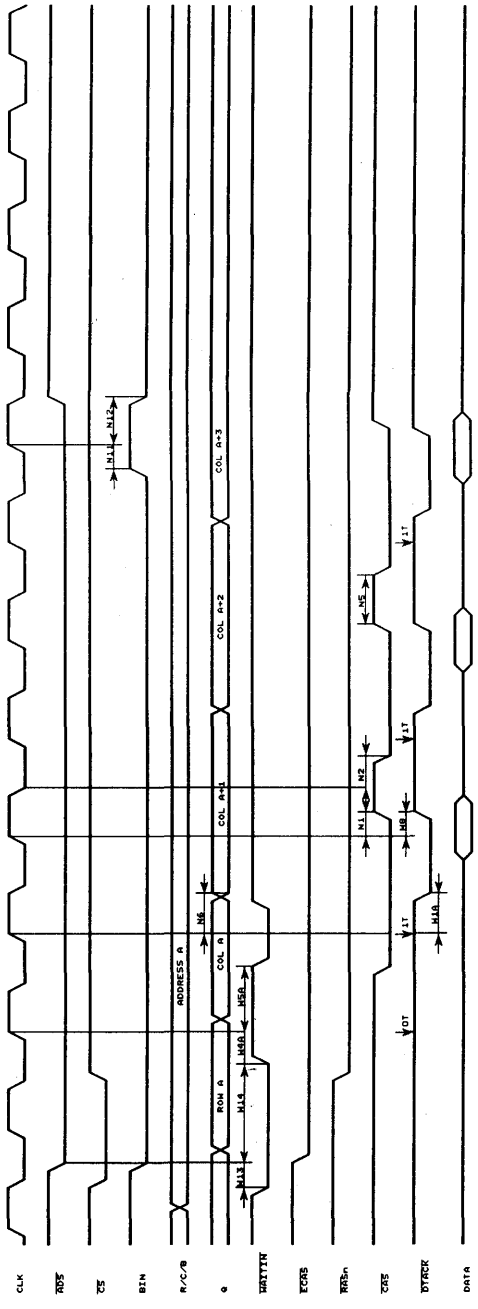


Figure 40. 68040 Burst Access Mode with Static Column DRAMs

MODE SETTING		
R0	0	2T tRP
R1	0	
R2	0	1T NON BURST
R3	0	
R4	0	1T BURST
R5	1	
R6	0	ADD 1T
R7	0	CLK RISING EDGE
R8	1	NON INTERL.
R9	X	
C0	X	
C1	X	
C2	X	
C3	X	
C4	0	RAS/CAS PAIRS
C5	1	
C6	0	
C7	X	
C8	X	
C9	1	DELAY CAS (MIN)
R0	0	ADDRESS LATCH
R1	0	SYN MODE 0
ECAS0	0	
ECAS1	0	
ECAS2	0	
ECAS3	1	BURST MODE

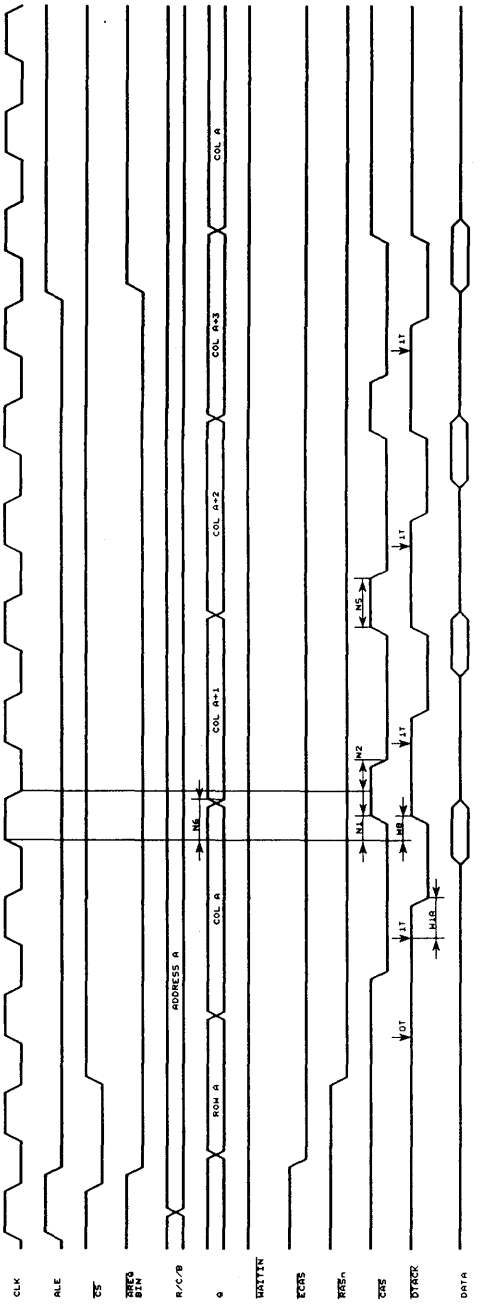


Figure 41. 68040 Burst Access Mode
Mode 0 DELAY $\overline{CAS}$ During Burst Write

MODE SETTING		
R0	0	2T tRP
R1	0	
R2	0	1T NON BURST
R3	0	
R4	0	1T BURST
R5	1	
R6	0	ADD 1T
R7	0	CLK RISING EDGE
R8	1	NON INTERL.
R9	X	
C0	X	
C1	X	
C2	X	
C3	X	
C4	0	RAS/CAS PAIRS
C5	1	
C6	0	
C7	X	
C8	X	
C9	1	DELAY CAS (MIN)
B0	0	ADDRESS LATCH
B1	0	SYN MODE 0
ECAS0	0	
ECAS1	0	
ECAS2	0	
ECAS3	1	BURST MODE

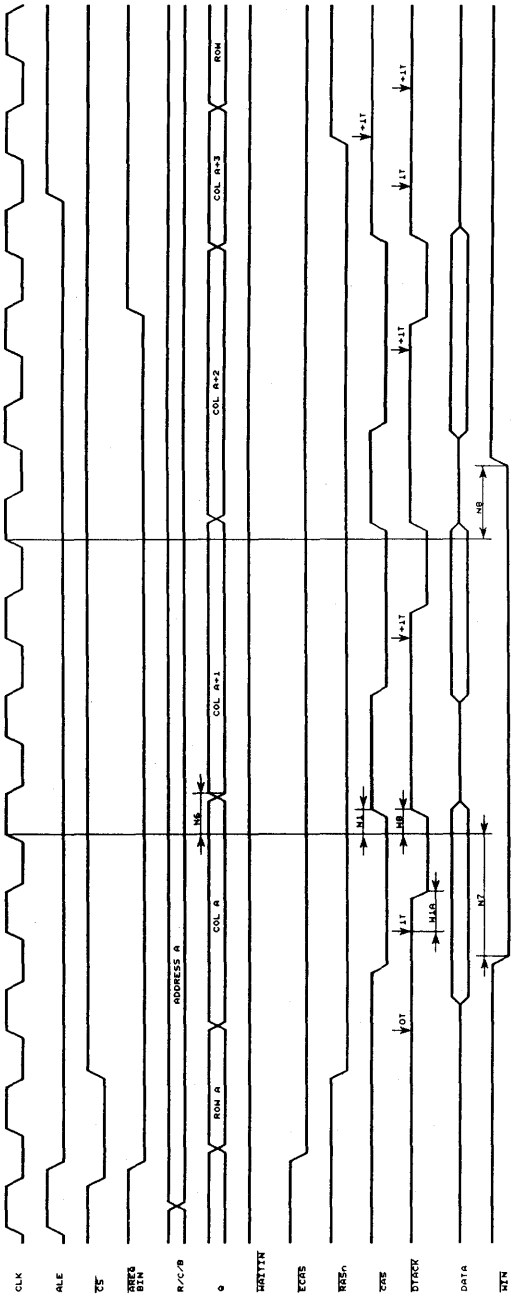


Figure 42. Mode Load by Fake Access

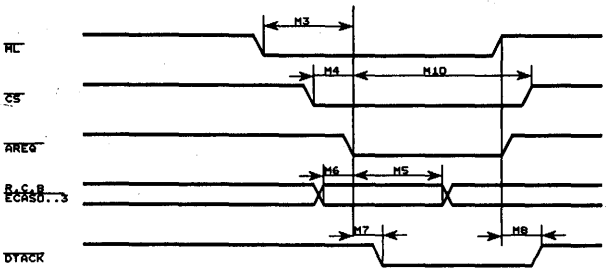


Figure 43. Mode Load Controlled by Mode Load Input Only

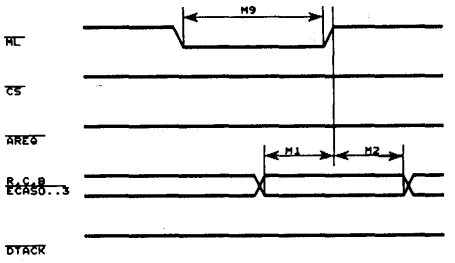


Figure 44. REFRESH, Single Access Mode Burst Mode

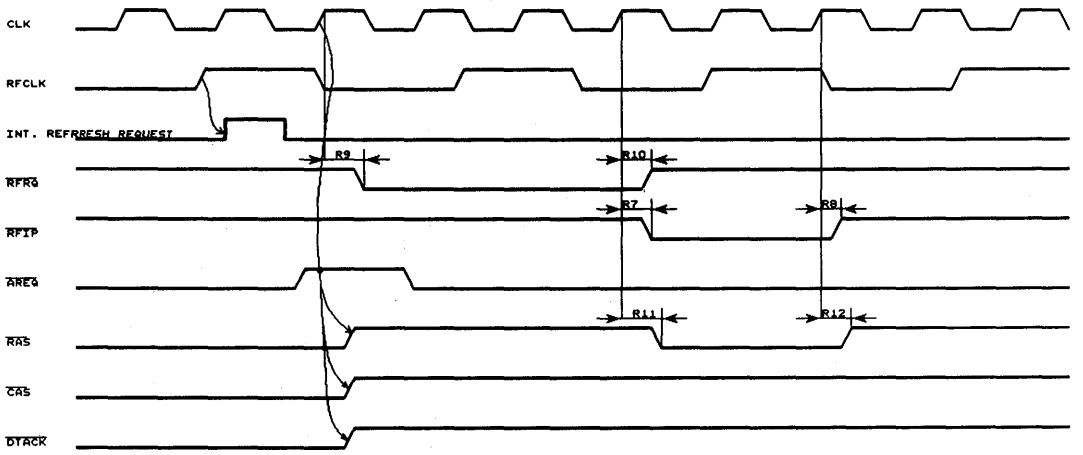


Figure 45. REFRESH in Page Mode

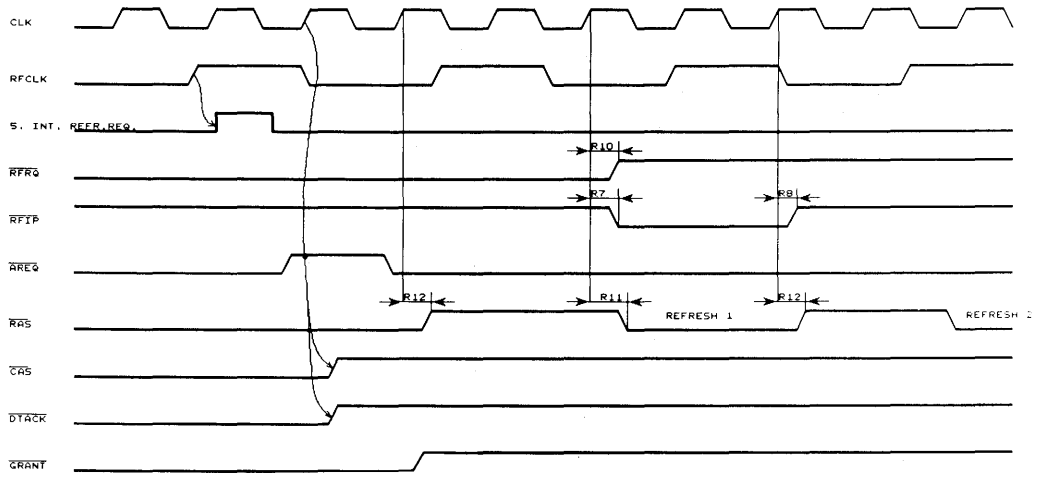


Figure 46. REFRESH with Extend Refresh

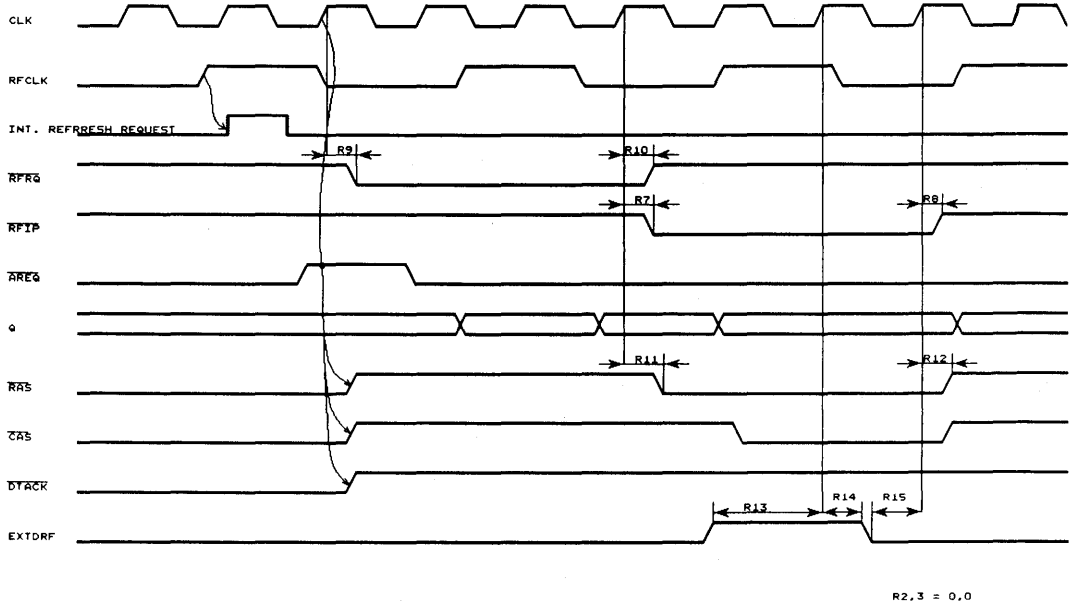


Figure 47. Page Mode REFRESH with Extend Refresh

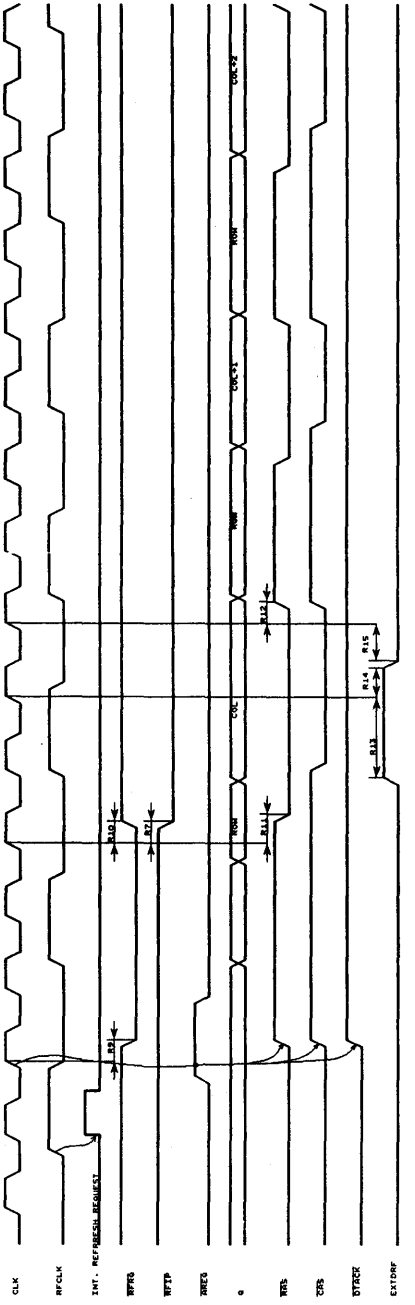


Figure 48. External Controlled Refresh

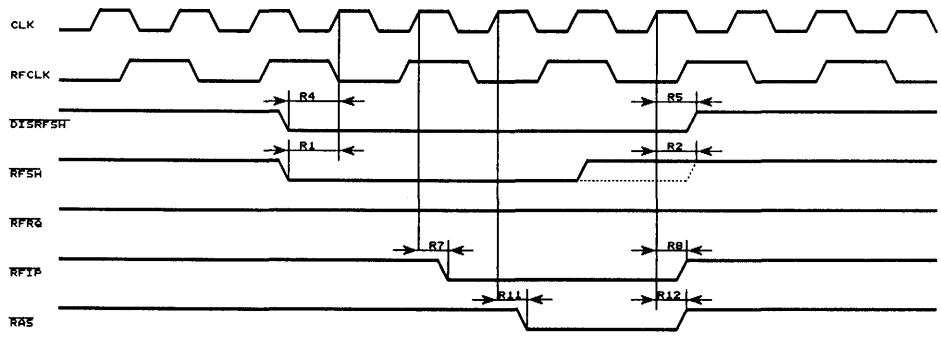


Figure 49. External Controlled Refresh ($\overline{ECAS0}$ = '0')

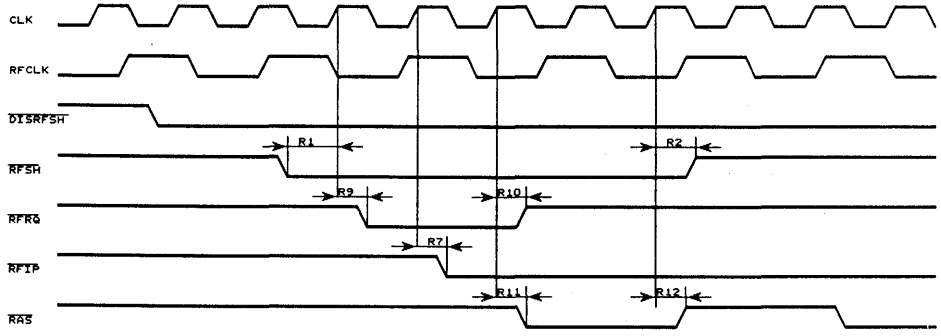


Figure 50. Page Mode — Disable Page Mode and Internal Refresh

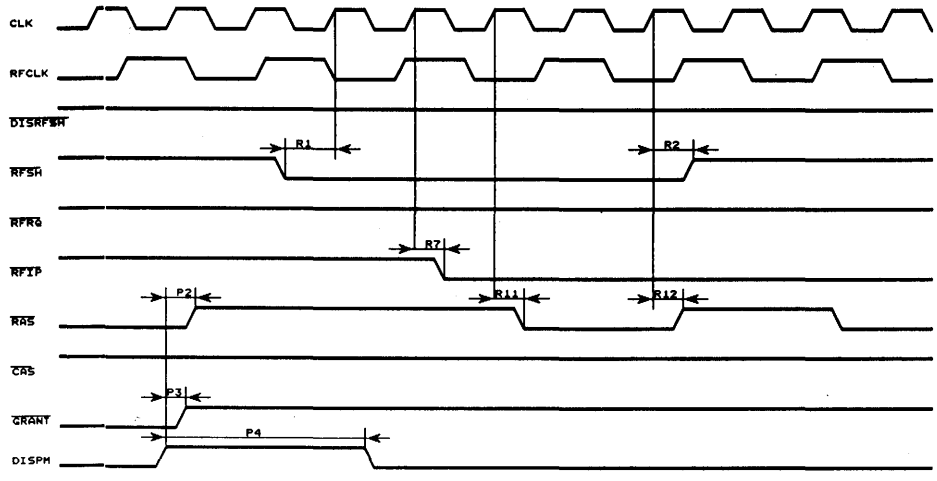


Figure 51. Staggered Refresh

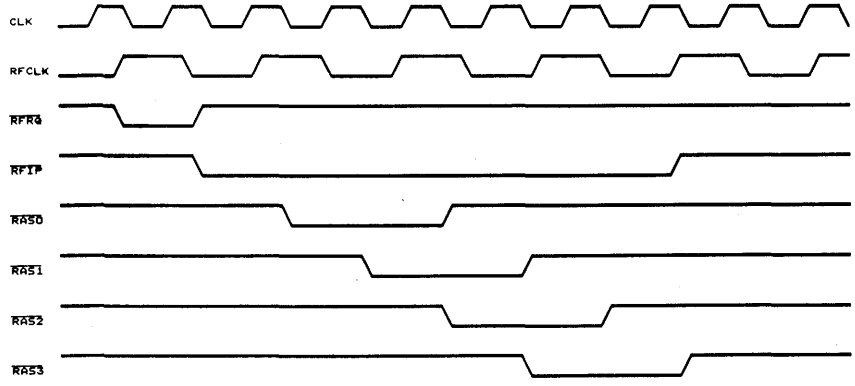


Figure 52. Access Cycle Termination

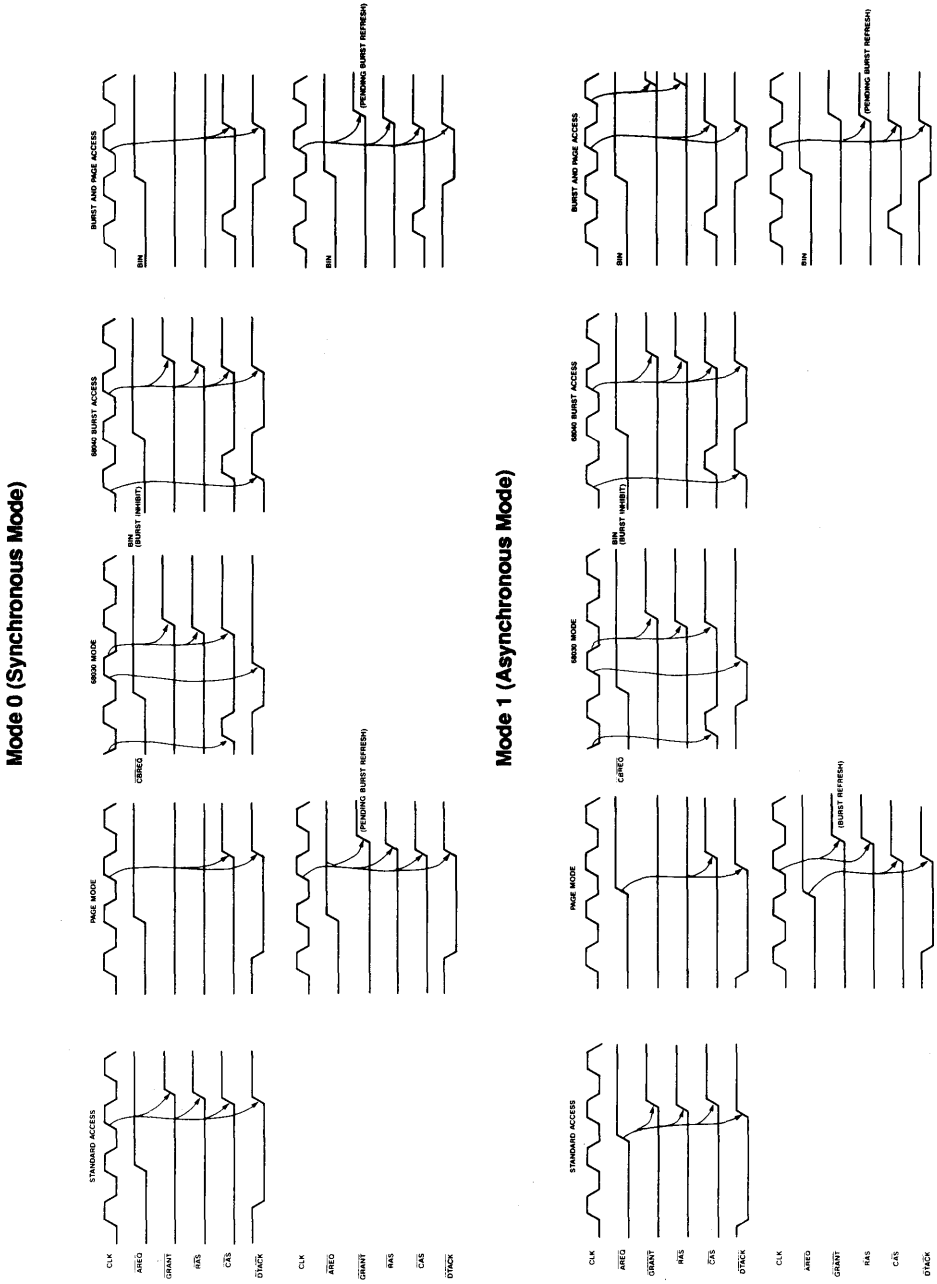
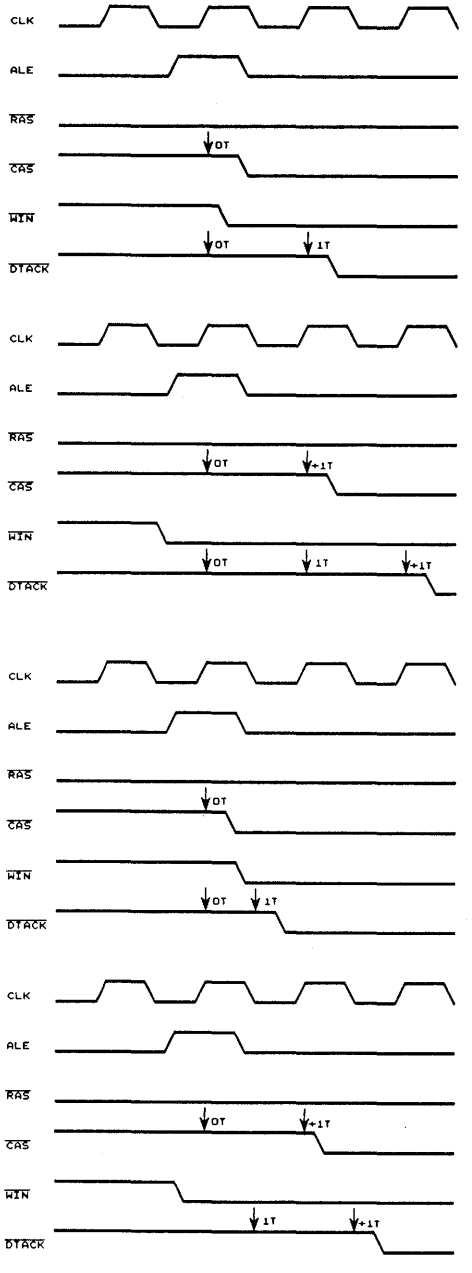


Figure 52. Access Cycle Termination (Continued)

Page Mode — Mode 0



Page Mode — Mode 1

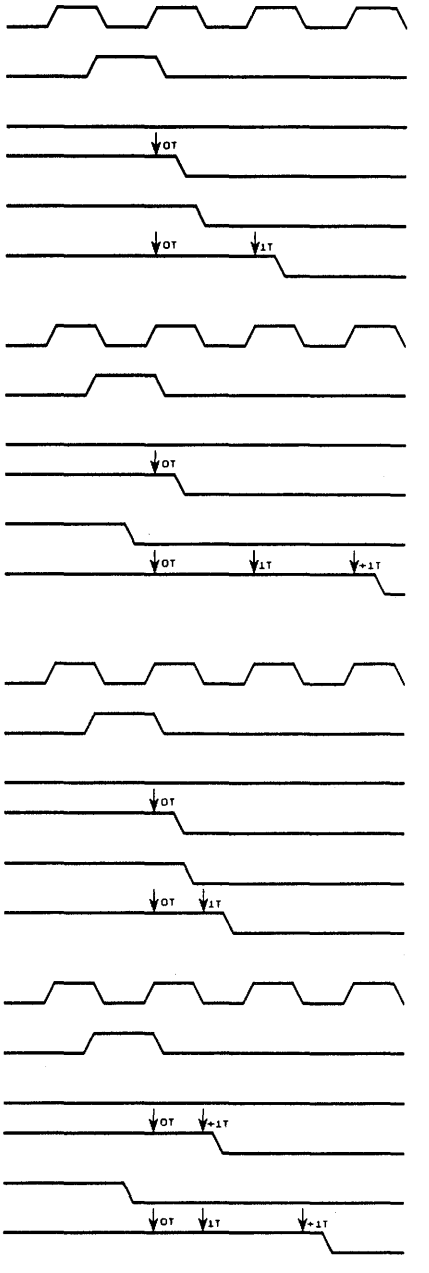


Figure 52. Access Cycle Termination (Continued)

68030 Mode

68040 Burst Mode

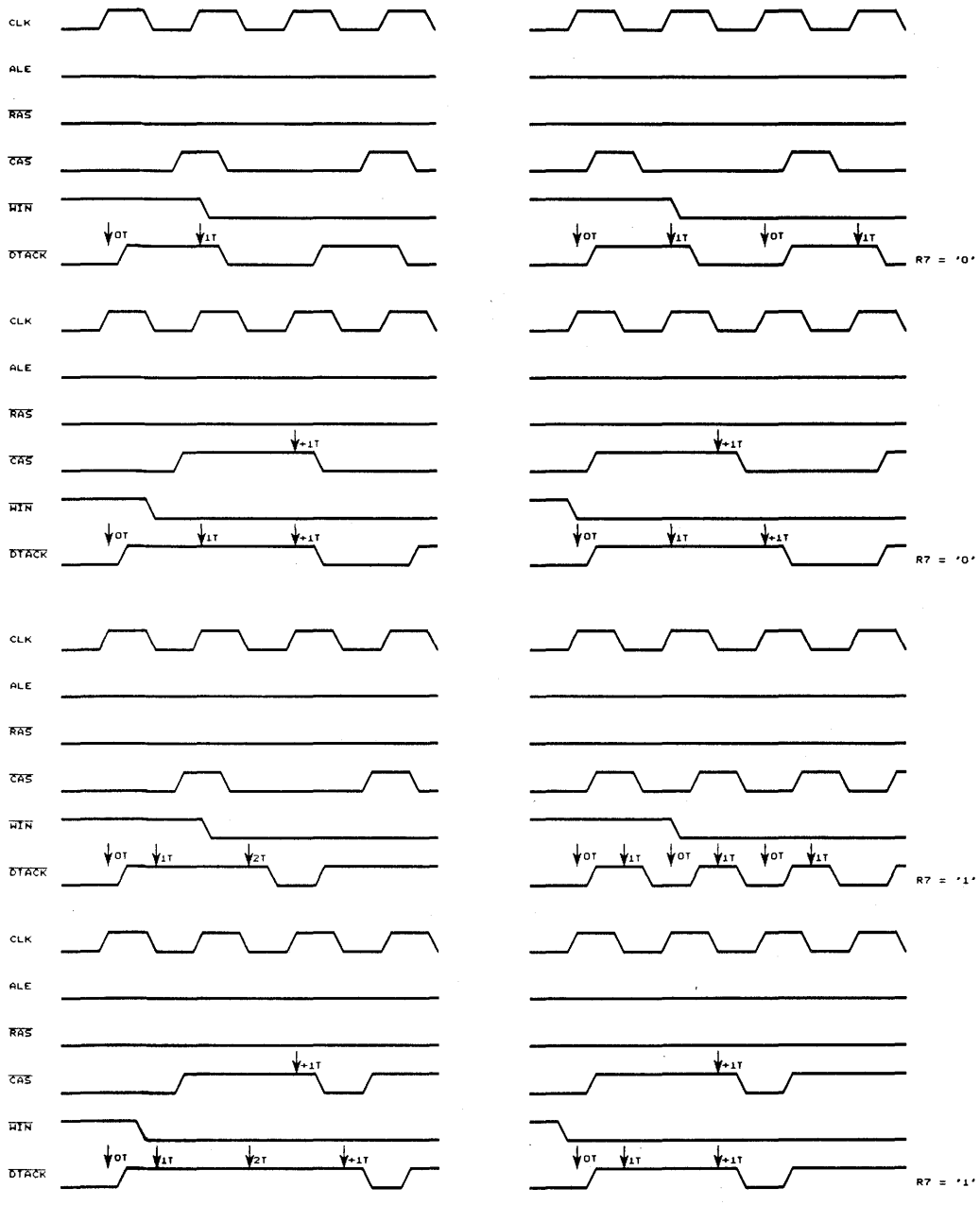


Figure 52. Access Cycle Termination (Continued)

68030 Mode

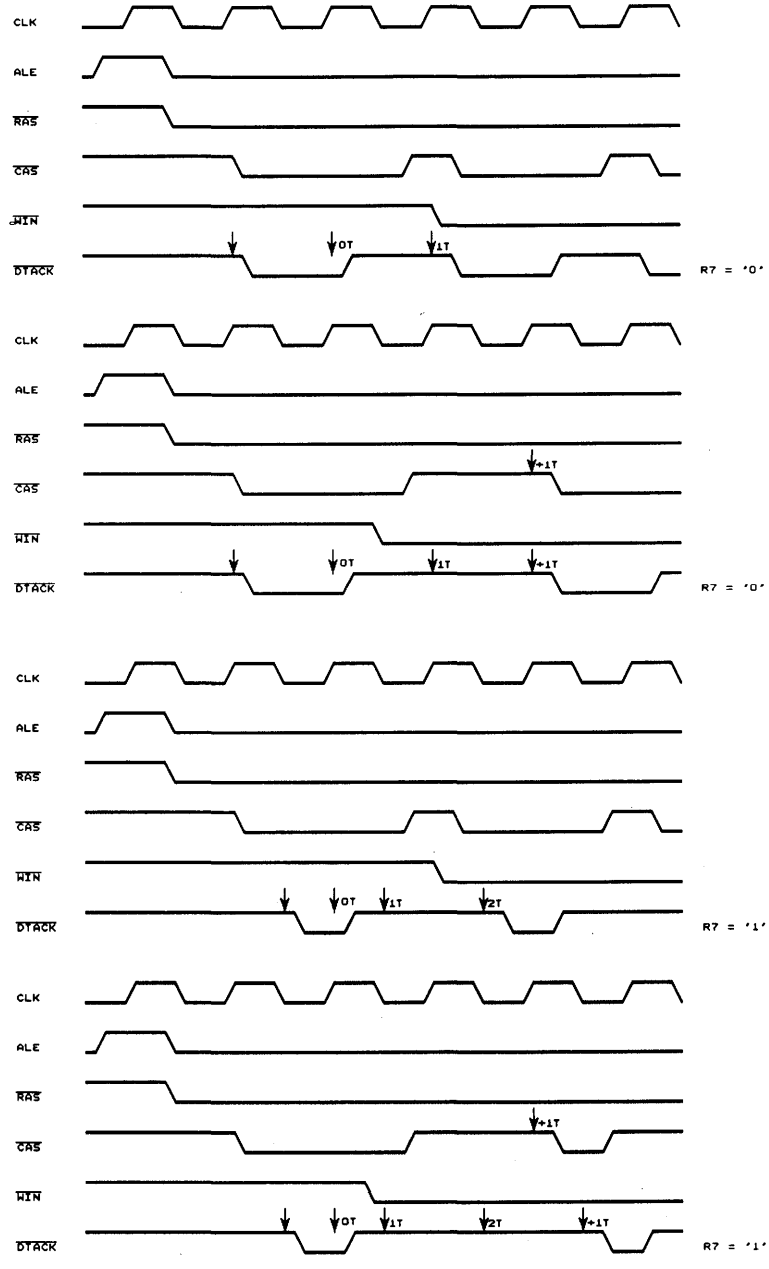
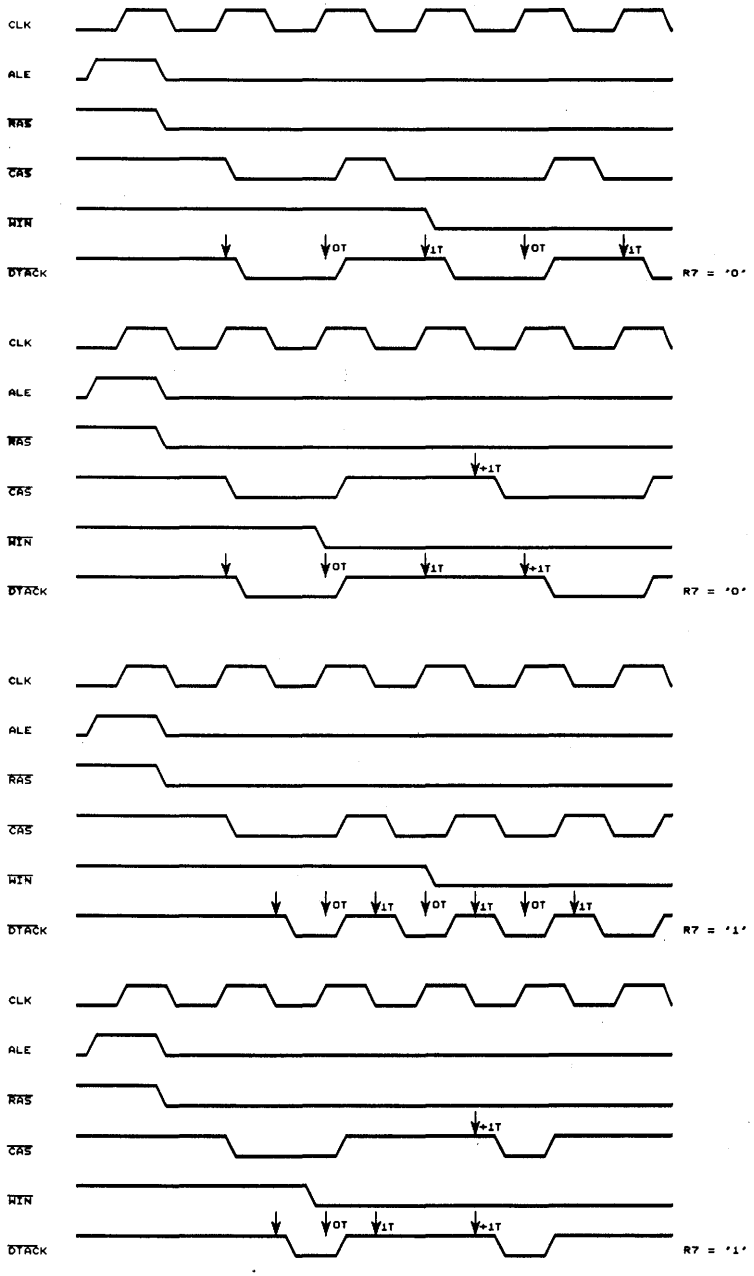


Figure 52. Access Cycle Termination (Continued)

68040 Burst Mode



Mode 0 Parameters

	Parameter	-25		-33	
		Min	Max	Min	Max
01	ALE minimum low time	10		10	
02	$\overline{CS}$ to access start setup	3		3	
03	Access start to $\overline{RAS}$ asserted		35		30
04	Address setup to access start to guarantee 0ns row address setup time	8		6	
05	Address hold time fromALE low using the on chip latch	20		20	
06	Access start to $\overline{CAS}$ asserted				
a	t_{RAH} = 12ns, t_{ASC} = 0ns	50	85	50	80
b	t_{RAH} = 12ns, t_{ASC} = 10ns	60	95	60	90
c	t_{RAH} = 20ns, t_{ASC} = 0ns	60	95	60	90
d	t_{RAH} = 20ns, t_{ASC} = 10ns	70	105	70	100
07	Access start to column address				
a	t_{RAH} = 12ns		75		70
b	t_{RAH} = 20ns		85		80
08	ALE high to CLK rising edge	10		7	
09	ALE pulse width	12		10	
010	$\overline{CS}$ hold after access start	10		10	
011	$\overline{AREQ}$ to CLK rising edge setup time	12		8	
012	$\overline{AREQ}$ from CLK rising edge hold time	2		2	
014	CLK rising edge to $\overline{RAS}$ deasserted		35		30
015	CLK rising edge to $\overline{CAS}$ deasserted		25		20
016	CLK rising edge to $\overline{GRANT}$ deasserted		20		18
017	ALE negated from CLK rising edge	0		0	

Mode 0 Page Mode Related Parameters

	Parameter	-25		-33	
		Min	Max	Min	Max
P01	Access start (CLK rising edge) to $\overline{GRANT}$ asserted (non-delayed access)		20		10
P02	$\overline{AREQ}$ high setup to access start to guarantee $\overline{CAS}$ will stay high in case of page miss	10+1T		8+1T	
P03	CAS deasserted from CLK rising edge	5	20	4	18
P04	Access Start to $\overline{CAS}$ low if page hit	5	25	4	20
P05	$\overline{GRANT}$ high from access start in case of page miss		20		18
P06	$\overline{RAS}$ high from access start in case of a page miss	8	35	5	30
P07	Row and bank address set up to assure a page miss is recognized		8		6
P08	Row and bank address hold from access start		20		20
P09	$\overline{WIN}$ low set up to access start (C9 = '1')	8		6	
P010	$\overline{WIN}$ low hold time from access start (C9 = '1')	2		2	
P011	DISPM high setup to CLK rising edge	15		10	
P012	DISPM asserted to access start	15		10	

Mode 1 Parameters

	Parameter	-25		-33	
		Min	Max	Min	Max
11					
a	Access start to CLK rising edge (R7 = '0')	5		4	
b	Access start to CLK falling edge (R7 = '1')	5		4	
12	$\overline{CS}$ to access start setup	3		3	
13	Access start to $\overline{RAS}$ asserted		35		30
14	Address setup to access start to guarantee 0ns row address setup time	8		6	
15	Address hold time from access start using the on chip latch	20		20	
16	Access start to $\overline{CAS}$ asserted				
a	t_{RAH} = 12ns, t_{ASC} = 0ns	50	85	50	80
b	t_{RAH} = 12ns, t_{ASC} = 10ns	60	95	60	90
c	t_{RAH} = 20ns, t_{ASC} = 0ns	60	95	60	90
d	t_{RAH} = 20ns, t_{ASC} = 10ns	70	105	70	100
17	Access start to column address				
a	t_{RAH} = 12ns		75		70
b	t_{RAH} = 20ns		85		80
18	$\overline{AREQ}$ rising edge to CLK rising edge to be recognized as 1T of $\overline{RAS}$ precharge	12		10	
19	$\overline{ADS}$ pulse width	12		10	
110	$\overline{CS}$ hold after access start	10		10	
111	$\overline{AREQ}$ deasserted to $\overline{RAS}$ deasserted		35		30
112	$\overline{AREQ}$ deasserted to $\overline{CAS}$ deasserted	5	25	4	20
113	$\overline{GRANT}$ deasserted from $\overline{AREQ}$ high		20		18
114	$\overline{AREQ}$ asserted	10		8	
115	$\overline{AREQ}$ pulse width	12		10	
116	$\overline{AREQ}$ rising edge to access start (R8 = '1' non interleave)	15		10	

Mode 1 Page Mode Related Parameters

	Parameter	-25		-33	
		Min	Max	Min	Max
P11	Access start ($\overline{ADS}$ falling edge) to $\overline{GRANT}$ low		20		18
P12	$\overline{AREQ}$ high set-up to access start to guarantee $\overline{CAS}$ will stay high in case of page miss	20		15	
P13	$\overline{AREQ}$ rising edge to $\overline{CAS}$ deasserted	5	20	4	18
P14	Access start to $\overline{CAS}$ low if page hit		25		20
P15	$\overline{GRANT}$ high from $\overline{ADS}$ falling edge if page miss is detected		20		18
P16	$\overline{RAS}$ high from access start in case of a page miss		35		30
P17	Row and bank address set up to assure a page miss is recognized		10		8
P18	Row and bank address hold from access start		20		20
P19	$\overline{WIN}$ low set up to access start (C9 = '1')	8		6	
P110	$\overline{WIN}$ low hold time from access start (C9 = '1')	2		2	
P112	DISPM asserted to access start	15		10	

Common Parameters

	Parameter	-25		-33	
		Min	Max	Min	Max
C1	R, C input to Q output while ALE/$\overline{ADS}$ is high		35		30
C2	R, C input to Q output		35		30
C3	Row address hold time				
a	t_{RAH} = 12ns	15		12	
b	t_{RAH} = 20ns	25		20	
C4					
a	$\overline{WIN}$ high to $\overline{WE}$ high		40		35
b	$\overline{WIN}$ low to $\overline{WE}$ low		40		35
C5	Column address setup time				
a	t_{ASC} = 0ns	0		0	
b	t_{ASC} = 10ns	10		10	
C6	Column address hold time (interleave only)	25	40	25	40
C7	CLK rising edge to $\overline{RAS}$ asserted after delayed access		35		30
C8	CLK rising edge to $\overline{CAS}$ asserted after delayed access				
a	t_{RAH} = 12ns, t_{ASC} = 0ns	50	85	50	80
b	t_{RAH} = 12ns, t_{ASC} = 10ns	60	95	60	90
c	t_{RAH} = 20ns, t_{ASC} = 0ns	60	95	60	90
d	t_{RAH} = 20ns, t_{ASC} = 10ns	70	105	70	100
C9	CLK rising edge to $\overline{CAS}$ deasserted (mode C9 = '1')		25		20
C10					
a	$\overline{ECAS}$ high to $\overline{CAS}$ high		25		20
b	$\overline{ECAS}$ low to $\overline{CAS}$ low		25		20
C11	CLK high	16		14	
C12	CLK low	16		14	
C13	CLK period	40		30	
C14	RFCLK high	16		16	
C15	RFCLK low	16		16	
C16	RFCLK period	40		40	
C17	CLK rising edge to column address				
a	t_{RAH} = 12ns		75		70
b	t_{RAH} = 20ns		85		80

Common Page Mode Related Parameters

	Parameter	-25		-33	
		Min	Max	Min	Max
P1	$\overline{GRANT}$ low from access start (defered access)		20		18
P2	DISPM rising edge to $\overline{RAS}$ negated		25		25
P3	DISPM rising edge to $\overline{GRANT}$ negated		25		20
P4	DISPM high pulse width	15		15	

Common Wait State Parameters

	Parameter		-25 Min	-25 Max	-33 Min	-33 Max
W1						
a	CLK rising edge to $\overline{\text{DTACK}}$ low	(R7 = '0')		20		18
b	CLK falling edge to $\overline{\text{DTACK}}$ low	(R7 = '1')		20		18
W2						
a	$\overline{\text{WAITIN}}$ setup to CLK rising edge to add 1T	(R6 = '0', R7 = '0')	10		8	
b	$\overline{\text{WAITIN}}$ setup to CLK falling edge to add 1T	(R6 = '0', R7 = '1')	10		8	
W3						
a	$\overline{\text{WAITIN}}$ hold time from clock rising edge	(R6 = '0', R7 = '0')	5		5	
b	$\overline{\text{WAITIN}}$ hold time from clock falling edge	(R6 = '0', R7 = '1')	5		5	
W4	$\overline{\text{WAITIN}}$ high setup time to	(R6 = '1')				
a	CLK rising edge	(R7 = '0')	0		0	
b	CLK falling edge	(R7 = '1')	0		0	
W5	$\overline{\text{WAITIN}}$ high hold time from	(R6 = '1')				
a	CLK rising edge	(R7 = '0')	15		15	
b	CLK falling edge	(R7 = '1')	15		15	
W7	$\overline{\text{WAITIN}}$ low hold time from	(R6 = '1')				
a	CLK rising edge	(R7 = '0')	10		10	
b	CLK falling edge	(R7 = '1')	10		10	
W8	CLK rising edge to $\overline{\text{DTACK}}$ deasserted (burst mode)			20		18

Mode 0 Wait State Parameters

	Parameter		-25 Min	-25 Max	-33 Min	-33 Max
W01	CLK rising edge to $\overline{\text{DTACK}}$ high			20		18
W02	$\overline{\text{WAITIN}}$ low setup to access start	(R6 = '1')	5		5	
W03	$\overline{\text{WAITIN}}$ low hold time from access start	(R6 = '1')	10		10	

Mode 1 Wait State Parameters

	Parameter		-25 Min	-25 Max	-33 Min	-33 Max
W12	$\overline{\text{AREQ}}$ rising edge to $\overline{\text{DTACK}}$ deasserted		5	20	4	18
W13	$\overline{\text{WAITIN}}$ low setup to access start	(R6 = '1')	5		5	
W14	$\overline{\text{WAITIN}}$ low hold time from access start	(R6 = '1')	10		10	

Mode Load Parameters

	Parameter	-25		-33	
		Min	Max	Min	Max
M1	Mode address setup time	5		5	
M2	Mode address hold time	5		5	
M3	$\overline{ML}$ asserted to $\overline{AREQ}$ asserted	10		10	
M4	$\overline{CS}$ asserted to $\overline{AREQ}$ asserted	5		5	
M5	Mode address hold time from $\overline{AREQ}$ asserted	20		20	
M6	Mode address setup time to $\overline{AREQ}$ asserted	5		5	
M7	$\overline{AREQ}$ asserted to $\overline{DTACK}$ asserted		15		15
M8	$\overline{AREQ}$ or $\overline{ML}$ deasserted to $\overline{DTACK}$ deasserted		15		15
M9	$\overline{ML}$ pulse width	20		20	
M10	$\overline{CS}$ hold time from $\overline{AREQ}$ falling edge (for "fake access")	10		10	

Burst Mode Parameters

	Parameter		-25		-33	
			Min	Max	Min	Max
N1	CLK rising edge to $\overline{CAS}$ deasserted	($\overline{ECAS3}$ = '1')	5	25	4	20
N2	CLK falling edge to $\overline{CAS}$ asserted	($\overline{ECAS3}$ = '1')	5	25	4	20
N3	CLK falling edge to $\overline{CAS}$ deasserted	($\overline{ECAS1}$ = '1')	5	25	4	20
N4	CLK rising edge to $\overline{CAS}$ asserted	($\overline{ECAS1}$ = '1')	5	25	4	20
N5	$\overline{CAS}$ high pulse width		12		10	
N6	CLK rising/falling edge to column + 1 output	(B0 = '0')	5	38	4	33
N7	$\overline{WIN}$ low set up to CLK rising edge	(C9 = '1')	15		10	
N8	$\overline{WIN}$ low hold time from CLK rising edge	(C9 = '1')	5		5	
N9	$\overline{CBREQ}$ setup to CLK rising edge that negates $\overline{DTACK}$		10		8	
N10	$\overline{CBREQ}$ hold time form CLK rising edge that negates $\overline{DTACK}$		2		2	
N11	BIN setup to CLK rising edge		12		8	
N12	BIN hold time from CLK rising edge		2		2	

Refresh Related Parameters

	Parameter	-25		-33	
		Min	Max	Min	Max
R1	$\overline{RFSH}$ low setup time to CLK rising edge	10		10	
R2	$\overline{RFSH}$ low hold time from CLK rising edge	2		2	
R3	$\overline{RFSH}$ pulse width for resetting refresh counter	15		15	
R4	$\overline{DISRFSH}$ low setup to CLK rising edge	10		10	
R5	$\overline{DISRFSH}$ low hold time to CLK rising edge	2		2	
R6	$\overline{DISRFSH}$ low pulse width	15		15	
R7	CLK rising edge to $\overline{RFIP}$ asserted		15		15
R8	CLK rising edge to $\overline{RFIP}$ asserted		15		15
R9	CLK rising edge to $\overline{RFRQ}$ asserted		15		15
R10	CLK rising edge to $\overline{RFRQ}$ deasserted		15		15
R11	CLK rising edge to refresh $\overline{RAS}$ asserted		25		25
R12	CLK rising edge to refresh $\overline{RAS}$ deasserted		25		25
R13	EXTDRF setup to CLK rising edge	10		10	
R14	EXTDRF hold time from CLK rising edge	2		2	
R15	EXTDRF low setup to CLK rising edge	0		0	

PACKAGE DIMENSIONS

The Samsung KS84CXX DRAM Controllers are available in two packages. The KS84C31 68-Pin PLCC package is shown in Figure 53, while the 84-Pin version is shown in Figure 54.

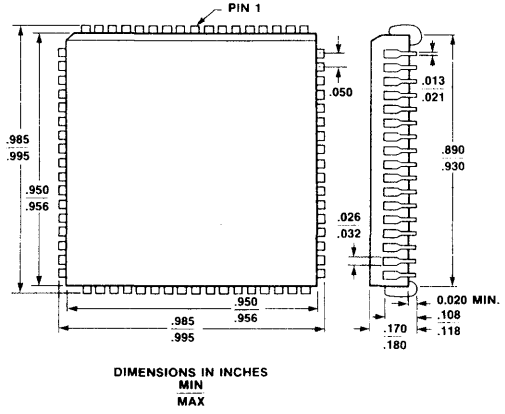


Figure 53. 68-Pin PLCC Package

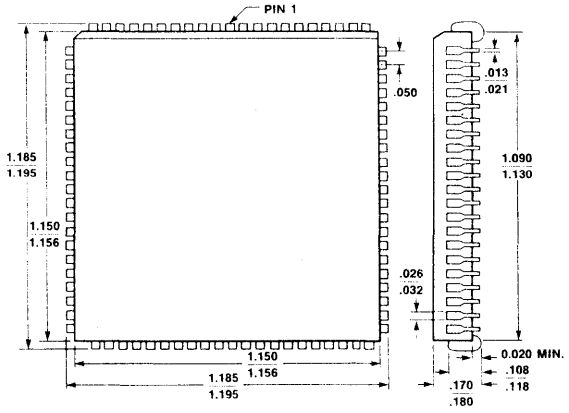
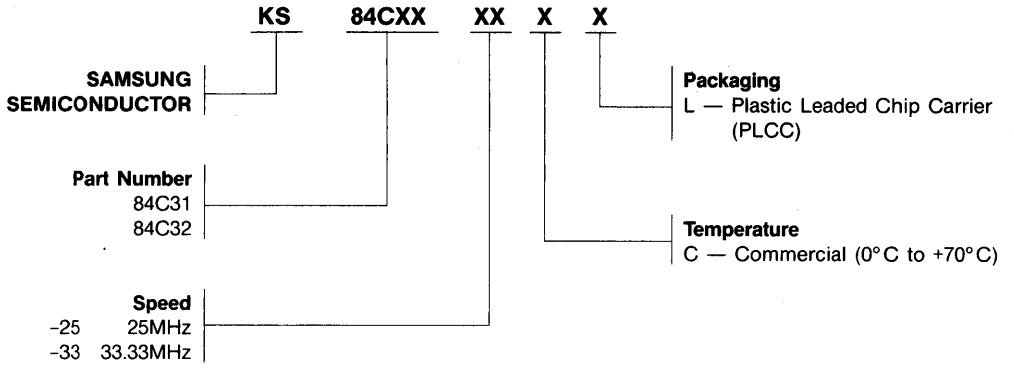


Figure 54. 84-Pin PLCC Package

ORDERING INFORMATION AND PRODUCT CODE



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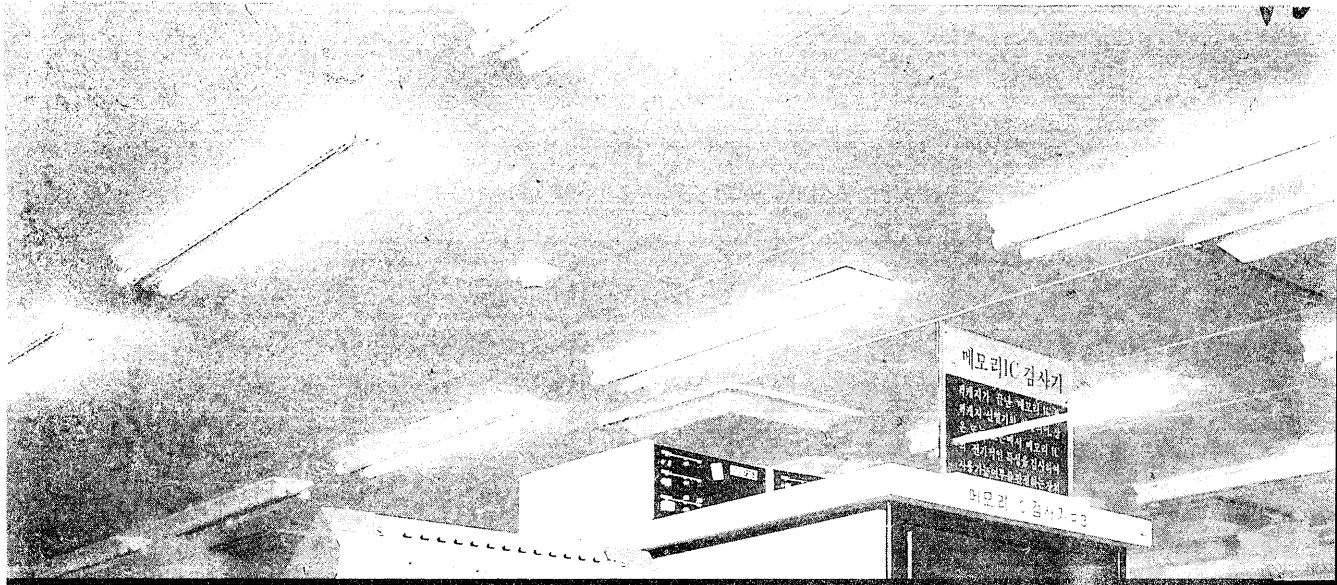

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