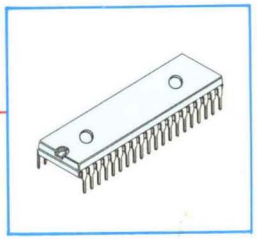
SAMSUNG

Data Book

Linear IC

VOL. 3, 1989



•Data Converter IC

SAMSUNG Linear IC Data Book Vol. 3 (Data Converter IC) 1989

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DATA BOOK LIST

I. Semiconductor Product Guide

II. Transistor Data Book

Vol. 1: Small Signal TR
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**: Under Development

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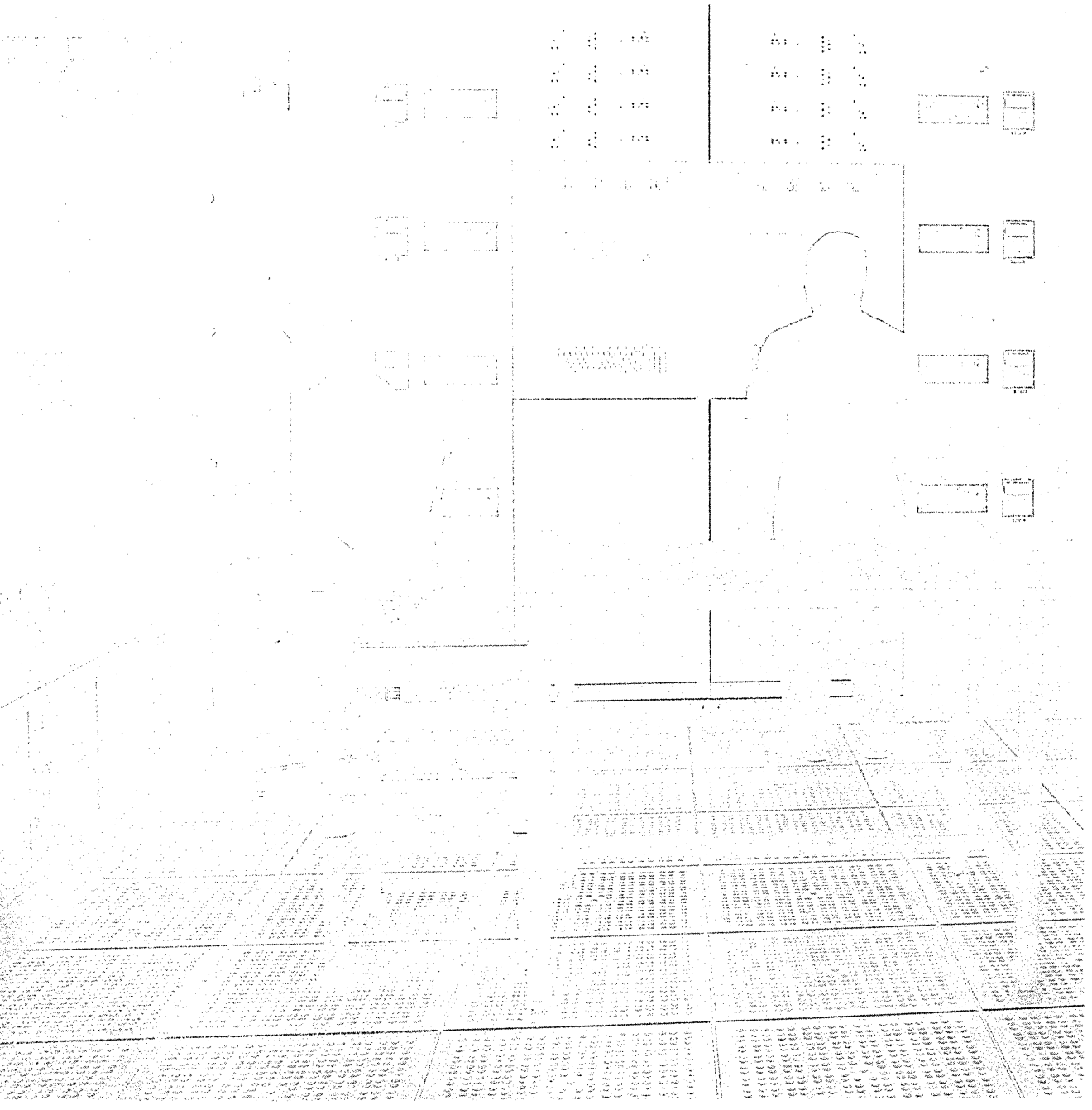


1. FUNCTION GUIDE

Function	Device	Package	Feature	Application
A/D + D/A Converter	KSV3100A	40 DIP	High speed 8 bit A/D + 10 bit D/A	Image processing video graphics
	*KSV3110	40 DIP	Enhanced version of KSV3100A	
A/D Converter	*KSV3200	26 DIP	High speed 8 bit A/D converter	
	**KAD0206	30 SDIP 32 SOIC	High speed 6 bit A/D converter	
	KAD0808/9	28 DIP	8 bit up-interface A/D with 8 channel	General purpose
	*KAD0817	40 DIP	8 bit up-interface A/D with 16 channel	
	KAD0820	20 DIP	8 bit up-interface A/D converter	
DMM A/D	KS7126	40 DIP/60 FQP	3 1/2 digit A/D converter	DMM
	**KAD7000	48 QFP	2000-3000 CNT converter	
	**KAD7001	80 QFP	3200 CNT converter	
D/A Converter	*KDA3310	28 CERDIP	High speed 10 bit D/A	Image processing video graphics
	*KDA0406	28 SOIC 28 SDIP	High speed tripple 6 bit D/A converter	
	KDA0800/08	16 DIP	8 bit D/A converter	General purpose
S.A.R.	KS25002/03	16 DIP	6 bit CMOS S.A.R.	SAR of A/D converter
	KS25C04	24 SDIP	12 bit CMOS S.A.R.	

* New Product
** Under Development

2. CROSS REFERENCE GUIDE

Application	SAMSUNG	N.S.	TI	Intersil	Other	Remark
A/D + D/A Converter	KSV3100A				UVC3101 UVC3100	
	*KSV3110				UVC3130	Not Pin to Pin
High Speed A/D	*KSV3208 (8 bit)				CXA1096	Not Pin to Pin
	**KAD0206 (6 bit)				MB40576	Not Pin to Pin
8 bit A/D Converter	KAD0808/9	ADC0808/9	ADC0808/9			
	*KAD0817	ADC0817	ADC0817			
	KAD0820	ADC0820				
3-1/2 Digit A/D	KS7126			ICL 7126	TSC 7126	
High Speed D/A	*KDA3310 (10 bit)				TDC1016	Not Pin to Pin
	*KDA0406 (6 bit)					
8 bit D/A	KDA0800/08	DAC0800/08		AD1408	MC1408	
S.A.R.	KS25C02/03	DM25C02/03				
	KS25C04	DM2504				

* New Product
** Under Development

WHAT IS DATA CONVERTER

2

Introduction to A/D, D/A Converter

1. Preface

Digital and analog signal processing correspond to two fundamental, yet distinctly different, modes of information handling. In the analog case, the signals are handled in a nonquantized, continuously variable manner; in digital processing, they are quantized in binary bits, that is, in 1's and 0's. In many cases, it is necessary to interface these two fundamental means of signal processing and to convert the data from digital to analog or vice versa. This is accomplished by the use of digital-to-analog (D/A) and analog-to-digital (A/D) converter circuits.

In their natural state, all variables (such as current, voltage, pressure, distance, time) appear in analog form. However, for signal transmission and computation purposes, they are often handled in a digital manner. Therefore, the A/D and D/A converter can be considered to be a class of coding and decodig devices, respectively. The input to a D/A converter is a digital word of a prescribed number of bits, and the output is an analog voltage level uniquely corresponding to the input word. Conversely, the analog input applied to the A/D converter results in a digital word of a prescribed number of bits.

2. A/D Converter

Analog-to-digital converters, also called ADC's or encoders, employ a variety of different circuit techniques to implement the conversion function. The function of an A/D converter is to convert any analog quantity such as a voltage, or a current into a digital word. Figure 1 shows the very simplistic block diagram of an A/D converter circuit.

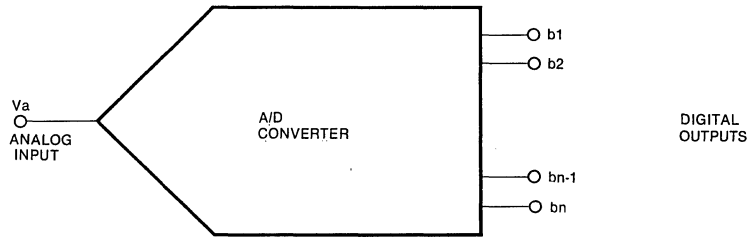


Fig. 1 Symbolic Block Diagram of A/D Converter

The A/D converter encodes an analog input into a digital output of predetermined bit length. The analog input voltage Va of figure 1 is approximated as a binary fraction of a full-scale output voltage Vfs. Thus, the output of the converter corresponds to an n-bit digital word D given as

$$\frac{Va}{Vfs} = \frac{b1}{2^1} + \frac{b2}{2^2} + \cdots\cdots + \frac{bn}{2^n}$$

where b1, b2, ..., bn are the binary bit coefficients having a value of either a 1 or a 0.

1) Successive-Approximation A/D Converters

Of the various A/D conversion techniques available, the choice depends on the resolution and speed required.

By far, the most popular A/D conversion technique in general use for moderate to high speed applicatioons is the successive-approximation type A/D. This method falls into a class of techniques known as feedback type A/D converters. In the successive-approximation converter, the DAC is controlled in an optimum manner to complete a conversion in just n-step, where n is the resolution of the converter in bits.

The operation of this converter is analogous to weighing an unknown on a laboratory balance scale using standard weights in a binary sequence such as 1, 1/2, 1/4, 1/8, ... , $1/2^{n-1}$. The correct procedure is to begin with the largest standard weight and proceed in order down to the smallest one.

The largest weight is placed on the balance pan first; if it does not tip, the weight is left on and the next largest weight is added. The same procedure is used for the next largest weight and so on down to the smallest. After the n'th standard weight has been tried and a decision made, the weighing is finished. The total of the standard weights remaining on the balance is the closest possible approximation to the unknown.

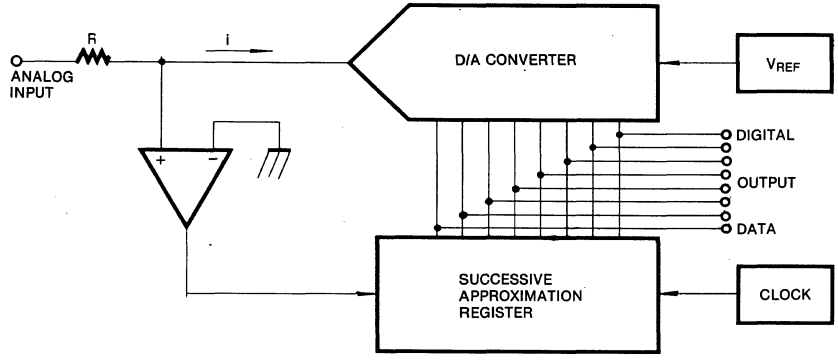


Fig. 2 Functional Block Diagram of Successive-Approximation A/D Converter.

In the successive-approximation A/D converter illustrated in Figure 2, a successive-approximation register (SAR) controls the D/A converter by implementing the weighting logic just described. The SAR first turns on the MSB of the DAC and the comparator tests this output against the analog input. A decision is made by the comparator to leave the bit on or turn it off after which bit 2 is turned on and a second comparision made. After n-comparisions the digital output of the SAR indicates all those bits which remain on and produces the desired digital code. The clock circuit controls the timing of the SAR. Fig. 3 shows the D/A converter output during a typical conversion.

The conversion efficiency of this technique means that high resolution conversions can be made in very short times. For example, it is possible to perform a 10 bit conversion in 1 μsec. or less and a 12 bit conversion in 2 μsec. or less. Of course the speed of the internal circuitry, in particular the D/A and comparator, are critical for high speed performance.

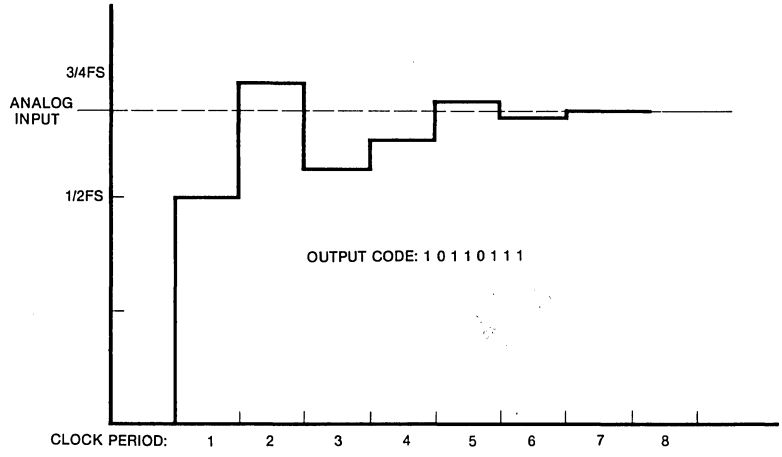


Fig. 3 D/A Output for 8-Bit Successive-Approximation Conversion

2) The Flash (Parallel) A/D Converter

For ultra-fast conversions required in video signal processing, image processing and radar applications where up to 8 bits or the more high bits resolution is required, a different technique is employed; it is known as the flash (also parallel) method and is illustrated in figure 4.

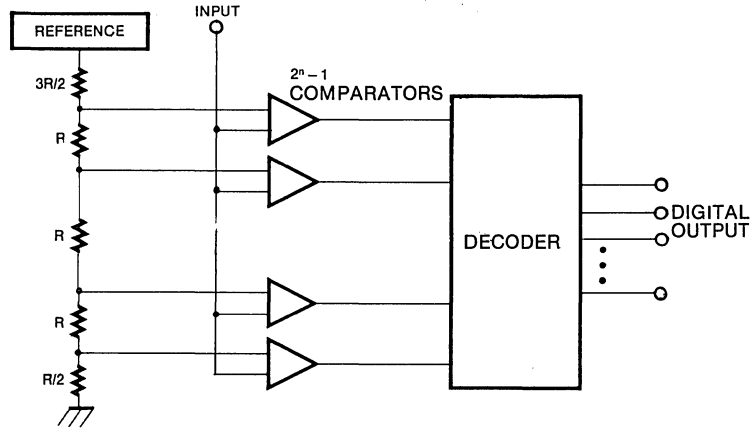


Fig. 4 Functional Block Diagram of Flash A/D Converter

This circuit employs $2^n - 1$ analog comparators to directly implement the quantizer transfer function of an A/D converter.

The comparator trip-points are spaced a LSB apart by the series resistor chain and voltage reference. For a given analog input voltage all comparators biased below the voltage turn on and all those biased above it remain off. Since all comparators change state simultaneously, the quantization process is a one-step operation.

A second step is required, however, since the logic output of the comparators is not in binary form.

Therefore an ultra-fast decoder circuit is employed to make the logic conversion to binary. The flash technique reaches the ultimate in high speed because only two sequential operations are required to make the conversion.

3) Subranging (Half-flash) A/D Converter

The limitation of the flash method, however, is in the large number of comparators required for even moderate resolutions. A 4-bit converter, for example, requires only 15 comparators, but an 8-bit converter needs 255. For this reason it is common practice to implement an 8-bit A/D with two 4-bit stage as shown in figure 5.

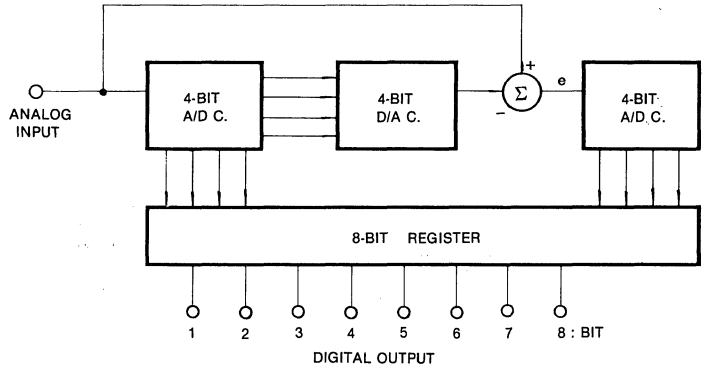


Fig. 5 Functional Block Diagram of Subranging A/D Converter

The result of the first 4-bit conversion is converted back to analog by means of an ultra-fast 4-bit D/A and then subtracted from the analog input. The resulting residue is then converted by the second 4-bit converter, and the two sets of data are accumulated in the 8-bit output register.

4) Integrating A/D Converter (Dual-slope A/D converter)

Integrating A/D converters perform the A/D conversion in an indirect manner. The analog input is first converted to a timing pulse whose duration is proportional to the analog voltage Va. The duration of the timing pulse is then measured in a digital format by counting the number of cycles of a stable reference frequency (the clock signal) between the beginning and the end of the timing pulse. Because of this basic principle of operation, such converters are often called indirect or pulse-width-modulating converters.

The dual-slope-type A/D converter is one of the most popular types of integrating A/D converters. Figure 6 shows the functional block diagram of a dual-slope converter.

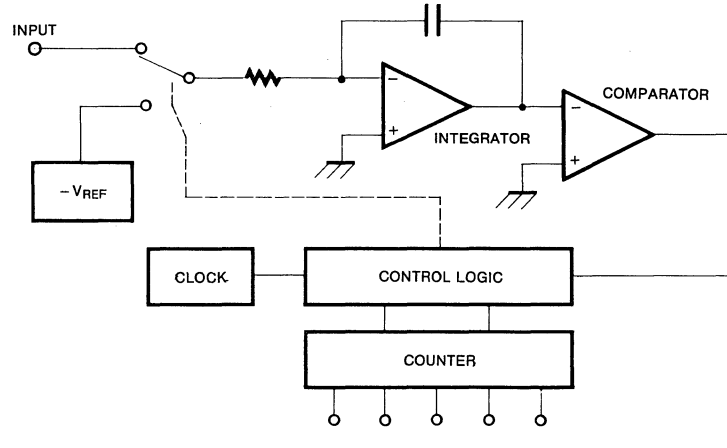


Fig. 6 Functional Block Diagram of Dual-Slope A/D Converter.

Conversion begins when the unknown input voltage is switched to the integrator input; at the same time the counter begins to count clock pulses and counts up to overflow. At this point the control circuit switches the integrator to the negative reference voltage which is integrated until the output is back to zero. Clock pulses are counted during this time until the comparator detects the zero crossing and turns them off. Figure 7 shows the integrator output waveform for dual-slope A/D converter.

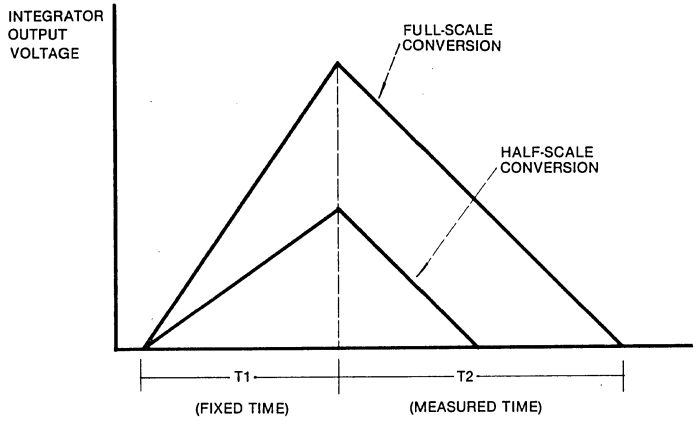


Fig. 7 Integrator Output Waveform for Dual-Slop A/D Converter

The counter output is then the converted digital word. Where T1 is a fixed time and T2 is a time proportional to the input voltage. The times are related as follows:

$$T2 = T1\frac{V^{IN}}{V_{REF}}$$

The digital output word therefore represents the ratio of the input voltage to the reference. Dual-slope convertion has several important features. First, convertion accuracy is independent of the stability of the clock and integrating capacitor so long as they are constant during the conversion period. Accuracy depends only on the reference accuracy and the integrator circuit linearity. Second, the noise rejection of the converter can be infinite if T1 is set to equal the period of the noise. To reject 60Hz power noise therefore requires that T1 be 16.667 msec.

3. D/A Converter

The digital-to analog conversion circuits, which are also called D/A converters, or DACs, can be considered as decoding devices that accept digitally coded signals and provide analog outputs in the form of circuits or voltages. In this manner, they provide an interface between the digital signals of the computer systems and continuous signals of the analog world. They are employed in a variety of applications from CRT display systems and voice synthesizers to automatic test systems, digital controlled attenuators, and process control actuators. In addition, they are key components inside most A/D converters.

Figure 8 shows the functional block diagram of a basic D/A converter system. The input to the D/A converter is a digital word, made up a stream of binary bits comprised of 1's and 0's. The output analog quantity A, which can be a voltage or current, is related to the input as

$$A = KV_{REF}\left(\frac{b1}{2^1} + \frac{b2}{2^2} + \ldots + \frac{bn}{2^n}\right)$$

where K is a scale factor, V_{REF} is a reference voltage, n is the total number of bits, and b1, b2, ... bn are the bit coefficient, which are quantized to be a 1 or a 0.

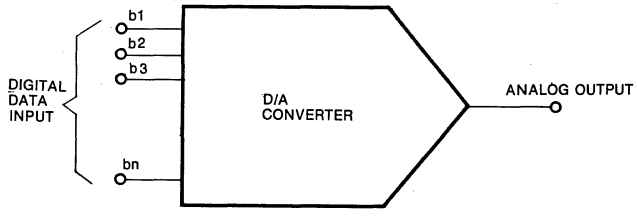


Fig. 8 Functional Block Diagram of a Basic D/A Converter

As a function of the input binary word which determines the bit coefficients, the output exhibits 2^n discrete voltage levels ranging from zero to a maximum value of

$$(Vo)max = V_{REF}\frac{2^n - 1}{2^n}$$

with a minimum step change $\triangle Vo$ given as

$$\triangle Vo = \frac{V_{REF}}{2^n}$$

The transfer function of an ideal 3-bit D/A converter is shown in figure 9.

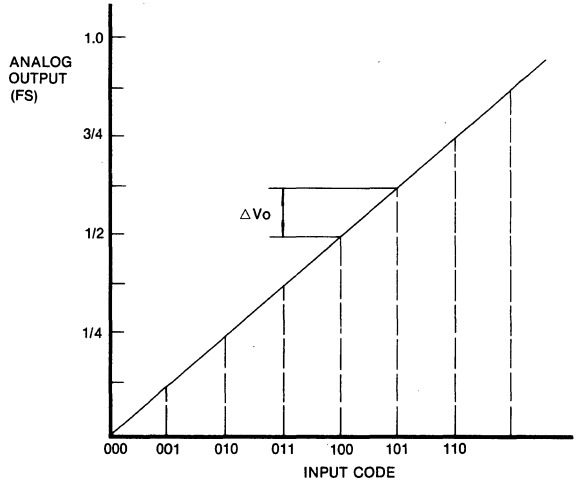


Fig. 9 Transfer Function of Ideal 3-bit D/A Converter

1) Current Scaling D/A Converter

A. Weighted Current Source D/A Converter

The most popular D/A converter design in use today is the weighted current sources circuit illustrated in figure 10. An array of switched transistor current sources is used with binary weighted currents.

$$I_1 = 2\ I_2 = 4\ I_3 = \ldots\ldots = (2_n - 1)\ In$$

The binary weighting is achieved by using emitter resistors with binary related values of R, 2R, 4R, ... $2^{n-1}R$. The resulting collector currents are then added together at the current summing line.

The current sources are switched on or off from standard TTL input by means of the control diodes connected to each emitter. When the TTL input is high the current source is on; when the input is low it is off, with the current flowing through the control diode. Fast switching speed is achieved because there is direct control of the transistor current, and the current source never go into saturation.

To interface with standard TTL levels, the current sources are biased to a base voltage of +1.2V. The emitter currents are regulated to constant values by means of the control amplifier and a precision voltage reference circuit together with a bipolar transistor.

The summed output currents from all current source that are on go to an operational amplifier summing junction; the amplifier converts this output current into an output voltage. In some D/A converters the output current is used to directly drive a resistor load for maximum speed, but the positive output voltage in this case is limited to about +1 volt.

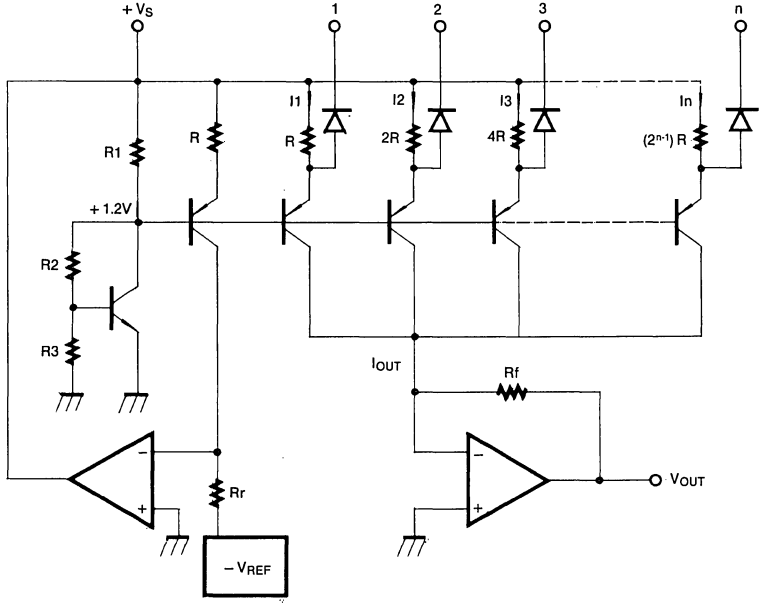


Fig. 10 Weighted Current Source D/A Converter

B. R-2R Ladder D/A Converter

A second popular technique for D/A convertion is the R-2R ladder method. As shown in figure 11, the network consists of series resistor of value R and shunt resistors of value 2R. The bottom of each shunt resistor has a singlepole duble-throw electronic switch which connects the resistor to either ground or the output current summing line.

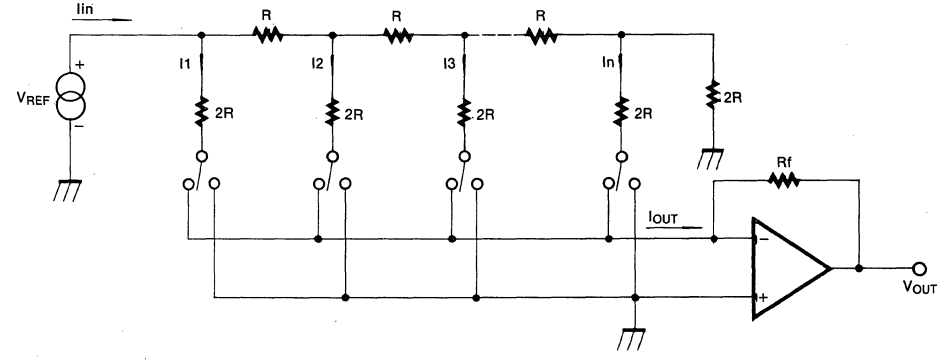


Fig. 11 R-2R Ladder D/A Converter

The operation of the R-2R ladder network is based on the binary division of current as it flows down the ladder. Examination of the ladder configuration reveals that at point a looking to the right, one measures a resistance of 2R; therefore the reference input to the ladder has a resistance of R. At the reference input the current splits into two equal parts since it sees equal resistances in either direction. Likewise, the current flowing down the ladder to the right continues to divide into two equal parts at each resistor junction.

The result is binary weighted currents flowing down each shunt resistor in the ladder. The digitally controlled switches direct the currents to either the summing line or ground. Assuming all bits are on as shown in the diagram, the output current is

$$I_{OUT} = \frac{V_{REF}}{R} \ (1/2 + 1/4 + 1/8 \ ..... \ + 1/2^n)$$

which is a binary series. The sum of all currents is then

$$I_{OUT} = \frac{V_{REF}}{R} \ (1 - 2^{-n})$$

where the 2 term physically represents the portion of the input current flowing through the 2R terminating resistor to ground at the far right.

As in the previous circuit, the output current summing line goes to an operational amplifier which converts current to voltage.

$$V_{OUT} = -Rf \ I_{OUT}$$

The advantage of the R-2R ladder technique is that only two values of resistors are required, with the resultant ease of matching or trimming and excellent temperature tracking. In addition, for high speed applications relatively low resistor values can be used. Excellent results can be obtained for high resolution D/A converters by using laser-trimmed thin film resistor networks.

2) Voltage-Scaling D/A Converter

Voltage-scaling D/A converters produce an analog output voltage by selectively "tapping" a voltage-divider resistor string connected between the reference voltage and ground. For n-bit converter circuit, the resistor string is made up of 2 identical segments connected in series, and it is used as a potentiometer where the voltage levels between the resistor segments are sampled by means of binary switches. For this reason, these types of converters are also called potentiometric D/A converters. Figure 12 shows the conceptual diagram of a 3-bit D/A converter operating on the voltage-scaling principle. The resistor string is comprised of eight identical resistor, connected between V_{REF} and ground. The voltage drop across each resistor section is equal to 1 LSB of output voltage change, or $V_{REF}/2^n$. The output is sampled by means of a decoding switch matrix, and is sensed by a high-impedance buffer amplifier or voltage follower.

With reference to figure 12, the operation of the switch matrix which decodes the input logic signal into an analog voltage can be described as follows. The analog switches marked A, B, and C are driven by the input logic lines corresponding to the input bits b1, b2 and b3, where b1 corresponds to the MSB and b3 corresponds to the LSB. The switches designated A, B and C are driven by the complements of the input logic levels.

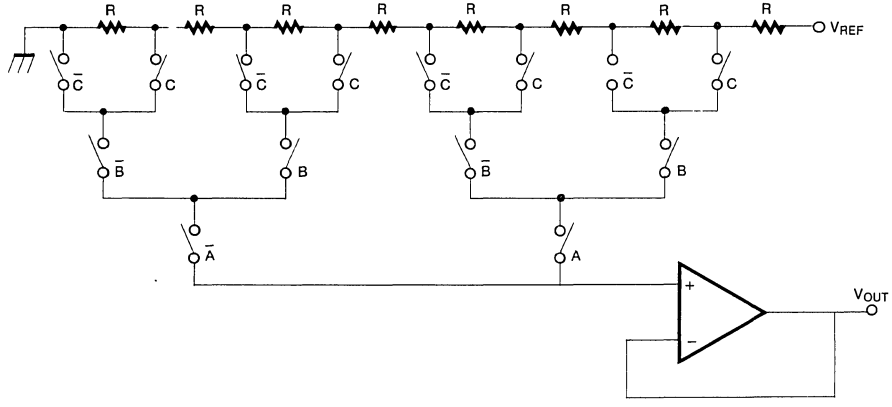


Fig. 12 3-Bit D/A Converter Example Using Voltage-Scaling Principle

The voltage-scaling D/A converter finds its widest application as a building block in MOS A/D conversion systems, where it is used as the D/A converter subsection of a successive-approximation-type A/D converter.

NOTES

A/D CONVERTER 3

1. KSV3100A
2. KSV3110
3. KSV3208
4. KAD0206
5. KAD0808/09
6. KAD0816/17
7. KAD0820
8. KS7126

HIGH-SPEED A/D-D/A CONVERTER

Samsung KSV3100A, VLSI circuit in CI (Collector Implanted) technology, consists of a high-speed flash-type 8-bit A/D converter and a high-speed low-glitch 10-bit D/A converter designed as an R-2R network with switched current sources. Also, the various auxiliary circuits, as reference voltage sources, pre-amplifier, input clamping circuit and feed-in output amplifier are integrated on the single chip.

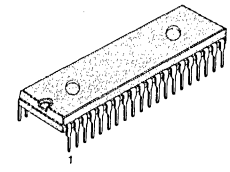
KSV3100A has been developed for use in all applications which call for a high-speed A/D-D/A converter.

For instance, this VLSI circuit can be used to advantage to decode television signals in Pay-TV converters or for MAC converters used in direct satellite broadcast.

Other promising applications can be seen in industrial electronics, e.g. in conjunction with signal processing.

Although KSV3100A was initially designed as high-speed codecs for the video range, it can be used with equal benefits for lower frequencies, even down to zero.

40 DIP



BLOCK DIAGRAM

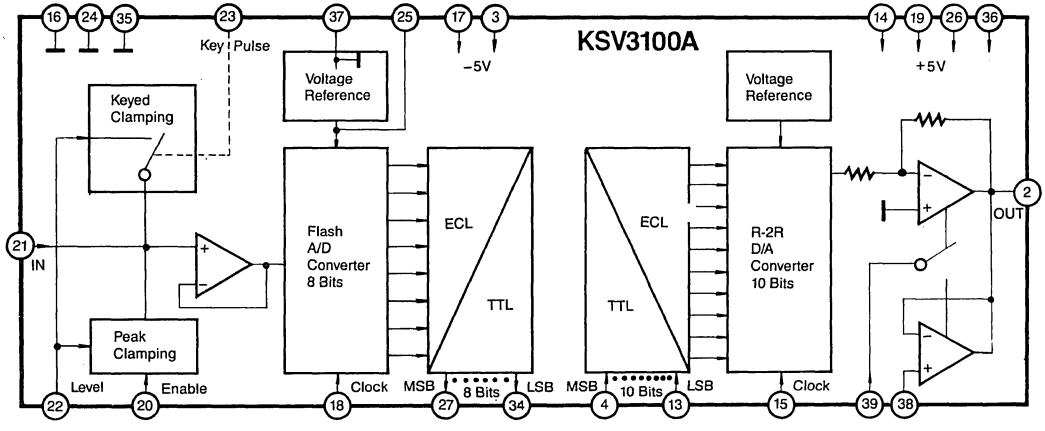


Fig. 1

The auxiliary circuits contained on-chip provide versatile potential applications needing a minimum of external components. For example, an impedance converter is connected upstream of the A/D converter to provide a high-impedance signal input, in spite of the high input capacitance of the A/D converter. The reference voltage for the A/D converter is generated on-chip, but both the ground of the circuit and the reference voltage are fed to pins, so that an external filter capacitor may be connected.

Further, the input is equipped with switches which optionally provide operation with keyed clamping or peak clamping or without clamping. Also the D/A converter's reference voltage is generated on-chip, and a gated amplifier is arranged at the output of the D/A converter so that an external analog signal can be fed-in instead of the signal delivered by the D/A converter.

Separate clock inputs are provided for the A/D converter and the D/A converter thus enabling the application of time compression procedures.

All inputs and outputs are TTL compatible.

PIN DESCRIPTION

Pin No.	Description	Pin No.	Description
1	No Connection	21	Analog Input A/D Converter
2	Analog Output D/A Converter	22	Clamping Level Input
3	−5V Supply D/A Converter-Analog	23	Clamping Pulse Input
4	Digital Input Bit 9 (MSB)	24	Analog Ground A/D Converter
5	Digital Input Bit 8	25	Reference Voltage A/D Converter
6	Digital Input Bit 7	26	+5V Supply A/D Converter-Digital
7	Digital Input Bit 6	27	Digital Output Bit 7 (MSB)
8	Digital Input Bit 5	28	Digital Output Bit 6
9	Digital Input Bit 4	29	Digital Output Bit 5
10	Digital Input Bit 3	30	Digital Output Bit 4
11	Digital Input Bit 2	31	Digital Output Bit 3
12	Digital Input Bit 1	32	Digital Output Bit 2
13	Digital Input Bit 0 (LSB)	33	Digital Output Bit 1
14	+5V Supply D/A Converter-Analog-Digital	34	Digital Output Bit 0 (LSB)
15	Clock Input D/A Converter	35	Digital Ground A/D Converter
16	GND D/A Conv. & Clock A/D Converter	36	+5V Supply A/D Converter-Analog
17	−5V Supply A/D Converter-Analog	37	GND of Ref. Voltage A/D Converter
18	Clock Input A/D Converter	38	External Analog Input
19	+5V Supply A/D Converter	39	Output Signal Switchover Input
20	Peak Clamping Enable Input	40	No Connection

TEST CIRCUIT

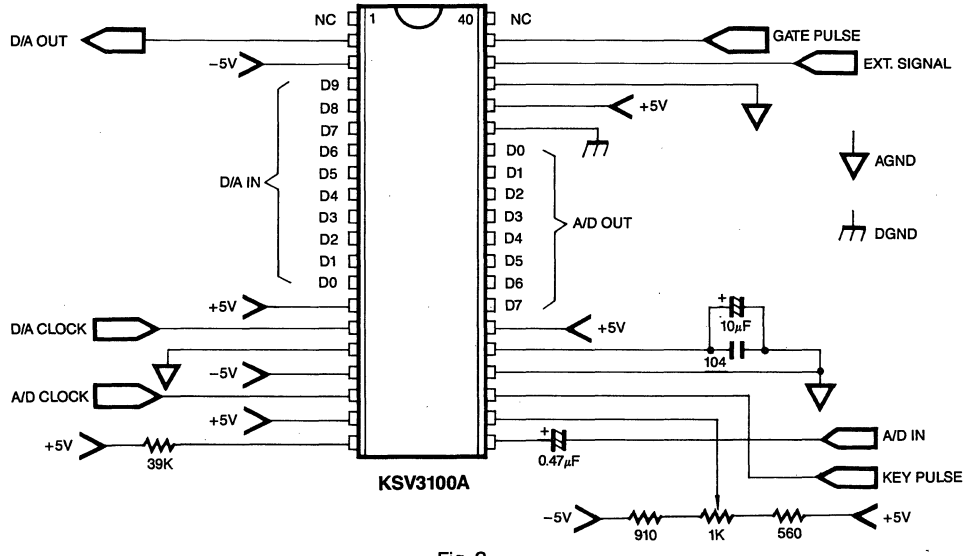


Fig. 2

ABSOLUTE MAXIMUM RATINGS

Characteristics	Symbol	Value	Unit
Positive Supply Voltage	V_{CC}	6	V
Negative Supply Voltage	V_{EE}	−6	V
Input Voltages (Digital)	V_I	−0.5 ~ V_{CC} +0.5	V
Input Voltages (Analog)	V_I	−0.5 ~ V_{CC} +0.5	V
Output Current Pin 2	I_o	±10	mA
Ambient Operating Temperature Range	T_a	0 ~ +70	°C
Storage Temperature Range	T_{stg}	−40 ~ +125	°C

RECOMMENDED OPERATING CONDITIONS

Characteristics	Symbol	Min	Typ	Max	Unit
Positive Supply Voltage	V_{CC}	4.75	5	5.25	V
Negative Supply Voltage	V_{EE}	−4.75	−5	−5.25	V
A/D Converter					
Analog Input Voltage	V_I	0	—	2	V
Input Frequency, Analog Input	f_I	—	—	$f_{cl}/2$	—
Clock Amplitude	V_{18H}	2.0	—	V_{CC}	V
	V_{18L}	0	—	0.8	V
Conversion Rate	f_{18}	0	—	20	MSPS*
Clock High Time (See Fig. 3)	t_H	15	—	—	ns
Clock Low Time (See Fig. 3)	t_L	35	—	—	ns
A/D Output Voltage	V_{OH}	2.4	—	V_{CC}	V
	V_{OL}	0	—	0.4	V
Clamping Level	V_{22}	−1	—	+2	V
Clamping Pulse	V_{23H}	2.0	—	V_{CC}	V
	V_{23L}	0	—	0.8	V
Activation of Peak Clamping	—	Resistor of 20 to 60KΩ from Pin 20 to +5V			—
D/A Converter					
Clock Amplitude	V_{15H}	2.0	—	V_{CC}	V
	V_{15L}	0	—	0.8	V
Conversion Rate	f_{15}	0	—	20	MSPS*
Digital Input Voltage	V_{IH}	2.0	—	V_{CC}	V
	V_{IL}	0	—	0.8	V
Analog Input Voltage at Pin 38	V_{38}	−1	—	+3	V
Output Signal Switch Over Input					
for the D/A Converter Out	V_{39}	0	—	0.8	V
for the Ext. Signal (from Pin 38) Out	V_{39}	2	—	V_{CC}	V

* MSPS (Mega Sample Per Second)

ELECTRICAL CHARACTERISTICS ($V_{CC}=5V$, $V_{EE}=-5V$, $f_{15}=20MHz$, $f_{18}=20MHz$, $Ta=25°C$)

Characteristic	Symbol	Min	Typ	Max	Unit
Current Consumption	I_{CC} I_{EE}	— —	90 −80	120 −110	mA mA
Power Dissipation	P_{TOT}	—	—	1.2	W
Total Transfer Time A/D-D/A	t_{TOT}	See Fig. 3			—
A/D Converter					
Input Current Pin 21	I_I	—	2	—	μA
Input Capacitance Pin 21	C_I	—	10	—	pF
Input Impedance Pin 21					
at f = 1KHz	Z_I	—	20	—	MΩ
at f = 10MHz	Z_I	—	100	—	KΩ
3dB Bandwidth of the Input Amp.	—	—	50	—	MHz
Keyed Clamping Active Level	V_{23}	2.0	—	V_{CC}	V
On Resistance of the Clamping Switch Between Pin 21 and 22	R_{ON}	—	300	—	Ohm
Input Current of the Clamping Level Input Pin 22 ($V_{20}=3V$, $V_{22}=2V$)	I_{22}	—	150	—	μA
Aperture Delay (② in Fig. 3)	t_{AD}	—	—	10	ns
Digital Output Delay (③ in Fig. 3)	t_{DV}	—	25	—	ns
Transfer Time (⑥ in Fig. 3)	t_W	One clock period			—
Differential Non-Linearity	—	See "Ordering Information"			—
Absolute Non-Linearity	—	—	1	—	%
Number of Bits	—	—	8	—	—
Code of the Digital Output Signal	—	Binary			—
Output CODE at the Input with $V_{21}=0V$ with $V_{21}=V_{ref}$	 — —	 00000000 11111111			 — —
Internal Reference Voltage	V_{25}	1.8	2.0	2.2	V
D/A Converter					
Output Impedance Pin 2	Z_O	—	15	—	Ω
Input Current Pin 38 ($V_{38}=2V$)	I_{ID}	—	0.6	—	mA
Internal Reference Voltage	V_{ref}	1.8	2.0	2.2	V
Input Resister Hold Time (⑦ in Fig. 3)	t_{IH}	6.0	—	—	ns
Input Resister Setup Time (⑧ in Fig. 3)	t_{IH}	20	—	—	ns
Differential Non-Linearity	—	See "Ordering Information"			—
Absolute Non-Linearity	—	—	1	—	%
Number of Bits	—	—	10	—	—
Code of the Digital Input Signal	—	Binary			—
Output Signal at the Input with 00000 00000 with 11111 11111	 V_2 V_2	 — —	 0 2	 — —	 V V
Settling Time	t_S	—	50	—	ns

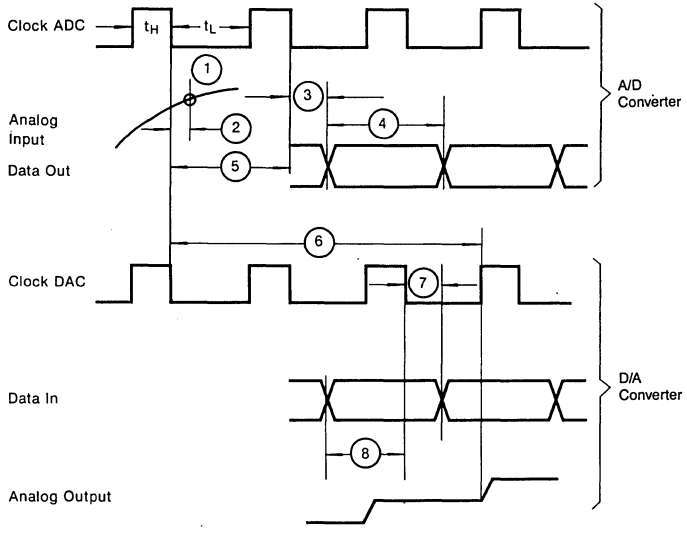
ORDERING INFORMATION

KSV3100A has four kind of version according to the accuracy bit (so called 'Precision') of D/A Converter, and their marking specifications are as follow;

Device	Package	Temperature Range	D/A Converter		A/D Converter
			Accurary Bit	Diff. Nonlinearity	Diff. Nonlinearity
KSV3100ACN-10	40 DIP	0 ~ +70°C	10 bit	± 1/2 LSB	± 1/2 LSB
KSV3100ACN-9			9 bit	± 1 LSB	
KSV3100ACN-8			8 bit	± 2 LSB	
KSV3100ACN-7			7 but	± 4 LSB	

* The accuracy of A/D Converter can be guaranteed as '8 bit' (differential nonlinearity = ± 1/2 LSB) regardless of the D/A Converter's accuracy.

TIMING DIAGRAM



① Sample
② Aperture Delay
③ Digital Output Delay
④ Data Valid (after Sample ①)
⑤ Transfer Time A/D
⑥ Total Transfer Time A/D-D/A with Common Clock
⑦ Input Register Hold Time
⑧ Input Register Setup Time

Fig. 3

INNER CONFIGURATION OF THE CONNECTION PINS

The following figures schematically show the circuitry at the various pins.

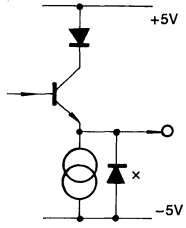


Fig. 4: Pin 2, Output

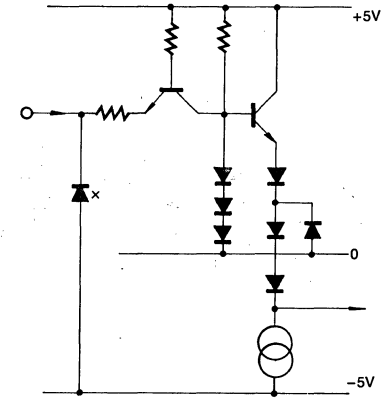


Fig. 5: Pins 4 to 13, 15, 18, 23 and 39, Inputs

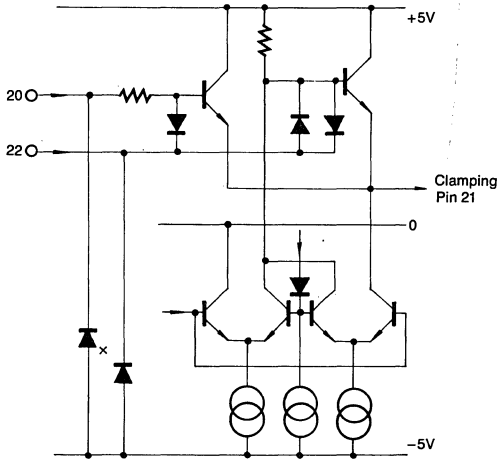


Fig. 6: Pins 20 and 22, Inputs

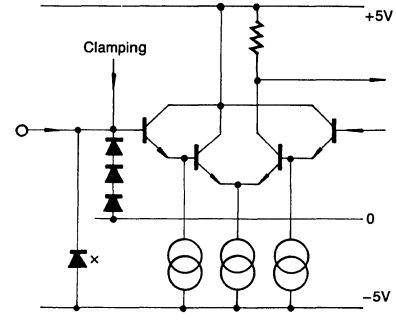


Fig. 7: Pin 21, Input

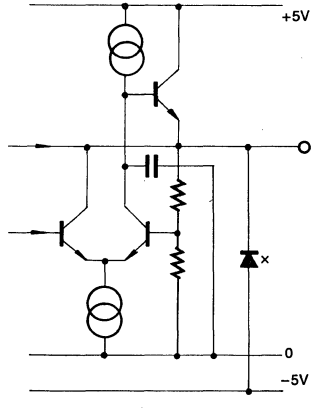


Fig. 8: Pin 25, Reference Voltage Pin

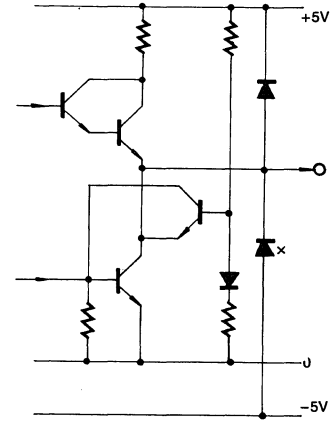


Fig. 9: Pins 27 to 34, Outputs

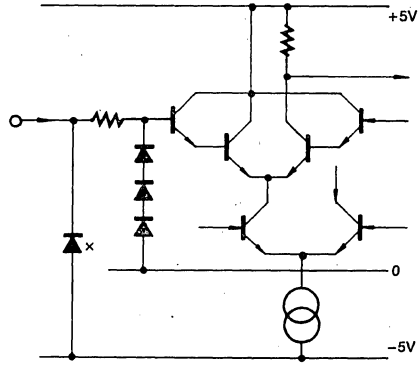


Fig. 10: Pin 38, Input
x = protection diode

DESCRIPTION OF THE CONNECTIONS AND THE SIGNALS

Pin No.	Description
Pin 1	No Connection
Pin 2	Analog Output D/A Converter This pin whose diagram is shown in Fig. 4, is the output for the processed analog signal either originating from the D/A converter or from the external analog input pin 38.
Pin 3	−5 Volt Supply D/A Converter, Analog This pin gets the negative supply for the analog part of the D/A converter.
Pin 4 to 13	Digital Inputs Bit 9 to Bit 0 This diagram of these pins is shown in Fig. 5. They are the inputs of the D/A converter and not-used inputs should be connected to the ground.
Pin 14	+5 Volt Supply D/A Converter, Digital This pin gets the positive supply for the digital part of the D/A converter.
Pin 15	Clock Input D/A Converter This pin whose diagram is shown in Fig. 5 must be supplied with the clock signal for the D/A converter.
Pin 16	Ground D/A Converter and Clock A/D Converter This pin serves as ground pin for the D/A converter and for the clock of the A/D converter.
Pin 17	−5 Volt Supply A/D Converter, Analog This pin is the negative supply pin for the analog part of the A/D converter.
Pin 18	Clock Input A/D Converter The diagram of this pin is shown in Fig. 5. Pin 18 is supplied with the clock of the A/D converter.
Pin 19	+5 Volt Supply A/D Converter Via this pin the A/D converter gets its positive supply.
Pin 20	Peak Clamping Enable Input Via pin 20 whose diagram is shown in Fig. 6, the peak clamping facility can be enabled.

DESCRIPTION OF THE CONNECTIONS AND THE SIGNALS (Continued)

Pin No.	Description
Pin 21	Analog Input A/D Converter Fig. 7 is the diagram of this input. To pin 21 is applied the analog signal to be converted into digital.
Pin 22	Clamping Level Input Via this pin whose diagram is shown in Fig. 6, the input of the A/D converter is supplied with the desired clamping level.
Pin 23	Clamping Pulse Input Fig. 5 is the diagram of this input. Pin 23 must be supplied with the key pulse if keyed clamping is required.
Pin 24	Analog Ground A/D Converter This pin serves as ground pin for the analog part of the A/D converter.
Pin 25	Reference Voltage A/D Converter This pin whose diagram is shown in Fig. 8, is intended for connecting a decoupling capacitor to the A/D converter's reference voltage, the other end of this capacitor to pin 37.
Pin 26	+5 Volt Supply A/D Converter, Digital This pin is the positive supply pin for the digital part of the A/D converter.
Pin 27 to 34	Digital Outputs Bit 7 to Bit 0 Fig. 9 shows the diagram of these outputs which supply the digitized analog signal in parallel 8-bit code.
Pin 35	Digital Ground A/D Converter This pin is the ground connection for the digital part of the A/D converter.
Pin 36	+5 Volt Supply A/D Converter, Analog This pin is the positive supply pin for the analog part of the A/D converter.
Pin 37	Ground of Reference Voltage A/D Converter To this pin must be connected the ground end of the decoupling which is at pin 25.
Pin 38	External Analog Input The diagram of this input is shown in Fig. 10. Pin 38 serves for feeding an external analog signal into the output amplifier of the KSV3100A instead of the D/A-converted signal originating from pin 4 to 13.
Pin 39	Output Signal Switchover Input This pin whose diagram is shown in Fig. 5, is intended for enabling the external analog signal fed to pin 38.
Pin 40	No Connection

APPENDIX: APPLICATION CIRCUITS

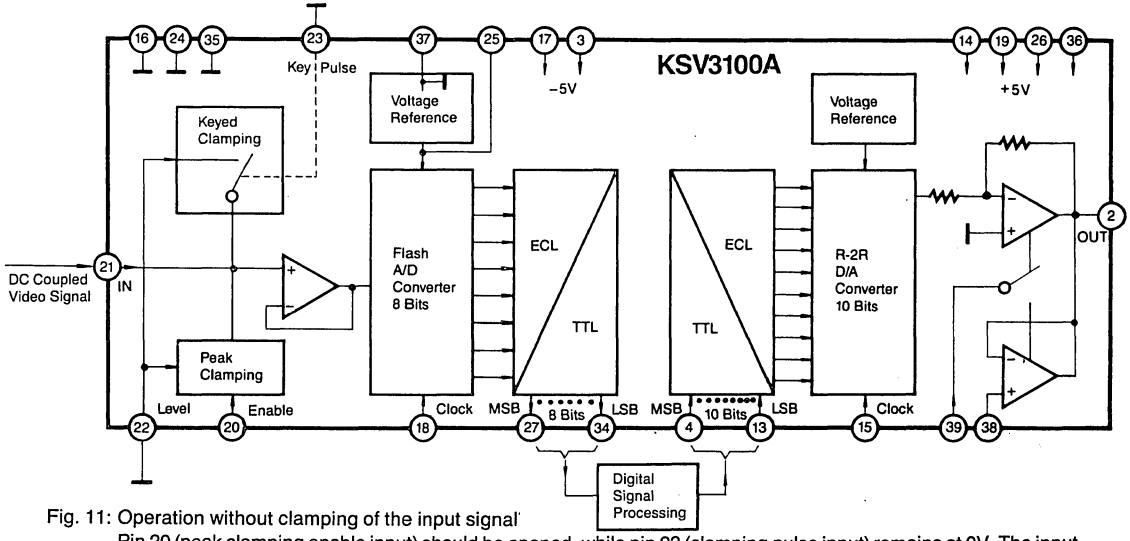


Fig. 11: Operation without clamping of the input signal

Pin 20 (peak clamping enable input) should be opened, while pin 23 (clamping pulse input) remains at 0V. The input signal is applied to the analog input, pin 21, without coupling capacitor such that it lies between 0 and +2V.

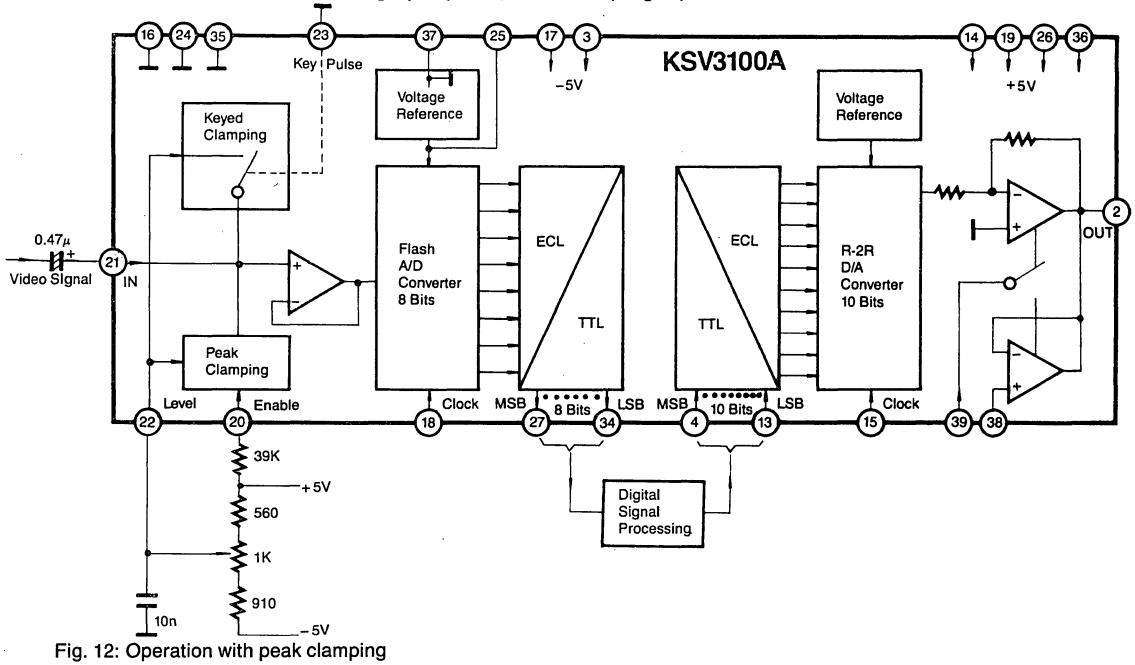


Fig. 12: Operation with peak clamping

The input signal is clamped automatically to the negative peak value. Pin 20 is connected to +5V via a 39KΩ resistor, and pin 22 (clamping level input) is connected, as desired, to zero or a voltage between −1 and +2V. The input signal is fed to pin 21 by way of a coupling capacitor, and no key pulse (clamping pulse) is needed.

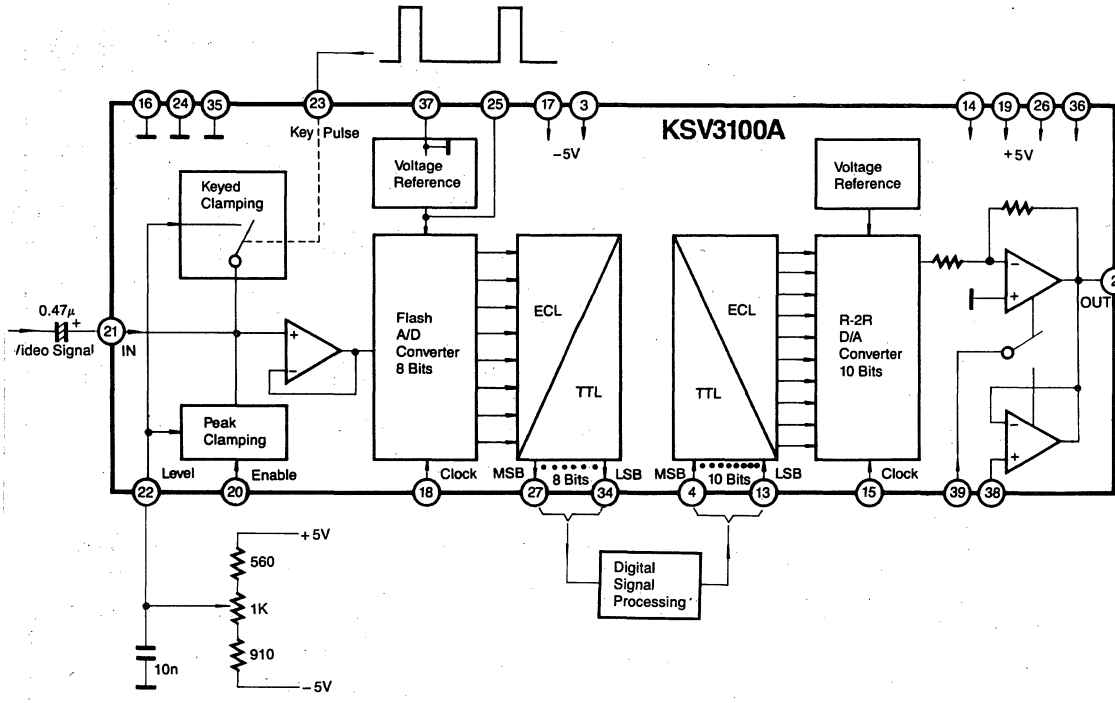


Fig. 13: Operation with keyed clamping

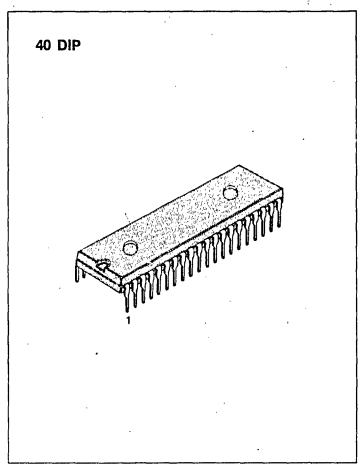
The input signal is applied to pin 21 through a coupling capacitor. Pin 20 must not be connected. While the input signal is at the desired clamping level, an high-level is applied at the clamping pulse input, pin 23. By this means the clamping switch in the KSV3100A connects the input with the clamping level at pin 22 and recharges the coupling capacitor accordingly. The clamping level can be set to zero or, by means of an external voltage devider, to any desired value between −1 and +2V.

HIGH-SPEED A/D-D/A CONVERTER (20MHz 8 bits A/D + 10 bits D/A)

KSV3110 consist of high speed low glitch 10 bit DAC and high speed flash 8 bit ADC with the various auxiliary circuits (reference voltage source, pre buffer amp, input clamp circuit and feed-in output amp).

KSV3110 is suitable for video application, capable of converting an analog signal with full power frequency components upto 6MHz into 8 bit digital signal.

All digital input and output are TTL compatible.



FEATURES

- **8 bit A/D + 10 bit D/A resolution**
- **TTL digital interface**
- **Internal input buffer amp**
- **Internal clamp circuit (Peak, Keyed)**
- **20MSPS conversion rate**
- **Internal reference voltage (2V)**
- **Internal feed-in Amp**
- **Few external components for application**
- **Easy and simple video application**

APPLICATION

- Medical image processing
- Data acquisition system
- Radar data conversion
- Video data conversion

BLOCK DIAGRAM

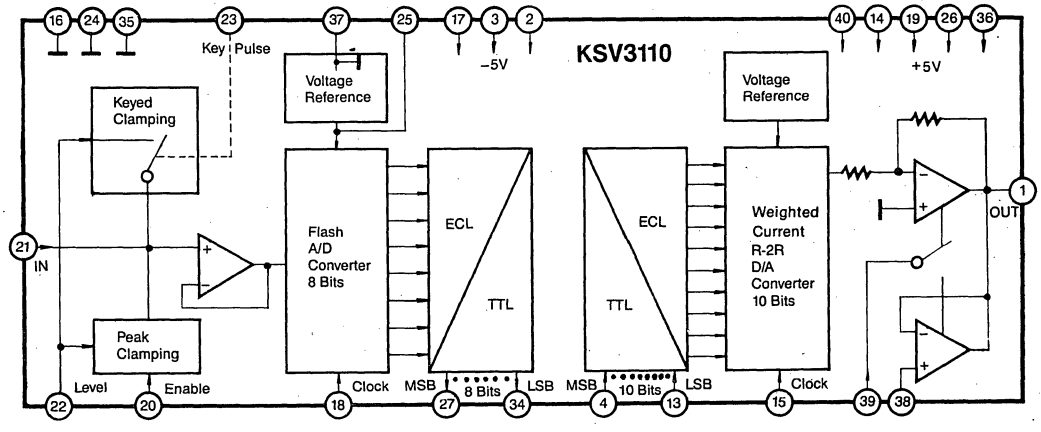


Fig. 1

PIN DESCRIPTION

Pin No.	Description	Pin No.	Description
1	Analog Output D/A Converter	21	Analog Input A/D Converter
2	−5V Supply D/A-Analog	22	Clamping Level Input
3	−5V Supply D/A Converter-Digital	23	Clamping Pulse Input
4	Digital Input Bit 9 (MSB)	24	Analog Ground A/D Converter
5	Digital Input Bit 8	25	Reference Voltage A/D Converter
6	Digital Input Bit 7	26	+5V Supply A/D Converter-Digital
7	Digital Input Bit 6	27	Digital Output Bit 7 (MSB)
8	Digital Input Bit 5	28	Digital Output Bit 6
9	Digital Input Bit 4	29	Digital Output Bit 5
10	Digital Input Bit 3	30	Digital Output Bit 4
11	Digital Input Bit 2	31	Digital Output Bit 3
12	Digital Input Bit 1	32	Digital Output Bit 2
13	Digital Input Bit 0 (LSB)	33	Digital Output Bit 1
14	+5V Supply D/A Converter-Analog-Digital	34	Digital Output Bit 0 (LSB)
15	Clock Input D/A Converter-Analog	35	Digital Ground A/D Converter
16	GND D/A Conv. & Clock A/D Converter	36	+5V Supply A/D Converter-Analog
17	−5V Supply A/D Converter-Analog	37	GND of Ref. Voltage A/D Converter
18	Clock Input A/D Converter-Analog	38	External Analog Input
19	+5V Supply A/D Converter	39	Output Signal Switchover Input
20	Peak Clamping Enable Input	40	+5V Supply D/A-Analog

EVALUATION CIRCUIT

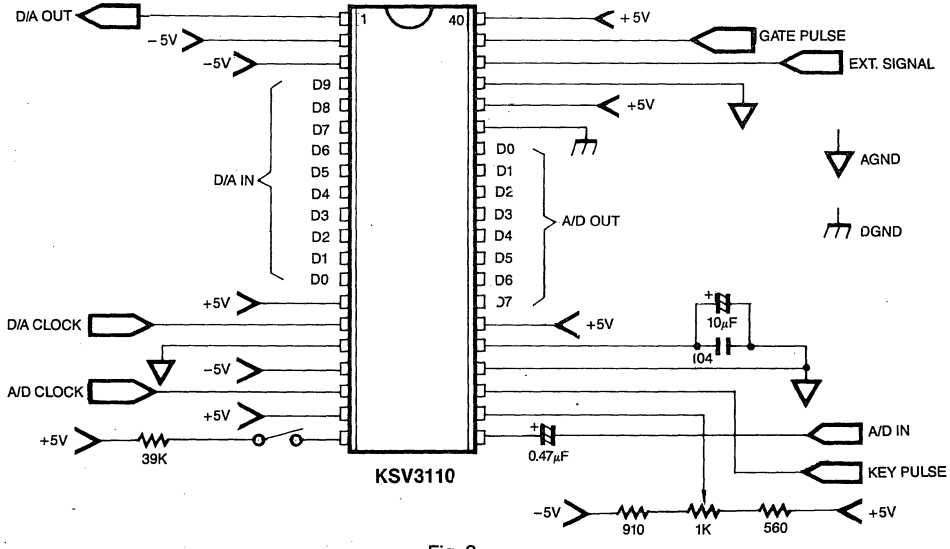


Fig. 2

ABSOLUTE MAXIMUM RATINGS

Characteristics	Symbol	Value	Unit
Positive Supply Voltage	V_{CC}	−0.5 to +6	V
Negative Supply Voltage	V_{EE}	+0.5 to −6	V
Input Voltages (digital)	V_{DI}	−0.5 to +5.5	V
Input Voltages (analog)	V_{AI}	−0.5 to +5.5	V
Digital Output Applied Voltage	V_{DO}	−0.5 to +5.5	V
Digital Output Forced Current	I_{DO}	−2.0 to +6.0	mA
Digital Output Short Time	t_{SHORT}	1	sec
Analog Output Applied Voltage	V_{AO}	−0.5 to +5.5	V
Analog Output Forced Current	I_{AO}	−10 to +0.5	mA
Ambient Operating Temperature	T_A	−25 to +85	degree
Storage Temperature Range	T_{stg}	−40 to +125	degree

NOTE: 1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions.
2. Functional operation under any of these conditions is NOT implied.
3. Applied voltage must be current limited to specified range.
4. Current is specified as positive when flowing into the device.

OPERATING CONDITIONS

Characteristics	Symbol	Min	Typ	Max	Unit
Positive Supply Voltage	V_{CC}	4.75	5.0	5.25	V
Negative Supply Voltage	V_{EE}	−4.75	−5.0	−5.25	V
A/D Converter					
Clock High Time (1)	t_{CKH1}	15			ns
Clock Low Time (1)	t_{CKL1}	25			ns
Clamping Pulse High Time	t_{CLPH}	1			μs
Clamping Pulse Low Time	t_{CLPL}	1			μs
Digital Input High Voltage (1)	V_{DIH1}	2.0			V
Digital Input Low Voltage (1)	V_{DIL1}			0.8	V
Digital Output High Current	I_{DOH}			−400	μA
Digital Output Low Current	I_{DOL}			2.4	mA
Peak Clamping Resistance	R_{20}	20	39	60	Kohm
Analog Input Voltage	V_{AI}	0		V_{ref}	V
Clamping Level	V_{22}	−1		2	V
D/A Converter					
Clock High Time (2)	t_{CKH2}	20			ns
Clock Low Time (2)	t_{CKL2}	20			ns

(Continue)

OPERATING CONDITIONS (Continued)

Characteristics	Symbol	Min	Typ	Max	Unit
Switch Over Pulse High Time	t_{39H}	1			μs
Switch Over Pulse Low Time	t_{39L}	1			μs
Digital Input High Voltage (2)	V_{DIH2}	2.0			V
Digital Input Low Voltage (2)	V_{DIL2}			0.8	V
Digital Input Set-up Time	t_{SET}	15			ns
Digital Input Hold Time	t_{HOLD}	12			ns
External Analog Input Voltage	V_{38}	−1		3	V
Ambient Temperature	T_A	0		70	degree

ELECTRICAL CHARACTERISTICS (within specified operation condition)

Characteristics	Symbol	Condition	Min	Typ	Max	Unit
Positive Supply Current	I_{CC}	V_{CC} = Max		105	140	mA
Negative Supply Current	I_{EE}	V_{EE} = Max		−95	−130	mA
A/D Converter						
Analog Input Bias Current	I_{AIN}	V_{AI} = 2.0V, V_{EE} = Max			5	μA
Analog Input Capacitance	C_{AIN}			5		pF
Analog Input Resistance	R_{AIN}	F_{AIN} = 100KHz		100		Kohm
Total String Resistance	R_{STRING}	$R_{(pin\ 25-pin\ 37)}$	350	450	550	ohm
Reference Voltage	V_{REF}	$V_{pin\ 25}$	1.8		2.2	V
Clock High Current	I_{CKH1}	V_{CK} = 2.4V, V_{CC} = Max			50	μA
Clock Low Current	I_{CKL1}	V_{CK} = 0.4V, V_{CC} = Max			−800	μA
Clamping Pulse High Current	I_{CLPH}	V_{CLP} = 2.4V, V_{CC} = Max		8	50	μA
Clamping Pulse Low Current	I_{CLPL}	V_{CLP} = 0.4V, V_{CC} = Max			−500	μA
Digital Output High Voltage	V_{DOH}	I_{DOH} = 0.4mA V_{CC} = Min	2.4			V
Digital Output Low Voltage (1)	V_{DOL1}	I_{DOL} = 1.6mA V_{CC} = Min			0.5	V
Digital Output Low Voltage (2)	V_{DOL2}	I_{DOL} = 2.4mA V_{CC} = Min			0.7	V
Maximum Conversion Rate	F_{AS}	V_{CC}, V_{EE} = Min	20			MSPS
Aperture Delay Time	t_{AP}	V_{CC}, V_{EE} = Min	−10		0	ns
Digital Output Delay	t_D	V_{CC}, V_{EE} = Min		15	20	ns
Clamp Level Sink Current	I_{22}	Peak: off, Keyed: off	0		150	μA
Peak Clamp Level Difference	$\triangle V_{PEAK}$	V_{22} V_{21}	−250	−100	0	mV
Keyed Clamp Level Difference	$\triangle V_{KEY}$	V_{22} V_{21}	−60			mV
Peak Clamp Charge Resistance	R_{PEAK}	$\triangle V_{21}/\triangle I_{22}$, $V_{21} < V_{22}$		150		ohm
Keyed Clamp Charge Resistance	R_{KEY}	$\triangle V_{21}/\triangle I_{22}$, $V_{21} < V_{22}$		150		ohm
Keyed Clamp Discharge Current	I_{KEY}	$V_{21} > V_{22}$		100		μA
Static Diff. Non Linearity	SDNL1	F_{IN} = 1KHz CK = 1MHz		0.2		%

ELECTRICAL CHARACTERISTICS (Continued)

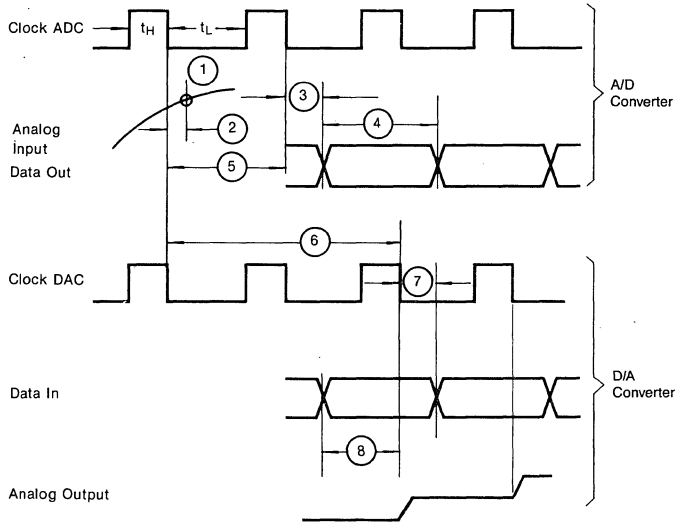
Characteristics	Symbol	Condition	Min	Typ	Max	Unit
Dynamic Diff. Non Linearity	DDNL	A_{IN} = 1.02MHz CK = 10MHz		0.3		%
		A_{IN} = 6.0018MHz				
		CK = 25MHz (37.5% DUTY)			0.6	%
Dynamic Integral Non Linearity	DINL	A_{IN} = 1.02MHz CK = 10MHz		0.8		%
Full Power Input Band Width	BW		6			MHz
Full Code Offset Error	E_{FULL}	(Full Code Input) − V_{REF}	0	+100	+200	mV
Zero Code Offset Error	E_{ZERO}	(Zero Code Input) − V_{REF}	−100	+40	+100	mV
Signal to Noise Ratio	SNR	A_{IN} = 1.02MHz CK = 10MHz		42		dB
(RMS Signal/RMS Noise)		A_{IN} = 1.02MHz CK = 20MHz		35		dB
		A_{IN} = 3.601MHz				
		CK = 25MHz (37.5% DUTY)	30	34		dB
Differential Gain Error	DG	A_{IN} = 3.579545MHz				
		CK = 14.318MHz	−1		3	%
Differential Phase Error	DP	A_{IN} = 3.579545MHz				
		CK = 14.318MHz	−2		2	degree
D/A Converter						
Digital Input High Current	I_{DIH2}	V_{CC} = Max, V_{DIH2} = 2.4V			50	μA
Digital Input Low Current	I_{DIH2}	V_{CC} = Max, V_{DIL2} = 0.4V			−500	μA
External Input Bias Current	I_{38}	V_{CC} = Max, V_{38} = 3V			10	μA
External Input Capacitance	C_{38}			5		pF
External Input Equ. Resistance	R_{38}	F_{38} = 10KHz		1		Mohm
External Amp. Offset Error	E_{OFFSET}	V_{38} = −1V	−100		100	mV
External Amp. Gain Error	E_{GAIN}	{(V1/V38) − 1}*100	−5		5	%
Max. Data Conversion Rate	F_{DC}		20			MSPS
Analog Output Delay	t_D				25	ns
Settling Time	t_{SET}	settle to 0.2%			40	ns
Rising Time	t_R	10% to 90%			50	ns
Falling Time	t_F	90% to 10%			35	ns
Glitch Amplitude	G_A				80	mV
Glitch Duration	G_D				7	ns
Glitch Energy	G_E				250	pV-sec
Static Diff. Non Linearity	SDNL2	KSV3110-10			0.05	%
		KSV3110-9			0.1	%
		KSV3110-8			0.2	%
Static Integral Non Linearity	SINL				1	%
Full Scale Output Voltage	V_{FULL}	V_{CC} = typ, V_{EE} = typ	1.8		2.2	V
Zero Scale Output Voltage	V_{ZERO}	V_{CC} = typ, V_{EE} = typ	−60		+60	mV

MARKING SPECIFICATIONS (Ordering Information)

KSV3110 has three kind of version according to the accuracy bit (so called 'precision') of D/A Converter, and their marking specifications are as follow:

Marking Spec.	D/A Converter		A/D Converter	Package	Temp. Range
	Accuracy Bit	Diff. Nonlinearity	Diff. Nonlinearity		
KSV3110-10	10 BIT	0.05%	0.2%	40 DIP	0 ~ +70°C
KSV3110-9	9 BIT	0.1%			
KSV3110-8	8 BIT	0.2%			

TIMING DIAGRAM



① Sample
② Aperture Delay
③ Digital Output Delay
④ Data Valid (after Sample ①)
⑤ Transfer Time A/D
⑥ Total Transfer Time A/D-D/A with Common Clock
⑦ Input Register Hold Time
⑧ Input Register Setup Time

Fig. 3

PACKAGE LAYOUT

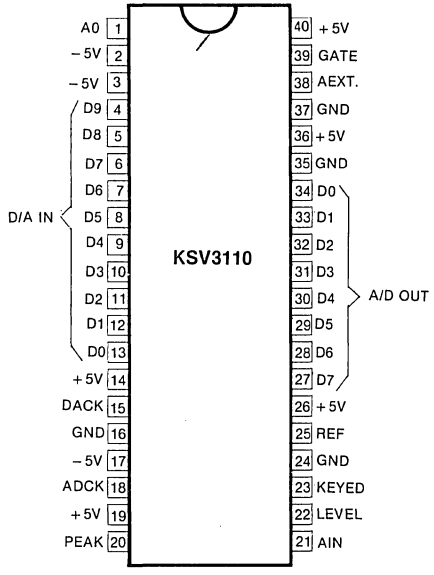


Fig. 4

DESCRIPTION OF THE CONNECTION AND THE SIGNALS

Pin No.	Description
Pin 1	Analog Output D/A Converter This pin whose diagram is shown in Fig. 7, is the output for the processed analog signal either originating from the D/A converter or from the external analog input pin 38.
Pin 2	−5 Volt Supply D/A Converter, Analog This pin gets the negative supply for the analog part of the D/A converter
Pin 3	−5 Volt Supply D/A Converter, Digital This pin gets the negative supply for the digital part of the D/A converter.
Pin 4 to 13	Digital Inputs Bit 9 to Bit 0 This diagram of these pins is shown in Fig. 5. They are the inputs of the D/A converter and not-used inputs should be connected to the ground.
Pin 14	+5 Volt Supply D/A Converter, Digital This pin gets the positive supply for the digital part of the D/A converter.
Pin 15	Clock Input D/A Converter This pin whose diagram is shown in Fig. 5 must be supplied with the clock signal for the D/A converter.
Pin 16	Ground D/A Converter and Clock A/D Converter This pin serves as ground pin for the D/A converter and for the clock of the A/D converter.

DESCRIPTION OF THE CONNECTION AND THE SIGNALS (Continued)

Pin No.	Description
Pin 17	−5 Volt Supply A/D Converter, Analog This pin is the negative supply pin for the analog part of the A/D Converter.
Pin 18	Clock Input A/D Converter The diagram of this pin is shown in Fig. 5 Pin 18 is supplied with the clock of the A/D converter.
Pin 19	+5 Volt Supply A/D Converter Via this pin the A/D converter gets its positive supply.
Pin 20	Peak Clamping Enable Input Via pin 20 whose diagram is shown in Fig. 6, the peak clamping facility can be enabled.
Pin 21	Analog Input A/D Converter Fig. 7 is the diagram of this input. To pin 21 is applied the analog signal to be converted into digital.
Pin 22	Clamping Level Input Via this pin whose diagram is shown in Fig. 6, the input of the A/D converter is supplied with the desired clamping level.
Pin 23	Clamping Pulse Input Pin 23 must be supplied with the key pulse if keyed clamping is required.
Pin 24	Analog Ground A/D Converter This pin serves as ground pin for the analog part of the A/D converter.
Pin 25	Reference Voltage A/D Converter This pin whose diagram is shown in Fig. 8, is intended for connecting a decoupling capacitor to the A/D converter's reference voltage, the other end of this capacitor to pin 37.
Pin 26	+5 Volt Supply A/D Converter, Digital This pin is the positive supply pin for the digital part of the A/D converter.
Pin 27 to 34	Digital Outputs Bit 7 to Bit 0 Fig. 9 shows the diagram of these outputs which supply the digitized analog signal in parallel 8-bit code.
Pin 35	Digital Ground A/D Converter This pin is the ground connection for the digital part of the A/D converter.
Pin 36	+5 Volt Supply A/D Converter, Analog This pin is the positive supply pin for the analog part of the A/D converter.
Pin 37	Ground of Reference Voltage A/D Converter To this pin must be connected the ground end of the decoupling which is at pin 25.
Pin 38	External Analog Input The diagram of this input is shown in Fig. 10. Pin 38 serves for feeding an external analog signal into the output amplifier of the KSV3110 instead of the D/A-converted signal originating from pin 4 to 13.
Pin 39	Output Signal Switchover Input This pin whose diagram is shown in Fig. 5, is intended for enabling the external analog signal fed to pin 38.
Pin 40	+5 Volt Supply Converter, Analog This pin is the negative supply pin for the analog parts of the D/A converter.

INNER CONFIGURATION OF THE CONNECTION PINS

The following figures schematically show the circuitry at the various pins.

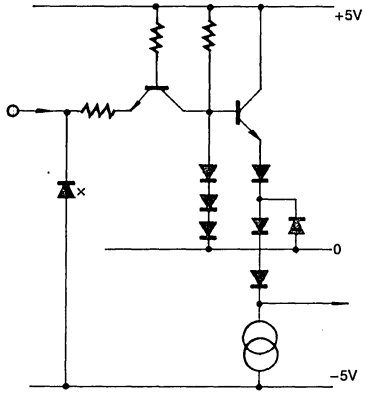


Fig. 5: Pins 4 to 13, 15, 18, 23 and 39, Inputs

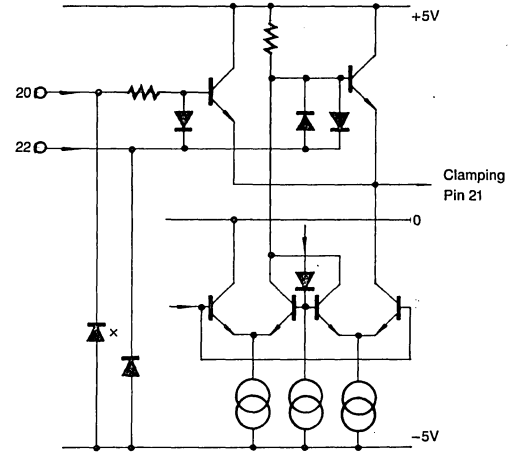


Fig. 6: Pins 20 and 22, Inputs

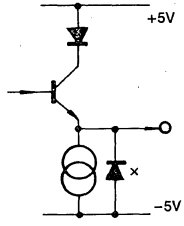


Fig. 7: Pin 1, Output

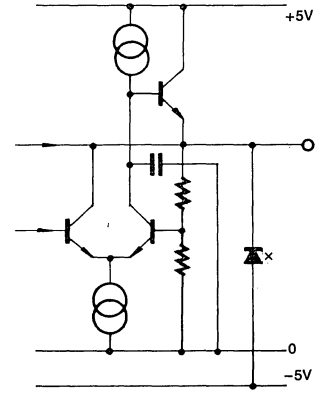


Fig. 8: Pin 25, Reference Voltage Pin

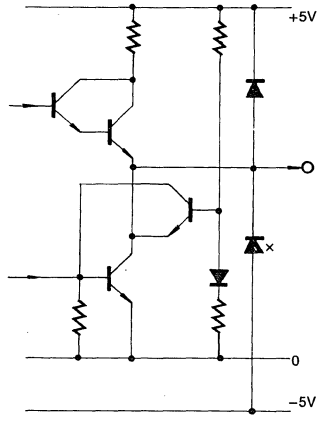


Fig. 9: Pins 27 to 34, Outputs

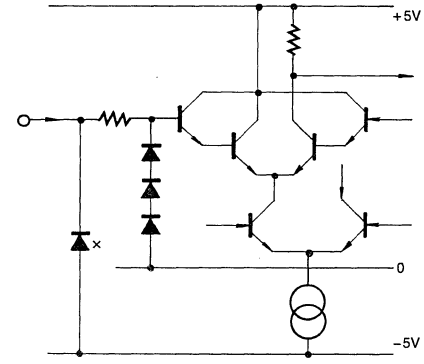


Fig. 10: Pin 38, Input
×=protection diode

RECOMMENDED APPLICATION CIRCUIT

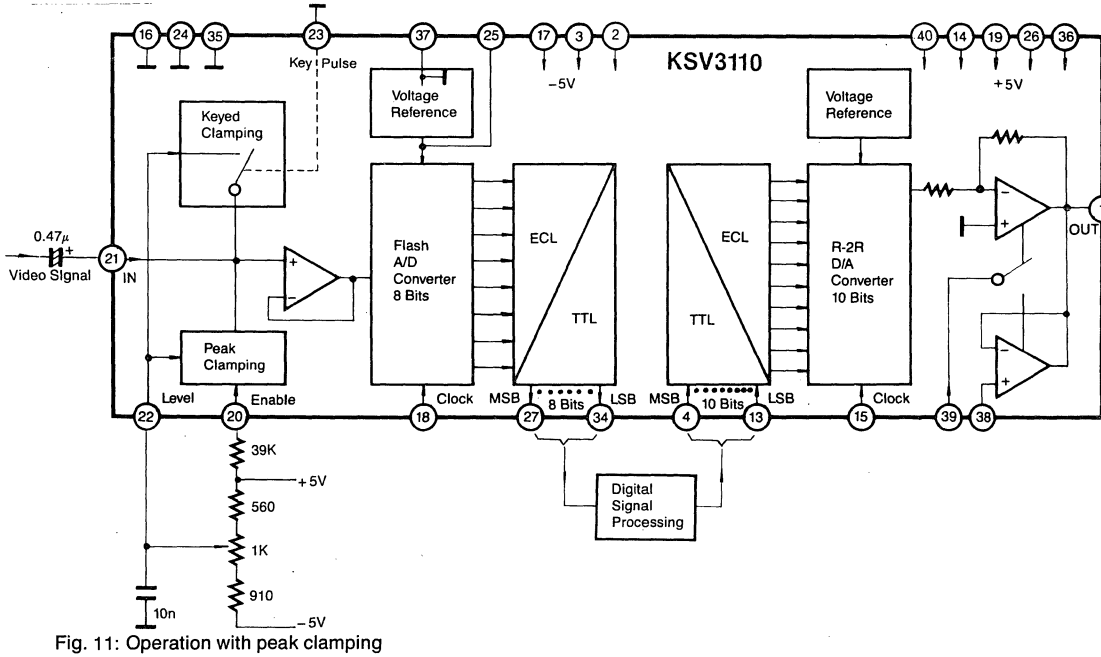


Fig. 11: Operation with peak clamping

The input signal is clamped automatically to the negative peak value. Pin 20 is connected to +5V via a 39KΩ resistor, and pin 22 (clamping level input) is connected, as desired, to zero or a voltage between −1 and +2V. The input signal is fed to pin 21 by way of a coupling capacitor, and no key pulse (clamping pulse) is needed.

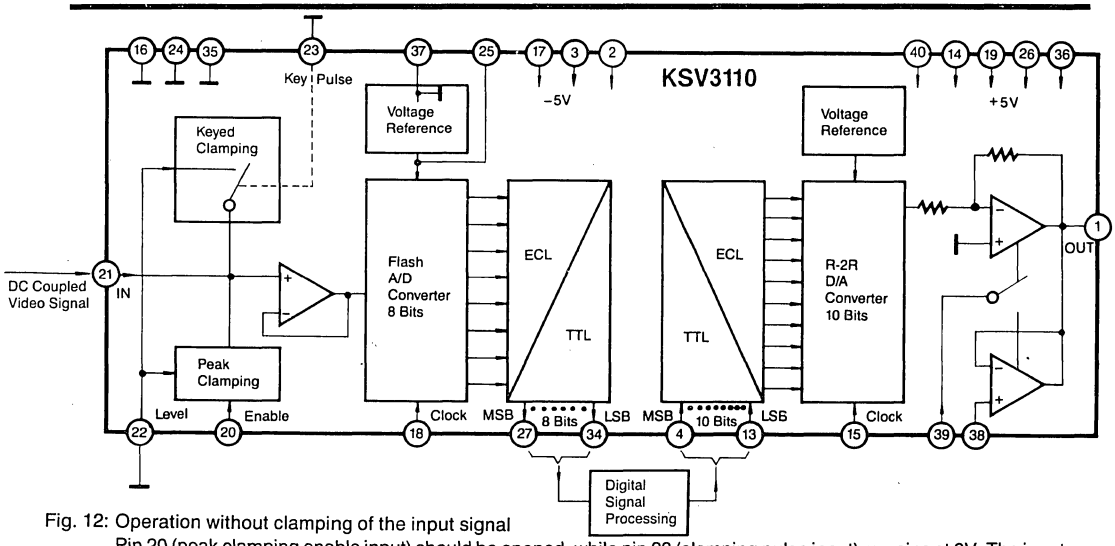


Fig. 12: Operation without clamping of the input signal
Pin 20 (peak clamping enable input) should be opened, while pin 23 (clamping pulse input) remains at 0V. The input signal is applied to the analog input, pin 21, without coupling capacitor such that it lies between 0 and +2V.

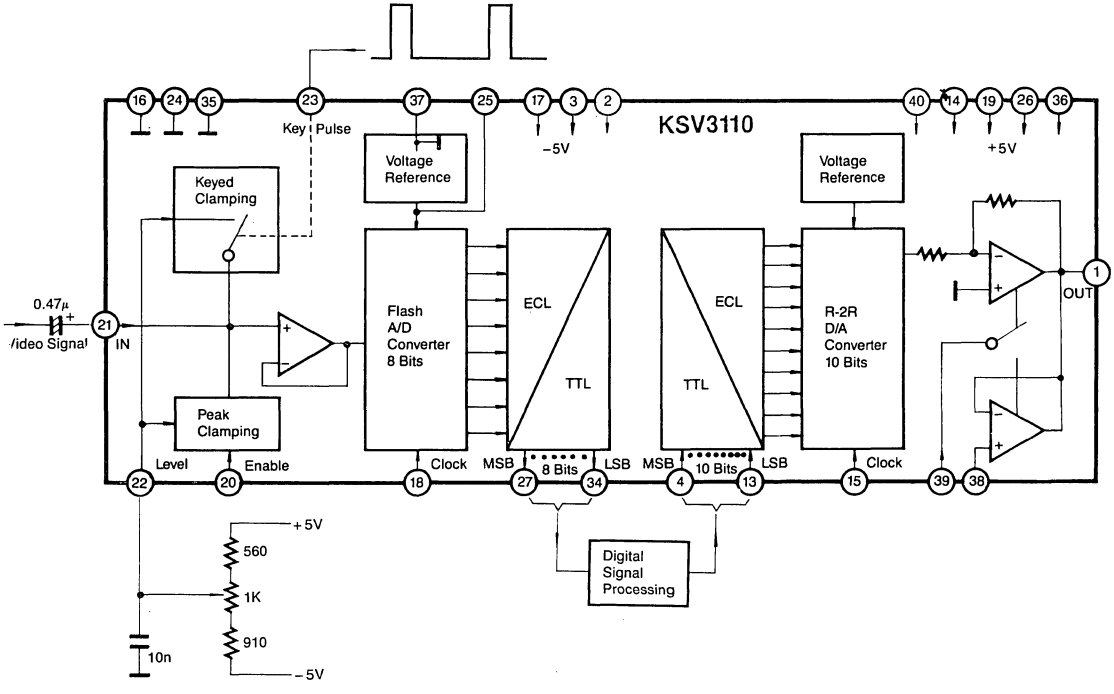


Fig. 13: Operation with keyed clamping
The input signal is applied to pin 21 through a coupling capacitor. Pin 20 must not be connected. While the input signal is at the desired clamping level, an high-level is applied at the clamping pulse input, pin 23. By this means the clamping switch in the KSV3110 connects the input with the clamping level at pin 22 and recharges the coupling capacitor accordingly. The clamping level can be set to zero or, by means of an external voltage devider, to any desired value between −1 and +2V.

HIGH-SPEED A/D CONVERTER

Samsung KSV3208, VLSI circuit in CI (Collector Implanted) technology, consists of a high-speed flash-type 8-bit A/D converter. Also, the various auxiliary circuits, as reference voltage sources, pre-amplifier, input clamping circuits are integrated on the single chip.

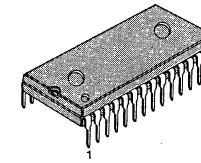
KSV3208 has been developed for use in all applications which call for a high-speed A/D converter.

For instance, this VLSI circuit can be used to advantage to decode television signals in Pay-TV converters or for MAC converters used in direct satellite broadcast.

Other promising applications can be seen in industrial electronics, e.g. in conjunction with signal processing.

Although KSV3208 was initially designed as high-speed converter for video frequency range, it can be used with equal benefits for lower frequencies, even down to zero.

28 DIP



ORDERING INFORMATION

Device	Package	Temperature Range	Diff. Nonlinearity
KSV3208CN	28 DIP	0 ~ +70°C	± 1/2 LSB

BLOCK DIAGRAM

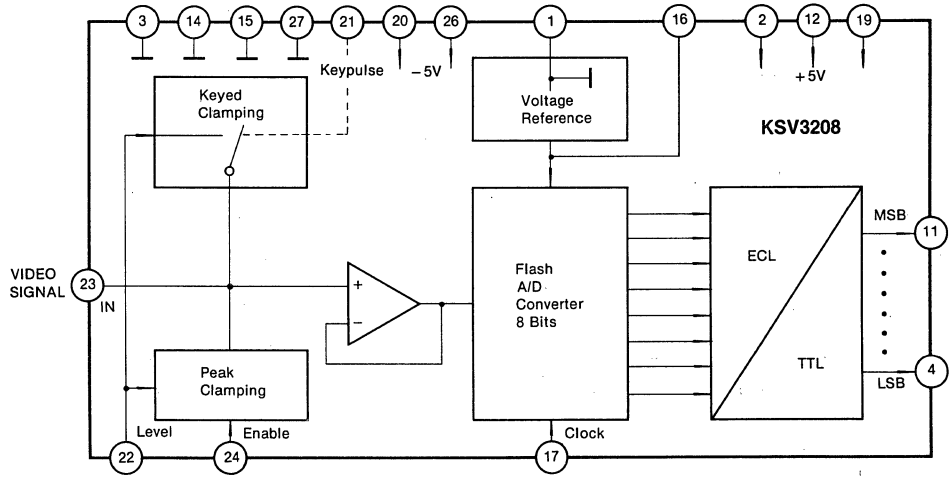


Fig. 1

The auxiliary circuits contained on-chip provide versatile potential applications needing a minimum of external components. For example, an impedance converter is connected upstream of the A/D converter to provide a high-impedance signal input in spite of the high input capacitance of the A/D converter. The reference voltage for the A/D converter is generated on-chip, but both the ground of the circuit and the reference voltage are fed to pins, so that an external filter capacitor may be connected.

Further, the input is equipped with switches which optionally provide operation with keyed clamping of peak clamping or without clamping.

All inputs and outputs are TTL compatible.

PIN DESCRIPTION

Pin No.	Description
1	GND of Reference Resistor String
2	+5V Supply of ECL Logic Part, Digital
3	GND of ECL to TTL Translator Part, Digital
4	Digital Output Bit 0 (LSB)
5	Digital Output Bit 1
6	Digital Output Bit 2
7	Digital Output Bit 3
8	Digital Output Bit 4
9	Digital Output Bit 5
10	Digital Output Bit 6
11	Digital Output Bit 7 (MSB)
12	+5V Supply of TTL Output Part, Digital
13	No Connection
14	GND of ECL Logic Part, Digital
15	GND of Input Stage, Analog
16	$+V_{REF}$, Reference Voltage Point of Resistor String
17	Clock Input
18	No Connection
19	+5V Supply of Input Stage, Analog
20	−5V Input Stage, Analog
21	Clamping Pulse Input
22	Clamping Level Input
23	Analog Signal Input
24	Peak Clamp Enable Input
25	No Connection
26	No Connection
27	GND of ECL Clock Part, Digital
28	−5V Supply of ECL Logic Part, Digital

RECOMMENDED OPERATING CIRCUIT

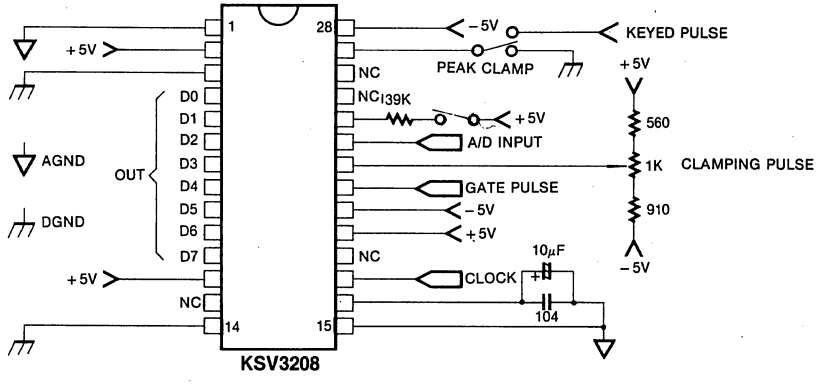


Fig. 2

ABSOLUTE MAXIMUM RATINGS

Characteristics	Symbol	Value	Unit
Positive Supply Voltage	V_{CC}	−0.5 to +6	V
Negative Supply Voltage	V_{EE}	−0.5 to +6	V
Digital Input Voltage	V_{DI}	−0.5 to 5.5	V
Analog Input Voltage	V_{AI}	−0.5 to 5.5	V
Digital Output Applied Voltage	V_{DO}	−0.5 to 5.5	V
Digital Output Forced Current	I_{DO}	−2.0 to 6.0	V
Single Digital Output Short Time Duration	t_{short}	1	sec
Ambient Operating Temperature	T_A	−25 to +85	°C
Storage Temperature	T_{stg}	−40 to +125	°C

Notes: 1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions.
2. Functional operation under any of these conditions is not implied.
3. Applied voltage must be current limited to specified range.
4. Current is specified as positive when flowing into the device.

RECOMMENDED OPERATING CONDITIONS

Characteristics	Symbol	Min	Typ	Max	Unit
Positive Supply Voltage	V_{CC}	4.75	5	5.25	V
Negative Supply Voltage	V_{EE}	−4.75	−5	−5.25	V
Analog Input Voltage	V_{AI}	0	—	V_{ref}	V
Analog Input Frequency	f_I	—	—	$f_{ck/2}$	—
Digital Input High Voltage	V_{DIH1}	2.0	—	—	V
Digital Input Low Voltage	V_{DIL1}	0	—	0.8	V
Conversion Rate	f_{17}	0	—	20	MSPS*
Clock High Time 1 (See Fig. 3)	t_{CKH1}	15	—	—	ns
Clock Low Time 1 (See Fig. 3)	t_{CKL1}	25	—	—	ns
Clamping Level	V_{22}	−1	—	+2	V
Clamping Pulse High Time	t_{CLPH}	1	—	—	μs
Clamping Pulse Low Time	t_{CLPL}	1	—	—	μs
Digital Output High Current	I_{DOH}	—	—	−400	μA
Digital Output Low Current	I_{DOL}	—	—	3	mA
Resistance for Peak Clamping	R_{pin20}	20	39	60	KΩ
Ambient Temperature	T_a	0	—	70	°C

* MSPS (Mega Sample Per Second)

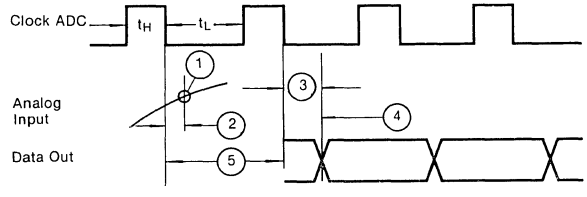
ELECTRICAL CHARACTERISTICS (V_{CC} = +5V, V_{EE} = −5V, f_{17} = 20MHz, Ta = 25°C)

Characteristics	Symbol	Condition	Min	Typ	Max	Unit
Positive Supply Current	I_{CC}	V_{CC} = Max	—	100	120	mA
Negative Supply Current	I_{EE}	V_{EE} = Max	—	−76	−100	mA
Analog Input Bias Current	I_{AIN}	V_{AI} = 2.0V, V_{EE} = Max	—	—	5	μA
Analog Input Capacitance	C_{AIN}		—	5	—	pF

ELECTRICAL CHARACTERISTICS (V_{CC} = +5V, V_{EE} = −5V, f_{17} = 20MHz, Ta = 25°C)

Characteristics	Symbol	Condition	Min	Typ	Max	Unit
Analog Input Equ. Resistance	R_{AIN}	F_{AIN} = 100KHz		100		KΩ
Total String Resistance	R_{string}	$R_{(pin\ 16-pin\ 1)}$	120	200	300	ohm
Reference Voltage	V_{ref}	$V_{pin\ 16}$	1.8	2.0	2.2	V
Clock High Current	I_{CKH1}	V_{CC} = Max, V_{CK} = 2.4V			50	μA
Clock Low Current	I_{CKL1}	V_{CC} = Max, V_{CK} = 0.4V			−800	μA
Clamping Pulse High Current	I_{CLPH}	V_{CC} = Max, V_{CLP} = 2.4V			50	μA
Clamping Pulse Low Current	I_{CLPL}	V_{CC} = Max, V_{CLP} = 0.4V			−500	μA
Digital Output High Voltage	V_{DOH}	V_{CC} = Min, I_{DOH} = 0.4mA	2.4			V
Digital Output Low Voltage	V_{DOL}	V_{CC} = Min, I_{DOL} = 3mA			0.4	V
Maximum Conversion Rate	F_{AS}	V_{CC} = Min, V_{EE} = Min	20			MSPS
Aperture Delay Time	t_{AP}	V_{CC} = Min, V_{EE} = Min	−10		0	ns
Digital Output Delay	t_D	V_{CC} = Min, V_{EE} = Min		15	20	ns
Clamp Level Sink Current	I_{22SNK}	Peak: off, Keyed: off	0		150	μA
Clamping Level Source Current	I_{22SOR}	Peak or Keyed: on	−250		0	μA
Peak Clamp Level Difference	$\triangle V_{Peak}$	$V_{22} - V_{21}$	−250	−100	0	mV
Keyed Clamp Level Difference	$\triangle V_{Keyed}$	$V_{22} - V_{21}$	−60		0	mV
Peak Clamp Charge Resistance	R_{Peak}	$\triangle V_{21}/\triangle I_{21}$, $V_{21} < V_{22}$		150		ohm
Keyed Clamp Charge Resistance	R_{Key}	$\triangle V_{21}/\triangle I_{21}$, $V_{21} < V_{22}$		150		ohm
Keyed Clamp Discharge Current	I_{Key}	$V_{21} > V_{22}$		100		μA
Static Differential Non Linearity	SDNL	A_{IN} = 1KHz, CK = 1MHz		0.2		%
Dynamic Differential Non Linearity	DDNL	A_{IN} = 1.02MHz, CK = 10MHz		0.3		%
		A_{IN} = 6.0018MHz, CK = 25MHz			0.6	%
Full Power Input Bandwidth	BW		6			MHz
Full Code Offset Error	E_{Full}	(Full Code Input) − (V_{ref})	0		+200	mV
Zero Code Offset Error	E_{Zero}	(Zero Code Input) − (V_{37})	−100		+100	mV
Signal to Noise Ratio	SNR	A_{IN} = 1.013MHz, CK = 25MHz	40			dB
(RMS Signal/RMS Noise)		A_{IN} = 3.601MHz, CK = 25MHz	36	39		dB
Differential Gain Error	DG	A_{IN} = 3.58649MHz, CK = 14.318MHz	−2		2	%
Differential Phase Error	DP	A_{IN} = 3.58649MHz, CK = 14.318MHz	−2		2	°C

TIMING DIAGRAM



① Sample
② Aperture Delay
③ Digital Output Delay
④ Data Valid (after Sample ①)
⑤ Transfer Time A/D

Fig. 3

INNER CONFIGURATION OF THE CONNECTION PINS

The following figures schematically show the circuitry at the various pins.

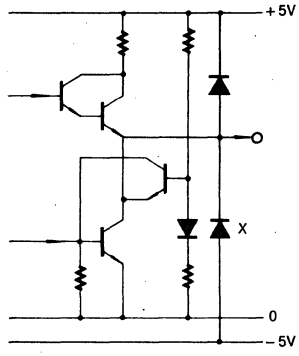


Fig. 4: Pin 4 to 11, Outputs

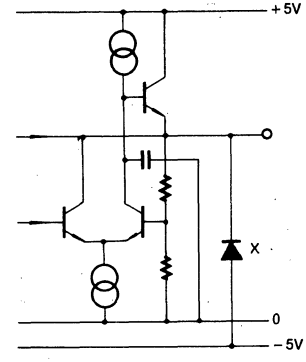


Fig. 5: Pin 16, Reference Voltage

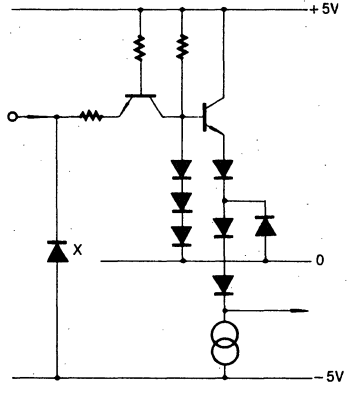


Fig. 6: Pin 17, 21 Input

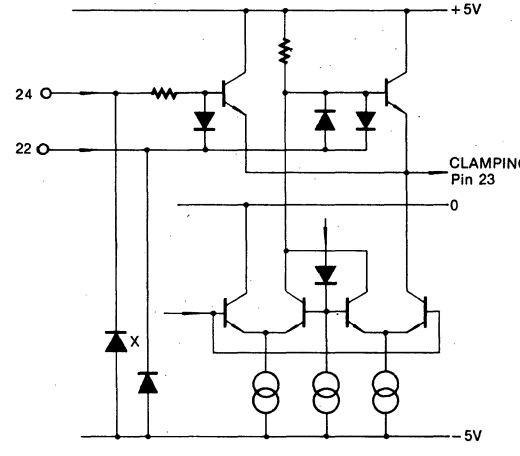


Fig. 7 Pins 22 and 24, Inputs

x: Protection Diode

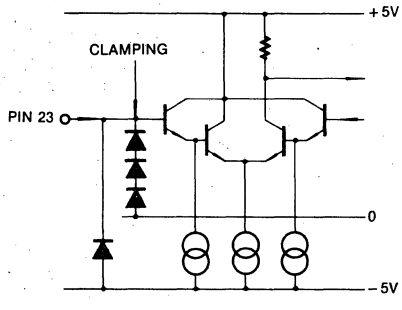


Fig. 8: Pin 23, Input

DESCRIPTION OF THE CONNECTIONS AND THE SIGNALS

Pin No.	Description
Pin 1	GND of Reference Resistor String This pin must be connected to the ground of the decoupling capacitor whitch is at pin 16.
Pin 2	+5 Volt Supply of ECL Logic Part, Digital This pin is the positive supply pin for the ECL logic part.
Pin 3	Digital Ground of ECL to TTL Translator Part. This pin is the digital ground connection for the TTL output stage where ECL level is translated to TTL level.
Pin 4 to Pin 11	Digital Outputs Bit 0 to Bit 7. Fig. 4 shows the diagram of there outputs which supply the digitized analog signal in parallel 8-bit code.
Pin 12	+5 Volt Supply off TTL Output Part, Digital This pin is the digital positive supply pin for the TTL output stage where ECL level is translated to TTL level.
Pin 14	Digital GND of ECL Logic Part This pin serves as the digital ground for the ECL logic part.
Pin 15	Analog GND of Input Stage This pin serves as the analog ground for the input stage; buffer amp, bandgap reference, clamp block.
Pin 16	+V_{REF}, Reference Voltage Point of Resistor String This pin whose diagram is shown is Fig. 5, is intended for connecting a decoupling capacitor to the A/D converter's reference voltage. The other end of this capacitor is connected to pin 1. (GND of Reference Resistor String).
Pin 17	Clock Input The diagram of this pin is shown in Fig. 6. Pin 17 is supplied with the clock of A/D converter.
Pin 19	+5 Volt Supply of Input Stage, Analog This pin is the analog positive supply pin for the input stage; bandgap reference.
Pin 20	−5 Volt Supply of Input Stage, Analog This pin is the analog negative supply pin for the input stage; buffer amp, bandgap reference, clamp block.
Pin 21	Clamping Pulse Input Fig. 6 is diagram of this pin. Pin 21 must be supplied with the key pulse if keyed clamping is required.
Pin 22	Clamping Level Input Via this pin whose diagram is shown is Fig. 7, the input of the A/D converter is supplied with the desired clamping level.
Pin 23	Analog Signal Input Fig. 8 is the diagram of this input. To pin 23 is applied the analog signal to be converted into digital.
Pin 24	Peak Clamp Enable Input Via pin 24 whose diagram is shown in Fig. 7, the peak clamping facilities can be enable.
Pin 27	Digital GND of ECL Clock Part This pin serves as the digital ground for the ECL clock block.
Pin 28	−5 Volt Supply of ECL Logic Part, Digital This pin is the digital negative supply for the ECL logic part.

APPENDIX: APPLICATION CIRCUITS

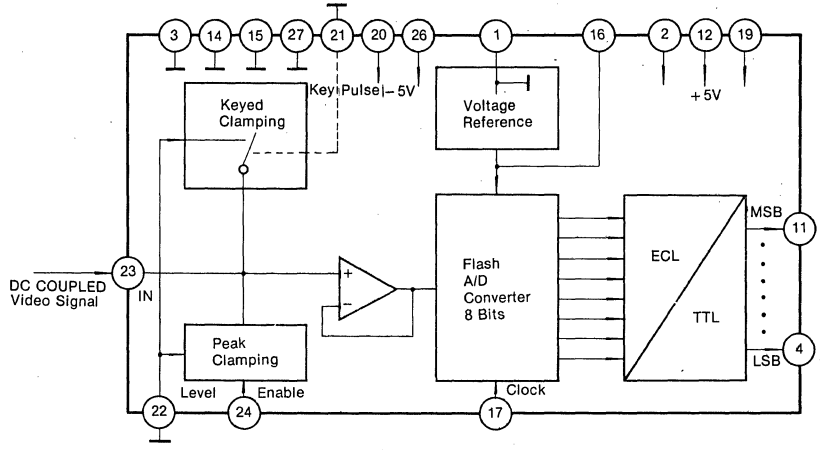


Fig. 9: Operation without clamping of the input signal
Pin 24 (peak clamping enable input) should be opened, while pin 21 (clamping pulse input) remains at 0V. The input signal is applied to the analog input, pin 23, without coupling capacitor such that it lies between 0 and + 2V

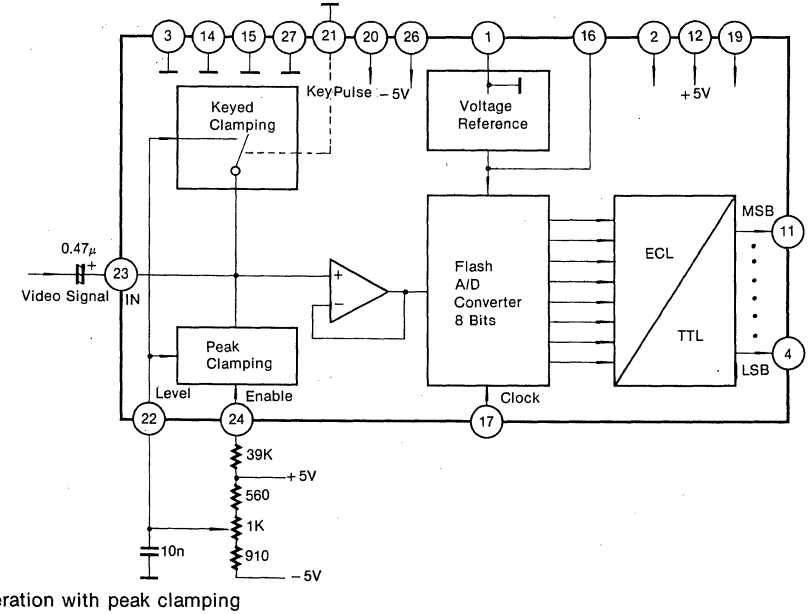


Fig. 10: Operation with peak clamping
The input signal is clamped automatically to the negative peak value. Pin 24 is connected to + 5V via a 39Kohm resistor and pin 22 (clamping level input) is connected, as desired, to zero or a voltage betgween – 1 and + 2V. The input signal is fed to pin 23 by way of a coupling capacitor, and no key pulse (clamping pulse) is needed.

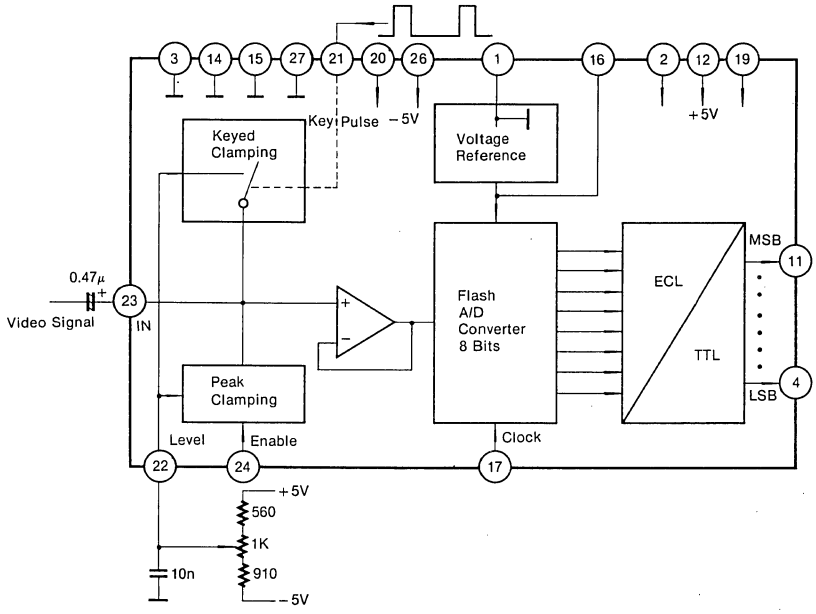
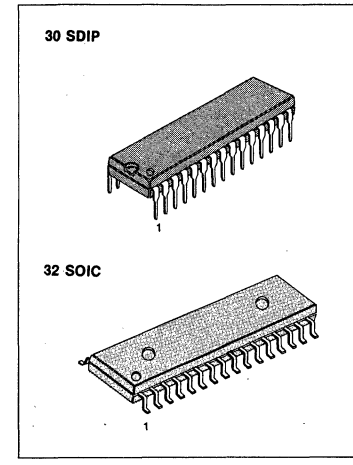


Fig. 11: Operation with keyed clamping

The input signal is applied to pin 23 through a coupling capacitor. Pin 24 must not be connected. While the input signal is at the desired clamping level, an high-level is applied at the clamping pulse input, pin 21. By this means the clamping switch in the KSV3208 connects the input with the clamping level at pin 22 and recharges the coupling capacitor accordingly. The clamping level can be set to zero or, by means of an external voltage devider, to any desired value between −1 and +2V.

HIGH SPEED A/D CONVERTER

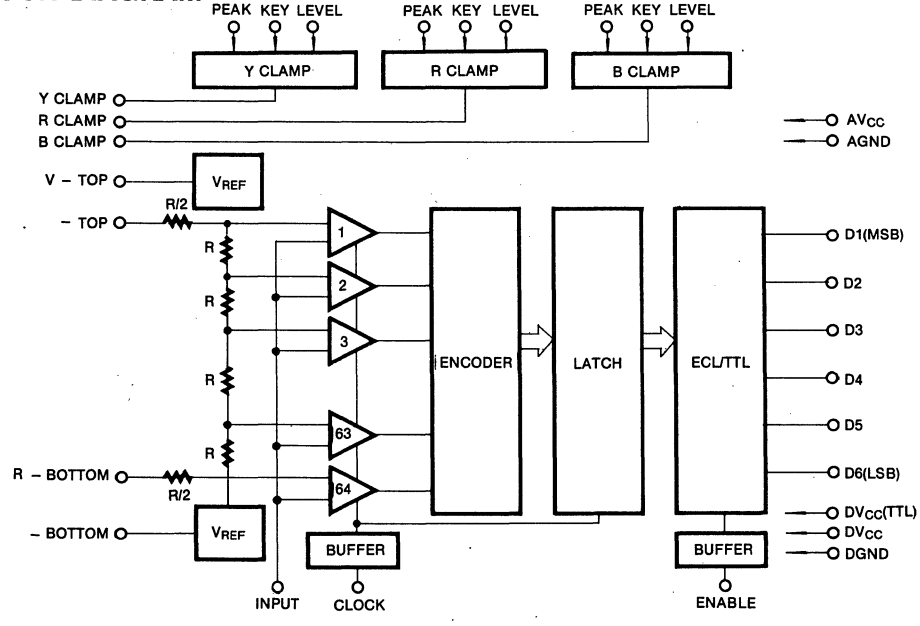


The KAD0206 is a monolithic 6 bit flash type ADC in which 2μm bipolar process is applied. Signal transformation up to 20 MSPS is available in the device and it is also ideal for converting wide band analog signal into digital signal.
The device has three different clamping functions. Also the range of optional external circuit can be easily modified into input dynamic range. Each clamping stages supplements keyed clamping function and peak clamping function which can be selected according to its use. Since the device has a large input resistance and small analog input capacitance, the input signal can be directly processed without buffer. Moreover, in order to simplify the application circuit, two different bandgap reference are provided for the top and the bottom of resistor string. Output data enable function quarentees easy applications of this data converter.

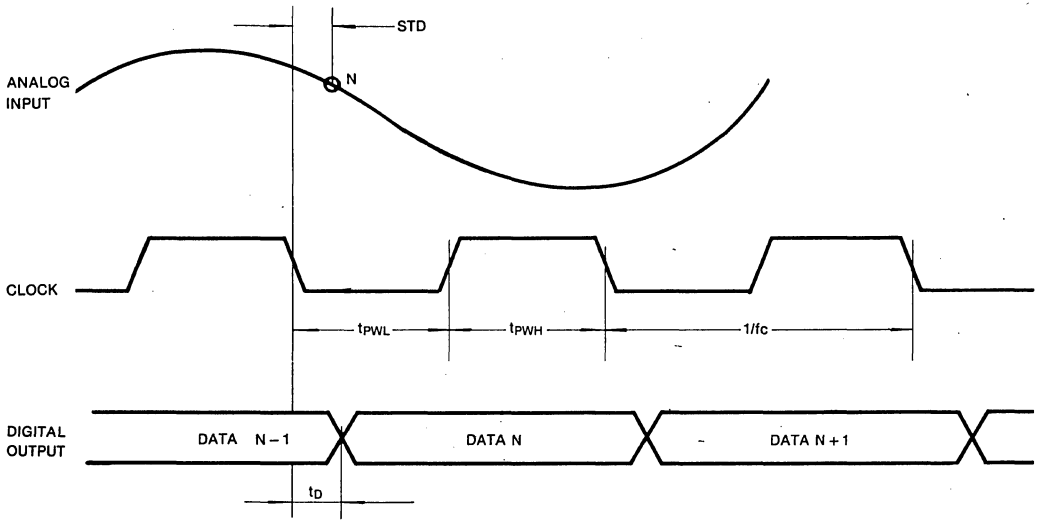
FEATURES

- **Resolution: 6 Bit**
- **Linearity error: under ± 1/2 LSB**
- **Maximum conversion rate: 20 MSPS**
- **Input full power bandwidth: 6 MHz**
- **Analog input dynamic range: 2.65V – 5.0V**
- **Clamp range: 2.65V – 3.75V**
- **Clock, enable, key pulse: TTL, CMOS compatible**
- **Data output level: TTL**
- **Single power supply: 5 ± 0.25V**
- **Low power dissipation: 300 mW (typ.)**
- **Data out enable: Active high or open**
- **Keyed clamp pulse input: Active high**
- **Pipe line delay: 0 clock**
- **Built-in 3.75V, 2.75V bandgap reference circuit**
- **Package: 30 SDIP 32 SOIC**

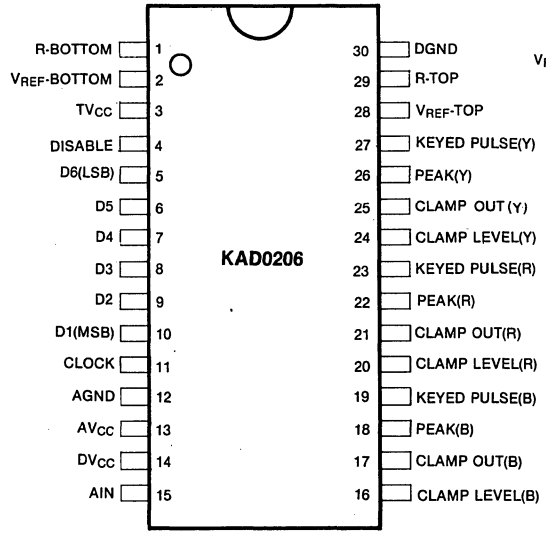
BLOCK DIAGRAM



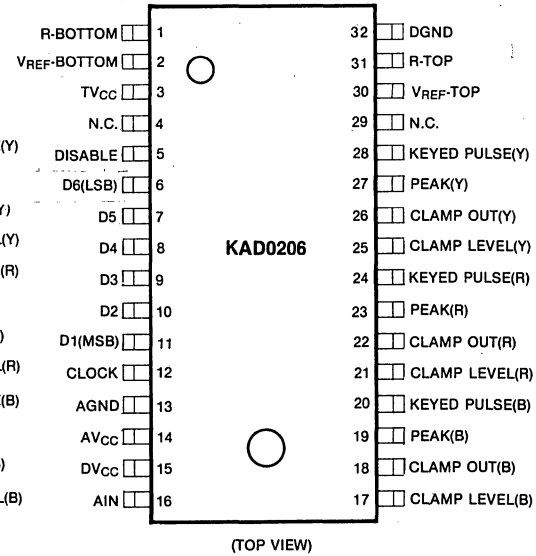
TIMING DIAGRAM



PIN CONFIGURATION



(TOP VIEW)
30 SDIP



(TOP VIEW)
32 SOIC

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Characteristics	Symbol	Value	Unit
Supply Voltage	V_{CCA}, V_{CCD}	−0.5 to 6.0	V
Supply Difference	$V_{CCA} - V_{CCD}$	−0.5 to 0.5	V
Digital Input Voltage	V_{DIN}	−0.5 to 6.0	V
Reference Voltage Difference	$V_{RT} - V_{RB}$	−1.5 to 1.5	v
Reference Voltage	V_{RT}, V_{RB}	2.5 to 6.5	V
Digital Output Current (Low)	I_{OL}	6	mA
Digital Output Current (High)	I_{OH}	2	mA
Ambient Operating Temperature Range	T_a	−25 ~ 95	°C
Storage Temperature Range	T_{stg}	−55 ~ 125	°C

Notes: 1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions.
2. Functional operation under any of these conditions is not implied.
3. Applied voltage must be current limited to specified range.
4. Current is specified as positive when flowing into the device.

RECOMMENDED OPERATING CONDITIONS

Characteristics	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CCA}, V_{CCD}	4.75	5.0	5.25	V
Supply Difference	$V_{CCA} - V_{CCD}$	−0.05	0	0.05	V
Reference Voltage Difference	$V_{RT} - V_{RB}$	0.8	1.0	1.2	V
Analog Input Voltage	V_{AIN}	V_{RB}	—	V_{RT}	V
Top Reference Voltage	V_{RT}	3.45	3.75	5.25	V
Bottom Reference Voltage	V_{RB}	2.65	2.75	4.45	V
Clock High Time	t_{PWH}	25			ns
Clock Low Time	t_{PWL}	25			ns
Digital Input Voltage, Low	V_{IL}			0.8	V
Digital Input Voltage, High	V_{IH}	2.0			V
Clamp Level Range	V_{clamp}	2.65		3.75	V
Peak Clamp Enable Resistor	R_{peak}	2	3	5	Kohm
Ambient Operating Temperature Range	T_a	0		70	°C
Digital Output Current, Low	I_{OL}			4	mA
Digital Output Current, High	I_{OH}			−0.4	mA

D.C. ELECTRICAL CHARACTERISTICS WITHIN SPECIFIED CONDITION

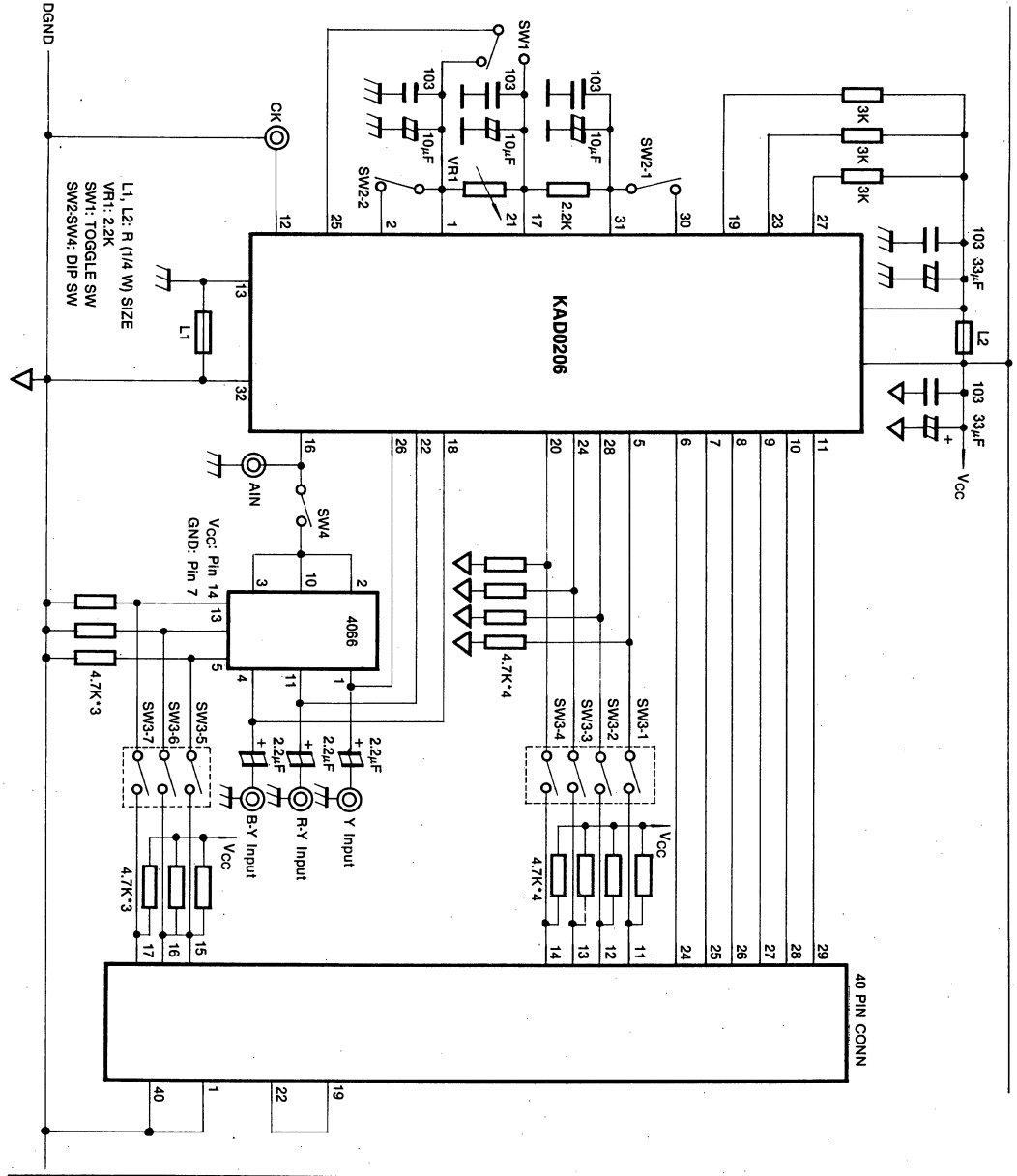
Characteristics	Symbol	Test Condition	Min	Typ	Max	Unit
Supply Current	$I_{CCD} + I_{CCA}$	V_{CC} = Max		60	80	mA
Reference Current	I_{REF}	$V_{RT} - V_{RB}$ = 1V		5	8	mA
Reference Resistor	R_{REF}	Ta = 25°C	140	200	260	ohm
Analog Input Equivalent Resistor	R_{AIN}	$V_{AIN} = V_{RT}$	100			Kohm
Analog Input Capacitance	C_{AIN}	$V_{AIN} = V_{RT}$		30	60	pF
Analog Input Current	I_{AIN}	V_{CC} = Max, $V_{AIN} = V_{RT}$		40	70	μA
Digital Input Current, Low	I_{IL}	V_{CC} = Max, V_I = 0.4V		− 100	− 400	μA
Digital Input Current, High	I_{IH}	V_{CC} = Max, V_I = 2.4V		100	200	μA
Digital Maximum Input Current	I_{IM}	V_{CC} = Max, V_I = 5.25V			500	μA
Output Voltage, High	V_{OH}	V_{CC} = Min, I_{OH} = Max	2.7			V
Output Voltage, Low	V_{OL}	V_{CC} = Min, I_{OL} = Max			0.4	V
Clamp Level Input Current 1	$I_{CLAMP}(1)$	V_{LEVEL} = 3.0V, Key = 'H'		10	30	μA
Clamp Level Input Current 2	$I_{CLAMP}(2)$	V_{LEVEL} = 3.0V, Key = 'L'		20	40	μA
Keyed Clamp Out Level Difference	$\triangle V_{CLAMP}$	V_{LEVEL} = 3.0V, Key = 'H'	− 100	0	100	mV
Bottom Bandgap Reference Voltage	V_{BTM}	Ta = 25°C	2.65	2.75	2.85	V
Top Bandgap Reference Voltage	V_{TOP}	Ta = 25°C	3.65	3.75	3.85	V
Reference Voltage Variation	$\triangle(V_T - V_B)$	Ta = 0°C ~ 70°C			28	mV

A.C. ELECTRICAL CHARACTERISTICS WITHIN SPECIFIED CONDITION

Characteristics	Symbol	Test Condition	Min	Typ	Max	Unit
Maximum Conversion Rate	f_C	V_{CC} = Min			20	MSPS
Sampling Time Offset	t_{STD}	V_{CC} = Min			20	ns
Digital Output Delay	t_D	V_{CC} = Min			20	ns

PERFORMANCE CHARACTERISTICS WITHIN SPECIFIED CONDITION

Characteristics	Symbol	Test Condition	Min	Typ	Max	Unit
Differential Linearity Error	E_{LD}	V_{CC} = Typ			± 0.8	%
Integral Linearity Error	E_{LI}	V_{CC} = Typ			± 0.8	%
Full-Power Input Bandwidth	BW	f_C = Max			6	MHz
Top Offset Error	E_{OT}	$V_{AIN} = V_{RT}$			50	mV
Bottom Offset Error	E_{OB}	$V_{AIN} = V_{RB}$			− 50	mV
Differential Gain	DP	f_C = 4 fsc			2	°C
Differential Phase	DG	f_C = 4 fsc			2	%

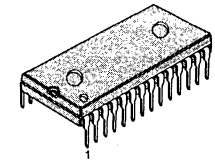

KAD0206
DGND
CK
SW1
SW2-1
SW2-2
VR1
2.2K
10μF
103
3K
33μF
L1
L2
VCC
AIN
SW4
4066
4.7K*4
4.7K*3
SW3-1
SW3-2
SW3-3
SW3-4
SW3-5
SW3-6
SW3-7
2.2μF
Y Input
R-Y Input
B-Y Input
40 PIN CONN
L1, L2: R (1/4 W) SIZE
VR1: 2.2K
SW1: TOGGLE SW
SW2-SW4: DIP SW
VCC: Pin 14
GND: Pin 7

8-BIT μP-COMPATIBLE A/D CONVERTERS WITH 8-CHANNEL MULTIPLEXER

The KAD0808/KAD0809 Analog to Digital converter is a monolithic CMOS device with an 8-bit resolution, 8-channel input multiplexer and microprocessor compatible control logic. It uses successive approximation as the conversion technique.

The design of the KAD0808/KAD0809 has been optimized by incorporating the most desirable aspects of several A/D conversion techniques. The KAD0808/KAD0809 offers high speed, high accuracy, minimal temperature dependence, excellent long-term accuracy and repeatability, and consumes minimal power.

28 DIP



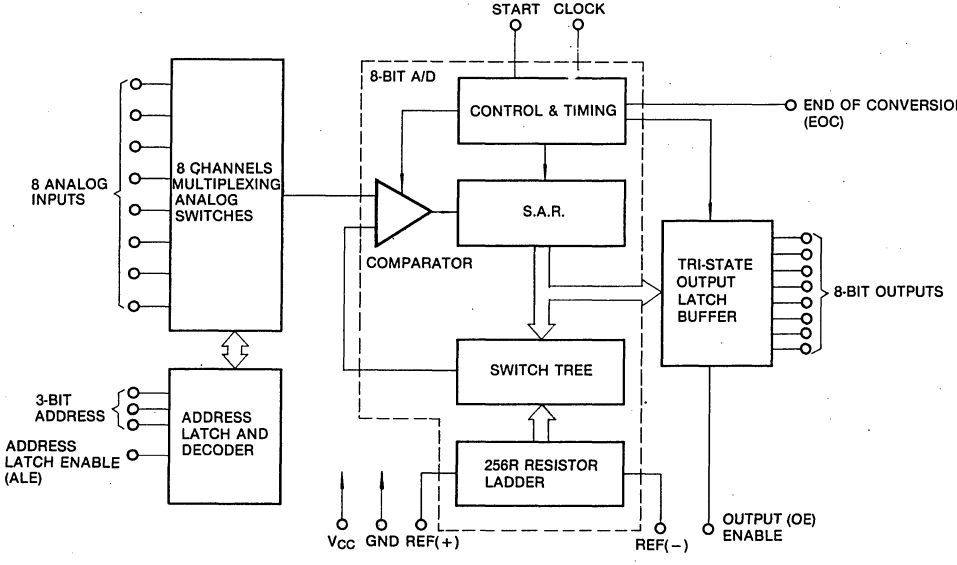
FEATURES

- **Total unadjusted error— ±1/2 LSB or ±1 LSB**
- **Resolution—8-bits**
- **Conversion time—100μS**
- **No missing codes**
- **Latched TRI-STATE output**
- **Easy interface to all microprocessors, or operates "stand alone"**
- **Single supply—5 V_{DC}**
- **8-channel multiplexer with latched control logic**
- **Outputs meet TTL voltage level specifications**
- **0V to 5V analog input voltage range with single 5V supply**
- **No zero or full-scale adjust required**
- **Standard 28-pin DIP package**

ORDERING INFORMATION

Device	Package	Temperature Range	Diff. Nonlinearity
KAD0808IN	28 DIP	−40°C ~ +85°C	±1/2 LSB
KAD0809IN			±1 LSB

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Note 1 & 2)

Characteristic	Symbol	Value	Unit
Supply Voltage (Note 3)	V_{CC}	6.5	V
Voltage at Any Pin Except Control Inputs	V_I	$-0.3V \sim (V_{CC}+0.3V)$	V
Voltage at Control Inputs	V_I	$-0.3V \sim +15V$	V
Package Dissipation at Ta = 25°C	P_D	875	mW
Operating Temperature	T_{opr}	$-40°C \sim +85°C$	°C
Storage Temperature Range	T_{stg}	$-65°C \sim +125°C$	°C

ELECTRICAL CHARACTERISTICS

Converter Specifications: $V_{CC}=5$ $V_{DC}=V_{ref(+)}$, $V_{ref(-)}=GND$, $T_f=T_r=20ns$ and $f_{CLK}=640KHz$ unless otherwise stated.

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
KAD0808						
Total Unadjusted Error		25°C	—	—	±1/2	LSB
(Note 5)		−40°C ~ 85°C	—	—	±3/4	LSB
KAD0809		0°C ~ 70°C	—	—	±1	LSB
Total Unadjusted Error						
(Note 5)		−40°C ~ 85°C	—	—	$\pm 1\frac{1}{4}$	LSB
Input Resistance	R_{ref}	From Ref(+) to Ref(−)	1.0	2.5	—	KΩ
Analog Input Voltage Range	V_{in}	(Note 4) V(+) or V(−)	GND − 0.10	—	$V_{CC}+0.10$	V
Comparator Input Current	I_{on}	$f_C=640KHz$, (Note 6)	−2	±0.5	2	μA
Analog Multiplexer						
OFF Channel Leakage Current	$I_{OFF(+)}$	$V_{CC}=5V$, $V_{IN}=5V$, Ta = 25°C	—	10	200	nA
OFF Channel Leakage Current	$I_{OFF(-)}$	$V_{CC}=5V$, $V_{IN}=0$, Ta = 25°C	−200	−10	—	nA
Control Inputs						
Logical "1" Input Voltage	V_{IH}		$V_{CC}-1.5$	—	V_{CC}	V
Logical "0" Input Voltage	V_{IL}			—	1.5	V
Supply Current	I_{CC}	$f_{CLK}=640KHz$	—	0.3	3.0	mA
Logical "1" Output Voltage	V_{OH}	$I_O=-360\mu A$	$V_{CC}-0.4$	—		V
Logical "0" Output Voltage	V_{OL}	$I_O=1.6mA$		—	0.45	V
Logical "0" Output Voltage EOC	$V_{OUT(0)}$	$I_O=1.2mA$		—	0.45	V
TRI-STATE Output Current	I_{OUT}	$V_O=5V$	—	—	3	μA
		$V_O=0$	−3	—	—	μA

ELECTRICAL CHARACTERISTICS

Timing Specifications $V_{CC} = V_{ref(+)} = 5V$, $V_{ref(-)} = GND$, $t_r = t_f = 20ns$ and $Ta = 25°C$ unless otherwise noted.

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Minimum Start Pulse Width	t_{WS}	(Figure 5)	—	100	200	ns
Minimum ALE Pulse Width	t_{WALE}	(Figure 5)	—	100	200	ns
Minimum Address Set-Up Time	t_s	(Figure 5)	—	25	50	ns
Minimum Address Hold Time	t_h	(Figure 5)	—	25	50	ns
Analog MUX Delay Time From ALE	t_d	$R_S = 0\Omega$ (Figure 5)	—	1	2.5	μS
OE Control to Q Logic State	t_{H1}, t_{H0}	$C_L = 50pF$, $R_L = 10K$ (Figure 8)	—	125	250	ns
OE Control to Hi-Z	t_{1H}, t_{0H}	$C_L = 10pF$, $R_L = 10K$ (Figure 8)	—	125	250	ns
Conversion Time	t_{CON}	$f_c = 640KHz$, (Figure 5)	90	100	116	μS
Clock Frequency	f_{CLK}		10	640	1280	KHz
Input Capacitance	C_{IN}	At Control Inputs	—	10	15	pF
TRI-STATE Output Capacitance	C_{OUT}	At TRI-STATE Outputs	—	10	15	pF

Note 1: Absolute maximum ratings are those values beyond which the life of the device may be impaired.

Note 2: All voltages are measured with respect to GND, unless otherwise specified.

Note 3: A zener diode exists, Internally, from V_{CC} to GND and has a typical breakdown voltage of 7 V_{DC}.

Note 4: Two on-chip diodes are tied to each analog input which will forward conduct for analog input voltages one diode drop below ground or one diode drop greater than the V_{CC} supply. The spec allows 100mV forward bias of either diode. This means that as long as the analog V_{IN} does not exceed the supply voltage by more than 100mV, the output code will be correct. To achieve an absolute $0V_{DC}$ to $5V_{DC}$ input voltage range will therefore require a minimum supply voltage 4.900 V_{DC} over temperature variations, initial tolerance and loading.

Note 5: Total unadjusted error includes offset, full-scale, linearity, and multiplexer errors. See Figure 3. None of those A/Ds requires a zero or full-scale adjust. However, if an all zero code is desired for an analog input other than 0.0V, or if a narrow full-scale span exists (for example: 0.5V to 4.5V full-scale) the reference voltages can be adjusted to achieve this. See Figure 13.

Note 6: Comparator input current is a bias current into or out of the chopper stabilized comparator. The bias current varies directly with clock frequency and has little temperature dependence (Figure 6).

FUNCTIONAL DESCRIPTION

Multiplexer. The device contains an 8-channel single-ended analog signal multiplexer. A particular input channel is selected by using the address decoder. Table 1 shows the input states for the address lines to select any channel. The address is latched into the decoder on the low-to-high transition of the address latch enable signal.

Selected Analog Channel	Address Line		
	C	B	A
IN0	L	L	L
IN1	L	L	H
IN2	L	H	L
IN3	L	H	H
IN4	H	L	L
IN5	H	L	H
IN6	H	H	L
IN7	H	H	H

CONVERTER CHARACTERISTICS

The Converter

The heart of this single chip data acquisition system is its 8-bit analog-to-digital converter. The converter is designed to give fast, accurate, and repeatable conversions over a wide range of temperatures. The converter is partitioned into 3 major sections: the 256R ladder network, the successive approximation register, and the comparator. The converter's digital outputs are positive true.

The 256R ladder network approach (Figure 1) was chosen over the conventional R/2R ladder because of its inherent monotonicity, which guarantees no missing digital codes. Monotonicity is particularly important in closed loop feedback control systems. A non-monotonic relationship can cause oscillations that will be catastrophic for the system. Additionally, the 256R network does not cause load variations on the reference voltage.

The bottom resistor and the top resistor of the ladder network in Figure 1 are not the same value as the remainder of the network. The difference in these resistors causes the output characteristic to be symmetrical with the zero and full-scale points of the transfer curve. The first output transition occurs when the analog signal has reached +1/2 LSB and succeeding output transitions occur every 1 LSB later up to full-scale.

The successive approximation register (SAR) performs 8 iterations to approximate the input voltage. For any SAR type converter, n-iterations are required for an n-bit converter. Figure 2 shows a typical example of a 3-bit converter. In the KAD0808, KAD0809 the approximation technique is extended to 8 bits using the 256R network.

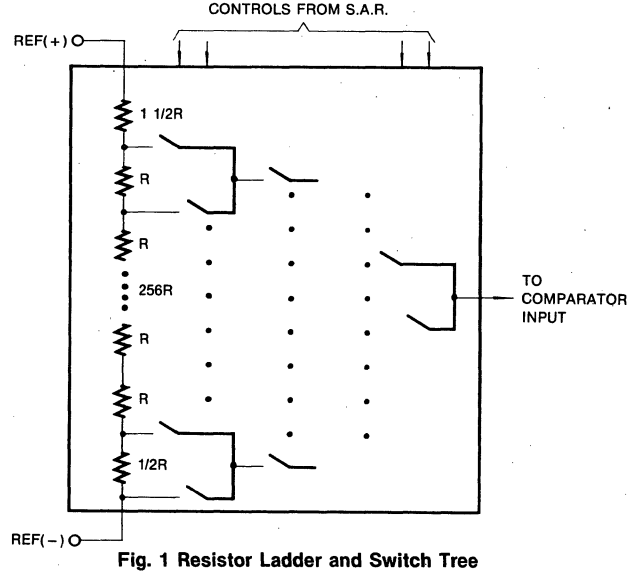


Fig. 1 Resistor Ladder and Switch Tree

FUNCTIONAL DESCRIPTION (Continued)

The A/D converter's successive approximation register (SAR) is reset on the positive edge of the start conversion (SC) pulse. The conversion is begun on the falling edge of the start conversion pulse. A conversion in process will be interrupted by receipt of a new start conversion pulse. Continuous conversion may be accomplished by tying the end-of-conversion (EOC) output to the SC input. If used in this mode, an external start conversion pulse should be applied after power up. End-of-conversion will go low between 0 and 8 clock pulses after the rising edge of start conversion.

The most important section of the A/D converter is the comparator. It is this section which is responsible for the ultimate accuracy of the entire converter. It is also the comparator drift which has the greatest influence on the repeatability of the device. A chopper-stabilized comparator provides the most effective method of satisfying all the converter requirements.

The chopper-stabilized comparator converts the DC input signal into an AC signal. This signal is then fed throught a high gain AC amplifier and has the DC level restored. This technique limits the drift component of the amplifier since the drift is a DC component which is not passed by the AC amplifier. This makes the entire A/D converter extremely insensitive to temperature, long term drift and input offset errors.

Figure 4 shows a typical error curve for the KAD0808.

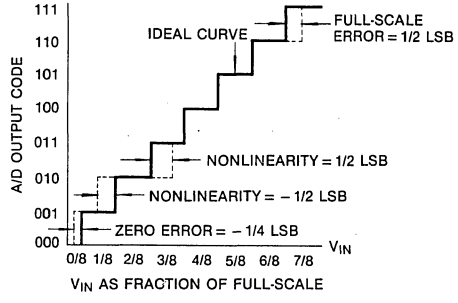


Fig. 2 3-Bit A/D Transfer Curve

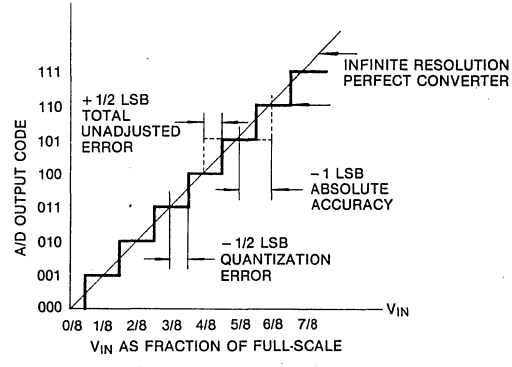


Fig. 3 3-Bit A/D Absolute Accuracy Curve

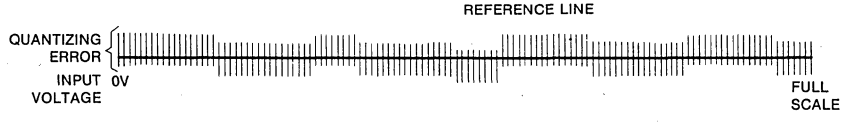
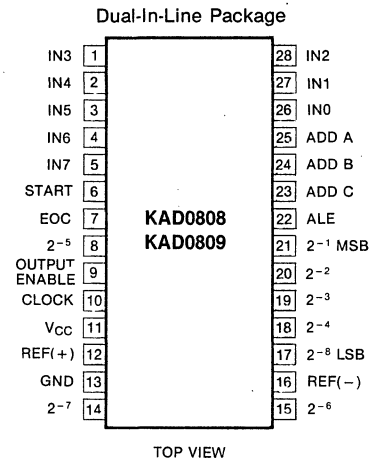


Fig. 4 Typical Error Curve

PIN CONFIGURATION



TIMING DIAGRAM

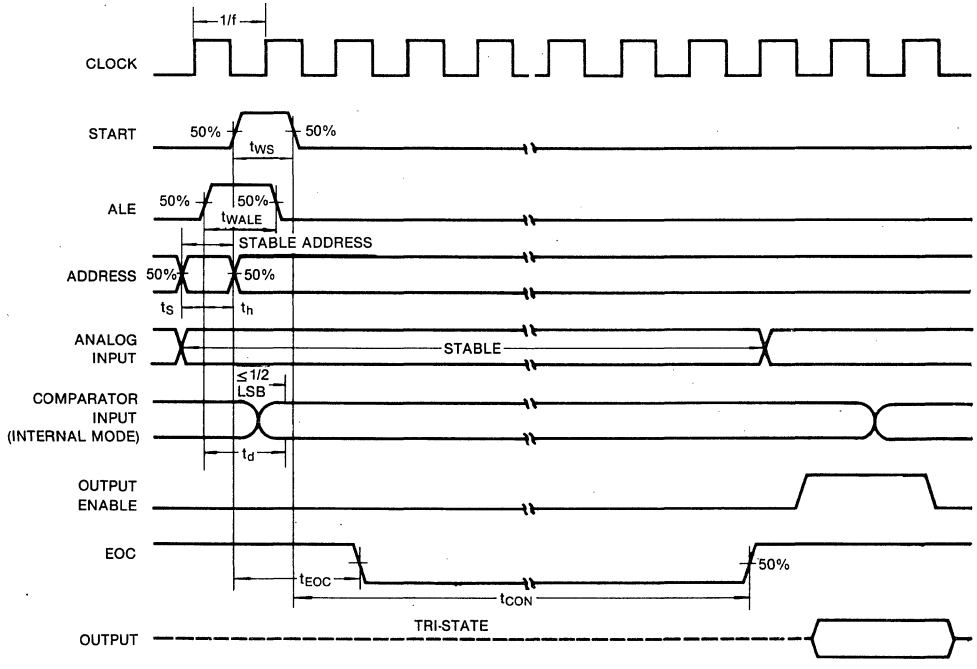


Fig. 5

TYPICAL PERFORMANCE CHARACTERISTICS

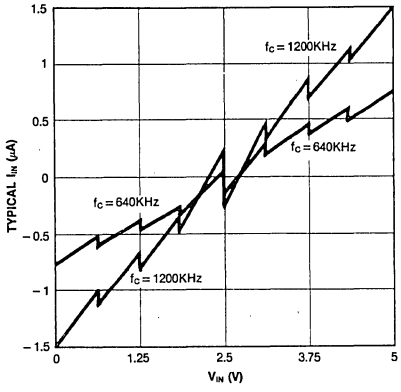


Fig. 6 Comparator I_{IN} vs V_{IN} ($V_{CC} = V_{REF} = 5V$)

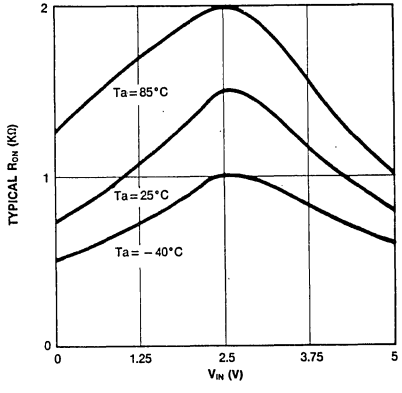


Fig. 7 Multiplexer R_{ON} vs V_{IN} ($V_{CC} = V_{REF} = 5V$)

TRI-STATE TEST CIRCUITS AND TIMING DIAGRAMS

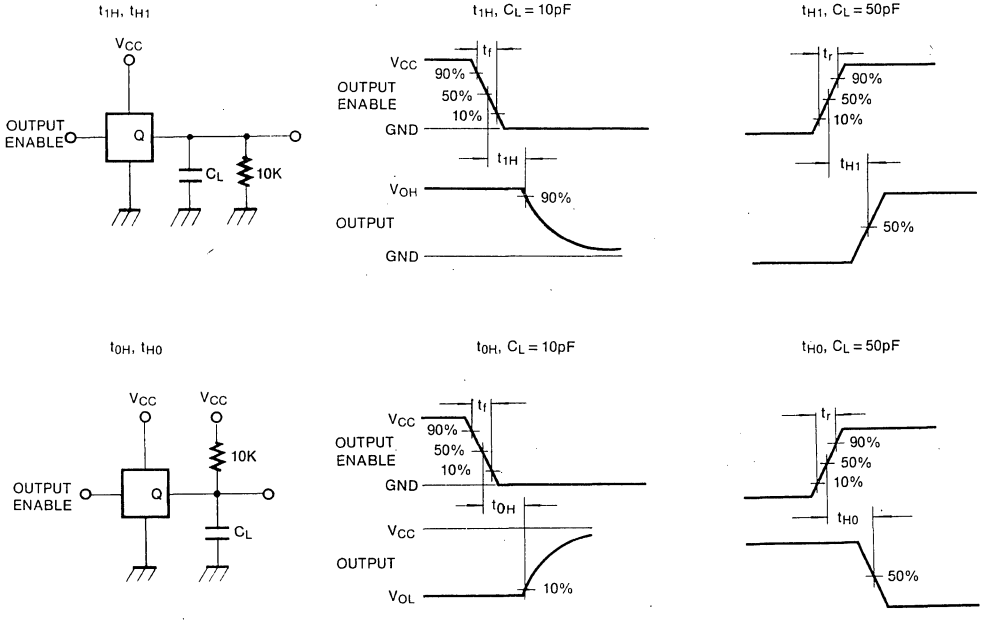


Fig. 8

APPLICATIONS INFORMATION

OPERATION

1.0 Ratiometric Conversion

The KAD0808, KAD0809 is designed as a complete Data Acquisition System (DAS) for ratiometric conversion systems. In ratiometric systems, the physical variable being measured is expressed as a percentage of full-scale which is not necessarily related to an absolute standard. The voltage input to the KAD0808 is expressed by the equation.

$$\frac{V_{IN}}{V_{fs} - V_Z} = \frac{D_X}{D_{max} - D_{min}}$$

V_{IN} = Input voltage into the KAD0808
V_{fs} = Full-scale voltage
V_Z = Zero voltage
D_X = Data point being measured
D_{max} = Maximum data limit
D_{min} = Minimum data limit

A good example of a ratiometric transducer is a potentiometer used as a position sensor. The position of the wiper is directly proportional to the output voltage which is a ratio of the full-scale voltage across it. Since the data is represented as a proportion of full-scale, reference requirements are greatly reduced, eliminating a large source of error and cost for many applications. A major advantage of the KAD0808, KAD0809 is that the input voltage range is equal to the supply range so the transducers can be connected directly across the supply and thier outputs connected directly into the multiplexer inputs, (Figure 9).

Ratiometric transducers such as potentiometers, strain gauges, thermistor bridges, pressure transducers, etc., are suitable for measuring proportional relationships; however, many types of measurements must be referred to an absolute standard such as voltage or current. This means a system reference must be used which relates the full-scale voltage to the standard volt. For example, if $V_{CC} = V_{REF} = 5.12V$, then the full-scale range is divided into 256 standard steps. The smallest standard step is a LSB which is then 20mV.

2.0 Resistor Ladder Limitations

The voltages from the resistor ladder are compared to the selected into 8 times in a conversion. These voltages are coupled to the comparator via an analog switch tree which is referenced to the supply. The voltages at the top, center and bottom of the ladder must be controlled to maintain proper operation.

The top of the ladder, Ref(+), should not be more positive than the supply, and the bottom of the ladder, Ref(−), should not be more negative than ground. The center of the ladder voltage must also be near the center of the supply because the analog switch tree changes from N-channel switches to P-channel switches. These limitations are automatically satisfied in ratiometric systems and can be easily met in ground referenced systems.

Figure 10 shows a ground referenced system with a separate supply and reference. In this system, the supply must be trimmed to match the reference voltage. For instance, if a 5.12V is used, the supply should be adjusted to the same voltage within 0.1V.

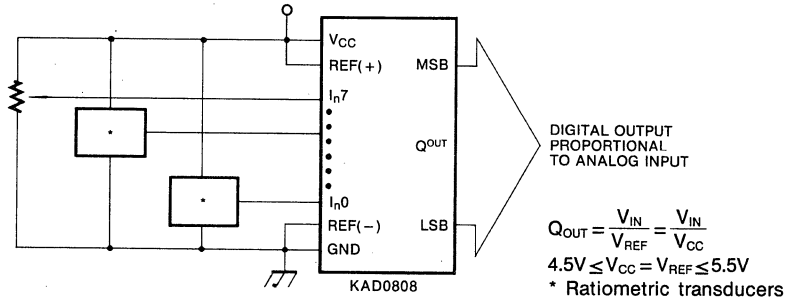


Fig. 9 Ratiometric Conversion System

APPLICATIONS INFORMATION (Continued)

The KAD0808 needs less than a milliamp of supply current so developing the supply from the reference is readily accomplished. In Figure 11 a ground referenced system is shown which generates the supply from the reference. The buffer shown can be an op amp of sufficient drive to supply the milliamp of supply current and the desired bus drive, or if a capacitive bus is driven by the outputs a large capacitor will supply the transient supply current as seen in Figure 12. The KA301A is overcompensated to insure stability when loaded by the 10μF output capacitor.

The top and bottom ladder voltages cannot exceed V_{CC} and ground, respectively, but they can be symmetrically less than V_{CC} and greater than ground. The center of the ladder voltage should always be near the center of the supply. Sensitivity of the converter can be increased, (i.e., size of the LSB steps decreased) by using a symmetrical reference system. In Figure 13, a 2.5V reference is symmetrically centered about $V_{CC}/2$ since the same current flows in identical resistors. This system with a 2.5V reference allows the LSB bit to be half the size of a 5V reference system.

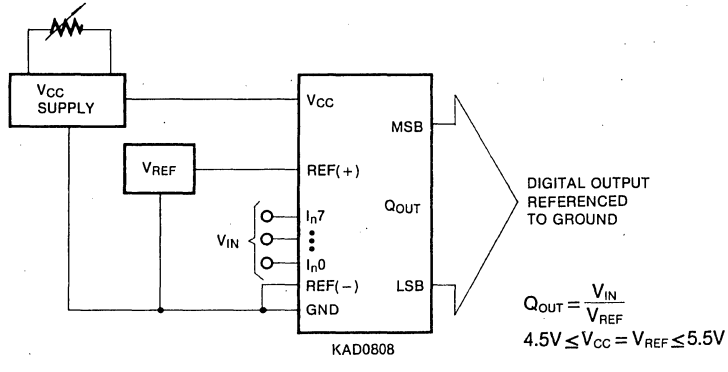


Fig. 10 Ground Referenced Conversion System Using Trimmed Supply

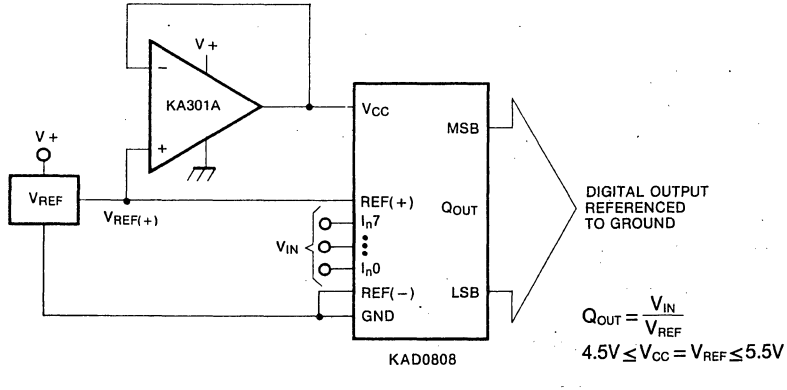


Fig. 11 Ground Referenced Conversion System with Reference Generating V_{CC} Supply

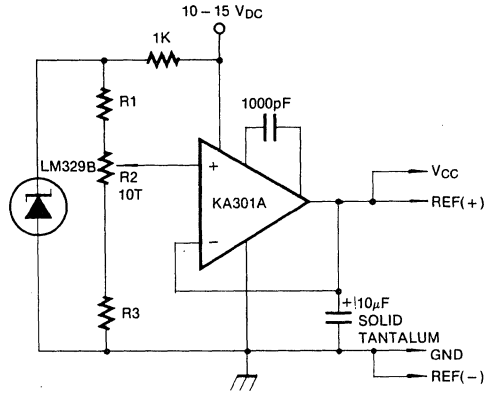


Fig. 12 Typical Reference and Supply Circuit

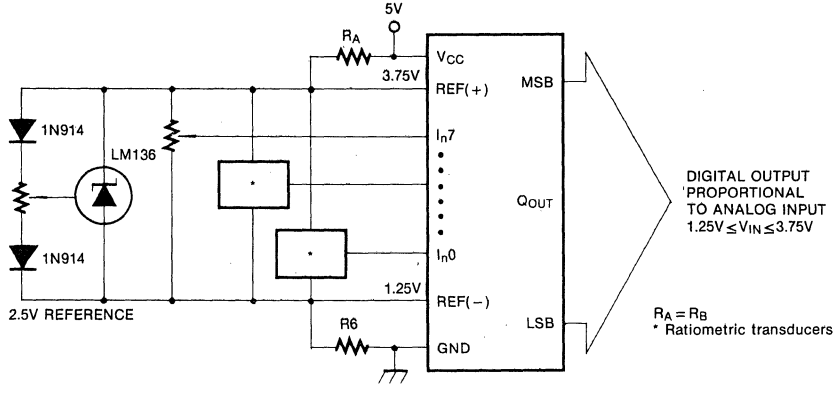


Fig. 13 Symmetrically Centered Reference

3.0 Converter Equations

The transition between adjacent codes N and N + 1 is givn by:

$$V_{IN} = \{(V_{REF(+)} - V_{REF(-)}) \left[\frac{N}{256} + \frac{1}{512}\right] \pm V_{TUE}\} + V_{REF(-)}$$

The center of an output code N is given by:

$$V_{IN}\{(V_{REF(+)} - V_{REF(-)})\left[\frac{N}{256}\right] \pm V_{TUE}\} + V_{REF(-)}$$

The output code N for an arbitrary input are the integers within the range:

$$N = \frac{V_{IN} - V_{REF(-)}}{V_{REF(+)} - V_{REF(-)}} \times 256 \pm \text{Absolute Accuracy}$$

Where: V_{IN} = Voltage at comparator input
$V_{REF(+)}$ = Voltage at Ref(+)
$V_{REF(-)}$ = Voltage at Ref(–)
V_{TUE} = Total unadjusted error voltage (typically $V_{REF(+)} \div 512$)

4.0 Analog Comparator Inputs

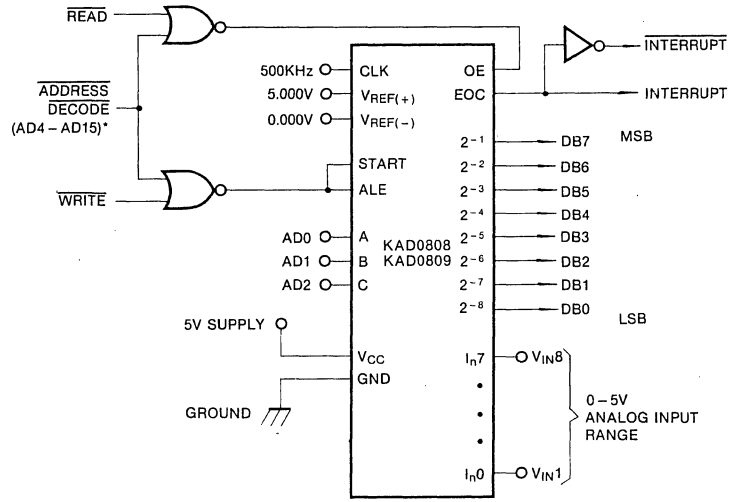
The dynamic comparator input current is caused by the pariodic switching of on-chip stray capacitances. These are connected alternately to the output of the resistor ladder/switch tree network and to the comparator input as part of the operation of the chopper stabilized comparator.

The average value of the comparator input current varies directly with clock frequency and with V_{IN} as shown in Figure 6.

If no filter capacitors are used at the analog inputs and the signal source impedances are low, the comparator input current should not introduced converter errors, as the transient created by the capacitance discharge will die out before the comparator output is strobed.

If input filter capacitors are desired for noise reduction and signal conditioning they will tend to average out the dynamic comparator input current. I will then take on the characteristics of a DC bias current whose effect can be predicted conventionally.

TYPICAL APPLICATION

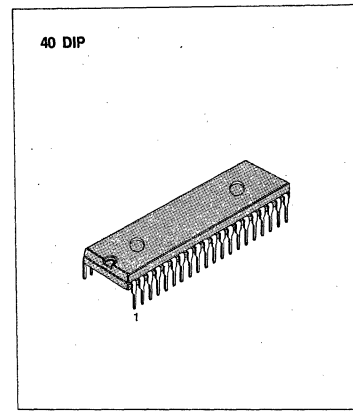


* Address latches needed for 8085 and SC/MP interfacing the KAD0808 to a microprocessor

MICROPROCESSOR INTERFACE TABLE

Processor	$\overline{\text{Read}}$	$\overline{\text{Write}}$	Interrupt (Comment)
8080	$\overline{\text{MEMR}}$	$\overline{\text{MEMW}}$	INTR (Thru RST Circuit)
8085	$\overline{\text{RD}}$	$\overline{\text{WR}}$	INTR (Thru RST Circuit)
Z-80	$\overline{\text{RD}}$	$\overline{\text{WR}}$	$\overline{\text{INT}}$ (Thru RST Circuit, Mode 0)
SC/MP	NRDS	NWDS	SA (Thru Sense A)
6800	VMA• ϕ 2•R/W	VMA• ϕ •$\overline{\text{R/W}}$	$\overline{\text{IRQA}}$ or $\overline{\text{IRQB}}$ (Thru PIA)

8-BIT μP-COMPATIBLE A/D CONVERTERS WITH 16-CHANNEL MULTIPLEXER



The KAD0816/KAD0817 Analog to Digital Converter is a Monolithic

Silicon gate CMOS Device with 8-bit resolution. It is 16-channel input multiplexer and microprocessor compatible logic. It uses successive approximation as the conversion technique which includes 256R potentiometer divider with switch tree and charge balancing comparator with high input impedance and successive approximation register etc.
It also confirms monotonicity and no missing codes. The 16-channel multiplexer can directly access any of 16-analog signal based on address combination. The single 5 volts supply and low power consumption enable KAD0816, KAD0817 especially to be useful for a wide variety of applications.

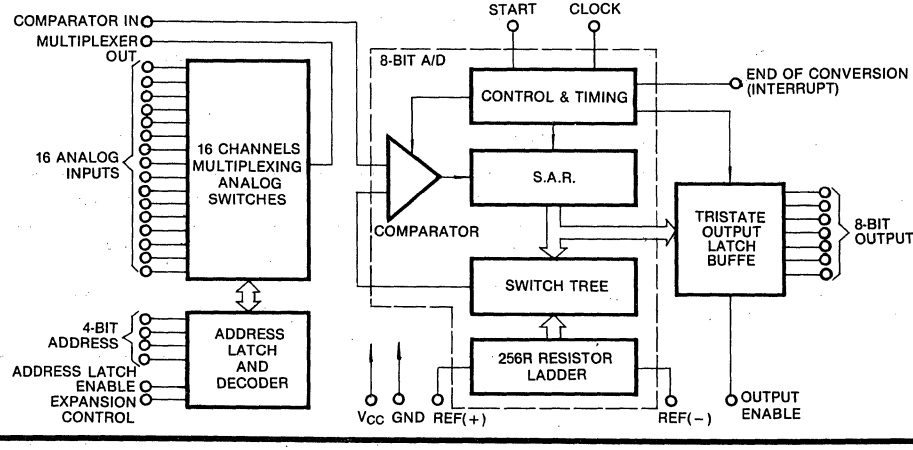
ORDERING INFORMATION

Device	Package	Temperature Range	Diff. Nonlinearity
KAD0816IN	40 DIP	−40°C ~ +85°C	±1/2 LSB
KAD0817IN			±1LSB

FEATURES

- **Total unadjusted error: ±1/2 LSB for KAD0816 and ±1 LSB for KAD0817**
- **Resolution: 8 Bits**
- **100μs conversion time**
- **Monotonicity and no missing codes**
- **Easy interface with microprocessors, or operates 'Stand Alone'**
- **Latched tri-state outputs**
- **Output meets TTL level**
- **Latched address inputs**
- **Single 5 volts supply**
- **Low power consumption**
- **Designed to be interchangeable with National Semiconductor ADC0816, ADC0817 and Texas Instruments ADC0816, ADC0817**

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3~7.0	V
Voltage at Any Pin Except Control Inputs	V_I	−0.3~(V_{CC}+0.3)	V
Voltage at Control Inputs	V_I	−0.3~+15	V
Package Dissipation at Ta=25°C	P_D	875	mW
Operating Temperature Range	T_{opr}	−40~+85	°C
Storage Temperature Range	T_{stg}	−65~+125	°C

ELECTRICAL CHARACTERISTICS

(Converter Specifications: $V_{CC}=5$ $V_{DC}=V_{ref(+)}$, $V_{ref(-)}=GND$, $T_f=T_r=20ns$ and $f_{CLK}=640KHz$, unless otherwise stated)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Voltage	V_{CC}		4.5	5	5.5	V
KAD0816 Total Unadjusted Error		25°C −40°C to 85°C			±1/2 ±3/4	LSB LSB
KAD0817 Total Unadjusted Error		0°C to 70°C −40°C to 85°C			±1 ±1.25	LSB LSB
Input Resistance	R_{ref}	From $V_{ref(+)}$ to $V_{ref(-)}$	1	4.5		KΩ
Analog Input Voltage Range	V_{IN}		GND −0.1		V_{CC} +0.1	V_{DC}
Comparator Input Current	I_{on}	Clock=640KHz	−2		2	μA
Off Channel Leakage	I_{off}	Clock=640KHz	−2 00		 200	 nA
Control Inputs High Level	V_{IH}	$V_{CC}=5V$	V_{CC} −1.5			V
Control Inputs Low Level	V_{IL}	$V_{CC}=5V$			1.5	V
Supply Current	I_{CC}	$V_{CC}=5V$		0.3	3.0	mA
Logical "1" Output	V_{OH}	$I_{source}=360\mu A$ $V_{CC}=5V$	4.6			V

ELECTRICAL CHARACTERISTICS

(Timing Specifications: $V_{CC} = V_{ref(+)} = 5V$, $V_{ref(-)} = GND$, $t_r = t_f = 20ns$ and $Ta = 25°C$, unless otherwise noted)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Logical "0" Output	V_{OL}	$I_{sink} = 1.6mA$ $V_{CC} = 5V$			0.45	V
Min. Start Pulse Width	T_{ws}	(Figure Timing Diagram)		100	200	ns
Min. Ale Pulse Width	T_{wale}	(Figure Timing Diagram)		100	200	ns
Min. Address Set-Up Time	T_s	(Figure Timing Diagram)		25	50	ns
Min. Address Hold Time	T_h	(Figure Timing Diagram)		25	50	ns
Analog Mux. Delay Time From Ale	T_d	(Figure Timing Diagram)		1	2.5	μs
Output Enable Time	T_{en}	(Figure Timing Diagram) $C_L = 50pF$ $R_L = 10K$		125	250	ns
Output Disable Time	T_{dis}	(Figure Timing Diagram) $C_L = 10pF$ $R_L = 10K$		125	250	ns
Conversion Time	T_{con}	(Figure Timing Diagram)	90	100	116	μs
Clock Rate	F_{clr}		10	640	1280	KHz
Input Capacitance	C_{in}	At control input		10	15	pF
Tri-State Output Capacitance	C_{out}	At digital output		10	15	pF
Analog Multiplexer on Resistance	R_{on}	(Any Selected Channel) $Ta = 25°C$, $R_L = 10K$		1.5	3	KΩ
On Resistance Between Any 2 Channels	$\triangle R_{on}$	(Any Selected Channel) $R_L = 10K$		75		Ω

FUNCTIONAL DESCRIPTION

Multiplexer

The analog multiplexer selects 1 of 16 single-ended input channels as determined by the address decoder. Address latch enable control loads the address code into the decoder on a low to high transition. Table 1 shows the input states for the address line and the expansion control line to select any channel.

TABLE 1

Inputs						Selected Analog Channel
Address					Address Latch Enable	
Exp.	D	C	B	A		
H	L	L	L	L	Low to High	IN0
H	L	L	L	H	Low to High	IN1
H	L	L	H	L	Low to High	IN2
H	L	L	H	H	Low to High	IN3
H	L	H	L	L	Low to High	IN4
H	L	H	L	H	Low to High	IN5
H	L	H	H	L	Low to High	IN6
H	L	H	H	H	Low to High	IN7
H	H	L	L	L	Low to High	IN8
H	H	L	L	H	Low to High	IN9
H	H	L	H	L	Low to High	IN10
H	H	L	H	H	Low to High	IN11
H	H	H	L	L	Low to High	IN12
H	H	H	L	H	Low to High	IN13
H	H	H	H	L	Low to High	IN14
H	H	H	H	H	Low to High	IN15
L	X	X	X	X		All Channels Off

Exp: Expansion Control

X: Don't Care

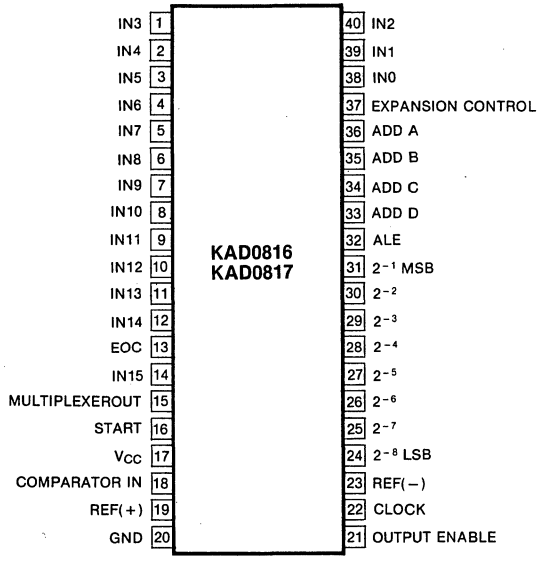
Converter

The converter is designed to give fast, accurate, and repeatable conversions over a wide range of temperatures. The converter is partitioned into three major sections: 256R ladder network, the successive approximation register, and the comparator.

The 256R ladder can confirm its inherent monotonicity and no missing codes. The S.A.R. performs 8 iterations to approximate analog input during 64 clocks. The 8 clocks is required to determine one bit. The S.A.R. is reset on the positive edge of start pulse and conversion is proceed on the falling edge of the start one and it can be interrupted by receipt of a new start pulse. Continuous conversion may be accomplished by tying the EOC (end of conversion) to start.

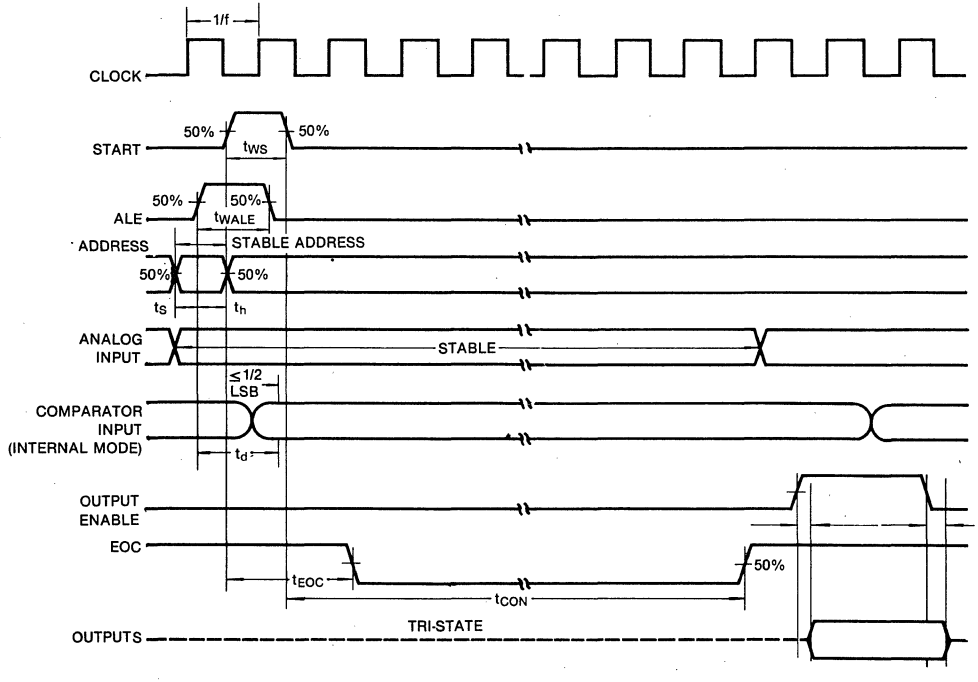
PIN CONFIGURATION

DUAL-IN-PACKAGE



TOP VIEW

TIMING DIAGRAM



TYPICAL PERFORMANCE CHARACTERISTICS

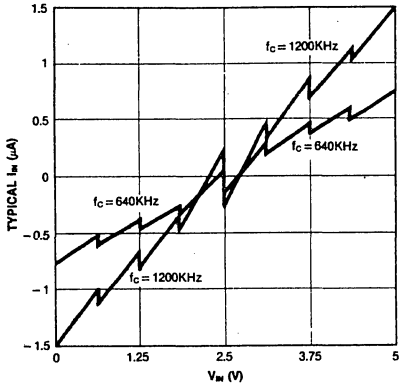


Fig. 1 Comparator I_{IN} vs V_{IN} ($V_{CC} = V_{REF} = 5V$)

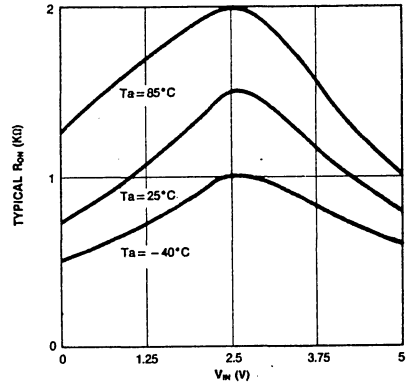


Fig. 2 Multiplexer R_{ON} vs V_{IN} ($V_{CC} = V_{REF} = 5V$)

TRI-STATE TEST CIRCUITS AND TIMING DIAGRAMS

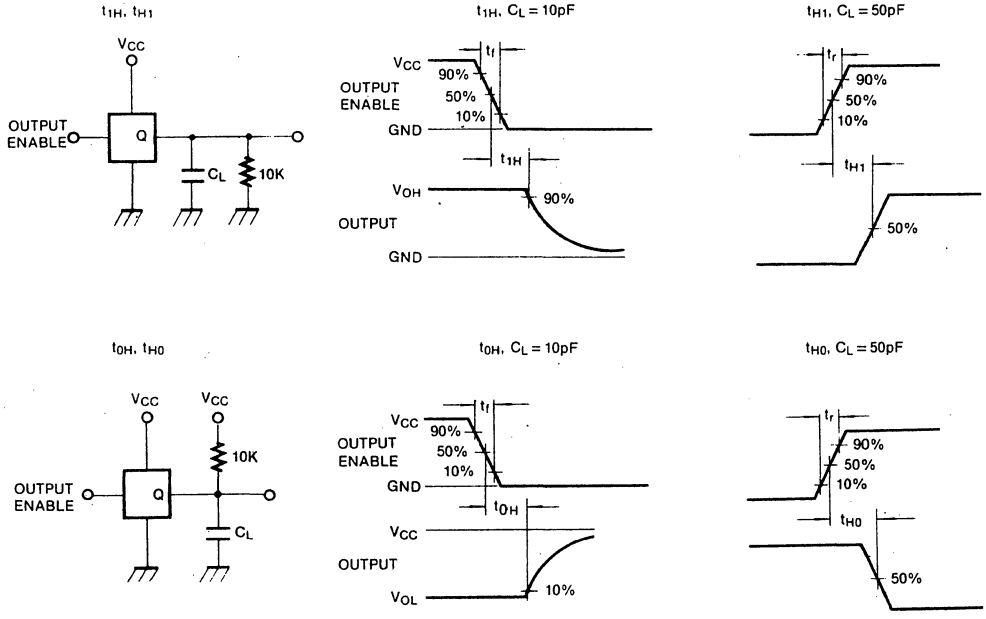


Fig. 3

APPLICATIONS INFORMATION

OPERATION

1.0 Ratiometric Conversion

The KAD0816, KAD0817 is designed as a complete Data Acquisition System (DAS) for ratiometric conversion systems. In ratiometric systems, the physical variable being measured is expressed as a percentage of full-scale which is not necessarily related to an absolute standard. The voltage input to the KAD0816 is expressed by the equation.

$$\frac{V_{IN}}{V_{fs} - V_Z} = \frac{D_X}{D_{max} - D_{min}}$$

V_{IN} = Input voltage into the KAD0816
V_{fs} = Full-scale voltage
V_Z = Zero voltage
D_X = Data point being measured
D_{max} = Maximum data limit
D_{min} = Minimum data limit

A good example of a ratiometric transducer is a potentiometer used as a position sensor. The position of the wiper is directly proportional to the output voltage which is a ratio of the full-scale voltage across it. Since the data is represented as a proportion of full-scale, reference requirements are greatly reduced, eliminating a large source of error and cost for many applications. A major advantage of the KAD0816, KAD0817 is that the input voltage range is equal to the supply range so the transducers can be connected directly across the supply and their outputs connected directly into the multiplexer inputs, (Figure 4).

Ratiometric transducers such as potentiometers, strain gauges, thermistor bridges, pressure transducers, etc., are suitable for measuring proportional relationships; however, many types of measurements must be referred to an absolute standard such as voltage or current. This means a system reference must be used which relates the full-scale voltage to the standard volt. For example, if $V_{CC} = V_{REF} = 5.12V$, then the full-scale range is divided into 256 standard steps. The smallest standard step is 1 LSB which is then 20mV.

2.0 Resistor Ladder Limitations

The voltages from the resistor ladder are compared to the selected input 8 times in a conversion. These voltages are coupled to the comparator via an analog switch tree which is referenced to the supply. The voltages at the top, center and bottom of the ladder must be controlled to maintain proper operation.

The top of the ladder, REF(+), should not be more positive than the supply, and the bottom of the ladder, REF(−), should not be more negative than ground, the center of the ladder voltage must also be near the center of the supply because the analog switch tree changes from N-channel switches to P-channel switches. These limitations are automatically satisfied in ratiometric systems and can be easily met in-ground referenced systems.

The KAD0816 needs less than a milliamp of supply current so developing the supply from the reference is readily accomplished. In figure 6 a ground references system is shown which generates the supply from the reference. The buffer shown can be an OP Amp of sufficient drive to supply the milliamp of supply current and the desired bus drive, or if a capacitive bus is driven by the outputs a large capacitor will supply the transient supply current as seen in figure 7. The KA301 is overcompensated to insure stability when loaded by the 10μF output capacitor.

The top and bottom ladder voltages cannot exceed V_{CC} and ground, respectively, but they can be symmetrically less than V_{CC} and greater than ground. The center of the ladder voltage should always be near the center of the supply, (i.e., size of the LSB steps) by using a symmetrical reference system. In figure 8, A 2.5V reference is symmetrically cantered about $V_{CC}/2$ since the same current allows the LSB to be half the size of the LSB in a 5V reference system.

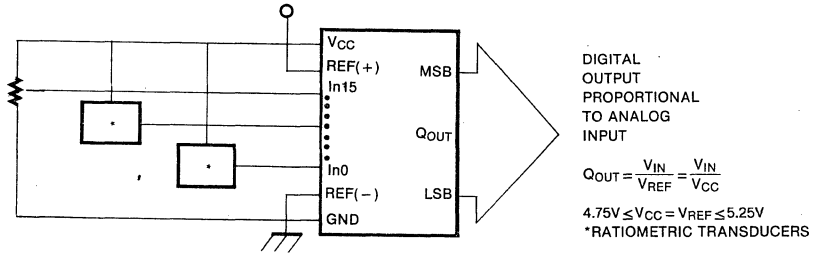


Fig. 4 Ratiometric Conversion System

APPLICATIONS INFORMATION (Continued)

The KAD0816 needs less than a milliamp of supply current so developing the supply from the reference is readily accomplished. In Figure 6 a ground references system is shown which generates the supply from the reference. The buffer shown can be an op amp of sufficient drive to supply the milliamp of supply current and the desired bus drive, or if a capacitive bus is driven by the outputs a large capacitor will supply the transient supply current as seen in Figure 7. The KA301 is overcompensated to insure stability when loaded by the 10μF output capacitor.

The top and bottom ladder voltages cannot exceed V_{CC} and ground, respectively, but they can be symmetrically less than V_{CC} and greater than ground. The center of the ladder voltage should always be near the center of the supply. Sensitivity of the converter can be increased, (i.e., size of the LSB steps decreased) by using a symmetrical reference system. In Figure 8, a 2.5V reference is symmetrically centered about $V_{CC}/2$ since the same current flows in identical resistors. This system with a 2.5V reference allows the LSB bit to be half the size of a 5V reference system.

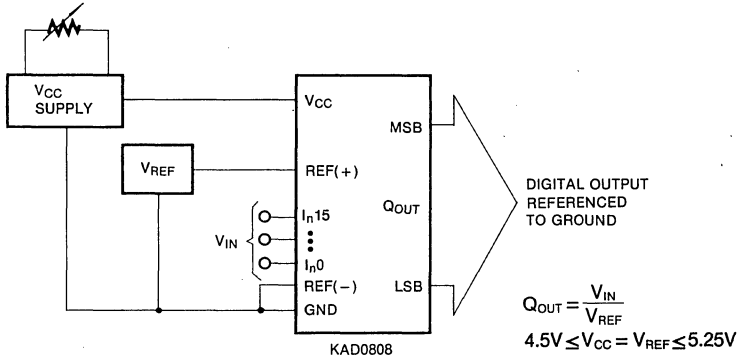


Fig. 5 Ground Referenced Conversion System Using Trimmed Supply

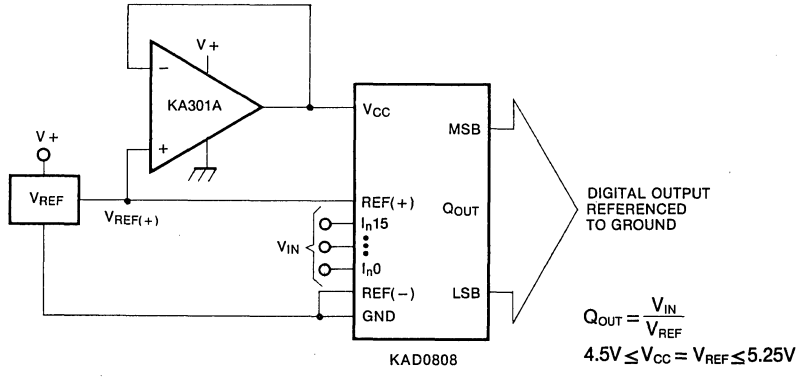


Fig. 6 Ground Referenced Conversion System with Reference Generating V_{CC} Supply

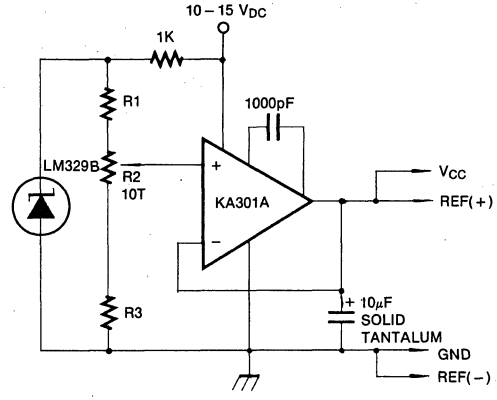


Fig. 7 Typical Reference and Supply Circuit

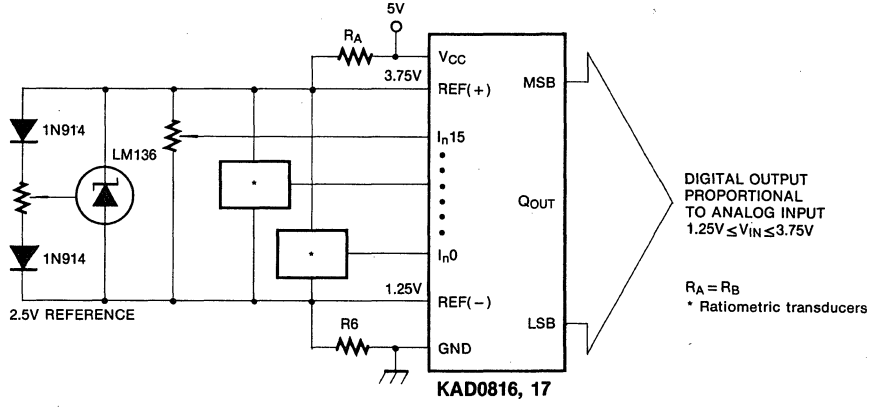


Fig. 8 Symmetrically Centered Reference

TYPICAL APPLICATION

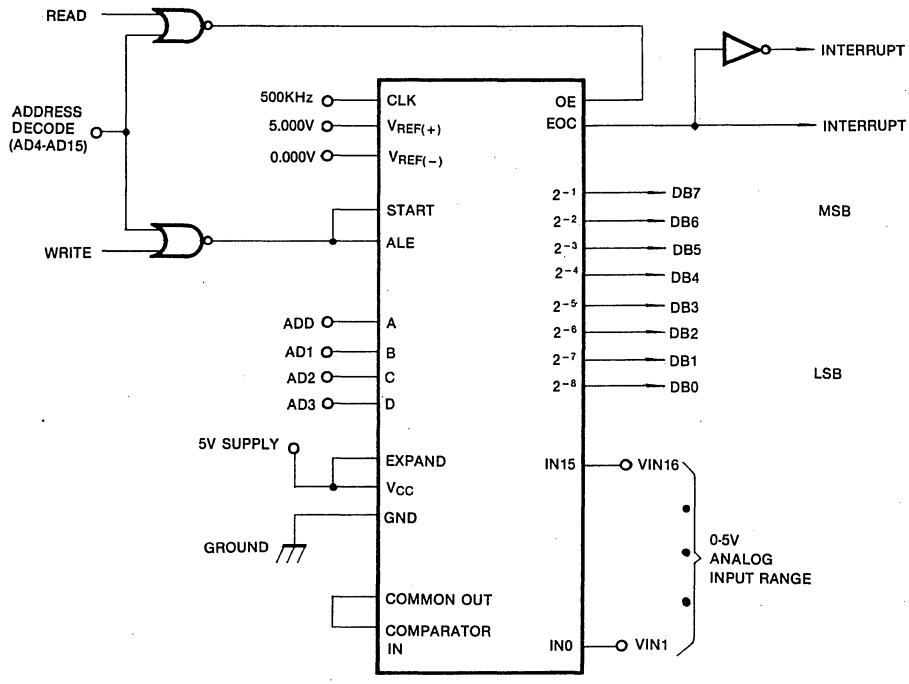


Fig. 9 KAD0816/KAD0817

MICROPROCESSOR INTERFACE TABLE

Processor	$\overline{\text{Read}}$	$\overline{\text{Write}}$	Interrupt (Comment)
8080	$\overline{\text{MEMR}}$	$\overline{\text{MEMW}}$	INTR (Thru RST Circuit)
8085	$\overline{\text{RD}}$	$\overline{\text{WR}}$	INTR (Thru RST Circuit)
Z-80	$\overline{\text{RD}}$	$\overline{\text{WR}}$	$\overline{\text{INT}}$ (Thru RST Circuit, Mode 0)
SC/MP	NRDS	NWDS	SA (Thru Sense A)
6800	VMA, ø 2, R/W	VMA, Q2, $\overline{\text{R/W}}$	$\overline{\text{IRQA}}$ or $\overline{\text{IRQB}}$ (Thru PIA)

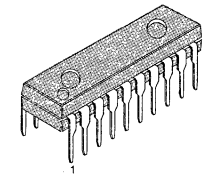
8-BIT HIGH SPEED μP-COMPATIBLE A/D CONVERTER WITH TRACK/HOLD FUNCTION

By using a half-flash conversion technique, the 8-bit KAD0820A/B CMOS A/D offers a 1.5μs conversion time and dissipates only 75mW of power. The half-flash technique consists of 32 comparators, a most significant 4-bit ADC and a least significant 4-bit ADC.

The input to the KAD0820A/B is tracked and held by the input sampling circuitry eliminating the need for an external sample-and-hold for signals moving at less than 100mV/μs.

For ease of interface to microprocessors, the KAD0820A/B has been designed to appear as a memory location or I/O port without the need for external interfacing logic.

20 DIP



FEATURES

- **Built-in track-and-hold function**
- **No missing codes**
- **No external clocking**
- **Single supply $+5V_{DC}$**
- **Easy interface to all microprocessors, or operates stand-alone**
- **Latched TRI-STATE output**
- **Logic inputs and outputs meet both CMOS and TTL voltage level specifications**
- **Operates ratiometrically or with any reference value equal to or less than V_{CC}**
- **0V to 5V analog input voltage range with single 5V supply**
- **No zero or full-scale adjust required**
- **Overflow output available for cascading**
- **0.3″ standard width 20-pin DIP**

ORDERING INFORMATION

Device	Package	Temperature Range	Diff. Nonlinearity
KAD0820AIN	20 DIP	−40°C ~ +85°C	±1/2 LSB
KAD0820BIN			±1 LSB

BLOCK DIAGRAMS

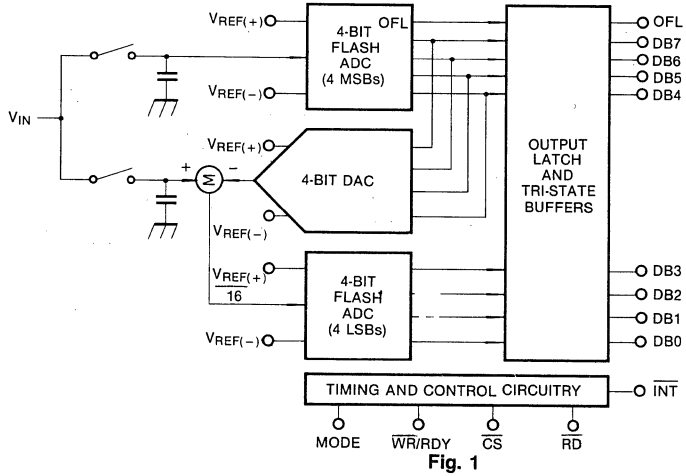


Fig. 1

ABSOLUTE MAXIMUM RATINGS (Note 1 & 2)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	10	V
Package Dissipation at Ta = 25°C	P_D	875	mW
Logic Control Inputs	V_I	−0.2 ~ V_{CC} + 0.2	V
Voltage at Other Inputs and Output	V_I	−0.2 ~ V_{CC} + 0.2	V
Operating Temperature Range	T_{opr}	−40 ~ +85	°C
Storage Temperature Range	T_{stg}	−65 ~ +150	°C

ELECTRICAL CHARACTERISTICS

The following specifications apply for RD mode (pin 7 = 0), V_{CC} = +5V, $V_{REF(+)}$ = +5V, and $V_{REF(-)}$ = GND, Ta = 25°C unless otherwise specified.

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Resolution			—	8	8	Bits
Total Unadjusted Error (Note 3)	INL	KAD0820A KAD0820B	—	±1/2 ±1	±1/2 ±1	LSB LSB
Reference Resistance	R_{REF}		1.4	2.3	5.3	KΩ
Maximum $V_{REF(+)}$ Input Voltage		$V_{REF(+)max}$	—	V_{CC}	V_{CC}	V
Minimum $V_{REF(-)}$ Input Voltage		$V_{REF(-)min}$	—	GND	GND	V
Minimum $V_{REF(+)}$ Input Voltage		$V_{REF(+)min}$	—	$V_{REF(-)}$	$V_{REF(-)}$	V
Maximum $V_{REF(-)}$ Input Voltage		$V_{REF(-)max}$	—	$V_{REF(+)}$	$V_{REF(+)}$	V
V_{IN} Input Voltage	V_{IN}		GND-0.1	—	V_{CC} + 0.1	V
Maximum Analog Input Leakage Current	I_L	$\overline{CS} = V_{CC}$ $V_{IN} = V_{CC}$ V_{IN} = GND	—	0.3 −0.3	3 −3	μA μA
Power Supply Sensitivity	I_S	V_{CC} = 5V ± 5%	—	±1/16	±1/4	LSB

DC ELECTRICAL CHARACTERISTICS

The following specifications apply for $V_{CC}=5V$, $Ta=25°C$ unless otherwise specified.

Characteristic	Symbol	Test Conditions		Min	Typ	Max	Units
Logical "1" Input Voltage	$V_{IN(1)}$	$V_{CC}=5.25V$	$\overline{CS}$, $\overline{WR}$, $\overline{RD}$	2.0	—	V_{CC}	V
			Mode	3.5	—	V_{CC}	V
Logical "0" Input Voltage	$V_{IN(0)}$	$V_{CC}=4.75V$	$\overline{CS}$, $\overline{WR}$, $\overline{RD}$	0	—	0.8	V
			Mode	0	—	1.5	V
Logical "1" Input Current	$I_{IN(1)}$	$V_{IN(1)}=5V$; $\overline{CS}$, $\overline{RD}$		—	0.1	1	μA
		$V_{IN(1)}=5V$; $\overline{WR}$		—	0.1	1	μA
		$V_{IN(1)}=5V$; Mode		—	50	170	μA
Logical "0" Input Current	$V_{IN(0)}$	$V_{IN(0)}=0V$; $\overline{CS}$, $\overline{RD}$, $\overline{WR}$, Mode		—	0.1	1	μA
Logical "1" Output Voltage	$V_{OUT(1)}$	$V_{CC}=4.75V$, $I_{OUT}=-360\mu A$; DB0 – DB7, $\overline{OFL}$, $\overline{INT}$		—	2.4	2.8	V
		$V_{CC}=4.75V$, $I_{OUT}=-10\mu A$; DB0 – DB7, $\overline{OFL}$, $\overline{INT}$		—	4.5	4.6	V
Logical "0" Output Voltage	$V_{OUT(0)}$	$V_{CC}=4.75V$, $I_{OUT}=1.8mA$; DB0 – DB7, $\overline{OFL}$, $\overline{INT}$, RDY		—	0.34	0.4	V
TRI-STATE Output Current	I_{OUT}	$V_{OUT}=5V$; DB0 – DB7, RDY		—	0.1	1	μA
		$V_{OUT}=0V$; DB0 – DB7, RDY		—	−0.1	−1	μA
Output Source Current	I_{SOURCE}	$V_{OUT}=0V$; DB0 – DB7, OFL		−7.2	−12	—	mA
		$\overline{INT}$		−5.3	−9	—	mA
Output Sink Current	I_{SINK}	$V_{OUT}=5V$; DB0 – DB7, OFL, $\overline{INT}$, RDY		8.4	14	—	mA
Supply Current	I_{CC}	$\overline{CS}=\overline{WR}=\overline{RD}=0$		—	7.5	13	mA

AC ELECTRICAL CHARACTERISTICS

The following specifications apply for $V_{CC}=5V$, $t_r=t_f=20ns$, $V_{REF(+)}=5V$, $V_{REF(-)}=GND$ and $Ta=25°C$ unless otherwise specified.

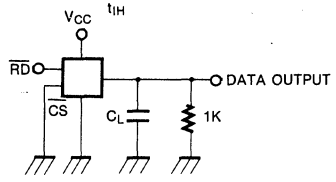
Characteristic		Symbol	Test Conditions	Min	Typ	Max	Unit
Conversion Time for $\overline{RD}$ Mode		t_{CRD}	Pin 7 = 0, (Figure 2)	—	1.6	2.5	μs
Access Time (Delay from Falling Edge of $\overline{RD}$ to Output Valid)		t_{RCCO}	Pin 7 = 0, (Figure 2)	—	$t_{CRD}+20$	$t_{CRD}+50$	ns
Conversion Time for WR-RD Mode		t_{CWR-RD}	Pin 7 = V_{CC}; $t_{WR}=600ns$, $t_{RD}=600ns$; (Figures 3a and 3b)	—	1.52	—	μs
Write Time	Min	t_{WR}	Pin 7 = V_{CC}; (Figures 3a and 3b) (Note 4) See Graph	—	—	600	ns
	Max			—	50	—	μs
Read Time	Min	t_{RD}	Pin 7 = V_{CC}; (Figures 3a and 3b) (Note 4) See Graph	—	—	600	ns

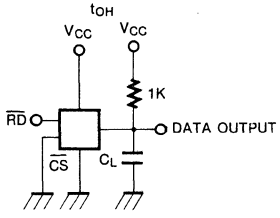
AC ELECTRICAL CHARACTERISTICS (Continued) The following specifications apply for $V_{CC}=5V$, $t_r=t_f=20ns$, $V_{REF(+)}=5V$, $V_{REF(-)}=0V$ and $Ta=25°C$ unless otherwise specified.

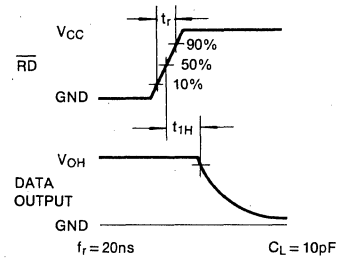
Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Access Time (Delay from Falling Edge of $\overline{RD}$ to Output Valid)	t_{ACC1}	Pin 7 = V_{CC}, $t_{RD}<t_I$; (Figure 3a) $C_L=15pF$	—	190	280	ns
		$C_L=100pF$	—	210	320	ns
Access Time (Delay from Falling Edge of $\overline{RD}$ to Output Valid)	t_{ACC2}	Pin 7 = V_{CC}, $t_{RD}>t_I$; (Figure 3b) $C_L=15pF$	—	70	120	ns
		$C_L=100pF$	—	90	150	ns
Internal Comparison Time	t_I	Pin 7 = V_{CC}; (Figure 3b and 4) $C_L=50pF$	—	800	1300	ns
TRI-STATE Control (Delay from Rising Edge of $\overline{RD}$ to Hi-Z State)	t_{1H}, t_{0H}	$R_L=1K$, $C_L=10pF$	—	100	200	ns
Delay from Rising Edge of $\overline{WR}$ to Falling Edge of $\overline{INT}$	$\overline{t_{INTL}}$	Pin 7 = V_{CC}, $C_L=50pF$ $t_{RD}>t_I$; (Figure 3b) $t_{RD}<t_I$; (Figure 3a)	— —	 $t_{RD}+200$	 t_I $t_{RD}+290$	ns ns ns
Delay from Rising Edge of $\overline{RD}$ to Rising Edge of $\overline{INT}$	$\overline{t_{INTH}}$	(Figure 2, 3a and 3b) $C_L=50pF$	—	125	225	ns
Delay from Rising Edge of $\overline{WR}$ to Rising Edge of $\overline{INT}$	$\overline{t_{INTHWR}}$	(Figure 4), $C_L=50pF$	—	175	270	ns
Delay from $\overline{CS}$ to RDY	t_{RDY}	(Figure 2), $C_L=50pF$, Pin 7 = 0	—	50	100	ns
Delay from $\overline{INT}$ to Output Valid	t_{ID}	(Figure 4)	—	20	50	ns
Delay from $\overline{RD}$ to $\overline{INT}$	t_{RI}	Pin 7 = V_{CC}, $t_{RD}<t_I$ (Figure 3a)	—	200	290	ns
Delay from End of Conversion to Next Conversion	t_P	(Figure 2, 3a, 3b and 4) (Note 4) See Graph	—	—	500	ns
Slew Rate, Tracking			—	0.1	—	V/μs
Analog Input Capacitance	C_{VIN}		—	45	—	pF
Logic Output Capacitance	C_{OUT}		—	5	—	pF
Logic Input Capacitance	C_{IN}		—	5	—	pF

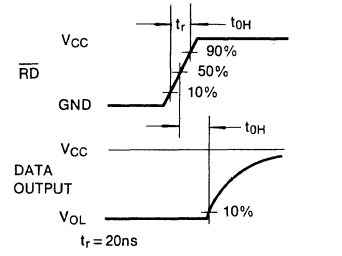
Note 1: Absolute Maximum Ratings are those values beyond which the life of the device may be impaired.
Note 2: All voltages are measured with respect to GND, unless otherwise specified.
Note 3: Total unadjusted error includes offset, full-scale, and linearity errors.
Note 4: Accuracy may degrade if t_{WR} or t_{RD} is shorter than the minimum value specified. See Accuracy vs t_{WR} and Accuracy vs t_{RP} graphs.

TRI-STATE TEST CIRCUITS AND TIMING DIAGRAMS









TIMING DIAGRAMS

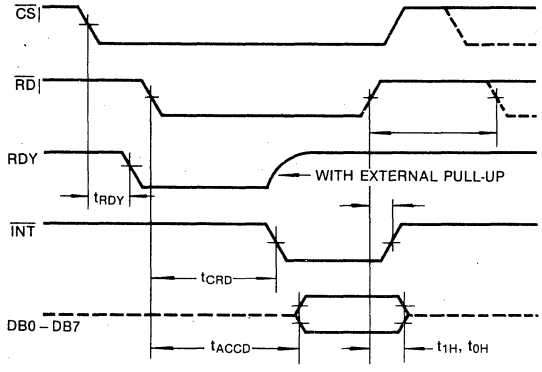


Fig. 2 RD Mode (Pin 7 is Low)

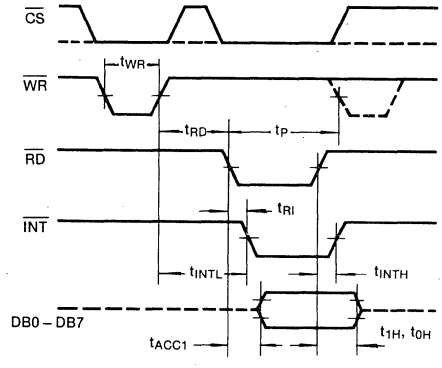


Fig. 3a WR-RD Mode (Pin 7 is High and $t_{RD} < t_I$)

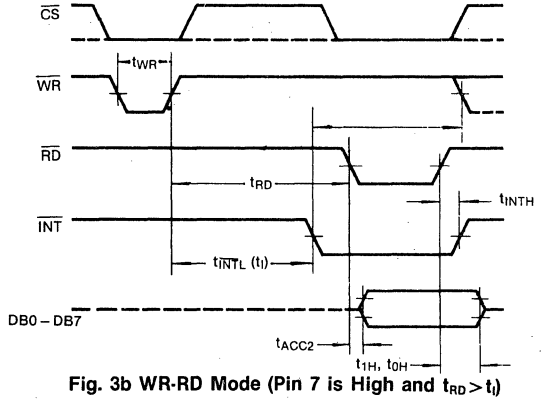


Fig. 3b WR-RD Mode (Pin 7 is High and $t_{RD} > t_I$)

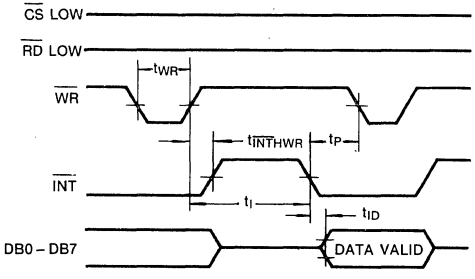
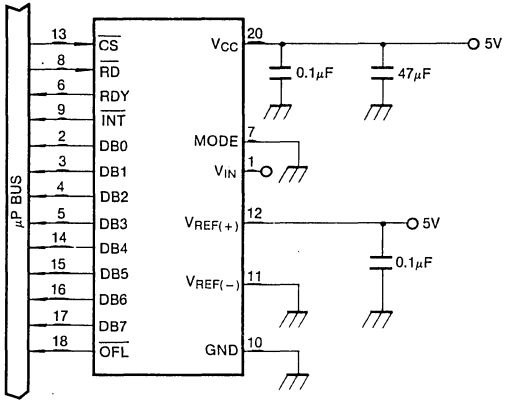
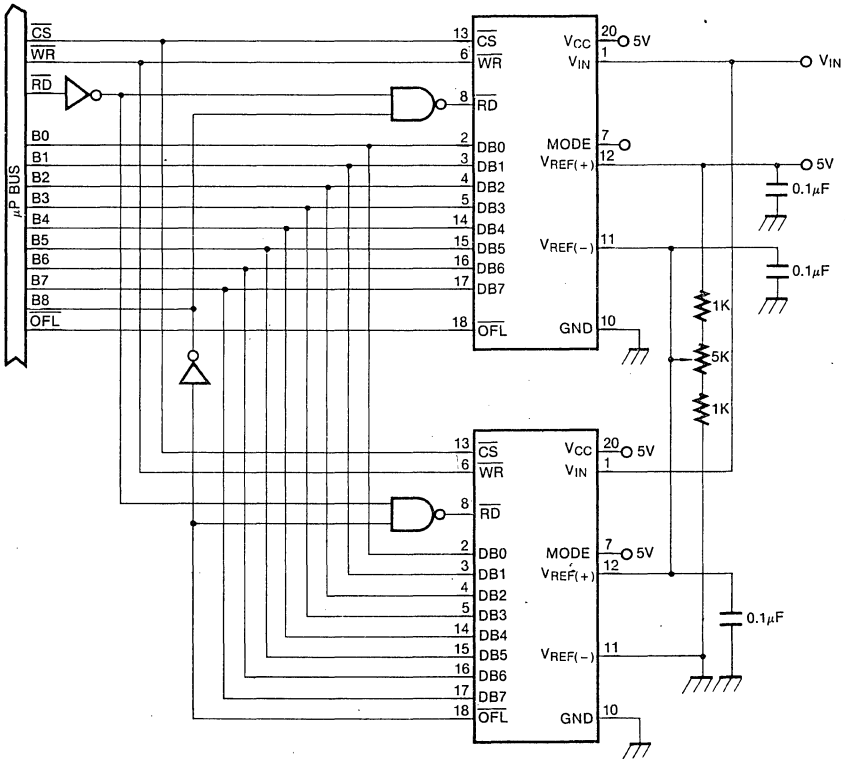


Fig. 4 WR-RD Mode (Pin 7 is High)
Stand-Alone Operation

TYPICAL APPLICATIONS

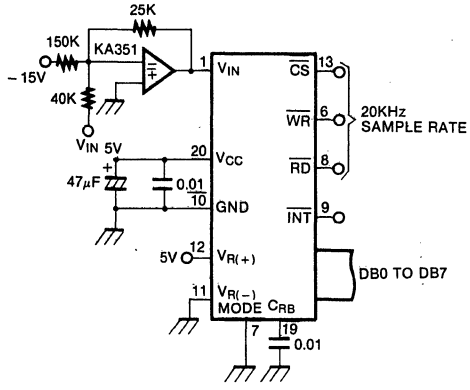


8-Bit Resolution Configuration

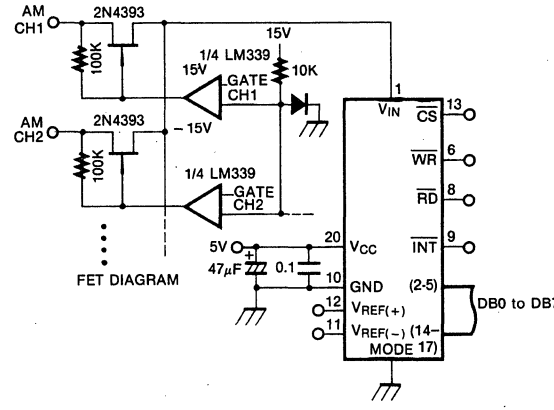


9-Bit Resolution Configuration

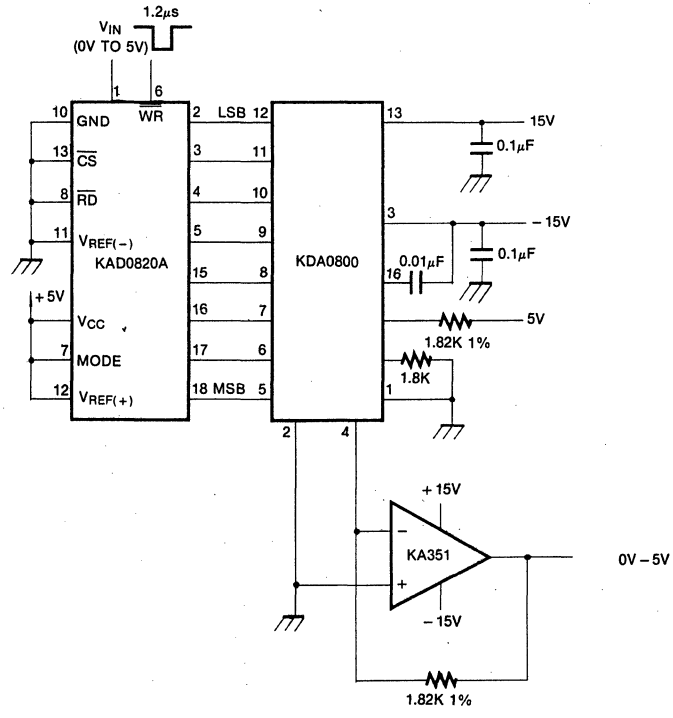
TYPICAL APPLICATIONS (Continued)



Telecom A/D Converter

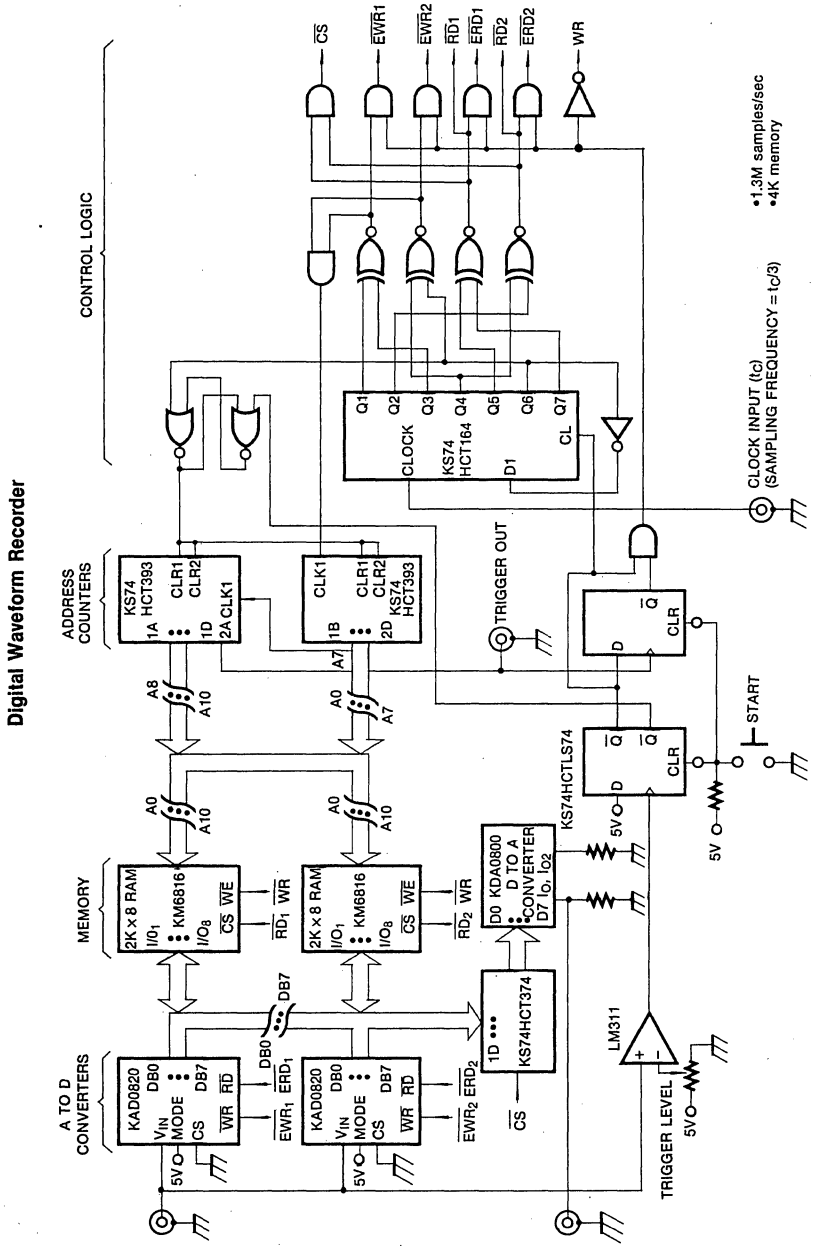


Multiple Input Channels

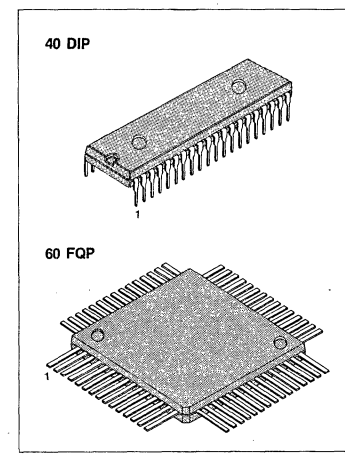


Fast Infinite Sample-and-Hold

TYPICAL APPLICATIONS (Continued)



3 1/2 DIGIT A/D CONVERTER



The single chip CMOS KS7126 incorporates all the active devices for a 3 1/2 digit analog-to-digital converter to directly drive an LCD display. The internal oscillator, voltage reference and display segment/backplane drivers simplify system integration, reduce board space requirements and lower total cost. A low cost, high resolution-0.05%-indicating meter requires only a display, four resistors, four capacitors and 9V battery.

The KS7126 dual slope conversion technique rejects interference signal when the integration time is set to a multiple of the interference signal period. This is especially useful in industrial measurement environments where 50, 60 and 40Hz line frequency signals are present. With an auto-zero error less than 10μV, zero drift less than 1μV/°C, input bias current of 10pA max and rollover error of less than one count, the KS7126 brings exceptional value to the portable battery powered field.

In addition, the differential input and reference allows the measurement on load cells, strain gauges and other bridge type transducers. The low power KS7126 can be used as a plug-in replacement for existing 7106 based systems by changing only the values of seven passive components.

FEATURES

- **Long Battery Life: 800 Hours Typical**
- **Auto-Zero Cycle**
- **Guaranteed Zero Reading With Zero Input**
- **Low Noise: 15μVp-p**
- **High Resolution (0.05%) and Wide Dynamic Range (72dB)**
- **Low Input Leakage Current: 1pA Typical, 10pA Maximum**
- **Direct LCD Display Drive-No External Components**
- **Precision Null Detection With True Polarity at Zero**
- **High Impedance Differential Input**
- **Convenient 9V Battery Operation With Low Power Dissipation: 500μW Typical, 900μW Maximum**
- **Internal Clock Circuit**
- **Drop-In Replacement for TSC7126, ICL7126**

ORDERING INFORMATION

Device	Package	Temperature Range
KS7126CN	40 DIP 60 FQP	0 ~ +70°C

TYPICAL APPLICATIONS

- Thermometry
- Bridge Readouts (Strain Gauges, Load Cells, Null Detectors)
- Digital Meters
  - — Voltage/Current/Ohms/Power
  - — pH
  - — Capacitance/Inductance
  - — Fluid/flow Rate/Viscosity/Level
- Digital Scales
- LVDT Indicators
- Portable Instrumentation
- Power Supply Readouts
- Process Monitors
- Photometers

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	15	V
Analog Input Voltage (Either Input) (1)	V_{IN}	$V_{CC} \sim V_{EE}$	V
Reference Input Voltage (Either Input)	V_{REF}	$V_{CC} \sim V_{EE}$	V
Clock Input	V_{CL}	Test $\sim V_{CC}$	V
Power Dissipation	P_d	800	mW
Lead Temperature (Soldering, 60 Sec)	T_l	300	°C
Operating Temperature	T_{opr}	0 ~ +70	°C
Storage Temperature	T_{stg}	−65 ~ +160	°C

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Test Conditons	Min	Typ	Max	Unit
Zero Input Reading	—	V_{IN} = 0.0V Full scale = 200.0mV	−000.0	+000.0	+000.0	Digital Reading
Zero Rading Drift	—	V_{IN} = 0, 0°C<Ta<70°C		0.2	1	μV/°C
Ratiometric Reading	—	$V_{IN} = V_{REF}$ V_{REF} = 100mV	999	999 1000	1000	Digital Reading
Linearity (Max. deviation from straight line fit)	NL	Full scale = 200mV or full scale = 2,000V	−1	+0.2	+1	Counts
Rollover Error (Difference in reading for equal positive and negative reading near full scale)	—	$-V_{IN} = +V_{IN}$ = 200.0mV	−1	+0.2	+1	Counts
Noise (Pk-Pk value not exceed 95% of time)	E_N	V_{IN} = 0V	—	—	15	μV
Leakage Current @ Input	I_L	V_{IN} = 0V		1	10	pA
Common Mode Rejection Ratio	CMRR	V_{CM} = +1V, V_{IN} = 0V Full scale = 200.0mV	—	50	—	μV/V
Scale Factor Temperature Coefficient	—	V_{IN} = 199.0mV 0<Ta<70°C (Ext. Ref. 0 ppm/°C)	—	1	5	ppm/°C
Temp. Coeff. of Analog Common (with respect to positive supply)	V_{CTL}	250KΩ between common and positive supply	—	80	—	ppm/°C
Analog Common Voltage (with respect to positive supply)	V_C	250KΩ between common and positive supply	2.4	2.8	3.2	V
Pk-Pk Segment Drive Voltage (Note 5)	V_{SO}	V_{CC} to V_{EE} = 9V	4	5	6	V
Pk-Pk Backplane Drive Voltage (Note 5)	V_{BD}	V_{CC} to V_{EE} = 9V	4	5	6	V
Power Supply Current	I_S	V_{IN} = 0V, V_{CC} to V_{EE} = 9V	—	55	100	μA

Notes

1) Input voltage may exceed the supply voltage provided the input current is limited to ± 100μA
2) Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.
3) Unless otherwise noted, specifications apply T_a =25°C, f_{CLOCK} =16KHz and are tested in the circuit of Figure 1.
4) Refer to "Differential Input" discussion on page 7.
5) Backplane drive is in phase with segment drive for 'off' segment, 180 out of phase for 'on' segment. Frequency is 20 times conversion rate. Average DC component is less than 50mV.
6) During auto-zero phase, current is 10 ~ 20μA higher, 48KHz oscillator, Figure 2, increases current by 8μA (Typ.)

TYPICAL OPERATING CIRCUITS

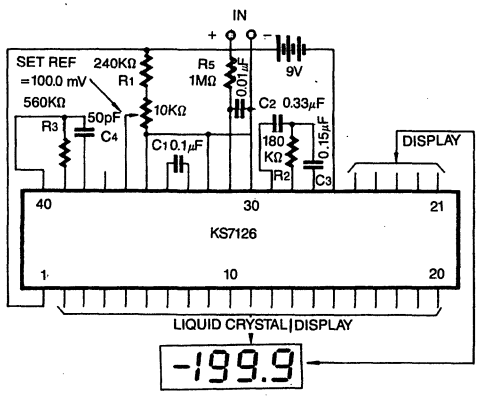


Figure 1: KS7126 Clock Frequency 16 KHz (1 reading/sec.)

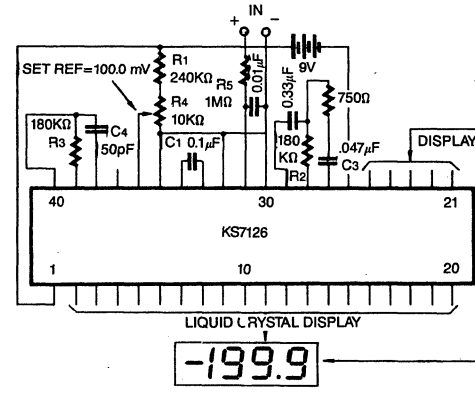
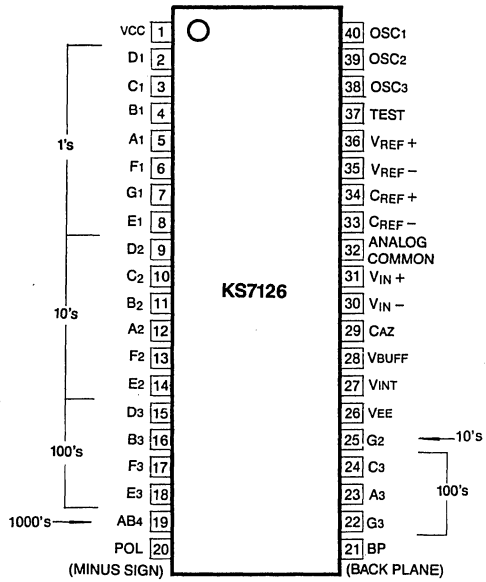
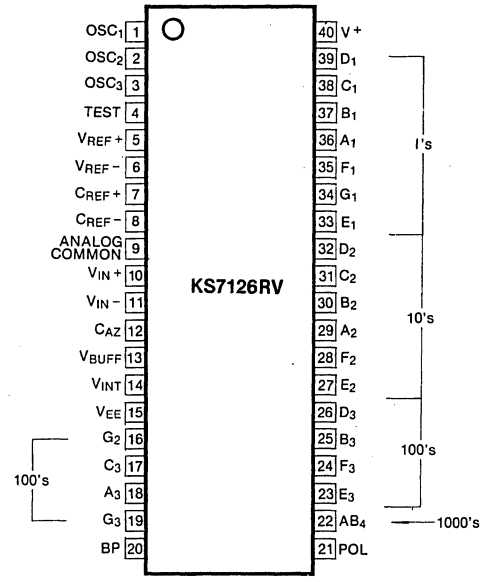


Figure 2: KS7126 Clock Frequency 48 KHz (3 readings/sec.)

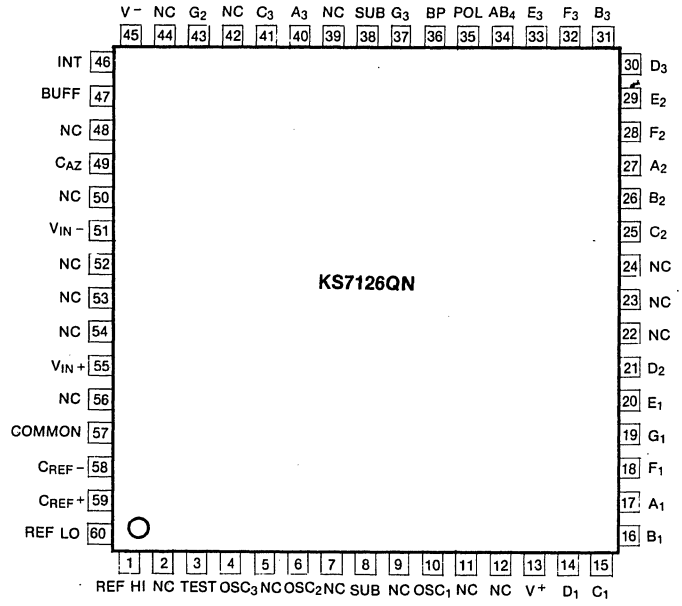
PIN CONFIGURATION



NORMAL TYPE



REVERSE TYPE



FLAT TYPE

PIN DESCRIPTION

40-Pin DIP Pin Number Normal (Reverse)	60-Pin Flat Package Pin Number	Name	Description
1 (40)	13	V^+	Positive power supply
2 (39)	14	D_1	Activates the D section of the units display
3 (38)	15	C_1	Activates the C section of the units display
4 (37)	16	B_1	Activates the B section of the units display
5 (36)	17	A_1	Activates the A section of the units display
6 (35)	18	F_1	Activates the F section of the units display
7 (34)	19	G_1	Activates the G section of the units display
8 (33)	20	E_1	Activates the E section of the units display
9 (32)	21	D_2	Activates the D section of the tens display
10 (31)	25	C_2	Activates the C section of the tens display
11 (30)	26	B_2	Activates the B section of the tens display
12 (29)	27	A_2	Activates the A section of the tens display
13 (28)	28	F_2	Activates the F section of the tens display
14 (27)	29	E_2	Activates the E section of the tens display
15 (26)	30	D_3	Activates the D section of the hundreds display
16 (25)	31	B_3	Activates the B section of the hundreds display
17 (24)	32	F_3	Activates the F section of the hundreds display
18 (23)	33	E_3	Activates the E section of the hundreds display
19 (22)	34	AB_4	Activates both halves of the 1 in the thousands display
20 (21)	35	POL	Activates the negative polarity display
21 (20)	36	BP	Backplane drive output
22 (19)	37	G_3	Activates the G section of the hundreds display
23 (18)	40	A_3	Activates the A section of the hundreds display
24 (17)	41	C_3	Activates the C section of the hundreds display
25 (16)	43	G_2	Activates the E section of the tens display
26 (15)	45	V^-	Negative power supply voltage
27 (14)	46	V_{INT}	The integrating capacitor should be selected to give the maximum voltage swing that ensures component tolerance build up will not allow the integrator output to saturate. When analog common is used as a reference and the conversion rate is 3 reading per second, a 0.047μF capacitor may be used. The capacitor must have a low dielectric constant to prevent roll-over errors.

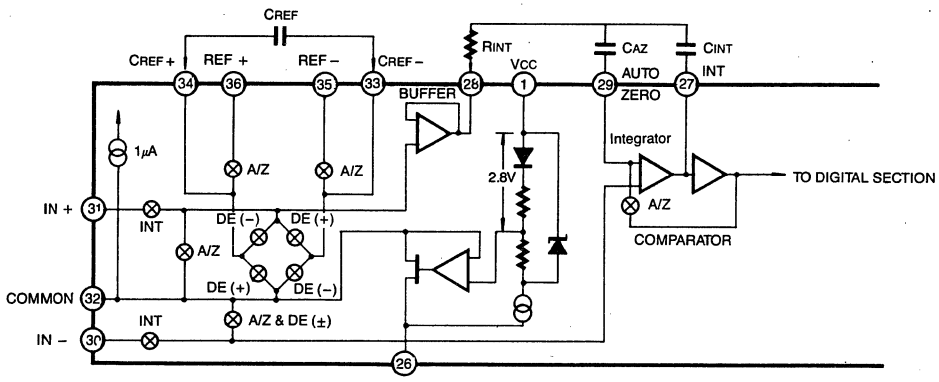
PIN DESCRIPTION (Continued)

40-Pin DIP Pin Number Normal (Reverse)	60-Pin Flat Package Pin Number	Name	Description
28 (13)	47	V_{BUFF}	Integration resistor connection. Use a 180KΩ for a 200mV full-scale range and a 1.8MΩ for 2V full-scale range.
29 (12)	49	C_{AZ}	The size of the auto-zero capacitor influences the system noise. Use a 0.33μF capacitor for a 200mV full-scale, and a 0.033μF capacitor for a 2V full-scale.
30 (11)	51	V_{IN-}	The low input is connected to this pin.
31 (10)	55	V_{IN+}	The high input signal is connected to this pin.
32 (9)	57	ANALOG COMMON	This pin is primarily used to set the analog common-mode voltage for battery operation or in systems where the input signal is referenced to the power supply. See paragraph on ANALOG COMMON for more details. It also acts as a reference voltage source.
33 (8)	58	C_{REF}	See pin 34
34 (7)	59	C_{REF+}	A 0.1μF capacitor is used in most applications. If a large common mode voltage exists (for example the V_{IN} pin is not at analog common), and a 200mV scale is used, a 1.0μF is recommended and will hold the rollover error to 0.5 count.
35 (6)	60	V_{REF-}	See pin 36.
36 (5)	1	V_{REF+}	The analog input required to generate a full-scale output (1,999 counts). Place 100mV between pins 35 and 36 for 199.9mV full-scale. Place 1.000volt between pins 35 and 36 for 2V full-scale. See paragraph on REFERENCE VOLTAGE.
37 (4)	3	TEST	Lamp test. When pulled high (to V_{CC}) all segments will be turned ON and the display should read-1888. It may also be used as a negative supply for externally generated decimal points. See paragraph under TEST for additional information.
38 (3)	4	OSC_3	See pin 40.
39 (2)	6	OSC_2	See pin 40.
40 (1)	10	OSC_1	Pin 40, 39, 38 make up the oscillator section. For a 48KHz clock (3 readings per second) connect pin 40 to the junction of a 180KΩ resistor an a 50pF capacitor. The 180KΩ resistor is tied to pin 39 and the 50pF capacitor is tied to pin 38.

DETAILED DESCRIPTION

ANALOG SECTION

Fig. 3 shows the Block Diagram of the Analog Section for the KS7126. Each measurement cycle is divided into three phases. They are (1) Auto-zero (A-Z), (2) Signal integrate (INT) and (3) De-Integrate (DE).



Flg. 3 Analog Section of KS7126

1. Auto-zero phase

During auto-zero three things happen. First, input high and low are disconnected from the pins and internally shorted to analog COMMON. Second, the reference capacitor is charged to the reference voltage. Third, a feedback loop is closed around the system to charge the auto-zero capacitor C_{AZ} to compensate for offset voltages in the buffer amplifier, integrator, and comparator. Since the comparator is included in the loop, the A-Z accuracy is limited only by the noise of the system. In any case, the offset referred to the input is less than 10μV.

2. Signal integrate phase

During signal integrate, the auto-zero loop is opened, the internal short is removed, and the internal input high and low are connected to the external pins. The converter then integrates the differential voltage between IN+ and IN– for a fixed time. This differential voltage can be within a wide common mode range; within one Volt of either supply. If, on the other hand, the input signal has no return with respect to the converter power supply, IN– can be tied to analog COMMON to establish the correct common mode voltage. At the end of this phase, the polarity of the integrated signal is determined.

3. De-integrate phase

The final phase is de-integrate, or reference integrate. Input low is internally connected to analog COMMON and input high is connected across the previously charged reference capacitor. Circuitry within the chip ensures that the capacitor will be connected with the correct polarity to cause the integrator output to return to zero. The time required for the output to return to zero is proportional to the input signal. Specifically the digital reading displayed is $1000(\frac{V_{IN}}{V_{REF}})$

Differential Input

The input can accept differential voltages anywhere within the common mode range of the input amplifier; or specifically from 0.5 Volts below the positive supply to 1.0 Volt above the negative supply. In this range the system has a CMRR of 86dB typical. However, since the integrator also swings with the common mode voltage, care must be exercised to assure the integrator output does not saturate. A worst case condition would be a large positive common-mode voltage with a near full-scale negative differential input voltage. The negative input signal drives the integrator positive when most of its swing has been used up by the positive common mode voltage. For these critical applications the integrator swing can be reduced to less than the recommended 2V full scale swing with little loss of accuracy. The integrator output can swing within 0.3 Volts of either supply without loss of linearity.

Differential Reference

The reference voltage can be generated anywhere within the power supply voltage of the converter. The main source of common mode error is a roll-over voltage caused by the reference capacitor losing or gaining charge to stray capacity on its modes. If there is a large common mode voltage, the reference capacitor can gain charge (increase voltage) when called up to de-integrate a positive signal but lose charge (decrease voltage) when called up to de-integrate a negative input signal. This difference in reference for (+) or (−) input voltage will give a roll-over error However, by selecting the reference capacitor large enough in comparision to the stray capacitance, this error can be held to less than 0.5 count for the worst case condition (See component Value Section)

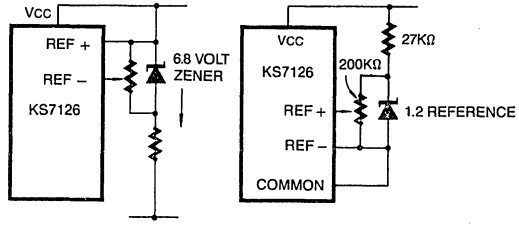


Fig. 4: Using an External Reference

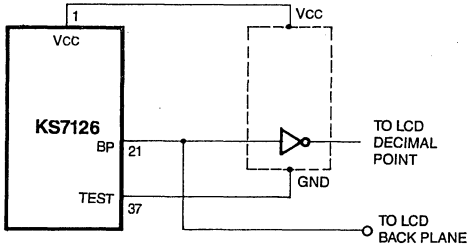


Figure 5: Simple Inverter for Fixed Decimal Point

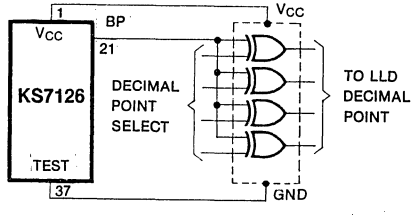


Figure 6: Exclusive-OR Gate for Decimal Point

Analog Common

This pin is included primarily to set the common mode voltage for battery operation or for any system where the input signals are floating with respect to the power supply. The COMMON pin sets a voltage that is approximately 2.8 Volts more negative than the positive supply. This is selected to give a minimum end-of-life battery voltage of about 6V. However, the analog COMMON has some of the attributes of a reference voltage. When the total supply voltage is large enough to cause the zener to regulate (<7V), the COMMON voltage will have a low voltage coefficient (0.001%/%), low output impedance (≅15Ω), and a temperature coefficient typically less than 80 ppm/°C.

The limitations of the on-chip reference should be also recognized, however. The reference temperature coefficient (TC) can cause some degradation in performance. Temperature changes of 2 to 8°C, typical for instruments, can give a scale factor error of a count or more. Also the common voltage will have a poor voltage coefficient when the total supply voltage is less than that which will cause the zener to regulate (<7V). These problems are eliminated if an external reference is used, as shown in Fig. 4.

Analog COMMON is also used as the input low return during auto-zero and de-integrate. If IN− is different from analog COMMON, a common mode voltage exists in the system and is taken care of by the excellent CMRR of the converter. However, in some applications IN− will be set at a fixed known voltage (power supply common for instance). In this application, analog COMMON should be tied to the same point, thus removing the common mode voltage from the converter. The same holds true for the reference voltage. If reference can be conveniently referenced to analog COMMON, it should be since this removes the common mode voltage from the reference system.

Within the IC, analog COMMON is tied to an N channel FET that can sink 100μA or more of current to hold the voltage 2.8 volts below the positive supply (when a load is trying to pull the common line positive). However, there is only 1μA of source current, so COMMON may easily be tied to a more negative voltage thus overriding the internal reference.

Test

The TEST pin serves two functions. It is coupled to the internally generated digital supply through a 500Ω resistor. Thus it can be used as the negative supply for externally generated segment drivers such as decimal points or any other presentation the user may want to include on the LCD display Fig. 5 and Fig. 6 show such an application. No more than a 1mA load should be applied.

The second function is a "lamp test". When TEST is pulled high (to V_{CC}) all segments will be turned on and the display should read — 1888. The TEST pin will sink about 10mA under these conditions.

CAUTION: In the lamp test mode, the segments have a constant D-C voltage (no square wave) and may burn the LCD display if left in this mode for extended periods.

DIGITAL SECTION

Fig. 7 shows the digital section for the KS7126. An internal digital ground is generated from a 6 volt zener diode and a large P channel source follower. This supply is made stiff to absorb the relative large capacitive current when the back plane (BP) voltage is switched. The BP frequency is the clock frequency divided by 800. For three readings/second this is a 60Hz square wave with a nominal amplitude of 5 volts. The segments are driven at the same frequency and amplitude and are in phase with BP when OFF, but out of phase when ON. In all cases negligible DC voltage exists across the segments. The polarity indication is "ON" for negative analog inputs. If IN− and IN+ are reversed, this indication can be reversed also, if desired.

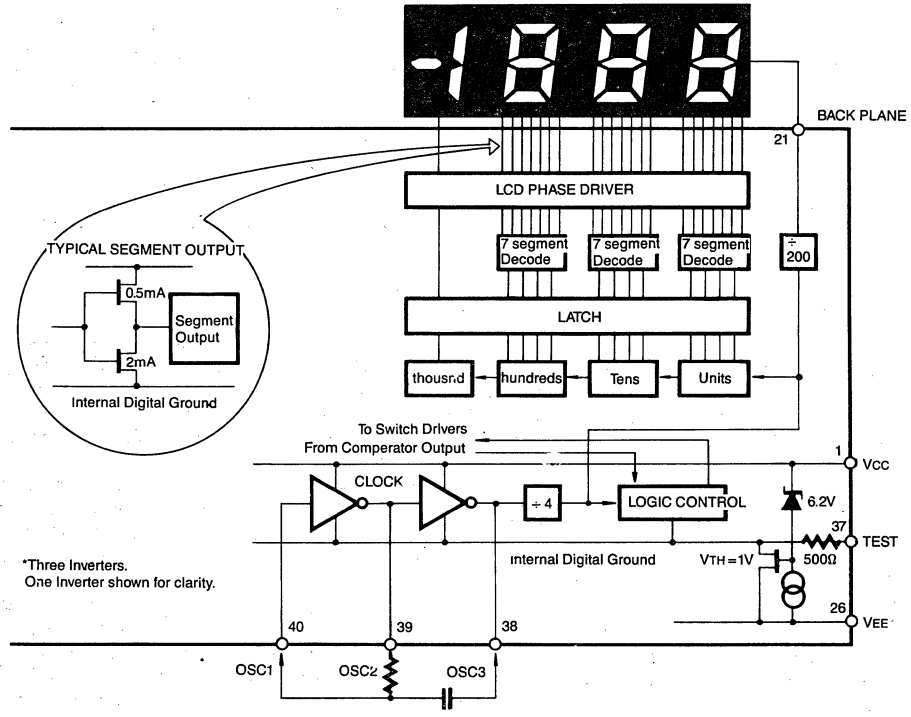


Fig. 7: Digital Section

System Timing

Fig. 8 shows the clocking arrangement used in the KS7126. Three basic clocking arrangements can be used.

1. An external oscillator connected to pin 40
2. A crystal between pins 39 and 40.
3. An R-C oscillator using all three pins

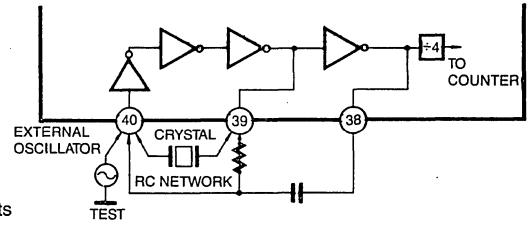


Fig. 8: Clock Circuits

The oscillator frequency is divided by four before it clocks the decade counts. It is then futher divided to form the three convert — cycle phases. These are signal integrate (1000 counts), reference de-integrate (0 to 2000 counts) and auto — zero (1000 to 3000 counts). For signals less than full scale, auto — zero gets the unused portion of reference de-integrate. This makes a complete measure cycle of 4,000 (1,600 clock pulses) independent of input voltage. For three readings/second, an oscillator frequency of 48 KHz would be used.

To achieve maximum rejection of 60Hz pickup, the signal integrate cycle should be a multiple of 60Hz. Oscillator frequency of 60KHz, 48KHz, 33⅓KHz, etc. should be selected. For 50Hz rejection, oscillator frequencies of 66⅔KHz, 50KHz, 40KHz, etc. would be suitable. Note that 40KHz (2.5 readings/second) will reject both 50 and 60Hz (also 400 and 440Hz)

COMPONENT VALUE SELECTION

1. Integrating Resistor

Both the buffer amplifier and the integrator have a class A output stage with 6 μA of quiescent current. They can supply ~1μA of drive current with negligible non-linearity. The integrating resistor should be large enough to remain in this very linear region over the input voltage range, but small enough that undue leakage requirements are not placed on the PC board. For 2 Volt full scale, 1.8MΩ is near optimum and similarly 180KΩ for a 200.0mV scale.

2. Integrating Capacitor

The integrating capacitor should be selected to give the maximum voltage swing that ensures tolerance build-up will not saturate the integral swing (approx. 0.3 Volt from either supply). When the analog COMMON is used as a reference, a nominal ±2 Volt full scale integrator swing is fine.For three readings/second (48KHz clock) nominal values for C_{INT} are 0.047μF, for 1/sec (16KHz) 0.15μF of course, it different oscillator frequencies are used, these values should be changed in inverse proportion to maintain the same output swing.

The integrating capacitor should have low dielectric absorption to prevent roll-over errors. While other types may be adequate for this application, polypropylene capacitors give undetectable errors at reasonable cost. At three readings/sec., a 750Ω resistor should be placed in series with the integrating capacitor, to compensate for comparator delay.

3. Auto-Zero Capacitor

The size of the auto-zero capacitor has some influence on the noise of the system. For 200mV full scale where noise is very important, a 0.32μF capacitor is recommended. On the 2 Volt scale, a 0.033μF capacitor increases the speed of recovery from overload and is adequate for noise on this scale.

4. Reference Capacitor

A 0.1μF capacitor gives good results in most applications. However, where a large common mode voltage exists (i.e. the REF− pin is not analog COMMON) and a 200mV scale is used, a large value is required to prevent roll-over error. Generally 1.0μF will hold the roll-over error to 0.5 count in this instance.

5. Oscillator Components

For all ranges of frequency a 50pF capacitor is recommended and the resistor is selected from the approximate equation $f \approx \frac{0.45}{RC}$ For 48KHz clock (3 readings/second) R=18KΩ

TYPICAL APPLICATIONS

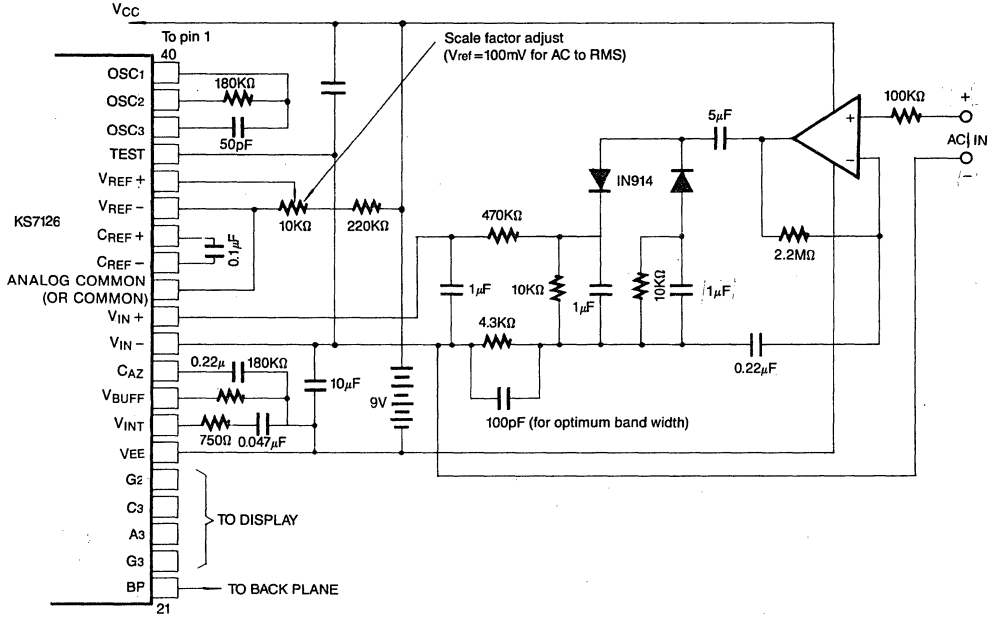


Figure 9: AC to DC Converter with KS7126. Test is Used as a Common Mode Reference Level to Ensure Compatibility with Most Op-Amps.

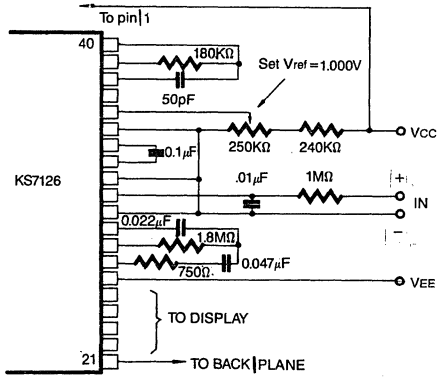


Figure 10: Recommended Values for 2.000V Full-Scale, Three Readings Per Second.

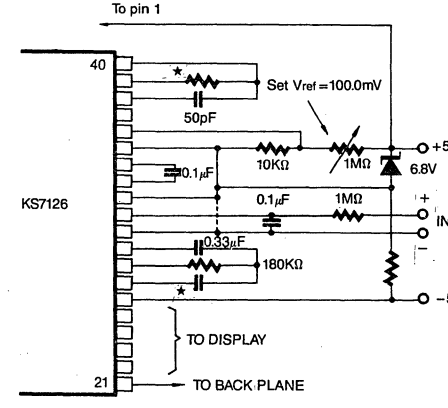


Figure 11: KS7126 with Zener Diode Reference.

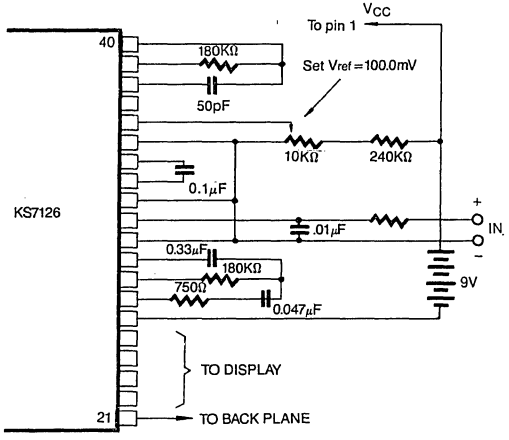


Figure 12: KS7126 Using the Internal Reference. 200.0mV Full-Scale, Three Readings Per Second, Floating Supply Voltage (9V Battery).

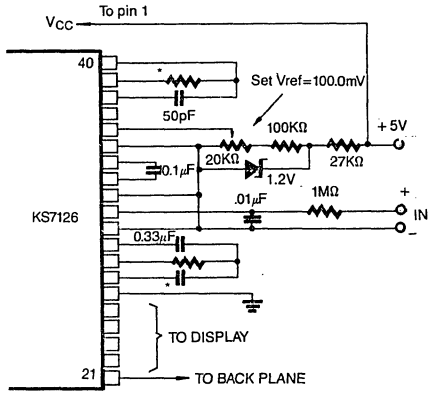
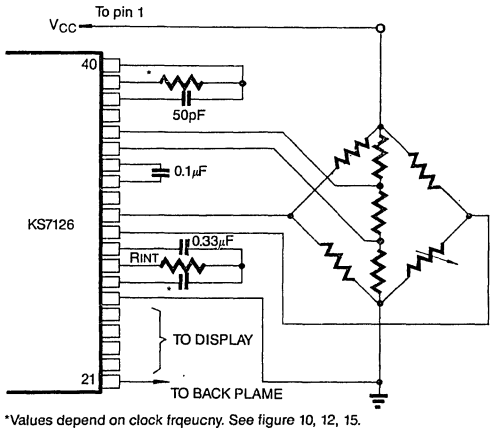


Figure 13: KS7126 Operated From Single +5V Supply. An External Reference Must Be Used.



*Values depend on clock frqeucny. See figure 10, 12, 15.

Figure 14: KS7126 Measuring Ratiometric Values of Quad Load Cell. The Resistor Values Within theBridge are Determined by the Desired Sensitivity.

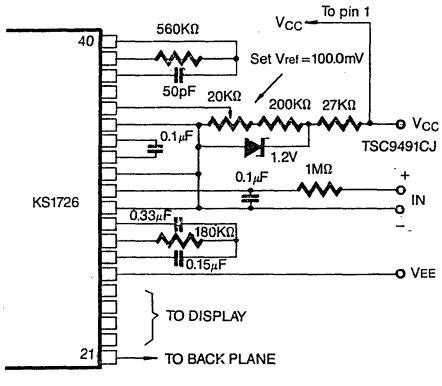


Figure 15: KS7126 with an External Band-Gap Reference (1.2V Typ) IN– is tied to Common. Values Shown are for One Reading Per Second.

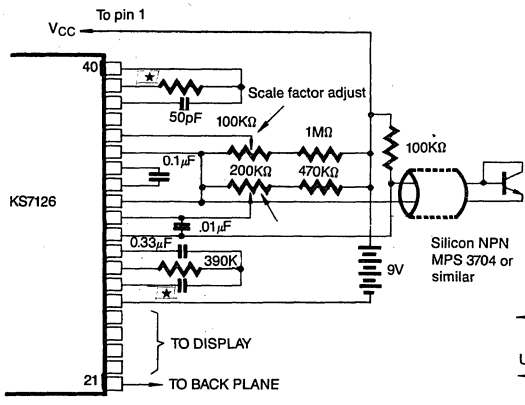


Figure 16: KS7126 Used as a Digital Centigrade Thermometer. A Silicon Diode-Connected Transistor Has a Temperature Coefficient of About 2mV/°C.

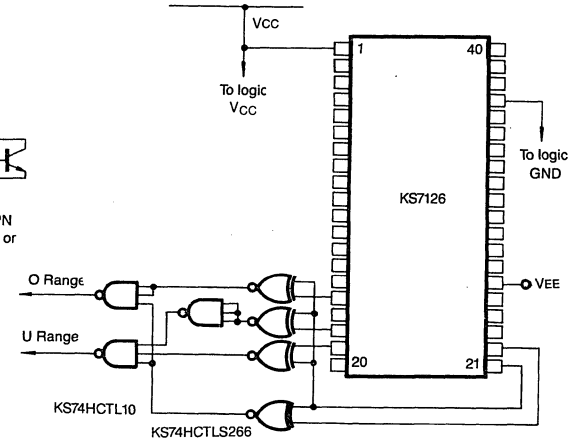


Figure 17: Circuit for Developing Underrange and Overrange Signals from KS7126 Outputs.

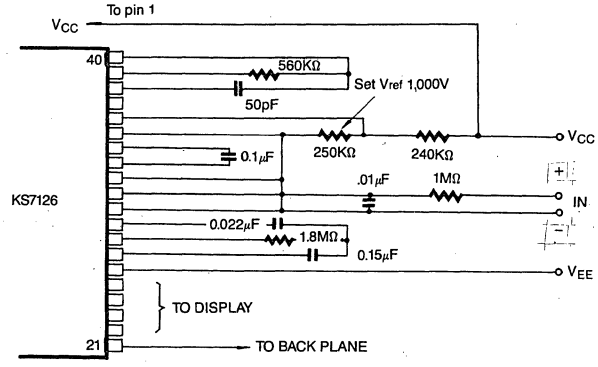


Figure 18: Recommended Component Values for 2.00V Full-Scale, One Reading Per Second.

★Values depend on clock frequency. See Figure 10, 12,15

D/A CONVERTER

4

1. KDA3310
2. KDA0406
3. KDA0800/08
4. KS25C02/03/04

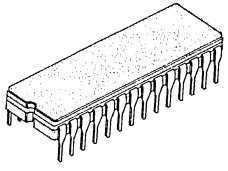
HIGH SPEED D/A CONVERTER 10 BIT 25 MSPS

The KDA3310 is a bipolar monolithic digital-to-analog converter, which has single +5V supply and all the digital input stage is operated at the level of TTL or CMOS LOGIC and CML internally, with a conversion rate of 25MSPS.

The device has a built in input data register and operates without an external deglitcher. A digital data is first sync into a clock signal and then converted into an analog signal.

Moreover video controls, sync and blank, are included for an easy video signal output in RS343A standard ratio form. The dynamic range of analog output is 1.0V and the full-scaled output can be modulated by the size of base voltage entering the pin 6.

28 CERDIP



FEATURE

- **Single +5V supply**
- **8, 9, 10 bit linearity**
- **TTL interface**
- **25 MSPS conversion rate**
- **Voltage output**
- **Low glitch energy**

ORDERING INFORMATION

Marking	INL	DNL
KDA3310-10	±1 LSB	±1/2 LSB
KDA3310-9	±1 LSB	±1 LSB
KDA3310-8	±2 LSB	±2 LSB

BLOCK DIAGRAM

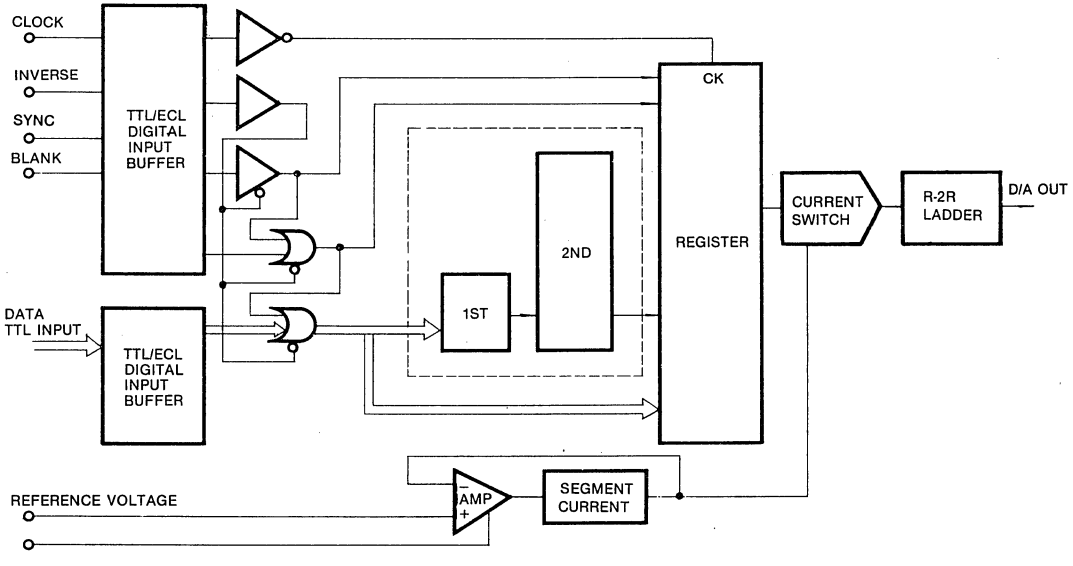


Fig. 1

PIN DESCRIPTION

Pin No.	Description
1	No Connection
2	No Connection
3	Blank Signal Input
4	Sync Signal Input
5	Inverse Signal Input
6	Reference Voltage Input
7	OP Amp. Compensation Capacitor
8	Analog Output
9	Analog Ground
10	Analog Supply + 5V
11	No Connection
12	Substrate Ground
13	No Connection
14	No Connection
15	Digital Ground
16	No Connection
17	Digital Supply + 5V
18	Clock Input
19	Digital Input Bit 0 (MSB)
20	Digital Input Bit 1
21	Digital Input Bit 2
22	Digital Input Bit 3
23	Digital Input Bit 4
24	Digital Input Bit 5
25	Digital Input Bit 6
26	Digital Input Bit 7
27	Digital Input Bit 8
28	Digital Input Bit 9 (LSB)

RECOMMENDED OPERATING CIRCUIT

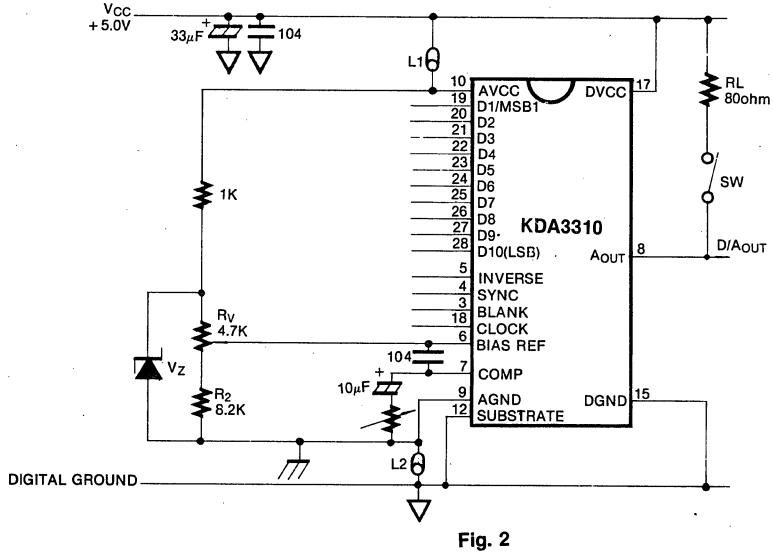


Fig. 2

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Characteristics	Symbol	Value	Unit
Digital Supply Voltage	DV_{CC}	−0.5 to +6.0	V
Analog Supply Voltage	AV_{CC}	−0.5 to +6.0	V
Digital Input Voltage	V_{IN}	−0.5 to +6.0	V
Reference Voltage Input	V_{REF}	2.5 to 5.5	V
Clock Input Voltage	V_{CK}	−0.5 to 6.0	V
Output Compliance Voltage	V_{OC}	3.0 to 6.0	V
Ambient Operating Temp.	T_A	−25.0 to 85.0	°C
Storage Temperature	T_{STG}	−55.0 to +125.0	°C
Soldering Temperature (5 sec)	T_{SOL}	260	°C

Notes: 1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions.
2. Functional operation under any of these conditions is not implied.
3. Applied voltage must be current limited to specified range.
4. Current is specified as positive when flowing into the device.

4

RECOMMENDED OPERATING CONDITIONS

Characteristics	Symbol	Min	Typ	Max	Unit
Analog Supply Voltage	AV_{CC}	4.75	5.0	5.25	V
Digital Supply Voltage	DV_{CC}	4.75	5.0	5.25	V
Output Dynamic Range	V_{DYN}	3.5	—	V_{CC}	V
Digital Input Low Voltage	V_{IL}	—	—	0.8	V
Digital Input High Voltage	V_{IH}	2.0	—	—	V
Clock High Time	V_{CKH}	20	—	—	ns
Clock Low Time	V_{CKL}	20	—	—	ns
Input Set-up Time	t_S	12	—	—	ns
Input Hold Time	t_H	12	—	—	ns
OP Amp Compersation Capacitor	C_{COMP}	1.0	—	—	1μF
Operating Ambient Temperature	T_A	0	—	70	°C

ELECTRICAL CHARACTERISTICS ($DV_{CC} = AV_{CC} = 5.0V$, $Ta = 25°C$)

Characteristics	Symbol	Test Condition	Min	Typ	Max	Unit
Supply Current	I_{CC}	$DV_{CC} = AV_{CC} = Max$	90	120	150	mA
Digital Input High Current	I_{IH}	$DV_{CC} = AV_{CC} = Max$, $V_{IN} = 2.4V$		100	200	μA
Digital Input Low Current	I_{IL}	$DV_{CC} = AV_{CC} = Max$, $V_{IN} = 0.4V$		−200	−500	μA
Output Resistance	R_{OUT}	Between AV_{CC} and A_{OUT}	80	90	100	ohm
Analog Output Delay Time	t_D	$V_{CC} = Min$, $V_{ref} = 4V$, $R_L = \infty$			25	ns
Rising Time	t_R	$V_{CC} = Min$, $V_{ref} = 4V$, $R_L = \infty$			10	ns
Falling Time	t_F	$V_{CC} = Min$, $V_{ref} = 4V$, $R_L = \infty$			10	ns
Settling Time	t_{SET}	$V_{CC} = Min$, $V_{ref} = 4V$, $R_L = \infty$			40	ns
Blank Level	V_{BLANK}	$V_{CC} = Typ$, $V_{ref} = 4V$, $R_L = \infty$	71	81	91	mV
Synk Level	V_{SYNC}	$V_{CC} = Typ$, $V_{ref} = 4V$, $R_L = \infty$	380	432	480	mV
Zero Code Output Voltage	V_{ZERO}	$V_{CC} = Typ$, $V_{ref} = 4V$, $R_L = \infty$	3.95	4.0	4.05	V
Full Scale Ouput Voltage	V_{FS}	$V_{CC} = Typ$, $V_{ref} = 4V$, $R_L = \infty$	0.95	1.0	1.05	V
Output Offset Voltage	V_{OFS}	$V_{CC} = Max$, $R_L = \infty$		±15	±25	mV
Differential Linearity Error	DLE	$V_{CC} = Typ$, $V_{ref} = 4V$, $R_L = \infty$	−0.5		+0.5	LSB
Integral Linearity Error	ILE	$V_{CC} = Typ$, $V_{ref} = 4V$, $R_L = \infty$	−1		+1	LSB
Glitch Energy	GE				200	PV-sec
Differential Phase	DP	$F_{CK} = 4$ fsc (NTSC)			2	°C
Differential Gain	DG	$F_{CK} = 4$ fsc (NTSC)			2	%
Max. Conversion Rate	F_{CK}	$V_{ref} = 4V$, $R_L = \infty$	25			MSPS

TIMING DIAGRAM

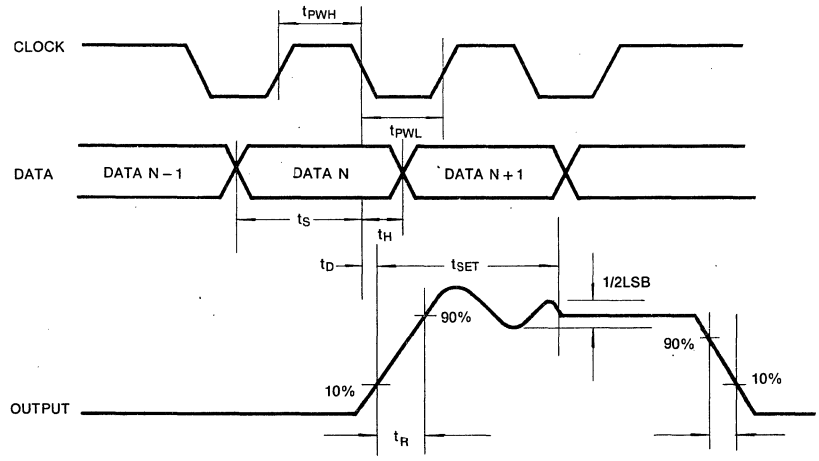


Fig. 3

INPUT/OUTPUT EQUIVALENT CIRCUIT

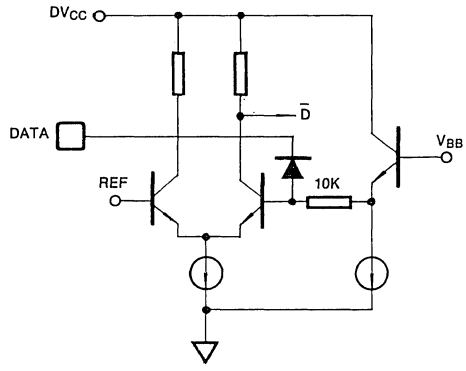


Fig. 4 Pin 19-26, Digital Input

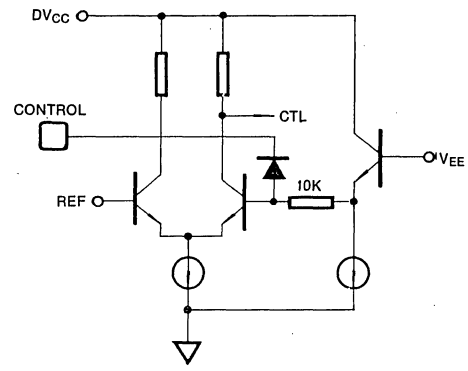


Fig. 5 Pin 3, 4, 5 & Pin 18, Control Signal & Clock Input

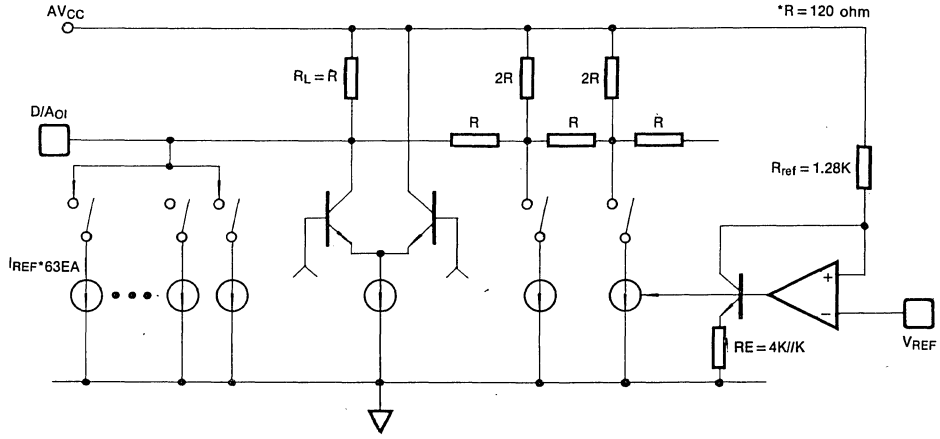


Fig. 6 Pin 6, 8, Reference Voltage and Analog Output

TEST CIRCUIT

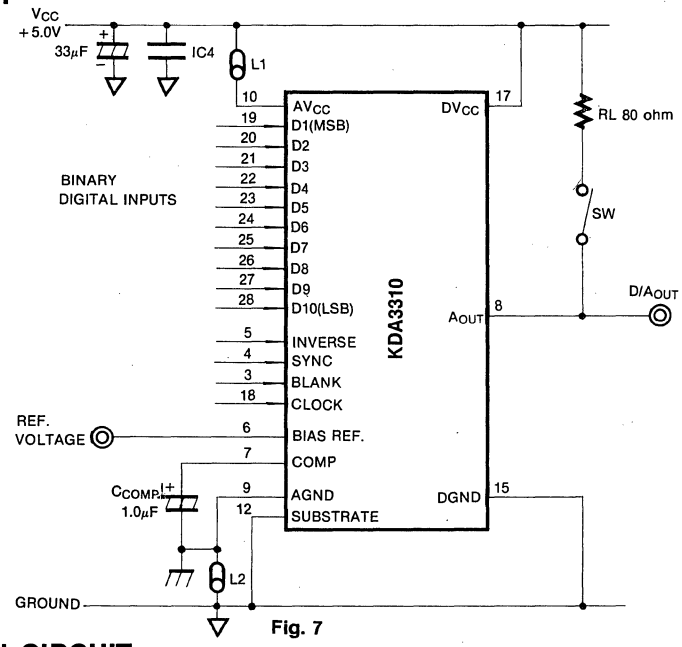


Fig. 7

APPLICATION CIRCUIT

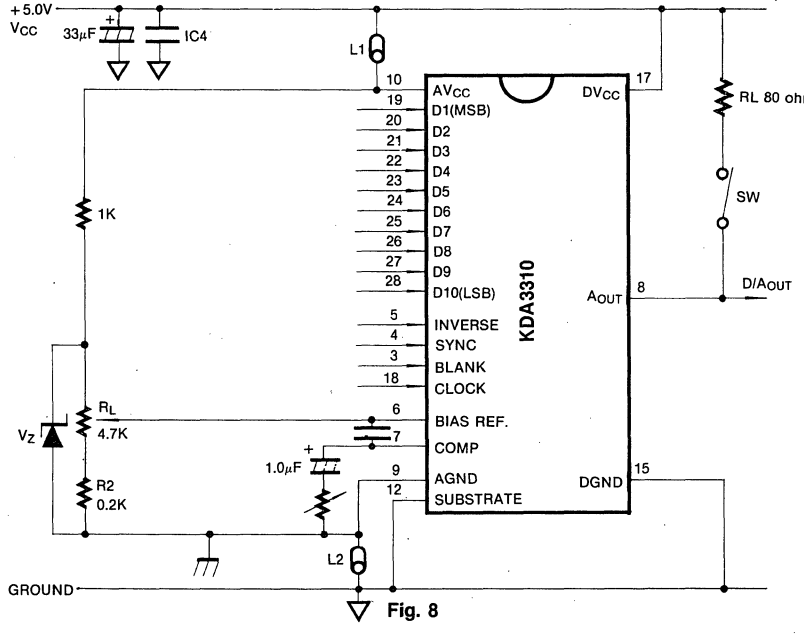


Fig. 8

ANALOG OUTPUT WAVEFORM

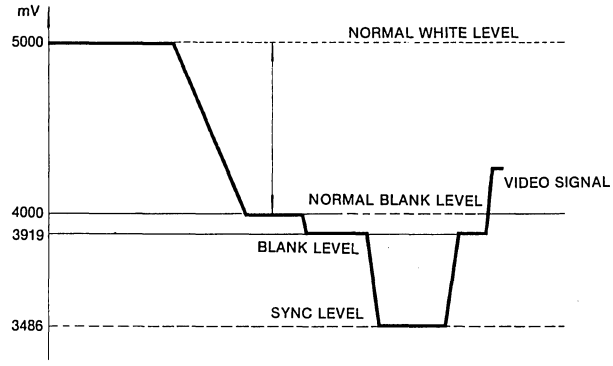


Fig. 9 Without Inverse Signal Input

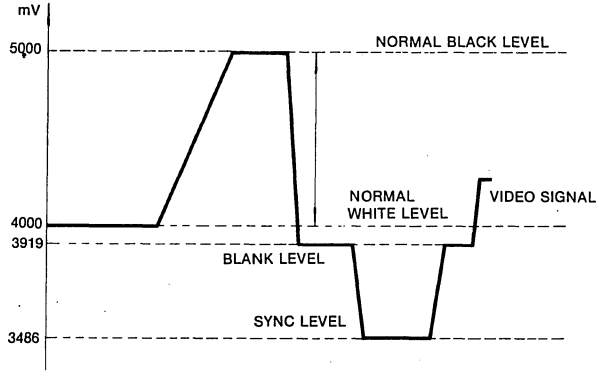


Fig. 10 With Inverse Signal Input

INPUT CODING vs. OUTPUT LEVEL

Without Video Control Signal (SYNC = BLANK = Low)

Inverse	Data Input	Output Level [mV]	Descriptions
0	1 1 1 ..... 1 1 1	5000	When V_{ref} = 4.0V, Standard Swing is $1V_{p-p}$
0	0 0 0 ..... 0 0 0	4000	
1	1 1 1 ..... 1 1 1	4000	
1	0 0 0 ..... 0 0 0	5000	

With Video Control Signal

Inverse	Sync	Blank	Data	Output Level [mV]	Descriptions
0	0	0	1 1 1 ..... 1 1 1	5000	Normal White
0	0	0	0 0 0 ..... 0 0 0	4000	Normal Black
0	0	1	X X X ..... X X X	3919	Blank Level
0	1	X	X X X ..... X X X	3486	Sync Level
1	0	0	1 1 1 ..... 1 1 1	4000	Inverse Normal White
1	0	0	0 0 0 ..... 0 0 0	5000	Inverse Normal Black
X	0	1	X X X ..... X X X	3919	Blank Level
X	1	X	X X X ..... X X X	3487	Sync Level

Notes: 1. Logic "high" is $+2.0V < V_{IH} < +5.0V$ at TTL input level.
2. Logic "low" is $+0.0V < V_{IH} < +0.8V$ at TTL input level.
3. X = "don't care."

OPERATION

1. General Information

KDA3310 is operated by +5.0V single supply. All the digital inputs is composed of TTL-to-CML input buffer circuit to transform the TTL signal into CML level which is needed internally.

Data through input buffer, upper 6 bits is separated into 63 segmented signals at decoder circuit and lower 4 bits is passed through 67 internal registers directly. At the internal register all the data, which is triggered at the falling edge of clock pulse signal, is latched simultaneously.

Latched data is transferred to the output current-switch, and their current switch is operatd by current source of data states. Analog output voltage is generated by the voltage drop across the resistor network.

Output voltage swing is determined by the applied voltage to external reference voltage pin 6. In the case of not using video control signals such as sync and blank and when R_L = open and V (pin 6) = 4V, output amplitude is 1 $V_{p\text{-}p}$ swing, when R_L = 85 and V (pin 6) = 3V, output becomes 1 $V_{p\text{-}p}$ swing. Moreover, KDA3310 has sync, blank, inverse function of video control signal.

2. Power Supply

The KDA3310 can be operated from a single +5.0V power supply. In order to prevent digital ground noise from disturbing the analog circuitry, digital and analog sections are separated. Current from the current sources are switched accordingly and combined in the resistor network to give an analog output voltage. Digital current path is applied in input buffer stage, decorder circuit and register block.

3. Input Stage

The input stage transforms the TTL mode input signal into required CML level. With low inverse signal, data input signal is activated in low logic state. Therefore output level is reduced. In high logic state control input becomes reverse result occurs.

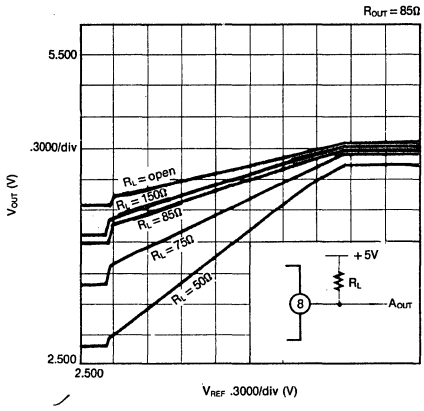
4. Image Control Signal

Unlike data signal, control signal is activated in high logic state. Without control signal, analog output is determined according to the input data. If blank signal is present, all data signals are "set" and also blank output level is obtained by blank current switch.
However, sync signal ignores both data and blank signals which are set to activate additional current switch. As a result sync level is achieved. Only gray scale signal is influence by inverse signal and negative blank and sync level is resulted.

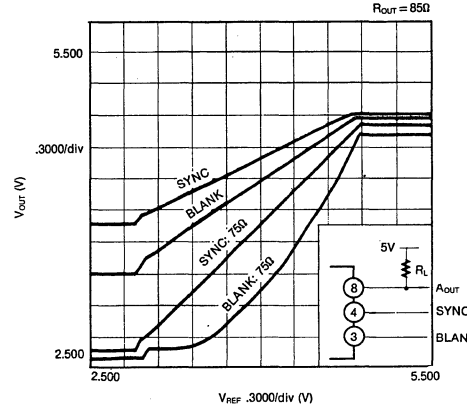
5. Base Voltage Circuit and Analog Output Circuit

The ZA33100 acquires built-in oscillator. The standard input voltage is normally 4.0V and by modulating this voltage can vary the swing width of output level. The internal operational amplifier of ZA33100 is frequency stabilized by an compansation capacitor of pin 7. 1.0μF tantalum capacitor is recommended for optimum performance. The analog output voltage appears proportionally with the input data.

GRAPHICS PLOT (V_{REF} vs AV_{OUT})



GRAPHICS PLOT (V_{REF} vs AV_{OUT} WITH BLANK, SYNC)



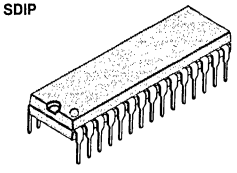
HIGH SPEED TRIPPLE D/A CONVERTER
6 BITS TRIPPLE, 20 MSPS

The KDA0406 is a monolithic 6 bit tripple DAC which applies 2μm bipolar process. Decoding method and R-2R collector split method are combined to realize the device. In the device operating on a single +5V, signal transformation upto 20MSPS (Mega Sample Per Second) is possible. This DAC is designed for Video Application and has output dynamic range of 4 to 5V.

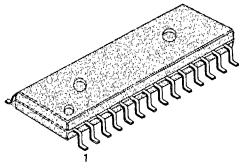
In order to have less input data lines and package pins, six pins provide input data to three DAC according to whether clock is enabled. Where clock is unenabled, its internal register holds the input data of previous condition so the analog output in previous condition is maintained.

All the data input and input signals of clock and control are controlled by the TTL CMOS level. Since there is a built-in register, the input data can be used by transforming into analog signal, after being synchronized into a clock signal, without additional deglitch circuit. Moreover the built-in generating circuit for reference voltage provides easy application of the device.

28 SDIP



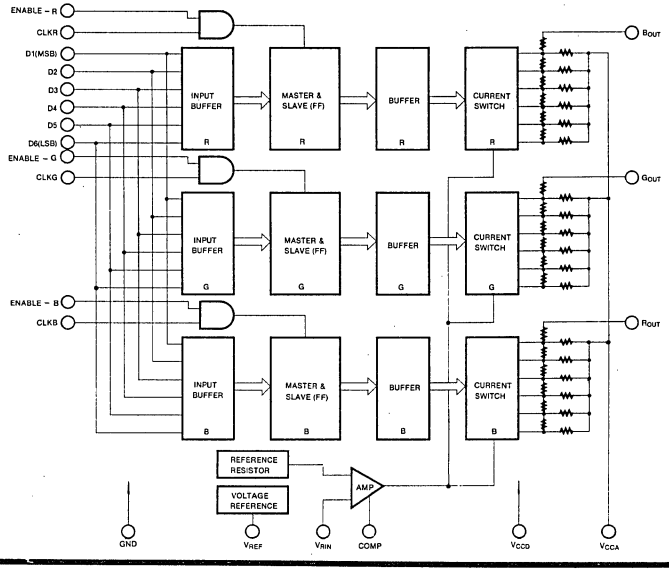
28 SOP



FEATURES

- **Resolution: 6 Bit**
- **Linearity error: less than ±1/2 LSB**
- **Maximum conversion rate: 20 MSPS**
- **Analog output dynamic range: 4 – 5V**
- **Data, clock enable input: TTL, CMOS level compatible**
- **Single power supply: 5 ± 0.25V**
- **Low power dissipation: 300 mW (typ.)**

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Characteristics	Symbol	Value	Unit
Supply Voltage	V_{CCA}, V_{CCD}	−0.5 to 6.0	V
Supply Difference	$V_{CCA} - V_{CCD}$	−0.5 to 0.5	V
Digital Input Voltage	V_{DIN}	−0.5 to 6.0	V
Reference Voltage Input	V_{RIN}	3.0 to 6.0	V
Analog Output Voltage	V_{OUT}	3.0 to 6.0	V
Ambient Operating Temperature Range	T_a	−25 ~95	°C
Storage Temperature Range	T_{stg}	−55 ~125	°C

Notes: 1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions.
2. Functional operation under any of these conditions is not impiled.
3. Applied voltage must be current limited to specified range.
4. Current is specified as positive when flowing into the device.

RECOMMENDED OPERATING CONDITIONS

Characteristics	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CCA}, V_{CCD}	4.75	5.00	5.25	V
Supply Difference	$V_{CCA} - V_{CCD}$	−0.05	0	0.05	V
Clock High Time	t_{PWH}	25			ns
Clock Low Time	t_{PWL}	25			ns
Input Data Set-up Time	t_S	15			ns
Input Data Hold Time	t_H	15			ns
Digital Input Voltage, Low	V_{IL}			0.8	V
Digital Input Voltage, High	V_{IH}		2.0		V
Reference Voltage Input	V_{RIN}	3.8	4.0	4.2	V
Compensation Capacitor	C_{COMP}	1			μF
Ambient Operating Temperature Range	T_a	0		70	°C

D.C. ELECTRICAL CHARACTERISTICS WITHIN SPECIFIED CONDITION

Characteristics	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Current	$I_{CCD} + I_{CCA}$	V_{CC} = Max		60	80	mA
Reference Output Voltage	V_{ROUT}	V_{CC} = Typ	3.8	4.0	4.2	V
Reference Output Voltage Variation	V_{ROT}	0°C ~ 70°C			28	mV
Reference Input Current	I_{RIN}	V_{CC} = Max			10	μA
Digital Input Current, Low	I_{IL}	V_{CC} = Max, V_I = 0.4V			−400	μA
Digital Input Current, High	I_{IH}	V_{CC} = Max, V_I = 2.4V			200	μA
Output Resistance	R_{OUT}	V_{CCA} to A_{OUT}	190	240	290	ohm

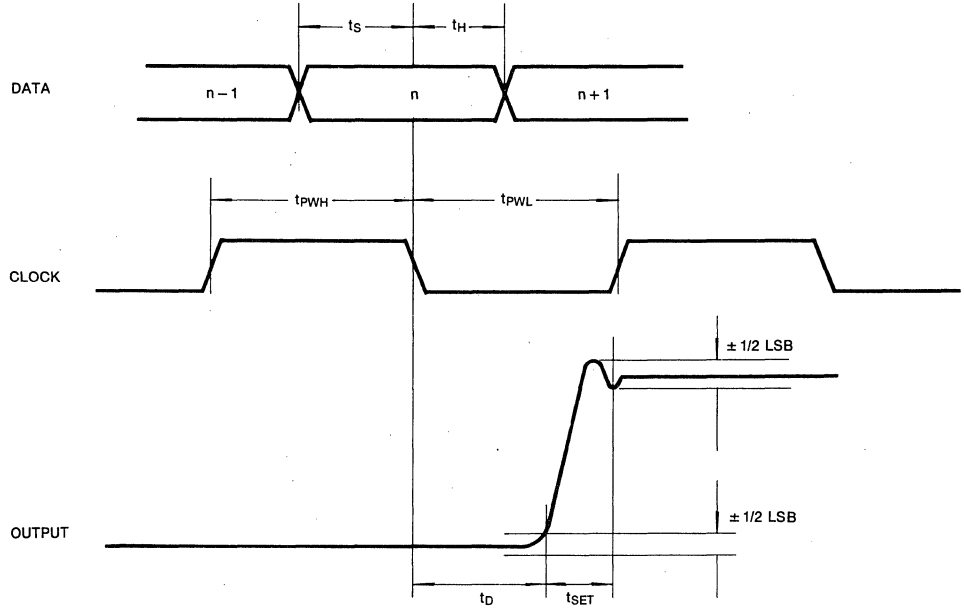
A.C. ELECTRICAL CHARACTERISTICS WITHIN SPECIFIED CONDITION

Characteristics	Symbol	Test Conditions	Min	Typ	Max	Unit
Maximum Conversion Rate	f_C	V_{CC} = Min			20	MSPS
Analog Output Delay	t_D	V_{CC} = Min			20	ns
Settling Time	t_{SET}	V_{CC} = Min			40	ns
Rise Time (10%→90%)	t_r	V_{CC} = Typ			10	ns

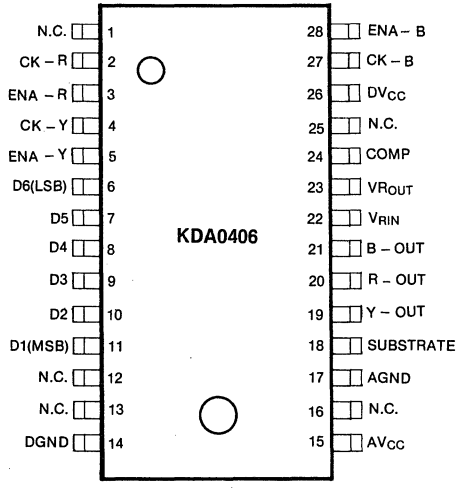
PERFORMANCE CHARACTERISTICS WITHIN SPECIFIED CONDITION

Characteristics	Symbol	Test Conditions	Min	Typ	Max	Unit
Integral Linearity Error	E_{LI}	V_{CC} = Typ			±0.8	%
Differential Linearity Error	E_{LD}	V_{CC} = Typ			±0.8	%
Zero Scale Output Voltage	V_{OZS}	V_{CC} = Typ, V_{RIN} = 4.0V	3.9	4.0	4.1	V
Full Scale Output Voltage	V_{OFS}	V_{CC} = Max	V_{CC} − 15	V_{CC}	V_{CC} + 15	mV
Zero Scale Channel Variation	$\triangle V_{CH}$	V_{CC} = Typ, V_{RIN} = 4.0V			30	mV
Differential Phase	DP	f_C = 4 fsc			2	°C
Differential Gain	DG	f_C = 4 fsc			2	%

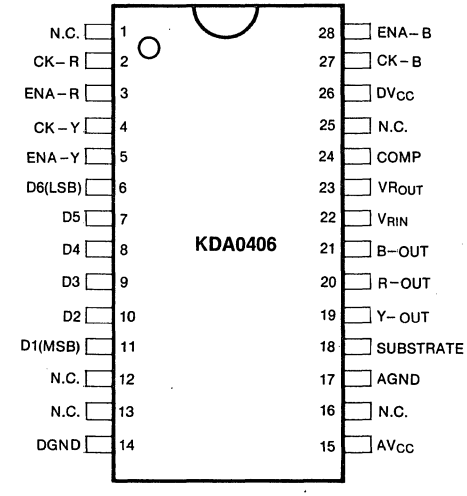
TIMING DIAGRAM



PIN CONFIGURATION

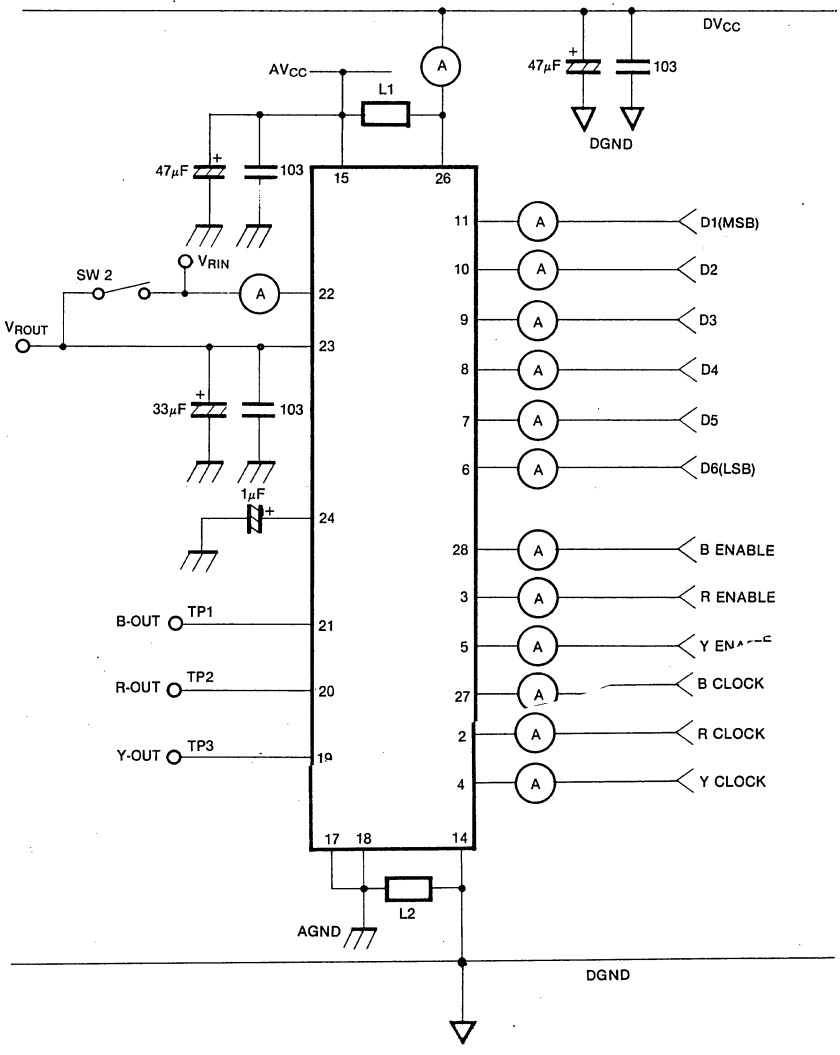


(TOP VIEW)

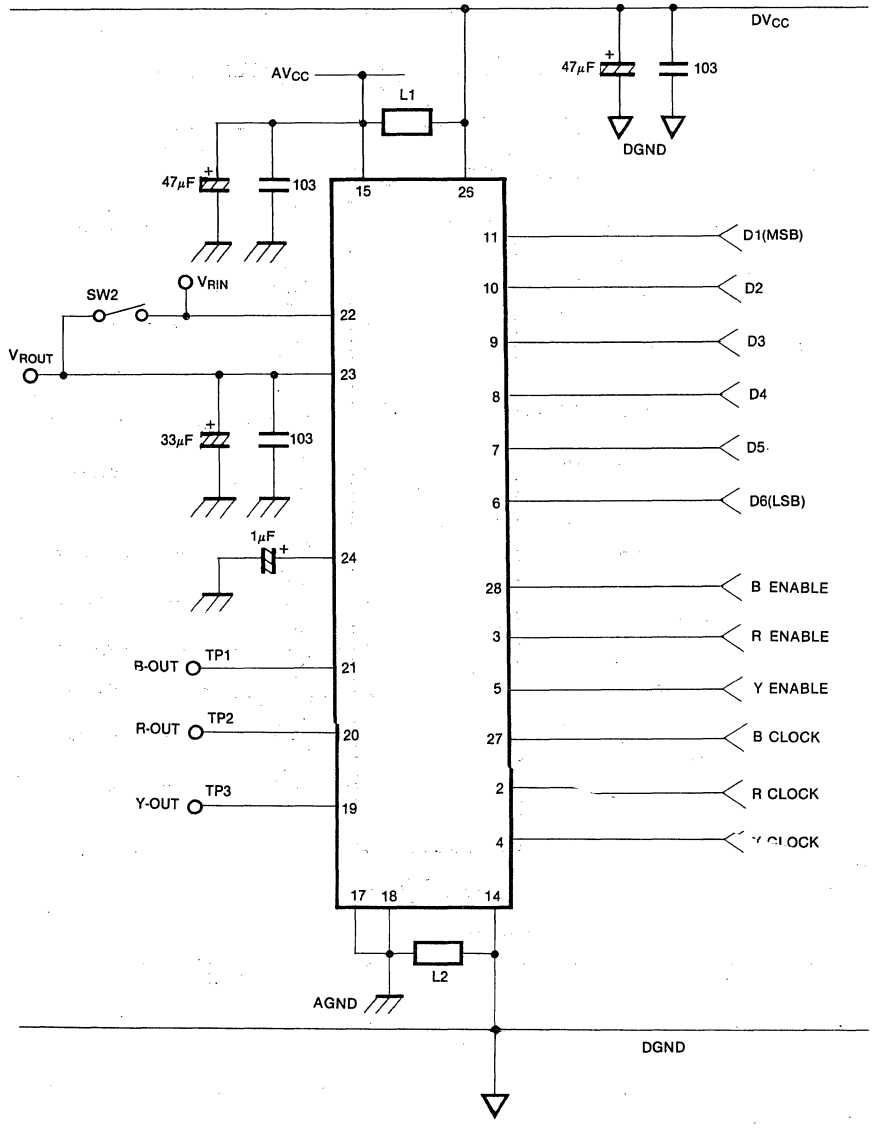


(TOP VIEW)

KDA0406 D.C. TEST CIRCUIT



KDA0406 A.C. TEST CIRCUIT

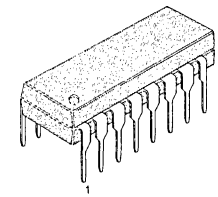


8-BIT D/A CONVERTER

The KDA0800 series are monolithic 8-bit high-speed current-output digital-to-analog converters (DAC) featuring typical settling times of 100ns. When used as a multiplying DAC, monotonic performance over a 40 to 1 reference current range is possible. The KDA0800 series also features high compliance complementary current outputs to allow differential output voltages of 20 V_{p-p} with simple resistor loads. The reference-to-full-scale current matching of better than ±1 LSB eliminates the need for full-scale trims in most applications while the nonlinearities of better than ±0.1% over temperature minimizes system error accumulations.

The noise immune inputs of the KDA0800 series will accept TTL levels with the logic threshold pin, V_{LC}, potential allow direct interface to all logic families. The performance and characteristics of the device are essentially unchanged over the full ±4.5V to ±18V power supply range; power dissipation is only 33mW with ±5V supplies and is independent of the logic input states.

16 DIP



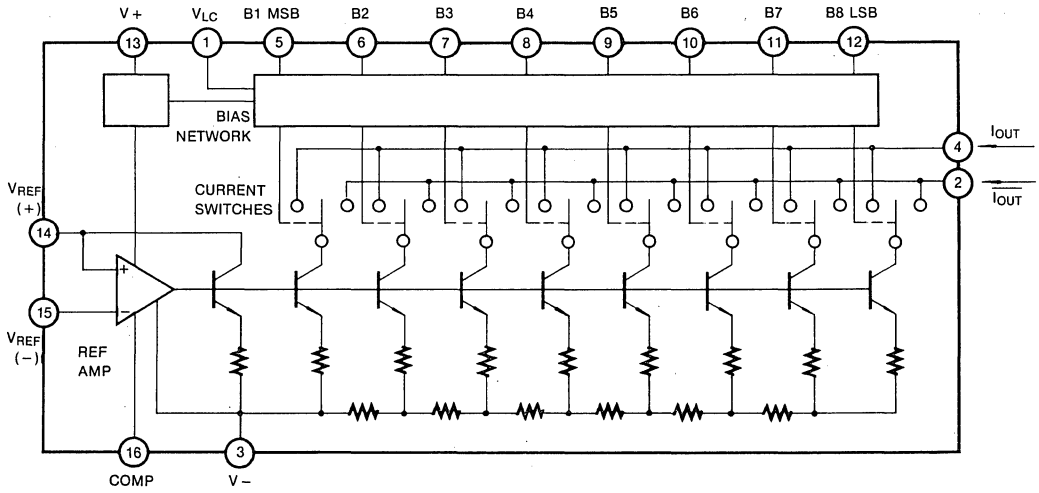
FEATURES

- **Fast settling output time: 100ns**
- **Full scale error: ±1 LSB**
- **Nonlinearity over temperature: ±0.1%**
- **Full scale current drift: ±10 ppm/°C**
- **High output compliance: −10V to +18V**
- **Complementary current outputs**
- **Interface directly with TTL, CMOS, PMOS and others**
- **2 quadrant wide range multiplying capability**
- **Wide power supply range: ±4.5V to ±18V**
- **Low power consumption: 33mW at ±5V**
- **Low cost**
- **Standard 16 DIP package**

ORDERING INFORMATION

Device	Package	Temperature Range	Nonlinearity
KDA0800CN	16 DIP	0 ~ +70°C	±0.19%FS
KDA0801CN			±0.39%FS
KDA0802CN			±0.1%FS

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	±18V or 36V	V
Power Dissipation	P_D	500	mW
Reference Input Differential Voltage (V14 to V15)	V_{IN}	$V_- \sim V_+$	V
Reference Input Common-Mode Range (V14, V15)	V_{IN}	$V_- \sim V_+$	V
Reference Input Current	I_{ref}	5	mA
Logic Inputs	V_{IN}	$V_- \sim V_- + 36V$	V
Operating Temperature	T_{opr}	0°C ~ +70°C	°C
Storage Temperature	T_{stg}	−65°C ~ +150°C	°C

ELECTRICAL CHARACTERISTICS

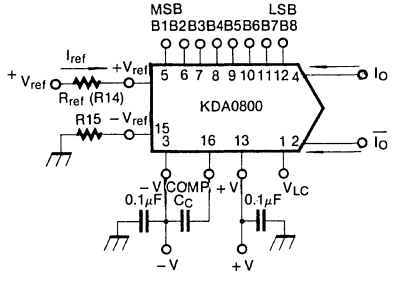
($V_S = \pm 15V$, $I_{ref} = 2mA$, $T_{min} \leq Ta \leq T_{max}$ unless otherwise specified. Output characteristics refer to both I_{OUT} and I_{OUT}.)

Characteristic	Symbol	Test Conditions	KDA0800			Unit
			Min	Typ	Max	
Resolution			8	8	8	Bits
Monotonicity			8	8	8	Bits
Nonlinearity		KDA0802 KDA0800 KDA0801	—	—	±0.1 ±0.19 ±0.39	%FS
Settling Time	t_S	To ±1/2 LSB, all bits switched "ON" or "OFF", Ta=25°C	—	100	150	ns
Propagation Delay Each Bit All Bits Switched	t_{PLH}, t_{PHL}	Ta=25°C	 — —	 35 35	 60 60	 ns ns
Full Scale Tempco	TCI_{FS}			±10	±50	ppm/°C
Output Voltage Compliance	V_{OC}	Full scale current change <1/2 LSB, R_{OUT}>20MΩ Typ	−10	—	18	V
Full Scale Current	I_{FS4}	V_{ref}=10V, R14=5KΩ R15=5KΩ, Ta=25°C	1.94	1.99	2.04	mA
Full Scale Symmetry	I_{FSS}	$I_{FS4} - I_{FS2}$	—	±1	±8.0	μA
Zero Scale Current	I_{ZS}		—	0.2	2.0	μA
Output Current Range	I_{FSR}	V− = −5V V− = −8V to −18V	0 0	2.0 2.0	2.1 4.2	mA mA
Logic Input Levels Logic "0" Logic "1"	 V_{IL} V_{IH}	V_{LC}=0V	 2.0	 — —	 0.8	 V V
Logic Input Current Logic "0" Logic "1"	 I_{IL} I_{IH}	V_{LC}=0V −10V≤V_{IN}≤+0.8V 2V≤V_{IN}≤+18V	 — —	 −2.0 0.002	 −10 10	 μA μA
Logic Input Swing	V_{IS}	V− = −15V	−10	—	18	V
Logic Threshold Range	V_{THR}	$V_S = \pm 15V$	−10	—	13.5	V
Reference Bias Current	I_{15}		—	−1.0	−3.0	μA
Reference Input Slew Rate	dI/dt		4.0	8.0	—	mA/μs
Power Supply Sensitivity	$PSSI_{FS+}$	4.5V≤V+≤18V	—	0.0001	0.01	%/%

ELECTRICAL CHARACTERISTICS (Continued)

Characteristic	Symbol	Test Conditions	KDA0800			Unit
			Min	Typ	Max	
	$PSSI_{FS-}$	$-4.5V \leq V- \leq 18V$ $I_{ref} = 1mA$	—	0.0001	0.01	%/%
Power Supply Current	I+	$V_S = \pm 5V$, $I_{ref} = 1mA$	—	2.3	3.8	mA
	I−		—	−4.3	−5.8	mA
	I+	$V_S = 5V, -15V$, $I_{ref} = 2mA$	—	2.4	3.8	mA
	I−		—	−6.4	−7.8	mA
	I+	$V_S = \pm 15V$, $I_{ref} = 2mA$	—	2.5	3.8	mA
	I−		—	−6.5	−7.8	mA
Power Dissipation	P_D	$\pm 5V$, $I_{ref} = 1mA$	—	33	48	mW
		$5V, -15V$, $I_{ref} = 2mA$	—	108	136	mW
		$\pm 15V$, $I_{ref} = 2mA$	—	135	174	mW

TYPICAL APPLICATIONS



$$I_{FS} \cong \frac{+V_{ref}}{R_{ref}} \times \frac{255}{256}$$

$I_O + \overline{I_O} = I_{FS}$ for all logic states

For fixed reference, TTL operation, typical values are:

$V_{ref} = 10V$

$R_{ref} = 5K\Omega$

$R15 \cong R_{ref}$

$C_C = 0.01\mu F$

$V_{LC} = 0V$ (Ground)

Fig. 1 Basic Positive Reference Operation

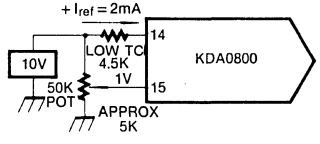
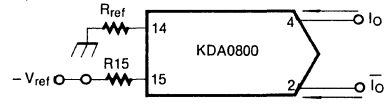


Fig. 2 Recommended Full Scale Adjustment Circuit

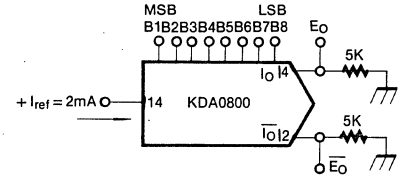


$$I_{FS} \cong \frac{-V_{ref}}{R_{ref}} \times \frac{255}{256}$$

Note: R_{ref} sets I_{FS}: R15 is for bias current cancellation

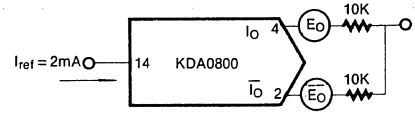
Fig. 3 Basic Negative Reference Operation

TYPICAL APPLICATIONS (Continued)



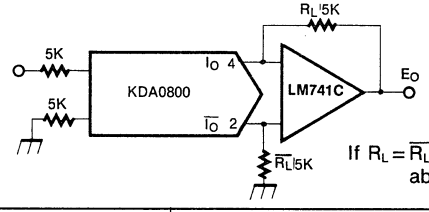
	B1	B2	B3	B4	B5	B6	B7	B8	I_o mA	$\overline{I_o}$ mA	E_o	$\overline{E_o}$
Full Scale	1	1	1	1	1	1	1	1	1.992	0.000	−9.960	0.000
Full Scale − LSB	1	1	1	1	1	1	1	0	1.984	0.008	−9.920	−0.040
Half Scale + LSB	1	0	0	0	0	0	0	1	1.008	0.984	−5.040	−4.920
Half Scale	1	0	0	0	0	0	0	0	1.000	0.992	−5.000	−4.960
Half Scale − LSB	0	1	1	1	1	1	1	1	0.992	1.000	−4.960	−5.000
Zero Scale + LSB	0	0	0	0	0	0	0	1	0.008	1.984	−0.040	−9.920
Zero Scale	0	0	0	0	0	0	0	0	0.000	1.992	0.000	−9.960

Fig. 4 Basic Unipolar Negative Operation



	B1	B2	B3	B4	B5	B6	B7	B8	E_o	$\overline{E_o}$
Pos. Full Scale	1	1	1	1	1	1	1	1	−9.920	+10.000
Pos. Full Scale − LSB	1	1	1	1	1	1	1	0	−9.840	+9.920
Zero Scale + LSB	1	0	0	0	0	0	0	1	−0.080	+0.160
Zero Scale	1	0	0	0	0	0	0	0	0.000	+0.080
Zero Scale − LSB	0	1	1	1	1	1	1	1	+0.080	0.000
Neg. Full Scale + LSB	0	0	0	0	0	0	0	1	+9.920	−9.840
Neg. Full Scale	0	0	0	0	0	0	0	0	+10.000	−9.920

Fig. 5 Basic Diploar Output Operation

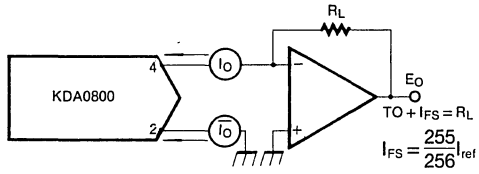


If $R_L = \overline{R_L}$ within ±0.05%, output is symmetrical about ground

	B1	B2	B3	B4	B5	B6	B7	B8	E_o
Pos. Full Scale	1	1	1	1	1	1	1	1	+9.920
Pos. Full Scale − LSB	1	1	1	1	1	1	1	0	+9.840
(+) Zero Scale	1	0	0	0	0	0	0	0	+0.040
(−) Zero Scale	0	1	1	1	1	1	1	1	−0.040
Neg. Full Scale + LSB	0	0	0	0	0	0	0	1	−9.840
Neg. Full Scale	0	0	0	0	0	0	0	0	−9.920

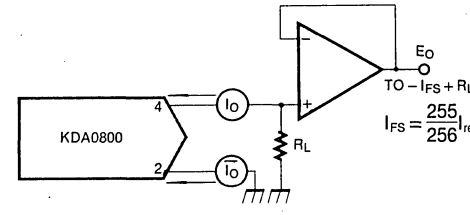
Fig. 6 Symmetrical Offset Binary Operation

TYPICAL APPLICATIONS (Continued)



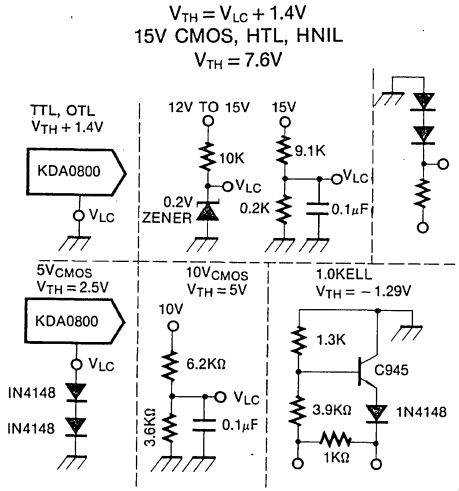
For complementary output (operation as negative logic DAC), connect inverting input of op amp to $\overline{I_O}$ (pin 2), connect I_O (pin 4) to ground.

Fig. 7 Positive Low Impedance Output Operation



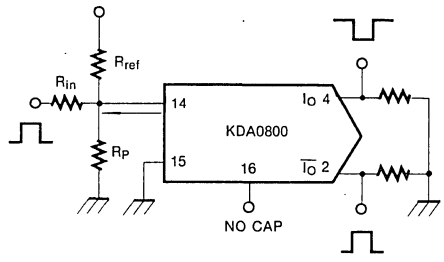
For complementary output (operation as a negative logic DAC) connect non-inverting input of op am to I_O (pin 2); connect I_O (pin 2); connect I_O (pin 4) to ground.

Fig. 8 Negative Low Impedance Output Operation



Do not exceed negative logic input range of DAC.

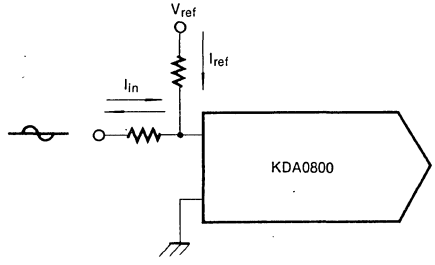
Fig. 9 Interfacing with Various Logic Families



Typical values: $R_{IN} = 5K_1 + V_{IN} = 10V$

Fig. 10 Pulsed Reference Operation

(a) $I_{ref} \geq$ peak negative swing of I_{IN}



(b) $+V_{ref}$ must be above peak positive swing of V_{IN}

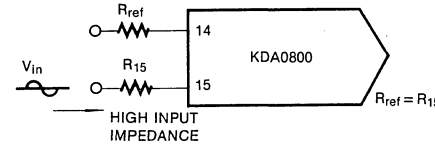


Fig. 11. Accommodating Bipdlar References

TYPICAL APPLICATIONS (Continued)

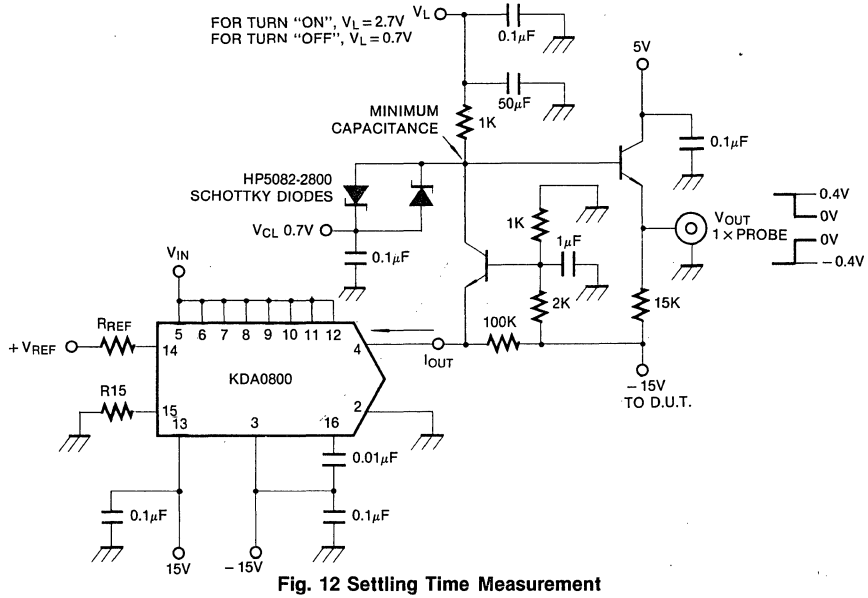
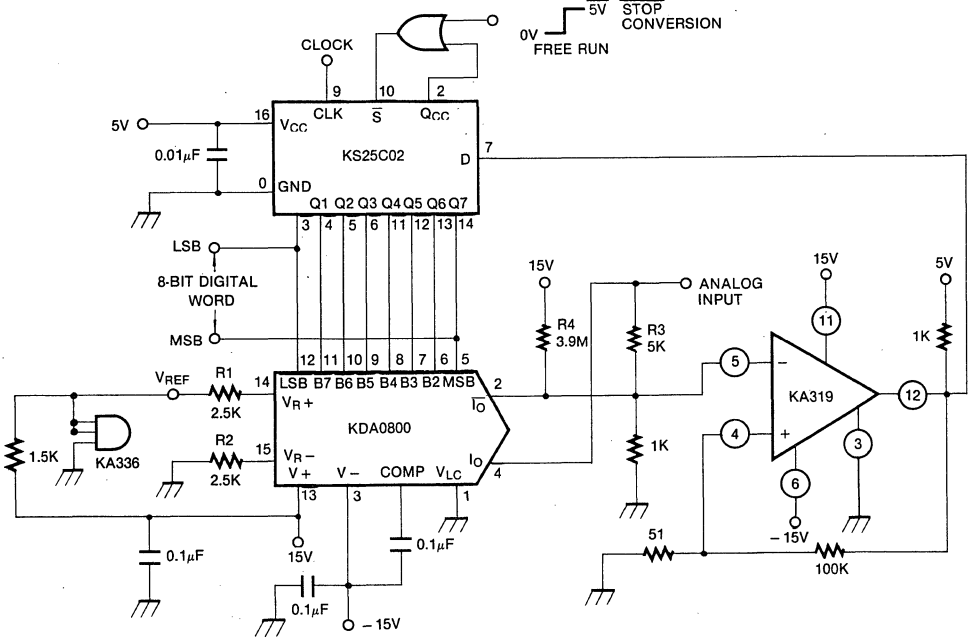


Fig. 12 Settling Time Measurement



Note. For 1 μs conversion time with 8-bit resolution and 7-bit accuracy, an KA361 comparator replaces the KA319 and the reference current is doubled by reducing R1, R2 and R3 to 1.25KΩ and R4 to 2MΩ.

Fig. 13 A Complete 2 μs Conversion Time, 8-Bit A/D Converter

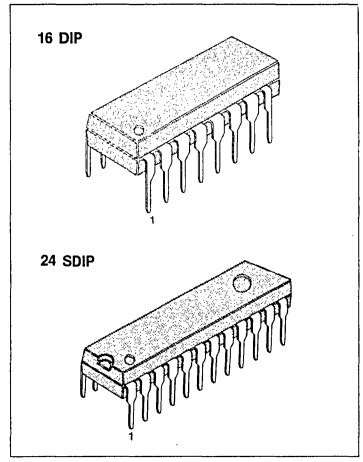
8-BIT AND 12-BIT CMOS SUCCESSIVE APPROXIMATION REGISTERS

These are 8-bit and 12-bit CMOS registers designed for use in successive approximation A/D converters. They contain all the logic and control circuits necessary in combination with the A/D converter to perform successive approximation analog-to-digital conversions.

The KS25C02 has 8 bits with serial capability and is not expandable. The KS25C03 has 8 bits and is expandable without serial capability. The KS25C04 has 12 bits with serial capability and expandibility.

Fabricated using a 2μm, dual-layer metal CMOS process, these parts deliver speeds and drive capability equivalent to their TTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.



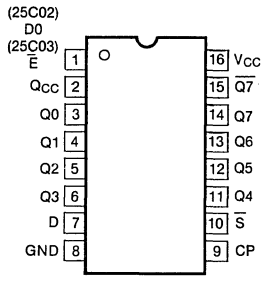
ORDERING INFORMATION

Device	Package	Temperature Range	Registers
KS25C02IN	16 DIP	−40°C ~ +85°C	8 bit
KS25C03IN	16 DIP		
KS25C04IN	24SDIP		12 bit

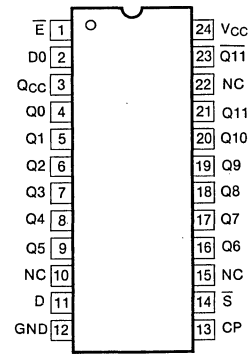
FEATURES

- **Complete logic for successive approximation A/D converters**
- **8-bit and 12-bit registers**
- **Capable of short cycle or expanded operation**
- **Continuous or start-stop operation**
- **Compatible with D/A converters using any logic code**
- **Active low or active high logic outputs**
- **Use as general purpose serial-to-parallel converter or ring counter**
- **Low power consumption characteristics of CMOS**
- **Inputs and outputs interface directly with TTL, NMOS and TTL devices.**

PIN CONFIGURATIONS

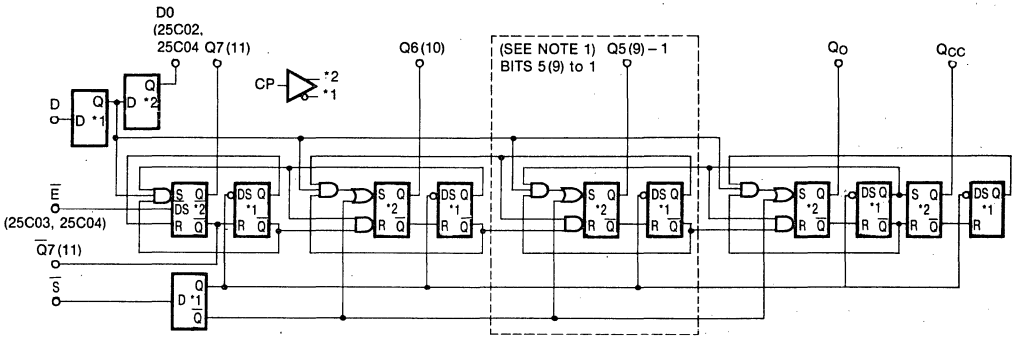


KS25C02 AND KS25C03



KS25C04

LOGIC DIAGRAM



NOTE 1: Cell logic is repeated for register stages Q5 to Q1 KS25C02, KS25C03
2: Numbers in parenthesis are for KS25C04

TRUTH TABLE

Time	Inputs			Outputs[1]									
t_n	D	$\overline{S}$	$\overline{E}$[2]	D0[3]	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0	Q_{CC}
0	X	L	L	X	X	X	X	X	X	X	X	X	X
1	D7	H	L	X	L	H	H	H	H	H	H	H	H
2	D6	H	L	D7	D7	L	H	H	H	H	H	H	H
3	D5	H	L	D6	D7	D6	L	H	H	H	H	H	H
4	D4	H	L	D5	D7	D6	D5	L	H	H	H	H	H
5	D3	H	L	D4	D7	D6	D5	D4	L	H	H	H	H
6	D2	H	L	D3	D7	D6	D5	D4	D3	L	H	H	H
7	D1	H	L	D2	D7	D6	D5	D4	D3	D2	L	H	H
8	D0	H	L	D1	D7	D6	D5	D4	D3	D2	D1	L	H
9	X	H	L	D0	D7	D6	D5	D4	D3	D2	D1	D0	L
10	X	X	L	X	D7	D6	D5	D4	D3	D2	D1	D0	L
	X	X	H	X	H	NC	NC	NC	NC	NC	NC	NC	NC

NOTES:
1: Truth table for KS25C04 is extended to include 12 outputs.
2: Truth table for KS25C02 does not include $\overline{E}$ column or last line in truth table shown.
3: Truth table for KS25C03 does not include D0 column.
H = High Voltage Level
L = Low Voltage Level
X = Don't Care
NC = No Change

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.5 ~ +7	V
DC Input Diode Current	I_{IK}	±20	mA
DC Output Diode Current	I_{OK}	±20	mA
Continuous Output Current Per Pin	I_O	±35	mA
Continuous Current Through V_{CC} or GND Pins	I_{CON}	±125	mA
Power Dissipation Per Package	P_D	500	mW
Operating Temperature	T_{opr}	0 ~ +70	°C
Storage Temperature	T_{stg}	−55 ~ +125	°C

DC ELECTRICAL CHARACTERISTICS (Over Recommended Operating Conditions)

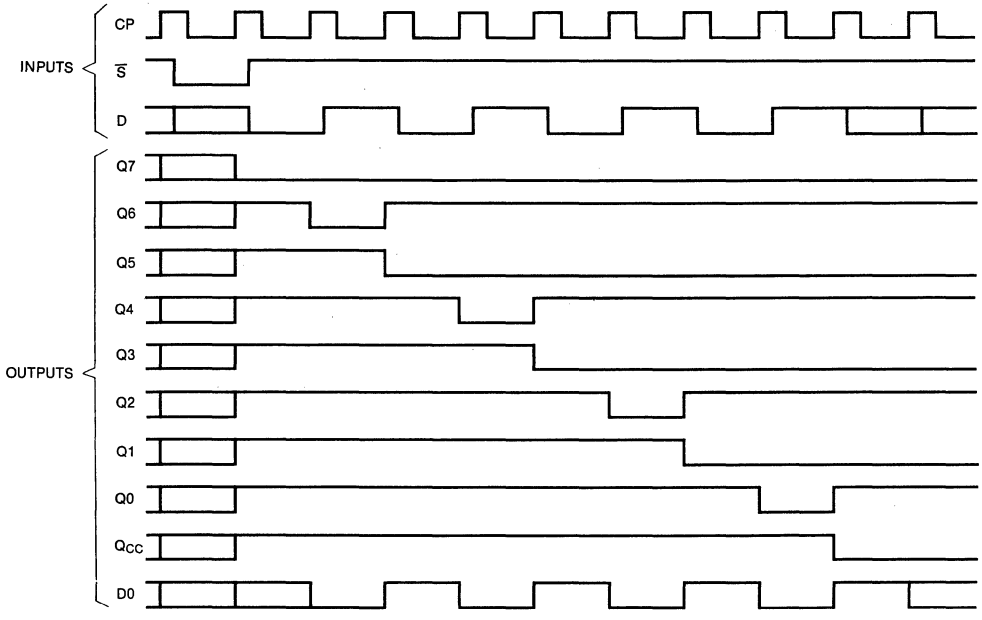
Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Operation Voltage	V_{CC}		4.5	5.0	5.5	V
High-Level Input Voltage	V_{IH}	V_{CC} = Min	2.0	—	V_{CC}	V
Low-Level Input Voltage	V_{IL}	V_{CC} = Min	0	—	0.8	V
High-Level Output Voltage	V_{OH}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL} I_O = −20μA I_O = −4mA	 V_{CC}-0.1 2.4	 — —	 V_{CC} V_{CC}	 V V
Low-Level Output Voltage	V_{OL}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL} I_O = 20μA I_O = 9.6mA	 0 0	 — —	 0.1 0.4	 V V
Low-Level Input Current	I_{IL}	V_{CC} = Max, V_{IL} = 0.4V	—	0.5	1.0	μA
High-Level Input Current	I_{IH}	V_{CC} = Max, V_{IH} = 2.4V	—	0.5	1.0	μA
Supply Current	I_{CC}	V_{CC} = Max, V_{IN} = V_{CC} or GND	—	1.0	10.0	μA

AC ELECTRICAL CHARACTERISTICS (Over Recommended Operating Conditions), C_L = 15pF

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Propagation Delay to a Logical "0" from CP to any Output	t_{PD0}		10	18	28	ns
Propagation Delay to a Logical "0" from $\overline{E}$ to Q7(Q11) Output	t_{PD0}	CP high, $\overline{S}$ low, KS25C03, KS25C04 only	—	15	24	ns
Propagation Delay to a Logical "1" from CP to Any Output	t_{PD1}		10	20	38	ns
Propagation Delay to a Logical "1" from $\overline{E}$ to Q7(Q11) Output	t_{PD1}	CP high, $\overline{S}$ low, KS25C03, KS25C04 only	—	12	19	ns
Data Input Setup Time	$t_{S(D)}$		−10	4	8	ns
Start Input Setup Time	$t_{S(S)}$		0	5	10	ns
Minimum Low CP Width	t_{PWL}		—	5	20	ns
Minimum High CP Width	t_{PWH}		—	15	20	ns
Maximum Clock Frequency	f_{MAX}		—	—	25	MHz

TIMING DIAGRAMS

KS25C02, KS25C03, KS25C04



APPLICATION INFORMATION

Operation

The registers consist of a set of master latches that act as the control elements in the device and change state on the input clock high-to-low transition and a set of slave latches that hold the register data and change on the input clock low-to-high transition. Externally the device acts as a special purpose serial-to-parallel converter that accepts data at the D input of the register and sends the data to the appropriate slave latch to appear at the register output and the D0 output on the KS25C02 and KS25C04 when the clock goes from low-to-high. There are no restrictions on the data input; it can change state at any time except during a short interval centered about the clock low-to-high transition. At the same time that data enters the register bit the next less significant bit register is set to a low ready for the next iteration.

The register is reset by holding the $\overline{S}$ (Start) signal low during the clock low-to-high transition. The register synchronously resets to the state Q7(11) low, and all the remaining register outputs high. The Q_{CC} (Conversion Complete) signal is also set high at this time. The $\overline{S}$ signal should not be brought back high until after the clock low-to-high transition in order to guarantee correct resetting. After the clock has gone high resetting the register, the $\overline{S}$ signal must be removed. On the next clock low-to-high transition the data on the D input is set into the Q7(11) register bit and the Q6(10) register bit and Q5(9) is set to a low. This operation is repeated for each register bit in turn until the register has been filled. When the data goes into Q0, the Q_{CC} signal goes low, and the register is inhibited from further change until reset by a Start signal.

The KS25C02, KS25C03 and KS25C04 have a specially tailored two-phase clock generator to provide non-overlapping two-phase clock pulses (i.e., the clock waveforms intersect below the thresholds of the gates they drive). Thus, even at very slow dV/dt rates at the clock input (such as from relatively weak comparator outputs), improper logic operation will not result.

Logic Codes

All three registers can be operated with various logic codes. Two's complement code is used by offsetting the comparator 1/2 full range + 1/2 LSB and using the complement of the MSB ($\overline{Q}7$ or $\overline{Q}11$) with a binary D/A

APPLICATION INFORMATION (Continued)

converter. Offset binary is used in the same manner but with the MSB ($\overline{Q}7$ or $\overline{Q}11$). BCD D/A converters can be used with the addition of illegal code suppression logic.

Active High or Active Low Logic

The register can be used with either D/A converters that require a low voltage level to turn on, or D/A converters that require a high voltage level to turn the switch on. If D/A converters are used which turn on with a low logic level, the resulting digital output from the register is active low. That is, a logic "1" is represented as a low voltage level. If D/A converters are used that turn on with a high logic level then the digital output is active high; a logic "1" is represented as a high voltage level.

Expanded Operation

An active low enable input, $\overline{E}$, on the KS25C03 and KS25C04 allows registers to be connected together to form a longer register by connecting the clock, D, and S inputs in parallel and connecting the Q_{CC} output of one register to the $\overline{E}$ input of the next less significant register. When the start resets the register, the $\overline{E}$ signal goes high, forcing the Q7(11) bit high and inhibiting the register from accepting data until the previous register is full and its Q_{CC} goes low. If only one register is used the $\overline{E}$ input should be held at a low logic level.

Short Cycle

If all bits are not required, the register may be truncated and conversion time saved by using a register output going low rather than the Q_{CC} signal to indicate the end of conversion. If the register is truncated and operated in the continuous conversion mode, a lock-up condition may occur on power turn-on. This condition can be avoided by making the start input the OR function of Q_{CC} and the appropriate register output.

Comparator Bias

To minimize the digital error below ±1/2 LSB, the comparator must be biased. If a D/A converter is used which requires a low voltage level to turn on, the comparator should be biased +1/2 LSB. If the D/A converter requires a high logic level to turn on, the comparator must be biased −1/2 LSB.

Definition of Terms

CP: The clock input of the register.

D: The serial data input of the register.

D0: The serial data out. (The D input delayed one bit).

$\overline{E}$: The register enable. This input is used to expand the length of the register and when high forces the Q7(11) register output high and inhibits conversion. When not used for expansion the enable is held at a low logic level (ground).

Q_I I = 7(11) to 0: The outputs of the register.

Q_{CC}: The conversion complete output. This output remains high during a conversion and goes low when a conversion is complete.

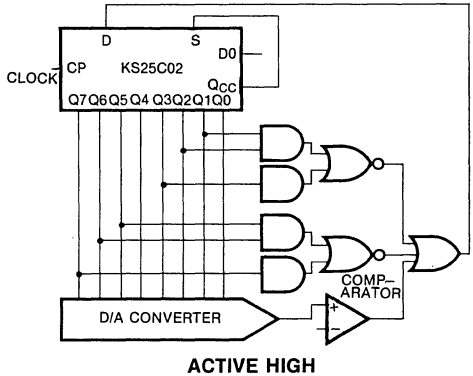
Q7(11): The true output of the MSB of the register.

$\overline{Q7}$(11): The complement output of the MSB of the register.

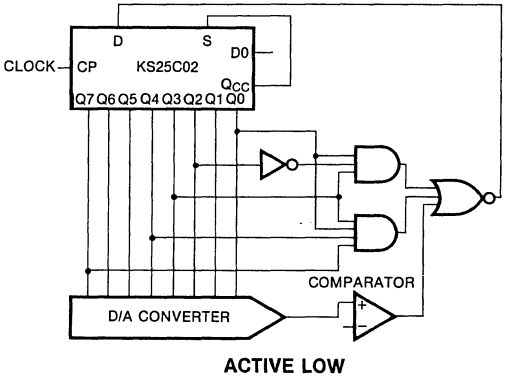
$\overline{S}$: The start input. If the start input is held low for at least a clock period the register will be reset to Q7(11) low and all the remaining outputs high. A start pulse that is low for a shorter period of time can be used if it meets the set-up time requirements of the S input.

TYPICAL APPLICATIONS

BCD ILLEGAL CODE SUPPRESSION

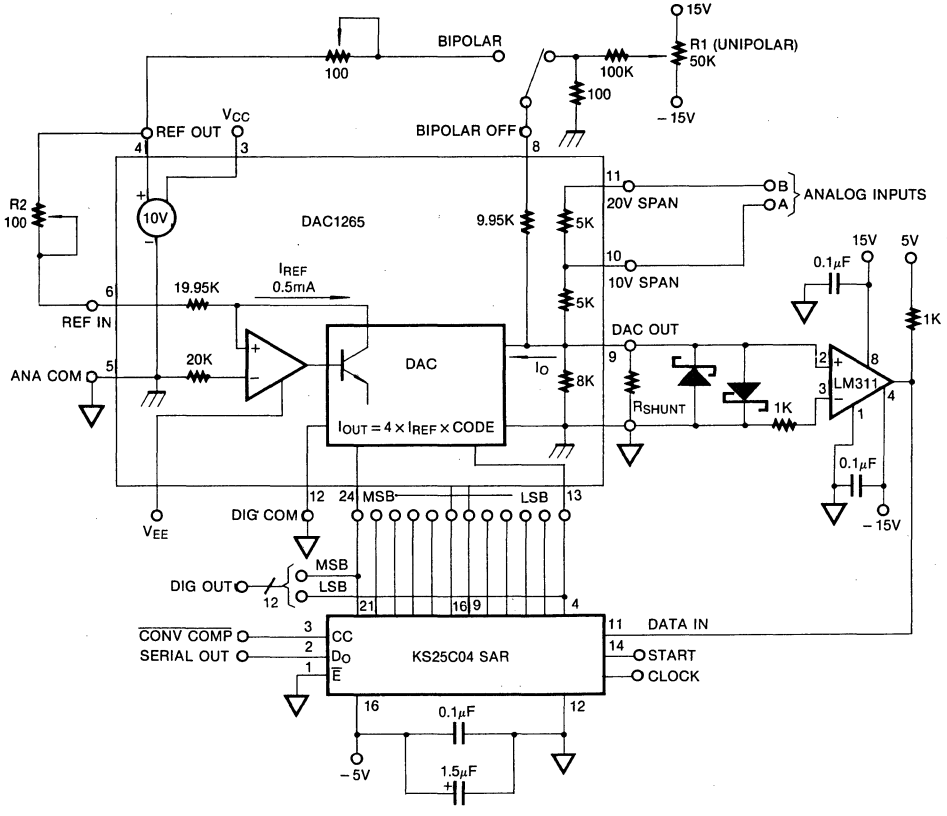


ACTIVE HIGH



ACTIVE LOW

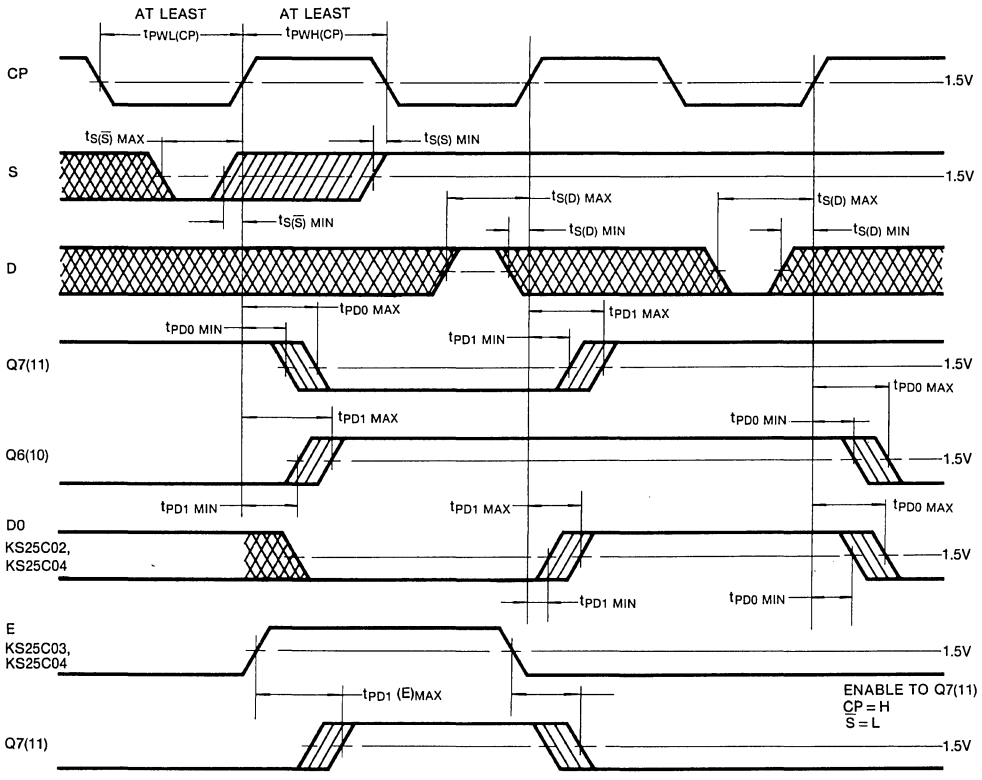
FAST PRECISION A/D CONVERTER



INPUT RANGES

UNIPOLAR	BIPOLAR	CONNECT	EQUIV. DAC Z_{OUT}
0 to 10	±5	Input to A	2.36KΩ
0 to 5	±2.5	Input to A	1.90KΩ
0 to 20	±10	Input to B B to DAC OUT	3.08KΩ

SWITCHING TIME WAVEFORMS



WAVEFORMS	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from H to L	Will be changing from H to L
	May change from L to H	Will be changing from L to H
	Don't care: any change permitted	Changing: state unknown

NOTES

APPLICATION NOTE 5

1. A/D, D/A Converter
2. KSV3110, KSV3208
3. KSV3110 DEMO Board
4. Digital Filter

INTRODUCTION TO SAMPLING THEOREM

1. Preface

Under certain conditions a continuous-time (Analog) signal can be completely represented by and recoverable from knowledge of its instantaneous values or samples equally spaced in time. This theorem is extremely important and useful. It is exploited, for example, in moving pictures, which consist of a time sequence of individual frames, each of which refresents an instantaneous view (i.e., a time sample) of a continuously changing scene. Much of the importance of the sampling theorem also lies in its role as a bridge between continuous-time (Analog) signal and discrete-time (Digital) signals. As we develop in some detail, the ability under certain conditions to completely represent an analog signal by a sequence of instantaneous samples provides a mechanism for representing an analog signal by a digital signal. In many contexts, processing of digital signals is more flexible and is often preferable to processing analog signals. This technology (i.e., analog-to-digital and digital-to-analog convereter) also offers the possibility of exploiting the concept of sampling to convert a continuous-time signal to a discrete-time signal. After processing the discrete-time signal using a digital system, we can then convert back to continuous time.

2. An Introduction to the Sampling Theorem

The introduction of the sampling theorem by C.E.SHANNON in 1949 places restrictions on the frequency content of the time function signal, x(t), and can be simply stated as follows:

In order to recover the signal function x(t) exactly, it is necessary to sample x(t) at a rate greater than twice its highest frequency component.

Practically speaking for example, to sample an analog signal having a maximum frequency of 10KHz requires sampling at greater than 20KHz to preserve and recover the waveform exactly.

The consequences of sampling a signal at a rate below its highest frequency component results in a phenomenon known as aliasing. This concept results in a frequency mistakenly taking on the identity of an entirely different frequency when recovered. In an attempt to clarify this, envision the ideal sampler of Figure 1(a), with a sample period of T shown in(b), sampling the waveform x(t) are shown in (d) and can be defined as the sample set of the continuous function x(t). Note in Figure 1(e) that another frequency component, ap(t) can be found that has the same sample set of data points as xp(t) in (d). Because of this it is difficult to determine which frequency ap(t), is truly being observed. This effect is similar to that observed in western movies when watching the spoded wheels of a rapidly moving stagecoach rotate backwards at a slow rate. The effect is a result of each individual frame of film resembling a discrete stobed sampling operation flashing at a rate slightly faster than that of the rotating wheel. Each observed sample point or frame catches the spiked wheel slightly displaced from its previous position giving the effective appearance of a wheel rotating backwards. Again, aliasing is evidenced and in this example it becomes difficult to determine which is the true rotational frequency being observed. On the surface it is easily said that anti-aliasing designs can be achieved by sampling at a rate greater than twice the maximum frequency found within the signal to be sampled. In the real world, however, most signals contain the entire spectrum of frequency components: from the desired to those present in white noise.

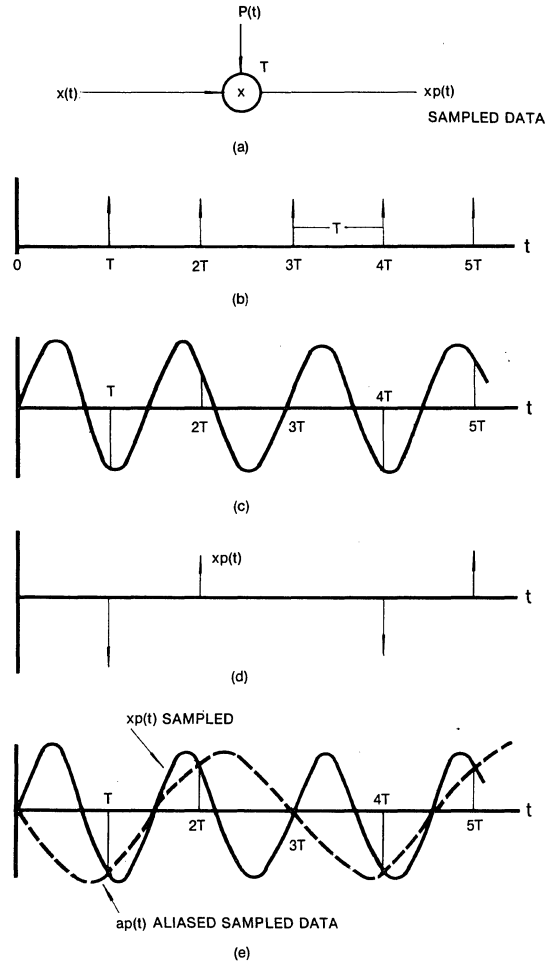


Fig. 1 When sampling, many signals may be found to have the same set of data points. These are called aliaes of each other.

To recover each information accurately the system would require an unrealizably high sample rate. This difficulty can be easily overcome by preconditioning the input signal, the means of which would be a band-limiting or frequency filtering function performed prior to the sample data input. The prefilter, typically called anti-aliasing filter guarantees, for example in the low pass filter case, that the sampled data system receives analog signals having a spectral content no greater then those frequencies allowed by the filter. As illustrated in Figure 2, it thus becomes a simple matter to sample at greater than twice the maximum frequency content of va given signal.

A parallel analog of band-limiting can be made to the world of perception when considering the spectrum of while light. It can be realized that the study of violet light wave-lengths generated from a white light source would be vastly simplified if initial band-limiting were performed through the use of a prism or white light filter.

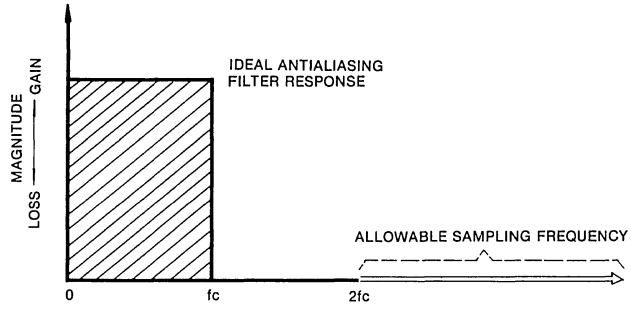


Fig. 2 Shown in the shaded area is an ideal, low pass, anti-aliasing filter responce.

5

3. The Sampling Theorem

In a manner identical to that used to analyze the more general case of pulse amplitude modulation, let us consider the specific case of impulse-train sampling depicted in Figure 1. The pulse train P(t) is referred to as the sampling function, the period T as the sampling period, and the fundamental frequency of P(t), Ws(t) = 2x/T, as the sampling frequency. In the time domain we have.

where $xp(t) = x(t)P(t)$

$P(t) =$ $(t - nT)$

xp(t) is an impulse train with the amplitudes of the impulses equal to the samples of x(t) at intervals spaced by T, that is,

$xp(t) =$ $\times (nT)$ $(t - nT)$

And in the frequency domain

$$Xp(W) = \frac{1}{2\pi}[X(W) * P(W)]$$

$$P(W) = \frac{2\pi}{T} \quad (W - kWs)$$

so that

$$Xp(W) = \frac{1}{T} \quad X(W - kWs)$$

That is, Xp(W) is a periodic function of frequency consisting of a sum of shifted replicas of X(W), scaled by 1/T as illustrated in figure 3. In figure 3(c), Wm<(Ws – Wm) or equivalently Ws>2Wm, and thus there is no overlap between the shifted replicas of X(W), whereas in figure 3(d) with Ws<2Wm, there is overlap.

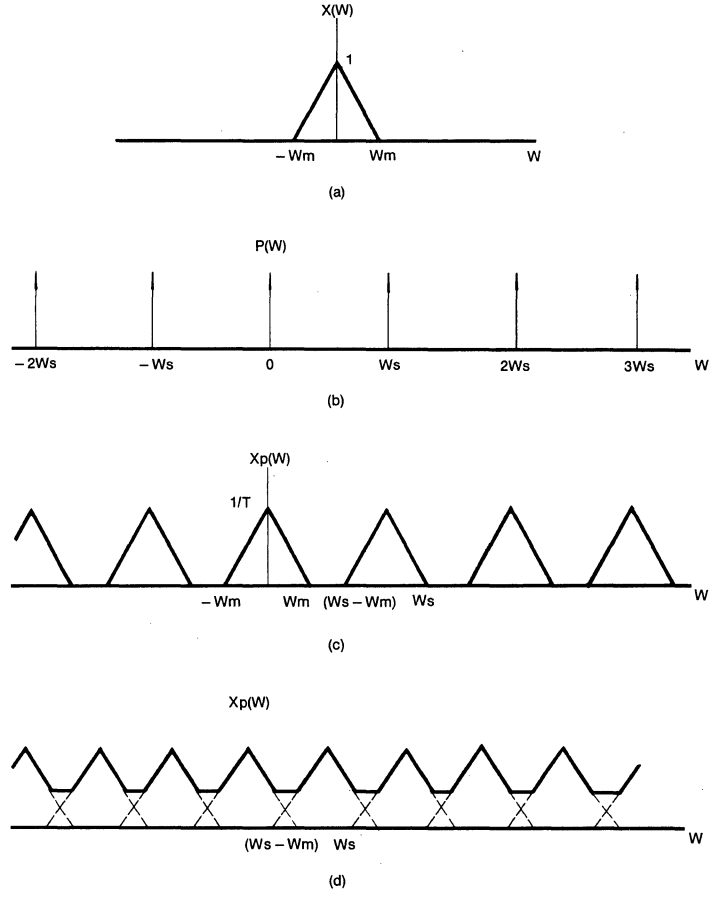


Fig 3. Effect in the frequency domain of sampling in the time domain:
(a) spectrum of original signal;
(b) spectrum of sampling function;
(c) spectrum of sampled signal with Ws>2Wm;
(d) spectrum of sampled signal with Ws<2Wm.

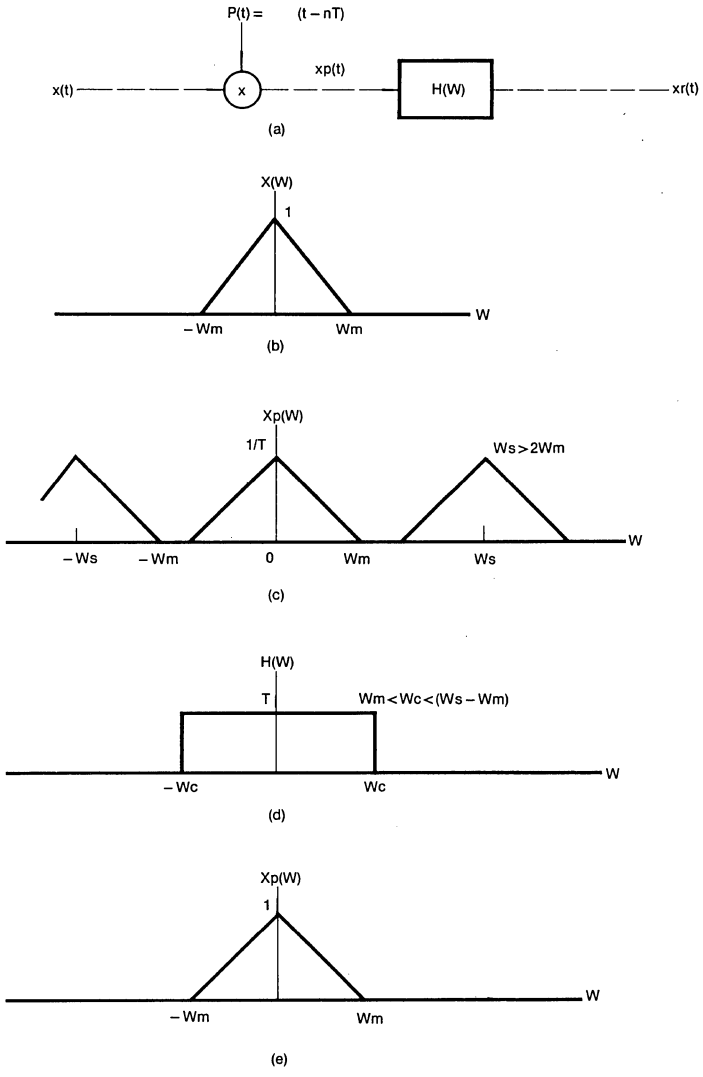


Fig. 4 Recovery of a original signal from its samples using an ideal lowpass-filter.

For the case illustrated in figure 3(c), X(W) is faithfully reproduced at integer multiples of the sampling frequency. Consequently, if Ws > 2Wm, x(t) can be recovered exactly from xp(t) by means of a lowpass filter with gain T and a cutoff frequency greater than Wm and less than (Ws – Wm), as indicated in Figure 4. This basic result, referred to as the sampling theorem, can be stated as follows:

Sampling Theorem:
Set x(t) be a bandlimited signal with $X(w) = 0$ for $|W| > Wm$. Then x(t) is uniquely determined by its samples x(nT), $n = 0, \pm 1, \pm 2, \ldots$ if

$$Ws > 2Wm$$

where

$$Ws = \frac{2\pi}{T}$$

Given these samples, we can reconstruct x(t) by generating a periodic impulse train in which successive impulses have amplitudes that are succissive sample values. This impulse train is then processed through an ideal lowpass filter with gain T and cutoff frequency greater than Wm and less than (Ws – Wm). The resulting output signal will exactly equal x(t).

The sampling frequency Wx is also referred to as the Nyquist frequency. The frequency 2Wm, which, under the sampling theorem, must be exceeded by the sampling frequency, is commonly referred to as the Nyquist rate.

3. The Sampling Theorem and Its Hardware Implications

Though there are numerous sophisticated techniques of implimintation, it is appropriate to re-emphasize that the intent of this article is to give the first time user a basic and fundamental approach toward the design of a sample data system. The method with which to achieve this goal will be to introduce a few of the common perils encountered when implementing such a system. We begin by considering the generalized block diagram of Figure 5.

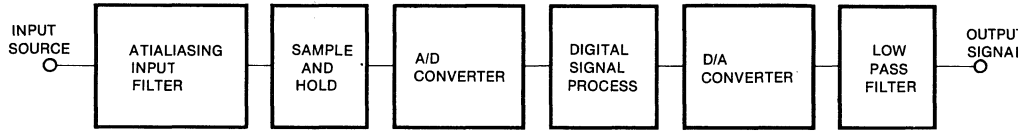


Fig. 5 Generalized single channel sample data system

As shown in Figure 5, prior to any signal processing manipulation the analog input signal must be preconditioned to prevent aliasing and thereafter digitized to logic signals usable by the logic function block. The antialiasing and digitizing functions are performed by an input filter and analog-to-digital converter respectively. Once digitized the signal can then be altered or processed and upon completion, reconstructed back to a continuous analog signal via a digital-to-analog converter followed by a low-pass filter. To this point no mention has been made concerning the sample and hold circuit block depicted in Figure 5. In general the analog-to-digital converter can operate as a stand alone unit. In many high speed operations however, the converter speed is insufficient and thus requires the assist detail further in the article.

A. The Antialiasing Input Filter

As indicated earlier in the text, the antialiasing filter should bond-limit the input signal's spectrum to frequencies no greater than the Nyquist frequency. In the real world however, filters are non-ideal and have typical attenuation or band-limiting and phase characteristics as shown in Figure 6. It must also be realized that true band-limiting of a specific frequency spectrum is not possible. In the sample data system band-limiting is achieved by attenuation those frequencies greater than the Nyquist frequency to a level undetectable or invisible to the system analog-to-digital (A/D) converter. This level would typically be less than the rms quantization noise level defined by the specific converter being used.

As an example of how an antialiasing filter would be applied, assume a sample data system having within it an 8-bit A/D converter. Eight bits translates to $2^n = 2^8 = 256$ levels of resolution. If a 2.56 volt reference were used each quantization level, Q, would represent the equivalent of 2.56 volts/256 = 10 millivolts. Realizing this the antialiasing filter would be designed such that frequencies in the stopband were attenuated to less than the rms quantization noise level of $Q/2\sqrt{3}$ and thus appearing invisible to the system.
More specifically

$$-20 \log 10\frac{V \text{ full scale}}{Vq/2\sqrt{3}} = -59dB = Amin$$

It can be seen, for example in the Butterworth filter case (characterized as having a maximally flat pass-band) of Figure 7(a) that any order of filter may be used to achieve the 59dB attenuation level, however, the higher the order, the faster the roll off rate and the closer the filter magnitude response will approach the ideal. Referring back to Figure 5 it is observed that those frequencies greater than Wa are not recognized by the A/D converter and thus the sampling frequency of the sample data system would be defined as $Ws \leq 2Wm$. Additionally, the frequencies present within the filtered input signal would be those less than Wa. Note however, that the portion of the signal frequencies least distorted are those between W = 0 and Wp and those within the transition are distorted to a substantial degree, though it was originally desired to limit the signal to frequencies less than the cutoff Wp, because of the non-ideal frequency response the true Nyquist frequency occurred at Wa. We see then that the sample data system could at most be accurate for those frequencies within the antialiasing filter pass-band.

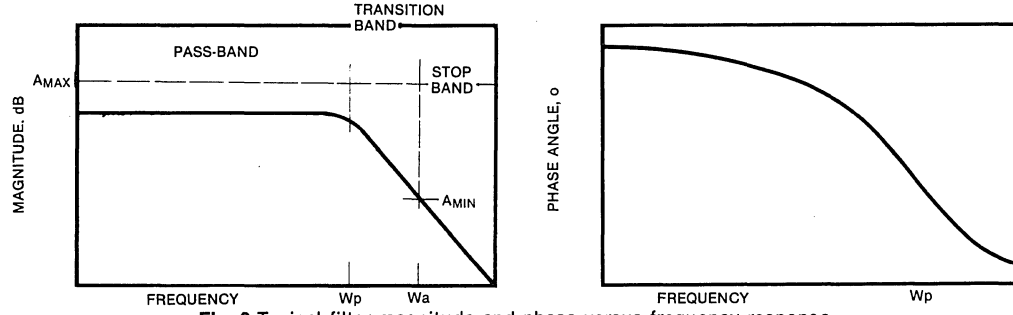
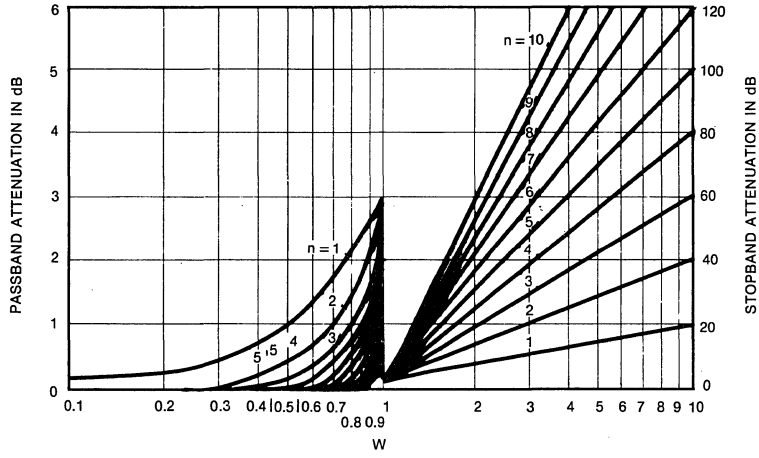


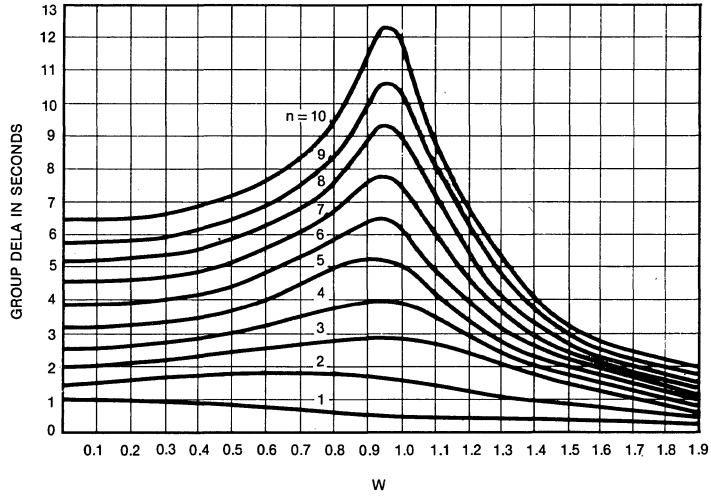
Fig. 6 Typical filter magnitude and phase versus frequency response

From the above example, the design of an antialiasing filter appears to be quite straight formward. Recall however, that all waveforms are composed of the sums and differences of various frequency components and as a result, if the response of the filter pass-band were not flat for the desired signal frequency spectra, the recovered signal would be an inaccurate summation of all frequency components altered by their relative attenuations in the pass-band. Additionally the antialiasing filter design should not neglect the effects of delay. As illustrated in Figure 6, and 7(b), delay time corresponds to a specific phase shift at a particular frequenct. Similar to the flat pass-band consideration, if the phase shift of the filter is not exactly proportional to the frequency, the output of the filter will be a waveform in which the summation of all frequency components has been altered by shifts in their relative phase. Figure 7(b) further indicates that contrart to the roll off rate, the higher the filter order the more non-ideal the delay becomes (increased delay) and the result being a distorted output signal. When designing antialiasing filters it will be found that the closer the filter response approaches the ideal the more complex the filter becomes.

Along with this an increase in delay and pass-band ripple combine to distort and alias the input signal. In the final analysis the design will involve trade offs made between filter complexity, sampling speed and thus system bandwidth.



(a) Attenuation characteristics of a normalized Butterworth filter as a function of degree n.



(b) Group delay performances of normalized Butterworse lowpass filter as a function of degree n.

B. The Analog-to-digital Converter

Following the antialiasing filter is the A/D converter which performs the operations of quantizing and coding the input signal in some finite amount of time. Figure 8 shows the quantization process of converting a continuous analog input signal into a set of discrete output levels. A quantization, Q, is thus defined as the smallest step used in the digital representation of xp(n) where x(n) is the sample set of an input signal x(t) and is expressed by a finite number of bits giving the sequence xp(n). Digitally speaking Q is the value of shown in Figure 8 is called quantization noise or error and can be defined as $e(n) = x(n) - xp(n)$. This error is an irreducible one and is a function of the quantizing process. Its error amplitude is dependent on the number of quantization levels or quantizer resolution and as shown, the maximum quantization is Q/2. Generally e(n) is treated as a random error when described in terms of its prohability density function, that is, all values of e(n) between Q/2 and $-Q/2$ are equally probable, then for the average value $e(n)avg = 0$ and for the rms value $e(n)rms = Q/2\sqrt{3}$.

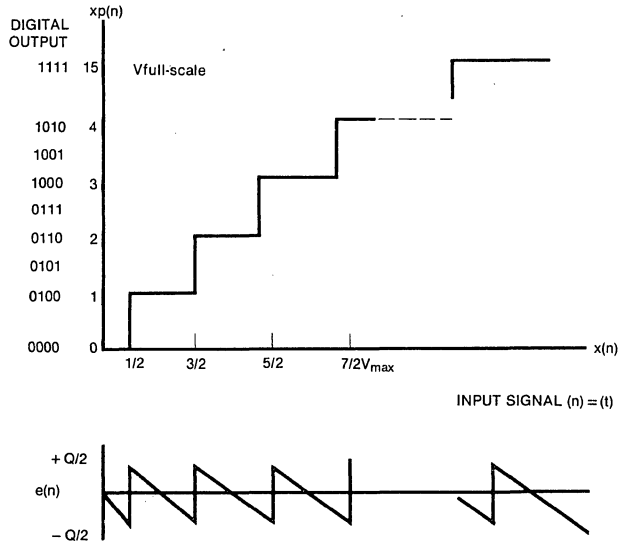


Fig. 8 Quantization characteristics.

As a side note it is appropriate at this point to emphasize that all analog signals have some form of noise corruption. If for example an input signal has a finite signal-to-noise ratio of 40dB it would be superfluous to select an A/D converter with a high number of bits. It may be realized that the use of a large number of bits does not give the digitized signal a higher signal-to-noise ratio than that of the original analog input signal. As a supportive argument one may say that though the quantization steps Q are very small with respect to the peak input signal the lower order bits of the A/D converter merely provide a more accurate representation of the noise inherent in the analog input signal. Returning to our discussion, we define the conversion time as the time taken by the A/D converter to convert the analog input signal to its equivalent quantization or digital code. The conversion speed required in any particular application depends upon the time variation of the signal to be converted and the amount of resolution or bits, n, required. Though the antialiasing filter helps to control the input signal time rate of change by band-limition its frequency spectrum, a finite amount of time is still required to make a measurement or conversion. This time is henerally called the aperture time and as illustrated in Figure 9 porduces amplitude measurement uncertainty errors.

The maximum rate of change detectable by an A/D converter can simply be stated as

$$\left.\frac{dv}{dt}\right|_{\substack{\text{maximum resolvable}\\ \text{rate of change}}} = \frac{\text{V full scale}}{2^n\text{T conversion time}}$$

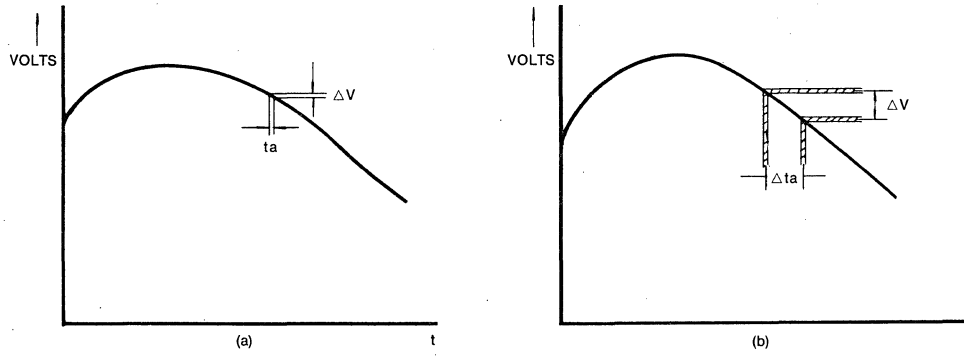


Fig. 9 Amplitude uncertainty as a function of
(a) a nonvarying aperture and
(b) aperture time uncertainty.

If for example V full scale = 10.24 volts, T conversion time = 10ms, and n = 10 or 1024 bits of resolution then the maximum rate of change resolvable by the A/D converter would be Q volt/sec. If the input signal has a faster rate of change than 1 volt/sec, 1 LSB changes cannot be resolved within the sampling period.

In many instances a sample-and-hold circuit may be used to reduce the amplitude uncertainty error by measuring the input signal with the smaller aperture time than the conversion time aperture of the A/D converter. In this case the maximum rate of change resolvable by the sample-and-hold would be

$$\left.\frac{dv}{dt}\right|_{\substack{\text{maximum resolvable}\\ \text{rate of change}}} = \frac{\text{V full scale}}{\text{t aperture}}$$

Note also that the actual calculated rate of change may be limited by the slew rate specification to the sample-and-hold in the track mode. Additionally it is very important to clarify that this does not imply vioating the sampling theorem instead of the increased ability to more accurately sample signals having a fast time rate of change. An ideal sample-and-hold effectively takes a sample in zero time and with perfact accuracy holds the value of the sample indefinitely. This type of sampler is also known as a zero-order hold circuit and its effect on a sample data system warrants some discussion. It is appropriate to recall the earlier discussion that the spectrum of a sampled

signal is one in which the resultant spectrum is the product obtain by convolving the input signal spectrum with the Sin(X)/X spectrum of the sampling waveform. Figure 10 illustrates the frequency spectrum plotted from the Fourier transform

$$F(W) = AT\frac{Sin\ (WT/2)}{WT/2}$$

of a rectangular pulse. The Sin(X)/X form occurs frequently in modern communication theory and is commonly called the sampling function.

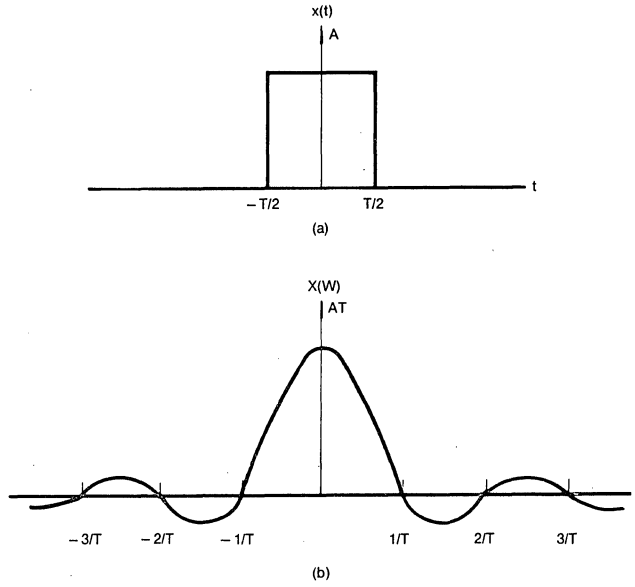


Fig. 10 The Fourier transform of the rectangular pulse (a) is shown in (b).

The magnitude and phase of a typical zero order hold sampler spectrum

$$H(W) = A[\ \frac{Sin(W\ \ )}{W} + j\frac{1}{W}(Cos(W) - 1)]$$

is shown in Figure 11 and Figure 12 illustrates the spectrums of various sampler pulse-widths.

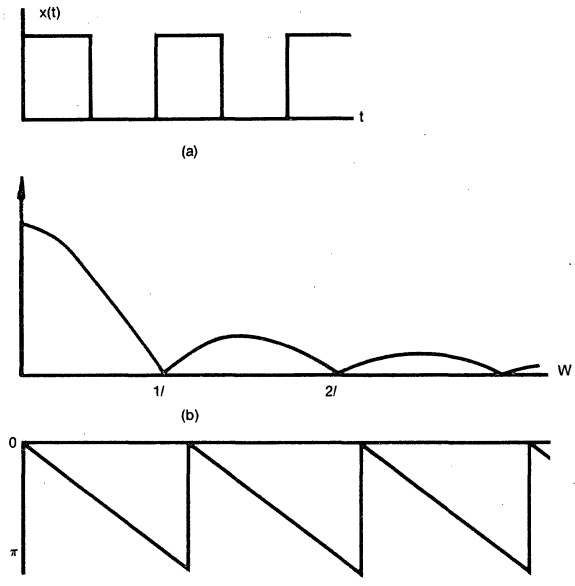
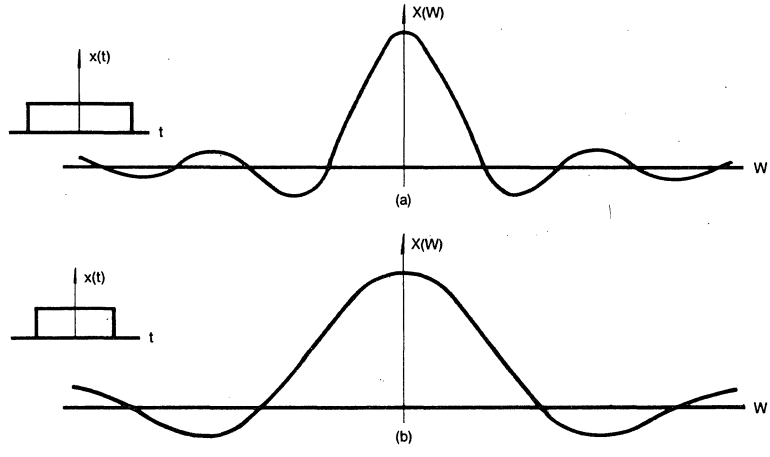


Fig. 11 (b) Magnitude and (c) phase frequency response of the sampling pulse (a).

From Figure 12 it is realized that the main lobe of the Sin(X)/X function varies inversely proportional with the sampler pulse-width. In other words a side pulse-width, or in this case the aperture window, acts as a low pass filtering function and limits the amount of information resolvable by the sample data system. On the other hand a narrow sampler pulse-width or aperture window has a broader main lobe or band-width and thus when convolved with the analog input signal produces the least amount of distortion.

Understandably then the effect of the sampler's spectral phase and main lobe width must be considered when developing a sampling system so that no unexpected aliasing occurs from its convolution with the input signal spectrum.



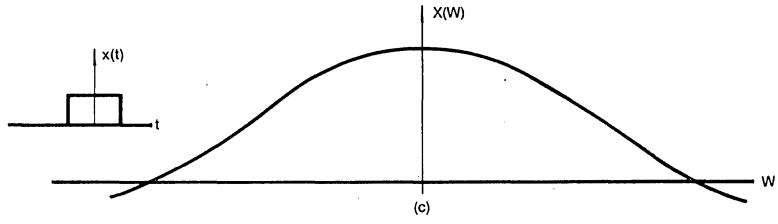
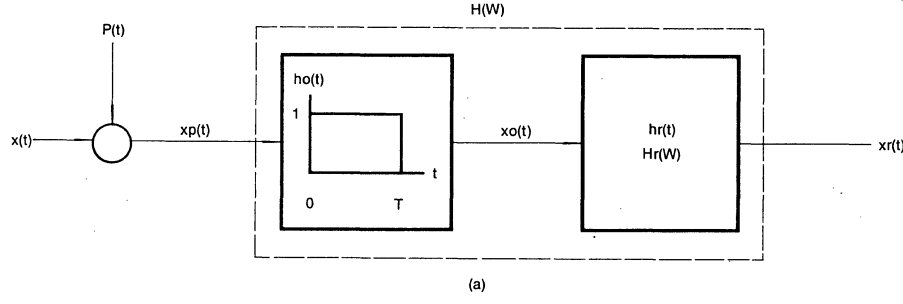


Fig. 12 Pulse width and how it effects the Sin(X)/X envelop spectrum (normalized amplitudes).

C. The Digital-to-Analog Converter and Lowpass Filter

The sampling theorem establishes the fact that a bandlimited signal is uniquely represented by its samples, and is motivated on the basis of impulse-train sampling. After a signal has been digitally conditioned by the signal processing unit of Figure 5, a D/A converter is used to convert the sampled binary information back in to an analog signal. The conversion is called a zero-order hold type where each output sample level is a function of its binary weight value and is held until the next sample arrives, see Figure 13. As a result of the D/A converter step function response it is apparent that a large amount of undesirable high frequency energy is present. Reconstruction of x(t) from the output of D/A converter is usually followed by lowpass filter, having a cutoff frequency no greater than half the sampling frequency. As its name suggests the filter output produces a smoothed version of the D/A converter output which is fact is a convolved function. In Figure 13(a), to reconstruct x(t) from xo(t), we consider processing xo(t) with impulse response h(t) and frequency response Hr(W). The cascade of this system with the Figure 13, where we wish to specify Hr(W) so that xr(t) = x(t). Comparing the system in Figure 13(a) with that in Figure 4(a), we see that xr(t) = x(t) if the cascade combination of ho(t) and hr(t) is the ideal lowpass filter H(W) used in Figure 4. More simply said, the spectrum of the resultion signal is the product of a step function Sin(X)/X spectrum and the band-limited analog filter spectrum. Analogous to the input sampling problem, the smoothed output may have aliasing effects resulting from the phase and attenuation relations of the signal recovery system (defined as the D/A converter and lowpass filter combination). As a final note, the attenuation due to the D/A converter Sin(X)/X spectrum shape may in some cases be compensated for in the signal processing unit by pre-processing using a digital filter with an inverse response X/Sin(X) prior to D/A conversion. This allows an overall flat magnitude signal response to be smoothed by the final filter.



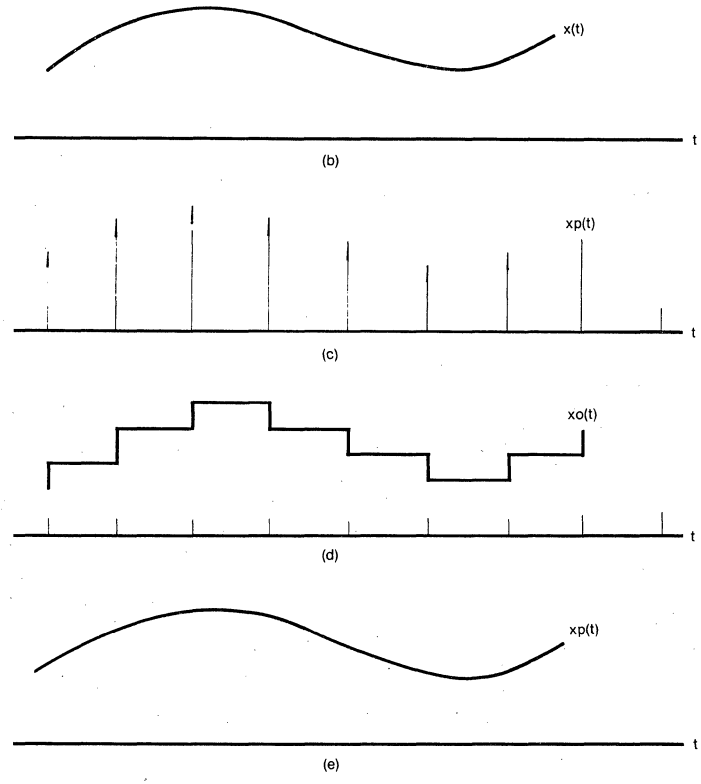


Fig. 13 (a) Casade of the representation of a zero-order hold
(b) Original input signal
(c) Processed signal points
(d) Output of D/A converter
(e) reconstruction signal

4. Summary

In this article we have developed the concept of sampling, whereby a analog or digital signal is represented by a sequence of equally spaced samples. The conditions under which the signal is exactly recoverable from the samples is embodied in the sampling theorem. This theorem requires, for exact reconstruction, that the signal to be sampled be band-limited and that the sampling frequency be greater than twice the highest frequency in the signal to be sampled. Under these conditions reconstruction of the original signal is carried out by means of ideal low-pass filtering. If a signal is undersampled (i.e. the sampling frequency is less than that required by the sampling theorem), then the signal reconstructed by ideal bandlimited interpolation will be related to the original signal through a form of distortion referred to as aliasing. In many instances it is important to choose the sampling rate to avoid aliasing. The purpose of presenting these thought providing perils was perhaps give the beginning designer some insight or guidelines for consideration when developing a sample data system's interface.

GENERAL DESCRIPTION

Digitizing analog signals containing high frequency components with accuracy requires ultrahigh speed A/D converters. Such converter is essential in RADAR data transmission, high speed digital data transmission, image processing and digital television. In TV for example, high speed conversion will enhance images, correct time base errors, synchronize and store frames, and reduce noise. Analog-to-digital and digital-to-analog converters also play an important role in the field of microcomputers when they are used in control and measurement applications.

All these applications require much faster data conversion technique and one such technique is called flash conversion (or parallel conversion) technique.

The flash converter offers very high performance and has an ability to perform data conversions (from analog to digital or vice versa) at extremely high speed. The crucial parts in this type of converters are comparators. They not only determine the speed of the converter but also the accuracy. Also, the switches must be very fast and be able to withstand the reference voltage. Generally, the number of comparators in an n-bit converter will be $2^n - 1$. In flash conversion, the analog input is compared against 2^n graded voltage levels, using the same number of comparators (shown in figure 1). The comparator output logic levels are processed by a priority encoder, which converts the output to a binary code. The whole conversion occurs simultaneously, so it is the fastest means of conversion, however, it requires a large number of comparators having very high accuracy and a large number of gates.

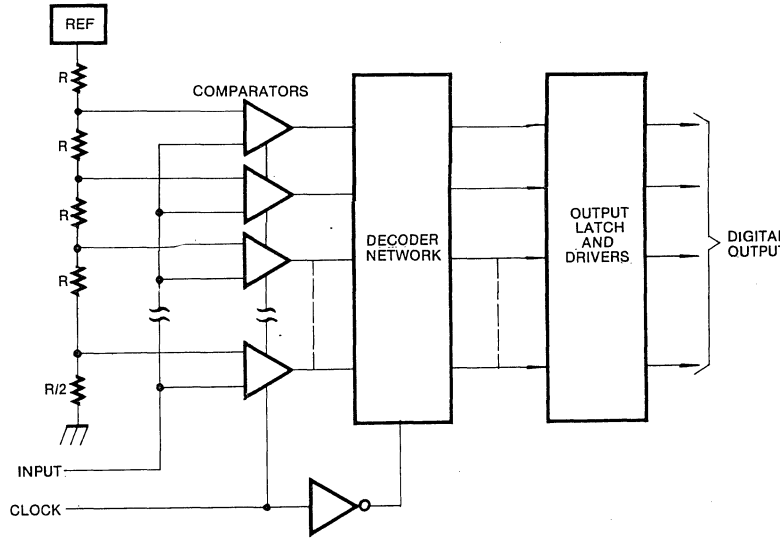


Fig. 1 Flash (Parallel) A/D Converter

Like other converters, parallel type of A/D converter also contains a quantizer circuit followed by a decoder circuit, but the difference is that both functions are separate in this type of converter. The quantizer in such A/D converters is defined by its parallel function. Figure 2 shows the transfer function for a 4-bit parallel type of converter. The output in this figure is divided into 16 different states or 2^n levels, where n is the number of bits. There are $2^n - 1$ analog transition points along the horizontal axis representing voltage levels that define the edges between adjacent output stages or codes. These are also called analog decision points. These decision points are set precisely in a quantizer in order to divide the analog voltage range into the correct quantized values.

The quantizer in this case assigns one output code to a small range or band of analog input values. The size of such band is a quantum Q which is given by:

$$Q = \frac{FSR}{2^n} \qquad \text{where FSR} = \text{Full Scale Analog Range}, \quad n = \text{number of bits}$$

In figure x, the full-scale-range is 2.0 volts, therefore:

$$Q = \frac{2.0}{2^4} = \frac{2.0}{16} = 0.125\text{mV}$$

The voltages 0.125, 0.25, 0.375, 0.5, 0.625, 0.75, and 0.825, are the center points of each output code generated by the A/D converter (shown in figure 2).

The transfer function shown in figure 2, is of an ideal quantizer of an A/AD converter, however, in practice, the A/D converter will have errors like offset or linearity for example. (see App. Note on "Glossary of Data Conversion").

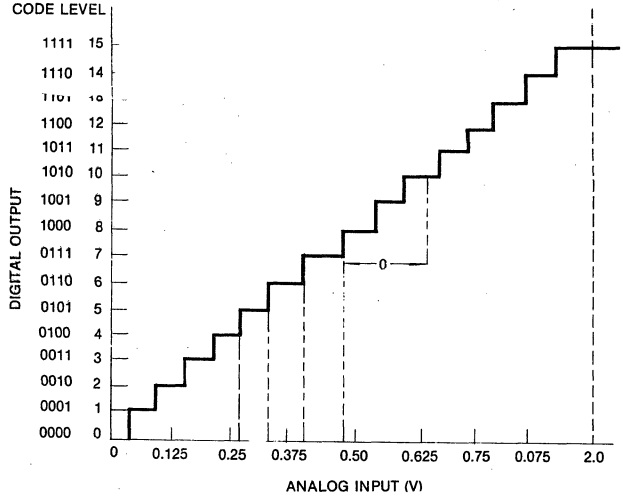


Fig. 2 The Quantizer Transfer Function for a 4-Bit Parallel A/D Converter

KSV3110 Flash A/D and D/A Converter on a Single Chip

The KSV3110 is a VLSI circuit designed using Samsung's CI (Collector Implanted) technology. It consists of a high-speed flash-type 8-bit A/D converter and a high-speed 10-bit low glitch D/A converter. Also, various auxiliary circuits like, reference voltage generator, pre-amplifier, and input clamping circuit are integrated on the same chip (Figure 3).

The KSV3110 has been developed for all applications involving high-speed data conversion. The KSV3110 is very useful for industrial applications in conjunction with image processing. It is also used for decoding Television signals in Pay-TV converters or MAC converters used for direct satellite broadcasting.

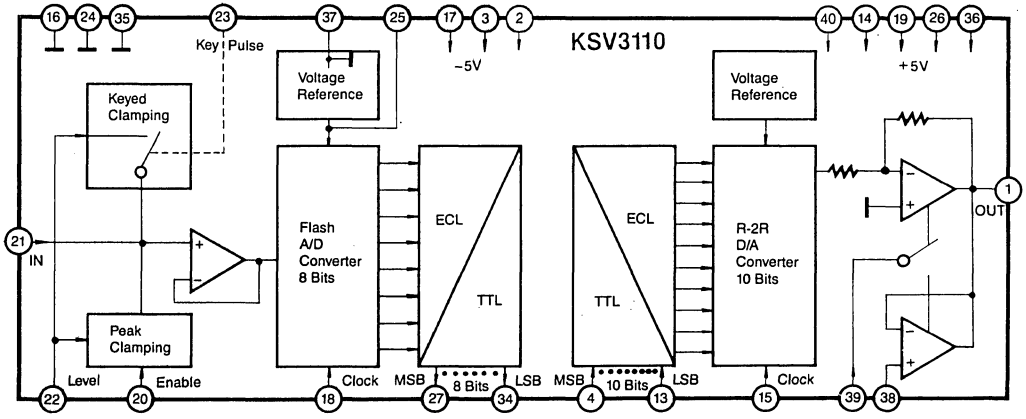


Fig. 3 KSV3110 Block Diagram

The on-chip A/D converter has an accuracy of 8-bits, but the on-chip D/A converter is available with an accuracy of either 7, 8, 9 or 10-bits. The KSV3110 comes in a 40-pin DIP plastic package.

In many applications, only A/D converter is required. The KSV3208 from Samsung contains a flash A/D converter for those who do not require D/A converter in their systems. Essentially, the KSV3208 contains the A/D converter section of the KSV3110.

KSV3208 Flash A/D Converter

The KSV3208, is a VLSI circuit similar to the KSV3110, designed using the same CI (Collector Implanted) technology. Like KSV3110, the KSV3208 also contains various auxiliary circuits such as; reference voltage generator, pre-amplifier, and input clamping circuit (Figure 4).

The KSV3208 has been developed for use in all applications requiring high-speed A/D converter. The applications involve low-cost video digitizing. Radar data conversion, data acquisition and medical imaging. Other promising applications are in the field of industrial electronics, in conjunction with image processing.

The reference voltage for A/D converter of the KSV3110 and KSV3208 is generated internally, but this voltage with the ground for the reference voltage circuitry are connected to the pins so that an external filter capacitor can be used. All inputs and outputs of these devices are TTL compatible.

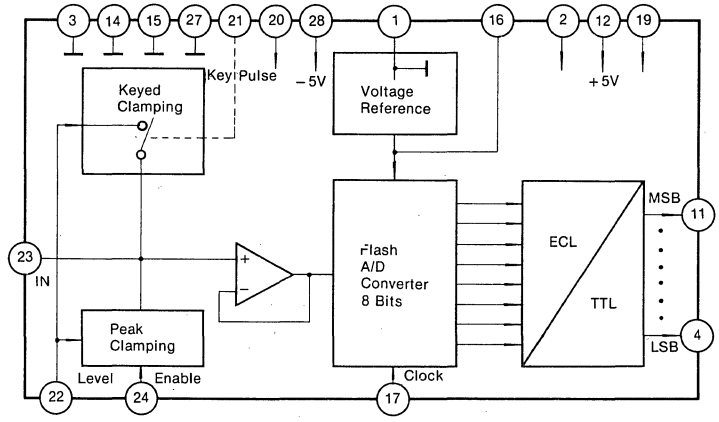


Fig. 4 KSV3208 Block Diagram

FUNCTIONAL DESCRIPTION

A/D Converter

The A/D converter on the KSV3110 and KSV3208 contains the following basic functions:

Analog section
Digital section
Data output section and
Auxiliary section

Analog Section

The analog section consists of the comparator array, reference resistor string and voltage reference. The input voltage to the A/D is compared with 2^n separate reference voltage points by a voltage equivalent to one LSB where n is the number of data outputs, or the resolution of A/D converter in bits.

The comparator reference voltage points are tapped from the reference resistor string which is driven by a voltage reference circuit.

Digital Section

In this section, the output from the 2^n comparators is encoded into an n-bit binary word for high speed operation. The emitter coupled logic (ECL) is used for encoding. The encoded n-bit data is latched in the output data latches.

Data Output Section

This section consists of output data latch, and logic level converter (e.g. ECL-to-TTL). The output latches of the converter hold data valid while the conversion is taking place. These latches are updated by the sampling clock signal.

The latched outputs of the ECL logic are converted into TTL level by the ECL-to-TTL logic converter circuit, so the outputs can easily interface with the external TTL devices.

Auxiliary Section

The auxiliary section contains the voltage reference circuit, pre-amplifier as buffer, and clamping circuit for peak or keyed clamping. All these functions will help reduce the size of the external components thereby reducing the overall system costs. Also, they will provide more stable features because of the identical characteristics.

Reference Voltage Generator

The reference voltage generator will operate from 2.0 Volts supply. The reference voltage generator is designed using the bandgap reference circuit, that will provide higher accuracy for the temperature coefficient characteristic.

Pre-amplifier

The input impedance of the A/D converter is 10 MOhms at the input frequency of 1 KHz and 100 KOhms at the input frequency of 10 MHz. In many instances, for using an A/D converter in a system, it becomes necessary to match the impedance of an external circuitry to the input impedance of the converter. The on-chip pre-amplifier on the KSV3110 and KSV3208 will take care of the impedance matching requirement. This pre-amplifier is used as a voltage follower (unity gain amplifier) so that it will not affect the gain of an input signal.

Clamping Circuit

The purpose of this clamping circuit is to provide an appropriate signal levels for the input of the A/D converter (see figure 5). The two basic methods for using this section are:

1. Peak clamping and
2. Keyed clamping

Peak Clamping

The amplitude of an analog signal for A/D converter should be 0V to 2 Volts. In several applications, the analog signal consists of different amplitude levels. It is necessary to shift the amplitude of such signal to match the input conditions required by the A/D converter. This signal conditioning can be achieved by the clamping circuit given in figure 6.

Keyed Clamping

This feature can be tailored by the user for clamping the analog input signal, according to the requirements. When using this method, the peak clamping function described above, must be disabled. The user can now provide key pulses to pin 23 of the KSV3110 and adjust the voltage levels of the analog input signal in correspondance with the key pulses shown in the figure?

If the amplitude of an analog signal is between 0V and 2 Volts, then the clamping is not required. In this case, the clamping circuit on KSV3110 should be disabled by connecting pins 22 and 23 to the ground and leaving pin 20 with no connection.

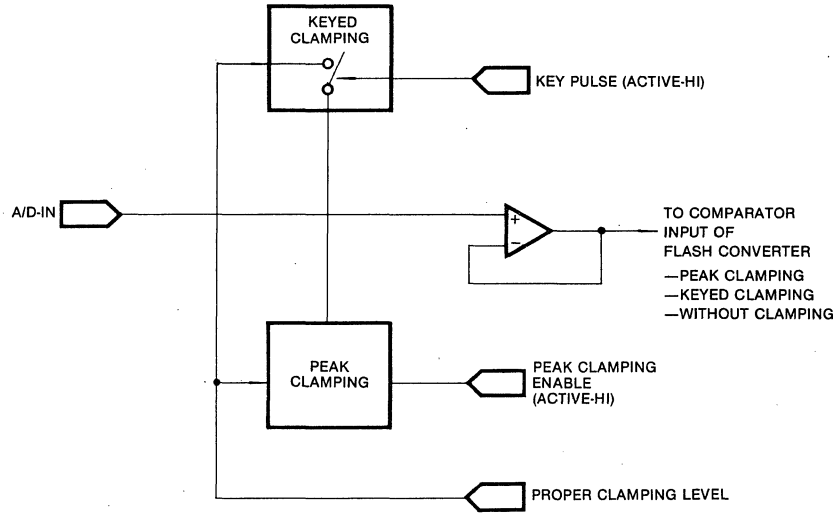
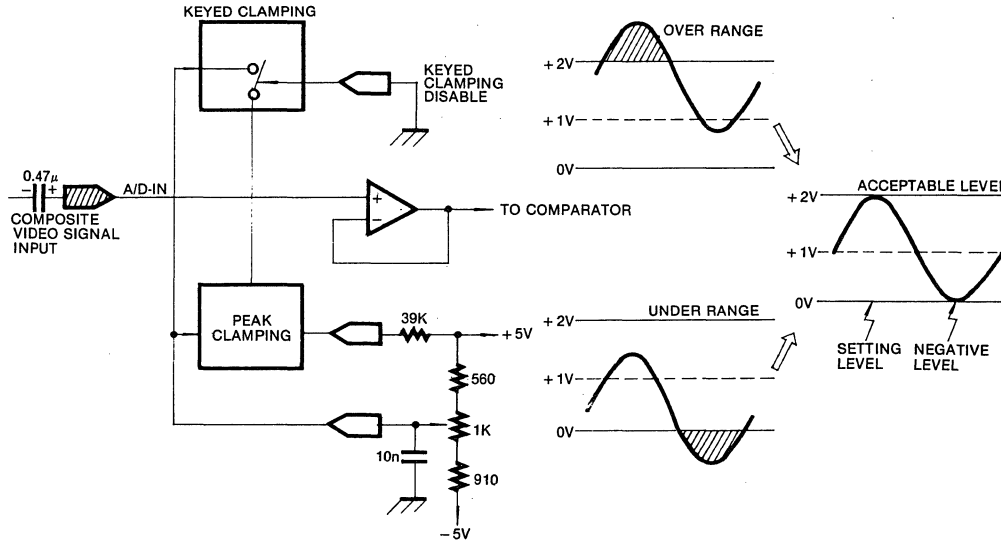


Fig. 5 KSV3208, KSV3110 Clamping Circuit for A/D Input



Input signal is clamped automatically to the negative peak value

Fig. 6 Operating with Peak Clamping

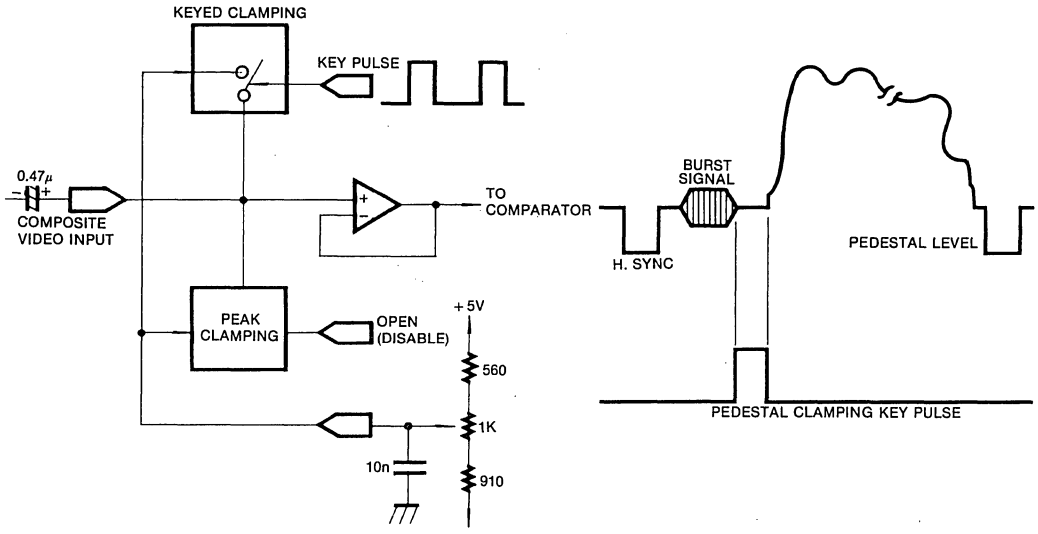


Fig. 7 Operating Keyed Clamping

D/A Converter

The D/A converter on the KSV3110 contains the following major function blocks:

- Data input section
- Decoding section
- Analog output section
- Output signal switchover circuit

Data Input Section

This section includes logic level converters, and data input register. The TTL data input to this section will be converted to the ECL logic level before entering into the register, since this register operates with the ECL voltage levels in order to obtain the desired conversion speed. The primary function of the input register is to hold the data constant during conversion. The register must assure precise matching of propagation delays to keep glitches to the minimum.

Decoding Section

The decoding section can be divided in two parts: first one generates very accurate currents and the second one causes these currents to be switches according to the contants of the input register. This section is the heart of the D/A converter and is called "switching network."

Analog Output Section

Normally, the output of the switching network is in the form of current which must to be converted into voltage for interfacing with the external world. A typical value of an output impedance for the D/A converter is 15 Ohms.

The output of the D/A section of KSV3110 contains who output op-amps, one of which is used to convert the output current into the output voltage. This amplifier has very low offset voltage and offset voltage drift, high slew rate and fast settling time. Also it requires very small bias current (which should be smaller than 1 LSB current).

Output Signal Switchover Circuit

The switchover circuit is unique to this product and is not found in other compatible products. The output switch over circuit consists of two amplifiers and an analog switch as shown in figure 8. They are designed to allow an external analog signal to be multiplexed with an internally converted analog signal which is an output of the D/A converter. When using this feature, the external analog signal should be supplied to pin 38. In this case, the output at pin 1 will be either of the two signals and the selection can be made by applying proper logic level to pin 39. A low on pin 39 will select the internally converted analog signal and a high on pin 39, will select the external signal (from pin 38) as an output at pin 1.

The advantage of this feature is obvious in video applications, where, the horizontal and vertical sync pulses are combined with a video signal to obtain the stabilized composite video signal as shown in figure 9. The slew rate of the amplifier for an external signal is 5.16 Volts/microsecond, when the frequency of the external input signal is 15.7 KHz, which is the frequency of the horizontal sync pulse.

The timing diagrams for the KSV3110 and KSV3208 are illustrated in figures 10 and 11.

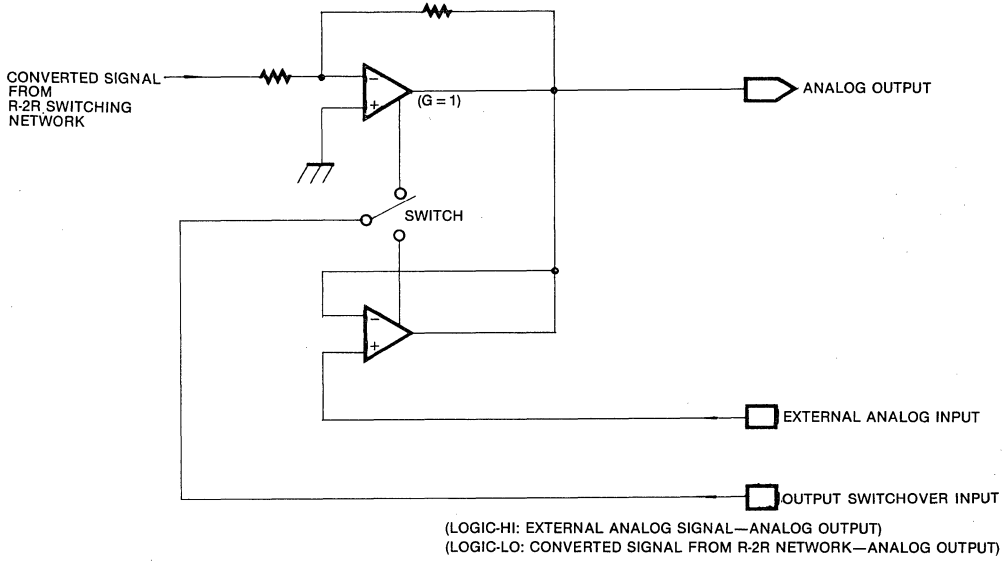
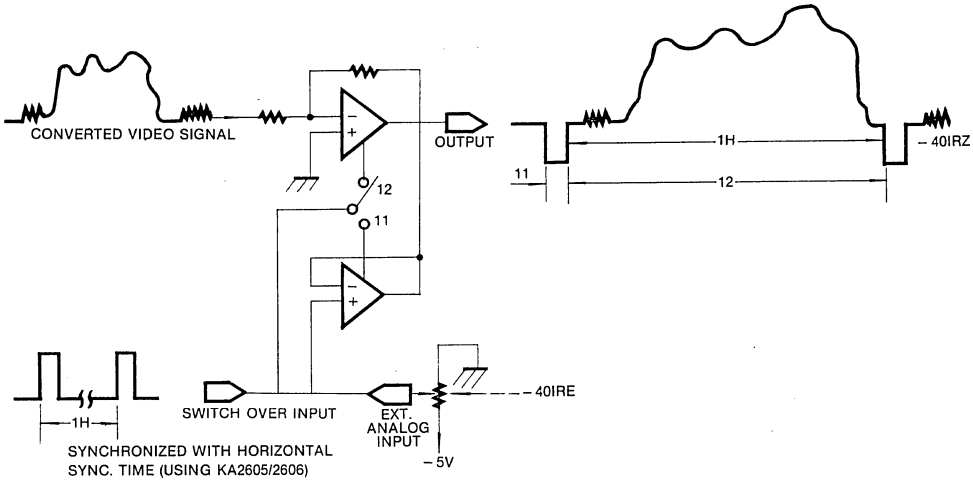
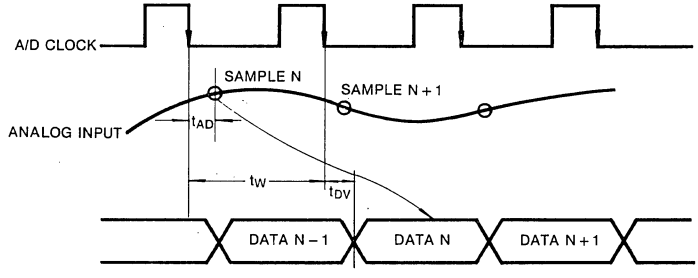


Fig. 8 KSV3110-DA Output Signal Switchover Circuit



Add horizontal sync. pulse of video signal to the converted composited signal; result is the stabilized sync. pulse

Fig. 9 Typical Application of Switchover Circuit



t_{AD}: APERTURE TIME
t_W: TRANSFET TIME A/D
t_{DV}: DIGITAL OUTPUT DELAY

Falling edge (negative) sampling
After 1 clock, negative triggering data out

3-stage latch is used in A/D section.

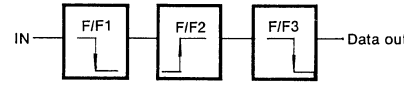


Fig. 10 KSV3208, KSV3110 Timing Diagram (A/D)

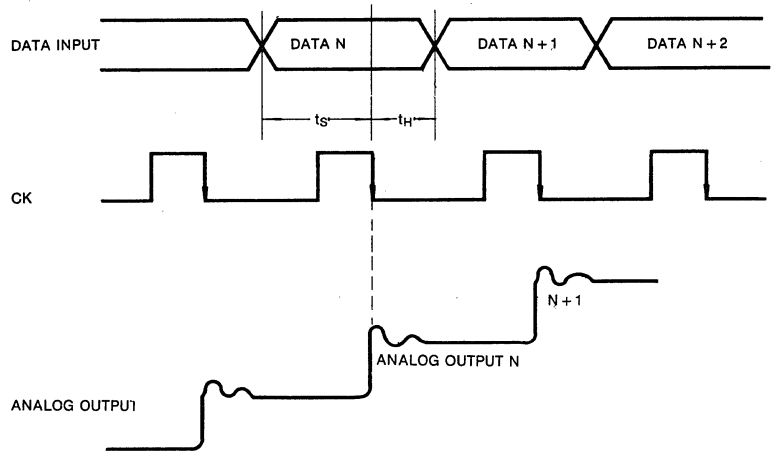
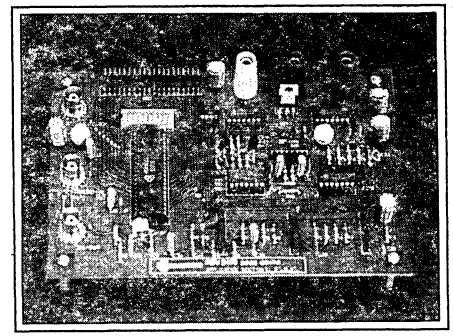


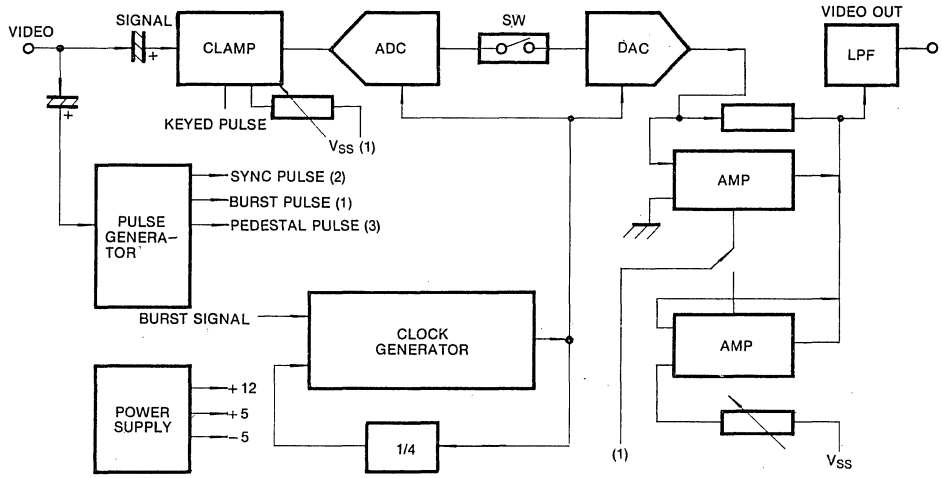
Fig. 11 KSV3110 Timing Diagram (D/A)

GENERAL DESCRIPTION

The KSV3110 Demo Board is intended to show the performance of KSV3110. It consists of a high speed low glitch 10-bit DAC and high speed flash 8-bit ADC with the various auxiliary circuits (reference voltage source, pre-amplifier, input clamping circuit and feed-in output amplifier).



BLOCK DIAGRAM



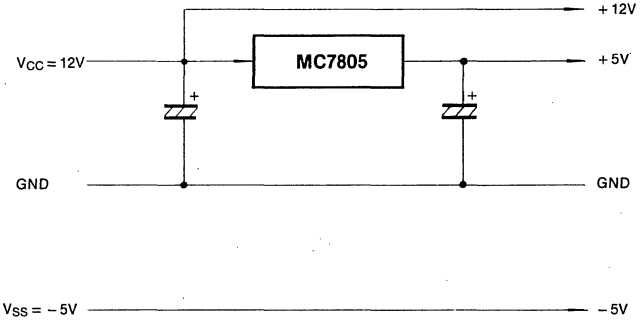
This demo board is a fully assembled and tested circuit board designed to aid the demonstration of KSV3110, 8 bit ADC and 10 bit DAC. The board contains circuitry for pulse generator, clock generator with KSV3110. The KSV3110 Demo Board consists of six functional sections, such as pulse generator, clock generator, clamp part, ADC, DAC, feed-in amp. The more detailed information is on the following pages.

BLOCK DESCRIPTION

1) Power Supply

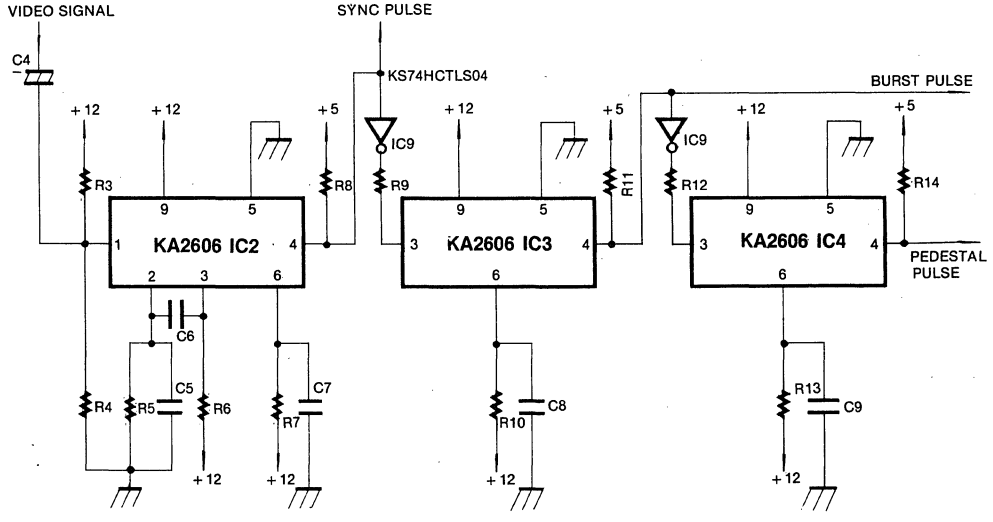
The board requires +12, +5 and −5 volt supplies. The +5 volt is made from MC7805. The +5 volt is supplied to the V_{CC} of KSV3110, XR210, and logic device. The +12 volt is supplied to the V_{CC} of KA2606 that makes several pulses. The −5 volt is supplied to the V_{SS} of KSV3110 and XR210.

The analog and digital ground in board should be separated and the analog and digital ground is separated in KSV3110 DVC. The digital ground, which is separated from analog ground, should be connected with ferrite core or coil for reducing the interference of each ground.

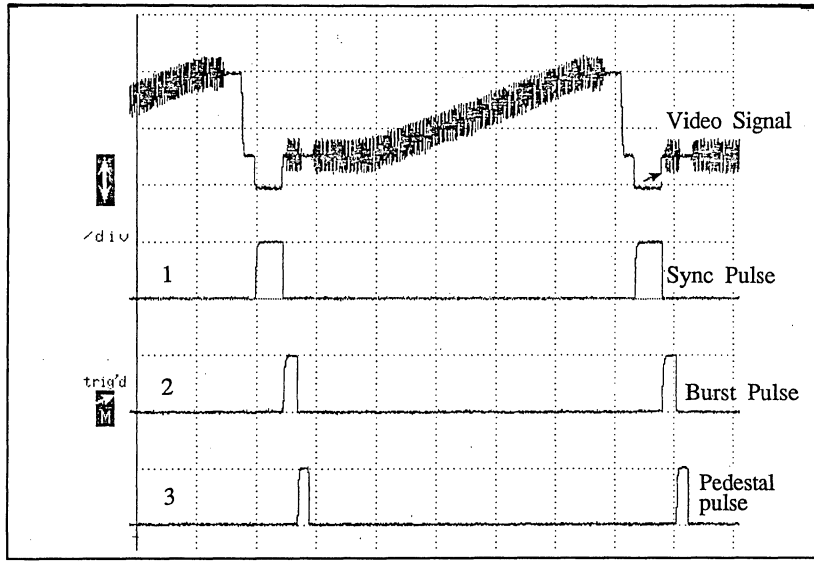


2) Pulse Generator

The pulse generator generates the several pulses—sync pulse, burst pulse, pedestal pulse—from the composite video signal. In this demo board, KA2606 is used for pulse generator.



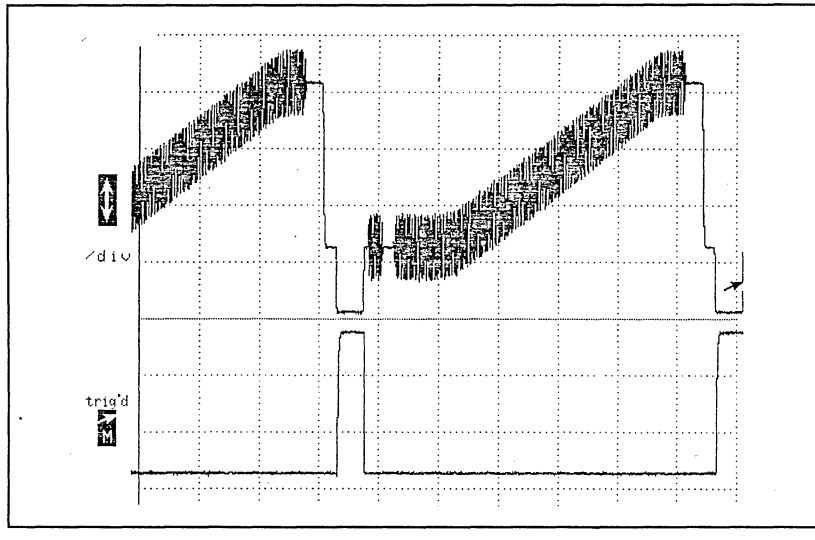
(The Pulse Generator Circuit)



(The Output Waveform)

a) The Sync Pulse

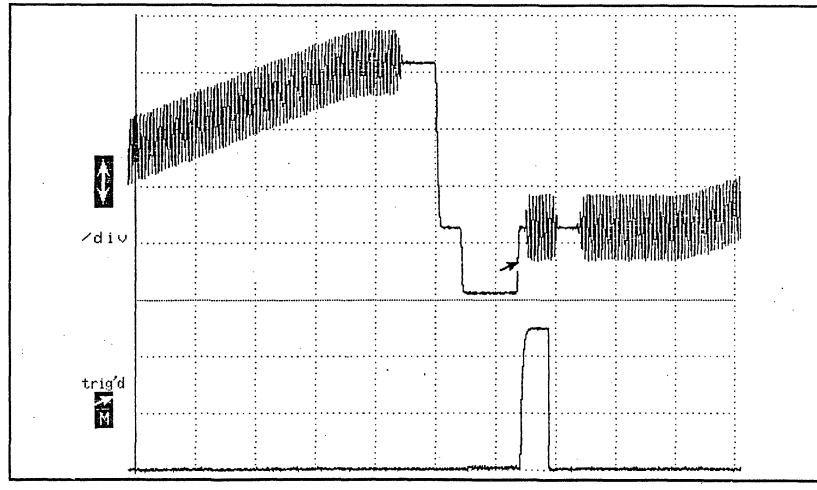
The sync pulse is generated from composite video signal through KA2606. The separated sync pulse is used for making sync pulse in D/A part of KSV3110, as being connected to the pin 39 of KSV3110. The sync level in D/A output is determined by adjusting the level of the pin 38 of KSV3110.



(The Generated Sync Pulse)

b) The Burst Pulse

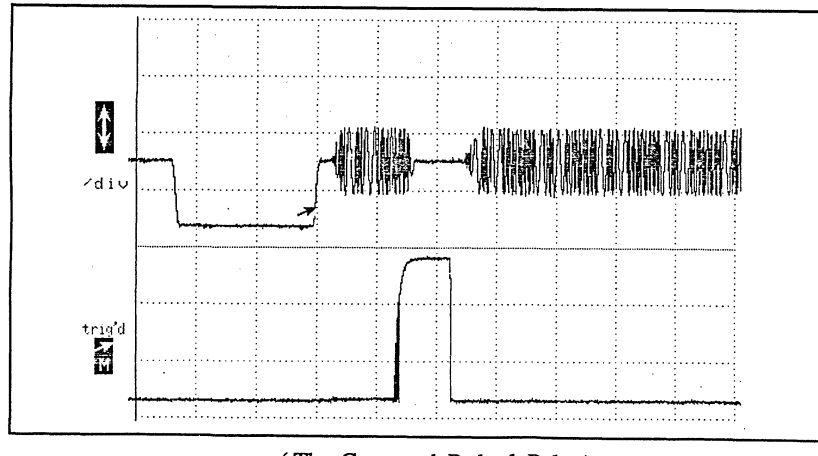
The burst pulse is generated from sync pulse through KA2606 by adjusting the delay time of KA2606. It is used for selecting the burst signal from data and the selected burst signal is connected to XR210 and it is used for making the clock signal. The XR210 generates the clock signal (4fsc = 14.3MHz) locked at burst signal.



(The Generated Burst Pulse)

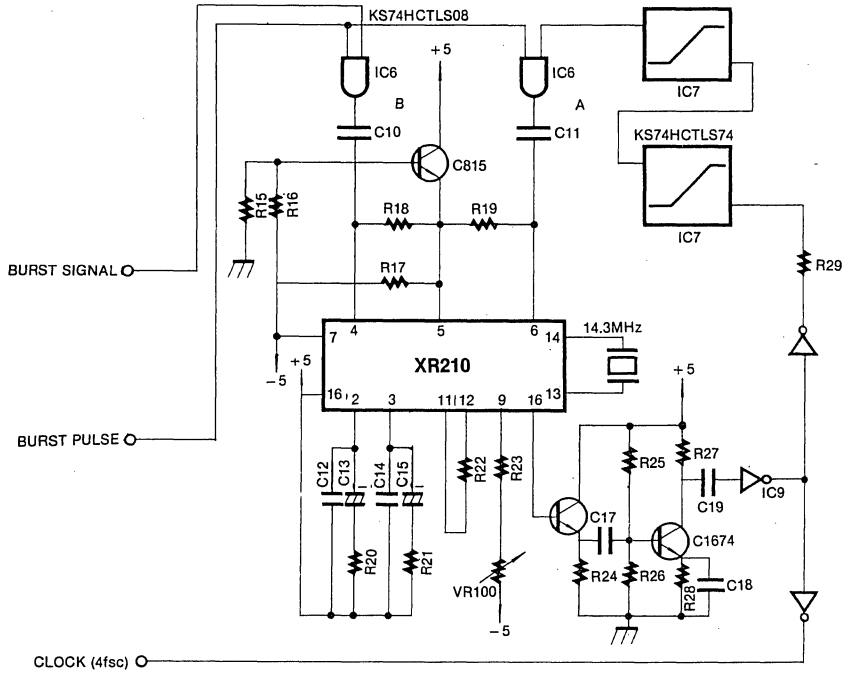
c) The Pedestal Pulse

The pulse is generated from the burst pulse through KA2606 by adjusting the delay time of KA2606 and it is used for detecting the pedestal level of video signal and clamping video signal as being connected to the pin 23 of KSV3110. The clamping level is determined by adjusting the level of pin 22 of KSV3110.



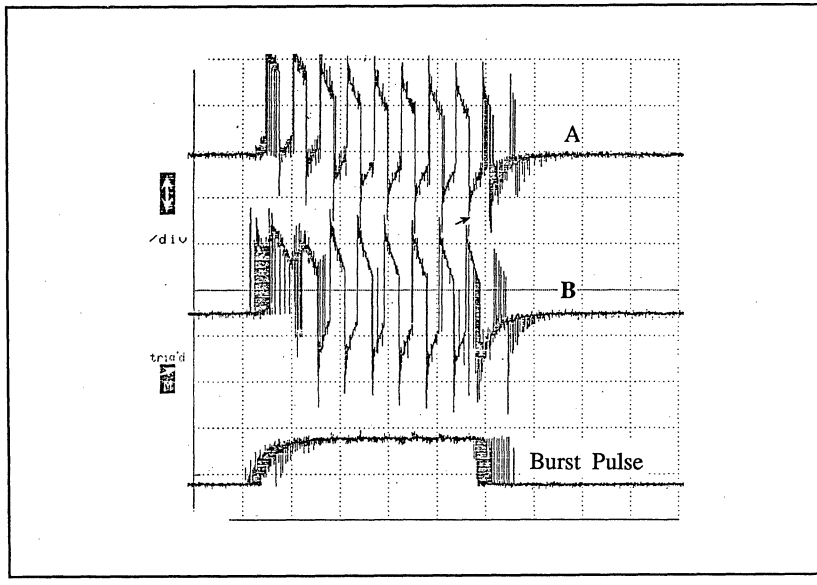
(The Generated Pedstal Pulse)

3) Clock Generator



(The Clock Generator Circuit)

The clock generator generates 4fsc (14.3MHz) clock signal. The generated clock signal is used for the sampling clock of ADC and DAC. The sampling frequency should be higher than 2*fsc according to sampling theory.



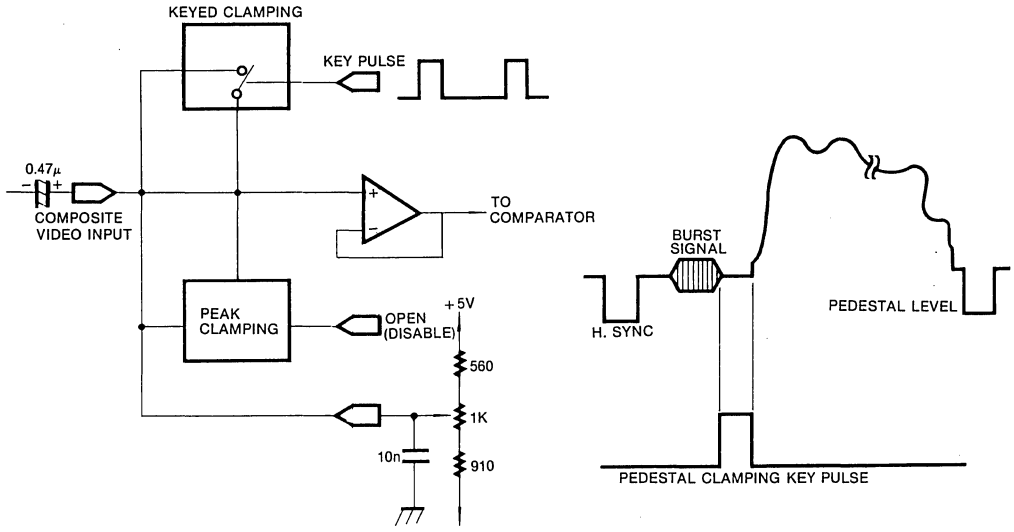
(A and B Point Signal)

The 4fsc signal should be synchronized with burst signal and it is generated from XR210.

4) Clamp

The clamp block clamps the video signal to the level to which user wants to clamp The KSV3110 has two types of clamp circuit—keyed clamp and peak clamp—in itself.

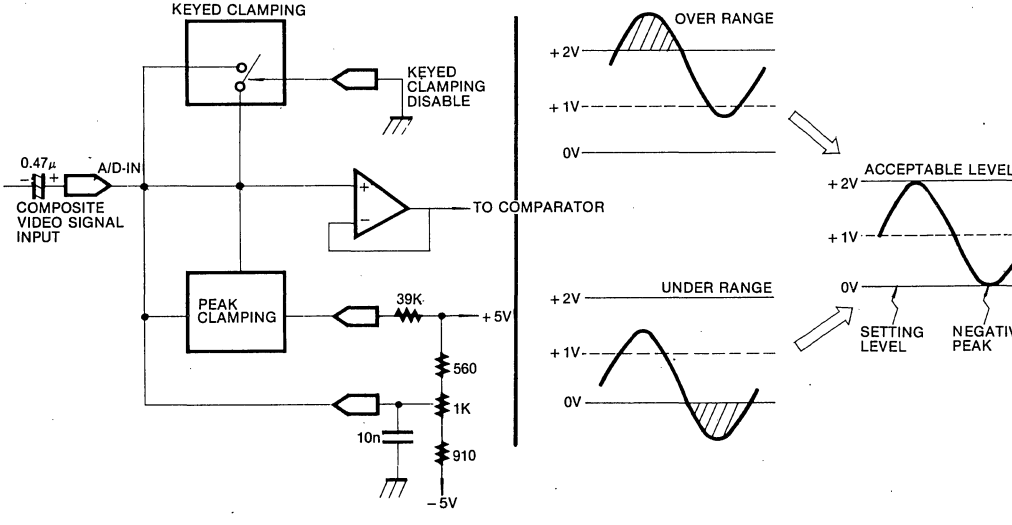
a) The Keyed Clamp



(The Keyed Clamp Circuit)

The keyed clamp circuit clamps the signal to the desired level when only key pulse is applied (pin 23). When being used the keyed clamping circuit, the pin 20 of KSV3110 should be open. The desired clamping level is determinded by the level of pin 22.

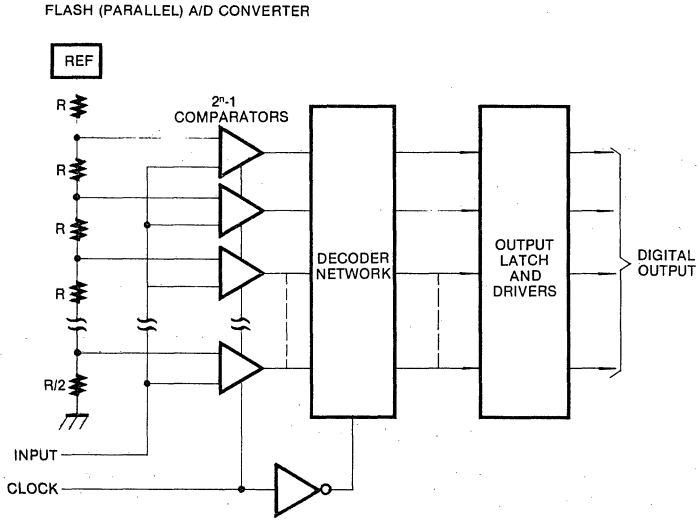
b) The Peak Clamp



(The Peak Clamp Circuit)

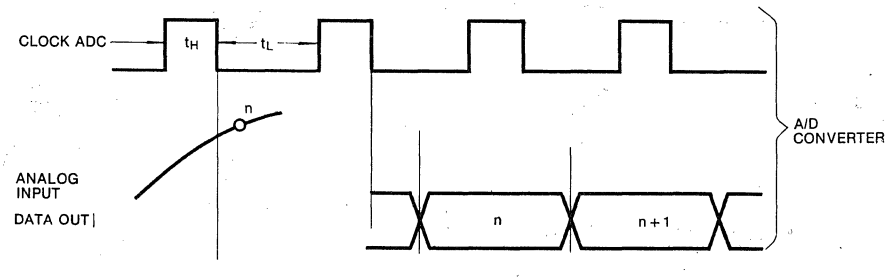
The peak clamping circuit clamps the negative peak value to the desired level. When the peak clamping circuit is used, the pin 20 of KSV3110 should be high with 39K ohm resistor and the pin 23 should be at ground level. The desired level is determinded by the level of the pin 22 of KSV3110. The KSV3110 demo board is being used the keyed clamping circuit.

5) The A/D Converter



(The Flash A/D Converter)

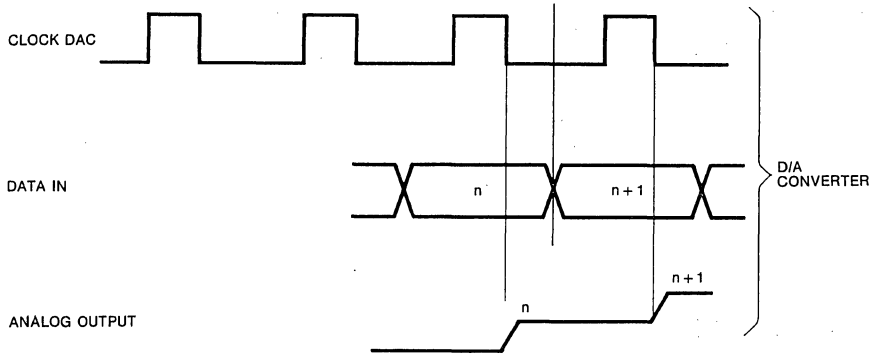
The A/D Converter part of KSV3110 is flash converter which consists of 255ea comparator. It's conversion speed is very fast (20 MSPS). The clamped video signal is converted to digital signal through A/D part with the sampling clock (4fsc). The A/D part timing diagram is as below.



(The Timing Diagram of A/D Part)

The signal is sampled at falling edge of clock and the sampled data are transed to latch part at raising edge of clock and the data are out at falling edge.

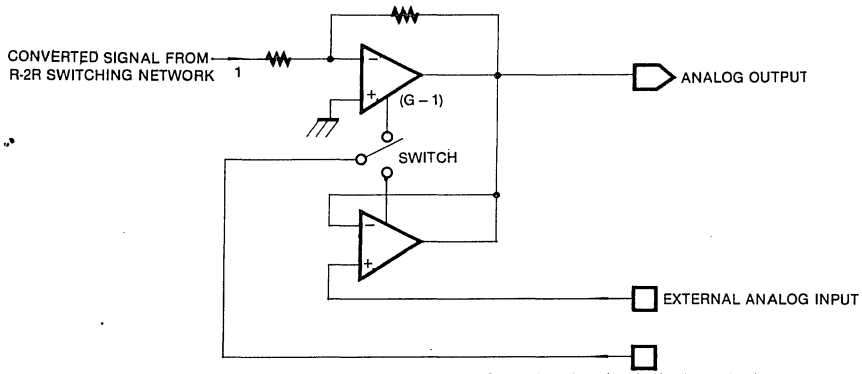
6) D/A Converter



(The Timing Diagram of D/A Part)

The analog signal is out at the falling edge of KSV3110 and the full range of D/A output signal is $2V_{p\text{-}p}$.

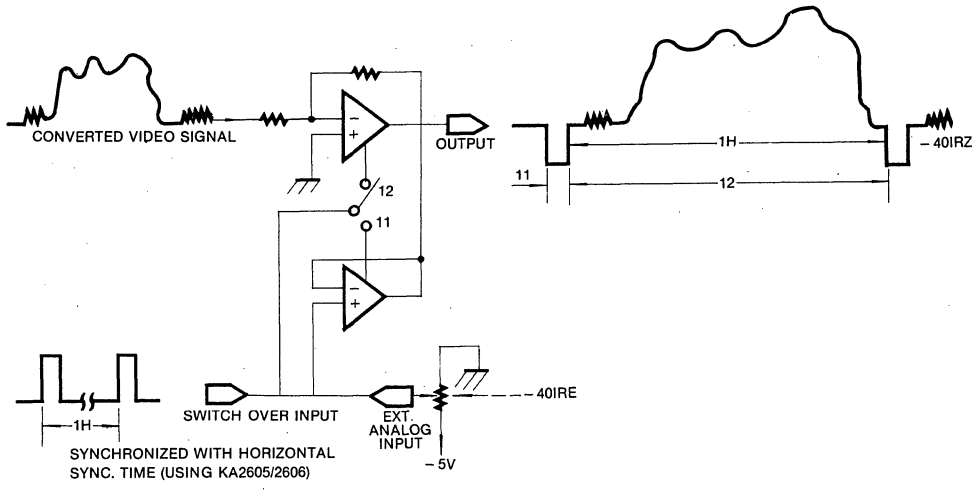
7) D/A Output Switch Over Circuit

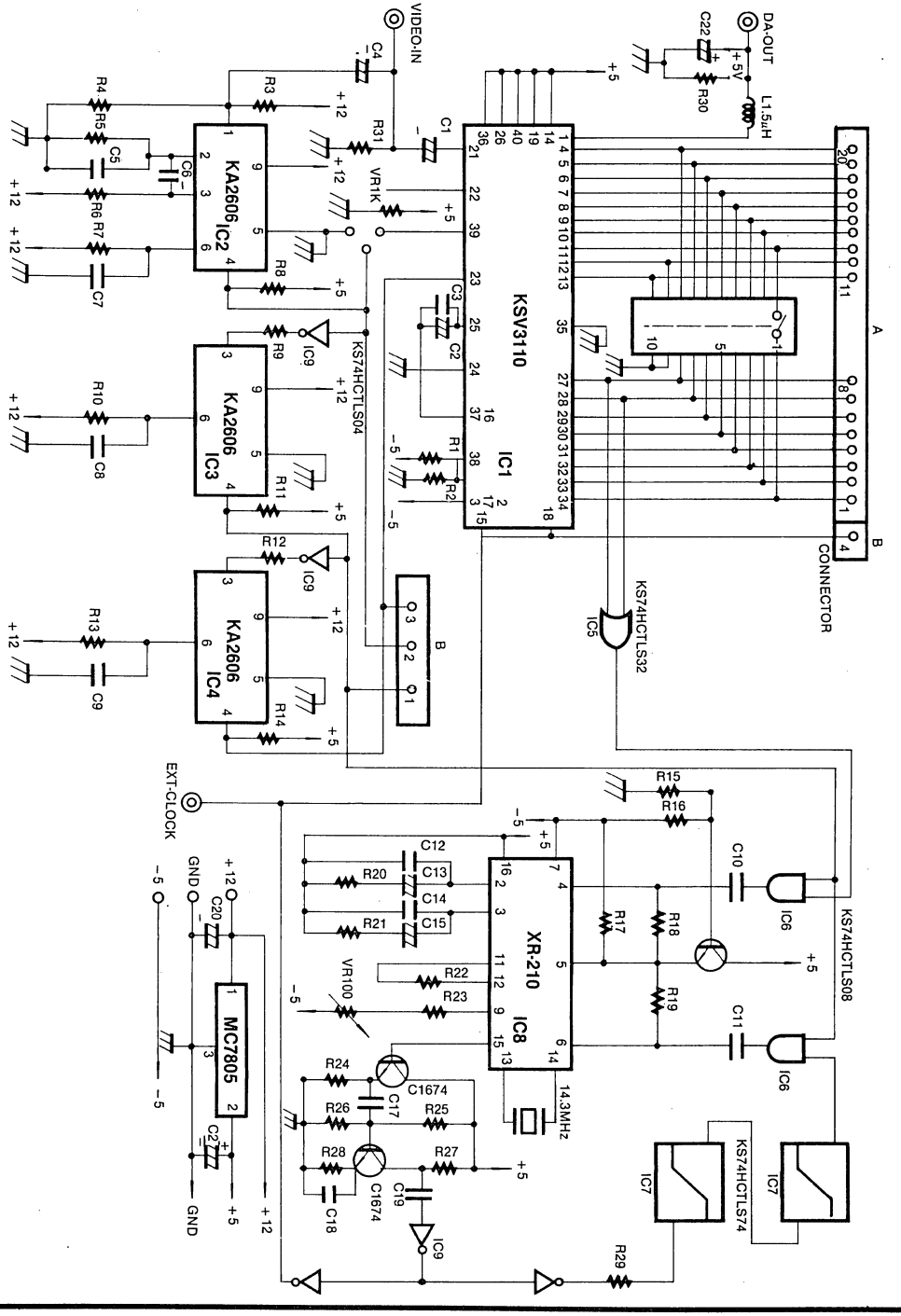


(Logic-HI: External analog signal—Analog output)
(Logic-LO: Converted signal from R-2R network—Analog output)

When the pin 39 of KSV3110 is high, the external signal which is connected to the pin 38 is out and when the pin 39 of KSV3110 is low, the converted signal is out. In the KSV3110 Demo Board, this block is used for adding the horizontal sync pulse to the converted composite video signal.

The sync pulse which is separated from the video signal through KA2606 is connected to the pin 39 which control the D/A output of KSV3110. The desired sync level is connected to the pin 38. When the separated sync pulse is high, the sync level is out and it makes the stabilized composite video signal.

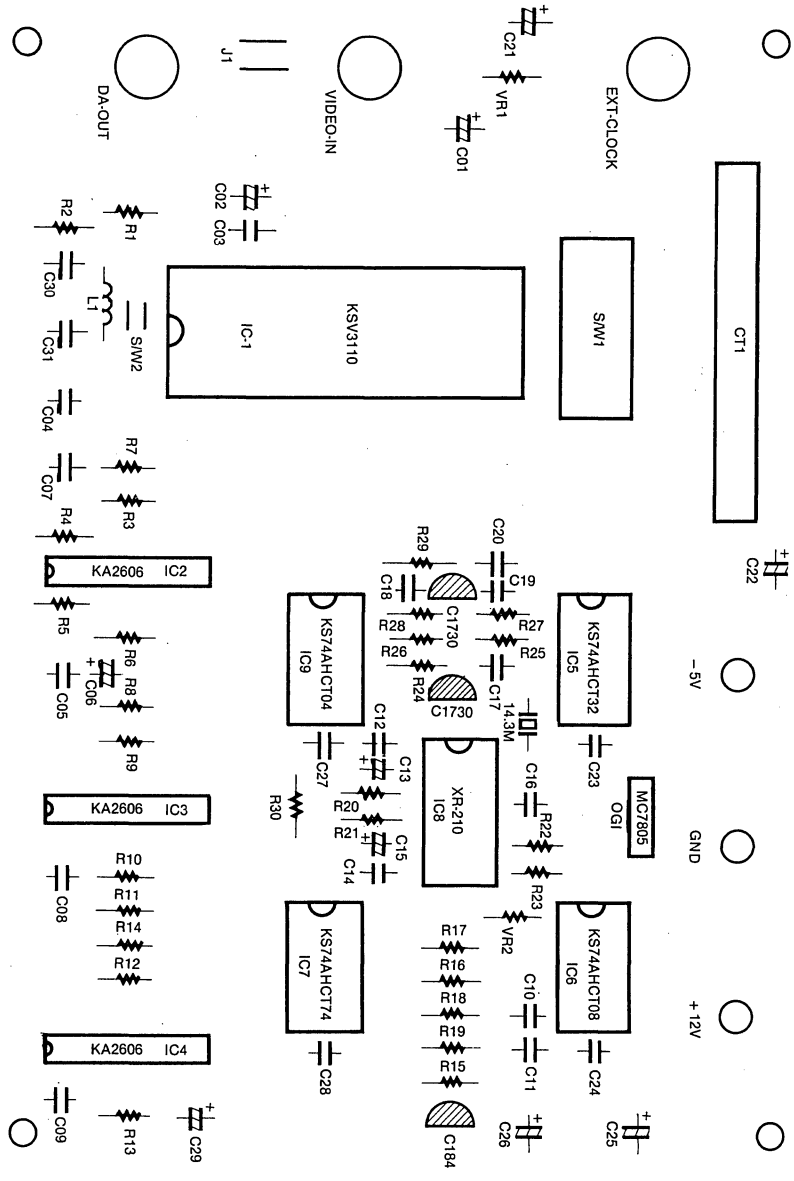

CONVERTED VIDEO SIGNAL
OUTPUT
12
11
1H
40IRZ
11
12
40IRE
SWITCH OVER INPUT
EXT.
ANALOG
INPUT
5V
1H
SYNCHRONIZED WITH HORIZONTAL
SYNC. TIME (USING KA2605/2606)


VIDEO-IN
DA-OUT
+5V
L1.5μH
C22
R30
KA2606 IC2
KA2606 IC3
KA2606 IC4
KSV3110
IC1
KS74HCTLS04
IC9
KS74HCTLS32
IC5
CONNECTOR
EXT-CLOCK
XR-210
IC8
MC7805
14.3MHz
KS74HCTLS08
IC6
KS74HCTLS74
IC7
C1674
VR1K
VR100
GND

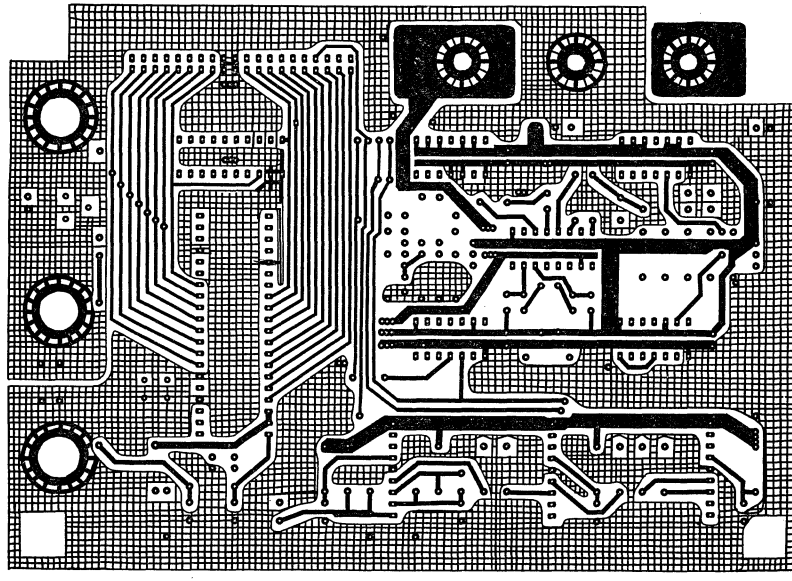
COMPONENT VALUE

No.	Value	Unit	No.	Value	Unit
R1	4.7	Kohm	C1	0.47	μF
R2	1.2	Kohm	C2	0.1	μF
R3	7.5	Kohm	C3	10	μF
R4	4.7	Kohm	C4	0.22	μF
R5	82	ohm	C5	560	pF
R6	820	Kohm	C6	1	μF
R7	12	Kohm	C7	0.0068	μF
R8	3.3	Kohm	C8	0.0039	μF
R9	4.7	Kohm	C9	0.0033	μF
R10	12	Kohm	C10	100	pF
R11	3.3	Kohm	C11	100	pF
R12	4.7	Kohm	C12	0.1	μF
R13	12	Kohm	C13	0.47	μF
R14	3.3	Kohm	C14	0.1	μF
R15	2.2	Kohm	C15	0.47	μF
R16	3.3	Kohm	C16		
R17	22	Kohm	C17	0.002	μF
R18	1.2	Kohm	C18	470	pF
R19	1.2	Kohm	C19	0.015	μF
R20	3.9	Kohm	C20		
R21	3.9	Kohm	C21	47	μF
R22	4.7	Kohm	C22	47	μF
R23	47	ohm	C23	0.1	μF
R24	1	Kohm	C24	0.1	μF
R25	6.8	Kohm	C25	47	μF
R26	1.2	Kohm	C26	47	μF
R27	1.2	Kohm	C27	0.1	μF
R28	91	ohm	C28	0.1	μF
R29	100	ohm	C29	47	μF
R30	400 1K	ohm			
R31	400	ohm			

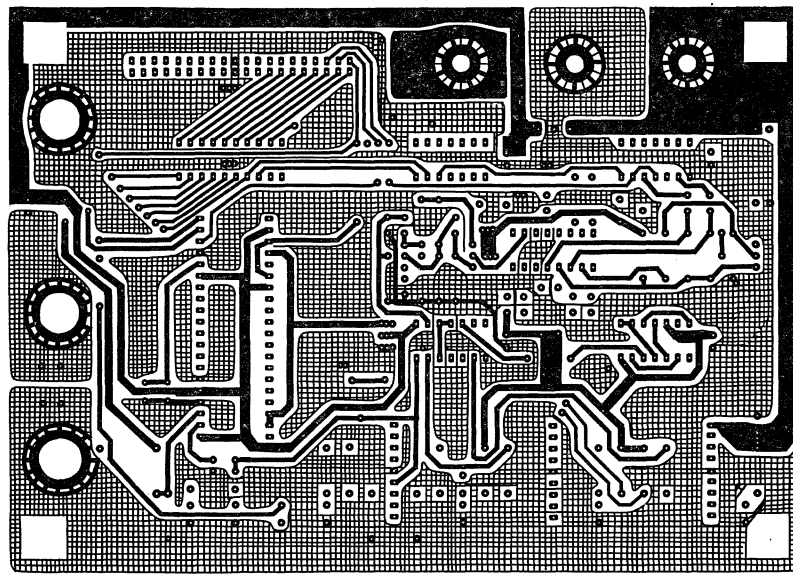
THE COMPONENT LAYOUT



The Front Side



The Back Side



GENERAL DISCRIPTION

Analog filter select the frequency which you want to, from larbitrary analog signal. Digital filter also select the spectrum which you want to, from larbitrary digital signal. Digital filter basically consist of binary adder, digital mux and delay element. Digital filter has several merits compared with analog filter, that is, in digital filter, the responce characteristics can be modified easily by changing filter constant, and digital filter perform successfully the filtering function, even if low frequency, and digital filter is strong to temperature drift, to interal/external noise. Now, we will explain the digital comb filter of digital composite video signal, and digital color demodulator which separate digital B – Y, digital R – Y signal from digital chrominance signal.

THE STRUCTURE OF VIDEO SIGNAL

NTSC signal is composed very precisely, as account of National Television System Committee decision. This NTSC signal consist of chrominance, luminance, sync signal.

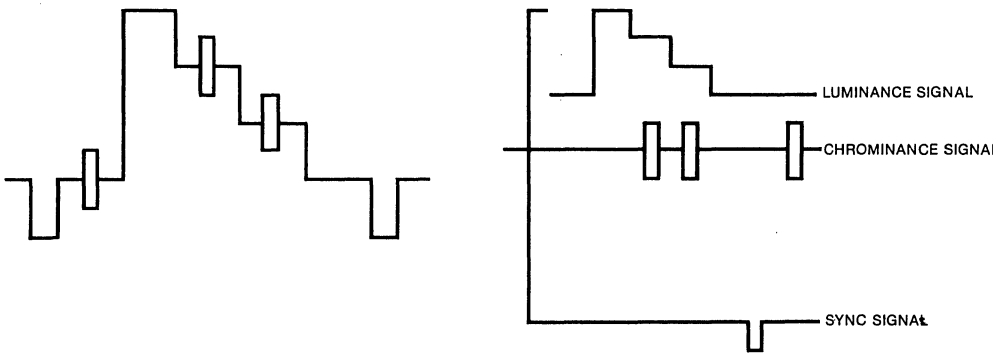


Fig. 1 NTSC Signal

1 THE RELATION OF NTSC SIGNAL

NTSC signal consist of three kinds of signal, as Figure 1.

* Luminance signal—Brightness
* Chrominance signal—Color
* Sync signal—Position of signal

These signal have their own frequency band width.

* Luminance signal—0 – 4.2 MHz
* Chrominance signal—3.58 MHz ± 500 KHz

and these signal have the relation, as below

$$Fsc = 455/2\ Fh \quad (1)$$
$$Fh = Fsif/286 = 15.734\ KHz \quad (2)$$
$$Fv = 2/255 * Fh = 59.94\ Hz \quad (3)$$

* Fh : Horizontal sync frequency
* Fv : Vertical sync frequency
* Fsc : Color carrier frequency (3.579545 MHz)
* Fsif : Sound intermadiate frequency (4.5 MHz)

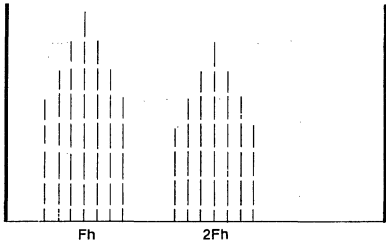


Fig. 2 Signal Spectrum

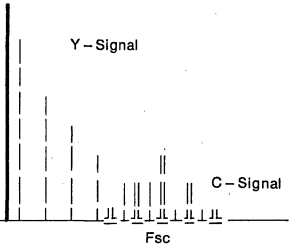


Fig. 3 Y/C Spectrum

2 THE ANALYSIS OF NTSC SIGNAL

The composite video signal can be expressed, as below

$$E1 = Ey1 + Ei1\ SinWct + Eq1\ CosWct \quad (4)$$
$$E2 = Ey2 + Ei2\ SinWct + Eq2\ CosWct \quad (5)$$
$$= Ey2 + Ei2\ SinWc(t + th) + Eq2\ CosWc(t + th)$$
$$= Ey2 + Ei2\ Sin(Wct + 2*180*fh*th*455/2) + Eq2\ Cos(Wct + 2*180*fh*th*455/2)$$
$$= Ey2 + Ei2\ Sin(Wct + 180) + Eq2\ Cos(Wct + 180)$$
$$= Ey2 - (Ei2\ SinWct + Eq2\ CosWct) \quad (6)$$

So, finally we can write these equation as general form as blow

$$En = Eyn + Ein\ SinWct + Eqn\ CosWct\ (n = 1, 3, 5, 7\ \ldots) \quad (7)$$
$$En = Eyn - (Ein\ SinWct + Eqn\ CosWct)\ (n = 2, 4, 6, 8\ \ldots) \quad (8)$$

In general equation, you can find out easily that the phase of color carrier signal, is inverted per adjacent horizontal line, this point is very important thing in application of digital filter.

DIGITAL COMB FILTER

The comb filter is refered to obtain the pure chrominance signal from the composite signal. Before explaination on digital comb filter, let's see analog comb filter first. To understand analog comb filter, you should remember the fact the phase of color carrier signal is inverted per adjacent horizontal line. As addition two adjacent horizontal line, chrominance signal is eliminated, and the twice luminance signal is obtained, according to equation 7 and 8. To subtract two adjacent horizontal line, luminance signal is eliminated, and the twise chrominance signal is obtained, according to equation 7 and 8.

In digital comb filter, the theory of filter is the same as analog comb filter. Digital comb filter seperate digital chrominance, luminance signal from digital composite signal, the sampled composite signal can be represented as below.

$$E(n) = Y(n) + C(n)$$
$$E(n+1) = Y(n+1) + C(n+1)$$

if $Y(n) = Y(n+1)$, and $C(n) = C(n+1)$

$$E(n) + E(n+1) = Y(n) + C(n) + Y(n+1) + C(n+1)$$
$$= 2*Y(n) + C(n) - C(n)$$
$$= 2*Y(n)$$
$$E(n) - E(n+1) = Y(n) + C(n) - Y(n+1) - C(n+1)$$
$$= 2*C(n) + Y(n) - Y(n)$$
$$= 2*C(n)$$

As a result, we can obtain digital chrominance, and luminance signal from digital composite signal, and we can design the block of digital comb filter.

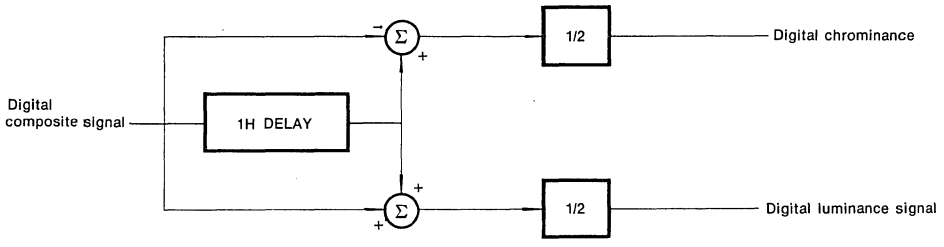


Fig. 4 Digital Comb Filter

We use the 1H delay element with the line memory that has FIFO dual port I/O. The ALU, adder and subtractor should be fast.

COLOR DEMODULATOR

The comb filter seperate the chrominance, luminance signal from the composite signal. The color demodulator seperate the R – Y, B – Y signal from chrominance signal. The theory of color demodulator is

$$Cn = (Er - y)\ SinWct + (Eb - y)\ CosWct \quad (9)$$

as product SinWct to Cn, we can obtain (Er – y) according to fourier series, that is,

$$Cn * SinWct = (Er - y) \quad (10)$$

as product CosWct to Cn, we can obtain (Eb – y) according to fourier series, that is,

$$Cn * CosWct = (Eb - y) \quad (11)$$

The analog color demodulator use the equation 10, 11 and 12. Digital color demodulator use the same theory as analog color demodulator. From now on, we will explain the digital color demodulator. The sampled chrominance signal with 4*fsc can be expressed as below

$$C(n) = (Er - y(n))Sin90n + (Eb - y)Cos90n \quad (12)$$

and the sampled SinWct, CosWct is sequence of data 1.0. – 1.. See Figure 5.

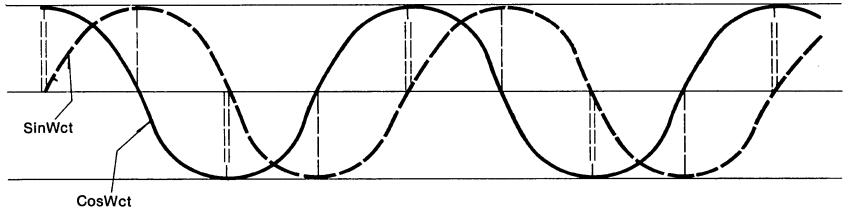


Fig. 5

The means of producting SinWct, CosWct to C(n) is to producting the sequence of data 1.0. – 1. in digital color demodulator. The sequence of data 1.0. – 1. means

1. _____ pass the data of C(n) through
0. _____ no pass the data of C(n)
– 1. _____ pass the 2'complimental data of C(n) through

in digital color demodulator.

The block diagram is represented as below

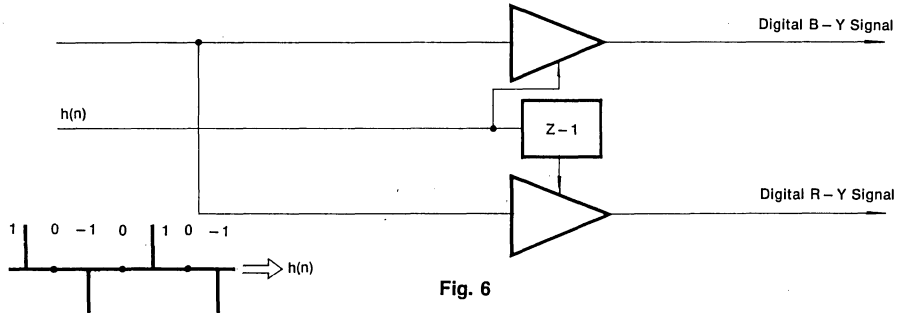


Fig. 6

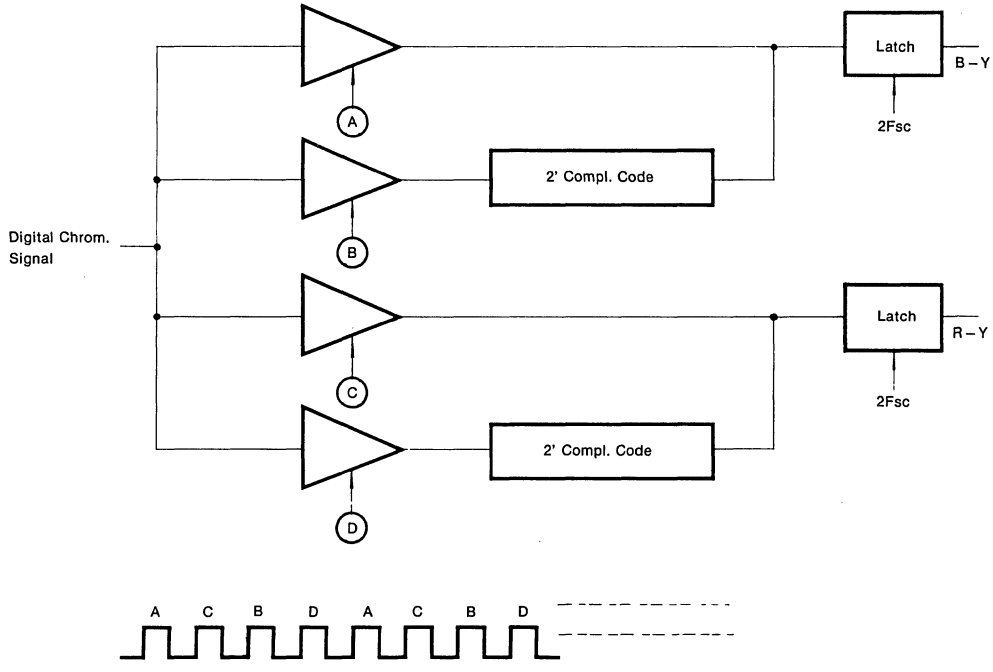


Fig. 7

THE CONCLUTION

We have explained the theory of digital comb filter, color demodulator. We are sure this meterial is useful to understand, design the digital comb filter and color demodulator.

NOTES

GLOSSARY 6

Accuracy

Accuracy can be specified as absolute or relative accuracy. Absolute accuracy is the difference between the theoritical value of input voltage to produce particular output code and the actual value of the input voltage required to produce this code. It comprises of gain error, zero error and non-linearity together with noise (See Figure 1).

Relative accuracy is measured in %, ppm or as fractions of LSB. It is a deviation of analog value from the theoritical value for a particular code. This deviation is relative to a full scale analog reange of its transfer characteristic, after this range has been calibrated.

ADC

Abbreviation for analog-to-digital converter (see A/D converter).

A/D Converter

Analog-to-digital converter. A circuit which converts an analog voltage or current into an output which is a digital code.

AGND (Analog Ground)

Ground reference point for analog power supply and analog circuitry.

Alias Frequency

If an analog signal converted to the digital code and then reconverted to the analog signal through a D/A converter, and if there is any lower frequency component present in the reconverted signal which does not belong to the original analog signal, then this frequency component is an alias frequency. The cause for this effect is that the sampling rate is lower than that required by the sampling theorem.

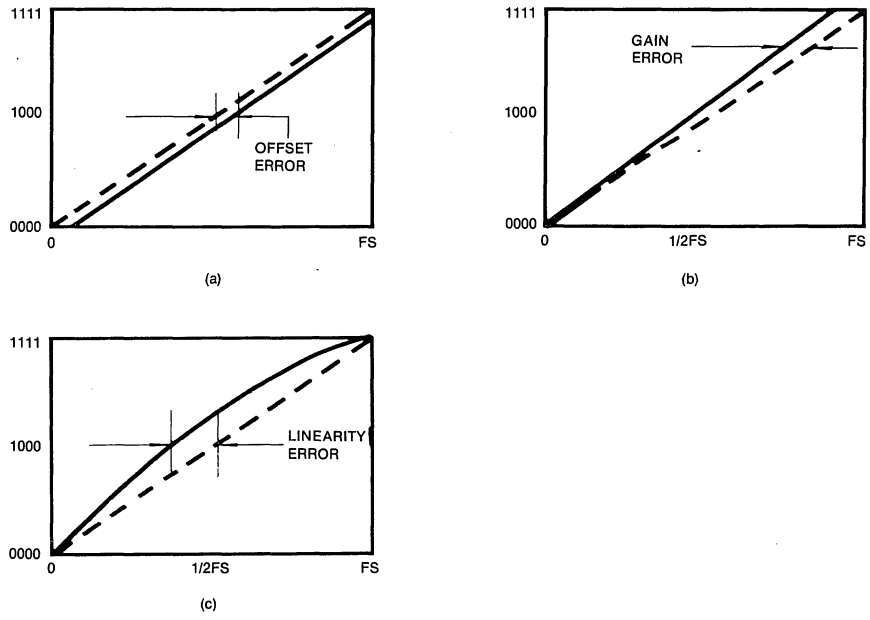


Fig. 1 Errors for an A/D Converter; (a) Offset; (b) Gain; (c) Linearity

Aperture Time

Aperture time is a time interval from the time the hold command is applied to the sample-and-hold circuit and the actual opening of the sampling switch. The aperture time depends on the delay of logic switching and an uncertainty (due to jitter etc). This is a predominant factor that imposes the limit on timing accuracy. Generally, when the apeture time is critical, the hold command is advanced to compensate for the known component of aperture delay.

Auto-Zero

A stabilization circuit which will bring the input offset of an amplifier or A/D converter to zero during operating cycle portion.

Bandgap Reference

A voltage reference circuit which is designed using the principle of the predictable base-to-emitter voltage of a transistor required to generate a constant voltage which is equal to the extrapolated bandgap voltage of silicon.

BCD (Binary Coded Decimal)

A binary code used to represent dicimal numbers in which each digit from 0 to 9 is represented by four bits weighted 8-4-2-1. Out of the 16 possible states from four bits, only 10 state are used in BCD code.

Bipolar Mode

For a data converter, when the analog signal range includes both positive and negative values, it is called bipolar mode.

Bipolar Offset

The analog displacement of one half of the full scale range in a data converter operated in the bipolar mode. The offset is generally derived from the converter reference circuit.

Buffer Amplifier

An amplifier employed to isolate the loading effect of one circuit to another circuit is called buffer amplifier.

Ci (Input Capacitance)

In flash converter, Ci is an approximation of its largely capacitive input impedance. This input capacitance is dependent upon the DC level of the analog input voltage and the input frequency. The input equivalent capacitance must be taken into account when designing a buffer to drive the flash converter.

Charge Balancing A/D Converter

The analog-to-digital conversion technique which employs an operational integrator circuit within a pulse generating feedback loop. Current pulses from the feedback loop are precisely balanced against the analog input by the integrator. The resulting pulses are counted for a fixed period of time to produce an output digital word. This technique is also known as the quantized feedback.

Clock

A continuous trail of pulses which is used to control the timing of the data conversion process. A circuit that generates this clock pulses is called the clock generator.

Clock Rate

The frequency of the timing pulses of the clock circuit in a data converter.

Co (output Capacitance)

This is a parasitic capacitance between the output terminal of a device and the ground.

CMRR (Common Mode Rejection Ratio)

For an amplifier, CMRR is a ratio of the differential voltage gain to the common mode voltage gain. Generally, this ratio is expressed in dB.

$$CMRR = 20 \log_{10} \frac{Ad}{Acm}$$

where, Ad is a differential voltage gain, and Acm is a common mode voltage gain.

Companding Converter

The companding converter can be An A/D or D/A converter which employs the logarithmic transfer function to expand or compress the analog signal range. This type of converter has large effective dynamic ranges and it is commonly used in digital voice communication systems.

Complementary Binary Code

A binary code which is the logical complement of a straight binary. In other words all 0's and 1's are interchanged.

Conversion Time

This is the time required by an A/D converter to finish the measurement. In flash converter, new conversions are already initiated before the results of the prior conversions have been determined. The time for an 8-bit conversion for this device is only one clock period.

Conversion Rate

The number of repetitive A/D or D/A conversions per second for a specified full scale range is attained. For most converters, if no additional system delays are involved, then the conversion rate is an inversion of the conversion time.

Counter Type A/D Converter

A feedback method of A/D conversion whereby a digital counter drives a D/A converter which generates an output ramp which is compared with the analog input. When the two are equal, a comparator stops the counter and output data is ready. It is also called a servo type A/D converter.

DAC

Abbreviation for Digital-to-Analog converter. See D/A converter.

D/A Converter

Digital to Analog Converter. A circuit which converts digital code into analog output voltage or current.

Data Acquisition System

A system consisting of analog multiplexers, sample-hold circuits, A/D converters and other related circuits which process one or more analog signals and convert them into digital form for use by a computer.

Data Converter

An A/D or D/A converter.

Decoder

A communications term for D/A converter.

Deglitched DAC

A D/A converter which incorporates a deglitching circuit to virtually eliminate output spikes (or glitches). They are commonly used in CRT display system.

Differential Linearity TEMPCO

The variation in differential linearity error with the temperature for a data converter is known as TEMPCO. It is expressed in ppm/°C of FSR, the full scale range.

Digitizer

A device which converts analog into digital data; an A/D converter.

DG (Differential Gain)

Differential gain is defined as the difference between the ratio of the amplitudes of the output of a small high frequency signal on which it is superimposed and the unity.

In color television, processing of a color signal requires that the amplitude of the chrominance signal is not affacted by the luminance function. The differential gain is a very important parameter because, the amplitude of a small signal that is superimposed upon another signal represents the saturation of color displayed; i.e., it determines the brightness of this color.

The standard method for measuring the differential gain is by using a standardized test signal, known as modulated ramp (shown in figure 2). The output of the A/D is then reconstructed by a reference D/A and low pass filter; the resultant signal is displayed on a vectorscope.

DGND (Digital Ground)

Ground reference point for digital power supply and digital circuitry.

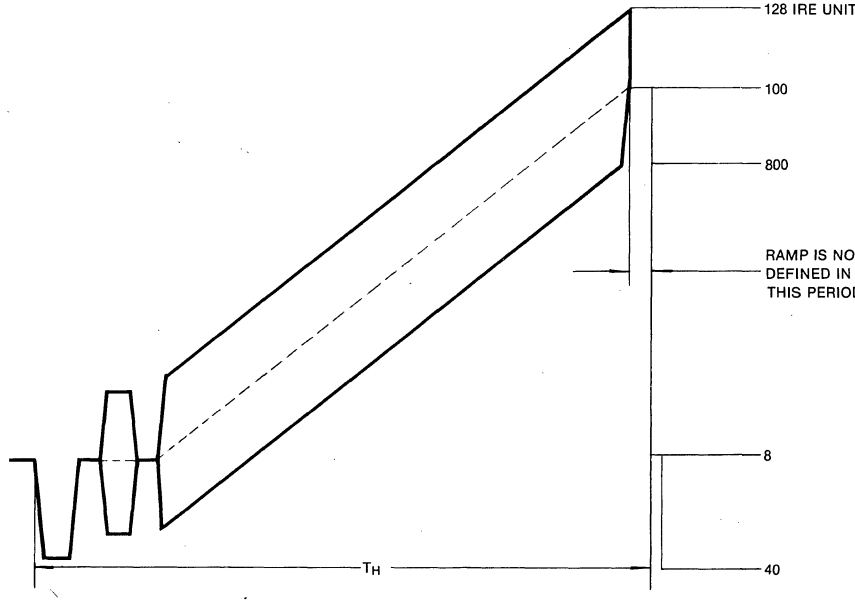


Fig. 2 Modulated Ramp Test Signal

DP (Differential Phase)

Differential phase is defined as the difference in the output phase of a small high frequency sine wave signal at two given levels of a low frequency on which it is superimposed. In color television, processing of a color signal requires that the phase of the chrominance signal is not affected by the luminance function. Errors in differential phase appear on the T.V. screen as changes in the hue of colors with the changes in brightness. Differential phase measurement is very similar to the differential gain testing.

Dual Slope A/D Converter

This represents An indirect method of A/D conversion where an analog voltage is converted into the time period by an integrator and a reference and then measured by a clock and counter. The method is relatively slow but highly accurate.

Dynamic Accuracy

The total error of a data converter or conversion system when operated at its maximum specified conversion rate or throughput rate.

Dynamic Range

The ratio of the full scale range (FSR) of a data converter to the smallest difference it can resolve. In terms of converter resolution;

Dynamic Range (DR) = 2^n

it is generally expressed in dB.

$DR = 20 \log_m 2^n = 6.02n$

where n is the resolution in bits.

Encoder

A communication term for A/D converter.

Feedback Type A/D Converter

A class of analog-to-digital converters in which a D/A converter is enclosed in the feedback loop of a digital control circuit which changes the D/A output until it equals the analog input.

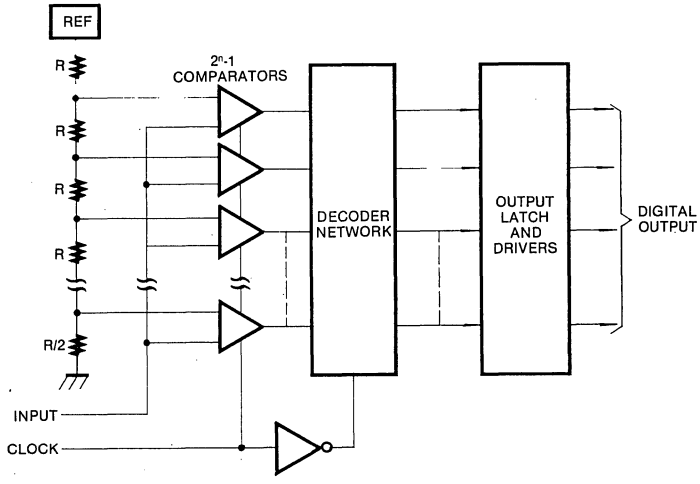


Fig. 3 Flash (Parallel) A/D Converter

Flash Type A/D Converter

An ultrafast method of A/D conversion which uses an array of 2^n-1 comparators to directly implement a quantizer, where n is the resolution in bits. The quantizer is followed by a decoder circuit which converts the comparator outputs into binary code. (See Figure 3)

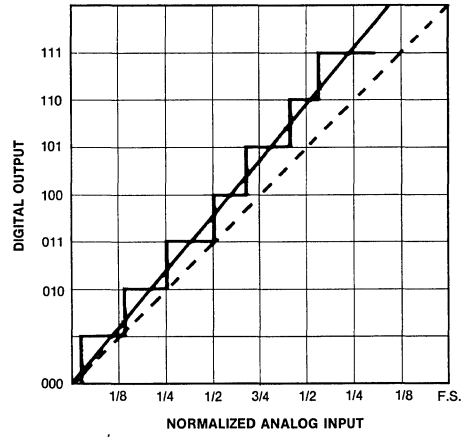
FSR (Full Scale Range)

The difference between maximum and minimum analog values for an A/D converter input or D/A converter outputs.

Full Power Bandwidth (BW)

Bandwidth for a flash A/D converter is defined as the maximum frequency of full-scale input sinewave which can be quantized by the A/D converter without any missing or spurious codes. The spurious code is a code which is largly inaccurate, for example, a full scale output code for an input which is near mid-scale is a spurious code. The bandwith is measured with worst case power supply conditions and at the fullscale sampling rate.

Fig. 4 Gain Error



Hysteresis Error

The small variation in analog transition points of an A/D converter whereby the transition level depends on the direction from which it is approached. In most A/D converters this hysteresis is very small and is caused by the analog comparator.

Gain Error

Gain error is a difference in slop between the ideal transfer function and the actual transfer function and it is expressed in percentage. The gain error may be eliminated by adjusting the reference voltage or current applied to the device. (see figure 4).

Hold Time

The time period after the operative edge of clock during which the input data must be stable in order to be correctly registered.

Icc (Supply Current)

Icc is the current drawn by the device from the Vcc supply. Icc is a positive valued parameter. It decreases with increasing temperatures in bipolar devices and is measured with Vcc at the maximum rate of value.

Iref (Reference Current)

Current flowing into or out of the reference input terminals of an A/D or D/A converter.

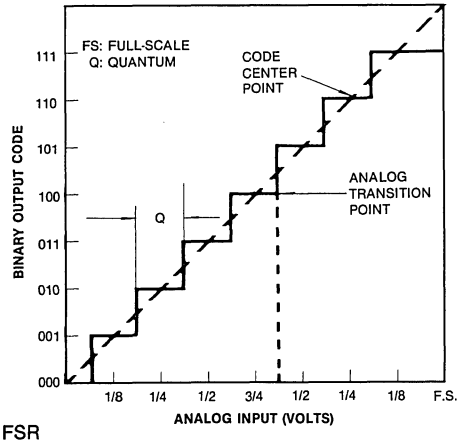
Integrating A/D Converter

This is one of the techniques for A/D conversion, in which the analog input is integrated with time. This includes dual slope, tripple slope, and charge balancing type of A/D converters.

LSB

The Least Significant Bit is a bit which carries the smallest value or weight. It represents the smallest change that can be resolved by an n-bit converter. This LSB (or a quantum) can be defined as:

Fig. 5 Ideal Transfer Function for a 3-bit A/D Converter with Quantized Characteristic.



$$\text{LSB Size (or Quantum)} = \frac{FSR}{2^n}$$

where FSR = full scale range, and
n = resolution in bits.

(See Figure 5)

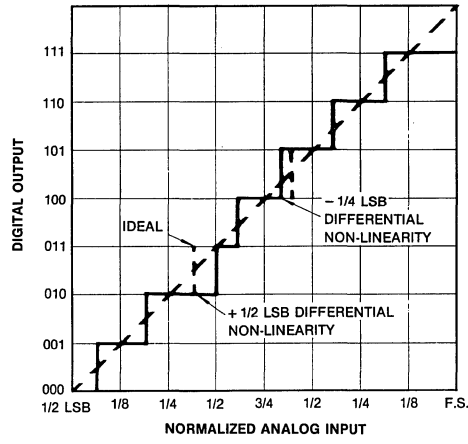
Linearity

Linearity is a maximum deviation from the straight line between the end points on the transfer curve of the converter. Generally, it is expressed as a function of LSB size. The linearity of a good converter is ± 1/2 LSB. The linearity error can be expressed as differential non-linearity and integral non-linearity.

Differential Non-Linearity

Differential Non-linearity is a measure of linearity from one digital state to the next. It applies to A/D and D/A converters. If differential linearity is specified as ± 1/2 LSB, the step size from one state to the next may be from 1/2 to 3/2 of an ideal 1 LSB step. (See Figure 6).

Fig. 6 Differential Non-linearity



For an n-bit converter, any particular digital output code should corroespond to a quantum of analog input value which is exactly 1 LSB in width. Any deviation of the measured value (step) from this ideal value is called differential non-linearity.

Differential non-linearity is an important specification because if this error is greater than 1 LSB, then it can lead to monotonic behaviour of a D/A converter part and will finally result in missing code in overall A/D converter's output. For example, if each transition is 1 LSB ± 1/2 LSB, then the differential linearity error of ± 1/2 LSB, but there is no possibility of missing code. If the transition is 1 LSB ± 1 LSB then there is a possibility of missing code (See Missing Code).

Integral Non-linearity

The differential nonlinearity deals with errors in step size and the integral nonlinearity deals with the deviations of overall of the conversion response.

Major Transition

In a data converter, the change from a code 1000...000 to 0111...111 or vice-versa is called major transition. This is the most difficult transition from a linearity standpoint, because the MSB weight must be exactly one LSB larger than the sum of all other bit weights.

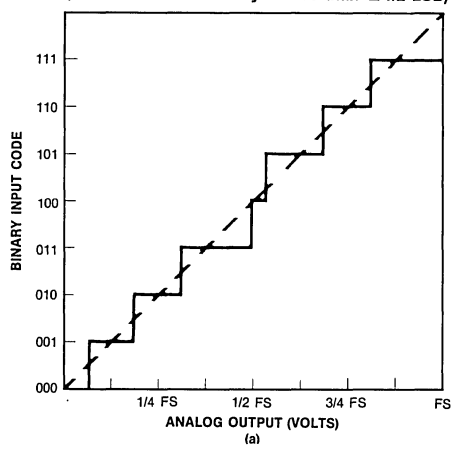
Missing Code

The missing code term applies to A/D converters. The output of an A/D converter may have a missing code when the differential linearity error is greater than ± 1 LSB. If the differential linearity error is less than ± 1 LSB, then there is no possibility of missing code (See Figure 7).

Maximum Sampling Rate (Fs)

Fs is the maximum sampling rate (or samples per second) at which the converter is guaranteed to operate. Most flash converters will operate reliably at any rate up to the maximum sampling rate. This is measured with worst-case supply, worst-case duty cycle condition and maximum full power input frequency.

Fig. 7 (a) No Missing Code
(Differential Non-linearity is less than ±1/2 LSB)



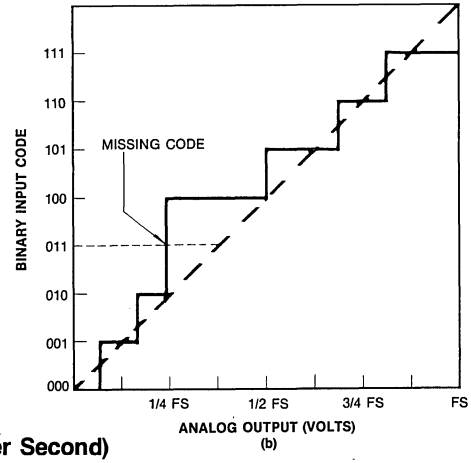
Monotonicity

This is a characteristic of the transfer function of a D/A converter, where, increase in input code will produce continuously increasing analog output. Monotonicity may occur in a D/A converter, when the differential linearity exceeds 1 LSB. This means that each successive output level is greater than the previous one (See Figure 8).

MSB

The Most Significant Bit is bit that carries the largest weight which is equal to one half of the full scale range.

(b) Missing Code



MSPS (Mega Samples Per Second)

The abbreviation for the conversion rate at which an A/D or D/A converter is operating.

Natural Binary Code

A positive weighted code in which a number is represented by

$$N = a_0\,2^0 + a_1\,2^1 + a_2\,2^2 \ldots\ldots + a_n\,2^n$$

where each coefficient "a" has a value of zero or one. Data converters use this code in its fractional form where:

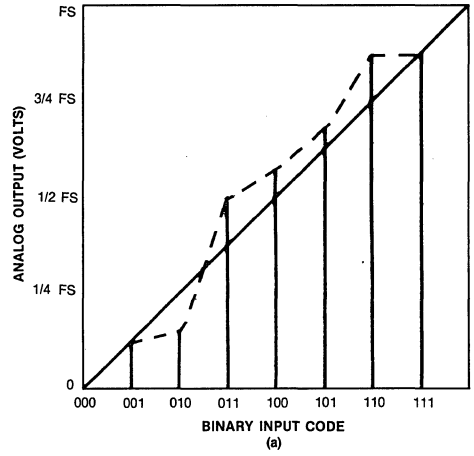
$$N = a_1\,2^{-1} + a_2\,2^{-2} + a_3\,2^{-3} \ldots\ldots + a_n\,2^{-n}$$

and N has a fractional value between zero and one.

Noise Rejection

The amount of suppression of normal mode analog input noise of an A/D converter or other circuit, generally expressed in dB. Good noise rejection is a characteristic of integrating type of A/D converters.

Fig. 8 Outputs of a D/A Converter:
(a) Monotonic Output:



Nonmonotonic

It is the characteristic of a transfer function of an A/D converter where the output does not continuously increase with the increase in input. When this occurs, there may be a dip at one or more points in the output function (See Figure 8).

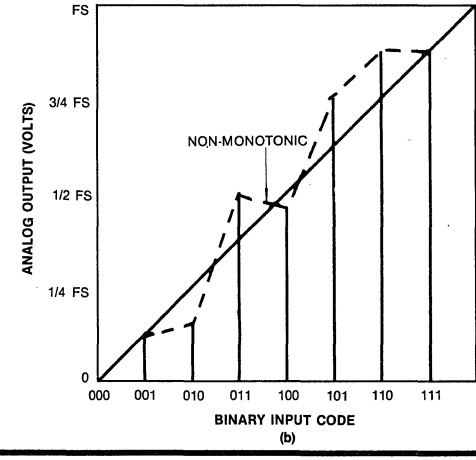
Nyquist Theorem (or Sampling Theorem)

A theorem developed by Nyquist which states that if a continuous, bandwidth limited signal contains no frequency components higher than fc, then the original signal can be recovered without distortion if it is sampled at a rate of at least 2fc samples per second where, fc is a carrier frequency.

Output Delay

The output delay is the time between the rising edge of the signal to be converted and the time when the output data from the A/D converter is guaranteed to be stable. This output delay can be measured with the test load specified in the data sheet. The output delay can be reduced in TTL type flash convertes by connecting the pull-up resistors from the outputs to the V_{CC}.

(b) Nonmonotonic Output



Quantizer

A circuit which transforms a continuous analog signal into a set of discrete output states. Its transfer function is the familiar staircase function.

Quantization Error

This is a basic type of error associated with dividing a continuous analog signal into a finite number of digital bits. For example, an 8-bit converter can only identify the input voltage to 1 part in 2^n, and there is an output uncertainty of $\pm$ 1/2 LSB as can be seen in Figure 3.

Resolution

The resolution of an A/D converter determines the number of bits available to the user. LSB step size is a function of the resolution and is very important in high resolution application.

The resolution of a D/A converter refers to the input logic levels utilized to control the analog output. Resolution is also considered in terms of 1 part of 2^n, where n is the number of controling bits.

SAR (Successive Approximation Register)

A digital control circuit used to control the operation of a successive approximation A/D converter.

Setting Time

The time elepsed from the application of a full scale step input in a circuit to the time when the output has entered and remained within a specified error band around its final value. This term is an important specification for operational amplifiers, analog multiplexers and D/A converters.

Settling Time

This is the time required after the specified change in input data, for the output of a D/A converter to reach and remain within the specified error band. Three parameters required to define the settling time are: step size, error band size, and settling time.

Slew Rate

The slew rate is the maximum rate of change during which an output can change due to the internal circuit characteristics. The slew rate is limited by internal charging currents and capacitances and is generally expressed in volts per microsecond.

SNR (Signal to Noise Ratio)

The signal-to-noise ratio is a ratio of the value of a signa to that of a noise. Usually these are RMS values, but for video signals, the value of signal is defined as peak-to-peak value and the value of noise is defined as RMS value. This is because, it is difficult to determine the RMS value for video signals. The signal-to-noise ratio for an A/D converter provides a good figure of merit for the dynamic accuracy of the device.

For measuring the SNR, a pure sine wave signal is supplied to the input of an A/D converter. This is sampled at a nonharmonic sampling rate and the output of the A/D converter is stored in memory. The output data of this converter is transformed into the frequiency domain with a fast fourier transformation and analyzed to determine the SNR. When analyzing the data, most of the noise will be located at the harmonic frequiency, so the SNR is a good estimate of total harmonic distortion. The SNR is expressed in dB as;

$$SNR = 20 \log_{10} \frac{Signal}{Noise}$$

Spurious Codes

A spurious code is a code which is largely inaccurate. For example, a full scale output generated for an input which is near mid- scale is a spurious code. If the output of an A/D converter contains such spurious code and is reconverted with a D/A converter, then the spurious code looks like a glitch.

Successive Approximation A/D Converter

An A/D conversion method that compares in sequence a series of binary weighted values with the analog input to produce an output digital word in just n steps. Where n is the resolution in bits. The process is efficient and is analogous to weighing the unknown quentity on a balance scale using a set of binary standard weights (See Figure 9).

Track-And-Hold

A sample-hold circuit which can continuously follow the input signal in the sample mode and then go into hold mode upon command (See Figure 8).

Tracking A/D Converter

A counter type analog-to-digital converter which can continuously follow the analog input at some specified maximum rate and continuously update its digital outputs as the inputs signal changes. The circuit uses a D/A converter driven by an up-down counter.

Two's Complement Code

A bipolar binary code in which positive and negative codes of the same magnitude sum to all zeros plus a carry.

Unipolar Mode

For a data converter, when the analog range includes values having one polarity only then it is called unipolar mode of converter.

V_{CC} (Positive Supply Voltage)

The positive power supply voltage required for device to operate.

V_{EE} (Negative Supply Voltage)

This is the negative supply voltage. Many converters will require both positive and negative supply voltage.

Weighted Current Source D/A Converter

This is a digital-to-analog converter whose design is based on a series of binary weighted transistor current sources which can be turned on or off by the digital inputs.

Zero Drift

For a data converter operating in the unipolar mode, the change in temperature of analog zero is called zero drift. Generally it is expressed in uV/°C.

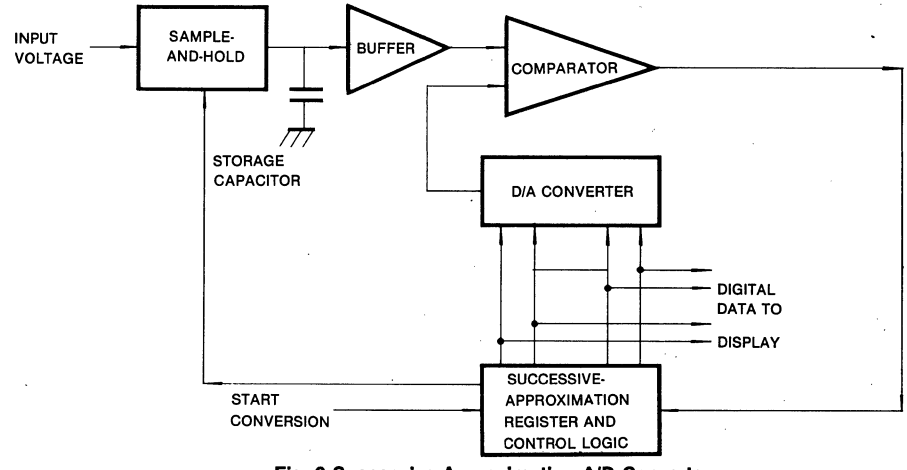
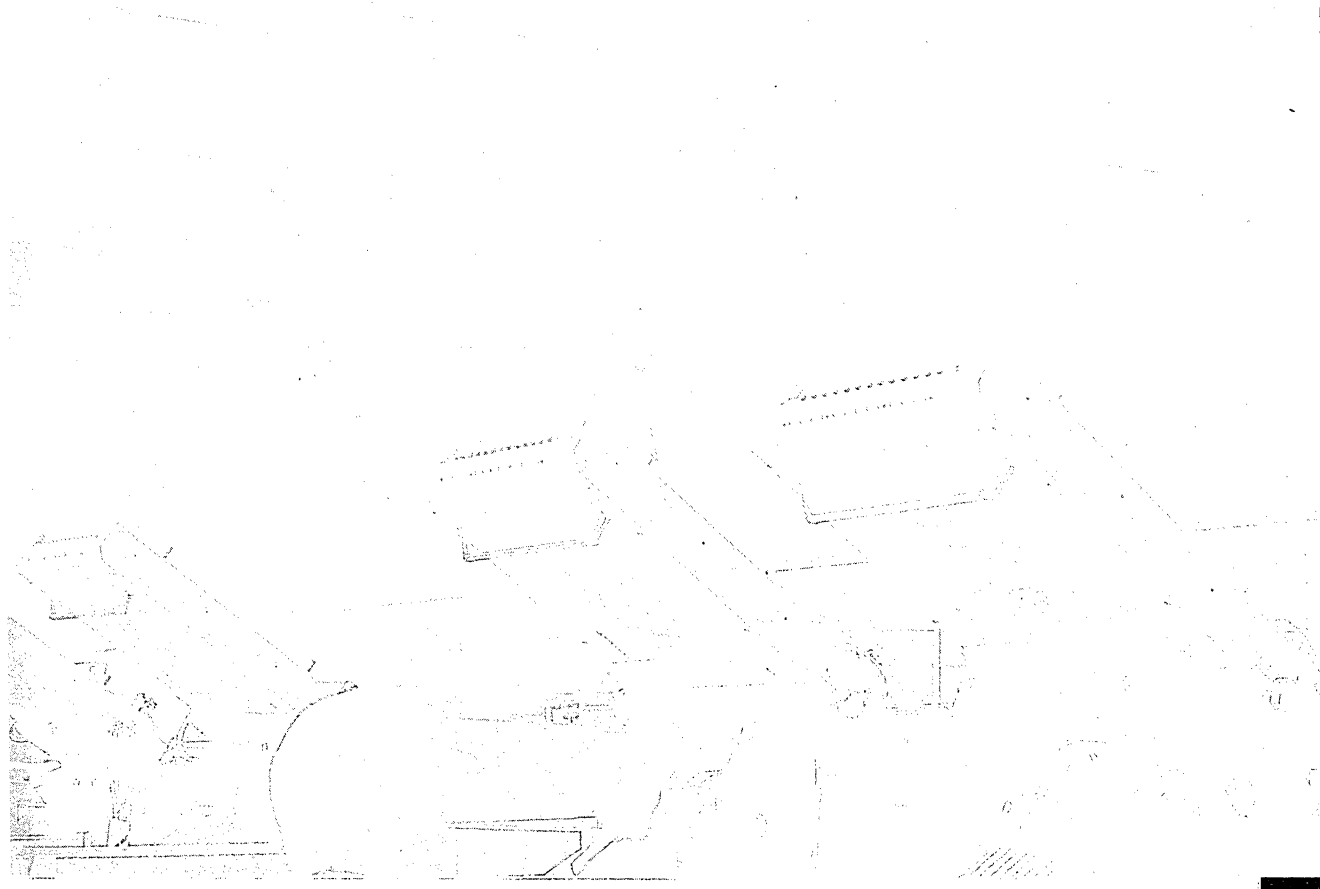
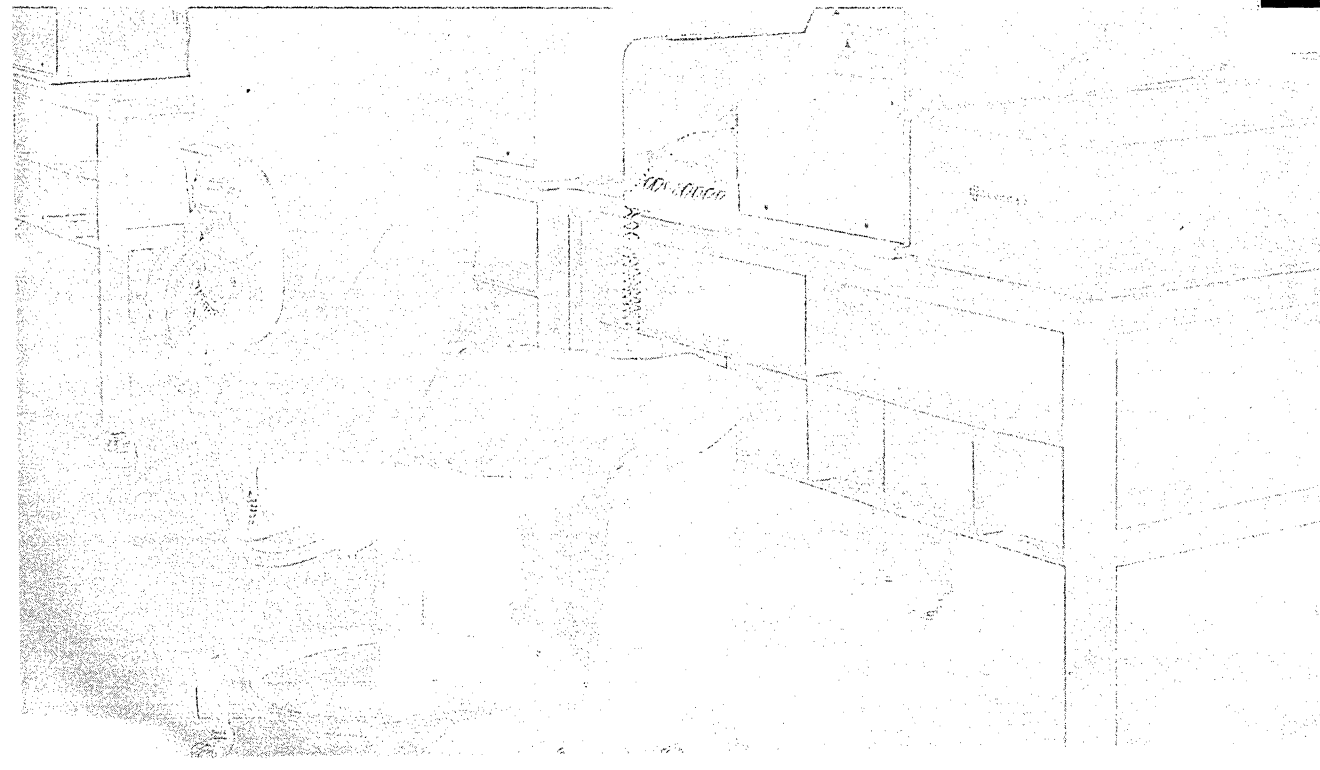


Fig. 9 Successive Approximation A/D Converter



PACKAGE DIMENSIONS

7



PACKAGE DIMENSIONS

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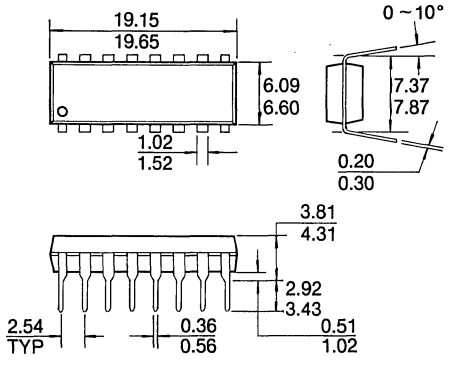
Unit: mm



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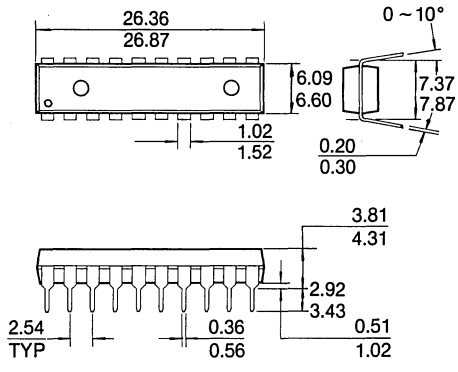

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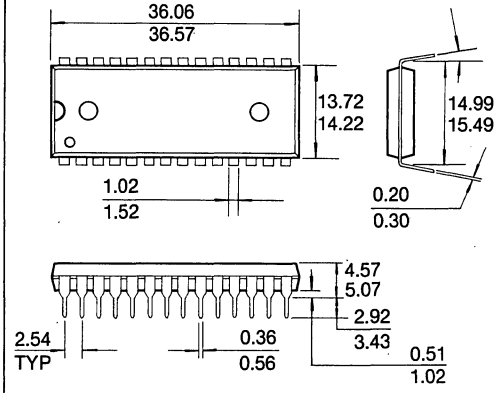
Unit: mm



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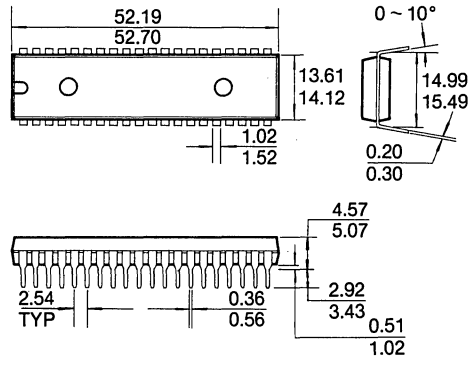

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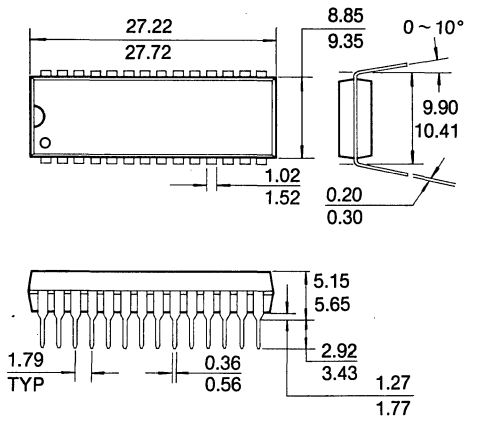

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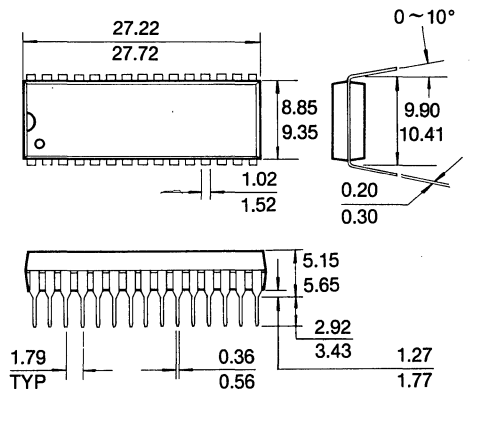

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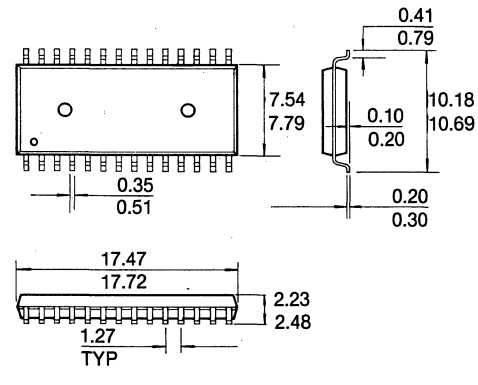
Unit: mm



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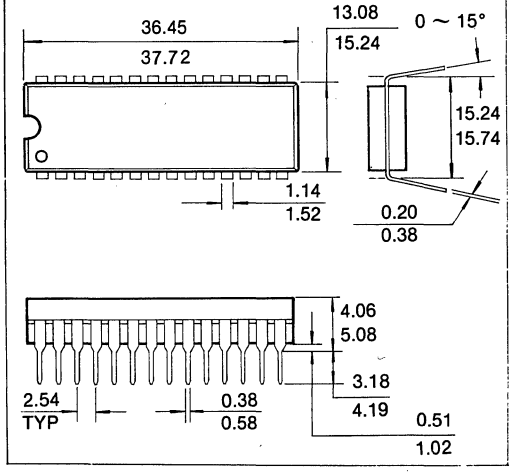
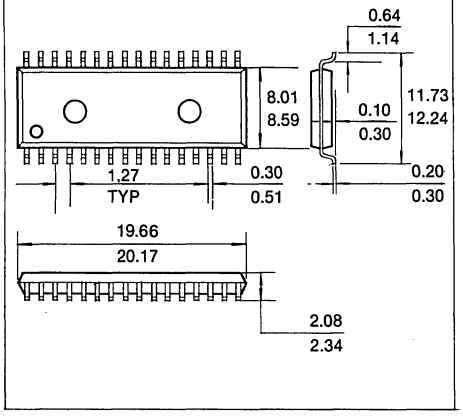
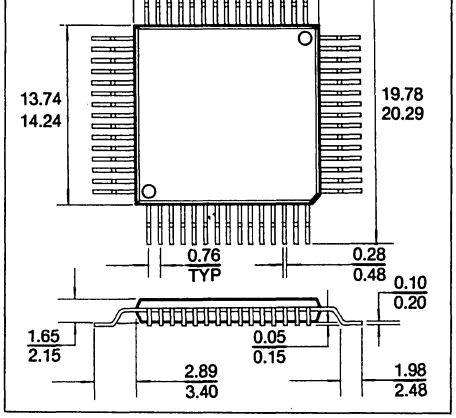


PACKAGE DIMENSIONS

32 SOP



60 FQP **Unit: mm**



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PRINTED IN KOREA
NOVEMBER 1989