LINE CARD ICs

DATABOOK

1st EDITION

SGS-THOMSON
MICROELECTRONICS

LINE CARD ICs

DATABOOK

1st EDITION

OCTOBER 1989

USE IN LIFE SUPPORT MUST BE EXPRESSLY AUTHORIZED 541

SGS-THOMSON' PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF SGS-THOMSON Microelectronics. As used herein:

1. Life support devices to systems are devices or systems which, are intended for surgical implant into the body to support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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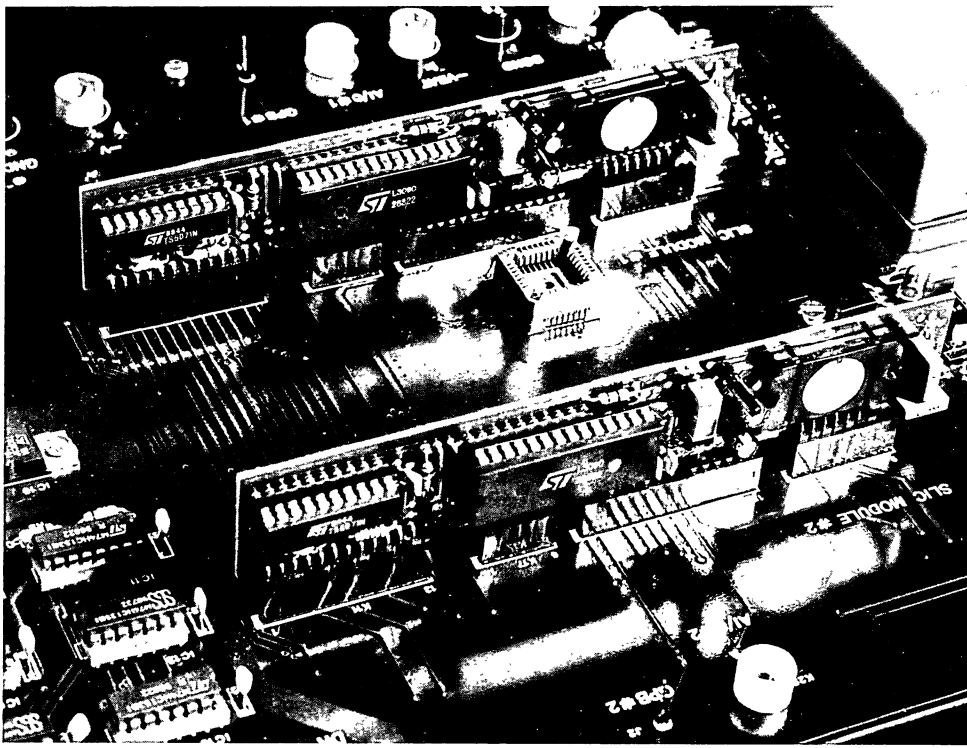
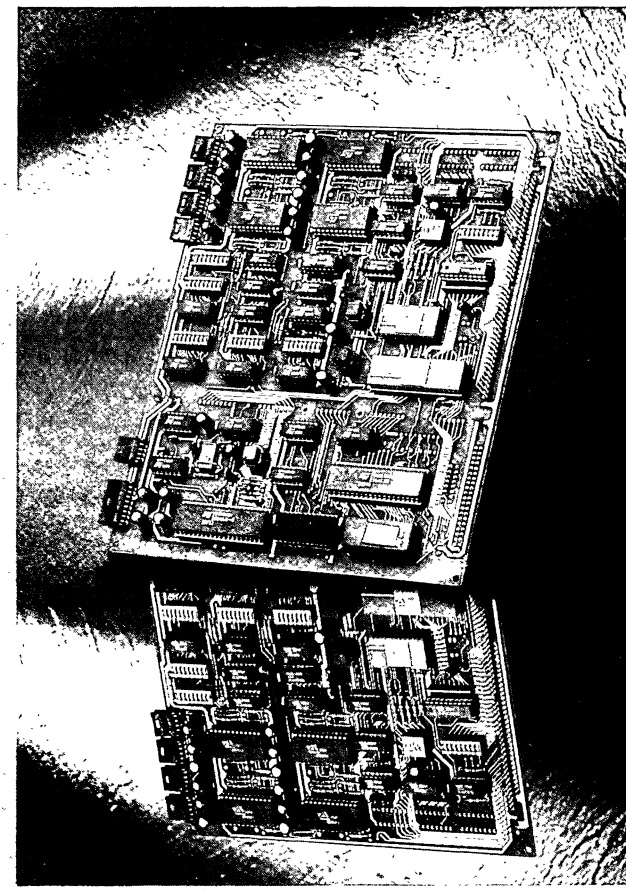
INTRODUCTION

SGS-THOMSON Microelectronics is a world leader in components for line card applications. Coupling vast system know-how, world class technologies and strong manufacturing experience, the company offers the most comprehensive range of solutions on the market-place.
Committed to offering solutions meeting all world standards, the company offers a complete family of single-chip codecs and filters, integrated first generation CMOS COMBO's, fully compatible with major manufacturers' families, and the programmable second generation COMBO® II.
Drawing on its world recognized bipolar capability SGS-THOMSON Microelectronics offers the most performant monolithic subscriber line interface circuits (SLIC) including the industry first internal ringing SLIC the L3000/L3XXX family.
Active in design at the system level the company offers a comprehensive family of switching matrix and special function devices, including our high performance conference call circuit, an industry first.
Active in a broad spectrum of application and technologies, the company employs state of the art processes including 3.0, 2.0 and 1.2 μm CMOS processes for mixed analog/digital functions and bipolar processes to 140V for high voltage applications such as SLICs. The company is also a world leader in BCD (Bipolar - CMOS - DMOS) technology providing the capability to mix low and high voltage applications on a single chip.
To simplify system design and application SGS-THOMSON Microelectronics offers comprehensive application support, including a full suite of application modules and software plus dedicated application support engineers and laboratories.



The SLIC-COMBO demo board allows design implementation and debug of line card using TS5070/1 COMBO II and SGS-THOMSON family of monolithic SLICs.



The M088/MI16 allows design implementation and debug of combined switching matrix/conference call functions.

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ALPHANUMERICAL INDEX

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PROTECTION DEVICES

TRANSIL

P_P (W)	V_{RM} (V)	Type		Case	Page
		Unidirectional	Bidirectional		
400/1 ms	5.8 to 376	BZW04../BZW04P..	BZW04..B/BZW04P..B	F126	717
600/1 ms	5.8 to 376	P6KE.. P,A	P6KE..CP, CA	CB-417	723
700/1 ms	10 to 110	P7T...	P7T...B	CB-417	729
1500/1 ms	5.8 to 376	1.5KE...P,A	1.5KE...CP, CA	CB-429	735
5000/1 ms	10 to 180	BZW50...	BZW50...B	AG	741

TRISIL

I_{PP} (A)	V_{BR} (V)	Types	Case	Page
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500/8-20 us	17 to 120	LS5018B/LS5060B/LS5120B,B1	MINIDIP	755
DUAL FUNCTION				
150/8-20μs	200	THBT 200D	TO220	759
150/8-20μs	—60	THDT 58D	TO220	763
TRIGGERED FUNCTION UNIDIRECTIONAL				
250/8-20 us	255	L3100B1	MINIDIP	767
TRIGGERED FUNCTION BIDIRECTIONAL				
250/8-20μs	100	L3121B	SIP.4	771

SURFACE MOUNT TRANSIL

P_P (W)	V_{RM} (V)	Type		Case	Page
		Unidirectional	Bidirectional		
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	5.5 to 171	—	SM4T..C, A	CB472	
600/1 ms	5.5 to 188	SM6T..., A	—	CB-472	781
	5.5 to 171	—	SM6T...C,A	CB-472	
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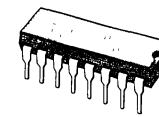
DATASHEETS

SGS-THOMSON MICROELECTRONICS

ETC5040
ETC5040A

PCM MONOLITHIC FILTER

- EXCEEDS ALL D3/D4 AND CCITT SPECIFICATIONS
- + 5V, – 5V POWER SUPPLIES
- LOW POWER CONSUMPTION :
  45mW (600Ω – 0dBm load)
  30mW (power amps disabled)
- POWER DOWN MODE : 0.5mW
- 20 dB GAIN ADJUST RANGE
- NO EXTERNAL ANTI-ALIASING COMPONENTS
- SIN x/x CORRECTION IN RECEIVE FILTER
- 50/60Hz REJECTION IN TRANSMIT FILTER
- TTL AND CMOS COMPATIBLE LOGIC
- ALL INPUTS PROTECTED AGAINST STATIC DISCHARGE DUE TO HANDLING



DIP16
(Ceramic)

ORDER CODES : ETC5040J
ETC5040AJ

DESCRIPTION

The ETC5040/ETC5040A filter is a monolithic circuit containing both transmit and receive filters specifically designed for PCM CODEC filtering applications in 8kHz sampled systems.

The filter is manufactured using double-poly silicon gate CMOS technology. Switched capacitor integrators are used to simulate classical LC ladder filters which exhibit low component sensitivity.

TRANSMIT FILTER STAGE

The transmit filter is fifth order elliptic low pass filter in series with a fourth order Chebychev high pass filter. It provides a flat response in the passband and rejection of signals below 200Hz and above 3.4kHz.

RECEIVE FILTER STAGE

The receive filter is a fifth order elliptic low pass filter designed to reconstruct the voice signal from the decoded/demultiplexed signal which, as a result of the sampling process, is a stair-step signal having the inherent sin x/x frequency response. The receive filter approximates the function required to compensate for the degraded frequency response and restores the flat pass-band response.

PIN CONNECTION

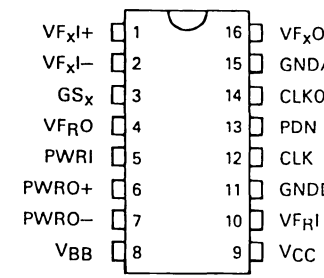
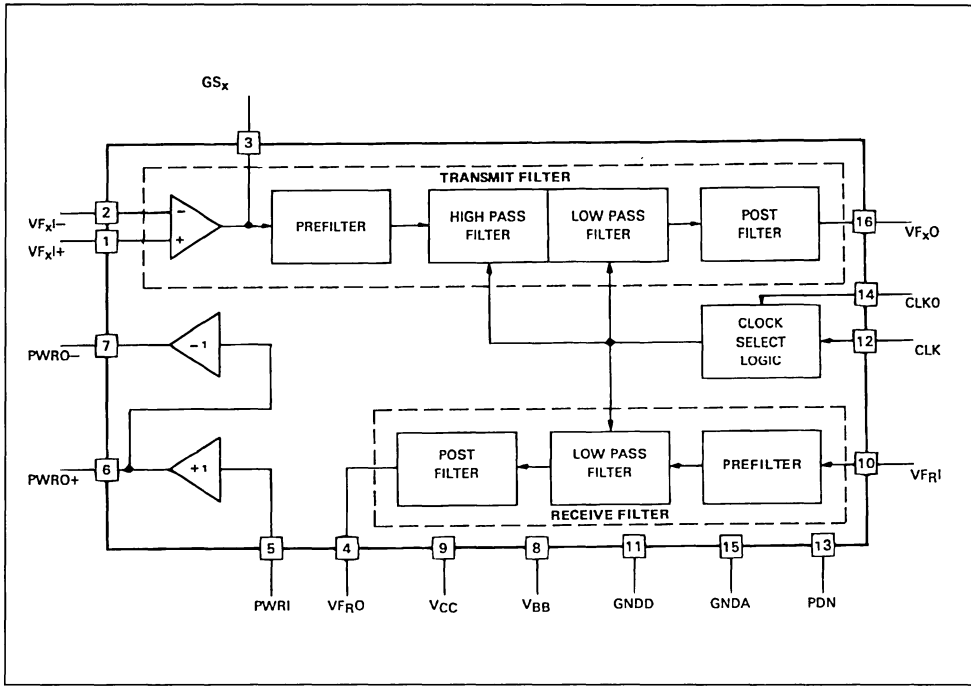


Figure 1 : Block Diagram.



PIN DESCRIPTION

Name	Pin Type	N°	Description
VF_XI^+	I	1	The Non-inverting Input to the Transmit Filter Stage
VF_xI^-	I	2	The Inverting Input to the Transmit Filter Stage
GS_x	O	3	The output used for gain adjustments of the transmit filter
VF_RO	O	4	The Low Power receive Filter Output. This pin can directly drive the receive port of an electronic hybrid.
PWRI	I	5	The Input to the Receive Filter Defferential Power Amplifier.
$PWRO^+$	O	6	The Non-inverting Output of the receive Filter Power Amplifier. This output can directly interface conventional transformer hybrids.
$PWRO^-$	O	7	The Inverting Output of the receive Filter Power Amplifier. This output can be used with $PWRO^+$ to differentially drive a transformer hybrid.
V_{BB}	S	8	The Negative Power Supply Pin. Recommended input is – 5 V.
V_{CC}	S	9	The Positive Power Supply Pin. The recommended input is 5 V.
VF_RI	I	10	The Input Pin for the Receive Filter Stage.
GNDD	GND	11	Digital Ground Input Pin. All digital signals are referenced to this pin.
CLK	I	12	Master Input Clock. Input frequency can be selected as 2.048 MHz, 1.544 MHz or 1.536 MHz.
PDN	I	13	The input pin used to power down the ETC5040/ETC5040A during idle periods. Logic 1 (V_{CC}) input voltage causes a power down condition. An Internal Pull-up is provided.
CLKO	I	14	This input pin selects internal counters in accordance with the CLK input clock frequency : CLK Connect CLKO to : 2048 kHz V_{CC} 1544 kHz GNDD 1536 kHz V_{BB} An Internal Pull-up is provided.
GNDA	GND	15	Analog Ground Input Pin. All analog signals are referenced to this pin. Not internally connected to GNDD.
VF_xO	O	16	The Output of the Transmit Filter Stage.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	± 7	V
V_{in}	Input Voltage	± 7	V
T_A	Operating Temperature Range	– 25 °C to + 125 °C	°C
T_{stg}	Storage Temperature	– 65 °C to + 150 °C	°C
P_D	Power Dissipation	1/Package	W
	Output Short-circuit Duration	Continuous	
	Lead Temperature	300	°C

DC ELECTRICAL CHARACTERISTICS

T_A = 0 °C to + 70 °C, V_{CC} = 5.0 V ± 5 %, V_{BB} = – 5.0 V ± 5 %, clock frequency is 2.048 MHz. Typical parameters are specified at T_A = + 25 °C, V_{CC} = 5.0 V, V_{BB} = – 5.0 V (unless otherwise specified). Digital interface voltages measured with respect to digital ground, GNDD. Analog voltages measured with respect to analog ground, GNDA.

POWER DISSIPATION

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{CCO}	V_{CC} Standby Current (PDN = V_{CC}, power down mode)	–	50	100	µA
I_{BBO}	V_{BB} Standby Current (PDN = V_{CC}, power down mode)	– 100	– 50	–	µA
I_{CC1}	V_{CC} Operating Current (PWRI = V_{BB}, power amp inactive)	–	3.0	4.0	mA
I_{BB1}	V_{BB} Operating Current (PWRI = V_{BB}, power amp inactive)	– 4.0	– 3.0	–	mA
I_{CC2}	V_{CC} Operating Current (note 1)	–	4.6	6.4	mA
I_{BB2}	V_{BB} Operating Current (note 1)	– 6.4	– 4.6	–	mA

DIGITAL INTERFACE

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{INC}	Input Current, CLK (0 V ≤ V_{IN} ≤ V_{CC})	– 10	–	10	µA
I_{INP}	Input Current, PDN (0 V ≤ V_{IN} ≤ V_{CC} – 2 V)	– 100	–	–	µA
I_{INO}	Input Current, CLKO (V_{BB} ≤ V_{IN} ≤ V_{CC} – 2 V)	– 10	–	– 0.1	µA
V_{IL}	Input Low Voltage, CLK, PDN	0	–	0.8	V
V_{IH}	Input High Voltage, CLK, PDN	2.2	–	V_{CC}	V
V_{ILO}	Input Low Voltage, CLKO	V_{BB}	–	V_{BB} + 0.5	V
V_{IIO}	Input Intermediate Voltage, CLKO	– 0.8	–	0.8	V
V_{IHO}	Input High Voltage, CLKO	V_{CC} – 0.5	–	V_{CC}	V

TRANSMIT INPUT AMP. OP.

Symbol	Parameter	Min.	Typ.	Max.	Unit
IB_xI	Input Leakage Current, VF_xI (V_{BB} ≤ VF_xI ≤ V_{CC})	– 100	–	100	nA
RI_xI	Input Resistance VF_xI (V_{BB} ≤ VF_xI ≤ V_{CC})	10	–	–	MΩ
VOS_xI	Input Offset Voltage, VF_xI (– 2.5 ≤ V_{IN} ≤ + 2.5 V)	– 20	–	20	mV
V_{CM}	Common-mode Range, VF_xI	– 2.5	–	2.5	V
CMRR	Common-mode Rejection Ratio (– 2.5 V ≤ V_{IN} ≤ 2.5 V)	60	–	–	dB
PSRR	Power Supply Rejection of V_{CC} or V_{BB}	60	–	–	dB
R_{OL}	Open Loop Output Resistance GS_x	–	1	–	kΩ
R_L	Minimum Load Resistance, GS_x	10	–	–	kΩ
C_L	Maximum Load Capacitance, GS_x	–	–	100	pF
V_{OxI}	Output Voltage Swing, GS_x (R_L ≥ 10 kΩ)	± 2.5	–	–	V
A_{VOL}	Open Loop Voltage Gain, GS_x (R_L ≥ 10 kΩ)	5000	–	–	V/V
F_C	Open Loop Unity Gain Bandwidth, GS_x	–	2	–	MHz

AC ELECTRICAL CHARACTERISTICS

T_A = 25 °C. All parameters are specified for a signal level of 0dBm0 at 1kHz. The 0dBm0 level is assumed to be 1.54Vrms measured at the output of the transmit or receive filter. (unless otherwise specified).

TRANSMIT FILTER (note 2)

Symbol	Parameter		Min.	Typ.	Max.	Unit
RL_x	Minimum Load Resistance					kΩ
	– 2.5 V < V_{OUT} < + 2.5 V		3	–	–	
	– 3.2 V < V_{OUT} < + 3.2 V		10	–	–	
CL_x	Load Capacitance VF_xO		–	–	100	pF
	Output Resistance, VF_xO		–	1	3.	Ω
PSRR1	V_{CC} Power Supply Rejection VF_xI (f = 1 kHz, VF_xI+ = 0 Vrms)		30	–	–	dB
PSRR2	V_{BB} Power Supply Rejection, VF_xO. (same as above)		35	–	–	dB
GA_x	Absolute Gain (f = 1 kHz)	ETC5040A				dB
		ETC5040	2.9	3.0	3.1	
			2.875	3.0	3.125	
GR_x	Gain Relative to GA_x					dB
	Below 50 Hz			–	– 35	
	50 Hz			– 41	– 35	
	60 Hz			– 35	– 30	
	200 Hz	ETC5040A	– 1.5	–	0	
		ETC5040	– 1.5	–	0.05	
	300 Hz to 3 kHz	ETC5040A	– 0.125	–	0.125	
		ETC5040	– 0.15	–	0.15	
	3.3 kHz	ETC5040A	– 0.35	–	0.03	
		ETC5040	– 0.35	–	0.125	
	3.4 kHz		– 0.70	–	– 0.1	
	4.0 kHz		–	– 15	– 14	
	4.6 kHz and above		–	–	– 32	
DA_x	Absolute Delay at 1 kHz		–	–	230	µs
	Differencial Envelope Delay from 1 kHz to 2.6 kHz		–	–	60	µs
DP_x1	Single Frequency Distortion Products		–	–	– 48	dB
DP_x2	Distortion at Maximum Signal Level 1.6 Vrms, 1 kHz Signal applied to VF_xI+, Gain = 20 dB, R_L = 10 kΩ		–	–	– 45	dB
NC_x1	Total C Message Noise at VF_xO		–	2	5	dBrncO
NC_x2	Total C Message Noise at VF_xO Gain setting Op Amp at 20 dB, non Inverting, Note 3, 0 °C ≤ T_A ≤ + 70 °C		–	3	6	dBrncO
GA_xT	Temperature Coefficient of 1 kHz Gain		–	0.0004	–	dB/°C
GA_xS	Supply Voltage Coefficient of 1 kHz Gain		–	0.01	–	dB/V
CT_{RX}	Crosstalk, Receive to Transmit 20 Log $\frac{VF_xO}{VF_RO}$ Receive Filter Output = 2.2 Vrms, VF_xI+ = 0 Vrms, f = 0.2 kHz to 3.4 kHz, Measure VF_xO		–	–	– 70	dB
GR_xL	Gaintracking Relative to GA_x					dB
	Output Level = + 3 dBmO		– 0.1	–	0.1	
	+ 2 dBmO to – 40 dBmO		– 0.05	–	0.05	
	– 40 dBmO to – 55 dBmO		– 0.1	–	0.1	

AC ELECTRICAL CHARACTERISTICS (continued)

RECEIVE FILTER (unless otherwise noted, the receive filter is preceded by a sin x/x filter with an input signal level of 1.54 Vrms).

Symbol	Parameter	Min.	Typ.	Max.	Unit
IB_R	Input Leakage Current, VF_RI (– 3.2 V ≤ VIN ≤ 3.2 V)	– 100	–	100	nA
RI_R	Input Resistance, VF_RI	10	–	–	MΩ
RO_R	Output Resistance, VF_RO	–	1	3	Ω
CL_R	Load Capacitance, VF_RO	–	–	100	pF
RL_R	Load Resistance, VF_RO	10	–	–	kΩ
PSRR3	Power Supply Rejection of V_{CC} or V_{BB} VF_RO (VF_RI connected to GNDA, f = 1 kHz)	 35	 –	 –	dB
VOS_RO	Output DC Offset, VF_RO (VF_RI connected to GNDA)	– 200	–	+ 200	mV
GA_R	Absolute Gain (f = 1 kHz) ETC5040A ETC5040	 – 0.1 – 0.125	 0 0	 0.1 0.125	dB
GR_R	Gain Relative to Gain at 1 kHz below 300 Hz 300 Hz to 3.0 kHz ETC5040A ETC5040 3.3 kHz 3.4 kHz 4.0 kHz 4.6 kHz and Above	– – 0.125 – 0.15 – 0.35 – 0.70 – –	– – – – – – –	0.125 0.125 0.15 0.03 – 0.1 – 14 – 32	dB
DA_R	Absolute Delay at 1 kHz	–	–	100	µs
DD_R	Differential Envelope Delay 1 kHz to 2.6 kHz	–	–	100	µs
DP_R1	Single Frequency Distortion Products (f = 1 kHz)	–	–	– 48	dB
DP_R2	Distortion at Maximum Signal Level 2.2 Vrms Input to Sin x/x Filter, f = 1 kHz, R_L = 10 kΩ	 –	 –	 – 45	dB
NC_R	Total C–message Noise at VF_RO	–	3	5	dBrnc0
GA_RT	Temperature Coefficient of 1 kHz Gain	–	0.0004	–	dB/°C
GA_RS	Supply Voltage Coefficient of 1 kHz Gain	–	0.01	–	dB/V
CT_{XR}	Crosstalk, Transmit to Receive 20 log $\frac{VF_RO}{VF_XO}$ (transmit filter output = 2. 2 Vrms, VF_RI = 0 Vrms, f = 0.3 kHz to 3.4 kHz, measure VF_RO)	 –	 – 80	 – 70	dB
GR_RL	Gaintraking Relative to GA_R Output Level = 3 dBm0 + 2 dBm0 to – 40 dBm0 – 40 dBm0 to – 55 dBm0	 – 0.1 – 0.05 – 0.1	 – – –	 0.1 0.05 0.1	dB

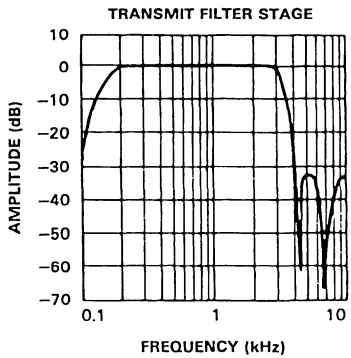
AC ELECTRICAL CHARACTERISTICS (continued)

RECEIVE OUTPUT POWER AMPLIFIER

Symbol	Parameter	Min.	Typ.	Max.	Unit
IBP	Input Leakage Current, PWRI (– 3.2 V ≤ V_{IN} ≤ 3.2 V)	0.1	–	3	µA
RIP	Input Resistance, PWRI	10	–	–	MΩ
ROP1	Output Resistance, PWRO +, PWRO – (amplifiers active)	–	1	–	Ω
CLP	Load Capacitance, PWRO +, PWRO –	–	–	500	pF
GA_P +	Gain, PWRI to PWRO + (R_L = 600 Ω connected between)	–	1	–	V/V
GA_P –	Gain, PWRI to PWRO – PWRO + and PWRO –, Input Level = 0 dBm0 (note 4)	–	– 1	–	V/V
GR_PL	Gaintraking Relative to OdBmO Output Level V = 2.05 Vrms, R_L = 600 Ω (notes 4, 5) V = 1.75 Vrms, R_L = 300 Ω (notes 4, 5)	 – 0.1 – 0.1	 – –	 0.1 0.1	dB
S/D_P	Signal/Distortion V = 2.05 Vrms, R_L = 600 Ω (notes 4, 5) V = 1.75 Vrms, R_L = 300 Ω (notes 4, 5)	 – –	 – –	 – 45 – 45	dB
VOSP	Output DC offset, PWRO +, PWRO – (PWRI connected to GNDA)	– 50	–	50	mV
PSRR5	Power Supply Rejection of V_{CC} or V_{BB} (PWRI connected to GNDA)	45	–	–	dB

Notes : 1. Maximum power consumption depend on the load impedance connected to the power amplifier. The specification listed assumes 0 dBm is delivred to 600Ω connected from PWRO + PWRO.
2. Transmit filter input op amp set to the non inverting unity gain mode, with VF_XI+ = 1.1Vrms, unless otherwise noted.
3. The 0dBm level for the filter is assumed to be 1.54Vrms measured at the output of the XMT or RCV filter.
4. The 0dBm0 level for the power amplifiers is load dependent. For R_L = – 600Ω to GNDA, the 0dBm0 level is 1.43Vrms measured at the amplifier output. For R_L = 300Ω the 0dBm0 level is 1.22Vrms.
5. VF_RO connected to PWRI, input signal applied to VF_RI.

TYPICAL PERFORMANCE CHARACTERISTICS



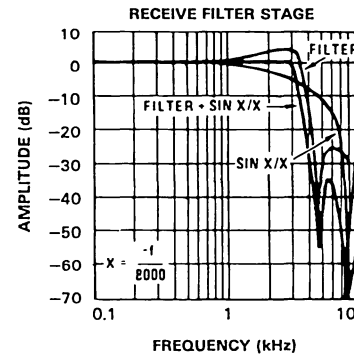
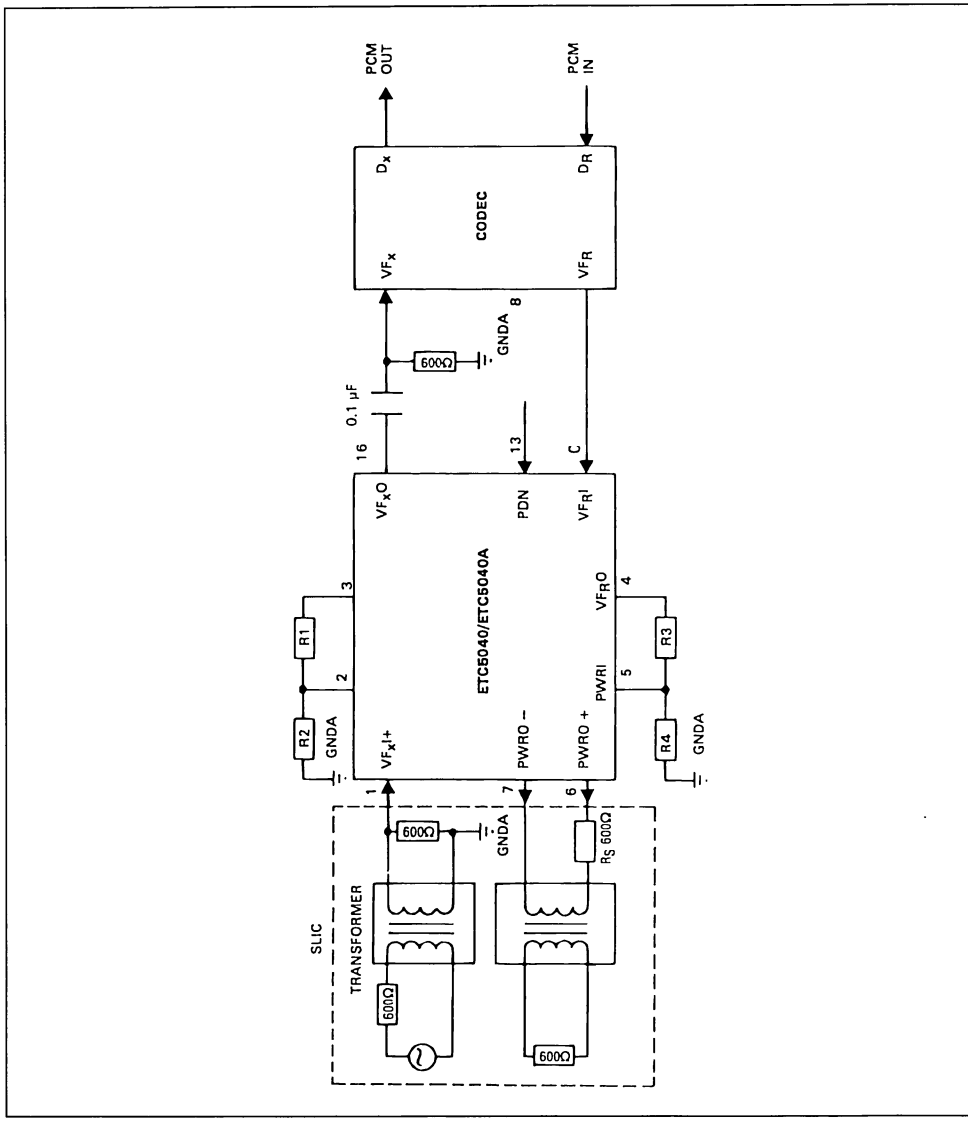


Figure 2 : Interface Circuit for CODEC.



Notes : 1. Transmit voltage gain = $\frac{R1 + R2}{R2} \times \sqrt{2}$ (the filter itself introduces a 3dB gain) (R1 + R2 ≥ 10kΩ).

2. Receive gain = $\frac{R4}{R3 + R4}$
(R3 + R4 ≥ 10kΩ)

3 In the configuration shown, the receive filter power amplifiers will drive a 600Ω T or R termination to a signal level of 8.5dBm. An alternative arrangement using a transformer winding ratio equivalent to 1 414 · 1 and 300Ω resistor R_S will provide a maximum signal level of 10dBm across 600Ω termination impedance.

FUNCTIONAL DESCRIPTION

The ETC 5040/ETC 5040A monolithic filter contains four main sections ; Transmit Filter, Receive Filter, Receive Filter Power Amplifier, and Frequency Divider/Select Logic (figure 1). A brief description of the circuit operation for each section is provided below.

TRANSMIT FILTER

The input stage of the transmit filter is a CMOS operational amplifier which provides an input resistance greater than 10MΩ, a voltage gain of greater than 5.000, low power consumption (less than 3mW), high power supply rejection, and is capable of driving a 10kΩ load in parallel with up to 25pF. The inputs and output of the amplifier are accessible for added flexibility. Non-inverting mode, inverting mode, or differential amplifier mode operation can be implemented with external resistors. It can also be connected to provide a gain of up to 20dB without degrading the overall filter performance.

The input stage is followed by a prefilter which is a two pole RC active low pass filter designed to attenuate high frequency noise before the input signal enters the switched-capacitor high pass and low pass filters.

A high pass filter is provided to reject 200Hz or lower noise which may exist in the signal path. The low pass portion of the switched-capacitor filter provides stopband attenuation which exceeds the D3 and D4 specifications as well as the CCITT G712 recommendations.

The output of the transmit filter, the postfilter, is also a two-pole RC active low pass filter which attenuates clock frequency noise by at least 40dB. The output of the transmit filter is capable of driving a ± 3.2V peak to peak signal into a 10kΩ load in parallel with up to 25pF.

RECEIVE FILTER

The input stage of the receive filter is a prefilter which is similar to the transmit prefilter. The prefilter attenuates high frequency noise that may be present on the receive input signal. A switched capacitor low pass filter follows the prefilter to provide the necessary passband flatness, stopband rejection and sin x/x gain correction. A postfilter which is similar to the transmit postfilter follows the low pass stage. It attenuates clock frequency noise and provides a low output impedance capable of directly driving an electronic subscriber-line-interface circuit.

RECEIVE FILTER POWER AMPLIFIERS

Two power amplifiers are also provided to interface to transformer coupled line circuits. These two amplifiers are driven by the output of the receive postfilter through gain setting resistors, R3, R4 (figure 2). The power amplifiers can be deactivated, when not required, by connecting the power amplifier input (pin 5) to the negative power supply V_{BB}. This reduces the total filter power consumption by approximately 10mW-20mW depending on output signal amplitude.

POWER DOWN CONTROL

A power down mode is also provided. A logic 1 power down command applied on the PDN pin (pin 13) will reduce the total filter power consumption to less than 1mW and turn the power amplifier outputs into high impedance state.

FREQUENCY DIVIDER AND SELECT LOGIC CIRCUIT

This circuit divides the external clock frequency down to the switching frequency of the low pass switched capacitor filters. The divider also contains a TTL-CMOS interface circuit which converts the external TTL clock level to the CMOS logic level required for the divider logic. This interface circuit can also be directly driven by CMOS logic.

A frequency select circuit is provided to allow the filter to operate with 2.048MHz, 1.544MHz or 1.536MHz clock frequencies. By connecting the frequency select pin CLKO (pin 14) to V_{CC}, a 2.048MHz clock input frequency is selected. Digital ground selects 1.544MHz and V_{BB} selects 1.536MHz.

APPLICATIONS INFORMATION

GAIN ADJUST

Figure 2 shows the signal path interconnections between the ETC5040/ETC5040A and single-channel CODEC. The transmit RC coupling components have been chosen both for minimum passband droop and to present the correct impedance to the CODEC during sampling.

Optimum noise and distortion performance will be obtained from the ETC5040/ETC5040A filter when operated with system peak overload voltages of ± 2.5V to ± 3.2V at VF_XO and VF_RO. When interfacing to a PCM CODEC with a peak overload voltage outside this range, further gain or attenuation may be required.

For example, the ETC5040/ETC5040A filter can be used with CODEC which has a 5.5V peak overload voltage. A gain stage following the transmit filter output and an attenuation stage following the CODEC output are required.

BOARD LAYOUT

Care must be taken in PCB layout to minimize power supply and ground noise. Analog ground (GNDA) of each filter should be connected to digital ground (GNDD) at a single point, which should be bypassed to both power supplies.

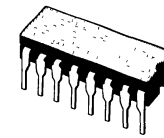
Further power supply decoupling adjacent to each filter and CODEC is recommended. Ground loops should be avoided, both between the GNDA traces of adjacent filters and CODECs.

SGS-THOMSON
MICROELECTRONICS

ETC5040X
ETC5040AX

EXTENDED TEMPERATURE RANGE PCM MONOLITHIC FILTER

- EXCEEDS ALL D3/D4 AND CCITT SPECIFICATIONS
- + 5 V, – 5 V POWER SUPPLIES
- LOW POWER CONSUMPTION :
- 45 mW (600 Ω -0 dBm load)
- 30 mW (power amps disabled)
- POWER DOWN MODE : 0.5 mW
- 20 dB GAIN ADJUST RANGE
- NO EXTERNAL ANTI-ALIASING COMPONENTS
- SIN x/x CORRECTION IN RECEIVE FILTER
- 50/60 Hz REJECTION IN TRANSMIT FILTER
- TTL AND CMOS COMPATIBLE LOGIC
- ALL INPUTS PROTECTED AGAINST STATIC DISCHARGE DUE TO HANDLING



DIP16
(Ceramic)

ORDER CODES : ETC5040X
ETC5040AX

DESCRIPTION

The ETC5040A filter is a monolithic circuit containing both transmit and receive filters specifically designed for PCM CODEC filtering applications in 8 kHz sampled systems.

The filter is manufactured using double-poly silicon gate CMOS technology. Switched capacitor integrators are used to simulate classical LC ladder filters which exhibit low component sensitivity.

TRANSMIT FILTER STAGE

The transmit filter is fifth order elliptic low pass filter in series with a fourth order Chebychev high pass filter. It provides a flat response in the passband and rejection of signals below 200 Hz and above 3.4 kHz.

RECEIVE FILTER STAGE

The receive filter is a fifth order elliptic low pass filter designed to reconstruct the voice signal from the decoded/demultiplexed signal which, as a result of the sampling process, is a stair-step signal having the inherent sin x/x frequency response. The receive filter approximates the function required to compensate for the degraded frequency response and restore the flat pass-band response.

PIN CONNECTION

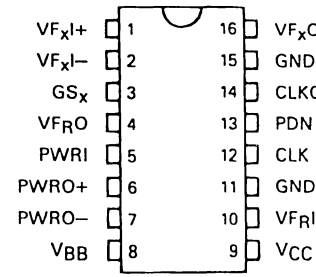
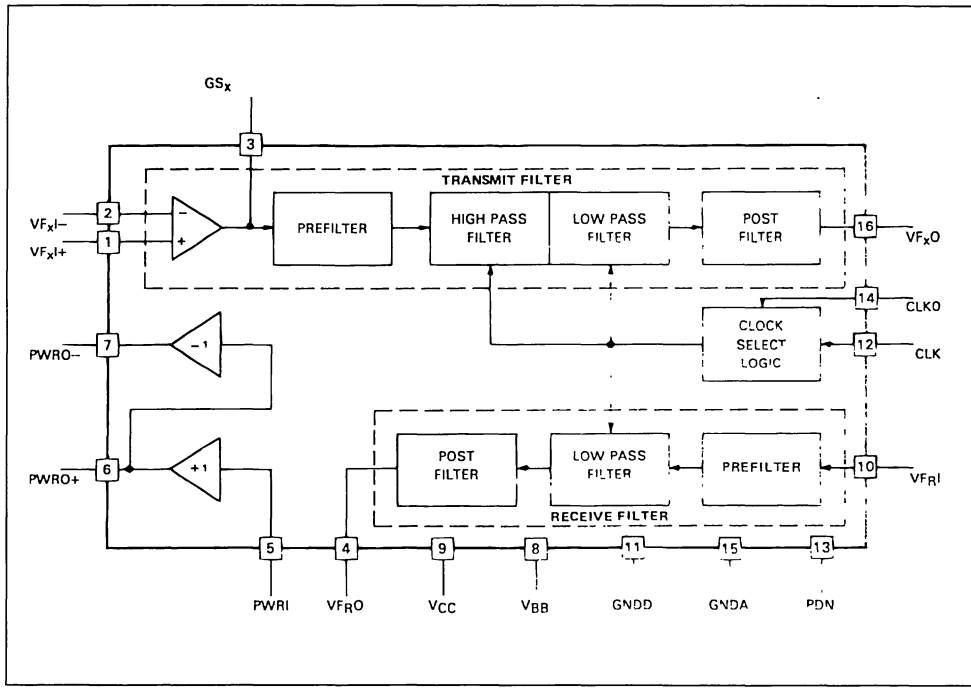


Figure 1 : Block Diagram.



PIN DESCRIPTION

Name	Pin Type	N°	Description
VF_xI^+	I	1	The Non-inverting Input to the Transmit Filter Stage
VF_xI^-	I	2	The Inverting Input to the Transmit Filter Stage
GS_x	O	3	The output used for gain adjustments of the transmit filter.
VF_RO	O	4	The Low Power Receive Filter Output. This pin can directly drive the receive port of an electronic hybrid.
PWRI	I	5	The Input to the Receive Filter Defferential Power Amplifier
$PWRO^+$	O	6	The Non-inverting Output of the Receive Filter Power Amplifier. This output can directly interface conventional transformer hybrids.
$PWRO^-$	O	7	The Inverting Output of the Receive Filter Power Amplifier. This output can be used with $PWRO^+$ to differentially drive a transformer hybrid.
V_{BB}	S	8	The Negative Power Supply Pin. Recommended input is – 5 V.
V_{CC}	S	9	The Positive Power Supply Pin. The recommended input is 5 V.
VF_RI	I	10	The Input Pin for the Receive Filter Stage
GNDD	GND	11	Digital Ground Input Pin. All digital signals are referenced to this pin.
CLK	I	12	Master Input Clock. Input frequency can be selected as 2.048 MHz, 1.544 MHz or 1.536 MHz.
PDN	I	13	The input pin used to power down the ETC5040/ETC5040A during idle periods. Logic 1 (V_{CC}) input voltage causes a power down condition. An internal pull-up is provided.
CLKO	I	14	This input pin selects internal counters in accordance with the CLK input clock frequency : **CLK** **Connect CLKO to :** 2048 kHz V_{CC} 1544 kHz GNDD 1536 kHz V_{BB} An internal pull-up is provided.
GNDA	GND	15	Analog Ground Input Pin. All analog signals are referenced to this pin. Not Internally connecded to GNDD.
VF_xO	O	16	The Output of the Transmit Filter Stage

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	± 7	V
V_{in}	Input Voltage	± 7	V
T_A	Operating Temperature Range	– 25 to + 125	°C
T_{stg}	Storage Temperature	– 65 to + 150	°C
P_D	Power Dissipation	1/Package	W
	Output Short-circuit Duration	Continuous	
	Lead Temperature	300	°C

DC ELECTRICAL CHARACTERSITICS

T_A = 40 °C to + 85 °C, V_{CC} = 5.0 V ± 5 %, V_{BB} = – 5.0 V ± 5 %, clock frequency is 2.048 MHz. Typical parameters are specified at T_A = + 25 °C, V_{CC} = 5.0 V, V_{BB} = – 5.0 V (unless otherwise specified). Digital interface voltages measured with respect to digital ground, GNDD. Analog voltages measured with respect to analog ground, GNDA.

POWER DISSIPATION

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{CCO}	V_{CC} Standby Current (PDN = V_{DD}, power down mode)	–	–	400	µA
I_{BBO}	V_{BB} Standby Current (PDN = V_{DD}, power down mode)	– 400	–	–	µA
I_{CC1}	V_{CC} Operating Current (PWRI = V_{BB}, power amp inactive)	–	–	5.0	mA
I_{BB1}	V_{BB} Operating Current (PWRI = V_{BB}, power amp inactive)	– 5.0	–	–	mA
I_{CC2}	V_{CC} Operating Current (note 1)	–	–	7.0	mA
I_{BB2}	V_{BB} Operating Current (note 1)	–7.0	–	–	mA

DIGITAL INTERFACE

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{INC}	Input Current, CLK (0 V ≤ V_{IN} ≤ V_{CC})	– 10	–	10	µA
I_{INP}	Input Current, PDN (0 V ≤ V_{IN} ≤ V_{CC} – 2 V)	– 100	–	–	µA
I_{INO}	Input Current, CLKO (V_{BB} ≤ V_{IN} ≤ V_{CC} – 2 V)	– 10	–	– 0.1	µA
V_{IL}	Input Low Voltage, CLK, PDN	0	–	0.8	V
V_{IH}	Input High Voltage, CLK, PDN	2.2	–	V_{CC}	V
V_{ILO}	Input Low Voltage, CLKO	V_{BB}	–	V_{BB} + 0.5	V
V_{IIO}	Input Intermediate Voltage, CLKO	– 0.8	–	0.8	V
V_{IHO}	Input High Voltage, CLKO	V_{CC} – 0.5	–	V_{CC}	V

TRANSMIT INPUT AMP. OP.

Symbol	Parameter	Min.	Typ.	Max.	Unit
IB_xI	Input Leakage Current, VF_xI (V_{BB} ≤ VF_xI ≤ V_{CC})	– 100	–	100	nA
RI_xI	Input Resistance VF_xI (V_{BB} ≤ VF_xI ≤ V_{CC})	10	–	–	MΩ
VOS_xI	Input Offset Voltage, VF_xI (– 2.5 ≤ V_{IN} ≤ + 2.5 V)	– 20	–	20	mV
V_{CM}	Common-mode Range, VF_xI	– 2.5	–	2.5	V
CMRR	Common-mode Rejection Ratio (– 2.5 V ≤ V_{IN} ≤ 2.5 V)	60	–	–	dB
PSRR	Power Supply Rejection of V_{CC} or V_{BB}	60	–	–	dB
R_{OL}	Open Loop Output Resistance GS_x	–	1	–	kΩ
R_L	Minimum Load Resistance, GS_x	10	–	–	kΩ
C_L	Maximum Load Capacitance, GS_x	–	–	100	pF
V_{OxI}	Output Voltage Swing, GS_x (R_L ≥ 10 kΩ)	± 2.5	–	–	V
A_{VOL}	Open Loop Voltage Gain, GS_x (R_I ≥ 10 kΩ)	5.000	–	–	V/V
F_C	Open Loop Unity Gain Bandwidth, GS_x	–	2	–	MHz

AC ELECTRICAL CHARACTERSITICS

T_A = – 40 °C to 85 °C All parameters are specified for a signal level of 0 dBm0 at 1 kHz. The 0 dBm0 level is assumed to be 1.54 Vrms measured at the output of the transmit or receive filter. (unless otherwise specified).

TRANSMIT FILTER (note 2)

Symbol	Parameter		Min.	Typ.	Max.	Unit
RL_x	Minimum Load Resistance					kΩ
	– 2.5 V < V_{OUT} < + 2.5 V		3	–	–	
	– 3.2 V < V_{OUT} < + 3.2 V		10	–	–	
CL_x	Load Capacitance VF_xO		–	–	100	pF
	Output Resistance, VF_xO		–	–	4	Ω
PSRR1	V_{CC} Power Supply Rejection VF_xI (f = 1 kHz, VF_xI+ = 0 Vrms)		30	–	–	dB
PSRR2	V_{BB} Power Supply Rejection, VF_xO. (same as above)		35	–	–	dB
GA_x	Absolute Gain (f = 1 kHz)					dB
		ETC5040A	2.850		3.100	
		ETC5040	2.875		3.125	
GR_x	Gain Relative to GA_x					dB
	Below 50 Hz		–	–	– 35	
	50 Hz		–	– 41	– 35	
	60 Hz		–	– 35	– 30	
	200 Hz	ETC5040	– 1.5	–	0.1	
		ETC5040A	– 1.5	–	0.05	
	300 Hz to 3 kHz	ETC5040	– 0.125	–	0.125	
		ETC5040A	– 0.15	–	0.15	
	3.3 kHz	ETC5040	– 0.35	–	0.15	
		ETC5040A	– 0.35	–	0.125	
	3.4 kHz		– 0.70	–	– 0.1	
	4.0 kHz		–	– 15	– 14	
	4.6 kHz and Above		–	–	– 32	
DA_x	Absolute Delay at 1 kHz		–	–	230	µs
	Differencial Envelope Delay from 1 kHz to 2.6 kHz		–	–	60	µs
DP_x1	Single Frequency Distortion Products		–	–	– 48	dB
DP_x2	Distortion at Maximum Signal Level 1.6 Vrms, 1 kHz Signal applied to VF_xI+, Gain = 20 dB, R_L = 10 kΩ		–	–	– 45	dB
NC_x1	Total C Message Noise at VF_xO		–	–	6	dBrncO
NCx2	Total C Message Noise at VF_xO Gain setting Op Amp at 20 dB, non Inverting, Note 3, 0 °C ≤ T_A ≤ + 70 °C		–	–	7	dBrncO
GA_xT	Temperature Coefficient of 1 kHz Gain		–	0.0004	–	dB/°C
GA_xS	Supply Voltage Coefficient of 1 kHz Gain		–	0.01	–	dB/V
CT_{RX}	Crosstalk, Receive to Transmit 20 Log $\frac{VF_xO}{VF_RO}$ Receive Filter Output = 2.2 Vrms, VF_xI+ = 0 Vrms, f = 0.2 kHz to 3.4 kHz, Measure VF_xO		–	–	– 70	dB
GR_xL	Gaintracking Relative to GA_x					dB
	Output Level = + 3 dBmO		– 0.1	–	0.1	
	+ 2 dBmO to – 40 dBmO		– 0.05	–	0.05	
	– 40 dBmO to – 55 dBmO		– 0.1	–	0.1	

AC ELECTRICAL CHARACTERSITICS (continued)

RECEIVE FILTER (unless otherwise noted, the receive filter is preceded by a sin x/x filter within an input signal level of 1.54 Vrms).

Symbol	Parameter		Min.	Typ.	Max.	Unit
IB_R	Input Leakage Current, VF_RI (– 3.2 V ≤ VIN ≤ 3.2 V)		– 100	–	100	nA
RI_R	Input Resistance, VF_RI		10	–	–	MΩ
RO_R	Output Resistance, VF_RO		–	–	4	Ω
CL_R	Load Capacitance, VF_RO		–	–	100	pF
RL_R	Load Resistance, VF_RO		10	–	–	kΩ
PSRR3	Power Supply Rejection of V_{CC} or V_{BB} (VF_RO VF_RI connected to GNDA, f = 1 kHz)		35	–	–	dB
VOS_RO	Output DC Offset, VF_RO (VF_RI connected to GNDA)		– 200	–	+ 200	mV
GA_R	Absolute Gain (f = 1 kHz)					dB
		ETC5040	– 0.15	–	0.15	
		ETC5040A	– 0.125	–	0.125	
GR_R	Gain Relative to Gain at 1 kHz below 300 Hz		–	–	0.15	dB
	300 Hz to 3.0 kHz	ETC5040	– 0.15	–	0.15	
		ETC5040A	– 0.175	–	0.175	
	3.3 kHz		– 0.35	–	0.03	
	3.4 kHz		– 0.70	–	– 0.1	
	4.0 kHz		–	–	– 14	
	4.6 kHz and above		–	–	– 32	
DA_R	Absolute Delay at 1 kHz		–	–	100	µs
DD_R	Differential Envelope Delay 1 kHz to 2.6 kHz		–	–	100	µs
DP_R1	Single Frequency Distortion Products (f = 1 kHz)		–	–	– 48	dB
DP_R2	Distortion at Maximum Signal Level 2.2 Vrms Input to Sin x/x Filter, f = 1 kHz, RL = 10 kΩ		–	–	– 45	dB
NC_R	Total C–message Noise at VF_RO		–	–	6	dBrnc0
GA_RT	Temperature Coefficient of 1 kHz Gain		–	0.0004	–	dB/°C
GA_RS	Supply Voltage Coefficient of 1 kHz Gain		–	0.01	–	dB/V
CT_{XR}	Crosstalk, Transmit to Receive 20 log $\frac{VF_RO}{VF_XO}$ (transmit filter output = 2. 2 Vrms, VF_RI = 0 Vrms, f= 0.3 kHz to 3.4 kHz, measure VF_RO)		–	– 80	– 70	dB
GR_RL	Gaintraking Relative to GA_P					dB
	Output Level = 3 dBm0		– 0.1	–	0.1	
	+ 2 dBm0 to – 40 dBm0		– 0.05	–	0.05	
	– 40 dBm0 to 55 dBm0		– 0.1	–	0.1	

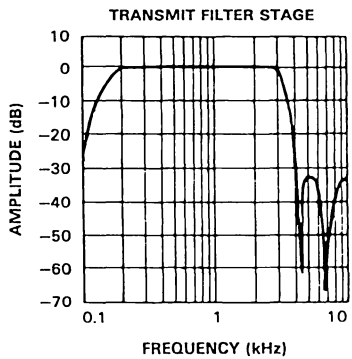
AC ELECTRICAL CHARACTERSITICS (continued)

RECEIVE OUTPUT POWER AMPLIFIER

Symbol	Parameter	Min.	Typ.	Max.	Unit
IBP	Input Leakage Current, PWRI (– 3.2 V ≤ V_{IN} ≤ 3.2 V)	0.1	–	4	µA
RIP	Input Resistance, PWRI	10	–	–	MΩ
ROP1	Output Resistance, PWRO +, PWRO – (amplifier active)	–	1	–	Ω
CLP	Load Capacitance, PWRO +, PWRO –	–	–	500	pF
GA_P +	Gain, PWRI to PWRO + (R_L = 600 Ω connected between)	–	1	–	V/V
GA_P –	Gain, PWRI to PWRO – PWRO + and PWRO –, Input, Level = 0 dBmO (note 4)	–	– 1	–	V/V
GR_PL	Gaintraking Relative to OdBmO Output Level V = 2.05 Vrms, R_L = 600 Ω (notes 4, 5) V = 1.75 Vrms, R_L = 300 Ω (notes 4, 5)	 – 0.1 – 0.1	 – –	 0.1 0.1	dB
S/D_P	Signal / Distortion V = 2.05 Vrms, R_L = 600 Ω (notes 4, 5) V = 1.75 Vrms, R_L = 300 Ω (notes 4, 5)	 – –	 – –	 – 45 – 45	dB
VOSP	Output DC Offset, PWRO +, PWRO – (PWRI connected to GNDA)	– 50	–	50	mV
PSRR5	Power Supply Rejection of V_{CC} ot V_{BB} (PWRI connected to GNDA)	45	–	–	dB

Notes : 1. Maximum power consumption depend on the load impedance connected to the power amplifier. The specification listed assumes 0 dBm is delivered to 600 Ω connected from PWRO + PWRO.
2. Transmit filter input op amp set to the non inverting unity gain mode, with VF_xI+ = 1 1 Vrms, unless otherwise noted.
3. The 0 dBm level for the filter is assumed to be 1.54 Vrms measured at the output of the XMT or RCV filter.
4. The 0 dBm0 level for the power amplifiers is load dependent. For R_L = – 600 Ω to GNDA, the 0 dBm0 level is 1.43 Vrms measured at the amplifier output. For R_L = 300 Ω the 0dBm0 level is 1.22 Vrms.
5. VF_RO connected to PWRI, input signal applied to VF_RI.

TYPICAL PERFORMANCE CHARACTERISTICS



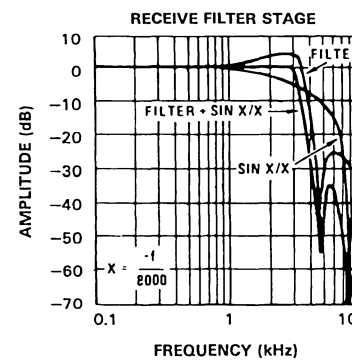
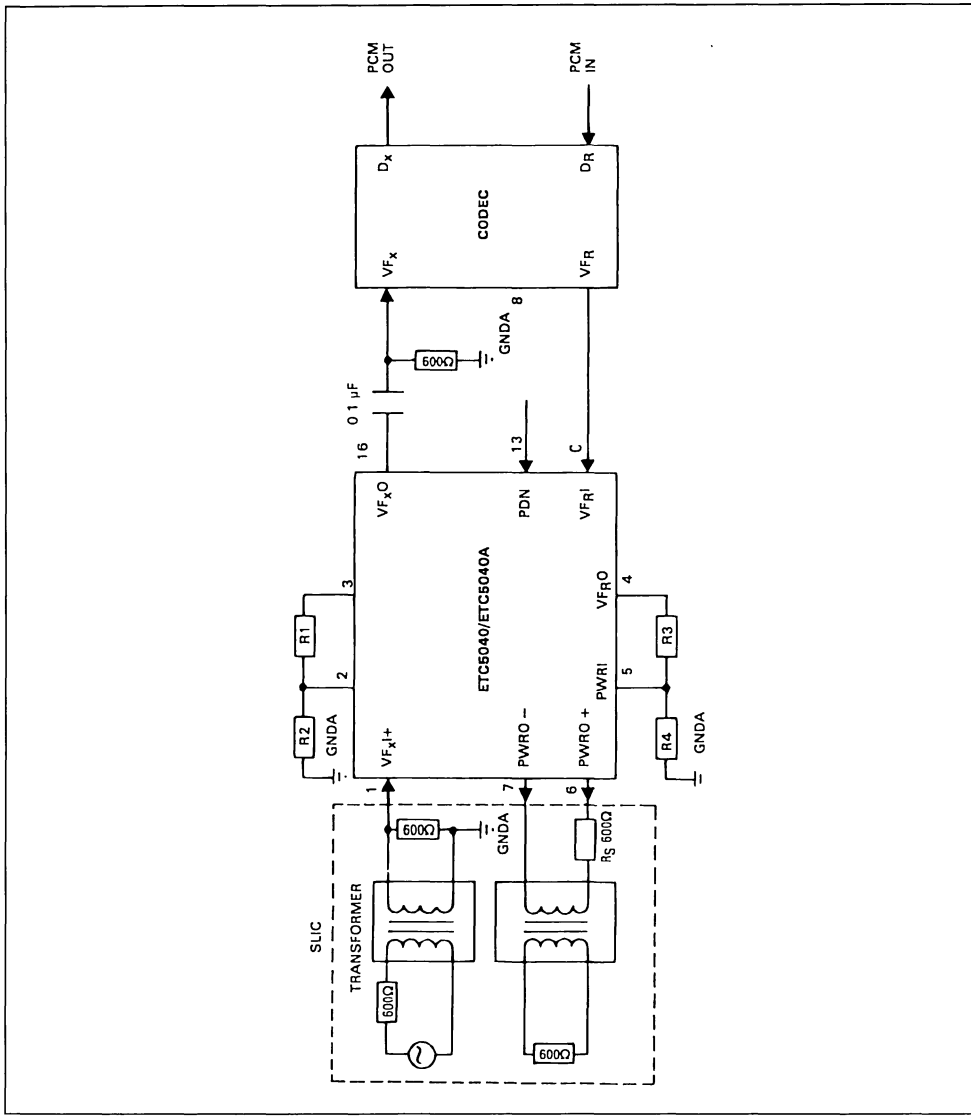


Figure 2 : Interface Circuit for CODEC.



Notes : 1. Transmit voltage gain = $\frac{R1 + R2}{R2}$ x √2 (the filter itself introduces a 3 dB gain) (R1 + R2 ≥ 10 KΩ).

2. Receive gain = $\frac{R4}{R3 + R4}$
(R3 + R4 ≥ 10 kΩ)
3. In the configuration shown, the receive filter power amplifiers will drive a 600 Ω T or R termination to a signal level of 8.5 dBm. An alternative arrangement using a transformer winding ratio equivalent to 1.414.1 and 300 Ω resistor R_S will provide a maximum signal level of 10 dBm across 600 Ω termination impedance.

FUNCTIONAL DESCRIPTION

ETC 5040A monolithic filter contains four main sections ; Transmit Filter, Receive Filter, Receive Filter Power Amplifier, and Frequency Divider/Select Logic (figure 1). A brief description of the circuit operation for each section is provided below.

TRANSMIT FILTER

The input stage of the transmit filter is a CMOS operational amplifier which provides an input resistance greater than 10 MΩ, a voltage gain of greater than 10.000 low power consumption (less than 3 mW), high power supply rejection, and is capable of driving a 10 kΩ load parallel with up to 25 pF. The inputs and output of the amplifier are accessible for added flexibility. Non-inverting mode, inverting mode, or differential amplifier mode operation can be implemented with external resistors. It can also be connected to provide a gain of up to 20 dB without degrading the overall filter performance.

The input stage is followed by a prefilter which is two-pole RC active low pass filter designed to attenuate high frequency noise before the input signal enters the switched-capacitor high pass and low pass filters.

A high pass filter is provided to reject 200 Hz or lower noise which may exist in the signal path. The low pass portion of the switched-capacitor filter provides stopband attenuation which exceeds the D3 and D4 specifications as well as the CCITT G712 recommendations.

The output of the transmit filter, the postfilter, is also a two-pole RC active low pass filter which attenuates clock frequency noise by at least 40 dB. The output of the transmit filter is capable of driving a ± 3.2 V peak to peak signal into a 10 kΩ load in parallel with up to 25 pF.

RECEIVE FILTER

The input stage of the receive filter is a prefilter which is similar to the transmit prefilter. The prefilter attenuates high frequency noise that may be present on the receive input signal. A switched capacitor low pass filter follows the prefilter to provide the necessary passband flatness, stopband rejection and sin x/x gain correction. A postfilter which is similar to the transmit postfilter follows the low pass stage. It attenuates clock frequency noise and provides a low output impedance capable of directly driving an electronic subscriber-line-interface circuit.

RECEIVE FILTER POWER AMPLIFIERS

Two power amplifiers are also provided to interface to transformer coupled line circuits. These two amplifiers are driven by the output of the receive postfilter through gain setting resistors, R3, R4 (figure 2). The power amplifiers can be deactivated, when not required, by connecting the power amplifier input (pin 5) to the negative power supply V_{BB}. This reduces the total filter power consumption by approximately 10 mW-20 mW depending on output signal amplitude.

POWER DOWN CONTROL

A power down mode is also provided. A logic 1 power down command applied on the PDN pin (pin 13) will reduce the total filter power consumption to less than 1 mW and turn the power amplifier outputs into high impedance state.

FREQUENCY DIVIDER AND SELECT LOGIC CIRCUIT

This circuit divides the external clock frequency down to the switching frequency of the low pass switched capacitor filters. The divider also contains a TTL-CMOS interface circuit which converts the external TTL clock level to the CMOS logic level required for the divider logic. This interface circuit can also be directly driven by CMOS logic.

A frequency select circuit is provided to allow the filter to operate with 2.048 MHz, 1.544 MHz or 1.536 MHz clock frequencies. By connecting the frequency select pin CLKO (pin 14) to V_{CC}, a 2.048 MHz clock input frequency is selected. Digital ground selects 1.544 MHz and V_{BB} selects 1.536 MHz.

APPLICATION INFORMATION

GAIN ADJUST

Figure 2 shows the signal path interconnections between the ETC5040/ETC5040A and single-channel CODEC. The transmit RC coupling components have been chosen both for minimum passband droop and to present the correct impedance to the CODEC during sampling.

Optimum noise and distortion performance will be obtained from the ETC5040/ETC5040A filter when operated with system peak overload voltages of ± 2.5 V to ± 3.2 V at VF_XO and VF_RO. When interfacing to a PCM CODEC with a peak overload voltage outside this range, further gain or attenuation may be required.

For example, the ETC5040/ETC5040A filter can be used with CODEC which has a 5.5 V peak overload voltage. A gain stage following the transmit filter output and an attenuation stage following the CODEC output are required.

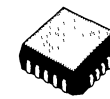
BOARD LAYOUT

Care must be taken in PCB layout to minimize power supply and ground noise. Analog ground (GNDA) of each filter should be connected to digital ground (GNDD) at a single point, which should be bypassed to both power supplies.

Further power supply decoupling adjacent to each filter and CODEC is recommended. Ground loops should be avoided, both between the GNDA traces of adjacent filters and CODECs.

PCM RECEIVE/TRANSMIT FILTER

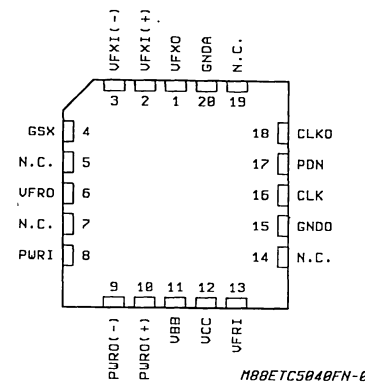
- EXCEEDS ALL D3/D4 AND CCITT SPECIFICATIONS
- + 5 V, – 5 V POWER SUPPLIES
- LOW POWER CONSUMPTION :
  45 mW (600 Ω - O dBm load)
  30 mW (power amps disabled)
- POWER DOWN MODE : 0.5mW
- 20 dB GAIN ADJUST RANGE
- NO EXTERNAL ANTI-ALIASING COMPONENTS
- SIN x/x CORRECTION IN RECEIVE FILTER
- 50/60 Hz REJECTION IN TRANSMIT FILTER
- TTL AND CMOS COMPATIBLE LOGIC
- ALL INPUTS PROTECTED AGAINST STATIC DISCHARGE DUE TO HANDLING



PLCC20

ORDER CODES : ETC5040FN
ETC5040FN/A

PIN CONNECTION



DESCRIPTION

The ETC5040FN ETC5040FN/A filter is a monolithic circuit containing both transmit and receive filters specifically designed for PCM CODEC filtering applications in 8 kHz sampled systems.

The filter is manufactured using double-poly silicon gate CMOS technology. Switched capacitor integrators are used to simulate classical LC ladder filters which exhibit low component sensitivity.

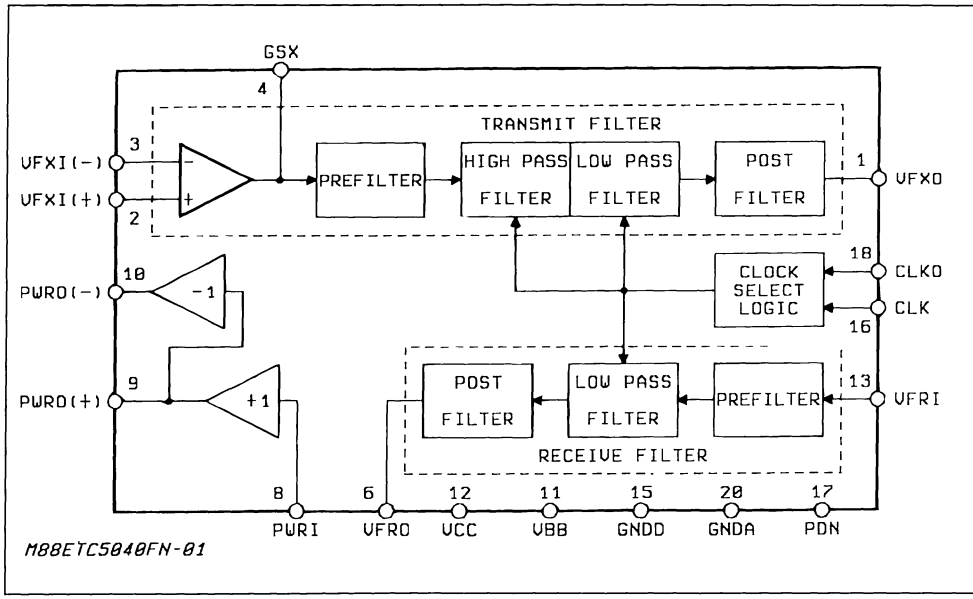
TRANSMIT FILTER STAGE

The transmit filter is fifth order elliptic low pass filter in series with a fourth order Chebychev high pass filter. It provides a flat response in the pass-band and rejection of signals below 200 Hz and above 3.4 kHz.

RECEIVE FILTER STAGE

The receive filter is a fifth order elliptic low pass filter designed to reconstruct the voice signal from the decoded/demultiplexed signal which, as a result of the sampling process, is a stair-step signal having the inherent sin x/x frequency response. The receive filter approximates the function required to compensate for the degraded frequency response and restore the flat pass-band response.

Figure 1 : Block Diagram.



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	V_{CC} to GNDA	7	V
V_{BB}	V_{BB} to GNDA	– 7	V
V_{IN}, V_{OUT}	Voltage at any Analog Input or Output	V_{CC} + 0.3 to V_{BB} – 0.3	V
	Voltage at any Digital Input or Output	V_{CC} + 0.3 to GNDA – 0.3	V
T_{oper}	Operating Temperature Range	– 25 to + 125	°C
T_{stg}	Storage Temperature Range	– 65 to + 150	°C
	Lead Temperature (soldering, 10 seconds)	300	°C

PIN DESCRIPTION

Name	Pin Type *	N°	Function	Description
VF_XO	O	1		The output of the transmit filter stage.
VF_XI+	I	2		The non-inverting input to the transmit filter stage.
VF_XI-	I	3		The inverting input to the transmit filter stage.
GS_X	O	4		The output used for gain adjustments of the transmit filter.
VF_RO	O	6		The low power receive filter output. This pin can directly drive the receive port of an electronic hybrid.
PWRI	I	8		The input to the receive filter differential power amplifier.
PWRO+	O	9		The non-inverting output of the receive filter power amplifier. This output can directly interface conventional transformer hybrids.
PWRO–	O	10		The inverting output of thr receive filter power amplifier. This output can be used with PWRO+ to differentially drive a transformer hybrid.
V_{BB}	S	11		The negative power supply pin. Recommended input is – 5 V.
V_{CC}	S	12		The positive power supply pin. The recommended input is 5 V.
VF_RI	I	13		The input pin for the receive filter stage.
GNDD	GND	15		Digital Ground Input Pin. All digital signals are referenced to this pin.
CLK	I	16		Master Input Clock. Input frequency can be selected as 2.048 MHz, 1.544 MHz or 1.536 MHz.
PDN	I	17		The input pin used to power down the ETC5040FN *, ETC5040FN/A during idle periods. Logic 1 (V_{CC}) input voltage causes a power down condition. An internal pull-up is provided.
CLKO	I	18		This input pin selects internal counters in accordance with the CLK input clock frequency : **CLK** **Connect CLKO to :** 2048 kHz V_{CC} 1544 kHz GNDD 1536 kHz V_{BB} An internal pull-up is provided.
GNDA	GND	20		Analog Ground Input Pin. All analog signals are referenced to this pin. Not internally connected to GNDD.

* I : Input, O Output, S : Power supply.

ELECTRICAL OPERATING CHARACTERISTICS V_{CC} = 5.0 V ± 5 %, V_{BB} = – 5.0 V ± 5 %, GNDA = 0 V, T_A = 0 °C to 70 °C (unless otherwise noted) ; typical characteristics specified at T_A = 25 °C ; all signals are referenced to GNDA.

POWER DISSIPATION

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{CCO}	V_{CC} Standby Current (PDN = V_{DD}, power down mode)	–	50	100	µA
I_{BBO}	V_{BB} Standby Current (PDN = V_{DD}, power down mode)	– 100	– 50	–	µA
I_{CC1}	V_{CC} Operating Current (PWRI = V_{BB}, power amp inactive)	–	3.0	4.0	mA
I_{BB1}	V_{BB} Operating Current (PWRI = V_{BB}, power amp inactive)	– 4.0	– 3.0	–	mA
I_{CC2}	V_{CC} Operating Current (note 1)	–	4.6	6.4	mA
I_{BB2}	V_{BB} Operating Current (note 1)	– 6.4	– 4.6	–	mA

DIGITAL INTERFACE

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{INC}	Input Current, CLK (0 V ≤ V_{IN} ≤ V_{CC})	– 10	–	10	µA
I_{INP}	Input Current, PDN (0 V ≤ V_{IN} ≤ V_{CC}–2 V)	– 100	–	–	µA
I_{INO}	Input Current, CLKO (V_{BB} ≤ V_{IN} ≤ V_{CC}–2 V)	– 10	–	– 0.1	µA
V_{IL}	Input Low Voltage, CLK, PDN	0	–	0.8	V
V_{IH}	Input High Voltage, CLK, PDN	2.2	–	V_{CC}	V
V_{ILO}	Input Low Voltage, CLKO	V_{BB}	–	V_{BB}+0.5	V
V_{IIO}	Input Intermediate Voltage, CLKO	– 0.8	–	0.8	V
V_{IHO}	Input High Voltage, CLKO	V_{CC}–0.5	–	V_{CC}	V

TRANSMIT INPUT AMP. OP.

Symbol	Parameter	Min.	Typ.	Max.	Unit
IB_XI	Input Leakage Current, VF_XI (V_{BB} ≤ VF_XI ≤ V_{CC})	– 100	–	100	nA
RI_XI	Input Resistance VF_XI (V_{BB} ≤ VF_XI ≤ V_{CC})	10	–	–	MΩ
VOS_XI	Input Offset Voltage, VF_XI (– 2.5 V ≤ V_{IN} ≤ + 2.5 V)	– 20	–	20	mV
V_{CM}	Common-mode Range, VF_XI	– 2.5	–	2.5	V
CMRR	Common-mode Rejection Ratio (– 2.5 V ≤ V_{IN} ≤ 2.5 V)	60	–	–	dB
PSRR	Power Supply Rejection of V_{CC} or V_{BB}	60	–	–	dB
R_{OL}	Open Loop Output Resistance GS_X	–	1	–	kΩ
R_L	Minimum Load Resistance, GS_X	10	–	–	kΩ
CL	Maximum Load Capacitance, GSX	–	–	100	pF
VO_XI	Output Voltage Swing, GS_X (R_L ≥ 10 kΩ)	± 2.5	–	–	V
A_{VOL}	Open Loop Voltage Gain, GS_X (R_l ≥ 10 kΩ)	5.000	–	–	V/V
F_C	Open Loop Unity Gain Bandwidth, GS_X	–	2	–	MHz

AC ELECTRICAL CHARACTERISTICS T_A = + 25 °C. All parameters are specified for a signal level of 0 dBm0 at 1 kHz. The 0 dBm0 level is assumed to be 1.54 Vrms measured at the output of the transmit or receive filter. (unless otherwise specified)

TRANSMIT FILTER (note 2)

Symbol	Parameter		Min.	Typ.	Max.	Unit
RL_X	Minimum Load Resistance					kΩ
	– 2.5 V < V_{out} < + 2.5 V		3	–	–	
	– 3.2 V < V_{out} < + 3.2 V		10	–	–	
CL_X	Load Capacitance, VF_XO		–	–	100	pF
	Output Resistance, VF_XO		–	1	3	Ω
PSRR1	V_{CC} Power Supply Rejection VF_XI (f = 1 kHz, VF_XI+ = 0 Vms)		30	–	–	dB
PSRR2	V_{BB} Power Supply Rejection, VF_XO (same as above)		35	–	–	dB
GA_X	Absolute Gain (f = 1 kHz)					dB
		ETC5040FN/A	2.9	3.0	3.1	
		ETC5040FN	2.875	3.0	3.125	
GR_X	Gain Relative to GA_X					dB
	Below 50 Hz		–	–	– 35	
	50 Hz		–	– 41	– 35	
	60 Hz		–	– 35	– 30	
	200 Hz	ETC5040FN/A	– 1.5	–	0	
		ETC5040FN	– 1.5	–	0.05	
	300 Hz to 3 kHz	ETC5040FN/A	– 0.125	–	0.125	
		ETC5040FN	– 0.15	–	0.15	
	3.3 kHz	ETC5040FN/A	– 0.35	–	0.03	
		ETC5040FN	– 0.35	–	0.125	
	3.4 kHz		– 0.70	–	– 0.1	
	4.0 kHz		–	– 15	– 14	
	4.6 kHz and Above		–	–	– 32	
DA_X	Absolute Delay at 1 kHz		–	–	230	µs
	Differential envelope Delay from 1 kHz to 2.6 kHz		–	–	60	µs
DP_X1	Single Frequency Distortion Products		–	–	– 48	dB
DP_X2	Distortion at Maximum Signal Level 1.6 Vrms, 1 kHz Signal Applied to VF_XI+, gain = 20 dB, R_L = 10 kΩ		–	–	– 45	dB
NC_X1	Total C Message Noise at VF_XO		–	2	5	dBrnco
NC_X2	Total C message Noise at VF_XO Gain Setting 0p Amp at 20 dB, non inverting, note, 3.0 °C ≤ T_A ≤ + 70 °C		–	3	6	dBrnco
GA_XT	Temperature Coefficient of 1 kHz Gain		–	0.0004	–	dB/°C
GA_XS	Supply Voltage Coefficient of 1 kHz Gain		–	0.01	–	dB/V
CT_{RX}	Crosstalk, receive to transmit 20 $\log\frac{VF_XO}{VF_RO}$					dB
	Receive Filter Output = 2.2 Vrms, VFX_XI+ = 0 Vrms, f = 0.2 kHz to 3.4 kHz, measure VF_XO		–	–	– 70	
GR_XL	Gaintracking Relative to GA_X					dB
	Output Level = + 3 dBm0		– 0.1	–	0.1	
	+ 2 dBm0 to – 40 dBm0		– 0.05	–	0.05	
	– 40 dBm0 to – 55 dBm0		– 0.1	–	0.1	

AC ELECTRICAL CHARACTERISTICS (continued)

RECEIVE FILTER (unless otherwise noted, the receive filter is preceeded by a sin X/X filter with an input signal level of 1.54 Vrms)

Symbol	Parameter	Min.	Typ.	Max.	Unit
IB_R	Input Leakage Current, VF_RI (– 3.2 V ≤ V_{IN} ≤ 3.2 V)	– 100	–	100	nA
RI_R	Input Resistance, VF_RI	10	–	–	MΩ
RO_R	Output Resistance, VF_RO	–	1	3	Ω
CL_R	Load Capacitance, VF_RO	–	–	100	pF
RL_R	Load Resistance, VF_RO	10	–	–	kΩ
PSRR3	Power Supply Rejection of V_{CC} or V_{BB} (VF_RO, VF_RI Connected to GNDA, f = 1 kHz)	35	–	–	dB
VOS_RO	Output DC Offset, VF_RO (VF_RI connected to GNDA)	– 200	–	+ 200	mV
GA_R	Absolute Gain (f = 1 kHz) ETC5040FN/A ETC5040FN	 – 0.1 – 0.125	 0 0	 0.1 0.125	dB
GR_R	Gain Relative to Gain at 1 kHz Below 300 Hz 300 Hz to 3.0 kHz ETC5040FN/A ETC5040FN 3.3 kHz 3.4 kHz 4.0 kHz 4.6 kHz and Above	– – 0.125 – 0.15 – 0.35 – 0.70 – –	– – – – – – –	0.125 0.125 0.15 0.03 – 0.1 – 14 – 32	dB
DA_R	Absolute Delay at 1 kHz	–	–	100	µs
DD_R	Differential Envelope Delay 1 kHz to 2.6 kHz	–	–	100	µs
DP_R1	Single Frequency Distortion Products (f = 1 kHz)	–	–	– 48	dB
DP_R2	Distortion at Maximum Signal Level 2.2 Vrms Input to Sin X/X Filter, f = 1 kHz, R_L = 10 kΩ	–	–	– 45	dB
NC_R	Total C Message Noise at VF_RO	–	3	5	dBrnc0
GA_RT	Temperature Coefficient of 1 kHz Gain	–	0.0004	–	dB/°C
GA_RS	Supply Voltage Coefficient of 1 kHz Gain	–	0.01	–	dB/V
CT_{XR}	Crosstalk, transmit to receive 20 log $\frac{VF_RO}{VF_XO}$ (transmit filter output = 2.2 Vrms, VF_RI = 0 Vrms, f = 0.3 kHz to 3.4 kHz, measure VF_RO)	–	– 80	– 70	dB
GR_RL	Gaintracking Relative to GA_R Output Level = 3 dBm0 + 2 dBm0 to – 40 dBm0 – 40 dBm0 to 55 dBm0	 – 0.1 – 0.05 – 0.1	 – – –	 0.1 0.05 0.1	dB

RECEIVE OUTPUT POWER AMPLIFIER

Symbol	Parameter	Min.	Typ.	Max.	Unit
IBP	Input Leakage Current, PWRI (– 3.2 V ≤ V_{IN} ≤ 3.2 V)	0.1	–	3	µA
RIP	Input Resistance, PWRI	10	–	–	MΩ
ROP1	Output Resistance, PWRO+, PWRO– (amplifiers active)	–	1	3	Ω
CLP	Load Capacitance, PWRO+, PWRO–	–	–	500	pF

AC ELECTRICAL CHARACTERISTICS (continued)

RECEIVER OUTPUT POWER AMPLIFIER (continued)

Symbol	Parameter	Min.	Typ.	Max.	Unit
GAp+ GAp–	Gain, PWRI to PWRO+ (R_L = 600 Ω connected between) Gain, PWRI to PWRO– PWRO+ and PWRO– input, level = 0 dBm0 (note 4)	– –	1 – 1	– –	V/V V/V
GRpL	Gaintrakıng Relative to 0dBm0 Output Level V = 2.05 Vrms, R_L = 600 Ω (notes 4, 5) V = 1.75 Vrms, R_L = 300 Ω (notes 4, 5)	 – 0.1 – 0.1	 – –	 0.1 0.1	dB
S/Dp	Signal/distortion V = 2.05 Vrms, R_L = 600 Ω (notes 4, 5) V = 1.75 Vrms, R_L = 300 Ω (notes 4, 5)	 – –	 – –	 – 45 – 45	dB
VOSP	Output DC Offset, PWRO+, PWRO– (PWRI connected to GNDA)	– 50	–	50	mV
PSRR5	Power Supply Rejection of V_{CC} or V_{BB} (PWRI connected to GNDA)	45	–	–	dB

Notes : 1 Maximum power consumption depend on the load impedance connected to the power amplifier. The specification listed assumes 0 dBm is delivered to 600 Ω connected from PWRO + PWRO –.
2. Transmit filter input op amp set to the non-inverting unity gain mode, with VF_XI+ = 1.1 Vrms, unless otherwise noted.
3. The 0 dBm0 level for the filter is assumed to be 1.54 Vrms measured at the output of the XMT or RCV filter.
4. The 0 dBm0 level for the power amplifiers is load dependent For R_L = 600 Ω to GNDA, the 0 dBm0 level is 1.43 Vrms measured at the amplifier output. For R_L = 300 Ω the dBm0 level is 1.22 Vrms
5. VF_RO connected to PWRI, input signal applied to VF_RI.

TYPICAL PERFORMANCE CHARACTERISTICS

Figure 1 : Transmit Filter Stage.

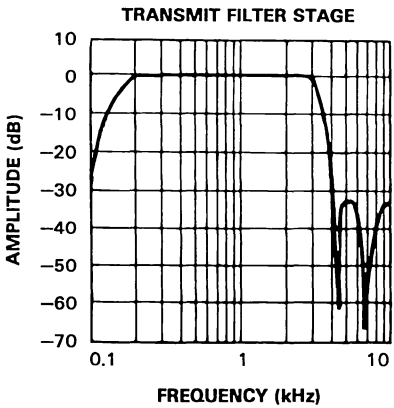


Figure 2 : Receive Filter Stage.

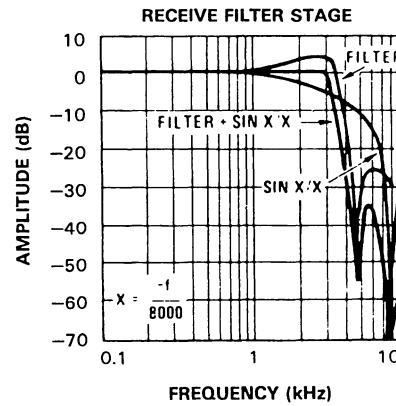
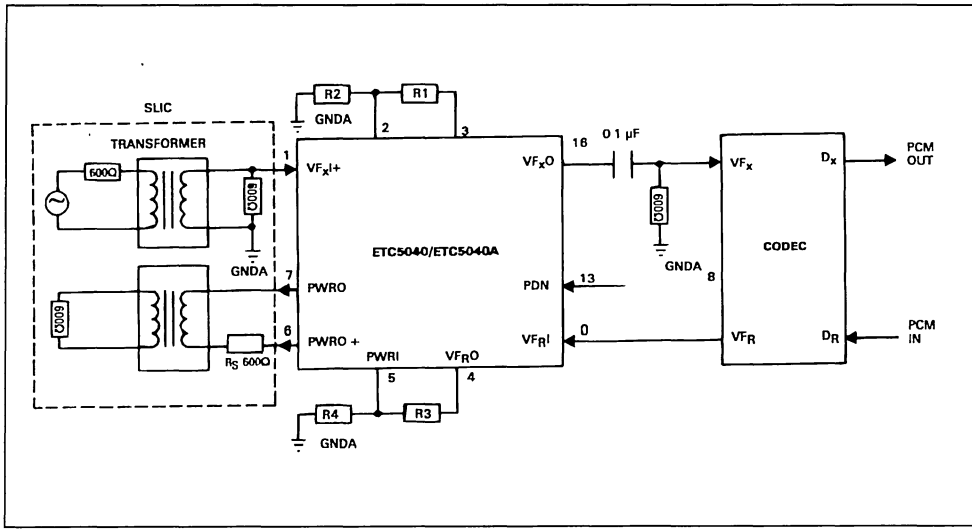


Figure 3 : Interface Circuit For CODEC.



Notes : 1. Transmit Voltage gain = $\frac{R1 + R2}{2}$ x √2 (the filter itself introduces a 3 dB gain) (R1 + R2 ≥ 10 kΩ)

2. Receive gain = $\frac{R4}{R3 + R4}$
(R3 + R4 ≥ 10 kΩ)
3. In the configuration shown, the receive filter power amplifiers will drive a 600 Ω T to R termination.
An alternative arrangement using a transformer winding ratio equivalent to 1.414.1 and 300 Ω resistor R level of 10 dBm across 600 Ω termination impedance.

FUNCTIONAL DESCRIPTION

The ETC5040FN-ETC5040FN/A monolithic filter contains four main sections ; Transmit Filter, Receive Filter, Receive Filter Power Amplifier, and Frequency Divider/Select Logic (figure 1). A brief description of the circuit operation for each section is provided below.

TRANSMIT FILTER

The input stage of the transmit filter is a CMOS operational amplifier which provides an input resistance greater than 10M, a voltage gain of greater than 5000, low power consumption (less than 3mW), high power supply rejection, and is capable of driving a 10k load parallel with up to 25pF. The inputs and output of the amplifier are accessible for added flexibility. Non-inverting mode, inverting mode, or differential amplifier mode operation can be implemented with external resistors. It can also be connected to provide a gain of up to 20dB without degrading the overall filter performance. The input stage is followed by a prefilter which is a two pole RC active low pass filter designed to attenuate high frequency noise before the input signal enters the switched-capacitor high pass and low pass filters.

A high pass filter is provided to reject 200Hz or lower noise which may exist in the signal path. The low pass portion of the switched-capacitor filter provides stopband attenuation which exceeds the D3 and D4 specifications as well as the CCITT G712 recommandations.

The output of the transmit filter, the postfilter, is also a two-pole RC active low pass filter which attenuates clock frequency noise by at least 40dB. The output of the transmit filter is capable of driving a 3.2V peak to peak signal into a 10kload in parallel with up to 25pF.

RECEIVE FILTER

The input stage of the receive filter is a prefilter which is similar to the transmit prefilter. The prefilter attenuates high frequency noise that may be present on the receive input signal. A switched capacitor low pass filter follows the prefilter to provide the necessary passband flatness, stopband rejection and sin x/x gain correction. A postfilter which is similar to the transmit postfilter follows the low pass stage. It attenuates clock frequency noise and provides a low output impedance capable of directly driving an electronic subscriber-line-interface circuit.

RECEIVE FILTER POWER AMPLIFIERS

Two power amplifiers are also provided to interface to transformer coupled line circuits. These two amplifiers are driven by the output of the receive postfilter through gain setting resistors, R3, R4 (figure 3). The power amplifiers can be deactivated, when not required, by connecting the power amplifier input (pin 5) to the negative power supply V_{BB}. This reduces the total filter power consumption by approximately 10mW to 20mW depending on output signal amplitude.

POWER DOWN CONTROL

A power down mode is also provided. A logic 1 power down command applied on the PDN pin (pin 17) will reduce the total filter power consumption to less than 1mW and turn the power amplifier outputs into high impedance state.

FREQUENCY DIVIDER AND SELECT LOGIC CIRCUIT

This circuit divides the external clock frequency down to the switching frequency of the low pass switched capacitor filters. The divider also contains a TTL-CMOS interface circuit which converts the external TTL clock level to the CMOS logic level required for the divider logic. This interface circuit can also be directly driven by CMOS logic.

A frequency select circuit is provided to allow the filter to operate with 2.048 MHz, 1544 MHz or 1.536 MHz clock frequencies. By connecting the frequency select pin CLKO (pin 18) to V_{CC}, a 2.048MHz clock input frequency is selected. Digital ground selects 1.544 MHz and V_{BB} selects 1.536 MHz.

APPLICATIONS INFORMATION

GAIN ADJUST

Figure 3 shows the signal path interconnections between the ETC5040FN-ETC5040FN/A and single-channel CODEC. The transmit RC coupling components have been chosen both for minimum passband droop and to present the correct impedance to the CODEC during sampling.

Optimum noise and distortion performance will be obtained from the ETC5040FN-ETC5040FN/A filter when operated with system peak overload voltages of 2.5 V to 3.2 V at VF_XO and VF_RO. When interfacing to a PCM CODEC with a peak overload voltage outside this range, further gain or attenuation may be required.

For example, the ETC5040FN-ETC5040FN/A filter can be used with CODEC which has a 5.5 V peak overload voltage. A gain stage following the transmit filter output and an attenuation stage following the CODEC output are required.

BOARD LAYOUT

Care must be taken in PCB layout to minimize power supply and ground noise. Analog ground (GNDA) of each filter shoult be connected to digital ground (GNDD) at a single point, which should be bypassed to both power supplies.

Further power supply decoupling adjacent to each filter and CODEC is recommended. Ground loops should be avoided, both between the GNDA traces of adjacent filters and CODECs.

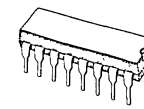
μ-255 LAW COMPANDING CODEC

- ±5-VOLT POWER SUPPLIES
- LOW POWER DISSIPATION - 30mW (Typ)
- FOLLOWS THE μ-255 COMPANDING LAW
- SYNCHRONOUS OR ASYNCHRONOUS OPERATION
- ON-CHIP SAMPLE AND HOLD
- ON-CHIP OFFSET NULL CIRCUIT ELIMINATES LONG-TERM DRIFT ERRORS AND NEED FOR TRIMMING
- SINGLE 16-PIN PACKAGE
- MINIMAL EXTERNAL CIRCUITRY REQUIRED
- SERIAL DATA OUTPUT OF 64kb/s-2.1Mb/s AT 8kHz SAMPLING RATE
- SEPARATE ANALOG AND DIGITAL GROUNDING PINS REDUCE SYSTEM NOISE PROBLEMS

DESCRIPTION

The M5116 is a monolithic CMOS companding CODEC which contains two sections : (1) An analog-to-digital converter which has a transfer characteristic conforming to the μ-255 companding law and (2) a digital-to-analog converter which also conforms to the μ-255 law.

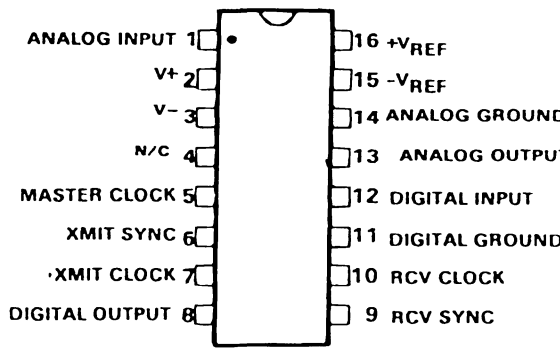
These two sections form a coder-decoder which is designed to meet the needs of the telecommunications industry for per-channel voice-frequency codecs used in telephone digital switching and transmission systems. Digital input and output are in serial format. Actual transmission and reception of 8-bit data words containing the analog information is done at a 64kb/s-2.1Mb/s rate with analog signal sampling occuring at an 8kHz rate. A sync pulse input is provided for synchronizing transmission and reception of multi-channel information being multiplexed over a single transmission line.



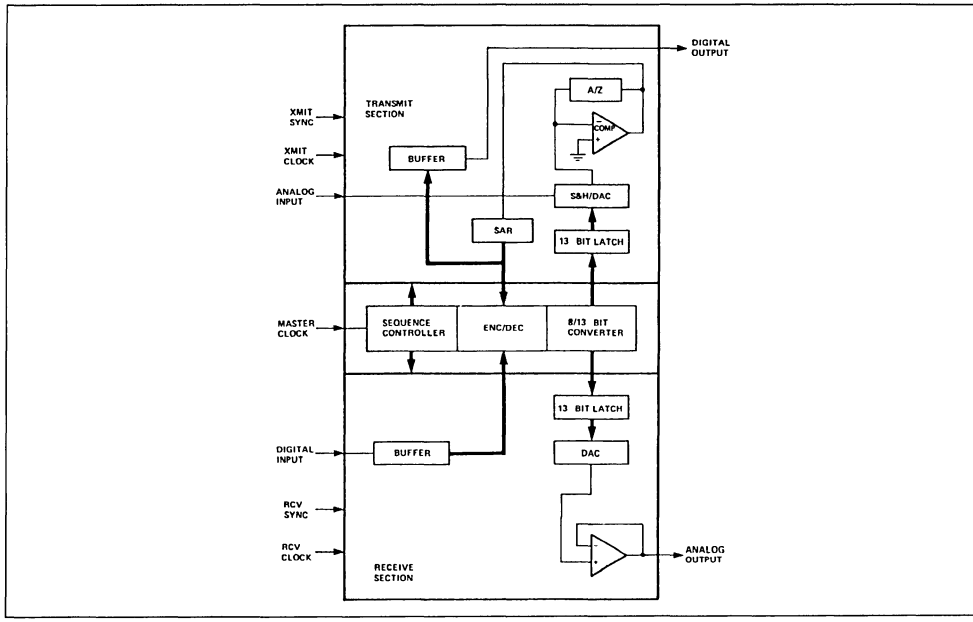
DIP-16

ORDER CODES : M5116N (Plastic)
M5116J (Ceramic)

PIN CONNECTION (top view)

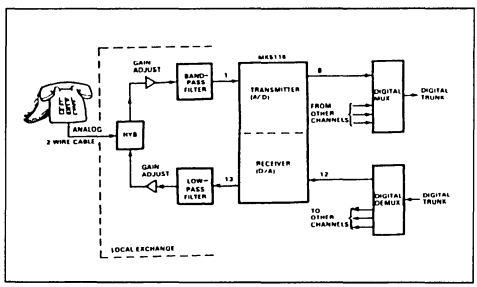


BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

PCM SYSTEM BLOCK DIAGRAM



POSITIVE AND NEGATIVE REFERENCE VOLTAGES (+ V + REF and - V_{REF}) Pins 16 and 15

These inputs provide the conversion references for the digital-to-analog converters in the M5116. + V_{REF} and - V_{REF} must maintain 100ppM/C regulation over the operating temperature range. Variation of the reference directly affects system gain.

ANALOG INPUT, Pin 1

Voice-frequency analog signals which are bandwidth-limited to 4kHz are input at this pin. Typically, they are then sampled at an 8kHz rate (refer to figure 1). The analog input must remain between + V_{REF} and - V_{REF} for accurate conversion. The recommended input interface circuit is shown in figure 6.

MASTER CLOCK ; Pin 5

This signal provides the basic timing and control signals required for all internal conversions. It does not have to be synchronized with RCV SYNC, RCV CLOCK, XMIT SYNC, or XMIT CLOCK and is not internally related to them.

XMIT SYNC, Pin 6 (refer to figure 7 for the Timing Diagram)

This input is synchronized with XMIT CLOCK. When XMIT SYNC goes high, the digital output is activated, and the A/D conversion begins on the next positive edge of MASTER CLOCK. The conversion by MASTER CLOCK can be asynchronous with XMIT CLOCK. The serial output data is clocked out by the positive edges of XMIT CLOCK. The negative edge of XMIT SYNC causes the digital output to become three-state. XMIT SYNC may remain high longer than 8 XMIT CLOCK cycles, but must go low for at least 1 master clock before the transmission of the next digital word (refer to figure 9).

XMIT CLOCK, Pin 7 (refer to figure 7 for the Timing Diagram)

The on-chip 8-bit output shift register of the M5116 is unloaded at the clock rate present on this pin. Clock rates of 64kHz-2.1MHz can be used for XMIT CLOCK. The positive edge of the INTERNAL CLOCK transfers the data from the master to the slave of a master-slave flip-flop (refer to the figure 5). If the positive edge of XMIT SYNC occurs after the positive edge of XMIT CLOCK, XMIT SYNC will determine when the first positive edge of INTERNAL CLOCK will occur. In this event, the hold time for the first clock pulse is measured from the positive edge of XMIT SYNC.

RVC SYNC, Pin 9 (refer to figure 8 for the Timing Diagram)

This input is synchronized with RCV CLOCK, and serial data is clocked in by RCV CLOCK. Duration of the RCV SYNC pulse is approximately 8 RCV CLOCK periods. The conversion from digital to analog starts after the negative edge of the RCV SYNC pulse (refer to figure 1). The negative edge of RCV SYNC should occur before the 9th positive clock edge to insure that only eight bits are clocked in. RCV SYNC must stay low for 17 MASTER CLOCKS (min.) before the next digital word is to be received (refer to figure 10).

RCV CLOCK, Pin 10 (refer to figure 8 for Timing Diagram)

The on-chip 8-bit shift register for the M5116 is loaded at the clock rate present on this pin. Clock rates of 64kHz-2.1MHz can be used for RCV CLOCK. Valid data should be applied to the digital input before the positive edge of the internal clock (refer to figure 2). This set up time, t_{RDS}, allows the data to be transferred into the MASTER of a master-slave flip-flop. A hold time, t_{RDH}, is required to complete this transfer. If the rising edge of RCV SYNC occurs after the first rising edge of RCV CLOCK, RCV SYNC will determine when the first positive edge of INTERNAL CLOCK will occur. In this event, the set-up and hold times for the first clock pulse should be measured from the positive edge of RCV SYNC.

Figure 1 : A/D, D/A Conversion Timing.

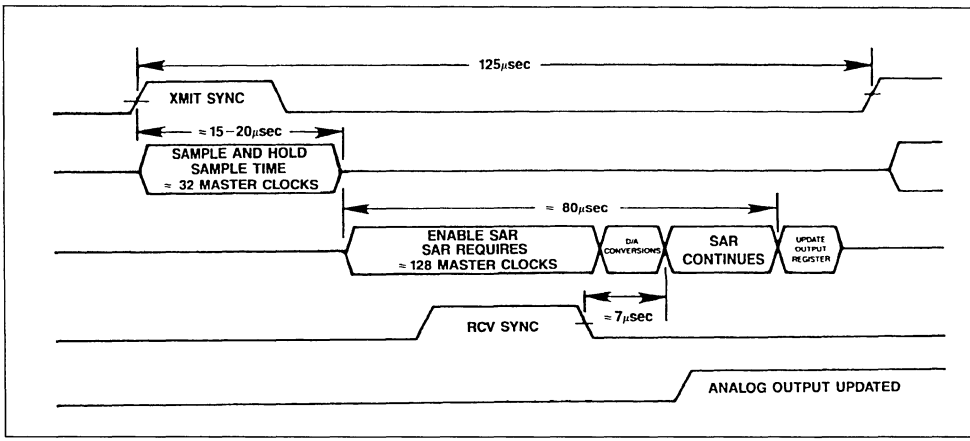
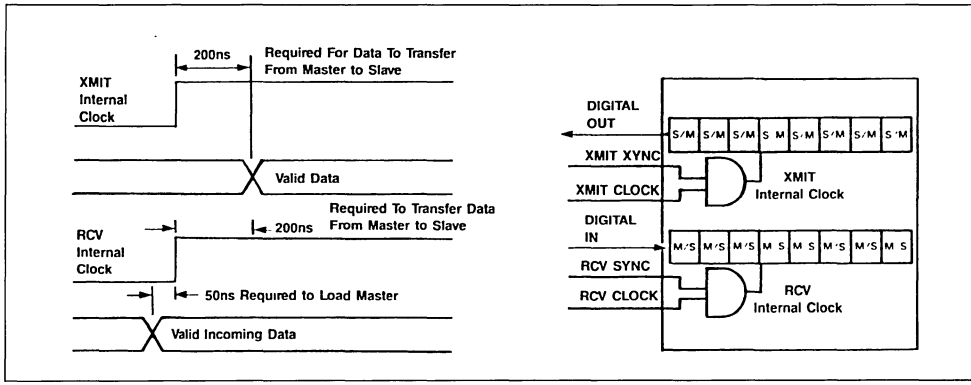


Figure 2 : Data Input/Output Timing.



DIGITAL OUTPUT, Pin 8

The M5116 output register stores the 8-bit encoded sample of the analog input. This 8-bit word is shifted out under control of XMIT SYNC and XMIT CLOCK. When XMIT SYNC is low, the DIGITAL OUTPUT is an open circuit. When XMIT SYNC is high, the state of the DIGITAL OUTPUT is determined by the value of the output bit in the serial shift register. The output is composed of a Sign Bit, 3 Chord Bits, and 4 Step Bits. The sign Bit indicates the polarity of the analog input while the Chord and Step Bits indicate the magnitude. In the first Chord, the Step Bit has a value of 0.6mV. In the second Chord, the Step Bit has a value of 1.2mV. This doubling of the step value continues for each of the six successive Chords.

Each Chord has a specific value ; and the Step Bits, 16 in each Chord, specify the displacement from that value (refer to Table 1). Thus the output, which follows the μ-255 law, has resolution that is proportional to the input level rather than to full scale. This provides the resolution of a 12-bit A/D converter at low input levels and that of a 6-bit converter as the input approaches full scale. The transfer characteristic of the A/D converter (μ-law Encoder) is shown in figure 3.

DIGITAL INPUT, Pin 12

The M5116 input register accepts the 8-bit sample of an analog value and loads it under control of RCV SYNC and RCV CLOCK. The timing diagram is shown in figure 11. When RCV SYNC goes high, the MK5116 uses RCV CLOCK to clock the serial data into its input register. RCV SYNC goes low to indicate the end of serial input data. The 8 bits of the input data have the same functions described for the DIGITAL OUTPUT. The transfer characteristic of the D/A converter (μ-Law Decoder) is shown in figure 4.

DIGITAL OUTPUT CODE μ-LAW

Table 1.

	Chord Code	Chord Value	Step Value
1.	000	0.0mV	0.163mV
2	001	10.11mV	1.226mV
3.	010	30.3mV	2.45mV
4.	011	70.8mV	4.90mV
5.	100	151.7mV	9.81mV
6.	101	313mV	19.61mV
7.	110	637mV	39.2mV
8	111	1.284V	78.4mV

EXAMPLE :

1 011 0010 = + 70.8mV + (2 x 4.90mV)

Sign Bit Chord Step Bits

If the sign bit were a zero, then both plus signs would be changed to minus signs.

Figure 3 : A/D Converter (μ-law encoder) Transfer Characteristic.

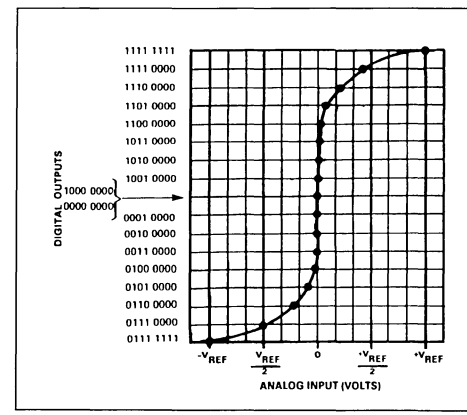
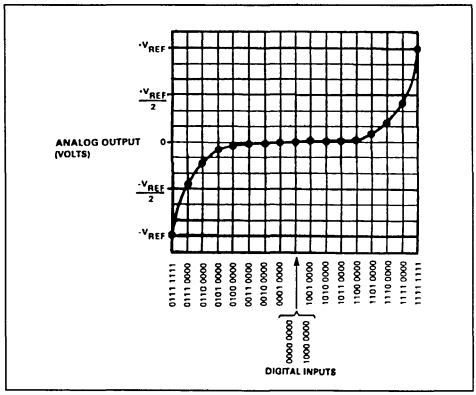


Figure 4 : D/A Converter (μ-law encoder) Transfer Characteristic.



ANALOG OUTPUT, Pin 13

The analog output is in the form of voltage steps (100% duty cycle) having amplitude equal to the analog sample which was encoded. This waveform is then filtered with an external low-pass filter with sinx/x correction to recreate the sampled voice signal.

OPERATION OF CODEC WITH 64kHz XMIT/RCV CLOCK FREQUENCIES

XMIT/RCV SYNC must not be allowed to remain at a logic "1" state. XMINT SYNC is required to be at a logic "0" state for 1 master-clock period (min.) before the next digital word is transmitted. RCV SYNC is required to be at a logic "0" state for 17 master-clock periods (min.) before the next digital word is received (refer to figures 9 and 10).

OFFSET NULL

The offset-null feature of the MK5116 eliminates long-term drift errors and conversion errors due to temperature changes by going through an offset-adjustment cycle before every conversion, thus guaranteeing accurate A/D conversion for inputs near ground. There is no offset adjust of the output amplifier because the resultant DC error ($V_{OFFSET0}$) will have no effect, since the output is intended to be AC-coupled to the external filter. The sign is not used to null the analog input. Therefore, for an analog input of 0 volts, the sign bit will be stable.

PERFORMANCE EVALUATION

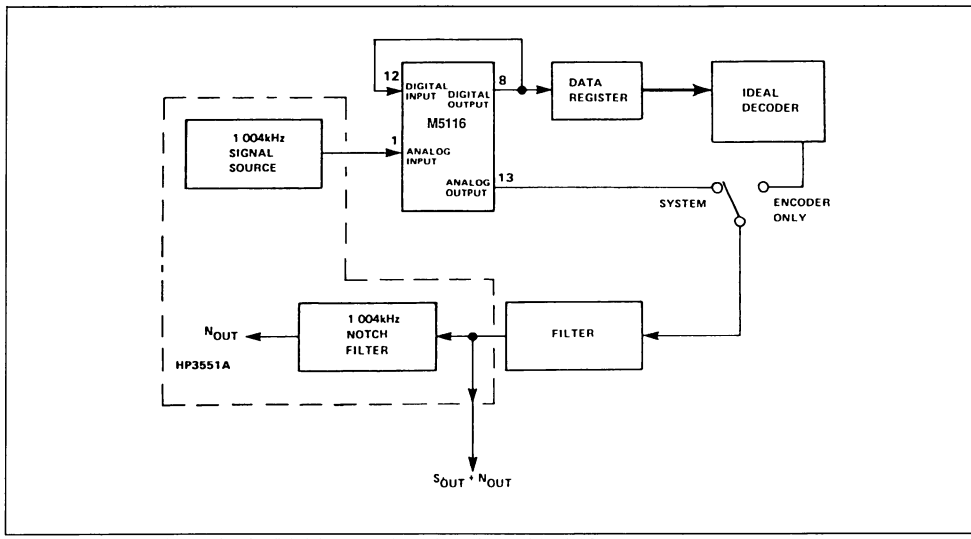
The equipment connections shown in figure 5 can be used to evaluate the performance of the MK5116. An analog signal provided by the HP3551A Transmission Test Set is connected to the Analog Input (Pin 1) of the MK5116. The Digital Output of the CODEC is tied back to the Digital Input, and the Analog Output is fed through a low-pass filter to the HP3551A. Remaining pins of the MK5116 are connected as follows :

(1) RCV SYNC is tied to XMIT SYNC
(2) XMIT CLOCK is tied to MASTER CLOCK. The signal is inverted and tied to RCV CLOCK.

The following timing signals are required :
(1) MASTER CLOCK = 1.536MHz
(2) XMIT SYNC repetition rate = 8kHz
(3) XMIT SYNC width = 8 XMIT CLOCK periods

When all the above requirements are met, the setup of figure 5 permits the measurement of synchronous system performance over a wide range of analog inputs. The data register and ideal decoder provide a means of checking the encoder portion of the MK5116 independently of the decoder section. To test the system in the asynchronous mode, MASTER CLOCK should be separated from XMIT CLOCK, and MASTER CLOCK should be separated from RCV CLOCK. XMIT and RCV SYNCS are also separated. Some experimental results obtained with the MK5116 are shown in figure 11 and figure 12. In each case, both the measured results and the corresponding D3 Channel Bank specifications are shown. The MK5116 exceeds the requirements for Signal-to-Distortion ratio (figure 11) and for Gain Tracking (figure 12).

Figure 5 : System Characteristics Test Configuration.



Note : The ideal decoder consist of a digital decompander and a 13-bit precision DAC

ABSOLUTE MAXIMUM RATINGS

Parameter	Value	Unit
DC Supply Voltage, V+	+ 6	V
DC Supply Voltage, V–	– 6	V
Ambient Operating Temperature, T_A	0 to 70	°C
Storage Temperature	– 55 to + 125	°C
Package Dissipation at 25 °C (derated 9mW/°C when soldered into PCB)	500	mW
Digital Input	$-0.5V \leq V_{IN} \leq V+$	
Analog Input	$V- \leq V_{IN} \leq V+$	
$+ V_{REF}$	$-0.5V \leq + V_{REF} \leq V+$	
$- V_{REF}$	$V- \leq - V_{REF} \leq + 0.5$	V

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damages to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operation sections of this specification is not implied Exposure to absolute maximum rating conditions for extended periods may effect device reliability.

ELECTRICAL OPERATING CHARACTERISTICS

POWER SUPPLY REQUIREMENTS

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
V+	Positive Supply Voltage	4.75	5.0	5.25	V	
V–	Negative Supply Voltage	– 5.25	– 5.0	– 4.75	V	
$+ V_{REF}$	Positive Reference Voltage	2.375	2.5	2.625	V	1
$- V_{REF}$	Negative Reference Voltage	– 2.625	– 2.5	– 2.375	V	1

TEST CONDITIONS : V+ = 5.0V, V– = – 5.0V, + V_{REF} = 2.5V, – V_{REF} = – 2.5V, T_A = 0°C to 70°C

DC CHARACTERISTICS

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
R_{INAS}	Analog Input Resistance During Sampling		2		kΩ	2
R_{INANS}	Analog Input Resistance Non-Sampling		100		MΩ	
C_{INA}	Analog Input Capacitance		150	250	pF	2
$V_{OFFSET/1}$	Analog Input Offset Voltage		± 1	± 8	mV	2
R_{OUTA}	Analog Output Resistance		1	10	Ω	
I_{OUTA}	Analog Output Current	0.25	0.5		mA	
$V_{OFFSET/0}$	Analog Output Offset Voltage		+ 20	± 850	mV	
I_{INLOW}	Logic Input Low Current (V_{IN} = 0.8V) Digital Input, Clock Input, Sync Input		± 0.1	± 10	µA	3
I_{INHIGH}	Logic Input High Current (V_{IN} = 2.4V) Digital Input, Master and RCV Clock Input, RCV Sync Input		± 0.1	± 10	µA	3
I_{INHIGH_X}	Logic Input High Current (V_{IN} = 2.4V) TX Clock, TX Sync		– .25	– 0.8	mA	3
C_{DO}	Digital Output Capacitance		8	12	pF	
I_{DOL}	Digital Output Leakage Current		± 0.1	± 10	µA	
V_{OUTLOW}	Digital Output Low Voltage			0.4	V	4
$V_{OUTHIGH}$	Digital Output High Voltage	3.9			V	4
I+	Positive Supply Current		4	10	mA	5
I–	Negative Supply Current		2	6	mA	5
I_{REF+}	Positive Reference Current		4	20	µA	
I_{REF-}	Negative Reference Current		4	20	µA	

AC CHARACTERISTICS (refer to figure 10 and figure 11)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
F_M	Master Clock Frequency	1.5	1.544	2.1	MHz	
F_R, F_X	XMIT, RCV Clock Frequency	0.064	1.544	2.1	MHz	
PW_{CLK}	Clock Pulse Width (MASTER, XMIT, RCV)	200			ns	
t_{RC}, t_{FC}	Clock Rise, Fall Time (MASTER, XMIT, RCV)			25% of PW_{CLK}	ns	
t_{RS}, t_{FS}	Sync Rise, Fall Time (XMIT, RCV)			25% of PW_{CLK}	ns	
t_{DIR}, t_{DIF}	Data Input Rise, Fall Time			25% of PW_{CLK}	ns	
t_{WSX}, t_{WSR}	Sync Pulse Width (XMIT RCV)		$\frac{8}{F_X(F_R)}$		µs	

DC CHARACTERISTICS (refer to figure 7 and figure 8)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
t_{PS}	Sync Pulse Perlod (XMIT, RCV)		125		µs	
t_{XCS}	XMIT Clock-to-XMIT Sync Delay	50% of t_{FC} (t_{RS})			ns	6
t_{XCSN}	XMIT Clock-to-XMIT Sync (negative edge) Delay	200			ns	
t_{XSS}	XMIT Sync Set-Up Time	200			ns	
t_{XDD}	XMIT Data Delay	0		200	ns	4
t_{XDP}	XMIT Data Present	0		200	ns	4
t_{XDT}	XMIT Data Three State			150	ns	4
t_{DOF}	Digital Output Fall Time		50	100	ns	4
t_{DOR}	Digital Output Rise Time		50	100	ns	4
t_{SRC}	RVC Sync-to-RCV Clock Delay	50% of t_{RC} (t_{FS})			ns	6
t_{RDS}	RCV Data Set-up Time	50			ns	7
t_{DRH}	RCV Data Hold Time	200			ns	7
t_{RCS}	RCV Clock-to-RCV Sync Delay	200			ns	
t_{RSS}	RCV Sync Set-up Time	200			ns	7
t_{SAO}	RCV Sync-to-Analog Output Delay		7		µs	
SLEW+	Analog Output Positive Slew Rate		1		V/µs	
SLEW–	Analog Output Negative Slew Rate		1		V/µs	
DROOP	Analog Output Droop Rate		25		µV/µs	

AC CHARACTERISTICS (refer to figures 11 and 12)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
GT_X	Gain Tracking Transmit	Analog Input = + 3 to – 37dBm0 Analog Input = – 37 to – 50dBm0 Analog Input = – 50 to – 55dBm0 Relative to 0 dBm0	– .2 – .4 – 1.25	0.0 ± 0.1 ± 0.2	+ .2 + .4 + 1.25	dB dB dB
GT_R	Gain Tracking Receive	Input Level = + 3 to – 37dBm0 Input Level = – 37 to – 50dBm0 Input Level = – 50 to – 55dBm0 Relative to 0 dBm0	– .2 – .4 – 1.25	0.0 ± 0.1 ± 0.2	+ .2 + .4 + 1.25	dB dB dB
GT_{E-E}	Gain Tracking End to End	Analog Input = + 3 to – 37dBm0 Analog Input = – 37 to – 50dBm0 Analog Input = – 50 to – 55dBm0 Relative to 0 dBm0	– .4 – .8 – 2.50	0.0 ± 0.1 ± 0.2	+ .4 + .8 + 2.50	dB dB dB
SD_X	Signal to Distortion Transmit	Analog Input = 0 to – 30dBm0 Analog Input = – 40dBm0 Analog Input = – 45dBm0	37 31 26			dB dB dB
SD_R	Signal to Distortion Receive	Input Level = 0 to – 30dBm0 Input Level = – 40dBm0 Input Level = – 45dBm0	37 31 26			dB dB dB

AC CHARACTERISTICS (refer to figures 11 and 12)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
SD_{E-E}	Signal to Distortion End to End	Analog Input = 0 to – 30dBm0 Analog Input = – 40 dBm0 Analog Input = – 45 dBm0	35 29 24			dB dB dB
N_X	Idle Channel Noise Transmit	Analog Input = 0Volts			17	dBnc0
N_R	Idle Channel Noise Receive	Digital Input = 0 Code			0	dBnc0
N_{E-E}	Idle Channel Noise End to End	Analog Input = 0Volts Digital Output to Digital Input			18	dBncO
CT_{RX}	Crosstalk Receive to Transmit	Analog In = – 50dBm0 at 2600Hz Digital Input = 0dBm0 at 1008Hz digital			– 80	dB
CT_{XR}	Crosstalk Transmit to Receive	Analog In = 0dBm0 at 1008Hz Digital Input = 0 Code			– 80	dB
TLP	Transmit Level Point	600Ω		+ 4		dB

Notes :
1. $+V_{REF}$ and $-V_{REF}$ must be matched within ±1 % in order to meet system requirements.
2. Sampling is accomplished by charging an internal capacitor ; therefore, the designer should avoid excessive source impedance. Input-related device characteristics are derived using the Recommended Analog Input Circuit. See figure 6.
3. When a transition from a "1" to a "0" takes place, the user must sink the "1" current until reaching the "0" level
4. Driving 30pF with I_{OH} = 100µA, I_{OL} = 500µA
5. Results in 30mW typical power dissipation (clocks applied) under normal operating conditions
6. This delay is necessary to avoid overlapping CLOCK and SYNC.
7. The first bit of data is loaded when the Sync and Clock are both "1" during bit time 1 as shown on RCV timing diagram

Figure 6 : Recommended Analog Input Circuit.

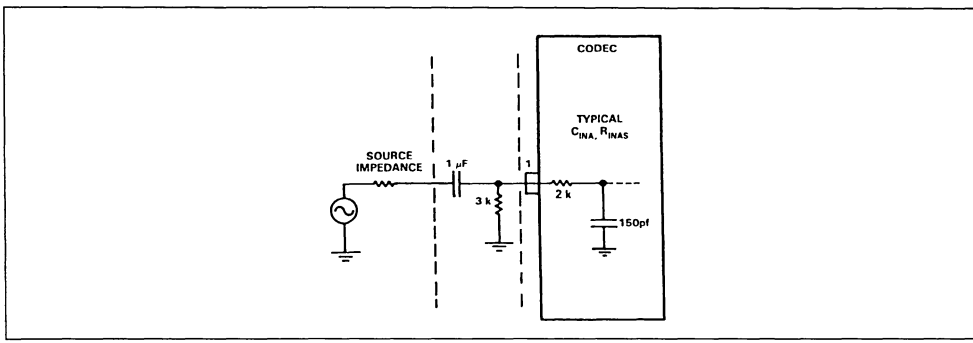
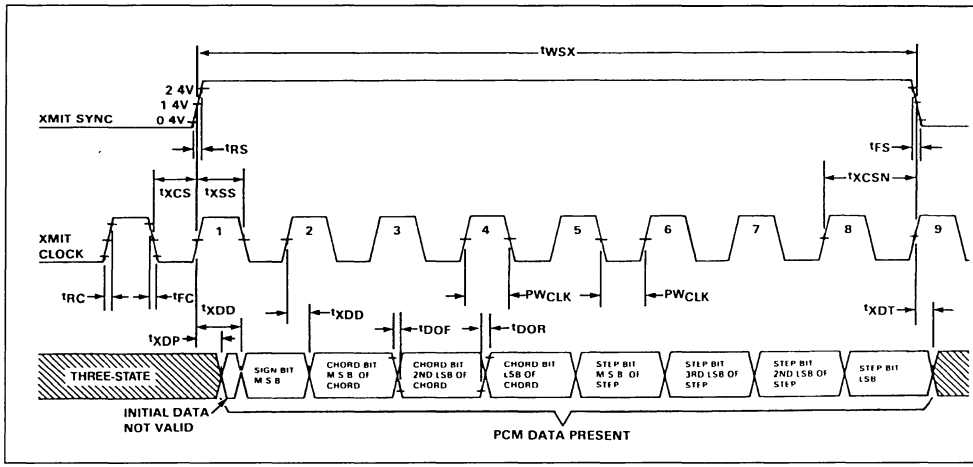
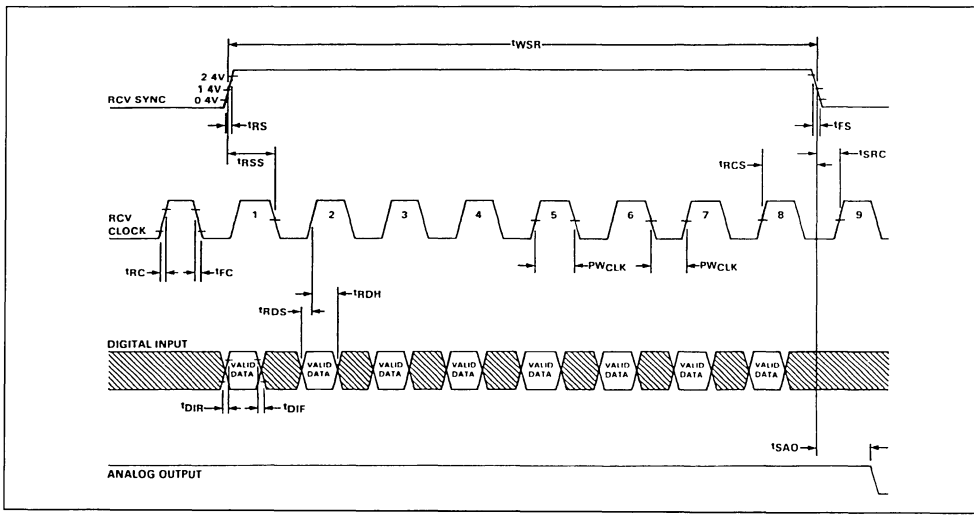


Figure 7 : Transmitter Section Timing.



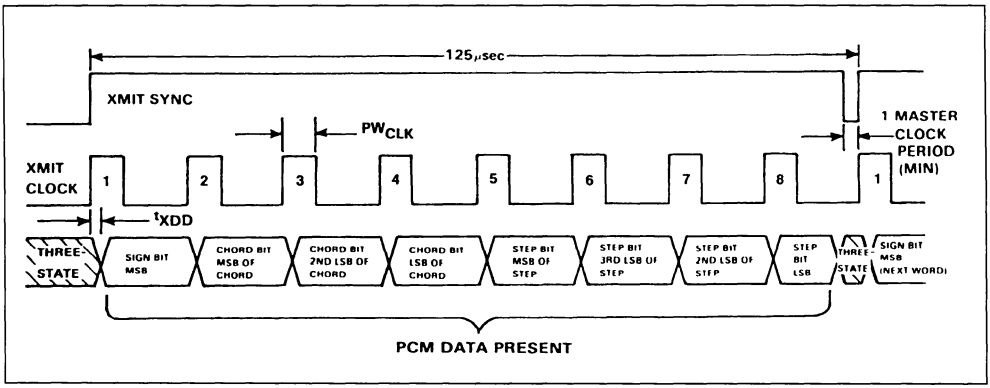
Note : All rise and fall times are measured from 0 4V and 2 4V. All delay times are measured from 1 4V

Figure 8 : Receiver Section Timing.



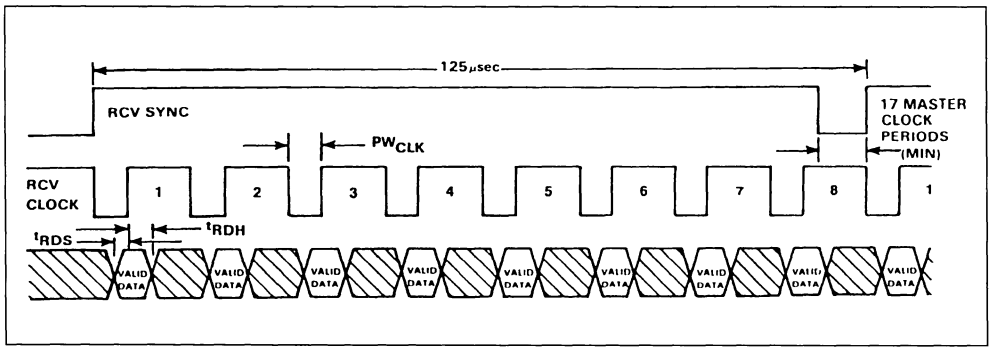
Note : All rise and fall times are measured from 0.4V and 2 4V All delay times are measured from 1.4V

Figure 9 : 64kHz Operation, Transmitter Section Timing.



Note : All rise and fall times are measured from 0 4V and 2 4V. All delay times are measured from 1 4V.

Figure 10 : 64kHz Operation, Receiver Section Timing.



Note : All rise and fall times are measured from 0 4V and 2.4V. All delay times are measured from 1 4V.

Figure 11 : Single-ended Signal to Distortion.

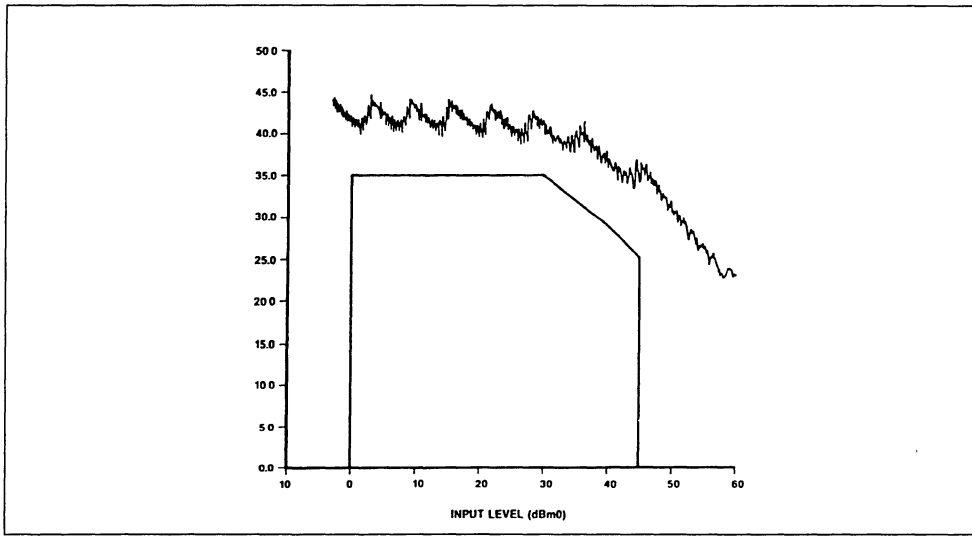
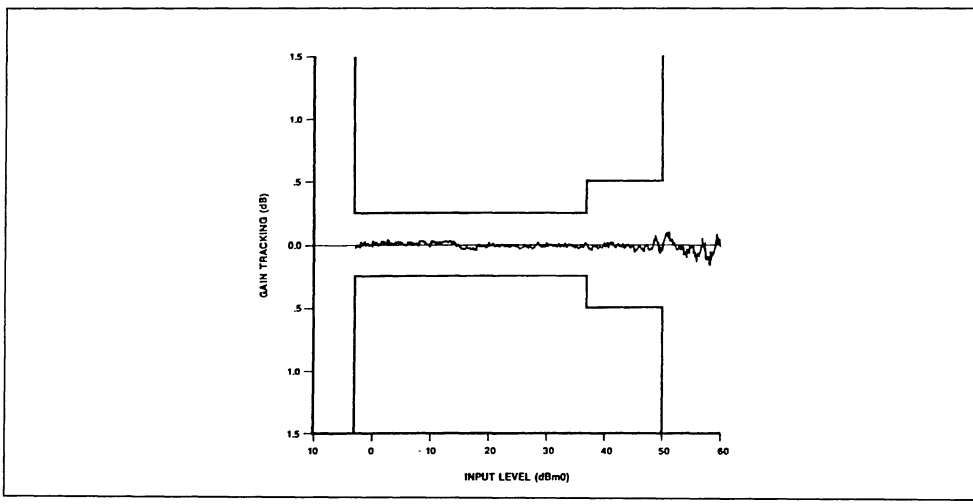


Figure 12 : Single-ended Gain Tracking.



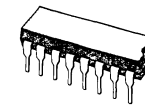
A-LAW COMPANDING CODEC

- ±5-VOLT POWER SUPPLIES
- LOW POWER DISSIPATION - 30mW (Typ)
- FOLLOWS THE A-LAW COMPANDING CODE
- INCLUDES CCITT RECOMMENDED EVEN-ORDER-BIT INVERSION
- SYNCHRONOUS OR ASYNCHRONOUS OPERATION
- ON-CHIP SAMPLE AND HOLD
- ON-CHIP OFFSET NULL CIRCUIT ELIMINATES LONG-TERM DRIFT ERRORS AND NEED FOR TRIMMING
- MINIMAL EXTERNAL CIRCUITRY REQUIRED
- SERIAL DATA OUTPUT OF 64kb/s THROUGH 2.1Mb/s AT 8kHz SAMPLING RATE
- SEPARATE ANALOG AND DIGITAL GROUNDS REDUCE NOISE PROBLEMS

DESCRIPTION

The M5156 is a monolithic CMOS companding CODEC that contains two sections : (1) An analog-to-digital converter with a transfer characteristic conforming to the A-law companding code and (2) a digital-to-analog converter that also conforms to the A-law code.

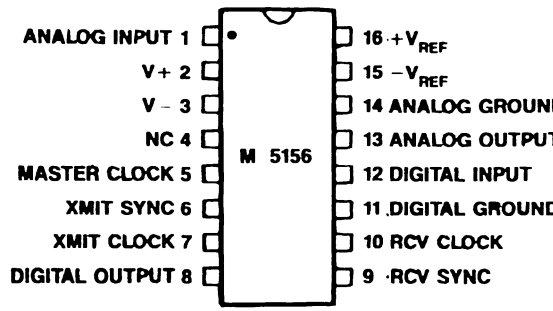
These two sections form a coder-decoder designed to meet the needs of the telecommunications industry for per-channel voice-frequency CODECs used in digital switching and transmission systems. Digital input and output are in serial format. Actual transmission and reception of 8-bit data words containing the analog information is done at a 64kb/s through 2.1Mb/s rate with analog signal sampling occuring at an 8kHz rate. A sync pulse input is provided for synchronizing transmission and reception of multi-channel information being multiplexed over a single transmission line.



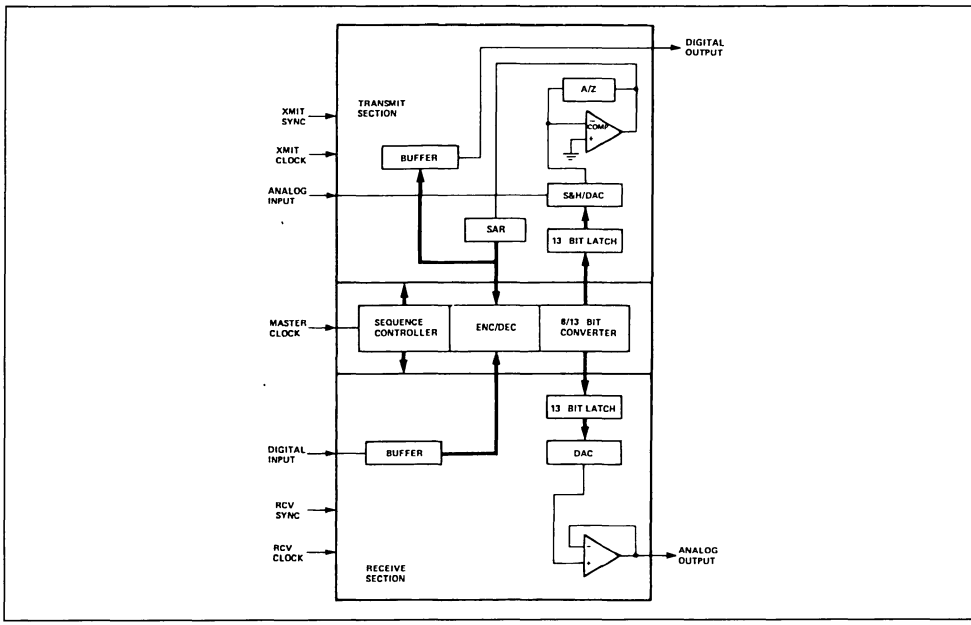
DIP-16

ORDER CODES : M5156FI (Ceramic)

PIN CONNECTION (top view)

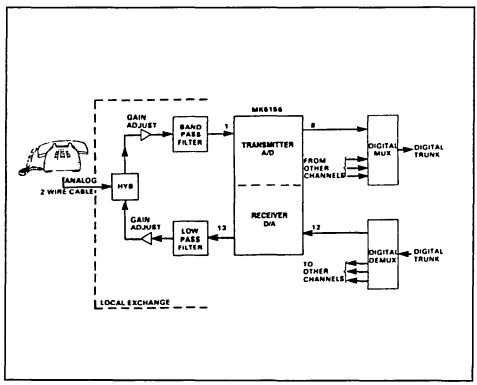


BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

PCM SYSTEM BLOCK DIAGRAM



+ V_{REF} AND - V_{REF}

Input. Pins 16 and 15. These positive and negative reference voltages provide the conversion references for the digital-to-analog converters in the M5156. + V_{REF} and - V_{REF} must maintain 100ppM/°C regulation over the operating temperature range. Variation of the reference directly affects system gain.

ANALOG INPUT

Input. Pin 1. Voice-frequency analog signals that are bandwidth-limited to 4kHz are input at this pin. Typically, they are then sampled at an 8kHz rate. (See figure 1). The analog input must remain between + V_{REF} and - V_{REF} for accurate conversion. The recommended input interface circuit is shown in figure 6.

MASTER CLOCK

Input. Pin 5. This signal provides the basic timing and control signals required for all internal conversions. It does not have to be synchronized with RCV SYNC, RCV CLOCK, XMIT SYNC or XMIT CLOCK and is not internally related to them.

XMIT SYNC

Input. Pin 6. This input is synchronized with XMIT CLOCK. When XMIT SYNC goes high, the digital output is activated and the A/D conversion begins on the next positive edge of MASTER CLOCK. The

conversion by MASTER CLOCK can be asynchronous with XMIT CLOCK. The serial output data is clocked out by the positive edges of XMIT CLOCK. The negative edge of XMIT SYNC causes the digital output to become three-state. XMIT SYNC must go low for at least one master clock period prior to the transmission of the next digital word. (see figure 9).

XMIT CLOCK

Input. Pin 7. The on-chip 8-bit output shift register of the M5156 is unloaded at the clock rate present on this pin. Clock rates of 64kHz-2.1MHz can be used for XMIT CLOCK. The positive edge of the INTERNAL CLOCK transfers the data from the master to the slave of a master-slave flip-flop. (See figure 2). If the positive edge of XMIT SYNC occurs after the positive edge of XMIT CLOCK, XMIT SYNC will determine when the first positive edge of internal clock will occur. In this event, the hold time for the first clock pulse is measured from the positive edge of XMIT SYNC.

RCV SYNC

Input. Pin 9. This input is synchronized with RCV CLOCK and serial data is clocked in by RCV CLOCK. Duration of the RCV SYNC pulse is approximately 8 RCV CLOCK periods. The conversion from digital-to-analog starts after the negative edge of the RCV SYNC pulse. (see figure 1). The negative edge of RCV SYNC should occur before the 9th positive clock edge of insure that only eight bits are clocked in. RCV SYNC must stay low for 17 MASTER CLOCKS (min.) before the next digital word is to be received (see figure 10).

RCV CLOCK

Input. Pin 10. The on-chip 8-bit shift register for the M5156 is loaded at the clock rate present on this pin. Clock rates of 64kHz-2.1MHz can be used for

Figure 1 : A/D, D/A Conversion Timing.

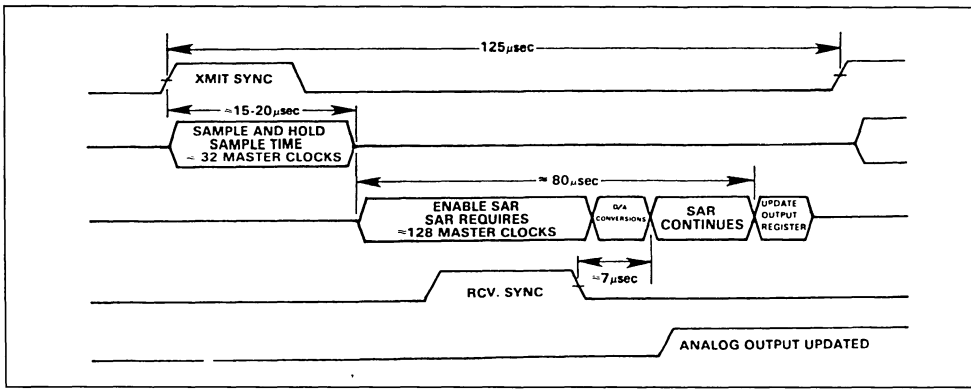
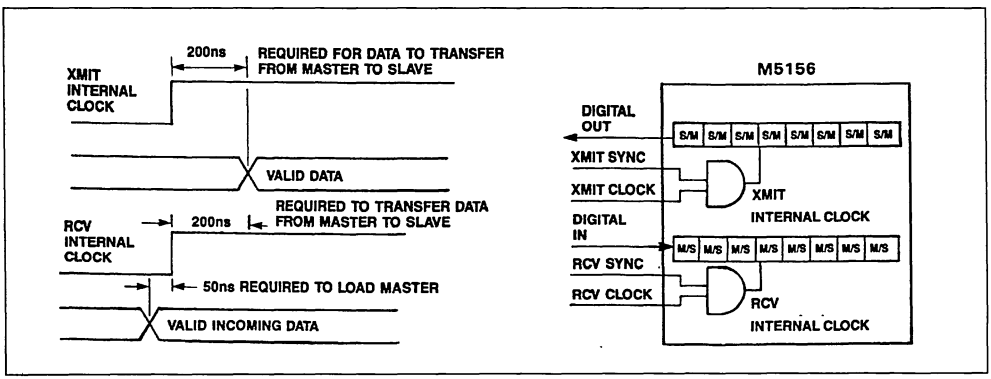


Figure 2 : Data Input/Output Timing.



RCV CLOCK. Valid data should be applied to the digital input before the positive edge of the internal clock. (See figure 2). This set up time, t_{RDS}, allows the data to be transferred into the master of a master-slave flip-flop. The positive edge of the internal clock transfers the data to the slave of the master-slave flip-flop. A hold time, t_{RDH}, is required to complete this transfer. If the rising edge of RCV SYNC occurs after the first rising edge of RCV CLOCK, RCV SYNC will determine when the first positive edge of internal clock will occur. In this event, the set-up and hold times for the first clock pulse should be measured from the positive edge of RCV SYNC.

DIGITAL OUTPUT

Output. Pin 8. The M5156 output register stores the 8-bit encoded sample of the analog input. This 8-bit word is shifted out under control of XMIT SYNC and XMIT CLOCK. When XMIT SYNC is low, the DIGITAL OUTPUT is an open circuit. When XMIT SYNC is high, the state of the DIGITAL OUTPUT is determined by the value of the output bit in the serial shift register. The output is composed of a Sign Bit, 3 Chord Bits, and 4 Step Bits. The Sign Bit indicates the polarity of the analog input while the Chord and Step Bits indicate the magnitude. In the first two Chords, the Step Bit has a value of 1.2mV. In the third Chord, the Step Bit has a value of 2.4mV. This doubling of the step value continues for each of the five successive Chords.

Each Chord has a specific value and the Step Bits, 16 in each Chord, specify the displacement from that value (refer to table 1). Thus the output, wich follows the A-law, has resolution that is proportional to the input level rather than to full scale. This provides the resolution of a 12-bit A/D converter at low input levels and that of a 16-bit converter as the input approaches full scale. The transfer characteristic of the A/D converter (A-law Encoder) is shown in figure 3.

DIGITAL INPUT

Input. Pin 12. The M5156 input register accepts the 8-bit sample of an analog value and loads it under control of RCV SYNC and RVC CLOCK. The timing diagram is shown in figure 11. When RCV SYNC goes high, the M5156 uses RCV CLOCK to clock the serial data into its input register. RCV SYNC goes low to indicate the end of serial inputr data. The eight bits of the input data have the same functions described for the DIGITAL OUTPUT. The transfer characteristic of the D/A converter (A-law Decoder) is shown in figure 4.

Table 1 : Digital Output Code : A Law.

	Chord Code	Chord Value	Step Value
1.	101	0.0mV	1.221mV
2.	100	20.1mV	1.221mV
3.	111	40.3mV	2.44mV
4.	110	80.6mV	4.88mV
5.	001	161.1mV	9.77mV
6.	000	332mV	19.53mV
7.	011	645mV	39.1mV
8.	010	1.289V	78.1mV

EXAMPLE :
1 110 0111 = + 80.6mV + (2 x 4.88mV)
Sign Bit Chord Step Bits
If the sign bit were a zero, then both plus signs would be changed to minus signs.

Figure 3 : A/D Converter (A-law encoder) Transfer Characteristic.

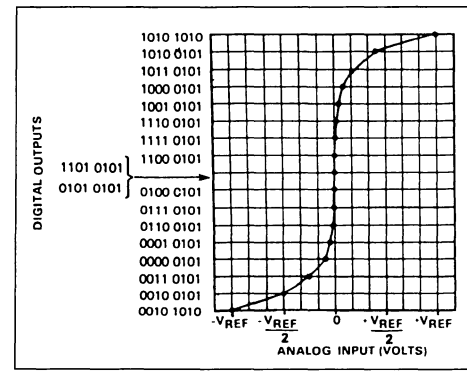
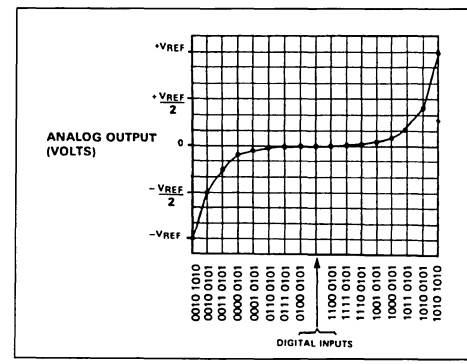


Figure 4 : D/A Converter (A-law encoder) Transfer Characteristic.



ANALOG OUTPUT

Output. Pin 13. The analog output is in the form of voltage steps (100 % duty cycle) having amplitude equal to the analog sample which was encoded. This waveform is then filtered with an external low-pass filter with sinx/x correction to recreate the sampled voice signal.

OPERATION OF CODEC WITH 64kHz XMIT/RCV. CLOCK FREQUENCIES

XMIT/RCV SYNC must not be allowed to remain at a logic "1" state. XMIT SYNC is required to be at a logic "0" state for one master clock period (min.) before the next digital word is transmitted. RCV SYNC is required to be at a logic "0" state for 17 master clock periods (min.) before the next digital word is received (see figures 9 and 10).

OFFSET NULL

The offset null feature of the M5156 eliminates long-term drift errors and conversion errors due to temperature changes by going through an offset adjustment cycle before every conversion, thus guaranteeing accurate A/D conversion for inputs near ground. There is no offset adjust of the output amplifier because, since the output is intended to be AC-coupled to the external filter, the resultant DC error ($V_{OFFSET\ O}$) will have no effect. The sign bit is not used to null the analog input. Therefore, for an analog input of 0 volts, the sign bit will be stable.

PERFORMANCE EVALUATION

The equipment connections shown in figure 5 can be used to evaluate the performance of the M5156. An analog signal provided by the HP3552A Transmission Test Set is connected to the Analog Input (pin 1) of the M5156. The Digital Output of the CODEC is tied back to the Digital Input and the Analog Output is fed through a low-pass filter to the HP2552A. Remaining pins of the M5156 are connected as follows :

(1) RCV SYNC is tied to XMIT SYNC
(2) XMIT CLOCK is tied to MASTER CLOCK. The signal is inverted and tied to RCV CLOCK.

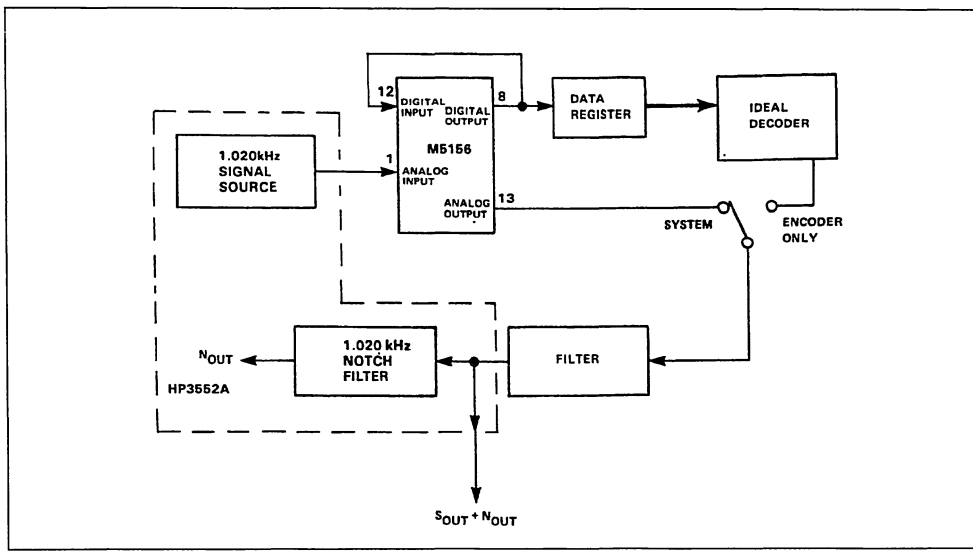
The following timing signals are required :

(1) MASTER CLOCK = 2.048MHz
(2) XMIT SYNC repetition rate = 8kHz
(3) XMIT SYNC width = 8 XMIT CLOCK periods

When all the above requirements are met, the setup of figure 5 permits the measurement of synchronous system performance over a wide range of analog inputs.

The data register and ideal decoder provide a means of checking the encoder portion of the M5156 independently of the decoder section. To test the system in the asynchronous mode, MASTER CLOCK should be separated from XMIT CLOCK and MASTER CLOCK should be separated from RCV CLOCK. XMIT CLOCK and RCV CLOCK are separated also.

Figure 5 : System Characteristics Test Configuration.



Note : The ideal decoder consists of a digital decompander and a 13-bit precision DAC.

ABSOLUTE MAXIMUM RATINGS

Parameter	Value	Unit
DC Supply Voltage, V+	+ 6	V
DC Supply Voltage, V–	– 6	V
Ambient Operating Temperature, T_A	0 to 70	°C
Storage Temperature	– 55 to + 125	°C
Package Dissipation at 25°C (derated 9mW/°C when soldered into PCB)	500	mW
Digital Input	$-0.5V \leq V_{IN} \leq V+$	
Analog Input	$V- \leq V_{IN} \leq V+$	
$+ V_{REF}$	$-0.5V \leq + V_{REF} \leq V+$	
$- V_{REF}$	$V- \leq - V_{REF} \leq + 0.5$	V

* Stressed above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition abolve those indicated in the operational section of this specification is not implied Exposure to absolute maximum rating condition for extended periods may affect device reliability.

ELECTRICAL OPERATING CHARACTERISTICS

POWER SUPPLY

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
V+	Positive Supply Voltage	4.75	5.0	5.25	V	
V–	Negative Supply Voltage	– 5.25	– 5.0	– 4.75	V	
$+ V_{REF}$	Positive Reference Voltage	2.375	2.5	2.625	V	1
$- V_{REF}$	Negative Reference Voltage	– 2.625	– 2.5	– 2.375	V	1

TEST CONDITIONS : V+ = 5.0V, V– = – 5.0V, $+ V_{REF}$ = 2.5V, $- V_{REF}$ = – 2.5V, T_A = 0°C to 70°C

DC CHARACTERISTICS

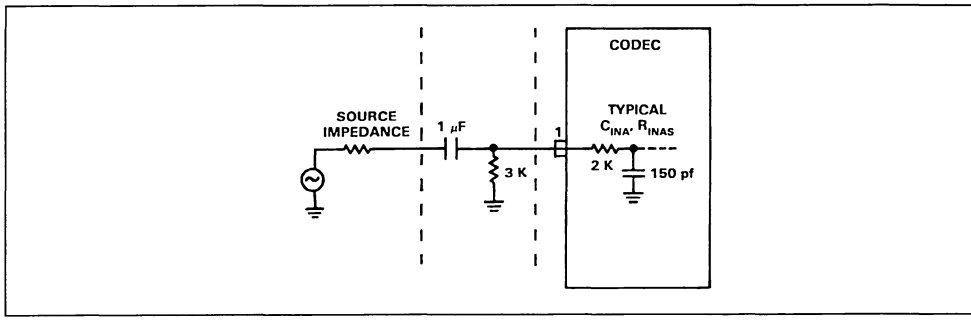
Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
R_{INAS}	Analog Input Resistance During Sampling		2		kΩ	2
R_{INANS}	Analog Input Resistance Non-sampling		100		MΩ	
C_{INA}	Analog Input Capacitance		150	250	pF	2
$V_{OFFSET/1}$	Analog Input Offset Voltage		± 1	± 8	mV	2
R_{OUTA}	Analog Output Resistance		1	50	Ω	
I_{OUTA}	Analog Output Current	0.25	0.5		mA	
$V_{OFFSET/0}$	Analog Output Offset Voltage		+ 50	± 850	mV	
I_{INLOW}	Logic Input Low Current (V_{IN} = 0.8V) Digital Input, Clock Input, Sync Input		± 0.1	± 10	µA	3
I_{INHIGH}	Logic Input High Current (V_{IN} = 2.4V) Digital Input, Clock Input, Sync Input		– 0.25	– 0.8	mA	3
C_{DO}	Digital Output Capacitance		8	12	pF	
I_{DOL}	Digital Output Leakage Current		± 0.1	± 10	µA	
V_{OUTLOW}	Digital Output Low Voltage			0.4	V	4
$V_{OUTHIGH}$	Digital Output High Voltage	3.9			V	4
I+	Positive Supply Current		4	10	mA	5
I–	Negative Supply Current		2	6	mA	5
I_{REF+}	Positive Reference Current		4	20	µA	
I_{REF-}	Negative Reference Current		4	20	µA	

AC CHARACTERISTICS

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
GT_X	Gain Tracking Transmit CCITT G712 Method 2	Analog Input = + 3 to – 40dBm0 Analog Input = – 40 to – 50dBm0 Analog Input = – 50 to – 55dBm0 Relative to – 10 dBm0	– .2 – .4 – 1.25	0.0 ± 0.1 ± 0.2	+ .2 + .4 + 1.25	dB dB dB
GT_R	Gain Tracking Receive CCITT G712 Method 2	Input Level = + 3 to – 40dBm0 Input Level = – 40 to – 50dBm0 Input Level = – 50 to – 55dBm0 Relative to – 10 dBm0	– .2 – .4 – 1.25	0.0 ± 0.1 ± 0.2	+ .2 + .4 + 1.25	dB dB dB
GT_{EE}	Gain Tracking End to End CCITT G712 Method 2	Analog Input = + 3 to – 40dBm0 Analog Input = – 40 to – 50dBm0 Analog Input = – 50 to – 55dBm0 Relative to – 10 dBm0	– 0.4 – 0.8 – 2.5	± 0.1 ± 0.1 ± 0.2	+ 0.4 + 0.8 + 2.5	dB dB dB
$SD1_X$	Signal to Distortion Transmit CCITT G712 Method 1	Analog Input = – 3dBm0 Analog Input = – 6 to – 27dBm0 Analog Input = – 34dBm0 Analog Input = – 40dBm0 Analog Input = – 55dBm0 Narrow Band Noise Input	30 36 34 30 15			dB dB dB dB dB
$SD1_R$	Signal to Distortion Receive CCITT G712 Method 1	Input Level = – 3dBm0 Input Level = – 6 to – 27dBm0 Input Level = – 34dBm0 Input Level = – 40dBm0 Input Level = – 55dBm0 Narrow Band Noise Input	30 37 35 31 16			dB dB dB dB dB
$SD2_X$	Signal to Distortion Transmit CCITT G712 Method 2	Analog Input = 0 to – 30dBm0 Analog Input = – 40dBm0 Analog Input = – 45dBm0	37 31 25			dB dB dB
$SD2_R$	Signal to Distortion Receive CCITT G712 Method 2	Input Level = 0 to – 30dBm0 Input Level = – 40dBm0 Input Level = – 45dBm0	37 31 25			dB dB dB
SD_{EE}	Signal to Distortion End to End CCITT G712 Method 2	Analog Input = 0 to – 30dBm0 Analog Input = – 40dBm0 Analog Input = – 45dBm0	35 29 24	39 34 29		db db dB
N_X	Idle Channel Noise Transmit	Analog Input = 0Volts			– 68	dBm0p
N_R	Idle Channel Noise Receive	Digital Input = + 0 Code			– 90	dBm0p
N_{EE}	Idle Channel Noise End to End	Analog Input = 0Volts		– 80	– 68	dBm0p
CT_{RX}	Crosstalk Receive to Transmit	Analog In = – 50dBm0 at 2600Hz Digital Input = 0dBm0 at 1008Hz Digital			– 80	dB
CT_{XR}	Crosstalk Transmit to Receive	Analog In = 0dBm0 at 1008Hz Digital Input = + 0 Code			– 80	dB
TLP	Transmission Level Point	600Ω		+ 4		dB

Notes :
1. - V_{REF} and - V_{REF} must be matched within ±1 % in order to meet system requirements.
2. Sampling is accomplished by charging an internal capacitor ; therefore, the designer should avoid excessive source impedance Input related device characteristics are derived using the Recommended Analog Input Circuit. See figure 6.
3. When a transition from a "1" to a "0" takes place, the user must sink the "1" current until reading the "0" level
4. Driving 30pF with I_{OH} = - 100 µA, I_{OL} - 500 µA
5. Results in 30mW typical power dissipation (clocks applied) under normal operating conditions
6. This delay is necessary to avoid overlapping Clock and Sync.
7. This first bit of data is loaded when Sync and Clock are both "1" during bit time 1 as shown on RCV timing diagram

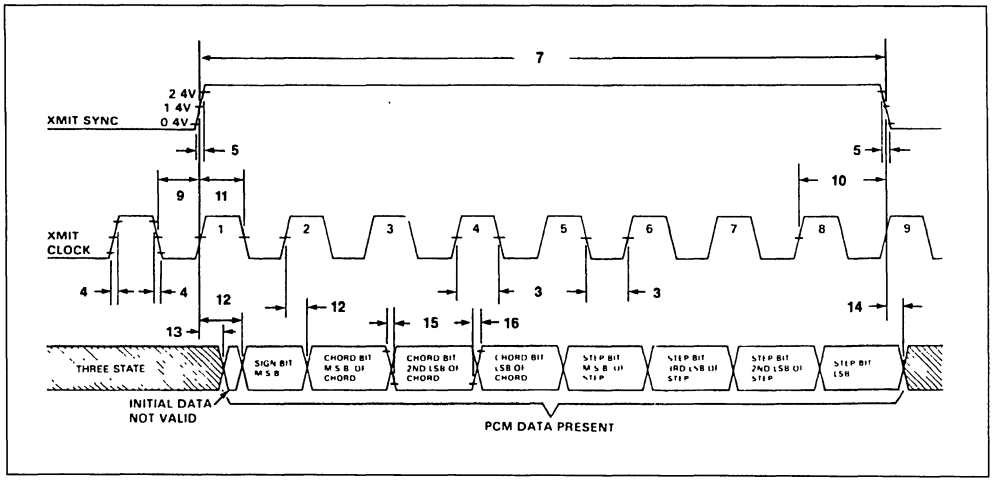
Figure 6 : Recommended Analog Input Circuit.



TIMING SPECIFICATIONS (refer to figures 7 and 8)

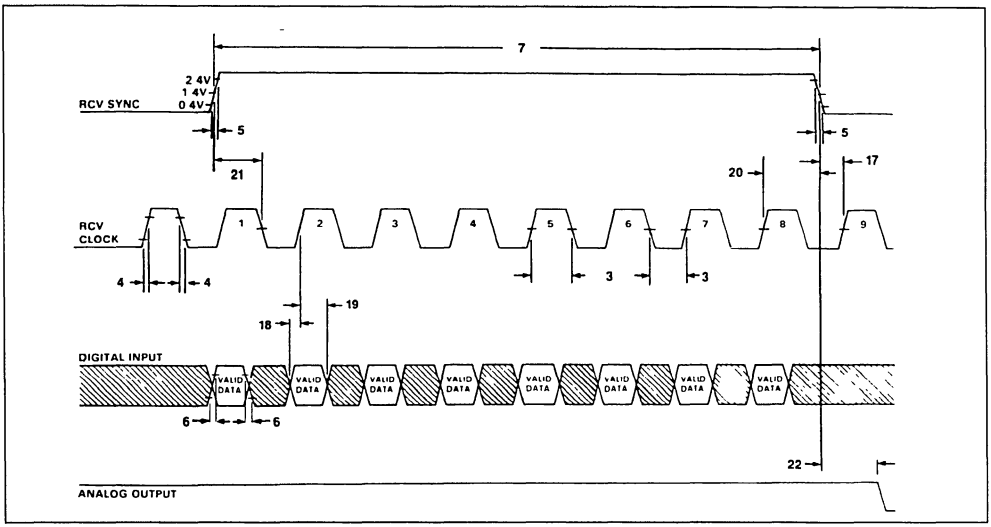
#	Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
1	F_M	Master Clock Frequency	1.5	2.048	2.1	MHz	
2	F_R, F_X	XMIT, RCV Clock Frequency	0.064	2.048	2.1	MHz	
3	PW_{CLK}	Clock Pulse Width (MASTER, XMIT, RCV)	200			ns	
4	t_{RC}, t_{FC}	Clock Rise, Fall Time (MASTER, XMIT, RCV)			25% of PW_{CLK}	ns	
5	t_{RS}, t_{FS}	Sync Rise, Fall Time (XMIT, RCV)			25% of PW_{CLK}	ns	
6	t_{DIR}, t_{DIF}	Data Input Rise, Fall Time			25% of PW_{CLK}	ns	
7	t_{WSX}, t_{WSR}	Sync Pulse Width (XMIT RCV)		$\frac{8}{F_X(F_R)}$		μs	
8	t_{PS}	Sync Pulse Period (XMIT, RCV)		125		μs	
9	t_{XCS}	XMIT Clock-to-XMIT Sync Delay	50% of t_{FC} (t_{RS})			ns	6
10	t_{XCSN}	XMIT Clock-toXMIT Sync (negative edge) Delay	200			ns	
11	t_{XSS}	XMIT Sync Set-up Time	200			ns	
12	t_{XDD}	XMIT Data Delay	0		200	ns	4
13	t_{XDP}	XMIT Data Present	0		200	ns	4
14	t_{XDT}	XMIT Data Three State			150	ns	4
15	t_{DOF}	Digital Output Fall Time		50	100	ns	4
16	t_{DOR}	Digital Output Rise Time		50	100	ns	4
17	t_{SRC}	RVC Sync-to-RCV Clock Delay	50% of t_{RC} (t_{FS})			ns	6
18	t_{RDS}	RCV Data Set-up Time	50			ns	7
19	t_{RDH}	RCV Data Hold Time	200			ns	7
20	t_{RCS}	RCV Clock-to-RCV Sync Delay	200			ns	
21	t_{RSS}	RCV Sync Set-up Time	200			ns	7
22	t_{SAO}	RCV Sync-to-analog Output Delay		7		μs	
23	SLEW+	Analog Output Positive Slew Rate		1		V/μs	
24	SLEW–	Analog Output Negative Slew Rate		1		V/μs	
25	DROOP	Analog Output Droop Rate		25		μV/μs	

Figure 7 : Transmitter Section Timing.



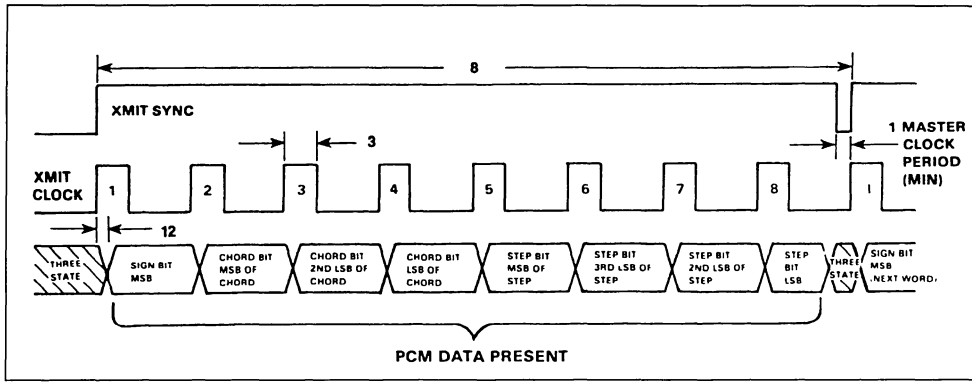
Note : All rise and fall times are measured from 0.4V and 2.4V. All delay times are measured from 1.4V.

Figure 8 : Receiver Section Timing.



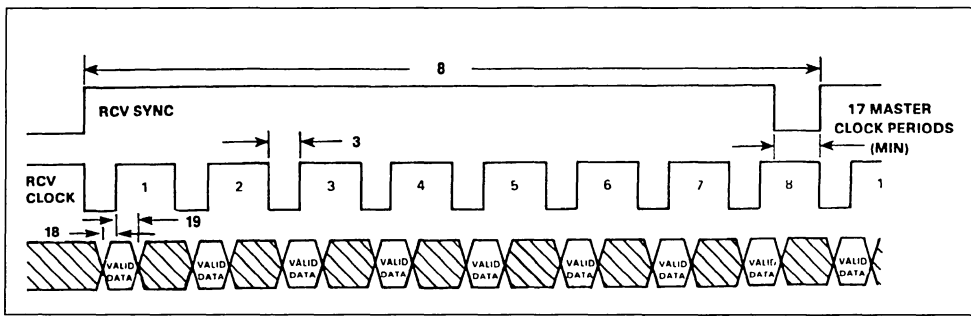
Note : All rise and fall times are measured from 0.4V and 2.4V. All delay times are measured from 1.4V.

Figure 9 : 64kHz Operation, Transmitter Section Timing.



Note : All rise and fall times are measured from 0.4V and 2 4V. All delay times are measured from 1 4V.

Figure 10 : 64kHz Operation, Receiver Section Timing.



Note : All rise and fall times are measured from 0.4V and 2.4V. All delay times are measured from 1.4V.

Figure 11 : M5156 Single-ended Signal to Distortion.

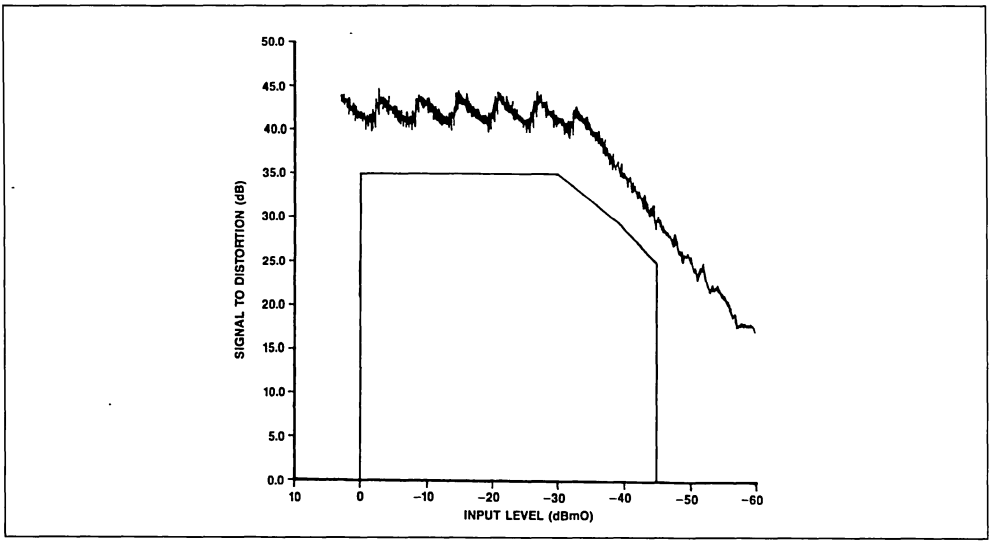
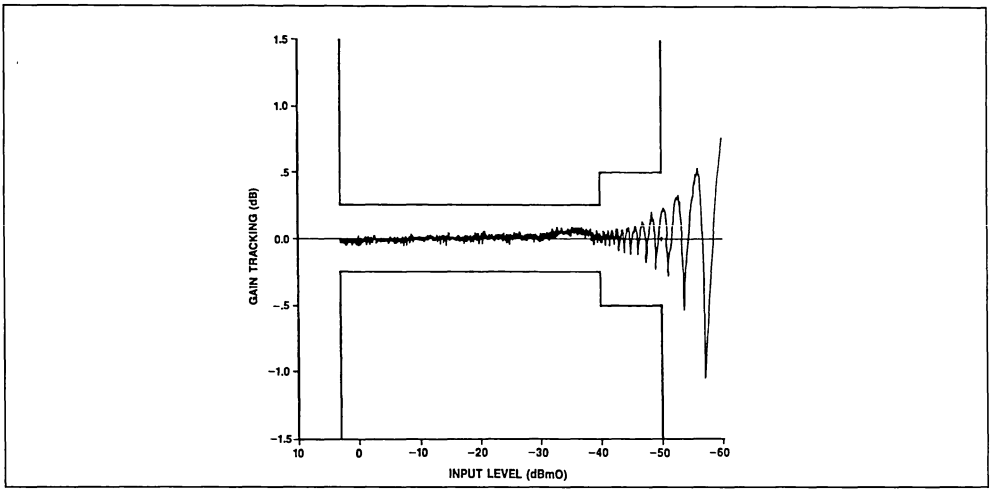


Figure 12 : M5156 Single-ended Gain Tracking.



SGS-THOMSON MICROELECTRONICS

ETC5057
ETC5054

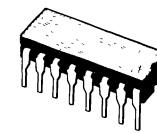
SERIAL INTERFACE CODEC/FILTER

- COMPLETE CODEC AND FILTERING SYSTEM (COMBO) INCLUDING :
  - Transmit high-pass and low-pass filtering
  - Receive low-pass filter with sin x/x correction
  - Active RC noise filters
  - A-law or μ-law compatible COder and DECoder
  - Internal precision voltage reference
  - Serial I/O interface
  - Internal auto-zero circuitry
- A-LAW, 16-PINS-ETC5057
- μ-LAW WITHOUT SIGNALING, 16-PINS-ETC5054
- MEETS OR EXCEEDS ALL D3/D4 AND CCITT SPECIFICATIONS
- ± 5 V OPERATION
- LOW OPERATING POWER - TYPICALLY 60 mW
- POWER-DOWN STANDBY - TYPICALLY 3 mW
- AUTOMATIC POWER-DOWN
- TTL OR CMOS COMPATIBLE DIGITAL INTERFACES
- MAXIMIZES LINE INTERFACE CARD CIRCUIT DENSITY
- SECOND SOURCE OF TP3057, TP3054

DESCRIPTION

The ETC5057/ETC5054 family consists of A-law and μ-law monolithic PCM CODEC/filters utilizing the A/D and D/A conversion architecture shown in figure 1, and a serial PCM interface. The devices are fabricated using double poly CMOS process.

The encode portion of each device consists of an input gain adjust amplifier, an active RC pre-filter which eliminates very high frequency noise prior to entering a switched-capacitor band-pass filter that rejects signals below 200 Hz and above 3400 Hz. Also included are auto-zero circuitry and a companding coder which samples the filtered signal and encodes it in the companded A-law or μ-law PCM format. The decode portion of each device consists of an expanding decoder, which reconstructs the analog signal from the companded A-law or μ-law code, a low-pass filter which corrects for the sin x/x response of the decoder output and rejects signals above 3400 Hz and is followed by a single-ended power amplifier capable of driving low impedance loads. The devices require 1.536 MHz, 1.544 MHz, or 2.048 MHz transmit and receive master clocks, which may be asynchronous, transmit and receive bit clocks which may vary from 64 kHz to 2.048 MHz, and transmit and receive frame sync pulses. The timing of the frame sync pulses and PCM data is compatible with both industry standard formats.



DIP16
(Ceramic) J
(Plastic) N

ORDER CODES : ETC5057J
ETC5054J
ETC5057N
ETC5054N

PIN CONNECTION

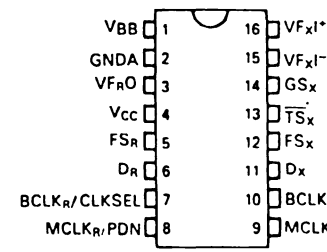
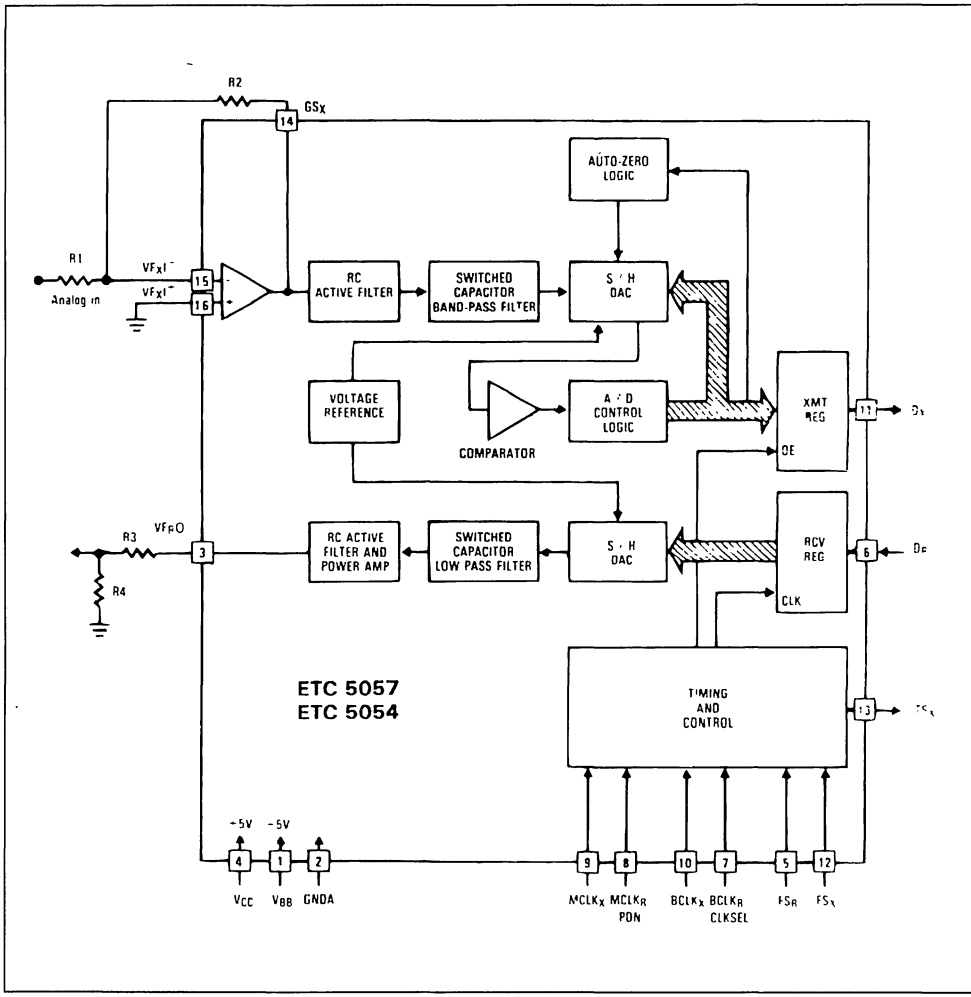


Figure 1 : Block Diagram.



PIN DESCRIPTION

Name	Pin Type*	N°	Function	Description
V_{BB}	S	1	Negative Power Supply	$V_{BB} = -5\ V \pm 5\ \%$
GNDA	GND	2	Analog Ground	All signals are referenced to this pin.
VF_RO	O	3	Receiver Filter Output	Analog Output of the Receive Filter
V_{CC}	S	4	Positive Power Supply	$V_{CC} = +5\ V \pm 5\ \%$
FS_R	I	5	Receive Frame Sync Pulse	Enables $BCLK_R$ to shift PCM data into D_R. FS_R is an 8 kHz pulse train. See figures 2,3 and 4 for timing details.
D_R	I	6	Receive Data Input	PCM data is shifted into D_R following the FS_R leading edge.
$BCLK_R$/CLKSEL	I	7	Shift-in Clock	Shifts data into D_R after the FS_R leading edge. May vary from 64 kHz to 2.048 MHz. Alternatively, may be a logic input which selects either 1.536 MHz/1.544 MHz or 2.048 MHz for master clock in synchronous mode and $BCLK_X$ is used for both transmit and receive directions (see table 1). This input has an internal pull-up.
$MCLK_R$/PDN	I	8	Receive Master Clock	Must be 1.536 MHz, 1.544 MHz or 2.048 MHz. May be asynchronous with $MCLK_X$, but should be synchronous with $MCLK_X$ for best performance. When $MCLK_R$ is connected continuously low, $MCLK_X$ is selected for all internal timing. When $MCLK_R$ is connected continuously high, the device is powered down.
$MCLK_X$	I	9	Transmit Master Clock	Must be 1.536 MHz, 1.544 MHz or 2.048 MHz. May be asynchronous with $MCLK_R$.
$BCLK_X$	I	10	Shift out Clock	Shift out the PCM data on D_X. May vary from 64 kHz to 2.048 MHz, but must be synchronous with $MCLK_X$.
D_X	O	11	Transmit Data Output	The TRI-STATE® PCM data output which is enabled by FS_X.
FS_X	I	12	Transmit Frame Sync Pulse	Enables $BCLK_X$ to shift out the PCM data on D_X. FS_X is an 8 kHz pulse train. See figures 2, 3 and 4 for timing details.
$\overline{TS_X}$	O	13	Transmit Time Slot	Open drain output which pulses low during the encoder time slot. Recommended to be grounded if not used.
GS_X	O	14	Gain Set	Analog output of the transmit input amplifier. Used to set gain externally.
VF_XI^-	I	15	Inverting Amplifier Input	Inverting input of the transmit input amplifier.
VF_XI^+	I	16	Non-inverting Amplifier Input	Non-inverting input of the transmit input amplifier.

* I : Input, o : Output, S : Power Supply.
TRI-STATE ® is a trademark of National Semiconductor Corp.

FUNCTIONAL DESCRIPTION

POWER-UP

When power is first applied, power-on reset circuitry initializes the COMBO and places it into the power-down mode. All non-essential circuits are deactivated and the D_X and VF_RO outputs are put in high impedance states. To power-up the device, a logical low level or clock must be applied to the $MCLK_R$/PDN pin and FS_X and/or FS_R pulses must be present. Thus, 2 power-down control modes are available. The first is to pull the $MCLK_R$/PDN pin high ; the alternative is to hold both FS_X and FS_R inputs continuously low. The device will power-down approximately 2 ms after the last FS_X or FS_R pulse. Power-up will occur on the first FS_X or FS_R pulse. The TRI-STATE PCM data output, D_X, will remain in the high impedance state until the second FS_X pulse.

SYNCHRONOUS OPERATION

For synchronous operation, the same master clock and bit clock should be used for both the transmit and receive directions. In this mode, a clock must be applied to $MCLK_X$ and the $MCLK_R$/PDN pin can be used as a power-down control. A low level on $MCLK_R$/PDN powers up the device and a high level powers down the device. In either case, $MCLK_X$ will be selected as the master clock for both the transmit and receive circuits. A bit clock must also be applied to $BCLK_X$ and the $BCLK_R$/CLKSEL can be used to select the proper internal divider for a master clock of 1.536 MHz, 1.544 MHz or 2.048 MHz. For 1.544 MHz operation, the device automatically compensates for the 193 rd clock pulse each frame.

With a fixed level on the $BCLK_R$/CLKSEL pin, $BCLK_X$ will be selected as the bit clock for both the transmit and receive directions. Table 1 indicates the frequencies of operation which can be selected, depending on the state of $BCLK_R$/CLKSEL. In this synchronous mode, the bit clock, $BCLK_X$, may be from 64 kHz to 2.048 MHz, but must be synchronous with $MCLK_X$.

Table 1: Selection of Master Clock Frequencies.

$BCLK_R$/CLKSEL	Master Clock Frequency Selected	
	ETC 5057	ETC 5054
Cloked	2.048 MHz	1.536 MHz or 1.544 MHz
0	1.536 MHz or 1.544 MHz	2.048 MHz
1 (or open circuit)	2.048 MHz	1.536 MHz or 1.544 MHz

Each FS_X pulse begins the encoding cycle and the PCM data from the previous encode cycle is shifted out of the enabled D_X output on the positive edge of $BCLK_X$. After 8 bit clock periods, the TRI-STATE D_X output is returned to a high impedance state. With an FS_R pulse, PCM data is latched via the D_R input on the negative edge of $BCLK_X$ (or $BCLK_R$ if running). FS_X and FS_R must be synchronous with $MCLK_{X/R}$.

ASYNCHRONOUS OPERATION

For asynchronous operation, separate transmit and receive clocks may be applied. $MCLK_X$ and $MCLK_R$ must be 2.048 MHz for the ETC5057, or 1.536 MHz, 1.544 MHz for the ETC5054, and need not be synchronous. For best transmission performance, however, $MCLK_R$ should be synchronous with $MCLK_X$, which is easily achieved by applying only static logic levels to the $MCLK_R$/PDN pin. This will automatically connect $MCLK_X$ to all internal $MCLK_R$ functions (see Pin Description). For 1.544 MHz operation, the device automatically compensates for the 193 rd clock pulse each frame. FS_X starts each encoding cycle and must be synchronous with $MCLK_X$ and $BCLK_X$. FS_R starts each decoding cycle and must be synchronous with $BCLK_R$. $BCLK_R$ must be a clock, the logic levels shown in Table 1 are not valid in asynchronous mode. $BCLK_X$ and $BCLK_R$ may operate from 64 kHz to 2.048 MHz.

SHORT FRAME SYNC OPERATION

The COMBO can utilize either a short frame sync pulse or a long frame sync pulse. Upon power initialization, the device assumes a short frame mode. In this mode, both frame sync pulses, FS_X and FS_R, must be one bit clock period long, with timing relationships specified in figure 3. With FS_X high during a falling edge of $BCLK_X$, the next rising edge of $BCLK_X$ enables the D_X TRI-STATE output buffer, which will output the sign bit. The following seven rising edges clock out the remaining seven bits, and the next falling edge disables the D_X output. With FS_R high during a falling edge of $BCLK_R$ ($BCLK_X$ in synchronous mode), the next falling edge of $BCLK_R$ latches in the sign bit. The following seven falling edges latch in the seven remaining bits. Both devices may utilize the short frame sync pulse in synchronous or asynchronous operating mode.

LONG FRAME SYNC OPERATION

To use the long frame mode, both the frame sync pulses, FS_X and FS_R, must be three or more bit clock periods long, with timing relationships specified in figure 4. Based on the transmit frame sync, FS_X, the

COMBO will sense whether short or long frame sync pulses are being used. For 64 kHz operation, the frame sync pulse must be kept low for a minimum of 160 ns (see fig. 2). The D_X TRI-STATE output buffer is enabled with the rising edge of FS_X or the rising edge of $BCLK_X$, whichever comes later, and the first bit clocked out is the sign bit. The following seven $BCLK_X$ rising edges clock out the remaining seven bits. The D_X output is disabled by the falling $BCLK_X$ edge following the eighth rising edge, or by FS_X going low, whichever comes later. A rising edge on the receive frame sync pulse, FS_R, will cause the PCM data at D_R to be latched in on the next eight falling edges of $BCLK_R$ ($BCLK_X$ in synchronous mode). Both devices may utilize the long frame sync pulse in synchronous or asynchronous mode.

TRANSMIT SECTION

The transmit section input is an operational amplifier with provision for gain adjustment using two external resistors, see figure 5. The low noise and wide bandwidth allow gains in excess of 20 dB across the audio passband to be realized. The op amp drives a unity-gain filter consisting of RC active pre-filter, followed by an eighth order switched-capacitor bandpass filter clocked at 256 kHz. The output of this filter directly drives the encoder sample-and-hold circuit. The A/D is of companding type according to A-law (ETC5057) or μ-law (ETC5054) coding conventions. A precision voltage reference is trimmed in manufacturing to provide an input overload (t_{MAX}) of nominally 2.5 V peak (see table of Transmission Characteristics). The FS_X frame sync pulse controls the sampling of the filter output, and then the successive-approximation encoding cycle begins. The 8-bit code is then loaded into a buffer and shifted out through D_X at the next FS_X pulse. The total encoding delay will be approximately 165 μs (due to the transmit filter) plus 125 μs (due to encoding delay), which totals 290 μs. Any offset voltage due to the filters or comparator is cancelled by sign bit integration.

RECEIVE SECTION

The receive section consists of an expanding DAC which drives a fifth order switched-capacitor low pass filter clocked at 256 kHz. The decoder is A-law (ETC5057) or μ-law (ETC5054) and the 5th order low pass filter corrects for the sin x/x attenuation due to the 8 kHz sample and hold. The filter is then followed by a 2 nd order RC active post-filter and power amplifier capable of driving ja 600 Ω load to a level of 7.2 dBm. The receive section is unity-gain. Upon the occurence of FS_R, the data at the D_R input is clocked in on the falling edge of the next eight $BCLK_R$ ($BCLK_X$) periods. At the end of the decoder time slot, the decoding cycle begins, and 10 μs later the decoder DAC output is updated. The total decoder delay is ~ 10 μs (decoder update) plus 110 μs (filter delay) plus 62.5 μs (1/2 frame), which gives approximately 180 μs.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	V_{CC} to GNDA	7	V
V_{BB}	V_{BB} to GNDA	– 7	V
V_{IN} V_{OUT}	Voltage at Any Analog Input or Output	V_{CC} + 0.3 to V_{BB} – 0.3	V
	Voltage at Any Digital Input or Output	V_{CC} + 0.3 to GNDA – 0.3	V
T_{oper}	Operating Temperature Range	– 25 to + 125	°C
T_{stg}	Storage Temeperature Range	– 65 to + 150	°C
	Lead Temperature (soldering, 10 seconds)	300	°C

ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0 V ± 5 %, V_{BB} = – 5.0 V ± 5 %, GNDA = 0 V, T_A = 0 °C to 70 °C (unless otherwise noted) ; Typical characteristics specified at V_{CC} = 5.0 V, V_{BB} = – 5.0 V, T_A = 25 °C ; all signals are referenced to GNDA.

DIGITAL INTERFACE

Symbol	Parameter		Min.	Typ.	Max.	Unit
V_{IL}	Input Low Voltage		–	–	0.6	V
V_{IH}	Input High Voltage		2.2	–	–	V
V_{OL}	Output Low Voltage					V
	I_L = 3.2 mA	D_X	–	–	0.4	
	I_L = 3.2 mA, Open Drain	$\overline{TS_X}$	–	–	0.4	
V_{OH}	Output High Voltage					V
	I_H = 3.2 mA	D_X	2.4	–	–	
I_{IL}	Input Low Current (GNDA ≤ V_{IN} ≤ V_{IL}, all digital inputs)		– 10	–	10	µA
I_{IH}	Input High Current (V_{IH} ≤ V_{IN} ≤ V_{CC}) except $BCLK_R$/BCLKSEL		– 10	–	10	µA
I_{OZ}	Output Current in High Impedance State (TRI–STATE)					µA
	(GNDA ≤ V_0 ≤ V_{CC})	D_X	– 10	–	10	

ANALOG INTERFACE WITH TRANSMIT INPUT AMPLIFIER (all devices)

Symbol	Parameter		Min.	Typ.	Max.	Unit
I_IXA	Input Leakage Current (– 2.5 V ≤ V ≤ + 2.5 V)	VF_XI^+ or VF_XI^-	– 200	–	200	nA
R_IXA	Input Resistance (– 2.5 ≤ V ≤ + 2.5 V)	VF_XI^+ or VF_XI^-	10	–	–	MΩ
R_OXA	Output Resistance (closed loop, unity gain)		–	1	3	Ω
R_LXA	Load Resistance	GS_X	10	–	–	kΩ
C_LXA	Load Capacitance	GS_X	–	–	50	pF
V_OXA	Output Dynamic Range (R_L ≥ 10 kΩ)	GS_X	± 2.8	–	–	V
A_VXA	Voltage Gain (VF_XI^+ to GS_X)		5000	–	–	V/V
F_UXA	Unity Gain Bandwidth		1	2	–	MHz
$V_{OS}XA$	Offset Voltage		– 20	–	20	mV
$V_{CM}XA$	Common-mode Voltage		– 2.5	–	2.5	V
CMRRXA	Common-mode Rejection Ratio		60	–	–	dB
PSRRXA	Power Supply Rejection Ratio		60	–	–	dB

ANALOG INTERFACE WITH RECEIVE FILTER (all devices)

Symbol	Parameter		Min.	Typ.	Max.	Unit
R_ORF	Output Resistance	VF_RO	–	1	3	Ω
R_LRF	Load Resistance (VF_RO = ± 2.5 V)		600	–	–	Ω
C_LRF	Load Capacitance		–	–	500	pF
VOS_RO	Output DC Offset Voltage		– 200	–	200	mV

ELECTRICAL CHARACTERISTICS (continued)

POWER DISSIPATION (all devices)

Symbol	Parameter	Min.	Typ.	Max.	Unit
$I_{CC}0$	Power-down Current	–	0.5	1.5	mA
$I_{BB}0$	Power-down Current	–	0.05	0.3	mA
$I_{CC}1$	Active Current	–	6.0	9.0	mA
$I_{BB}1$	Active Current	–	6.0	9.0	mA

TIMING SPECIFICATIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
$1/t_{PM}$	Frequency of Master Clocks $MCLK_X$ and $MCLK_R$ Depends on the device used and the $BCLK_R$/CLKSEL pin.	– – –	1.536 1.544 2.048	– – –	MHz
t_{WMH}	Width of Master Clock High $MCLK_X$ and $MCLK_R$	160	–	–	ns
t_{WML}	Width of Master Clock Low $MCLK_X$ and $MCLK_R$	160	–	–	ns
t_{RM}	Rise Time of Master Clock $MCLK_X$ and $MCLK_R$	–	–	50	ns
t_{FM}	Fall Time of Master Clock $MCLK_X$ and $MCLK_R$	–	–	50	ns
t_{PB}	Period of Bit Clock	485	488	15.725	ns
t_{WBH}	Width of Bit Clock High (V_{IH} = 2.2 V)	160	–	–	ns
t_{WBL}	Width of Bit Clock Low (V_{IL} = 0.6 V)	160	–	–	ns
t_{RB}	Rise Time of Bit Clock (t_{PB} = 488 ns)	–	–	50	ns
t_{FB}	Fall Time of Bit Clock (t_{PB} = 488 ns)	–	–	50	ns
t_{SBFM}	Set-up Time from $BCLK_X$ High to $MCKL_X$ Falling Edge (first bit clock after the leading edge of FS_X)	100	–	–	ns
t_{HBF}	Holding Time from Bit Clock Low to the Frame Sync (long frame only)	0	–	–	ns
t_{SFB}	Set-up Time from Frame Sync to Bit Clock Low (long frame only)	80	–	–	ns
t_{HBFI}	Hold Time from 3rd Period of Bit Clock Low to Frame Sync (long frame only) FS_X or FS_R	100	–	–	ns
t_{DZF}	Delay time to valid data from FS_X or $BCLK_X$, whichever comes later and delay time from FS_X to data output disabled. (C_L = 0 pF to 150 pF)	20	–	165	ns
t_{DBD}	Delay Time from $BCLK_X$ High to Data Valid (Load = 150 pF plus 2 LSTTL loads)	0	–	180	ns
t_{DZC}	Delay Time from $BCLK_X$ Low to Data Output Disabled	50	–	165	ns
t_{SDB}	Set-up Time from D_R Valid to $BCLK_{R/X}$ Low	50	–	–	ns
t_{HBD}	Hold Time from $BCLK_{R/X}$ Low to D_R Invalid	50	–	–	ns
t_{HOLD}	Holding Time from Bit Clock High to Frame Sync (short frame only)	0	–	–	ns

Note : 1. For short frame sync timing FS_X and FS_R must go high while their respective bit clocks are high.

TIMING SPECIFICATIONS (continued)

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{SF}	Set-up Time from $FS_{X/R}$ to $BCLK_{X/R}$ Low (short frame sync pulse) - Note 1	80	–	–	ns
t_{HF}	Hold Time from $BCLK_{X/R}$ Low to $FS_{X/R}$ Low (short frame sync pulse) - Note 1	100	–	–	ns
t_{XDP}	Delay Time. To TS_X Low (load = 150 pF plus 2 LSTTL loads)	–	–	140	ns
t_{WFL}	Minimum Width of the Frame Sync Pulse (low level) (64 k bit/s operating mode)	160	–	–	ns

Note : 1. For short frame sync timing FS_X and FS_R must go high while their respective bit clocks are high.

Figure 2 : 64 k bits/s TIMING DIAGRAM (see next page for complete timing).

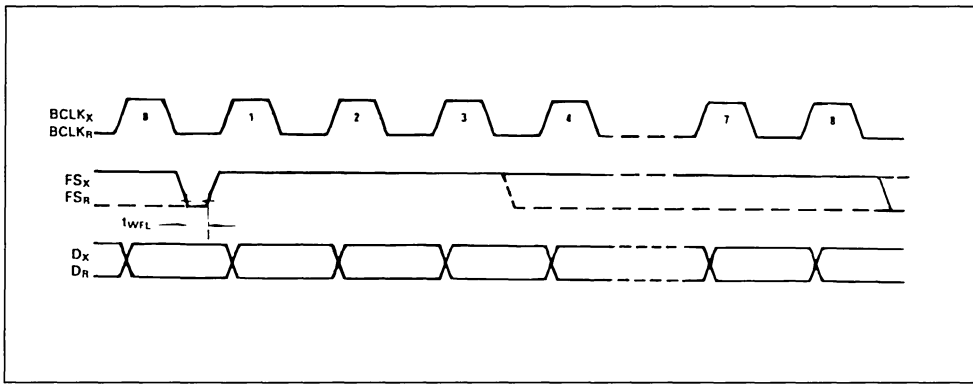


Figure 3 : Short Frame Sync Timing.

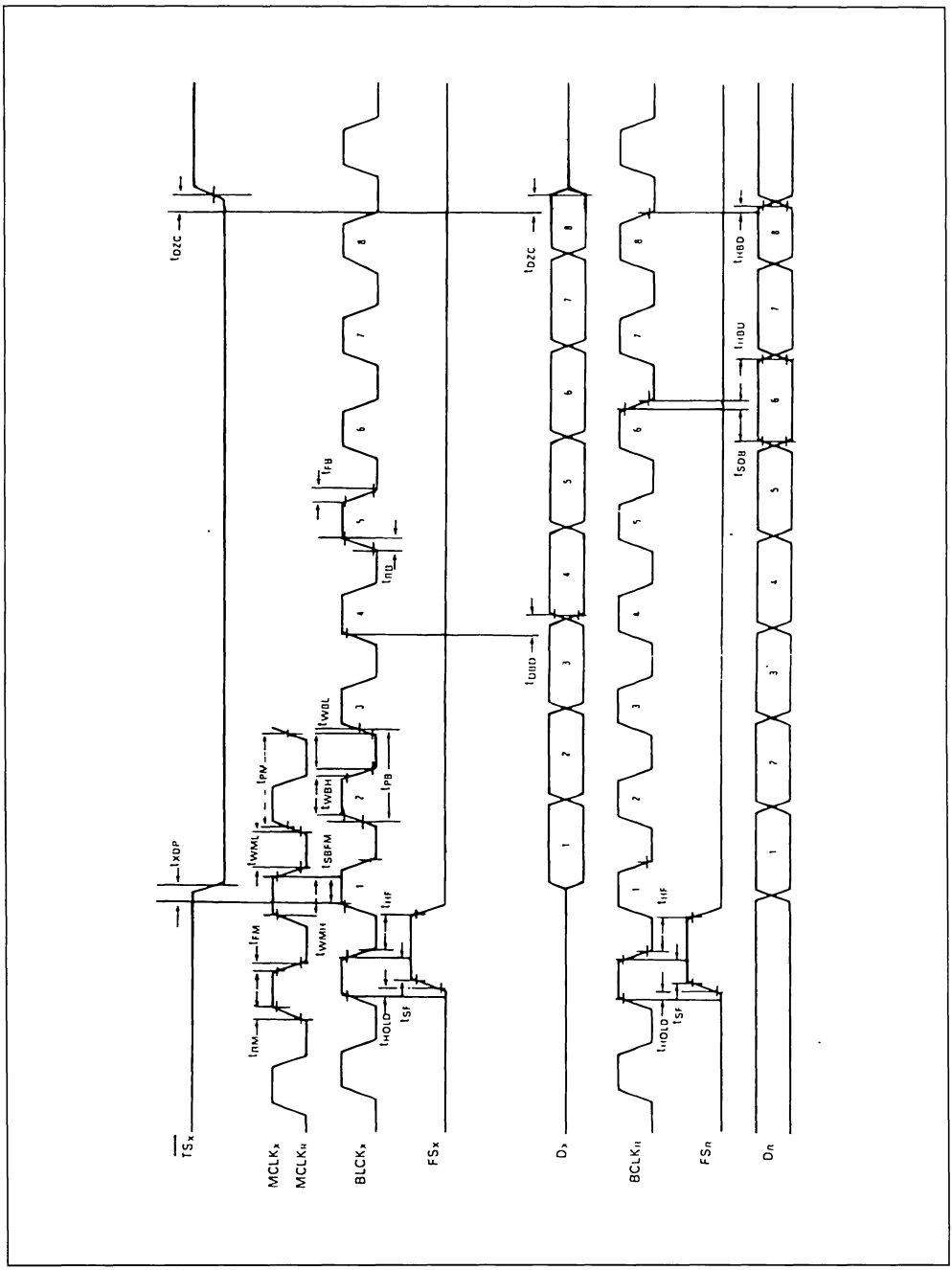
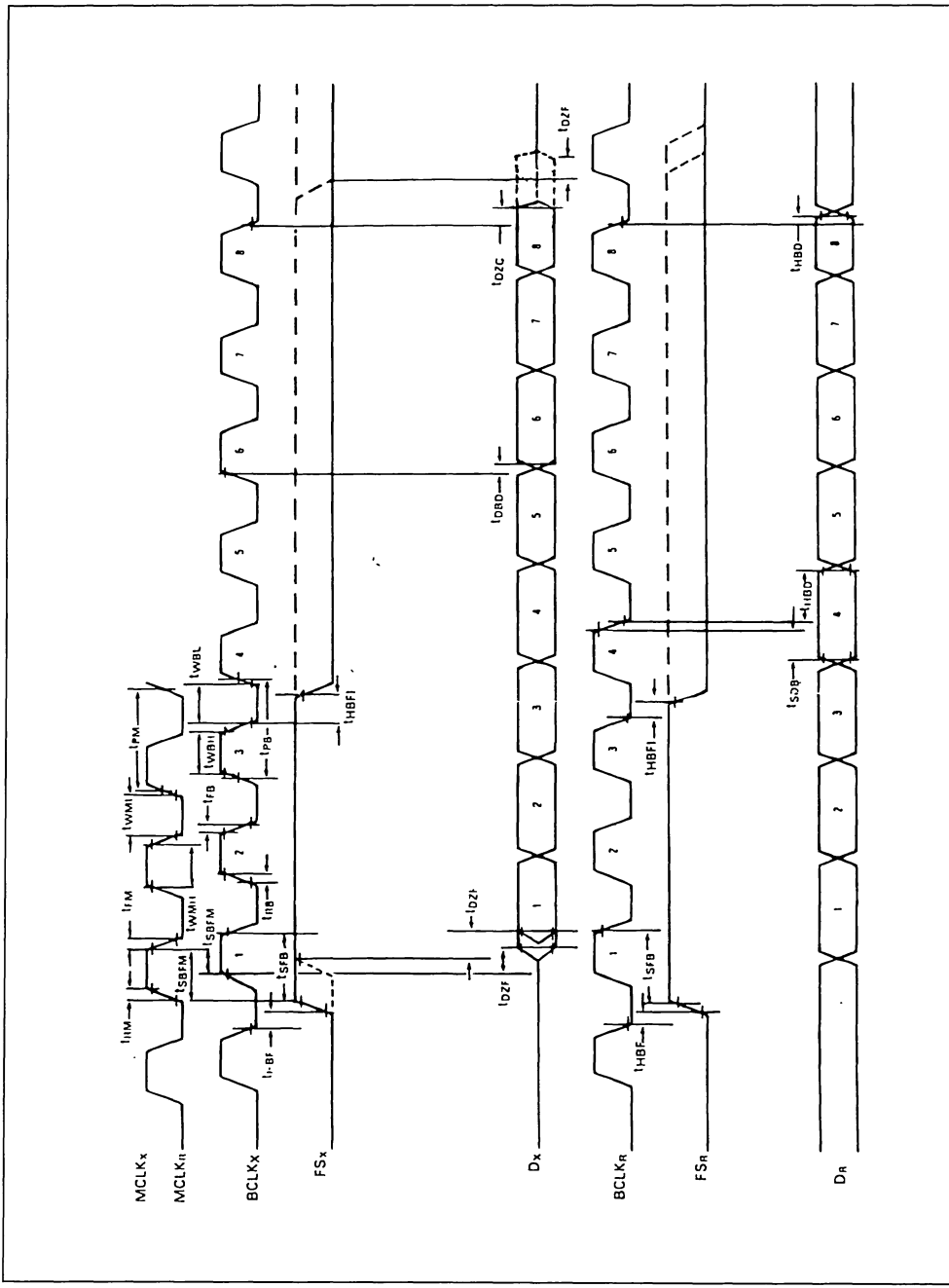


Figure 4 : Long Frame Sync Timing.



TRANSMISSION CHARACTERISTICS

(all devices) T_A = 0 °C to 70 °C, V_{CC} = 5 V ± 5 %, V_{BB} = – 5 V ± 5 %, GNDA = 0 v, f = 1.02 kHz, V_{IN} = 0 dBm0 transmit input amplifier connected for unity-gain non-inverting (unless otherwise specified).

AMPLITUDE RESPONSE

Symbol	Parameter	Min.	Typ.	Max.	Unit
	Absolute Levels – Nominal 0 dBm0 level is 4 dBm (600 Ω). 0 dBm0	–	1.2276	–	V_{rms}
t_{MAX}	Max Overload Level 3.14 dBm0 (A LAW) 3.17 dBm0 (U LAW)	 – –	 2.492 2.501	 – –	V_{PK}
G_{XA}	Transmit Gain, Absolute (T_A = 25 °C, V_{CC} = 5 V, V_{BB} = – 5 V) Input at GS_X = 0 dBm0 at 1020 Hz	 – 0.15	 –	 0.15	dB
G_{XR}	Transmit Gain, Relative to G_{XA} f = 16 Hz f = 50 Hz f = 60 Hz f = 180 Hz f = 200 Hz f = 300 Hz – 3000 Hz f = 3300 Hz f = 4000 Hz f = 3400 Hz f = 4600 Hz and up, measure response from 0 Hz to 4000 Hz	 – – – – 2.8 – 1.8 – 0.15 – 0.35 – 0.7 – –	 – – – – – – – – – – –	 – 40 – 30 – 26 – 0.2 – 0.1 0.15 0.05 0 – 14 – 32	dB
G_{XAT}	Absolute Transmit Gain Variation with Temperature (T_A = 0 °C to + 70 °C)	 – 0.1	 –	 + 0.1	dB
G_{XAV}	Absolute Transmit Gain Variation with Supply Voltage (V_{CC} = 5 V ± 5 %, V_{BB} = – 5 V ± 5 %)	 – 0.05	 –	 + 0.05	dB
G_{XRL}	Transmit Gain Variations with Level Sinusoidal Test Method Reference Level = – 10 dBm0 VF_XI^+ = – 40 dBm0 to + 3 dBm0 VF_XI^+ = – 50 dBm0 to – 40 dBm0 VF_XI^+ = – 55 dBm0 to – 50 dBm0	 – 0.2 – 0.4 – 1.2	 – – –	 0.2 0.4 1.2	dB
G_{RA}	Receive Gain, Absolute (T_A = 25 °C, V_{CC} = 5 V, V_{BB} = – 5 V) Input = Digital Code Sequence for 0 dBm0 Signal at 1020 Hz	 – 0.15	 –	 0.15	dB
G_{RR}	Receive Gain, Relative to G_{RA} f= 0 Hz to 3000 Hz f = 3300 Hz f = 3400 Hz f = 4000 Hz	 – 0.15 – 0.35 – 0.7 –	 – – – –	 0.15 0.05 0 – 14	dB
G_{RAT}	Absolute Receive Gain Variation with Temperature (T_A = 0 °C to + 70 °C)	 – 0.1	 –	 + 0.1	dB
G_{RAV}	Absolute Receive Gain Variation with Supply Voltage (V_{CC} = 5 V ± 5 %, V_{BB} = – 5 V ± 5 %)	 – 0.05	 –	 + 0.05	dB
G_{RRL}	Receive Gain Variations with Level Sinusoidal Test Method ; Reference input PCM code corresponds to an ideally encoded – 10 dBm0 signal PCM level = – 40 dBm0 to + 3 dBm0 PCM level = – 50 dBm0 to – 40 dBm0 PCM level = – 55 dBm0 to – 50 dBm0	 – 0.2 – 0.4 – 1.2	 – – –	 0.2 0.4 1.2	dB
V_{RO}	Receive Output Drive Level (R_L = 600 Ω)	– 2.5	–	2.5	V

TRANSMISSION CHARACTERISTICS (continued)

ENVELOPE DELAY DISTORTION WITH FREQUENCY

Symbol	Parameter	Min.	Typ.	Max.	Unit
D_{XA}	Transmit Delay, Absolute (f = 1600 Hz)	–	290	315	µs
D_{XR}	Transmit Delay, Relative to D_{XA}				µs
	f = 500 Hz – 600 Hz	–	195	220	
	f = 600 Hz – 800 Hz	–	120	145	
	f = 800 Hz – 1000 Hz	–	50	75	
	f = 1000 Hz – 1600 Hz	–	20	40	
	f = 1600 Hz – 2600 Hz	–	55	75	
	f = 2600 Hz – 2800 Hz	–	80	105	
	f = 2800 Hz – 3000 Hz	–	130	155	
D_{RA}	Receive Delay, Absolute (f = 1600 Hz)	–	180	200	µs
D_{RR}	Receive Delay, Relative to D_{RA}				µs
	f = 500 Hz – 1000 Hz	– 40	– 25	–	
	f = 1000 Hz – 1600 Hz	– 30	– 20	–	
	f = 1600 Hz – 2600 Hz	–	70	90	
	f = 2600 Hz – 2800 Hz	–	100	125	
	f = 2800 Hz – 3000 Hz	–	145	175	

NOISE

Symbol	Parameter	Min.	Typ.	Max.	Unit
N_{XP}	Transmit Noise, P Message Weighted (A LAW, $VF_XI^+ = 0$ V)	–	– 74	– 69 (note 1)	dBM0p
N_{RP}	Receive Noise, P Message Weighted (U LAW, PCM Code Equals Positive Zero)	–	– 82	– 79	dBm0p
N_{XC}	Transmit Noise, C Message Weighted U LAW (VFXI + = 0 V)	–	12	15	dBrnC0
N_{RC}	Receive Noise, C Message Weighted (U LAW, PCM Code Equals Alternating Positive and Negative Zero)	–	8	11	dBrnC0
N_{RS}	Noise, Single Frequency f = 0 kHz to 100 kHz, Loop Around Measurement, $VF_XI^+ = 0$ Vrms	–	–	– 53	dBm0
$PPSR_X$	Positive Power Supply Rejection, Transmit $VF_XI^+ = 0$ Vrms, V_{CC} = 5.0 V_{DC} + 100 mVrms, f = 0 kHz – 50 kHz	40	–	–	dBp
$NPSR_X$	Negative Power Supply Rejection, Transmit $VF_XI^+ = 0$ Vrms, V_{BB} = – 5.0 V_{DC} + 100 mVrms, f = 0 kHz – 50 kHz	40	–	–	dBp
$PPSR_R$	Positive Power Supply Rejection, Receive (PCM code equals positive zero, V_{CC} = 5.0 V_{DC} + 100 mVrms)				
	f = 0 Hz – 4000 Hz	40	–	–	dBp
	f = 4 kHz – 25 kHz	40	–	–	dB
	f = 25 kHz – 50 KHZ	36	–	–	dB
$NPSR_R$	Negative Power Supply Rejection, Receive (PCM code equals positive zero, V_{BB} = – 5.0 V_{DC} + 100 mVrms)				
	f = 0 Hz – 4000 Hz	40	–	–	dBp
	f = 4 kHz – 25 kHz	40	–	–	dB
	f = 25 kHz – 50 kHz	36	–	–	dB

TRANSMISSION CHARACTERISTICS (continued)

Symbol	Parameter	Min.	Typ.	Max.	Unit
SOS	Spurious out-of band signals at the channel output. Loop around measurement, 0 dBm0, 300 Hz – 3400 Hz input applied to VF_XI^+, measure individual image signals at VF_R0				dB
	4600 Hz – 7600 Hz	–	–	– 32	
	7600 Hz – 8400 Hz	–	–	– 40	
	8400 Hz – 100,000 Hz	–	–	– 32	

DISTORTION

Symbol	Parameter		Min.	Typ.	Max.	Unit
STD_X or STD_R	Signal to Total Distortion (sinusoidal test method) Transmit or Receive Half-channel					dBp
	Level = 3 dBm0		33	–	–	
	= 0 dBm0 to – 30 dBm0		36	–	–	
	= – 40 dBm0	XMT	29	–	–	
		RCV	30	–	–	
	= – 55 dBm0	XMT	14	–	–	
		RCV	15	–	–	
SFD_X	Single Frequency Distortion, Transmit		–	–	– 46	dB
SFD_R	Single Frequency Distortion, Receive		–	–	– 46	dB
IMD	Intermodulation Distortion Loop Around Measurement, VF_XI^+ = – 4 dBm0 to – 21 dBm0, Two Frequencies in the Range 300 Hz – 3400 Hz		–	–	– 41	dB

CROSSTALK

Symbol	Parameter	Min.	Typ.	Max.	Unit
CT_{X-R}	Transmit to Receive Crosstalk, 0 dBm0 Transmit Level f = 300 Hz – 3400 Hz, D_R = Steady PCM Mode	–	– 90	– 75	dB
CT_{R-X}	Receive to Transmit Crosstalk, 0 dBm0 Receive Level f = 300 Hz – 3400 Hz, VF_XI = 0 V	–	– 90	– 70 (note 2)	dB

Notes : 1. Theoretical worst-case for a perfectly zeroed encoder with alternating sign bit, due to the decoding law.
2. CT_{R-X} is measured with a – 40 dBm0 activating signal applied at VF_XI^+.

ENCODING FORMAT AT D_X OUTPUT

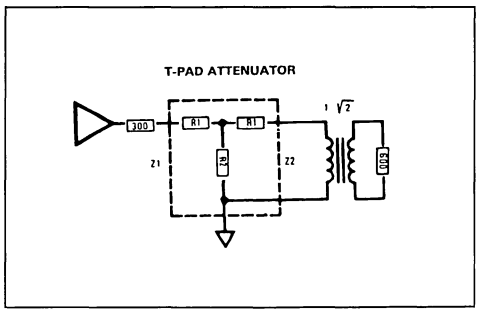
	A–Law (includes even bit inversion)	μLaw
V_{IN} (at GS_X) = + Full-scale	1 0 1 0 1 0 1 0	1 0 0 0 0 0 0 0
V_{IN} (at GS_X) = 0 V	1 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1	1 1 1 1 1 1 1 1 0 1 1 1 1 1 1 1
V_{IN} (at GS_X) = – Full-scale	0 0 1 0 1 0 1 0	0 0 0 0 0 0 0 0

APPLICATIONS INFORMATION

POWER SUPPLIES

While the pins of the ETC5050 family are well protected against electrical misuse, it is recommended that the standard CMOS practice be followed, ensuring that ground is connected to the device before any other connections are made. In applications where the printed circuit board may be plugged into a "hot" socket with power and clocks already present, an extra long ground pin in the connector is useful.

All ground connections to each device should meet at a common point as close as possible to the GNDA pin.



$$R1 = Z1 \left(\frac{N^2+1}{N^2-1}\right) - 2\sqrt{Z1.Z2}\left(\frac{N}{N^2-1}\right)$$

$$R2 = 2\sqrt{Z1.Z2}\left(\frac{N}{N^2-1}\right)$$

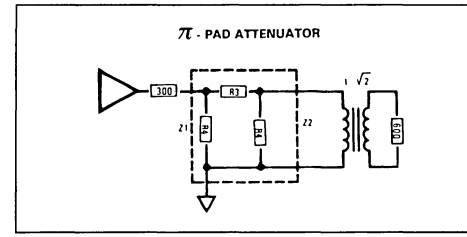
Where : $N = \sqrt{\frac{\text{POWER IN}}{\text{POWER OUT}}}$

and : $S = \sqrt{\frac{Z1}{Z2}}$

Also : $Z = \sqrt{Z_{SC} \cdot Z_{OC}}$

Where Z_{SC} = impedance with short circuit termination

and Z_{OC} = impedance with open circuit termination.



$$R3 = \sqrt{\frac{Z1.Z2}{2}}\left(\frac{N^2-1}{N}\right)$$

$$R3 = Z1\left(\frac{N^2-1}{N^2-2\,NS+1}\right)$$

This minimizes the interaction of ground return currents flowing through a common bus impedance. 0.1 µF supply decoupling capacitors should be connected from this common ground point to V_{CC} and V_{BB}.

For best performance, the ground point of beach/FILTER on a card should be connected to a common card. This common ground point should be decoupled to V_{CC} and V_{BB} with 10 µF capacitors.

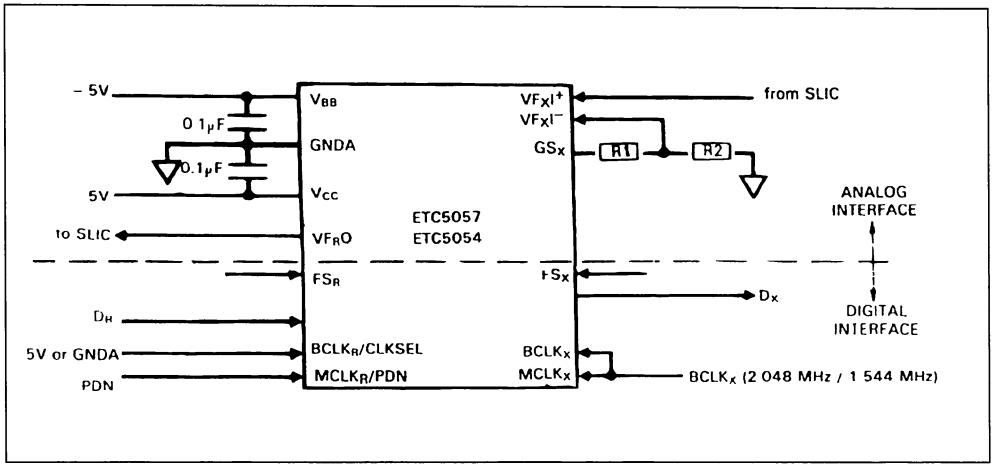
RECEIVE GAIN ADJUSTMENT

For applications where a ETC5050 family CODEC/filter receive output must drive a 600 Ω load, but a peak swing lower then ± 2.5 V is required, the receive gain can be easily a adjusted by inserting a matched T-pad or π-pad at the output. Table II lists the required resistor values for 600 Ω terminations. As these are generally non-standard values, the equations can be used to compute the attenuation of the closest pratical set of resistors. It may be necessary to use unequal values for the R1 or R4 arms of the attenuators to achieve a precise attenuation. Generally it is tolerable to allow a small deviation of the input impedance from nominal while still maintaining a good return loss. For example a 30 dB return loss against 600 Ω is obtained if the output impedance of the attenuator is in the range 282 Ω to 319 Ω (assuming a perfect transformer).

Table 2 : Attenuator Tables for Z1 = Z2 = 300 Ω (all values in Ω).

dB	R1	R2	R3	R4
0.1	1.7	26 k	3.5	52 k
0.2	3.5	13 k	6.9	26 k
0.3	5.2	8.7 k	10.4	17.4 k
0.4	6.9	6.5 k	13.8	13 k
0.5	8.5	5.2 k	17.3	10.5 k
0.6	10.4	4.4 k	21.3	8.7 k
0.7	12.1	3.7 k	24.2	7.5 k
0.8	13.8	3.3 k	27.7	6.5 k
0.9	15.5	2.9 k	31.1	5.8 k
1.0	17.3	2.6 k	34.6	5.2 k
2	34.4	1.3 k	70	2.6 k
3	51.3	850	107	1.8 k
4	68	650	144	1.3 k
5	84	494	183	1.1 k
6	100	402	224	900
7	115	380	269	785
8	129	284	317	698
9	143	244	370	630
10	156	211	427	527
11	168	184	490	535
12	180	161	550	500
13	190	142	635	473
14	200	125	720	450
15	210	110	816	430
16	218	98	924	413
18	233	77	1.17 k	386
20	246	61	1.5 k	366

Figure 5 : Typical Synchronous Application.



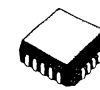
Note : 1. XMIT gain = $20.\log\left(\frac{R1 + R2}{R2}\right)$ (R1 + R2) > 10 kΩ.

SERIAL INTERFACE CODEC/FILTER

- COMPLETE CODEC AND FILTERING SYSTEM (combo) INCLUDING :
  - Transmit high-pass and low-pass filtering.
  - Receive low-pass filter with sin x/x correction.
  - Active RC noise filters.
  - μ-law or A-law compatible COder and DECoder.
  - Internal precision voltage reference.
  - Serial I/O interface.
  - Internal auto-zero circuitry.
- A-LAW 20 PINS ETC5057FN
- μ-LAW WITHOUT SIGNALING, 20 PINS ETC5054FN
- MEETS OR EXCEEDS ALL D3/D4 AND CCITT SPECIFICATIONS
- 5 V OPERATION
- LOW OPERATING POWER - TYPICALLY 60 mW
- POWER-DOWN STANDBY MODE - TYPICALLY 3 mW
- AUTOMATIC POWER-DOWN
- TTL OR CMOS COMPATIBLE DIGITAL INTERFACES
- MAXIMIZES LINE INTERFACE CARD CIRCUIT DENSITY
- SECOND SOURCE OF TP3057FN, TP3054FN

DESCRIPTION

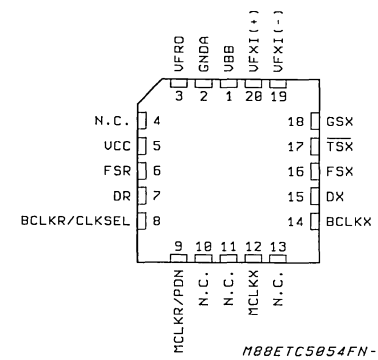
The ETC5057/ETC5054 family consists of A-law and μ–law monolithic PCM CODEC/filters utilizing the A/D and D/A conversion architecture shown in the block diagram below, and a serial PCM interface. The devices are fabricated using double-poly CMOS process. The encode portion of each device consists of an input gain adjust amplifier, an active RC pre-filter which eliminates very high frequency noise prior to entering a switched-capacitor bandpass filter that rejects signals below 200 Hz and above 3400 Hz. Also included are auto-zero circuitry and a companding coder which samples the filtered signal and encodes it in the companded A-law or μ–law PCM format. The decode portion of each device consists of an expanding decoder, which reconstructs the analog signal from the companded A-law or μ–law code, a low-pass filter which corrects for the sin x/x response of the decoder output and rejects signals above 3400 Hz and is followed by a single-ended power amplifier capable of driving low impedance loads. The devices require 1.536 MHz, 1.544 MHz, or 2.048 MHz transmit and receive master clocks, which may be asynchronous, transmit and receive bit clocks which may vary from 64 kHz to 2.048 MHz, and transmit and receive frame sync pulses. The timing of the frame sync pulses and PCM data is compatible with both industry standard formats.



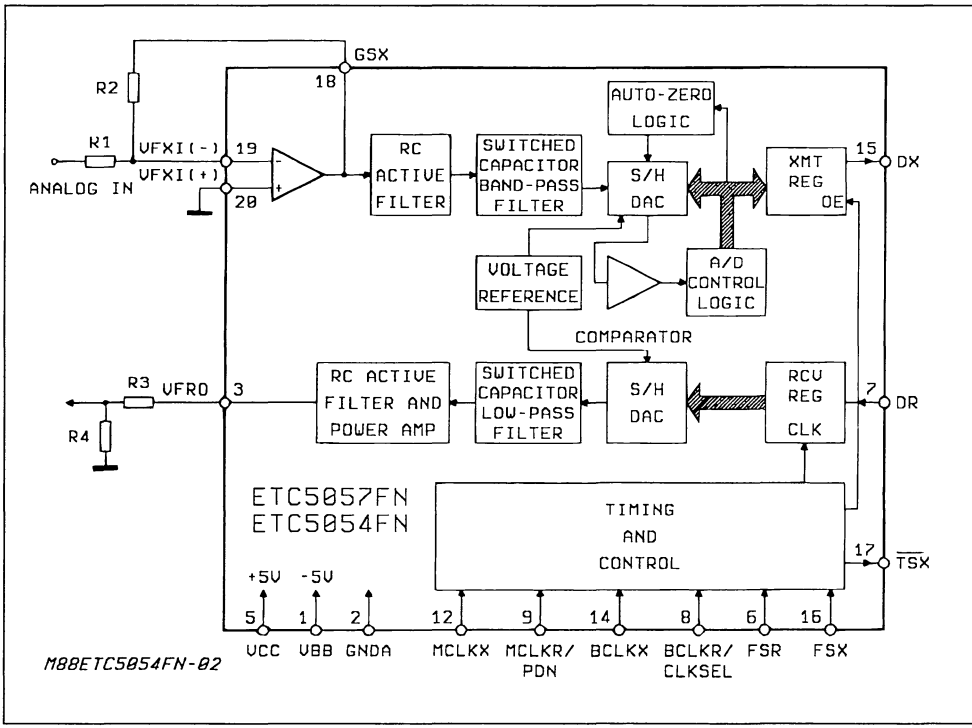
PLCC20

ORDER CODES : ETC5054FN
ETC5057FN

PIN CONNECTIONS



BLOCK DIAGRAM



PIN DESCRIPTION

Name	Pin Type *	N°	Function	Description
V_{BB}	S	1	Negative Power Supply	$V_{BB} = -5\ V \pm 5\ \%$.
GNDA	GND	2	Analog Ground	All signals are referenced to this pin.
VF_RO	O	3	Receive Filter Output	Analog Output of the Receive Filter
V_{CC}	S	5	Positive Power Supply	$V_{CC} = +5\ V \pm 5\ \%$.
FS_R	I	6	Receive Frame Sync Pulse	Enables $BCLK_R$ to shift PCM data into D_R. FS_R is an 8 kHz pulse train. See figures 1, 2 and 3 for timing details.
D_R	I	7	Receive Data Input	PCM data is shifted into D_R following the FS_R leading edge.
$BCLK_R$/CLKSEL	I	8	Shift-in Clock	Shifts data into D_R after the FS_R leading edge. May vary from 64 kHz to 2.048 MHz. Alternatively, may be a logic input which selects either 1.536 MHz/1.544 MHz or 2.048 MHz for master clock in synchronous mode and $BCLK_X$ is used for both transmit and receive directions (see table 1). This input has an internal pull-up.
$MCLK_R$/PDN	I	9	Receive	Must be 1.536 MHz, 1.544 MHz or 2.048 MHz. May be asynchronous with $MCLK_X$, but should be synchronous with $MCLK_X$ for best performance. When $MCLK_R$ is connected continuously low, $MCLK_X$ is selected for all internal timing. When $MCLK_R$ is connected continuously high, the device is powered down.
$MCLK_X$	I	12	Transmit Master Clock	Must be 1.536 MHz, 1.544 MHz or 2.048 MHz. May be asynchronous with $MCLK_R$.
$BCLK_X$	I	14	Shift-out Clock	Shifts out the PCM data on D_X. May vary from 64 kHz to 2.048 MHz, but must be synchronous with $MCLK_X$.
D_X	O	15	Transmit Data Output	The TRI-STATE® PCM data output which is enabled by FS_X.
FS_X	I	16	Transmit Frame Sync Pulse	Enables $BCLK_X$ to shift out the PCM data on D_X. FS_X is an 8 kHz pulse train. See figures 1, 2 and 3 for timing details.
$\overline{TS_X}$	O	17	Transmit Time Slot	Open drain output which pulses low during the encoder time slot. Recommended to be grounded if not used.
GS_X	O	18	Gain Set	Analog output of the transmit input amplifier. Used to set gain externally.
VF_XI^-	I	19	Inverting Amplifier Input	Inverting Input of the Transmit Input Amplifier.
VF_XI^+	I	20	Non-inverting Amplifier Input	Non-inverting Input of the Transmit Input Amplifier.

* I : Input, O : Output, S : Power Supply.

FUNCTIONAL DESCRIPTION

POWER-UP

When power is first applied, power-on reset circuitry initializes the COMBO and places it into the power-down mode. All non-essential circuits are deactivated and the D_X and VF_RO outputs are put in high impedance states. To power-up the device, a logical low level or clock must be applied to the $MCLK_R$/PDN pin and FS_X and/or FS_R pulses must be present. Thus, 2 power-down control modes are available. The first is to pull the $MCLK_R$/PDN pin high ; the alternative is to hold both FS_X and FS_R inputs continuously low. The device will power-down approximately 2 ms after the last FS_X or FS_R pulse. Power-up will occur on the first FS_X or FS_R pulse. The TRI-STATE PCM data output, D_X, will remain in the high impedance state until the second FS_X pulse.

SYNCHRONOUS OPERATION

For synchronous operation, the same master clock and bit clock should be used for both the transmit and receive directions. In this mode, a clock must be applied to $MCLK_X$ and the $MCLK_R$/PDN pin can be used as a power-down control. A low level on $MCLK_R$/PDN powers up the device and a high level powers down the device. In either case, $MCLK_X$ will be selected as the master clock for both the transmit and receive circuits. A bit clock must also be applied to $BCLK_X$ and the $VCLK_R$/CKSEL can be used to select the proper internal divider for a master clock of 1.536 MHz, 1.544 MHz or 2.048 MHz. For 1.544 MHz operation, the device automatically compensates for the 193rd clock pulse each frame. With a fixed level on the $BCLK_R$/CLKSEL pin, $BCLK_X$ will be selected as the bit clock for both the transmit and receive directions. Table 1 indicates the frequencies of operation which can be selected, depending on the state of $BCLK_R$/CLKSEL. In this synchronous mode, the bit clock, $BCLK_X$, may be from 64 kHz to 2.048 MHz, but must be synchronous with $MCLK_X$.

Table 1 : Selection of Master Clock Frequencies.

$BCLK_R$/CLKSEL	Master Clock Frequency Selected	
	ETC5057	ETC5054
Clocked	2.048 MHz	1.536 MHz or 1.544 MHz
0	1.536 MHz or 1.544 MHz	2.048 MHz
1 (or open circuit)	2.048 MHz	1.536 MHz or 1.544 MHz

Each FS_X pulse begins the encoding cycle and the PCM data from the previous encode cycle is shifted out of the enabled D_X output on the positive edge of $BCLK_X$. After 8 bit clock periods, the TRI-STATE D_X output is returned to a high impedance state. With and FS_R pulse, PCM data is latched via the D_R input on the negative edge of $BCLK_X$ (or $BCLK_R$ if running). FS_X and FS_R must be synchronous with $MCLK_{X/R}$.

ASYNCHRONOUS OPERATION

For asynchronous operation, separate transmit and receive clocks may be applied, $MCLK_X$ and $MCLK_R$ must be 2.048 MHz for the ETC5057, or 1.536 MHz, 1.544 MHz for the ETC5054, and need not be synchronous. For best transmission performance, however, $MCLK_R$ should be synchronous with $MCLK_X$, which is easily achieved by applying only static logic levels to the $MCLK_R$/PDN pin. This will automatically connect $MCLK_X$ to all internal $MCLK_R$ functions (see pin description). For 1.544 MHz operation, the device automatically compensates for the 193rd clock pulse each frame. FS_X starts each encoding cycle and must be synchronous with $MCLK_X$ and $BCLK_X$. FS_R starts each decoding cycle and must be synchronous with $BCLK_R$. $BCLK_R$ must be a clock, the logic levels shown in table 1 are not valid in asynchronous mode. $BCLK_X$ and $BCLK_R$ may operate from 64 kHz to 2.048 MHz.

SHORT FRAME SYNC OPERATION

The COMBO can utilize either a short frame sync pulse or a long frame sync pulse. Upon power initialization, the device assumes a short frame mode. In this mode, both frame sync pulses, FS_X and FS_R, must be one bit clock period long, with timing relationships specified in figure 2. With FS_X high during a falling edge of $BCLK_X$ the next rising edge of $BCLK_X$ enables the D_X TRI-STATE output buffer, which will output the sign bit. The following seven rising edges clock out the remaining seven bits, and the next falling edge disables the D_X output. With FS_R high during a falling edge of $BCLK_R$ ($BCLK_X$ in synchronous mode), the next falling edge of $BCLK_R$ latches in the sign bit. The following seven falling edges latch in the seven remaining bits. Both devices may utilize the short frame sync pulse in synchronous or asynchronous operating mode.

LONG FRAME SYNC OPERATION

To use the long frame mode, both the frame sync pulses, FS_X and FS_R, must be three or more bit clock periods long, with timing relationships specified in figure 3. Based on the transmit frame sync, FS_X, the

COMBO will sense whether short or long frame sync pulses are being used. For 64 kHz operation, the frame sync pulse must be kept low for a minimum of 160 ns (see fig. 1). The D_X TRI-STATE output buffer is enabled with the rising edge of FS_X or the rising edge of $BCLK_X$, whichever comes later, and the first bit clocked out is the sign bit. The following seven $BCLK_X$ rising edges clock out the remaining seven bits. The D_X output is disabled by the falling $BCLK_X$ edge following the eighth rising edge, or by FS_X going low, which-ever comes later. A rising edge on the receive frame sync pulse, FS_R, will cause the PCM data at D_R to be latched in on the next eight falling edges of $BCLK_R$ ($BCLK_X$ in synchronous mode).

Both devices may utilize the long frame sync pulse in synchronous or asynchronous mode.

TRANSMIT SECTION

The transmit section input is an operational amplifier with provision for gain adjustment using two external resistors, see figure 6. The low noise and wide bandwidth allow gains in excess of 20 dB across the audio passband to be realized. The op amp drives a unitygain filter consisting of RD active pre-filter, followed by an eighth order switched-capacitor bandpass filter clocked at 256 kHz. The output of this filter directly drives the encoder sample-and-hold circuit. The A/D is of companding type according to A-law (ETC5057) or μ–law (ETC5054) coding conventions. A precision voltage reference is trimmed in manufacturing to provide an input overload (t_{MAX}) of nominally 2.5 V peak (see table of transmission charcteristics). The FS_X frame sync pulse controls the sampling of the filter output, and then the successive-approximation encoding cycle begins. The 8-bit code is then loaded into a buffer and shifted out through D_X at the next FS_X pulse. The total encoding delay will be approximately 165 μs (due to the transmit filter) plus 125μs (due to encoding delay), which totals 290μs. Any offset voltage due to the filters or comparator is cancelled by sign bit integration.

RECEIVER SECTION

The receive section consists of an expanding DAC which drives a fifth order switched-capacitor low pass filter clocked at 256 kHz. The decoder is A-law (ETC5057) or μ–law (ETC5054) and the 5th order low pass filter corrects for the sin x/x attenuation due to the 8 kHz sample and hold. The filter is then followed by a 2nd order RC active post-filter and power amplifier capable of driving a 600Ω load to a level of 7.2 dBm. The receive section is unity-gain. Upon the occurence of FS_R, the data at the D_R input is clocked in on the falling edge of the next eight $BCLK_R$ ($BCLK_X$) periods. At the end of the decoder time slot, the decoding cycle begins, and 10μs later the decoder DAC output is updated. The total decoder delay is ~ 10μs (decoder update) plus 110μs (filter delay) plus 62.5μs (1/2 frame), which gives approximately 180μs.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	V_{CC} to GNDA	7	V
V_{BB}	V_{BB} to GNDA	– 7	V
V_{IN}, V_{OUT}	Voltage at any Analog Input or Output	V_{CC} + 0.3 to V_{BB} – 0.3	V
	Voltage at Any Digital Input or Output	V_{CC} + 0.3 to GNDA – 0.3	V
T_{oper}	Operating Temperature Range	– 25 to + 125	°C
T_{stg}	Storage Temperature Range	– 65 to + 150	°C
	Lead Temperature (soldering, 10 seconds)	300	°C

ELECTRICAL OPERATING CHARACTERISTICS V_{CC} = 5.0 V ± 5 %, V_{BB} = – 5.0 V ± 5% GNDA = 0 V, T_A = 0 °C to 70 °C (unless otherwise noted) ; Typical Characteristics Specified at T_A = 25 °C ; all signals are referenced to GNDA.

Symbol	Parameter		Min.	Typ.	Max.	Unit
V_{IL}	Input Low Voltage				0.6	V
V_{IH}	Input High Voltage		2.2			V
V_{OL}	Output Low Voltage I_L = 3.2 mA I_L = 3.2 mA, Open Drain	D_X $\overline{TS_X}$			0.4 0.4	V
V_{OH}	Output High Voltage I_H = 3.2 mA	D_X	2.4			V
I_{IL}	Input Low Current (GNDA ≤ V_{IN} ≤ all digital inputs)		– 10		10	µA
I_{IH}	Input High Current (V_{IH} ≤ V_{IN} ≤ V_{CC}) Except $BCLK_R$/CLKSEL		– 10		10	µA
I_{OZ}	Output Current in High Impedance State (TRI-STATE) (GNDA ≤ V_O ≤ V_{CC})	D_X	– 10		10	µA

ANALOG INTERFACE WITH TRANSMIT INPUT AMPLIFIER (all devices)

Symbol	Parameter		Min.	Typ.	Max.	Unit
I_IXA	Input Leakage Current (– 2.5 V ≤ V ≤ + 2.5 V)	VF_XI^+ or VF_XI^-	– 200		200	nA
R_IXA	Input Resistance (– 2.5 V ≤ V ≤ + 2.5 V)	VF_XI^+ or VF_XI^-	10			MΩ
R_OXA	Output Resistance (closed loop, unity gain)			1	3	Ω
R_LXA	Load Resistance	GS_X	10			kΩ
C_LXA	Load Capacitance	GS_X			50	pF
V_OXA	Output Dynamic Range (R_L ≥ 10 kΩ)	GS_X	± 2.8			V
A_VXA	Voltage Gain (VF_XI^+ to GS_X)		5000			V/V
F_UXA	Unity Gain Bandwidth		1	2		MHz
$V_{OS}XA$	Offset Voltage		– 20		20	mV
$V_{CM}XA$	Common-mode Voltage		– 2.5		2.5	V
CMRRXA	Common-mode Rejection Ratio		60			dB
PSRRXA	Power Supply Rejection Ratio		60			dB

ANALOG INTERFACE WITH RECEIVE FILTER (all devices)

Symbol	Parameter		Min.	Typ.	Max.	Unit
R_ORF	Output Resistance	VF_RO		1	3	Ω
R_LRF	Load Resistance (VF_RO = ± 2.5 V)		600			Ω
C_LRF	Load Capacitance				500	pF
VOS_RO	Output DC Offset Voltage		– 200		200	mV

POWER DISSIPATION (all devices)

Symbol	Parameter	Min.	Typ.	Max.	Unit
$I_{CC}0$	Power-down Current		0.5	1.5	mA
$I_{BB}0$	Power-down Current		0.05	0.3	mA
$I_{CC}1$	Active Current		6.0	9.0	mA
$I_{BB}1$	Active Current		6.0	9.0	mA

TIMING SPECIFICATIONS All timing parameters are measured at V_{OH} = 2.0 V and V_{OL} = 0.7 V. See "definitions" and "timing convertions" sections for that method information.

Symbol	Parameter	Min.	Typ.	Max.	Unit
$1/t_{PM}$	Frequency of master clocks Depends on the device used and the $BCLK_R$/CLKSEL Pin $MCLK_X$ and $MCLK_R$		1.536 1.544 2.048		MHz
t_{WMH}	Width of Master Clock High $MCLK_X$ and $MCLK_R$	160			ns
t_{WML}	Width of Master Clock Low $MCLK_X$ and $MCLK_R$	160			ns
t_{RM}	Rise Time of Master Clock $MCLK_X$ and $MCLK_R$			50	ns
t_{FM}	Fall Time of Master Clock $MCLK_X$ and $MCLK_R$			50	ns
t_{PB}	Period of Bit Clock	485	488	15.725	ns
t_{WBH}	Width of Bit Clock High (V_{IH} = 2.2 V)	160			ns
t_{WBL}	Width of Bit Clock Low (V_{IL} = 0.6 V)	160			ns
t_{RB}	Rise Time of Bit Clock (t_{PB} = 488 ns)			50	ns
t_{FB}	Fall Time of Bit Clock (t_{PB} = 488 ns)			50	ns
t_{SBFM}	set-up time from $BCLK_X$ high to $MCLK_X$ falling edge. (first bit clock after the leading edge of FS_X)	100			ns
t_{HBF}	Holding Time from Bit Clock Low to the Frame Sync (long frame only)	0			ns
t_{SFB}	Set-up Time from Frame Sync to Bit Clock (long frame only)	80			ns
t_{HBFI}	Hold Time from 3rd Period of Bit Clock Low to Frame Sync (long frame only). FS_X or FS_R	100			ns
t_{DZF}	Delay time to valid data from FS_X or $BCLK_X$, whichever comes later and delay time from FS_X to data output disabled. (C_L = 0 pF to 150 pF)	20		165	ns
t_{DBD}	Delay time from $BCLK_X$ high to data valid. (load = 150 pF plus 2 LSTTL loads)	0		180	ns
t_{DZC}	Delay time from $BCLK_X$ low to data output disabled.	50		165	ns
t_{SDB}	Set-up time from D_R valid to $BCLK_{R/X}$ low.	50			ns
t_{HBD}	Hold time from $BCLK_{R/X}$ low to D_R invalid.	50			ns
t_{HOLD}	Holding Time from Bit Clock High to Frame Sync (short frame only)	0			ns
t_{SF}	Set-up Time from $FS_{X/R}$ to $BCLK_{X/R}$ Low (short frame sync pulse) - Note 1	80			ns
t_{HF}	Hold Time from $BCLK_{X/R}$ Low to $FS_{X/R}$ Low (short frame sync pulse) - Note 1	100			ns
t_{XDP}	Delay Time to TS_Xlow (load = 150 pF plus 2 LSTTL loads)			140	ns
t_{WFL}	Minimum Width of the Frame Sync Pulse (low level) (64 k bit/s operating mode)	160			ns

Note : 1. For short frame sync timing. FS_X and FS_R must go high while their respective bit clocks are high.

Figure 1 : 64 k bits/s TIMING DIAGRAM.

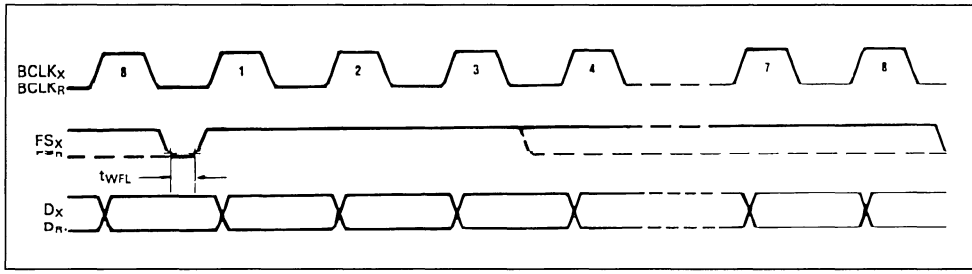


Figure 2 : Short Frame Sync Timing.

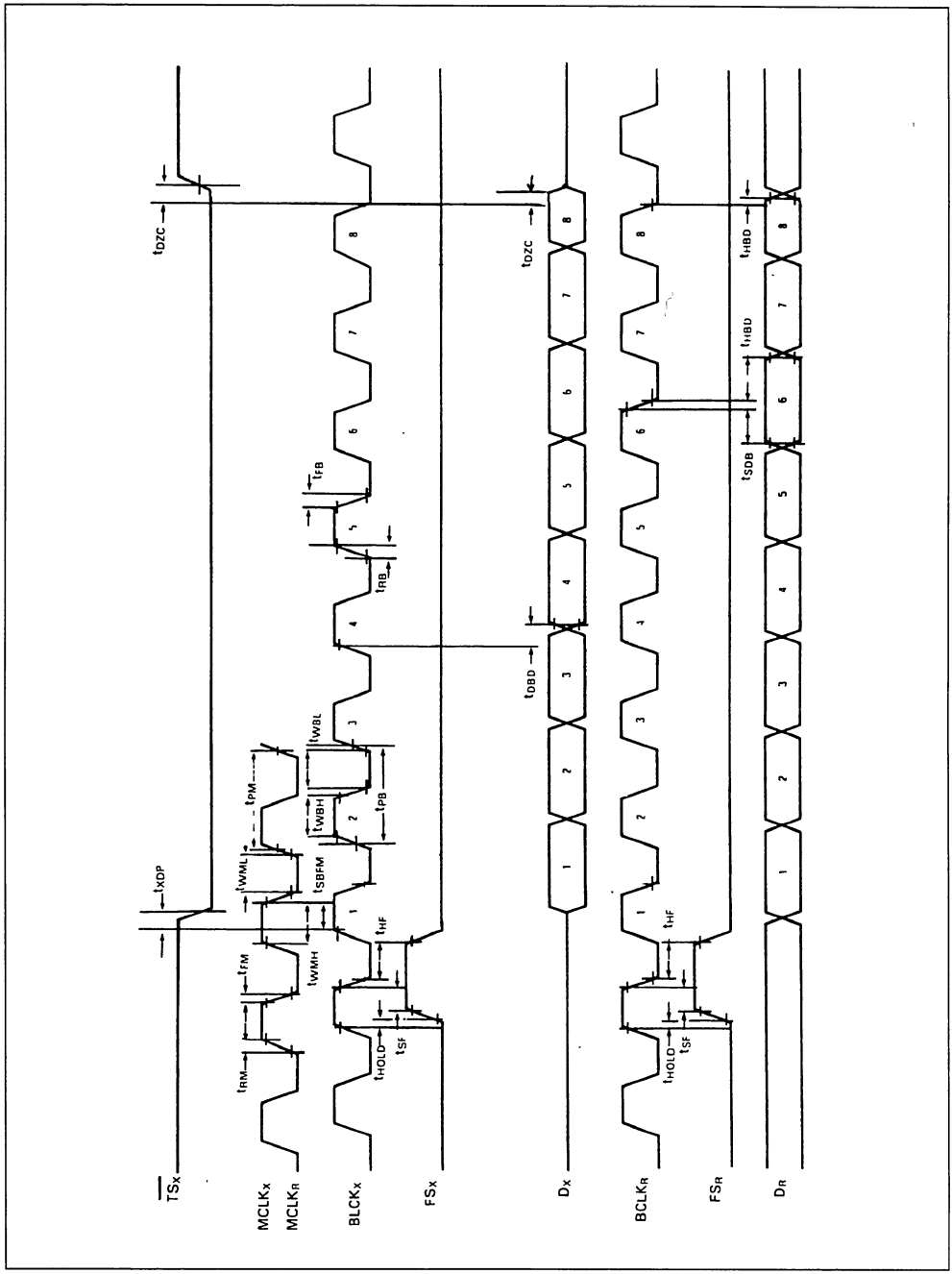
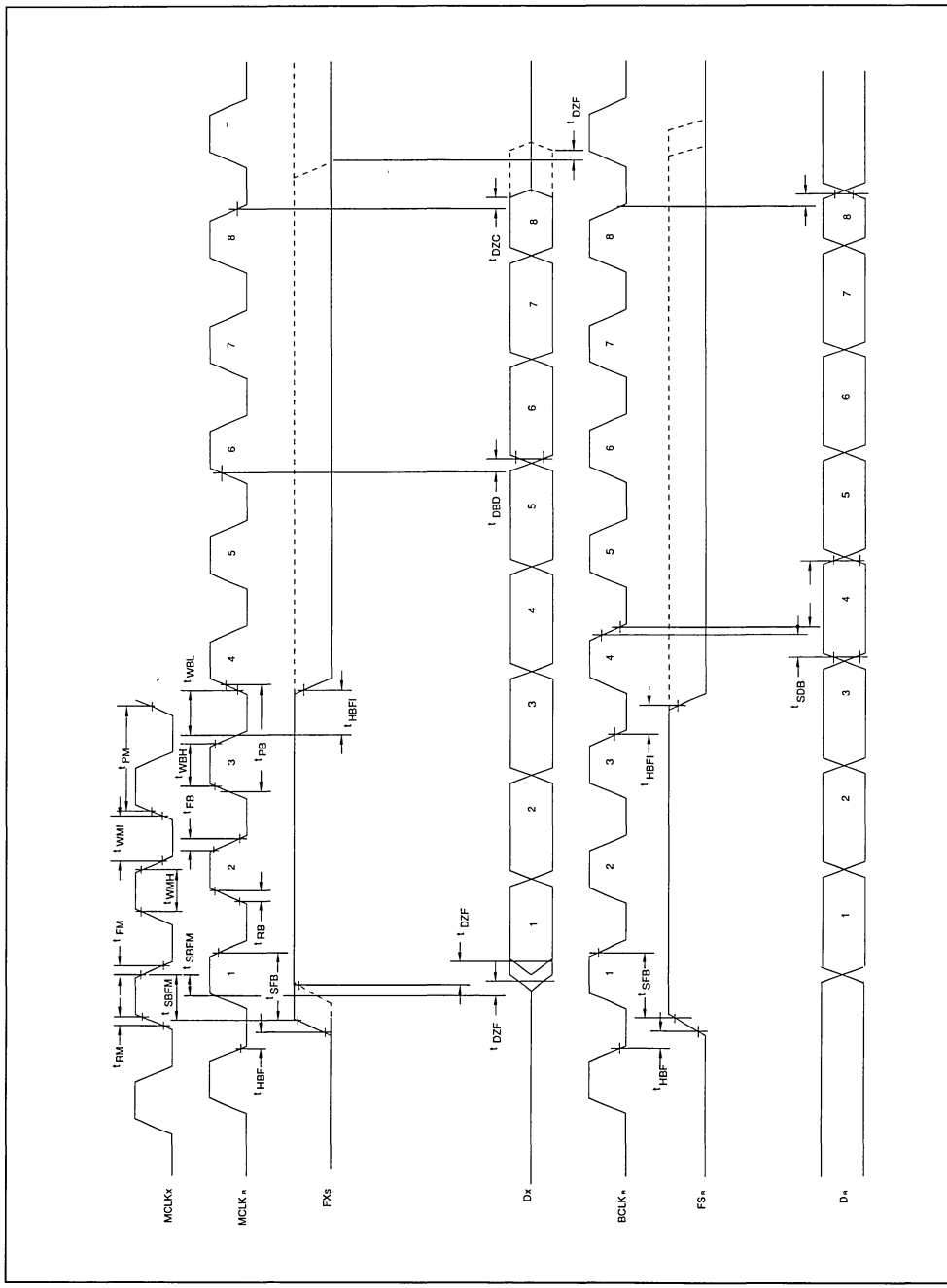


Figure 3 : Long Frame Sync Timing.



TRANSMISSION CHARACTERISTICS (all devices) T_A = 0°C to 70°C, V_{CC} = 5V ± 5%, V_{BB} = – 5V ± 5%, GNDA = 0V, f = 1.02kHz, V_{IN} = 0dBm0 transmit input amplifier connected for unity–gain non–inverting. (unless otherwise specified).

AMPLITUDE RESPONSE

Symbol	Parameter	Min.	Typ.	Max.	Unit
	Absolute levels - nominal 0 dBm0 level is 4 dBm (600 Ω) 0 dBm0		1.2276		Vrms
t_{MAX}	Max Overload Level 3.14 dBm0 (A LAW) 3.17 dBm0 (U LAW)		 2.492 2.501		V_{PK}
G_{XA}	Transmit Gain, Absolute (T_A = 25 °C, V_{CC} = 5 V, V_{BB} = – 5 V) Input at GS_X = 0 dBm0 at 1020 Hz	– 0.15		0.15	dB
G_{XR}	Transmit Gain, Relative to G_{XA} f = 16 Hz f = 50 Hz f = 60 Hz f = 180 Hz f = 200 Hz f = 300 Hz - 3000 Hz f = 3300 Hz f = 3400 Hz ETC 5057, ETC 5054 f = 4000 Hz f = 4600 Hz and up, Measure Reponse from 0 Hz to 4000 Hz	 – 2.8 – 1.8 – 0.15 – 0.35 – 0.7		 – 40 – 30 – 26 – 0.2 – 0.1 0.15 0.05 0 – 14 – 32	dB
G_{XAT}	Absolute Transmit Gain Variation with Temperature (T_A = 0 °C to + 70 °C)	– 0.1		0.1	dB
G_{XAV}	Absolute Transmit Gain Variation with Supply Voltage (V_{CC} = 5 V ± 5 %, V_{BB} = – 5 V ± 5 %)	– 0.05		0.05	dB
G_{XRL}	Transmit Gain Variations with Level Sinusoidal Test Method Reference Level = – 10 dBm0 VF_XI+ = – 40 dBm0 to + 3 dBm0 VF_XI+ = – 50 dBm0 to – 40 dBm0 VF_XI+ = – 55 dBm0 to – 50 dBm0	 – 0.2 – 0.4 – 1.2		 0.2 0.4 1.2	dB
G_{RA}	Receive Gain, Absolute (T_A = 25 °C, V_{CC} = 5 V, V_{BB} = – 5 V) Input = Digital Code Sequence for 0 dBM0 Signal at 1020 Hz	– 0.15		0.15	dB
G_{RR}	Receive Gain, Relative to G_{RA} f = 0 Hz to 3000 Hz f = 3300 Hz f = 3400 Hz f = 4000 Hz	 – 0.15 – 0.35 – 0.7		 0.15 0.05 0 – 14	dB
G_{RAT}	Absolute Receive Gain Variation with Temperature (T_A = 0 °C to + 70 °C)			± 0.1	dB
G_{RAV}	Absolute Receive Gain Variation with Supply Voltage (V_{CC} = 5 V ± 5 %, V_{BB} = – 5 v ± 5 %)			± 0.05	dB
G_{RRL}	Receive Gain Variations with Level Sinusuoidal test method ; reference input PCM code corresponds to an ideally encoded – 10 dBm0 signal PCM Level = – 40 dBm0 to + 3 dBm0 PCM Level = – 50 dBm0 to – 40 dBm0 PCM Level = – 55 dBm0 to – 50 dBm0	 – 0.2 – 0.4 – 1.2		 0.2 0.4 1.2	dB
V_{RO}	Receive Output Drive Level (R_L = 600 Ω)	– 2.5		2.5	V

TRANSMISSION CHARACTERISTICS (continued).

ENVELOPE DELAY DISTORTION WITH FREQUENCY

Symbol	Parameter	Min.	Typ.	Max.	Unit
D_{XA}	Transmit Delay, Absolute (f = 1600 Hz)		290	315	µs
D_{XR}	Transmit Delay, Relative to D_{XA}				µs
	f = 500 Hz-600 Hz		195	220	
	f = 600 Hz-800 Hz		120	145	
	f = 800 Hz-1000 Hz		50	75	
	f = 1000 Hz-1600 Hz		20	40	
	f = 1600 Hz-2600Hz		55	75	
	f = 2600 Hz-2800 Hz		80	105	
	f = 2800 Hz-3000 Hz		130	155	
D_{RA}	Receive Delay, Absolute (f = 1600 Hz)		180	200	µs
D_{RR}	Receive Delay, Relative to D_{RA}				µs
	f = 500 Hz-1000 Hz	− 40	− 25		
	f = 1000 Hz-1600 Hz	− 30	− 20		
	f = 1600 Hz-2600 Hz		70	90	
	f = 2600 Hz-2800 Hz		100	125	
	f = 2800 Hz-3000 Hz		145	175	

NOISE

Symbol	Parameter	Min.	Typ.	Max.	Unit
N_{XP}	Transmit Noise, P Message Weighted (ETC5057, VF_{XI}^+ = 0 V)		− 74	− 69 (note 1)	dBm0p
N_{RP}	Receive Noise, P Message Weighted (ETC5057, PCM code equals positive zero)		− 82	− 79	dBm0p
N_{XC}	Transmit Noise, C Message Weighted (ETC5054, VF_{XI}^+ = 0 V)		12	15	dBrnC0
N_{RC}	Receive Noise, C Message Weighted ETC5054, PCM Code Equals Alternating Positive and Negative Zero		8	11	dBrnC0
N_{RS}	Noise, Single Frequency f = 0 kHz to 100 kHz, Loop around Measurement, VF_{XI}^+ = 0 Vrms			− 53	dBm0
$PPSR_X$	Positive Power Supply Rejection, Transmit (note 2) − 50 dBm0VF_{XI}^+ V_{CC} = 5.0 V_{DC} + 100 mVrms, f = 0 kHz-50 kHz	40			dBp
$NPSR_X$	Negative Power Supply Rejection, Transmit (note 2) − 50 dBm0VF_{XI}^+ V_{BB} = − 5.0 V_{DC} + 100 mVrms, f = 0 kHz-50 kHz	40			dBp
$PPSR_R$	Positive Power Supply Rejection, Receive (PCM code equals positive zero, V_{CC} = 5.0 V_{DC} + 100 mVrms)				
	f = 0 Hz-4000Hz	40			dBp
	f = 4 kHz-25 kHz	40			dB
	f = 25 kHz-50 kHz	36			dB
$NPSR_R$	Negative Power Supply Rejection, Receive (PCM code equals positive zero, V_{BB} = − 5.0 V_{DC} + 100 mVrms)				
	f = 0 Hz-4000Hz	40			dBp
	f = 4 kHz-25 kHz	40			dB
	f = 25 kHz-50 kHz	36			dB

TRANSMISSION CHARACTERISTICS (continued).

NOISE (continued)

Symbol	Parameter	Min.	Typ.	Max.	Unit
SOS	Spurious out-of-band Signals at the Channel Output Loop around measurement, 0 dBm0, 300 Hz-3400 Hz input applied to DR, measure individual image signals at DX				
	4600 Hz-7600 Hz			– 32	dB
	7600 Hz-8400 Hz			– 40	dB
	8400 Hz-100,000 Hz			– 32	dB

DISTORTION

Symbol	Parameter		Min.	Typ.	Max.	Unit
STD_X or STD_R	Signal to Total Distortion (sinusoidal test method)					
	Transmit or Receive Half-channel					
	Level = 3.0 dBm0		33			
	= 0 dBm0 to – 30 dBm0		36			dBp
	= – 40 dBm0	XMT	29			
		RCV	30			
	= – 55 dBm0	XMT	14			
		RCV	15			
SFD_X	Single Frequency Distortion, transmit				– 46	dB
SFD_R	Single Frequency Distortion, receive				– 46	dB
IMD	Intermodulation Distortion Loop Around Measurement, VF_XI^+ = – 4 dBm0 to – 21 dBm0, two Frequencies in the Range 300 Hz-3400 Hz				– 41	dB

CROSSTALK

Symbol	Parameter	Min.	Typ.	Max.	Unit
CT_{X-R}	Transmit to Receive Crosstalk, 0dBm0 Transmit Level f = 300 Hz-3400 Hz, D_R = Steady PCM Code		– 90	– 75	dB
CT_{R-X}	Receive to Transmit Crosstalk, 0dBm0 Receive Level f = 300 Hz-3400 Hz, VF_XI = 0 V		– 90	– 70 (note 2)	dB

Notes : 1 Measured by extrapolation from the distortion test results.
2 PPSRX, NPSRX, CTR–X are measured with a –50dBm0 activating signal applied at VF_XI+

ENCODING FORMAT AT D_X OUTPUT

	A-Law (including even bit inversion)	μLaw
V_{IN} (at GS_X) = + Full-scale	1 0 1 0 1 0 1 0	1 0 0 0 0 0 0 0
V_{IN} (at GS_X) = 0 V	1 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1	1 1 1 1 1 1 1 1 0 1 1 1 1 1 1 1
V_{IN} (at GS_X) = – Full-scale	0 0 1 0 1 0 1 0	0 0 0 0 0 0 0 0

APPLICATION INFORMATION

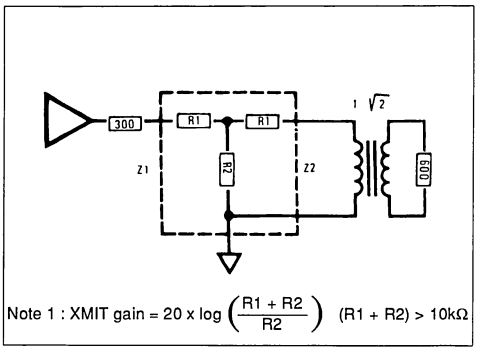
POWER SUPPLIES

While the pins at the ETC5050 family are well protected against electrical misuse, it is recommended that the standard CMOS practice be followed, ensuring that ground is connected to the device before any-other connections are made. In applications where the printed circuit board may be plugged into a "hot" socket with power and clocks already present, an extra long ground pin in the connector should be used.

All ground connections to each device should meet at a common point as close as possible to the GNDA pin. This minimizes the interaction of ground return currents flowing through a common bus impedance. 0.1 F supply decoupling capacitors should be connected from this common ground point to V_{CC} and V_{BB} as close to the device as possible.

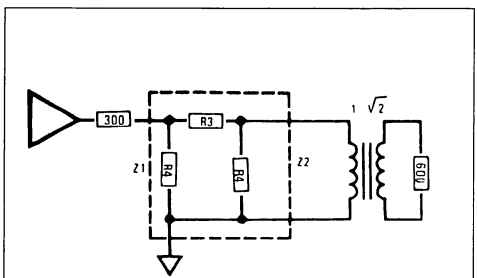
For best performance, the ground point of each CODEC/FILTER on a card should be connected to a common card ground in star formation, rather than via a ground bus. This common ground point should be decoupled to V_{CC} and V_{BB} with 10µF capacitors.

Figure 4 : T–PAD Attenuator.



Note 1 : XMIT gain = $20 \times \log \left(\frac{R1 + R2}{R2}\right)$ (R1 + R2) > 10kΩ

Figure 5 : π–PAD Attenuator.



Note 1 : XMIT gain = $20 \times \log \left(\frac{R1 + R2}{R2}\right)$ (R1 + R2) > 10kΩ

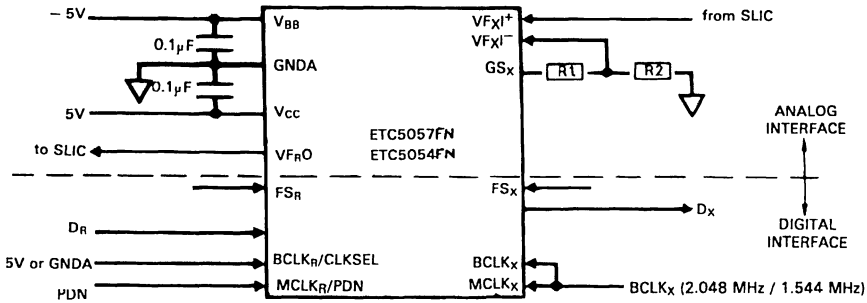
RECEIVE GAIN ADJUSTMENT

For applications where a ETC5050 family CODEC/filter receive output must drive a 600Ω load, but a peak swing lower then ± 2.5V is required, the receive gain can be easily adjusted by inserting a matched T-pad or π–pad at the output. Table II lists the required resistor values for 600Ω terminations. As these are generally non-standard values, the equations can be used to compute the attenuation of the closest pratical set of resistors. It may be necessary to use unequal values for the R1 or R4 arms of the attenuators to achieve a precise attenuation. Generally it is tolerable to allow a small deviation of the input impedance from nominal while still maintaining a good return loss. For example a 30dB return loss against 600Ω is obtained if the output impedance of the attenuator is in the range 282Ω to 319Ω (assuming a perfect transformer).

Table 2 : Attenuator Tables For Z1 = Z2 = 300 Ω (all values in Ω).

dB	R1	R2	R3	R4
0.1	1.7	26k	3.5	52k
0.2	3.5	13k	6.9	26k
0.3	5.2	8.7k	10.4	17.4k
0.4	6.9	6.5k	13.8	13k
0.5	8.5	5.2k	17.3	10.5k
0.6	10.4	4.4k	21.3	8.7k
0.7	12.1	3.7k	24.2	7.5k
0.8	13.8	3.3k	27.7	6.5k
0.9	15.5	2.9k	31.1	5.8k
1.0	17.3	2.6k	34.6	5.2k
2	34.4	1.3k	70	2.6k
3	51.3	850	107	1.8k
4	68	650	144	1.3k
5	84	494	183	1.1k
6	100	402	224	900
7	115	380	269	785
8	129	284	317	698
9	143	244	370	630
10	156	211	427	527
11	168	184	490	535
12	180	161	550	500
13	190	142	635	473
14	200	125	720	450
15	210	110	816	430
16	218	98	924	413
18	233	77	1.17k	386
20	246	61	1.5k	366

Figure 6 : Typical Synchronous Application.



Note 1 : XMIT gain = $20 \times \log\left(\frac{R1 + R2}{R2}\right)$ $(R1 + R2) > 10k\Omega$

SGS-THOMSON MICROELECTRONICS

ETC5057-X
ETC5054-X

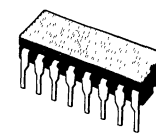
EXTENDED TEMPERATURE RANGE SERIAL INTERFACE CODEC/FILTER

- – 40 °C TO + 85 °C OPERATION
- COMPLETE CODEC AND FILTERING SYSTEM (COMBO) INCLUDING :
  - Transmit high-pass and low-pass filtering
  - Receive low-pass filter with sin x/x correction
  - Active RC noise filters
  - A-law or μ-law compatible COder and DECoder
  - Internal precision voltage reference
  - Serial I/O interface
  - Internal auto-zero circuitry
- A-LAW, 16-PINS - ETC5057
- μ-LAW WITHOUT SIGNALING, 16-PINS - ETC5054
- MEETS OR EXCEEDS ALL D3/D4 AND CCITT SPECIFICATIONS
- ± 5 V OPERATION
- LOW OPERATING POWER - TYPICALLY 60 mW
- POWER-DOWN STANDBY - TYPICALLY 3 mW
- AUTOMATIC POWER-DOWN
- TTL OR CMOS COMPATIBLE DIGITAL INTERFACES
- MAXIMIZES LINE INTERFACE CARD CIRCUIT DENSITY
- SECOND SOURCE OF TP3057, TP3054

DESCRIPTION

The ETC5057/ETC5054 family consists of A-law and μ-law monolithic PCM CODEC/filters utilizing the A/D and D/A conversion architecture shown in figure 1, and a serial PCM interface. The devices are fabricated using double-poly CMOS process.

The encode portion of each device consists of an input gain adjust amplifier, an active RC pre-filter which eliminates very high frequency noise prior to entering a switched-capacitor band-pass filter that rejects signals below 200 Hz and above 3400 Hz. Also included are auto-zero circuitry and a companding coder which samples the filtered signal and encodes it in the companded A-law or μ-law PCM format. The decode portion of each device consists of an expanding decoder, which reconstructs the analog signal from the companded A-law or μ-law code, a low-pass filter which corrects for the sin x/x response of the decoder output and rejects signals above 3400 Hz and is followed by a single-ended power amplifier capable of driving low impedance loads. The devices require 1.536 MHz, 1.544 MHz, or 2.048 MHz transmit and receive master clocks, which may be asynchronous, transmit and receive bit clocks which may vary from 64 kHz to 2.048 MHz, and transmit and receive frame sync pulses. The timing of the frame sync pulses and PCM data is compatible with both industry standard formats.



DIP16
(Ceramic)

ORDER CODES : ETC5057J-X
ETC5054J-X

PIN CONNECTION

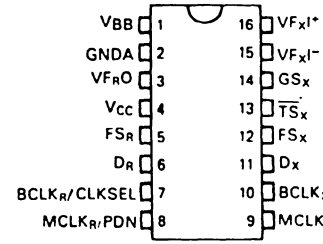
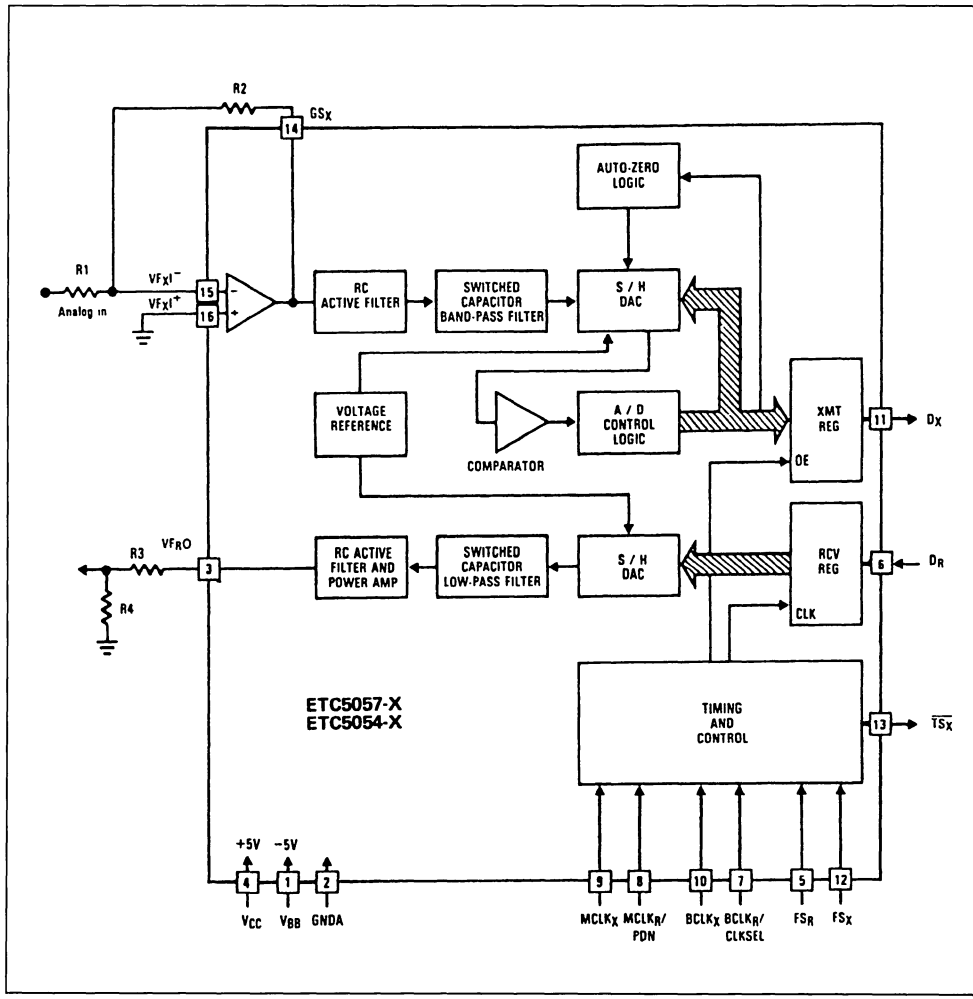


Figure 1 : Block Diagram.



PIN DESCRIPTION

Name	Pin Type*	N°	Function	Description
V_{BB}	S	1	Negative Power Supply	$V_{BB} = -5 \pm 5\ \%$
GNDA	GND	2	Analog Ground	All signals are referenced to this pin.
VF_RO	O	3	Receiver Filter Output	Analog Output of the Receive Filter
V_{CC}	S	4	Positive Power Supply	$V_{CC} = +5 \pm 5\ \%$
FS_R	I	5	Receive Frame Sync Pulse	Enable $BCLK_R$ to shift PCM data into D_R. FS_R is an 8 kHz pulse train. See figures 2,3 and 4 for timing details.
D_R	I	6	Receive Data Input	PCM data is shifted into D_R following the FS_R leading edge.
$BCLK_R$/CLKSEL	I	7	Shift-in Clock	Shifts data into DR after the FS_R leading edge. May vary from 64 kHz to 2.048 MHz. Alternatively, may be a logic input which selects either 1.536 MHz/1.544 MHz or 2.048 MHz for master clock in synchronous mode and $BCLK_X$ is used for both transmit and receive directions (see table 1). This input has an internal pull-up.
$MCLK_R$/PDN	I	8	Receive Master Clock	Must be 1.536 MHz, 1.544 MHz or 2.048 MHz. May be asynchronous with $MCLK_X$, but should be synchronous with $MCLK_X$ for best performance. When $MCLK_R$ is connected continuously low, $MCLK_X$ is selected for all internal timing when MCLKR is connected continuously high, the device is powered down.
$MCLK_X$	I	9	Transmit Master Clock	Must be 1.536 MHz, 1.544 MHz or 2.048 MHz. May be asynchronous with $MCLK_R$.
FS_X	I	12	Transmit Frame Sync Pulse	Enables $BCLK_X$ to shift out the PCM data on D_X. FS_X is an 8 kHz pulse train. See figures 2, 3 and 4 for timing details.
$BCLK_X$	I	10	Shift out Clock	Shifts out the PCM data on D_X. May vary from 64 kHz to 2.048 MHz, but must be synchronous with $MCLK_X$.
D_X	O	11	Transmit Data Output	The TRI-STATE® PCM data output which is enabled by FS_X.
$\overline{TS_X}$	O	13	Transmit Time Slot	Open drain output which pulses low during the encoder time slot. Must be grounded if not used.
GS_X	O	14	Gain Set	Analog output of the transmit input amplifier. Used to set gain externally.
VF_XI^-	I	15	Inverting Amplifier Input	Inverting input of the transmit input amplifier.
VF_XI^+	I	16	Non-inverting Amplifier Input	Non-inverting input of the transmit input amplifier.

* I : Input, o : Output, S : Power Supply.
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FUNCTIONAL DESCRIPTION

POWER-UP

When power is first applied, power-on reset circuitry initializes the COMBO and places it into the power-down mode. All non-essential circuits are deactivated and the D_X and VF_RO outputs are put in high impedance states. To power-up the device, a logical low level or clock must be applied to the $MCLK_R$/PDN pin and FS_X and/or FS_R pulses must be present. Thus, 2 power-down control modes are available. The first is to pull the $MCLK_R$/PDN pin high ; the alternative is to hold both FS_X and FS_R inputs continuously low. The device will power-down approximately 2 ms after the last FS_X or FS_R pulse. Power-up will occur on the first FS_X of FS_R pulse. The TRI-STATE PCM data output, D_X, will remain in the high impedance state until the second FS_X pulse.

SYNCHRONOUS OPERATION

For synchronous operation, the same master clock and bit clock should be used for both the transmit and receive directions. In this mode, a clock must be applied to $MCLK_X$ and the MCLKR/PDN pin can be used as a power-down control. A low level on $MCLK_R$/PDN powers up the device and a high level powers down the device. In either case, $MCLK_X$ will be selected as the master clock for both the transmit and receive circuits. A bit clock must also be applied to $BCLK_X$ and the $BCLK_R$/CLKSEL can be used to select the proper internal divider for a master clock of 1.536 MHz, 1.544 MHz or 2.048 MHz. For 1.544 MHz operation, the device automatically compensates for the 193 rd clock pulse each frame.

With a fixed level on the $BCLK_R$/CLKSEL pin, $BCLK_X$ will be selected as the bit clock for both the transmit and receive directions. Table 1 indicates the frequencies of operation which can be selected, depending on the state of $BCLK_R$/CLKSEL. In this synchronous mode, the bit clock, $BCLK_X$, may be from 64 kHz to 2.048 MHz, but must be synchronous with $MCLK_X$.

Table 1. Selection of Master Clock Frequencies.

$BCLK_R$/CLKSEL	Master Clock Frequency Selected	
	ETC 5057	ETC 5054
Clocked	2.048 MHz	1.536 MHz or 1.544 MHz
0	1.536 MHz or 1.544 MHz	2.048 MHz
1 (or open circuit)	2.048 MHz	1.536 MHz or 1.544 MHz

Each FS_X pulse begins the encoding cycle and the PCM data from the previous encode cycle is shifted out of the enabled D_X output on the positive edge of $BCLK_X$. After 8 bit clock periods, the TRI-STATE D_X output is returned to a high impedance state. With an FS_R pulse, PCM data is latched via the D_R input on the negative edge of $BCLK_X$ (or $BCLK_R$ if running). FS_X and FS_R must be synchronous with $MCLK_{X/R}$.

ASYNCHRONOUS OPERATION

For asynchronous operation, separate transmit and receive clocks may be applied. $MCLK_X$ and $MCLK_R$ must be 2.048 MHz for the ETC5057, or 1.536 MHz, 1.544 MHz for the ETC5054, and need not be synchronous. For best transmission performance, however, $MCLK_R$ should be synchronous with $MCLK_X$, which is easily achieved by applying only static logic levels to the $MCLK_R$/PDN pin. This will automatically connect $MCLK_X$ to all internal $MCLK_R$ functions (see Pin Description). For 1.544 MHz operation, the device automatically compensates for the 193 rd clock pulse each frame. FS_X starts each encoding cycle and must be synchronous with $MCLK_X$ and $BCLK_X$. FS_R starts each decoding cycle and must be synchronous with $BCLK_R$. $BCLK_R$ must be a clock, the logic levels shown in Table 1 are not valid in asynchronous mode. $BCLK_X$ and $BCLK_R$ may operate from 64 kHz to 2.048 MHz.

SHORT FRAME SYNC OPERATION

The COMBO can utilize either a short frame sync pulse or a long frame sync pulse. Upon power initialization, the device assumes a short frame mode. In this mode, both frame sync pulses, FS_X and FS_R, must be one bit clock period long, with timing relationships specified in figure 3. With FS_X high during a falling edge of $BCLK_X$, the next rising edge of $BCLK_X$ enables the D_X TRI-STATE output buffer, which will output the sign bit. The following seven rising edges clock out the remaining seven bits, and the next falling edge disables the D_X output. With FS_R high during a falling edge of $BCLK_R$ ($BCLK_X$ in synchronous mode), the next falling edge of $BCLK_R$ latches in the sign bit. The following seven falling edges latch in the seven remaining bits. Both devices may utilize the short frame sync pulse in synchronous or asynchronous operating mode.

LONG FRAME SYNC OPERATION

To use the long frame mode, both the frame sync pulses, FS_X and FS_R, must be three or more bit clock periods long, with timing relationships specified in figure 4. Based on the transmit frame sync. FS_X, the

COMBO will sense whether short or long frame sync pulses are being used. For 64 kHz operation, the frame sync pulse must be kept low for a minimum of 160 ns (See Fig. 2). The D_X TRI-STATE output buffer is enabled with the rising edge of FS_X or the rising edge of $BCLK_X$, whichever comes later, and the first bit clocked out is the sign bit. The following seven $BCLK_X$ rising edges clock out the remaining seven bits. The D_X output is disabled by the falling $BCLK_X$ edge following the eighth rising edge, or by FS_X going low, whichever comes later. A rising edge on the receive frame sync pulse, FS_R, will cause the PCM data at D_R to be latched in on the next eight falling edges of $BCLK_R$ ($BCLK_X$ in synchronous mode).

Both devices may utilize the long frame sync pulse in synchronous or asynchronous mode.

TRANSMIT SECTION

The transmit section input is an operational amplifier with provision for gain adjustment using two external resistors, see figure 5. The low noise and wide band-width allow gains in excess of 20 dB across the audio passband to be realized. The op amp drives a unity-gain filter consisting of RC active prefilter, followed by an eighth order switched-capacitor bandpass filter clocked at 256 kHz. The output of this filter directly drives the encoder sample-and-hold circuit. The A/D is of companding type according to A-law (ETC5057) or μ-law (ETC5054) coding conventions. A precision voltage reference is trimmed in manufacturing to provide an input overload (t_{MAX}) of nominally 2.5 V peak (see table of Transmission Characteristics). The FS_X frame sync pulse controls the sampling of the filter output, and then the successive-approximation encoding cycle begins. The 8-bit code is then loaded into a buffer and shifted out through D_X at the next FS_X pulse. The total encoding delay will be approximately 165 μs (due to the transmit filter) plus 125 μs (due to encoding delay), which totals 290 μs. Any offset voltage due to the filters or comparator is cancelled by sign bit integration.

RECEIVE SECTION

The receive section consists of an expanding DAC which drives a fifth order switched-capacitor low pass filter clocked at 256 kHz. The decoder is A-law (ETC5057) or μ-law (ETC5054) and the 5th order low pass filter corrects for the sin x/x attenuation due to the 8 kHz sample and hold. The filter is then followed by a 2 nd order RC active post-filter and power amplifier capable of driving a 600 Ω load to a level of 7.2 dBm. The receive section is unity-gain. Upon the occurence of FS_R, the data at the D_R input is clocked in on the falling edge of the next eight $BCLK_R$ ($BCLK_X$) periods. At the end of the decoder time slot, the decoding cycle begins, and 10 μs later the decoder DAC output is updated. The total decoder delay is ~ 10 μs (decoder update) plus 110 μs (filter delay) plus 62.5 μs (1/2 frame), which gives approximately 180 μs.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	V_{CC} to GNDA	7	V
V_{BB}	V_{BB} to GNDA	– 7	V
V_{IN}, V_{OUT}	Voltage at Any Analog Input or Output	V_{CC} + 0.3 to V_{BB} – 0.3	V
	Voltage at Any Digital Input or Output	V_{CC} + 0.3 to GNDA – 0.3	V
T_{oper}	Operating Temperature Range	– 40 to + 125	°C
T_{stg}	Storage Temeperature Range	– 55 to + 150	°C
	Lead Temperature (soldering, 10 seconds)	300	°C

ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0 V ± 5 %, V_{BB} = – 5 V ± 5 %, GNDA = 0 V, T_A = – 40 °C to 85 °C (unless otherwise noted) ; Typical characteristics specified at V_{CC} = 5.0 V, V_{BB} = – 5.0 V, T_A = 25 °C ; all signals are referenced to GNDA.

DIGITAL INTERFACE

Symbol	Parameter		Min.	Typ.	Max.	Unit
V_{IL}	Input Low Voltage		–	–	0.6	V
V_{IH}	Input High Voltage		2.2	–	–	V
V_{OL}	Output Low Voltage					V
	I_L = 3.2 mA	D_X	–	–	0.4	
	I_L = 3.2 mA, Open Drain	$\overline{TS_X}$	–	–	0.4	
V_{OH}	Output High Voltage					V
	I_H = – 3.2 mA	D_X	2.4	–	–	
I_{IL}	Input Low Current (GNDA ≤ V_{IN} ≤ V_{IL}, all digital inputs)		– 10	–	10	µA
I_{IH}	Input High Current (V_{IH} ≤ V_{IN} ≤ V_{CC}) except $BCLK_R$/CLKSEL		– 10	–	10	µA
I_{OZ}	Output Current in High Impedance State (TRI–STATE)					µA
	(GNDA ≤ V_0 ≤ V_{CC})	D_X	– 10	–	10	

ANALOG INTERFACE WITH TRANSMIT INPUT AMPLIFIER (all devices)

Symbol	Parameter		Min.	Typ.	Max.	Unit
I_IXA	Input Leakage Current (– 2.5 V ≤ V ≤ + 2.5 V)	VF_XI^+ or VF_XI^-	– 200	–	200	nA
R_IXA	Input Resistance (– 2.5 ≤ V ≤ + 2.5 V)	VF_XI^+ or VF_XI^-	10	–	–	MΩ
R_OXA	Output Resistance (closed loop, unity gain)		–	1	3	Ω
R_LXA	Load Resistance	GS_X	10	–	–	kΩ
C_LXA	Load Capacitance	GS_X	–	–	50	pF
V_OXA	Output Dynamic Range (R_L ≥ 10 kΩ)	GS_X	± 2.8	–	–	V
A_VXA	Voltage Gain (VF_XI^+ to GS_X)		5000	–	–	V/V
F_UXA	Unity Gain Bandwidth		1	2	–	MHz
$V_{OS}XA$	Offset Voltage		– 20	–	20	mV
$V_{CM}XA$	Common-mode Voltage		– 2.5	–	2.5	V
CMRRXA	Common-mode Rejection Ratio		60	–	–	dB
PSRRXA	Power Supply Rejection Ratio		60	–	–	dB

ANALOG INTERFACE WITH RECEIVE FILTER (all devices)

Symbol	Parameter		Min.	Typ.	Max.	Unit
R_ORF	Output Resistance	VF_RO	–	1	3	Ω
R_LRF	Load Resistance (VF_RO = ± 2.5 V)		600	–	–	Ω
C_LRF	Load Capacitance		–	–	500	pF
VOS_RO	Output DC Offset Voltage		– 200	–	200	mV

ELECTRICAL CHARACTERISTICS (continued)

POWER DISSIPATION (all devices)

Symbol	Parameter	Min.	Typ.	Max.	Unit
$I_{CC}0$	Power-down Current	–	0.5	–	mA
$I_{BB}0$	Power-down Current	–	0.05	0.4	mA
$I_{CC}1$	Active Current	–	6.0	11.0	mA
$I_{BB}1$	Active Current	–	6.0	11.0	mA

TIMING SPECIFICATIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
$1/t_{PM}$	Frequency of Master Clocks Depends on the device used and the $BCLK_R$/CLKSEL pin. $MCLK_X$ and $MCLK_R$	– – –	1.536 1.544 2.048	– – –	MHz
t_{WMH}	Width of Master Clock High $MCLK_X$ and $MCLK_R$	160	–	–	ns
t_{WML}	Width of Master Clock Low $MCLK_X$ and $MCLK_R$	160	–	–	ns
t_{RM}	Rise Time of Master Clock $MCLK_X$ and $MCLK_R$	–	–	50	ns
t_{FM}	Fall Time of Master Clock $MCLK_X$ and $MCLK_R$	–	–	50	ns
t_{PB}	Period of Bit Clock	485	488	15, 725	ns
t_{WBH}	Width of Bit Clock High (V_{IH} = 2.2 V)	160	–	–	ns
t_{WBL}	Width of Bit Clock Low (V_{IL} = 0.6 V)	160	–	–	ns
t_{RB}	Rise Time of Bit Clock (t_{PB} = 488 ns)	–	–	50	ns
t_{FB}	Fall Time of Bit Clock (t_{PB} = 488 ns)	–	–	50	ns
t_{SBFM}	Set-up Time from $BCLK_X$ High to $MCKL_X$ Falling Edge (first bit clock after the leading edge of FS_X)	100	–	–	ns
t_{HBF}	Holding Time from Bit Clock Low to the Frame Sync (long frame only)	0	–	–	ns
t_{SFB}	Set-up Time from Frame Sync to Bit Clock Low (long frame only)	80	–	–	ns
t_{HBFI}	Hold Time from 3rd Period of Bit Clock Low to Frame Sync (long frame only) FS_X or FS_R	100	–	–	ns
t_{DZF}	Delay time to valid data from FS_X or $BCLK_X$, whichever comes later and delay time from FS_X to data output disabled. (C_L = 0 pF to 150 pF)	20	–	165	ns
t_{DBD}	Delay Time from $BCLK_X$ High to Data Valid (Load = 150 pF plus 2 LSTTL loads)	0	–	180	ns
t_{DZC}	Delay Time from $BCLK_X$ Low to Data Output Disabled	50	–	165	ns
t_{SDB}	Set-up Time from D_R Valid to $BCLK_{R/X}$ Low	50	–	–	ns
t_{HBD}	Hold Time from $BCLK_{R/X}$ Low to D_R Invalid	50	–	–	ns
t_{HOLD}	Holding Time from Bit Clock High to Frame Sync (short frame only)	0	–	–	ns

Note : For short frame sync timing FSX and FSR must go high while their respective bit clocks are high.

TIMING SPECIFICATIONS (continued)

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{SF}	Set-up Time from $FS_{X/R}$ to $BCLK_{X/R}$ Low (short frame sync pulse) - Note 1	80	–	–	ns
t_{HF}	Hold Time from $BCLK_{X/R}$ Low to $FS_{X/R}$ Low (short frame sync pulse) - Note 1	100	–	–	ns
t_{XDP}	Delay Time TS_X Low (load = 150 pF plus 2 LSTTL loads)	–	–	140	ns
t_{WFL}	Minimum Width of the Frame Sync Pulse (low level) (64 k bit/s operating mode)	160	–	–	ns

Note : 1. For short frame sync timing F_{SX} and F_{SR} must go high while their respective bit clocks are high.

Figure 2 : 64 k bits/s TIMING DIAGRAM (see next page for complete timing).

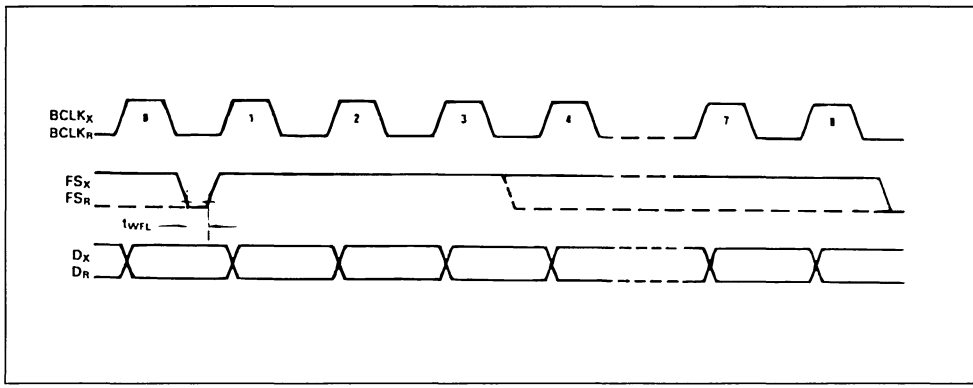


Figure 3 : Short Frame Sync Timing.

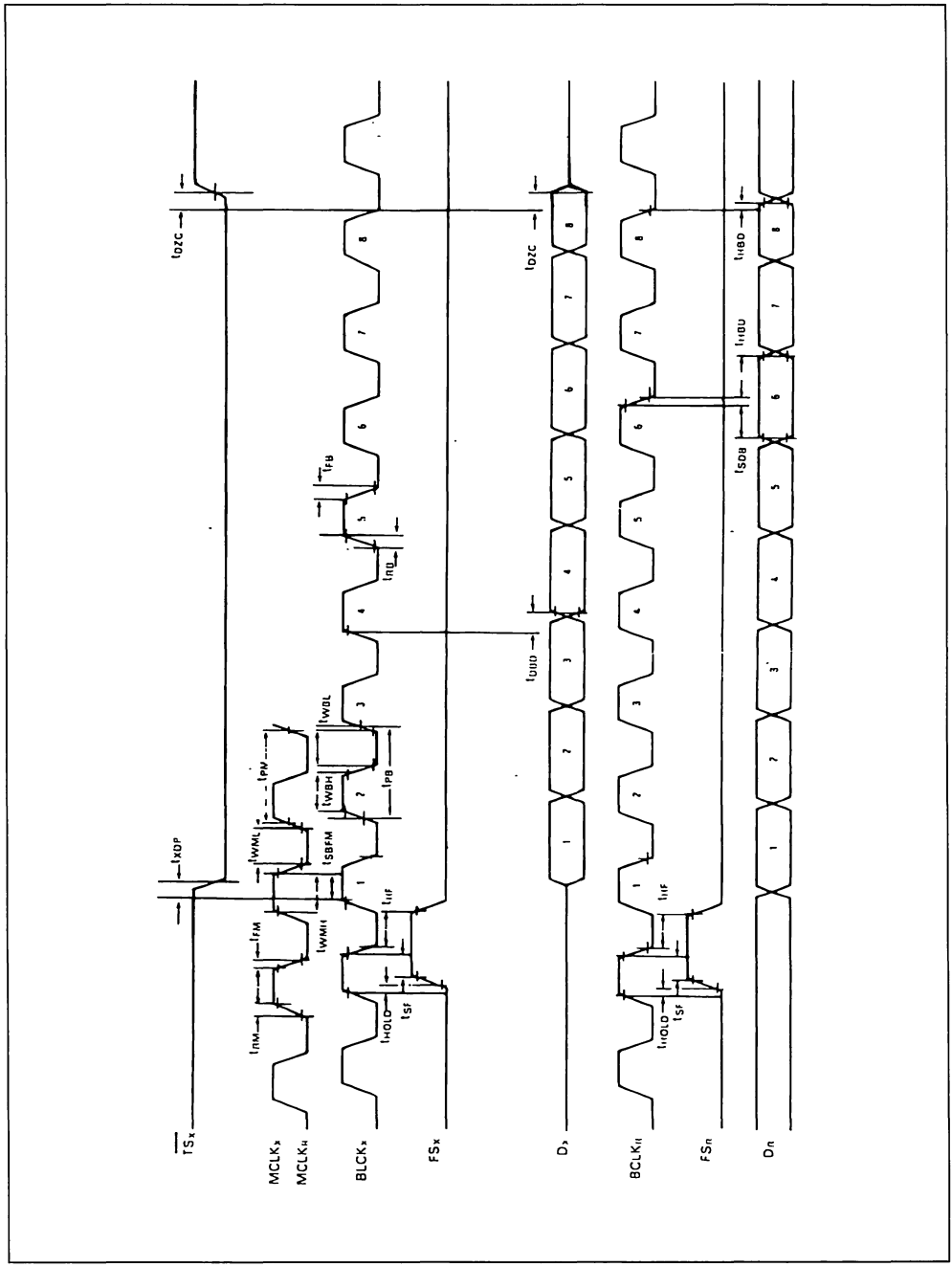
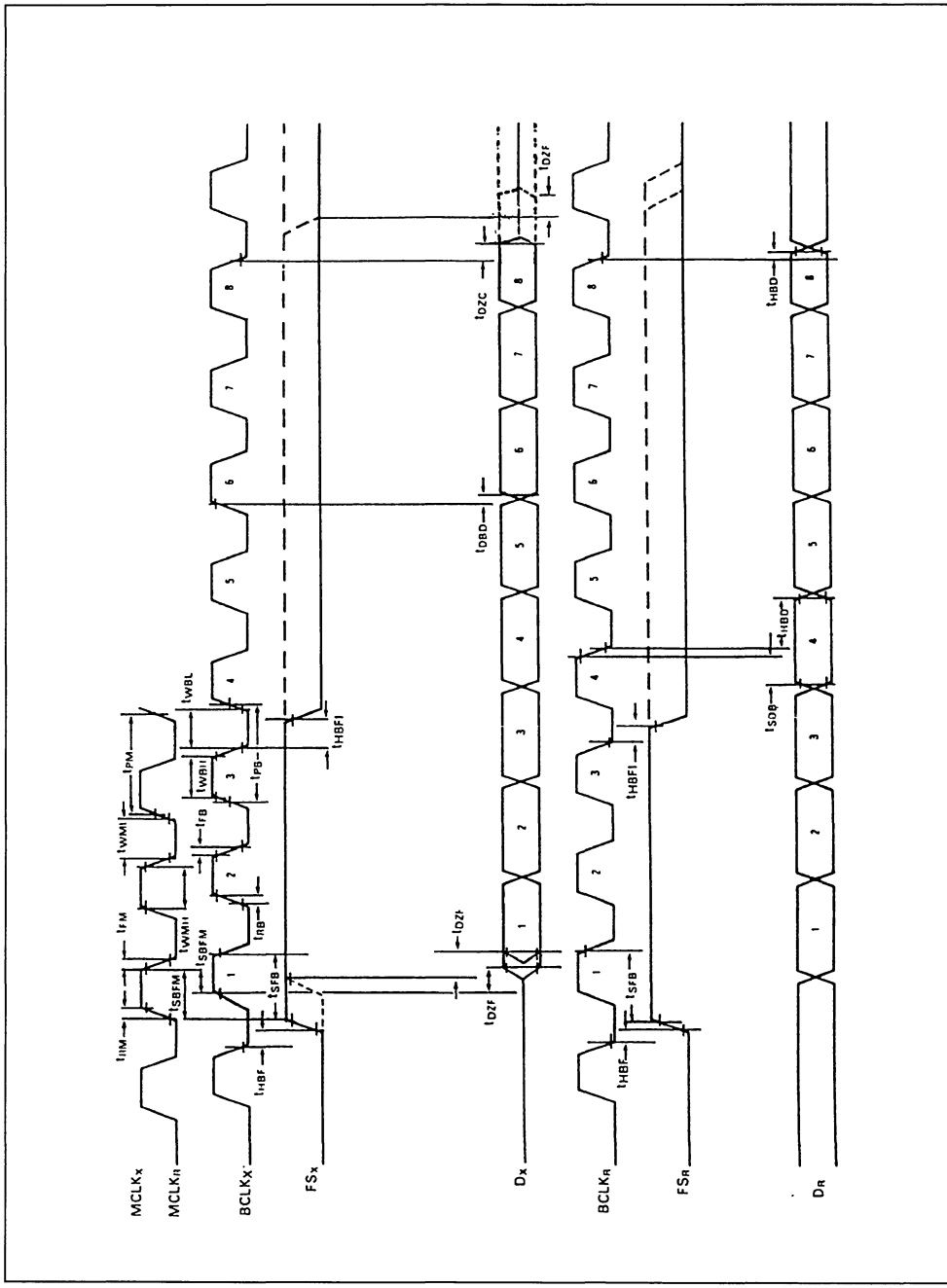


Figure 4 : Long Frame Sync Timing.



TRANSMISSION CHARACTERISTICS

(all devices) $T_A = -40\,°C$ to $85\,°C$, $V_{CC} = 5\,V \pm 5\,\%$, $VBB = -5\,V \pm 5\%$, $GNDA = 0\,V$, $f = 1.02\,kHz$, $V_{IN} = 0\,dBm0$ transmit input amplifier connected for unity-gain non-inverting (unless otherwise specified).

AMPLITUDE RESPONSE

Symbol	Parameter	Min.	Typ.	Max.	Unit
	Absolute Levels – Nominal 0 dBm0 level is 4 dBm (600 Ω). 0 dBm0	–	1.2276	–	V_{rms}
t_{MAX}	Max Overload Level 3.14 dBm0 (A LAW) 3.17 dBm0 (U LAW)	– –	2.492 2.501	– –	V_{PK}
G_{XA}	Transmit Gain, Absolute ($T_A = 25\,°C$, $V_{CC} = 5\,V$, $V_{BB} = -5\,V$) Input at $GS_X = 0$ dBm0 at 1020 Hz	– 0.15	–	0.15	dB
G_{XR}	Transmit Gain, Relative to G_{XA} f = 16 Hz f = 50 Hz f = 60 Hz f = 180 Hz f = 200 Hz f = 300 Hz – 3000 Hz f = 3200 Hz f = 3300 Hz f = 3400 Hz f = 4000 Hz f = 4600 Hz and up, measure response from 0 Hz to 4000 Hz	– – – – 2.8 – 1.8 – 0.15 – 0.35 – 0.35 – 0.7 – –	– – – – – – – – – – –	– 40 – 30 – 26 – 0.2 – 0.1 0.15 0.20 0.05 0 – 14 – 32	dB
G_{XAT}	Absolute Transmit Gain Variation with Temperature	– 0.15	–	0.15	dB
G_{XAV}	Absolute Transmit Gain Variation with Supply Voltage ($V_{CC} = 5\,V \pm 5\,\%$, $V_{BB} = -5\,V \pm 5\,\%$)	– 0.05	–	0.05	dB
G_{XRL}	Transmit Gain Variations with Level Sinusoidal Test Method Reference Level = – 10 dBm0 VF_XI^+ = – 40 dBm0 to + 3 dBm0 VF_XI^+ = – 50 dBm0 to – 40 dBm0 VF_XI^+ = – 55 dBm0 to – 50 dBm0	 – 0.2 – 0.4 – 1.2	 – – –	 0.2 0.4 1.2	dB
G_{RA}	Receive Gain, Absolute ($T_A = 25\,°C$, $V_{CC} = 5\,V$, $V_{BB} = -5\,V$) Input = Digital Code Sequence for 0 dBm0 Signal at 1020 Hz	– 0.15	–	0.15	dB
G_{RR}	Receive Gain, Relative to G_{RA} f = 0 Hz to 3000 Hz f = 3200 Hz f = 3300 Hz f = 3400 Hz f = 4000 Hz	 – 0.15 – 0.35 – 0.35 – 0.7 –	 – – – – –	 0.15 0.2 0.05 0 – 14	dB
G_{RAT}	Absolute Receive Gain Variation with Temperature	–	–	± 0.15	dB
G_{RAV}	Absolute Receive Gain Variation with Supply Voltage ($V_{CC} = 5\,V \pm 5\,\%$, $V_{BB} = -5\,V \pm 5\,\%$)	–	–	± 0.05	dB
G_{RRL}	Receive Gain Variations with Level Sinusoidal Test Method ; Reference input PCM code corresponds to an ideally encoded – 10 dBm0 signal PCM level = – 40 dBm0 to + 3 dBm0 PCM level = – 50 dBm0 to – 40 dBm0 PCM level = – 55 dBm0 to – 50 dBm0	 – 0.2 – 0.4 – 1.2	 – – –	 0.2 0.4 1.2	dB
V_{RO}	Receive Output Drive Level ($R_L = 600\,\Omega$)	– 2.5	–	2.5	V

TRANSMISSION CHARACTERISTICS (continued)

ENVELOPE DELAY DISTORTION WITH FREQUENCY

Symbol	Parameter	Min.	Typ.	Max.	Unit
D_{XA}	Transmit Delay, Absolute (f = 1600 Hz)	–	290	315	µs
D_{XR}	Transmit Delay, Relative to D_{XA}				µs
	f = 500 Hz – 600 Hz	–	195	220	
	f = 600 Hz – 800 Hz	–	120	145	
	f = 800 Hz – 1000 Hz	–	50	75	
	f = 1000 Hz – 1600 Hz	–	20	40	
	f = 1600 Hz – 2600 Hz	–	55	75	
	f = 2600 Hz – 2800 Hz	–	80	105	
	f = 2800 Hz – 3000 Hz	–	130	155	
D_{RA}	Receive Delay, Absolute (f = 1600 Hz)	–	180	200	µs
D_{RR}	Receive Delay, Relative to D_{RA}				µs
	f = 500 Hz – 1000 Hz	– 40	– 25	–	
	f = 1000 Hz – 1600 Hz	– 30	– 20	–	
	f = 1600 Hz – 2600 Hz	–	70	90	
	f = 2600 Hz – 2800 Hz	–	100	125	
	f = 2800 Hz – 3000 Hz	–	145	175	

NOISE

Symbol	Parameter	Min.	Typ.	Max.	Unit
N_{XP}	Transmit Noise, P Message Weighted (ETC 5057, $VF_XI^+ = 0$ V)	–	– 74	– 69 (note 1)	dBm0p
N_{RP}	Receive Noise, P Message Weighted – ETC 5057 U LAW, PCM Code Equals Positive Zero	–	– 82	– 79	dBm0p
N_{XC}	Transmit Noise, C Message Weighted (ETC 5054, $VFXI^+ = 0$ V)	–	12	16	dBrnC0
N_{RC}	Receive Noise, C Message Weighted ETC 5054 U LAW, PCM Code Equals Alternating Positive and Negative Zero	–	8	11	dBrnC0
N_{RS}	Noise, Single Frequency f = 0 kHz to 100 kHz, Loop Around Measurement, $VF_XI^+ = 0$ Vrms	–	–	– 53	dBm0
$PPSR_X$	Positive Power Supply Rejection, Transmit $VF_XI^+ = 0$ Vrms, $V_{CC} = 5.0\ V_{DC} + 100$ mVrms, f = 0 kHz – 50 kHz	40	–	–	dBp
$NPSR_X$	Negative Power Supply Rejection, Transmit $VF_XI^+ = 0$ Vrms, $V_{BB} = -5.0\ V_{DC} + 100$ mVrms, f = 0 kHz – 50 kHz	40	–	–	dBp
$PPSR_R$	Positive Power Supply Rejection, Receive (PCM code equals positive zero, $V_{CC} = 5.0\ V_{DC} + 100$ mVrms)				
	f = 0 Hz – 4000 Hz	40	–	–	dBp
	f = 4 kHz – 25 kHz	40	–	–	dB
	f = 25 kHz – 50 KHZ	36	–	–	dB
$NPSR_R$	Negative Power Supply Rejection, Receive (PCM code equals positive zero, $V_{BB} = -5.0\ V_{DC} + 100$ mVrms)				
	f = 0 Hz – 4000 Hz	40	–	–	dBp
	f = 4 kHz – 25 kHz	40	–	–	dB
	f = 25 kHz – 50 kHz	36	–	–	dB

TRANSMISSION CHARACTERISTICS (continued)

Symbol	Parameter	Min.	Typ.	Max.	Unit
SOS	Spurious out-of band signals at the channel output. Loop around measurement, 0 dBm0, 300 Hz – 3400 Hz input applied to VF_XI^+, measure individual image signals at VF_R0				dB
	4600 Hz – 7600 Hz	–	–	– 32	
	7600 Hz – 8400 Hz	–	–	– 40	
	8400 Hz – 100,000 Hz	–	–	– 32	

DISTORTION

Symbol	Parameter		Min.	Typ.	Max.	Unit
STD_X or STD_R	Signal to Total Distortion (sinusoidal test method)					dBp
	Transmit or Receive Half-channel					
	Level = 3 dBm0		33	–	–	
	= 0 dBm0 to – 30 dBm0		36	–	–	
	= – 40 dBm0	XMT	29	–	–	
		RCV	30	–	–	
	= – 55 dBm0	XMT	14	–	–	
		RCV	15	–	–	
SFD_X	Single Frequency Distortion, Transmit		–	–	– 46	dB
SFD_R	Single Frequency Distortion, Receive		–	–	– 46	dB
IMD	Intermodulation Distortion Loop Around Measurement, VF_XI^+ = – 4 dBm0 to – 21 dBm0, Two Frequencies in the Range 300 Hz – 3400 Hz		–	–	– 41	dB

CROSSTALK

Symbol	Parameter	Min.	Typ.	Max.	Unit
CT_{X-R}	Transmit to Receive Crosstalk, 0 dBm0 Transmit Level f = 300 Hz – 3400 Hz, D_R = Steady PCM Mode	–	–	– 65	dB
CT_{R-X}	Receive to Transmit Crosstalk, 0 dBm0 Receive Level f = 300 Hz – 3400 Hz, VF_XI = 0 V	–	–	– 65 (note 2)	dB

Notes : 1. Measured by extrapolation from the distortion test result.
2. CT_{R-X} is measured with a – 40 dBm0 activating signal applied at VF_XI^+.

ENCODING FORMAT AT D_X OUTPUT

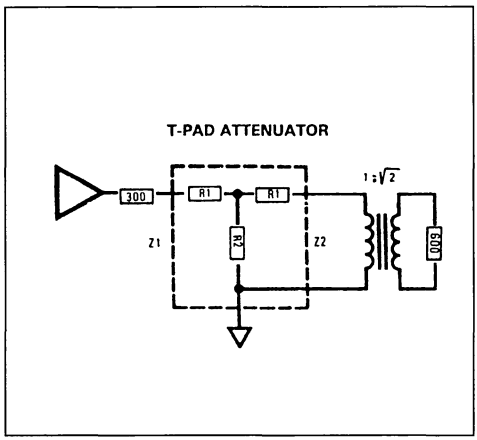
	A–Law (includes even bit inversion)	μLaw
V_{IN} (at GS_X) = + Full-scale	1 0 1 0 1 0 1 0	1 0 0 0 0 0 0 0
V_{IN} (at GS_X) = 0 V	1 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1	1 1 1 1 1 1 1 1 0 1 1 1 1 1 1 1
V_{IN} (at GS_X) = – Full-scale	0 0 1 0 1 0 1 0	0 0 0 0 0 0 0 0

APPLICATIONS INFORMATION

POWER SUPPLIES

While the pins of the ETC5050 family are well protected against electrical misuse, it is recommended that the standard CMOS practice be followed, ensuring that ground is connected to the device before any other connections are made. In applications where the printed circuit board may be plugged into a "hot" socket with power and clocks already present, an extra long ground pin in the connector is useful.

All ground connections to each device should meet at a common point as close as possible to the GNDA pin.



$$R1 = Z1 \left(\frac{N^2+1}{N^2-1}\right) - 2 \quad Z1.Z2 \left(\frac{N}{N^2-1}\right)$$

$$R2 = 2\sqrt{Z1.Z2} \left(\frac{N}{N2-1}\right)$$

Where : $N = \sqrt{\frac{\text{POWER IN}}{\text{POWER OUT}}}$

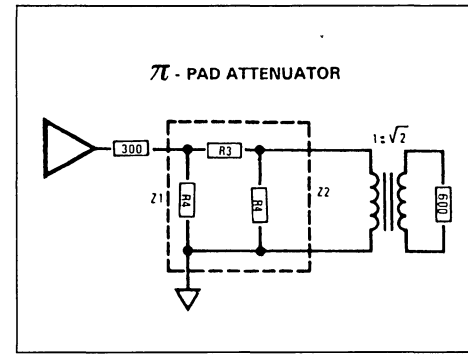
and :

$$S = \sqrt{\frac{Z1}{Z2}}$$

Also : $Z = \sqrt{Z_{SC} \cdot Z_{OC}}$

Where Z_{SC} = impedance with short circuit termination

and Z_{OC} = impedance with open circuit termination.



$$R3 = \sqrt{\frac{Z1.Z2}{2}} \left(\frac{N^2-1}{N}\right)$$

$$R4 = Z1 \left(\frac{N^2-1}{N^2-2NS+1}\right)$$

This minimizes the interaction of ground return currents flowing through a common bus impedance. 0.1 µF supply decoupling capacitors should be connected from this common ground point to V_{CC} and V_{BB}.

For best performance, the ground point of beach/FILTER on a card should be connected to a common card. This common ground point should be decoupled to V_{CC} and V_{BB} with 10 µF capacitors.

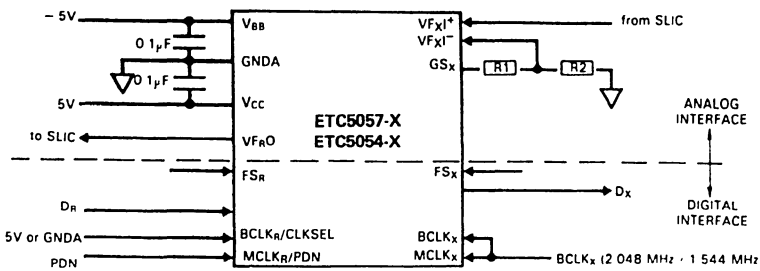
RECEIVE GAIN ADJUSTMENT

For applications where a ETC5050 family CODEC/filter receive output must drive a 600 Ω load, but a peak swing lower then ± 2.5 V is required, the receive gain can be easily adjusted by inserting a matched T-pad or π-pad at the output. Table II lists the required resistor values for 600 Ω terminations. As these are generally non-standard values, the equations can be used to compute the attenuation of the closest pratical set of resistors. It may be necessary to use unequal values for the R1 or R4 arms of the attenuators to achieve a precise attenuation. Generally it is tolerable to allow a small deviation of the input impedance from nominal while still maintaining a good return loss. For example a 30 dB return loss against 600 Ω is obtained if the output impedance of the attenuator is in the range 282 Ω to 319 Ω (assuming a perfect transformer).

Table 2 : Attenuator Tables for Z1 = Z2 = 300 Ω (all values in Ω).

dB	R1	R2	R3	R4
0.1	1.7	26 k	3.5	52 k
0.2	3.5	13 k	6.9	26 k
0.3	5.2	8.7 k	10.4	17.4 k
0.4	6.9	6.5 k	13.8	13 k
0.5	8.5	5.2 k	17.3	10.5 k
0.6	10.4	4.4 k	21.3	8.7 k
0.7	12.1	3.7 k	24.2	7.5 k
0.8	13.8	3.3 k	27.7	6.5 k
0.9	15.5	2.9 k	31.1	5.8 k
1.0	17.3	2.6 k	34.6	5.2 k
2	34.4	1.3 k	70	2.6 k
3	51.3	850	107	1.8 k
4	68	650	144	1.3 k
5	84	494	183	1.1 k
6	100	402	224	900
7	115	380	269	785
8	129	284	317	698
9	143	244	370	630
10	156	211	427	527
11	168	184	490	535
12	180	161	550	500
13	190	142	635	473
14	200	125	720	450
15	210	110	816	430
16	218	98	924	413
18	233	77	1.17 k	386
20	246	61	1.5 k	366

Figure 5 : Typical Synchronous Application.

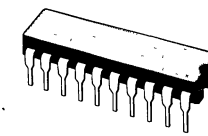


Note 1 : XMIT gain = $20 \times \log \left(\frac{R1 + R2}{R2} \right)$ (R1 + R2) > 10 kΩ.

PARALLEL DATA INTERFACE CODEC/FILTER

- COMPLETE CODEC AND FILTERING SYSTEM INCLUDING :
  - TRANSMIT HIGH PASS AND LOW PASS FILTERING
  - RECEIVE LOW PASS FILTER WITH SIN x/x CORRECTION
  - RECEIVE POWER AMPLIFIER
  - ACTIVE RC NOISE FILTERS
  - A-LAW COder AND DECoder
  - INTERNAL PRECISION VOLTAGE REFERENCE
  - INTERNAL AUTO-ZERO CIRCUITRY
- MEETS OR EXCEEDS ALL D3/D4 AND CCITT SPECIFICATIONS
- ± 5 V OPERATION
- LOW OPERATING POWER - TYPICALLY 60mW
- POWER DOWN STANDBY MODE - TYPICALLY 3 mW
- HIGH SPEED TRI-STATE ® DATA BUS.
- 2 LOOPBACK TEST MODES
- SECOND SOURCE OF TP3056

The ETC5056 is especially designed to be used with a line interface controller providing local time and space switching in a distributed control switching system.



DIP20
(Ceramic)

ORDER CODES : ETC5056J

DESCRIPTION

The ETC5056 family is a A-law monolithic PCM CODEC/filters utilizing the A/D and D/A conversion architecture shown in figure 1, parallel I/O data bus interface. The device is fabricated using double-poly CMOS process.

The encode portion consists of an input gain adjust amplifier, an active RC pre-filter which eliminates very high frequency noise prior to entering a switched-capacitor band-pass filter that rejects signals below 200 Hz and above 3400 Hz. Also-included are auto-zero circuitry and a companding coder which samples the filtered signal and encodes it in the companded A-law PCM format..

The decode portion consists of an expanding decoder, which reconstructs the analog signal from the companded A-law code, a low-pass filter which corrects for the sin x/x response of the decoder output and rejects signals above 3400 Hz and is followed by a single-ended power amplifier capable of driving low impedance loads.

PIN CONNECTION

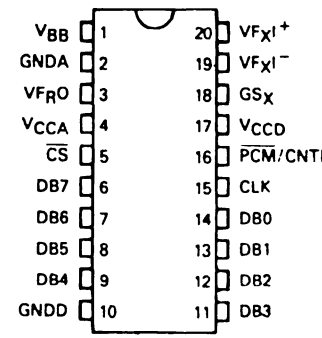
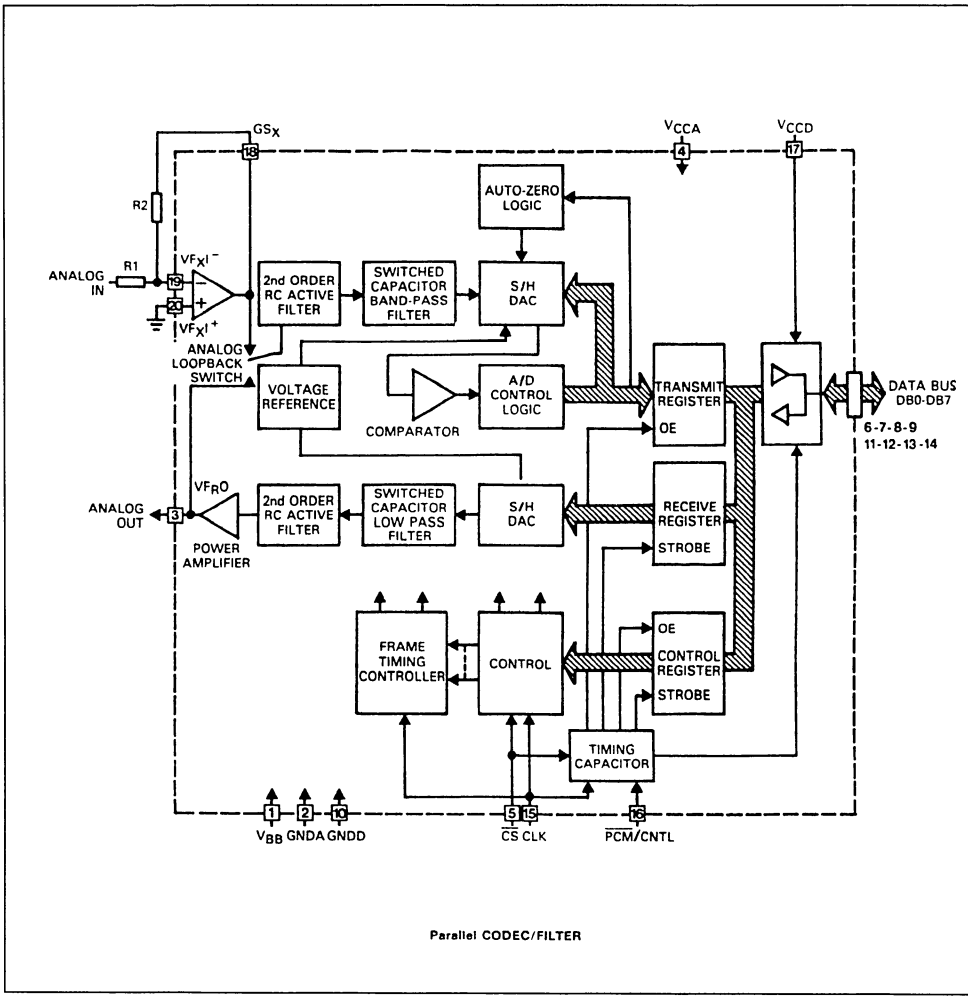


Figure 1 : Block Diagram.



Parallel CODEC/FILTER

PIN DESCRIPTION

Name	Pin Type*	N°	Description
V_{BB}	S	1	Negative power supply pin. $V_{BB} = -5$ V ± 5 %
GNDA	GND	2	Analog ground. All analog signals are referenced to this pin.
VF_RO	0	3	Analog output of the receive power amplifier. This output can drive a 600 Ω load to ± 2.5 V.
V_{CCA}	S	4	Positive power supply voltage pin for the analog circuitry. $V_{CCA} = 5$ V ± 5 %. Must be connected to V_{CCD}.
$\overline{CS}$	I	5	Device chip select input which controls READ write and TRI-STATE® operations on the data bus. $\overline{CS}$ does not control the state of any analog functions.
DB7	I/O	6	Bit 7 I/O on the data bus. The PCM LSB.
DB6	I/O	7	Bit 6 I/O on the data bus.
DB5	I/O	8	Bit 5 I/O on the data bus.
DB4	I/O	9	Bit 4 I/O on the data bus.
GNDD	GND	10	Digital ground. All digital signals are referenced to this pin.
DB3	I/O	11	Bit 3 I/O on the data bus.
DB2	I/O	12	Bit 2 I/O on the data bus.
DB1	I/O	13	Bit 1 I/O on the data bus.
DB0	I/O	14	Bit 0 I/O on the data bus. This is the PCM sign bit.
CLK	I	15	The clock input for switched-capacitor filter and CODEC. Clock frequency must be 768 kHz, 772 kHz, 1.024 MHz or 1.28 MHz and must be synchronous with the system clock input.
$\overline{PCM}$/CNTL	I	16	This control input determines whether the information on the data bus is PCM data or control data.
V_{CCD}	S	17	Positive power supply pin for the bus drivers. $V_{CCD} = 5$ V ± 5 %. Must be connected to V_{CCA}.
GS_X	O	18	Analog output of the transmit input amplifier. Used to externally set gain.
VF_XI^-	I	19	Inverting input of the transmit input amplifier.
VF_XI^+	I	20	Non-inverting input of the transmit input amplifier.

* I : Input, O · Output, S : Power Supply.

FUNCTIONAL DESCRIPTION

CLOCK AND DATA BUS CONTROL

The CLK input signal provides timing for the encode and decode logic and the switched-capacitor filters. It must be one of the frequencies listed in Table 1 and must be correctly selected by control bits C0 and C1.

CLK also functions as a READ/$\overline{\text{WRITE}}$ control signal, with the device reading the data bus on a positive half-clock cycle and writing the bus on a negative half-clock cycle, as shown in figure 4.

POWER-UP

When power is first applied, power-on reset circuitry initializes the CODEC/filter and sets it in the power-down mode. All non-essential circuits are deactivated and the data bus outputs, DB0-DB7, and receive power amplifier output, VF_RO, are in high impedance states.

The ETC5056 is powered-up via a command to the control register (see Control Register Functions). This sets the device in the standby mode with all circuitry activated, but encoding and decoding do not begin until PCM READ and PCM WRITE chip selects occur.

Table 1 : Control Bit Functions.

Control Bits	Function		
C0, C1	Select Clock Frequency		
	C0	**C1**	**Frequency**
	0	X	1.024 MHz
	1	0	0.768 MHz or 0.772 MHz
	1	1	1.28 MHz
C2, C3	Digital and Analog Loopback		
	C2	**C3**	**Mode**
	1	X	Digital Loopback
	0	1	Analog Loopback
	0	0	Normal
C4	Power-down/power-up		
	1 = Power-down 0 = Power-up		
C5	ETC5056 0 = A-law without Even Bit Inversion 1 = A-law with Even Bit Inversion		
C6, C7	Don't Care		

DATA BUS ASSIGNEMENT

The parallel I/O data bus is defined as follows :

Data Type	DB0	DB7
PCM	Sign Bit	LSB
Control Data	C0	C7

READING THE BUS

If CLK is low when $\overline{\text{CS}}$ goes low, bus data is gated in during the next positive half-clock cycle of CLK and latched on the negative-going transition. If PCM/CNTL is low during the falling $\overline{\text{CS}}$ transition, then the bus data is defined as PCM voice data, which is latched into the receive register. This also functions as an internal receive frame synchronization pulse to start a decode cycle and must occur once per receive frame ; i.e., at an 8 KHz rate.

If PCM/CNTL is high during the falling $\overline{\text{CS}}$ transition, the bus data is latched into the control register. This does not effect frame synchronization.

WRITING THE BUS

If CLK is high when $\overline{\text{CS}}$ goes low, at the next falling transition of CLK, the bus drivers are enabled and either the PCM transmit data or the contents of the control register are gated into the bus, depending on the level of PCM/CNTL at the $\overline{\text{CS}}$ transition. If PCM/CNTL is low during the $\overline{\text{CS}}$ falling transition, the transmit register data is written to the bus. An internal transmit frame synchronization pulse is also generated to start an encode cycle, and this must occur once per transmit frame ; i.e., at an 8 KHz rate.

If PCM/CNTL is high during the $\overline{\text{CS}}$ falling transition, the control register data is written to the bus. This does not affect frame synchronization.

The receive register contents may also be written back to the bus, as described in the Digital Loopback section.

Except during a WRITE cycle, the bus drivers are in TRI-STATE mode.

CONTROL REGISTER FUNCTIONS

Writing to the control register allows the user to set the various operating states of the ETC5056. The control register can also be read back via the data bus to verify the current operating mode of the device.

1. CLK Select.
   Since one of three distinct clock frequencies may be used, the actual frequency must be known by

the device for proper operation of the switched-capacitor filters. This is achieved by writting control register bits C0 and C1, normally in the same WRITE cycle that powers-up the device, and before any PCM data transfers take place.

2. Digital Loopback.
In order to establish that a valid path has been selected through a network, it is sometimes desirable to be able to send data through the network to its destination, then loop it back through the network return path to the originating source where the data can be verified. This loopback function can be performed in ETC5056 by setting control register bit C2 to 1. With C2 set, the PCM data in the receive register will be written back into the data bus during the next PCM WRITE cycle. In the digital loopback mode, the receive section is set to an idle channel condition in order to maintain a low impedance termination at VF_RO.
3. Analog Loopback.
In the analog loopback mode, the transmit filter input is switched from the gain adjust amplifier to the receive power amplifier output, forming a unity-gain loop from the receive register back to the transmit register. This mode is enterred by setting control register bits C2 to 0 and C3 to 1. The receive power amplifier continues to drive the load in this mode.
4. Power-Down/Power-Up.
The ETC5056 may be put in the power-down mode by setting control register bit C4 to 1. Conversely, setting bit C4 to 0 power up the device.

TRANSMIT FILTER AND ENCODE SECTION

The transmit section input is an operational amplifier with provision for gain adjustment using two external resistors, see figure 2. The low noise and wide bandwidth allow gains in excess of 20 dB across the audio passband to be realized. The op amp drives a unity-gain filter consisting of a 2 nd order RC active pre-filter, followed by an 8 th order switched-capacitor bandpass filter clocked at 256 KHz.

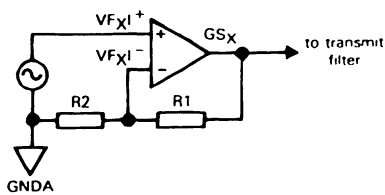
The output of this filter directly drives the encoder sample-and-hold circuit. The A/D is of companding type according to A-law (ETC5056) coding schemes. A precision voltage reference is trimmed in manufacturing to provide an input overload (t_{max}) of nominally 2.5 V peak (see table of Transmission Characteristics). Any offset voltage due to the filters or comparator is cancelled by sign bit integration in the auto-zero circuit.

The total encoding delay referenced to a PCM WRITE chip select will be approximately 165 µs (due to the transmit filter) plus 125 µs (due to endoding delay), which totals 290 µs.

DECODER AND RECEIVE FILTER SECTION

The receive section consists of an expanding DAC which drives a 5 th order switched-capacitor low pass filter clocked at 256 KHz. The decoder is of A-law (ETC5056) coding law and the 5 th order low pass filter corrects for the sin x/x attenuation due to the 8 KHz sample/hold. The filter is then followed by a 2 nd order RC active post-filter. The power amplifier output stage is capable of driving a 600 Ω load to a level of 7.2 dBm. The receive section has unity-gain. Following a PCM READ chip select, the decoding cycle begins, and 10 µs later the decoder DAC output is updated. The total decoder delay is – 10 µs (decoder update) plus 110 µs (filter delay) plus 62.5 µs (1/2 frame), which gives approximately 180 µs.

Figure 2 : Transmit Gain Adjustement.



Non inverting transmit gain = $20 \log_{10} \left(\frac{R1 + R2}{R2} \right)$

Out gain to provide peak overload level = t_{max} at G_{SX} (see transmission characteristics)

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
	GNDD to GNDA	± 0.3	V
V_{CC}	V_{CCA} or V_{CCD} to GNDD or GNDA	± 7.0	V
V_{IN}, V_{OUT}	Voltage at Any Input or Output	V_{CC} + 0.3 to V_{BB} – 0.3	V
	Voltage at Any Digital Input or Output	V_{CC} + 0.3 to GNDD – 0.3	V
T_{oper}	Operating Temperature Range	– 25 to + 125	°C
T_{stg}	Storage Temperature Range	– 60 to + 150	°C
	Lead Temperature (soldering, 10 seconds)	300	°C

ELECTRICAL OPERATING CHARACTERSITICS

V_{CC} = 5.0 V ± 5 %, V_{BB} = – 5 V ± 5 %, GNDA = 0 V, T_A = 0 °C to 70 °C (unless otherwise noted) ; Typical characteristics specified at V_{CC} = 5.0 V, V_{BB} = – 5.0 V, T_A = 25 °C, all signals are referenced to GNDA.

DIGITAL INTERFACE

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{IL}	Input Low Voltage	–	–	0.6	V
V_{IH}	Input High Voltage	2.2	–	–	V
V_{OL}	Output Low Voltage IL = 2.5 mA, DB0-DB7	–	–	0.4	V
V_{OH}	Output High Voltage IH = – 2.5 mA, DB0-DB7	2.4	–	–	V
I_{IL}	Input Low Current (GNDA ≤ V_{IN} ≤ V_{IL}, all digital inputs)	– 10	–	10	µA
I_{IH}	Input High Current (V_{IH} ≤ V_{IN} ≤ V_{CC})	– 10	–	10	µA
I_{OZ}	Output Current in High impedance State (TRI-STATE) (GNDD ≤ V_O ≤ V_{CC}), DB0-DB7	– 10	–	10	µA

ANALOG INTERFACE WITH TRANSMIT INPUT AMPLIFIER (all devices)

Symbol	Parameter		Min.	Typ.	Max.	Unit
I_IXA	Input Leakage Current (– 2.5 V ≤ V ≤ + 2.5 V)	VF_XI^+ or VF_XI^-	– 200	–	200	nA
R_IXA	Input Resistance (– 2.5 V ≤ V ≤ + 2.5 V)	VF_XI^+ or VF_XI^-	10	–	–	MΩ
R_OXA	Output Resistance (closed loop, unity gain)		–	1	3	Ω
R_LXA	Load Resistance	GS_X	10	–	–	kΩ
C_LXA	Load Capacitance	GS_X	–	–	50	pF
V_OXA	Output Dynamic Range (R_L ≥ 10 kΩ)	GS_X	± 2.8	–	–	V
A_VXA	Voltage Gain (VF_XI^+ to GS_X)		5000	–	–	V/V
F_UXA	Unity Gain Bandwidth		1	2	–	MHz
$V_{OS}XA$	Offset Voltage		– 20	–	20	mV
$V_{CM}XA$	Common-mode Voltage		– 2.5	–	2.5	V
CMRRXA	Common-mode Rejection Ratio		60	–	–	dB
PSRRXA	Power Supply Rejection Ratio		60	–	–	dB

ELECTRICAL OPERATING CHARACTERSITICS (continued)

ANALOG INTERFACE WITH RECEIVE FILTER (all devices)

Symbol	Parameter	Min.	Typ.	Max.	Unit
R_ORF	Output Resistance VF_RO	–	1	3	Ω
R_LRF	Load Resistance ($VF_RO = \pm 2.5$ V)	600	–	–	Ω
C_LRF	Load Capacitance	–	–	500	pF
VOS_RO	Output DC Offset Voltage	– 200	–	200	mV

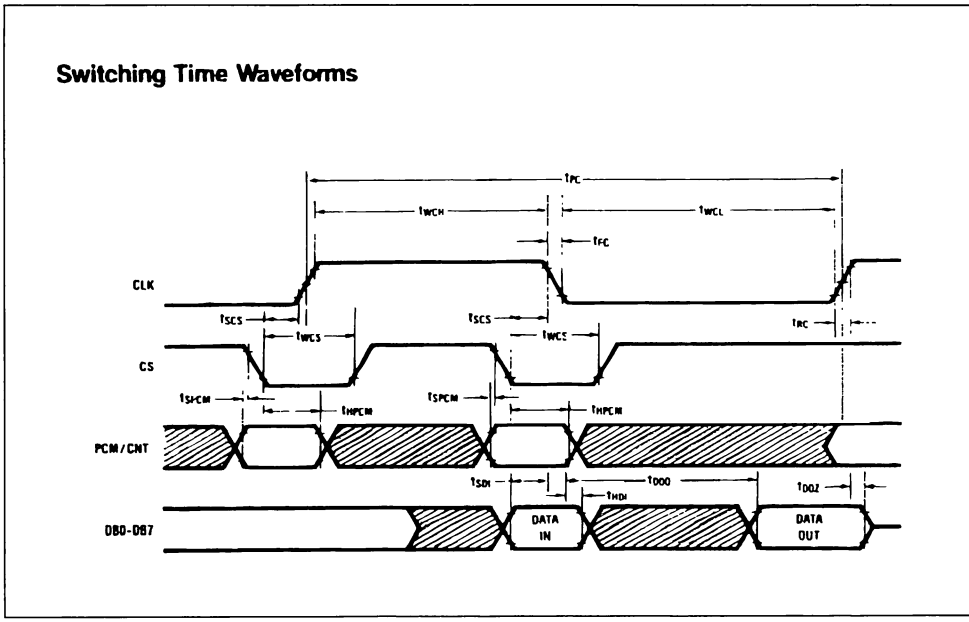
POWER DISSIPATION (all devices)

Symbol	Parameter	Min.	Typ.	Max.	Unit
$I_{CC}0$	Power-down Current	–	0.5	1.5	mA
$I_{BB}0$	Power-down Current	–	0.05	0.3	mA
$I_{CC}1$	Active Current	–	6.0	9.0	mA
$I_{BB}1$	Active Current	–	6.0	9.0	mA

TIMING SPECIFICATIONS

Symbol	Parameter	Value			Unit
		Min.	Typ.	Max.	
t_{PC}	Period of Clock	760	–	–	ns
t_{WCH}	Width of Clock High	330	–	–	ns
t_{WCL}	Width of Clock Low	330	–	–	ns
t_{RC}	Rise Time of Clock	–	–	50	ns
t_{FC}	Fall Time of Clock	–	–	50	ns
t_{SCS}	Set-up Time of CLK High or Low	100	–	–	ns
t_{HCS}	Hold Time from $\overline{CS}$ Low to CLK	100	–	–	ns
t_{WCS}	Width of Chip Select	100	–	–	ns
t_{SPCM}	Set-up Time of $\overline{PCM}$/CNTL	0	–	–	ns
t_{HPCM}	Hold Time of $\overline{PCM}$/CNTL	100	–	–	ns
t_{SDI}	Set-up Time of Data in	50	–	–	ns
t_{HDI}	Hold Time of Data in	20	–	–	ns
t_{DDO}	Delay Time of Data Out Valid (C_L = 0 pF to 200 pF)	90	–	260	ns
t_{DDZ}	Delay Time to Data Output Disabled (C_L = 0 pF to 200 pF)	20	–	80	ns

Figure 4 : Timing Waveforms for ETC5056.



TRANSMISSION CHARACTERSITICS

(all devices) T_A = 0 °C to 70 °C, V_{CC} = 5 V ± 5 %, V_{BB} = – 5 V ± 5 %, GNDA = 0 v, f = 1.02 kHz, V_{IN} = 0 dBm0 transmit input amplifier connected for unity-gain non-inverting (unless otherwise specified).

AMPLITUDE RESPONSE

Symbol	Parameter	Min.	Typ.	Max.	Unit
	Absolute Levels – Nominal 0 dBm0 level is 4 dBm (600 Ω). 0 dBm0 ETC5056	–	1.2276	–	V_{rms}
t_{MAX}	Max Overload Level 3.17 dBm0	–	2.501	–	V_{PK}
G_{XA}	Transmit Gain, Absolute (T_A = 25 °C, V_{CC} = 5 V, V_{BB} = – 5 V) Input at GS_X = 0 dBm0 at 1020 Hz	– 0.15	–	0.15	dB
G_{XR}	Transmit Gain, Relative to G_{XA}				dB
	f = 16 Hz	–	–	– 40	
	f = 50 Hz	–	–	– 30	
	f = 60 Hz	–	–	– 26	
	f = 180 Hz	– 2.8	–	– 0.2	
	f = 200 Hz	– 1.8	–	– 0.1	
	f = 300 Hz – 3000 Hz	– 0.15	–	– 0.15	
	f = 3300 Hz	– 0.35	–	+ 0.05	
	f = 3400 Hz	– 0.7	–	0	
	f = 4000 Hz	–	–	– 14	
	f = 4600 Hz and up, measure response from O Hz to 4000 Hz	–	–	– 32	
G_{XAT}	Absolute Transmit Gain Variation with Temperature (T_A = 0 °C to + 80 °C)	– 0.1	–	+ 0.1	dB
G_{XAV}	Absolute Transmit Gain Variation with Supply Voltage (V_{CC} = 5 V ± 5 %, V_{BB} = – 5 V ± 5 %)	– 0.05	–	+ 0.05	dB
G_{XRL}	Transmit Gain Variations with Level Sinusoidal Test Method Reference Level = – 10 dBm0				dB
	VF_XI^+ = – 40 dBm0 to + 3 dBm0	– 0.2	–	0.2	
	VF_XI^+ = – 50 dBm0 to – 40 dBm0	– 0.4	–	0.4	
	VF_XI^+ = – 55 dBm0 to – 50 dBm0	– 1.2	–	1.2	
G_{RA}	Receive Gain, Absolute (T_A = 25 °C, V_{CC} = 5 V, V_{BB} = – 5 V) Input = Digital Code Sequence for 0 dBm0 Signal at 1020 Hz	– 0.15	–	0.15	dB
G_{RR}	Receive Gain, Relative to G_{RA}				dB
	f= 0 Hz to 3000 Hz	– 0.15	–	0.15	
	f = 3300 Hz	– 0.35	–	0.05	
	f = 3400 Hz	– 0.7	–	0	
	f = 4000 Hz	–	–	– 14	
G_{RAT}	Absolute Receive Gain Variation with Temperature (T_A = 0 °C to + 70 °C)	– 0.1	–	+ 0.1	dB
G_{RAV}	Absolute Receive Gain Variation with Supply Voltage (V_{CC} = 5 V ± 5 %, V_{BB} = – 5 V ± 5 %)	– 0.05	–	+ 0.05	dB
G_{RRL}	Receive Gain Variations with Level Sinusoidal Test Method ; Reference input PCM code corresponds to an ideally encoded – 10 dBm0 signal				dB
	PCM level = – 40 dBm0 to + 3 dBm0	– 0.2	–	0.2	
	PCM level = – 50 dBm0 to – 40 dBm0	– 0.4	–	0.4	
	PCM level = – 55 dBm0 to – 50 dBm0	– 1.2	–	1.2	
V_{RO}	Receive Output Drive Level (R_L = 600 kΩ)	– 2.5	–	2.5	V

TRANSMISSION CHARACTERSITICS (continued)

ENVELOPE DELAY DISTORTION WITH FREQUENCY

Symbol	Parameter	Min.	Typ.	Max.	Unit
D_{XA}	Transmit Delay, Absolute (f = 1600 Hz)	–	290	315	µs
D_{XR}	Transmit Delay, Relative to D_{XA}				µs
	f = 500 Hz – 600 Hz	–	195	220	
	f = 600 Hz – 800 Hz	–	120	145	
	f = 800 Hz – 1000 Hz	–	50	75	
	f = 1000 Hz – 1600 Hz	–	20	40	
	f = 1600 Hz – 2600 Hz	–	55	75	
	f = 2600 Hz – 2800 Hz	–	80	105	
	f = 2800 Hz – 3000 Hz	–	130	155	
D_{RA}	Receive Delay, Absolute (f = 1600 Hz)	–	180	200	µs
D_{RR}	Receive Delay, Relative to D_{RA}				µs
	f = 500 Hz – 1000 Hz	– 40	– 25	–	
	f = 1000 Hz – 1600 Hz	– 30	– 20	–	
	f = 1600 Hz – 2600 Hz	–	70	90	
	f = 2600 Hz – 2800 Hz	–	100	125	
	f = 2800 Hz – 3000 Hz	–	145	175	

NOISE

Symbol	Parameter	Min.	Typ.	Max.	Unit
N_{XP}	Transmit Noise, P Message Weighted (VF_XI^+ = 0 V)	–	– 74	– 69 (note 1)	dBM0p
N_{RP}	Receive Noise, P Message Weighted (PCM Code Equals Positive Zero)	–	– 82	– 79	dBm0p
N_{RS}	Noise, Single Frequency f = 0 kHz to 100 kHz, Loop Around Measurement, VF_XI^+ = 0 Vrms	–	–	– 53	dBm0
$PPSR_X$	Positive Power Supply Rejection, Transmit VF_XI^+ = 0 Vrms, V_{CC} = 5.0 V_{DC} + 100 mVrms, f = 0 kHz – 50 kHz	40	–	–	dBp
$NPSR_X$	Negative Power Supply Rejection, Transmit VF_XI^+ = 0 Vrms, V_{BB} = – 0.5 V_{DC} + 100 mVrms, f = 0 kHz – 50 kHz	40	–	–	dBp
$PPSR_R$	Positive Power Supply Rejection, Receive (PCM code equals positive zero, V_{CC} = 5.0 V_{DC} + 100 mVrms)				
	f = 0 Hz – 4000 Hz	40	–	–	dBp
	f = 4 kHz – 25 kHz	40	–	–	dB
	f = 25 kHz – 50 KHZ	36	–	–	dB
$NPSR_R$	Negative Power Supply Rejection, Receive (PCM code equals positive zero, V_{BB} = – 5.0 V_{DC} + 100 mVrms)				
	f = 0 Hz – 4000 Hz	40	–	–	dBp
	f = 4 kHz – 25 kHz	40	–	–	dB
	f = 25 kHz – 50 kHz	36	–	–	dB

TRANSMISSION CHARACTERISTICS (continued)

Symbol	Parameter	Min.	Typ.	Max.	Unit
SOS	Spurious out-of band signals at the channel output. Loop around measurement, 0 dBm0, 300 Hz – 3400 Hz input applied to VF_XI^+, measure individual image signals at VF_R0				dB
	4600 Hz – 7600 Hz	–	–	– 32	
	7600 Hz – 8400 Hz	–	–	– 40	
	8400 Hz – 100,000 Hz	–	–	– 30	

DISTORTION

Symbol	Parameter		Min.	Typ.	Max.	Unit
STD_X or STD_R	Signal to Total Distortion (sinusoidal test method) Transmit or Receive Half-channel					dBp
	Level = 3 dBm0		33	–	–	
	= 0 dBm0 to – 30 dBm0		36	–	–	
	= – 40 dBm0	XMT	29	–	–	
		RCV	30	–	–	
	= – 55 dBm0	XMT	14	–	–	
		RCV	15	–	–	
SFD_X	Single Frequency Distortion, Transmit		–	–	– 46	dB
SFD_R	Single Frequency Distortion, Receive		–	–	– 46	dB
IMD	Intermodulation Distortion Loop Around Measurement, VF_XI^+ = – 4 dBm0 to – 21 dBm0, Two Frequencies in the Range 300 Hz – 3400 Hz		–	–	– 41	dB

CROSSTALK

Symbol	Parameter	Min.	Typ.	Max.	Unit
CT_{X-R}	Transmit to Receive Crosstalk, 0 dBm0 Transmit Level f = 300 Hz – 3400 Hz, D_R = Steady PCM Mode	–	– 90	– 75	dB
CT_{R-X}	Receive to Transmit Crosstalk, 0 dBm0 Receive Level f = 300 Hz – 3400 Hz, VF_XI = 0 V	–	– 90	– 70 (note 2)	dB

Notes : 1. Measured by extrapolation of the S/N ratio result in the first segment of the encoder
2. CT_{R-X} is measured with a – 40 dBm0 activating signal applied at VF_XI^+.

ENCODING FORMAT AT DATA BUS OUTPUT

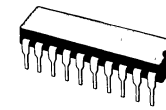
	TRUE A–Law, C5 = 0 (includes even bit inversion)							
	MSB							**LSB**
V_{IN} = + Full-scale	1	0	1	0	1	0	1	0
V_{IN} = 0 V	1	1	0	1	0	1	0	1
	0	1	0	1	0	1	0	1
V_{IN} = – Full-scale	0	0	1	0	1	0	1	0
	SIGN + MAGNITUDE A–LAW, C_5 = 1 (before even bit inversion)							
V_{IN} = + Full-scale	1	1	1	1	1	1	1	1
V_{IN} = 0 V	1	0	0	0	0	0	0	0
	0	0	0	0	0	0	0	0
V_{IN} = – Full-scale	0	1	1	1	1	1	1	1

SGS-THOMSON MICROELECTRONICS

ETC5067
ETC5064

SERIAL INTERFACE CODEC/FILTER WITH RECEIVE POWER AMPLIFIER

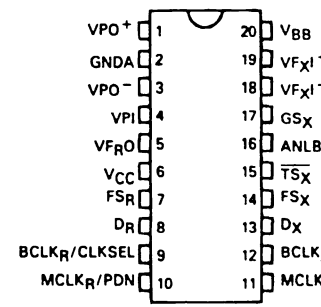
- COMPLETE CODEC AND FILTERING SYSTEM INCLUDING :
  - Transmit high-pass and low-pass filtering
  - Receive low-pass filter with sin x/x correction
  - Active RC noise filters
  - μ-law or A-law compatible COder and DECoder
  - Internal precision voltage reference
  - Serial I/O interface
  - Internal auto-zero circuitry
  - Receive push-pull power amplifiers
- μ -LAW ETC5064
- A-LAW ETC5067
- MEETS OR EXCEEDS ALL D3/D4 AND CCITT SPECIFICATIONS
- ± 5 V OPERATION
- LOW OPERATING POWER - TYPICALLY 70 mW
- POWER-DOWN STANDBY MODE - TYPICALLY 3 mW
- AUTOMATIC POWER-DOWN
- TTL OR CMOS COMPATIBLE DIGITAL INTERFACES
- MAXIMIZES LINE INTERFACE CARD CIRCUIT DENSITY



DIP20
(Ceramic) J
(Plastic) N

ORDER CODES : ETC5067J
ETC5064J
ETC5067N
ETC5064N

PIN CONNECTIONS



DESCRIPTION

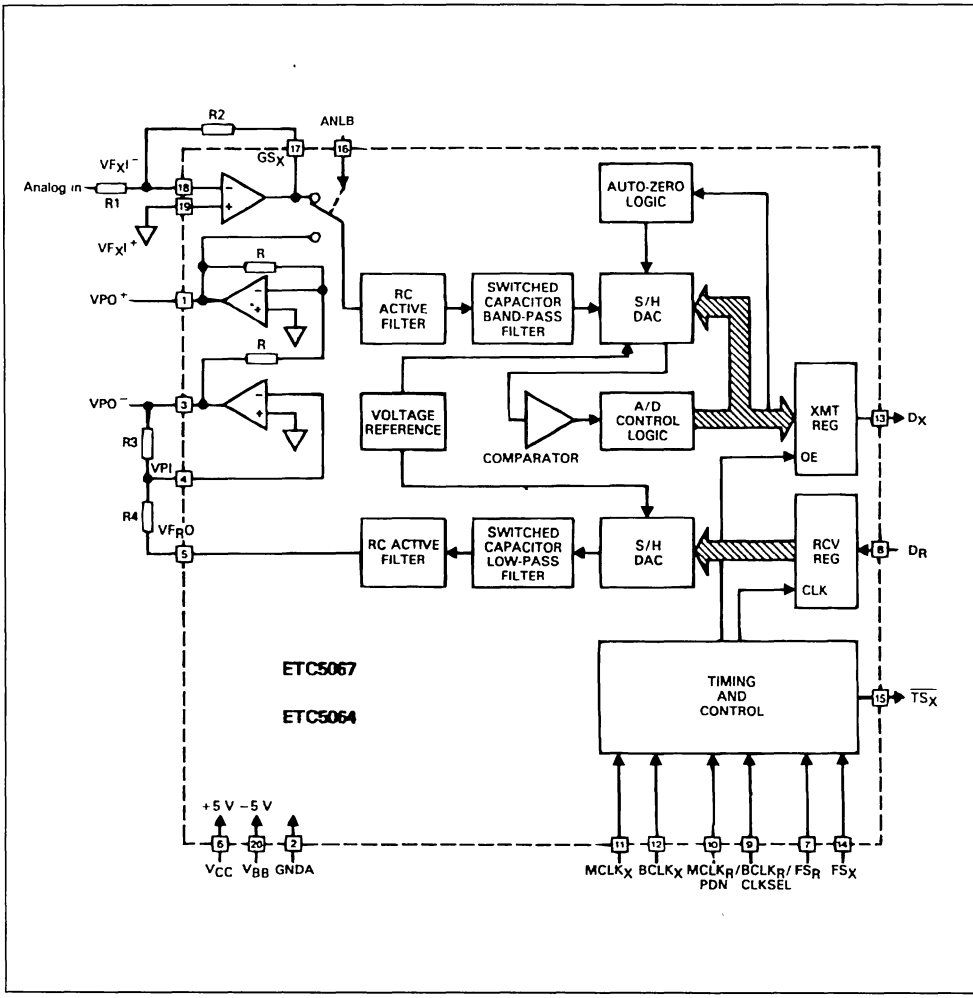
The ETC5064 (μ-law) and ETC5067 (A-law) are monolithic PCM CODEC/FILTERS utilizing the A/D and D/A conversion architecture shown in figure 1, and a serial PCM interface.

The devices are fabricated using double poly CMOS process.

Similar to the ETC505X family, these devices feature an additional Receive Power Amplifier to provide push-pull balanced output drive capability. The receive gain can be adjusted by means of two external resistors for an output level of up to ± 6.6 V across a balanced 600 Ω load.

Also included is an Analog Loopback switch and $\overline{TS_X}$ output.

Figure 1 : Block Diagram.



PIN DESCRIPTION

Name	Pin Type*	N°	Description
VPO^+	O	1	The Non-inverting Output of the Receive Power Amplifier
GNDA	GND	2	Analog Ground. All signals are referenced to this pin.
VPO^-	O	3	The Inverting Output of the Receive Power Amplifier
VPI	I	4	Inverting Input to the Receive Power Amplifier. Also powers down both amplifiers when connected to V_{BB}.
VF_RO	O	5	Analog Output of the Receive Filter.
V_{CC}	S	6	Positive Power Supply Pin. $V_{CC} = +5\ V \pm 5\ \%$
FS_R	I	7	Receive Frame Sync Pulse which enable $BCLK_R$ to shift PCM data into D_R. FS_R is an 8 kHz pulse train. See figures 2 and 3 for timing details.
D_R	I	8	Receive Data Input. PCM data is shifted into D_R following the FS_R leading edge.
$BCLK_R$/CLKSEL	I	9	The bit Clock which shifts data into D_R after the FS_R leading edge. May vary from 64 kHz to 2.048 MHz. Alternatively, may be a logic input which selects either 1.536 MHz/1.544 MHz or 2.048 MHz for master clock in synchronous mode and $BCLK_X$ is used for both transmit and receive directions (see table 1). This input has an internal pull-up.
$MCLK_R$/PDN	I	10	Receive Master Clock. Must be 1.536 MHz, 1.544 MHz or 2.048 MHz. May be asynchronous with $MCLK_X$, but should be synchronous with $MCLK_X$ for best performance. When $MCLK_R$ is connected continuously low, $MCLK_X$ is selected for all internal timing. When $MCLK_R$ is connected continuously high, the device is powered down.
$MCLK_X$	I	11	Transmit Master Clock. Must be 1.536 MHz, 1.544 MHz or 2.048 MHz. May be asynchronous with $MCLK_R$.
$BCLK_X$	I	12	The bit clock which shifts out the PCM data on D_X. May vary from 64 kHz to 2.048 MHz, but must be synchronous with $MCLK_X$.
D_X	O	13	The TRI-STATE® PCM data output which is enabled by FS_X.
FS_X	I	14	Transmit frame sync pulse input which enables $BCLK_X$ to shift out the PCM data on D_X. FS_X is an 8 kHz pulse train. See figures 2 and 3 for timing details.
$\overline{TS_X}$	O	15	Open drain output which pulses low during the encoder time slot. Must to be grounded if not used.
ANLB	I	16	Analog Loopback Control Input. Must be set to logic '0' for normal operation. When pulled to logic '1', the transmit filter input is disconnected from the output of the transmit preamplifier and connected to the VPO^+ output of the receive power amplifier. The input has an internal* pull down.
GS_X	O	17	Analog output of the transmit input amplifier. Used to set gain externally.
VF_XI^-	I	18	Inverting input of the transmit input amplifier.
VF_XI^+	I	19	Non-inverting input of the transmit input amplifier.
V_{BB}	S	20	Negative Power Supply Pin. $V_{BB} = -5\ V \pm 5\ \%$

* I : Input, O : Output, S : Power Supply

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FUNCTIONAL DESCRIPTION

POWER-UP

When power is first applied, power-on reset circuitry initializes the COMBO and places it into the power-down mode. All non-essential circuits are deactivated and the D_X and VF_RO outputs are put in high impedance states. To power-up the device, a logical low level or clock must be applied to the $MCLK_R$/PDN pin and FS_X and/or FS_R pulses must be present. Thus, 2 power-down control modes are available. The first is to pull the $MCLK_R$/PDN pin high ; the alternative is to hold both FS_X and FS_R inputs continuously low. The device will power-down approximately 2 ms after the last FS_X or FS_R pulse. Power-up will occur on the first FS_X or FS_R pulse. The TRI-STATE PCM data output, D_X, will remain in the high impedance state until the second FS_X pulse.

SYNCHRONOUS OPERATION

For synchronous operation, the same master clock and bit clock should be used for both the transmit and receive directions. In this mode, a clock must be applied to $MCLK_X$ and the $MCLK_R$/PDN pin can be used as a power-down control. A low level on $MCLK_R$/PDN powers up the device and a high level powers down the device. In either case, $MCLK_X$ will be selected as the master clock for both the transmit and receive circuits. A bit clock must also be applied to $BCLK_X$ and the $BCLK_R$/CLKSEL can be used to select the proper internal divider for a master clock of 1.536 MHz, 1.544 MHz or 2.048 MHz. For 1.544 MHz operation, the device automatically compensates for the 193 rd clock pulse each frame.

With a fixed level on the $BCLK_R$/CLKSEL pin, $BCLK_X$ will be selected as the bit clock for both the transmit and receive directions. Table 1 indicates the frequencies of operation which can be selected, depending on the state of $BCLK_R$/CLKSEL. In this synchronous mode, the bit clock, $BCLK_X$, may be from 64 KHz to 2.048 MHz, but must be synchronous with $MCLK_X$.

Table 1: Selection of Master Clock Frequencies.

$BCLK_R$/CLKSEL	Master Clock Frequency Selected	
	ETC 5067	ETC 5064
Clocked	2.048 MHz	1.536 MHz or 1.544 MHz
0	1.536 MHz or 1.544 MHz	2.048 MHz
1 (or open circuit)	2.048 MHz	1.536 MHz or 1.544 MHz

Each FS_X pulse begins the encoding cycle and the PCM data from the previous encode cycle is shifted out of the enabled D_X output on the positive edge of $BCLK_X$. After 8 bit clock periods, the TRI-STATE D_X output is returned to a high impedance state. With an FS_R pulse, PCM data is latched via the D_R input on the negative edge of $BCLK_X$ (or $BCLK_R$ if running). FS_X and FS_R must be synchronous with $MCLK_{X/R}$.

ASYNCHRONOUS OPERATION

For asynchronous operation, separate transmit and receive clocks may be applied. $MCLK_X$ and $MCLK_R$ must be 2.048 MHz for the ETC5067, or 1.536 MHz 1.544 MHz for the ETC5064, and need not be synchronous. For best transmission performance, however, $MCLK_R$ should be synchronous with $MCLK_X$, which is easily achieved by applying only static logic levels to the $MCLK_R$/PDN pin. This will automatically connect $MCLK_X$ to all internal $MCLK_R$ functions (see Pin Description). For 1.544 MHz operation, the device automatically compensates for the 193 rd clock pulse each frame. FS_X starts each encoding cycle and must be synchronous with $MCLK_X$ and $BCLK_X$. FS_R starts each decoding cycle and must be synchronous with $BCLK_R$. $BCLK_R$ must be a clock, the logic levels shown in Table 1 are not valid in asynchronous mode. $BCLK_X$ and $BCLK_R$ may operate from 64 KHz to 2.048 MHz.

SHORT FRAME SYNC OPERATION

The COMBO can utilize either a short frame sync pulse or a long frame sync pulse. Upon power initialization, the device assumes a short frame mode. In this mode, both frame sync pulses, FS_X and FS_R, must be one bit clock period long, with timing relationships specified in figure 3. With FS_X high during a falling edge of $BCLK_X$, the next rising edge of $BCLK_X$ enables the D_X TRI-STATE output buffer, which will output the sign bit. The following seven rising edges clock out the remaining seven bits, and the next falling edge disables the D_X output. With FS_R high during a falling edge of $BCLK_R$ ($BCLK_X$ in synchronous mode), the next falling edge of $BCLK_R$ latches in the sign bit. The following seven falling edges latch in the seven remaining bits. Both devices may utilize the short frame sync pulse in synchronous or asynchronous operating mode.

LONG FRAME SYNC OPERATION

To use the long frame mode, both the frame sync pulses, FS_X and FS_R, must be three or more bit clock periods long, with timing relationships specified in figure 4. Based on the transmit frame sync. FS_X, the

COMBO will sense whether short or long frame sync pulses are being used. For 64 KHz operation, the frame sync pulses must be kept low for a minimum of 160 ns (see fig. 2). The D_X TRI-STATE output buffer is enabled with the rising edge of FS_X or the rising edge of $BCLK_X$, whichever comes later, and the first bit clocked out is the sign bit. The following seven $BCLK_X$ rising edges clock out the remaining seven bits. The D_X output is disabled by the falling $BCLK_X$ edge following the eight rising edge, or by FS_X going low, whichever comes later. A rising edge on the receive frame sync pulse, FS_R, will cause the PCM data at D_R to be latched in on the next eight falling edges of $BCLK_R$ ($BCLK_X$ in synchronous mode). Both devices may utilize the long frame sync pulse in synchronous or asynchronous mode.

TRANSMIT SECTION

The transmit section input is an operational amplifier with provision for gain adjustment using two external resistors, see figure 5. The low noise and wide band-width allow gains in excess of 20 dB across the audio passband to be realized. The op amp drives a unity gain filter consisting of RC active prefilter, followed by an eighth order switched-capacitor bandpass filter clocked at 256 KHz. The output of this filter directly drives the encoder sample-and-hold circuit. The A/D is of companding type according to A-law (ETC5067) or μ-law (ETC5064) coding conventions. A precision voltage reference is trimmed in manufacturing to provide an input overload (t_{MAX}) of nominally 2.5 V peak (see table of Transmission Characteristics). The FS_X frame sync pulse controls the sampling of the filter output, and then the successive-approximation encoding cycle begins. The 8-bit code is then loaded into a buffer and shifted out through D_X at the next FS_X pulse. The total encoding delay will be approximately 165 μs (due to the transmit filter) plus 125 μs (due to encoding delay), which totals 290 μs. Any offset voltage due to the filters or comparator is cancelled by sign bit integration.

RECEIVE SECTION

The receive section consists of an expanding DAC which drives a fifth order switched-capacitor low pass filter clocked at 256 kHz. The decoder is A-law (ETC5067) or μ-law (ETC5064) and the 5 th order low pass filter corrects for the sin x/x attenuation due to the 8 kHz sample and hold. The filter is then followed by a 2 nd order RC active post-filter and power amplifier capable of driving a 600 Ω load to a level of 7.2 dBm. The receive section is unity-gain. Upon the occurence of FS_R, the data at the D_R input is clocked in on the falling edge of the next eight $BCLK_R$ ($BCLK_X$) periods. At the end of the decoder time slot, the decoding cycle begins, and 10 μs later the decoder DAC output is updated. The total decoder delay is ~ 10 μs (decoder update) plus 110 μs (filter delay) plus 62.5 μs (1/2 frame), which gives approximately 180 μs.

RECEIVE POWER AMPLIFIERS

Two inverting mode power amplifiers are provided for directly driving a matched line interface tranformer. The gain of the first power amplifier can be adjusted to boost the ± 2.5 V peak output signal from the receive filter up ± 3.3 V peak into an unbalanced 300 Ω load, or 4.0 V into an unbalanced 15 k load. The second power amplifier is internally connected in unity-gain inverting mode to give 6 dB of signal gain for balanced loads.

Maximum power transfer to a 600 Ω subscriber line termination is obtained by differentially driving a balanced transformer with a $\sqrt{2}$: 1 turns ratio, as shown in figure 5. A total peak power of 15.6 dBm can be delivered to the load plus termination.

Both power amplifiers can be powered down independently from the PDN input by connecting the VPI input to V_{BB}, saving approximately 12 mW of power.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	V_{CC} to GNDA	7	V
V_{BB}	V_{BB} to GNDA	– 7	V
V_{IN} V_{OUT}	Voltage at Any Analog Input or Output	V_{CC} + 0.3 to V_{BB} – 0.3	V
	Voltage at Any Digital Input or Output	V_{CC} + 0.3 to GNDA – 0.3	V
T_{oper}	Operating Temperature Range	– 25 to + 125	°C
T_{stg}	Storage Temeperature Range	– 65 to + 150	°C
	Lead Temperature (soldering, 10 seconds)	300	°C

ELECTRICAL OPERATING CHARACTERISTICS

V_{CC} = 5.0 V ± 5 %, V_{BB} = – 5 V ± 5 %, GNDA = 0 V, T_A = 0 °C to 70 °C (unless otherwise noted) ; Typical characteristics specified at V_{CC} = 5.0 V, V_{BB} = – 5.0 V, T_A = 25 °C ; all signals are referenced to GNDA.

DIGITAL INTERFACE

Symbol	Parameter		Min.	Typ.	Max.	Unit
V_{IL}	Input Low Voltage		–	–	0.6	V
V_{IH}	Input High Voltage		2.2	–	–	V
V_{OL}	Output Low Voltage					V
	I_L = 3.2 mA	D_X	–	–	0.4	
	I_L = 3.2 mA, Open Drain	$\overline{TS_X}$	–	–	0.4	
V_{OH}	Output High Voltage					V
	I_H = – 3.2 mA	D_X	2.4	–	–	
I_{IL}	Input Low Current (GNDA ≤ V_{IN} ≤ V_{IL}, all digital inputs, except $BCLK_R$)		– 10	–	10	µA
I_{IH}	Input High Current (V_{IH} ≤ V_{IN} ≤ V_{CC}) except ANLB		– 10	–	10	µA
I_{OZ}	Output Current in High Impedance State (TRI–STATE)					µA
	(GNDA ≤ V_0 ≤ V_{CC})	D_X	– 10	–	10	

ANALOG INTERFACE WITH TRANSMIT INPUT AMPLIFIER (all devices)

Symbol	Parameter		Min.	Typ.	Max.	Unit
I_IXA	Input Leakage Current (– 2.5 V ≤ V ≤ + 2.5 V)	VF_XI^+ or VF_XI^-	– 200	–	200	nA
R_IXA	Input Resistance (– 2.5 ≤ V ≤ + 2.5 V)	VF_XI^+ or VF_XI^-	10	–	–	MΩ
R_OXA	Output Resistance (closed loop, unity gain)		–	1	3	Ω
R_LXA	Load Resistance	GS_X	10	–	–	kΩ
C_LXA	Load Capacitance	GS_X	–	–	50	pF
V_OXA	Output Dynamic Range (R_L ≥ 10 kΩ)	GS_X	± 2.8	–	–	V
A_VXA	Voltage Gain (VF_XI^+ to GS_X)		5000	–	–	V/V
F_UXA	Unity Gain Bandwidth		1	2	–	MHz
$V_{OS}XA$	Offset Voltage		– 20	–	20	mV
$V_{CM}XA$	Common-mode Voltage		– 2.5	–	2.5	V
CMRRXA	Common-mode Rejection Ratio		60	–	–	dB
PSRRXA	Power Supply Rejection Ratio		60	–	–	dB

ANALOG INTERFACE WITH RECEIVE FILTER (all devices)

Symbol	Parameter		Min.	Typ.	Max.	Unit
R_ORF	Output Resistance	VF_RO	–	1	3	Ω
R_LRF	Load Resistance (VF_RO + ± 2.5 V)		10	–	–	kΩ
C_LRF	Load Capacitance		–	–	25	pF
VOS_RO	Output DC Offset Voltage		– 200	–	200	mV

ELECTRICAL OPERATING CHARACTERISTICS (continued)

ANALOG INTERFACE WITH POWER AMPLIFIERS (all devices)

Symbol	Parameter	Min.	Typ.	Max.	Unit
IPI	Input Leakage Current (– 1.0 V ≤ VPI ≤ 1.0 V)	– 100	–	100	nA
RIPI	Input Resistance (– 1.0 V ≤ VPI ≤ 1.0 V)	10	–	–	MΩ
VIOS	Input Offset vOltage	– 25	–	– 25	mV
ROP	Output Resistance (inverting unity-gain at VPO $^+$ or VPO $^-$)	–	1	–	Ω
F_C	Unity-gain Bandwidth, Open Loop (VPO $^-$)	–	400	–	kHz
C_LP	Load Capacitance (VPO $^+$ or VPO $^-$ to GNDA) $R_L \geq 1500\ \Omega$ $R_L = 600\ \Omega$ $R_L = 300\ \Omega$	 – – –	 – – –	 100 500 1000	pF
GAp $^+$	Gain VPO $^-$ to VPO $^+$ to GNDA, Level at VPO $^-$ = 1.77 Vrms (+ 3 dBm0)	–	– 1	–	V/V
$PSRR_P$	Power Supply Rejection of V_{CC} or V_{BB} (VPO $^-$ connected to VPI) 0 kHz – 4 kHz 0 kHz – 50 kHz	 60 36	 – –	 – –	dB

POWER DISSIPATION (all devices)

Symbol	Parameter	Min.	Typ.	Max.	Unit
$I_{CC}0$	Power-down Current	–	0.5	1.5	mA
$I_{BB}0$	Power-down Current	–	0.05	0.3	mA
$I_{CC}1$	Active Current	–	7.0	10.0	mA
$I_{BB}1$	Active Current	–	7.0	10.0	mA

ALL TIMING SPECIFICATIONS

Symbol	Parameter		Min.	Typ.	Max.	Unit
$1/t_{PM}$	Frequency of Master Clocks $MCLK_X$ and $MCLK_R$ Depends on the device used and the $BCLK_R$/CLKSEL pin.		– – –	1.536 2.048 1.544	– – –	MHz
t_{WMH}	Width of Master Clock High	$MCLK_X$ and $MCLK_R$	160	–	–	ns
t_{WML}	Width of Master Clock Low	$MCLK_X$ and $MCLK_R$	160	–	–	ns
t_{RM}	Rise Time of Master Clock	$MCLK_X$ and $MCLK_R$	–	–	50	ns
t_{FM}	Fall Time of Master Clock	$MCLK_X$ and $MCLK_R$	–	–	50	ns
t_{PB}	Period of Bit Clock		485	488	15,725	ns
t_{WBH}	Width of Bit Clock High (V_{IH} = 2.2 V)		160	–	–	ns
t_{WBL}	Width of Bit Clock Low (V_{IL} = 0.6 V)		160	–	–	ns
t_{RB}	Rise Time of Bit Clock (t_{PB} = 488 ns)		–	–	50	ns
t_{FB}	Fall Time of Bit Clock (t_{PB} = 488 ns)		–	–	50	ns
t_{SBFM}	Set-up Time from $BCLK_X$ High to $MCKL_X$ Falling Edge (first bit clock after the leading edge of FS_X)		100	–	–	ns
t_{HBF}	Holding Time from Bit Clock Low to the Frame Sync (long frame only)		0	–	–	ns
t_{SFB}	Set-up Time from Frame Sync to Bit Clock Low (long frame only)		80	–	–	ns

Note : For short frame sync timing FS_X and FS_R must go high while their respective bit clocks are high.

ALL TIMING SPECIFICATIONS (continued)

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{HBFI}	Hold Time from 3rd Period of Bit Clock Low to Frame Sync (long frame only) FS_X or FS_R	100	–	–	ns
t_{DZF}	Delay time to valid data from FS_X or $BCLK_X$, whichever comes later and delay time from FS_X to data output disabled. (C_L = 0 pF to 150 pF)	20	–	165	ns
t_{DBD}	Delay Time from $BCLK_X$ High to Data Valid (Load = 150 pF plus 2 LSTTL loads)	0	–	150	ns
t_{DZC}	Delay Time from $BCLK_X$ Low to Data Output Disabled	50	–	165	ns
t_{SDB}	Set-up Time from D_R Valid to $BCLK_{R/X}$ Low	50	–	–	ns
t_{HBD}	Hold Time from $BCLK_{R/X}$ Low to D_R Invalid	50	–	–	ns
t_{HOLD}	Holding Time from Bit Clock High to Frame Sync (short frame only)	0	–	–	ns
t_{SF}	Set-up Time from $FS_{X/R}$ to $BCLK_{X/R}$ Low (short frame sync pulse) - Note 1	80	–	–	ns
t_{HF}	Hold Time from $BCLK_{X/R}$ Low to $FS_{X/R}$ Low (short frame sync pulse) - Note 1	100	–	–	ns
t_{XDP}	Delay Time TS_X Low (load = 150 pF plus 2 LSTTL loads)	–	–	140	ns
t_{WFL}	Minimum Width of the Frame Sync Pulse (low level) (64 k bit/s operating mode)	160	–	–	ns

Note : 1. For short frame sync. timing FS_X and FS_R must go high while their respective bit clocks are high.

Figure 2 : 64 k bits/s TIMING DIAGRAM (see next page for complete timing).

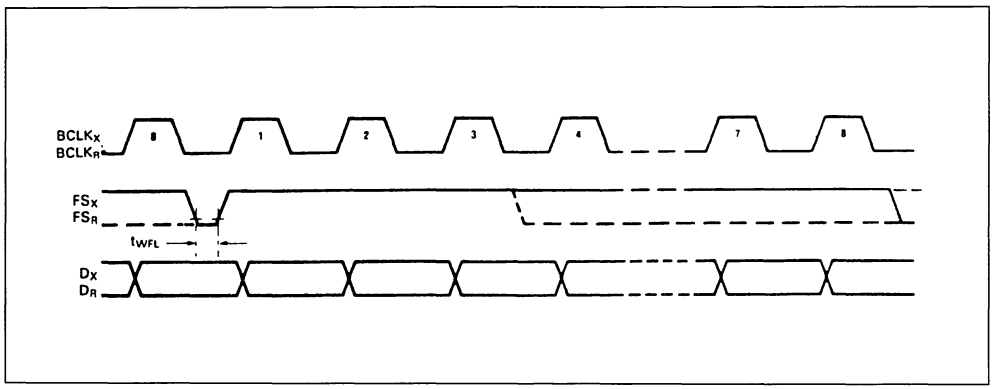


Figure 3 : Short Frame Sync Timing.

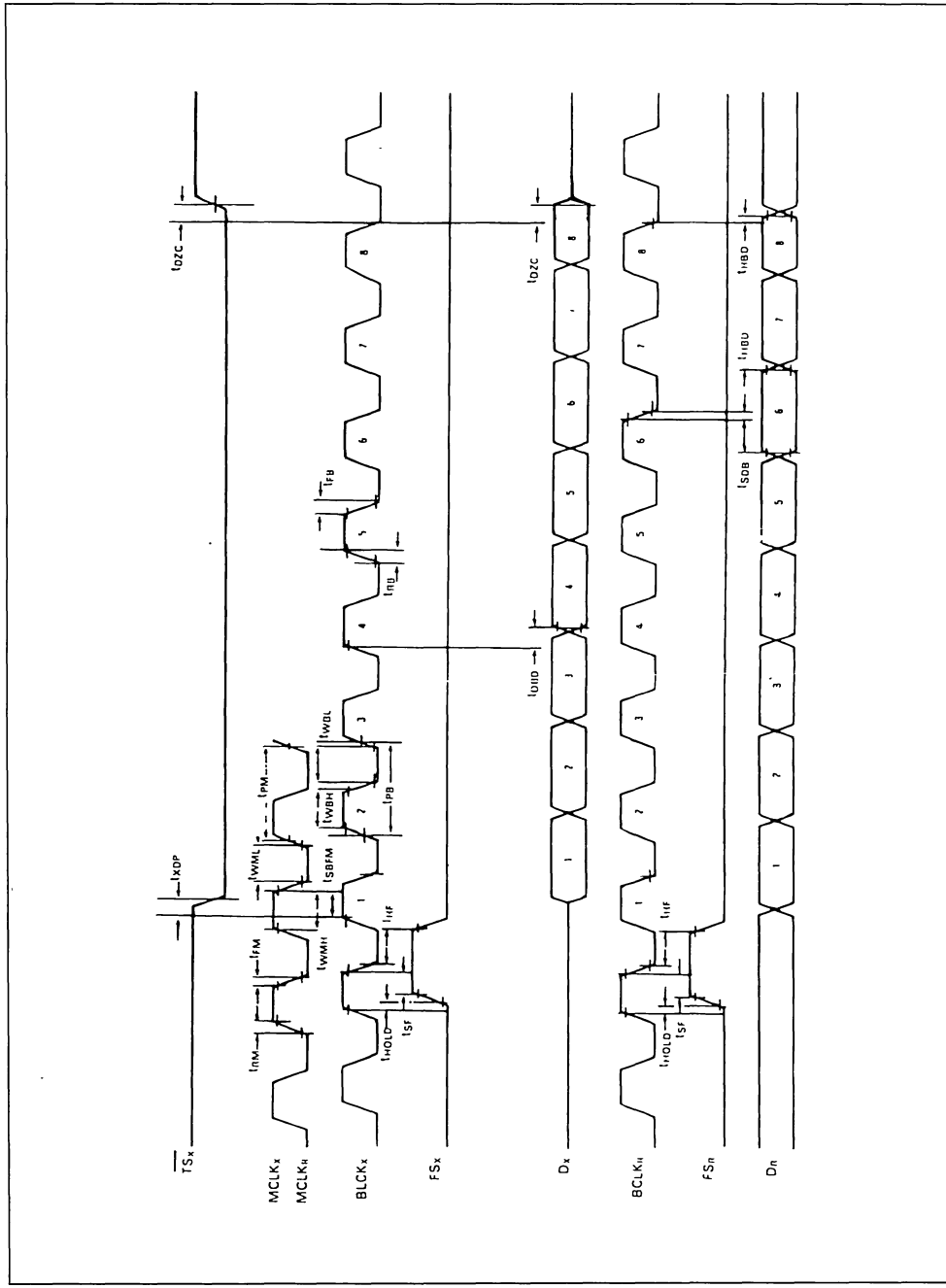
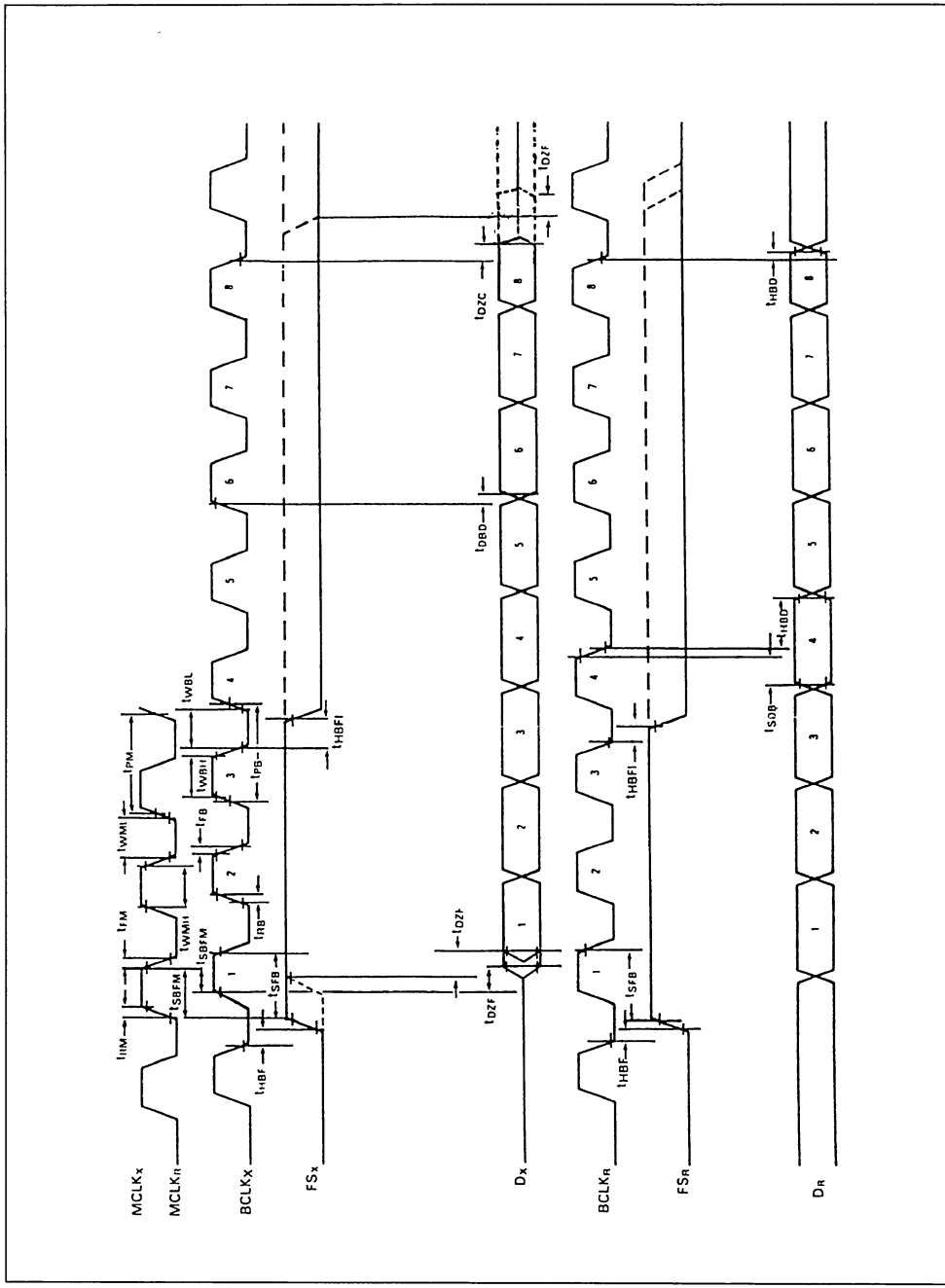


Figure 4 : Long Frame Sync Timing.



TRANSMISSION CHARACTERISTICS

(all devices) T_A = 0 °C to 70 °C, V_{CC} = 5 V ± 5 %, V_{BB} = – 5 V ± 5 %,GNDA = 0 v, f = 1.02 kHz, V_{IN} = 0 dBm0 transmit input amplifier connected for unity-gain non-inverting (unless otherwise specified).

AMPLITUDE RESPONSE

Symbol	Parameter	Min.	Typ.	Max.	Unit
	Absolute Levels – Nominal 0 dBm0 level is 4 dBm (600 Ω). 0 dBm0	– –	 1.2276	 –	V_{rms}
t_{MAX}	Max Overload Level 3.14 dBm0 ETC5067 3.17 dBm0 ETC5064	 – –	 2.492 2.501	 – –	V_{PK}
G_{XA}	Transmit Gain, Absolute (T_A = 25 °C, V_{CC} = 5 V, V_{BB} = – 5 V) Input at GS_X = 0 dBm0 at 1020 Hz	 – 0.15	 –	 0.15	dB
G_{XR}	Transmit Gain, Relative to G_{XA} f = 16 Hz f = 50 Hz f = 60 Hz f = 180 Hz f = 200 Hz f = 300 Hz – 3000 Hz f = 3300 Hz f = 3400 Hz f = 4000 Hz f = 4600 Hz and up, measure response from O Hz to 4000 Hz	 – – – – 2.8 – 1.8 – 0.15 – 0.35 – 0.7 – –	 – – – – – – – – – –	 – 40 – 30 – 26 – 0.2 – 0.1 0.15 0.05 0 – 14 – 32	dB
G_{XAT}	Absolute Transmit Gain Variation with Temperature (T_A = 0 °C to + 70 °C)	 – 0.1	 –	 0.1	dB
G_{XAV}	Absolute Transmit Gain Variation with Supply Voltage (V_{CC} = 5 V ± 5 %, V_{BB} = – 5 V ± 5 %)	 – 0.05	 –	 0.05	dB
G_{XRL}	Transmit Gain Variations with Level Sinusoidal Test Method Reference Level = – 10 dBm0 VF_XI^+ = – 40 dBm0 to + 3 dBm0 VF_XI^+ = – 50 dBm0 to – 40 dBm0 VF_XI^+ = – 55 dBm0 to – 50 dBm0	 – 0.2 – 0.4 – 1.2	 – – –	 0.2 0.4 1.2	dB
G_{RA}	Receive Gain, Absolute (T_A = 25 °C, V_{CC} = 5 V, V_{BB} = – 5 V) Input = Digital Code Sequence for 0 dBm0 Signal at 1020 Hz	– 0.15	–	0.15	dB
G_{RR}	Receive Gain, Relative to G_{RA} f= 0 Hz to 3000 Hz f = 3300 Hz f = 3400 Hz f = 4000 Hz	 – 0.15 – 0.35 – 0.7 –	 – – – –	 0.15 0.05 0 – 14	dB
G_{RAT}	Absolute Receive Gain Variation with Temperature (T_A = 0 °C to + 70 °C)	 – 0.1	 –	 0.1	dB
G_{RAV}	Absolute Receive Gain Variation with Supply Voltage (V_{CC} = 5 V ± 5 %, V_{BB} = – 5 V ± 5 %)	 – 0.05	 –	 0.05	dB
G_{RRL}	Receive Gain Variations with Level Sinusoidal Test Method ; Reference input PCM code corresponds to an ideally encoded – 10 dBm0 signal PCM level = – 40 dBm0 to + 3 dBm0 PCM level = – 50 dBm0 to – 40 dBm0 PCM level = – 55 dBm0 to – 50 dBm0	 – 0.2 – 0.4 – 1.2	 – – –	 0.2 0.4 1.2	dB
V_{RO}	Receive Filter Output at VF_RO R_L = 10 kΩ	– 2.5	–	2.5	V

TRANSMISSION CHARACTERISTICS (continued)

ENVELOPE DELAY DISTORTION WITH FREQUENCY

Symbol	Parameter	Min.	Typ.	Max.	Unit
D_{XA}	Transmit Delay, Absolute (f = 1600 Hz)	–	290	315	µs
D_{XR}	Transmit Delay, Relative to D_{XA}				µs
	f = 500 Hz – 600 Hz	–	195	220	
	f = 600 Hz – 800 Hz	–	120	145	
	f = 800 Hz – 1000 Hz	–	50	75	
	f = 1000 Hz – 1600 Hz	–	20	40	
	f = 1600 Hz – 2600 Hz	–	55	75	
	f = 2600 Hz – 2800 Hz	–	80	105	
	f = 2800 Hz – 3000 Hz	–	130	155	
D_{RA}	Receive Delay, Absolute (f = 1600 Hz)	–	180	200	µs
D_{RR}	Receive Delay, Relative to D_{RA}				µs
	f = 500 Hz – 1000 Hz	– 40	– 25	–	
	f = 1000 Hz – 1600 Hz	– 30	– 20	–	
	f = 1600 Hz – 2600 Hz	–	70	90	
	f = 2600 Hz – 2800 Hz	–	100	125	
	f = 2800 Hz – 3000 Hz	–	145	175	

NOISE

Symbol	Parameter	Min.	Typ.	Max.	Unit
N_{XP}	Transmit Noise, P Message Weighted (ETC5067, $VF_XI^+ = 0$ V)	–	– 74	– 69 (note 1)	dBm0p
N_{RP}	Receive Noise, P Message Weighted (ETC5067, PCM Code Equals Positive Zero)	–	– 82	– 79	dBm0p
N_{XC}	Transmit Noise, C Message Weighted (ETC5064, $VFXI^+ = 0$ V)	–	12	15	dBrnC0
N_{RC}	Receive Noise, C Message Weighted (ETC5064, PCM Code Equals Alternating Positive and Negative Zero)	–	8	11	dBrnC0
N_{RS}	Noise, Single Frequency f = 0 kHz to 100 kHz, Loop Around Measurement, $VF_XI^+ = 0$ Vrms	–	–	– 53	dBm0
$PPSR_X$	Positive Power Supply Rejection, Transmit $VF_XI^+ = 0$ Vrms, $V_{CC} = -5.0\ V_{DC} + 100$ mVrms, f = 0 kHz – 50 kHz	40	–	–	dBp
$NPSR_X$	Negative Power Supply Rejection, Transmit $VF_XI^+ = 0$ Vrms, $V_{BB} = -5.0\ V_{DC} + 100$ mVrms, f = 0 kHz – 50 kHz	40	–	–	dBp
$PPSR_R$	Positive Power Supply Rejection, Receive (PCM code equals positive zero, $V_{CC} = 5.0\ V_{DC} + 100$ mVrms)				
	f = 0 Hz – 4000 Hz	40	–	–	dBp
	f = 4 kHz – 25 kHz	40	–	–	dB
	f = 25 kHz – 50 KHZ	36	–	–	dB
$NPSR_R$	Negative Power Supply Rejection, Receive (PCM code equals positive zero, $V_{BB} = -5.0\ V_{DC} + 100$ mVrms)				
	f = 0 Hz – 4000 Hz	40	–	–	dBp
	f = 4 kHz – 25 kHz	40	–	–	dB
	f = 25 kHz – 50 kHz	36	–	–	dB

TRANSMISSION CHARACTERISTICS (continued)

Symbol	Parameter	Min.	Typ.	Max.	Unit
SOS	Spurious out-of band signals at the channel output. Loop around measurement, 0 dBm0, 300 Hz – 3400 Hz input applied to VF_XI^+, measure individual image signals at VF_R0				dB
	4600 Hz – 7600 Hz	–	–	– 32	
	7600 Hz – 8400 Hz	–	–	– 40	
	8400 Hz – 100,000 Hz	–	–	– 32	

DISTORTION

Symbol	Parameter		Min.	Typ.	Max.	Unit
STD_X or STD_R	Signal to Total Distortion (sinusoidal test method) Transmit or Receive Half-channel					dBp
	Level = 3 dBm0		33	–	–	
	= 0 dBm0 to – 30 dBm0		36	–	–	
	= – 40 dBm0	XMT	29	–	–	
		RCV	30	–	–	
	= – 55 dBm0	XMT	14	–	–	
		RCV	15	–	–	
SFD_X	Single Frequency Distortion, Transmit		–	–	– 46	dB
SFD_R	Single Frequency Distortion, Receive		–	–	– 46	dB
IMD	Intermodulation Distortion Loop Around Measurement, VF_XI^+ = – 4 dBm0 to – 21 dBm0, Two Frequencies in the Range 300 Hz – 3400 Hz		–	–	– 41	dB

CROSSTALK

Symbol	Parameter	Min.	Typ.	Max.	Unit
CT_{X-R}	Transmit to Receive Crosstalk, 0 dBm0 Transmit Level f = 300 Hz – 3400 Hz, D_R = Steady PCM Mode	–	– 90	– 75	dB
CT_{R-X}	Receive to Transmit Crosstalk, 0 dBm0 Receive Level f = 300 Hz – 3400 Hz, VF_XI = 0 V	–	– 90	– 70 (note 2)	dB

POWER AMPLIFIERS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{OL}	Maximum 0 dBm0 level for better than ± 0.1 dB linearity over the range 10 dBm0 to + 3 dBm0 (balanced load, R_L connected between VPO^+ and VPO^-).				Vrms
	R_L = 600 Ω	3.3	–	–	
	R_L = 1200 Ω	3.5	–	–	
	R_L = 30 kΩ	4.0	–	–	
S/Dp	Signal/Distortion R_L = 600 Ω, 0 dBm0	50	–	–	dB

Notes : 1. Measured by extrapolation from the distortion test result
2. CT_{R-X} is measured with a – 40 dBm0 activating signal applied at VF_XI^+.

ENCODING FORMAT AT D_X OUTPUT

	A–Law (including even bit inversion)	μLaw
V_{IN} (at GS_X) = + Full-scale	10101010	10000000
V_{IN} (at GS_X) = 0 V	{11010101 01010101	{11111111 01111111
V_{IN} (at GS_X) = – Full-scale	00101010	00000000

APPLICATIONS INFORMATION

POWER SUPPLIES

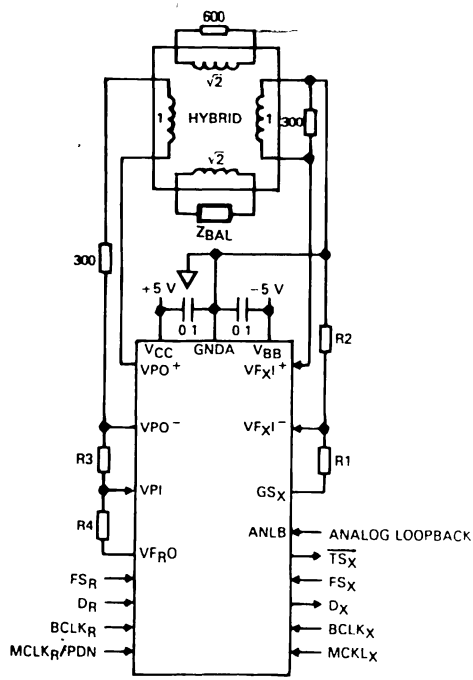
While the pins of the ETC5060 family are well protected against electrical misuse, it is recommended that the standard CMOS practice be followed, ensuring that ground is connected to the device before any other connections are made. In applications where the printed circuit board may be plugged into a "hot" socket with power and clocks already present, an extra long ground pin in the connector should be used.

All ground connections to each device should meet at a common point as close as possible to the GNDA pin. This minimizes the interaction of ground return currents flowing through a common bus impedance. 0.1 μF supply decoupling capacitors should be connected from this common ground point to V_{CC} and V_{BB} as close to the device as possible.

For best performance, the ground point of each CODEC/FILTER on a card should be connected to a common card ground in star formation, rather than via a ground bus. This common ground point should be decoupled to V_{CC} and V_{BB} with 10 μF capacitors.

For best performance either, $\overline{TS}_X$ should be grounded if not used.

Figure 5 : Typical Asynchronous Application.



Notes : 1. Transmit Gain = 20 x log $\left(\frac{R1 + R2}{R2}\right)$ (R1 + R2) ≥ 10 kΩ.

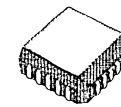
2. Receive gain = 20 x log $\left(\frac{2 \times R3}{R4}\right)$ R4 ≤ 10 kΩ.

SGS-THOMSON MICROELECTRONICS

ETC5064FN
ETC5067FN

SERIAL INTERFACE CODEC/FILTER WITH RECEIVE POWER AMPLIFIER

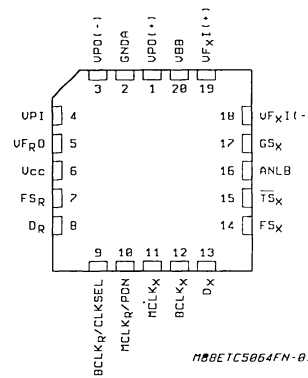
- COMPLETE CODEC AND FILTERING SYSTEM INCLUDING :
  - TRANSMIT HIGH-PASS AND LOW-PASS FILTERING
  - RECEIVE LOW-PASS FILTER WITH SIN X/X CORRECTION
  - ACTIVE RC NOISE FILTER
  - μ-LAW OR A-LAW COMPATIBLE CODER AND DECODER
  - INTERNAL PRECISION VOLTAGE REFERENCE
  - SERIAL I/O INTERFACE
  - INTERNAL AUTO-ZERO CIRCUITRY
  - RECEIVE PUSH-PULL POWER AMPLIFIERS
- μ-LAW 20 PINS ETC5064FN
- A-LAW 20 PINS ETC5067FN
- MEETS OR EXCEEDS ALL D3/D4 AND CCITT SPECIFICATIONS
- ± 5V OPERATION
- LOW OPERATING POWER-TYPICALLY 70mW
- POWER-DOWN STANDBY MODE-TYPICALLY 3mW
- AUTOMATIC POWER-DOWN
- TTL OR CMOS COMPATIBLE DIGITAL INTERFACES
- MAXIMIZES LINE INTERFACE CARD CIRCUIT DENSITY



PLCC20

ORDER CODES : ETC5064FN
ETC5067FN

PIN CONNECTION



DESCRIPTION

The ETC5064 (μ-law) and ETC5067 (A-law) are monolithic PCM CODEC/FILTERS utilizing the A/D and D/A conversion architecture shown in the block diagram below and a serial PCM interface. The devices are fabricated using double-poly CMOS process.

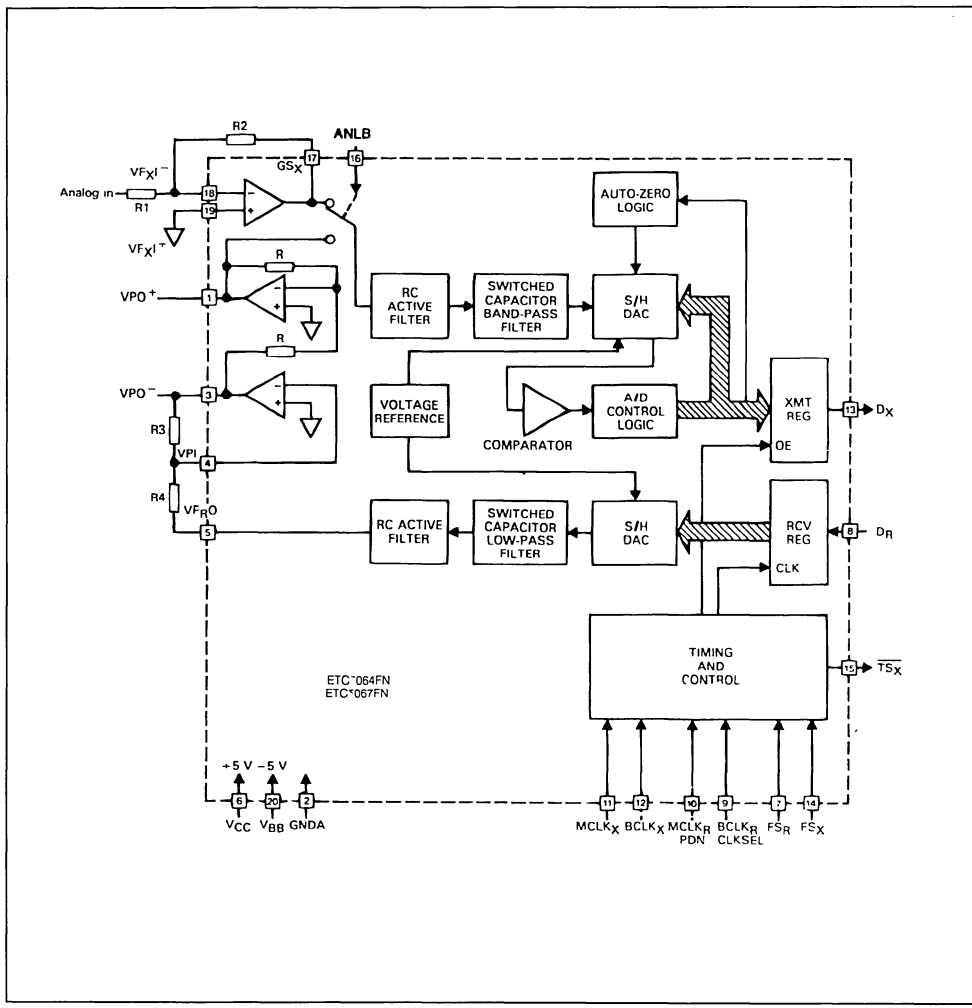
Similar to the ETC5050 family, these devices feature and additional Receive Power Amplifier to provide push-pull balanced output drive capability. The receive gain can be adjusted by means of two external resistors for an output level of up to ± 6.6V across a balanced 600Ω load.

Also included is an Analog Loopback switch and a $\overline{TS_X}$ output.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	V_{CC} to GNDA	7	V
V_{BB}	V_{BB} to GNDA	– 7	V
V_{IN}, V_{OUT}	Voltage at any Analog Input or Output	V_{CC} + 0.3 to V_{BB} – 0.3	V
	Voltage at Any Digital Input or Output	V_{CC} + 0.3 to GNDA – 0.3	V
T_{oper}	Operating Temperature Range	– 25 to + 125	°C
T_{stg}	Storage Temperature Range	– 65 to + 150	°C
	Lead Temperature (soldering 10 seconds)	300	°C

BLOCK DIAGRAM



PIN DESCRIPTION

Name	Pin Type	N°	Description
VPO+	O	1	The non-inverted Output of the receive power amplifier.
GNDA	GND	2	Analog Ground. All signal are referenced to this pin.
VPO–	O	3	The inverted output to the receive power amplifier.
VPI	I	4	Inverting input to the receive power amplifier. Also powers down both amplifiers when connected to V_{BB}.
VF_RO	O	5	Analog Output of the Receive Filter
V_{CC}	S	6	Positive Power Supply Pin. V_{CC} = + 5 V ± 5 %
FS_R	I	7	Receive frame sync pulse which enables $BCLK_R$ to shift PCM data into D_R. FS_R is an 8 kHz pulse train. See figures 1 and 2 for timing details.
D_R	I	8	Receive Data Input. PCM data is shifted into D_R following the FS_R leading edge.
$BCLK_R$/CLKSEL	I	9	The bit clock which shifts data into D_R after the FS_R leading edge. May vary from 64 kHz to 2.048 MHz. Alternatively, may be a logic input which selects either 1.536 MHz/1.544 MHz or 2.048 MHz for master clock in synchronous mode and $BCLK_X$ is used for both transmit and receive directions (see table I). This input has an internal pull–up.
$MCLK_R$/PDN	I	10	Receive Master Clock. Must be 1.536 MHz, 1.544 MHz or 2.048 MHz. May be asynchronous with $MCLK_X$, but should be synchronous with $MCLK_X$ for best performance. When $MCLK_R$ is connected continuously low, $MCLK_X$ is selected for all internal timing. When $MCLK_R$ is connected continuously high, the device is powered down.
$MCLK_X$	I	11	Transmit Master Clock. Must be 1.536 MHz, 1.544 MHz or 2.048 MHz. May be asynchronous with $MCLK_R$.
$BCLK_X$	I	12	The bit clock which shifts out the PCM data on D_X. May vary from 64 kHz to 2.048 MHz, but must be synchronous with $MCLK_X$.
D_X	O	13	The tri–state PCM data output which is enabled by FS_X.
FS_X	I	14	Transmit frame sync pulse input which enables $BCLK_X$ to shift out the PCM data on D_X.FS_X is an 8 kHz pulse train, see figures 1 and 2 timing details.
$\overline{TS_X}$	O	15	Open drain output which pulses low during the encoder time slot. Must to be grounded it not used.
ANLB	I	16	Analog Loopback Control Input. Must be set a logic '0' for normal operation. When pulled to logic '1', the transmit filter input is disconnected from the output of the transmit preamplifier and connected to theVPO + output of the receive power amplifier. This input has an internal pull–down.
GS_X	O	17	Analog Output of the Transmit Input Amplifier. Used to externally set gain.
VF_XI^-	I	18	Inverting Input of the Transmit Input Amplifier.
VF_XI^+	I	19	Non–inverting Input of the Transmit Input Amplifier.
V_{BB}	S	20	Negative Power Supply Pin. V_{BB} = – 5 V ± 5

* I : Input, O : Output, S : Power Supply

FUNCTIONAL DESCRIPTION

POWER-UP

When power is first applied, power-on reset circuitry initializes the COMBO and places it into the power-down mode. All non-essential circuits are deactivated and the D_X and VF_RO outputs are put in high impedance states. To power-up the device, a logical low level or clock must be applied to the $MCLK_R$/PDN pin and FS_X and/or FS_R pulses must be present. Thus, 2 power-down control modes are available. The first is to pull the $MCLK_R$/PDN pin high ; the alternative is to hold both FS_X and FS_R inputs continuously low. The device will power-down approximately 2ms after the last FS_X pulse. The TRI-STATE PCM data output, D_X, will remain in the high impedance state until the second FS_X pulse.

SYNCHRONOUS OPERATION

For synchronous operation, the same master clock and bit clock should be used for both the transmit and receive directions. In this mode, a clock must be applied to $MCLK_X$ and the $MCLK_R$/PDN pin can be used as a power-down control. A low level on $MCLK_R$/PDN powers up the device and a high level powers down the device. In either case, $MCLK_X$ will be selected as the master clock for both the transmit and receive circuits. A bit clock must also be applied to $BCLK_X$ and the BCL_R/CLKSEL can be used to select the proper internal divider for a master clock of 1.536MHz, 1.544MHz or 2.048MHz. For 1.544MHz operation, the device automatically compensates for the 193 rd clock pulse each frame.

With a fixed level on the $BCLK_R$/CKSEL pin, $BCLK_X$ will be selected as the bit clock for both the transmit and receive directions. Table 1 indicates the frequencies of operation which can be selected, depending on the state of $BCLK_R$/CLKSEL. In this synchronous mode, the bit clock, $BCLK_X$, may be from 64kHz to 2.048MHz, but must be synchronous with $MCLK_X$.

Table 1 : Selection of Master Clock Frequencies.

$BCLK_R$/CLKSEL	Master Clock Frequency Selected	
	ETC5067	ETC5064
Clocked	2.048 MHz	1.536 MHz or 1.544 MHz
0	1.536 MHz or 1.544 MHz	2.048 MHz
1 (or open circuit)	2.048 MHz	1.536 MHz or 1.544 MHz

Each FS_X pulse begins the encode cycle and the PCM data from the previous encode cycle is shift out of the enabled D_X output on the positive edge of $BCLK_X$. After 8 bit clock periods, the TRI-STATE D_X output is returned to a high impedance state. With an FS_R pulse, PCM data is latched via the D_R input the negative edge of $BCLK_X$ (or on $BCKL_R$ if running). FS_X and FS_R must be synchronized with $MCLK_{X/R}$.

ASYNCHRONOUS OPERATION

For asynchronous operation, separate transmit and receive clocks may be applied. $MCLK_X$ and $MCLK_R$ must be 2.048MHz for the ETC5067, or 1.536MHz, 1.544MHz for the ETC5064, and need not be synchronous. For best transmission performance, however, $MCLK_R$ should be synchronous with $MCLK_X$, which is easily achieved by applying only static logic levels to the $MCLK_R$/PDN pin. This will automatically connect $MCLK_X$ to all internal $MCLK_R$ functions (see pin description). For 1.544MHz operation, the device automatically compensates for the 193 rd clock pulse each frame. FS_X starts each encoding cycle and must be synchronous with $MCLK_X$ and $BCLK_X$. FS_R starts each decoding sycle and must be synchronous with $BCLK_R$. $BCLK_R$ must be a clock, the logic levels shown in Table 1 are not valid in asynchronous mode. $BCLK_X$ and $BCLK_R$ may operate from 64kHz to 2.048MHz.

SHORT FRAME SYNC OPERATION

The COMBO can utilize either a short frame sync pulse or a long frame sync pulse. Upon power initialization, the device assumes a short frame mode. In this mode, both frame sync pulses. FS_X and FS_R, must be one bit clock period long, with timing relationships specified in figure 3 with FS_R high during a falling edge of $BCLK_R$, the next rising edge of $BCLK_X$ enables the D_X TRI-STATE output buffer, which will output the sign bit. The following seven rising edges clock out the remaining seven bits, and the next falling edge disables the D_X output. With FS_R high during a falling edge of $BCLK_R$ ($BCLK_X$ in synchronous mode), the next falling edge of $BCLK_R$ latches in the sign bit. The following seven falling edges latch in the seven remaining bits. Both devices may utilize the short frame sync pulse in synchronous or asynchronous operating mode.

LONG FRAME SYNC OPERATION

To use the long frame mode, both the frame sync pulses, FS_X and FS_R, must be three or more bit clock periods long, with timing relationships specified in

figure 3. Based on the transmit frame sync FS_X, the COMBO will sense whether short or long frame sync pulses are being used. For 64kHz operation, the frame sync pulse must be kept low for a minimum of 160ns (see fig. 1). The D_X TRI-STATE output buffer is enabled with the rising edge of FS_X or the rising edge of $BCLK_X$, whichever comes later, and the first bit clocked out is the sign bit. The following seven BCLKX rising edges clock out the remaining seven bits. The D_X output is disabled by the falling $BCLK_X$ edge following the eighth rising edge, or by FS_X going low, whichever comes later. A rising edge on the receive frame sync pulse, FS_R, will cause the PCM data at D_R to be latched in on the next eight falling edges of $BCLK_R$ ($BCLK_X$ in synchronous mode). Both devices may utilize the long frame sync pulse in synchronous or asynchronous mode.

TRANSMIT SECTION

The transmit section input is an operational amplifier with provision for gain adjustment using two external resistors, see figure 4. The low noise and wide bandwidth allow gains in excess of 20dB across the audio passband to be realized. The op amp drives a unity gain filter consisting of RC active pre-filter, followed by an eighth order switched-capacitor bandpass filter clocked at 256kHz. The output of this filter directly drives the encoder sample-and-hold circuit. The A/D is of companding type according to A-law (ETC5067) or μ-law (ETC5064) coding conventions. A precision voltage reference is trimmed in manufacturing to provide an input overload (t_{MAX}) of nominally 2.5V peak (see table of Transmission Characteristics). The FS_X frame sync pulse controls the sampling of the filter output, and then the successive-approximation encoding cycle begins. The 8-bit code is then loaded into a buffer and shifted out through D_X at the next FS_X pulse. The total encoding delay will be approximately 165μs (due to the transmit filter) plus 125μs (due to encoding delay), which totals 290μs. Any offset voltage due to the filters or comparator is cancelled by sign bit integration.

RECEIVE SECTION

The receive section consist of an expanding DAC which drives a fifth order switched-capacitor low pass filter clocked at 256kHz. The decoder is A-law (ETC5067) or μ–law (ETC5064) and the 5 th order low pass filter corrects for the sin x/x attenuation due to the 8kHz sample and hold. The filter is then followed by a 2 nd order RC active post-filter and power amplifier capable of driveing a 600Ω load to a level of 7.2dBm. The receive section is unity-gain. Upon the occurence of FS_R, the data at the DR input is clocked in on the falling edge of the next eight $BCLK_R$ ($BCKL_X$) periods. At the end of the decoder time slot, the decoding cycle begins, and 10μs later the decoder DAC output is updated. The total decoder delay is ~ 10μs (decoder up-date) plus 110μs (filter delay) plus 62.5μs (1/2 frame), which gives approximately 180μs.

RECEIVE POWER AMPLIFIERS

Two inverting mode power amplifiers are provided for directly driving a matched line interface transformer. The gain of the first power amplifier can be adjusted to boost the ± 2.5V peak output signal from the receive filter up ± 3.3V peak into an unbalanced 300Ω load, or ± 4.0V into an unbalanced 15kΩ load. The second power amplifier is internally connected in unity-gain inverting mode to give 6dB of signal gain for balanced loads. Maximum power transfer to a 600Ω subscriber line termination is obtained by differentially driving a balanced transformer with a $\sqrt{2}$: 1 turns ratio, as shown in figure 4. A total peak power of 15.6dBm can be delivered to the load plus termination. Both power amplifier can be powered down independently from the PDN input by connecting the VPI input to V_{BB} saving approximately 12mW of power.

ELECTRICAL OPERATING CHARACTERISTICS V_{CC} = 5.0 V ± 5 %, V_{BB} = – 5%, GNDA = 0 V, T_A = 0 °C to 70 °C (unless otherwise noted) ; typical characteristics specified at V_{CC} = 5.0V, V_{BB} = – 5.0V, T_A = 25 °C ; all signals are referenced to GNDA.

DIGITAL INTERFACE (all devices)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{IL}	Input Low Voltage			0.6	V
V_{IH}	Input High Voltage	2.2			V
V_{OL}	Output Low Voltage I_L = 3.2 mA D_X I_L = 3.2 mA, Open Drain $\overline{TS_X}$			0.4 0.4	V
V_{OH}	Output High Voltage I_H = 3.2 mA D_X	2.4			V
I_{IL}	Input Low Current (GNDA ≤ V_{IN} ≤ V_{IL}) all Digital Inputs Except $BCLK_R$	– 10		10	µA
I_{IH}	Input High Current (V_{IH} ≤ V_{IN} ≤ V_{CC}) Except ANLB	– 10		10	µA
I_{OZ}	Output Current in High Impedance State (TRI-STATE) (D_X GNDA ≤ V_O ≤ V_{CC})	– 10		10	µA

ANALOG INTERFACE WITH TRANSMIT INPUT AMPLIFIER (all devices)

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_IXA	Input Leakage Current ($VFxI^+$ or $VFxI^-$) (– 2.5 V ≤ V ≤ + 2.5 V)	– 200		200	nA
R_IXA	Input Resistance (VF_XI^+ or VF_XI^-) (– 2.5 V ≤ V ≤ + 2.5 V)	10			MΩ
R_OXA	Output Resistance (closed loop, unity gain)		1	3	Ω
R_LXA	Load Resistance GS_X	10			kΩ
C_LXA	Load Capacitance GS_X			50	pF
V_OXA	Output Dynamic Range (R_L ≥ 10 kΩ) GS_X	– 2.8		+ 2.8	V
A_VXA	Voltage Gain (VF_XI^+ to GS_X)	5000			V/V
F_UXA	Unity Gain Bandwidth	1	2		MHz
$V_{OS}XA$	Offset Voltage	– 20		20	mV
$V_{CM}XA$	Common-mode Voltage	– 2.5		2.5	V
CMRRXA	Common-mode Rejection Ratio	60			dB
PSRRXA	Power Supply Rejection Ratio	60			dB

ANALOG INTERFACE WITH RECEIVE FILTER (all devices)

Symbol	Parameter	Min.	Typ.	Max.	Unit
R_ORF	Output Resistance VF_RO		1	3	Ω
R_LRF	Load Resistance (VF_RO = ± 2.5 V)	10			kΩ
C_LRF	Load Capacitance			25	pF
VOS_RO	Output DC Offset Voltage	– 200		200	mV

ANALOG INTERFACE WITH POWER AMPLIFIERS (all devices)

Symbol	Parameter	Min.	Typ.	Max.	Unit
IPI	Input Leakage Current (– 1.0 V ≤ VPI ≤ 1.0 V)	– 100		100	nA
RIPI	Input Resistance (– 1.0 ≤ VPI ≤ 1.0 V)	10			MΩ
VIOS	Input Offset Voltage	– 25		25	mV
ROP	Output Resistance (inverting unity–gain at VPO^+ or VPO^-)		1		Ω
F_C	Unity–gain Bandwidth, Open Loop (VPO^-)		400		kHz
C_LP	Load Capacitance (VPO^+ or VPO^- to GNDA) $R_L \geq 1500\ \Omega$ $R_L = 600\ \Omega$ $R_L = 300\ \Omega$			 100 500 1000	pF
GAp^+	Gain VPO^- to VPO^+ to GNDA, Level at $VPO^- = 1.77$ Vrms (+ 3 dBm0)		– 1		V/V
PSRRp	Power Supply Rejection of V_{CC} or V_{BB} (VPO^- connected to VPI) 0 kHz – 4 kHz 0 kHz – 50 kHz	 60 36			dB

POWER DISSIPATION (all devices)

Symbol	Parameter	Min.	Typ.	Max.	Unit
$I_{CC}0$	Power-down Current		0.5	1.5	mA
$I_{BB}0$	Power-down Current		0.05	0.3	mA
$I_{CC}1$	Active Current		7.0	10.0	mA
$I_{BB}1$	Active Current		7.0	10.0	mA

TIMING SPECIFICATIONS All timings parameters are measured at V_{OH} = 2.0 V and V_{OL} = 0.7 V.

Symbol	Parameter	Min.	Typ.	Max.	Unit
$1/t_{PM}$	Frequency of master clocks $MCLK_X$ and $MCLK_R$ Depends on the device used and the $BCLK_R$/CLKSEL Pin		1.536 1.544 2.048		MHz
t_{WMH}	Width of Master Clock High $MCLK_X$ and $MCLK_R$	160			ns
t_{WML}	Width of Master Clock Low $MCLK_X$ and $MCLK_R$	160			ns
t_{RM}	Rise Time of Master Clock $MCLK_X$ and $MCLK_R$			50	ns
t_{FM}	Fall Time of Master Clock $MCLK_X$ and $MCLK_R$			50	ns
t_{PB}	Period of Bit Clock	485	488	15.725	ns
t_{WBH}	Width of Bit Clock High (V_{IH} = 2.2 V)	160			ns
t_{WBL}	Width of Bit Clock Low (V_{IL} = 0.6 V)	160			ns
t_{RB}	Rise Time of Bit Clock (t_{PB} = 488 ns)			50	ns
t_{FB}	Fall Time of Bit Clock (t_{PB} = 488 ns)			50	ns
t_{SBFM}	Set-up time from $BCLK_X$ high to $MCLK_X$ falling edge. (first bit clock after the leading edge of FS_X)	100			ns
t_{HBF}	Holding Time from Bit Clock Low to the Frame Sync (long frame only)	0			ns
t_{SFB}	Set-up Time from Frame Sync to Bit Clock (long frame only)	80			ns
t_{HBFI}	Hold Time from 3rd Period of Bit Clock Low to Frame Sync (long frame only) FS_X or FS_R	100			ns
t_{DZF}	Delay Time to valid data from FS_X or $BCLK_X$, whichever comes later and delay time from FSX to data output disabled (C_L = 0 pF to 150 pF)	20		165	ns
t_{DBD}	Delay Time from $BCLK_X$ high to data valid (load = 150 pF plus 2 LSTTL loads)	0		180	ns
t_{DZC}	Delay Time from $BCLK_X$ low to data output disabled	50		165	ns
t_{SDB}	Set-up Time from D_R valid to $BCLK_{R/X}$ low	50			ns
t_{HBD}	Hold Time from $BCLK_{R/X}$ low to D_R invalid	50			ns
t_{HOLD}	Holding Time from Bit Clock High to Frame Sync (short frame only)	0			ns
t_{SF}	Set-up Time from $FS_{X/R}$ to $BCLK_{X/R}$ Low (short frame sync pulse) - Note 1	80			ns
t_{HF}	Hold Time from $BCLK_{X/R}$ Low to $FS_{X/R}$ Low (short frame sync pulse) - Note 1	100			ns
t_{XDP}	Delay Time to TS_X low (load = 150 pF plus 2 LSTTI loads)			140	ns
t_{WFL}	Minimum Width of the Frame Sync Pulse (low level) (64 bit/s operating mode)	160			ns

Note : 1.For short frame sync timing. FS_X and FS_R must go high while their respective bit clocks are high.

Figure 1 : 64 k bits/s TIMING DIAGRAM. (see next page for complete timing)

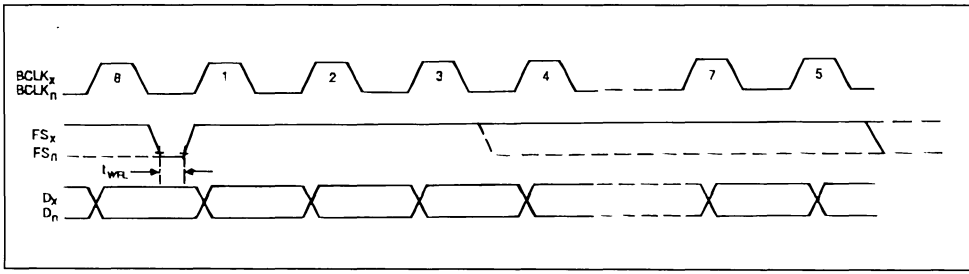


Figure 2 : Short Frame Sync Timing.

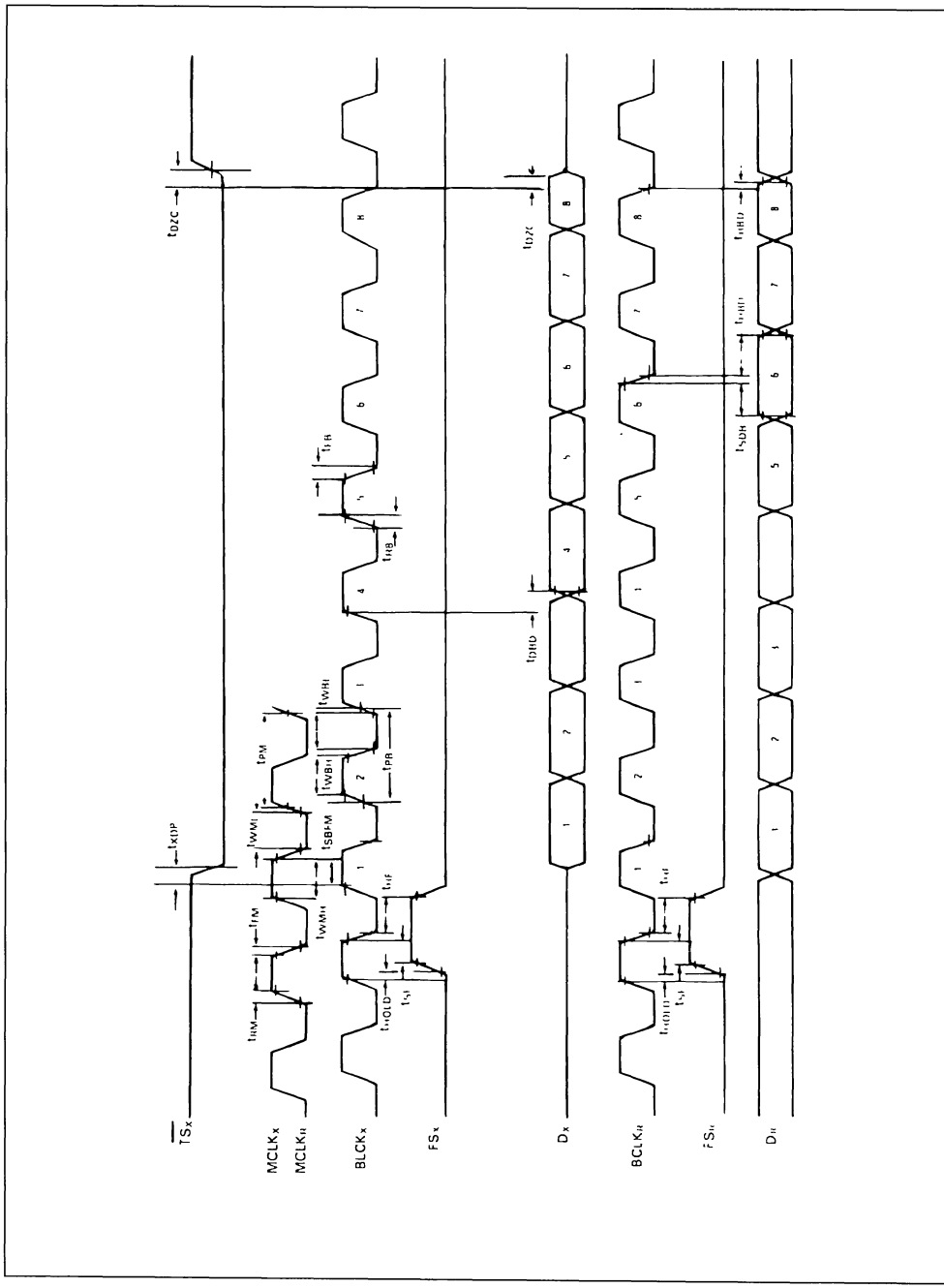
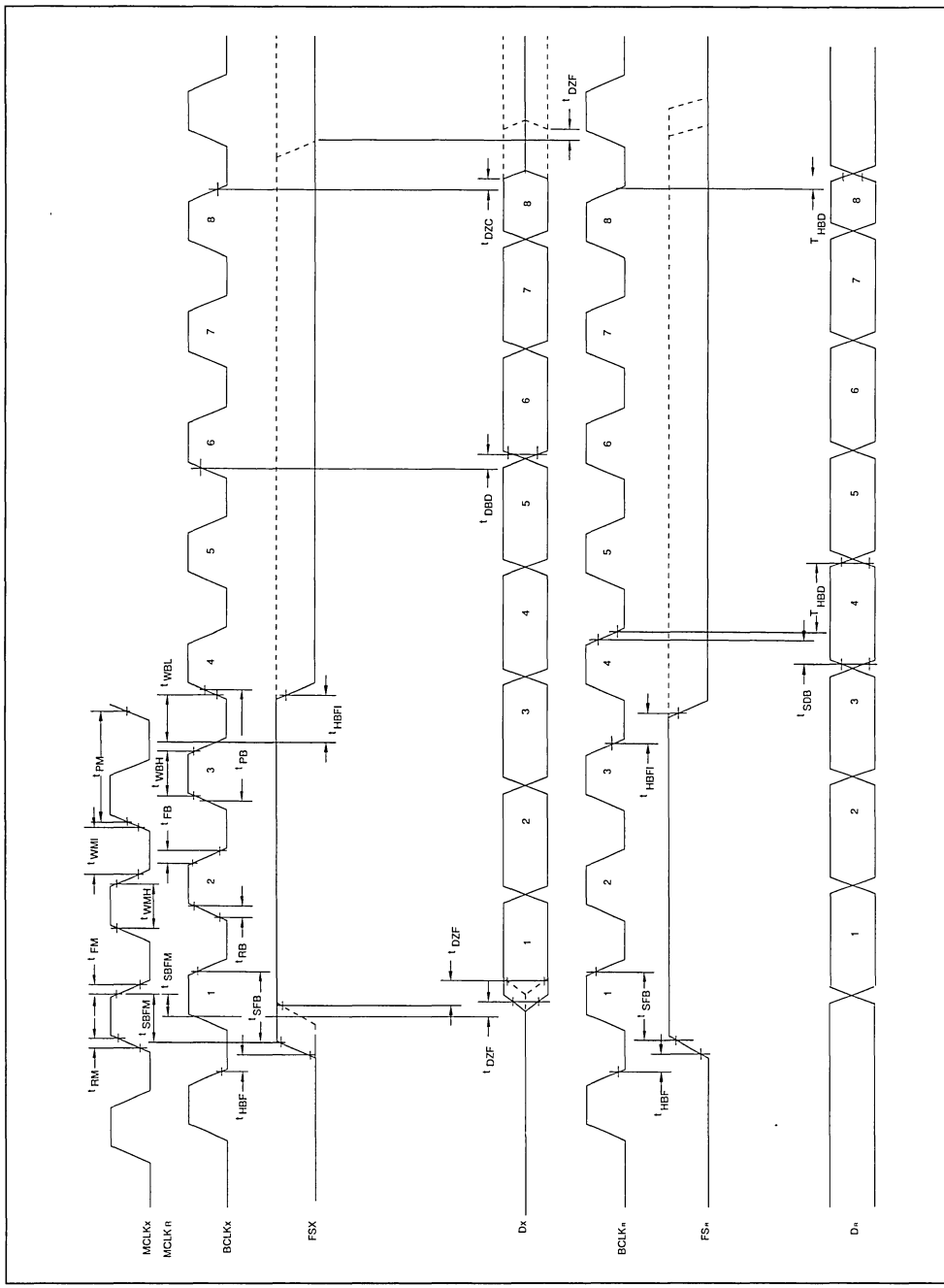


Figure 3 : Long Frame Sync Timing.



TRANSMISSION CHARACTERISTICS (all devices) T_A = 0°C to 70°C, V_{CC} = 5V ± 5%, V_{BB} = – 5V ± 5%, GNDA = 0V, f = 1.02kHz, V_{IN} = 0dBm0, transmit input amplifier connected for unity–gain non–inverting. (unless otherwise specified).

AMPLITUDE RESPONSE

Symbol	Parameter	Min.	Typ.	Max.	Unit
	Absolute levels - nominal 0 dBm0 level is 4 dBm (600 Ω) 0 dBm0		1.2276		Vrms
t_{MAX}	Max Overload Level 3.14 dBm0 ETC5067 3.17 dBm0 ETC5064		 2.492 2.501		V_{PK}
G_{XA}	Transmit Gain, Absolute (T_A = 25 °C, V_{CC} = 5 V, V_{BB} = – 5 V) Input at G_{SX} = 0 dBm0 at 1020 Hz	– 0.15		0.15	dB
G_{XR}	f = 16 Hz f = 50 Hz f = 60 Hz f = 200 Hz f = 300 Hz - 3000 Hz f = 3300 Hz f = 3400 Hz f = 4000 Hz f = 4600 Hz and up, Measure Reponse from 0 Hz to 4000 Hz	 – 1.8 – 0.15 – 0.35 – 0.7		– 40 – 30 – 26 – 0.1 0.15 0.05 0 – 14 – 32	dB
G_{XAT}	Absolute Transmit Gain Variation with Temperature (T_A = 0 °C to + 70 °C)	– 0.1		0.1	dB
G_{XAV}	Absolute Transmit Gain Variation with Supply Voltage (V_{CC} = 5 V ± 5 %, V_{BB} = – 5 V ± 5%)	– 0.05		0.05	dB
G_{XRL}	Transmit Gain Variation with Level Sinusoidal Test Method Reference Level = – 10 dBmO VF_XI^+ = – 40 dBm0 to + 3 dBm0 VF_XI^+ = – 50 dBm0 to – 40 dBm0 VF_XI^+ = – 55 dBm0 to – 50 dBm0	 – 0.2 – 0.4 – 1.2		 0.2 0.4 1.2	dB
G_{RA}	Receive Gain, Absolute (T_A = 25 °C, V_{CC} = 5 V, V_{BB} = – 5 V) Input = Digital Code Sequence for 0 dBM0 Signal at 1020 Hz	– 0.15		0.15	dB
G_{RR}	Receive Gain, Relative to G_{RA} f = 0 Hz to 3000 Hz f = 3300 Hz f = 3400 Hz f = 4000 Hz	 – 0.15 – 0.35 – 0.7		 0.15 0.05 0 – 14	dB
G_{RAT}	Absolute Receive Gain Variation with Temperature (T_A = 0 °C to + 70 °C)	– 0.1		0.1	dB
G_{RAV}	Absolute Receive Gain Variation with Supply Voltage (V_{CC} = 5 V ± 5 %, V_{BB} = – 5 v ± 5 %)	– 0.05		0.05	dB
G_{RRL}	Receive Gain Variation with Level Sinusuoidal test method ; reference input PCM code corresponds to an ideally encoded – 10 dBmO signal PCM Level = – 40 dBm0 to + 3 dBm0 PCM Level = – 50 dBm0 to – 40 dBm0 PCM Level = – 55 dBm0 to – 50 dBm0	 – 0.2 – 0.4 – 1.2		 0.2 0.4 1.2	dB
V_{RO}	Receive Filter Output at VR_RO R_L = 10 kΩ	– 2.5		2.5	V

TRANSMISSION CHARACTERISTICS (continued).

ENVELOPE DELAY DISTORTION WITH FREQUENCY

Symbol	Parameter	Min.	Typ.	Max.	Unit
D_{XA}	Transmit Delay, Absolute (f = 1600 Hz)		290	315	µs
D_{XR}	Transmit Delay, Relative to D_{XA}				
	f = 500 Hz-600 Hz		195	220	
	f = 600 Hz-800 Hz		120	145	
	f = 800 Hz-1000 Hz		50	75	
	f = 1000 Hz-1600 Hz		20	40	µs
	f = 1600 Hz-2600Hz		55	75	
	f = 2600 Hz-2800 Hz		80	105	
	f = 2800 Hz-3000 Hz		130	155	
D_{RA}	Receive Delay, Absolute (f = 1600 Hz)		180	200	µs
D_{RR}	Receive Delay, Relative to D_{RA}				
	f = 500 Hz-1000 Hz	− 40	− 25		
	f = 1000 Hz-1600 Hz	− 30	− 20		µs
	f = 1600 Hz-2600 Hz		70	90	
	f = 2600 Hz-2800 Hz		100	125	
	f = 2800 Hz-3000 Hz		145	175	

NOISE

Symbol	Parameter	Min.	Typ.	Max.	Unit
N_{XP}	Transmit Noise, P Message Weighted (ETC5067, VF_XI^+ = 0 V)		− 74	− 69 (note 1)	dBm0p
N_{RP}	Receive Noise, P Message Weighted (ETC5067, PCM code equals positive zero)		− 82	− 79	dBm0p
N_{XC}	Transmit Noise, C Message Weighted (ETC5064, $VFxI^+$ = 0 V)		12	15	dBrnC0
N_{RC}	Receive Noise, C Message Weighted (ETC5064, PCM Code Equals Alternating Positive and Negative Zero)		8	11	dBrnC0
N_{RS}	Noise, Single Frequency f = 0 kHz to 100 kHz, Loop around Measurement, VF_XI^+ = 0 V			− 53	dBm0
$PPSR_X$	Positive Power Supply Rejection, Transmit (note 2) V_{CC} = 5.0 V_{DC} + 100 mVrms, f = 0 kHz-50 kHz	40			dBp
$NPSR_X$	Negative Power Supply Rejection, Transmit (note 2) V_{BB} = 5.0 V_{DC} + 100 mVrms, f = 0 kHz-50 kHz	40			dBp
$PPSR_R$	Positive Power Supply Rejection, Receive (PCM code equals positive zero, V_{CC} = 5.0 V_{DC} + 100 mVrms)				
	f = 0 Hz-4000Hz 5067	40			dBp
	f = 4 kHz-25 kHz	40			dB
	f = 25 kHz-50 kHz	36			dB
$NPSR_R$	Negative Power Supply Rejection, Receive (PCM code equals positive zero, V_{BB} = − 5.0 V_{DC} + 100 mVrms)				
	f = 0 Hz-4000Hz 5067	40			dBp
	f = 4 kHz-25 kHz	40			dB
	f = 25 kHz-50 kHz	36			dB
SOS	Spurious out-of-band Signals at the Channel Output Loop around measurement, 0 dBm0, 300 Hz-3400 Hz input applied to D_R, measure individual image signals at D_X				
	4600 Hz-7600 Hz			− 32	
	7600 Hz-8400 Hz			− 40	
	8400 Hz-100,000 Hz			− 32	

TRANSMISSION CHARACTERISTICS (continued).

DISTORTION

Symbol	Parameter		Min.	Typ.	Max.	Unit
STD_X or STD_R	Signal to Total Distortion (sinusoidal test method) Transmit or Receive Half-channel					
	Level = 3.0 dBm0		33			dBp
	= 0 dBm0 to – 30 dBm0		36			
	= – 40 dBm0	XMT	29			
		RCV	30			
	= – 55 dBm0	XMT	14			
		RCV	15			
SFD_X	Single Frequency Distortion, Transmit				– 46	dB
SFD_R	Single Frequency Distortion, Receive				– 46	dB
IMD	Intermodulation Distortion Loop Around Measurement, VF_XI^+ = – 4 dBm0 to – 21 dBm0, two Frequencies in the Range 300 Hz-3400 Hz				– 41	dB

CROSSTALK

Symbol	Parameter	Min.	Typ.	Max.	Unit
CT_{X-R}	Transmit to Receive Crosstalk, 0dBm0 Transmit f = 300 Hz-3400 Hz, D_R = Steady PCM Code		– 90	– 75	dB
CT_{R-X}	Receive to Transmit Crosstalk, 0dBm0 Receive Level f = 300 Hz-3400 Hz, VF_XI = 0 V		– 90	– 70 (note 2)	dB

POWER AMPLIFIERS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{OL}	Maximum 0 dBm0 Level for Better than ± 0.1 dB Linearity Over the Range 10 dBm0 to + 3 dBm0 (balanced load, R_L connected between VPO^+ and VPO^-)				Vrms
	R_L = 600 Ω	3.3			
	R_L = 1200 Ω	3.5			
	R_L = 30 kΩ	4.0			
S/D_P	Signal/Distortion R_L = 600 Ω, 0 dBm0	50			dB

Notes : 1. Measured by extrapolation from the distortion test results
2 PPSRX, NPSRX, CTR–X measured with a –50dBm0 activating signal applied at VF_XI^+

ENCODING FORMAT AT D_X OUTPUT

	A-Law (including even bit inversion)	μLaw
V_{IN} (at GS_X) = + Full-scale	1 0 1 0 1 0 1 0	1 0 0 0 0 0 0 0
V_{IN} (at GS_X) = 0 V	1 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1	1 1 1 1 1 1 1 1 0 1 1 1 1 1 1 1
V_{IN} (at GS_X) = – Full-scale	0 0 1 0 1 0 1 0	0 0 0 0 0 0 0 0

APPLICATION INFORMATION

POWER SUPPLIES

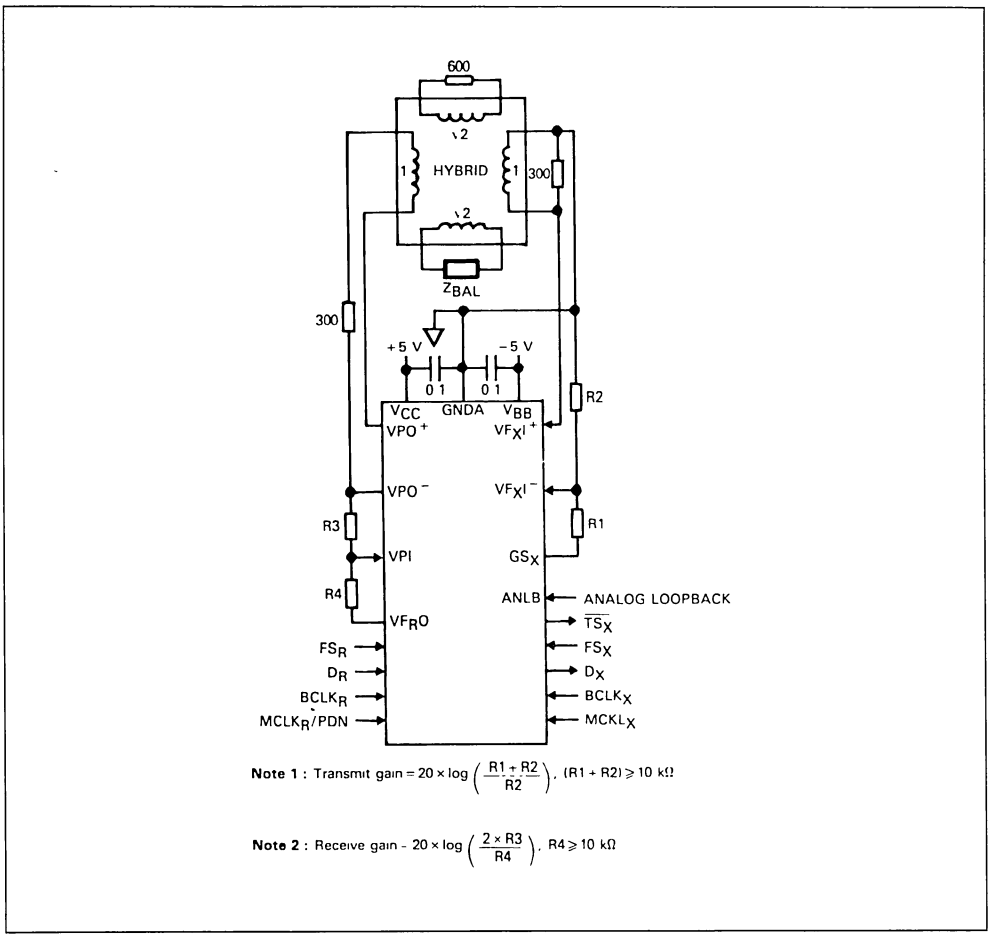
While the pins at the ETC5060 family are well protected against electrical misure, it is recommended that the standard CMOS practice be followed, ensuring that ground is connected to the device before any other connections are made. In applications where the printed circuit board may be plugged into a "hot" socket with power and clocks already present, an extra long ground pin in the connector should be used.

All ground connections to each device should meet at a common point as close as possible to the GNDA pin. This minimizes the interaction of ground return currents flowing through a common bus impedance. 0.1µF supply decoupling capacitors should be connected from this common ground point to V_{CC} and V_{BB} as close to the device as possible.

For best performance, the ground point of each CODEC/FILTER on a card should be connected to a common card ground in star formation, rather than via a ground bus. This common ground point should be decoupled to V_{CC} and V_{BB} with 10µF capacitors.

For best performance, TSX should be grounded if not used.

Figure 4 : Typical Asynchronous Application.



Note 1 : Transmit gain = $20 \times \log \left(\frac{R1 + R2}{R2} \right)$, $(R1 + R2) \geq 10\ k\Omega$

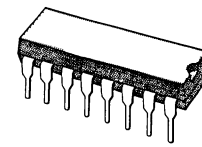
Note 2 : Receive gain = $20 \times \log \left(\frac{2 \times R3}{R4} \right)$, $R4 \geq 10\ k\Omega$

SGS-THOMSON MICROELECTRONICS

ETC50S64
ETC50S67

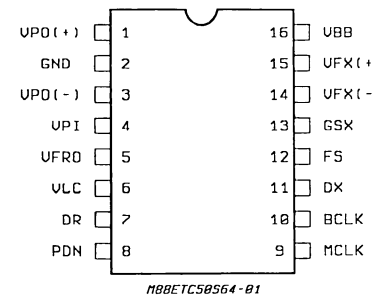
SYNCHRONOUS SERIAL INTERFACE CODEC/FILTER WITH RECEIVE POWER AMPLIFIER

- COMPLETE CODEC AND FILTERING SYSTEM (combo) INCLUDING :
  - TRANSMIT HIGH-PASS AND LOW-PASS FILTERING
  - RECEIVE LOW-PASS FILTER WITH SIN X/X CORRECTION
  - ACTIVE RC NOISE FILTERS
  - μ-LAW OR A-LAW COMPATIBLE CODER AND DECODER
  - INTERNAL PRECISION VOLTAGE REFERENCE
  - SERIAL I/O INTERFACE
  - INTERNAL AUTO-ZERO CIRCUITRY
  - RECEIVE PUSH-PULL POWER AMPLIFIERS
- μ-LAW ETC50S64
- A-LAW ETC50S67
- MEETS OR EXCEEDS ALL D3/D4 AND CCITT SPECIFICATIONS
- ± 5 V OPERATION
- LOW OPERATING POWER - TYPICALLY 70 mW
- POWER-DOWN STANDBY MODE - TYPICALLY 3 mW
- AUTOMATIC POWER-DOWN
- TTL OR CMOS COMPATIBLE DIGITAL INTERFACE
- MAXIMIZES LINE INTERFACE CARD CIRCUIT DENSITY
- IDEAL FOR DIGITAL TELEPHONE SET APPLICATION



DIP16
(Plastic)
ORDER CODES : ETC50S67N
ETC50S64N

PIN CONNECTION

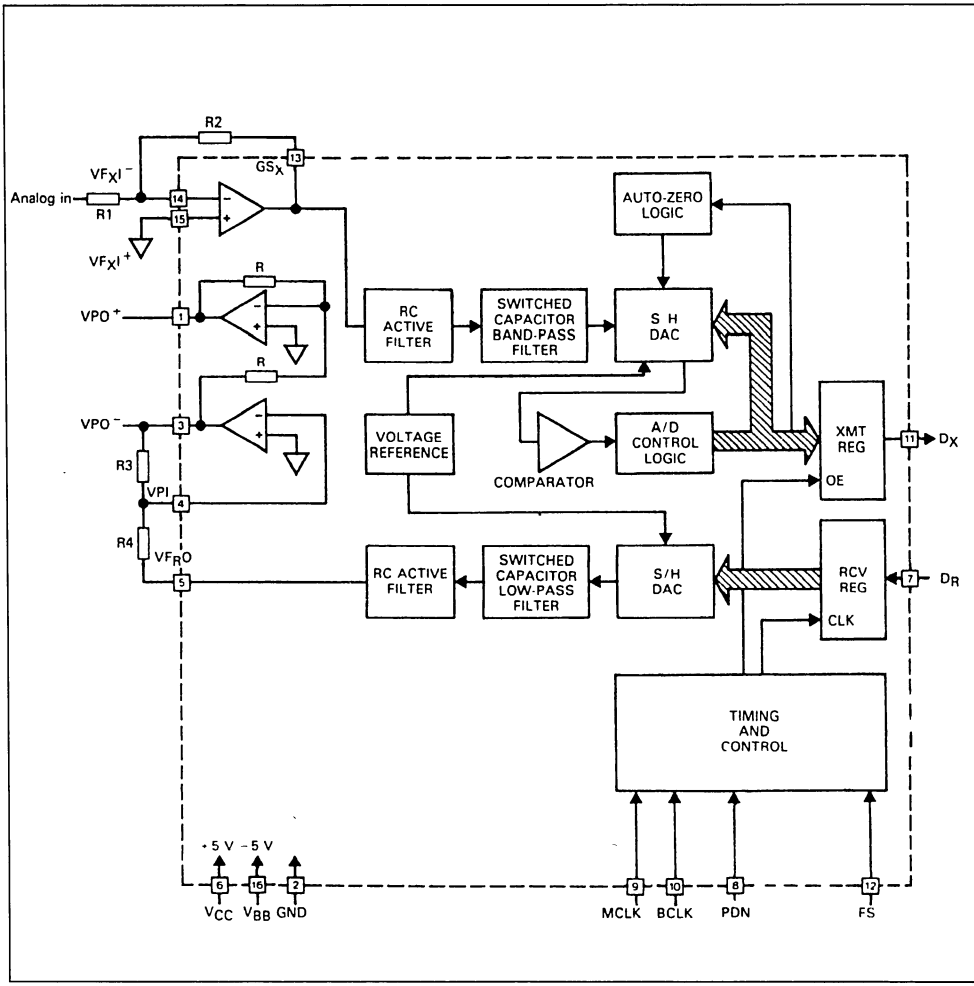


M88ETC50S64-01

DESCRIPTION

The ETC50S64 (μ-law) and ETC50S67 (A-Law) are synchronous monolithic PCM CODEC/FILTERS utilizing the A/D and D/A conversion architecture shown in the block diagram below, and a serial PCM interface. The devices are fabricated using double-poly CMOS process. Similar to ETC505X - family, these devices feature an additional Receive Power Amplifier to provide push-pull balanced output drive capability. The receive gain can be adjusted by means of two external resistors for an output level of up to ± 6.6 V across a balanced 600 Ω load.

BLOCK DIAGRAM



PIN DESCRIPTION

Name	Pin Type (*)	N°	Description
VPO+	O	1	The Non-inverted Output to the Receive Power Amplifier.
GND	GND	2	Ground. All signals are referenced to this pin.
VPO–	O	3	The Inverted Output of the Receive Power Amplifier.
VPI	I	4	Inverting input to the receive power amplifier. Also powers down both amplifiers when connected to V_{BB}.
VF_RO	O	5	Analog Output of the Receive Filter.
V_{CC}	S	6	Positive Power Supply Pin. V_{CC} = + 5 V ± 5 %.
D_R	I	7	Receive Data Input. PCM data is shifted into D_R following the FS_R leading edge.
PDN	I	8	Power Down Selection. Must be connected continuously low in operation. When PDN is connected continuously high, the device is powered down.
MCLK	I	9	Master Clock. Must be 2.048 MHz for ETC50S67 and 1.536 or 1.544 MHz for ETC50S64.
BCLK	I	10	Bit clock which shifts out the PCM data on D_X and shifts PCM data into DR. May vary from 64 kHz to 2.048 MHz, but must be synchronous with MCLK.
D_X	O	11	The tri-state PCM data output which is enabled by FS.
FS	I	12	Frame sync. pulse, which enables BCLK to shift out the PCM data on DX, and to shift PCM data into DR. FS is a 8KHz pulse train.
GS_X	O	13	Analog Output of the Transmit Input Amplifier. Used to externally set gain.
$VF_XI–$	I	14	Inverting Input of the Transmit Input Amplifier.
VF_XI+	I	15	Non-inverting Input of the Transmit Input Amplifier.
V_{BB}	S	16	Negative Power Supply Pin. V_{BB} = – 5 V ± 5 %.

(*) I : Input, O : Outputs, S : Power supply.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	V_{CC} to GND	7	V
V_{BB}	V_{BB} to GND	– 7	V
V_{IN}, V_{OUT}	Voltage at any Analog Input or Output	V_{CC} + 0.3 to V_{BB} – 0.3	V
	Voltage at any Digital Input or Output	V_{CC} + 0.3 to GND – 0.3	V
T_{oper}	Operating Temperature Range	– 25 to + 125	°C
T_{stg}	Storage Temperature Range	– 65 to + 150	°C
	Lead Temperature (soldering, 10 seconds)	300	°C

FUNCTIONAL DESCRIPTION

POWER-UP

When power is first applied, power-on reset circuitry initializes the COMBO and places it into the power-down mode. All non-essential circuits are deactivated and the D_X and VF_RO outputs are put in high impedance states. To power-up the device, a logical low level or clock must be applied to the PDN pin and FS pulses must be present. Thus, 2 power-down control modes are available. The first is to pull the PDN pin high ; the alternative is to hold FS input continuously low. The device will power-down approximately 2 ms after the last FS pulse. Power-up will occur on the first FS pulse. The TRI-STATE PCM data output, DX, will remain in the high impedance state until the second FS pulse.

OPERATION

A clock must be applied to MCLK (2.048 MHz for ETC50S67, 1.544 or 1.536 for ETC50S64) and the PDN pin can be used as a power-down control. A low level on PDN powers up the device and a high level powers down the device. A bit clock must also be applied to BCLK. For 1.544 MHz operation, the device automatically compensates for the 193rd clock pulse each frame. The bit clock, BCLK may be from 64 kHz to 2.048 MHz, but must be synchronous with MCLK. Each FS pulse begins the encoding cycle and the PCM data from the previous encode cycle is shifted out of the enabled DX output on the positive edge of BCLK. After 8 bit clock periods, the TRI-STATE D_X output is returned to a high impedance state. With an FS pulse. PCM data is latched via the D_R input on the negative edge of BCLK. FS must be synchronous with MCLK.

SHORT FRAME SYNC OPERATION

The COMBO can utilize either a short frame sync pulse or a long frame sync pulse. Upon power initialization, the device assumes a short frame mode. In this mode FS sync pulse must be one bit period long, with timing relationships specified in figure 2. With FS high during a falling edge of BCLK, the next rising edge of BCLK enables the DX TRI-STATE output buffer, which will output the sign bit. The following seven rising edges clock out the remaining seven bits, and the next falling edge disables the DX output. With FS high during a falling edge of BCLK, the next falling edge of BCLK latches in the sign bit. The following seven falling edges latch in the seven remaining bits.

LONG FRAME SYNC OPERATION

To use the long frame mode, FS must be three or more bit clock periods long, with timing relationships specified in figure 3. Based on FS the COMBO will sense whether short or long frame sync pulses are being used. For 64 kHz operation, the frame sync pulse must be kept low for a minimum of 160 ns (see fig. 1). The D_X TRI-STATE output buffer is enabled with the rising edge of FS or the rising edge of BCLK, whichever comes later, and the first bit clocked out is the sign bit. The following seven BCLK rising edges clock out the remaining seven bits. The D_X output is disabled by the falling BCLK edge following the eighth rising edge or by FS going low, whichever comes later. A rising edge on the receive frame sync pulse, FS, will cause the PCM data at D_R to be latched in on the next eight falling edges of BCLK.

TRANSMIT SECTION

The transmit section input is an operational amplifier with provision for gain adjustment using two external resistor, see figure 5. The low noise and wide band-width allow gains in excess of 20 dB across the audio passband to be realized. The op amp drives a unity-gain filter consisting of RC active prefilter, followed by an eighth order switched-capacitor bandpass filter clocked at 256 kHz. The output of this filter directly drives the encoder sample-and-hold circuit. The A/D is of companding type according to A-law (ETC50S67) or μ-law (ETC50S64) coding conventions. A precision voltage reference is trimmed in manufacturing to provide on input overload (t_{MAX}) of nominally 2.5 V peak (see table of Transmission Characteristics). The FS frame sync pulse controls the sampling of the filter output, and then the successive-approximation encoding cycle begins. The 8-bit code is then loaded into a buffer and shifted out through D_X at the next FS pulse. The total encoding delay will be approximately 165 μs (due to the transmit filter) plus 125 μs (due to encoding delay), which totals 290 μs. Any offset voltage due to the filters or comparator is cancelled by sign bit integration.

RECEIVE SECTION

The receive section consists of an expanding DAC which drives a fifth order switched-capacitor low pass filter clocked at 256 kHz. The decoder is A-law (ETC50S67) or μ-law (ETC50S64) and the 5 th order low pass filter corrects for the sin x/x attenuation due to the 8 kHz sample and hold. The filter is then followed by a 2 nd order RC active post-filter and power amplifier capable of driving a 600 Ω load to a level of 7.2 dBm. The receive section is unity-gain. Upon the occurence of FS, the data at the D_R input is clocked in on the falling edge of the next eight BCLK periods. At the end of the decoder time slot, the decoding cycle begins, and 10 μlater the decoder DAC output is updated. The total decoder delay is ~ 10 μs (decoder update) plus 110 μs (filter delay) plus 62.5 μs (1/2 frame), which gives approximately 180 μs.

RECEIVE POWER AMPLIFIERS

Two inverting mode power amplifiers are provided for directly driving a matched line interface transformer. The gain of the first power amplifier can be adjusted to boost the ± 2.5 V peak output signal from the receive filter up ± 3.3 V peak into an unbalanced 300 Ω load, or ± 4.0 V into an unbalanced 15 kΩ

load. The second power amplifier is internally connected in unity-gain inverting mode to give 6 dB of signal gain for balanced loads. Maximum power transfer to a 600 Ω subscriber line termination is obtained by differentially driving a balanced transformer with a √2 : 1 turns ratio. A total peak power of 15.6 dBm can be delivered to the load plus termination. Both power amplifiers can be powered down independently form the PDN input by connecting the VPI input to V_{BB} saving approximately 12 mW of power.

ELECTRICAL OPERATING CHARACTERISTICS V_{CC} = 5.0 V ± 5 %, V_{BB} = − 5 V ± 5 %, GND = 0 V, T_A = 0 °C to 70 °C (unless otherwise noted) ; typical characteristics specified at V_{CC} = 5.0 V, V_{BB} = − 5.0 V, T_A = 25 °C ; all signals are referenced to GND.

DIGITAL INTERFACE

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{IL}	Input Low Voltage	–	–	0.6	V
V_{IH}	Input High Voltage	2.2	–	–	V
V_{OL}	Output Low Voltage I_{IL} = 3.2 mA D_X	–	–	0.4	V
V_{OH}	Output High Voltage I_H = − 3.2 mA D_X	2.4	–	–	V
I_{IL}	Input Low Current (GND ≤ V_{IN} ≤ V_{IL} all digital inputs except BCLK)	− 10	–	10	µA
I_{IH}	Input High Current (V_{IH} ≤ V_{IN} ≤ V_{CC})	− 10	–	10	µA
I_{OZ}	Output Current in High Impedance State (TRI-STATE) (GND ≤ V_O ≤ V_{CC}) D_X	− 10	–	10	µA

ANALOG INTERFACE WITH TRANSMIT INPUT AMPLIFIER (all devices)

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_IXA	Input Leakage Current (− 2.5 V ≤ V ≤ + 2.5 V) VF_XI^+ or VF_XI^-	− 200	–	200	nA
R_IXA	Input Resistance (− 2.5 V ≤ V ≤ + 2.5 V) VF_XI^+ or VF_XI^-	10	–	–	MΩ
R_OXA	Output Resistance (closed loop, unity gain)	–	1	3	Ω
R_LXA	Load Resistance GS_X	10	–	–	kΩ
C_LXA	Load Capacitance GS_X	–	–	50	pF
V_OXA	Output Dynamic Range (R_L ≥ 10 kΩ) GS_X	± 2.8	–	–	V
A_VXA	Voltage Gain (VF_XI^+ to GS_X)	5000	–	–	V/V
F_UXA	Unity Gain Bandwidth	1	2	–	MHz
$V_{OS}XA$	Offset Voltage	− 20	–	20	mV
$V_{CM}XA$	Common-mode Voltage	− 2.5	–	2.5	V
CMRRXA	Common-mode Rejection ratio	60	–	–	dB
PSRRXA	Power Supply Rejection Ratio	60	–	–	dB

ANALOG INTERFACE WITH RECEIVE FILTER (all devices)

Symbol	Parameter	Min.	Typ.	Max.	Unit
R_ORF	Output Resistance VF_RO	–	1	3	Ω
R_LRF	Load Resistance (VF_RO = ± 2.5 V)	10	–	–	kΩ
C_LRF	Load Capacitance	–	–	25	pF
VOS_RO	Output DC Offset Voltage	− 200	–	200	mV

ELECTRICAL OPERATING CHARACTERISTICS (continued)

ANALOG INTERFACE WITH POWER AMPLIFIERS (all devices)

Symbol	Parameter	Min.	Typ.	Max.	Unit
IPI	Input Leakage Current (– 1.0 V ≤ VPI ≤ 1.0 V)	– 100	–	100	nA
RIPI	Input Resistance (– 1.0 V ≤ VPI ≤ 1.0 V)	10	–	–	MΩ
VIOS	Input Offset Voltage	– 25	–	25	mV
ROP	Output Resistance (inverting unity-gain at VPO^+ or VPO^-)	–	1	–	Ω
F_C	Unity-gain Bandwidth, open loop (VPO^-)	–	400	–	kHz
C_LP	Load Capacitance (VPO^+ or VPO^- to GND) $R_L \geq 1500\ \Omega$ $R_L = 600\ \Omega$ $R_L = 300\ \Omega$	 – – –	 – – –	 100 500 1000	pF
GAp+	Gain VPO– to VPO^+ to GND, Level at $VPO^- = 1.77$ Vrms (+ 3 dBmO)	–	– 1	–	V/V
PSRRp	Power Supply Rejection of V_{CC} or V_{BB} (VPO^- connected to VPI) 0 kHz - 4 kHz 0 kHz - 50 kHz	 60 36	 – –	 – –	dB

POWER DISSIPATION (all devices)

Symbol	Parameter	Min.	Typ.	Max.	Unit
$I_{CC}0$	Power-Down Current	–	0.5	2.0	mA
$-I_{BB}0$	Power-Down Current	–	0.05	0.5	mA
$-I_{CC}1$	Active Current	–	7.0	12.0	mA
$I_{BB}1$	Active Current	–	7.0	12.0	mA

TIMING SPECIFICATIONS. All timing parameters are measured at V_{OH} = 2.0 V and V_{OL} = 0.7 V. See "definitions" and "timing conventions" section for test method information.

Symbol	Parameter		Min.	Typ.	Max.	Unit
$1/t_{PM}$	Frequency of Master Clock ETC50S64 ETC50S67	MCLK	– – –	1.536 1.544 2.048	– – –	MHz
t_{WMH}	Width of Master Clock High	MCLK	160	–	–	ns
t_{WML}	Width of Master Clock Low	MCLK	160	–	–	ns
t_{RM}	Rise Time of Master Clock	MCLK	–	–	50	ns
t_{FM}	Fall Time of Master Clock	MCLK	–	–	50	ns
t_{PB}	Period of Bit Clock		485	488	15.725	ns
t_{WBH}	Width of Bit Clock High (V_{IH} = 2.2 V)		160	–	–	ns
t_{WBL}	Width of Bit Clock Low (V_{IL} = 0.6 V)		160	–	–	ns
t_{RB}	Rise Time of Bit Clock (t_{PB} = 488 ns)		–	–	50	ns
t_{FB}	Fall Time of Bit Clock (t_{PB} = 488 ns)		–	–	50	ns
t_{SBFM}	Set-up time from BCLK high to MCLK falling edge. (first bit clock after the leading edge of FS)		100	–	–	ns
t_{HBF}	Holding Time from Bit Clock Low to the Frame Sync (long frame only)		0	–	–	ns
t_{SFB}	Set-up Time from Frame Sync to Bit Clock Low (long frame only)		80	–	–	ns
t_{HBFI}	Hold Time from 3rd Period of Bit Clock Low to Frame Sync (long frame only)	FS	100	–	–	ns
t_{DZF}	Delay Time to Valid Data from FS or BCLK Whichever Comes Later and Delay Time from FS to Data Output Disabled (C_L = 0 pF to 150 pF)		20	–	165	ns
t_{DBD}	Delay Time from BCLK High to Data Valid (load = 150 pF plus 2 LSTTL loads)		0	–	180	ns
t_{DZC}	Delay Time from BCLK Low to Data Output Disabled		50	–	165	ns
t_{SDB}	Set-up Time from D_R Valid to BCLK Low		50	–	–	ns
t_{HBD}	Hold Time from BCLK Low to D_R Invalid		50	–	–	ns
t_{HOLD}	Holding Time from Bit Clock High to Frame Sync (short frame only)		0	–	–	ns
t_{SF}	Set-up Time from FS to BCLK Low (short frame sync pulse) - Note 1		80	–	–	ns
t_{HF}	Hold Time from BCLK Low to FS Low (short frame sync pulse) Note 1		100	–	–	ns
t_{WFL}	Minimum Width of the Frame Sync Pulse (low level) (64k bit/s operating mode)		160	–	–	ns

Note : 1. For short frame sync timing FS must go high while bit clock is high.

Figure 1 : 64 k bits/s TIMING DIAGRAM.

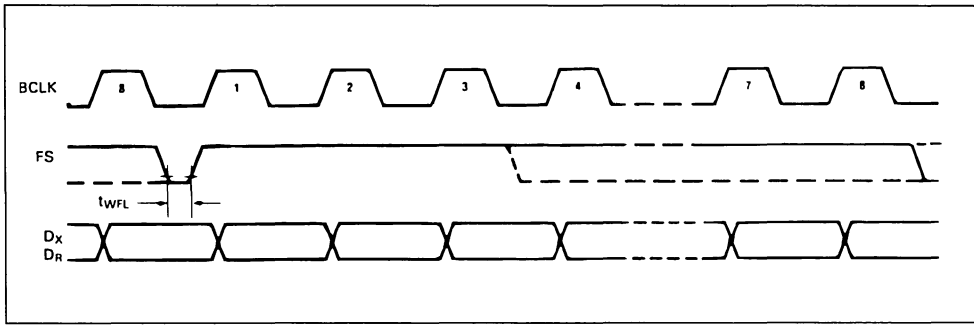


Figure 2 : Short Frame Sync Timing.

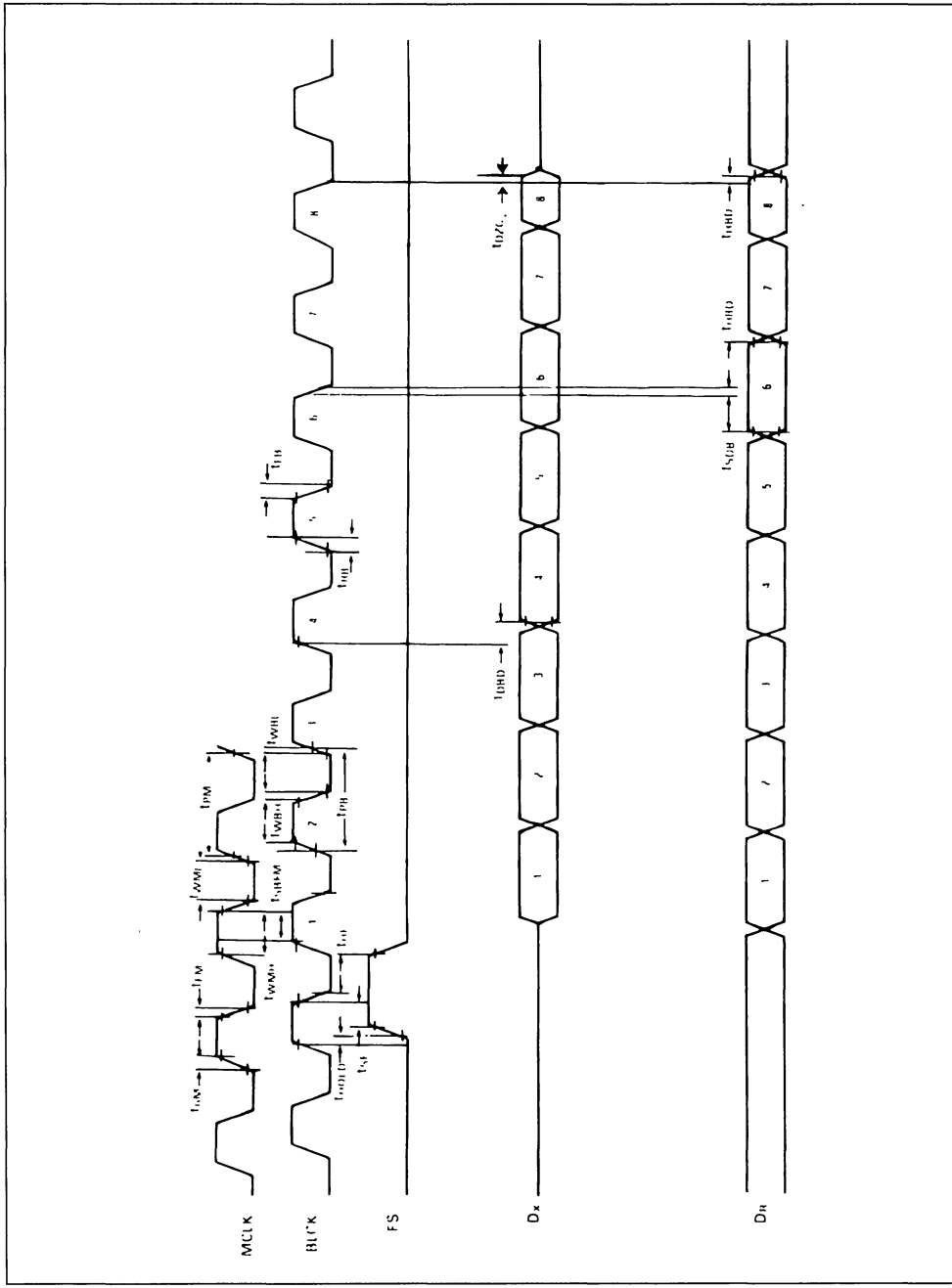
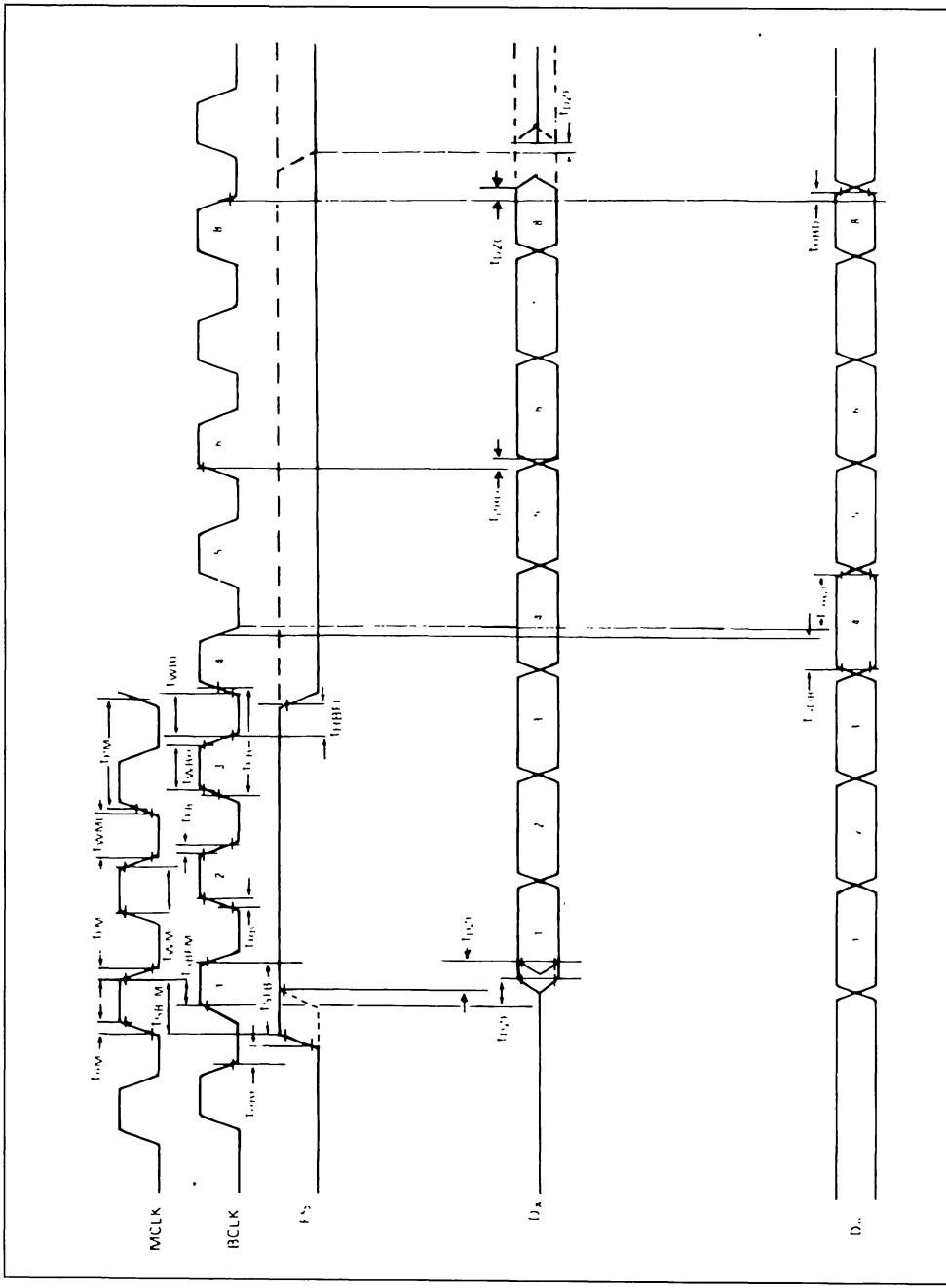


Figure 3 : Long Frame Sync Timing.



TRANSMISSION CHARACTERISTICS (all devices) T_A = 0 °C to 70 °C, V_{CC} = 5 V ± 5 %, V_{BB} = – 5 V ± 5 %, GND = 0 V, f = 1.02 kHz, V_{IN} = 0 dBm0 transmit input amplifier connected for unity-gain non-inverting.
(unless otherwise specified)

AMPLITUDE RESPONSE

Symbol	Parameter	Min.	Typ.	Max.	Unit
	Absolute Levels - Nominal 0 dBm0 level is 4 dBm (600 Ω) 0 dBm0	–	1.2276	–	Vrms
t_{MAX}	Max Overload Level				V_{PK}
	3.14 dBm0 ETC50S67	–	2.492	–	
	3.17 dBm0 ETC50S64	–	2.501	–	
G_{XA}	Transmit Gain, Absolute (T_A = 25 °C, V_{CC} = 5 V, V_{BB} = – 5 V) Input at GS_X = 0 dBm0 at 1020 Hz	– 0.15	–	0.15	dB
G_{XR}	Transmit Gain, Relative to G_{XA}				dB
	f = 16 Hz	–	–	– 40	
	f = 50Hz	–	–	– 30	
	f = 60 Hz	–	–	– 26	
	f = 180 Hz	– 2.8	–	– 0.2	
	f = 200 Hz	– 1.8	–	– 0.1	
	f = 300 Hz-3000Hz	– 0.15	–	0.15	
	f = 3300 Hz	– 0.35	–	0.05	
	f = 3400 Hz	– 0.7	–	0	
	f = 4000 Hz	–	–	– 14	
	f = 4600 Hz and up, measure reponse from 0Hz to 4000 Hz	–	–	– 32	
G_{XAT}	Absolute Transmit Gain Variation with Temperature (T_A = 0 °C to + 70 °C)	– 0.1	–	0.1	dB
G_{XAV}	Absolute Transmit Gain Variation with Supply Voltage (V_{CC} = 5 V ± 5 %, V_{BB} = – 5 V ± 5 %)	– 0.05	–	– 0.05	dB
G_{XRL}	Transmit Gain Variation with Level Sinusoidal Test Method Reference Level = – 10 dBm0				dB
	VF_XI^+ = – 40 dBm0 to + 3 dBm0	– 0.2	–	0.2	
	VF_XI^+ = – 50 dBm0 to – 40 dBm0	– 0.4	–	0.4	
	VF_XI^+ = – 55 dBm0 to – 50 dBmo	– 1.2	–	1.2	
G_{RA}	Receive Gain, Absolute (T_A = 25 °C, V_{CC} = 5 V, V_{BB} = – 5 V) Input = Digital Code Sequence for 0dBm0 Signal at 1020 Hz	– 0.15	–	0.15	dB
G_{RR}	Receive Gain, relative to G_{RA}				dB
	f = 0 Hz to 3000 Hz	– 0.15	–	0.15	
	f = 3300 Hz	– 0.35	–	0.05	
	f = 3400 Hz	– 0.7	–	0	
	f = 4000 Hz	–	–	– 14	
G_{RAT}	Absolute Receive Gain Variation with Temperature (T_A = 0 °C to + 70 °C)	– 0.1	–	0.1	dB
G_{RAV}	Absolute Receive Gain Variation with Supply Voltage (V_{CC} = 5 V ± 5 %, V_{BB} = – 5 V ± 5 %)	– 0.05	–	0.05	dB
G_{RRL}	Receive Gain Variation with Level Sinusuoidal Test Method ; reference input PCM code corresponds to an ideally encoded – 10 dBm0 signal				dB
	PCM Level = – 40 dBm0 to + 3 dBm0	– 0.2	–	0.2	
	PCM Level = – 50 dBm0 to – 40 dBm0	– 0.4	–	0.4	
	PCM Level = – 55 dBm0 to – 50 dBm0	– 1.2	–	1.2	
V_{RO}	Receive Filter Output at VF_RO, R_L = 10 kΩ	– 2.5	–	2.5	V

TRANSMISSION CHARACTERISTICS (continued)

ENVELOPE DELAY DISTORTION WITH FREQUENCY

Symbol	Parameter	Min.	Typ.	Max.	Unit
D_{XA}	Transmit Delay, Absolute (f = 1600 Hz)	–	290	315	µs
D_{XR}	Transmit Delay, Relative to D_{XA}				µs
	f = 500 Hz-600 Hz	–	195	220	
	f = 600 Hz-800 Hz	–	120	145	
	f = 800 Hz-1000 Hz	–	50	75	
	f = 1000 Hz-1600 Hz	–	20	40	
	f = 1600 Hz-2600Hz	–	55	75	
	f = 2600 Hz-2800 Hz	–	80	105	
	f = 2800 Hz-3000 Hz	–	130	155	
D_{RA}	Receive Delay, Absolute (f = 1600 Hz)	–	180	200	µs
D_{RR}	Receive Delay, Relative to D_{RA}				µs
	f = 500 Hz-1000 Hz	– 40	– 25	–	
	f = 1000 Hz-1600 Hz	– 30	– 20	–	
	f = 1600 Hz-2600 Hz	–	70	90	
	f = 2600 Hz-2800 Hz	–	100	125	
	f = 2800 Hz-3000 Hz	–	145	175	

NOISE

Symbol	Parameter	Min.	Typ.	Max.	Unit
N_{XP}	Transmit Noise, P Message Weighted (ETC50S67, VF_XI^+ = 0 V)	–	– 74	– 67 (note 1)	dBm0p
N_{RP}	Receive Noise, P Message Weighted (ETC50S67, PCM code equals positive zero)	–	– 82	– 79	dBm0p
N_{XC}	Transmit Noise, C Message Weighted (ETC50S64, $VFXI^+$ = 0 v)	–	12	15	dBmCO
N_{RC}	Receive Noise, C Message Weighted (ETC50S64, PCM code equals alternating positive and negative zero)	–	8	11	dBmC0
N_{RS}	Noise, Single Frequency f = 0 kHz to 100 kHz, Loop around Measurement, VF_XI^+ = 0 V	–	–	– 53	dBm0
$PPSR_X$	Positive Power Supply Rejection, Transmit (note 2) V_{CC} = 5.0 V_{DC} + 100 mVrms, f = 0 kHz-50 kHz	40	–	–	dBp
$NPSR_X$	Negative Power Supply Rejection, Transmit (note 2) V_{BB} = – 5.0 V_{DC} + 100 mVrms, f = 0 kHz-50 kHz	40	–	–	dBp
$PPSR_R$	Positive Power Supply Rejection, receive (PCM code equals positive zero, V_{CC} = 5.0 V_{DC} + 100 mVrms) f = 0 Hz-4000Hz f = 4 kHz-25 kHz f = 25 kHz-50 kHz	 40 40 36	 – – –	 – – –	 dBp dB dB
$NPSR_R$	Negative Power Supply Rejection, receive (PCM code equals positive zero, V_{BB} = – 5.0 V_{DC} + 100 mVrms) f = 0 Hz-4000Hz f = 4 kHz-25 kHz f = 25 kHz-50 kHz	 40 40 36	 – – –	 – – –	 dBp dB dB
SOS	Spurious out-of-band Signals at the Channel Output Loop around measurement, 0 dBm0, 300 Hz-3400 Hz input applied to DR, measure individual image signals at DX 4600 Hz-7600 Hz 7600 Hz-8400 Hz 8400 Hz-100,000 Hz	 – – –	 – – –	 – 32 – 40 – 32	 dB dB dB

TRANSMISSION CHARACTERISTICS (continued)

DISTORTION

Symbol	Parameter		Min.	Typ.	Max.	Unit
STD_X or STD_R	Signal to Total Distortion (sinusoidal test method) Transmit or Receive Half-channel					dBp
	Level = 3.0 dBm0		33	–	–	
	= 0 dBm0 to – 30 dBm0		36	–	–	
	= – 40 dBm0	XMT	29	–	–	
		RCV	30	–	–	
	= – 55 dBm0	XMT	14	–	–	
		RCV	15	–	–	
SFD_X	Single Frequency Distortion, transmit		–	–	– 46	dB
SFD_R	Single Frequency Distortion, receive		–	–	– 46	dB
IMD	Intermodulation Distortion Loop Around Measurement, VF_XI + = – 4 dBm0 to – 21 dBm0, two Frequencies in the Range 300 Hz-3400 Hz		–	–	– 41	dB

CROSSTALK

Symbol	Parameter	Min.	Typ.	Max.	Unit
CT_{X-R}	Transmit to Receive Crosstalk, 0dBm0 Transmit f = 300 Hz-3400 Hz, D_R = Steady PCM Code	–	– 90	– 75	dB
CT_{R-X}	Receive to Transmit Crosstalk, 0dBm0 Receive Level f = 300 Hz-3400 Hz, VF_XI = 0 V	–	– 90	– 70 (note 2)	dB

POWER AMPLIFIERS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{OL}	Maximum 0 dBm0 Level for better than ± 0.1 dB Linearity over the Range 10 dBm0 to + 3 dBm0 (balanced load, R_L connected between VPO^+ and VPO^-)				Vrms
	R_L = 600 Ω	33	–	–	
	R_L = 1200 Ω	3.5	–	–	
	R_L = 30 kΩ	4.0	–	–	
S/D_P	Signal/Distortion R_L = 600 Ω, 0dBm0	50	–	–	dB

Notes : 1. Measured by extrapolation from the distortion test result.
2. PPSRX, NPSRX, CTR-X measured with a - 50 dBmO activating signal applied at VFxI+.

ENCODING FORMAT AT D_X OUTPUT

	A-Law (including even bit inversion)	μLaw
V_{IN} (at GS_X) = + Full-scale	1 0 1 0 1 0 1 0	1 0 0 0 0 0 0 0
V_{IN} (at GS_X) = 0 V	1 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1	1 1 1 1 1 1 1 1 0 1 1 1 1 1 1 1
V_{IN} (at GS_X) = – Full-scale	0 0 1 0 1 0 1 0	0 0 0 0 0 0 0 0

APPLICATION INFORMATION

POWER SUPPLIES

While the pins at the ETC5056 family are well protected against electrical misure, it is recommended that the standard CMOS practice be followed, ensuring that ground is connected to the device before any other connections are made. In applications where the printed circuit board may be plugged into a "hot" socket with power and clocks already present, an extra long ground pin in the connector should be used.

All ground connections to each device should meet at a common point as close as possible to the GND pin. This minimizes the interaction of ground return currents flowing through a common bus impedance. 0.1 µF supply decoupling capacitors should be connected from this common ground point to V_{CC} and V_{BB} as close to the device as possible.

For best performance, the ground point of each CODEC/FILTER on a card should be connected to a common card ground in star formation, rather than via a ground bus. This common ground point should be decoupled to V_{CC} and V_{BB} with 10 µF capacitors.

COMBINED SINGLE CHIP PCM CODEC AND FILTER

- M5914 ASYNCHRONOUS CLOCK, 8th BIT SIGNALING, LOOP BACK TEST CAPABILITY
- M5913 SYNCHRONOUS CLOCKS ONLY
- AT&T D3/D4 AND CCITT COMPATIBLE
- TWO TIMING MODES :
  FIXED DATA RATE MODE : 1.536 MHz, 1.544 MHz, 2.048 MHz
  VARIABLE DATA MODE : 64 kHz - 4.096 MHz
- PIN SELECTABLE μ-LAW OR A-LAW OPERATION
- NO EXTERNAL COMPONENTS FOR SAMPLE AND HOLD AND AUTO ZERO FUNCTIONS
- LOW POWER DISSIPATION :
  0.5 mW POWER DOWN 70 mW OPERATING
- EXCELLENT POWER SUPPLY REJECTION

DESCRIPTION

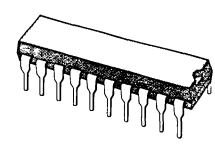
The M5913 and M5914 are fully integrated PCM (pulse code modulation) codecs and transmit/receive filter using CMOS silicon gate technology.

The primary applications for the M5913 and M5914 are telephone systems :

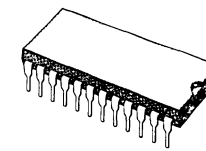
- Switching - M5913-Digital PBX's and Central Office Switching Systems
- Transmission - M5914-D3/D4 Channel Banks
- Concentration - M5913 and M5914-Subscriber Carrier and Concentrators.

The wide dynamic range of the M5913 and M5914 (78 dB) and the minimal conversion time make them ideal products for other applications such as :

Voice Store and Forward - Digital Echo Cancellers - Secure Communications Systems - Satellite Earth Stations.



DIP20
(Plastic and Ceramic)

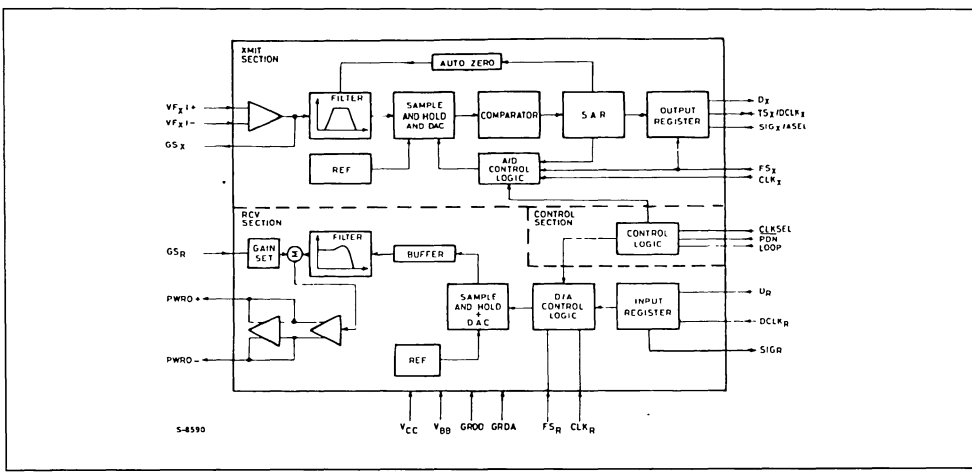


DIP24
(Plastic and Ceramic)

ORDER CODES :

M5913B1	M5913F1
M5914B1	M5914F1

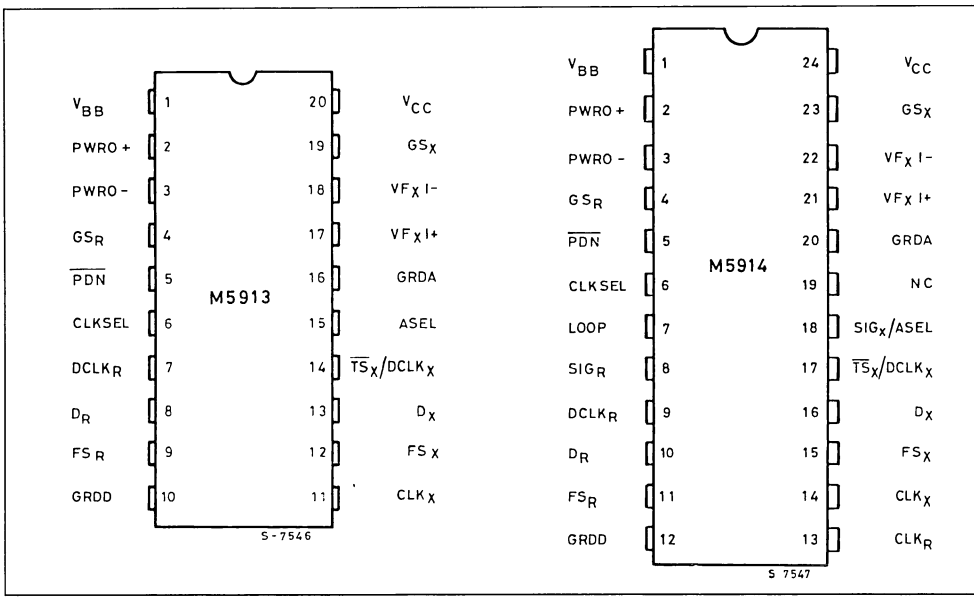
BLOCK DIAGRAM



PIN NAMES

V_{BB}	Power (– 5 V)	GS_X	Gain Control
PWRO+, PWRO–	Power Amplifier Outputs	$VF_XI–$, VF_XI+	Analog Inputs
$\overline{GS_R}$	Gain Setting Input for Receive Channel	GRDA	Analog Ground
PDN	Power Down Select	NC	No Connect
CLKSEL	Master Clock Select	SIG_X	Transmit Digital Signaling Input
LOOP	Analog Loop Back	$\overline{ASEL}$	μ or A-law Select
SIG_R	Signaling Bit Output	$\overline{TS_X}$	Digital Output - Timeslot Strobe
$DCLK_R$	Receive Data Rate Clock	$DCLK_X$	Transmit Data Rate Clock
D_R	Receive Channel Input	D_X	Transmit (digital) Output
FS_R	Receive Frame Synchronization Clock	FS_X	Transmit Frame Synchronization Clock
GRDD	Digital Ground	CLK_X	Transmit Master Clock
V_{CC}	Power (+ 5 V)	CLK_R	Receive Master Clock

PIN CONNECTION



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	With Respect GRDD, GRDA = 0 V	– 0.6 to 7	V
V_{BB}	With Respect GRDD, GRDA = 0 V	0.6 to – 7	V
GRDD, GRDA	In Such Case : $0 \leq V_{CC} \leq +7$ V, -7 V $\leq V_{BB} \leq 0$ V	± 0.3	V
$V_{I/O}$	Analog Inputs, Analog Outputs and Digital Inputs	$V_{BB} - 0.3 \leq V_{IN}/V_{OUT} \leq V_{CC} + 0.3$	V
$V_{O\ DIG}$	Digital Outputs	$GRDD - 0.3 \leq V_{OUT} \leq V_{CC} + 0.3$	V
T_{op}	Temperature Range	– 10 to 80	°C
T_{stg}	Storage Temperature	– 65 to 150	°C
P_{tot}	Power Dissipation	1	W

PIN DESCRIPTIONS

Symbol	Function
V_{BB}	Most negative supply, input voltage is – 5 V ± 5 %.
PWRO+	Non-inverting Output of Power Amplifier. Can drive transformer hybrids or high impedance loads directly in either a differential or single ended configuration.
PWRO–	Inverting Output of Power Amplifier. Functionally identical and complementary to PWRO+.
GS_R	Input to the Gain Setting Network on the Output Power Amplifier. Transmission level can be adjusted over a 12 dB range depending on the voltage at GS_R.
$\overline{PDN}$	Power Down Select. When $\overline{PDN}$ is TTL high, the device is active. When low, the device is powered down.
CLKSEL	Input which must be pinstrapped to reflect the master clock frequency at CLK_X, CLK_R. CLKSEL = V_{BB} ..... 2.048 MHz CLKSEL = GRDD ..... 1.544 MHz CLKSEL = V_{CC} ..... 1.536 MHz
LOOP	Analog Loopback. When this pin is TTL high, the receive output (PWRO+) is internally connected to VF_XI+, GS_R is internally connected top PWRO–, and VF_XI- 0s internally connected to GS_X. A 0 dBm0 digital signal input at D_R is returned as a + 3 dBm0 digital signal outupt at D_X.
SIG_R	Signaling Bit Output, Receive Channel. In fixed data rate mode, SIG_R outputs the logical state of the eighth bit of the PCM word in the most recent signaling frame.
$DCLK_R$	Selects the fixed or variable data rate mode. When $DCLK_R$ is connected to V_{BB}, the fixed data rate mode is selected. When $DCLK_R$ is not connected to V_{BB}, the device operates in the variable data rate mode. In this mode $DCLK_R$, becomes the receive data clock which operates a TTL levels from 64 kB to 4.096 MB data rates.
D_R	Receive PCM Input. PCM data is clocked in on this lead on eight consecutive negative transitions of the receive data clock ; CLK_R in the fixed data rate mode and $DCLK_R$ in variable data rate mode.
FS_R	8 KHz frame synchronization clock input/timeslot enable, receive channel. A multifunction input which in fixed data rate mode distinguishes between signaling and non-signaling frames by means of a double or single wide pulse respectively. In variable data rate mode this signal must remain high for the entire length of the timeslot. The receive channel enters the standby state whenever FS_R is TTL low for 30 milliseconds.
GRDD	Digital Ground for all Internal Logic Circuits. Not Internally Tied to GRDA.
CLK_R	Receive master and data clock for the fixed data rate mode ; receive master clock only in variable data rate mode.
CLK_X	Transmit master and data clock for the fixed data rate mode, transmit master clock only in variable data rate mode.
FS_X	8 KHz frame synchronization clock input/timeslot enable, transmit channel. Operates independently but in an analogous manner to FS_R. The transmit channel enters the standby state whenever FS_X is TTL low for 30 milliseconds.
D_X	Transmit PCM output PCM data is clocked out on this lead on eight consecutive positive transitions of the transmit data clock : CLK_X in fixed data rate mode and $DCLK_X$ in variable data rate mode.
$\overline{TS_X}/DCLK_X$	Transmit channel timeslot strobe (output) or data clock (input) for the transmit channel. In variable data rate mode, this pin becomes the transmit data clock which operates at TTL levels from 64 KB to 4.096 MB data rates.

PIN DESCRIPTIONS (continued)

Symbol	Function
SIG_X/ASEL	A dual purpose selects μ-law and pin. When connected to V_{BB}. A-law operation is selected. When it is not connected to V_{BB} this pin is a TTL level input for signaling operation. This input is transmitted as the eighth bit of the PCM word during signaling frames on the D_X lead.
NC	No Connect
GRDA	Analog Ground Return for all Internal Voice Circuits. Not internally connected to GRDD.
VF_XI+	Non-inverting analog input to uncommitted transmit operational amplifier.
VF_XI-	Inverting analog input to uncommitted transmit operational amplifier.
GS_X	Output terminal of on-chip uncommitted op amp. Internally, this is the voice signal input to the transmit filter.
V_{CC}	Most Positive Supply, Input Voltage is + 5 V ± 5 %.

FUNCTIONAL DESCRIPTION

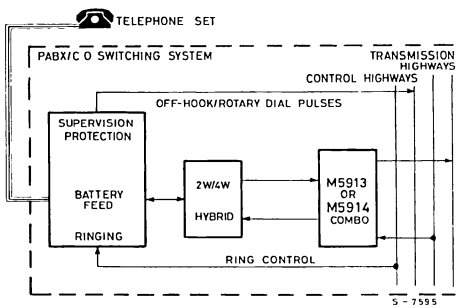
The M5913 and M5914 provide the analog-to-digital and the digital-to-analog conversions and the transmit and receive filtering necessary to interface a full duplex (4 wires) voice telephone circuit with the PCM highways of a time division multiplexed (TDM) system. They are intended be used at the analog termination of a PCM line or trunk.

The following major functions are provided :

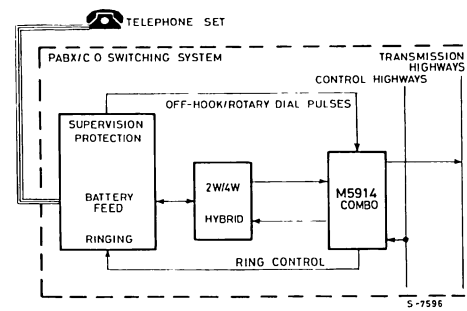
- Bandpass filtering of the analog signals prior to encoding and after decoding
- Encoding and decoding of voice and call progress information
- Encoding and decoding of the signaling and supervision information

Figure 3 : Typical Line Terminations.

SWITCHING

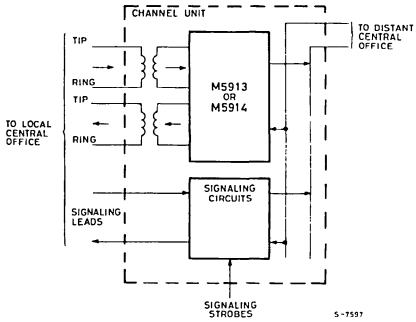


Functional block diagram of a line circuit with separate signaling control highways.

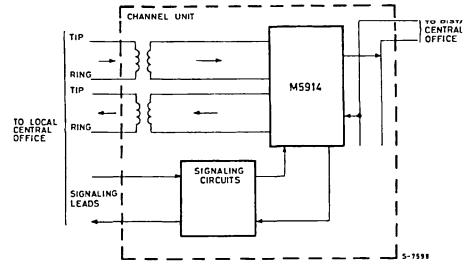


Functional block diagram of a line circuit with borrowed 8th bit signaling.

CHANNEL BANKS



A typical CCITT channel unit.



A typical 4-wire channel unit with signaling using borrowed 8th bit.

GENERAL OPERATION

SYSTEM RELIABILITY FEATURES

The combo-chip can be powered up by pulsing FS_X and/or FS_R while a TTL high voltage is applied to $\overline{PDN}$, provided that all clocks and supplies are connected. The M5913 and M5914 have internal resets on power up (or when V_{BB} or V_{CC} are re-applied) in order to ensure validity of the digital outputs and thereby maintain integrity of the PCM highway.

On the transmit channel, digital outputs D_X and $\overline{TS}_X$ are held in a high impedance state for approximately four frames (500µs) after power up or application of V_{BB} or V_{CC}. After this delay, DX, $\overline{TS}_X$, and signaling will be functional and will occur in the proper timeslot. The analog circuits on the transmit side require approximately 40 milliseconds to reach their equilibrium value due to the autozero circuit setting time. Thus, valid digital information, such as for on/off hook detection, is available almost immediately, while analog information is available after some delay.

On the receive channel, the digital output SIG_R is also held low for a maximum of four frames after power up or application of V_{BB} or V_{CC}. SIG_R will remain low thereafter until it is updated by a signaling frame.

To further enhance system reliability, $\overline{TS}_X$ and $\overline{D}_X$ will be placed in a high impedance state approximately 20µs after an interruption of CLK_X. Similarly, SIG_R will be held low approximately 20µs after an interruption of CLK_R. These interruptions could possibly occur with some kind of fault condition.

POWER DOWN AND STANDBY MODES

To minimize power consumption, two power down modes are provided in which most M5913/M5914

Table 1 : Power-down Methods.

Device Status	Power-down Method	Digital Outputs Status
Power Down Mode	$\overline{PDN}$ = TTL low	$\overline{TS}_X$ and D_X are placed in a high impedance state and SIG_R is placed in a TTL low state within 10 µs.
Standby Mode	FS_X and FS_R are TTL low.	$\overline{TS}_X$ and D_X are placed in a high impedance state and SIGR is placed in a TTL low state 30 milliseconds after FS_X and FS_R are removed.
Only transmit is on standby.	FS_X is TTL low.	$\overline{TS}_X$ and D_X are placed in a high impedance state within 30 milliseconds.
Only receive is on standby.	FS_R is TTL low.	SIG_R is placed in a TTL low state within 30 milliseconds.

functions are disabled. Only the power down, clock, and frame sync buffers, which are required to power up the device, are enabled in these modes. As shown in Table 1, the digital outputs on the appropriate channels are placed in a high impedance state until the device returns to the active mode.

The Power Down mode utilizes an external control signal to the PDN pin. In this mode, power consumption is reduced to an average of 0.5 milliwatts. The device is active when the signal is high and inactive when it is low. In the absence of any signal, the PDN pin floats to TTL high allowing the device to remain active continuously.

The Standby mode leaves the user an option of powering either channel down separately or powering the entire device down by selectively removing FS_X and/or FS_R. With both channels in the standby state, power consumptions is reduced to an average of 1 milliwatts. If transmit only operation is desired, FS_X should be applied to the device while FS_R is held low. Similarly, if receive only operation is desired, FS_R should be applied while FS_X is held low.

FIXED DATA RATE MODE

Fixed data rate timing, is selected by connecting $DCLK_R$ to V_{BB}. It employs master clocks CLK_X and CLK_R, frame synchronization clocks FS_X and FS_R, and output $\overline{TS}_X$.

CLK_X and CLK_R serve both as master clocks to operate the codec and filter sections and bit clocks to clock the data in and out from the PCM highway. FS_X and FS_R are 8 kHz inputs which set the sampling frequency and distinguish between signaling and non-signaling frames by their pulse width. A frame synchronization pulse which is one master clock wide designates a non-signaling frame, while a double wide sync pulse enables the signaling function. TS_X is a timeslot strobe/buffer enable output which gates the PCM word onto the PCM highway when an external buffer is used to drive the line.

Data is transmitted on the highway at D_X on the first eight positive transitions of CLK_X following the rising edge of FS_X. Similarly on the receive side, data is received on the first eitht falling edges of CLK_R. The frequency of CLK_X and CLK_R is selected by the CLKSEL pin to be either 1.536, 1.544 or 2.048 MHz. No other frequency of operation is allowed in the fixed data rate mode.

VARIABLE DATA RATE MODE

Variable data rate timing is selected by connecting $DCLK_R$ to the bit clock for the receive PCM highway rather than to V_{BB}. It employs master clocks CLK_X and CLK_R, bit clocks $DCLK_R$ and $DCLK_X$ and frame synchronization clocks FS_R and FS_X.

Variable data rate timing allows for a flexible data frequency. It provides the ability to vary the frequency of the bit clocks, which can be asynchronous in the case of the M5914, or synchronous in the case of the M5913 from 64 KHz to 4.096 MHz. Master clocks inputs are still restricted to 1.536, 1.544, or 2.048 MHz.

In this mode, $DCLK_R$ and $DCLK_X$ become the data clocks for the receive and transmit PCM highways. While FS_X is high, PCM data from D_X is transmitted onto the highway on the next eight consecutive positive transitions of $DCLK_X$. Similary, while FS_R is high, each PCM bit from the highway is received by D_R on the next eight consecutive negative transition of $DCLK_R$.

On the transmit side, the PCM word will be repeated in all remaining timeslots in the 125 s frame as long as $DCLK_X$ is pulsed and FS_X is held high. This feature allows the PCM word to be transmitted to the PCM highway more than once per frame, if desired, and is only available in the variable data rate mode. Conversely, signaling is only allowed in the fixed data rate mode since the variable mode provides no means with which to specify a signaling frame.

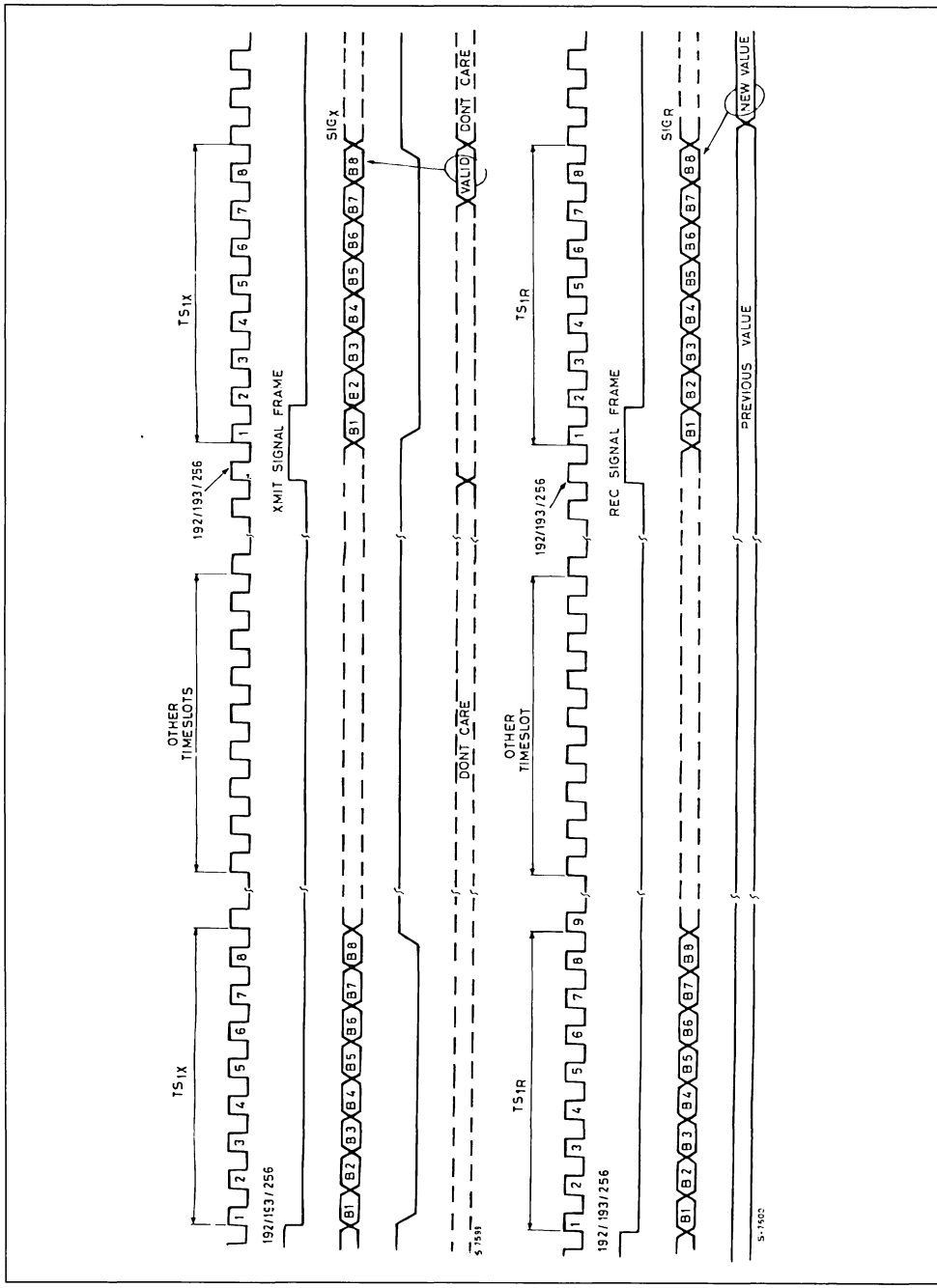
SIGNALING

Signaling can only be performed with the 24-pin device in the fixed data rate timing mode ($DCLK_R = V_{BB}$). Signaling frames on the transmit and receive sides are independent of one another and are selected by a double-width frame sync pulse on the appropriate channel. During a transmit signaling frame, the codec will encode the incoming analog signal and substitute the signal present on SIG_X for the least significant bit of the encoded PCM word. Similarly, in a receive signaling frame, the codec will decode the seven most significant bits according to CCITT recommendation G.733 and output the logical state of the LSB on the SIG_R lead until it is updated in the next signaling frame. Timing relationships for signaling operation are shown in figure 4.

ASYNCHRONOUS OPERATION

The M5914 can be operated with asynchronous clocks in either the fixed or variable data rate modes. In order to avoid crosstalk problems associated with special interrupt circuitry the design of the M5913/M5914 combochip includes separate digital-

Figure 4 : Signaling Timing (used only with fixed data rate mode).



to-analog converters and voltage references on the transmit and receive sides to allow completely independent operation of the two channels.

In either timing mode, the master clock, data clock, and timeslot strobe must be synchronized at the beginning of each frame. Specifically, in variable data rate mode the rising edge of CLK_X must occur within t_{FSD} nanoseconds before the rise of FS_X, while the leading edge of $DCLK_X$ must occur within t_{TSDX} nanoseconds of the rise of FS_X. Thus, CLK_X and $DCLK_X$ are synchronized once per frame but may be of different frequencies. The receive channel operates in a similar manner and is completely independent of the transmit timing (refer to Variable Data Rate Timing Diagram). This approach requires the provision of two separate master clocks, even in variable data rate mode, but avoids the use of a synchronizer which can cause intermittent data conversion errors.

ANALOG LOOPBACK

A distinctive feature of the M5914 is its analog loopback capability. This feature allows the user to send a control signal which internally connects the analog input and output ports. As shown in figure 5, when LOOP is TTL high the receive output (PWRO+) is internally connected to VF_XI+, GS_R in internally connected to PWRO- and VF_XI- is internally connected to GS_X.

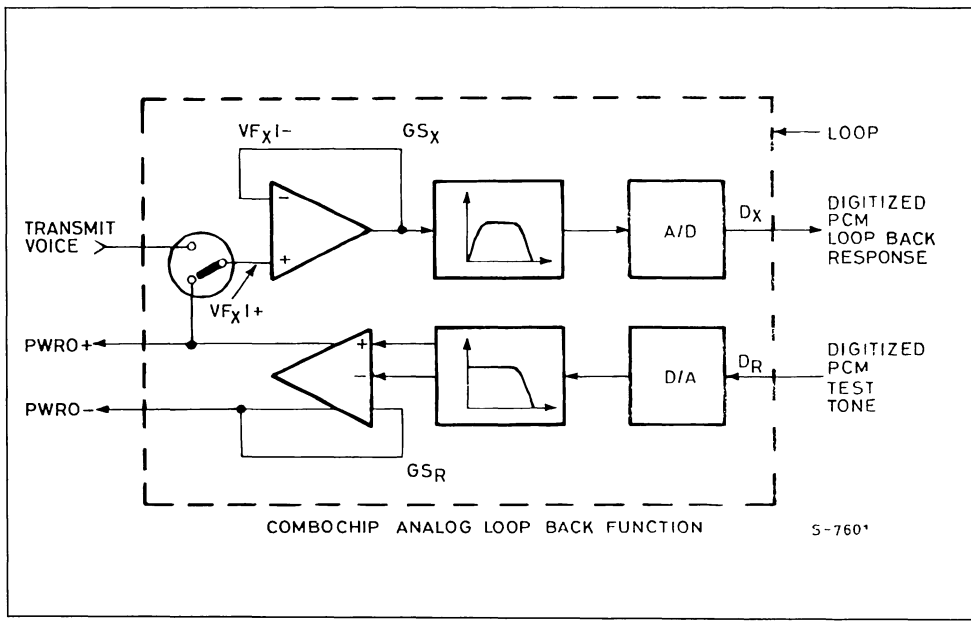
With this feature, the user can test the line circuit remotely by comparing the digital codes sent into the receive channel (D_R) with those generated on the transmit channel (D_X). Due to the difference in transmission levels between the transmit and receive sides, a0 dBm0 code sent into D_R will emerge from D_X as a + 3 dBm0 code, an implicit gain of 3 dB. Thus, the maximum signal input level which can be tested using analog loopback is 0 dBm0.

PRECISION VOLTAGE REFERENCE

No external components are required with the combochip to provide the voltage reference function. Voltage references are generated on-chip and are calibrated during the manufacturing process. The technique use the bandgap principle to derive a temperature and bias stable reference voltage. These references determine the gain and dynamic range characteristics of the device.

Separate references are supplied to the transmit and receive sections. Transmit and receive section are trimmed independently in the filter stages to a final precision value. With this method the combochip can achieve manufacturing tolerances of typically ±0.04 dB in absolute gain for each half chan-

Figure 5 : Simplified Block Diagram of M5914 Combship in the Analog Loopback Configuration.



nel, providing the user a significant margin for error in other board components.

CONVERSION LAWS

The M5913 and M5914 are designed to operate in both μ-law and A-law systems. The user can select either conversion law according to the voltage present on the SIG_X/ASEL pin. In each case the coder and decoder process a companded 8-bit PCM word following CCITT recommendation G.711 for μ-law and A-law conversion. If A-law operation is desired, SIG_X should be tied to V_{BB}. Thus, signaling is not allowed during A-law operation. If μ= 255-law operation is selected, then SIG_X is a TTL level input which modifies the LSB on the PCM output in signaling frames.

TRANSMIT OPERATION

TRANSMIT FILTER

The input section provides gain adjustment in the passband by means of an on-chip uncommitted operational amplifier. This operational amplifier has a common mode range of 2.17 volts, a maximum DC offset of 25 mV, a minimum voltage gain of 5000, and a unity gain bandwidth of typically 1 MHz. Gain of up to 20 dB can be set without degrading the performance of the filter. The load impedance to ground (GRDA) at the amplifier output (GS_X) must be greater than 10 kilohms in parallel with less than 50 pF. The input signal on lead VF_XI+ can be either AC or DC coupled. The input op amp can also be used in the inverting mode or differential amplifier mode (see figure 6).

A low pass anti-aliasing section is included on-chip. This section typically provides 35 dB attenuation at the sampling frequency. No external components are required to provide the necessary anti-aliasing function for the switched capacitor section of the transmit filter.

The passband section provides flatness and stopband attenuation which fulfills the AT & T D3/D4 channel bank transmission specification and CCITT recommendation G.712. The M5913 and M5914 specifications meet or exceed digital class 5 central office switching systems requirements. The transmit filter transfer characteristics and specifications will be within the limits shown in the relative table.

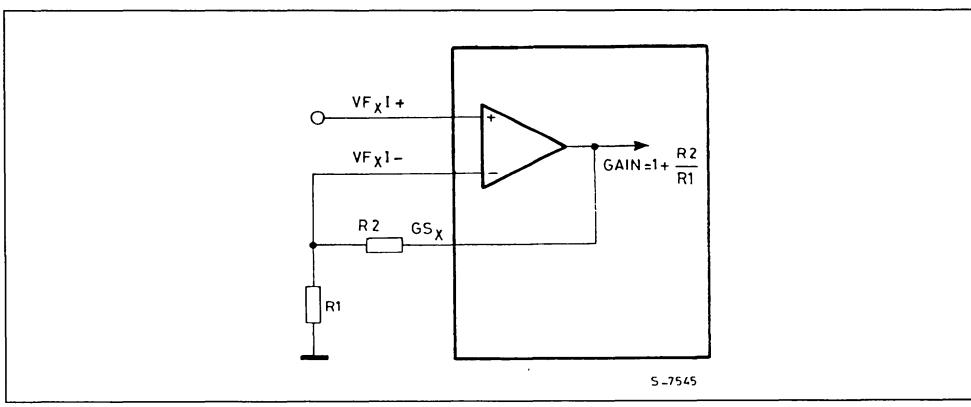
A high pass section configuration was chosen to reject low frequency noise from 50 and 60 Hz power lines, 17 Hz European electric railroads, ringing frequencies and their harmonics, and other low frequency noise. Even though there is high rejection at these frequencies, the sharpness of the band edge gives low attenuation at 200 Hz. This feature allows the use of low-cost transformer hybrids without external components.

ENCODING

The encoder internally samples the output of the transmit filter and holds each sample on an internal sample and hold capacitor. The encoder then performs an analog to digital conversion on a switched capacitor array. Digital data representing the sample is transmitted on the first eight data clock bits of the next frame.

An on-chip autozero circuit corrects for DC-offset on the input signal to encoder. This autozero circuit uses the sign bit averaging technique. In this way, all DC offset is removed from the encoder input waveform.

Figure 6 : Transmit Filter Gain Adjustment.



RECEIVE OPERATION

DECODING

The PCM word at the D_R lead is serially fetched on the first eight data clock bits of the frame. A D/A conversion is performed on the digital word and the corresponding analog sample is held on an internal sample and hold capacitor. This sample is then transferred to the receive filter.

RECEIVE FILTER

The receive section of the filter provides passband flatness and stopband rejection which fulfills both the AT & T D3/D4 specification and CCITT recommendation G.712. The filter contains the required compensation for the (sin X)/X response of such decoders. The receive filter characteristics and specifications are shown in the relative table.

RECEIVE OUTPUT POWER AMPLIFIERS

A balanced output amplifier is provided in order to allow maximum flexibility in output configuration. Either of the two outputs can be used single ended (referenced to GRDA) to drive single ended loads. Alternatively, the differential output will drive a bridged load directly. The output stage is capable of driving loads as low as 300Ω single ended to a level of 12 dBM or 600Ω differentially to a level of 15 dBM.

The receive channel transmission level may be adjusted between specified limits by manipulation of the GS_R input. GS_R is internally connected to an analog gain setting network. When GS_R is strapped to PWRO–, the receive level is maximized ; when it is tied to PWRO+, the level is minimized. The output transmission level interpolates between 0 and –12 dB as GS_R is interpolated (with potentiometer) between PWRO– and PWRO+. The use of the output gain set is illustrated in figure 7.

Transmission levels are specified relative to the receive channel output under digital milliwatt conditions, that is, when the digital input at D_R is the eight-code sequence specified in CCITT recommendation G.711.

OUTPUT GAIN SET : DESIGN CONSIDERATIONS

(refer to figure 7)

PWRO+ and PWRO– are low impedance complementary outputs. The voltages at the nodes are :

Vo+ at PWRO+

Vo at PWRO

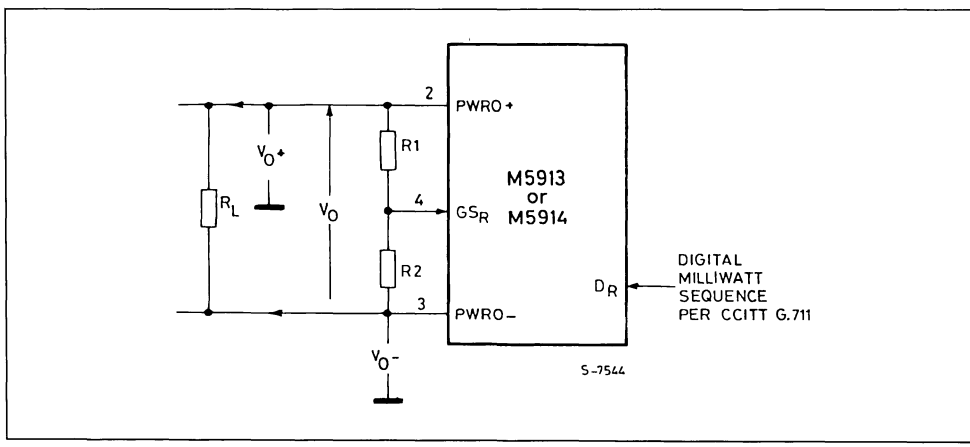
Vo = Vo+ Vo– (total differential response)

R1 and R2 are a gain setting resistor network with the center tap connected to the GS_R input. A value greater than 10 KΩ and less than 100KΩ for R1 + R2 is recommended because :

a) The parallel combination of R1 + R2 and R_L sets the total loading.

b) The total capacitance at the GS_R input and the parallel combination of R1 and R2 define a time constant which has to be minimized to avoid inaccuracies.

Figure 7 : Gain Setting Configuration.



If V_A represents the output voltage without any gain setting resistor network connected, you can have :

$$Vo = AV_A$$

where $A = \frac{1 + (R_1/R_2)}{4 + (R_1/R_2)}$

For design purposes, a useful form is R1/R2 as a function of A.

$$R1/R2 = \frac{4A - 1}{1 - A}$$

(allowable values for A are those which make R1/R2 positive)

Examples are :

If A = 1 (maximum output), then

R1/R2 = ∞ or $V(GS_R) = Vo$;

i.e., GS_R is tied to PWRO-

If A = 1/2, then

R1/R2 = 2

If A = 1/4 (minimum output) then

R1/R2 = 0 or $V(GS_R) = Vo+$;

i.e., GS_R is tied to PWRO+

DC CHARACTERISTICS (T_{amb} = 0 °C to 70 °C, V_{CC} = + 5 ± 5 %, V_{BB} = – 5 V ± 5 %, GRDA = 0 V, unless otherwise specified) Typical values are for T_{amb} = 25 °C and nominal power supply values.

DIGITAL INTERFACE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{IL}	Low Level Input Current	GRDD ≤ V_{IN} ≤ V_{IL} (note[1])			10	µA
I_{IH}	High Level Input Current	V_{IH} ≤ V_{IN} ≤ V_{CC}			10	µA
V_{IL}	Input Low Voltage, Except CLKSEL				0.8	V
V_{IH}	Input High Voltage, Except CLKSEL		2.0			V
V_{OL}	Output Low Voltage	I_{OL} = 3.2 mA at D_X $\overline{TS_X}$ and SIG_R			0.4	V
V_{OH}	Output High Voltage	I_{OH} = 9.6 mA at D_X I_{OH} = 1.2 mA at SIG_R	2.4			V
V_{ILO}	Input Low Voltage, CLKSEL[2]		V_{BB}		V_{BB}+0.5	V
V_{IIO}	Input Intermediate Voltage, CLKSEL		GRDD – 0.5		0.5	V
V_{IHO}	Input High Voltage, CLKSEL		V_{CC}–0.5		V_{CC}	V
C_{OX}	Digital Output Capacitance[3]			5		pF
C_{IN}	Digital Input Capacitance			5	10	pF

Notes : 1. V_{IN} is the voltage on any digital pin

2 SIG_X and $DCLK_R$ are TTL level inputs between GRDD and V_{CC} ; they are also pinstraps for mode selection when tied to V_{BB} Under these conditions V_{ILO} is the input low voltage requirement.

3 Timing parameters are guaranteed based on a 100 pF load capacitance. Up to eight digital outputs may be connected to a common PCM highway without buffering, assuming a board capacitance of 60 pF

DC CHARACTERISTIC (continued)

POWER DISSIPATION All measurements made at f_{DCLK} = 2.048 MHz, outputs unloaded.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{CC1}	V_{CC} Operating Current			6	10	mA
I_{BB1}	V_{BB} Operating Current			6	9	mA
I_{CC0}	V_{CC} Power Down Current	PDN ≤ V_{IL} ; after 10 µs		40	300	µA
I_{BB0}	V_{BB} Power Down Current	PDN ≤ V_{IL} ; after 10 µs		40	300	µA
I_{CCS}	V_{CC} Standby Current	FS_X, FS_R ≤ V_{IL} ; after 30 ms		300	600	µA
I_{BBS}	V_{BB} Standby Current	FS_X, FS_R ≤ V_{IL} ; after 30 ms		40	300	µA
P_{D1}	Operating Power Dissipation			60	100	mW
P_{D0}	Power Down Dissipation	PDN ≤ V_{IL} ; after 10 µs		0.4	3	mW
P_{ST}	Standby Power Dissipation	FS_X, FS_R ≤ V_{IL} ; after 30 ms		1.7	5	mW

Notes : 1. V_{IN} is the voltage on any digital pin
2. SIG_X and $DCLK_R$ are TTL level inputs between GRDD and V_{CC} , they are also pinstraps for mode selection when tied to V_{BB} Under these conditions V_{ILO} is the input low voltage requirement
3 Timing parameters are guaranteed based on a 100 pF based on a 100 pF load capacitance. Up to eight digital outputs may be connected to a common PCM highway without buffering, assuming a board capacitance of 60 pF

ANALOG INTERFACE, TRANSMIT FILTER INPUT STAGE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{BX1}	Input Leakage Current VF_XI+, VF_XI-	– 2.17 V ≤ V_{IN} ≤ 2.17 V			100	nA
R_{IXI}	Input Resistance, VF_XI+, VF_XI-		10			MΩ
V_{OSXI}	Input Offset Voltage, VF_XI+, VF_XI-				25	mV
CMRR	Common Mode Rejection, VF_XI+, VF_XI-	– 2.17 ≤ V_{IN} ≤ 2.17 V	55			dB
A_{VOL}	DC Open Loop Voltage Gain, GS_X	R_L = 10 KΩ	5000	20.000		
f_C	Open Loop Unity Gain Bandwidth, GS_X			1		MHz
V_{OXI}	Output Voltage Swing GS_X	R_L ≥ 10 kΩ	2.17		– 2.17	V
C_{LXI}	Load Capacitance, GS_X				50	pF
R_{LXI}	Minimum Load Resistance, GS_X		10			kΩ

DC CHARACTERISTIC (continued)

ANALOG INTERFACE, RECEIVE FILTER DRIVER AMPLIFIER STAGE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
R_{ORA}	Output Resistance, PWRO+, PWRO–			1		Ω
V_{OSRA}	Single Ended Output DC Offset, PWRO+, PWRO–	Relative to GRDA	– 150	75	150	mV
C_{LRA}	Load Capacitance, PWRO+, PWRO–				100	pF

AC CHARACTERISTICS - TRANSMISSION PARAMETERS

Unless otherwise noted, the analog input is a 0 dBm0, 1020 Hz sine wave[1]. Input amplifier is set for unity gain, noninverting. The digital input is a PCM bit stream generated by passing a 0 dBm0, 1020 Hz sine wave through an ideal encoder. Receive output is measured single ended, maximum gain configuration[2]. All output levels are (sin X)/X corrected.

GAIN AND DYNAMIC RANGE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
EmW	Encoder Milliwatt Response (transmit gain tolerance)	T_{amb} = 25 °C ; V_{BB} = – 5 V ; V_{CC} = 5 V	– 0.15	± 0.04	0.15	dBmO
EmW_{TS}	EmW Variation with Temperature and Supplies	± 5 % Supplies, 0 to 70 °C Relative to Nominal Condition	– 0.12		0.12	dB
DmW	Digital Milliwatt Response (receive gain tolerance)	T_{amb} = 25 °C, V_{BB} = – 5 V ; V_{CC} = 5 V	– 0.15	± 0.04	0.15	dBmO
DmW_{TS}	DmW Variation with Temperature and Supplies	± 5 %, 0 to 70 °C	– 0.08		0.08	dB
0 TLP_{1X}	Zero Transmission Level Point Transmit Channel (0dBm0) μ-law	600 Ω Load 900 Ω Load		2.76 1.00		dBm dBm
0 TLP_{2X}	Zero Transmission Level Point Transmit Channel (0 dBm0) A-law	600 Ω Load 900 Ω Load		2.79 1.03		dBm dBm
$0TLP_{1R}$	Zero Receive Level Point Receive Channel (0 dBm0) μ-law	600 Ω Load 900 Ω Load		5.76 4.00		dBm dBm
$0TLP_{2R}$	Zero Receive Level Point Receive Channel (0 dBm0) A-law	600 Ω Load 900 Ω Load		5.79 4.03		dBm dBm

Note : 1. 0 dBm0 is defined as the zero reference point of the channel under test (0 TLP). This corresponds to an analog signal input of 1.064 V_{rms} or an output of 1.503 V_{rms} (μ-Law) dual 1.068 V_{rms} or an output 1.516 V_{rms} (A-Law).

2. Unity gain input amplifier : GS_X is connected to VF_XI, Signal input VF_XI+ , Maximum gain output amplifier : GS_R is connected to PWRO, output to PWRO+.

AC CHARACTERISTIC (continued)

GAIN TRACKING

Reference Level = – 10 dBm0

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$GT1_X$	Transmit Gain Tracking Error Sinusoidal Input ; μ-law	3 to – 40 dBm0 – 40 to – 50 dBm0 – 50 to – 55 dBm0			± 0.2 ± 0.4 ± 1.0	dB dB dB
$GT2_X$	Transmit Gain Tracking Error Sinusoidal Input ; A-law	3 to – 40 dBm0 – 40 to – 50 dBm0 – 50 to – 55 dBm0			± 0.2 ± 0.4 ± 1.0	dB dB dB
$GT1_R$	Receive Gain Tracking Error Sinusoidal Input ; μ-law	3 to – 40 dBm0 – 40 to – 50 dBm0 – 50 to – 55 dBm0			± 0.2 ± 0.4 ± 1.0	dB dB dB
$GT2_R$	Receive Gain Tracking Error Sinusoidal Input ; A-law	3 to – 40 dBm0 – 40 to – 50 dBm0 – 50 to – 55 dBm0			± 0.2 ± 0.4 ± 1.0	dB dB dB

NOISE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
N_{XC1}	Transmit Noise, C-message Weighted	VF_XI+ = GRDA VF_XI- = GS_X		0	13	dBrnc0
N_{XC2}	Transmit Noise, C-message Weighted with Eighth Bit Signaling	VF_XI+ = GRDA VF_XI- = GS_X ; 6 th Frame Signaling		13	18	dBrnc0
N_{XP}	Transmit Noise, Psophometrically Weighted	VF_XI+ = GRDA VF_XI- = GS_X		(1)*	– 80	dBm0p
N_{RC1}	Receive Noise C-message Weighted : Quiet Code	D_R = 11111111 Measure at PWRO+		1	9	dBrnc0
N_{RC2}	Receiver Noise, C-message Weighted : Sign Bit Toggle	Input to D_R is Zero Code with Sign Bit Toggle at 1 kHz Rate		1	10	dBrnc0
N_{RP}	Receive Noise, Psophometrically Weighted	D_R = Lowest Positive Decode Level		– 90	– 81	dBm0p
N_{SF}	Single Frequency NOISE End to End Measurement	CCITT G.712.4.2			– 50	DBM0
$PSRR_1$	V_{CC} Power Supply Rejection, Transmit Channel	Idle Channel ; 200 mV P-P Signal on Supply ; 0 to 50 kHz, Measure at D_X		– 40		dB
$PSRR_2$	V_{BB} Power Supply Rejection, Transmit Channel	Idle Channel ; 200 mV P-P Signal on Supply ; 0 to 50 kHz, Measure at D_X		– 40		dB
$PSRR_3$	V_{CC} Power Supply Rejection, Receive Channel	Idle Channel ; 200 mV P-P Signal on Supply ; Measure Narrow Band at PWRO+ Single Ended, 0 to 50 kHz		– 40		dB
$PSRR_4$	V_{BB} Power Supply, Rejection Receive Channel	Idle Channel ; 200 mV P-P Signal on Supply ; Measure Narrow Band at PWRO+ Single Ended, 0 to 50 kHz		– 40		dB

(1) * Noise free : DX PCM Code stable at 01010101.

AC CHARACTERISTIC (continued)

NOISE (continued)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
CT_{TR}	Crosstalk, Transmit to Receive, Single Ended Outputs	VF_XI+ = 0 dBm0, 1.02 kHz, D_R = Lowest Positive Decode Level, Measure at PWRO+			– 80	dB
CT_{RT}	Crosstalk, Receive to Transmit, Single Ended Outputs	D_B = 0 dBm0, 1.02 kHz, VF_XI+ = GRDA, measure at D_X			– 80	dB

DISTORTION

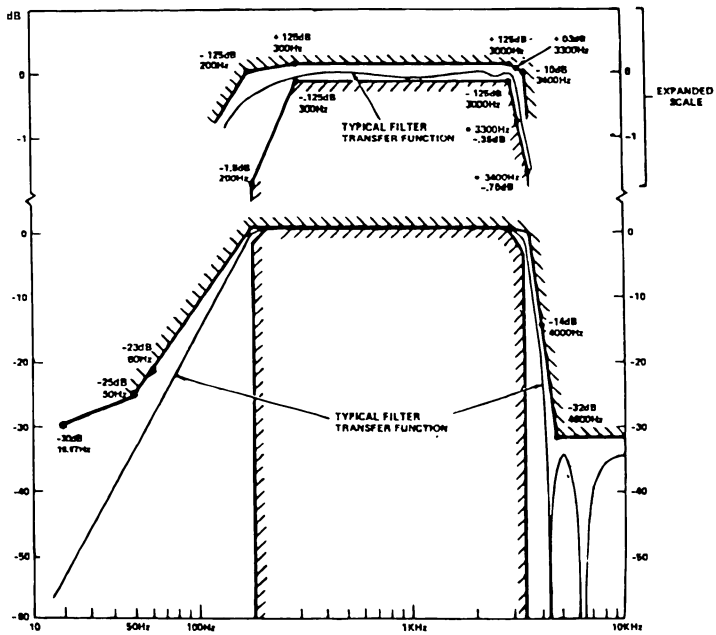
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$SD1_X$	Transmit Signal to Distortion, μ-law Sinusoidal Input ; CCITT G, 712-method 2	0 ≤ VF_XI+ ≤ – 30 dBm0 – 40 dBm0 – 45 dBm0	36 30 25			dB dB dB
$SD2_X$	Transmit Signal to Distortion, A-law Sinusoidal Input CCITT G, 712-method 2	0 ≤ VF_XI+ ≤ – 30 dBm0 – 40 dBm0 – 45 dBm0	36 30 25			dB dB dB
$SD1_R$	Transmit Signal to Distortion, μ-law Sinusoidal Input ; CCITT G, 712-method 2	0 ≤ VF_XI+ ≤ – 30 dBm0 – 40 dBm0 – 45 dBm0	36 30 25			dB dB dB
$SD2_R$	Receive Signal to Distortion, A-law Sinusoidal Input ; CCITT G, 712-method 2	0 ≤ VF_XI+ ≤ – 30 dBm0 – 40 dBm0 – 45 dBm0	36 30 25			dB dB dB
DP_{X1}	Transmit Single Frequency Distortion Products	AT & T Adivisory # 64 (3.8) 0 dBm0 Input Signal			– 46	dB
DP_{R1}	Receive Single Frequency Distortion Products	AT & T Adivisory # 64 (3.8) 0 dBm0 Input Signal			– 46	dB
IMD_1	Intermodulation Distortion, End to End Measurement	CCITT G.712 (7.1)			– 35	dB
IMD_2	Intermodulation Distortion, End to End Measurement	CCITT G.712 (7.2)			– 49	dB
SOS	Spurious out of Band Signals, End to End Measurement	CCITT G.712 (6.1)			– 30	dBm0
SIS	Spurious in Band Signals, End to End Measurement	CCITT G.712 (9)			– 40	dBm0
D_{AX}	Transmit Absolute Delay	Fixed Data Rate CLK_X = 2.048 MHz ; 0 dBm0, 1.02 kHz Signal at VF_XI+ Measure at D_X		300		μs
D_{DX}	Transmit Differential Envelope Delay Relative to D_{AX}	f = 500 – 600 Hz f = 600 – 1000 Hz f = 1000 – 2600 Hz f = 2600 – 2800 Hz		170 95 45 80		μs μs μs μs
D_{AR}	Receive Absolute Delay	Fixed data rate, CLK_R = 2.048 MHz ; digital input is DMW codes. Measure at PWRO+			190	μs
D_{DR}	Receive Differential Envelope Delay Relative to D_{AR}	f = 500 – 600 Hz f = 600 – 1000 Hz f = 1000 – 2600 Hz f = 2600 – 2800 Hz		10 10 85 110		μs μs μs μs

AC CHARACTERISTIC (continued)

TRANSMIT FILTER TRANSFER CHARACTERISTICS
Input amplifier is set for unity gain, noninverting ; maximum gain output.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
G_{RX}	Gain Relative to Gain at 1.02 kHz	0 dBm0 Signal Input at VF_XI+				
	16.67 Hz				– 30	dB
	50 Hz				– 25	dB
	60 Hz				– 23	dB
	200 Hz		– 1.8		– 0.125	dB
	300 to 3000 Hz		– 0.125		0.125	dB
	3300 Hz		– 0.35		0.03	dB
	3400 Hz		– 0.7		– 0.10	dB
	4000 Hz				– 14	dB
	4600 Hz and Above				– 32	dB

Figure 8 : Transmit Filter.

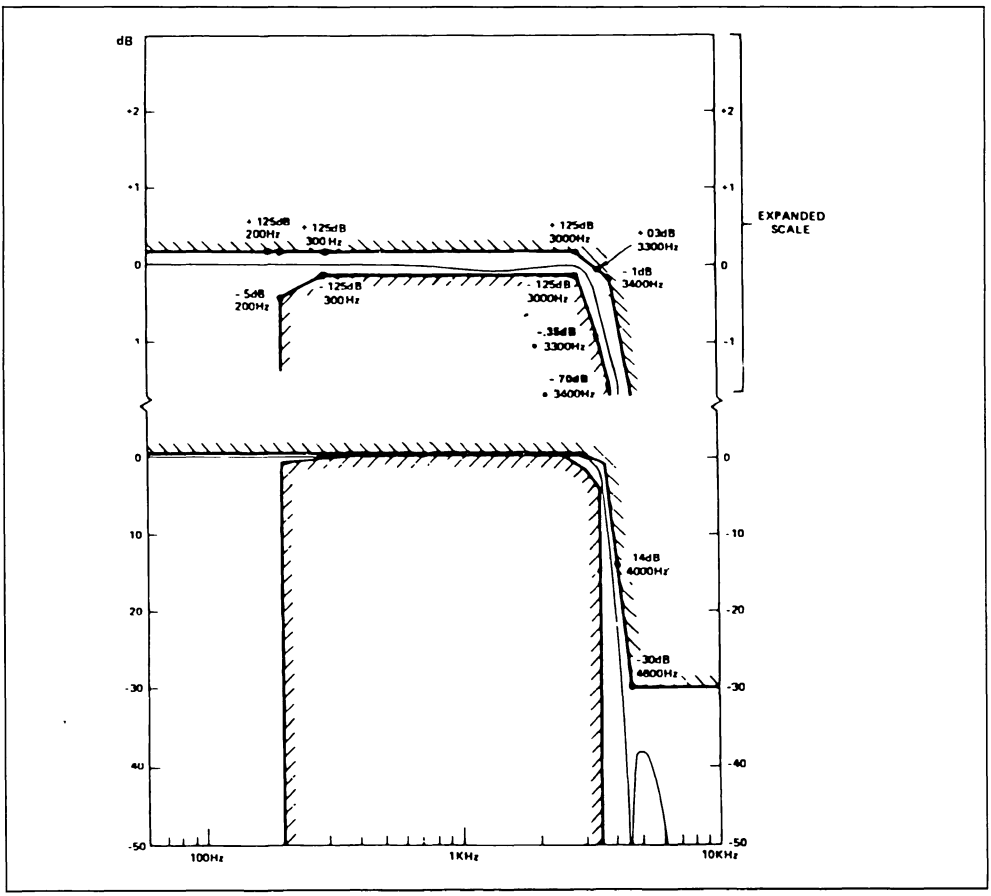


AC CHARACTERISTIC (continued)

RECEIVE FILTER TRANSFER CHARACTERISTICS

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
G_{RR}	Gain Relative to Gain at 1.02 kHz	0 dBm0 Signal Input at D_R				
	below 200 Hz				0.125	dB
	200 Hz		– 0.5		0.125	dB
	300 to 3000 Hz		– 0.125		0.125	dB
	3300 Hz		– 0.35		0.03	dB
	3400 Hz		– 0.7		– 0.1	dB
	4000 Hz				– 14	dB
	4600 Hz and Above				– 30	dB

Figure 9 : Receive Filter.



AC CHARACTERISTICS - TIMING PARAMETERS

CLOCK SECTION

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
t_{CY}	Clock Period, CLK_X, CLK_R	$f_{CLKX} = f_{CLKR} = 2.048$ MHz	488			ns
t_{CLK}	Clock Pulse Width	CLK_X, CLK_R	195			ns
t_{DCLK}	Data Clock Pulse Width[1]	64 kHz ≤ f_{DCLK} ≤ 2.048 MHz	195			ns
t_{CDC}	Clock Duty Cycle	CLK_X, CLK_R	40	50	60	%
t_r, t_f	Clock Rise and Fall Time		5		30	ns

TRANSMIT SECTION, FIXED DATA RATE MODE[2]

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
t_{DZX}	Data Enabled on TS Entry	0 < C_{LOAD} < 100 pF	0		145	ns
t_{DDX}	Data Delay from CLK_X	0 < C_{LOAD} < 100 pF	0		145	ns
t_{HZX}	Data Float on TS Exit	C_{LOAD} = 0	60		190	ns
t_{SON}	Timeslot X to Enable	0 < C_{LOAD} < 100 pF	0		145	ns
t_{SOFF}	Timeslot X to Disable	C_{LOAD} = 0	50		190	ns
t_{FSD}	Frame Sync Delay		0		120	ns
t_{SS}	Signal Setup Time		0			ns
t_{SH}	Signal Hold Time		0			ns

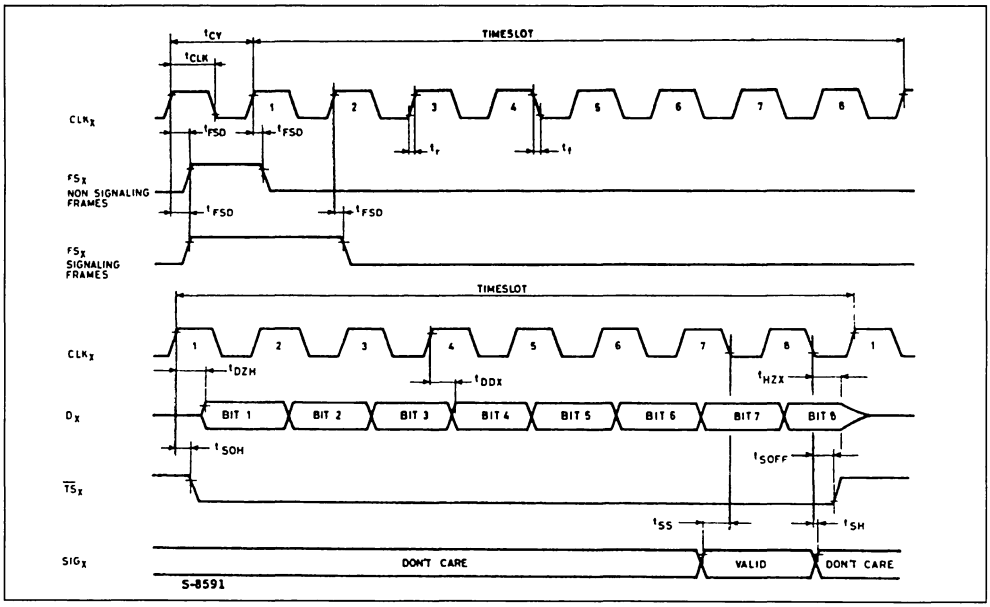
RECEIVE SECTION, FIXED DATA RATE MODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
t_{DSR}	Receive Data Setup		10			ns
t_{DHR}	Receive Data Hold		60			ns
t_{FSD}	Frame Sync Delay		0		120	ns
t_{SIGR}	SIG_R Update		0		2	µs

Notes : 1. Devices are available wich operate at data rates up to 4.096 MHz , the minimum data clock pulse width for these devices is 110 ns.
2. Timing parameters t_{DZX}, t_{HZX}, and t_{SOFF} are referenced to a high impedance state.

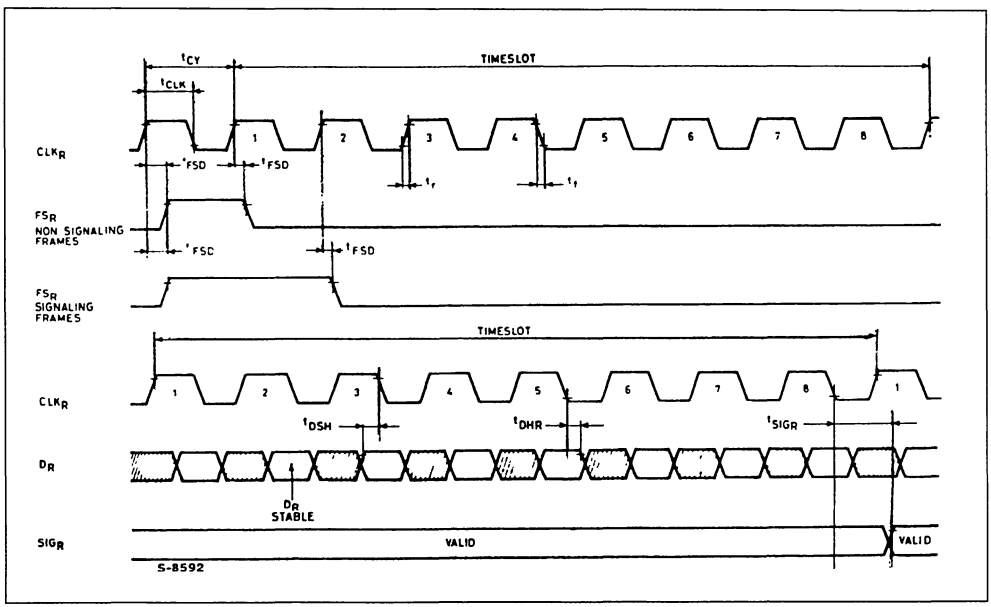
WAVEFORMS

Fixed Data Rata Timing - Transmit Timing



Note : All timing parameters referenced to V_{IH} and V_{IL} except t_{DZX}, t_{SOFF} and t_{HZX} which reference a high impedance state.

Receive Timing



Note : All timing parameters referenced to V_{IH} and V_{IL}.

AC CHARACTERISTICS (continued)

TRANSMIT SECTION, VARIABLE DATA RATE MODE[1]

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
t_{TSDX}	Timeslot Delay from $DCLK_X$		– 80		80	ns
t_{FSD}	Frame Sync Delay		0		120	ns
t_{DDX}	Data Delay from $DCLK_X$	$0 < C_{LOAD} < 100$ pF	0		100	ns
t_{DON}	Timeslot to D_X Active	$0 < C_{LOAD} < 100$ pF	0		50	ns
t_{DOFF}	Timeslot to D_X Inactive	$0 < C_{LOAD} < 100$ pF	0		80	ns
f_{DX}	Data Clock Frequency		64		2048[2]	kHz
t_{DFSX}	Data Delay from FS_X	$t_{TSDX} = 80$ ns	0		140	ns

RECEIVE SECTION, VARIABLE DATA RATE MODE

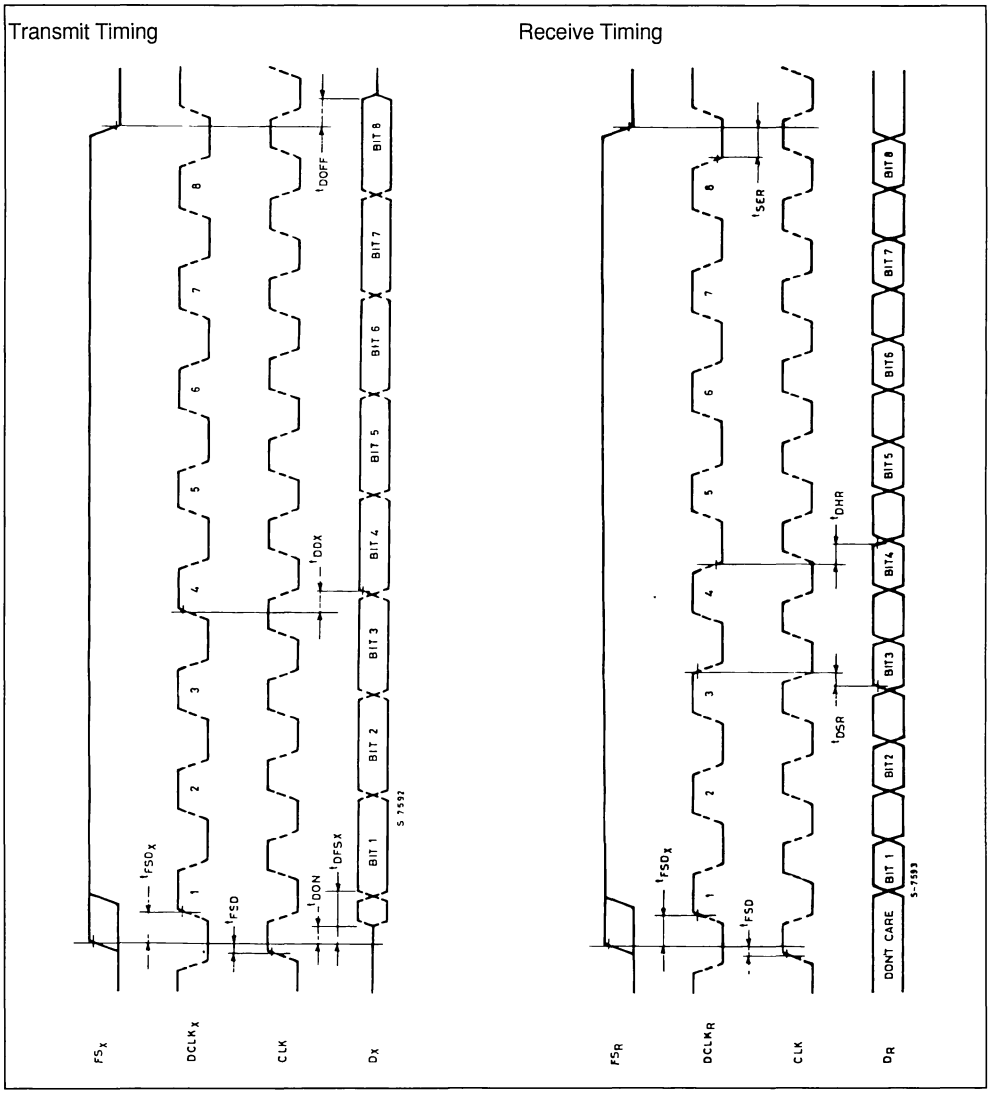
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
t_{TSDR}	Timeslot Delay from $DCLK_R$		– 80		80	ns
t_{FSD}	Frame Sync Delay		0		120	ns
t_{DSR}	Data Setup Time		10			ns
t_{DHR}	Data Hold Time		60			ns
f_{DR}	Data Clock Frequency		64		2048[2]	kHz
t_{SER}	Timeslot End Receive Time		0			ns

64 KB OPERATION, VARIABLE DATA RATE MODE

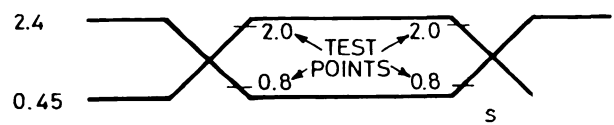
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
t_{FSLX}	Transmit Frame Sync Minimum Downtime	FS_X is TTL high for remainder of frame	488			ns
t_{FSLR}	Receive Frame Sync Minimum Downtime	FS_R is TTL high for remainder of frame	1952			ns
t_{DCLK}	Data Clock Pulse Width				10	µs

Notes : 1. Timing parameters t_{DON} and t_{DOFF} are referenced to a high impedance state.
2 Device are avalilable which operate at data rates up to 4.096 MHz.

VARIABLE DATA RATE TIMING



AC Testing Input, Output Waveform.



SINGLE CHIP PCM CODEC AND FILTER

- A-LAW, 2.048MHz MASTER CLOCK
- 300MIL 16-PIN PACKAGE FOR HIGHER LINE-CARD DENSITY
- AT&T D3/D4 AND CCITT COMPATIBLE
- VARIABLE TIMING MODE FOR FLEXIBLE DIGITAL INTERFACE : SUPPORTS DATA RATES FROM 64KB TO 4.096MB
- FIXED TIMING MODE FOR STANDARD 32-CHANNEL SYSTEMS : 2.048MHz MASTER CLOCK
- FULLY DIFFERENTIAL ARCHITECTURE ENHANCES NOISE IMMUNITY
- LOW POWER CMOS TECHNOLOGY
- 0.5mW TYPICAL POWER DOWN
- 70mW TYPICAL OPERATING
- ON CHIP AUTO ZERO, SAMPLE AND HOLD, AND PRECISION VOLTAGE REFERENCES

DESCRIPTION

The M5917 is a limited feature version of Intel's 2913 and 2914 combination codec/filter chips. They are fully integrated PCM codecs with transmit/receive filters fabricated in a highly reliable and proven silicon gate technology.

The primary applications for the M5917 is in telephone systems :

- Switching - Digital PBX's and Central Office Switching Systems
- Subscriber Instruments - Digital Handsets and Office Workstations

Other possible applications can be found where the wide dynamic range (78dB) and minimum conversion time (125µs) are required for analog to digital interface functions :

- High Speed Modems
- Voice Store and Forward
- Secure Communications
- Digital Echo Cancellation

Figure 1 : Pin Connection.

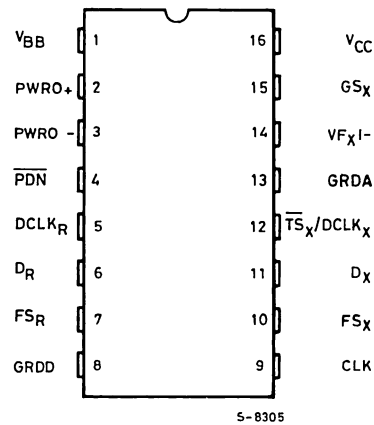


Figure 2 : Block Diagram.

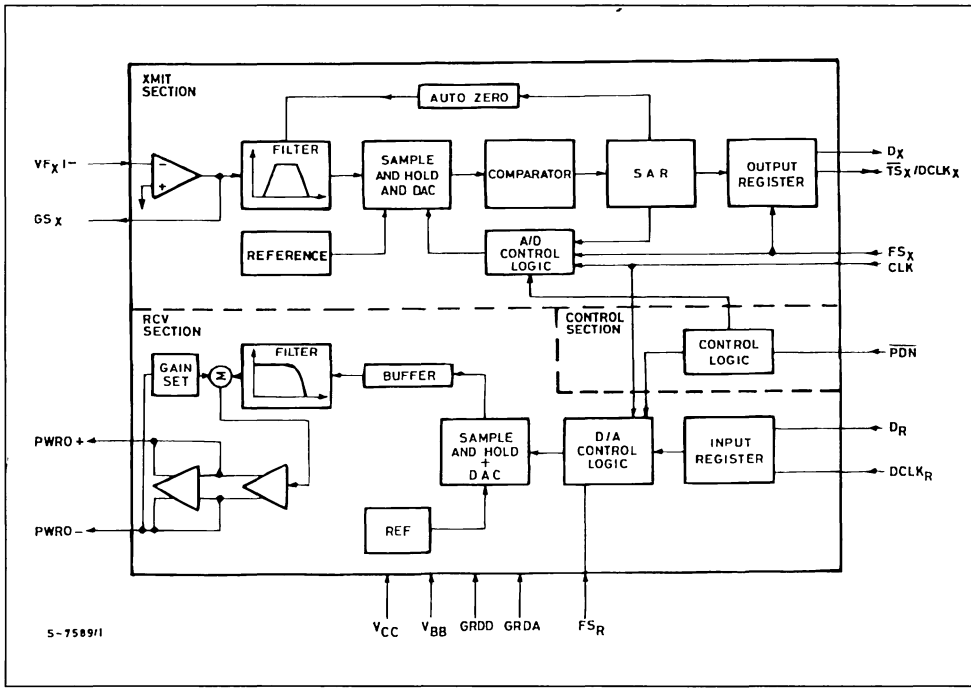


Table 1 : Pin Names.

V_{BB}	Power (– 5V)	GS_X	Transmit Gain Control
PWRO+, PWRO–	Power Amplifier Outputs	$VF_XI–$	Analog Input
$\overline{PDN}$	Power Down Select	GRDA	Analog Ground
$DCLK_R$	Receive Variable Data Clock	$\overline{TS_X}$	Timeslot Strobe/buffer Enable
D_R	Receive PCM Input	$DCLK_X$	Transmit Variable Data Clock
FS_R	Receive Frame	D_X	Transmit PCM Output
	Synchronization Clock	FS_X	Transmit Frame
GRDD	Digital Ground		Synchronization Clock
V_{CC}	Power (+ 5V)	CLK	Master Clock

Table 2 : Pin Description.

Symbol	Function
V_{BB}	Most Negative Supply. Input voltage is – 5 volts ± 5%.
PWRO+	Non-inverting Output of Power Amplifier. Can drive transformer hybrids or high impedance loads directly in either a differential or single ended configuration.
PWRO–	Inverting Output of Power Amplifier. Functionally identical and complementary to PWRO+.
$\overline{PDN}$	Power Down Select. When $\overline{PDN}$ is TTL high, the device is active.When low, the device is powered down.
$DCLK_R$	Selects the fixed or variable data rate mode. When $DCLK_R$ is connected to V_{BB}, the fixed data rate mode is selected. When $DCLK_R$ is not connected to V_{BB}, the device operates in the variable data rate mode. In this mode $DCLK_R$ becomes the receive data clock wich operates at TTL levels from 64kB to 4096MB data rates.
D_R	Receive PCM Input. PCM data is clocked in on this lead on eight consecutive negative transitions of the receive data clock ; CLK in the fixed data rate mode and $DCLK_R$ in variable data rate mode.
FS_R	8KHz frame synchronization clock input/timeslot enable, receive channel. In variable data rate mode this signal must remain high for the entire length of the timeslot. The receive channel enters the standby state whenever FS_R is TTL low for 30 miliseconds.
GRDD	Digital Ground for all Internal Logic Circuits. Not internally tied to GRDA.
CLK	Master and data clock for the fixed data rate mode ; master clock only in variable data rate mode.
FS_X	8KHz frame synchronization clock input/timeslot enable, transmit channel. Operates independently but in an analogous manner to FS_R. The transmit channel enters the standby state whenever FS_X is TTL low for 30 milliseconds.
D_X	Transmit PCM Output. PCM data is clocked out on this lead on eight consecutive positive transitions of the transmit data clock : CLK in fixed data rate mode and $DCLK_X$ in variable data rate mode.
$\overline{TS_X}/DCLK_X$	Transmit channel timeslot strobe (output) or data clock (input) for the transmit channel. In fixed data rate mode, this pin is an open drain output designed to be used as an enable signal for a three-state buffer variable data rate mode, this pin becomes the transmit data clock which operates at TTL levels from 64kB to 2.048MB data rates.
GRDA	Analog ground return for all internal voice circuits. Not internally connected to GRDD.
VF_XI-	Inverting analog input to uncommitted transmit operational amplifier.
GS_X	Output terminal of on-chip uncommitted op amp. Internally, this is the voice signal input to the transmit filter.
V_{CC}	Most positive supply ; input voltage is + 5 volts ± 5%.

FUNCTIONAL DESCRIPTION

The M5917 provides the analog-to-digital and the digital-to-analog conversion and the transmit and receive filtering necessary to interface a full duplex (4 wires) voice telephone circuit with the PCM highway of a time division multiplexed (TDM) system. It is intended to be used at the analog termination of a PCM line.

The following major functions are provided :

- Bandpass filtering of the analog signals prior to encoding and after decoding
- Encoding and decoding of voice and call progress information

GENERAL OPERATION

SYSTEM RELIABILITY FEATURES

The combochip can be powered up by pulsing FS_X and/or FS_R while a TTL high voltage is applied to PDN, provided that all clocks and supplies are connected. The M5917 has internal resets on power up (or when V_{BB} or V_{CC} are re-applied) in order to ensure validity of the digital outputs and thereby maintain integrity of the PCM highway.

On the transmit channel, digital outputs DX and $\overline{TS_X}$ are held in a high impedance state for approximately four frames (500µs) after power up or application

of V_{BB} or V_{CC}. After this delay, D_X and $\overline{TS}_X$ will be functional and will occur in the proper timeslot. The analog circuits on the transmit side require approximately 35 milliseconds to reach their equilibrium value due to the autozero circuit settling time.

To enhance system reliability, $\overline{TS}_X$ and D_X will be placed in a high impedance state approximately 20µs after an interruption of CLK.

POWER DOWN AND STANDBY MODES

To minimize power consumption, two power down modes are provided in which most M5917 functions are disabled. Only the power down, clock, and frame sync buffers, which are required to power up the device, are enabled in these modes. As shown in table 3, the digital outputs on the appropriate channels are placed in a high impedance state until the device returns to the active mode.

The Power Down mode utilizes an external control signal to the $\overline{PDN}$ pin. In this mode, power consumption is reduced to an average of 0.5mW. The device is active when the signal is high and inactive when it is low. In the absence of any signal, the $\overline{PDN}$ pin floats to TTL high allowing the device to remain active continuously.

The Standby mode leaves the user an option of powering either channel down separately or powering the entire down by selectively removing FS_X and/or FS_R. With both channels in the standby state, power consumption is reduced to an average of 1mW. If transmit only operation is desired, FS_X should be applied to the device while FS_R is held low. Similarly, if receive only operation is desired, FS_R should be applied while FS_X is held low.

Table 3 : Power-down Methods.

Device Status	Power-downMethod	DigitalOutputStatus
Power Down Mode	$\overline{PDN}$ = TTL low	$\overline{TS}_X$ and D_X are placed in a high impedance state within 10µs.
Standby Mode	FS_X and FS_R are TTL low.	$\overline{TS}_X$ and D_X are placed in a high impedance state within 30 milliseconds.
Only transmit is on standby.	FS_X is TTL low.	$\overline{TS}_X$ and DX are placed in a high impedance state within 30 milliseconds.
Only receive is on standby.	FS_R is TTL low.	

FIXED DATA RATE MODE

Fixed data rate timing, is selected by connecting $\overline{DCLK}_R$ to V_{BB}. It employs master clock CLK, frame synchronization clocks FS_X and FS_R, and output $\overline{TS}_X$.

CLK serves as the master clock to operate the codec and filter sections and as the bit clock to clock the data in and out from the PCM highway. FS_X and FS_R are 8kHz inputs which set the sampling frequency. $\overline{TS}_X$ is a timeslot strobe/buffer enable output which gates the PCM word onto the PCM highway when an external buffer is used to drive the line.

Data is transmitted on the highway at D_X on the first eight positive transitions of CLK following the rising edge of FS_X. Similarly, on the receive side, data is received on the first eight falling edges of CLK. The frequency of CLK must be 2.048MHz. No other frequency of operation is allowed in the fixed data rate mode.

VARIABLE DATA RATE MODE

Variable data rate timing is selected by connecting $DCLK_R$ to the bit clock for the receive PCM highway rather than to V_{BB}. It employs master clock CLK, bit clocks $DCLK_R$ and $DCLK_X$, and frame synchronization clocks FS_R and FS_X.

Variable data rate timing allows for a flexible data frequency. It provides the ability to vary the frequency of the bit clocks, from 64kHz to 4096MHz. The master clock is still restricted to 2.048MHz.

In this mode, $DCLK_R$ and $DCLK_X$ become the data clocks for the receive and transmit PCM highways. While FS_X is high, PCM data from D_X is transmitted onto the highway on the next eight consecutive positive transitions of $DCLK_X$. Similarly, while FS_R is high, each PCM bit from the highway is received by D_R on the next eight consecutive negative transitions of $DCLK_R$.

On the transmit side, the PCM word will be repeated in all remaining timeslots in the 125s frame as long as $DCLK_X$ is pulsed and FS_X is held high. This feature allows the PCM word to be transmitted to the PCM highway more than once per frame, if desi-red, and is only available in the variable data rate mode.

PRECISION VOLTAGE REFERENCES

No external components are required with the combochip to provide the voltage reference function. Voltage references are generated on-chip and are calibrated during the manufacturing process. The technique use the bandgap principle to derive a temperature and bias stable reference voltage. These references determine the gain and dynamic range characteristics of the device.

Separate references are supplied to the transmit and receive sections. Transmit and receive section are trimmed independently in the filter stages to a final precision value. With this method the combochip can achieve manufacturing tolerances of typically ± 0.04dB in absolute gain for each half channel, providing the user a significant margin for error in other board components.

TRANSMIT OPERATION

TRANSMIT FILTER

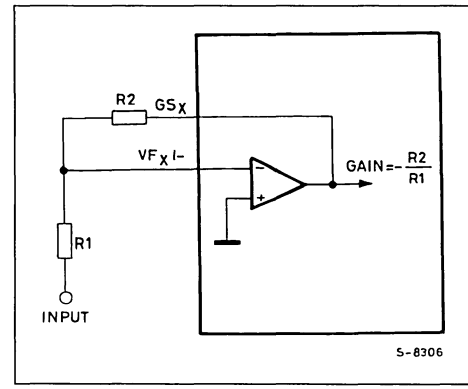
The input section provides gain adjustment in the passband by means of an on-chip uncommitted operational amplifier. This operational amplifier has a common mode range of 2.17 volts, a maximum DC offset of 25mV, a minimum voltage gain of 5000, and a unity gain bandwidth of typically 1MHz. Gain of up to 20dB can be set without degrading the performance of the filter. The load impedance to ground (GRDA) at the amplifier output (GS_X) must be greater than 10 kilohms in parallel high less than 50pF. The input signal on lead VF_XI can be either AC or DC coupled. The input op amp can only be used in the inverting mode as shown in figure 3.

A low pass anti-aliasing section is included on-chip. This section typically provides 35dB attenuation at the sampling frequency. No external components are required to provide the necessary anti-aliasing function for the switched capacitor section of the transmit filter.

The passband section provides flatness and stopband attenuation which fulfills the AT&T D3/D4 channel bank transmission specification and CCITT recommendation G.712. The M5917 specifications meet or exceed digital class 5 central office switching systems requirements. The transmit filter transfer characteristics and specifications will be within the limits shown in figure 4.

A high pass section configuration was chosen to reject low frequency noise from 50 and 60Hz power lines, 17Hz European electric railroads, ringing frequencies and their harmonics, and other low frequency noise. Even though there is high rejection at these frequencies, the sharpness of the band edge gives low attenuation at 200Hz. This feature allows the use of low-cost transformer hybrids without external components.

Figure 3 : Transmit Filter Gain Adjustment.



ENCODING

The encoder internally samples the output of the transmit filter and holds each sample on an internal sample and hold capacitor. The encoder then performs an analog to digital conversion on a switched capacitor array. Digital data representing the sample is transmitted on the first eight data clock bits of the next frame.

An on-chip autozero circuit corrects for DC-offset on the input signal to the encoder. This autozero circuit uses the sign bit averaging technique. In this way, all DC offset is removed from the encoder input waveform.

RECEIVE OPERATION

DECODING

The PCM word at the D_R lead is serially fetched on the first eight data clock bits of the frame. A D/A conversion is performed on the digital word and the corresponding analog sample is held on an internal sample and hold capacitor. This sample is then transferred to the receive filter.

RECEIVE FILTER

The receive section of the filter provides passband flatness and stopband rejection which fulfills both the AT&T D3/D4 specification and CCITT recommendation G.712. The filter contains the required compensation for the (sin x)/x response of such decoders. The receive filter characteristics and specifications will be within the limits shown in figure 5.

RECEIVE OUTPUT POWER AMPLIFIERS

A balanced output amplifier is provided in order to allow maximum flexibility in output configuration. Either of the two outputs can be used single ended (referenced to GRDA) to drive single ended loads. Alternatively, the differential output will drive a bridged load directly. The output stage is capable of driving loads as low as 300 ohms single ended to a level of 12dBm or 600 ohms differentially to a level of 15dBm.

Transmission levels are specified relative to the receive channel output under digital milliwatt conditions, that is, when the digital input at D_R is the eight-code sequence specified in CCITT recommendation G.711.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	With Respect GRDD, GRDA = 0V	− 0.6 to 7	V
V_{BB}	With Respect GRDD, GRDA = 0V	+ 0.6 to − 7	V
GRDD, GRDA	In Such Case : $0 \leq V_{CC} \leq +7V$, $-7V \leq V_{BB} \leq 0V$	± 0.3	V
$V_{I/O}$	Analog Inputs, Analog Outputs and Digital Inputs	$V_{BB} - 0.3 \leq V_{IN}/V_{OUT} \leq V_{CC} + 0.3$	V
V_{ODIG}	Digital Outputs	$GRDD - 0.3 \leq V_{OUT} \leq V_{CC} + 0.3$	V
T_{op}	Temperature Range	− 10 to + 80	°C
T_{stg}	Storage Temperature	− 65 to + 150	°C
P_{tot}	Power Dissipation	1	W

DC CHARACTERISTICS (T_A = 0°C to 70°C, V_{CC} = +5V ± 5%, V_{BB} = − 5V ± 5%, GRDA = 0V, GRDD = 0V, unless otherwise specified)
Typical values are for T_A = 25°C and nominal power supply values.

DIGITAL INTERFACE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{IL}	Low Level Input Current	$GRDD \leq V_{IN} \leq V_{IL}$ (note 1)			10	µA
I_{IH}	High Level Input Current	$V_{IH} \leq V_{IN} \leq V_{CC}$			10	µA
V_{IL}	Input Low Voltage				0.8	V
V_{IH}	Input High Voltage		2.0			V
V_{OL}	Output Low Voltage	I_{OL} = 3.2mA at D_X, $\overline{TS}_X$			0.4	V
V_{OH}	Output High Voltage	I_{OH} = 9.6mA at D_X	2.4			V
C_{OX}	Digital Output Capacitance[2]			5		pF
C_{IN}	Digital Input Capacitance			5	10	pF

POWER DISSIPATION All measurements made at f_{DCLK} = 2.048MHz, outputs unloaded.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{CC1}	V_{CC} Operating Current			6	10	mA
I_{BB1}	V_{BB} Operating Current			6	9	mA
I_{CC0}	V_{CC} Power Down Current	PDN ≤ V_{IL} ; after 10µs		40	300	µA
I_{BB0}	V_{BB} Power Down Current	PDN ≤ V_{IL} ; after 10µs		40	300	µA
I_{CCS}	V_{CC} Standby Current	FS_X, FS_R ≤ V_{IL} ; after 30ms		300	600	µA
I_{BBS}	V_{BB} Standby Current	FS_X, FS_R ≤ V_{IL} ; after 30ms		40	300	µA
P_{D1}	Operating Power Dissipation			60	100	mW
P_{D0}	Power Down Dissipation	PDN ≤ V_{IL} ; after 10µs		0.4	3	mW
P_{ST}	Standby Power Dissipation	FS_X, FS_R ≤ V_{IL} ; after 30ms		1.7	5	mW

Notes : 1. V_{IN} is the voltage on any digital pin.
2. Timing parameters are guaranteed based on a 100pF load capacitance. Up to eight digital outputs may be connected to a common PCM highway without buffering, assuming a board capacitance of 60pf.
3. With nominal power supply values.

ANALOG INTERFACE, TRANSMIT CHANNEL INPUT STAGE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{BX1}	Input Leakage Current, VF_XI-	– 2.17V ≤ V_{IN} ≤ 2.17V			100	nA
R_{IXI}	Input Resistance, VF_XI-		10			MΩ
V_{OSXI}	Input Offset Voltage, VF_XI-				25	mV
A_{VOL}	DC Open Loop Voltage Gain, GS_X	R_L = 10K	5000	20.000		
f_C	Open Loop Unity Gain Bandwidth, GS_X			1		MHz
V_{OXI}	Output Voltage Swing GS_X	R_L ≥ 10kΩ	– 2.17		2.17	V
C_{LXI}	Load Capacitance, GS_X				50	pF
R_{LXI}	Minimum Load Resistance, GS_X		10			kΩ

ANALOG INTERFACE, RECEIVE CHANNEL DRIVER AMPLIFIER STAGE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
R_{ORA}	Output Resistance, PWRO+, PWRO–			1		Ω
V_{OSRA}	Single-ended Output DC Offset, PWRO+, PWRO–	Relative to GRDA	– 150	75	150	mV
C_{LRA}	Load Capacitance, PWRO+, PWRO–				100	pF

A.C. CHARACTERISTICS - TRANSMISSION PARAMETERS

Unless otherwise noted, the analog input is a 0dBm0, 1020Hz sine wave. Input amplifier is set for unity gain,[2] inverting. The digital input is a PCM bit stream generated by passing a 0dBm0, 1020Hz sine wave through an ideal encoder. Receive output is measured single ended. All output levels are (sin x)/x corrected.

GAIN AND DYNAMIC RANGE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
EmW	Encoder Milliwatt Response (transmit gain tolerance)	Signal Input of 1.068Vrms T_A = 25°C, V_{BB} = – 5V, V_{CC} = + 5V	– 0.15	± 0.04	+ 0.15	dBm0
EmW_{TS}	EmW Variation with Temperature and Supplies	± 5% Supplies, 0 to 70°C Relative to Nominal Conditions	– 0.1		+ 0.1	dB
DmW	Digital Milliwatt Response (receive gain tolerance)	Measure Relative to $0TLP_R$. Signal Input per CCITT Recommendation G.711. Output Signal of 1000Hz. T_A = 25°C ; V_{BB} = – 5V ; V_{CC} = + 5V	– 0.15	± 0.04	+ 0.15	dBm0
DmW_{TS}	DmW Variation with Temperature and Supplies	± 5% Supplies, 0 to 70°C	– 0.1		+ 0.1	dB
$0TLP2_X$	Zero Transmission Level Point Transmit Channel (0dBm0)	Referenced to 600Ω Referenced to 900Ω		+ 2.79 + 1.03		dBm dBm
$0TLP2_R$	Zero Receive Level Point Receive Channel (0dBm0)	Referenced to 600Ω Referenced to 900Ω		+ 5.79 + 4.03		dBm dBm

Notes : 1. 0dBm0 is defined as the zero reference point of the channel under test (0TLP) This corresponds to an analog signal input of 1.068 volts rms or an output of 1.516 volts rms.
2 Unity gain input amplifier, signal input VF_{XI} –.

GAIN TRACKING Reference Level = – 10dBm0

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$GT2_X$	Transmit Gain Tracking Error Sinusoidal Input.	+ 3 to – 40dBm0 – 40 to – 50dBm0 – 50 to – 55dBm0			± 0.2 ± 0.4 ± 1.0	dB dB dB
$GT2_R$	Receive Gain Tracking Error Sinusoidal Input.	+ 3 to – 40dBm0 – 40 to – 50dBm0 – 50 to – 55dBm0			± 0.2 ± 0.4 ± 1.0	dB dB dB

NOISE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
N_{XP}	Transmit Noise, Psophometrically Weighted	VF_XI+ = GRDA, VF_XI- = GS_X		(1)*	– 80	dBm0p
N_{RP}	Receive Noise, Psophometrically Weighted	D_R = Lowest Positive Decode Level		+ 9	– 81	dBm0p
N_{SF}	Single Frequency NOISE End to End Measurement	CCITT G.712.4.2			– 50	dBm0
$PSRR_1$	V_{CC} Power Supply Rejection, Transmit Channel	Idle Channel ; 200mV P-P Signal on Supply ; 0 to 50kHz, Measure at D_X		– 40		dB
$PSRR_2$	V_{BB} Power Supply Rejection, Transmit Channel	Idle Channel ; 200mV P-P Signal on Supply ; 0 to 50kHz, Measure at D_X		– 40		dB
$PSRR_3$	V_{CC} Power Supply Rejection, Receive Channel	Idle Channel ; 200mV P-P Signal on Supply ; Measure Narrow Band at PWRO+ Single Ended, 0 to 50kHz		– 40		dB
$PSRR_4$	V_{BB} Power Supply Rejection, Receive Channel	Idle Channel ; 200mV P-P Signal on Supply ; Measure Narrow Band at PWRO+ Single Ended, 0 to 50kHz		– 40		dB
CT_{TR}	Crosstalk, Transmit to Receive, Single Ended Outputs	VF_XI+ = 0dBm0, 1.02kHz, D_R = Lowest Positive Decode Level, Measure at PWRO+			– 80	dB
CT_{RT}	Crosstalk, Receive to Transmit, Single Ended Outputs	D_B = 0dBm0, 1.02kHz, VF_XI+ = GRDA, Measure at D_X			– 80	d

(1) * Noise free : DXPCM Code stable at 01010101.

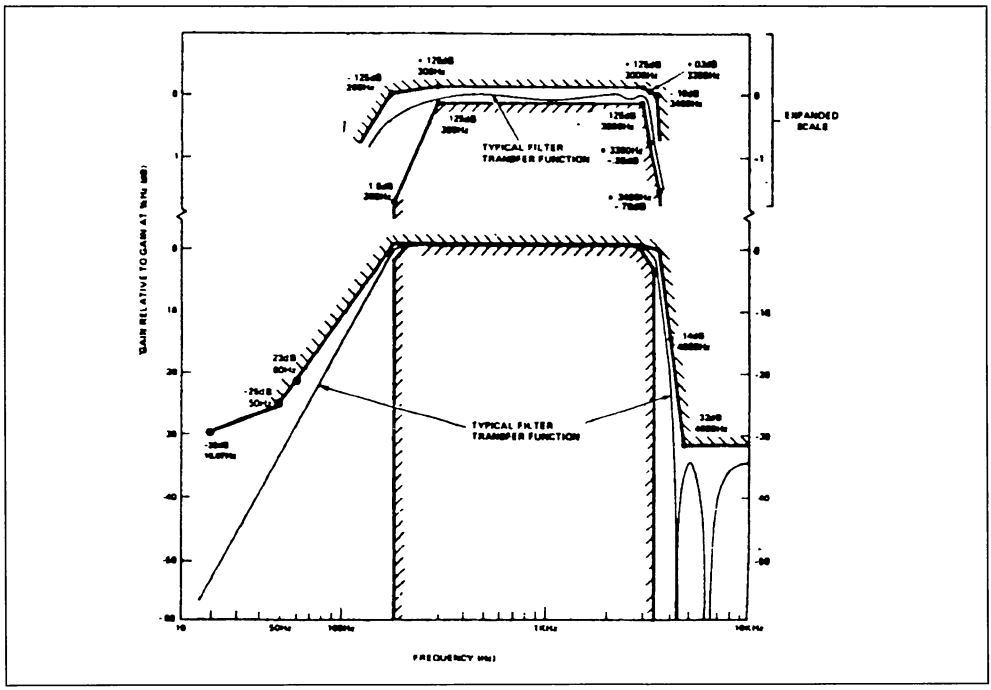
DISTORTION

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$SD2_X$	Transmit Signal to Distortion, Sinusoidal Input CCITT G.712-method 2	$0 \leq VF_XI+ \leq -30dBm0$ $-40dBm0$ $-45dBm0$	36 30 25			dB dB dB
$SD1_R$	Transmit Signal to Distortion, μ-law Sinusoidal Input ; CCITT G.712-method 2	$0 \leq VF_XI+ \leq -30dBm0$ $-40dBm0$ $-45dBm0$	36 30 25			dB dB dB
$SD2_R$	Receive Signal to Distortion, Sinusoidal Input ; CCITT G.712-method 2	$0 \leq VF_XI+ \leq -30dBm0$ $-40dBm0$ $-45dBm0$	36 30 25			dB dB dB
DP_{X1}	Transmit Single Frequency Distortion Products	AT & T Adivisory = 64 (3.8) 0dBm0 Input Signal			– 46	dB
DP_{R1}	Receive Single Frequency Distortion Products	AT & T Adivisory = 64 (3.8) 0dBm0 Input Signal			– 46	dB
IMD_1	Intermodulation Distortion, End to End Measurement	CCITT G.712 (7.1)			– 35	dB
IMD_2	Intermodulation Distortion, End to End Measurement	CCITT G.712 (7.2)			– 49	dB
SOS	Spurious Out of Band Signals, End to End Measurement	CCITT G.712 (6.1)			– 30	dBm0
SIS	Spurious in Band Signals, End to End Measurement	CCITT G.712 (9)			– 40	dBm0
D_{AX}	Transmit Absolute Delay	Fixed Data Rate CLK_X = 2.048MHz ; 0dBm0, 1.02kHz Signal at VF_XI+ Measure at D_X		300		μs
D_{DX}	Transmit Differential Envelope Delay Relative to D_{AX}	f = 500 – 600Hz f = 600 – 1000Hz f = 1000 – 2600Hz f = 2600 – 2800Hz		170 95 45 80		μs μs μs μs
D_{AR}	Receive Absolute Delay	Fixed data rate, CLK_R = 2.048MHz ; digital input is DMW codes. Measure at PWRO+		190		μs
D_{DR}	Receive Differential Envelope Delay Relative to D_{AR}	f = 500 – 600Hz f = 600 – 1000Hz f = 1000 – 2600Hz f = 2600 – 2800Hz		10 10 85 110		μs μs μs μs

TRANSMIT CHANNEL TRANSFER CHARACTERISTICS Input amplifier is set for unity gain, inverting.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
G_{RX}	Gain Relative to Gain at 1.02 kHz	0 dBm0 Signal Input at VF_XI-				
	16.67Hz				– 30	dB
	50Hz				– 25	dB
	60Hz				– 23	dB
	200Hz		– 1.8		– 0.125	dB
	300 to 3000Hz		– 0.125		+ 0.125	dB
	3300Hz		– 0.35		+ 0.03	dB
	3400Hz		– 0.7		– 0.10	dB
	4000Hz				– 14	dB
	4600Hz and Above				– 32	dB

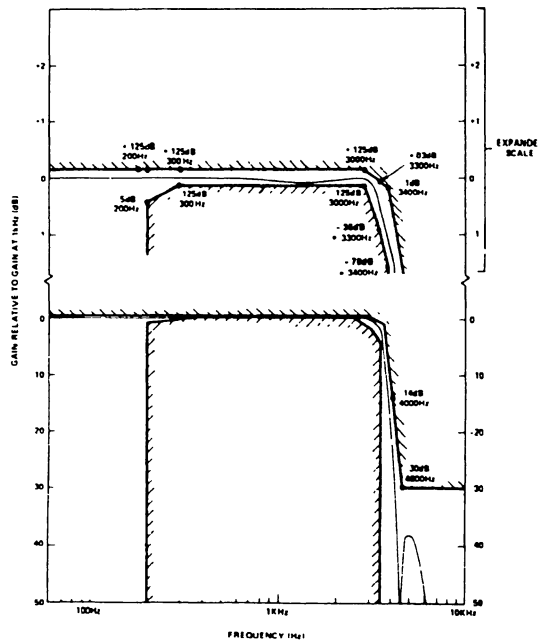
Figure 4 : Transmit Channel.



RECEIVE CHANNEL TRANSFER CHARACTERISTICS

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
G_{RR}	Gain Relative to Gain at 1.02kHz	0dBm0 Signal Input at D_R				
	below 200Hz				+ 0.125	dB
	200Hz		– 0.5		+ 0.125	dB
	300 to 3000Hz		– 0.125		+ 0.125	dB
	3300Hz		– 0.35		+ 0.03	dB
	3400Hz		– 0.7		– 0.1	dB
	4000Hz				– 14	dB
	4600Hz and Above				– 30	dB

Figure 5 : Receive Channel.



AC CHARACTERISTICS - TIMING PARAMETERS

CLOCK SECTION

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
t_{CY}	Clock Period, CLK	f_{CLK} = 2.048MHz	488			ns
t_{CLK}	Clock Pulse Width	CLK	195			ns
t_{DCLK}	Data Clock Pulse Width[1]	64kHz ≤ f_{DCLK} ≤ 2.048MHz	195			ns
t_{CDC}	Clock Duty Cycle	CLK	40	50	60	%
t_r, t_f	Clock Rise and Fall Time		5		30	ns

AC CHARACTERISTICS - TIMING PARAMETERS (continued)

TRANSMIT SECTION, FIXED DATA RATE MODE[2]

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
t_{DZX}	Data Enabled on TS Entry	$0 < C_{LOAD} < 100pF$	0		145	ns
t_{DDX}	Data Delay from CLK	$0 < C_{LOAD} < 100pF$	0		145	ns
t_{HZX}	Data Float on TS Exit	$C_{LOAD} = 0$	60		190	ns
t_{SON}	Timeslot X to Enable	$0 < C_{LOAD} < 100pF$	0		145	ns
t_{SOFF}	Timeslot X to Disable	$C_{LOAD} = 0$	50		190	ns
t_{FSD}	Frame Sync Delay		0		120	ns

RECEIVE SECTION, FIXED DATA RATE MODE

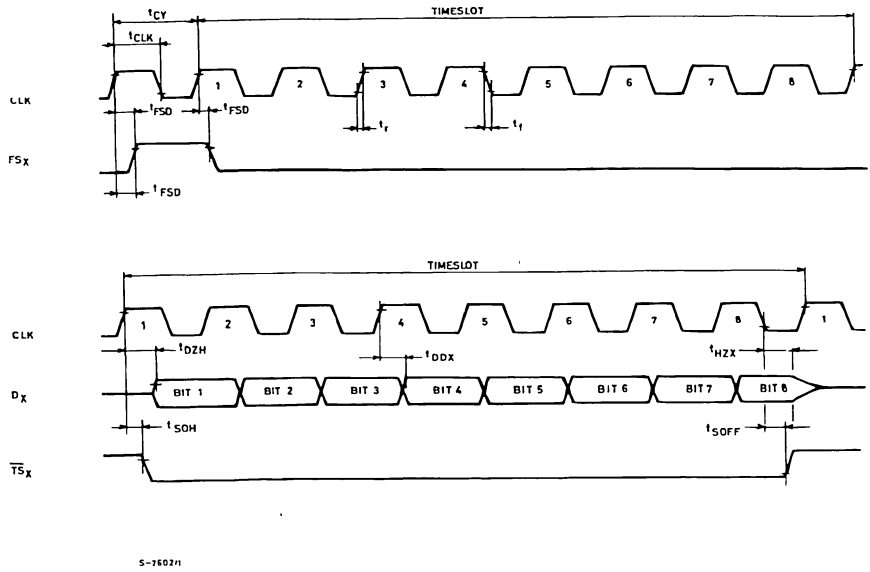
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
t_{DSR}	Receive Data Setup		10			ns
t_{DHR}	Receive Data Hold		60			ns
t_{FSD}	Frame Sync Delay		0		120	ns

Notes : 1. Devices are available which operate at data rates up to 4.096MHz ; the minimum data clock pulse width for these devices is 110ns.
2. Timing parameters t_{DZX}, t_{HZX}, and t_{SOFF} are referenced to a high impedance state.

WAVEFORMS

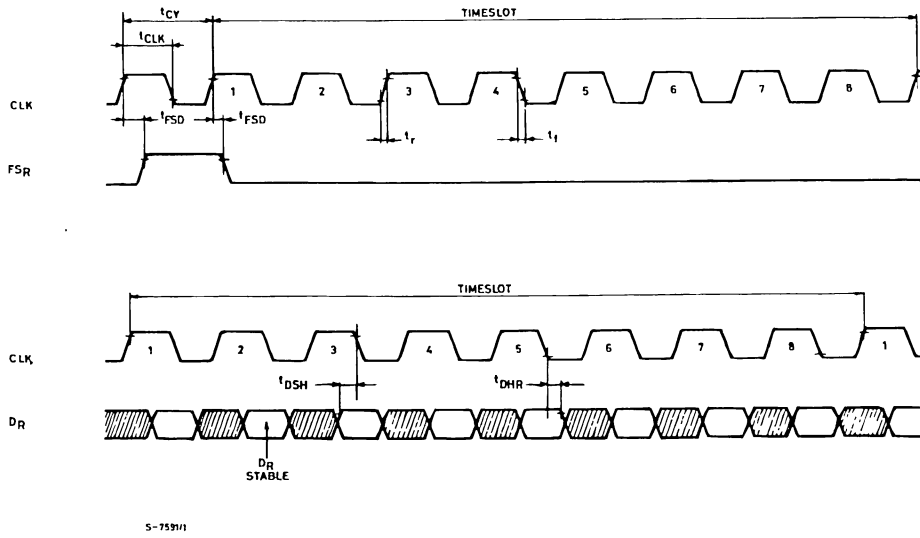
FIXED DATA RATE TIMING.

TRANSMIT TIMING



Note : All timing parameters referenced to V_{IH} and V_{IL} except t_{DZX}, t_{SOFF} and t_{HZX} which reference a high impedance state.

RECEIVE TIMING



Note : All timing parameters referenced to V_{IH} and V_{IL}

AC CHARACTERISITCS - TIMING PARAMETERS (continued)

TRANSMIT SECTION, VARIABLE DATA RATE MODE[1]

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
t_{TSDX}	Timeslot Delay from $DCLK_X$		– 80		80	ns
t_{FSD}	Frame Sync Delay		0		120	ns
t_{DDX}	Data Delay from $DCLK_X$	$0 < C_{LOAD} < 100pF$	0		100	ns
t_{DON}	Timeslot to D_X Active	$0 < C_{LOAD} < 100pF$	0		50	ns
t_{DOFF}	Timeslot to D_X Inactive	$0 < C_{LOAD} < 100pF$	0		80	ns
f_{DX}	Data Clock Frequency		64		2048[2]	kHz
t_{DFSX}	Data Delay from FS_X	t_{TSDX} = 80ns	0		140	ns

RECEIVE SECTION, VARIABLE DATA RATE MODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
t_{TSDR}	Timeslot Delay from $DCLK_R$		– 80		80	ns
t_{FSD}	Frame Sync Delay		0		120	ns
t_{DSR}	Data Setup Time		10			ns
t_{DHR}	Data Hold Time		60			ns
f_{DR}	Data Clock Frequency		64		2048[2]	kHz
t_{SER}	Timeslot End Receive Time		0			ns

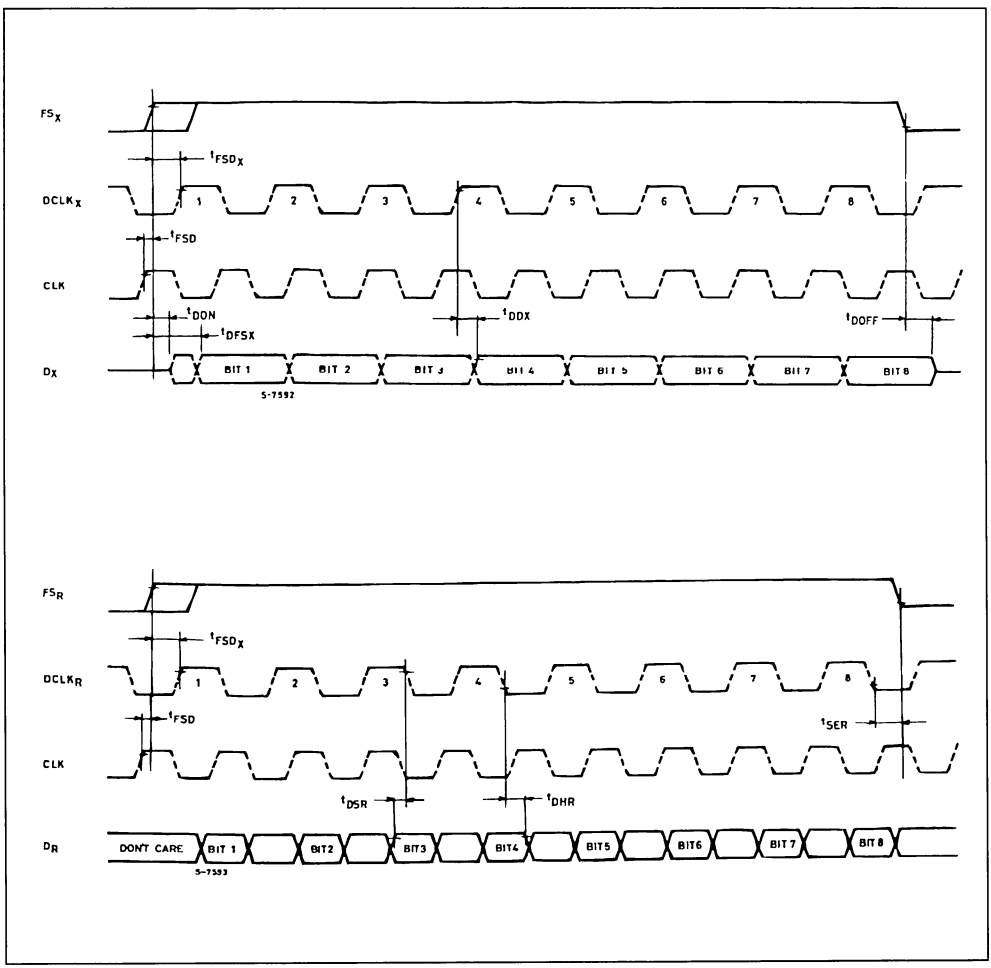
AC CHARACTERISTICS - TIMING PARAMETERS (continued)

64KB OPERATION, VARIABLE DATA RATE MODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
t_{FSLX}	Transmit Frame Sync Minimum Downtime	FS_X is TTL high for remainder of frame	488			ns
t_{FSLR}	Receive Frame Sync Minimum Downtime	FS_R is TTL high for remainder of frame	1952			ns
t_{DCLK}	Data Clock Pulse Width				10	µs

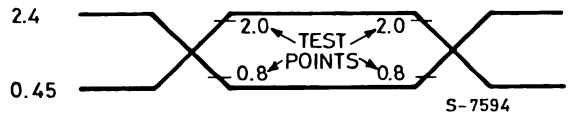
Notes : 1. Timing parameters t_{DON} and t_{DOFF} are referenced to a high impedance state.
2. Device are available which operate at data rates up to 4.096MHz.

VARIABLE DATA RATE TIMING



Note : All timing parameters referenced to V_{IH} and V_{IL} except t_{DON} and t_{OFF} which reference a high impedance state.

A.C. TESTING INPUT, OUTPUT WAVEFORM



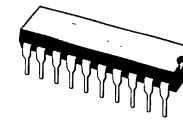
A.C. testing inputs are driven at 2.4V for a logic "1" and 0.45V for a logic "0" timing measurements are made at 2.0V for a logic "1" and 0.8V for a logic "0".

SGS-THOMSON MICROELECTRONICS

TS5070
TS5071

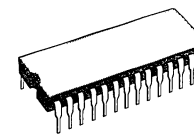
PROGRAMMABLE CODEC/FILTER COMBO 2ND GENERATION

- COMPLETE CODEC AND FILTER SYSTEM INCLUDING :
  - TRANSMIT AND RECEIVE PCM CHANNEL FILTERS
  - μ-LAW OR A-LAW COMPANDING CODER AND DECODER
  - RECEIVE POWER AMPLIFIER DRIVES 300 Ω
  - 4.096 MHz SERIAL PCM DATA (max)
- PROGRAMMABLE FUNCTIONS :
  - TRANSMIT GAIN : 25.4 dB RANGE, 0.1 dB STEPS
  - RECEIVE GAIN : 25.4 dB RANGE, 0.1 dB STEPS
  - HYBRID BALANCE CANCELLATION FILTER
  - TIME-SLOT ASSIGNMENT : UP to 64 SLOTS/FRAME
  - 2 PORT ASSIGNMENT (TS5070)
  - 6 INTERFACE LATCHES (TS5070)
  - A or μ-LAW
  - ANALOG LOOPBACK
  - DIGITAL LOOPBACK
- DIRECT INTERFACE TO SOLID-STATE SLICs
- SIMPLIFIES TRANSFORMER SLIC, SINGLE WINDING SECONDARY
- STANDARD SERIAL CONTROL INTERFACE
- 70 mW OPERATING POWER (typ)
- 2 mW STANDBY POWER (typ)
- MEETS OR EXCEEDS ALL CCITT AND LSSGR SPECIFICATIONS
- TTL AND CMOS COMPATIBLE DIGITAL INTERFACES
- SECOND SOURCE OF TP3070, TP3071/COMBO II ®



DIP20
(Plastic and Ceramic)

ORDER CODE : TS5071N
TS5071J



DIP28L
(Ceramic)

ORDER CODE : TS5070J

PLCC28

ORDER CODE : TS5070FN

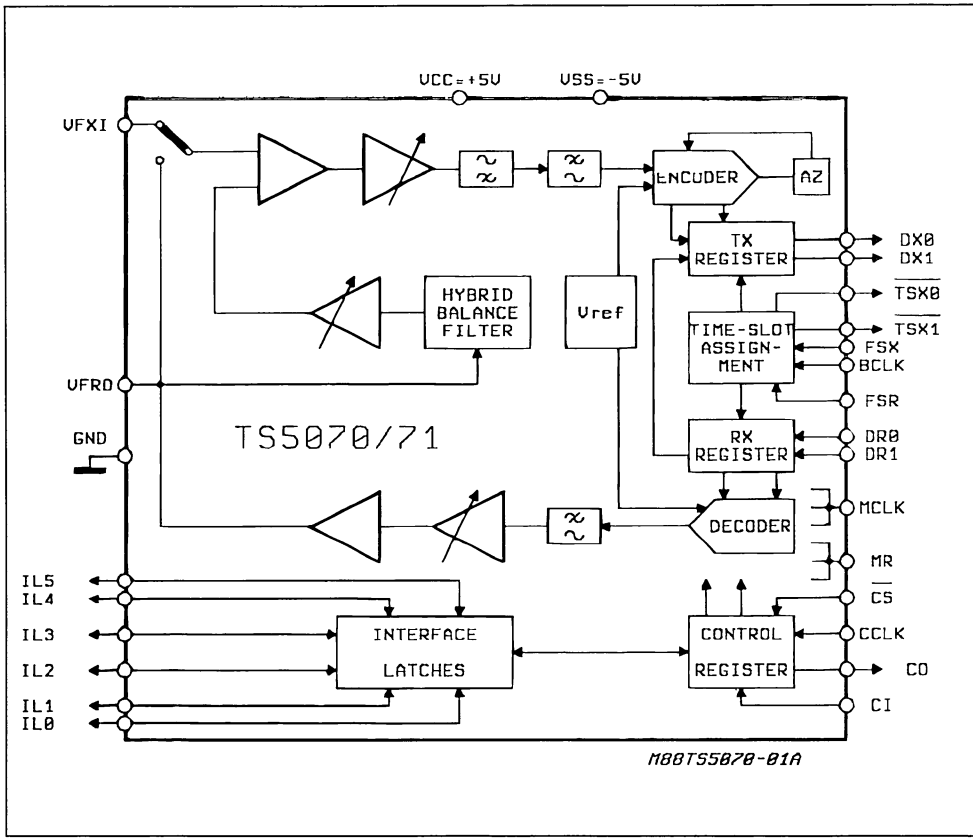
DESCRIPTION

The TS5070 series are second generation combined PCM CODEC and Filter devices optimized for digital switching applications on subscriber and trunk line cards. Using advanced switched capacitor techniques the TS5070 and TS5071 combine transmit bandpass and receive lowpass channel filters with a companding PCM encoder and decoder. The devices are A-law and μ-law selectable and employ a conventional serial PCM interface capable of being clocked up to 4.096 MHz. A number of programmable functions may be controlled via a serial control port.

Channel gains are programmable over a 25.4 dB range in each direction, and a programmable filter is included to enable Hybrid Balancing to be adjusted to suit a wide range of loop impedance conditions. Both transformer and active SLIC interface circuits with real or complex termination impedances can be balanced by this filter, with cancellation in excess of 30 dB being readily achievable when measured across the passband against standard test termination networks.

To enable COMBO IIG to interface to the SLIC control leads, a number of programmable latches are included ; each may be configured as either an input or an output. The TS5070 provides 6 latches and the TS5071 5 latches.

BLOCK DIAGRAM

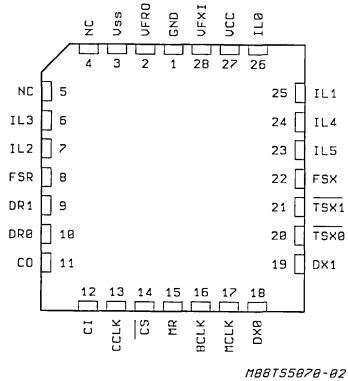


ABSOLUTE MAXIMUM RATINGS

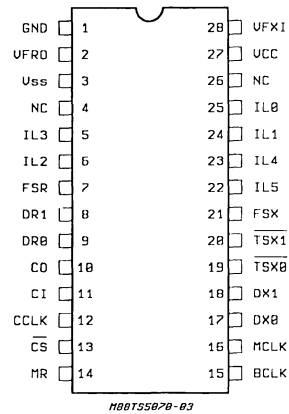
Symbol	Parameter	Value	Unit
V_{CC}	V_{CC} to GND	7	V
V_{SS}	V_{SS} to GND	– 7	V
	Voltage at VFXI	V_{CC} + 0.5 to V_{SS} – 0.5	V
V_{IN}	Voltage at Any Digital Input	V_{CC} + 0.5 to GND – 0.5	V
	Current at VFRO	± 100	mA
I_O	Current at Any Digital Output	± 50	mA
T_{stg}	Storage Temperature Range	– 65, + 150	°C
T_{lead}	Lead Temperature Range (soldering, 10 seconds)	300	°C

PIN CONNECTIONS

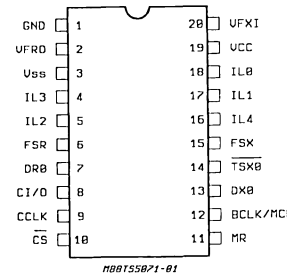
PLCC28
TS5070FN



DIP28
TS5070J



DIP20
TS5071J/N



PIN DESCRIPTION

POWER SUPPLY, CLOCK

Name	Pin Type	TS5070 J	TS5070 FN	TS5071	Function	Description
V_{CC}	S	27	27	19	Positive Power Supply	+ 5 V ± 5 %
V_{SS}	S	3	3	3	Negative Power Supply	– 5 V ± 5 %
GND	S	1	1	1	Ground	All analog and digital signals are referenced to this pin.
BCLK	I	15	16	12	Bit Clock	Bit clock input used to shift PCM data into and out of the D_R and D_X pins. BCLK may vary from 64 kHz to 4.096 MHz in 8 kHz increments, and must be synchronous with MCLK.
MCLK	I	16	17	12	Master Clock	Master clock input used by the switched capacitor filters and the encoder and decoder sequencing logic. Must be 512 kHz, 1. 536/1. 544 MHz, 2.048 MHz or 4.096 MHz and synchronous with BCLK. BCLK and MCLK are wired together in the TS5071.

PIN DESCRIPTION (continued)

TRANSMIT SECTION

Name	Pin Type	TS5070 J	TS5070 FN	TS5071	Function	Description
FS_X	I	21	22	15	Transmit Frame Sync.	Normally a pulse or squarewave waveform with an 8 kHz repetition rate is applied to this input to define the start of the transmit time-slot assigned to this device (non–delayed data mode) or the start of the transmit frame (delayed data mode using the internal time–slot assigment counter).
VF_XI	I	28	28	20	Transmit Analog	This is a high–impedance input. Voice frequency signals present on this input are encoded as an A–law or μ–law PCM bit stream and shifted out on the selected D_X pin.
D_X0 D_X1	0 0	17 18	18 19	13 –	Transmit Data	D_X1 is available on the TS5070 only, D_X0 is available on all devices. These transmit data TRI–STATE® outputs remain in the high impedance state except during the assigned transmit time–slot on the assigned port, during wich the transmit PCM data byte is shifted out on the rising edges of BCLK.
$\overline{TS_X0}$ $\overline{TS_X1}$	0 0	19 20	20 21	14 –	Transmit Time–slot	$\overline{TS_X1}$ is available on the TS5070 only. $\overline{TS_X0}$ is available on all devices. Normally these opendrain outputs are floating in a high impedance state except when a time–slot is active on one of the D_X outputs, when the apppropriate $\overline{TS_X}$ output pulls low to enable a backplane line–driver. Should be strapped to ground (GND) when not used.

RECEIVE SECTION

Name	Pin Type	TS5070 J	TS5070 FN	TS5071	Function	Description
FS_R	I	7	8	6	Receive Frame Sync.	Normally a pulse or squrewave waveform with an 8 kHz repetition rate is applied to this input to define the start of the receive time–slot assigned to this device (non-delayed frame mode) or the start of the receive frame (delayed frame mode using the internal time–slot assignment counter).
VF_R0	0	2	2	2	Receive Analog	The receive analog power amplifier output, capable of driving load impedances as low as 300 Ω (depending on the peak overload level required). PCM data received on the assigned D_R pin is decoded and appears at this output as voice frequency signals.
D_R0 D_R1	I I	9 8	10 9	7 –	Receive Data	D_R1 is available on the TS5070 only, D_R0 is available on all devices. These receive data input(s) are inactive except during the assigned receive time–slot of the assigned port when the receive PCM data is shifted in on the falling edges of BCLK.

PIN DESCRIPTION (continued)

INTERFACE, CONTROL, RESET

Name	Pin Type	TS5070 J	TS5070 FN	TS5071	Function	Description
IL5 IL4 IL3 IL2 IL1 IL0	I/O I/O I/O I/O I/O I/O	22 23 5 6 24 25	23 24 6 7 25 26	– 16 4 5 17 18	Interface Latches	IL5 through IL0 are available on the TS5070, IL4 through IL0 are available on the TS5071. Each interface Latch I/O pin may be individually programmed as an input or an output determined by the state of the corresponding bit in the Latch Direction Register (LDR) . For pins configured as inputs, the logic state sensed on each input is latched into the interface Latch Register (ILR) whenever control data is written to COMBO IIG, while $\overline{CS}$ is low, and the information is shifted out on the CO (or CI/O) pin. When configured as outputs, control data written into the ILR appears at the corresponding IL pins.
CCLK	I	12	13	9	Control Clock	This clock shifts serial control information into or out of CI or CO (or CI/O) when the $\overline{CS}$ input is low depending on the current instruction. CCLK may be asynchronous with the other system clocks.
CI/O	I/O	–	–	8	Control Data Input/output	This is Control Data I/O pin wich is provided on the TS5071. Serial control information is shifted into or out of COMBO IIG on this pin when $\overline{CS}$ is low. The direction of the data is determined by the current instruction as defined in Table 1.
CI CO	I O	11 10	12 11	– –	Control Data Input Control Data Output	These are separate controls, availables only on the TS5070. They can be wired together if required.
$\overline{CS}$	I	13	14	10	Chip Select	When this pins is low, control information can be written into or out of COMBO IIG via the CI and CO pins (or CI/O).
MR	I	14	15	11	Master Reset	This logic input must be pulled low for normal operation of COMBO IIG. When pulled momentarily high, all programmable registers in the device are reset to the states specified under "Power–on Initialization".

FUNCTIONAL DESCRIPTION

POWER-ON INITIALIZATION

When power is first applied, power-on reset circuitry initializes COMBO IIG and puts it into the power-down state. The gain control registers for the transmit and receive gain sections are programmed for no output, the hybrid balance circuit is turned off, the power amp is disabled and the device is in the non-delayed timing mode. The Latch Direction Register (LDR) is pre-set with all IL pins programmed as inputs, placing the SLIC interface pins in a high impedance state. The CI/O pin is set as an input ready for the first control byte of the initialization sequence.

A reset to these same initial conditions may also be forced by driving the MR pin momentarily high. This may be done either when powered-up or down. For normal operation this pin must be pulled low.

The desired modes for all programmable functions may be initialized via the control port prior to a Power-up command.

POWER-DOWN STATE

Following a period of activity in the powered-up state the power-down state may be re-entered by writing a Power-Down instruction into the serial control port as indicated in table 1. The power down instruction may be included within any other instruction code. It is recommended that the chip be powered down before executing any instructions. In the power-down state, all non-essential circuitry is de-activated and the D_X0 and D_X1 outputs are in the high impedance TRI-STATE condition.

The coefficients stored in the Hybrid Balance circuit and the Gain Control registers, the data in the LDR and ILR, and all control bits remain unchanged in the power-down state unless changed by writing new data via the serial control port, which remains operational. The outputs of the Interface Latches also remain active, maintaining the ability to monitor and control a SLIC.

TRANSMIT FILTER AND ENCODER

The Transmit section input, VF_XI, is a high impedance summing input which is used as the differencing point for the internal hybrid balance cancellation signal. No external components are needed to set the gain. Following this circuit is a programmable gain/attenuation amplifier which is controlled by the contents of the Transmit Gain Register (see Programmable Functions section). An active prefilter then precedes the 3rd order high-pass and 5th order low-pass switched capacitor filters. The A/D converter has a compressing characteristic according to the standard CCITT A or μ255 coding laws, which must be selected by a control instruction during initialization (see table 1 and 2). A precision on-chip voltage reference ensures accurate and highly stable transmission levels. Any offset voltage arising in the gain-set amplifier, the filters or the comparator is cancelled by an internal auto-zero circuit.

Each encode cycle begins immediately following the assigned Transmit time-slot. The total signal delay referenced to the start of the time-slot is approximately 165 μs (due to the Transmit Filter) plus 125 μs (due to encoding delay), which totals 290 μs. Data is shifted out on D_X0 or D_X1 during the selected time slot on eight rising edges of BCLK.

DECODER AND RECEIVE FILTER

PCM data is shifted into the Decoder's Receive PCM Register via the D_R0 or D_R1 pin during the selected time-slot on the 8 falling edges of BCLK. The Decoder consists of an expanding DAC with either A or μ255 law decoding characteristic, which is selected by the same control instruction used to select the Encode law during initialization. Following the Decoder is a 5th order low-pass switched capacitor filter with integral Sin x/x correction for the 8 kHz sample and hold. A programmable gain amplifier, which must be set by writing to the Receive Gain Register, is included, and finally a Post-Filter/Power Amplifier capable of driving a 300 Ω load to ± 3.5 V, a 600 Ω load to ± 3.8 V or 15 kΩ load to ± 4.0 V at peak overload.

A decode cycle begins immediately after each receive time-slot, and 10 μs later the Decoder DAC output is updated. The total signal delay is 10 μs plus 120 μs (filter delay) plus 62.5 μs (1/2 frame) which gives approximately 190 μs.

PCM INTERFACE

The FS_X and FS_R frame sync inputs determine the beginning of the 8-bit transmit and receive time-slots respectively. They may have any duration from a single cycle of BCLK to a square wave. Two different relationships may be established between the frame sync inputs and the actual time-slots on the PCM busses by setting bit 3 in the Control Register (see table 2). Non delayed data mode is similar to long-frame timing on the ETC 5050/60 series of devices : time-slots being nominally coincident with the rising edge of the appropriate FS input. The alternative is to use Delayed Data mode which is similar to short-frame sync timing, in which each FS input must be high at least a half-cycle of BCLK earlier than the time-slot.

The Time-Slot Assignment circuit on the device can only be used with Delayed Data timing. When using Time-Slot Assignment, the beginning of the first time-slot in a frame is identified by the appropriate FS input. The actual transmit and receive time-slots are then determined by the internal Time-Slot Assignment counters. Transmit and Receive frames and time-slots may be skewed from each other by any number of BCLK cycles.

During each assigned transmit time-slot, the selected $D_X0/1$ output shifts data out from the PCM register on the rising edges of BCLK. TS_X0 (or TS_X1 as appropriate) also pulls low for the first 7 1/2 bit times of the time-slot to control the TRI-STATE Enable of a backplane line driver. Serial PCM data is shifted into the selected $D_R0/1$ input during each assigned Receive time slot on the falling edges of BCLK. D_X0 or D_X1 and D_R0 or D_R1 are selectable on the TS5070 only.

SERIAL CONTROL PORT

Control information and data are written into or readback from COMBO IIG via the serial control port consisting of the control clock CCLK ; the serial data input/output CI/O (or separate input CI, and output $\overline{CO}$ on the TS5070 only) ; and the Chip Select input $\overline{CS}$. All control instructions require 2 bytes, as

listed in table 1, with the exception of a single byte power-up/down command. To shift control data into COMBO IIG, CCLK must be pulsed high 8 times while $\overline{CS}$ is low. Data on the CI or CI/O input is shifted into the serial input register on the falling edge of each CCLK pulse. After all data is shifted in, the contents of the input shift register are decoded, and may indicate that a 2nd byte of control data will follow. This second byte may either be defined by a second byte-wide $\overline{CS}$ pulse or may follow the first continuously, i.e. it is not mandatory for $\overline{CS}$ to return high in between the first and second control bytes. On the falling edge of the 8th CCLK clock pulse in the 2nd control byte the data is loaded into the appropriate programmable register. $\overline{CS}$ may remain low continuously when programming successive registers, if desired. However $\overline{CS}$ should be set high when no data transfers are in progress.

To readback interface Latch data or status information from COMBO IIG, the first byte of the appropriate instruction is strobed in during the first $\overline{CS}$ pulse, as defined in table 1. $\overline{CS}$ must then be taken low for a further 8 CCLK cycles, during which the data is shifted onto the CO or CI/O pin on the rising edges of CCLK. When $\overline{CS}$ is high the CO or CI/O pin is in the high-impedance TRI-STATE, enabling the CI/O pins of many devices to be multiplexed together. Thus, to summarize, 2-byte READ and WRITE instructions may use either two 8-bit wide $\overline{CS}$ pulses or a single 16-bit wide $\overline{CS}$ pulse.

Table 1 : Programmable Register Instructions.

Function	Byte 1								Byte 2
	7	6	5	4	3	2	1	0	
Single Byte Power–up/down	P	X	X	X	X	X	0	X	None
Write Control Register	P	0	0	0	0	0	1	X	See Table 2
Read–back Control Register	P	0	0	0	0	1	1	X	See Table 2
Write Latch Direction Register	P	0	0	1	0	0	1	X	See Table 4
(LDR)	P	0	0	1	0	1	1	X	See Table 4
Read Latch Direction Register									
Write Latch Content Register (ILR)	P	0	0	0	1	0	1	X	See Table 5
Read Latch Content Register	P	0	0	0	1	1	1	X	See Table 5
Write Transmit Time–slot/port	P	1	0	1	0	0	1	X	See Table 6
Read–back Transmit Time–slot/port	P	1	0	1	0	1	1	X	See Table 6
Write Receive Time–slot/port	P	1	0	0	1	0	1	X	See Table 6
Read–back Receive Time–slot/port	P	1	0	0	1	1	1	X	See Table 6
Write Transmit Gain Register	P	0	1	0	1	0	1	X	See Table 7
Read Transmit Gain Register	P	0	1	0	1	1	1	X	See Table 7
Write Receive Gain Register	P	0	1	0	0	0	1	X	See Table 8
Read Receive Gain Register	P	0	1	0	0	1	1	X	See Table 8
Write Hybrid Balance Register ≠ 1	P	0	1	1	0	0	1	X	See Table 9
Read Hybrid Balance Register ≠ 1	P	0	1	1	0	1	1	X	See Table 9
Write Hybrid Balance Register ≠ 2	P	0	1	1	1	0	1	X	See Table 10
Read Hybrid Balance Register ≠ 2	P	0	1	1	1	1	1	X	See Table 10
Write Hybrid Balance Register ≠ 3	P	1	0	0	0	0	1	X	
Read Hybrid Balance Register ≠ 3	P	1	0	0	0	1	1	X	

Notes : 1. Bit 7 of bytes 1 and 2 is always the first bit clocked into or out of the CI, CO or CI/CO pin.
2. "P" is the power-up/down control bit, see "Power-up" section ("0" = Power Up "1" = Power Down).
X = Don't Care.

PROGRAMMABLE FUNCTIONS

POWER-UP/DOWN CONTROL

Following power-on initialization, power-up and power-down control may be accomplished by writing any of the control instructions listed in table 1 into COMBO IIG with the "P" bit set to "0" for power-up or "1" for power-down. Normally it is recommended that all programmable functions be initially programmed while the device is powered down. Power state control can then be included with the last programming instruction or the separate single-byte instruction. Any of the programmable registers may also be modified while the device is powered-up or down be setting the "P" bit as indicated. When the power up or down control is ente-

red as a single byte instruction, bit one (1) must be set to a 0.

When a power-up command is given, all de-activated circuits are activated, but the TRI-STATE PCM output(s), D_X0 (and D_X1), will remain in the high impedance state until the second FS_X pulse after power-up.

CONTROL REGISTER INSTRUCTION

The first byte of a READ or WRITE instruction to the Control Register is as shown in table 1. The second byte functions are detailed in table 2.

MASTER CLOCK FREQUENCY SELECTION

A Master clock must be provided to COMBO IIG for operation of the filter and coding/decoding functions. The MCLK frequency must be either 512 kHz, 1.536 MHz, 1.544 MHz, 2.048 MHz, or 4.096 MHz and must be synchronous with BCLK. Bits F_1 and F_0 (see table 2) must be set during initialization to select the correct internal divider.

CODING LAW SELECTION

Bits "MA" and "IA" in table 2 permit the selection of μ255 coding or A-law coding with or without even-bit inversion.

ANALOG LOOPBACK

Analog Loopback mode is entered by setting the "AL" and "DL" bits in the Control Register as shown in table 2. In the analog loopback mode, the Transmit input VF_XI is isolated from the input pin and internally connected to the VF_RO output, forming a loop from the Receive PCM Register back to the Transmit PCM Register. The VF_RO pin remains active, and the programmed settings of the Transmit and Receive gains remain unchanged, thus care must be taken to ensure that overload levels are not exceeded anywhere in the loop.

DIGITAL LOOPBACK

Digital Loopback mode is entered by setting the "DL" bit in the Control Register as shown in table 2. This

Table 2 : Control Register Byte 2 Functions.

Bit Number								Function
7	6	5	4	3	2	1	0	
F1	F0	MA	IA	DN	DL	AL	PP	
0 0 1 1	0 1 0 1							MCLK = 512 kHz MCLK = 1. 536 or 1. 544 MHz MCLK = 2. 048 MHz * MCLK = 4. 096 MHz
		0 1 1	X 0 1					Select μ. 255 Law * A–law, Including Even Bit Inversion A–Law, No Even Bit Inversion
				0 1				Delayed Data Timing Non–delayed Data Timing *
					0 1 0	0 X 0		Normal Operation * Digital Loopback Analog Loopback
							0 1	Power Amp Enabled in PDN Power Amp Disabled in PDN *

* = State at power-on initialization (bit 4 = 0).

Table 3 : Coding Law Conventions.

	μ255 Law								True A–law Including Even Bit Inversion								A–law Without Even Bit Inversion							
	MSB							LSB	MSB							LSB	MSB							LSB
V_{IN} = + Full Scale	1	0	0	0	0	0	0	0	0	1	0	1	0	1	0	1	0	1	1	1	1	1	1	1
V_{IN} = 0 V	1	1	1	1	1	1	1	1	1	1	0	1	0	1	0	1	1	0	0	0	0	0	0	0
	0	1	1	1	1	1	1	1	1	0	1	0	1	0	1	0	1	0	0	0	0	0	0	0
V_{IN} = – Full Scale	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0	0	1	1	1	1	1	1	1

Note : The MSB is always the first PCM bit shifted in or out of COMBO IIG.

mode provides another stage of path verification by enabling data written into the Receive PCM Register to be read back from that register in any Transmit time-slot at D_X0 or D_X1.

For Analog Loopback as well as for Digital Loopback PCM decoding continues and analog output appears at VF_RO. The output can be disabled by pro gramming "no output" in the Receive Gain Register (see table 8).

INTERFACE LATCH DIRECTIONS

Immediately following power-on, all Interface Latches assume they are inputs, and therefore all IL pins are in a high impedance state. Each IL pin may be individually programmed as a logic input or output by writing the appropriate instruction to the LDR, see table 1 and 4. Bits L_5-L_0 must be set by writing the specific instruction to the LDR with the L bits in the second byte set as specified in table 4. Unused interface latches should be programmed as outputs.

Table 4 : Byte 2 Functions of Latch Direction Register.

Bit Number							
7	6	5	4	3	2	1	0
L0	L1	L2	L3	L4	L5	X	X

L_N Bit	IL Direction
0	Input *
1	Output

* = State at power-on initialization.
Note : L5 should be programmed as an output for the TS5071.

INTERFACE LATCH STATES

Interface Latches configured as outputs assume the state determined by the appropriate data bit in the 2-byte instruction written to the Latch Content Register (ILR) as shown in tables 1 and 5. Latches configured as inputs will sense the state applied by an external source, such as the Off-Hook detect output of a SLIC. All bits of the ILR, i.e. sensed inputs and the programmed state of outputs, can be read back in the 2nd byte of a READ from the ILR. It is recommended that, during initialization, the state of IL pins to be configured as outputs should first be programmed, followed immediately by the Latch Direction Register.

Table 5 : Interface Latch Data Bit Order.

Bit Number							
7	6	5	4	3	2	1	0
D0	D1	D2	D3	D4	D5	X	X

TIME-SLOT ASSIGNMENT

COMBO IIG can operate in either fixed time-slot or time-slot assignment mode for selecting the Transmit and Receive PCM time-slots. Following power-on, the device is automatically in Non-Delayed Timing mode, in which the time-slot always begins with the leading (rising) edge of frame sync inputs FS_X and FS_R. Time-Slot Assignment may only be used with Delayed Data timing : see figure 6. FS_X and FS_R may have any phase relationship with each other in BCLK period increments.

Table 6 : Byte 2 of Time-slot and Port Assignment Instructions.

Bit Number								Function
7 EN	6 PS (note 1)	5 T5 (note 2)	4 T4	3 T3	2 T2	1 T1	0 T0	
0	X	X	X	X	X	X	X	Disable D_X Outputs (transmit instruction) * Disable D_R Inputs (receive instruction) *
1	0	Assign One Binary Coded Time–slot from 0–63						Enable D_X0 Output, Disable D_X1 Output (Transmit instruction)
		Assign One Binary Coded Time–slot from 0–63						Enable D_R0 Input, Disable D_R1 Input (receive instruction)
1	1	Assign One Binary Coded Time–slot from 0–63						Enable D_X1 Output, Disable D_X0 Output (Transmit instruction)
		Assign One Binary Coded Time–slot from 0–63						Enable D_R1 Input, Disable D_R0 Input (receive instruction)

Notes : 1. The "PS" bit MUST always be set to 0 for the TS5071.
2. T5 is the MSB of the time-slot assignment.
* = State at power-on initialization.

Alternatively, the internal time-slot assignment counters and comparators can be used to access any time-slot in a frame, using the frame sync inputs as marker pulses for the beginning of transmit and receive time-slot 0. In this mode, a frame may consist of up to 64 time-slots of 8 bits each. A time-slot is assigned by a 2-byte instruction as shown in table 1 and 6. The last 6 bits of the second byte indicate the selected time-slot from 0-63 using straight binary notation. A new assignment becomes active on the second frame following the end of the Chip Select for the second control byte. The "EN" bit allows the PCM inputs $D_R0/1$ or outputs $D_X0/1$ as appropriate, to be enabled or disabled.

Time-Slot Assignment mode requires that the FS_X and FS_R pulses must conform to the delayed timing format shown in figure 6.

PORT SELECTION

On the TS5070 only, an additional capability is available : 2 Transmit serial PCM ports, D_X0 and D_X1 and 2 receive serial PCM ports, D_R0 and D_R1, are provided to enable two-way space switching to be implemented. Port selections for transmit and receive are made within the appropriate time-slot assignment instruction using the "PS" bit in the second byte.

On the TS5071, only ports D_X0 and D_R0 are available, therefore the "PS" bit MUST always be set to 0 for these devices.

Table 6 shows the format for the second byte of both transmit and receive time-slot and port assignment instructions.

TRANSMIT GAIN INSTRUCTION BYTE 2

The transmit gain can be programmed in 0.1 dB steps by writing to the Transmit Gain Register as defined in tables 1 and 7. This corresponds to a range of 0 dBm0 levels at VF_XI between 1.619 Vrms and 0.087 Vrms (equivalent to + 6.4 dBm to – 19.0 dBm in 600 Ω). To calculate the binary code for byte 2 of this instruction for any desired input 0 dBm0 level in Vrms, take the nearest integer to the decimal number given by :

$$200 \times \log_{10} (V/\sqrt{0.6}) + 191$$

and convert to the binary equivalent. Some examples are given in table 7.

Table 7 : Byte 2 of Transmit Gain Instructions.

Bit Number								0dBm0 Test Level at VF_XI	
7	6	5	4	3	2	1	0	In dBm (into 600 Ω)	In Vrms
0	0	0	0	0	0	0	0	No Output *	
0	0	0	0	0	0	0	1	– 19	0. 087
0	0	0	0	0	0	1	0	– 18. 9	0. 088
1	0	1	1	1	1	1	1	0	0. 775
1	1	1	1	1	1	1	0	+ 6.3	1. 60
1	1	1	1	1	1	1	1	+ 6.4	1. 62

* = state at power initialization.

RECEIVE GAIN INSTRUCTION BYTE 2

The receive gain can be programmed in 0.1 dB steps by writing to the Receive Gain Register as defined in table 1 and 8. Note the following restriction on output drive capability :

a) 0 dBm0 levels ≤ 1.97 Vrms at VF_RO may be driven into a load of ≥ 15 kΩ to GND,

b) 0 dBm0 levels ≤ 1.86 Vrms at VF_RO may be driven into a load of ≥ 600 Ω to GND,

c) 0 dBm levels ≤ 1.71 Vrms at VF_RO may be driven into a load of ≥ 300 Ω to GND.

To calculate the binary code for byte 2 of this instruction for any desired output 0 dBm0 level in Vrms, take the nearest integer to the decimal number given by :

$$200 \times \log_{10} (V/\sqrt{0.6}) + 174$$

and convert to the binary equivalent. Some examples are given in table 8.

Table 8 : Byte 2 of Receive Gain Instructions.

Bit Number								0dBm0 Test Level at VF_RO	
7	6	5	4	3	2	1	0	In dBm (into 600 Ω)	In Vrms
0	0	0	0	0	0	0	0	No Output * (low Z to GND)	
0	0	0	0	0	0	0	1	– 17. 3	0. 106
0	0	0	0	0	0	1	0	– 17. 2	0. 107
1	0	1	0	1	1	1	0	0	0. 775
1	1	1	1	0	0	1	1	+ 6. 9 (note 1)	1. 71
1	1	1	1	1	0	1	0	+ 7.6 (note 2)	1. 86
1	1	1	1	1	1	1	1	+ 8.1 (note 3)	1. 97

Notes : 1 Maximum level into 300 Ω
2. Maximum level into 600 Ω.
3. RL ≥ 15 kΩ.
* = State at power on initialization.

HYBRID BALANCE FILTER

The Hybrid Balance Filter on COMBO IIG is a programmable filter consisting of a second-order Bi-Quad section, Hybal1, followed by a first-order section, Hybal2, and a programmable attenuator. Either of the filter sections can be bypassed if only one is required to achieve good cancellation. A selectable 180 degree inverting stage is included to compensate for interface circuits which also invert the transmit input relative to the receive output signal. The Bi-Quad is intended mainly to balance low frequency signals across a transformer SLIC, and the first order section to balance midrange to higher audio frequency signals. The attenuator can be programmed to compensate for VF_RO to VF_XI echos in the range of – 2.5 to – 8.5 dB.

As a Bi-Quad, Hybal1 has a pair of low frequency zeroes and a pair of complex conjugate poles. When configuring the Bi-Quad, matching the phase of the hybrid at low to midband frequencies is most critical. Once the echo path is correctly balanced in phase, the magnitude of the cancellation signal can be corrected by the programmable attenuator.

The Bi-Quad mode of Hybal1 is most suitable for balancing interfaces with transformers having high inductance of 1.5 Henries or more. An alternative configuration for smaller transformers is available by converting Hybal1 to a simple first-order section with a single real low frequency pole and 0 Hz zero. In this mode, the pole frequency may be programmed.

Many line interfaces can be adequately balanced by use of the Hybal1 section only, in which case the Hybal2 filter should be de-selected to bypass it.

Hybal2, the higher frequency first-order section, is provided for balancing an electronic SLIC, and is also helpful with a transformer SLIC in providing additional phase correction for mid and high-band frequencies, typically 1 kHz to 3.4 kHz. Such a correction is particularly useful if the test balance impedance includes a capacitor of 100 nF or less, such as the loaded and non-loaded loop test networks in the United States. Independent placement of the pole and zero location is provided.

Table 9 : Hybrid Balance Register 1 Byte 2 Instruction.

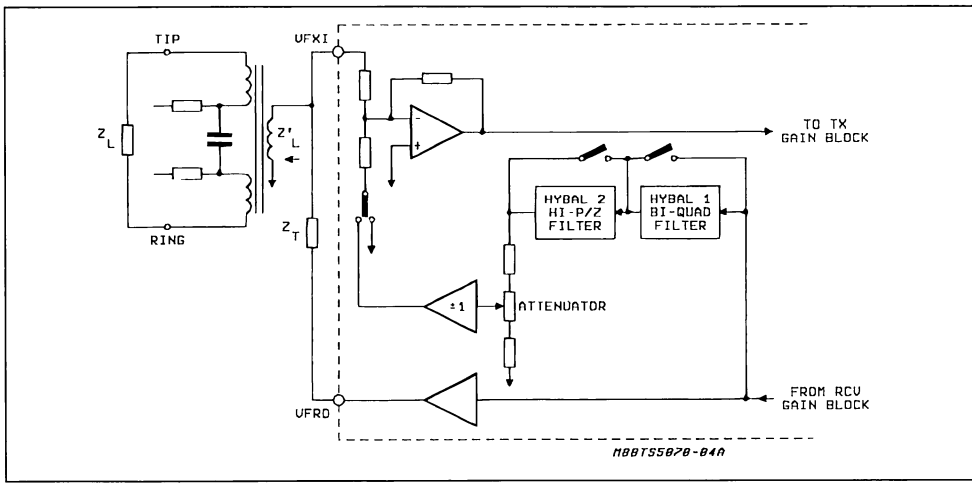
Bit	State	Function
7	0	Disable Hybrid Balance Circuit Completely. No internal cancellation is provided. *
	1	Enable Hybrid Balance Cancellation Path
6	0	Phase of the internal cancellation signal assumes inverted phase of the echo path from VF_RO to VF_XI.
	1	Phase of the internal cancellation signal assumes no phase inversion in the line interface.
5	0	Bypass Hybal 2 Filter Section
	1	Enable Hybal 2 Filter Section
G4–G0		Attenuation Adjustment for the Magnitude of the Cancellation Signal. Range is – 2.5 dB (00000) to – 8.5 dB (11000).

* = State at power on initialization.
Settling = Please refer to software TS5077-2

Figure 1 shows a simplified diagram of the local echo path for a typical application with a transformer interface. The magnitude and phase of the local echo signal, measured at VF_XI are a function of the termination impedance Z_T, the line transformer and the impedance of the 2 W loop, Z_L. If the impedance reflected back into the transformer primary is expressed as Z_L' then the echo path transfer function from VF_RO to VF_XI is :

$$H(W) = Z_L' / (Z_T + Z_L')$$

Figure 1 : Simplified Diagram of Hybrid Balance Circuit.



PROGRAMMING THE FILTER

On initial power-up the Hybrid Balance filter is disabled. Before the hybrid balance filter can be programmed it is necessary to design the transformer and termination impedance in order to meet system 2 W input return loss specifications, which are normally measured against a fixed test impedance (600 or 900 Ω in most countries). Only then can the echo path be modeled and the hybrid balance filter programmed. Hybrid balancing is also measured against a fixed test impedance, specified by each national Telecom administration to provide adequate control of talker and listener echo over the majority of their network connections. This test impedance is Z_L in figure 1. The echo signal and the degree of transhybrid loss obtained by the programmable filter must be measured from the PCM digital input D_R0, to the PCM digital output D_X0, either by digital test signal analysis or by conversion back to analog by a PCM CODEC/Filter.

Three registers must be programmed in COMBO IIG to fully configure the Hybrid Balance Filter as follows :

Register 1 : select/de-select Hybrid Balance Filter
invert/non-invert cancellation signal
select/de-select Hybal2 filter section attenuator setting.

Register 2 : select/de-select Hybal1 filter
set Hybal1 to Bi-Quad or 1st order
program pole and zero frequency.

Table 10 : Hybrid Balance Register 2 Byte 2 Instruction.

Bit Number								Function
7	6	5	4	3	2	1	0	
0	0	0	0	0	0	0	0	By Pass Hybal 1 Filter
X	X	X	X	X	X	X	X	Pole/zero Setting

Register 3 : program pole frequency in Hybal2 filter
program zero frequency in Hybal2 filter
settings = Please refer to software TS5077-2.

Standard filter design techniques may be used to model the echo path and design a matching hybrid balance filter configuration. Alternatively, the frequency response of the echo path can be measured and the hybrid balance filter programmed to replicate it.

An Hybrid Balance filter design guide and software optimization program are available under license from SGS-Thomson Microelectronics (order TS5077-2).

APPLICATION INFORMATION

Figure 2 shows a typical application of the TS5070 together with a transformer SLIC.

The design of the transformer is greatly simplified due to the on-chip hybrid balance cancellation filter. Only one single secondary winding is required (see application note AN.091 - Designing a subscriber line card module using the TS5070/COMBO IIG). Figures 3 and 4 show an arrangement with SGS-Thomson monolithic SLICS.

POWER SUPPLIES

While the pins of the TS5070 and TS5071/COMBO IIG devices are well protected against electrical misuse, it is recommended that the standard CMOS practice of applying GND to the device before any other connections are made should always be followed. In applications where the printed circuit card may be plugged into a hot socket with power and clocks already present, an extra long ground pin on the connector should be used and a Schottky diode connected between V_{SS} and GND. To minimize noise sources all ground connections to each device should meet at a common point as close as possible to the GND pin in order to prevent the interaction of ground return currents flowing through a common bus impedance. Power supply decoupling capacitors of 0.1 µF should be connected from this common device ground point to V_{CC} and V_{SS} as close to the device pins as possible. V_{CC} and V_{SS} should be decoupled with low effective series resistance capacitors of at least 10 µF near the card edge connector.

Figure 2 : Transformer SLIC + COMBO IIG.

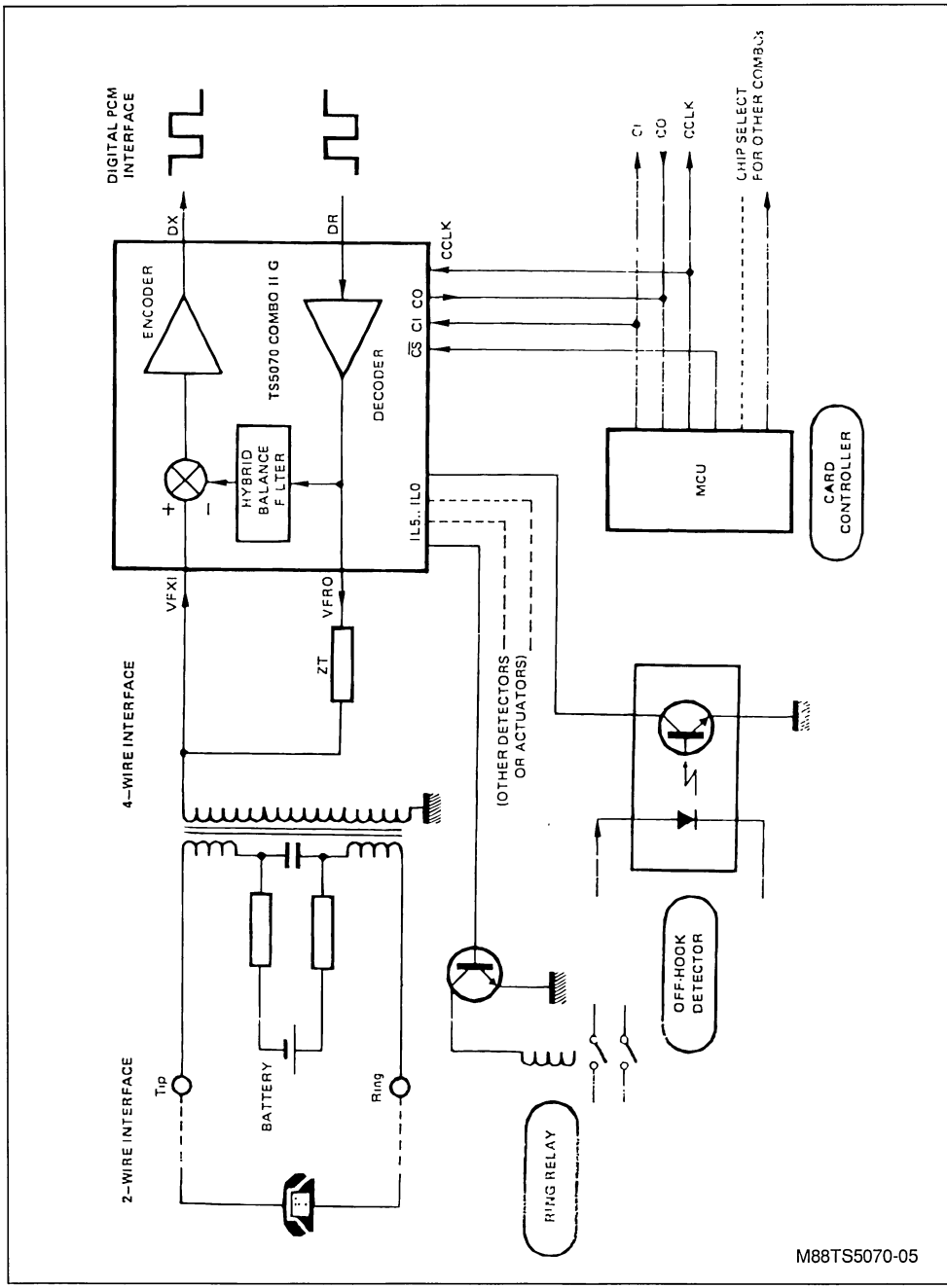


Figure 3 : Interface with TDB 7711 + 7712 or L3010 + L3000 Silicon SLIC.

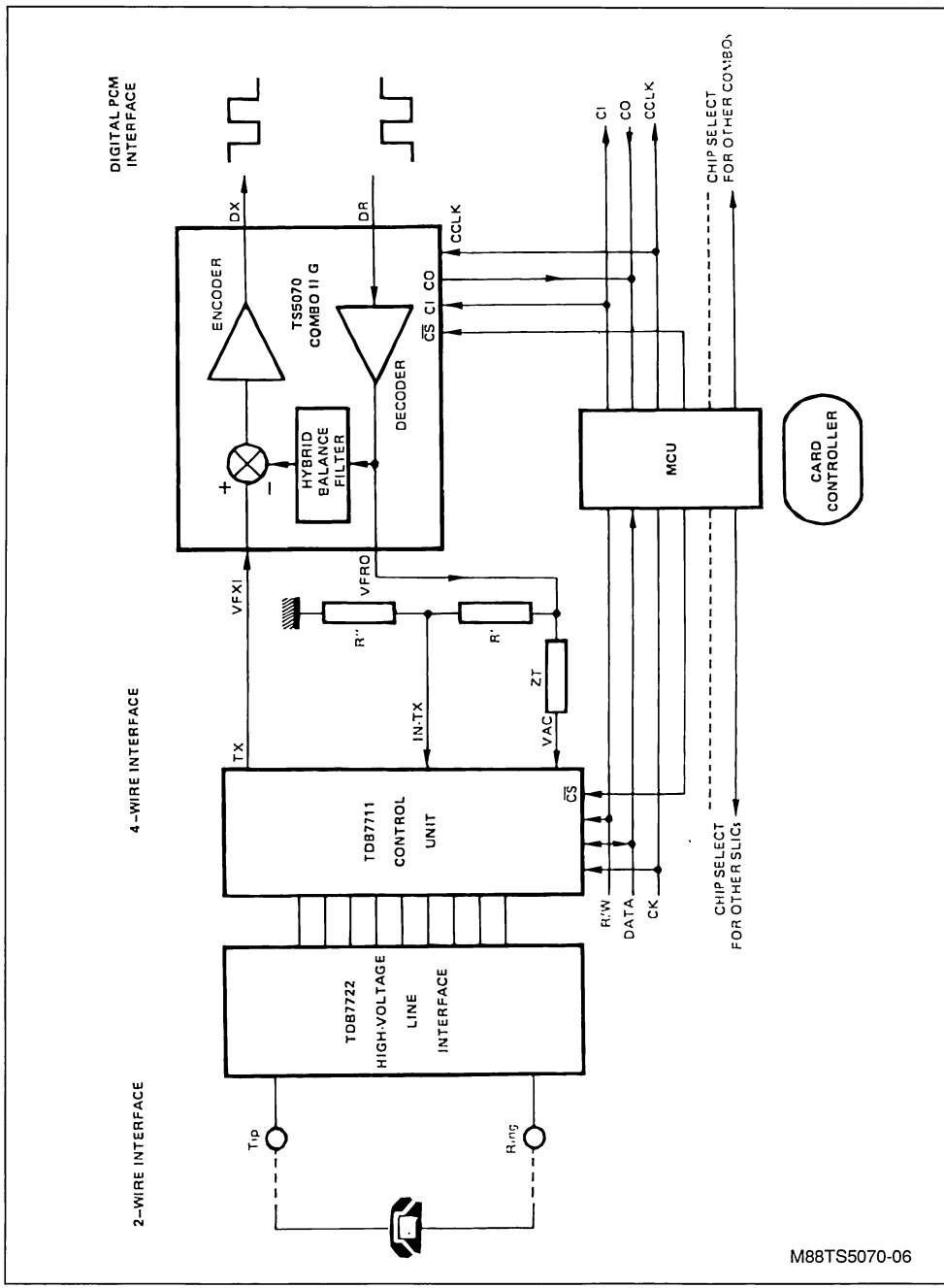
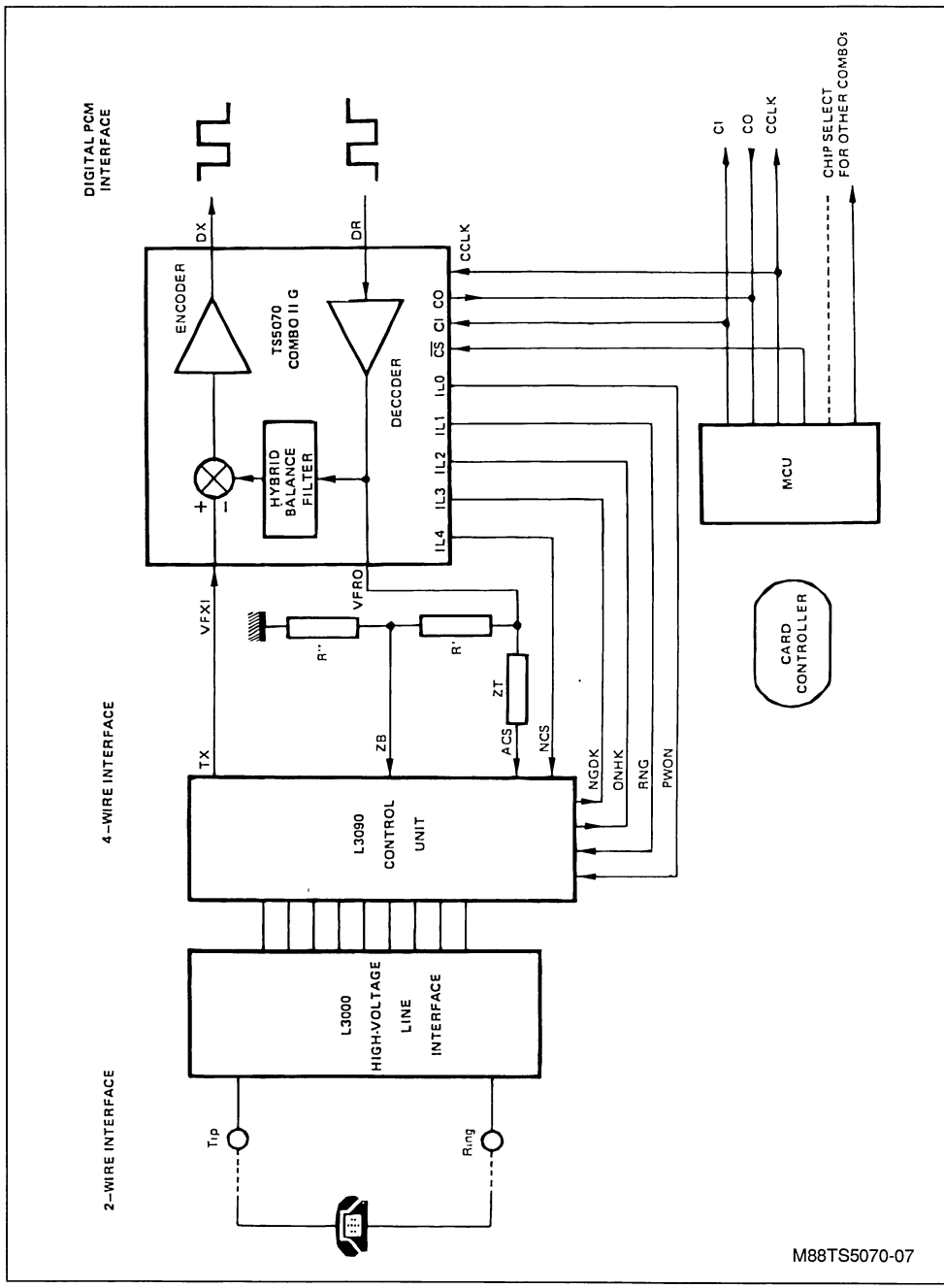


Figure 4 : Interface with L3090 + L3000 Silicon SLIC.



ELECTRICAL OPERATING CHARACTERISTICS

Unless otherwise noted, limits in **BOLD** characters are guaranteed for V_{CC} = + 5 V ± 5 % ; V_{SS} = − 5 V ± 5 %. T_A = 0 °C to 70 °C by correlation with 100 % electrical testing at T_A = 25 °C. All other limits are assured by correlation with other production tests and/or product design and characterisation. All signals referenced to GND. Typicals specified at $V_{CC = +5\ V, VSS}$ = − 5 V, T_A = 25 °C.

DIGITAL INTERFACE

Symbol	Parameter		Min.	Typ.	Max.	Unit
V_{IL}	Input Low Voltage	All Digital Inputs			**0.7**	V
V_{IH}	Input high Voltage	All Digital Inputs	**2.0**			
V_{OL}	Output Low Voltage	D_X0 and D_X1, $\overline{TS_XO}$, $\overline{TS_X1}$ and CO, IL = 3. 2 mA All Other Digital Outputs, IL = 1 mA			**0.4**	V
V_{OH}	Output high Voltage	D_X0 and D_X1 and CO, I_L = − 3.2 mA All other digital outputs except $\overline{TS_X}$, IL = − 1 mA All Digital Outputs, I_L = − 100 µA	**2.4** V_{CC}–0.5			V V
I_{IL}	Input Low Current all Digital Inputs (GND < V_{IN} < V_{IL})		**− 10**		**10**	µA
I_{IH}	Input High Current all Digital Inputs Except MR (V_{IH} < V_{IN} < V_{CC})		**− 10**		**10**	µA
I_{IH}	Input High Current on MR		**− 10**		**100**	µA
I_{OZ}	Output Current in High Impedance State (TRI–STATE) D_X0 and D_X1, CO and CI/O (as an input) IL5 – IL0 as Inputs (GND < V_O < V_{CC})		**− 10**		**10**	µA

ANALOG INTERFACE

Symbol	Parameter		Min.	Typ.	Max.	Unit
I_{VFXI}	Input Current VF_XI (− 3.3 V < VF_XI < 3.3 V)		**− 10**		**10**	µA
R_{VFXI}	Input Resistance VF_XI (− 3.3 V < VF_XI < 3.3 V)		**390**	620		kΩ
VOS_X	Input offset voltage at VF_XI	0dBm0= − 19 dBm 0dBm0 = + 6.4 dBm			20 200	mV mV
RL_{VFRO}	Load Resistance at VF_RO (− 3.5 V < VF_RO < 3.5 V)		**300**			Ω
CL_{VFRO}	Load Capacitance CL_{VFRO} from VF_RO to GND				**200**	pF
RO_{VFRO}	Output Resistance VF_RO (steady zero PCM code applied to D_R0 or D_R1)			1	3	Ω
V_{OSR}	Output Offset Voltage at VF_RO (alternating ± zero PCM code applied to D_R0 or D_R1, 0dBm0 = 8.1 dBm)		**− 200**		**200**	mV

ELECTRICAL OPERATING CHARACTERISTICS (continued)

POWER DISSIPATION

Symbol	Parameter	Min.	Typ.	Max.	Unit
ICC0	Power Down Current (CCLK, CI/O, CI = 0.4 V, $\overline{CS}$ = 2.4 V) Interface latches set as outputs with no load. All Other Inputs active, Power Amp Disabled		.3	**1.5**	mA
–ISS0	Power Down Current (as above)		.1	**0.3**	mA
ICC1	Power Up Current (CCLK, CI/O, CI = 0.4 V, $\overline{CS}$ = 2.4 V) No Load on Power Amp Interface latches set as outputs with no load.		7	**10**	mA
–ISS1	Power Up Current (as above)		7	**10**	mA

TIMING SPECIFICATIONS

Unless otherwise noted, limits in BOLD characters are guaranteed for V_{CC} = + 5 V ± 5 % ; V_{SS} = 5 V ± 5 %. T_A = 0 °C to 70 °C by correlation with 100 % electrical testing at T_A = 25 °C. All other limits are assured by correlation with other production tests and/or product design and characterization. All signals referenced to GND. Typicals specified at V_{CC} = + 5 V, V_{SS} = 5 V, T_A = 25 °C. All timing parameters are measured at V_{OH} = 2.0 V and V_{OL} = 0.7 V.

See Definitions and Timing Conventions section for test methods information.

MASTER CLOCK TIMING

Symbol	Parameter	Min.	Typ.	Max.	Unit
f_{MCLK}	Frequency of MCLK (selection of frequency is programmable, see table 2)		512 1.536 1.544 2.048 **4.096**		kHz MHz MHz MHz MHz
t_{WMH}	Period of MCLK High (measured from V_{IH} to V_{IH}, see note 1)	**80**			ns
t_{WML}	Period of MCLK Low (measured from V_{IL} to V_{IL}, see note 1)	**80**			ns
t_{RM}	Rise Time of MCLK (measured from V_{IL} or V_{IH})			30	ns
t_{FM}	Fall Time of MCLK (measured from V_{IH} to V_{IL})			30	
t_{HBM}	Hold Time, BCLK Low to MCLK High (TS5070 only)	**50**			ns
t_{WFL}	Period of FS_X or FS_R Low	2			µs

TIMING SPECIFICATIONS (continued)

PCM INTERFACE TIMING

Symbol	Parameter	Min.	Typ.	Max.	Unit
f_{BCLK}	Frequency of BCLK (may vary from 64 kHz to 4.096 MHz in 8 kHz increments, TS5070 only)	**64**		**4.096**	kHz
t_{WBH}	Period of BCLK High (measured from V_{IH} to V_{IH})	**80**			ns
t_{WBL}	Period of BCLK Low (measured from V_{IL} to V_{IL})	**80**			ns
t_{RB}	Rise Time of BCLK (measured from V_{IL} to V_{IH})			30	ns
t_{FB}	Fall Time of BCLK (measured from V_{IH} to V_{IL})			30	ns
t_{HBF}	Hold Time, BCLK Low to $FS_{X/R}$ High or Low	**0**			ns
t_{SFB}	Setup Time $FS_{X/R}$ High to BCLK Low	**30**			ns
t_{DBD}	Delay Time, BCLK High to Data Valid (load = 100 pF plus 2 LSTTL loads)			**80**	ns
t_{DBZ}	Delay Time from BCLK8 Low to Dx disabled (if FSx already low) ; FSx Low to Dx Disabled (if BCLK8 low) ; BCLK9 High to Dx Disabled (if $\overline{FSx}$ still high) ;	**15**		**80**	ns
t_{DBT}	Delay Time, from BCLK and FS_X Both High to $\overline{TS_X}$ Low (load = 100 pF plus 2 LSTTL loads)			60	ns
t_{ZBT}	Delay Time from BCLK8 low to $\overline{TSx}$ Disabled (if FSx already low) ; FSx Low to $\overline{TSx}$ Disabled (if BCLK8 low) ; BCLK9 High to TSx Disabled (if FSx still high) ;	15		60	ns
t_{DFD}	Delay Time, FS_X High to Data Valid (load = 100 pF plus 2 LSTTL loads, applies if FS_X rises later than BCLK rising edge in non–delayed data mode only)			**80**	ns
t_{SDB}	Setup Time , D_R 0/1 Valid to BCLK Low	**30**			ns
t_{HDB}	Hold Time, BCLK Low to D_R 0/1 Invalid	**10**			ns

Note : 1. Applies only to MCLK frequencies ≥ 1.536 MHz. At 512 kHz a 50:50 ± 2 % duty cycle must be used.

Figure 5 : Non Delayed Data Timing (long frame mode).

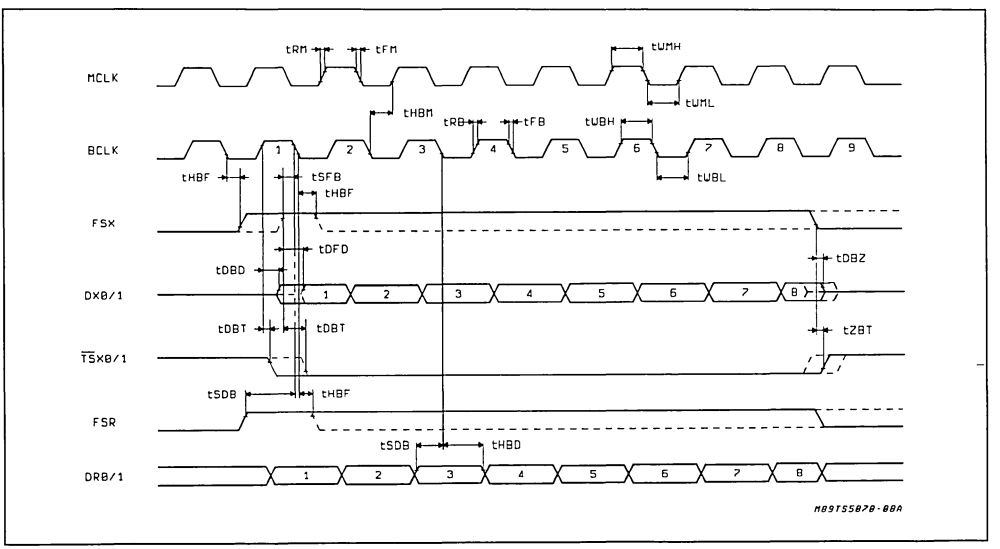
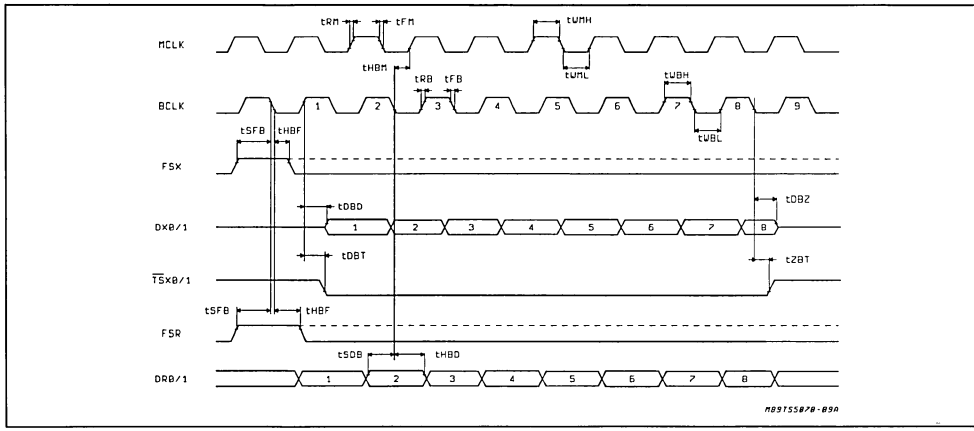


Figure 6 : Delayed Data Timing (short frame mode).



SERIAL CONTROL PORT TIMING

Symbol	Parameter	Min.	Typ.	Max.	Unit
f_{CCLK}	Frequency of CCLK			**2.048**	MHz
t_{WCH}	Period of CCLK High (measured from V_{IH} to V_{IH})	**160**			ns
t_{WCL}	Period of CCLK Low (measured from V_{IL} to V_{IL})	**160**			ns
t_{RC}	Rise Time of CCLK (measured from V_{IL} to V_{IH})			50	ns
t_{FC}	Fall Time of CCLK (measured from V_{IH} to V_{IL})			50	ns
t_{HCS}	Hold Time, CCLK Low to $\overline{CS}$ Low (CCLK1)	**10**			ns
t_{HSC}	Hold Time, CCLK Low to $\overline{CS}$ High (CCLK8)	**100**			ns
t_{SSC}	Setup Time, $\overline{CS}$ Transition to CCLK Low	**70**			ns
t_{SSCO}	Setup Time, $\overline{CS}$ Transition to CCLK High (to insure CO is not enabled for single byte)	**50**			ns
t_{SDC}	Setup Time, CI (CI/O) Data in to CCLK low	**50**			ns
t_{HCD}	Hold Time, CCLK Low to CI (CI/O) Invalid	50			ns
t_{DCD}	Delay Time, CCLK High to CO (CI/O) Data Out Valid (load = 100 pF plus 2 LSTTL loads)			**50**	ns
t_{DSD}	Delay Time, $\overline{CS}$ Low to CO (CI/O) Valid (applies only if separate $\overline{CS}$ used for byte 2)			**50**	ns
t_{DDZ}	Delay Time, $\overline{CS}$ or CCLK9 High to CO (CI/O) High Impedance (applies to earlier of $\overline{CS}$ high or CCLK9 high)	15		80	ns

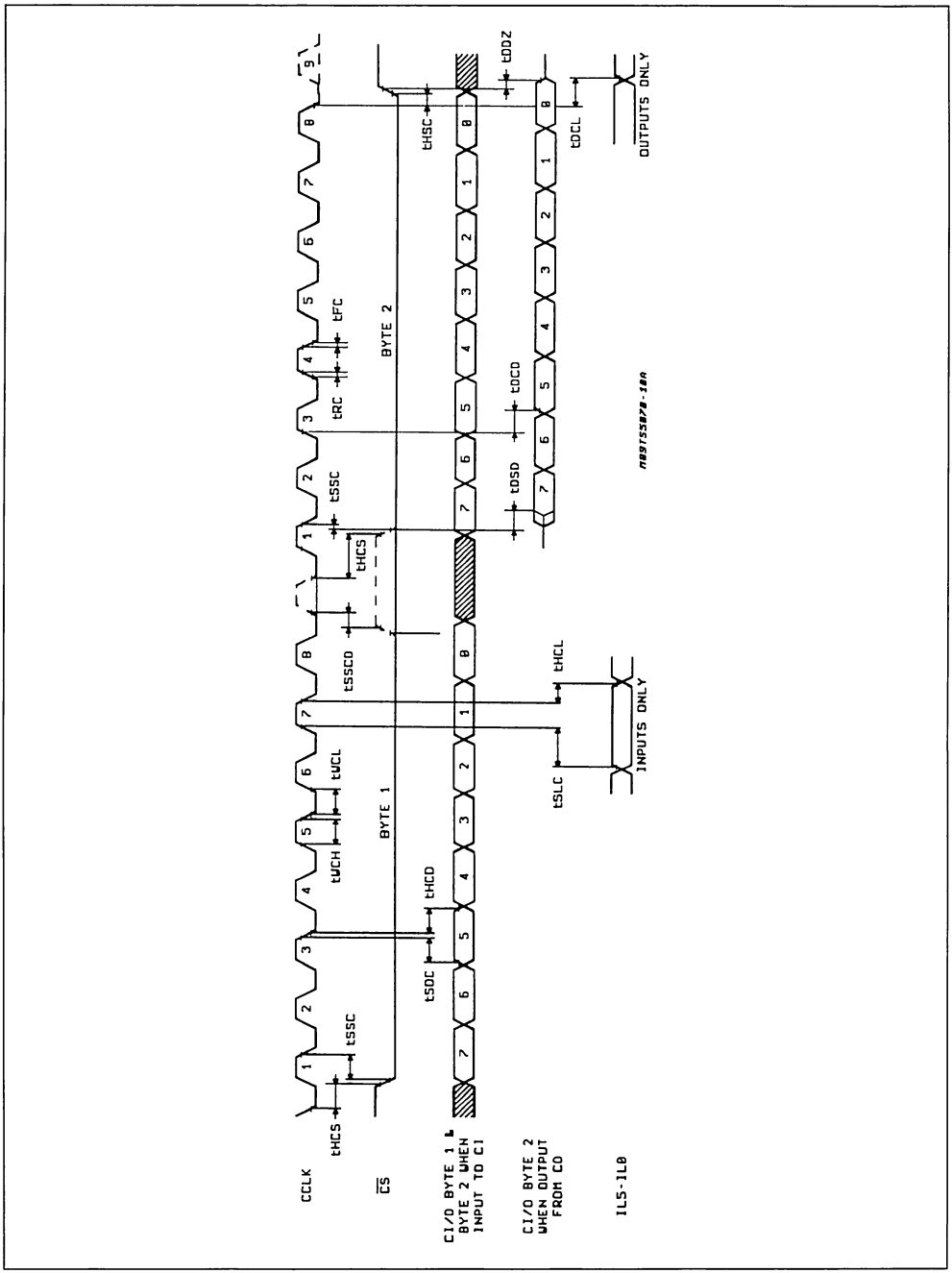
INTERFACE LATCH TIMING

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{SLC}	Setup Time, I_L Valid to CCLK 8 of Byte 1 Low. I_L as Input	**100**			ns
t_{HCL}	Hold Time, I_L Valid from CCLK 8 of Byte 1 Low. I_L as Input	50			ns
t_{DCL}	Delay Time, CCLK 8 of Byte 2 Low to I_L. C_L = 50 pF. I_L as Output			200	ns

MASTER RESET PIN

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{WMR}	Duration of Master Reset High	1			µs

Figure 7 : Control Port Timing.



TRANSMISSION CHARACTERISTICS

Unless otherwise noted, limits printed in BOLD characters are guaranteed for V_{CC} = + 5 V ± 5 % ; V_{SS} = – 5 V ± 5 %, T_A = 0 °C to 70 °C by correlation with 100 % electrical testing at T_A = 25 °C. f = 1015.625 Hz, VF_XI = 0 dBm0, D_R0 or D_R1 = 0 dBm0 PCM code, Hybrid Balance filter disabled. All other limits are assured by correlation with other production tests and/or product de-sign and characterization. All signals referenced to GND. dBm levels are into 600 ohms. Typicals specified at V_{CC} = + 5 V, V_{SS} = 5 V, T_A = 25 °C.

AMPLITUDE RESPONSE

Symbol	Parameter	Min.	Typ.	Max.	Unit
	Absolute levels				
	The nominal 0 dBm 0 levels are :				
	VF_XI 0 dB Tx Gain		1.618		Vrms
	25.4 dB Tx Gain		86.9		mVrms
	VF_RO 0 dB Rx Attenuation (RL ≥ 15 kΩ)		1.968		Vrms
	0.5 dB Rx Attenuation (RL ≥ 600 Ω)		1.858		Vrms
	1.2 dB Rx Attenuation (RL ≥ 300 Ω)		1.714		Vrms
	25.4 dB Rx Attenuation		105.7		mVrms
	Maximum Overload				
	The nominal overload levels are :				
	A-law				
	VF_XI 0 dB Tx Gain		2.323		Vrms
	25.4 dB Tx Gain		124.8		mVrms
	VF_RO 0 dB Rx Attenuation (R_L ≥ 15 kΩ)		2.825		Vrms
	0.5 dB Rx Attenuation (R_L ≥ 300 Ω)		2.667		Vrms
	1.2 dB Rx Attenuation (R_L ≥ 300 Ω)		2.461		Vrms
	25.4 dB Rx Attenuation		151.7		mVrms
	μ-law				
	VF_XI 0 dB Tx Gain		2.332		Vrms
	25.4 dB Tx Gain		125.2		mVrms
	VF_RO 0 dB Rx Attenuation (R_L ≥ 15 kΩ)		2.836		Vrms
	0.5 dB Rx Attenuation (R_L ≥ 600 Ω)		2.677		Vrms
	1.2 dB Rx Attenuation (R_L ≥ 300 Ω)		2.470		Vrms
	25.4 dB Rx Attenuation		152.3		mVrms
	Transmit Gain Absolute Accurary				
GXA	Transmit Gain Programmed for 0 dBm0 = 6.4 dBm, A-law Measure Deviation of Digital Code from Ideal 0 dBm0 PCM Code at $D_X0/1$, f = 1015.625 Hz T_A = 25 °C, V_{CC} = 5 V, V_{SS} = – 5 V	**– 0.15**		**0.15**	dB
	Transmit gain Variation with Programmed Gain				
GXAG	– 19 dBm ≤ 0 dBm0 ≤ 6.4 dBm Calculate the Deviation from the Programmed Gain Relative to GXA i.e., GXAG = Gactual – Gprog – GXA T_A = 25 °C, V_{CC} = 5 V, V_{SS} = – 5 V	**– 0.1**		**0.1**	dB

AMPLITUDE RESPONSE (continued)

Symbol	Parameter	Min.	Typ.	Max.	Unit
GXAF	**Transmit Gain Variation with Frequency**				
	Relative to 1015.625 Hz (note 2)				
	– 19 dBm ≤ 0 dBm0 ≤ 6.4 dBm				
	D_R0 (or D_R1) = 0 dBm0 Code				
	f = 60 Hz			– 26	dB
	f = 200 Hz	– 1.8		– 0.1	dB
	f = 300 Hz to 3000 Hz	– 0.15		0.15	dB
	f = 3400 Hz	– 0.7		0	dB
	f = 4000 Hz			– 14	dB
	f ≥ 4600 Hz Measure Response at Alias Frequency from 0 kHz to 4 kHz			– 32	dB
	0 dBm0 = 6.4 dBm				
	VF_XI = – 4 dBm0 (note 2)				
	f = 62.5 Hz			**– 24.9**	dB
	f = 203.125 Hz	**– 1.7**		**– 0.1**	dB
	f = 2093.750 Hz	**– 0.15**		**0.15**	dB
	f = 2984.375 Hz	**– 0.15**		**0.15**	dB
	f = 3296.875 Hz	**– 0.15**		**0.15**	dB
	f = 3406.250 Hz	**– 0.7**		**0**	dB
	f = 3984.375 Hz			**– 13.5**	dB
	f = 4593.750 Hz, Measure 3406.25 Hz			**– 32**	dB
	f = 5015.625 Hz, Measure 2984.375 Hz			**– 32**	dB
	f = 10015.625 Hz, Measure 2015.625 Hz			**– 32**	dB
GXAT	**Tansmit Gain Variation with Temperature**				
	Measured Relative to G_{XA}, V_{CC} = 5 V, V_{SS} = – 5 V				
	– 19 dBm ≤ 0 dBm0 ≤ 6.4 dBm	– 0.1		0.1	dB
GXAV	**Transmit Gain Variation with Supply**				
	V_{CC} = 5 V ± 5 %, V_{SS} = – 5 V ± 5 %				
	Measured Relative to GXA				
	T_A = 25 °C, 0 dBm0 = 6.4 dBm	**– 0.05**		**0.05**	dB
GXAL	**Transmit Gain Variation with Signal Level**				
	Sinusoidal Test Method, Reference Level = 0 dBm0				
	VF_xI = – 40 dBm0 to + 3 dBm0	**– 0.2**		**0.2**	dB
	VF_xI = – 50 dBm0 to – 40 dBm0	**– 0.4**		**0.4**	dB
	VF_xI = – 55 dBm0 to – 50 dBm0	**– 1.2**		**1.2**	dB
GRA	**Receive Gain Absolute Accuracy**				
	0 dBm0 = 8.1 dBm, A-law				
	Apply 0 dBm0 PCM Code to D_R0 or D_R1 Measure VF_RO	**– 0.15**		**0.15**	dB
	T_A = 25 °C, V_{CC} = 5 V, V_{SS} = – 5 V				
GRAG	**Receive Gain Variation with Programmed Gain**				
	– 17.3 dBm ≤ 0 dBm0 ≤ 8.1 dBm				
	Calculate the Deviation from the Programmed Gain Relative to GRA	**– 0.1**		**0.1**	dB

AMPLITUDE RESPONSE (continued)

Symbol	Parameter	Min.	Typ.	Max.	Unit
	i.e. GRAG = Gactual – Gprog – GRA T_A = 25 °C, V_{CC} = 5 V, V_{SS} = – 5 V				
GRAT	**Receive Gain Variation with Temperature** Measured Relative to GRA V_{CC} = 5 V, V_{SS} = – 5 V – 17.3 dBm ≤ 0 dBm0 ≤ 8.1 dBm	– 0.1		0.1	dB
GRAV	**Receive Gain Variation with Supply** Measured Relative to G_{RA} V_{CC} = 5 V ± 5 %, V_{SS} = – 5 V ± 5 % T_A = 25 °C, 0 dBm 0 = 8.1 dBm	**– 0.05**		**0.05**	dB
GRAF	**Receive Gain Variation with Frequency** Relative to 1015.625 Hz, (note 2) D_R0 or D_R1 = 0 dBm0 Code – 17.3 dBm ≤ 0 dBm0 ≤ 8.1 dBm f = 200 Hz f = 300 Hz to 3000 Hz f = 3400 Hz f = 4000 Hz GR = 0 dBm0 = 8.1 dBm GX = D_R0 = – 4 dBm0 f = 296.875 Hz f = 1906.250 Hz f = 2812.500 Hz f = 2984.375 Hz f = 3406.250 Hz f = 3984.375 Hz	 – 0.25 – 0.15 – 0.7 **– 0.15** **– 0.15** **– 0.15** **– 0.15** **– 0.7**		 0.15 0.15 0 – 14 **0.15** **0.15** **0.15** **0.15** **0** **– 13.5**	 dB dB dB dB dB dB dB dB dB dB
GRAL	**Receive Gain Variation with Signal Level** Sinusoidal Test Method Reference Level = 0 dBm0 D_R0 = – 40 dBm0 to + 3 dBm0 D_R0 = – 50 dBm0 to – 40 dBm0 D_R0 = – 55 dBm0 to – 50 dBm0	 **– 0.2** **– 0.4** **– 1.2**		 **0.2** **0.4** **1.2**	 dB dB dB

ENVELOPPE DELAY DISTORTION WITH FREQUENCY

Symbol	Parameter	Min.	Typ.	Max.	Unit
DXA	**Tx Delay Absolute**			315	µs
	f = 1600 Hz				
DXR	**Tx Delay, Relative**				
	f = 500 – 600 Hz			220	µs
	f = 600 – 800 Hz			145	µs
	f = 800 – 1000 Hz			75	µs
	f = 1000 – 1600 Hz			40	µs
	f = 1600 – 2600 Hz			75	µs
	f = 2600 – 2800 Hz			105	µs
	f = 2800 – 3000 Hz			155	µs
DRA	**Rx Delay, Absolute**				
	f = 1600 Hz			200	µs
DRR	**Rx Delay, Relative**				
	f = 500 – 1000 Hz	– 40			µs
	f = 1000 – 1600 Hz	– 30			µs
	f = 1600 – 2600 Hz			90	µs
	f = 2600 – 2800 Hz			125	µs
	f = 2800 – 3000 Hz			175	µs

NOISE

Symbol	Parameter	Min.	Typ.	Max.	Unit
NXC	**Transmit Noise, C Message Weighted** μ-law Selected (note 3) o dBm0 = 6.4 dBm		12	**15**	dBrnC0
NXP	**Transmit Noise, Psophometric Weighted** A-law Selected (note 3) 0 dBm0 = 6.4 dBm		– 74	**– 67**	dBm0p
NRC	**Receive Noise, C Message Weighted** μ-law Selected PCM code is alternating positive		8	**11**	dBrnC0
NRP	**Receive Noise, Psophometric Weighted** A-law Selected PCM Code Equals Positive Zero		– 82	**– 79**	dBm0p
NRS	**Noise, Single Frequency** f = 0 kHz to 100 kHz, Loop Around Measurement VF_XI = 0 Vrms			– 53	dBm0
PPSRX	**Positive Power Supply Rejection Transmit** V_{CC} = 5 V_{DC} + 100 mVrms f = kHz – 50 kHz (note 4)	**30**			dBp
NPSRX	**Negative Power Supply Rejection Transmit** V_{SS} = – 5 VDC + 100 mVrms	**30**			dBp
PPSRR	**Positive Power Supply Rejection Receive** PCM Code Equals Positive Zero V_{CC} = 5 V_{DC} + 100 mVrms Measure VF_R0 f = 0 Hz – 4000 Hz f = 4 kHz – 25 kHz f = 25 kHz – 50 kHz	 **30** 40 36			 dBp dB dB
NPSRR	**Negative Power Supply Rejection Receive** PCM Code Equals Positive Zero V_{SS} = – 5 V_{DC} + 100 mVrms Measure VF_RO f = 0 Hz – 4000 Hz f = 4 kHz – 25 kHz f = 25 kHz – 50 kHz	 **30** 40 36			 dBp dB dB
SOS	**Spurious Out-of Band Signals at the Channel Output** 0 dBm0 300 Hz to 3400Hz input PCM applied at D_R0 (D_R1) 4600 Hz – 7600 Hz 7600 Hz – 8400 Hz 8400 Hz – 100 000 Hz			 – 30 – 40 – 30	 dB dB dB

DISTORTION

Symbol	Parameter	Min.	Typ.	Max.	Unit
STDX	**Signal to Total Distortion Transmit** Sinusoidal Test Method Half Channel				
	Level = 3 dBm0	**33**			dBp
	– 30 dBm0 to 0 dBm0	**36**			dBp
	– 40 dBm0	**29**			dBp
	– 45 dBm0	**25**			dBp
STDR	**Signal to Total Distortion Receive** Sinusoidal Test Method Half Channel				
	Level = 3 dBm0	**33**			dBp
	– 30 dBm0 to 0 dBm0	**36**			dBp
	– 40 dBm0	**30**			dBp
	– 45 dBm0	**25**			dBp
SFDX	Single frequency Distortion Transmit			**– 46**	dB
SFDR	Single Frequency Distortion Receive			**– 46**	dB
IMD	Intermodulation Distortion Transmit or Receive Two Frequencies in the Range 300 Hz – 3400 Hz			**– 41**	dB

CROSSTALK

Symbol	Parameter	Min.	Typ.	Max.	Unit
CTX-R	transmit to Receive Crosstalk, 0 dBm0 Transmit Level f = 300 – 3400 Hz DR = Steady PCM Code		– 90	**– 75**	dB
CTR-X	Receive to transmit Crosstalk, 0 dBm0 Receive Level f = 300 – 3400 Hz, (note 4)		– 90	**– 70**	dB

Notes : 1. Applies only to MCLK frequencies ≥ 1 536 MHz At 512 kHz A 50·50 ± 2 % duty cycle must be used.
2 A multi-tone test technique is used (peak/rms ≤ 9 5 dB)
3 Measured by extrapolation from distortion test result at – 50 dBm0
4 PPSRX, NPSRX and CTR-X are measured with a – 50 dBm0 activation signal applied to VF_XI.
A signal is Valid if it is above V_{IH} or below V_{IL} and invalid if it is between V_{IL} and V_{IH}. For the purpose of the specification the following conditions apply :
a) All input signals are defined as V_{IL} = 0.4 V, V_{IH} = 2.7 V, t_R < 10 ns, t_F 10 ns
b) t_R is measured from V_{IL} to V_{IH}, t_F is measured from V_{IH} to V_{IL}
c) Delay Times are measured from the input signal Valid to the clock input invalid
d) Setup Times are measured from the data input Valid to the clock input invalid
e) Hold Times are measured from the clock signal Valid to the data input invalid
f) Pulse widths are measured from V_{IL} to V_{IL} or from V_{IH} to V_{IH}

DEFINITIONS AND TIMING CONVENTIONS

DEFINITIONS

V_{IH}	V_{IH} is the D.C. input level above which an input level is guaranteed to appear as a logical one. This parameter is to be measured by performing a functional test at reduced clock speeds and nominal timing (i.e. not minimum setup and hold times or output strobes), with the high level of all driving signals set to V_{IH} and maximum supply voltages applied to the device.
V_{IL}	V_{IL} is the D.C. input level below which an input level is guaranteed to appear as a logical zero the device. This parameter is measured in the same manner as V_{IH} but with all driving signal low levels set to V_{IL} and minimum supply voltage applied to the device.
V_{OH}	V_{OH} is the minimmum D.C. output level to which an output placed in a logical one state will converge when loaded at the maximum specified load current.
V_{OL}	V_{OL} is the maximum D.C. output level to which an output placed in a logical zero state will converge when loaded at the maximum specified load current.
Threshold Region	The threshold region is the range of input voltages between V_{IL} and V_{IH}.
Valid Signal	A signal is Valid if it is in one of the valid logic states. (i.e. above V_{IH} or below V_{IL}). In timing specifications, a signal is deemed valid at the instant it enters a valid state.
Invalid signal	A signal is invalid if it is not in a valid logic state, i.e., when it is in the threshold region between V_{IL} and V_{IH}. In timing specifications, a signal is deemed Invalid at the instant it enters the threshold region.

TIMING CONVENTIONS

For the purpose of this timing specifications the following conventions apply :

Input Signals	All input signals may be characterized as : $V_L = 0.4$ V, $V_H = 2.4$ V, tR < 10 ns, tF < 10 ns.
Period	The period of the clock signal is designated as tPxx where xx represents the mnemonic of the clock signal being specified.
Rise Time	Rise times are designated as tRyy, where yy represents a mnemonic of the signal whose rise time is being specified, tRyy is measured from V_{IL} to V_{IH}.
Fall Time	Fall times are designated as tFyy, where yy represents a mnemonic of the signal whose fall time is being specified, tFyy is measured from V_{IH} to V_{IL}.
Pulse Width High	The high pulse width is designated as tWzzH, where zz represents the mnemonic of the input or output signal whose pulse width is being specified. High pulse width are measured from V_{IH} to V_{IH}.
Pulse Width Low	The low pulse is designated as tWzzL' where zz represents the mnemonic of the input or output signal whose pulse width is being specified. Low pulse width are measured from V_{IL} to V_{IL}.
Setup Time	Setup times are designated as tSwwxx where ww represents the mnemonic of the input signal whose setup time is being specified relative to a clock or strobe input represented by mnemonic xx. Setup times are measured from the ww Valid to xx Invalid.
Hold Time	Hold times are designated as THwwxx where ww represents the mnemonic of the input signal whose hold time is being specified relative to a clock or strobe input represented by the mnemonic xx. Hold times are measured from xx Valid to ww Invalid.
Delay Time	Delay times are designated as TDxxyy [H/L], where xx represents the mnemonic of the input reference signal and yy represents the mnemonic of the output signal whose timing is being specified relative to xx. The mnemonic may optionally be terminated by an H or L to specify the high going or low going transition of the output signal. Maximum delay times are measured from xx Valid to yy Valid. Minimum delay times are measured from xx Valid to yy Invalid. This parameter is tested under the load conditions specified in the Conditions column of the Timing Specifications section of this datasheet.

SGS-THOMSON MICROELECTRONICS

ST5075
ST5076

PROGRAMMABLE CODEC / FILTER FOR ISDN AND DIGITAL PHONE APPLICATIONS

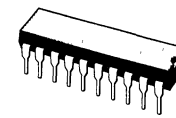
ADVANCE DATA

- COMPLETE CODEC AND FILTER SYSTEM INCLUDING :
  - TRANSMIT AND RECEIVE PCM CHANNEL FILTERS
  - μ-LAW OR A-LAW COMPANDING CODER AND DECODER
  - RECEIVE POWER AMPLIFIER DRIVES 300 Ω
  - 4.096 MHz SERIAL PCM DATA (max)
- PROGRAMMABLE FUNCTIONS :
  - TRANSMIT GAIN : 25.4 dB RANGE, 0.1 dB STEPS
  - RECEIVE GAIN : 25.4 dB RANGE, 0.1 dB STEPS
  - TIME-SLOT ASSIGNMENT : UP to 64 SLOT/FRAME
  - 2 PORT ASSIGNMENT (ST5075)
  - 6 INTERFACE LATCHES (ST5075)
  - 4 INTERFACE LATCH (ST5076)
  - A or μ-LAW
  - ANALOG LOOPBACK
  - DIGITAL LOOPBACK
- STANDARD SERIAL CONTROL INTERFACE
- 70 mW OPERATING POWER (typ)
- 2 mW STANDBY POWER (typ)
- MEETS OR EXCEEDS ALL CCITT AND LSSGR SPECIFICATIONS
- TTL AND CMOS COMPATIBLE DIGITAL INTERFACES
- SECOND SOURCE OF TP3075, TP3076/COMBO II ®

DESCRIPTION

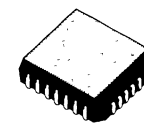
The ST5075/76 series are second generation combined PCM CODEC and Filter devices optimized for digital switching applications on subscriber and trunk line cards. Using advanced switched capacitor techniques the ST5075/76 combines transmit bandpass and receive lowpass channel filters with a companding PCM encoder and decoder. The devices are A-law and μ-law selectable and employ a conventional serial PCM interface capable of being clocked up to 4.096 MHz. A number of programmable functions may be controlled via a serial control port.

Channel gains are programmable over a 25.4 dB range in each direction.



DIP20
(Plastic)

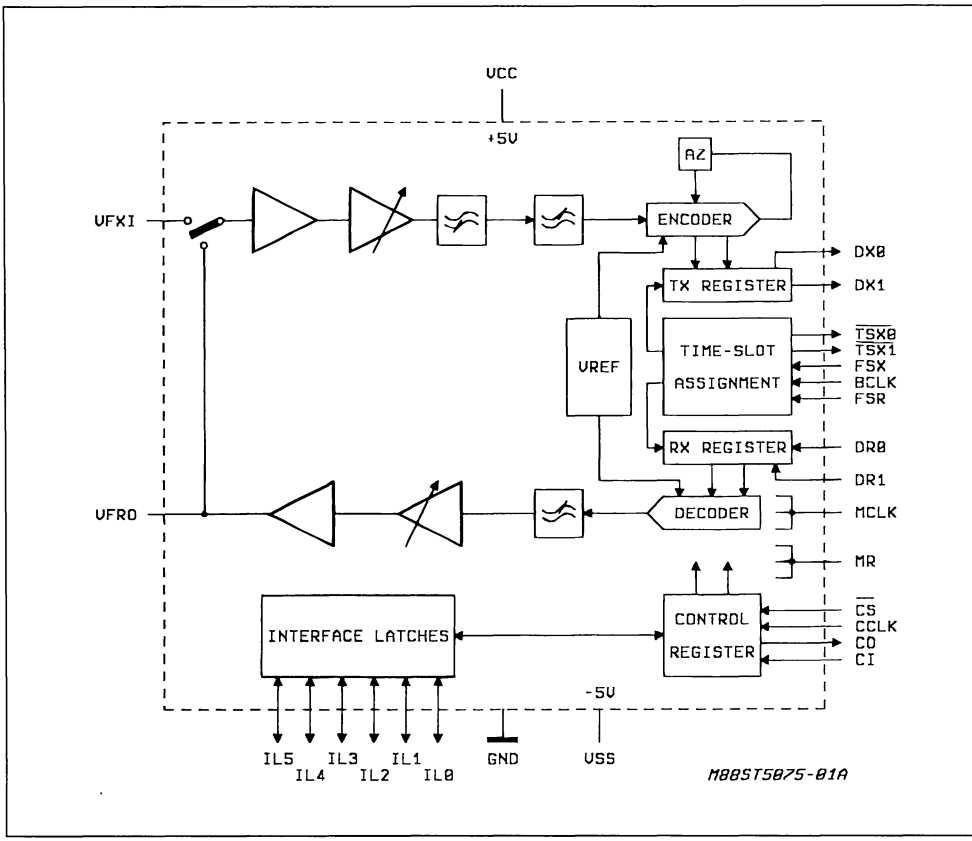
ORDER CODE : ST5076N



PLCC28

ORDER CODE : ST5075FN

A number of programmable latches are included ; each may be configured as either an input or an output. The ST5075 provides 6 latches and the ST5076 4 latches.

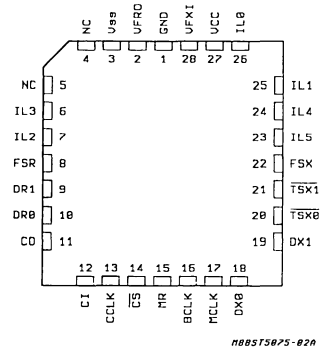


ABSOLUTE MAXIMUM RATINGS

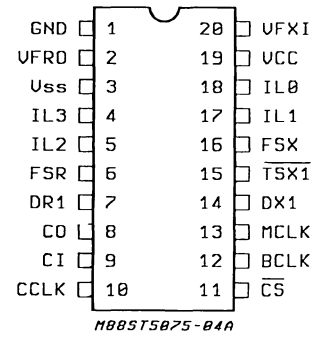
Symbol	Parameter	Value	Unit
V_{CC}	V_{CC} to GND	7	V
V_{SS}	V_{SS} to GND	– 7	V
	Voltage at VFXI	V_{CC} + 0.5 to V_{SS} – 0.5	V
V_{IN}	Voltage at Any Digital Input	V_{CC} + 0.5 to GND – 0.5	V
	Current at VFRO	± 100	mA
I_O	Current at Any Digital Output	± 50	mA
T_{stg}	Storage Temperature Range	– 65, + 150	°C
T_{lead}	Lead Temperature Range (soldering, 10 seconds)	300	°C

PIN CONNECTIONS

PLCC28



DIP20



PIN DESCRIPTION

POWER SUPPLY, CLOCK

Name	Pin Type	ST5075	ST5076	Function	Description
V_{CC}	S	27	19	Positive Power Supply	+ 5 V ± 5 %
V_{SS}	S	3	3	Negative Power Supply	− 5 V ± 5 %
GND	S	1	1	Ground	All analog and digital signals are referenced to this pin.
BCLK	I	16	12	Bit Clock	Bit clock input used to shift PCM data into and out of the D_R and D_X pins. BCLK may vary from 64 kHz to 4.096 MHz in 8 kHz increments, and must be synchronous with MCLK.
MCLK	I	17	13	Master Clock	Master clock input used by the switched capacitor filters and the encoder and decoder sequencing logic. Must be 512 kHz, 1.536/1.544 MHz, 2.048 MHz or 4.096 MHz and synchronous with BCLK.

PIN DESCRIPTION (continued)

TRANSMIT SECTION

Name	Pin Type	ST5075	ST5076	Function	Description
FS_X	I	22	16	Transmit Frame Sync.	Normally a pulse or squarewave waveform with an 8 kHz repetition rate is applied to this input to define the start of the transmit time-slot assigned to this device (non-delayed data mode) or the start of the transmit frame (delayed data mode using the internal time-slot assignment counter).
VF_XI	I	28	20	Transmit Analog	This is a high-impedance input. Voice frequency signals present on this input are encoded as an A–law or μ–law PCM bit stream and shifted out on the selected D_X pin.
D_X0 D_X1	O O	18 19	14	Transmit Data	D_X0 is available on the ST5075 only, D_X1 is available on all devices. These transmit data TRI–STATE® outputs remain in the high impedance state except during the assigned transmit time-slot on the assigned port, during wich the transmit PCM data byte is shifted out on the rising edges of BCLK.
$\overline{TS_X0}$ TS_X1	O O	20 21	15	Transmit Time–slot	$\overline{TS_X0}$ is available on the ST5075 only. TS_X1 is available on all devices. Normally these opendrain outputs are floating in a high impedance state except when a time–slot is active on one of the D_X outputs, when the appropriate $\overline{TS_X}$ outputs pulls low to enable a blackplane line–driver. Should be strapped to ground (GND) when not used.

RECEIVE SECTION

Name	Pin Type	ST5075 FN	ST5076	Function	Description
FS_R	I	8	6	Receive Frame Sync.	Normally a pulse or squarewave waveform with an 8 kHz repetition rate is applied to this input to define the start of the receive time–slot assigned to this device (non–delayed frame mode) or the start of the receive frame(delayed frame mode using the internal time–slot assignment counter).
VF_RO	O	2	2	Receive Analog	The receive analog power amplifier output, capable of driving load impedances as low as 300 Ω (depending on the peak overload level required). PCM data received on the assigned D_R pin is decoded and appears at this output as voice frequency signals.
D_R0 D_R1	I I	10 9	7	Receive Data	$\overline{D_R0}$ is available on the ST5075 only, D_R1 is available on all devices. These receive data input(s) are inactive except during the assigned receive time–slot of the assigned port when the receive PCM data is shifted in on the falling edges of BCLK.

PIN DESCRIPTION (continued)

INTERFACE, CONTROL, RESET

Name	Pin Type	ST5075 FN	ST5076	Function	Description
IL5 IL4 IL3 IL2 IL1 IL0	I/O I/O I/O I/O I/O I/O	23 24 6 7 25 26	– – 4 5 17 18	Interface Latches	IL5 through IL0 are available on the ST5075, IL3 through IL0 are available on the ST5076. Each Interface Latch I/O pin may be individually programmed as an input or an output determined by the state of the corresponding bit in the Latch Direction Register (LDR). For pins configured as inputs, the logic state sensed on each input is latched into the Interface Latch Register (ILR) whenever control data is written to COMBO IIG, while $\overline{CS}$ is low, and the information is shifted out on the CO pin. When configured as outputs, control data written into the ILR appears at the corresponding IL pins.
CCLK	I	13	10	Control Clock	This clock shifts serial control information into or out of CI or CO when the $\overline{CS}$ input is low depending on the current instruction. CCLK may be asynchronous with the other system clocks.
CI	I	12	9	Control Data Input	Serial control information is shifted into COMBO II on this pin when $\overline{CS}$ is low.
CO	O	11	8	Control Data Output	Serial control or status information is shiftted out of COMBO II on this pin $\overline{CS}$ is low.
$\overline{CS}$	I	14	11	Chip Select	When this pin is low, control information can be written into or out of COMBO IIG via the CI and CO pins.
MR	I	15	–	Master Reset	This logic input must be pulled low for normal operation of COMBO IIG. When pulled momentarily high, all programmable registers in the device are reset to the states specified under "Power–on Initialization". Not available on ST5076.

FUNCTIONAL DESCRIPTION

POWER-ON INITIALIZATION

When power is first applied, power-on reset circuitry initializes COMBO IIG and puts it into the power-down state. The gain control registers for the transmit and receive gain sections are programmed for not output, the power amp is disabled and the device is in the non-delayed timing mode. The Latch Direction Register (LDR) is pre-set with all IL pins programmed as inputs, placing the SLIC interface pins in a high impedance state. The CO pin is TRI-STATE condition.

A reset to these same initial conditions may also be forced by driving the MR pin momentarily high (ST5075 only). This may be done either when powered-up or down. For normal operation this pin must be pulled low.

The desired modes for all programmable functions may be initialized via the control port prior to a Power-up command.

POWER-DOWN STATE

Following a period of activity in the powered-up state the power-down state may be re-entered by writing a Power-Down instruction into the serial control port as indicated in table 1. The power down instruction may be included within any other instruction code. It is recommended that the chip be powered down before executing any instructions. In the power-down state, all non-essential circuitry is de-activated and the D_X0 and D_X1 outputs are in the high impedance TRI-STATE condition.

The coefficients stored in the Gain Control registers, the data in the LDR and ILR, and all control bits remain unchanged in the power-down state unless changed by writing new data via the serial control port, which remains operational. The outputs of the Interface Latches also remain active.

TRANSMIT FILTER AND ENCODER

The Transmit section input, VF_XI is a high impedance input. No external components are needed to set the gain. Following this circuit is a programmable gain/attenuation amplifier which is controlled by the contents of the Transmit Gain Register (see Programmable Functions section). An active prefilter then precedes the 3rd order high-pass and 5th order low-pass switched capacitor filters. The A/D converted has a compressing characteristic according to the standard CCITT A or μ255 coding laws, which must be selected by a control instruction during initialization (see table 1 and 2). A precision on-chip voltage reference ensures accurate and highly stable transmission levels. Any offset voltage arising in the gain-set amplifier, the filters or the comparator is cancelled by an internal auto-zero circuit.

Each encode cycle begins immediately following the assigned Transmit time-slot. The total signal delay referenced to the start of the time-slot is approximately 165 μs (due to the Transmit Filter) plus 125 μs (due to encoding delay), which totals 290 μs. Data is shifted out on D_X0 or D_X1 during the selected time slot on eight rising edges of BCLK.

DECODER AND RECEIVE FILTER

PCM data is shifted into the Decoder's Receive PCM Register via the D_R0 or D_R1 pin during the selected time-slot on the 8 falling edges of BCLK. The Decoder consists of an expanding DAC with either A or μ255 law decoding characteristic, which is selected by the same control instruction used to select the Encode law during initialization. Following the Decoder is a 5th order low-pass switched capacitor filter with integral Sin x/x correction for the 8 kHz sample and hold. A programmable gain amplifier, which must be set by writing to the Receive Gain Register, is included, and finally a Post-Filter/Power Amplifier capable of driving a 300 Ω load to ± 3.5 V, a 600 Ω load to ± 3.8 V or 15 kΩ load to ± 4.0 V at peak overload.

A decode cycle begins immediately after each receive time-slot, and 10 μs later the Decoder DAC output is updated. The total signal delay is 10 μs plus 120 μs (filter delay) plus 62.5 μs (1/2 frame) which gives approximately 190 μs.

PCM INTERFACE

The FS_X and FS_R frame sync inputs determine the beginning of the 8-bit transmit and receive time-slots respectively. They may have any duration from a single cycle of BCLK to a square wave. Two different relationships may be established between the frame sync inputs and the actual time-slots on the PCM busses by setting bit 3 in the Control Register (see table 2). Non delayed data mode is similar to long-frame timing on the ETC 5050/60 series of devices : time-slots being nominally coincident with the rising edge of the appropriate FS input. The alternative is to use Delayed Data mode which is similar to short-frame sync timing, in which each FS input must be high at least a half-cycle of BCLK earlier than the time-slot.

The Time-Slot Assignment circuit on the device can only be used with Delayed Data timing. When using Time-Slot Assignment, the beginning of the first time-slot in a frame is identified by the appropriate FS input. The actual transmit and receive time-slot are then determined by the internal Time-Slot Assignment counters. Transmit and Receive frames and time-slots may be skewed from each other by any number of BCLK cycles.

During each assigned transmit time-slot, the selected $D_X0/1$ output shifts data out from the PCM register on the rising edges of BCLK. TS_X0 (or TS_X1 as appropriate) also pulls low for the first 7 1/2 bit times of the time-slot to control the TRI-STATE Enable of a backplane line driver. Serial PCM data is shifted into the selected $D_R0/1$ input during each assigned Receive time slot on the falling edges of BCLK. D_X0 or D_X1 and D_R0 or D_R1 are selectable on the ST5075 only.

SERIAL CONTROL PORT

Control information and data are written into or read-back from COMBO IIG via the serial control port consisting of the control clock CCLK ; the serial data input CI, and output CO and the Chip Select input CS. All control instructions require 2 bytes, as listed in table 1, with the exception of a single byte power-

up/down command. To shift control data into COMBO IIG, CCLK must be pulsed high 8 times while CS is low. Data on the CI input is shifted into the serial input register on the falling edge of each CCLK pulse. After all data is shifted in, the contents of the input shift register are decoded, and may indicate that a 2nd byte of control data will follow. This second byte may either be defined by a second byte-wide CSpulse or may follow the first continuously, i.e. it is not mandatory for CS to return high in between the first and second control bytes. On the falling edge of the 8th CCLK clock pulse in the 2nd control byte the data is loaded into the appropriate programmable register. CS may remain low continuously when programming successive registers, if desired. However CS should be set high when no data transfers are in progress.

To readback interface Latch data or status information from COMBO IIG, the first byte of the appropriate instruction is strobed in during the first CS pulse, as defined in table 1. CS must then be taken low for a further 8 CCLK cycles, during which the data is shifted onto the CO pin on the rising edges of CCLK. When CS is high the CO pin is in the high-impedance TRI-STATE, enabling the CI and CO pins of many devices to be multiplexed together. Thus, to summarize, 2-byte READ and WRITE ins-tructions may use either two 8-bit wide CS pulses or a single 16-bit wide CS pulse.

Table 1 : Programmable Register Instructions.

Function	Byte 1								Byte 2
	7	6	5	4	3	2	1	0	
Single Byte Power–up/down	P	X	X	X	X	X	0	X	None
Write Control Register	P	0	0	0	0	0	1	X	See Table 2
Read–back Control Register	P	0	0	0	0	1	1	X	See Table 2
Write Latch Direction Register (LDR)	P	0	0	1	0	0	1	X	See Table 4
Read Latch Direction Register	P	0	0	1	0	1	1	X	See Table 4
Write Latch Content Register (ILR)	P	0	0	0	1	0	1	X	See Table 5
Read Latch Content Register	P	0	0	0	1	1	1	X	See Table 5
Write Transmit Time–slot/port	P	1	0	1	0	0	1	X	See Table 6
Read–back Transmit Time–slot/port	P	1	0	1	0	1	1	X	See Table 6
Write Receive Time–slot/port	P	1	0	0	1	0	1	X	See Table 6
Read–back Receive Time–slot/port	P	1	0	0	1	1	1	X	See Table 6
Write Transmit Gain Register	P	0	1	0	1	0	1	X	See Table 7
Read Transmit Gain Register	P	0	1	0	1	1	1	X	See Table 7
Write Receive Gain Register	P	0	1	0	0	0	1	X	See Table 8
Read Receive Gain Register	P	0	1	0	0	1	1	X	See Table 8

Notes : 1. Bit 7 of bytes 1 and 2 is always the first bit clocked into or out of the CI or CO pin
2. "P" is the power-up/down control bit, see "Power-up" section ("0" = Power-Up, 1 = Power Down).
X = Don't Care.

PROGRAMMABLE FUNCTIONS

POWER-UP/DOWN CONTROL

Following power-on initialization, power-up and power-down control may be accomplished by writing any of the control instructions listed in table 1 into COMBO IIG with the "P" bit set to "0" for power-up or "1" for power-down. Normally it is recommended that all programmable functions be initially programmed while the device is powered down. Power state control can then be included with the last programming instruction or the separate single-byte instruction. Any of the programmable registers may also be modified while the device is powered-up or down be setting the "P" bit as indicated. When the power up or down control is entered as a single byte ins-truction, bit one must be set to a 0.

When a power-up command is given, all de-activated circuits are activated, but the TRI-STATE PCM output(s), D_X0 (and D_X1), will remain in the high impedance state until the second FS_X pulse after power-up.

CONTROL REGISTER INSTRUCTION

The first byte of a READ or WRITE instruction to the Control Register is as shown in table 1. The second byte functions are detailed in table 2.

MASTER CLOCK FREQUENCY SELECTION

A Master clock must be provided to COMBO IIG for operation of the filter and coding/decoding functions. The MCLK frequency must be either 512 kHz, 1.536 MHz, 1.544 MHz, 2.048 MHz, or 4.096 MHz and must be synchronous with BCLK. Bits F_1 and F_0 (see table 2) must be set during initialization to select the correct internal divider.

CODING LAW SELECTION

Bits "MA" and "IA" in table 2 permit the selection of μ255 coding or A-law coding with or without even-bit inversion.

ANALOG LOOPBACK

Analog Loopback mode is entered by setting the "AL" and "DL" bits in the Control Register as shown in table 2. In the analog loopback mode, the Transmit input VF_XI is isolated from the input pin and internally connected to the VF_RO output, forming a loop from the Receive PCM Register back to the Transmit PCM Register. The VF_RO pin remains active, and the programmed settings of the Transmit and Receive gains remain unchanged, thus care must be taken to ensure that overload levels are not exceeded anywhere in the loop.

DIGITAL LOOPBACK

Digital Loopback mode is entered by setting the "DL" bit in the Control Register as shown in table 2. This mode provides another stage of path verification by enabling data written into the Receive PCM Register to be read back from that register in any Transmit time-slot at D_X0 or D_X1.

For Analog Loopback as well as for Digital Loopback PCM decoding continues and analog output appears at VF_RO. The output can be disabled by programming "no output" in the Receive Gain Register (see table 8).

Table 2 : Control Register Byte 2 Functions.

Bit Number								Function
7	6	5	4	3	2	1	0	
F1	F0	MA	IA	DN	DL	AL	PP	
0 0 1 1	0 1 0 1							MCLK = 512 kHz MCLK = 1.536 or 1.544 MHz MCLK = 2.048 MHz (*) MCLK = 4.096 MHz
		0 1 1	X 0 1					Select μ. 255 Law (*) A-law, Including Even Bit Inversion A-Law, No Even Bit Inversion
				0 1				Delayed Data Timing Non-delayed Data Timing (*)
					0 1 0	0 X 0		Normal Operation (*) Digital Loopback Analog Loopback
							0 1	Power Amp Enabled in PDN Power Amp Disabled in PDN (*)

(*) = State at power on initialization (bit 4 = 0).

	μ255 Law								True A–law Including Even Bit Inversion								A–law Without Even Bit Inversion							
	MSB							LSB	MSB							LSB	MSB							LSB
V_{IN} = + Full Scale	1	0	0	0	0	0	0	0	0	1	0	1	0	1	0	1	0	1	1	1	1	1	1	1
V_{IN} = 0 V	1	1	1	1	1	1	1	1	1	1	1	0	1	0	1	0	1	1	0	0	0	0	0	0
	0	1	1	1	1	1	1	1	1	0	1	0	1	0	1	0	1	0	0	0	0	0	0	0
V_{IN} = – Full Scale	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0	0	1	1	1	1	1	1

Note : The MSB is always the first PCM bit shifted in or out of COMBO IIG

INTERFACE LATCH DIRECTIONS

Immediately following power-on, all Interface Latches assume they are inputs, and therefore all IL pins are in a high impedance state. Each IL pin may be individually programmed as a logic input or output by writing the appropriate instruction to the LDR, see table 1 and 4. Bits L_5-L_0 must be set by writing the specific instruction to the LDR with the L bits in the second byte set as specified in table 4. Unused interface latches should be programmed as outputs.

Table 4 : Byte 2 Functions of Latch Direction Register.

Bit Number							
7	6	5	4	3	2	1	0
L0	L1	L2	L3	L4	L5	X	X

L_N Bit	IL Direction
0	Input *
1	Output

* = State at power-on initialization.

Note : L4 and L5 should be programmed as an output for the ST5076.

INTERFACE LATCH STATES

Interface Latches configured as outputs assume the state determined by the appropriate data bit in the 2-byte instruction written to the Latch Register (ILR) as shown in tables 1 and 5. Latches configured as inputs will sense the state applied by an external source, such as the Off-Hook detect output of a SLIC. All bits of the ILR, i.e. sensed inputs and the programmed state of outputs, can be read back in the 2nd byte of a READ from the ILR. It is recommended that, during initialization, the state of IL pins to be configured as outputs should first be programmed, followed immediately by the Latch Direction Register.

Table 5 : Interface Latch Data Bit Order.

Bit Number							
7	6	5	4	3	2	1	0
D0	D1	D2	D3	D4	D5	X	X

TIME-SLOT ASSIGNMENT

COMBO IIG can operate in either fixed time-slot or time-slot assignment mode for selecting the Transmit and Receive PCM time-slots. Following power-on, the device in automatically in Non-Delayed Timing mode, in which the time-slot always begins with the leading (rising) edge of frame sync inputs FS_X and FS_R. Time-Slot Assignment may only be used with Delayed Data timing : see figure 6. FS_X and FS_R may have any phase relationship with each other in BCLK period increments.

Table 6 : Byte 2 of Time-slot and Port Assignment Instructions.

Bit Number								Function
7 EN	6 PS (note 1)	5 T5 (note 2)	4 T4	3 T3	2 T2	1 T1	0 T0	
0	X	X	X	X	X	X	X	Disable D_X Outputs (transmit instruction) * Disable D_R Inputs (receive instruction) *
1	0	Assign One Binary Coded Time-slot from 0–63						Enable D_X0 Output, Disable D_X1 Output (Transmit instruction) Enable D_R0 Input, Disable D_R1 Input (receive instruction)
		Assign One Binary Coded Time-slot from 0–63						
1	1	Assign One Binary Coded Time-slot from 0–63						Enable D_X1 Output, Disable D_X0 Output (Transmit instruction) Enable D_R1 Input, Disable D_R0 Input (receive instruction)
		Assign One Binary Coded Time-slot from 0–63						

* = State at power-on initialization.

Notes : 1. The "PS" bit MUST always be set to 1 for the ST5076.
2. T5 is the MSB of the time-slot assignment.

Alternatively, the internal time-slot assignment counters and comparators can be used to access any time-slot in a frame, using the frame sync inputs as marker pulses for the beginning of transmit and receive time-slot 0. In this mode, a frame may consist of up to 64 time-slots of 8 bits each. A time-slot is assigned by a 2-byte instruction as shown in table 1 and 6. The last 6 bits of the second byte indicate the selected time-slot from 0-63 using straight binary notation. A new assignment becomes active on the second frame following the end of the Chip Select for the second control byte. The "EN" bit allows the PCM inputs $D_R0/1$ or outputs $D_X0/1$, as appropriate, to be enabled or disabled.

Time-Slot Assignment mode requires that the FS_X and FS_R pulses must conform to the delayed timing format shown in figure 6.

PORT SELECTION

On the ST5075 only, an additional capability is available : 2 Transmit serial PCM ports, D_X0 and D_X1 are 2 receive serial PCM ports, D_R0 and D_R1, are provided to enable two-way space switching to be implemented. Port selections for transmit and receive are made within the appropriate time-slot assignment instruction using the "PS" bit in the second byte.

On the ST5076, only ports D_X1 and D_R1 are available, therefore the "PS" bit MUST always be set to 1 for these devices.

Table 6 shows the format for the second byte of both transmit and receive time-slot and port assignment instructions.

TRANSMIT GAIN INSTRUCTION BYTE 2

The transmit gain can be programmed in 0.1 dB steps by writing to the Transmit Gain Register as defined in tables 1 and 7. This corresponds to a range of 0 dBm0 levels at VF_XI between 1.375 Vrms and 0.075 Vrms (equivalent to + 5.0 dBm to – 20.4 dBm in 600 Ω). To calculate the binary code for byte 2 of this instruction for any desired input 0 dBm0 level in Vrms, take the nearest integer to the decimal number given by :

$$200 \times \log_{10} (V/\sqrt{0.6}) + 205$$

and convert to the binary equivalent. Some examples are given in table 7.

Table 7 : Byte 2 of Transmit Gain Instructions.

Bit Number								0 dBm0 Test Level at VF_XI	
7	6	5	4	3	2	1	0	In dBm (into 600 Ω)	In Vrms
0	0	0	0	0	0	0	0	No Output *	
0	0	0	0	0	0	0	1	– 20.4	0. 074
0	0	0	0	0	0	1	0	– 20.5	0. 075
1	1	0	0	1	1	0	1	0	0. 775
1	1	1	1	1	1	1	0	+ 4.9	1.36
1	1	1	1	1	1	1	1	+ 5.0	1.38

* = State at power initialization.

RECEIVE GAIN INSTRUCTION BYTE 2

The receive gain can be programmed in 0.1 dB steps by writing to the Receive Gain Register as defined in table 1 and 8. Note the following restriction on output drive capability :

a) 0 dBm0 levels ≤ 1.97 Vrms at VF_RO may be driven into a load of ≥ 15 kΩ to GND,

b) 0 dBm0 levels ≤ 1.86 Vrms at VF_RO may be driven into a load of ≥ 600 Ω to GND,

c) 0 dBm0 levels ≤ 1.71 Vrms at VF_RO may be driven into a load of ≥ 300 Ω to GND.

To calculate the binary code for byte 2 of this instruction for any desired output 0 dBm0 level in Vrms, take the nearest integer to the decimal number given by :

$$200 \times \log_{10} (V/\sqrt{0.6}) + 174$$

and convert to the binary equivalent. Some examples are given in table 8.

Table 8 : Byte 2 of Receive Gain Instruction.

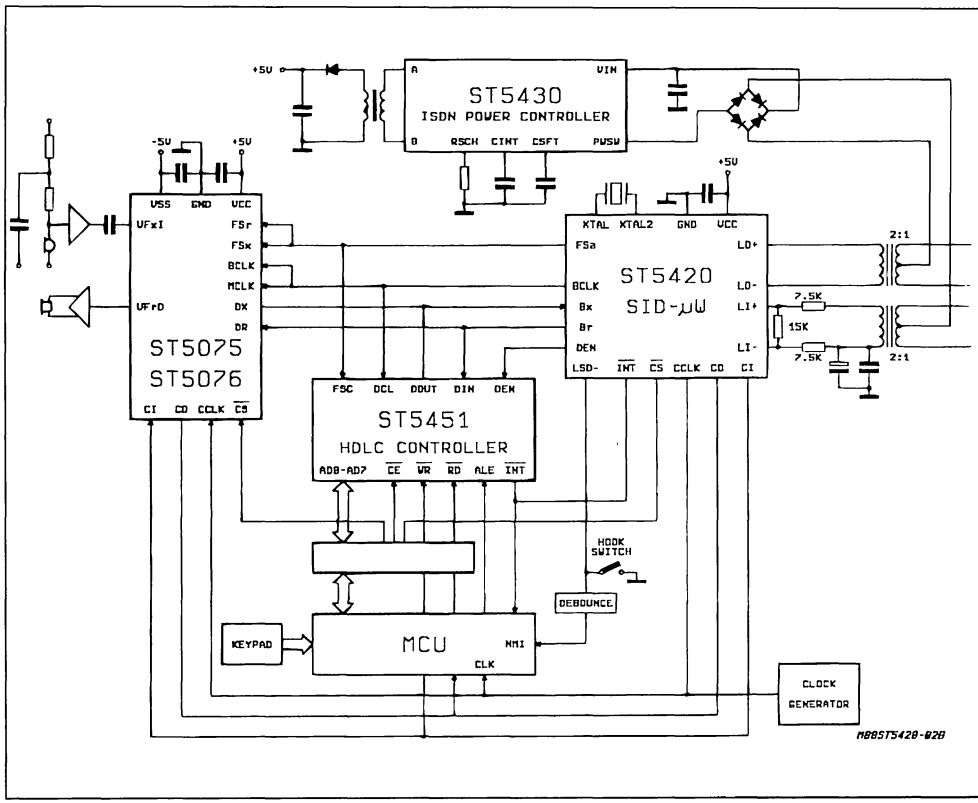
Bit Number								0 dBm0 Test Level at VF_RO	
7	6	5	4	3	2	1	0	In dBm (into 600 Ω)	In Vrms
0	0	0	0	0	0	0	0	No Output * (low Z to GND)	
0	0	0	0	0	0	0	1	− 17. 3	0. 106
0	0	0	0	0	0	1	0	− 17. 2	0. 107
1	0	1	0	1	1	1	0	0	0. 775
1	1	1	1	0	0	1	1	+ 6. 9 (note 1)	1. 71
1	1	1	1	1	0	1	0	+ 7.6 (note 2)	1. 86
1	1	1	1	1	1	1	1	+ 8.1 (note 3)	1. 97

Notes : 1. Maximum level into 300 Ω.
2. Maximum level into 600 Ω
3. RL ≥ 15 kΩ.
* = State at power on initialization

APPLICATIONS INFORMATIONS

Figure 1 shows a typical ISDN phone application of ST5076 together with a ST5420 S Interface device and ST5451 HDLC controller.

Figure 1 : Voice Terminal Application Diagram.



POWER SUPPLIES

While the pins of the ST5075 and TS5076/COMBO IIG devices are well protected against electrical misuse, it is recommended that the standard CMOS practice of applying GND to the device before any other connections are made should always be followed. In applications where the printed circuit card may be plugged into a hot socket with power and clocks already present, an extra long ground pin on the connector should be used and a schottky diode connected between V_{SS} and GND. To minimize noise sources all ground connections to each device should meet at a common point as close as possible to the GND pin in order to prevent the interaction of ground return currents flowing through a common bus impedance. Power supply decoupling capacitors of 0.1 µF should be connected from this common device ground point to V_{CC} and V_{SS} as close to the device pins as possible. V_{CC} and V_{SS} should be decoupled with low effective series resistance capacitors of at least 10 µF near the card edge connector.

ELECTRICAL OPERATING CHARACTERISTICS

Unless otherwise noted, limits in **BOLD** characters are guaranteed for V_{CC} = + 5 V ± 5 % ; V_{SS} = – 5 V ± 5 %. T_A = 0 °C to 70 °C by correlation with 100 % electrical testing at T_A = 25 °C. All other limits are assured by correlation with other production tests and/or product design and characterisation. All signals referenced to GND. Typicals specified at V_{CC} = + 5 V, V_{SS} = – 5 V, T_A = 25 °C.

DIGITAL INTERFACE

Symbol	Parameter		Min.	Typ.	Max.	Unit
V_{IL}	Input Low Voltage	All Digital Inputs			**0.7**	V
V_{IH}	Input High Voltage	All Digital Inputs	**2.0**			
V_{OL}	Output Low Voltage	D_X0 and D_X1, $\overline{TS_X0}$, $\overline{TS_X1}$ and CO, IL = 3. 2 mA All Other Digital Outputs, IL = 1 mA			**0.4**	V
V_{OH}	Output High Voltage	D_X0 and D_X1 and CO, I_L = – 3.2 mA All other digital outputs except $\overline{TS_X}$, IL = – 1 mA All Digital Outputs, I_L = – 100 µA	**2.4** V_{CC}–0.5			V V
I_{IL}	Input Low Current all Digital Inputs (GND < V_{IN} < V_{IL})		**– 10**		**10**	µA
I_{IH}	Input High Current all Digital Inputs Except MR (V_{IH} < V_{IN} < V_{CC})		**– 10**		**10**	µA
I_{IH}	Input High Current on MR		**– 10**		**100**	µA
I_{OZ}	Output Current in High Impedance State (TRI–STATE) D_X0 and D_X1, CO IL5 – IL0 as Inputs (GND < V_O < V_{CC})		**– 10**		**10**	µA

ANALOG INTERFACE

Symbol	Parameter		Min.	Typ.	Max.	Unit
I_{VFXI}	Input Current VF_XI (– 3.3 V < VF_XI < 3.3 V)		**– 1.0**		**1.0**	µA
R_{VFXI}	Input Resistance VF_XI (– 3.3 V < VF_XI < 3.3 V)		**1.0**			MΩ
VOS_X	Input offset voltage at VF_XI	0dBm0= – 20.4 dBm 0dBm0 = + 5.0 dBm			20 200	mV mV
RL_{VFRO}	Load Resistance at VF_RO (– 3.5 V < VF_RO < 3.5 V)		**300**			Ω
CL_{VFRO}	Load Capacitance CL_{VFRO} from VF_RO to GND				**200**	pF
RO_{VFRO}	Output Resistance VF_RO (steady zero PCM code applied to D_R0 or D_R1)			1	3	Ω
V_{OSR}	Output Offset Voltage at VF_RO (alternating ± zero PCM code applied to D_R0 or D_R1, 0dBm0 = 8.1 dBm)		**– 200**		**200**	mV

ELECTRICAL OPERATING CHARACTERISTICS (continued)

POWER DISSIPATION

Symbol	Parameter	Min.	Typ.	Max.	Unit
ICC0	Power Down Current (CCLK, CI = 0.4 V, $\overline{CS}$ = 2.4 V) Interface latches set as outputs with no load. All Other Inputs active, Power Amp Disabled		.3	**1.5**	mA
–ISS0	Power Down Current (as above)		.1	**0.3**	mA
ICC1	Power Up Current (CCLK, CI = 0.4 V, $\overline{CS}$ = 2.4 V) No Load on Power Amp Interface latches set as outputs with no load.		7	**10**	mA
–ISS1	Power Up Current (as above)		7	**10**	mA

TIMING SPECIFICATIONS

Unless otherwise noted, limits in BOLD characters are guaranteed for V_{CC} = + 5 V ± 5 % ; V_{SS} = 5 V ± 5 %. T_A = 0 °C to 70 °C by correlation with 100 % electrical testing at T_A = 25 °C. All other limits are assured by correlation with other production tests and/or product design and characterization. All signals referenced to GND. Typicals specified at V_{CC} = + 5 V, V_{SS} = 5 V, T_A = 25 °C. All timing parameters are mesured at V_{OH} = 2.0 V and V_{OL} = 0.7 V.

See Definitions and Timing Conventions section for test methods information.

MASTER CLOCK TIMING

Symbol	Parameter	Min.	Typ.	Max.	Unit
f_{MCLK}	Frequency of MCLK (selection of frequency is programmable, see table 2)		512 1.536 1.544 2.048 **4.096**		kHz MHz MHz MHz MHz
t_{WMH}	Period of MCLK High (measured from V_{IH} to V_{IH}, see note 1)	**80**			ns
t_{WML}	Period of MCLK Low (measured from V_{IL} to V_{IL}, see note 1)	**80**			ns
t_{RM}	Rise Time of MCLK (measured from V_{IL} or V_{IH})			30	ns
t_{FM}	Fall Time of MCLK (measured from V_{IH} to V_{IL})			30	
t_{HBM}	Hold Time, BCLK Low to MCLK High	**50**			ns
t_{WFL}	Period of FS_X or FS_R Low	2			µs

TIMING SPECIFICATIONS (continued)

PCM INTERFACE TIMING

Symbol	Parameter	Min.	Typ.	Max.	Unit
f_{BCLK}	Frequency of BCLK (may vary from 64 kHz to 4.096 MHz in 8 kHz increments)	**64**		**4.096**	kHz
t_{WBH}	Period of BCLK High (measured from V_{IH} to V_{IH})	**80**			ns
t_{WBL}	Period of BCLK Low (measured from V_{IL} to V_{IL})	**80**			ns
t_{RB}	Rise Time of BCLK (measured from V_{IL} to V_{IH})			30	ns
t_{FB}	Fall Time of BCLK (measured from V_{IH} to V_{IL})			30	ns
t_{HBF}	Hold Time, BCLK Low to $FS_{X/R}$ High or Low	**0**			ns
t_{SFB}	Setup Time $FS_{X/R}$ High to BCLK Low	**30**			ns
t_{DBD}	Delay Time, BCLK High to Data Valid (load = 100 pF plus 2 LSTTL loads)			**80**	ns
t_{DBZ}	Delay Time from BCLK8 Low to Dx Disabled (if FS_X already low) FS_X Low to Dx Disabled (if BCLK8 low) BCLK9 High to Dx Disabled (if FS_X still high)	**15**		**80**	ns
t_{DBT}	Delay Time, from BCLK and FS_X Both High to $\overline{TS_X}$ Low (load = 100 pF plus 2 LSTTL loads)			60	ns
t_{ZBT}	Delay Time from BCLK8 low to TS_X Disabled (if FS_X already low) FS_X Low to $\overline{TS_X}$ Disabled (if BCLK8 low) BCLK9 High to TS_X Disabled (if FS_X still high)	15		60	ns
t_{DFD}	Delay Time, FS_X High to Data Valid (load = 100 pF plus 2 LSTTL loads, applies if FS_X rises later than BCLK rising edge in non–delayed data mode only)			**80**	ns
t_{SDB}	Setup Time , D_R 0/1 Valid to BCLK Low	**30**			ns
t_{HDB}	Hold Time, BCLK Low to D_R 0/1 Invalid	**10**			n

Note : 1 Applies only to MCLK frequencies ≥ 1 536 MHz. At 512 kHz a 50.50 ± 2 % duty cycle must be used.

Figure 5 : Non Delayed Data Timing (long frame mode).

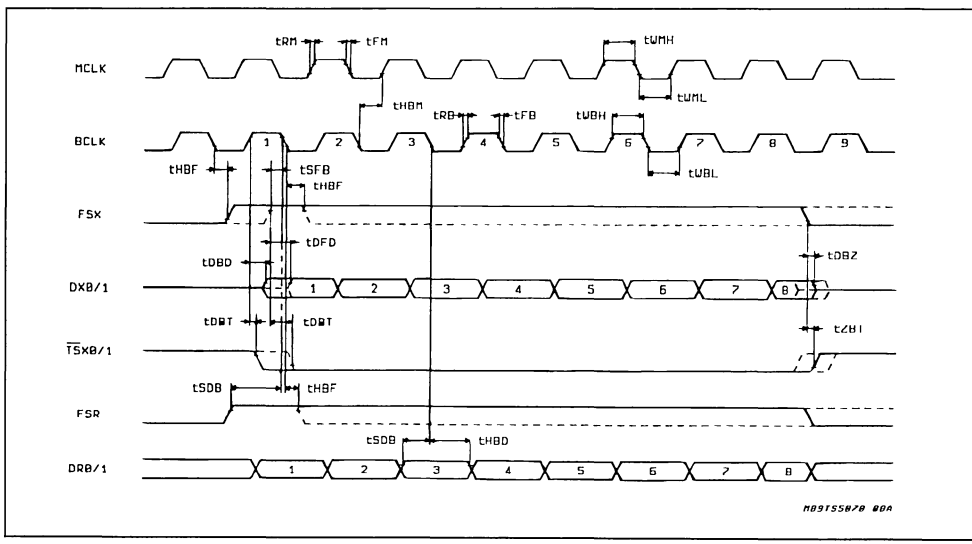
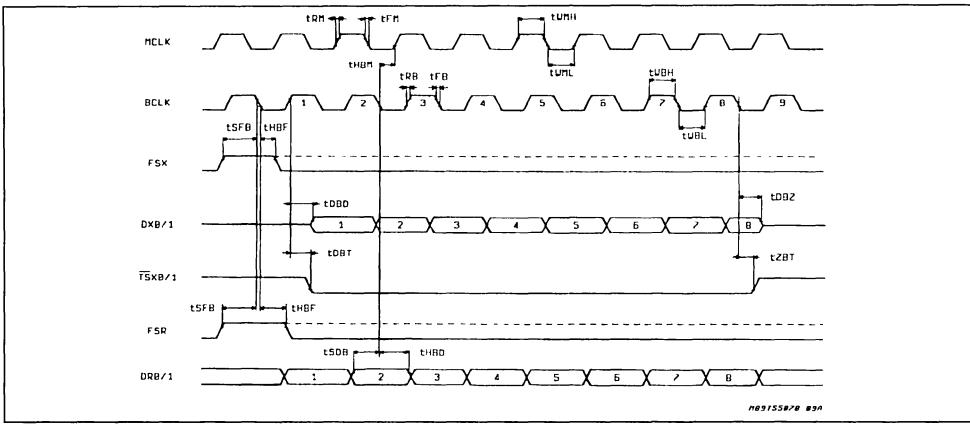


Figure 6 : Delayed Data Timing (short frame mode).



SERIAL CONTROL PORT TIMING

Symbol	Parameter	Min.	Typ.	Max.	Unit
f_{CCLK}	Frequency of CCLK			**2.048**	MHz
t_{WCH}	Period of CCLK High (measured from V_{IH} to V_{IH})	**160**			ns
t_{WCL}	Period of CCLK Low (measured from V_{IL} to V_{IL})	**160**			ns
t_{RC}	Rise Time of CCLK (measured from V_{IL} to V_{IH})			50	ns
t_{FC}	Fall Time of CCLK (measured from V_{IH} to V_{IL})			50	ns
t_{HCS}	Hold Time, CCLK Low to $\overline{CS}$ Low (CCLK1)	**10**			ns
t_{HSC}	Hold Time, CCLK Low to $\overline{CS}$ High (CCLK8)	**100**			ns
t_{SSC}	Setup Time, $\overline{CS}$ Transition to CCLK Low	**70**			ns
t_{SSCO}	Setup Time, $\overline{CS}$ Transition to CCLK High (to insure CO is not enabled for single byte)	**50**			ns
t_{SDC}	Setup Time, CI Data in to CCLK low	**50**			ns
t_{HCD}	Hold Time, CCLK Low to CI Invalid	50			ns
t_{DCD}	Delay Time, CCLK High to CO Data Out Valid (load = 100 pF plus 2 LSTTL loads)			**50**	ns
t_{DSD}	Delay Time, $\overline{CS}$ Low to $\overline{CO}$ Valid (applies only if separate $\overline{CS}$ used for byte 2)			**50**	ns
t_{DDZ}	Delay Time, $\overline{CS}$ or $\overline{CCLK9}$ High to CO High Impedance (applies to earlier of $\overline{CS}$ high or CCLK9 high)	15		80	ns

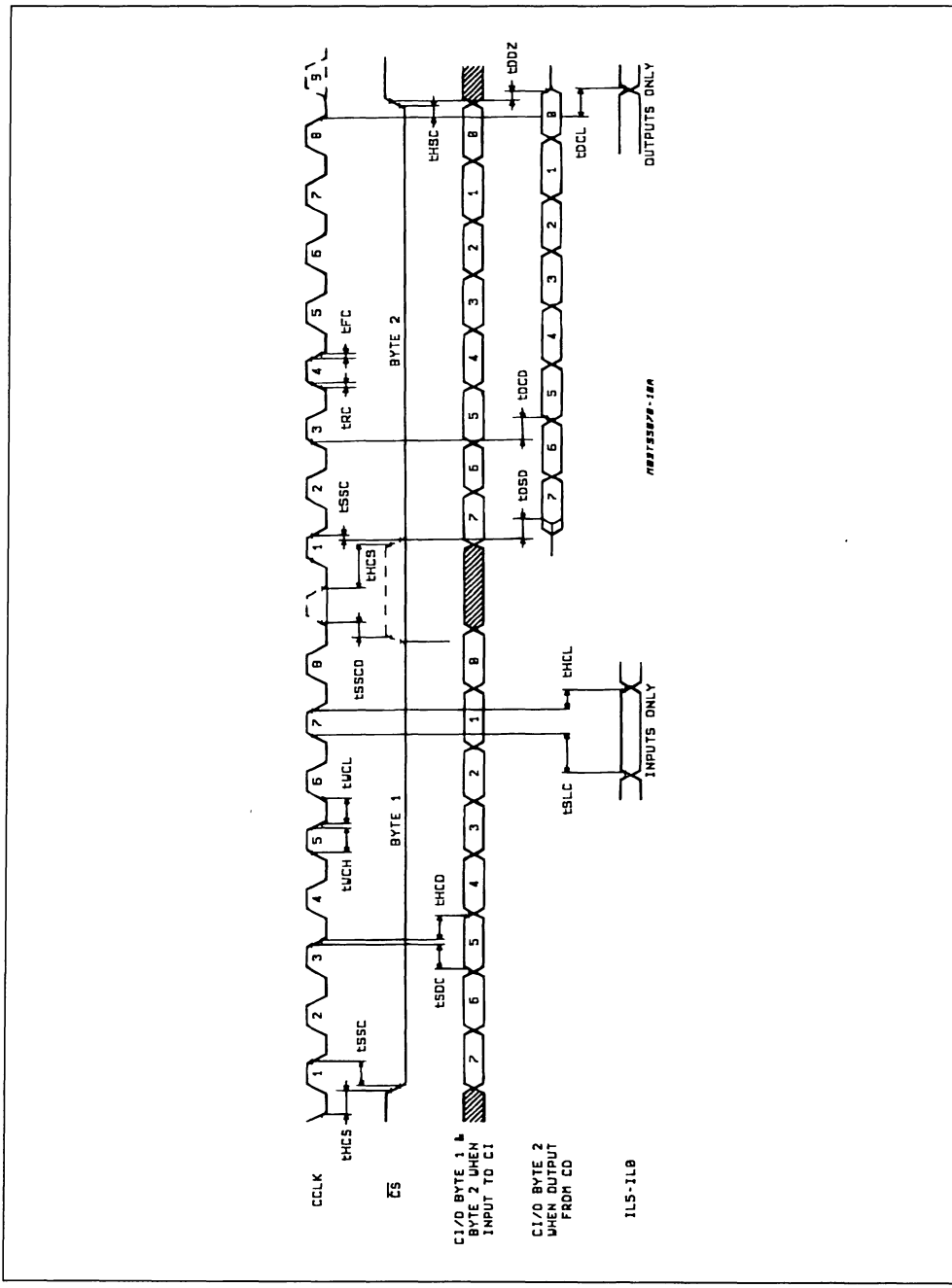
INTERFACE LATCH TIMING

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{SLC}	Setup Time, I_L Valid to CCLK 8 of Byte 1 Low. I_L as Input	**100**			ns
t_{HCL}	Hold Time, I_L Valid from CCLK 8 of Byte 1 Low. I_L as Input	50			ns
t_{DCL}	Delay Time, CCLK 8 of Byte 2 Low to I_L. C_L = 50 pF. I_L as Output			200	ns

MASTER RESET PIN

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{WMR}	Duration of Master Reset High (ST5075 only)	1			µs

Figure 7 : Control Port Timing.



TRANSMISSION CHARACTERISTICS

Unless otherwise noted, limits printed in BOLD characters are guaranteed for V_{CC} = + 5 V± 5 % ; V_{SS} = – 5 V± 5 %, T_A = 0 °C to 70 °C by correlation with 100 % electrical testing at T_A = 25 °C. f = 1015.625 Hz, VF_XI = 0 dBm0, D_R0 or D_R1 = 0 dBm0 PCM code. All other limits are assured by correlation with other production tests and/or product design and characterization. All signals referenced to GND. dBm levels are into 600 ohms. Typicals specified at V_{CC} = + 5 V, V_{SS} = 5 V, T_A = 25 °C.

AMPLITUDE RESPONSE

Symbol	Parameter	Min.	Typ.	Max.	Unit
	Absolute levels				
	The nominal 0 dBm 0 levels are :				
	VF_XI 0 dB Tx Gain		1.377		Vrms
	25.4 dB Tx Gain		74.0		mVrms
	VF_RO 0 dB Rx Attenuation (RL ≥ 15 kΩ)		1.968		Vrms
	0.5 dB Rx Attenuation (RL ≥ 600 Ω)		1.858		Vrms
	1.2 dB Rx Attenuation (RL ≥ 300 Ω)		1.714		Vrms
	25.4 dB Rx Attenuation		105.7		mVrms
	Maximum Overload				
	The nominal overload levels are :				
	A-law				
	VF_XI 0 dB Tx Gain		1.978		Vrms
	25.4 dB Tx Gain		106.2		mVrms
	VF_RO 0 dB Rx Attenuation (R_L ≥ 15 kΩ)		2.825		Vrms
	0.5 dB Rx Attenuation (R_L ≥ 300 Ω)		2.667		Vrms
	1.2 dB Rx Attenuation (R_L ≥ 300 Ω)		2.461		Vrms
	25.4 dB Rx Attenuation		151.7		mVrms
	μ-law				
	VF_XI 0 dB Tx Gain		1.985		Vrms
	25.4 dB Tx Gain		106.6		mVrms
	VF_RO 0 dB Rx Attenuation (R_L ≥ 15 kΩ)		2.836		Vrms
	0.5 dB Rx Attenuation (R_L ≥ 600 Ω)		2.677		Vrms
	1.2 dB Rx Attenuation (R_L ≥ 300 Ω)		2.470		Vrms
	25.4 dB Rx Attenuation		152.3		mVrms
	Transmit Gain Absolute Accurary				
GXA	Transmit Gain Programmed for 0 dBm0 = 5 dBm, A-Law Measure Deviation of Digital Code from Ideal 0 dBm0 PCM Code at $D_X0/1$, f = 1015.625 Hz T_A = 25 °C, V_{CC} = 5 V, V_{SS} = – 5 V	**– 0.15**		**0.15**	dB
	Transmit Gain Variation with Programmed Gain				
GXAG	– 20.4 dBm ≤ 0 dBm0 ≤ 5 dBm Calculate the Deviation from the Programmed Gain Relative to GXA i.e., GXAG = Gactual – Gprog – GXA T_A = 25 °C, V_{CC} = 5 V, V_{SS} = – 5 V	**– 0.1**		**0.1**	dB

AMPLITUDE RESPONSE (continued)

Symbol	Parameter	Min.	Typ.	Max.	Unit
GXAF	**Transmit Gain Variation with Frequency**				
	Relative to 1015.625 Hz (note 2)				
	– 20.4 dBm ≤ 0 dBm0 ≤ 5.0 dBm				
	D_R0 (or D_R1) = 0 dBm0 Code				
	f = 60 Hz			– 26	dB
	f = 200 Hz	– 1.8		– 0.1	dB
	f = 300 Hz to 3000 Hz	– 0.15		0.15	dB
	f = 3400 Hz	– 0.7		0	dB
	f = 4000 Hz			– 14	dB
	f ≥ 4600 Hz Measure Response at Alias Frequency from 0 kHz to 4 kHz			– 32	dB
	0 dBm0 = 5.0 dBm				
	VF_XI = – 4 dBm0 (note 2)				
	f = 62.5 Hz			**– 24.9**	dB
	f = 203.125 Hz	**– 1.7**		**– 0.1**	dB
	f = 2093.750 Hz	**– 0.15**		**0.15**	dB
	f = 2984.375 Hz	**– 0.15**		**0.15**	dB
	f = 3296.875 Hz	**– 0.15**		**0.15**	dB
	f = 3406.250 Hz	**– 0.7**		**0**	dB
	f = 3984.375 Hz			**– 13.5**	dB
	f = 4593.750 Hz, Measure 3406.25 Hz			**– 32**	dB
	f = 5015.625 Hz, Measure 2984.375 Hz			**– 32**	dB
	f = 10015.625 Hz, Measure 2015.625 Hz			**– 32**	dB
GXAT	**Tansmit Gain Variation with Temperature**				
	Measured Relative to G_{XA}, V_{CC} = 5 V, V_{SS} = – 5 V				
	– 20.4 dBm ≤ 0 dBm0 ≤ 5.0 dBm	– 0.1		0.1	dB
GXAV	**Transmit Gain Variation with Supply**				
	V_{CC} = 5 V ± 5 %, V_{SS} = – 5 V ± 5 %				
	Measured Relative to GXA				
	T_A = 25 °C, 0 dBm0 = 5.0 dBm	**– 0.05**		**0.05**	dB
GXAL	**Transmit Gain Variation with Signal Level**				
	Sinusoidal Test Method, Reference Level = 0 dBm0				
	VF_xI = – 40 dBm0 to + 3 dBm0	**– 0.2**		**0.2**	dB
	VF_xI = – 50 dBm0 to – 40 dBm0	**– 0.4**		**0.4**	dB
	VF_xI = – 55 dBm0 to – 50 dBm0	**– 1.2**		**1.2**	dB
GRA	**Receive Gain Absolute Accuracy**				
	0 dBm0 = 8.1 dBm, A-Law				
	Apply 0 dBm0 PCM Code to D_R0 or D_R1 Measure VF_RO	**– 0.15**		**0.15**	dB
	T_A = 25 °C, V_{CC} = 5 V, V_{SS} = – 5 V				
GRAG	**Receive Gain Variation with Programmed Gain**				
	– 17.3 dBm ≤ 0 dBm0 ≤ 8.1 dBm				
	Calculate the Deviation from the Programmed Gain Relative to GRA	**– 0.1**		**0.1**	dB

AMPLITUDE RESPONSE (continued)

Symbol	Parameter	Min.	Typ.	Max.	Unit
	i.e. GRAG = Gactual – Gprog – GRA T_A = 25 °C, V_{CC} = 5 V, V_{SS} = – 5 V				
GRAT	**Receive Gain Variation with Temperature** Measured Relative to GRA V_{CC} = 5 V, V_{SS} = – 5 V – 17.3 dBm ≤ 0 dBm0 ≤ 8.1 dBm	– 0.1		0.1	dB
GRAV	**Receive Gain Variation with Supply** Measured Relative to G_{RA} V_{CC} = 5 V ± 5 %, V_{SS} = – 5 V ± 5 % T_A = 25 °C, 0 dBm 0 = 8.1 dBm	**– 0.05**		**0.05**	dB
GRAF	**Receive Gain Variation with Frequency** Relative to 1015.625 Hz, (note 2) D_R0 or D_R1 = 0 dBm0 Code – 17.3 dBm ≤ 0 dBm0 ≤ 8.1 dBm f = 200 Hz f = 300 Hz to 3000 Hz f = 3400 Hz f = 4000 Hz GR = 0 dBm0 = 8.1 dBm GX = D_R0 = – 4 dBm0 f = 296.875 Hz f = 1906.250 Hz f = 2812.500 Hz f = 2984.375 Hz f = 3406.250 Hz f = 3984.375 Hz	 – 0.25 – 0.15 – 0.7 **– 0.15** **– 0.15** **– 0.15** **– 0.15** **– 0.7** 		 0.15 0.15 0 – 14 **0.15** **0.15** **0.15** **0.15** **0** **– 13.5**	 dB dB dB dB dB dB dB dB dB dB
GRAL	**Receive Gain Variation with Signal Level** Sinusoidal Test Method Reference Level = 0 dBm0 D_R0 = – 40 dBm0 to + 3 dBm0 D_R0 = – 50 dBm0 to – 40 dBm0 D_R0 = – 55 dBm0 to – 50 dBm0	 **– 0.2** **– 0.4** **– 1.2**		 **0.2** **0.4** **1.2**	 dB dB dB

ENVELOPPE DELAY DISTORTION WITH FREQUENCY

Symbol	Parameter	Min.	Typ.	Max.	Unit
DXA	**Tx Delay Absolute**			315	µs
	f = 1600 Hz				
DXR	**Tx Delay, Relative**				
	f = 500 – 600 Hz			220	µs
	f = 600 – 800 Hz			145	µs
	f = 800 – 1000 Hz			75	µs
	f = 1000 – 1600 Hz			40	µs
	f = 1600 – 2600 Hz			75	µs
	f = 2600 – 2800 Hz			105	µs
	f = 2800 – 3000 Hz			155	µs
DRA	**Rx Delay, Absolute**				
	f = 1600 Hz			200	µs
DRR	**Rx Delay, Relative**				
	f = 500 – 1000 Hz	– 40			µs
	f = 1000 – 1600 Hz	– 30			µs
	f = 1600 – 2600 Hz			90	µs
	f = 2600 – 2800 Hz			125	µs
	f = 2800 – 3000 Hz			175	µs

NOISE

Symbol	Parameter	Min.	Typ.	Max.	Unit
NXC	**Transmit Noise, C Message Weighted** μ-law Selected (note 3) 0 dBm0 = 5.0 dBm		12	**15**	dBrnC0
NXP	**Transmit Noise, Psophometric Weighted** A-law Selected (note 3) 0 dBm0 = 5.0 dBm		– 74	**– 67**	dBm0p
NRC	**Receive Noise, Psophometric Weighted** μ-law Selected PCM code is alternating positive		8	**11**	dBrnC0
NRP	**Receive Noise, Psophometric Weighted** A-law Selected PCM Code Equals Positive Zero		– 82	**– 79**	dBm0p
NRS	**Noise, Single Frequency** f = 0 kHz to 100 kHz, Loop Around Measurement VF_XI = 0 Vrms			– 53	dBm0
PPSRX	**Positive Power Supply Rejection Transmit** V_{CC} = 5 V_{DC} + 100 mVrms f = kHz – 50 kHz (note 4)	**30**			dBp
NPSRX	**Negative Power Supply Rejection Transmit** V_{SS} = – 5 VDC + 100 mVrms	**30**			dBp
PPSRR	**Positive Power Supply Rejection Receive** PCM Code Equals Positive Zero V_{CC} = 5 V_{DC} + 100 mVrms Measure VF_R0 f = 0 Hz – 4000 Hz f = 4 kHz – 25 kHz f = 25 kHz – 50 kHz	 **30** 40 36			 dBp dB dB
NPSRR	**Negative Power Supply Rejection Receive** PCM Code Equals Positive Zero V_{SS} = – 5 V_{DC} + 100 mVrms Measure VF_RO f = 0 Hz – 4000 Hz f = 4 kHz – 25 kHz f = 25 kHz – 50 kHz	 **30** 40 36			 dBp dB dB
SOS	**Spurious Out-of Band Signals at the Channel Output** 0 dBm0 300 Hz to 3400Hz input PCM applied at D_R0 (D_R1) 4600 Hz – 7600 Hz 7600 Hz – 8400 Hz 8400 Hz – 100 000 Hz			 **– 30** – 40 **– 30**	 dB dB dB

DISTORTION

Symbol	Parameter	Min.	Typ.	Max.	Unit
STDX	**Signal to Total Distortion Transmit** Sinusoidal Test Method Half Channel, Level = 3 dBm0 – 30 dBm0 to 0 dBm0 – 40 dBm0 – 45 dBm0	 **33** **36** **29** **25**			 dBp dBp dBp dBp
STDR	**Signal to Total Distortion Receive** Sinusoidal Test Method Half Channel, Level = 3 dBm0 – 30 dBm0 to 0 dBm0 – 40 dBm0 – 45 dBm0	 **33** **36** **30** **25**			 dBp dBp dBp dBp
SFDX	Single Frequency Distortion Transmit			**– 46**	dB
SFDR	Single Frequency Distortion Receive			**– 46**	dB
IMD	Intermodulation Distortion Transmit or Receive Two Frequencies in the Range 300 Hz – 3400 Hz			**– 41**	dB

CROSSTALK

Symbol	Parameter	Min.	Typ.	Max.	Unit
CTX-R	Transmit to Receive Crosstalk, 0 dBm0 Transmit Level f = 300 – 3400 Hz DR = Steady PCM Code		– 90	**– 75**	dB
CTR-X	Receive to transmit Crosstalk, 0 dBm0 Receive Level f = 300 – 3400 Hz, (note 4)		– 90	**– 70**	dB

Notes : 1. Applies only to MCLK frequencies ≥ 1.536 MHz. At 512 kHz A 50:50 ± 2 % duty cycle must be used.
2. A multi-tone test technique is used (peak/rms ≤ 9.5 dB).
3. Measured by extrapolation from distortion test result at – 50 dBm0.
4. PPSRX, NPSRX and CTR-X are measured with a – 50 dBm0 activation signal applied to VFxI.
A signal is Valid if it is above V_{IH} or below V_{IL} and invalid if it is between V_{IL} and V_{IH}. For the purpose of the specification the following conditions apply :
a) All input signals are defined as V_{IL} = 0.4 V, V_{IH} = 2.7 V, t_R < 10 ns, t_F 10 ns
b) t_R is measured from V_{IL} to V_{IH}, t_F is measured from V_{IH} to V_{IL}
c) Delay Times are measured from the input signal Valid to the clock input invalid
d) Setup Times are measured from the data input Valid to the clock input invalid
e) Hold Times are measured from the data signal Valid to the data input invalid
f) Pulse widths are measured drom V_{IL} to V_{IL} or from V_{IH} to V_{IH}

DEFINITIONS AND TIMING CONVENTIONS

DEFINITIONS

V_{IH}	V_{IH} in the D.C input level above which an input level is guaranteed to appear as a logical one. This parameter is to be measured by performing a functional test at reduced clock speeds and nominal timing. (i.e. not minimum setup and hold times or output strobes), with the high level of all driving signals set to V_{IH} and maximum supply voltages applied to the device.
V_{IL}	V_{IL} is the D.C. input level below which an input level is guaranteed to appear as a logical zero the device. This parameter is measured in the same manner as V_{IH} but with all driving signal low levels set to V_{IL} and minimum supply voltage applied to the device.
V_{OH}	V_{OH} is the minimum D.C. output level to which an output placed in a logical one state will converge when loaded at the maximum specified load current.
V_{OL}	V_{OL} is the maximum D.C. output level to which an output placed in a logical zero state will converge when loaded at the maximum specified load current.
Threshold Region	The threshold region is the range of input voltages between V_{IL} and V_{IH}.
Valid Signal	A signal is Valid if it is in one of the valid logic states. (i.e. above V_{IH} or belowe V_{IL}). In timing specifications, a signal is deemed valid at the instant it enters a valid state.
Invalid signal	A signal is invalid if it is not in a valid logic state, i.e., when it is in the threshold region between V_{IL} and V_{IH}. In timing specifications, a signal is deemed Invalid at the instant it enters the threshold region.

TIMING CONVENTIONS

For the purpose of this timing specifications the following conventions apply :

Input Signals	All input signals may be characterized as : $V_L = 0.4$ V, $V_H = 2.4$ V, tR < 10 ns, tF < 10 ns.
Period	The period of the clock signal is designated as tPxx where xx represents the mnemonic of the clock signal being specified.
Rise Time	Rise times are designated as tRyy, where yy represents a mnemonic of the signal whose rise time is being specified, tRyy is measured from V_{IL} to V_{IH}.
Fall Time	Fall times are designated as tFyy, where yy represents a mnemonic of the signal whose fall time is being specified, tFyy is measured from V_{IH} to V_{IL}.
Pulse Width High	The high pulse width is designated as tWzzH, where zz represents the mnemonic of the input or output signal whose pulse width is being specified. High pulse widths are measured from V_{IH} to V_{IH}.
Pulse Width Low	The low pulse width is designated as tWzzL' where zz represents the mnemonic of the input or output signal whose pulse width is being specified. Low pulse widths are measured from V_{IL} to V_{IL}.
Setup Time	Setup times are designated as tSwwxx where ww represents the mnemonic of the input signal whose setup time is being specified relative to a clock or strobe input represented by mnemonic xx. Setup times are measured from the ww Valid to xx Invalid.
Hold Time	Hold times are designated as THwwxx where ww represents the mnemonic of the input signal whose hold time is being specified relative to a clock or strobe input represented by the mnemonic xx. Hold times are measured from xx Valid to ww Invalid.
Delay Time	Delay times are designated as TDxxyy [H/L], where xx represents the mnemonic of the input reference signal and yy represents the mnemonic of the output signal whose timing is being specified relative to xx. The mnemonic may optionally be terminated by an H or L to specify the high going or low going transition of the output signal. Maximum delay times are measured from xx Valid to yy Valid. Minimum delay times are measured from xx Valid to yy Invalid. This parameter is tested under the load conditions specified in the Conditions column of the Timing Specifications section of this datasheet.

SUBSCRIBER LINE INTERFACE CIRCUIT KIT

ADVANCE DATA

MAIN CHARACTERISTICS

- PROGRAMMABLE DC FEEDING RESISTANCE AND LIMITING CURRENT (four values available)
- THREE OPERATING MODES :
- STAND-BY, CONVERSATION, RINGING
  - 1. NORMAL/BOOST BATTERY : DIRECT/ REVERSE POLARITY
  - 2. QUICK OFF-HOOK DETECTION IN CVS (1ms) FOR LOW DISTORTION DIAL PULSE DETECTION
  - 3. GROUND KEY DETECTION
- TELETAXE SIGNAL INJECTION WITH INTERNAL FILTER
- HYBRID FUNCTION
- RINGING GENERATION WITH QUASI ZERO OUTPUT IMPEDANCE, ZERO CROSSING INJECTION (no ext. relay needed) AND RING TRIP DETECTION
- AUTOMATIC RINGING STOP WHEN OFF-HOOK IS DETECTED
- SERIAL DIGITAL INTERFACE SLD BUS COMPATIBLE
- LOW NUMBER OF EXTERNAL COMPONENTS
- POSSIBILITY TO WORK ALSO WITH HIGH COMMON MODE CURRENTS
- INTEGRATED THERMAL PROTECTION
- GOOD REJECTION OF THE NOISE ON BATTERY VOLTAGE (20dB at 10Hz ; 40dB at 1kHz)

DESCRIPTION

The SLIC KIT (L3000/L3010) is a set of solid state devices designed to integrate many of the functions needed to interface a telephone line. It consists of 2 integrated devices ; the L3000 line interface circuit and the L3010 control unit

The kit implements the main features of the BORSHT functions :

- Battery feed (balance mode)
- Ringing
- Signalling
- Hybrid

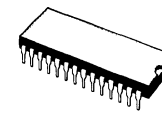
The SLIC KIT injects the ringing signal in balanced mode and requires a positive supply voltage of typically + 72V to be available on the subscriber card.

The L3000/L3010 KIT generates the ringing signal internally, avoiding the requirement for expensive external circuitry. A low level 1Vrms input is required.

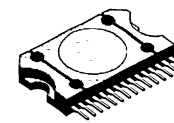
This kit is fabricated using a 140V Bipolar technology for L3000 and a 12V Bipolar I2L technology for L3010.

This kit is suitable for all the following applications :

C.O. (Central Office), DLC (Digital Loop Carrier) and high range PABX (Private Automatic Branch Exchange).



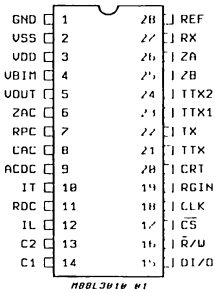
DIP28

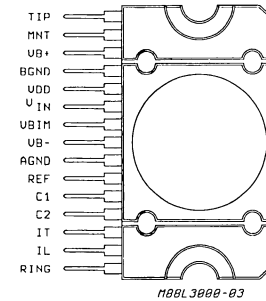


FLEXIWATT15

ORDER CODES :
L3010 (Dip28)
L3000 (Flexiwatt15)

PIN CONNECTION





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ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_b-	Negative Battery Voltage	– 80	V
V_b+	Positive Battery Voltage	80	V
$\|V_b- \|+\| V_b+\|$	Total Battery Voltage	140	V
V_{dd}	Positive Supply Voltage	+ 5.5	V
V_{ss}	Negative Supply Voltage	– 5.5	V
$V_{agnd}-V_{bgnd}$	Max Voltage between Analog Ground and Battery Ground	5	V
T_j	Max Junction Temperature	+ 150	°C
T_{stg}	Storage Temperature	– 55 to + 150	°C

THERMAL DATA

L3000 HIGH VOLTAGE

R_{thjc}	Max Resistance Junction to Case	4	°C/W
R_{thja}	Max Resistance Junction to Ambient	50	°C/W

L3010 LOW VOLTAGE

R_{thja}	Max Resistance Junction to Ambient	80	°C/W

OPERATING RANGE

Symbol	Parameter	Min.	Typ.	Max.	Unit
T_{oper}	Operating Temperature Range	0		70	°C
V_b-	Negative Battery Voltage	– 70	– 48	– 24	V
V_b+	Positive Battery Voltage	0	+ 72	+ 75	V
$\|V_b- \|+\| V_b+\|$	Total Battery Voltage		120	130	V
V_{dd}	Positive Supply Voltage	+ 4.5		+ 5.5	V
V_{ss}	Negative Supply Voltage	– 5.5		– 4.5	V
I_{max}	Total Line Current ($I_L + I_T$)			85	mA

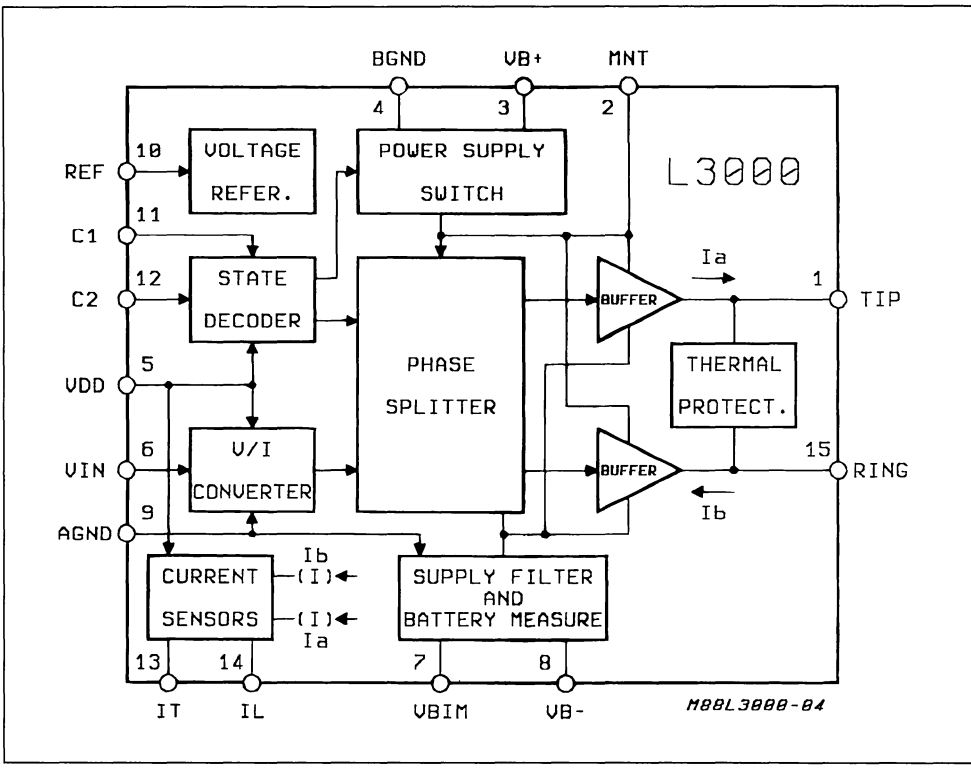
PIN DESCRIPTION (L3000)

N°	Name	Description
1	TIP	A line termination output with current capability up to 100mA (I_a is the current sourced from this pin).
2	MNT	Positive Supply Voltage Monitor
3	V_B+	Positive Battery Supply Voltage
4	BGND	Battery ground relative to the V_B+ and the V_B- supply voltages. It is also the reference ground for TIP and RING signals.
5	V_{DD}	Positive Power Supply + 5V
6	VIN	2 wire unbalanced voltage input.
7	VBIM	Output voltage without current capability, with the following functions : - give an image of the total battery voltage scaled by 40 to the low voltage part. - fliter by an external capacitor the noise on V_B-.
8	V_B-	Negative Battery Supply Voltage
9	AGND	Analog Ground. All input signals and the V_{DD} supply voltage must be referred to this pin.
10	REF	Voltage reference output with very low temperature coefficient. The connected resistor sets internal circuit bias current.
11	C1	Digital signal input (3 levels) that defines device status with pin 12.
12	C2	Digital signal input (3 levels) that defines device status with pin 11.
13	I_T	High precision scaled transversal line current signal. $I_T = \frac{I_a + I_b}{100}$
14	IL	Scaled longitudinal line current signal. $IL = \frac{I_a - I_b}{100}$
15	RING	B line termination output with current capability up to 100mA (I_b is the current sunk into this pin).

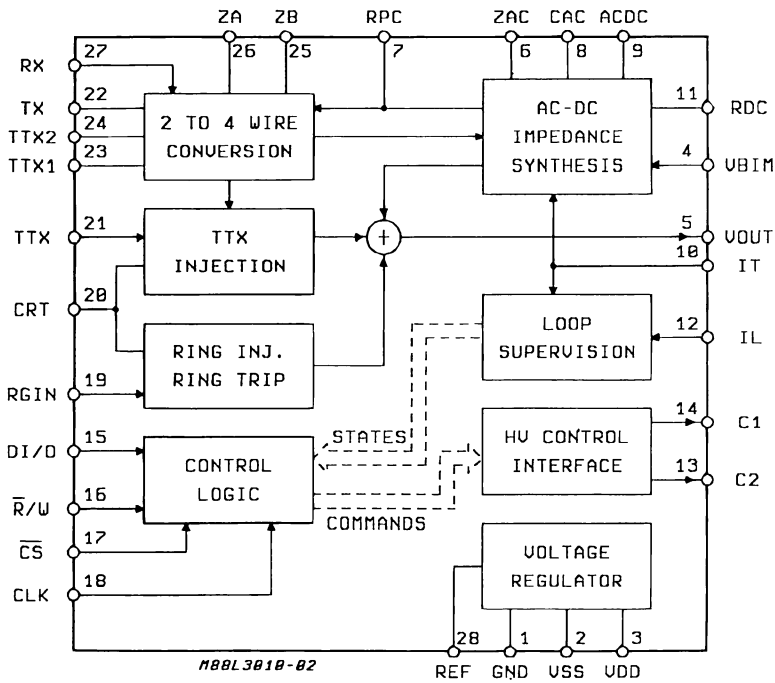
PIN DESCRIPTION (L3010)

N°	Name	Description
1	GND	Analog and Digital Ground
2	VSS	Negative Supply Voltage, – 5V
3	VDD	Positive Supply Voltage, + 5V
4	V_{BIM}	Battery voltage scaled by 40 input ; from L3000, pin 7.
5	VOUT	Two wire unbalanced output carrying out the following signals reduced by 40 : 1) DC voltage to perform the proper DC characteristic. 2) Ringing Signal 3) Voice Signal 4) Teletax Signal
6	ZAC	AC Line Impedance Synthesis
7	RPC	AC Line Impedance Adjustment. Protection Resistances Compensation
8	CAC	AC Feedback Input
9	ACDC	AC - DC Feedback Input
10	IT	Transversal Line Current Input $IT = \frac{I_a + I_b}{100}$
11	RDC	DC Feeding System
12	IL	Longitudinal Line Current Input $IL = \frac{I_a - I_b}{100}$
13	C2	State Control Signal 2
14	C1	State Control Signal 1. Combination of C1 and C2 define operating mode of the high voltage part.
15	DI/O	data Input/output of the Serial Digital Interface
16	$\overline{R}/W$	Read/write Input of the Serial Digital Interface
17	$\overline{CS}$	Chip Select Input
18	CLK	Clock Input of the Serial Digital Interface
19	RGIN	Low Level Ringing Signal Input
20	CRT	Ring Trip Detection and TTX Shoping
21	TTX	Teletaxe Signal Analog Input
22	TX	Transmit Amplifier Output
23	TTX1	Teletaxe Filter
24	TTX2	Teletaxe Filter
25	ZB	Two to four wire conversion Circuit Inputs
26	ZA	Two to four wire conversion Circuit Inputs
27	RX	Receiving Input
28	REF	Bias Setting Pin

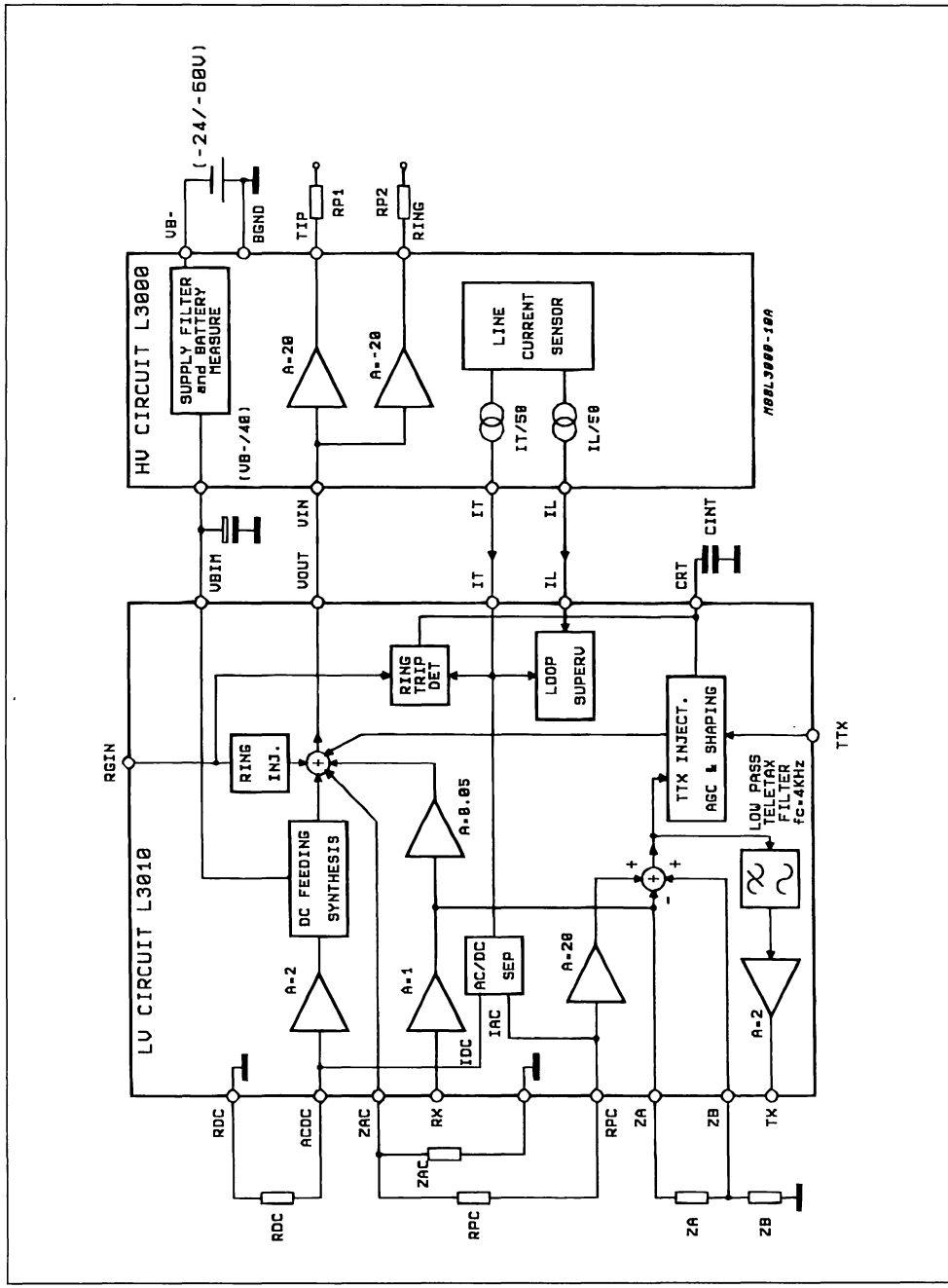
L3000 BLOCK DIAGRAM



L3010 BLOCK DIAGRAM



L3000-L3010 FUNCTIONAL DIAGRAM



FUNCTIONAL DESCRIPTION

L3000 - HIGH VOLTAGE CIRCUIT

The L3000 line interface provides a battery feeding for telephone lines and ringing injection. The IC contains a state decoder that under external control can force the following operational modes : stand-by, conversation and ringing.

In addition Power down mode can be forced connecting the bias current resistor to VDD by an external transistor.

Two pins, I_L and I_T, carry out the information concerning line status which is detected by sensing the line current into the output stage.

The L3000 amplifies both the AC and DC signals entering at pin 6 (VIN).

Separate grounds are provided :

- Analog ground as a reference for analog signals
- Battery ground as a reference for the output stages

The L3000 can work with a (DC + AC) voltage signal up to 5V between the two grounds.

L3010 - LOW VOLTAGE CIRCUIT

The L3010 Low Voltage Control Unit controls the L3000 line interface module, giving the proper informations to set line feed characteristic, to inject the ringing and the teletaxe signals and synthesizes the line and the balance impedances.

An on-chip digital serial interface allows the L3010 to be directly connected to a SLD Bus Interface or to a microprocessor to control all the operations.

L3010 defines working states of line interface and also informs the controller about line status.

WORKING STATES OF THE KIT

In order to carry out the different possible operations, the ST SLIC kit has several different working states. Each state is defined by the voltage respectively applied by pins 14 and 13 of L3010 to the pins 11 and 12 of L3000.

Three different voltage levels (– 5, 0, + 5) are available at each connection, so defining nine possible states as listed in tab. 1.

Table 1.

		Pin 13 of L3010 / Pin 12 of L3000		
		+ 5	0	– 5
Pin 14 of L3010	+ 5	Stand-by	Conversation NB-DP	Conversation NB-RP
	0	Not Used	Conversation BB-DP	Conversation BB-RP
Pin 11 of L3000	– 5	Not Used	Ringing DP	Ringing RP

NB . Normal Battery
BB : Boosted Battery
NP · Normal Polarity
RP · Reverse Polarity

Appropriate combinations of two pins define the three status of the kit, that are :

a) Stand-by (SBY)

b) Conversation (CVS)

c) Ringing (RING)

A fourth status Power down (PD) can be set disconnecting the bias resistor (RH) from pin 10 of L3000 through an external transistor.

The main difference between Stand-by and Power down is that in SBY the power consumption on the voltage battery VB– (– 48V) is reduced but the SLIC can recognize yet the On hook/off hook status. In PD the power consumption on VB- is reduced to zero, but none operation can be performed by the SLIC.

The SBY status should be used when the telephone is in on hook and PD status only in emergency condition when it is mandatory to cut any possible dissipation but no operation are requested.

OPERATING MODES

STAND-BY (SBY) MODE

In this mode the bias currents of both L3000 and L3010 are reduced as only some parts of the two circuits are completely active, control interface and current sensors among them.

The Line Feeding DC Characteristics has two region :

a) Current limiting region with a DC impedance very high (> 20KΩ). The value of the limiting line current is fixed at 10mA.

b) A low resistive region where the equation for the line voltage is equal to

$$V_{LINE} = (|VBAT| - 10) - I_{LINE} * \frac{2}{3} (R_{FS} + 2R_P)$$

The AC characteristic in Stand-by corresponds to a low impedance (2xRP).

In Stand-by mode the Line Voltage Polarity is just in direct condition, that is the TIP wire more positive than the RING one.

The ON/OFF HOOK detection circuit is active and provide at the digital interface the ON-HOOK indication when the Transversal lime current is lower than 6mA and the OFF-HOOK indication when it is higher than 7.5mA.

When the ST SLIC is in Stand-by mode, the power dissipation of L3000 does not exceed 200mW (from – 48V) eventually increased of a certain amount if some current is flowing into the line.

The power dissipation of the L3010 in the same condition is typically 120mW.

CONVERSATION (CVS) MODE

In conversation Mode it is possible to select between two different DC characteristics (Normal and Boost battery) and the polarity of the DC Line Voltage.

As far as the DC characteristic in Normal Battery is concerned three different feeding conditions are present :

a) Current limiting region : the DC impedance of the SLIC is very high (> 20KΩ) and therefore the system works like a current generator. The limiting current value is defined by programmation via the serial digital interface and selected among the four following values : 30/45/60/70mA.

b) A resistive feeding region : the characteristic $V_{LINE} = F(I_{LINE})$ is :

$V_{LINE} = 46V - 2RFS * I_{LINE}$. This part of the DC characteristic does not depend of the Battery Voltage value.

c) A low resistive Feeding region : the Line Voltage is equal to :

$$V_{LINE} = (|VBAT| - 10) - I_{LINE} * \frac{2}{3} (R_{FS} + 2R_P)$$

Switching between the three regions is automatic without discontinuity, and depends on the loop resistance.

Figure 1 : DC Characteristics in Stand-by Mode.

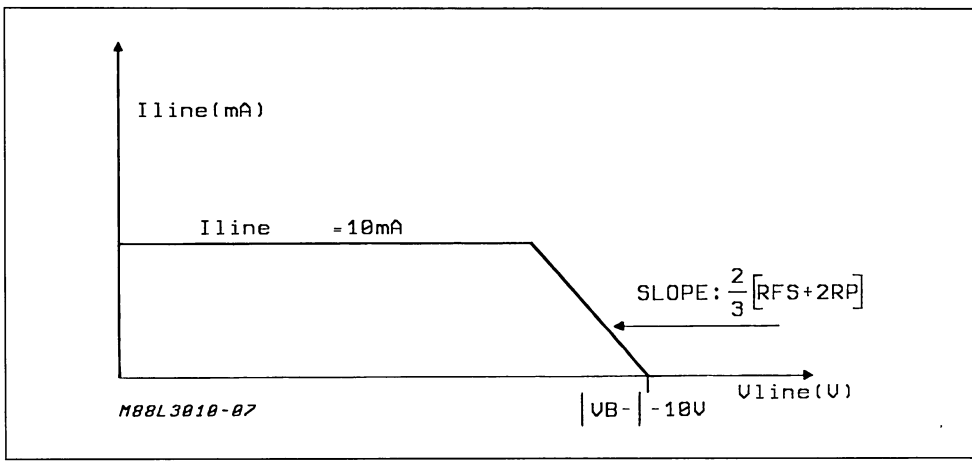


Figure 2 : DC Characteristic in Conversation Mode - R_{FS} = 200Ω ; R_P = 30Ω ; VB– = –48V.

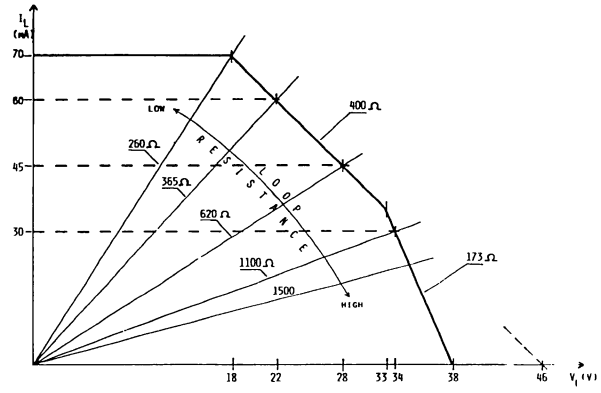
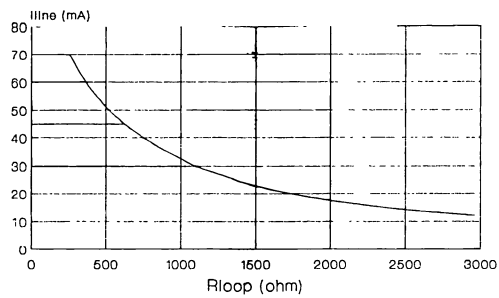


Figure 3 : Line Current versus Loop Resistance - R_{FS} = 200Ω ; R_P = 30Ω ; VB– = –48V.



In Boost Battery the DC characteristic has two Feeding conditions :

a) current limiting region : it has the same characteristics as in Normal Battery

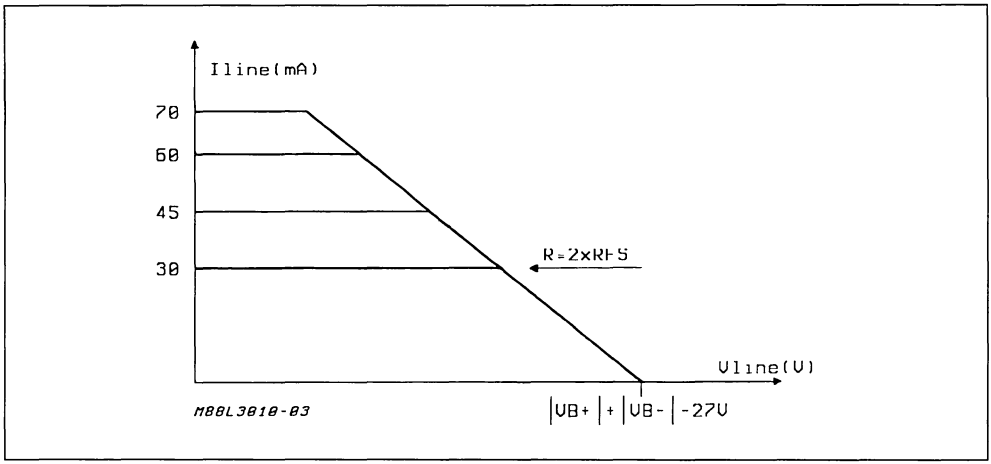
b) resistive Feeding region : the Line Voltage is

$V_{LINE} = (|V_{B-}| + |V_{B+}| - 27V) - I_{LINE} \times 2 \times R_{FS}$

In conversation mode, whatever the condition (normal or boost battery, direct or reverse polarity), it is always possible to inject into the line the 12Khz (or 16Khz) signal with a level of 1Vrms, permanently applied at the L3010's pin 21, as metering pulses, when request by the control processor (through BIT3 set to "1"). A patented automatic control system adjusts the level of the metering signal to contain 2Vrms across the line, regardless of impedance. Moreover the metering signal is ramped at the beginning and at the end of each pulse to prevent undesirable clicking noise : the slope is determined by the value of CINT (see the external component list of L3010).

The metering pulse signals and the AC transmitting and receiving signals can be injected or received from the line also with a DC Line current equal to zero. This allows the ON-HOOK Transmission Function.

Figure 4 : DC Characteristic in Boost Battery Mode.



In conversation mode the AC impedance at the line terminals is synthesized by the external components ZAC and RP, according to the following formula :

$$ZML = \frac{4}{5} Z_{AC} + 2 \times RP$$

Depending on the characteristic of the ZAC network, ZML can be either a pure resistance or a complex impedance. This allows the SLIC to meet different standards as far as the return loss is concerned. The capacitor CCOMP guarantees stability to the system.

The two to four wire conversion is achieved by means of a circuit that can be represented as a Wheatstone bridge the branches of which being :

1) The line impedance (Zline),

2) The SLIC impedance at line terminals (ZML),

3) The balancing network ZA connected between the pin 25 (ZB) and the pin 26 (ZA) of L3010,

4) The network ZB between the pin 25 (ZB) and ground that shall copy the line impedance.

It is important to underline that ZA and ZB are not equal to ZML and to Zline. They both must be multiplied by a factor in the range up to 10, allowing use of smaller capacitors.

In conversation mode, the L3000 dissipates about 500mW for its own operation. The dissipation related to the current supplied to the line shall be added, in order to get the total dissipation. In the same condition the power dissipation of L3010 is typically 200mW.

RINGING MODE

When the ringing function is selected by the control processor a low level signal (1Vrms) with a frequency in the range from 16 to 70Hz, permanently applied to the L3010 (pin RGIN), is amplified and injected in balanced mode into the line through the L3000 with a super imposed DC voltage of 22V.

It is important to underline that the low level ringing signal must be always connected to the pin RGIN also when the SLIC is not in Ringing Mode.

The first and the last ringing cycles are synchronized by the L3010 so that the ringing signal always starts and stops when the line voltage crosses zero.

When this mode is activated, the L3000 operates between the negative and the positive battery voltages, typically - 48V and + 72V, and the impedance to the line is just equal to the two external resistors (typ. = 60 ohm).

There is a sophisticated ring trip detection circuit insensitive to the parasitic noise on the line. The ring trip principle is as follows :

- 1 - During the ringing signal injection at the beginning of each period the voltage across the external capacitor CINT connected between ground and pin 20 (CRT) of L3010 is reset to 0V.
- 2 - The transversal Line Current is sensed, therefore the ring trip detection is not sensitive to the longitudinal current.
- 3 - A fraction of the line current is sent to the ext. capacitor CINT.
- 4 - At the end of each period the voltage across CINT is measured. If it is under a certain value (250mV) the procedure restart as at point - 1 -. If the voltage is higher of 250mV the ringing signal is automatically suspended for three periods and the SLIC is programmed in Conversation Mode.
- 5 - At the end of the third period the On Hook/Off Hook detection circuit checks the line status.
- 6 - If the Off-hook condition is confirmed it sets the BIT 0 (HS Hook Status) of the internal reading register.
- 7 - If the Off-Hook condition is not confirmed the SLIC automatically will come back in Ringing Mode and the ringing signal will be re-injected into the line.

In order to performs the Off-Hook detection in one period the value of the capacitor CINT must be choosen in function of the ringing frequency.

(see external component list table).

DIGITAL CONTROL INTERFACE BETWEEN THE SLIC AND THE BOARD CONTROLLER

The programmable functions of the SLIC are controlled by a microprocessor or a Board Controller through a 4-Wire serial bus SLD compatible.

The four pins have following functions :

CLK : Shift Clock (512kHz max)

$\overline{CS}$: Chip select (active low)

DI/O : Bidirectional pin : data-in (8 bit), data-out (4-bit)

$\overline{R}/W$: $\overline{R}/W = 0$ read operation ; $\overline{R}/W = 1$ writing operation.

The data are shifted into and read by the low voltage L3010- on the falling edge of each CLK pulse, if $\overline{CS} = 0$ and $\overline{R}/W = 1$.

The data are shifted out from L3010 on the rising edge of each CLK pulse, if $\overline{CS} = 0$ and $\overline{R}/W = 0$.

DATA INPUT

One byte can be written into the SLIC to program its functions.

The following table shows the meaning of each bit.

Table 1.

Input Data				
Meaning	**Value**			
BIT 0 = Activation	0 : stand-by			
	1 : power up			
BIT 1 = Battery Polarity	0 : normal Pol. (tip to ground)			
	1 : reverse Pol. (ring to ground)			
BIT 2 = Ringing	0 : ring off			
	1 : ring on			
BIT 3 = Teletaxe	0 : teletaxe off			
	1 : teletaxe on			
BIT 4 = Extra Feeding	0 : normal battery			
	1 : boost battery			
BIT 5	0	0	1	1
BIT 6	0	1	0	1
Line Current Limiting	30mA	45mA	60mA	70mA
BIT 7 = Parity Control	0 : $\sum_{0\text{-}6}$ bit = ODD			
	1 : $\sum_{0\text{-}6}$ bit = EVEN			

Notes : 1. The BIT0 is the first bit to be sent to the L3010 and the BIT7 is the last.
2. In Conversation Mode and in Ringing Mode the BIT0 must be set to "1".
3. BIT7 is the parity control bit. It must be set to 0 if the number of ones into the previous bits from BIT0 to BIT6 is odd.

DATA OUTPUT

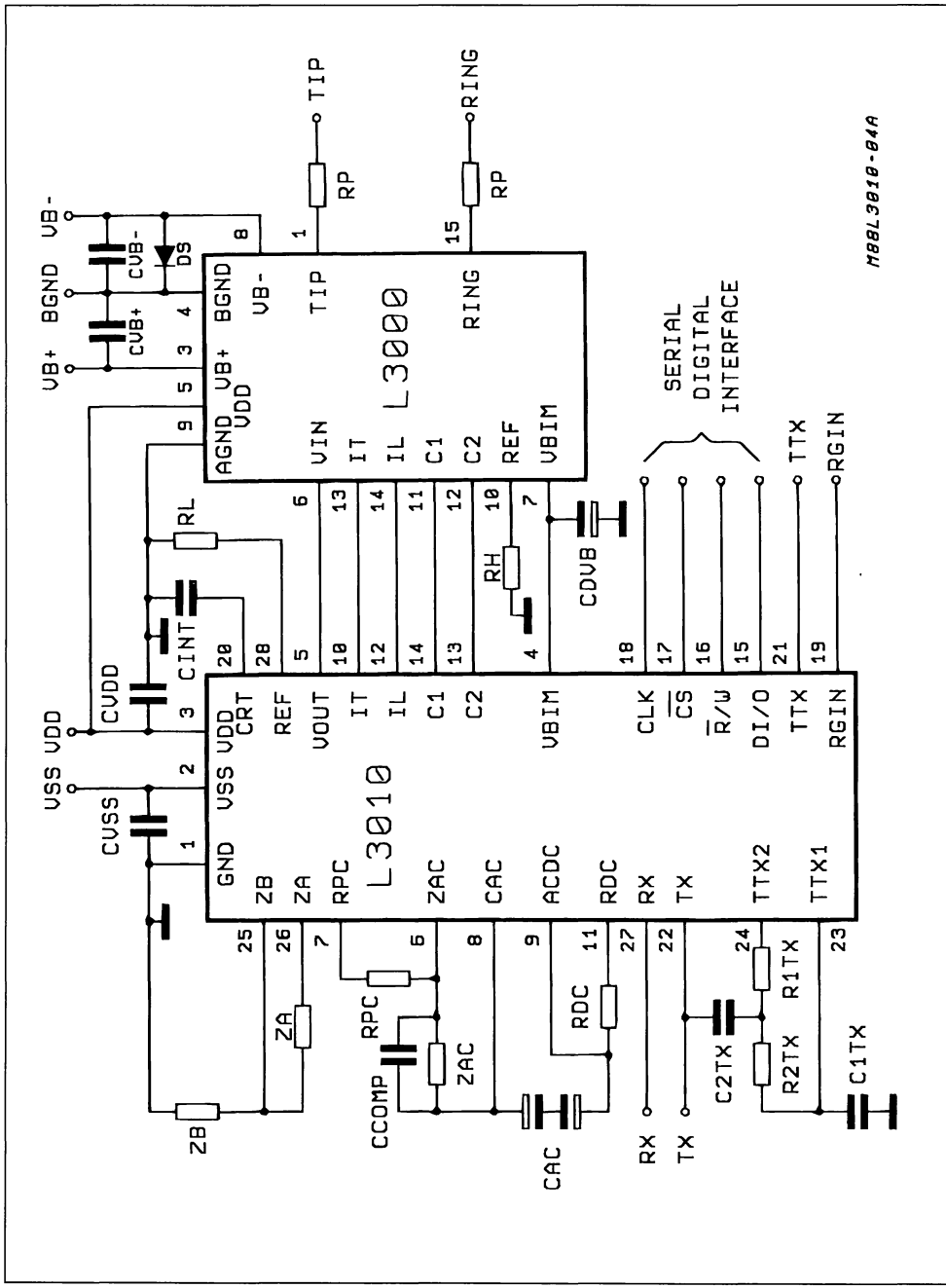
Four bits can be read from the SLIC as shown in the following table 2.

Table 2.

Input Data	
Meaning	**Value**
BIT 0 = Line Supervision (note 1)	0 : on-hook
	1 : off-hook
BIT 1 = Line Current > 60mA (note 2)	0 : off
	1 : on
BIT 2 = Ground Key Detection (note 3-4)	0 : long. Line Curr. < Iline/2.5
	1 : long. Line Curr. > Iline/2
BIT 3 = Previous Word	0 : not accepted
	1 : accepted

Notes : 1. The BIT0 is the first that L3010 send in the output
2. If the line current exceeds 60mA. BIT1 = 1
3. This relation is valid for line current over 5mA
4. The longitudinal current is defined as follows $I_{GDK} = (I_A - I_B)/2$
where I_A is the current sourced from the TIP pin and I_B is the current sunk into the RING pin

Figure 5 : Typical Application Circuit.



EXTERNAL COMPONENTS LIST

To set up the SLIC kit into operation, the following parameters have to be defined :

- The DC feeding resistance RFS, defined as the resistance of each side of the traditional feeding system (most common value for RFS are 200, 400 or 500 ohms).
- The AC input/output SLIC impedance at line terminals, ZML, to which the return loss measurement is refered. It can be real (typically 600 ohms) or complex.
- The equivalent AC impedance of the line Zline used for evaluation of the trans-hybrid loss (2/4 wire conversation). It is usually a complex impedance.
- The frequency of the ringing signal Fr (SLIC can work with this frequency ranging from 16 to 68Hz).
- The metering pulse frequency F_t (two values are possible : 12kHz and 16kHz.
- The value of the two resistors RP in series with the line terminals ; main purpose of the a.m. resistors is to allow primary protection to fire. A minimum value of 30 ohm for each side is suggested.

With these assumptions, the following component list is defined :

EXTERNAL COMPONENT LIST FOR THE L3000

Component		Involved Parameter or Function
Ref	Value	
RH	24.9KΩ ± 2%	Bias Resistor
RP	30 to 100Ω	Line Series Resistor
CDVB	47µF – 20WV ± 20%	Battery Voltage Rejection
CVB + (note 1)	0.1µF – 100WV ± 20%	Positive Battery Filter
CVB – (note 1)	0.1µF – 100WV ± 20%	Negative Battery Filter
DS (note 1)	BAT 49	Protective Shottky Diode

EXTERNAL COMPONENT LIST FOR THE L3010

Component		Involved Parameter or Function
Ref	Value	
CVSS	0.1µF – 15WV (note 1)	Negative Supply Voltage Filter
CVDD	0.1µF – 15WV (note 1)	Positive Supply Voltage Filter
CAC	47µF – 10WV ± 20%	AC Path Decoupling (not polarised)
ZAC	(ZML – 2xRP) x 1.25	2 Wire AC Impedance
CCOMP	$\frac{1}{6.28 \times 30000 \times ZAC}$	AC Loop Compensation
RPC	RP x 2.5	R_p Insertion Less Compensation
RDC	(RFS – RP) x 1.25	DC Feeding Resistor
RL	24.9KΩ 1%	Bias Resistor
ZB	K Z_{LINE} (note 2)	Line Impedance Balancing Network
ZA	$0.8 \times K \times RPC + (0.8 \times K \times ZAC \,//\, \frac{CCOMP}{0.8 \times K})$	Line Impedance Balancing Network
C1 TX C2 TX R1 TX R2 TX	15nF 1% 15nF 1% 1.3KΩ 1% 2.21KΩ 1%	Teletaxe Filter (12kHz) (note 4)
CINT	(note 5)	Ring Trip Detection Time Constant

Notes : 1. In most applications these components can be shared between all the SLIC's on the Subscriber Card.
2. The structure of this network shall copy the line impedance Z_{LINE}, multiplied by a factor K=1 to . 10.
3 The structure of this network shall copy the SLIC output Impedance ZML multiplied by a factor K = 1 to 10 and compensate the effect of CCOMP on transhybrid rejection
4. If the Teletex Filter is not used, pin 23 must be connected to the pin 24 and the ext. component can be avoided.
5. CINT value depends on the ringing frequency Fr :

Fr (Hz)	16/19	19/23	23/27	27/34	34/41	41/49	49/61	61/68
CINT (nF)	470	390	330	270	220	180	150	120

ELECTRICAL CHARACTERISTICS

VDD = + 5V ; VSS = – 5V ; VB+ = + 72V ; VB– = – 48V ; Tamb = + 25°C)

STAND-BY

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
VLS	Output Voltage at L3000 Terminals	I line = 0mA	37		39	V
ILCC	Short Circuit Current				12	mA
Iot	Off-hook Detection Threshold		6		7.5	mA
Hys	Off-hook/on-hook Hysteresis		1.5		2.5	mA
Vls	Symmetry to Ground	I line = 0mA			.75	V

DC OPERATION - NORMAL BATTERY

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
VLO	Output Voltage at L3000 Line Terminals	I line = 0mA Data in 1X000XXX	37		39	V
Ilim	Current Program through the Digital Interface	Data in 1X000XXX	I_{LIM} – 10%	I_{LIM}	I_{LIM} + 10%	mA
Iot	Off-hook Detection Threshold		7.5			mA
Hys	Off-hook/on-hook Hysteresis		1.5		2.5	mA
Ilgk	Longitudinal Line Current with GDK Detect	I_{line} > 5mA	$\frac{I_{LINE}}{2.6}$		$\frac{I_{LINE}}{2.2}$	mA

DC OPERATION - BOOST BATTERY

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{LO}	Output Voltage at L3000 Line Terminals	I_{LINE} = 0mA	90		96	V
		I_{LINE} = 20mA RFS = 200Ω	81		89	V

AC OPERATION

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Ztx	Sending Output Impedance on TX	Data in 1X000XXX			15	Ω
THD	Signal Distortion at 2W and 4W Terminals	Vtx = 0dBm @ 1020Hz			0.5	%
Rl	2W Return Loss	f = 300 to 3400Hz	20			dB
Thl	Transhybrid Loss	f = 300 to 3400Hz	24			dB
Gs	Sending Gain	Vso = 0dBm f = 1020Hz	– 0.25		+ 0.25	dB
Gsf	Sending Gain Flatness vs. Frequency	f = 300 to 3400Hz Respect to 1020Hz	– 0.1		+ 0.1	dB
Gsl	Sending Gain Linearity	fr = 1020Hz Vsoref = – 10dBm Vso = + 4/– 40dBm	– 0.1		+ 0.1	dB

ELECTRICAL CHARACTERISTICS (continued)

AC OPERATION (continued)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Gr	Receiving Gain	Vri = 0dBm ; F = 1020Hz	– 0.25		+ 0.25	dB
Grf	Receiving Gain Flatness	f = 300 to 3400Hz Respect to 1020Hz	– 0.1		+ 0.1	dB
Grl	Receiving Gain Linearity	fr = 1020Hz Vriref = – 10dBm Vri = + 4/– 40 dBm	– 0.1		+ 0.1	dB
Np4W	Psophomet. Noise 4W - Tx Terminals			– 75	70	dBmop
NP2W	Psophomet. at Line Terminals			– 75	70	dBmop
SVRR	Supply Voltage Rejection Ratio Relative to VB–	Vn = 0.7Vrms F = 3400Hz F = 1000Hz F = 10Hz			 – 36 – 40 – 20	dB
SVRR	Relative to VDD	F = 3400Hz Vn = 100mVrms			– 20	dB
SVRR	Relative to VSS				– 20	dB
Ltc	Longitudinal to Transversal Conversion	F = 300 to 3400Hz I line = 30mA ZML = 600Ω	49 (*)	60		dB
Tlc	Transversal to Longitudinal Conversion		49 (*)	60		dB
Td	Propagation Time	Both Direction			40	µs
Tdd	Propagation Time Distortion				25	µs
Vttx	Line Voltage of Teletaxe Signal	Z_{LINE} = 200Ω	1.8		2.2	V
THD	Teletaxe Signal Harmonic Dist.				5	%
Zitt	Teletaxe Amplif. Input Impedance		100			KΩ

(*) : up to 52dB using selected L3000.

AC OPERATION BOOST BATTERY

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Gs	Sending Gain	Vso = 0dBm f = 1020HZ	– 0.5		+ 0.5	dB
Gr	Receiving Gain	Vri = 0dBm f = 1020HZ	– 0.5		+ 0.5	dB
Np4W	Psophometric Noise at 4W-Tx Terminals				– 68	dBmp
Np2W	Psophometric Noise at line Terminals			– 73	– 68	dBmp
SVRR	Supply Voltage Rejection Ratio Relative to VB+ (fig. 15)	V = 100mVrsm f = 3400Hz			– 30	dB
SVRR	Relative to Vdd	f = 3400Hz Vs = 100mVrms			– 20	dB
SVRR	Relative to Vss				– 20	dB

ELECTRICAL CHARACTERISTICS (continued)

RINGING PHASE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Vlr	Superimposed DC Voltage	Rloop > 100KΩ	19		30	V
		Rloop = 1KΩ	17		28	V
Vacr	Ringing Signal at Line Terminal	V_{RGIN} = 1Vrms/30Hz Rloop = 1kΩ + 1µF	56	60		Vrms
If	DC Off-hook Del Threshold		1.7		2.3	mA
Ilim	Output Current Capability		85		130	mA
Vrs	Ringing Voltage Symmetry				2	Vrms
THDr	Ringing Signal Distorsion				5	%
Zir	Ringing Amplicat. Input Impedance	Pin RGIN	50			KΩ
Vrr	Residual of Ringing Signal at Tx Output				600	mVrms
Trt	Ring Trip Detection Time	fring = 25Hz (T = 1/fring) CRT = 330nF			80(2T)	ms
Toh	Off-hook Status Delay after the Ringing Stop				120(3T)	µs

SUPPLY CURRENT

Symbol	Parameter		Min.	Typ.	Max.	Unit
I_{DD}	Positive Supply Current CS = 1	Stand-by Conversation (NB/BB) Ringing		16.3 26.4 26.4		mA mA mA
I_{SS}	Negative Supply Current CS = 1	Stand-by Conversation (NB/BB) Ringing		9.5 18 18		mA mA mA
I_{BAT-}	Negative Battery Supply Current Line Current = ØmA	Stand-by Conversation NB Conversation BB Ringing		2.9 9.8 13 26	4 12 16 28.5	mA mA mA mA
I_{BAT+}	Positive Battery Supply Current Line Current = ØmA	Stand-by Conversation NB Conversation BB Ringing		10 10 8 16	15 15 10 18.5	µA µA mA mA

NB = Normal Battery
BB = Boosted Battery

DIGITAL INTERFACE ELECTRICAL CHARACTERISTICS

(VDD = + 5V, ± 5% ; VSS = – 5V, ± 5% ; Tamb = 0 to + 70°C)

STATIC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Vil	Input Voltage at Logical "0"	Pins 15, 16, 17, 18	0		0.8	V
Vih	Input Voltage at Logical "1"		2.0		5	V
Iil	Input Current at Logical "0"	Vil = 0V			200	µA
Iih	Input Current at Logical "1"	Vih = 5V			40	µA
Vol	Output Voltage at Logical "0"	Pin 15 Iout = – 1mA			0.4	V
Voh	Output Voltage at Logical "1"	Pin 15 Iout = 1mA	2.4			V
Ilk	Tristate Leak Current	Pin 15 with NCS = "1"			10	µA

DINAMIC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
fclk	CKL Signal Frequency		1		512	Khz
Tr, Tf	CLK Rise and Fall Time				50	ns
Twh, Twl	CLK Impulse Width		800			ns
Tec	"1" RW to CKL Set up Time		100			ns
Tsc	CS to CLK Set up Time		0			ns
Tsk	CS to CLK Set up Time		400			ns
Tsd	Data in Set up Time		0			ns
Thd	Data in Hold Time		300			ns
Tcs	CS to CKL Hold Time		0		400	ns
Tca	RW to CKL Hold Time		200			ns
Tac	RW to CKL Set up Time		100			ns
Tzd	Data out to CS Delay		0		600	ns
Tce	RW to CKL Hold Time		200			ns
Tdz	High Imp. to CS Delay		50		200	ns
Tdd	Data out to CKL Delay		400		800	ns

Figure 6 : Writing Operation Timing (from controller to slic).

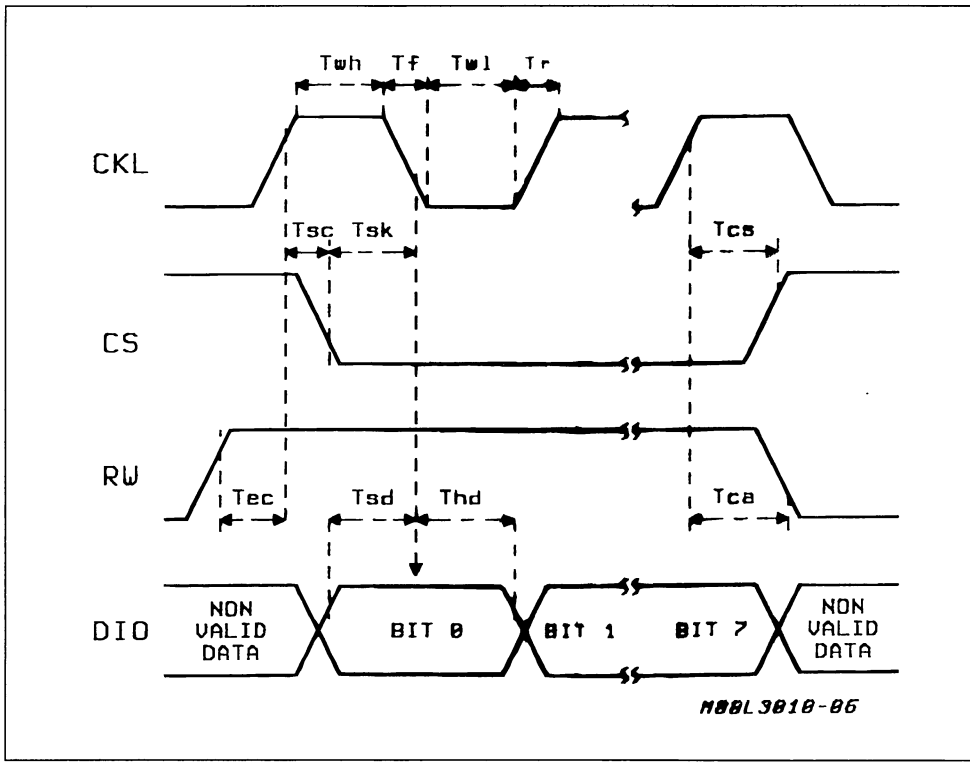


Figure 7 : Reading Operation Timing (from slic to controller).

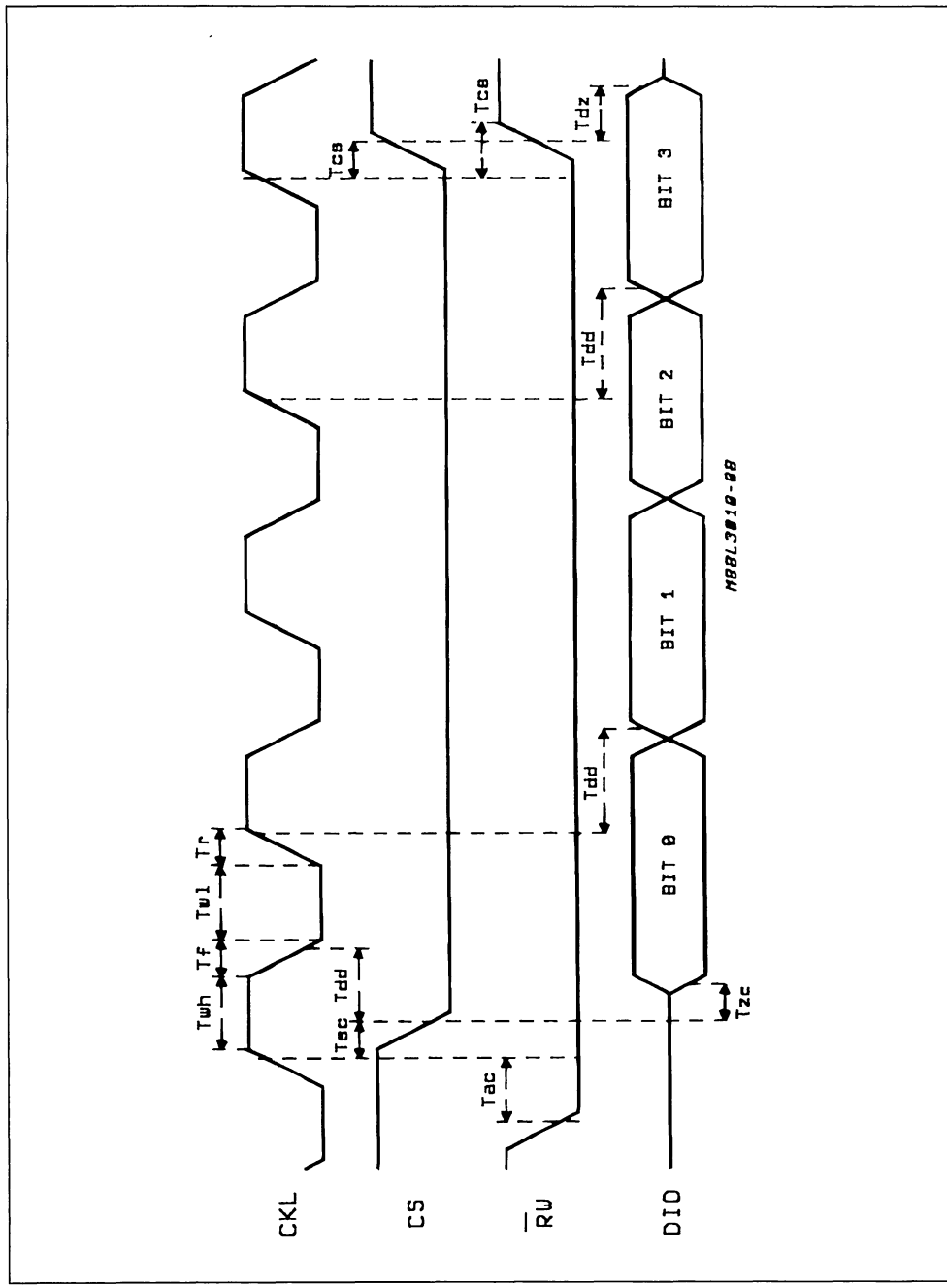
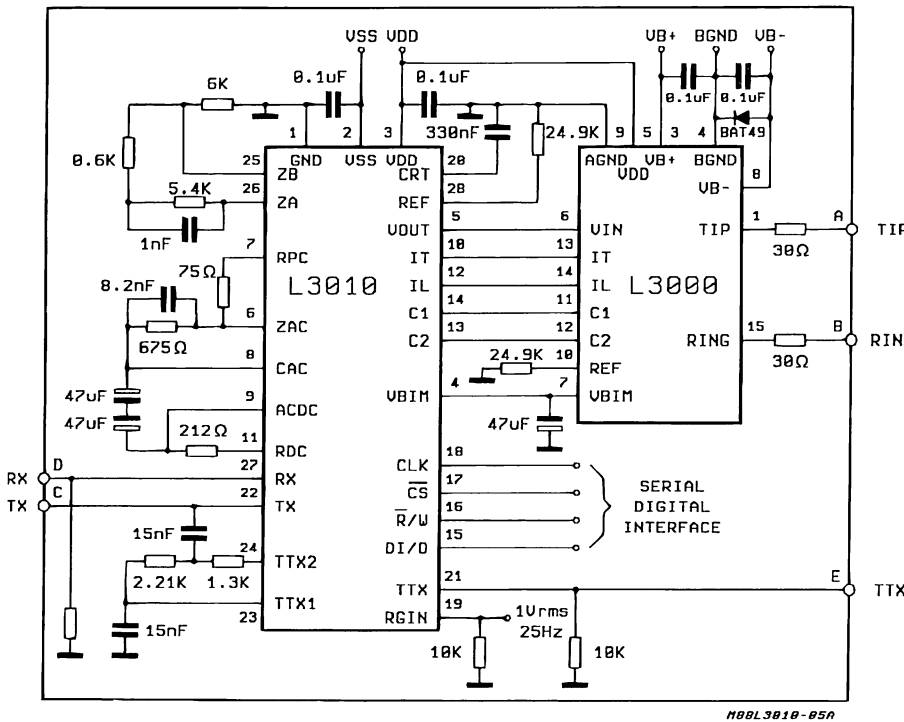


Figure 8 : Slic Test Circuit Schematic.



APPENDIX

SLIC test circuits

Referring to the test circuit reported at the end of each SLIC data sheet here below you can find the proper configuration for each measurement.

In particular : A-B : Line terminals

C : T_X sending output on 4W side

D : R_X receiving input on 4W side

E : T_{TX} teletaxe signal input

R_{GIN} : low level ringing signal input

TEST CIRCUITS

Figure 1 : Symmetry to Ground.

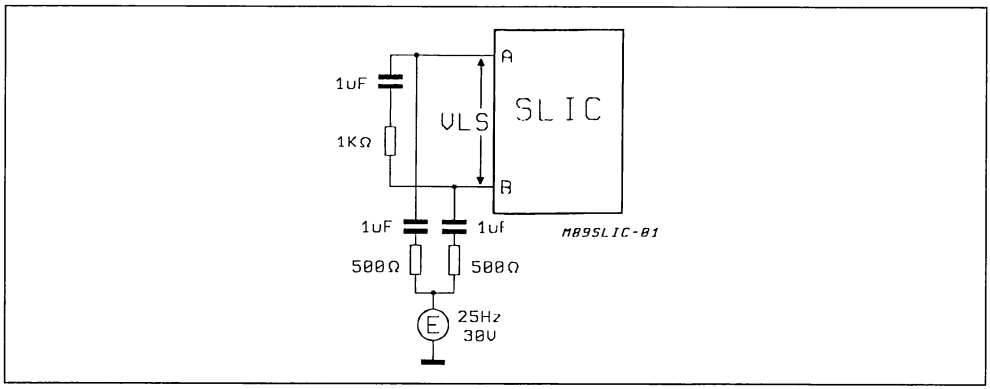
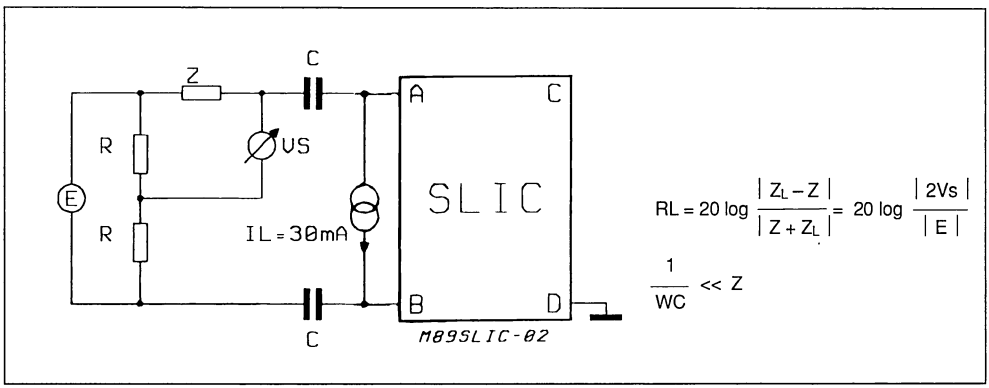


Figure 2 : 2W Return Loss.



TEST CIRCUITS (continued)

Figure 3 : Trans-hybrid Loss.

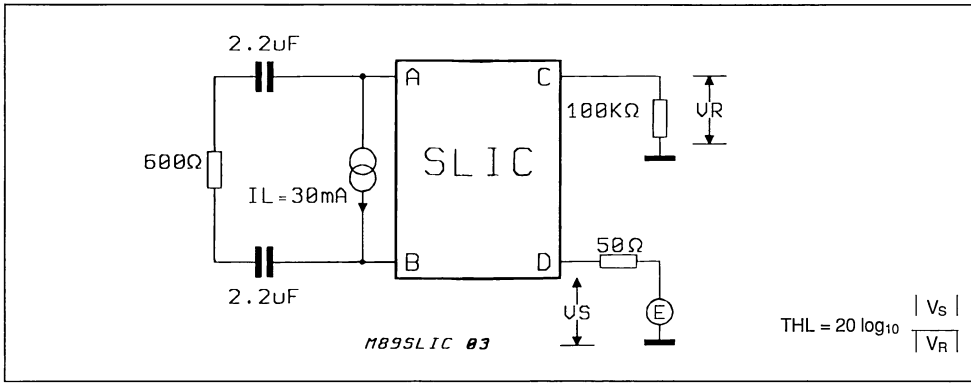


Figure 4 : Sending Gain.

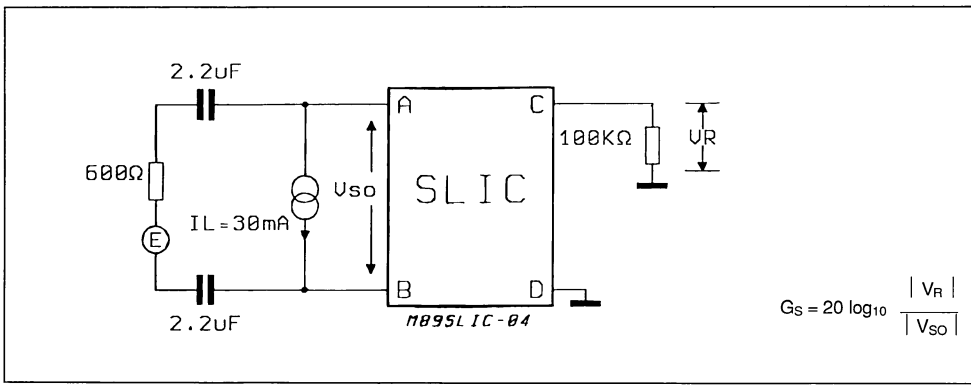
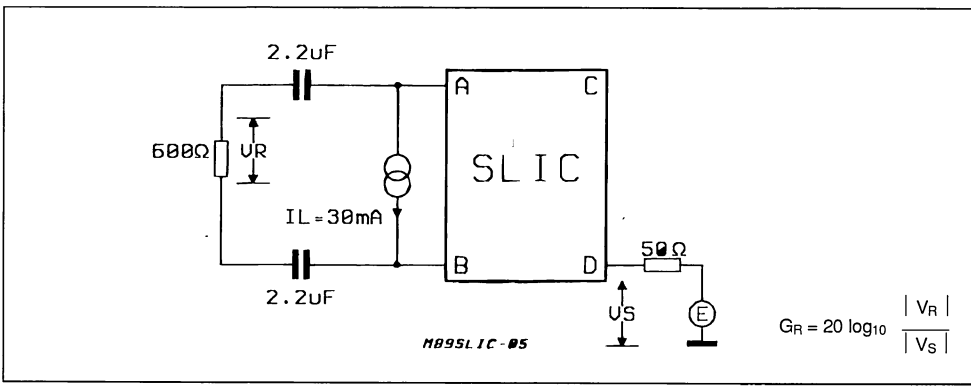


Figure 5 : Receiving Gain.



TEST CIRCUITS (continued)

Figure 6 : SVRR Relative to Battery Voltage VB–.

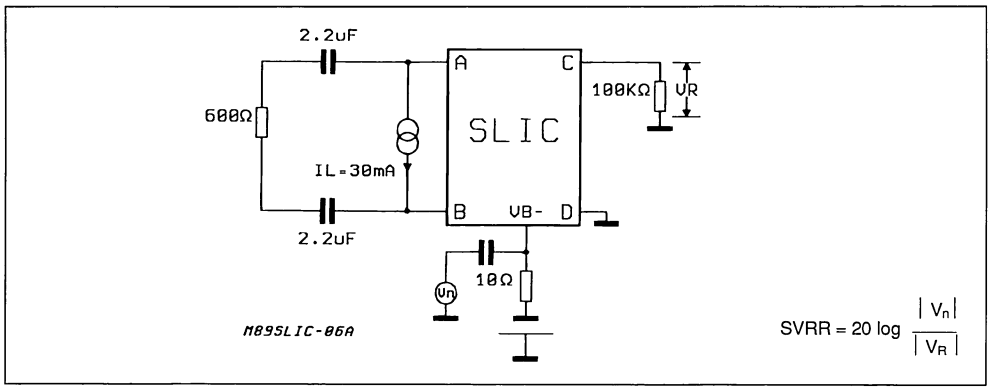


Figure 7 : Longitudinal to Transversal Conversion.

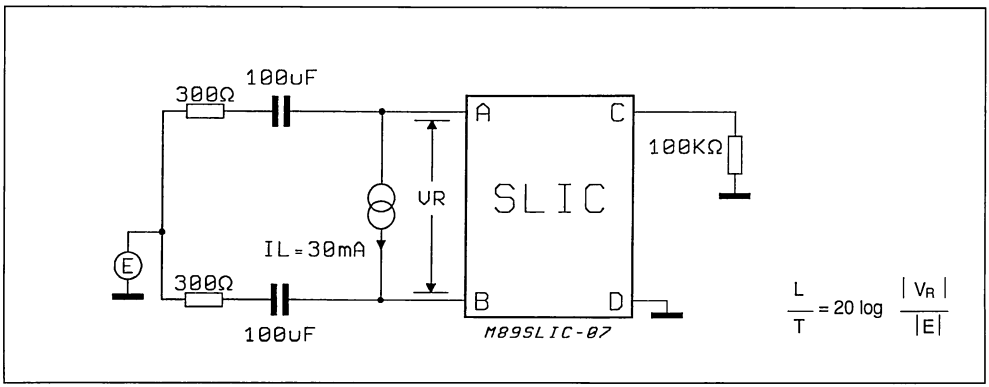
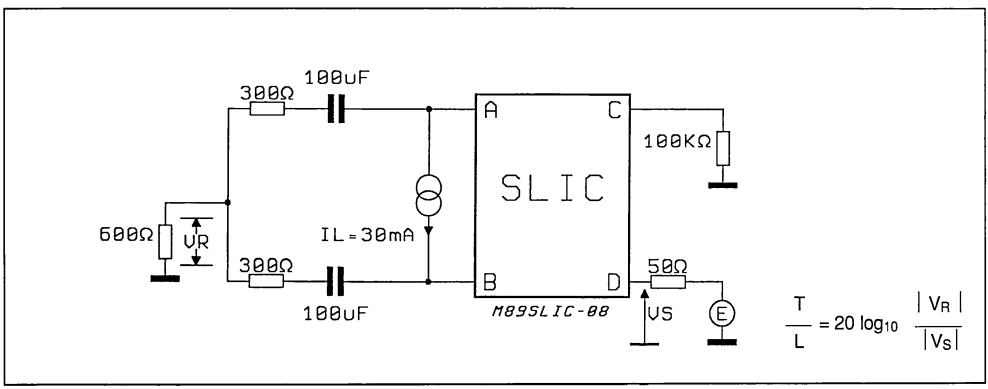


Figure 8 : Transversal to Longitudinal Conversion.



TEST CIRCUITS (continued)

Figure 9 : TTX Level at Line Terminals.

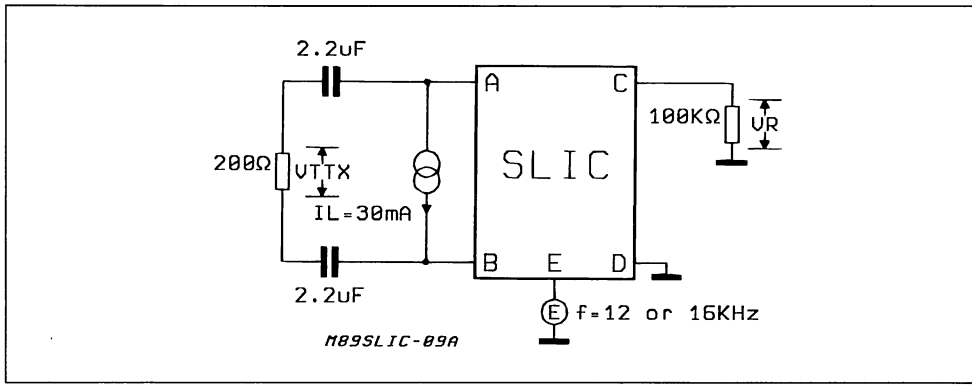
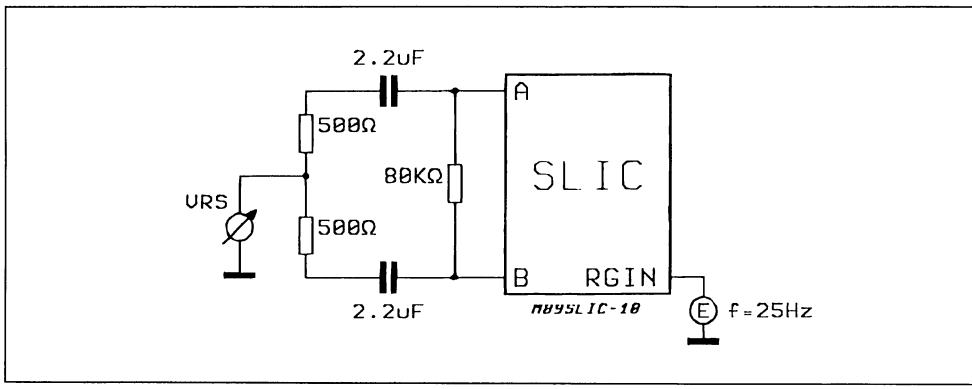


Figure 10 : Ringing Simmetry.



SGS-THOMSON MICROELECTRONICS

L3000
L3030

SUBSCRIBER LINE INTERFACE KIT

MAIN CHARACTERISTICS

- PROGRAMMABLE DC FEEDING RESISTANCE AND LIMITING CURRENT (four values available)
- THREE OPERATING MODES : STAND-BY, CONVERSATION, RINGING
- NORMAL/BOOST BATTERY, DIRECT/REVERSE POLARITY
- SIGNALLING FUNCTION (off-hook/GND-key)
- FILTERED OFF-HOOK DETECTION IN STAND-BY (10ms)
- QUICK OFF-HOOK DETECTION IN CONVERSATION (< 1ms) FOR LOW DIAL PULSE DETECTION DISTORTION
- HYBRID FUNCTION
- RINGING GENERATION WITH QUASI ZERO OUTPUT IMPEDANCE, ZERO CROSSING INJECTION (no ext. relay needed) AND RING TRIP DETECTION
- AUTOMATIC RINGING STOP WHEN OFF-HOOK IS DETECTED
- PARALLEL AND SERIAL DIGITAL INTERFACES
- TELETAXE SIGNAL INJECTION ($2V_{RMS}/5V_{RMS}$)
- LOW NUMBER OF EXTERNAL COMPONENTS
- GOOD REJECTION OF THE NOISE ON BATTERY VOLTAGE (20dB at 10Hz and 40dB at 1kHz)
- POSSIBILITY TO WORK ALSO WITH HIGH COMMON MODE CURRENTS
- INTEGRATED THERMAL PROTECTION WITH THERMAL OVERLOAD INDICATION

DESCRIPTION

The ST SLIC KIT (L3000/L3030) is a set of solid state devices designed to integrate main of the functions needed to interface a telephone line. It consists of 2 integrated devices : the L3000 line interface circuit and the L3030 control unit.

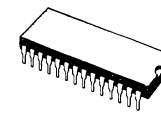
This kit performs the main features of the BORSHT functions :

- Battery feed
- Ringing
- Signalling
- Hybrid

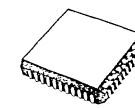
Additional functions, such as battery reversal, extra battery use, line overvoltage sensing and metering-pulse injection are also featured ; most external characteristics, as AC and DC impedances, are programmable with external components. The ST SLIC injects ringing in balanced mode and for that, as well as for the operation in battery boosted, a positive battery voltage shall be available on the subscriber card. As the right ringing signal amplification both in voltage and in current is provided by SLIC, the ring signal generator shall only provide a low level signal (0.285Vrms).

This kit is fabricated using a 140V Bipolar technology for L3000 and a 12V Bipolar I2L technology for L3030.

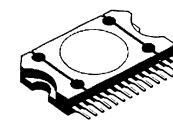
This kit is suitable for Central Office (German Specifications) and for the high range of PABX (Private Automatic Branch Exchange).



DIP28



PLCC44

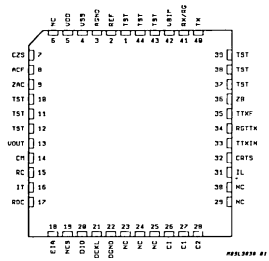


FLEXIWATT15

ORDER CODES :
L3030 (DIP28)
L3030P (PLCC44)
L3000 (FLEXIWATT15)

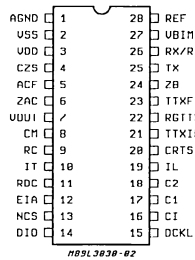
PIN CONNECTION (top view)

M89L3030-01



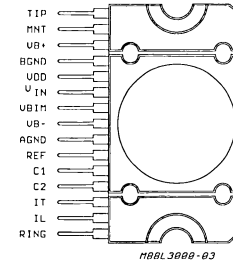
PLCC44

M89L3030-02



DIP28

M89L3000-03



FLEXIWATT15

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_b-	Negative Battery Voltage	– 80	V
V_b+	Positive Battery Voltage	80	V
$\|V_b-\| + \|V_b+\|$	Total Battery Voltage	140	V
V_{dd}	Positive Supply Voltage	+ 5.5	V
V_{ss}	Negative Supply Voltage	– 5.5	V
$V_{agnd} - V_{bgnd}$	Max. Voltage between Analog Ground and Battery Ground	5	V
T_j	Max. Junction Temperature	+ 150	°C
T_{stg}	Storage Temperature	– 55 to + 150	°C

THERMAL DATA

L3000 HIGH VOLTAGE

R_{thjc}	Max. Resistance Junction to Case	4	°C/W
R_{thja}	Max. Resistance Junction to Ambient	50	°C/W

L3030 LOW VOLTAGE

R_{thja}	Max. Resistance Junction to Ambient	80	°C/W

OPERATING RANGE

Symbol	Parameter	Min.	Typ.	Max.	Unit
T_{oper}	Operating Temperature Range	0		70	°C
V_b-	Negative Battery Voltage	– 70	– 48	– 24	V
V_b+	Positive Battery Voltage	0	+ 72	+ 75	V
$V_b- + V_b+$	Total Battery Voltage		120	130	V
V_{dd}	Positive Supply Voltage	+ 4.5		+ 5.5	V
V_{ss}	Negative Supply Voltage	– 5.5		– 4.5	V
I_{max}	Total Line Current			85	mA

PIN DESCRIPTIONS (L3000)

N°	Name	Description
1	TIP	A line termination output with current capability up to 100mA (I_a is the current sourced from this pin).
2	MNT	Positive Supply Voltage Monitor
3	V_B+	Positive Battery Supply Voltage
4	BGND	Battery ground relative to the V_B+ and the V_B- supply voltages. It is also the reference ground for TIP and RING signals.
5	V_{DD}	Positive Power Supply + 5V
6	VIN	2 wire unbalanced voltage input.
7	VBIM	Output voltage without current capability, with the following functions : - give an image of the total battery voltage scaled by 40 to the low voltage part. - filter by an external capacitor the noise on V_B-.
8	V_B-	Negative Battery Supply Voltage
9	AGND	Analog Ground. All input signals and the V_{DD} supply voltage must be referred to this pin.
10	REF	Voltage reference output with very low temperature coefficient. The connected resistor sets internal circuit bias current.
11	C1	Digital signal input (3 levels) that defines device status with pin 12.
12	C2	Digital signal input (3 levels) that defines device status with pin 11.
13	I_T	High precision scaled transversal line current signal. $I_T = \frac{I_a + I_b}{100}$
14	IL	Scaled longitudinal line current signal. $IL = \frac{I_a - I_b}{100}$
15	RING	B line termination output with current capability up to 100mA (I_b is the current sunk into this pin).

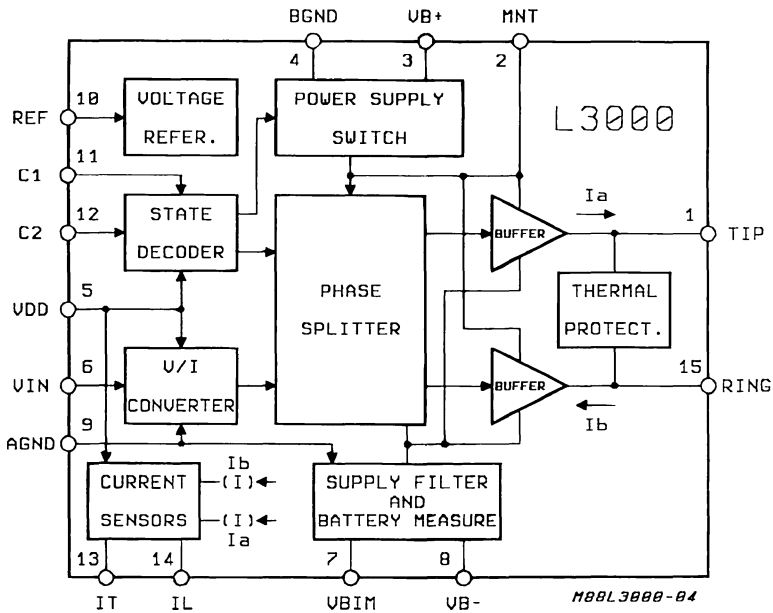
L3030 - PIN CONFIGURATION

Pin		Symbol	Function
PLCC-44	DIP-28		
1		TST	This pin is connected internally for test purpose. It should not be used as a tie point for external components.
2	28	REF	Bias Set
3	1	AGND	Analog Ground
4	2	VSS	– 5V
5	3	VDD	+ 5V
6		N.C.	Not connected.
7	4	CZS	AC Feedback Input
8	5	ACF	AC Line Impedance Synthesis
9	6	ZAC	AC Impedance Adjustement
10		TST	This pin is connected internally for test purpose. It should not be used as a tie point for external components.
11		TST	This pin is connected internally for test purpose. It should not be used as a tie point for external components.
12		TST	This pin is connected internally for test purpose. It should not be used as a tie point for external components.
13	7	VOUT	Two wire unbalanced output.
14	8	CM	Capacitor Multiplier Input
15	9	RC	DC Feedback Input
16	10	IT	Transversal Line Current
17	11	RDC	DC Feeding System
18	12	EIA	Read/write Command
19	13	NCS	Chip Select Command
20	14	DIO	Data Input/output
21	15	DCLK	Clock Signal
22		DGND	Digital Ground
23		N.C.	Not connected.
24		N.C.	Not connected.
25		N.C.	Not connected.
26	16	CI	Input/output Changing Command
27	17	C1	State Control Signal 1
28	18	C2	State Control Signal 2
29		N.C.	Not connected.
30		N.C.	Not connected.
31	19	IL	Longitudinal Line Current
32	20	CRTS	Ring trip Det. & TTX Shaping
33	21	TTXIN	Teletax Signal Input
34	22	RGTTX	TTX Filter Level Compensation
35	23	TTXF	TTX Filter Input
36	24	ZB	Balancing Network

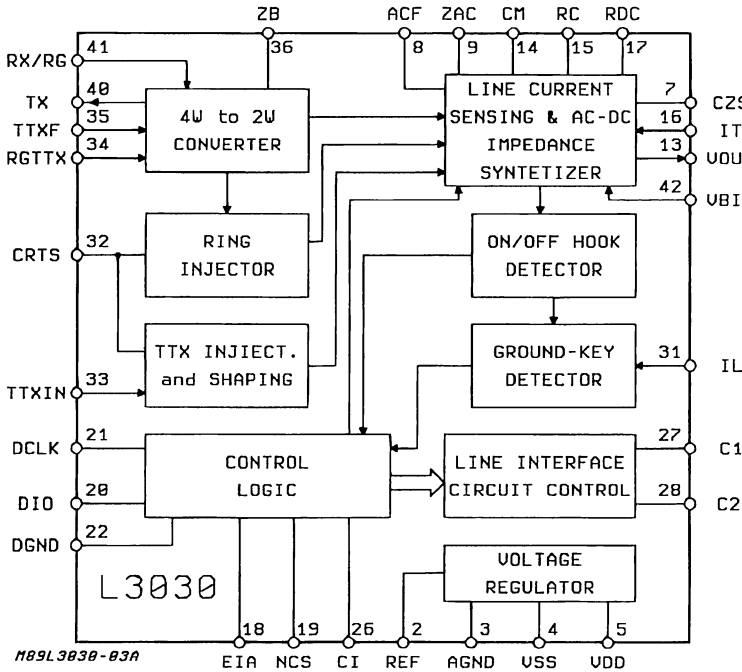
L3030 - PIN CONFIGURATION (continued)

Pin		Symbol	Function
PLCC-44	DIP-28		
37		TST	This pin is connected internally for test purpose. It should not be used as a tie point for external components.
38		TST	This pin is connected internally for test purpose. It should not be used as a tie point for external components.
39		TST	This pin is connected internally for test purpose. It should not be used as a tie point for external components.
40	25	TX	4W Sending Output
41	26	RX/RG	4W Receiving and Ring Input
42	27	VBIM	Battery Image Input
43		TST	This pin is connected internally for test purpose. It should not be used as a tie point for external components.
44		TST	This pin is connected internally for test purpose. It should not be used as a tie point for external

L3000 BLOCK DIAGRAM



L3030 BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

L3000 - HIGH VOLTAGE CIRCUIT

The L3000 line interface provides a battery feeding for telephone lines and ringing injection. The IC contains a state decoder that under external control can force the following operational modes : stand-by, conversation and ringing.

In addition Power down mode can be forced connecting the bias current resistor to VDD.

Two pins, I_L and I_T, carry out the information concerning line status which is detected by sensing the line current into the output stage.

The L3000 amplifies both the AC and DC signals entering at pin 6 (VIN).

Separate grounds are provided :

- Analog ground as a reference for analog signals
- Battery ground as a reference for the output stages

L3030 - CONTROL UNIT

The L3030 low voltage control unit controls L3000 line interface module, giving the proper information to set line feed characteristic, to inject ringing and TTX signal. An on chip digital interface allows a microprocessor to control all the operations. L3030 defines working states of line interface and also informs the controller about line status.

If it's not otherwise specified pins number are coming from PLCC44 package.

L3000 - WORKING STATES

In order to carry out the different possible operations, the ST SLIC kit has several different working states. Each state is defined by the voltage respectively applied by pins 27 and 28 of L3030 to the pins 11 and 12 of L3000.

Three different voltage levels (– 5, 0, + 5) are available at each connection, so defining nine possible states as listed in tab. 1.

Table 1.

		Pin 28 of L3030 / Pin 12 of L3000		
		+ 3	0	– 3
Pin 27 of L3030 / Pin 11 of L3000	+ 3	Stand-by	Conversation in Normal Battery Direct Polarity	Conversation in Normal Battery Reverse Polar
	0	Not allowed.	Conversation in Boost Battery Direct Polarity	Conversation in Boost Battery Reverse Polar
	– 3	Not allowed.	Ringing with Direct Polarity	Not allowed.

Appropriate combinations of two pins define the three modes of the ST SLIC, that are :

a) Stand-by (SBY)

b) Conversation (CVS)

c) Ringing (RING)

In Stand-by and in ringing just one condition is allowed (normal battery and direct polarity) but four are possible in conversation (normal battery or boost battery, direct polarity or reverse polarity).

Inside the conversation mode, two more functions are also available, that do not affect the particular operation where the SLIC is set. The functions are :

1) Current limiting (with 4 possible levels)

2) Metering pulse injection

It is always possible to switch from one state to another.

A fourth status, Power down (PD), can be set disconnecting the bias resistor (RH) from pin 10 of L3000 by means of an external transistor.

The main difference between Stand-by and Power down is that in SBY the power consumption on the voltage battery VB– (– 48V) is reduced but the SLIC can recognize yet the On hook/Off hook status. In PD the power consumption on VB- is reduced to zero, but none operation can be performed by the SLIC.

The SBY status should be used when the telephone is in On hook and PD status only in emergency condition when it is mandatory to cut any possible dissipation but no operation are requested.

OPERATING MODES

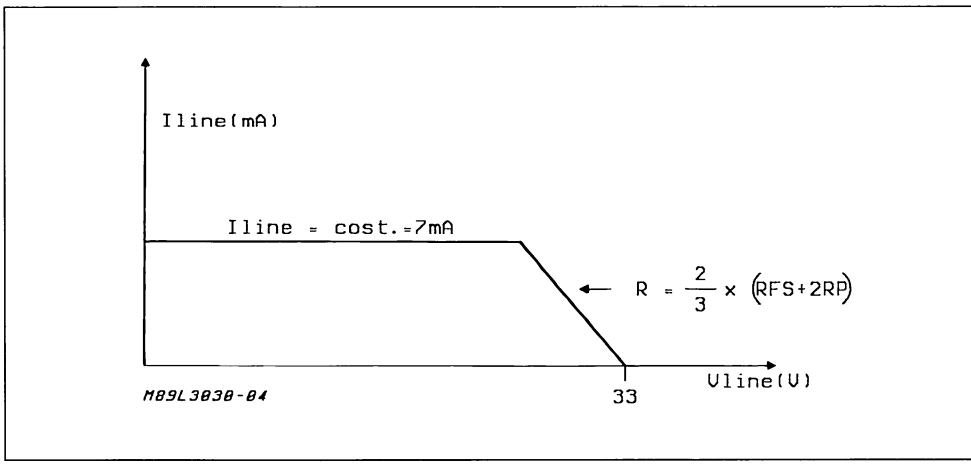
STAND-BY (SBY) MODE

In this mode, the bias currents of both L3000 and L3030 are reduced as only some parts of the two circuits are completely active, control interface and current sensors among them. The current supplied to the line is limited at 7mA, and the slope of the DC characteristic corresponds to :

$$R = \frac{2}{3} \times (RFS + 2RP)$$

The Line voltage with an infinite load resistance is just the battery voltage minus the voltage drop (approx. 15V) of the output stage amplifiers (see fig. 1).

Figure 1 : DC Characteristics in Stand-by Mode.



The AC characteristic is just the resistance of the two serial resistors RP.

In Stand-by mode the battery polarity is just in direct condition, that is the TIP wire more positive than the RING one ; boost battery is not achievable. There are two possible line conditions where the SLIC is expected to be in stand-by mode :

1) ON-HOOK (Iline < 5mA). Normal on-hook condition.

2) OFF-HOOK (Iline > 7mA). Handset is unhooked, the SLIC is waiting for command to activate conversation.

When the ST SLIC is in stand-by mode, the power dissipation of L3000 does not exceed 200mW (from - 48V) eventually increased of a certain amount if some current is flowing into the line. Depending on the total loop resistance, included telephone set and RP, this quantity will range from 200mW (total loop resistance of 3.5 Kohm) to about 800mW (total loop resistance of 140 ohm).

The power dissipation of L3030 in the same condition, is typically 120mW.

The Stand-By Mode is set when the byte sent to the L3030 Serial Digital Interface has the first two bits (BIT0R and BIT1R) equal to "0".

Setting to 0 all the 8 bits of the command sent to the digital interface of L3030, the bias currents of both L3000 and L3030 are reduced and only some parts of the two circuits are active similarly to the stand-by mode ; in this situation, named power-down denial, the line sensors are disabled (ON/OFF-HOOK line conditions cannot be recognized) and the current supplied to the line is limited at 0.25mA.

CONVERSATION (CVS) OR ACTIVE MODE

In conversation mode it is possible to select between two different DC Characteristics by the BIT5R of the Serial Interface.

1) Normal Battery (NB)

2) Boost Battery (BB)

It is also possible to select (BIT4R) the polarity of the DC line voltage and (BIT6R-BIT7R) one of the four values of limiting current (25mA or 30mA or 45mA or 70mA).

Battery reverse can take place either before or during conversation.

As far as the DC characteristic in Normal Battery is concerned, three different feeding conditions are present :

a) current limiting region ; the DC impedance of the SLIC is very high (> 20 Kohm) and therefore the system works like a current generator, the current value being set through the digital interface (25/30/45/70mA).

b) standard feeding system region ; the characteristic is equal to a – 48V (– 60V) battery (note 1), in series with two resistors, whose value is set by external components (see external component list of L3030).

c) low impedance region ; the battery value is reduced to 33V (45V) and the serial resistance is reduced to the value specified in stand by mode, that is :

$$\frac{2}{3} \times (RFS + 2\,RP)$$

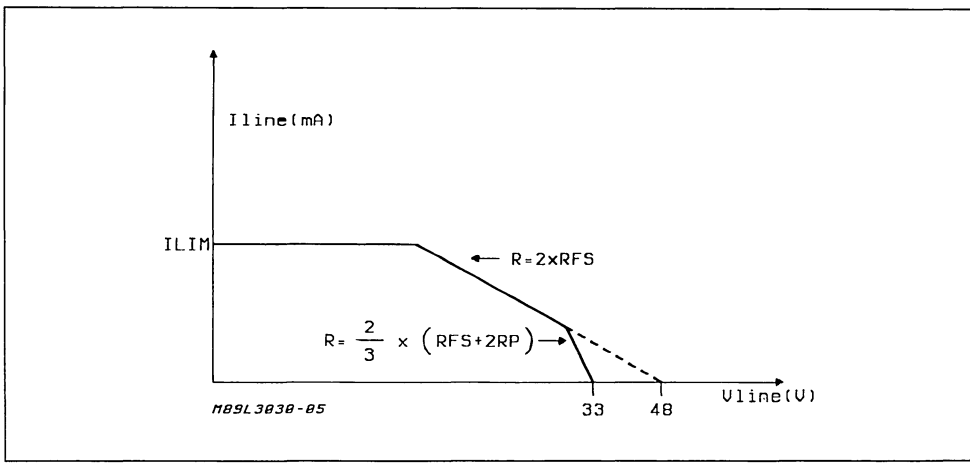
Switching between the three region is automatic without discontinuity, and depends on the loop resistance. Fig. 2 shows the DC characteristic in normal battery condition.

When the boost battery condition is activated the low impedance region can never be reached by the system ; in this case the internal dropout voltage is equal to 30V.

Fig. 3 shows the DC characteristic in boost battery condition.

In conversation mode, on request of control processor, whatever condition is set (normal or boost battery, direct or reverse polarity), you can inject the 12kHz (or 16kHz) signal (permanently applied at the pin 33), as metering pulses. A patented automatic control system adjust the level of the metering signal, across the line, to 2Vrms setting BIT3 = 0, or to 5Vrms setting BIT3 = 1 ; this, regardless of the line impedance. Moreover the metering signal is ramped at the beginning and at the end of each pulse to prevent undesirable clicking noise ; the slope is determined by the value of CINT (see the external component list of L3030). The SLIC also provides, in the transmit direction (from line to 4-wire side), an amplifier to insert an external notch filter (series resonator) for suppressing the 12/16kHz residual signal.

Figure 2 : DC Characteristic (n.b.) I_{LIM} = 25/30/45/70 mA.



Note : 1. This value of voltage battery, named apparent battery, is fixed internally by the control unit and is independent of the actual battery value So, the voltage drop in the low impedance region is 15V. It is also possible to increase up to 25V this value setting BIT3R to 1.

Figure 3 : DC Characteristic (b.b.) I_{LIM} = 25/30/45/70 mA.

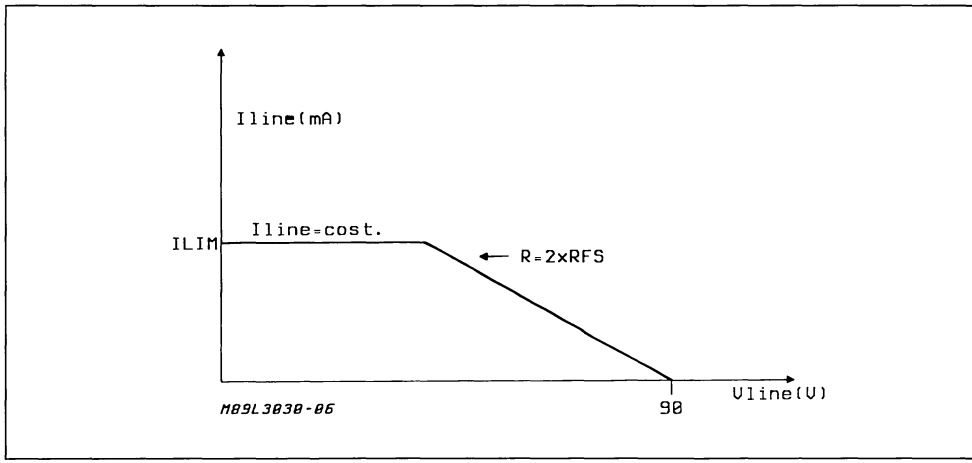


Fig. 4 shows a suggested notch Filter configuration.

The metering pulses can be injected with a DC line current equal to zero (ON-HOOK Operation).

In conversation mode the AC impedance at the line terminals, ZML, is synthetized by the external components ZAC and RP, according to the following formula :

$$ZML = ZAC + (RP1 + RP2)$$

Depending on the characteristic of the ZIAC network, ZML can be either a pure resistance or a complex impedance, so allowing ST SLIC to meet different standards as far as the return loss is concerned. The capacitor CCOMP guarantees stability to the system.

The two-to-four wire conversion is achieved by means of a Wheatstone bridge configuration, the sides of which being :

1) the line impedance (Zline),

2) the SLIC impedance at line terminals (ZML),

3) the network ZA connected between pin 36 and 41 of L3030 (see external component list of L3030),

4) the network ZB between pin 36 and ground that shall copy the line impedance.

For a perfect balancing, the following equation shall be verified :

$$\frac{ZA}{ZB} = \frac{ZML}{Zline}$$

It is important to underline that ZA and ZB are not obliged to be equal to ZML and to Zline, but they both may be multiplied by a factor (up to ten) so allowing use of smaller capacitors.

In conversation, the L3000 dissipates about 500mW for its own operation ; the dissipation depending on the current supplied to the line shall be added.

The fig 5 and fig 6 show the DC characteristic for two different Feeding resistance.

2 x 200 Ohm and 2 x 400 respectively.

Figure 4 : External Teletaxe Filter.

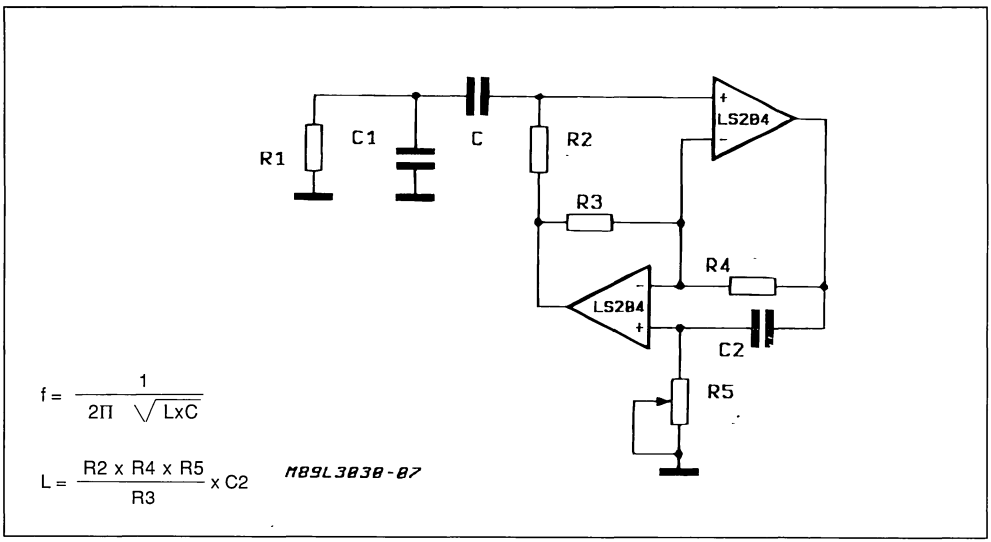


Figure 5 : DC Characteristic for 2 x 200 ohm Feeding System.

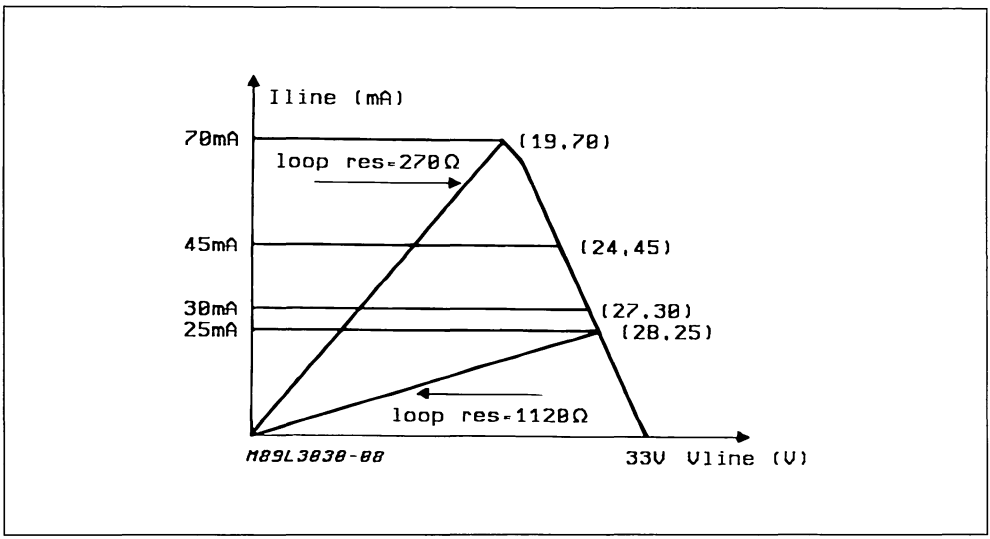


Figure 6 : DC Characteristic for 2 x 400 ohm Feeding System.

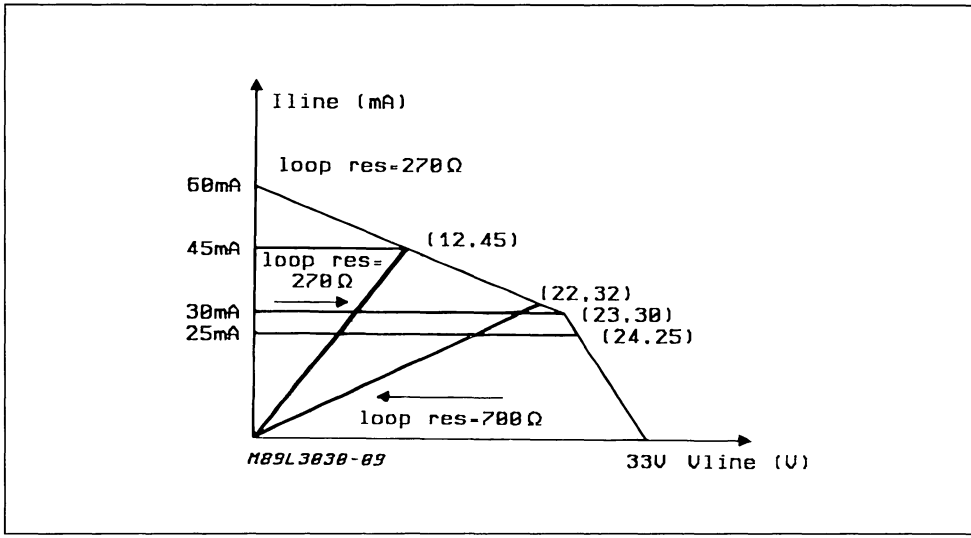
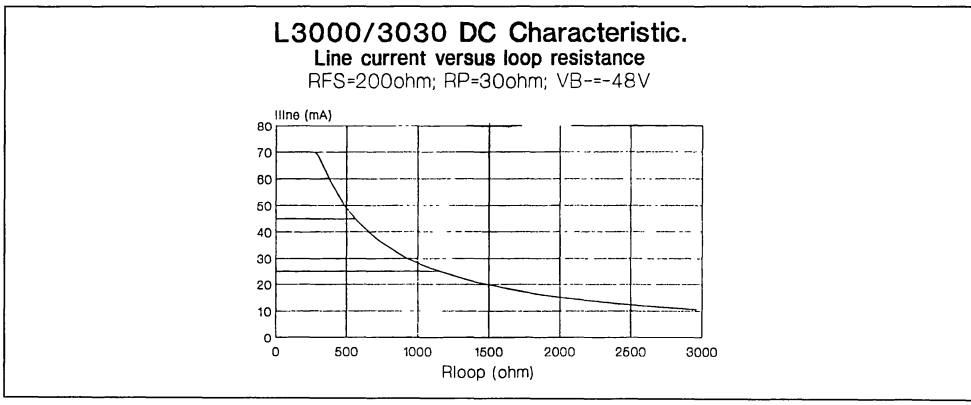


Figure 7 : Line Current Versus Loop Resistance.



RINGING

When ringing is selected BIT2R = 1, BIT0R = 0), the control unit L3030 presets the L3000 to operate between – 48V (– 60V) and + 72V (+ 60V) battery. Then, setting BIT1 = 1, a low level signal (0.285Vrms with frequency range 16-66Hz) applied to pin 41, is amplified and injected in balanced mode to the line through L3000 with a superimposed DC voltage of 24V. The impedance to the line is given by the two external resistors and the 24V DC polarity can only be direct.

The first and the last ringing cycles are synchronized by L3030 so that ringing always starts and stops at zero crossing. Ring trip detection is performed autonomously by the SLIC, without any particular command, using a patented system ; when handset is lifted, SLIC suspends the ringing signal just remaining in the ringing mode. In this condition, the control unit L3030 checks that the loop is closed for a time equal to two periods of the ringing signal ; if the closure is confirmed, a flag (BIT0T = 1) is set and the SLIC waits the new command from the control processor. Whereas the loop closure is not confirmed, the ringing signal is newly applied to the line, without setting BIT0T.

DIGITAL INTERFACE

FUNCTIONAL DESCRIPTION

The L3030 states and functions are controlled by central processor through five wires defining a digital interface. It is possible to select the interface working mode between SERIAL or PARALLEL (pin 33 tied to a voltage between 4 and 5V).

1) SERIAL MODE

The five wires of the digital interface have the following functions :

- clock (DCLK), entering at pin 21
- data in/data out (DIO), exchanged at pin 20
- input/output select (EIA), entering at pin 18
- chip select (NCS), entering at pin 19
- change NCS from in to out (CI), entering at pin 26 (note 1)

The maximum clock frequency is 600Khz.

When EIA signal is low data are transferred from the card controller into I/O registers of the L3030 selected by NCS signal tied at low level ; then data are latched for execution. In this phase a complete 8 bit word is loaded into internal register and consequently NCS signal must remain low for the corresponding 8 clock pulses (DCLK). The EIA signal must remain at low level at least for the time in which NCS signal remain low. The device load data in input register during the positive edge of clock signal (DCLK) and store the contents of the register on the positive edge of NCS signal.

When EIA signal is high data are transferred from the L3030 selected by NCS tied to low level to the card controller. The L3030 status is described by five bits contained in the output register ; the NCS signal can remain low for five or less clock pulses depending if the card controller want to read the complete L3030 status or only a part of it.

Fig. 8, 9 show the complete write and read operation timing. Table 1 shows the meaning of each bit of an I/O data.

Table 1 : Serial Mode.

Data in (note 2)				
Meaning	**Value**			
BIT0R = Impedance (note 3)	0 - Stand-by/ringing			
	1 - Conversation			
BIT1R = TTX & Ring Timing (note 4)	0 - Timing off			
	1 - Timing on			
BIT2R = Ring (note 5)	0 - TTX Signal Injection			
	1 - Ring Signal Injection			
BIT3R = TTX Level	0 - Low Amplitude ($2V_{RMS}$)			
	1 - High Amplitude ($5V_{RMS}$)			
BIT4R = Battery Polarity	0 - Normal Polarity			
	1 - Reverse Polarity			
BIT5R = Extra Feeding	0 - Normal Battery			
	1 - Boosted Battery			
BIT6R Current BIT7R Limiting	0 25mA 0	0 30mA 1	1 45mA 1	1 70mA 0

Notes : 1. When CI signal is tied to low level, NCS signal is the chip select input ; with CI signal at high level, the NCS signal becomes an output that carry out the logical sum of the following bits : BIT0T, BIT1T.
2. The description of the commands is referred to the system L3030 + LINE INTERFACE module.
3. To set SBY mode with Ilim = 7mA : BIT0R = 0 and at least one of the two last bits (BIT6R ; BIT7R) must be set to 1.
4. TTX and RING signals are injected into the line interface module with BIT1R to "1".
5. To set RING mode at least one of the three last bits (BIT5R, BIT6R, BIT7R) must be set to 1, in addition BIT0R must be set to 0.

Table 1 : Serial Mode.

Data Out (note 1)	
Meaning	**Value**
BIT0T = Line Supervision	0 - On Hook
	1 - Off Hook
BIT1T = Ground Key	1 - Long. Line Current < 17mA
	0 - Long. Line Current > 17mA
BIT2T = Internal Line Current Limiter (note 2)	0 - Off
	1 - On
BIT3T = Line Voltage	0 - Normal
	1 - Minus of Half Battery
BIT4T = Thermal Overload (note 3)	1 - Off
	0 - On

Notes : 1. The description of the commands is referred to the system L3030 + LINE INTERFACE module.
2. The bit BIT2T is set to 1 when the SLIC is operating in Conversation Mode and into the limiting current region (short loop).
3. The bit BIT4T is set to 1 when the junction temperature of L3000 is about 140°C.

Figure 8 : Writing Operation Timing (serial mode).

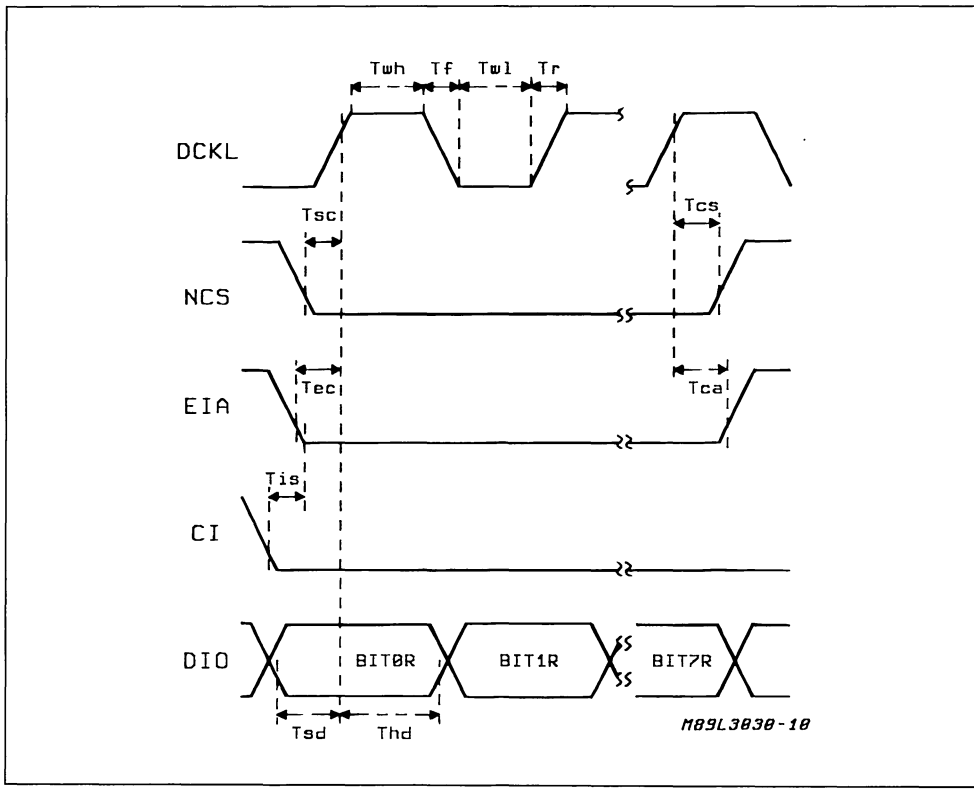
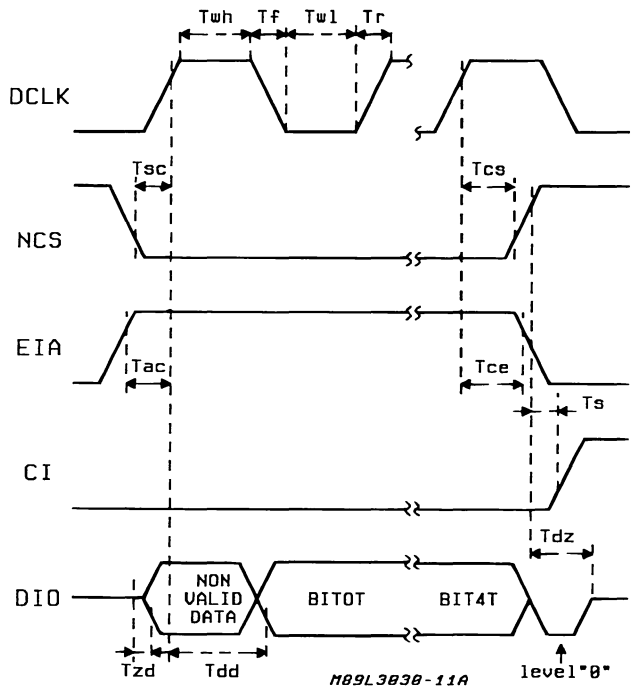


Figure 9 : Reading Operation Timing (serial mode).



2) PARALLEL MODE

This operating mode is enabled connecting pin 33 to a voltage in the range from 4V to 5V. The five wire have the following functions :

- power down/feeding (EIA), entering at pin 18
- timing (CI), entering at pin 26
- ring (DCLK), entering at pin 21
- on-hook/off-hook (NCS), outgoing at pin 19
- ground-key (DIO), outgoing at pin 20

In this operating mode the signals at the inputs are immediately executed, without any external clock timing ; all the internal registers are bypassed. The informations sent back on pins 19 and 20, display in real time the setting of internal circuits, that means line status. In the table 2 the correspondence between the interface wires in the parallel mode and equivalent bit in serial mode is pointed out ; where there isn't this correspondence, the internal setting is shown.

Table 2 : Parallel Mode.

Pin	Rif.	Meaning (note 1)	Eq. Bit of Ser. Interf.	Value
18	EIA	PD/feeding	BIT0R	0 : High Impedance
				1 : Low Impedance
26	CI	Timing	BIT1R	0 : Ring Timing Off
				1 : Ring Timing On
21	DCLK	Ring	BIT2R	0 : No Ring
				1 : Ring Injection
			BIT3R	0 : Low Amplitude
			BIT4R	0 : Normal Polarity
			BIT5R	0 : Normal Battery
			BIT6R	0 :
			BIT7R	1 : Line Curr. = 30mA
19	NCS	On-hook/off-hook	BIT0T	0 : On-hook
				1 : Off-hook
20	DIO	Ground Key	BIT1T	0 : Long. Curr. < 17mA
				1 : Long. Curr. > 17mA
			BIT2T	
			BIT3T	
			BIT4T	

Note : 1 The description of the commands is referred to the system L3030 + LINE INTERFACE module

DIGITAL INTERFACE ELECTRICAL CHARACTERISTICS (VDD = + 5V, VSS = – 5V, Tamb. = @% C) (refer to PLCC44 package)

STATIC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Vil	Input Voltage at Logical "0"	Pins 18, 19, 20, 21, 26	0		0.8	V
Vih	Input Voltage at Logical "1"		2.0		5	V
Iil	Input Current at Logical "0"	Vil = 0V			200	µA
Iih	Input Current at Logical "1"	Vih = 5V			10	µA
Vol	Output Voltage at Logical "0"	Pins 19, 20 Iout = – 1mA			0.4	V
Voh	Output Voltage at Logical "1"	Pins 19, 20 Iout = 1mA	2.4			V
Ilk	Tristate Leak. Current	Pin 20 NCS = "1"			10	µA

DINAMIC ELECTRICAL CHARACTERISITCS

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
fclk	Clock Frequency		1		600	KHz
Tr, Tf	Clock Rise and Fall Time				50	ns
Twh, Twl	Clock Impulse Width		750			ns
Tis	CI to NCS Set up Time		300			ns
Tec	"0" EIA to DCLK Set up Time		300			ns
Tsc	DCKL to NCS Delay (+ edge)		300			ns

DINAMIC ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Tsd	Data in Set up Time		0			ns
Thd	Data in Hold Time		500			ns
Tcs	NCS to DCLK Hold Time		800			ns
Tca	"0" EIA to DCLK Hold Time		800			ns
Tac	"1" EIA to DCLK Set up Time		200			ns
Tzd	Data out to "0" NCS Delay		0		600	ns
Tce	"1" EIA to DCLK Hold Time		800			ns
Tdz	Data out to "1" NCS Delay				500	ns
Tdd	Data out to DCLK Delay				1500	ns
Tsi	"0" CI to NCS Hold Time		300			ns

OPERATION DESCRIPTION

To set ST SLIC in operation the following parameters have to be defined :

- the DC feeding resistance RFS, defined as the resistance of each side of the traditional feeding system (most common values are 200, 400 or 500 ohm).
- the AC impedance at line terminals, ZML, to which the return loss measurement references. It can be real (typically 600 ohm) or complex.
- the equivalent AC impedance of the line Zline, when evaluating the trans hybrid loss (2/4 wire conversion). It is usually a complex impedance.
- the ringing signal frequency Fr (ST SLIC allows frequency ranging from 16 to 66Hz).
- the metering pulse frequency Ft (two values are possible : 12Khz or 16Khz).
- the value of the two resistors RP1/RP2 in series with the line terminals ; main purpose of the a.m. resistors is to allow primary protection to fire. ST suggest the minimum value of 50 ohm for each side.

On this assumptions, the following component list is defined.

EXTERNAL COMPONENT LIST FOR THE LINE INTERFACE L3000

Component			Involved Parameter or Function
Ref.	Pin	Value	
RH	10	24.9KΩ ± 2%	Bias Resistance
RP	1, 15	30 to 100Ω	Line Series Resistor
CDVB	7	47µF – 10V	Battery Voltage Rejection
CVB+ (note 1)	3	0.1µF – 100V	Positive Battery Filter
CVB– (note 1)	8	0.1µF – 100V	Negative Battery Filter
D1 (note 1)	8	BAT 49	Protective Shottky Diode

Note : 1. CVB+, CVB- and D1 can be shared with the others SLIC of the Line Card.

EXTERNAL COMPONENT LIST FOR THE CONTROL UNIT L3030

Pin PLCC44	Component		Involved Parameter or Function
	Ref.	Value	
4-3	CVSS	0.1µF – 15V	Negative Supply Voltage Filter (note 6)
5-3	CVDD	0.1µF – 15V	Positive Supply Voltage Filter (note 6)
7-8	RR	10.....50KΩ	Capacitor Multiplier Gain
15-17	RDC	2 x (RFS – RP1)	(RP1 = RP2)
7-15	CAC1 (note 1)	$\frac{1}{6.28 \times 250 \times (ZAC + RDC)}$	
14-15	CAC2	CAC1	
8-9	ZAC	ZML – (RP1 + RP2)	DC Feeding System and AC Impedence Adjustement
8-9	CCOMP	1/(6.28 x 150000 x (RPc))	
9-14	RPC	RP1 + RP2	
2-3	RL	24.9KΩ 1%	Bias Resistance
36-3	ZB	K x Zline (note 2)	Line Imped. Balancing Network
36-41	ZA	K x RPC in Series with K x ZAC // (CCOMP/K)	SLIC Impedence Balancing Network (note 3)
32-3	CINT	(note 4)	Time Constant
31-4	D2	BAT48	Protective Shottky Diode (note 6)
15-16	Ccon	0.15µF (note 5)	Interface Time Constant

Notes : 1. If the internal capacity multiplier stage is not used, pin 7 must be connected with pin 14 without mounting RR and CAC2. In this case CAC1 = 1/(6 28 x 30 x RDC).
2. The structure of this network shall copy the line impedance, in case multiplied by a factor K = 1... 10
3. K as fixed at note 2.
4 CINT can have the following values :

Fr. (Hz)	16/18	18/21	21/26	26/31	31/38	38/46	46/57	57/66
CINT (nF)	560	470	390	330	270	220	180	150

5. Ccon is necessary to work "without on/off hook detection-errors" during TTX-pulses.
6. CVSS, CVDD, can be shared with the others SLIC of the Line Card.

Figure 10 : Typical Application Schematic Diagram.

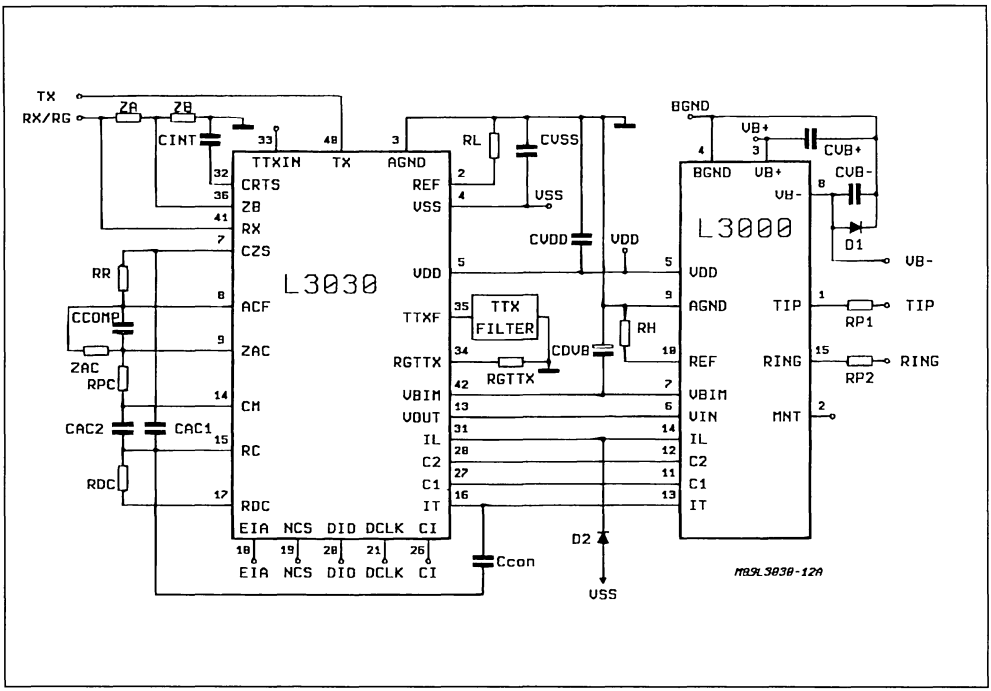
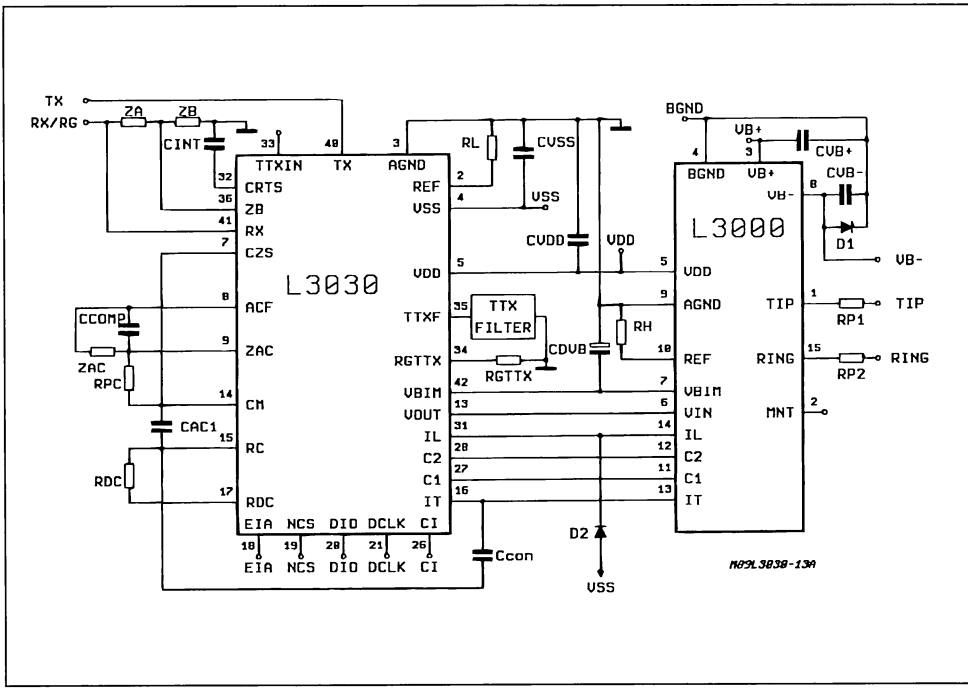


Figure 11 : Typical Application Schematic Diagram without Capacitor Multiplier.



ELECTRICAL CHARACTERISTICS (refer to the test circuits of the Fig.12 VDD = + 5V, VSS = – 5V, VB+ = + 72V, VB– = – 48V, Tamb = + 25°C, TTX FILT = 1KΩ).

STAND-BY

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Vls	Output Voltage at L3000 Terminals	Iline = 0mA	31.5		34.5	V
		Iline = 5mA	29.7		33	V
Ilcc	Short Circuit Current	DATA IN (note 1) 000X00X1	5		8.5	mA
Iot	On/off-hook Detection Threshold		5		8.5	mA
Vls	Symmetry to Ground	Iline = 0mA			.75	V

STAND BY DENIAL

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Ilcc	Short Circuit Current	DATA IN 000X00X0			2	mA

Note : 1. The data into the digital interface of L3030 are send in serial mode. The format of data is the following :
a) DATA IN : the bit at left side is BIT 0 of the writing word, while the bit at the right side is BIT 7.
b) DATA OUT : the bit at the left side is BIT0 of the reading word, while the bit at the right is BIT4.
When appear a symbol X, the value of the bit don't care.

ELECTRICAL CHARACTERISTICS (continued)

DC OPERATION - NORMAL BATTERY

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Vlo	Output Voltage at L3000 Terminals Ilim = 70mA Data in 10000010	Iline = 0mA	31.5		34.5	V
		Iline = 20mA	24.5		28.3	V
		Iline = 50mA	2.5		17.5	V
Ilim	Current Programmed Through the Digital Inter.		– 10%	Ilim	+ 10%	mA
Io	On-hook Detection Threshold				8	mA
If	Off-hook Detection Threshold		12			mA
Ilgk	Longitudinal Line Current with GK Detect		10	17	24	mA
Io	On-hook Detection Threshold				8	mA
If	Off-hook Detection Threshold		12			mA
Ilgk	Longitudinal Line Current with GK Detect.		10	17	24	mA

DC OPERATION - BOOST BATTERY

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Vlo	Output Voltage at L3000 Terminals	Iline = 0mA	86		95.6	V
		Iline = 20mA	68.6		81	V

AC OPERATION

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Ztx	Sending Output Impedance 4 Wire Side				10	Ω
Zrx	Receiving Input Impedance 4 Wire Side		100			kΩ
THD	Signal Distorsion at 2W and 4W Terminals				0.5	%
Rl	2W Return Loss	f = 300 to 500Hz	16.5			dB
		f = 500 to 3400Hz	20			dB
Thl	Trans Hybrid Loss	f = 300 to 3400Hz	16			dB
		f = 500 to 3000Hz	24			dB
Gs	Sending Gain	Vso = 0dBm f = 1020Hz				
		Norm. Polarity	– 0.24	0	+ 0.24	dB
		Rev. Polarity	– 0.24	0	+ 0.24	
Gsf	Sending Gain Flatness vs. Frequency	f = 300 to 3400Hz Respect to 1020Hz	– 0.1		+ 0.1	dB
Gsl	Sending Gain Linearity	fr = 1020Hz Vsoref = – 10dBm Vso = + 4 /– 40dBm		0.1		dB
		Vso = – 40 /– 50dBm		0.1		dB

ELECTRICAL CHARACTERISTICS (continued)

AC OPERATION (continued)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Gr	Receiving Gain	Vri = 0dBm f = 1020Hz				
		Norm. Polarity	– 0.23	0	+ 0.23	dB
		Rev. Polarity	– 0.23	0	+ 0.23	
Grf	Receiving Gain Flatness	f = 300 to 3400Hz Respect to 1020Hz	– 0.1		+ 0.1	dB
Grl	Receiving Gain Linearity	fr = 1020Hz Vriref = – 10dBm Vri = + 4 /– 40dBm		0.1		dB
		Vso = – 40 /– 50dBm		0.1		dB
Np4W	Psophometric Noise at 4W-Tx Terminals			– 75	– 70	dBmp
Np2W	Psophometric Noise at Line Terminals			– 75	– 70	* dBmp
SVRR	Supply Voltage Rejection Ratio Relative to VB–	f = 1000Hz			– 40	dB
		f = 3400Hz			– 36	
SVRR	Relative to Vdd	f = 3400Hz Vs = 100mVrms		– 26	– 23	dB
SVRR	Relative to VSS			– 32	– 30	dB
Ltc	Longitudinal to Transversal Conversion	f = 300 to 3400Hz Iline = 30mA ZML = 600Ω	49(*)	60		dB
Tlc	Transversal to Longitudinal Conversion		49(*)	60		dB

* Up to 52dB using selected L3000

AC OPERATION BOOST BATTERY

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Gs	Sending Gain	Vso = 0dBm f = 1020Hz				
		Norm. Polarity	– .61	– .16	+ .29	dB
		Rev. Polarity	– .61	– .16	+ .29	
Gr	Receiving Gain	Vri = 0dBm f = 1020Hz				
		Norm. Polarity	– .27	+ .08	+ .43	dB
		Rev. Polarity	– .27	+ .08	+ .43	
Np4W	Psophometric Noise at 4W-Tx Terminals			– 73	– 68	dBmp
Np2W	Psophometric Noise at line Terminals			– 73	– 68	dBmp

ELECTRICAL CHARACTERISTICS (continued)

AC OPERATION

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
SVRR	Supply Voltage Rejection Ratio Relative to VB+	V = 100mVrms f = 3400Hz			– 30	dB
SVRR	Relative to Vdd	f = 3400Hz Vs = 100mVrms			– 23	dB
SVRR	Relative to Vss				– 23	dB
Td	Propagation Time	Both Direction			40	µs
Tdd	Propag. Time Distortion				25	µs
Vttx	Line Voltage of Teletaxe Signal	Note 6	1.7		2.3	V
		Note 7	4.5		5.5	V
THD	Teletaxe Signal Harmonic Distortion	Ttx Filt = 0Ω @ 16Khz (note 8)			5	%
Zitt	Teletaxe Amplif. Input Impedance	Pin 33 of L3030	100			KΩ

RINGING PHASE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Vlr	Superimposed DC Voltage	Rloop > 100KΩ	20	24	30	V
		Rloop = 1KΩ	18	22	28	V
Vacr	Ringing Signal at Line Termin.	Rloop = 1KΩ + 1µF	57			Vrms
If	DC Off-hook Det. Threshold		1.5		3.5	mA
Ilim	Current Limit.		85		130	mA
Vrs	Ringing Simmetry				2	Vrms
THDr	Ringing Signal Distortion	Vac = 0.285Vrms fRING = 30Hz			5	

RINGING PHASE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Zir	Ringing Amplif. Input Impedance	Pin 41 of L3030	100			KΩ
Vrr	Residual of Ringing Signal at TX Output				600	mV
Trt	Ring Trip Detection Time	fring = 16Hz T = 1/fring	(1T)		125 (2T)	ms
Toh	Off-hook Status Delay after the Ringing Stop				125 (2T)	ms
Trs	Cut off of Ringing	Ring Trip not Confirmed			188 (3T)	ms

Notes : 6 The configuration of data sent to device change, every 100mS, from - 1100X010 - to - 1000X010 -
7. The configuration of data sent to device change, every 100mS, from - 1101X010 - to - 1001X010 -
8. Error generated by ttx filt ≠ 0 ohm, on the output teletax amplitude is
err% = 100 x (1 + A) x B/C
where
A = 10 Kohm/RGTTX[Kohm]
B = TTXFILT[Kohm]
C = (TTXFILT[Kohm] + 1 Kohm)
for example 10 ohm means err% = 2%.

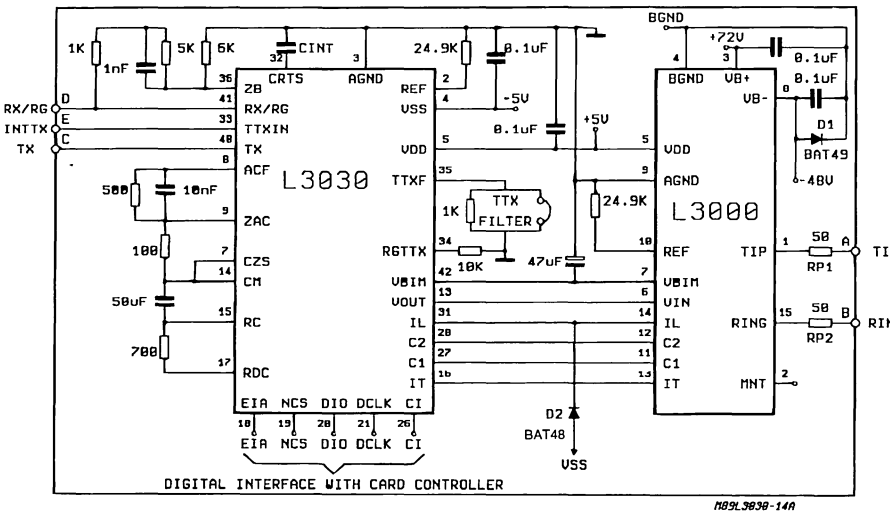
ELECTRICAL CHARACTERISTICS (continued)

SUPPLY CURRENT

Symbol	Parameter		Min.	Typ.	Max.	Unit
IDD	Positive Supply Current NCS = 1	Stand-by		16.3	20.9	mA
		Conversation (NB/BB)		26.4	33	mA
		Ringing		18	23	mA
ISS	Negative Supply Current NCS = 1	Stand-by		9	12	mA
		Conversation (NB/BB)		18	23	mA
		Ringing		9	12	mA
I_{BAT-}	Negative Battery Supply Current	Stand-by		2.9	4	mA
	Line Current = 0mA	Conversation NB		9.8	12	mA
		Conversation BB		13	16	mA
		Ringing		26	28.5	mA
I_{BAT+}	Positive Battery Supply Current	Stand by		10	15	µA
	Line Current = 0mA	Conversation NB		10	15	µA
		Conversation BB		8	10	mA
		Ringing		16	18.5	mA

NB = Normal Battery
BB = Boosted Battery

Figure 12 : Slic Test Circuit Schematic.



APPENDIX

SLIC TEST CIRCUITS

Referring to the test circuit reported at the end of each SLIC data sheet here below you can find the proper configuration for each measurement.

In particular : A-B : Line terminals

C : TX sending output on 4W side

D : RX receiving input on 4W side

E : TTX teletaxe signal input

R_{GIN} : low level ringing signal input.

TEST CIRCUITS

Figure 1 : Symmetry to Ground.

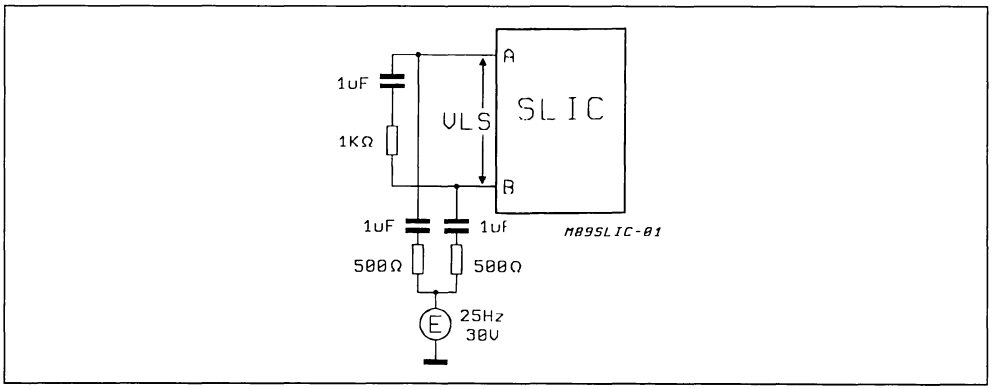
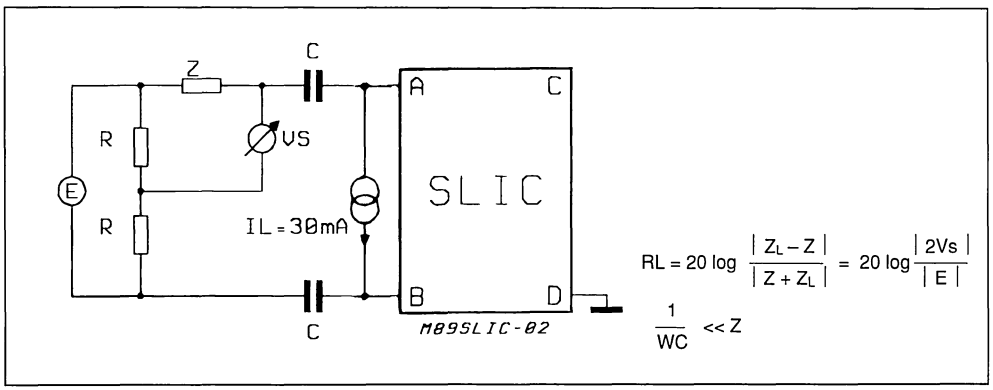


Figure 2 : 2W Return Loss.



TEST CIRCUITS (continued)

Figure 3 : Trans-hybrid Loss.

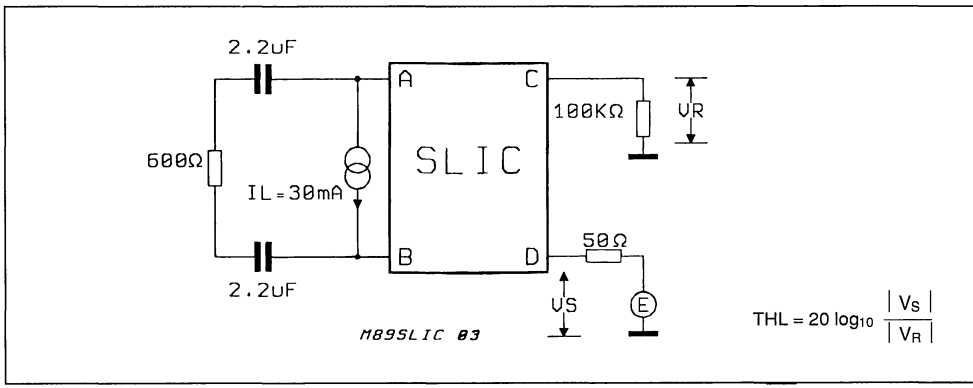


Figure 4 : Sending Gain.

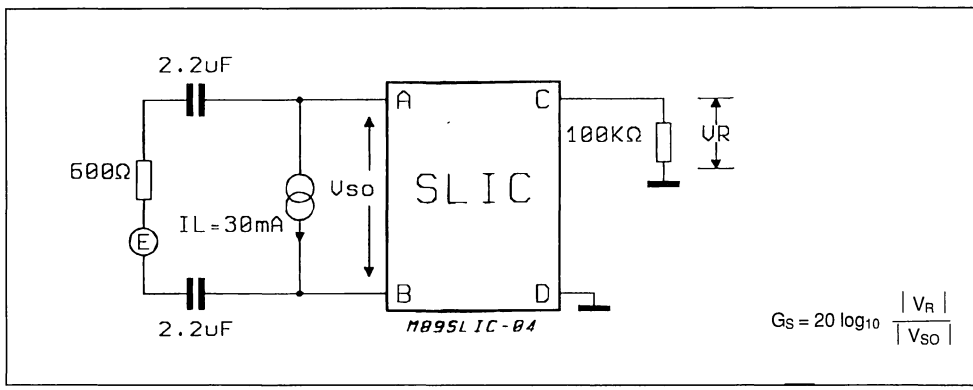
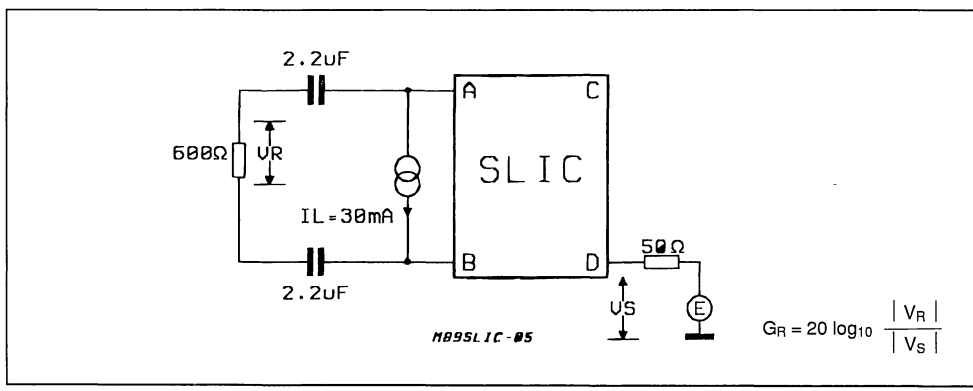


Figure 5 : Receiving Gain.



TEST CIRCUITS (continued)

Figure 6 : SVRR Relative to Battery Voltage VB–.

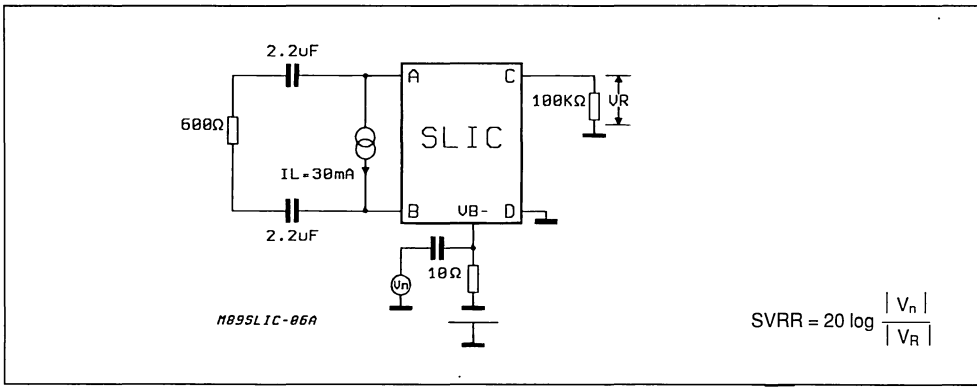


Figure 7 : Longitudinal to Transversal Conversion.

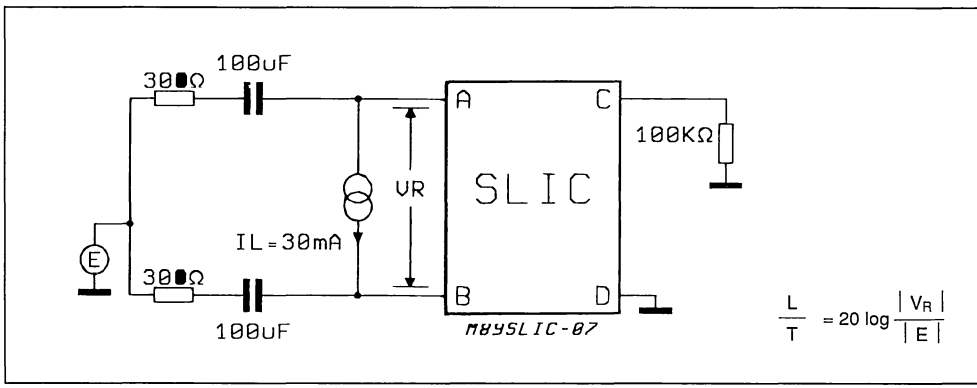
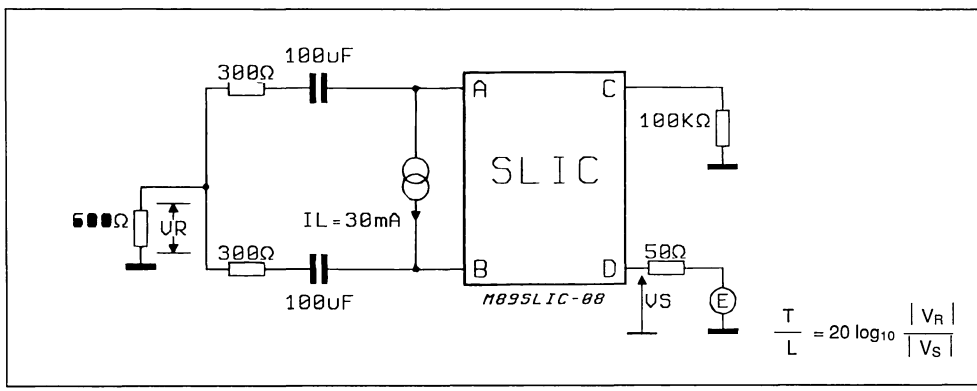


Figure 8 : Transversal to Longitudinal Conversion.



TEST CIRCUITS (continued)

Figure 9 : TTX Level at Line Terminals.

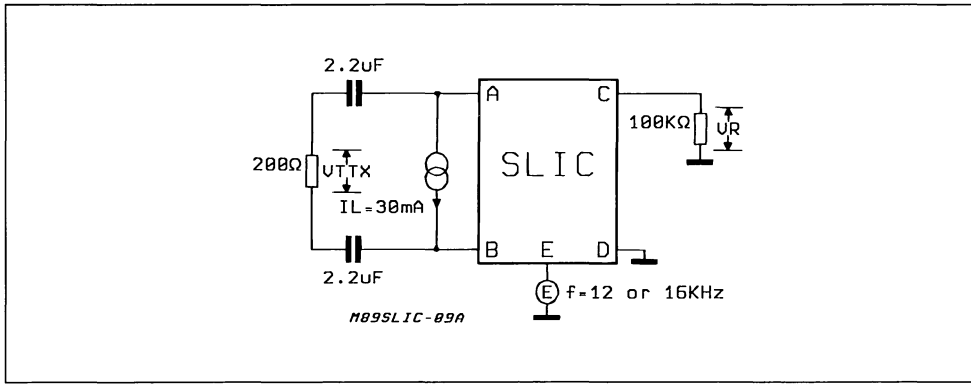
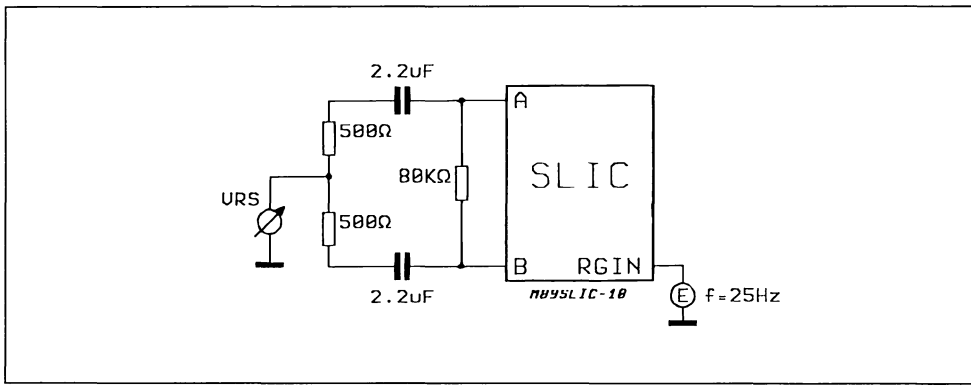


Figure 10 : Ringing Simmetry.



SGS-THOMSON MICROELECTRONICS

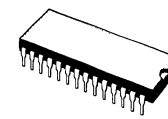
L3000 L3090

SUBSCRIBER LINE INTERFACE CIRCUIT KIT

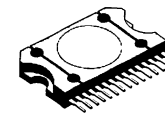
- PROGRAMMABLE DC FEEDING RESISTANCE and LIMITING CURRENT (42/62mA)
- FOUR OPERATING MODES : POWER DOWN, STAND-BY, CONVERSATION, RINGING
- SIGNALLING FUNCTION (off-hook/GND-Key)
- QUICK OFF-HOOK DETECTION IN CVS FOR LOW DISTORTION (< 1 %) DIAL PULSE DETECTION
- HYBRID FUNCTION
- RINGING GENERATION WITH QUASI ZERO OUTPUT IMPEDANCE, ZERO CROSSING INJECTION (no ext. relay needed) and RING TRIP DETECTION
- AUTOMATIC RINGING STOP WHEN OFF-HOOK IS DETECTED
- PARALLEL LATCHED DIGITAL INTERFACE (5 pins)
- LOW NUMBER of EXTERNAL COMPONENTS WITH STANDARD TOLERANCE ONLY : 9 1 % RESISTORS and 5 10-20 % CAPACITORS (for 600 ohm appl.)
- POSSIBILITY TO WORK ALSO WITH HIGH COMMON MODE CURRENTS
- GOOD REJECTION OF THE NOISE ON BATTERY VOLTAGE (20 dB at 10 Hz ; 40 dB at 1 KHz)
- INTEGRATED THERMAL PROTECTION

This kit is fabricated using a 140 V Bipolar technology for L3000 and a 12 V Bipolar I2L technology for L3090.

This kit is specially suitable to Private Automatic Branch Exchange (PABX).



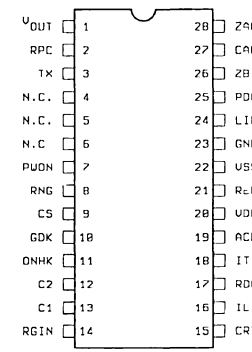
DIP28



FLEXIWATT 15

ORDER CODES : L3090 (DIP28)
L3000 (FLEXIWATT)

PIN CONNECTION



DESCRIPTION

The SLIC KIT (L3000/L3090) is a set of solid state devices designed to integrate many of the functions needed to interface a telephone line. It consists of 2 integrated devices ; the L3000 line interface circuit and the L3090 control unit.

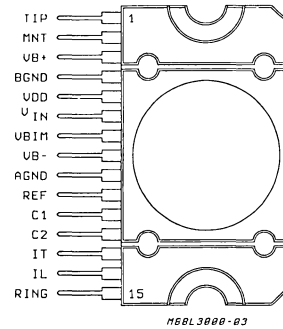
The kit implements the main features of the BORSHT functions :

- Battery feed (balance mode)
- Ringing
- Signalling
- Hybrid

The SLIC KIT injects the ringing signal in balanced mode and requires a positive supply voltage of typically + 72 V to be available on the subscriber card.

The L3000/L3090 KIT generates the ringing signal internally, avoiding the requirement for expensive external circuitry. A low level 1.5 V_{rms} input is required. (This can be provided by the combo).

PIN CONNECTION (continued)



ABSOLUTE MAXIMUM RATING

Symbol	Parameter	Value	Unit
V_b-	Negative Battery Voltage	– 80	V
V_b+	Positive Battery Voltage	80	V
$\|V_b\text{-}\| + \|V_b\text{+}\|$	Total Battery Voltage	140	V
V_{dd}	Positive Supply Voltage	+ 5.5	V
V_{ss}	Negative Supply Voltage	– 5.5	V
$\|V_{agnd}-V_{bgnd}\|$	Max Voltage Between Analog Ground and Battery Ground	5	V
T_j	Max Junction Temperature	+ 150	°C
T_{stg}	Storage Temperature	– 55 to + 150	°C

THERMAL DATA

L3000 HIGH VOLTAGE

R_{thjc}	Max Resistance Junction to Case	4	°C/W
R_{thja}	Max Resistance Junction to Ambient	50	°C/W

L3090 LOW VOLTAGE

R_{thja}	Max Resistance Junction to Ambient	80	°C/W

OPERATING RANGE

Symbol	Parameter	Min.	Typ.	Max.	Unit
T_{oper}	Operating Temperature Range	0		70	°C
V_b-	Negative Battery Voltage	– 70	– 48	–24	V
V_b+	Positive Battery Voltage	0	+ 72	+ 75	V
$\|V_b\text{-}\| + \|V_b\text{+}\|$	Total Battery Voltage		120	130	V
V_{dd}	Positive Supply Voltage	+ 4.5		+ 5.5	V
V_{ss}	Negative Supply Voltage	– 5.5		– 4.5	V
I_{max}	Total Line Current ($I_L + I_T$)			85	mA

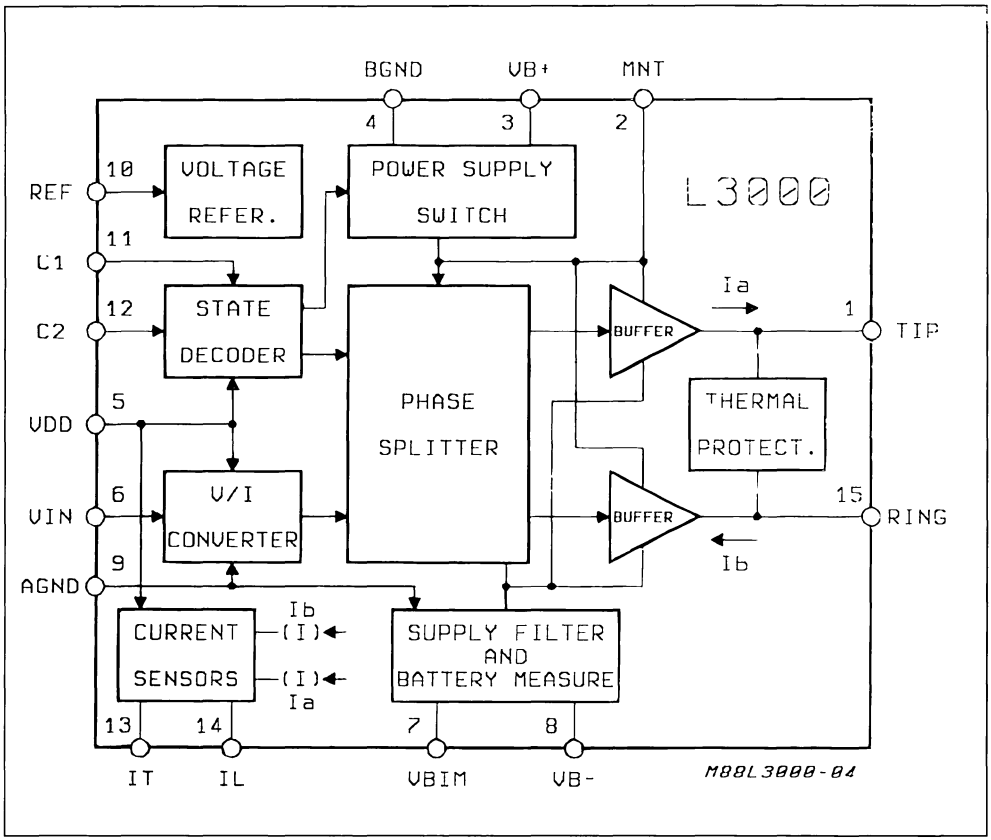
PIN DESCRIPTION (L3000)

N°	Name	Description
1	TIP	A line termination output with current capability up to 100 mA (I_a is the current sourced from this pin).
2	MNT	Positive Supply Voltage Monitor
3	V_B+	Positive Battery Supply Voltage
4	BGND	Battery Ground Relative to the V_B+ and the V_B- supply Voltages. It is also the reference ground for TIP and RING signals.
5	V_{DD}	Positive Power Supply + 5 V
6	VIN	2 Wire unbalanced Voltage Input.
7	VBIM	Output Voltage without current capability, with the following functions : – give an image of the total battery voltage scaled by 40 to the low voltage part. – filter by an external capacitor the noise on V_B-
8	V_B-	Negative Battery Supply Voltage
9	AGND	Analog Ground. All input signals and the V_{DD} supply voltage must be referred to this pin.
10	REF	Voltage reference output with very low temperature coefficient. The connected resistor sets internal circuit bias current.
11	C1	Digital signal input (3 levels) that defines device status with pin 12.
12	C2	Digital signal input (3 levels) that defines device status with pin 11.
13	I_T	High precision scaled transversal line current signal. $I_T = \frac{I_a + I_b}{100}$
14	IL	Scaled longitudinal line current signal. $IL = \frac{I_a - I_b}{100}$
15	RING	B line termination output with current capability up to 100 mA (I_b is the current sunk into this pin).

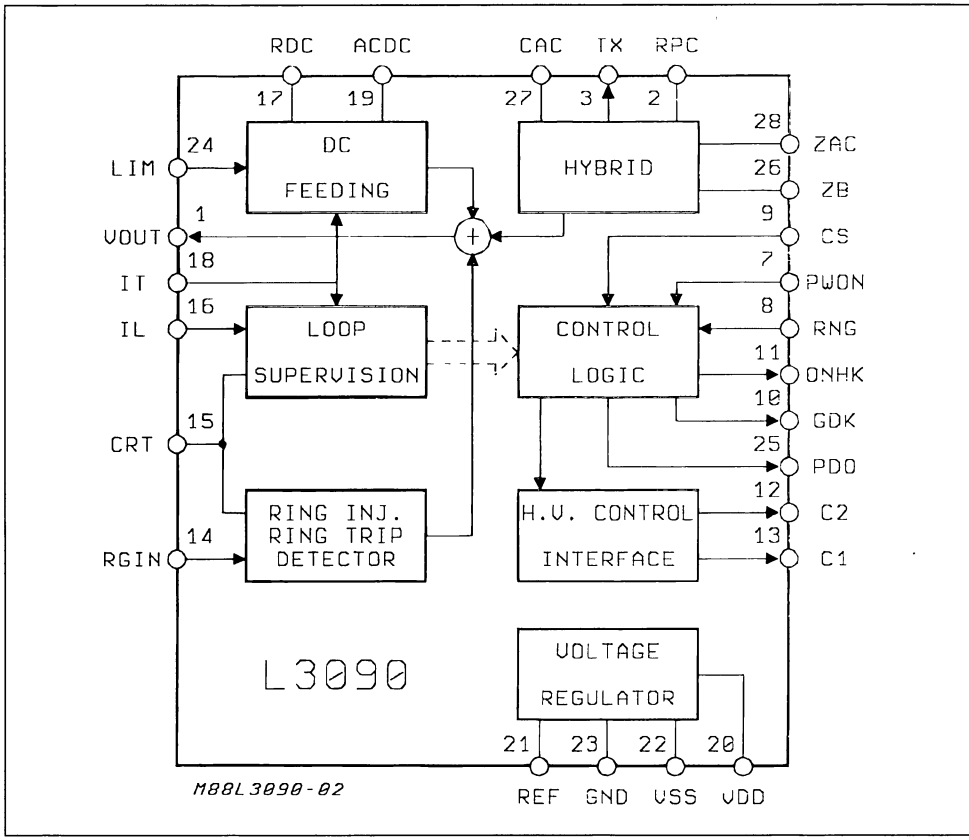
PIN DESCRIPTION (L3090)

N°	Name	Description
1	VOUT	Two wire unbalanced output carrying out the following signals reduced by 40 1) DC voltage to perform the proper DC characteristic. 2) Ringing Signal 3) Voice Signal
2	RPC	AC Line Impedance Adjustment. Protection Resistances Compensation.
3	TX	Transmit Amplifier Output
4	NC	Not Connected. This pin is connected to an internal circuitry and should not be used as a tie-point for external circuitry.
5	NC	Not Connected. This pin is connected to an internal circuitry and should not be used as a tie–point for external circuitry.
6	NC	Not Connected.This pin is connected to an internal circuitry and should not be used as a tie-point for external circuitry.
7	PWON	Power on/power off Input. This input is part of digital interface. Loaded when CS is low.
8	RNG	Ring Enable Input. This input is part of the digital interface. Loaded when CS is low.
9	CS	Chip Select Input
10	GDK	Ground Key Output. Enabled by CS low.
11	ONHK	On Hook/off Hook Output. Enabled by CS low.
12	C2	State Control Signal 2
13	C1	State Control Signal 1. Combination of C1 and C2 define operating mode of the high voltage part.
14	RGIN	Low Level Ringing Signal Input.
15	CRT	Ring Trip Detection
16	IL	Longitudinal Line Current Input $IL = \frac{I_a - I_b}{100}$
17	RDC	DC Feeding System
18	IT	Transversal Line Current Input $IT = \frac{I_a + I_b}{100}$
19	ACDC	AC – DC Feedback Input
20	VDD	Positive Supply Voltage, + 5 V
21	REF	Bias Setting Pin
22	VSS	Negative Supply Voltage, – 5 V
23	GND	Analog and Digital Ground
24	LIM	Limiting Current Selection Input
25	PDO	Power Down Output. Driving the high voltage part L3000 through its bias resistor RH.
26	ZB	TX Amplifier Negative Input. Performing the two to four wire conversion.
27	CAC	AC Feedback Input
28	ZAC	AC Line Impedance Synthesis

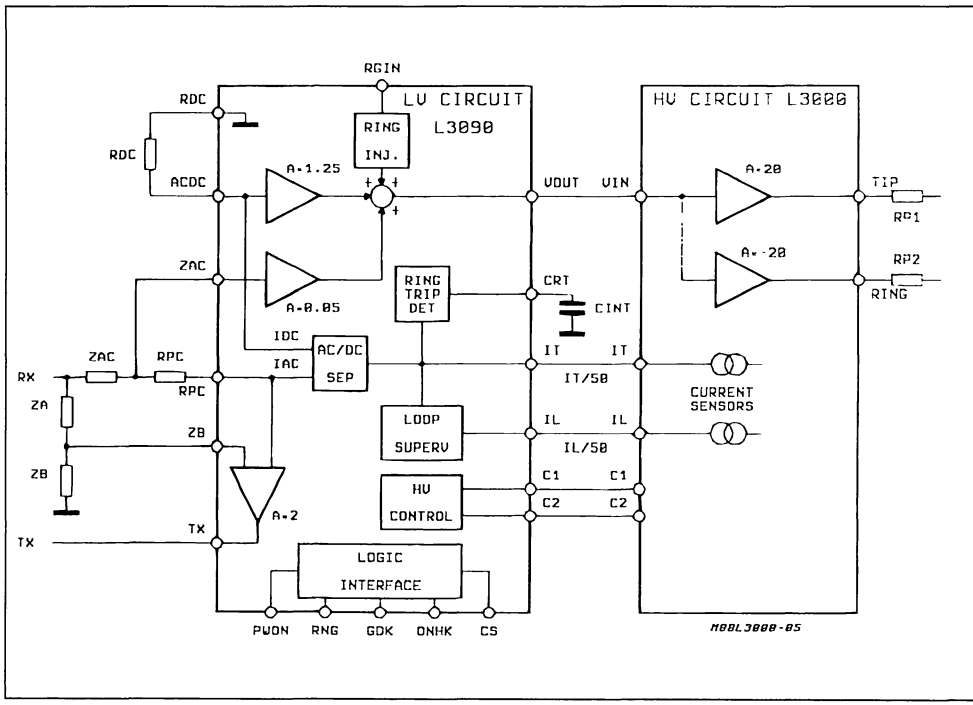
L3000 BLOCK DIAGRAM



L3090 BLOCK DIAGRAM



FUNCTIONAL DIAGRAM



FUNCTIONAL DESCRIPTION

L 3000 - HIGH VOLTAGE CIRCUIT

The L3000 line interface provides a battery feeding for telephone lines and ringing injection. The IC contains a state decoder that under external control can force the following operational modes : stand-by, conversation and ringing.

In addition Power down mode can be forced connecting the bias current resistor to VDD.

Two pins, I_L and I_T, carry out the information concerning line status which is detected by sensing the line current into the output stage.

The L3000 amplifies both the AC and DC signals entering at pin 6 (VIN).

Separate grounds are provided :

- Analog ground as a reference for analog signals
- Battery ground as a reference for the output stages

L3090 - LOW VOLTAGE CIRCUIT

The L3090 Low Voltage Control Unit controls the L3000 line interface module providing set up data to set line feed characteristics and to inject ringing. An on chip digital parallel interface allows a microprocessor or a second generation COMBO as the TS5070 to control all the operations.

L3090 defines working states of line interface and also informs the controller about line status.

WORKING STATES OF THE KIT

In order to carry out the different possible operations, the SLIC kit has several different working states. Each state is defined by the voltage respectively applied by pins 12 and 13 of L3090 to the pins 12 and 11 of L3000.

Three different voltage levels (5, 0, + 5) are available at each connection, so defining nine possible states as listed in tab. 1.

Appropriate combinations of two pins define three of the four possible status of the kit, that are :

a) Stand-by (SBY)

b) Conversation (CVS)

c) Ringing (RING)

Table 1.

		Pin 12 of L3090 / Pin 12 of L3000		
		+ 5	0	– 5
Pin 13 of L3090	+ 5	Stand–by	Conversation	Not Used
———	0	Not Used	Not Used	Not Used
Pin 11 of L3000	– 5	Not Used	Ringing	Not Used

The fourth status, Power down (PD), is set by the output pin PDO of the L3090.

The main difference between Stand-by and Power down is that in SBY the power consumption on the voltage battery VB– (–48 V) is reduced but the SLIC can still recognize yet the On hook/Off hook status. In PD the power consumption on VB– is reduced to zero, but none operation can be performed by the SLIC.

The SBY status should be used when the telephone is in On hook and PD status only in emergency condition when it is mandatory to cut any possible dissipation but no operation are requested.

OPERATING MODES

STAND-BY (SBY) MODE

In this mode (PWON=OV RNG=OV) the bias currents of both L3000 and L3090 are reduced as only some parts of the two circuits are completely active, control interface and current sensors among them. The current supplied to the line is limited at 12 mA, and the slope of the DC characteristic corresponds to 2xRFS.

The AC characteristic in Stand-by corresponds to a low impedance (2xRP).

In Stand-by mode the line voltage polarity is just in direct condition, that is the TIP wire more positive than the RING one.

When the SLIC is in Stand-by mode, the power dissipation of L3000 does not exceed 200 mW (from 48 V) eventually increased of a certain amount if some current is flowing into the line.

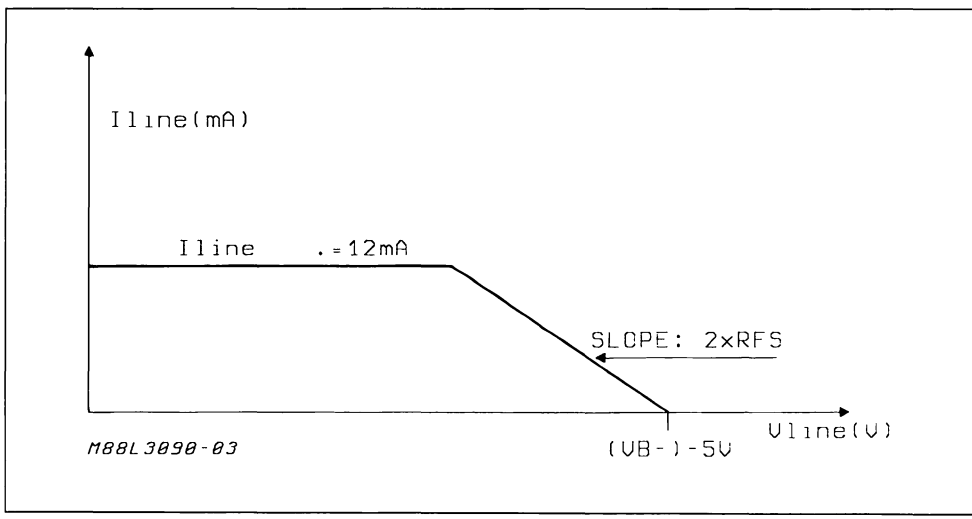
The power dissipation of the L3090 in the same condition is typically 60 mW.

CONVERSATION (CVS) MODE

This operating mode is set by the control processor when the Off hook condition has been recognized (PWON=+5V RNG=0V).

As far as the DC Characteristic is concerned two different feeding conditions are present :

Figure 1 : DC Characteristic in Stand-by Mode.



a) Current limiting region : the DC impedance of the SLIC is very high (> 20 KΩ) and therefore the system works like a current generator. The input pin LIM of the L3090 selects the value of the limiting current : 62 mA (LIM=0V) or 42 mA (LIM=+5V)

b) A standard resistive feeding mode : the characteristic is equal to a battery voltage (VB–) minus 5 V, in series with a resistor, whose value is set by external components (see external component list of L3090).

Switching between the two regions is automatic without discontinuity, and depends on the loop resistance. Fig. 2 shows the DC characteristic in conversation mode.

Fig. 3 shows the line current versus loop resistance for two different battery values and RFS = 200 Ω.

The allowed maximum loop resistance depends on the values of the battery voltage (VB), on the RFS and on the value of the longitudinal current (I_{GDK}). With a battery voltage of 48 V, RFS = 200 Ω and I_{GDK} = 0 mA, the maximum loop resistance is over 3000 Ω and with I_{GDK} = 20 mA is about 2000 Ω (see Application Note on maximum loop resistance for L3000/L3090 SLIC KIT).

Figure 2 : DC Characteristic in Conversation Mode.

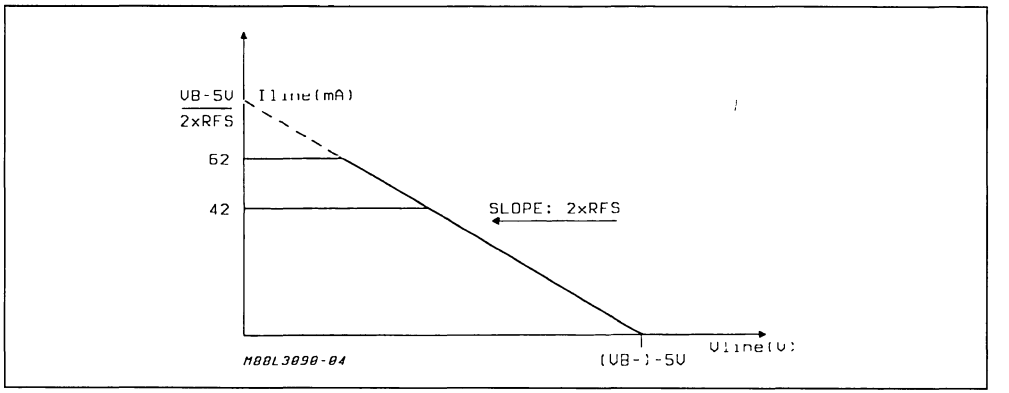
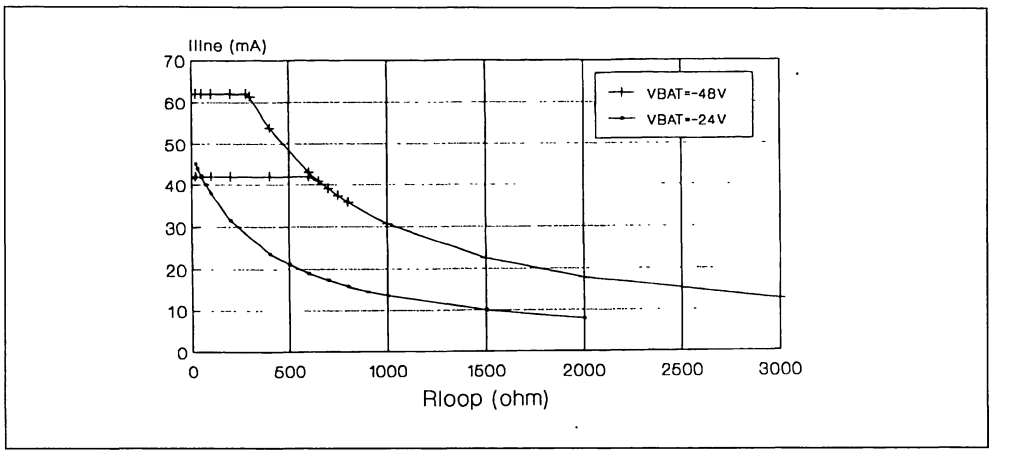


Figure 3 : Line Current Versus Loop Resistance - RFS = 200 Ω ; Limiting Currents : 42 ; 62 mA.



In conversation mode the AC impedance at the line terminals is synthetized by the external components ZAC and RP, according to the following formula :

$$ZML = \frac{ZAC}{25} + 2 \times RP$$

Depending on the characteristic of the ZAC network, ZML can be either a pure resistance or a complex impedance. This allows for ST SLIC to meet different standards as far as the return loss is concerned. The capacitor CCOMP guarantees stability to the system.

The two to four wire conversion is achieved by means of a circuit that can be represented as a Wheatstone bridge, the branches of which being :

1) The line impedance (Zline),

2) The SLIC impedance at line terminals (ZML),

3) The balancing network ZA connected between RX input and ZB pin of L3090,

4) The network ZB between ZB pin and ground that shall copy the line impedance.

It is important to underline that ZA and ZB are not equal to ZML and to Zline. They both must be multiplied by a factor in the range of 10 to 25, allowing use of smaller capacitors.

In conversation mode, the L3000 dissipates about 500 mW for its own operation. The dissipation related to the current supplied to the line shall be added, in order to get the total dissipation.

In the same condition the power dissipation of L3090 is typically 100 mW.

POWER DOWN MODE

In this mode (PWON=0V RNG=+ 5 V) the SLIC presents an high impedance to the line and cannot provide any line current.

The power dissipation from the battery voltage (VB) is equal to zero and the only function that the SLIC can perform is to recognize a command on PWON and RNG input pins and change its operating mode.

In this condition the power dissipation of the L3090 is typically 60 mW.

RINGING MODE

When the ringing function is selected by the control processor (PWON = + 5 V, RNG = + 5 V), a low level signal (1.5 Vrms) with a frequency in the range from 16 to 70 Hz, permanently applied to the L3090 (pin RGIN), is amplified and injected in balanced mode into the line through the L3000 with a super imposed DC voltage of 22 V.

This low level sinewave can be obtained also from COMBO connecting RGIN pin to RX COMBO output with a decoupling capacitor.

The first and the last ringing cycles are synchronized by the L3090 so that the ringing signal always starts and stops when the line voltage crosses zero.

When this mode is activated, the L3000 operates between the negative and the positive battery voltages typically – 48 V and + 72 V. The impedance to the line is just equal to the two external resistors (typ. = 60 Ω).

Ring trip detection is performed autonomously by the SLIC, without waiting for a command from the control processor, using a patented system which allows detection during a ringing burst ; when the off-hook condition is detected, the SLIC stops the ringing signal and forces the Conversation Mode.

In this condition, if CS = 0 V, the output pin ONHK goes to 0 V.

After the detection of the ONHK = 0, the Card Controller must set the SLIC in Conversation Mode to remove the internal latching of the On/Off hook information.

CONTROL INTERFACE BETWEEN THE SLIC AND THE CARD CONTROLLER

The SLIC states and functions are controlled by microprocessor or interface latches of a second generation combo through five wires that define a parallel digital interface.

The five pins of the digital interface have the following functions :

- Power on/off input (PWON)
- Ring enable input (RNG)
- Chip select input (CS)
- On hook/Off hook detection output (ONHK)
- Ground key detection output (GDK)

The two input pins PWON and RNG set the status of the SLIC as shown in the following Table.

The output pin ONHK is equal to 0 V when the line is in OFF hook condition (I_{line} 7,5 mA) and is equal to + 5 V when the line is in On hook condition (I_{line} 5,5 mA).

The output pin GDK monitors the ground key functions.

When I_{GDK} (longitudinal current) > 12 mA, pin GDK set to 0 V

		PWON PIN	
		0 V	+ 5 V
RNG PIN	0 V	Stand–by	Conversation
	+ 5 V	Power Down	Ringing

When I_{GDK} < 8 mA, pin GDK set to + 5 V

The longitudinal current (I_{GDK}) is defined as follows :

$$I_{GDK} = \frac{I_A - I_B}{2}$$

Where I_A is the current sourced from pin TIP and I_B is the current sunk into pin RING.

The CS input pin allows to connect the I/O pins of the digital interfaces of many SLIC together.

It is possible to do it because :

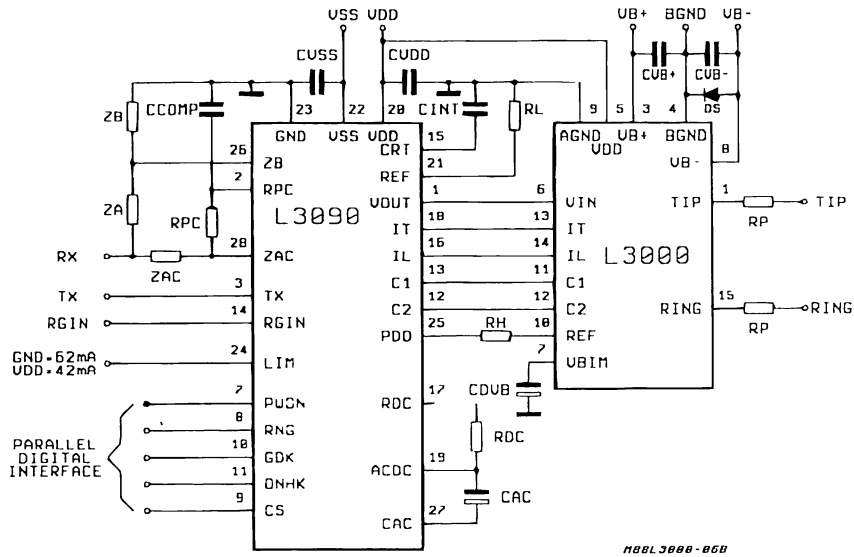
When the CS = + 5 V the output pins (ONHK, GDK) are in high impedance condition (>100 KΩ). The signals present at the input pins (PWON and RNG) are not transfered into the SLIC.

When the CS = 0 V the output pins change in function of the values of the line current (I_{line}) and the longitudinal current (I_{GDK}). The operating status of the SLIC are set by the voltage applied to the input pins.

The rising edge of the CS signal latches the signal applied to the input pins. The status of the SLIC will not change until the CS signal will be again equal to zero.

See timings fig. 5 & 6.

Figure 4 : Typical Application Circuit.



EXTERNAL COMPONENTS LIST

To set up the SLIC kit into operation, the following parameters have to be defined :

- The DC feeding resistance RFS, defined as the resistance of each side of the traditional feeding system (most common value for RFS are 200, 400 or 500).
- The AC input/output SLIC impedance at line terminals, ZML, to which the return loss measurement is refered. It can be real (typically 600Ω) or complex.
- The equivalent AC impedance of the line Zline used for evaluation of the trans-hybrid loss (2/4 wire conversion). It is usually a complex impedance.
- The frequency of the ringing signal Fr (SLIC can work with this frequency ranging from 16 to 68 Hz).
- The value of the two resistors RP in series with the line terminals ; main purpose of the a.m. resistors is to allow primary protection to fire. A minimum value of 30Ω for each side is suggested.

With these assumptions, the following component list is defined :

EXTERNAL COMPONENT LIST FOR THE L3000

Component		Involved Parameter or Function
Ref	Value	
RH	24.9 Kohms ± 2 %	Bias Resistor
RP	30 to 100 ohm	Line Series Resistor
CDVB	47 uF – 20 WV ± 20 %	Battery Voltage Rejection
CVB + (note 1)	0,1 uF – 100 WV ± 20 %	Positive Battery Filter
CVB – (note 1)	0, 1 uF – 100 WV ± 20 %	Negative Battery Filter
DS (note 1)	BAT 49	Protective Shottky Diode

EXTERNAL COMPONENT LIST FOR THE L3090

Component		Involved Parameter or Function
Ref	Value	
CVSS	0,1 uF – 15 WV (note 1)	Negative Supply Voltage Filter
CVDD	0,1 uF – 15 WV	Positive Supply Voltage Filter
CAC	47 uF – 10 WV ± 20 %	AC Path Decoupling
ZAC	25 x (ZML – 2xRP)	2 Wire AC Impedance
CCOMP	$\frac{1}{6.28 \times 30000 \times ZML \times 25}$	AC Loop Compensation
RPC	25 x (2xRP)	R_P Insertion Less Compensation
RDC	2x (RFS – RP)	DC Feeding Resistor
RL	63.4 Kohms ± 1 %	Bias Resistor
ZA	K x ZML (note 2)	SLIC Impedance Balancing Network
ZB	(K x Zline) // ($\frac{25}{K}$ x CCOMP) (note 3)	Line Impedance Balancing Network
CINT	(note 4)	Ring Trip Detection Time Constant

Notes : 1. In most applications these components can be shared between all the SLIC's on the Subscriber Card.
2 The structure of this network shall copy the SLIC output impedance multiplied by a factor K=10 to 25.
3. The structure of this network shall copy the line impedance, Z line, multiplied by a factor K=10 to 25 and compensate the effect of CCOMP on transhybrid rejection.
4 The CINT value depends on the ringing frequency Fr .

Fr [Hz]	16/18	19/21	22/27	28/32	33/38	39/46	47/55	56/68
CINT [nF]	680	560	470	390	330	270	220	180

The CINT value can be optimized experimentally for each application choosing the lower value that in correspondance of the lower ringing frequency, the minimum line lenght and the higher number of ringers doesn't produce false off-hook detection.

ELECTRICAL CHARACTERISTICS

(VDD = + 5 V ; VSS = 5 V ; VB + = + 72 V ; VB – = – 48 V ; Tamb = + 25 °C)

STANDBY

Symbol	Parametrer	Test Conditions	Min.	Typ.	Max.	Unit
VLS	Output Voltage at L3OOO Terminals	I Line = 0 mA		43		V
ILCC	Short Circuit Current		10		14	mA
Iot	Off–hook Detection Threshold		5.6		9.8	mA
Hys	Off–hook/On– hook Hysteresis		1.5		2.5	mA
Vls	Symmetry to Ground	I Line = 0 mA			.75	V

DC OPERATION – NORMAL BATTERY

Symbol	Parametrer	Test Conditions	Min.	Typ.	Max.	Unit
VLO	Output Voltage at L3000 Line Terminals	I Line = 0 mA		43		V
Ilim	Current programmed through the LIM Input	Pin 24 to + 5 V	38	42	46	mA
		Pin 24 to 0 V	56	62	68	mA
Iot	Off–hook Detection Threshold		5.6		9.8	mA
Hys	Off–hook/On–hook Hysteresis		1.5		2.5	mA
Ilgk	Longitudinal Line Current With GDK Detect		6.5		15	mA

SUPPLY CURRENT

Symbol	Parameter		Min.	Typ.	Max.	Unit
I_{DD}	Positive Supply Current CS = 1	Power Down Stand-by Conversation Ringing		6.0 7.8 13.2 12.8		mA mA mA mA
I_{SS}	Negative Supply Current CS = 1	Power Down Stand-by Conversation Ringing		5.4 5.4 8.2 8.2		mA mA mA mA
I_{BAT-}	Negative Battery Supply Current Line Current = 0mA	Power Down Stand-by Conversation Ringing		0 2.9 9.8 26	 4 12 28.5	mA mA mA mA
I_{BAT+}	Positive Battery Supply Current Line Current = 0mA	Power Down Stand-by Conversation Ringing		0 10 10 16	 15 15 18.5	mA µA µA mA

AC OPERATION

Symbol	Parametrer	Test Conditions	Min.	Typ.	Max.	Unit
Ztx	Sending Output Impedance on TX				15	ohm
THD	Signal Distortion at 2 W and 4 W Terminals	Vtx = 0 dBm@ 1020 Hz			0.5	%
Rl	2 W Return Loss	f = 300 to 3400 Hz	20			dB
Thl	Transhybrid Loss	f = 300 to 3400 Hz	24			dB
Gs	Sending Gain	Vso = 0 dBm f = 1020 Hz	– 0.25		+ 0.25	dB
Gsf	Sending Gain Flatness vs. Frequency	f = 300 to 3400 Hz respect to 1020 Hz	– 0.1		+ 0.1	dB
Gl	Sending Gain Linearity	fr = 1020 Hz Vsoref = – 10 dBm Vso = + 4 / – 40 dBm	– 0.1		+ 0.1	dB
Gr	Receiving Gain	Vri = 0 dBm f = 1020 Hz	– 0.25		+ 0.25	dB
Grf	Receiving Gain Flatness	f = 300 to 3400 Hz Respect to 1020 Hz	– 0.1		+ 0.1	dB
Grl	Receiving Gain Linearity	fr = 1020 Hz Vriref = – 10 dBm Vri = + 4 / – 40 dBm	– 0.1		+ 0.1	dB
Np4W	Psophomet. Noise 4 W– Tx Terminals		– 70	– 75		dBmp
NP2W	Psophomet. at Line Terminals		– 70	– 75		dBmp
SVRR	Supply Voltage Rejection Ratio Relative to VB–	f = 10 Hz Vn = 0.7 Vrms		– 20		dB
		f = 1 KHz Vn = 0.7 Vrms			– 40	dB
		f = 3.4 KHz Vn = 0.7 Vrms			– 36	dB
Ltc	Longitudinal to Transversal Conversion	f = 300 to 3400 Hz I Line = 30 mA ZML = 600 ohms	49 (*)	60		dB
Tlc	Transversal to Longitudinal Conversion		49	60		dB

(*) : up to 52dB using selected L3000

RINGING PHASE

Symbol	Parametrer	Test Conditions	Min.	Typ.	Max.	Unit
Vlr	Superimposed DC Voltage	Rloop > 100 Kohms	19		29	V
		Rloop = 1 Kohm	17		27	V
Vacr	Ringing Signal at Line Terminal	Rloop > 100 kOhms V_{RGIN} = 1.5 Vrms/30 Hz	56.0			Vrms
		Rloop = 1 Kohm +1 uF V_{RGIN} = 1.5 Vrms/30 Hz	56.0			Vrms
If	DC Off–hook Det. Threshold			5.5		mA
Ilim	Output Current Capability		85		130	mA
V_{rs}	Ringing Symmetry				2	Vrms
THDr	Ringing Signal Distorsion				5	%
Zir	Ringing Amplicat. Input Impedance	L3090's Pin RGIN	50			Kohm
Vrr	Residual of Ringing Signal at Tx Output				100	mVrms
Trt	Ring Trip Detection Time	fring = 25 Hz (T = 1/fring) CINT = 470 nF		120 (3T)		ms
Toh	Off–hook Status Delay After the Ringing Stop				50	us

DIGITAL INTERFACE ELECTRICAL CHARACTERISTICS

(VDD = + 5 V ; VSS = – 5 V ; Tamb = 25 °C)

STATIC ELECTRICAL CHARACTERISTICS

Symbol	Parametrer	Test Conditions	Min.	Typ.	Max.	Unit
Vil	Input Voltage at Logical "0"	Pins CS PWON RNG LIM	0		0.8	V
Vih	Input Voltage at Logical "1"		2,0		5	V
Iil	Input Current at Logical "0"	Vil = 0 V			200	uA
Iih	Input Current at Logical "1"	Vih = 5 V			100	uA
Vol	Output Voltage at Logical "0"	Pins ONHK GDK Iout = – 1 mA			0.4	V
Voh	Output Voltage at Logical "1"	Iout = 1 mA	2.4			V
Ilk	Tristate Leak. Current	CS = "1"			10	uA

DYNAMIC ELECTRICAL CHARACTERISTICS

Symbol	Parametrer	Test Conditions	Min.	Typ.	Max.	Unit
Tsd	PWON, RNG Set up Time to + Edge CS		400			nS
Thd	PWON, RNG Hold Time to + Edge CS		500			nS
Tww	CS Impulse Width (writing Op.)		800			nS
Thv	ONHK, GDK Data Out to "0" CS Delay				600	nS
Tvh	ONHK, GDK High Imped. to "1" CS Delay				600	nS
Twr	CS Impulse Width (writing Op.)		800			nS

Figure 5 : Writing Operation Timing (controller to slic).

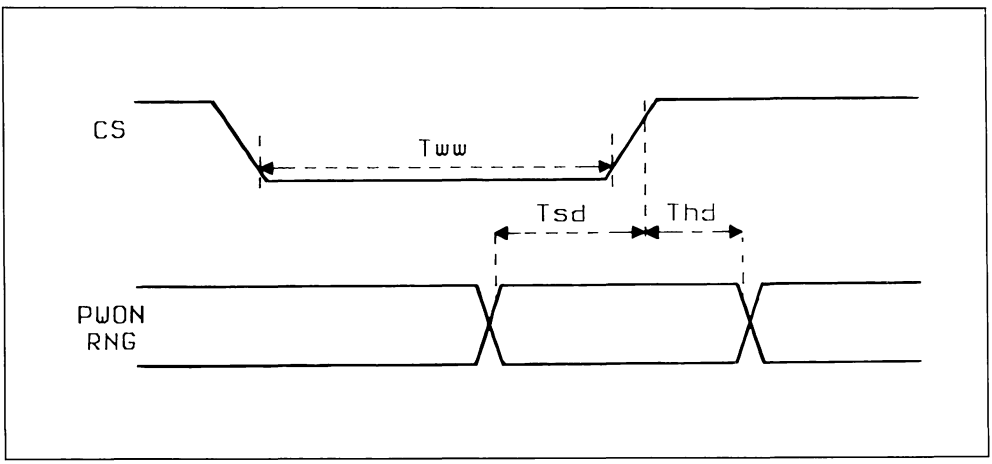


Figure 6 : Reading Operation Timing (from slic to controller).

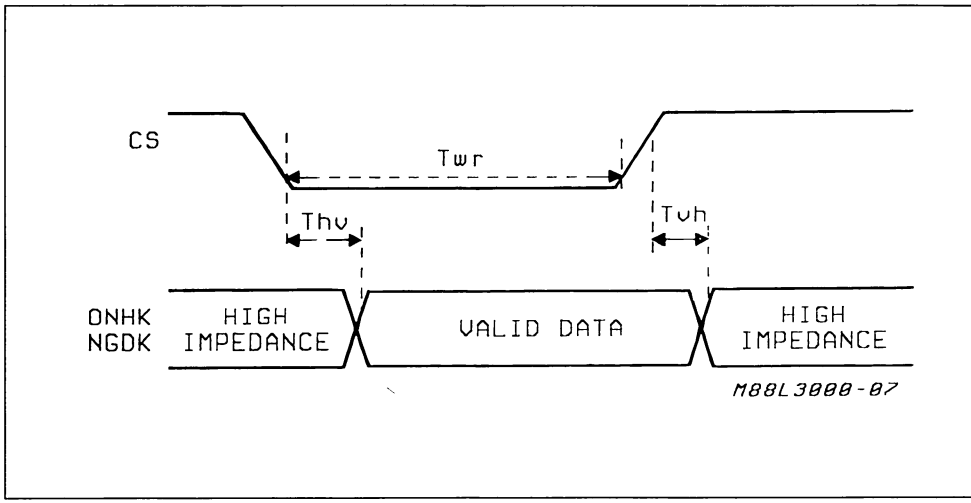
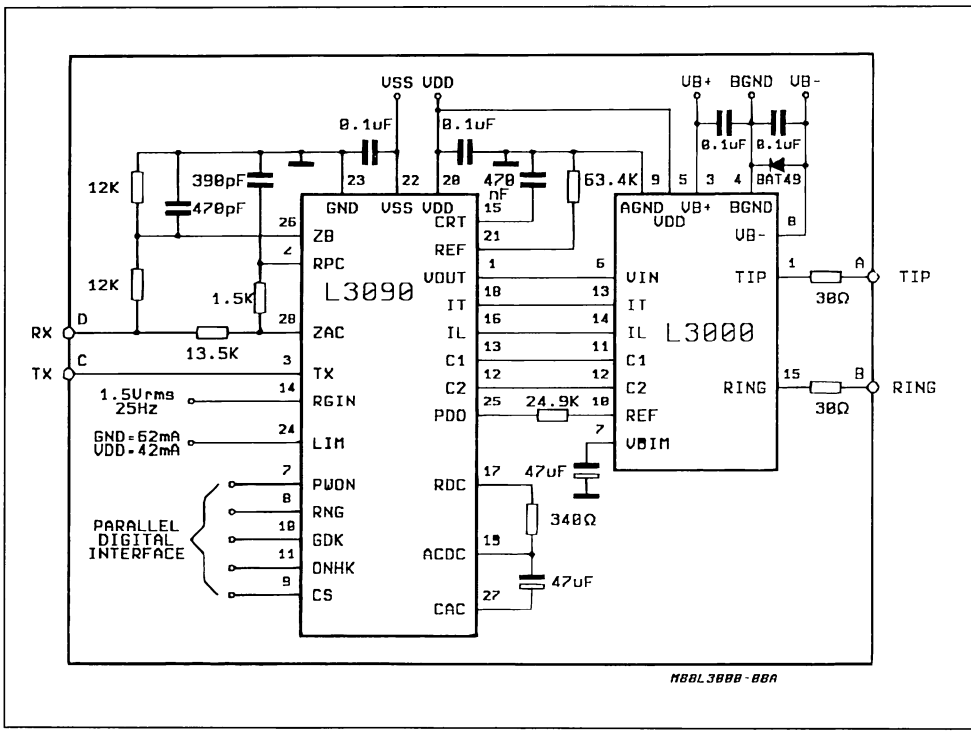


Figure 7 : Test Circuit.



A, B, C, D are test reference points used driving testing.

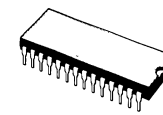
SGS-THOMSON MICROELECTRONICS

L3000 L3091

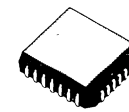
SUBSCRIBER LINE INTERFACE CIRCUIT KIT

ADVANCE DATA

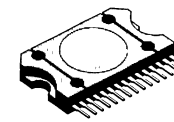
- PROGRAMMABLE DC FEED RESISTANCE AND LIMITING CURRENT (25/42/62mA)
- LOW ON-HOOK POWER DISSIPATION (70mW typ)
- SIGNALLING FUNCTION (off-hook/GND-Key)
- QUICK OFF-HOOK DETECTION IN CVS FOR LOW DISTORTION (< 1%) DIAL PULSE DETECTION
- HYBRID FUNCTION
- RINGING GENERATION WITH QUASI ZERO OUTPUT IMPEDANCE, ZERO CROSSING INJECTION (no ext. relay needed) AND RING TRIP DETECTION
- AUTOMATIC RINGING STOP WHEN OFF-HOOK IS DETECTED
- TEST MODE ALLOWS LINE LENGHT MEASUREMENT
- PARALLEL LATCHED DIGITAL INTERFACE
- LOW NUMBER OF EXTERNAL COMPONENTS WITH STANDARD TOLERANCE ONLY : 9 1% RESISTORS AND 5 10-20% CAPACITORS (for 600 ohm appl.)
- POSSIBILITY TO WORK ALSO WITH HIGH COMMON MODE CURRENTS
- GOOD REJECTION OF THE NOISE ON BATTERY VOLTAGE (20dB at 10Hz ; 40dB at 1KHz)
- INTEGRATED THERMAL PROTECTION



DIP28



PLCC28



FLEXIWATT15

ORDER CODES :
L3091 (DIP28)
L3091P (PLCC28)
L3000 (FLEXIWATT15)

DESCRIPTION

The SLIC KIT (L3000/L3091) is a set of solid state devices designed to integrate many of the functions needed to interface a telephone line. It consists of 2 integrated devices ; the L3000 line interface circuit and the L3091 control unit.

The kit implements the main features of the BORSHT functions :

- Battery feed (balance mode)
- Ringing Injection
- Signalling Detection
- Hybrid Function

The SLIC KIT injects the ringing signal in balanced mode and requires a positive supply voltage of typically + 72V to be available on the subscriber card.

The L3000/L3091 KIT generates the ringing signal internally, avoiding the requirement for expensive external circuitry. A low level 1.5Vrms input is required. (This can be provided by the combo).

A special operating mode limits the SLIC KIT power dissipation to 70mW in on-hook condition keeping the on/off hook detection circuit active.

Through the Digital Interface it is also possible to set an operating mode that allows measurements of loop resistance and therefore of line lenght.

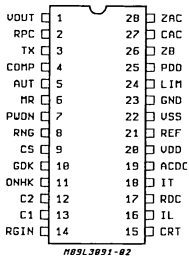
The L3091 is full compatible with L3090 but with additional functions.

This kit is fabricated using a 140V Bipolar technology for L3000 and a 12V Bipolar I2L technology for L3091.

This kit is specially suitable to Private Automatic Branch Exchange (PABX) and Low Range C.O. Applications.

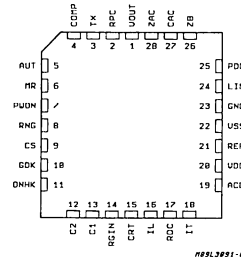
PIN CONNECTIONS

M89L3091-02



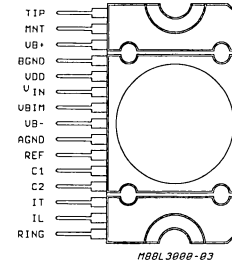
DIP28

M89L3091-01



PLCC28

M89L3091-03



FLEXIWATT15

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_b-	Negative Battery Voltage	– 80	V
V_b+	Positive Battery Voltage	80	V
$\|V_b- \|+\| V_b+\|$	Total Battery Voltage	140	V
V_{dd}	Positive Supply Voltage	+ 5.5	V
V_{ss}	Negative Supply Voltage	– 5.5	V
$\|V_{agnd}-V_{bgnd}\|$	Max Voltage between Analog Ground and Battery Ground	5	V
T_j	Max Junction Temperature	+ 150	°C
T_{stg}	Storage Temperature	– 55 to + 150	°C

THERMAL DATA

L3000 HIGH VOLTAGE

R_{thjc}	Max Resistance Junction to Case	4	°C/W
R_{thja}	Max Resistance Junction to Ambient	50	°C/W

L3091 LOW VOLTAGE

R_{thja}	Max Resistance Junction to Ambient	80	°C/W

OPERATING RANGE

Symbol	Parameter	Min.	Typ.	Max.	Unit
T_{oper}	Operating Temperature Range	0		70	°C
V_b-	Negative Battery Voltage	– 70	– 48	– 24	V
V_b+	Positive Battery Voltage	0	+ 72	+ 75	V
$\|V_b- \|+\| V_b+\|$	Total Battery Voltage		120	130	V
V_{dd}	Positive Supply Voltage	+ 4.5		+ 5.5	V
V_{ss}	Negative Supply Voltage	– 5.5		– 4.5	V
I_{max}	Total Line Current ($I_L + I_T$)			85	mA

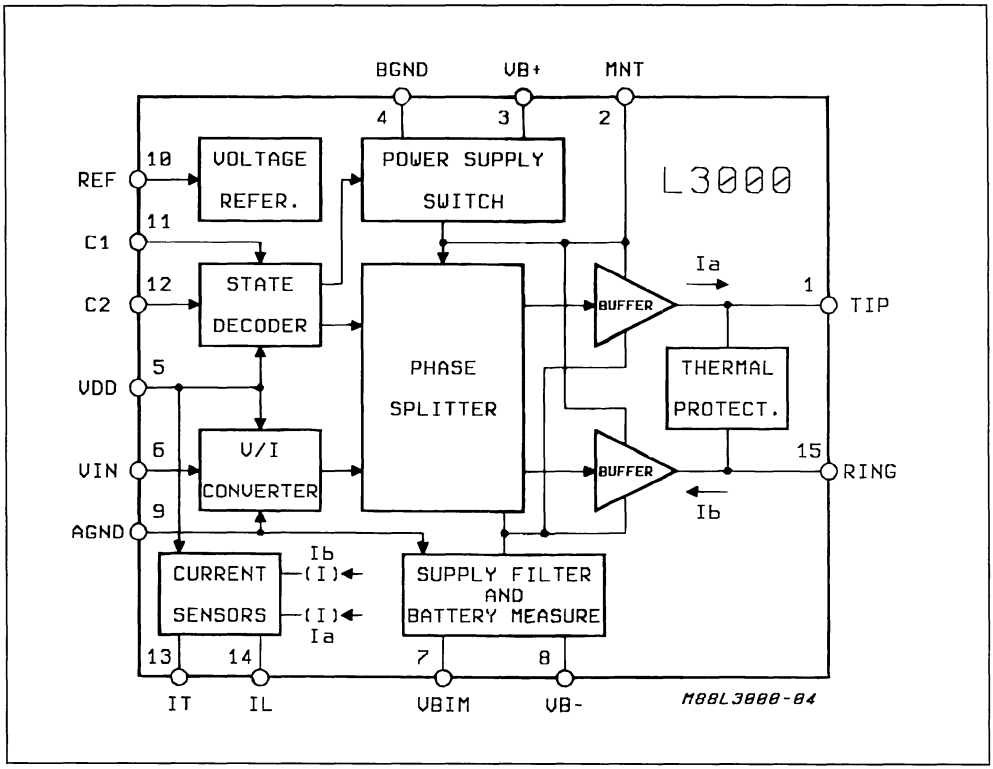
PIN DESCRIPTION (L3000)

N°	Name	Description
1	TIP	A line termination output with current capability up to 100mA (I_a is the current sourced from this pin).
2	MNT	Positive Supply Voltage Monitor
3	V_B+	Positive Battery Supply Voltage
4	BGND	Battery ground relative to the V_B+ and the V_B- supply voltages. It is also the reference ground for TIP and RING signals.
5	V_{DD}	Positive Power Supply + 5V
6	VIN	2 wire unbalanced voltage input.
7	VBIM	Output voltage without current capability, with the following functions : - give an image of the total battery voltage scaled by 40 to the low voltage part. - fliter by an external capacitor the noise on V_B-.
8	V_B-	Negative Battery Supply Voltage
9	AGND	Analog Ground. All input signals and the V_{DD} supply voltage must be referred to this pin.
10	REF	Voltage reference output with very low temperature coefficient. The connected resistor sets internal circuit bias current.
11	C1	Digital signal input (3 levels) that defines device status with pin 12.
12	C2	Digital signal input (3 levels) that defines device status with pin 11.
13	I_T	High precision scaled transversal line current signal. $I_T = \frac{I_a + I_b}{100}$
14	IL	Scaled longitudinal line current signal. $IL = \frac{I_a - I_b}{100}$
15	RING	B line termination output with current capability up to 100mA (I_b is the current sunk into this pin).

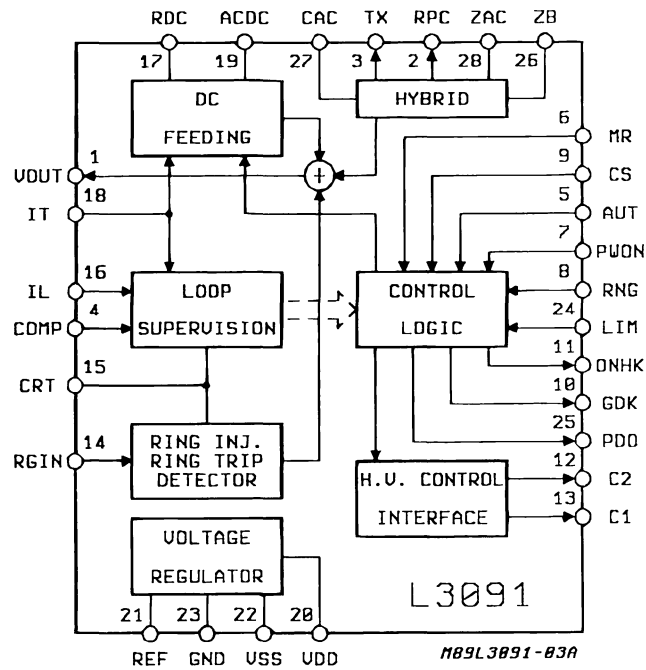
PIN DESCRIPTION (L3091)

N°	Name	Description
1	VOUT	Two wire unbalanced output carrying out the following signals reduced by 40 : 1) DC voltage to perform the proper DC characteristic. 2) Ringing Signal 3) Voice Signal
2	RPC	AC line Impedance Adjustment Protection Resistances Compensation
3	TX	Transmit Amplifier Output
4	COMP	Comparator Input. This is the input of the comparator that senses the line voltage in power down and in automatic stand-by , allowing off hook detection in this mode.
5	AUT	Aut. Input. It is a part of the digital interface. Looded when CS is low.
6	MR	Master Reset Input. When it is connected to ground the SLIC is forced in power down. It has an internal pull-up.
7	PWON	Power on/power off Input. This input is part of digital interface. Loaded when CS is low.
8	RNG	Ring Enable Input, This input is part of the digital interface. Loaded when CS is low.
9	CS	Chip Select Input
10	GDK	Ground Key Output Enabled by CS Low
11	ONHK	On Hook/off Hook Output Enabled by CS Low
12	C2	State Control Signal 2
13	C1	State Control Signal 1. Combination of C1 and C2 define operating mode of the high voltage part.
14	RGIN	Low Level Ringing Signal Input
15	CRT	Ring Trip Detection
16	IL	Longitudinal Line Current Input $IL = \frac{I_a - I_b}{100}$
17	RDC	DC Feeding System
18	IT	Transversal Line Current Input $IT = \frac{I_a + I_b}{100}$
19	ACDC	AC - DC Feedback Input
20	VDD	Positive Supply Voltage, + 5V
21	REF	Bias Setting Pin
22	VSS	Negative Supply Voltage, – 5V
23	GND	Analog and Digital Ground
24	LIM	Limiting Current Selection Input. Looded when CS is low.
25	PDO	Power Down Output. Driving the high voltage part L3000 through the bias resistor RH.
26	ZB	TX Amplifier Negative Input. Performing the two to four wire conversion.
27	CAC	AC Feedback Input
28	ZAC	AC Line Impedance Synthesis

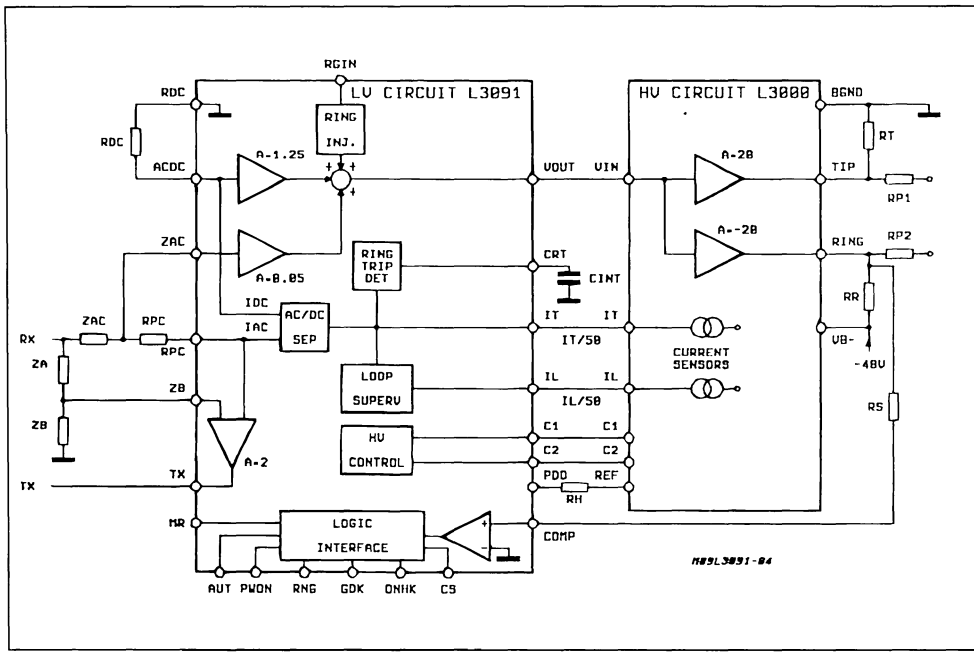
L3000 BLOCK DIAGRAM



L3091 BLOCK DIAGRAM (pins are for DIP28)



FUNCTIONAL DIAGRAM



FUNCTIONAL DESCRIPTION

L3000 - HIGH VOLTAGE CIRCUIT

The L3000 line interface provides battery feed for telephone lines and ringing injection. Both these operations are done in Balance Mode. This is very important in order to avoid the generation of common mode signals in particular during the pulse dialling operation of the telephone set connected to the SLIC. The IC contains a state decoder that under external control can force the following operational modes : stand-by, conversation and ringing.

In addition Power down mode can be forced connecting the bias current resistor of L3000 (RH) to VDD.

Two pins, I_L and I_T, carry out the information concerning line status which is detected by sensing the line current into the output stage.

The L3000 amplifies both the AC and DC signals entering at pin 6 (VIN) by a factor equal to 40.

Separate grounds are provided :

- Analog ground as reference for analog signals
- Battery ground as a reference for the output stages

L3091 - LOW VOLTAGE CIRCUIT

The L3091 Low Voltage Control Unit controls the L3000 line interface module providing set up data to set line feed characteristics and to inject ringing. An on chip digital parallel interface allows a microprocessor or a second generation COMBO as the TS5070 to control all the operations.

L3091 defines working states of Line Interface Circuit and also informs the controller about line status.

L3000 WORKING STATES

In order to carry out the different possible operations, the L3000 has several different working states. Each state is defined by the voltage respectively applied by pin 12 and 13 of L3091 to the pins 12 and 11 of L3000.

Three different voltage levels (5.0, + 5) are available at each connection, so defining nine possible states as listed in tab. 1.

Appropriate combinations of two pins define three of the four possible L3000 working states that are :
a) Stand-by (SBY)
b) Conversation (CVS)
c) Ringing (RING)

Table 1.

		Pin 12 of L309 / Pin 12 of L3000		
		+ 5	0	– 5
Pin 13 of L30	+ 5	Stand-by	Conversation	Not Used
	0	Not Used	Not Used	Not Used
Pin 11 of L3000	– 5	Not Used	Ringing	Not Used

The fourth status, Power down (PD), is set by the output pin PDO of the L3091 that disconnect the Bias Resistor, RH, of L3000 from ground.

The main difference between Stand-by and Power down is that in SBY the power consumption on the battery voltage VB– (– 48V) is reduced but the L3000 DC feeding and monitoring circuits are still active, in PD the power consumption on VB- is reduced to zero, and the L3000 is completely switched off.

SLIC OPERATING MODES

Through the L3091 Digital Interface it is possible to select six different SLIC OPERATING MODES :

1) Conversation or Active Mode (CVS)

2) Stand - By Mode (SBY)

3) Power - Down Mode (PD)

4) Automatic Stand - By Mode (ASBY)

5) Test Mode (TS)

6) Ringing Mode (RNG)

CONVERSATION (CVS) OR ACTIVE MODE

This operating mode is set by the control processor when the Off hook condition has been recognized,

As far as the DC Characteristic is concerned two different feeding conditions are present :

a) Current limiting region : the DC impedance of the SLIC is very high (> 20KΩ) and therefore the system works like a current generator. By the L3091 Digital Interface it is possible to selects the value of the limiting current. :

62mA, 42mA or 25mA.

b) A standard resistive feeding mode : the characteristic is equal to a battery voltage (VB-) minus 5V, in series with a resistor, whose value is set by external components (see external component list of L3091).

Switching between the two regions is automatic without discontinuity, and depends on the loop resistance. The SLIC AC characteristics are guaranteed in both regions.

Fig. 1 shows the DC characteristic in conversation mode.

Fig. 2 shows the line current versus loop resistance for two different battery values and RFS = 200Ω.

The allowed maximum loop resistance depends on the values of the battery voltage (VB), on the RFS and on the value of the longitudinal current (I_{GDK}). With a battery voltage of 48V, RFS = 200Ω and I_{GDK} = 0mA, the maximum loop resistance is over 3000Ω and with I_{GDK} = 20mA is about 2000Ω (see Application Note on maximum loop resistance for L3000/L3090 SLIC KIT).

In conversation mode the AC impedance at the line terminals is synthetized by the external components ZAC and RP, according to the following formula :

$$ZML = \frac{ZAC}{25} + 2 \times RP$$

Depending on the characteristic of the ZAC network, ZML can be either a pure resistance or a complex impedance. This allows for ST SLIC to meet different standards as far as the return loss is concerned. The capacitor CCOMP guarantees stability to the system.

The two to four wire conversion is achieved by means of a circuit that can be represented as a Wheatstone bridge, the branches of which being :

1) The line impedance (Zline).

2) The SLIC impedance at line terminals (ZML).

3) The balancing network ZA connected between RX input and ZB pin of L3091.

4) The network ZB between ZB pin and ground that shall copy the line impedance.

It is important to underline that ZA and ZB are not equal to ZML and to Zline. They both must be multiplied by a factor in the range of 10 to 25, allowing use of smaller capacitors.

In conversation mode, the L3000 dissipates about 500mW for its own operation. The dissipation related to the current supplied to the line shall be added, in order to get the total dissipation.

In the same condition the power dissipation of L3090 is typically 100mW.

Figure 1 : DC Characteristics in Conversation Mode.

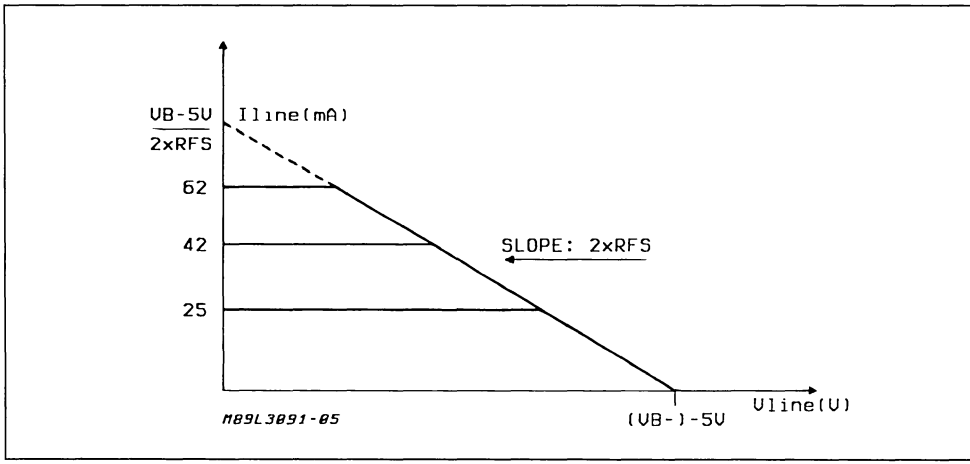
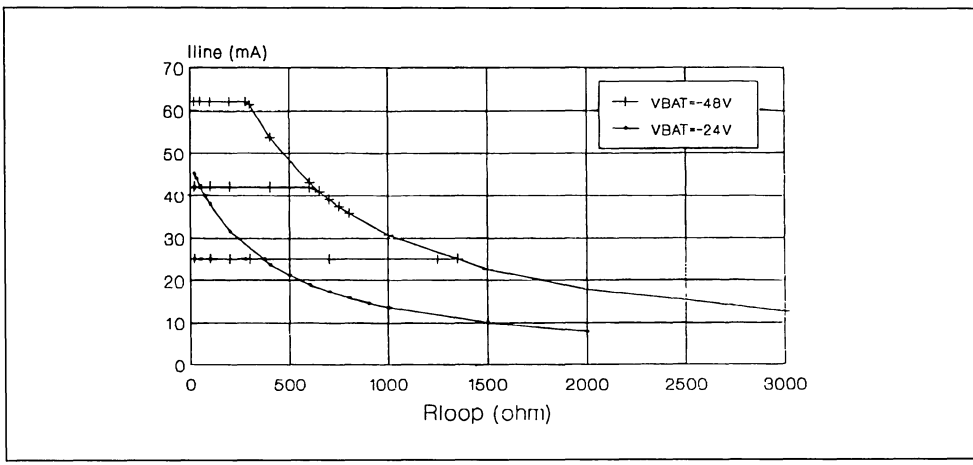


Figure 2 : Line Current versus Loop Resistance - RFS = 200Ω ; Limiting Currents : 25/42/62 mA.



STAND-BY (SBY) MODE

In this mode the bias currents of both L3000 and L3090 are reduced as only some parts of the two circuits are completely active, control interface and current sensors among them. The current supplied to the line is limited at 12mA, and the slope of the DC characteristic corresponds to 2 x RFS.

The AC characteristic in Stand-by corresponds to a low impedance (2 x RP)

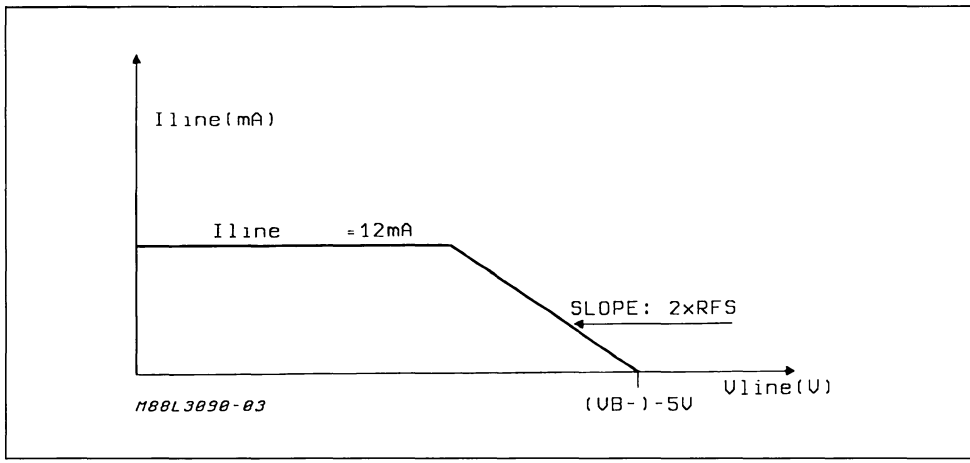
In Stand-by mode the line voltage polarity is just in direct condition, that is the TIP wire more positive than the RING one as in Conversation Mode.

When the SLIC is in Stand-by mode, the power dissipation of L3000 does not exceed 200mW from – 48V) eventually increased of a certain amount if some current is flowing into the line.

The power dissipation of the L3091 in the same condition is typically 70mW.

SBY Mode is usually selected when the telephone is in on-hook. It allows a proper off-hook detection also in presence of high common mode line current or with telephone set sinking few milliAmpere of line current in on hook condition.

Figure 3 : DC Characteristic in Stand-by Mode.



SLIC OPERATING MODES

POWER DOWN (PD) MODE

In this mode the L3000 present a high impedance (> 1 Mohm) to the line and cannot feed any line current.

The L3091 forces L3000 in Power Down disconnecting its bias Resistor, RH, from the ground through the output pin PD0.

The power dissipation from the battery voltage (– VB) is almost equal to zero and the power dissipation of L3091 is typically 70mW.

The PD mode is normally used in emergency condition but can be used also in normal on-hook condition.

In this case the off-hook detection is performed using the line sense comparator integrated in the L3091.

The fig. 4 shows the functional circuit to perform the off hook detection in Power down mode.

The resistor RR and RT feed the line current. The voltage at the terminal of the resistor RS connected to RING wire is normally – 48V.

When there is a loop resistor between TIP and RING wires the voltage will increases to – 24V.

The comparator C1 will change its output voltage from low to high level.

If the Chip Select input (CS) is low the ONHK output pin will be set to low level (+ 0V) indicating that the off hook condition is present.

This off-hook detection circuit can be influenced by common mode signal present on RING Terminal. The capacitor Cs is used to filter this common mode signal.

In the case of very high common mode signal after the detection of an high level on the ONHK output pin, it is suggested to set the SLIC in Stand-by. In this operating mode the off-hook detection circuit is not sensitive to the line common mode signal.

If in Stand-by Mode the off-hook detection is not confirmed (ONHK output set to low level) we suggest after few second to set the SLIC again in Power Down Mode.

Total operation is managed by line card controller.

Figure 4 : Off-hook Detection Circuit in Power Down Mode.

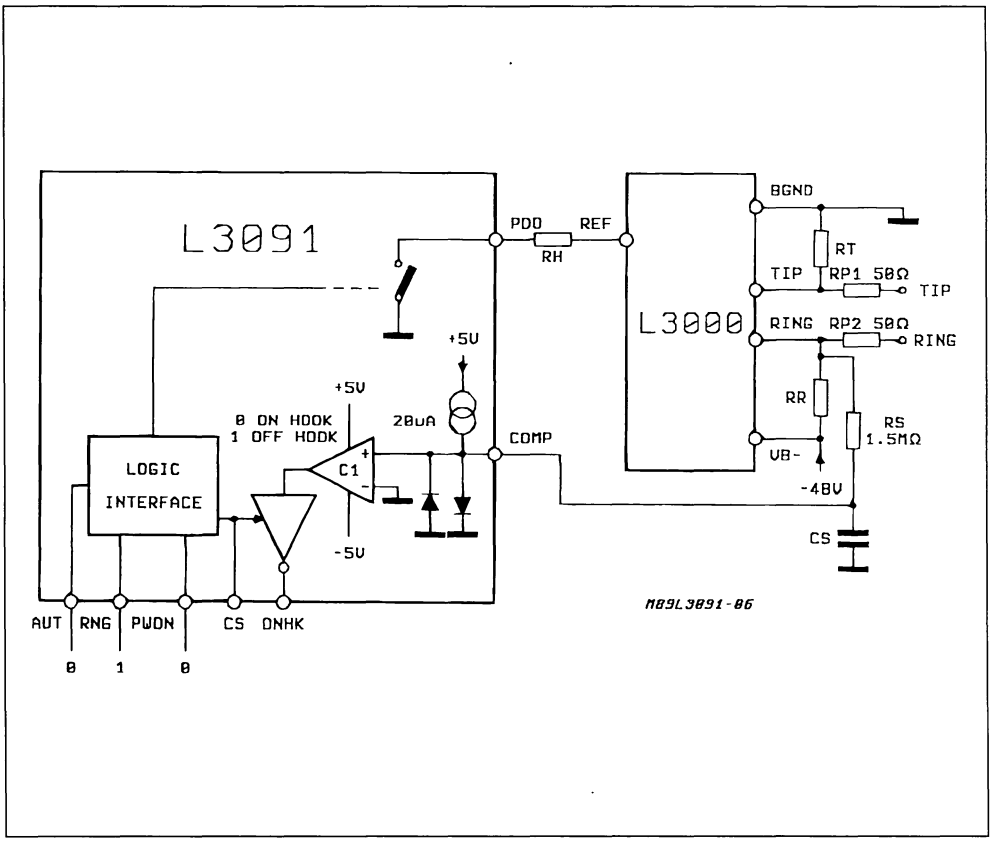
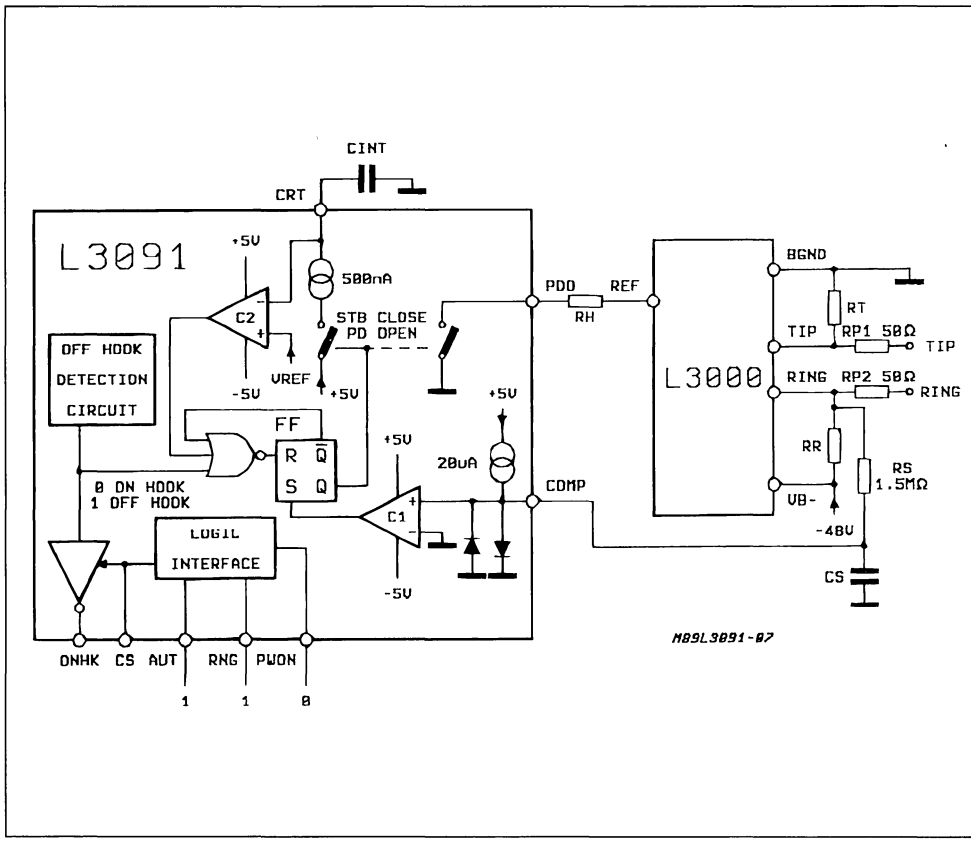


Figure 5 : Off-hook Detection Circuit in Automatic Standby Mode.



AUTOMATIC STAND - BY (ASBY) MODE

This is an operating mode similar to the Power Down Mode, but with the software procedure to detect off-hook condition integrated in hardware on chip.

Fig. 5 shows the functional circuit activated in this mode.

When the off-hook condition occurs RING wire voltage goes high (from - 48V to - 24V).

The output of the comparator C1 will go high setting the output of the flip - flop FF high.

Therefore L3091 will set L3000 in Stand-by providing a ground signal at pin PDO.

At the same time the external capacitor CINT will be slowly charged.

In Stand-by the internal off-hook Detection circuit will be activated and will check if the off-hook condition detected by the comparator C1 was true or not true.

If the off-hook condition is confirmed the SLIC will be kept in Stand-by Mode and the output ONHK will go low when CS is low.

If the off-hook condition is not confirmed the SLIC will be kept in Stand - By only for a few seconds. When the voltage at CRT out put will reach the V_{REF} value the C2 comparator will reset the FF Flip - Flop and therefore the SLIC will be set again in Power Down.

The Automatic Stand-by (ASBY) Mode combine the key characteristics of Power Down (PD) and Stand-by (SBY) Modes in particular it is characterized by a very low power consumption (as the Power Down mode) and a sophisticated off hook detection circuit (as the Stand-By mode).

The card controller will receive the off-hook information from the pin ONHK only after that it is checked and confirmed by the internal off-hook detector that is not sensitive to spikes and common mode line signal. Therefore the software required to manage the SLIC will be very simple.

TEST (TS) MODE

When this mode is activated the SLIC will be set in conversation mode keeping the initial value of limiting current.

The GDK output pin of L3091 Digital Interface will be set to "0" if the SLIC is operating in the limiting current region of the DC characteristic, see fig. 1 and 2. GDK output will be set to 1 if the SLIC is operating in the resistive region.

The SLIC will work in one of the two region depending on the loop resistance and the programmed limiting current value.

By changing the limiting current value selected in conversation mode it is possible to measure the Loop Resistance and therefore the line lenght connected to the SLIC.

The following table shows the ranges of the loop resistance that set the GDK output pin to high and low level in correspondance of all the possible limiting current values (25/42/62mA) with RFS = 200Ω.

Limiting Current	GDK = 0	GDK = 1
62mA	(0 – 300) ohm	> 300 ohm
42mA	(0 – 600) ohm	> 600 ohm
25mA	(0 – 1300) ohm	> 1300 ohm

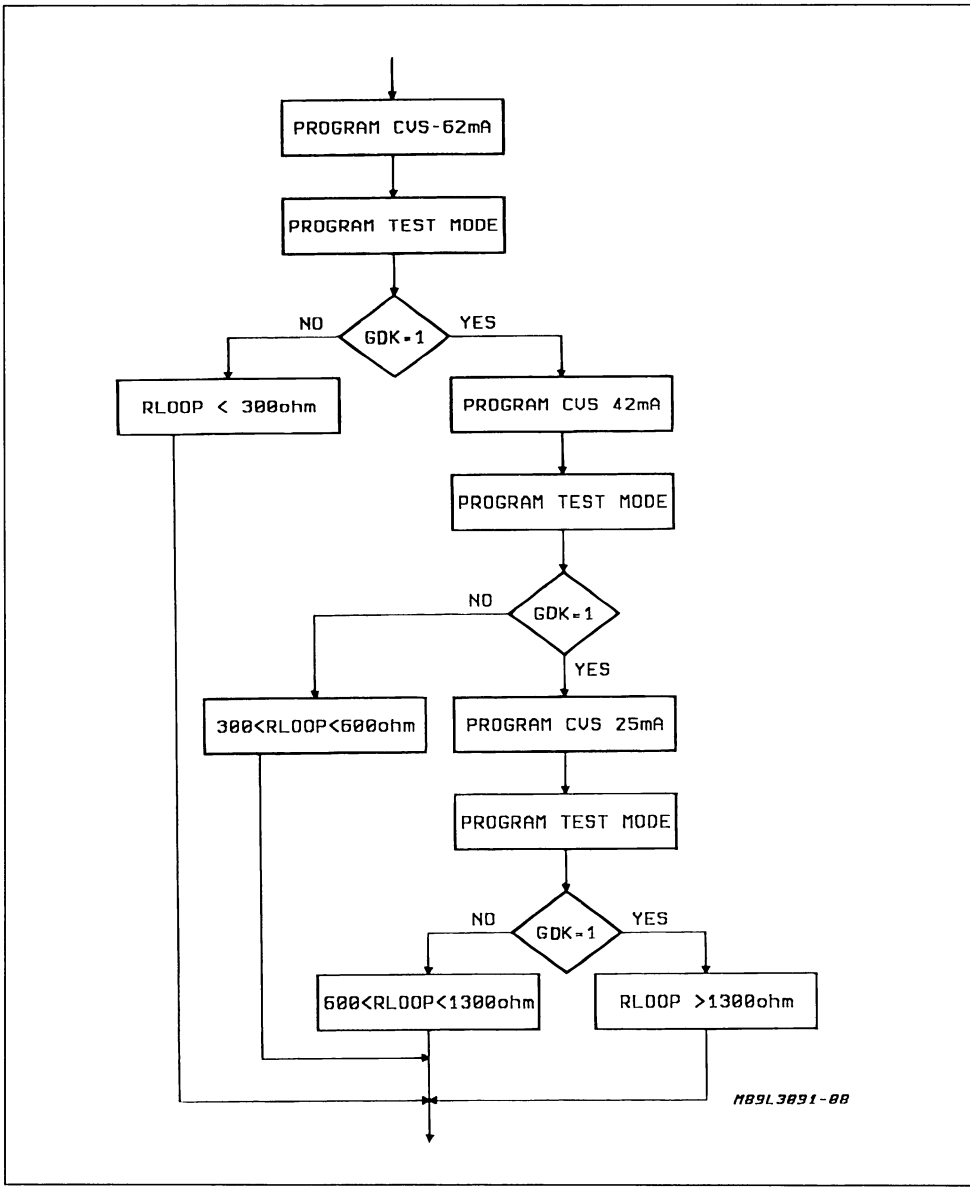
If, for example, the loop resistance is 400Ω the GDK output will be 0 only when the limiting current value is 42 or 25mA.

The card controller can program consecutive Test Mode and Conversation Mode with different limiting current in order to individuate the range of loop resistance as shown in the flow chart of fig. 6.

The information of the Loop Resistance Range can be very useful to optimize the transmission characteristics of the Line Card to each line.

For example, if a second generation COMBO like ST TS 5070 is used the Card Controller can use this information to change the T_X, R_X Gains and echo cancellation characteristics into the programmable COMBO improving the quality of the system.

Figure 6 : Procedure for Loop Resistance Evaluation.



RINGING MODE

When the ringing function is selected by the control processor a low level signal (1.5Vrms) with a frequency in the range from 16 to 70Hz, permanently applied to the L3091 (pin RGIN), is amplified and injected in balanced mode into the line through the L3000 with a super imposed DC voltage of 22V.

This low level sinewave can be obtained also from COMBO connecting RGIN pin to RX COMBO output with a decoupling capacitor.

The first and the last ringing cycles are synchronized by the L3091 so that the ringing signal always starts and stops when the line voltage crosses zero.

When this mode is activated, the L3000 operates between the negative and the positive battery voltages typically - 48V and + 72V. The impedance to the line is just equal to the two external resistors (typ. 100Ω).

Ring trip detection is performed autonomously by the SLIC, without waiting for a command from the control processor, using a patented system which allows detection during a ringing burst ; when the off-hook condition is detected, the SLIC stops the ringing signal and forces the Conversation Mode.

In this condition, if CS = 0V, the output pin ONHK goes to 0V.

After the detection of the ONHK = 0, the Card Controller must set the SLIC in Conversation Mode to remove the internal latching of the On/Off hook information.

CONTROL INTERFACE BETWEEN THE SLIC AND THE CARD CONTROLLER

The SLIC states and functions are controlled by microprocessor or interface latches of a second generation combo through seven wires that define a parallel digital interface.

The seven pins of the digital interface have the following functions :

- Chip select input (CS)
- Power on/off input (PWON)
- Ring enable input (RNG)
- Automatic SBY input (AUT)
- Limiting current input (LIM)
- On hook/Off hook detection output (ONHK)
- Ground Key detection output (GDK)

The four input pins PWON, RNG, AUT and LIM, set the status of the SLIC as shown in the following table.

The output pin ONHK is equals to 0V when the line is in off-hook condition (I_{line} > 7,5mA) and is equal to + 5V when the line is in On hook condition (I_{line} < 5,5mA).

The output pin GDK monitors the ground key function when the SLIC is in Conversation (CVS) Mode and the DC operating region (limiting or resistive) in Test (TS) Mode. When the SLIC is in Conversation (CVS) Mode and I_{GDK} (longitudinal current) > 12mA, pin GDK is set to 0V ;

Operating Mode	Input Pin				Output Pin	
	RNG	PWON	AUT	LIM	ONHK	GDK
Conversation 25mA	0	1	1	X	1 on-hook 0 off-hook	1 Ground key not detected. 0 Ground dey detected.
Conversation 42mA	0	1	0	1		
Conversation 62mA	0	1	0	0		
Boosted Battery 25mA	0	1	HI	X		
Stand-by	0	0	0	X		Disable
Automatic Stand-by	1	0	1	X		
Power-down	1	0	0	X	C1 Comparator Output	Disable
Test Mode	0	0	1	X	1 on-hook 0 off-hook	0 Limiting Region 1 Resistive Region
Ringing Inj. (CVS 25mA)	1	1	1	X		Disable
Ringing Inj. (CVS 42mA)	1	1	0	1		
Ringing Inj. (CVS 62mA)	1	1	0	0		

N.B. : When Ringing Mode is selected, you must choose also which of the three possible Conversation Modes, the SLIC will automatically select if Off-Hook condition will be detected during ringing

When I_{GDK} < 8MA, pin GDK set to + 5V

The longitudinal current (I_{GDK}) is defined as follows :

$$I_{GDK} = \frac{I_A - I_B}{2}$$

Where I_A is the current sourced from pin TIP and I_B is the current sunk into pin RING.

The CS input pin allows to connect the I/O pins of the digital interfaces of many SLIC together.

It is possible to do it because :

When the CS = + 5V the output pins (ONHK, GDK) are in high impedance condition (> 100KΩ). The signals present at the input pins are not transfered into the SLIC.

When the CS = 0V the output pins change in function of the values of the line current (I_{line}) and the longitudinal current (I_{GDK}). The operating status of the SLIC are set by the voltage applied to the input pins.

The rising edge of the CS signal latches the signal applied to the input pins. The status of the SLIC will not change until the CS signal will be again equal to zero.

See timings fig 8 & 9.

An additional input pin MR (Master Reset) can be useful during the system start up phase or in emergency condition.

Infact when this pin is set to "0" the SLIC will be set in POWER DOWN MODE. This pin has an internal pull-up resistor of about 70KΩ

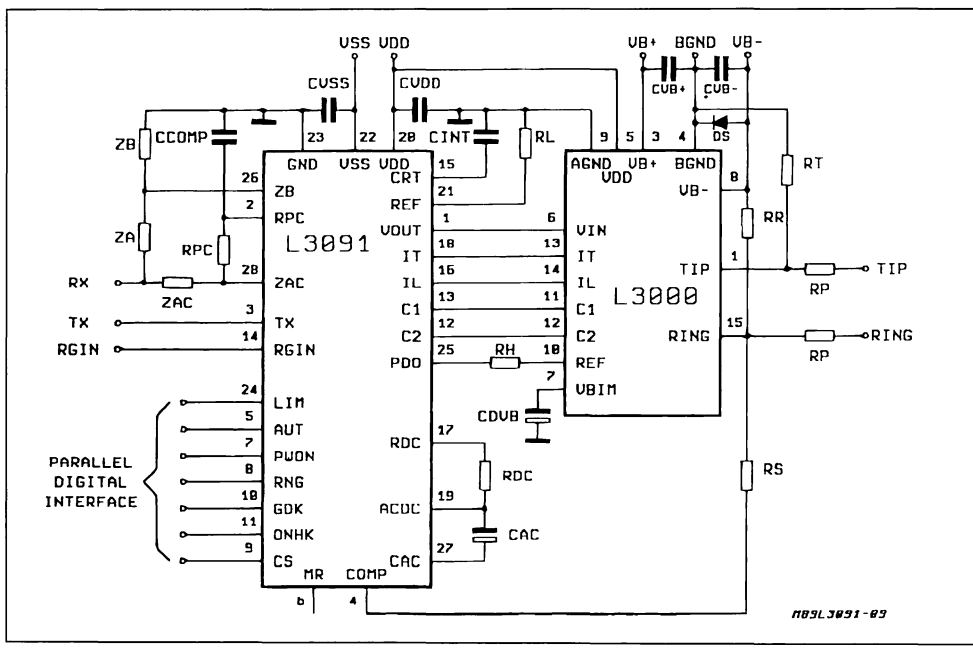
EXTERNAL COMPONENTS LIST

To set up the SLIC kit into operation, the following parameters have to be defined :

- The DC feeding resistance RFS, defined as the resistance of each side of the traditional feeding system (most common value for RFS are 200, 400 or 500).
- The AC input/output SLIC impedance at line terminals, ZML, to which the return loss measurement is refered. It can be real (typically 600Ω) or complex.
- The equivalent AC impedance of the line Z_{line} used for evaluation of the trans-hybrid loss (2/4 wire conversion). It is usually a complex impedance.
- The frequency of the ringing signal Fr (SLIC can work with this frequency ranging from 16 to 68Hz).
- The value of the two resistors RP in series with the line terminals ; main purpose of the a.m. resistors is to allow primary protection to fire..

With these assumptions the following components list is defined :

Figure 7 : Typical Application Circuit.



EXTERNAL COMPONENT LIST FOR THE L3000

Component		Involved Parameter or Function
Ref	Value	
RH	24.9KΩ ± 2%	Bias Resistor
RP	30 to 100Ω	Line Series Resistor
CDVB	47µF – 20WV ± 20%	Battery Voltage Rejection
CVB + (note 1)	0.1µF – 100WV ± 20%	Positive Battery Filter
CVB – (note 1)	0.1µF – 100WV ± 20%	Negative Battery Filter
DS (note 1)	BAT 49	Protective Shottky Diode

EXTERNAL COMPONENT LIST FOR THE L3091

Component		Involved Parameter or Function
Ref	Value	
CVSS	0.1µF – 15WV (note 1)	Negative Supply Voltage Filter
CVDD	0.1µF – 15WV (note 1)	Positive Supply Voltage Filter
CAC	47µF – 10WV ± 20%	AC Path Decoupling
ZAC	25 x (ZML – 2xRP)	2 Wire AC Impedance
CCOMP	$\frac{1}{(6.28 \times 30000 \times ZML \times 25)}$	AC Loop Compensation
RPC	25 x (2xRP)	R_p Insertion Loss Compensation
RDC	2 x (RFS – RP)	DC Feeding Resistor
RL	63.4KΩ ± 1%	Bias Resistor
ZA	K x Z_{ML} (note 2)	SLIC Impedance Balancing Network
ZB	(K x Zline) // ($\frac{25}{K}$ x CCOMP) (note 3)	Line Impedance Balancing Network
CINT	(note 4)	Ring Trip Detection Time Constant
RT	47KΩ	Resistors used only in the automatic stand-by mode.
RR	47KΩ	
RS	1.5MΩ	

Notes : 1. In most applications these components can be shared between all the SLIC s on the Subscriber Card.
2. The structure of this network shall copy the SLIC output impedance multiplied by a factor K = 10 to 25.
3. The structure of this network shall copy the line impedance, Z_{line}, multiplied by a factor K = 10 to 25 and compensate the effect of CCOMP on transhybrid rejection.
4. The CINT value depends on the ringing frequency Fr :

Fr (Hz)	16/18	19/21	22/27	28/32	33/38	39/46	47/55	56/68
CINT (nF)	680	580	470	390	330	270	220	180

The CINT value can be optimized experimentally for each application choosing the lower value that in correspondance of the lower ringing frequency, the minimum line lenght and the higher number of ringers doesn't produce false off-hook detection.

ELECTRICAL CHARACTERISTICS

(VDD = + 5V ; VSS = 5V ; VB + = + 72V ; VB – = – 48V ; Tamb = + 25°C)

STANDBY

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
VLS	Output Voltage at L3000 Terminals	I Line = 0mA		43		V
ILCC	Short Circuit Current		10		14	mA
Iot	Off-hook Detection Threshold		5.6		9.8	mA
Hys	Off-hook/on-hook Hysteresis		1.5		2.5	mA
Vis	Symmetry to Ground	I Line = 0mA			.75	V

CONVERSATION

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
VLO	Output Voltage at L3000 Line Terminals	I Line = 0mA		43		V
Ilim	Current Programmed Through the LIM and AUT Inputs		Ilim – 10%		Ilim + 10%	mA
Iot	Off-hook Detection Threshold		5.6		9.8	mA
Hys	Off-hook/on-hook Hysteresis		1.5		2.5	mA
Iigk	Longitudinal Line Current with GDK Detect		6.5		15	mA

POWER-DOWN

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{CN}	Input Voltage at Pin COMP to Set the Output Pin ONHK = 1				– 50	mV
V_{CF}	Input Voltage at Pin COMP to Set the Output Pin ONHK = 0		50			mV
I_{COM}	Output Current at Pin COMP	COMP = GND		20		µA

SUPPLY CURRENT

Symbol	Parameter		Min.	Typ.	Max.	Unit
I_{DD}	Positive Supply Current	Power Down/aut. Stand-by		7.0		mA
	CS = 1	Stand-by		8.8		mA
		Conversation		13.2		mA
		Ringing		12.8		mA
I_{SS}	Negative Supply Current	Power Down/aut. Stand-by		6.4		mA
	CS = 1	Stand-by		6.4		mA
		Conversation		8.2		mA
		Ringing		8.2		mA
I_{BAT-}	Negative Battery Supply Current	Power Down-aut. Stand-by		0		mA
	Line Current = ∅mA	Stand-by		2.9	4	mA
		Conversation		9.8	12	mA
		Ringing		26	28.5	mA
I_{BAT+}	Positive Battery Supply Current	Power Down-aut. Stand-by		0		mA
	Line Current = ∅mA	Stand-by		10	15	µA
		Conversation		10	15	µA
		Ringing		16	18.5	mA

AC OPERATION

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
ZIx	Sending Output Impedance on TX				15	Ω
THD	Signal Distortion at 2W and 4W Terminals	Vtx = 0dBm @ 1020Hz			0.5	%
RI	2W Return Loss	f = 300 to 3400Hz	20			dB
THI	Transhybrid Loss	f = 300 to 3400Hz	24			dB
Gs	Sending Gain	Vso = 0dBm f = 1020Hz	– 0.25		+ 0.25	dB
Gsf	Sending Gain Flatness vs. Frequency	f = 300 to 3400Hz Respect to 1020Hz	– 0.1		+ 0.1	dB
GI	Sending Gain Linearity	fr = 1020Hz Vsoref = – 10dBm Vso = + 4/– 40dBm	– 0.1		+ 0.1	dB
Gr	Receiving Gain	Vri = 0dBm ; f = 1020Hz	– 0.25		+ 0.25	dB
Grf	Receiving Gain Flatness	f = 300 to 3400Hz Respect to 1020Hz	– 0.1		+ 0.1	dB
Grl	Receiving Gain Linearity	fr = 1020Hz Vriref = – 10dBm Vri = + 4/– 40 dBm	– 0.1		+ 0.1	dB
Np4W	Psophomet. Noise 4W - Tx Terminals		– 70	– 75		dBmp
NP2W	Psophomet. at Line Terminals		– 70	– 75		dBmp
SVRR	Supply Voltage Rejection Ratio Relative to VB–	f = 10Hz Vn = 0.7Vrms		– 20		dB
		f = 1KHz Vn = 0.7Vrms			– 40	dB
		f = 3.4KHz Vn = 0.7Vrms			– 36	dB
Ltc	Longitudinal to Transversal Conversion	f = 300 to 3400Hz I line = 30mA ZML = 600Ω	49(*)	60		dB
Tlc	Transversal to Longitudinal Conversion		49(*)	60		dB

(*) : up to 52dB using selected L3000.

RINGING PHASE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Vir	Superimposed DC Voltage	Rloop > 100KΩ	19		29	V
		Rloop = 1KΩ	17		27	V
Vacr	Ringing Signal at Line Terminal	Rloop > 100kΩ V_{RGN} = 1.5Vrms/30Hz	56.0			Vrms
		Rloop = 1KΩ + 1μF V_{RGN} = 1.5Vrms/30Hz	56.0			Vrms
If	DC Off-hook Del Threshold			5.5		mA
Ilim	Output Current Capability		85		130	mA
Vrs	Ringing Symmetry				2	Vrms
THDr	Ringing Signal Distorsion				5	%
Zir	Ringing Amplicat. Input Impedance	L3091's Pin RGIN	50			KΩ
Vrr	Residual of Ringing Signal at Tx Output				100	mVrms
Trt	Ring Trip Detection Time	fring = 25Hz (T = 1/fring) CINT = 470μF		120(3T)		ms
Toh	Off-hook Status Delay after the Ringing Stop				50	μs

DIGITAL INTERFACE ELECTRICAL CHARACTERISTICS
(VDD = + 5V ; VSS = – 5V ; Tamb = 25°C)

STATIC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Vil	Input Voltage at Logical "0"	Pins CS PWON RNG LIM-AUT	0		0.8	V
Vih	Input Voltage at Logical "1"		2.0		5	V
Iil	Input Current at Logical "0"	Vil = 0V			200	μA
Iih	Input Current at Logical "1"	Vih = 5V			100	μA
Vol	Output Voltage at Logical "0"	Pins ONHK GDK Iout = – 1mA			0.4	V
Voh	Output Voltage at Logical "1"	Iout = 1mA	2.4			V
Ilk	Tristate Leak Current	CS = "1"			10	μA
I_{MR}	Pull-up MR Output Current	MR = 0		50		μA

DYNAMIC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Tsd	PWON, RNG, AUT, LIM		400			ns
Thd	PWON, RNG, AUT, LIM		500			ns
Tww	CS Impulse Width (writing op.)		800			ns
Thv	ONHK, GDK Data Out to "0" CS Delay				600	ns
Tvh	ONHK, GDK High Imped. to "1" CS Delay				600	ns
Twr	CS Impulse Width (writing op.)		800			ns

Figure 8 : Writing Operation Timing (controller to SLIC).

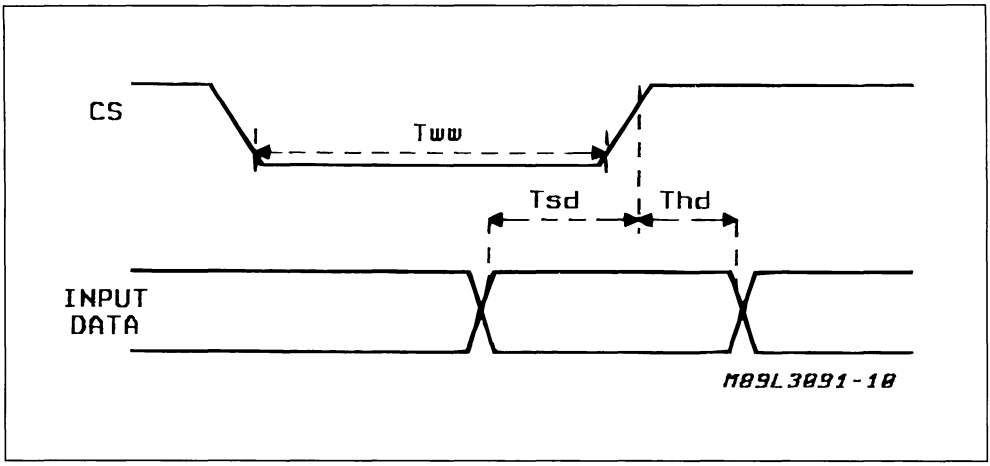


Figure 9 : Reading Operation Timing (from slic to controller).

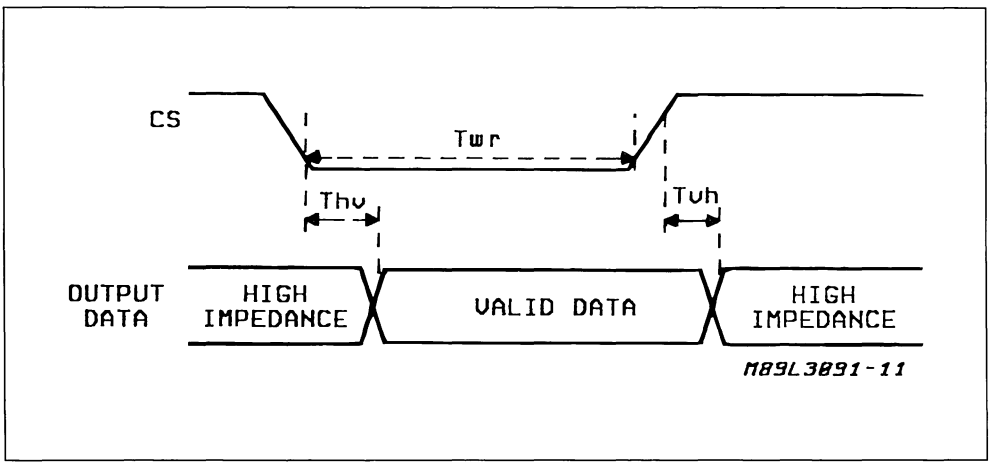
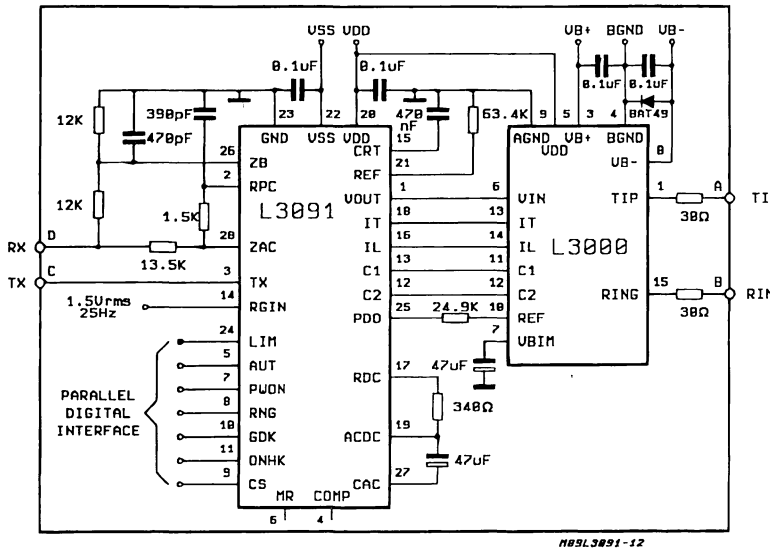
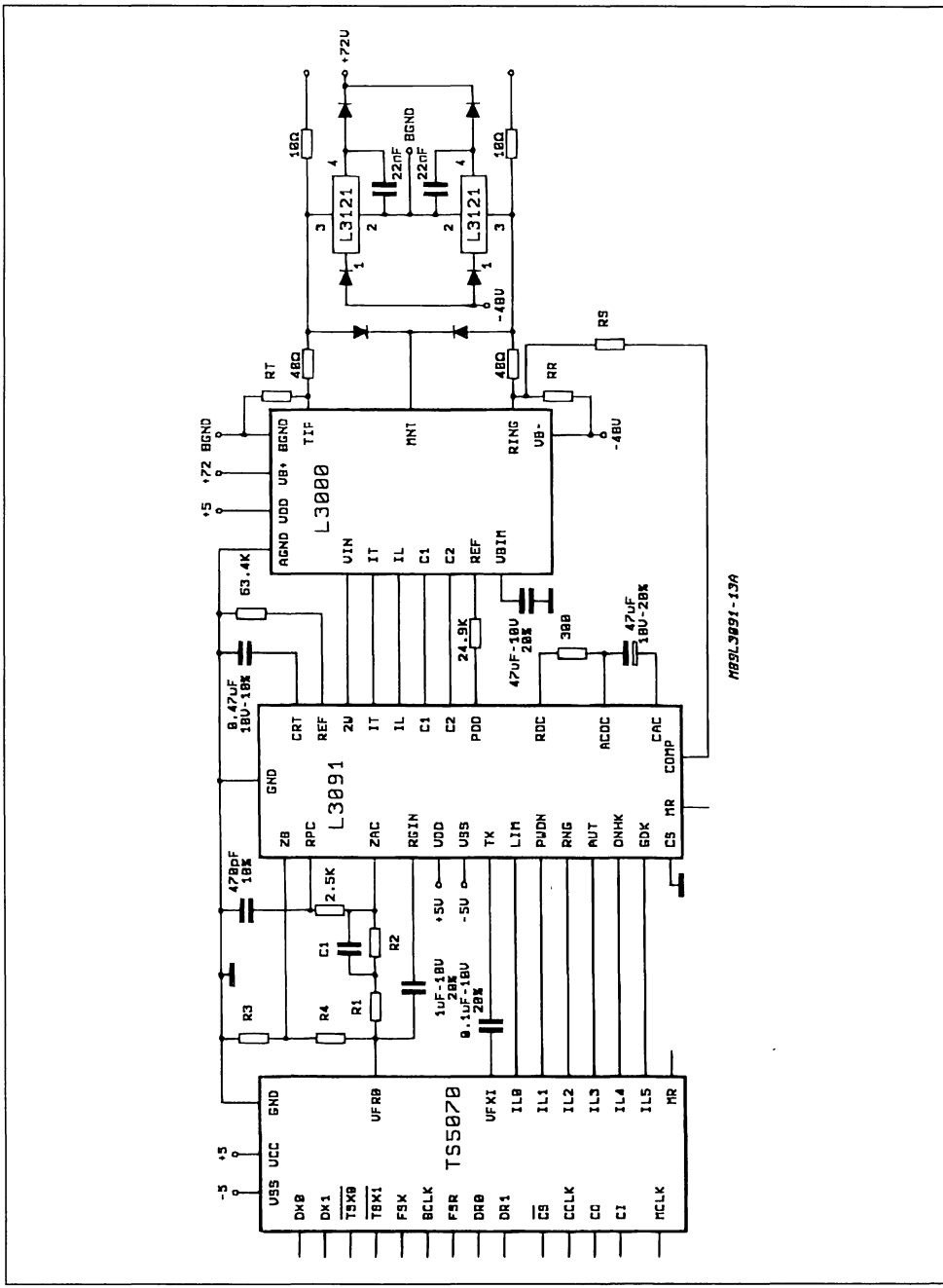


Figure 10 : Test Circuit.



A, B, C, D are test reference points use driving testing.

Figure 11 : Typical Application Circuit for Complete Subscriber Circuit (Protection - SLIC - COMBO).



APPENDIX A

SLIC TEST CIRCUITS

Referring to the test circuit reported at the end of each SLIC data sheet here below you can find the proper configuration for each measurement.

In particular : A-B : Line terminals

C : Tx sending output on 4W side

D : Rx receiving input on 4W Side

E : TTx teletaxe signal input

R_{GIN} : low level ringing signal input.

TEST CIRCUITS

Figure 1 : Symmetry to Ground.

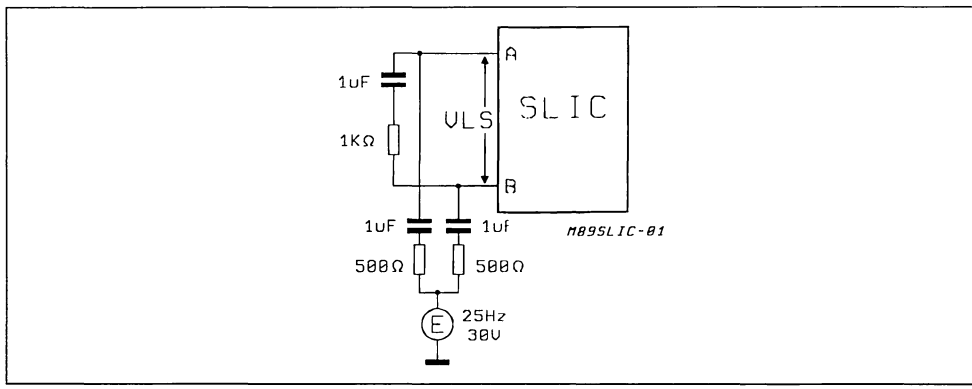
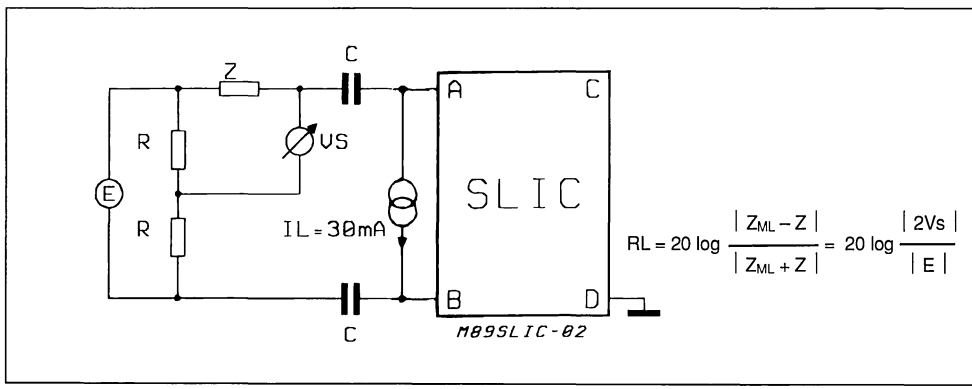


Figure 2 : 2W Return Loss.



TEST CIRCUITS (continued)

Figure 3 : Trans-hybrid Loss.

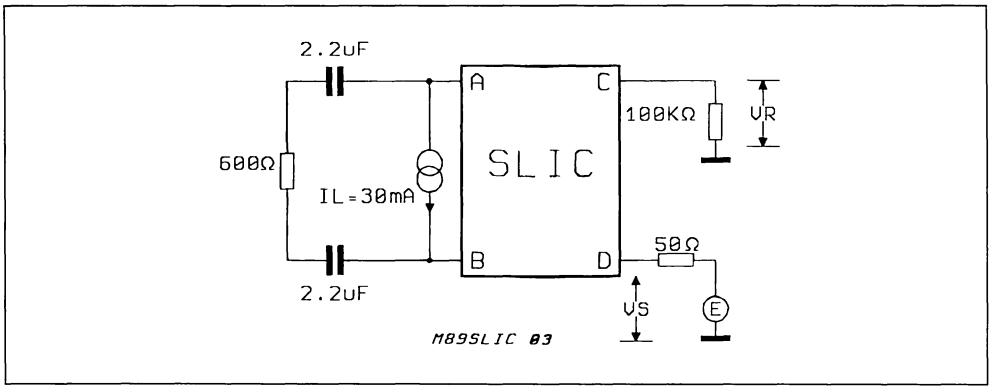


Figure 4 : Sending Gain.

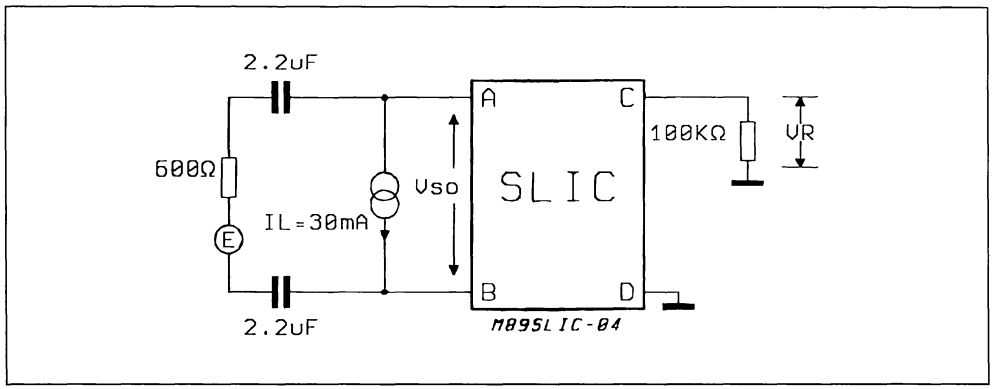
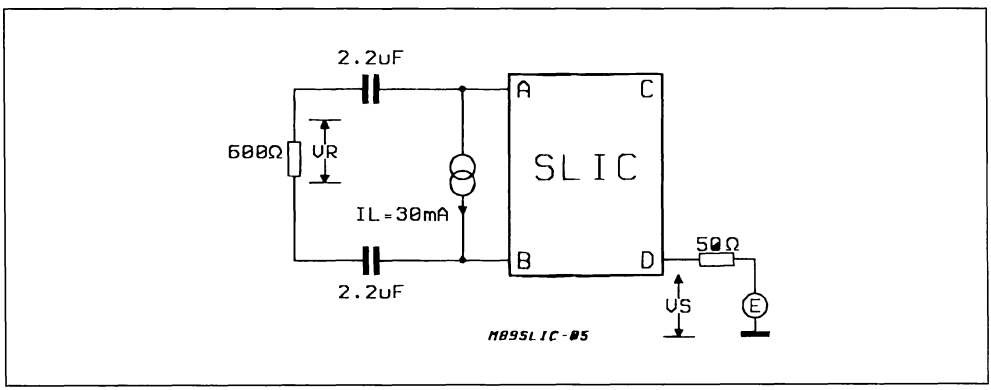


Figure 5 : Receiving Gain.



TEST CIRCUITS (continued)

Figure 6 : PSRR Relative to Battery Voltage VB–.

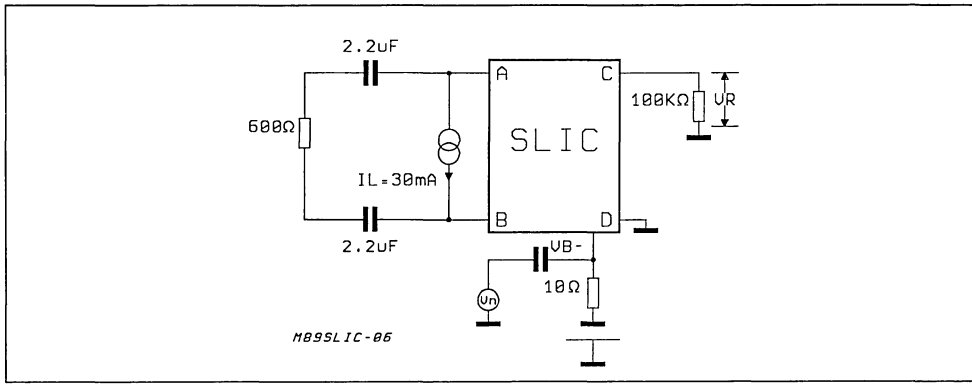


Figure 7 : Longitudinal to Transversal Conversion.

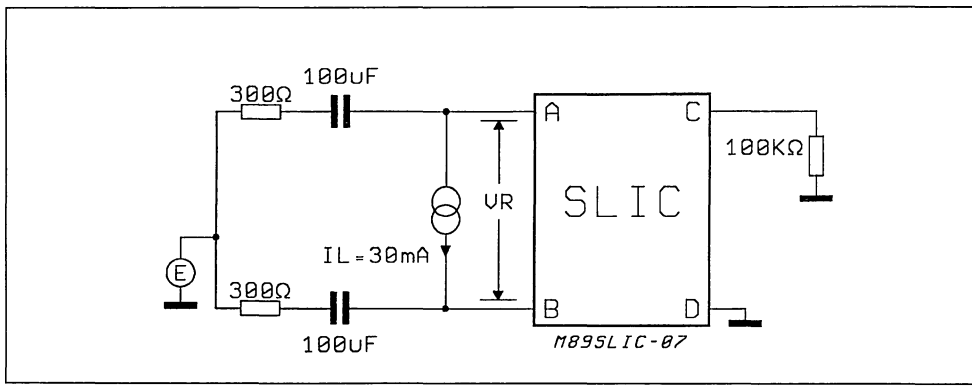
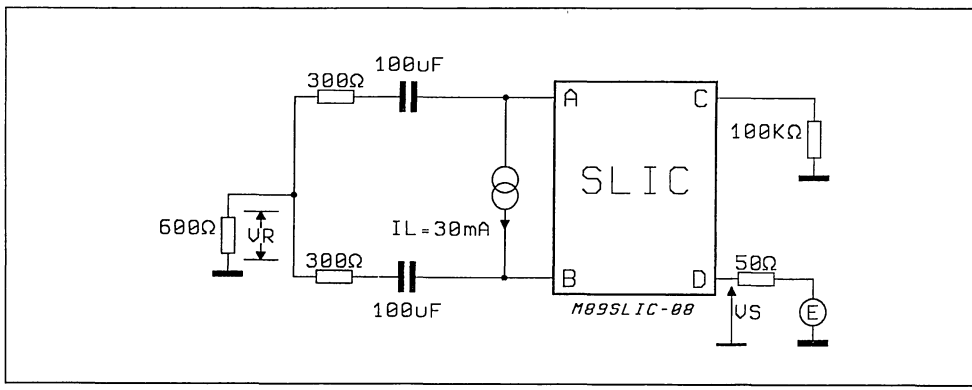


Figure 8 : Transversal to Longitudinal Conversion.



TEST CIRCUITS (continued)

Figure 9 : TTX Level at Line Terminals.

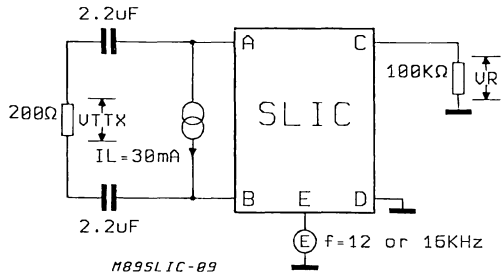
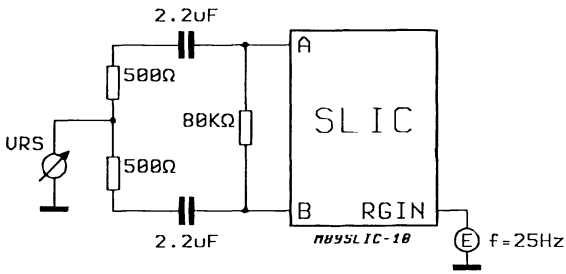


Figure 10 : Ringing Simmetery.



APPENDIX B

ADDITIONAL OPERATING FEATURES

Two further operating modes are provided on the L3091, boosted battery and ring pause. Both of these Modes are accessed by applying a high impedance on inputs AUT and or RNG of the digital interface.

1. BOOSTED BATTERY (BB)

This operating mode is equivalent to conversation mode with respect to AC and signalling functions but with the following changes to the DC characteristics :

(a) Current limiting value is fixed at 25mA.

(b) Characteristic in the resistive feeding region corresponds to a battery voltage equal to (-15+ |VB-| + VB+) Volt in series with the same feeding resistor utilized in the DC characteristic of conversation mode.

BB mode is typically used to feed long lines (20mA/4KΩ) and to implement special functions such as message waiting where high voltage signals are required.

Further information about this operating mode may be found by referring to the L3000/L3030 datasheet.

2. RINGING PAUSE MODE

During Ring Pause - Mode the SLIC is always in ringing mode but the AC ringing signal is not injected into the line. This mode is used in applications where it is mandatory to avoid perturbations on adjacent lines during ringing injection.

Further information about this operating mode may be found by referring to the L3000/L3030 datasheet.

The following table shows all operating modes of L3000/L3091 SLIC KIT. Boosted Battery or Ringing Pause Modes are selected by applying a high impedance (HI) to input pins RNG and/or AUT.

Included also in this table are the operating modes to which the SLIC defaults automatically during ringing mode when OFF HOOK is detected.

CONTROL INTERFACE BETWEEN THE SLIC AND THE CARD CONTROLLER

Operating Mode	Input Pin				Output Pin	
	RNG	PWON	AUT	LIM	ONHK	GDK
Conversation 25mA	0	1	1	X	1 on-hook 0 off-hook	1 Ground key not detected. 0 Ground key detected.
Conversation 42mA	0	1	0	1		
Conversation 62mA	0	1	0	0		
Boosted Battery 25mA	0	1	HI	X		
Stand-by	0	0	0	X		Disable
Automatic Stand-by	1	0	1	X		
Power-down	1	0	0	X	C1 Comparator Output	Disable
Test Mode	0	0	1	X	1 on-hook 0 off-hook	0 Limiting Region 1 Resistive Region
Ringing Inj. (CVS 25mA)	1	1	1	X	1 on-hook 0 off-hook	Disable
Ringing Inj. (CVS 42mA)	1	1	0	1		
Ringing Inj. (CVS 62mA)	1	1	0	0		
Ringing Inj. (BB 25mA)	1	1	HI	X		
Ringing Pause (CVS 25mA)	HI	1	1	X		
Ringing Pause (CVS 42mA)	HI	1	0	1		
Ringing Pause (CVS 62mA)	HI	1	0	0		
Ringing Pause (BB 25mA)	HI	1	HI	X		

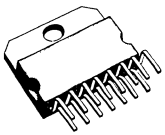
NB : HI = High Impedance.
BB = Boosted Battery.

SGS-THOMSON MICROELECTRONICS

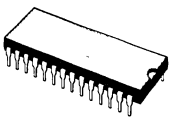
TDB7711
TDB7722

SUBSCRIBER LINE INTERFACE CIRCUIT KIT

- PROGRAMMABLE DC FEEDING RESISTANCE AND LIMITING CURRENT (seven values)
- LONGITUDINAL BALANCE PERFORMANCE : UP TO 63 dB
- FOUR OPERATING MODES (power-down, stand-by, conversation, ringing control)
- POWER SAVING FEATURE
- SIGNALLING FUNCTION (off-hook/ground key)
- HYBRID FUNCTION
- EXTERNAL RINGING ALLOWING BALANCED AND UNBALANCED RINGING WITH ZERO CROSSING INJECTION AND RING TRIP DETECTION
- AUTOMATIC RINGING STOP WHEN OFF-HOOK IS DETECTED
- LOW POWER CURRENT CONSUMPTION IN STAND-BY MODE (90 mW)
- LOW NUMBER OF EXTERNAL COMPONENTS. THESE COMPONENTS REQUIRE ONLY STANDARD TOLERANCE : 1 % RESISTORS AND 10-20 % CAPACITORS
- POSSIBILITY TO WORK WITH HIGH COMMON MODE CURRENTS
- TELETAXE
- ANALOG INPUT/OUTPUT
- GENERAL PURPOSE BIT
- INTEGRATED THERMAL PROTECTION



Multiwatt 15

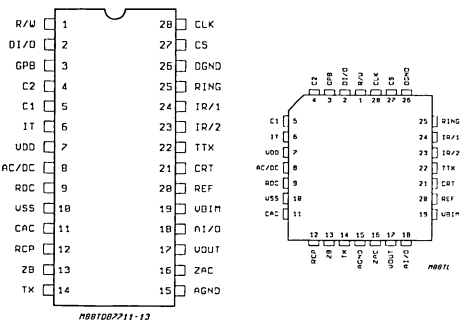


DIP28

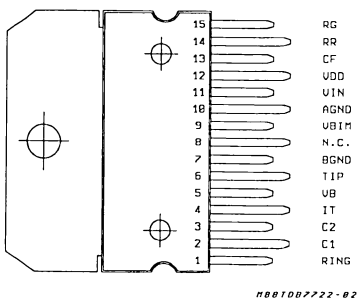
PLCC28

ORDER CODES : TDB7722 (Multiwatt 15)
TDB7711 (DIP28)
TDB7711 (PLCC28)

PIN CONNECTION



TDB7711



TDB7722

DESCRIPTION

The ST SLIC KIT (TDB7722/7711) is a set of solid state devices designed to integrate the main functions needed to interface a telephone line.

It consists of 2 integrated devices : the TDB7722 line interface circuit and the TDB7711 control unit. This kit performs main of the BORSHT functions :

- Battery feed
- Overvoltage protection with double trisil device and 2 protection resistors
- Ringing control
- Signalling
- Hybrid

The ST SLIC KIT has been designed to achieve performant transmission characteristics like excellent longitudinal balance and very low consumption.

In addition, this kit controls an external ringing relay with zero crossing injection.

This kit is fabricated using a 80 V Bipolar, junction isolated technology, with accurate thin film resistors for the TDB7722 and a 10 V Bipolar I2L technology for TDB7711.

This kit is suitable for all applications, C.O or PBX, where balanced or unbalanced ringing are requested.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{b-}	Negative Battery Voltage	72	V
V_{dd}	Positive Supply Voltage	+ 5.5	V
V_{ss}	Negative Supply Voltage	- 5.5	V
V_{agnd}-V_{bgnd}	Maximum Voltage Between Analog GND and Battery GND	± 2	V
T_j	Maximum Junction Temperature	+ 150'	'C
T_{stg}	Storage Temperature	– 55' to 150'	'C

THERMAL DATA

TDB7722 HIGH VOLTAGE

R_{thjc}	Max. Resistance Junction to Case	3	'C/W
R_{thja}	Max. Resistance Junction to Ambient	40	'C/W

TDB7711 LOW VOLTAGE

R_{thja}	Max. Resistance Junction to Ambient	80	'C/W

OPERATING RANGE

Symbol	Characteristics	Min.	Typ.	Max.	Unit.
T_{oper}	Operating Temperature Range	0		70	'C
V_{b-}	Negative Battery Voltage	– 72		– 20	V
V_{dd}	Positive Supply Voltage	+ 4.5		+ 5.5	V
V_{ss}	Negative Supply Voltage	– 5.5		– 4.5	V
I_{max}	Total Line Current			120	mA

PIN DESCRIPTION

TB7722

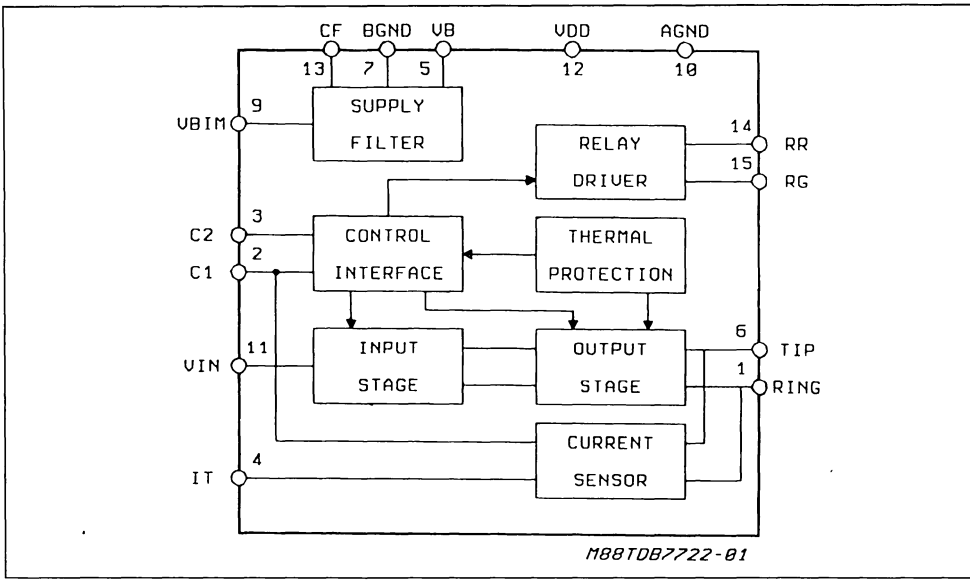
N'	NAME	DESCRIPTION
1	RING	B Line Termination Output with Current Capability up to 120 mA (I_b is the current sunk into this pin).
2	C_1	Digital signal input (3 voltage levels) that defines device status with pin 3. Longitudinal current is also provided.
3	C_2	Digital signal input (3 voltage levels) that defines device status with pin 2. Thermal warning current is also provided by TDB7722 through this pin.
4	I_T	High precision scaled transversal line current signal. It is a current generator referred to AGND. $I_T = \frac{I_a + I_b}{200}$.
5	V_B	Negative Battery Supply Voltage.
6	TIP	A Line Termination Output with Current Capability up to 120 mA (I_A is the current sourced from this pin).
7	BGND	Battery Ground Relative to V_B^- Supply Voltage. It is also the reference ground for TIP and RING signals.
8	NC	Not connected, this pin is connected to internal circuitry and should not be used as a tiepoint for external circuitry.
9	V_{BIM}	This voltage output provides $V_{REF}/40$ Voltage to TDB7711 V_{REF} : Filtered Battery Voltage - (!V_{BAT}!-2.1 V)
10	A_{GND}	Analog ground, all input signals and V_{DD} supply voltage must be referred to this pin.
11	VIN	2 Wire Unbalanced Voltage Input
12	V_{DD}	Positive Power Supply + 5 V
13	CF	An external capacitor connected between this pin and BGND filters battery noise.
14	RR	Ring relay driver : output used to drive a 5 V or 12 V external ring relay.
15	RG	Ring Relay Ground

PIN DESCRIPTION

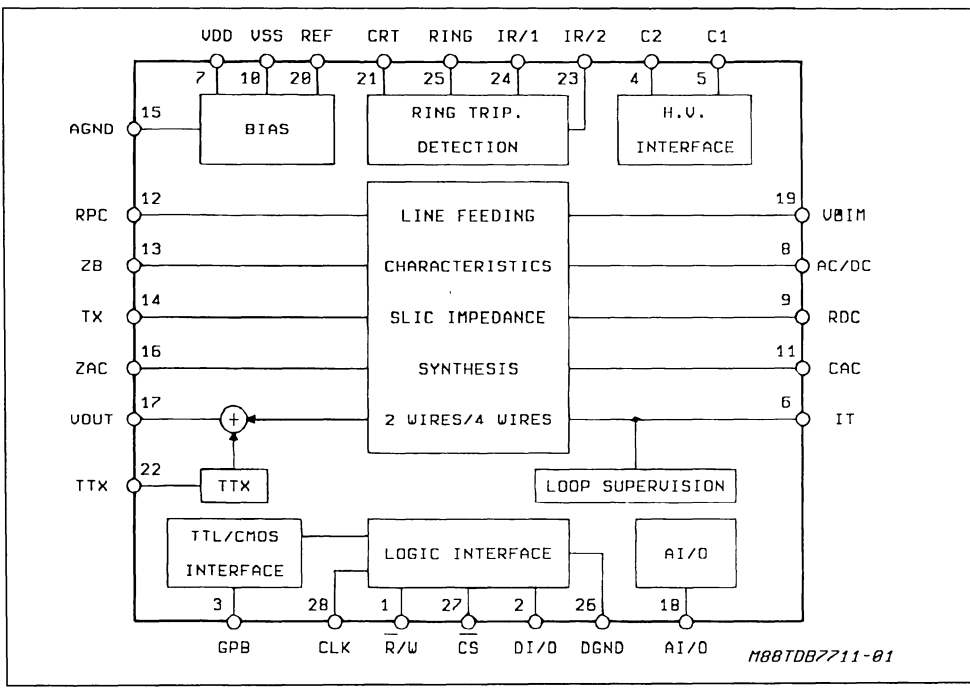
TB7711

N'	NAME	DESCRIPTION
1	$\overline{R}$/W	Read/Write Command of the Serial Digital SLIC Control
2	DI/O	Data Input/output for SLIC Serial Control
3	GPB	General Purpose Bit. TTL/CMOS Output Available for any Specific Application.
4	C2	State control signal output (3 voltage levels) used also as thermal warning current input from TDB7722.
5	C1	State controll signal output (3 voltage levels) used also as scaled tranversal line current input from TDB7722. C1 and C2 combination defines operating mode of the high voltage part.
6	I_T	Scaled down Transversal Line Current Input $I_T = \frac{I_a + I_b}{200}$.
7	V_{DD}	Positive Supply Voltage, + 5 V.
8	AC/DC	AC-DC Feedback Input.
9	RDC	DC Feeding System.
10	V_{ss}	Negative Supply Voltage, – 5V.
11	CAC	AC Feedback Input.
12	RPC	AC Line Impedance Adjustment.
13	ZB	Tx amplifier negative input performing the two to four wire conversion.
14	Tx	Transmit Amplifier Output.
15	AGND	Analog Ground. V_{DD} and V_{SS} supply voltages are referenced to this pin.
16	ZAC	AC Line Impedance Synthesis.
17	VOUT	Two wire unbalanced output carrying out following signals : - DC voltage to perform the proper DC characteristic - Voice signal - Teletax
18	AI/O	Programmable analog input/output pin, used to feed the SLIC with a low voltage battery offering power saving capability. Also used to detect line short circuits.
19	V_{BIM}	V_{REF}/40 Voltage Input from TDB 7722.
20	REF	Bias Setting Pin
21	C_{RT}	Ringing filter Capacitor used also to filter longitudinal current and to shape teletax signal.
22	TTX	Teletax Signal Analog Input.
23	IR/2	Differential line current inputs in ringing network.
24	IR/1	
25	RING	Ringing Signal Input for Synchronisation.
26	DGND	Digital Ground
27	$\overline{CS}$	Chip Select Input
28	CLK	Clock 128 kHz

TDB7722 BLOCK DIAGRAM



TDB7711 BLOCK DIAGRAM



FUNCTIONAL DIAGRAM

Figure 1 : Simplified Block Diagram.

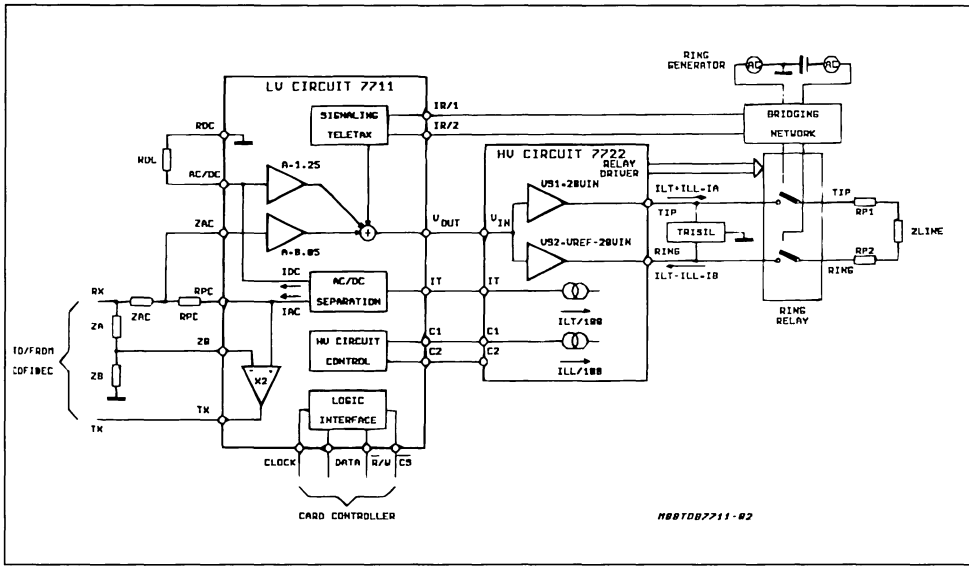


Figure 2 : Functional Diagram - DC Path.

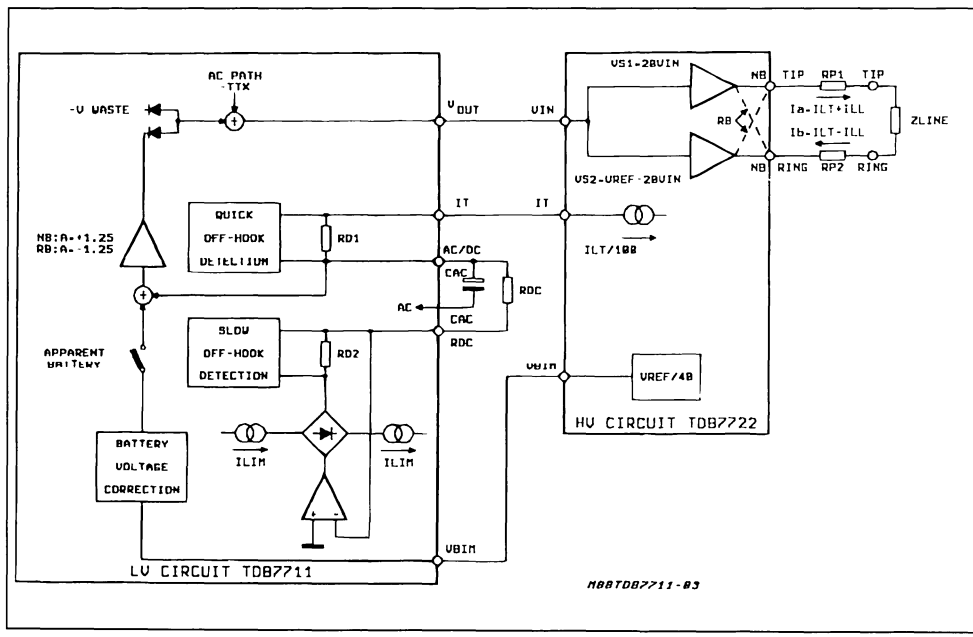


Figure 3 : Functional Diagram - AC Path.

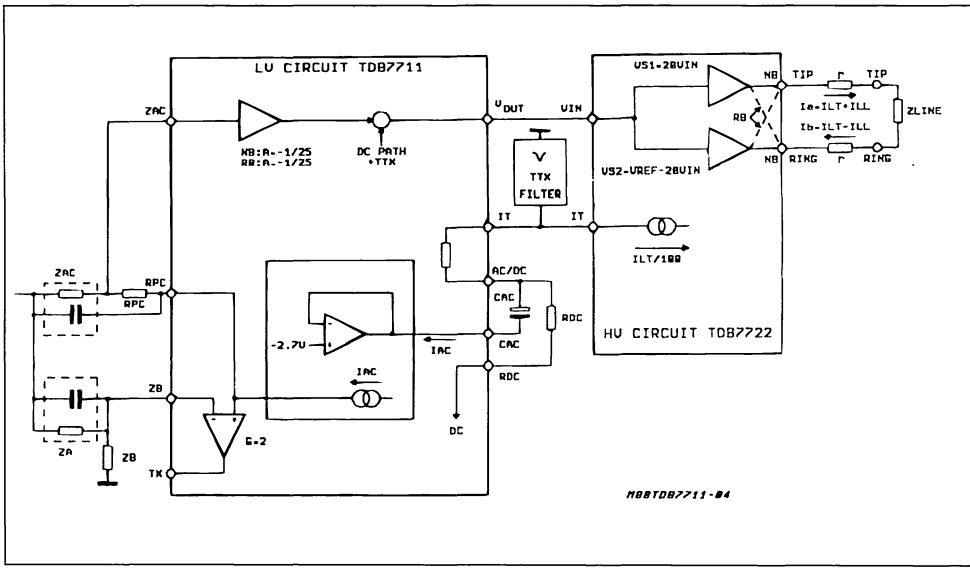
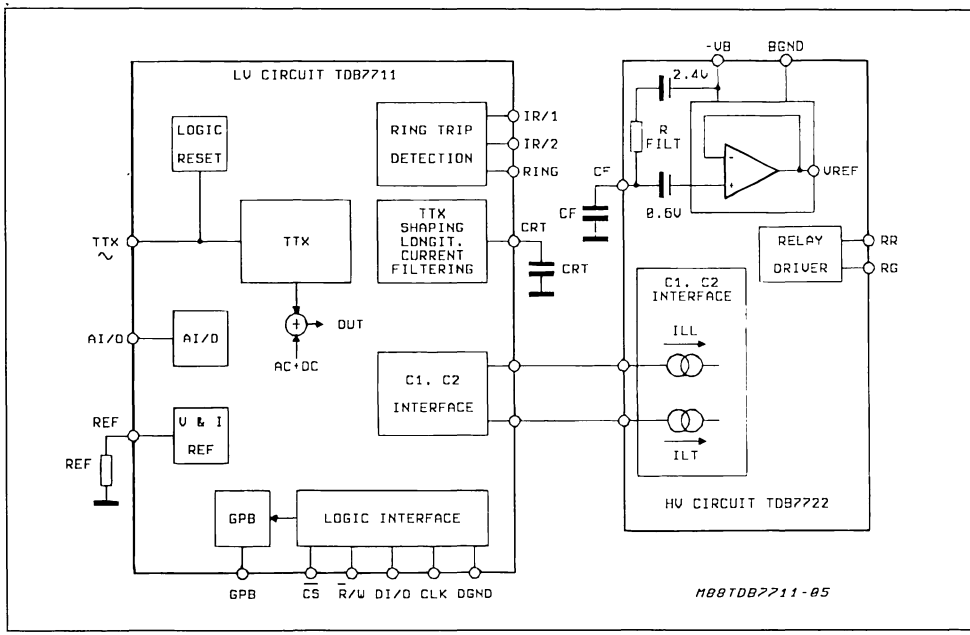


Figure 4 : Functional Diagram - Ringing and Miscellaneous Functions.



FUNCTIONAL DESCRIPTION

TDB7722 - HIGH VOLTAGE CIRCUIT

The TDB7722 line interface provides a battery feeding and drives a ring relay.

The TDB7722 contains a state decoder which is under control of the low voltage TDB7711. This decoder selects :
- one of the following operational modes : power down, stand-by, conversation, ring relay control, power saving
- direct or reverse battery operation.

The circuit makes the sum and difference of the two wire currents (I_a, I_b) to provide the transverse and longitudinal components to the LV SLIC (Scaled down : 1/100).
The scaled down transverse current flows by I_T pin.
The scaled down longitudinal current flows by C_1 pin.
In addition, TDB7722 provides thermal warning current to the low voltage chip via pin C_2.

The TDB7722 amplifies both the AC and DC signals entering pin 11 (VIN).
Separate grounds are provided :
- analog ground as a reference for analog signals
- battery ground as a reference for the output stages

TDB7711 - LOW VOLTAGE CIRCUIT

1) The TDB7711 low voltage control unit controls TDB7722 line interface module, giving the proper informations to set line feed characteristics (drop voltage mode, feed resistance mode, current limitation) for several working modes :
- apparent battery
- real battery
- special DC characteristic

2) The transmission characteristics of the SLIC are the following :
- a 2/4 wires conversion
- longitudinal current rejection
- based on TDB7722 informations and external components configuration, the TDB7711 handles the impedance synthesis and hybrid balance

3) Signalling features are :
- teletax (shaping and filtering)
(described in application note AN298)
- ring trip detection
(described in application note AN298)
- pulse dialing
- ground key detection

4) Other features
- analog input/output pin
(described in application note AN298)
- general purpose bit
(described in application note AN298)
- interface with the card controller through a 4 wire serial bus
- thermal warning

WORKING STATES OF THE KIT

In order to carry out the various operation modes, the ST SLIC kit has several different working states. Each mode, externally selected by microcontroller, is defined by the voltage respectively applied by pins 5 and 4 of TDB7711 to the pins 2 and 3 of TDB7722.

Three different voltage levels (1.4 ; 0 ; + 1,4) are available at each connection, defining all possible states as listed in table 1.

		C1			
		Pin 5 of TDB7711			Pin 2 of TDB7722
			+ 1.4	0	– 1.4
C2	Pin 4 of TDB7711	+ 1.4	Power Down	Reverse Battery	Not Allowed
	Pin3 of TDB7722	0	Power Down	Normal Battery	Ringing
		– 1.4	Power Down	Standby	Not Allowed

Appropriate combinations of two pins define the four possible status of the kit, that are :

a) Stand-by (SBY)
b) Conversation (CVS)
c) Ringing (RING)
d) Power down (PD)

The main difference between stand-by and power down is that in SBY the power consumption on the voltage battery V_B– (– 48 V) is reduced but the SLIC can feed the line, recognize the on-hook, off-hook status and ground key status.

In power down, the power consumption is closed to zero, tip and ring terminals are in high impedance and all line detection circuits are disabled.

The SBY status should be used when the telephone is in on-hook and PD status only in emergency condition when it is mandatory to cut any possible power dissipation with no running operation.

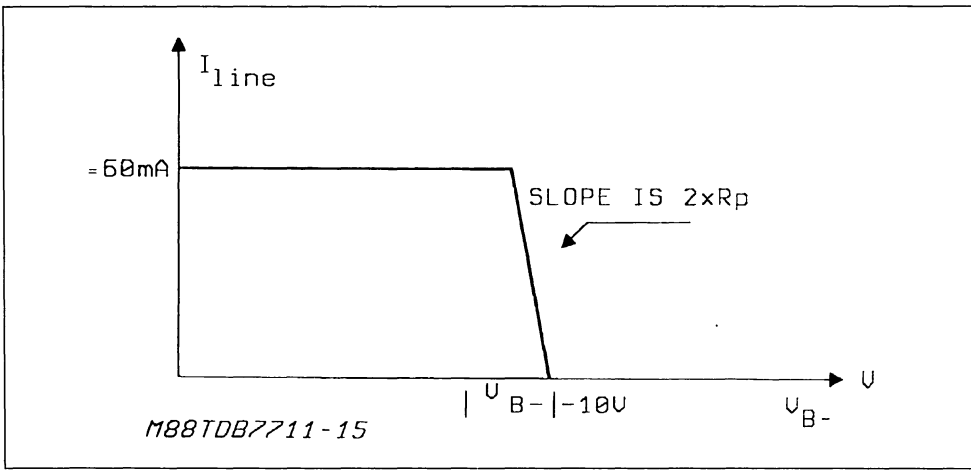
OPERATION MODES

STAND-BY (SBY) MODE. In this mode, most of the functions of both low voltage and high voltage circuit are not active in order to reduce the power consumption.

The only working functions are following :

* Line feeding

- line voltage |Vbat| – 10 V
- current supplied to the line limited to 60 mA
- output resistance = protection resistance (Rp)



* On/off hook detection

The current of the 2 wires are sensed and the scaled down transverse current is provided to low voltage SLIC for signalling detection.

In this mode, the polarity of the battery should be direct (TIP wire more positive than RING one).

When the SLIC is set in SBY mode, the power dissipation of TDB7711/TDB7722 kit is 90 mW.

CONVERSION (CVS) MODE. This operation mode is set when the off-hook condition has been recognized.

As far as the DC characteristic is concerned, three different feeding conditions are present :

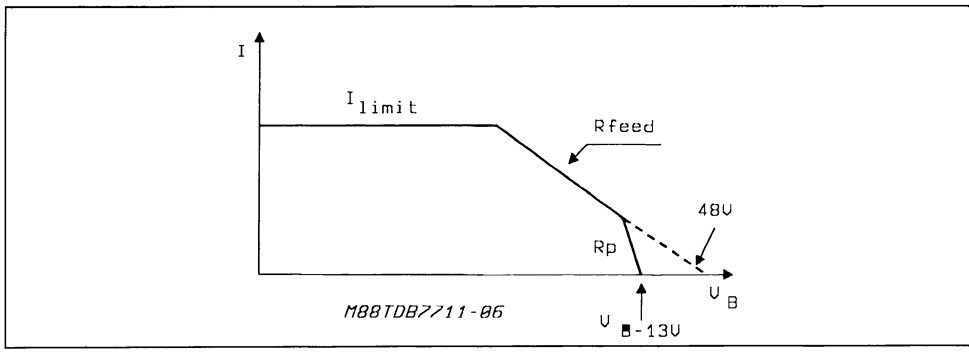
a) Current limiting region
The DC impedance of the SLIC is very high (> 20 Kohms) and therefore the system works like a current generator.
The limiting current is defined by programmation via the logic interface and selected among the seven following values :
12 mA, 20 mA, 30 mA, 32 mA, 42 mA, 50 mA, 62 mA

b) A standard resistive feeding mode
The characteristic is :
V_{BAT} minus a voltage equal to R_{feed} x I_{line} with R_{feed} defined by external resistor RDC (RDC = 2 (R_{feed} Rp))

c) A nearly constant voltage mode
The voltage value is $|V_{BAT}| - 13$ V. This 13 V drop voltage allows the output amplifiers to keep a good linearity.
For $|V_{BAT}| > 48 + 13 = 61$ V, this mode does not exist.

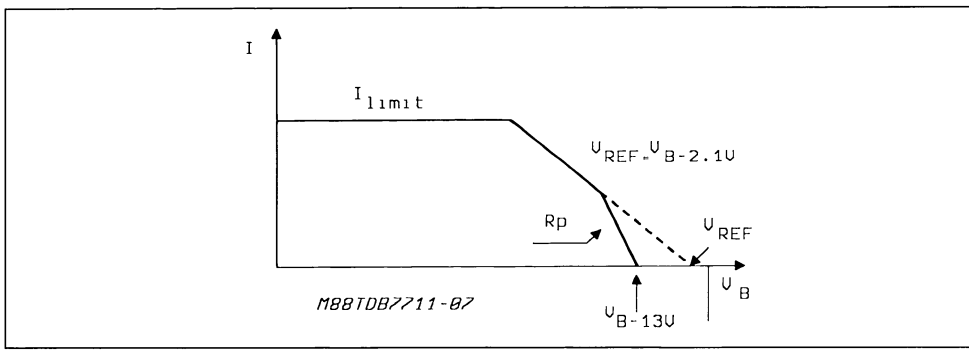
The three different feeding conditions are applicable or not in the three different following feeding modes. These three feeding modes are controlled by the two digital eight bits word written in the low voltage circuit.

1) Apparent Battery.



In this mode, the three feeding conditions are available, the line sees an apparent voltage of 48 V whatever the actual battery voltage is.

2) Real Battery.



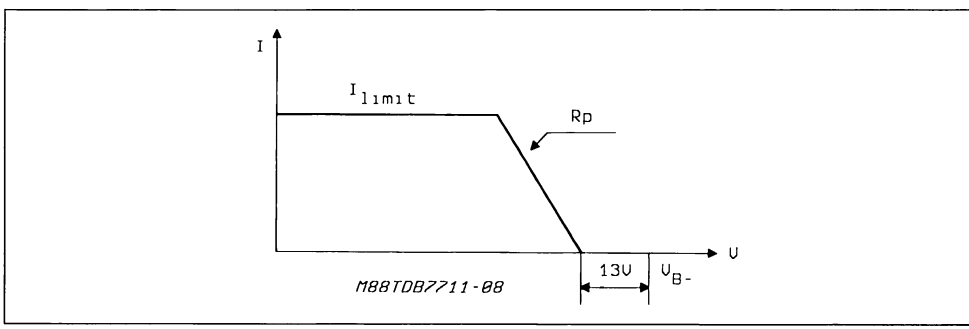
This solution is same as apparent battery except for the standard resistive mode where the voltage value is :

$|Vline| = |V_{REF}| - Rfeed \times Iline$

with $|V_{REF}| = |V_{B-}| - 2{,}1\ V$

Therefore the line voltage depends on the current battery voltage V_B.

3) Special Characteristic.



In this mode, there is no standard resistive feeding region. This mode is specially suitable for PBX applications.

The three feeding modes above can operate either in normal polarity or in reverse polarity.

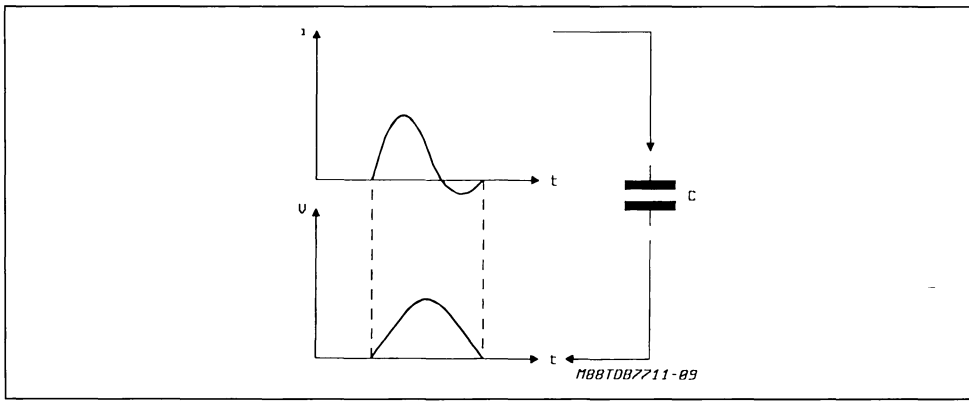
RINGING MODE (RING). When ringing, the SLIC must be in normal battery mode.
An external circuit applies ringing signal through the ringing network and the ring relay.
This circuit consists of a balanced or unbalanced sinus generator (70 to 100 VRMS) in serie with the battery (– 48 V).
When the ringing control is selected (by software), ring relay is energized at the zero crossing point of the ringing generator. The ring relay is disenergized either when ring trip is detected or by software, using one bit of the second byte written in the SLIC (see page 13: data input).

There is a sophisticated ring trip detection circuitry insensitive to parasitic noise on the line. The ring trip principle is as follows :

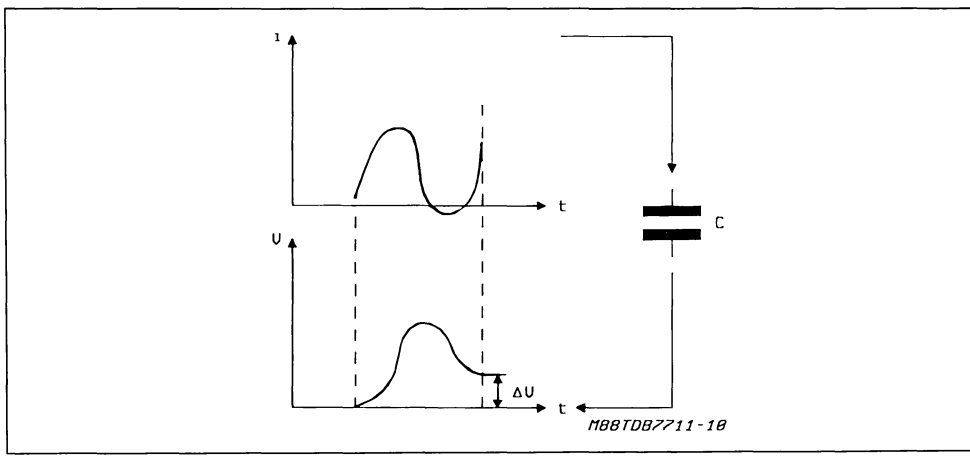
- the line current is sensed by a resistive network, not sensitive to longitudinal current.
- a fraction of the line current is sent in a capacitor during one period of the ringing signal.
- V is measured at the beginning and at the end of the period.

2 cases :

1) No Voltage Difference and Therefore No DC Component Exists in Line Current.



2) Voltage Difference and Therefore a DC Component Exists in Line Current.



POWER DOWN MODE (PD). In case of overtemperature or on logic control (see page 13: data output) the high voltage SLIC TDB7722 can be set in power down mode. In this case, the power consumption is very low, the line drivers amplifiers (TIP and RING) are set in high impedance state and cannot deliver any current.

DIGITAL CONTROL INTERFACE

The programmable functions of the SLIC are set by the contents of two 8-bits registers in the TDB7711 (low voltage) chip.

Connection between TDB7711 and the card controller is realized through a 4-wire serial bus.

The four pins have following functions :

$\overline{CLK}$: Shift Clock (128 kHz max)
$\overline{CS}$: Chip select (active low)
DI/O : Bidirectional pin : data-in (2 bytes), data-out (12 bit word)
$\overline{R}/W$: Read (if "o") or write (if "1")

The datas are shifted into the low voltage TDB7711 on the rising edge of each CLK pulse, if CS = 0 and $\overline{R}/W = 1$.

The datas are shifted out from TDB7711 on the rising edge of each CLK pulse, if $\overline{CS} = 0$ and R/W = 0.

The first bit B0 can even be read without any CLK pulse, as soon as $\overline{CS} = 0$ and $\overline{R}/W = 0$.

This bit is read again, as B0, upon the first CLK rising edge of a read operation.

When $\overline{CS} = 1$, the DI/O pin is in high impedance, allowing several SLICS to share the same data link.

Data input

Two bytes can be written into the SLIC to program its registers.

B0 = 0 = First Byte Selected		Note 2
B1 = Standby	0 = Power up 1 = Standby	
B2 = Normal/Special Characteristic	0 = Normal 1 = Special	
B3 = Real/Apparent Battery	0 = Apparent 1 = Real	
B4 = Current Limitation 1	0 = 0 mA 1 = 30 mA	Note 1
B5 = Current Limitation 2	0 = 0 mA 1 = 20 mA	Note 1
B 6 = Current Limitation 3	0 = 0 mA 1 = 12 mA	Note 1
B 7 = Validation	0 = This word is not stored into the SLIC 1 = This word is stored into the SLIC on rising edge of $\overline{CS}$	

Notes : 1. The current values can be added Therefore seven values are available from 12 mA to 62 mA.
2 The B0 bit is always the first bit shifted into or shifted out from the DI/O pin
3. The SLIC is set in POWER DOWN mode if B1 = 1 and B4 = B5 = B6 = 0.

B0 = 1 = Second Byte Selected	Note 1
B1 = General Purpose Bit	0 = Low Level Voltage on GPB Pin 1 = High Level Voltage on GPB Pin
B2 = Analog Input/Output Pin	0 = Input Mode 1 = Output Mode
B3 = Teletax	0 = Teletax Off 1 = Teletax On
B4 = Direct/Reverse Battery	0 = Direct Battery 1 = Reverse Battery
B5 = Ringing	0 = Ringing Off 1 = Ringing On
B6 = TTX Drop Voltage Variation	0 = Variation 1 = No Variation
B7 = Validation	0 = This word is not stored into the SLIC 1 = This word is stored into the SLIC upon rising edge of $\overline{CS}$

Note : 1 The B0 bit is always the first bit shifted into or shifted out from the DI/O pin.

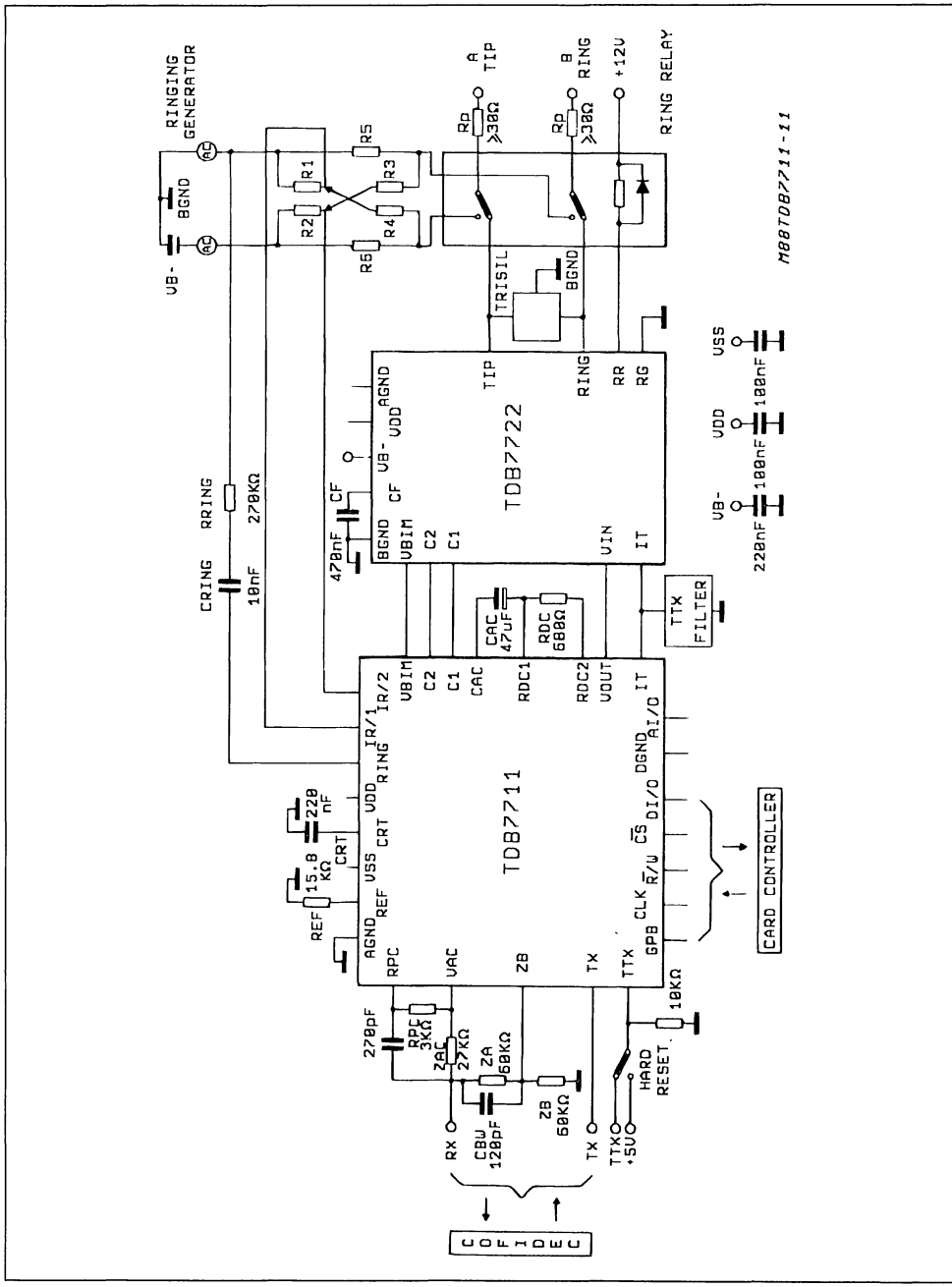
Data output

One twelve bit word can be read from the SLIC.

B0 = Hook Status (HS)	0 = On Hook Status 1 = Off Hook	Note 1
B1 = Comparison Result Bit (CRB)	0 = !line voltage! > voltage set on AI/O pin 1 = !line voltage! < voltage set on AI/O pin	
B2 = Ground Key (GK)	0 = No Ground Key 1 = Ground Key	
B3 = Thermal Warning (TW)	0 = Normal 1 = HV Circuit Temperature > 150' C	
B4 to B11 = Last byte written into the SLIC for checking		

Note : 1. The B0 bit is always the first bit shifted into or shifted out from the DI/O pin.
Reset : The logic circuitry is automatically reset at power on, or by hardware, when applying the V_{DD} voltage on the TTX pin

APPLICATION DIAGRAM



EXTERNAL COMPONENTS LIST

TDB7722 (high voltage)

Component		
Ref	**Value**	**Function**
RP CF	> = 30 OHMS 470 nF/100 V (20 %)	Protection Resistor Battery Voltage Rejection

TBD7711 (low voltage)

Component		
Ref	**Value**	**Function**
REF	15.8 Kohms (1 %)	Bias Resistor
RDC	680 ohms	Feeding Bridge Resistor
CAC	47 µ F/10 V (20 %)	AC Path Decoupling
ZAC	27 Kohms (Z0 = 600 ohms)	Scaled AC Impedance
RPC	3 Kohms (Rp = 30 ohms)	PTC Resistor Compensation
ZA	60 Kohms (Z0 = 600 ohms)	SLIC Impedance Balance Network
ZB	60 Kohms (Z0 = 600 ohms)	Line Impedance Balance Network
CBW	270 pF/10 V (10 %)	Bandwith Capacitor
C'BW	120 pF/10 V (10 %)	Bandwith Capacitor Compensation
CRT	220 nF/10 V (20 %)	Ring Trip Capacitor
R1 to R4 R5 and R6	560 Kohms (5 %) 220 ohms/2 W	Line Current Sensing During Ringing
RRing	270 Kohms (10 %)	Ring Generator Zero Crossing Detection
CRING	10 nF (20 %)	Ring Generator Zero Crossing Detection

Note : For external components definition, please refer to application note AN298

ELECTRICAL OPERATING CHARACTERISTICS

The characteristics apply when the application diagram (see figure 1) has nominal value of typical external components and unless otherwise specified :
T_{amb} = 25 °C, V_B = – 30 to – 72 V, V_{DD} = + 5 V ± 5 %, V_{SS} = – 5 V ± 5 %
Transverse Line Current (I_{LT}) = 30 mA

LINE FEEDING CHARACTERISTICS

Symbol	Parameter		Min.	Typ.	Max.	Unit.
I_{lim}	Loop Current at Constant Current Feed	– Range – Accuracy	12 – 0		62 + 10	mA %
R_{feed}	Feed Resistance	– Range – Accuracy	300 – 5		1000 + 5	Ω %
V_{app}	Apparent Battery Voltage		– 50.4	– 48	– 45.6	V

ELECTRICAL OPERATING CHARACTERISTICS (continued)

SIGNALLING

Symbol	Parameter			Min.	Typ.	Max.	Unit.
I_H (off)	Off Hook Detection Threshold	Power up or Power Down		5		8	mA
I_H (on)	On Hook Detection Threshold	Power up or Power Down		4		7	mA
I_H (hys)	Off/On Hook Hysteresis				1		mA
	Dialing Distortion					3	ms
	Off Hook Reponse Time	Transverse Line Current I_{LT} = 20 mA Power Down				70	ms
I_{GK} (on)	Ground Key Detection Threshold			3.5		7	mA
	Ground Key Detection Reponse Time	Longitudinal Line Current I_{LL} = 20 mA				250	ms
I_R (ton)	Ring Trip Detection Threshold			5		10	mA
F_R	Ringing Frequency			16		70	Hz
	Ring Trip Delay	I_{LT} = 15 mA				4/FR	s
V_{TTX}	Teletax Sending (with TT_X Filter) F ≤ 18 kHz		Line Level	2.2		2.5	V_{rms}
G_{TTX}	R_L = 200 Ω		Gain	7	8	9	

2 WIRE PORT TRANSMISSION

Symbol	Parameter		Min.	Typ.	Max.	Unit.
	Overload Level	100 < F < 4000 Hz	6			dBm
	Return Loss	300 < F < 3400 Hz	20			dB
	Longitudinal Impedance	On or Off Hook R_p = Protection Resistance	r − 10		r + 10	Ω per wire
	Longitudinal Balance Conversation Mode	Off-Hook 200<F<1000Hz Off-Hook F=3000Hz On-Hook 200<F<3400	58 53 50	63 58 53		dB
	Longitudinal Signal Generation	100 < F < 3400 Hz	52	60		dB
	Longitudinal Handling Capability		35			mArms

ELECTRICAL OPERATING CHARACTERISTICS (continued)

4 WIRE PORT TRANSMISSION

Symbol	Parameter		Min.	Typ.	Max.	Unit.
	Overload Level	On RX On TX	3 3			dBm dBm
	TX Output Offset Voltage				100	mV
Z_{TX}	TX Output Impedance				10	Ω
G_{RX}	RX to Line Gain	F = 1020 Hz, V_{RX} = 0 dBm	−0.15	0	0.15	dB
G_{TX}	Line to TX Gain	V_{TX} = 0 dBm	−0.15	0	0.15	dB
	Frequency Response	300 < F < 3400 Hz	−0.1	0	0.1	dB
	Gain Linearity	F = 1020 Hz, V_{TX} or V_{RX} + 3 to − 40 dBm − 40 to − 50 dBm − 50 to − 55 dBm	 − 0.05 − 0.1 − 0.2		 0.05 0.1 0.2	 dB dB dB
	Transhybrid Loss	V_{RX} = 0 dBm 300 < F < 3400 Hz	 30		 40	 dB
THD	Total Harmonic Distorsion	F < 1020 Hz. 0 dBm	− 50			dB
Np	Psophometric Noise on TX, or on the Line		− 75			dBmp
PSRR	Power Supply Rejection Ratio	300 < F < 3400 Hz V_B V_{DD}, V_{SS}	− 34 − 20			dB dB

RELAY DRIVER

Symbol	Parameter		Min.	Typ.	Max.	Unit.
I_{sink}	Sink Current				100	mA
	Leakage Current				100	µA
	Voltage Drop	Switch On			1	V
	Breakdown Voltage	I_C = 200 µA	75			V

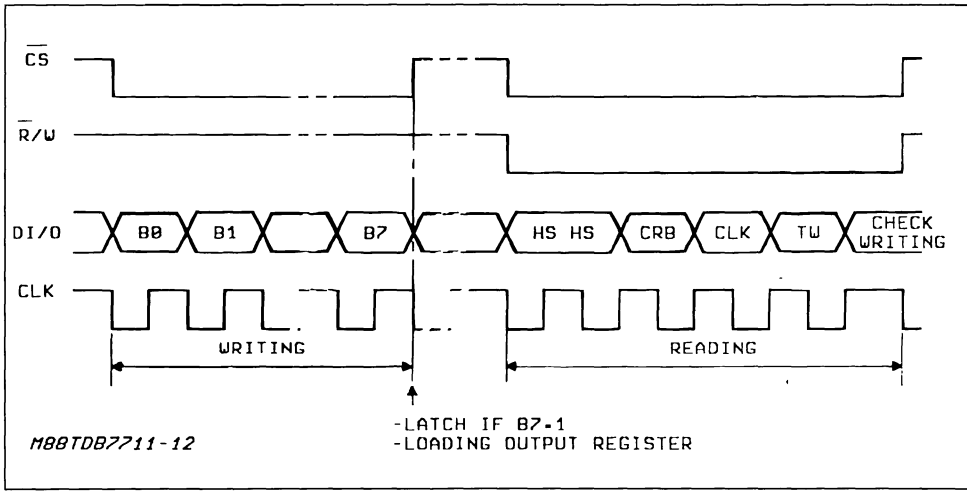
DIGITAL INTERFACE

Symbol	Parameter	Min.	Typ.	Max.	Unit.
	Clock Frequency		128	150	KHz

SUPPLY CURRENT

Symbol	Parameter		Min.	Typ.	Max.	Unit.
ICC^+	Positive Supply	Standby Power up			8 22	mA mA
ICC^-	Negative Supply Current	Standby Power up			6 24	mA mA
I_{BAT}	Battery Supply Current	Standby Power up			0.7 5	mA mA

TIMING DIAGRAM (controller to SLIC to controller)



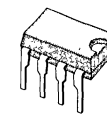
BATTERY FEED

AN AT & T PRODUCT

- BASIC BATTERY FEED FUNCTION AT A LOW COST
- HIGH AC IMPEDANCE CHARACTERISTICS FOR BALANCED LINE, DIFFERENTIAL-MODE, VOICE-BAND SIGNALS
- FULL INTERNAL LIGHTNING SURGE PROTECTION UP TO 4 AMPS
- DC VOLTAGE DROPS CAN BE ADJUSTED TO ACCOMODATE DIFFERENT PEAK SIGNAL LEVELS

DESCRIPTION

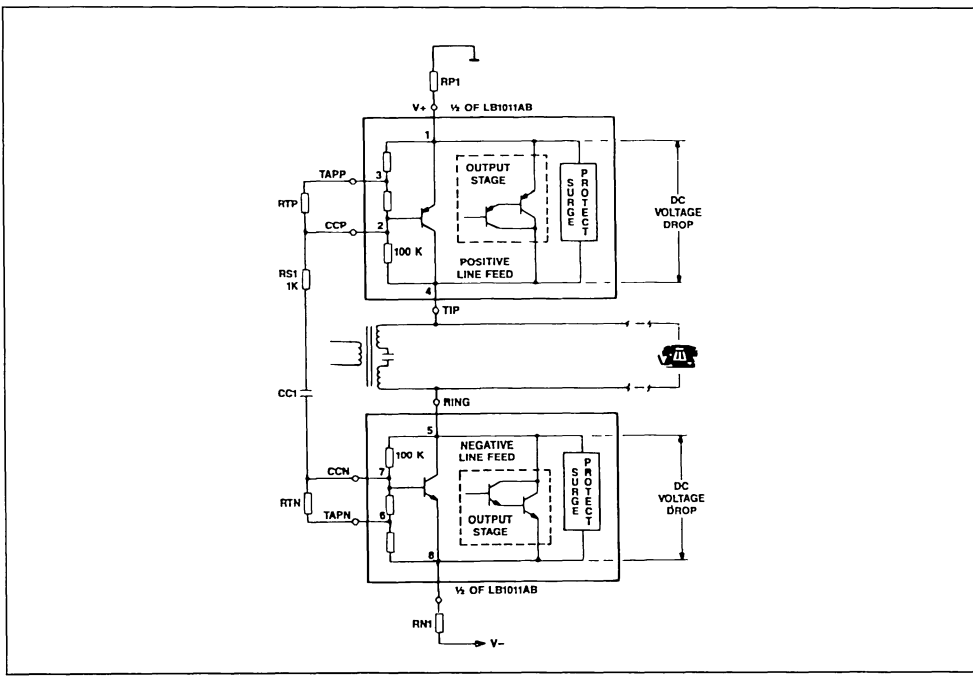
The LB1011 is an electronic battery feed circuit which supplies DC currents to a telephone line with minimal loading on the AC signals. The LB1011 is integrated as two complementary chips to supply DC currents of both negative and positive polarities to either balanced or unbalanced lines. In the balanced line application, this device helps to suppress undesirable common-mode signals.



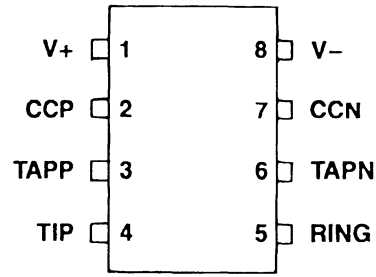
MINIDIP-A PLASTIC

ORDER CODE : LB1011AB

Figure 1 : Functional Diagram.



PIN CONNECTION



PIN DESCRIPTION

Pin	Name	Description
1	V+	This pin connects to the "most positive" external power supply (in some cases this is ground) through an external resistor. This external resistor is a factor in determining the amount of current which will be supplied by the "Positive Line Feed" output.
2 7	CCP CCN	"Cross-Coupling", Positive and Negative respectively. A capacitor between these two pins (for balanced line applications) creates a high AC impedance between TIP and RING. Since full Tip-to-ring voltage appears across these pins, it is recommended that a 1k ohm resistor be placed in series with the crosscoupling capacitor for surge protection purposes. Unbalanced line applications should connect the cross-coupling capacitor to ground so that the common-mode impedance of the output is greatly increased.
3 6	TAPP TAPN	Resistor tap pins. These terminals are used to adjust the "DC VOLTAGE DROP" across the "Positive Line Feed" and the "Negative Line Feed" respectively. The nominal "DC VOLTAGE DROP" is 3 volts when no resistors are connected between pins 2-to-3 or pins 6-to-7 respectively. A short circuit between these same pins will produce a nominal voltage drop of 4 volts. Resistors connected between these pins will produce voltage drops varying between 3 and 4 volts. A higher "DC VOLTAGE DROP" (greater than 3 volts) may be desirable for high operating temperatures, or when the peak value of the AC signals exceed 2.5 volts.
4	TIP	Output of the "Positive Line Feed Supply".
5	RING	Output of the "Negative Line Feed Supply".
8	V–	This pin connects to the "most negative" external power supply through an external resistor. This external resistor is a factor in determining the amount of current which will be supplied by the "Negative Line Feed" output.

ABSOLUTE MAXIMUM RATINGS (at 25°C unless otherwise specified)

Parameter	Value	Unit
Ambient Operating Temperature Range	– 20 to + 70	°C
Storage Temperature Range	– 40 to + 125	°C
Pin Soldering Temperature (t = 15 sec.)	300	°C

ELECTRICAL CHARACTERISTICS : (T_A = 25°C unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
DC Voltage Drop, Positive Line Feed	I_{V+} = 50mA (See Fig. 3)	2.50		3.50	V
DC Voltage Drop, Positive Line Feed, High-level Mode	I_{V+} = 50mA TAPP shorted to CCP (See Fig. 4)	3.75		4.85	V
DC Voltage Drop, Negative Line Feed	I_{V-} = – 50mA (See Fig. 3)	– 2.50		– 3.50	V
DC Voltage Drop, Negative Line Feed, High-level Mode	I_{V-} = – 50mA TAPN shorted to CCN (See Fig. 4)	– 3.60		– 4.00	V
Shunt Impedance	(See Fig. 14)	18			KΩ
Common Mode (longitudinal) Rejection	V_{IN} = 1.0Vrms, f = 1kHz RP1 = RN1 (see fig. 5) (See Fig. 12)	45			dB
Common Mode (longitudinal) Rejection, High-Level Mode	TAP shorted to CC V_{IN} = 1.0Vrms, f = 1kHz (See Fig. 12) RP1 = RN1 (see fig. 5)	45			dB
Distortion	V(TIP to RING) = 1.0Vrms (See Fig. 13)			2.0	%
Distortion, High-Level-Mode	TAP shorted to CC (See Fig. 13) V(TIP to RING) = 2.0Vrms			2.0	%

TEST SPECIFICATION (T_A = 25 °C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
V_{BEP}	PNP Base-Emitter Voltage	I_{PNP} = 50mA (See Fig. 2)	– 2.0	– 1.0	V
ΔV_{BEP}	PNP Base-Emitter Voltage Change	(See Fig. 2) $\Delta V_{BEP} = V_{BEP}(100mA) – V_{BEP}(50mA)$	– 250	– 25	mV
V_{BEN}	NPN Base-Emitter Voltage	I_{NPN} = 50mA (See Fig. 2)	1.2	2.0	V
ΔV_{BEN}	PNP Base-Emitter Voltage Change	(See Fig. 2) $\Delta V_{BEN} = V_{BEN}(100mA) – V_{BEN}(50mA)$	+ 25	+ 250	mV
V_{CEP}	PNP Collector-Emitter Voltage	(See Fig. 3)	2.5	3.5	V
V_{CEN}	NPN Colletor-Emitter Voltage	(See Fig. 3)	– 3.5	– 2.5	V
V_{BF}	BF Total Volts	I_1 = 50mA S1, S2 open (See Fig. 4)	5.0	6.8	V
ΔV_{BF}	BF Total Voltage Difference	I_1 = 100mA S1, S2 open (See Fig. 4) $\Delta V_{BF} = V_{BF}(100mA) – V_{BF}(50mA)$	– 400	+ 600	mV
V_{BF}	BF Total Volts (High Level Mode)	I_1 = 50mA S1, S2 closed (See Fig. 4)	7.2	9.4	V
ΔV_{BF}	BF Total Voltage Difference (High Level Mode)	I_1 = 100mA S1, S2 closed (See Fig. 4) $\Delta V_{BF} = V_{BF}(100mA) – V_{BF}(50mA)$	– 400	+ 600	mV
V_F	Forward Voltage	I_T = 200mA (See Fig. 5)		1.4	V

TEST SPECIFICATION (Continued)

Symbol	Parameter	Test Conditions		Min.	Max.	Unit
VF	Forward Voltage	I_T = 200mA	(See Fig. 6)		1.4	
		I_T = 75mA	(See Fig. 7)		1.4	
		I_T = 75mA	(See Fig. 8)		1.4	
		I_T = 75mA	(See Fig. 9)		1.4	
		I_T = 75mA	(See Fig. 10)		1.4	V
V_{BO}	PNPN Breakdown Voltage	I_T = 35mA	(See Fig. 5)	– 10	– 8	
V_S	PNPN Sustain Voltage	I_T = 200mA S1 closed	(See Fig. 6)	– 5	– 2	
V_{BO}	PNPN Breakdown Voltage	I_T = – 35mA S1 closed	(See Fig. 6)	– 10	– 8	
V_S	PNPN Sustain Voltage	I_T – 200mA S1 closed	(See Fig. 6)	– 5	– 2	
Z_S	Shunt Impedance	S1, S2 open Z_S(in ohms) = 100/V_M(in volt)	(See Fig. 11)	18		KΩ
Z_S	Shunt Impedance	S1, S2 closed Z_S(in ohms) = 100/V_M(in volt)	(See Fig. 11)	18		KΩ
L_B	Longitudinal Balance	S1, S2 open L_B = Log[V_M/V_{IN}] (in dB)	(See Fig. 12)	– 45		dB
L_B	Longitudinal Balance	S1, S2 closed L_B = Log[V_M/V_{IN}] (in dB)	(See Fig. 12)	– 45		dB
T_{HD}	Distorsion Test	S1, S2 open V_{IN} = 1V rms	(See Fig. 13)		2	%
T_{HD}	Distorsion High	S1, S2 closed V_{IN} = 2V rms	(See Fig. 13)		2	%

TEST CIRCUITS

Figure 2.

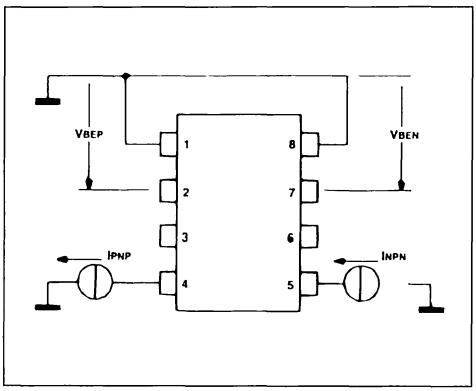


Figure 3.

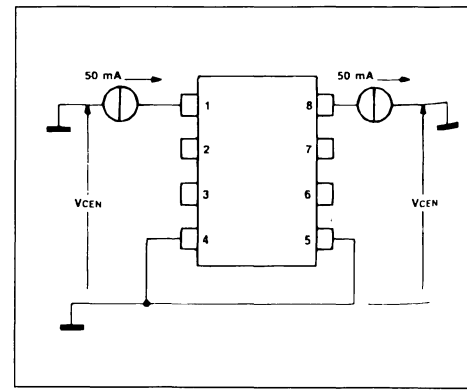


Figure 4 .

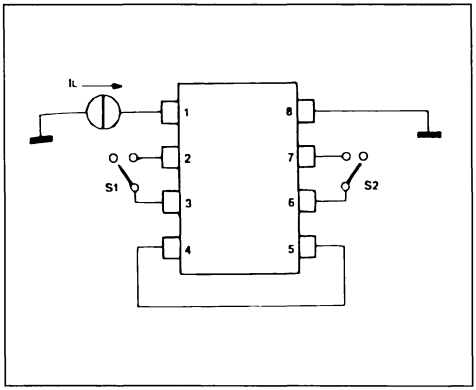


Figure 5.

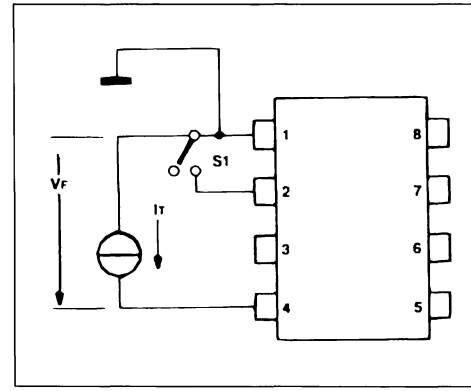


Figure 6.

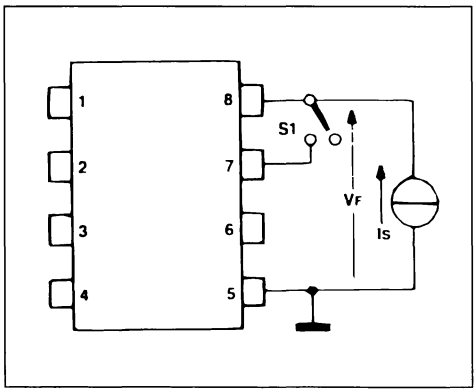


Figure 7.

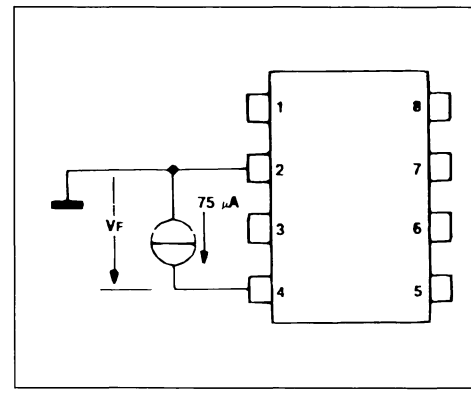


Figure 8.

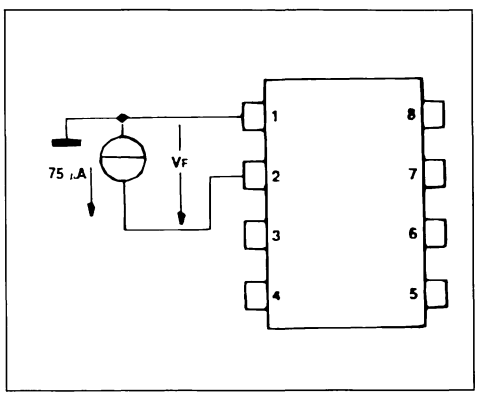


Figure 9.

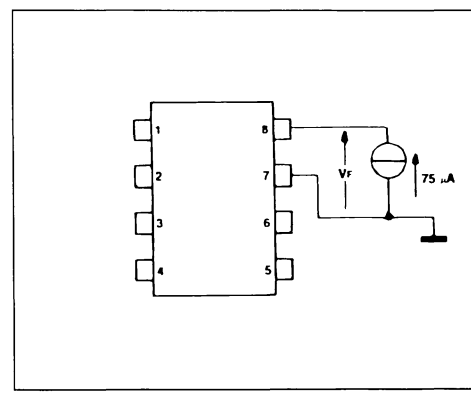


Figure 10.

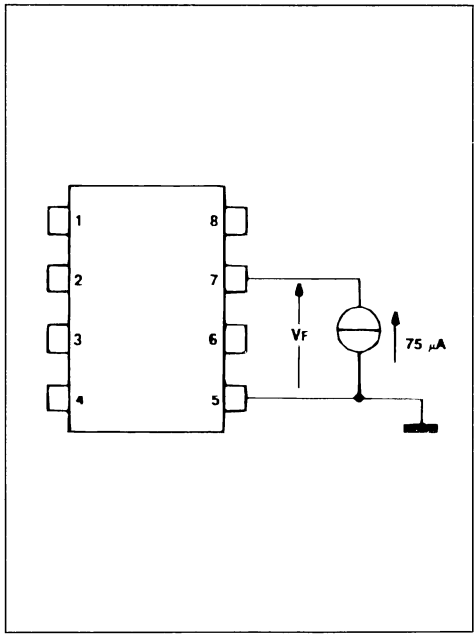


Figure 11.

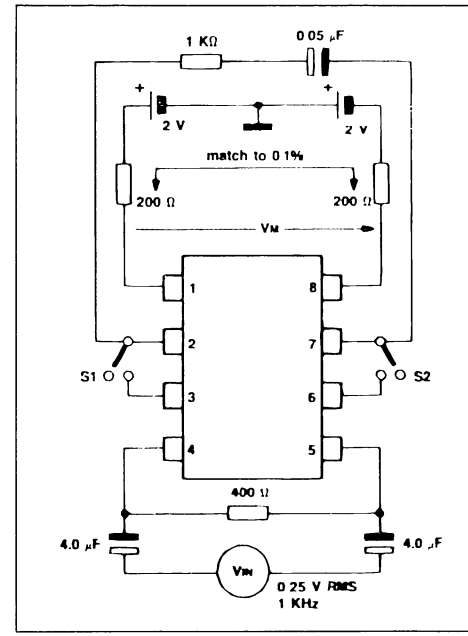


Figure 12.

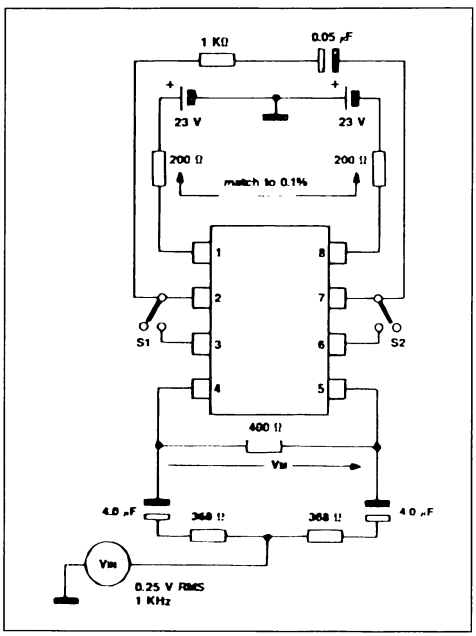


Figure 13.

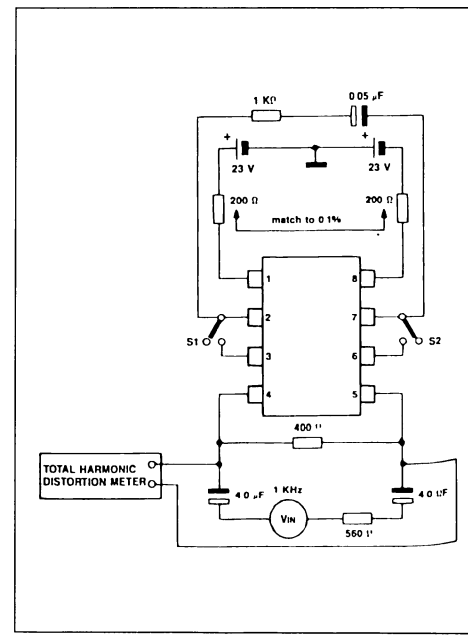
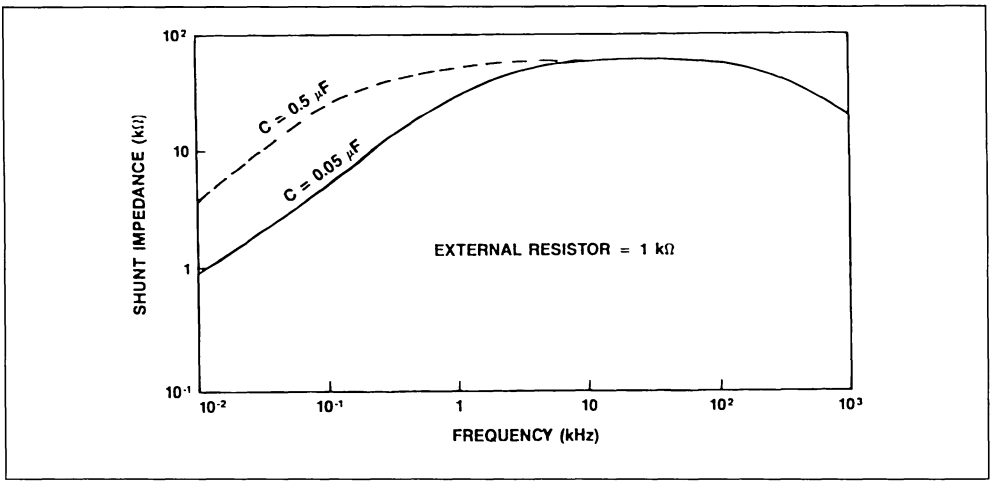


Figure 14.



SURGE PROTECTION CHARACTERISTICS

Internal surge protection circuitry (see figure 1) in conjunction with external resistors, provides protection against forward voltage surges. Reverse surges are dissipated through large internal diodes bridged across each "Line Feed" section. Forward surge protection consists of a composite PNPN device. This composite PNPN device can withstand surges as shown in figure 15. It has a breakover point (V_{BO}) of about 9 volts as shown in figure 16. After breakover, the output is clamped at less than 2 volts as long as the surge source supplies more than 150mA. When the surge source drops below 150mA, the PNPN device recovers and normal operation resumes.

Figure 15 : Maximum Applied Forward Surge Limits (PNPN Composite Device).

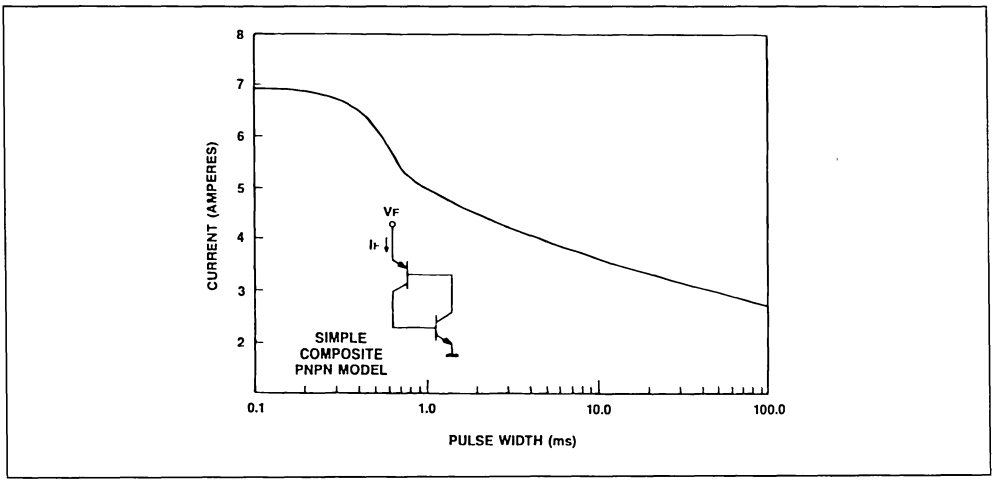
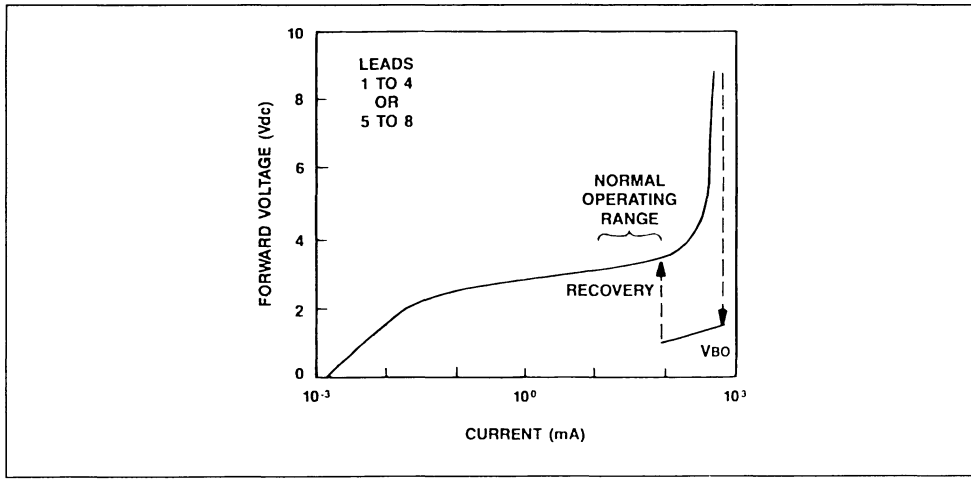


Figure 16 : Typical Voltage vs. Current (PNPN Composite).



APPLICATION

Figure 17 shows the LB1011 in a balanced line configuration. The complementary Positive and Negative Line Feeds are capacitively cross-coupled. Differential signals on the balanced line (TIP-RING) do not disturb the AC ground at the center of the cross-coupled connection. Therefore, both circuits act as constant current sources which present a high shunt impedance of approximately 50K ohms. The cross coupling does not affect feedback for either DC or common-mode signals. Therefore, for common-mode noise, the two complementary power supplies act as low impedance paths to ground through the resistors connected to V+ and V-. Common-mode rejection depends on the degree of matching between resistors RP1 and RN1. Figure 18 illustrates the LB1011 in a single-ended configuration in which it exhibits a very low DC impedance and a very high AC impedance. In some applications, where DC current needs to flow and AC Current should be blocked, this LB1011 configuration can replace an inductor. It does not, however, have the phase and amplitude vs frequency characteristics of a true inductor or RL network. The TAPP connection (pin 2) permits an external resistor (RTAP) to change the "DC Voltage Drop" (see figure 1). RTAP can be selected to raise the voltage from 3V (normal operating value) to as high as 4V. This voltage may be desirable for high operating temperature, or if the peak voltage of the AC signal exceeds 2.5V.

Since the "DC Voltage Drop" is relatively constant, the current supplied to the line is controlled by the supply voltage, the external resistor to the supply, and the resistance shunting the line. For AC signals, however, the capacitively-coupled "ground" causes the LB1011 to operate as a constant-current source with an impedance of approximately 25 Kohms.

Figure 17 : LB1011 Battery Feed Application Diagram (Balanced Configuration).

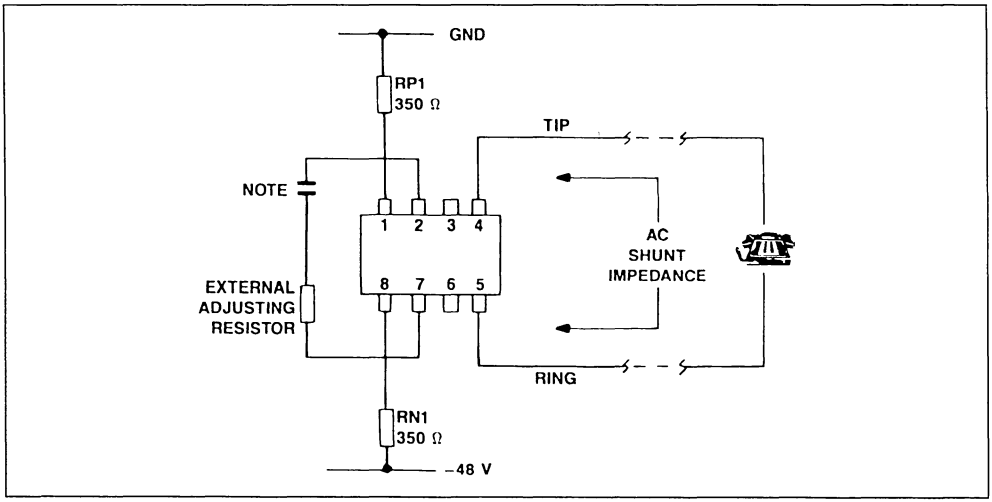
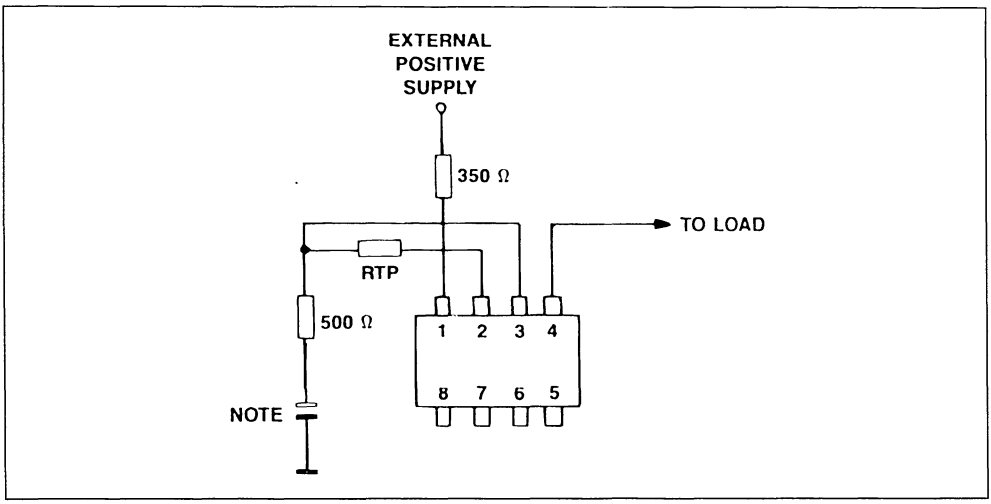


Figure 18 : LB1011 AC Blocking, DC Current Feed Application.



Note : 1. Value of capacitor selected based on frequency requirements.

85V DUAL OP-AMP

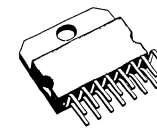
- OPERATES FROM 5 TO 85V ; DUAL OR SINGLE POWER SUPPLY OPERATION
- BIAS IS SET EXTERNALLY
- TYPICAL ft = 1MHz
- OPEN LOOP GAIN ; 50dB @ 3kHz
- PROVIDES OUTPUT CURRENTS FROM ± 40mA TO ± 80mA DEPENDING UPON -THE IBIAS VALUE
- OPERATING TEMPERATURE RANGE : FROM - 25°C TO + 100°C

APPLICATIONS

- TRANSCONDUCTANCE AMPLIFIERS FOR TELEPHONE LINE DRIVING
- VOLTAGE FOLLOWERS
- AUDIO AMPLIFIERS
- GENERAL PURPOSE CIRCUITS REQUIRING HIGH-VOLTAGE, HIGH-POWER OP-AMPS

DESCRIPTION

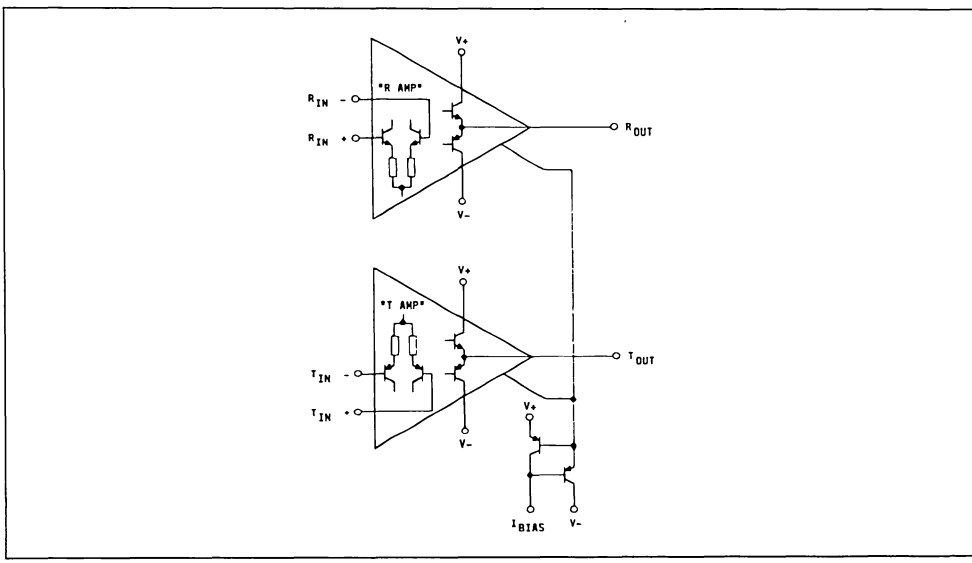
The LB1013 HIGH-VOLTAGE OP-AMP operates off of a single power supply from 5 to 85 volts. The amplifiers are internally compensated and are designed to operate in the audio band. This device is powered up with a 40µA current supplied to the IBIAS pin.
External circuitry is required to provide short-circuit protection.



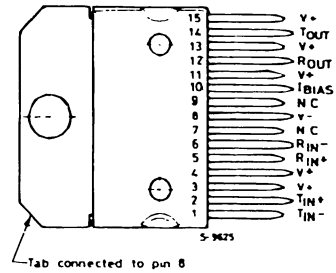
Multiwatt 15

ORDER CODE : LB1013AW

Figure 1 : High Voltage Dual Op-Amp Diagram.



PIN CONNECTION



PIN DESCRIPTION

Pin	Symbol	Function
3, 4, 11, 13, 15	V+	The more positive supply-voltage is connected to the five pins designated as V+. Either V+ or V– can be connected to ground.
14 12	T_{OUT} R_{OUT}	These pins are the Op-amp outputs for "T" and "R" amplifier respectively.
8	V–	The more negative supply-voltage is connected to the case. Either V– or V+ can be connected to ground.
1 2	T_{IN-} T_{IN+}	These pins are the non-inverting and the inverting inputs respectively for the "T" amplifier.
5 6	R_{IN+} R_{IN-}	These pins are the non-inverting and the inverting pins respectively for the "R" amplifier.
10	I_{BIAS}	A current source (or a suitable value resistor to V-) can be connected to this pin. A negative current flow must be present before the device becomes operational.
7, 9	NC	Not connected.

TYPICAL DEVICE CHARACTERISTICS (T_A = 25°C)

Parameter	I_{BIAS} = 40µA	I_{BIAS} = 80µA
Slew Rate	2V/µsec	4V/µsec
Output Current	± 40mA	± 80mA
Power Supply Rejection Ratio	45dB	45dB

ABSOLUTE MAXIMUM RATINGS (at 25°C unless otherwise specified)

Parameter	Value	Unit
Ambient Operating Temperature Range	– 25 to + 100	°C
Storage Temperature Range	– 40 to + 125	°C
Pin Temperature (Soldering Time = 15sec.)	300	°C
Power Dissipation (see note under Outline Drawing)	2	W
Voltage (V+ to V–)	85	V

Stressed in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied . Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (T_A = 25C, V+ = 25V, V– = 25V, I_{BIAS} connects through 1.25MΩ to V– unless otherwise specified)

Parameter	Test Conditions		Min.	Typ.	Max.	Unit
Open Loop Gain	f = 100Hz		75			dB
	f = 1KHz		55			dB
Input Offset Voltage					± 5.0	mV
Input Bias Current	Inverting and Non-inverting Pins				± 1.0	µA
Input Offset Current					± 1.0	µA
Common Mode Rejection Ratio	V– = – 30V, V_{CM} = ± 20V		80			dB
Output Voltage Swing ("T" Amplifier)	V+ = 38V ; V– = – 38V Non-inverting Input = GND ; R_L = 1kΩ ΔV (Inverting Input = ± 0.5V) V_{HIGH} V_{LOW}		 34.6 – 34.6			V
Output Voltage Swing ("R" Amplifier)	V+ = 38V ; V– = – 38V Non-inverting Input = GND ; R_L = 1kΩ ΔV (Inverting Input = ± 0.5V) V_{HIGH} V_{LOW}		 34.6 – 34.6			
Power Supply Currents (Amplifiers activated under no-load conditions)	Test Circuit (see figure 2) V+ = 42.5V ; V– = – 42.5V I_{V+} I_{V-}				 1.1 – 1.1	mA
Power Supply Leakage Current (Amplifier Off)	Test Circuit (see figure 2) V+ = 35V ; V– = – 35V ; IBIAS = (open) I_{V+} I_{V-}				 ± 10 ± 10	µA
Output Leakage Currents (Amplifier Off)	Test Circuit (see figure 3) V+ = 35V ; V– = – 35V IBIAS = (open) V_{LOAD} = + 30V V_{LOAD} = – 30V				 ± 10 ± 10	µA
T_{OUT} to V+ Fault Current	Test Circuit (see figure 4) V+ = 35V ; V– = – 35V ; t = 100ms	V_{LOAD} = + 35V	41		47	mA
T_{OUT} to V– Fault Current		V_{LOAD} = – 35V	– 41		– 47	
R_{OUT} to V+ Fault Current		V_{LOAD} = + 35V	41		47	
R_{OUT} to V– Fault Current		V_{LOAD} = – 35V	– 41		– 47	

Figure 2 : Power Supply Current, Test Circuit (for this test, connect both op-amps as shown above).

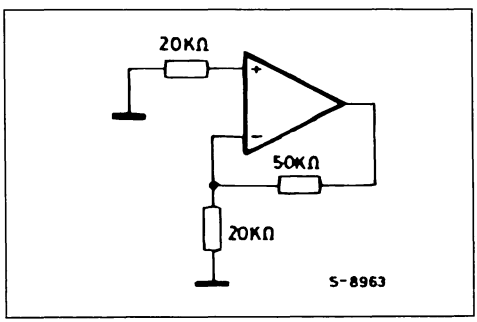


Figure 3 : Output Leakage Current, Test Circuit (the current through this 10K resistor is the "Leakage Current").

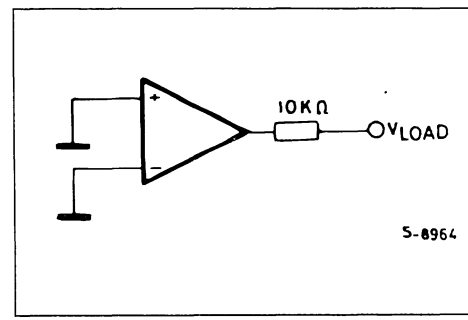


Figure 4 : Fault Current Test Circuit.

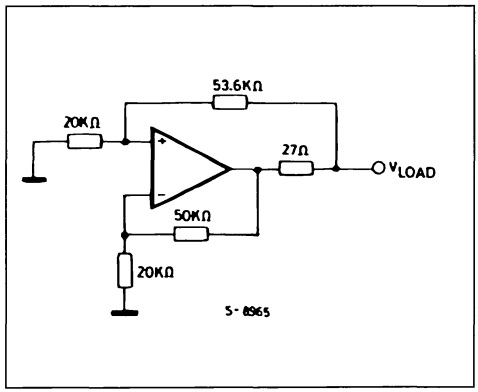
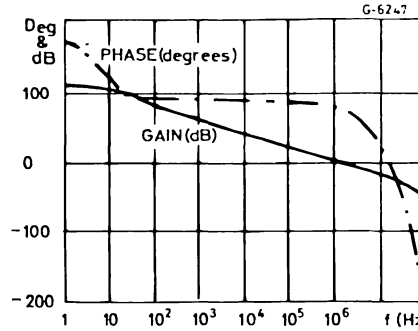
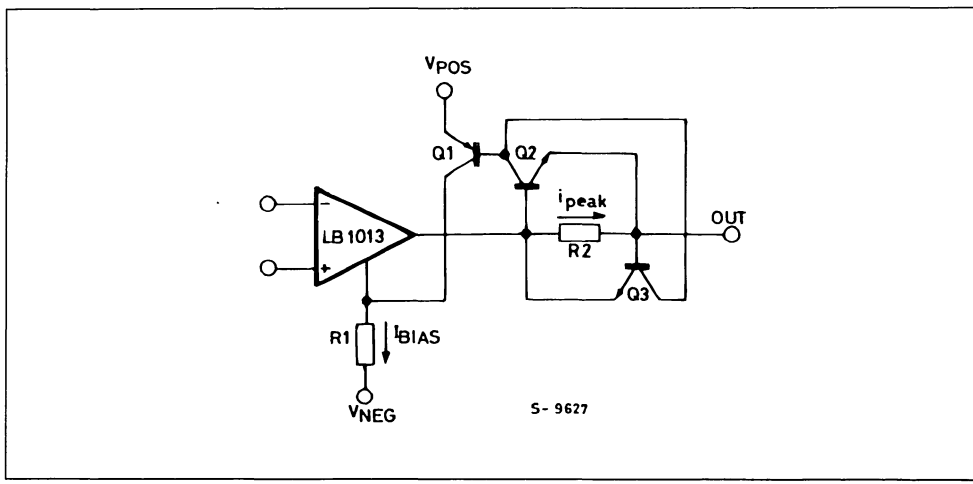


Figure 5 : Typical Characteristics : Gain/phase vs. Frequency.



SHORT-CIRCUIT PROTECTION

Figure 6 : AD External Circuitry for Short-circuit Protection.



Notes : 1. Q1, Q2, Q3 ; $BV_{CEO} > 90$ Volts

2. $R1 = \dfrac{V_{POS} - V_{NEG} - 1.2V}{I_{BIAS}}$

3. $R2 = \dfrac{0.6V}{i_{peak}}$

APPLICATION

The simplified schematic shown below illustrates an application as a transconductance amplifier for telephone line drive applications. Other applications include high voltage/power voltage followers, audio amplifiers and circuits where high-voltage, high-power op-amp capability are required.

The equations relating to the circuit shown below are as follows :

for R1 & R2 > > R3

$$I_T = \frac{V_C - V_D}{R1} \bullet \frac{R2}{R3}$$

$$I_R = \frac{V_C - V_D}{R1} \bullet \frac{R2}{R3}$$

Figure 7 : Simplified Line Feed Operation.

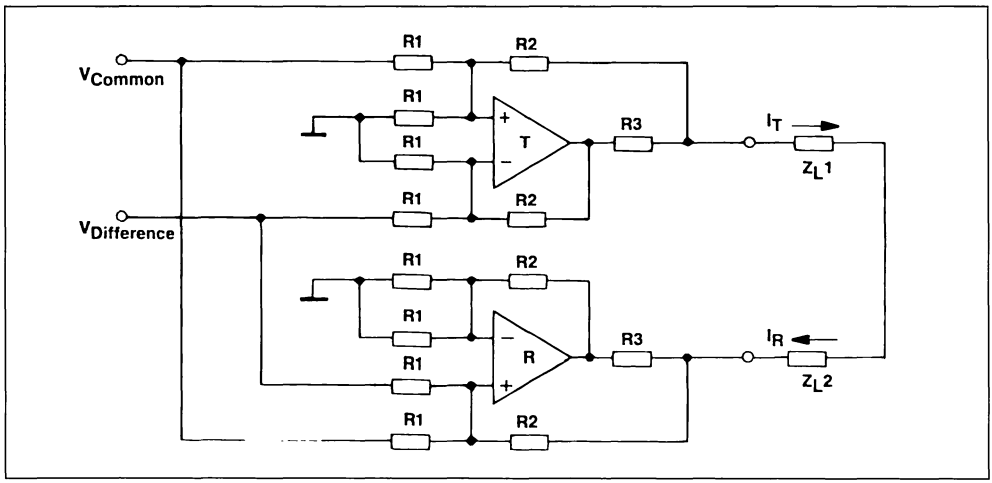
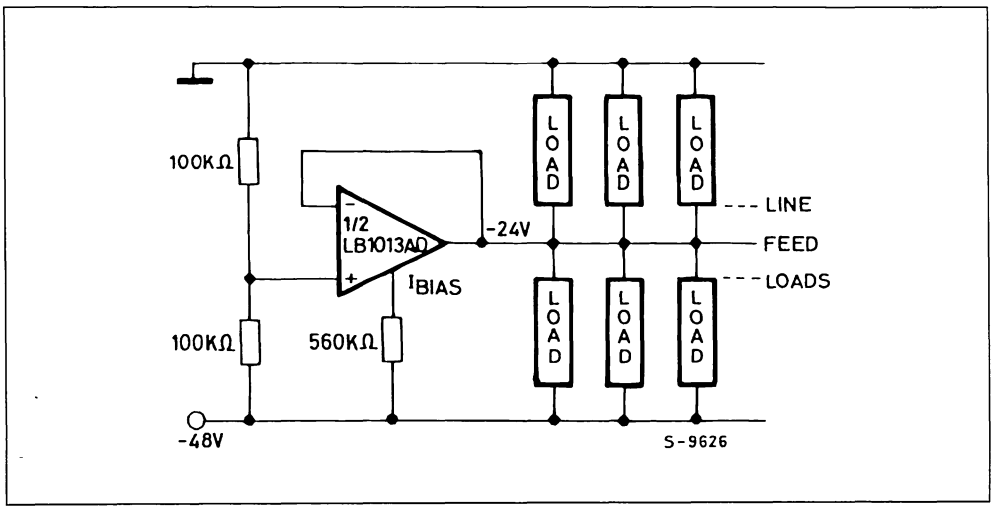


Figure 8 : Typical Voltage Follower Application.



SGS-THOMSON
MICROELECTRONICS

M079

N-CHANNEL 2 x 2 x 2 CROSSPOINT SWITCH WITH CONTROL MEMORY

- LOW ON RESISTANCE : 18Ω
- INTERNAL CONTROL LATCHES
- 5.5V_{PP} ANALOG SIGNAL CAPABILITY
- LESS THAN 1% TOTAL DISTORTION AT 0dbm
- LESS THAN – 90db CROSS-TALK AT 1.6KHz $2V_{rms}$

DIP14 (Plastic)

DIP14 (Ceramic)

ORDER CODES : M079B1
M079F1

DESCRIPTION

The M079 consists of a 2 x 2 x 2 crosspoint array and 4 memory cells. Connection between two paths is determined by the status of the corresponding memory elements. If the latch is ON the paths are connected, if OFF disconnected.

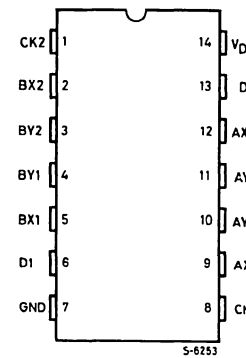
Every memory configuration can be set by writing the two D inputs using the two clocks. "1" on D determines the ON status and 0 the OFF status. The clock enters the Data input, on the high level. The correspondent switch is influenced at once. Data is then latched on falling edge of CK input. Thus storage is defined when CK goes down (see fig. 6, 7). CK and D levels are TTL compatible. The power on reset puts the memory elements into OFF status disconnecting the switches.

The M079 is available in 14 pin dual in-line plastic and ceramic packages.

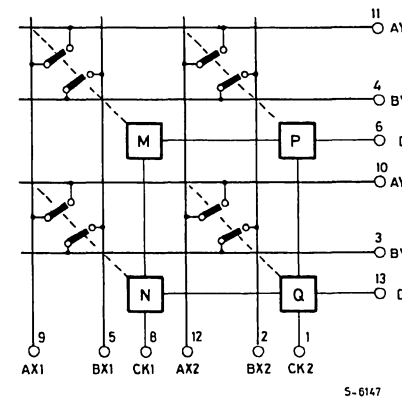
TRUTH TABLE

Logic Input D1	D2	CK1	CK2	Analog Connections Involved				Memory Status
1	X	1	0	AX1	BX1	AY1	BY1	M on
0	X	1	0	AX1	BX1	AY1	BY1	M off
X	1	1	0	AX1	BX1	AY2	BY2	N on
X	0	1	0	AX1	BX1	AY2	BY2	N off
1	X	0	1	AX2	BX2	AY1	BY1	P on
0	X	0	1	AX2	BX2	AY1	BY1	P off
X	1	0	1	AX2	BX2	AY2	BY2	Q on
X	0	0	1	AX2	BX2	AY2	BY2	Q off

PIN CONFIGURATION



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage Range	– 0.5 to 14	V
V_I	Input Voltage Range (CK1, CK2, D1, D2)	V_{DD} + 0.5	V
V_{IN}, V_{OUT}	Differential Voltage between the Two Ends of every Crosspoint in "OFF" Status	14	V
P_{tot}	Power Dissipation	600	mW
T_{op}	Operating Temperature Range	0 to 70	°C
T_{stg}	Storage Temperature Range	– 55 to 150	°C

Stresses above those listed under "Absolute Maximum Ratings" may causes permanent damage to the device This is a stress ratings only and functional operation of the the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions to extended periods may affect device reliability

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, V_{DD} at 12V ± 5%, V_{EE} = 3V)

Symbol		Parameter	Test Conditions*	Min.	Typ.	Max.	Unit
Crosspoint	αN	(cross talk) Diaphony Attenuation beetween Each Couple (fig. 2)	V_{IN} = 2V_{rms} 1.6KHz	90			dB
	αN	Longitudinal Attenuation (fig. 3)	V_{IN} = 2V_{rms} 1.6KHz			0.15	dB
	RD	Differential Impedance between AXi and BXi (on AYm an BYm)	V_{IN} = 2V_{rms} 1.6KHz	200			KΩ
	RT	Total Longitudinal Resistance* (fig. 3)				18	Ω
	CP	Attenuation in off Status	V_{IN} = 2V_{rms} 1.6KHz	100			dB
	$\Delta\frac{RT}{2}$	Resistance Difference Related to one CP				1	Ω
		Total Distortion	V_{IN} = 0dBm 1.6KHz			1	%
Control Logic	V_{INH}	Di and CKi High Level Input		2.4			V
	V_{INL}	Di and CKi Low Level Input				0.8	V
	I_{INH}	Di and CKi High Level Input	VCK = 2.7V V_D = 2.7V			1	µA
	I_{INL}	Di and CKi Low Level Input Current	VCK = 0.4V V_D = 0.4V			1	µA
	I_{DD}	Supply Current : N0 CP "ON" 1 CP "ON" 2 CP "ON"				 3 2.5 2	 mA mA mA
	I_{AL}	Analog Input Leakage (when switches off)	V_{IN} = 0 to 12V			1	µA

* This is the sum of 2-switch resistance : the single switch is tested at 9Ω and its typical value is 5Ω.

AC CHARACTERISTICS (T_{amb} = 25°C, V_{DD} = 12V)

Symbol	Parameter	Refer to Figure	Min.	Typ.	Max.	Unit
f	Clock	fig. 5			0.7	MHz
t	Turn-on	fig. 6		300	500	ns
t	Turn-off	fig. 6		330	700	ns
t_S	Setup	fig. 7	300			ns
t_H	Hold	fig. 7	300			ns
t_W	Clock Pulse Width		300			ns

Supply voltage must rise in more than 5ms.						

Figure 2 : Cross Talk Measurement.

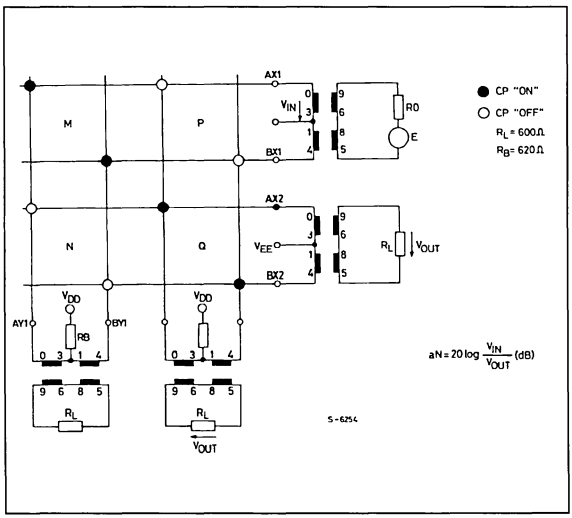


Figure 3 : Equivalent Circut of an Activated Phonic Connection.

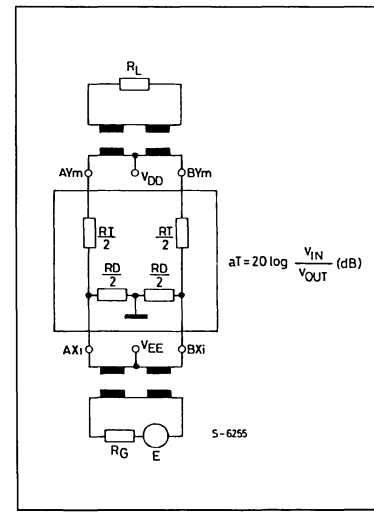


Figure 4 : Equivalent Circuit in Unactivated Phonic Connection.

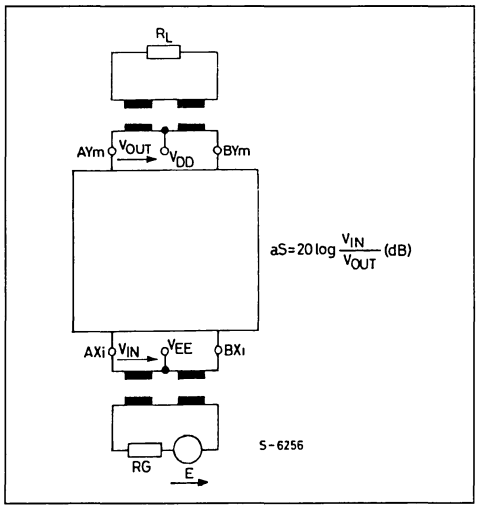


Figure 5 : Circuit for Turn-on/Turn-off Measurement.

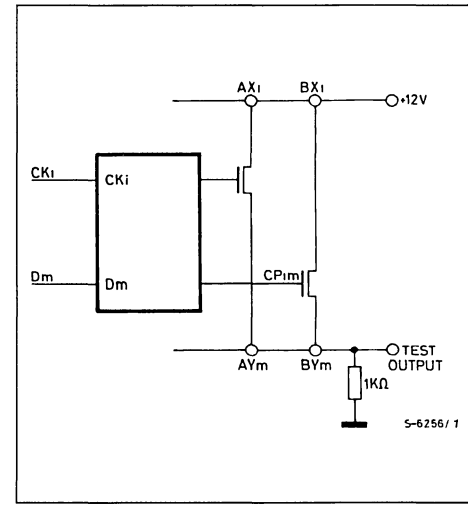


Figure 6 : Switch Turn-on/Turn-off Measurement.

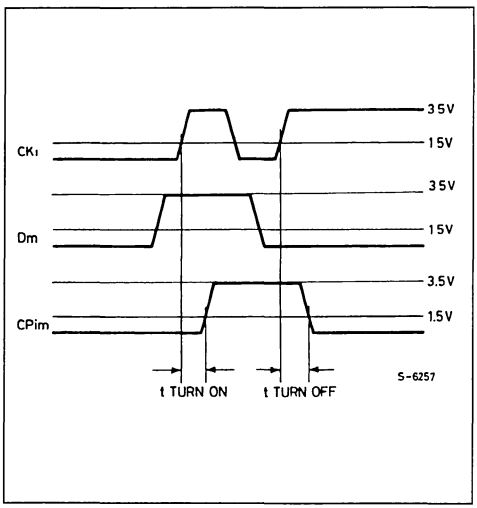
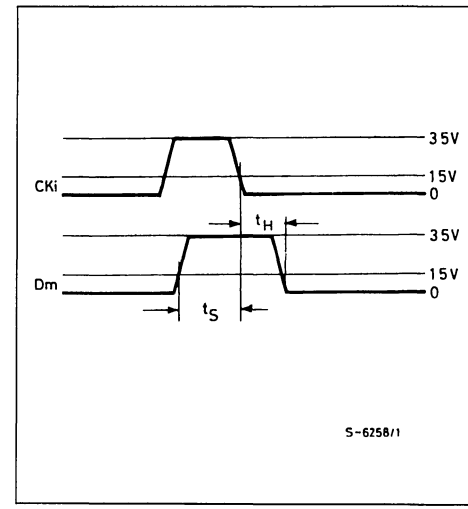
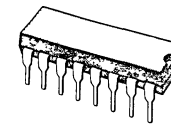


Figure 7 : $t_{set\text{-}up}/t_{Hold}$ Measurement.



2 x 8 CROSSPOINT MATRIX

- VERY LOW ON RESISTANCE
- HIGH CROSS-TALK AND OFF-STATE ISOLATION
- SERIAL SWITCH ADDRESSING, μ-PROCESSOR COMPATIBLE



(Plastic)
(Ceramic Frit-seal)
(Ceramic Metal-seal)

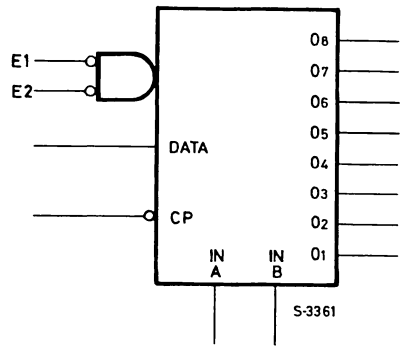
ORDER CODES : M089 B1
M089 F1
M089 D1

DESCRIPTION

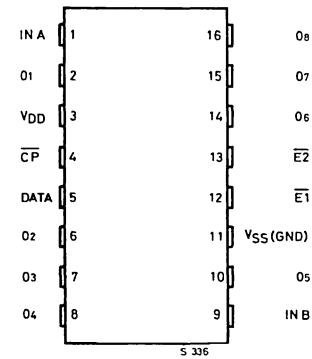
The M089 is a 2 x 8 crosspoint matrix consisting of 16 N-channel MOS transistors.

The device has been specially designed to provide switches with low cross-talk, high off-state isolation (both better than - 90dB) and low on-resistance.

LOGIC DIAGRAM



PIN CONFIGURATION

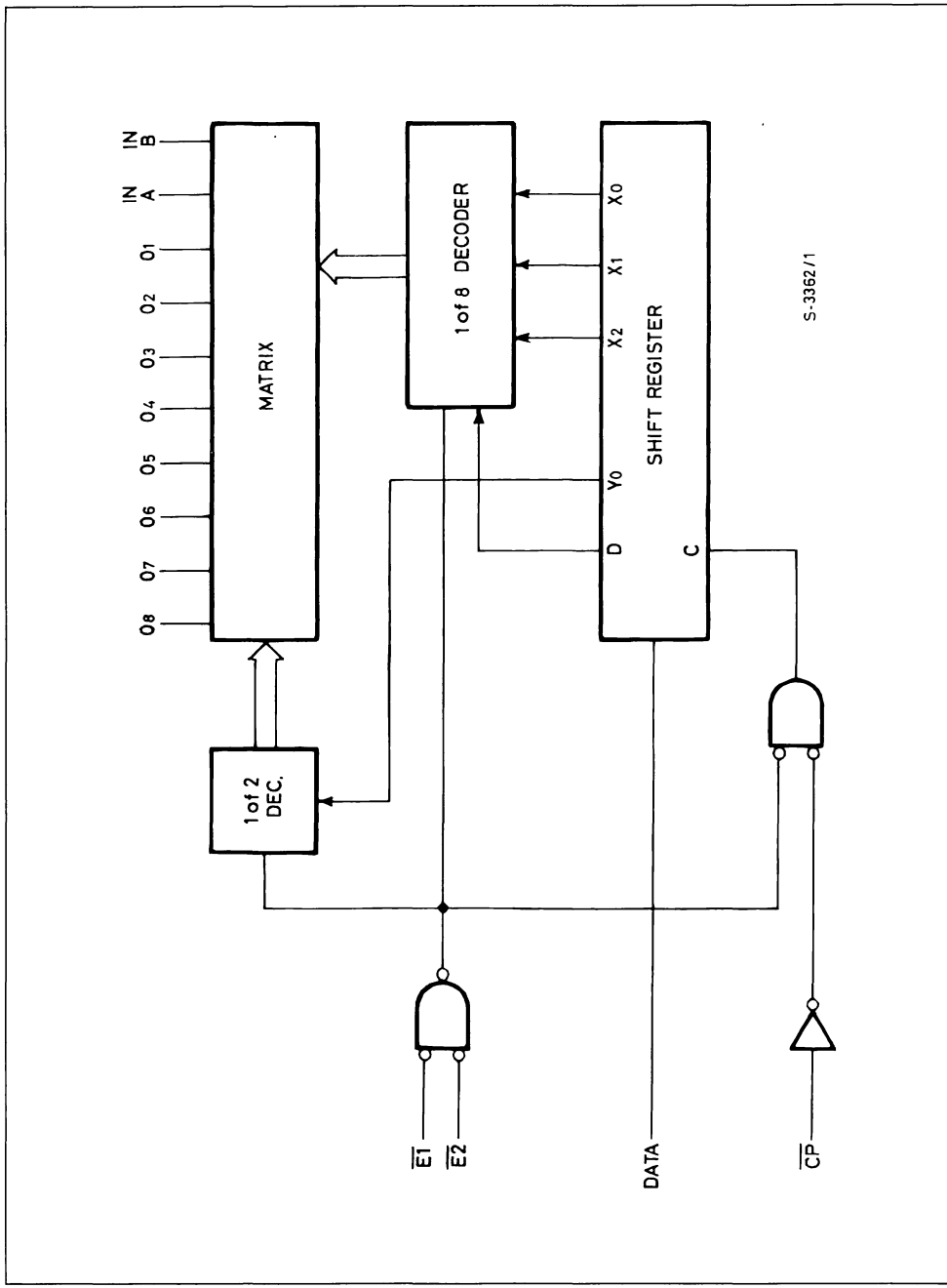


ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	– 0.5 to 17	V
V_I	Input Voltage Pins 4, 5, 12, 13	– 0.5 to 17	V
V_{IN}-V_{OUT}	Differential Voltage Across any Disconnected Switch	10	V
P_{tot}	Total Power Dissipation	640	mW
T_{op}	Operating Temperature Range : for Plastic for Ceramic	0 to 70 – 40 to 70	°C °C
T_{stg}	Storage Temperature Range	– 65 to 150	°C

Stresses above those listed under " Absolute Maximum Ratings" may cause permanent damage to the device This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the opera-tional sections of this specification is not implied Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

BLOCK DIAGRAM



CIRCUIT DESCRIPTION

The M089 is capable of forming any combination of switch conditions in an 8 x 2 matrix. Each switch is individually set and a latch maintains it in its set condition.

The switch address and control bits are loaded serially into an internal shift register (5 bits), when inputs E_1, and E_2 are low. The address bits consist of : 3 input selection bits (X_0-X_2) and a single output selection bit (Y_0). A fifth (control) bit (D) defines whether the chosen switch is to be opened or closed.

D	Y_0	X_2	X_1	X_0

M089 Shift Register Bit Allocation

Data bits are clocked into the shift register on the high to low transition of the clock input (CP). If more than 5 clock transmission are applied during loading of the shift register the last 5 data bits are loaded into it. The status of the switch addressed changes on the low to high transition of one or both enable inputs.

ENABLE INPUTS TRUTH TABLE

$\overline{E}_1$	$\overline{E}_2$	Function Data Load
L	L	Addressed Switch Changed
⌐	L	
L	⌐	
⌐	⌐	

DATA BIT TRUTH TABLE

Data	Switch Status after Enable Transition
L	Disconnect
H	Connect

DATA BITS TRUTH TABLE FOR SWITCH SELECTION

	O_1 Y_0 X_2 X_1 X_0	O_2	O_3	O_4	O_5	O_6	O_7	O_8
IN A	1111	1011	1101	1001	1110	1010	1100	1000
IN B	0111	0011	0101	0001	0110	0010	0100	0000

For example to address the switch connecting IN A to O_5 the shift register must be loaded with the code :

	D Y_0 X_2 X_1 X_0
to Connect	11110
to Disconnect	01110

ELECTRICAL CHARACTERISTICS (T_{amb} = 0 to 70°C for M089 B1 ; – 40 to 70°C for M089 F1, D1 ; V_{DD} = 14V to 16V unless otherwise specified)

Symbol	Parameter		Test Conditions	Min.	Typ.	Max.	Unit
R_{ON}*	ON-resistance		T_{amb} = 25°C $V_{I(A, B)}$ = 3.5V V_{DD} = 14V $I_{D(min)}$ = 10mA		10	15	Ω
ΔR_{ON}	ON-resistance Variation in any Package		T_{amb} = 25°C V_I = 3.5V V_{DD} = 14V I_D = 10mA			± 2	%
I_{DD}	Supply Current					7	mA
I_{LI}	Input Leakage	Pins 4, 5, 12, 13	V_I = 5V			1	µA
		Pins 1, 9	V_{IA}, V_{IB} = 4.5V V_{O1}, V_{O8} = 1.5V			0.2	µA
			V_{IA}, V_{IB} = 6V V_{O1}, V_{O8} = 1.5V			1	µA
I_{LO}	Output Leakage	Pins 2, 6, 7, 8, 10, 14, 15, 16	V_{O1}, V_{O8} = 4.5V V_{IA}, V_{IB} = 1.5V			0.2	µA
			V_{O1}, V_{O8} = 6V V_{IA}, V_{IB} = 1.5V			1	µA
V_{low}	Logic 0 Input Level		All Inputs	– 0.3		0.8	V
V_{high}	Logic 1 Input Level		All Inputs	4.5		V_{DD}	V
CT	Cross-talk Attenuation		See fig. 4	90	95		dB
I_O	Off Isolation		See fig. 5	90	95		dB
f_{CL}	Maximum Clock Input Frequency		See fig. 6			1	MHz
T_{LG}	Lag Time			100			ns
T_{LD1}	Lead Time			400			ns
T_{LD2}				150			
T_{WR}	Write Time					3	µs
t_W	Clock Pulse Width			0.4		100	µs

* See figure 1 and 2 for R_{ON} variation with temperature and V_{BIAS}.

Figure 1 : R_{ON} derating vs. temperature typ.

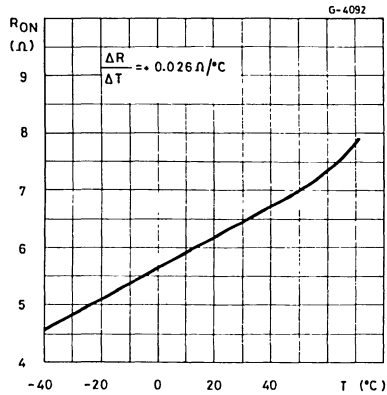
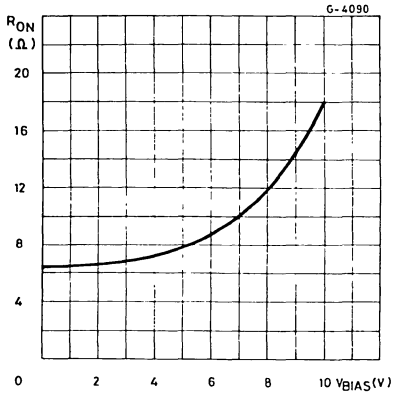


Figure 2 : R_{ON} derating vs. V_{BIAS}.



TEST CIRCUITS

Figure 3 : R_{ON} measurement.

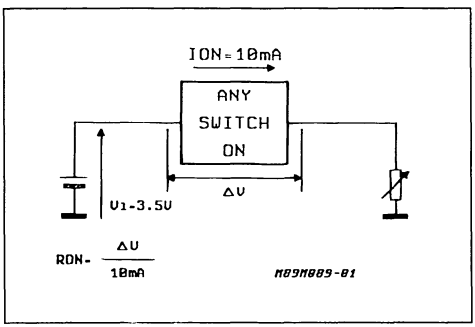


Figure 4 : Crosstalk Measurements.

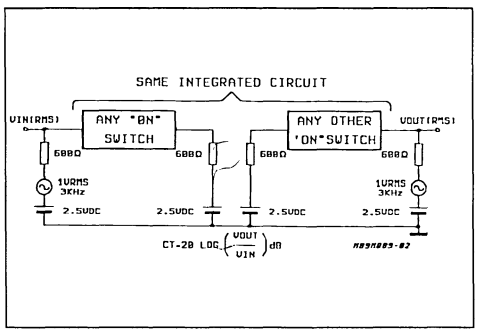
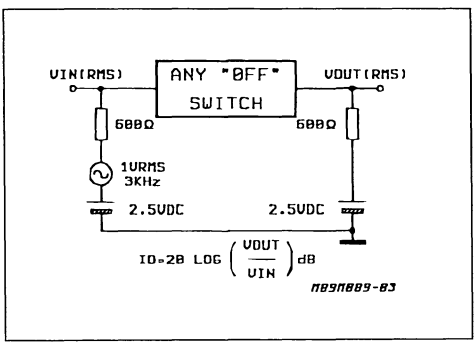
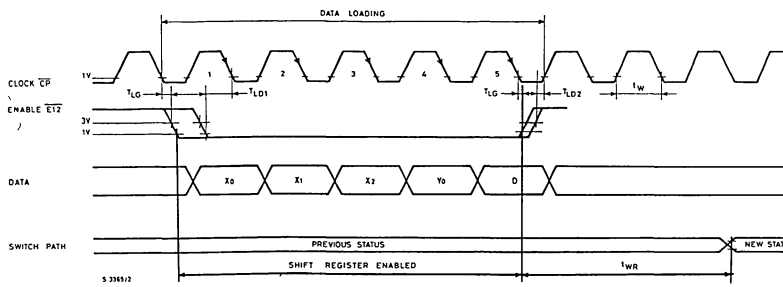


Figure 5 : Off Isolation Measurement.



TIMING DIAGRAM

Figure 6.

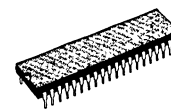


SGS-THOMSON
MICROELECTRONICS

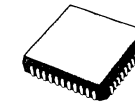
M093

N-CHANNEL 12 x 8 CROSSPOINT SWITCH WITH CONTROL MEMORY

- LOW ON RESISTANCE (typ. 35Ω at V_{DD} = 14V)
- INTERNAL CONTROL LATCHES
- 2 V_{PP} ANALOG SIGNAL CAPABILITY
- LESS THAN 1% TOTAL DISTORTION AT 0dBm
- LESS THAN – 95dB CROSS-TALK AT 1KHZ 1 V_{PP}



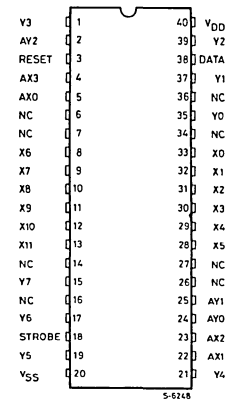
DIP40
(Plastic)



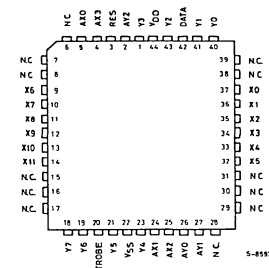
Plastic Chip Carrier

ORDER CODES : M093B
M093C

PIN CONNECTIONS



CHIP CARRIER

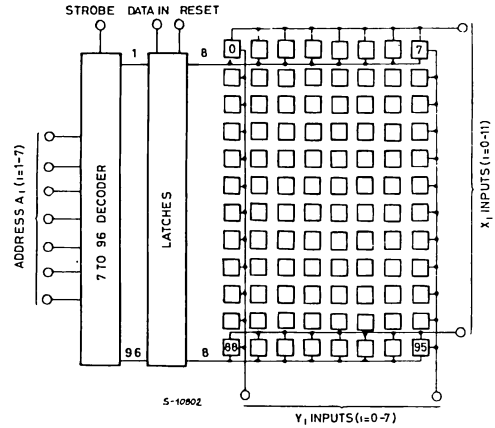


DESCRIPTION

The M093 contains a 12 x 8 array of cross-point together with a 7 to 96 line decoder and latch circuits. Anyone of the 96 switches can be addressed by selecting the appropriate 7 input bits. The selected switch can be turned on or off by applying a logical one or zero to the data in and the strobe input at logical one. A reset signal can be used to turn off all the switches together when is switched at logical one.

The M093 is available in a 40 lead dual in-line plastic or 44 lead plastic chip carrier packages. Logic inputs are TTL compatible.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	– 0.5 to 18	V
V_{IN}	Input Voltage Range	– 0.5 to V_{DD} + 0.5	V
I_{IN}	DC Input Current (analog input)	± 10	mA
P_{tot}	Power Dissipation	1	W
T_{op}	Operating Temperature Range	0 to 70	°C
T_{stg}	Storage Temperature Range	– 50 to 125	°C

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THRUTH TABLE

Address							Connections
AX0	AX1	AX2	AX3	AY0	AY1	AY2	
0	0	0	0	0	0	0	X0 - Y0
1	0	0	0	0	0	0	X1 - Y0
0	1	0	0	0	0	0	X2 - Y0
1	1	0	0	0	0	0	X3 - Y0
0	0	1	0	0	0	0	X4 - Y0
1	0	1	0	0	0	0	X5 - Y0
0	1	1	0	0	0	0	No Connection
1	1	1	0	0	0	0	No Connection
0	0	0	1	0	0	0	X6 - Y0
1	0	0	1	0	0	0	X7 - Y0
0	1	0	1	0	0	0	X8 - Y0
1	1	0	1	0	0	0	X9 - Y0
0	0	1	1	0	0	0	X10 - Y0
1	0	1	1	0	0	0	X11 - Y0
0	1	1	1	0	0	0	No Connection
1	1	1	1	0	0	0	No Connection
0	0	0	0	1	0	0	X0 - Y1
↓	↓	↓	↓	↓	↓	↓	↓ ↓
1	0	1	1	1	0	0	X11 - Y1
0	0	0	0	0	1	0	X0 - Y2
↓	↓	↓	↓	↓	↓	↓	↓ ↓
1	0	1	1	0	1	0	X11 - Y2
0	0	0	0	1	1	0	X0 - Y3
↓	↓	↓	↓	↓	↓	↓	↓ ↓
1	0	1	1	1	1	0	X11 - Y3
0	0	0	0	0	0	1	X0 - Y4
↓	↓	↓	↓	↓	↓	↓	↓ ↓
1	0	1	1	0	0	1	X11 - Y4
0	0	0	0	1	0	1	X0 - Y5
↓	↓	↓	↓	↓	↓	↓	↓ ↓
1	0	1	1	1	0	1	X11 - Y5
0	0	0	0	0	1	1	X0 - Y6
↓	↓	↓	↓	↓	↓	↓	↓ ↓
1	0	1	1	0	1	1	X11 - Y6
0	0	0	0	1	1	1	X0 - Y7
↓	↓	↓	↓	↓	↓	↓	↓ ↓
1	0	1	1	1	1	1	X11 - Y7

RECOMMENDED OPERATING CONDITION

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	10 to 16	V
T_{op}	Operating Temperature	0 to 70	°C
V_{IN}	(logic signal)	0 to V_{DD}	

STATIC ELECTRICAL CHARACTERISTICS (T_{amb} = 0 to 70°C, V_{DD} = 14V)

CROSSPOINT

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
	Operating Current	f_o = 100KHz			35	mA
	On Resistance	V_{IDC} = 6.75V V_{ODC} = 6.5V (see fig. 1)		35	60	Ω
	ΔR on between any 2 Switch			6	10	Ω
	Off Leakage*	All Switches off $V_{OS} = V_{IS}$ = 0 to V_{DD}			± 3	μA

CONTROLS

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{IL}					0.8	V
V_{IN}			2.4			V
	Input Leakage*	V_{IN} = 0 to V_{DD}			± 3	μA

* There limits are valid on the total temperature range · 0–70 °C at 25 °C these limits become ± 100nA.

DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, C_L = 50pF all input square wave rise and fall times = 20ns, V_{DD} = 14V)

CROSSPOINTS

Symbol	Parameter	Test Conditions					Value			Unit
		Note	f_I (KHz)	R_L (KΩ)	V_{is} (V_{PP})	V_{DC} (V)	Min.	Typ.	Max.	
t_{PHL}, t_{PLH}	Propagation Delay Time (switch ON) Signal Input to Output	Fig. 2		1	2	5		30	100	ns
	Frequency Response (any switch ON) (20 log (V_{OS}/V_{IS}) = – 3dB	C_L = 3pF		0.091	2	5		50		MHz
	Sine Wave Distortion		1000	0.091	2	5			1	%
	Feedthrough (all switches OFF)	Fig. 3	10	1	2	5	– 90			dB
	Frequency for Signal Crosstalk Attenuation of 40dB Attenuation of 110dB	Fig. 4		 1	 2	 5	1 5			MHz KHz
C	Capacitance Xn to Ground							15		pF
	Yn to Ground		1000		0.1	5		15		
	Feedthrough							0.4		
C	Capacitance Logic Input to Ground		1000		0.1	5		5		pF

DYNAMIC ELECTRICAL CHARACTERISTICS (continued)

CONTROLS

Symbol	Parameter	Test Conditions	See Fig.	V_{DD} (V)	Value Min.	Value Typ.	Value Max.	Unit
t_{PSN}	Propagation Delay Time Strobe to Output (switch turn-ON)	R_L = 1KΩ C_L = 50pF t_r, t_f = 20ns	5	14V			400	ns
t_{PZH}	Data-in to Output (turn-ON to high level)		6	14V			500	ns
t_{PAN}	Address to Output (turn-ON to high level)		7	14V			400	ns
t_{PSF}	Propagation Delay Time Strobe to Output (switch turn-OFF)		5	14V			300	ns
t_{PZL}	Data-in to Output (turn-ON to low level)		6	14V			500	ns
t_{PAF}	Address to Output (turn-OFF)		7	14V			300	ns
t_{SS}	Set-up Time Data-in to Strobe		5	14V	120			ns
t_{SH}	Hold Time Data-in to Strobe		5	14V	200			ns
t_{AS}	Set-up Time Data-in to Address		7	14V	160			ns
t_{AH}	Hold Time Data-in to Address		7	14V	100			ns
$f_{Ø}$	Switching Frequency			14V		1		MHz
t_W	Strobe Pulse Width			14V	100			ns
	Control Crosstalk Data-in, Address, or Strobe to Output	Square Wave Input V_{IN} = 3V t_r, t_f = 20ns R_L = 10KΩ	8	14V		75		mV
t_W	Reset Pulse Width	R_L = 1KΩ C_L = 50pF t_r, t_f = 20ns	9	14V	100			ns
t_{PHZ}	Reset Turn-OFF Delay		9	14V			260	ns

TEST CIRCUITS

Figure 1 : R_{ON} Measurement.

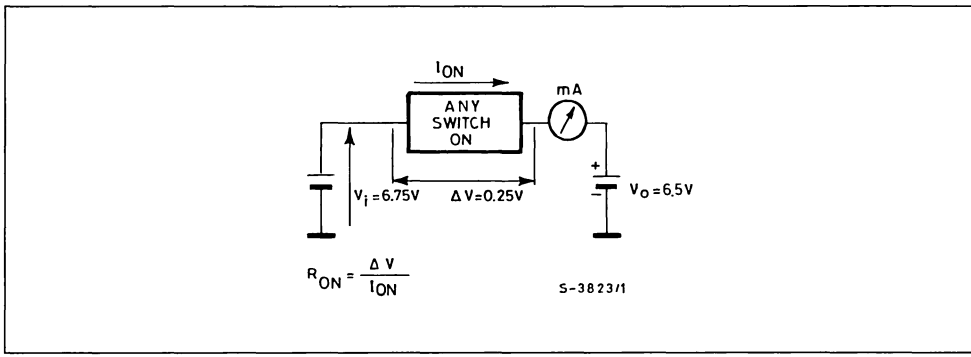


Figure 2 : Propagation Delay Time and Waveforms (signal input to signal output, switch ON).

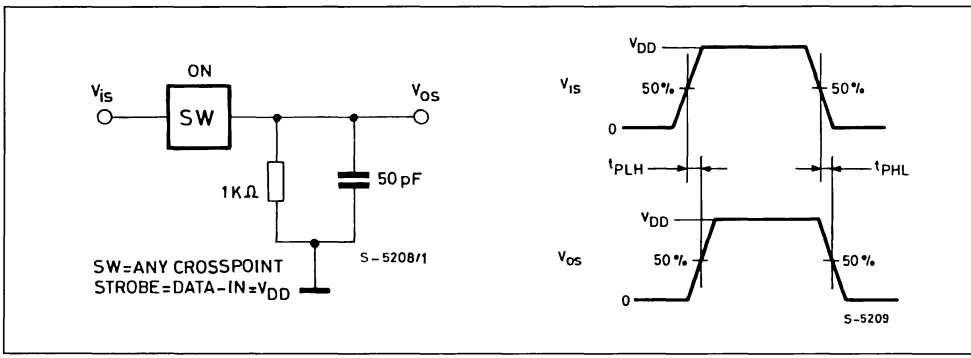
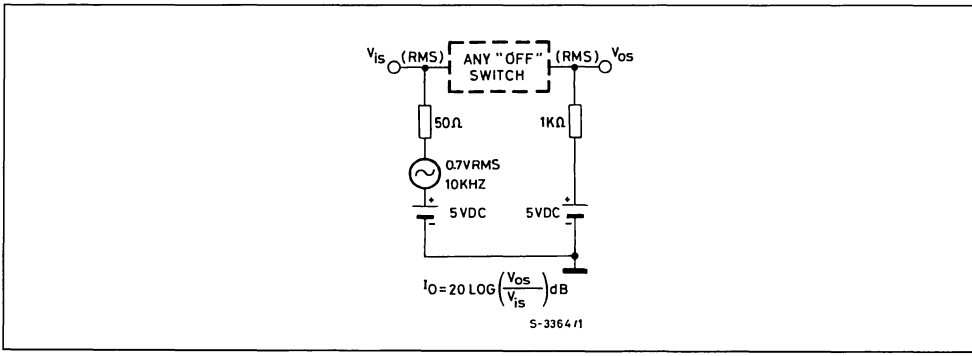


Figure 3 : Off Isolation Measurement (Feed through).



TEST CIRCUITS (continued)

Figure 4 : Crosstalk Measurements.

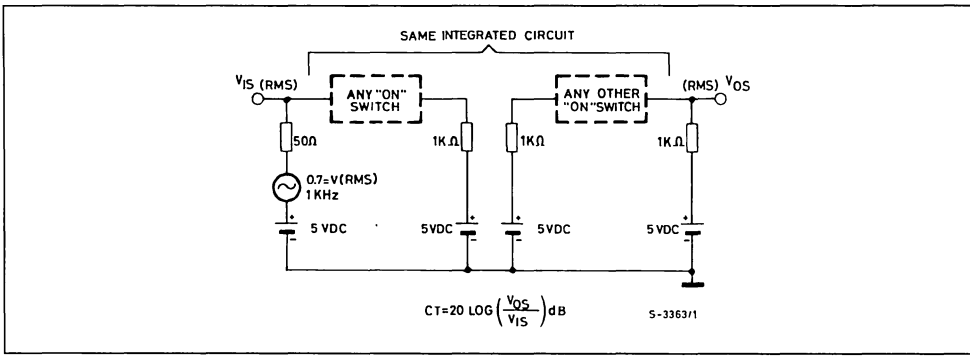


Figure 5 : Propagation Delay Time and Waveforms (strobe to signal output, switch Turn-ON or Turn-OFF).

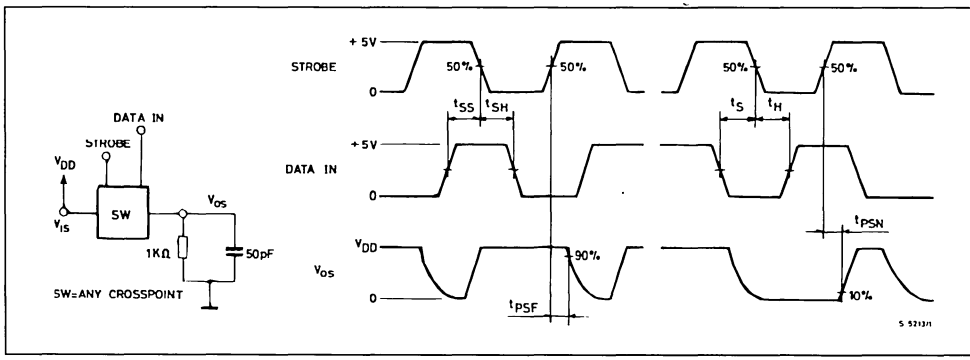
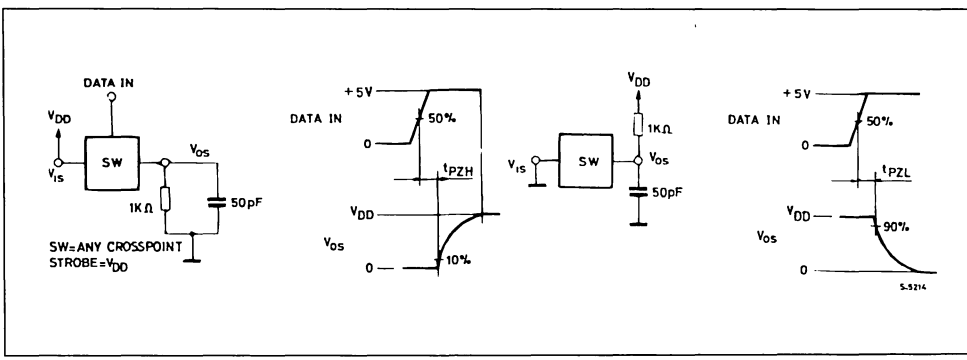


Figure 6 : Propagation Delay Time and Waveforms (data-in signal output, switch Turn-ON to high or low level).



TEST CIRCUITS (continued)

Figure 7 : Propagation Delay Time and Waveforms (address to signal output, switch Turn-ON or Turn-OFF).

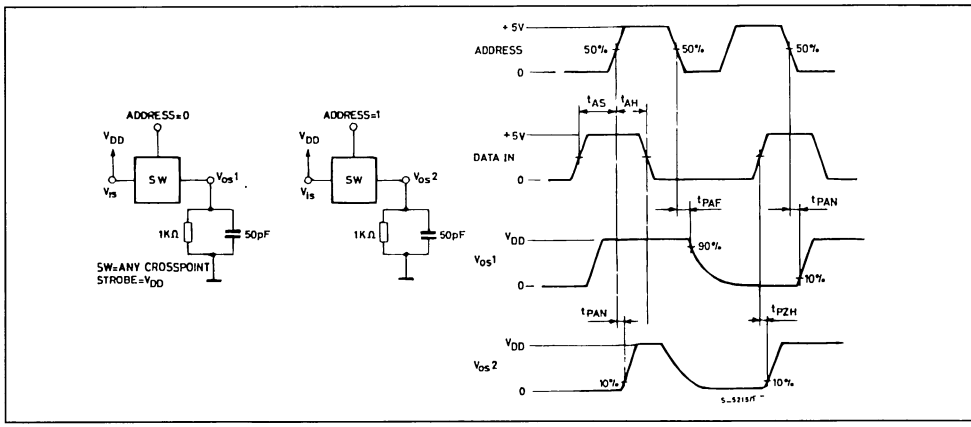


Figure 8 : Waveforms for Crosstalk (control input to signal output).

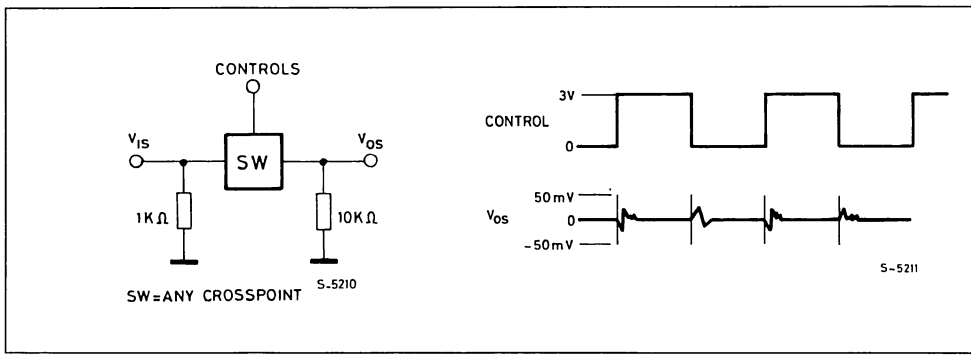
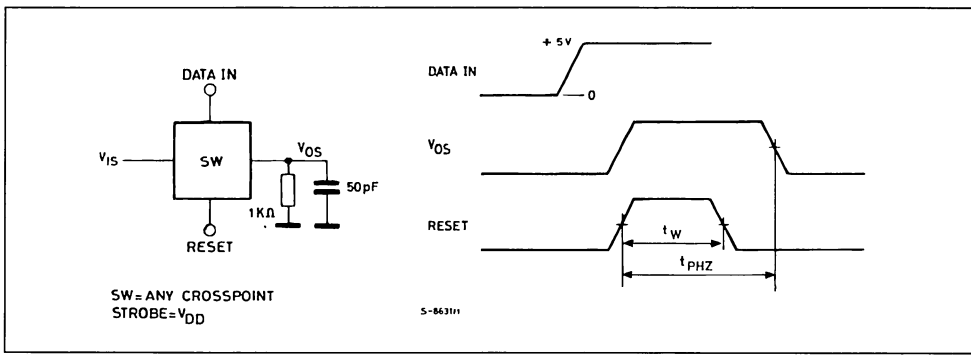
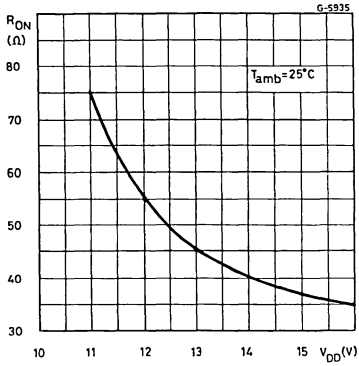


Figure 9 : Propagation Delay Time and Waveforms (reset to output delay).

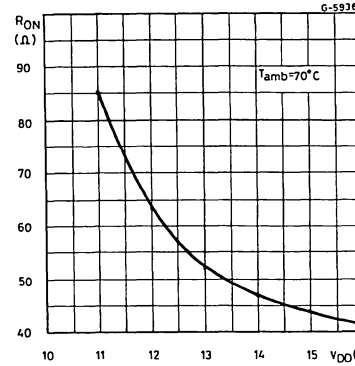


Note : Data latch can be performed either by the strobe falling edge a by the address change (with strobe at high level). Advised operation is to move data/address with strobe input at 0, then latching with a strobe pulse.

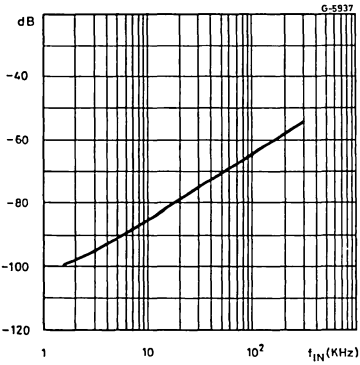
Typical ON Resistance vs. V_{DD}.



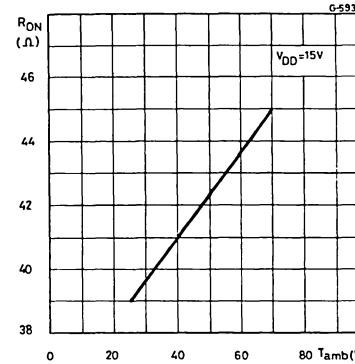
Typical ON Resistance vs. V_{DD}.



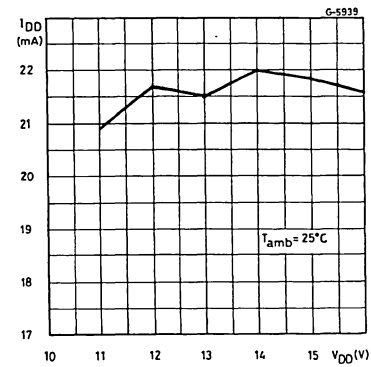
Typical Crosstalk between two CROSS-POINT vs. Input Frequency.



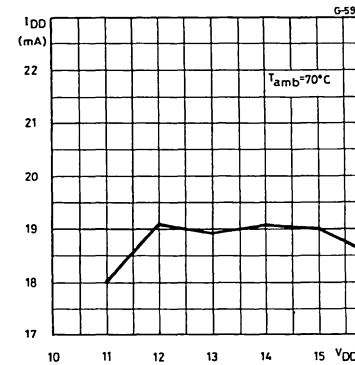
Typical ON Resistance vs. Temperature.



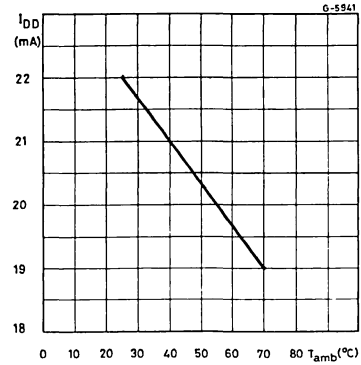
Typical Maximum I_{DD} vs. V_{DD}.



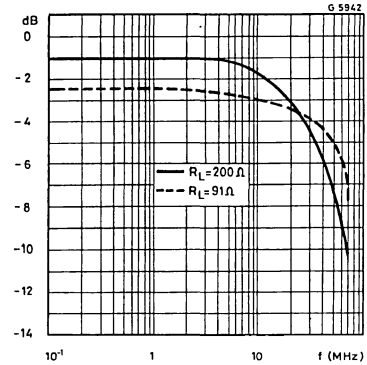
Typical Maximum I_{DD} vs. V_{DD}.



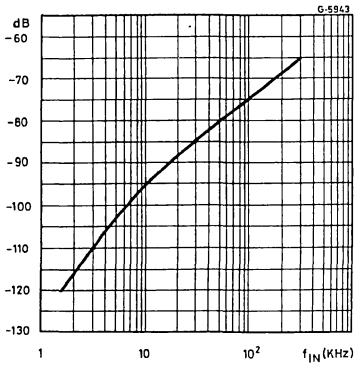
Typical Maximum I_{DD} vs. Temperature.



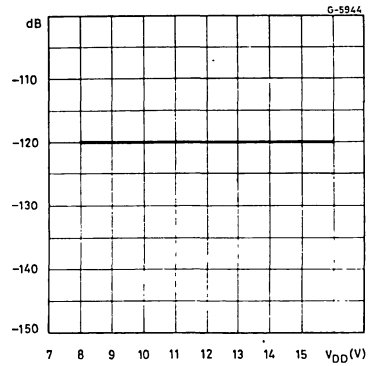
Bandwidth Insertion Loss vs. Frequency.



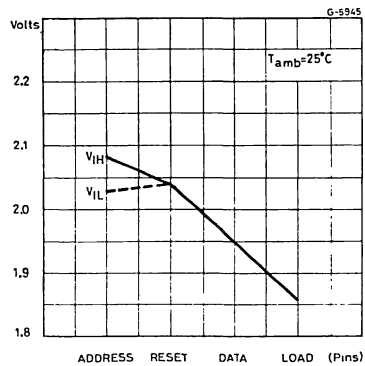
Typical Crosstalk Switches vs. Signal Frequency.



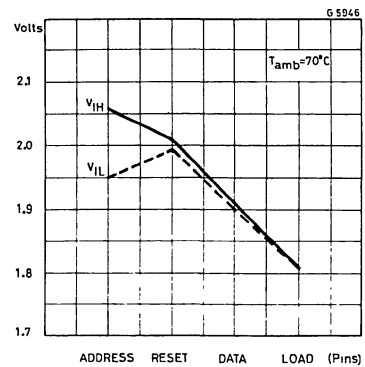
Crosstalk vs. Power Supply at Every Switch.



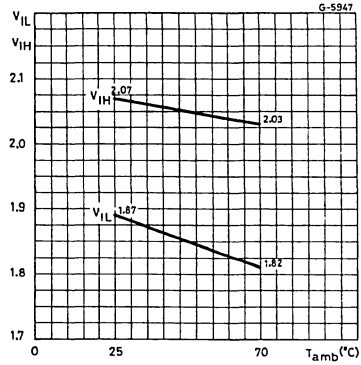
Pin Dependance V_{IH} and V_{IL}.



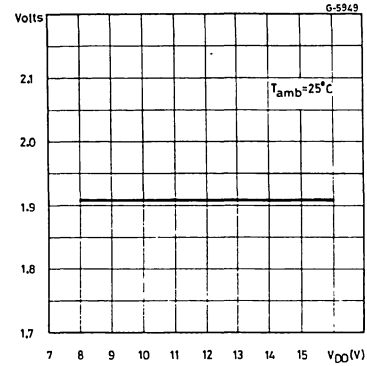
Pin Dependance V_{IH} and V_{IL}.



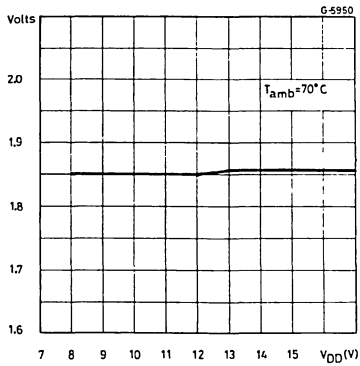
Typical V_{IL} and V_{IH} vs. Temperature.



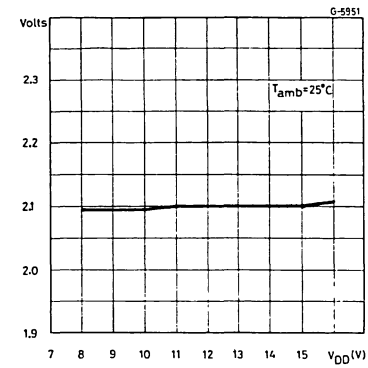
Typical V_{IL} vs. V_{DD}.



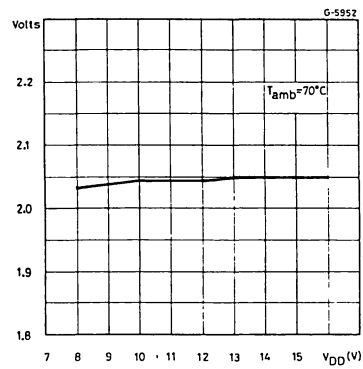
Typical V_{IL} vs. V_{DD}.



Typical V_{IH} vs. V_{DD}.

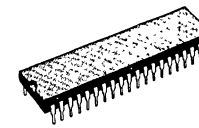


Typical V_{IH} vs. V_{DD}.

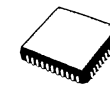


CMOS 12 X 8 CROSSPOINT WITH CONTROL MEMORY

- LOW ON RESISTANCE (typ. 40 Ω at V_{DD} = 10 V)
- INTERNAL CONTROL LATCHES
- ANALOG SIGNAL SWING CAPABILITY EQUAL TO POWER SUPPLY VOLTAGE APPLIED
- LESS THAN 1 % TOTAL DISTORT. AT 0 dBm
- LESS THAN – 95 dB CROSS-TALK AT 1 KHz 1 V_{PP}
- VERY LOW POWER CONSUMPTION
- PIN-TO-PIN COMPATIBLE WITH M093



DIP40
(Plastic)



PLCC44

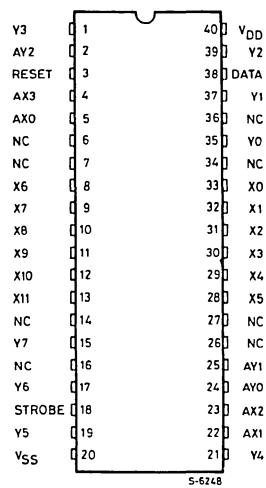
ORDER CODES : M3493B1 (DIP40)
M3493C1 (PLCC44)

DESCRIPTION

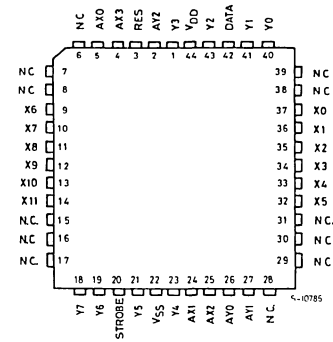
The M3493 contains a 12 x 8 array of crosspoint together with a 7 to 96 line decoder and latch circuits. Anyone of the 96 switches can be addressed by selecting the appropriate 7 input bits. The selected switch can be turned on or off by applying a logical one or zero to the data in and the strobe input at logical one. A reset signal can be used to turn off all the switches together when is switched at logical one.

M3493 is available in 40 lead dual in-line plastic, or 44 lead plastic chip carrier packages.

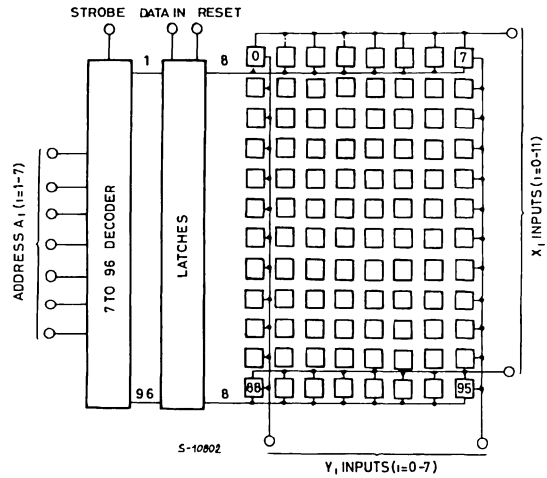
PIN CONNECTIONS (top view)



CHIP CARRIER



BLOCK DIAGRAM



INPUT/OUTPUT DESCRIPTION

POWER

I/O	Symbol	Pin	Description
I	V_{DD}	40	Positive Power Supply
I	V_{SS}	20	Negative Power Supply

ADDRESS

I/O	Symbol	Pin	Description
I	AX0-AX3	4, 5, 22, 23	X Address Lines. These 4 pins are used to select one of the 16 rows of switches. Refer to the truth table for legal address.
I	AY0-AY2	2, 24, 25	Y Address Lines. These 3 pins are used to select one of the 8 columns of switches. Refer to the truth table for legal address.

CONTROL

I/O	Symbol	Pin	Description
I	DATA	38	This input determines if the selected switch will be turned on (closed) or off (opened). If the pin is held high, the selected switch will be closed. If the pin is held low, the switch will be opened.
I	STROBE	18	This pin enables whatever action is selected by the ADDRESS and DATA pins. When the STROBE pin is held low, no switch openings or closings take place. When the STROBE pin is held high, the switch addressed by the select lines will be opened or closed (depending upon the state of the DATA pin)
I	RESET	3	Master Reset. This pin turns off (opens) all 128 switches. The states of the above control lines are irrelevant. This pin is active high.

DATA

I/O	Symbol	Pin	Description
I/O	X0-X11	8-13, 28-33	Analog Input/Outputs. These pins are connected to the Y0-Y7 pins in according to the truth table.
I/O	Y0-Y7	1,15,17,19,21 35,37,39	Analog Input/Outputs. These pins are connected to the X0-X15 pins in according to the truth table.

TRUTH TABLE

Address							Connections
AX0	AX1	AX2	AX3	AY0	AY1	AY2	
0	0	0	0	0	0	0	X0 - Y0
1	0	0	0	0	0	0	X1 - Y0
0	1	0	0	0	0	0	X2 - Y0
1	1	0	0	0	0	0	X3 - Y0
0	0	1	0	0	0	0	X4 - Y0
1	0	1	0	0	0	0	X5 - Y0
0	1	1	0	0	0	0	No connection
1	1	1	0	0	0	0	No connection
0	0	0	1	0	0	0	X6 - Y0
1	0	0	1	0	0	0	X7 - Y0
0	1	0	1	0	0	0	X8 - Y0
1	1	0	1	0	0	0	X9 - Y0
0	0	1	1	0	0	0	X10 - Y0
1	0	1	1	0	0	0	X11 - Y0
0	1	1	1	0	0	0	No connection
1	1	1	1	0	0	0	No connection
0	0	0	0	1	0	0	X0 - Y1
↓	↓	↓	↓	↓	↓	↓	↓ ↓
1	0	1	1	1	0	0	X11 - Y1
0	0	0	0	0	1	0	X0 - Y2
↓	↓	↓	↓	↓	↓	↓	↓ ↓
1	0	1	1	0	1	0	X11 - Y2
0	0	0	0	1	1	0	X0 - Y3
↓	↓	↓	↓	↓	↓	↓	↓ ↓
1	0	1	1	1	1	0	X11 - Y3
0	0	0	0	0	0	1	X0 - Y4
↓	↓	↓	↓	↓	↓	↓	↓ ↓
1	0	1	1	0	0	1	X11 - Y4
0	0	0	0	1	0	1	X0 - Y5
↓	↓	↓	↓	↓	↓	↓	↓ ↓
1	0	1	1	1	0	1	X11 - Y5
0	0	0	0	0	1	1	X0 - Y6
↓	↓	↓	↓	↓	↓	↓	↓ ↓
1	0	1	1	0	1	1	X11 - Y6
0	0	0	0	1	1	1	X0 - Y7
↓	↓	↓	↓	↓	↓	↓	↓ ↓
1	0	1	1	1	1	1	X11 - Y7

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	– 0.5 to 14	V
V_{IN}	Input Voltage Range	– 0.5 to V_{DD} + 0.5	V
P_{tot}	Power Dissipation	1	W
T_{op}	Operating Temperature Range	0 to 70	°C
T_{stg}	Storage Temperature Range	– 50 to 125	°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	10	V
T_{op}	Operating Temperature	0 to 70	°C
V_{IN}	(logic signal)	0 to V_{DD}	

STATIC ELECTRICAL CHARACTERISTICS (T_{amb} = 0 to 70 °C, V_{DD} = 10 V)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_s	Supply Current	Reset = V_{DD}			1	mA

CROSSPOINT

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
	On Resistance	V_{IDC} = 4.75 V V_{ODC} = 4.5 V (see fig. 1)		60	100	Ω
	On Resistance Variation			6	10	Ω
	Off Leakage*	All switches off $V_{OS} = V_{IS} = 0$ to V_{DD}			± 3	µA

CONTROLS

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{IL}					0.8	V
V_{IH}			2.4			V
	Input Leakage*	V_{IN} = 0 to V_{DD}			± 3	µA

* The device is guaranteed with such limits up to 70°C. At 25°C these limits become ± 100nA

DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb} = 25 °C, C_L = 50 pF all input square wave rise and fall times = 10 ns, V_{DD} = 10 V)

CROSSPOINTS

Symbol	Parameter	Test Conditions				Value			Unit
		Note	f_q (KHz)	R_h (KΩ)	V_{is} (Vpp)	Min.	Typ.	Max.	
t_{PHL}, t_{PLH}	Propagation Delay Time (switch ON) Signal Input to Output	Fig. 2		1	2		30	100	ns
	Frequency Response (any switch ON) 20 log (V_{OS}/V_{IS}) = – 3 dB	C_L = 3 pF		0.081	2		50		MHz
	Sine Wave Distortion		1	0.6	8			1	%
	Feed Through (any switches OFF)	Fig. 3	10	1	2	– 80			dB
	Frequency For Signal Crosstalk Attenuation of 40 dB Attenuation of 110 dB	Fig. 4		1	2	1 5			MHz KHz
C	Capacitance Xn to Ground						15		pF
	V_n to Ground		1000		0.1		15		
	Feed Through						0.4		
C	Capacitance Logic Input to Ground		1000		0.1		5		pF

DYNAMIC ELECTRICAL CHARACTERISTICS (continued)

CONTROLS

Symbol	Parameter	Test Conditions		Value			Unit
		V_{DD} = 10 V	See Fig.	Min.	Typ.	Max.	
t_{PSN}	Propagation Delay Time Strobe to Output (switch turn-ON to high level)	R_L = 1 KΩ C_L = 50 pF t_r, t_f = 10 ns	5		150	200	ns
t_{PZH}	Data-in to Output (turn-ON to high level)		6		150	200	ns
t_{PAN}	Address to Output (turn-ON to high level)		7		150	200	ns
t_{PSF}	Propagation Delay Time Strobe to Output (switch turn-OFF)		5		150	200	ns
t_{PZL}	Data-in to Output (turn-ON to low level)		6		150	200	ns
t_{PAF}	Address to Output (turn-OFF)		7		150	200	ns
t_S	Set-UP Time Data-in to Strobe		5, 10	20			ns
t_H	Hold time Data-in to Strobe		5, 10	120			ns
t_o	Switching Frequency				1		MHz
t_W	Strobe Pulse Width		10	100			ns
t_{WR}	Reset Pulse Width		9	150			ns
t_{PHZ}	Reset Turn-OFF to Output Delay		9		150	200	ns
t_{AS}	Address Set-UP Time Address to Strobe		10	20			ns
t_{AH}	Address Hold Time Address to Strobe		10	20			ns
	Control Crosstalk Data-in, Address, or Strobe to Output	Square Wave V_{IN} = 3 V Input t_r, t_f = 10 ns R_L = 10 kΩ	8		75		mV

TEST CIRCUITS

Figure 1 : R_{ON} Measurement.

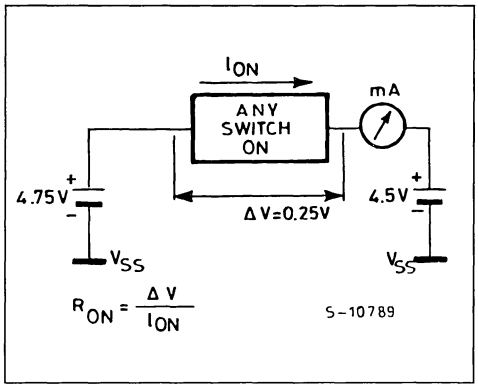


Figure 2 : Propagation Delay Time and Waveforms (signal input to signal output switch ON).

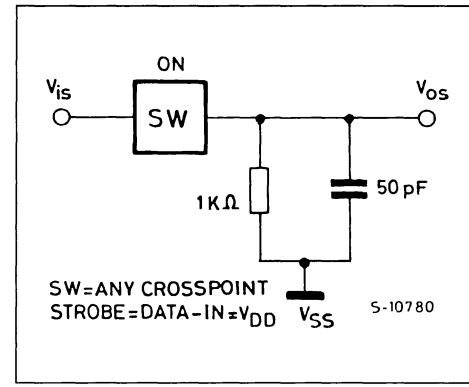
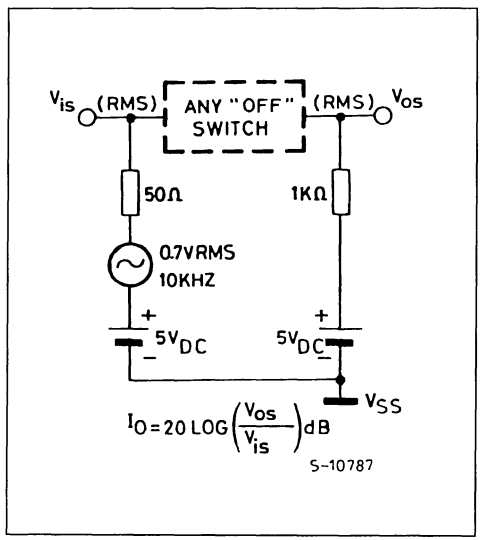


Figure 3 : Off Isolation Measurement (Feed through).



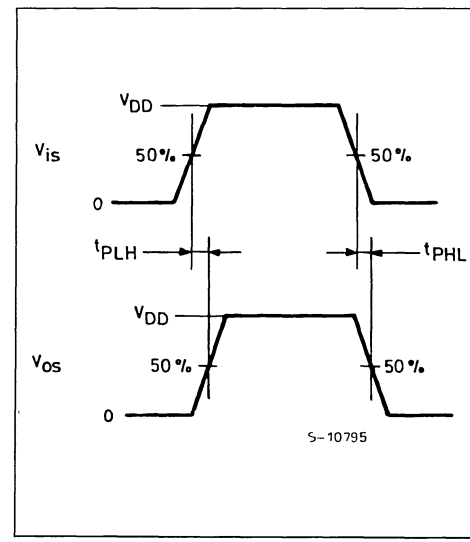


Figure 4 : Crosstalk Measurements.

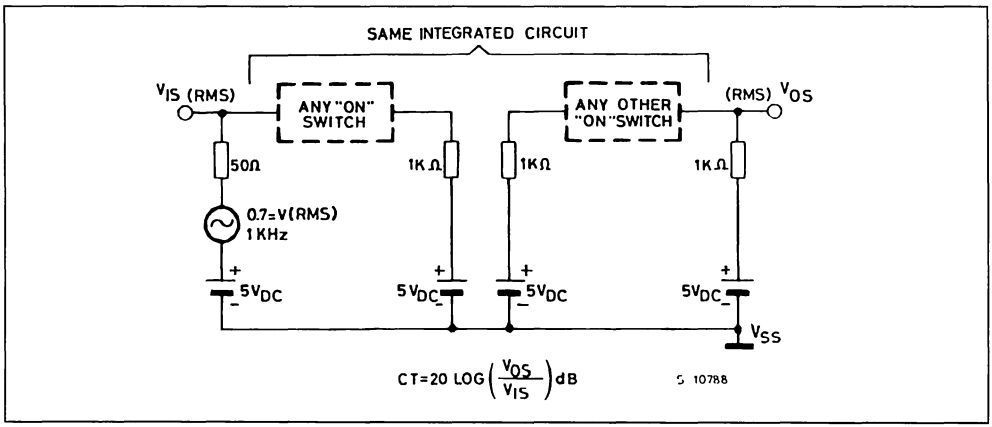


Figure 5 : Propagation Delay Time and Waveforms (strobe to signal output switch Turn-ON or Turn-OFF).

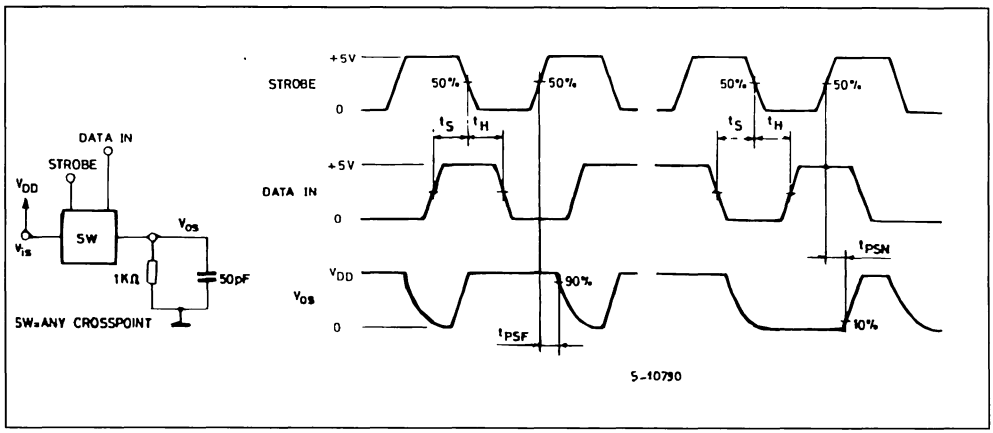


Figure 6 : Propagation Delay Time and Waveforms (data-in signal output, switch Turn-ON to high or low level).

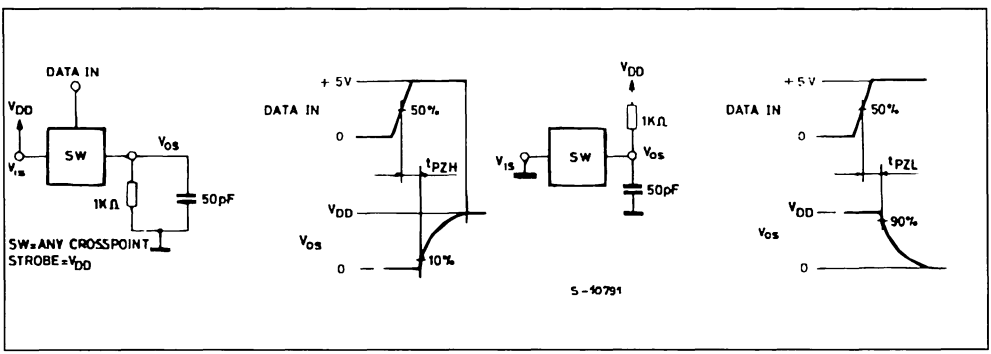


Figure 7 : Propagation Delay Time and Waveforms (address to signal output switch Turn-ON or Turn-OFF).

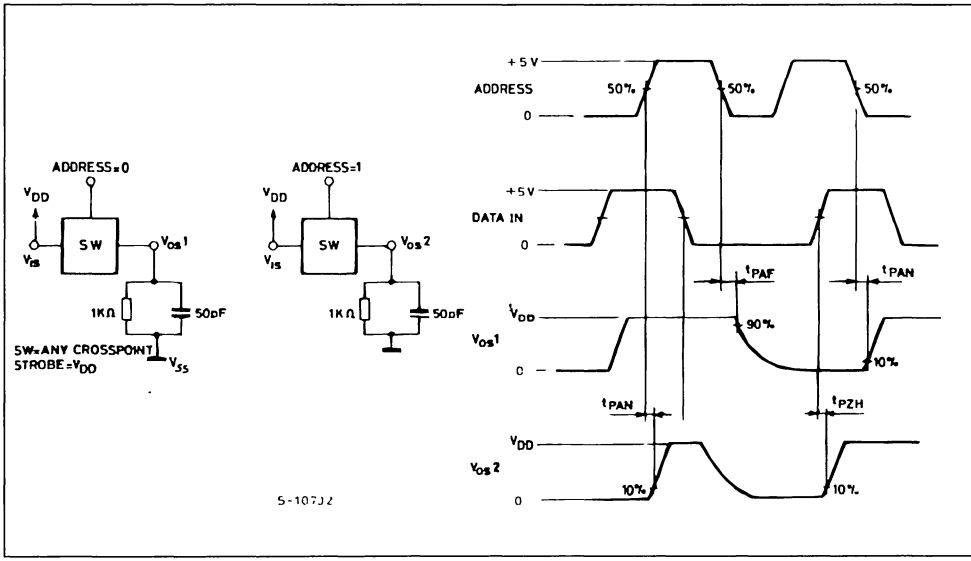


Figure 8 : Waveforms for Crosstalk (control input to signal output).

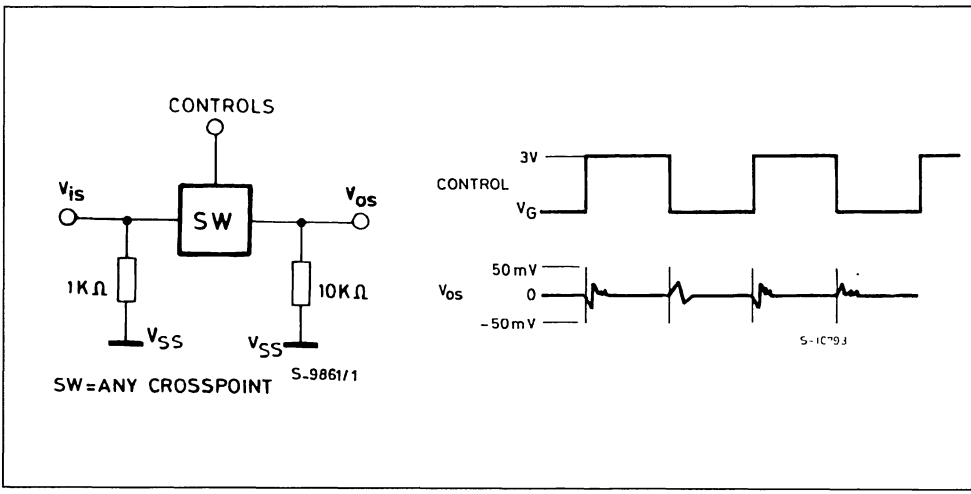


Figure 9 : Propagation Delay Time and Waveforms (reset to output delay).

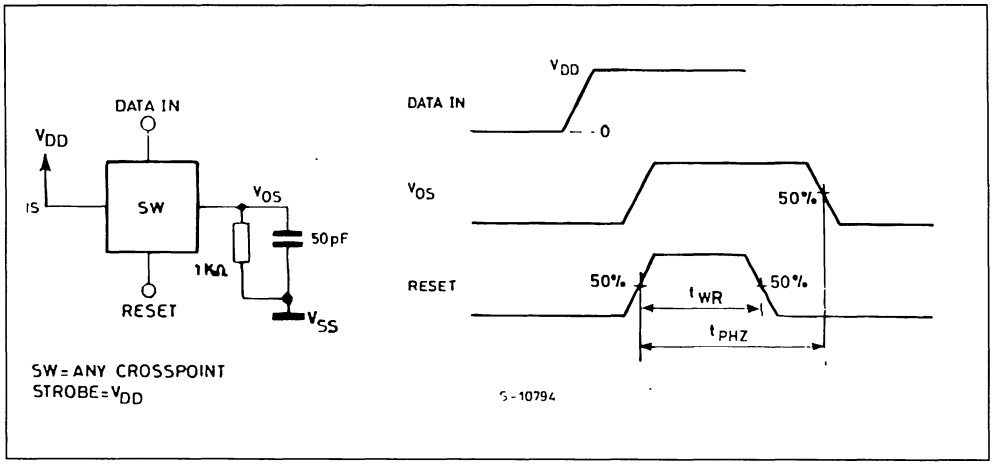


Figure 10 : Propagation Delay Time and Waveforms (Strobe and C/S to signal output switch).

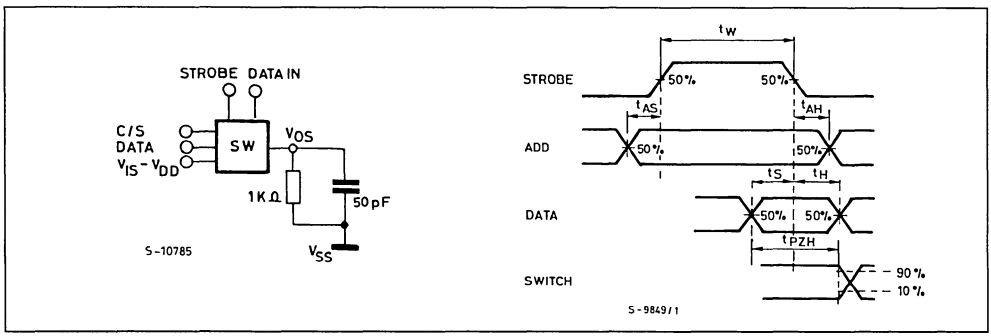


Figure 11 : Typical R_{ON} versus V_{IS}.

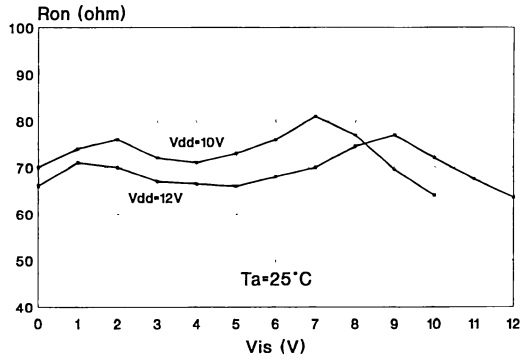


Figure 12 : Peak to Peak Voltage Capability versus Total Harmonic Distortion.

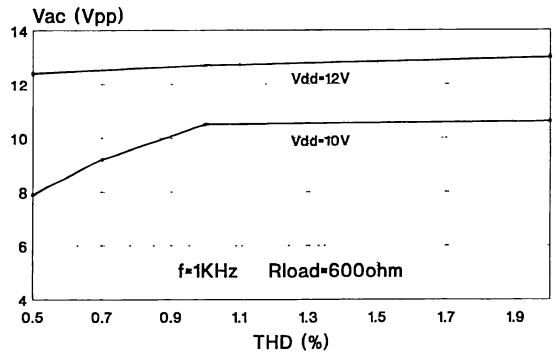
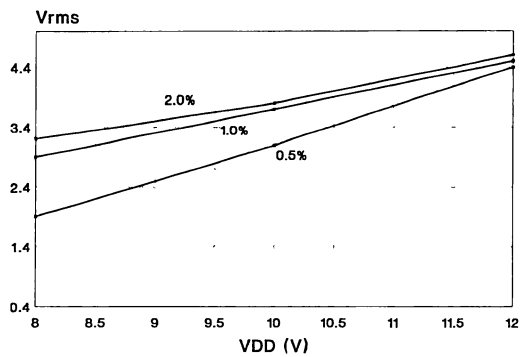


Figure 13 : V_{RMS} Capability versus V_{DD}.



TYPICAL APPLICATIONS

The figures 14, 15 and 16 show the system configuration for expanded matrices (16 x 16, 8 x 64, 32 x 32).

Figure 14 : (16 x 16 non blocking matrix).

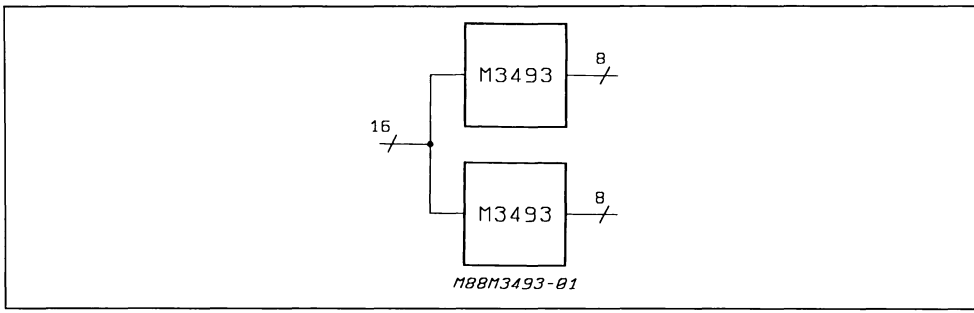


Figure 15 : (8 x 64 matrix).

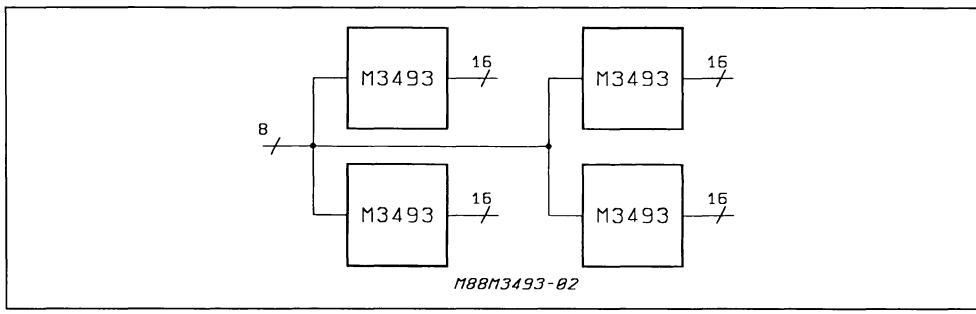
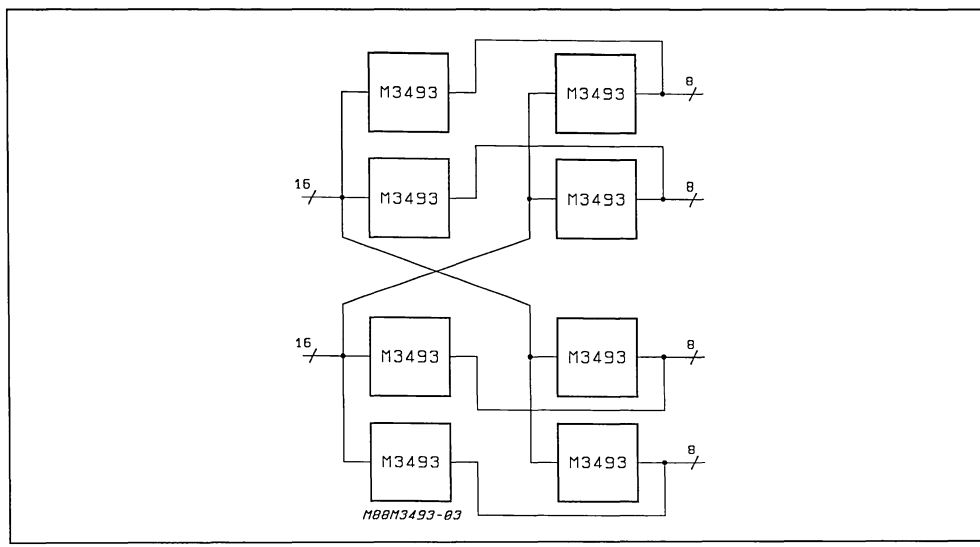
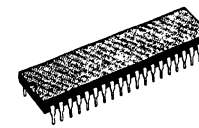


Figure 16 : (32 x 32 non blocking matrix).

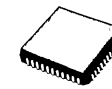


CMOS 16 X 8 CROSSPOINT WITH CONTROL MEMORY

- LOW ON RESISTANCE (typ. 60 Ω at V_{DD} = 10 V)
- INTERNAL CONTROL LATCHES
- ANALOG SIGNAL SWING CAPABILITY EQUAL TO POWER SUPPLY VOLTAGE APPLIED
- LESS THAN 1 % TOTAL DISTORT. AT 0 dBm
- LESS THAN – 95 dB CROSS-TALK AT 1 KHz 1 V_{pp}
- VERY LOW POWER CONSUMPTION



DIP40
(Plastic)



PLCC44

ORDER CODES : M3494 B1
M3494 C1

DESCRIPTION

The M3494 contains a 16 x 8 array of crosspoint together with a 7 to 128 line decoder and latch circuits. Anyone of the 128 switches can be addressed by selecting the appropriate 7 input bits. The selected switch can be turned on or off by applying a logical one or zero to the data in and the strobe input at logical one. A reset signal can be used to turn off all the switches together when is set at logical one.

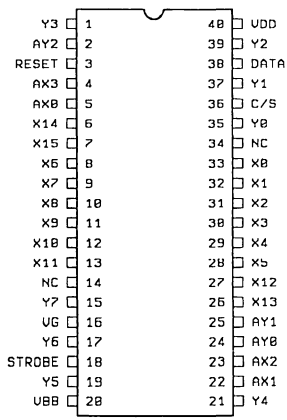
The input pin V_G shifts the logic level of the digital inputs. It allows one M3494 supplied between V_{BB} and V_{DD} to have input logic levels equal to V_G and V_{DD}.

M3494 can handle analog signals with an amplitude equal to the voltage power supply.

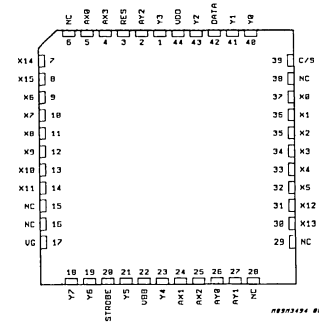
The C/S allows the control inputs of different devices to be connected in parallel in multiple chip system. Each device is selected when its own C/S input pin is high level.

M3494 is available in 40 lead dual in-line plastic, or 44 lead plastic chip carrier packages.

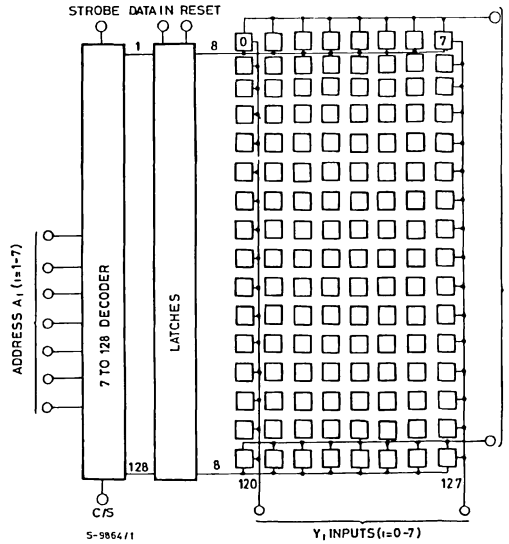
PIN CONNECTION (top view)



CHIP CARRIER



BLOCK DIAGRAM



INPUT/OUTPUT DESCRIPTION

POWER

I/O	Symbol	Pin	Description
I	V_{DD}	40	Positive Power Supply
I	V_{BB}	20	Negative Power Supply
I	V_G	16	Digital Signal Ground

ADDRESS

I/O	Symbol	Pin	Description
I	AX0-AX3	4, 5, 22, 23	X Address Lines. These 4 pins are used to select one of the 16 rows of switches. Refer to the truth table for legal address.
I	AY0-AY2	2, 24, 25	Y Address Lines. These 3 pins are used to select one of the 8 columns of switches. Refer to the truth table for legal address.

CONTROL

I/O	Symbol	Pin	Description
I	DATA	38	This input determines if the selected switch will be turned on (closed) or off (opened). If the pin is held high, the selected switch will be closed. If the pin is held low, the switch will be opened.
I	STROBE	18	This pin enables whatever action is selected by the ADDRESS and DATA pins. When the STROBE pin is held low, no switch openings or closings take place. When the STROBE pin is held high, the switch addressed by the select lines will be opened or closed (depending upon the state of the DATA pin)
I	RESET	3	Master Reset. This pin turns off (opens) all 128 switches. The states of the above control lines are irrelevant. This pin is active high.
I	C/S	36	Chip Select. This pin allow the input control lines of different M3494's to be connected in parallel in multiple chip system. This pin is active high. Each device is selected by its own C/S input pin.

DATA

I/O	Symbol	Pin	Description
I/O	X0-X15	6-13, 26-33	Analog Input/outputs. These pins are connected to the Y0-Y7 pins according to the truth table.
I/O	Y0-Y7	1,15,17,19,21, 35,37,39	Analog Input/outputs. These pins are connected to the X0-X15 pins according to the truth table.

TRUTH TABLE

Address							Connections
AX0	AX1	AX2	AX3	AY0	AY1	AY2	
0	0	0	0	0	0	0	X0 - Y0
1	0	0	0	0	0	0	X1 - Y0
0	1	0	0	0	0	0	X2 - Y0
1	1	0	0	0	0	0	X3 - Y0
0	0	1	0	0	0	0	X4 - Y0
1	0	1	0	0	0	0	X5 - Y0
0	1	1	0	0	0	0	X12 - Y0
1	1	1	0	0	0	0	X13 - Y0
0	0	0	1	0	0	0	X6 - Y0
1	0	0	1	0	0	0	X7 - Y0
0	1	0	1	0	0	0	X8 - Y0
1	1	0	1	0	0	0	X9 - Y0
0	0	1	1	0	0	0	X10 - Y0
1	0	1	1	0	0	0	X11 - Y0
0	1	1	1	0	0	0	X14 - Y0
1	1	1	1	0	0	0	X15 - Y0
0	0	0	0	1	0	0	X0 - Y1
↓	↓	↓	↓	↓	↓	↓	↓ ↓
1	1	1	1	1	0	0	X15 - Y1
0	0	0	0	0	1	0	X0 - Y2
↓	↓	↓	↓	↓	↓	↓	↓ ↓
1	1	1	1	0	1	0	X15 - Y2
0	0	0	0	1	1	0	X0 - Y3
↓	↓	↓	↓	↓	↓	↓	↓ ↓
1	1	1	1	1	1	0	X15 - Y3
0	0	0	0	0	0	1	X0 - Y4
↓	↓	↓	↓	↓	↓	↓	↓ ↓
1	1	1	1	0	0	1	X15 - Y4
0	0	0	0	1	0	1	X0 - Y5
↓	↓	↓	↓	↓	↓	↓	↓ ↓
1	1	1	1	1	0	1	X15 - Y5
0	0	0	0	0	1	1	X0 - Y6
↓	↓	↓	↓	↓	↓	↓	↓ ↓
1	1	1	1	0	1	1	X15 - Y6
0	0	0	0	1	1	1	X0 - Y7
↓	↓	↓	↓	↓	↓	↓	↓ ↓
1	1	1	1	1	1	1	X15 - Y7

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage (V_{BB} = 0)	– 0.5 to 14	V
V_{IN}	Input Voltage Range	V_G – 0.5 to V_{DD} + 0.5	V
P_{tot}	Power Dissipation	1	W
T_{op}	Operating Temperature Range	0 to 70	°C
T_{stg}	Storage Temperature Range	– 50 to 125	°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{DD} V_{BB}	Supply Voltages	$V_G = 0$	+ 5 ± 10 % − 5 ± 10 %	
T_{op}	Operating Temperature		0 to 70	°C
V_{IN}	(logic signal)		V_G to V_{DD}	

STATIC ELECTRICAL CHARACTERISTICS (T_{amb} = 0 to 70 °C, V_{DD} = + 5 V, V_{BB} = − 5 V, V_G = 0 V)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_s	Supply Current	Reset = V_{DD}			1	mA

CROSSPOINT

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
	On Resistance	V_{IDC} = 0.75 V	V_{ODC} = 0.5 V (see fig. 1)		60	100	Ω
	On Resistance Variation				6	10	Ω
	Off Leakage*	All switches off	$V_{OS} = V_{IS}$ = V_{BB} to V_{DD}			± 3	µA

CONTROLS

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{IL}					0.8	V
V_{IH}			2.4			V
	Input Leakage*	$V_{IN} = V_G$ to V_{DD}			± 3	µA

DYNAMIC ELECTRICAL CHARACTERISTICS(T_{amb} = 25 °C, C_L = 50 pF all input square wave rise and fall times = 10 ns, V_{DD} = + 5 V, V_{BB} = – 5 V, V_G = 0 V)

CROSSPOINTS

Symbol	Parameter	Test Conditions				Value			Unit
		Note	f_i (KHz)	R_L (KΩ)	V_{is} (Vpp)	Min.	Typ.	Max.	
t_{PHL}, t_{PLH}	Propagation Delay Time (switch ON) Signal Input to Output	Fig. 2		1			30	100	ns
	Frequency Response (any switch ON) 20 log (V_{OS}/V_{IS}) = – 3 dB	C_L = 3 pF		0.091	2			50	MHz
	Sine Wave Distortion		1	0.6	8			1	%
	Feedthrough (any switches OFF)	Fig. 3	10	1	2	– 90			dB
	Frequency For Signal Crosstalk Attenuation of 40 dB Attenuation of 110 dB	Fig. 4			1	2	1 5		MHz KHz
C	Capacitance Xn to V_{BB}							15	pF
	Y_n to V_{BB}		1000		0.1	15			
	Feedthrough							0.4	
C	Capacitance Logic Input to V_G		1000		0.1	5		pF	

DYNAMIC ELECTRICAL CHARACTERISTICS (continued)

CONTROLS

Symbol	Parameter	Test Conditions	See Fig.	Value			Unit
		V_{DD} = + 5 V V_G = 0 V V_{BB} = − 5 V		Min.	Typ.	Max.	
t_{PSN}	Propagation Delay Time Strobe to Output (switch turn-ON to high level)	R_L = 1 KΩN C_L = 50 pF t_r, t_f = 10 ns	5		150	200	ns
t_{PZH}	Data-in to Output (turn-ON to high level)		6		150	200	ns
t_{PAN}	Address to Output (turn-ON to high level)		7		150	200	ns
t_{PSF}	Propagation Delay Time Strobe to Output (switch turn-OFF)		5		150	200	ns
t_{PZL}	Data-in to Output (turn-ON to low level)		6		150	200	ns
t_{PAF}	Address to Output (turn-OFF)		7		150	200	ns
t_S	Set-UP Time Data-in to Strobe or C/S		5, 10	20			ns
t_H	Hold Time Data-in to Strobe or C/S		5, 10	120			ns
t_o	Switching Frequency				1		MHz
t_W	Strobe Pulse Width C/S Pulse Width		10	100			ns
t_{WR}	Reset Pulse Width		9	150			ns
t_{PHZ}	Reset Turn-OFF to Output Delay		9		150	200	ns
t_{AS}	Address Set-UP Time Address to Strobe or C/S		10	20			ns
t_{AH}	Address Hold Time Address to Strobe or C/S		10	20			ns
	Control Crosstalk Data-in, Address, or Strobe to Output	Square Wave V_{IN} = 3 V Input t_r, t_f = 10 ns R_L = 10 kΩ	8		75		mV

TEST CIRCUITS

Figure 1 : RON Measurement.

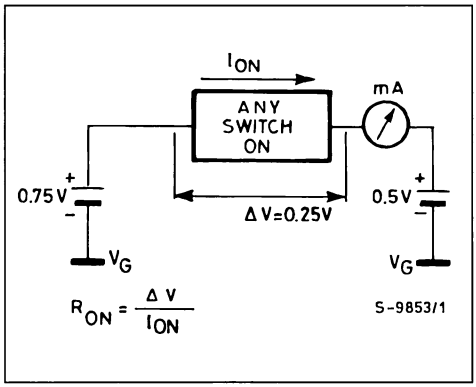


Figure 2 : Propagation Delay Time and Waveforms (signal input to signal output switch ON).

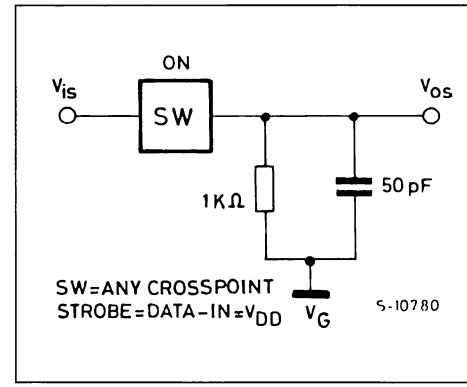
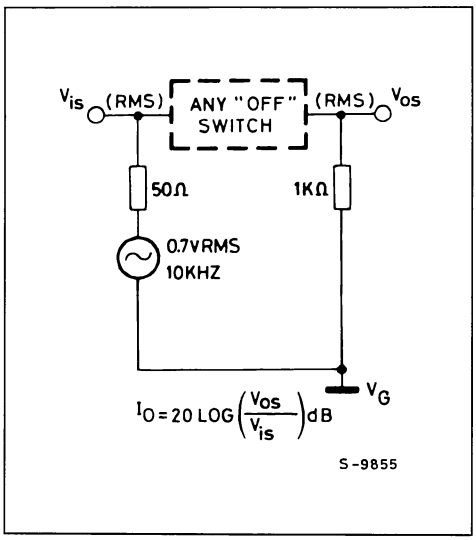


Figure 3 : Off Isolation Measurement (Feed through).



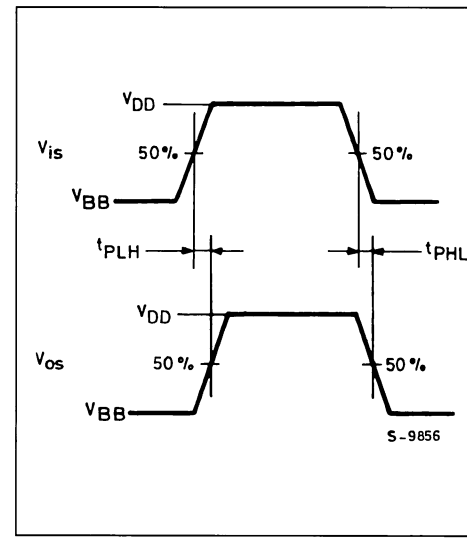


Figure 4 : Crosstalk Measurements.

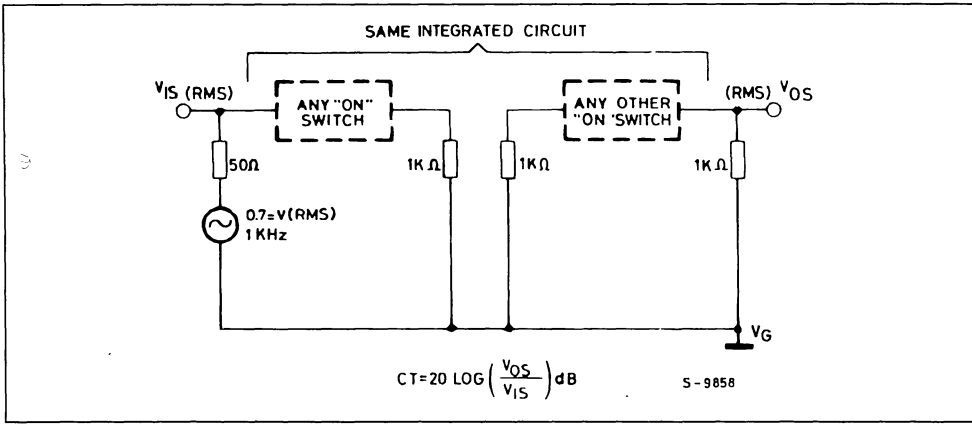


Figure 5 : Propagation Delay Time and Waveforms (strobe to signal output switch Turn-ON or Turn-OFF).

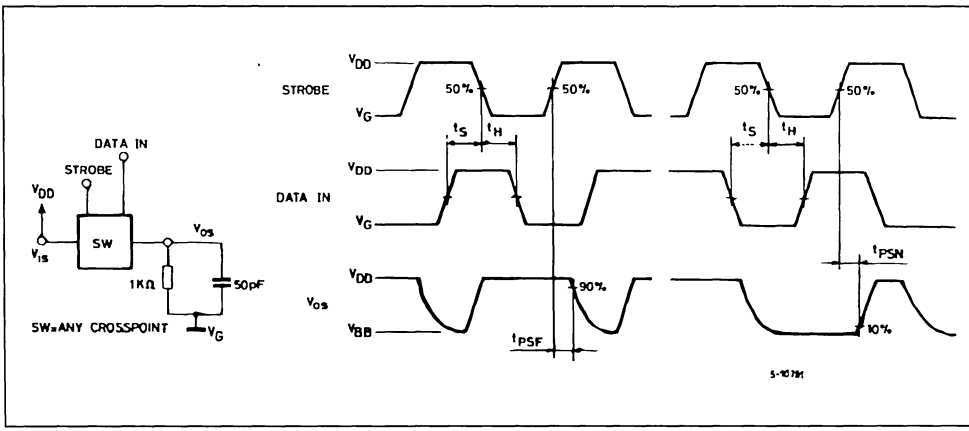


Figure 6 : Propagation Delay Time and Waveforms (data-in signal output, switch Turn-ON to high or low level).

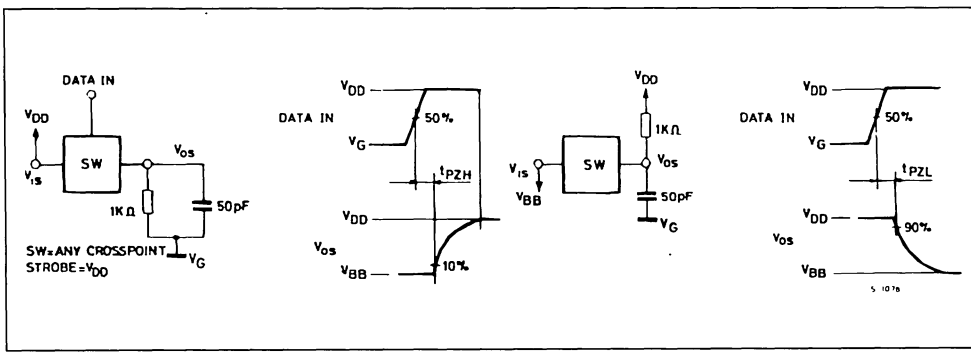


Figure 7 : Propagation Delay Time and Waveforms (address to signal output switch Turn-ON or Turn-OFF).

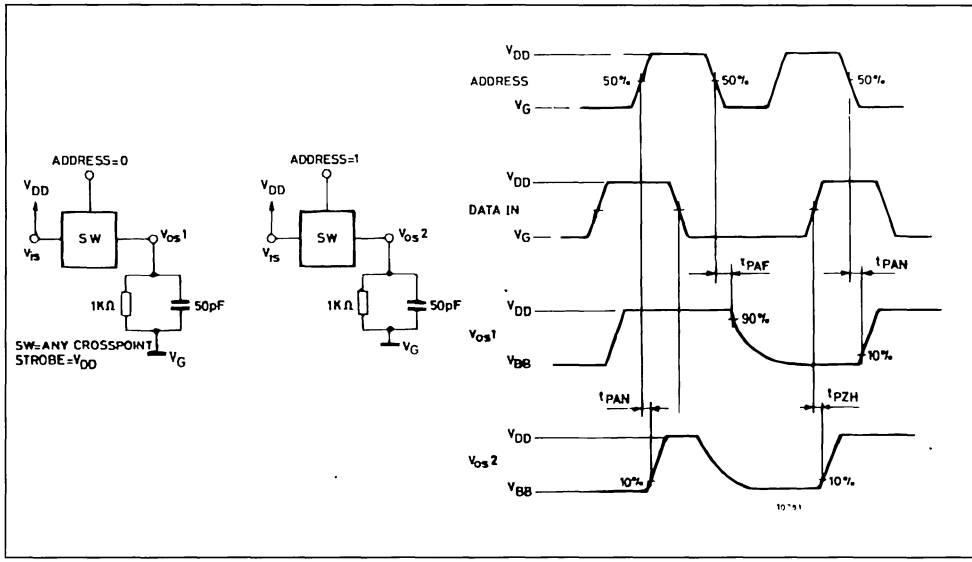


Figure 8 : Waveforms for Crosstalk (control input to signal output).

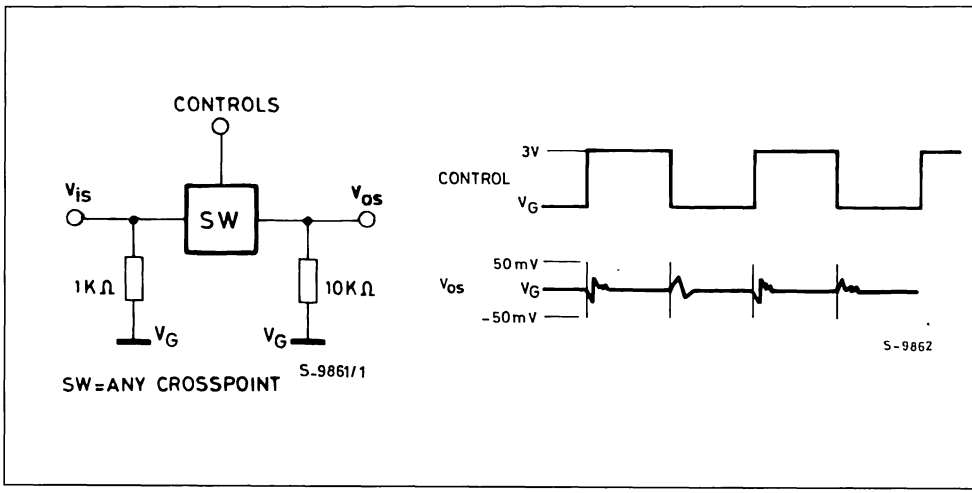


Figure 9 : Propagation Delay Time and Waveforms (reset to output delay).

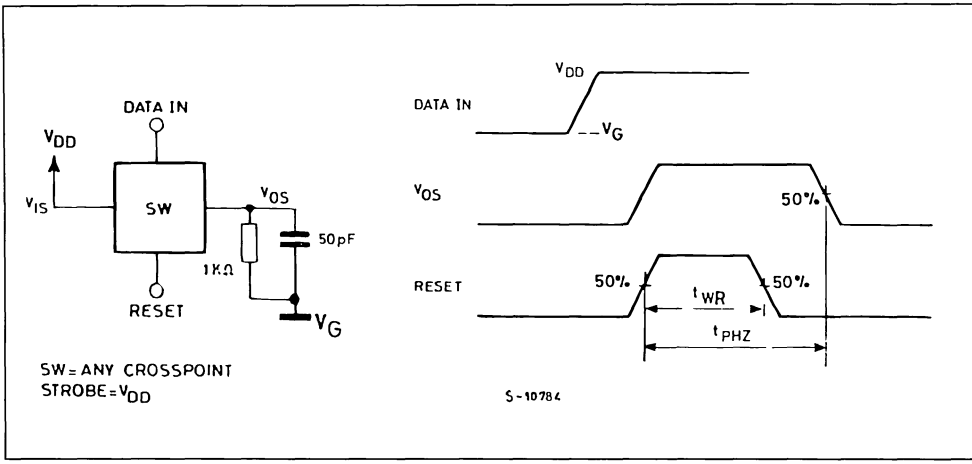


Figure 10 : Propagation Delay Time and Waveforms (Strobe and C/S to signal output switch).

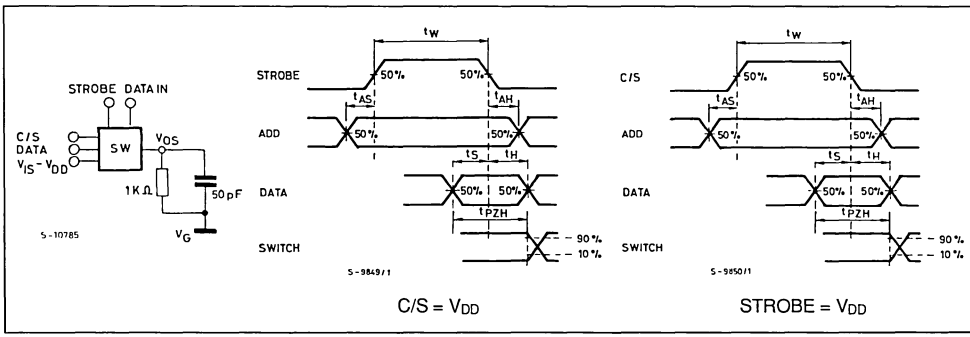


Figure 11 : Typical R_{ON} versus V_{is}.

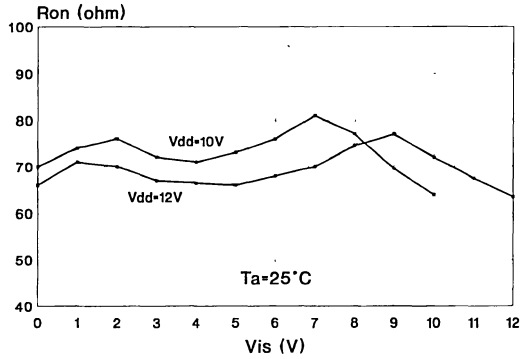


Figure 12 : Peak to Peak Voltage Capability versus Total Harmonic Distortion.

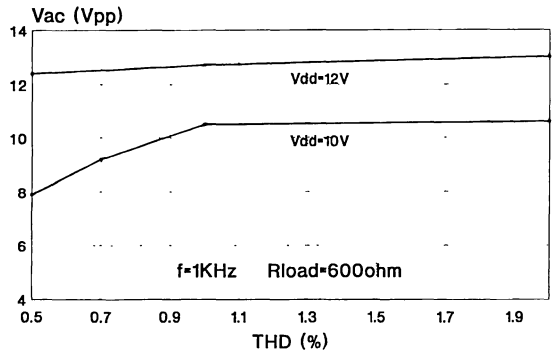
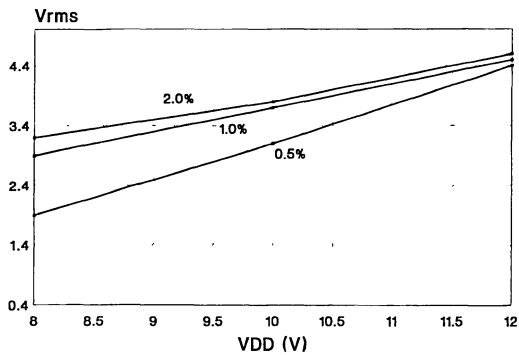


Figure 13 : V_{RMS} Capability versus V_{DD}.



TYPICAL APPLICATIONS

The figures 14, 15 and 16 show the system configuration for expanded matrices (16 x 16, 8 x 64, 32 x 32).

Figure 14 : (16 x 16 non blocking matrix).

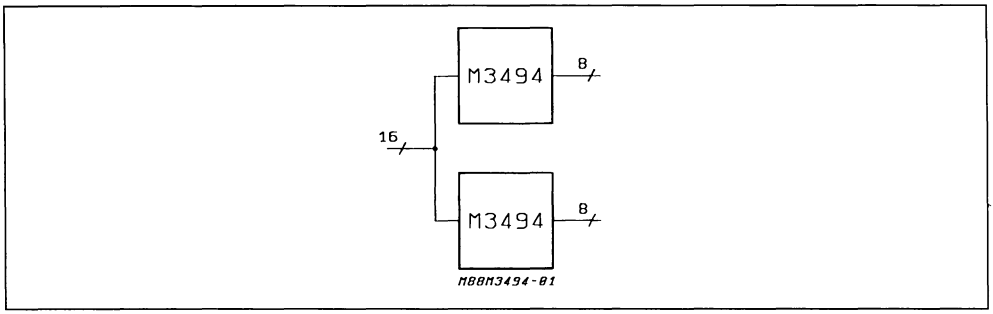


Figure 15 : (8 x 64 matrix).

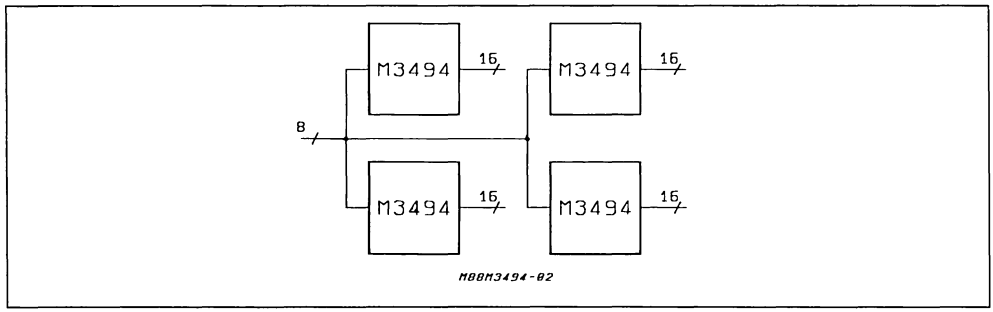
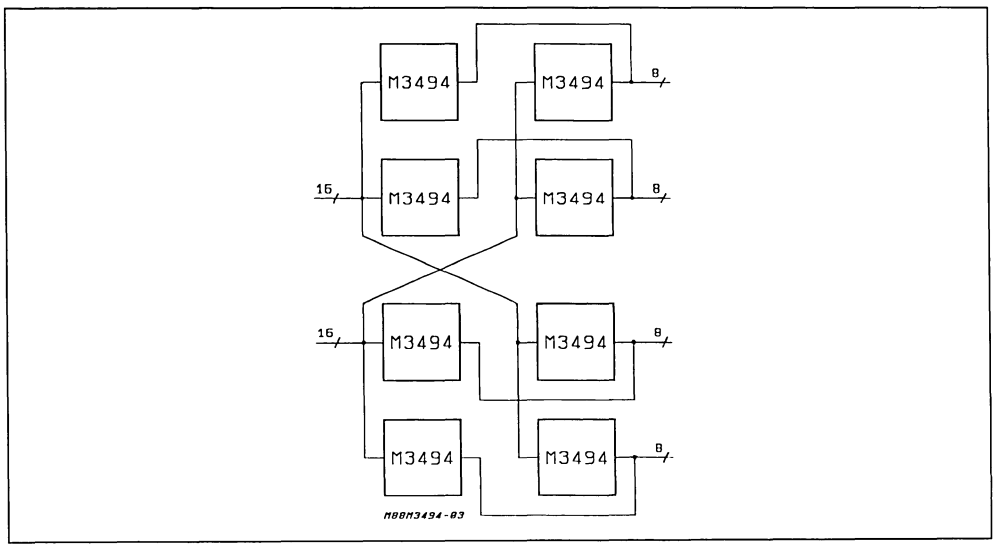


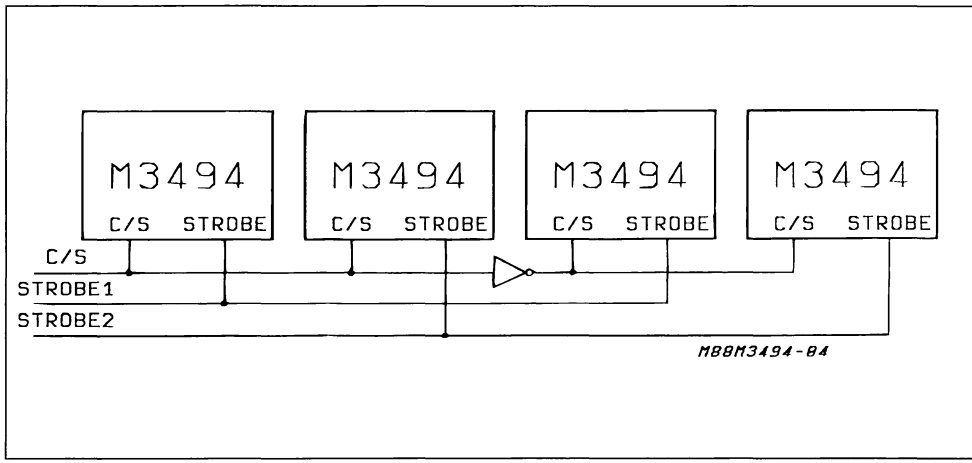
Figure 16 : (32 x 32 non blocking matrix).



The availability of the C/S input in addition of the STROBE input aids the addressing circuit for expanded matrices.

Fig. 17 shows an example, the selection circuit for a matrix with 4 x M3494 that implement this function with only one extenal inverter.

Figure 17.



Note : The Reset, Data and Address inputs are connected in parallel.

SGS-THOMSON MICROELECTRONICS

M34930

12 X 8 CROSSPOINT

ADVANCE DATA

- LOW ON RESISTANCE (typ. 40Ω at V_{DD} = 10V)
- INTERNAL CONTROL LATCHES
- ANALOG SIGNAL SWING CAPABILITY EQUAL TO POWER SUPPLY VOLTAGE
- LESS THAN 1% TOTAL DISTORT. AT 0dBm
- LESS THAN – 95dB CROSS-TALK AT 1kHz $1V_{PP}$
- VERY LOW POWER CONSUMPTION
- EXPECIALLY OPTIMIZED FOR "ON-HOLD" APPLICATIONS

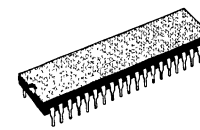
DESCRIPTION

The M34930 contains a 12 x 8 array of crosspoint together with a 7 to 96 line decoder and latch circuits. Anyone of the 96 switches can be addressed by selecting the appropriate 7 input bits. The selected switch can be turned on or off by applying a logical one or zero to the data in and the strobe input at logical one. A reset signal can be used to turn off all the switches together when is switched at logical one.

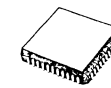
The M34930 can handle signals with an amplitude equal to the supply voltage.

Moreover the device guarantees excellent (60dB) Yi to Yj isolation (for any "i" and "j on Xo channel (grounded).

This feature is used for applications where a service channel (i.e. music) can feed several incoming lines (typically in waiting queue : "on-hold").



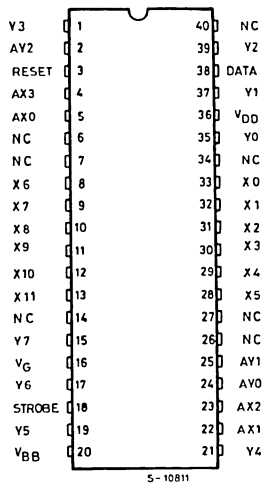
DIP40
(Plastic)



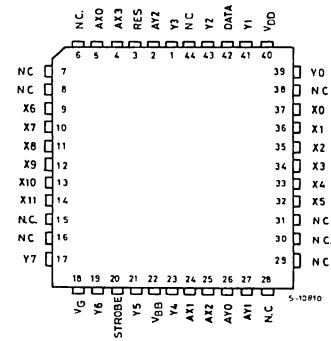
PLCC44

ORDER CODES : M34930B1 (DIP40)
M34930C1 (PLCC44)

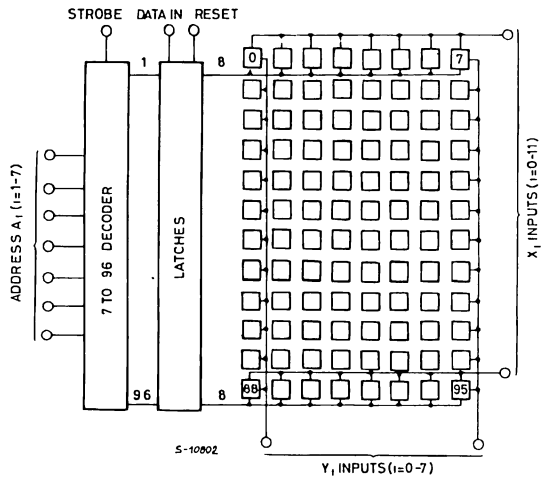
PIN CONNECTIONS (top view)



CHIP CARRIER



BLOCK DIAGRAM



INPUT/OUTPUT DESCRIPTION

POWER

I/O	Symbol	Pin	Description
I	V_{DD}	36	Positive Power Supply
I	V_{BB}	20	Negative Power Supply
I	V_G	16	Digital Signal Ground

ADDRESS

I/O	Symbol	Pin	Description
I	AX0-AX3	4, 5, 22, 23	X Address Lines. These 4 pins are used to select one of the 16 rows of switches. Refer to the truth table for legal address.
I	AY0-AY2	2, 24, 25	Y Address Lines. These 3 pins are used to select one of the 8 columns of switches. Refer to the truth table for legal address.

CONTROL

I/O	Symbol	Pin	Description
I	DATA	38	This input determines if the selected switch will be turned on (closed) or off (opened). If the pin is held high, the selected switch will be closed. If the pin is held low, the switch will be opened.
I	STROBE	18	This pin enables whatever action is selected by the ADDRESS and DATA pins. When the STROBE pin is held low, no switch openings or closings take place. When the STROBE pin is held high, the switch addressed by the select lines will be opened or closed (depending upon the state of the DATA pin)
I	RESET	3	Master Reset. This pin turns off (opens) all 96 switches. The states of the above control lines are irreleant. This pin is active high.

DATA

I/O	Symbol	Pin	Description
I/O	X0-X11	8-13, 28-33	Analog Input/Outputs. These pins are connected to the Y0-Y7 pins in according to the truth table.
I/O	Y0-Y7	1,15,17,19,21 35,37,39	Analog Input/Outputs. These pins are connected to the X0-X11 pins in according to the truth table.

GENERAL INFORMATIONS

- TRUTH TABLE
  (see M3493 data sheet)
- ABSOLUTE MAXIMUM RATINGS
  (see M3493 data sheet)
- RECOMMENDED OPERATING CONDITIONS
  (see M3494 data sheet)
- STATIC AND DYNAMIC ELECTRICAL CHARACTERISTICS
  (see M3494 data sheet)

SGS-THOMSON MICROELECTRONICS

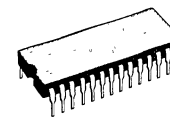
M044

128 X 128 DIGITAL SWITCHING MATRIX

- 128 INPUT AND 128 OUTPUT CHANNEL DIGITAL SWITCHING MATRIX (non blocking)
- TYPICAL APPLICATION IN PABX
- PCM INPUTS AND OUTPUTS MATUALLY COMPATIBLE
- ACTUAL INPUT-OUTPUT CHANNEL CONNECTIONS STORED AND MODIFIED VIA AN ON-CHIP 8-BIT PARALLEL MICROPROCESSOR INTERFACE
- 5 MAIN "FUNCTIONS" or "INSTRUCTIONS" AVAILABLE
- TYPICAL BIT RATE : 2Mbit/s
- TYPICAL SYNCHRONIZATION RATE : 8 KHz (time frame is 125 µs)
- 5 VOLT POWER SUPPLY WITH INTERNALLY GENERATED BIAS VOLTAGE
- MOS & TTL INPUT/OUTPUT LEVELS COMPATIBLE
- DIFFUSED WITH ST N-CHANNEL SILICON GATE HIGH DENSITY MOS PROCESS

Main instruction controlled by the microprocessor interface

- CHANNEL CONNECTION/DISCONNECTION
- CHANNEL DISCONNECTION
- INSERTION OF A BYTE ON A PCM OUTPUT CHANNEL
- TRANSFER TO THE MICROPROCESSOR OF A SINGLE PCM OUTPUT CHANNEL SAMPLE
- TRANSFER TO THE MICROPROCESSOR OF A SINGLE OUTPUT CONTROL WORD



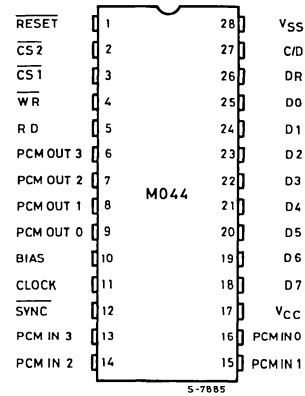
DIP28
(Ceramic)

ORDER CODE : M044F1

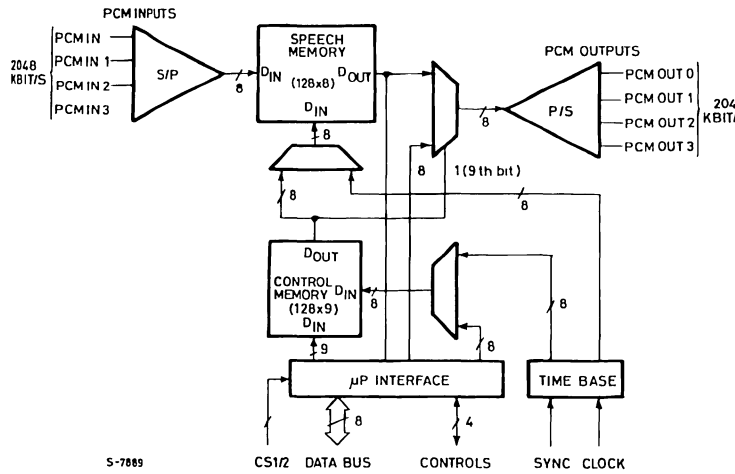
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	– 0.3 to 7	V
V_I	Input Voltage	– 0.3 to 7	V
V_O	Off State Output Voltage	7	V
P_{tot}	Total Package Power Dissipation	1.5	W
T_{stg}	Storage Temperature Range	– 65 to 150	°C
T_{op}	Operating Temperature Range	0 to 70	°C

PIN CONNECTION



BLOCK DIAGRAM



RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	4.75 to 5.25	V
V_I	Input Voltage	0 to 5.25	V
V_O	Off State Input Voltage	0 to 5.25	V
CLOCK Freq.	Input Clock Frequency	4.096	MHz
$\overline{\text{SYNC}}$ Freq.	Input Synchronization Frequency	8	KHz
T_{op}	Operating Temperature	0 to 70	°C

CAPACITANCES (measurements freq. = 1 MHz ; T_{op} = 0 to 70 °C ; unused pins tied to V_{SS})

Symbol	Parameter	Pins	Min.	Typ.	Max.	Unit
C_I	Input Capacitance	6 to 15 ; 26 to 30 ; 32 to 36			5	pf
$C_{I/O}$	I/O Capacitance	20 to 24			15	pf
C_O	Output Capacitance	1 to 4 ; 17 to 19 ; 25 ; 37 to 40			10	pf

DC ELECTRICAL CHARACTERISTICS (T_{amb} = 0 to 70 °C, V_{CC} = 5 V ± 5 %)
All DC characteristics are valid 250 µs after V_{CC} and clock have been applied.

Symbol	Parameter	Pins	Test Conditions	Min.	Typ.	Max.	Unit
V_{ILC}	Clock Input Low Level	6		– 0.3		0.8	V
V_{IHC}	Clock Input High Level	6		3.0		V_{CC}	V
V_{IL}	Input Low Level	7 to 15 20 to 24 26 to 30 32 to 36		– 0.3		0.8	V
V_{IH}	Input High Level	7 to 15 20 to 24 26 to 30 32 to 36		2.0		V_{CC}	V
V_{OL}	Output Low Level	17 to 25	I_{OL} = 1.8 mA			0.4	V
V_{OH}	Output High Level	17 to 25	I_{OH} = 250 µA	2.4			V
V_{OL}	PCM Output Low Level	1 to 4 37 to 40	I_{OL} = 2.0 mA			0.4	V
I_{IL}	Input Leakage Current	6 to 15 26 to 30 32 to 36	V_{IN} = 0 to V_{CC}			10	µA
I_{OL}	Data Bus Leakage Current	17 to 24	V_{IN} = 0 to V_{CC} V_{CC} applied ; Pins 35 and 36 tied to V_{CC}. After device Initialization			± 10	µA
I_{CC}	Supply Current	16	Clock Freq. = 4.096 MHz		170		mA

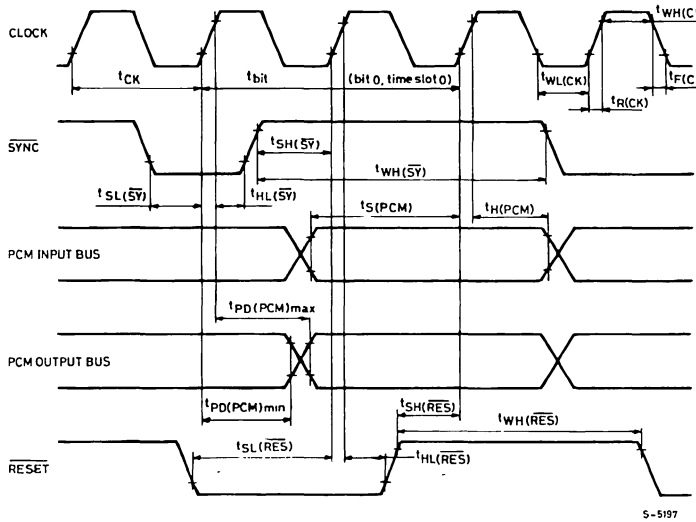
AC ELECTRICAL CHARACTERISTICS (T_{amb} = 0 to 70 °C, V_{CC} = 5 V ± 5 %)
All AC characteristics are valid 250 µs after V_{CC} and clock have been applied. C_L is the max capacitive load and R_L the test pull up resistor.

Signal	Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
CK (clock)	t_{CK}	Clock Period		230			ns
	t_{WL}	Clock Low Level Width		100			ns
	t_{WH}	Clock High Level Width		100			ns
	t_R	Rise Time				25	ns
	t_F	Fall Time				25	ns
$\overline{SYNC}$	t_{SL}	Low Level Setup Time		80			ns
	t_{HL}	Low Level Hold Time		40			ns
	t_{SH}	High Level Setup Time		80			ns
	t_{WH}	High Level Width		t_{CK}			ns
PCM Input Busses	t_S	Setup Time		− 5			ns
	t_H	Hold Time		45			ns
PCM Output Busses	$t_{PO\ min}$	Propagation time referred to CK low level	C_L = 50 pf, R_L = 2 KΩ	45		180	ns
	$t_{PO\ max}$	Propagation time referred to CK high level	C_L = 50 pf, R_L = 2 KΩ	45		200	ns
$\overline{RESET}$	t_{SL}	Low Level Setup Time		100			ns
	t_{HL}	Low Level Hold Time		50			ns
	t_{SH}	High Level Setup Time		90			ns
	t_{WH}	High Level Width		t_{CK}			ns
$\overline{WR}$	t_{WL}	Low Level Width		150			ns
	t_{WH}	High Level Width		t_{CK}			ns
	t_{REP}	Repetition Interval Between Active Pulses	$t_{REP} = 40 + 2\ t_{CK} + t_{WL(CK)} + t_{R(CK)}$	see formula			ns
	t_{SH}	High Level Setup Time to Active Read Strobe		0			ns
	t_{HH}	High Level Hold Time from Active Read Strobe		20			ns
	t_R	Rise Time				60	ns
	t_F	Fall Time				60	ns
$\overline{RD}$	t_{WL}	Low Level Width		180			ns
	t_{WH}	High Level Width		t_{CK}			ns
	t_{REP}	Repetition Interval Between Active Pulses	$t_{REP} = 40 + 2\ t_{CK} + t_{WL(CK)} + t_{R(CK)}$	see formula			ns
	t_{SH}	High Level Setup Time to Active Read Strobe		0			ns
	t_{HH}	High Level Hold Time from Active Read Strobe		20			ns
	t_R	Rise Time				60	ns
	t_F	Fall Time				60	

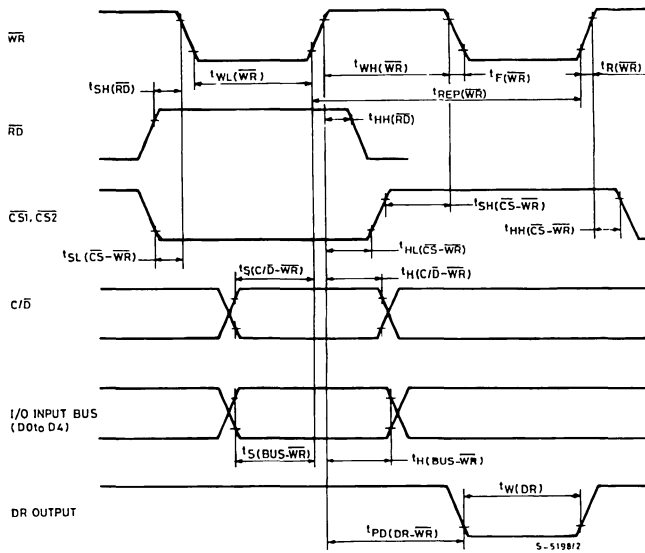
AC ELECTRICAL CHARACTERISTICS (continued)

Signal	Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$\overline{CS1}$, CS2	$t_{SL(\overline{CS}\text{-}\overline{WR})}$	Low level setup time to $\overline{WR}$ falling edge	Active Case	0			ns
	$t_{HL(\overline{CS}\text{-}\overline{WR})}$	Low level hold time from $\overline{WR}$ rising edge	Active Case	0			ns
	$t_{SH(\overline{CS}\text{-}\overline{WR})}$	High level setup time to $\overline{WR}$ falling edge	Inactive Case	0			ns
	$t_{HH(\overline{CS}\text{-}\overline{WR})}$	High level hold time from $\overline{WR}$ rising edge	Inactive Case	0			ns
	$t_{SL(\overline{CS}\text{-}\overline{RD})}$	Low level setup time to $\overline{RD}$ falling edge	Active Case	0			ns
	$t_{HL(\overline{CS}\text{-}\overline{RD})}$	Low level hold time from $\overline{RD}$ rising edge	Active Case	0			ns
	$t_{SH(\overline{CS}\text{-}\overline{RD})}$	High level setup time $\overline{RD}$ falling edge	Inactive Case	0			ns
	$t_{HH(\overline{CS}\text{-}\overline{RD})}$	High level hold time from $\overline{RD}$ rising edge	Inactive Case	0			ns
C/$\overline{D}$	$t_{S(C/\overline{D}\text{-}\overline{WR})}$	Setup time to write strobe end		180			ns
	$t_{H(C/\overline{D}\text{-}\overline{WR})}$	Hold time from write strobe end		25			ns
	$t_{S(C/\overline{D}\text{-}\overline{RD})}$	Setup time to read strobe start		20			ns
	$t_{H(C/\overline{D}\text{-}\overline{RD})}$	Hold time from read strobe end		25			ns
DR (data ready)	t_W	Low state width	Instructions 5 and 6			2-t_{CK}	ns
	t_{PD}	DP output delay from write strobe end (active command)	Instruction 5, C_L = 50 pf	5-t_{CK}		14-t_{CK}	ns
D0 to D7 (interface bus)	$t_{S(BUS\text{-}\overline{WR})}$	Input setup time to write strobe end		130			ns
	$t_{H(BUS\text{-}\overline{WR})}$	Input hold time from write strobe end		25			ns
	$t_{PD(BUS)}$	Propagation time from (active) falling Edge of read strobe	C_L = 200 pF			130	ns
	$t_{HZ(BUS)}$	Propagation time from (active) rising Edge of read strobe to high impedance state				80	ns

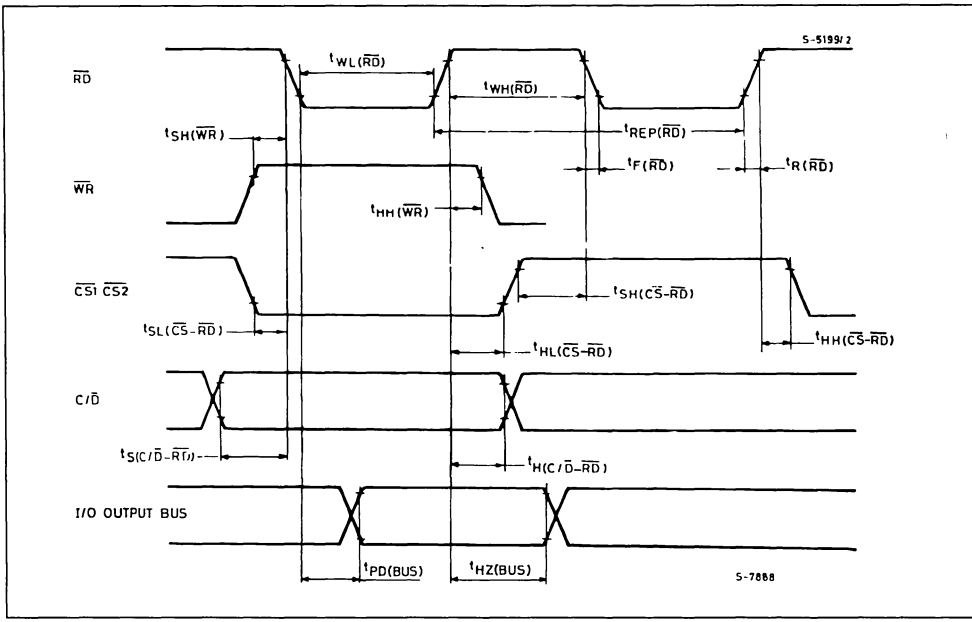
PCM TIMING, $\overline{RESET}$



WRITE OPERATION TIMING



READ OPERATION TIMING



GENERAL DESCRIPTION

The M044 is intended for PABX Systems and digital like concentrators where a micromputer control approach is extensively used. It consists of a speech memory (SM), a control memory (CM), a serial/parallel and a parallel/serial converter, an internal parallel bus, and interface (8 data lines, 11 control signals) and dedicated control logic. By means of repeated clock division two timebases are generated. These are preset from an external synchronisation signal to two specific count numbers so that sequential scanning of the bases give synchronous addresses to the memories and I/O channel controls. The timebase for the input channels is delayed and the timbase for output channels is advanced with respect to the actual time. Each serial PCM input channel is converted to parallel data and stored in the speech memory at the beginning of any new time slot (according to first timebase) in the location determined by input pin number and time slot number. The control memory CM maintains the correspondences between input and output channels.

More exactly for any output pin/output channel combination the control memory gives either the full address of the speech memory location involved in the PCM transfer or an 8-bit word to be supplied to the parallel/serial output converter, A 9th bit at each CM location defines the data source for output links, low for SM, high for CM.

The late timebase is used to scan the output channels and to determine the pins to be serviced within each channel ; enough idle cycles are left to the microprocessor for asynchronous instruction processing.

Two 8-bit registers OR1 and OR2 supply feedback data for control or diagnostic purposes ; OR1 comes from internal bus i.e. from memories, OR2 gives an opcode copy and additional data to the microcomputer. A four byte-five bit stack register and an instruction register, under microcomputer control store input data available at the interface.

PIN DESCRIPTION

D7 to D0 (pins 17 to 24)

Data bus pins. The bidirectional bus is used to transfer data and instructions to / from the microprocessor. D0 is the least significant digit. The output bus is 8 bits wide ; input is only 5 bits wide. The bus is tristate and cannot be used while $\overline{RESET}$ is held low.

The meaning of input data, such as bus or channel numbers, and of expected output data is specified in detail by the instruction description.

C/$\overline{D}$

Input control pin, select pin. In a write operation C/$\overline{D}$ = 0 qualifies any bus content as data, while C/D = 1 qualifies it as an opcode. In a read operation OR1 is selected by C/$\overline{D}$ = 0, OR2 by C/$\overline{D}$ = 1.

$\overline{CS1}$, $\overline{CS2}$

Commutative chip select pins. They enable the device to perform valid read/write operations (active low). Two pins allow row/column selection with different types of microprocessors ; normally one is tied to ground.

$\overline{WR}$

Pin $\overline{WR}$, when $\overline{CS1}$ and $\overline{CS2}$ are low, enables data transfer from microprocessor to the device. Data or opcode and controls are latched on $\overline{WR}$ rising edge. Because of internal clock resynchronization one single additional requirement is recommended in order to procedure a simultaneous instruction execution in a multichip configuration : WR rising edge has to be 20 to 20 + $t_{WL(CK)}$ nsed late relative to clock falling edge.

$\overline{RD}$

When $\overline{CS1}$ and $\overline{CS2}$ are low and a low level on $\overline{RD}$ enables a register OR1 or OR2 read operation, through the bidirectional bus.

In addition, the rising edge of $\overline{RD}$ latches C/$\overline{D}$ and the match condition pins in order to direct the internal flow of operations. Because of internal clock resynchronization, one single additional requirement is recommended in order to produce a simultaneous instruction flow in a multichip configuration : the $\overline{RD}$ rising edge has to be 20 to 20 + $t_{WL(CK)}$ nsec late relative to clock falling edge.

DR

This is the data ready signal, it informs the microprocessor that data is available for reading (through OR1/OR2 registers)

$\overline{RESET}$

$\overline{RESET}$ control pin is normally used at the very beginning to inizialize the device or the network. Any logical status is reset and CM is set all "ones" after $\overline{RESET}$ going low.

The internal initialization routine takes one time frame whatever the $\overline{RESET}$ width on low level (minimum one cycle roughly), but it is repeated an integrer number of time frames as long as $\overline{RESET}$ is found low during 0 time slot.

Initialization pulls the interface bus immediately to a high impedance state. After the CM has been set to all "ones" the PCM output channels are also set to high impedance state (that is pulled to "ones").

CLOCK

Input master clock. Typical frequency is 4.096 MHz. First division gives an internal clock controlling the input and output channels bit rate.

$\overline{SYNC}$

Input synchronization signal is active low. Typical frequency is 8 kHz.

Internal time bases are forced by synchronism to an assigned count number in order to restore channels and bit sequential addressing to a known state. Count difference between the bases is 32, corresponding to two time slots, that is the minimum PCM propagation time, or latency time.

PCM IN 3 TO PCM IN 0

PCM input busses or pins ; they accept a standard 2 Mbit/s rate. Bit 1 (sign bit) is the first of the serial sequence ; in a parallel conversion it is left adjusted as the most significant digit.

PCM OUT3 TO PCM OUT0

PCM output busses or pins ; bit rate and organization are the same as input pins.

Output buffers are open drain type in order to simplify wired-or connections and minimize current spike problems in multichip configuration systems. The device drives the output channels theoretically one bit time before input channels are needed by specifications : this feature allows inputs and outputs to be tied together cancelling any analog delay of digital outputs up to :

$$t_{DEL\,max} = t_{bit} - \overline{t_{PD(PCM)max}} + \underline{t_{PD(PCM)min}}$$

BIAS

Internally generated bias voltage (– 2.5 to – 3.0 V for V_{CC} in the operating range). A max 220 pf capacitor connected to pin 5 provides improved filtering.

MIXED $\overline{RD}$ & $\overline{WR}$ OPERATIONS

In principle $\overline{RD}$ and $\overline{WR}$ operations are allowed in any order within specification constraints.

In practive, only one control pin is low at any given time when CS1 and $\overline{CS2}$ are enabled.

If by mistake or hardware failure both $\overline{RD}$ and $\overline{WR}$ pins are low, the interface bus is internally pushed to tristate condition as long as $\overline{WR}$ is held low and input registers are protected.

Registers OR1 and OR2 can be read in any order with a single $\overline{RD}$ strobe using C/$\overline{D}$ as multiplexing control ; never the less this procedure is not recommended because the device is directed for instruction flow only according to data latched by $\overline{RD}$ rising edge.

Multiple $\overline{RD}$ operations of the same kind ar allowed without affecting the instruction flow : only "new" OR1 or OR2 read operations step the flow.

Input and output registers are held for sure in the previous state for the first 3 cycles following an opcode or an OR2 read.

FUNCTIONAL DESCRIPTION OF SPECIFIC MICROPROCESSOR OPERATIONS

The device, under microprocessor control, performs the following instructions :

1. CHANNEL CONNECTION/DISCONNECTION
2. CHANNEL DISCONNECTION
3. INSERTION OF A BYTE ON A PCM OUTPUT CHANNEL/CHANNEL DISCONNECTION
4. TRANSFER OF A SINGLE PCM OUTPUT CHANNEL SAMPLE
5. TRANSFER OF A SINGLE OUTPUT CHANNEL CONTROL WORD

Any input protocol is started by the microprocessor interface loading the internal stack register with 2 bytes (4 bytes for instructions 1 and 3) qualified as data bytes by C/$\overline{D}$ = 0 and a specific opcode qualified by C/$\overline{D}$ = 1 (match condition is normally needed).

At the end of an instruction it is normally recommended to read one or both registers.

INSTRUCTION TABLES

The most significant digits of OR2 are a copy of the PCM selected output bus ; the least significant digits of OR2 are the opcode. C8 is the control bit. In any case parentheses () define actual register content.

INSTRUCTION 1 : CHANNEL CONNECTION/DISCONNECTION

Control Signals				Data Bus								Notes
C/$\overline{D}$	$\overline{CS}$	$\overline{WR}$	$\overline{RD}$	D7	D6	D5	D4	D3	D2	D1	D0	
0	0	0	1	X	X	X	X	X	Bi2	Bi1	Bi0	1 st Data Byte : selected input bus
0	0	0	1	X	X	X	Ci4	Ci3	Ci2	Ci1	Ci0	2 nd Data Byte : selected input channel
0	0	0	1	X	X	X	X	X	Bo2	Bo1	Bo0	3 rd Data Byte : selected input bus
0	0	0	1	X	X	X	Co4	Co3	Co2	Co1	Co0	4 th Data Byte : selected output channel
1	0	0	1	X	X	X	X	0	0	0	1	Instruction Opcode
0	0	1	0	C7 (Bi2	C6 Bi1	C5 Bi0	C4 Ci4	C3 Ci3	C2 Ci2	C1 Ci1	C0 Ci0)	OR1 : CM Content Copy
1	0	1	0	A7 (Bo2	A6 Bo1	A5 Bo0	C8 0	0 0	0 0	0 0	1 1)	OR2

INSTRUCTION 2 : OUTPUT CHANNEL DISCONNECTION

Control Signals				Data Bus								Notes
C/D	CS	WR	RD	D7	D6	D5	D4	D3	D2	D1	D0	
0	0	0	1	X	X	X	X	X	Bo2	Bo1	Bo0	1 st Data Byte : selected output bus
0	0	0	1	X	X	X	Co4	Co3	Co2	Co1	Co0	2 nd Data Byte : selected output channel
1	0	0	1	X	X	X	X	0	0	1	0	Instruction Opcode
0	0	1	0	1	1	1	1	1	1	1	1	OR1 : CM Content Copy (output channel is inactive)
1	0	1	0	A7 (Bo2	A6 Bo1	A5 Bo0	1 1	0 0	0 0	1 1	0 0)	OR2

INSTRUCTION 3 : LOADING A MICROPROCESSOR BYTE

Control Signals				Data Bus								Notes
C/D	CS	WR	RD	D7	D6	D5	D4	D3	D2	D1	D0	
0	0	0	1	X	X	X	X	X	Ci7	Ci6	Ci5	1 st Data Byte : Most significant digits to be inserted
0	0	0	1	X	X	X	Ci4	Ci3	Ci2	Ci1	Ci0	2 nd Data Byte : Least significant digits to be inserted
0	0	0	1	X	X	X	X	X	Bo2	Bo1	Bo0	3 rd Data Byte : selected output bus
0	0	0	1	X	X	X	Co4	Co3	Co2	Co1	Co0	4 th Data Byte : selected output channel
1	0	0	1	X	X	X	X	0	1	0	0	Instruction Opcode
0	0	1	0	C7 (Ci7	C6 Ci6	C5 Ci5	C4 Ci4	C3 Ci3	C2 Ci2	C1 Ci1	C0 Ci0	OR1 : CM content copy, that is for match condition
1	0	1	0	A7 (Bo2	A6 Bo1	A5 Bo0	1 1	0 0	1 1	0 0	0 0)	OR2 : that is

INSTRUCTION 4 : TRANSFER OF A SINGLE PCM SAMPLE

Control Signals				Data Bus								Notes
C/D	CS	WR	RD	D7	D6	D5	D4	D3	D2	D1	D0	
0	0	0	1	X	X	X	X	X	Bo2	Bo1	Bo0	1 st Data Byte : selected output bus
0	0	0	1	X	X	X	Co4	Co3	Co2	Co1	Co0	2 nd Data Byte : selected output channel
1	0	0	1	X	X	X	X	1	0	1	1	Instruction Opcode
0	0	1	0	C7 S7	C6 S6	C5 S5	C4 S4	C3 S3	C2 S2	C1 S1	C0 S0	OR1 : CM Content Copy if C8 = 1 ; or SM Content Sample if C8 = 0
1	0	1	0	A7 (Bo2	A6 Bo1	A5 Bo0	C8 C8	1 1	0 0	1 1	1 1)	OR2 : that is

Note : S7...S0 is a parallel copy of a PCM data, S7 is the most significant digit and the first of the sequence.

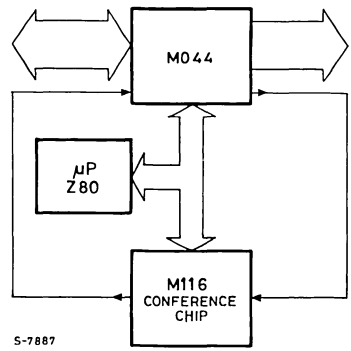
INSTRUCTION 5 : TRANSFER OF AN OUTPUT CHANNEL CONTROL WORD

Control Signals				Data Bus								Notes
C/D	CS	WR	RD	D7	D6	D5	D4	D3	D2	D1	D0	
0	0	0	1	X	X	X	X	X	Bo2	Bo1	Bo0	1 st Data Byte : selected input bus
0	0	0	1	X	X	X	Co4	Co3	Co2	Co1	Co0	2 nd Data Byte : selected input channel
1	0	0	1	X	X	X	X	1	0	0	0	Instruction Opcode
0	0	1	0	C7	C6	C5	C4	C3	C2	C1	C0	OR1 : CM selected CM word copy
1	0	1	0	A7 (Bo2	A6 Bo1	A5 Bo0	C8 0	1 0	0 0	0 0	0 1)	OR2 : that is

CONFERENCE CALL

A kit which includes Z80 µP and the M116 allows a flexible conference call system to be built up in which the participants can enter on any channel of the M044 (refer to M116 data sheet for detailed information).

TYPICAL APPLICATION



SGS-THOMSON
MICROELECTRONICS

3488

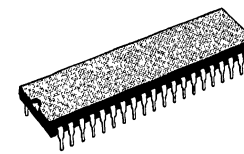
M088

256 x 256 DIGITAL SWITCHING MATRIX

- 256 INPUT AND 256 OUTPUT CHANNEL DIGITAL SWITCHING MATRIX
- BUILDING BLOCK DESIGNED FOR LARGE CAPACITY ELECTRONIC EXCHANGES, SUBSYSTEMS AND PABX
- NO EXTRA PIN NEEDED FOR NOT-BLOCKING SINGLE STAGE AND HIGHER CAPACITY SYNTHESIS BLOCKS (512 or 1024 channels)
- EUROPEAN TELEPHONE STANDARD COMPATIBLE (32 serial channels per frame)
- PCM INPUTS AND OUTPUTS MUTUALLY COMPATIBLE
- INPUT-OUTPUT CHANNEL CONNECTIONS STORED AND MODIFIED VIA ON CHIP 8-BIT PARALLEL MICROPROCESSOR INTERFACE
- 6 MAIN "FUNCTIONS" OR "INSTRUCTIONS" AVAILABLE
- TYPICAL BIT RATE : 2Mbit/s
- TYPICAL SYNCHRONIZATION RATE : 8KHz (time frame is 125µs)
- 5V POWER SUPPLY WITH INTERNALLY GENERATED BIAS VOLTAGE
- MOS & TTL INPUT/OUTPUT LEVELS COMPATIBLE
- SGS-THOMSON N-CHANNEL SILICON GATE HIGH DENSITY MOS PROCESS

Main instructions controlled by the microprocessor interface

- CHANNEL CONNECTION/DISCONNECTION
- CHANNEL DISCONNECTION
- INSERTION OF A BYTE ON A PCM OUTPUT CHANNEL
- TRANSFER TO THE MICROPROCESSOR OF A SINGLE PCM OUTPUT CHANNEL SAMPLE
- TRANSFER TO THE MICROPROCESSOR OF A SINGLE OUTPUT CHANNEL CONTROL WORD
- TRANSFER TO THE MICROPROCESSOR OF A SELECTED 0 CHANNEL PCM INPUT DATA



DIP-40
(Ceramic)

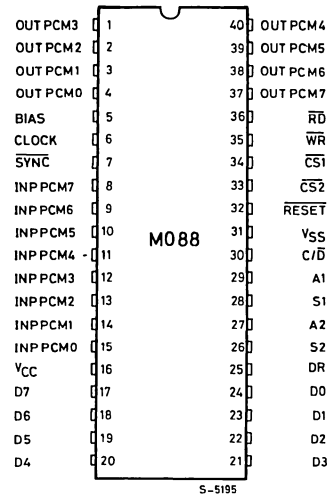
ORDER CODE : M088 F1

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	– 0.3 to 7	V
V_I	Input Voltage	– 0.3 to 7	V
V_O	Off State Output Voltage	7	V
P_{tot}	Total Package Power Dissipation	1.5	W
T_{stg}	Storage Temperature Range	– 65 to 150	°C
T_{op}	Operating Temperature Range	0 to 70	°C

Stresses above those listed under " Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operating conditions of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

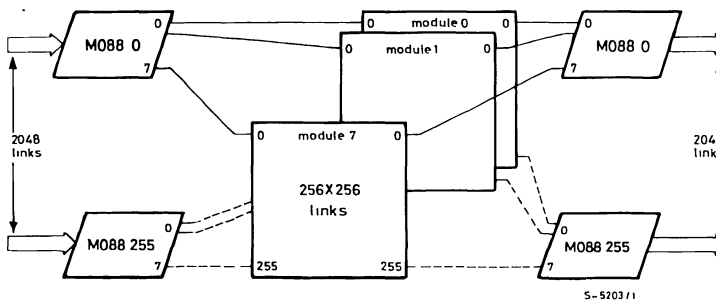
PIN CONNECTIONS



EXCHANGE NETWORKS APPLICATIONS

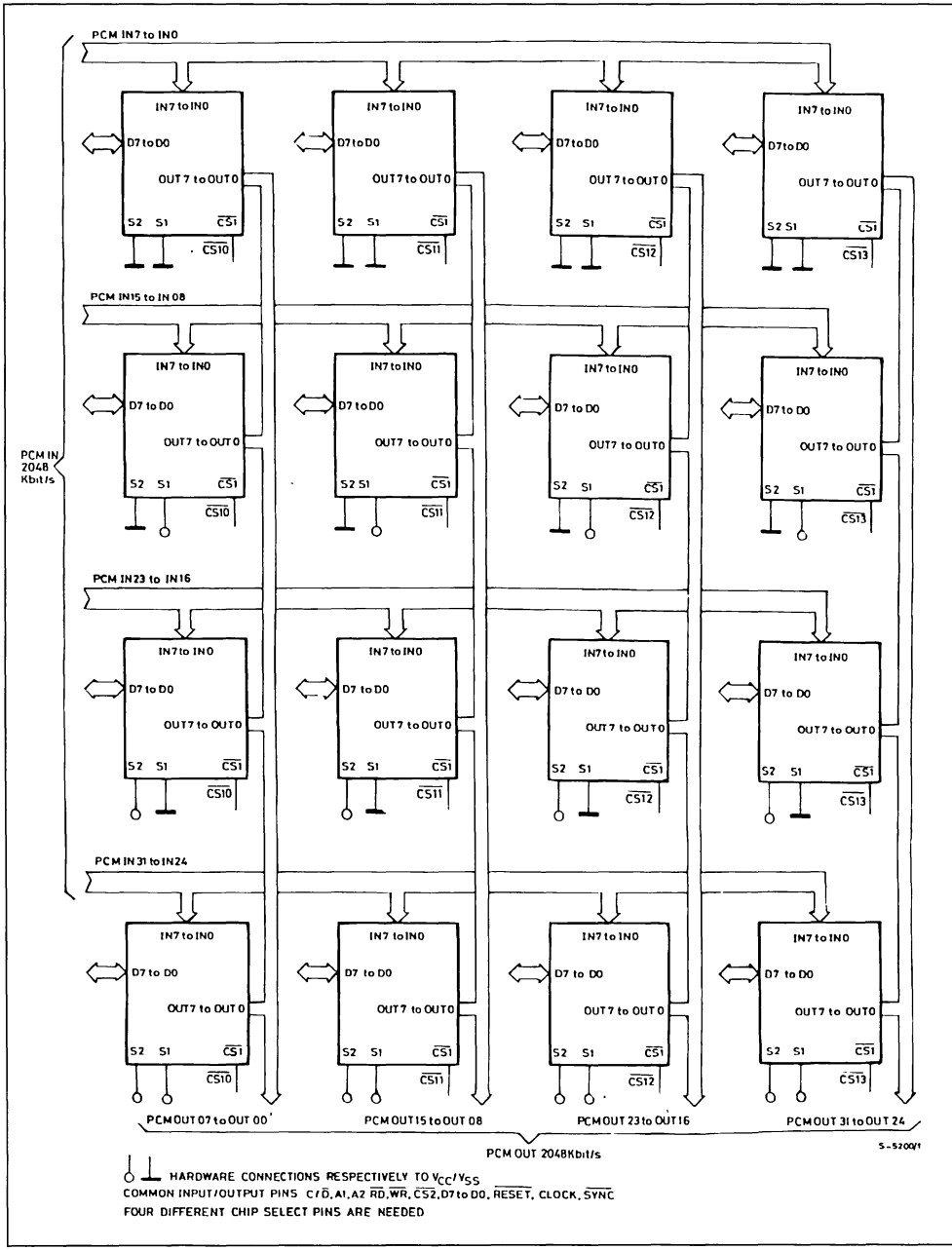
256 PCM links network (160 or 192 DSM) : the 32 x 32 link module shown on the next page.

2048 PCM links network (1792 or 2048 DSM) : the 256 x 256 link network is shown above.

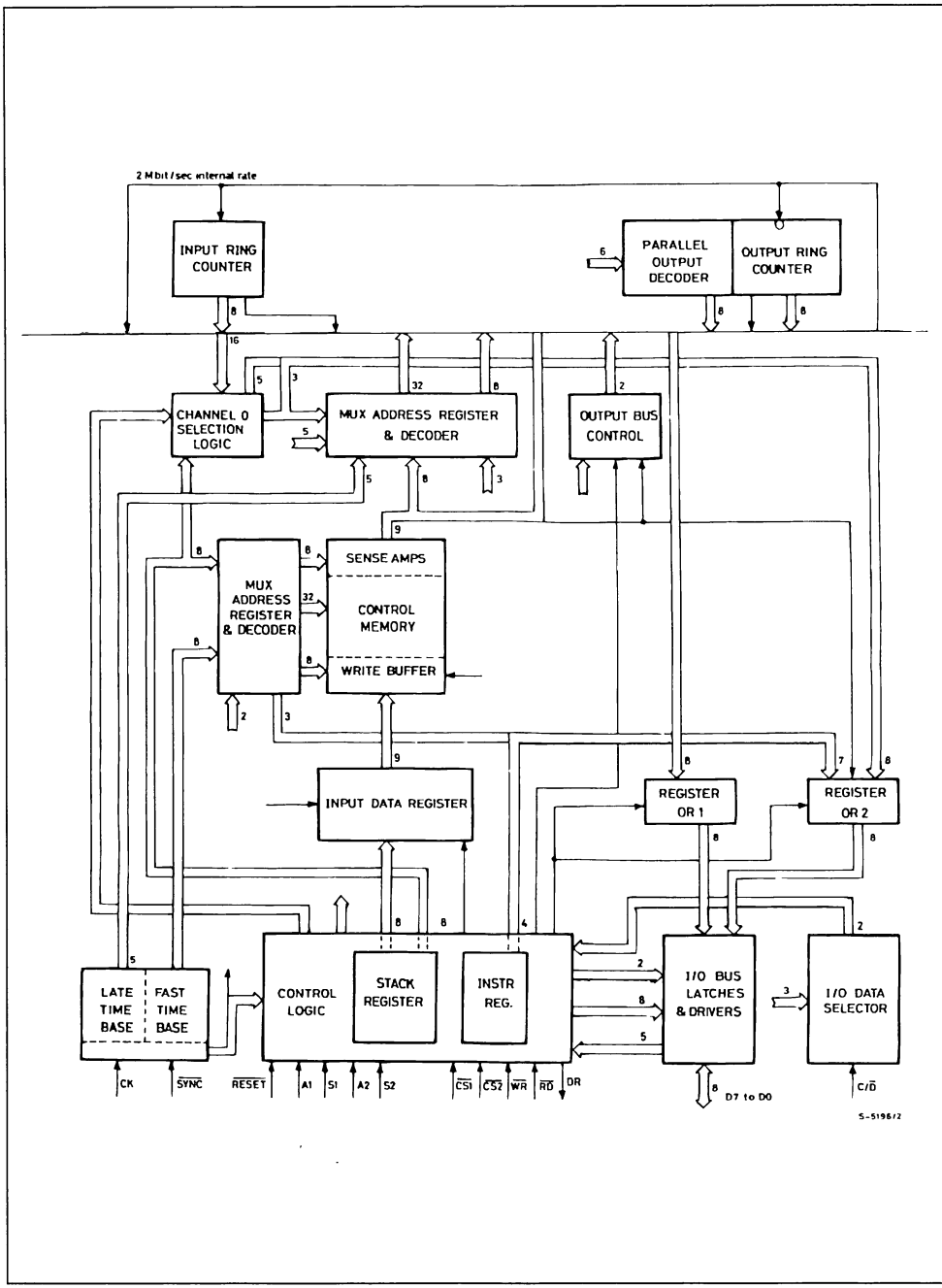


EXCHANGE NETWORKS APPLICATIONS (continued)

Single Stage/Sixteen Devices Configuration (32 by 32 links or 1024 channels).



BLOCK DIAGRAM



RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	4.75 to 5.25	V
V_I	Input Voltage	0 to 5.25	V
V_O	Off State Input Voltage	0 to 5.25	V
CLOCK Freq.	Input Clock Frequency	4.096	MHz
$\overline{\text{SYNC}}$ Freq.	Input Synchronization Frequency	8	KHz
T_{op}	Operating Temperature	0 to 70	°C

CAPACITANCES (measurement freq. = 1MHz ; T_{op} = 0 to 70°C ; unused pins tied to V_{SS})

Symbol	Parameter	Pins	Min.	Typ.	Max.	Unit
C_I	Input Capacitance	6 to 15 ; 26 to 30 ; 32 to 36			5	pf
$C_{I/O}$	I/O Capacitance	20 to 24			15	pf
C_O	Output Capacitance	1 to 4 ; 17 to 19 ; 25 ; 37 to 40			10	pf

D.C. ELECTRICAL CHARACTERISTICS (T_{amb} = 0 to 70°C, V_{CC} = 5V ± 5%)
All D.C. characteristics are valid 250µs after V_{CC} and clock have been applied.

Symbol	Parameter	Pins	Test Conditions	Min.	Typ.	Max.	Unit
V_{ILC}	Clock Input Low Level	6		– 0.3		0.8	V
V_{IHC}	Clock Input High Level	6		2.4		V_{CC}	V
V_{IL}	Input Low Level	7 to 15 20 to 24 26 to 30 32 to 36		– 0.3		0.8	V
V_{IH}	Input High Level	7 to 15 20 to 24 26 to 30 32 to 36		2.0		V_{CC}	V
V_{OL}	Output Low Level	17 to 25	I_{OL} = 1.8mA			0.4	V
V_{OH}	Output High Level	17 to 25	I_{OH} = 250µA	2.4			V
V_{OL}	PCM Output Low Level	1 to 4 37 to 40	I_{OL} = 2.0mA			0.4	V
I_{IL}	Input Leakage Current	6 to 15 26 to 30 32 to 36	V_{IN} = 0 to V_{CC}			10	µA
I_{DL}	Data Bus Leakage Current	17 to 24	V_{IN} = 0 to V_{CC} V_{CC} applied ; Pins 35 and 36 tied to V_{CC}, after Device Initialization			± 10	µA
I_{CC}	Supply Current	16	Clock Freq. = 4.096MHz			180	mA

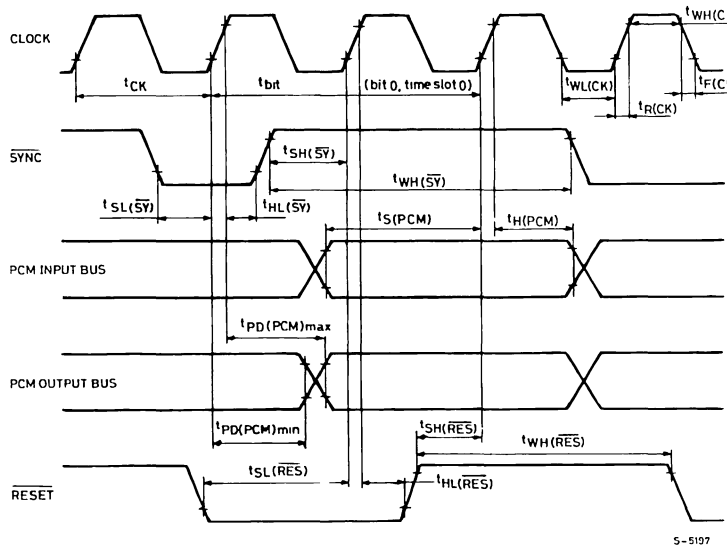
A.C. ELECTRICAL CHARACTERISTICS (T_{amb} = 0 to 70°C, V_{CC} = 5V ± 5%)
All A.C. characteristics are valid 250µs after V_{CC} and clock have been applied. C_L is the max. capacitive load and R_L the test pull up resistor.

Signal	Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
CK (clock)	t_{CK}	Clock Period		230			ns
	t_{WL}	Clock Low Level Width		100			ns
	t_{WH}	Clock High Level Width		100			ns
	t_R	Rise Time				25	ns
	t_F	Fall Time				25	ns
$\overline{SYNC}$	t_{SL}	Low Level Setup Time		80			ns
	t_{HL}	Low Level Hold Time		40			ns
	t_{SH}	High Level Setup Time		80			ns
	t_{WH}	High Level Width		t_{CK}			ns
PCM Input Busses	t_S	Setup Time		− 5			ns
	t_H	Hold Time		45			ns
PCM Output Busses	$t_{PD\ min}$	Propagation time referred to CK low level	C_L = 50pf, R_L = 2K	45			ns
	$t_{PD\ max}$	Propagation time referred to CK high level	C_L = 50pf, R_L = 2K			200	ns
$\overline{RESET}$	t_{SL}	Low Level Setup Time		100			ns
	t_{HL}	Low Level Hold Time		50			ns
	t_{SH}	High Level Setup Time		90			ns
	t_{WH}	High Level Width		t_{CK}			ns
$\overline{WR}$	t_{WL}	Low Level Width		150			ns
	t_{WH}	High Level Width		t_{CK}			ns
	t_{REP}	Repetition Interval between Active Pulses	$t_{REP} = 40 + 2\ t_{CK} + t_{WL(CK)} + t_{R(CK)}$	see formula			ns
	t_{SH}	High Level Setup Time to Active Read Strobe		0			ns
	t_{HH}	High Level Hold Time from Active Read Strobe		20			ns
	t_R	Rise Time				60	ns
	t_F	Fall Time				60	
$\overline{RD}$	t_{WL}	Low Level Width		180			ns
	t_{WH}	High Level Width		t_{CK}			ns
	t_{REP}	Repetition Interval between Active Pulses	$t_{REP} = 40 + 2\ t_{CK} + t_{WL(CK)} + t_{R(CK)}$	see formula			ns
	t_{SH}	High Level Setup Time to Active Read Strobe		0			ns
	t_{HH}	High Level Hold Time from Active Write Strobe		20			ns
	t_R	Rise Time				60	ns
	t_F	Fall Time				60	

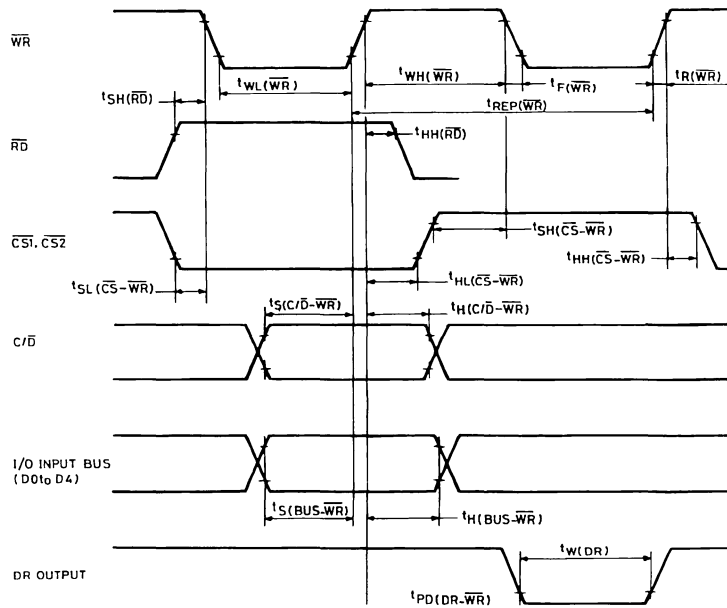
A.C. ELECTRICAL CHARACTERISTICS (continued)

Signal	Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$\overline{CS1}$, $\overline{CS2}$	$t_{SL(\overline{CS}\text{-}\overline{WR})}$	Low level setup time to $\overline{WR}$ falling edge	Active Case	0			ns
	$t_{HL(\overline{CS}\text{-}\overline{WR})}$	Low level hold time from $\overline{WR}$ rising edge	Active Case	0			ns
	$t_{SH(\overline{CS}\text{-}WR)}$	High level setup time to $\overline{WR}$ falling edge	Inactive Case	0			ns
	$t_{HH(\overline{CS}\text{-}WR)}$	High level hold time from $\overline{WR}$ rising edge	Inactive Case	0			ns
	$t_{SL(\overline{CS}\text{-}RD)}$	Low level setup time to $\overline{RD}$ falling edge	Active Case	0			ns
	$t_{HL(\overline{CS}\text{-}RD)}$	Low level hold time from $\overline{RD}$ rising edge	Active Case	0			ns
	$t_{SH(\overline{CS}\text{-}RD)}$	High level setup time $\overline{RD}$ falling edge	Inactive Case	0			ns
	$t_{HH(\overline{CS}\text{-}RD)}$	High level hold time from $\overline{RD}$ rising edge	Inactive Case	0			ns
C/$\overline{D}$	$t_{S(C/\overline{D}\text{-}WR)}$	Setup time to write strobe end		130			ns
	$t_{H(C/\overline{D}\text{-}WR)}$	Hold time from write strobe end		25			ns
	$t_{S(C/\overline{D}\text{-}RD)}$	Setup time to read strobe start		20			ns
	$t_{H(C/\overline{D}\text{-}RD)}$	Hold time from read strobe end		25			ns
A1, S1, A2, S2 (match inputs)	t_S(match-$\overline{WR}$)	Setup time to write strobe end		130			ns
	t_H(match-$\overline{WR}$)	Hold time from strobe end		25			ns
	t_S(match-$\overline{RD}$)	Setup time to read strobe start		20			ns
	t_H(match-$\overline{RD}$)	Hold time from read strobe end		25			ns
DR (data ready)	t_W	Low state width	Instructions 5 and 6			2.t_{CK}	ns
	t_{PD}	DR output delay from write strobe end (active command)	Instruction 5, C_L = 50pf	5.t_{CK}		14.t_{CK}	ns
D0 to D7 (interface bus)	$t_{S(\overline{BUS}\text{-}WR)}$	Input setup time to write strobe end		130			ns
	$t_{H(\overline{BUS}\text{-}WR)}$	Input hold time from write strobe end		25			ns
	$t_{PD(BUS)}$	Propagation time from (active) falling Edge of read strobe	C_L = 200pF			120	ns
	$t_{HZ(BUS)}$	Propagation time from (active) rising Edge of read strobe to high impedance state				80	ns

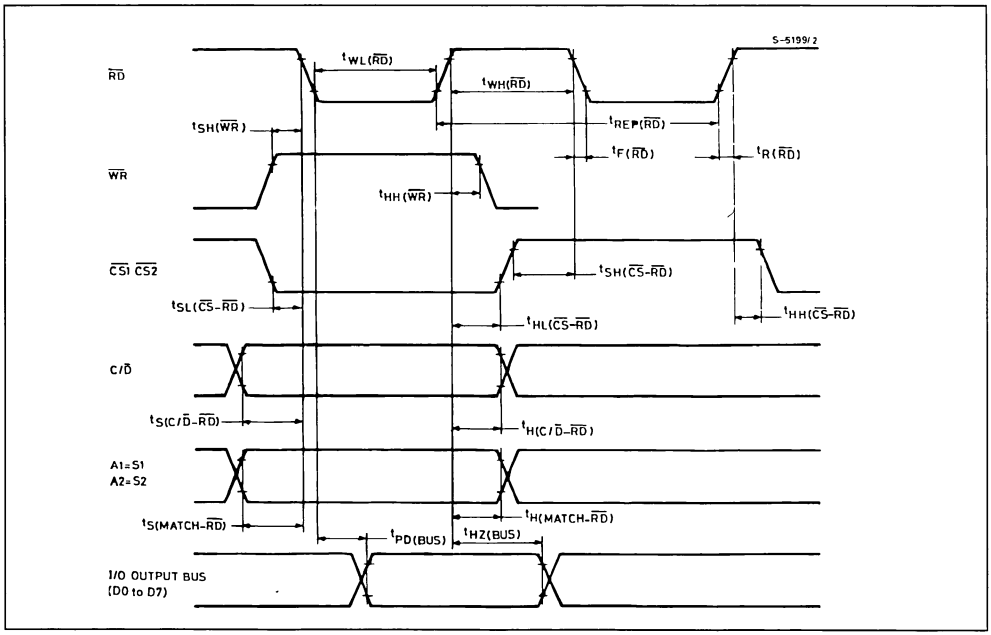
PCM TIMING, $\overline{RESET}$



WRITE OPERATION TIMING



READ OPERATION TIMING



GENERAL DESCRIPTION

The M088 is intended for large telephone switching systems, mainly central exchanges, digital line concentrators and private branch exchanges where a distributed microcomputer control approach is extensively used. It consists of a speech memory (SM), a control memory (CM), a serial/parallel and a parallel/serial converter, an internal parallel bus, an interface (8 data lines, 11 control signals) and dedicated control logic. By means of repeated clock division two timebases are generated. These are preset from an external synchronization signal to two specific count numbers so that sequential scanning of the bases give synchronous addresses to the memories and I/O channel controls. Different preset count numbers are needed because of processing delays and data path direction. The timebase for the input channels is delayed and the timebase for output channels is advanced with respect to the actual time. Each serial PCM input channel is converted to parallel data and stored in the speech memory at the beginning of any new time slot (according to first timebase) in the location determined by input pin number and time slot number. The control memory CM maintains the correspondences between input and output channels. More exactly, for any output pin/output channel combination the control memory gives either the full address of the speech memory location involved in the PCM transfer or an 8-bit word to be supplied to the parallel/serial output converter. A 9th bit at each CM location defines the data source for output links, low for SM, high for CM.

The late timebase is used to scan the output channels and to determine the pins to be serviced within each channel ; enough idle cycles are left to the microprocessor for asynchronous instruction processing. Two 8-bit registers OR1 and OR2 supply feedback data for control or diagnostic purposes ; OR1 comes from internal bus i.e. from memories, OR2 gives an opcode copy and additional data to the microcomputer. A four byte-five bit stack register and an instruction register, under microcomputer control, store input data available at the interface.

Dedicated logic, under control of the microprocessor interface, extracts the 0 channel content of any selected PCM input bus, using spare cycles of SM.

PIN DESCRIPTION

D7 to D0 (pins 17 to 24)

Data bus pins. The bidirectional bus is used to transfer data and instructions to/from the microprocessor. D0 is the least significant digit. The output bus is 8 bits wide ; input is only 5 bits wide.

The bus is tristate and cannot be used while $\overline{\text{RESET}}$ is held low.

The meaning of input data, such as bus or channel numbers, and of expected output data is specified in detail by the instruction description.

C/$\overline{\text{D}}$ (pin 30)

Input control pin, select pin. In a write operation C/$\overline{\text{D}}$ = 0 qualifies any bus content as data, while C/$\overline{\text{D}}$ = 1 qualifies it as an opcode. In a read operation OR1 is selected by C/$\overline{\text{D}}$ = 0, OR2 by C/$\overline{\text{D}}$ = 1.

A1, S1, A2, S2 (pins 26 to 29)

Address select or match pins. In a multi-chip configuration (e.g. a single stage matrix expansion), using the same $\overline{\text{CS}}$ pins, the match condition (A1 = S1 and A2 = S2) leaves the command instruction as defined ; on the contrary the mismatch condition modifies the execution as follows : instructions 1 and 3 are reversed to channel disconnection, instruction 5 is unaffected, instructions 2-4-6 are cancelled (not executed).

Bus reading takes place only on match condition, instruction flow is in any case affected.

Each pins couple is commutative : in a multichip configuration pins S1 and S2 give a hard-wired address selection for individual matrixes, while in single configuration S1 and A1 or S2 and A2 are normally tied together.

$\overline{\text{CS1}}$, $\overline{\text{CS2}}$ (pins 33, 34)

Commutative chip select pins. They enable the device to perform valid read/write operations (active low). Two pins allow row/column selection with different types of microprocessors ; normally one is tied to ground.

$\overline{\text{WR}}$ (pin 35)

Pin $\overline{\text{WR}}$, when $\overline{\text{CS1}}$ and $\overline{\text{CS2}}$ are low, enables data transfer from microprocessor to the device. Data or opcode and controls are latched on $\overline{\text{WR}}$ rising edge. Because of internal clock resynchronization one single additional requirement is recommended in order to produce a simultaneous instruction execution in a multichip configuration : $\overline{\text{WR}}$ rising edge has to be 20 to 20 + $t_{WL(CK)}$ nsec late relative to clock falling edge.

$\overline{\text{RD}}$ (pin 36)

When CS1 and CS2 are low and match condition exists, a low level on RD enables a register OR1 or OR2 read operation, through the bidirectional bus.

In addition, the rising edge of $\overline{\text{RD}}$ latches C/$\overline{\text{D}}$ and the match condition pins in order to direct the internal flow of operations. Because of internal clock resynchronization, one single additional requirement is recommended in order to produce a simultaneous instruction flow in a multichip configuration : the $\overline{\text{RD}}$ rising edge has to be 20 to 20 + $t_{WL(CK)}$ nsec late relative to clock falling edge.

DR (pin 25)

Data ready. Normally high, DR output pin goes low to tell the microprocessor that :

a) the instruction code was found to be invalid ;

b) executing instruction 5 an active output channel was found in the whole matrix array, that is a CM word not all "ones" was found in a configuration of devices sharing the same CS pins ;

c) executing instruction 6 "0 channel extraction" took place and OR2 was loaded with total number of messages inserted on 0 time slot.

DR is active about two clock cycles in case **b** and **c** ; in case a it is left low until a valid instruction code is supplied.

$\overline{\text{RESET}}$ (pin 32)

$\overline{\text{RESET}}$ control pin is normally used at the very beginning to initialize the device or the network. Any logical status is reset and CM is set to all "ones" after $\overline{\text{RESET}}$ going low.

The internal initialization routine takes one time frame whatever the $\overline{\text{RESET}}$ width on low level (minimum one cycle roughly), but it is repeated an integer number of time frames as long as $\overline{\text{RESET}}$ is found low during 0 time slot.

Initialization pulls the interface bus immediately to a high impedance state. After the CM has been set to all "ones" the PCM output channels are also set to high impedance state (that is pulled to "ones").

CLOCK (pin 6)

Input master clock. Typical frequency is 4.096MHz. First division gives an internal clock controlling the input and output channels bit rate.

$\overline{\text{SYNC}}$ (pin 7)

Input synchronization signal is active low. Typical frequency is 8kHz.

Internal time bases are forced by synchronism to an assigned count number in order to restore channels and bit sequential addressing to a known state. Count difference between the bases is 32, corresponding to two time slots, that is the minimum PCM propagation time, or latency time.

INP PCM 7 to INP PCM 0 (pins 8 to 15)

PCM input busses or pins ; they accept a standard 2Mbit/s rate. Bit 1 (sign bit) is the first of the serial sequence ; in a parallel conversion it is left adjusted as the most significant digit.

OUT PCM 7 to OUT PCM 0 (pins 37 to 40 and 1 to 4)

PCM output busses or pins ; bit rate and organization are the same as input pins.

Output buffers are open drain type in order to simplify wired-or connections and minimize current spike problems in multichip configuration systems.

The device drives the output channels theoretically one bit time before input channels are needed by specifications : this feature allows inputs and outputs to be tied together cancelling any analog delay of digital outputs up to

$t_{DEL\ max} = t_{bit} - t_{\overline{PD(PCM)max}} + t_{\underline{PD(PCM)min}}$

BIAS (pin 5)

Internally generated bias voltage (- 2.5 to - 3.0V for V_{CC} in the operating range). A max. 220pf capacitor connected to pin 5 provides improved filtering.

MIXED $\overline{RD}$ & $\overline{WR}$ OPERATIONS

In principle $\overline{RD}$ and $\overline{WR}$ operations are allowed in any order within specification constraints.

In practive, only one control pin is low at any given time when CS1 and CS2 are enabled.

If by mistake or hardware failure both $\overline{RD}$ and $\overline{WR}$ pins are low, the interface bus is internally pushed to tristate condition as long as WR is held low and input registers are protected.

Registers OR1 and OR2 can be read in any order with a single $\overline{RD}$ strobe using C/$\overline{D}$ as multiplexing control ; never the less this procedure is not recommended because the device is directed for instruction flow only according to data latched by $\overline{RD}$ rising edge.

Multiple $\overline{RD}$ operations of the same kind are allowed without affecting the instruction flow : only "new" OR1 or OR2 read operations step the flow.

Input and output registers are held for sure in the previous state for the first 3 cycles following an opcode or an OR2 read.

FUNCTIONAL DESCRIPTION OF SPECIFIC MICROPROCESSOR OPERATIONS

The device, under microprocessor control, performs the following instructions :

1 CHANNEL CONNECTION/DISCONNECTION

2 CHANNEL DISCONNECTION

3 INSERTION OF A BYTE ON A PCM OUTPUT CHANNEL/CHANNEL DISCONNECTION)

4 TRANSFER OF A SINGLE PCM OUTPUT CHANNEL SAMPLE

5 TRANSFER OF A SINGLE OUTPUT CHANNEL CONTROL WORD

6 TRANSFER OF A SELECTED 0 CHANNEL PCM INPUT DATA ACCORDING TO AN 8-BIT MASK PREVIOUSLY STORED IN THE "EXPECTED MESSAGES" REGISTER

The instruction flow is as follows.

Any input protocol is started by the microprocessor interface loading the internal stack register with 2 bytes (4 bytes for instructions 1 and 3) qualified as data bytes by C/$\overline{D}$ = 0 and a specific opcode qualified by C/$\overline{D}$ = 1 (match condition is normally needed).

After the code is loaded in the instruction register it is immediately checked to see whether it is acceptable and if not it is rejected. If accepted the instruction is also processed as regards match condition and is appended for execution during the memories' space cycles.

Four cases are possible :

a) the code is not valid ; execution cannot take place, the DR output pin is reset to indicate the error ; all registers are saved ;

b) the code is valid for types 2, 4 and 6 but it is unmatched ; execution cannot take place, DR is not affected.

c) the code is valid for types 1 and 3 and it is unmatched ; the instruction is interpreted as a channel disconnection.

d) the code is valid and is either matched or of type 5 ; the instruction is processed as received.

Validation control takes only two cycles out of a total execution time of 5 to 13 cycles ; the last operation is updating of the content of registers OR1 and OR2.

During a very long internal operation (device initialization after RESET going high or execution of instruction 6) a new set of data bytes with a valid opcode is accepted while a wrong code is rejected. At the end of the current routine execution takes place in the same way as described before.

At the end of an instruction it is normally recommended to read one or both registers. To enable instruction 6, however, it is necessary to read register OR2. This is because instruction 6, used between other short instructions of type 1 to 5, must have a lower priority and can be enabled only after the short instructions have been completed. Instruction 6 normally has a long process and a special flow which is described below.

First a not-all-zero mask is stored in the "expected messages" register and in another "background" register. This operation starts the second phase of instruction 6 which is called "channel 0 extraction" and is repeated at the beginning of any new time frame. At the beginning of the time frame a new copy of activated channels to be extracted is made from the "background register" and put in the "expected messages" register. In addition the latter register is modified to indicate the exact number of messages that have arrived. The term messages covers any input 0 channel data with starting sequence different from the label 01. So using this label the number of expected messages can be reduced to correspond to the number of effective messages. If and only if the residual number is different from zero will the device start the extraction protocol at the end of the current routine.

The procedure is as follows : the DR output is pulsed low as a two cycle interrupt request and OR2 is loaded with the total number of active channels to be extracted.

The transfer of OR2 content to the microprocessor continues the extraction which consists of repeated steps of OR1 and OR2 loading, indicating respectively the message and the incoming bus number. Reading the registers in the order OR1, OR2 must be continued until completion or until the time frame runs out.

With a new time frame a new extraction process begins, resuming the copy operation from the background register.

During extraction the active channels are scanned from the highest to the lowest number (from 7 to 0). While extraction is being carried out the time interval requirements between active rising edges of RD are minimum 5 to 13 t_{CK} for sequence OR2 - OR1 and minimum 3 times t_{CK} for sequence OR1 - OR2. More details are given in the following tables.

INSTRUCTION TABLES

The most significant digits of OR2 A7, A6, A5 are a copy of the PCM selected output bus ; the least significant digits of OR2 are the opcode, C8 is the control bit. In any case parentheses () define actual register content.

INSTRUCTION 1 : CHANNEL CONNECTION/DISCONNECTION

Control Signals					Data Bus								Notes
Match	C/D	CS	WR	RD	D7	D6	D5	D4	D3	D2	D1	D0	
X	0	0	0	1	X	X	X	X	X	Bi2	Bi1	Bi0	1 st Data Byte : selected input bus.
X	0	0	0	1	X	X	X	Ci4	Ci3	Ci2	Ci1	Ci0	2 nd Data Byte : selected input channel.
X	0	0	0	1	X	X	X	X	X	Bo2	Bo1	Bo0	3 rd Data Byte : selected output bus.
X	0	0	0	1	X	X	X	Co4	Co3	Co2	Co1	Co0	4 th Data Byte : selected output channel.
Yes/no	1	0	0	1	X	X	X	X	0	0	0	1	Instruction Opcode
Yes	0	0	1	0	C7 (1 (Bi2	C6 1 Bi1	C5 1 Bi0	C4 1 Ci4	C3 1 Ci3	C2 1 Ci2	C1 1 Ci1	C0 1) Ci0)	OR1 : CM content copy, that is for mismatch condition for match condition.
Yes	1	0	1	0	A7 (Bo2 (Bo2	A6 Bo1 Bo1	A5 Bo0 Bo0	C8 1 0	0 0 0	0 0 0	0 0 0	1 1) 1)	OR2 : that is for mismatch condition, for match condition.

INSTRUCTION 2 : OUTPUT CHANNEL DISCONNECTION

Control Signals					Data Bus								Notes
Match	C/D	CS	WR	RD	D7	D6	D5	D4	D3	D2	D1	D0	
X	0	0	0	1	X	X	X	X	X	Bo2	Bo1	Bo0	1 st Data Byte : selected output bus.
X	0	0	0	1	X	X	X	Co4	Co3	Co2	Co1	Co0	2 nd Data Byte : selected output channel.
Yes	1	0	0	1	X	X	X	X	0	0	1	0	Instruction Opcode
Yes	0	0	1	0	1	1	1	1	1	1	1	1	OR1 : CM Content Copy (output channel is inactive)
Yes	1	0	1	0	A7 (Bo2	A6 Bo1	A5 Bo0	1 1	0 0	0 0	1 1	0 0)	OR2 : that is

INSTRUCTION 3 : LOADING A MICROPROCESSOR BYTE

Control Signals					Data Bus								Notes
Match	C/D	CS	WR	RD	D7	D6	D5	D4	D3	D2	D1	D0	
X	0	0	0	1	X	X	X	X	X	Ci7	Ci6	Ci5	1 st Data Byte : most significant digits to be inserted.
X	0	0	0	1	X	X	X	Ci4	Ci3	Ci2	Ci1	Ci0	2 nd Data Byte : least significant digits to be inserted.
X	0	0	0	1	X	X	X	X	X	Bo2	Bo0	Bo1	3 rd Data Byte : selected output bus.
X	0	0	0	1	X	X	X	Co4	Co3	Co2	Co1	Co0	4 th Data Byte : selected output channel.
Yes/no	1	0	0	1	X	X	X	X	0	1	0	0	Instruction Opcode
Yes	0	0	1	0	C7 (1 (Ci7	C6 1 Ci6	C5 1 Ci5	C4 1 Ci4	C3 1 Ci3	C2 1 Ci2	C1 1 Ci1	C0 1) Ci0)	OR1 : CM content copy, that is for mis match condition for match condition.
Yes	1	0	1	0	A7 (Bo2	A6 Bo1	A5 Bo0	1 1	0 0	1 1	0 0	0 0)	OR2 : that is.

INSTRUCTION 4 : TRANSFER OF A SINGLE PCM SAMPLE

Control Signals					Data Bus								Notes
Match	C/D	CS	WR	RD	D7	D6	D5	D4	D3	D2	D1	D0	
X	0	0	0	1	X	X	X	X	X	Bo2	Bo1	Bo0	1 st Data Byte : selected output bus.
X	0	0	0	1	X	X	X	Co4	Co3	Co2	Co1	Co0	2 nd Data Byte : selected output channel.
Yes	1	0	0	1	X	X	X	X	1	0	1	1	Instruction Opcode
Yes	0	0	1	0	C7 S7	C6 S6	C5 S5	C4 S4	C3 S3	C2 S2	C1 S1	C0 S0	OR1 : CM Content Copy if C8 = 1 ; or SM Content Sample if C8 = 0
Yes	1	0	1	0	A7 (Bo2	A6 Bo1	A5 Bo0	C8 C8	1 1	0 0	1 1	1 1)	OR2 : that is.

Notes : S7 S0 is a parrallel copy of a PCM data, S7 is the most significant digit and the first of the sequence.

INSTRUCTION 5 : TRANSFER OF AN OUTPUT CHANNEL CONTROL WORD

Control Signals					Data Bus								Notes
Match	C/D	CS	WR	RD	D7	D6	D5	D4	D3	D2	D1	D0	
X	0	0	0	1	X	X	X	X	X	Bo2	Bo1	Bo0	1 st Data Byte : selected output bus.
X	0	0	0	1	X	X	X	Co4	Co3	Co2	Co1	Co0	2 nd Data Byte : selected output channel.
X	1	0	0	1	X	X	X	X	1	0	0	0	Instruction Opcode
Yes	0	0	1	0	C7	C6	C5	C4	C3	C2	C1	C0	OR1 : CM selected CM word copy.
Yes	1	0	1	0	A7 (Bo2	A6 Bo1	A5 Bo0	C8 C8	1 1	0 0	0 0	0 0)	OR2 : that is.

INSTRUCTION 6 : CHANNEL 0 SELECTION MASK STORE/DATA TRANSFER

Control Signals					Data Bus								Notes
Match	C/D	CS	WR	RD	D7	D6	D5	D4	D3	D2	D1	D0	
X	0	0	0	1	X	X	X	X	X	Mi7	Mi6	Mi5	1 st Data Byte : most sign. digits of selection mask.
X	0	0	0	1	X	X	X	Mi4	Mi3	Mi2	Mi1	Mi0	2 nd Data Byte : most sign. digits of selection mask.
Yes	1	0	0	1	X	X	X	X	1	1	1	0	Instruction Opcode
Mask store control													
Yes	0	0	1	0	(previous content)								OR1 : register is not affected.
Yes	1	0	1	0	N2	N1	N0	Tn	1	1	1	0	OR2 : see below.
First Data Transfer (after DR going low)													
Yes	0	0	1	0	(previous content)								OR1 : register is not affected.
Yes	1	0	1	0	N2	N1	N0	Tn	1	1	1	0	OR2 : see below.
Repeated Data Transfer (after first OR2 transfer)													
Yes	0	0	1	0	S7	S6	S5	S4	S3	S2	S1	S 0	OR1 : expected message stored in SM.
Yes	1	0	1	0	P2	P1	P0	Fn	1	1	1	0	OR2 : see below.

Notes :
1. About mask bits Mi0 to Mi7 a logic "0" level means disabling condition, a logic "1" level means enabling condition.
2. A null mask or a RESET pulse clear the mask and the deep background mask registers and disable channel 0 extraction function.
3. Reading of OR2 is optional after mask store or redefinition, because function is activated only by not-null mask writing.
4. After mask store (N2 N1 N0) is the sum of activated channels, after DR is the sum of active channels ; Tn = 1/0 means activation/suppression of the function after store while after DR only Tn = 1 can appear to tell a not-null configuration to be extracted.
5. Reading of OR2 is imperative after DR in order to step the data transfer ; reading of OR1 is also needed to scan in descending order the priority register. Relevant messages only are considered, that means only messages with a MSD label different from 0 1.
6. (P2 P1 P0) is the PCM bus on which the message copied in OR1 was found ; Fn is a continuation bit telling respectively on level 1/0 for any more/no more extraction to be performed

SGS-THOMSON MICROELECTRONICS

M3444

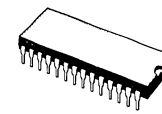
CMOS 128 X 128 DIGITAL SWITCHING MATRIX

ADVANCE DATA

- HARDWARE (pin-to-pin) AND SOFTWARE COMPATIBLE WITH M044
- 128 INPUT AND 128 OUTPUT CHANNEL DIGITAL SWITCHING MATRIX (non blocking)
- TYPICAL APPLICATION IN PABX
- EUROPEAN AND U.S. STANDARD COMPATIBLE (32/24 serial channels per frame)
- PCM INPUTS AND OUTPUTS MATUALLY COMPATIBLE
- ACTUAL INPUT-OUTPUT CHANNEL CONNECTIONS STORED AND MODIFIED VIA AN ON-CHIP 8-BIT PARALLEL MICROPROCESSOR INTERFACE
- 5 MAIN "FUNCTIONS" OR "INSTRUCTIONS" AVAILABLE
- TYPICAL BIT RATE : 2Mbit/s (lower allowed)
- TYPICAL SYNCHRONIZATION RATE : 8KHz (time frame is 125µs)
- 5 VOLT POWER SUPPLY WITH INTERNALLY GENERATED BIAS VOLTAGE
- TYPICAL CURRENT CONSUMPTION IS 22mA
- MOS & TTL INPUT/OUTPUT LEVELS COMPATIBLE
- DIFFUSED WITH HIGH DENSITY ADVANCED 1.2µs CMOS PROCESS HCMOS3

Main instruction controlled by the microprocessor interface

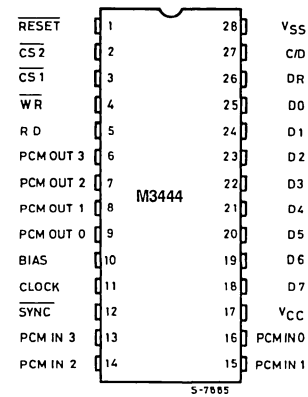
- CHANNEL CONNECTION/DISCONNECTION
- CHANNEL DISCONNECTION
- INSERTION OF A BYTE ON A PCM OUTPUT CHANNEL
- TRANSFER TO THE MICROPROCESSOR OF A SINGLE PCM OUTPUT CHANNEL SAMPLE
- TRANSFER TO THE MICROPROCESSOR OF A SINGLE OUTPUT CONTROL WORD



DIP28
(Ceramic)

ORDER CODE : M3444F1

PIN CONNECTION



SGS-THOMSON MICROELECTRONICS

M3488

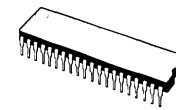
CMOS 256 X 256 DIGITAL SWITCHING MATRIX

ADVANCE DATA

- HARDWARE (pin-to-pin) AND SOFTWARE COMPATIBLE WITH M088
- 256 INPUT AND 256 OUTPUT CHANNEL DIGITAL SWITCHING MATRIX
- BUILDING BLOCK DESIGNED FOR LARGE CAPACITY ELECTRONIC EXCHANGES, SUBSYSTEMS AND PABX
- NO EXTRA PIN NEEDED FOR NOT-BLOCKING SINGLE STAGE AND HIGH CAPACITY SYNTHESIS BLOCKS (512 or 1024 channels)
- EUROPEAN AND U.S. STANDARD COMPATIBLE (32/24 serial channels per frame)
- PCM INPUTS AND OUTPUTS MUTUALLY COMPATIBLE
- ACTUAL INPUT-OUTPUT CHANNEL CONNECTIONS STORED AND MODIFIED VIA AN ON CHIP 8-BIT PARALLEL MICROPROCESSOR INTERFACE
- 6 MAIN "FUNCTIONS" OR "INSTRUCTIONS" AVAILABLE
- TYPICAL BIT RATE : 2Mbit/s
- TYPICAL SYNCHRONIZATION RATE : 8KHz (time frame is 125µs)
- 5V POWER SUPPLY WITH INTERNALLY GENERATED BIAS VOLTAGE
- TYPICAL CURRENT CONSUMPTION IS 22mA
- MOS & TTL INPUT/OUTPUT LEVELS COMPATIBLE
- DIFFUSED WITH HIGH DENSITY ADVANCED 1.2 µm CMOS PROCESS HCMOS3

Main instructions controlled by the microprocessor interface

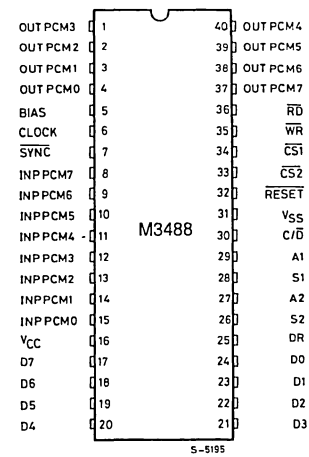
- CHANNEL CONNECTION/DISCONNECTION
- CHANNEL DISCONNECTION
- INSERTION OF A BYTE ON A PCM OUTPUT CHANNEL
- TRANSFER TO THE MICROPROCESSOR OF A SINGLE PCM OUTPUT CHANNEL SAMPLE
- TRANSFER TO THE MICROPROCESSOR OF A SINGLE OUTPUT CHANNEL CONTROL WORD
- TRANSFER TO THE MICROPROCESSOR OF A SELECTED 0 CHANNEL PCM INPUT DATA



DIP40
(Ceramic)

ORDER CODE : M3488F1

PIN CONNECTION (top view)



CEPT PCM TRUNK CONTROLLER

DESCRIPTION

The basic function of the CEPT PCM trunk controller is to synchronize a PCM interface with the local exchange clock. The EF7333 is provided as part of a kit also containing the EF73321 PCM line transceiver. In addition to its basic function, the device also features :

INCOMING LINK PROCESSING FUNCTIONS

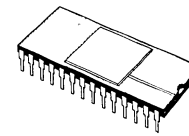
- INPUT SIGNAL HDB3, BINARY OR BIPOLAR DECODING
- FRAME SYNCHRONIZATION WITH LOCAL CLOCK
- LINE JITTER ABSORPTION
- FRAME SKIP/DOUBLING
- RECEIVE ERROR DETECTION AND ALARM GENERATION
- REMOTE ALARM EXTRACTION

OUTGOING LINK PROCESSING FUNCTIONS

- INSERTION OF SYNCHRONIZATION DATA INTO OUTGOING FRAMES
- OUTPUT SIGNAL BINARY, HDB3 OR BIPOLAR CODING
- RECEIVE FAULT ALARM TRANSMISSION

OTHER CHARACTERISTICS

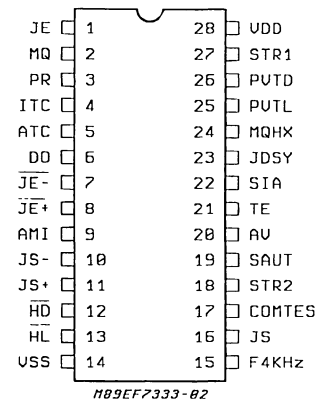
- NMOS TECHNOLOGY
- 5 V SUPPLY
- LOW POWER CONSUMPTION (200 mW)
- CONFORMS TO CCITT RECOMMENDATION G.737
- OPERATES IN STAND-ALONE MODE OR WITH MARKER INTERFACE



DIP28
(Ceramic)

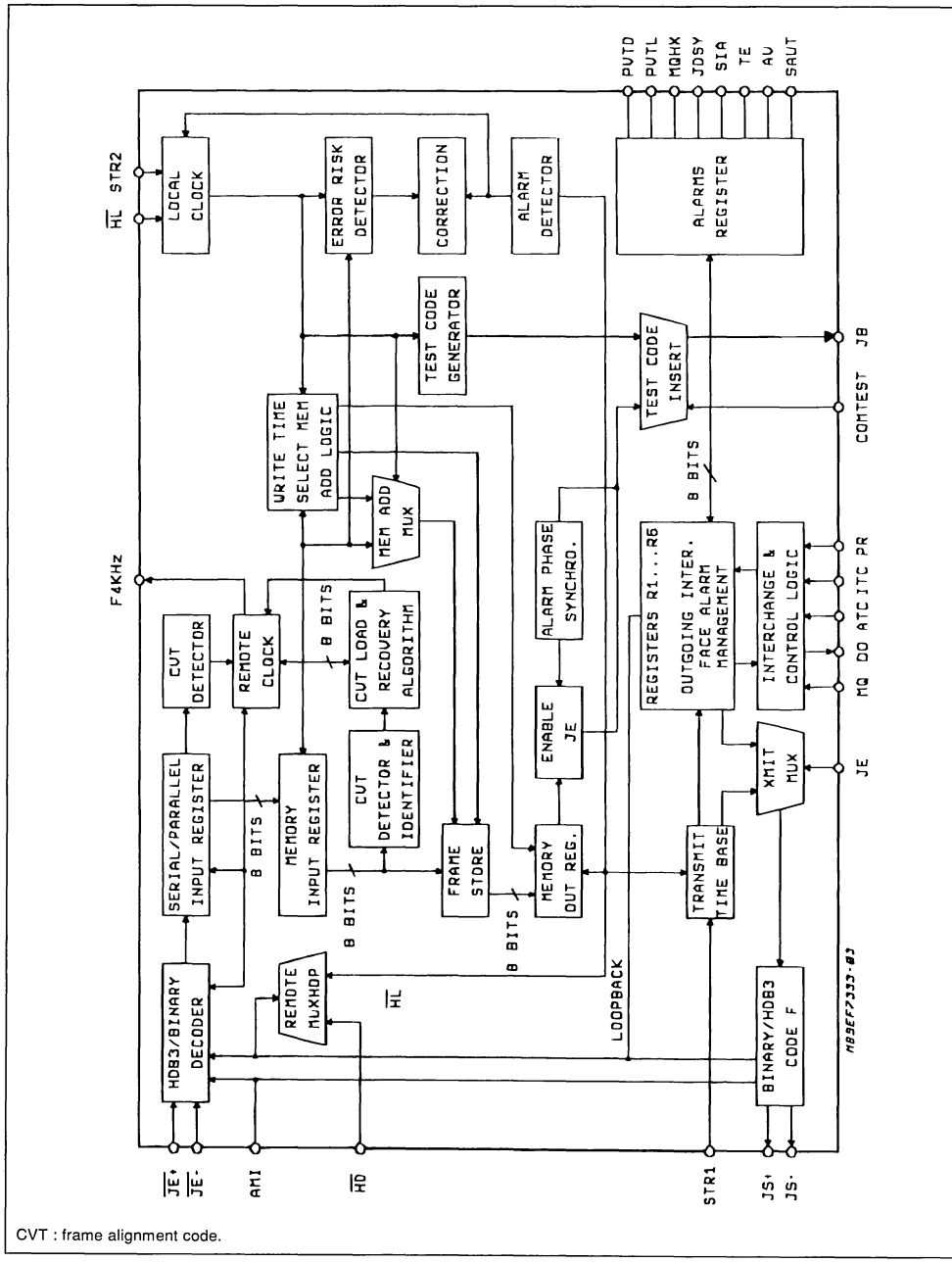
ORDER CODE : EF7333

PIN CONNECTION



M89EF7333-02

BLOCK DIAGAM



CVT : frame alignment code.

PIN DESCRIPTION

POWER SUPPLY

Name	Pin Type	N°	Function	Description
V_{SS}	Power	14	Ground	Ground
V_{DD}	Power	28	Power Supply	+ 5 V ± 5 %

CLOCKS

Name	Pin Type	N°	Function	Description
$\overline{HD}$	I	12	Distant Clock	Remote clock synchronizing incoming data at $\overline{JE}^+$, $\overline{JE}^-$, frequency 2048 kHz (jitter-free)
$\overline{HL}$	I	13	Local Clock	Local clock synchronizing outgoing data at JS, JS^+, JS^-, frequency 2048 kHz

RECEIVE

Name	Pin Type	N°	Function	Description
STR2	I	18	Synchronization Frame Signal	Local Clock Synchronization Signal Frequency 4 kHz
$\overline{JE}^+$ $\overline{JE}^-$	I I	8 7	Input Trunk	Data from remote interface at frequency of $\overline{HD}$, normally in HDB3 code
JS	O	16	Binary Data Output	Binary data from remote interface, restored to frequency of $\overline{HL}$
JDSY	O	23	Alarm	Loss of interface synchronization alarm : three consecutive frame alignment codes or three consecutive identifier absent.
TE	O	21	Alarm	Error rate alarm, as measured on incoming interface as per CCITT Recommendation G.737
PVTD	O	26	Alarm	Loss of frame alignment at remote end alarm : bit 3 in timeslot TSO of odd frames received from remote interface set to 1
PVTL	O	25	Alarm	Loss of frame alignment alarm : no frame alignment code in timeslot TSO of even frames from incoming interface
SIA	O	22	Alarm	Alarm Indication Signal : more than 75 % bits at 1 in messages received from remote end
MQHX	O	24	Alarm	Remote Clock $\overline{HD}$ Missing
SAUT	O	19	Alarm	Changes of State for Each Frame Skip or doubling Operation
AV	O	20	Alarm	"1" : Frame Skip $\overline{HD}$ Faster than $\overline{HL}$ "0" : Frame Doubling $\overline{HD}$ Slower than $\overline{HL}$
F4kHz	O	15	Remote Clock	Remote Clock Output, Frequency 4 kHz

TRANSMIT

Name	Pin Type	N°	Function	Description
STR1	I	27	Synchronization Frame Signal	Frame Synchronization Signal from Transmit Clock, Frequency 4 kHz
JE	I	1	Binary Data Input	Binary Data from Local Exchange Synchronized by HL
JS^+ JS^-	O O	11 10	Output Trunk	Transcoding of data received on input JE, synchronization by HL

CONTROL

Name	Pin Type	N°	Function	Description
AMI	I	9	Mode Select	Selects Transmit/receive Information Coding/decoding Mode
COMTEST	I	17	Test Command	Commands test providing for insertion of a code at the outgoing interface in order to test the network : 10101100 in Even Frame Timeslots 01010011 in Odd Frame Timeslots
PR	I	3	Validation Signal	Signal Validating ATC, ITC, DO
ATC	I	5	Address Register Input	Internal Register Addressing Input (R1...R6)
ITC	I	4	Register Content Input	Data Input for Internal Register Addressed by ATC
DO	O	6	Register Content Output	Data Output for Internal Register Addressed by ATC (in high impedance state when PR = 0)
MQ	I	2	Marker Interface Select	Operation with Marker Interface

FUNCTIONAL DESCRIPTION

NORMAL OPERATION

RECEIVE PATH. The circuit decodes the data received on inputs $\overline{JE}^+$ and $\overline{JE}^-$. There are three decoding modes, selected according to the state of the AMI pin :

- AMI = 0 HDB3code Inputs : $\overline{JE}^+$ and $\overline{JE}^-$
- AMI = 1 Bipolar code Inputs : $\overline{JE}^+$ and $\overline{JE}^-$
- AMI = 1 Binary code Input : $\overline{JE}^+$ and $\overline{JE}^- = 1$ } or $\overline{JE}^-$ and $\overline{JE}^+ = 1$ }

The data are then formatted in eight-bit words corresponding to a timeslot and presented to the frame memory.

The circuit synchronizes the interface by analyzing the content of the channel 0 timeslots (TS0).

The circuit is synchronized when the following have been recognized :

- An even frame alignment code in frame Tn (X0011011),
- An identifier in frame $T_n + 1$ (second bit of TS0 at 1),
- An even frame alignment code in frame $T_n + 2$.

Loss of frame alignment (desynchronization) is declared on detection of the absence of three consecutive even frame alignment codes or three consecutive odd frame identifiers (see appendix 1). In this case, the outgoing interface remains at "1".

The remote clock, slaved to clock $\overline{HD}$, operates when the interface is synchronized. It delivers frame memory write addresses.

The local clock, slaved to clock $\overline{HL}$, is synchronized by signal STR2 which defines the time at which bit 8 of the even or odd frame TS0 is output by the outgoing interface device.

It delivers the frame memory read addresses (frequency 4 kHz). The frame memory capacity is 64 words x 8 bits (double frame).

Jitter absorption : there are two devices within the circuit :

Frame memory write time select.

This provided for absorbing at least ± 1 bit on each time-slot without loss of information at the outgoing interface. Write time selection and detection are instantaneous.

Frame skip or doubling.

This operation is initiated on reading frame memory address 63 (last timeslot of an odd frame Tn) :

- If the write address is between 56 and 63 (write frame Tn + 2) reading is resumed at address 32. The even frame Tn + 1 is skipped on reading.
- If the write address is between 63 and 6 (write frame Tn + 1), reading is resumed at address 32. The odd frame Tn is read again.

Under limiting conditions for this correction operation, the jitter absorbed by the circuit without loss of information is at least ± 8 TS.

The circuit detects the following alarms :

- Remote frame misalignment (PVTD),
- Incoming interface frame alignment code absent (PVTL),
- Incoming interface desynchronized (JDSY),
- Error rate > 10^{-3} (TE),
- Over than 75 % bits at "1" in received data (SIA),
- Remote clock $\overline{Hd}$ absent (MQHX),
- Frame skip or doubling (SAUT),
- Clocks plesiochronous (AV).

Alarms resulting dispositions.

When JDSY, TE or MQHX are set :

- Bit 3 of registers R5 and R2 is set to "1" and immediately transmitted to the odd TSO on the outgoing interface JS (when circuit EF7333 is used without marker interface).
- The outgoing interface JS will remain high.

When the JDSY alarm is set, the TE alarm is disabled and the F4kHz output remains at "0".

TRANSMIT PATH. The transmit multiplexing function provides for insertion at the outgoing interface of even or odd frame timeslots TS0 contained in two internal registers R1 and R2.

The transmit clock, synchronized by signal STR1, controls this multiplexing : Signal STR1 define the time at which bit 8 of the even timeslot TS0 is present at the incoming interface input (frequency 4 kHz).

In this operating mode, the content of the even TS0 is X0011011 (R1) and the content of the odd TS0 is X1XXXXXX (R2).

In the absence of a programmed value, bit 3 of the odd TS0 applies the "OR" operation to the JDSY, TE and SIA alarms.

According to the decoding mode selected for inputs $\overline{JE}$+ and $\overline{JE}$–, the code used for the data on outputs JS+ and JS– will be as follows :

- AMI = 0 HDB3 code Outputs : JS^+ and JS^-
- AMI = 1 Bipolar code Outputs : JS^+ and JS^-
- AMI = 1 Binary code Output : JS^+ "or" JS^-

For proper operation, pins PR, ITC and ATC must be tied to V_{SS} when the marker interface is not selected (MQ = 0).

OPERATION WITH MARKER INTERFACE

Input MQ is at "1" in this case. This operating mode provides access to six internal registers of the circuit. (refer to APPENDIX 3).

To be replaced by the enclosed registers description

The six registers are accessible by programming pins ATC, ITC.

Pin ATC receives the register address and pin ITC receives the content to be written into the addressed register. The last bit of ATC is a read bit and the last bit of ITC is write bit. The register content may be read serially at D0.

These registers are not initialized on powering up the circuit.

BIT	1	2	3	4	5	6	7	8
Content of Register R5	PVTD	PVTL	MQHX	JDSY	SIA	TE	AV	SAUT

CIRCUIT TEST

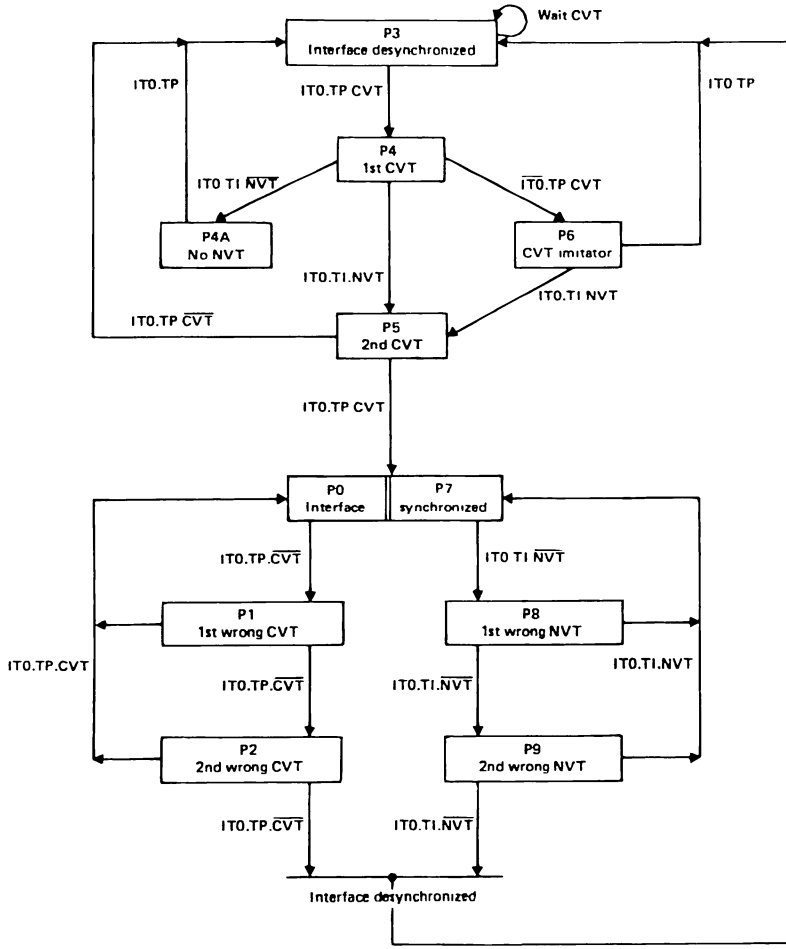
The COMTEST input is used to insert at the outgoing interface a test which is 10101100 for all even frame timeslots and 01010011 for all odd frame timeslots.

The 1-bit register R6 is used to loop the outgoing interface to the incoming interface when set to "1" (JS^+ and JS^- internaly switched to $\overline{JE}$+ and $\overline{JE}$–).

In this case, the remote clock $\overline{HD}$ is internaly switched to the local clock HL. The even and odd timeslots TS0 are then the contents of registers R3 and R4.

APPENDIX 1

FRAME ALIGNMENT LOSS AND RECOVERY ALGORITHM



- $\underline{CVT}$: Even frame alignment code correct
- $\overline{CVT}$: Even frame alignment code not recognized
- $\underline{NVT}$: Odd frame identifier correct
- $\overline{NVT}$: Odd frame identifier not recognized
- $\underline{ITO}$: Channel 0 timeslot
- $\overline{ITO}$: Channels 1 - 31 timeslot
- TP : Even frame
- TI : Odd frame

APPENDIX 2

ERROR RATE ALARM

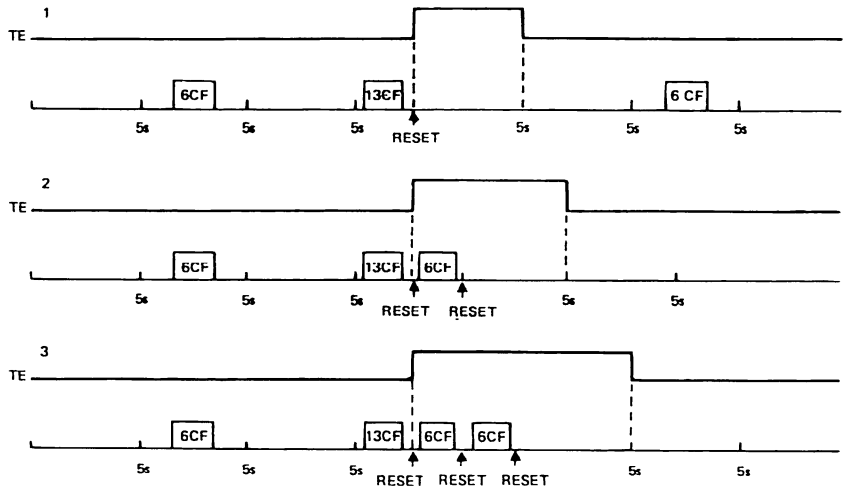
The error rate is calculated over a 5 s period, interrupted as soon as the threshold (13 even frame alignment codes wrong) is reached.

The TE alarm then goes to "1" and is reset only if the number of wrong frame alignment codes is less than six in the next 5 s period.

If not, when the six wrong frame alignment codes threshold is reached a new 5 s count is begun, the TE alarm remaining at "1".

The TE alarm is disabled when the interface is desynchronized (JDSY = 1).

EXAMPLE



CF . Wrong even frame alignment codes

APPENDIX 3

ALARM INDICATION SIGNAL

The frame examination covers 512 bits (1 double-frame), after which the JDSY alarm goes to "1" if the circuit is desynchronized. If the number of "0" bits in the frame during this interval is two or less, the alarm indication signal (SIA) goes to "1".

APPENDIX 3

REGISTERS DESCRIPTION

Register R1 : contains the outgoing junction even frame TSO value.
Only bit 1 can be accessed by the microprocessor interface. The content of this register will be transmitted in line if the circuit is not operating in looped mode.

Register R2 : contains the outgoing junction odd frame TSO value.
Only bit 2 cannot be modified, it remains at "1". Bit 3 can either be at "0" or "1" as a result of a logic OR with the 3 alarms JDSY, TE and MQHX. The content of this register will be transmitted in line only if the circuit is not operating in looped mode.

Register R3 : will contain a value to be introduced into even frame TSO (8 bits). Its content is transmitted in looped mode.

Register R4 : will contain a value to be introduced into odd frame TSO. Its content is transmitted in looped mode.

Register R5 : is a read only register containing the alarms. It is controlled by receive function of EF7333 circuit

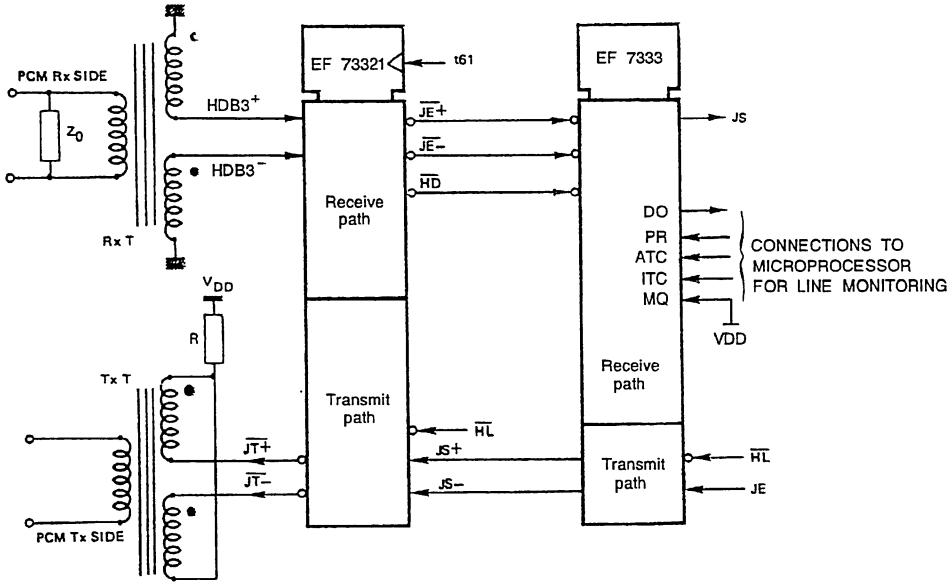
- bit 1 contains the value of bit 3 of incoming junction odd frame TSO. When the value of this bit is "1", this means that the remote end does not control the frame it receives any more. (PVTD alarm - remote frame locking loss).
- bit 2 indicates that the EF7333 synchronous device has found no frame locking code (PVTL alarm - local frame locking loss).
- bit 3 indicates that clock $\overline{HD}$ is missing (MQHX alarm).
  In this application oscillator t61 has stopped operating.
- bit 4 indicates that the synchronous device is no more synchronized (JDSY alarm - synchronization loss).
- bit 5 indicates that a SIA signal is received (SIA alarm - remote alarm indication signal). When JDSY = 0, the junction is synchronized, SIA = 0. When JDSY = 1, the junction is not synchronized, SIA = 1 during two frames.
- bit 6 indicates an excessive error rate higher than 10^{-3} detected on the frame locking codes (TE alarm).
- bit 7 indicates local clock lead or delay compared to remote clock (AV alarm)
  - AV = 1 : frame skip ($\overline{HD}$ faster than $\overline{HL}$)
  - AV = 0 : frame doubling ($\overline{HD}$ slower than $\overline{HL}$)
- bit 8 indicates frame skip or doubling on reading of internal frame memory. Its state changes on each frame skip or doubling operation (SAUT alarm).

Register R6 : contains only 1 bit for selecting the looped mode ;

- If R6 = 0, normal operation, the contents of R1 and R2 are in time.
- If R6 = 1, looped mode operation. JS+ and JS– are internally connected to $\overline{JE}$+ and $\overline{JE}$–, and $\overline{HD}$ is internally connected to $\overline{HL}$. The contents of R3 and R4 are in line.

TYPICAL APPLICATION

Using EF7333 and EF73321 in a 2048 kHz PCM line
For data transmission/reception and frame monitoring



t61 : 16384 kHz clock
R x T : Line receiver transformer
T x T : Line transmit transformer
HL : Local 2048 kHz clock

Note : EF73321 layout considerations : for correct operation of transmission drivers a 100 nF decoupling capacitor must be connected between V_{DD} and V_{SS} as close as possible to the supply pins.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}, V_{SS}	Supply Voltage	$-0.3\ V < V_{DD}-V_{SS} < 7\ V$	V
V_I	Input Voltage	$V_{SS}-0.3\ V \leq V_I \leq V_{DD} + 0.3\ V$	V
P	Maximum Power Dissipation	Pmax = 600 mW	mV
T_{stg}	Storage Temperature Range	− 55 °C to 125 °C	°C

STATIC ELECTRICAL CHARACTERISTICS

Ambient Temperature Range : 0 °C to 70 °C–TYPICAL VALUES AT 25 °C

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage	4.75	5	5.25	V
P_W	Power Consumption		200	450	mW
C_e	Stray Capacitance between One Input and Ground		5	10	pF
C_s	Stray Capacitance between One Output and Ground		5		pF

INPUTS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{IL}	Input Low Voltage	– 0.3		0.6	V
V_{IH}	Input High Voltage	2.2		V_{DD}+0.3	V
$\|I_{IL}\|$	Input Low Current (V_I = 0 V)			1	µA
I_{IH}	Input High Current ($V_I = V_{DD}$)			1	µA

OUTPUTS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{OL}	Output Low Voltage (I_{OL} = 0.4 mA)			0.4	V
V_{OH}	Output High Voltage (I_{OH} = – 40 µA)	2.5			V
$\|I_Z\|$	DO Output Leakage Current (0.4 V ≤ V_O ≤ 2.4 V)			10	µA

DYNAMIC ELECTRICAL CHARACTERISTICS

Ambient Temperature Range : 0 °C to 70 °C–TYPICAL VALUES AT 25 °C

Symbol	Parameter	Min.	Typ.	Max.	Unit
	Clocks $\overline{HD}$, $\overline{HL}$ (fig. 1)				
T	Period $\overline{HD}$	350	488	2000	ns
t_{WL}	Duration when Low $\overline{HD}$	150			ns
T	Period $\overline{HL}$ (duty cycle = 1/2 ± 5 %)	450	488	2000	ns
t_{TLH}	Rise Time		10	25	ns
t_{THL}	Fall Time		10	25	ns
	Inputs $\overline{JE}^+$, $\overline{JE}^-$/$\overline{HD}$. (fig. 2)				
$t_{set\text{-}up}$	Set-up Time	50			ns
t_{hold}	Hold Time	30			ns
	Inputs STR1, STR2, COMTEST, JE/$\overline{HL}$. (fig. 2)				
$t_{set\text{-}up}$	Set-up Time	50			ns
t_{hold}	Hold Time	30			ns
t_{PLH}	Outputs JS^+, JS^-, JS, F4 kHz (C_L = 50 pF)-(fig. 3)			250	ns
t_{PHL}	Propagation Time			250	ns

Alarms TE, SIA, JDSY, MQHX, PVTD, PVTL, SAUT, AV are held for 512 $\overline{HD}$ or $\overline{HL}$ clock pulses
Inputs AMI and MQ are wired to a fixed value ("0" or "1") according to the selected operating mode.

Figure 1.

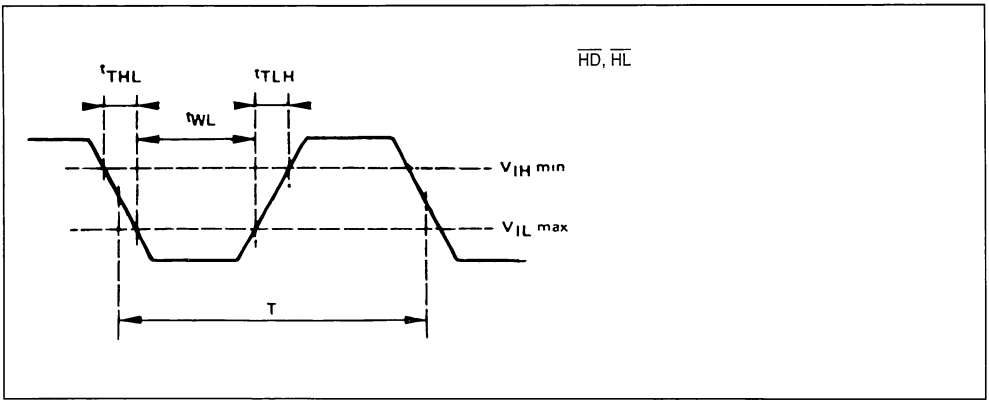


Figure 2.

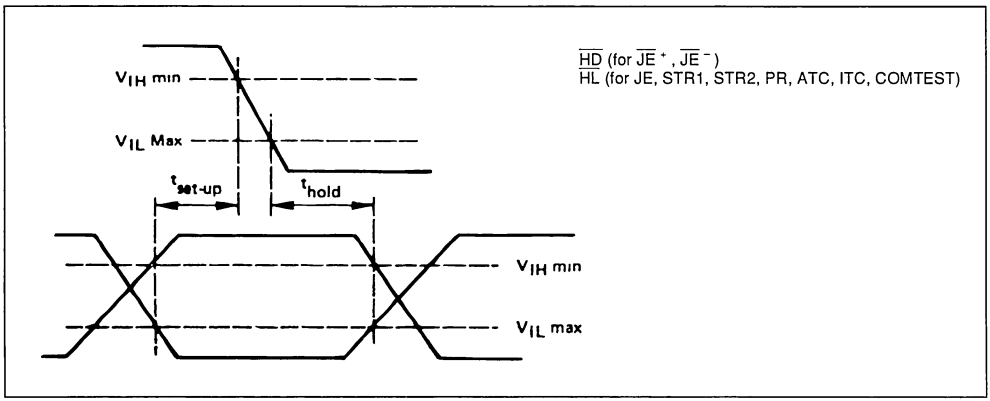
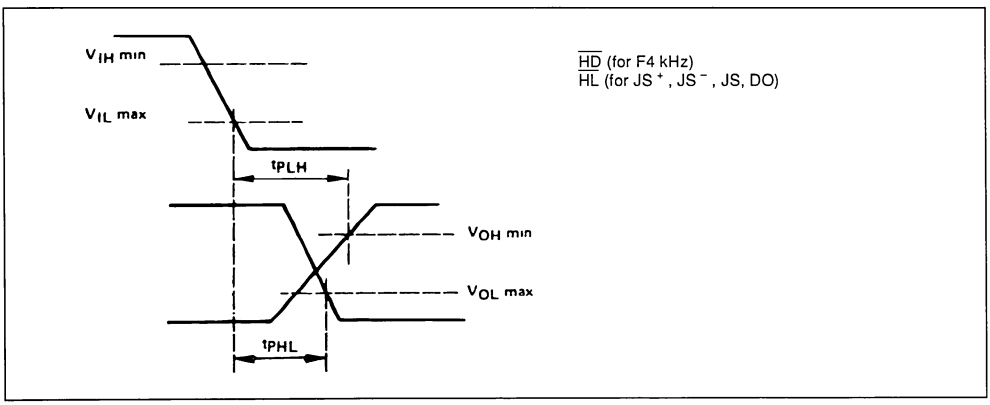


Figure 3.



TIMING DIAGRAMS

Figure 4 : Outgoing Interface Synchronization by STR2.

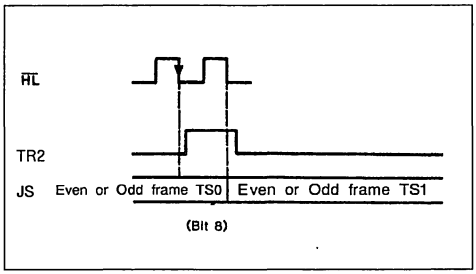


Figure 5 : Incoming Interface Synchronization by STR1.

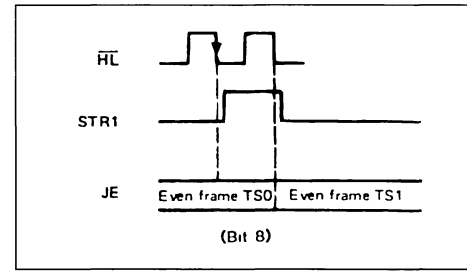


Figure 6 : PVTD alarm.

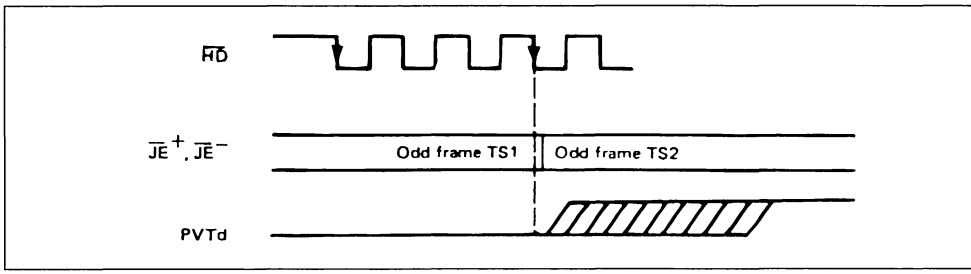


Figure 7 : PVTL alarm.

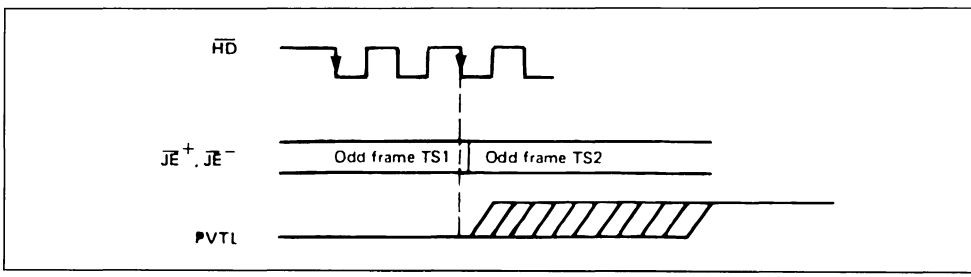


Figure 8 : TE alarm.

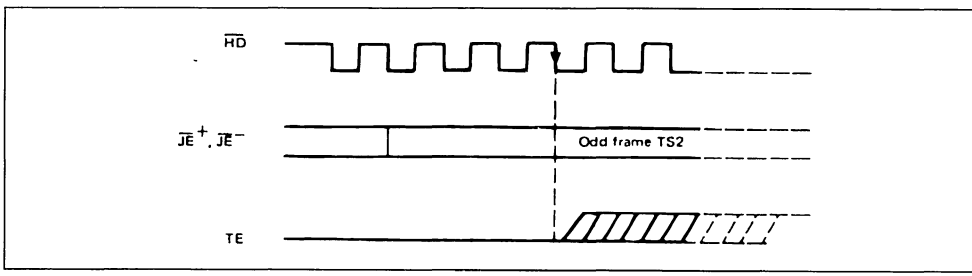


Figure 9 : MQHX alarm.

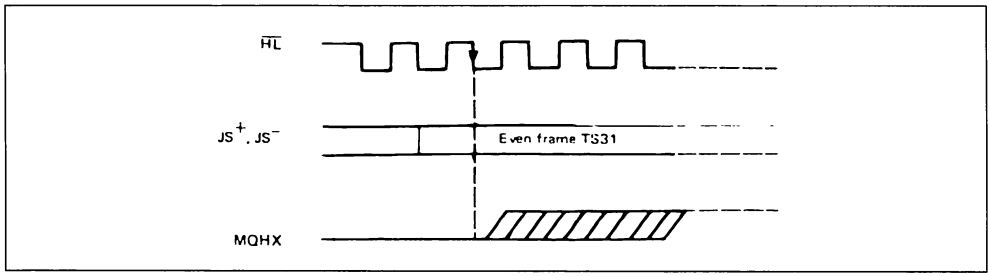


Figure 10 : Frame Doubling.

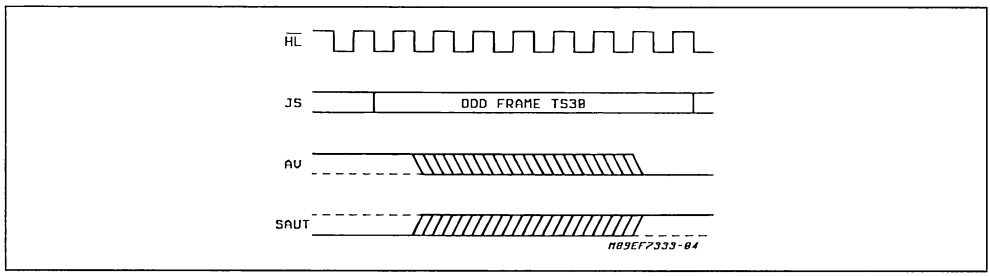


Figure 11 : Frame Skip.

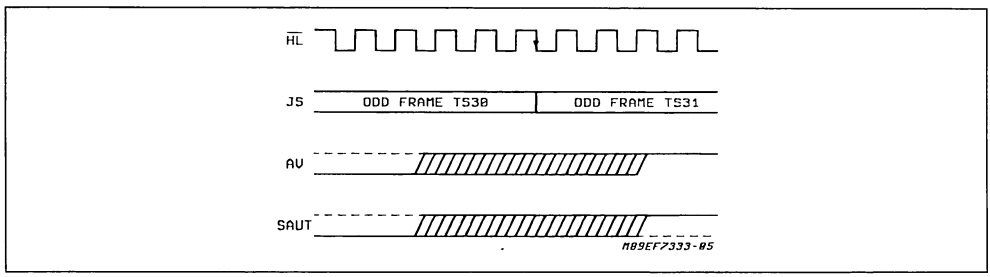


Figure 12 : JDSY alarm

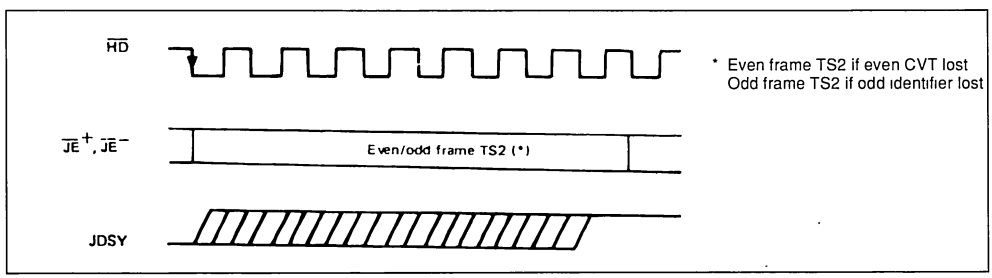
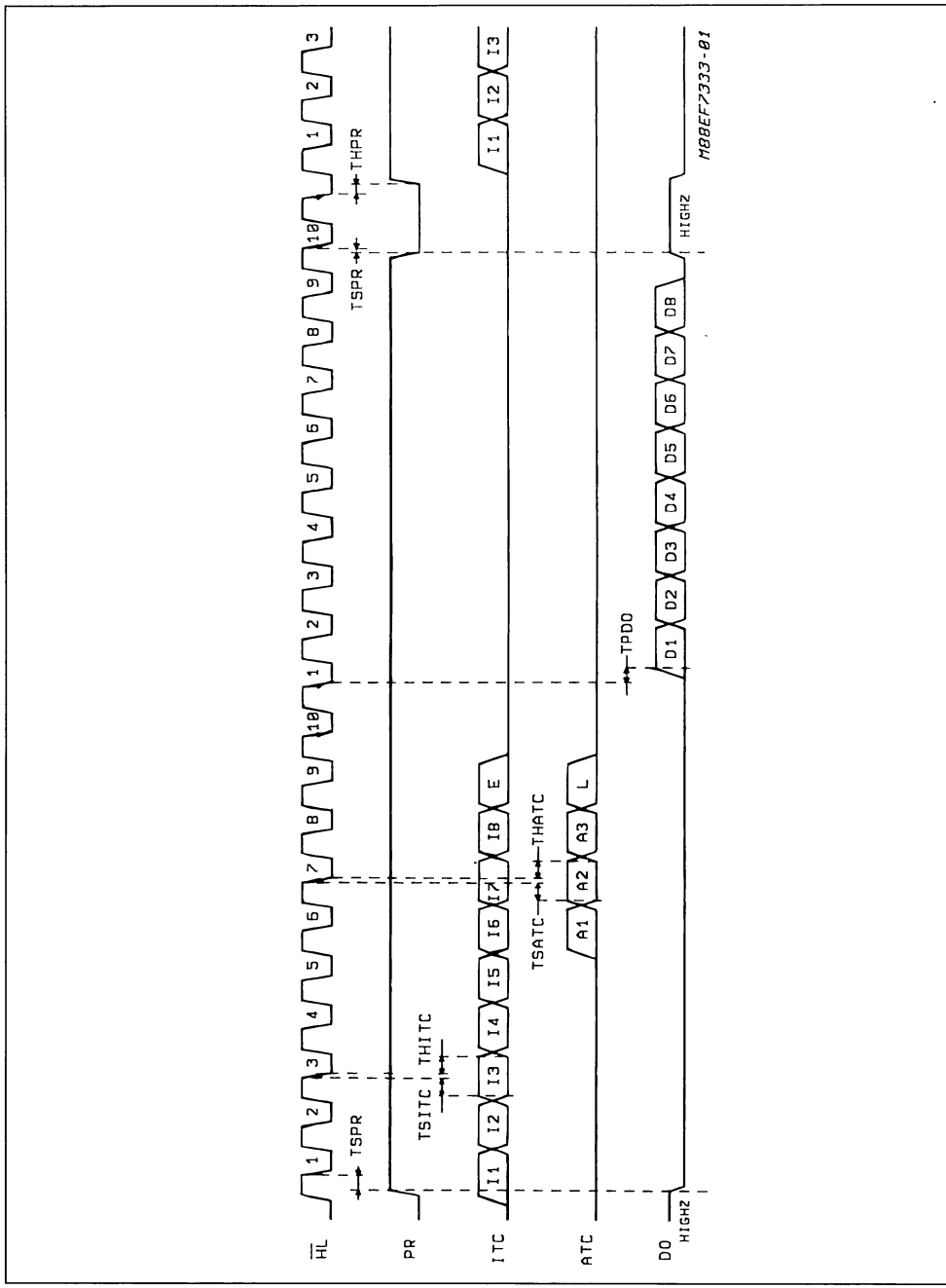


Figure 13 : Marker Interface Timing Diagram.

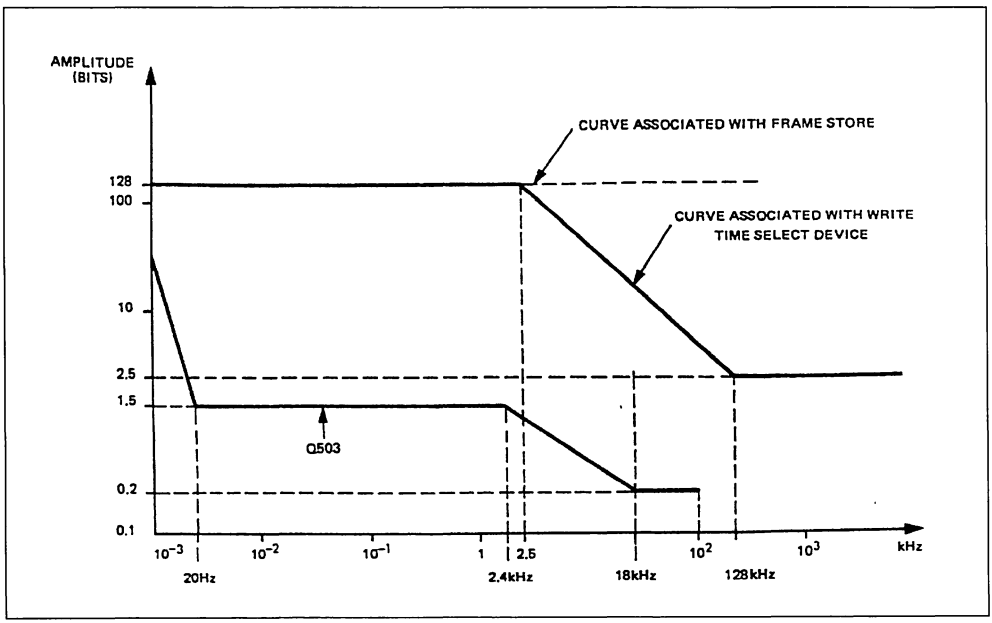


Symbol	Parameter	Min.	Typ.	Max.	Unit
TSPR	Set-up Time	50			ns
THPR	Hold Time	30			ns
TSITC	Set-up Time	50			ns
THITC	Hold Time	30			ns
TSATC	Set-up Time	50			ns
THATC	Hold Time	30			ns
TPDO	Propagation Time (C_L = 50 pF)			300	ns

ADDRESSING			
A1	A2	A3	Addressed Register
1	0	0	R1
0	1	0	R2
1	1	0	R3
0	0	1	R4
1	0	1	R5
0	1	1	R6

L = 1 E = 0 Read
L = 0 E = 1 Write
L = 1 E = 1 Write and then read

Figure 14 : Limiting Curves for Jitter Absorbed by EF7333 (without loss of information or frame skipping).

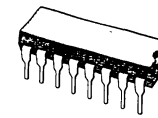


SGS-THOMSON MICROELECTRONICS

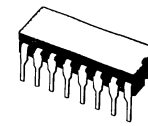
EF73321

PCM LINE TRANSCEIVER

- NMOS TECHNOLOGY
- OPERATES FROM + 5 V SUPPLY
- DIGITAL TECHNOLOGY THROUGHOUT
- EXTRACTS DISTANT CLOCK TRANSMITTED BY A PCM TRUNK
- CAN HANDLE PEAK TO PEAK JITTER AMPLITUDE UP TO 0.25 BIT FOR AN 8-BIT PERIOD
- INTEGRATED TRANSMIT AND RECEIVE AMPLIFIERS
- TTL-COMPATIBLE INPUT/OUTPUT



DIP16
Plastic



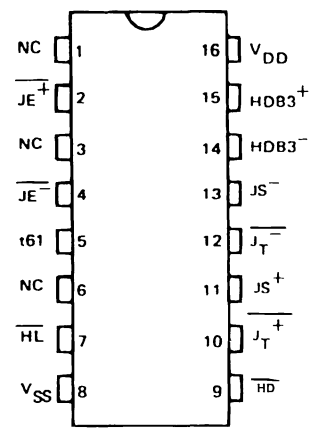
DIP16
Ceramic

ORDER CODE : EF73321P
EF73321C

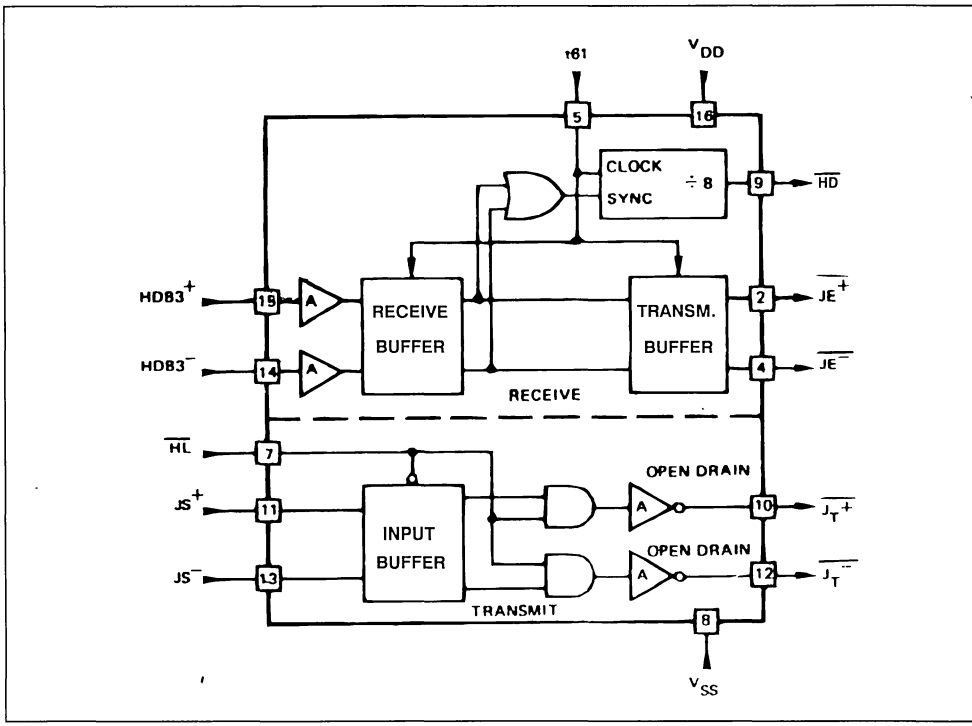
DESCRIPTION

The EF73321 provides the interface between a 2.048 or 1.544 Mbits/s PCM trunk and the switching equipment. The receiving side amplifies and reshapes the bipolar signals from a receive transformer and extracts from the signals the distant clock HD. On the transmitting side it calibrates pulses in terms of duration and amplitude by means of transistor circuits directly coupled to a transmit transformer.

PIN CONNECTIONS



BLOCK DIAGRAM



PIN DESCRIPTION

POWER SUPPLY

N°	Name	Type	Function	Description
8	V_{SS}	S	Supply	Ground
16	V_{DD}	S		+ 5 V ± 5 %

RECEIVE

N°	Name	Type	Function	Description
5	t61	I	–	16384 kHz or 12352 kHz Clock. Synchronises outputs JE+; JE– and HD.
15 14	HDB3+ HDB3–	I I	Data Input	Bipolar signals in HDB3 code received from the receive transformer. The amplitude of these signals is between – 5 V and + 5 V. Each positive pulse on HDB3+ (HDB3–) resynchronises the circuit clock and is reconstituted in calibrated form on output JE+ (JE–). Negative pulses have no effect on the circuit as the inputs are protected.
2 4	JE+ JE–	O O	Data Output	Received HDB3 signals are resynchronised with HD and calibrated in terms of amplitude (TTLLS compatible levels).
9	HD	O	Distant Clock Output	The distant clock recovered from the signal on HDB3+, HBD3–. The nominal frequency is 2048 kHz or 1544 kHz in the absence of jitter.

TRANSMIT

N°	Name	Type	Function	Description
7	HL	I	Clock	Local clock, nominal frequency 2048 kHz or 1544 kHz.
11 13	JS+ JS–	I I	Data Input	The data is recognised on the falling edge of HL.
10 12	JT+ JT–	O O	Data Output	These open drain outputs are connected to the windings of the transmit transformer. Recognition of a "1" on JS+ (JS–) grounds the winding of the transformer connected to JT+ (JT–) for the duration of "1" level of HL. These outputs are protected against short-circuits by current limiting internal to the circuit.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	$-0.3\ V \leq V_{DD} \leq 7\ V$	V
V_I	Input Voltage Range (except inputs HDB3 + and HBD3 –)	$-0.3\ V \leq V_I \leq V_{DD} + 0.3\ V$	V
P	Maximum Power	P_{max} = 250 mW in 0 °C to 70 °C Range	mW
T_{stg}	Storage Temperature Range	– 55 °C to + 150 °C	°C

FUNCTIONAL DESCRIPTION

RECEIVE PATH

The PCM Line Transceiver receives directly from the receive transformer on inputs HDB3 + and HDB3– data in HDB3 code. It synchronizes this data by means of the clock on input t61 and converts it to voltage pulses of calibrated duration on outputs $\overline{JE}$+ and $\overline{JE}$–. To be recognized correctly by this circuit the received data must satisfy minimum and maximum duration conditions (Refer to timing diagrams).

Distant clock $\overline{HD}$ is provided by a counter which divides by 8 the frequency of the clock t61. This counter is resynchronized with the data of the PCM trunk on each positive-going edge at HDB3 + or HDB3–. The period of $\overline{HD}$ may vary by 0.25 bit within a period of 8 bits without degradation of the phase relationships between $\overline{JE}$+, $\overline{JE}$– and $\overline{HD}$ (Cf. fig.1). If the variation occurs in an interval exceeding 4 bits but less than 8 bits the phase relationships between $\overline{JE}$+, $\overline{JE}$– and $\overline{HD}$ are modified (Cf. fig. 2 and fig. 3).

In all cases outputs $\overline{JE}$+ and $\overline{JE}$– remain stable on either side of the falling edge of HL so as to be sampled correctly by the EF7333.

TRANSMIT PATH

The signals JS+ and JS– to transmit are sampled on the falling edge of clock signal HL and calibrated by the duration for which this signal is high.

Open drain outputs $\overline{JT}$+ and $\overline{JT}$– drive the primary windings of the transmit transformer directly. They are protected against overcurrents occurring should the secondary windings of this transformer be short-circuited, in which case the primary behaves as a very low resistance connecting the output to supply rail V_{DD}.

RECEIVE TIMING DIAGRAM

Figure 1 : External Signals with Jitter < 0.25 Bit within 8-Bit Period.

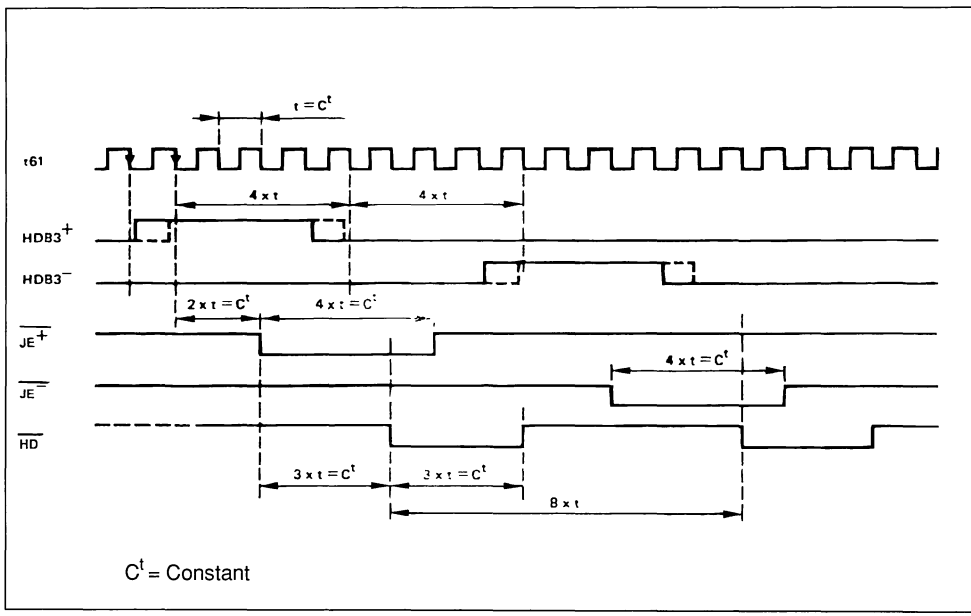


Figure 2 : External Signals with HDB3$^+$ and HDB3$^-$ Signal Period 6 x t.

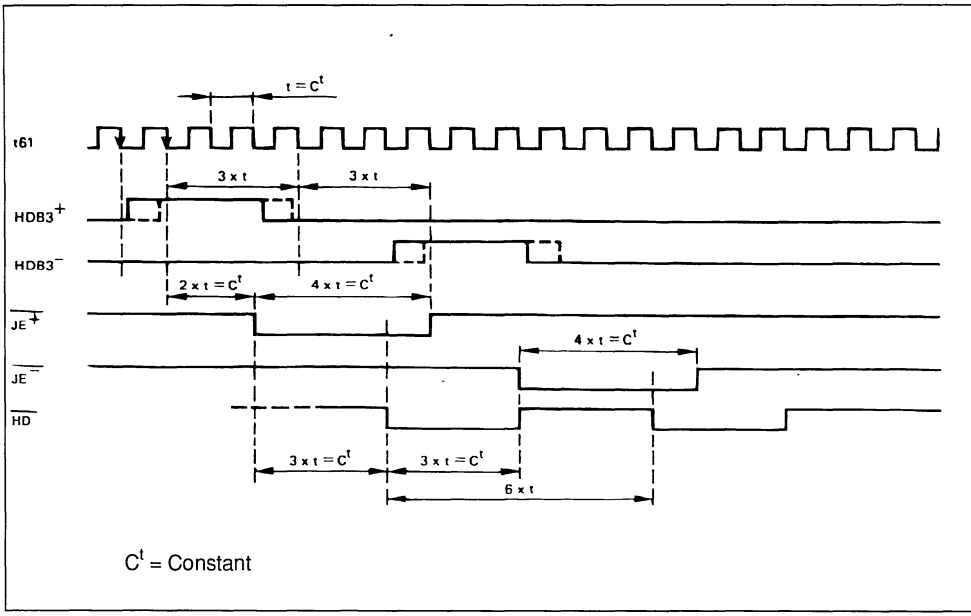
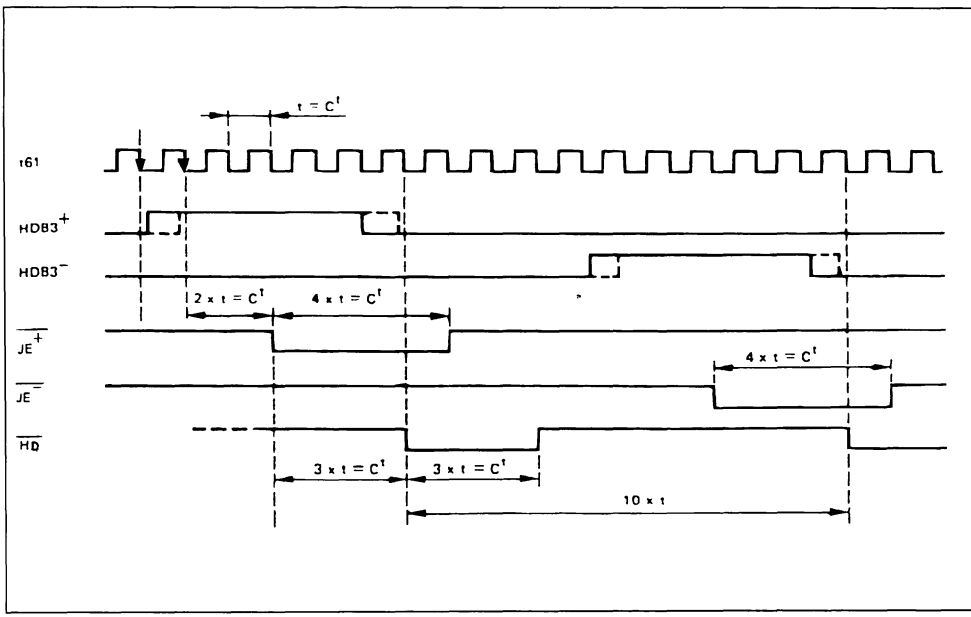


Figure 3 : External Signals with HDB3$^+$ and HDB3$^-$ Signal Period 10 x t.



TRANSMIT

Figure 4 .

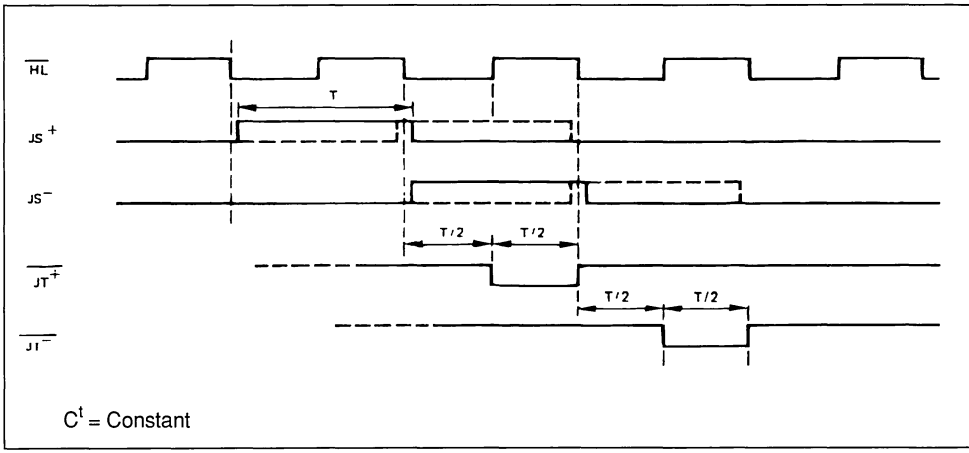
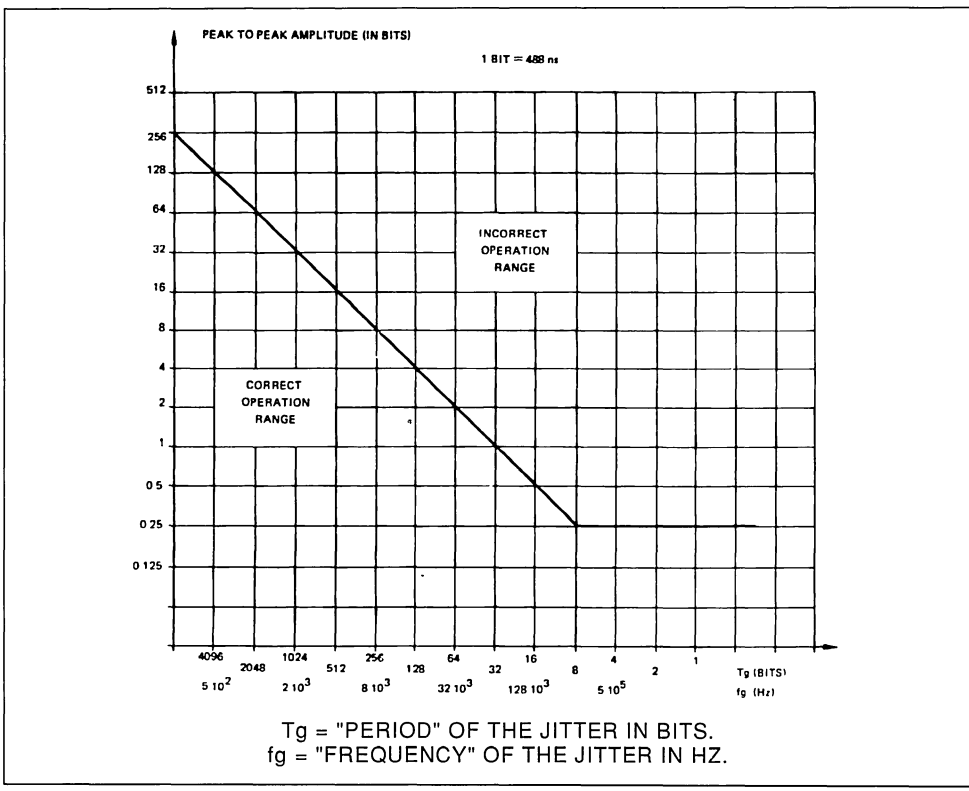


Figure 5 : EF73321 Operating Range as a Function of Jitter Period and Frequency.

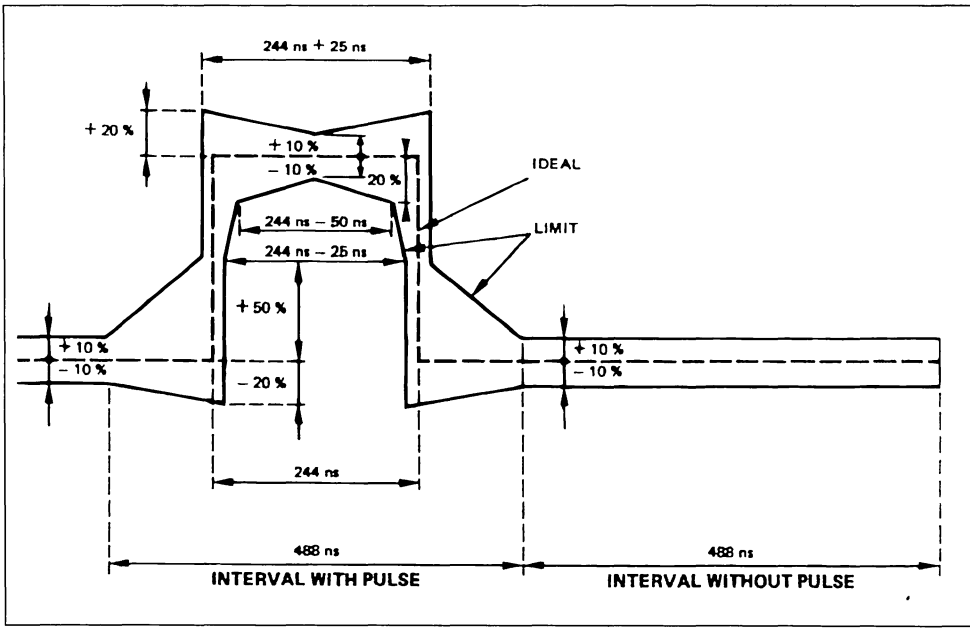


TRANSMIT PATH

Pulse limiting curves for 2 048 kbit/s CEPT PCM trunk.

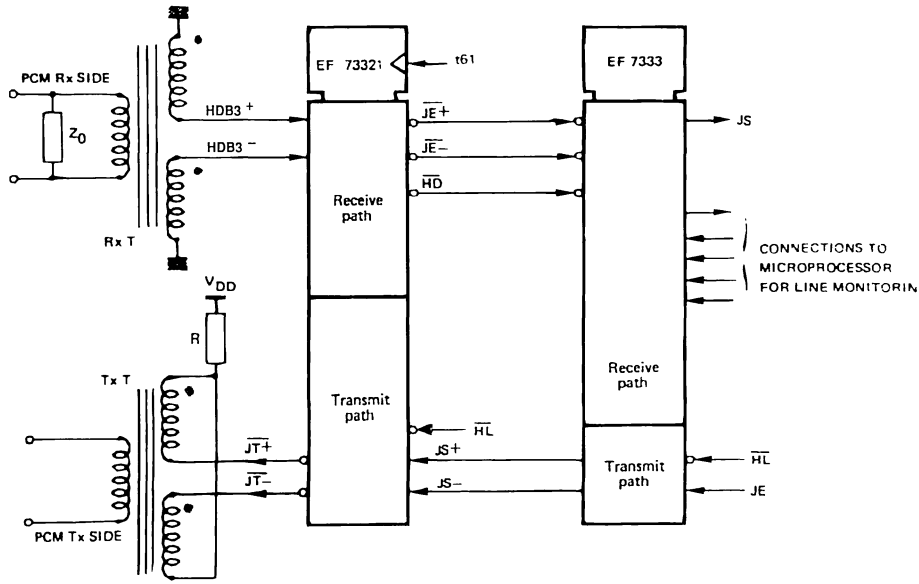
The limiting curves below are for a resistive load of 120 Ω connected across the secondary winding of the transmit transformer.

Figure 6 .



TYPICAL APPLICATION

Using EF7333 and EF73321 in a 2048 kHz PCM line
for Data transmission/reception and frame monitoring.



t61 : 16384 Khz CLOCK

Rx T : LINE RECEIVE TRANSFORMER

Tx T : LINE TRANSMIT TRANSFORMER

$\overline{HL}$: LOCAL 2048 Khz CLOCK

Note : EF73321 layout considerations : for correct operation of transmission drivers a 100 nF decoupling capacitor must be connected between V_{DD} and V_{SS} and located as close as possible to the supply pins.

STATIC ELECTRICAL CHARACTERISTICS

Ambient Temperature Range : 0 °C to + 70 °C - Typical Values at + 25 °C

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{DD}	Positive Power Supply	4.75	5	5.25	V
I_{DD}	Supply Current	–	20	40	mA
	Stray Capacitance between one Input and Ground (outputs loaded with C_L = 25 pF)	–	5	10	pF

INPUTS

Symbol	Parameter	Min.	Typ.	Max.	Unit
	Voltage at Input HDB3+/HDB3– When Low When High	 – 5 2.2	 – –	 0.6 5	 V V
	Resistance at Input HDB3+/HDB3– (inverse voltage V_I = – 5 V)	—	10	—	kΩ
	Voltage at input JS+/JS–/$\overline{HL}$ When Low When High	 – 0.3 2.2	 – —	 0.6 V_{DD}	 V V
	Voltage at Input t61 When Low When High	 0 2.6	 — —	 0.6 V_{DD}	 V V

OUTPUTS

Symbol	Parameter	Min.	Typ.	Max.	Unit
	Voltage at Output $\overline{HD}$/$\overline{JE}$+/$\overline{JE}$– When Low (I_{OL} = 0.4 mA) When High (I_{OH} = – 40 µA)	 0 2.6	 — —	 0.4 V_{DD}	 V V
	Voltage at Output $\overline{JT}$+/$\overline{JT}$– when Low (R_L = 175 Ω to V_{DD})	250	450	750	mV
	Current at Output $\overline{JT}$+/$\overline{JT}$– when High Impedance (V_{OH} = 12 V)	—	—	100	µA
	Current at Output $\overline{JT}$+/$\overline{JT}$– (output current protection)	—	—	35	mA

DYNAMIC CHARACTERISTICS

Typical values at + 25 °C (0 °C < T_A < + 70 °C).

CLOCKS

Symbol	Parameter	Min.	Typ.	Max.	Unit
	Clock t61 (fig.8)	—	12352	—	kHz
		—	16384	16500	kHz
t_{PL}	when Low	20	—	—	ns
t_{PH}	when High	20	—	—	ns
	Clock $\overline{HL}$ (fig. 10)	—	1544	—	kHz
		—	2048	2200	kHz
t_{THL}	Fall Time	—	—	30	ns
t_{TLH}	Rise Time	—	—	30	ns

INPUTS

Symbol	Parameter	Min.	Typ.	Max.	Unit
	Inputs HDB3+/HDB3– (fig. 9)				
t_H	Min. Pulse Duration	t			ns
t_L	Max. Pulse Duration			4 x t	ns
	Inputs JS+/JS– (fig. 10)				
t_{set-up}	Set up Time	20			ns
t_{hold}	Hold Time	30			ns

OUTPUTS

Symbol	Parameter	Min.	Typ.	Max.	Unit
	Outputs $\overline{JE}$+/$\overline{JE}$– Relative to $\overline{Hd}$ (CL = 25 pF, fig. 11)				
t_{set-up}	Set up Time	150	3 x t		ns
t_{hold}	Hold Time	30	t		ns
t_{THL}	Fall Time		15		ns
t_{TLH}	Rise Time		20		ns
	Outputs $\overline{JT}$+/$\overline{JT}$– (R_L = 175 Ω = to V_{DD}, fig. 12)				
t_{WM}	Pulse Duration (C_L = 25 pF)	219	244	269	ns
	$\overline{HL}$ = 2048 kHz				

Figure 8.

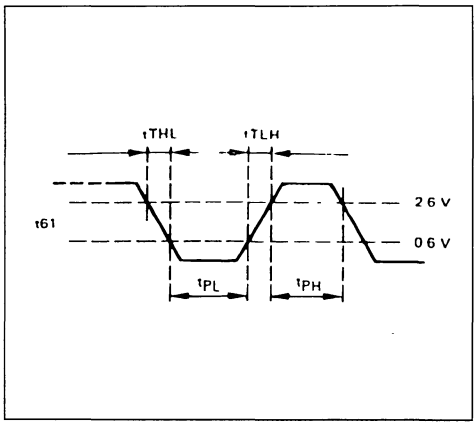


Figure 9.

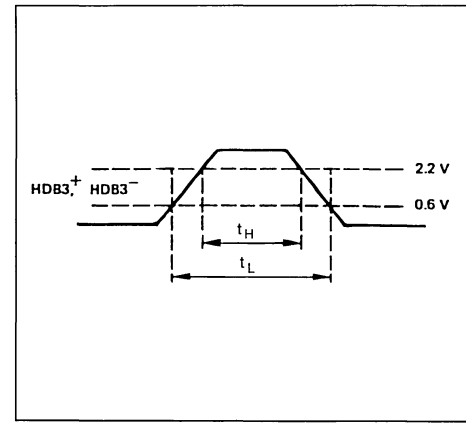


Figure 10.

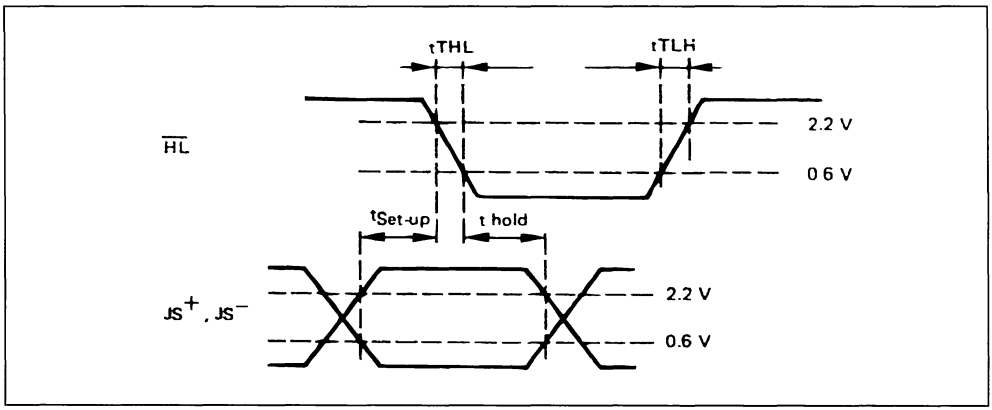


Figure 11.

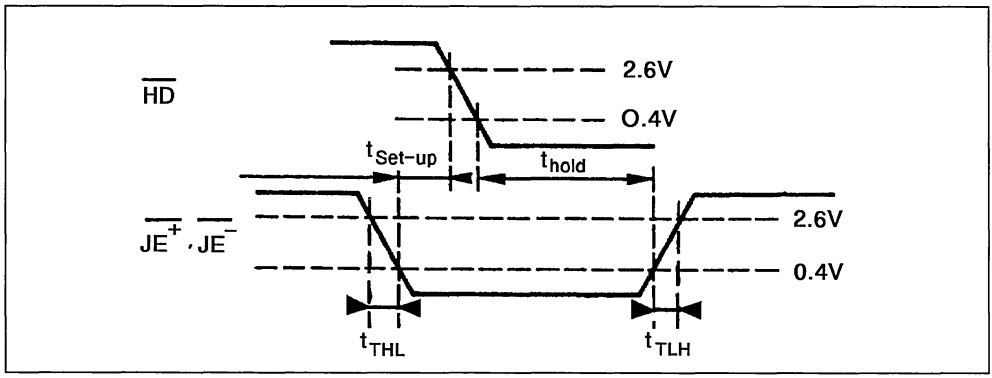
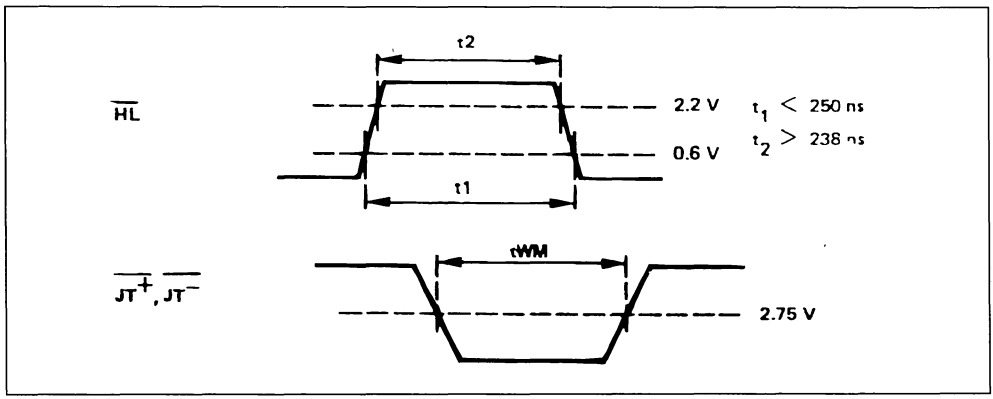


Figure 12.

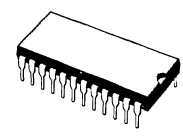


SGS-THOMSON MICROELECTRONICS

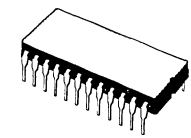
M116

PCM CONFERENCE CALL AND ATTENUATION/NOISE SUPPRESSION CIRCUIT

- 32 MAXIMUM CONFERENCED CHANNELS IN ANY COMBINATION FROM 10 CONFERENCES OF 3 CHANNELS TO 1 CONFERENCE OF 32 CHANNELS
- 3 TO 32 SERIAL CHANNELS PER FRAME (controlled by $\overline{\text{SYNC}}$ signal period)
- TWO OPERATION MODES AVAILABLE (conference and transparent modes)
- TYPICAL BIT RATES : 1536/1544/2048Kbits/s
- COMPATIBLE WITH ALL KINDS OF PCM BYTE FORMAT
- MU AND A LAWS AVAILABLE (pin programmable)
- EQUAL PRIORITY TO EVERY CHANNEL
- ONE FRAME (and one channel) DELAY FROM SENDING TO RECEIVING CHANNELS
- OVERFLOW INFORMATION FOR EACH CONFERENCE SENT OUT BY PINS $\overline{\text{OS}}$ (overflow signalling) AND ON DATABUS ON MPU REQUEST
- TONE OUTPUT FOR MASKABLE CONFERENCED CHANNELS. THE DURATION AND FREQUENCY ARE CONTROLLED BY EXTERNAL PINS (TD and TF)
- INSTRUCTION SET COMPATIBLE WITH THE M088
- PROGRAMMABLE ATTENUATION (0/3/6dB) ON EACH INPUT CHANNEL (both in conference or transparent mode)
- PROGRAMMABLE NOISE SUPPRESSION FOR EACH OUTPUT CHANNEL ACTING ON FOUR DIFFERENT LEVELS
- 5V POWER SUPPLY
- MOS AND TTL COMPATIBLE INPUT/OUTPUT LEVELS
- MAIN INSTRUCTIONS CONTROLLED BY THE MICROPROCESSOR INTERFACE :
  - Channel connection to a conference
  - Channel attenuation and/or noise suppression in transparent mode
  - Channel disconnection from both conference and transparent modes
  - Overflow status
  - Operating mode
  - Channel status



DIP24 (Plastic)



DIP24 (Ceramic)

ORDER CODES : M116F1
M116B1

DESCRIPTION

The M116 is a product specifically designed for applications in connection with PCM digital exchanges. It is able to handle up to 32 channels in any conference combination, from 3 people (max number of conferences is 10) to 32 people (only one conference).

The parties to be conferenced must previously be allocated through the Digital Switching Matrix (M088) in a single serial wire at the M116 PCM input (IN PCM pin).

Each channel is converted inside the chip from PCM law to linear law (14 bits). Then it is added to the sum of its conference, from which was previously subtracted its information from the previous frame. In this way a new sum signal is generated.

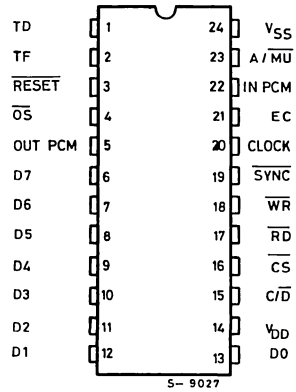
The channel output signal will contain the information of all the other channels in its conference except its own.

After the PCM encoding, the data is serialized by the M116 in the same sequence as the PCM input frame, with one frame (plus one channel) delay and will be reallocated by the DSM (M088) at the final channel and bus position.

A programmable attenuation as well as a programmable noise suppression threshold can be inserted in any channels connected in conference mode or in transparent mode.

M116 is realized with N-Channel technology and packaged in a 24 pin DIL package.

PIN CONNECTION

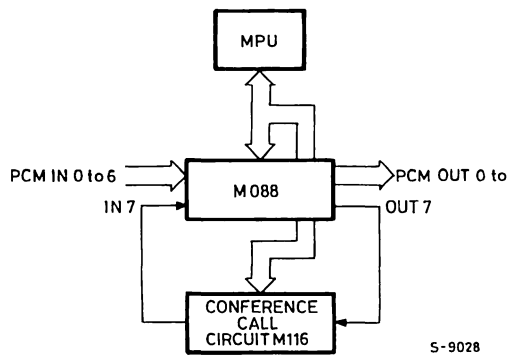


ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}*	Supply Voltage	– 0.3 to 20	V
V_I	Input Voltage	– 0.3 to V_{DD}	
$V_{O\ (off)}$	Off State Output Voltage	– 0.3 to 20	V
P_{tot}	Total Power Dissipation	500	mW
T_{stg}	Storage Temperature	– 65 to 150	°C
T_{op}	Operating Temperature	0 to 70	°C

Stresses above those listed under "Absolute Maximum Ratings" may causes permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

Figure 1 : PCM Conference Call Insertion Scheme.



PIN DESCRIPTION

TD (pin 1)

Tone Duration input pin. When TD = 1, a PCM coded tone is sent out to all channels of the enabled conferences instead of PCM data. TD is latched by the SYNC signal so that all channels have the same tone during the same number of frame. TD = 0 for normal operation.

TF (pin 2)

Tone Frequency input pin. When TF = 1, the tone's amplitude is high. When TF = 0, the tone's amplitude is low. TF is latched by the SYNC signal so that all channels have the same tone frequency during the same number of frame. The PCM coded tone levels correspond to the 1/10 of the full scale.

$\overline{\text{RESET}}$ (pin 3)

Master reset input pin. Reset must be used at the very beginning after power up to initialize the device or when switching from A Law to Mu Law. The internal initialization routine takes two time frames starting from the rising edge of $\overline{\text{RESET}}$. During this initialization time, all databus and PCM output are pulled to a high impedance state.

$\overline{\text{OS}}$ (pin 4)

Overflow Signalling output pin. When $\overline{\text{OS}}$ = 0 one conference is in overflow. This signal is delayed a little over half time slot with respect to the output channel involved in the conference in overflow, see Fig. 9. Ex : if output channel 3 is one of the parties of one conference in overflow, $\overline{\text{OS}}$ = 0 during the second half of the time slot corresponding to output channel 3.

OUT PCM (pin 5)

PCM output pin. The bit rate is 2048 Kbit/s max. The sign bit is the first bit of the serial sequence. The output buffer is open drain to allow for multiple connections.

D0 to **D7** (pins 6 through 13)

Bidirectional Data bus pins. Data and instructions are transferred to or from the microprocessor. D0 is the Least Significant Bit. The bus is tristate when RESET is low and/or $\overline{\text{CS}}$ is high.

C/$\overline{\text{D}}$ (pin 15)

Control input pin. In a write operation C/$\overline{\text{D}}$ = 0 qualifies any bus content as data while C/$\overline{\text{D}}$ = 1 qualifies it as an opcode. In a read operation, the overflow information of the first eight conferences is selected by C/$\overline{\text{D}}$ = 0, the overflow of the last two conferences and the status by C/$\overline{\text{D}}$ = 1.

$\overline{\text{CS}}$ (pin 16)

Chip select input pin. When $\overline{\text{CS}}$ = 0, data and instructions can be transferred to or from the microprocessor and when $\overline{\text{CS}}$ = 1 the data bus is in tristate.

$\overline{\text{RD}}$ (pin 17)

Read control input pin. When $\overline{\text{RD}}$ = 0, read operation is performed. When match conditions for the opcode exist, data is transferred to the microprocessor on the falling edge of $\overline{\text{RD}}$.

$\overline{\text{WR}}$ (pin 18)

Write control input pin. Instructions and opcode from the microprocessor are latched on the rising edge of $\overline{\text{WR}}$ when match conditions exist.

$\overline{\text{SYNC}}$ (pin 19)

Synchronization input pin. When $\overline{\text{SYNC}}$ rises to logic 1, the internal counter is reset so that a new frame can start. The frame format can vary from three channel (three is the minimum number of parties required to form a conference) to thirty two and this number is selected by SYNC. When PCM frames of 1544 Kbit/s are used, the rise edge of the $\overline{\text{SYNC}}$ signal must correspond to the Extra bit (193th). In the other case it must correspond to the first bit of the first channel.

CLOCK (pin 20)

Master clock input pin. Max frequency is 4096KHz.

EC (pin 21)

External clock output pin. This pin provides the master clock for the DSM (M088).
Normally is the same signal as applied to CLOCK input (pin 20). When you select, by Instruction 5, Extra bit operating mode, the first two period of the master clock are cancelled, see fig. 8, in order to allow the operation of the M116 and DSM with PCM frame with Extra bit (ex. 193 bit/frame with PCM I/O of 1544 Kbit/s).

IN PCM (pin 22)

PCM input pin. The max bit rate is 2048 Kbit/s. The first bit of the first channel is found with the rising edge of the SYNC signal if operating mode with Extra bit is not inserted. The Extra bit is found with the rising edge of the SYNC signal if operating mode with Extra bit is inserted.

PIN DESCRIPTION (continued)

A/MU (pin 23)

A Law or MU Law select pin. When A/$\overline{MU}$ = 1. A Law is selected. When A/$\overline{MU}$ = 0, MU Law is selected. The law selection must be done before initializing the device using the $\overline{RESET}$ pin.

Figure 2 : Insertion Schema of M116 in a 480 x 480 Non-Blocking Digital Switching Matrix.

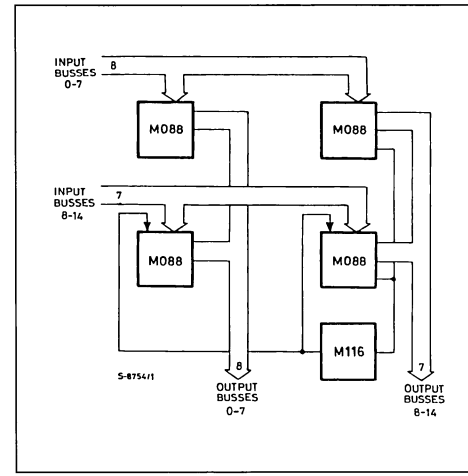
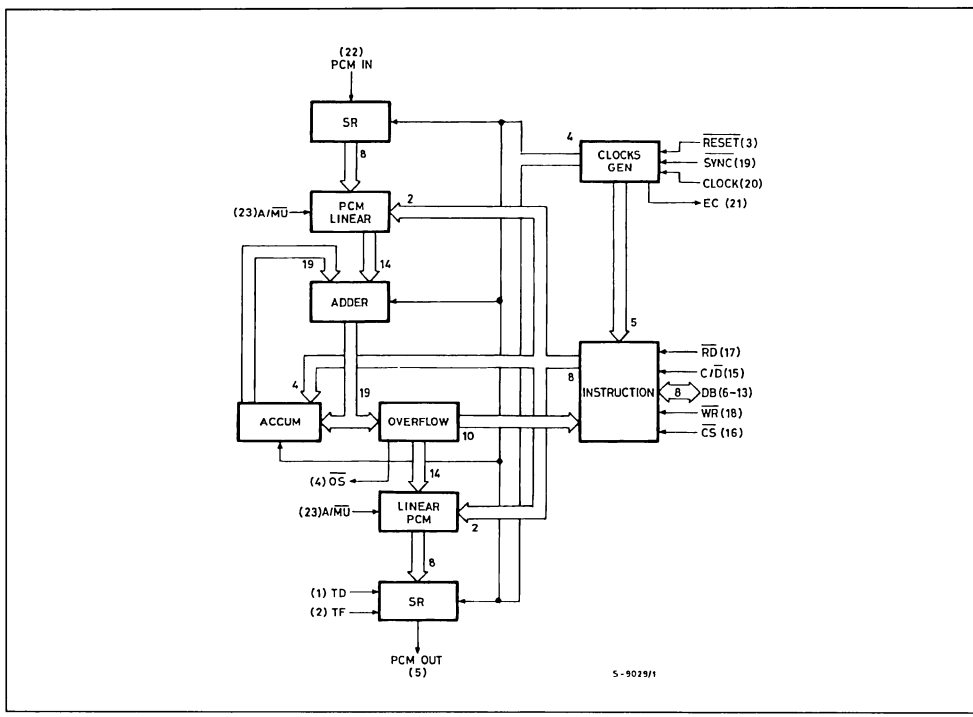


Figure 3 : Block Diagram.



CIRCUIT DESCRIPTION

Through a protocol, the MPU sends the M116 connecting information for each party : the conference number, the conference start bit, the tone insertion enable bit, the number, the attenuation and the noise suppression value for that party.

When a party has to be disconnected the information needed is the disconnection code together with the channel to be disconnected.

The information of channel N, frame M is added during the first half of channel N + 1, frame M and subtracted during the second half of channel N – 1 frame M + 1.

After the Linear to PCM conversion, the subtraction result goes to the parallel-in serial-out Shift Register appearing at the output with one frame plus one channel delay with respect to the corresponding sending information of the specific party.

When many channel are to be conferenced, an attenuation can be desired for each specific party and this is obtained from the PCM to Linear conversion ROM.

If the sum of the channels involved in one conference exceeds the full scale value a saturation appears and the device M116 can signal this overflow condition.

The overflow information, sent out to the databus on MPU request, tells specifically which conference is in overflow at the moment requested.

The number of the channel creating the overflow or in the conference already in overflow, can also be extracted from the $\overline{OS}$ pin, correlating this signal with the $\overline{SYNC}$ signal.

The $\overline{OS}$ signal is low during the second half of a generical output channel slot time N if the channel N belongs to a conference in overflow, see Fig. 9.

This information can be used in the selection of the attenuation value, and the channel to be attenuated. If noise suppression is desired, four threshold are available.

When you insert in a channel belonging to some conference this function, all the PCM output bytes which are related to all the channels belonging to that conference and which are at a level less than the selected threshold, are converted into PCM bytes corresponding to the minimum level.

The four thresholds available correspond to the first, the ninth and the sixteenth step of the first segment, and the sixteenth step of the second segment.

These thresholds correspond respectively to 1/4096, 9/4096, 16/4096, 32/4096 respect to the full scale if A-law is selected and to 1/8159, 9/8159, 16/8159, 32/8159 respect to the full scale is MU-law is selected.

The instruction 5 (operating mode) allows the device M116 to be compatible with any kind of PCM byte format, see table 1, and to work also with PCM frames with Extra bit (ex. 193 bit/frame at 1544 Kbit/s).

The EC pin (External Clock) provides the output clock signal to be applied to the DSM (M088).

This signal is usually the same as the one applied to the input CLOCK pin, only with a little delay (40ns typ.).

When you select, by instructions 5, operating mode with Extra bit, the output clock signal at pin EC has two periods "frozen" in order to allow the DSM (M008) to work also with this king of PCM frame, see fig. 8.

The M116 can also operate in transparent mode. In this case a channel of PCM information can be sent through the M116 and it will appear at the output after one frame (and one channel) delay.

This is useful for a stand/alone system or if the attenuation and noise suppression features are desired without conference.

A tone can be outputted instead of PCM information by using the two tone programming pins (TD/TF).

This tone is a square wave with the same frequency of the signal applied to pin TF, a level corresponding to 1/10 of the full scale value and it is outputed only when pin TD = 1.

Only channels connected in a conference with insertion tone bit (IT) active will have the PCM coded tone at their output.

This feature allows the system to remind the users that they are in conference, or send information of a new party connection and so on.

The chip select pin ($\overline{CS}$) allows several M116 to be connected in parallel on the same databus and access only a particular one.

For testing and diagnostic purposes, a status instruction has been added that provides (for each channel requested) its conference location, the noise suppression threshold level and the attenuation value. This information will appear on the databus.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	4.75 to 5.25	V
V_I	Input Voltage	0 to 5.25	V
V_O	Off State Output Voltage	0 to 5.25	V
CLOCK Freq.	Input Clock Frequency	4.096	MHz
$\overline{SYNC}$ Freq.	Input Synchronization Frequency	8	KHz
T_{op}	Operating Temperature	0 to 70	°C

CAPACITANCES (measurements freq. = 1MHz ; T_{op} = 0 to 70°C ; unused pins tied to V_{SS})

Symbol	Parameter	Pins	Min.	Typ.	Max.	Unit
C_I	Input Capacitance	1 to 3 ; 15 to 20 ; 22 to 23			5	pF
$C_{I/O}$	I/O Capacitance	6 to 13			15	pF
C_O	Output Capacitance	4, 5, 21			10	pF

DC ELECTRICAL CHARACTERISTICS (T_{amb} = 0 to 70°C, V_{CC} = 5V ± 5%)

All DC characteristica are valid 250µs after V_{CC} and clock have been applied.

Symbol	Parameter	Pins	Test Conditions	Min.	Typ.	Max.	Unit
V_{IL}	Input Low Level	1 to 3 6 to 13 15 to 20 22 to 23		– 0.3		0.8	V
V_{IH}	Input High Level	1 to 3 6 to 13 15 to 20 22 to 23		2.0		V_{CC}	V
V_{OL}	Output Low Level	4, 6 to 13	I_{OL} = 1.8mA			0.4	V
V_{OH}	Output High Level	4, 6 to 13	I_{OH} = 250µA	2.4			V
V_{OL}	Output Low Level	5, 21	I_{OL} = 5.0mA			0.4	V
I_{IL}	Input Leakage Current	1 to 3 6 to 13 15 to 20 22 to 23	V_{IN} = 0 to V_{CC}			10	µA
I_{OL}	Data Bus Leakage Current	6 to 13	$\underline{V_{IN}}$ = 0 to V_{CC} $\overline{CS}$ = V_{CC}			± 10	µA
I_{CC}	Supply Current	14	Clock Freq. = 4.096MHz			150	mA

AC ELECTRICAL CHARACTERISTICS (T_{amb} = 0 to 70°C, V_{CC} = 5V ± 5%)
All AC characteristics are valid 250µs after V_{CC} and clock have been applied. C_L is the max. capacitive load and R_L the test pull up resistor.

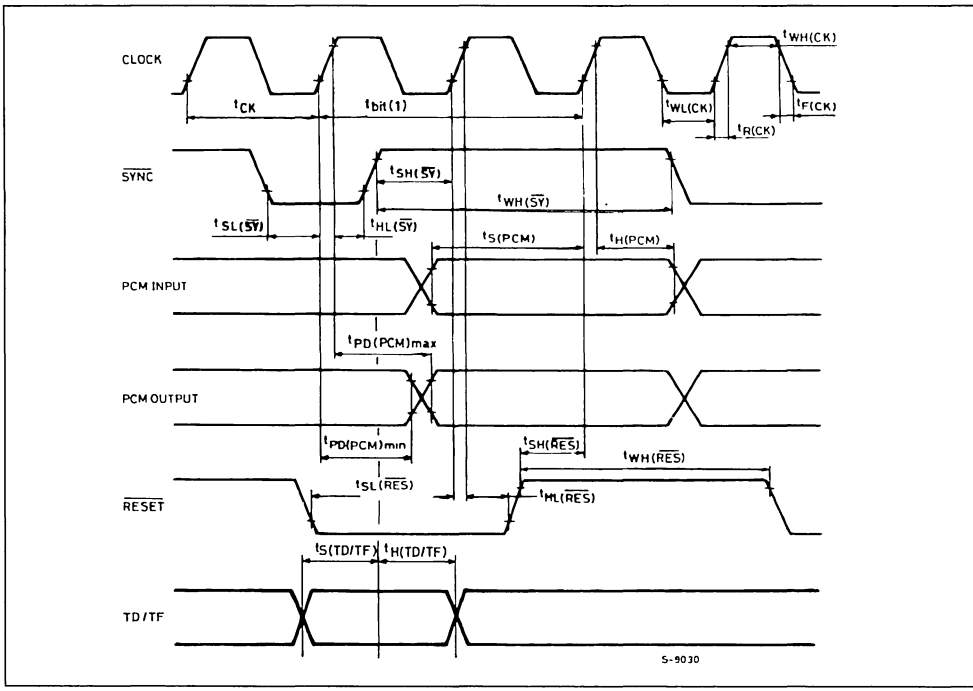
Signal	Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
CK (clock)	t_{CK}	Clock Period		230			ns
	t_{WL}	Clock Low Level Width		100			ns
	t_{WH}	Clock High Level Width		100			ns
	t_R	Rise Time				25	ns
	t_F	Fall Time				25	ns
$\overline{SYNC}$	t_{SL}	Low Level Set-up Time	See note 1	80			ns
	t_{HL}	Low Level Hold Time		40			ns
	t_{SH}	High Level Set-up Time		80			ns
	t_{WH}	High Level Width		t_{CK}			ns
PCM Input	t_S	Set-up Time		80			ns
	t_H	Hold Time		35			ns
PCM Output	$t_{PD\ min}$	Propagation time referred to CK low level.	C_L = 50pF R_L = 1KΩ	45			ns
	$t_{PD\ max}$	Propagation time referred to CK high level.	C_L = 50pF R_L = 1KΩ See note 2			180	ns
$\overline{RESET}$	t_{SL}	Low Level Set-up Time		100			ns
	t_{HL}	Low Level Hold Time		50			ns
	t_{SH}	High Level Set-up Time		90			ns
	t_{WH}	High Level Set-up Time		t_{CK}			ns
$\overline{WR}$	t_{WL}	Low Level Width		150			ns
	t_{WH}	High Level Width		200			ns
	t_{REP}	Repetition interval between active pulses.		500			ns
	t_{SH}	High level set-up time to active read strobe.		0			ns
	t_{HH}	High level hold time from active read strobe.		20			ns
	t_R	Rise Time				60	ns
	t_F	Fall Time				60	ns
$\overline{RD}$	t_{WL}	Low Level Width		180			ns
	t_{WH}	High Level Width		200			ns
	t_{REP}	Reception interval between active pulses.		500			ns
	t_{SH}	High level set-up time to active write strobe.		0			ns
	t_{HH}	High level hold time strobe.		20			ns
	t_R	Rise Time				60	ns
	t_F	Fall Time				60	ns

Notes : 1. With Extra Bit operating mode insert this time become 3 t_{CK}.
2. With Extra Bit operating mode insert these times are 80ns longer.

AC ELECTRICAL CHARACTERISTICS (continued)

Signal	Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$\overline{CS}$	$t_{SL(\overline{CS}\text{-}\overline{WR})}$	Low level set-up time to WR falling edge.	Active Case	0			ns
	$t_{HL(\overline{CS}\text{-}\overline{WR})}$	Low level hold time from WR rising edge.	Active Case	0			ns
	$t_{SH(\overline{CS}\text{-}\overline{WR})}$	High level set-up time to WR falling edge.	Inactive Case	0			ns
	$t_{HH(\overline{CS}\text{-}\overline{WR})}$	High level hold time from WR rising edge.	Inactive Case	0			ns
	$t_{SL(\overline{CS}\text{-}\overline{RD})}$	Low level set-up time to RD falling edge.	Active Case	0			ns
	$t_{HL(\overline{CS}\text{-}\overline{RD})}$	Low level hold time from RD rising edge.	Active Case	0			ns
	$t_{SH(\overline{CS}\text{-}\overline{RD})}$	High level set-up time to RD falling edge.	Inactive Case	0			ns
	$t_{HH(\overline{CS}\text{-}\overline{RD})}$	High level hold time from RD rising edge.	Inactive Case	0			ns
C/$\overline{D}$	$t_{S(C/\overline{D}\text{-}\overline{WR})}$	Set-up time to write strobe end.		130			ns
	$t_{H(C/\overline{D}\text{-}\overline{WR})}$	Hold time from write strobe end.		25			ns
	$t_{S(C/\overline{D}\text{-}\overline{RD})}$	Set-up time to read strobe start.		20			ns
	$t_{H(C/\overline{D}\text{-}\overline{RD})}$	Hold time from read strobe end.		25			ns
$\overline{OS}$	$t_{PD(\overline{OS})}$	Propagation time from rising edge of CK.	C_L = 50pF			100	ns
EC	$t_{PD(EC)}$	Propagation time referred to CK edges.	C_L = 50pF			80	ns
TD/TF	t_S	Set-up		80			ns
	t_H	Hold Time		40			ns
D0 to D7 (interface bus)	$t_{S(BUS\text{-}\overline{WR})}$	Input set-up time to write strobe end.		130			ns
	$t_{H(BUS\text{-}\overline{WR})}$	Input hold time from write strobe end.		25			ns
	$t_{PD(BUS)}$	Propagation time from (active) falling edge of read strobe.	C_L = 200pF			120	ns
	$t_{HZ(BUS)}$	Propagation time from (active) rising edge of read strobe to high impedance state.				80	ns

Figure 4 : $\overline{SYNC}$, PCM I/O, $\overline{RESET}$, TD/TF Timings.



(1) t_{bit} corresponds to bit 0, channel 0 or Extra Bit.

Figure 5 : WRITE Operating Timing.

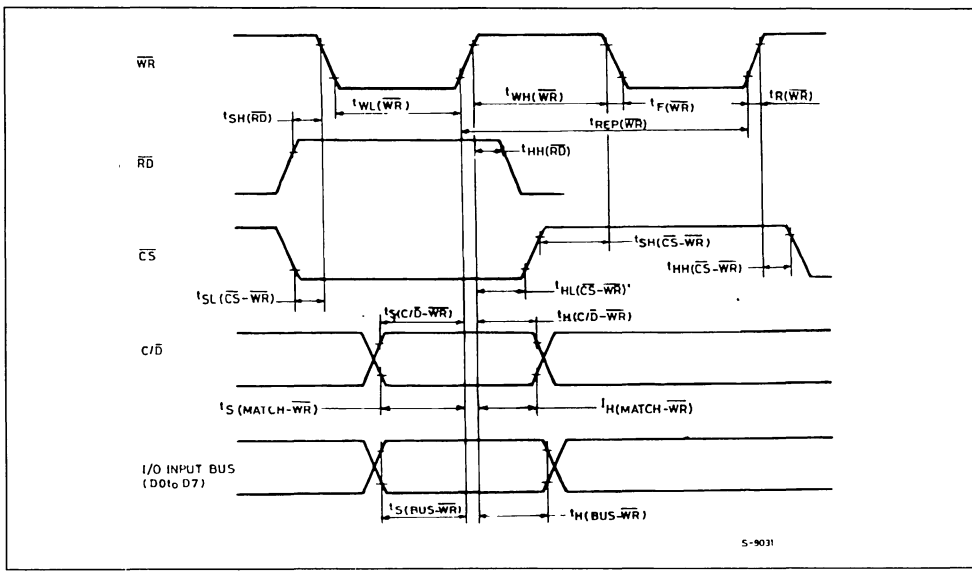


Figure 6 : READ Operating Timing.

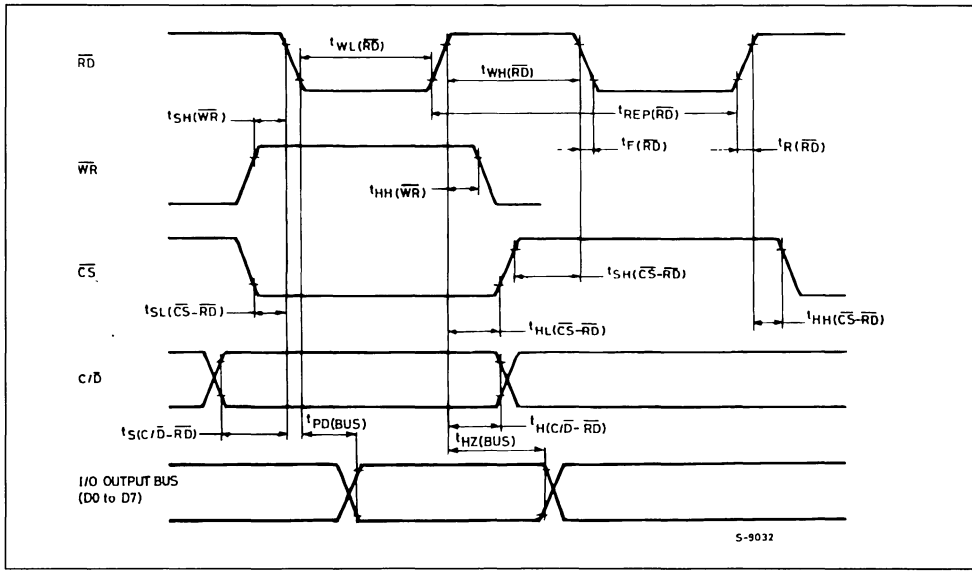


Figure 7 : EC (External Clock) and $\overline{OS}$ (Overflow Signalling) Timings.

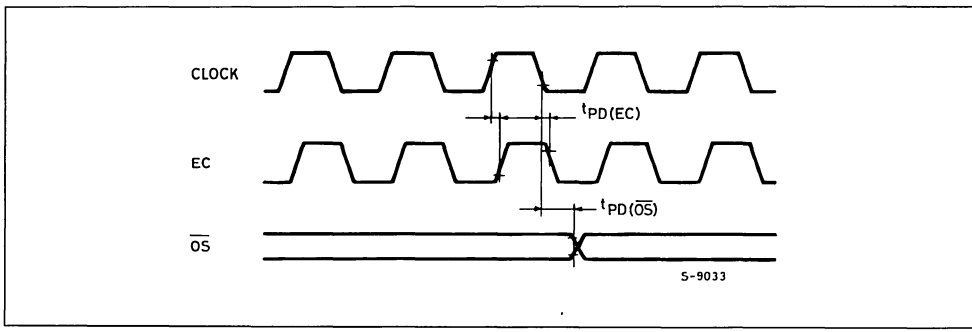


Figure 8 : EC Timing with Extra Bit Operating Mode Insert.

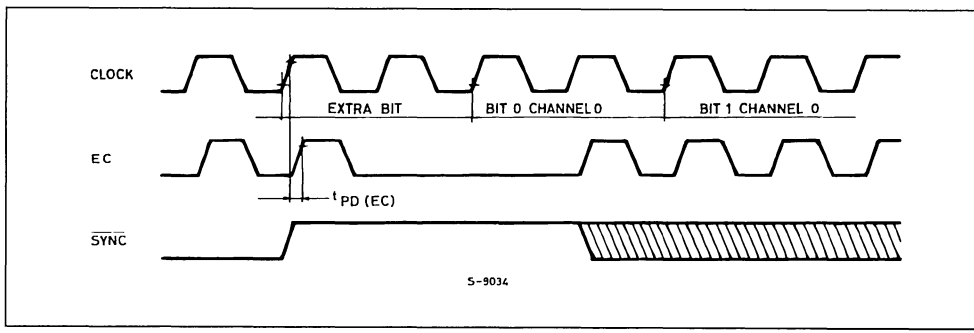


Figure 9 : $\overline{OS}$Timing with Output PCM Channel (n) belonging to a Conference in Overflow.

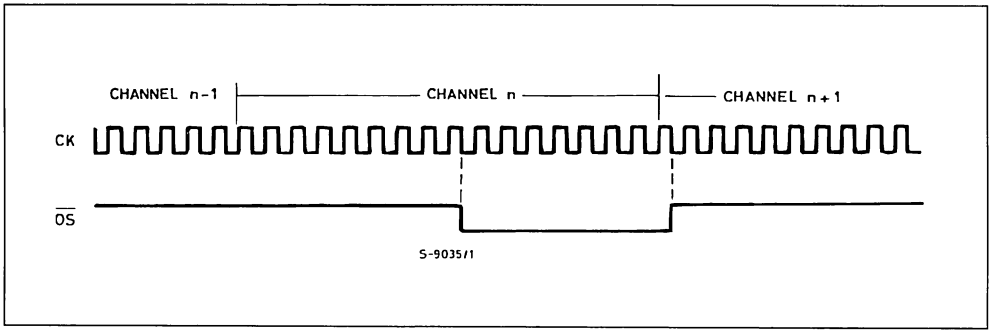
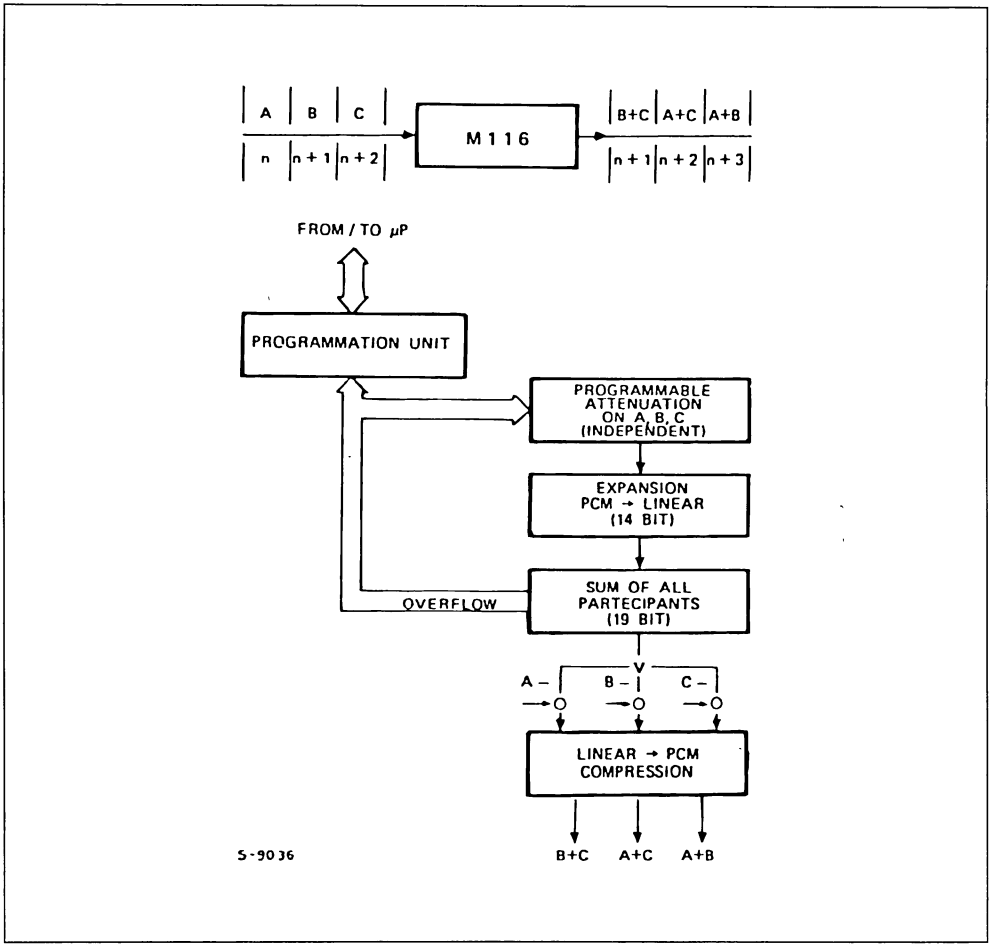


Figure 10 : Simplified Operating Procedures.



INSTRUCTION SET

INSTRUCTION 1 : CHANNEL CONNECTION IN CONFERENCE MODE

Three byte are needed :

1) The first byte contains the conference number (bits D0-D3) and the Start bit S (bit D4). When S = 1, all registers of the conference will be cleared. S = 1 is only required in the instruction 1 set of the first channel connected to a new conference.
2) The second byte contains in the bits (D0-D4) the number of the channel to be connected and the Insert Tone Enable bit IT (D5). When bit IT = 1 all the channels belonging to that conference are enabled using insert tone function if it's active (TD = 1).
3) The third byte contains information about the attenuation level and the noise suppression level to be applied to that channel and the opcode (0111).

Instruction 1 Format

Control Signal				Data Bus							
$\overline{CS}$	$\overline{RD}$	C/$\overline{D}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	X	X	X	S	P3	P2	P1	P0
0	1	0	0	X	X	IT	C4	C3	C2	C1	C0
0	1	1	0	A1	A0	T1	T0	0	1	1	1

S : Conference Start bit
P3 - P0 : Conference number (1-10)
IT : Insertion Tone function enable (IT = 1)
C4 - C0 : Channel number (0-31)
A1 - A0 : Channel attenuation
00 = – 0dB
01 = – 3dB
10 = – 6dB

T1 - T0 : Noise suppression decision value (referred to PCM coding, 128 + 128 steps)
00 = no noise suppression
01 = ninth step, first segment
10 = sixteenth step, first segment
11 = sixteenth step, second segment

INSTRUCTION 2 : CHANNEL CONNECTION IN TRANSPARENT MODE

Two bytes are needed :

1) The first byte contains the number of the channel.
2) The second byte contains information about the attenuation level and the noise suppression level to be applied to that channel and the opcode (0011).

PCM data of this channel is not added to any conference and it is transferred to the PCM output. It is not affected by the tone control pins.

Instruction 2 Format

Control Signal				Data Bus							
$\overline{CS}$	$\overline{RD}$	C/$\overline{D}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	X	X	X	C4	C3	C2	C1	C0
0	1	1	0	A1	A0	T1	T0	0	0	1	1

INSTRUCTION 3 : CHANNEL DISCONNECTION

Two bytes are needed :

1) The first word contains the number of the channel to be disconnected.
2) The second word contais the opcode (1111).

One time frame must exist between disconnection and connection of the same channel.

Instruction 3 Format

Control Signal				Data Bus							
$\overline{CS}$	$\overline{RD}$	C/$\overline{D}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	X	X	X	C4	C3	C2	C1	C0
0	1	1	0	X	X	X	X	1	1	1	1

INSTRUCTION SECTION (continued)

INSTRUCTION 4 : OVERFLOW INFORMATION

Two bytes are needed to know the status of all 10 conferences : C/$\overline{D}$ = 0 reads the first byte (first 8 conferences) and C/$\overline{D}$ = 1 reads the second byte (the last 2 conferences). A conference is in overflow when the corresponding bit is high.

Instruction 4 Format

Control Signal				Data Bus							
$\overline{CS}$	$\overline{RD}$	C/$\overline{D}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	CF8	CF7	CF6	CF5	CF4	CF3	CF2	CF1
0	0	1	1	X	X	X	X	X	X	CF10	CF9

CF10 – CF1 : Conference in overflow when high
nb : as long as $\overline{RD}$ remains low, the overflow status of the conference selected by C/$\overline{D}$ can be monitored in real time.

INSTRUCTION 5 : OPERATING MODE

The single byte needed contains the Extra bit E (D6), the format bits F1-F0 (D5-D4) and the opcode (0101).

The E bit must be E = 1 when the PCM frame contains a number of bit multiple of eight plus one bit (ex. PCM frame at 1544Kbit/s). Normally E = 0.

The bits F1-F0 select the kinds of PCM format byte according table 1. After Reset the default values correspond to F1 = 0, F0 = 1 if A-law is selected and F1 = 1, F0 = 1 if Mu-law is selected.

All channels must be disconnected when the Operating Mode Instruction is sent. They must remain disconnected for at least two time frames after the instruction was sent.

We recommende to use this instruction right after the RESET (see pin $\overline{RESET}$ description).

Instruction 5 Format

Control Signal				Data Bus							
$\overline{CS}$	$\overline{RD}$	C/$\overline{D}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	0	X	E	F1	F0	0	1	0	1

E : Extra bit insertion (active when E = 1)
F1 - F0 : PCM byte Format selection (see also table 1)
00 = no bit inverted
01 = even bit (B0-B2-B4-B6) inverted
10 = odd bit (B1-B3-B5) inverted
11 = all bit (B0-B1-B2-B3-B4-B5-B6) inverted

INSTRUCTION 6 : STATUS

Three bytes are needed :

1) The first byte contains the number of the channel ;

2) The second byte contains the opcode (0110) ;

3) By a reading cycle you extract from the third byte the information about the operating mode of the channel (no connection or transparent mode or number of the conference, bits D4-D7) ; the attenuation (D2-D3) and noise suppression values (D0-D1) eventually inserted.

This reading cycle must be executed at least one frame after the end of the opcode writing cycle.

Instruction 6 Format

Control Signal				Data Bus							
$\overline{CS}$	$\overline{RD}$	C/$\overline{D}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	X	X	X	C4	C3	C2	C1	C0
0	1	1	0	X	X	X	X	0	1	1	0
0	0	1	1	P3	P2	P1	P0	A1	A0	T1	T0

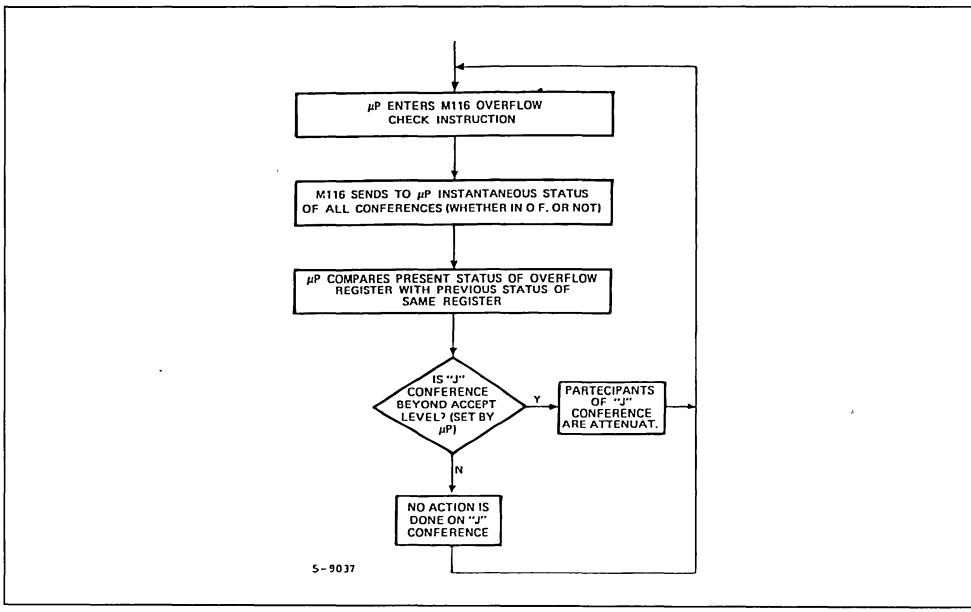
P3 - P0 : channel mode operation information
0000 = no connection
1111 = transparent mode
1010 - 0001 = conference mode,
P3-P0 give the number of the conference

nb : the Instruction 6 enables the data bus to read the status until reset by C/$\overline{D}$ = 0 and $\overline{WR}$ = 1.

Table 1 : PCM Byte Format. B7 (sign-bit) is the MSB and B0 is the LSB. F1-F0 corresponds to D5-D4 in the byte of the Operating Mode Instruction (instruction 5).

F1	F0		B7	B6	B5	B4	B3	B2	B1	B0
0	0	+ FULL SCALE	1	1	1	1	1	1	1	1
		MIN LEVELS	1	0	0	0	0	0	0	0
			0	0	0	0	0	0	0	0
		– FULL SCALE	0	1	1	1	1	1	1	1
0	1	+ FULL SCALE	1	0	1	0	1	0	1	0
		MIN LEVELS	1	1	0	1	0	1	0	1
			0	1	0	1	0	1	0	1
		– FULL SCALE	0	0	1	0	1	0	1	0
1	0	+ FULL SCALE	1	1	0	1	0	1	0	1
		MIN LEVELS	1	0	1	0	1	0	1	0
			0	0	1	0	1	0	1	0
		– FULL SCALE	0	1	0	1	0	1	0	1
1	1	+ FULL SCALE	1	0	0	0	0	0	0	0
		MIN LEVELS	1	1	1	1	1	1	1	1
			0	1	1	1	1	1	1	1
		– FULL SCALE	0	0	0	0	0	0	0	0

Figure 11 : Overflow Control with µP Interactive Procedure.



SUPPORT MATERIAL AVAILABLE

A) DEMONSTRATION BOARD : Developed to introduce users to the use of the M088 and M116, without building any external hardware but using mnemonic and easy commands through a standard asynchronous terminal. (order code : DEMOCONF).

B) TECHNICAL NOTE : AN177 and AN299.

SINGLE POLE HIGH-VOLTAGE SOLID-STATE RELAY

AN AT &T PRODUCT

- HIGH VOLTAGE IC FABRICATED IN A DIELECTRIC ISOLATION PROCESS
- OPTICAL COUPLING BETWEEN INPUT AND OUTPUT
- CAN SWITCH LOADS UP TO 350V AT CURRENTS UP TO 100mA
- LOW ON-RESISTANCE
- CLEAN, BOUNCE-FREE SWITCHING
- HIGH CURRENT SURGE CAPABILITY
- LOW-POWER CONSUMPTION
- NO ELECTROMAGNETIC INTERFERENCE

DIP6
(Plastic Package)

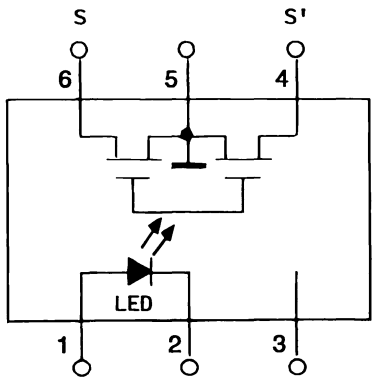
ORDER CODE : LH1056AT

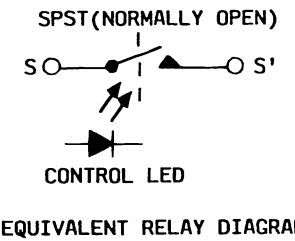
DESCRIPTION

The LH1056 (Multipurpose Solid-State Relay) is a low-cost, bi-directional, SPST designed to switch both AC and DC loads. Output is rated at 350 volts and can handle loads up to 100mA. It is packaged in a special 6-pin plastic DIP.

Each device consists of one GaAlAs LED to optically couple the control signal to a high-voltage integrated circuit. The typical ON-Resistance is 30 ohms at 25mA, and is exceptionally linear up to 50mA. Beyond 50mA, the incremental resistance becomes even less, thereby minimizing internal power dissipation. The LH1056 also has internal current limiting which clamps the load current at 150mA to insure that the device will survive during current surges.

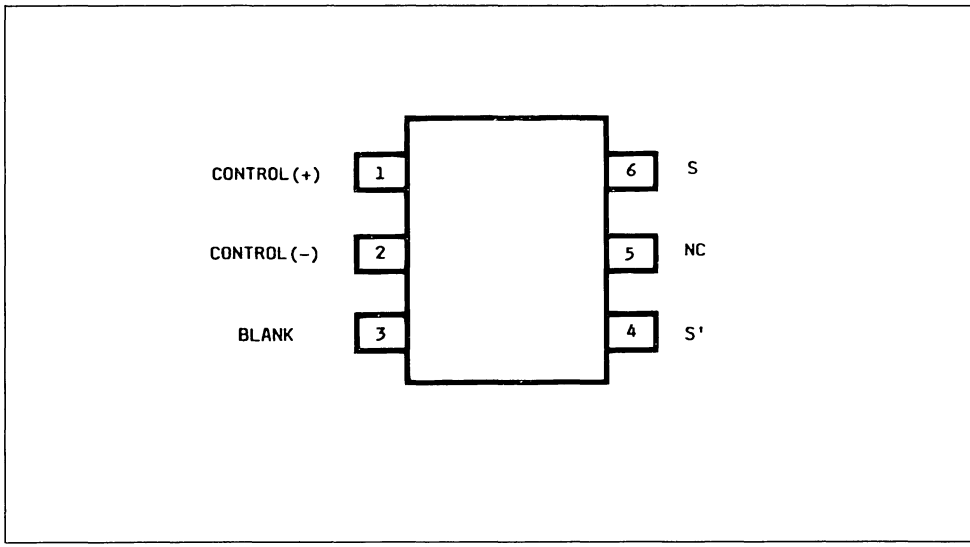
Figure 1 : Functional and Equivalent Relay Diagrams.





EQUIVALENT RELAY DIAGRAM

PIN CONNECTION (top view)



PIN DESCRIPTION

Name	Description
Control + Control –	These pins are the positive and negative inputs respectively to the input control LED. An appropriate amount of current through the LED will close the circuit path between S and S'.
S-S'	These pins are the outputs. The pin pair S-S' represents one normally open relay pole.
Blank	This pin may be used as a tie-point for external components. Voltage on this pin should not exceed 300V.
NC	This pin is connected to internal circuitry. It should not be used as a tie-point for external circuitry.

ABSOLUTE MAXIMUM RATINGS (at 25°C unless otherwise specified)

Parameter	Value	Unit
Ambient Operating Temperature Range	– 40 to + 85	°C
Storage Temperature Range	– 40 to + 100	°C
Pin Temperature (soldering time =15s)	300	°C
LED Input Ratings : Continuous Forward Current Reverse Voltage	20 10	mA V
Recommeded Maximum Output Operation : Operating Voltage Load Current	350 100	V mA

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied Exposure to absolute maximum rating conditions for extended periods may affect device reliability

ELECTRICAL CHARACTERISTICS (at 25°C unless otherwise noted)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
* LED Forward Current for Turn-on	I_{LOAD} = 100mA		1.5	2.5	mA
	I_{LOAD} = 80mA, 70°C		2.5	5.0	
LED ON Voltage	I_{LED} = 10mA	1.15	1.30	1.45	V
ON Resistance : $R_{ON} = V_M/25mA$	I_{LED} = 2.5mA ; I_{LOAD} = 25mA	20	30	50	Ω
Breakdown Voltage	I_{LED} = 0μA ; I_{LOAD} = 50μA	350	380		V
Output Off-state Leakage Current	100V, I_{LED} = 0μA		1.0	200	nA
	100V, I_{LED} = 200μA		0.1	2.0	μA
	300V, I_{LED} = 200μA		0.1	5.0	μA
Turn-on Time	R_{LOAD} = 10kΩ ; I_{LED} = 5mA		1.0	2.0	ms
Turn-off Time			0.5	2.0	
Feedthrough Capacitance, Pin 4 to 6 ($4V_{p-p}$, 1kHz)			24		pF

* Supply a minimum of 6mA LED current to insure proper operation over the full operating temperature range.

TEST CIRCUITS

Figure 2 : R_{ON}, ON Voltage and Breakdown Voltage.

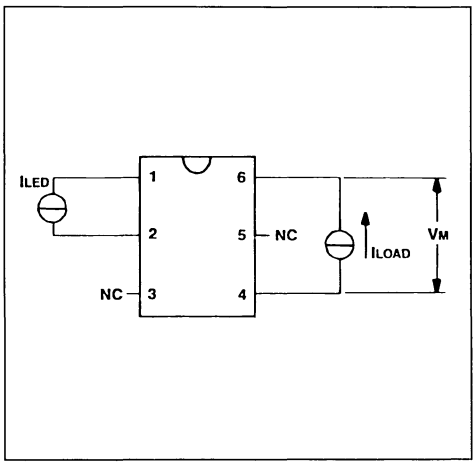


Figure 3 : Leakage Current.

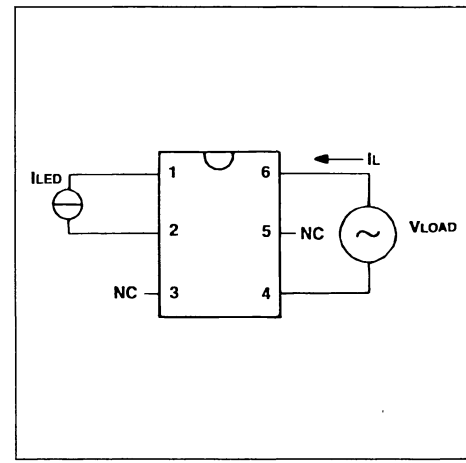
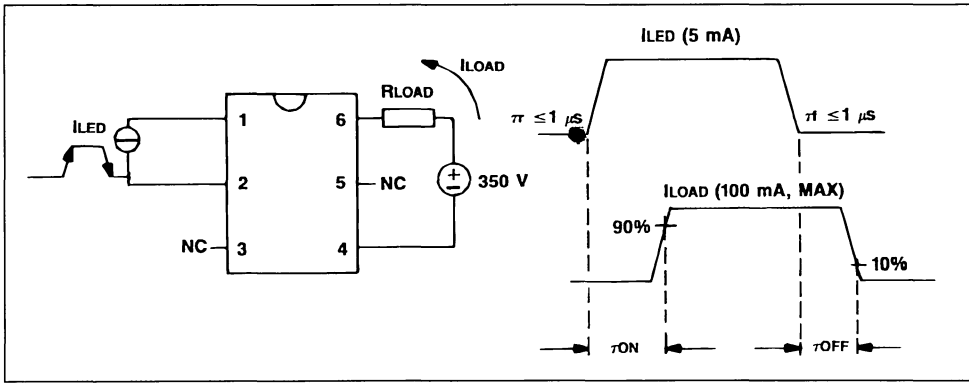


Figure 4 : τ_{ON}/τ_{OFF} Test Circuit and Waveform.



CHARACTERISTIC CURVES

Figure 5 : Solid-state Relay Typical ON Characteristics.

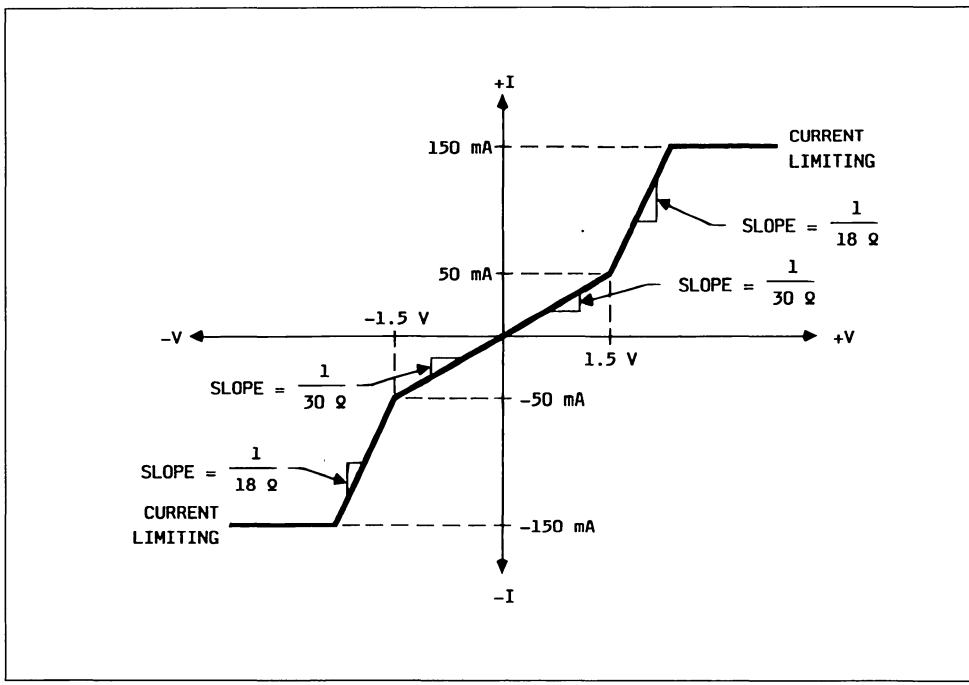


Figure 6 : Normalized Turn-on Time vs. Temperature.

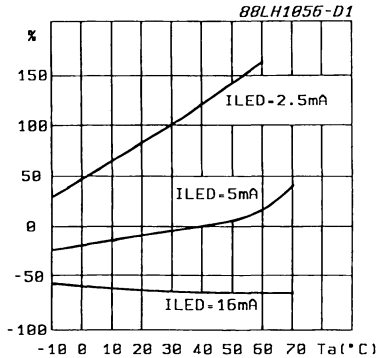


Figure 7 : Normalized Turn-off Time vs. Temperature.

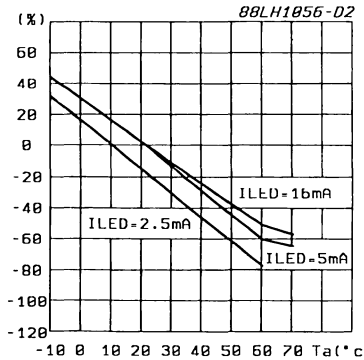


Figure 8 : Normalized Switching Time vs. Load Voltage.

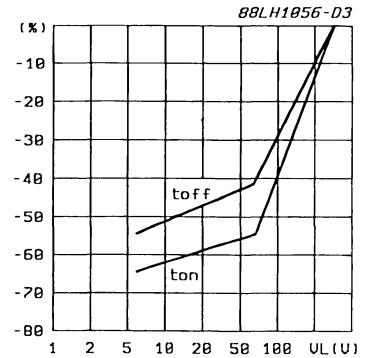


Figure 9 : Normalized On-resistance vs. Temperature.

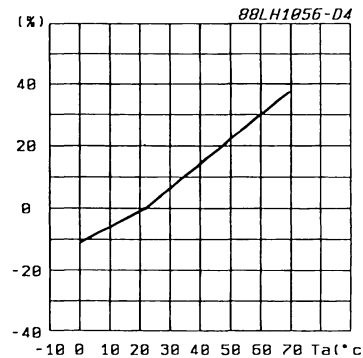


Figure 10 : Normalized Threshold Current vs. Temperature.

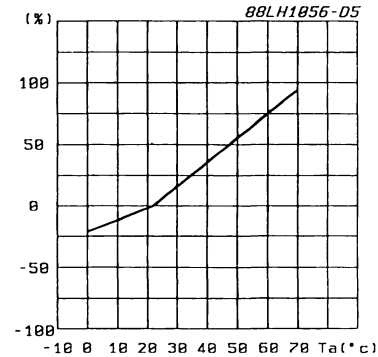
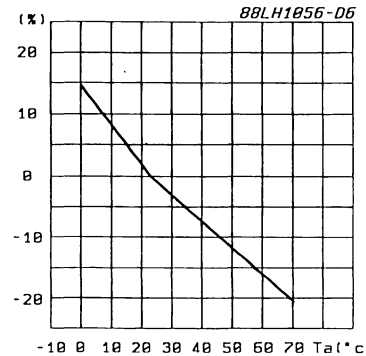


Figure 11 : Normalized Current Limit vs. Temperature.



INPUT/OUTPUT ISOLATION

The optical coupling between input and output provides a great degree of isolation between the low-voltage control and the high voltage output. Each device meets the 1500Vrms U/L (Underwriters Laboratories) test, which requires the product to withstand 1500Vrms for a time of one minute. For throughput purposes, U/L allows reduction of the test time to 1 second if the stress is increased to 1800Vrms.

In order to further assure long term reliability, each device is tested with an additional 600Vrms of guardband, bringing the total test stress to 2400Vrms for one second. During the test, less than 100nA of leakage is required. After passing this test, the part is subjected to the parameters specified by the data sheet.

LOAD PROTECTION

The LH1056 has been designed to protect the switching load by quick transient suppression and by output current limitation. These features can be illustrated by evaluation of the step response of the closed contact.

The circuit used for evaluation is shown in figure 12. First, a control signal is applied in order to activate the switch. Then transistor TR1 is turned on, which activates a 50V step through 100Ω across the closed switch. The switch reacts to the leading edge of the step by quickly deactivating, stopping current flow in the load. The resultant load current is shown in figure 13. After 250µs, the switch recloses, allowing current to flow in the load, up to the current limit of the device, if necessary. This clamping can be seen in figure 14 which also shows the fast shutoff at the leading edge of the step.

Figure 12 : Circuit used for Measurements of figures 13, 14.

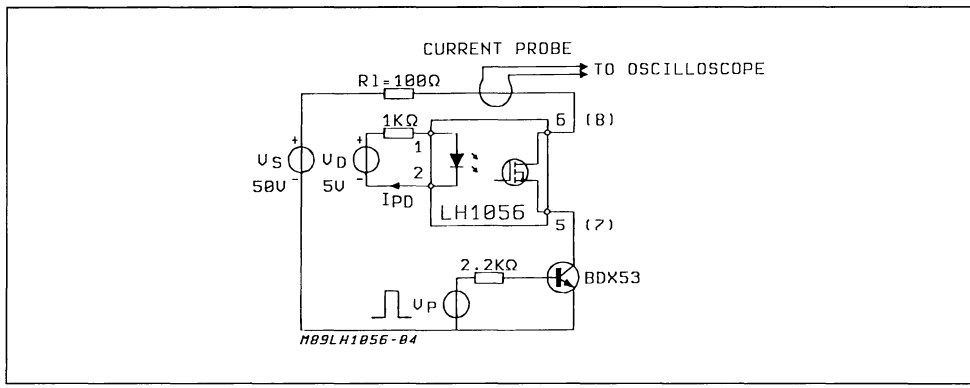


Figure 13 : Current Spike (R_L = 100Ω, V_S = 22V).
X = 0.5µs/div.
Y = 30mA/div.
Upper Trace : load current.
Lower Trace : command pulse.

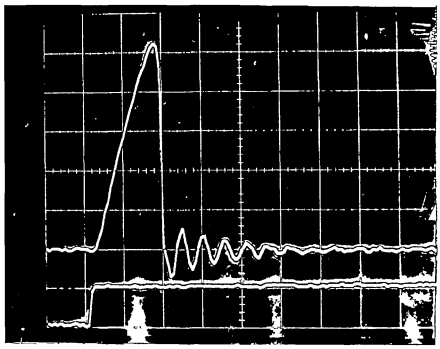
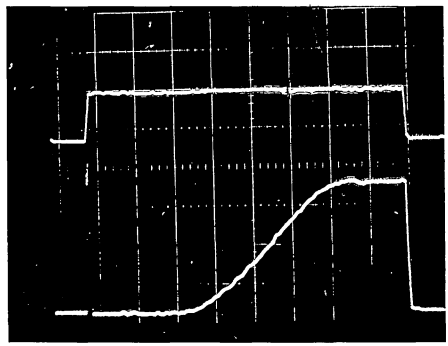


Figure 14 : Current limiting (V_S = 22V, R_L = 100Ω).
X = 0.2ms/div.
Y = 40mA/div.
Upper Trace : command pulse.
Lower Trace : load current.



APPLICATION

This device has been optimized to meet the demands of switching high voltages at moderate current levels in applications such as telecommunications, instrumentation, and medium-power switching. It is ideally suited for applications where high performance, noise-free switching of ac and dc signals is desirable.

The operational range of this device includes low-power commercial voltage applications where millampere control signals and low ON-resistance are required. The speed, reliability, and linearity of this switch makes it well suited for those applications which are beyond the range of mechanical relays, thyristors, and triacs. For lower ON resistance, higher voltages, or greater current capability, the LH1056 can be easily combined in parallel or series arrangements, as required, with their control LEDs simply driven in series.

The low ON-resistance and low-noise features are beneficial in instrumentation applications. The optical coupling provides isolation of the switch from the control signal in high-voltage and high-frequency applications.

The fabrication of high-voltage, monolithic ICs in a unique dielectric isolation process provides high reliability and the solid-state construction eliminates problems associated with mechanical relays such as sensitivity to shock and vibration.

Figure 15 : Triac Predriver.

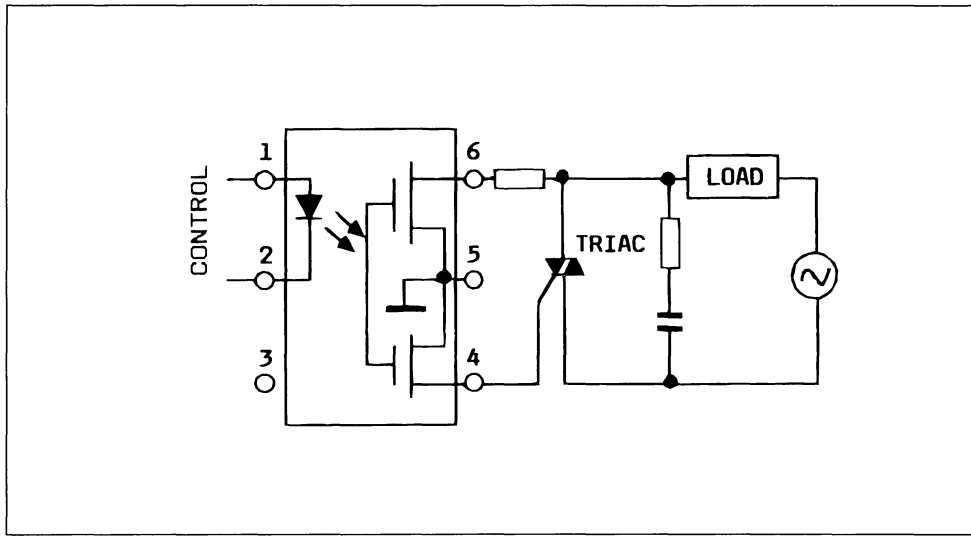
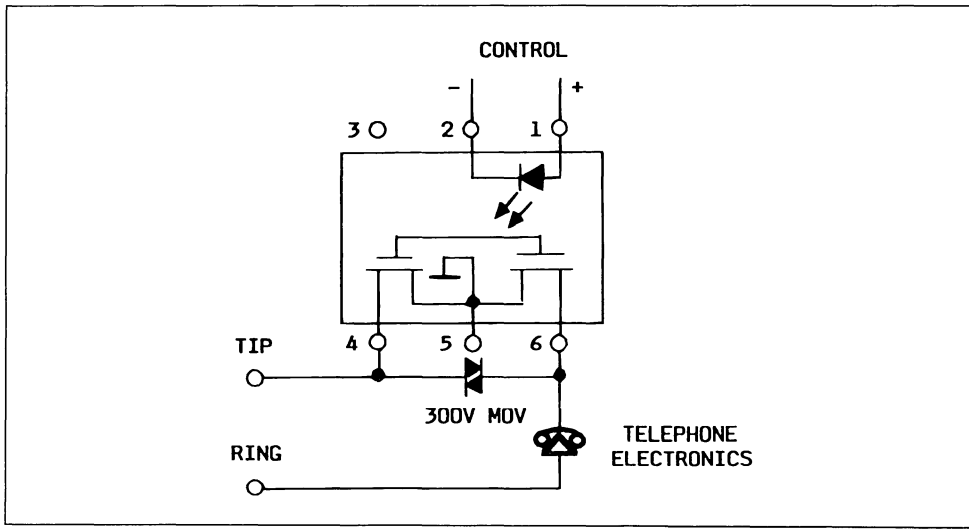


Figure 16 : Telephone Switchhook.



SGS-THOMSON MICROELECTRONICS

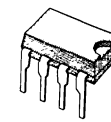
LH1061

DOUBLE POLE HIGH-VOLTAGE SOLID-STATE RELAY

ADVANCE DATA

AN AT & T PRODUCT

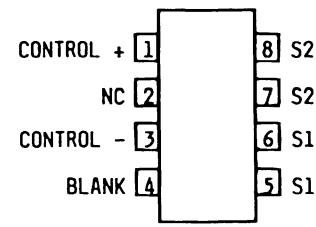
- HIGH VOLTAGE IC FABRICATED IN A DIELECTRIC ISOLATION PROCESS
- OPTICAL COUPLING BETWEEN INPUT AND OUTPUT
- CAN SWITCH TWO SEPARATE LOADS UP TO 200V EACH AT CURRENTS UP TO 200mA
- LOW ON-RESISTANCE
- CLEAN, BOUNCE-FREE SWITCHING
- HIGH CURRENT SURGE CAPABILITY
- LOW-POWER CONSUMPTION
- NO ELECTROMAGNETIC INTERFERENCE



Minidip

ORDER CODE : LH1061AB

PIN CONNECTION

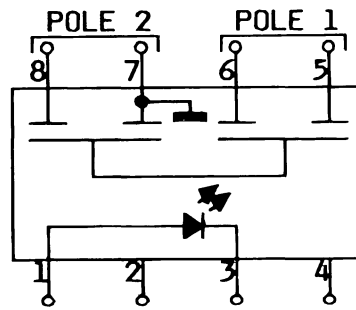


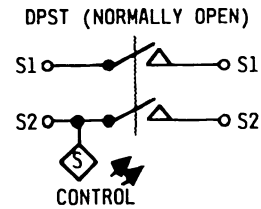
DESCRIPTION

The LH1061 (Multipurpose Solid-State Relay) is a low-cost, bi-directional, SPDT designed to switch both AC and DC loads. Outputs are rated at 200V and can handle contemporarily two loads up to 200mA. It is packaged in a special 8-pin plastic DIP.

Each device consists of one GaAlAs LED to optically couple the control signal to two high-voltage integrated switches. The typical ON-Resistance is 15Ω at 25mA, and is exceptionally linear up to 100mA. Beyond 100mA, the incremental resistance becomes even less, thereby minimizing internal power dissipation. The LH1061 also has internal current limiting which clamps the load current at 300mA to insure that the device will survive during current surges.

Figure 1 : Functional and Equivalent Diagram.





PIN DESCRIPTION

Name	Description
Control + Control –	These pins are the positive and negative inputs respectively to the input control LED. An appropriate amount of current through the LED will close the circuit path between S and S'.
S1, S1' S2, S2'	These pins are the outputs. The pins designated as S represents one side of a relay pole. The pins designated as S' are the complementary side of a relay pole. Note that S2 is connected to the substrate.
NC	This pin is connected internally for test purposes. It should NOT be used as a tie-point for external components.
Blank	This pin may be used as a tie point for external components. Voltage applied to this pin should no exceed 150V.

ABSOLUTE MAXIMUM RATINGS (at 25°C unless otherwise specified)

Parameter	Value	Unit
Ambient Operating Temperature Range	– 40 to + 85	°C
Storage Temperature Range	– 40 to + 100	°C
Pin Soldering Temperature (t = 15s max)	300	°C
LED INPUT : Continuous Forward Current Reverse Voltage	 20 10	 mA V
Operating Voltage	200	V
One Pole (S1, S1' or S2, S2')	300	mA
Each Pole (two poles operating simultaneously)	200	mA

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

ELECTRICAL CHARACTERISTICS (at 25°C unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
LED Forward Current for Turn-on*	I_{LOAD} = 200mA		1.5	2.5	mA
	I_{LOAD} = 160mA, 70°C		2.5	5.0	mA
LED ON Voltage @ 10mA	I_{LED} = 10mA	1.15	1.30	1.45	V
ON Resistance : $R_{ON} = V_M/50mA$	I_{LED} = 2.5mA ; I_{LOAD} = 50mA	8	12	15	Ω
ON Voltage	I_{LED} = 2.5mA ; I_{LOAD} = 200mA		2.0	2.5	V
Output Off-state Leakage Current	100V, I_{LED} = 0µA		1.0		nA
	100V, I_{LED} = 200µA		0.1	2.0	µA
Breakdown Voltage @ 50µA (figure 2)	I_{LED} = 0µA ; I_{LOAD} = 50µA	200	230		V
Turn-on Time	R_L = 15kΩ I_{LED} = 5mA		2.0		ms
Turn-off Time			1.0		
Feedthrough Capacitance, Pin 4 to 6 ($4V_{pp}$, 1kHz)			35		pF
Pole to pole Capacitance ($4V_{pp}$, 1kHz)			20		pF

* Supply a minimum of 6mA LED current to insure proper operation over the full operating temperature range

TEST CIRCUITS

Figure 2 : R_{ON}, ON Voltage and Breakdown Voltage.

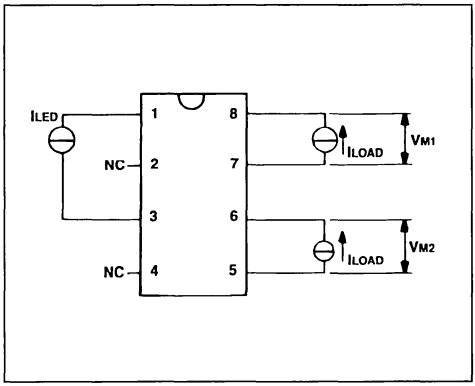


Figure 3 : Leakage Current.

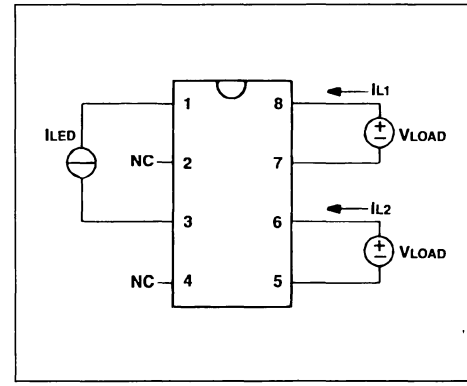
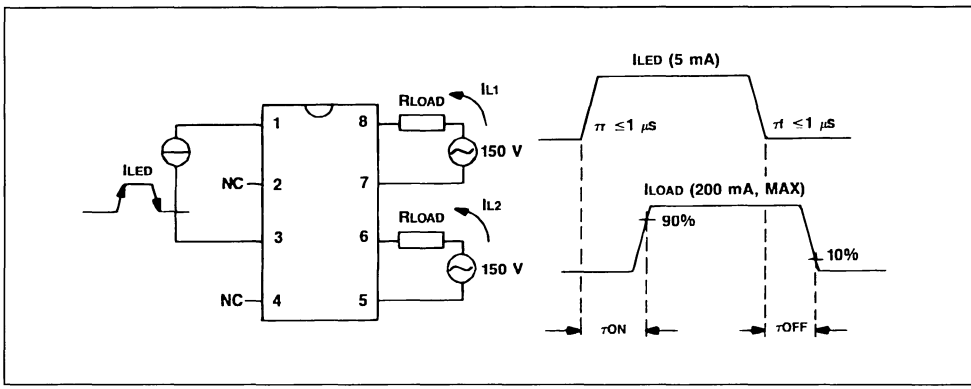


Figure 4 : τ_{ON}/τ_{OFF} Test Circuit and Waveform.



CHARACTERISTICS CURVES

Figure 5 : Solid-state Relay Typical ON Characteristics.

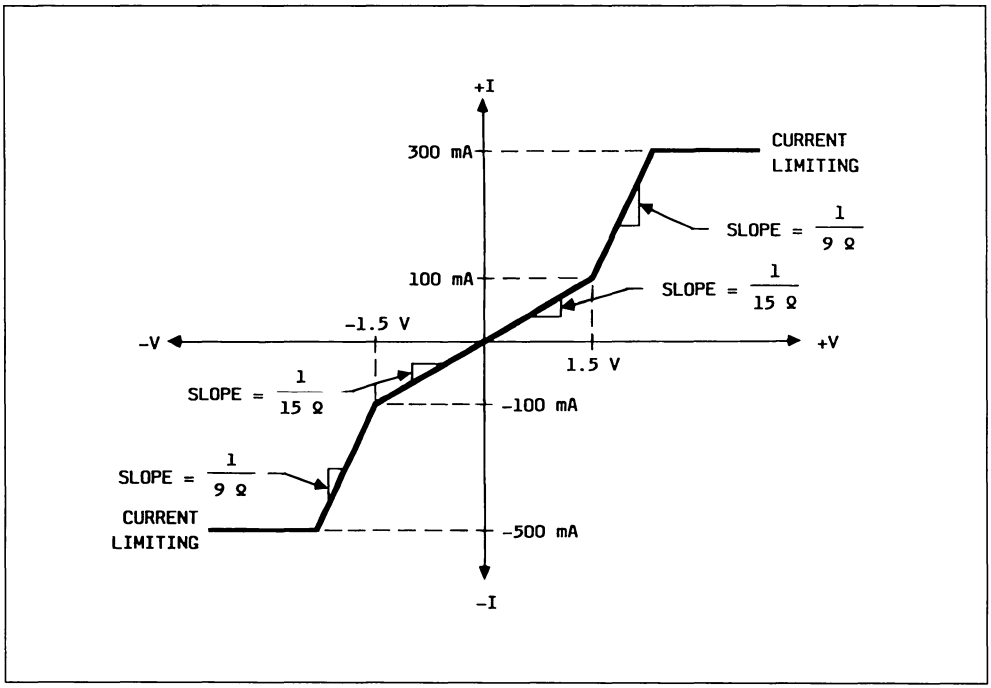


Figure 6 : Normalized Turn-on Time vs. Temperature.

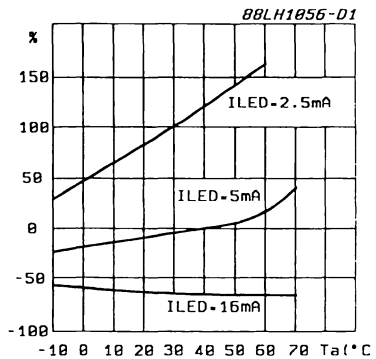


Figure 7 : Normalized Turn-off Time vs. Temperature.

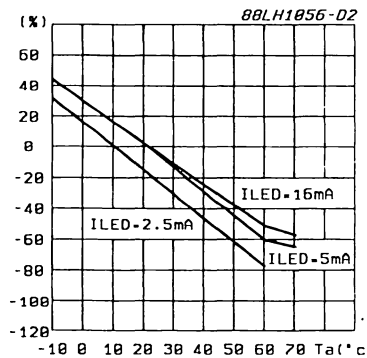


Figure 8 : Normalized Switching Time vs. Load Voltage.

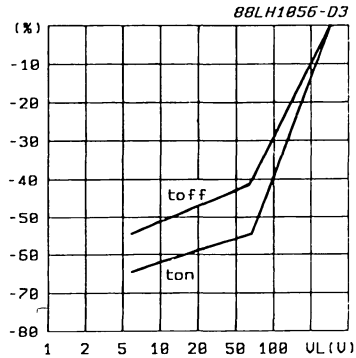


Figure 9 : Normalized On-resistance vs. Temperature.

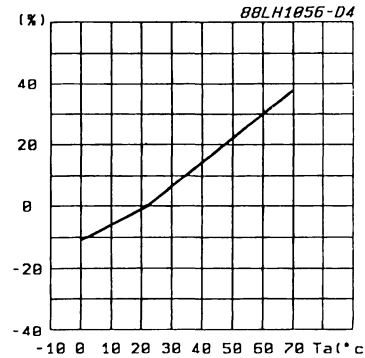


Figure 10 : Normalized Threshold Current vs. Temperature.

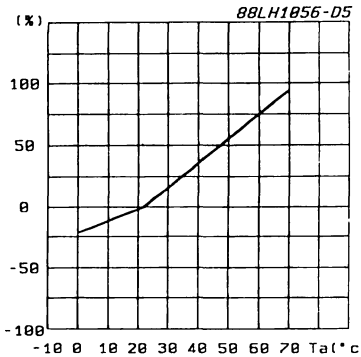


Figure 11 : Normalized Current Limit vs. Temperature.

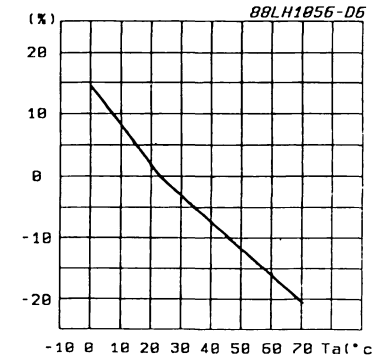


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Figure 12 : Circuit used for Measurements of figures 13, 14.

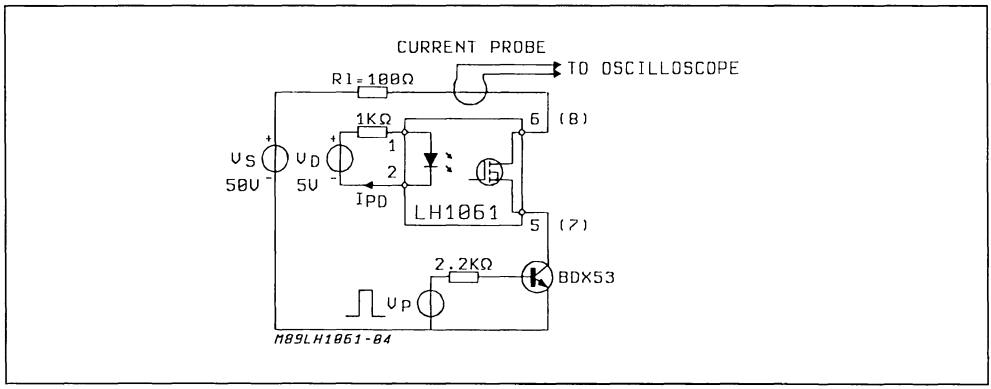


Figure 13 : Current spike (R_L = 100Ω, V_S = 50V).
X = 0.5µs/div.
Y = 60mA/div.
Upper Trace : load current.
Lower Trace : command pulse.

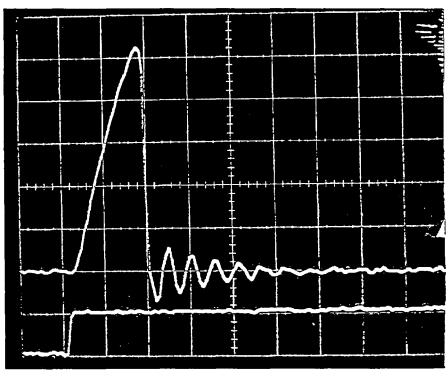
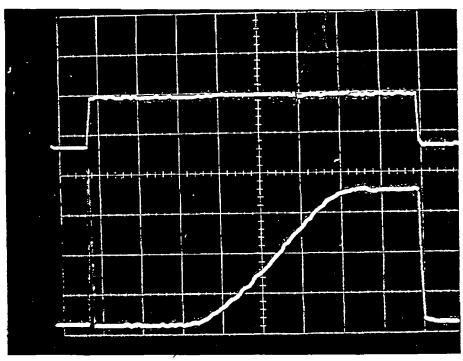


Figure 14 : Current limiting (V_S = 50V, R_L = 100Ω).
X = 0.2ms/div.
Y = 80mA/div.
Upper Trace : command pulse.
Lower Trace : load current.



APPLICATION

This device has been optimized to meet the demands of switching high voltages at moderate current levels in applications such as telecommunications, instrumentation, and medium-power switching. It is ideally suited for applications where high performance, noise-free switching of ac and dc signals is desirable.

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The fabrication of high-voltage, monolithic ICs in a unique dielectric isolation process provides high reliability and the solid-state construction eliminates problems associated with mechanical relays such as sensitivity to shock and vibration.

Figure 15 : Balanced Switchhook Application.

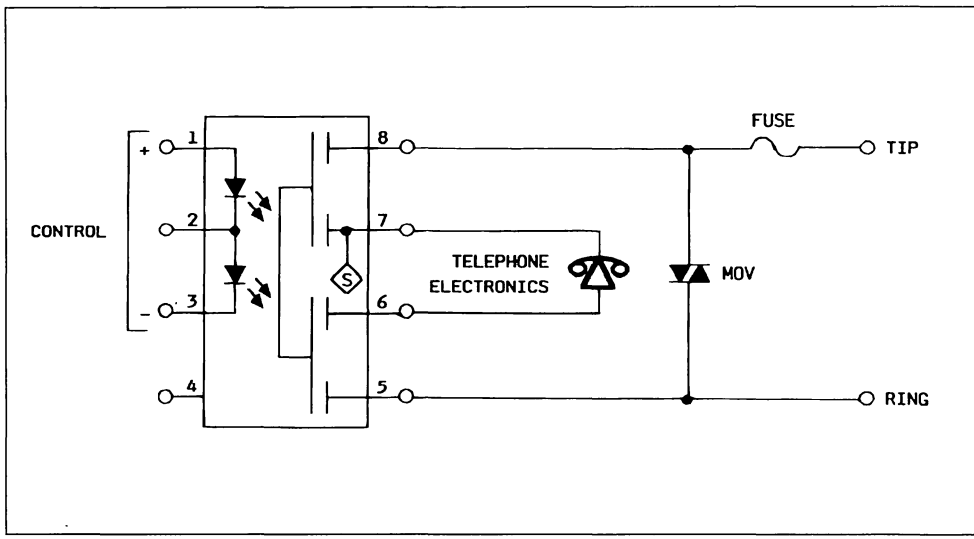
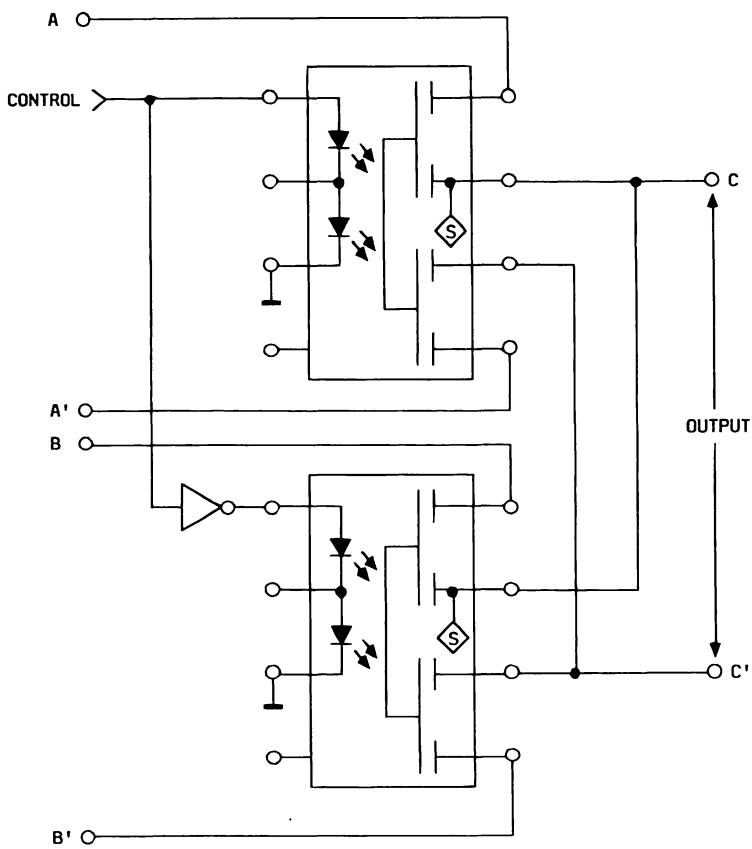
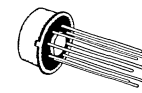


Figure 16 : Balanced Two-line Multiplexer Application.

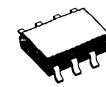


HIGH PERFORMANCE DUAL OPERATIONAL AMPLIFIER

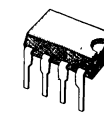
- SINGLE OR SPLIT SUPPLY OPERATION
- LOW POWER CONSUMPTION
- SHORT CIRCUIT PROTECTION
- LOW DISTORTION, LOW NOISE
- HIGH GAIN-BANDWIDTH PRODUCT
- HIGH CHANNEL SEPARATION



TO-99



SO-8J



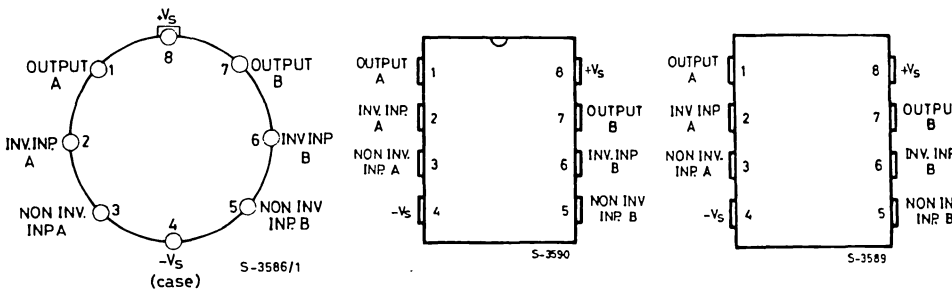
MINIDIP
(Plastic)

DESCRIPTION

The LS204 is a high performance dual operational amplifier with frequency and phase compensation built into the chip. The internal phase compensation allows stable operation as voltage follower in spite of its high gain-bandwidth products.

The circuit presents very stable electrical characteristics over the entire supply voltage range, and it particularly intended for professional and telecom applications (active filters, etc).

PIN CONNECTIONS (top views)

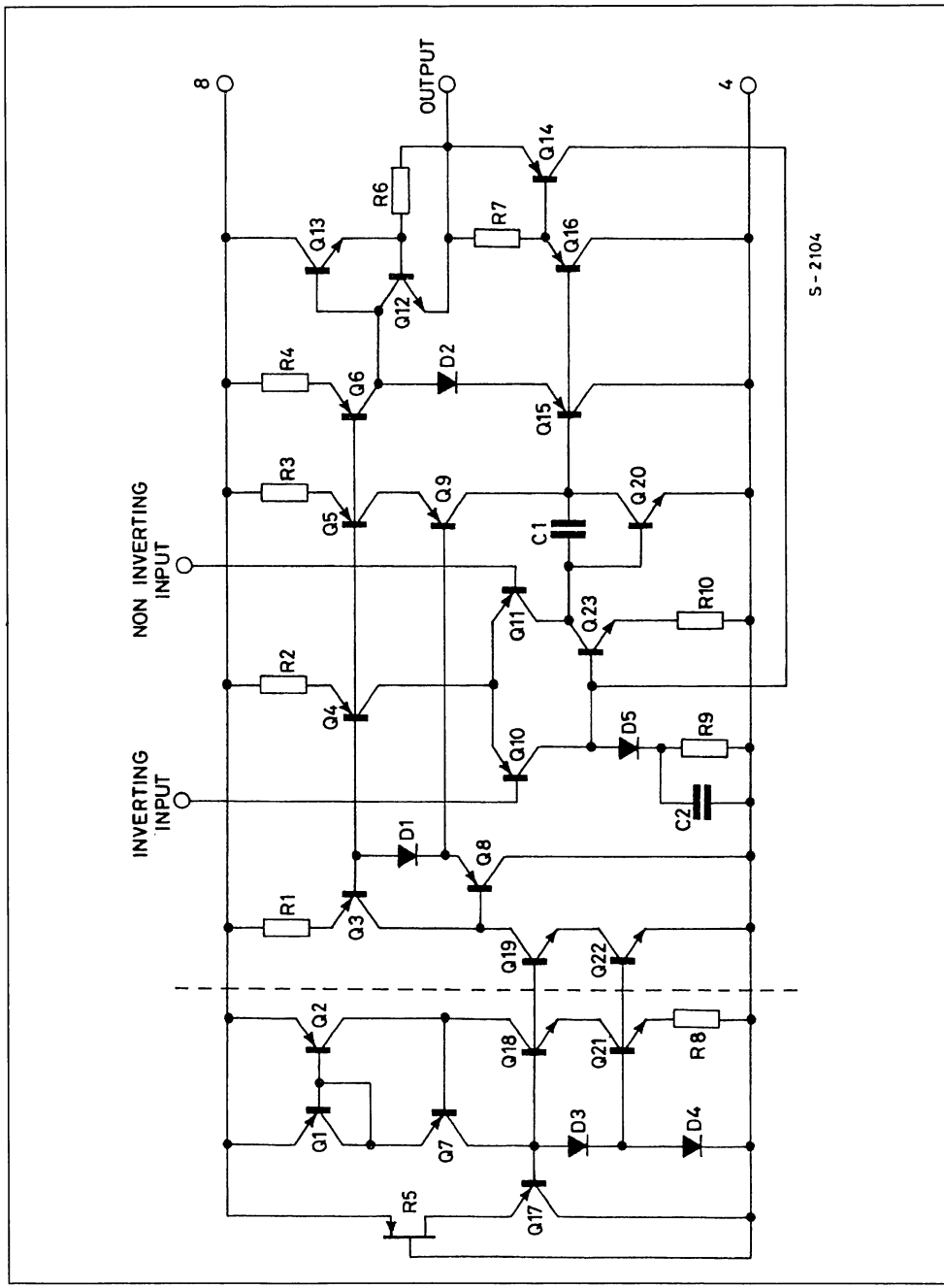


TO-99 Minidip SO-8

ORDER CODES

Type	TO-99	Minidip	SO-8
LS204	LS204TB	–	LS204M
LS204A	LS204ATB	–	–
LS204C	LS204CTB	LS204CB	LS204CM

SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		TO-99	Minidip	µPackage
V_s	Supply Voltage		± 18V		
V_i	Input Voltage		± V_s		
V_i	Differential Input Voltage		± (V_s – 1)		
T_{op}	Operating Temperature for	**LS204** **LS204A** **LS204C**	– 25 to 85°C – 55 to 125°C 0 to 70°C		
P_{tot}	Power Dissipation at T_{amb} = 70°C		520mW	665mW	400mW
T_j	Junction Temperature		150°C	150°C	150°C
T_{stg}	Storage Temperature		– 65 to 150°C	– 55 to 150°C	– 55 to 150°C

THERMAL DATA

			TO-99	Minidip	SO-8J
$R_{thj\text{-}amb}$	Thermal Resistance Junction-ambient	Max	155°C/W	120°C/W	200°C/W

ELECTRICAL CHARACTERISTICS (V_s = ± 15V, T_{amb} = 25°C, unless otherwise specified)

Symbol	Parameter	Test Conditions	LS204/LS204A			LS204C			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
I_s	Supply Current			0.7	1.2		0.8	1.5	mA
I_b	Input Bias Current			50	150		100	300	nA
		$T_{min} < T_{op} < T_{max}$			300			700	nA
R_i	Input Resistance	f = 1KHz		1			0.5		MΩ
V_{os}	Input Offset Voltage	$R_g \leq 10K\Omega$		0.5	2.5		0.5	3.5	mV
		$R_g \leq 10K\Omega$ $T_{min} < T_{op} < T_{max}$			3.5			5	mV
$\frac{\Delta V_{os}}{\Delta T}$	Input Offset Voltage Drift	$R_g = 10K\Omega$ $T_{min} < T_{op} < T_{max}$		5			5		µV/°C
I_{os}	Input Offset Current			5	20		12	50	nA
		$T_{min} < T_{op} < T_{max}$			40			100	nA
$\frac{\Delta I_{os}}{\Delta T}$	Input Offset Current Drift	$T_{min} < T_{op} < T_{max}$		0.08			0.1		nA/°C
I_{sc}	Output Short Circuit Current			23			23		mA
G_v	Large Signal Open Loop Voltage Gain	$T_{min} < T_{op} < T_{max}$ R_L = 2KΩ V_s = ± 15V V_s = ± 4V	90	100 95		86	100 95		dB
B	Gain-bandwidth Product	f = 20KHz	1.8	3		1.5	2.5		MHz
e_N	Total Input Noise Voltage	f = 1KHz R_g = 50Ω R_g = 1KΩ R_g = 10KΩ		8 10 18	15		10 12 20		nV/√Hz

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions	LS204/LS204A			LS204C			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
d	Distortion	G_V = 20dB R_L = 2KΩ V_o = 2 V_{PP} f = 1KHZ		0.03	0.1		0.03	0.1	%
V_o	DC Output Voltage Swing	R_L = 2KΩ V_s = ± 15V V_s = ± 4V	± 13	± 3		± 13	± 3		V
V_o	Large Signal Voltage Swing	R_L = 10KΩ f = 10KHz		28			28		V_{pp}
SR	Slew Rate	Unity Gain R_L = 2KΩ	0.8	1.5			1		V/µs
CMR	Common Mode Rejection	V_i = 10V $T_{min} < T_{op} < T_{max}$	90			86			dB
SVR	Supply Voltage Rejection	V_i = 1V f = 100Hz $T_{min} < T_{op} < T_{max}$	90			86			dB
CS	Channel Separation	f = 1KHz 100	120			120			dB

Note :

Temp.	LS204	LS204A	LS204C
T_{min}	– 25°C	– 55°C	0°C
T_{max}	+ 85°C	+ 125°C	+ 70°C

Figure 1: Supply Current vs. Supply Voltage.

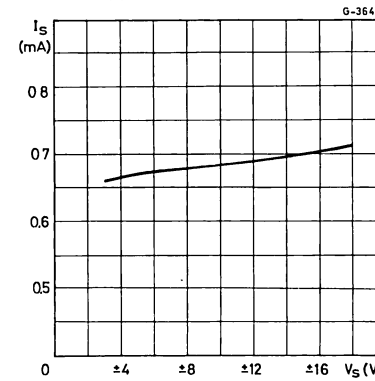


Figure 2 : Supply Current vs. Ambient Temperature.

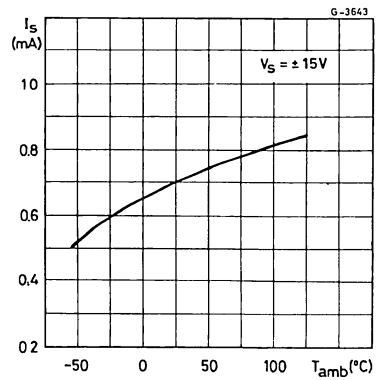


Figure 3 : Output Short Circuit Current vs. Ambient Temperature.

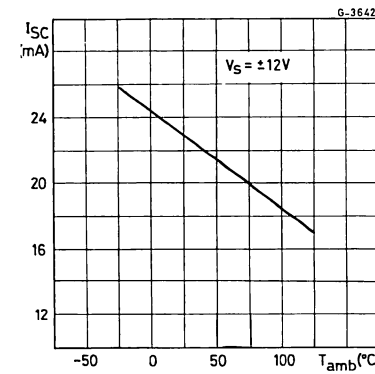


Figure 4: Open Loop Frequency and Phase Response.

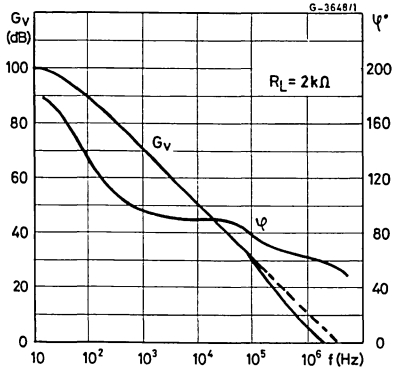


Figure 5: Open Loop Gain vs. Ambient Temperature.

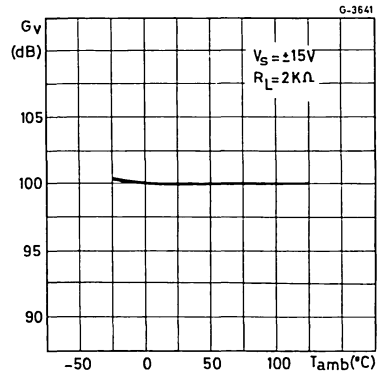


Figure 6 : Supply Voltage Rejection vs. Frequency.

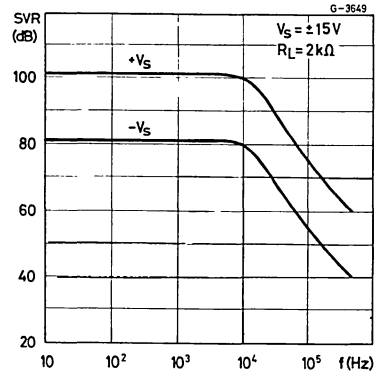


Figure 7 : Large Signal Frequency Response.

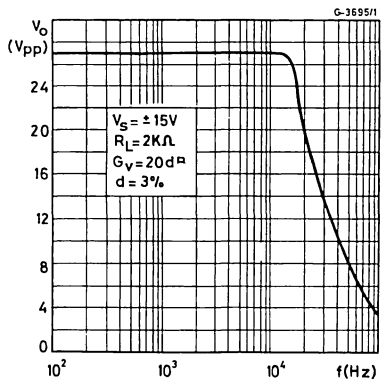


Figure 8 : Output Voltage Swing vs. Load Resistance.

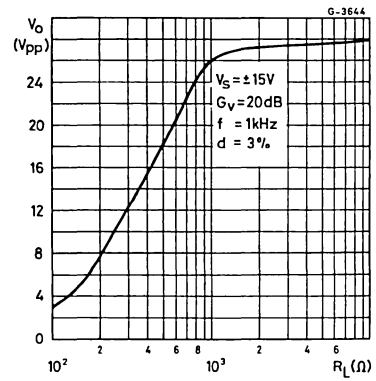
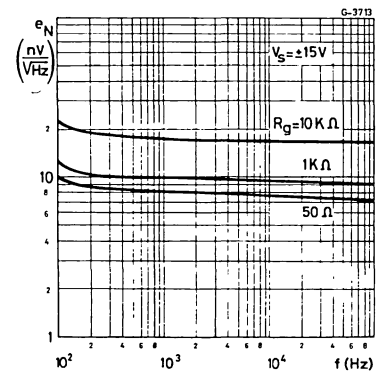


Figure 9 : Total Input Noise vs. Frequency.



APPLICATION INFORMATION

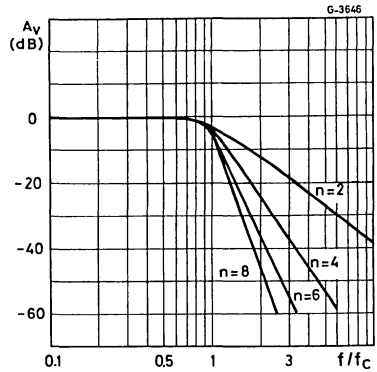
Active low-pass filter :

BUTTERWORTH

The Butterworth is a "maximally flat" amplitude response filter. Butterworth filters are used for filtering signals in data acquisition systems to prevent aliasing errors in sampled-data applications and for general purpose low-pass filtering.
The cutoff frequency, f_c, is the frequency at which the amplitude response is down 3 dB. The attenuation rate beyond the cutoff frequency is n6 dB per octave of frequency where n is the order (number of poles) of the filter.
Other characteristics :

- Flattest possible amplitude response.
- Excellent gain accuracy at low frequency end of passband.

Figure 10 : Amplitude Response.



BESSEL

The Bessel is a type of "linear phase" filter. Because of their linear phase characteristics, these filters approximate a constant time delay over a limited frequency range. Bessel filters pass transient waveforms with a minimum of distortion. They are also used to provide time delays for low pass filtering of modulated waveforms and as a "running average" type filter.

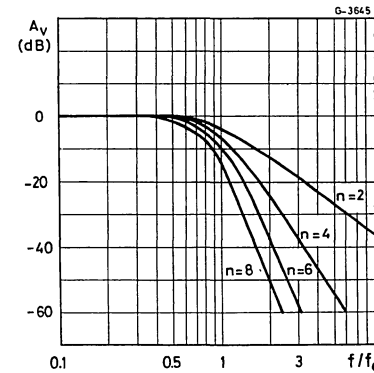
The maximum phase shift is $\frac{-n\pi}{2}$ radians where n is the order (number of poles) of the filter. The cutoff frequency, fc, is defined as the frequency at which the phase shift is one half of this value. For accurate delay, the cutoff frequency should be twice the maximum signal frequency. The following table can be used to obtain the – 3dB frequency of the filter

	2 pole	4 Pole	6 Pole	8 Pole
– 3dB Frequency	0.77 f_c	0.67 f_c	0.57 f_c	0.50 f_c

Other characteristics :

- Selectivity not as great as Chebyschev or Butterworth.
- Very little overshoot response to step inputs.
- Fast rise time.

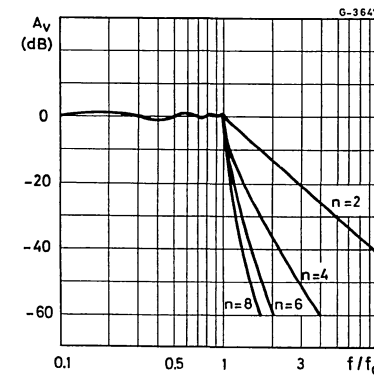
Figure 11 : Amplitude Response.



CHEBYSCHEV

Chebyschev filters have greater selectivity than either Bessel or Butterworth at the expense of ripple in the passband.

Figure 12 : Amplitude Response (± 1dB ripple).



APPLICATION INFORMATION (continued)

Chebyschev filters are normally designed with peak-to-peak ripple values from 0.2 dB to 2 dB.

Increased ripple in the passband allows increased attenuation above the cutoff frequency.
The cutoff frequency is defined as the frequency at which the amplitude response passes through the specified maximum ripple band and enters the stop band.

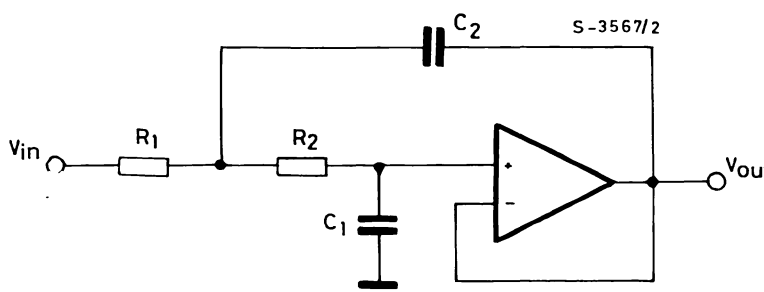
Other characteristics :
- Greater selectivity
- Very nonlinear phase response
- High overshoot response to step inputs

The table below shows the typical overshoot and settling time response of the low pass filters to a step input.

	Number of Poles	Peak Overshoot	Settling Time (% of final value)		
		% Overshoot	± 1%	± 0 .1%	± 0.01%
Butterworth	2	4	$1.1/f_c$sec.	$1.7/f_c$sec.	$1.9/f_c$sec.
	4	11	$1.7/f_c$	$2.8/f_c$	$3.8/f_c$
	6	14	$2.4/f_c$	$3.9/f_c$	$5.0/f_c$
	8	16	$3.1/f_c$	$5.1/f_c$	$7.1/f_c$
Bessel	2	0.4	$0.8/f_c$	$1.4/f_c$	$1.7/f_c$
	4	0.8	$1.0/f_c$	$1.8/f_c$	$2.4/f_c$
	6	0.6	$1.3/f_c$	$2.1/f_c$	$2.7/f_c$
	8	0.3	$1.6/f_c$	$2.3/f_c$	$3.2/f_c$
Chebyschev (ripple ± 0.25dB)	2	11	$1.1/f_c$	$1.6/f_c$	–
	4	18	$3.0/f_c$	$5.4/f_c$	–
	6	21	$5.9/f_c$	$10.4/f_c$	–
	8	23	$8.4/f_c$	$16.4/f_c$	–
Chebyschev (ripple ± 1dB)	2	21	$1.6/f_c$	$2.7/f_c$	–
	4	28	$4.8/f_c$	$8.4/f_c$	–
	6	32	$8.2/f_c$	$16.3/f_c$	–
	8	34	$11.6/f_c$	$24.8/f_c$	–

Design of 2nd order active low pass filter (Sallen and Key configuration unity gain-op-amp).

Figure 13 : Filter Configuration.



$$\frac{V_o}{V_i} = \frac{1}{1 + 2\xi \frac{S}{\omega c} + \frac{S^2}{\omega c^2}}$$

Where :

$\omega c = 2\pi f_c$ with f_c = cutoff frequency

ξ = damping factor.

APPLICATION INFORMATION (continued)

Three parameters are needed to characterise the frequency and phase response of a 2nd order active filter : the gain (G_V), the damping factor (ξ) or the Q-factor ($Q = (2\xi)^{-1}$), and the cutoff frequency (f_c).

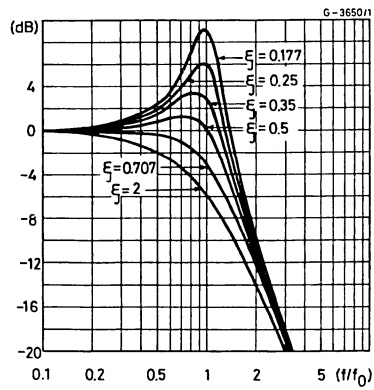
The higher order responses are obtained wit a series of 2nd order sections. A simple RC section is introduced when an odd filter is required.

The choice of 'ξ' (or Q-factor) determines the filter response (see table).

Table 1.

Filter Response	ξ	Q	Cutoff Frequency f_c
Bessel	$\frac{\sqrt{3}}{2}$	$\frac{1}{\sqrt{3}}$	Frequency at which Phase Shift is – 90°C
Butterworth	$\frac{\sqrt{2}}{2}$	$\frac{1}{\sqrt{2}}$	Frequency at Which $G_v = -3$dB
Chebyschev	$< \frac{\sqrt{2}}{2}$	$> \frac{1}{\sqrt{2}}$	Frequency at which the amplitude response passes through specified max. ripple band and enters the stop band.

Figure 14 : Filter Response vs. Damping Factor.



Fixed R = R1 = R2, we have (see fig. 13)

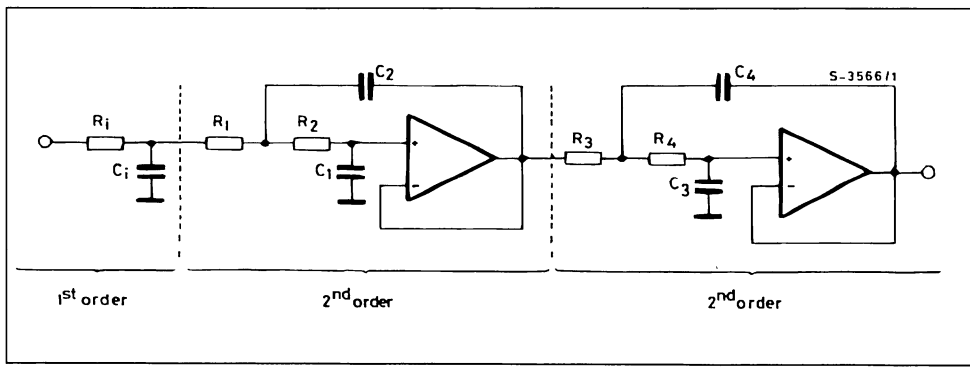
$$C_1 = \frac{1}{R} \quad \frac{\xi}{\omega_c}$$

$$C_2 = \frac{1}{R} \quad \frac{1}{\xi\omega_c}$$

The diagram of fig.14 shows the amplitude response for different values of damping factor ξ in

EXAMPLE

Figure 15 : 5th Order Low Pass Filter (Butterworth) with Unity Gain Configuration.



APPLICATION INFORMATION (continued)

In the circuit of fig. 15, for f_c = 3.4 KHz and $R_I = R_1 = R_2 = R_3 = R_4$ =10 KΩ, we obtain :

$$C_I = 1.354 \cdot \frac{1}{R} \cdot \frac{1}{2\pi f_c} = 6.33nF$$

$$C_1 = 0.421 \cdot \frac{1}{R} \cdot \frac{1}{2\pi f_c} = 1.97nF$$

$$C_2 = 1.753 \cdot \frac{1}{R} \cdot \frac{1}{2\pi f_c} = 8.20nF$$

$$C_3 = 0.309 \cdot \frac{1}{R} \cdot \frac{1}{2\pi f_c} = 1.45nF$$

$$C_4 = 3.325 \cdot \frac{1}{R} \cdot \frac{1}{2\pi f_c} = 15.14nF$$

The attenuation of the filter is 30 dB at 6.8 KHz and better than 60 dB at 15 KHz.

The same method, referring to Tab. II and fig. 16, is used to design high-pass filter. In this case the damping factor is found by taking the reciprocal of the numbers in Tab. II. For f_c = 5 KHz and $C_i = C_1 = C_2 = C_3 = C_4$ = 1 nF we obtain :

$$R_i = \frac{1}{1.354} \cdot \frac{1}{C} \cdot \frac{1}{2\pi f_c} = 23.5K\Omega$$

$$R_1 = \frac{1}{0.421} \cdot \frac{1}{C} \cdot \frac{1}{2\pi f_c} = 75.6K\Omega$$

$$R_2 = \frac{1}{1.753} \cdot \frac{1}{C} \cdot \frac{1}{2\pi f_c} = 18.2K\Omega$$

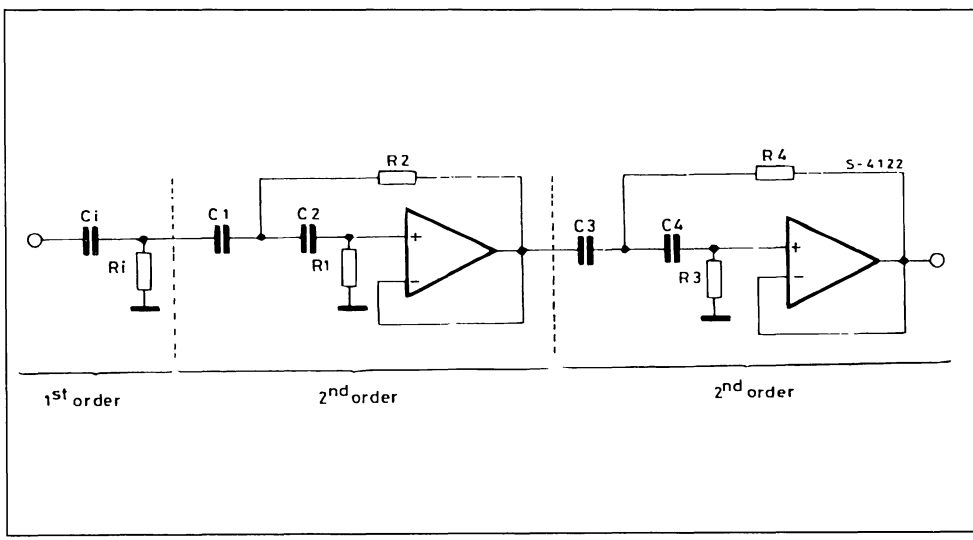
$$R_3 = \frac{1}{0.309} \cdot \frac{1}{C} \cdot \frac{1}{2\pi f_c} = 103K\Omega$$

$$R_4 = \frac{1}{3.325} \cdot \frac{1}{C} \cdot \frac{1}{2\pi f_c} = 9.6K\Omega$$

Table 2 : Damping Factor for Low-pass Butterworth Filters.

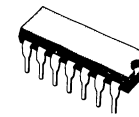
Order	C_I	C_1	C_2	C_3	C_4	C_5	C_6	C_7	C_8
2		0.707	1.41						
3	1.392	0.202	3.54						
4		0.92	1.08	0.38	2.61				
5	1.354	0.421	1.75	0.309	3.235				
6		0.966	1.035	0.707	1.414	0.259	3.86		
7	1.336	0.488	1.53	0.623	1.604	0.222	4.49		
8		0.98	1.02	0.83	1.20	0.556	1.80	0.195	5.125

Figure 16 : 5th Order High-pass Filter (Butterworth) with Unity Gain Configuration.

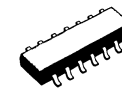


HIGH PERFORMANCE QUAD OPERATIONAL AMPLIFIERS

- SINGLE OR SPLIT SUPPLY OPERATION
- VERY LOW POWER CONSUMPTION
- SHORT CIRCUIT PROTECTION
- LOW DISTORTION, LOW NOISE
- HIGH GAIN-BANDWIDTH PRODUCT
- HIGH CHANNEL SEPARATION



DIP14
(Plastic 0.25)



SO-14J

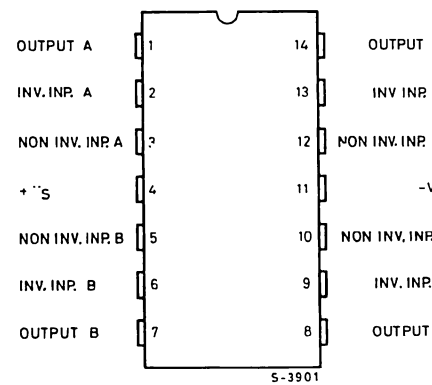
DESCRIPTION

The LS404 is a high performance quad operational amplifier with frequency and phase compensation built into the chip. The internal phase compensation allows stable operation as voltage follower in spite of its high gain-bandwidth product. The circuit presents very stable electrical characteristics over the entire supply voltage range, and it is particularly intended for professional and telecom applications (active filters, etc.).

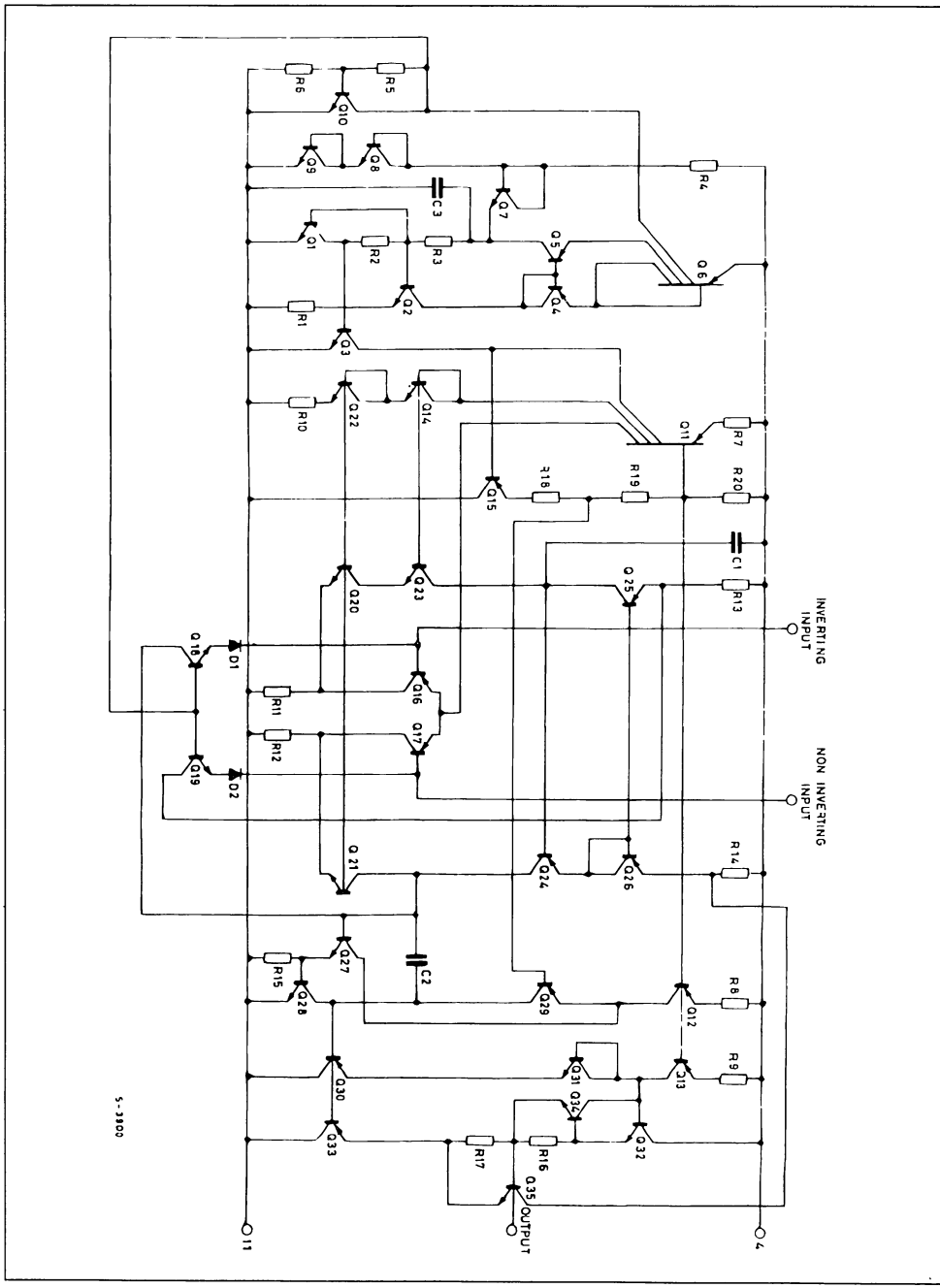
The patented input stage circuit allows small input signal swings below the negative supply voltage and prevents phase inversion when the input is over driven.

CONNECTION DIAGRAM AND ORDERING NUMBERS (top view)

Type	DIP 14	SO-14
LS404 LS404C	– LS404CB	LS404D1 LS404CD1



SCHEMATIC DIAGRAM (one section)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_s	Supply Voltage		± 18	V
V_i	Input Voltage	(positive) (negative)	+ V_s − V_s − 0.5	V
V_i	Differential Input Voltage		± (V_s − 1)	
T_{op}	Operating Temperature	**LS404** **LS404C**	− 25 to + 85 0 to + 70	°C °C
P_{tot}	Power Dissipation	(T_{amb} = 70°C)	400	mW
T_{stg}	Storage Temperature		− 55 to + 150	°C

THERMAL DATA

			DIP 14	SO−14 J
$R_{th j\text{-}amb}$	Thermal Resistance Junction-ambient	Max	200°C/W	200°C/W

(*) Measured with the device mounted on a ceramic substrate (25 x 16 x 0.6 mm).

ELECTRICAL CHARACTERISTICS (V_s = ± 12 V, T_{amb} = 25 °C, unless otherwise specified)

Symbol	Parameter	Test Conditions		LS404			LS404C			Unit
				Min.	Typ.	Max.	Min.	Typ.	Max.	
I_s	Supply Current				1.3	2		1.5	3	mA
I_b	Input Bias Current				50	200		100	300	nA
R_i	Input Resistance	f = 1 KHz			0.7	2.5		0.5	5	MΩ
V_{os}	Input Offset Voltage	R_g = 10 KΩ			1			1		mV
$\frac{\Delta V_{os}}{\Delta T}$	Input Offset Voltage Drift	R_g = 10 KΩ $T_{min} < T_{op} < T_{max}$			5			5		µV/°C
I_{os}	Input Offset Current				10	40		20	80	nA
$\frac{\Delta I_{os}}{\Delta T}$	Input Offset Current Drift	$T_{min} < T_{op} < T_{max}$			0.08			0.1		nA/°C
I_{sc}	Output Short Circuit Current				23			23		mA
G_v	Large Signal Open Loop Voltage Gain	R_L = 2 KΩ	V_s = ± 12 V V_s = ± 4 V	90	100 95		86	100 95		dB
B	Gain-bandwidth Product	f = 20 KHz		1.8	3		1.5	2.5		MHz
e_N	Total Input Noise Voltage	f = 1 KHz R_g = 50 Ω R_g = 1 KΩ R_g = 10 KΩ			8 10 18	15		10 12 20		nV/√Hz
d	Distortion	Unity Gain R_L = 2 KΩ V_o = 2 V_{PP}	f = 1 KHz f = 20 KHz		0.01 0.03	0.04		0.01 0.03		%
V_o	DC Output Voltage Swing	R_L = 2 KΩ	V_s = ± 12 V V_s = ± 4 V	± 10	± 3		± 10	± 3		V

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions	LS404			LS404C			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
V_o	Large Signal Voltage Swing	f = 10 KHz R_L = 10 KΩ R_L = 1 KΩ		22 20			22 20		V_{pp}
SR	Slew Rate	Unity Gain R_L = 2 KΩ	0.8	1.5			1		V/μs
CMR	Common Mode Rejection	V_i = 10 V	90	94		80	90		dB
SVR	Supply Voltage Rejection	V_i = 1 V f = 100 Hz	90	94		86	90		dB
CS	Channel Separation	f = 1 KHz	100	120			120		dB

Figure 1: Supply Current vs. Supply Voltage.

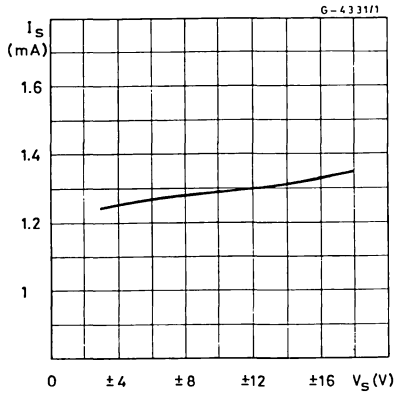


Figure 2 : Supply Current vs. Ambient Temperature.

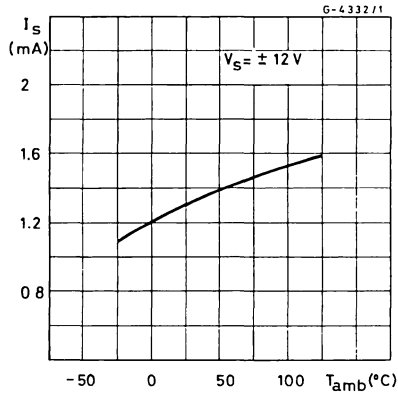


Figure 3 : Output Short Circuit Current vs. Ambient Temperature.

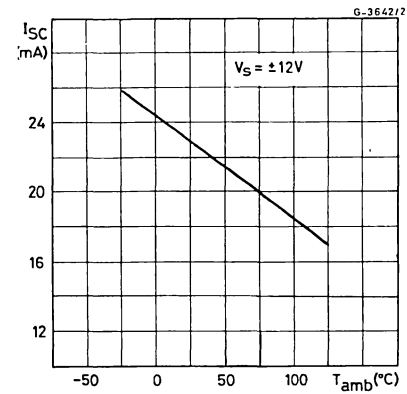


Figure 4: Open Loop Frequency and Phase Response.

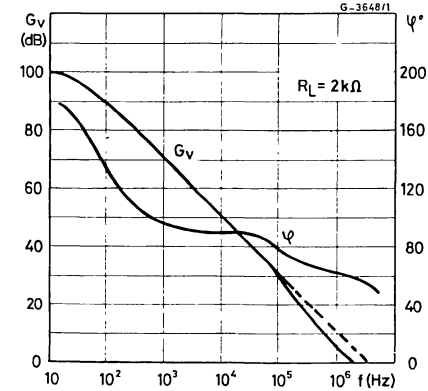


Figure 5: Open Loop Gain vs. Ambient Temperature.

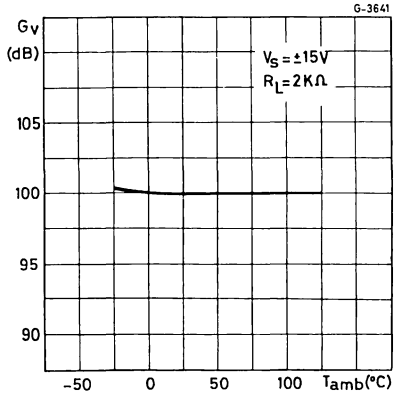


Figure 6 : Supply Voltage Rejection vs. Frequency.

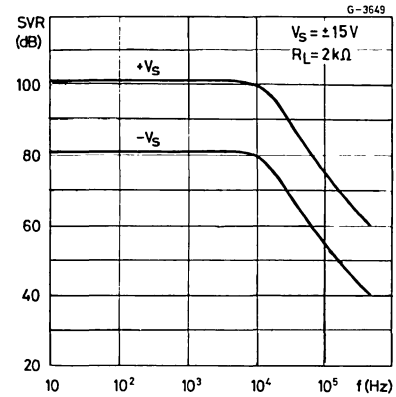


Figure 7 : Large Signal Frequency Response.

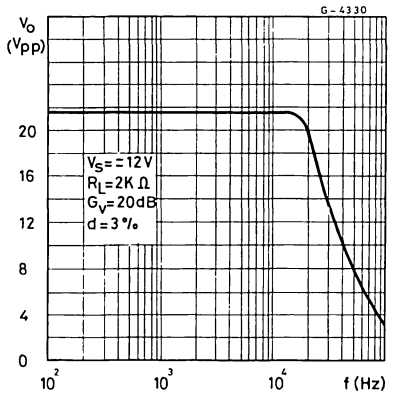


Figure 8 : Output Voltage Swing vs. Load Resistance.

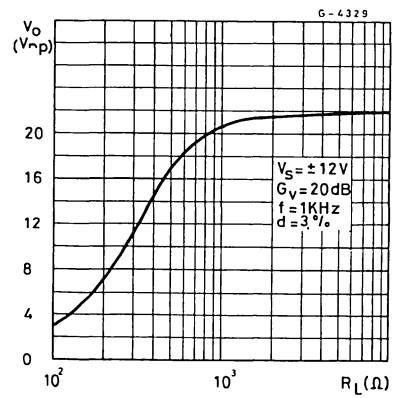
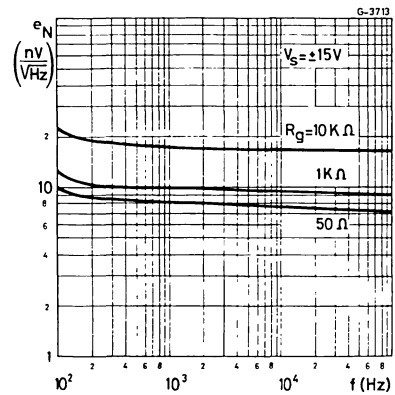


Figure 9 : Total Input Noise vs. Frequency.



APPLICATION INFORMATION

Active low-pass filter :

BUTTERWORTH

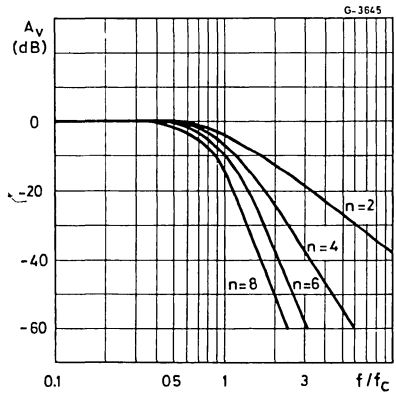
The Butterworth is a "maximally flat" amplitude response filter. Butterworth filters are used for filtering signals in data acquisition systems to prevent aliasing errors in sampled-data applications and for general purpose low-pass filtering.

The cutoff frequency, f_c, is the frequency at which the amplitude response in down 3 dB. The attenuation rate beyond the cutoff frequency is - n6 dB per octave of frequency where n is the order (number of poles) of the filter.

Other characteristics :

- Flattest possible amplitude response.
- Excellent gain accuracy at low frequency end of passband.

Figure 10 : Amplitude Response.



BESSEL

The Bessel is a type of "linear phase" filter. Because of their linear phase characteristics, these filters approximate a constant time delay over a limited frequency range. Bessel filters pass transient waveforms with a minimum of distortion. They are also used to provide time delays for low pass filtering of modulated waveforms and as a "running average" type filter.

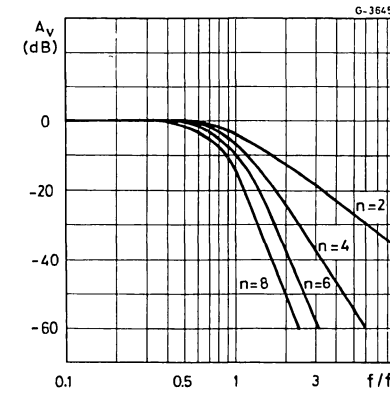
The maximum phase shift is $\frac{-n\pi}{2}$ radians where n is the order (number of poles) of the filter. The cutoff frequency, f_c, is defined as the frequency at which the phase shift is one half to this value. For accurate delay, the cutoff frequency should be twice the maximum signal frequency. The following table can be used to obtain the – 3 dB frequency of the filter.

	2 pole	4 Pole	6 Pole	8 Pole
– 3dB Frequency	0.77 f_c	0.67 f_c	0.57 f_c	0.50 f_c

Other characteristics :

- Selectivity not as great as Chebyschev or Butterworth.
- Very small overshoot response to step inputs.
- Fast rise time.

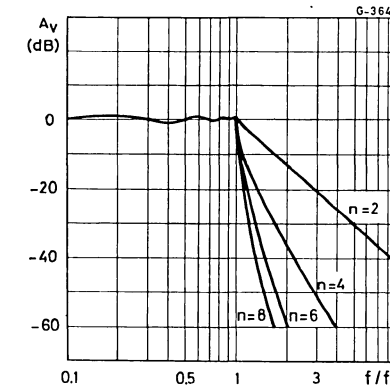
Figure 11 : Amplitude Response.



CHEBYSCHEV

Chebyschev filters have greater selectivity than either Bessel or Butterworth at the expense of ripple in the passband.

Figure 12 : Amplitude Response (± 1 dB ripple).



APPLICATION INFORMATION (continued)

Chebyschev filters are normally designed with peak-to-peak ripple values from 0.2 dB to 2 dB.

Increased ripple in the passband allows increased attenuation above the cutoff frequency.

The cutoff frequency is defined as the frequency at which the amplitude response passes through the specified maximum ripple band and enters the stop band.

Other characteristics :

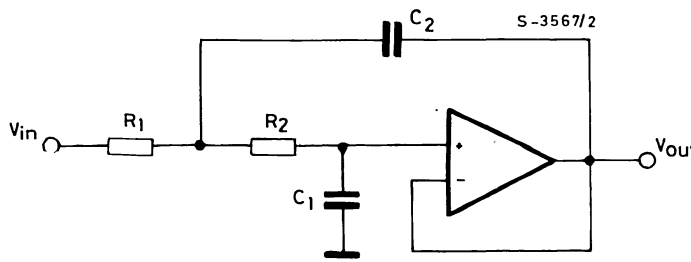
- Greater selectivity.
- Very nonlinear phase response.
- High overshoot response to step inputs.

The table below shows the typical overshoot and setting time response of the low pass filter to a step input.

	Number of Poles	Peak Overshoot	Settling Time (% of final value)		
		% Overshoot	± 1%	± 0.1%	± 0.01%
Butterworth	2	4	$1.1/f_c$ sec.	$1.7/f_c$ sec.	$1.9/f_c$ sec.
	4	11	$1.7/f_c$	$2.8/f_c$	$3.8/f_c$
	6	14	$2.4/f_c$	$3.9/f_c$	$5.0/f_c$
	8	16	$3.1/f_c$	$5.1/f_c$	$7.1/f_c$
Bessel	2	0.4	0.8/fc	1.4/fc	1.7/fc
	4	0.8	1.0/fc	1.8/fc	2.4/fc
	6	0.6	1.3/fc	2.1/fc	2.7/fc
	8	0.3	1.6/fc	2.3/fc	3.2/fc
Chebyschev (ripple ± 0.25dB)	2	11	1.1/fc	1.6/fc	–
	4	18	3.0/fc	5.4/fc	–
	6	21	5.9/fc	10.4/fc	–
	8	23	8.4/fc	16.4/fc	–
Chebyschev (ripple ± 1dB)	2	21	1.6/fc	2.7/fc	–
	4	28	4.8/fc	8.4/fc	–
	6	32	8.2/fc	16.3/fc	–
	8	34	11.6/fc	24.8/fc	–

Design of 2nd order active low pass filter (Sallen and Key configuration unity gain op-amp).

Figure 13 : Filter Configuration.



$$\frac{V_o}{V_I} = \frac{1}{1 + 2\xi \frac{S}{\omega_c} + \frac{S^2}{\omega_c^2}}$$

Where :

$\omega c = 2\pi f_c$ with f_c = cutoff frequency

ξ = damping factor.

APPLICATION INFORMATION (continued)

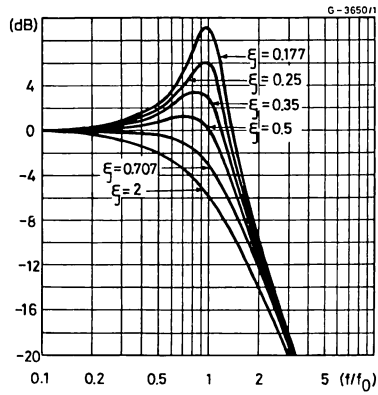
Three parameters are needed to characterize the frequency and phase response of a 2nd order active filter : the gain (G_V), the damping factor (ξ) or the Q-factor ($Q = (2\xi)^{-1}$), and the cutoff frequency (f_c).
The higher order responses are obtained with a series of 2nd order sections. A simple RC section is introduced when an odd filter is required.

The choice of 'ξ' (or Q-factor) determines the filter response (see table).

Table 1.

Filter Response	ξ	Q	Cutoff Frequency f_c
Bessel	$\frac{\sqrt{3}}{2}$	$\frac{1}{\sqrt{3}}$	Frequency at which Phase Shift is – 90°C
Butterworth	$\frac{\sqrt{2}}{2}$	$\frac{1}{\sqrt{2}}$	Frequency at which G_v = – 3dB
Chebyschev	$< \frac{\sqrt{2}}{2}$	$> \frac{1}{\sqrt{2}}$	Frequency at which the amplitude response passes through specified max. ripple band and enters the stop band.

Figure 14 : Filter Response vs. Damping Factor.



Fixed $R = R_1 = R_2$, we have (see fig. 13)

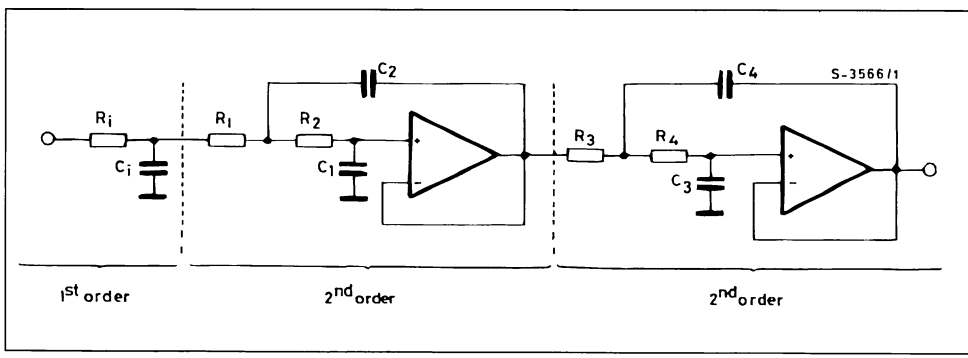
$$C_1 = \frac{1}{R}\,\frac{\xi}{\omega_c}$$

$$C_2 = \frac{1}{R}\,\frac{1}{\xi\omega_c}$$

The diagram of fig.14 shows the amplitude response for different values of damping factor ξ in 2nd order filters.

EXAMPLE

Figure 15 : 5th Order Low Pass Filter (Butterworth) with Unity Gain Configuration.



APPLICATION INFORMATION (continued)

In the circuit of fig. 15, for f_c = 3.4 KHz and $R_i = R_1 = R_2 = R_3 = R_4$ =10 KΩ, we obtain :

$$C_i = 1.354 \cdot \frac{1}{R} \cdot \frac{1}{2\pi f_c} = 6.33\text{nF}$$

$$C_1 = 0.421 \cdot \frac{1}{R} \cdot \frac{1}{2\pi f_c} = 1.97\ \text{nF}$$

$$C_2 = 1.753 \cdot \frac{1}{R} \cdot \frac{1}{2\pi f_c} = 8.20\ \text{nF}$$

$$C_3 = 0.309 \cdot \frac{1}{R} \cdot \frac{1}{2\pi f_c} = 1.45\ \text{nF}$$

$$C_4 = 3.325 \cdot \frac{1}{R} \cdot \frac{1}{2\pi f_c} = 15.14\ \text{nF}$$

The attenuation of the filter is 30 dB at 6.8 KHz and better than 60 dB at 15 KHz.

The same method, referring to Tab. II and fig. 16, is used to design high-pass filter. In this case the damping factor is found by taking the reciprocal of the numbers in Tab. II. For f_c = 5 KHz and $C_i = C_1 = C_2 = C_3 = C_4$ = 1 nF we obtain :

$$R_i = \frac{1}{1.354} \cdot \frac{1}{C} \cdot \frac{1}{2\pi f_c} = 23.5\ \text{K}\Omega$$

$$R_1 = \frac{1}{0.421} \cdot \frac{1}{C} \cdot \frac{1}{2\pi f_c} = 75.6\ \text{K}\Omega$$

$$R_2 = \frac{1}{1.753} \cdot \frac{1}{C} \cdot \frac{1}{2\pi f_c} = 18.2\ \text{K}\Omega$$

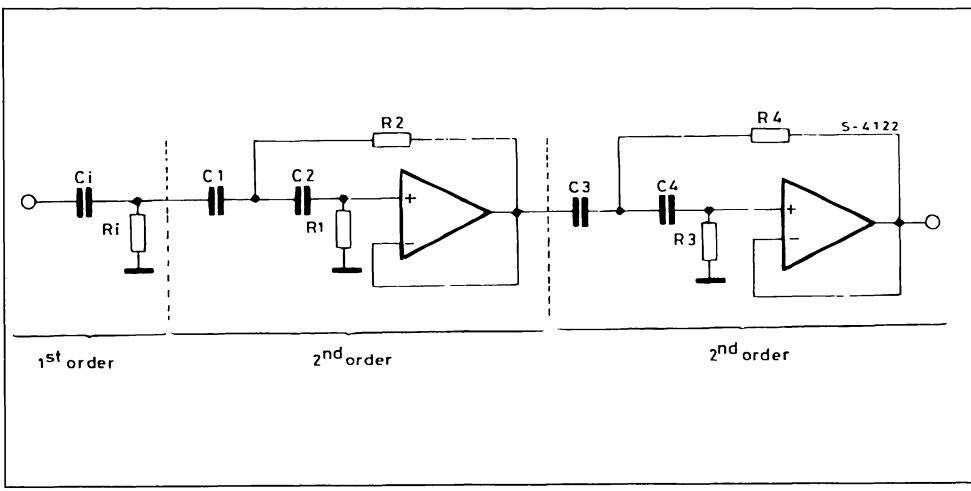
$$R_3 = \frac{1}{0.309} \cdot \frac{1}{C} \cdot \frac{1}{2\pi f_c} = 103\ \text{K}\Omega$$

$$R_4 = \frac{1}{3.325} \cdot \frac{1}{C} \cdot \frac{1}{2\pi f_c} = 9.6\ \text{K}\Omega$$

Table II : Damping Factor for Low-pass Butterworth Filters.

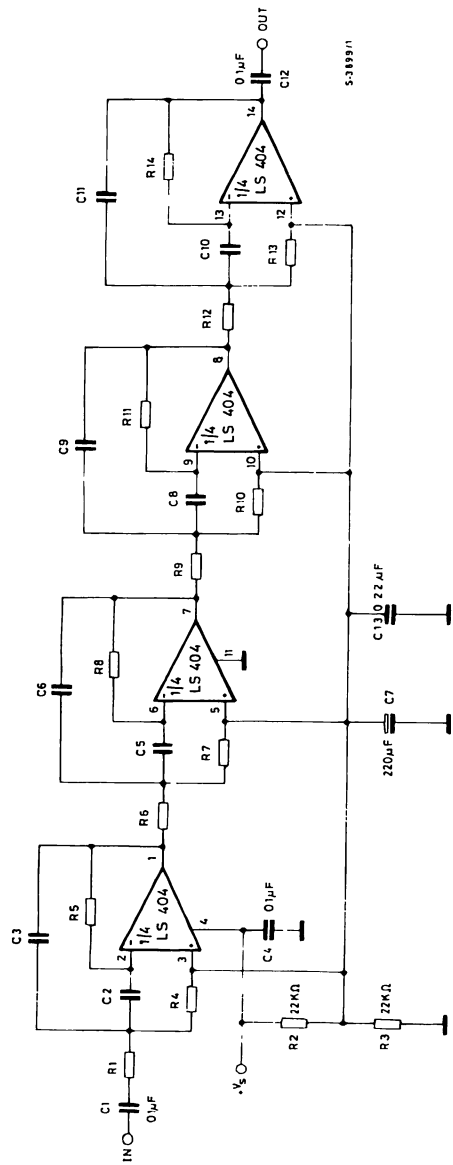
Order	C_I	C_1	C_2	C_3	C_4	C_5	C_6	C_7	C_8
2		0.707	1.41						
3	1.392	0.202	3.54						
4		0.92	1.08	0.38	2.61				
5	1.354	0.421	1.75	0.309	3.235				
6		0.966	1.035	0.707	1.414	0.259	3.86		
7	1.336	0.488	1.53	0.623	1.604	0.222	4.49		
8		0.98	1.02	0.83	1.20	0.556	1.80	0.195	5.125

Figure 16 : 5th Order High-pass Filter (Butterworth) with Unity Gain Configuration.



APPLICATION INFORMATION (continued)

Figure 17 : Multiple Feedback 8-pole Bandpass Filter.



f_c = 1.180 Hz ; A = 1 ; $C_2 = C_3 = C_5 = C_6 = C_8 = C_9 = C_{10} = C_{11}$ = 3.300 pF ;

$R_1 = R_6 = R_9 = R_{12}$ = 160 KΩ ; $R_5 = R_8 = R_{11} = R_{14}$ = 330 KΩ ; $R_4 = R_7 = R_{10} = R_{13}$ = 5.3 KΩ

Figure 18 : Frequency Response of Band-pass Filter.

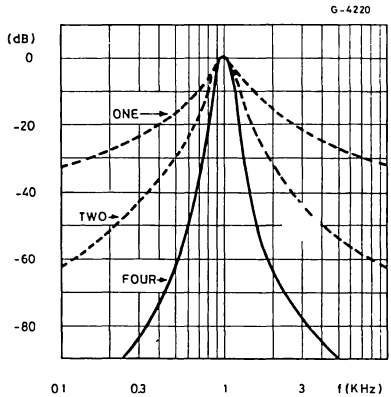


Figure 19 : Bandwidth of Band-pass Filter.

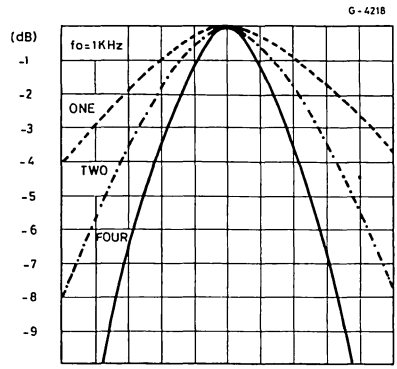
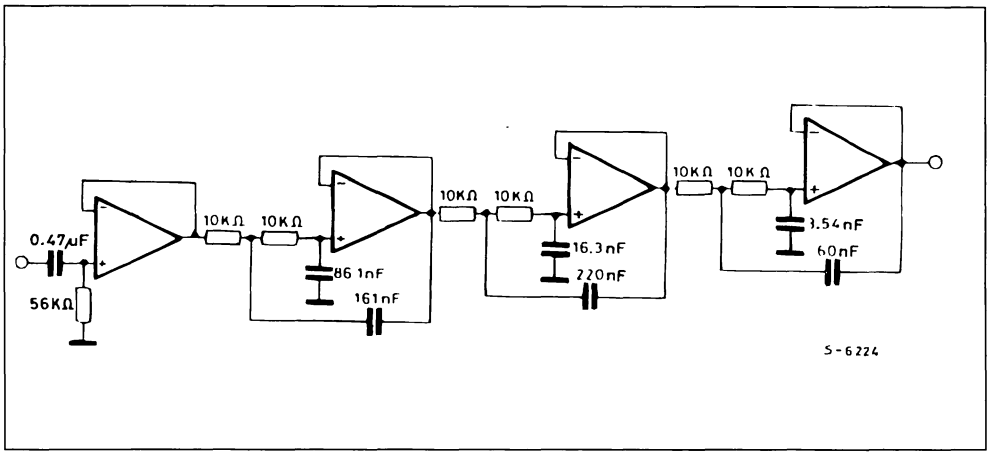
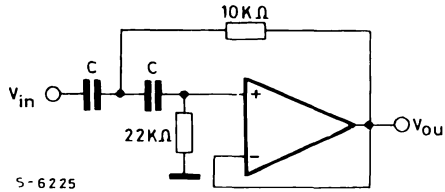


Figure 20 : Six-pole 355 Hz Low-pass Filter (chebychev type).



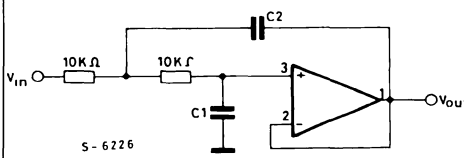
This is a 6-pole Chebychev type with ± 0.25 dB ripple in the passband. A decoupling stage is used to avoid the influence of the input impedance on the filter's characteristics. The attenuation is about 55 dB at 710 Hz and reaches 80 dB at 1065 Hz. The in band attenuation is limited in practice to the ± 0.25 dB ripple and does not exceed 0.5 dB at 0.9 fc.

Figure 21 : Subsonic Filter (G_v = 0 dB).



f_c (Hz)	C (µF)
15	0.68
22	0.47
30	0.33
55	0.22
100	0.1

Figure 22 : High Cut Filter (G_v = 0 dB).



f_c (KHz)	C1 (nF)	C2 (nF)
3	3.9	6.8
5	2.2	4.7
10	1.2	2.2
15	0.68	1.5

SGS-THOMSON MICROELECTRONICS

TEB1033
TEF1033 - TEC1033

BIPOLAR DUAL OPERATIONAL AMPLIFIERS

- LOW DISTORTION RATIO
- LOW NOISE
- VERY LOW SUPPLY CURRENT
- LOW INPUT OFFSET CURRENT
- VERY LOW INPUT OFFSET VOLTAGE
- LARGE COMMON-MODE RANGE
- HIGH GAIN
- HIGH OUTPUT CURRENT
- GAIN-BANDWIDTH PRODUCT : 2.5 MHz
- TEMPERATURE DRIFT : 2 µV/°C
- LONG TERM STABILITY : 8 µV/YEAR (for $T_{amb} \leq 50$ °C)
- THE TEB1033 AND TEF1033 ARE PIN TO PIN REPLACEMENT OF THE LS204C AND LS204 RESPECTIVELY

N
DIP8
(Plastic Package)

D
SO8
(Plastic Micropackage)

GC
LCC20
(Tricecop (LCC))

DESCRIPTION

The TEB1033, TEF1033 and TEC1033 are high performance dual-operational amplifiers intended for active filter applications. The internal phase compensation allows stable operation as voltage follower in spite of their high gain-bandwidth products.

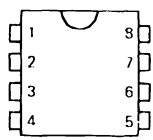
The circuits present very stable electrical characteristics over the entire supply voltage range.

ORDERING INFORMATION

Part Number	Temperature Range	Package		
		N	D	GC
TEB1033	0 °C to + 70 °C	•	•	
TEF1033	– 40 °C to + 105 °C	•	•	
TEC1033	– 55 °C to + 125 °C			•
Examples : TEB1033N, TEC1033GC				

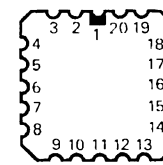
PIN CONNECTIONS (top views)

DIP8/SO8



1 - Output 1
2 - Inverting input 1
3 - Non-inverting input 1
4 - V_{CC}^-
5 - Non-inverting input 2
6 - Inverting input 2
7 - Output 2
8 - V_{CC}^+

LCC20

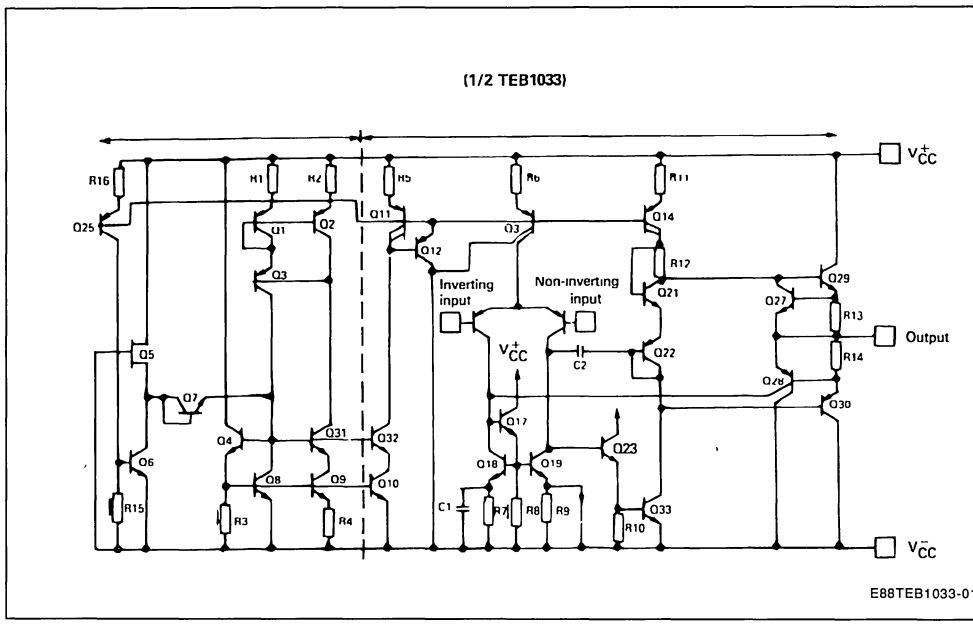


1 - NC
2 - Output 1
3 - NC
4 - NC
5 - Inverting input 1
6 - NC
7 - Non-inverting input 1
8 - NC
9 - NC
10 - V_{CC}^-
11 - NC
12 - Non-Inverting input 2
13 - NC
14 - NC
15 - Inverting Input 2
16 - NC
17 - Output 2
18 - NC
19 - NC
20 - V_{CC}^+

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		± 18	V
V_I	Input Voltage		± V_{CC}	V
V_{ID}	Differential Input Voltage		± (V_{CC} –1)	V
P_{tot}	Power Dissipation			mW
		TEB1033D, TEF1033D	400	
		TEB1033N	665	
		TEC1033GC	665	
T_{oper}	Operating Free-air Temperature Range			°C
		TEB1033	0 to + 70	
		TEF1033	– 40 to + 105	
		TEC1033	– 55 to + 125	
T_{stg}	Storage Temperature Range		– 55 to + 150	°C

BLOCK DIAGRAM



Case	Outputs	Inverting Inputs	Non-inverting Inputs	V_{CC}^+	V_{CC}^-	N. C.
DIP8 SO8	1, 7	2, 6	3, 5	8	4	
LCC20	2, 17	5, 15	7, 12	20	10	*

* **LCC20 :** Other pins are not connected.

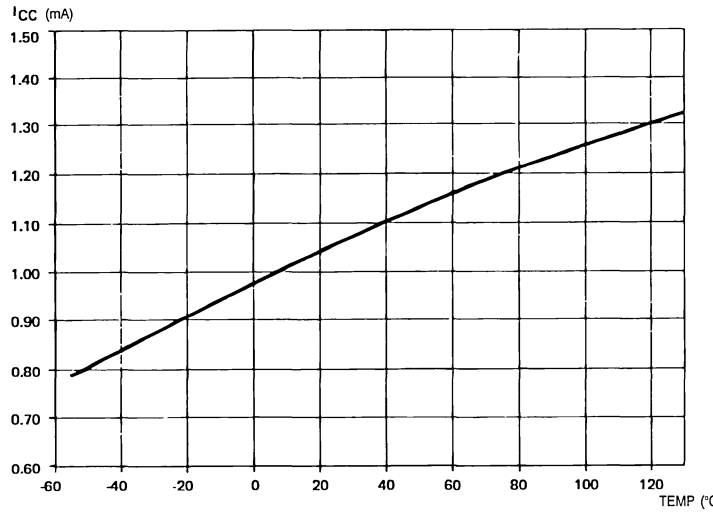
ELECTRICAL CHARACTERISTICS

$V_{CC} = \pm 15$ V (unless otherwise specified)
TEC 1033 : $-55 \leq T_{amb} \leq +125$ °C
TEF 1033 : $-40 \leq T_{amb} \leq +105$ °C
TEB 1033 : $0 \leq T_{amb} \leq +70$ °C

Symbol	Parameter	TEB 1033 TEF 1033 TEC 1033			Unit
		Min.	Typ.	Max.	
V_{IO}	Input Offset Voltage T_{amb} = 25 °C (RS ≤ 10 kΩ) $T_{min} \leq T_{amb} \leq T_{max}$		0.3	1 3	mV
DV_{IO}	Input Offset Voltage Drift		2		µV/°C
I_{IO}	Input Offset Current T_{amb} = 25 °C $T_{min} \leq T_{amb} \leq T_{max}$		5	20 40	nA
I_{IB}	Input Bias Current T_{amb} = 25 °C $T_{min} \leq T_{amb} \leq T_{max}$		50	100 200	nA
A_{vd}	Large Signal Voltage Gain (R_L = 2 kΩ, $V_O = \pm 10$ V) T_{amb} = 25 °C $T_{min} \leq T_{amb} \leq T_{max}$	 100 100	 300		V/mV
SVR	Supply Voltage Rejection Ratio DV_{CC} from ± 15 V to ± 4 V T_{amb} = 25 °C $T_{min} \leq T_{amb} \leq T_{max}$	 100 100	 110		dB
I_{CC}	Supply Current, all Amp, no Load T_{amb} = 25 °C $T_{min} \leq T_{amb} \leq T_{max}$		1	1.5 2	mA
V_I	Input Voltage Range T_{amb} = 25 °C	− 12		+ 12	V
CMR	Common Mode Rejection Ratio (R_S ≤ 10 kΩ, $V_I = \pm 10$ V) T_{amb} = 25 °C $T_{min} \leq T_{amb} \leq T_{max}$	 100 100	 110		dB
I_{os}	Output Short-circuit Current T_{amb} = 25 °C $T_{min} \leq T_{amb} \leq T_{max}$	 10 10	 23	 40 40	mA
$\pm V_{opp}$	Output Voltage Swing T_{amb} = 25 °C R_L = 2 kΩ $T_{min} \leq T_{amb} \leq T_{max}$ R_L = 2 kΩ $V_{CC} = \pm 4$ V, R_L = 2 KΩ $V_{CC} = \pm 6$ V, R_L = 600 Ω	 13 12 2.8 4.6	 14 3		V
S_{vo}	Slew-rate ($V_I = \pm 10$ V, R_L = 2 kΩ, $C_L \leq 100$ pF, T_{amb} = 25 °C, unity gain)	0.6	1	3	V/µs
GBP	Gain Bandwidth Product (f = 100 KHz, T_{amb} = 25 °C, V_{IN} = 10 mV, R_L = 2 kΩ, C_L = 100 pF)	1.8	2.5	3.2	MHz
R_I	Input Resistance (T_{amb} = 25 °C)		1		MΩ

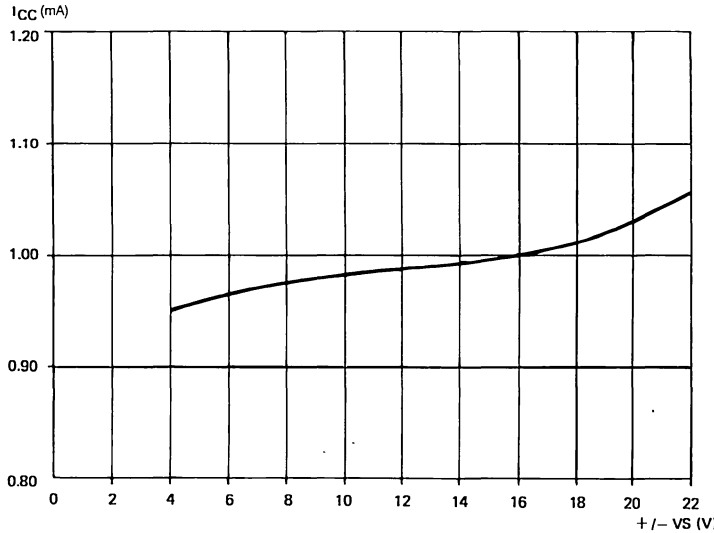
ELECTRICAL CHARACTERISTICS(continued)

Symbol	Parameter	TEB 1033 TEF 1033 TEC 1033			Unit
		Min.	Typ.	Max.	
THD	Total Harmonic Distortion (f = 1KHz, A_v = 20 dB, R_L = 2 kΩ $C_L \leq 100$ pF, T_{amb} = 25 °C, V_o = 2 V_{pp})		0.008	0.05	%
V_n	Equivalent Input Noise Voltage (f = 1 KHz) R_S = 50 Ω R_S = 1 kΩ R_S = 10 kΩ		 8 10 18	 15	 nV/√Hz
V_{OPP}	Large Signal Voltage Swing R_L =10 kΩ, f = 10 KHz	26	28		V
φM	Phase Margin		45		Degrees
V_{o1}/V_{o2}	Channel Separation	100	120		dB



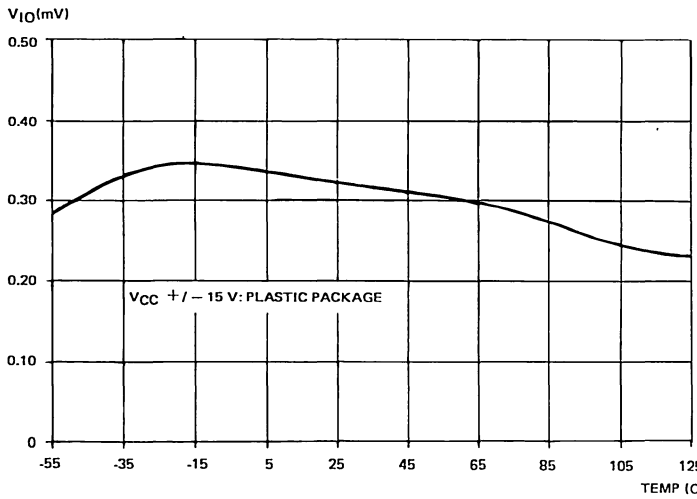
SUPPLY CURRENT VS. AMBIENT TEMPERATURE

E88TEB1033-02



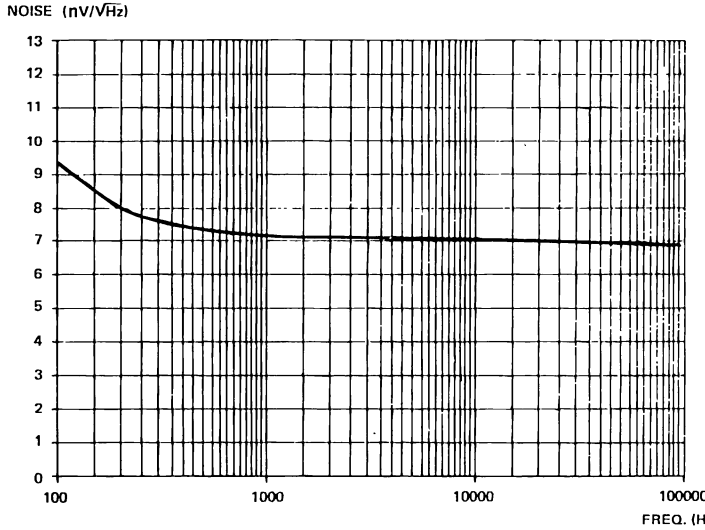
SUPPLY CURRENT VS. SUPPLY VOLTAGE

E88TEB1033-03



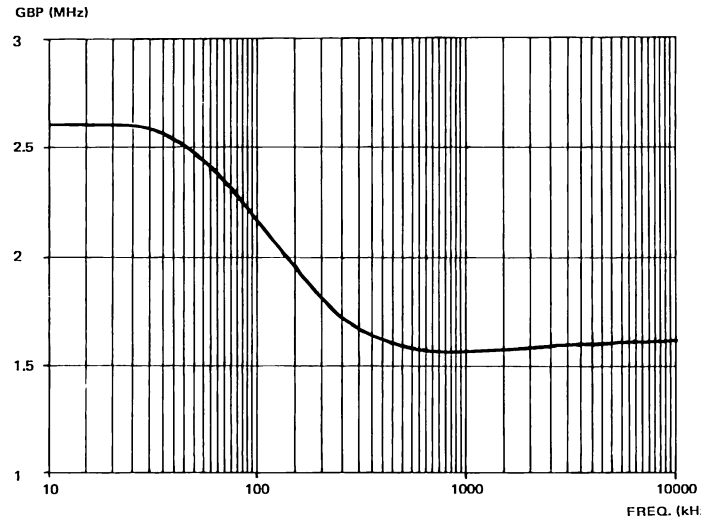
OFFSET VOLTAGE VS. AMBIENT TEMPERATURE

E88TEB1033-04



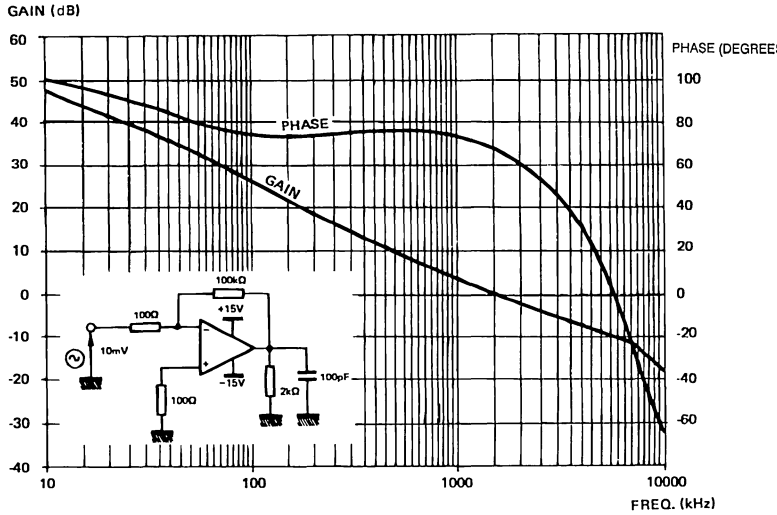
TOTAL INPUT NOISE VS. FREQUENCY

E88TEB1033-05



GAIN BANDWIDTH PRODUCT VS. FREQUENCY

E88TEB1033-06

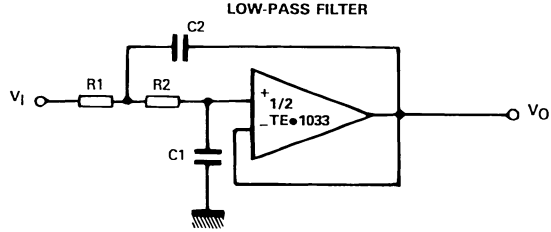


BODE PLOT

E88TEB1033-07

TYPICAL APPLICATION

LOW-PASS FILTER



E88TEB1033-08

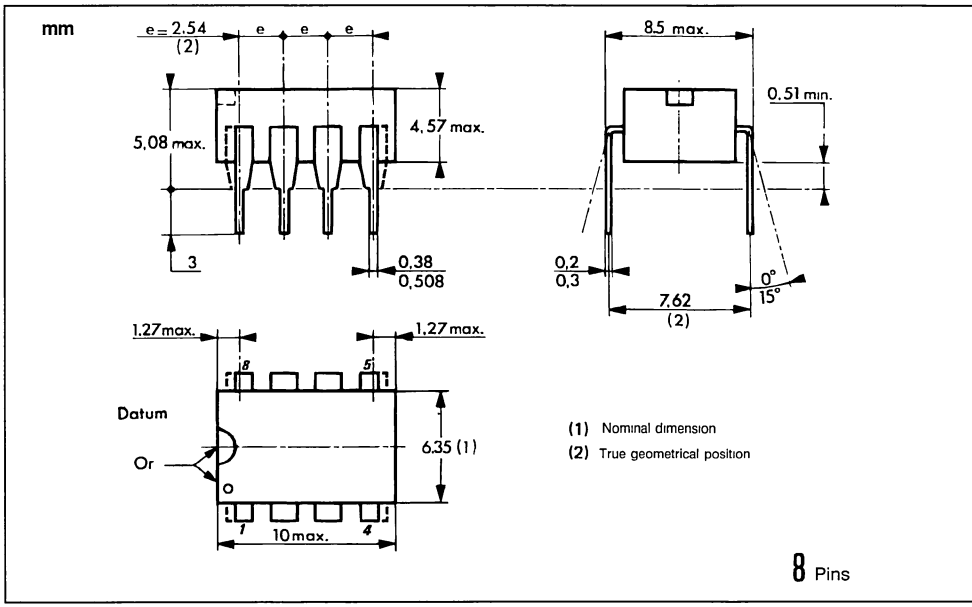
$$\frac{V_o}{V_i} = \frac{1}{1 + 2\xi \frac{S}{\omega_c} + \frac{S^2}{\omega_c^2}}$$

$\omega_c = 2\pi f_c$, with f_c = cutt-off frequency

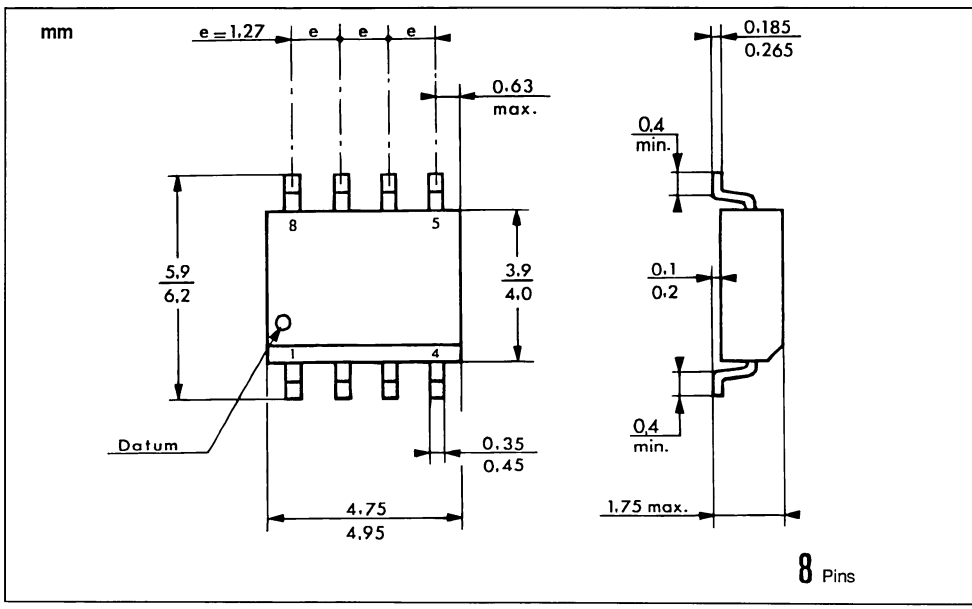
ξ = damping factor

PACKAGE MECHANICAL DATA

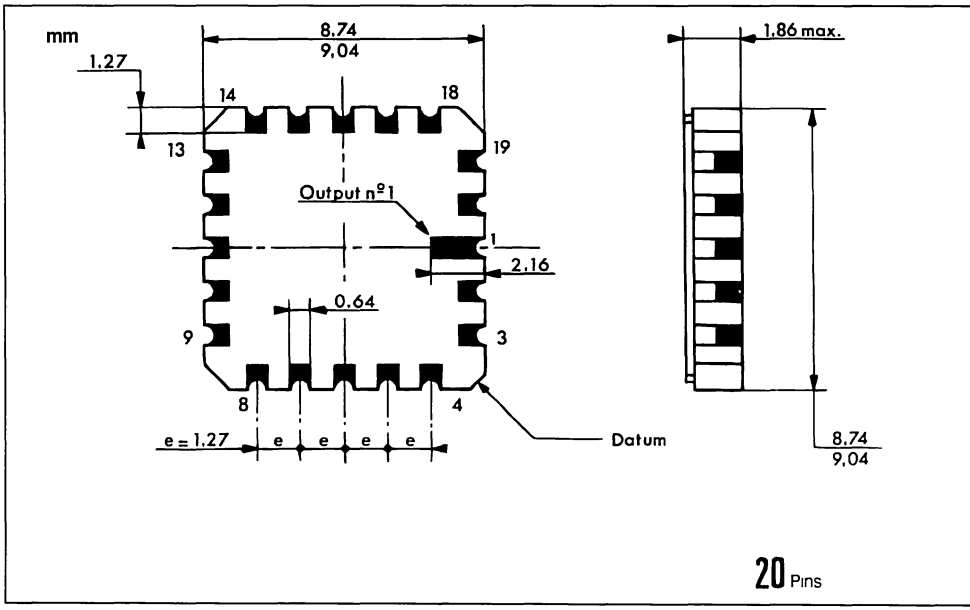
8 PINS – PLASTIC DIP



8 PINS – PLASTIC MICROPACKAGE (SO)



20 PINS – TRICECOP (LCC)

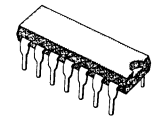


SGS-THOMSON MICROELECTRONICS

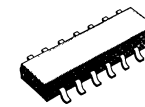
TEB4033
TEF4033 - TEC4033

BIPOLAR QUAD OPERATIONAL AMPLIFIERS

- LOW DISTORTION RATIO
- LOW NOISE
- VERY LOW SUPPLY CURRENT
- LOW INPUT OFFSET CURRENT
- VERY LOW INPUT OFFSET VOLTAGE
- LARGE COMMON-MODE RANGE
- HIGH GAIN
- HIGH OUTPUT CURRENT
- GAIN-BANDWIDTH PRODUCT : 2.5 MHz
- TEMPERATURE DRIFT : 2 µV/°C
- LONG TERM STABILITY : 8 µV/YEAR (for $T_{amb} \leq 50$ °C)
- THE TEB4033 AND TEF4033 ARE PIN TO PIN REPLACEMENT OF THE LS404C AND LS404 RESPECTIVELY



N
DIP14
(Plastic Package)



D
SO14
(Plastic Micropackage)

J
CERDIP14
(Cerdip Package)

GC
LCC20
(Tricecop (LCC))

DESCRIPTION

The TEB4033, TEF4033 and TEC4033 are high performance quad-operational amplifiers intended for active filter applications. The internal phase compensation allows stable operation as voltage follower in spite of their high gain-bandwidth products.

The circuits present very stable electrical characteristics over the entire supply voltage range.

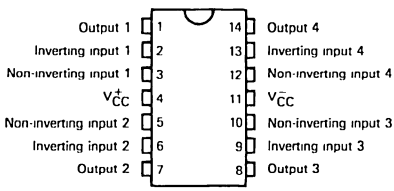
ORDERING INFORMATION

Part Number	Temperature Range	Package		
		N	D	GC
TEB4033	0 °C to + 70 °C	•	•	
TEF4033	– 40 °C to + 105 °C	•	•	
TEC4033	– 55 °C to + 125 °C			•

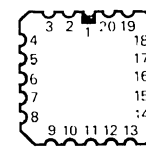
Examples : TEB4033N, TEC4033GC

PIN CONNECTIONS (top views)

DIP14/CERDIP14
SO14



LCC20

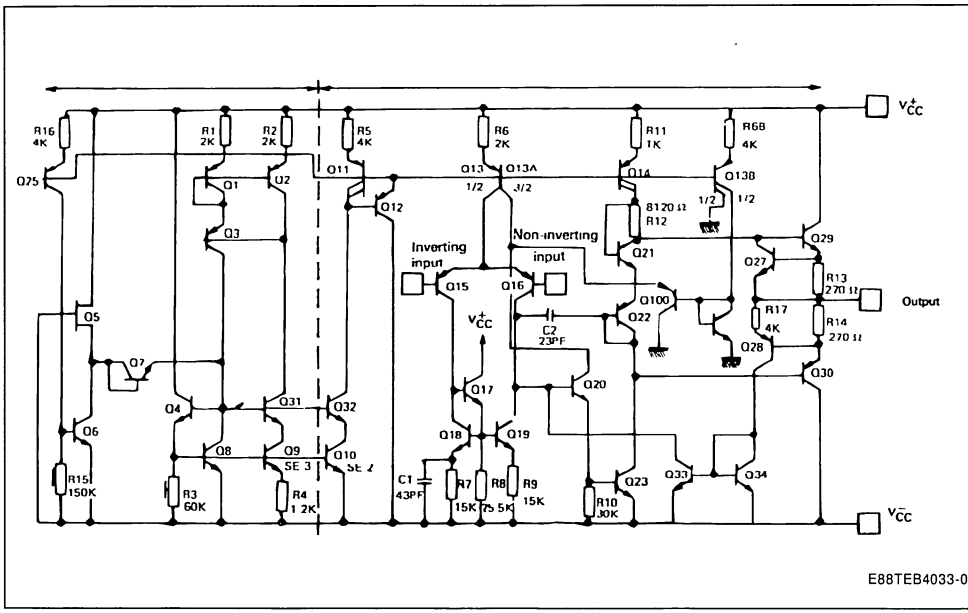


1 - NC
2 - Output 1
3 - Inverting input 1
4 - Non-inverting input 1
5 - NC
6 - V_{CC}^{+}
7 - NC
8 - Non-inverting input 2
9 - Inverting input 2
10 - Output 2
11 - NC
12 - Output 3
13 - Inverting input 3
14 - Non-inverting input 3
15 - NC
16 - V_{CC}^{-}
17 - NC
18 - Non-inverting input 4
19 - Inverting input 4
20 - Output 4

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	± 18	V
V_I	Input Voltage	± V_{CC}	V
V_{ID}	Differential Input Voltage	± (V_{CC} –1)	V
P_{tot}	Power Dissipation TEB4033D, TEF4033D TEB4033N, TEF4033N TEC4033GC	 400 665 665	mW
T_{oper}	Operating Free-air Temperature Range TEB4033 TEF4033 TEC4033	 0 to + 70 – 40 to + 105 – 55 to + 125	°C
T_{stg}	Storage Temperature Range	– 65 to + 150	°C

BLOCK DIAGRAM



Case	Outputs	Inverting Inputs	Non-inverting Inputs	V_{CC}^+	V_{CC}^-	N. C.
DIP14 CERDIP14 SO14	1, 7 8, 14	2, 6 9, 13	3, 5 10, 12	4	11	
LCC20	2, 10 12, 20	3, 9 13, 19	4, 8 14, 18	6	16	*

* **LCC20 :** Other pins are not connected.

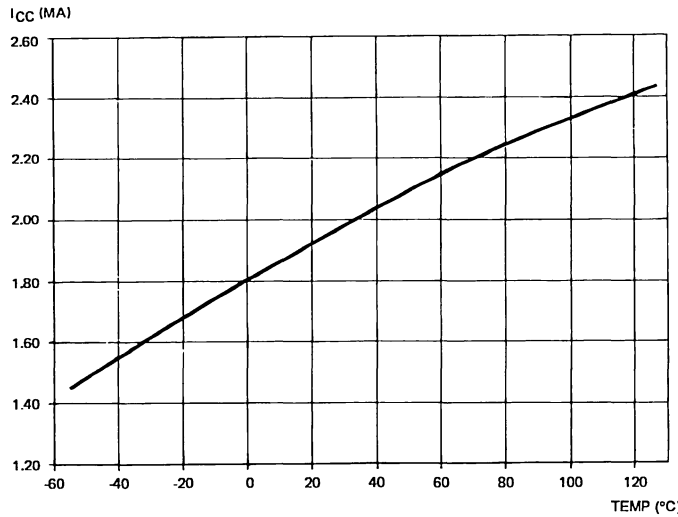
ELECTRICAL CHARACTERISTICS

V_{CC} = ± 15 V (unless otherwise specified)
TEC 4033 : $-55 \leq T_{amb} \leq +125$ °C
TEF 4033 : $-40 \leq T_{amb} \leq +105$ °C
TEB 4033 : $0 \leq T_{amb} \leq +70$ °C

Symbol	Parameter	TEB 4033 TEF 4033 TEC 4033			Unit
		Min.	Typ.	Max.	
V_{IO}	Input Offset Voltage T_{amb} = 25 °C ($R_S \leq 10$ kΩ) $T_{min} \leq T_{amb} \leq T_{max}$		0.3	1 3	mV
DV_{IO}	Input Offset Voltage Drift		2		µV/°C
I_{IO}	Input Offset Current T_{amb} = 25 °C $T_{min} \leq T_{amb} \leq T_{max}$		5	20 40	nA
I_{IB}	Input Bias Current T_{amb} = 25 °C $T_{min} \leq T_{amb} \leq T_{max}$		50	100 200	nA
A_{vd}	Large Signal Voltage Gain (R_L = 2 kΩ, V_O = ± 10 V) T_{amb} = 25 °C $T_{min} \leq T_{amb} \leq T_{max}$	 100 100	300		V/mV
SVR	Supply Voltage Rejection Ratio DV_{CC} from ± 15 V to ± 4 V T_{amb} = 25 °C $T_{min} \leq T_{amb} \leq T_{max}$	 100 100	110		dB
I_{CC}	Supply Current, all Amp, no Load T_{amb} = 25 °C $T_{min} \leq T_{amb} \leq T_{max}$		2	3 4	mA
V_I	Input Voltage Range T_{amb} = 25 °C	− 12		+ 12	V
CMR	Common Mode Rejection Ratio ($R_S \leq 10$ kΩ, V_I = ± 10 V) T_{amb} = 25 °C $T_{min} \leq T_{amb} \leq T_{max}$	 100 100	110		dB
Ios	Output Short-circuit Current T_{amb} = 25 °C $T_{min} \leq T_{amb} \leq T_{max}$	 10 10	23	40 40	mA
± V_{opp}	Output Voltage Swing T_{amb} = 25 ° C R_L = 2 kΩ $T_{min} \leq T_{amb} \leq T_{max}$ R_L = 2 kΩ V_{CC} = ± 4 V, R_L = 2 kΩ V_{CC} = ± 6 V, R_L = 600 Ω	 13 12 2.8 4.6	 14 3		V
S_{vo}	Slew-rate (V_I = ± 10 V, R_L = 2 kΩ $C_L \leq 100$ pF, T_{amb} = 25°C, unity gain)	0.6	1	3	V/µs
GBP	Gain Bandwidth Product (f = 100 KHz, T_{amb} = 25 °C, V_{IN} = 10 mV, R_L = 2 kΩ, C_L = 100 pF)	1.8	2.5	3.2	MHz
R_I	Input Resistance (T_{amb} = 25 °C)		1		MΩ

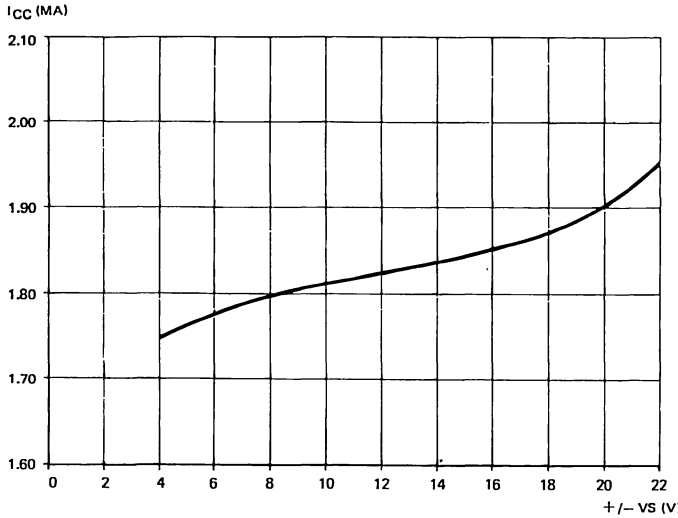
ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	TEB 4033 TEF 4033 TEC 4033			Unit
		Min.	Typ.	Max.	
THD	Total Harmonic Distortion (f = 1KHz, A_v = 20 dB, R_L = 2 kΩ $C_L \leq$ 100 pF, T_{amb} = 25 °C, V_o = 2 V_{pp})		0.008	0.05	%
V_n	Equivalent Input Noise Voltage (f = 1 KHz) R_S = 50 Ω R_S = 1 kΩ R_S = 10 kΩ		 8 10 18	 15	 nV/√Hz
V_{OPP}	Large Signal Voltage Swing R_L = 10 kΩ, f = 10 KHz	26	28		V
φM	Phase Margin		45		Degrees
V_{o1}/V_{o2}	Channel Separation	100	120		dB



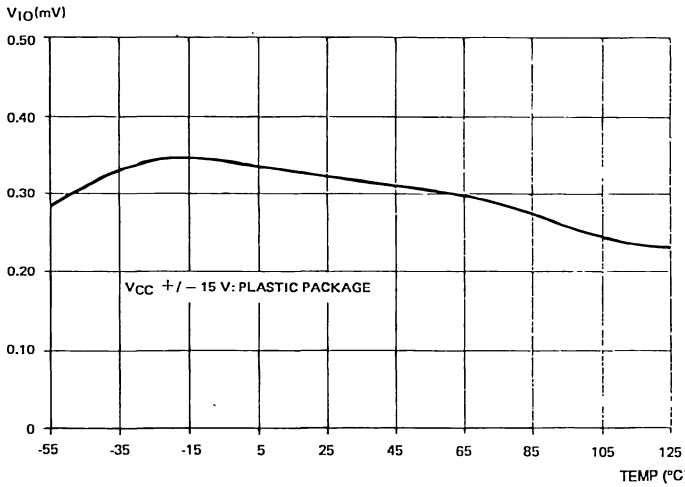
SUPPLY CURRENT VS. AMBIENT TEMPERATURE

E88TEB4033-02



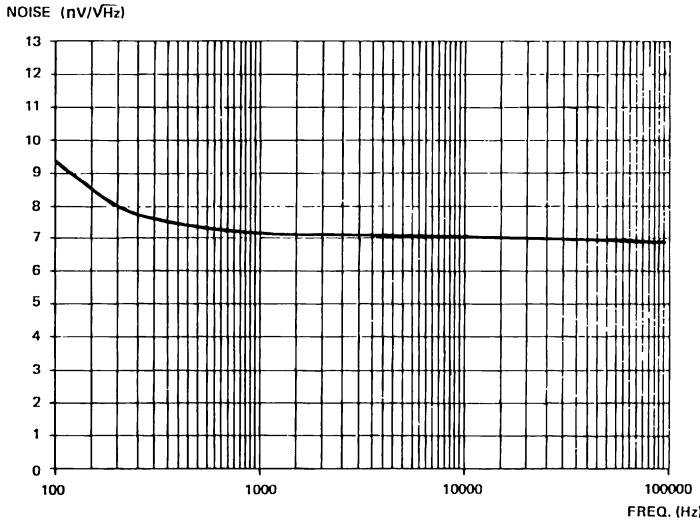
SUPPLY CURRENT VS. SUPPLY VOLTAGE

E88TEB4033-03



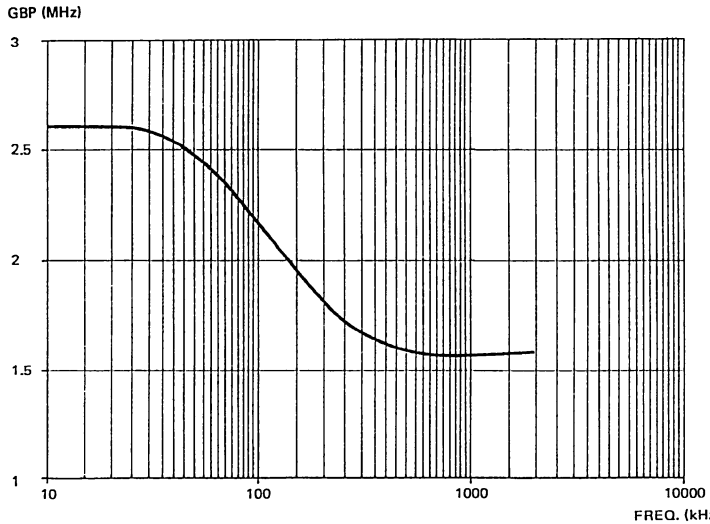
OFFSET VOLTAGE VS. AMBIENT TEMPERATURE

E88TEB4033-04



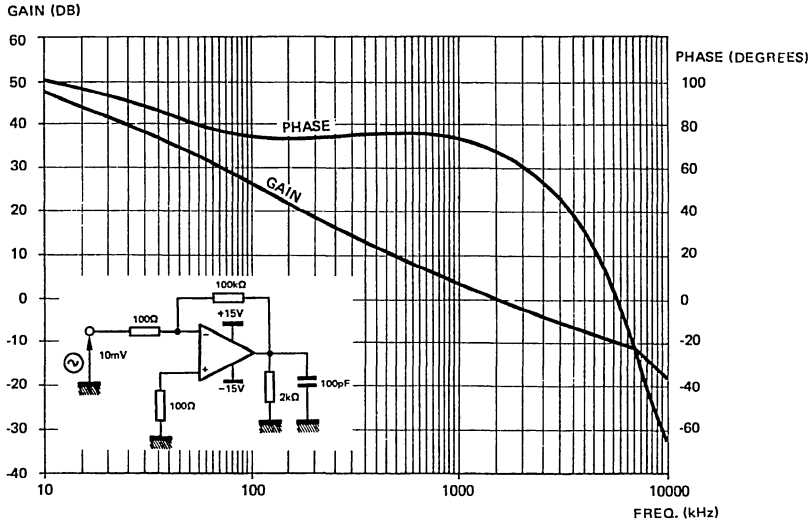
TOTAL INPUT NOISE VS. FREQUENCY

E88TEB4033-05



GAIN BANDWIDTH PRODUCT VS. FREQUENCY

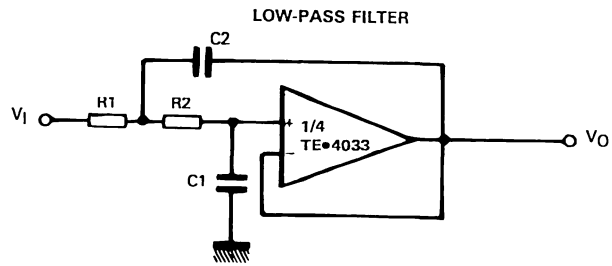
E88TEB4033-06



BODE PLOT

E88TEB4033-07

TYPICAL APPLICATION



E88TEB4033-08

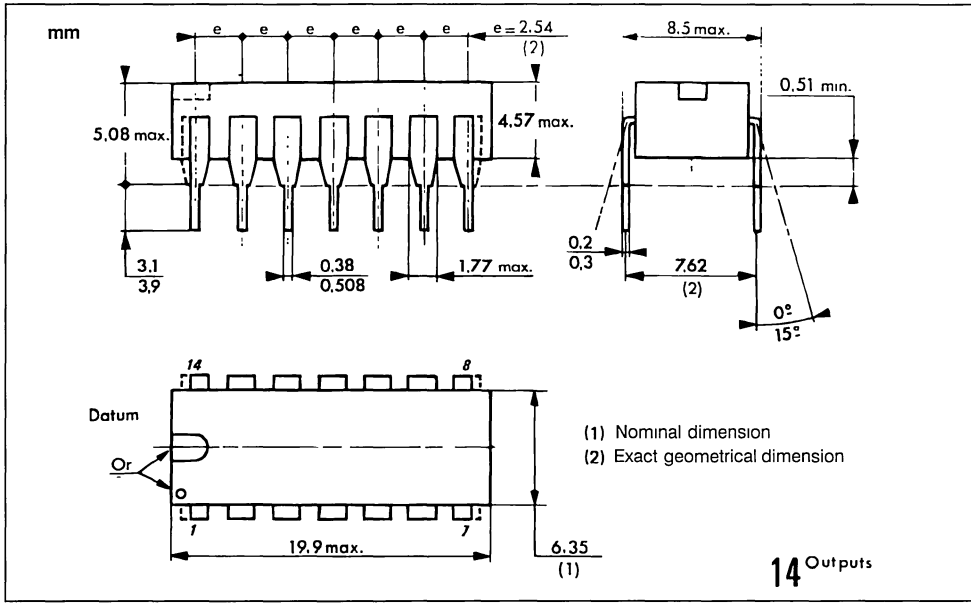
$$\frac{V_o}{V_i} = \frac{1}{1 + 2\xi\frac{S}{\omega_c} + \frac{S^2}{\omega_c^2}}$$

$\omega_c = 2\pi f_c$, with f_c = cutt-off frequency

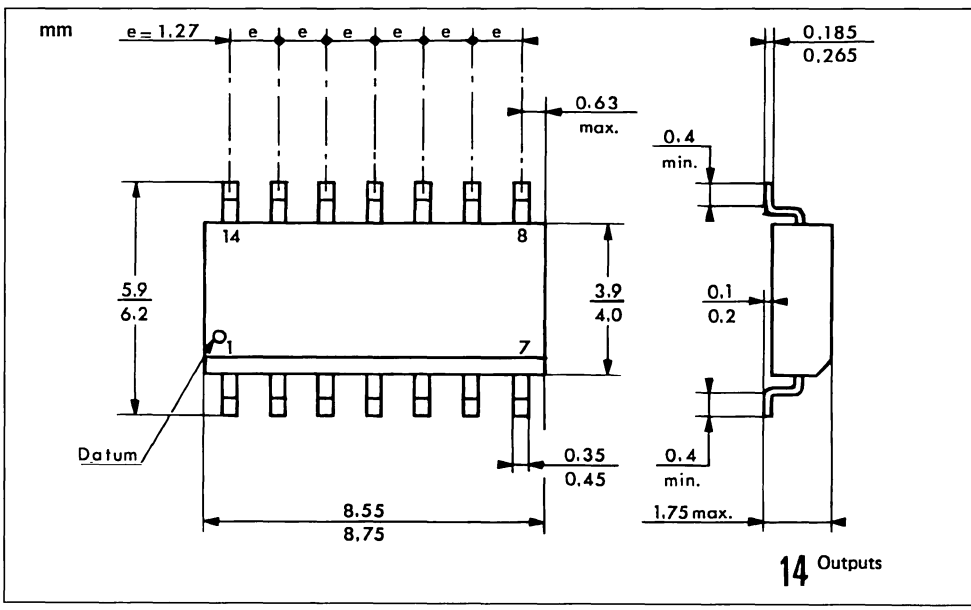
ξ = damping factor

PACKAGE MECHANICAL DATA

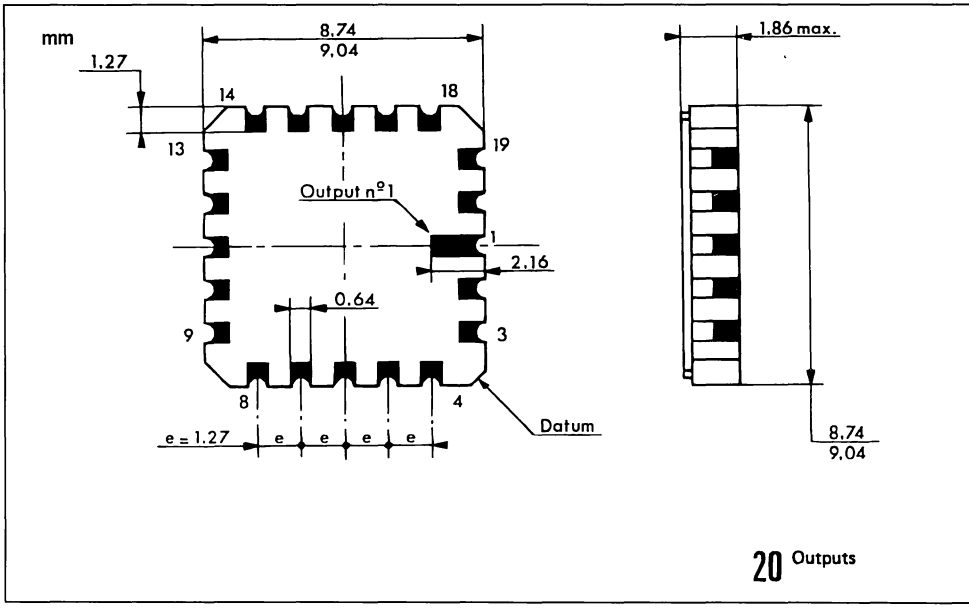
14 PINS – PLASTIC DIP OR CERDIP



14 PINS – PLASTIC MICROPACKAGE (SO)



20 PINS – TRICECOP (LCC)



SGS-THOMSON MICROELECTRONICS

TSGF SERIES

MASK PROGRAMMABLE FILTERS ANALOG SWITCHED CAPACITOR FILTER ARRAYS

- HCMOS MASK PROGRAMMABLE SWITCHED CAPACITOR FILTERS : FAST DESIGN TURN-AROUND TIME (5 to 6 weeks average), THANKS TO GATE ARRAY APPROACH
- INTEGRATION OF ANY KIND OF CLASSIC, NON-CLASSIC FILTERS : BANDPASS, LOW-PASS, HIGHPASS, BAND REJECT...
- CAUER, CHEBYCHEV, BUTTERWORTH, LEGENDRE...
- FILTER ORDER : FROM 2ND TO 12TH
- CASCADABLE STRUCTURE : HIGHER ORDER ACHIEVABLE
- NO EXTERNAL COMPONENTS REQUIRED TO REALIZE THE FILTERING FUNCTION
- ADDITIONAL OPTIONS AVAILABLE ON CHIP :
  - UNCOMMITED OP-AMPS (for anti-aliasing and/or smoothing filters, half or full wave rectifiers...) ;
  - INTERNAL DIVIDER (sampling frequency generated from external clock) ;
  - OUTPUT SAMPLE-AND-HOLD
- TSGF SERIES PROVIDES :
  - LEAPFROG STRUCTURE FOR VERY LOW SENSITIVITY FILTERS ;
  - CASCADABLE BIQUADRATIC CELLS FOR NON-CLASSIC FILTER DESIGN
- TSGF SERIES FULLY SUPPORTED BY "FILCAD"® CAD SOFTWARE FROM FILTER SYNTHESIS AND SIMULATION UP TO LAYOUT
  - APPLICATION NOTES
  - EVALUATION BOARDS
  - INPUT SIGNAL FREQUENCY : 0 TO 30KHz
  - SIGNAL TO NOISE RATIO : 60 TO 85dB
- POWER SUPPLY : DUAL ± 5V
  SINGLE 0 - 10V
  SINGLE 0 - 5V
- ADJUSTABLE POWER CONSUMPTION : 0.5mW TO 20mW PER FILTER ORDER
- QUALITY FACTOR : UP TO 50
- PASS-BAND GAIN : UP TO 40dB
- INPUT SENSITIVITY : 1mVRMS (min)

DESCRIPTION

TSGF series is a family of Mask Programmable Filters (MPFs) developed by SGS-THOMSON Microelectronics.

The TSGF product range is composed of 3 switched capacitor filter base arrays, TSGF04, TSGF08 and TSGF12 providing filter integration capability from 2nd to 12th order.

TSGF04/08/12 are using "gate array" technique : the filter customization is achieved only by the final metallization mask.

Therefore TSGF series provide users with filter integration solutions with very fast design turn-around time : 5 to 6 weeks up to delivery of full tested prototypes.

TSGF04/08/12 base arrays provide on chip all necessary functions to realize all kind of filters :

- transconductance amplifiers
- switches
- capacitor fields
- sample-and-hold
- non overlapping phase generator

Additional on-chip integration capabilities are offered by TSGF products such as :

- prefiltering and post filtering functions antialiasing and smoothing filters)
  - cosine filter
  - output sample-and-hold driving
  - power consumption adjustment
  - output DC level adjustment.

TSGF series provide users a fast and complete design solution for their specific filter circuits resulting in highly accurate and reliable products thanks to switched capacitor technique.

But SGS-THOMSON filtering approach is not only limited to the Mask Programmable Filter (MPF) products.

TSGF SERIES PRODUCT RANGE

Part Number	Number of on-chips Filters	Filter Order	Uncommitted Op-amps	Clock	Output Sample-and Hold	Packages
TSGF04	1	2 to 4	1	Internal Oscillator* TTL/CMOS Levels	External* Driving	PDIP 8-14 Pins CDIP 14 Pins SO Wide 16 Pins
TSGF08	1	4 to 8	2	1 Clock Input TTL/CMOS Levels	Internal Driving	PDIP 8-16 Pins CDIP 16 Pins SO Wide 16 Pins
TSGF12	1 or 2	8 to 12	2	2 Clock Inputs TTL/CMOS Levels	External* Driving	PDIP 16-18-20 Pins CDIP 16-18-20 Pins SO Wide 18-24 Pins

* Optional.

Users are given :

- Standard Device Filters which are general purpose filters designed by SGS-THOMSON from the 3 TSGF base arrays.
  - TSG 87xx developed on TSGF04 filter array (2nd to 4th order)
  - TSG 85xx developed on TSGF08 filter array (4th to 8th order)
  - TSG 86xx developed on TSGF12 filter array (8th to 12th order).

Refer to data sheets of these standard filter products.

- "Gate Array" Filters which are the TSGF04, TSGF08, TSGF12 filter arrays described in this data sheet.
- "Standard Cell" Filters described in the TSGSM Series Data Sheet.

By offering TSGF-like macrocells in its library, the mixed analog/digital TSGSM Standard Cell family also provides filtering capabilities and then can extend integration possibilities offered by TSGF series.

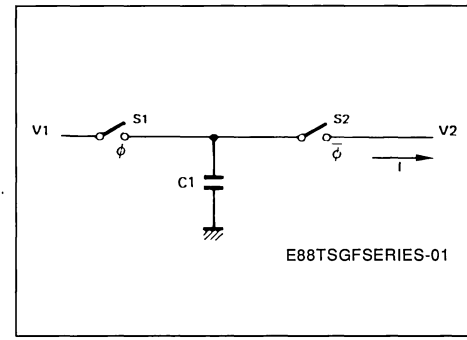
For example higher than 12th order filters or circuit combining filters with digital and analog functions on the same chip are achievable with TSGSM Standard Cells.

SWITCHED CAPACITOR TECHNIQUE

SGS-THOMSON TSGF products are active filters where resistors are replaced by capacitors which are switched at a frequency, named sampling frequency (F_i).

Figure 1 is showing the basic principle of switched capacitor technique.

Figure 1.



The 2 switches (S1 and S2) are controlled by 2 complementary and non overlapping clock phases.

During the phase $\varnothing = 1$ (S1 on, S2 off) the charge stored in C1 is :

$Q1 = C1.V1$ (1)

During the phase $\overline{\varnothing} = 1$ (S1 off, S2 on) the charge stored in C1 becomes :

$Q2 = C1.V2$ (2)

During a complete clock period $Ti = \frac{1}{Fi} = \varnothing + \overline{\varnothing}$

the transferred charge is :

$\Delta Q = Q1 - Q2 = C1\ (V1 - V2)$ (3)

During this Ti period, this charge flow is equivalent to a current, I :

$\Delta Q = C1\ (V1 - V2) = I.Ti$ (4)

$$I = C1.Fi\,(V1 - V2) = \frac{C1\,(V1 - V2)}{T_i} \quad (5)$$

Comparing (5) with Ohm's law applied to a resistance :

$$I = \frac{V1 - V2}{R} \quad (6)$$

The equivalent resistor is then :

$$Req = \frac{T_i}{C1} \quad (7)$$

Then, with (7), a RC product becomes :

$$Req.\,C = \frac{C}{C1}\,T_i \quad (8)$$

product but the component values R and C used with the Op-amp are absolutely uncorrelated : so trimmings, tunings are very often needed to obtain an accurate template. On the other hand, with switched capacitor networks, only capacitor ratios are used. These ratios are obtained with capacitors integrated on the same chip. The available accuracy is 0.1% to 0.5% whatever the temperature condition may be.

As the time constant is fixed by capacitor ratio, fully integrated filters are achievable without trimming. In addition, as shown in (8) the time constant RC is proportional to the sampling period Ti : the filter cutoff frequency can be shifted by tuning the sampling clock frequency without any change on the shape of response curves.

SWITCHED CAPACITOR FILTER BENEFITS

In active filters, the time constant is fixed by the RC

SWITCHED CAPACITOR FILTER FEATURES

Key Points	Results
• Monolithic Filter. • The coefficients of the filter transfer function are completely determined by : – a single crystal controlled clock frequency – and ratioed capacitors • Fully HCMOS Integrated Filters • Switched capacitor filters are sampled-and-hold circuits.	• Board Size Reduction. • High Accuracy Template. • Stability in Temperature and Time. • High Order Filter Achievable. • No Adjustment. • Clock Tunable Cutoff Frequency. • Low Power. • No External Components. • Ease and Safety of Use. • Antialiasing prefiltering is required if the input signal is wide band. • Smoothing post filtering may be used to avoid spectral rays around the sampling frequency.

SWITCHED CAPACITOR FILTER ARRAY ARCHITECTURE

Analog switched capacitor filter arrays, TSGF series, are processed with a 3.5/2 polysilicon layer/1 metal layer HCMOS process.

SGS-THOMSON offers 3 filter base arrays, TSGF04, TSGF08 and TSGF12, providing filtering capabilities from 2nd to 12th order.

The 3 arrays are designed around a "Universal biquadratic filter cell", SGS-THOMSON patented. This cell consists of 2 adder integrators using a transconductance amplifier, switches, and capacitor fields. Fields of capacitors are composed of hundred unit capacitors (0.1pF) and then provide high and accurate capacitor values.

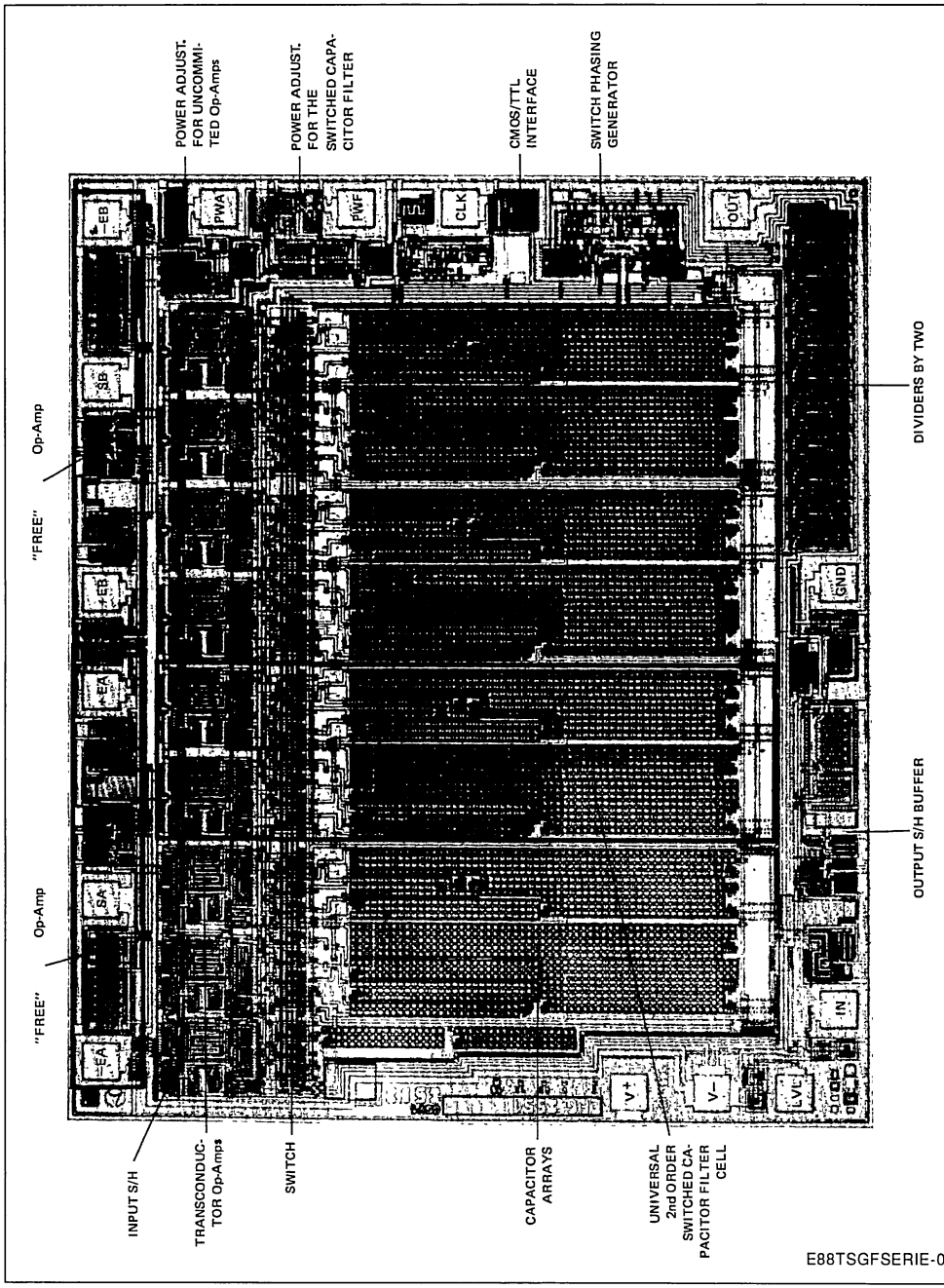
Figure 2 shows the TSGF08 chips, outlining all functions available on TSGF filter arrays :

- Universal 2nd order Filter Cell. Clock divider generating internal sampling frequency from external clock.
- Non overlapping phase generator.
- Input Sample-and-Hold.
- Uncommitted free Op-amps. Power consumption Adjustment cells for filter and Op-amps.
- Output Sample-and-Hold.

The internal sampling frequency Fi can be set from 500Hz to 700KHz by an external oscillator (or an internal one with TSGF04 base wafer).

When the external available clock frequency is

Figure 2 : TSGF08 CHIP.



higher than 700KHz, the set of Mask Programmable dividers by 2 is used to adapt the external clock frequency to the sampling frequency. In any case the external clock frequency must be lower than 5MHz.

As the ratio Fi/Fc between sampling frequency Fi and selected filter frequency Fc is a constant, designers can move the filter characteristics (central or cut-off frequency) only by tuning the clock.

A 10V power supply, either 0V and 10V, or - 5V and + 5V, gives the best performances : maximum output swing of 8V. The TSGF filters can also operate with a standard 0/5V power supply. In that case the maximum output swing is 2.2V.

Typical power consumption is 0.5mA per filter order. This power consumption is user adjustable between 0.1mA and 2mA with an external resistor, depending on the frequency range.

The power consumption adjustment is also provided to the uncommitted operational amplifiers : the bias current must be increased when a high gain - bandwidth product is required.

These uncommitted Op-amps give the designer the capability to create auxiliary circuits like voltage gain, prefiltering and post filtering functions half or full wave rectifier functions, or local oscillator (refer to application notes AN-061, AN-069, AN-070, AN-075).

The offset voltage of TSGF products is typically a few millivolts, with a 300mV max depending of the filter type.

Moreover, there is a possibility to adjust the filter output DC levels, thanks to an external bias voltage applied on "LVL" pin. Automatic offset compensation can be done by mean of one uncommitted on-chip operational amplifier, as indicated in Application note AN-069.

The TSGF products feature a high input impedance (typ. : 3MΩ) and a low output impedance (typ. : 10Ω) allowing then cascadable filter network in order to achieve higher than 12th order.

The output buffers are configurated as sample-and-hold amplifiers which can drive a 1KΩ load resistance and a 100pF load capacitance.

On the TSGF04 and TSGF12 an external sample-and-hold clocking allows to connect the filter output directly to an analog to digital converter (Optional ; see fig. 7).

In addition some particular switched capacitor cells have been implemented on the first 2 integrators of each chip allowing realization of special functions like :

- cosine filter
- complementary high pass filter
- exact bilinear leapfrog filter.

Figure 3a : TSG8512 : 7th Order Cauer Low pass Filter.

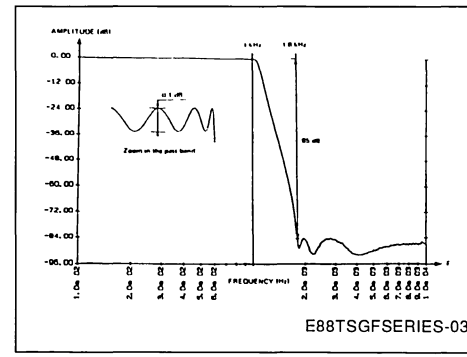
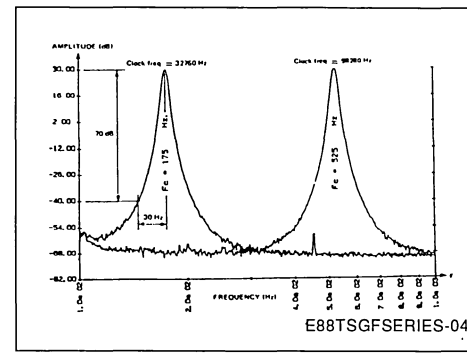


Figure 3b : TSG8551 : 8th Order High-Q Band pass Filter (Q = 35).



BENEFITS

With the TSGF series of SGS-THOMSON, designers are given unique "Gate Array" filter products for the replacement of their passive/active filters or the design of new filters.

The TSGF04/08/12 provide then with gate Array technique 3 complete arrays where all functions necessary to realize the filter function and its external circuit environment are available on chips.

The switched capacitor process permits the realization of very accurate and fully integrated filters and breaks down the equipment production costs by providing fully tested filters parts : tuning or adjustment of external components are no more ne-

cessary with TSGF series.

Figures 3A, 3B is showing 2 examples of Standard Filters designed with the TSGF08 matrix.

APPLICATIONS

TSGF products from SGS-THOMSON can integrate all filtering functions (replacement of active or passive filters...) and then can be implemented very quickly into an application/equipment requiring a filter with a maximum input signal frequency of 30KHz.

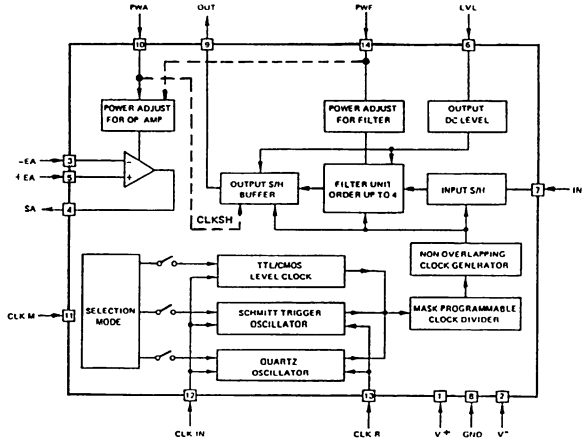
Mask Programmable Filters (MPFs) typical applications are :
- audio filtering/processing
- signal/frequency detection
- scrambling/coding
- spectrum analysis
- process control
- remote control
- harmonic analysis
- equalization
- frequency tracking
- alarm systems
- robotics
- anti-knock system
- data acquisition (before A/D and after D/A converters)
- automatic answering
- inwarding
- speech processing
- security system (coding, recognition)
- sonar detection
- mobile radio
- modems

BLOCK DIAGRAMS

Figure 4 outlines the mean features and options offered by each of the 3 MPF arrays by showing TSGF04, TSGF08 and TSGF12 block diagrams.

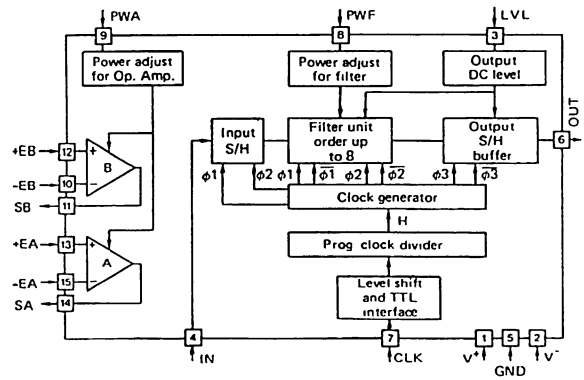
Figure 4 : Block Diagrams.

TSGF04



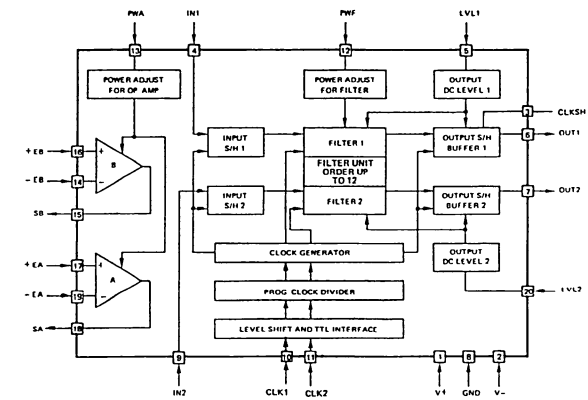
E88TSGF SERIES-05

TSGF08



E88TSGF SERIES-06

TSGF12



E88TSGF SERIES-07

PIN DESCRIPTION

The table below gives the pin description of the 3 MPF arrays, TSGF04 TSGF08 and TSGF12. The pin assignment is given for the extended and complete version of each array, it means with all the available on-chip options connected to the package.

Name	Pin Type	TSGF04 N°	TSGF08 N°	TSGF12 N°	Function	Description
V^+	I	1	1	1	Positive Supply	
V^-	I	2	2	2	Negative Supply	
LVL	I	6	3	LVL1 5 LVL2 20	Output DC Level Adjustment	Filter output DC level adjustment when connecting a potentiometer between V^+ and V^- with its middle point to LVL. When no adjustment is needed, LVL pin is connected to GND.
IN	I	7	4	IN1 4 IN2 9	Filter Input	
GND	I	8	5	8	General Ground	GND Voltage = $\frac{V^+ + V^-}{2}$
OUT	O	9	6	OUT1 6 OUT2 7	Filter Output	
CLK	I	See CLKIN	7	CLK1 10 CLK2 11	Clock Input	TTL/CMOS Level Compatibility
PWF	I	14	8	12	Filter Power Adjustment	Filter power consumption can be chosen by connecting a resistor between PWF and GND (or V^+). Stand by mode is obtained by connecting PWF to V^- (or non connected)
PWA	I	10*	9	13	Op Amp Power Adjustment	Idem PWF but for Op Amp (PWA)
–EB	I		10	14	Inverting Input Op Amp B	
SB	O		11	15	Output Op Amp B	
+EB	I		12	16	Non Inverting Input Op Amp B	
+EA	I	5	13	17	Non Iverting Input Op Amp A	
SA	O	4	14	18	Output Op Amp A	
–EA	I	3	15	19	Inverting Input Op Amp A	
NC			16		Non Connected	
CLKSH	I	10*		3	S/H Clock Input	External Driving Clock of Output Sample-and-hold
CLKIN	I	12			Clock Input	See TSGF04 Clock Oscillator Section
CLKR	O	13			Clock Pin for External Oscillator	For TSGF04, external RC or crystal oscillator are connected to CLKIN and CLKR pins. See TSGF04 clock oscillator section
CLKM	I	11			Clock Selection Mode	Connected to GND or V^- see TSGF04 clock oscillator section

* For TSGF04 when external driving clock of output sample-and-hold (CLKSH) is used, PWF realizes the power adjustment of both uncommitted Op-amp and filter.

Note : For other packing pin-out, refer to package drawings and pin-out at the end of data sheet.

FUNCTIONAL DESCRIPTION

INTERNAL CLOCK DIVIDER (CLK)

The internal sampling frequency F_i can be fixed from 500Hz to 700KHz (F_i can be used between 700KHz and 1MHz with some limitations) by an external oscillator (or internal one with TSGF04 filter array). When the external clock frequency F_e, is higher than 700KHz, a mask programmable on-chip divider is used to adapt available clock frequency to the sampling rate.

	TSGF04	TSGF08	TSGF12
Number of Divide by 2 Available Per Chip	8	10	8
Max. F_e/Fi Ratio	256	1024	256

In any case, the external clock frequency F_e must be less than 5MHz.

Example : The TSG8510 features (TSG8510 is a standard filter based on TSGF08 array) :

F_e max = 1.5MHz and F_i max = 750KHz then

$$\frac{F_e}{F_i} = 2$$

only one divider by 2 is used for this filter (which is the case of most of SGS-THOMSON' general purpose filters).

Note : As the internal clock divider is mask programmable, the ratio F_e/F_i is fixed for each filter. The change of this ratio is possible but results into a new part number.

ADJUSTMENT OF OUTPUT DC LEVEL (LVL)

The output DC offset voltage can be removed thanks to an external bias voltage applied on "LVL" pin, as shown on figure 8.

However automatic offset compensation can be implemented by using one of the uncommitted on-chip Op-amps, as indicated in application note AN-069 (see fig. 9 in AN-069).

The offset voltage of TSGF filters is typically a few millivolts, with a 300mV max, depending on the type of the filter.

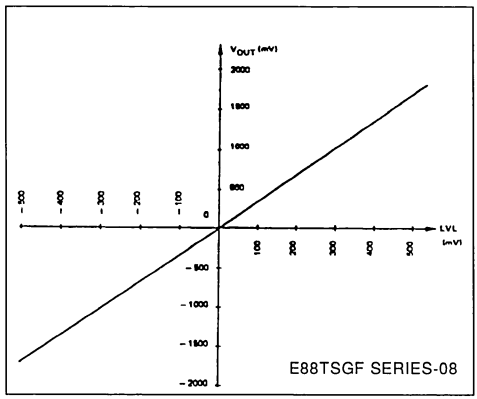
A drift of this offset voltage can be observed when user increases the power consumption of the filter with an external resistor connected to PWF pin. So when the filter operates at high frequencies, a compromise exists between the filter frequency response performance and its output DC offset voltage.

When no DC output level adjustment is required, LVL pin has to be connected to the GND voltage.

The level gain, LG, of each filter can be deduced from the curve representing V_{OUT} = f (LVL). This curve is filter dependent.

For example the TSG8510 presents following curve shown in figure 5 (measured with F_e = 256KHz, I_{PWF} = 100µA) :

Figure 5 : Output DC Voltage Adjustment from LVL Pin.



The TSG8510's level gain is :

$$LG = \frac{V_{OUT}}{LVL} \cong \frac{1000}{300} \cong 3.3$$

For example if one TSG8510 presents a 100mV offset voltage at its output, user must apply an external bias voltage LVL = 30mV to compensate it.

FILTER POWER ADJUSTMENT (PWF)

The filter power consumption can be chosen by connecting an external resistor, R_{PWF} between PWF and GND (or V+) pins.

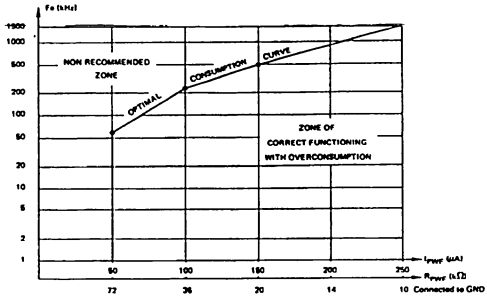
This power adjustment operates the variation of the bias current of the integrators used in the switched capacitor filter. This current, I_{PWF}, can be low when filter operates at low cut-off frequencies ($F_c \cong 1$KHz), but must be increased at high cut-off frequencies ($F_c \cong 20$KHz), in order to charge and discharge the capacitors at a higher rate.

As a result, an optimal choice of I_{PWF} bias current can be deduced from the curve representing I_{PWF} = f (F_e), F_e being the external clock frequency applied on CLK pin.

This curve is dependent on the filter. For example, as shown in figure 6, the TSG8510 presents following characteristics :

Example : if the cutoff frequency of the low pass TSG8510 filter has to be set at 3.4KHz, user must apply the external clock frequency F_e = 75.3 x 3.4 = 256KHz.

Figure 6 : TSGF10 user's Guide for IPWFand RPWF Choise.



E88TSGFSERIES-09

The User's guide for I_{PWF} choice indicates :

- optimal I_{PWF} = 100µA
  R_{PWF} = 35kΩ
- non recommanded zone for I_{PWF} 100µA
  Operation within this area can lead to increase the ripple in the pass band and to decrease the stop band attenuation.
- zone of correct functioning with over consumption for I_{PWF} > 100µA.

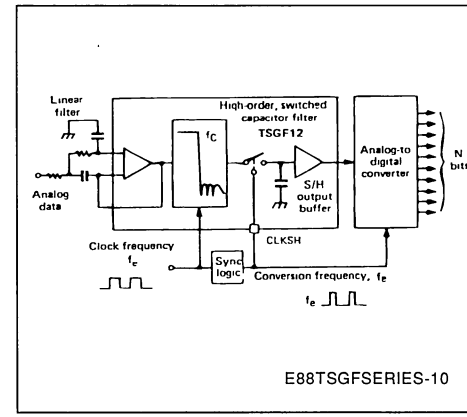
Note : Power consumption choice has to be prioritized when major concern in TSGF design is the frequency response (gain versus frequency). The output DC offset voltage comes in 2nd position in that case.

EXTERNAL DRIVING OF OUTPUT SAMPLE-AND-HOLD

This facility allows the filter output to be connected directly to an analog-to-digital converter, as illustrated in figure 7.

The clock signal which enters on the CLKSH pin must be synchronous with the sampling frequency. As a result, the external clock frequency F_e must be the sampling frequency F_i (the on-chip divider does not have to be used).

Figure 7 : External Driving of Output Sample and Hold (example).



E88TSGFSERIES-10

The clock signal applied on CLKSH pin has to be optimized in order to read a settled signal issued from the switched capacitor filter.

On the example shown in figure 7, a 12th order low pass filter makes an ideal antialiasing filter to precede data conversion. The filter precludes the need for oversampling when driving the A/D converter.

CLKSH option is only available on TSGF04 and TSGF12 arrays.

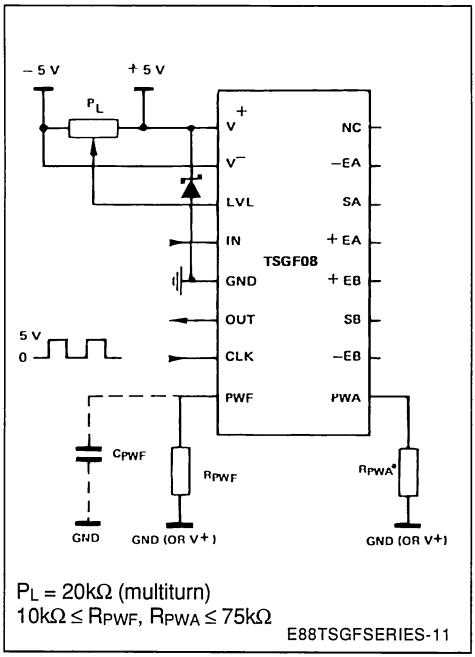
USE OF THE MPF WITH - 5V/+5V DUAL POWER SUPPLY

The adjustment of the DC output level of the M.P.F. is achieved by an external voltage source (for example, a bridge divider connected between the positive and the negative power supplies and whose the middle point is connected to the LVL pin of the M.P.F.). If no output DC adjustment is required, the LVL pin can be directly connected to GND.

The consumption of the filter can be also adjusted by means of an external resistance connected between GND (or V^+) and the PWF pin of the circuit.

The consumption can thus be chosen to match the particular application.

Figure 8 : Example of a TSGF08 Fed in Dual Supply : +5V, 0, -5V.



P_L = 20kΩ (multiturn)
10kΩ ≤ R_{PWF}, R_{PWA} ≤ 75kΩ

E88TSGFSERIES-11

If the Op-Amps are not used, RPWA has not to be connected between PWA and GND.

The stand-by mode is obtained by strapping the PWF pin to V^- (or non connected).

The adjustment of the power consumption of the two operational amplifiers can be achieved exactly like for the previous case, but via the PWA pin of the circuit. The stand-by mode is also obtained by strapping the PWA pin to V^- (or non connected).

The clock levels are TTL, but CMOS levels are accepted. With these previous conditions, the output linear dynamic range of the M.P.F. is about 8V, between - 4.5V and + 3.5V.

A capacitor C_{PWF} can be added in parallel with R_{PWF} in order to improve the clock feedthrough rejection : (Typical value C_{PWF} = 33pF).

As for all CMOS circuits operating with dual power supply (- 5V, 0, + 5V), it is advised to use clamping diodes (Threshold voltage less than 0.6V) (Schottky is preferrable) in order to avoid transients during power up which could drive TSGF circuits over their maximum ratings. Only 1 Schottky diode between GND and V+ is sufficient for TSGF products.

USE OF THE MPF WITH 0/10V SINGLE POWER SUPPLY

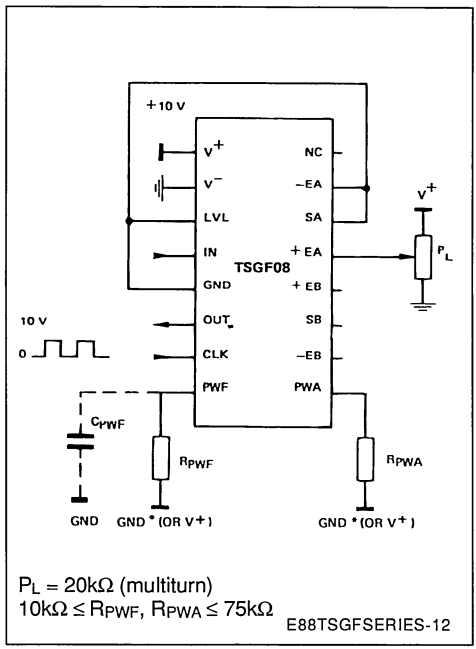
In this case, V^- is the reference ground of the circuit and GND must be adjusted to + 5V by means of the potentiometer P_L (V_+ - V^-)/2), or by using a simple bridge divider. But in that case small resistors values (2kΩ) have to be used in order to set GND at a low impedance value.

The adjustments of the DC output level of the M.P.F. of the power consumptions of the filter and of the operational amplifiers can be achieved exactly like previously.

The high level of the clock must be at least 1.4V upper the GND level.

With these previous conditions, the output linear dynamic range of the M.P.F. is about 8V between 0.5 and 8.5V.

Figure 9 : Example of a TSGF08 FED, in Single Power Supply 0 - 10V.



P_L = 20kΩ (multiturn)
10kΩ ≤ R_{PWF}, R_{PWA} ≤ 75kΩ

E88TSGFSERIES-12

* GND is used, when the user provides the 5V voltage.

USE OF THE MPF WITH 0/5V SINGLE POWER SUPPLY

In this case, V^- is the reference ground of the circuit

and GND must be adjusted to + 2.5V by means of the potentiometer P_L ((V+ - V⁻)/2), and one Op-amp used as buffer in order to provide a low impedance on GND reference.

Otherwise, without Op-amp, a simple bridge divider is sufficient, but small resistor values (2kΩ) have to be used in order to set GND at a low impedance value.

The other adjustments are achieved exactly like previously except for bias resistance of the filter and of the operational amplifiers (R_{PWF} and R_{PWA}), whose must be exclusively to V+.

The clock levels must be CMOS levels. With these previous conditions, the output linear dynamic range of the M.P.F. is about 2.2V, between 1.2 and 3.4V.

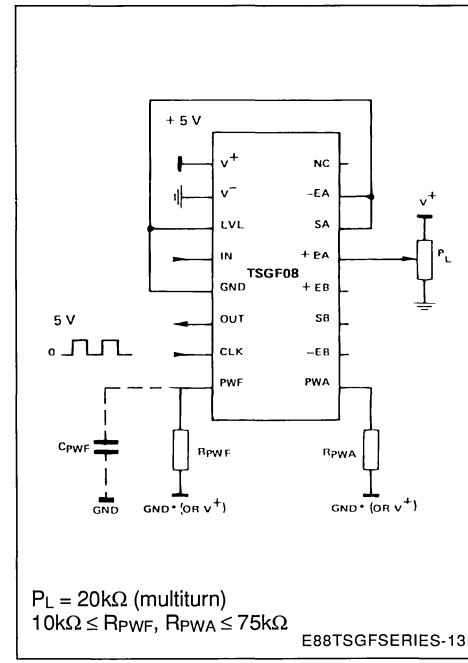
ANTI-ALIASING AND SMOOTHING

Anti-aliasing : The switched capacitor filters are sampled systems and must verify the SHANNON condition imposing a sampling frequency (F_i) equal, at least, to the double of the upper frequency (F_c) contained in the spectrum to transmit. With this condition, no information is added or lost on the transmitted signal. This theorem describes the well-known phenomenon called spectrum aliasing shown figure 11 where the entire spectrum to transmit appears around F_i, 2 F_i, 3 F_i... and so on.

Thus, all spectrum components of the signal contained around these frequencies are transmitted by the M.P.F., oppositively to the desired result.

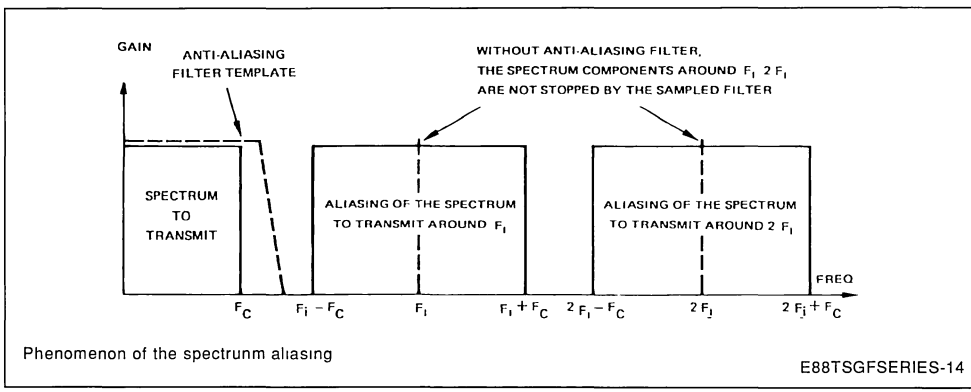
To cancel the effects of this phenomenon, it is required, before all sampled systems, to filter all the spectrum components of the intput signal upper than F_i - F_c. An analog filter, called "anti-aliasing filter", must be therefore applied before the M.P.F.

Figure 10 : Example of a TSGF08 FED in Single Power Supply 0-5V.



*GND is used, when the user provides the 2 5V Voltage.

Figure 11.



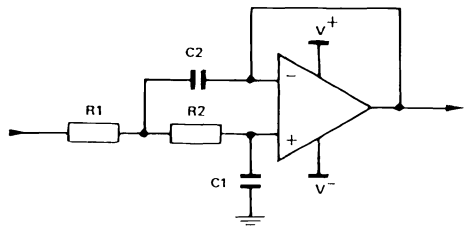
- Without anti-aliasing filter . Spectrum to transmit ≠ transmitted spectrum
- With anti-aliasing filter Spectrum to transmit = transmitted spectrum

The selectivity of this filter depends upon the F_i/F_c ratio.

If F_i/F_c 200, a RC filter (first order low-pass) is sufficient.

If F_i/F_c 200, a SALLEN-KEY structure (second order low-pass) must be used. This structure and its relationships are described (figure 12). In these relationships, F_c is the cut-off frequency desired of the anti-aliasing filter and ξ its damping coefficient. For a cut-off as tight as possible and in order to correct the sin x/x effect, ξ must have a value around 0.7.

Figure 12.



E88TSGFSERIES-15

R1 = R2 = arbitrary value
F_c = cut-off frequency for the antialiasing filter.
An optimal choice is Fc = 2 x cut-off frequency of the main filter
ξ = damping coefficient ; the optimal value is 0.7

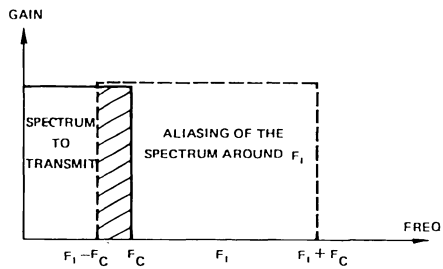
$$C1 = \frac{\xi}{2\pi R1 Fc}$$

$$(C1 = \xi 2 - C2)$$

$$C2 = \frac{1}{2\pi\xi R1 Fc}$$

SALLEN-KEY structure (second order low-pass Filter) for anti-aliasing and smoothing.
Note : If F_i/F_c 2 (figure 13), the spectrum to transmit and the spectrum aliased have a part in common and it becomes impossible to share the useful signals from the undesirable signals.

Figure 13.



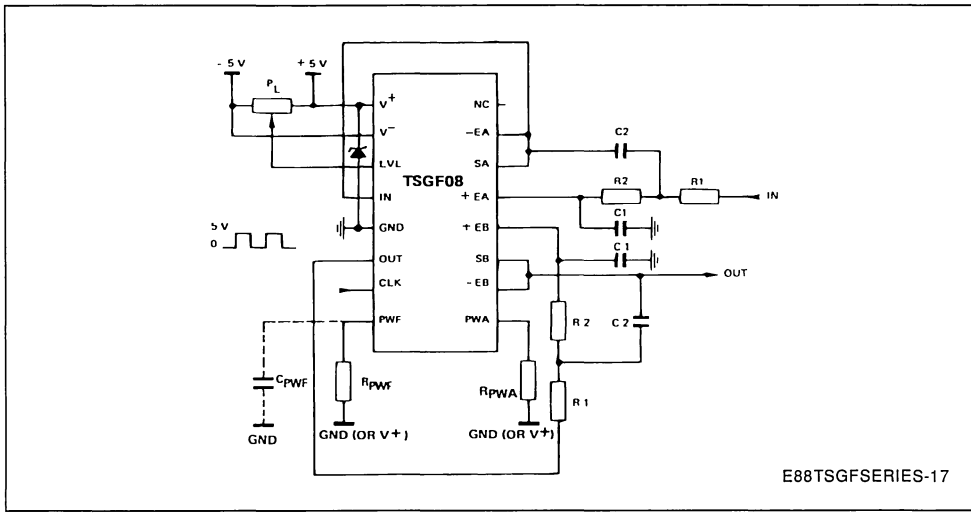
E88TSGFSERIES-16

When Fi/Fc<2, the spectrum component included between Fi-Fc and Fc and which are due to spectrum aliasing are not stopped by the sampled filter.

- Smoothing : As the signal obtained at the output of the M.P.F. is a sampled and hold signal, it is often required to smooth it. This smoothing filter can be achieved from the SALLEN-KEY structure previously described (figure 12).
- Hardware implementation : In order to make easier anti-aliasing and smoothing. SGS-THOMSON has designed, on the TSGF chip one or, two general purpose operational amplifiers. A few external components are therefore sufficient to achieve these functions (figure 14).

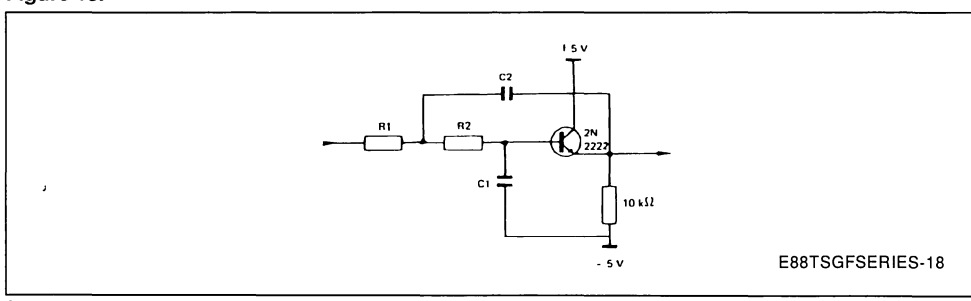
On the other hand, in the most of M.P.F.'s, a spe cial integrated cell is included in the chip (cosine filter) to reduce the aliasing effects around F_i.

Figure 14.



M.P.F. With anti-aliasing and smoothing filters.
P_L = 20kΩ (multiturn)
10kΩ ≤ R_{PWF}, R_{PWA} ≤ 75kΩ
R1,R2,C1,C2 } See anti-aliasing
R'1, R'2,C'1,C'2 } and smoothing considerations

Figure 15.



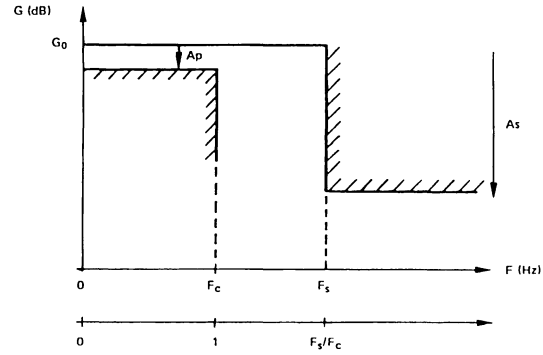
Second order low-pass Filter (SALLEN-KEY STRUCTURE) with a transistor replacing the operational amplifier.

Nonetheless, if the application allows it, these two operational amplifiers can be used to implement other functions (gain, comparator, oscillator...).

In this case, the circuit shown figure 15 can be used as anti-aliasing or smoothing filter. This structure is the same as the SALLEN-KEY structure described figure 12 (second order low-pass), in the same way as the corresponding relationships.

CUT-OFF FREQUENCY DEFINITION

Figure 16 : Design Specifications.

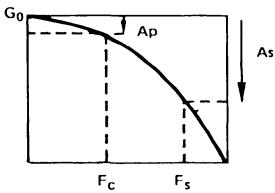


E88TSGFSERIES-19

The cut-off frequency F_c is the passband limit frequency as defined on the design specifications above mentioned. The maximum value of the attenuation variation in the passband : Ap is 3dB for Butterworth, Bessel and Legendre filters (figure 17a), and is called passband ripple for Chebychev (figure 17b) and Cauer filters (figure 17c).

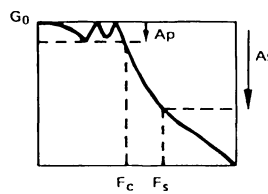
The passband ripple is design dependent and between 0.05dB and 0.2dB with TSGF standard filters. The parameters G_o called passband gain is the maximum value of the gain in the passband, and may have low variation from part to part.

Figure 17a.



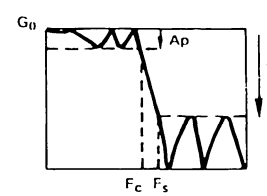
E88TSGFSERIES-20

Figure 17b.



E88TSGFSERIES-21

Figure 17c.



E88TSGFSERIES-22

ELECTRICAL SPECIFICATION

The following electrical characteristics are common to the 3 base filter arrays TSGF04, TSGF08 and TSGF12, because their structures are designed with the same basic components.

ABSOLUTE MAXIMUM RATINGS

T_{amb} = 25°C, V+ = 5V, GND = 0V, V– = – 5V, I_{PWF} = 100µA (unless otherwise specified)

Symbol	Parameter	Value	Unit
V+	Positive Supply Voltage	– 0.15 to + 7	V
V–	Negative Supply Voltage	– 7 to + 0.15	V
V	Voltage to any Pin (except for GND)	(V–) – 0.3 to (V+) + 0.3	V
T_{oper}	Operating Temperature Range	T_{min} – 5°C to T_{max} + 5°C	°C
T_{stg}	Storage Temperature Range	– 60 to + 150	°C

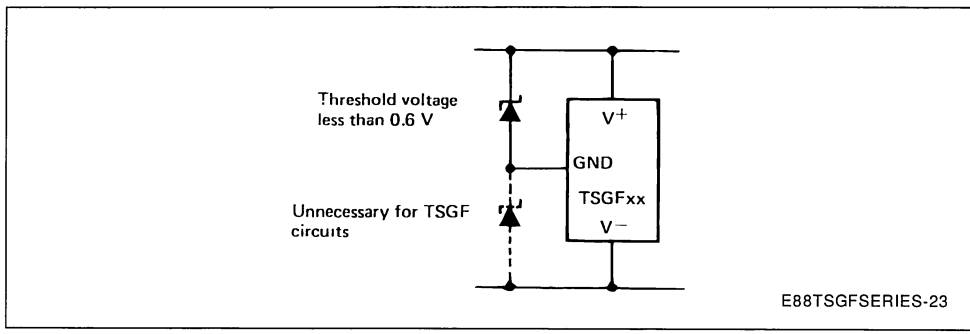
WARNING : DUAL POWER SUPPLY (- 5V, 0, + 5V)

Although TSGF circuits are internally gate protected to minimize the possibility of static damage, MOS handling and operating procedure precautions should be observed. Maximum rated supply voltages must not be exceeded. Use decoupling networks to remove power supply turn on/off transients, ripple and switching transients.

Do not apply independently powered signals or clocks to the chip with power off as this will forward bias the substrate. Damage may result if external protection precautions are not taken :

As for all CMOS circuits operating with three supply voltages (V+, GND, V-), it is advised to use clamping diodes (Schottky is preferable), in order to avoid transient during power up that would drive the circuit over its maximum ratings (see figure 18).

Figure 18 : Application Hint for CMOS ICs with Three Supply Voltages.



ELECTRICAL OPERATING CHARACTERISTICS

$V^+ = 5V$, GND = 0V, $V^- = -5V$, $T_{amb} = 25°C$, $I_{PWF} = 100\mu A$ (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V^+	Positive Supply Voltage	4	5	6	V
V^-	Negative Supply Voltage	−6	−5	−4	V
V_{OUT}	Output Voltage Swing (*)	$(V^-) + 0.5$		$(V^+) - 1.5$	V_{PP}
V_{IN}	Input Voltage (*) (with filter gain = 0dB)	$(V^-) + 0.5$		$(V^+) - 1.5$	V_{PP}
I_{PWF}	Bias Current on PWF (stand-by mode by connecting PWF to V^-)	50		250	µA
V_{IL}	TTL Clock Input "0" (**)			+ 0.8	V
V_{IH}	TTL Clock Input "1" (**)	2			V
T_{CP}	Ext. Clock Pulse Width	80			ns
R_{IN}	Input Resistance	1	3		MΩ
C_{IN}	Input Capacitance			20	pF
R_{OUT}	Output Resistance		10		Ω
C_L	Load Capacitance			100	pF
R_L	Load Resistance	0.1	1		kΩ

Note : with supply (0, + 10V) : same specifications
with single supply (0, + 5V) : contact SGS-THOMSON sales office or representative.
(*) Depending on I_{PWF} current
(**) TTL levels are referenced to GND voltage

Other filter's characteristics, such as noise, power supply rejection ratio, total harmonic distortion... are filter dependent. As a result, for such characteristics, SGS-THOMSON can only guarantee the lower level of performance for each parameter, as indicated below. (this lower level has been determined from measurements on a set of hundred different TSGF filters, as shown in figure 19).

PSRR + > 2dB : V+ Power supply rejection ratio.

PSRR − > 10dB : V^- Power supply rejection ratio.

V_n < 1mVrms : V_n is the total output noise voltage measured in the passband of the filter.

SNR > 57dBm/600 Ohm : Signal to noise ratio with V_{IN} = 775mVrms.

SNR > 65dBV : signal to noise ratio with V_{IN} = 2Vrms.

THD < 0.1% : Total harmonic distortion.

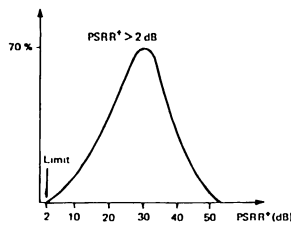
As such characteristics are not predictable from simulation results, their typical values are provided from measurements of the customized filter prototypes. (These measurements could be performed by SGS-THOMSON on special request).

These typical values, obtained with TSGF products, are better than the lowest level guaranteed, and designers can get a more accurate idea about them by two means.

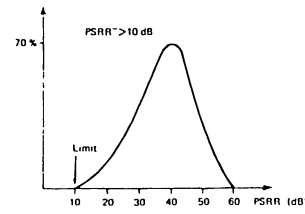
1) Such characteristics are given for general-purpose filters. Refer to TSG85xx, 86xx, 87xx data sheets.

2) Figure 19 gives histograms of the 5 parameters discussed above. These histograms indicate the distribution of the typical value of the considered parameter over a set of hundred different TSGF filters. (Note that the aim of these histograms indicate the dispersion of the considered characteristic for a given TSGF filter).

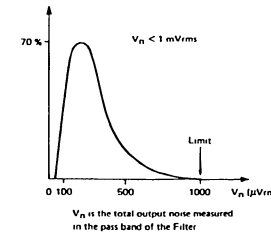
Figure 19 : Distribution of Typical Value Over a set of Hundred Different TSGF Filters.



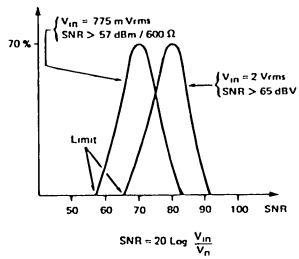
E88TSGFSERIES-24



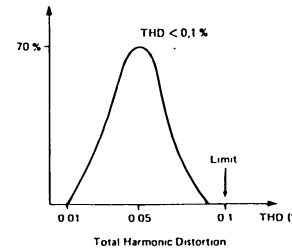
E88TSGFSERIES-25



E88TSGFSERIES-26

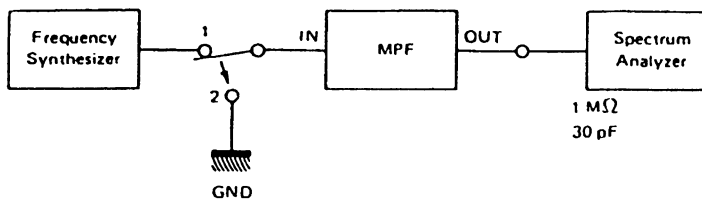


E88TSGFSERIES-27



E88TSGFSERIES-28

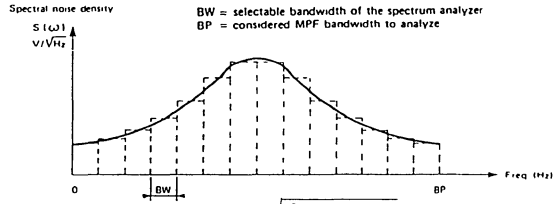
Figure 20 : Method of Noise Measurement.



Position 1 : Calibration of the spectrum analyzer to 0dBV (1Vrms).
Position 2 : Measurement with filter input connected to GND.

E88TSGFSERIES-29

Figure 20 : (continued).



We obtain theoretical noise voltage : $Vn(Vrms) = \sqrt{\int_0^{BP} S^2(\omega).d\omega}$

and measured noise voltage : $Vn(Vrms) = \sqrt{\sum_{k=1}^{BP/BW} S^2(k) \cdot BW}$

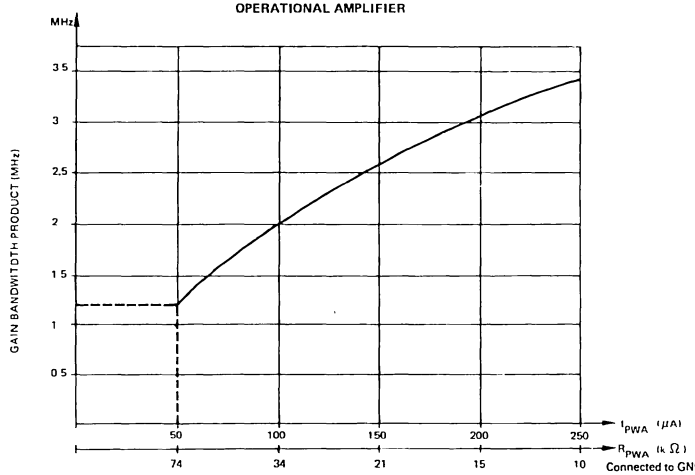
E88TSGFSERIES-30

UNCOMMITTED ON-CHIP OPERATIONAL AMPLIFIERS

$V^+ = 5V$, GND = 0V, $V^- = -5V$, $T_{amb} = 25°C$, RL = 2kΩ, $I_{PWA} = 100\mu A$ (unless otherwise specified)

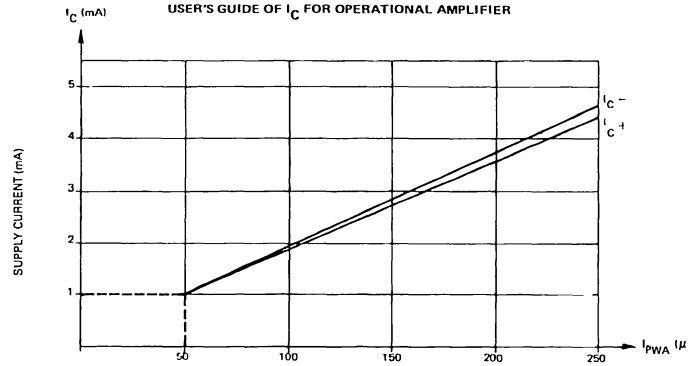
Symbol	Parameter	Min.	Typ.	Max.	Unit
G_0^+ G_0^-	DC Open Loop Gain (without load)	60 60	75 75		dB dB
G_{Bp}	Gain Bandwidth Product (without load)	1	2		MHz
V_{IO}	Input Offset Voltage (without load)		± 5	± 10	mV
$V_{OP}P$	Output Swing		− 4.5 3.5	− 4.7 3.7	V V
I_{IB}	Input Bias Current (without load)		± 5	± 10	nA
SVR	Supply Rejection (without load)	60	65		dB
CMR	Common Mode Rejection V_{CM} = 1V (without load)	60	65		dB
R_O	Output Resistance		10		Ω
Ia^+ Ia^-	Supply Current		2.6 2.6	3.2 3.2	mA mA
SR^+ SR^-	Slew Rate	2 2	5 6		V/µs V/µs

USER'S GUIDE OF I_{PWA} AND R_{PWA} FOR UNCOMMITTED ON-CHIP OPERATIONAL AMPLIFIER



E88TSGFSERIES-31

USER'S GUIDE OF I_C FOR OPERATIONAL AMPLIFIER



E88TSGFSERIES-32

CAD SOFTWARE : FILCAD

In order to take full advantage of its Mask Programmable filter TSGF approach for Semicustom applications, SGS-THOMSON has developed a comprehensive software package called FILCAD® to cover all the development steps, starting from the feasibility evaluation of the customer's specifications, up to the single-metal interconnection routing required for the MPF customization.

More specifically, the FILCAD system gives the de signer strong assistance during the following steps :

- Evaluation of MPF solutions well suited to specific filter circuit requirements,

- Filter synthesis, leading to a switched capacitor electrical schematic,

- MPF filter simulation (performed with MPF capacitor capabilities),

- Schematic capture and routing of the optional connections,

- Layout file generation, and final verification performed by accurate post-routing simulation.

All FILCAD modules run on VAX® under VMS operating System, and are linked toghether as shown in figure 21. All modules are fully described in the TSGF's User's manual (Vol. 5 of SGS-THOMSON ASIC User's Manuals).

The entry to FILCAD is the customer filter specification which can be provided to SGS-THOMSON in different forms :

- amplitude - phase - group delay templates

- poles and zeros

- biquadratic cell coefficients

- polynomial transfer functions

In addition SGS-THOMSON can perform feasibility study of customer specific filter circuits : in order for customers to get fast and accurate answer, SGS-THOMSON generated a feasibility analysis TSGF questionnaire that customers are kindly required to fill. This questionnaire is available on request at SGS-THOMSON Design centers or nearest sales office or representative.

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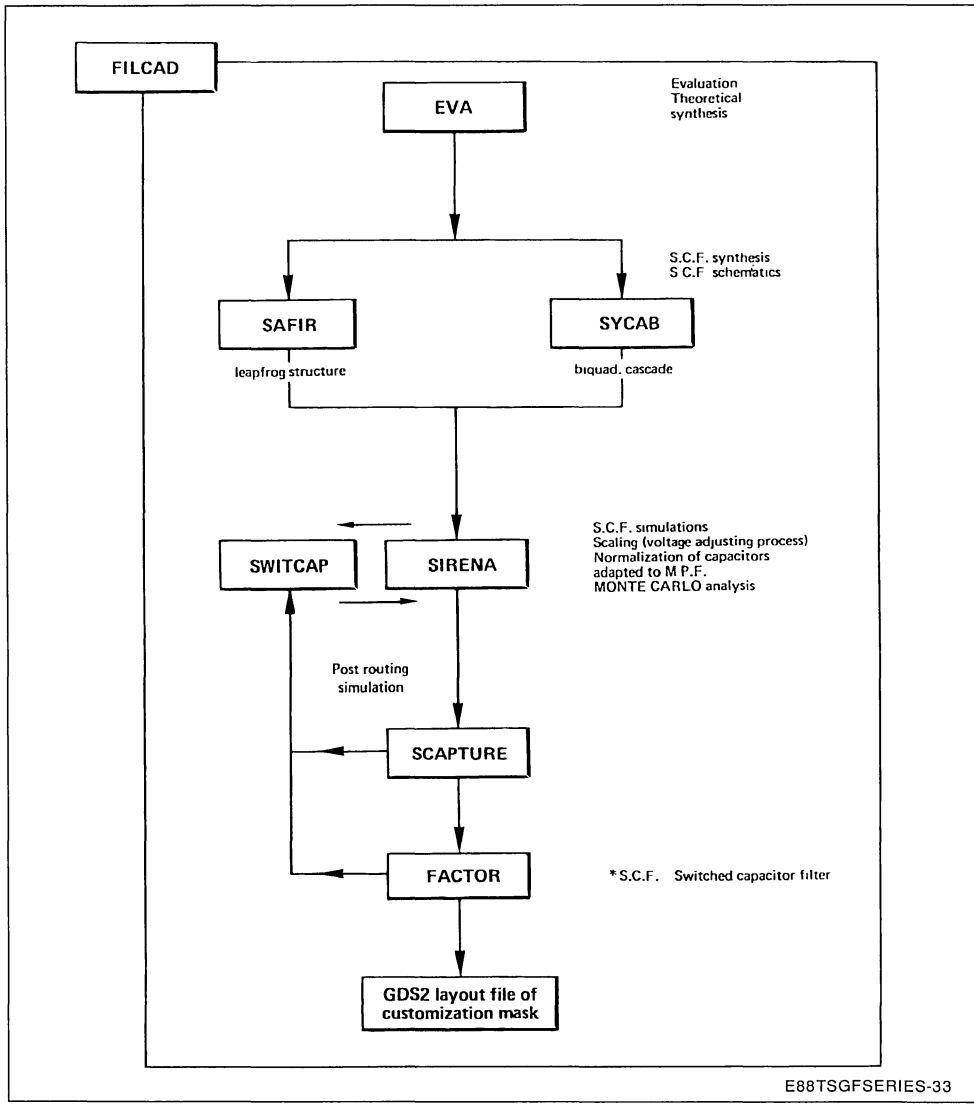
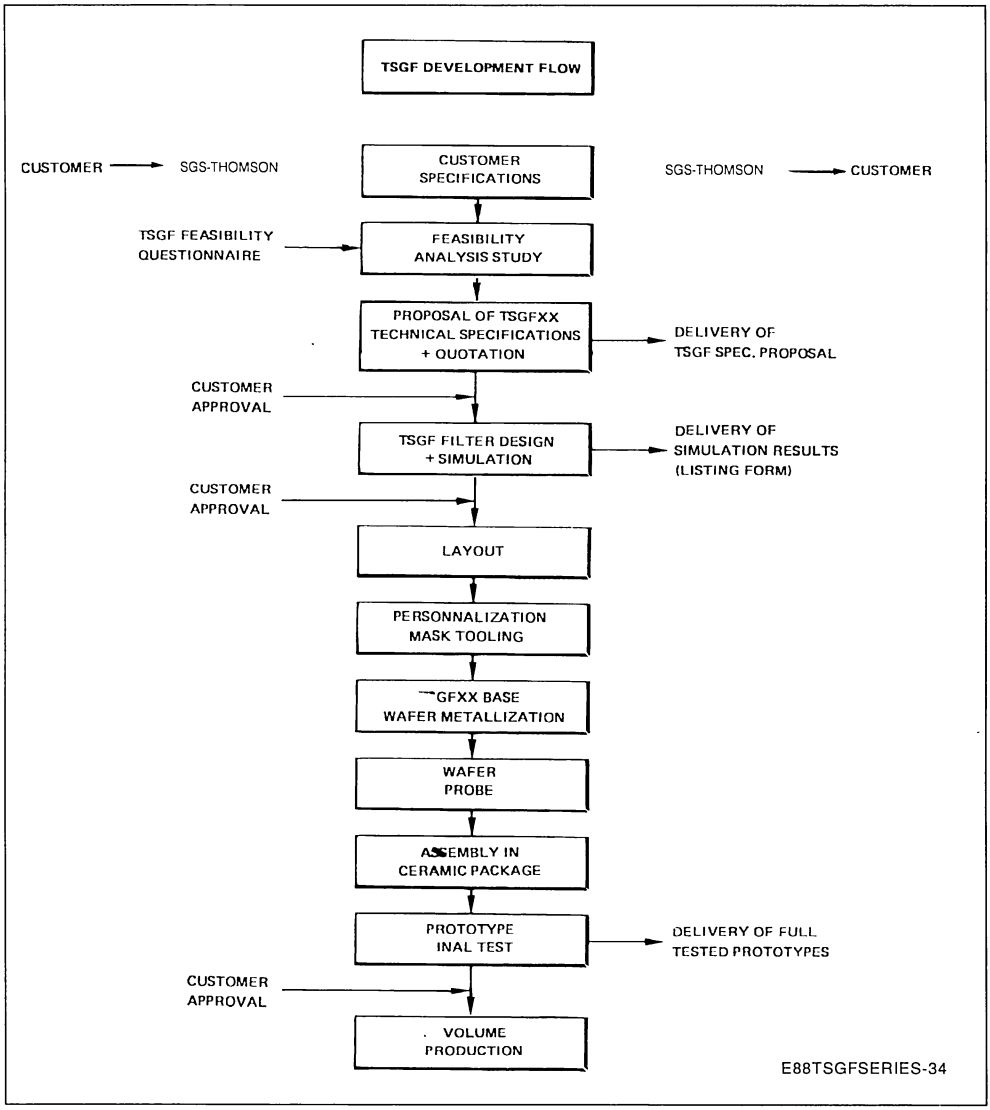
VAX® is a registered trademark of Digital Equipment Corp.

FILCAD, CAD software package developed by SGS-THOMSON for Switched Capacitor Filter designs, TSGF series, is also available for mixed analog-digital TSGSM Standard Cells or Full custom circuits integrating TSGF-like filtering functions.

Figure 21.



FILCAD is a trademark of SGS-Thomson
SWITCAP is a trademark of Columbia University



SGS-THOMSON proposes presently 2 design interfaces to customers for the design of their filter circuits with TSGF series :

- design entirely done by SGS-THOMSON within its Design Centers ;
- design done by customer up to simulation and then completed by SGS-THOMSON.

The table below outlines customer and SGS-THOMSON respective responsibilities for these 2 design interfaces.

DESIGN INTERFACES

Design Step	FILCAD Software	Int 2	Int 3
Theoretical Synthesis	EVA	SGS-THOMSON	Customer
Switched Capacitor Filters Schematics before Scaling	SYCAB or SAFIR	SGS-THOMSON	Customer
Final Schematics	SIRENA (SWITCAP)	SGS-THOMSON	Customer
Additional Simulation	SIRENA (SWITCAP)	SGS-THOMSON	Customer
Approval		Customer	SGS-THOMSON
Schematics Capture	SCAPTURE	SGS-THOMSON	SGS-THOMSON
Layout - Personnalization Mask Generation	FACTOR	SGS-THOMSON	SGS-THOMSON
Post Routing Simulation	SIRENA (SWITCAP)	SGS-THOMSON	SGS-THOMSON

DOCUMENTATION AND SUPPORT

In order to bring users the maximum support on switched capacitor TSGF filter arrays, SGS-THOMSON generated a complete set of documentation and tools which are available on request :

* TSGF User's Manual

* Application Notes
  - AN052 : How to choose a filter in a specific application
  - AN061 : implementation and applications around Standard MPFS
  - AN069 : A supplement to the utilization of switched capacitor filters.
    AN070 : Band Pass and Band Stop Filters.
  - AN075 : Signal detection and sinewave generation.

* MPF's evaluation boards.

* TSGF feasibility/analysis questionnaire.

In addition specialists can be contacted within SGS-THOMSON Microelectronics Filter Design Centers.

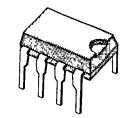
2nd TO 4th ORDER ANALOG FILTER ARRAY

With the TSGF04 array, whose block diagram is given below, user is given 2 different pin-out configurations :

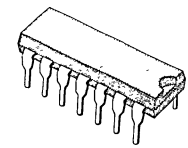
- 8 pin DIL only the filter up to 4th order is accessible.
- 14 pin DIL version where in addition, one uncommitted Op-amp and one internal oscillator capability are offered.

When the external driving of output sample-and-hold is used (CLKSH pin), PWF pin realizes the power adjustement of both uncommited Op-amp and filter unit.

TSGF04 are also available in SO wide package version (0.3 inch) : 16 pin version only.



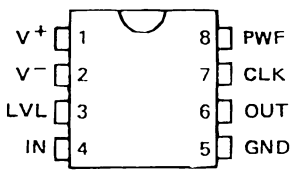
P
DIP-8
(Plastic Package)



P
DIP-14
(Plastic Package)

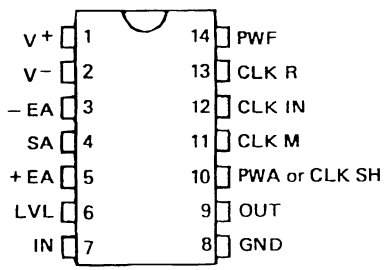
TSGF04
BLOCK DIAGRAM
See figure 4 (E88TSGFSERIES-05)

PIN CONNECTIONS



E88TSGF04-01

8 pins : FILTER ONLY
Compatible with TSGF08



E88TSGF04-02

14 pins : Filter
: + 1 Op - Amp

CLOCK OSCILLATOR

The TSGF04 base accepts external compatible TTL/CMOS clocks on CLKIN pin and provides an internal oscillator performed either by RC or crystal connected between CLKIN and CLKR pins.

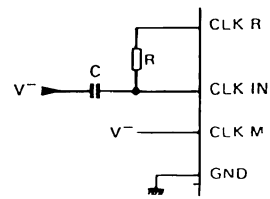
The clock selection mode is provided by CLKM pad which can be connected to V- or GND voltage levels. This connection is realized by two means, depending on the package type chosen :

- with 14-pin package, via CLKM pin.
- with 8-pin package, by internal connection readily performed, only on custom filters.

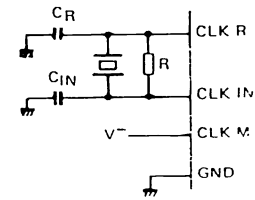
(Note that CLKM pin connected to V+, allows the selection of the internal crystal-controlled oscillator, but the selection by CLKM connected to V- is recommended).

The different possibilities are :

- two internal oscillator modes :
  - RC
  - Crystal

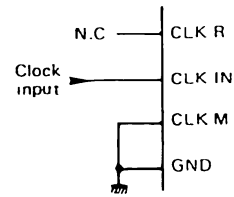


E88TSGF04-03



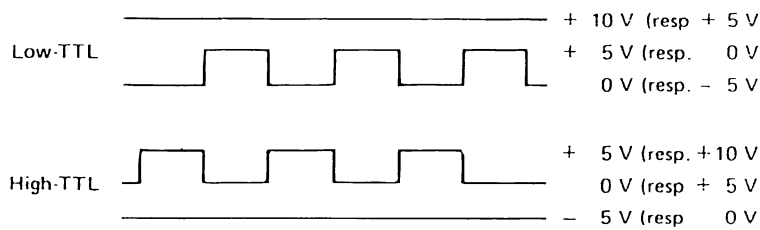
E88TSGF04-04

- three external clocks :
  - low-TTL
  - high-TTL
  - CMOS



E88TSGF04-05

The "low-TTL" and "high-TTL" clock levels are :



E88TSGF04-06

For each package version, the following tables resume, the availability of the different clocks, in terms of the power supply.

Note that in 8-pin version, the clock mode (CLKM) is internally set to GND voltage, except in the case of CMOS clock and 0-5V power supply, where CLKM is internally connected to V- voltage.

8-pin Package			
	0/5V	0/10V	– 5/+ 5V
Low-TTL	NO	C	C
High-TTL	NO	YES	YES
CMOS	C	YES	YES
RC Mode	NO	NO	NO
Crystal Mode	NO	NO	NO

C = Customization option.

14-pin Package			
	0/5V	0/10V	– 5/+ 5V
Low-TTL	NO	C	C
High-TTL	NO	CLKM=GND	CLKM=GND
CMOS	CLKM=V–	CLKM=GND	CLKM=GND
RC Mode	CLKM=V–	CLKM=V–	CLKM=V–
Crystal Mode	CLKM=V–	CLKM=V–	CLKM=V–

ELECTRICAL OPERATING CHARACTERISTICS :

WITH SINGLE SUPPLY VOLTAGE :
T_{amb} = 25°C, V + = 10V, V – = 0V, GND = 5V (unless otherwise specified)

CLKM	Parameter	Min.	Typ.	Max.	Unit
GND	Threshold Voltage		1.5		V
	External Clock Frequency			5	MHz
V –	RC MODE :				
	High Threshold Voltage on CLKIN	1	1.25	1.5	V
	Corresponding Voltage on CLKR		– 5		V
	Low Threshold Voltage on CLKIN	1.5	– 1.25	– 1	V
	Corresponding Voltage on CLKR		+ 5		V
	Oscillator Frequency			5	MHz
	Resistor	2		10 000	kΩ
	Capacitor	0		47	nF
V –	CRYSTAL MODE :				
	Oscillator Frequency			5	MHz
	Resistor		1		MΩ
	Capacitor C_R	10		100	pF
	Capacitor C_{IN}	10		30	pF

ELECTRICAL OPERATING CHARACTERISTICS (continued)

WITH DUAL SUPPLY VOLTAGE :
T_{amb} = 25°C, V + = 5V, V – = – 5V, GND = 0V (unless otherwise specified)

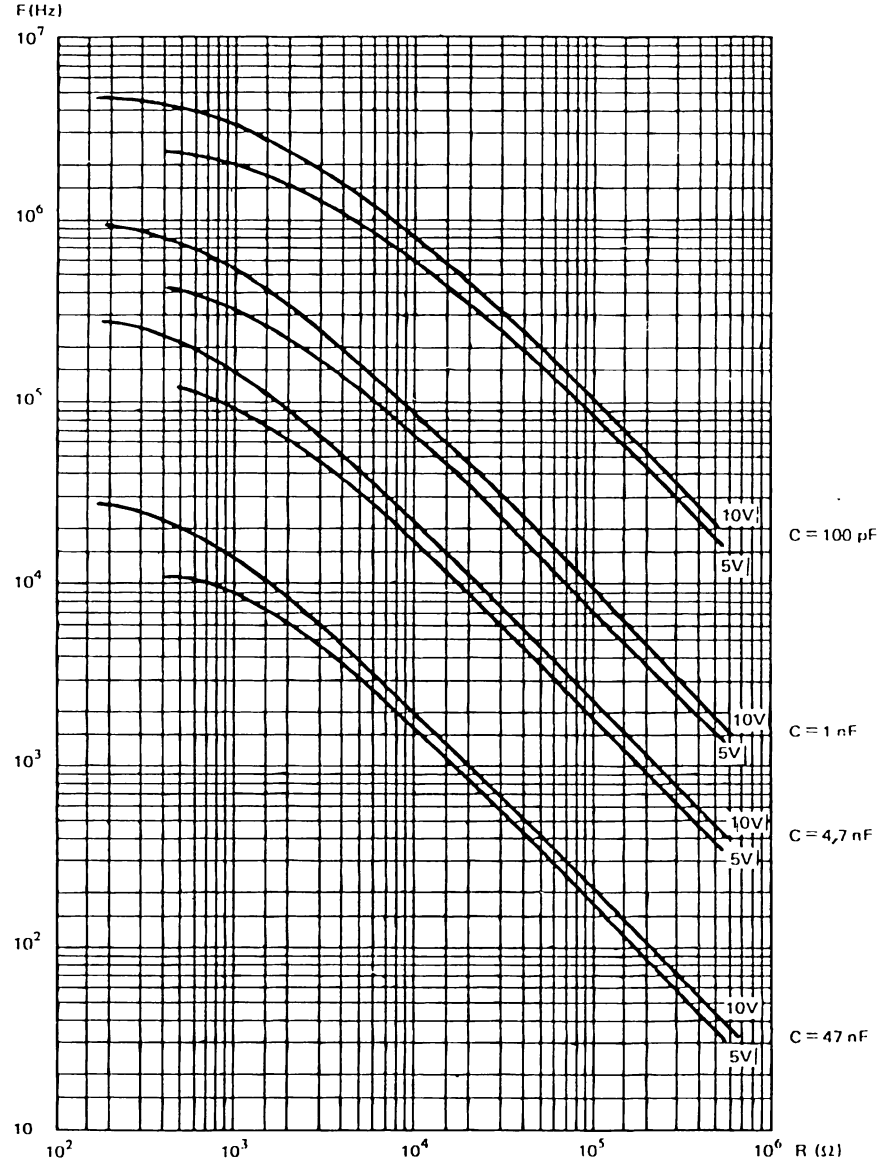
CLKM	Parameter	Min.	Typ.	Max.	Unit
GND	Threshold Voltage		6.5		V
	External Clock Frequency			5	MHz
V –	RC MODE :				
	High Threshold Voltage on CLKIN	6	6.25	6.5	V
	Corresponding Voltage on CLKR		0		V
	Low Threshold Voltage on CLKIN	3.5	3.75	4	V
	Corresponding Voltage on CLKR		+ 10		V
	Oscillator Frequency			5	MHz
	Resistor	2		10 000	kΩ
	Capacitor	0		47	nF
V –	CRYSTAL MODE :				
	Oscillator Frequency			5	MHz
	Resistor		1		MΩ
	Capacitor C_R	10		100	pF
	Capacitor C_{IN}	10		30	pF

WITH SINGLE SUPPLY VOLTAGE :
T_{amb} = 25°C, V + = 5V, V – = 0V, GND = 2.5V (unless otherwise specified)

CLKM	Parameter	Min.	Typ.	Max.	Unit
GND	Threshold Voltage		3.8		V
	External Clock Frequency			5	MHz
V –	RC MODE :				
	High Threshold Voltage on CLKIN	3	3.2	3.4	V
	Corresponding Voltage on CLKR		0		V
	Low Threshold Voltage on CLKIN	1.5	1.8	2	V
	Corresponding Voltage on CLKR		+ 5		V
	Oscillator Frequency			5	MHz
	Resistor	2		10 000	kΩ
	Capacitor	0		47	nF
V –	CRYSTAL MODE :				
	Oscillator Frequency			5	MHz
	Resistor		1		MΩ
	Capacitor C_R	10		100	pF
	Capacitor C_{IN}	10		30	pF

INVERTING TRIGGER FUNCTIONING FREQUENCY VARIATION AS FUNCTION OF R

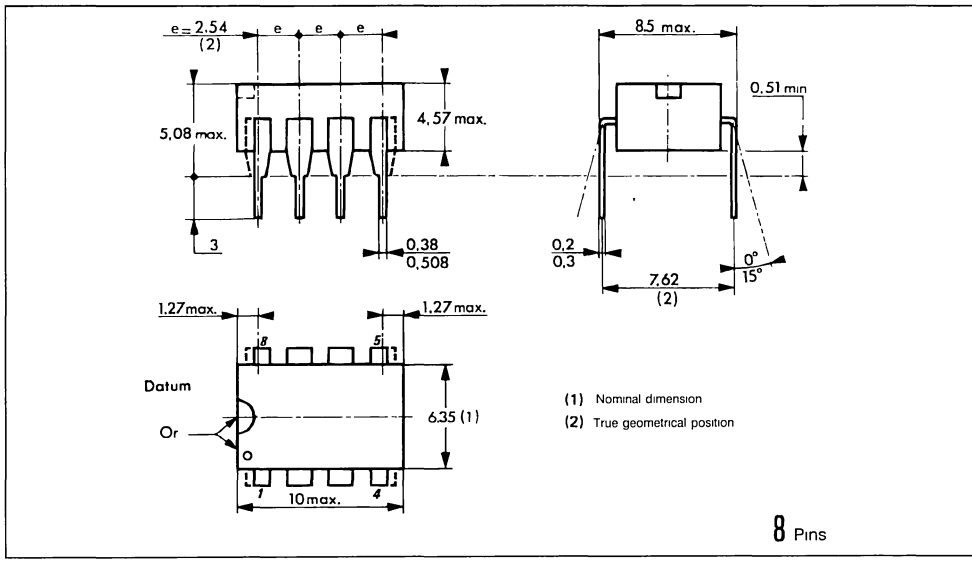
With internal RC oscillator mode, the user's guide for R and C choice is given by following curves and for both supply voltages : 0.5V, 0.10V.



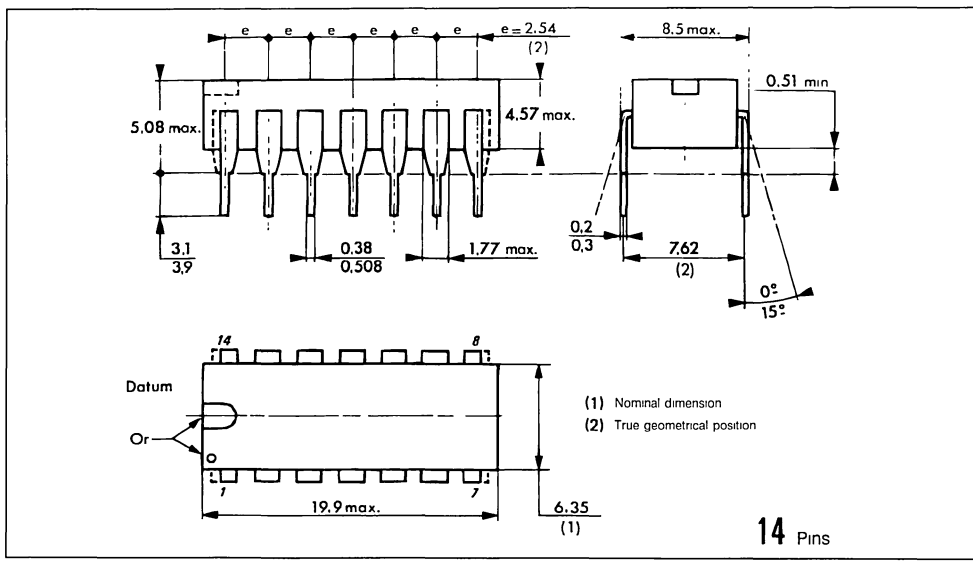
E88TSGF04-07

PACKAGE MECHANICAL DATA

8 PINS - PLASTIC DIP



14 PINS - PLASTIC DIP

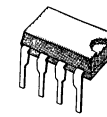


TSGF08 - 4th TO 8th ORDER ANALOG FILTER

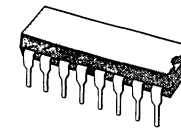
The TSGF08 array provides users with filter integration from 4th to 8th order. 2 package versions are offered to users :

- 8 pin DIL, where only the filter unit is accessible,
- 16 pin DIL, where 2 uncommitted Op-amps are added to previous version.

TSGF08 are also available in SO wide package version (0.3 inch) : 16 pin version only.



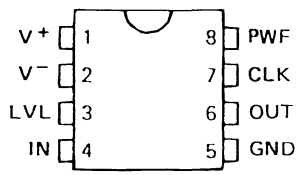
P
DIP-8
(Plastic Package)



P
DIP-16
(Plastic Package)

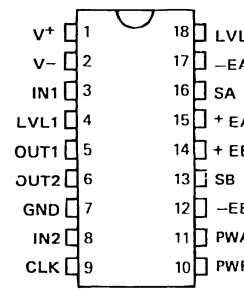
TSGF08
BLOCK DIAGRAM
See figure 4 (E88TSGFSERIES-05)

PIN CONNECTIONS



E88TSGF08-01

8 pins : FILTER ONLY
Compatible with TSGF04

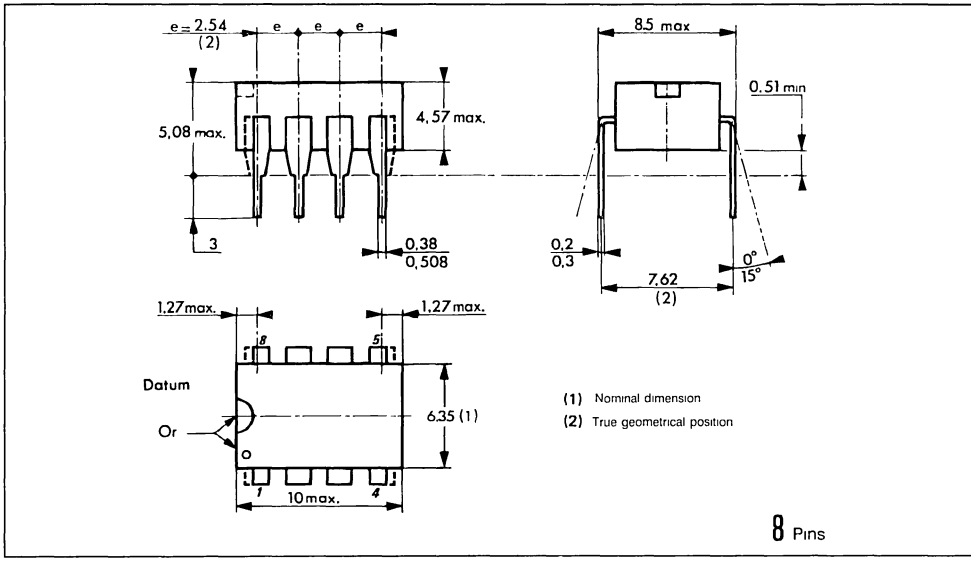


E88TSGF08-02

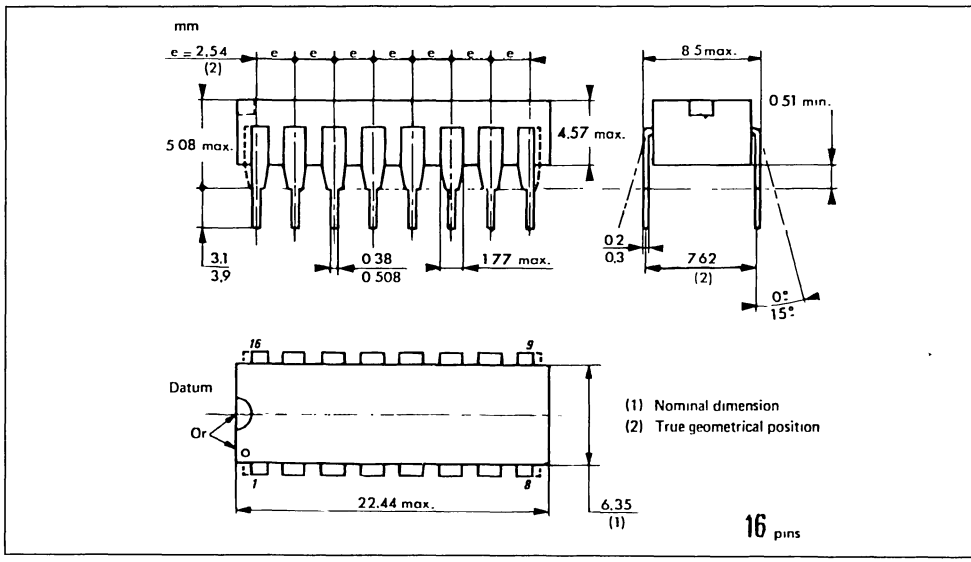
16 pins : Filter
: + 2 Op - Amp
Compatible with TSGF12 (with a single filter)

PACKAGE MECHANICAL DATA

8 PINS - PLASTIC DIP



16 PINS - PLASTIC DIP



TSGF12 - 8th TO 12th ORDER ANALOG FILTER

TSGF12 array offers the capability to integrate either one single from 8th to 12th order or 2 different filters whose sum of orders cannot exceed 12.

These 2 different filters can have either same clock or 2 different clock inputs.

The TSGF12 package versions are :

- 16 pin DIL : 1 filter + 2 Op-amps
- 16 pin DIL : 1 filter + 2 Op-amps + driving of output S/H
- 16 pin DIL : 2 filters + 1 Op-amp + 2 clock inputs.
- 18 pin DIL : 2 filters + 2 Op-amps + 1 clock input.
- 20 pin DIL : 2 filters + 2 Op-amps + 2 clock inputs.
- 20 pin DIL : 2 filters + 2 Op-amps + 2 clock inputs + driving of output S/H.

TSGF12 array are also avaialble in SO wide package version (0.3 inch) : 18 and 24 pin versions.

In case of dual filter integration, the CLKSH pin operates only on the output of filter n° 1 (OUTPUT 1). In the same case, for the 16 pin version, only LVL2 pin is available : therefore user can only adjust the Output DC level of filter 2.

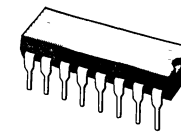
Clock divider :

The number of dividers by 2 available on TSGF12 array is 8.

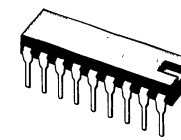
Therefore in case of dual filter on chip integration, there are 2 possibilities to use the clock divider :

- if one filter does not require internal dividers, the 8 dividers by 2 are available for the second filter ;
- if the first filter requires n internal dividers, it remains only 7-n ones available for the second filter.

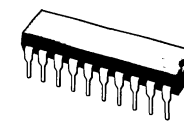
TSGF12
BLOCK DIAGRAM
See figure 4 (E88TSGFSERIES-05)



P
DIP-16
(Plastic Package)

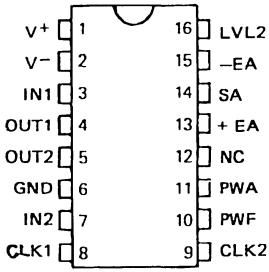


P SUFFIX
DIP-18
(Plastic Package)



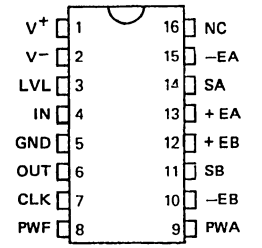
P
DIP-20
(Plastic Package)

PIN CONNECTIONS



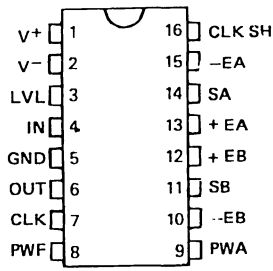
E88TSGF12-01

16 PINS : 2 filters
+ 1 OP - Amp
+ 2 Clock inputs.



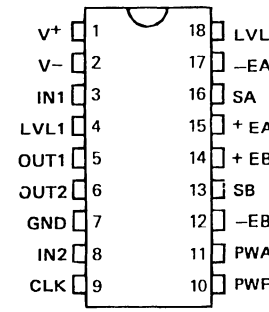
E88TSGF12-02

16 PINS : 1 filter
+ 2 OP - Amp
Compatible with TSGF08



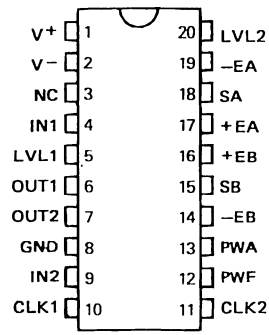
E88TSGF12-03

16 PINS : 1 filters
+ 2 OP - Amps
+ Driving of output S/H.



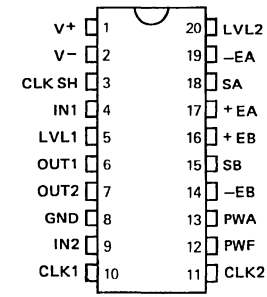
E88TSGF12-04

18 PINS : 2 filters
+ 1 OP - Amp
+ 1 Clock input.



E88TSGF12-05

20 PINS : 2 filters
+ 2 OP - Amps
+ 2 Clock inputs.

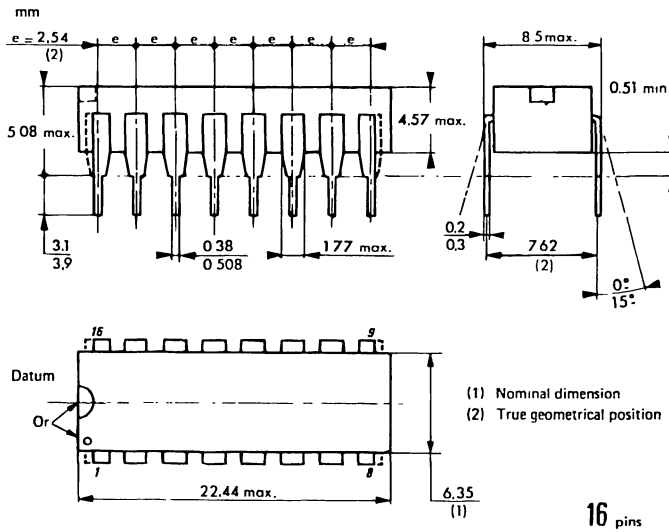


E88TSGF12-06

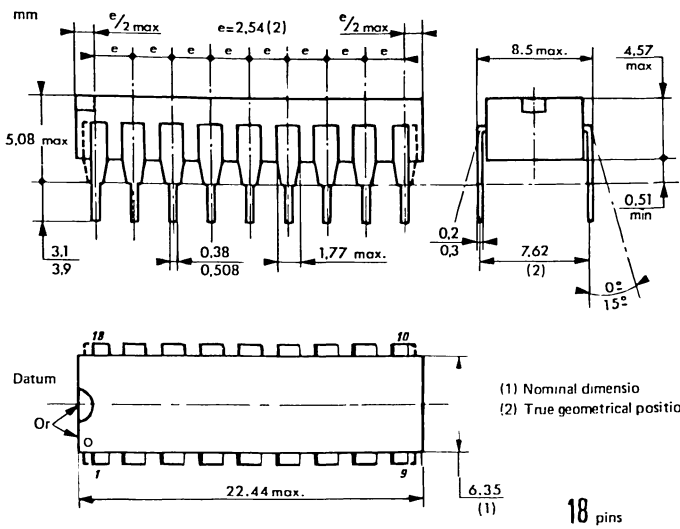
20 PINS : 2 filters
+ 2 OP - Amps
+ 2 Clock inputs
+ Driving of output S/H.

PACKAGE MECHANICAL DATA

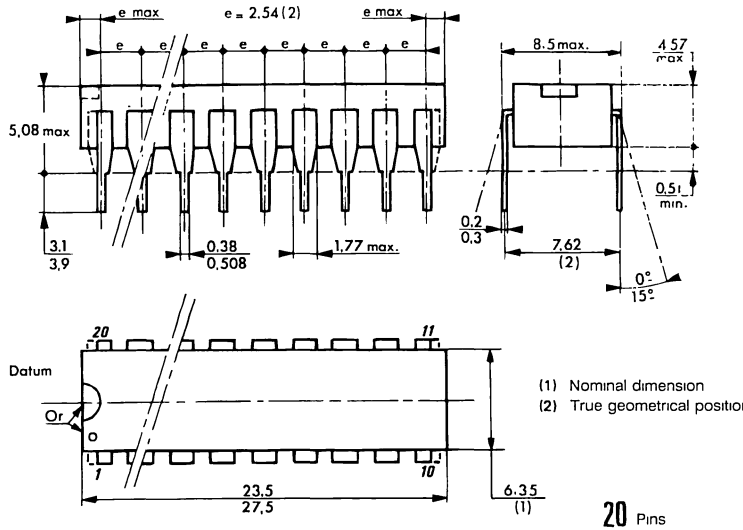
16 PINS - PLASTIC DIP



18 PINS - PLASTIC DIP

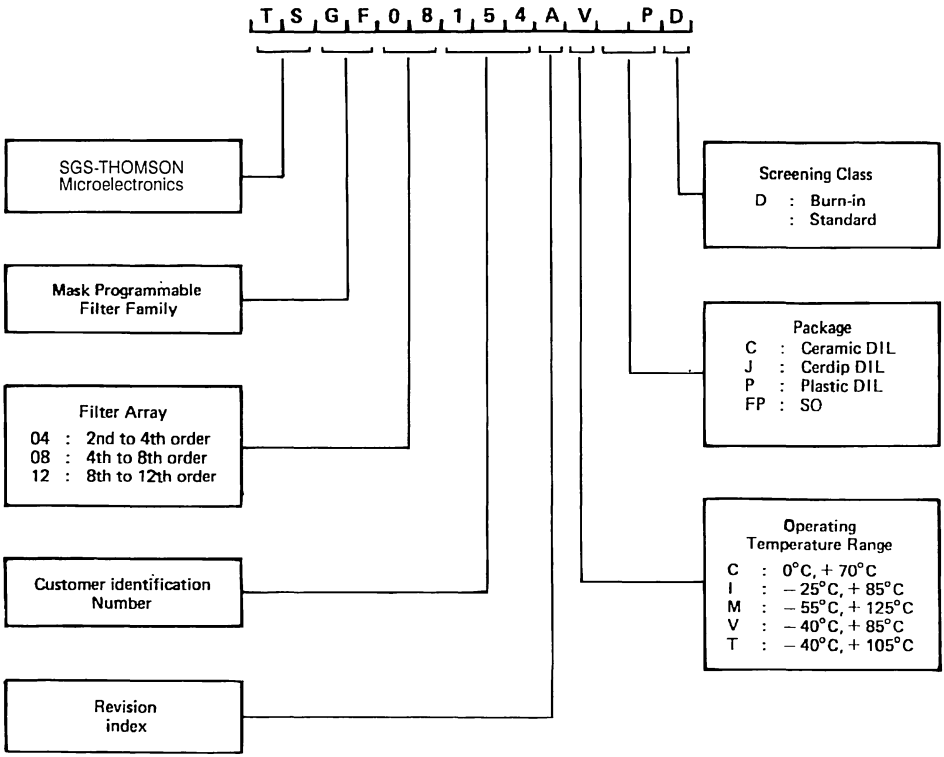


20 PINS - PLASTIC DIP



(1) Nominal dimension
(2) True geometrical position

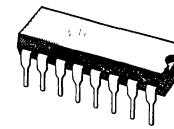
ORDER CODES


T S G F 0 8 1 5 4 A V P D
SGS-THOMSON Microelectronics
Mask Programmable Filter Family
Filter Array
04 : 2nd to 4th order
08 : 4th to 8th order
12 : 8th to 12th order
Customer identification Number
Revision index
Screening Class
D : Burn-in
: Standard
Package
C : Ceramic DIL
J : Cerdip DIL
P : Plastic DIL
FP : SO
Operating Temperature Range
C : 0°C, + 70°C
I : − 25°C, + 85°C
M : − 55°C, + 125°C
V : − 40°C, + 85°C
T : − 40°C, + 105°C

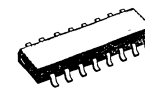
SWITCHED CAPACITOR MASK PROGRAMMABLE FILTER

- CAUER TYPE
- 5TH ORDER
- STOPBAND ATTENUATION : 33dB (typ.)
- PASSBAND RIPPLE : 0.05dB (typ.)
- CLOCK TO CUT-OFF FREQ; RATIO : 75.3
- CLOCK FREQUENCY RANGE : 1 TO 1500kHz
- CUT-OFF FREQUENCY RANGE : 13Hz TO 20kHz

Note : For general characteristics, see TSG85XX specifications. For non standard quality level, consult SGS-THOMSON general ordering information.



P
DIP-16
(Plastic Package)



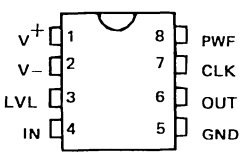
FP
SO-16
(Plastic Micropackage)

P
DIP-8
(Plastic Package)

DESCRIPTION

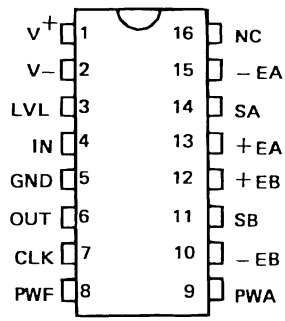
The TSG8510 is a HCMOS lowpass elliptic filter.

PIN CONNECTIONS



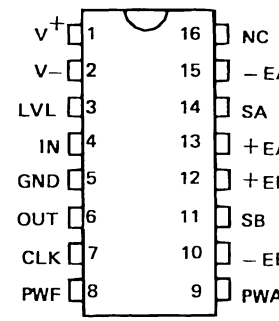
8 pins : FILTER ONLY
DIP-8 Package

E88TSG8510-01



16 pins : FILTER + 2 OP-AMPs
DIP-16 Package

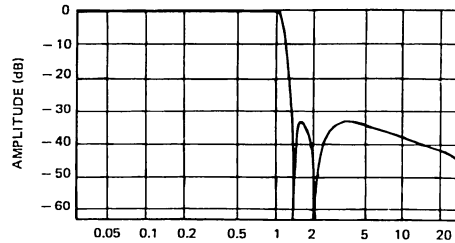
E88TSG8510-02



SO-16 Package

E88TSG8510-03

AMPLITUDE RESPONSE CURVE



E88TSG8510-04

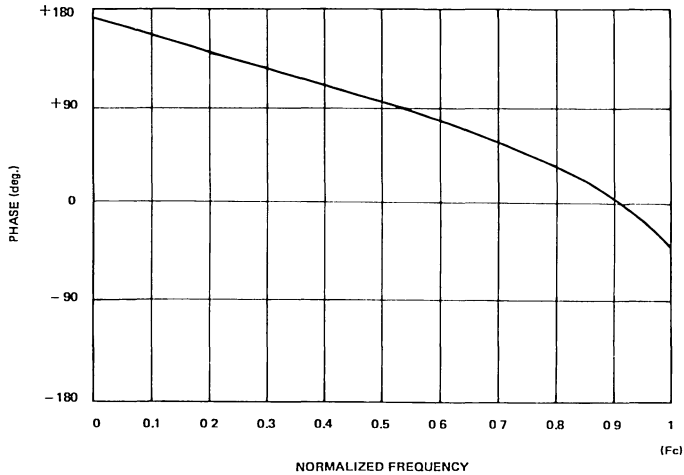
FILTER SPECIFICATIONS

Lowpass Filter : TSG8510 ; Type : Cauer ; Order : 5.
$V^+ = 5V$, $V^- = -5V$, T = 25°C, RL = 5kΩ, CL = 100pF, $I_{PWF} = 100\mu A$

Symbol	Parameter		Typ.	Tested Limits	Unit
F_e	External Clock Frequency		1 1500(*)		kHz (min) kHz (max)
F_i	Internal Sampling Frequency		0.5 750(*)		kHz (min) kHz (max)
F_e/F_c	Clock to Cutoff fr. Ratio		75.3 ± 1%		
F_c	Cutoff Frequency		0.013 20(*)		kHz (min) kHz (max)
G_o	Passband Gain		– 0.3 0		dB (min) dB (max)
Ap	Passband Ripple	Fe = 256kHz	0.05	0.4	dB (max)
As	Stopband Attenuation	Fe = 256kHz F > 1.37 Fc	33	32	dB (min)
Voff	Output DC Offset Voltage	LVL = 0V	± 100	± 200	mV (max)
LVL	DC Level Adjustment		± 60		mV
LG	Level gain		3.3		
R_{PWF}	PWF Resistance		10 72		kΩ (min) kΩ (max)
I_{PWF}	Input Current on PWF		50 250		µA (min) µA (max)
I^+	V^+ Supply Current	Fe = 100kHz $I_{pwa} = 0\mu A$	3	5	mA (max)
I^-	V^- Supply Current		3	5	mA (max)
$PSRR^+$	V^+ Supply Rejection Ratio	Fe = 256kHz Fin = 1kHz	35		dB
$PSRR^-$	V^- Supply Rejection Ratio		55		dB
R_{IN}	Input Resistance		3		MΩ
C_{IN}	Input Capacitance		20		pF
V_o	Output Voltage Swing		+ 3.5 – 4.5		Vp - p (max)
Vn	Output Noise	BW = 3.4kHz Fe = 256kHz Vin = 2Vrms	89		µVrms
SNR	Signal to Noise Ratio		87		dB

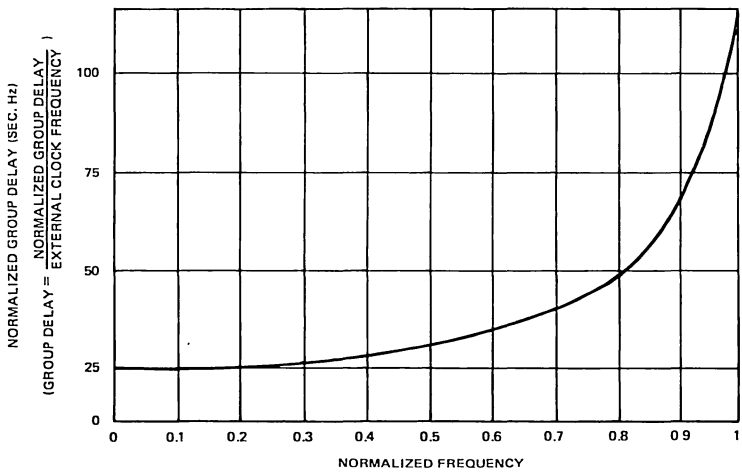
(*) At maximum Fe - stopband attenuation As > 32dB for F > 1 37Fc
(with $I_{pwf} = 250\mu A$) - passband ripple . A_p = 0 8dB
- passband gain : G_0 = – 0 4dB

PHASE RESPONSE CURVE (in passband)



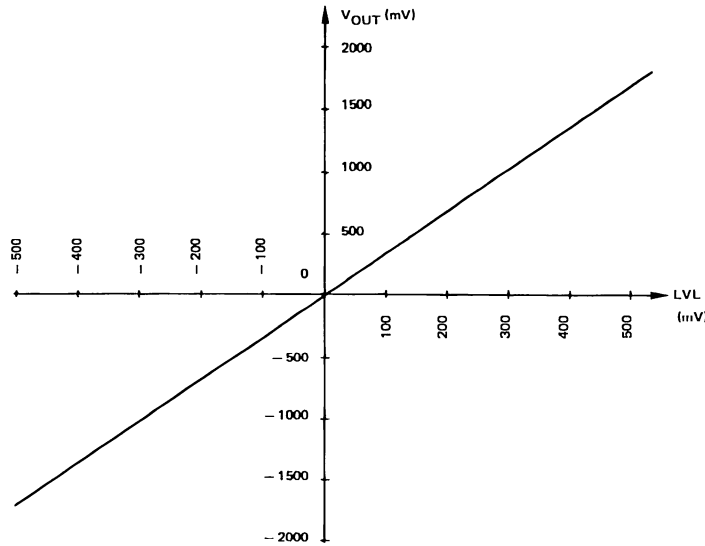
E88TSG8510-05

GROUP DELAY CURVE (in passband)



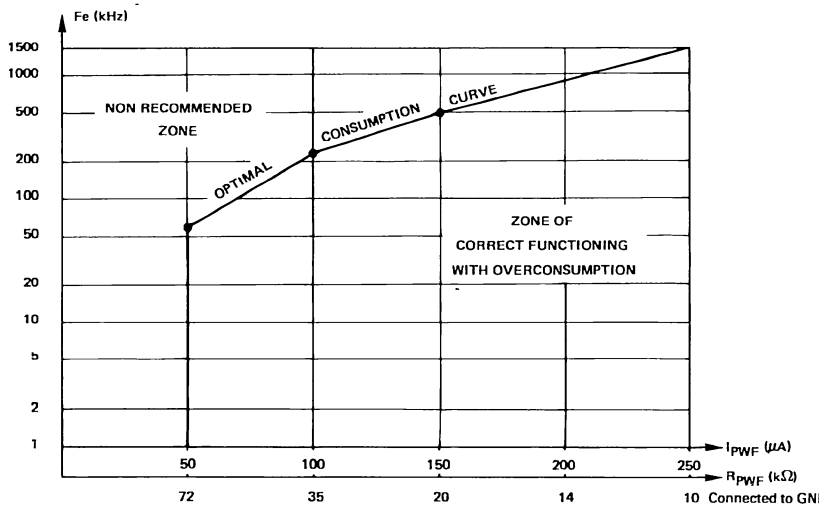
E88TSG8510-06

OUTPUT DC VOLTAGE ADJUSTMENT FROM LVL PIN



E88TSG8510-07

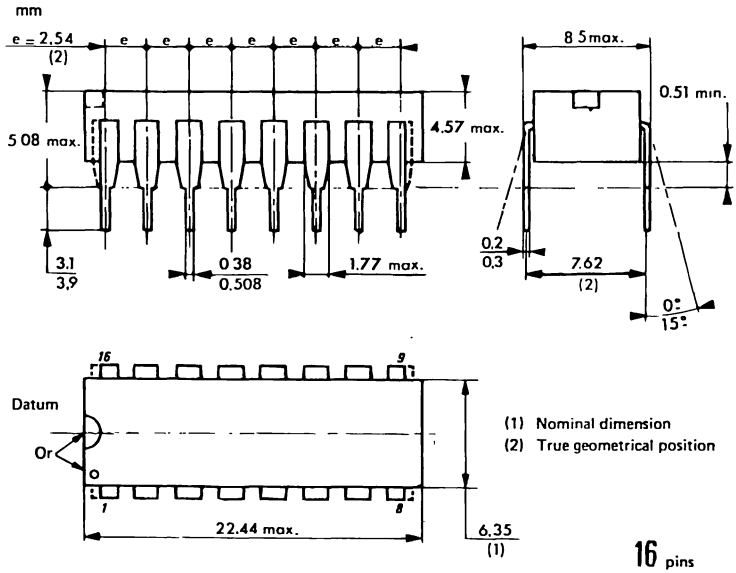
USER'S GUIDE FOR I_{PWF} AND R_{PWF} CHOICE



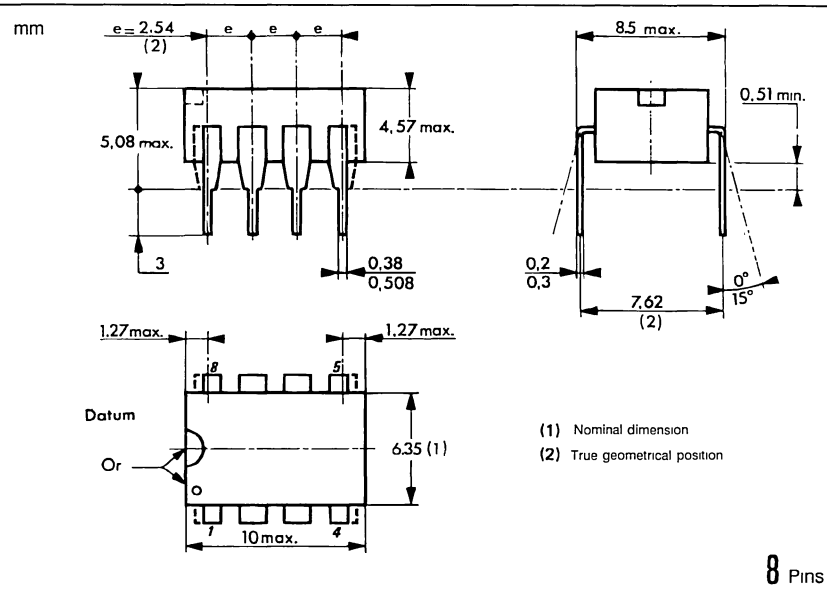
E88TSG8510-08

PACKAGE MECHANICAL DATA

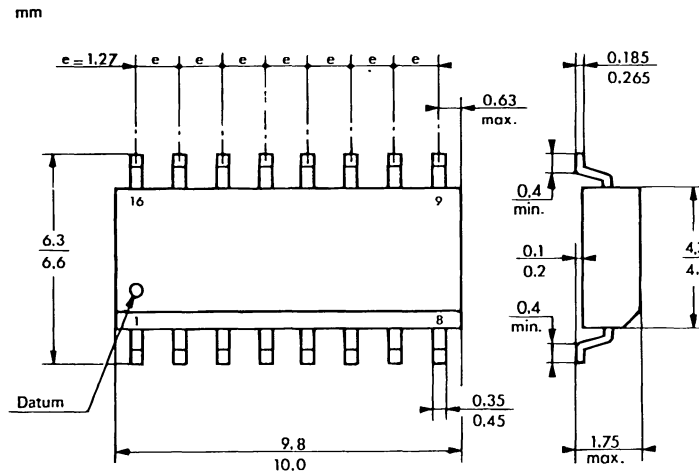
16 PINS - Plastic Dip



8 PINS - Plastic Dip



16 PINS - Plastic Micropackage



16 pins

ORDER CODES

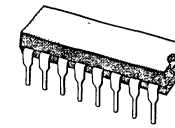
Plastic	16 Pins Package : TSG8510XP
Ceramic	16 Pins Package : TSG8510XC
Cerdip	16 Pins Package : TSG8510XJ
Plastic	8 Pins Package : TSG85101XP

X : Temperature Range = C : 0°C, + 70°C
I : – 25°C, + 85°C
V : – 40°C, + 85°C
M : – 55°C, + 125°C

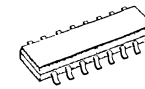
SWITCHED CAPACITOR MASK PROGRAMMABLE FILTER

- CAUER TYPE
- 7TH ORDER
- STOPBAND ATTENUATION : 55dB (typ)
- PASSBAND RIPPLE : 0.1dB (typ)
- CLOCK TO CUT-OFF FREQ. RATIO : 75.3
- CLOCK FREQUENCY RANGE : 1 TO 1300kHz
- CUT-OFF FREQUENCY RANGE : 13Hz TO 17.3kHz

Note : For general characteristics, see TSG85XX specifications. For non standard quality level, consult SGS-THOMSON general ordering information.



P
DIP-16
(Plastic Package)



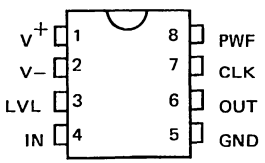
FP
SO-16
(Plastic Micropackage)

P
DIP-8
(Plastic Package)

DESCRIPTION

The TSG8511 is a HCMOS lowpass elliptic filter.

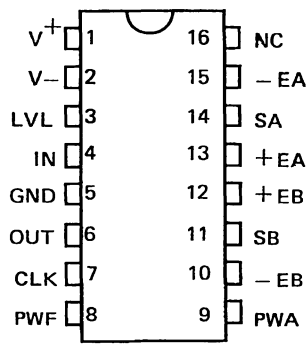
PIN CONNECTIONS



8 pins : FILTER ONLY

E88TSG8511-01

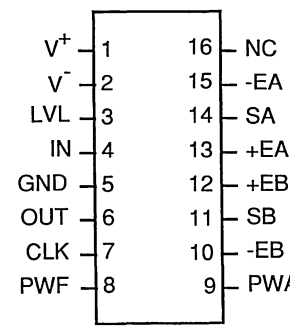
DIP Package



16 pins : FILTER + 2 OP-AMPs

DIP Package

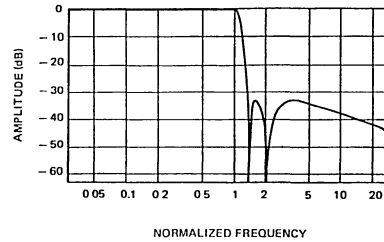
E88TSG8511-02



SO-16 Package

E88TSG8511-03

AMPLITUDE RESPONSE CURVE



E88TSG8511-04

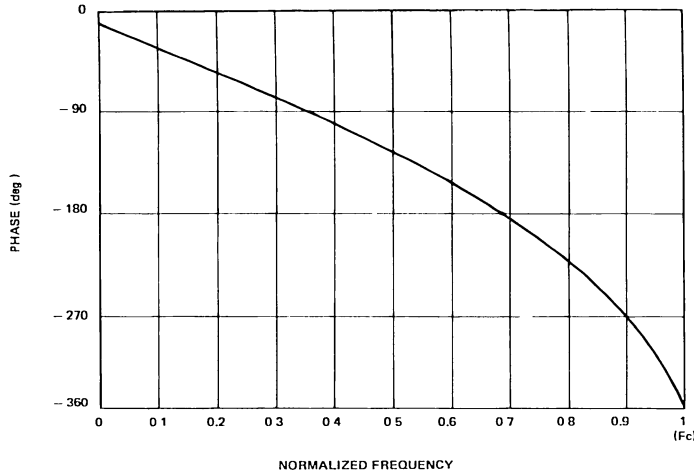
FILTER SPECIFICATIONS

Lowpass Filter : TSG8511 ; Type : Cauer ; Order : 7.
$V^+ = 5V$, $V^- = -5V$, T = 25°C, RL = 5kΩ, CL = 100pF, $I_{PWF} = 100\mu A$

Symbol	Parameter		Typ.	Tested Limits	Unit
Fe	External Clock Freq.		1 1300(*)		kHz (min) kHz (max)
Fi	Internal Sampling Freq.		0.5 650(*)		kHz (min) kHz (max)
Fe/Fc	Clock to Cutoff fr. Ratio		75.3 ± 1%		
Fc	Cutoff Frequency		0.013 17.3(*)		kHz (min) kHz (max)
G_o	Passband Gain		– 0.3 0		dB (min) dB (max)
Ap	Passband Ripple	Fe = 256kHz	0.1	0.5	dB (max)
As	Stopband Attenuation	Fe = 256kHz F > 1.3Fc;	55	50	dB (min)
Voff	Output DC Offset Voltage	LVL = 0V	± 150	± 300	mV (max)
LVL	DC Level Adjustment		± 64		mV
LG	Level gain		– 4.7		
R_{PWF}	PWF Resistance		10 72		kΩ (min) kΩ (max)
I_{PWF}	Input Current on PWF		50 250		µA (min) µA (max)
I^+	V^+ Supply Current	Fe = 100kHz Ipwa = 0µA	3.5	5	mA (max)
I^-	V^- Supply Current		3.5	5	mA (max)
$PSRR^+$	V^+ Supply Rejection Ratio	Fe = 256kHz Fin = 1kHz	32		dB
$PSRR^-$	V^- Supply Rejection Ratio		47		dB
R_{IN}	Input Resistance		3		MΩ
C_{IN}	Input Capacitance		20		pF
Vo	Output Voltage Swing		+ 3.5 – 4.5		Vp-p (max)
Vn	Output Noise	BW = 3.4kHz Fe = 256kHz Vin = 2Vrms	158		µVrms
SNR	Signal to Noise Ratio		82		dB

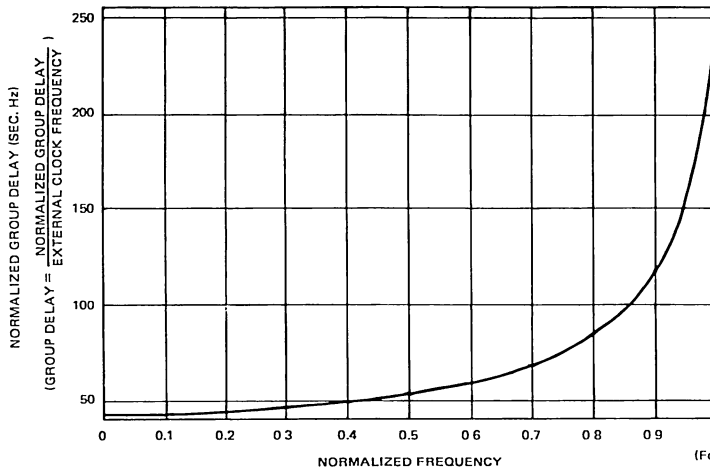
(*) At maximum Fe : - stopband attenuation As > 50dB for F > 1.3Fc
(with $I_{pwf} = 250\mu A$) - passband ripple $A_p = 0.5dB$
- passband gain . $G_0 = -0.7dB$

PHASE RESPONSE CURVE (in passband)



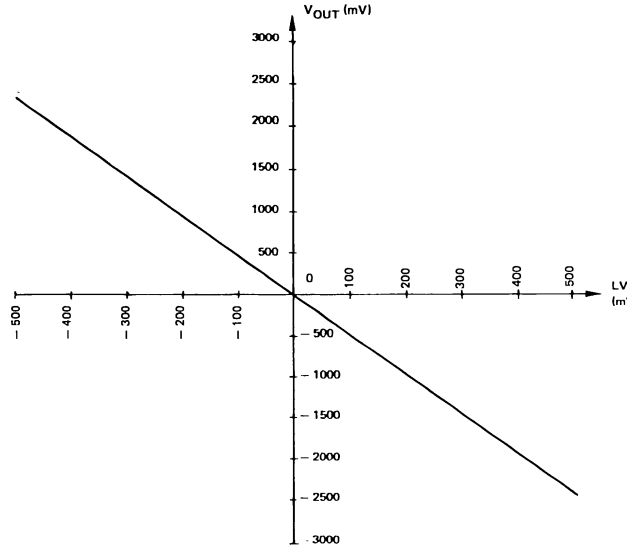
E88TSG8511-05

GROUP DELAY CURVE (in passband)



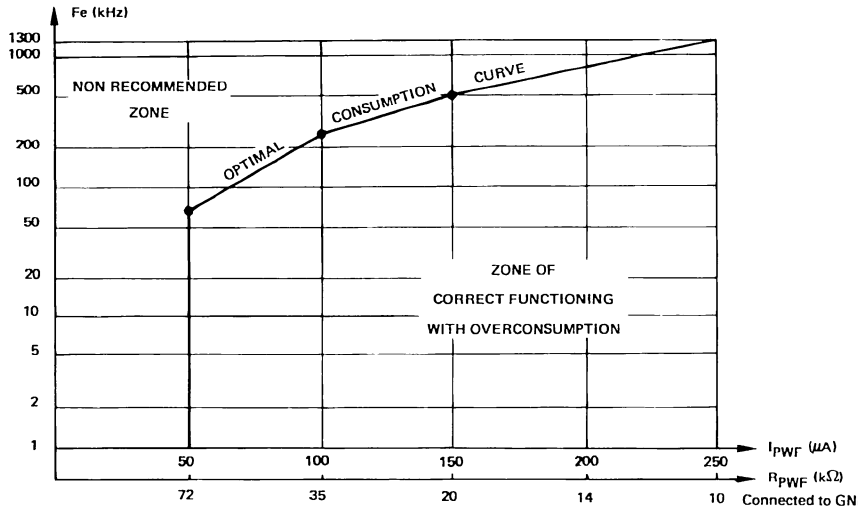
E88TSG8511-06

OUTPUT DC VOLTAGE ADJUSTMENT FROM LVL PIN



E88TSG8511-07

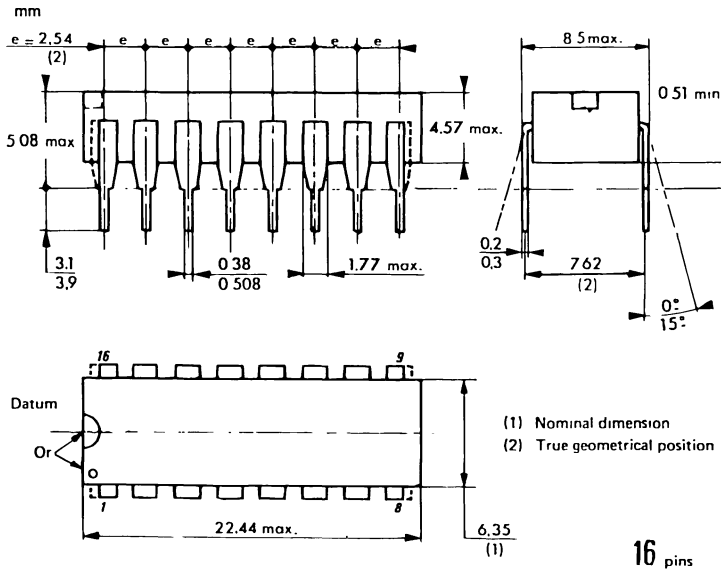
USER'S GUIDE FOR I_{PWF} AND R_{PWF} CHOICE



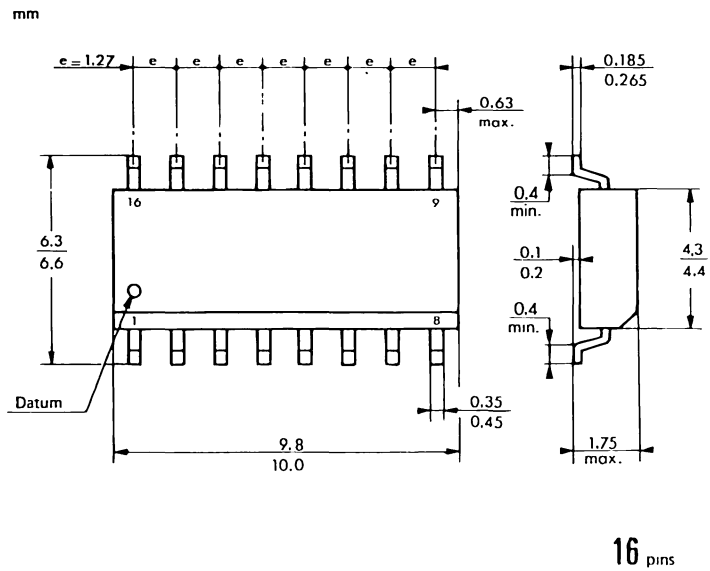
E88TSG8511-08

PACKAGE MECHANICAL DATA

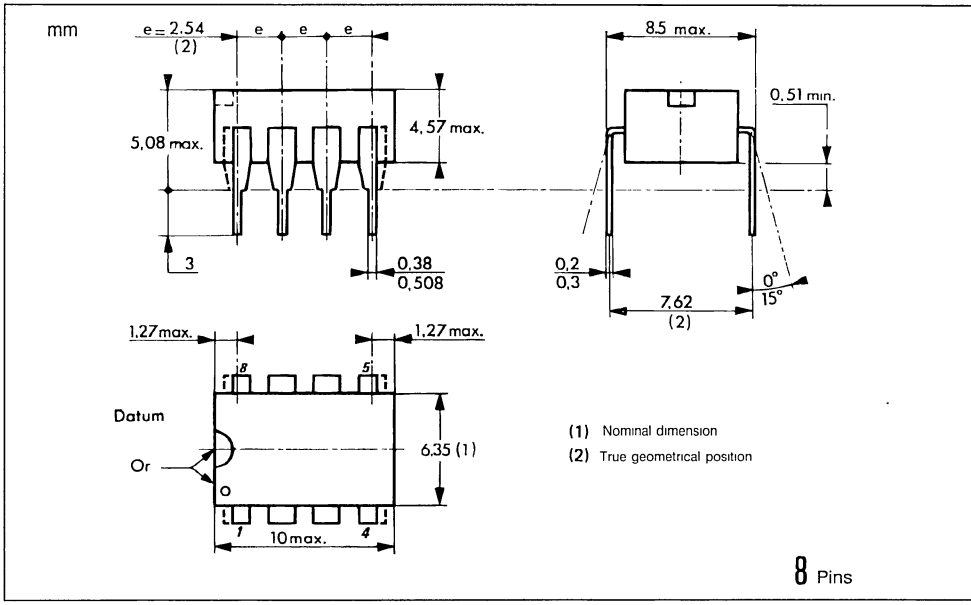
16 PINS - Plastic Dip



16 PINS - Plastic Micropackage



8 PINS - Plastic Dip



ORDER CODES

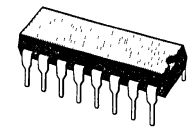
Plastic	16 Pins Package : TSG8511XP
Ceramic	16 Pins Package : TSG8511XC
Cerdip	16 Pins Package : TSG8511XJ
Plastic	8 Pins Package : TSG85111XP

X : Temperature Range = C : 0°C + 70°C
I : – 25°C + 85°C
V : – 40°C + 85°C
M : – 55°C + 125°C

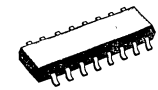
SWITCHED CAPACITOR MASK PROGRAMMABLE FILTER

- CAUER TYPE
- 7TH ORDER
- STOPBAND ATTENUATION : 85dB (typ)
- PASSBAND RIPPLE : 0.15dB (typ)
- CLOCK TO CUT-OFF FREQ. RATIO : 100
- CLOCK FREQUENCY RANGE : 1 TO 2000kHz
- CUT-OFF FREQUENCY RANGE : 10Hz TO 20kHz

Note : For general characteristics, see TSG85XX specifications. For non standard quality level, consult SGS-THOMSON general ordering information.



P
DIP-16
(Plastic Package)



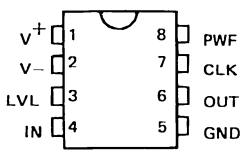
FP
SO-16
(Plastic Micropackage)

P
DIP-8
(Plastic Package)

DESCRIPTION

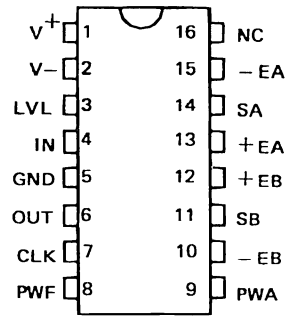
The TSG8512 is a HCMOS lowpass elliptic filter.

PIN CONNECTIONS



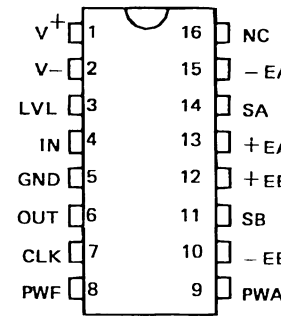
8 pins : FILTER ONLY
DIP-8 Package

E88TSG8512-01



16 pins : FILTER + 2 OP-AMPs
DIP-16 Package

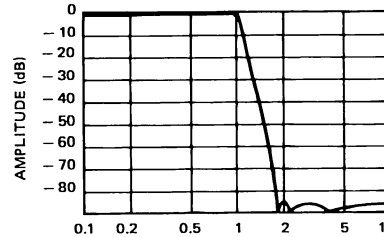
E88TSG8512-02



SO-16 Package

E88TSG8512-03

AMPLITUDE RESPONSE CURVE



E88TSG8512-04

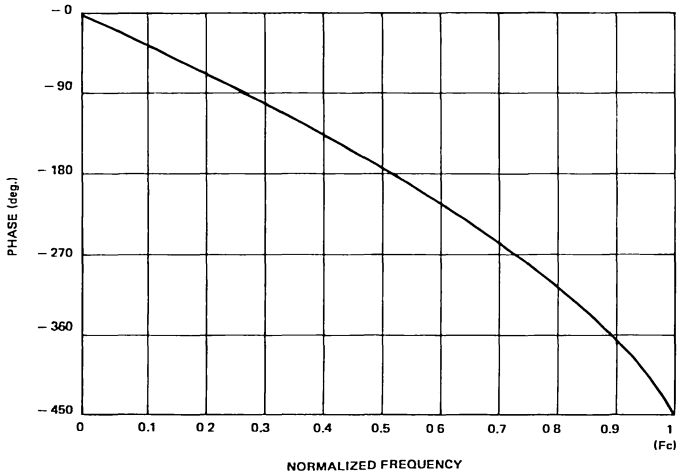
FILTER SPECIFICATIONS

Lowpass Filter : TSG8512 ; Type : Cauer ; Order : 7.
$V^+ = 5V$, $V^- = -5V$, T = 25°C, RL = 5kΩ, CL = 100pF, $I_{PWF} = 100\mu A$

Symbol	Parameter		Typ.	Tested Limits	Unit
Fe	External Clock Freq.		1 2000(*)		kHz (min) kHz (max)
Fi	Internal Sampling Freq.		0.5 1000(*)		kHz (min) kHz (max)
Fe/Fc	Clock to Cutoff fr. Ratio		100 ± 1%		
Fc	Cutoff Frequency		0.010 20(*)		kHz (min) kHz (max)
G_o	Passband Gain		– 0.3 0		dB (min) dB (max)
Ap	Passband Ripple	Fe = 100kHz	0.15	0.5	dB (max)
As	Stopband Attenuation	Fe = 100kHz F > 1.8Fc	85	75	dB (min)
Voff	Output DC Offset Voltage	LVL = 0V	± 150	± 250	mV (max)
LVL	DC Level Adjustment		± 22.5		mV
LG	Level gain		– 11.1		
R_{PWF}	PWF Resistance		10 72		kΩ (min) kΩ (max)
I_{PWF}	Input Current on PWF		50 250		µA (min) µA (max)
I^+	V^+ Supply Current	Fe = 100kHz Ipwa = 0µA	3.5	5	mA (max)
I^-	V^- Supply Current		3.5	5	mA (max)
$PSRR^+$	V^+ Supply Rejection Ratio	Fe = 200kHz Fin = 1kHz	20		dB
$PSRR^-$	V^- Supply Rejection Ratio		35		dB
R_{IN}	Input Resistance		3		MΩ
C_{IN}	Input Capacitance		20		pF
Vo	Output Voltage Swing		+ 3.5 – 4.5		Vp-p (max)
Vn	Output Noise	BW = 1kHz Fe = 100kHz Vin = 2Vrms	112		µVrms
SNR	Signal to Noise Ratio		85		dB

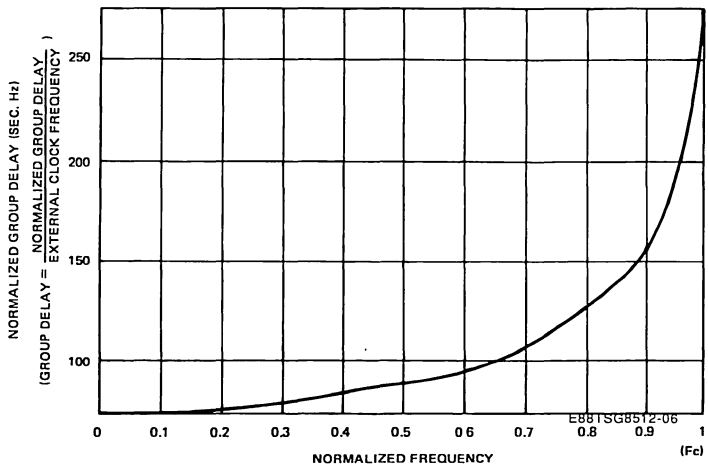
(*) At maximum Fe : - stopband attenuation As > 62dB for F > 1 8Fc
(with $I_{pwf} = 250\mu A$) - passband ripple : A_p = 0 6dB
- passband gain : $G_0 = -0.4dB$

PHASE RESPONSE CURVE (in passband)



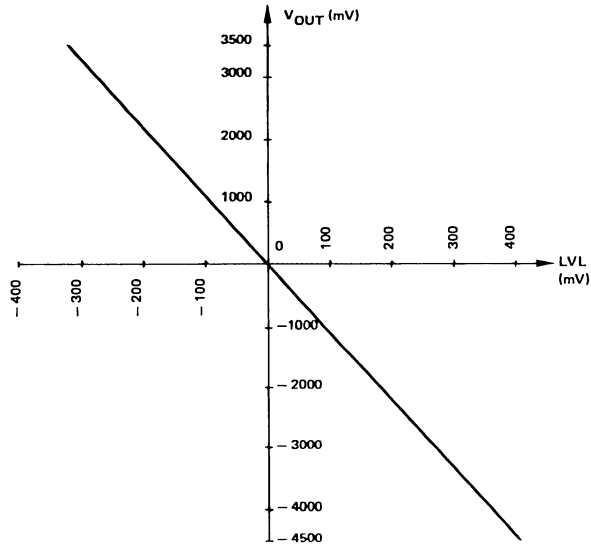
E88TSG8512-05

GROUP DELAY CURVE (in passband)



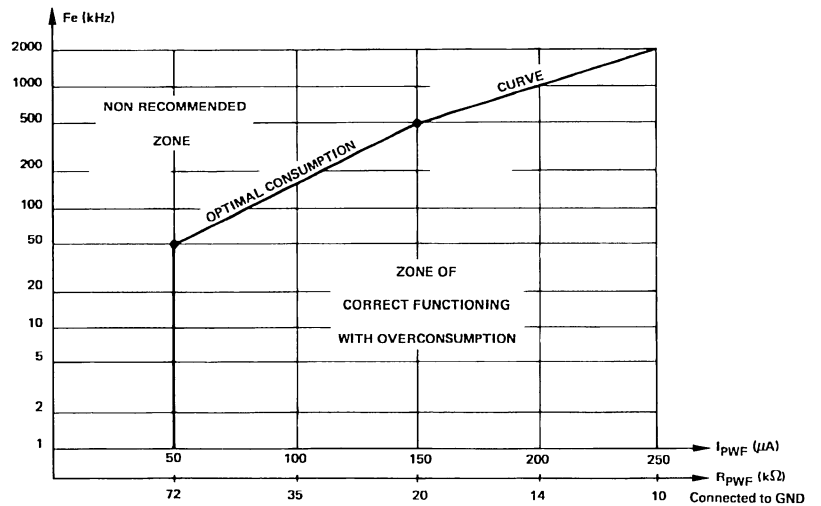
E88TSG8512-06

OUTPUT DC VOLTAGE ADJUSTMENT FROM LVL PIN



E88TSG8512-07

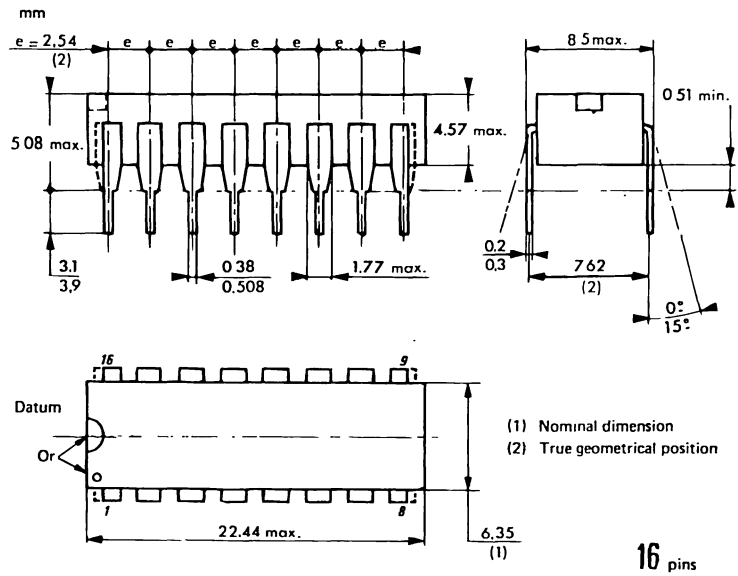
USER'S GUIDE FOR I_{PWF} AND R_{PWF} CHOICE



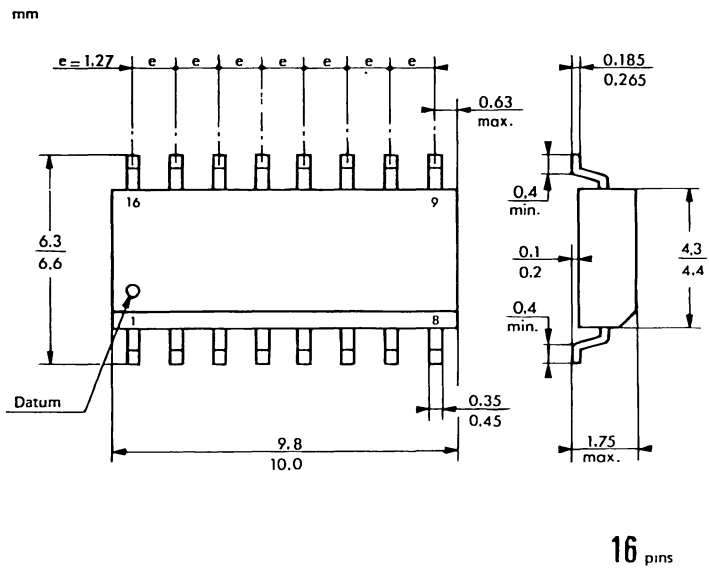
E88TSG8512-08

PACKAGE MECHANICAL DATA

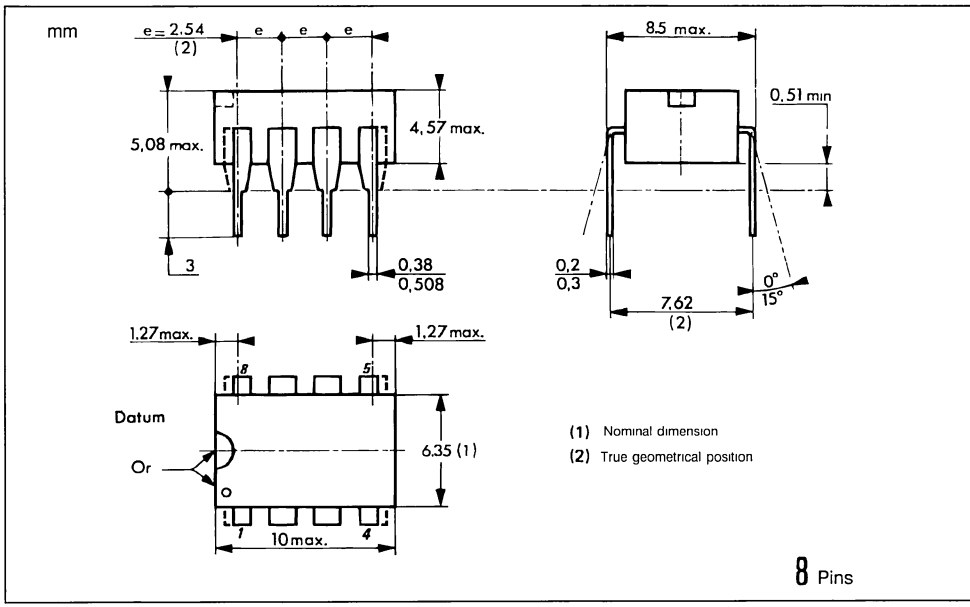
16 PINS - Plastic Dip



16 PINS - Plastic Micropackage



8 PINS - Plastic Dip



ORDER CODES

Plastic	16 Pins Package : TSG8512XP
Ceramic	16 Pins Package : TSG8512XC
Cerdip	16 Pins Package : TSG8512XJ
Plastic	8 Pins Package : TSG85121XP

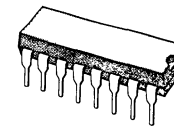
X : Temperature Range :

C :	0°C	+	70°C
I :	– 25°C	+	85°C
V :	– 40°C	+	85°C
M :	– 55°C	+	125°C

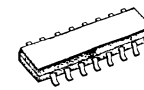
SWITCHED CAPACITOR MASK PROGRAMMABLE FILTER

- CHEBYCHEV TYPE
- 8TH ORDER
- STOPBAND ATTENUATION : 69dB (typ) AT 2 x F_C
- PASSBAND RIPPLE : 0.15dB (typ)
- CLOCK TO CUT-OFF FREQ; RATIO : 60
- CLOCK FREQUENCY RANGE : 1 TO 1500kHz
- CUT-OFF FREQUENCY RANGE : 16Hz TO 25kHz

Note : For general characteristics, see TSG85XX specifications. For non standard quality level, consult SGS-THOMSON general ordering information.



P
DIP-16
(Plastic Package)



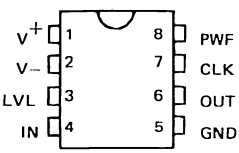
FP
SO-16
(Plastic Micropackage)

P
DIP-8
(Plastic Package)

DESCRIPTION

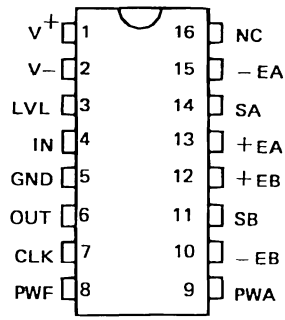
The TSG8513 is a HCMOS lowpass polynomial filter.

PIN CONNECTIONS



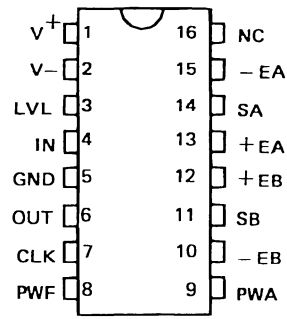
8 pins : FILTER ONLY
DIP-8 Package

E88TSG8513-01



16 pins : FILTER + 2 OP-AMPs
DIP-16 Package

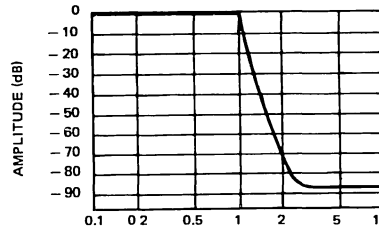
E88TSG8513-02



SO-16 Package

E88TSG8513-03

AMPLITUDE RESPONSE CURVE



E88TSG8513-04

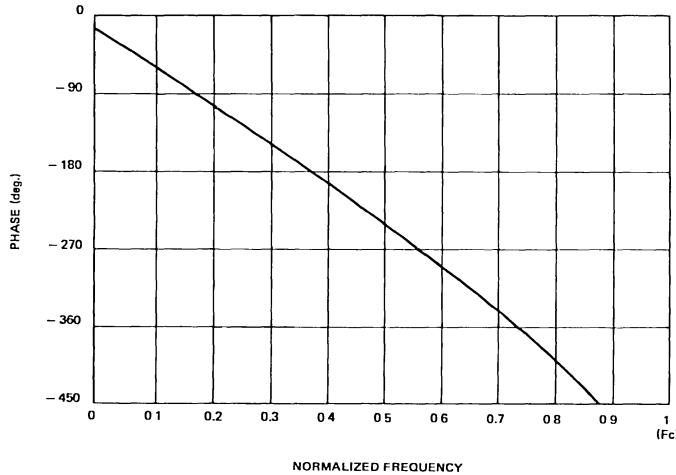
FILTER SPECIFICATIONS

Lowpass Filter : TSG8513 ; Type : Chebychev ; Order : 8.
$V^+ = 5V$, $V^- = -5V$, $T = 25°C$, $RL = 5k\Omega$, $CL = 100pF$, $I_{PWF} = 100\mu A$

Symbol	Parameter		Typ.	Tested Limits	Unit
Fe	External Clock Frequency		1 1500(*)		kHz (min) kHz (max)
Fi	Internal Sampling Freq.		0.5 750(*)		kHz (min) kHz (max)
Fe/Fc	Clock to Cutoff fr. Ratio		60 ± 1%		
Fc	Cutoff Frequency		0.016 25(*)		kHz (min) kHz (max)
G_o	Passband Gain		– 0.3 0		dB (min) dB (max)
Ap	Passband Ripple	Fe = 60kHz	0.15	0.5	dB (max)
As	Stopband Attenuation	Fe = 60kHz F > 2Fc	69	65	dB (min)
Voff	Output DC Offset Voltage	LVL = 0V	± 100	± 250	mV (max)
LVL	DC Level Adjustment		± 100		mV (max)
LG	Level gain		– 2.5		
R_{PWF}	PWF Resistance		10 72		kΩ (min) kΩ (max)
I_{PWF}	Input Current on PWF		50 250		µA (min) µA (max)
I^+	V^+ Supply Current	Fe = 100kHz Ipwa = 0µA	3.8	5	mA (max)
I^-	V^- Supply Current		3.8	5	mA (max)
$PSRR^+$	V^+ Supply Rejection Ratio	Fe = 120kHz Fin = 1kHz	25		dB
$PSRR^-$	V^- Supply Rejection Ratio		40		dB
R_{IN}	Input Resistance		3		MΩ
C_{IN}	Input Capacitance		20		pF
Vo	Output Voltage Swing		+ 3.5 – 4.5		Vp-p (max)
Vn	Output Noise	BW = 1kHz Fe = 60kHz Vin = 2Vrms	107		µVrms
SNR	Signal to Noise Ratio		85		dB

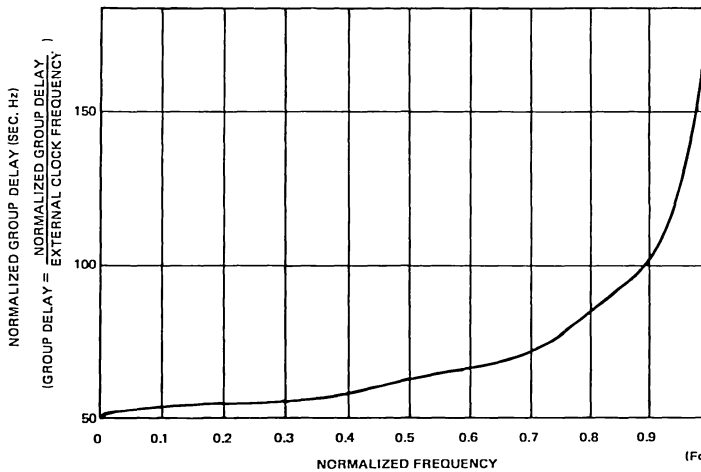
(*) At maximum Fe . - stopband attenuation As > 55dB for f > 2Fc
(with $I_{pwf} = 250\mu A$) - passband ripple : $A_p = 0.8dB$
- passband gain : $G_0 = -0.6dB$

PHASE RESPONSE CURVE (in passband)



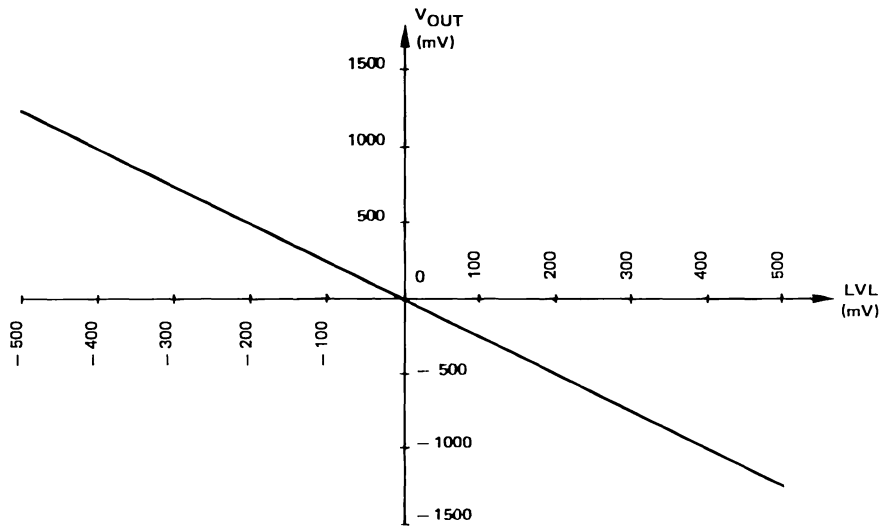
E88TSG8513-05

GROUP DELAY CURVE (in passband)



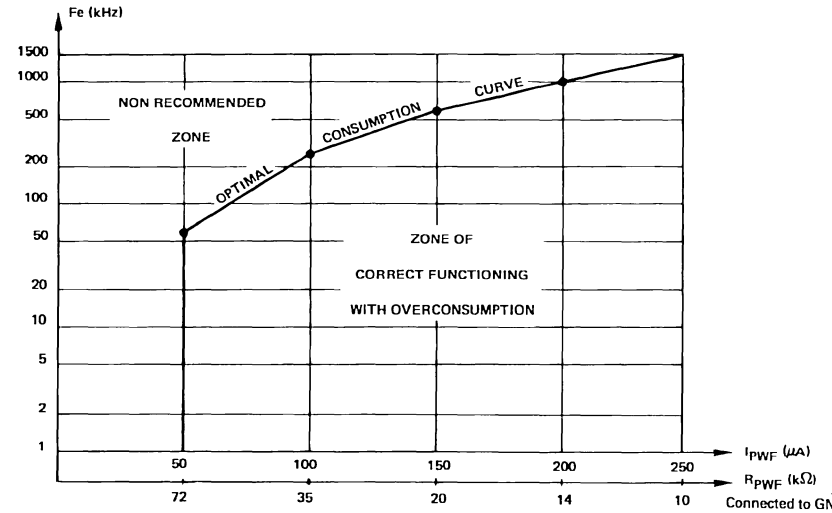
E88TSG8513-06

OUTPUT DC VOLTAGE ADJUSTMENT FROM LVL PIN



E88TSG8513-07

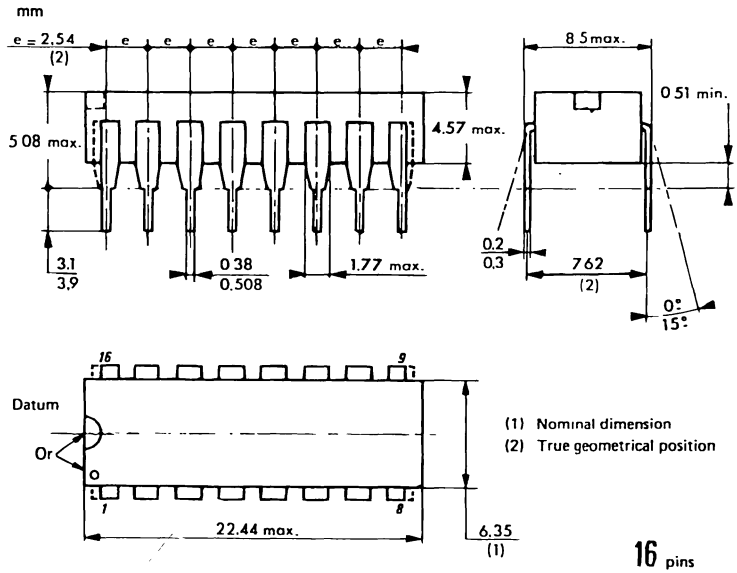
USER'S GUIDE FOR I_{PWF} AND R_{PWF} CHOICE



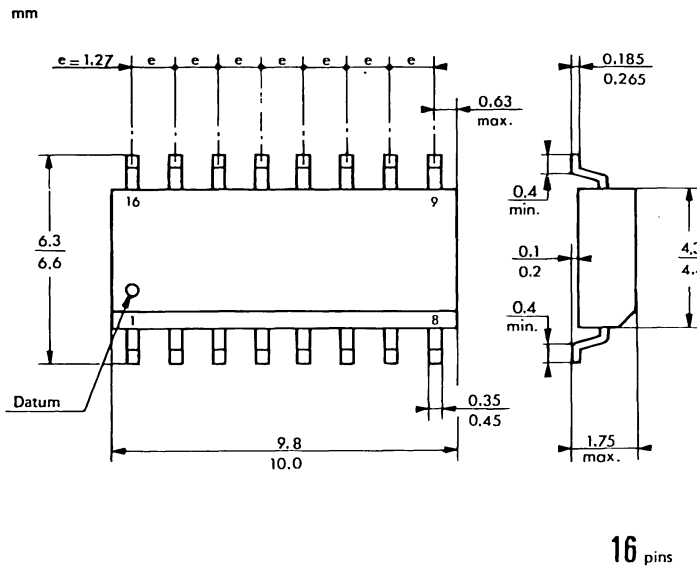
E88TSG8513-08

PACKAGE MECHANICAL DATA

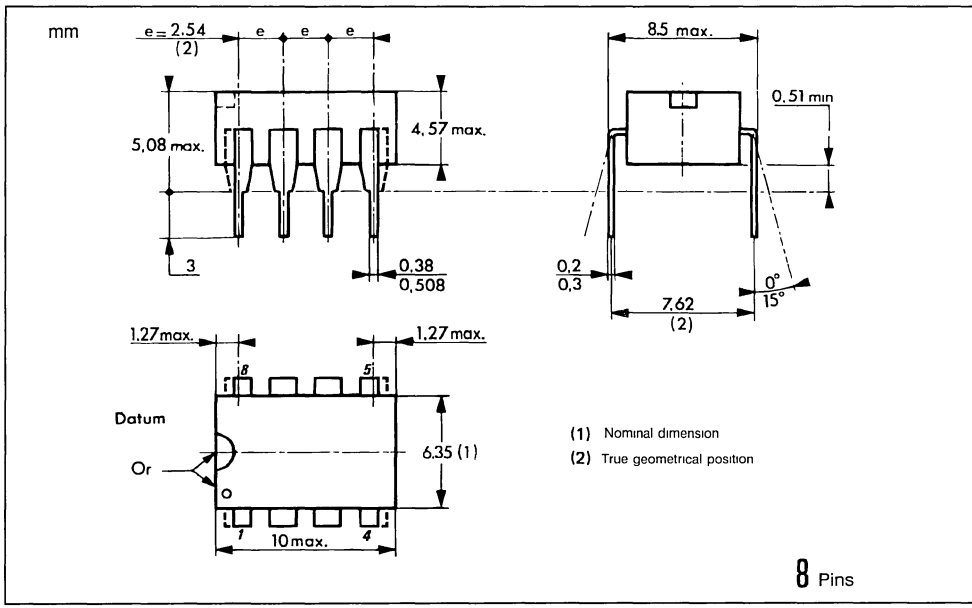
16 PINS - Plastic Dip



16 PINS - Plastic Micropackage



8 PINS - Plastic Dip



ORDER CODES

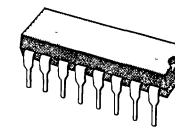
Plastic	16 Pins Package : TSG8513XP
Ceramic	16 Pins Package : TSG8513XC
Cerdip	16 Pins Package : TSG8513XJ
Plastic	8 Pins Package : TSG85131XP

X : Temperature Range = I : 0°C + 70°C
C : – 25°C + 85°C
V : – 40°C + 85°C
M : – 55°C + 125°C

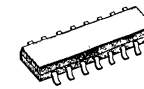
SWITCHED CAPACITOR MASK PROGRAMMABLE FILTER

- BUTTERWORTH TYPE
- 8TH ORDER
- STOPBAND ATTENUATION : 74dB (typ) AT 3.6 x F_C
- PASSBAND RIPPLE : MAXIMALLY FLAT
- CLOCK TO CUT-OFF FREQ. RATIO : 80
- CLOCK FREQUENCY RANGE : 1 TO 1000kHz
- CUT-OFF FREQUENCY RANGE : 12.5Hz TO 12.5kHz

Note : For general characteristics, see TSG85XX specifications. For non standard quality level, consult SGS-THOMSON general ordering information.



P
DIP-16
(Plastic Package)



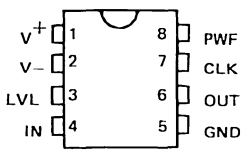
FP
SO-16
(Plastic Micropackage)

P
DIP-8
(Plastic Package)

DESCRIPTION

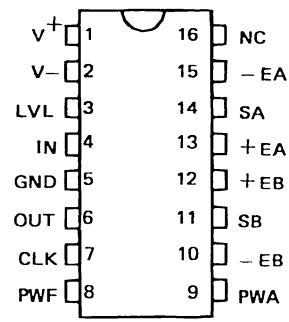
The TSG8514 is a HCMOS lowpass polynomial filter.

PIN CONNECTIONS



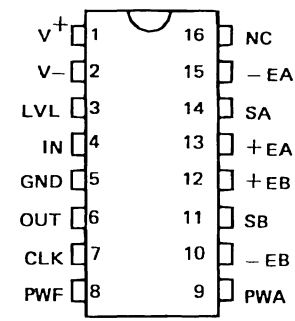
8 pins : FILTER ONLY
DIP-8 Package

E88TSG8514-01



16 pins : FILTER + 2 OP-AMPs
DIP-16 Package

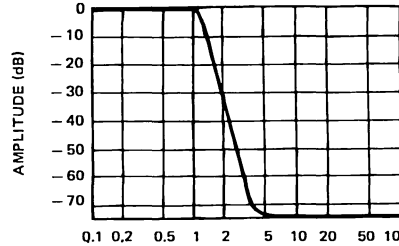
E88TSG8514-02



SO-16 Package

E88TSG8514-03

AMPLITUDE RESPONSE CURVE



E88TSG8514-04

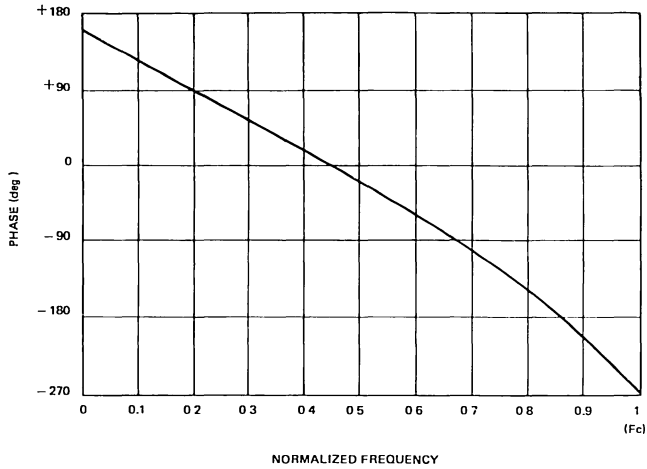
FILTER SPECIFICATIONS

Lowpass Filter : TSG8514 ; Type : Butterworth ; Order : 8.
$V^+ = 5V$, $V^- = -5V$, T = 25°C, RL = 5kΩ, CL = 100pF, $I_{PWF} = 100\mu A$

Symbol	Parameter		Typ.	Tested Limits	Unit
Fe	External Clock Frequency		1 1000(*)		kHz (min) kHz (max)
Fi	Internal Sampling Freq.		0.5 500(*)		kHz (min) kHz (max)
Fe/Fc	Clock to Cutoff fr. Ratio		80 ± 1%		
Fc	Cutoff Frequency		0.0125 12.5(*)		kHz (min) kHz (max)
G_o	Passband Gain		– 0.3 0		dB (mın) dB (max)
Ap	Passband Ripple	Fe = 80kHz	maxi mally Flat		dB (max)
As	Stopband Attenuation	Fe = 80kHz F > 3.6 Fc	74	68	dB (min)
Voff	Output DC Offset Voltage	LVL = 0V	± 100	± 200	mV (max)
LVL	DC Level Adjustment		± 100		mV
LG	Level gain		– 2		
R_{PWF}	PWF Resistance		10 72		kΩ (min) kΩ (max)
I_{PWF}	Input Current on PWF		50 250		µA (min) µA (max)
I^+	V^+ Supply Current	Fe = 100kHz I_{pwa} = 0µA	3.8	5	mA (max)
I^-	V^- Supply Current		3.8	5	mA (max)
$PSRR^+$	V^+ Supply Rejection Ratio	Fe = 160kHz Fin = 1kHz	30		dB
$PSRR^-$	V^- Supply Rejection Ratio		42		dB
R_{IN}	Input Resistance		3		MΩ
C_{IN}	Input Capacitance		20		pF
Vo	Output Voltage Swing		+ 3.5 – 4.5		Vp-p (max)
Vn	Output Noise	BW = 3.4kHz Fe = 256kHz Vin = 2Vrms	86		µVrms
SNR	Signal to Noise Ratio		87		dB

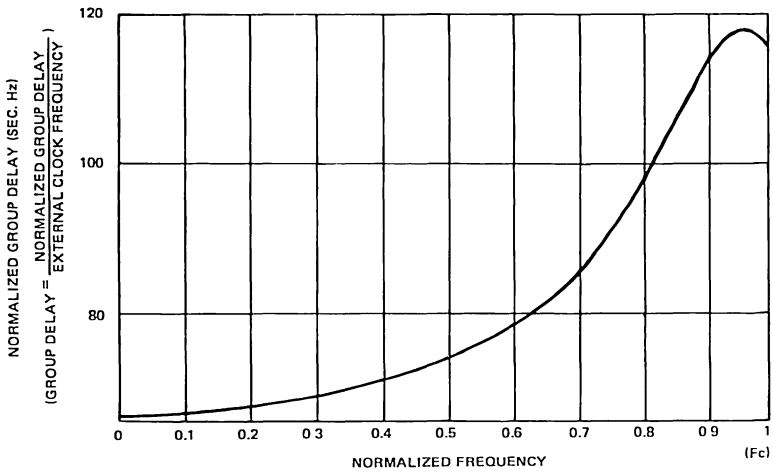
(*) At maximum Fe - stopband attenuation As > 50dB for F > 3 6Fc
(with I_{pwf} = 250µA) - passband gain : G_0 = – 0.5dB

PHASE RESPONSE CURVE (in passband)



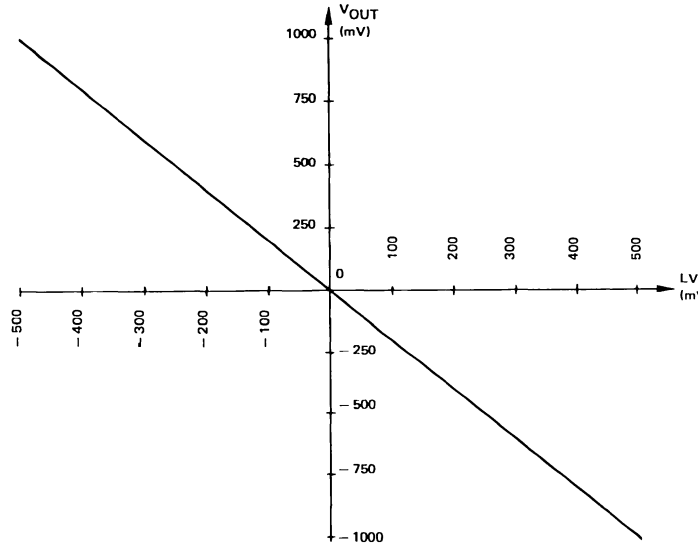
E88TSG8514-05

GROUP DELAY CURVE (in passband)



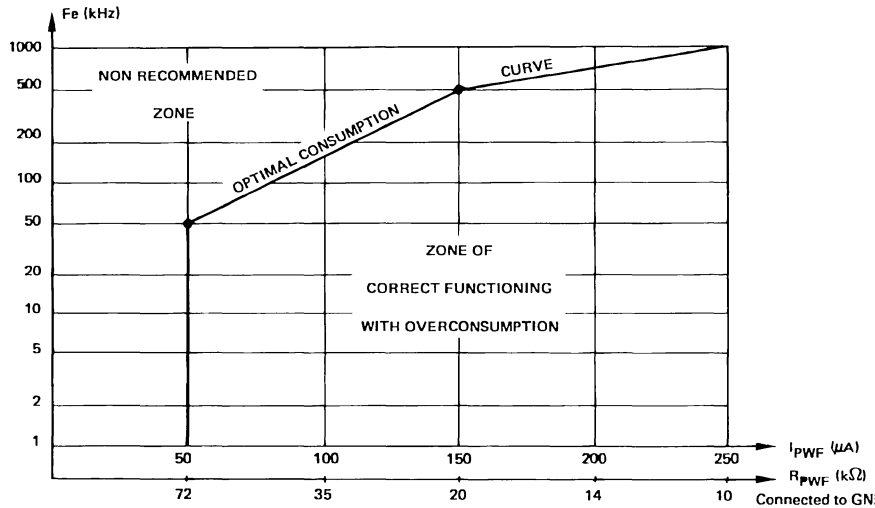
E88TSG8514-06

OUTPUT DC VOLTAGE ADJUSTMENT FROM LVL PIN



E88TSG8514-07

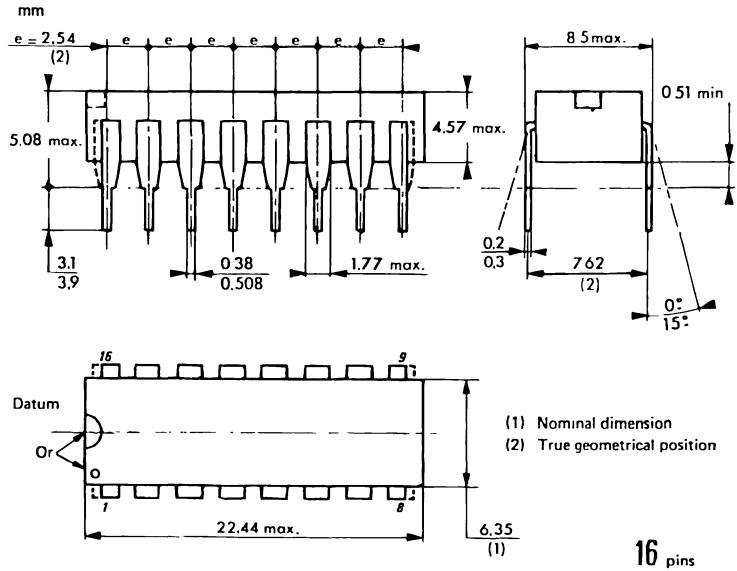
USER'S GUIDE FOR I_{PWF} AND R_{PWF} CHOICE



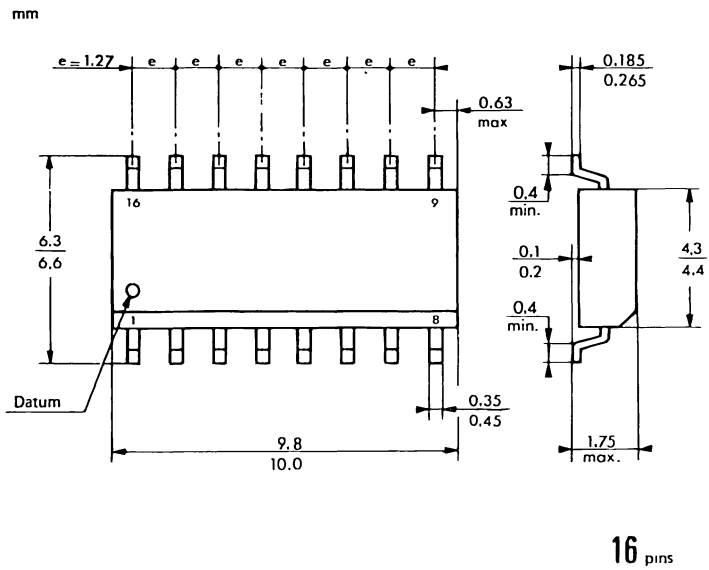
E88TSG8514-08

PACKAGE MECHANICAL DATA

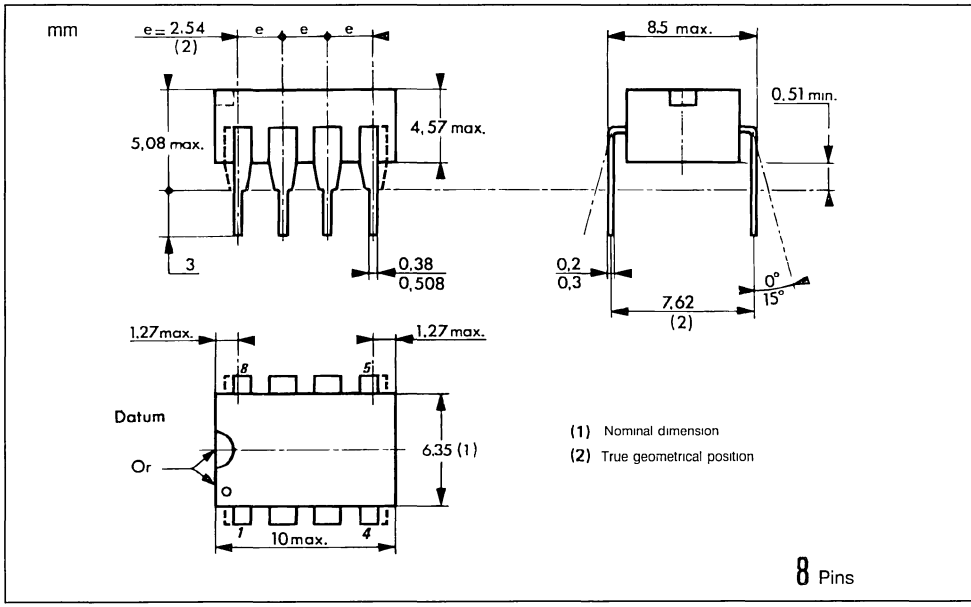
16 PINS - Plastic Dip



16 PINS - Plastic Micropackage



8 PINS - Plastic Dip



ORDER CODES

Plastic	16 Pins Package : TSG8514XP
Ceramic	16 Pins Package : TSG8514XC
Cerdip	16 Pins Package : TSG8514XJ
Plastic	8 Pins Package : TSG85141XP

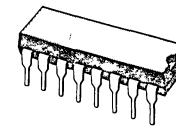
X : Temperature Range = C : 0°C + 70°C
I : – 25°C + 85°C
V : – 40°C + 85°C
M : – 55°C + 125°C

SWITCHED CAPACITOR MASK PROGRAMMABLE FILTER

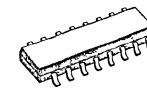
- CAUER TYPE
- 3TH ORDER
- STOPBAND ATTENUATION : 15dB (typ)
- PASSBAND RIPPLE : 0.2dB (typ)
- CLOCK TO CUT-OFF FREQ. RATIO : 320
- CLOCK FREQUENCY RANGE : 4 TO 2400kHz
- CUT-OFF FREQUENCY RANGE : 12Hz TO 7.5kHz

* According to spectrum aliasing phenomenon, the TSG8530 must be considered as a highpass filter only in the range [Fc, Fi/2], where Fi is the internal sampling frequency.

Note : For general characteristics, see TSG85XX specifications. For non standard quality level, consult SGS-THOMSON general ordering information.



P
DIP-16
(Plastic Package)



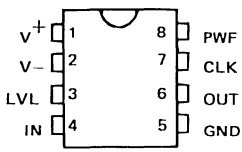
FP
SO-16
(Plastic Micropackage)

P
DIP-8
(Plastic Package)

DESCRIPTION

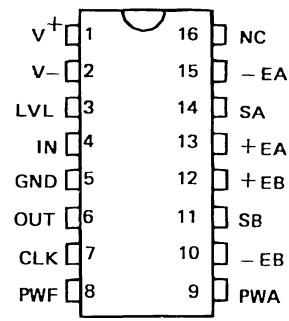
The TSG8530 is a HCMOS highpass* elliptic filter.

PIN CONNECTIONS



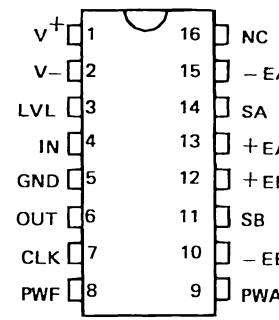
8 pins : FILTER ONLY
DIP-8 Package

E88TSG8530-01



16 pins : FILTER + 2 OP-AMPs
DIP-16 Package

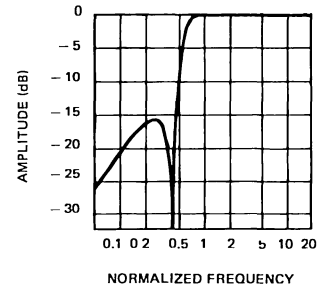
E88TSG8530-02



SO-16 Package

E88TSG8530-03

AMPLITUDE RESPONSE CURVE



E88TSG8530-04

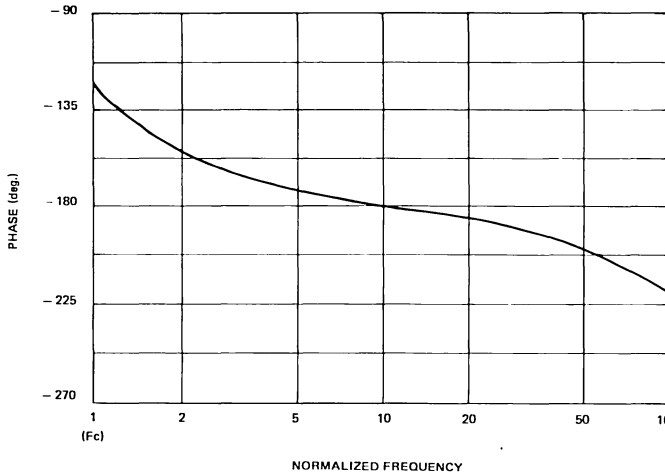
FILTER SPECIFICATIONS

Highpass Filter : TSG8530 ; Type : Cauer ; Order : 3.
$V^+ = 5V$, $V^- = -5V$, $T = 25°C$, $RL = 5k\Omega$, $CL = 100pF$, $I_{PWF} = 100\mu A$

Symbol	Parameter		Typ.	Tested Limits	Unit
Fe	External Clock Frequency		4 2400(*)		kHz (min) kHz (max)
Fi	Internal Sampling Freq.		2 1200(*)		kHz (min) kHz (max)
Fe/Fc	Clock to Cutoff fr. Ratio		320 ± 1%		
Fc	Cutoff Frequency		0.0125 7.5(*)		kHz (min) kHz (max)
G_o	Passband Gain		– 0.3 0		dB (min) dB (max)
Ap	Passband Ripple	[Fc, 30Fc] Fe = 320kHz	0.2	0.5	dB (max)
As	Stopband Attenuation	F < 0.49Fc Fe = 320kHz	15	14	dB (min)
Voff	Output DC Offset Voltage	LVL = 0V	± 100	± 200	mV (max)
LVL	DC Level Adjustment		± 40		mV
LG	Level gain		– 6		
R_{PWF}	PWF Resistance		10 72		kΩ (min) kΩ (max)
I_{PWF}	Input Current on PWF		50 250		µA (min) µA (max)
I^+	V^+ Supply Current	Fe = 100kHz Ipwa = 0µA	2.8	5	mA (max)
I^-	V^- Supply Current		2.8	5	mA (max)
$PSRR^+$	V^+ Supply Rejection Ratio	Fe = 32kHz Fin = 1kHz	33		dB
$PSRR^-$	V^- Supply Rejection Ratio		38		dB
R_{IN}	Input Resistance		3		MΩ
C_{IN}	Input Capacitance		20		pF
Vo	Output Voltage Swing		+ 3.5 – 4.5		Vp-p (max)
Vn	Output Noise	BW = 2kHz Fe = 32kHz Vin = 2Vrms	80		µVrms
SNR	Signal to Noise Ratio		85		dB

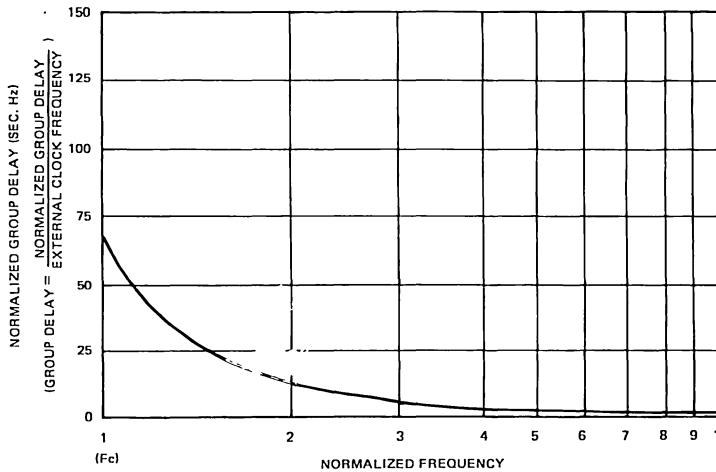
(*) At maximum Fe . - stopband attenuation As > 14dB for F < 0.49Fc
(with $I_{pwf} = 250\mu A$) - passband ripple $A_p = 0.2dB$
- passband gain $G_0 = -0.6dB$

PHASE RESPONSE CURVE (in passband)



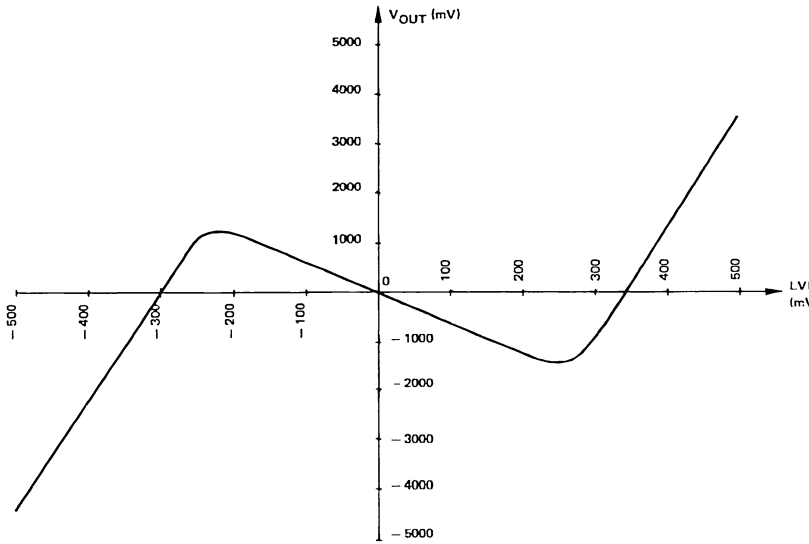
E88TSG8530-05

GROUP DELAY CURVE (in passband)



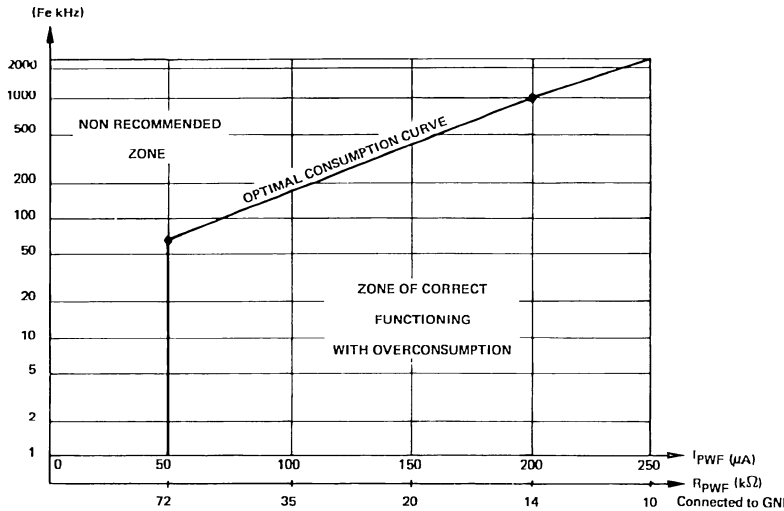
E88TSG8530-06

OUTPUT DC VOLTAGE ADJUSTMENT FROM LVL PIN



E88TSG8530-07

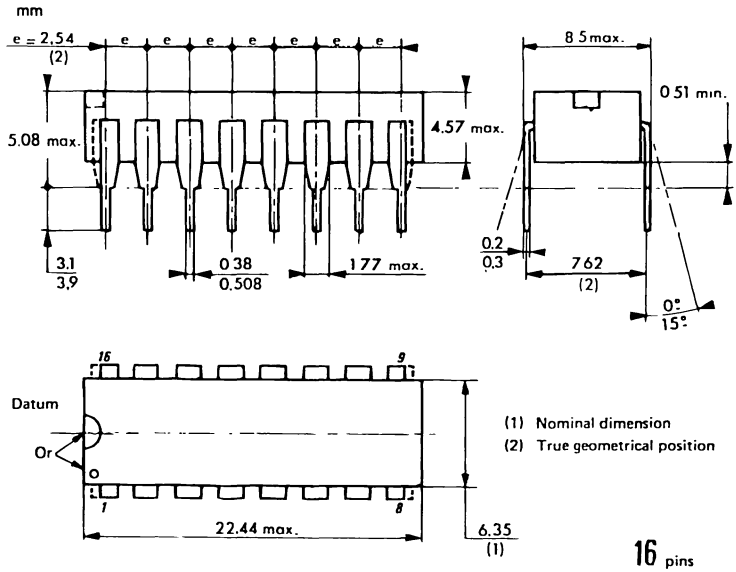
USER'S GUIDE FOR I_{PWF} AND R_{PWF} CHOICE



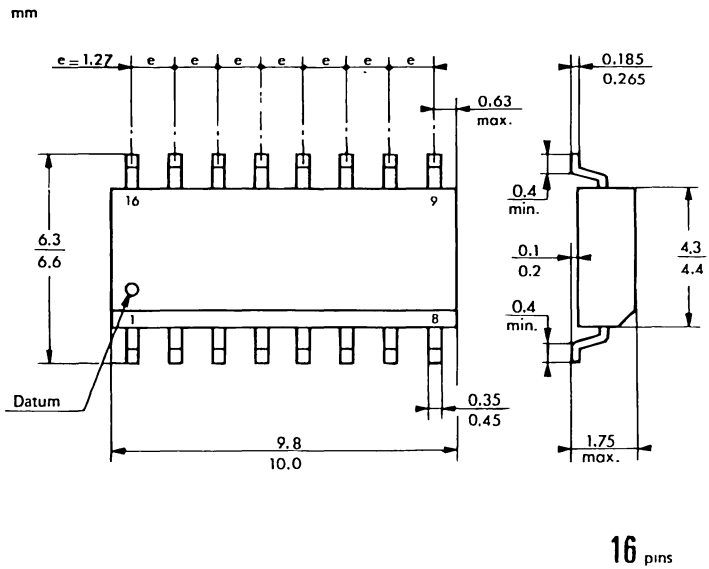
E88TSG8530-08

PACKAGE MECHANICAL DATA

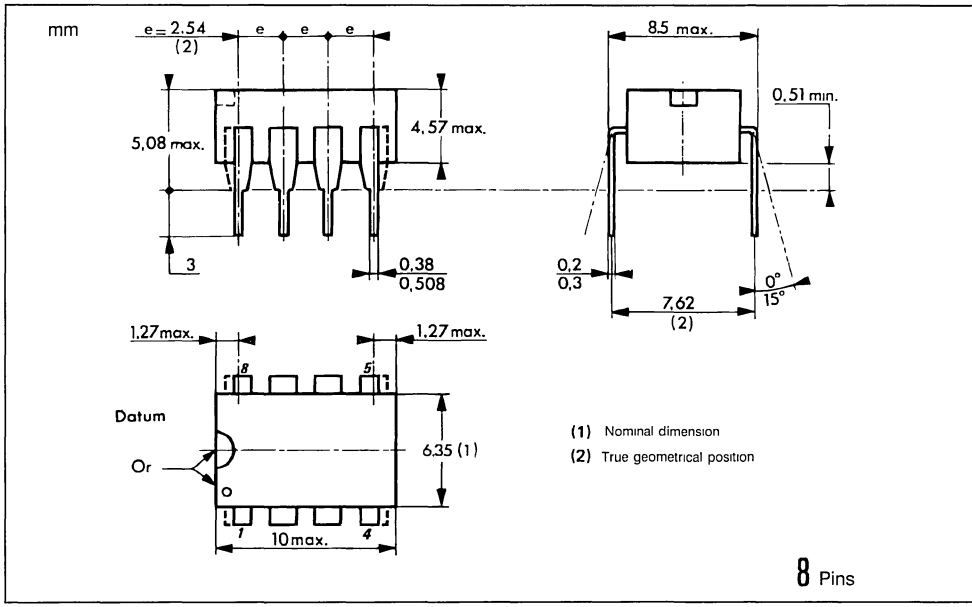
16 PINS - Plastic Dip



16 PINS - Plastic Micropackage



8 PINS - Plastic Dip



ORDER CODES

Plastic	16 Pins Package : TSG8530XP
Ceramic	16 Pins Package : TSG8530XC
Cerdip	16 Pins Package : TSG8530XJ
Plastic	8 Pins Package : TSG85301XP

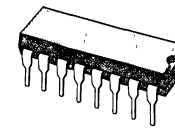
X : Temperature Range = C : 0°C + 70°C
I : − 25°C + 85°C
V : − 40°C + 85°C
M : − 55°C + 125°C

SWITCHED CAPACITOR MASK PROGRAMMABLE FILTER

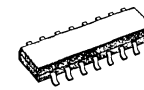
- CAUER TYPE
- 6TH ORDER
- STOPBAND ATTENUATION : 32dB (typ)
- PASSBAND RIPPLE : 0.15dB (typ)
- CLOCK TO CUT-OFF FREQ. RATIO : 400
- CLOCK FREQUENCY RANGE : 4 TO 1800kHz
- CUT-OFF FREQUENCY RANGE : 10Hz to 4.5kHz

* According to spectrum aliasing phenomenon, the TSG8531 must be considered as a highpass filter only in the range [Fc, Fi/2], where Fi is the internal sampling frequency.

Note : For general characteristics, see TSG85XX specifications. For non standard quality level, consult SGS-THOMSON general ordering information.



P
DIP-16
(Plastic Package)



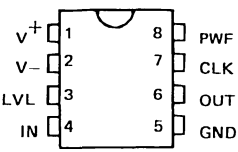
FP
SO-16
(Plastic Micropackage)

P
DIP-8
(Plastic Package)

DESCRIPTION

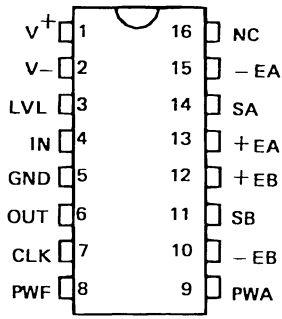
The TSG8531 is a HCMOS highpass* elliptic filter.

PIN CONNECTIONS



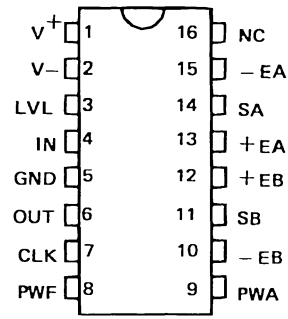
8 pins : FILTER ONLY
DIP-8 Package

E88TSG8531-01



16 pins : FILTER + 2 OP-AMPs
DIP-16 Package

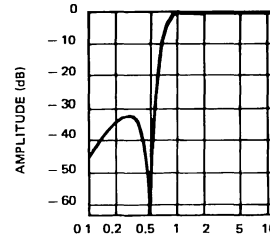
E88TSG8531-02



SO-16 Package

E88TSG8531-03

AMPLITUDE RESPONSE CURVE



E88TSG8531-04

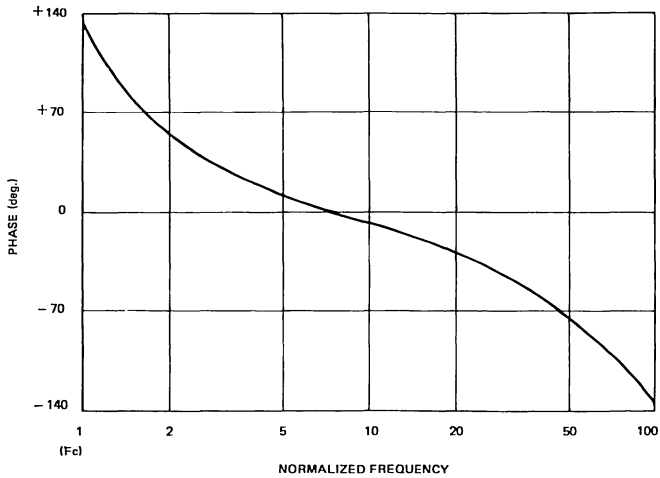
FILTER SPECIFICATIONS

Highpass Filter : TSG8531 ; Type : Cauer ; Order : 6.
$V^+ = 5V$, $V^- = -5V$, T = 25°C, RL = 5kΩ, CL = 100pF, $I_{PWF} = 100\mu A$

Symbol	Parameter		Typ.	Tested Limits	Unit
Fe	External Clock Frequency		4 1800(*)		kHz (min) kHz (max)
Fi	Internal Sampling Freq.		2 900(*)		kHz (min) kHz (max)
Fe/Fc	Clock to Cutoff fr. Ratio		400 ± 1%		
Fc	Cutoff Frequency		0.01 4.5(*)		kHz (min) kHz (max)
G_o	Passband Gain		– 0.1 0.1		dB (min) dB (max)
Ap	Passband Ripple	[Fc, 30Fc] Fe = 400kHz	0.15	0.4	dB (max)
As	Stopband Attenuation	F < 0.55Fc Fe = 400kHz	32	30	dB (min)
Voff	Output DC Offset Voltage	LVL = 0V	± 100	± 200	mV (max)
LVL	DC Level Adjustment		± 300		mV
LG	Level gain		0.1		
R_{PWF}	PWF Resistance		10 72		kΩ (min) kΩ (max)
I_{PWF}	Input Current on PWF		50 250		µA (min) µA (max)
I^+	V^+ Supply Current	Fe = 100kHz Ipwa = 0µA	3.5	5	mA (max)
I^-	V^- Supply Current		3.5	5	mA (max)
$PSRR^+$	V^+ Supply Rejection Ratio	Fe = 40kHz Fin = 1kHz	36		dB
$PSRR^-$	V^- Supply Rejection Ratio		48		dB
R_{IN}	Input Resistance		3		MΩ
C_{IN}	Input Capacitance		20		pF
Vo	Output Voltage Swing		+ 3.5 – 4.5		Vp-p (max)
Vn	Output Noise	BW = 2kHz Fe = 40kHz Vin = 2Vrms	178		µVrms
SNR	Signal to Noise Ratio		80		dB

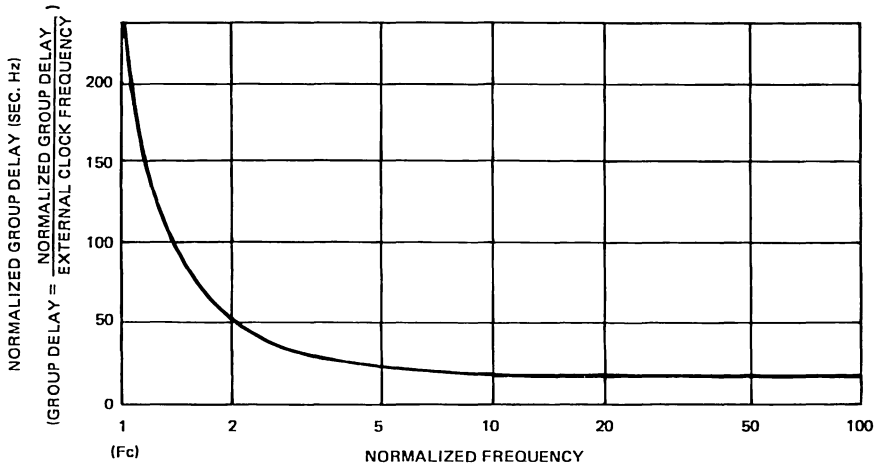
(*) At maximum Fe - stopband attenuation As > 30dB for F < 0.55Fc
(with $I_{pwf} = 250\mu A$) - passband ripple : $A_p = 0.3dB$
- passband gain . $G_0 = -1dB$

PHASE RESPONSE CURVE (in passband)



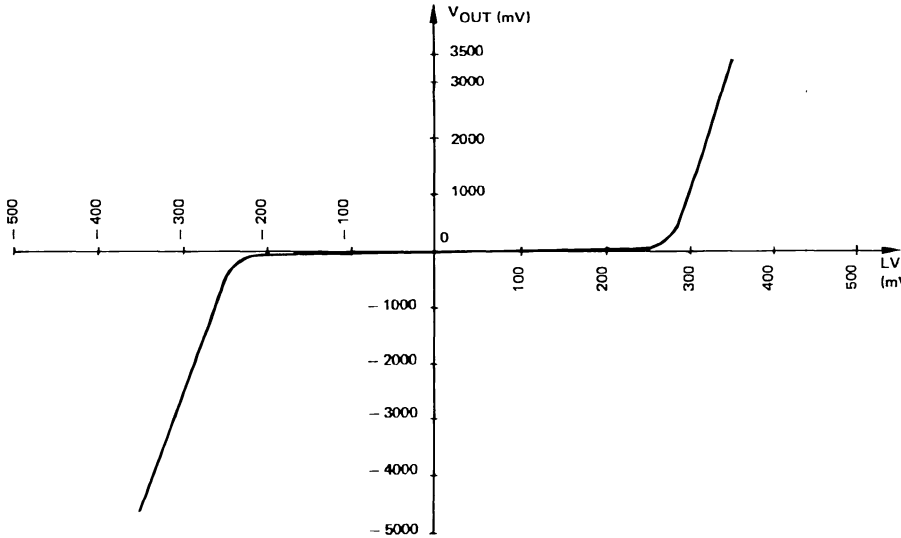
E88TSG8531-05

GROUP DELAY CURVE (in passband)



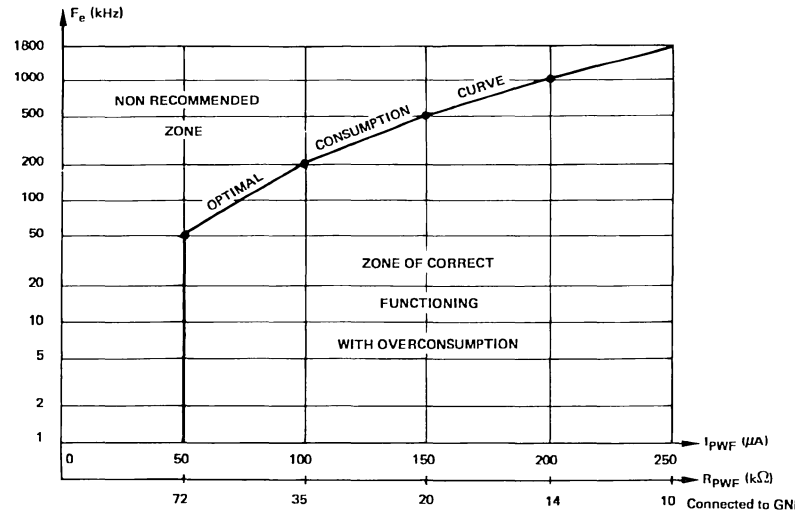
E88TSG8531-06

OUTPUT DC VOLTAGE ADJUSTMENT FROM LVL PIN



E88TSG8531-07

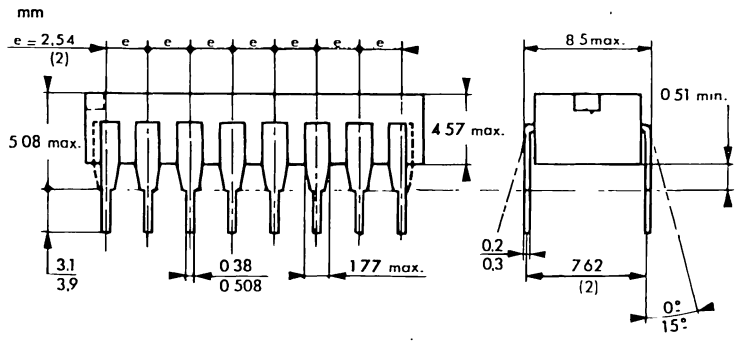
USER'S GUIDE FOR I_{PWF} AND R_{PWF} CHOICE



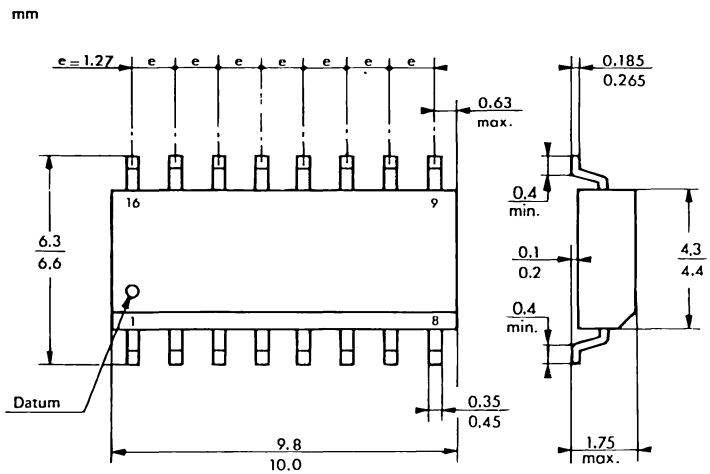
E88TSG8531-08

PACKAGE MECHANICAL DATA

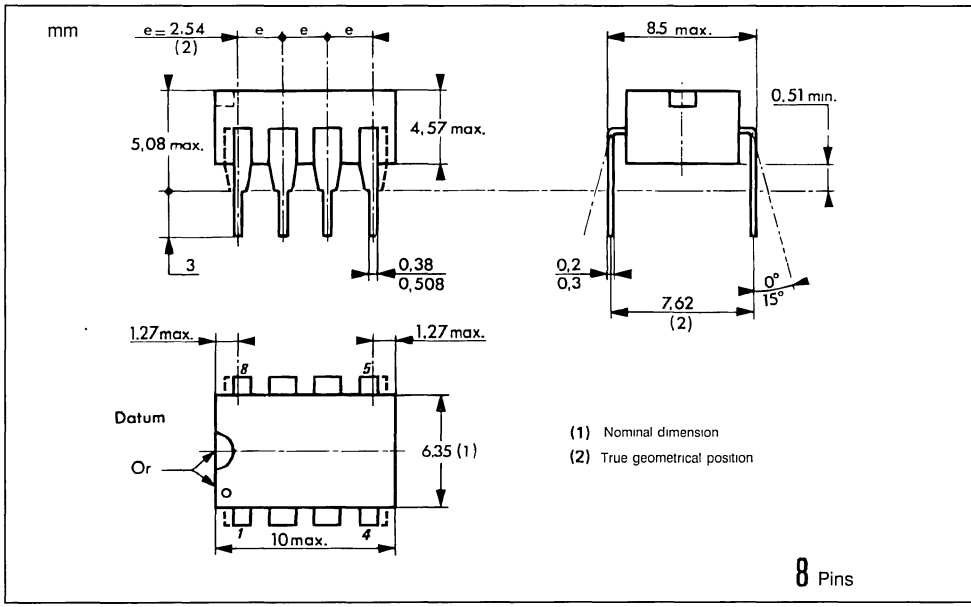
16 PINS - Plastic Dip



16 PINS - Plastic Micropackage



8 PINS - Plastic Dip



ORDER CODES

Plastic	16 Pins Package : TSG8531XP
Ceramic	16 Pins Package : TSG8531XC
Cerdip	16 Pins Package : TSG8531XJ
Plastic	8 Pins Package : TSG85311XP

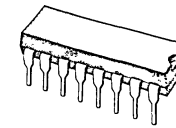
X : Temperature Range = C : 0°C + 70°C
I : – 25°C + 85°C
V : – 40°C + 85°C
M : –55°C + 125°C

SWITCHED CAPACITOR MASK PROGRAMMABLE FILTER

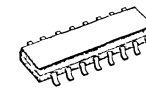
- CHEBYCHEV TYPE
- 6TH ORDER
- STOPBAND ATTENUATION : 60dB (typ) AT 0.25 x F_C
- PASSBAND RIPPLE : 0.45dB (typ)
- CLOCK TO CUT-OFF FREQ. RATIO : 500
- CLOCK FREQUENCY RANGE : 5 TO 1800kHz
- CUT-OFF FREQUENCY RANGE : 10Hz TO 3.6kHz

* According to spectrum aliasing phenomenon, the TSG8532 must be considered as a highpass filter only in the range [Fc, Fi/2], where Fi is the internal sampling frequency.

Note : For general characteristics, see TSG85XX specifications. For non standard quality level, consult SGS-THOMSON general ordering information



P
DIP-16
(Plastic Package)



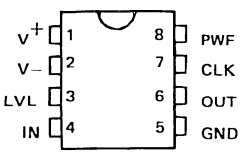
FP
SO-16
(Plastic Micropackage)

P
DIP-8
(Plastic Package)

DESCRIPTION

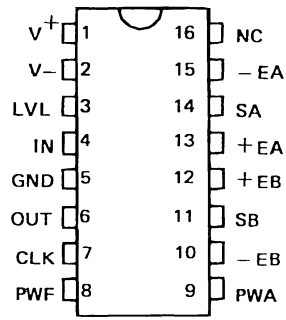
The TSG8532 is a HCMOS highpass* polynomial filter.

PIN CONNECTIONS



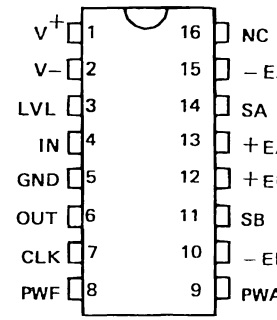
8 pins : FILTER ONLY
DIP-8 Package

E88TSG8532-01



16 pins : FILTER + 2 OP-AMPs
DIP-16 Package

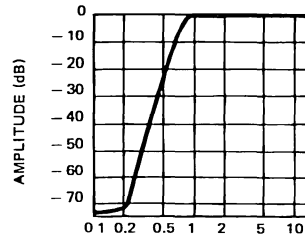
E88TSG8532-02



SO-16 Package

E88TSG8532-03

AMPLITUDE RESPONSE CURVE



E88TSG8532-04

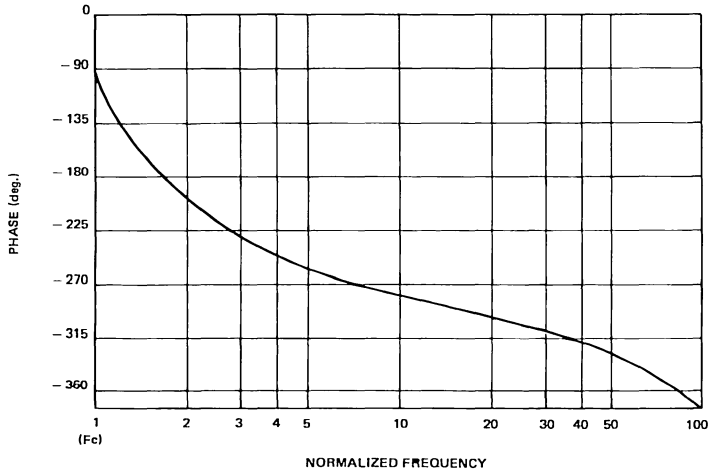
FILTER SPECIFICATIONS

Highpass Filter : TSG8532 ; Type : Chebychev ; Order : 6.
V^+ = 5V, V^- = – 5V, T = 25°C, RL = 5kΩ, CL = 100pF, I_{PWF} = 100µA

Symbol	Parameter		Typ.	Tested Limits	Unit
Fe	External Clock Frequency		5 1800(*)		kHz (min) kHz (max)
Fi	Internal Sampling Frequency		2.5 900(*)		kHz (min) kHz (max)
Fe/Fc	Clock to Cutoff fr. Ratio		500 ± 1%		
Fc	Cutoff Frequency		0.01 3.6(*)		kHz (min) kHz (max)
G_o	Passband Gain		– 0.4 0		dB (min) dB (max)
Ap	Passband Ripple	[1Fc, 45Fc] Fe = 500kHz	0.45	0.8	dB (max)
As	Stopband Attenuation	F < 0.25Fc Fe = 500kHz	60	55	dB (min)
Voff	Output DC Offset Voltage	LVL = 0V	± 80	± 200	mV (max)
LVL	DC Level Adjustment		± 75		mV (max)
LG	Level gain		– 2.7		
R_{PWF}	PWF Resistance		10 72		kΩ (min) kΩ (max)
I_{PWF}	Input Current on PWF		50 250		µA (min) µA (max)
I^+	V^+ Supply Current	Fe = 100kHz Ipwa = 0µA	3.4	5	mA (max)
I^-	V^- Supply Current		3.4	5	mA (max)
$PSRR^+$	V^+ Supply Rejection Ratio	Fe = 50kHz Fin = 1kHz	49		dB
$PSRR^-$	V^- Supply Rejection Ratio		46		dB
R_{IN}	Input Resistance		3		MΩ
C_{IN}	Input Capacitance		20		pF
Vo	Output Voltage Swing		+ 3.5 – 4.5		Vp-p (max)
Vn	Output Noise	BW = 2kHz Fe = 50kHz Vin = 2Vrms	88		µVrms
SNR	Signal to Noise Ratio		85		dB

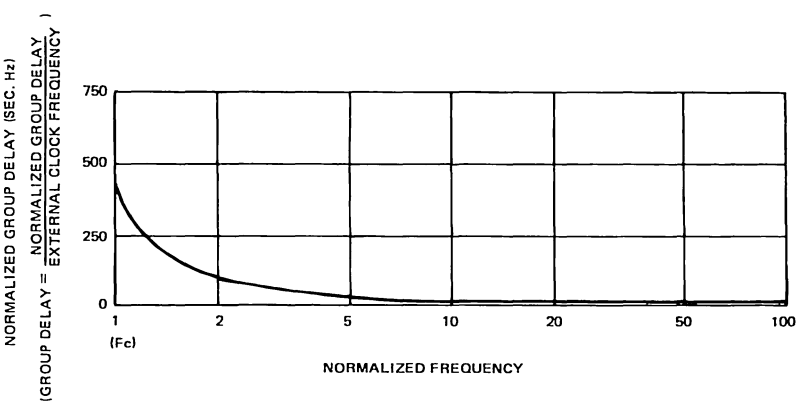
(*) At maximum Fe ·
(with I_{pwf} = 250µA) - passband ripple · A_p = 0 8dB
- passband gain · G_0 = – 0.8dB

PHASE RESPONSE CURVE (in passband)



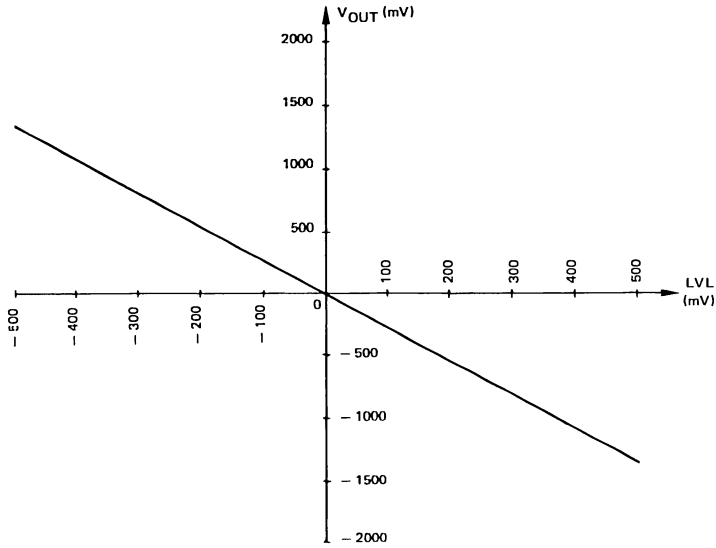
E88TSG8532-05

GROUP DELAY CURVE (in passband)



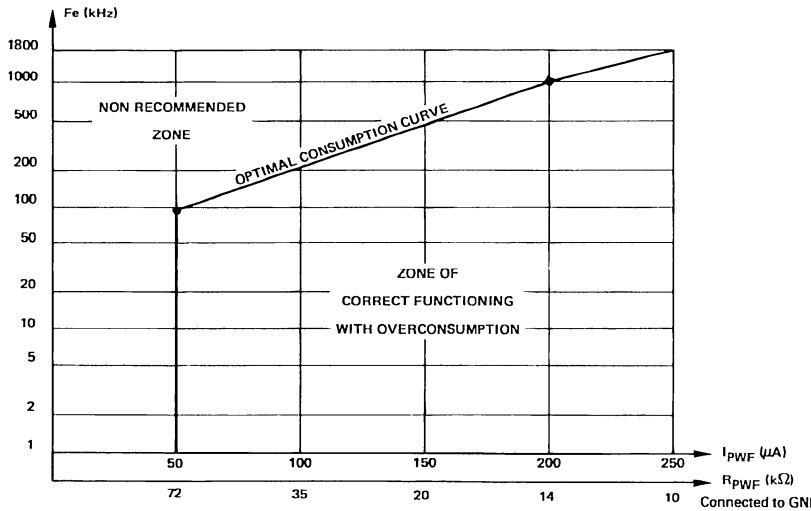
E88TSG8532-06

OUTPUT DC VOLTAGE ADJUSTMENT FROM LVL PIN



E88TSG8532-07

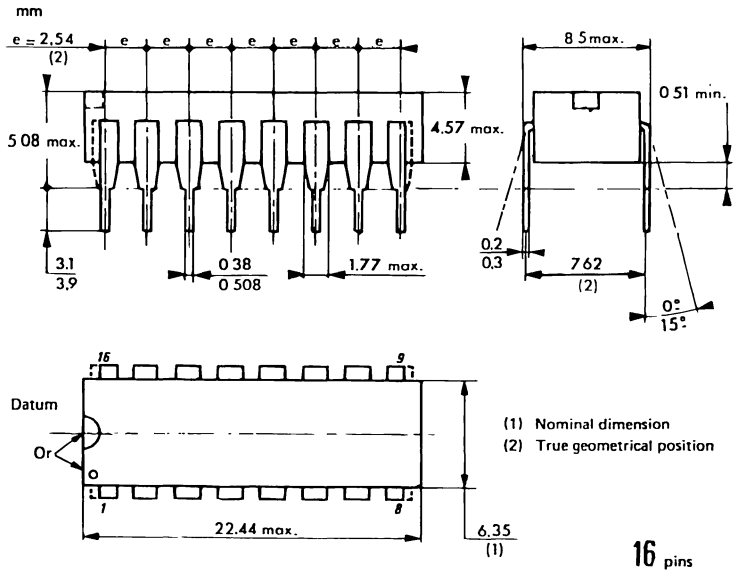
USER'S GUIDE FOR I_{PWF} AND R_{PWF} CHOICE



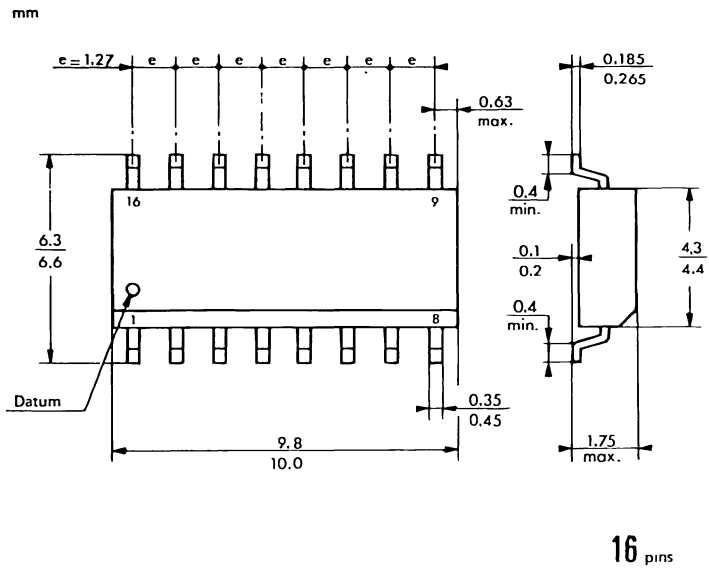
E88TSG8532-08

PACKAGE MECHANICAL DATA

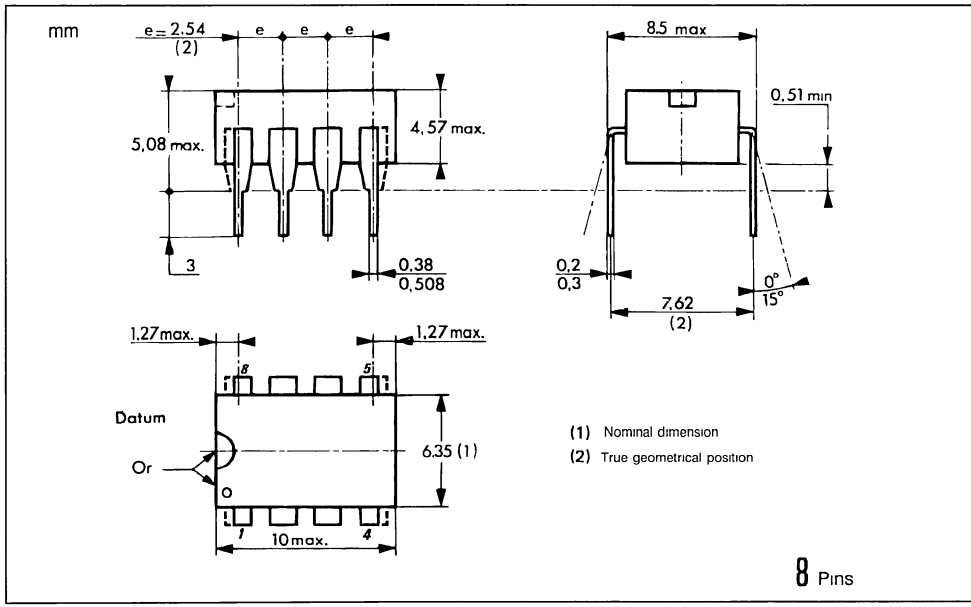
16 PINS - Plastic Dip



16 PINS - Plastic Micropackage



8 PINS - Plastic Dip



ORDER CODES

Plastic	16 Pins Package : TSG8532XP
Ceramic	16 Pins Package : TSG8532XC
Cerdip	16 Pins Package : TSG8532XJ
Plastic	8 Pins Package : TSG85321XP

X : Temperature Range = C : 0°C + 70°C
I : – 25°C + 85°C
V : – 40°C + 85°C
M : – 55°C + 125°C

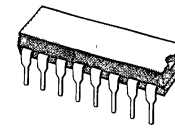
SGS-THOMSON MICROELECTRONICS

TSG8540

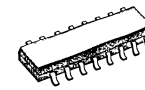
SWITCHED CAPACITOR FILTER

- 6TH ORDER
- SELECTIVITY FACTOR : Q = 5
- ATTENUATION AT CENTER FREQUENCY FROM 36dB TO 56dB DEPENDING ON CENTER FREQUENCY
- TYPICAL CLOCK TO CENTER FREQUENCY RATIO : 925
- CLOCK FREQUENCY RANGE : 18.5kHz TO 1110kHz
- CENTER FREQUENCY RANGE : 20Hz TO 1200Hz

Note : For general characteristics, see TSGF08 specifications. For non standard quality level, consult SGS-THOMSON general ordering information.



P
DIP-16
(Plastic Package)



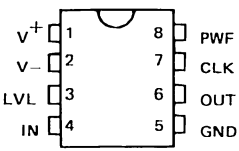
FP
SO-16
(Plastic Micropackage)

P
DIP-8
(Plastic Package)

DESCRIPTION

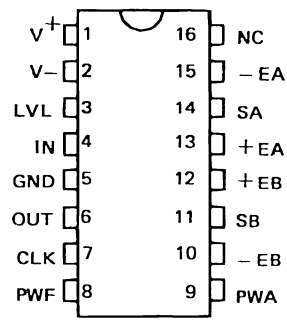
The TSG8540 is a HCMOS bandreject filter.

PIN CONNECTIONS



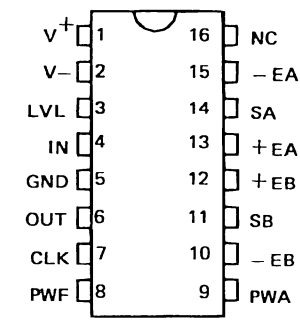
8 pins : FILTER ONLY
DIP-8 Package

E88TSG8540-01



16 pins : FILTER + 2 OP-AMPs
DIP-16 Package

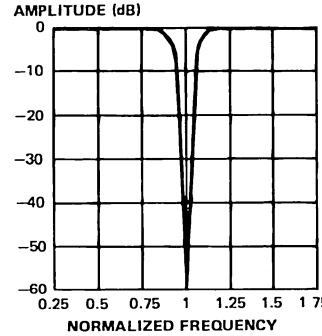
E88TSG8540-02



SO-16 Package

E88TSG8540-03

AMPLITUDE RESPONSE CURVE



E88TSG8540-04

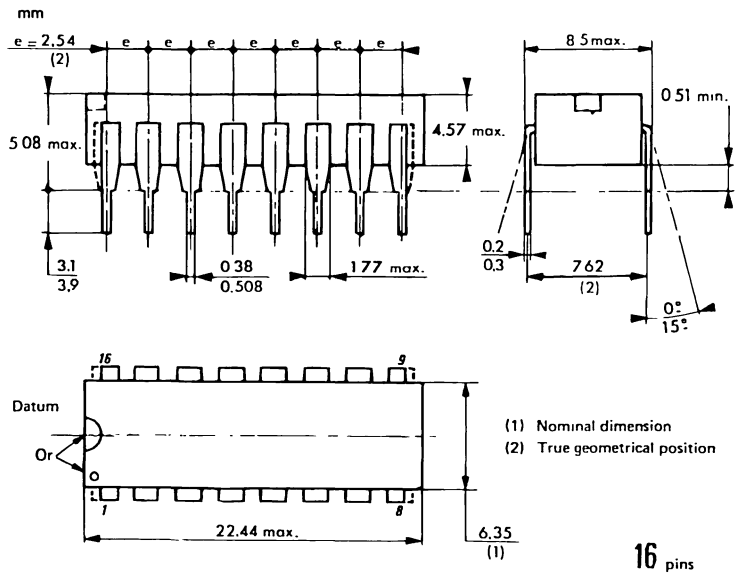
FILTER SPECIFICATIONS

T = 25°C, V_{DD} = + 5V, V_{SS} = – 5V, RL = 5kΩ, CL = 100pF, I_{PWF} = 140µA (unless otherwise specified)

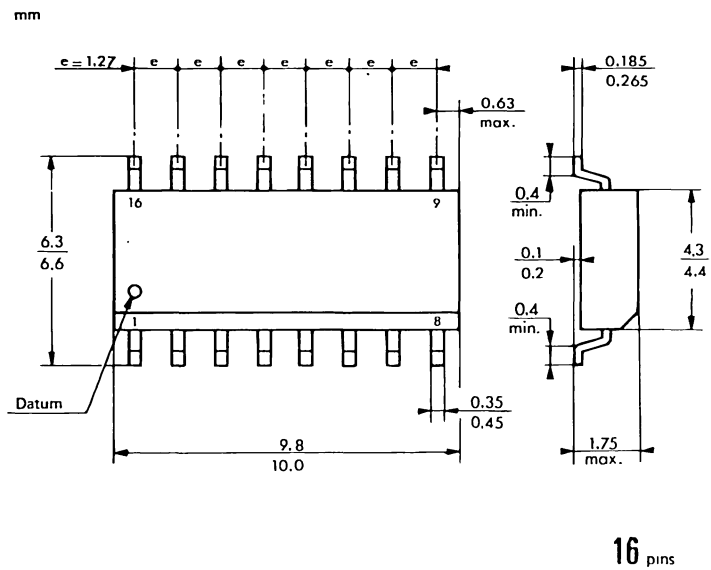
Symbol	Parameter		Value			Unit
			Min.	Typ.	Max.	
f_e	External Clock Frequency		18.6		1116	kHz
f_i	Internal Sampling Freq.	$fo = \sqrt{(flc \cdot fhc)}$	9.3		558	kHz
fe/fo	Clock to Center fr. Ratio			930 ± 2%		
fo	Center Frequency		20		1200	kHz
G_o	Attenuation at Center Frequency	with fe = 370kHz	30	35		dB
flc	Low Cut-off Frequency	Flc = 0.91fo	18.2		1092	Hz
fhc	High Cut-off Frequency with Fe = 372kHz	fhc = 1.1fo	22		1320	Hz
BW	– 3dB Bandwich	1.1/fo – 0.91/fo	3.8		228	Hz
Q	Quality Factor	Q = fo BW		5		
Alp	Low Passband Gain	for f < fo/2	– 1	0	+ 1	dB
Ahp	High Passband Gain	for f > 2fo	– 1.5	0	+ 0.5	dB
V_{off}	Output DC Offset Voltage	LVL = 0V		± 100	± 250	mV
LVL	DC Level Adjustment			± 17	± 42	mV
LG	Level Gain			6		
R_{PWF}	PWF Resistance 72KΩ		9.7		272	kΩ
I_{PWF}	Input Current on PWF		50		260	µA
I + I –	Supply Current	fe = 372kHz I_{PWF} = 140µA I_{PWA} = 0µA		4.6 –4.6	9 – 9	mA
PSSR + PSSR –	Supply Rejection Ratio	fe = 372kHz fin = 500kHz		20 33		dB
R_{in}	Input Resistance			3		MΩ
C_{in}	Input Capacitance			20		pF
V_O	Output Voltage Swing			+ 3.5 – 4.5		VPP
Vn	Output Noise	BW = 93kHz fe = 372kHz V_{IN} = 2Vrms		900		µVrms
SNR	Signal to Noise Ratio			67		dB

PACKAGE MECHANICAL DATA

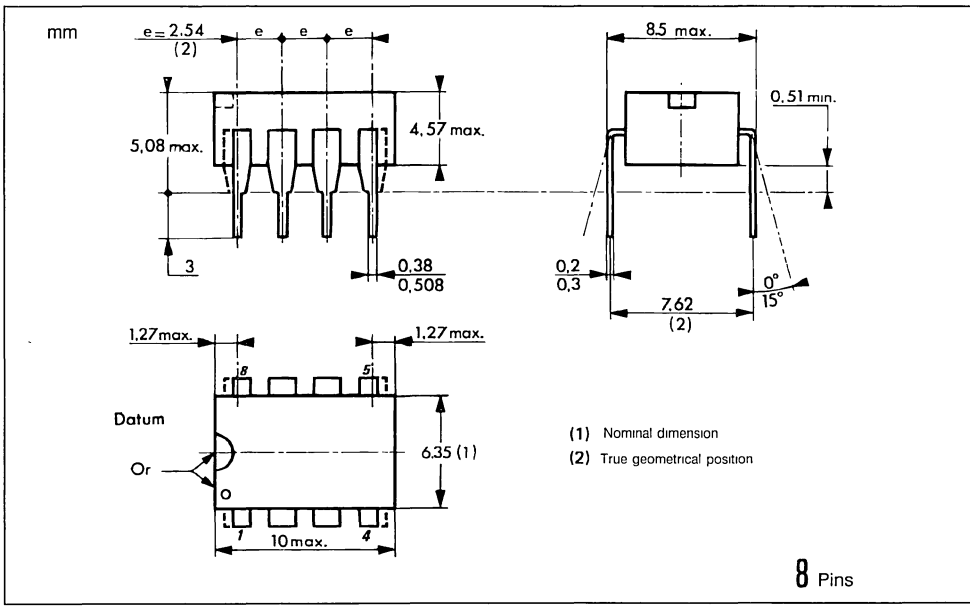
16 PINS - Plastic Dip



16 PINS - Plastic Micropackage



8 PINS - Plastic Dip



ORDER CODES

Plastic	16 Pins Package : TSG8540XP
Ceramic	16 Pins Package : TSG8540XC
Cerdip	16 Pins Package : TSG8540XJ
Plastic	8 Pins Package : TSG8540XP

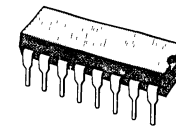
X : Temperature Range =

C :	0°C	+	70°C
I :	– 25°C	+	85°C
V :	– 40°C	+	85°C
T :	– 40°C	+	105°C
M :	– 55°C	+	125°C

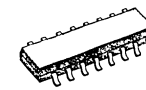
SWITCHED CAPACITOR MASK PROGRAMMABLE FILTER

- 6TH ORDER
- SELECTIVITY FACTOR : Q = 7
- GAIN AT CENTER FREQUENCY : 0dB (typ)
- LOW STOPBAND ATTENUATION : 40dB (typ)
- HIGH STOPBAND ATTENUATION : 40dB (typ)
- CLOCK TO CENTER FREQ. RATIO : 48
- CLOCK FREQUENCY RANGE : 1 TO 1200kHz
- CENTER FREQUENCY RANGE : 20.8Hz TO 25kHz

Note : For general characteristics, see TSG85XX specifications. For non standard quality level, consult SGS-THOMSON general ordering information.



P
DIP-16
(Plastic Package)



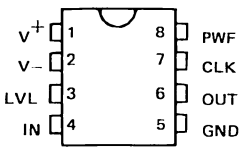
FP
SO-16
(Plastic Micropackage)

P
DIP-8
(Plastic Package)

DESCRIPTION

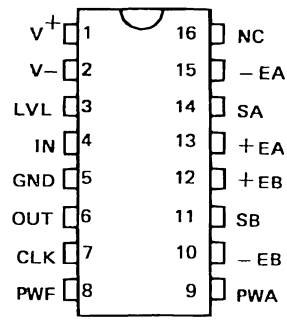
The TSG8550 is a HCMOS Cauer band-pass filter.

PIN CONNECTIONS



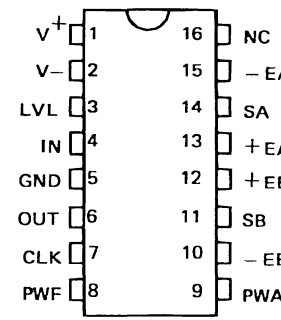
8 pins : FILTER ONLY
DIP-8 Package

E88TSG8550-01



16 pins : FILTER + 2 OP-AMPs
DIP-16 Package

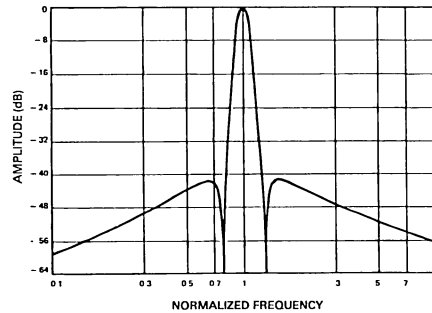
E88TSG8550-02



SO-16 Package

E88TSG8550-03

AMPLITUDE RESPONSE CURVE



E88TSG8550-04

FILTER SPECIFICATIONS

Band-pass Filter : TSG8550 ; Type : CAUER ; Order : 6
$V^+ = 5V$, $V^- = -5V$, $T = 25°C$, $RL = 5k\Omega$, $CL = 100pF$, $I_{PWF} = 50\mu A$

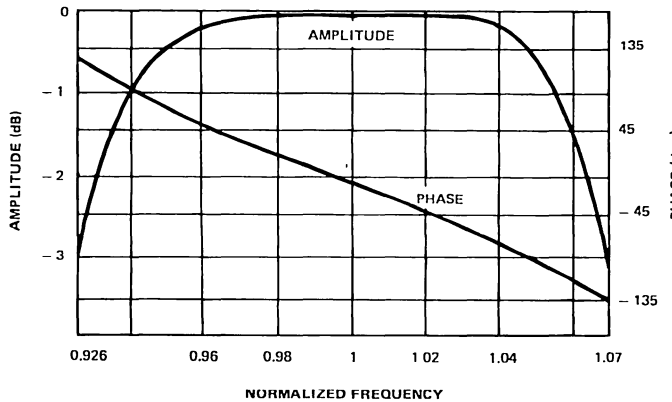
Symbol	Parameter		Typ.	Tested Limits	Unit
Fe	External Clock Frequency		1 1200(*)		kHz (min) kHz (max)
Fi	Internal Sampling Frequency		0.5 600(*)		kHz (min) kHz (max)
Fe/Fo	Clock to Center Frequency Ratio		48 ± 1%		
Fo	Center Frequency		0.0208 25(*)		kHz (min) kHz (max)
Go	Gain at Center Frequency	Typ. Go = – 0.2dB for Fe = 48kHz	0	0 – 2	dB (max) dB (min)
Flc	Low Cutoff Frequency	Flc = 0.971 Fo	0.0204 24.5(*)		kHz (min) kHz (max)
Fhc	High Cutoff Frequency	Fhc = 1.035 Fo	0.0216 25.9(*)		kHz (min) kHz (max)
BW	– 3dB Bandwidth	[0.926 Fo, 1.07 Fo]	0.003 3.15(*)		kHz (min) kHz (max)
Q	Selectivity Coefficient	Q = Fo/BW	7		
Ap	Passband Ripple		0.05	0.3	dB (max)
Als	Low Stopband Attenuation	F < 0.8 Fo	40.5	40	dB (min)
Ahs	High Stopband Attenuation	F > 1.24 Fo	40.5	40	dB (min)
Voff	Output DC Offset Voltage	LVL = 0V	± 100	± 200	mV (max)
LG	Level Gain		– 1.7		
LVL	DC Level Adjustment		± 118		mV (max)
R_{PWF}	PWF Resistance		10 72		kΩ (min) kΩ (max)
I_{PWF}	Input Current on PWF		50 250		µA (min) µA (max)

(*) At maximum Fe · - stopband attenuation Als > 39dB for F < 0 8Fo
(with $I_{pwf} = 250\mu A$) - stopband attenuation Ahs > 42dB for F > 1 24Fo
- passband ripple $A_p = 0$ 3dB
- Gain at center freq $G_0 = -1.5$dB
- – 3dB bandwidth BW = 3 15kHz [0 926Fo, 1.052Fo]
- Selectivity Q = 7 9

FILTER SPECIFICATIONS (continued)

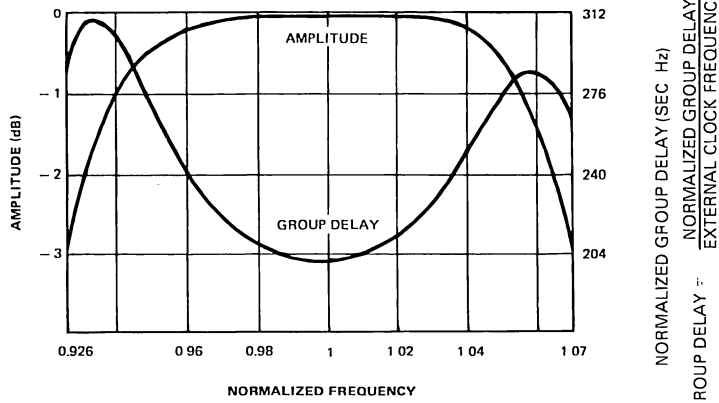
Symbol	Parameter		Typ.	Tested Limits	Unit
I^+	V^+ Supply Current	Fe = 48kHz Ipwa = 0µA	1.7	5	mA (max)
I^-	V^- Supply Current		1.7	5	mA (max)
$PSRR^+$	V^+ Supply Rejection Ratio	Fe = 48kHz Fin = 1kHz	9		dB
$PSRR^-$	V^- Supply Rejection Ratio		20		dB
Rin	Input Resistance		3		MΩ
Cin	Input Capacitance		20		pF
Vo	Output Voltage Swing		+ 3.5 − 4.5		Vp-p (max)
Vn	Output Noise	BW = 144kHz C_{PWF} = 33pF Fe = 48kHz Vin = 2Vrms	272		µVrms
SNR	Signal to Noise Ratio		78		dB

PHASE RESPONSE CURVE (in passband)



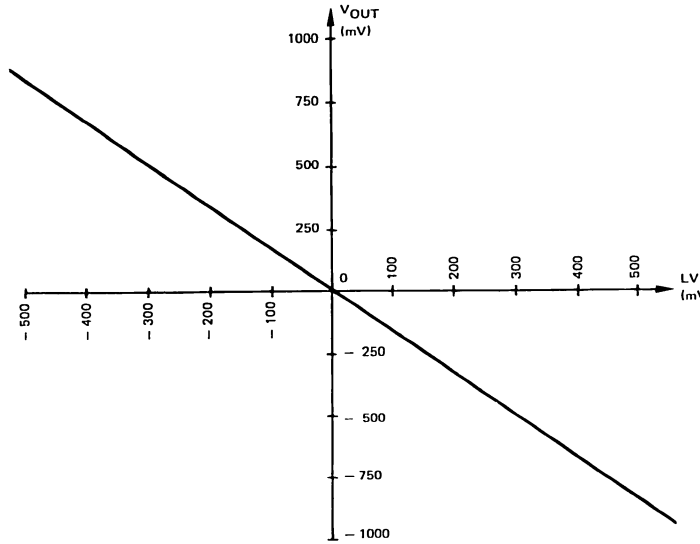
E88TSG8550-05

GROUP DELAY CURVE (in passband)



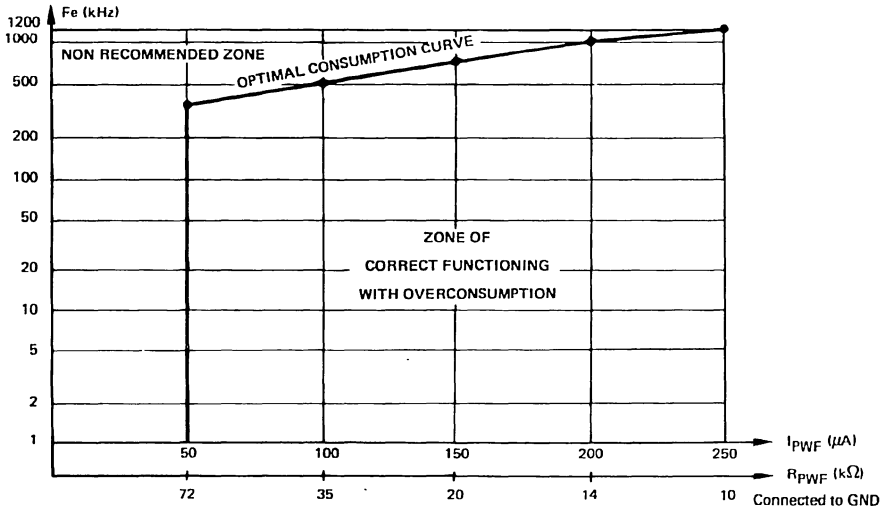
E88TSG8550-06

OUTPUT DC VOLTAGE ADJUSTMENT FROM LVL PIN



E88TSG8550-07

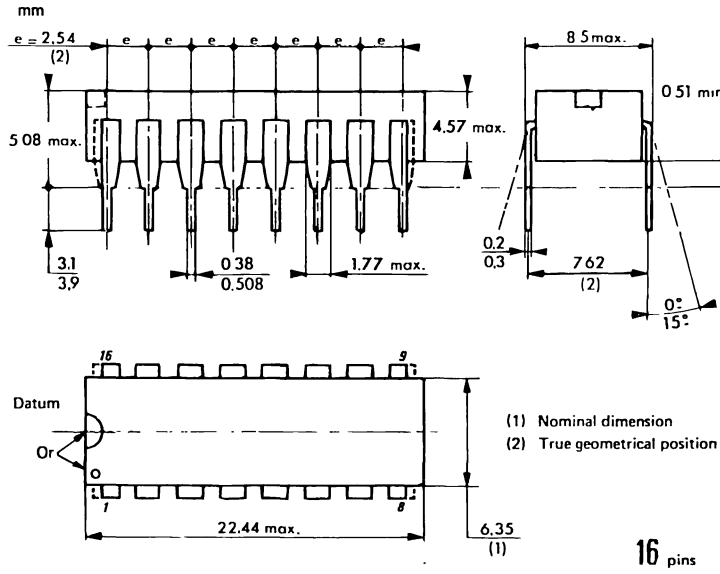
USER'S GUIDE FOR I_{PWF} AND R_{PWF} CHOICE



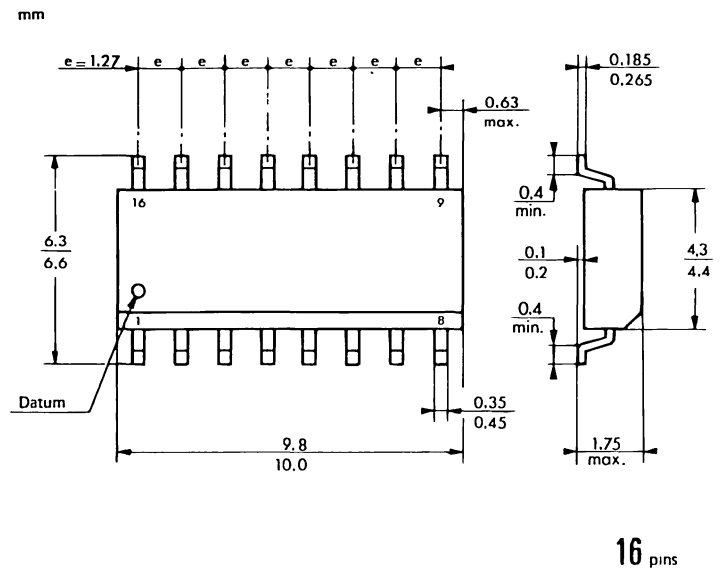
E88TSG8550-08

PACKAGE MECHANICAL DATA

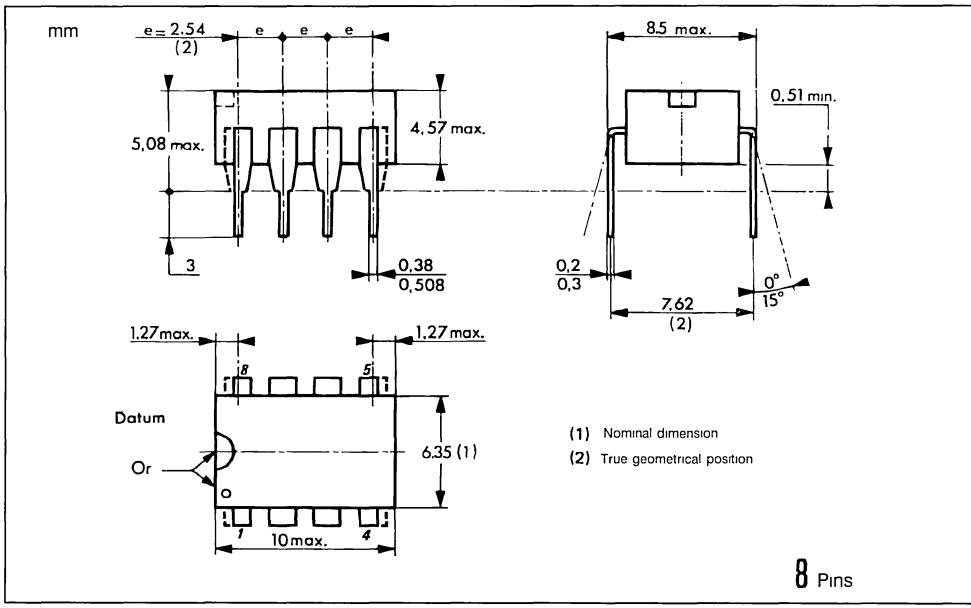
16 PINS - Plastic Dip



16 PINS - Plastic Micropackage



8 PINS - Plastic Dip



ORDER CODES

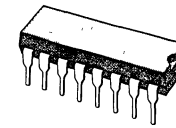
Plastic	16 Pins Package : TSG8550XP
Ceramic	16 Pins Package : TSG8550XC
Cerdip	16 Pins Package : TSG8550XJ
Plastic	8 Pins Package : TSG85501XP

X : Temperature Range = C : 0°C + 70°C
I : − 25°C + 85°C
V : − 40°C + 85°C
M : − 55°C + 125°C

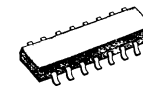
SWITCHED CAPACITOR MASK PROGRAMMABLE FILTER

- 8TH ORDER
- SELECTIVITY FACTOR : Q = 35
- GAIN AT CENTER FREQUENCY : 30dB (typ)
- LOW STOPBAND ATTENUATION : 70dB (typ)
- HIGH STOPBAND ATTENUATION : 70dB (typ)
- CLOCK TO CENTER FREQ. RATIO : 187.2
- CLOCK FREQUENCY RANGE : 4 TO 3800kHz
- CENTER FREQUENCY RANGE : 22Hz TO 20.3kHz

Note : For general characteristics, see TSG85XX specifications. For non standard quality level, consult SGS-THOMSON general ordering information.



P
DIP-16
(Plastic Package)



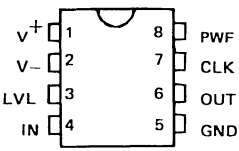
FP
SO-16
(Plastic Micropackage)

P
DIP-8
(Plastic Package)

DESCRIPTION

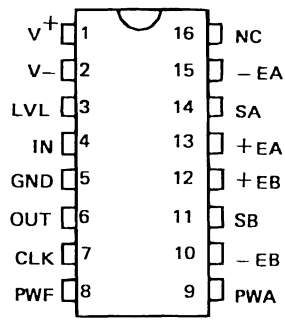
The TSG8551 is a HCMOS high selectivity band-pass filter.

PIN CONNECTIONS



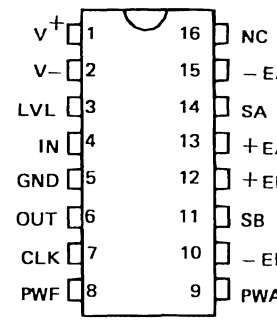
8 pins : FILTER ONLY
DIP-8 Package

E88TSG8551-01



16 pins : FILTER + 2 OP-AMPs
DIP-16 Package

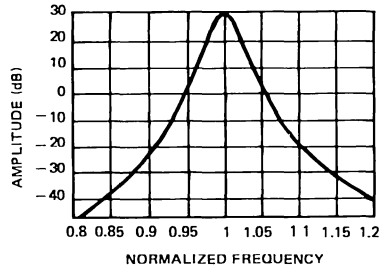
E88TSG8551-02



SO-16 Package

E88TSG8551-03

AMPLITUDE RESPONSE CURVE



E88TSG8551-04

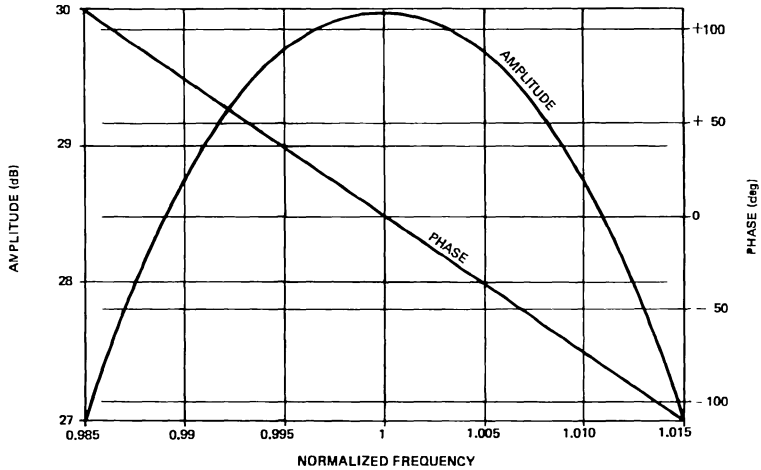
FILTER SPECIFICATIONS

Bandpass Filter : TSG8551 ; Type : High Q ; Order : 8.
$V^+ = 5V$, $V^- = -5V$, T = 25°C, RL = 5kΩ, CL = 100pF, $I_{PWF} = 100\mu A$

Symbol	Parameter		Typ.	Tested Limits	Unit
Fe	External Clock Frequency		4 3800(*)		kHz (min) kHz (max)
Fi	Internal Sampling Frequency		0.5 475(*)		kHz (min) kHz (max)
Fe/Fo	Clock to Center Ratio		187.2 ± 1%		
Fo	Center Frequency		0.022 20.3(*)		kHz (min) kHz (max)
G_o	Gain at Center Frequency	Fe = 400kHz	30	32 28	dB (min) dB (max)
Q	Selectivity Coefficient		35		
Ap	Passband Ripple				dB (max)
Als	Low Stopband Attenuation	F < 0.8 Fo	70	55	dB (min)
Ahs	High Stopband Attenuation	F > 1.2 Fo	70	55	dB (min)
Voff	Output DC Offset Voltage	LVL = 0V	± 100	± 200	mV (max)
LVL	DC Level Adjustment		± 70		mV (max)
LG	Level gain		– 3.3		
R_{PWF}	PWF Resistance		10 72		KΩ (min) KΩ (max)
I_{PWF}	Input Current on PWF		50 250		µA (min) µA (max)
I^+	V^+ Supply Current	Fe = 100kHz Ipwa = 0µA	3.8	5	mA (max)
I^-	V^- Supply Current		3.8	5	mA (max)
$PSRR^+$	V^+ Supply Rejection Ratio	Fe = 187.2kHz Fin = 1kHz	10**		dB
$PSRR^-$	V^- Supply Rejection Ratio		19**		dB
R_{IN}	Input Resistance		3		MΩ
C_{IN}	Input Capacitance		20		pF
Vo	Output Voltage Swing		+ 3.5 – 4.5		Vp-p (max)
Vn	Output Noise	BW = 3Hz Fe = 187.2kHz Vin = 2Vrms	56**		µVrms
SNR	Signal to Noise Ratio		90**		dB

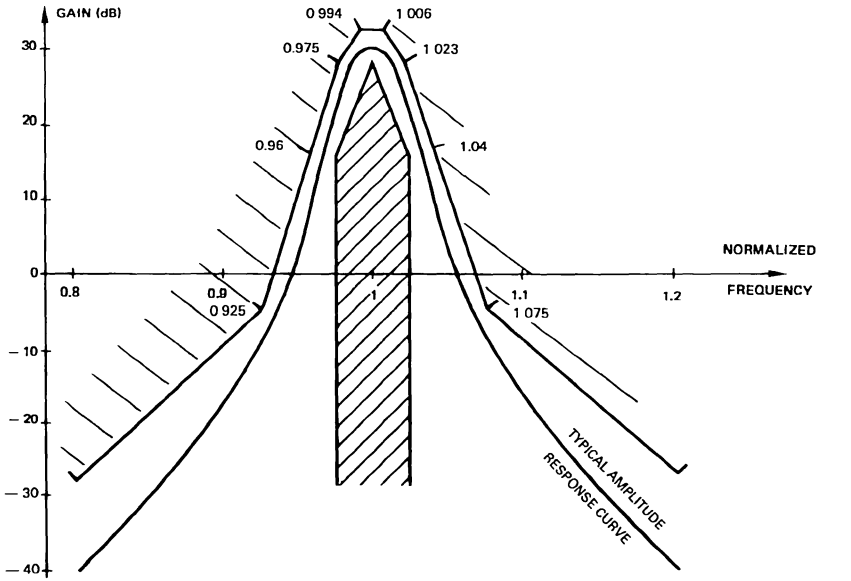
* $I_{PWF} = 200\mu A$
* * Value divided by the gain.

PHASE RESPONSE CURVE (in passband)



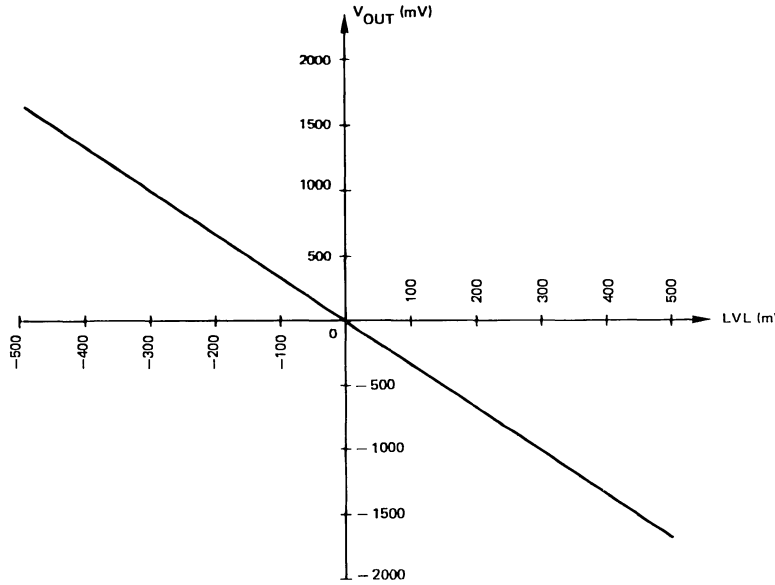
E88TSG8551-05

AMPLITUDE RESPONSE TEMPLATE (tested)



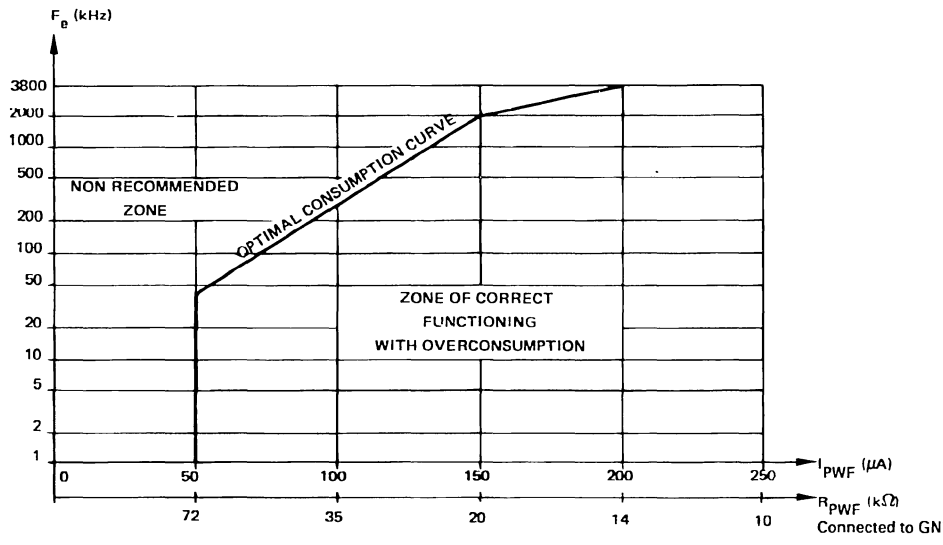
E88TSG8551-06

OUTPUT DC VOLTAGE ADJUSTMENT FROM LVL PIN



E88TSG8551-07

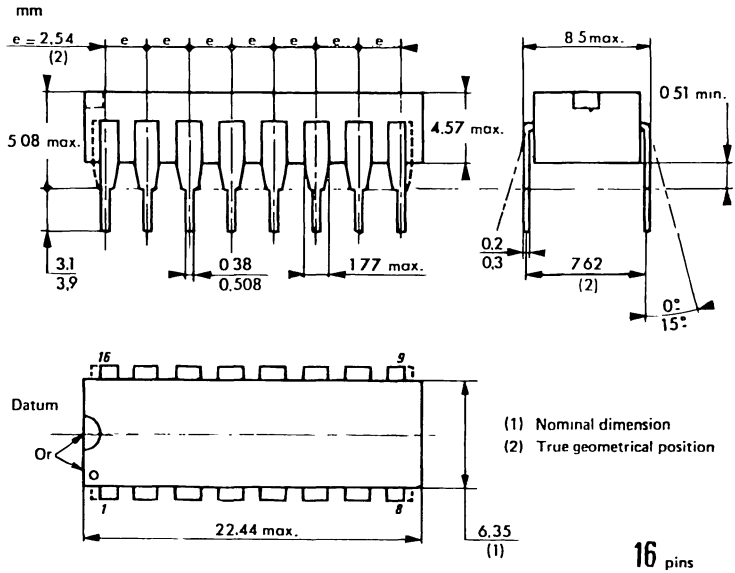
USER'S GUIDE FOR I_{PWF} AND R_{PWF} CHOICE



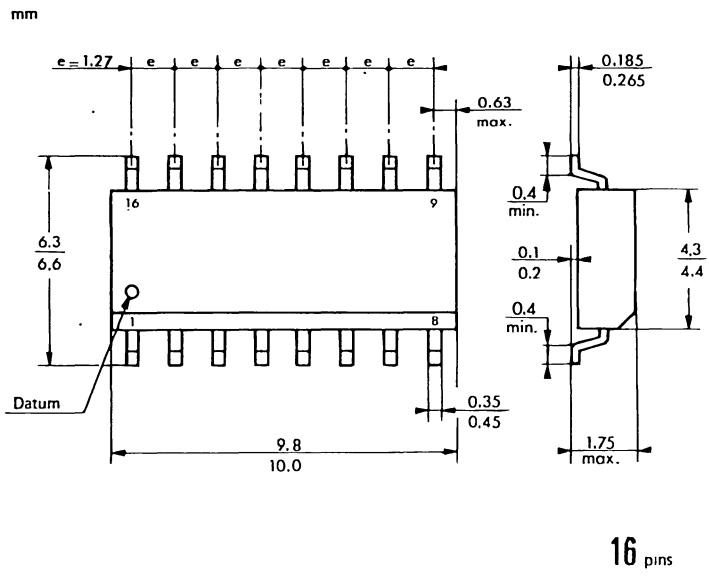
E88TSG8551-08

PACKAGE MECHANICAL DATA

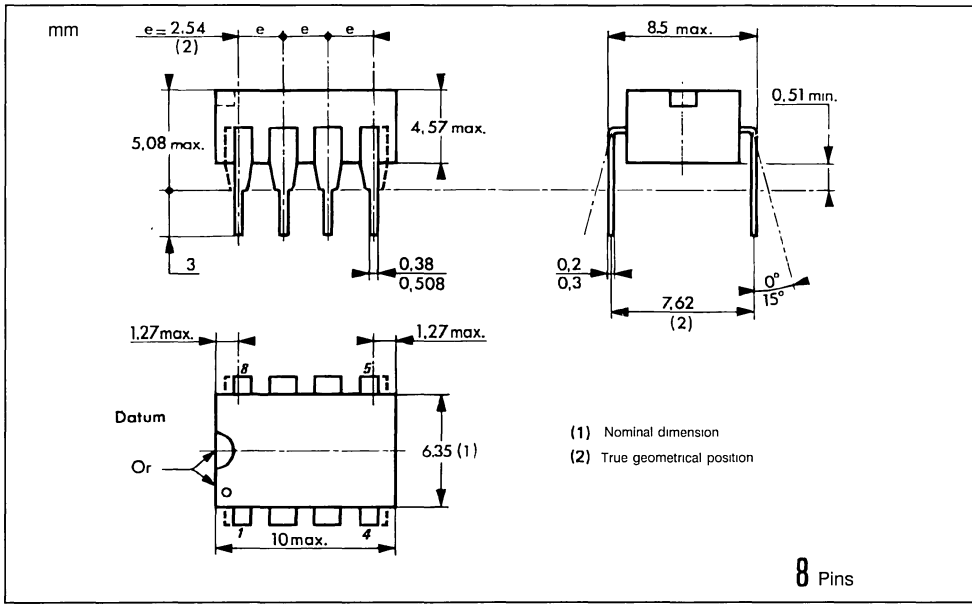
16 PINS - Plastic Dip



16 PINS - Plastic Micropackage



8 PINS - Plastic Dip



ORDER CODES

Plastic	16 Pins Package : TSG8551XP
Ceramic	16 Pins Package : TSG8551XC
Cerdip	16 Pins Package : TSG8551XJ
Plastic	8 Pins Package : TSG85511XP

X : Temperature Range = C : 0°C + 70°C
I : – 25°C + 85°C
V : – 40°C + 85°C
M : – 55°C + 125°C

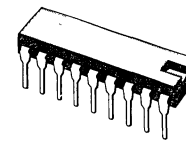
SGS-THOMSON MICROELECTRONICS

TSG8670

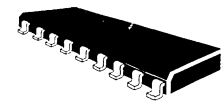
MPF VOICE-GRADE DUAL FILTER FOR TELEPHONE LINE INTERFACE SWITCHED CAPACITOR FILTER

OUT1 : RECEIVE LOW-PASS FILTER
- CAUER TYPE
- 4TH ORDER
- STOPBAND ATTENUATION : 34dB
- PASSBAND RIPPLE : 0.3dB
- CLOCK TO CUTOFF FREQUENCY RATIO : 85.33
- CLOCK FREQUENCY RANGE : 32 TO 1000kHz
- CUTOFF FREQUENCY RANGE : 188Hz TO 12kHz

OUT2 : TRANSMIT BAND-PASS FILTER
- 8TH ORDER (5th order CAUER low-pass + 3rd order CHEBYCHEV high-pass)
- SELECTIVITY FACTOR : Q = 0.52
- UPPER STOPBAND ATTENUATION : 42dB
- PASSBAND RIPPLE : 0.2dB
- CLOCK TO CENTER FREQUENCY RATIO : 148
- CLOCK FREQUENCY RANGE : 32 TO 1000kHz
- CENTER FREQUENCY RANGE : 216Hz TO 6.7kHz



P
DIP-18
(Plastic Package)

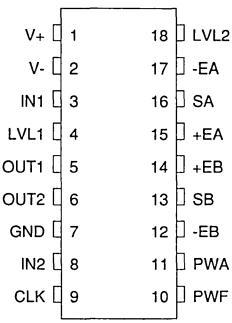


FP
SO-18
(Plastic Micropackage)

DESCRIPTION

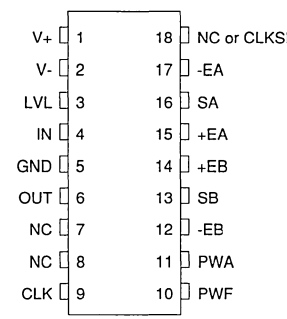
The TSG8670 is a HCMOS voice-grade dual filter for telephone line interface.

PIN CONNECTIONS



DIP-18 Package

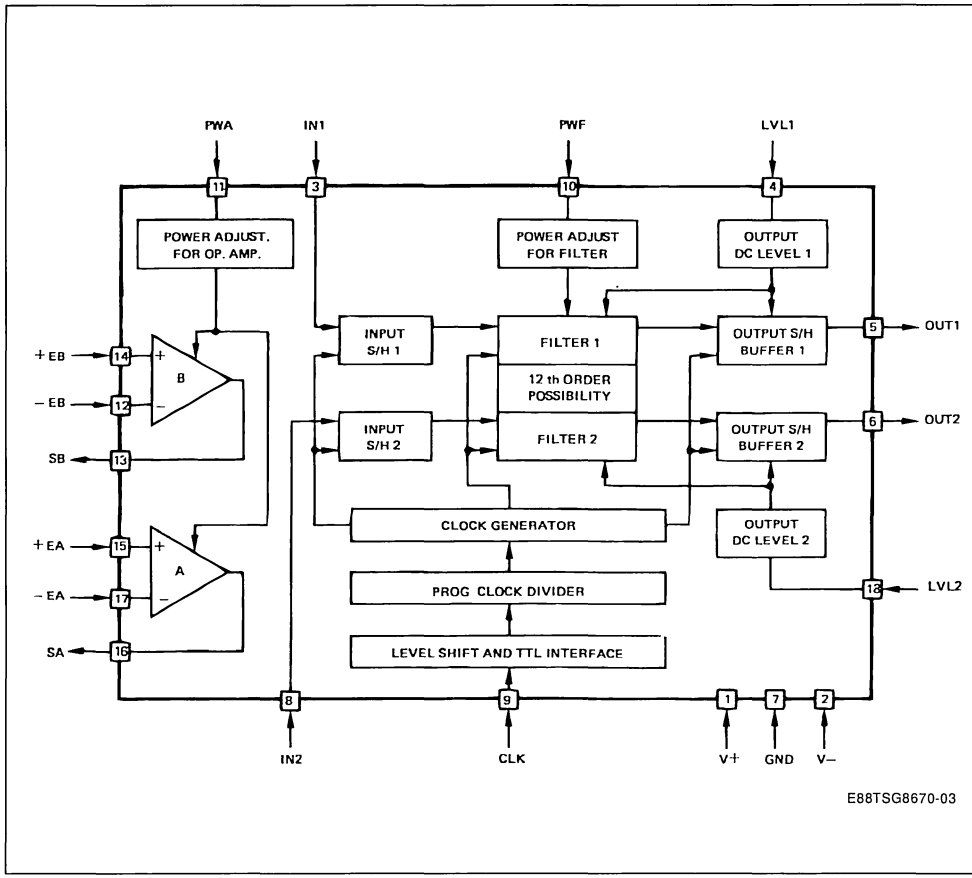
E88TSG8670-01



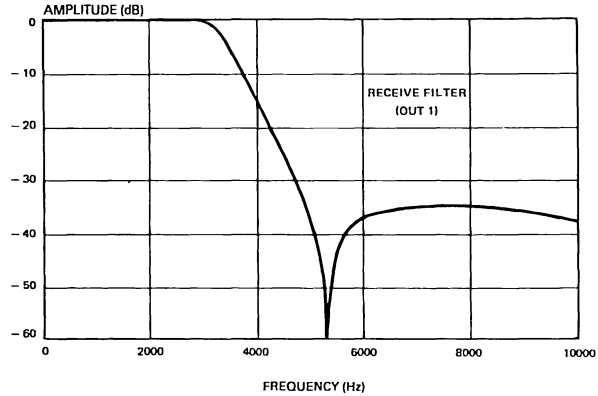
SO-18 Package

E88TSG8670-02

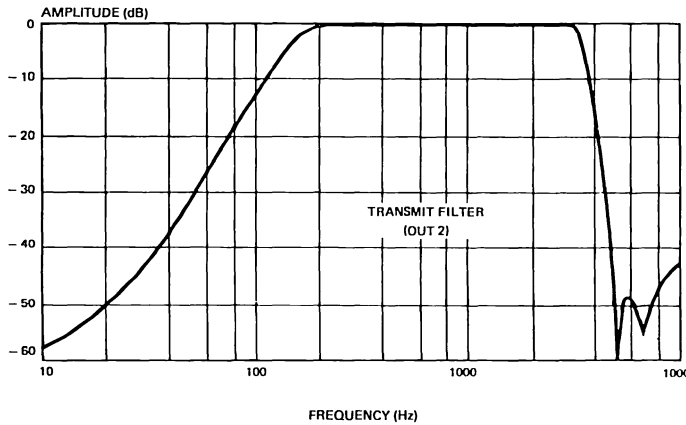
BLOCK DIAGRAM



TYPICAL AMPLITUDE RESPONSE CURVE FOR TELEPHONE APPLICATION (CLK = 256kHz)



E88TSG8670-04



E88TSG8670-05

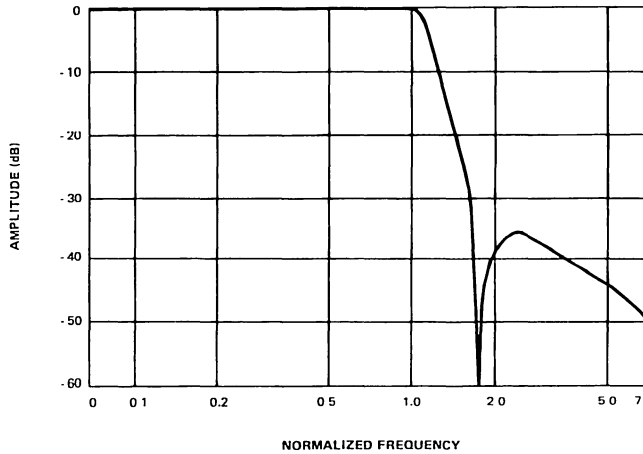
ELECTRICAL OPERATING CHARACTERISTICS

T_{amb} = 25°C, V + = 5V, V – = – 5V, R_L = 5kΩ, CL = 100pF, I_{PWF} = 50µA (unless otherwise specified)

Symbol	Parameter		Value			Unit
			Min.	Typ.	Max.	
f_e	External Clock Frequency		32		1000(*)	kHz
f_i	Internal Sampling Freq.		16		500(*)	kHz
f_e f_c	Clock to Cutoff fr. Ratio		83.6	85.33	87.05	
f_c	Cut Off Frequency		0.188		12(*)	kHz
G_0	Passband Gain	f_e = 256kHz	– 0.2	0.065	+ 0.3	dB
A_P	Passband Ripple	f_e = 256kHz		0.3	0.5	dB
A_S	Stop Band Attenuation	f > 1.63f_c	33	34.8		dB
V_{off}	Output DC Offset Voltage	LVL = 0V I_{PWF} = 50µA		± 80	± 150	mV
LVL	DC Level Adjustment			± 45.5		mV
LG	Level gain			– 3.3		
R_{PWF}	PWF Resistance		20		200	kΩ
I_{PWF}	Input Current on PWF		50		150	µA
I+ I–	Supply Current (**)	f_e = 256kHz I_{PWF} = 50µA I_{PWA} = 0µA		3.6 3.6	5 5	mA
PSRR+ PSRR–	Supply Rejection Ratio	f_e = 256kHz f_{in} = 1kHz		46 42		dB
R_{IN}	Input Resistance			3		MΩ
C_{IN}	Input Capacitance			20		pF
V_O	Output Voltage Swing				+ 3.5 – 4.5	VPP
V_A	Output Noise	BW = 5.9kHz f_e = 256kHz V_{IN} = 2Vrms		190		µVrms
SNR	Signal to Noise Ratio			80		dB

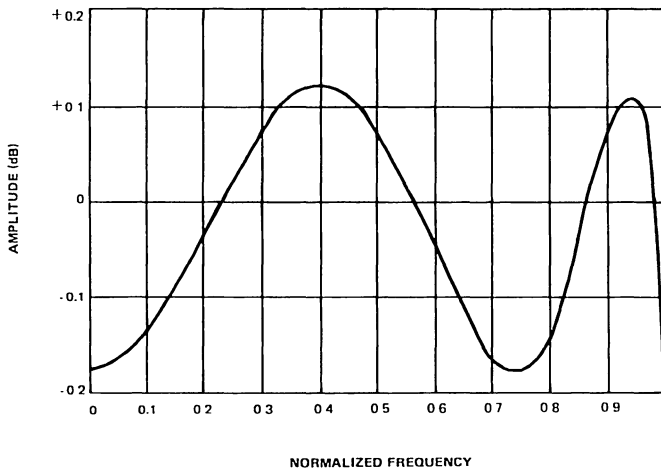
(*) At maximum f_e (with I_{PWF} = 150µA) : f_e/f_o = 85.3 ± 2%.
(**) For both receive and transmit filters.

TYPICAL AMPLITUDE RESPONSE CURVE



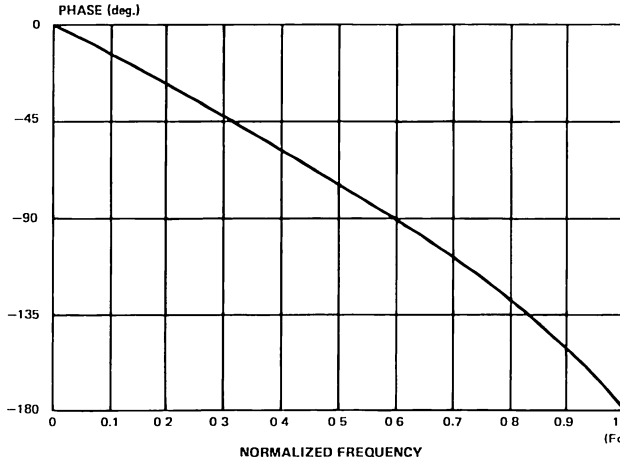
E88TSG8670-06

TYPICAL AMPLITUDE RESPONSE CURVE IN PASSBAND



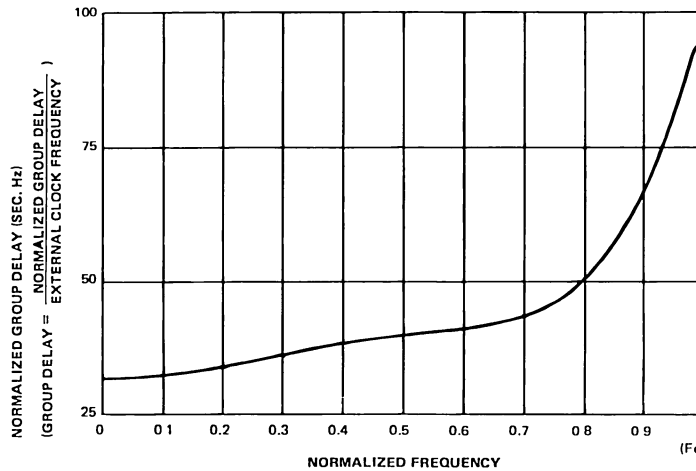
E88TSG8670-07

TYPICAL PHASE RESPONSE CURVE IN PASSBAND



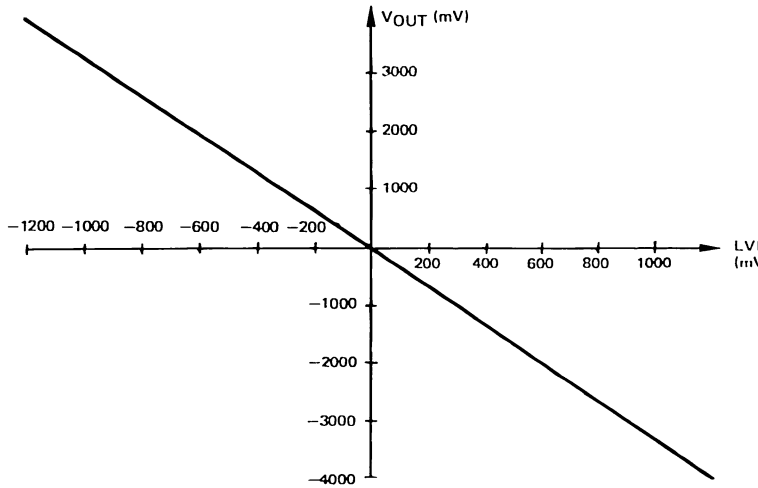
E88TSG8670-08

TYPICAL GROUP DELAY CURVE IN PASSBAND



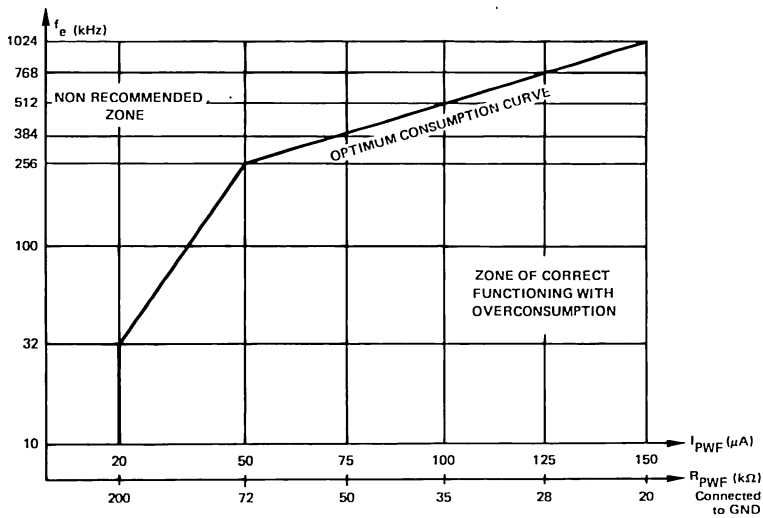
E88TSG8670-09

TYPICAL OUTPUT DC VOLTAGE ADJUSTMENT FROM LVL PIN



E88TSG8670-10

USER'S GUIDE FOR I_{PWF} AND R_{PWF} CHOICE



E88TSG8670-11

2nd FILTER SPECIFICATIONS

Transmit bandpass filter Order : 8

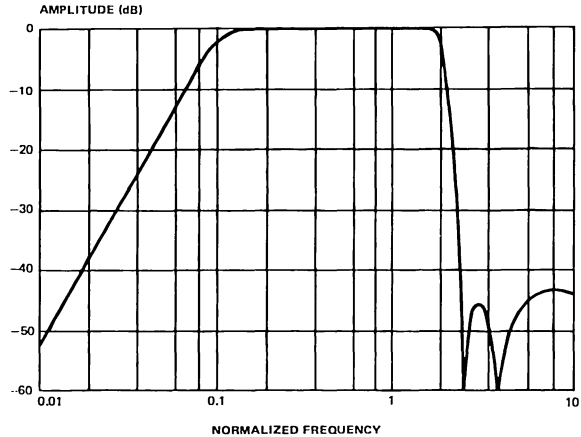
ELECTRICAL OPERATING CHARACTERISTICS

T_{amb} = 25°C, V + = 5V, V − = − 5V, R_L = 5kΩ, CL = 100pF, I_{PWF} = 50µA (unless otherwise specified)

Symbol	Parameter		Value			Unit
			Min.	Typ.	Max.	
f_e	External Clock Frequency		32		1000(*)	kHz
f_I	Internal Sampling Freq.		16		500(*)	kHz
f_e/f_c	Clock to Center fr. Ratio		145	148	151	
f_0	Center Frequency	$f_0 = (f_{lc} + f_{hc})/2$	0.216		6.757(*)	kHz
G_0	Passband Gain	f_e = 256kHz	− 0.4	− 0.2	+ 0	dB
f_{lc}	Low Cut-off Frequency	$F_{lc} = 0.148\ f_0$	0.032		1(*)	kHz
f_{hc}	High Cut-off Frequency	$f_{hc} = 1.852 f_0$	0.4		12.5(*)	kHz
BW	− 3dB Bandwidth	$[0.0925 f_0, 2.023 f_0]$	0.417		13(*)	kHz
Q	Quality Factor	$Q = f_0/BW$		0.52		
A_P	Passband Ripple	f_e = 256kHz		0.15	0.3	dB
Als	Low Stopband Attenuation	$f < 0.0145\ f_0$	41	42		dB
Ahs	High Stopband Attenuation	$f > 2.83\ f_0$	41	42		dB
V_{off}	Output DC Offset Voltage	LVL = 0V I_{PWF} = 50µA		± 50	± 300	mV
LVL	DC Level Adjustment			± 48		mV
LG	Level Gain			− 6.2		
R_{PWF}	PWF Resistance		20		200	kΩ
I_{PWF}	Input Current on PWF		20		150	µA
I + I −	Supply Current (**)	f_e = 256kHz I_{PWF} = 50µA I_{PWA} = 0µA		3.6 3.6	5 5	mA
PSRR + PSRR −	Supply Rejection Ratio	f_e = 256kHz f_{in} = 1.73kHz		32 42		dB
R_{IN}	Input Resistance			3		MΩ
C_{IN}	Input Capacitance			20		pF
V_O	Output Voltage Swing				+ 3.5 − 4.5	VPP
V_A	Output Noise	BW = 3.34kHz f_e = 256kHz V_{IN} = 2Vrms		277		µVrms
SNR	Signal to Noise Ratio			77		dB

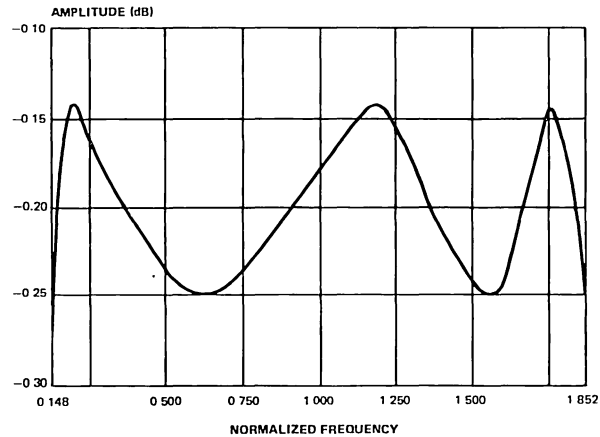
(*) At maximum f_e (with I_{PWF} = 150µA) f_e/f_o = 148 ± 2% and − 0.7dB < G_O < − 0.3dB.
(**) For both receive and transmit filters.

TYPICAL AMPLITUDE RESPONSE CURVE



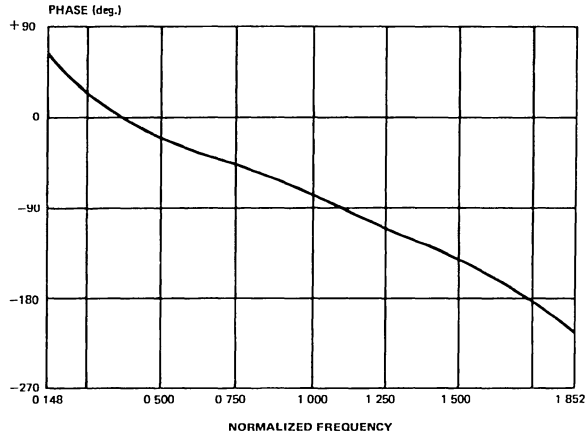
E88TSG8670-12

TYPICAL AMPLITUDE RESPONSE CURVE IN PASSBAND



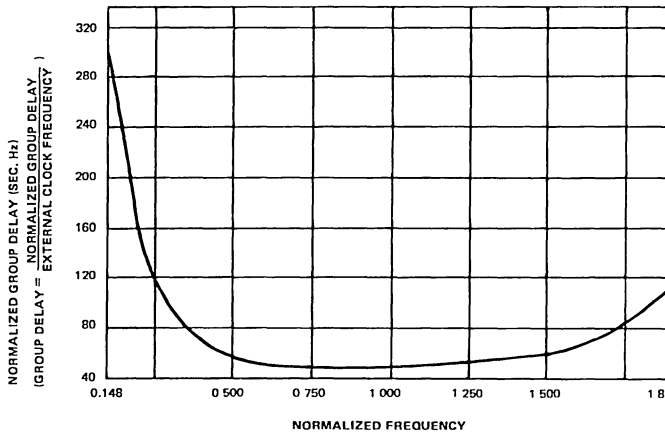
E88TSG8670-13

TYPICAL PHASE RESPONSE CURVE IN PASSBAND



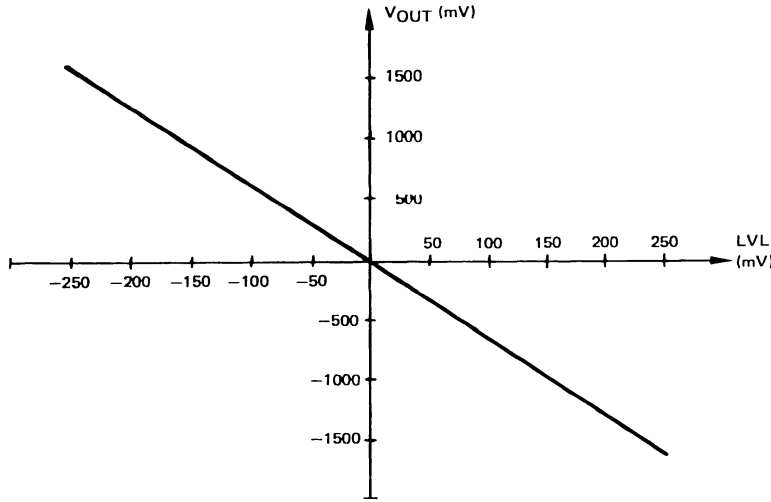
E88TSG8670-14

TYPICAL GROUP DELAY CURVE IN PASSBAND



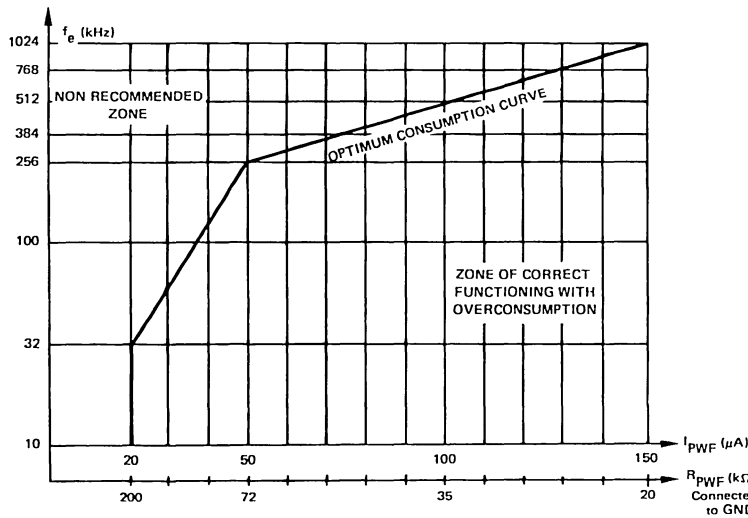
E88TSG8670-15

TYPICAL OUTPUT DC VOLTAGE ADJUSTMENT FROM LVL PIN



E88TSG8670-16

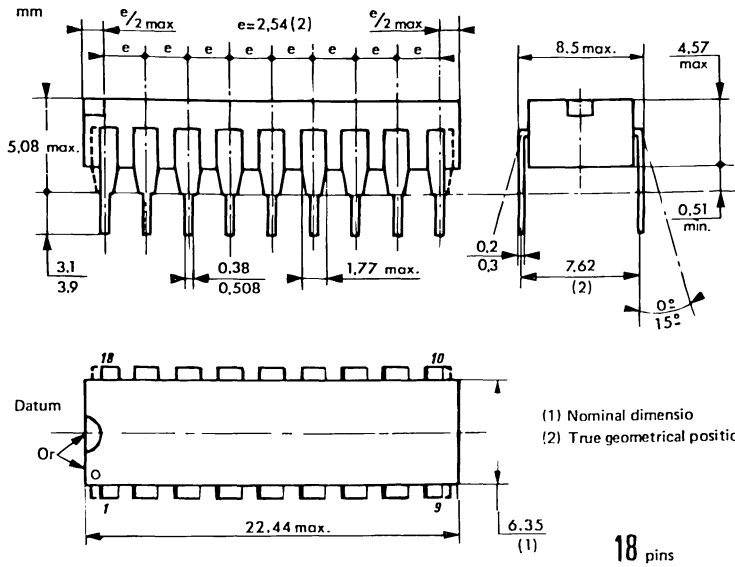
USER'S GUIDE FOR IPWF AND RPWF CHOICE



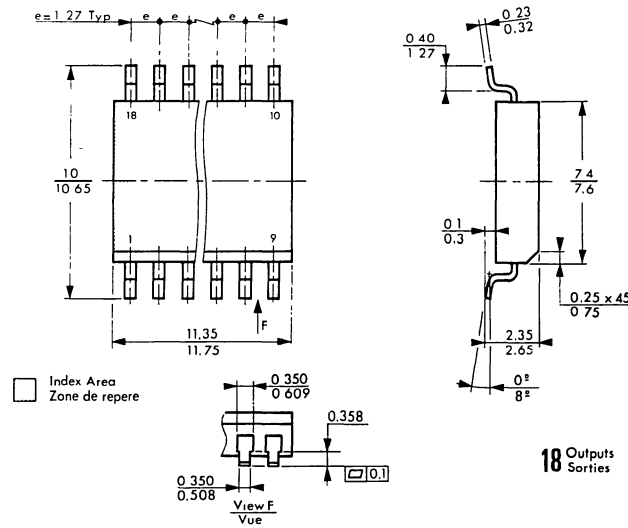
E88TSG8670-17

PACKAGE MECHANICAL DATA

18 PINS - Plastic Dip



18 PINS - Plastic Micropackage



ORDER CODES

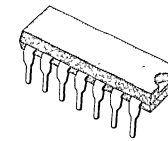
Plastic	18 Pins Package : TSG8670XP
Ceramic	18 Pins Package : TSG8670XC
Cerdip	18 Pins Package : TSG8670XJ

X : Temperature Range = C : 0°C + 70°C
I : – 25°C + 85°C
V : – 40°C + 85°C
M : – 55°C + 125°C

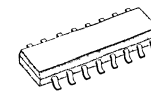
SWITCHED CAPACITOR FILTER

- 4TH ORDER
- SELECTIVITY FACTOR Q = 25
- GAIN AT CENTER FREQUENCY G_O : 20dB (typ.)
- LOW STOPBAND ATTENUATION : G_O : – 65dB (typ.) AT f < 0.3 f_O
- HIGH STOPBAND ATTENUATION : G_O : – 65dB (typ.) AT f > 3 f_O
- CLOCK TO CENTER FREQ. RATIO : 60
- CLOCK FREQUENCY RANGE : 1.5 TO 720kHz
- CENTER FREQUENCY RANGE : 25Hz TO 12kHz

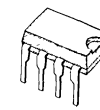
Note : For general characteristics, see TSGF04 specifications. For non standard quality level, consult SGS-THOMSON general ordering information.



P
DIP-14
(Plastic Package)



FP
SO-18
(Plastic Micropackage)

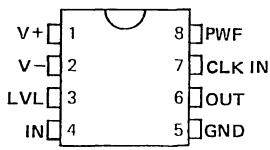


P
DIP-8
(Plastic Package)

DESCRIPTION

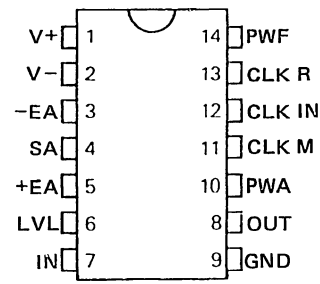
The TSG8751 is a HCMOS high selectivity band-pass filter.

PIN CONNECTIONS



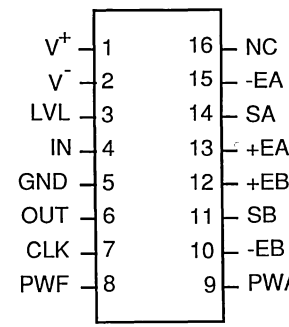
8 pins : FILTER ONLY
DIP-8 Package

E88TSG8751-01



14 pins : FILTER + 1 OP-AMP
DIP-14 Package

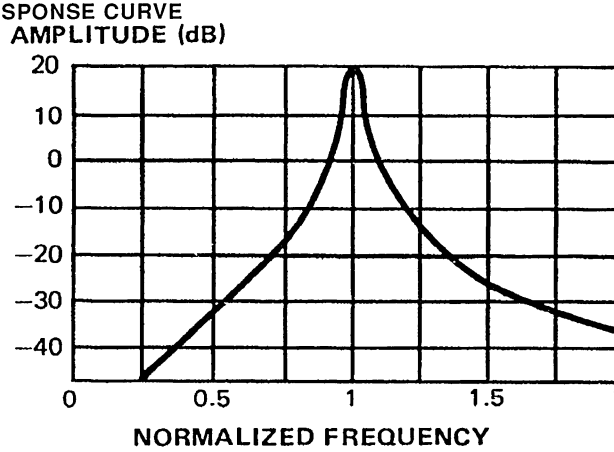
E88TSG8751-02



SO-16 Package

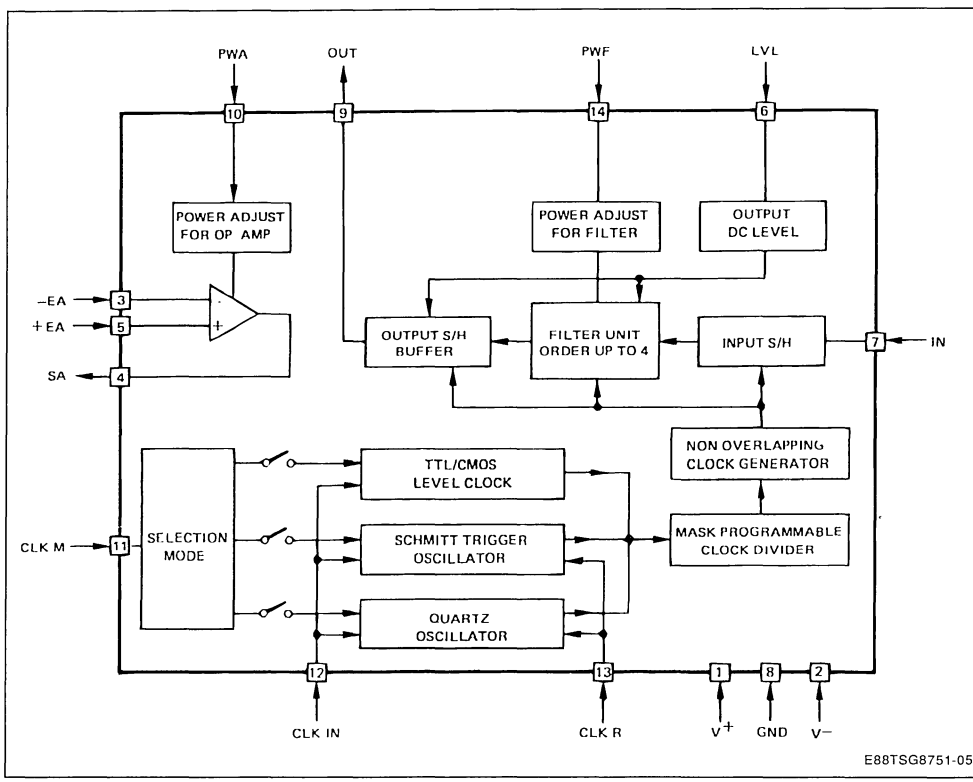
E88TSG8751-03

AMPLITUDE RESPONSE CURVE



E88TSG8751-04

BLOCK DIAGRAM



E88TSG8751-05

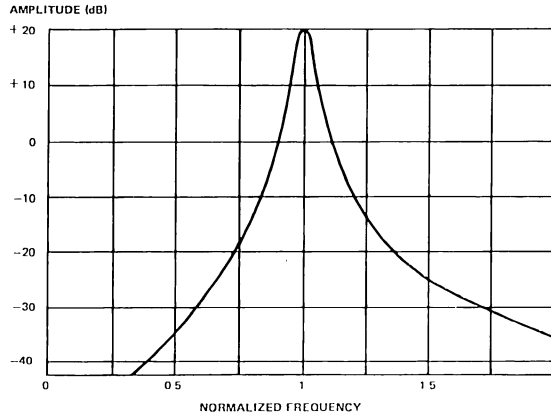
FILTER SPECIFICATIONS

ELECTRICAL OPERATING CHARACTERISTICS
T_{amb} = 25°C, V + = 5V, V – = – 5V, R_L = 5kΩ, CL = 100pF, I_{PWF} = 50μA (unless otherwise specified)

Symbol	Parameter		Value			Unit
			Min.	Typ.	Max.	
f_e	External Clock Frequency		1.5		720(*)	kHz
f_i	Internal Sampling Freq.		0.75		360(*)	kHz
f_e f_0	Clock to Center fr. Ratio		58 8	60	61.2	
f_0	Center Frequency	$f_0 = (f_{lc} + f_{hc})$ 2	0.025		12(*)	kHz
G_0	Gain at Center Frequency	f_e = 60kHz I_{PWF} = 50μA	19	20	21	dB
f_{lc}	Low Cut Off Frequency	$F_{lc} = 0.98\ f_0$	0.0245		11.76	kHz
f_{hc}	High Cut Off Frequency	$f_{hc} = 1.02\ f_0$	0.0255		12.24	kHz
BW	– 3dB Bandwich	[0.98 f_0, 1.02 f_0]	1		480	Hz
Q	Quality Factor	$Q = f_0$ BW		25		
Als	Low Stopband Attenuation	$f < 0.3\ f_0$	$G_0 - 63$	$G_0 - 65$		dB
Ahs	High Stopband Attenuation	$f > 3\ f_0$	$G_0 - 63$	$G_0 - 65$		dB
V_{off}	Output DC Offset Voltage	LVL = 0V I_{PWF} = 50μA		± 100	± 200	mV
LVL	DC Level Adjustment			± 67		mV
LG	Level Gain			3		
R_{PWF}	PWF Resistance		20		72	kΩ
I_{PWF}	Input Current on PWF		50		150	μA
I + I –	Supply Current	f_e = 60kHz I_{PWF} = 50μA I_{PWA} = 0μA		1.6 1.6	3 3	mA
PSRR + PSRR –	Supply Rejection Ratio	f_e = 60kHz f_{in} = 1kHz		30(**) 31(**)		dB
R_{IN}	Input Resistance			3		MΩ
C_{IN}	Input Capacitance			20		pF
Vo	Output Voltage Swing			+ 3.5 – 4.5		VPP
V_A	Output Noise	BW = 1kHz f_e = 60kHz V_{IN} = 2Vrms		91.8(**)		μVrms
SNR	Signal to Noise Ratio			66		dB

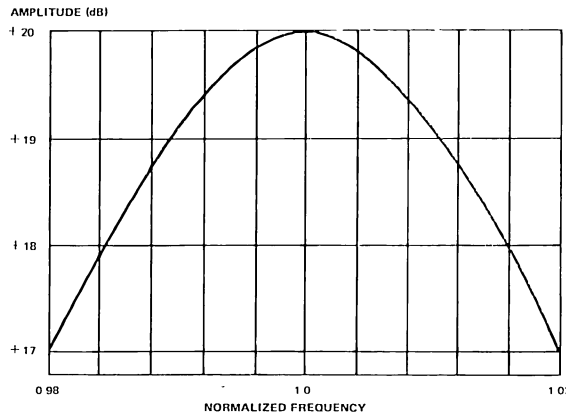
(*) At maximum f_e (with I_{PWF} = 150μA) · f_e/f_o = 61 ± 2%
(**) Value divided by the gain

TYPICAL AMPLITUDE RESPONSE CURVE



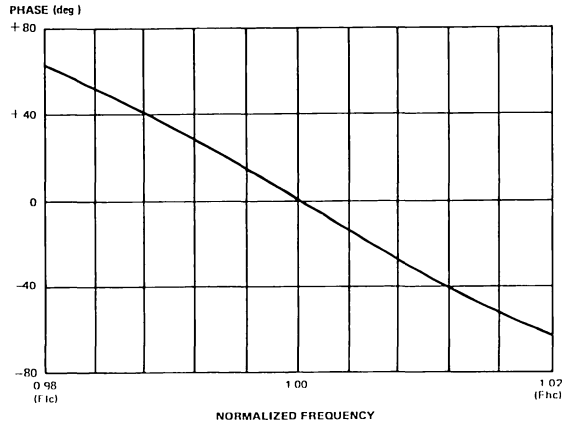
E88TSG8751-06

TYPICAL AMPLITUDE RESPONSE CURVE IN PASSBAND



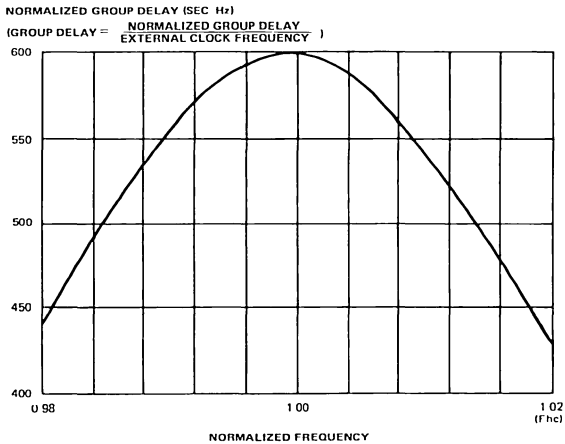
E88TSG8751-07

TYPICAL PHASE RESPONSE CURVE IN PASSBAND



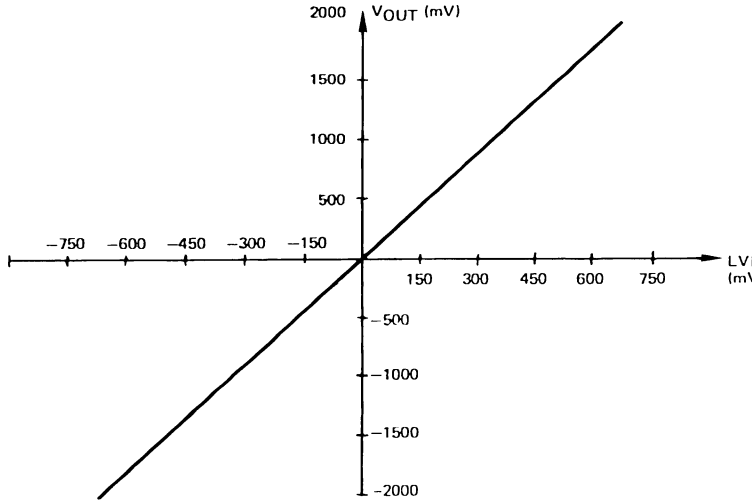
E88TSG8751-08

TYPICAL GROUP DELAY CURVE IN PASSBAND



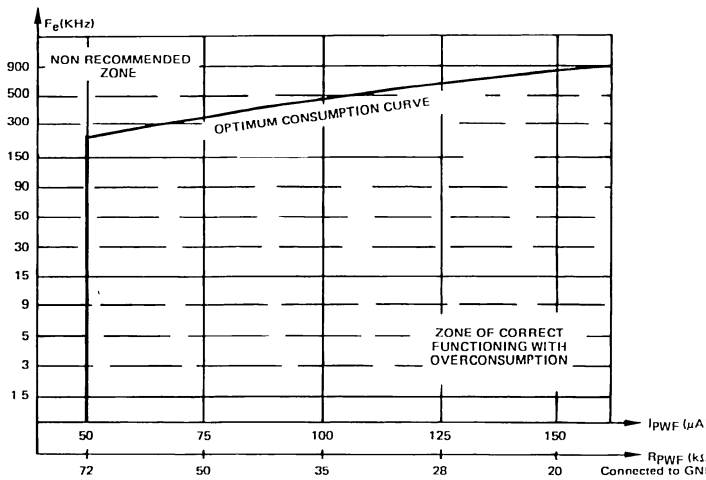
E88TSG8751-09

TYPICAL OUTPUT DC VOLTAGE ADJUSTMENT FROM LVL PIN



E88TSG8751-10

USER'S GUIDE FOR I_{PWF} AND R_{PWF} CHOICE



E88TSG8751-11

CLOCK OSCILLATOR

The TSGF04 base accepts external compatible TTL/CMOS clocks on CLKIN pin and provides an internal oscillator performed either by RC or crystal connected between CLKIN and CLKR pins.

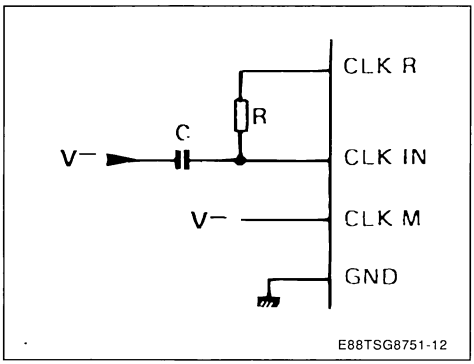
The clock selection mode is provided by CLKM pad which can be connected to V- or GND voltage levels. This connection is realized by two means, depending on the package type chosen :

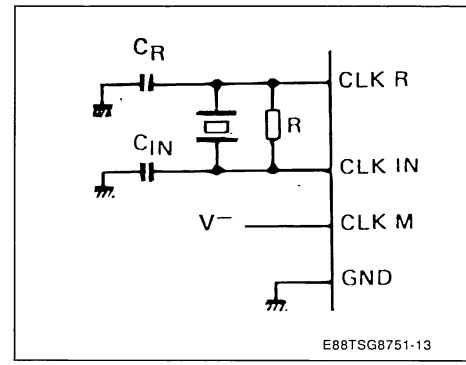
- with 14-pin package, via pin CLKM
- with 8-pin package, by internal connection readily performed, only on custom filters.

(note that CLKM pin connected to V+, allows the selection of the internal crystal-controlled oscillator, but the selection by CLKM connected to V- is recommended).

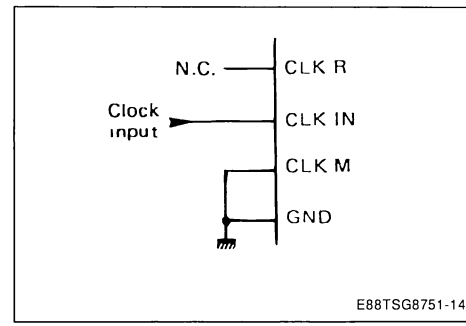
The different possibilities are :

- two internal oscillator modes :
  - RC
  - Crystal

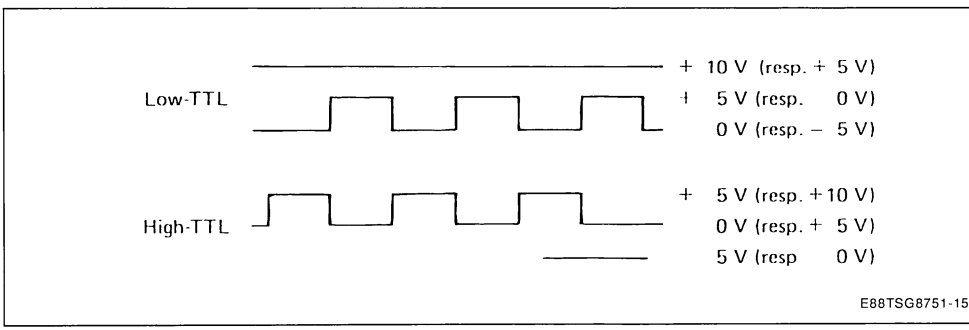




- three external clocks :
  - low-TTL
  - high-TTL
  - CMOS



The "low-TTL" and "high-TTL" clock levels are :



For each package version, the following tables resume, the availability of the different clocks, in terms of the power supply.

Note that in 8-pin version, the clock mode (CLKM) is internally set to GND voltage, except in the case of CMOS clock and 0-5V power supply, where CLKM is internally connected to V- voltage.

8-Pin Package			
	0.5V	0.10V	– 5. + 5V
Low-TTL	NO	C	C
High-TTL	NO	YES	YES
CMOS	C	YES	YES
RC Mode	NO	NO	NO
Crystal Mode	NO	NO	NO

C = Customization option

14-Pin Package			
	0.5V	0.10V	– 5. + 5V
Low-TTL	NO	C	C
High-TTL	NO	CLKM = GND	CLKM = GND
CMOS	CLKM = V^-	CLKM = GND	CLKM = GND
RC Mode	CLKM = V^-	CLKM = V^-	CLKM = V^-
Crystal Mode	CLKM = V^-	CLKM = V^-	CLKM = V^-

ELECTRICAL OPERATING CHARACTERISTICS

WITH DUAL SUPPLY VOLTAGE
T_{amb} = 25°C, V+ = 5V, V– = – 5V, GND = 0V, (unless otherwise specified)

Symbol	Parameter	Value			Unit
		Min.	Typ.	Max.	
GND	Threshold Voltage		1.5		V
	External Clock Frequency			5	MHz
V –	RC MODE :				
	High Threshold Voltage on CLKIN	1	1.25	1.5	V
	Corresponding Voltage on CLKR		– 5		V
	Low Threshold Voltage on CLKIN	– 1.5	– 1.25	– 1	V
	Corresponding Voltage on CLKR		+ 5		V
	Oscillator Frequency			5	MHz
	Resistor	2		10 000	kΩ
	Capacitor	0		47	nF
V –	CRYSTAL MODE :				
	Oscillator Frequency			5	MHz
	Resistor		1		MΩ
	Capacitor C_R	10		100	pF
	Capacitor C_{IN}	10		30	pF

ELECTRICAL OPERATING CHARACTERISTICS (continued)

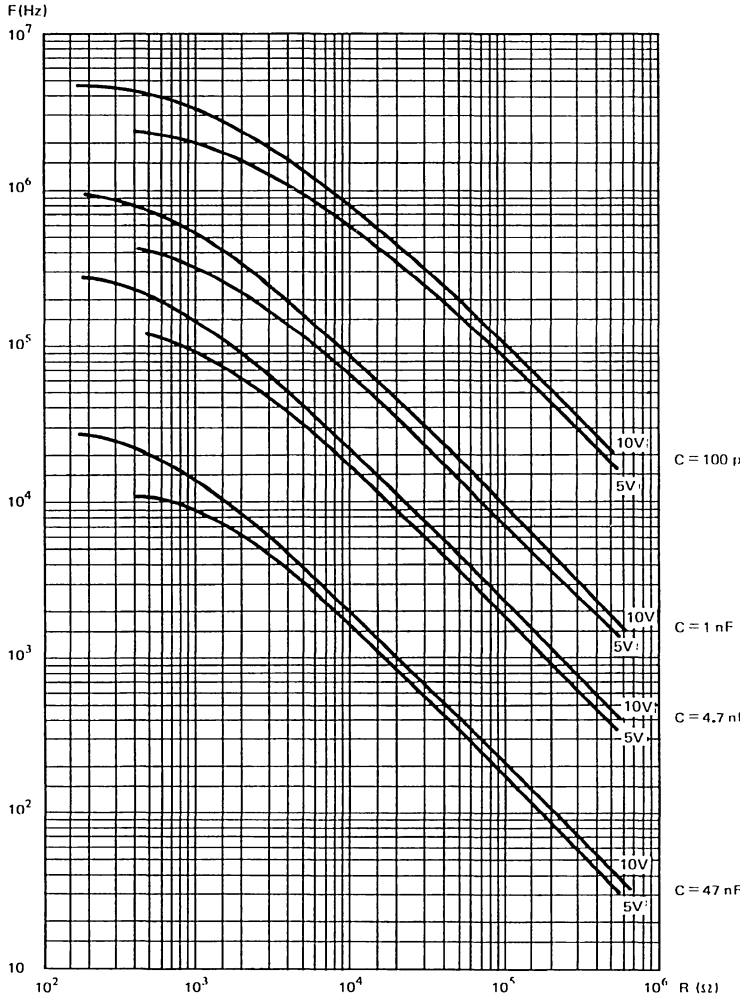
WITH SINGLE SUPPLY VOLTAGE
T_{amb} = 25°C, V+ = 10V, V– = 0V, GND = 5V, (unless otherwise specified)

CLKM	Parameter	Value			Unit
		Min.	Typ.	Max.	
GND	Threshold Voltage		6.5		V
	External Clock Frequency			5	MHz
V –	RC MODE :				
	High Threshold Voltage on CLKIN	6	6.25	6.5	V
	Corresponding Voltage on CLKR		0		V
	Low Threshold Voltage on CLKIN	3.5	3.75	4	V
	Corresponding Voltage on CLKR		+ 10		V
	Oscillator Frequency			5	MHz
	Resistor	2		10 000	kΩ
	Capacitor	0		47	nF
V –	CRYSTAL MODE :				30
	Oscillator Frequency			5	
	Resistor		1		MHz
	Capacitor C_R	10			MΩ
	Capacitor C_{IN}	10		100	pF

WITH SINGLE SUPPLY VOLTAGE
T_{amb} = 25°C, V+ = 5V, V– = 0V, GND = 2.5V, (unless otherwise specified)

CLKM	Parameter	Value			Unit
		Min.	Typ.	Max.	
GND	Threshold Voltage		3.8		V
	External Clock Frequency			5	MHz
V –	RC MODE :				
	High Threshold Voltage on CLKIN	3	3.2	3.4	V
	Corresponding Voltage on CLKR		0		V
	Low Threshold Voltage on CLKIN	1.5	1.8	2	V
	Corresponding Voltage on CLKR		+ 5		V
	Oscillator Frequency			5	MHz
	Resistor	2		10 000	kΩ
	Capacitor	0		47	nF
V –	CRYSTAL MODE :				
	Oscillator Frequency			5	
	Resistor		1		MHz
	Capacitor C_R	10		100	MΩ
	Capacitor C_{IN}	10		30	pF

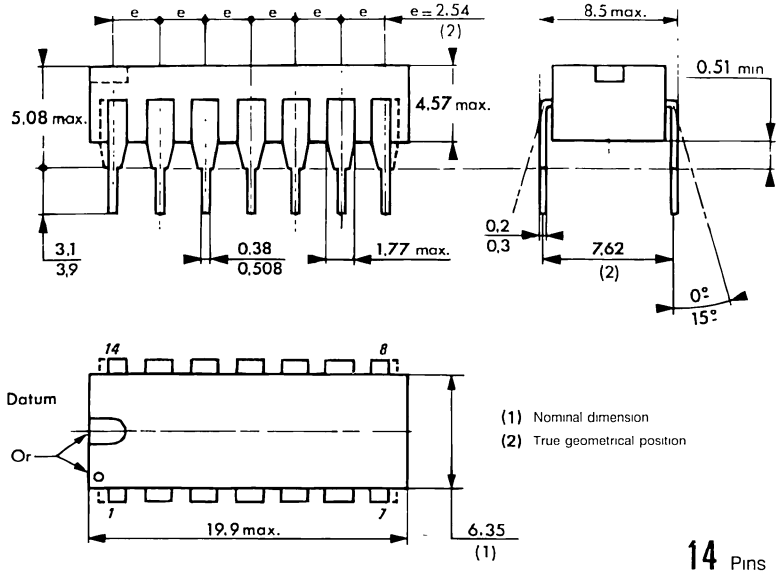
With internal RC oscillator mode, the user's guide for R and C choice is given by following curves and for both supply voltages : 0-5V, 0-10V.



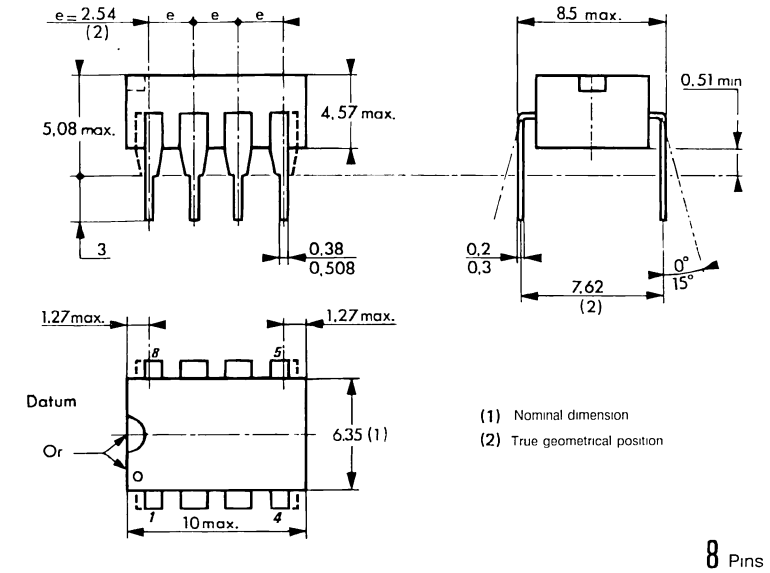
E88TSG8751-16

PACKAGE MECHANICAL DATA

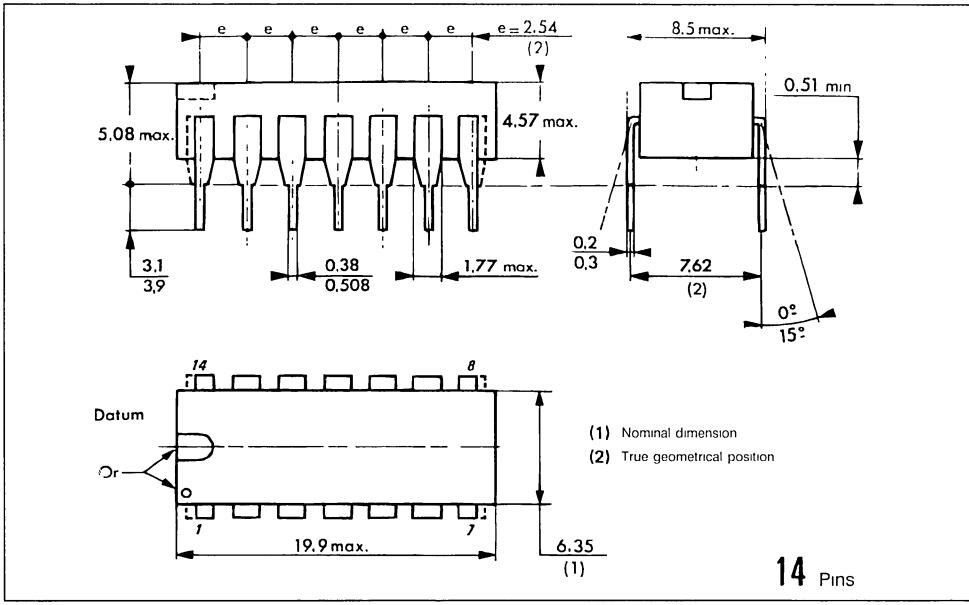
14 PINS - Plastic Dip



8 PINS - Plastic Package



16 PINS - Plastic Micropackage



ORDER CODES

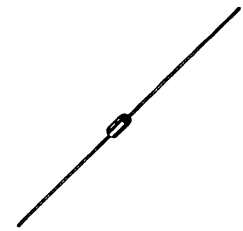
Plastic	14 Pins Package : TSG8751XP
Ceramic	14 Pins Package : TSG8751XC
Cerdip	14 Pins Package : TSG8751XJ
Plastic	8 Pins Package : TSG87511XP

SGS-THOMSON MICROELECTRONICS

BZW04-5V8, B → 376, B
BZW04P5V8, B → 376, B

UNI-AND BIDIRECTIONAL TRANSIENT VOLTAGE SUPPRESSORS

- HIGH SURGE CAPABILITY : 400 W / 1 ms EXPO
- VERY FAST CLAMPING TIME : 1 ps FOR UNIDIRECTIONAL TYPES 5 ns FOR BIDIRECTIONAL TYPES
- LARGE VOLTAGE RANGE : 5.8 V → 376 V
- ORDER CODE : TYPE NUMBER FOR UNIDIRECTIONAL TYPES, TYPE NUMBER + SUFFIX B FOR BIDIRECTIONAL TYPES



F 126
(Plastic)

DESCRIPTION

Transient voltage suppressor diodes especially useful in protecting integrated circuits, MOS, hybrids and other voltage-sensitive semiconductors and components.

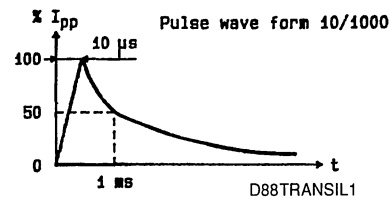
ABSOLUTE MAXIMUM RATINGS (limiting values)

Symbol	Parameter		Value	Unit
P_p	Peak Pulse Power for 1 ms Exponential Pulse	T_j Initial = 25 °C See note 1	400	W
P	Power Dissipation on Infinite Heatsink	T_{amb} = 50 °C	1.7	W
I_{FSM}	Non Repetitive Surge Peak Forward Current for Unidirectional Types	T_j Initial = 25 °C t = 10 ms	50	A
T_{stg} T_j	Storage and Operating Junction Temperature Range		– 55 to 150 150	°C °C
T_L	Maximum Lead Temperature for Soldering During 10 s at 4 mm from Case		230	°C

THERMAL RESISTANCE

Symbol	Parameter	Value	Unit
$R_{th(j-l)}$	Junction-leads on Infinite Heatsink for L_{lead} = 10 mm	60	°C/W

Note : 1. For surges upper than the maximum values, the diode will present a short-circuit anode-cathode



ELECTRICAL CHARACTERISTICS (T_j = 25 °C)

Symbol	Parameter		Value
V_{RM}	Stand-off Voltage		See tables
$V_{(BR)}$	Breakdown Voltage		
$V_{(CL)}$	Clamping Voltage		
I_{pp}	Peak Pulse Current		
α_T	Temperature Coefficient of $V_{(BR)}$		
C	Capacitance		
$t_{clamping}$	Clamping Time (0 volt to $V_{(BR)}$)	Unidirectional Types	1 ps max.
		Bidirectional Types	5 ns max.

Types		I_{RM} @ V_{RM} max.		$V_{(BR)}$* @ I_R (V)				$V_{(CL)}$ @ I_{pp} max. 1ms expo		$V_{(CL)}$ @ I_{pp} max. 8-20µs expo		α_T max.	C** typ. V_R=0 f=1MHz
Unidirectional	Bidirectional	(µA)	(V)	min.	nom.	max.	(mA)	(V)	(A)	(V)	(A)	(10^{-4}/°C)	(pF)
P BZW04P5V8	P BZW04P5V8B	1000	5.8	6.45	6 8	7.48	10	10.5	38	13 4	174	5.7	3500
BZW04-5V8	BZW04-5V8B	1000	5.8	6.45	6.8	7.14	10	10 5	38	13 4	174	5 7	3500
BZW04P6V4	P BZW04P6V4B	500	6.4	7.13	7.5	8.25	10	11.3	35.4	14.5	160	6.1	3100
BZW04-6V4	BZW04-6V4B	500	6.4	7.13	7.5	7.88	10	11.3	35.4	14.5	160	6.1	3100
BZW04P7V0	P BZW04P7V0B	200	7.02	7.79	8.2	9.02	10	12.1	33	15.5	148	6.5	2700
BZW04-7V0	BZW04-7V0B	200	7.02	7.79	8.2	8.61	10	12.1	33	15.5	148	6.5	2700
BZW04P7V8	BZW04P7V8B	50	7.78	8 65	9.1	10.0	1	13.4	30	17.1	134	6.8	2300
BZW04-7V8	BZW04-7V8B	50	7.78	8.65	9.1	9 55	1	13.4	30	17 1	134	6 8	2300
BZW04P8V5	BZW04P8V5B	10	8.55	9.50	10	11.0	1	14 5	27.6	18 6	258	7.3	2000
BZW04-8V5	BZW04-8V5B	10	8 55	9.50	10	10 50	1	14 5	27 6	18 6	258	7.3	2000
P BZW04P9V4	P BZW04P9V4B	5	9 4	10.5	11	12.1	1	15.6	25 7	20.3	236	7 5	1750
BZW04-9V4	BZW04-9V4B	5	9 4	10.5	11	11.6	1	15.6	25.7	20 3	236	7 5	1750
BZW04P10	BZW04P10B	5	10.2	11 4	12	13.2	1	16 7	24	21.7	221	7.8	1550
BZW04-10	BZW04-10B	5	10.2	11.4	12	12.6	1	16.7	24	21.7	221	7.8	1550
P BZW04P11	P BZW04P11B	5	11.1	12.4	13	14.3	1	18.2	22	23.6	203	8 1	1450
BZW04-11	BZW04-11B	5	11.1	12.4	13	13.7	1	18.2	22	23.6	203	8.1	1450
P BZW04P13	P BZW04P13B	5	12.8	14.3	15	16.5	1	21.2	19	27.2	176	8.4	1200
BZW04-13	BZW04-13B	5	12.8	14.3	15	15.8	1	21.2	19	27.2	176	8.4	1200
P BZW04P14	P BZW04P14B	5	13.6	15 2	16	17.6	1	22 5	17 8	28.9	166	8.6	1100
BZW04-14	BZW04-14B	5	13.6	15 2	16	16.8	1	22.5	17 8	28.9	166	8 6	1100
P BZW04P15	P BZW04P15B	5	15.3	17.1	18	19 8	1	25.2	16	32.5	148	8 8	975
BZW04-15	BZW04-15B	5	15 3	17.1	18	18.9	1	25.2	16	32.5	148	8.8	975
BZW04P17	BZW04P17B	5	17.1	19	20	22	1	27.7	14.5	36.1	133	9.0	850
BZW04-17	BZW04-17B	5	17.1	19	20	21	1	27.7	14.5	36.1	133	9.0	850
BZW04P19	BZW04P19B	5	18.8	20.9	22	24.2	1	30.6	13	39.3	122	9.2	800
BZW04-19	BZW04-19B	5	18.8	20.9	22	23 1	1	30.6	13	39.3	122	9 2	800
BZW04P20	P BZW04P20B	5	20.5	22 8	24	26.4	1	33.2	12	42 8	112	9.4	725
BZW04-20	BZW04-20B	5	20.5	22.8	24	25 2	1	33.2	12	42 8	112	9.4	725
P BZW04P23	BZW04P23B	5	23.1	25 7	27	29.7	1	37 5	10 7	48 3	99	9 6	625
BZW04-23	BZW04-23B	5	23 1	25.7	27	28.4	1	37 5	10.7	48 3	99	9.6	625
P BZW04P26	P BZW04P26B	5	25.6	28 5	30	33	1	41.5	9.6	53.5	90	9.7	575
BZW04-26	BZW04-26B	5	25 6	28.5	30	31 5	1	41.5	9 6	53.5	90	9.7	575
BZW04P28	P BZW04P28B	5	28 2	31.4	33	36.3	1	45.7	8.8	59	81.5	9.8	510
BZW04-28	BZW04-28B	5	28.2	31.4	33	34.7	1	45.7	8.8	59	81.5	9.8	510
P BZW04P31	P BZW04P31B	5	30.8	34.2	36	39.6	1	49.9	8	64.3	74.5	9.9	480
BZW04-31	BZW04-31B	5	30.8	34.2	36	37.8	1	49.9	8	64.3	74.5	9.9	480
P BZW04P33	BZW04P33B	5	33.3	37.1	39	42.9	1	53.9	7.4	69.7	69	10.0	450

* Pulse test $t_p \leq 50$ ms $\delta < 2$ %

** Divide these values by 2 for bidirectional types

For bidirectional types, electrical characteristics apply in both directions.

P · Preferred device.

Types		I_{RM} @ V_{RM} max.		$V_{(BR)}$* @ I_R (V)				$V_{(CL)}$ @ I_{pp} max. 1ms expo		$V_{(CL)}$ @ I_{pp} max. 8-20µs expo		α_T max.	C** typ. V_R=0 f=1MHz
Unidirectional	Bidirectional	(µA)	(V)	min.	nom.	max.	(mA)	(V)	(A)	(V)	(A)	(10^{-4}/°C)	(pF)
BZW04-33	BZW04-33B	5	33.3	37.1	39	41	1	53.9	7.4	69.7	69	10.0	450
BZW04P37	P BZW04P37B	5	36.8	40.9	43	47.3	1	59.3	6.7	76 8	62 5	10 1	400
BZW04-37	BZW04-37B	5	36 8	40.9	43	45.2	1	59.3	6.7	76.8	62.5	10.1	400
BZW04P40	BZW04P40B	5	40.2	44.7	47	51.7	1	64.8	6.2	84	57	10.1	370
BZW04-40	BZW04-40B	5	40.2	44.7	47	49.4	1	64.8	6.2	84	57	10.1	370
BZW04P44	BZW04P44B	5	43.6	48.5	51	56 1	1	70.1	5.7	91	52.5	10.2	350
BZW04-44	BZW04-44B	5	43.6	48 5	51	53.6	1	70.1	5.7	91	52.5	10.2	350
BZW04P48	BZW04P48B	5	47.8	53 2	56	61.6	1	77	5 2	100	48	10.3	320
BZW04-48	BZW04-48B	5	47.8	53 2	56	58.8	1	77	5 2	100	48	10.3	320
BZW04P53	BZW04P53B	5	53	58 9	62	68 2	1	85	4.7	111	43	10 4	290
BZW04-53	BZW04-53B	5	53	58 9	62	65.1	1	85	4.7	111	43	10.4	290
BZW04P58	BZW04P58B	5	58.1	64.6	68	74.8	1	92	4.3	121	39.5	10.4	270
BZW04-58	BZW04-58B	5	58.1	64 6	68	71 4	1	92	4.3	121	39.5	10.4	270
BZW04P64	BZW04P64B	5	64.1	71.3	75	82.5	1	103	3.9	134	36	10.5	250
BZW04-64	BZW04-64B	5	64.1	71.3	75	78.8	1	103	3.9	134	36	10.5	250
BZW04P70	P BZW04P70B	5	70 1	77.9	82	90.2	1	113	3.5	146	33	10.5	230
BZW04-70	BZW04-70B	5	70.1	77.9	82	86.1	1	113	3.5	146	33	10.5	230
BZW04P78	BZW04P78B	5	77.8	86.5	91	100	1	125	3.2	162	29.5	10 6	210
BZW04-78	BZW04-78B	5	77.8	86 5	91	95.5	1	125	3.2	162	29.5	10.6	210
P BZW04P85	BZW04P85B	5	85.5	95	100	110	1	137	2.9	178	27	10.6	200
BZW04-85	BZW04-85B	5	85.5	95	100	105	1	137	2.9	178	27	10.6	200
BZW04P94	BZW04P94B	5	94	105	110	121	1	152	2.6	195	24.5	10.7	185
BZW04-94	BZW04-94B	5	94	105	110	116	1	152	2.6	195	24.5	10.7	185
BZW04P102	BZW04P102B	5	102	114	120	132	1	165	2.4	212	22.5	10.7	170
BZW04-102	BZW04-102B	5	102	114	120	126	1	165	2.4	212	22.5	10.7	170
P BZW04P111	BZW04P111B	5	111	124	130	143	1	179	2.2	230	20.8	10.7	165
BZW04-111	BZW04-111B	5	111	124	130	137	1	179	2.2	230	20 8	10.7	165
P BZW04P128	P BZW04P128B	5	128	143	150	165	1	207	2.0	265	18.1	10.8	145
BZW04-128	BZW04-128B	5	128	143	150	158	1	207	2.0	265	18.1	10.8	145
P BZW04P136	P BZW04P136B	5	136	152	160	176	1	219	1.8	282	17	10.8	140
BZW04-136	BZW04-136B	5	136	152	160	168	1	219	1.8	282	17	10.8	140
P BZW04P145	BZW04P145B	5	145	161	170	187	1	234	1.7	301	16	10.8	135
BZW04-145	BZW04-145B	5	145	161	170	179	1	234	1.7	301	16	10 8	135
BZW04P154	BZW04P154B	5	154	171	180	198	1	246	1.6	317	15.1	10.8	125
BZW04-154	BZW04-154B	5	154	171	180	189	1	246	1.6	317	15.1	10.8	125
BZW04P171	BZW04P171B	5	171	190	200	220	1	274	1.5	353	13 6	10.8	120
BZW04-171	BZW04-171B	5	171	190	200	210	1	274	1 5	353	13.6	10.8	120
BZW04P188	P BZW04P188B	5	188	209	220	242	1	301	1.4	388	12.4	10.8	110
BZW04-188	BZW04-188B	5	188	209	220	231	1	301	1.4	388	12.4	10.8	110
P BZW04P213	BZW04P213B	5	213	237	250	275	1	344	1.5	442	12	11	100
BZW04-213	BZW04-213B	5	213	237	250	263	1	344	1.5	442	12	11	100
P BZW04P239	BZW04P239B	5	239	266	280	308	1	384	1.5	494	12	11	95
BZW04-239	BZW04-239B	5	239	266	280	294	1	384	1.5	494	12	11	95
BZW04P256	BZW04P256B	5	256	285	300	330	1	414	1.2	529	10	11	90
BZW04-256	BZW04-256B	5	256	285	300	315	1	414	1.2	529	10	11	90
BZW04P273	BZW04P273B	5	273	304	320	352	1	438	1.2	564	10	11	85
BZW04-273	BZW04-273B	5	273	304	320	336	1	438	1 2	564	10	11	85
P BZW04P299	BZW04P299B	5	299	332	350	385	1	482	0 9	618	9	11	80
BZW04-299	BZW04-299B	5	299	332	350	368	1	482	0 9	618	9	11	80
BZW04P342	BZW04P342B	5	342	380	400	440	1	548	0.9	706	8	11	75
BZW04-342	BZW04-342B	5	342	380	400	420	1	548	0.9	706	8	11	75
BZW04P376	BZW04P376B	5	376	418	440	484	1	603	0.8	776	8	11	70
BZW04-376	BZW04-376B	5	376	418	440	462	1	603	0.8	776	8	11	70

* Pulse test $t_p \leq 50$ ms $\delta < 2$ %.

** Divide these values by 2 for bidirectional types.

For bidirectional types, electrical characteristics apply in both directions

P · Preferred device

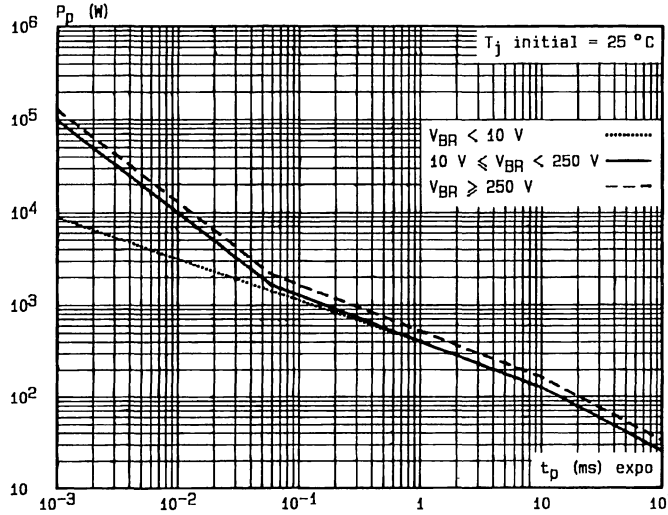


Fig.1 - Peak pulse power versus exponential pulse duration.

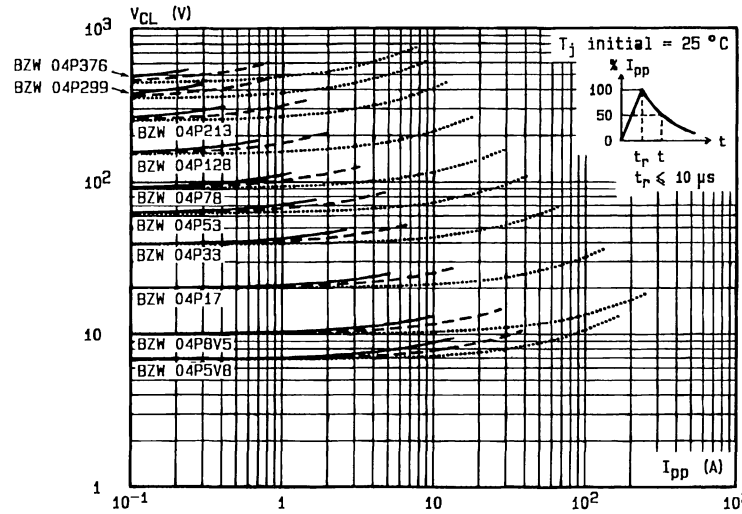


Fig.2 - Clamping voltage versus peak pulse current.
exponential waveform t = 20 µs ·····
t = 1 ms – – –
t = 10 ms ——

Note : The curves of the figure 2 are specified for a junction temperature of 25 °C before surge. The given results may be extrapolated for other junction temperatures by using the following formula : $\Delta V_{(BR)} = \alpha_{T(V(BR))} \times [T_j - 25] \times V_{(BR)}$
For intermediate voltages, extrapolate the given results.

D88BZW04P4

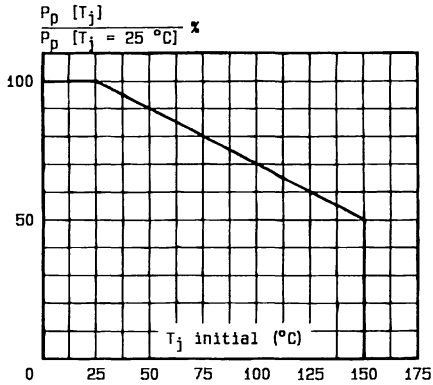


Fig.3 - Allowable power dissipation versus junction temperature.

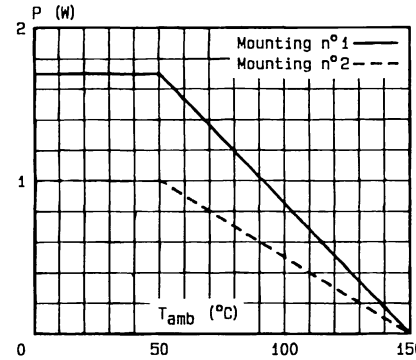


Fig.4 - Power dissipation versus ambient temperature.

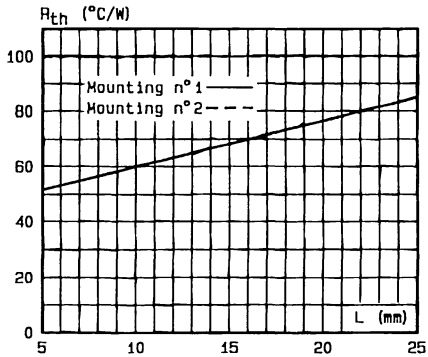


Fig.5 - Thermal resistance versus lead length.

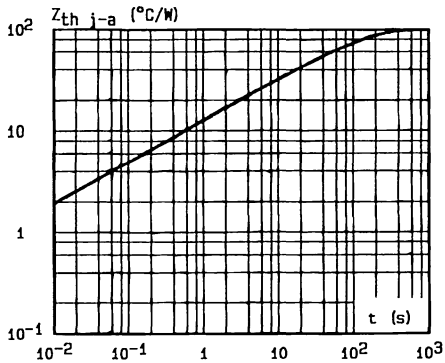


Fig.6 - Transient thermal impedance junction-ambient for mounting n°2 versus pulse duration (L = 10 mm).

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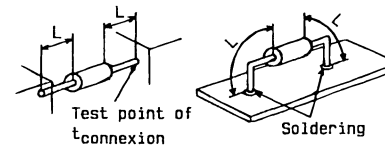
Mounting n°1
INFINITE HEATSINK

Mounting n°2
PRINTED CIRCUIT



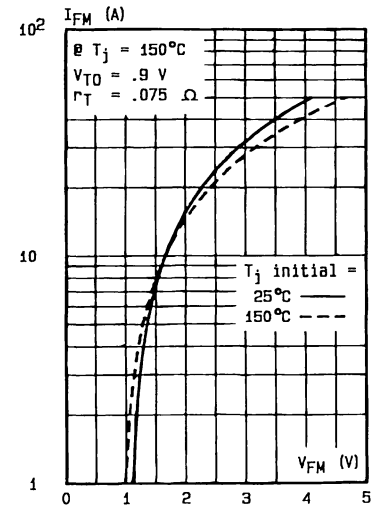


Fig.7 - Peak forward current versus peak forward voltage drop (typical values for unidirectional types).

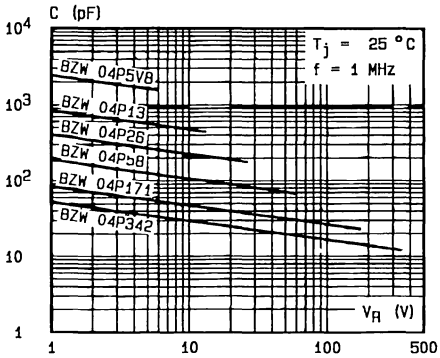


Fig.8a - Capacitance versus reverse applied voltage for unidirectional types (typical values).

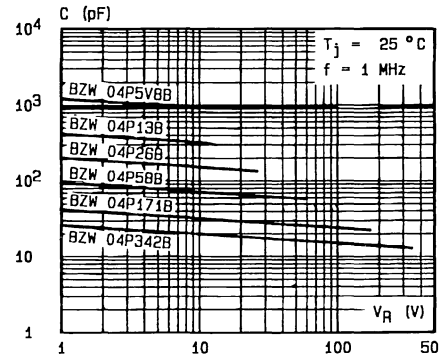


Fig.8b - Capacitance versus reverse applied voltage for bidirectional types (typical values).

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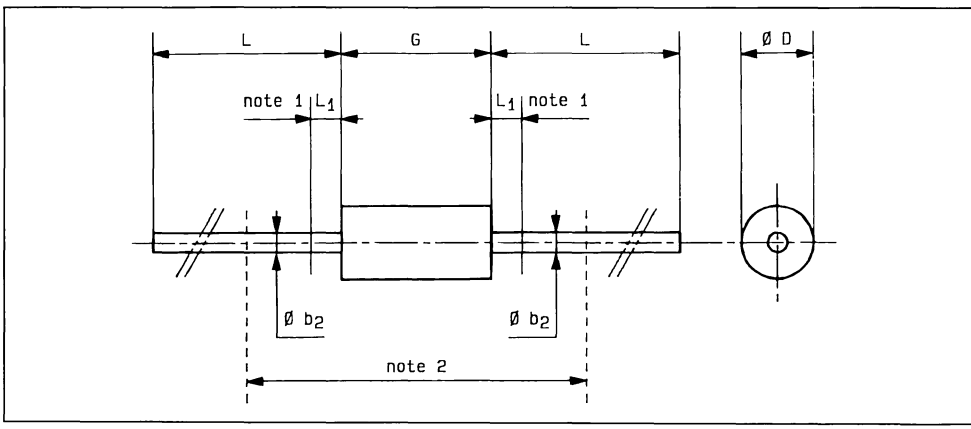
PACKAGE MECHANICAL DATA

F 126 Plastic

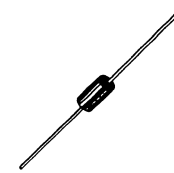


Ref.	Millimeters		Inches		Notes
	Min.	Max.	Min.	Max.	
Ø b_2	0.76	0.86	0.029	0.034	1 - The lead diameter Ø b_2 is not controlled over zone L_1. 2 - The minimum axial lengh within which the device may be placed with its leads bent at right angles is 0.59" (15 mm).
Ø D	2.95	3.05	0.116	0.120	
G	6.05	6.35	0.238	0 250	
L	26	–	1.024	–	
L_1	–	1.27	–	0.050	

Cooling method : by convection (method A).
Marking . type number , white band indicates cathode for unidirectional types.
Weight : 0.4 g.

UNI-AND BIDIRECTIONAL TRANSIENT VOLTAGE SUPPRESSORS

- HIGH SURGE CAPABILITY : 600 W / 1 ms EXPO
- VERY FAST CLAMPING TIME : 1 ps FOR UNIDIRECTIONAL TYPES 5 ns FOR BIDIRECTIONAL TYPES
- LARGE VOLTAGE RANGE : 5.8 V → 376 V
- ORDER CODE : TYPE NUMBER FOR UNIDIRECTIONAL TYPES, TYPE NUMBER + SUFFIX C FOR BIDIRECTIONAL TYPES



CB-417
(Plastic)

DESCRIPTION

Transient voltage suppressor diodes especially useful in protecting integrated circuits, MOS, hybrids and other voltage-sensitive semiconductors and components.

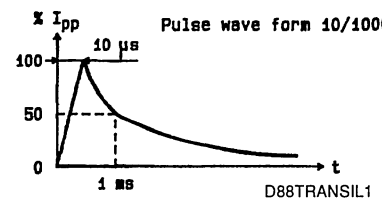
ABSOLUTE RATINGS (limiting values)

Symbol	Parameter		Value	Unit
P_p	Peak Pulse Power for 1 ms Exponential Pulse	T_j Initial = 25 °C See note 1	600	W
P	Power Dissipation on Infinite Heatsink	T_{amb} = 75 °C	5	W
I_{FSM}	Non Repetitive Surge Peak Forward Current for Unidirectional Types	T_j Initial = 25 °C t = 10 ms	100	A
T_{stg} T_j	Storage and Operating Junction Temperature Range		– 55 to 175 175	°C °C
T_L	Maximum Lead Temperature for Soldering During 10 s at 4 mm from Case		230	°C

THERMAL RESISTANCE

Symbol	Parameter	Value	Unit
$R_{th(j-l)}$	Junction-leads on Infinite Heatsink for L_{lead} = 10 mm	20	°C/W

Note : 1. For surges upper than the maximum values, the diode will present a short-circuit anode-cathode.



D88TRANSIL1

ELECTRICAL CHARACTERISTICS (T_j = 25 °C)

Symbol	Parameter		Value
V_{RM}	Stand-off Voltage		See tables
$V_{(BR)}$	Breakdown Voltage		
$V_{(CL)}$	Clamping Voltage		
I_{pp}	Peak Pulse Current		
α_T	Temperature Coefficient of $V_{(BR)}$		
C	Capacitance		
$t_{clamping}$	Clamping Time (0 volt to $V_{(BR)}$)	Unidirectional Types	1 ps max.
		Bidirectional Types	5 ns max.
V_{FM}	Forward Voltage Drop for Unidirectional Types (I_{FM} = 50 A)		3.5 V max.

Types		I_{RM} @ V_{RM} max.		$V_{(BR)}$* @ I_R (V)				$V_{(CL)}$ @ I_{pp} max. 1 ms expo		$V_{(CL)}$ @ I_{pp} max. 8-20 µs expo		α_T max.	C** typ V_R=0 f=1 MHz
Unidirectional	Bidirectional	(µA)	(V)	min.	nom.	max.	(mA)	(V)	(A)	(V)	(A)	(10^{-4}/°C)	(pF)
P P6KE6V8P	P P6KE6V8CP	1000§	5.8	6.45	6.8	7.48	10	10.5	57	13.4	261	5.7	4000
P6KE6V8A	P6KE6V8CA	1000§	5.8	6.45	6.8	7.14	10	10.5	57	13.4	261	5.7	4000
P P6KE7V5P	P P6KE7V5CP	500§	6.4	7.13	7.5	8.25	10	11.3	53	14.5	241	6.1	3700
P6KE7V5A	P6KE7V5CA	500§	6.4	7.13	7.5	7.88	10	11.3	53	14.5	241	6.1	3700
P P6KE8V2P	P6KE8V2CP	200§	7.02	7.79	8.2	9.02	10	12.1	50	15.5	226	6.5	3400
P6KE8V2A	P6KE8V2CA	200§	7.02	7.79	8.2	8.61	10	12.1	50	15.5	226	6.5	3400
P6KE9V1P	P6KE9V1CP	50§	7.78	8.65	9.1	10	1	13.4	45	17.1	205	6.8	3100
P6KE9V1A	P6KE9V1CA	50§	7.78	8.65	9.1	9.55	1	13.4	45	17.1	205	6.8	3100
P6KE10P	P6KE10CP	10§	8.55	9.5	10	11	1	14.5	41	18.6	387	7.3	2800
P6KE10A	P6KE10CA	10§	8.55	9.5	10	10.5	1	14.5	41	18.6	387	7.3	2800
P6KE11P	P6KE11CP	5§	9.4	10.5	11	12.1	1	15.6	38	20.3	355	7.5	2500
P6KE11A	P6KE11CA	5§	9.4	10.5	11	11.6	1	15.6	38	20.3	355	7.5	2500
P P6KE12P	P P6KE12CP	5	10.2	11.4	12	13.2	1	16.7	36	21.7	332	7 8	2300
P6KE12A	P6KE12CA	5	10.2	11.4	12	12.6	1	16.7	36	21.7	332	7.8	2300
P P6KE13P	P P6KE13CP	5	11.1	12.4	13	14.3	1	18.2	33	23.6	305	8.1	2150
P6KE13A	P6KE13CA	5	11.1	12.4	13	13.7	1	18.2	33	23.6	305	8.1	2150
P P6KE15P	P P6KE15CP	5	12.8	14.3	15	16.5	1	21.2	28	27.2	265	8.4	1900
P6KE15A	P6KE15CA	5	12.8	14.3	15	15.8	1	21.2	28	27.2	265	8.4	1900
P6KE16P	P6KE16CP	5	13.6	15.2	16	17.6	1	22.5	27	28.9	249	8.6	1800
P6KE16A	P6KE16CA	5	13.6	15.2	16	16.8	1	22.5	27	28.9	249	8.6	1800
P P6KE18P	P P6KE18CP	5	15.3	17.1	18	19.8	1	25.2	24	32.5	222	8.8	1600
P6KE18A	P6KE18CA	5	15.3	17.1	18	18.9	1	25.2	24	32.5	222	8.8	1600
P P6KE20P	P6KE20CP	5	17.1	19	20	22	1	27.7	22	36.1	199	9.0	1500
P6KE20A	P6KE20CA	5	17.1	19	20	21	1	27.7	22	36.1	199	9.0	1500
P6KE22P	P P6KE22CP	5	18.8	20.9	22	24.2	1	30.6	20	39.3	183	9.2	1350
P6KE22A	P6KE22CA	5	18.8	20.9	22	23.1	1	30.6	20	39.3	183	9.2	1350
P6KE24P	P6KE24CP	5	20.5	22.8	24	26.4	1	33.2	18	42.8	168	9.4	1250
P6KE24A	P6KE24CA	5	20.5	22.8	24	25.2	1	33.2	18	42.8	168	9.4	1250
P P6KE27P	P6KE27CP	5	23.1	25.7	27	29.7	1	37.5	16	48.3	149	9.6	1150
P6KE27A	P6KE27CA	5	23.1	25.7	27	28.4	1	37.5	16	48 3	149	9 6	1150
P P6KE30P	P6KE30CP	5	25.6	28.5	30	33	1	41.5	14 5	53.5	134	9.7	1075
P6KE30A	P6KE30CA	5	25 6	28.5	30	31.5	1	41.5	14.5	53.5	134	9.7	1075
P P6KE33P	P P6KE33CP	5	28 2	31.4	33	36.3	1	45.7	13.1	59	122	9.8	1000
P6KE33A	P6KE33CA	5	28 2	31.4	33	34.7	1	45.7	13.1	59	122	9.8	1000
P P6KE36P	P6KE36CP	5	30.8	34.2	36	39.6	1	49.9	12	64.3	112	9.9	950
P6KE36A	P6KE36CA	5	30.8	34.2	36	37.8	1	49.9	12	64.3	112	9.9	950

* Pulse test $t_p \leq 50$ ms $\delta < 2$ %.
** Divide these values by 2 for bidirectional types.
For bidirectional types P6KE6V8CP → 11CA, IRM must be double that specified for unidirectional types.
For bidirectional types, electrical characteristics apply in both directions.
P : Preferred device.

Types		I_{RM} @ V_{RM} max.		$V_{(BR)}$* @ I_R (V)				$V_{(CL)}$ @ I_{pp} max. 1 ms expo		V_{CL} @ I_{pp} max. 8-20 µs expo		α_T max.	C** typ. V_R=0 f=1 MHz
Unidirectional	Bidirectional	(µA)	(V)	min.	nom.	max.	(mA)	(V)	(A)	(V)	(A)	(10^{-4}/°C)	(pF)
P P6KE39P	P P6KE39CP	5	33.3	37.1	39	42.9	1	53.9	11.1	69.7	103	10.0	900
P6KE39A	P6KE39CA	5	33.3	37.1	39	41	1	53.9	11.1	69.7	103	10.0	900
P6KE43P	P6KE43CP	5	36.8	40.9	43	47.3	1	59.3	10.1	76.8	94	10.1	850
P6KE43A	P6KE43CA	5	36.8	40.9	43	45.2	1	59.3	10.1	76.8	94	10.1	850
P6KE47P	P P6KE47CP	5	40.2	44.7	47	51.7	1	64.8	9.3	84	86	10.1	800
P6KE47A	P6KE47CA	5	40.2	44.7	47	49.4	1	64.8	9.3	84	86	10.1	800
P P6KE51P	P6KE51CP	5	43.6	48.5	51	56.1	1	70.1	8.6	91	79	10.2	750
P6KE51A	P6KE51CA	5	43.6	48.5	51	53.6	1	70.1	8.6	91	79	10.2	750
P P6KE56P	P6KE56CP	5	47.8	53.2	56	61.6	1	77	7.8	100	72	10.3	700
P6KE56A	P6KE56CA	5	47.8	53.2	56	58.8	1	77	7.8	100	72	10.3	700
P6KE62P	P6KE62CP	5	53	58.9	62	68.2	1	85	7.1	111	65	10.4	650
P6KE62A	P6KE62CA	5	53	58.9	62	65.1	1	85	7.1	111	65	10.4	650
P P6KE68P	P6KE68CP	5	58.1	64.6	68	74.8	1	92	6.5	121	59.5	10.4	625
P6KE68A	P6KE68CA	5	58.1	64.6	68	71.4	1	92	6.5	121	59.5	10.4	625
P6KE75P	P6KE75CP	5	64.1	71.3	75	82.5	1	103	5.8	134	53.5	10.5	575
P6KE75A	P6KE75CA	5	64.1	71.3	75	78.8	1	103	5.8	134	53.5	10.5	575
P P6KE82P	P6KE82CP	5	70.1	77.9	82	90.2	1	113	5.3	146	49	10.5	550
P6KE82A	P6KE82CA	5	70.1	77.9	82	86.1	1	113	5.3	146	49	10.5	550
P6KE91P	P6KE91CP	5	77.8	86.5	91	100	1	125	4.8	162	44.5	10 6	525
P6KE91A	P6KE91CA	5	77.8	86.5	91	95.5	1	125	4.8	162	44.5	10.6	525
P6KE100P	P6KE100CP	5	85.5	95	100	110	1	137	4.4	178	40.5	10.6	500
P6KE100A	P6KE100CA	5	85.5	95	100	105	1	137	4.4	178	40.5	10.6	500
P6KE110P	P6KE110CP	5	94	105	110	121	1	152	3.9	195	37	10.7	470
P6KE110A	P6KE110CA	5	94	105	110	116	1	152	3.9	195	37	10.7	470
P6KE120P	P6KE120CP	5	102	114	120	132	1	165	3.6	212	34	10.7	450
P6KE120A	P6KE120CA	5	102	114	120	126	1	165	3.6	212	34	10.7	450
P P6KE130P	P6KE130CP	5	111	124	130	143	1	179	3.4	230	31.5	10.7	420
P6KE130A	P6KE130CA	5	111	124	130	137	1	179	3.4	230	31.5	10.7	420
P6KE150P	P6KE150CP	5	128	143	150	165	1	207	2.9	265	27 2	10.8	400
P6KE150A	P6KE150CA	5	128	143	150	158	1	207	2.9	265	27.2	10.8	400
P6KE160P	P P6KE160CP	5	136	152	160	176	1	219	2.7	282	25 5	10.8	380
P6KE160A	P6KE160CA	5	136	152	160	168	1	219	2.7	282	25.5	10.8	380
P6KE170P	P6KE170CP	5	145	161	170	187	1	234	2.6	301	24	10.8	370
P6KE170A	P6KE170CA	5	145	161	170	179	1	234	2.6	301	24	10.8	370
P P6KE180P	P6KE180CP	5	154	171	180	198	1	246	2.4	317	22.7	10.8	360
P6KE180A	P6KE180CA	5	154	171	180	189	1	246	2.4	317	22.7	10.8	360
P P6KE200P	P6KE200CP	5	171	190	200	220	1	274	2.2	353	20.4	10.8	350
P6KE200A	P6KE200CA	5	171	190	200	210	1	274	2.2	353	20.4	10.8	350
P6KE220P	P6KE220CP	5	188	209	220	242	1	301	2	388	18.6	10.8	330
P6KE220A	P6KE220CA	5	188	209	220	231	1	301	2	388	18 6	10.8	330
P P6KE250P	P6KE250CP	5	213	237	250	275	1	344	2	442	19	11	310
P6KE250A	P6KE250CA	5	213	237	250	263	1	344	2	442	19	11	310
P6KE280P	P6KE280CP	5	239	266	280	308	1	384	2	494	18	11	300
P6KE280A	P6KE280CA	5	239	266	280	294	1	384	2	494	18	11	300
P6KE300P	P6KE300CP	5	256	285	300	330	1	414	1.6	529	14	11	290
P6KE300A	P6KE300CA	5	256	285	300	315	1	414	1.6	529	14	11	290
P6KE320P	P6KE320CP	5	273	304	320	352	1	438	1.6	564	14	11	280
P6KE320A	P6KE320CA	5	273	304	320	336	1	438	1.6	564	14	11	280
P6KE350P	P6KE350CP	5	299	332	350	385	1	482	1.6	618	14	11	270
P6KE350A	P6KE350CA	5	299	332	350	368	1	482	1.6	618	14	11	270
P P6KE400P	P P6KE400CP	5	342	380	400	440	1	548	1.3	706	11	11	360
P6KE400A	P6KE400CA	5	342	380	400	420	1	548	1.3	706	11	11	360
P P6KE440P	P6KE440CP	5	376	418	440	484	1	603	1.3	776	11	11	350
P6KE440A	P6KE440CA	5	376	418	440	462	1	603	1.3	776	11	11	350

* Pulse test $t_p \leq 50$ ms $\delta < 2$ %.
** Divide these values by 2 for bidirectional types.
For bidirectional types, electrical characteristics apply in both directions.
P : Preferred device.

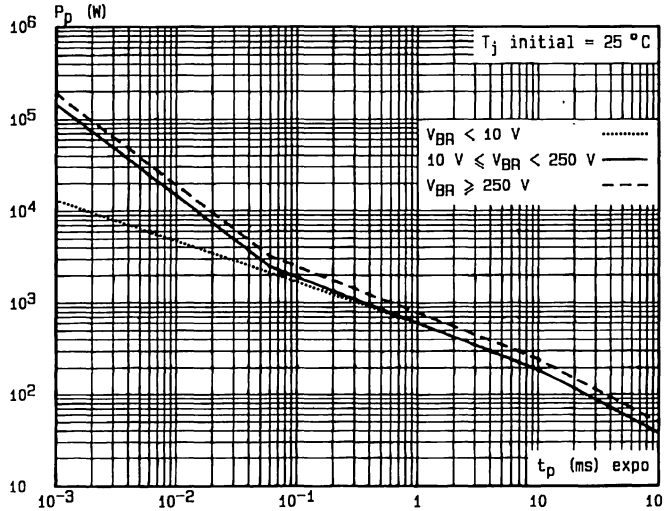


Fig.1 - Peak pulse power versus exponential pulse duration.

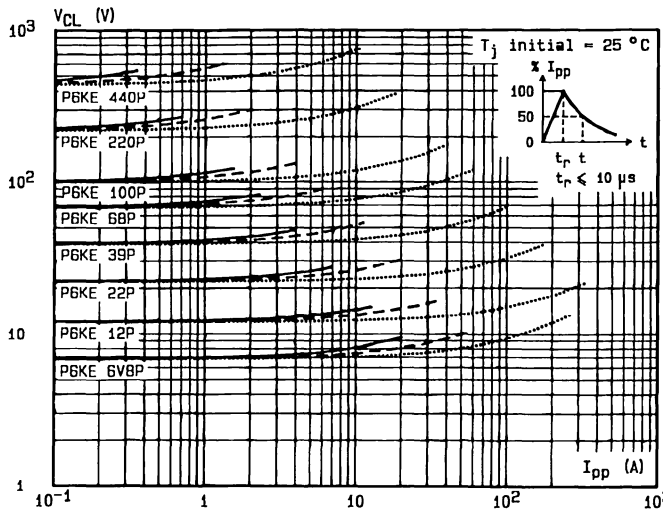


Fig.2 - Clamping voltage versus peak pulse current.
exponential waveform t = 20 µs ·····
t = 1 ms – – –
t = 10 ms ——

Note : The curves of the figure 2 are specified for a junction temperature of 25 °C before surge. The given results may be extrapolated for other junction temperatures by using the following formula : $\Delta V_{(BR)} = \alpha_{T(V(BR))} \times [T_j - 25] \times V_{(BR)}$
For intermediate voltages, extrapolate the given results.

D88P6KEP4

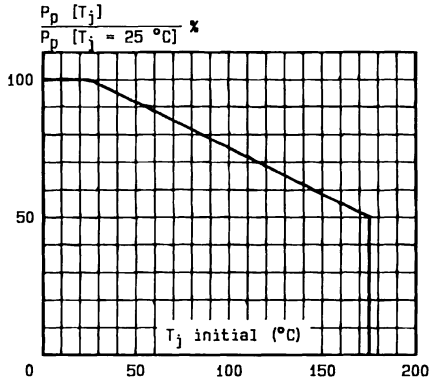


Fig.3 - Allowable power dissipation versus junction temperature.

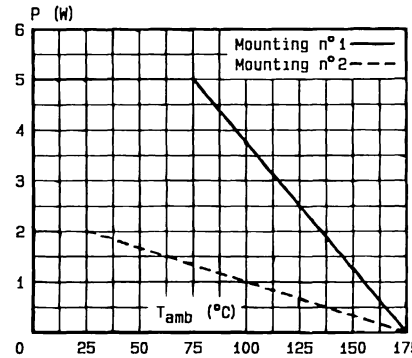


Fig.4 - Power dissipation versus ambient temperature.

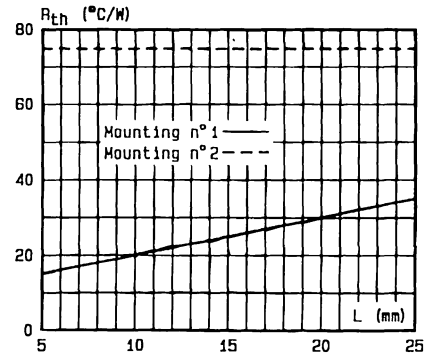


Fig.5 - Thermal resistance versus lead length.

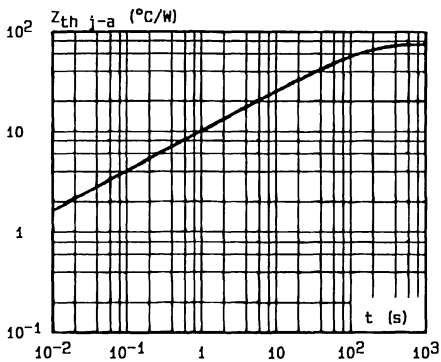
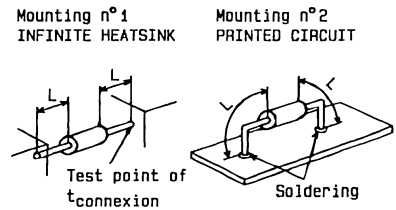


Fig.6 - Transient thermal impedance junction-ambient for mounting n°2 versus pulse duration (L = 10 mm).



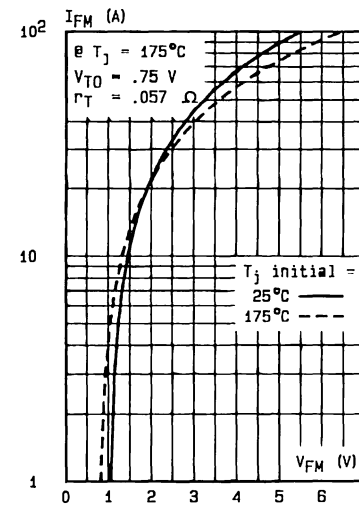


Fig.7 - Peak forward current versus peak forward voltage drop (typical values for unidirectional types).

D88P6KEP5

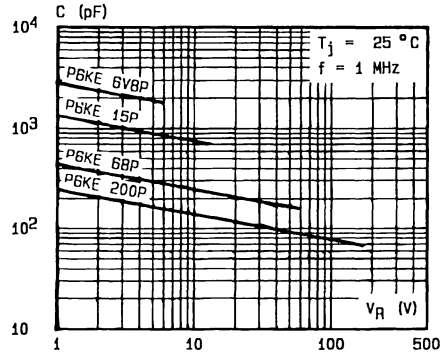


Fig.8a - Capacitance versus reverse applied voltage for unidirectional types (typical values).

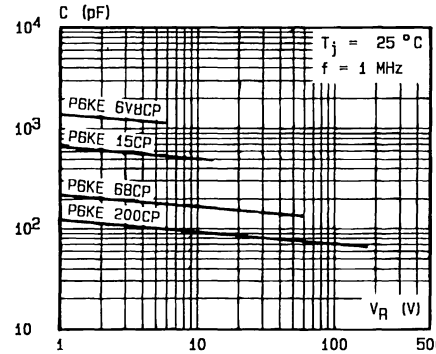
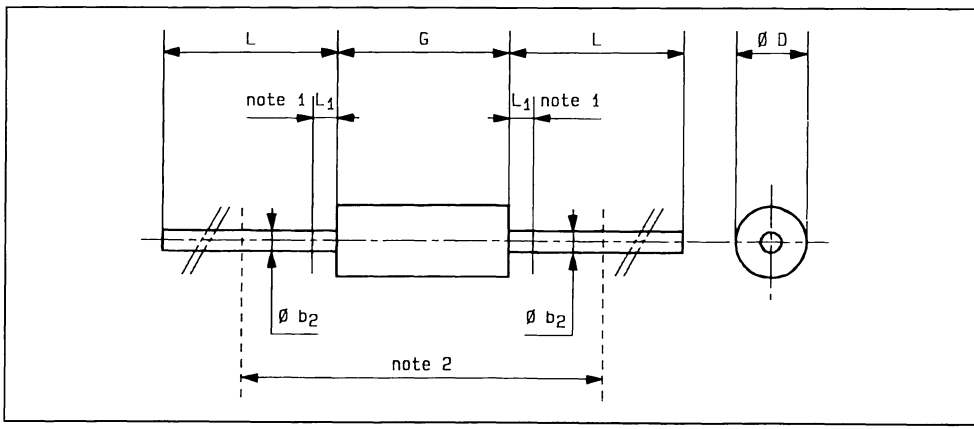


Fig.8b - Capacitance versus reverse applied voltage for bidirectional types (typical values).

D88P6KEP6

PACKAGE MECHANICAL DATA

CB-417 Plastic



Ref.	Millimeters		Inches		Notes
	Min.	Max.	Min.	Max.	
Ø b_2	–	1.092	–	0.043	1 - The lead diameter Ø b_2 is not controlled over zone L_1. 2 - The minimum axial lengh within which the device may be placed with its leads bent at right angles is 0.59" (15 mm).
Ø D	–	3.683	–	0.145	
G	–	8 89	–	0.350	
L	25 4	–	1.000	–	
L_1	–	1.25	–	0.049	

Cooling method : by convection (method A).
Marking : type number ; white band indicates cathode for unidirectional types.
Weight : 0.6 g

SGS-THOMSON MICROELECTRONICS

P7T-10, B → 110, B

UNI-AND BIDIRECTIONAL TRANSIENT VOLTAGE SUPPRESSORS

- HIGH SURGE CAPABILITY : 700 W / 1 ms EXPO
- VERY FAST CLAMPING TIME : 1 ps FOR UNIDIRECTIONAL TYPES 5 ns FOR BIDIRECTIONAL TYPES
- LARGE VOLTAGE RANGE : 10 V → 110 V
- ORDER CODE : TYPE NUMBER FOR UNIDIRECTIONAL TYPES, TYPE NUMBER + SUFFIX B FOR BIDIRECTIONAL TYPES

CB-417
(Plastic)

DESCRIPTION

Transient voltage suppressor diodes especially useful in protecting integrated circuits, MOS, hybrids and other voltage-sensitive semiconductors and components.

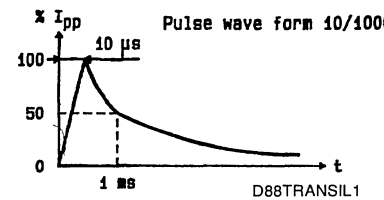
ABSOLUTE RATINGS (limiting values)

Symbol	Parameter		Value	Unit
P_p	Peak Pulse Power for 1 ms Exponential Pulse	T_j Initial = 25 °C See note 1	700	W
P	Power Dissipation on Infinite Heatsink	T_{amb} = 50 °C	5	W
I_{FSM}	Non Repetitive Surge Peak Forward Current for Unidirectional Types	T_j Initial = 25 °C t = 10 ms	120	A
T_{stg} T_j	Storage and Operating Junction Temperature Range		– 55 to 150 150	°C °C
T_L	Maximum Lead Temperature for Soldering During 10 s at 4 mm from Case		230	°C

THERMAL RESISTANCE

Symbol	Parameter	Value	Unit
$R_{th(j-l)}$	Junction-leads on Infinite Heatsink for L_{lead} = 10 mm	20	°C/W

Note : 1. For surges upper than the maximum values, the diode will present a short-circuit anode-cathode.



D88TRANSIL1

ELECTRICAL CHARACTERISTICS (T_j = 25 °C)

Symbol	Parameter		Value
V_{RM}	Stand-off Voltage		See tables
$V_{(BR)}$	Breakdown Voltage		
$V_{(CL)}$	Clamping Voltage		
I_{pp}	Peak Pulse Current		
α_T	Temperature Coefficient of $V_{(BR)}$		
C	Capacitance		
$t_{clamping}$	Clamping Time (0 volt to $V_{(BR)}$)	Unidirectional Types	1 ps max.
		Bidirectional Types	5 ns max.

Types		I_{RM} @ V_{RM} max.		$V_{(BR)}$* @ I_R (V)				$V_{(CL)}$ @ I_{pp} max. 1 ms expo		$V_{(CL)}$ @ I_{pp} max. 8-20 µs expo		α_T max.	C** typ. V_R=0 f=1 MHz
Unidirectional	Bidirectional	(µA)	(V)	min.	nom.	max.	(mA)	(V)	(A)	(V)	(A)	(10^{-4}/°C)	(pF)
P7T-10	P7T-10B	5	10	13	18	20	5	25	30	32	265	8.4	2600
P7T-27	P7T-27B	5	27	29.6	36	43.5	5	53	13	68	125	9.6	1100
P7T-43	P7T-43B	5	43	50	62	75	5	90	8	115	74	10.3	620
P7T-110	P7T-110B	5	110	130	160	200	5	235	3	300	28	10.8	370

* Pulse test $t_p \leq 50$ ms $\delta < 2$ %.
** Divide these values by 2 for bidirectional types.
For bidirectional types, electrical characteristics apply in both directions.

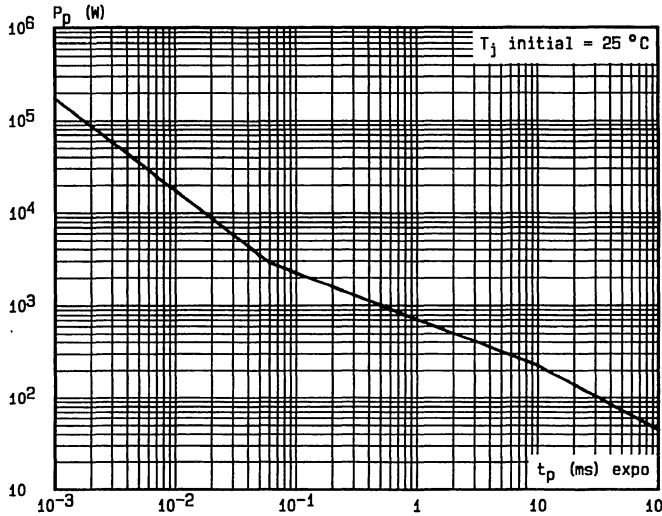


Fig.1 - Peak pulse power versus exponential pulse duration.

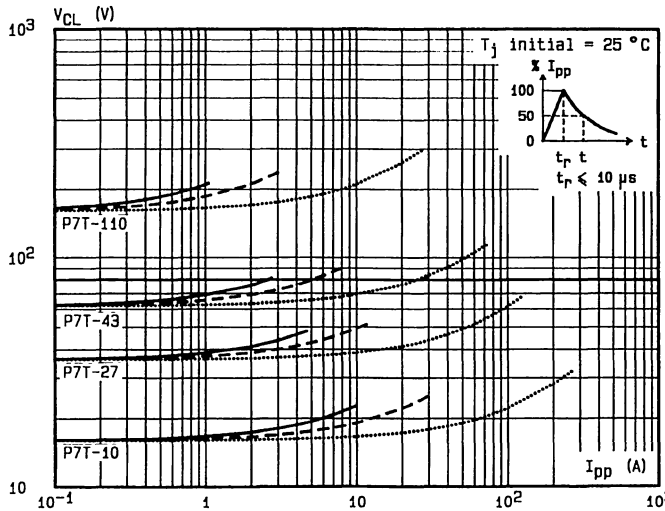


Fig.2 - Clamping voltage versus peak pulse current.
exponential waveform t = 20 µs ·····
t = 1 ms – – –
t = 10 ms ——

Note : The curves of the figure 2 are specified for a junction temperature of 25 °C before surge. The given results may be extrapolated for other junction temperatures by using the following formula : $\Delta V_{(BR)} = \alpha_T (V_{(BR)}) \times [T_j - 25] \times V_{(BR)}$
For intermediate voltages, extrapolate the given results.

D88P7TP3

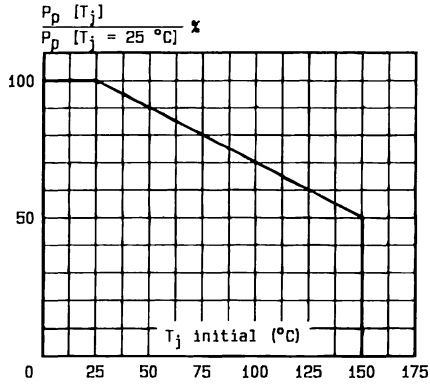


Fig.3 - Allowable power dissipation versus junction temperature.

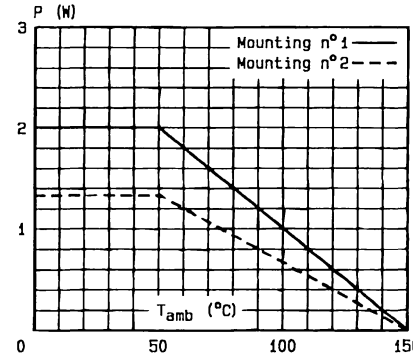


Fig.4 - Power dissipation versus ambient temperature.

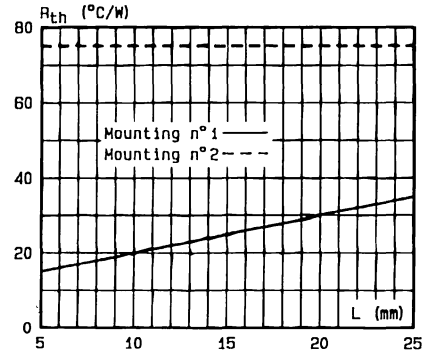
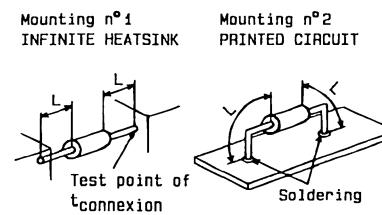


Fig.5 - Thermal resistance versus lead length.



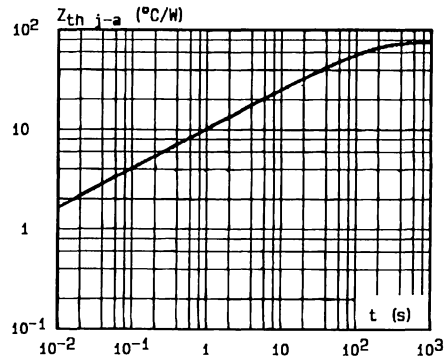


Fig.6 - Transient thermal impedance junction-ambient for mounting n°2 versus pulse duration (L = 10 mm).

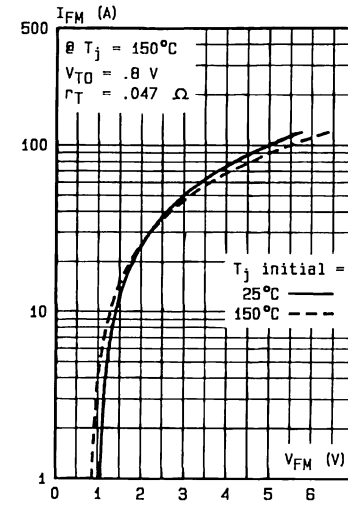


Fig.7 - Peak forward current versus peak forward voltage drop (typical values for unidirectional types).

D88P7TP4

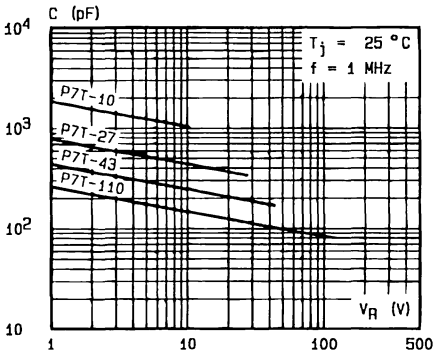


Fig.8a - Capacitance versus reverse applied voltage for unidirectional types (typical values).

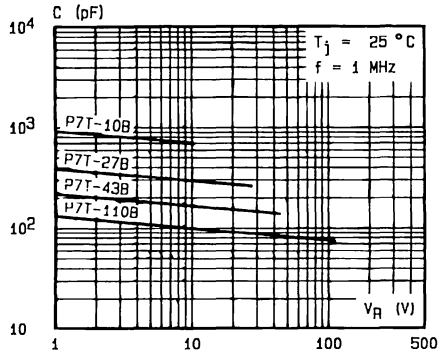
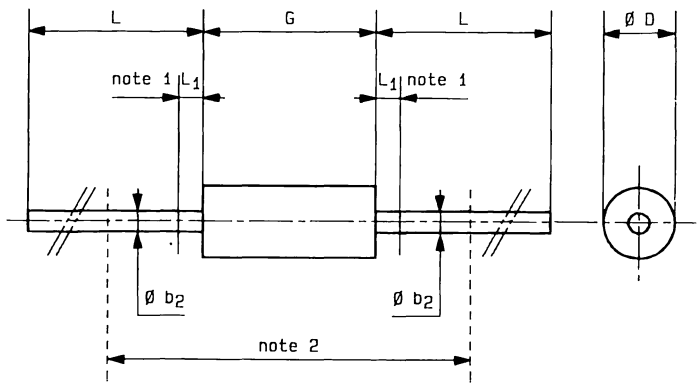


Fig.8b - Capacitance versus reverse applied voltage for bidirectional types (typical values).

D88P7TP5

PACKAGE MECHANICAL DATA

CB-417 Plastic

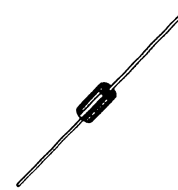


Ref.	Millimeters		Inches		Notes
	Min.	Max.	Min.	Max.	
Ø b_2	–	1.092	–	0.043	1 - The lead diameter Ø b_2 is not controlled over zone L_1. 2 - The minimum axial lengh within which the device may be placed with its leads bent at right angles is 0.59" (15 mm).
Ø D	–	3.683	–	0.145	
G	–	8.89	–	0.350	
L	25.4	–	1.000	–	
L_1	–	1.25	–	0.049	

Cooling method : by convection (method A).
Marking : type number ; white band indicates cathode for unidirectional types.
Weight : 0.6 g.

UNI-AND BIDIRECTIONAL TRANSIENT VOLTAGE SUPPRESSORS

- HIGH SURGE CAPABILITY : 1.5 kW / 1 ms EXPO
- VERY FAST CLAMPING TIME : 1 ps FOR UNIDIRECTIONAL TYPES 5 ns FOR BIDIRECTIONAL TYPES
- LARGE VOLTAGE RANGE : 5.8 V → 376 V
- ORDER CODE : TYPE NUMBER FOR UNIDIRECTIONAL TYPES, TYPE NUMBER + SUFFIX C FOR BIDIRECTIONAL TYPES



CB-429
(Plastic)

DESCRIPTION

Transient voltage suppressor diodes especially useful in protecting integrated circuits, MOS, hybrids and other voltage-sensitive semiconductors and components.

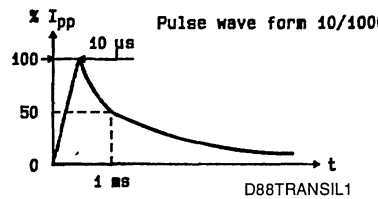
ABSOLUTE RATINGS (limiting values)

Symbol	Parameter		Value	Unit
P_p	Peak Pulse Power for 1 ms Exponential Pulse	T_j Initial = 25 °C See note 1	1.5	kW
P	Power Dissipation on Infinite Heatsink	T_{amb} = 75 °C	5	W
I_{FSM}	Non Repetitive Surge Peak Forward Current for Unidirectional Types	T_j Initial = 25 °C t = 10 ms	250	A
T_{stg} T_j	Storage and Operating Junction Temperature Range		– 65 to 175 175	°C °C
T_L	Maximum Lead Temperature for Soldering During 10 s at 4 mm from Case		230	°C

THERMAL RESISTANCE

Symbol	Parameter	Value	Unit
$R_{th(j-l)}$	Junction-leads on Infinite Heatsink for L_{lead} = 10 mm	20	°C/W

Note : 1. For surges upper than the maximum values, the diode will present a short-circuit anode-cathode.



D88TRANSIL1

ELECTRICAL CHARACTERISTICS (T_j = 25 °C)

Symbol	Parameter		Value
V_{RM}	Stand-off Voltage		See tables
$V_{(BR)}$	Breakdown Voltage		
$V_{(CL)}$	Clamping Voltage		
I_{pp}	Peak Pulse Current		
α_T	Temperature Coefficient of $V_{(BR)}$		
C	Capacitance		
$t_{clamping}$	Clamping Time (0 volt to $V_{(BR)}$)	Unidirectional Types	1 ps max.
		Bidirectional Types	5 ns max.

Types		I_{RM} @ V_{RM} max.		$V_{(BR)}$* @ I_R (V)				$V_{(CL)}$ @ I_{pp} max. 1 ms expo		$V_{(CL)}$ @ I_{pp} max. 8-20 µs expo		α_T max.	C** typ. V_R=0 f=1 MHz
Unidirectional	Bidirectional	(µA)	(V)	min.	nom.	max.	(mA)	(V)	(A)	(V)	(A)	(10^{-4}/°C)	(pF)
P 1 5KE6V8P	P 1.5KE6V8CP	1000§	5.8	6.45	6.8	7.48	10	10.5	143	13.4	746	5.7	9500
1 5KE6V8A	1 5KE6V8CA	1000§	5.8	6 45	6.8	7.14	10	10.5	143	13.4	746	5.7	9500
P 1.5KE7V5P	1.5KE7V5CP	500§	6.4	7.13	7.5	8 25	10	11.3	132	14.5	690	6.1	8500
1.5KE7V5A	1.5KE7V5CA	500§	6.4	7.13	7 5	7.88	10	11.3	132	14.5	690	6 1	8500
1.5KE8V2P	1.5KE8V2CP	200§	7.02	7.79	8.2	9 02	10	12.1	124	15.5	645	6.5	8000
1.5KE8V2A	1.5KE8V2CA	200§	7.02	7.79	8 2	8.61	10	12.1	124	15.5	645	6.5	8000
1.5KE9V1P	1.5KE9V1CP	50§	7.78	8.65	9.1	10	1	13.4	112	17.1	585	6.8	7500
1.5KE9V1A	1.5KE9V1CA	50§	7.78	8.65	9.1	9.55	1	13.4	112	17.1	585	6.8	7500
P 1.5KE10P	1.5KE10CP	10§	8.55	9.5	10	11	1	14.5	103	18.6	968	7.3	7000
1.5KE10A	1.5KE10CA	10§	8.55	9.5	10	10.5	1	14.5	103	18.6	968	7.3	7000
1.5KE11P	1.5KE11CP	5§	9.4	10.5	11	12.1	1	15.6	96	20.3	887	7.5	6400
1.5KE11A	1.5KE11CA	5§	9.4	10.5	11	11.6	1	15.6	96	20.3	887	7.5	6400
P 1.5KE12P	P 1.5KE12CP	5	10.2	11.4	12	13 2	1	16.7	90	21.7	829	7.8	6000
1.5KE12A	1.5KE12CA	5	10.2	11.4	12	12.6	1	16.7	90	21.7	829	7.8	6000
P 1.5KE13P	1.5KE13CP	5	11.1	12 4	13	14.3	1	18.2	82	23 6	763	8.1	5500
1.5KE13A	1.5KE13CA	5	11.1	12.4	13	13.7	1	18.2	82	23.6	763	8 1	5500
1.5KE15P	1.5KE15CP	5	12.8	14.3	15	16.5	1	21.2	71	27.2	662	8.4	5000
1.5KE15A	1.5KE15CA	5	12.8	14.3	15	15.8	1	21.2	71	27.2	662	8.4	5000
P 1.5KE16P	1.5KE16CP	5	13.6	15.2	16	17.6	1	22.5	67	28.9	623	8.6	4700
1.5KE16A	1.5KE16CA	5	13.6	15.2	16	16.8	1	22.5	67	28.9	623	8.6	4700
P 1.5KE18P	P 1.5KE18CP	5	15.3	17.1	18	19.8	1	25.2	59.5	32.5	554	8.8	4300
1.5KE18A	1.5KE18CA	5	15.3	17.1	18	18.9	1	25.2	59.5	32.5	554	8.8	4300
P 1.5KE20P	P 1.5KE20CP	5	17.1	19	20	22	1	27.7	54	36.1	498	9.0	4000
1.5KE20A	1.5KE20CA	5	17.1	19	20	21	1	27.7	54	36.1	498	9.0	4000
P 1.5KE22P	1.5KE22CP	5	18 8	20.9	22	24.2	1	30.6	49	39.3	458	9.2	3700
1.5KE22A	1.5KE22CA	5	18.8	20.9	22	23.1	1	30.6	49	39.3	458	9.2	3700
1.5KE24P	1.5KE24CP	5	20.5	22.8	24	26.4	1	33.2	45	42.8	421	9.4	3500
1.5KE24A	1.5KE24CA	5	20.5	22.8	24	25.2	1	33.2	45	42.8	421	9.4	3500
P 1.5KE27P	1.5KE27CP	5	23.1	25.7	27	29.7	1	37.5	40	48.3	373	9.6	3200
1.5KE27A	1.5KE27CA	5	23.1	25.7	27	28.4	1	37.5	40	48.3	373	9.6	3200
P 1.5KE30P	P 1.5KE30CP	5	25.6	28.5	30	33	1	41.5	36	53.5	336	9.7	2900
1.5KE30A	1.5KE30CA	5	25.6	28.5	30	31.5	1	41.5	36	53.5	336	9.7	2900
P 1.5KE33P	P 1 5KE33CP	5	28.2	31.4	33	36.3	1	45 7	33	59	305	9.8	2700
1.5KE33A	1.5KE33CA	5	28 2	31.4	33	34.7	1	45.7	33	59	305	9.8	2700
P 1.5KE36P	P 1.5KE36CP	5	30.8	34.2	36	39.6	1	49 9	30	64.3	280	9.9	2500
1.5KE36A	1.5KE36CA	5	30.8	34.2	36	37.8	1	49.9	30	64.3	280	9.9	2500
P 1.5KE39P	P 1.5KE39CP	5	33.3	37.1	39	42.9	1	53.9	28	69.7	258	10.0	2400

* Pulse test $t_p \leq 50$ ms $\delta < 2$ %.
** Divide these values by 2 for bidirectional types.
§ For bidirectional types 1.5KE6V8CP → 11CA, I_{RM} must be double that specified for unidirectional types.
For bidirectional types, electrical characteristics apply in both directions.
P : Preferred device.

Types		I_{RM} @ V_{RM} max.		$V_{(BR)}$* @ I_R (V)				$V_{(CL)}$ @ I_{pp} max. 1 ms expo		$V_{(CL)}$ @ I_{pp} max. 8-20 µs expo		α_T max.	C** typ V_R=0 f=1 MHz
Unidirectional	Bidirectional	(µA)	(V)	min.	nom.	max.	(mA)	(V)	(A)	(V)	(A)	(10^{-4}/°C)	(pF)
	1 5KE39A	1.5KE39CA	5	33.3	37.1	39	41	1	53.9	28	69.7	258	10.0	2400
P	1.5KE43P	1.5KE43CP	5	36.8	40.9	43	47.3	1	59.3	25.3	76.8	234	10.1	2200
	1.5KE43A	1.5KE43CA	5	36.8	40.9	43	45.2	1	59 3	25.3	76 8	234	10.1	2200
P	1.5KE47P	P 1.5KE47CP	5	40.2	44.7	47	51.7	1	64.8	23.2	84	214	10.1	2050
	1.5KE47A	1.5KE47CA	5	40.2	44.7	47	49.4	1	64.8	23.2	84	214	10.1	2050
P	1.5KE51P	1.5KE51CP	5	43.6	48.5	51	56.1	1	70 1	21.4	91	198	10.2	1950
	1.5KE51A	1.5KE51CA	5	43.6	48.5	51	53.6	1	70.1	21.4	91	198	10.2	1950
	1.5KE56P	1.5KE56CP	5	47.8	53.2	56	61.6	1	77	19.5	100	180	10.3	1800
	1.5KE56A	1.5KE56CA	5	47.8	53.2	56	58.8	1	77	19.5	100	180	10.3	1800
	1.5KE62P	1.5KE62CP	5	53	58.9	62	68.2	1	85	17.7	111	162	10.4	1700
	1.5KE62A	1.5KE62CA	5	53	58.9	62	65.1	1	85	17.7	111	162	10 4	1700
P	1.5KE68P	P 1.5KE68CP	5	58.1	64.6	68	74.8	1	92	16.3	121	148	10.4	1550
	1.5KE68A	1.5KE68CA	5	58.1	64.6	68	71.4	1	92	16.3	121	148	10.4	1550
	1.5KE75P	1.5KE75CP	5	64.1	71.3	75	82.5	1	103	14.6	134	134	10.5	1450
	1.5KE75A	1.5KE75CA	5	64.1	71.3	75	78.8	1	103	14.6	134	134	10.5	1450
P	1.5KE82P	P 1.5KE82CP	5	70.1	77.9	82	90.2	1	113	13.3	146	123	10.5	1350
	1.5KE82A	1.5KE82CA	5	70.1	77.9	82	86.1	1	113	13.3	146	123	10.5	1350
	1.5KE91P	1.5KE91CP	5	77.8	86.5	91	100	1	125	12	162	111	10.6	1250
	1.5KE91A	1.5KE91CA	5	77 8	86.5	91	95.5	1	125	12	162	111	10.6	1250
	1.5KE100P	1.5KE100CP	5	85.5	95	100	110	1	137	11	178	101	10.6	1150
	1.5KE100A	1.5KE100CA	5	85.5	95	100	105	1	137	11	178	101	10.6	1150
	1.5KE110P	P 1.5KE110CP	5	94	105	110	121	1	152	9.9	195	92	10.7	1050
	1.5KE110A	1.5KE110CA	5	94	105	110	116	1	152	9.9	195	92	10.7	1050
	1.5KE120P	1.5KE120CP	5	102	114	120	132	1	165	9.1	212	85	10.7	1000
	1.5KE120A	1.5KE120CA	5	102	114	120	126	1	165	9.1	212	85	10.7	1000
	1.5KE130P	P 1.5KE130CP	5	111	124	130	143	1	179	8.4	230	78	10.7	950
	1.5KE130A	1.5KE130CA	5	111	124	130	137	1	179	8.4	230	78	10.7	950
	1.5KE150P	1.5KE150CP	5	128	143	150	165	1	207	7.2	265	68	10.8	850
	1.5KE150A	1.5KE150CA	5	128	143	150	158	1	207	7.2	265	68	10.8	850
	1.5KE160P	1.5KE160CP	5	136	152	160	176	1	219	6.8	282	64	10.8	800
	1.5KE160A	1.5KE160CA	5	136	152	160	168	1	219	6.8	282	64	10.8	800
P	1.5KE170P	1.5KE170CP	5	145	161	170	187	1	234	6.4	301	60	10.8	750
	1.5KE170A	1.5KE170CA	5	145	161	170	179	1	234	6.4	301	60	10.8	750
P	1.5KE180P	P 1.5KE180CP	5	154	171	180	198	1	246	6.1	317	57	10.8	725
	1.5KE180A	1.5KE180CA	5	154	171	180	189	1	246	6.1	317	57	10.8	725
P	1.5KE200P	P 1.5KE200CP	5	171	190	200	220	1	274	5.5	353	51	10.8	675
	1.5KE200A	1.5KE200CA	5	171	190	200	210	1	274	5.5	353	51	10.8	675
	1.5KE220P	P 1.5KE220CP	5	188	209	220	242	1	328	4.6	388	46.5	10.8	625
	1.5KE220A	1.5KE220CA	5	188	209	220	231	1	328	4.6	388	46.5	10 8	625
P	1.5KE250P	P 1.5KE250CP	5	213	237	250	275	1	344	5.0	442	47	11	560
	1.5KE250A	1.5KE250CA	5	213	237	250	263	1	344	5.0	442	47	11	560
	1.5KE280P	1.5KE280CP	5	239	266	280	308	1	384	5.0	494	47	11	520
	1.5KE280A	1.5KE280CA	5	239	266	280	294	1	384	5 0	494	47	11	520
P	1.5KE300P	P 1.5KE300CP	5	256	285	300	330	1	414	5.0	529	47	11	500
	1.5KE300A	1.5KE300CA	5	256	285	300	315	1	414	5.0	529	47	11	500
	1.5KE320P	1.5KE320CP	5	273	304	320	352	1	438	4.5	564	42	11	460
	1.5KE320A	1.5KE320CA	5	273	304	320	336	1	438	4.5	564	42	11	460
P	1.5KE350P	P 1.5KE350CP	5	299	332	350	385	1	482	4.0	618	37	11	430
	1.5KE350A	1.5KE350CA	5	299	332	350	368	1	482	4.0	618	37	11	430
P	1.5KE400P	P 1.5KE400CP	5	342	380	400	440	1	548	4.0	706	37	11	390
	1.5KE400A	1.5KE400CA	5	342	380	400	420	1	548	4 0	706	37	11	390
P	1.5KE440P	P 1.5KE440CP	5	376	418	440	484	1	603	3.5	776	33	11	360
	1.5KE440A	1.5KE440CA	5	376	418	440	462	1	603	3.5	776	33	11	360

* Pulse test $t_p \leq 50$ ms $\delta < 2$ %.
** Divide these values by 2 for bidirectional types.
For bidirectional types, electrical characteristics apply in both directions.
P : Preferred device.

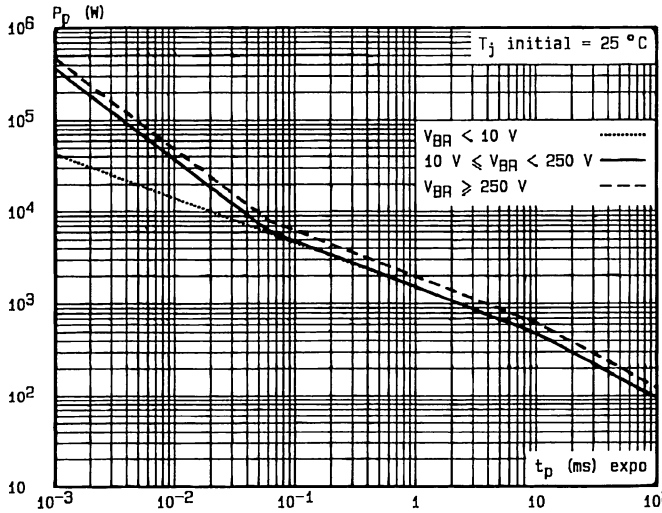


Fig.1 - Peak pulse power versus exponential pulse duration.

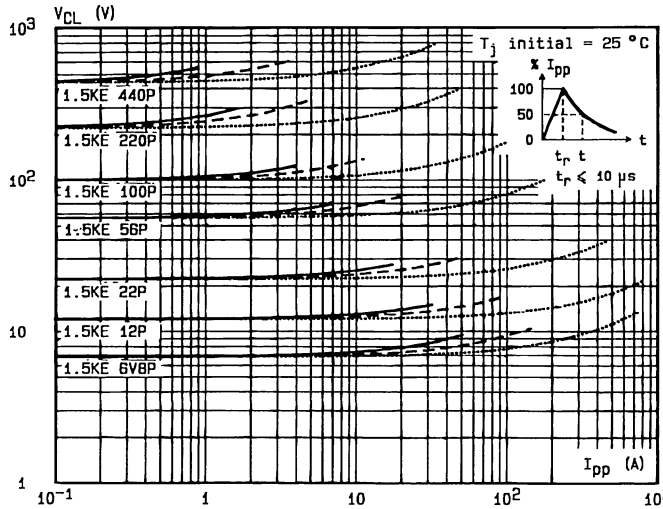


Fig.2 - Clamping voltage versus peak pulse current.
exponential waveform t = 20 µs ·····
t = 1 ms – – –
t = 10 ms ——

Note : The curves of the figure 2 are specified for a junction temperature of 25 °C before surge. The given results may be extrapolated for other junction temperatures by using the following formula : $\Delta V_{(BR)} = \alpha_{T(V(BR))} \times [T_j - 25] \times V_{(BR)}$
For intermediate voltages, extrapolate the given results.

D881.5KEP4

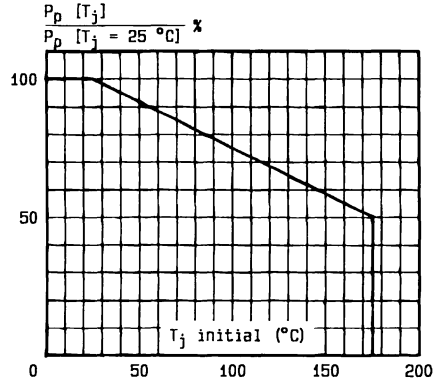


Fig.3 - Allowable power dissipation versus junction temperature.

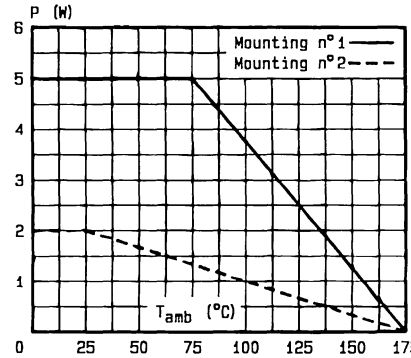


Fig.4 - Power dissipation versus ambient temperature.

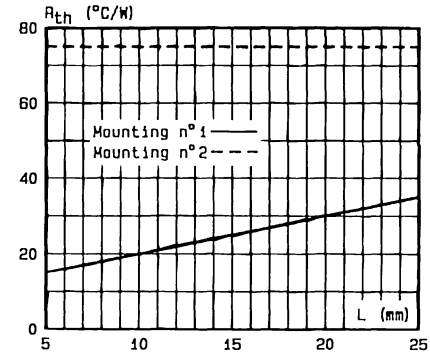


Fig.5 - Thermal resistance versus lead length.

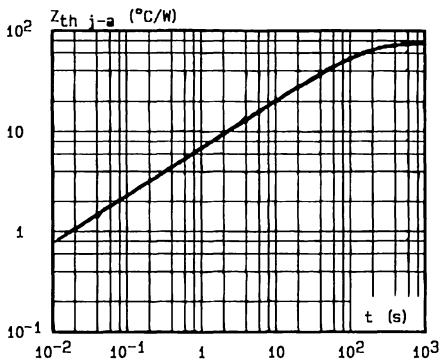
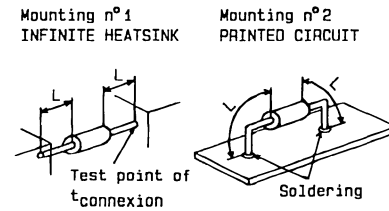


Fig.6 - Transient thermal impedance junction-ambient for mounting n°2 versus pulse duration (L = 10 mm).



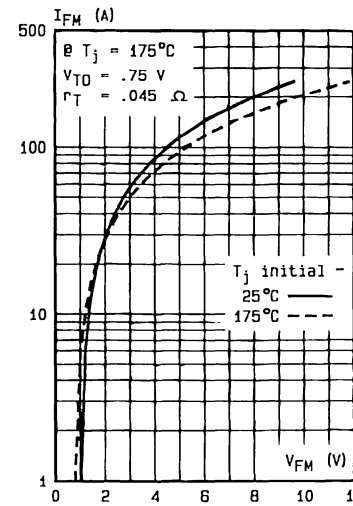


Fig.7 - Peak forward current versus peak forward voltage drop (typical values for unidirectional types).

D881.5KEP5

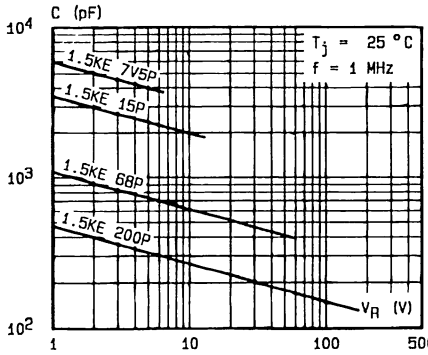


Fig.8a - Capacitance versus reverse applied voltage for unidirectional types (typical values).

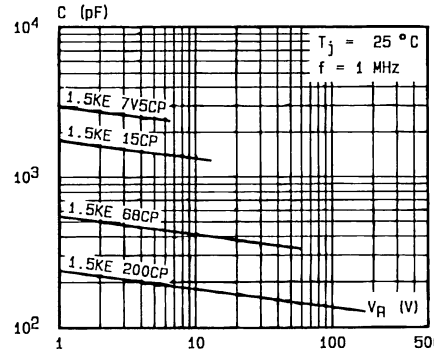
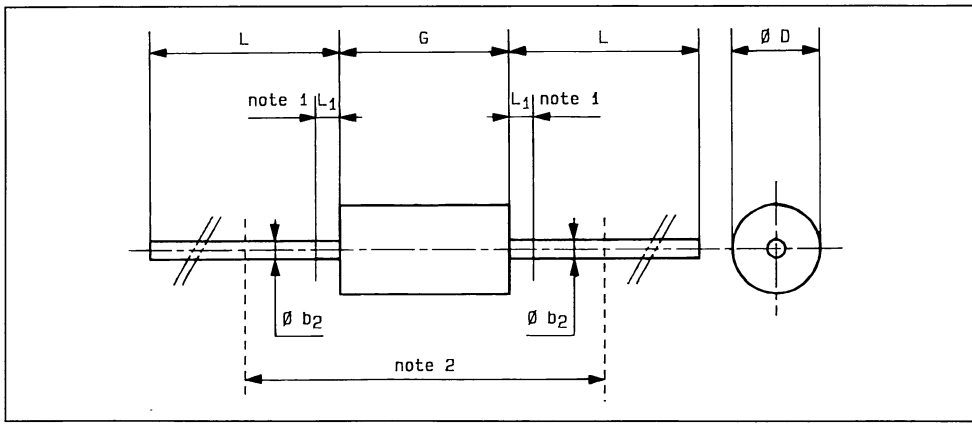


Fig.8b - Capacitance versus reverse applied voltage for bidirectional types (typical values).

D881.5KEP6

PACKAGE MECHANICAL DATA

CB-429 Plastic



Ref.	Millimeters		Inches		Notes
	Min.	Max.	Min.	Max.	
Ø b_2	–	1.06	–	0.042	1 - The lead diameter Ø b_2 is not controlled over zone L_1. 2 - The minimum axial lengh within which the device may be placed with its leads bent at right angles is 0.70" (18 mm).
Ø D	–	5.1	–	0.20	
G	–	9.8	–	0.386	
L	26	–	1.024	–	
L_1	–	1.27	–	0.050	

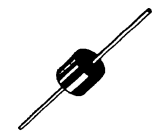
Cooling method : by convection (method A).
Marking : type number ; white band indicates cathode for unidirectional types.
Weight : 0.9 g.

SGS-THOMSON MICROELECTRONICS

BZW50-10,B → 180, B

UNI-AND BIDIRECTIONAL TRANSIENT VOLTAGE SUPPRESSORS

- HIGH SURGE CAPABILITY : 5 kW / 1 ms EXPO
- VERY FAST CLAMPING TIME : 1 ps FOR UNIDIRECTIONAL TYPES 5 ns FOR BIDIRECTIONAL TYPES
- LARGE VOLTAGE RANGE : 10 V → 180 V
- ORDER CODE : TYPE NUMBER FOR UNIDIRECTIONAL TYPES, TYPE NUMBER + SUFFIX B FOR BIDIRECTIONAL TYPES



AG
(Plastic)

DESCRIPTION

Transient voltage suppressor diodes especially useful in protecting integrated circuits, MOS, hybrids and other voltage-sensitive semiconductors and components.

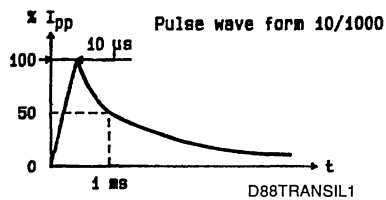
ABSOLUTE RATINGS (limiting values)

Symbol	Parameter		Value	Unit
P_p	Peak Pulse Power for 1 ms Exponential Pulse	T_j Initial = 25 °C See note 1	5	kW
P	Power Dissipation on Infinite Heatsink	T_{amb} = 75 °C	5	W
I_{FSM}	Non Repetitive Surge Peak Forward Current for Unidirectional Types	T_j Initial = 25 °C t = 10 ms	500	A
T_{stg} T_j	Storage and Operating Junction Temperature Range		– 65 to 150 150	°C °C
T_L	Maximum Lead Temperature for Soldering During 10 s at 4 mm from Case		230	°C

THERMAL RESISTANCE

Symbol	Parameter	Value	Unit
$R_{th(j-l)}$	Junction-leads on Infinite Heatsink for L_{lead} = 10 mm	15	°C/W

Note : 1. For surges upper than the maximum values, the diode will present a short-circuit anode-cathode.



ELECTRICAL CHARACTERISTICS (T_j = 25 °C)

Symbol	Parameter		Value
V_{RM}	Stand-off Voltage		See tables
$V_{(BR)}$	Breakdown Voltage		
$V_{(CL)}$	Clamping Voltage		
I_{pp}	Peak Pulse Current		
α_T	Temperature Coefficient of $V_{(BR)}$		
C	Capacitance		
$t_{clamping}$	Clamping Time (0 volt to $V_{(BR)}$)	Unidirectional Types	1 ps max.
		Bidirectional Types	5 ns max.

Types		I_{RM} @ V_{RM} max.		$V_{(BR)}$* @ I_R (V)				$V_{(CL)}$ @ I_{pp} max. 1 ms expo		$V_{(CL)}$ @ I_{pp} max. 8-20 µs expo		α_T max.	C** typ. V_R=0 f=1 MHz
Unidirectional	Bidirectional	(µA)	(V)	min.	nom.	max.	(mA)	(V)	(A)	(V)	(A)	(10^{-4}/°C)	(pF)
BZW50-10	BZW50-10B	5	10	11.1	12.4	13.6	1	18.8	266	23.4	2564	7.8	24000
BZW50-12	BZW50-12B	5	12	13.3	14.8	16.3	1	22	227	28	2143	8 4	18500
BZW50-15	BZW50-15B	5	15	16.6	18.5	20.4	1	26.9	186	35	1714	8.8	13500
BZW50-18	BZW50-18B	5	18	20	22.2	24.4	1	32.2	155	41.5	1446	9.2	11500
BZW50-22	BZW50-22B	5	22	24.4	27.1	29.8	1	39.4	127	51	1177	9.6	8500
BZW50-27	BZW50-27B	5	27	30	33.3	36.6	1	48.3	103	62	968	9.8	7000
BZW50-33	BZW50-33B	5	33	36.6	40.7	44.7	1	59	85	76	789	10	5750
BZW50-39	BZW50-39B	5	39	43.3	48.1	53	1	69.4	72	90	667	10.1	4800
BZW50-47	BZW50-47B	5	47	52	57.8	63.6	1	83.2	60.1	108	556	10.3	4100
BZW50-56	BZW50-56B	5	56	62.2	69.1	76	1	99.6	50	129	465	10.4	3400
BZW50-68	BZW50-68B	5	68	75.6	84	92.4	1	121	41	157	382	10.5	3000
BZW50-82	BZW50-82B	5	82	91	101.2	111	1	145	34	189	317	10.6	2600
BZW50-100	BZW50-100B	5	100	111	123.5	136	1	179	28	228	263	10.7	2300
BZW50-120	BZW50-120B	5	120	133	148.1	163	1	215	23	274	219	10.8	1900
BZW50-150	BZW50-150B	5	150	166	185.2	204	1	269	19	343	175	10.8	1700
BZW50-180	BZW50-180B	5	180	200	222	244	1	322	16	410	146	10.8	1500

* Pulse test $t_p \leq 50$ ms $\delta < 2$ %.
** Divide these values by 2 for bidirectional types.
For bidirectional types, electrical characteristics apply in both directions.

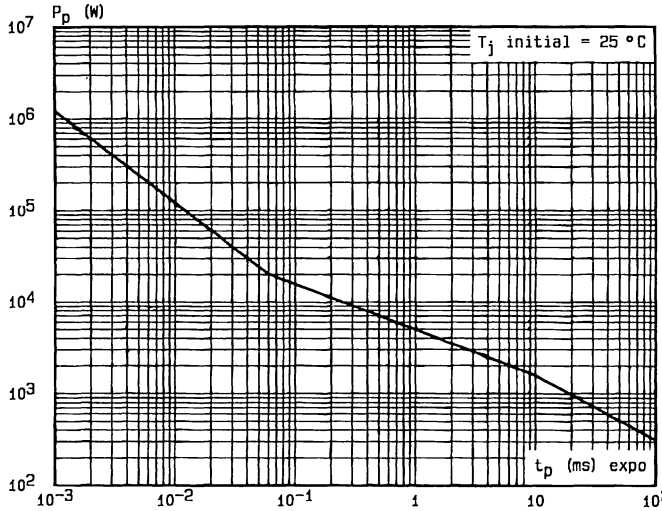


Fig.1 - Peak pulse power versus exponential pulse duration.

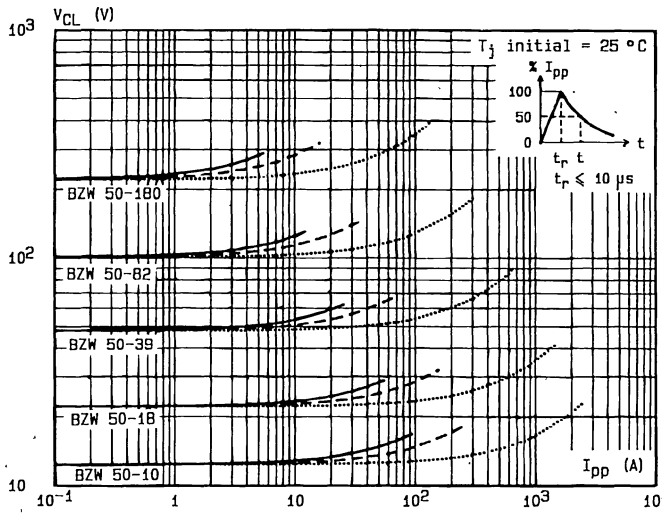


Fig.2 - Clamping voltage versus peak pulse current.
exponential waveform t = 20 µs ·
t = 1 ms - - - -
t = 10 ms ———

Note : The curves of the figure 2 are specified for a junction temperature of 25 °C before surge. The given results may be extrapolated for other junction temperatures by using the following formula : $\Delta V_{(BR)} = \alpha_{T(V(BR))} \times [T_j - 25] \times V_{(BR)}$
For intermediate voltages, extrapolate the given results.

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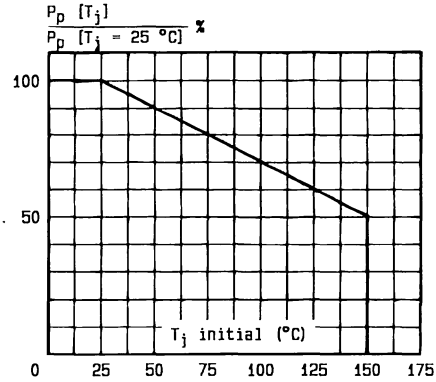


Fig.3 - Allowable power dissipation versus junction temperature.

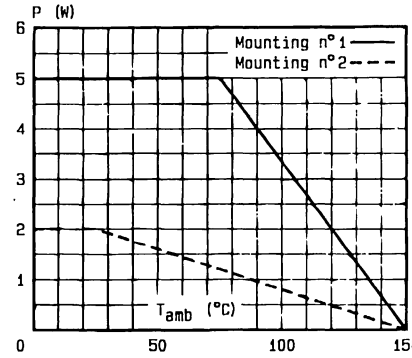


Fig.4 - Power dissipation versus ambient temperature.

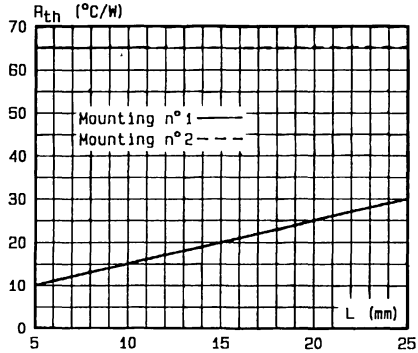
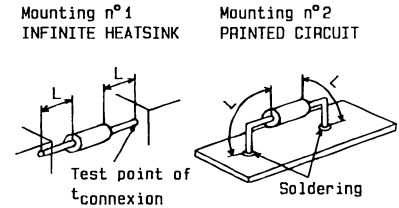


Fig.5 - Thermal resistance versus lead length.



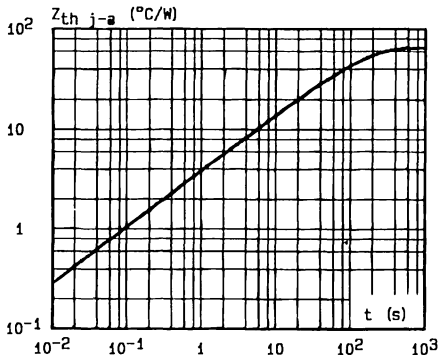


Fig.6 - Transient thermal impedance junction-ambient for mounting n°2 versus pulse duration (L = 10 mm).

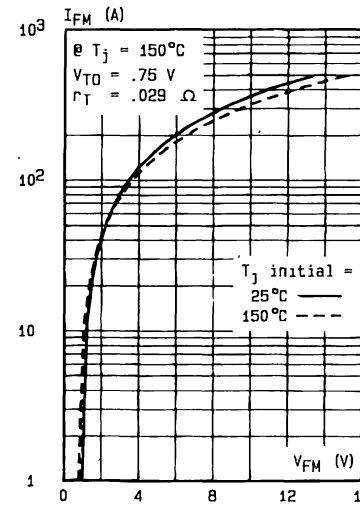


Fig.7 - Peak forward current versus peak forward voltage drop (typical values for unidirectional types).

D88BZW50P4

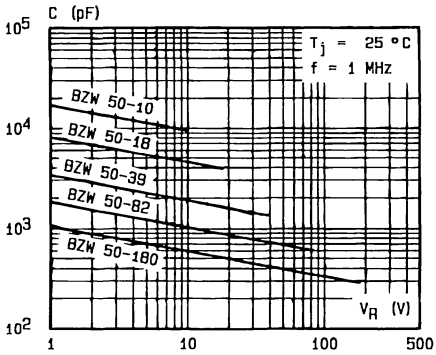


Fig.8a - Capacitance versus reverse applied voltage for unidirectional types (typical values).

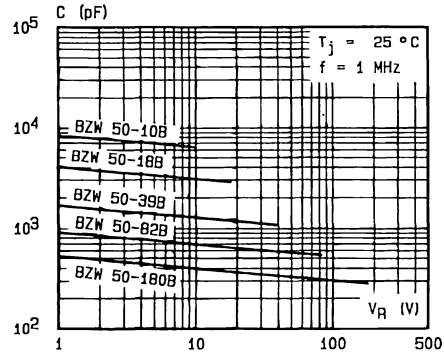
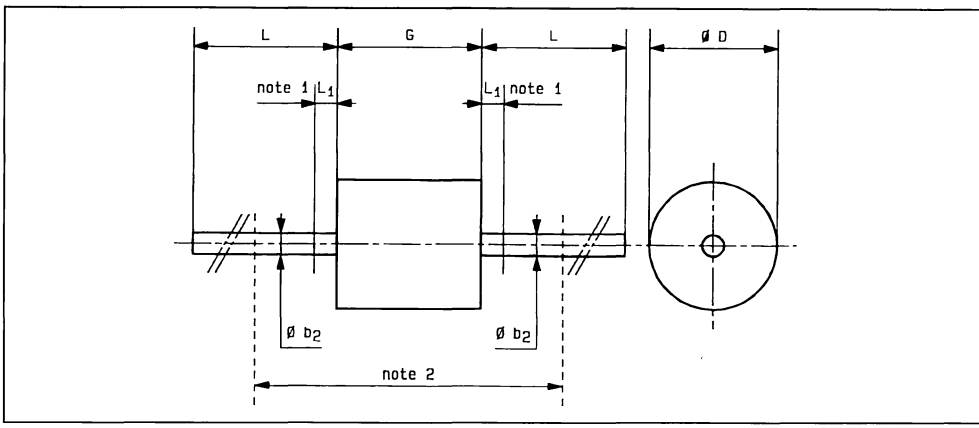


Fig.8b - Capacitance versus reverse applied voltage for bidirectional types (typical values).

D88BZW50P5

PACKAGE MECHANICAL DATA

AG Plastic



Ref.	Millimeters		Inches		Notes
	Min.	Max.	Min.	Max.	
Ø b_2	1.35	1.45	0.053	0.057	1 - The lead diameter Ø b_2 is not controlled over zone L_1. 2 - The minimum axial lengh within which the device may be placed with its leads bent at right angles is 0.79" (20 mm).
Ø D	–	8	–	0.315	
G	–	9	–	0.354	
L	20	–	0.787	–	
L_1	–	1.27	–	0.050	

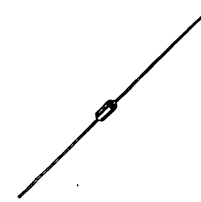
Cooling method : by convection (method A).
Marking : type number ; white band indicates cathode for unidirectional types.
Weight : 1 g.

SGS-THOMSON MICROELECTRONICS

TPA SERIES

TRISIL

- BIDIRECTIONAL DEVICE USED TO **TELEPHONE PROTECTION**
- CHARACTERISTIC OF STAND-OFF AND BREAKDOWN VOLTAGE SIMILAR TO A TRANSIL (V_{off})
- HIGH FLOWOUT CAPABILITY BECAUSE OF ITS BREAKOVER CHARACTERISTIC (V_{on})



F 126
(Plastic)

ABSOLUTE RATINGS (limiting values) (T_j = 25 °C - L = 10 mm)

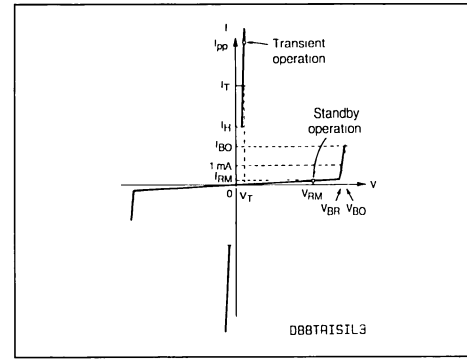
Symbol	Parameter		Value	Unit
P	Power Dissipation on Infinite Heatsink	T_{amb} = 50 °C	1.7	W
I_{pp}	Peak Pulse Current	1 ms expo	50	A
		8-20 µs expo	100	
I_{TSM}	Non Repetitive Surge Peak on-state Current	t_p = 20 ms	30	A
di/dt	Critical Rate of Rise of on-state Current	Non Repetitive	100	A/µs
dv/dt	Critical Rate of Rise of off-state Voltage	67 % $V_{(BR)}$ min	5	kV/µs
T_{stg} T_j	Storage and Operating Junction Temperature Range		– 40 to 150 150	°C °C
T_L	Maximum Lead Temperature for Soldering During 10 s at 4 mm from Case		230	°C

THERMAL RESISTANCES

Symbol	Parameter		Value	Unit
$R_{th(j-l)}$	Junction-leads on Infinite Heatsink	L = 10 mm	60	°C/W
$R_{th(j-a)}$	Junction-ambient on Printed Circuit		100	°C/W

ELECTRICAL CHARACTERISTICS
(T_j = 25 °C)

Symbol	Parameter
V_{RM}	Stand-off Voltage
V_{BR}	Breakdown Voltage
V_{BO}	Clamping Voltage
I_H	Holding Current
V_T	On-state Voltage : 2.5 V typ. @ I_T = 1 A (t_p = 300 µs)



Types	I_{RM} @ V_{RM} max.		$V_{(BR)}$ @ I_R min.		V_{BO} max.	I_{BO} max.	I_H min.
	(µA)	(V)	(V)	(mA)	(V)	(mA)	(mA)
TPA62A - 12 or 18	2	56	62	1	82	800	
(1) TPA62B - 12 or 18	2	56	62	1	75	800	
TPA68A - 12 or 18	2	61	68	1	90	800	
(1) TPA68B - 12 or 18	2	61	68	1	82	800	
(1) TPA75A - 12 or 18	2	67	75	1	100	800	
(1) TPA75B - 12 or 18	2	67	75	1	91	800	
(1) TPA82A - 12 or 18	2	74	82	1	109	300	
(1) TPA82B - 12 or 18	2	74	82	1	99	300	
(1) TPA91A - 12 or 18	2	82	91	1	121	300	
(1) TPA91B - 12 or 18	2	82	91	1	110	300	
P TPA100A - 12 or 18	2	90	100	1	133	300	12 Suffix for 120 mA
TPA100B - 12 or 18	2	90	100	1	121	300	
TPA110A - 12 or 18	2	99	110	1	147	300	
TPA110B - 12 or 18	2	99	110	1	133	300	
P TPA120A - 12 or 18	2	108	120	1	160	300	
TPA120B - 12 or 18	2	108	120	1	145	300	
P TPA130A - 12 or 18	2	117	130	1	173	300	
TPA130B - 12 or 18	2	117	130	1	157	300	
(1) TPA150A - 12 or 18	2	135	150	1	200	300	
(1) TPA150B - 12 or 18	2	135	150	1	181	300	18 Suffix for 180 mA
(1) TPA160A - 12 or 18	2	144	160	1	213	300	
(1) TPA160B - 12 or 18	2	144	160	1	193	300	
(1) TPA180A - 12 or 18	2	162	180	1	240	300	
(1) TPA180B - 12 or 18	2	162	180	1	217	300	
(1) TPA200A - 12 or 18	2	180	200	1	267	300	
(1) TPA200B - 12 or 18	2	180	200	1	241	300	
P TPA220A - 12 or 18	2	198	220	1	293	300	
TPA220B - 12 or 18	2	198	220	1	265	300	
P TPA240A - 12 or 18	2	216	240	1	320	300	
TPA240B - 12 or 18	2	216	240	1	289	300	
P TPA270A - 12 or 18	2	243	270	1	360	300	
TPA270B - 12 or 18	2	243	270	1	325	300	

P : Preferred device.
(1) : These volages are on request. Consult us.

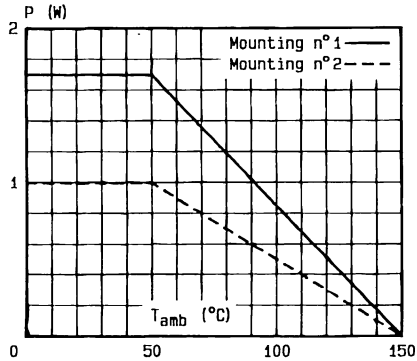


Fig.1 - Power dissipation versus ambient temperature.

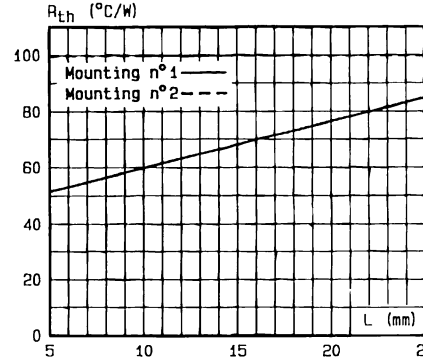


Fig.2 - Thermal resistance versus lead length.

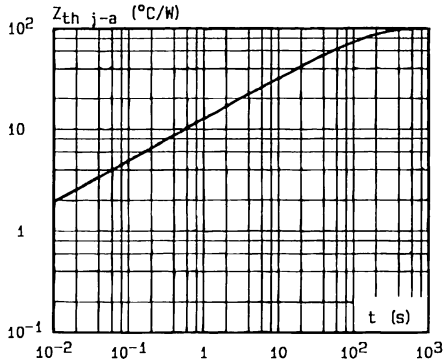
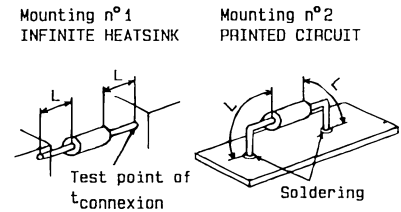


Fig.3 - Transient thermal impedance junction-ambient for mounting n°2 versus pulse duration (L = 10 mm).



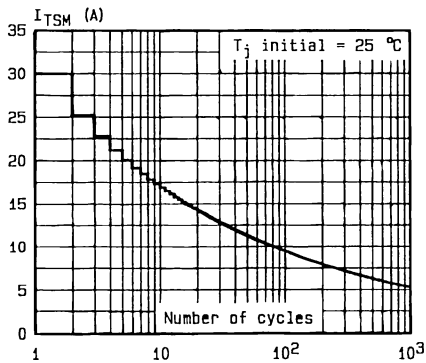


Fig.4 - Non repetitive surge peak on-state current versus number of cycles.

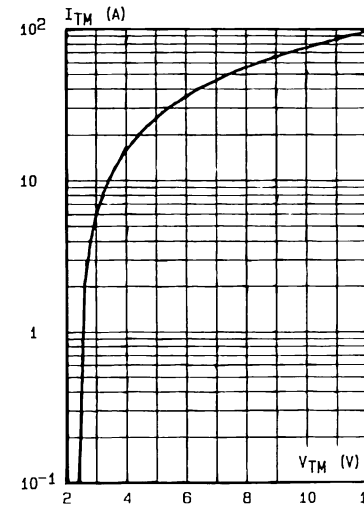


Fig.5 - Peak forward current versus peak forward voltage drop (typical values).

DBBTPAP3

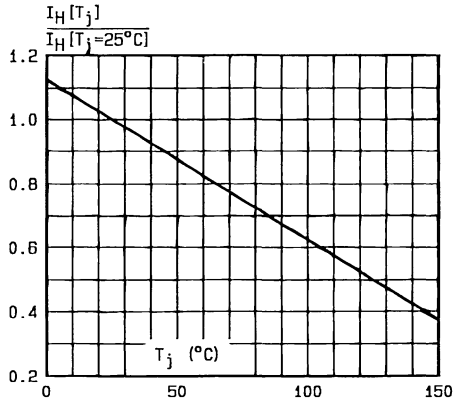


Fig.6 - Relative variation of holding current versus junction temperature.

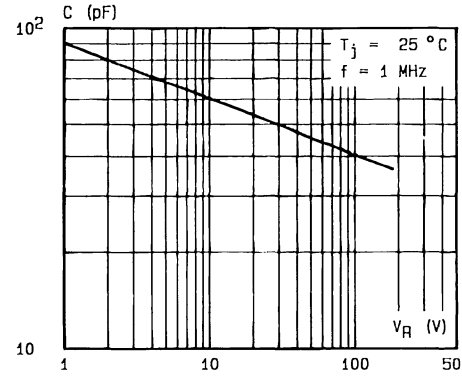
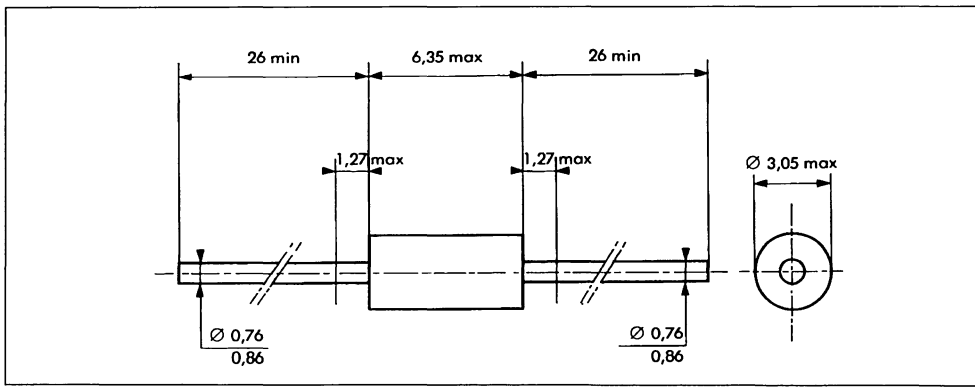


Fig.7 - Capacitance versus reverse applied voltage.

DB8TPAP4

PACKAGE MECHANICAL DATA

F 126 Plastic



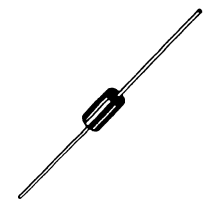
Cooling method : by conduction (method A)
Marking · type number
Weight · 0 4 g

SGS-THOMSON MICROELECTRONICS

TPB SERIES

TRISIL

- BIDIRECTIONAL DEVICE USED TO **TELEPHONE PROTECTION**
- CHARACTERISTIC OF STAND-OFF AND BREAKDOWN VOLTAGE SIMILAR TO A TRANSIL (V_{off})
- HIGH FLOWOUT CAPABILITY BECAUSE OF ITS BREAKOVER CHARACTERISTIC (V_{on})



CB 429
(Plastic)

ABSOLUTE RATINGS (limiting values) (T_{amb} = 25 °C - L = 10 mm)

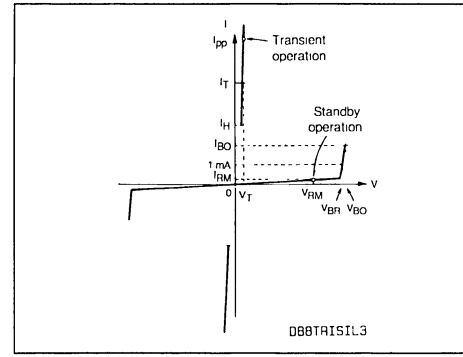
Symbol	Parameter		Value	Unit
P	Power Dissipation on Infinite Heatsink	T_{amb} = 50 °C	5	W
I_{pp}	Peak Pulse Current	1 ms expo	100	A
		8-20 µs expo*	150	
I_{TSM}	Non Repetitive Surge Peak on-state Current	t_p = 20 ms	50	A
di/dt	Critical Rate of Rise of on-state Current	Non Repetitive	100	A/µs
dv/dt	Critical Rate of Rise of off-state Voltage	67 % $V_{(BR)}$ min	5	kV/µs
T_{stg} T_j	Storage and Operating Junction Temperature Range		– 40 to 150 150	°C °C
T_L	Maximum Lead Temperature for Soldering During 10 s at 4 mm from Case		230	°C

THERMAL RESISTANCES

Symbol	Parameter		Value	Unit
$R_{th(j-l)}$	Junction-leads on Infinite Heatsink	L = 10 mm	20	°C/W
$R_{th(j-a)}$	Junction-ambient on Printed Circuit		75	°C/W

ELECTRICAL CHARACTERISTICS
(T_j = 25 °C)

Symbol	Parameter
V_{RM}	Stand-off Voltage
V_{BR}	Breakdown Voltage
V_{BO}	Clamping Voltage
I_H	Holding Current
V_T	On-state Voltage : 1.6 V typ. @ I_T = 1 A (t_p = 300 µs)



Types	I_{RM} @ V_{RM} max.		$V_{(BR)}$ @ I_R min.		V_{BO} max.	I_{BO} max.	I_H min.
	(µA)	(V)	(V)	(mA)	(V)	(mA)	(mA)
TPB62A - 12 or 18	2	56	62	1	82	800	
(1) TPB62B - 12 or 18	2	56	62	1	75	800	
TPB68A - 12 or 18	2	61	68	1	90	800	
(1) TPB68B - 12 or 18	2	61	68	1	82	800	
(1) TPB75A - 12 or 18	2	67	75	1	100	800	
(1) TPB75B - 12 or 18	2	67	75	1	91	800	
(1) TPB82A - 12 or 18	2	74	82	1	109	300	
(1) TPB82B - 12 or 18	2	74	82	1	99	300	
(1) TPB91A - 12 or 18	2	82	91	1	121	300	
(1) TPB91B - 12 or 18	2	82	91	1	110	300	
P TPB100A - 12 or 18	2	90	100	1	133	300	12 Suffix for 120 mA
TPB100B - 12 or 18	2	90	100	1	121	300	
TPB110A - 12 or 18	2	99	110	1	147	300	
TPB110B - 12 or 18	2	99	110	1	133	300	
P TPB120A - 12 or 18	2	108	120	1	160	300	
TPB120B - 12 or 18	2	108	120	1	145	300	
P TPB130A - 12 or 18	2	117	130	1	173	300	
TPB130B - 12 or 18	2	117	130	1	157	300	
(1) TPB150A - 12 or 18	2	135	150	1	200	300	
(1) TPB150B - 12 or 18	2	135	150	1	181	300	
(1) TPB160A - 12 or 18	2	144	160	1	213	300	18 Suffix for 180 mA
(1) TPB160B - 12 or 18	2	144	160	1	193	300	
(1) TPB180A - 12 or 18	2	162	180	1	240	300	
(1) TPB180B - 12 or 18	2	162	180	1	217	300	
(1) TPB200A - 12 or 18	2	180	200	1	267	300	
(1) TPB200B - 12 or 18	2	180	200	1	241	300	
P TPB220A - 12 or 18	2	198	220	1	293	300	
TPB220B - 12 or 18	2	198	220	1	265	300	
P TPB240A - 12 or 18	2	216	240	1	320	300	
TPB240B - 12 or 18	2	216	240	1	289	300	
P TPB270A - 12 or 18	2	243	270	1	360	300	
TPB270B - 12 or 18	2	243	270	1	325	300	

P : Preferred device.
(1) : These voltages are on request Consult us.

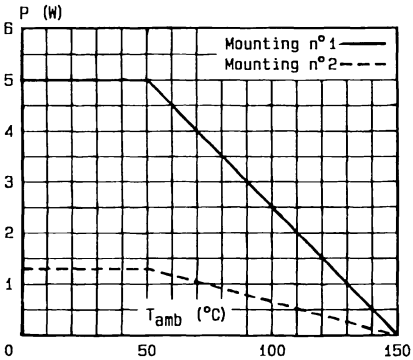


Fig.1 - Power dissipation versus ambient temperature.

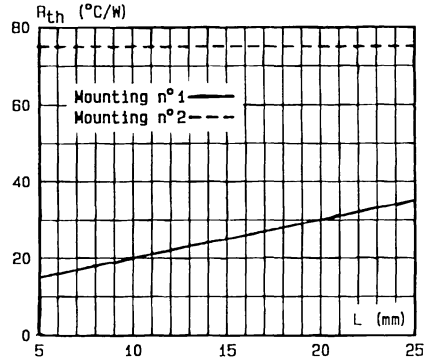


Fig.2 - Thermal resistance versus lead length.

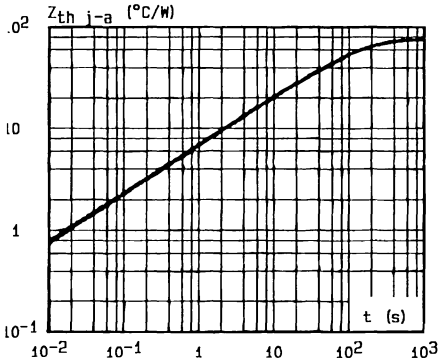
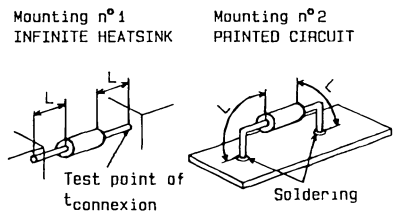


Fig.3 - Transient thermal impedance junction-ambient for mounting n°2 versus pulse duration (L = 10 mm).



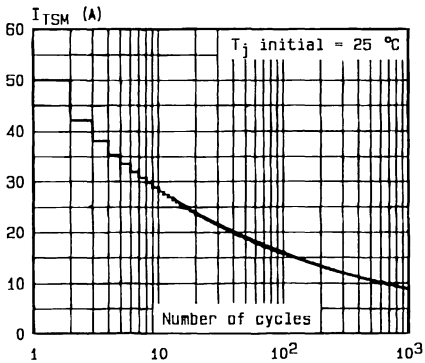


Fig.4 - Non repetitive surge peak on-state current versus number of cycles.

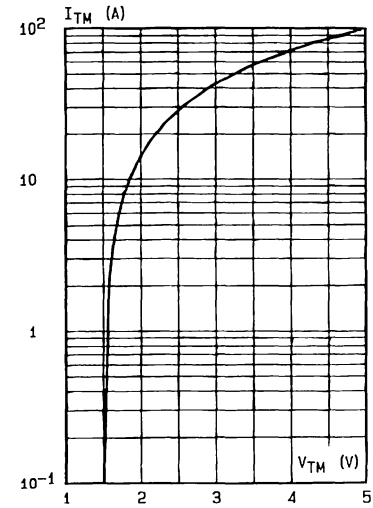


Fig.5 - Peak forward current versus peak forward voltage drop (typical values).

D88TPBP3

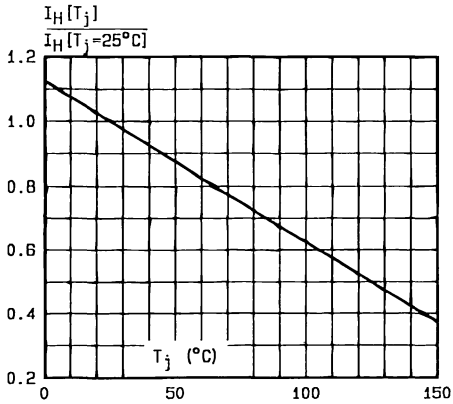


Fig.6 - Relative variation of holding current versus junction temperature

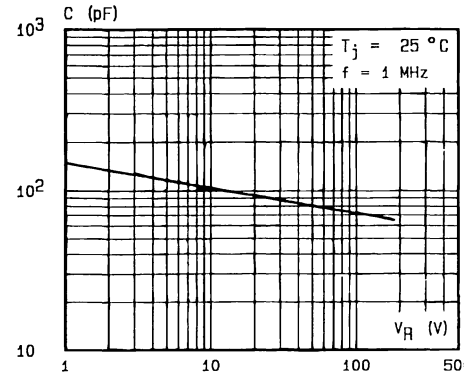
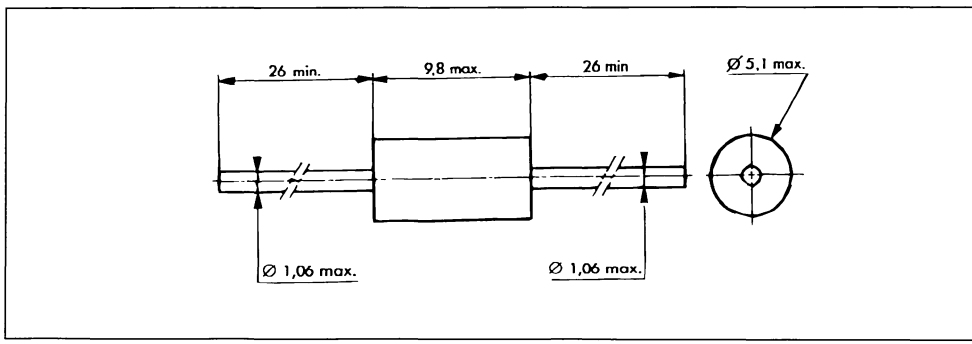


Fig.7 - Capacitance versus reverse applied voltage.

DBBTPBP4

PACKAGE MECHANICAL DATA

CB 429 Plastic



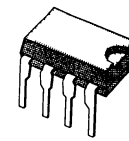
Cooling method : by conduction (method A)
Marking : type number
Weight : 0.9 g

SGS-THOMSON MICROELECTRONICS

LS5018B/LS5060B LS5120B/LS5120B1

BIDIRECTIONAL TRISIL

- CHARACTERISTIC OF STAND-OFF AND BREAKDOWN VOLTAGE SIMILAR TO A TRANSIL (V_{off})
- HIGH FLOWOUT CAPABILITY BECAUSE OF ITS BREAKOVER CHARACTERISTICS (V_{on})
- AUTOMATIC RECOVERY AFTER SURGE



Minidip
(Plastic)

DESCRIPTION

The LS5018B, LS5060B and LS5120B/B1 are bidirectional transient overvoltage suppressor designed to protect sensitive components in electronic telephones and telecommunication equipments against transient caused by lightning, induction from power lines, etc.

ABSOLUTE RATINGS (limiting values) (T_j = 25 °C)

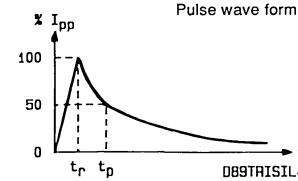
Symbol	Parameter		Value	Unit
I_{pp}	Peak Pulse Current	1 ms expo	100	A
		8-20 µs expo*	500	
I_{TSM}	Non Repetitive Surge Peak on-state Current	t_p = 20 ms – Sinus	50	A
di/dt	Critical Rate of Rise of on-state Current	Non repetitive	100	A/µs
T_{stg} T_j	Storage and Junction Temperature Range		– 40 to 150 150	°C °C

THERMAL RESISTANCE

Symbol	Parameter	Value	Unit
$R_{th(j-a)}$	Junction to Ambient	80	°C/W

* ANSI STD C62.

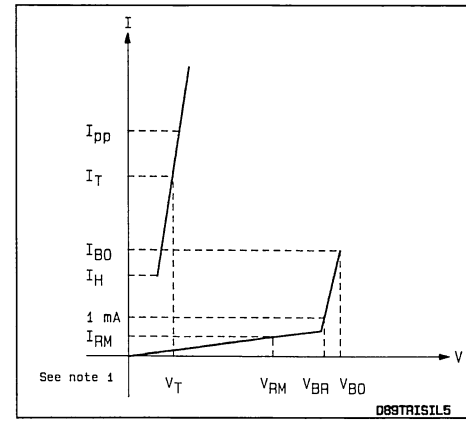
Pulse wave form



ELECTRICAL CHARACTERISTICS

(T_j = 25 °C)

Symbol	Parameter
V_{RM}	Stand-off Voltage
V_{BR}	Breakdown Voltage
V_{BO}	Clamping Voltage
I_H	Holding Current
V_T	On-state Voltage @ I_T
I_{BO}	Breakover Current
I_{pp}	Peak-pulse Current

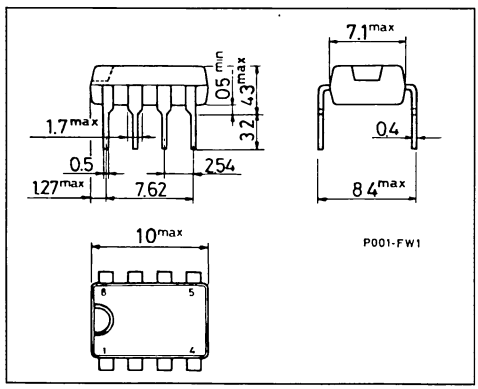


Type	I_{RM} @ V_{RM} max.		$V_{(BR)}$ @ I_R min.		V_{BO} @ max.	min.	I_{BO} typ.	max. See note 2	I_H min.	V_T typ. I_T = 1 A	C max. V_R = 5 V F = 1 MHz
	(µA)	(V)	(V)	(mA)	(V)	(mA)	(mA)	(mA)	(mA)	(V)	(pF)
LS5018B	5	16	17	1	22		1300		200	2	150
LS5060B	10	50	60	1	85		1000		200	2	150
LS5120B	20	100	120	1	180	500		1250	250	2	150
LS5120B1	20	100	120	1	180	500		1250	200	2	150

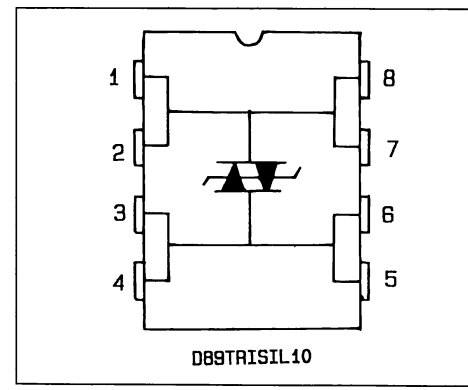
Notes : 1. Same characteristic both sides.
2. These devices are not designed to function as zeners ; continuous operation between 1 mA and I_{BO} will damage them.

PACKAGE MECHANICAL DATA

MINIDIP Plastic



CONNECTION DIAGRAM



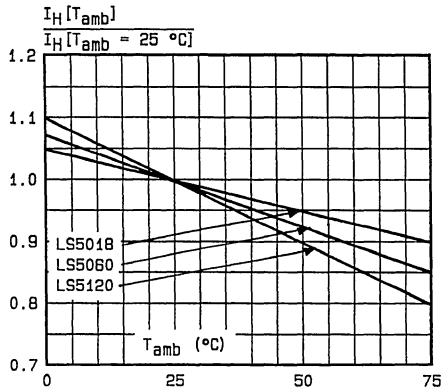


Fig.1 - Relative variation of holding current versus ambient temperature.

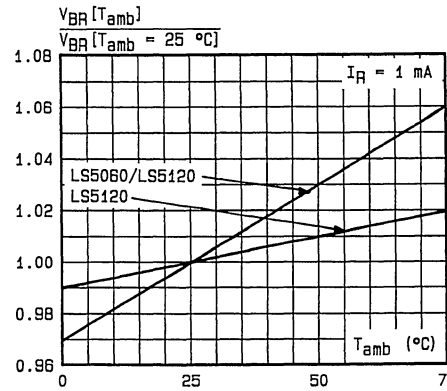


Fig.2 - Relative variation of breakdown voltage versus ambient temperature.

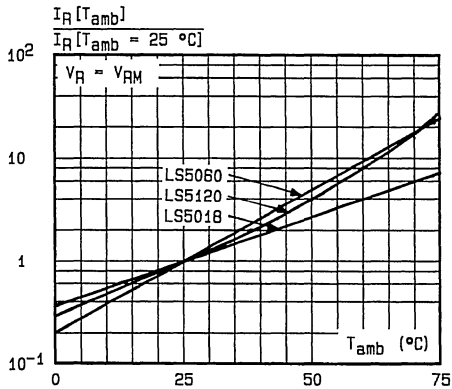


Fig.3 - Relative variation of leakage current versus ambient temperature.

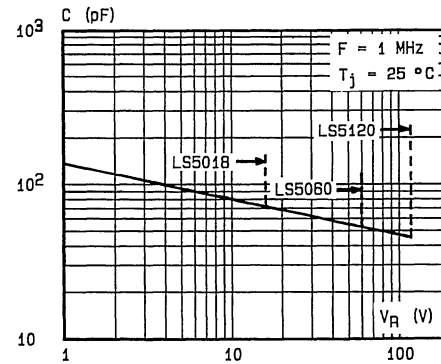


Fig.4 - Junction capacitance versus reverse applied voltage.

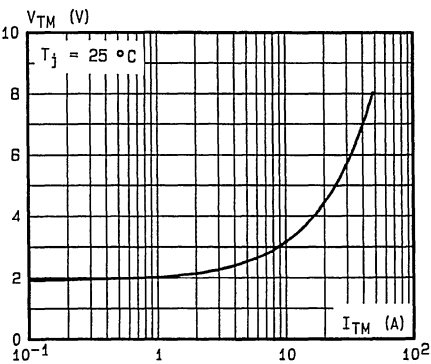


Fig.5 - On-state voltage versus on-state current (typical values).

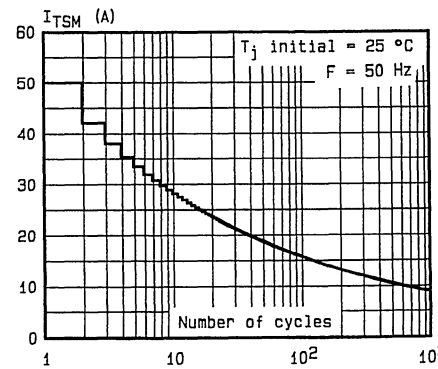


Fig.6 - Non repetitive surge peak on-state current versus number of cycles.

SGS-THOMSON MICROELECTRONICS

THBT 200 D

TRISIL

DESCRIPTION

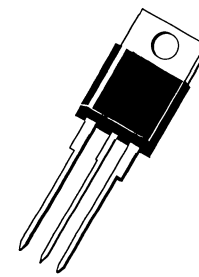
This protection device has been especially designed for subscriber line-card and terminal protection. By itself, it enables to protect integrated SLIC against transient overvoltages. A diode clips positive overloads and breakover device negative overloads.

Its ion-implanted technology confers excellent electrical characteristics on it.

This is why this THBT 200 D easily corresponds to the main protection standard norms which are related to the overvoltages on subscribers lines.

IN ACCORDANCE WITH FOLLOWING STANDARDS :

CCITT K17 - K20	10/700 µs	1.5 kV
	5/310 µs	38 A
VDE 0433	10/700 µs	2 kV
	5/200 µs	50 A
CNET	0.5/700 µs	1.5 kV
	0.2/310 µs	38 A



TO 220 AB
(Plastic)

ABSOLUTE RATINGS (limiting values) (T_j = 25 °C)

Symbol	Parameter		Value	Unit
I_{pp}	Peak Pulse Current	1 ms expo	75	A
		8-20 µs expo*	150	
I_{TSM}	Non Repetitive Surge Peak on-state Current	t_p = 20 ms	30	A
di/dt	Critical Rate of Rise of on-state Current	Non Repetitive	100	A/µs
T_{stg} T_j	Storage and Operating Junction Temperature Range		– 40 to 150 150	°C °C
T_L	Maximum Lead Temperature for Soldering During 10 s at 4 mm from Case		230	°C

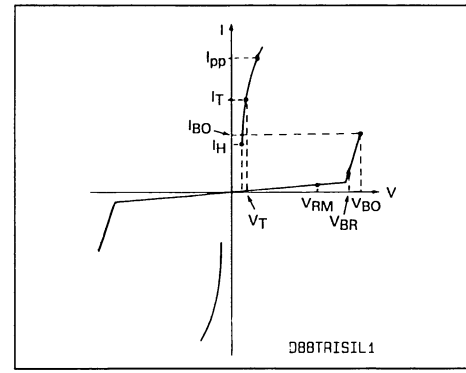
* ANSI STD C62.

THERMAL RESISTANCES

Symbol	Parameter	Value	Unit
$R_{th(j-c)}$	Junction to Case for DC	5	°C/W
$R_{th(j-a)}$	Junction to Ambient	60	°C/W

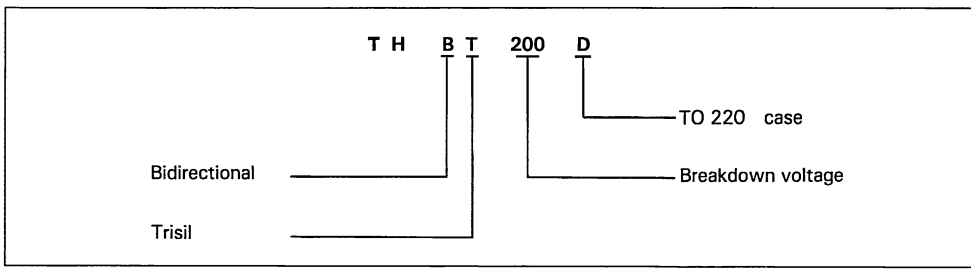
ELECTRICAL CHARACTERISTICS

Symbol	Parameter
V_{RM}	Stand-off Voltage
V_{BR}	Breakdown Voltage
V_{BO}	Clamping Voltage
I_H	Holding Current
V_T	On-state Voltage
I_{BO}	Breakover Current
I_{pp}	Peak-pulse Current



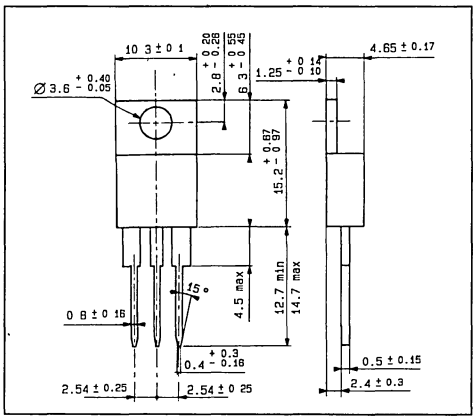
Symbol	Test Conditions			Min.	Typ.	Max.	Unit
I_{RM}	T_j = 25 °C	V_{RM} = 180 V				10	µA
V_{BR}	T_j = 25 °C	I_R = 1 mA		200			V
V_{BO}	T_j = 25 °C	t_p = 100 µs				290	V
I_{BO}	T_j = 25 °C	t_p = 100 µs		150		800	mA
I_H	T_j = 25 °C	I_T = 2 A		150			mA
V_T	T_j = 25 °C	I_T = 5 A	t_p = 100 µs			3	V
α_T					20		10^{-4}/°C
C	T_j = 25 °C	F = 1 MHz	V_R = 5 V			200	pF
dv/dt	T_j = 25 °C	Exponential Ramp 67 % V_{BR}		5000			V/µs

ORDER CODE

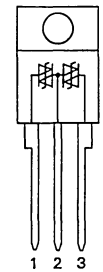


PACKAGE MECHANICAL DATA

TO 220 AB Plastic



PIN CONNECTIONS

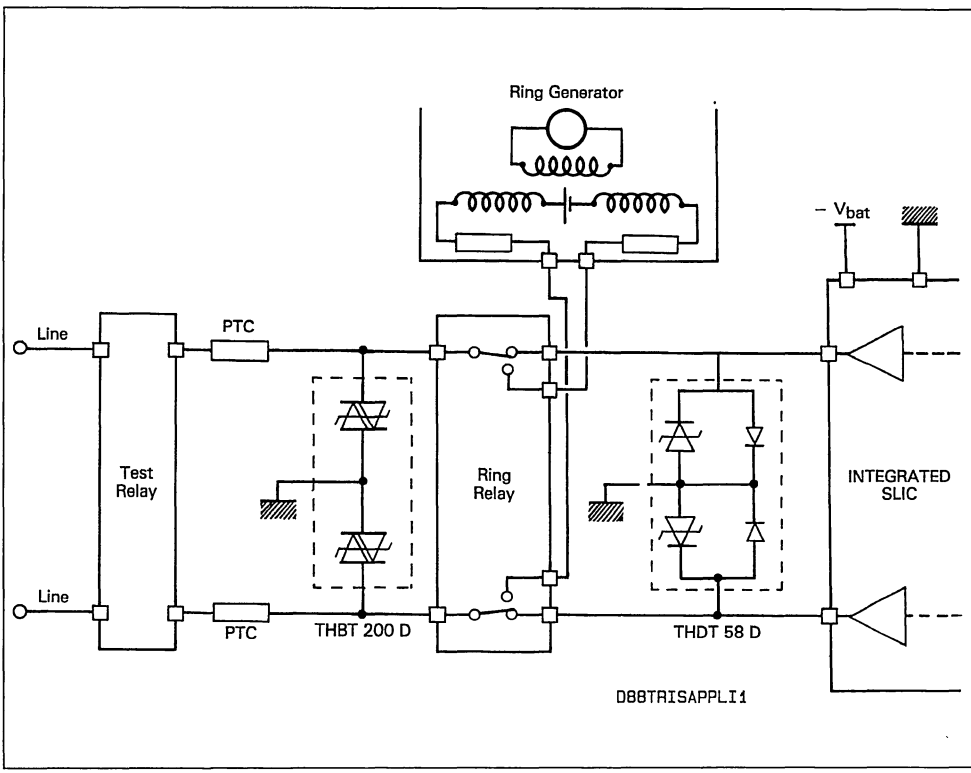


* 1 = Tip or Ring
* 2 = GROUND
* 3 = Tip or Ring

Tab is connected to center pin.

Cooling method : by conduction (Method C)
Marking : type number
Weight : 2 g.

APPLICATION CIRCUIT



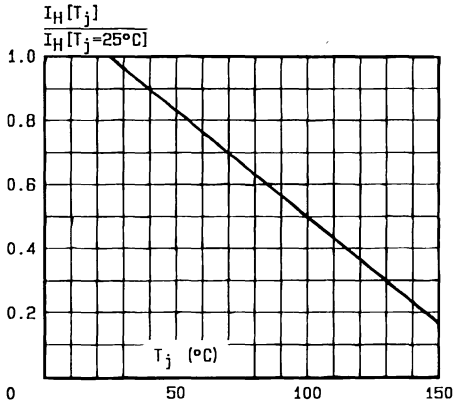


Fig.1 - Relative variation of holding current versus junction temperature.

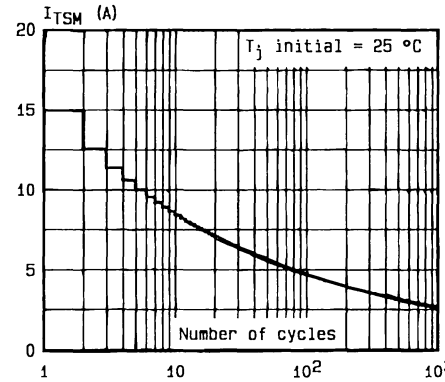


Fig.2 - Non_repetitive surge peak on-state current versus number of cycles (1 cycle = 20 ms).

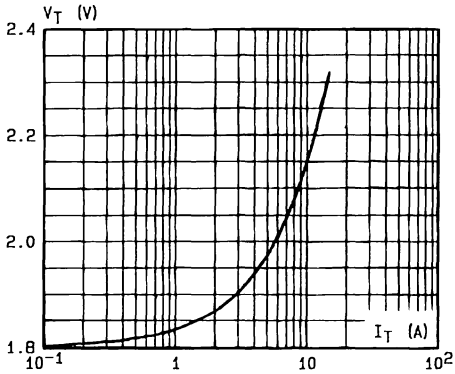


Fig.3 - Peak on-state voltage versus peak on-state current (typical values).

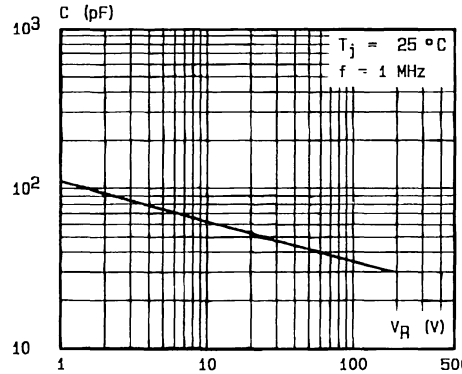


Fig.4 - Capacitance versus reverse applied voltage (typical values).

D89THBT200DP4

SGS-THOMSON MICROELECTRONICS

THDT 58 D

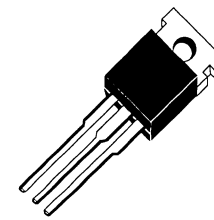
TRISIL

DESCRIPTION

This protection device has been especially designed for subscriber line-card and terminal protection. By itself, it enables to protect integrated SLIC against transient overvoltages. A diode clips positive overloads and breakover device negative overloads.

Its ion-implanted technology confers excellent electrical characteristics on it.

This is why this THDT 58 D easily corresponds to the main protection standard norms which are related to the overvoltages on subscribers lines.



TO 220 AB
(Plastic)

IN ACCORDANCE WITH FOLLOWING STANDARDS :

CCITT K17 - K20	10/700 µs	1.5 kV
	5/310 µs	38 A
VDE 0433	10/700 µs	2 kV
	5/200 µs	50 A
CNET	0.5/700 µs	1.5 kV
	0.2/310 µs	38 A

ABSOLUTE RATINGS (limiting values) (T_j = 25 °C)

Symbol	Parameter		Value	Unit
I_{pp}	Peak Pulse Current	1 ms expo	75	A
		8-20 µs expo*	150	
I_{FSM} I_{TSM}	Non Repetitive Surge Peak on-state Current	t_p = 20 ms	30	A
di/dt	Critical Rate of Rise of on-state Current	Non Repetitive	100	A/µs
T_{stg} T_j	Storage and Operating Junction Temperature Range		– 40 to 150 150	°C °C
T_L	Maximum Lead Temperature for Soldering During 10 s at 4 mm from Case		230	°C

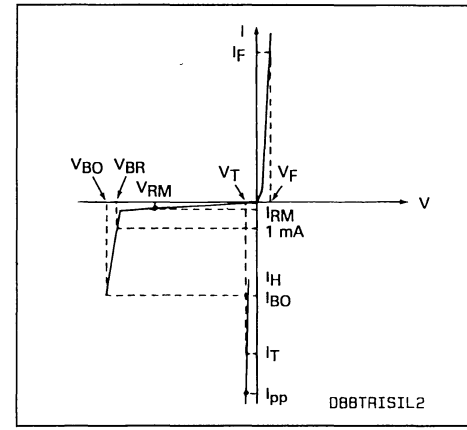
* ANSI STD C62.

THERMAL RESISTANCES

Symbol	Parameter	Value	Unit
$R_{th(j-c)}$	Junction to Case for DC	5	°C/W
$R_{th(j-a)}$	Junction to Ambient	60	°C/W

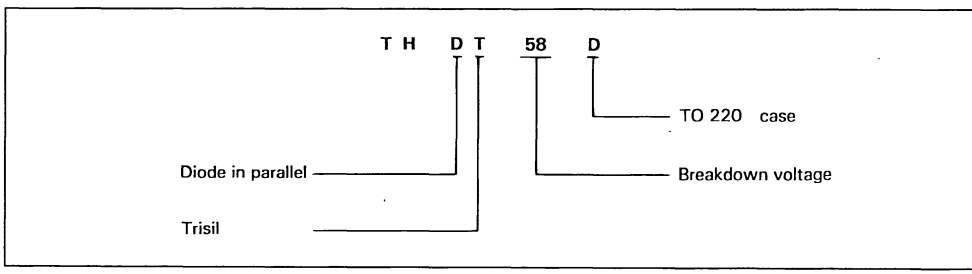
ELECTRICAL CHARACTERISTICS

Symbol	Parameter
V_{RM}	Stand-off Voltage
V_{BR}	Breakdown Voltage
V_{BO}	Clamping Voltage
I_H	Holding Current
V_T	On-state Voltage
V_F	Forward Voltage Drop
I_{BO}	Breakover Current
I_{pp}	Peak-pulse Current



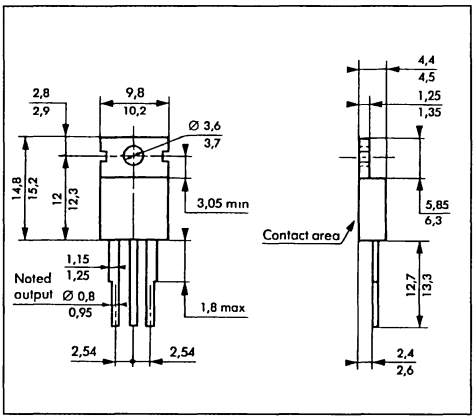
Symbol	Test Conditions			Min.	Typ.	Max.	Unit
I_{RM}	T_j = 25 °C	V_{RM} = – 56 V				– 10	µA
V_{BR}	T_j = 25 °C	I_R = – 1 mA		– 58	– 60		V
V_{BO}	T_j = 25 °C	t_p = 100 µs				– 80	V
I_{BO}	T_j = 25 °C	t_p = 100 µs		– 150		– 800	mA
I_H	T_j = 25 °C	I_T = – 2 A		– 150			mA
V_T	T_j = 25 °C	I_T = – 5 A	t_p = 100 µs			– 3	V
V_F	T_j = 25 °C	I_F = 5 A	t_p = 100 µs			3	V
α_T					10		10^{-4}/°C
C	T_j = 25 °C	F = 1 MHz	V_R = – 5 V			500	pF
dv/dt	T_j = 25 °C	Exponential Ramp 67 % V_{BR}		5000			V/µs

ORDER CODE

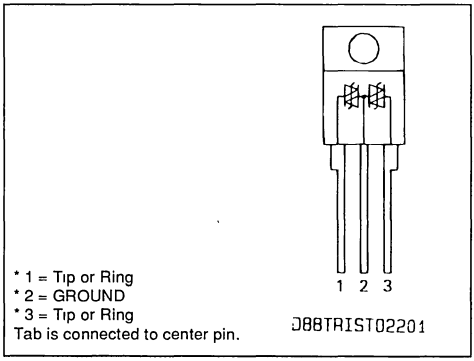


PACKAGE MECHANICAL DATA

TO 220 AB Plastic

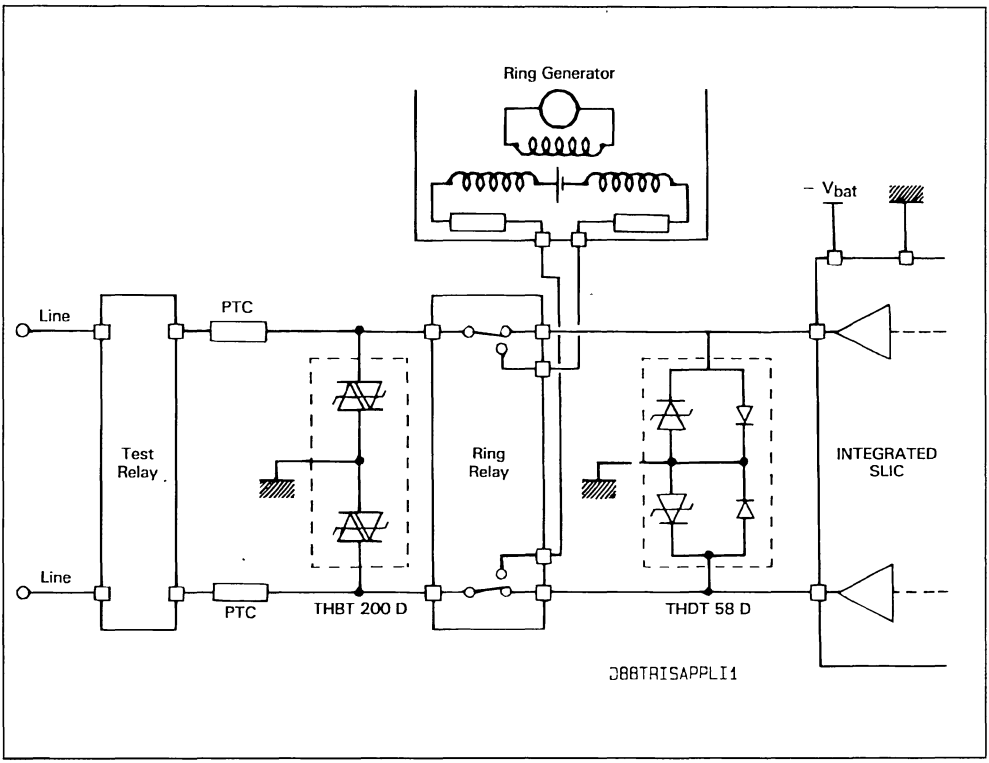


PIN CONNECTIONS



Cooling method : by conduction (Method C)
Marking : type number
Weight : 2 g.

APPLICATION CIRCUIT



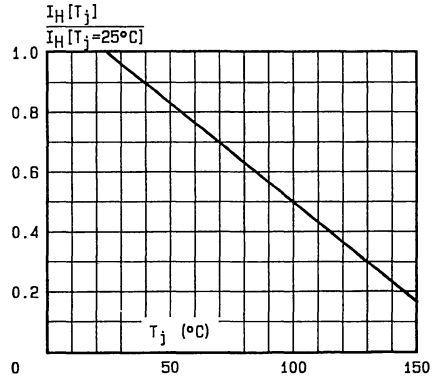


Fig.1 - Relative variation of holding current versus junction temperature.

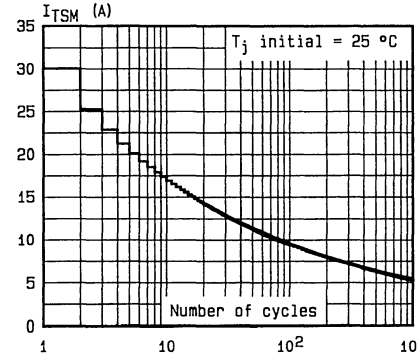


Fig.2 - Non_repetitive surge peak on-state current versus number of cycles (1 cycle = 20 ms).

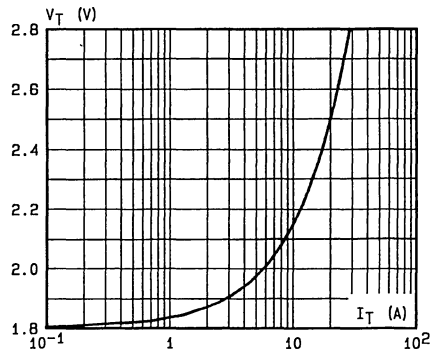


Fig.3 - Peak on-state voltage versus peak on-state current (typical values).

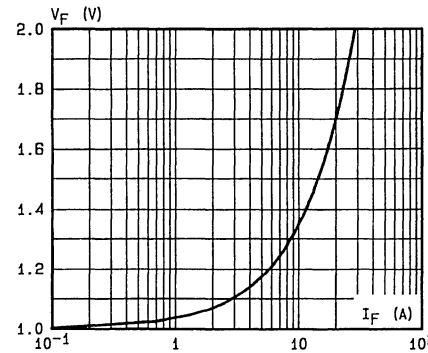


Fig.4 - Peak forward voltage drop versus peak forward current (typical values).

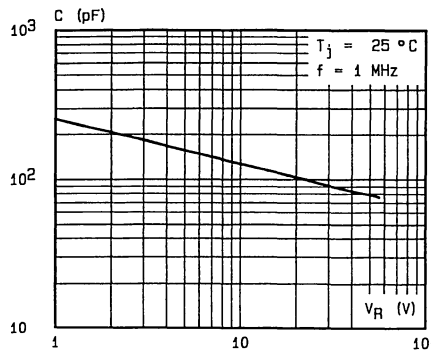


Fig.5 - Capacitance versus reverse applied voltage (typical values).

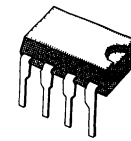
D89THDT58DP4

SGS-THOMSON MICROELECTRONICS

L3100B
L3100B1

TRISIL
UNIDIRECTIONAL PROGRAMMABLE VOLTAGE AND CURRENT SUPPRESSOR

- HIGH CURRENT CAPABILITY
- PROGRAMMABILITY BOTH IN VOLTAGE AND CURRENT
- AUTOMATIC RECOVERY



Minidip
(Plastic)

DESCRIPTION

The L3100B/B1 is a transient overvoltage suppressor/overcurrent arrester designed to protect sensitive components in electronic telephones and telecommunication equipments against transients caused by lightning, induction from power lines, etc.

The L3100B/B1 characteristic, that is its firing voltage and current, can be easily programmed by means of inexpensive external components ; more over, since this device recoveres automatically when the surge current falls below a fixed holding current, it may be used on remotely supplied lines. Finally, if destroyed, it becomes a permanent short circuit.

ABSOLUTE RATINGS (limiting values) (T_j = 25 °C)

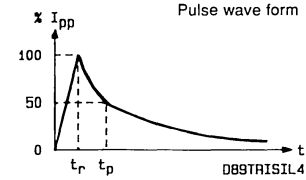
Symbol	Parameter		Value	Unit
I_{pp}	Peak Pulse Current	1 ms expo	150	A
		8-20 µs expo*	250	
I_{TSM}	Non Repetitive Surge Peak on-state Current	t_p = 10 ms – Sinus	50	A
di/dt	Critical Rate of Rise of on-state Current	Non repetitive	100	A/µs
T_{stg} T_j	Storage and Junction Temperature Range		– 40 to 150 150	°C °C

THERMAL RESISTANCE

Symbol	Parameter	Value	Unit
$R_{th(j-a)}$	Junction to Ambient	80	°C/W

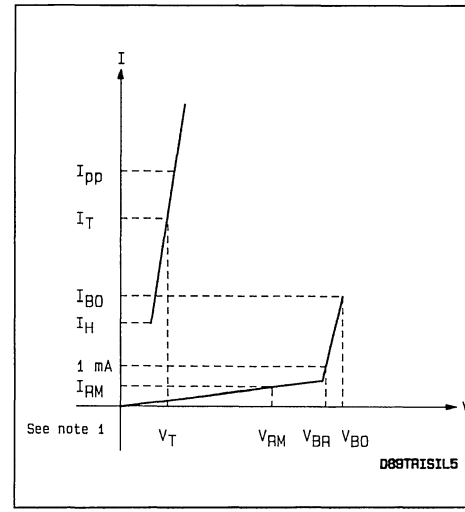
* ANSI STD C62

Pulse wave form



ELECTRICAL CHARACTERISTICS
(T_j = 25 °C)

Symbol	Parameter
V_{RM}	Stand-off Voltage
V_{BR}	Breakdown Voltage
V_{BO}	Clamping Voltage
I_H	Holding Current
V_T	On-state Voltage @ I_T
I_{BO}	Breakover Current
I_{pp}	Peak-pulse Current
V_{GN}	Gate Voltage
I_{GN}	Firing Gate N Current
V_{RGN}	Reverse Gate N Voltage
I_{GP}	Firing Gate P Current



OPERATION WITHOUT GATE

Type	I_{RM} @ V_{RM} max.		V_{BR} @ I_R min.		max.	V_{BO} @ I_{BO} max. See note 2	min.	max.	I_H min.	V_T typ. I_T = 1 A	C max. V_R = 5 V F = 1 MHz
	(µA)	(V)	(V)	(V)	(mA)	(V)	(mA)	(mA)	(mA)	(V)	(pF)
L3100B/B1	6 40	60 250	255 (3) 265 (4)		1	350	200	500	210 (3) 280 (4)	2	100

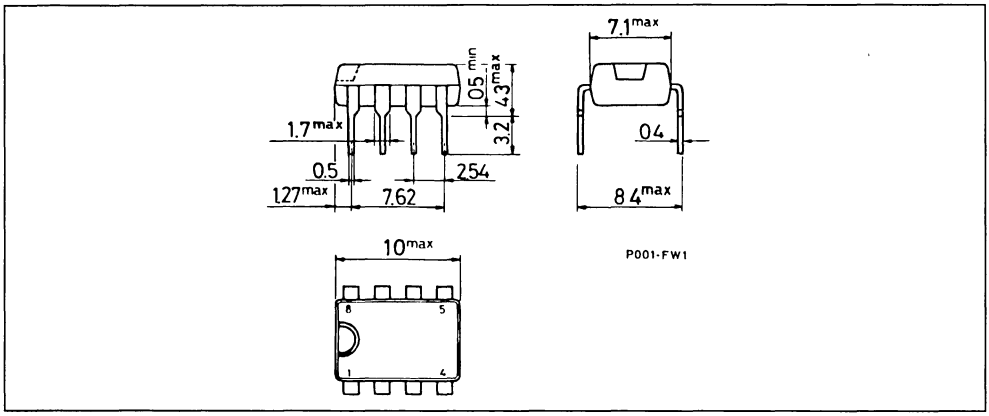
OPERATION WITH GATES

Type	V_{GN} (V) I_G = 200 mA		I_{GN} (mA) V_A – C = 100 V		V_{RGN} (V) I_G = – 1 mA		I_{GP} (mA) V_A – C = 100 V	
	min.	max.	min.	max.	min.	max.	min.	max.
L3100B/B1	0.6	1.8	30	200	0.7			150

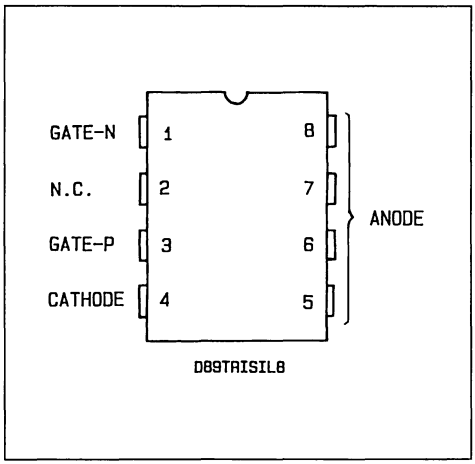
Notes : 1. Reverse characteristic : I_R < 1 mA @ V_R = 0.7V.
2. These devices are not designed to function as zeners ; continuous operation between 1 mA and I_{BO} will damage them
3. L3100B1
4 L3100B

PACKAGE MECHANICAL DATA

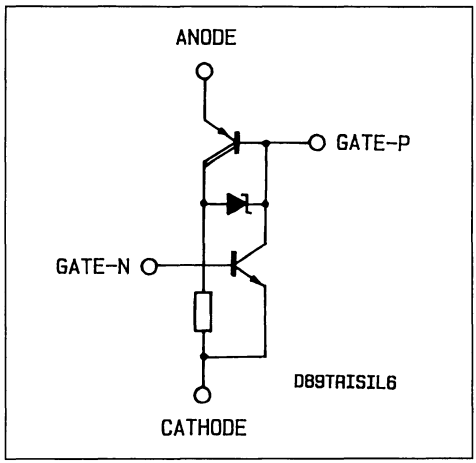
MINIDIP Plastic



CONNECTION DIAGRAM



SCHEMATIC DIAGRAM



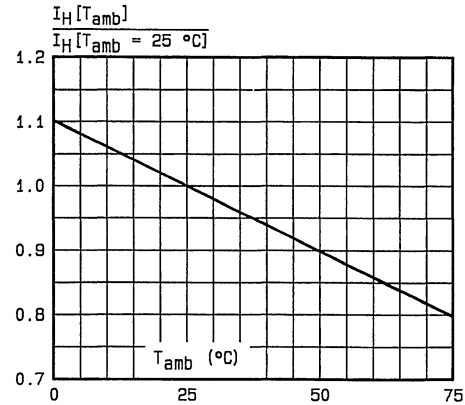


Fig.1 - Relative variation of holding current versus ambient temperature.

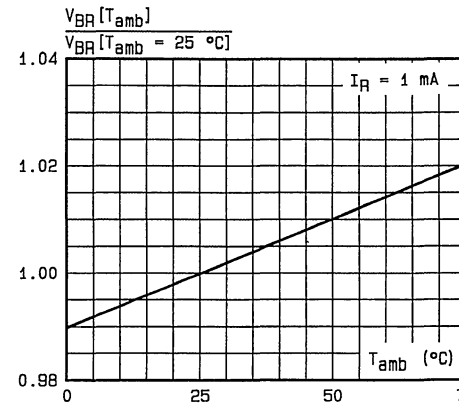


Fig.2 - Relative variation of breakdown voltage versus ambient temperature.

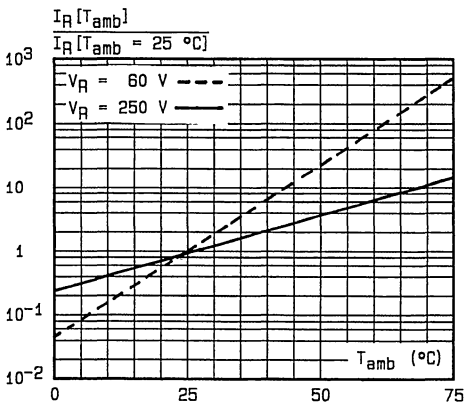


Fig.3 - Relative variation of leakage current versus ambient temperature.

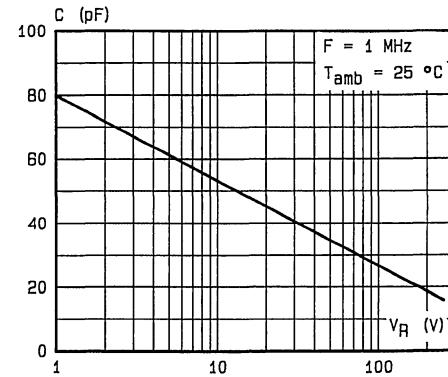


Fig.4 - Junction capacitance versus reverse applied voltage.

D89L3100B1P4

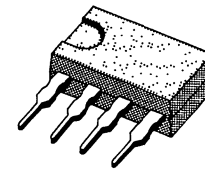
SGS-THOMSON MICROELECTRONICS

L3121B

TRISIL

BIDIRECTIONAL PROGRAMMABLE VOLTAGE AND CURRENT SUPPRESSOR

- HIGH CURRENT CAPABILITY
- PROGRAMMABILITY BOTH IN VOLTAGE AND CURRENT
- AUTOMATIC RECOVERY



SIP-4
(Plastic)

DESCRIPTION

The L3121B is a bidirectional transient overvoltage/overcurrent protections derived from the programmable L3101B to provide full feature protection for the subscriber line interface.

Full programmability is allowed through access to the triggering gate available on the chips. The L3121B protects the line to ground either against positive or negative transients with external and independent adjustment of the threshold voltages (zener or external battery) in the two directions.

ABSOLUTE RATINGS (limiting values) (T_j = 25 °C)

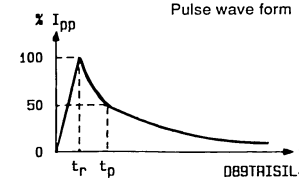
Symbol	Parameter		Value	Unit
I_{pp}	Peak Pulse Current	1 ms expo	150	A
		8-20 µs expo*	250	
I_{TSM}	Non Repetitive Surge Peak on-state Current	t_p = 10 ms Sinus	50	A
di/dt	Critical Rate of Rise of on-state Current	Non repetitive	100	A/µs
T_{stg} T_j	Storage and Junction Temperature Range		– 40 to 150 150	°C °C

THERMAL RESISTANCE

Symbol	Parameter	Value	Unit
$R_{th(j-a)}$	Junction to Ambient	80	°C/W

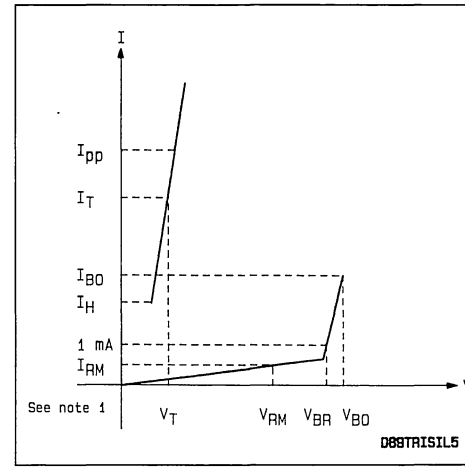
* ANSI STD C62.

Pulse wave form



ELECTRICAL CHARACTERISTICS
(T_j = 25 °C)

Symbol	Parameter
V_{RM}	Stand-off Voltage
V_{BR}	Breakdown Voltage
V_{BO}	Clamping Voltage
I_H	Holding Current
V_T	On-state Voltage @ I_T
I_{BO}	Breakover Current
I_{pp}	Peak-pulse Current
V_G	Gate Voltage
I_{GN}	Firing Gate N Current
I_{GP}	Firing Gate P Current



OPERATION WITHOUT GATE

Type	I_{RM} @ V_{RM} max.		V_{BR} @ I_R min.		max.	V_{BO} @ I_{BO} max.	typ.	max. See note 2	I_H min.	V_T typ. I_T = 1 A	C max. V_R = 5 V F = 1 MHz
	(μA)	(V)	(V)	(V)	(mA)	(V)	(mA)	(mA)	(mA)	(V)	(pF)
L3121B	5 8	60 90	100		1	180	200	500	150	2	200

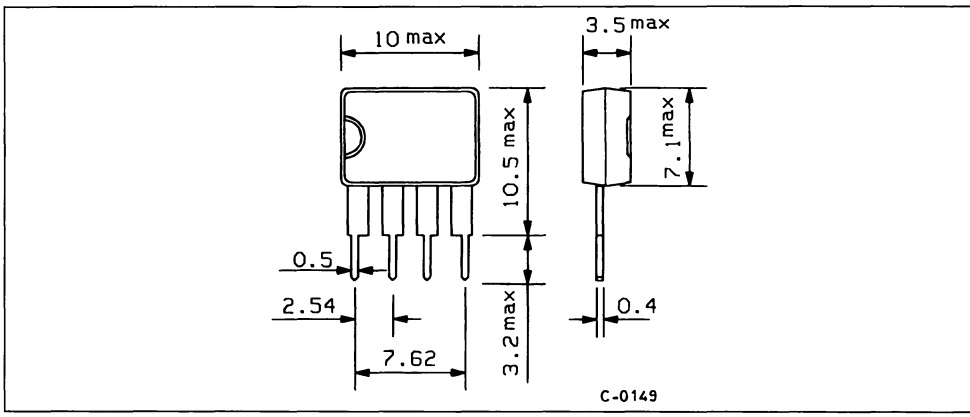
OPERATION WITH GATES

Type	V_G (V) I_G = 200 mA		I_{GN} (mA) $V_A - C$ = 60 V		I_{GP} (mA) $V_A - C$ = 60 V	
	min.	max.	min.	max.	min.	max.
L3121B	0.6	1.8	80	200		180

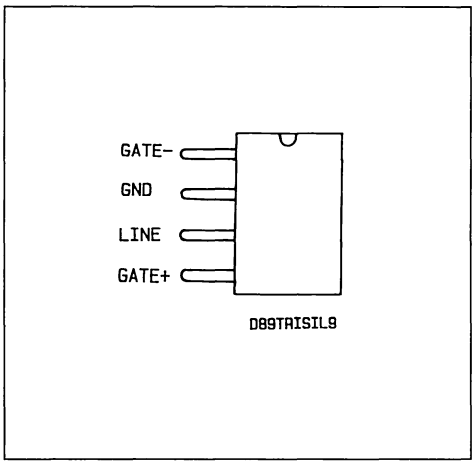
Notes : 1 Same characteristic both sides
2. These devices are not designed to function as zeners ; continuous operation between 1 mA and I_{BO} will damage then.

PACKAGE MECHANICAL DATA

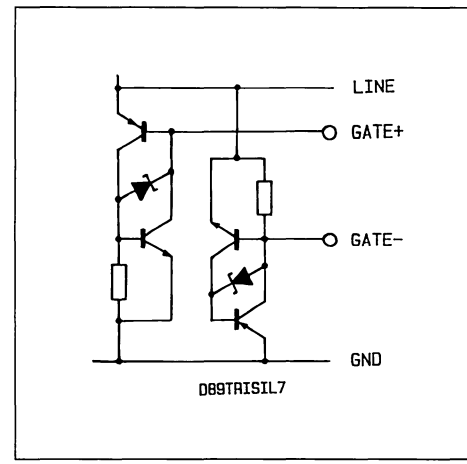
SIP-4 Plastic



CONNECTION DIAGRAM



SCHEMATIC DIAGRAM



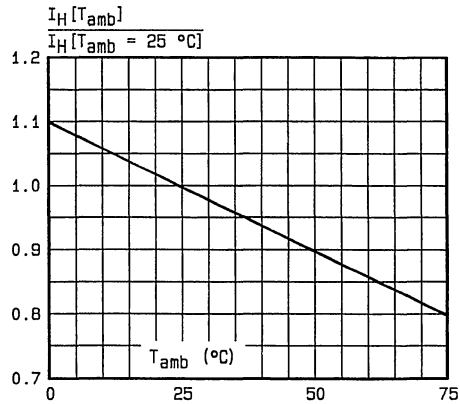


Fig.1 - Relative variation of holding current versus ambient temperature.

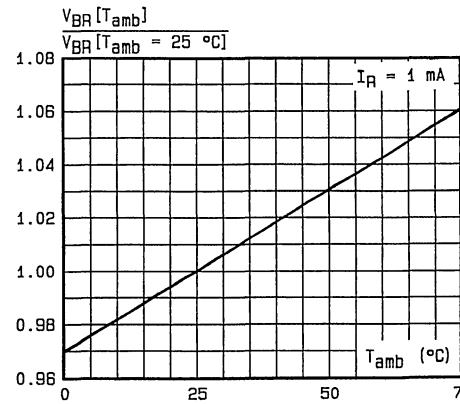


Fig.2 - Relative variation of breakdown voltage versus ambient temperature.

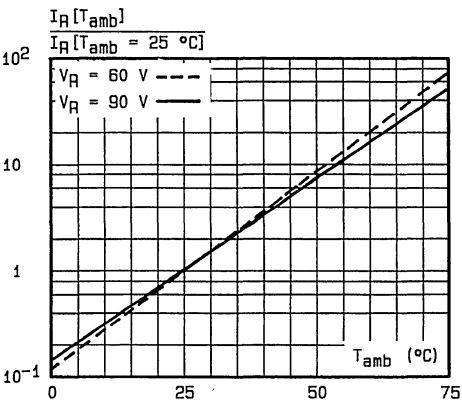


Fig.3 - Relative variation of leakage current versus ambient temperature.

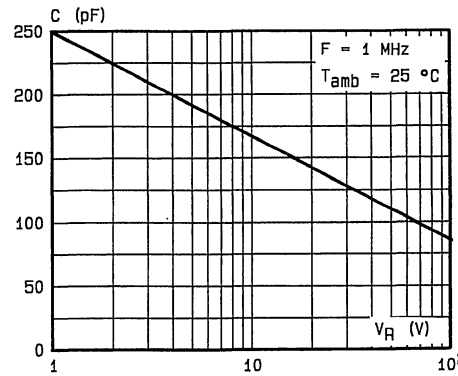


Fig.4 - Junction capacitance versus reverse applied voltage.

D89L3121BP4

SGS-THOMSON MICROELECTRONICS

SM4T6V8, A → 220, A
SM4T6V8C, A → 200C, A

UNI-AND BIDIRECTIONAL TRANSIENT VOLTAGE SUPPRESSORS

- HIGH SURGE CAPABILITY : 400 W / 1 ms EXPO
- VERY FAST CLAMPING TIME : 1 ps FOR UNIDIRECTIONAL TYPES 5 ns FOR BIDIRECTIONAL TYPES
- LARGE VOLTAGE RANGE : 5.5 V → 188 V
- ORDER CODE : TYPE NUMBER FOR UNIDIRECTIONAL TYPES, TYPE NUMBER + SUFFIX C FOR BIDIRECTIONAL TYPES

SOD 6
(Plastic)

SURFACE MOUNT TRANSIL FEATURES

- A PERFECT PICK AND PLACE BEHAVIOUR
- AN EXCELLENT ON BOARD STABILITY
- A FULL COMPATIBILITY WITH BOTH GLUING AND PASTE SOLDERING TECHNOLOGIES
- BODY MARKED WITH TYPE CODE AND LOGO
- STANDARD PACKAGING : 12 mm TAPE (EIA STD. RS481)
- TINNED COPPER LEADS
- HIGH TEMPERATURE RESISTANT RESIN

DESCRIPTION

Transient voltage suppressor diodes especially useful in protecting integrated circuits, MOS, hybrids and other voltage-sensitive semiconductors and components.

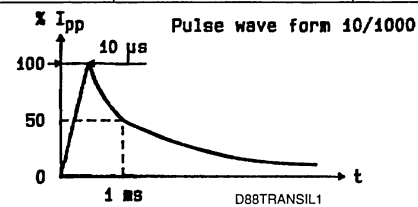
ABSOLUTE RATINGS (limiting values)

Symbol	Parameter		Value	Unit
P_p	Peak Pulse Power for 1 ms Exponential Pulse	T_j Initial = 25 °C See note 1	400	W
P	Power Dissipation on Infinite Heatsink	T_{amb} = 25 °C	1.2	W
I_{FSM}	Non Repetitive Surge Peak Forward Current for Unidirectional Types	T_j Initial = 25 °C t = 10 ms	50	A
T_{stg} T_j	Storage and Operating Junction Temperature Range		– 65 to 175 150	°C °C
T_L	Maximum Lead Temperature for Soldering During 10 s		260	°C

THERMAL RESISTANCE

Symbol	Parameter	Value	Unit
$R_{th(j-l)}$	Junction-leads	20	°C/W

Note : 1. For surges upper than the maximum values, the diode will present a short-circuit anode-cathode.



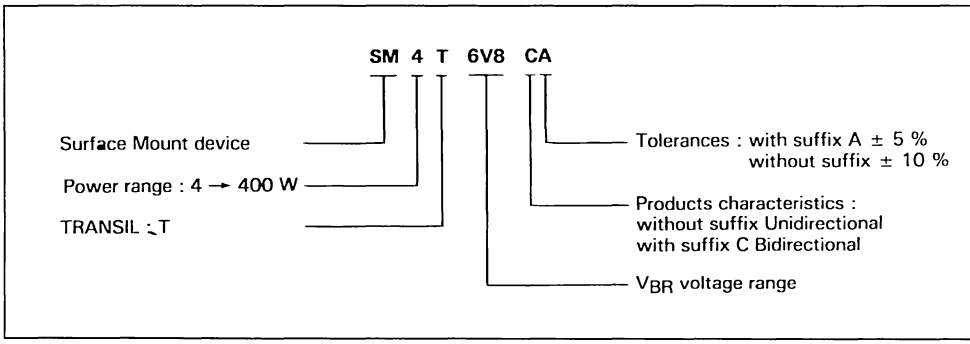
ELECTRICAL CHARACTERISTICS (T_j = 25 °C)

Symbol	Parameter		Value
V_{RM}	Stand-off Voltage		See tables
$V_{(BR)}$	Breakdown Voltage		
$V_{(CL)}$	Clamping Voltage		
I_{pp}	Peak Pulse Current		
α_T	Temperature Coefficient of $V_{(BR)}$		
C	Capacitance		
$t_{clamping}$	Clamping Time (0 volt to $V_{(BR)}$)	Unidirectional Types	1 ps max.
		Bidirectional Types	5 ns max.

Types		Marking		I_{RM} @ V_{RM} max.		$V_{(BR)}$* @ I_R (V)				$V_{(CL)}$ @ I_{pp} max. 1ms expo		$V_{(CL)}$ @ I_{pp} max. 8-20µs expo		α_T max.	C** typ. V_R=0 f=1MHz
Unidirectional	Bidirectional	Unidirectional	Bidirectional	(µA)	(V)	min.	nom.	max.	(mA)	(V)	(A)	(V)	(A)	(10^{-4}/°C)	(pF)
SM4T6V8	SM4T6V8C	QD	VD	1000	5.5	6.12	6.8	7.48	10	10.8	37	14	164	5.7	3500
SM4T6V8A	SM4T6V8CA	QE	VE	1000	5 8	6 45	6.8	7 14	10	10 5	38	13.4	174	5.7	3500
SM4T7V5	SM4T7V5C	QF	VF	500	6 05	6 75	7 5	8.25	10	11 7	34	15.2	151	6.1	3100
SM4T7V5A	SM4T7V5CA	QG	VG	500	6 4	7 13	7.5	7 88	10	11 3	35 4	14.5	160	6.1	3100
SM4T10	SM4T10C	QN	VN	1 0	8.1	9	10	11	1	15	27	19.5	246	7.3	2000
SM4T10A	SM4T10CA	QP	VP	1 0	8.55	9.5	10	10 5	1	14 5	27 6	18 6	258	7 3	2000
SM4T12	SM4T12C	QS	VS	5	9.72	10.8	12	13.2	1	17.3	23 1	22 7	211	7 8	1550
SM4T12A	SM4T12CA	QT	VT	5	10.2	11.4	12	12.6	1	16.7	24	21.7	221	7.8	1550
SM4T15	SM4T15C	QW	VW	5	12.1	13.5	15	16.5	1	22	18.2	28 4	169	8 4	1200
SM4T15A	SM4T15CA	QX	VX	5	12.8	14.3	15	15.8	1	21.2	19	27.2	176	8.4	1200
SM4T18	SM4T18C	RD	UD	5	14.5	16.2	18	19.8	1	26.5	15.1	34	141	8.8	975
SM4T18A	SM4T18CA	RE	UE	5	15 3	17.1	18	18.9	1	25.2	16	32.5	148	8.8	975
SM4T22	SM4T22C	RH	UH	5	17.8	19.8	22	24.2	1	31 9	12.5	41.2	116	9 2	800
SM4T22A	SM4T22CA	RK	UK	5	18 8	20 9	22	23 1	1	30 6	13	39 3	122	9.2	800
SM4T24	SM4T24C	RL	UL	5	19.4	21 6	24	26 4	1	34.7	11.5	44.9	107	9.4	725
SM4T24A	SM4T24CA	RM	UM	5	20 5	22.8	24	25 2	1	33 2	12	42 8	112	9 4	725
SM4T27	SM4T27C	RN	UN	5	21.8	24.3	27	29.7	1	39 1	10.2	50.5	95	9.6	625
SM4T27A	SM4T27CA	RP	UP	5	23 1	25.7	27	28.4	1	37.5	10 7	48.3	99	9.6	625
SM4T30	SM4T30C	RQ	UQ	5	24.3	27	30	33	1	43.5	9.2	56.1	86	9.7	575
SM4T30A	SM4T30CA	RR	UR	5	25 6	28.5	30	31.5	1	41.5	9.6	53.5	90	9.7	575
SM4T33	SM4T33C	RS	US	5	26.8	29.7	33	36.3	1	47 7	8.4	61.7	78	9.8	510
SM4T33A	SM4T33CA	RT	UT	5	28 2	31.4	33	34.7	1	45 7	8.8	59	81.5	9.8	510
SM4T36	SM4T36C	RU	UU	5	29 1	32 4	36	39.6	1	52	7.7	67.3	71	9.9	480
SM4T36A	SM4T36CA	RV	UV	5	30.8	34 2	36	37.8	1	49.9	8	64.3	74.5	9 9	480
SM4T39	SM4T39C	RW	UW	5	31.6	35 1	39	42 9	1	56 4	7 1	73	66	10 0	450
SM4T39A	SM4T39CA	RX	UX	5	33.3	37.1	39	41	1	53.9	7 4	69 7	69	10 0	450
SM4T68	SM4T68C	SN	WN	5	55.1	61.2	68	74.8	1	98	4.1	127	38	10.4	270
SM4T68A	SM4T68CA	SP	WP	5	58.1	64.6	68	71.4	1	92	4.3	121	39.5	10.4	270
SM4T100	SM4T100C	SW	WW	5	81	90	100	110	1	144	2.8	187	25.5	10.6	200
SM4T100A	SM4T100CA	SX	WX	5	85.5	95	100	105	1	137	2.9	178	27	10.6	200
SM4T150	SM4T150C	TH	XH	5	121	135	150	165	1	215	1.9	277	17.3	10.8	145
SM4T150A	SM4T150CA	TK	XK	5	128	143	150	158	1	207	2	265	18.1	10.8	145
SM4T200	SM4T200C	TS	XS	5	162	180	200	220	1	287	1.4	370	13	10.8	120
SM4T200A	SM4T200CA	TT	XT	5	171	190	200	210	1	274	1.5	353	13 6	10 8	120
SM4T220		TU		5	178	198	220	242	1	315	1.3	406	11 8	10 8	110
SM4T220A		TV		5	188	209	220	231	1	301	1 4	388	12 4	10 8	110

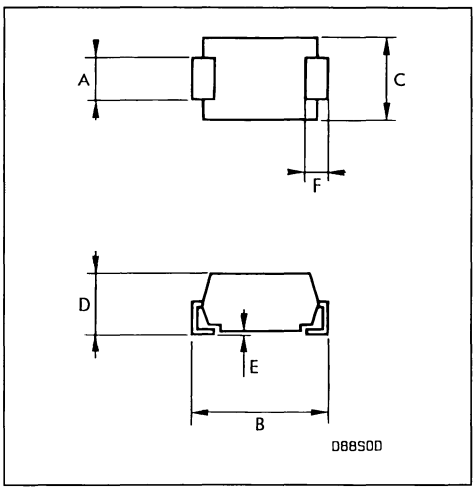
* Pulse test $t_p \leq 50$ ms $\delta < 2$ %.
** Divide these values by 2 for bidirectional types.
For bidirectional types, electrical characteristics apply in both directions.

ORDER CODE



PACKAGE MECHANICAL DATA

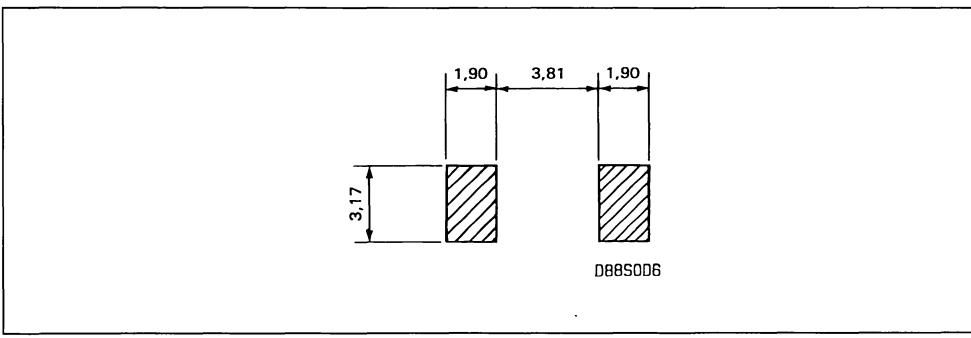
SOD 6 Plastic



Ref.	Millimetres		Inches	
	Min.	Max.	Min.	Max.
A	2.8	3.2	0.110	0.126
B	6.0	6.4	0.236	0.252
C	3.8	4.2	0.150	0.165
D	2.5	3.1	0.098	0.122
E	–	0.1	–	0.004
F	0.9	1.3	0.035	0.051

Laser marking.
The logo indicates cathode for unidirectional types.

FOOT PRINT DIMENSIONS (Millimeters)



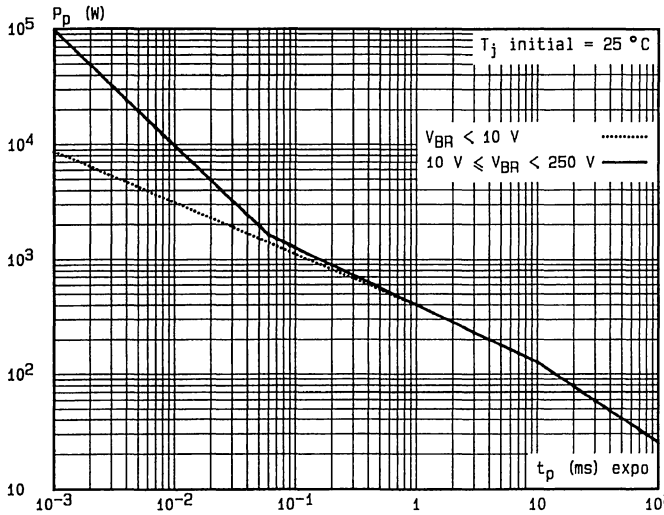


Fig.1 - Peak pulse power versus exponential pulse duration.

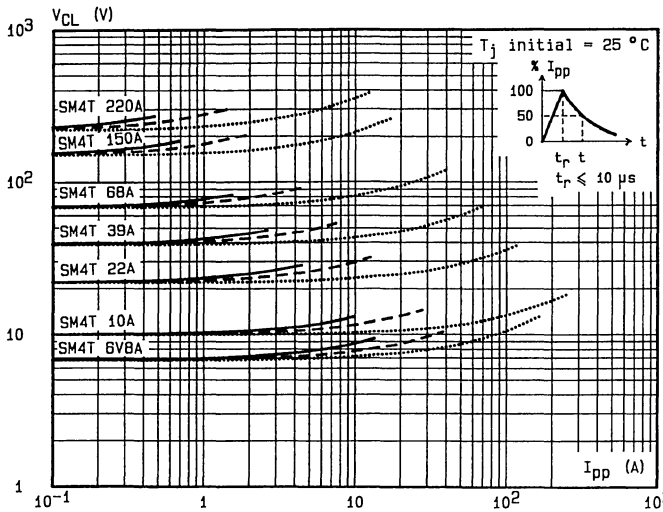


Fig.2 - Clamping voltage versus peak pulse current.
exponential waveform t = 20 µs ·····
t = 1 ms – – –
t = 10 ms ——

Note : The curves of the figure 2 are specified for a junction temperature of 25 °C before surge. The given results may be extrapolated for other junction temperatures by using the following formula : $\Delta V_{(BR)} = \alpha_{T(V(BR))} \times [T_j - 25] \times V_{(BR)}$
For intermediate voltages, extrapolate the given results.

D88SM4TP4

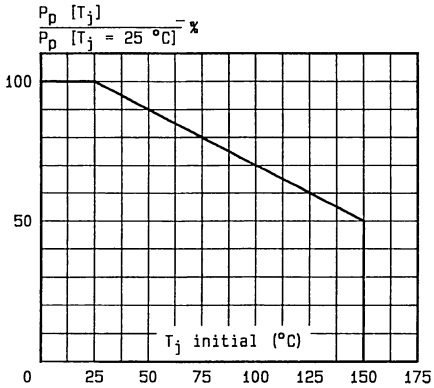


Fig.3 - Allowable power dissipation versus junction temperature.

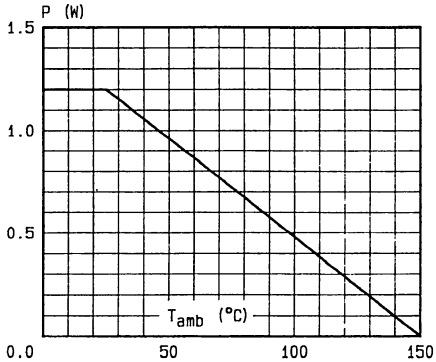


Fig.4 - Power dissipation versus ambient temperature.

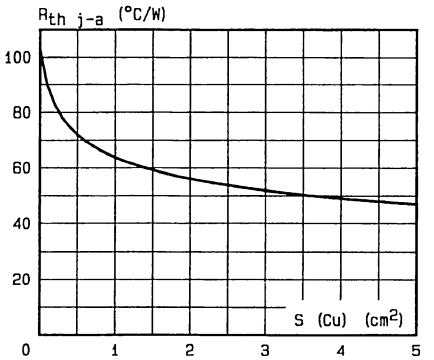


Fig.5 - Thermal resistance junction-ambient versus Cu surface (printed circuit).

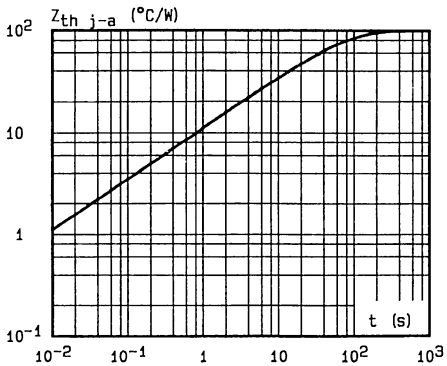


Fig.6 - Transient thermal impedance junction-ambient versus pulse duration.

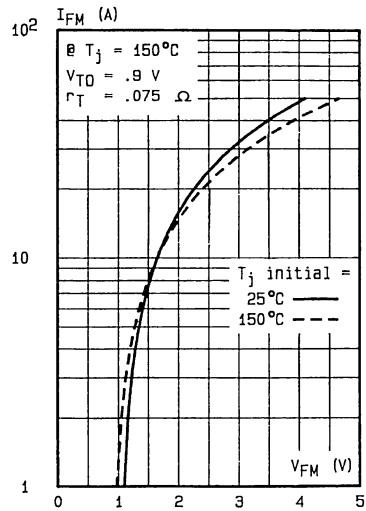


Fig.7 - Peak forward current versus peak forward voltage drop (typical values for unidirectional types).

D88SM4TP5

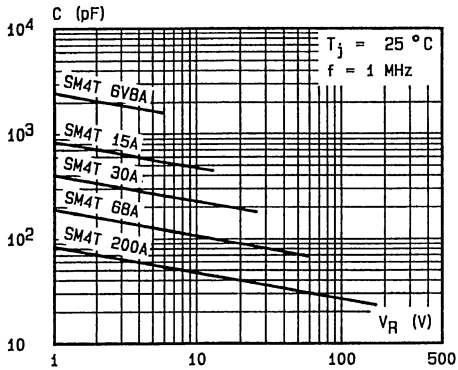


Fig.8a - Capacitance versus reverse applied voltage for unidirectional types (typical values).

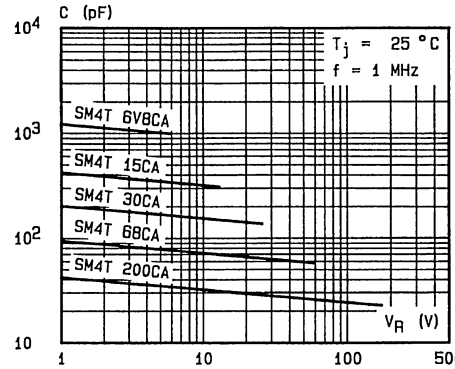


Fig.8b - Capacitance versus reverse applied voltage for bidirectional types (typical values).

D88SM4TP6

SM6T6V8, A → 220, A
SM6T6V8C, A → 200C, A

UNI-AND BIDIRECTIONAL TRANSIENT VOLTAGE SUPPRESSORS

- HIGH SURGE CAPABILITY : 600 W / 1 ms EXPO
- VERY FAST CLAMPING TIME : 1 ps FOR UNIDIRECTIONAL TYPES 5 ns FOR BIDIRECTIONAL TYPES
- LARGE VOLTAGE RANGE : 5.5 V → 188 V
- ORDER CODE : TYPE NUMBER FOR UNIDIRECTIONAL TYPES, TYPE NUMBER + SUFFIX C FOR BIDIRECTIONAL TYPES

SOD 6
(Plastic)

SURFACE MOUNT TRANSIL FEATURES

- A PERFECT PICK AND PLACE BEHAVIOUR
- AN EXCELLENT ON BOARD STABILITY
- A FULL COMPATIBILITY WITH BOTH GLUING AND PASTE SOLDERING TECHNOLOGIES
- BODY MARKED WITH TYPE CODE AND LOGO
- STANDARD PACKAGING : 12 mm TAPE (EIA STD. RS481)
- TINNED COPPER LEADS
- HIGH TEMPERATURE RESISTANT RESIN

DESCRIPTION

Transient voltage suppressor diodes especially useful in protecting integrated circuits, MOS, hybrids and other voltage-sensitive semiconductors and components.

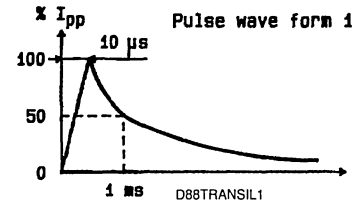
ABSOLUTE RATINGS (limiting values)

Symbol	Parameter		Value	Unit
P_p	Peak Pulse Power for 1 ms Exponential Pulse	T_j Initial = 25 °C See note 1	600	W
P	Power Dissipation on Infinite Heatsink	T_{amb} = 25 °C	1.2	W
I_{FSM}	Non Repetitive Surge Peak Forward Current for Unidirectional Types	T_j Initial = 25 °C t = 10 ms	50	A
T_{stg} T_j	Storage and Operating Junction Temperature Range		– 65 to 175 150	°C °C
T_L	Maximum Lead Temperature for Soldering During 10 s		260	°C

THERMAL RESISTANCE

Symbol	Parameter	Value	Unit
$R_{th(j-l)}$	Junction-leads	20	°C/W

Note : 1. For surges upper than the maximum values, the diode will present a short-circuit anode-cathode.



ELECTRICAL CHARACTERISTICS (T_j = 25 °C)

Symbol	Parameter		Value
V_{RM}	Stand-off Voltage		See tables
$V_{(BR)}$	Breakdown Voltage		
$V_{(CL)}$	Clamping Voltage		
I_{pp}	Peak Pulse Current		
α_T	Temperature Coefficient of $V_{(BR)}$		
C	Capacitance		
$t_{clamping}$	Clamping Time (0 volt to $V_{(BR)}$)	Unidirectional Types	1 ps max.
		Bidirectional Types	5 ns max.

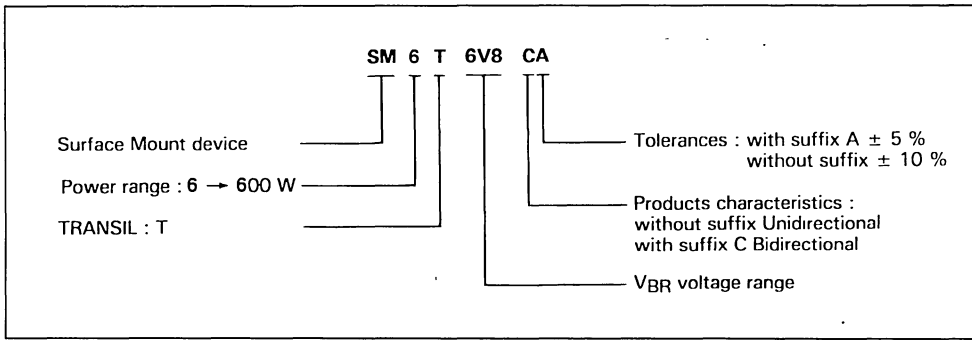
Types		Marking		I_{RM} @ V_{RM} max.		$V_{(BR)}$* @ I_R (V)				$V_{(CL)}$ @ I_{pp} max. 1ms expo		$V_{(CL)}$ @ I_{pp} max. 8-20µs expo		α_T max.	C** typ. V_R=0 f=1MHz
Unidirectional	Bidirectional	Unidirectional	Bidirectional	(µA)	(V)	min.	nom.	max.	(mA)	(V)	(A)	(V)	(A)	(10^{-4}/°C)	(pF)
SM6T6V8	SM6T6V8C	DD	LD	1000	5.5	6.12	6 8	7 48	10	10 8	55	14	250	5.7	4000
SM6T6V8A	SM6T6V8CA	DE	LE	1000	5 8	6.45	6 8	7 14	10	10 5	57	13 4	261	5 7	4000
SM6T7V5	SM6T7V5C	DF	LF	500	6.05	6.75	7 5	8 25	10	11.7	51	15 2	230	6.1	3700
SM6T7V5A	SM6T7V5CA	DG	LG	500	6.4	7.13	7.5	7.88	10	11.3	53	14 5	241	6 1	3700
SM6T10	SM6T10C	DN	LN	1 0	8.1	9.0	10	11	1	15	40	19 5	369	7 3	2800
SM6T10A	SM6T10CA	DP	LP	1 0	8 55	9 5	10	10.5	1	14.5	41	18.6	387	7 3	2800
SM6T12	SM6T12C	DS	LS	5	9 72	10.8	12	13.2	1	17 3	35	22.7	317	7 8	2300
SM6T12A	SM6T12CA	DT	LT	5	10.2	11.4	12	12 6	1	16 7	36	21.7	332	7.8	2300
SM6T15	SM6T15C	DW	LW	5	12 1	13 5	15	16 5	1	22	27.5	28.4	254	8.4	1900
SM6T15A	SM6T15CA	DX	LX	5	12.8	14 3	15	15.8	1	21.2	28	27.2	265	8 4	1900
SM6T18	SM6T18C	ED	MD	5	14.5	16 2	18	19 8	1	26 5	22 5	34	212	8 8	1600
SM6T18A	SM6T18CA	EE	ME	5	15.3	17.1	18	18 9	1	25 2	24	32 5	222	8 8	1600
SM6T22	SM6T22C	EH	MH	5	17.8	19.8	22	24 2	1	31 9	18 5	41 2	175	9.2	1350
SM6T22A	SM6T22CA	EK	MK	5	18.8	20.9	22	23.1	1	30 6	20	39 3	183	9 2	1350
SM6T24	SM6T24C	EL	ML	5	19.4	21.6	24	26.4	1	34 7	17.5	44 9	160	9 4	1250
SM6T24A	SM6T24CA	EM	MM	5	20.5	22.8	24	25.2	1	33.2	18	42.8	168	9 4	1250
SM6T27	SM6T27C	EN	MN	5	21.8	24.3	27	29.7	1	39.1	15.5	50.5	143	9.6	1150
SM6T27A	SM6T27CA	EP	MP	5	23.1	25 7	27	28.4	1	37 5	16	48.3	149	9.6	1150
SM6T30	SM6T30C	EQ	MQ	5	24.3	27	30	33	1	43 5	13.5	56.1	128	9.7	1075
SM6T30A	SM6T30CA	ER	MR	5	25 6	28 5	30	31.5	1	41.4	14 5	53.5	134	9.7	1075
SM6T33	SM6T33C	ES	MS	5	26 8	29 7	33	36 3	1	47 7	12 5	61 7	117	9 8	1000
SM6T33A	SM6T33CA	ET	MT	5	28.2	31.4	33	34.7	1	45 7	13 1	59	122	9 8	1000
SM6T36	SM6T36C	EU	MU	5	29.1	32.4	36	39 6	1	52	11 5	67.3	107	9 9	950
SM6T36A	SM6T36CA	EV	MV	5	30.8	34 2	36	37.8	1	49 9	12	64 3	112	9 9	950
SM6T39	SM6T39C	EW	MW	5	31.6	35.1	39	42.9	1	56 4	10 6	73	99	10 0	900
SM6T39A	SM6T39CA	EX	MX	5	33.3	37.1	39	41	1	53.9	11.1	69.7	103	10 0	900
SM6T68	SM6T68C	FP	NP	5	55.1	61 2	68	74.8	1	98	6 1	127	57	10.4	625
SM6T68A	SM6T68CA	FQ	NQ	5	58.1	64 6	68	71.4	1	92	6.5	121	59.5	10.4	625
SM6T100	SM6T100C	FX	NX	5	81	90	100	110	1	144	4 2	187	38.5	10 6	500
SM6T100A	SM6T100CA	FY	NY	5	85 5	95	100	105	1	137	4.4	178	40 5	10.6	500
SM6T150	SM6T150C	GK	OK	5	121	135	150	165	1	215	2 8	277	26	10 8	400
SM6T150A	SM6T150CA	GL	OL	5	128	143	150	158	1	207	2 9	265	27.2	10 8	400
SM6T200	SM6T200C	GT	OT	5	162	180	200	220	1	287	2.1	370	19 4	10 8	350
SM6T200A	SM6T200CA	GU	OU	5	171	190	200	210	1	274	2 2	353	20 4	10 8	350
SM6T220		GV		5	178	198	220	242	1	316	1.9	406	17 7	10.8	330
SM6T220A		GW		5	188	209	220	231	1	301	2	388	18.6	10.8	330

* Pulse test $t_p \leq 50$ ms $\delta < 2$ %

** Divide these values by 2 for bidirectional types

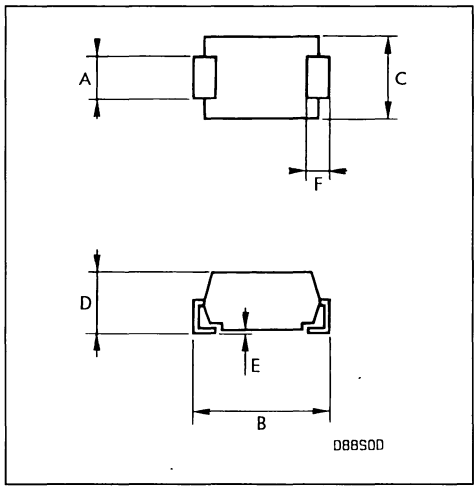
For bidirectional types, electrical characteristics apply in both directions

ORDER CODE



PACKAGE MECHANICAL DATA

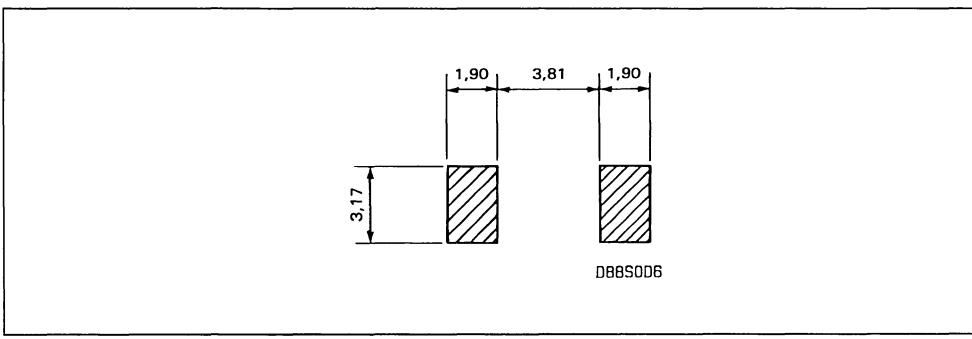
SOD 6 Plastic



Ref.	Millimetres		Inches	
	Min.	Max.	Min.	Max.
A	2.8	3.2	0.110	0.126
B	6.0	6.4	0.236	0.252
C	3.8	4.2	0.150	0.165
D	2.5	3.1	0.098	0.122
E	–	0.1	–	0.004
F	0.9	1.3	0.035	0.051

Laser marking
The logo indicates cathode for unidirectional types.

FOOT PRINT DIMENSIONS (Millimeters)



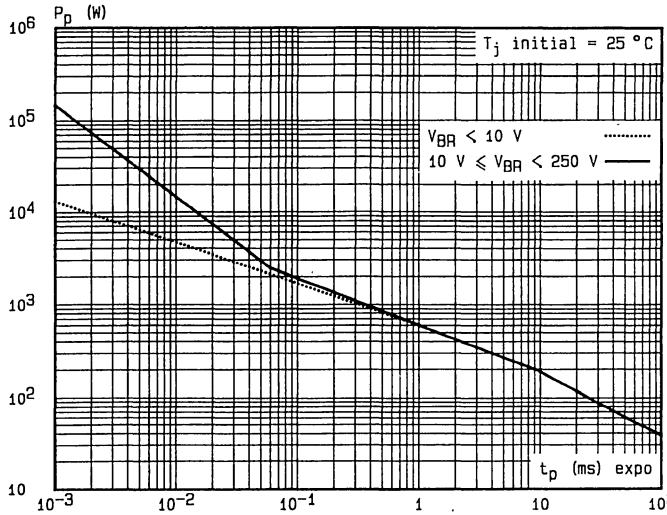


Fig.1 - Peak pulse power versus exponential pulse duration.

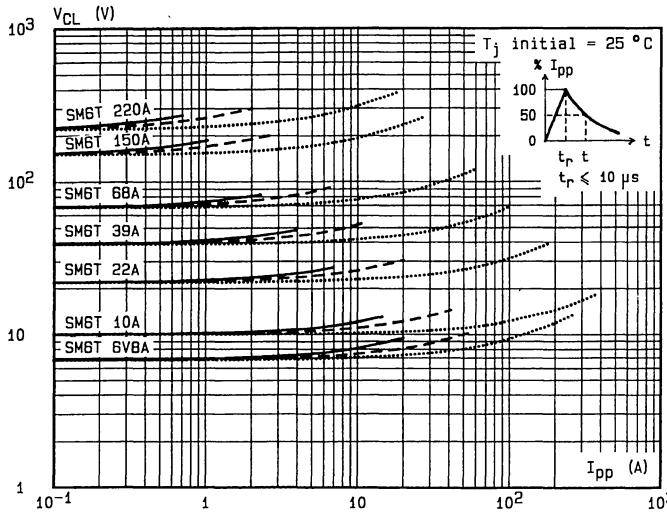


Fig.2 - Clamping voltage versus peak pulse current.
exponential waveform t = 20 µs ·····
t = 1 ms – – –
t = 10 ms ——

Note : The curves of the figure 2 are specified for a junction temperature of 25 °C before surge. The given results may be extrapolated for other junction temperatures by using the following formula : $\Delta V_{(BR)} = \alpha_{T(V(BR))} \times [T_j - 25] \times V_{(BR)}$
For intermediate voltages, extrapolate the given results.

D88SM6TP4

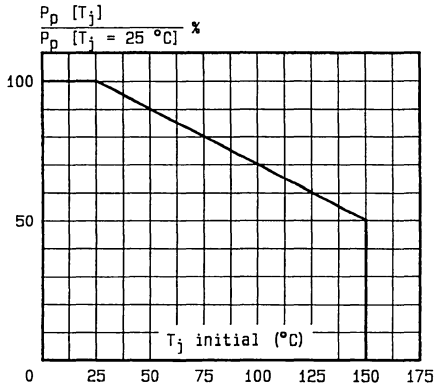


Fig.3 - Allowable power dissipation versus junction temperature.

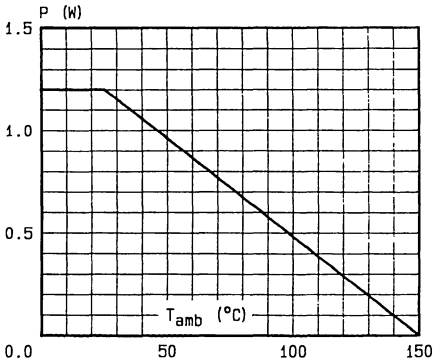


Fig.4 - Power dissipation versus ambient temperature.

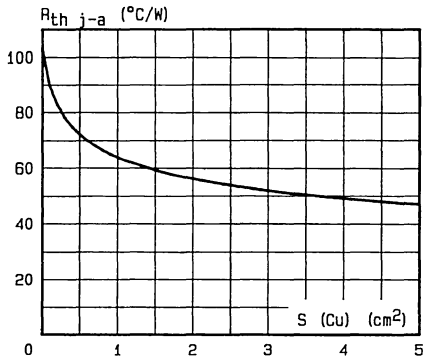


Fig.5 - Thermal resistance junction-ambient versus Cu surface (printed circuit).

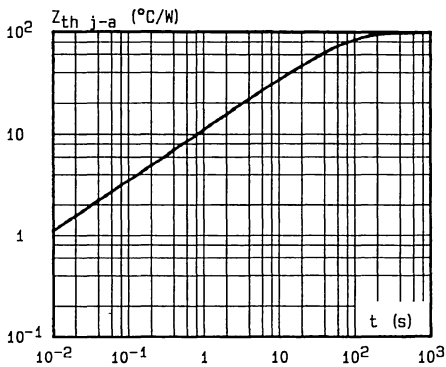


Fig.6 - Transient thermal impedance junction-ambient versus pulse duration.

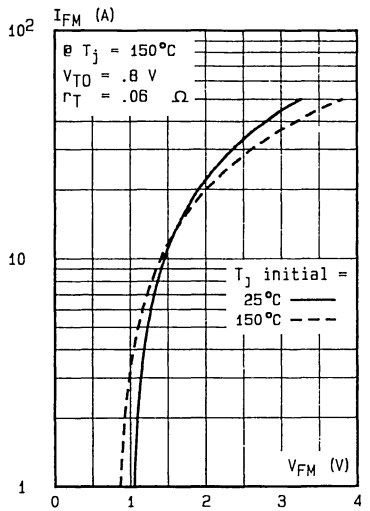


Fig.7 - Peak forward current versus peak forward voltage drop (typical values for unidirectional types).

D88SM6TP5

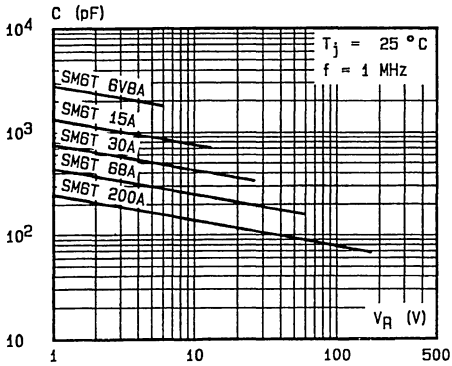


Fig.8a - Capacitance versus reverse applied voltage for unidirectional types (typical values).

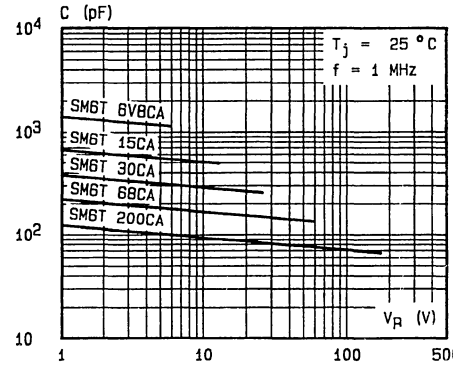


Fig.8b - Capacitance versus reverse applied voltage for bidirectional types (typical values).

D88SM6TP6

SM15T6V8, A → 220, A
SM15T6V8C, A → 200C, A

UNI-AND BIDIRECTIONAL TRANSIENT VOLTAGE SUPPRESSORS

- HIGH SURGE CAPABILITY :
  1.5 kW / 1 ms EXPO
- VERY FAST CLAMPING TIME :
  1 ps FOR UNIDIRECTIONAL TYPES
  5 ns FOR BIDIRECTIONAL TYPES
- LARGE VOLTAGE RANGE :
  5.5 V → 188 V
- ORDER CODE :
  TYPE NUMBER FOR UNIDIRECTIONAL TYPES, TYPE NUMBER + SUFFIX C FOR BIDIRECTIONAL TYPES

SOD 15
(Plastic)

SURFACE MOUNT TRANSIL FEATURES

- A PERFECT PICK AND PLACE BEHAVIOUR
- AN EXCELLENT ON BOARD STABILITY
- A FULL COMPATIBILITY WITH BOTH GLUING AND PASTE SOLDERING TECHNOLOGIES
- BODY MARKED WITH TYPE CODE AND LOGO
- STANDARD PACKAGING : 12 mm TAPE (EIA STD. RS481)
- TINNED COPPER LEADS
- HIGH TEMPERATURE RESISTANT RESIN

DESCRIPTION

Transient voltage suppressor diodes especially useful in protecting integrated circuits, MOS, hybrids and other voltage-sensitive semiconductors and components.

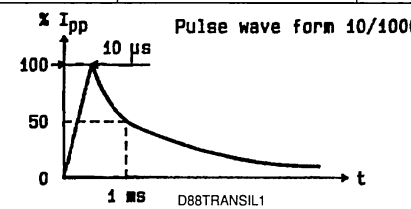
ABSOLUTE RATINGS (limiting values)

Symbol	Parameter		Value	Unit
P_p	Peak Pulse Power for 1 ms Exponential Pulse	T_j Initial = 25 °C See note 1	1500	W
P	Power Dissipation on Infinite Heatsink	T_{amb} = 25 °C	1.7	W
I_{FSM}	Non Repetitive Surge Peak Forward Current for Unidirectional Types	T_j Initial = 25 °C t = 10 ms	150	A
T_{stg} T_j	Storage and Operating Junction Temperature Range		– 65 to 175 150	°C °C
T_L	Maximum Lead Temperature for Soldering During 10 s		260	°C

THERMAL RESISTANCE

Symbol	Parameter	Value	Unit
$R_{th(j-l)}$	Junction-leads	10	°C/W

Note : 1. For surges upper than the maximum values, the diode will present a short-circuit anode-cathode



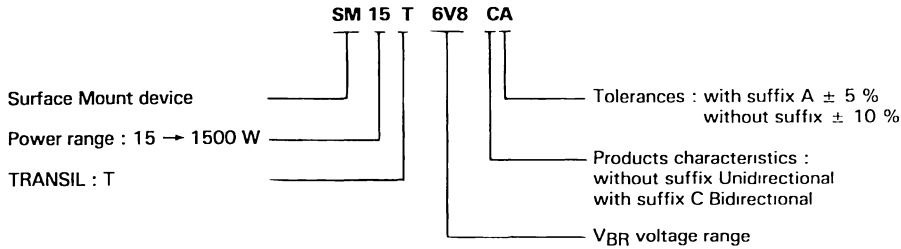
ELECTRICAL CHARACTERISTICS (T_j = 25 °C)

Symbol	Parameter		Value
V_{RM}	Stand-off Voltage		See tables
$V_{(BR)}$	Breakdown Voltage		
$V_{(CL)}$	Clamping Voltage		
I_{pp}	Peak Pulse Current		
α_T	Temperature Coefficient of $V_{(BR)}$		
C	Capacitance		
$t_{clamping}$	Clamping Time (0 volt to $V_{(BR)}$)	Unidirectional Types	1 ps max.
		Bidirectional Types	5 ns max.

Types		Marking		I_{RM} @ V_{RM} max.		$V_{(BR)}$* @ I_R (V)				$V_{(CL)}$ @ I_{pp} max. 1ms expo		$V_{(CL)}$ @ I_{pp} max. 8-20µs expo		α_T max.	C** typ. V_R=0 f=1MHz
Unidirectional	Bidirectional	Unidirectional	Bidirectional	(µA)	(V)	min.	nom.	max.	(mA)	(V)	(A)	(V)	(A)	(10^{-4}/°C)	(pF)
SM15T6V8	SM15T6V8C	MDD	BDD	1000	5.5	6.12	6.8	7 48	10	10.8	139	14	714	5.7	9500
SM15T6V8A	SM15T6V8CA	MDE	BDE	1000	5.8	6.45	6.8	7.14	10	10.5	143	13 4	746	5.7	9500
SM15T7V5	SM15T7V5C	MDF	BDF	1000	6.05	6.75	7.5	8.25	10	11.7	128	15.2	660	6.1	8500
SM15T7V5A	SM15T7V5CA	MDG	BDG	1000	6 4	7.13	7.5	7.88	10	11.3	132	14.5	690	6 1	8500
SM15T10	SM15T10C	MDN	BDN	1 0	8.1	9.0	10	11	1	15	100	19.5	928	7.3	7000
SM15T10A	SM15T10CA	MDP	BDP	1 0	8.55	9.5	10	10.5	1	14.5	103	18 6	968	7.3	7000
SM15T12	SM15T12C	MDS	BDS	5	9.72	10.8	12	13 2	1	17.3	87	22.7	793	7.8	6000
SM15T12A	SM15T12CA	MDT	BDT	5	10 2	11 4	12	12 6	1	16 7	90	21 7	829	7 8	6000
SM15T15	SM15T15C	MDW	BDW	5	12.1	13.5	15	16 5	1	22	68	28 4	634	8.4	5000
SM15T15A	SM15T15CA	MDX	BDX	5	12 8	14 3	15	15.8	1	21.2	71	27.2	662	8.4	5000
SM15T18	SM15T18C	MED	BED	5	14.5	16.2	18	19.8	1	26.5	56 5	34	529	8.8	4300
SM15T18A	SM15T18CA	MEE	BEE	5	15.3	17.1	18	18.9	1	25.2	59.5	32.5	554	8 8	4300
SM15T22	SM15T22C	MEH	BEH	5	17.8	19.8	22	24.2	1	31.9	47	41.2	437	9.2	3700
SM15T22A	SM15T22CA	MEK	BEK	5	18.8	20.9	22	23.1	1	30.6	49	39.3	458	9.2	3700
SM15T24	SM15T24C	MEL	BEL	5	19.4	21.6	24	26.4	1	34.7	43	44.9	401	9.4	3500
SM15T24A	SM15T24CA	MEM	BEM	5	20.5	22 8	24	25.2	1	33.2	45	42.8	421	9.4	3500
SM15T27	SM15T27C	MEN	BEN	5	21 8	24.3	27	29 7	1	39 1	38.5	50.5	356	9.6	3200
SM15T27A	SM15T27CA	MEP	BEP	5	23 1	25 7	27	28 4	1	37.5	40	48.3	373	9.6	3200
SM15T30	SM15T30C	MEQ	BEQ	5	24.3	27	30	33	1	43 5	34.5	56.1	321	9.7	2900
SM15T30A	SM15T30CA	MER	BER	5	25 6	28 5	30	31.5	1	41.4	36	53 5	336	9 7	2900
SM15T33	SM15T33C	MES	BES	5	26.8	29.7	33	36.3	1	47.7	31.5	61 5	292	9 8	2700
SM15T33A	SM15T33CA	MET	BET	5	28.2	31.4	33	34 7	1	45.7	33	59	305	9 8	2700
SM15T36	SM15T36C	MEU	BEU	5	29.1	32.4	36	39.6	1	52	29	67 3	267	9.9	2500
SM15T36A	SM15T36CA	MEV	BEV	5	30.8	34.2	36	37.8	1	49.9	30	64.3	280	9.9	2500
SM15T39	SM15T39C	MEW	BEW	5	31.6	35.1	39	42.9	1	56.4	26.5	73	246	10.0	2400
SM15T39A	SM15T39CA	MEX	BEX	5	33.3	37.1	39	41	1	53 9	28	69.7	258	10.0	2400
SM15T68	SM15T68C	MFN	BFN	5	55.1	61.2	68	74.8	1	98	15.3	127	142	10.4	1550
SM15T68A	SM15T68CA	MFP	BFP	5	58.1	64 6	68	71 4	1	92	16 3	121	148	10.4	1550
SM15T100	SM15T100C	MFW	BFW	5	81	90	100	110	1	144	10 4	187	96	10.6	1150
SM15T100A	SM15T100CA	MFX	BFX	5	85 5	95	100	105	1	137	11	178	101	10.6	1150
SM15T150	SM15T150C	MGH	BGH	5	121	135	150	165	1	215	7	277	65	10.8	850
SM15T150A	SM15T150CA	MGK	BGK	5	128	143	150	158	1	207	7 2	265	68	10.8	850
SM15T200	SM15T200C	MGU	BGU	5	162	180	200	220	1	287	5 2	370	48 5	10 8	675
SM15T200A	SM15T200CA	MGV	BGV	5	171	190	200	210	1	274	5.5	353	51	10.8	675
SM15T220		MGW		5	175	198	220	242	1	344	4.3	406	44.5	10.8	625
SM15T220A		MGX		5	185	209	220	231	1	328	4.6	388	46.5	10.8	625

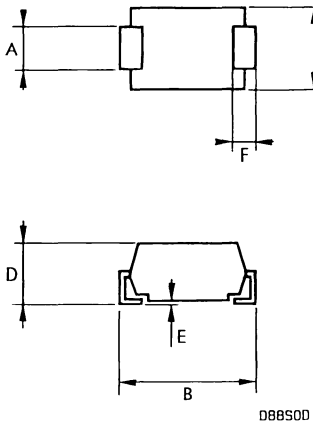
* Pulse test $t_p \leq 50$ ms $\delta < 2$ %.
** Divide these values by 2 for bidirectional types.
For bidirectional types, electrical characteristics apply in both directions.

ORDER CODE



PACKAGE MECHANICAL DATA

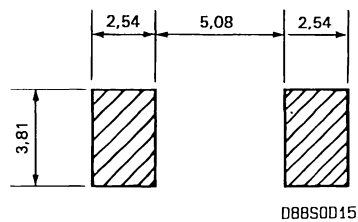
SOD 15 Plastic



Ref.	Millimetres		Inches	
	Min.	Max.	Min.	Max.
A	2.8	3.2	0.110	0.126
B	7.6	8.0	0.300	0.315
C	4.8	5.2	0.190	0.200
D	2.5	3.1	0.098	0.122
E	–	0.1	–	0.004
F	1.3	1.7	0.051	0.067

Laser marking.
The logo indicates cathode for unidirectional types.

FOOT PRINT DIMENSIONS (Millimeters)



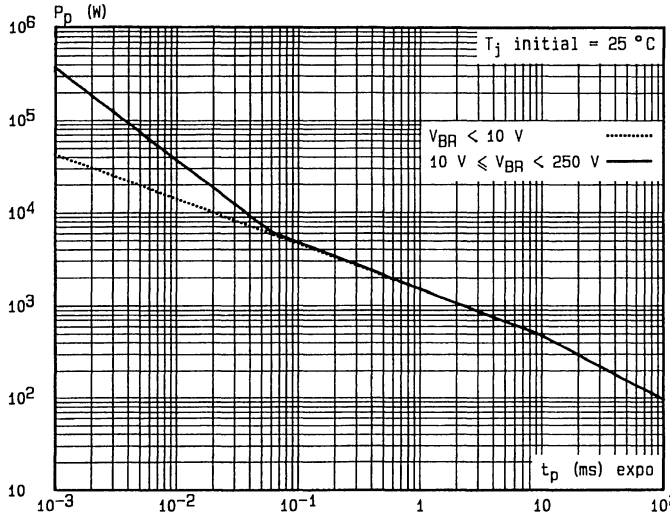


Fig.1 - Peak pulse power versus exponential pulse duration.

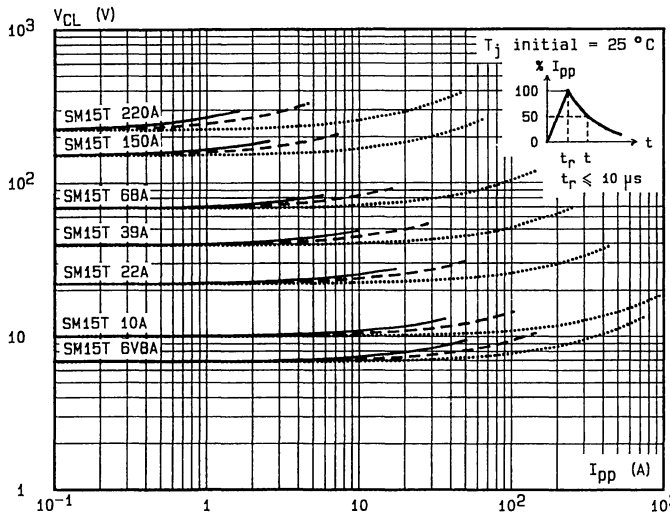


Fig.2 - Clamping voltage versus peak pulse current.
exponential waveform t = 20 µs ·····
t = 1 ms – – –
t = 10 ms ——

Note : The curves of the figure 2 are specified for a junction temperature of 25 °C before surge. The given results may be extrapolated for other junction temperatures by using the following formula : $\Delta V_{(BR)} = \alpha_{T(V(BR))} \times [T_j - 25] \times V_{(BR)}$
For intermediate voltages, extrapolate the given results.

D88SM15TP4

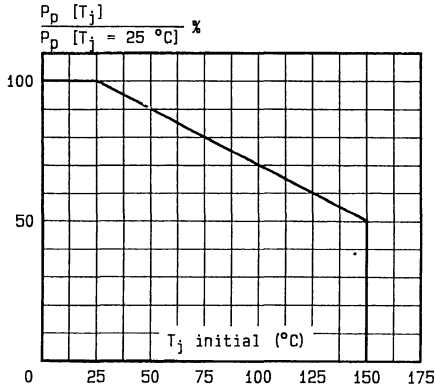


Fig.3 - Allowable power dissipation versus junction temperature.

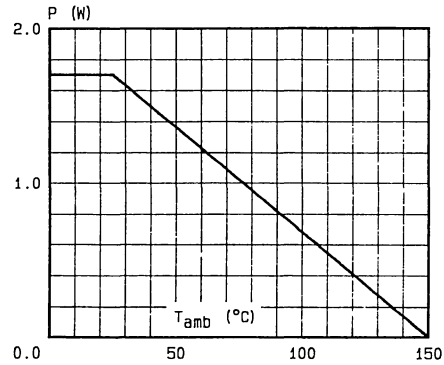


Fig.4 - Power dissipation versus ambient temperature.

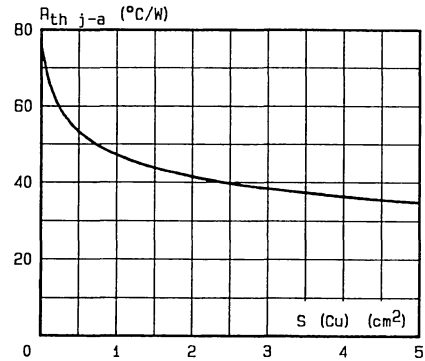


Fig.5 - Thermal resistance junction-ambient versus Cu surface (printed circuit).

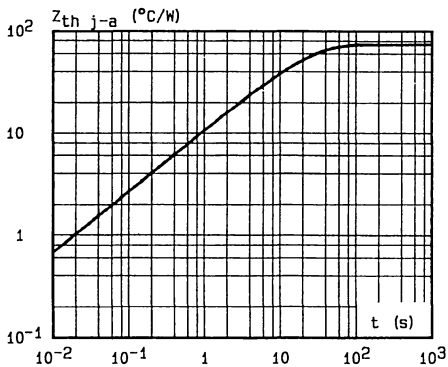


Fig.6 - Transient thermal impedance junction-ambient versus pulse duration.

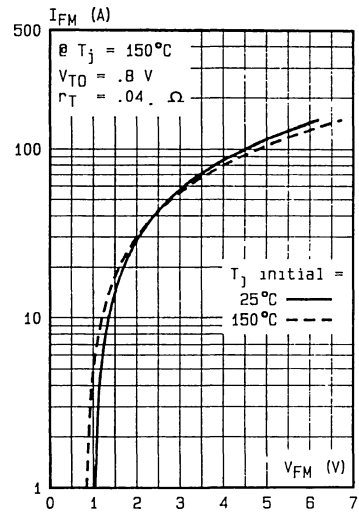


Fig.7 - Peak forward current versus peak forward voltage drop (typical values for unidirectional types).

D88SM15TP5

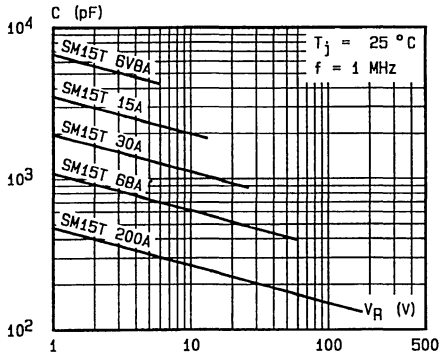


Fig.8a - Capacitance versus reverse applied voltage for unidirectional types (typical values).

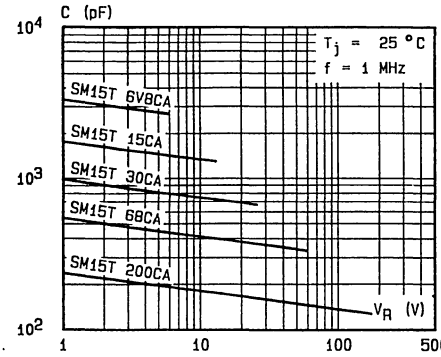


Fig.8b - Capacitance versus reverse applied voltage for bidirectional types (typical values).

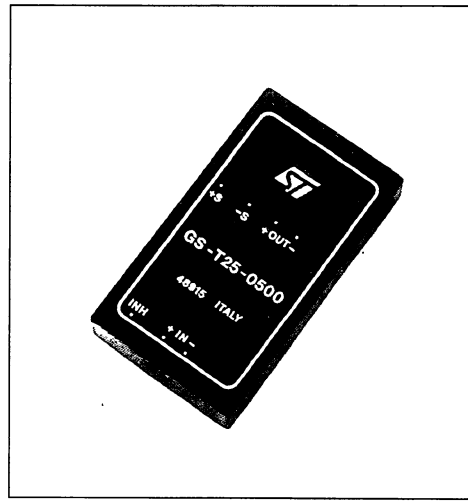
D88SM15TP6

SGS-THOMSON MICROELECTRONICS

GS-T25/30 FAMILY

25-30 WATT DC-DC CONVERTERS

- MTBF IN EXCESS OF 1M HOURS AT + 45°C AMBIENT TEMPERATURE
- PCB OR CHASSIS MOUNTABLE
- NO EXTERNAL COMPONENT REQUIRED
- SIX SIDED CASE
- HIGH EFFICIENCY (see data)
- 500 V_{DC} MINIMUM ISOLATION
- WIDE INPUT VOLTAGE RANGE (36 to 72V)
- REVERSE INPUT POLARITY PROTECTION
- PEAK INPUT OVERVOLTAGE WITHSTAND (90V/1 sec.)
- MINIMIZED INPUT REFLECTED CURRENT
- SOFT START
- REMOTE INHIBIT/ENABLE WITH LOW STAND BY CURRENT
- REMOTE OUTPUT VOLTAGE SENSE
- NON LATCHING PERMANENT SHORT CIRCUIT PROTECTION
- LATCHING OUTPUT OVERVOLTAGE PROTECTION
- PARALLEL OPERATION
- NO DERATING OVER THE TEMPERATURE RANGE



DESCRIPTION

The GS-T25/30 series is a family of isolated DC-DC converters specially designed for Telecom application, available in different output voltages : 5V ; 6V ; 12V and 15V. (OTHER OUTPUT VOLTAGES available on request).

The output power is in the range of 25W to 30W.

To ensure very long life, these converters don't use any electrolytic capacitor or optoelectronic feedback system.

The converters permit paralleling of outputs.

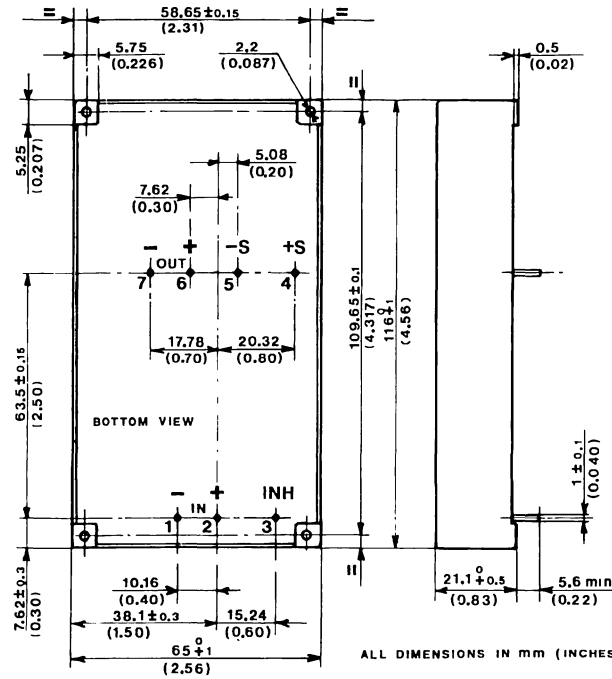
PRODUCTS FAMILY

Order Number	Output Voltage	Output Current	Output Power
GS-T25-0500	5V	5A	25W
GS-T27-0600	6V	4.5A	27W
GS-T30-1200	12V	2.5A	30W
GS-T30-1500	15V	2A	30W

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_i	DC Input Voltage	34 to 72	V
V_{ipk}	Input Transient Overvoltage (T ≤ 1sec.)	90	V
V_{ir}	Input Reverse Voltage	100	V
T_{stg}	Storage Temperature Range	– 55 to 105	°C
T_{op}	Operating Temperature Range	– 25 to 71	°C

CONNECTION DIAGRAM AND MECHANICAL DATA (bottom view)



PIN FUNCTIONS

Pin	Function
1	– Input.
2	+ Input. Unregulated input voltage (typically 48V) must be applied between pin 1-2. The input section of the DC-DC converter is protected against reverse polarity by a series diode. No external fuse is required. Input is filtered by a Pi network.
3	Remote inhibit/enable logically compatible with CMOS or open collector TTL. The converter is ON when the voltage applied to pin 3 is 1.8V_{DC} min or left open referenced to the pin 1. The converter is OFF for a control voltage lower than 1.2V_{DC}.
4	Sensing Positive. For connection to remote loads this pin allows voltage sensing to the load itself. TO BE CONNECTED TO PIN 6 WHEN REMOTE SENSING IS NOT USED.
5	Sensing Negative. See pin 4. TO BE CONNECTED TO PIN 7 WHEN REMOTE SENSING IS NOT USED.
6	+ Output.
7	– Output.

ELECTRICAL CHARACTERISTICS (Tamb = 25°C unless otherwise specified)

INPUT

Type			GS-T25-0500			GS-T27-0600			GS-T30-1200			GS-T30-1500			Unit
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max	
V_i	Input Voltage	Full Load	36	48	72	36	48	72	36	48	72	36	48	72	V
I_i	No Load Input Current	V_{IN} = 48V		15			15			15			20		mA
I_i	Full Load Input Current	V_{IN} = 48V		640			680			730			730		mA
I_{ir}	Input Reflected Current (sinusoidal)	V_{IN} = 48V/full Load		200			200			200			200		mApp
I_i	Input Short Circuit Current	V_{IN} = 48V		22			24			43			55		mA
I_{isb}	Input Stand by Current	V_{IN} = 48V V_3 = 0V		5			5			5			5		mA
V_{INHL}	Low Inhibit Voltage	V_{IN} = 48V, Full Load			1.2			1.2			1.2			1.2	V
V_{INHH}	High Enable Voltage	V_{IN} = 48V, Full Load	1.8 or open			1.8 or open			1.8 or open			1.8 or open			V
I_{INH}	Input Inhibit Current	V_{IN} = 48V, Full Load		1 8			1.8			1.8			1.8		mA

OUTPUT

Type			GS-T25-0500			GS-T27-0600			GS-T30-1200			GS-T30-1500			Unit
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
V_O	Output Voltage	V_{IN} = 48V Full Load	4.95	5.00	5.05	5.94	6.00	6 06	11 88	12 00	12 12	14.85	15.00	15.15	V
ΔV_O	Line Regulation	V_{IN} = 36V to 72V Full Load		± 0.001			± 0 001			± 0.001			± 0.001		%
ΔV_O	Load Regulation	V_{IN} = 48V Full Load to no Load		± 0.05			± 0 05			± 0 05			± 0.05		%
V_r	Ripple and Noise Voltage	V_{IN} = 48V Full Load		5			5			5			5		mVRMS
$V_{O\ OV}$	Output Overvoltage Protection	V_{IN} = 48V Full Load			6.8			8.2			15			18	V
ΔV_O	Remote Sense per Leg	V_{IN} = 36V			0.6			0.6			0.6			0.6	V
t_{ss}	Soft Start Time	V_{IN} = 48V Full Load		30			30			30			30		ms
I_o	Max Output Current	V_{IN} = 48V			5			4.5			2.5			2	A
I_{sck}	Output Current Limit	V_{IN} = 48V Overload		5.5			4.95			2.75			2 2		A
I_{osc}	Output Average Short Circuit Current	V_{IN} = 48V,		0.7			0.8			1.1			1.2		A

ELECTRICAL CHARACTERISTICS (continued)

OUTPUT (continued)

Type			GS-T25-0500			GS-T27-0600			GS-T30-1200			GS-T30-1500			Unit
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
T_{rt}	Transient Recovery Time	V_{IN} = 48V ΔI_o = 25% Step Load Change		75			75			75			75		µs
T_c	Temperature Coefficient	V_{IN} = 48V, Full Load ; Operating Temperature Range		+ 0 02			+ 0.02			+ 0.02			+ 0.02		%/°C

GENERAL

Type			GS-T25-0500			GS-T27-0600			GS-T30-1200			GS-T30-1500			Unit
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max	
η	Efficiency	V_{IN} = 36 to 72V Full Load		81			82			86			86		%
P_d	Power Dissipation in Short Circuit Condition	V_{IN} = 48V		1.06			1.15			2 06			2.6		W
V_{IS}	Isolation Voltage			500			500			500			500		V_{DC}
R_{IS}	Isolation Resistance			10^9			10^9			10^9			10^9		Ω
f_s	Switching Frequency	V_{IN} = 48V Full Load		150			150			150			150		kHz

The GS-T25/30 series of DC-DC converter has been designed to meet the demanding application of the Telecommunication industry.

Particular attention has been devoted to maximize the reliability of the converters as described in the following.

SYSTEM ARCHITECTURE

The switching push-pull current mode architecture has been adopted because :

- it allows large duty cycle (80%) so lowering the input peak current ;
- it minimizes the transformer flux imbalance (current mode cycle by cycle control) :
- it allows, because of its symmetry and together with a switching frequency of 150kHz, to minimize the inductance and capacitance values ;
- it offers exceptional performance in terms of line regulation because of the feedforward effect inherent to current mode control.

COMPONENT CHOICE

Because of the system architecture, ceramic or solid tantalum capacitors only are used.

In addition, the voltage regulation loop is closed by sensing directly the output voltage on the secondary side without any optocoupler feedback device.

Power MOS transistors with a current capability 30 times larger than maximum operating condition have been adopted as primary side switches ; voltage capability is 2.5 times higher than nominal condition.

Efficiency is maximized by lowering switching and conduction losses on the primary side and rectification losses on the secondary side by use of Schottky diodes on the GS-T25/27 models.

PACKAGE

The package is of die casted aluminum type that offers a typical thermal resistance case to ambient of 4°C/W.

This, together with the low power dissipation, allows to keep junction temperature of silicon devices at less than 100°C even for ambient temperature of 71°C with free air convection.

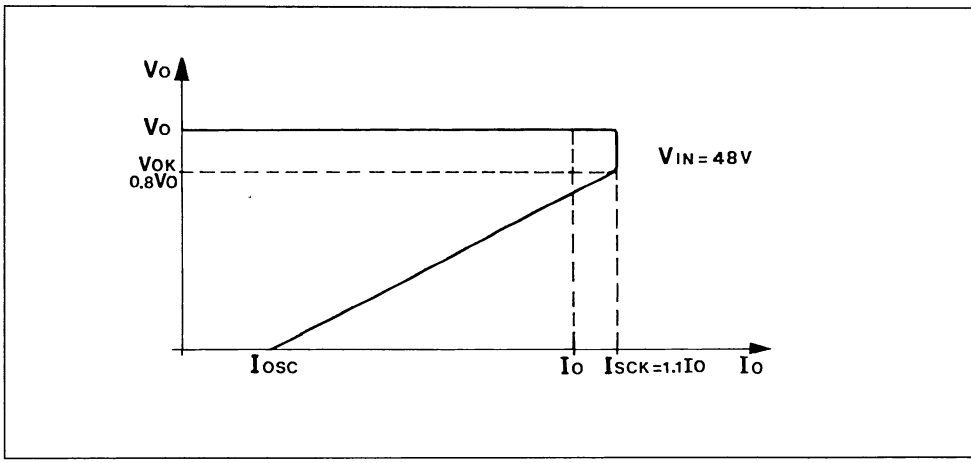
OVERLOAD PROTECTION

The overload protection has been designed so that two different objectives are met :

- parallel connection possibility, to increase available output regulated power ;
- reduction of available current during heavy overload and/or short circuit.

The typical diagram of this protection is shown in fig. 1.

Figure 1 : Typical Overload Protection.



During short circuit, current stresses on primary and secondary side are actually lower than in nominal condition.

Power dissipation inside the module is minimized.

OVERVOLTAGE PROTECTION

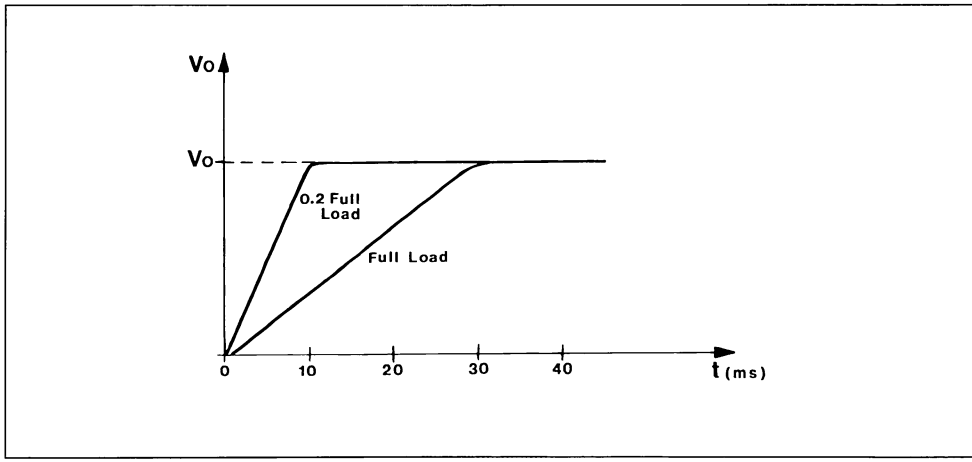
In case of output voltage higher than overvoltage limits, the DC-DC converter is shut down and it remains in a latching condition.

Current drain at the input is 20mA typically, so that this latching condition is not hazardous for the whole equipment where the DC-DC converter is used.

SOFT START

To avoid heavy inrush current the output voltage rise time is controlled as a function of the load condition : the larger the output current, the softer the output voltage rise. See fig. 2.

Figure 2 : Soft Start as a Function of the Output Current.



EFFICIENCY

The efficiency of these DC-DC converters is shown in fig. 3, 4, 5 and 6.

Figure 3.

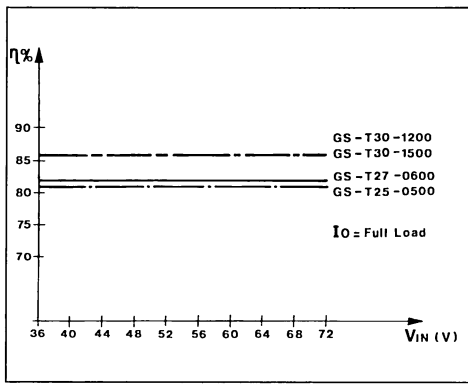


Figure 4.

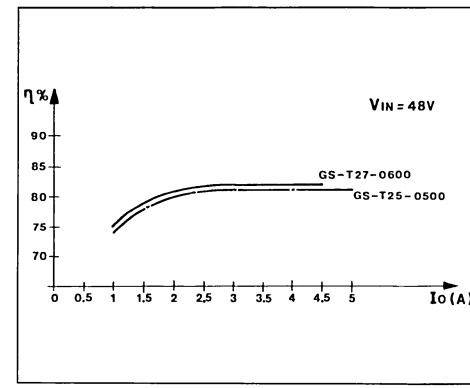


Figure 5.

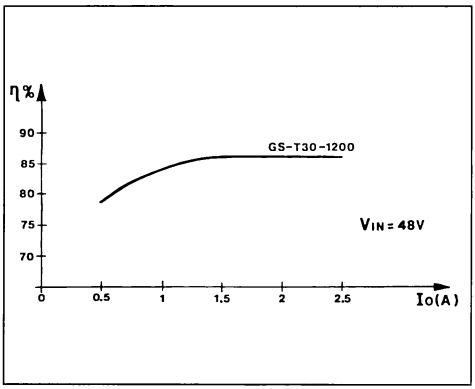
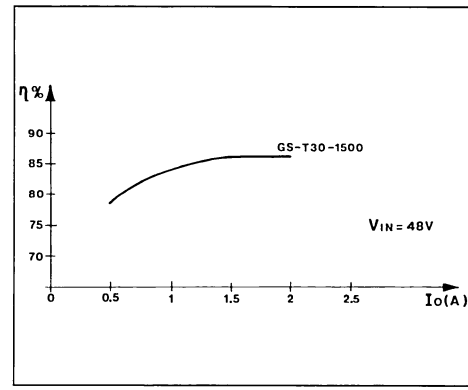


Figure 6.



APPLICATION NOTES

M088 DIGITAL SWITCHING MATRIX

BY ANGELO PARIANI

INTRODUCTION

The M088 DIGITAL SWITCHING MATRIX device can be used as a basic component in modern digital switching systems.

This Technical Note is a guide for designers who wish to use the M088 in their systems.

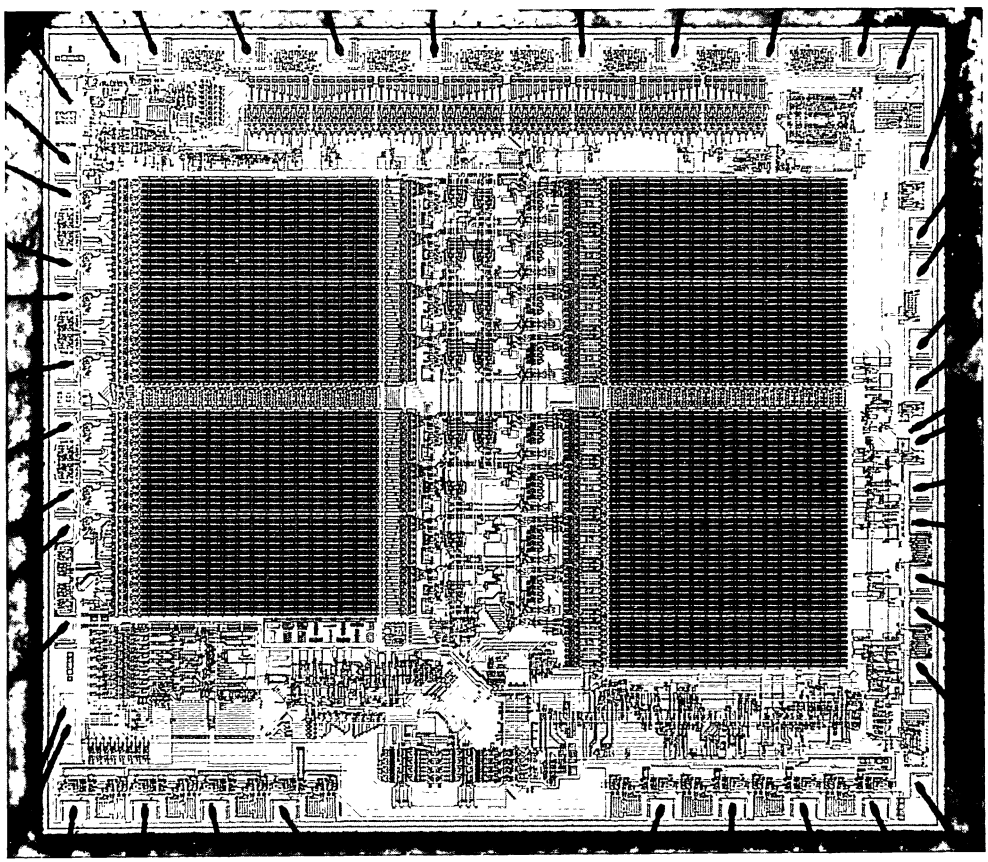
Section 1 contains introductory material in the field of digital switching and can be quickly passed over by experienced designers.

The main characteristics of the M088 are shown in Section 2.

Sections 3 and 4 describe, respectively, the internal structure, and the various functions which may be implemented.

Some detailed material concerning timing and some important services are examined in Section 5.

Section 6 is dedicated to applications. Another component, the M116, used in this field, are introduced in this section ; of particular note is the fact that the M116 is a digital device which realizes conference functions.



1. DIGITAL SWITCHING TUTORIAL

WHAT IS A DIGITAL SWITCHING MATRIX (DSM) ?

A Digital Switching Matrix is a device which permits switching a certain number of signals among themselves.

The signals to be switched can either be digital or analog ; in the latter case, digitalization of these signals must be provided before switching takes place.

Digitalization takes place in three stages :

a) band limiting (by a low pass filter) ;

b) sampling ;

c) digital coding.

PULSE CODE MODULATION (PCM)

The technique of digitalizing signals used in telephonic applications is called PCM.

The signal to be digitalized is sampled every 125 µs, in other words, with a frequency equal to 8 KHz since, according to the Nyquist law, the sampling frequency must be greater or equal to twice the maximum frequency of the analog signal being sampled. As is well known in telephony, this frequency is less than 4 KHz.

Based on input signal sampling (see fig. 1-1), the coding links a given sample to an 8-bit binary number.

Thus, the number of discrete levels becomes $2^8 = 256$.

Non-linear coding laws are used. The main ones are the two following :

- Mu law used in the USA, Canada and Japan ;
- A law used in Europe, South America, Australia and Africa (see fig. 1-2).

Since the sampling frequency is 8 KHz, the digitalized signal will be made up of a number of bits per second equal to (8 · 8000) = 64000 bit/s.

TIME DIVISION MULTIPLEXER (TDM)

TDM is a technique which permits merging various digital signals into a single high velocity signal. Many stages of switching will, thus, become easier.

Fig. 1-3 presents a diagram of the TDM principle.

TDM is based on the serializer, which accepts PCM signals at the input, and provides them at the output, accessed cyclically.

Each input channel is linked to a time slot, and is thus fixed precisely in the serialized output stream.

Figure 1.1 : SAMPLING & CODING. The Analog Signal to be digitalized is First Bandwidth limited (fig. 1.1a) Then Sampled at a Frequency f_S (fig. 1.1b). The Resulting Periodic Sequence of Samples is shown in Fig. 1.1c. Each Sample is then replaced with an 8–Bit Word representing the Amplitude (fig. 1.1d).

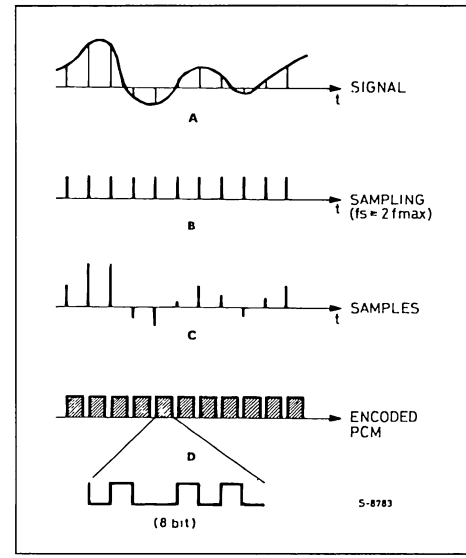
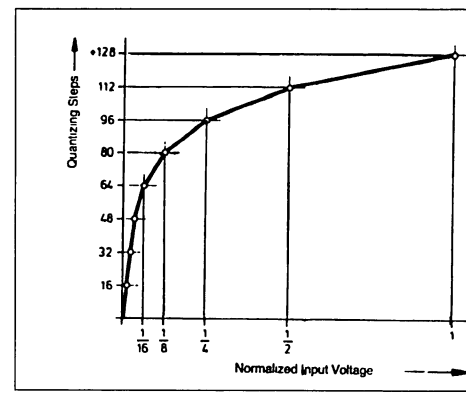


Figure 1.2 : The Quantization Curve for A-law Limited to Positive Samples. Each Group of 16 Steps is Contained in a Segment and the Normalized Values of the Input Signal Corresponding to the Extremes of Each Segment are One Half of Each Other.



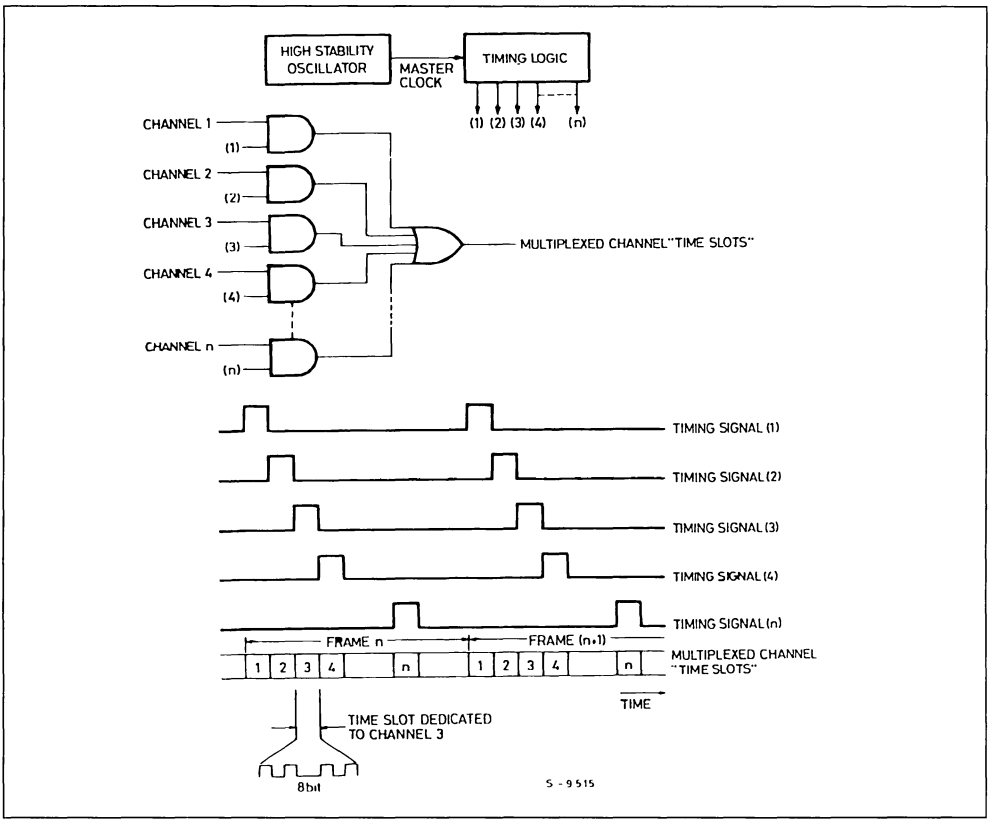
A very stable oscillator provides the master clock and all the timing functions used in the multiplexer.

The international standards for the TDM are two, namely :

a) the North American Standard (PCM 24 Transmission System) ;

b) the European Primary System (PCM 30 Transmission System) ;

Figure 1.3 : The Basic Principle of Time Division Multiplexing (TDM). Data from n Independent Channels are Compressed and Transferred to a Single Output. Each Channel Outputs Its Data in Separate Time Slots Defined by a Timing Circuit.



THE NORTH AMERICAN STANDARD (PCM 24)

Fig. 1-4 presents the PCM 24 Transmission System frame format.

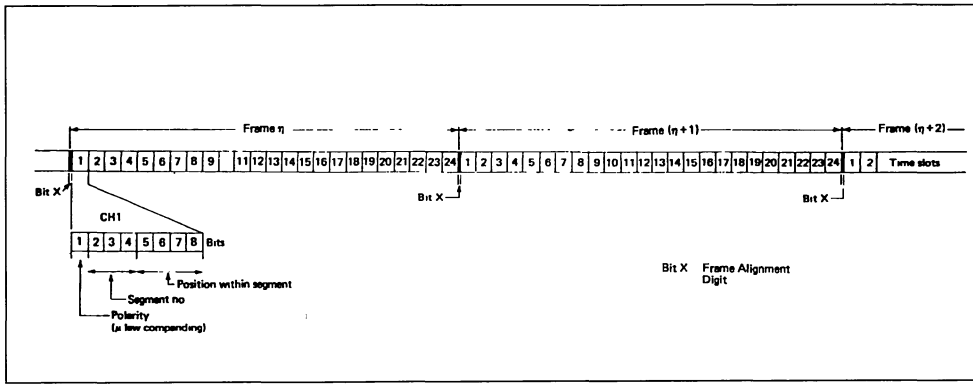
Each of the 24 channels has already been sampled at 8 KHz and coded, using Mu law with 8-bit words.

Messages reaching the channels are word interleaved, forming an uninterrupted sequence of 192 bits.

A single alignment framing digit (bit X) is inserted at the beginning of each sequence ; thus the total number of digits in a frame is 193. The velocity of the signal in bit/s is thus (8000 · 193) = 1544 Kbit/s.

In certain applications, usually PABX, the Extra bit (bit X) is omitted. In this last case the velocity of the signal becomes (8000 · 192) = 1536 Kbit/s.

Figure 1.4 : Frame Format of the Bell T1 (PCM24) System. Each Frame Contains 24 Channels PLus One Signalling Bit (bit X). This Format is Used in the USA, Canada and Japan.



THE EUROPEAN PRIMARY SYSTEM (PCM 30)

Fig. 1-5 shows the European Primary System frame format.

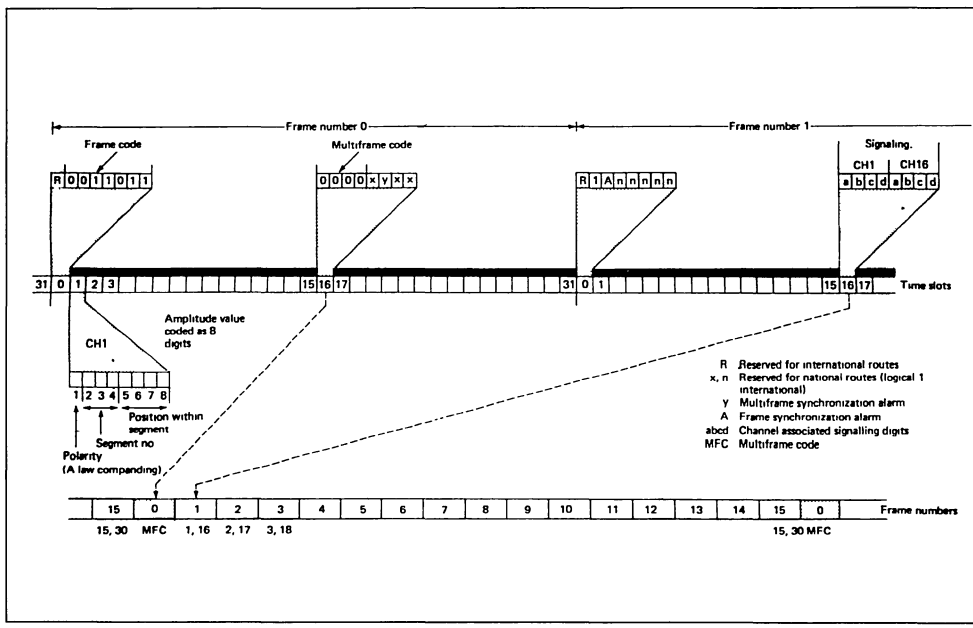
TDM combines 30 voice channels, sampled at 8 KHz, and coded using A law with 8-bit words.

Various channels messages are combined by word interleaving ; thirty 8-bit words are inserted in a frame with 32 time slots, numbered from 0 to 31.

Two of the slots (0 and 16) are used for frame alignment and signalling.

Each frame has (8 · 32) = 256 bits, and its velocity is (8000 · 256) = 2048 Kbit/s.

Figure 1.5 : Frame Format of the European System (PCM30). Each Frame contains 32 Channels of which two are dedicated to signalling. This Format is used in Europe, Latin America, Australia and Africa.



TIME AND SPACE DIVISION SWITCHING

Fig. 1-6 represents, using blocks, a digital switching system. Individual analog lines are applied to a multiplexer, which provides for their digitalization and merges them into a frame.

The various frames are transmitted to the switching matrix which carries out exactly the switching function, building various output frames as required.

These frames are transmitted to a demultiplexer which separates them into single channels, which, after conversion from digital to analog, are transmitted to the respective analog output lines.

Fig. 1-6 presents an example : subscriber S1-5 wishes to be connected to subscriber S8-11 ; S1-8 with S4-10.

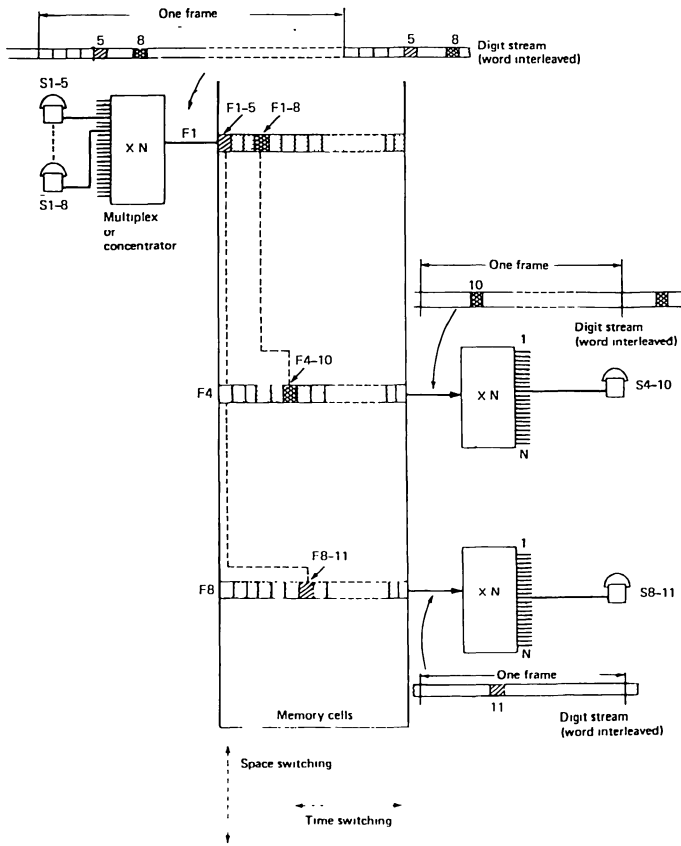
The connection operation between S1-5 and S8-11 involves two operations :

1) transfer of information from layer F1 to layer F8 (space division switching) ;
2) transfer from position 5 to 11 (time division switching).

Likewise, the connection between S1-8 and S4-10 involves space switching between F1 and F4, and time switching between positions 8 and 10.

SGS THOMSON digital switching matrixes operate, using this technique of time and space division switching, permitting switching without blocking, in other words, simultaneously of 256 channels.

Figure 1.6 : Space-and-Time-switching Digitally encoded Signals.



2. INTRODUCTION TO THE M088 DSM

GENERAL DESCRIPTION

The M088 device implements a non-blocking digital switching matrix, which operates with a maximum of 256 x 256 channels.

These channels are applied and extracted from the device, using 8 PCM frames at 2048 Kbit/s, each containing 32 channels.

The M088 can connect each input channel with, or disconnect it from, any output channel in addition to carrying out other functions described in Section 4.

It can also be used at lower velocity, for example, to switch 192 x 192 channels, organized in eight frames of 24 channels each, at 1544 Kbit/s, using the North American Standard (PCM 24) or at 1536 Kbit/s.

Finally, there is no prohibition against using the device for non-standard applications, for example, in the field of Data Communications. A few examples are cited in Section 6.

KEY FEATURES

- A 256 input and 256 output channels digital switching matrix ;
- A building block designed for large capacity electronic exchanges, subsystems, voice-data PABXs ;
- European Primary System compatible (32 channels per frame) ;
- North American Standard (T1 System) compatible (24 channels par frame) (*) ;
- PCM input and output mutually compatible ;
- Actual input-output channel connections stored and modified using an on-chip 8-bit parallel microprocessor interface.
- 6 main functions or instructions available ;
- 5-volt power supply with internal-generated bias voltage ;
- MOS and TTL input/output levels compatible ;
- Constructed with SGS THOMSON N-Channel silicon gate high-density MOS

(*) For further information, see below, Section 6.

3. M088 INTERNAL STRUCTURE

The component includes a Speech Memory, Control Memory, circuits for Serial to Parallel Conversion of incoming PCM links and for Parallel to Serial Conversion of the outgoing PCM links and a Bidirectional Interface for an 8-bit microprocessor (e. g., Z80 or Z8). In addition, the M088 performs other useful functions, such as Byte Insertion and Extraction, Addressing Memory Reading and 0 Channel Extraction. Referring to Fig. 3-1, the following functional blocks can be distinguished :

- Time Base
- Serial Parallel Converter for the PCM input links
- Speech Memory
- Control Memory
- Internal PCM Bus
- Parallel Serial Converter for the PCM output links
- Control and Interface Logic to and from the µP

TIME BASE

The time base generates the internal synchronous timing signals, using only two external signals, the clock (4.096 MHz) and the frame synchronism (8 KHz), supplied to the corresponding external pins of the device (CK and SYNC pins). The time base provides two ring counters, generating two sets of timing signals (e1 to e8 and u1 to u8), used for Serial to Parallel Conversion of input time slots and Parallel to Serial reconversion of output PCM time slots, respectively.

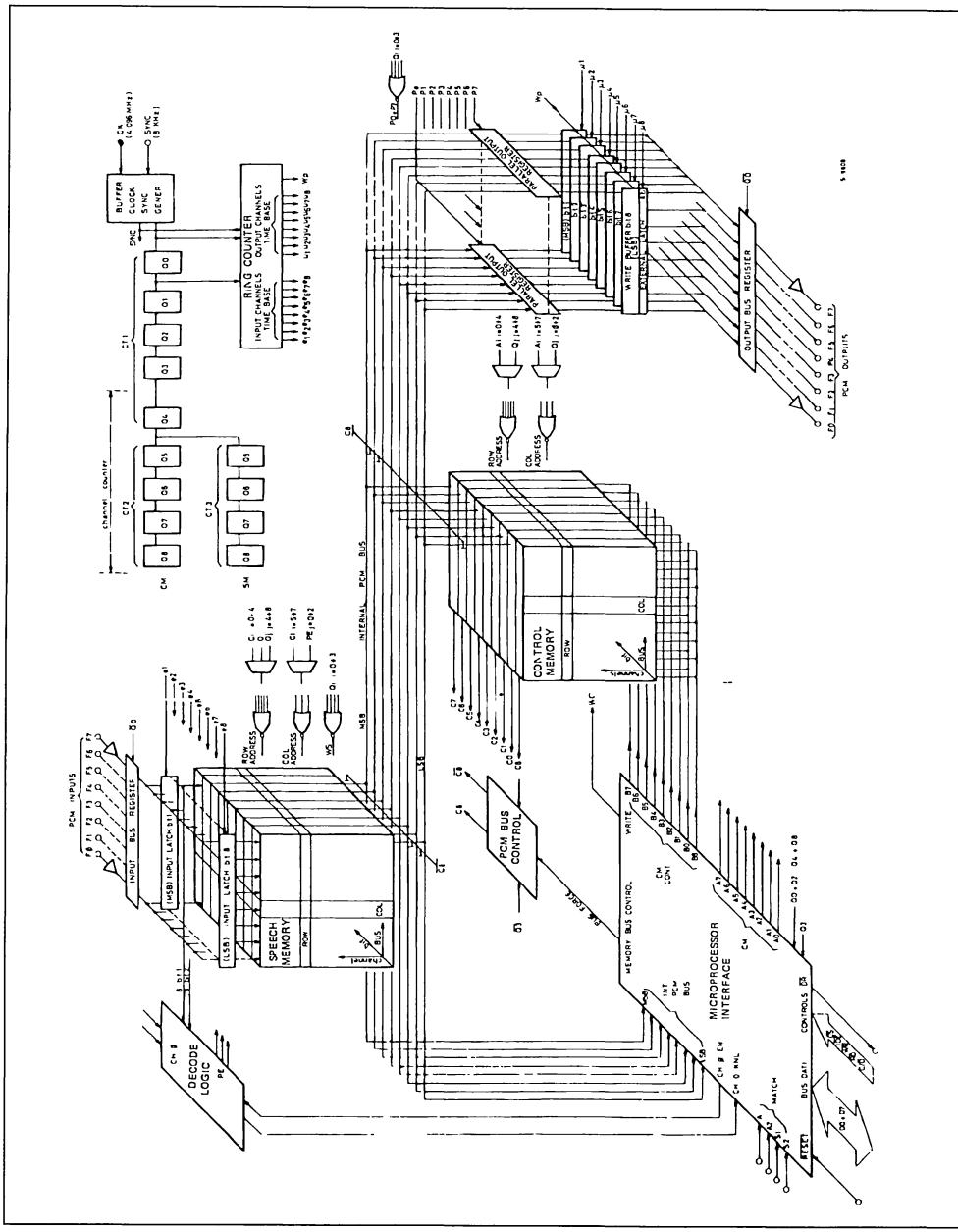
The time base consists mainly of a fast synchronous parallel resettable counter of which stages are obtained by repeated clock division and grouped into three subsets : the first, CT1, starting from the 250ns rate, generates the time phases controlling the 4µs input and output time slot servicing ; in particular, the signal Q3 (4µs) specifies two working phases : one dedicated to the microprocessor interface operations, the other related to PCM operations. The other two subsets, CT2 and CT3, operating synchronously with respect to CT1, generate the sequential channel addresses for control memory reading and for speech memory reading, respectively.

The counter CT2 addresses the control memory, using the output PCM channel address increased by one ; the counter CT3 addresses the speech memory, using the input PCM channel address decreased by one. This address difference is necessary to compensate for the internal component delay due to input and output PCM conversion.

INPUT SERIAL TO PARALLEL PCM CONVERTER

During each time slot (4µs), the 8 serial PCM (2048 Kbit/s) input bits are regenerated and sampled using a 500 ns clock signal, Q0, and then are stored in 8-bit latches clocked by the input ring counter's e1 to e8 signals. As soon as the 64 bits are updated, they are written, using a single write pulse, into the speech memory at the corresponding input channel address, selected by subset counter CT3, performing the parallel conversion in the same writing operation.

Figure 3.1 : The Fundamental Blocks are the Speech Memory (SM), which memorizes for Each Frame the Contents of All 256 Channels, and the Control Memory (CM) which contains Information on the Status of the 256 Output Channels (connected or not connected, loaded by the micro with a given byte).



SPEECH MEMORY

The memory is organized as 32 planes of 8 rows and 8 columns each ; every plane corresponds to an input PCM channel, every row to a bit of content and every column to an input PCM line. The working cycle is about 4µs, with this time divided into 2µs phases. The first one consists of eight 250 ns cycles : one particular cycle is devoted to memory updating according to input channel data ; in the other cycles, functions engaged by the µP interface logic can be performed at random in the memory (that is the case of PCM output channel reading). In the second, memory is cyclically read 8 times, using the control memory addresses, C0 to C7 (switching function).

CONTROL MEMORY

Control Memory is organized in 32 planes of 9 rows and 8 columns each ; every plane corresponds to any output PCM channel, every row to a content bit and every column to an output PCM line. The Control Memory working cycle is similar to the Speech Memory.

During the first 2µs phase, the Control Memory is idle and normally accessible to µP interface. On occasion, because of network connection updating or µP requests, some cycles are stolen here for this purpose. During the latter 2µs phase, the memory is read eight times, using the addresses coming from the time base (subsets CT1 and CT2). The output contents of 9 bits each are used as addresses for Speech Memory (C0 to C7) and as a control signal for switching the internal PCM bus to the proper Control or Speech Memory output data (C8).

INTERNAL PCM BUS

Speech and Control Memories are connected to the internal 8-bit parallel bus. The 9th Control Memory bit controls each memory's output during the switch function ; otherwise, it is forced by the µP interface.

The internal bus is connected on one side to the µP interface to perform functions like memory content transfer. On the other side, the bus connects the PCM Parallel to Serial conversion unit.

OUTPUT PARALLEL TO SERIAL CONVERTER

The bytes of the internal PCM bus, belonging to the 8 cycles previously mentioned in Control Memory, are saved in a group of 8 temporary registers, each selected by the timing signals P0 to P7 (see fig. 3-1). When all bytes are stored, a single pulse transfer takes place in order to supply new PCM data to the output registers.

The proper time phases u1 and u8 sequentially scan the 8 output registers and simultaneously feed the output pins performing the Parallel to Serial conversion. The output PCM flows are resynchronized, using a 500ns clock signal (Q0). PCM outputs are open drain type.

MICROPROCESSOR INTERFACE LOGIC

The interface logic controls, asynchronously with respect to the PCM timing, the 8 bit data bus and the control bus to and from the microprocessor. It also stores, in a five byte stack, the data field and the opcode instruction. It gives the other internal blocks the necessary signals to perform the function in the right time phase. Moreover, it stores the status information, which can be read by the µP for diagnostic purposes, in two internal registers, OR1 and OR2.

The external control bus allows the component to be used as a standard 8-bit peripheral device, compatible with most Ps, such as the Z80 and Z8. It consists of RD and WR signals for reading and writing into the M088 respectively, and the C/D signals, which selects between data and operating the code of command bytes to the written into the M088. Signals CS1 and CS2 activate the component when other peripheral devices are connected to the same bus.

Signals A1, S1, A2 and S2 allow more M088s to be connected in a simple way to obtain non-blocking matrix structures. An M088 in a match condition

4. FUNCTIONAL DESCRIPTION

The device, controlled by the microprocessor, implements six different instructions. A specific function is executed after the microprocessor has transmitted, using the data bus, the data bytes and the command bytes.

Two or four data bytes carry the information necessary for the correct interpretation of the function. The command byte follows these with the operative coding information necessary for M088 to execute the function.

Brief descriptions of individual functions are given here. For further information, the M088 data sheet for the device should be consulted.

FUNCTION 1 : CHANNEL CONNECTION/DISCONNECTION

This function permits the formation of a new connection between a given input channel (C_{IN}) and a given output channel (C_{OUT}). See fig. 4-1.

The message coming from the microprocessor consist of four data bytes plus a command byte.

The first two data bytes carry, respectively, information about the PCM input line and the input channel ; the third and fourth bytes carry information about the PCM output line and the output channel.

The first two bytes are loaded in the control memory cell (CM), the address of which is specified in the last two bytes.

It cases of switching systems of more than 256 x 256 channels some examples are given in Section 6 use is made of additional M088 chips, interconnected as required (multi-chip matrices).

In this case, the connection function is executed only by the M088 in match condition (A1 = S1 and A2 = S2) ; all the other M088s of the multi-chip matrix involved with channel C_{OUT} will execute a disconnection operation from that selected output channel (C_{OUT}).

FUNCTION 2 : CHANNEL DISCONNECTION

Disconnect the selected output (C_{OUT}). See fig. 4-2.

The message coming from the microprocessor is made up of two data bytes plus a command byte.

The first and the second bytes carry, respectively, information about the PCM output line and the output channel which must be disabled.

FUNCTION 3 : BYTE INSERTION/CHANNEL DISCONNECTION

The function permits a byte furnished by the microprocessor to be inserted in an output data channel (C_{OUT}). See fig. 4-3.

The message is made up of four data bytes plus a command byte.

The first and second bytes contain information for transferral to the PCM output channel. This 8-bit information is memorized inside a control memory cell (CM).

The third and fourth data bytes contain, respectively, information on the PCM output lines and on the output channel in which the byte is to be inserted. These last bytes are used as an address to specify the CM cell in which to load the information contained in the first two data bytes.

As was the case for the first instruction examined, in the case of multi-chip matrices, this instruction is executed only by the selected M088 ; all the remaining M088s of the matrix will execute a disconnection operation on the selected output channel.

FUNCTION 4 : BYTE EXTRACTION

This function permits transferral of the byte contained in an output data channel to the microprocessor, using the data bus.

The message is made up of two data bytes plus a command byte.

The first and second bytes contain, respectively, the number of PCM output line and of the output channel, the contents of which are to be read by the microprocessor.

The PCM octet is memorized by the device in register OR1 ; thereafter, the microprocessor, using the aforementioned register's read cycle, transfers the PCM sample to the CPU.

If it is useful to read the PCM byte from an input data channel C_{IN}, C_{IN} must be connected with a particular output channel C_{OUT}, and thus apply the extraction function to C_{OUT}. See fig. 4-4.

Figure 4.1 : Connection Any of the 256 Input Channels (C_{IN}) can be Permanently connected to any of the 256 Output Channels (C_{OUT}). It is Possible tohave 256 Connections simultaneously.

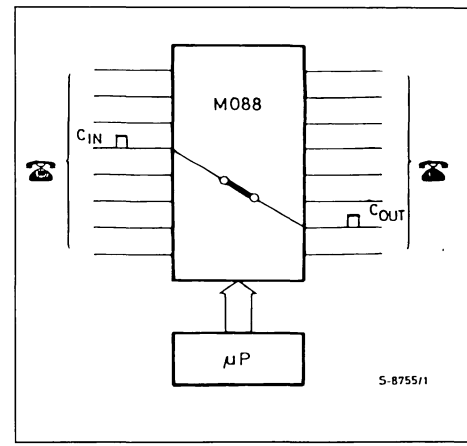


Figure 4.2 : Disconnection. Each Connection Previously made can be interrupted at any Time.

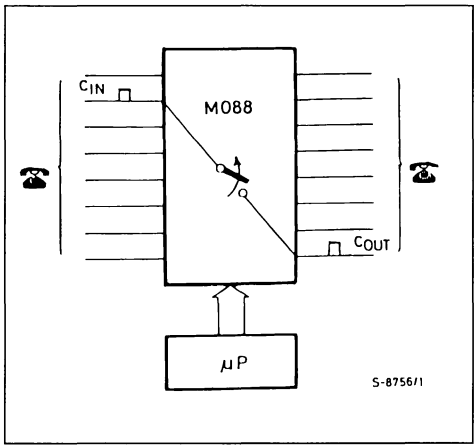


Figure 4.3 : Insertion of a Byte. The Control Microprocessor can send a given Byte to Any Output Channel.

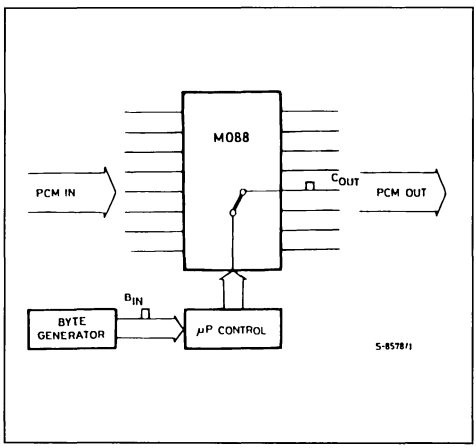
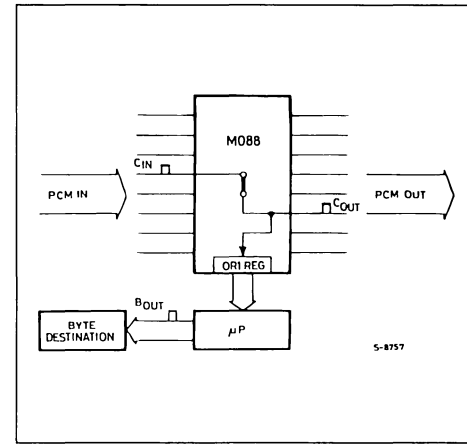


Figure 4.4 : Extraction of a Byte. The Micro Can Extract from Any Output Channel (C_{OUT}) the Contents (B_{OUT}) at the Time of the Request.



FUNCTION 5 : CONNECTION MAP READING

This function makes it possible to know, starting from a particular output channel C_{OUT}, the contents of the corresponding control memory cell CM, the address of which is exactly the same as C_{OUT}. See fig. 4-5.

As already explained in Section 3, each control memory cell CM is made up of nine bits (C8, C7.... C0).

If the ninth bit is equal to zero, the eight remaining bits (C7, C6.... C0) provide information concerning the input channel C_{IN} connected simultaneously with C_{OUT}. In particular, C7, C6 and C5 provide the PCM input line number, while C4, C3, C2, C1 and C0 provide the relevant C_{IN} channel number.

On the contrary, if bit C8 is equal to one, two possibilities can be examined :

a) byte C7, C6.... C0 is equal to 11111111 – in this case, output channel C_{OUT} is not connected to any input channel C_{IN}, and the microprocessor

never loaded any byte on the basis of instruction 3 ;

b) byte C7, C6.... C0 is not equal to 11111111 – also, in this case, the C_{OUT} channel is not connected to any input channel C_{IN}, however, the aforementioned byte is a copy of the one which the microprocessor has already loaded in C_{OUT}.

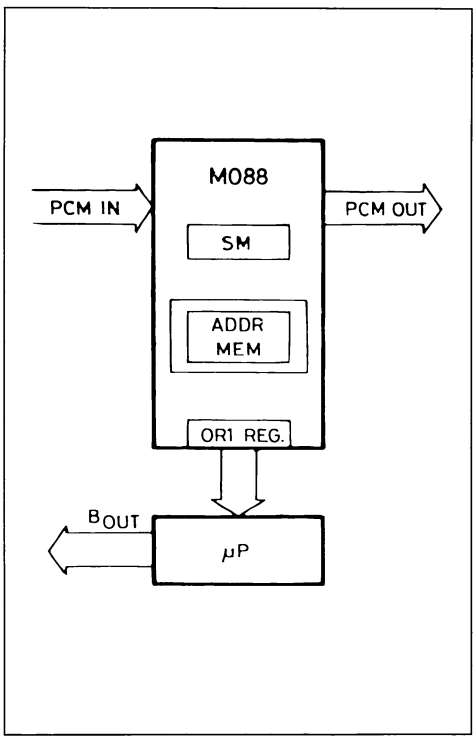
The message coming from the microprocessor is made up of two data bytes plus a command byte.

The first and second bytes correspond, respectively, to the number of PCM output line and to the C_{OUT} channel, and, as already mentioned, correspond to the CM cell address whose contents the microprocessor must read.

Bits C7, C6.... C0 are memorized in the OR1 register, while bit C8 is memorized in the OR2 register.

With two read cycles, the microprocessor can thus transfer the contents of the two registers OR1 and OR2 into the CPU.

Figure 4.5 : Reading the Control Memory. Through This Operation the Microprocessor Can Read the Status of Every Output Channel.



Timeslot 0

FUNCTION 6 : CHANNEL 0 CONNECTION MASK STORE/DATA TRANSFER

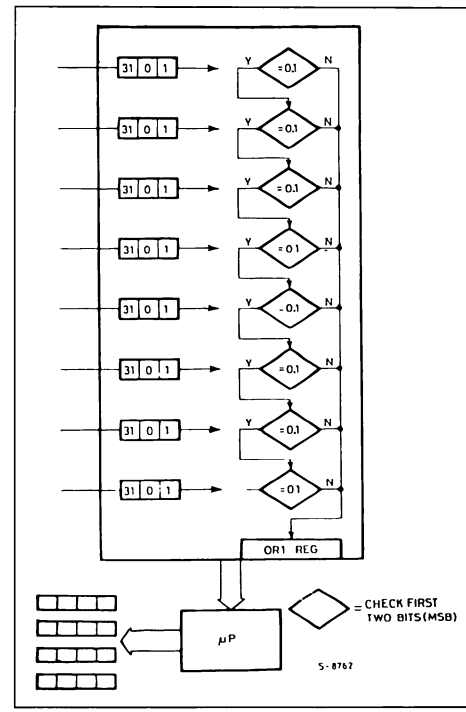
This last function is used to extract information rapidly from channel 0. See fig. 4-6. The indispensable requirement for the extraction to take place is that the two most significant bits of the byte contained in channel 0 not be equal to 01.

The PCM input lines from which the 0 channels are extracted are selected by using the microprocessor to load two data bytes, comprising the mask byte and a command byte.

The contents of channel 0 are available from the OR1 register, from which the microprocessor can transfer them externally by successive reads from the same register.

Experimental testing has shown that, with a CPU clock of 4.000 MHz in a time frame (125μs), it is possible to extract the 0 channels from all eight PCM lines.

Figure 4.6 : Rapid Extraction of Channel 0. Allows the Extraction of the Contents of the Active Channel Zeros and Channels with the Most Significant Bits Not Equal to 01.



5. VARIOUS NOTES AND CONSIDERATIONS ABOUT THE M088

In this section, certain aspects of the timing and operation of the device will be described in some detail.

In order to better understand the subject matter, it is recommended to have already read the component's data sheet.

SYNC TIMING

One of the aspects which should be handled with particular attention in the use of the component is the timing relation between the synchronization signal ($\overline{SYNC}$) and the clock signal (CK).

The $\overline{SYNC}$ signal, specifically its rising edge, specifies the beginning of the frame and, thus, bit 0 of channel 0.

The zone sketched in fig. 5-1 shows the areas of possible transition of the rising and falling edges of the $\overline{SYNC}$ signal with respect to the CK signal.

The absolute value of the width of this zone (t_V) is :

$$t_V(\overline{SY}) = t_{CK} - t_R - t_{HL}(\overline{SY}) - t_{SH}(\overline{SY})$$

in which :

$t_V(\overline{SY})$ is the maximum time width of the area of the rising edge of SYNC ;

t_{CK} is the clock (CK) period ;

t_R is the maximum clock (CK) rise time (= 25 ns) ;

$t_{HL}(\overline{SY})$ is the $\overline{SYNC}$ minimum low level hold time (= 40 ns) ;

$t_{SH}(\overline{SY})$ is the $\overline{SYNC}$ minimum high level set-up time (= 80 ns).

The falling edge of $\overline{SYNC}$ can take place anywhere if the length of level 1 is greater or equal to t_{CK} and the length of level 0 is greater than or equal to :

$$t_{SL}(SY) + t_R + t_{HL}(SY) = 145 \text{ ns},$$

$t_{SL}(\overline{SY})$ being the $\overline{SYNC}$ min low level set-up time (80 ns).

PCM INPUT SIGNAL TIMING

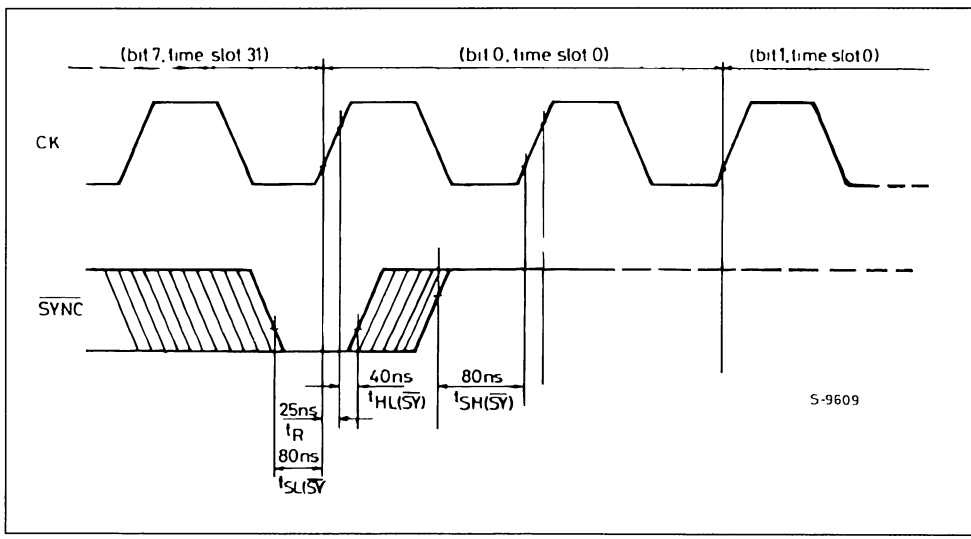
Another very important point is the timing relationship between the PCM input signals and the SYNC signal.

In many cases, it is of major importance to know how much the eight PCM input signals can be mutually dephased with respect to the CK signal.

Fig. 5-2 presents an example of dephasing of the general PCM input signal with respect to CK. To better illustrate this aspect in the figure, the PCM input signal is represented both with the minimum, and with the maximum, permissible delay.

In the same figure, an extremely interesting aspect is evident, namely, that the various PCM input flows

Figure 5.1 : SYNC Signal Timing. The Shaded Zones are the Regions of Possible Transitions. The Rising Edge of SYNC Determines Bit 0 of Channel 0.



are able to mutually tolerate dephasing at a level of nearly one bit-time.

Indeed, the time variation between the PCM input signals with minimum and maximum permissible delays, t_V (PCM), is as follows :

$t_V(PCM) = (2 \cdot t_{CK}) - (t_H(PCM) + t_R(CK) - t_S(PCM))$

Therefore, referring to fig. 5-2 ;

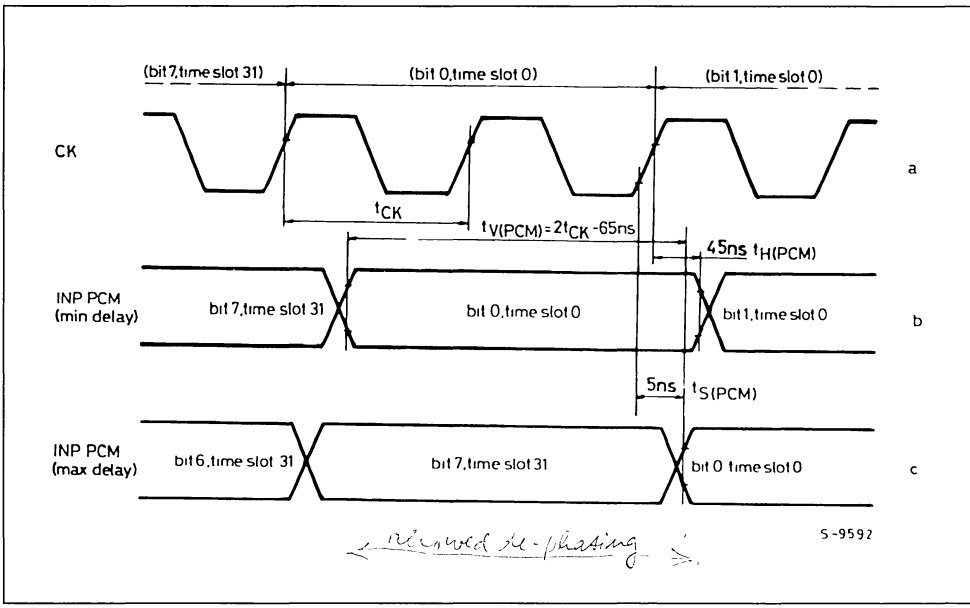
$t_V(PCM) = (2 \cdot t_{CK})$ 65 ns.

In the case of the European PCM (2048 Kbit/s), t_V (PCM) = 423 ns, or 86 % of bit-time.

In the case of the North American PCM (1544 Kbit/s, t_V (PCM) = 582 ns, or 90 % of bit-time.

This fact suggests one of the component's possible alternative applications, namely that of the PCM flow rephaser for delays included in values which have already been mentioned.

Figure 5.2 : Timing of the PCM Input Signal (INP PCM). This Diagram Illustrates the Cases of (INP PCM) with the Minimum (b) and Maximum (c) Tolerated delay Referred to the Clock Period (a) Corresponding to Bit 0 of Channel 0. Note That the Regions of Possible Variation Correspond to Almost One PCM Bit Period.



PCM OUTPUT SIGNAL TIMING

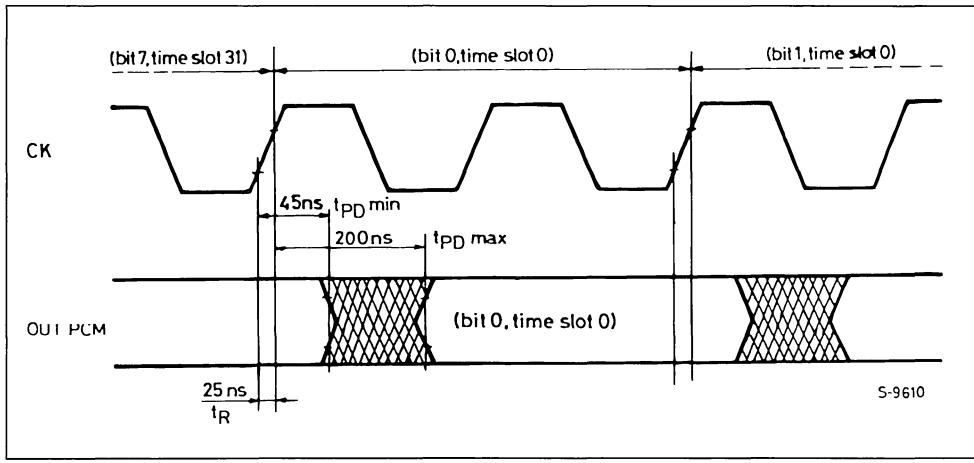
Fig. 5-3 shows the areas of variation of the edges of the PCM output signal with respect to the CK signal, the PCM input signal with maximum and minimum delay.

The width of such areas amounts to 155ns.

Also, the figure clearly indicates the possibility of using the PCM output flows as PCM input flows, in other words, to create a loop between the PCM outputs and inputs.

This could be used for test operations or for introducing frame delays into the PCM flow.

Figure 5.3 : Timing of the PCM Output Signal (OUT PCM). The Shaded Regions Indicate Where the Transitions May Take Place.



READ AND WRITE TIMING

The M088 device requires that the PCM signals be correlated with the CK signal.

In theory, the microprocessor interface signals could be completely asynchronous with the CK signal.

In reality, that is completely true only in cases where M088 is not inserted in a multi-chip matrix. In this last case, it is indeed to be recommended to link the $\overline{RD}$ and $\overline{WR}$ signals to the CK signal.

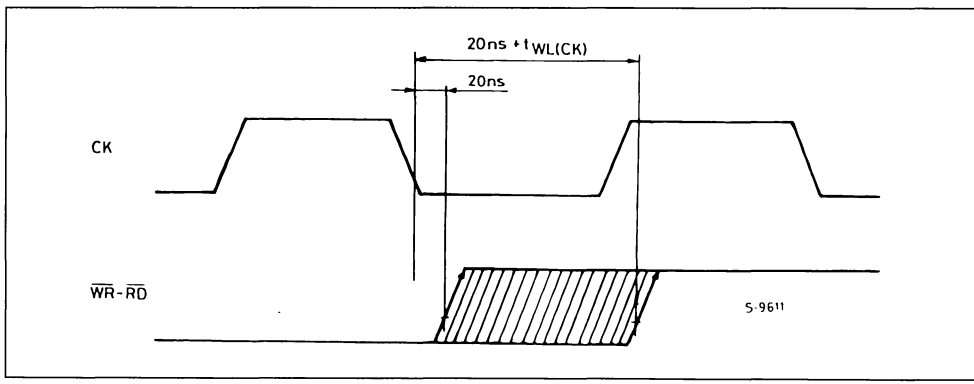
In particular, their rising edges must be delayed with respect to the falling edge of CK in a single phase, t_V (RW), in the range between 20ns and (20ns + t_{WL} (CK) = 120ns.

Fig. 5-4 presents an example of areas of transition among the rising edges of the aforementioned signals with respect to CK.

Given certain special conditions which are very difficult to deal with, problems could occur if the recommended synchronization for a multi-chip switching matrix is not respected. The connection of the relevant M088 will be carried out before the disconnection of the output channels of all the remaining M088s of the matrix.

This could cause an error in the correlation of the first bit in the first byte of the signal transferred.

Figure 5.4 : The Shaded Area Shows the Recommended Variation in the Rising Edge of the READ and WRITE Signals in the Case of Multi-chip Matrices.



Anyhow, this only concerns the first byte transferred ; there will be no problem with those following. Another interesting parameter concerning the $\overline{RD}$ and $\overline{WR}$ signals is the minimum timing interval to maintain between two consecutive cycles, in other words, between the two rising edges.

The timing, t_{REP}, is a CK period function, namely :

$$t_{REP} = 40\ ns + 2\ t_{CK} + t_{WL}\ (CK) + t_R\ (CK).$$

When $t_{CK} = 244ns$, $t_{REP} = 653ns$.

The reading operations of the OR1 and OR2 registers during instruction 6 are the only exceptions.

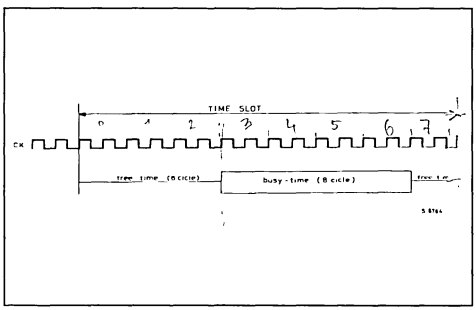
In this case, a request is indeed made for the minimum time between RD rising edges to be 3 CK periods for sequences from OR1 to OR2, and 13, for sequences from OR2 to OR1.

INSTRUCTION EXECUTION TIMING

Within a time slot (3.92µs for PCM input flows of 2048 Kbit/s), there are 16 CK periods. Each period corresponds to a machine cycle.

Of the 16 cycles contained in a time slot, 8 are free and are used to carry out instructions received from the microprocessor. Fig. 5-5 shows the internal distribution in a time slot with these cycles.

Figure 5.5 : The Division within Each Time Slot Between the Time Reserved for Internal Processing and That Reserved for the Execution of Commands Supplied by the Microprocessor.



Physical time for internal execution of an instruction amounts to 5 cycles, excluding loading time for data bytes and commands coming from the microprocessor.

This time can be increased by 8 cycles if the instruction execution is not complete before the beginning of the block of 8 cycles reserved for internal operations.

Moreover, if instruction 6 is activated, all other instructions will be processed after instruction 6 has been completed or, at the latest, at the beginning of the new frame.

By activating instruction 1 (Connection/Disconnection) between a given input channel C_{IN} and an output channel C_{OUT}, the byte transferred to C_{OUT} corresponds to the byte taken from C_{IN} in the same or the preceding frame, based on the relative position of C_{OUT} with respect to C_{IN}.

In particular, if the number of C_{OUT} channels (NC_{OUT}) is greater than or equal to two units as compared with the number of C_{IN} channels (NC_{IN}), the connection occurs in the same frame.

6. APPLICATIONS

EXCHANGE NETWORK

The M088 device was designed to be used as a basic element in large-scale switching systems, with up to 65536 connections.

An example of a structure which could be used for this purpose is shown in fig. 6-1, which shows that a system of 64 K users (2048 PCM links, each having 32 channels) is made up of eight central modules, each with a capacity equal to 8 K connections (256 PCM links, each having 32 channels) and of (256 + 256) M088 peripherals.

Fig. 6-2 shows the internal organization of a central module with 8 K connections.

It should be noted that it is made up of eight switching units, each with a capacity equal to 1 K connections (32 PCM links, each having 32 channels) and of (32 + 32) M088 peripherals.

Figure 6.1 : Simplified Block Diagram of a Switching Matrix with 65536 Channels Concentrated in 2048 PCM Links at 2048 Kbit/s Each.

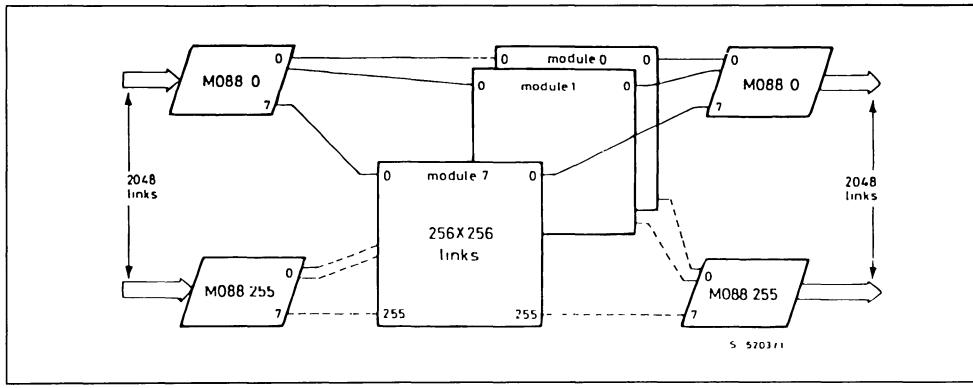
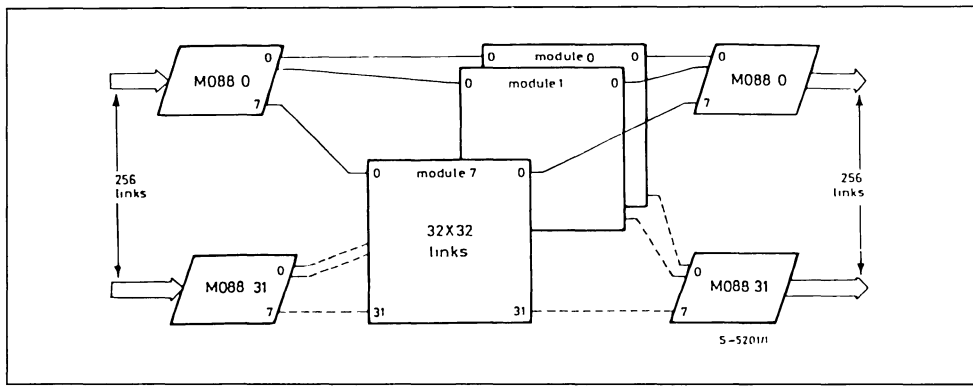


Figure 6.2 : Simplified Block Diagram of a Switching Module Four 8192 Channels Concentrated Into 256 PCM Links at 2048 Kbits/s.



The internal structure of a switching unit with 1K connections is shown in fig. 6.3.

It is made up of 16 M088s organized in a square matrix (multi–chip matrix).

It is important to stop, finally, with this last structure, insofar as it could, without any variation, be used as a PABX switching matrix, up to 1000 lines.

The 1000 lines, or, more precisely, 1024, are concentrated in 32 PCM flows at 2048 Kbit/s.

All 16 M088s have microprocessor interface signals in common (D7 to D0, RD, WR, C/D, RESET), as well as CK, SYNC and selection pins A1, A2 and CS2.

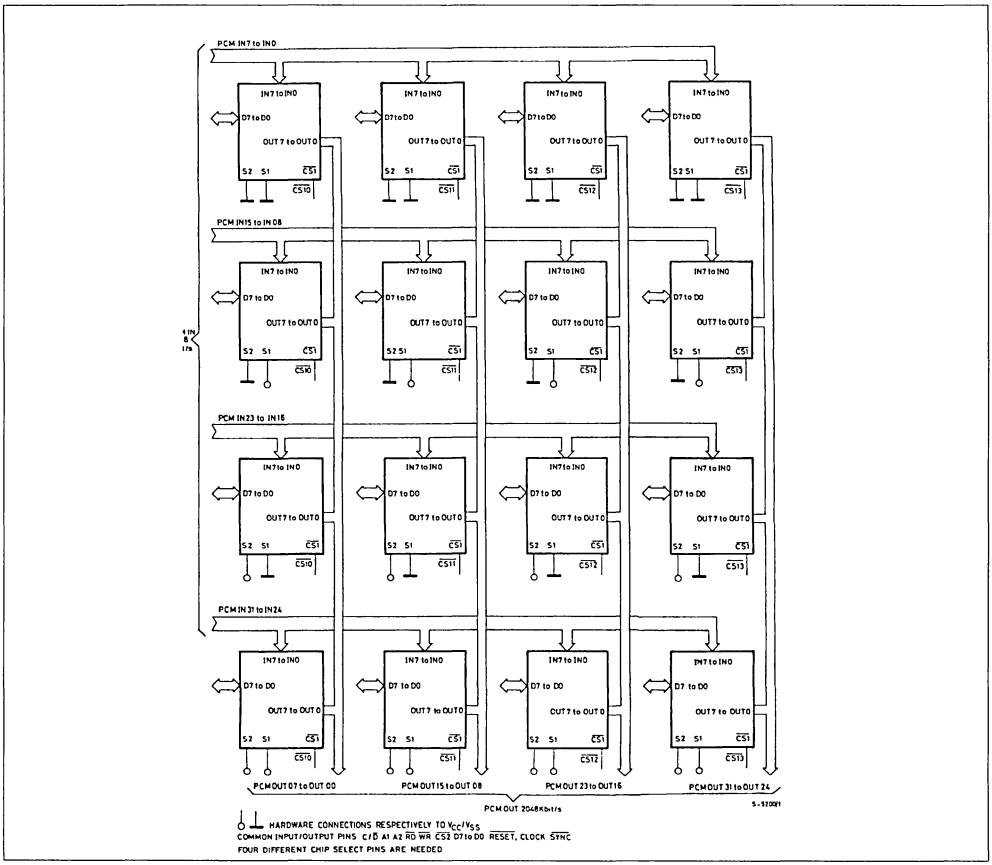
Also, all 4 M088s belonging to the same column have the same output channels in common and all 4 M088s belonging to the same row have the same input channels. When the microprocessor needs to execute an operation on a certain output channel C_{OUT}, the relevant M088 column is chosen from among the chip select signals CS10, CS11, CS12 and CS13.

Thus, the microprocessor transmits the relevant bytes which, obviously, are received by all the M088s of the matrix.

However, only one of these M088s should execute the instruction.

The single M088 which should execute the function request is the one in which pins S1 and S2 have been connected to V_{CC} and V_{SS} in such a way as to correspond to the signals present, respectively, on the common wires A1 and A2.

Figure 6.3 : Switching Matrix for 1024 Channels Concentrated Into 32 Links at 2048 Kbits/s.



The other M088s in the column selected recognize that, even though having to do with an operation of a channel under their control, this operation must be carried out by another M088 in their column and they act on this basis.

In the case of instructions 1 and 3, they carry out a disconnection from the relevant output channel C_{OUT}, instruction 5 is unaffected and instructions 2, 4 and 6 are not executed.

*Bus reading only takes place on M088 in match condition (A1 = S1, A2 = S2).

This fact greatly simplifies the controlling software of the matrix insofar as, when a new connectionneeds to be executed or a byte loaded on a certain C_{OUT}, it is possible to ignore the same C_{OUT} disconnection from earlier connections because the disconnection is carried out automatically by the multichip matrix.

PABX

What was explained in the previous paragraph applies to switching systems up to 1024 lines.

The switching matrix for systems up to 512 users is represented in fig. 6-4.

Also, in this case, it is important to demonstrate the great simplification in the control software determined by the use of S1, S2, A1 and A2 for the choice of M088 involved in operations.

A single M088 will suffice for switching system up to 256 channels.

In the sphere of the PABX, regardless of its size, a function currently always in demand is the conference function, that is, the possibility to interconnect several users.

Figure 6.4 : Switching Matrix for 512 Channels Concentrated Into 16 PCM Links at 2048 Kbits/s.

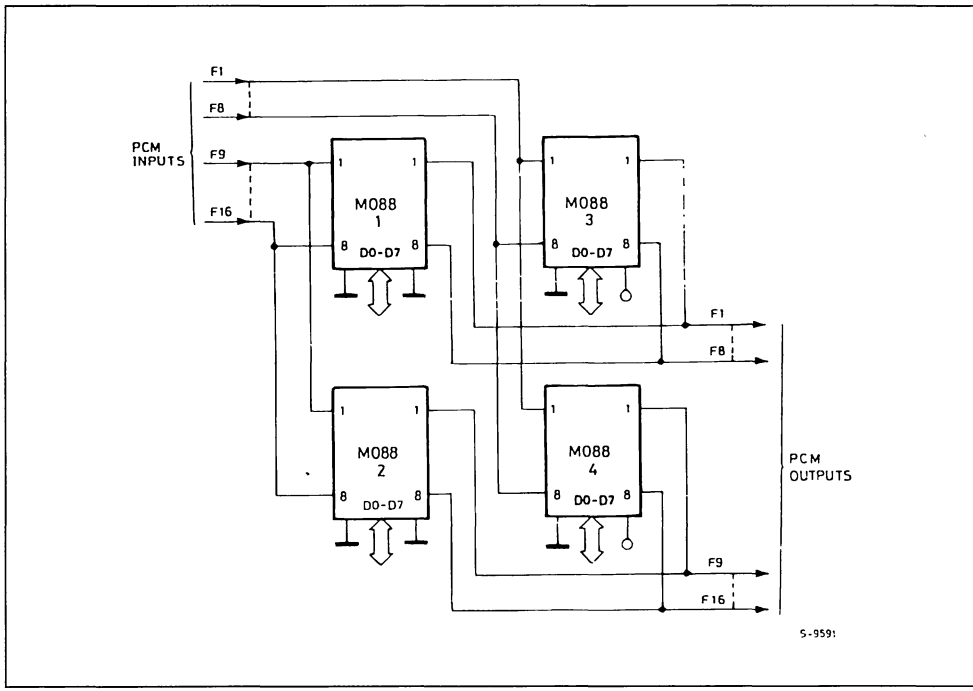
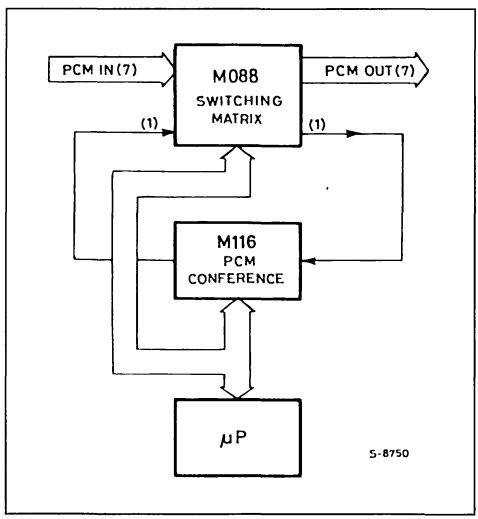


Figure 6.5 : Typical M088-M116-µP Configuration. One Output Stream of the M088 are Connected to the M116 and Dedicated to the Conference Function.



SGS-THOMSON has developped a device for this purpose, called CONFERENCE CALL (M116), which is used in conjunction with the M088 to carry out this function.

Fig. 6-5 demonstrates this application.

The M116 is also controlled by an 8-bit microprocessor, for example, the Z80 or the Z8, and, therefore, has been given a parallel interface for the microprocessor, using characteristics exactly the same as those available in the M088.

In order to carry out a conference operation, it is essential to reserve a PCM output and input in the matrix, for which, when using a single M088, switching capacity decreases to (224 x 224) users. With a single M116, it is possible to carry out from 1 to 10 conferences simultaneously, with the only limitation being that the total number of users involved in the conferences must be less than 32 ; fig. 6-6 illustrates this aspect.

With reference to fig. 6-7, in which the case of three users in conference is examined, we can see which phases are required to bring about a conference :

1) the channels to use for the conference (A, B and C, in the example) are allocated in any channel

position of the reserved PCM bus. The operation is carried out by the M088.

2) the supplementary channels are added together, in other words, the contents of channel B arereplaced by the sum of channels (A and C) etc. This is carried out by the M116. These sum signals are loaded in the reserved PCM output bus.

3) the sum signal are withdrawn from the reserved PCM bus and switched into the relevant output channels. This operation is carried out by the M088.

Figure 6.6 : With a Single M116 It is Possible to Realize from 1 to 10 Independent Conferences with a Total of up to 32 Channels Conferenced.

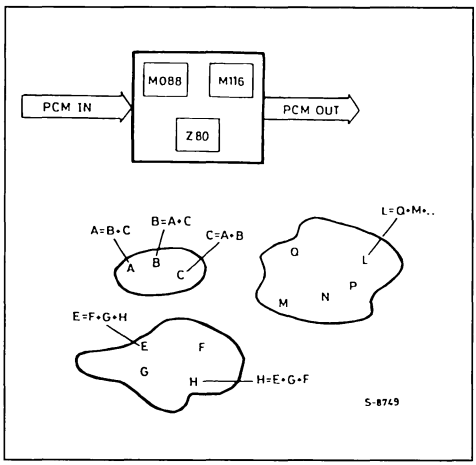
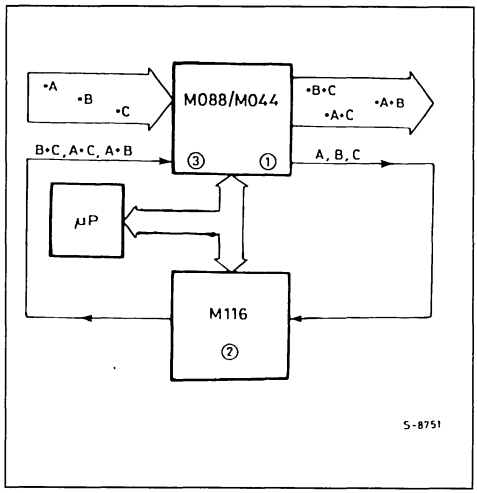


Figure 6.7 : Example of a conference with three channels ; A, B and C.

1) The M088 allocated A, B and C to the PCM stream applied to the M116.

2) The M116 processes the channels A, B and C, returning to the outputs B+C, A+C and A+B respectively.

3) The M088 allocates the signals B+C, A+C and A+B, to the outputs corresponding to the time slots of the channels A, B & C.



It is also possible to use the M116 in a multi-chip switching matrix - see fig. 6-8 - or use more than one M116 in the same matrix - see fig. 6-9.

Figure 6.8 : The M116 Can Also Been Used in Multichip Matrices.

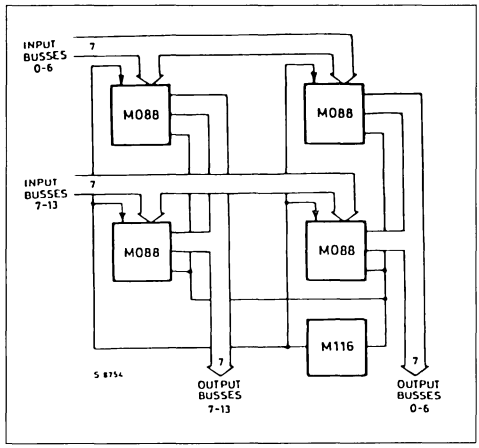
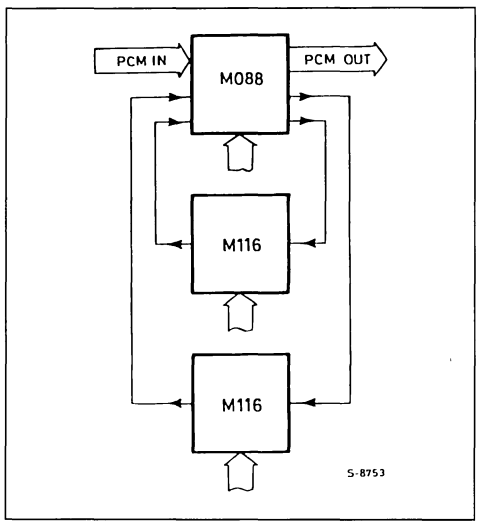


Figure 6.9 : More Than One M116 May be Added to Each Matrix to Increase the Number fo Conferences (10 per device).



For more detailed information see the M116 datasheet.

Finally, it is interesting to note how the M116, on its own, can be used with other types of switching matrixes ; however, two considerations lead to recommending its use with the M088 ;

a) M116 PCM signal timing and microprocessor interface are exactly the same as those of the M088 ;

b) the command format that the microprocessor sends to the M116 to program the different operations is the same as the one used to program the M088.

To sum up, by using the M116 with the M088, complete compatibility is obtained, both with hardware and software, between switching matrices and the M116.

M088 WITH LESS PCM LINKS THAN 32 CHANNELS

It is also possible to use M088 when the PCM frames are made up of a number of channels other than 32.

Suppose that the PCM frames are made up of N-Channels, which will be numbered from 0 to (N-1).

Each PCM frame will thus be made up of a number of bits multiplied by 8 ; this exactly equal to (N · 8).

Also, in this case, it is necessary to respect the timing relationship between the different signals shown on the data sheet ; in particular, a relation-ship is always carefully made between the rising edge of SYNC and the first clock (CK) bit contained in the slot time for bit 0 of channel 0.

In order to use M088 with these frames, it is sufficient, using the data bytes sent by the microprocessor, to modify the numbering of a few channels.

In particular :

a) in all instructions in which reference is made to the input channel (N-1), the number 31 should be substituted for the number (N-1) ;

b) in all instructions in which reference is made to the output channel 0, the number N should be substituted for the number 0.

These variations can be made insofar as the M088 is internally programmed to execute the different operations using 32 channels.

In particular, during the time slot which corresponds to the last channel of the frame, channel (N-1), the M088 loads the bits corresponding to the next channel to be output in the next slot time into its registers.

We consider this last channel to be channel 0, but for the M088 it is Channel N ; indeed, the M088 draws the bits that it will successively output from the corresponding cells of Channel-N.

Likewise, during the general time slot X, M088 loads the PCM input frame bits corresponding to channel X ; simultaneously, it memorizes the bits loaded in the previous time slot into the Speech Memory (SM) memory location corresponding to channel (X-1).

Therefore, during the time slot corresponding to channel 0, M088 memorizes the bits received in the previous time slot, which we consider to be channel (N-1), in the SM memory locations corresponding to channel 31.

For whoever wishes to connect the input channel (N-1) to any output channel, the same channel's PCM samples will be drawn from locations reserved for channel 31.

M088 WITH THE NORTH AMERICAN PCM STANDARD

The operation of the M088 with PCM frames using the North American standard can be considered a special case of the operating mode described in the previous paragraph.

The only variable in this case is the presence in each frame of an auxiliary bit (bit X), for which the total number of bits in a frame is :

(24 channels . 8 bits) + 1 bit = 193 bits/frame

As in the preceding case, in alteration in the numbering of the canals is introduced, in particular, the number 23 is replaced by the number 31 in every case in which reference is made to the last channel of the PCM input frame, and in every case where reference is made to output channel 0, the number 0 is replaced by the number 24.

Also, the signals for synchronization ($\overline{SYNC}$) and for clock (CK) are modified as shown in fig. 6-10.

In particular, the rising edge of the $\overline{SYNC}$ signal must appear in bit X's bit time (the 193rd of the PCM input frame). The single variation in the timing of this signal as far as the MCK and CK signals is concerned in that the minimum time for t_{WH} $\overline{SYNC}$ high level width must be from 1 t_{CK} to 3 t_{CK} and thus with (3 . 324) ns = 972ns.

The clock (CK) signal to be applied to the M088 (pin 6) must be frozen for two clock periods during bit X's bit time. A scheme which is recommended for obtain CK beginning from the MCK and $\overline{SYNC}$ signals is shown in fig. 6-11.

The signal bits located in the PCM input frames are ignored, while, in the corresponding positions of the PCM output frames, they assume the same logical values of the 0 bits of channel 0.

If you use the M088 with an M116 the scheme recommended of fig. 6.11 is not necessary. In fact the "frozen clock" is provide by M116 itself (pin EC).

Therefore is enough to connect pin EC of M116 to pin CK of M088. Of course the $\overline{SYNC}$ signal must be the same as shown in Fig. 6.10 and must be connect both to M088 and M116.

DATA FLOW SWITCHING

A very simple, but very important, application of the M088 is that of using it to switch PCM or other high speed data links.

To enable this function, it suffices to switch all relevant input channels to their preselected output channels.

The data rate of these data flows can have any value less that the maximum permissible velocity (2048 Kbit/s).

Obviously, the CK frequency must be the double of the data rate chosen, while the $\overline{SYNC}$ frequency must be included between 1/16 and 1/256 of the same data rate.

Figure 6.10 : Timing of the CLOCK, $\overline{SYNC}$ and PCM IN Signals for 1544 Kbit/s PCM Streams. At the 193 rd Bit (bit X) the CLOCK Signal applied to the M088 is frozen for two Periods.

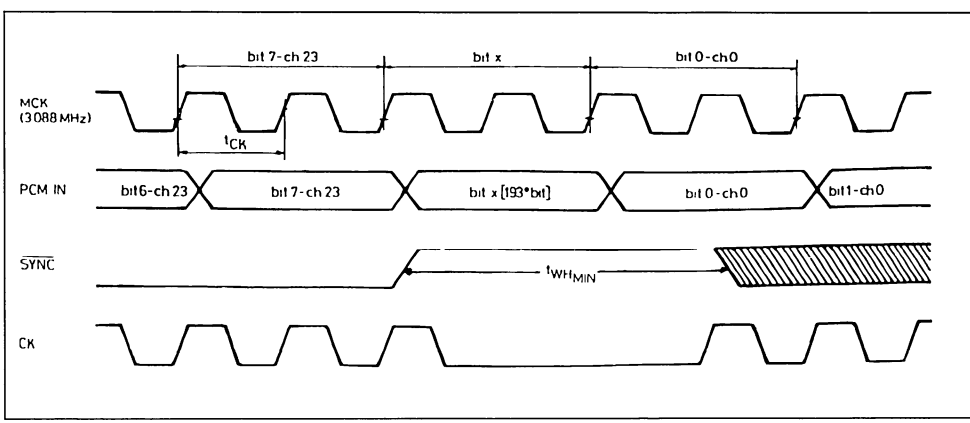
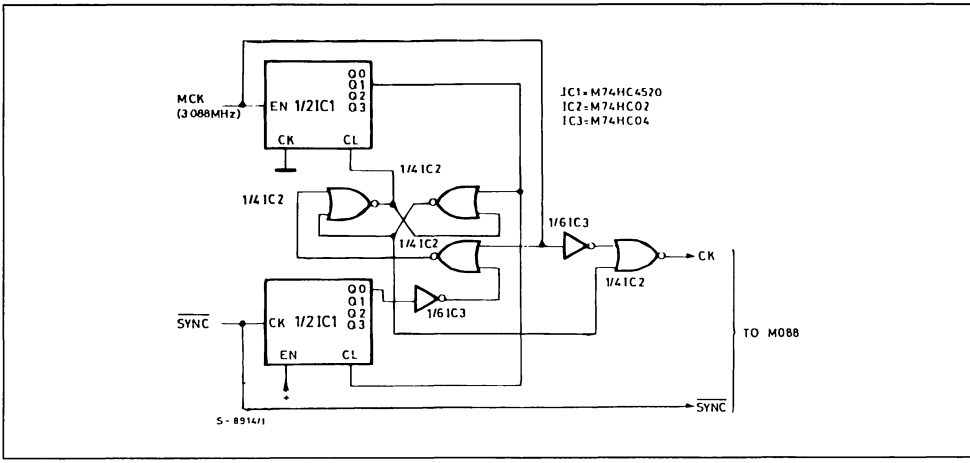


Figure 6.11 : Auxiliary Circuit to use the M088 with 1544 Kbits/s PCM Streams. This Circuit is not necessary if the M088 is used with an M116.



It is particularly interesting, in this application, to demonstrate a characteristic of the M088 which has already been mentioned and, therefore, of the fact that the device accepts that a certain delay can exist between one data flow and another.

The absolute value of the maximum acceptable delay is not constant, but depends on the velocity of the data flow ; in any case, it is always greater than 80 % of bit time.

This obviously means that when the data flows are not generated internally, but come from peripheral devices located at different distances - See fig. 6-12- within certain limits, it is not necessary to equalize the delays caused by variable arrival times.

RS232 C/V-24 DATA INTERFACE SWITCHING

One of the alternative fields for possible use of the M088 is that of DATA COMMUNICATIONS.

Fig. 6-13 presents the block diagram of one of the possible applications : a device which allows for switching between the V-24 interface of four DTEs and the V-24 of four DCEs.

As is well known, the RS232 C/V-24 is one of the most common connection interfaces between Data Terminal Equipment (DTE), i.e., computers and terminals, and Data Communication Equipment (DCE), i.e., modems, etc.

Figure 6.12 : Structure of a PABX with Peripheral Concentration Blocks. Note That the CE-PP Connections are PCM Links.

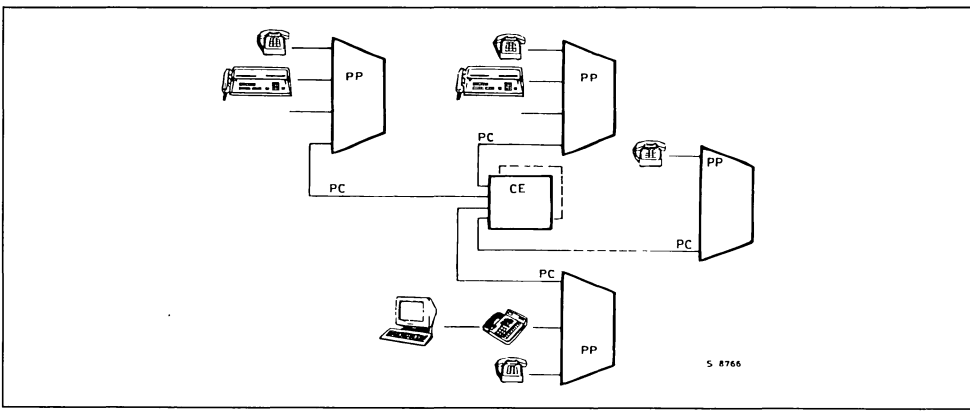


Figure 6.13 : Switching Matrix for Parallel Data Interfaces (eg : RS232C/V24). Signals from the Parallel Interfaces are Serialized, Switched and Parallelized.

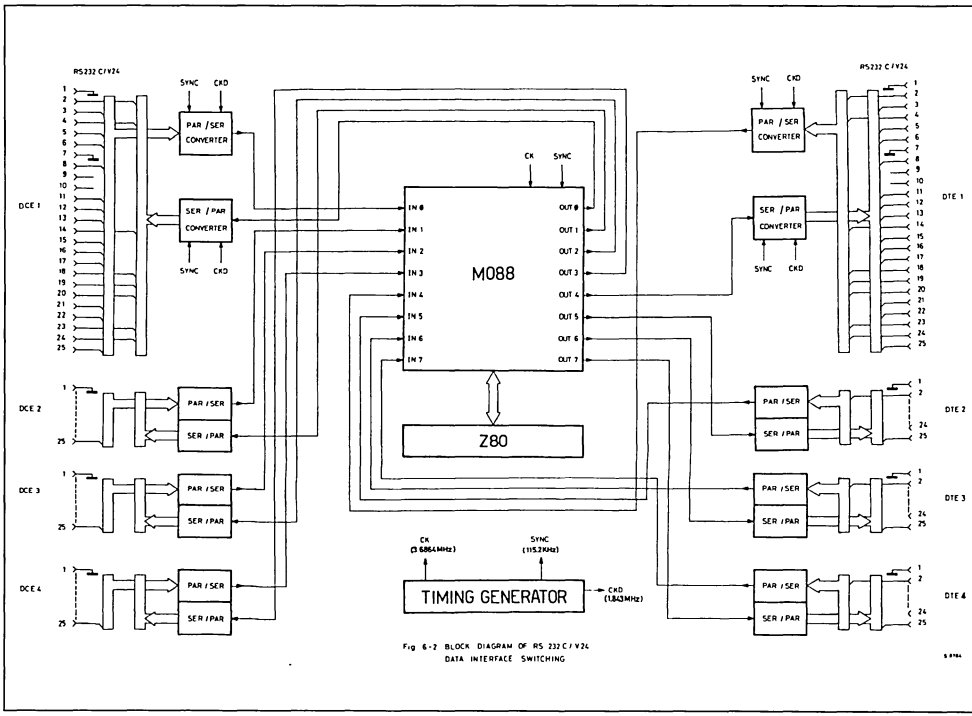


Fig 6-2 BLOCK DIAGRAM OF RS 232 C / V24 DATA INTERFACE SWITCHING

The table in fig. 6-14 presents the names of 25 distinct pins which determine the interface and the direction of the same signals (13 DCE → DTE and 8 DTE → DCE).

The basic idea of the device is to sample, using a frequency of 115.2 KHz, the 21 usable interface signals, serialized at a velocity of 1843.2 Kbit/s, and send or receive them through the switching matrix exactly as if they were PCM streams.

In the case of interfaces coming from DCE, of the 21 usable signals, 13 are signals inputting the device, and 8 outputting it, thus it is necessary to run a parallel/serial conversion on the first, and obviously, serial/parallel on the second.

For reasons of simplicity in the serialization phase for the 13 bits, three bits are added so that every sampling period (8.7 µs) will amount to exactly two octets ; in the parallel/serial conversion phase, the three additional bits are disregarded.

Concerning the DTE, the discussion is similar, with the obvious exception of the fact that the signals undergoing serial/parallel conversion are 13 and those which undergoing parallel/serial conversion are 8.

To these last 8 bits should be added, for the same reasons mentioned before, 8 bits so that, during each sampling period, exactly 16 bits are serialized.

An input and an output made available by the M088 are reserved for each interface.

The M088 views the data streams which are entering exactly if they were PCM frames at 1843 Kbit/s.

In this case, the difference is that the number of channels used is only two, thus each two octets require that the M088 internal channel counter be reset to zero.

This is obtained simply by raising the frequency of the SYNC signal from the usual 8 KHz to 115.2 Khz, in other words, to use as SYNC the same signal used to sample the interfaces (see fig. 6-13).

Wanting, for example, to switch the V-24 from DCE1 to that of DTE4 is sufficient through the microprocessor sending to the M088 instructions for connecting channels 0 and 1 of input 0 with channels 0 and 1 of output 7, channels 0 and 1 of input 7 with 0 and 1 of output 0.

Figure 6.14 : RS-232-C/V. 24 Data Interface Connector Pin Assignements.

Pin	Circuit EIA	Circuit CCITT	SIGNAL NAME	Direction DTE ——— DCE
1	AA	101	Protective Ground	→
2	BA	103	Transmitted Data	→
3	BB	104	Received Data	←
4	CA	105	Request to Send	→
5	CB	106	Clear to Send	—
6	CC	107	Data Set Ready	←
7	AB	102	Signal Ground (Common Return)	↔
8	CF	109	Received Line Signal Detector	←
9			Unassigned	
10			Unassigned	
11		126	Select Tx Frequency	←
12	SCF	122	Secondary Received Line Signal Detector	←
13	SCB	121	Secondary Clear to Send	←
14	SBA	118	Secondary Transmitted Data	→
15	DB	114	Transmit Signal Element Timing (DCE Source)	←
16	SBB	119	Secondary Received Data	←
17	DD	115	Receiver Signal Element Timing (DCE Source)	←
18		141	Local Loopback	→
19	SCA	120	Secondary Request to Send	→
20	CD	108/2	Data Terminal Ready	→
21	CG	110	Signal Quality Detector	←
22	CE	125	Ring Indicator	←
23	CH	111	Data Signal Rate Selector (DTE Source)	→
24	DA	113	Transmit Signal Element Timing (DTE Source)	→
25		142	Test Indicator	←

Obviously, it is possible to carry out simultaneously all four connections in any combination.

Using M088 instead of standard analog cross-point besides switching, you can also implement addition functions as monitoring or programming by µP the status of the interfaces using the instruction 3 and 4 of the M088 itself.

Using more M088s extends at will the number of interfaces thus switchable due to their subdivision between DTE and DCE V-24s.

Finally, there are no limits to the use of this system for switching other interface types.

7. SUPPORT MATERIAL

To introduce users to the use of the M088 and M116, a demonstration board have been developed.

This board allows the user to study the behavoir of M088 and M116 without building any external hardware but using mnemonic and easy commands through a standard asynchronous terminal.

On the board there are also 4 SGS THOMSON MICROELECTRONICS CMOS Combos M5914 that allow the test of the Conference function starting from analog signals.

There are two versions of the demoboard :

- Democonf
- Democonf-Plus

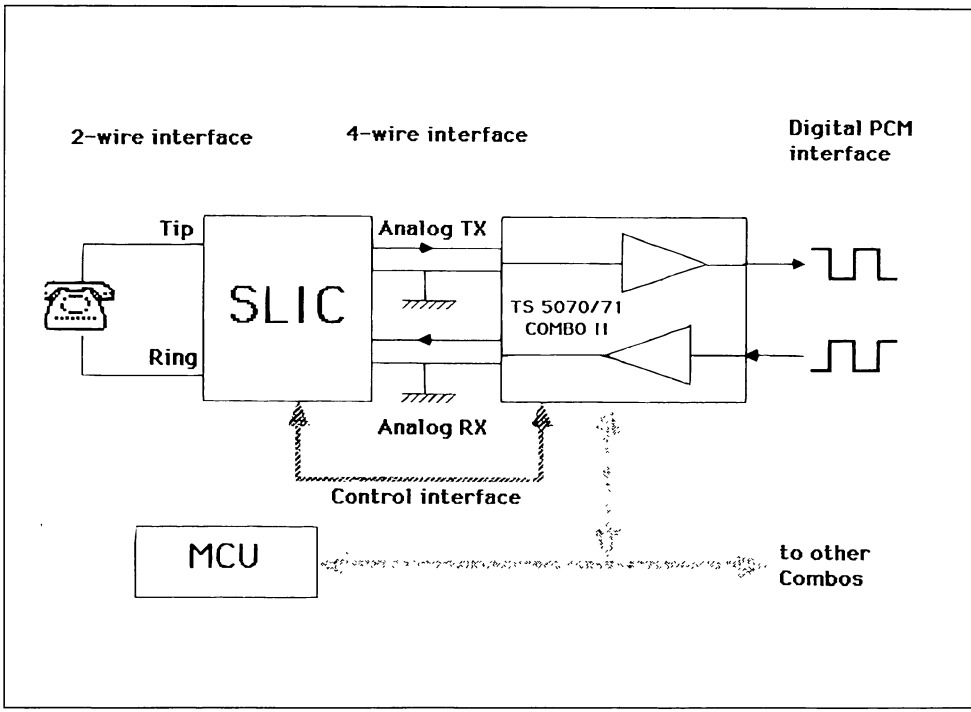
The second one is delivered in a specially-designed executive briefcase and consists of the board, four telephone handsets, a power supply and a user manual.

SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE

TS5070/5071 COMBO II PROGRAMMING AND HYBRID BALANCING WITH SOLID-STATE SLICs

By Bernard SABY



1. INTRODUCTION

The TS5070/71 COMBO II is a programmable Codec/Filter circuit especially developped for the subscriber line card applications in a central office or PABX.

Compared to the currently used first generation codecs, such as : ETC 5054/57, M5913/14, ... the TS5070/71 COMBO II provides two major enhancements :

1) Several functions, previously assumed by external components, are now "on-chip" with the TS5070/71 COMBO II. Such features include :

- Gain adjustable transmit and receive amplifiers (25.4dB range).
- Time-slot assignment (one out of 64).
- PCM port assignment (2 transmit and receive ports, on the TS5070).
- Analog and digital loopback, for test mode.
- Hybrid balance cancellation filter.

2) All these added functions are programmed by the card-controller, through a 4-wire serial bus. Other programmable features include :

- A-law or μ-law selection.
- European (2.048 or 4.096MHz) or North American master clock (1.536 or 1.544MHz).
- 6 input/output interface latches (5 on the TS5071). These latches facilitate the logical interface with a transformer or an electronic parallel control SLIC, such as L3090 or any other function.

The programmable features of the TS5070/71 COMBO II simplify the design of the line card and provide more flexibility, especially when the same module must operate in different countries and must deal with the various telecom administrations requirements : only a few external components must be changed in the SLIC and the major adaptations are assumed by the TS5070/71 COMBO II programming.

As an example, this note describes briefly the design of a line card module, using a TS5070/71 COMBO II with a transformer SLIC and the solid state SLICs from SGS-THOMSON Microelectronics : the TDB7711 Central-office oriented SLIC, the L3090 PABX oriented SLIC and the adaptation of the line card kit to several telecom administrations requirements.

The TS5071 basic version of the COMBO II is packaged in a 20-pin DIL case. The TS5070 is a full feature version available in a 28-pin PLCC or 28-pin DIP package :

- Interface latch pin IL5 is bonded out : 6 input/output latches are available.
- Programmable ports : DX1, DR1, and TSX1 are bonded out : 2 PCM port are available.
- Serial interface : CI and CO are separated.
- Clock inputs : BCLK and MCLK are not bonded together, providing two separate clock inputs.

2. SCHEMATIC DIAGRAM

TRANSFORMER SLIC

The design of the transformer is greatly simplified, due to the on-chip hybrid balance cancellation filter : Only one single secondary winding is required (see fig. 1). ZT is the line termination impedance as reflected through the transformer (impedance measured between Tip and Ring) : its value is determined by the administration requirements and the transformer characteristics.

ZT provides an echo : a part of the receive signal on VFRO is injected into the transmit path VFXI. The internal hybrid balance filter is designed in order to replicate the echo path, and thus to cancel it.

In this application, the input/output latches are used as relay drivers (buffered through an external transistor) : ring relay, test relays... and line monitoring : off-hook detection, ground key detection. Thus, the card controller can monitor the whole line card module through the unique control port of the TS5070/71 COMBO II.

When the CS pin is held high by the card controller (chip disabled), the CO output of the TS5070 is placed in a high impedance state, allowing several TS5070/71 COMBO II to share the same data link.

SGS-THOMSON MICROELECTRONICS SLIC AND THE TS5070/71 COMBO II : A KIT APPROACH

SGS-THOMSON Microelectronics provides now solid-state monolithic SLICs. These chip-set (a high voltage line interface and a low voltage control unit), associated with the TS5070/71 COMBO II and the especially designed protection components, feature all the BORSCH functions (i.e. Battery feeding, Overvoltage protection, Ringing injection, Supervision of the loop, Codec/Filter and Hybrid 2-wire to 4-wire conversion). The versatility of these kits allows an easy adaptation for the different Telecom Administrations requirements throughout the world.

The schematic diagrams are detailed in fig. 2 and 3. When using the TDB7711, or the L3030, serial interface SLIC, the control interface must be directly connected to the card controller through a separate serial data link for informations exchange between the SLIC and the card controller (see fig. 2).

When using the L3090 PABX dedicated SLIC, its parallel control interface allows the use of the IL interface latches of the TS5070/71 COMBO II (see fig. 3).

The ZAC impedance synthesizes the output impedance of the SLIC on Tip & Ring ; hence, this network should be designed differently for each country. The structure of this network is a copy of the line impedance ; please, refer to the relevant SLIC data-sheet for more details. The "balancing" network, ZA and ZB is used by the SLIC to balance the 2-wire/4-wire conversion. When using the TS5070/71 COMBO II, this balancing network is reduced : 2 single resistors, the main part of the hybrid balancing is performed by the "Hybal" filter of the Combo.

3. PROGRAMMING THE TS5070/71 COMBO II

The control information of the TS5070/71 COMBO II require 2 bytes of informations, with the exception of a single-byte power-up/down command.

When CS is pulled low a first "instruction" byte is shifted into the TS5070 COMBO II, at pin CI (or CI/O for the TS5071) on the falling edge of each CCLK clock pulse, the most significant bit first. During the 8th (dummy) bit, the content of this instruction is decoded by the Combo and, depending wether a "read" or a "write" instruction is performed, a second "data" byte is shifted into or shifted out from the Combo.

* Bit #1 is the single-byte control bit : when 0, this is a single-byte power-up/down instruction, no data byte is expected.

* Bit #2 is the read/write control bit : when 0, the data byte will be written by the card controller into the Combo. When 1, the data byte will be read by the card controller from the Combo.

* Bit #3, 4, 5, 6 specify which one of the 10 registers of the TS5070/71 COMBO II is to be accessed.

* Bit #7 is the power control bit : when 0, the Combo is placed in power-up state ; when 1, the Combo is placed in power-down. Note that the power state can be set in any instruction.

* Bit #0, the last bit, is a dummy bit to allow for decoding of the 7 previously entered bits. Its value is not taken into account and has no influence on the TS5070/71 COMBO II operation.

When writing to the TS5070/71 COMBO II, the data byte may follow the instruction byte immediately, or CS may be pulled high between the 2 bytes. The data byte is shifted into the Combo in the same way as the instruction byte : MSB first, on the falling edge of each CCLK clock pulse.

When reading from the TS5070 COMBO II, the data byte is shifted out, onto the CO pin (CI/O pin for the TS5071), MSB first, on the rising edge of each CCLK clock pulse. As for the write operation, CS can be pulled high between the instruction and the data byte.

After a read or a write operation is completed, it is recommended, although this is not mandatory, that the CS pin should be put high to reset the control port logic.

The content of the instruction byte is detailed in table 1 :

Table 1 : Instruction Byte.

Bit #	7	6	5	4	3	2	1	0
Single Byte Power-up/down	P	X	X	X	X	X	0	X
Control Register	P	0	0	0	0	W	1	X
Latch Direction Register	P	0	0	1	0	W	1	X
Interface Latch Register	P	0	0	0	1	W	1	X
Receive Time-slot/port	P	1	0	0	1	W	1	X
Transmit Time-slot/port	P	1	0	1	0	W	1	X
Receive Gain Register	P	0	1	0	0	W	1	X
Transmit Gain Register	P	0	1	0	1	W	1	X
Hybrid Balance Register # 1	P	0	1	1	0	W	1	X
Hybrid Balance Register # 2	P	0	1	1	1	W	1	X
Hybrid Balance Register # 3	P	1	0	0	0	W	1	X

P = Power control bit : "0" = Power-up, "1" Power-down
W = Read/Write control bit : "0" = Write, "1" = Read
X = don't care (0 or 1)

DATA BYTE : CONTROL REGISTER

The content of the control register is detailed in table 2 :

Table 2 : Control Register.

Bit Number								Function
7	6	5	4	3	2	1	0	
0	0							MCLK = 512KHz
0	1							MCLK = 1.536 or 1.544MHz
1	0							MCLK = 2.048MHz*
0	1							MCLK = 4.096MHz
		0	X					μ-255 Law*
		1	0					A-law, with Even Bit Inversion
		1	1					A-law, no Even Bit Inversion
				0				Delayed Data Timing
				1				Non-delayed Data Timing*
					0	0		Normal Operation*
					1	X		Digital Loopback
					0	1		Analog Loopback
							0	Power Amp Enabled in PDN
							1	Power Amp Disabled in PDN*

* = State at power-on initialization.

The * specifies the default value of the control register at the power-on initialization.

MCLK : Master clock used by the Combo's filters, encoder and decoder. It is necessary to indicate which frequency is beeing applied to the Combo, for a correct filter operation.

COMPANDING LAW : the μ-255 **com**pressing and ex**panding** law is used in USA & Japan, A-law in Europe. Usually, in A-law, even bits are inverted : 0000 0000 becomes : 0101 0101 ; if this even bit inversion is performed in another part of the switching system, a "No even bit inversion" is available.

DATA TIMING : In Non-delayed Data Timing mode, the time-slot always begin with the rising-edge of FSX or FSR ; Time-slot Assignment is not available in this mode.
In Delayed Data Timing mode, time-slot begins after a falling edge of BCLK, when FSX or FSR is set high ; the Time-slot Assignment feature of COMBO II can be used in this mode only.

Note that PCM port selection is available in both timing modes.

LOOPBACK : Test modes : In Analog Loopback, VFXI is isolated from input pin and internally connected to the VFRO output, providing a complete D to D test loop.

In Digital Loopback, the PCM byte written into the Receive register, can be read back in any Transmit Time-slot at DX0 (or DX1) pin.

POWER AMP : if "1", the power amplifier, at VFRO output is disabled during the power-down state, i.e. VFRO pin is high impedance state.

It is very easy to set the TS5070/71 COMBO II configuration in any "U.S." or "European" environment.

In the following example, the line card module must be adapted to an european telecom administration specifications ; should be selected :

- Master clock = 2.048MHz
- A-law with even bit inversion
- Delayed data timing (which allows the Time-slot assignment feature)
- Normal operation (no loop back)
- Power amp disabled in power-down

Consequently, the instruction byte 10000010 (82 hexadecimal), followed by the data byte "10100001" (A1 hexadecimal) should be written into the COMBO II.

DATA BYTE : LATCH DIRECTION REGISTER

Bit Number							
7	6	5	4	3	2	1	0
L0	L1	L2	L3	L4	L5	X	X

* The bits #7 to #2 specify the function of each interface latch pin ; bit #0 and bit #1 are dummy bits.
* If Ln = 0 then ILn is a high-impedance input.
* If Ln = 1 then ILn is an output.

Notes : - unused pins should be programmed as outputs.
- When using the TS5071 the IL5 pin should be programmed as an output.

In the case of a L3090 SLIC, as described in fig. 3, IL0 pin, IL1 and IL4 are connected to L3090 inputs : they must be programmed as outputs. IL2 and IL3 must be set as inputs, because they are connected to L3090 outputs and IL5 is not used : this pin should be set as output.

In this example a "11001100" (CC hexadecimal) code should be written into the Latch Direction Register.

DATA BYTE : INTERFACE LATCH REGISTER

Bit Number							
7	6	5	4	3	2	1	0
D0	D1	D2	D3	D4	D5	X	X

X = Don't Care.

* When writing to this register, the IL pins programmed as outputs assume the state of the corresponding bit Dn, in data byte.

* When reading from this register : for the IL pins programmed as outputs, the Dn bits correspond to the data previously written in this register ; for the IL pins programmed as inputs, the Dn bits correspond to the data read by these input pins.

In the case of the L3090 (fig. 3), if the SLIC must be put in "stand-by" mode, i.e. PWON and RNG pins = 0 and NCS = 1, "00001000" (08 hexadecimal) should be written into the Interface Latch Register. Note that bit #5 and bit #4 have no effect, since the IL2 and IL3 pins are programmed as input.

DATA BYTE : RECEIVE TIME-SLOT REGISTER AND TRANSMIT TIME-SLOT REGISTER

Bit Number and Name								
7 EN	6 PS	5 T5	4 T4	3 T3	2 T2	1 T1	0 T0	
0	1	X	X	X	X	X	X	Disable DX Outputs (in TX reg.) Disable DR Inputs (in RX reg.)
1	0	Time-slot (0-63)						Enable DX0 Output, Disable DX1 (in TX reg.) Enable DR0 Input, Disable DR1 (in RX reg.)
1	1	Time-slot (0-63)						Enable DX1 Output, Disable DX0 (in TX reg.) Enable DR1 Input, Disable DR0 (in TX reg.)

* The 6 bits T5-T0 assign one time-slot from 0 to 63 (111111 in binary) ; available in Delayed Data Timing only.

* The PS "Port Selection" bit #6 selects the DR0 input, when 0, or the DR1 input, when 1, in the Receive Time-slot register, and, respectively DX0 or DX1 output in the Transmit Time-slot register.

Note : On the TS5071 the DR1 and DX1 pins are not bonded out : the PS bit must always be set to 0.

* The EN bit enables (when 1) the PCM input or output selected by the PS bit or disables them (when 0).

Note : the disabled pins are in a high impedance state.

In the above example, "Delayed Data Timing" was selected in the Control Register : when using the DX0/DR0 PCM port, time-slot #5 for transmission and time-slot #27 for reception, the contents of the TX time-slot and RX time-slot registers must be : "10000101" (85 hexadecimal) and "10011011" (9B hexadecimal).

DATA BYTE : TRANSMIT GAIN AND RECEIVE GAIN REGISTER

The TS5070/71 COMBO II includes a transmit and a receive programmable amplifier ; these amplifiers allow an easy setting of the transmission level point (0TLP = 0dBm0) of the COMBO II, within the specified limits. The following formulas give the 2 bytes to be programmed in the TX and the RX gain registers :

200 X log10 (V_{VFXI} / $\sqrt{0.6}$) + 191, for the TX Gain Register, converted in binary.

200 X log10 (V_{VFRO} / $\sqrt{0.6}$) + 174, for the RX Gain Register, converted in binary.

V is the desired analog voltage, at VFXI pin for TX gain and VFRO pin for RX gain, expressed in Vrms, and corresponding to a digital 0dBm0 PCM level, as defined in CCITT G.711 ; the transmit input signal at VFXI must be in the range of 0.087 to 1.619Vrms, and the output receive amplifier at VFRO provides a signal from 0.106 to 1.96Vrms (for a 0dBm0 PCM signal).

The TX and RX gains can be also calculated from

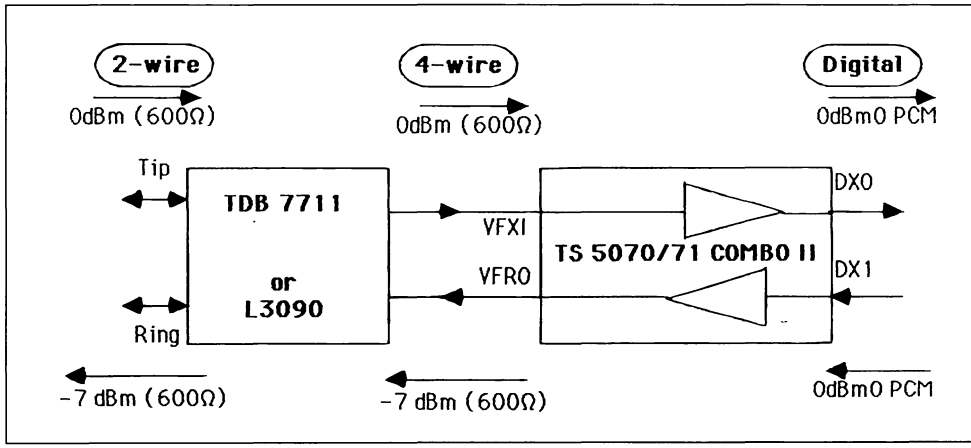
the desired analog levels at VFXI and VFRO expressed in dBm into 600Ω ; in this case, the bytes to be programmed are calculated as follows :

10 X (VFXI level in dBm 600Ω) + 191, for the TX Gain Register, converted in binary.

10 X (VFRO level in dBm 600Ω) + 174, for the RX Gain Register, converted in binary.

Refer to the following example (fig. 4) :

Figure 4 : Example of TX and RX Levels.



- the transmit signal is 0dBm (600Ω) on Tip-Ring wires for a 0dBm0 PCM level at the DX0 output.
- the receive signal is - 7dBm (600Ω) on Tip-Ring wires for a 0dBm0 PCM level at the DR0 input.

The 0dBm0 PCM level is the bit sequence defined in the CCITT recommendation G.711.

We must first determine the analog levels at VFXI input and VFRO output of the TS5070/71 COMBO II. Due to their "feedback loop" structure, the SGS-THOMSON SLICs always have a unity gain, in both transmit and receive direction. Consequently, the analog level at VFXI input will be : 0dBm (600Ω) = 0.7746Vrms, and the output level at VFRO : – 7dBm(600Ω) = 0.346Vrms.

The TX gain to be programmed in the TS5070/71 COMBO II will be :

10 X (0dBm) + 191 = 191 = BF hexa = 10111111 binary

this byte must be written in the TX gain register.

The RX gain will be :

10 X (- 7dBm) + 174 = 174 - 70 = 104 = 68 hexa = 01101000 binary

this byte must be written into the RX gain register.

These programmable gains provide more flexibility for the design of the line-card : if the transmit signal is - 8dBm instead of 0dBm, it is easy to re-program the TX gain register :

10 X (- 8dBm) + 191 = 191 - 80 = 111 = 6F hexa = 01101111 binary

In this case, TX gain must be set to 111 decimal = 6F hexadecimal = 01101111 binary. It is easy to adapt this example to any particular configuration. The designers shall notice that the gains are adjusted in 0.1dB steps. Consequently, the gain for - 8dBm will be 80 steps below the gain for 0dBm, i.e. 191 - 80 = 111.

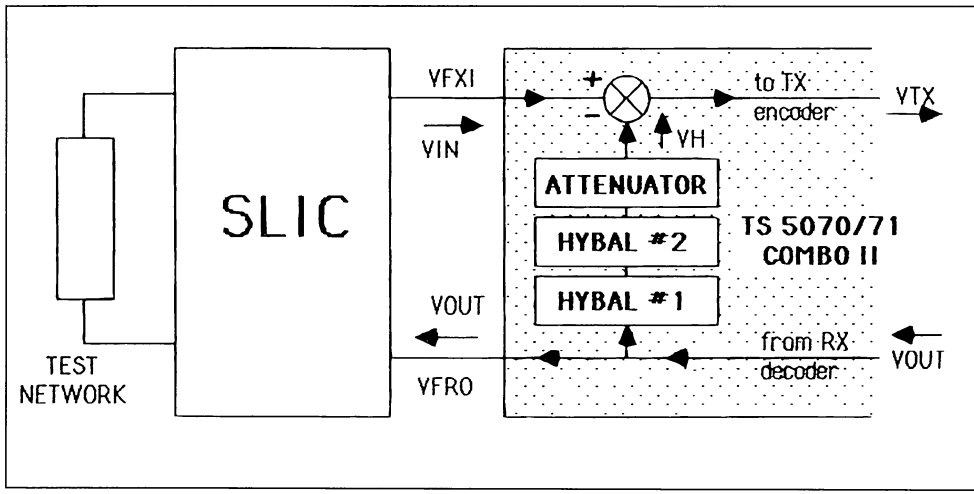
Note that if the analog output level, at VFRO, exceeds 1.7Vrms, for a 0dBm0 PCM input at DR0, there are some restrictions on the value of the load connected at VFRO :

- if the level is less than 1.7Vrms, the load impedance must be greater than 300Ω
- if the level is between 1.7Vrms and 1.9Vrms, the load impedance must be greater than 600Ω
- if the level is between 1.9Vrms and 1.96Vrms, the load impedance must be greater than 15KΩ

4. HYBRID BALANCING

The hybrid balance filter of the TS5070/71 COMBO II is entirely programmable : the "zero" and "pole" combinations for the low frequency Hybal filter #1 and the high frequency Hybal filter #2 can be set by the card controller ; in addition, a programmable attenuator adjust the amplitude of the cancellation signal (see fig. 5).

Figure 5 : Hybrid Balance Cancellation Filter.



The Hybrid Balance Filter is set by the contents of 3 registers ; an optimization software (TS5077) determines the 3 bytes to be written in these registers.

ECHO PATH OF THE SLIC

The first step for the calculation of the Hybrid Balance Filter is the echo path of the SLIC : VIN/VOUT (see fig. 5). The amplitude and the phase of the echo signal must be determined for 14 frequencies, from 200 to 3500Hz. A "Hybrid Balance" test network must be connected between Tip and Ring wires.

The echo path can be measured or calculated by simulation of the transfer function of the SLIC. The TS5077 optimization software includes a simulation module for a transformer SLIC.

OPTIMISATION SOFTWARE

The echo path must be entered into the program, for each balancing network, then the optimization routine is run. This routine tests all the combinations of the Hybrid Balance Filter and selects the one which is the closest to the echo path, and then provides the three bytes to be programmed into the three Hybrid Balance registers. Some optimization examples with the different SLIC kits from SGS-THOMSON Microelectronics are described in the Application Note "COMBO II Hybal optimization with STM's SLIC kits".

5. CONCLUSION

These examples show the great flexibility of the TS5070/71 COMBO II in its adaptation with different line-cards, different SLICs and different countries. This flexibility, coupled with the programmable features, enhance the integration of the line-card : more subscribers per board, more reliability, easier adaptation, ... and, last but not least : a significant reduction of the total cost of the line card.

Figure 1 : Interface with Transformer SLIC.

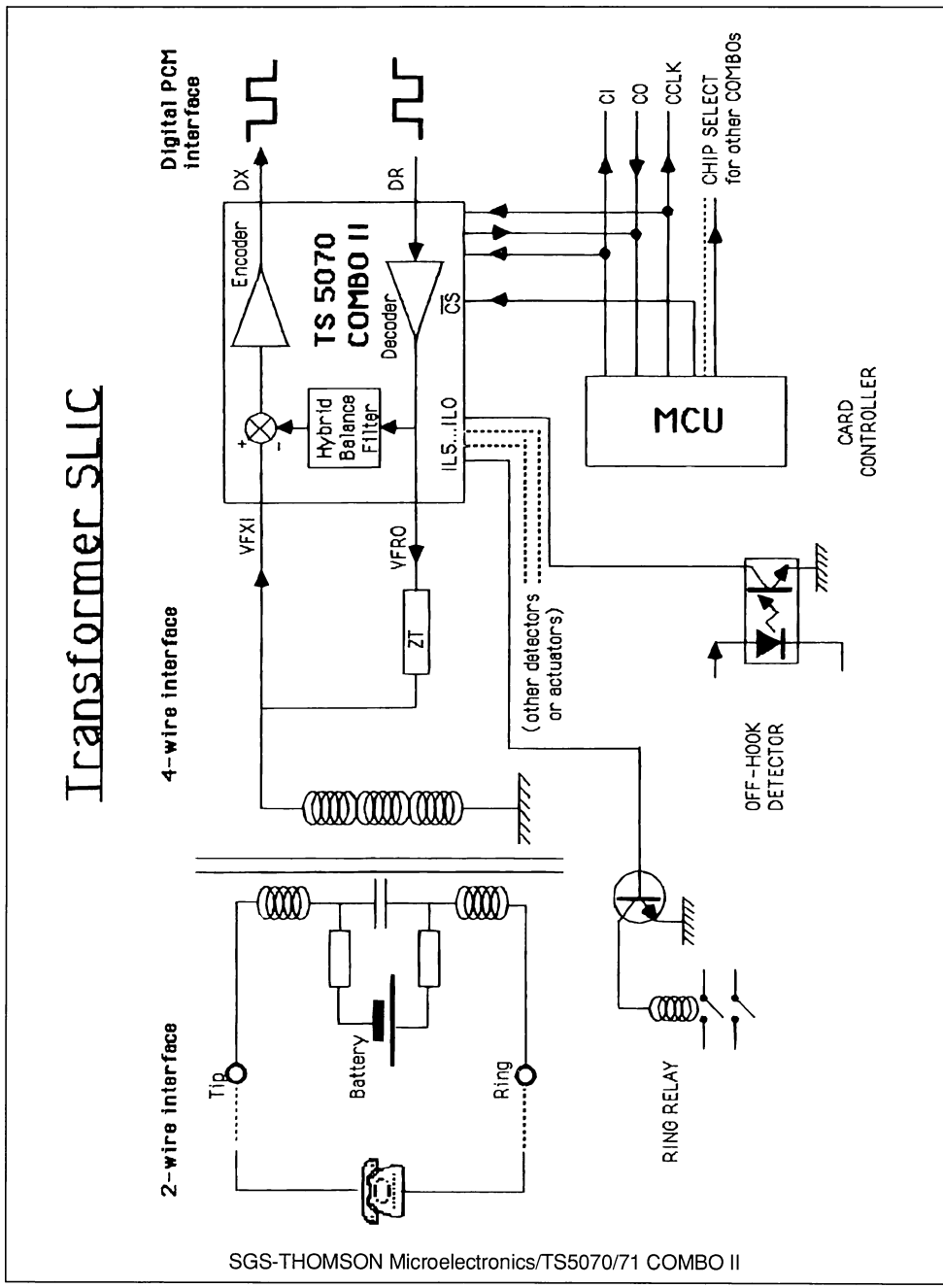


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Figure 2 : Interface with TDB 7711 + 7722 Solid-state SLIC.

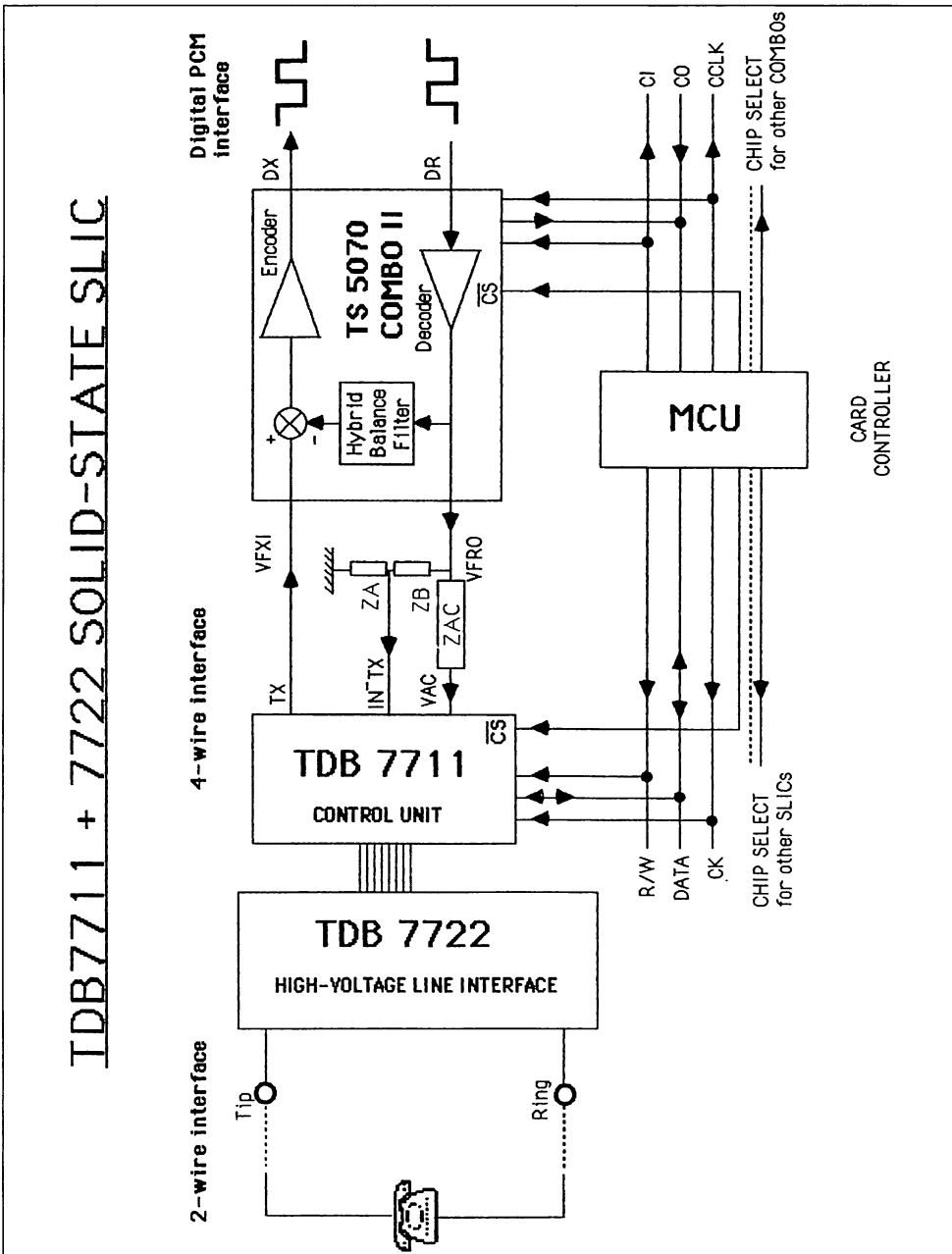

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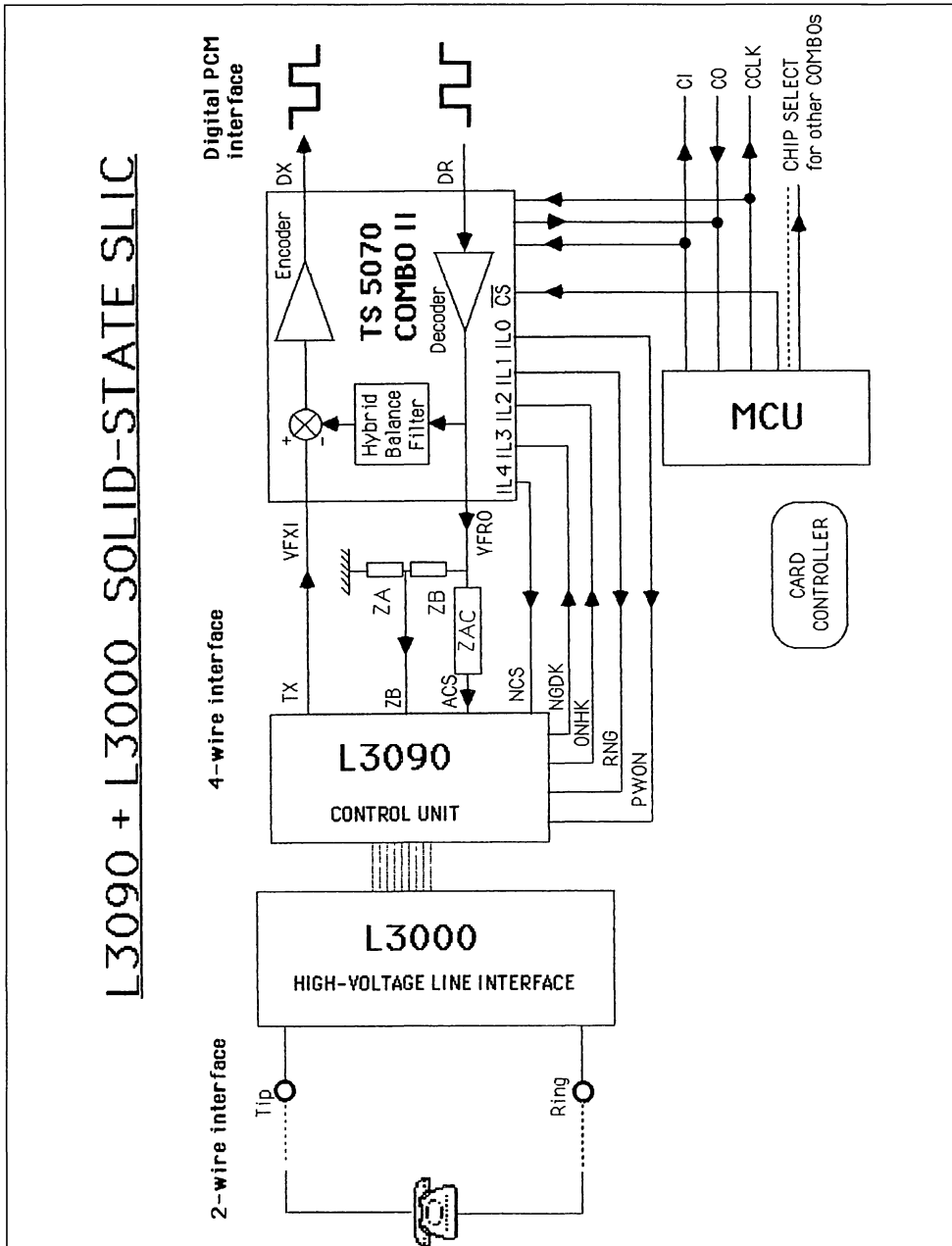
Figure 3 : Interface with L3090 + L3000 Solid-state SLIC.



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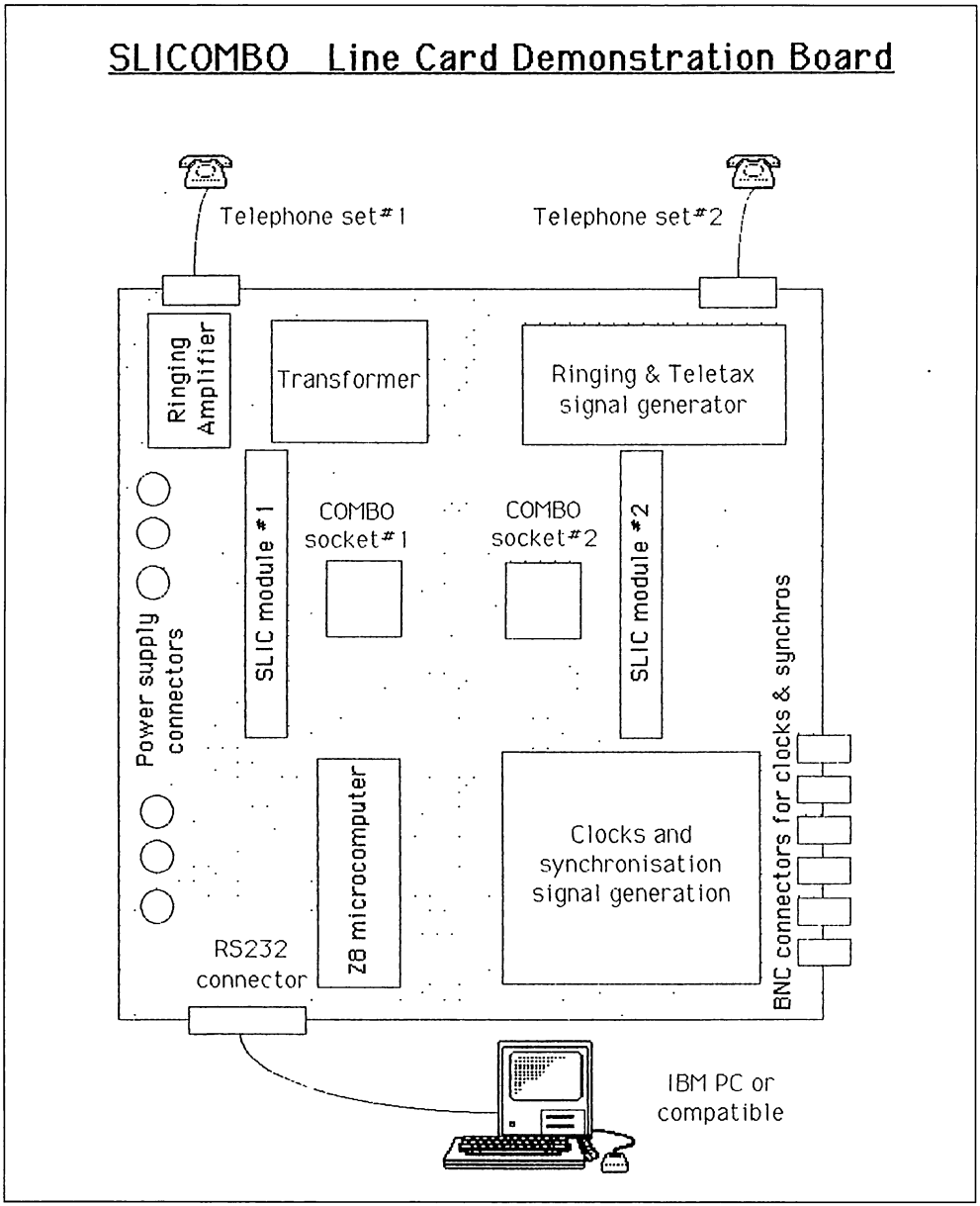


SLICOMBO is a conversational demonstration board for the subscriber line card oriented circuits developped by SGS-THOMSON Microelectronics. It includes two complete transmission modules, each of them made of a programmable codec/filter COMBO II associated with a full silicon SLIC to achieve the "BORSCH" function (**B**attery feed, **O**vervoltage protection, **R**inging, **S**ignalling, **C**o-dec/filter, **H**ybrid 2-wire/4-wire conversion).

The 2-wire interface of each SLIC can be connected to a telephone set or to an appropriate test equipment. The PCM interface of the 2 COMBOs can also be connected to a PCM test equipment, or to the same PCM highway, thus allowing a real phone conversation between the 2 telephone sets through the 2 SLICs and the 2 COMBOs.

As SGS-THOMSON Microelectronics provides a wide range of SLICs, they are implemented on interchangeable modules ; 2 modules are available : one version is for the central office oriented SLIC TDB7711/7722, and one version for the PABX oriented SLIC L3090/L3000. SLICOMBO can operate either with 2 TDB7711 or with 2 L3090 SLIC modules.

The mother-board includes a ringing signal and teletax metering signal generator, a ringing signal amplifier, for the SLICs, a master clock, bit clock and frame synchronization signal generator for European (4096KHz and 2048KHz) and North-American frequencies (1536KHz).

The card controller is a single-chip Z8 microcomputer : the Z86E11A includes 4K bytes of on-chip EPROM, 48-bit I/O ports, a serial asynchronous I/O port and runs with a 11.0592MHz clock in order to provide a 9600 bits/sec baud rate to the SIO. The Z8 manages the programming of the internal registers of the 2 COMBOs and the 2 SLICs ; the Z8 also manages the different clocks and synchronization signals that must be applied to the COMBOs.

The user interface with the board is performed by an IBM Personnal Computer or true compatible. An interactive software inputs the commands from the user and displays the results on the screen ; a multi-menus approach is used by the software to make easy the programming of the SLICOMBO board. The PC sends the commands to the Z8 on the SLICOMBO board through a RS232 data link : the Z8 executes the command and sends back the result to the PC for checking.

For availability of this board, please contact your local SGS-THOMSON Microelectronics sales office.

SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE

SLIC L3000/L3090 MAXIMUM LOOP RESISTANCE ANALYSIS

By W. Rossi , A. Pariani

1. INTRODUCTION

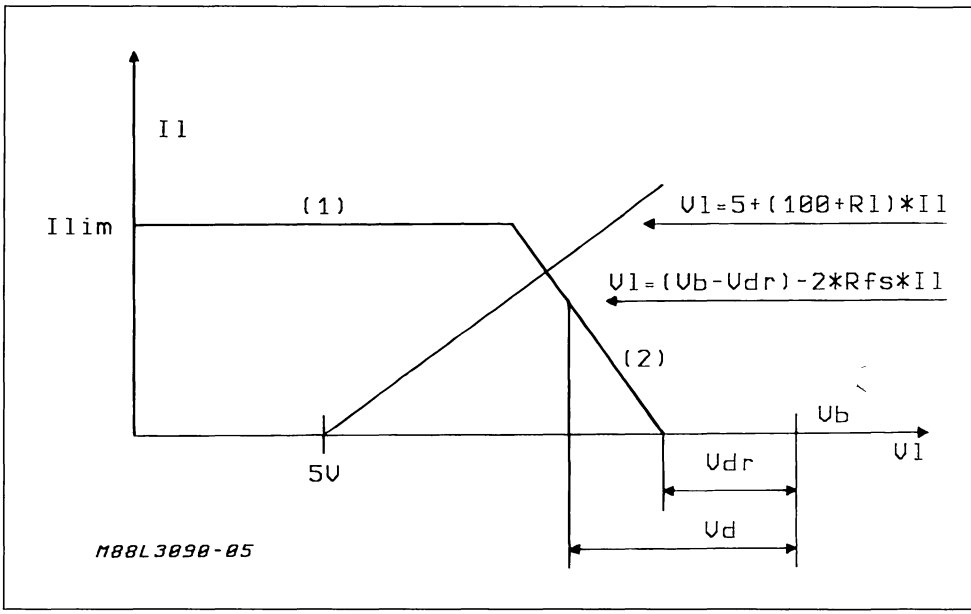
This evaluation was carried out in order to evaluate the maximum loop resistance allowed using the SLIC KIT L3000/L3090, the best for PABX applications.

The evaluation is performed in conversation mode ; it shows how the maximum loop resistance (Rl) is influenced by the battery voltage (Vb), the feeding resistance (Rfs) and the common mode current (Icm).

2. MAXIMUM LOOP RESISTANCE EVALUATION

In fig. 1 you can see the L3090 DC characteristic and the load curve. The load curve is obtained as the series of the loop resistance (Rl) and the subscriber telephone set. The subscriber telephone set is represented as the series of a 100Ω resistor and a 5V zener diode.

Figure 1 : SLIC Characteristic and Load Curve.



If the operating point is on region (1) its coordinates are :

Il1 = Ilim

Vl1 = 5 + (100+Rl)xIlim (1)

Note : The slope of region (2) is 2xRfs where the feeding resistor Rfs is fixed by an external resistor.

If the operating point is on region (2) you can find its coordinates solving the system of two equations :

1) Vl = (Vb-Vdr)-2xRfsxIl

2) Vl = 5+(100+Rl)xIl

obtaining :

Il2 = (Vb-Vdr-5)/(100+Rl+2*Rfs)

Vl2 = 5+(100+Rl)x(Vb-Vdr-5)/(100+Rl+2xRfs) (2)

If you consider the DC characteristic of the device you can see that the longer is the line the lower is the voltage drop between the battery voltage (Vb)

and the line voltage (Vl). It can happens that for very long line the voltage drop is not large enough to guarantee the fully AC performance of the device. In such condition the device is still working, but large signal can appear slightly distorted on the line. If you want guarantee the optimum behavior of the device you must be sure that the operating point of the device (Il, Vl) satisfy the following condition :

Vl ≤ Vb-Vd

with Vd=5+100xIl+60xIl+2+Vdcm

where :

5 : internal drop

100xIl : drop on sensing resistors (2x50Ω max)

60xIl : drop on external resistors (2x30Ω)

2 : maximum AC signal peak

Vdcm : (=100xIcm) drop for common mode current (Icm)

You can obtain the maximum value for Rl (maximum loop length) imposing :

Vl = Vb-Vd

If the operating point is on region (1) solving the equation Vl1=Vb-Vd where Vl1 is given by the relation (1) you obtain :

Rlmax= (Vb-12-260xIlim-100xIcm)/Ilim (3)

If the operating point is on region (2) solving the equation Vl2=Vb-Vd where Vl2 is given by the relation (2) you obtain :

Rlmax = ((100+2xRfs)x(Vb-12-100xIcm)-260x(Vb-Vdr-5))/(7-Vdr+100xIcm)

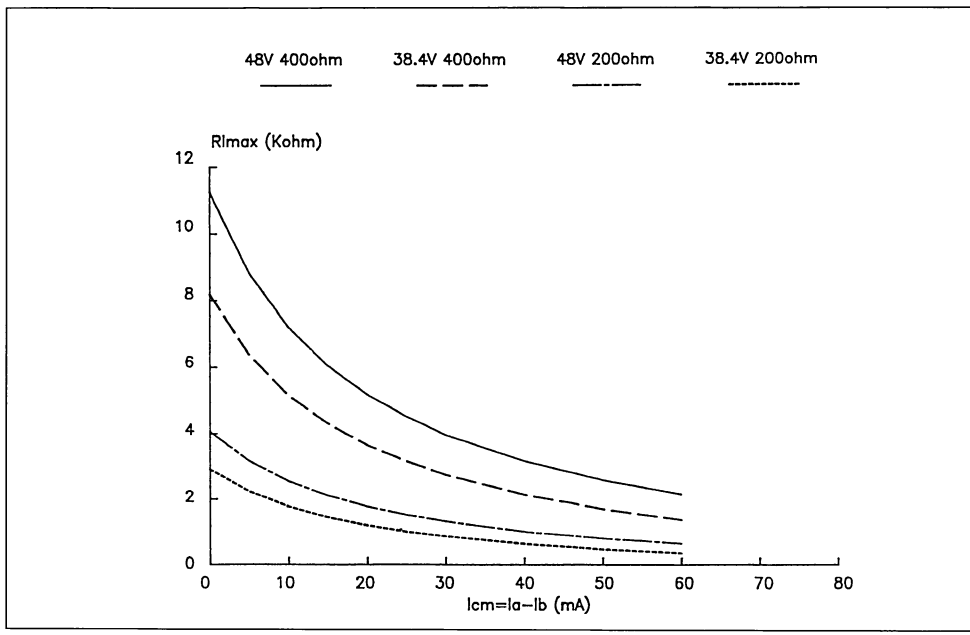
In the following you can find graphical representations of Rlmax versus Icm in four different situations :

3. CONCLUSION

The above relations show the possibility to work with good performances also in presence of common mode current. With a battery voltage of –48V, Rfs = 200Ω and no common mode current, the maximum loop resistance is over 3KΩ ; in the same condition but with a common mode current of 20mA the maximum loop resistance is about 2KΩ. Higher loop resistance can be obtained increasing Rfs (see fig. 2).

The parameters of each curve are the battery voltage (Vb) and the feeding resistance (Rfs).

Figure 2 : Maximum Line Resistance Versus Common Mode Current (conversation mode).



SLIC L3000/L3090 PERFORMANCE ANALYSIS WITH –24V BATTERY

By W. Rossi ; F. Falcini

1. INTRODUCTION

This technical note describes the L3000/L3090 SLIC performances when used with a battery voltage of – 24V. All the main characteristics are analyzed and compared with the results obtained with a standard battery voltage of – 48V.

The following data were obtained from a typical device in order to have an idea on how DC characteristic, power consumption, ringing voltage and AC performances are influenced by a reduced battery voltage.

2. POWER CONSUMPTION

Table 2.1 shows the L3000-L3090 current consumption with the battery voltage of – 48V and – 24V. The measurements are made in the different operating modes (Power Down ; Stand-By ; Conversation with IL = 0 ; IL = 44mA and Ringing without AC Line Load (Ringing Equivalent Number REN = 0).

Table 2.1 : Slic Current Consumption with Different Battery Voltages.

	Current Consumption (mA)			
	– 48V	**+ 72V**	**– 24V**	**+ 72V**
PW - DOWN	0	0	0	0
SBY (IL = 0)	3.3	0	3.1	0
CVS (IL = 0)	10.6	0	9.7	0
CVS (IL = 44mA)	61.1	0	60.9	0
RING (0 REN)	23.9	15.4	21.8	13.4

You can see that using – 24V of battery voltage we have a reduction of the power consumption of more than the 50% in STD-BY and CVS and of about 35% in RING mode.

3. DC CHARACTERISTICS

In fig. 3.1. you can see the typical DC characteristics for the two battery voltages ; feeding resistance was set to 2x200Ω.

3.1. MAXIMUM LOOP LENGHT

Two are the parameters influenced by line length increment : the first is the DC line current and the second is the maximum AC signal that can be sent without distortion (THD 1%), see AN294. Here below are shown the maximum loop resistance values and the relative line current in correspondance of which distortion is still less than 1% for +4dBm (1.23 VRMS) AC signals. The SLIC feeding resistance is set to 2 x 200Ω.

Vbatt. = – 48V	Vbatt. = – 24V
Rmax. = 2200Ω	Rmax. = 940Ω
IL = 16.61mA	IL = 14.47mA.

3.2. ON/OFF HOOK CURRENT THRESHOLDS

Here below are reported the typical values of the DC current thresholds used by the SLIC to detect the ON hook and OFF hook line conditions.

Vbatt. = – 48V

ON/OFF Hook commutation.

IL = 8.10mA VL = 40.58V RL = 5KΩ

OFF/ON Hook commutation.

IL = 5.91mA VL = 41.30V RL = 7KΩ

Vbatt. = – 24V

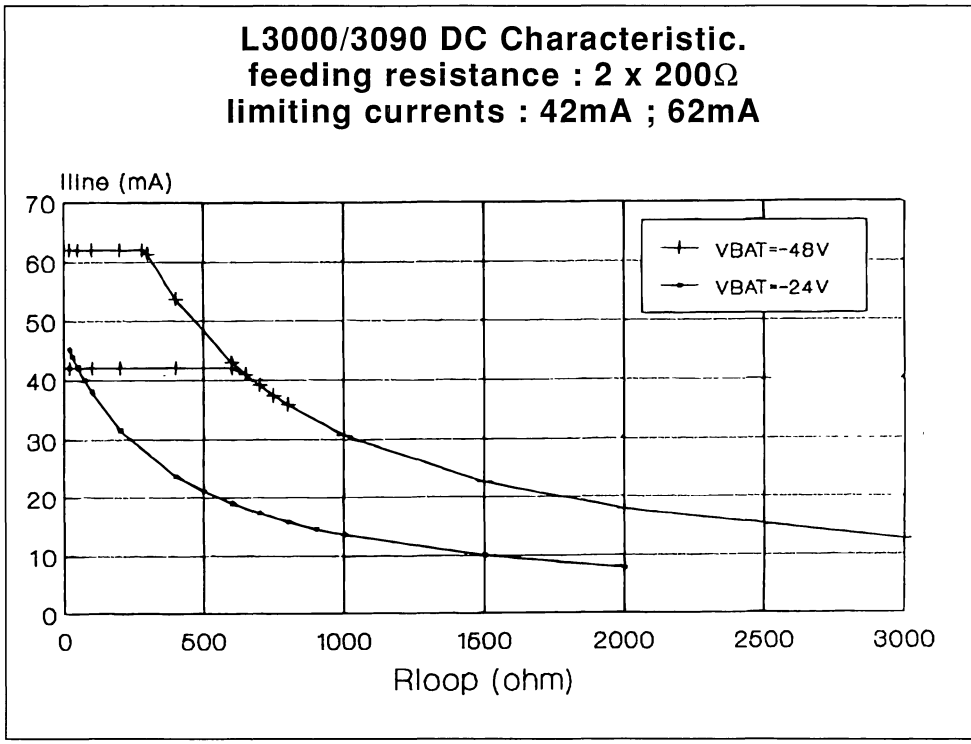
ON/OFF Hook commutation.

IL = 8.24mA VL = 16.52V RL = 2KΩ

OFF/ON Hook commutation.

IL = 5.82mA VL = 17.44V RL = 3KΩ

Figure 3.1 : DC Characteristic with a 2 x 200Ω Feeding Resistance.



4. AC PERFORMANCES

All the AC performances : TXgain, RX gain, Return Loss, Transhybrid Loss and Longitudinal Balance were measured and no significative variations were found changing from – 48V to – 24V of battery voltage.

GRX, GTX and THL variation were inside .03dB ; RL inside .07dB and longitudinal balance inside .9dB.

5. RINGING PERFORMANCES

L3000/L3090 SLIC injects directly the ringing signal into the line. The ringing signal has a DC component superimposed with the AC one. Here below you can see the measured values of these DC and AC voltages with a positive supply of + 72 and a battery voltage of -48V and -24V.

5.1. DC LEVEL

Vbatt. = – 48V

Vdc = + 21.06V

Vbatt. = – 24V

Vdc = + 17.68V

5.2. MAX AC LEVEL (Volts RMS) WITH A DISTORTION THD < 4%

Vbatt. = – 48V

Vac = 70.58V (RMS)

Vbatt. = – 24V

Vac = 47.30V (RMS)

6. CONCLUSIONS

The measurements carried on show that it is possible to make the SLIC working also with reduced battery voltage (down to – 24V) without any degradation in terms of AC performances.

It should be noted that with – 24V battery voltage you can get good performances up to 950Ω of loop length. In case you need higher line currents you can increase the battery voltage of the amount you need, optimizing in this way power dissipation.

SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE

SLIC L3000/L3090 USED IN KEY SYSTEM AND ANALOG PABX

By W. Rossi ; A. Pariani

1. L3000/L3090 SLIC KIT ; MAIN CHARACTERISTICS :

* Programmable DC feeding resistance and limiting current (two values available).
* Four operating modes (PW-DOWN/SBY/CVS/RNG).
* Signalling function (OFF-HOOK/GND-KEY).
* Hybrid function.
* Possibility to work with reduced battery voltage (- 24V).
* **Possibility to work in two-wire configuration.**
* Ringing generation with quasi zero output impedance, zero crossing injection (no external relay needed) and ring trip detection.
* Automatic ringing stop when OFF-HOOK is detected.
* Parallel latched digital interface (5 pins).
* Low number of standard tolerance external components, only 9 1% resistors and 4 10-20% capacitors (for 600Ω appl.)
* Possibility to work also with high common mode currents.
* Integrated thermal protection.

2. L3090/L3000 INTERNAL STRUCTURE

Here below you can see the simplified internal structure of the L3090/L3000 SLIC KIT and how it is possible to make it working in a two wire configuration. The output stage (L3000) is represented as single ended only to have a simplified model.

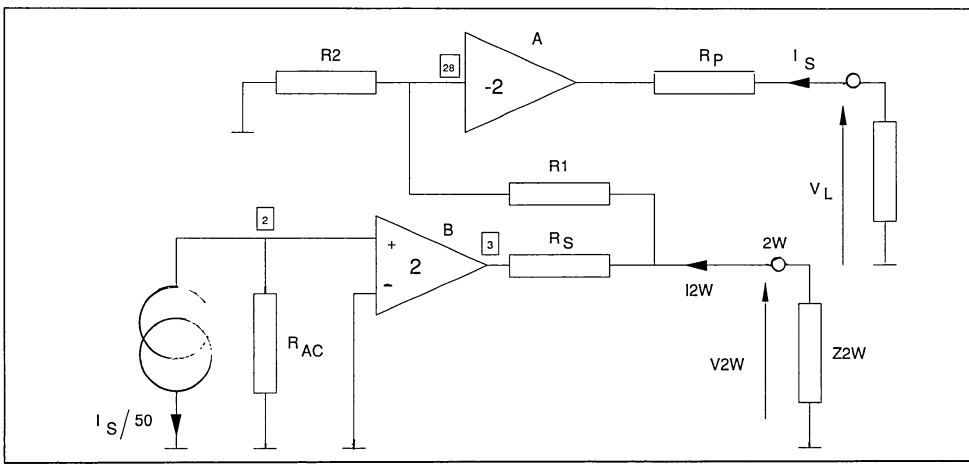
- Rac ; R1 ; R2 ; and Rs are external components, can be real or complex and are chosen in order to set the desired AC performances of the system.

- Rp is equal to the sum of the two external series resistor on the line.

- Z2w is the load impedance at the two wire termination and represents the input impedance at the same point of another SLIC in the same configuration.

If you look at fig. 2.1 it is evident that both the transmit and receive signals are present at the 2W point (typical for a two wire configuration). In fact if you suppose to inject a signal in the 2W point it will be transferred to the line through the A amplifier after a partition on the R1 ; R2 network. On the other side if a signal is applied at the line termination it will produce a current Is that scaled by 50 is fed back and injected on Rac, finally through the B amplifier the line signal is transferred at the 2W termination.

Figure 2.1 : L3090/L3000 Simplified AC Model.



3. HOW TO CHOOSE EXTERNAL COMPONENTS FOR EACH APPLICATION

Analyzing the circuit configuration shown in fig. 2.1 it is possible to obtain all the typical parameters of the system ; in particular, defining G = 2 x R2 / (R1 + R2) the results are :

- Z2w defined as V2w/I2w is the input impedance at the two wire termination :

$$Z2w = \frac{Rs}{1 + G \times Rac/(25 \times (Rp + Rl))} \quad (1)$$

- Zin defined as Vl/Is is the input impedance at the line termination :

$$Zin = Rp + Rac \times (G/25) \times \frac{Z2w}{Rs + Z2w} \quad (2)$$

Substituting the (1) in the (2) you obtain :

$$Zin = Rp + G \times Rac \times \frac{Rp + Rl}{50 \times (Rp + Rl) + G \times Rac} \quad (3)$$

- GTX defined as V2w/Vl is the transmit gain and can be evaluated applying Vl at the line termination and measuring V2w :

$$GTX = \frac{1}{G \times (1 + (Rp/(Rp + Rl)) + 50 \times (Rp/Rac)} \quad (4)$$

- GRX defined as Vl/V2w is the receive gain and can be evaluated applying V2W at the 2W termination and measuring Vl :

$$GRX = -G \times \frac{Rl}{Rl + Rp} \quad (5)$$

The problem is now how to choose the external components in order to obtain the desired value for the above parameters.

Solving the equations (1) ; (3) ; (4) and (5) you can obtain :

From the (5) :

$$R2 = K \times (Zl + Rp) \quad (6)$$
$$R1 = K \times ((2/GRX) - 1) \times Rl - K \times Rp$$

The value of K must be chosen in order to have R1, R2 > Z2w.

From the (4) :

$$Rac = \frac{50 \times Rp \times Zl/GRX}{((1 - GRX \times GTX)/(GRX \times GTX)) \times Rl - 2 \times Rp} \quad (7)$$

From the (3) :

$$Rp = \frac{(1 - GRX \times GTX) \times Zin \times Rl}{Rl + GRX \times GTX \times Zin} \quad (*) \quad (8)$$

From the (1) :

$$Rs = Z2w \times \left(1 + G \times \frac{Rac}{25 \times (Rp + Rl)}\right) \quad (9)$$

If you want to try a different approach in the Appendix you can find the input file for SPICE simulation of the circuit. The components names are the same used in fig. 2.1 and fig. 4.1.

(*) : If you want to keep the possibility to choose Rp not depending on the desired AC parameters of your system you can add a resistor Ro between the 2W termination and Z2w and select its value in the proper way.

4. ONE APPLICATION EXAMPLE

4.1. EXTERNAL COMPONENTS DEFINITION

Once defined the desired specs. (Zin, Z2w, GTX, GRX) from the (6) to (9) it is possible to define all the external components.

Let's suppose you want :

GTX = - 3dB (= .708)

GRX = - 3dB

Zin = 600Ω

Z2w = 600Ω

Substituting in the above relations you obtain :

Rp = 200Ω (from the (8))

Rac = 42.4 KΩ (from the (7))

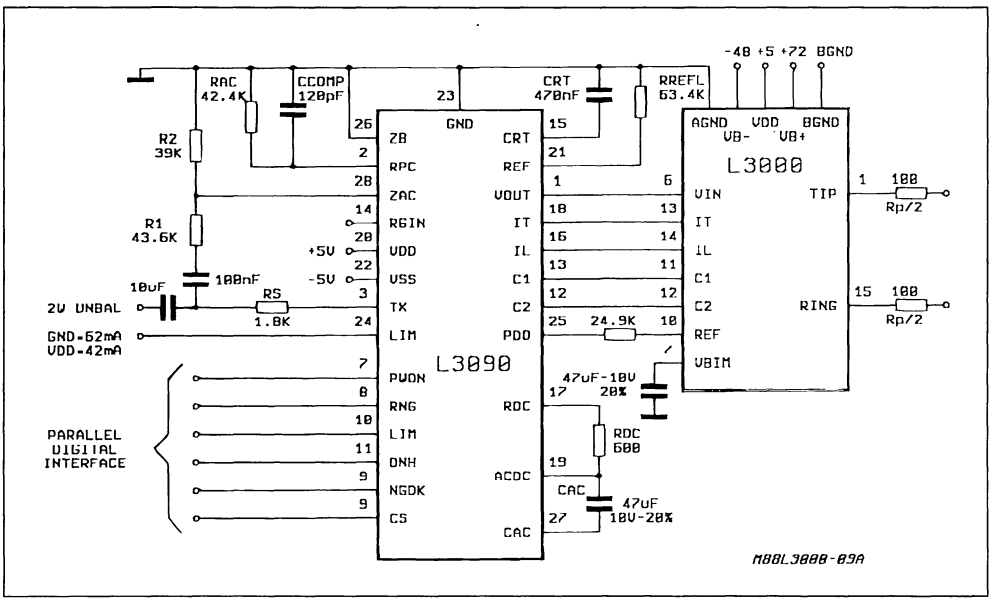
R1 = 43.6 KΩ (from the (6))

R2 = 39 KΩ

Rs = 1800Ω (from the (9))

Here below you can see the complete application diagram for the two wire configuration :

Figure 4.1 : L3090/L3000 SLIC KIT in Two Wire Configuration.



4.2. MEASUREMENTS

Here below you can see the results of some measurements on the application shown in fig. 4.2. The 2w termination is loaded with 600 ohm ; the line impedance is 600 ohm.

Figure 4.2 : Return Loss at Line Termination (Rref = 600Ω).

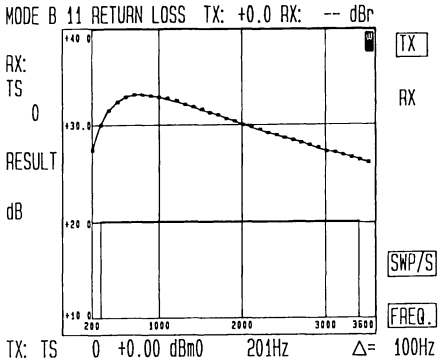


Figure 4.3 : Return Loss at the 2W Termination (Rref = 600Ω).

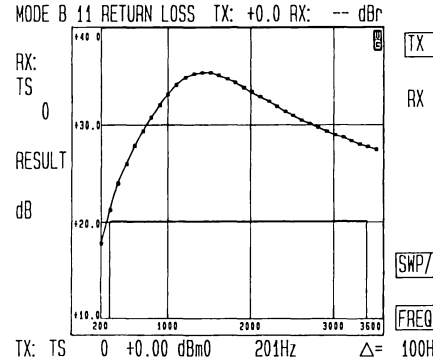


Figure 4.4 : TX Gain Flatness (GTX (1KHz) = –3dB).

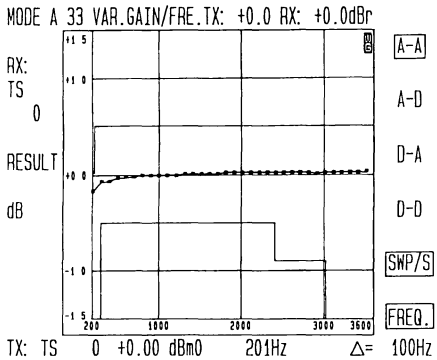
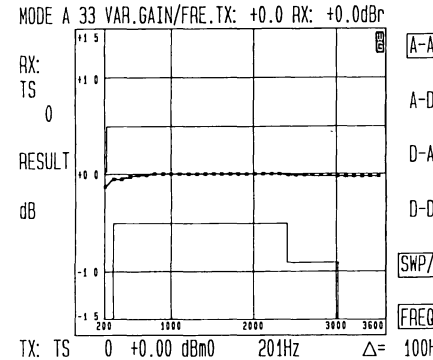


Figure 4.5 : RX Gain Flatness (GRX (1KHz) = –3dB).



```
L3090 2 WIRE AC ANALYSIS

*******************************************
*                                         *
*  SLIC DEFINITION IN 2W CONFIGURATION    *
*                                         *
*******************************************


.SUBCKT SLIC 7 8

******** SLIC EXTERNAL COMPONENTS ***********

RAC 1 0 42.4K
RS 2 3 1.8K
R1 9 4 43.6K
R2 4 0 39.0K
RP 5 6 200
C1 3 8 10U
C2 3 9 100N
CCOMP 1 0 120P

********* END SLIC EXTERNAL COMPONENTS ******


********* SLIC INTERNAL CHARACTERISTICS *****
********* DO NOT MODIFY THESE VALUES !! *****

V1 7 6

F1 1 0 V1 .02

E1 2 0 1 0 2
E2 5 0 4 0 -2

********* END SLIC INTERNAL CHARACTERISTICS *

.ENDS SLIC

*******************************************
*          END SLIC DEFINITION            *
*******************************************


.AC DEC 10 10 10K
.WIDTH IN=80 OUT=80

***** INSERT ONLY ONE OF THE FOLLOWING BLOKS  DEPENDING *********
***** ON WHICH ANALYSIS YOU WANT                         *********

*****************************************************************
*                                                               *
*    ANALYSIS ON ONLY ONE SLIC TERMINATED ON RL (LINE SIDE)     *
*    AND ON R2W (TWO WIRE SIDE)                                 *
*                                                               *
*****************************************************************

**** INPUT IMPEDANCE EVALUATION ********************************
*X1 1 2 SLIC
*R2W 2 0 600
*IL 0 1 AC
*.PRINT AC VM(1) VP(1)
*****************************************************************

**** 2W IMPEDANCE EVALUATION ***********************************
*X1 1 2 SLIC
```

```
*RL 1 0 600
*RG 0 2 10MEG
*I2W 0 2 AC
*.PRINT AC VM(2) VP(2)
**********************************************************************

**** SINGLE TX GAIN EVALUATION ***********************************
*X1 1 2 SLIC
*VL 1 0 AC
*R2W 2 0 600
*.PRINT AC VM(2) VP(2)
**********************************************************************

**** SINGLE RX GAIN EVALUATION ***********************************
*X1 1 2 SLIC
*RL 1 0 600
*V2W 2 0 AC
*.PRINT AC VM(1) VP(1)
**********************************************************************

**********************************************************************
*                                                                    *
* ANALYSIS ON TWO SLIC CONNECTED TOGETHER AT THE 2W TERMINATION      *
*                                                                    *
**********************************************************************

**** INPUT IMPEDANCE EVALUATION **********************************
*X1 1 2 SLIC
*X2 3 2 SLIC
*R2W 2 0 10MEG
*IL 0 1 AC
*RL 3 0 600
*.PRINT AC VM(1) VP(1)
**********************************************************************

**** TX GAIN EVALUATION ******************************************
*X1 1 2 SLIC
*X2 3 2 SLIC
*R2W 2 0 10MEG
*VL 1 0 AC
*RL 3 0 600
*.PRINT AC VM(2) VP(2)
**********************************************************************

**** OVERALL GAIN EVALUATION *************************************
*X1 1 2 SLIC
*X2 3 2 SLIC
*R2W 2 0 10MEG
*VL 1 0 AC
*RL 3 0 600
*.PRINT AC VM(3) VP(3)
**********************************************************************

.END
```

SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE

SLICs PROTECTION CIRCUITS

By W. Rossi ; A. Pariani

INDEX

1. INTRODUCTION.

In this technical note are described different ways to protect L3000/L30XX and TDB7722/7711 SLIC KITs.

The L3000/L30XX are the more complex to protect because the positive battery can be either GND or VB+ (typ. + 72V) depending on the SLIC operating mode. In the following the first three protection solutions refers to L3000/L30XX KITs and the last one to TDB7722/7711.

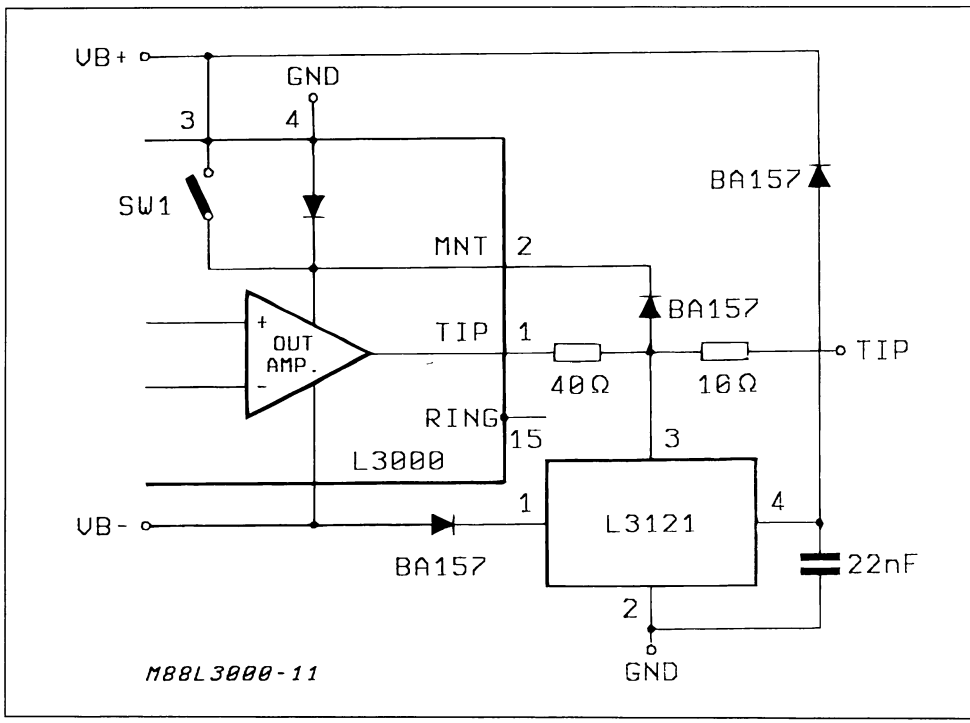
The first solution in based on programmable transient suppressor L3121; and this is the most complete one: another simpler solution, based on standard transient suppressor like LS5120 or TRISIL is proposed. In addition a way to use only one transient suppressor for more subscribers is described. Finally a protection circuit for TDB7722/7711 SLIC KIT is proposed.

2. L3000/L30XX PROTECTION CIRCUIT BASED ON PROGRAMMABLE TRANSIENT SUPPRESSOR L3121.

In fig. 2.1. you can see the circuit configuration used to protect the L3000/L30XX SLIC KITs with L3121. (The same structure is applied to the RING termination). When the voltage on the line increase above VB+ (typ +72V) or decrease below VB (typ. -48V) the transient suppressor L3121 intervenes and shorts the wire to ground.

For each wire we need one L3121 ; one 22nF capacitor to increase the intervention speed and three diodes : two to program the intervention voltage levels and one to pull up the supply voltage of the internal stages in order to avoid reverse voltage between line termination and supply voltage. In fact if you look at fig. 2.1. you can see that the internal output stage of the device can be fed either by GND or by VB+ depending on the status of the internal switch SW1. Since in normal operation the circuit is fed by GND and the protection intervenes when the line voltage exceeds VB+ it is evident that the reverse voltage between line termination and supply can damage the device. To avoid this fact a diode connected between line and supply increases the supply voltage when the line voltage increases (see fig.2.1.).

Figure 2.1 : Protection Circuit for L3000 (half section).



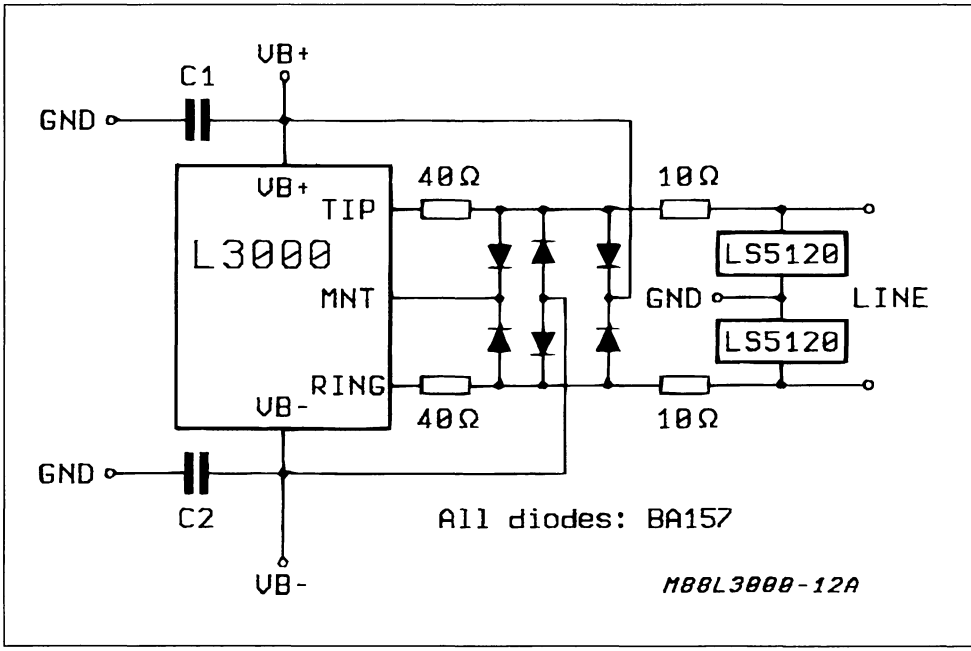
3. L3000/L30XX PROTECTION CIRCUIT BASED ON STANDARD TRANSIENT SUPPRESSOR AS L5120 OR TRISIL.

In this paragraph is described a cheaper solution (respect to the one described in par. 2) to protect L3000/L30XX SLIC KITs.

The protection circuit is based on two LS5120 or TRISIL, a polarity guard and two diodes to avoid reverse voltages between line termination and internal stages supply (see par. 2). The two external 50ohm resistors are splitted in two parts.

The circuit diagram follows :

Figure 3.1 : L3000 Surge Protection Circuit Based on LS5120.



If a surge is induced on the line the LS5120 intervenes and within 100ns it clamps the surge. During the first 100ns the LS5120 works like a 180V Zener Diode. The polarity guard avoid this 180V pulse to reach SLIC line terminations shorting it to the supply voltage (see fig. 3.1.).

Two capacitors C1 and C2 guarantee that in presence of negative or positive surges the supply vol-tage remain constant enough. These capacitors can be easily dimensioned considering that the 100ns current peak flowing through the polarity guard is equal to about 110V/10Ω = 11A in the case of positive surges and about 130V/10Ω = 13A in the case of negative ones.

For negative surges (worst case) the charge Q injected in the capacitor is 13A x 100ns=1.3μC (supposing that no current flows through the power supply) therefore a 1μF capacitor is large enough to guarantee a less than 1.5V supply variation.

If instead of LS5120 another similar device is used the capacitors C1 and C2 have to be dimensioned depending on the clamping time of such device.

It should be noted that the diode type used in the polarity guard is important in order to guarantee good performances. The suggested diodes for this application are BA157. We observe that this kind of diodes in presence of a 10A, 200ns current pulse show a voltage drop of about 3V, while diodes as 1N4004 in presence of the same pulse shows a voltage drop ten times larger (30V).

4. L3000/L30XX COMMON PROTECTION CIRCUIT FOR MORE SUBSCRIBERS BASED ON PROGRAMMABLE TRANSIENT SUPPRESSOR L3100.

In this solution each SLIC is protected by means of a polarity guard that, in case of a surge, avoid the line terminations to exceed the supply voltages. In the following page you can see the circuit schematic of this solution.

Consider that in this application the current peak flowing through the polarity guard can reach 100A for 3KV surges ; therefore proper diodes must be used in order to avoid excessive voltage drop in presence of such current peak.

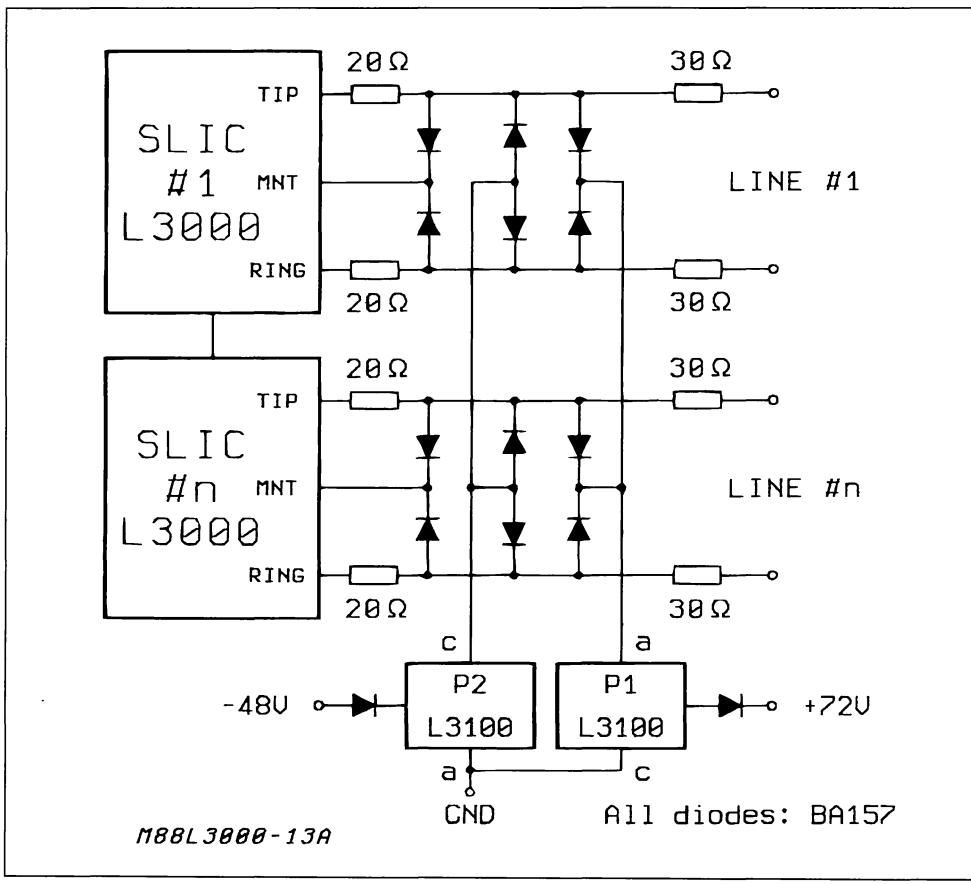
When a positive (negative) surge occurs on one line the common protection P1 (P2) clamps all the lines to ground.

Since when you short a line termination to ground the SLIC can source or sink (depending on the line termination status) up to 100mA, it can happens that once finished the surge the protection remain clamped because of the line currents.

If this fact happens all the SLICs connected to the same protection detect ground key, in this way the controller can recognize that one protection is clamped.

One possible way to open clamped protection (once the surge is finished) is to set all the SLICs connected to it in power down mode for a short time. In this way for a moment no current flow through protection allowing it to open.

Figure 4.1 : L3000 Common Protection Circuit .



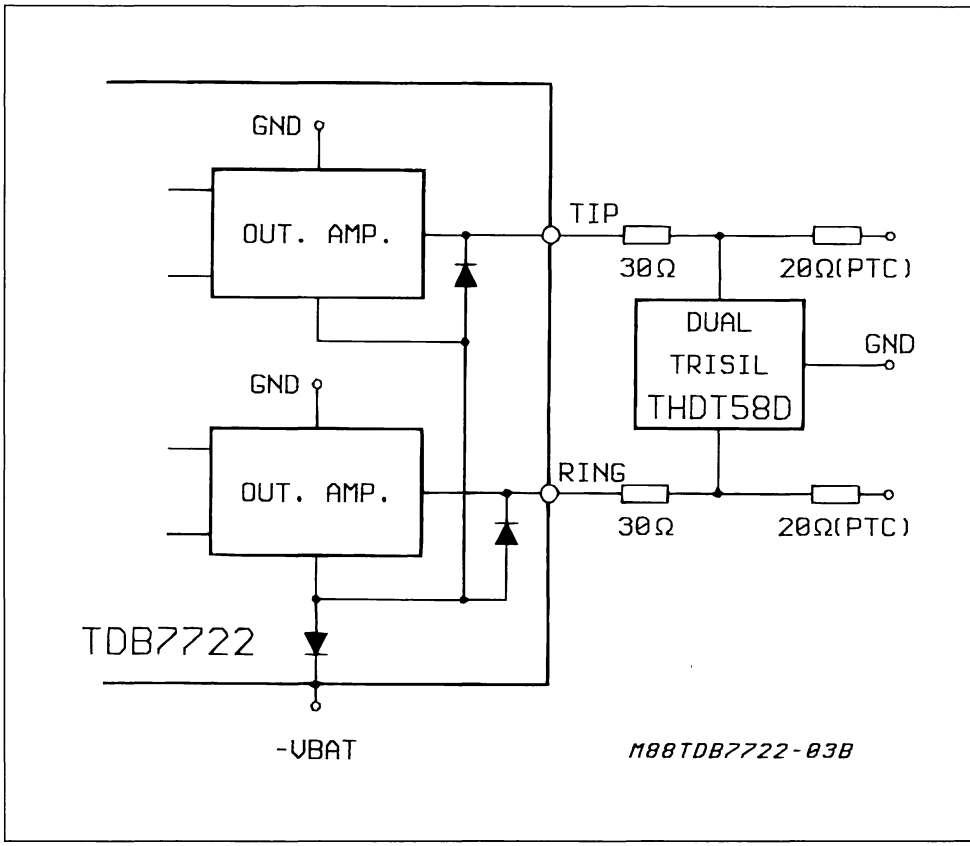
5. TDB7722/7711 PROTECTION CIRCUIT BASED ON DUAL TRISIL (THDT58D).

The fixed operating battery voltage (GND ; -VBAT) and the internal structure of the device allow to use a quite simple circuit to protect the TDB7722/7711 SLIC KIT against overvoltages induced on the line (see fig. 5.1.).

Positive surges on the line are clamped to GND by the DUAL TRISIL. In case of negative surges the TRISIL works for a short time (hundreds of nanoseconds) as a -72V zener diode before clamping the overvoltage to GND.

Since such voltage peak is usually lower than the negative battery voltage (typ. -48V), by means of internal diodes the negative supply voltage for the device is automatically switched to the most negative between battery and line voltage in order to avoid damage to the device.

Figure 5.1 : Protection Circuit for TDB7722 .



SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE

TDB7711-TDB7722
SUSCRIBER LINE INTERFACE CIRCUIT KIT

TABLE OF CONTENTS

1. HIGH VOLTAGE CIRCUIT DESCRIPTION (TDB7722)

(Refer to diagram of fig. 1)

1.1. VOLTAGE AMPLIFIERS

The input voltage of the circuit V_{IN} is symmetrically amplified by 2 voltage amplifiers, whose transfer functions are :

$$V_{S1} = 20\ V_{IN}\ ;\ V_{S2} = V_{(ref)} - 20\ V_{IN}$$

$V_{(ref)}$ is the filtered battery voltage. The outputs of these amplifiers drive, at very low impedance, the line (tip wire and ring wire).

The symmetry of the two gains is very good to provide high longitudinal balance.

1.2. LONGITUDINAL AND TRANSVERSE CURRENTS SEPARATION

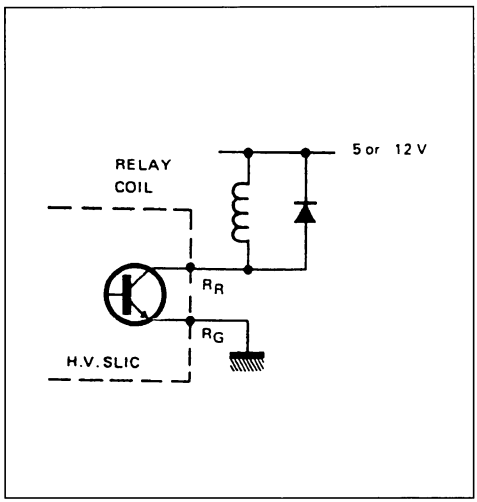
The circuit makes the sum and difference of the two wire currents to provide the transverse and longitudinal components to the LV SLIC (Scaled down : 1/100).

The scaled down transverse current flows by I_T pin.

The scaled down longitudinal current flows by C1 pin.

1.3. OTHER FUNCTIONS (figure page 12 of data sheet)

1.3.1. RING RELAY DRIVER. A transistor, used as a switch, can drive a 5V or 12V relay.



1.3.2. THERMAL WARNING. If the temperature of the IC reaches 150'C a thermal shut down sets the circuit in "HIGH IMPEDANCE" mode and warns the LV SLIC by modifying ILT current (via C2 pin).

1.3.3. STAND-BY. In standby mode, most of the functions are shut down.

Line voltage is set at about $|VB| - 10V$

The currents of the 2 wires are sensed, and the scaled down transverse current is provided to low voltage SLIC TDB7711 for off-hook detection.

1.3.4. POWER DOWN. Under software control, via LV SLIC, or when thermal warning is activated, the circuit is set in power down mode.

In this mode, tip and ring outputs are in high impedance status, and most of the functions are shut down. No line current is provided.

1.3.5. DEVICE CONTROL. The LV circuit controls HV circuit, via C1 and C2 pins, thanks to three different voltage levels.

The HV circuit provides longitudinal current and thermal warning current via the same pins.

The controls are described page 14 of data sheet.

1.3.6. SCALED DOWN BATTERY VOLTAGE. An output provides the LV SLIC with a $V_{(ref)}/40$ voltage ($V_{(ref)}$ is the filtered battery voltage).

This pin is V_{BIM}.

1.3.7. REFERENCE VOLTAGE $V_{(ref)}$. It is the filtered battery voltage. Its value is :

$$[\ |VB| - 2.1V\ ]$$

2. LOW VOLTAGE CIRCUIT DESCRIPTION (TDB7711)

2.1. TRANSMISSION CHARACTERISTICS

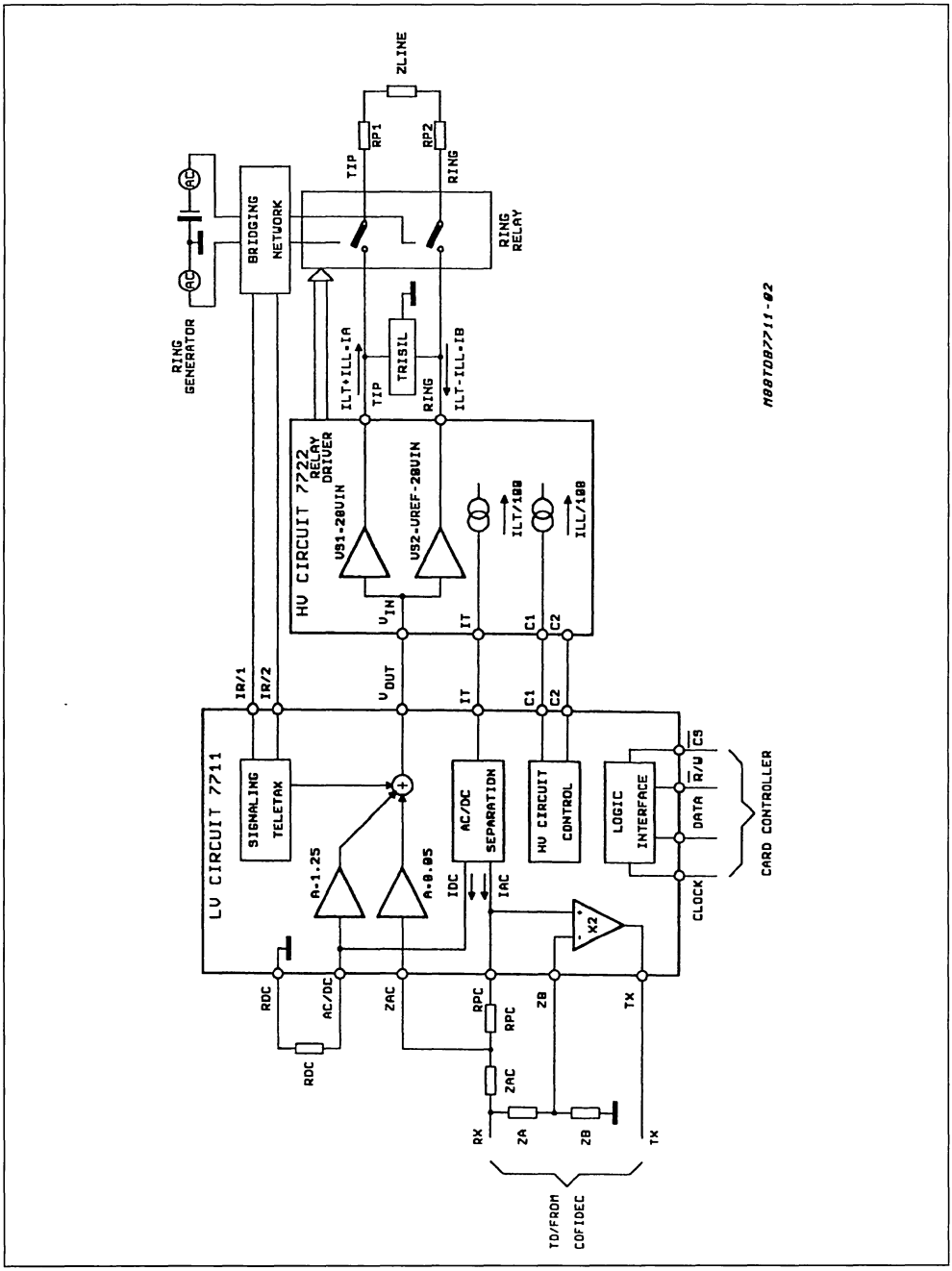
(Refer to diagram of fig. 2)

2.1.1. IMPEDANCE SYNTHESIS AND HYBRID BALANCE. The transverse current provided by the HV SLIC is splitted into DC and AC components. The AC currents flows across C_{AC} (C_{AC} pin is a virtual ground) and the DC component across R_{DC}.

The – 2.7V voltage on C_{AC} allows for the use of a polarized low voltage capacitor.

IAC current flows through ZAC, and gives a voltage divided by 20 (or – 20 in reverse battery) before driving the HV circuit input. This feedback gives the output impedance of the SLIC, between tip and ring wires

Figure 1 : Simplified Block Diagram.



C_{BW} capacitor insures the stability of the feedback. C'_{BW} compensates the C_{BW} effect on hybrid balance. Hybrid balance is done by the input circuitry of TX differential amplifier.

EXTERNAL COMPONENTS ARE DEFINED AS FOLLOWS :

If the required SLIC output impedance is Zline, Z_1 value is such that :

$$Z_{AC}//C_{BW} = 50\ (Z_{LINE} - 2\ rp)$$

. Hybrid balance

$Z_B = K^*ZML$ | $Z_A = K^*Zline$ | $RPC = 100rp$

Examples of Output Impedances (with Z_{ML} = Zline)

Z_0	r	Z_2	Z_1	C' BW ($Z_3 = Z_4 = R = 60k$)
600 Ω	30 Ω	3 kΩ	27 kΩ	120 pF
115 nF, 220Ω, 820Ω	30 Ω	3 kΩ	2 nF, RX, 8 kΩ, 41 kΩ, VAC, C8W, 270 pF	47 pF

For example, when K = 100

ZML = termination impedance between TIP and Ring

. Stability capacitor

$$\frac{C_{BW} = 8\ \mu s / |Z_{AC} + R_{PC}|}{C'_{BW} = 8\ \mu s / |Z_A|}$$

* (Can be lightly different, according to the teletax filter).

2.1.2. GAINS. The voltage gain of the LV circuit is 1/20.

Then the total SLIC (LV + HV circuits) voltage gain is 2 (1/20 x 40).

As the SLIC output impedance is Z_{LINE}, the RX ⇒ line gain is unity when $Z_{LINE} = Z_{HL}$.

LINE ⇒ TX GAIN

The TX differential amplifier gain is 2.

Then the voltage gain between the line and the TX output is unity.

2.1.3. BANDWIDTHS.

- Low cut off frequency.

The C_{AC} value gives the low frequency cut off of :

- the return loss. At low frequency, the return loss is :

$$\rho = \sqrt{1 + 4\ R^2_{DC}\ C^2_{AC}\ \omega^2} \# 2\ R_{DC}\ C_{AC}\ \omega$$

- the transhybrid loss (=HYBRID BALANCE). At low frequency, the transhybrid loss is :

$$R_{DC}\ CAC\ \omega$$

Then, the value of the product C_{AC} R_{DC} is defined by the return loss and transhybrid loss performances needed at low frequency.

R_{DC} is defined in "FEEDING CHARACTERISTICS"

Then :

$$(C_{AC})\ min = \frac{(R_{DC}\ C_{AC})\ min}{R_{DC}}$$

- High cut off frequency

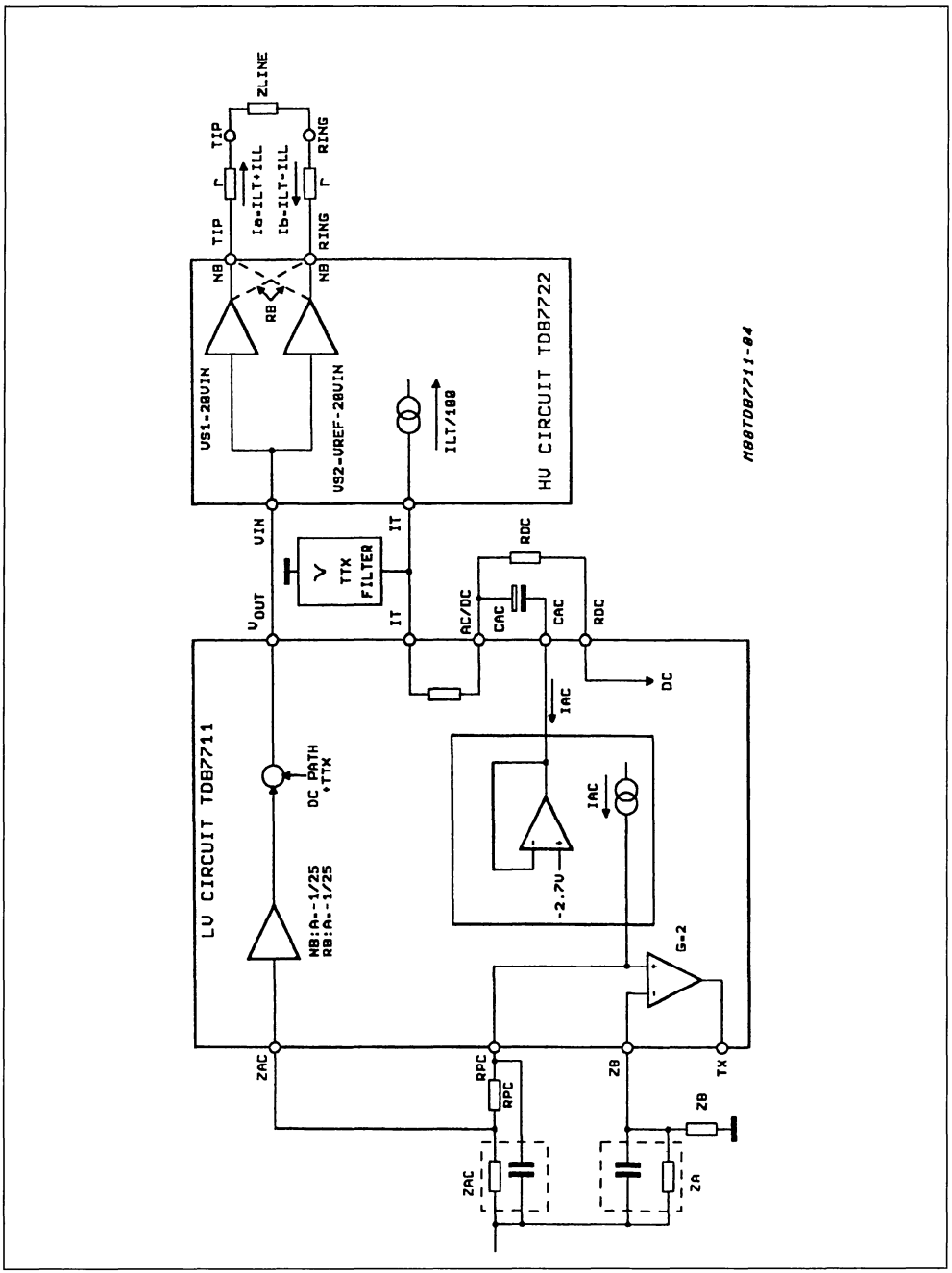
This frequency is given by the stabilization capacitor C_{BW} (see 2.1.1.). Its value is 34kHz.

Note : Improving desaturation time of AC path.

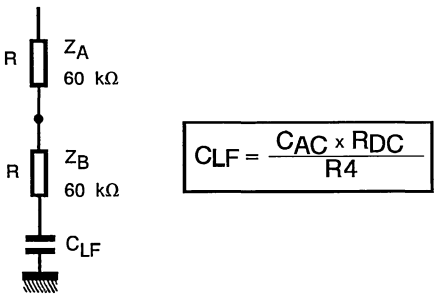
Large DC line current variations may overload the AC path. The recovery time depends on the C_{AC} x R_{DC} time constant.

This time can be lowered by decreasing the C_{AC} value.

Figure 2 : Functional Diagram (AC path).



In this case, in order to keep a good hybrid rejection at low frequencies, the Z_A Z_B network should be modified as follows :



Example : R_{DC} = 850Ω ; C_{AC} = 4.7µF ; Z_B = 60kΩ ; CLF # 68nF.

Desaturation time for IL = 30mA : 10ms.

2.2. FEEDING CHARACTERISTICS

(See diagram page 10 of the data sheet)

The DC component of the transverse current provided by the HV SLIC flows through R_{DC}.

For DC current I_{DC}, R_{DC} presents a virtual ground.

Then the AC/DC pin voltage is $V_{AC/DC} = I_{DC} \times R_{DC}$.

This voltage is amplified (x1, 25), before driving the HV circuit input.

It can be seen that the DC voltage at LV SLIC output is always :

$$V_{DROP}$$

Then, there are 3 possibilities :

- Low line current :

$$|V_{AC/DC}| < V_D \Rightarrow V_{OUT} = -V_D$$

The slic is in waste voltage mode.

- Middle line current :

$$V_{OUT} = V_{AC/DC} = R_{DC} \times I_{DC}$$

The SLIC is in feed resistance mode.

If R_F is the desired feed resistance of the line :

$$R_{DC} = 2 (R_F - 2\,Rp)$$

- Line current = Limitation current :

The voltage on R_{DC} varies quickly when line current is lightly higher than limitation current.

The line current is regulated at the limitation current value.

There are several working modes :

- Apparent battery :
  In this mode, a correcting voltage, depending on the current battery voltage, allows the line to see a dummy – 48V battery ; otherwise, the line "sees" a voltage $V_{(ref)}$ (= current battery voltage – 2.1V).
- Real battery :
  Same as apparent battery except for the standard resistive mode where the voltage value is
  $$|V_{LINE}| = |V_{REF}| - R_{feed} \times I_{LINE}$$
- Special DC characteristics :
  A low value R_{DC} resistance is simulated to have a rectangular feeding characteristic.
- Reverse battery :
  In this mode, the DC current is inverted. Then, the phase of the 1.25 gain amplifier is also inverted, to insure stability of the feedback.

2.3. SIGNALLING (see pages 10 and 12 of data sheet)

2.3.1. OFF-HOOK THRESHOLD AND RESPONSE TIME (SLOW LOOP DETECTION). In stand-by mode, the line is fed in "normal battery" (non-reserved). The off-hook threshold is 6.5 ± 1.5mA.

The hysteresis is 1mA. The response time for a given current I_{LTO} is :

$$t = (R_{DC} + 1\ k\Omega) \cdot C_{AC} \cdot LOG \left[1 \frac{6.5}{I_{LTO}\ (mA)}\right]$$

(because, in standby, R_{DC}^2 is no longer a virtual ground).

2.3.2. ROTARY DIAL PULSES DETECTION (QUICK LOOP DETECTION). In power up mode, the loop detection is quick : <1ms.

The threshold is the same as in power down mode :

$$6.5mA \pm 1.5mA$$

The hysteresis is 1mA also.

2.3.3. TELETAX (TTX)

- Gain

The gain between TTX input (on LV SLIC), and line output (TIP and RING on HV SLIC) is 18dB ± 1dB.

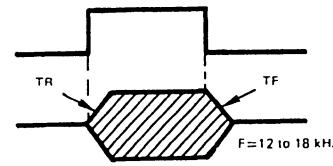
The line level depends on PTC (or protection resistance) value and line impedance at TTX frequency (Z_{LTTX}).

The level of the sinus signal to set at TTX input, for a given line level V_{LTTX} is :

$$V_{TTX} = VLTTX \left(\frac{Z_{LTTX} + 2r}{Z_{LTTX}} \right) \frac{1}{8}$$

Software control : $\frac{1}{0}$

Line signal.



The shaping is done by sending a ± 80µA current in the capacitor C_{RT}, whose voltage varies from – 2V to + 2V (or from + 2V to – 2V).

Then :

$$T_R = T_F = \frac{C_{RT} \times 4}{80} \; 10^6$$

i.e. : 10ms for C_{RT} = .22µF

- TTX filter

An external TTX filter allows the SLIC to have a low output impedance at TTX frequency, and a low leakage level at TX output.

This filter must have a low impedance (compared to 1kΩ at TTX frequency, and a high impedance in speech band (in order to avoid transmission performances degradation).

If Z_F is the filter impedance at the telefax frequency F_{TTX} :

- output SLIC impedance at F_{TTX} :

$$(Z_{T\text{-}R})_{TTX} \# Z_{T\text{-}R} \cdot \frac{Z_F}{Z_F + 1k\Omega}$$

With $Z_{T\text{-}R}$ = Speech band output impedance :

- TX level at F_{TTX} :

$$V_{TX} \# \frac{V_{LTTX}}{Z_{LTTX} + 2r} \cdot Z_{T\text{-}R} \cdot \frac{Z_F}{Z_F + 1\,k\Omega}$$

- TTX drop voltage

The drop voltage value depends on the TTX drop voltage bit (TWV). If TWV = 0, the drop voltage is about 12V (13 max). During sending TTX (TTX BIT = 1) this value becomes 18V.

If TWV = 1, the drop voltage is 18V, whatever the TTX BIT.

- Shaping

The line signal is as follows :

2.3.4. RING TRIP. When ringing, the SLIC must be in normal battery mode.

- Principle

An external circuit applies ringing through the ringing network and the ring relay. This circuit consists of a balanced or unbalanced sinus generator (70 to 100 V_{RMS}) in series with the battery (48V). The line current has, then, an AC component (there is a capacitor in series with the ring circuitry) with or without DC component, according to the hook state. So, the off-hook detection is done by sensing the DC component of the line current.

The following principle is used :

A fraction of the line current is sent into a capacitor (C_{RT}). At time t1, the voltage of this capacitor is set at a given value : V_O.

The voltage of this capacitor is sensed at times :

$t1 + T_R$, $t1 + 2\,T_R$ ..... $t1 + nT_R$. (T_R = ringing period).

If the voltage sensed is V_O, that means there was no DC component in the line current (on hook).

More precisely, the following tasks are made : when the ringing control is operating (software) :

- ring relay is energized at the zero crossing point of the ring generator = time t0,
- C_{RT} voltage is set at – 70mV during one ringing period,
- a scaled down line current is sent (after having substracted a threshold current into C_{RT}.
- at times $t0 + 2T_R$, ... , $t0 + nT_R$, the C_{RT} voltage is sensed :
  - if $V_{CRT} < -70mV$ (i.e. DC line current < I threshold) : V_{CRT} is set t0 – 70mV,
  - if $-70mV < V_{CRT} < 70mV$: V_{CRT} is unmodified,

- if V_{CRT} + 70mV, the off hook is detected : ring relay is desenergized and hook status bit is set on 1 state.
- Ringing network

The following networks are insensitive to longitudinal currents :

Figure 3 : Balanced Ringing.

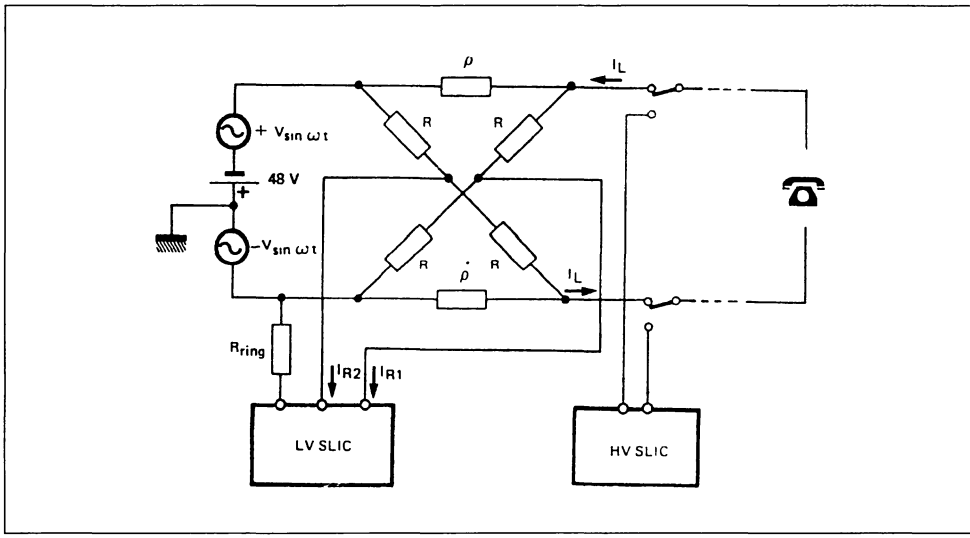
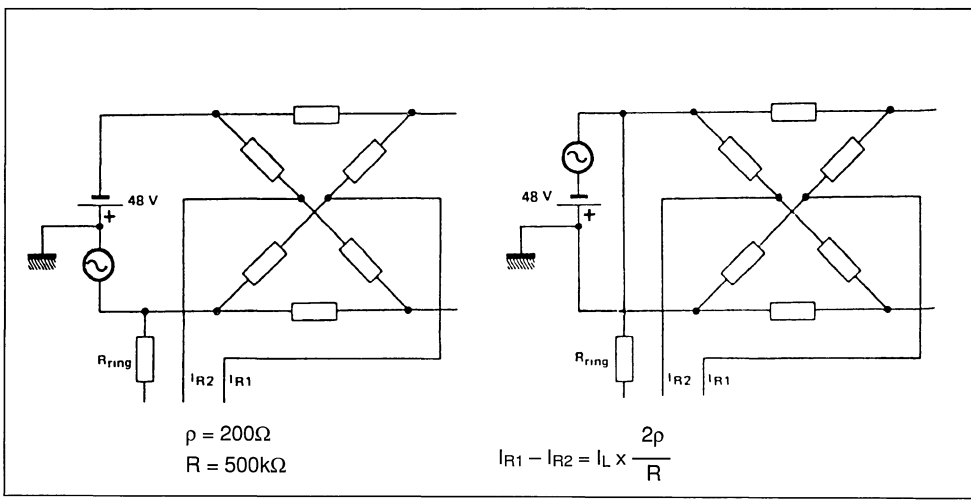


Figure 4 : Unbalanced Ringing.



■ Ring trip threshold and response time

We have seen :

$$I_{R1} - I_{R2} = I_L \times \frac{2\rho}{R}$$

The threshold current on LV SLIC input 6.8µA, i.e. :

$$6.8\mu A \times \frac{R}{2\rho} = 8.5mA$$

on the line with the network above.

The ring trip capacitor should be :

$$C_{RT} = \frac{220nF \times 50Hz}{F_R}$$

$$\left(\frac{1}{T_R} = F_R = \text{ringing frequency}\right)$$

Then, the ring trip response time for a DC loop current I_{LTO} is :

*

*

That's

■ $I_{R/1}$ and $I_{R/2}$ inputs compliance
The compliances of these inputs are : > + 350µA & < – 500µA.
These compliances allow, with the ringing network above, the use of balanced or unbalanced ringing with the limits :

$$-72V < V_{B-} < -20V$$

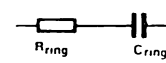
$$V_{ring} < 88\ V_{RMS}$$

If other values are needed, the equations above allow to find the values of ρ and R.

■ Bridging network accuracy
According to the desired ring trip accuracy, it is possible to find the resistors ratio accuracy, using the equations above. For example, a 1% ratio accuracy induces a 3mA accuracy in the threshold current (for $V_{B-} = 60V$).

■ R_{ring} value
It depends on the ringing generator level. The LV circuit requires a 70µArms minimum current.

■ Ring relay response time (tRR)
This time can be compensated by adding a capacitor in series with R_{ring} :



$$C_{ring} = \frac{t_g\,[90° - 360°\,t_{RR}\,F_R]}{2\,\pi\,F_R\,R_{ring}}$$

2.3.5. GROUND KEY. The HV SLIC provides a scaled down $(\frac{1}{100})$ line longitudinal current.

A threshold current is substracted from this current, in the LV SLIC and the differential current is sent, after dividing $(\frac{1}{9})$ to the ring trip capacitor C_{RT} (except when ringing or sending teletax). Then, if the DC component of the longitudinal line current is lower than the threshold current, the C_{RT} voltage is lower than a threshold voltage (+ 2V). Otherwise, ground key is detected.

The treshold longitudinal current is 50µA (i.e. 5mA on each wire, ring and trip).

The response time, for a line current I_{LLO} (each wire) is :

$$T = \frac{4 \times C_{RT}}{\frac{1}{9}\left[\frac{I_{LLO}}{100} - 50\,10^6\right]}$$

Example : $I_{LLO} = 10mA$, $C_{RT} = 0.22\mu F \Rightarrow r = 160ms$.

2.4. ANALOG INPUT - OUTPUT PIN

This pin is programmed by soft as an input or an output.

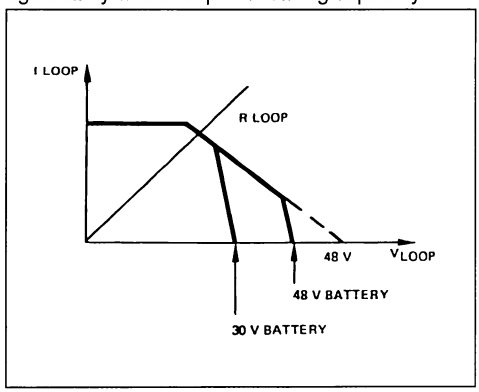
■ As an input

An external voltage $\frac{V_{EXT}}{40}$ is set on the pin.

The SLIC compares V_{EXT} voltage and the DC line voltage.

If : $V_{LINE} > V_{EXT} \Rightarrow C_{RB} = 0$
$V_{LINE} < V_{EXT} \Rightarrow C_{RB} = 1$

This can be used to feed the SLIC with a low voltage battery and offer power saving capability.



- As an output

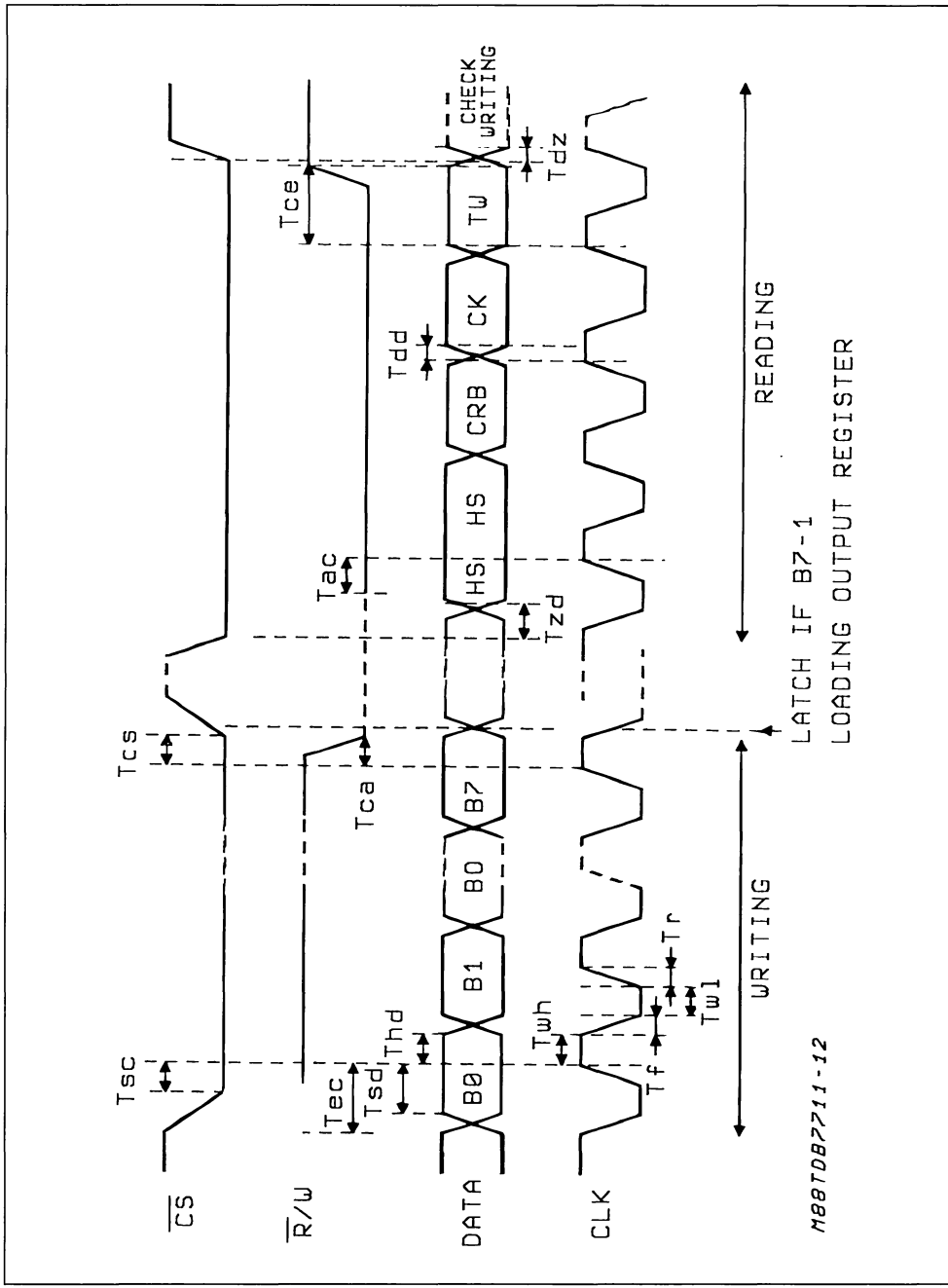
The voltage of this pin is 1/40 the DC line voltage.

This can be used to detect line short circuits.

2.5. DIGITAL CONTROL INTERFACE

The programmable functions of the SLIC are set by the contents of two 8-bit registers in the TDB7711, LV chip. This circuit communicates with the card controller through a 4-wire serial bus. The interface is described pages 17 and 18 of the data sheet.

Figure 5 : Timing Diagram.



3. OVERVOLTAGE PROTECTIONS

The HV circuit is protected against overvoltages with a pair of PTC or fuse resistors (matched to meet longitudinal requirements), plus a dual trisil with integrated diode.

Figure 6 : Protection Circuits.

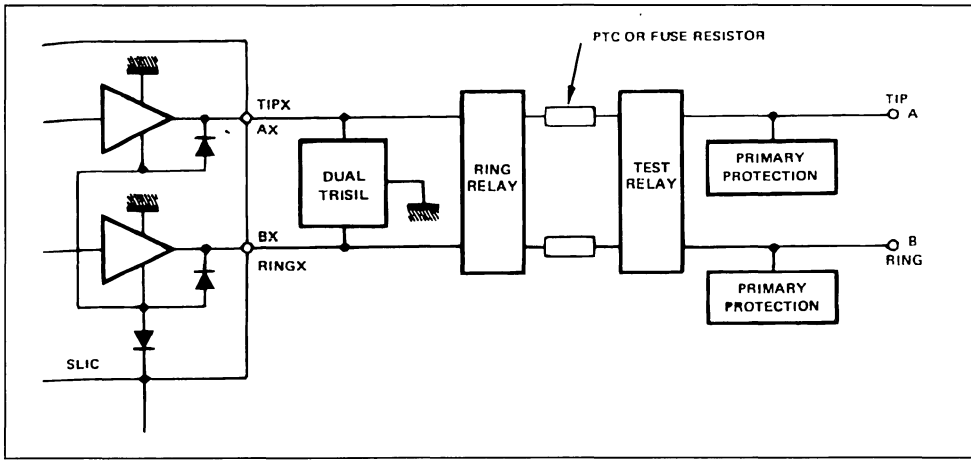
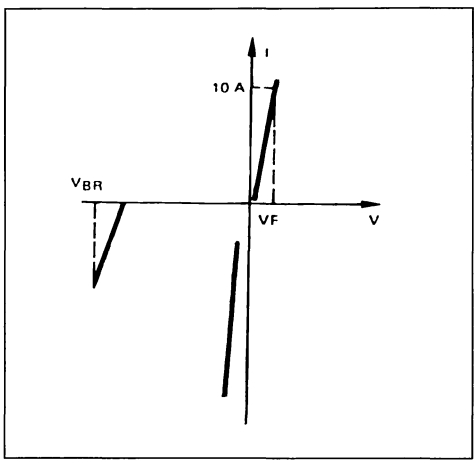


Figure 7 : Trisil Characteristics

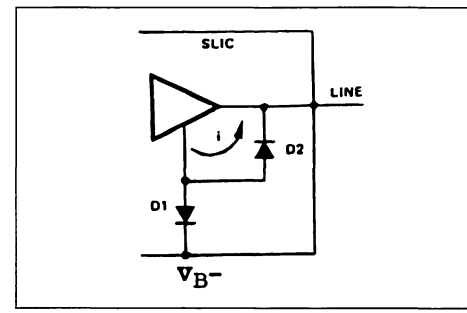


The trisil diode insures line voltage :
< 3V for positive voltage.
< | V_{BR} | for negative voltage.

On surges, negative voltages on trisil falls to a low value, (a couple of volts) keeping it in safety area.

- Behaviour of the high voltage SLIC when lightning surges
  - Positive surges < + 3V
    Current in wires are limited by the SLIC itself (– 150mA).

Negative surges
The voltage on the line can be more negative than the battery voltage.



In this case, diodes D1 and D2 act as if the supply voltage of the SLIC was – Vsurge instead of – V_{b-}

Then, we must have :

| V_{surge} | < 72V

(i.e. : maximum battery voltage allowed)

| VBR | < 72V

Note : Diodes D1 and D2 are integrated on the chip.

SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE

HOW TO HANDLE SIGNALING WITH THE M088 DIGITAL SWITCHING MATRIX

by Angelo Pariani - Francesco Natali

INTRODUCTION

One of the main problems in the design of electronic systems, and in particular in the design of private electronic switches (PABX : Private Automatic Branch Exchange) is to make an architectural choice between a system that is expandable and flexible, and another one that is optimized in terms of hardware and software, but more rigid because it is dedicated to a specific application.

The architectural section that is more influenced by such an initial choice is that related to the "transfer and handling of signaling messages", in order words all circuits and procedures which allow the request of single users to communicate to the mainframe computer and, in a reverse process, to communicate to the single user the decisions taken by the computer.

The diagram in figure 1 shows a typical digital exchange. The users are either analog (traditional telephones) or digital ISDN terminals (Integrated Service Digital Network). The main difference between the signaling messages of analog users and those of digital users is that the first are generated and activated through the resident circuits on the exchange (user board) and have for end points the mainframe and the user board, while the second are generated in the user terminal and the dialogue occurs mainly between the mainframe and the ISDN terminal.

In this technical note we will give a detailed description of an original and very advantageous solution to the problem of transfer and handling of signaling messages in analog user systems.

The architectural choice, on which the proposal is based, is in favor of an optimized system in terms of hardware/software and is limited to a maximum of 180 users.

The basic idea can however be applied to the development of systems with a large number of users as mentioned at the end of this note.

TRADITIONAL SOLUTIONS

Various architectural solutions are implemented today in the handling of signaling messages and we will briefly analyse only two of them. The first solution is chosen between simple ones and the second between more complex and sophisticated ones.

In figure 2a block diagram shows a typical system in which the signaling messages are handled by various microprocessors through parallel buses for data and addresses.

Each microprocessor, which we identify with the name "peripheral µP", is placed an a "peripheral control card" and from one side it interfaces with a "central µP" while on the other side it carries on the conversation with a number of user boards through a data bus and an address bus. Each user board, which we suppose analog (subscriber card), is linked to a maximum of 16 telephones through two-wire transmission lines (telephonic pairs).

We consider the example of 4 boards, each of which refers to 16 users. The peripheral µP handles them with an address technique through a data bus and an address bus linked to each board.

A possible allocation of the wires of the buses is as follows :

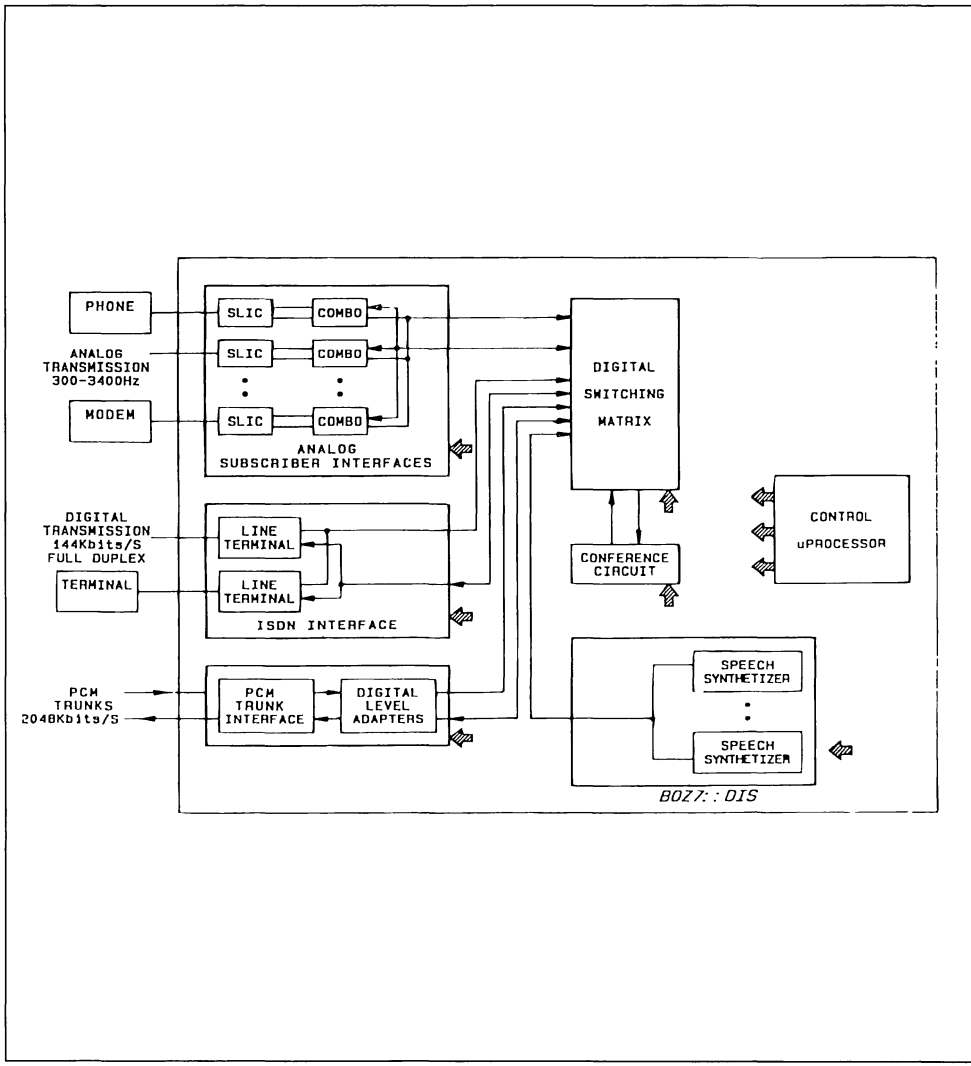
- 2 wires of the address bus will be sufficient to select the single board ;
- 4 wires of the address bus will select the single subscriber ;
- 1 wire of the address bus will select the kind of operation to execute, i.e. the direction of the flow of data (read/write).

A certain number of wires of the data bus will allow the µP to carry on a dialog with the SLIC (Subscriber Line Interface Circuit) and COMBO (COMBined PCM codec and filter) devices placed on the subscriber board. These devices are respectively used for interfacing with the line and the 2/4 wires conversion and for the analog-to-digital conversion and viceversa of the message.

Appropriate comparison circuits will select the board with which the µP wants to carry on a conversation and will enable the single user circuitry inside the board itself to extract or insert information from and on the data bus.

The peripheral µP is usually able to execute a preprocessing of data received from the user circuits or of data which need to be sent to the user circuits, as, for example, to recognize selected digits in the case of rotary dial pulsing or to generate the timing of the ringing signals.

Figure 1 : A Typical Digital Exchange for Voice an Data Switching.



This solution, simple from the viewpoint of the system, has the advantage of being based on standard components, but at the same time it presents two real and not negligible disadvantages :

1. an additional peripheral control card must be inserted for every 4/8 subscriber cards ;

2. the number of wires to be connected between the control card and the subscriber card becomes rather high and this undermines the system in terms of overloading, reliability and consequently economy.

A surely more "elegant" solution is outlined in figure 3. On each user board or subscriber card there is a board controller known as PCB (Peripheral Board Controller) and it is identified in the diagram by the adjective "slave". The function of this PBC is to interface between the board circuitry which includes the SLIC and COMBO, and another PBC, identified as "master", which is directly managed by the mainframe (central P).

In this case, the signaling is assigned either to a well-defined channel of the TDM (Time Division Multiplexed) highways or to two of the highways dedicated only to the coded signaling according to a HDLC (High level Data Link Control) protocol. This second possibility is shown in figure 3.

The more obvious advantages which can be obtained with such a solution can be identified as :

a. reduction to two wires for signaling messages transfer (protocol HDLC) ;

b. no need for intermediate control board ;

c. well coded interface and consequently facility of expansion of the system itself.

On the other hand, the following evaluations cannot be ignored :

1. the solution is rather costly as it requires a PBC controller for each 8/16 users ;

2. many of COMBOs that are available on the market cannot interface directly with the PCM board controller.

NEW SOLUTION TO THE PROBLEM OF "HOW TO HANDLE THE SIGNALING"

The proposed solution tries to combine the positive factors associated with the system architectures described above :

1. auxiliary wires are not needed to transfer the signaling ;

2. the solution uses standard Ps and does not require dedicated components ;

3. it does not use architectures with intermediate control boards.

The idea that resolves the problem is based on the use of an auxiliary function provided by the Digital Switching Matrix (DSM) M088, the function 6 which permits the "fast extraction of 0 channels of the PCM input highways.

HOW TO HANDLE SIGNALING WITH THE M088 DSM

The M088 Digital Switching Matrix (DSM) (see appendix A "Main Characteristics of the M088 DSM" and "Functions of the M088 DSM"), beside the main switching operation in a non-blocking way of up to 256 channels and beside instructions pertaining to switching (disconnection, read/write on a channel of a PCM word, acquisition of the connection map), offers an auxiliary and particular function : the fast acquisition of 0 channels found on the 8 PCM inputs, function described in details in appendix B "The M088 function 6 : fast extraction from channels 0".

Once activated function 6, the M088 under control of an 8 bit microprocessor working with a 4 MHz clock, can perform the following operations during the time internal of one PCM frame (125 sec) :

a. extract the content of channels 0 of the 8 PCM input streams if the two most significant bits of the byte of channel 0 are not equal to "01" ;

b. provide them to the microprocessor through its internal registers ;

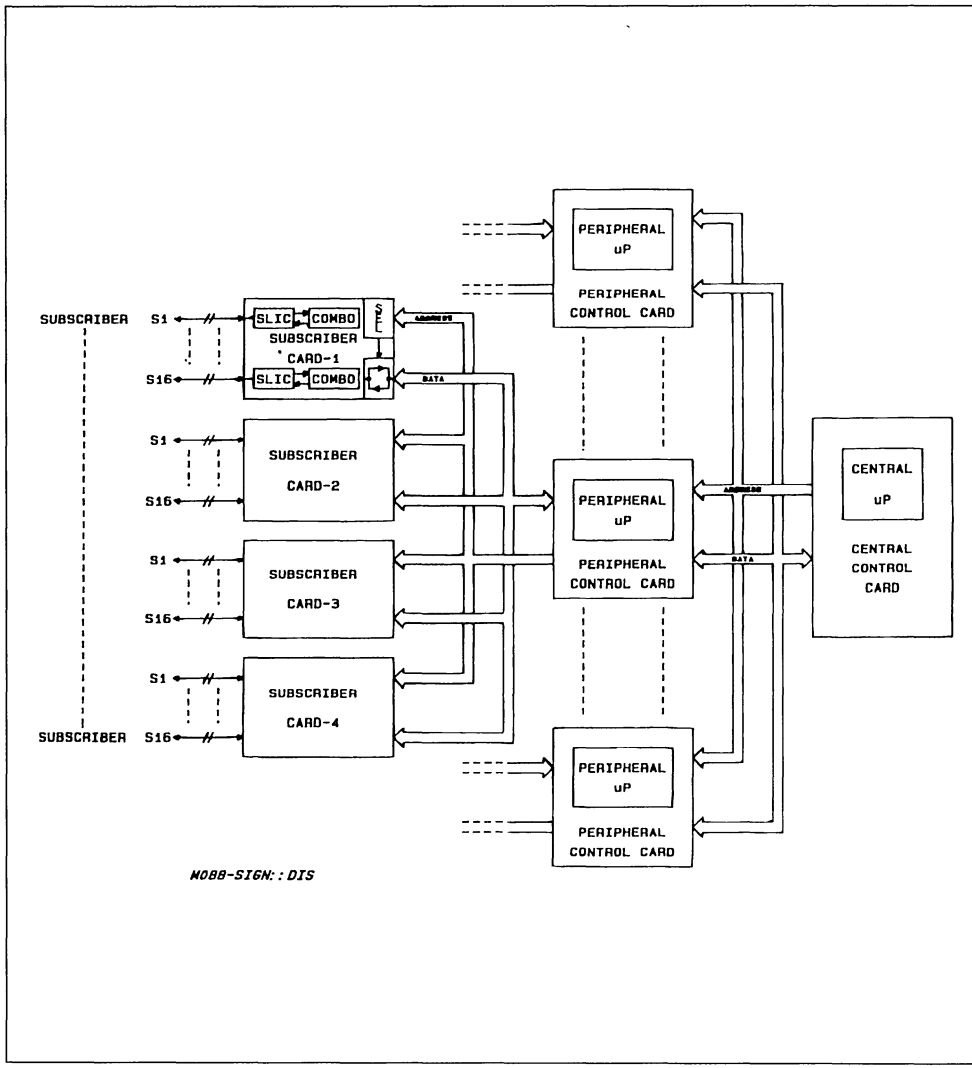
c. execute at least one more function among those available by the DSM, for example : the connecting function or the loading of a PCM byte on whatever output channel and in particular on the channels 0 of the output PCM streams.

M088 possibilities pointed out here together with the option of using channel 0 to transfer the "signaling" lead to the idea of using the DSM M088 not only as a switch "actuator" but also as device for the "handling of the signaling" i.e. for the extraction of the same from the PCM input streams and the insertion of the new signaling informations into the output PCM streams. The idea is more attractive in that the handling of the signaling is generally executed by circuits designed ad hoc, as described above.In brief, the M088 represents an ideal device capable of carrying on the multiple functions required in a modern switching system, functions all executed under the control of a standard microprocessor.

He will illustrate thereafter a system which, using a single M088 DSM, can manage the transfer of the signaling messages between the central processing "heart" of the system and the peripheral devices represented by the subscriber cards with up to 180 lines.

For systems of larger switching capacity, please refer to the paragraph on "How to Handle Signaling in Large Switching Systems" at the end of this note.

Figure 2 : Architectural Solution to Handle Signaling Messages Using Peripheral Control Cards.



SYSTEM ARCHITECTURE AND RELATING PROCEDURES

To illustrate the architecture of the new system we specify two main sections : the peripheral equipment represented by the subscriber cards and the main section relating to switching and processing.
As shown in figure 4a, the peripheral architecture, of the system consists of a subscriber card physically connected to two PCM buses of the DSM, one for the data flow from the card to the switching section and the other for the flow in the opposite direction, and this is valid for six subscriber cards. In fact, of the 8 PCM highways available in each direction, 6 are used to communicate with the subscriber cards while the remaining 2 are kept for other functions relative to the switching section (Conference and Tone Generation).
Each card manages 30 users, each of which being assigned to a pair of SLIC-COMBO. Each of these pairs, through a simple digital circuit, will insert or extract its digitized message into or from one of the 30 channels of the PCM stream reserved for such function (voice channels). The remaining 2 channels and specifically the channel 0 and the channel 15 are respectively reserved to contain the signaling and to transfer the maintenance signals (test, control, etc).

At user card level, the logic of extracting and adding the switching informations representing the signaling from or into the 0 channels of each PCM frame is very simple, because the single pair of PCM streams from and for the DSM is rigorously assigned to a well identified user board. Each of the 30 users of the card, once every 30 temporal intervals, each of the time duration of a frame (125 μs), uses the channel 0 to insert or extract its own signaling, apart from having reserved for each frame the channel needed to insert or extract the coded voice.

Regarding the section for the managing and executing of the switching function, the system architecture can be represented as in figure 4b. The interaction between the various blocks and the necessity for the existence of the same blocks are easy to understand, analysing the procedures that must be put into action for the handling, the processing, and the executing of the signaling in the channels 0 of the PCM streams.

- the DSM activated by the microcomputer to handle function 6 extracts the bytes from the channels 0 and makes them available in its own OR1 internal registers.
- he microcomputer μP1 (for example Z80), which we will refer to as "extractor/actuator μP", reads the data of the DSM channels 0 and stores them into the RAM FIFO 1 only when the DSM requests an interruption to signal the presence of available data.
- the high processing capacity microcomputer μP2 (for example Z8000), which we will refer to as "processor μP", takes this data already stacked up by the μP1, processes the information and as a result generates other data which are stacked up in the RAM FIFO 2.

the microcomputer μP1 extracts the data from this second FIFO and generates appropriate commands towards the DSM (connections, disconnections, loading into the channels 0 or into other channels), or towards other circuits such as CC (Conference Circuit) and TG (circuit for the Generation of Tones), executing in such a way the functions requested by the previously extracted signaling.

The existence of two μPs, as will appear more clearly below, is related to the necessity of accomplishing concurrently more types of operations as above described. This is possible only if the tasks are appropriately distributed between the two processors, which must transfer the data to each other through common storage areas, the two RAM FIFOs and using these also as buffer memories they can operate at different speeds.

PROTOCOL OF COMMUNICATION BETWEEN THE TWO PROCESSORS

The architectural structure proposed for the realization of the system does not introduce specific limitations to the protocol used to synchronize the operations of the two processors.

In any case, it is appropriate to point out that :

a. after having activated functions 6, the MDC can extract, for a duration of 125 μs, all 0 channels from the 8 PCM input streams and execute at least one of the other functions.

b. the microprocessor μP1, interfaced with the DSM, in acquiring this data from the internal registers of the DSM, must respect the minimum temporal intervals between subsequent read operations (see appendix B) : therefore, there are no advantages, in terms of time saving during the read phases, either in using microprocessors more complex than the standard 8-bit ones (i.e. Z80) or in using clock frequences higher than 4 MHz.

c. the DSM selects all channels 0 with most significant bits not equal to "01". Channels 0 containing bytes of the 01XXXXXX type will be ignored.

d. it is possible to choose through a byte called "mask byte" which input flows the DSM must respect to extract the channels 0. In our example a mask byte of the 11111100 type will be needed to enable the extraction of the channels 0 of the input PCM streams from PCMIN7 to PCMIN2 (6 enabled streams).

e. the bytes are extracted from the channels 0 in a sequential way, starting from the PCM bus connected to the PCMIN7 input until the PCMIN2 input.

f. the byte extracted from each channel 0 is supplied to the OR1 register of the DSM.

From the point of view of the RAM FIFO 1, that is the memory which stores the data written from the microcomputer µP1 and read to the µP2, it is advisable to insert, at the beginning of each 6 bytes read by the µP1 from the OR1 registers of the DSM, a delimiter byte (FLAG1) which has the function of facilitating the synchronization between the processors. For example, based on the preceeding c. observation, FLAG1 can have the two most significant bits equal to 01 and reserve the other bits to define a multi/frame counter : in this way there would be no possible confusion between such a byte and a single useful data extracted from the channels 0.

If we now move to the RAM FIFO 2, the storage memory of the data written to the µP2 and read from the µP1, we find the data processed by µP2 which represent the bytes for the instructions to be sent from µP1 to the DSM or to other circuits (CC, TG). These bytes must be such as to avoid as many processing operations are possible for the µP1. One of the solutions consists of preceding each block of bytes with data relative to a specific function to be executed by the DSM or by other circuits with one control byte (CNTL), containing indications on the type of function and structured in such a way to activate in the program memory of the µP1 the routines dedicated to the single specific function to be executed. We will also need a separating byte (FLAG2) to allow an easy synchronization between µP1 and µP2 and such FLAG2 can be used as the "head" of a block of useful data.

Figure 5 represents a possible protocol of the communication between the two processors µP1 and µP2 through the two RAM FIFO.

Figure 3 : Architectural Solution to Handle Signaling Messages Using PBC (Peripheral Board Controller).

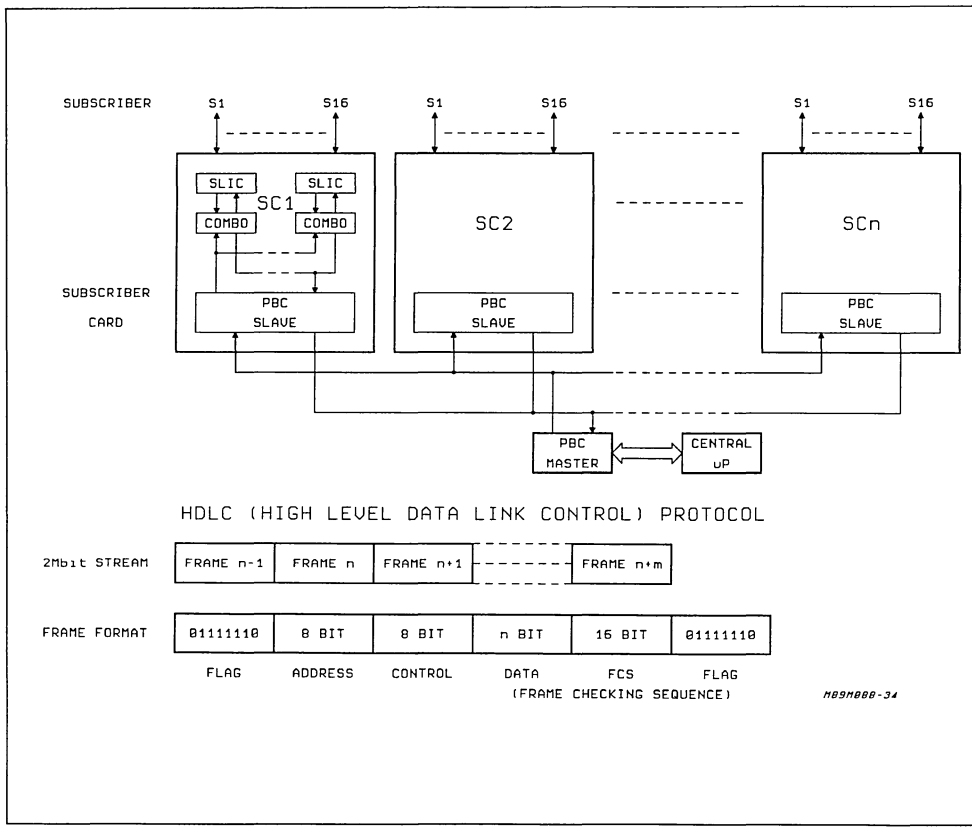


Figure 4a : Subscriber Card of the Proposed Architectural Solution to Handle Signaling Messages.

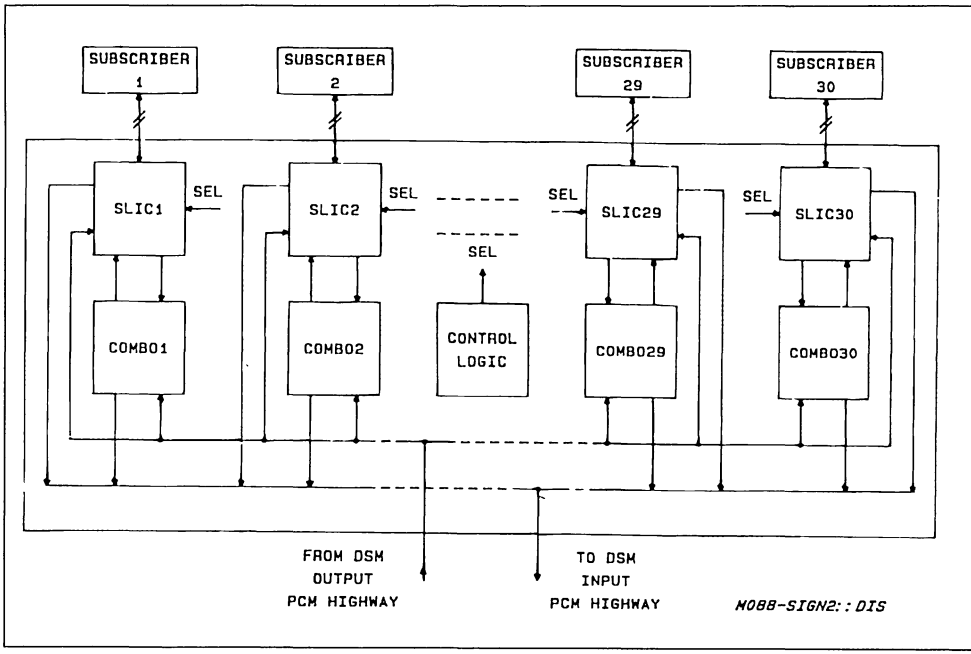


Figure 4b : Switching and Processing Section of the Proposed Architectural Solution to Handle Signaling Messages (max. 180 users).

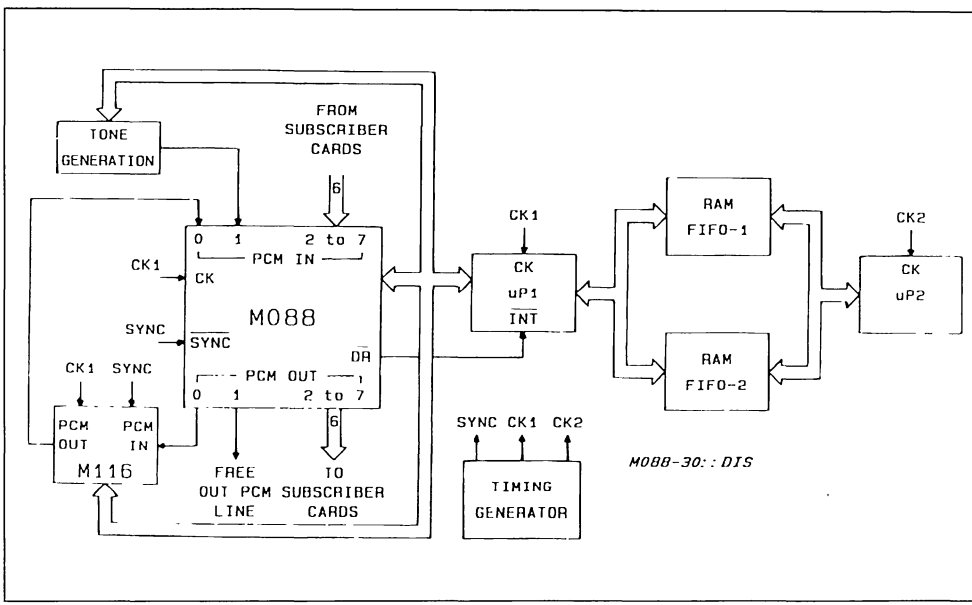
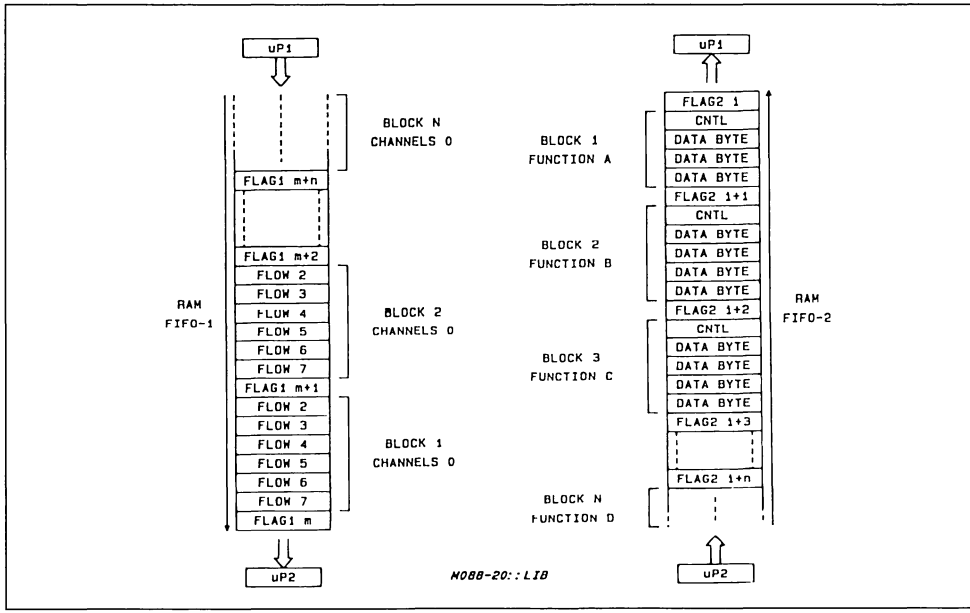


Figure 5 : A Possible Protocol of the Communication between the two Processors through the two RAM-FIFO.



SIGNALING BETWEEN SUBSCRIBER CARD AND SWITCHING AREA

The information sent by the peripheral are (subscriber card) for each single user to the switching area are essentially the following two :

1. line condition (ON HOOK/OFF HOOK)
2. ground key (ON/OFF)

The 8 bits to load into channel 0 could be selected as follows :

	MSB						LSB
CHANNEL 0	D7	D6	D5	D4	D3	D2	D1 D0

D7 = 1. Remember that M088 does not read out bytes beginning with "01".
D6 = line condition.
D5 = ground key.
D4 - D0 = binary number of the user (1 - 30) to which the signaling in D6 and D5 refers.

The user number enables the processor µP2 to know which user is the source of information, while the board identification to which the user belongs can automatically be deduced from the fact that the PCM stream in which the information is loaded is unequivocally assigned to a specific single user board and from the fact that the extractions of the channels 0 of the 6 input streams are orderly and sequential.

Viceversa the 8 bits of channel 0 sent from the DSM to the subscriber card can be assigned as follows :

	MSB						LSB
CHANNEL 0	D7	D6	D5	D4	D3	D2	D1 D0

D7 = used to program an auxiliary function of the COMBO (for example the LOOP function).
D6 - D5 = used to program various operating states of the SLIC-COMBO (i.e. in the case of SLIC L3090 it is possible to choose between the following states : CONVERSATION/RINGING/STAND-BY/POWER-DOWN).
D4 - D0 = binary number of the user (1 - 30) to which the commands present in D7, D6 and D5 refer.

COMMUNICATION PROCEDURE MICRO µP1 - DSM

It has already been described above which operations must be run in the communication between the µP1 microprocessor and the DSM.

We must state that the procedure of reading/storing of the contents of the channels 0 is performed by µP2 only as a routine of response and service to the main program interruption requested by the DSM through the signal on its own output DR indicating the availability of bytes read out from channels 0. The main program of µP1 is dedicated to the sequential flow, towards the DSM and eventually towards the CC

and TG circuits of the commands and the bytes of data necessary for them to execute the functions requested by the subscribers, using the data resulting from the processing of these requests executed by the µP2 processor.

Figure 6 represents a possible block diagram of the main program area which handles the interaction between µP1 and DSM.

We must pay attention to the fact that when the execution of a DSM function is requested, it is considered finished by the DSM only if the µP1 does a reading of the internal OR2 register of the DSM after the instruction opcode has been sent. It is only after this reading has been done that the DSM is reenabled to execute new or pending functions, including function 6.

Reading and storing in RAM FIFO 1 of other data can then be done if there is a need to introduce procedures for controlling the status of the DSM device (using function 4 and function 5) and of the CC device. In such a case the FLAG1, header byte of the blocks memorized by µP1, must contain additional information to tell the µP2 if the following data block is relative to the extraction from channels 0 or if it contains other information and from what device they are read. A possible allocation of the FLAG1 bits can be the following : the two most significant bits equal to 00, the following bit reserved for the identification of the device to which the block of successive bytes refers, the remaining 5 bits used as a counter. One must pay special attention to the control of the interruptions in order to avoid, during the storing of these subsequent data, that an interruption occurs from the DSM as this would create confusion in the RAM-FIFO 1 data.

The FLAG2 byte used to synchronize the communication between µP2 and µP1 which is there to indicate the beginning of a useful datablock to be processed by µP1 will need have a bit configuration such as not to give rise to a wrong identification. One hypothesis is to use a byte equal to 11111111 since the configuration does not exist for any data byte or control byte nor DSM byte or CC byte.

The next CNTL byte can contain in its 4 most significant bits the binary number of the function to be executed (6 DSM functions, 6 CC functions and 4 TG functions), while the other 4 bits can be used for the cyclical numbering of the blocks.

Figure 7 shows the block diagram of the interrupt service routine.

In this routine, special attention is paid to respect the minimum time intervals between two successive readings of the OR1 and OR2 registers of the DSM. For the OR2-OR1 sequence especially an interval of at least 13 CLOCK periods (3.2 µs per CLOCK frequence equal to 4096 KHz) is necessary, while for the OR1-OR2 sequence an interval of 3 CLOCK periods (750 ns) is sufficient.

Note that the only OR1 registers containing bytes extracted from channels 0 are stored.

We would like to point out the fact that the procedures indicated here, relate to a system designed to serve 180 users distributed in 6 user boards. In case this potentiality is not all used, the mask sent by the DSM to activate function 6 must contain a number of "1s" equal to the actual number of user boards connected to the system, and additionally in the interrupt routine a corresponding number of readings of the pairs of registers of the DSM must be done with a consequent increase in the speed of execution of the routine itself.

HOW MUCH TIME IS NEEDED FOR THE µP1 - DSM INTERACTION

The use of a Z80 microprocessor such as P1, at a clock frequency of 4 MHz or at the same frequency as the DSM CLOCK (4.096 MHz) allows, withing a frame (125 µs), to extract the 6 channels 0 and to store in RAM the contents of the OR1 and OR2 DSM registers, to send and to execute a function and a half, like connection (instruction 1 of the DSM) or loading into a channel a PCM word (instruction 3 of the DSM). These are functions that require the highest number of bytes to be sent to the DSM (4 data bytes + 1 control byte).

ABOUT THE SYSTEM TIME RESPONSES

Based on the previous observations, the information relative to each subscriber is transferred to the microprocessor every 30 PCM frame, or within a time interval equal to :

125 µsec. (length of a frame) · 30 (subscribers per board) = 3.75 msec.

This interval is sufficiently reduced to correctly capture the line condition of the user also during the dialing operation.

As for the number of operations which can be executed by the DSM we have verified that this number is equal to :

1.5 (function per frame) · 8000 (frames per second) = 12000 functions per second.

From these considerations we can see that realizing the connections, sending information to the subscriber cards in the channels 0, and executing other auxiliary functions do not present any problem in relation to the time necessary to satisfy the requests of all the subscribers.

Among all the functions that can be executed, here are, as an example, the most significant ones :

- the loading into channel 0 of an appropriate PCM stream of the information necessary to activate the ringing signal of a subscriber to carry out a calling request from another subscriber.
- the connection between two subscribers after the busy signal (OFF-HOOK) has come from the called subscriber.
- the activation of conference call between a specific number of subscribers.

Figure 6 : Main Program Flow-chart.

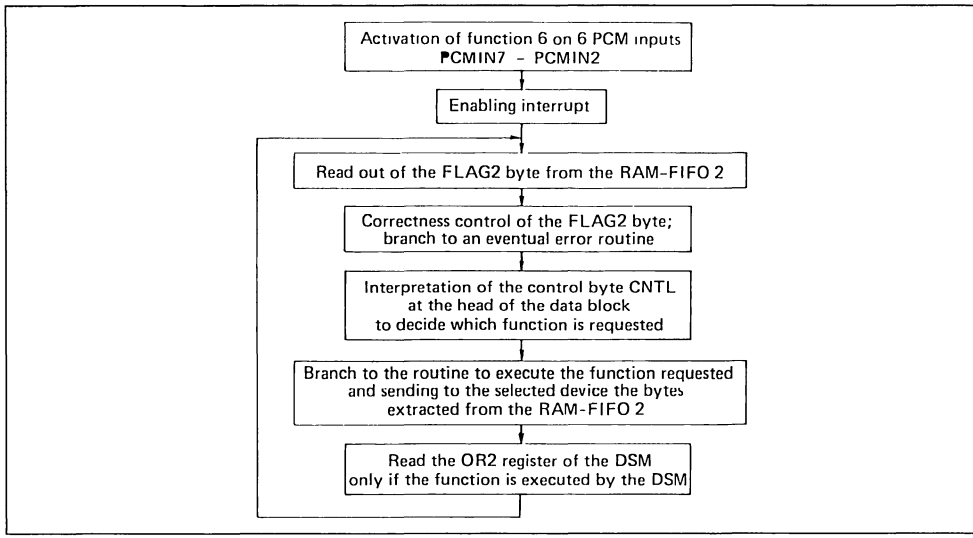
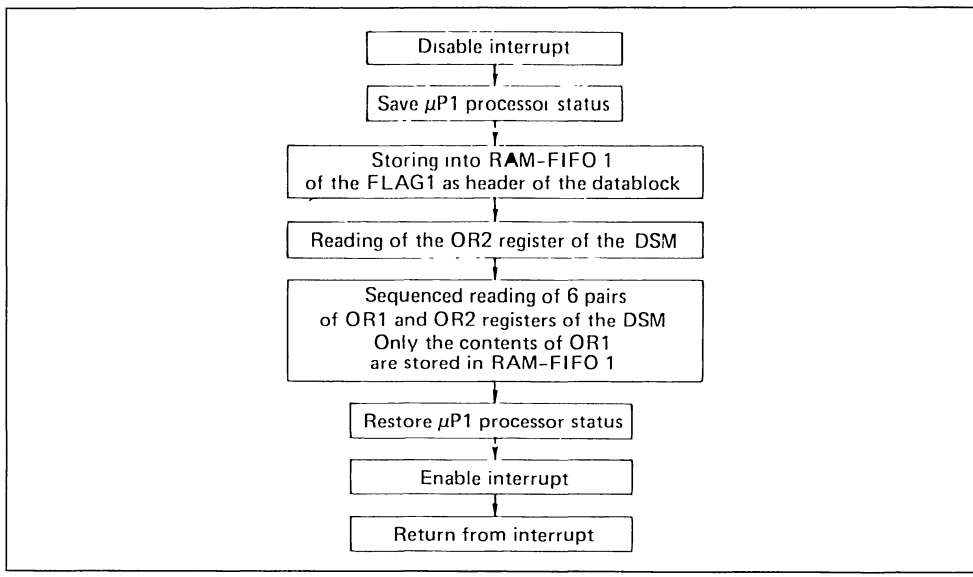


Figure 7 : Interrupt Service Routine Flow-chart.



HOW TO HANDLE SIGNALING IN LARGE SWITCHING SYSTEMS

At the end of this technical note we want to mention the possibility of extending the illustrated solution to system using more SGS MO88 matrices.

We will present here a specific application, without wanting to preclude the adaptability and the applicability of the fundamental idea of how to handle the signaling developed previously, for systems with a larger switching capability.

We refer to figure 8 which shows four MO88s arranged in a 2 x 2 matrix, all controlled by the same µP1 microprocessor. Supposing here some additional Conference and Tone Insertion services and reserving for each PCM input and output flow the channel 0 for the transfer of the signaling from and to the subscriber card and channel 15 for the insertion/extraction of the maintenance service signals, the system represented can control up to a maximum of 420 users arranged on 14 PCM flows and having, furthermore, the possibility of a whole PCM highway output for other auxiliary services.

The µP1 micro also carries out here the functions of an "extractor/actuator". Here there is no restriction with the processing speed : in fact during the MO88 dead times, which are necessary in order to respect the minimum time interval between one operation and another, the micro µP1 can dialogue with another MO88.

In figure 8, since the PCM input flows a, b, c, d, e, f and g are shown in parallel with the MO88-A and the MO88-B, while the h, i, l, m, n, o and p flows are shown in parallel with the MO88-C and the MO88-D, it can be decided that only the DSM-A and C will perform the function of extracting the channels 0 from the input flows. As a result in the main µP1 program, it will be necessary to enable the function 6 only for the seven MO88-A IN PCM flows (11111110 mask) and for the seven MO88-C IN PCM flows (11111110 mask).

The block diagram of the interrupt service routine changes with respect to the case of a unique DSM, as shown in figure 9.

The block diagram shows the alternate reading of both matrices : this allows the functioning of µP1 at an 8 MHz frequency and the minimum time intervals between successive reading operations for each DSM are respected.

There is a similar situation in the phase of sending data bytes and control bytes from µP1 towards the DSM or other devices (CC and TG) to execute various functions : the write operations can be done by µP1 at its highest speed without performing two consecutive writings on the same device.

Regarding the response time of the system, the same considerations must be taken as for the system with a single DSM, since the number of PCM streams is substantially duplicated but at the same time it has been possible to duplicate the execution speed of the µP1 microprocessor which is interfaced with the DSMs.

For the system of the figure 8, there is an alternative solution to the one shown above for the acquisition of the input PCM flows from the channels 0, which consists in enabling function 6 in all of the four MO88s according to the following chart :

The interrupt service routine must read the OR1 and OR2 registers from the MO88 cyclically following the sequence A-C-B-D 6 times and on the seventh time only from A and C, as shown in the block diagram in figure 9 for the reading of only two MO88s.
In this way the micro µP1 can use a 16 MHz clock frequency, since each MO88 is enabled one in four reading operations performed by µP1.

Device	Input PCM Flows Concerned	Mask
M088-A	a b c d	11110000
M088-B	e f g	00001110
M088-C	h i i m	11110000
M088-D	n o p	00001110

CONCLUSION

The process of integrating a greater number of sophisticated functions is a unique device opens the door to new architectural solutions in complex systems which are related to the problem of handling signaling and of switching.
The MO88 digital switching matrix belongs to this category of new devices.

The original architectural solution for switching systems outlined in this technical note is in fact based on using a function of this matrix definitely oriented towards the handling of the signaling.

Figure 8 : Example of Extension of the Proposed Architectural Solution for a Larger Switching Capacity (max. 420 users).

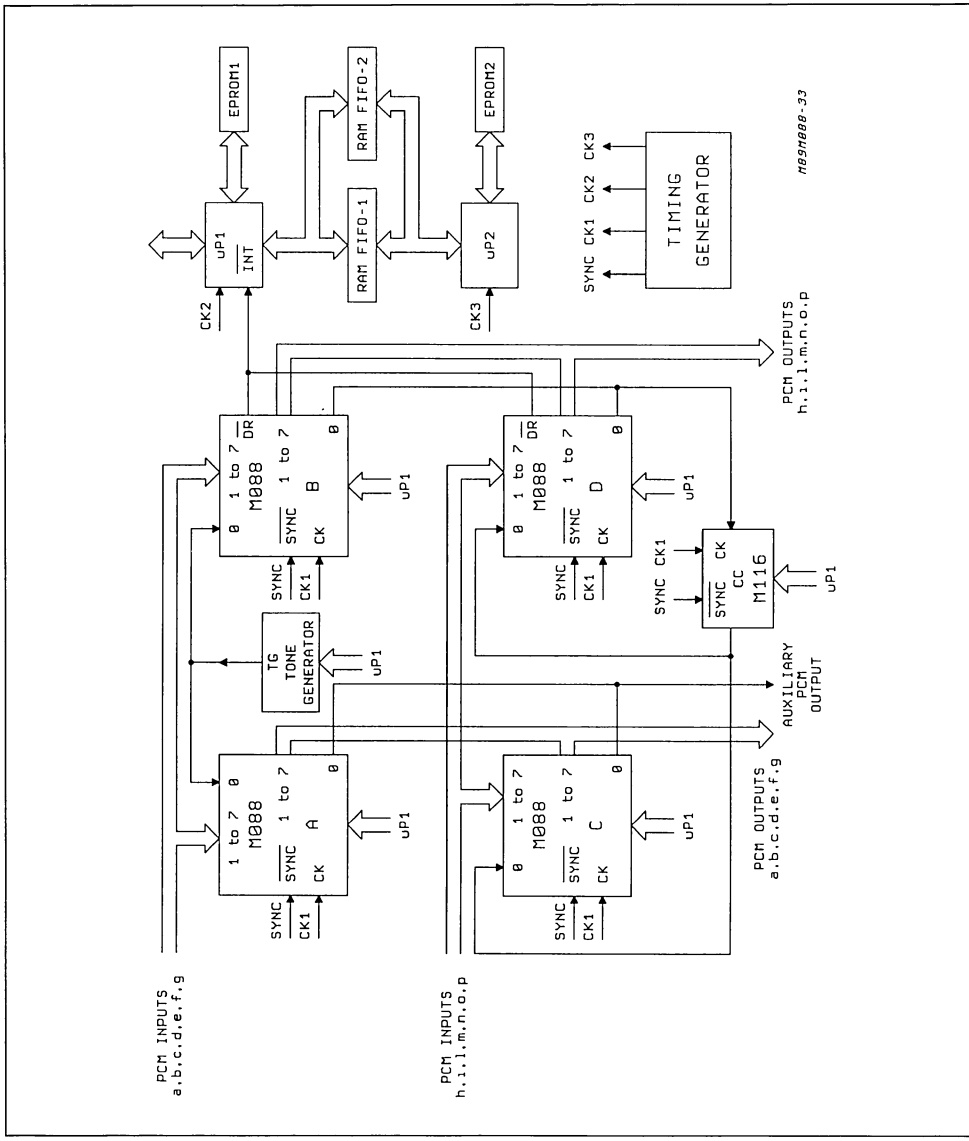
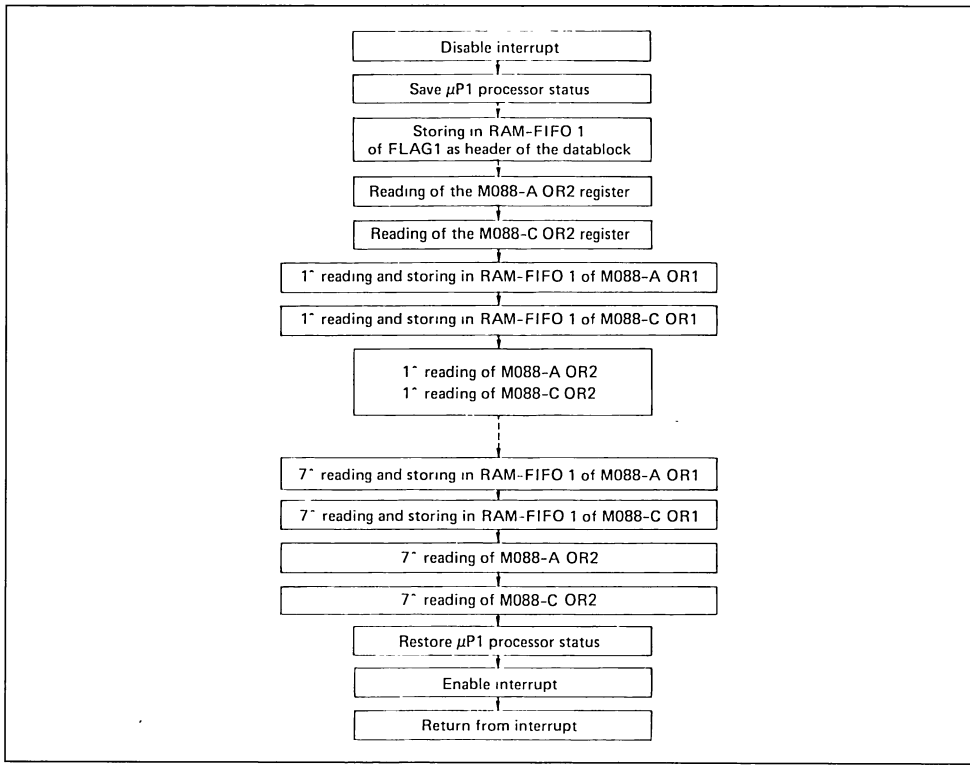


Figure 9 : Interrupt Service Routine Flow-chart for the System Described in fig. 8.



APPENDIX A

MAIN CHARACTERISTICS OF THE MO88 DSM

Figure A-1 gives a concise description of the DSM MO88.

The most significant signals are :

- 8 input PCM highways ;
- 8 output PCM highways ;
- one standard interface for an 8 bit microprocessor.

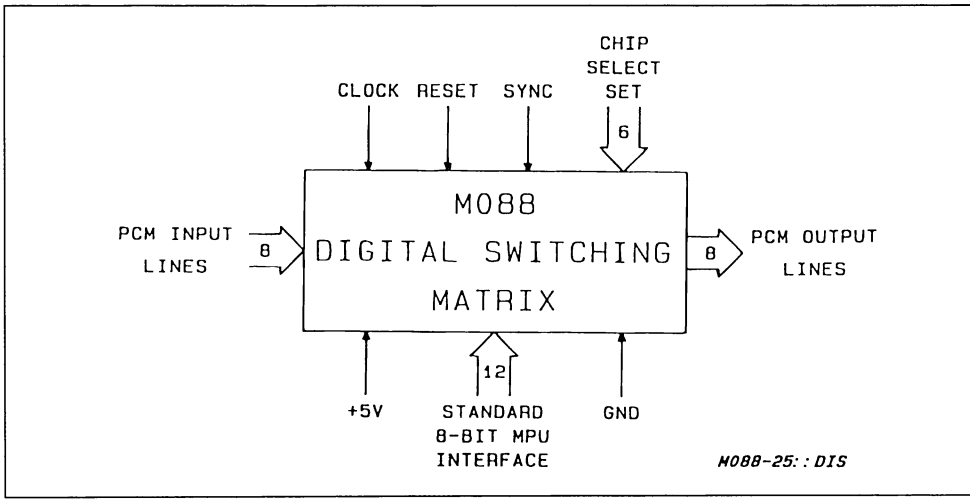
The DSM accepts in input and generated in output PCM highways in accordance either with the European standard (2048 Kbit/s) or with the Northern American one (1536, 1544 Kbit/s).

In the first case each input/output signal contains informations relative to 32 channels at 64 Kbit/s multiplexed with TDM (Time Division Multiplexing) techniques. In consequence, the MO88 DSM is capable of managing the informations coming from 256 input PCM channels.

The DSM interfacing with the microprocessor, can connect each of the 256 input PCM channels with whichever output channel among the 256 ones.

The DSM is "non-blocking", that is it is possible to obtain 256 connections simultaneously.

Figure A1 : M088 Input/Output Signals.



FUNCTIONS OF THE M088 DSM

Under the control of a microprocessor, the MO88 DSM can implement 6 different functions.
A generic function is executed after the microprocessor has sent some data bytes and a command byte through the data bus.

FUNCTION 1 :

Channel Connection/Disconnection. This is the main function. It allows making a new connection between an input PCM channel and an output PCM channel. The disconnection operation is valid only for the DSMs in a matrix structure.

FUNCTION 2 :

Channel Disconnection. It disconnects the selected output channel.

FUNCTION 3 :

Insertion of a Byte/Channel Disconnection. It is used to load a byte supplied by the microprocessor into a specific output channel. The disconnection operation is valid only for the DSMs in a matrix structure.

FUNCTION 4 :

Extraction of a Byte. It is used to transfer the byte contained in a selected output channel to the microprocessor through the data bus. Such a function is used to extract the only byte passing on the selected output channel at the moment of the request. Subsequent extractions are executed only after the new requests have been sent.

FUNCTION 5 :

Reading of the Control Memory. It allows the extraction of information about the status of an output channel : not connected to any input channel, loaded by the micro with a byte (the byte is also available), connect to a specific input channel (the number of the input channel and the number of the input highway to which this channel belonging are also available).

FUNCTION 6 :

Fast Extraction from Channels 0. See Appendix B : "The MO88 function 6".

NOTE : for more details on MO88 DSM see References.

APPENDIX B

THE MO88 FUNCTION 6 : FAST EXTRACTION FROM CHANNELS 0

Function 6 of the MO88 DSM is used to extract the content of the 0 channels belonging to the PCM highways or buses entering into the device on 8 input buses. A mask byte sent from the micro selects which highways the device must take into consideration and among these highways only those 0 channels whose digital word has the two most significant bits not equal to "01" are extracted. MO88 informs through an output signal (DR) the occurring of the extraction of a useful byte. The microprocessor retrieves such byte by reading the content of an internal register of the DSM.

We will see step by step how these actions are performed.

1. Activation of Function 6 : the microprocessor sends the MASK to indicate which input buses or highways must be observed by the device. Then it sends the operation code of instruction 6.

In detail :

Control Signals				Data Buses								Notes
C/D	CS	WR	RD	D7	D6	D5	D4	D3	D2	D1	D0	
0	0	0	1	X	X	X	X	X	M7	M6	M5	1^ Data Byte
0	0	0	1	X	X	X	M4	M3	M2	M1	M0	1^ Data Byte
1	0	0	1	X	X	X	X	1	1	1	0	Operation Code

Where :
M1 = mask bit relative to the nth bus (= 1 if it is the bus to observe or to enable)
X = bit whose value is of no interest

From the moment the operation code has been sent, at the beginning of each frame, the device executes function 6 in a repetitive way, always using the same mask and after having checked that there is not a pending instruction i.e. an instruction which would have been requested by the micro while the DSM was processing function 6. In this last case, before re-enabling the extraction from the channels 0, it executes the pending instruction. This operating way allows to keep function 6 constantly activated without sending again the three bytes mentioned above, but at the same time it allows the device to perform at least another function within a frame interval. Such function can be for example a connection.

2. Control of the Mask Stored by MO88 : it is possible to check if the DSM has correctly stored the mask by reading the internal register OR2 of the DSM. It is possible to obtain the information from MO88 only if the OR2 reading is done in the time interval between the moment when the opcode is sent and the instant in which the DSM makes the results of the extraction available (see below).

In detail :

Control Signals				Data Buses								Notes
C/D	CS	WR	RD	D7	D6	D5	D4	D3	D2	D1	D0	
1	0	1	0	N2	N1	N0	Tn	1	1	1	0	Reading of 0 R2

Where :
N2, N1, N0 = sum of the buses on which the device must activate function 6.
Tn = bit of activation or suppression of function 6.
If a mask has been sent which is not null or not composed only of 0, Tn = 1 : function activated.
If a null mask has been sent, Tn = 0 : function discativated.
1110 = operation code for instruction 6.

Since there are only three bits to indicate the sum of the activated buses, 7 activated buses maximum can be indicated when N1, N2, N3 = 111. The additional information supplied by Tn allows to discern between the case where all 8 buses have been activated (Tn = 1, N1, N2, N3 = 000) and the case where a null mask has been sent (Tn = 0, N1, N2, N3 = 000).

3. Extraction from Channels 0. Activating the extraction can lead to two different results :

3a. there is no useful information in the channels 0 belonging to the activated buses i.e. in all channels 0 tested the PCM words begin with "01". In such case, the DSM prepares itself to accept other instructions until the beginning of the next frame when it will re-activate function 6.

3b. at least in one of the channels 0 tested there is some useful information :

- a level 0 is sent on the DR output pin, level which remains for about two clock intervals (500 nsec. if the clock frequency is 4096 KHz), signaling in this way to the microprocessor that the information obtained on its channels 0 are available.
- the DSM makes available inside itself the contents of the 0 channels in sequential mode starting with the activated flow with the highest identification number.
- the procedure for the extraction of this information must begin with the reading of the OR2 register.

Control Signals				Data Buses								Notes
C/$\overline{D}$	$\overline{CS}$	$\overline{WR}$	$\overline{RD}$	D7	D6	D5	D4	D3	D2	D1	D0	
1	0	1	0	N2	N1	N0	Tn	1	1	1	0	Reading of OR2

Where :
Tn = activation bit. Always = 1 because there are always informations to extract given that the DR has become low.

N2, N1, N0 = sum of the activated buses i.e. sum of those buses previously activated by the sending the mask and with 0 channel's words not beginning with "01". Such sum can only be inferior or equal to the one found previously in the OR2 register before the DR becom became low. Having only 3 bits, the maximum sum can be only 7. In the case in which all 8 input buses are active, the situation of the OR2 bits will be :

N2, N1, N0 = 000 Tn = 1

1110 = operation code of function 6

- the data transfer procedure from MO88 to micro continues by reading alternatively OR1 and OR2 registers.

In detail :

Control Signals				Data Buses								Notes
C/$\overline{D}$	$\overline{CS}$	$\overline{WR}$	$\overline{RD}$	D7	D6	D5	D4	D3	D2	D1	D0	
0	0	1	0	S7	S6	S5	S4	S3	S2	S1	S0	Reading of OR1
1	0	1	0	P2	P1	P0	Fn	1	1	1	0	Reading of OR2

Where :
S7 S0 = PCM word contained in the channel 0 extracted.
P2, P1, P0 = binary number of the bus on which the channel 0 has been read ; the content is present in the OR1 previously read.
Fn = bit indicating if there are other OR1/OR2 pairs to read or not ; in detail :
Fn = 1 : there are other pairs to read in order to complete the execution of function 6.
Fn = 0 : there are no other pairs to read ; the pair read is the last one. Subsequent readings will supply meaningless data.

The alternate reading of both registers is necessary in order to correctly empty the stack in which the PCM words of the extracted channels 0 are stored by MO88. Continuous readings of only one of the registers would mean repeated readings of the same information.

During the reading of OR1 and OR2 registers by the micro, some minimum time intervals between two reading operations must be respect. An interval of at least 13 CLOCK periods (3.2 microseconds for CLOCK frequency equal to 4096 MHz) is necessary for the sequence OR2-OR1, while for OR1-OR2 an interval of 3 CLOCK periods (750 nanoseconds) is sufficient.

The conclusion of the procedure relative to function 6 is ratified by the reading of the OR2 register of the last useful pair (the first OR2 with the Fn bit = 0). It is only after the reading of such register that the DSM starts to process in the same frame the other functions which had been left waiting in the meantime and to re-active the same function 6 at the beginning of the next frame. Forgetting to read this register puts the DSM into a waiting state.

4. Deactivation of Function 6 : when the DSM receives a null mask i.e. made up of all 0s, it will deactivate the procedure of extraction from the channel 0. The deactivation will obviously occur also if the DSM is reinitiated with a RESET pulse.

REFERENCES

1. A Pariani "MO88 Digital Switching Matrix"

2. "MO88 Datasheet".

3. "M116 Datasheet".

CLOCK EXTRACTION AND TERMINAL SWITCHING ICS (EF73321 and EF7333)

1. CLOCK EXTRACTION CIRCUIT

1.1. DESCRIPTION

The EF73321 circuit provides the interface between a 2048 Kbit/s or 1544 Kbit/s PCM trunk and the switching equipment.

PCM junction time recovery as defined by the CCITT generally requires a damped oscillator sustained by logic 1's detected by the PCM junction.

Generally the oscillator consists of coils, capacitors, basic capacitors, and varicaps whose wiring diagram is not easily integrated.

The solution retained is the use of a digital integrated circuit for PCM junction transmission and reception (fig. 1).

The receiving side amplifies and reshapes the bipolar signals from the receive transformer.

From these signals it recovers the distant clock $\overline{HD}$ by means of a local 16384kHz (or 12352kHz) oscillator. The circuit also accepts external clock frequencies lower than or equal to 16384kHz for in line outputs smaller than or equal to 2048Kbits/s. The 16384kHz signal is asynchronous and can be common for different EF73321 circuits. Receive signals are buffered and synchronized with the $\overline{HD}$ clock.

On the transmitting side, it calibrates the applied signal in terms of duration and amplitude by means of a power output stage directly coupled to the primary winding of the transmit transformer.

1.2. BIPOLAR AND HDB3 CODES

Figure 2A shows a series of NRZ (non return to zero) linear data to be transmitted.

The logic 1 or 0 is present throughout the transmission of a bit. There is no return to zero for a logic 1 during this time.

Figure 2B shows this signal converted to bipolar form, logic 0's remain as they are but 1's alternately take a positive and a negative value.

In figures 2C and D this same signal is converted to HDB3 ; not more than three 0's may be received in line. A fourth 0 would systematically be transmitted as a 1 whose bipolarity has been violated with respect to the last 1 transmitted but whose bipolarity is respected compared to the last violation.

Two cases are possible :

- In figure 2C, the preceding violation (not represented) was positive, the first 4-bit word fill-in sequence will be :

  0 0 0 V

  where V is negative, the following fill-in sequence will be :

  B 0 0 V

  where B is a signal element different from zero, in this case positive since B should respect the polarity with respect to the last logic 1.

- In figure 2D, the preceding violation (not represented) was negative. In this case the first fill-in sequence will be :

  B 0 0 V

  where V is positive since the preceding violation was negative, and in order that this polarity really be a bipolarity violation, B is also positive. The value of the second sequence is :

  B 0 0 V

  where V is negative since the preceding bit V was positive and B is also negative and not equal to zero to ensure violation.

Then, it is verified that the sequences described are such that the in-line dc component is really equal to zero. Thus it is possible to use pulse transformers for galvanic insulation between line and terminals.

1.3. APPLICATION N°. 1 : EF73321 WITH FREE RUNNING OSCILLATOR

The crystal oscillator shown in the upper part of figure 3 is of the stand-alone type, t61 frequency in this application is in the order of 16384kHz, frequency accuracy is 50ppm.

One oscillator delivers t61 signals to different EF73321 circuits. Fan out of each 74LS04 gate is 8.

An alternative is to build this oscillator using HCMOS gates, in this case the 6.8 kW pull-up resistors can be ommitted.

The line signal is HDB3 coded with an attenuation of 6dB max for a 3V pulse delivered by a remote transmitter. Figure 4 shows the pulse for PCM CEPT junction.

Transmit and receive transformers are the same type. The transformation ratio between the single winding on the line side and each of both windgins on the circuit side is 2/3 (figure 3).

In this application, transmit and receive sides operate independently, transmission and reception are asynchronous.

Figure 1 : EF73321 Block Diagram.

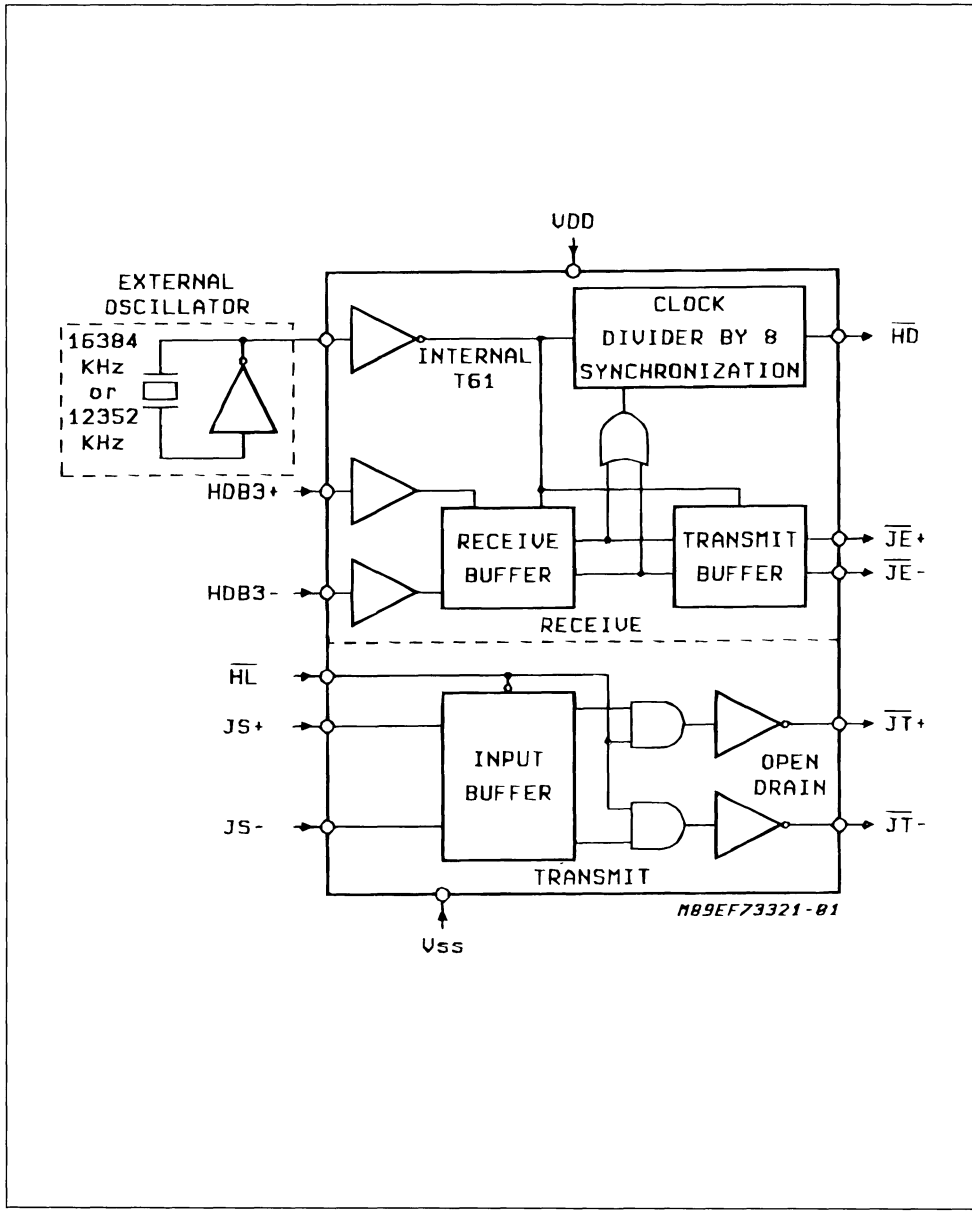
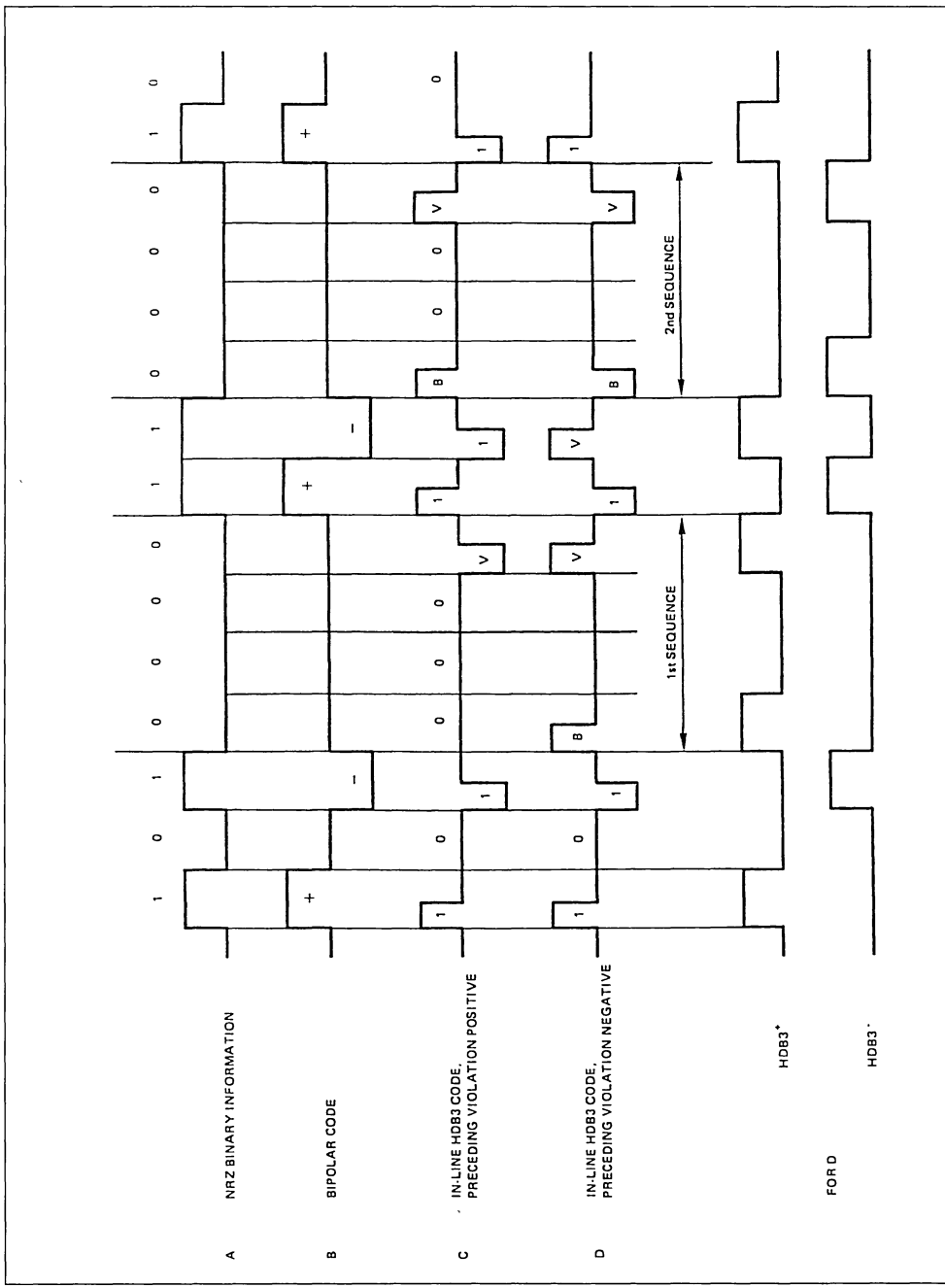


Figure 2 : EF73321 Receive Codes.



1.3.1. RECEIVE SECTION. The information delivered in the form JE+ and JE– at the receive inputs of EF73321 (which are the HDB3 signal rectified signals) have a constant phase relationship with the recovered clock signal HD. The HD clock period will be :

$$8t \pm -2t$$

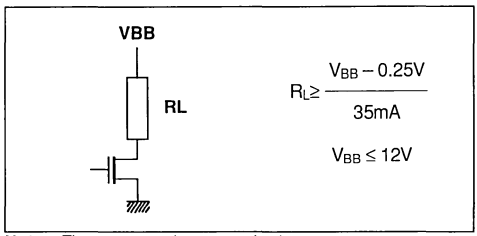
where t is the period of the t61 signal in this application. The delay caused at the input by the receive logic between HDB3+, HDB3– and JE+, JE– is 2t (122ns).

1.3.2. TRANSMIT SECTION. The phase relationship between the information at the JS+ and JS– inputs and the local clock HL should be constant. The positive pulse width defines the line pulse width of the HL signal on the JT+ and JT– outputs.

JT+ and JT– are open drain outputs. Output protection is achieved by sensing the output voltage when low (fig. 6).

Proper operation of the circuit is guaranteed for output currents below 35mA, i.e. as long as the voltage drop on the output is below the protection threshold. Therefore the output current should be limited by design to values below 35mA (see note).

Calculation of the corresponding minimum load resistance at JT+ and JT– is as follows :



Note : This protection does not make the output acting as a current source but switches out the output. For properly selected output loads, maximum power dissipation in each output transistor will be about 30mW

1.4. APPLICATION No. 2 : USING EF73321 WITH SLAVED OSCILLATOR

A buffer memory is used to overcome the differences in the information bit durations caused by the transmission and circuit EF73321. The information is latched by HD and read at the rate of the local clock from the oscillator slaved by HD. The buffer memory capacity only depends from the jitter characteristics and the slaved oscillator correction speed. Figure 7 gives the block diagram of such a memory associated with circuit EF73321. The functions represented are :

- HDB3/BIN code conversion,
- slaved Crystal oscillator,
- frequency dividers,
- buffer memory and its write/read control.

1.4.1. HDB3/BIN CONVERSION. This circuit is used to convert the two HDB3 components to one NRZ signal with the same jitter as the two original components.

1.4.2. CRYSTAL OSCILLATOR. The crystal oscillator frequency is 16.384kHz. It delivers t61 in the form of a square signal with a 61ns period driving the internal logic of circuit EF73321 and the oscillator-associated frequency divider. A submultiple of the crystal frequency is slaved by a submultiple of the distant clock recovered by EF73321.

1.4.3. FREQUENCY DIVIDER ASSOCIATED WITH THE CRYSTAL (read counter). This is a counter in which each stage divides the input signal frequency by 2. After 3 stages a 2048kHz signal is obtained corres-ponding to HD frequency whose jitter amplitude was reduced by the extreme values taken by the slaved oscillator.

The following two bits A' and B' are used to select the buffer memory reading time (see timing diagram of figure 8). The n following bit should be chosen by the user to set the crystal oscillator correction frequency. If n = 6, the oscillator frequency will be corrected every 125 µs.

1.4.4. FREQUENCY DIVIDER ASSOCIATED WITH HD (write counter). The first two bits A and B define the reading time in the buffer memory. If HD shows no jitter, counters A' B' and A, B are in phase and reading takes places with a time delay of 2 bits after writing.

Note : If 3 bits (A, B and C) define the writing time and 3 bits the reading time, reading will take place with a time delay of 4 bit-durations compared to the writing time.

1.4.5. BUFFER MEMORY. This memory consists of a number of bistable circuits depending on the jitter to be recovered. In this example the 4 latches circuits are used to recover a signal with a jitter of ± 2 bits in amplitude without loosing information.

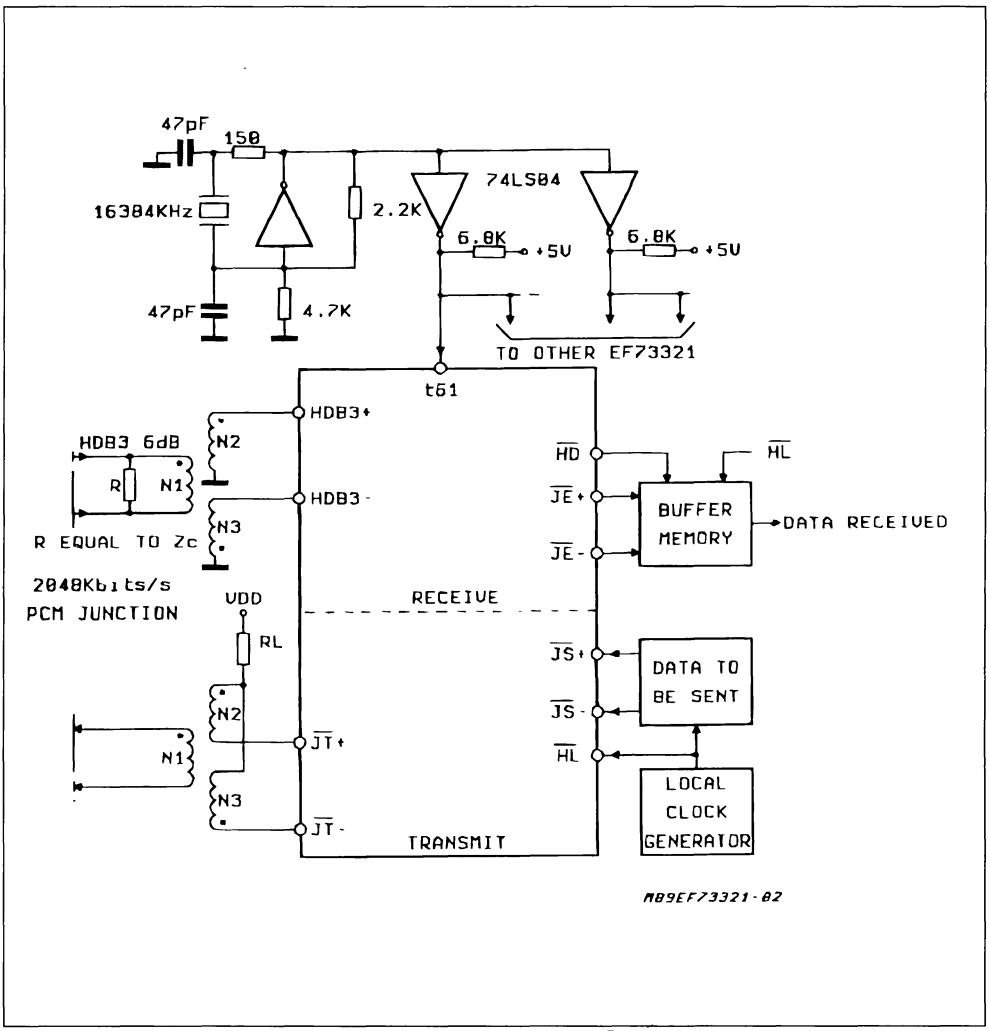
When the write counter A, B defines 2 as writing time, the read counter A' B' defines 0 as reading time and so on.

The residual jitter on the local clock HL and the data are determined by the selected slave crystal oscillator .

1.4.6. TRANSMIT SECTION. In this application the local clock signal HL can be used to sample the data to be transmitted (fig. 7).

Residual jitter is small enough to drive BIN/HDB3 decoder logic and to calibrate line pulse width.

Figure 3 : Application No. 1 - EF73321 Using Free Crystal Oscillation.



Note : A 100nF capacitor must be connected between V_{DD} and V_{SS} as close as possible to the supply pins

Figure 4 : EF73321 Output Stage.

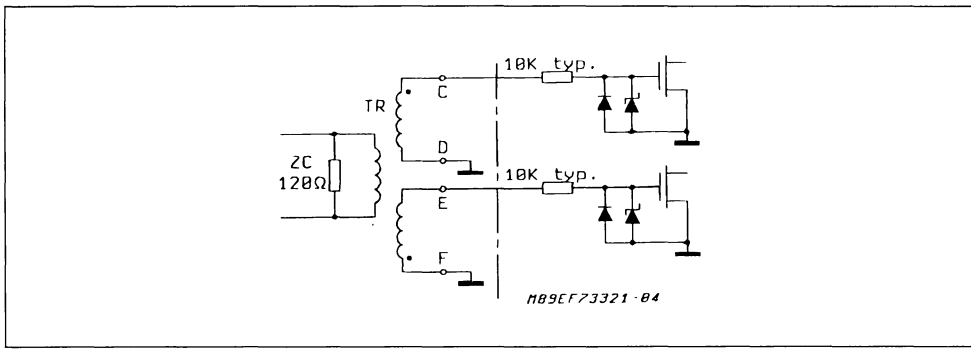


Figure 5 : EF73321 Input Stage.

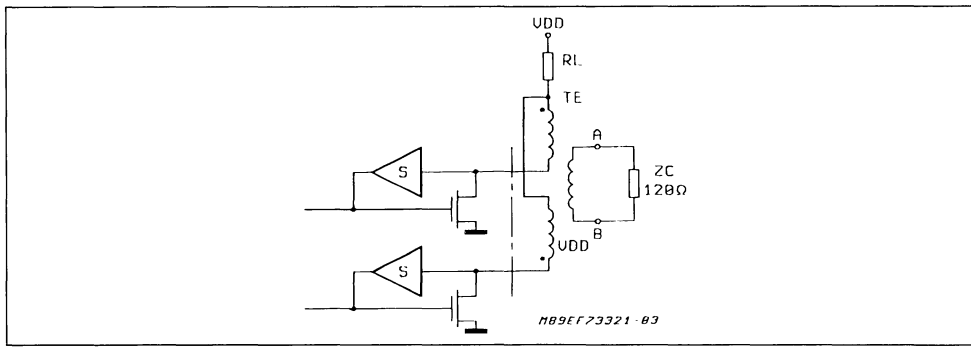


Figure 6 : Pulse Shape for 2048 Bits/s Cept PCM Junction.

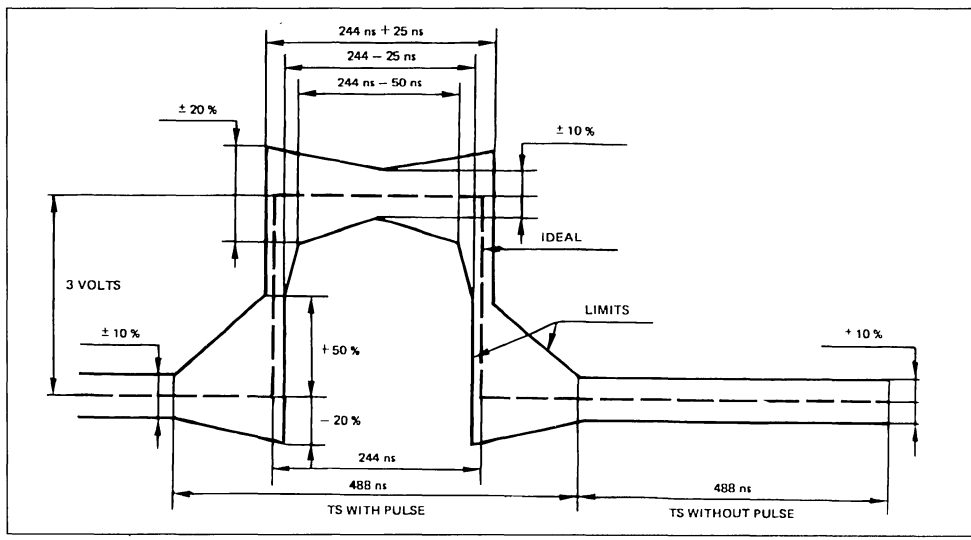
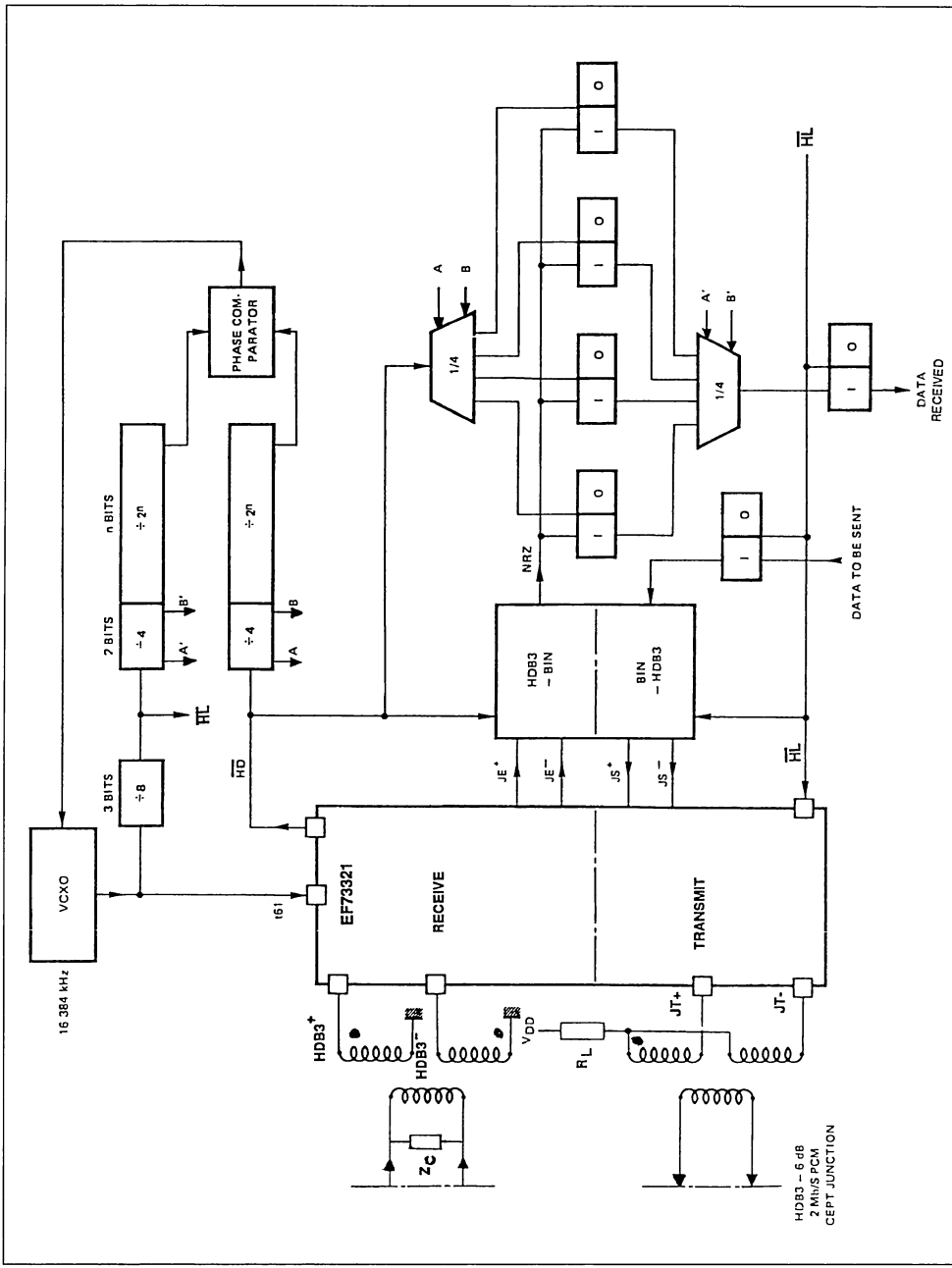
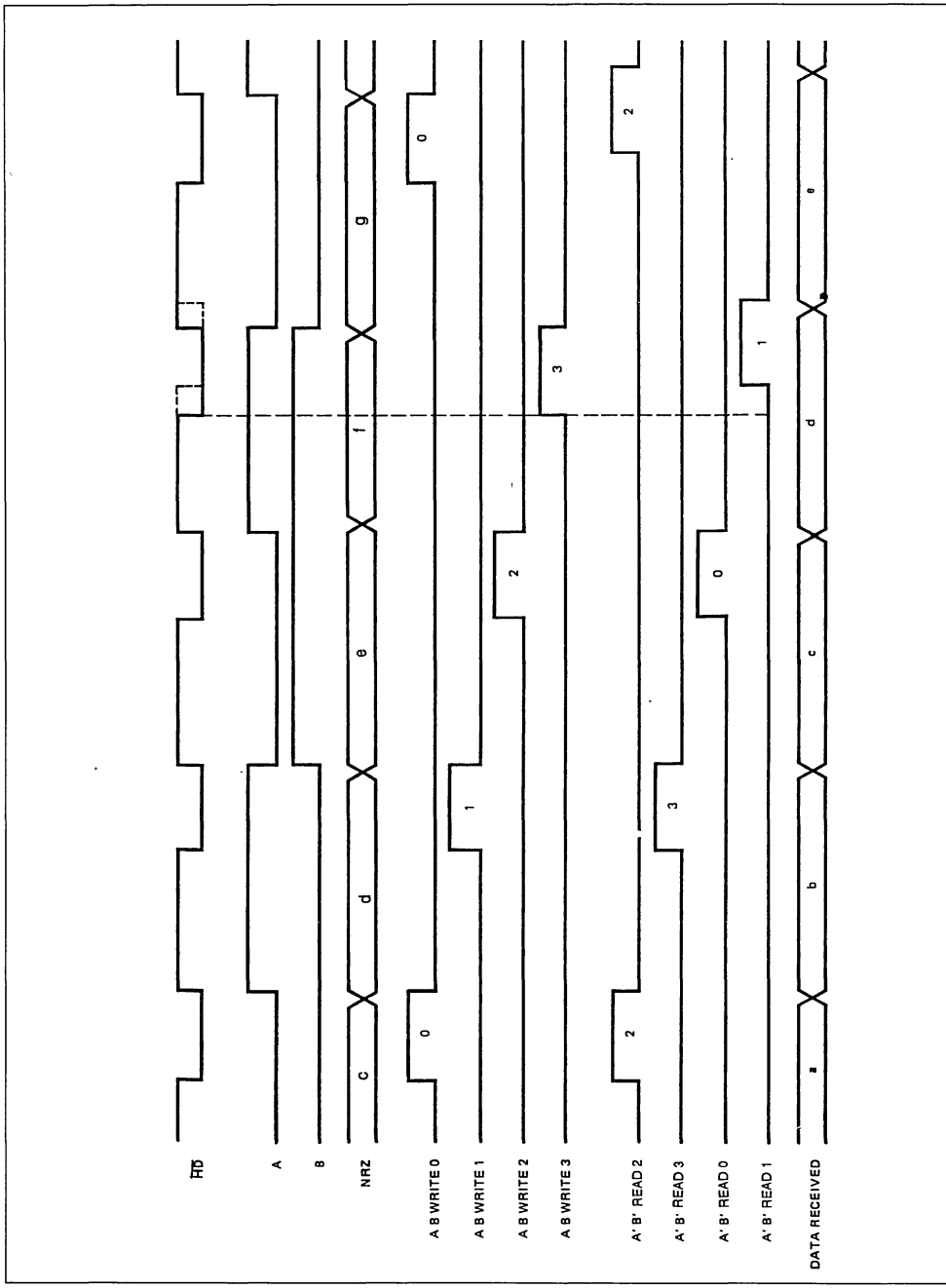


Figure 7 : Application No. 2 - EF73321 with Slaved Oscillator.



Note : A 100nF decoupling capacitor must be connected between V_{DD} and V_{SS} and located as close as possible to the supply pins

Figure 8 : Application Timing Diagram - EF73321 with Slaved Oscillator.



2. TERMINAL SWITCHING CIRCUIT (EF7333)

2.1. CIRCUIT DESCRIPTION

The EF7333 conforms to CCITT recommendation G737. In most applications it is connected between a clock extraction circuit of a PCM junction and multiplex switching circuits at 2.048Mbits/s.

The EF7333 basic functions are :

- frame synchronization of PCM junction input section with local clock,
- absorption of line jitter whose amplitude and frequency are given in EF7333 specifications.

In addition to these basic functions, the device also features :

– Incoming link processing functions :
- input signal HDB3, binary or bipolar decoding
- frame skip or doubling
- receive errors detection and alarms generation
- remote alarm extraction

– Outgoing link processing functions :
- insertion of synchronisation words into outgoing frames
- output signal binary, HDB3 or bipolar coding
- receive fault alarm transmission

The receive function provides a multiplex signal at 2.048Mbit/s synchronized with local center clock (fig. 10). The local center can be a connection network, a time concentrator, a computer interface, etc.

So, the PCM junctions from various centers in a plesiochronous network can be synchronized with the local center clock. Figure 9 shows that whatever the phase relationship between remote clocks HD1, HD2,...HDn, circuit EF7333 associated with remote centers can set in phase not only time slots but also incoming multiplex frames.

If distant and local centers are synchronized by a common clock (not represented on fig. 9). The EF7333 circuit resynchronizes the multiplex signal without loss of information accepting a peak-to-peak jitter of several time slots for very low jitter frequencies.

If remote centers are asynchronous, circuits EF7333 synchronizes the multiplex by skipping or doubling frames without loss of synchronisation.

Figure 9 : Plesiochronous Network.

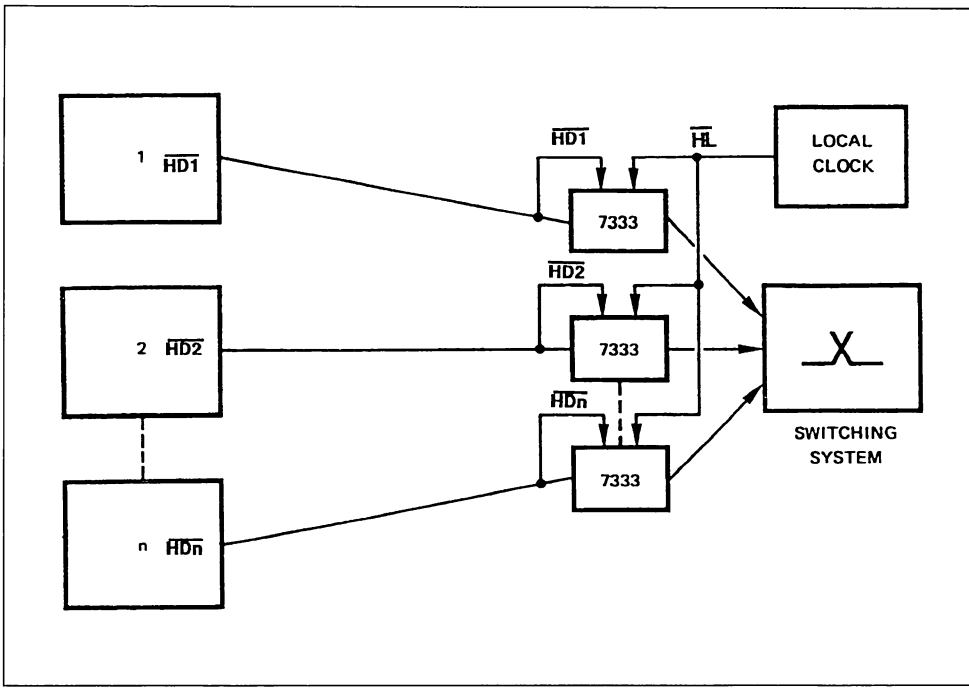
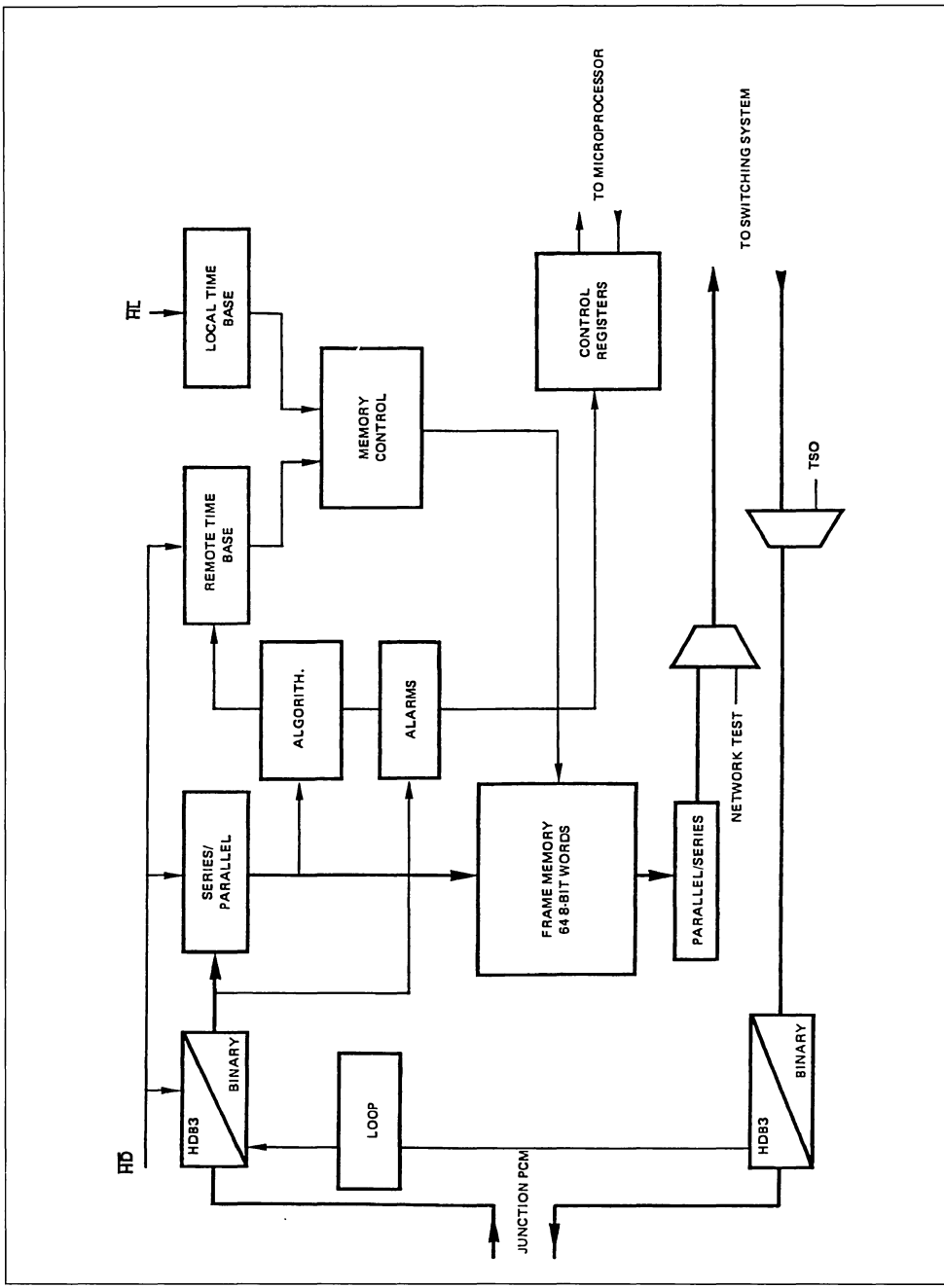


Figure 10 : Switching Terminal Module.



2.2. APPLICATION No. 3 : BINARY INPUTS - BINARY OUTPUT

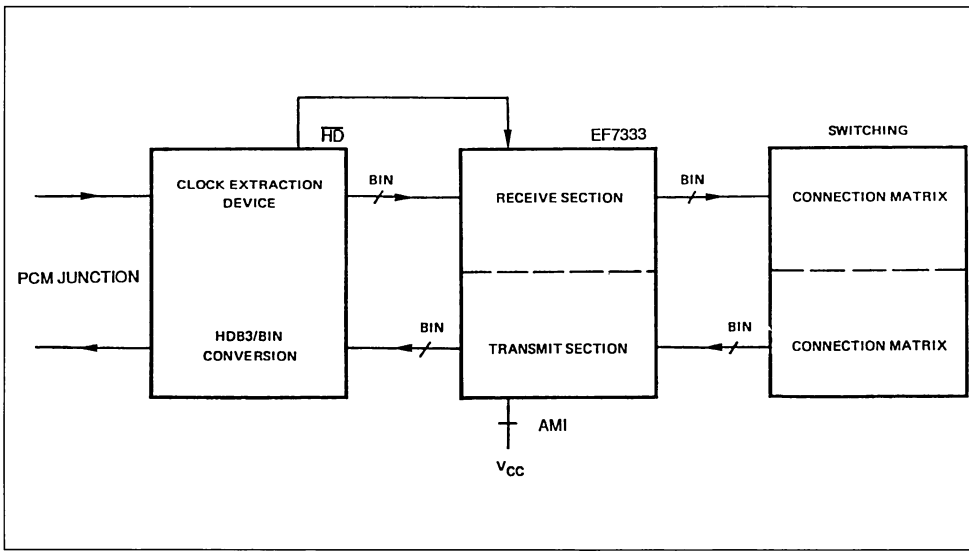
Figure 11 shows an environment where the EF7333 incoming and outgoing data are binary. Pin AMI is used to select the incoming data code. The incoming signal can be applied either on JE+ or JE– but the unused pin must be tied to VDD. The output signal is available on JS+ and JS–. In the receive mode a device external to circuit EF7333 should deliver :

- the clock signal recovered from an amplifier that has reshaped the signal likely to have been attenuated during line propagation,
- the associated information which has been converted (from HDB3 to binary).

In the same way, in the transmission mode circuit EF7333 receives a multiplex signal from the line, processes the 0 time slot content (TSO) in accordance with CCITT recommendations. A device external to the EF7333 circuit receives the processed multiplex signal and can convert it from binary to HDB3 before transmitting it in line.

This application enables the user to select line reception and transmission amplifiers depending on transmission characteristics.

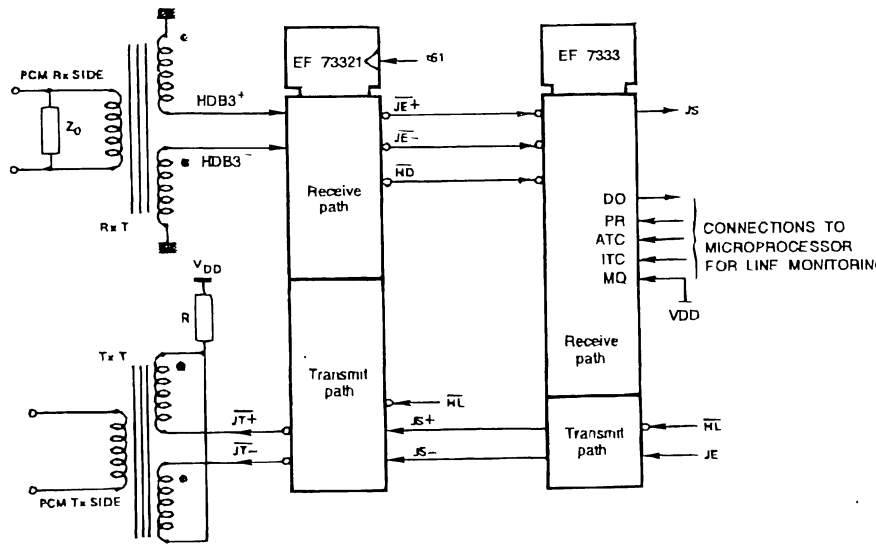
Figure 11 : Binary Incoming and Outgoing Information.



2.3. APPLICATION No. 4 : EF73321 - EF7333 ASSOCIATION USED WITH MARKER INTERFACE.

The diagram in figure 12 shows the whole switching terminal function. No additional circuitry is required between circuits EF73321 and EF7333. They are designed for direct interface.

Figure 12 : EF73321 and EF7333 Association.



t61 . 16384kHz clock
R x T : Line receive transformer
T x T : Line transmit transformer
HL : Local 2048kHz clock

Note : EF73321 layout considerations . for correct operation of transmission drivers, a 100nF decoupling capacitor must be connected between V_{DD} and V_{SS} and located as close as possible to the supply pins.

In this application MQ is wired to V_{DD}. A microprocessor can access the six internal registers R1 to R6. These registers are accessed by pins ITC, ATC, D0 and PR.

Pin ATC receives the register address and pin ITC receives the code to be written into the address register. The last bit of ATC is a read bit and the last bit of ITC is a write bit. The register content may be read serially at D0. PR valids data on ITC state, ATC and D0. D0 is in high impedance when PR is low.

Registers functions :

Register R1 : contains the outgoing junction even frame TS0 value. Only bit 1 can be accessed by the micro processor interface. The content of this register will be transmitted in line if the circuit is not operating in looped mode.

Register R2 : contains the outgoing junction odd frame TS0 value. Only bit 2 cannot be modified, it remains at "1". Bit 3 can either be at "0" or "1" as a result of a logic OR with the 3 alarms JDSY, TE and MQHX. The content of this register will be transmitted in line only if the circuit is not operating in looped mode.

Register R3 : will contain a value to be introduced into even frame TS0 (8 bits). Its content is transmitted in looped mode.

Register R4 : will contain a value to be introduced into odd frame TS0. Its content is transmitted in looped mode.

Register R5 : is a read only register containing the alarms. It is controlled by receive function of EF7333 circuit.

- bit 1 contains the value of bit 3 of incoming junction odd frame TS0. When the value of this bit is "1", this means that the remote end does not control the frame it receives any more. (PVTD alarm - remote frame locking loss).
- bit 2 indicates that the EF7333 synchronous device has found no frame locking code (PVTL alarm - local frame locking loss).
- bit 3 indicates that clock $\overline{HD}$ is missing (MQHX alarm).
  In this application oscillator t61 has stopped operating.
- bit 4 indicates that the synchronous device is no more synchronized (JDSY alarm - synchronization loss)
- bit 5 indicates that a SIA signal is received (SIA alarm - remote alarm indication signal).
  When JDSY = 0, the junction is synchronized and SIA = 0.
  When JDSY = 1, the junction is not synchronized and SIA = 1 during two frames.
- bit 6 indicates an excessive error rate higher than 10^{-3} detected on the frame locking codes (TE alarm).
- bit 7 indicates local clock lead or delay compared to remote clock (AV alarm).
  - AV = 1 : frame skip ($\overline{HD}$ faster than $\overline{HL}$).
  - AV = 0 : frame doubling ($\overline{HD}$ slower than $\overline{HL}$).
- bit 8 indicates frame skip or doubling on reading of internal frame memory. Its state changes on each frame skip or doubling operation (SAUT alarm).

Register R6 : Contains only 1 bit for selecting the looped mode ;

- if R6 = 0, normal operation, the contents of R1 and R2 are in line.
- if R6 = 1, looped mode operation. JS+ and JS– are internally connected to JE+ and JE–, and $\overline{HD}$ is internally connected to $\overline{HL}$. The contents of R3 and R4 are in line.

TSO	R6	
	R6 = 0	R6 = 1
Output JS + and JS –	Content of R1 and R2	Content of R3 and R4
Input Reception	Content of JE+ and $\overline{JE–}$	Content of R3 and R4

Note : Registers R1 to R6 are not initialized when powering-up the EF7333.

2.4. APPLICATION No. 5 : EF7333 WITHOUT MARKER INTERFACE

In this application, pin MQ is wired to V_{SS}. The alarms are directly available on real time on the alarm register outputs. The free bits of register R1 and R2 are set to "1".

Bit 3 of register R5 resulting of the logic OR of three alarms JDSY, TE and MQHX is internally set to "1" and transferred on the line by register 2 bit 3.

Caution :

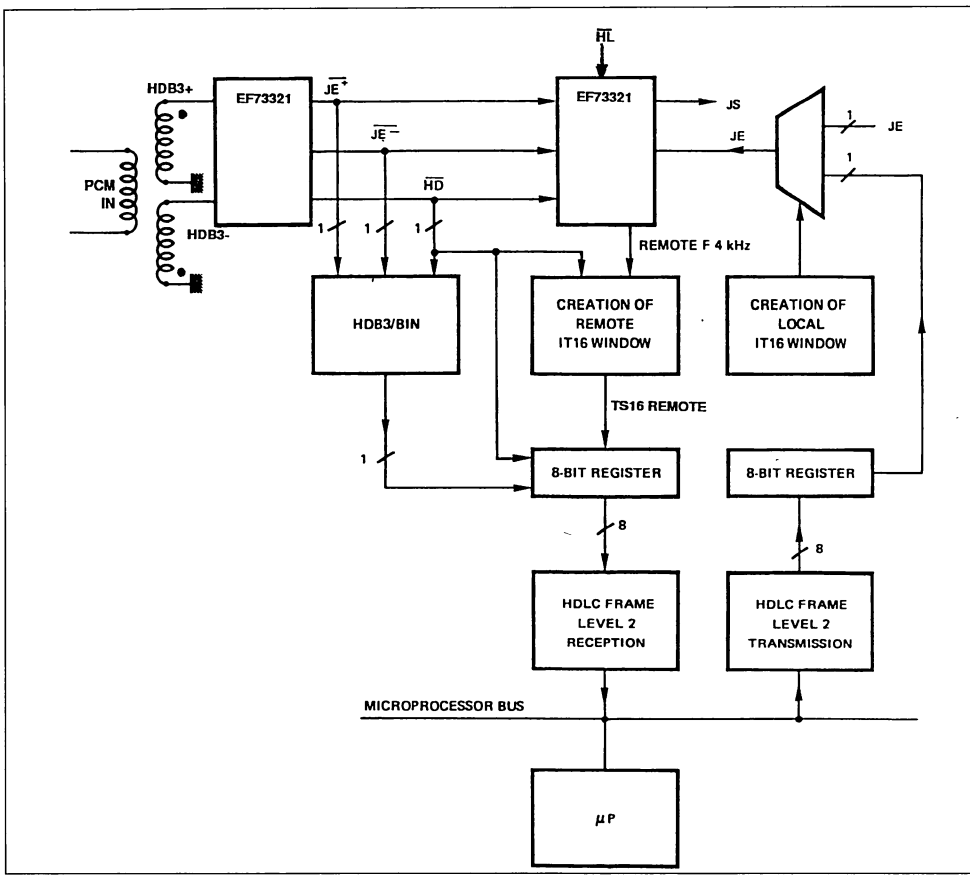
When MQ ≠ 0, PR, ITC and ATC inputs must also be tied to "0".

2.5. APPLICATION No. 6 : EXTRACTION OF TS16 CONTENT WITHOUT LOSS OF INFORMATION

We have seen that when the remote device was asynchronous with the local EF7333 circuit. Frames may be skipped or repeated between transmit and receive clocks.

For 64 Kbit voice channels, the suscriber will not be aware of frame skips or doubling, but for data channels, OSI system levels 2 (or 3) ensuring the exchange protocol between the two units will request repetition of the message. The following device avoids message repetition although the units are of the plesiochronous type.

Figure 13 : Remote TS16 Extraction.



Device description

One of the EF7333 outputs labeled F4kHz (pin 15) delivers 4kHz for the remote clock. The EF7333 extracts the 4kHz remote clock from the incoming junction in the same way as the EF73321 extracts the HD 2MHz remote clock from the incoming junction.

It is possible to extract a TS content, for example TS16 content from incoming signals HD, JE+, JE– and from signal F 4kHz (fig. 13).

An 8-bit word is delivered to a series-parallel register by a HDB3 converter operating at HD clock rate. This word is selected by a device giving the time slot chosen, for example TS16. At the end of TS16 the register content is loaded into a parallel-parallel register ; a microprocessor can read this word after an interrupt for example. In the transmit mode, the microprocessor of figure 13, delivers a HDLC frame that can be inserted in TS16 of circuit EF7333 local multiplex JE (transmit side).

Position of signal F 4kHz with respect to JE+, JE–, HD.

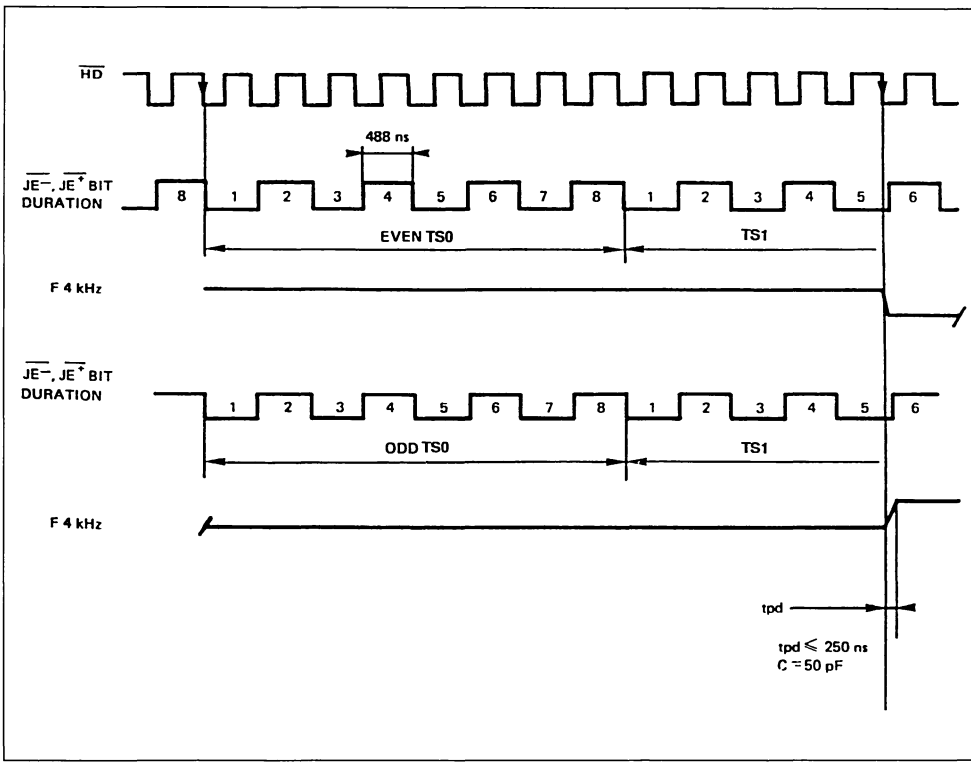
The EF7333 internal logic works on HD falling edge (receive side). Figure 14 shows the 250µs period F 4kHz signal with respect to :

- recovered remote clock (pin 12),
- JE+, JE–,

The 4kHz signal switches to another state on HD falling edge when bit 5 of TS0 arrives on JE–, JE+ (pins 7 and 8).

The delay (tpd) compared to HD falling edge is 250ns max for a 50pF load.

Figure 14 : F 4kHz Position with Respect to HD and Bit Duration of JE+ / JE–.



Note : if JDSY = 1, F 4kHz = 0.

SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE

SGS-THOMSON SLIC KIT AC MODELS

BY W. ROSSI, A. PARIANI

INDEX

1. INTRODUCTION

In this note you can find the basic structure of all SGS-THOMSON Microelectronics SLIC KIT concerning AC performances.

In all these KITs are present two capacitors one for AC/DC path splitting and the other for loop stability. The effect of these capacitors is neglectible in speech band (300 - 3400Hz) therefore for each KIT are evaluated the typical AC performances not considering their influence.

If performances on a wider band or very high accuracy are requested the effect of these capacitors must be included.

Another possibility to study the effect of these capacitors is to enter the SLIC structure in a circuit simulator like SPICE, as shown at the end of this note with the L3000/L3090 SLIC KIT.

2. L3000/L3010 SLIC KIT BASIC STRUCTURE

Here below you can see the basic structure of the L3000/L3010 SLIC KIT concerning AC performances.

For an easier representation the high voltage part is drawn as a single ended amplifier with a gain of 40. Close to each node is written the corresponding pin number of L3010. The components names are the same used in the data sheet.

Figure 2.1 : L3000/L3010 SLIC Basic Structure.

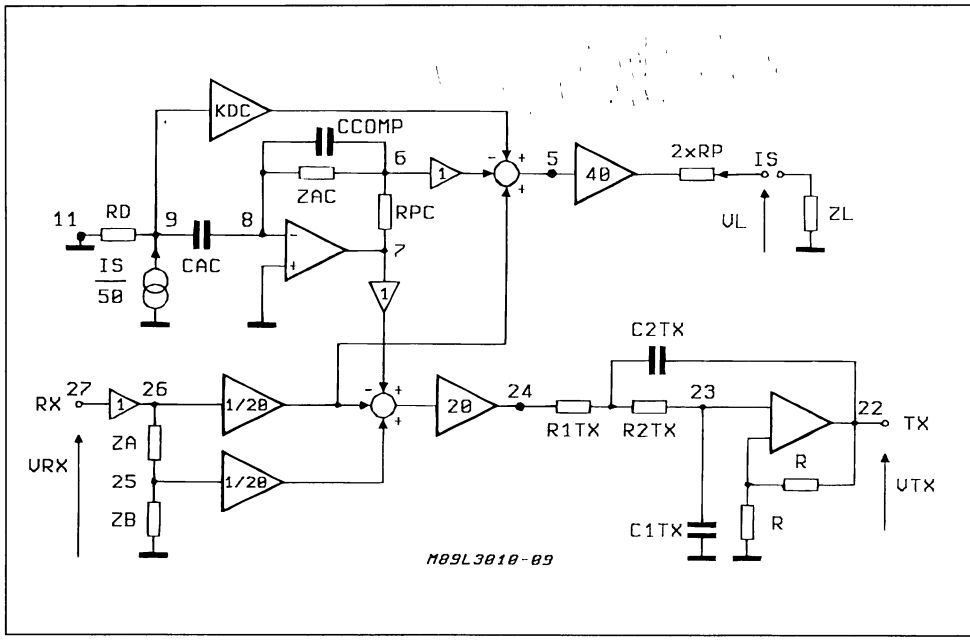
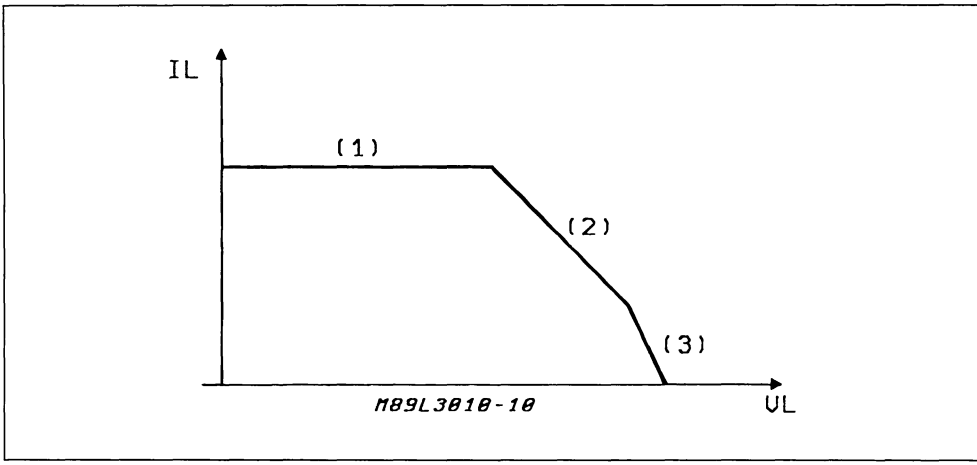


Figure 2.2 : L3000/L3010 DC Characteristic.



The RD and KDC values depends on the working point on DC characteristic, in particular :

RD = infinite ; KDC = 2 for region 1

RD = RDC ; KDC = 2 for region 2

RD = RDC ; KDC = 2/3 for region 3

CAC is a large capacitor (typ. 22µF) used to split AC and DC components of line current.

CCOMP is a small capacitor (typ. 8.2nF) used to guarantee loop stability.

CAC and CCOMP values are chosen in order to have a neglectible effect on speech band signals, therefore supposing CCOMP equivalent to an open circuit and CAC to a short circuit the following relationships can be easily obtained from the circuit diagram of fig. 2.1. Also the TTX filter influence in speech band is neglected.

2.1. SLIC IMPEDANCE AT LINE TERMINATIONS :

$$ZML = \frac{V_L}{I_S}\bigg|_{VRX=0} = (4/5) \times ZAC + 2 \times RP$$

2.2. RECEIVING GAIN :

$$G_R = \frac{V_L}{V_{RX}} = 2 \times \frac{ZL}{ZL + ZML}$$

therefore if ZL = ZML

$$G_R = 1$$

2.3. SENDING GAIN

$$G_S = \frac{V_{TX}}{V_L}\bigg|_{VRX=0} = -\frac{ZAC + RPC}{ZAC + (5/2) \times RP}$$

therefore if RPC = (5/2) x RP

$$G_S = -1$$

2.4. TRANS-HYBRID LOSS

$$THL = \frac{V_{TX}}{V_{RX}} = 2 \times \left(\frac{ZB}{ZA + ZB} \frac{ZL+2 \times RP - (4/5) \times RPC}{ZL + ZML}\right)$$

therefore if RPC = (5/2) x RP and ZA/ZB = ZML/ZL

THL = 0

If you need a more careful evaluation of AC performances you can include also the effect of CCOMP, CAC and TTX filter in the above relations or you can simulate the system behavior with SPICE or other circuit simulators (see example at par. 6).

3. L3000/L3030 SLIC KIT BASIC STRUCTURE

Here below you can see the basic structure of the L3000/L3030 SLIC KIT concerning AC performances.

For an easier representation the high voltage part is drawn as a single ended amplifier with a gain of 40. Close to each node is written the corresponding pin number of L3030 in PLCC package. The components names are the same used in the data sheet.

As you can see on the L3000/L3030 data sheet the large AC/DC splitting capacitor (typ. 22µF) can be avoided using the on chip capacitor multiplier. In the following you can see the basic structure in both cases.

Figure 3.1 : L3000/L3030 SLIC Configured without Capacitor Multiplier Basic Structure.

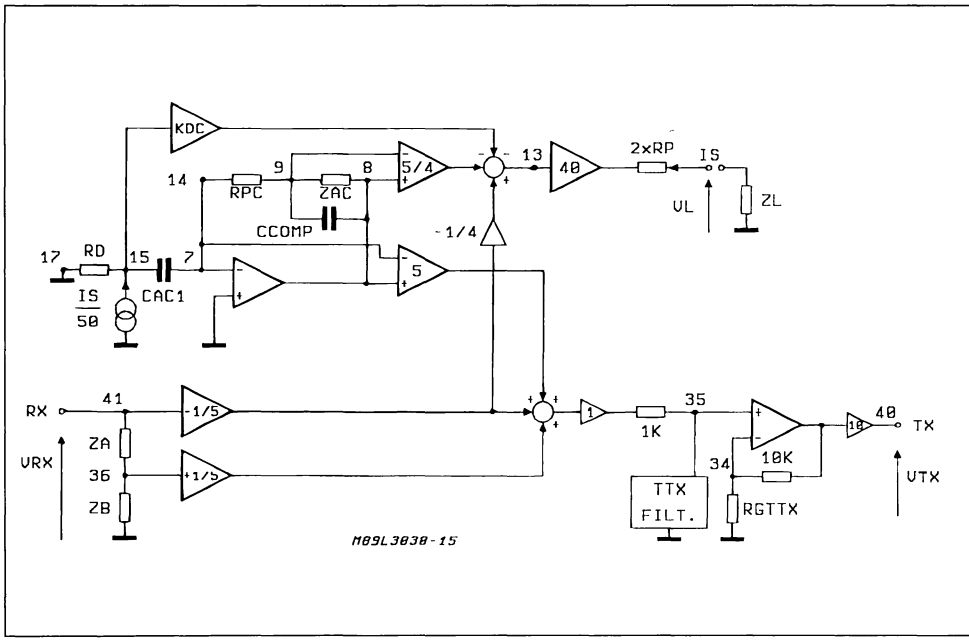


Figure 3.2 : L3000/L3030 SLIC Configured with Capacitor Multiplier Basic Structure.

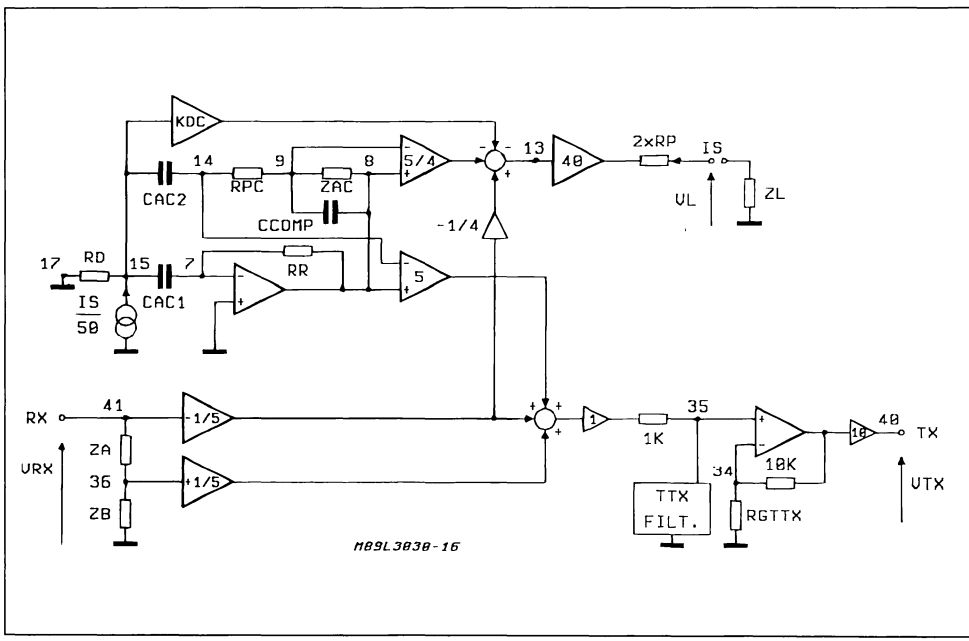
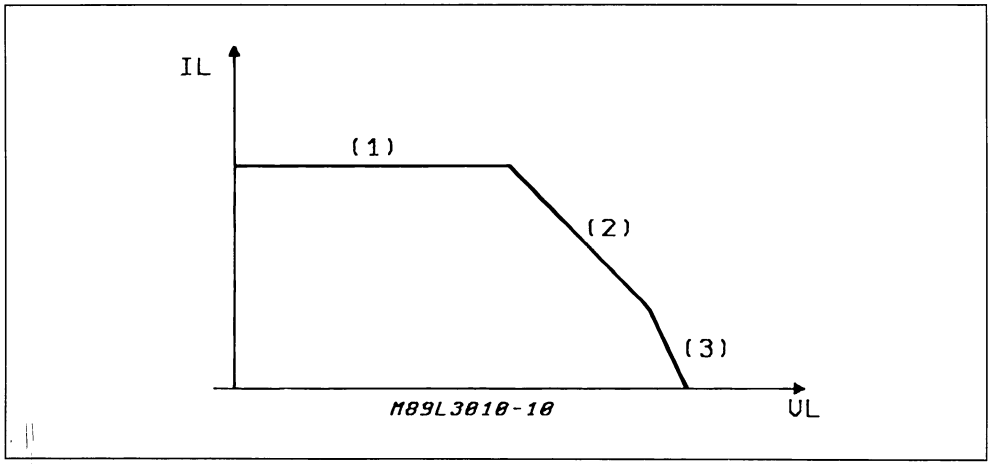


Figure 3.3 : L3000/L3030 DC Characteristic.



The RD and KDC values depends on the working point on DC characteristic, in particular :

RD = infinite ; KDC = 5/4 for region 1

RD = RDC ; KDC = 5/4 for region 2

RD = RDC ; KDC = 5/12 for region 3

CAC1 or the sinthetized capacitor obtained with the capacitor multiplier is relatively large (typ. 22µF) and it is used to split AC and DC components of line current.

CCOMP is a small capacitor (typ. 10nF) used to guarantee loop stability.

CAC1, CAC2 and CCOMP values are chosen in order to have a neglectible effect on speech band signals, therefore supposing CCOMP equivalent to an open circuit and CAC1 or the sinthetized capacitor obtained with the capacitor multiplier equivalent to a short circuit the following relationships can be easily obtained from the circuit diagram of fig. 3.1. Also the TTX filter influence in speech band is neglected. The TTX filter impedance is supposed to be equal to RGTTX/10 in speech band and zero at the TTX frequency.

3.1. SLIC IMPEDANCE AT LINE TERMINATIONS :

$$ZML = \left.\frac{V_L}{I_S}\right|_{VRX=0} = ZAC + 2 \times RP$$

3.2. RECEIVING GAIN :

$$G_R = \frac{V_L}{V_{RX}} = 2 \times \frac{ZL}{ZL + ZML}$$

therefore if ZL = ZML

$$G_R = 1$$

3.3. SENDING GAIN

$$G_S = \left.\frac{V_{TX}}{V_L}\right|_{VRX=0} = -\frac{ZAC + RPC}{ZAC + 2 \times RP}$$

therefore if RPC = 2 x RP

$$G_S = -1$$

3.4. TRANS-HYBRID LOSS

$$THL = \frac{V_{TX}}{V_{RX}} = 2 \times \left(\frac{ZB}{ZA + ZB} - \frac{ZL + 2 \times RP - RPC}{ZL + ZML}\right)$$

therefore if RPC = 2 x RP and ZA/ZB = ZML/ZL

THL = 0

If you need a more careful evaluation of AC performances you can include also the effect of CCOMP, CAC and TTX filter in the above relations or you can simulate the system behavior with SPICE or other circuit simulators (see example at par. 6).

4. L3000/L3090 SLIC KIT BASIC STRUCTURE

Here below you can see the basic structure of the L3000/L3090 SLIC KIT concerning AC performances.

For an easier representation the high voltage part is drawn as a single ended amplifier with a gain of 40. Close to each node is written the corresponding pin number of L3090. The components names are the same used in the data sheet.

Figure 4.1 : L3000/L3090 SLIC Basic Structure.

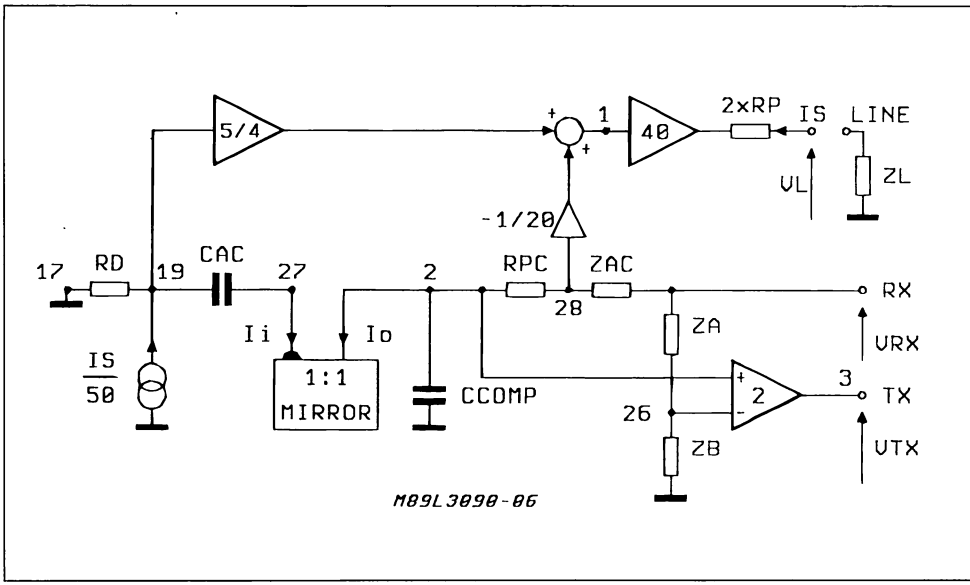
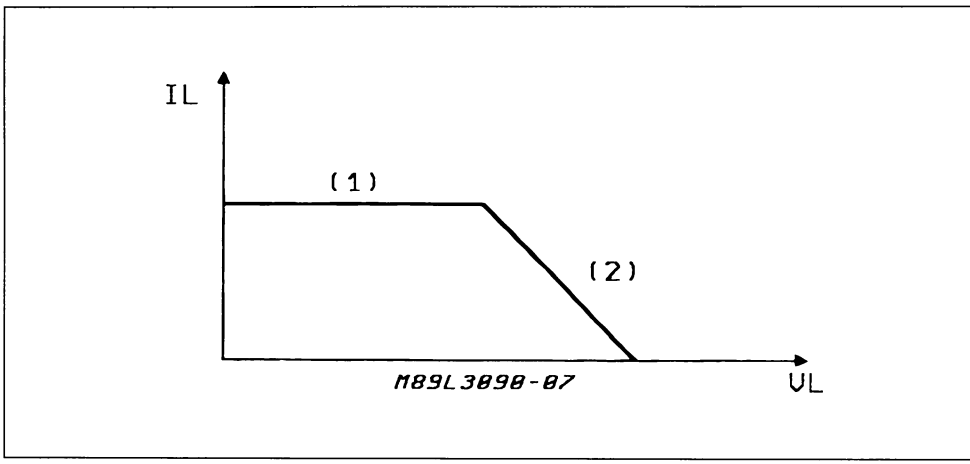


Figure 4.2 : L3000/L3090 DC Characteristic.



The RD value depends on the working point on DC characteristic, in particular :

RD = infinite for region 1

RD = RDC for region 2

CAC is a large capacitor (typ. 47µF) used to split AC and DC components of line current.

CCOMP is a small capacitor (typ. 390pF) used to guarantee loop stability.

CAC and CCOMP values are chosen in order to have a neglectible effect on speech band signals, therefore supposing CCOMP equivalent to an open circuit and CAC to a short circuit the following relationships can be easily obtained from the circuit diagram of fig. 4.1.

4.1. SLIC IMPEDANCE AT LINE TERMINATIONS :

$$ZML = \left.\frac{V_L}{I_S}\right|_{VRX=0} = (ZAC/25) + 2 \times RP$$

4.2. RECEIVING GAIN :

$$G_R = \frac{V_L}{V_{RX}} = -2 \times \frac{ZL}{ZL + ZML}$$

therefore if ZL = ZML

$$G_R = -1$$

4.3. SENDING GAIN

$$G_S = \left.\frac{V_{TX}}{V_L}\right|_{VRX=0} = -\frac{ZAC + RPC}{ZAC + 25 \times (2 \times RP)}$$

therefore if RPC = 25 x (2 x RP)

$$G_S = -1$$

4.4. TRANS-HYBRID LOSS

$$THL = \frac{V_{TX}}{V_{RX}} = 2 \times \left(\frac{ZL + 2 \times RP - (RPC/25)}{ZL+ZML} - \frac{ZB}{ZA+ZB}\right)$$

therefore if RPC = 25 (2 x RP) and ZA/ZB = ZML/ZL

THL = 0

If you need a more careful evaluation of AC performances you can include also the effect of CCOMP and CAC in the above relations or you can simulate the system behavior with SPICE or other circuit simulators (see example at par. 6).

5. TDB7722/TDB7711 SLIC KIT BASIC STRUCTURE

Here below you can see the basic structure of the TDB7722/TDB7711 SLIC KIT concerning AC performances.

For an easier representation the high voltage part is drawn as a single ended amplifier with a gain of 40. Close to each node is written the corresponding pin number of TDB7711. The components names are the same used in the data sheet.

Figure 5.1 : TDB7722/TDB7711 SLIC Basic Structure.

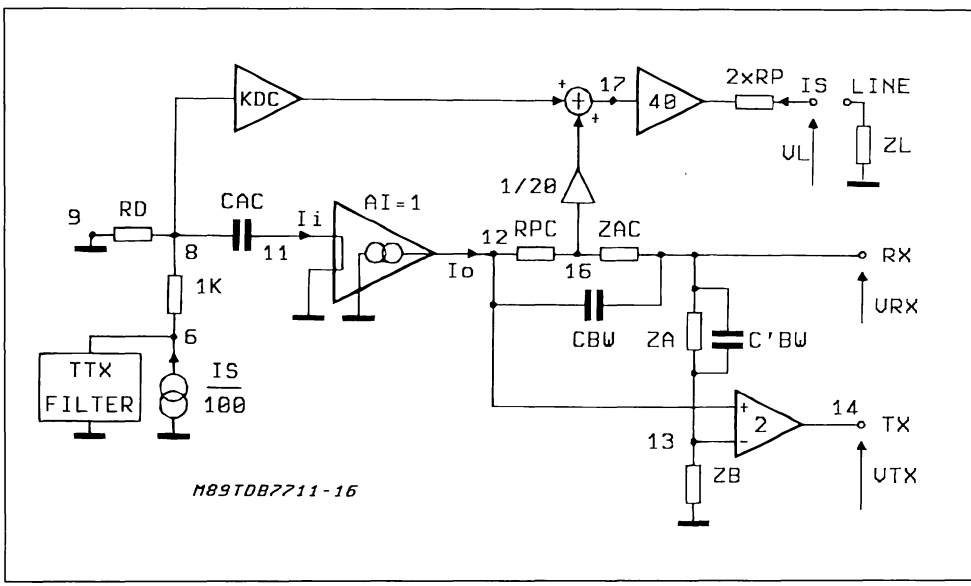
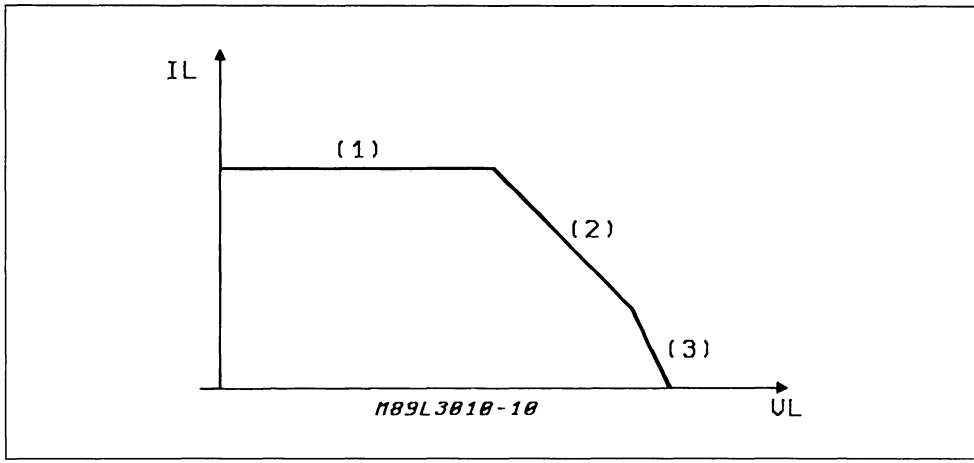


Figure 5.2 : TDB7722/TDB7711 DC Characteristic.



The RD and KDC values depends on the working point on DC characteristic, in particular :

RD = infinite ; KDC = 5/4 for region 1

RD = RDC ; KDC = 5/4 for region 2

RD = RDC ; KDC = 0 for region 3

CAC is a large capacitor (typ. 47µF) used to split AC and DC components of line current.

CBW and C'BW are small capacitors (typ. 270pF and 120pF) used to guarantee loop stability and good THL performances.

CAC, CBW and C'BW values are chosen in order to have a neglectible effect on speech band signals, therefore supposing CBW equivalent to an open circuit and CAC to a short circuit the following relationships can be easily obtained from the circuit diagram of fig. 5.1. Also the TTX filter influence in speech band is neglected ; the TTX filter impedance is supposed to be very high in speech band and zero at the TTX frequency.

5.1. SLIC IMPEDANCE AT LINE TERMINATIONS :

$$ZML = \left.\frac{V_L}{I_S}\right|_{VRX=0} = (ZAC/50) + 2 \times RP$$

5.2. RECEIVING GAIN :

$$G_R = \frac{V_L}{V_{RX}} = 2 \times \frac{ZL}{ZL+ZML}$$

therefore if ZL = ZML

$G_R = 1$

5.3. SENDING GAIN

$$G_S = \left.\frac{V_{TX}}{V_L}\right|_{VRX=0} = \frac{ZAC + RPC}{ZAC + (100 \times RP)}$$

therefore if RPC = 100 x RP

$G_S = 1$

5.4. TRANS-HYBRID LOSS

$$THL = \frac{V_{TX}}{V_{RX}} = 2 \times \left(\frac{ZL + 2 \times RP - (RPC/50)}{ZL + ZML} \frac{ZB}{ZA + ZB}\right)$$

therefore if RPC = 100 x RP and ZA/ZB = ZML/ZL

THL = 0

If you need a more careful evaluation of AC performances you can include also the effect of CBW, CAC and TTX filter in the above relations or you can simulate the system behavior with SPICE or other circuit simulators (see example at par. 6).

It should be noted that even if the CBW capacitor is relatively small it could have some effect on the return loss performances (anyway always within the specs.) at the higer frequencies. In order to obtain better return loss performances the CBW effect should be considered when the ZAC impedance is selected.

If for example the German return loss impedance (220Ω +(820Ω//115nF)) is requested supposing RP = 30Ω it should be : ZAC = 8K + (41K//2.3nF) as described in par. 5.1. If you look at the structure shown in fig. 5.1. you can see that CBW can be considered in parallel with ZAC therefore better return loss performances can be obtained considering the effect of CBW on ZAC. If you consider again the case of German network it shoul be : ZAC = 8K + (41K//2.0nF) supposing CBW about 300pF.

6. ONE EXAMPLE OF SPICE SIMULATION WITH L3000/L3090 SLIC KIT

Figure 6.1 : Circuit Diagram for L3000/L3090 SLIC KIT Spice Simulation.

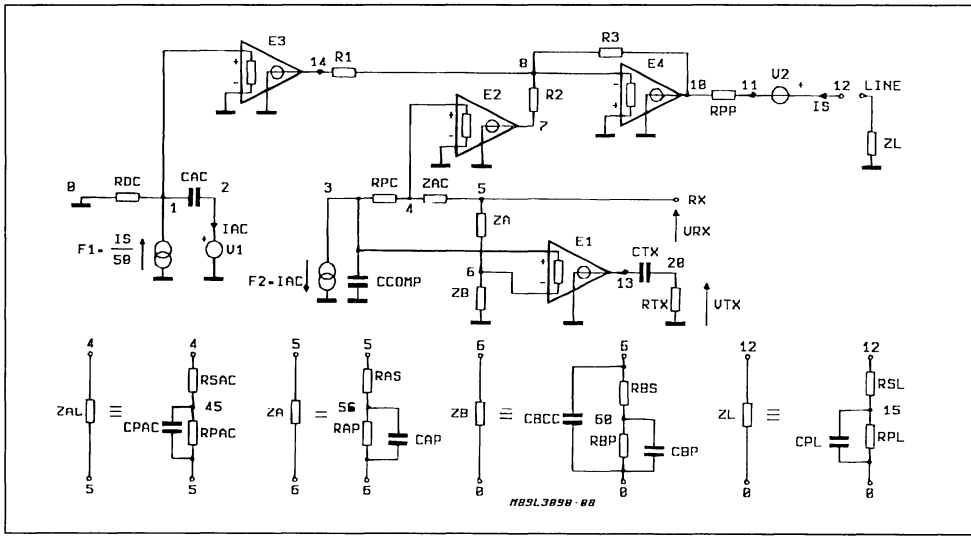
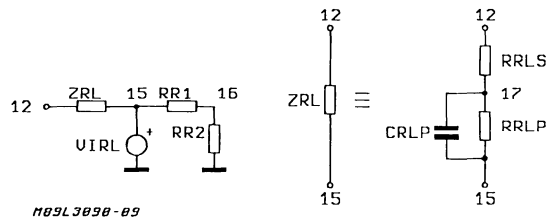
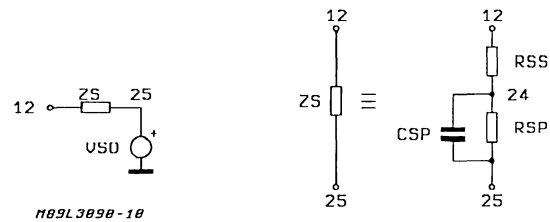


Figure 6.2 : Network for RL Evaluation ; ZRL = Return Loss Test Impedance.



$$RL = 20\log_{10}\left|\frac{ZRL - ZML}{ZRL + ZML}\right| = 20\log_{10}\left|\frac{2 \times V(12,16)}{VIRL}\right|$$

Figure 6.3 : Network for TX Gain Evaluation with Sending Generator Series Impedance Equal to ZS.



$$G_S = 2 \times VTX/VSO$$

SPICE INPUT FILE FOR L3000/L3090 SLIC KIT SIMULATION

```
L3090 AC ANALYSIS

********** CIRCUIT CONFIGURATION USED **********
*  PROT. RES. 2 x 50Ω → RPP = 100Ω ; RPC = 2.5 KΩ          *
*  FEEDING RES. 2 x 200Ω → RDC = 300Ω                      *
*  AC LINE IMPEDANCE 600Ω → RZAC = 12.5 KΩ                 *
*  (SAME CONFIGURATION OF L3000/L3090 TEST CIRCUIT)         *
************************************************************

********** EXTERNAL COMPONENTS **********

RPC 3 4 2.5K
RSAC 4 45.5K
RPAC 45 5 12K
*CPAC 45 5 1P
RAS 5 56 6K
RAP 56 6 6K
*CAP 56 6 1P
RBS 6 60 6K
RBP 60 0 6K
*CBP 60 0 1P
CBCC 6 0 470P
RPP 10 11 100
RTX 20 0 1MEG

CAC 1 2 47U
CCOMP 3 0 390P
CTX 13 20 10U

********** END EXT. COMPONENTS **********

********** MODEL COMPONENTS **********
R1 14 8 1K
R2 7 8 1K
R3 8 10 40K
R4 8 0 10MEG

E1 13 0 3 6 2
E2 7 0 4 0 + . 05
E3 14 0 1 0 – 1.25
E4 10 0 8 0 – 1MEG

V1 2 0
V2 12 11

F1 0 1 V2 .02
F2 3 0 V1 1

.AC LIN 40 100 4K
*.AC DEC 10 10 20K
.WIDTH IN = 80 OUT = 80
```

```
****** INSERT ONLY ONE OF THE FOLLOWING BLOCKS DEPENDING ******
****** ON THE DC CHARACTERISTIC REGION                    ******

****** LIM. CURRENT REGION ******
**** RDC 1 0 10MEG
****** END LIM. REGION **************

****** RES. FEED REGION ***********
**** RDC 1 0 300
****** END RES. REGION *************

****** INSERT ONLY ONE OF THE FOLLOWING BLOCKS DEPENDING ******
****** ON WHICH ANALYSIS YOU WANT                         ******

***** TX GAIN EVALUATION VTX/VL WITH VRX = 0 *****
*VRX 5 0 DC 0
*VL 12 0 AC
*.PRINT AC VDB(20)  VP(20)
*.PLOT AC VDB(20)  VP(20)
*.STORE AC VDB(20)  VP(20)
***** END TX GAIN ****************************************

** TX GAIN EVALUATION 2VTX/VSO WITH VRX= 0 **
** (SERIES IMP. OF SENDING GENERATOR = ZS)
*VRX 5 0 DC 0
*VSO 25 0 AC 2
*RSS 24 12 300
*RSP 24 25 300
**CSP 24 25 1P
*.PRINT AC VDB(20)  VP(20)
*.PLOT AC VDB(20)  VP(20)
*.STORE AC VDB(20)  VP(20)
***** END TX GAIN ****************************************

** RX GAIN EVALUATION VL/VRX ***********************
*RSL 12 15 300
*RPL 15 0 300
**CPL 15 0 1P
*VRX 5 0 AC
*.PRINT AC VDB(12)  VP(12)
*.PLOT AC VDB(12)  VP(12)
*.STORE AC VDB(12)  VP(12)
***** END RX GAIN ****************************************

** THL EVALUATION VTX/VRX ****************************
*RSL 12 15 300
*RPL 15 0 300
**CPL 15 0 1P
*VRX 5 0 AC
*.PRINT AC VDB(20)  VP(20)
*.PLOT AC VDB(20)  VP(20)
*.STORE AC VDB(20)  VP(20)
***** END THL EVALUATION *********************************
```

```
*** RETURN LOSS EVALUATION *************************
*VRX 5 0 DC 0
*VIRL 15 0 AC 2
*RCS 12 17 300
*RCP 17 15 300
**.CCP 17 15 1P
*RR1 15 16 1K
*RR2 16 0 1K
*.PRINT AC VDB(12.16)
*.PLOT AC VDB(12.16)
*.STORE AC VDB(12.16)
***** END RETURN LOSS EVALUATION ******************

*** INPUT IMPEDANCE EVAL. AT LINE TERMINALS ***
*VRX 5 0 DC 0
*IL 0 12 AC
*.PRINT AC VM(12)   VP(12)
*.PLOT AC VM(12)   VP(12)
*.STORE AC VM(12)   VP(12)
***** END INP. IMPED. EVALUATION **********************


.END
```

EMI TEST EVALUATION WITH L3000/L3090 SLIC KIT

PRELIMINARY RESULTS

INTRODUCTION

EMI test were performed on SGS-THOMSON L3000/L3090 SLIC KIT using the same test circuit described in FTZ specs (12 TR1 Teil 21).

In order to cut high frequencies two capacitors (C_{RF}) were connected respectively between TIP and GND and RING and GND (no coils needed!).

The measurements were performed in the range of 10KHz to 8MHz giving good results. The same behavior is expected for higher frequencies with a proper layout and good H.F. filtering capacitors.

Laboratory activity is going on about this subject ; further informations will be available in the next months.

MEASUREMENTS RESULTS

Referring to the test procedure described in the FTZ specs an amplitude modulated signal (m = 0.8 ; f = 1kHz) was applied at TIP/RING termination ; the amplitude of this signal was 1.5Vrms from 10KHz to 100KHz and 3Vrms from 100KHz to 8MHz.

The signal at TX output was measured after a psophometric filter ; this signal was always below 1mVrms as required (see fig. 1). In fig. 1 is also represented the H.F. rejection of the device itself (without filtering capacitors C_{RF}). The good behavior of the device itself at relatively low frequencies allow us to use smaller values for the C_{RF} capacitor reducing in this way also their influence in speech band.

AC PERFORMANCES

In fig. 2 is shown the SLIC circuit diagram with the two CRF capacitor. Of course these capacitors should produce some effects on the AC performances of the device. Anyway, thanks to the architecture of the L3000/L3090 SLIC KIT these effects can be very well compensated modifying properly the SLIC output impedance and the position of the compensation capacitor for the SLIC loop stability. In fig. 2 these modifications are already present. External components are selected in order to satisfy German requirements. Fig. 3 to 6 shown the AC performances measured with the SLIC configuration represented in fig. 2.

CONCLUSIONS

Using L3000/L3090 SLIC KIT it is possible to satisfy the FTZ requirements as described above simply using two 18nF capacitors, no coils are needed !

The eventual AC performances distortions can be compensated acting on the external components (see fig. 3 to 6).

Figure 1 : L3000/L3090 EMI Measurements.

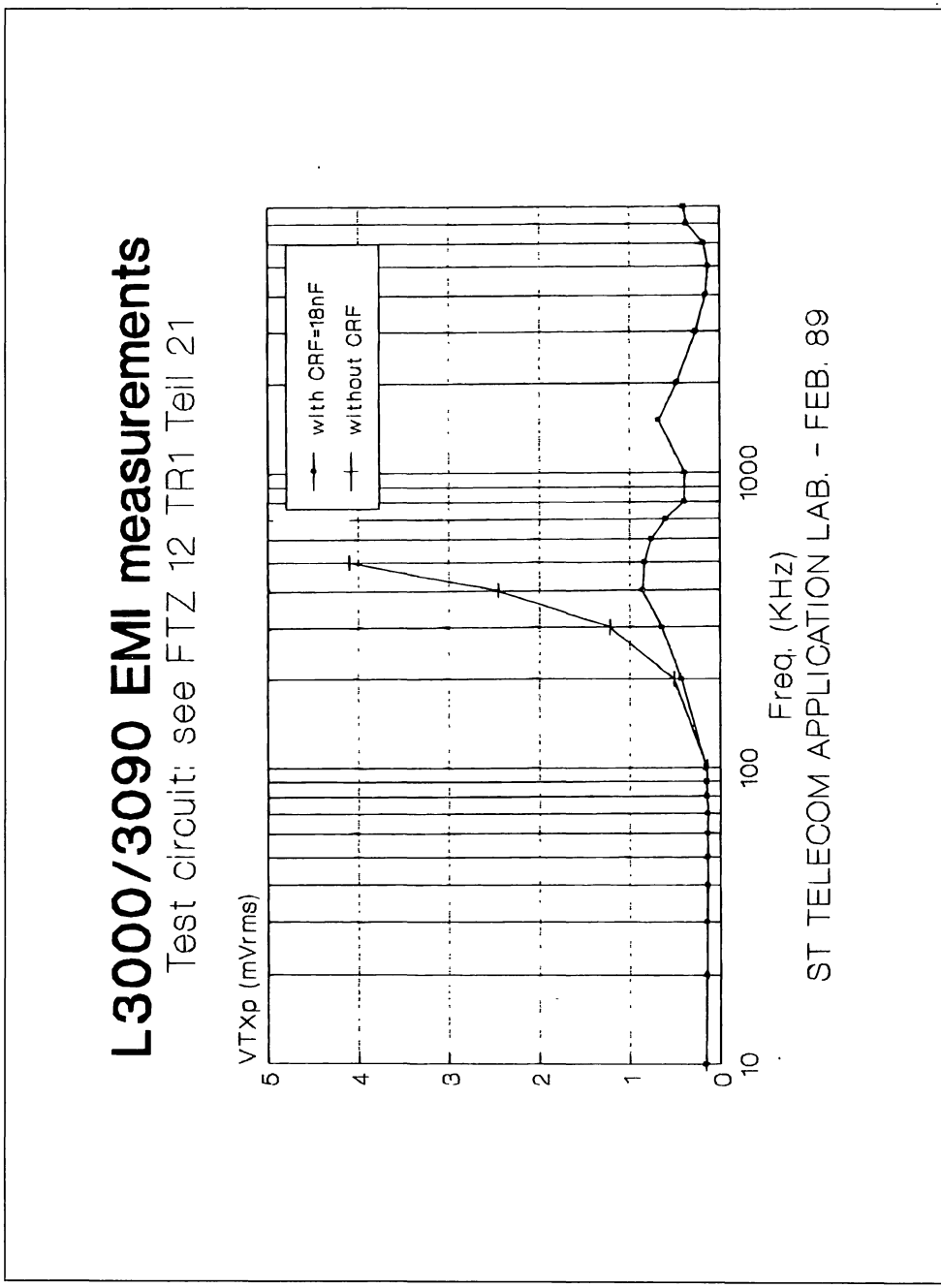


Figure 2 : L3000/L3090 Circuit Arrangement for EMI Rejection.

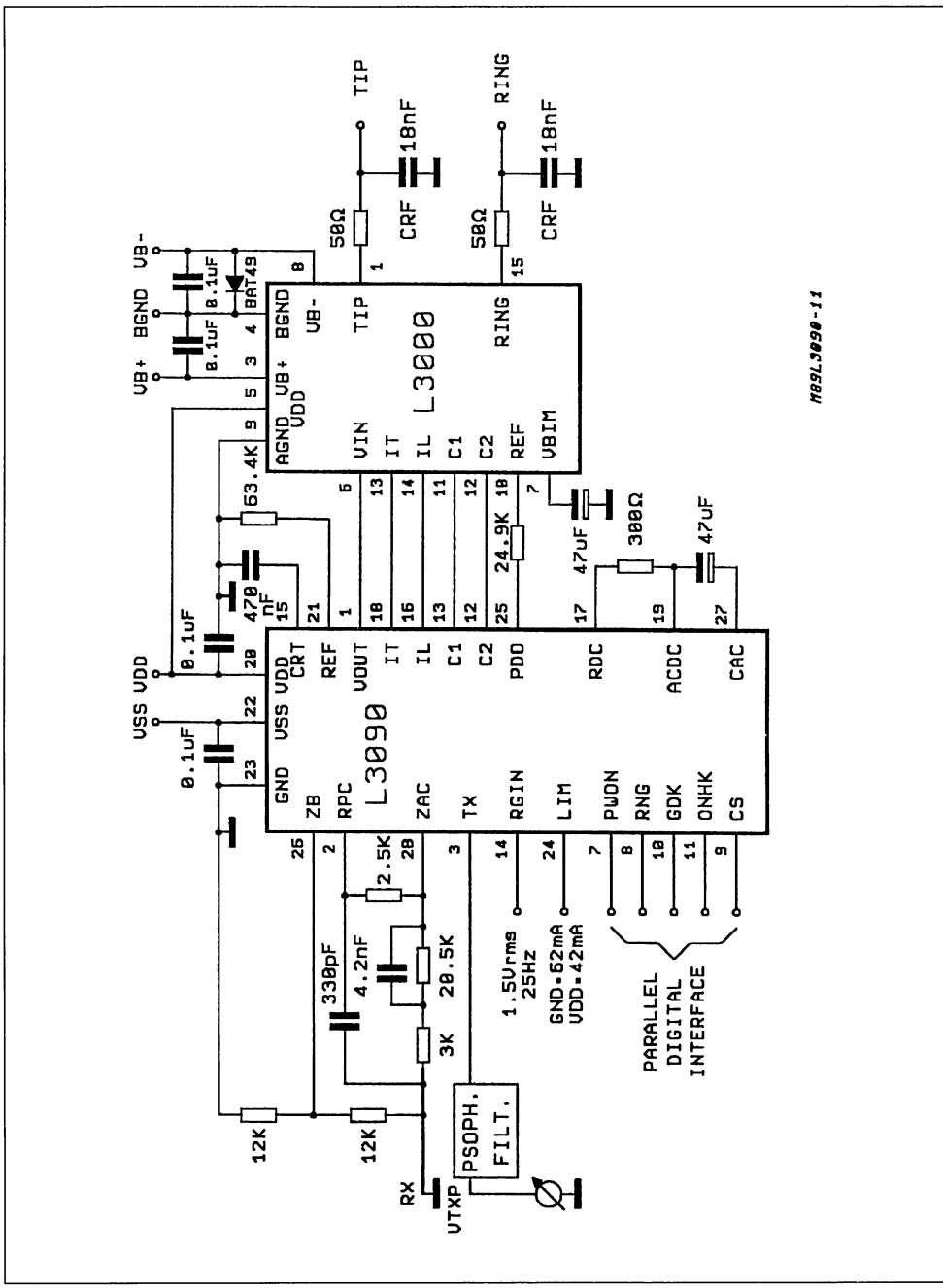
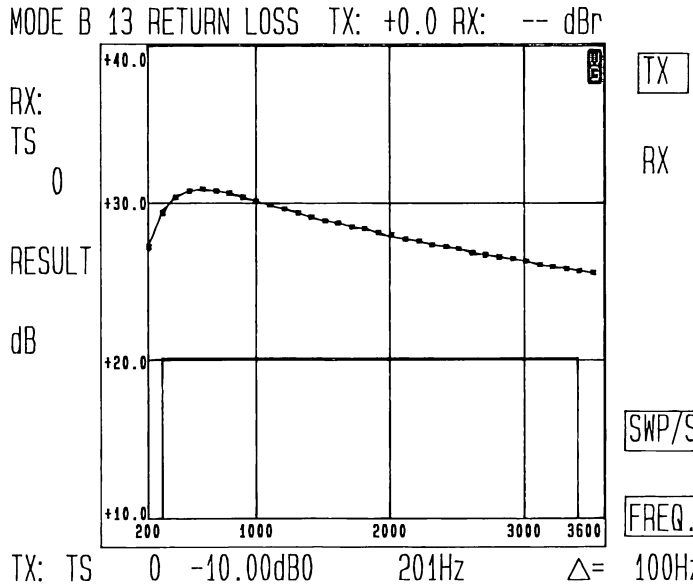
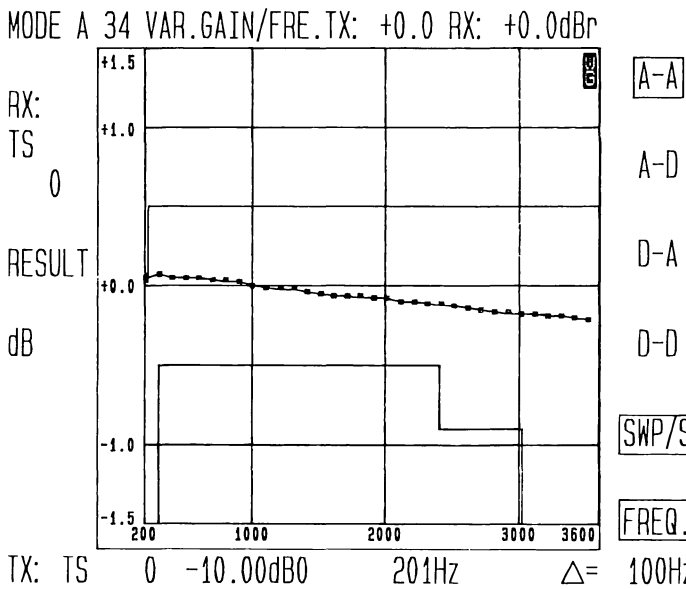


Figure 3 : Return Loss Performances.



W & G PCM-4 RETURN LOSS B 13			20. FEB. 89 12 : 14 TX TX : + 0.0dBr RX : -- dBr
PRINT MAN RESULTS			
TX-TSLOT 0	RX-TSLOT 0	Level – 10.00dB0	
Freq./Hz	**Result/dB**	**Freq./Hz**	**Result/dB**
201	+ 27.17	301	+ 29.35
402	+ 30.35	502	+ 30.79
602	+ 30.89	703	+ 30.79
803	+ 30.61	903	+ 30.38
1004	+ 30.14	1104	+ 29.88
1205	+ 29.64	1305	+ 29.39
1405	+ 29.15	1506	+ 28.92
1606	+ 28.70	1706	+ 28.50
1807	+ 28.30	1907	+ 28.11
2008	+ 27.92	2108	+ 27.73
2208	+ 27.56	2309	+ 27.39
2409	+ 27.22	2509	+ 27.06
2610	+ 26.90	2710	+ 26.74
2811	+ 26.59	2911	+ 26.44
3011	+ 26.29	3112	+ 26.14
3212	+ 26.00	3312	+ 25.85
3413	+ 25.71	3513	+ 25.56

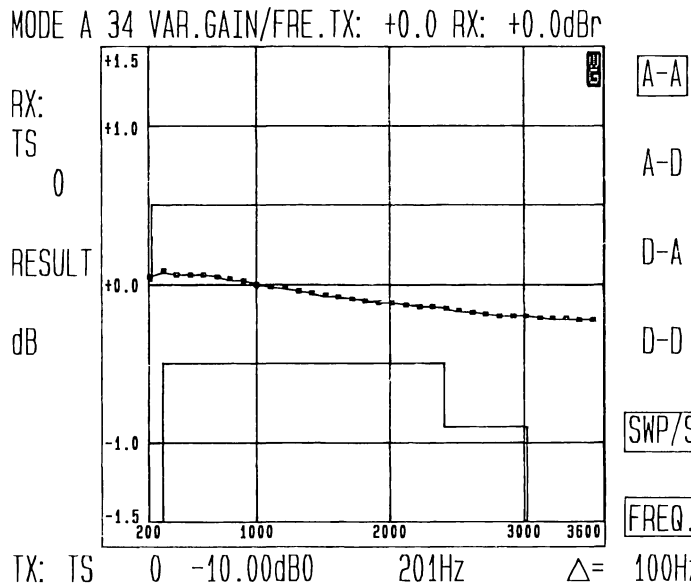
Figure 4 : Tx Gain Flatness.



W & G PCM-4			20. FEB. 89 12 : 28
VAR. OF GAIN WITH FREQUENCY		A-A	4-wire
A 34		TX : + 0.0dBr	RX : + 0.0dBr
	PRINT MAN RESULTS	Ri : cplx	Re : 30kΩ

TX-TSLOT	RX-TSLOT		
0	0	Level – 10.00dB0	
Freq./Hz	**Result/dB**	**Freq./Hz**	**Result/dB**
201	+ 0.05	301	+ 0.07
402	+ 0.05	502	+ 0.05
602	+ 0.05	703	+ 0.04
803	+ 0.03	903	+ 0.02
1004	+ 0.00	1104	– 0.01
1205	– 0.02	1305	– 0.02
1405	– 0.04	1506	– 0.05
1606	– 0.06	1706	– 0.06
1807	– 0.07	1907	– 0.08
2008	– 0.08	2108	– 0.10
2208	– 0.10	2309	– 0.11
2409	– 0.12	2509	– 0.13
2610	– 0.14	2710	– 0.15
2811	– 0.16	2911	– 0.17
3011	– 0.18	3112	– 0.18
3212	– 0.19	3312	– 0.19
3413	– 0.20	3513	– 0.21

Figure 5 : Rx Gain Flatness.

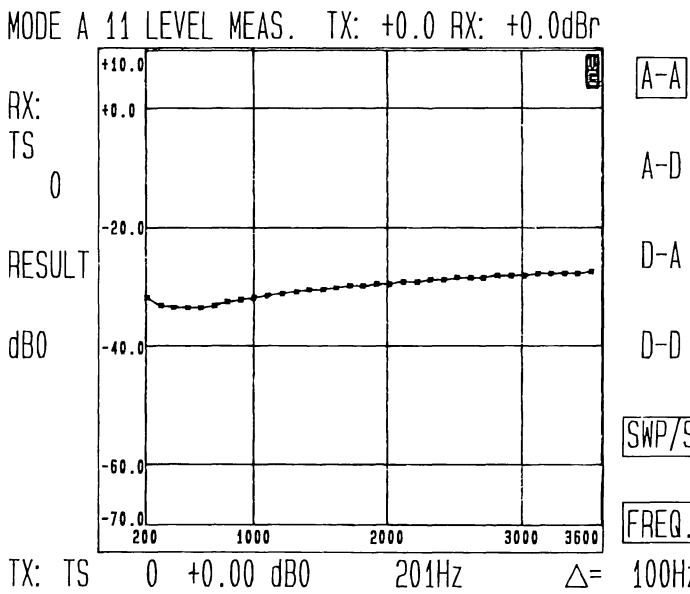


W & G PCM-4 VAR. OF GAIN WITH FREQUENCY A 34	PRINT MAN RESULTS	A-A TX : + 0.0dBr Ri : 600Ω	20. FEB. 89 12 : 34 4-wire RX : + 0.0dBr Re : cplx

TX-TSLOT	RX-TSLOT	Level – 10.00dB0	
0	0		

Freq./Hz	Result/dB	Freq./Hz	Result/dB
201	+ 0.05	301	+ 0.08
402	+ 0.06	502	+ 0.06
602	+ 0.06	703	+ 0.05
803	+ 0.03	903	+ 0.02
1004	+ 0.00	1104	– 0.01
1205	– 0.02	1305	– 0.04
1405	– 0.05	1506	– 0.07
1606	– 0.08	1706	– 0.09
1807	– 0.10	1907	– 0.11
2008	– 0.11	2108	– 0.13
2208	– 0.14	2309	– 0.14
2409	– 0.15	2509	– 0.17
2610	– 0.18	2710	– 0.19
2811	– 0.20	2911	– 0.20
3011	– 0.20	3112	– 0.21
3212	– 0.22	3312	– 0.22
3413	– 0.23	3513	– 0.23

Figure 6 : THL Performances.



W & G PCM-4			20. FEB. 89 12 : 42
LEVEL MEASUREMENT		A-A	4-wire
A 11		TX : + 0.0dBr	RX : + 0.0dBr
	PRINT MAN RESULTS	Ri : 600Ω	Re : 30kΩ

TX-TSLOT	RX-TSLOT	
0	0	Level + 0.00dB0

Freq./Hz	Result/dB0	Freq./Hz	Result/dB0
201	– 31.62	301	– 33.13
402	– 33.61	502	– 33.57
602	– 33.31	703	– 32.96
803	– 32.57	903	– 32.18
1004	– 31.82	1104	– 31.46
1205	– 31.13	1305	– 30.83
1405	– 30.54	1506	– 30.29
1606	– 30.05	1706	– 29.84
1807	– 29.63	1907	– 29.44
2008	– 29.27	2108	– 29.10
2208	– 28.95	2309	– 28.80
2409	– 28.67	2509	– 28.54
2610	– 28.42	2710	– 28.30
2811	– 28.19	2911	– 28.08
3011	– 27.98	3112	– 27.87
3212	– 27.78	3312	– 27.68
3413	– 27.59	3513	– 27.50

SGS-THOMSON SLIC KITS AND COMBO II

BY W. ROSSI

1. INTRODUCTION

One of the main feature of COMBO II is the possibility to program TX and RX gains and to perform the two to four wire conversion (echo cancellation).

In particular the echo cancellation feature allows you to save external components in the SLIC circuitry.

In the following tables you can find different values for COMBOII hybrid balance filter in order to satisfy different administrations requirements.

Three SLIC KITS are analyzed :

L3000/L3030
L3000/L3090/91
TDB7722/TDB7711

for each administration also the external components are specified.

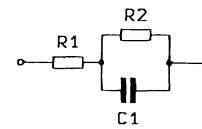
If you need more specific informations the complete Application Note is available, ask for it to our sales office.

In the complete Application Note you can find all the details for each country in particular :

- Echo measurements
- Combo II simulation software results
- Bench measurements with PCM-4 Wandel & Goltermann

2. L3000/L3030 + COMBO II APPLICATION

Test network :



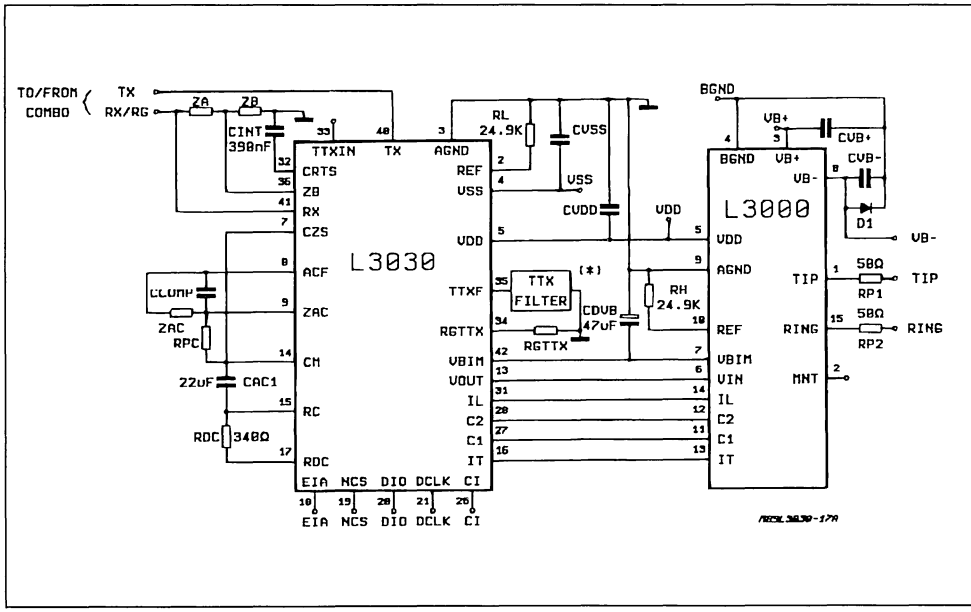
Here below you can find the SLIC external components and the COMBO II programming coefficient for Germany, Austria and Swisse followed by the application diagram.

TX and RX gain are chosen in order to have :

0dBm0 ⇔ 0dBm 800 ohm (TXgain reg. = BF ; RXgain reg. = AE)

	Administration	R. L. Test Netw.	SLIC Ext. Comp.	THL. Test Netw.	COMBOII Hybal Coeff.
1.	Germany/Austria/ Swisse	R1 = 220Ω R2 = 820Ω C1 = 115nF	ZAC = (1) RPC = 60Ω ZA = 2K ZB = 6.19K CCOMP = 10nF (1) : 160Ω + (820Ω//115nF)	R1 = 220Ω R2 = 820Ω C1 = 115nF	EC ; 32 ; C4

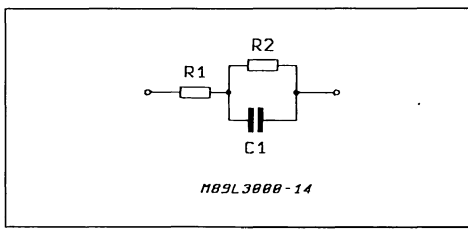
Figure 1 : L3000+L3030 Appl. Diagram.



(*) All measurements were made substituting the TTX filter with 1K resistor and RGTTX with 10K. The 1K resistor is equivalent to TTX filter for speech band signals.

3. L3000/L3090 + COMBO II APPLICATION

Test network :



Here below you can find the SLIC external components and the COMBO II programming coefficient for different countries, in the next page is shown the application diagram.

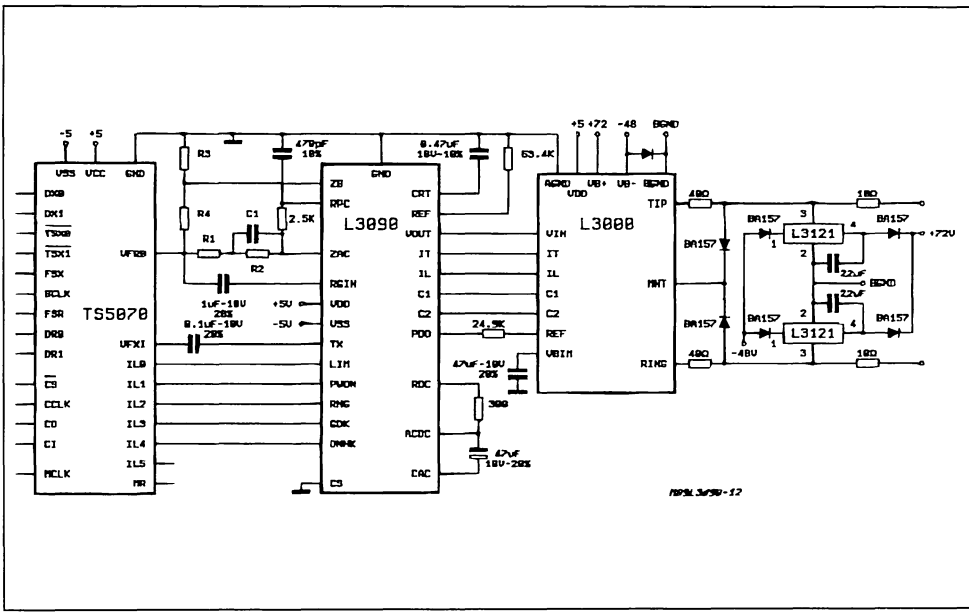
TX and RX gain are chosen in order to have :

0dBm0 ⇔ 0dBm 600 ohm (TXgain reg. = BF ; RXgain reg. = AE)

	Administration	R. L. Test Netw.	SLIC Ext. Comp.	THL. Test Netw.	COMBOII Hybal Coeff.
1.	Belgium Priv.	R1 = 150Ω R2 = 830Ω C1 = 72nF	R1 = 1.25K R2 = 20.75K R3 = 3.3K R4 = 15K C1 = 2.9nF	R1 = 150Ω R2 = 830Ω C1 = 72nF	E6 ; 12 ; AA
				R1 = 600Ω R2 = 0 ; C1 = 0	F4 ; 00 ; 03
2.	Korea/France Pub Portugal Priv./ USA Priv.	R1 = 600Ω R2 = 0 ; C1 = 0	R1 = 0 R2 = 12.5K R3 = 5.1K R4 = 15K C1 = 0	R1 = 600Ω R2 = 0 ; C1 = 0	EC ; 01 ; 48

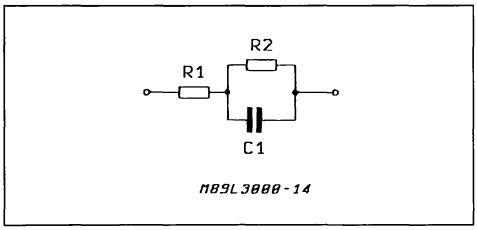
	Administration	R. L. Test Netw.	SLIC Ext. Comp.	THL. Test Netw.	COMBOII Hybal Coeff.
3.	Finland	R1 = 270Ω R2 = 910Ω C1 = 120nF	R1 = 4.25K R2 = 22.75K R3 = 5.1K R4 = 15K C1 = 4.8nF	R1 = 270Ω R2 = 1200Ω C1 = 120nF	E9 ; 23 ; 39
				R1 = 390Ω R2 = 620Ω C1 = 100nF	F2 ; 11 ; AF
4.	Germany/Austria/ Swisse	R1 = 220Ω R2 = 820Ω C1 = 115nF	R1 = 3K R2 = 20.5K R3 = 5.1K R4 = 15K C1 = 4.7nF	R1 = 220Ω R2 = 820Ω C1 = 115nF	EE ; 12 ; AA
5.	Italy Priv.	R1 = 180Ω R2 = 630Ω C1 = 60nF	R1 = 2K R2 = 15.75K R3 = 5.1K R4 = 15K C1 = 2.4nF	R1 = 0 R2 = 750Ω C1 = 18nF	F1 ; 01 ; 6D
6.	U. K. Priv.	R1 = 370Ω R2 = 620Ω C1 = 310nF	R1 = 6.75K R2 = 15.5K R3 = 5.1K R4 = 15K C1 = 12.4nF	R1 = 370Ω R2 = 620Ω C1 = 310nF	EE ; 01 ; CC
				R1 = 300Ω R2 = 1000Ω C1 = 220nF	E8 ; 24 ; 9A

Figure 2 : L3000/L3090 + COMBOII.



4. TDB7722/TDB7711 + COMBO II APPLICATION

Test network :



Here below you can find the SLIC external components and the COMBO II programming coefficient for different countries, in the next page is shown the application diagram.

TX and RX gain are chosen in order to have :

0dBm0 ⇔ 0dBm 600 ohm (TXgain reg. = BF ; RXgain reg. = AE)

	Administration	R. L. Test Netw.	SLIC Ext. Comp. (*)	THL. Test Netw.	COMBOII Hybal Coeff.
1.	Finland	R1 = 270Ω R2 = 910Ω C1 = 120nF	ZAC = (1) RPC = 3K ZA = 91K ZB = 30K R_p = 30Ω CBW = 270pF (1) : 10.5K + (45.5K//2.2nF)	R1 = 270Ω R2 = 1200Ω C1 = 120nF	E9 ; 34 ; BF
				R1 = 390Ω R2 = 620Ω C1 = 100nF	B3 ; 00 ; 8F
2.	France Publ./ Korea/USA Priv./ Portugal Priv.	R1 = 600Ω R2 = 0 C1 = 0	ZAC = 27K RPC = 3K ZA = 91K ZB = 30K R_p = 30Ω CBW = 270pF	R1 = 600Ω R2 = 0 C1 = 0	EE ; 24 ; 0C
3.	Germany Publ.	R1 = 220Ω R2 = 820Ω C1 = 115nF	ZAC = (2) RPC = 3K ZA = 91K ZB = 30K R_p = 30Ω CBW = 270pF (2) : 8K + (41K//2.0nF)	R1 = 220Ω R2 = 820Ω C1 = 120nF	EE ; 00 ; 8C
4.	Italy Publ.	R1 = 600Ω R2 = 0 C1 = 0	ZAC = 27K RPC = 3K ZA = 91K ZB = 39K R_p = 30Ω CBW = 270pF	R1 = 0 R2 = 1100Ω C1 = 33nF	E3 ; 23 ; C0

(*) C'BW = 0

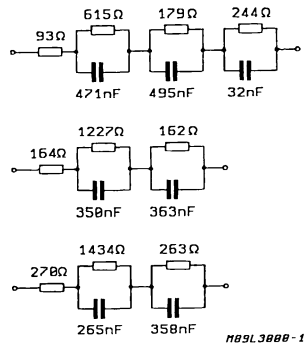
	Administration	R. L. Test Netw.	SLIC Ext. Comp. (*)	THL. Test Netw.	COMBOII Hybal Coeff.
5.	U. K. Public	R1 = 370Ω R2 = 620Ω C1 = 310Ω	ZAC = (1) RPC = 3K ZA = 80.5K ZB = 30K R_p = 30Ω CBW = 270pF (1) : 15.5K + (31K//6.2nF)	1. Short Lines	EF ; 25 ; DF
				2. Long Lines (s. g)	EE ; 3C ; 36
				3. Long Lines (l. g) (see note 1)	E3 ; 36 ; 31
6.	U. S. Public	R1 = 900Ω R2 = inf. C1 = 2.16µF	ZAC = (2) RPC = 8K ZA = 91K ZB = 51K (loaded) ZB = 10K (not loaded) R_p = 80Ω CBW = 150pF (2) : 37K + (47K//47nF)	1. Loaded Lines	E9 ; 50 ; DF
				2. Not Loaded l. (see note 2)	E1 ; 40 ; A8

Note : 1. U.K THL TEST NETWORKS :

1. Short lines

2. Long lines (small gauge)

3. Long lines (large gauge)



Note : 2. U.S. THL TEST NETWORKS :

1. Loaded line

2. Not Loaded line

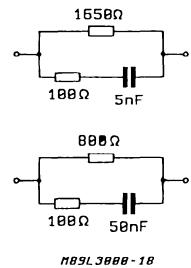
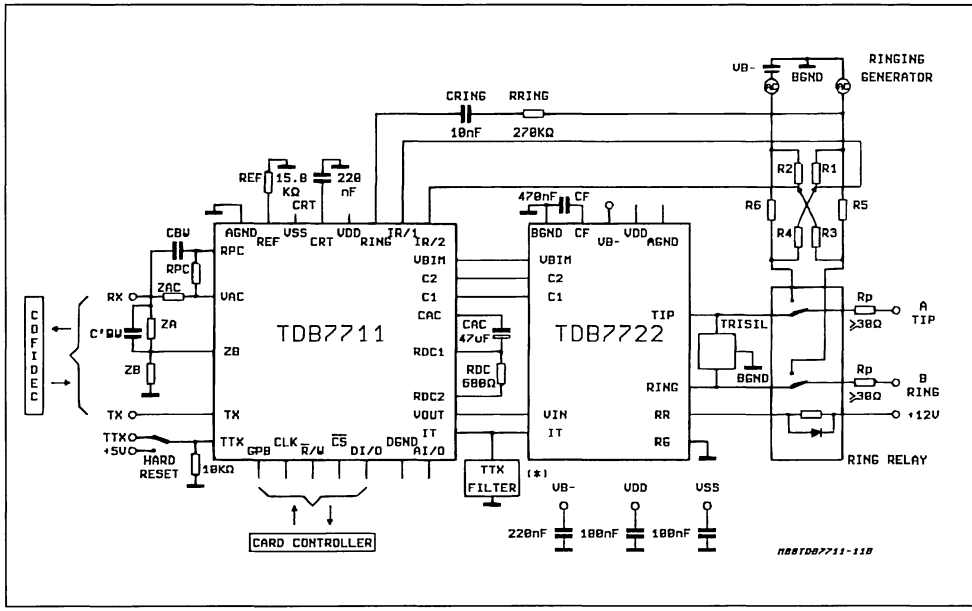


Figure 3 : TDB7722+TDB7711 Appl. Diagram.



(*) All measurements were made without TTX filter being such filter equivalent to an open circuit for speech band signals.

SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE

SLIC EVALUATION KIT

This kit is provided in order to give the possibility to make a quick evaluation of all the SGS-THOMSON Microelectronics SLIC KITs.

It consists of one CONTROL BOARD (code : SLIC-CTL/1) and different SLIC modules.

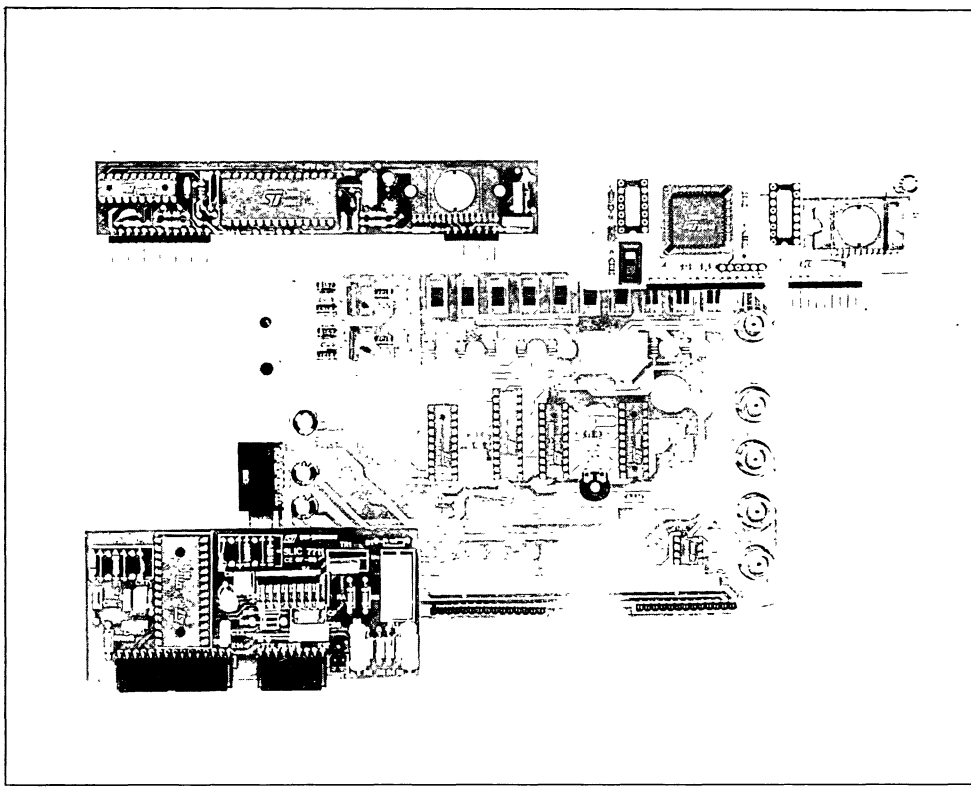
The main purpose of the CONTROL BOARD is to provide an easy read/write of the SLICs digital interface that except for L3090/91 are all serial. Data are written by means of eight switches and read by means of five LEDs ; two additional LEDs are provided in order to read the L3090/91 parallel interface. In addition it provides an easy connection for TIP/RING and TX/RX terminations of diferent SLIC MODULES that can be plugged in proper connectors provided on the board. This board, being very simple, allows to obtain good results also for very accurate measurements (like noise or distortion).

Concerning the SLIC MODULES the following are today available :

L3000/L3030	(code : SLIC 3030-1)
L3000/L3090/91	(code : SLIC 3090-3) (*)
TDB7722/TDB7711	(code : SLIC 7711) (*)

(*) the same used with the "SLICOMBO" demoboard.

Figure 1 : SLIC Evaluation KIT.



SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE

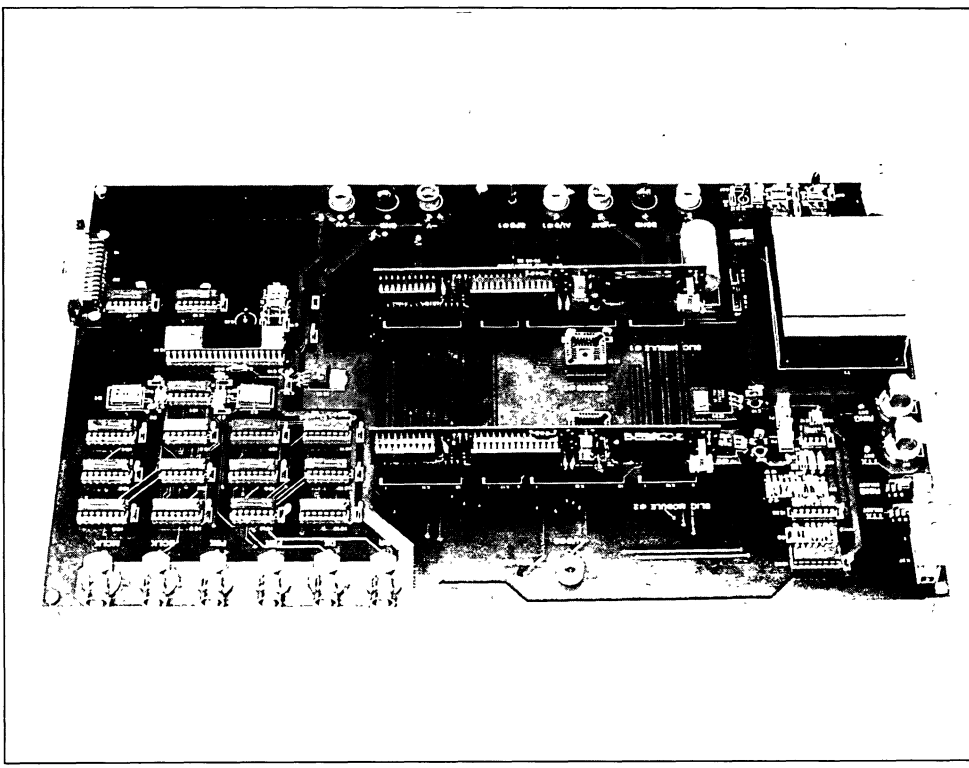
SLICOMBO LINE CARD DEMONSTRATION BOARD

SLICOMBO is a conversational demonstration board for the subscriber line card oriented circuits developped by SGS-THOMSON Microelectronics. It includes two complete transmission modules, each of them made of a programmable codec/filter COMBOII associated with a full silicon SLIC to achieve the "BORSCH" function (**B**attery feed, **O**vervoltage protection, **R**inging, **S**ignalling, **C**odec/filter, **H**ybrid 2-wire/4-wire conversion).

The 2-wire interface of each SLIC can be connected to a telephone set or to an appropriate test equipment. The PCM interface of the 2 COMBOs can also be connected to a PCM test equipment, or to the same PCM highway, thus allowing a real phone conversation between the 2 telephone sets through the 2 SLICs and the 2 COMBOs.

As SGS-THOMSON Microelectronics provides a wide range of SLICs, they are implemented on interchangeable modules ; 2 modules are available : one version is for the central office oriented SLIC TDB7711/7722, and one version for the PABX oriented SLIC L3090/L3000. SLICOMBO can operate either with 2 TDB7711 or with 2 L3090 SLIC modules.

The user interface with the board is performed by an IBM Personnal Computer or true compatible. An interactive software inputs the commands from the user and displays the results on the screen ; a multimenus approach is used by the software to make easy the programming of the SLICOMBO board.



RELIABILITY REPORT : ETC5040 FILTER, ETC5057 AND ETC5067 COMBOS

1 . RELIABILTY TEST MATRIX

The reliability evaluation program designed for the ETC5040 FILTER, ETC5057 and ETC5067 COMBOS requires the following tests :

- Operating life test
- Temperature cycling

2 . TEXT DESCRIPTION

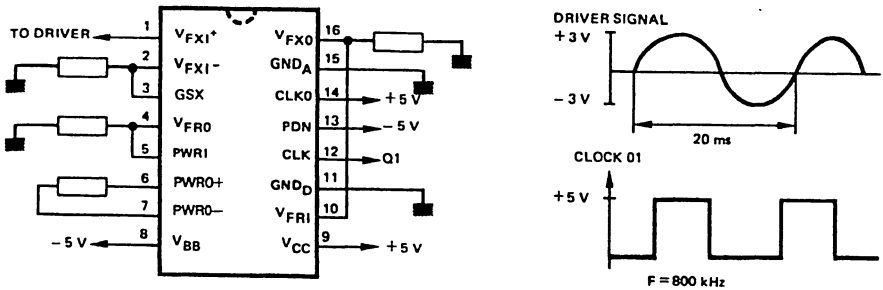
2.1. HIGH TEMPERATURE OPERATING LIFE TEST

The basic test used to evaluate device reliability is high temperature operating life test.

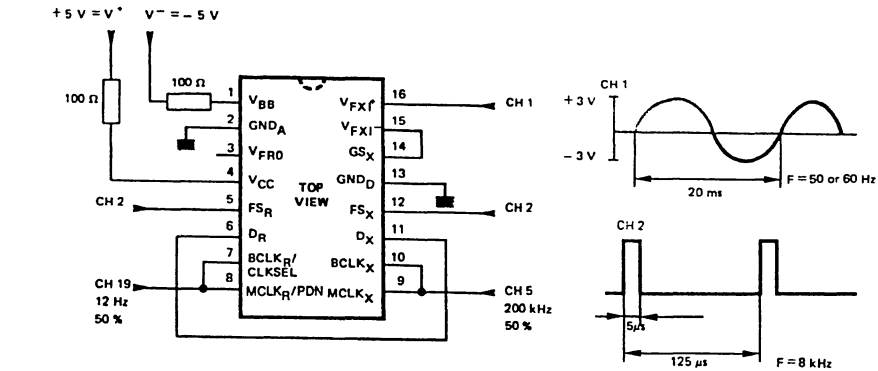
Failure mecanisms from the random area of the reliability life are accelerated at 125 °C.

The devices are loaded on boards and they are dynamically exercised as shown in the following figure.

ETC5040



ETC5057



2.2 OPERATING LIFE TEST FAILURE RATE COMPUTATION

The degradation processes affecting the reliability of electronic devices is such that the failure rate can be described by the Arrhenius model.

$$\lambda(T) = K \exp \frac{-E_A}{kT} \quad (2)$$

E_A : Activation energie (e)

k : Boltzmann's constant (8.63×10^{-5} eV K^{-1})

T : Absolute temperature (K)

K : Constant

At a given temperature, the failure rat is defined as :

$$\lambda(T) = \frac{N}{N_D \cdot T_H} \quad (3)$$

N : Number of failures

N_D : Number of devices tested

T_H : Number of test hours

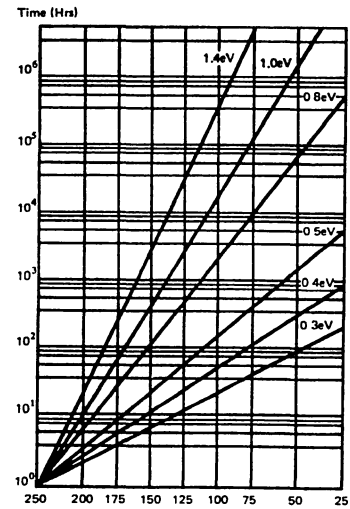
To determine the corresponding failure at other temperatures, an acceleration factor given by the Arrhenius Relationship is used :

$$F(T1, T2) = \frac{\lambda(T1)}{\lambda(T2)} \left[\frac{-E_A}{K} \left(\frac{1}{T1} - \frac{1}{T2} \right) \right] \quad (4)$$

T_1 : Junction temperature during test (K)

T_2 : Desired junciton temperature (K)

Shows the acceleration factor for different thermal activation energies (Arrhenius plot)



Arrhenius plot, used for the calculation of the acceleration factor for a given activation energy

Using equation), we can determine the equivalent device-hours EN_D T_H at temperature T_2 for a given activation energy :

$$EN_{D.\,TH}(2) = F(T_1, T_2) \times N_D \cdot T_H(T_1) \quad (5)$$

Thus the equivalent failure rate at temperature T_2 comes as :

$$\lambda(T_2) = \frac{N}{EN_D\, T_H(T_2)} \quad (6)$$

The failure rate of a device showing failures with different activation energies is computed by summing equation (6) on all the activation energies :

$$\lambda (T_2) = E_I \quad \frac{N_i}{(EN_D\ T_H)\ i\ (T_2)} \qquad (7)$$

Where Ni is the number of detects with an activation energy of E_{Ai}.

In this report, failure rate computations on high temperature operating life test data are performed with a confidence level) of 60 %, using the CHI-SQUARE (X^2) distribution as shown in (8).

$$\lambda (T) = \frac{X^2\ (1 - CL),\ (2N + 2)}{2\ N_D \cdot T_H} \qquad (8)$$

CL : Confidence level

For high temperature life test data, CL = 0.6 (60 %)

2.3 TEMPERATURE CYCLING

This test evaluates the devides ability to withstand both extermes of temperatures and rapid changes in temperature.

Temperature cycling is effective in testing thermal expansion compatibility of the various mechanical interfaces present on the device.

Test Conditions :

Ceramic encapsuled devices are submitted to temperature cycling specified by Mil Std 883C Method 1010.1 condition C which states a sequence of 100 cycles (air to air) from 65°C up to 150°C, with a transfer time less than 5 mn.

3 . RELIABILITY TEST RESULTS

ETC 5040
HIGH TEMPERATURE OPERATING LIFE TEST (HTOL)
TEMP. 125'C

Lot	168 H	500 H	1000 H	2000 H	3000 H
A	0/80	0/80	0/80		
B	1/100	0/99	0/99	0/99	0/99
C	0/59	0/59	0/59	0/59	
D	0/70	0/70	0/70	1/70	
E	0/70	0/70	0/70	0/70	
F	0/80	0/80	0/80	0/80	
G	0/80	0/80	1/80		
H	0/80	0/80	0/80		
I	0/80	0/80	1/80	0/79	
J	0/80	0/80	0/80	0/80	
K	1/80	0/79	0/79	0/79	
L	0/80	0/80	0/80		
M	0/80	0/80	0/77		
N	0/80	0/80	0/79		
O	0/80	0/80	0/80		
P	0/80	0/80	0/79		
Q	0/79	0/79	0/79		
R	0/80	0/80	0/80		
S	0/80	0/80	0/80		
T	0/80	0/78	0/78		
U	0/80	0/80	0/75		
V	0/76	0/76	0/76		
W	0/80	0/80	0/80		
X	0/77	0/77	0/77		
Y	0/80	0/80	0/80		
Z	0/80	0/80	0/80		
AA	0/77	0/77	0/77		
AB	0/80	0/80	0/80		
AC	0/80	0/80	0/80		
AD	0/80	0/80	0/80		
AE	0/78	0/78	0/77		
AF	0/80	0/79	1/79		
AG	0/80	0/80	0/80		
AH	0/39	0/39	0/39		
AI	0/40	1/40	0/39		
AJ	0/45	0/45	0/45		
AK	0/80	0/80	0/80		
AL	0/44	0/44	0/44	0/44	
AM	0/45	0/45	0/45	0/44	
AN	0/45	0/45	0/45	0/45	
AP	0/39	0/39	0/39		
AQ	0/50	0/50	0/50		

ETC 5057
HIGH TEMPERATURE OPERATING LIFE TEST
TEMP. 125' C

Lot	168 H	500 H	1000 H	2000 H
A	0/74	1/74	0/73	
B	2/80	0/78	0/78	
C	0/70	0/70	0/70	
D	0/83	0/83	0/83	
E	0/80	0/80	0/80	
F	0/80	0/80	0/80	
G	0/77	0/77	0/77	
H	0/75	0/75	0/75	
I	0/75	0/75	0/75	
J	0/80	0/80	0/80	
K	0/80	0/80	0/80	
L	0/80	0/80	0/80	
M	0/80	0/80	0/80	
N	0/80	0/80	0/80	
O	0/80	0/80	0/80	
P	0/80	0/80	0/80	
Q	0/80	0/80	0/80	
R	0/80	0/80	0/80	
S	0/80	0/80	0/80	
T	0/80	0/80	0/80	
U	0/80	0/80	0/80	
V	0/75	0/75	0/75	
W	0/80	0/78	0/78	
X	0/80	0/80	0/80	
Y	0/80	0/80	0/78	
Z	0/80	0/75	0/75	
AA	0/70	0/70	0/70	
AB	0/79	0/79	0/79	
AC	0/79	0/79	0/79	
AD	0/79	0/79	0/79	
AE	0/79	0/79	0/78	
AF	0/80	0/79	0/79	
AG	0/80	0/80	0/80	
AH	0/79	0/79	0/79	
AI	0/78	0/78	0/78	
AJ	0/80	2/80	0/78	
AK	0/80	0/80	0/80	
AL	0/78	0/78	0/77	
AM	0/80	0/80	0/73	
AN	0/79	0/79	0/77	
AO	0/76	0/76	0/72	
AP	0/80	0/79	0/79	
AQ	1/43	0/42	0/42	0/42
AR	0/48	0/48	0/48	0/48
AS	0/40	0/40	0/40	
AT	0/45	0/45	1/45	0/43
AU	0/80	0/80	0/80	
AV	0/80	0/80	0/80	
AW	0/45	0/45	0/45	0/45
AX	1/45	0/44	0/44	
AY	0/45	0/45	1/45	
AZ	1/45	0/43	0/43	
BA	0/45	0/45	0/45	0/45
BB	0/80	0/80	0/80	

ETC 5067
HIGH TEMPERATURE LIFE TEST
TEMP. 125'C

Lot	168 H	500 H	1000 H	2000 H
A	0/80	0/80	0/80	0/80
B	0/80	0/80	0/80	0/80
C	0/80	0/79	0/79	0/79
D	0/80	0/80	0/80	
E	0/72	1/72	0/71	
F	0/72	0/72	0/72	
G	0/80	0/80	0/80	
H	0/72	0/72	0/69	
I	0/72	0/72	0/72	
J	1/80	0/79	0/79	
K	1/45	0/44	0/44	
L	0/80	0/80	0/80	
M	0/44	0/44	0/44	0/44

TEMPERATURE CYCLING
(100 CY)

Lot	ETC 5040	Lot	ETC 5057	Lot	ETC 5067
A	0/40	A	0/38	A	0/47
B	0/23	B	0/40	B	0/40
C	0/50	C	0/40	C	0/40
D	0/40	D	0/45	D	1/40
E	0/40	E	0/39	E	0/40
F	0/37	F	0/40	F	0/40
G	0/36	G	0/40	G	0/40
H	0/39	H	0/40	H	0/40
I	0/40	I	0/40	I	0/40
J	0/40	J	0/40	J	0/40
K	0/40	K	0/37	K	0/40
L	0/40	L	0/38	L	1/40
M	0/40	M	0/40		
N	0/40	N	0/39		
O	0/40	O	0/40		
P	0/40	P	0/40		
Q	0/40	Q	0/40		
R	0/40	R	0/40		
S	0/40	S	0/40		
T	0/40	T	0/45		
U	0/40	U	0/40		
V	0/40	V	0/40		
		W	0/40		
		X	0/38		
		Y	0/38		
		Z	0/38		

4 . FAILURE RATE PREDICTION FOR ETC5040 / ETC5057 / ETC5067

4.1. OPERATING LIFE TEST FAILURE RATE :

Test estimation was made by assiging to all failures the average activation energy for MOS devices, defined by standards such as the MIL-HDBK 217B (E_A = 0.7 eV).

The acceleration factor was computed using junction temperatures taking into account the package thermal resistance and device power dissipation.

Results of this estimation are summarized in the following table :

	Device Hours at 125'C	EA (EV)	Equivalent Device Hours at 55'C	Life Test Failures	Failure Rate in Fits (60 % C. L.)
ETC5040J	3.85×10^6	0.7	2.77×10^8	7	30
ETC5057J	4.06×10^6	0.7	2.92×10^8	10	39
ETC5067J	1.21×10^6	0.7	8.71×10^8	3	48

5 . CONCLUSION

- This report summarizes updated reliability data for MCOS ETC5040 Filter and ETC5057 and ETC5067 COMBOS from SGS-THOMSON Micro-electronics.
- Using operating life test results, a failure of 30 fits may be predicted at 55 C (60 % C.L., EA = 0.7 eV) for ETC5040 and 39 for ETC5057. The failure rate for ETC5067 is expected to decrease since currently tested devices will generate additional devices hours.

HOW TO CHOOSE A FILTER IN A SPECIFIC APPLICATION

By O. Leenhardt

INTRODUCTION

OBJECT OF THIS APPLICATION NOTE

The approach of SGS-THOMSON Microelectronics regarding filtering is aimed at providing all the information required for designing the filter best tailored for a given application. The first step in this approach, and undoubtedly the most important since it is essential for all the others, therefore consists in indicating how, starting from this application, the complete system specifications of a filter must be written. This is the purpose of this application note.

REMINDERS ABOUT THE PRESENT STATUS OF THE SGS-THOMSON FILTERS

The SGS-THOMSON approach consists in manufacturing Mask Programmable Filters (M.P.F). These filters are of the switched capacitor type. They all have the same structure, up to the last mask level (interconnection level). This level is therefore the only one differenciating these filters from one another. We will not describe in full detail the structure of these filters, but simply remind their main features, and then briefly describe the presently available M.P.F's.

MAIN FEATURES :

The main features of these M.P.F's are as follows :

- TECHNOLOGY HCMOS1 (high-density linear CMOS)
- AVAILABLE ORDERS 2 TO 12 (whatever the type of M.P.F.)
- INPUT SIGNAL FREQUENCY 0 TO 30KHz
- INTERNAL SAMPLING FREQUENCY : 500Hz TO 1MHz (depending on the M.P.F. considered)
- INTERNAL SAMPLING FREQUENCY/CUT-OFF FREQUENCY RATIO : 10 TO 200 (depending on the M.P.F. considered)
- THE RESPONSE CURVES (amplitude and phase) may be translated by changing the sampling frequency
- SIGNAL/NOISE RATIO : 70 TO 85dB (depending on the internal structure of the M.P.F. considered)
- POWER SUPPLIES : + 5V OR - 10V
- CONSUMPTION MAY BE ADJUSTED BETWEEN 0.5 TO 20mW PER ORDER
- ACCURACY OF THE CAPACITOR RATIOS : 0.1%
- ACCURACY OF THE CUT-OFF FREQUENCIES : 0.5% (max.).

STANDARD M.P.F.'S AND CUSTOM M.P.F.'S :

SGS-THOMSON MANUFACTURES TWO TYPES OF M.P.F.'S

- Standard M.P.F.'s :

They make up a family presently consisting of 10 models, but this family will expand in the future, according to the evolution of requirements. These M.P.F.'s are the following :

- 5 Low-pass M.P.F.'s :
  TS 8510 (CAUER, 5th order : 32dB attenuation)
  TS 9511 (CAUER, 7th order : 50dB attenuation)
  TS 8512 (CAUER, 7th order : 75dB attenuation)
  TS 8513 (CHEBYCHEV, 8th order)
  TS 8514 (BUTTERWORTH, 8th order)
- 3 High-pass M.P.F.'s :
  TS 8530 (CAUER, 3rd order : 15dB attenuation)
  TS 8531 (CAUER, 6th order : 15dB attenuation)
  TS 8532 (CHEBYCHEV, 6th order)
- 1 Notch M.P.F.'s :
  TS 8540 (8th order : Q = 7)
- 2 Band-pass M.P.F.'s :
  TS 8550 (CAUER, 3rd order : Q = 5)
  TS 8551 (high-selectivity filter Q : 35)

Note : The detailed description of these M.P.F.'s has been the subject of a previous application note.

- Custom M.P.F.'s :

SGS-THOMSON commits itself to supply the first samples 4 to 6 weeks after the customer's definition of the template. All types of filters may be provided (BUTTERWORTH, LEGENDRE, CHEBYCHEV, BESSEL, CAUER), for conventional applications (low-pass, high-pass, bandpass, notch filters, group delay equalizers) or for simultaneous optimization of the amplitude and the phase templates.

HOW TO DEFINE THE COMPLETE SYSTEM SPECIFICATIONS OF A FILTER

FILTER SYSTEM SPECIFICATIONS

The system specifications of a filter are complete when they indicate :

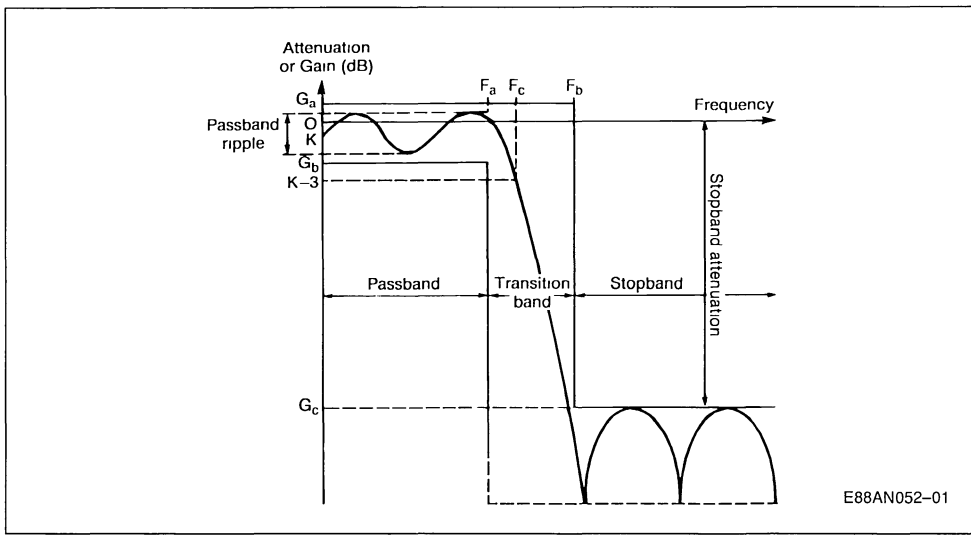
- the amplitude template (amplitude response curve)
- the phase template (phase response curve)
- the group delay curve
- the pulse and step responses
- the dynamics
- the noise factor
- the input and output impedances
- the load impedance (resistance and capacitance)
- the type of signals to filter (level, spectrum,...)
- the value of the power supply sources
- the operating temperature range
- the size (the dimensions)
- the price

Amongst all these parameters, the knowledge of three of them is essential from the technical point of view :

- the amplitude template
- the phase template
- the group delay curve.

As we shall see later on, the following definitions may be used, with minor modifications, for all types of filters. Our definitions are given only for low-pass filters, since we can always relate back to this type when studying any other kind of filter (see 3.B).

Figure 1 : Different Parameters used for Defining an Amplitude Template.



- Amplitude Template (figure1) :

We cannot expect two filters, assumed to be similar, to have exactly identical response curves. This is the reason why we use the concept of template, which is a sort of envelope of the response curve limits in terms of the frequency. The amplitude template is therefore the graphical representation of the filter's "amplitude - frequency" limiting conditions. Its definition is based on the following parameters (low-pass filter) :

- maximum passband attenuation (or gain) (G_a) : maximum level the signal may reach within the passband (in dB).
- minimum passband attenuation (or gain) (G_b) : minimum level the signal may reach within the passband (in dB).
- minimum stopband attenuation (Gc) : minimum attenuation level of the signal within the stopband (in dB).
- passband band of frequencies for which the attenuation (or the gain) must fall between G_a and G_b.
- transition band : band of frequencies for which the attenuation must fall between G_b and G_c.
- stopband : band of frequencies for which the attenuation must be less than G_c.
- cut-off frequency (F_a) : passband upper limit.

- selectivity factor k : equal to the ratio F_a/F_b, it defines the width of the template transition band, and therefore of the filter selectivity. It is always less than 1.

Other parameters must be added when the response curve considered falls within this template :

- passband transfer factor (K) : attenuation (or gain) factor of the response curve within the passband, relative to the 0dB (in dB).
- passband ripple : maximum amplitude difference between two points of the response curve within the passband.
- cut-off frequency (F_c) : frequency corresponding to a 3dB attenuation relative to the passband transfer factor.

Note : The template of a filter is therefore completely determined once the values of G_a, G_b, G_c, F_a and F_b are known.

- Phase template :

Within a real filter, all the frequencies are not transmitted at the same velocity. A non-constant phase shift results (and therefore a distortion) between the output signal and the filter input signal. The phase response curve of a filter is the phase shift curve due to this filter, in terms of the frequency. As with the amplitude response curve, it must be within a phase template, sort of graphical representation of the "phase - frequency" limiting conditions of the filter.

- Group delay curve :

As a consequence of what we have seen above, the group delay concept is preferred to that of propagation velocity of each of the frequencies of a spectrum. We shall thus no longer speak of the propagation velocity for a given frequency, but for a group of frequencies. This group delay is related to the phase shift by the following relationship :

$$t = \frac{d\Phi}{d\omega}$$

with ω = pulsation.

We may infer from this relationship that the steeper the slope of the phase response curve in terms of the frequency, and therefore the more abrupt the filter cut-off, the greater the group delay of a filter will be :

Note : On the group delay curve of the different filters shown below (see 3.D), the value to read on the y-axis corresponds to a normalized group delay ω_c . T equal to T_o, that is an actual group delay expressed in seconds equal to : $T = T_o/\omega_c$, with ω_c = cut-off pulsation of the filter.

- Other parameters :
- pulse and step responses :

The pulse response of a filter is its response to a DIRAC pulse. It can be shown that :

- x(t) any type of signal : $y(t) = h(t) \bigstar x(t)$ with $\bigstar$ - convolution product
  $\rightarrow Y(p) = H(p) \cdot X(p)$ with H(p) - transfer function
- x(t) DIRAC pulse (δ (t)) : $y\,\delta(t) = h(t) \bigstar \delta(t)$
  $\rightarrow Y\,\delta(p) = H(p)$

The pulse response y (t) of a filter is the time representation of its transfer function H(p). It is an intrinsic feature of the filter. It contains all the information relative to the response of the filter to any type of signal.

The step response of a filter is its response to a HEAVISIDE step (unit step). On figure 2, we can see the concept of filter settling time. In effect, if a signal having a spectrum within the filter passband is applied to the filter, the settling time is equal to the time elapsed between the time the signal was applied at the filter input and the output signal obtained, to within a given percentage of the final value (1%). This settling time is closely related to the width (B) of the filter passband (1/B for a bandpass, 1/2B for a low-pass).

- dynamics.

The dynamics of a filter is the ratio between the maximum level of the output signal and its minimum level, that is, the noise level. It is expressed in dB.

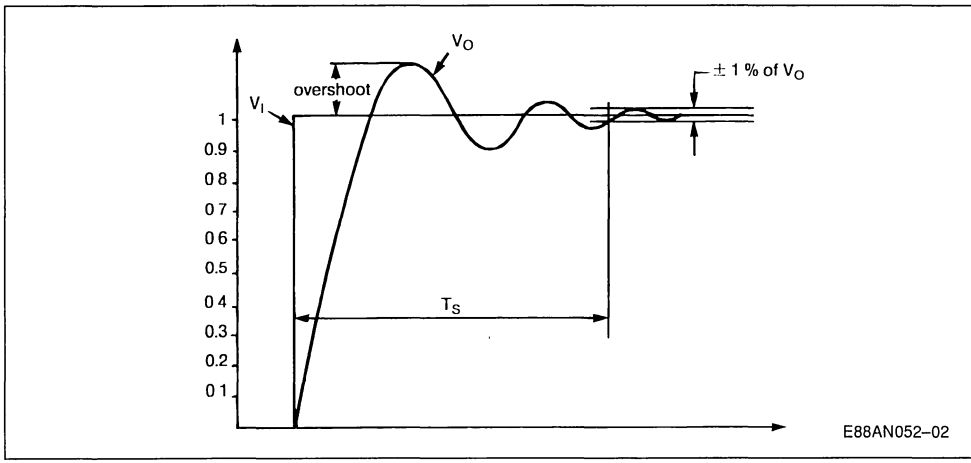
- noise factor.

The noise factor is the ratio between the total filter output noise power and the output noise power due only to the noise applied at the input. It is expressed in dB. For a given structure, the filter output noise mainly depends on the amplitude template, since it is an exponential function of the overvoltage factor Q (see 3.C). In the active filters, the noise is not "white", or at least not throughout the band considered. It is therefore necessary to split this band up into several frequency areas, and to define the corresponding noise features for each of them. We may then speak of a noise power (or voltage) per Hertz (or Hertz square root), for a given frequency (nW/Hz or nV/ $\sqrt{Hz}$). The noise optimization of a filter is not always easy, and this could be kept in mind at system specifications definition time, especially for filters requiring high dynamics (60dB).

- type of signals to be filtered :

Although this may seem obvious, it is not useless to remind the importance of knowing accurately the type of signal to filter, before defining the system specifications of the filter. The signal amplitude curve must be studied in detail (regarding the compatibility with the authorized filter input swing), as well as its frequency spectrum, in order to suppress the possible interaction of undesired frequencies (50Hz, various harmonic components,...) during system specifications definition time.

Figure 2 : Settling Time (t_s) of the Step Response of a Unit Step (v_I).



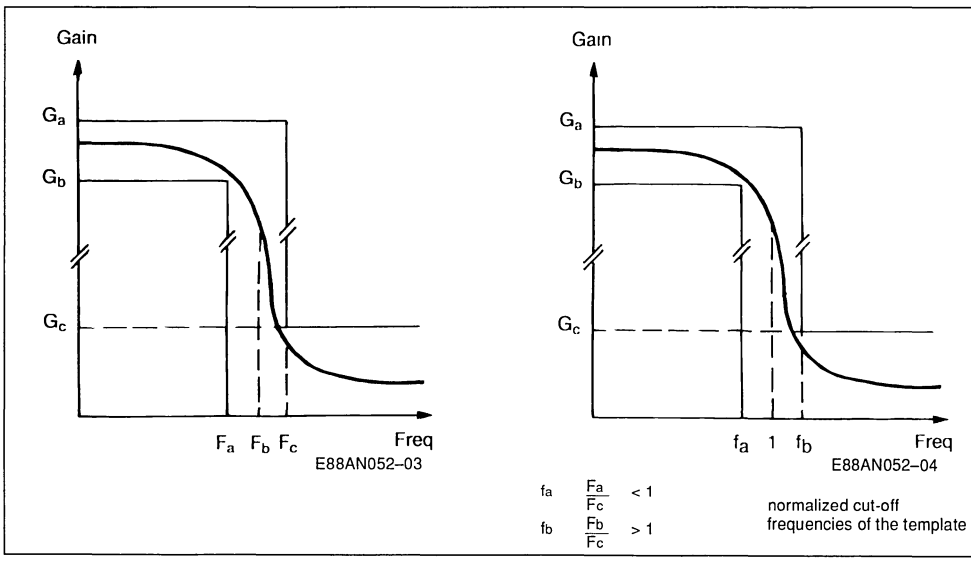
PROTOTYPE LOW-PASS FILTER

- Frequency standardization :

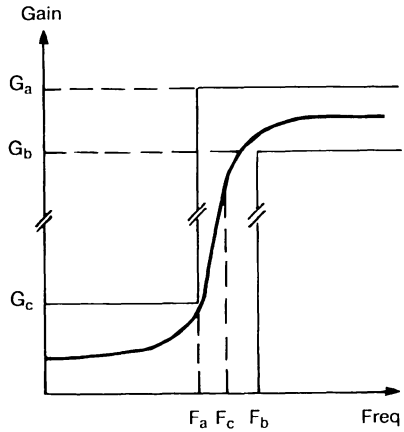
By standardizing the frequency units, the template of any filter may be related back to an template for which only the frequency ratios intervene.

Examples :

- low-pass :



- High-pass :



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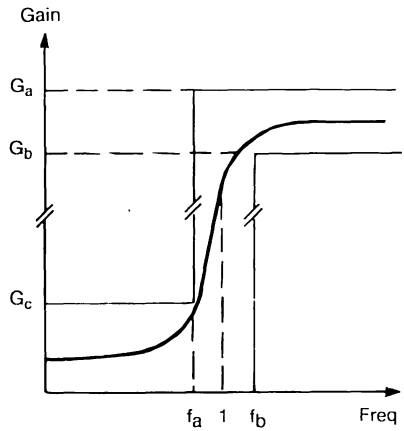
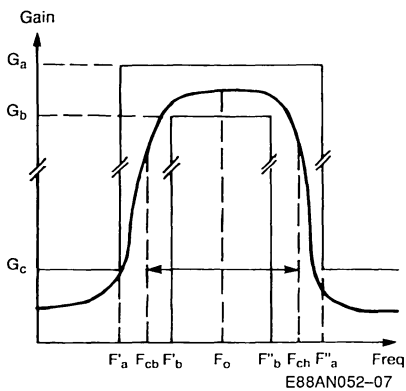


E88AN052–06

Same relationships as above

- Bandpass :



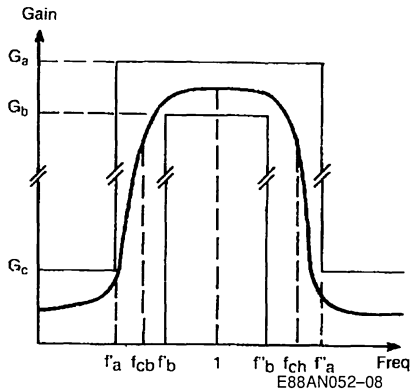
E88AN052–07

Fo $\sqrt{Fcb \cdot Fch}$ characteristic frequency

B Fch – Fcb passband

$\Delta \quad \frac{B}{Fo}$ relative band

$k \quad \frac{F''b - F'b}{F''a - F'a}$ selectivity factor



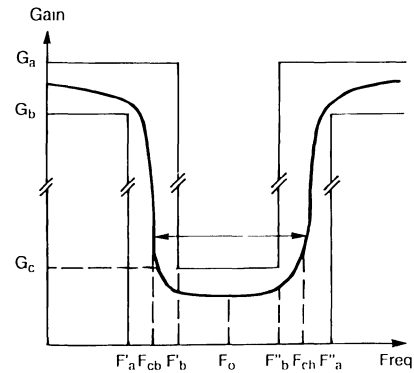
E88AN052–08

$f'a = \frac{F'a}{Fo} < 1$ $\quad f''a = \frac{F''a}{Fo} > 1$

$fcb = \frac{Fcb}{Fo} < 1$ $\quad fch = \frac{Fch}{Fo} > 1$

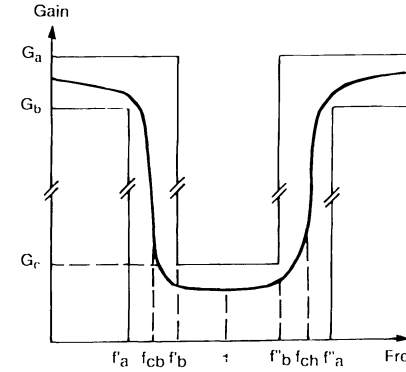
$f'b = \frac{F'b}{Fo} < 1$ $\quad f''b = \frac{F''b}{Fo} > 1$

- notch :



E88AN052-09

Same relationships as above



E88AN052-10

Same relationships as above

• Prototype low-pass filter :

Once the standardizations above have been performed, some transformations allow the high-pass, bandpass and notch filter template to relate back to that of a so-called "prototype" low-pass filter. These frequency transformations are as follows :

- low-pass → high-pass.

It consists in replacing p by 1/p in the low-pass filter transfer function. Thus, conversion from the low-pass template to the high-pass template is performed in the following way:

$f_a \rightarrow f'_a \; 1/f_a$

$f_b \rightarrow f'_b \; 1/f_b$

- low-pass → bandpass :

It consists in replacing p by $\frac{1}{\Delta}(p + 1/p)$ in the low-pass filter transfer function. Thus, conversion from the low-pass template to the bandpass template is performed in the following way :

$f_{cb}\ f_{ch}\ f'_a\ f''_a\ f'_b\ f''_b\ 1$

- low-pass → notch filter :

It consists in replacing p by $\frac{1}{\frac{1}{\Delta} \cdot (p + 1/p)}$

in the low-pass filter transfer function. Thus, conversion from the low-pass template to the notch filter template is performed in the following way :

$f_{cb}\ f_{ch}\ f'_a\ f''_a\ f'_b\ f''_b\ 1$

Therefore, in the remaining parts of this notice, all the calculations and examples will be related back to a (prototype) frequency-standardized low-pass filter template, since conversion to the template of any other type of filter can be obtained using the transformations above.

FILTER TRANSFER FUNCTION :

• General definitions :

The transfer function is the mathematical representation of the filter amplitude response curve. It is an obligatory intermediate, allowing the calculations of the different filter factors to be carried out. It is expressed as a ratio between the output level and the input level of the filter, in terms of the frequency. This ratio may be expressed as a function of the complex variable p :

$$H(p) = K\frac{N(p)}{D(p)} \qquad (1)$$

with N(p) and D(p) : p polynomials.

This expression may therefore be written in the following way :

$$H(p) = K\frac{a_m \cdot p^m + \ldots\ldots + a_1 \cdot p + a_0}{b_n \cdot p^n + \ldots\ldots + b_1 \cdot p + b_0} \qquad (2)$$

In this form, the order of the filter is defined as being equal to the degree of the denominator D(p) (in this case, n). The stability criterium for a filter dictates that the degree of D(p) (the order of the filter) be greater or equal to the degree of N(p). On the other hand, the higher the order of a filter, the more abrupt its cut-off, as can be seen on the relationship providing the asymptotic slope of a filter at the cut-off, in terms of its order :

P 6.n (dB per octave)

We may also express the transfer function in another way, by replacing the coefficients a_o,..., a_m, b_o,..., b_n by the roots z_1,..., z_m ; p_1,..., p_n of the N(p) and D(p) polynomials :

$$H(p) = K\frac{(p-z_1).....(p-z_m)}{(p-p_1).....(p-p_n)} \quad (3)$$

The zeros of the transfer function are the Z_1,..., Z_m constants and the poles are the P_1, ..., P_n constants.

These constants are either real or imaginary conjugated.

It can be shown that if n is even, the poles of H(p) are all imaginary conjugated, two by two, and that if n is odd there is a single negative real root. D(p) may therefore be written in the form of a product of 2nd order factors if n is even, and in the form of a product of 2nd order factors and of a 1st order factor, if n is odd. A new expression can then be obtained for the transfer function :

$$H(p) = K\frac{(p-z_1).....(p-z_m)}{(p-p_o).(p^2+2.\delta 1.p+\rho_1^2).....(p^2+2.\delta k.p.\rho_1^2)} \quad (4)$$

with $K = \frac{n-1}{2}$ if n is odd, and $k = \frac{n}{2}$ and without $(p-p_o)$ if is even

It can then be shown that any filter can be obtained by cascading 2nd order cells if n is even, or 2nd order cells and one 1st order cell if n is odd.

- General transfer function for a 1st order cell :

It may be expressed as :

$$H(p) = K\frac{N(p)}{1+a.p}$$

with

- p complex pulsation
- a time constant

This last parameter allows the cut-off pulsation (and therefore the cut-off frequency) of the cell to be defined as its reciprocal
($\omega c = 1/a$ and $F_c = 1/(2.\pi.a)$).

a is a time value such that 3.a (5.a) characterises the time after which the response has reached 95% (99%) of its final value.

Note : The expression of N(p) depends on the type of filter considered :

- polynomial low-pass filter : N(p) = 1
- polynomial high-pass filter : N(p) = p/a (with $p \rightarrow 1/p$)

- General transfer function for a 2nd order cell :

It may be written as follows :

$$H(p) = K\frac{N(p)}{1+2.\xi.p/\omega_o+p^2/\omega_o^2}$$

with :

- p : complex pulsation
- K : passband transfer factor

- For Low-pass and high-pass cells :

The relationship above allows the following parameters to be defined :

- the undamped natural pulsation ω_o (or characteristic pulsation) used as a standardization pulsation (F_o : characteristic frequency).
- the damping factor ξ , magnitude without units specifying the shape of the filter responses :

if $\xi < 0.707$ distinct, transient, ωp pulsation oscillations for the unit response ; resonance on the frequency response,

if $0.707 < \xi < 1$ not very distinct, transient oscillations ; the final value of the unit response is overstepped. No resonance on the frequency response,

if $\xi = 1$ damping factor critical value,

if $\xi > 1$ no oscillation, a periodic response without overstepping the final value of the unit response.

- the natural pulsation of the filter $\omega\rho = \omega_o.\sqrt{1-\xi^2}$ characterising the pulsation of the filter transient oscillations,
- the resonance pulsation $\omega_r = \omega_o.\sqrt{1-2.^2}$, specifying the resonance position,
- the overvoltage or resonance factor

$$Q = \frac{|H(j\omega r)|}{|H(O)|} = \frac{\sqrt{1}}{2\cdot\xi\ \sqrt{1-\xi^2}}$$

specifying the value of the gain of the filter for the resonance pulsation.

- the relative band Δ related to the overvoltage factor by the relationship

$$Q = \frac{1}{\Delta}$$

Note : The expression of N(p) depends on the type of filter considered :

- polynomial low-pass filter : N(p) = 1

- polynomial high-pass filter : $N(p) = p^2 / \omega^2$
- low-pass elliptic filter : $N(p) = p^2 + \omega_\infty^2$ with $\omega_\infty > \omega_o$
- high-pass elliptic filter : $N(p) = p^2 + \omega_\infty^2$ with $\omega_\infty > \omega_o$
- bandpass and notch filter cells :

The relationships above are slightly different for a bandpass and notch filter, 2nd order cell. In this case:

- $Fo = \sqrt{F_{CB} . F_{CH}}$ with F_{cb} and F_{ch} : low and high cut-off frequencies of the cell.
- $Q\ F_o / \Delta F$ with $\Delta F = F_{ch} - F_{cb}$, called relative band.

We may infer from this relationship :

$$Q = \frac{F_{ch} - F_{cb}}{F_o}$$

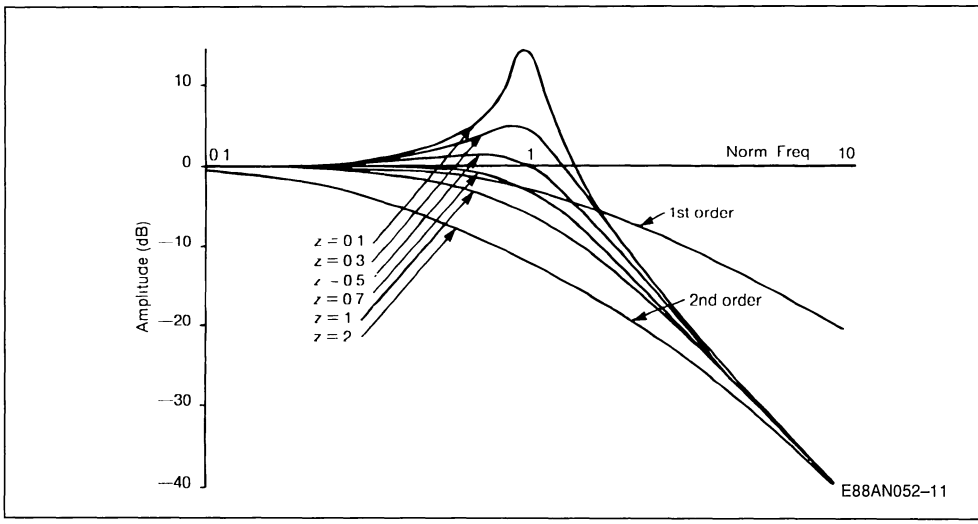
Note : The expression of N(p) depends on the type of filter considered :

- bandpass filter $N(p) = 2 . \xi . P/\omega_o$
- notch filter $N(p) = p^2 + \omega^2$

- Conclusion

Figure 3 shows the shapes of the amplitude response curves of the 1st and 2nd order low-pass cells, for different values of ξ . Let us keep in mind that a 2nd order filter presenting interesting features is obtained for ξ 0.707. In effect, the transient oscillations and the resonance (Q = 1) no longer appear, and the frequency response presents a passband equal to the value $F_o\ \omega_o/(2 . \pi)$.

Figure 3 : Amplitude Response Curves of á 1st and a 2nd Order Low Pass Cells in Terms of the Damping Factor (called Z on this figure).



CHARACTERISTIC FUNCTIONS

The major problem when designing a filter consists in factorising N(p) and D(p), in order to write the transfer function in the form shown on expression 4. To simplify the calculations, it is often preferrable to start from the template considered and to try to have a well known characteristic function pass within it. As there are a great number of functions that may be inscribed within a given template, the selection of one of them will depend on the following features :

- it must be possible to synthesize it
- it must be possible to split it up into a product (or an addition) of functions, and it must be possible to carry each one out
- it must comply with the filter system specifications (phase, group delay,...)

The filter designer must therefore optimize his selection, taking into account all these constraints. A relatively great number of well known characteristic functions simplifies this task.

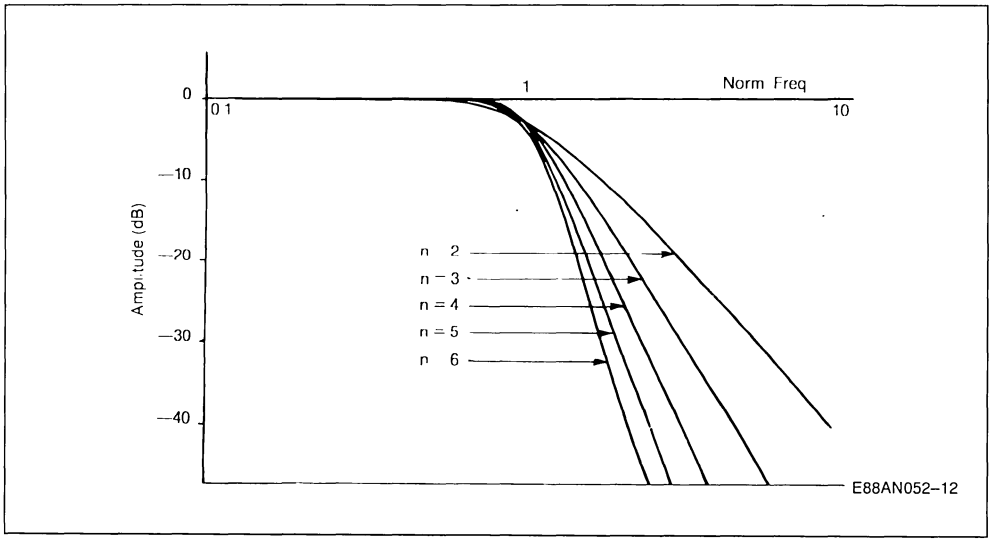
- Low-pass polynomial filters :

Their transfer functions comply with N(p) 1. The following are the most often used :

- BUTTERWORTH filters :

They correspond to amplitude response curves with the following features (figure 4).

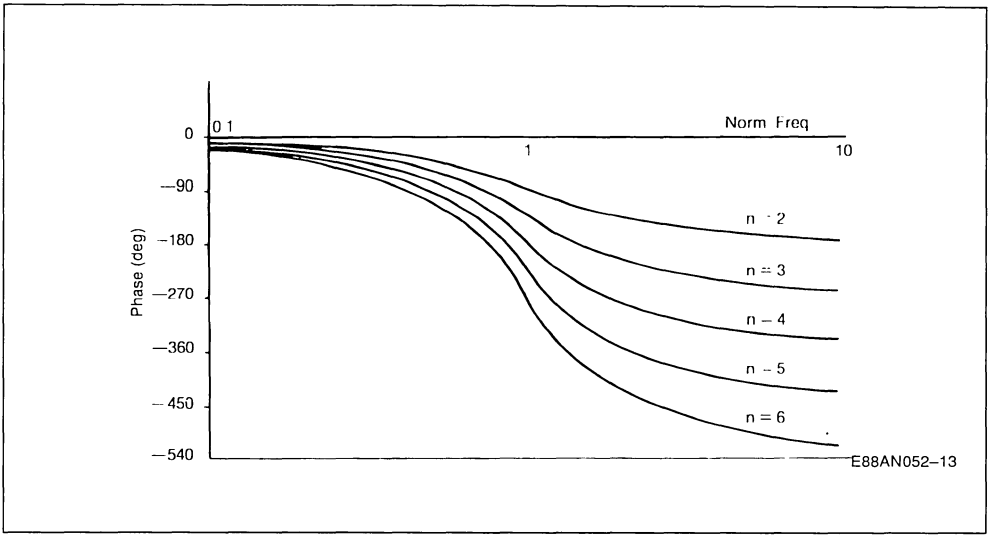
Figure 4 : Amplitude Response Curves of the Butterworth Low Pass Filters.



- no ripple within the passband
- not very rapid cut-off near the cut-off frequency.

The phase response curves of these filters present relatively small phase rotations (figure 5).

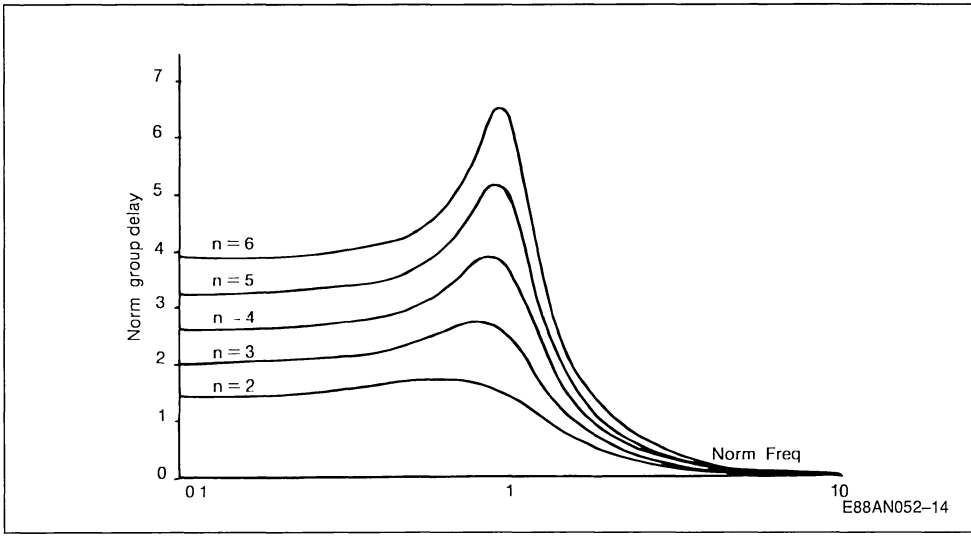
Figure 5 : Phase Response Curves of the Butterworth Low Pass Filters.



The group delays are relatively constant within the passband and their ratio with the group delays of the frequencies around the cut-off frequency is equal to 1/2 (figure 6).

Note : The higher the order n of the filter, the closer the amplitude response curve will be to the ideal curve (rectangular template)

Figure 6 : Group Delay Curves of the Butterworth Low Pass Filters.

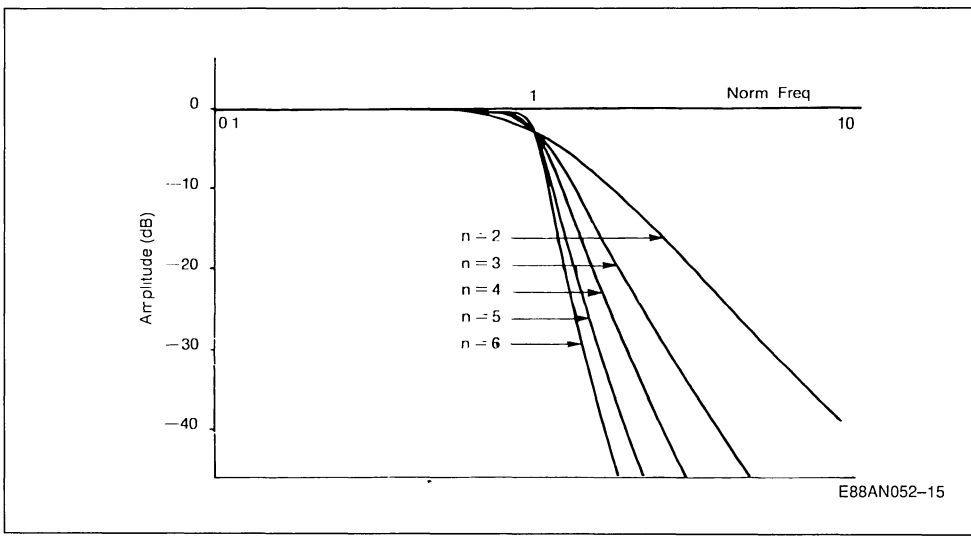


- LEGENDRE filters :

They correspond to amplitude response curves having the following features (figure 7) :

- cut-off as rapid as possible near the cut-off frequency
- regular attenuation within the stopband

Figure 7 : Amplitude Response Curves of the Legendre Low Pass Filters.



The phase response curves are practically identical to those of a BUTTERWORTH filter (figure 8). Regarding the group delays for a given order, they are relatively constant within the passband, and their ratio with the group delays for the frequencies around the cut-off frequency is equal to 1/2 (figure 9). But since the slopes of these curves are very steep for this frequency, these time are in general higher than those of the BUTTERWORTH filters.

Figure 8 : Phase Response Curves of the Legendre Low Pass Filters.

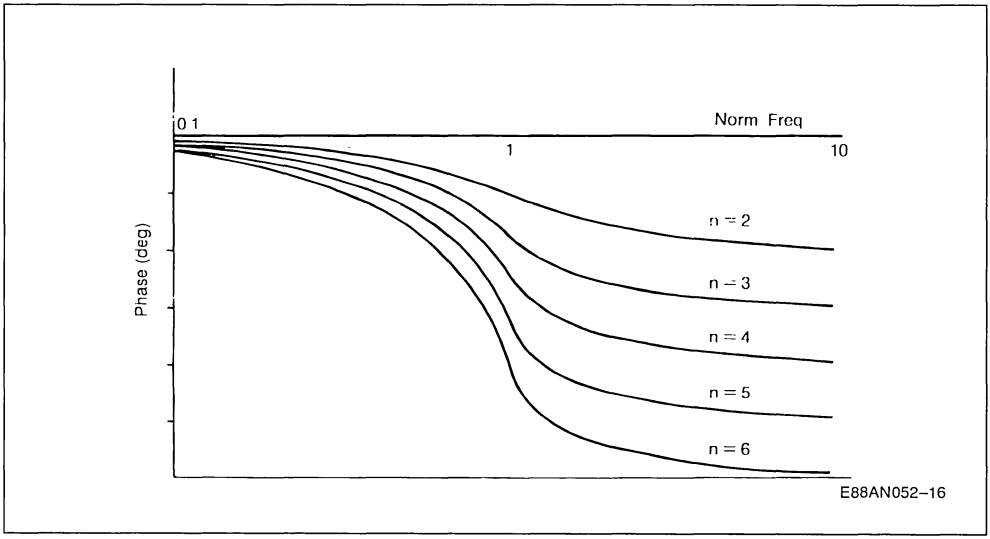
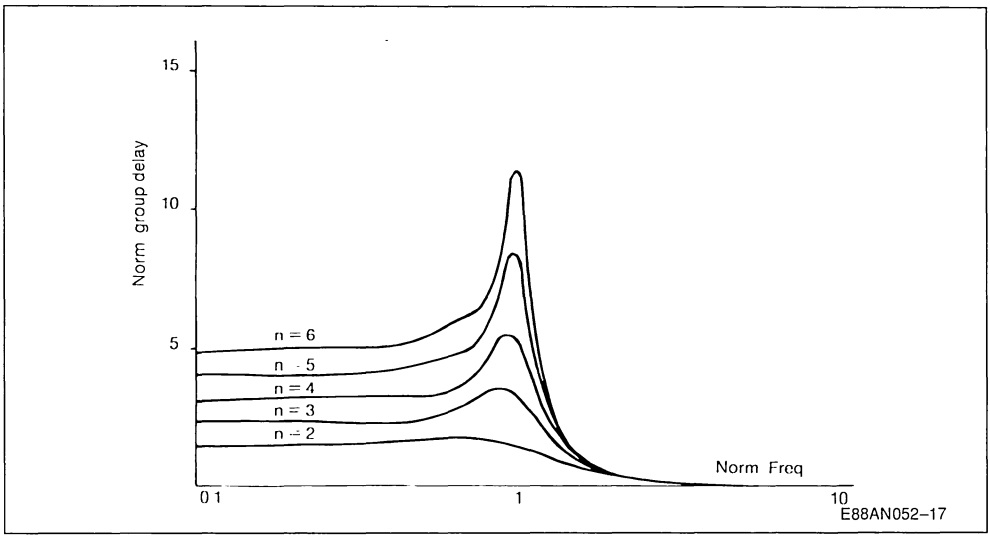


Figure 9 : Group Delay Curves of the Legendre Low Pass Filters.

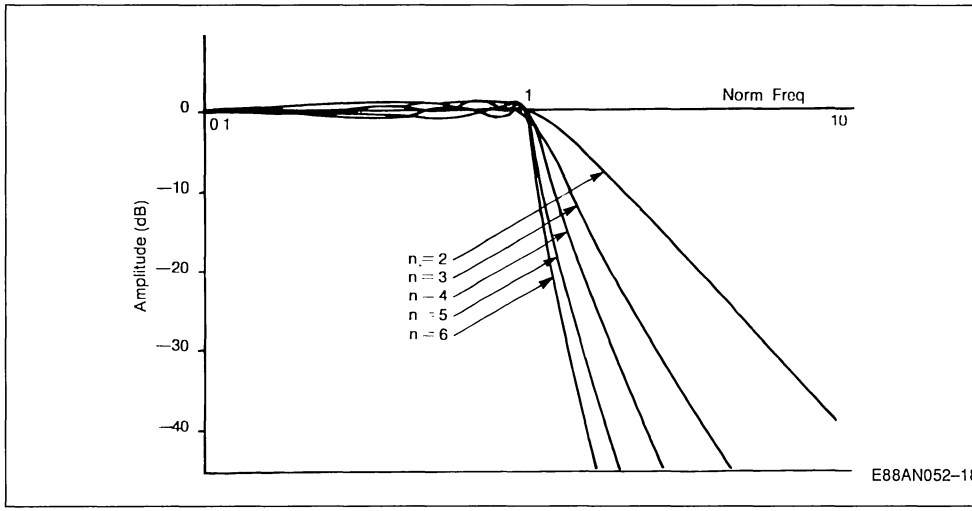


- - CHEBYCHEV filters

They correspond to amplitude response curves presenting the following features (figure 10).

- - ripples within the passband (up to 2dB)
- - rapid cut-off near the cut-off frequency (at least in the first octave)

Figure 10 : Amplitude Response Curves of the Chebychev Low Pass Filters.



The phase response curves present greater rotations than those of the BUTTERWORTH filters (figure 11). The group delays within the passband are not identical for a given order, and their ratio with the group delays of the frequencies around the cut-off frequency is equal to 1/3 (figure 12).

Note : The order of a CHEBYCHEV filter is equal to the number of extrema of the amplitude response curves located within the passband.

Figure 11 : Phase Response Curves of the Chebychev Low Pass Filters.

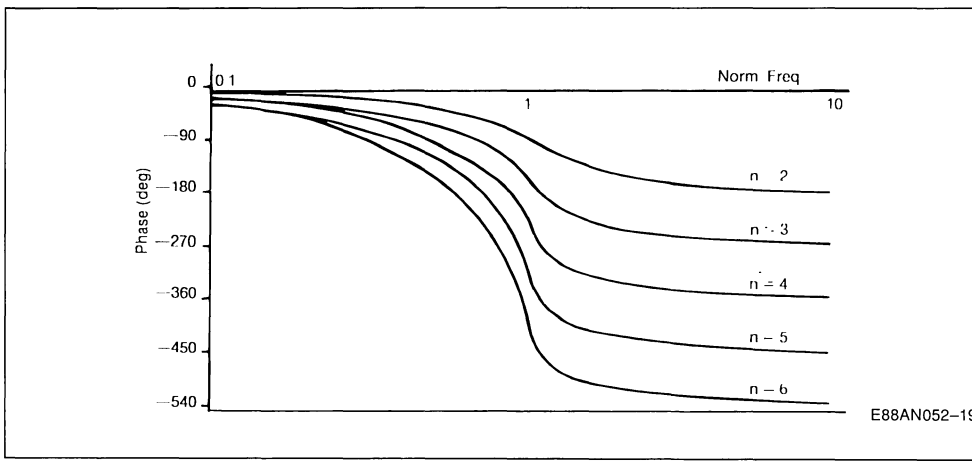
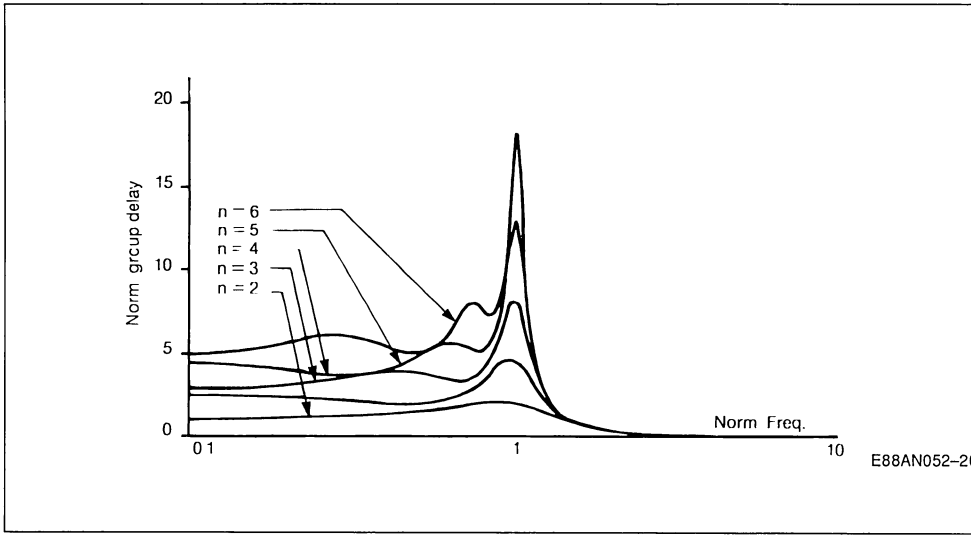


Figure 12 : Group delay Curves of the Chebychev Low Pass Filters.

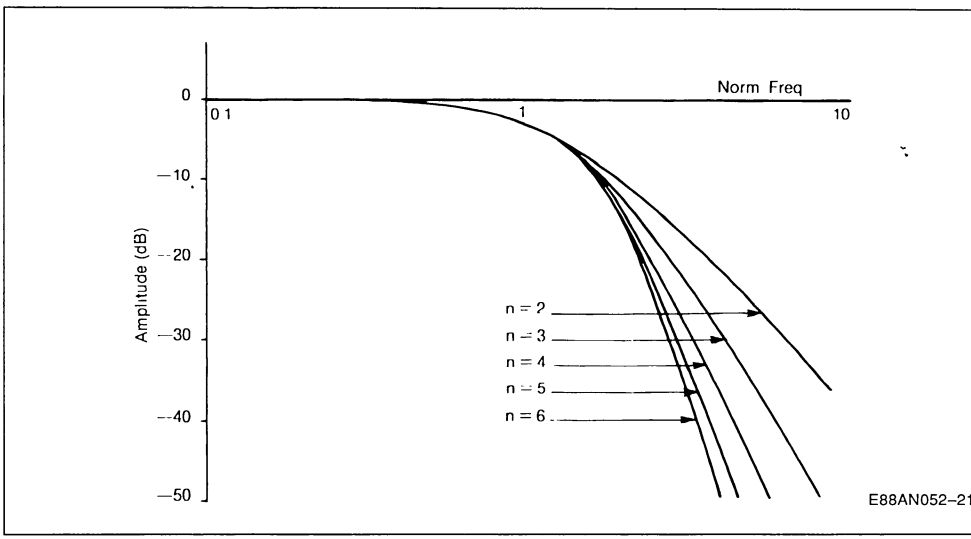


- BESSEL filters

They correspond to amplitude response curves presenting the following features (figure 13) :

- very slow cut-off near the cut-off frequency
- small attenuation within the stopband

Figure 13 : Amplitude Responses Curves of the Bessel Low Pass Filters.



The phase response curves are practically identical to those of the BUTTERWORTH filters (figure 14). These filters are mainly interesting because of their group delays, strictly constant within the passband until beyond the cut-off frequency (figure 15). They therefore have a very close to a pure delay characteristic, and they must be used in all applications for which the non-distortion of the signal is an essential factor.

Figure 14 : Phase Response Curves of the Bessel Low Pass Filters.

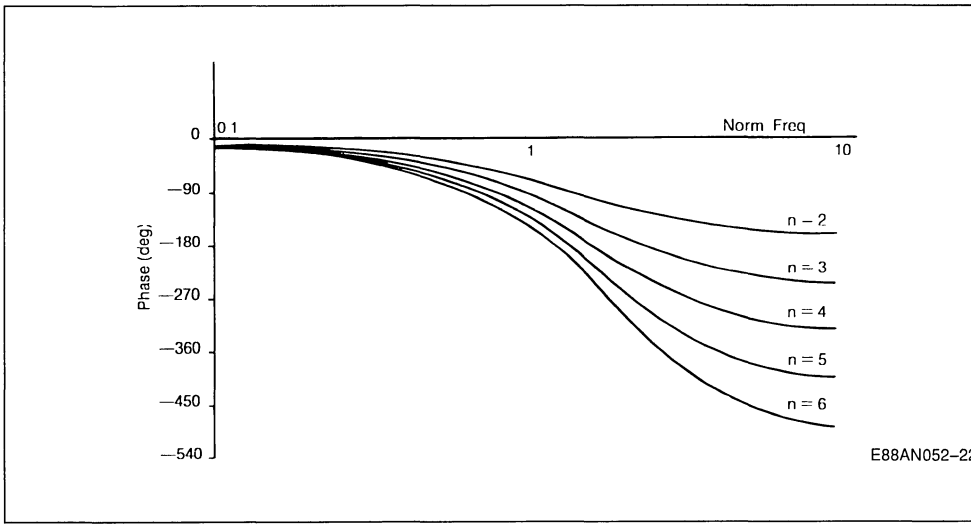
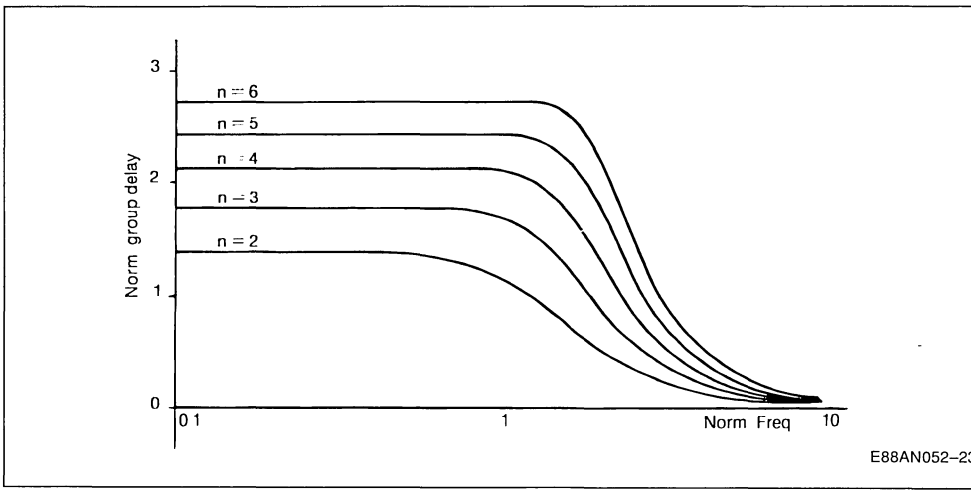


Figure 15 : Group Delay Curves of the Bessel Low Pass Filters.



- Low-pass elliptic filters :

Their transfer functions are such that N(p) may be expressed in the following way :

$$N(p) = (p^2 + \omega_1^2).....(p^2 + \omega_k^2) \text{ with } \begin{cases} k = \dfrac{n}{2} & \text{if n is even} \\ k = \dfrac{n-1}{2} & \text{if n is odd} \end{cases}$$

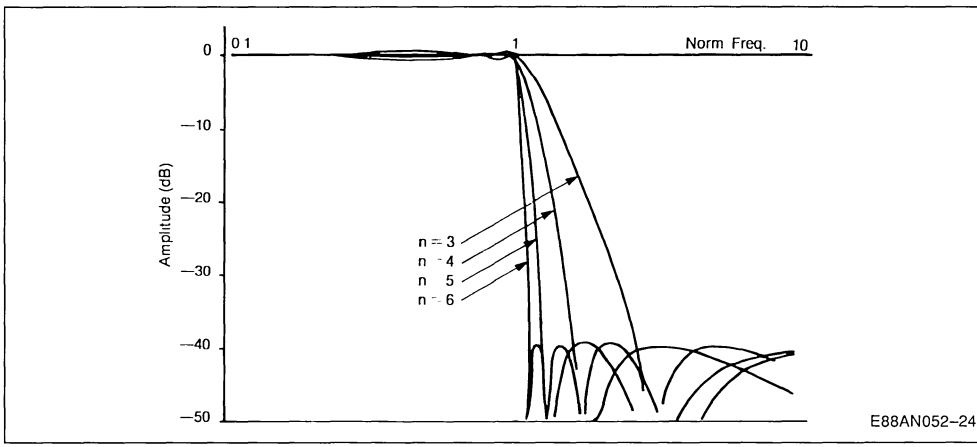
and ω_1, ..., ω_k : transmission zeros.

- CAUER filters :

They correspond to amplitude response curves presenting the following features (figure 16).

- ripples within the passband
- very rapid cut-off near the cut-off frequency
- presence of one or several transmission zeros (N(p) roots)

Figure 16 : Amplitude Response Curves of the Cauer Low Pass Filters.



The phase response curves have greater rotations than the CHEBYCHEV filter ones (figure 17).

The group delays are very different for a given order, from one area of the passband to another, and their ratio with the group delays of the frequencies around the cut-off frequency is equal to 1/10 (figure 18).

Figure 17 : Phase Response Curves of the Cauer Low Pass Filters.

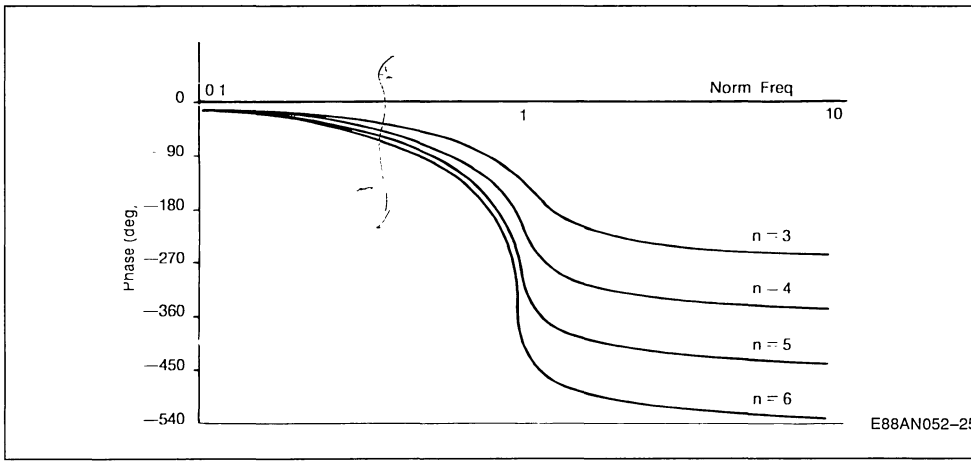
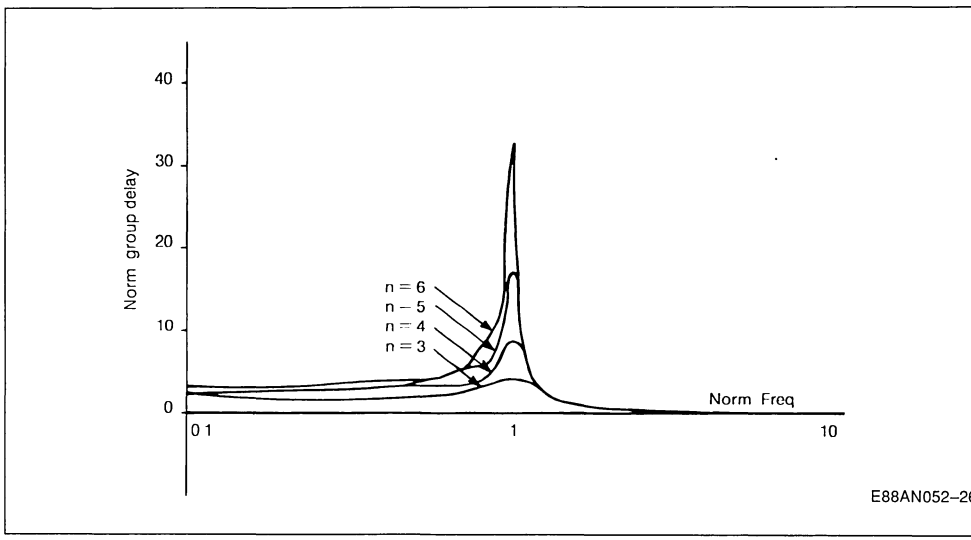


Figure 18 : Group Delay Curves of the Cauer Low Pass Filters.



• Conclusion :

A number of nomographs, tables and curves provide, for each type of function and according to its order, the amplitude response curves, the phase response curves, the group delay curves, and also the pulse and step responses. All these characteristics, and a few others, are summarized in the table on figure 19.

Regarding our subject, we will keep in mind the following :

- The BUTTERWORTH filters are interesting because of the regularity of their passband (no ripple) but their cut-off is not very abrupt
- The LEGENDRE filters associate a convenient regularity of the amplitude response curve with a cut-off abruptness and a transient behaviour that are of good quality
- The CHEBYCHEV filters present, at least within the first octave, an abrupt cut-off, but their transient behaviour is not very performing
- The BESSEL filters present a very good transient behaviour, but their cut-off is not very abrupt
- The CAUER filters allow an extremely abrupt cut-off be obtained, but their group delay regularity is mediocre. They present transmission zeros.

Figure 19 : Comparaison between the Performances of the Different Kinds of Filters.

Kind of Performance	Kind of Filter				
	Butterworth	**legendre**	**Chebychev**	**Bessel**	**Cauer**
Cut-off Abruptness for a Given Order	● ●	●	■ ■	● ● ●	■ ■ ■
Regularity of the Amplitude Response Curve	■ ■ ■	■ ■	Ripple within the Passband/ regular within the Notch	■ ■	Ripple within the Passband and the Notch
Regularity of the Group Delay	■	●	● ●	■ ■ ■	● ● ●
Sensitivity	■ ■	■ ■	●	■ ■	● ●
Transient Condition Distortions	■ ■	■ ■	● ●	■ ■ ■	● ● ●
Transmission Zeros	None	None	None	None	Yes
Required Overvoltage Factors	Very Low	Low	Medium	Medium	High

● ● ● : Very Mediocre
● ● : Mediocre
● : Medium

■ ■ ■ : Excellent
■ ■ : Very Good
■ : Good

SOME IDEAS CONCERNING FILTERS DESIGN

We will assume for the following that the future designer has a comprehensive knowledge of the system specifications of the filter required for this application. We will show briefly how, starting from these system specifications, he may design the filter required. Since this study is beyond the scope of his application specification, this approach will necessarily be very brief.

The design of a filter is performed in four steps :

- determining the characteristic parameters of the filter
- selecting the type of filter
- calculating the filter transfer function
- filter synthesis

A. DETERMINING THE CHARACTERISTIC PARAMETERS OF THE FILTER :

From the amplitude template related back to the prototype filter template (standardized low-pass), the following parameters are assumed to be known :

- G_a. maximum gain within the passband
- G_b. maximum attenuation within the passband
- G_c. minimum attenuation within the stopband
- k selectivity
- Δ relative band (only for the bandpass and the notch filters)

The knowledge of these parameters will allow the complete design of the filter to be performed.

B. SELECTING THE TYPE OF FILTER :

We have seen the different features of the BUTTERWORTH, LEGENDRE, CHEBYCHEV, BESSEL and CAUER filters. Let us keep in mind that the main criteria used for selecting a given type of filter are the following :

- the cut-off abruptness
- the passband regularity
- the group delay regularity
- the existence of transmission zeros
- the behaviour under transient conditions

C. CALCULATING THE FILTER TRANSFER FUNCTION :

Let us assume that the type of filter is known. We must now determine its transfer function. Three steps are required to this end :

a) determining the degree of this function :

The desired amplitude template is related back to the prototype filter template (standardized low-pass) ; by placing the different response curves of the above filters within this template, we obtain not only a type of filter but also its order, and thereby the degree of the corresponding transfer function.

b) determining the transfer function of the prototype filter :

Depending on the different values of the parameters of the prototype amplitude template desired, a number of nomographs and tables allow the calculation of the transfer function corresponding to this template to be carried out.

c) transposing the transfer function :

If the filter to be designed is not a low-pass (high-pass, bandpass, notch filter), the transfer function determined above may be transposed to the corresponding transfer function, using the transformations defined above.

D. FILTER SYNTHESIS :

It mainly consists in factorising the final transfer function in the form of a product of 1st and 2nd degree factors. The desired filter may then be easily designed, by cascading the 1st and 2nd order elementary filters corresponding to each of these factors.

CONCLUSION :

In most - not to say all - electronic applications, the filtering portion has become one of the most important. We have found out that it also was the least well known. By defining all the parameters specified in the system specifications of a filter, and by providing a selection guide amongst the different existing types, we offer anybody who wishes to do so the possibility of making up for lost time, and seeing how this may be inserted into his general application.

IMPLEMENTATION AND APPLICATIONS AROUND STANDARD MPF

INTRODUCTION

At a time when increased miniaturisation is the vogue, the problems posed by the filtering of electrical parameters are on an upward trend. The increase in filter order, progressively improved performances mean generally that in order to solve these problems, a considerable increase in components (also generally their size) has to be used. The adjustments in consequence become also more difficult to effect.

In this gloomy context, the advent of switched capacitor techniques has considerably widened the scope of classical filters. Not content to rest here, SGS–THOMSON Microelectronics goes even further and offers an even new concept in filtering : the M.P.F. (Mask Programmable Filter).

This application note has therefore several objectives : to explain the switched capacitor principle (application, advantages), to describe the M.P.F. general circuit (structure, block diagram, principal characteristics), to present the SGS–THOMSON approach (standard, custom) and to finish by a quick description of all the possible applications of the M.P.F. and more specially one amongst them : the frequency detection.

THE SWITCHED CAPACITOR

PRINCIPLE :

Consider figure 1. When the switch is in position 1, the charge at the capacitor terminals is $Q1 = C \times V1$. If the switch is now moved in position 2, the charge at the terminals of C becomes $Q2 = C \times V2$. This switching allows a charge transfer $Q = Q2 - Q1 = C \times (V_2 - V_1) = C \times \Delta V$ between the points 1 and 2 of the circuit.

This charge transfer in equivalent to the flow of a current $I = \Delta Q/T = \Delta Q \times F = C \times \Delta V \times F$ where F is the commutating frequency of the switch. ($F = 1/T$)

If we compare now the previous expression with Ohm law applied to a resistance ($I = \Delta V/R$), then we can deduce an electrical equivalence between the resistor and the switched capacitor :

$$R = \frac{1}{C \times F}$$

The technique of switched capacitors enables us therefore to simulate resistors with capacitors. Additionnally, the values of these resistors vary with the sampling frequency employed. These two key points offer considerable advantages to this technique.

This relationship leads to an important comment. In effect, the equivalence "transfered charge = discrete quantity of current" is only valid for high switching speeds. This is certainly the case for switched capacitor filters where, in order to avoid aliasing and smoothing problems inherent in all sampling systems, relatively high sampling frequencies are used, sufficiently high, in any case, for the previous relationship to remain valid.

EXAMPLE OF THE APPLICATION WITH AN INTEGRATOR :

In order to understand the operation of a switched capacitor integrator, consider the case of a standard inverting integrator as shown in figure 2.

Remember that the time constant of this circuit (= R x C') determines, in active filter circuits, parameters such as bandwith and cut-off frequency.

However, in this example, this time constant presents a major obstacle : the total lack of correlation between the values of R and C'. The eventual variations or drifts of these two values not necessarily moving in the same direction, leads to a relatively high and difficult to handle innacuracy when associated with the values mentioned above.

Consider now the switched capacitor integrator shown in figure 3. According to the equivalence previously mentioned, the time constant of this integrator is equal to :

$$\tau = \frac{C'}{C \times F}$$

Figure 1 : Principle of the Switched Capacitor.
1 : C produces the charge $Q_1 = C \times V_1$
2 : C produces the charge $Q_2 = C \times V_2$

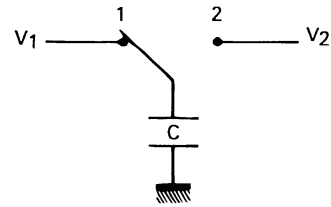


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Figure 2 : Standard Inverting Integrator ($\tau = R \times C'$).

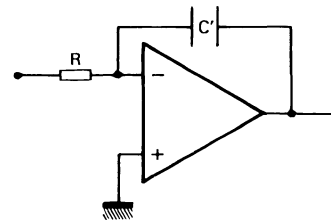

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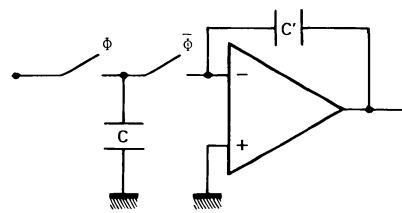
Figure 3 : Switched Capacitor Inverting Integrator ($\tau = \frac{C'}{C \times F}$).



where F is the switching frequency

($F = \frac{1}{T}$ with $T = \Phi + \overline{\Phi}$)

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Then, we show in a standard integrator, accuracy depends upon the absolute values of the components, when in a switched capacitor integrator, only the relative values are considered.

ADVANTAGES OF THE SWITCHED CAPACITOR TECHNIQUE :

The preceeding result shows three major advantages.

The first concerns the relative ease with which an MOS technology can supply excellent precision of capacitor ratio (0.1%). Also, since it is not difficult to obtain good sampling frequency accuracy, the accuracy of the global time constant can attain, with the switched capacitor technique and no external adjustments, values better than 0.5%. It is this precision that we find over the complete frequency range of M.P.F.

The second advantage concerns the equivalence "resistance = switched capacitor" and the possibility offered by this relationship of being able to integrate, in MOS technology, high values of resistance on a small surface area.

Finally, the use of a clock offers considerable scope for modification of the time constant by simple sampling frequency adjustment. Since this time constant is proportional to the cut-off frequency, we can deduce that a constant ratio exists between the sampling frequency and the cutt-off frequency of the M.P.F. It is possible therefore, using this technique, to offset the cut-off frequency of the M.P.F. by simply modifying the sampling frequency. This last point highlights the extreme flexibility of use of the M.P.F. Other advantages of equal importance such as the almost total absence of external components, low power consumption, no adjustment and high temperature stability confer on the M.P.F. extreme flexibility of use and very high operating reliability.

THE TS85XX PRODUCT

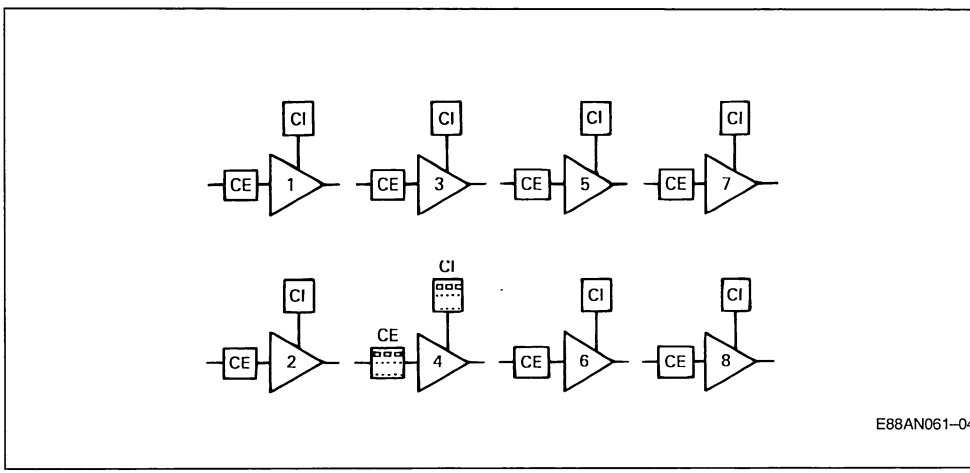
THE M.P.F. STRUCTURE :

The problems encountered now in filtering (varied requirements, prohibitive costs, long lead times) lead SGS-THOMSON to choose a pre-diffused technique where the final characterization of the filter is defined by the interconnection mask (last level of masking).

This structure, shown in figure 4, consists of 8 elementary cells each formed by a switched capacitor integrator and two capacitor areas CE and CI. Each area contains a high number of incremental capacitors each of value 0.1pF. Thus, according to the type and filter order of M.P.F. required, the integrators can be interconnected, and according to the "Gain-Frequency" response curve required, the various incremental capacitors are also interconnected. The number of incremental capacitors thus connected varies from one area to another and depends upon the different coefficients of the transfer function that the M.P.F. is required to execute.

N.B. : Generally, the number of integrators interconnected is equivalent to the filter order obtained.

Figure 4 : A filtering unit consisting of 8 elementary cells each containing a switched capacitor integrator. Each capacitance area (CI and CE) contains an optimum number of incremental capacitors of 0.1pF.

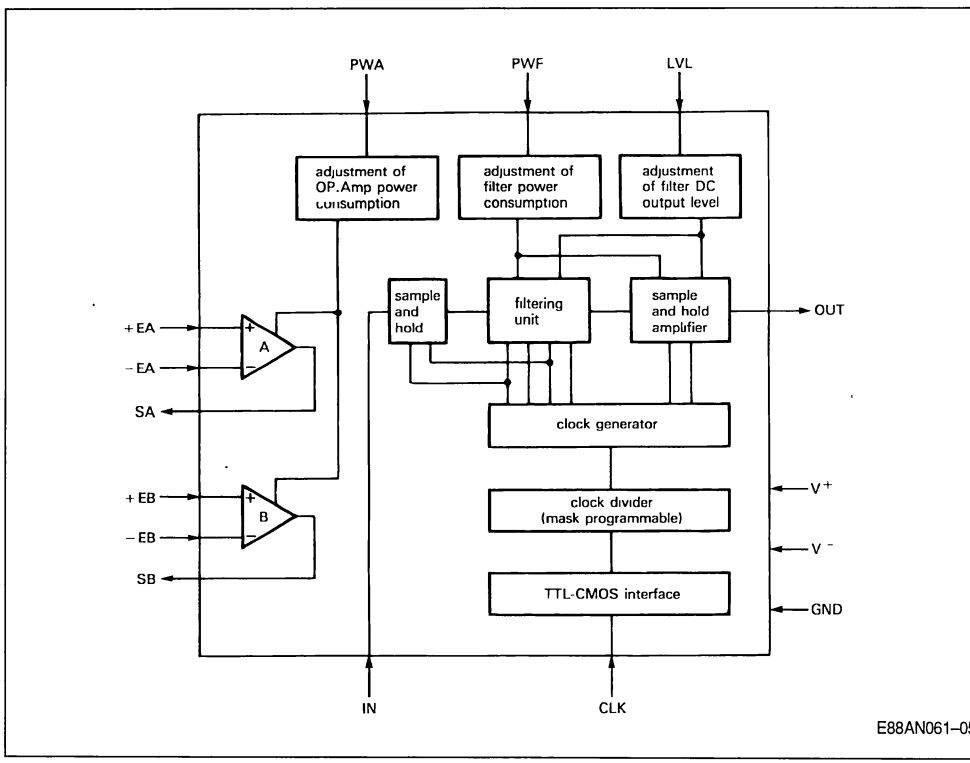


Block Diagram :

The block diagram of the M.P.F. structure utilised is shown in figure 5. The principal internal functions are :

- a filtering unit composed of 8 switched capacitor integrators interconnectable between each other at the final mask level (interconnection level),
- a clock generator producing the various phases required for the internal switching of the capacitors. These phases are imperatively non-overlapping. The internal clock is obtained via a divider, equally mask programmable, and which matches the external clock defined by the user to that of the M.P.F. As the clock input is TTL compatible, a TTL-MOS level interface is provided, within the circuit, in order to obtain the correct voltage swings,
- a sample and hold unit before the filtering unit,
- a sample and hold amplifier tied to the output of the filtering unit and which enables low impedance signals to be available at the output of the M.F.P.
- the adjustment of the DC output level of the M.P.F. by an external voltage source (for example a divider connected between the positive and the negative power supplies and whose midpoint is connected to LVL pin of the M.P.F.),
- two general purpose and independant operational amplifiers available and destined to be used by the customer for other applications associated with the M.P.F. (anti-aliasing, smoothing, comparator, oscillator,...) in association with external components (R, C, crystal),
- the adjustment of the power consumption of the filter by means of the external resistance tied between the positive supply terminal V^+ (or ground) and the corresponding pin of the circuit (PWF). The power consumption can thus be choosen to match the particular application.
- The stand-by mode is obtained by strapping pin PWF to the negative supply terminal V^-,
- the adjustment of the power consumption of the two operational amplifiers, obtainable exactly as for the previous case but via the pin PWA of the circuit.

Figure 5 : Block Diagram of the Construction Chosen by SGS–THOMSON.



Principal Characteristics :

The principal characteristics of product TS85XX are as follows :

- technology : HCMOS1 (high density linear CMOS)
- available order : 2 to 8 (whatever the type of M.P.F.)
- input signal frequency : 0 to 30kHz
- internal sampling frequency : 0.5 to 1000kHz (depends upon the M.P.F. under consideration)
- ratio between internal sampling frequency and cut-off frequency : 10 to 200 (depends upon the M.P.F. under consideration)
- response curves (amplitude and phase) translatable by changing the sampling frequency
- signal to noise ratio : 70 to 85dB (depends upon the internal construction of the M.P.F.)
- power supply : ± 5V or 0-10V
- power consumption adjustable from 0.5 to 20mW per order
- capacitor ratio tolerance : 0.1%
- cut-off frequency tolerance : 0.5% (max)

THE SGS-THOMSON APPROACH

The SGS-THOMSON approach is to produce two types of M.P.F. : custom M.F.P.'s and standard M.F.P.'s.

CUSTOM M.P.F.'s :

SGS-THOMSON undertakes to deliver the first samples within 6 to 8 weeks maximum after the definition of the overall specification by the customer. All types of filters can be designed (BUTTERWORTH, LEGENDRE, BESSEL, CHEBYCHEV, CAUER,...) according to the general applications (low-pass, high-pass, band-pass, notch, group delay time correctors) or by simultaneous optimisation of the response curve both in amplitude and in phase. A special application note on the custom M.P.F. will explain later now to define all the specifications required to design a filter and how to choose among them according to the desired application.

STANDARD M.P.F.'s :

These constitute a family, currently of 11 circuits, which will expand in the future according to the evolution of the market requirements. Here is the description of this family :

Part Number	Function	Type	Order	Clock to Cutt-off Freq. Ratio	Stopband Attenuation
TS8510	Low-pass	CAUER	5	75.3	33dB (typ)
TS8511	Low-pass	CAUER	7	75.3	55dB (typ)
TS8512	Low-pass	CAUER	7	100	85dB (typ)
TS8513	Low-pass	CHEBYCHEV	8	60	80dB (typ)
TS8514	Low-pass	BUTTERWORTH	8	80	74dB (typ)
TS8530	High-pass	CAUER	3	320	15dB (typ)
TS8531	High-pass	CAUER	6	400	32dB (typ)
TS8532	High-pass	CHEBYCHEV	6	500	60dB (typ)
TS8540	Notch	(Q = 7)	8	930	
TS8550	Band-pass	CAUER (Q = 5)	8	60	
TS8551	Band-pass	Q = 35	8	187.2	70dB (typ)

N.B. : For other information, please consult the corresponding data sheets.

APPLICATIONS

GENERAL APPLICATIONS AROUND M.P.F. :

With this new concept of M.P.F., SGS-THOMSON is looking to cover all applications covering standard filters (passive, active) involved in the processing of analog signals.

Amongst these, telecommunications (modem, PABX, telephone line, signaler, mobil telephone), data acquisition (before A/D conversion and after D/A conversion), speech (detection, analysis, storage), portable instrumentation (geophysics, biomedical) and specially industrial applications (process control, servomotor control, remote control). For all these applications, each filter function is reduced to one M.P.F. derived either from the standard range of M.P.F. or from custom design M.P.F.'s, according to the requirements of the equipment.

HARDWARE IMPLEMENTATION AROUND M.P.F. :

TYPICAL USE OF THE M.P.F. (figure 6) : The M.P.F. is fed in dual supply : ± 5V.

The adjustment of the DC output level of the M.P.F. is achieved by an external voltage source (for example, a bridge divider connected between the positive and the negative power supplies and whose the middle point is connected to the LVL pin of the M.P.F.). If no output DC adjustment is required, the LVL pin can be directly connected to GND.

The consumption of the filter can be also adjusted by means of an external resistance connected between V^+ (or GND) and the PWF pin of the circuit.

The consumption can thus be chosen to match the particular application.

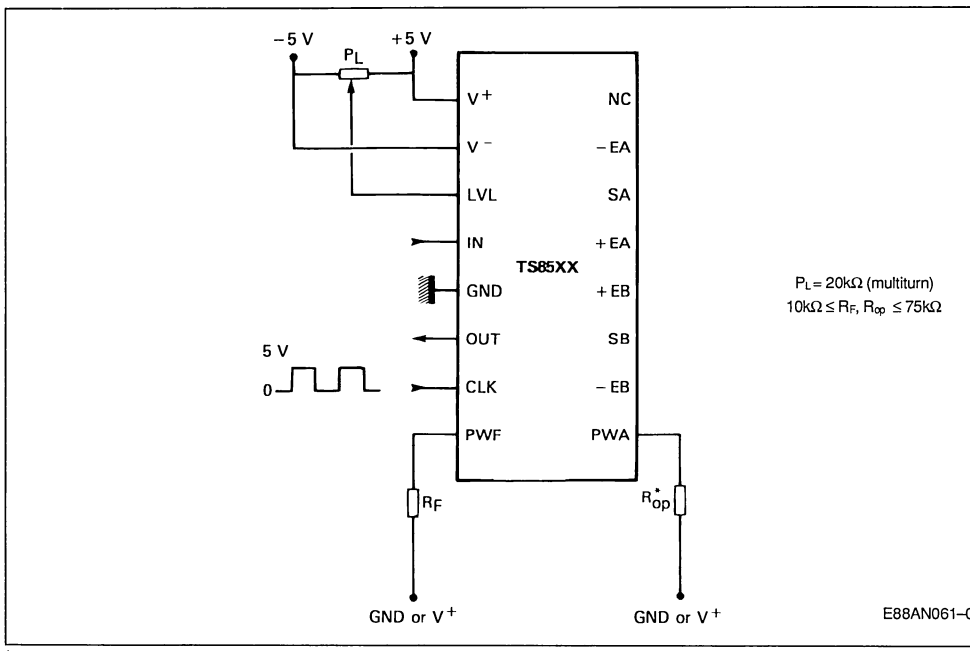
The stand-by mode is obtained by strapping the PWF pin to V^- (or non connected).

The adjustment of the power consumption of the two operational amplifiers can be achieved exactly like for the previous case, but via the PWA pin of the circuit. The stand-by mode is also obtained by strapping the PWA pin to V^- (or non connected).

The clock levels are TTL, but CMOS levels are accepted.

With these previous conditions, the output linear dynamic range of the M.P.F. is about 8V, between – 4.5 and 3.5V.

Figure 6 : Typical Use of the M.P.F. (± 5V).



* If the OP AMPS. are not used, R_{op} must not be connected between PWA and GND (or V^+).

USE OF THE M.P.F. WITH 0-10V (figure 7) : The M.P.F. is fed in single supply : 0-10V.

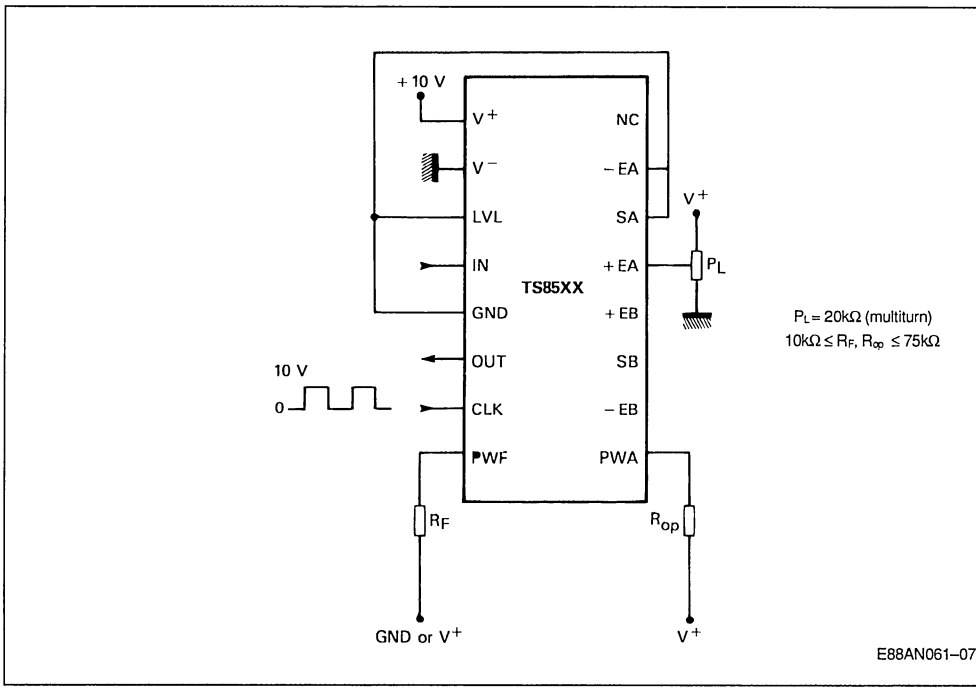
In this case, V^- is the reference ground of the circuit and GND must be adjusted to + 5V by means of the potentiometer P_L (V^+ - V^-)/2).

The adjustments of the DC output level of the M.P.F., of the power consumptions of the filter and of the operational amplifiers can be achieved exactly like previously.

The high level of the clock must be at least 1.4V upper the GND level.

With these previous conditions, the output linear dynamic range of the M.P.F. is about 8V between 0.5 and 8.5V.

Figure 7 : Use of the M.P.F. with 0–10V.



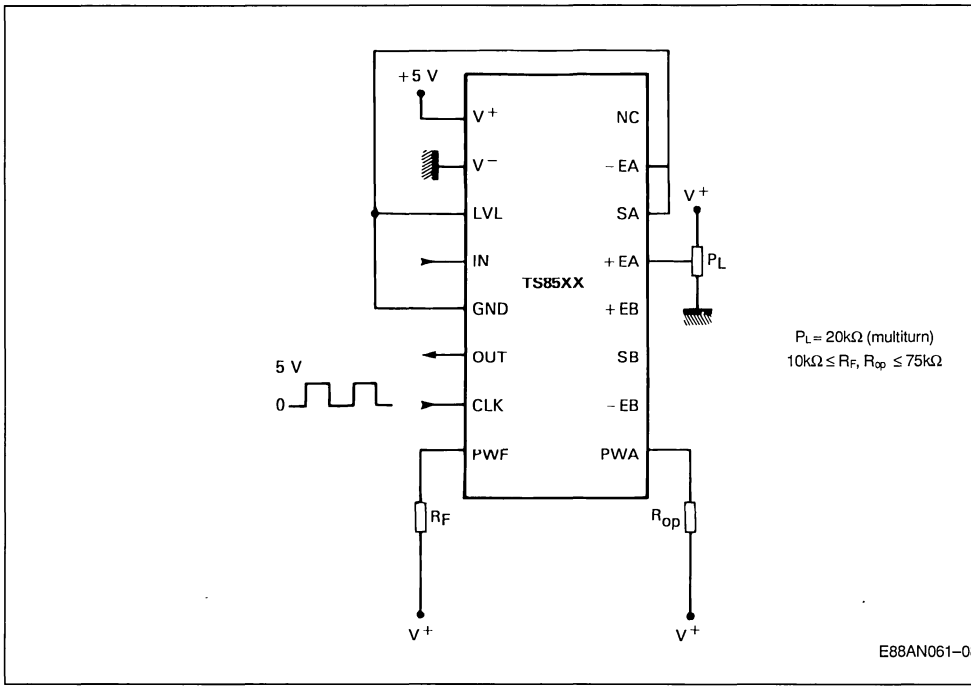
USE OF THE M.P.F. WITH 0-5V (figure 8) : The M.P.F. is fed on in single supply : 0-5V.

In this case, V^- is the reference ground of the circuit and GND must be adjusted to + 2.5V by means of the potentiometer P_L ((V^+ -V^-)/2).

The other adjustments are achieved exactly like previously except for bias resistances of the filter and of the operational amplifiers (Rf and Rop), whose must be exclusively connected to V^+.

The clock levels must be TTL levels. With these previous conditions, the output linear dynamic range of the M.P.F. is about 2.2V, between 1.2 and 3.4V.

Figure 8 : Use of the M.P.F. with 0–5V.



ANTI-ALIASING AND SMOOTHING :

- Anti-aliasing : the switched capacitor filters are sampled systems and must verify the SHANNON condition imposing a sampling frequency (Fs) equal, at least, to the double of the upper frequency (Fc) contained in the spectrum to transmit. With this condition, no information is added or lost on the transmitted signal. This theorem describes the well-known phenomenon called spectrum aliasing shown figure 9, where the entire spectrum to transmit appears around Fs, 2 Fs, 3 Fs,... and so on. Thus, all spectrum components of the signal contained around these frequencies are transmitted by the M.P.F., oppositively to the desired result.
  To cancel the effects of this phenomenon, it is required, before all sampled system, to filter all the spectrum components of the input signal upper than Fs-Fc. An analog filter, called "anti-aliasing filter", must be therefore applied before the M.P.F.
  The selectivity of this filter depends upon the Fs/Fc ratio.
  If Fs/Fc > 200, a RC filter (first order low-pass) is sufficient.
  If Fs/Fc < 200, a SALLEN-KEY structure (second order low-pass) must be used.
  This structure and its relationship are described figure 10. In these relationship, Fc is the cut-off frequency desired of the anti-aliasing filter and ξ its damping coefficient. For a cut-off as tight as possible and without overvoltage around it, ξ must have a value around 0.7.
  N.B. : If Fs/Fc < 2 (figure 11), the spectrum to transmit and the spectrum aliased have a part in common and it becomes impossible to share the useful signals from the undesirable signals.
- Smoothing : as the signal obtained as the output of the M.P.F. is a sampled and hold signal, it is often required to smooth it. This smoothing filter can be achieved from the SALLEN-KEY structure previously described (figure 9).

Figure 9 : Phenomenon of the Spectrum Aliasing.

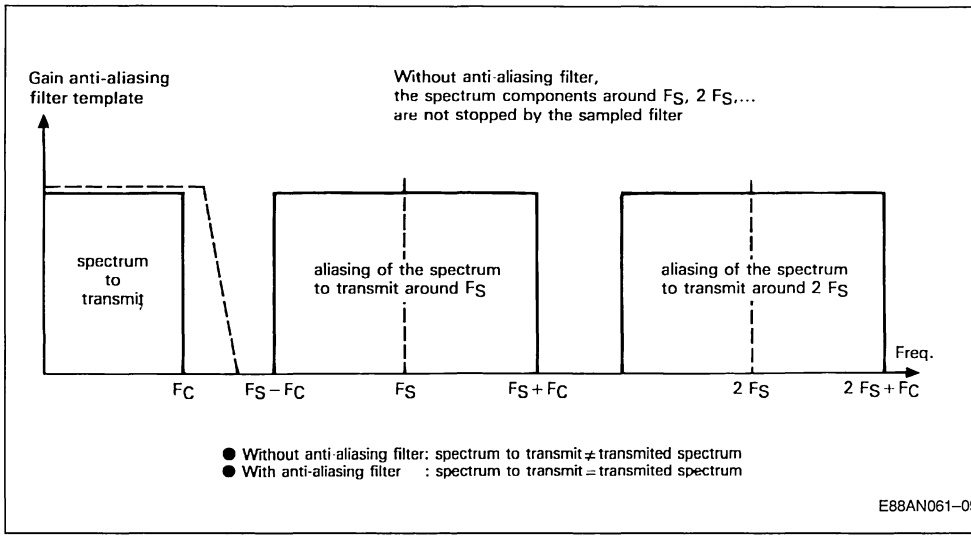
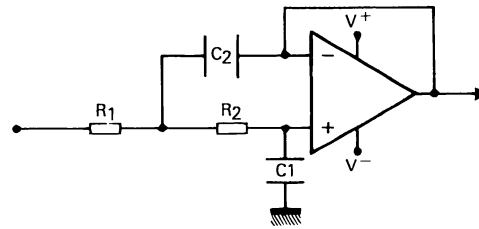


Figure 10 : Sallen–key (second order low–pass filter) for Anti–aliasing and Smoothing.



$R_1 = R_2$ = arbitrary value
F_c = cut–off frequency desired
ξ = damping coefficient

$$C_1 = \frac{\xi}{2\pi R_1 \times F_c}$$

$$(C_1 = \xi^2 \times C_2)$$

$$C_2 = \frac{1}{2\pi \xi R_1 \times f_c}$$

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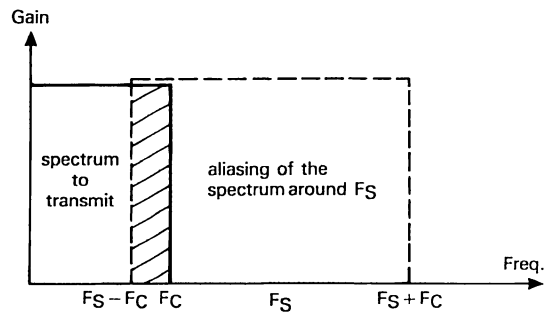
Figure 11 When Fs/Fc<2, the spectrum components including between Fs–Fc and Fc and which are due to spectrum aliasing are not stopped by the sampled filter.



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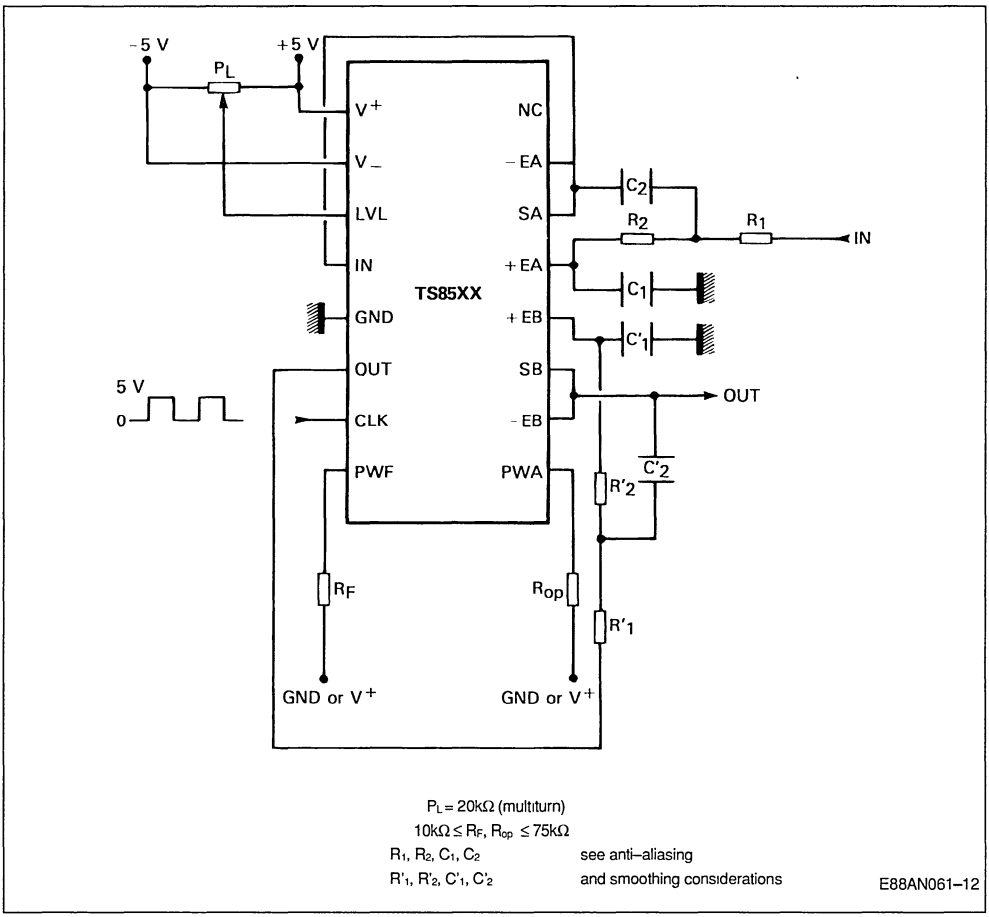
- Hardware implementation : in order to make easier anti-aliasing and smoothing, SGS-THOMSON has designed, on the even chip of the M.P.F., two general purpose operational amplifiers. A few external components are therefore sufficient to achieve these functions (figure 12).

Figure 12 : M.P.F. with Anti–aliasing and Smoothing Filters.

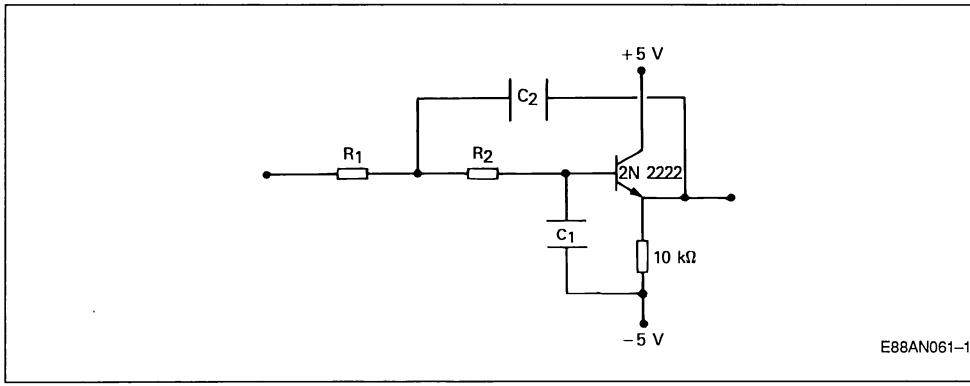


On the other hand, it the most M.P.F.'s, a special integrated cell is included in the chip (cosine filter) to reduce the aliasing effects around Fs.

Nonetheless, if the application allow it, these two operational amplifiers can be used to implement other functions (gain, comparator, oscillator,...).

In this case, the circuit shown figure 13 can be used as anti-aliasing or smoothing filter. This structure is the same as the SALLEN-KEY structure described figure 9 (second order low-pass), in the same way as the corresponding relationship.

Figure 13 Second Order Low–pass Filter (sallen–key structure) with a transistor replacing the operational Amplifier.



IMPLEMENTATION OF THE M.P.F. CLOCK FROM EXTERNAL COMPONENTS (figure 14) :

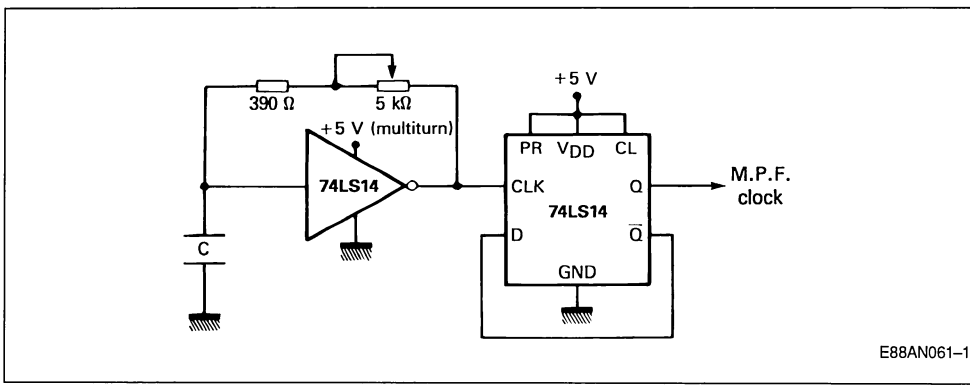
A mouting with a minimum of external components allows to achieve the clock required for the M.P.F.

The value of the frequency obtained with this mounting depends upon C value, as shown on the following board :

C(nF)	47	15	6.8	2.2	1	0.47	0.33	0.22
$\mathbf{F_s}$ **min** (kHz)	1.5	4.3	6.7	30	44	84	126	172
$\mathbf{F_s}$ **max** (kHz)	16	48	183	305	1020	1750	2430	3010

N.B. : The accuracy of these values is 20%, according to the usual resistor and capacitor accuracy.

Figure 14 : M.P.F. Clock Achieved from External Components.



APPLICATION EXAMPLE : FREQUENCY DETECTION :

The principle of this type of application is as follows : a sinewave (amplitude x, frequency f) modulated by digital information is superposed to an other signal, that we shall call the main signal. To better understand and illustrate this example, we shall take the hypothesis of a main signal equally sinoidal (amplitude X, frequency F) and we shall assume that X >> x and F < f (T > t). Thus, the main signal is modulated by frequency f during high level (+ 5V) and not modulated during low level (0V) of the bit to be transmitted. These wave trains can, for example, correspond to commands that must be received and then understand by a microprocessor in a suitable format for their processing.

Therefore, these wave trains must be detected and then applied to the microprocessor in form of logic pulse, of which high levels (+ 5V) correspond to the presence and low levels (0V) to the absence of the waves.

In this type of application, two factors are of prime consideration, namely : selectivity and size. Both transmission channel and transferred data being prone to noise, the M.P.F. must be adequately selective to reject the unwanted frequencies close to the center frequency f. On the other hand, as far as the industrial aspect of the application is concerned, the size is considered to be of major importance since it is impractical to envisage a large area to accomodate only the filtering section.

Let's consider the general diagram of figure 15. By using a suitable sampling frequency (Fs), the M.P.F. can have a center frequency equal to f.

Since TS8551 is a highly selective filter and the modulated wave has a very stable frequency, the M.P.F. will only filter out the main signal (frequency F) and let through the modulated signal (frequency f). An attenuator stage and an anti-aliasing analog filter are required preceeding the M.P.F. The attenuator stage is used to match the amplitude of the main signal (X) to the input characteristics of the M.P.F., and the analog filter to prevent the M.P.F. from passing the frequency spectrum of the incident wave aliased around Fs. At the output of the M.P.F., the combination of a first order high pass CR filter and a negative voltage clipping diode will produce a sinewave of frequency f and amplitude v. Following this filter, an amplifier of gain G > 1 also delivers a sinewave signal of frequency f but of amplitude V = G x v.

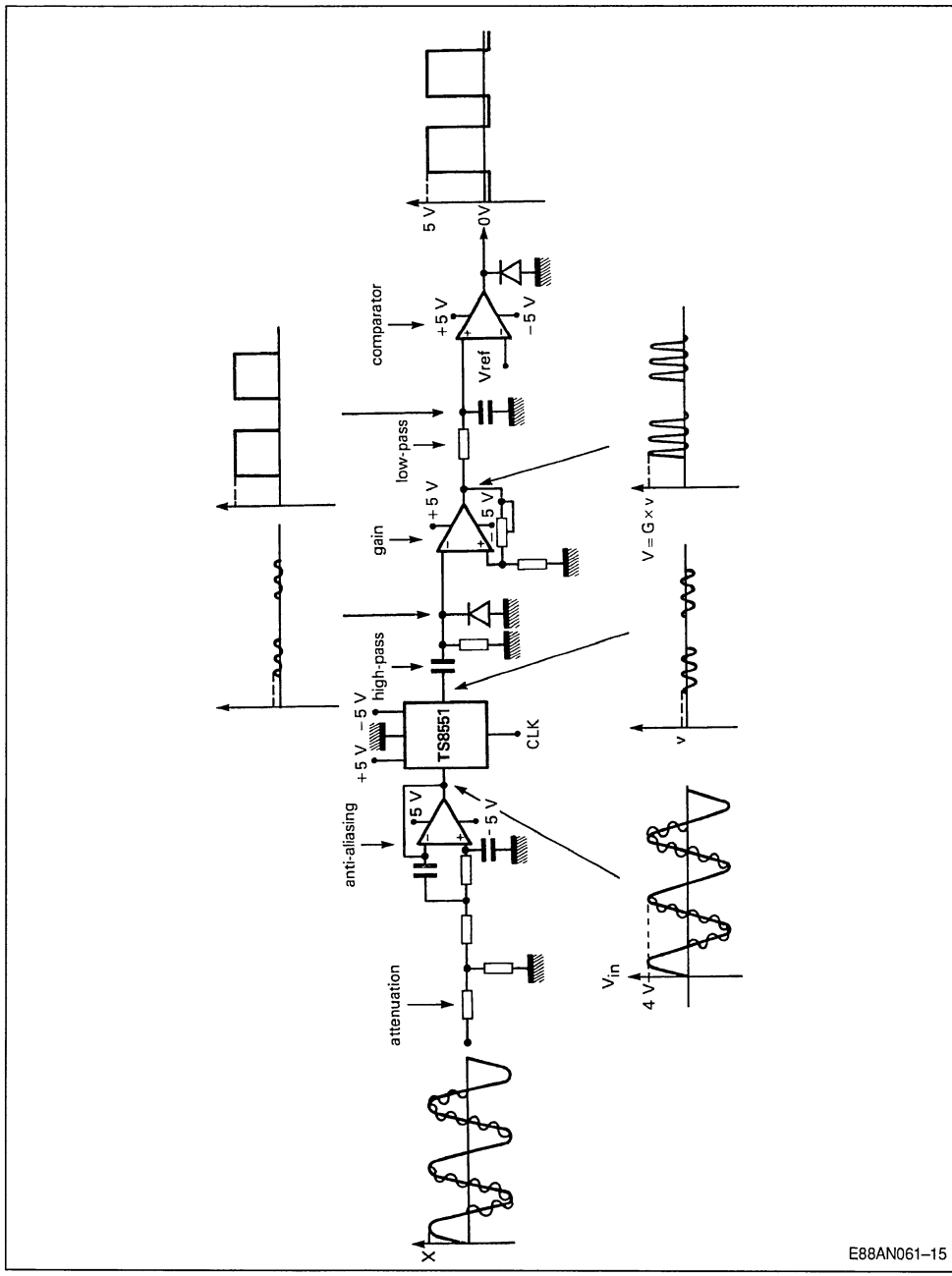
The following first order low pass RC filter detects the enveloppe of the amplified signal and then compares it with a reference voltage Vref.

If V > Vref, the output of the operational amplifier goes to the positive saturation state (+ Vsat) thereby indicating the presence of the wave, whereas if V < Vref, then the amplifier goes to the negative saturation state (- Vsat) to indicate the absence of the wave. A negative voltage clipping diode at the output of the comparator will provide a succession of high (+ 5V) and low (0V) states producing a pulse train. The period and the duration of this pulse train inform the microprocessor of the precise nature of control signal sent.

CONCLUSION

This unique example is sufficient to demonstrate the outstanding application possibilities offered by the M.P.F. Many other features were also discussed in various sections of the present article. Relying on these established facts, SGS-THOMSON is ready to provide an answer to every filtering problem in any application. Due to its remarkable and unlimited possibilities, the M.P.F. concept is estimated to become, in a very near future, as widely employed as gate-arrays and mask programmable ROM microcomputer devices are nowadays.

Figure 15 Example of an Application of the M.P.F. with a very Selective Band–pass Filter : the Frequency Tracking.



SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE

A SUPPLEMENT TO THE UTILIZATION OF SWITCHED CAPACITOR FILTERS

INTRODUCTION

This application note is a complement to the **"Application Note AN-061"** which introduced the range of switched capacitor filters manufactured by SGS-THOMSON Microelectronics and discussed the following topics :

- **Anti-aliasing & Smoothing filters**
- **Ground pin biasing techniques using a single supply voltage**
- **dc output level adjustment**

The present application note outlines and provides an in-depth discussion of other important factors related to the use of switched capacitor filters, namely :

- **Gain adjustment**
- **dc output level locking**
- **Oscillators**
- **Regulated power supply**
- **Wiring & Layout recommendations**

Information contained in various sections will yield cost-effective solutions and enable the designer to take full advantage of the outstanding performances offered by SGS-THOMSON' range of **Switched Capacitor Filters** ; **TSG85XX**, **TSG86XX**, **TSG87XX Standard Series** and **Semicustom Filters**.

GAIN ADJUSTMENT

Majority of standard SGS-THOMSON filters have an inherent pass band gain of approximately 0dB. In certain applications however, a larger gain value combined with the gain adjustment possibility is required.

Gain adjustment can be accomplished using one of the operational amplifiers available in the same package as the filter circuit.

Two cases are discussed next :

- **Operational amplifier used for gain adjustment**
- **Sallen-Key Cell with gain adjustment**

USING AN OPERATIONAL AMPLIFIER

This is the most straightforward solution. Amplifier configurations are commonplace and well-known. The two main arrangements are illustrated next.

Figure 1 : Inverting Configuration.

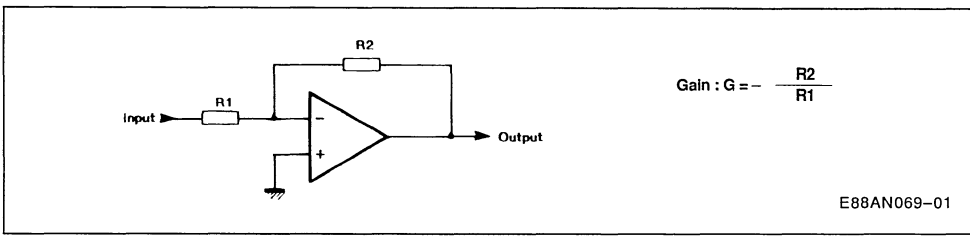
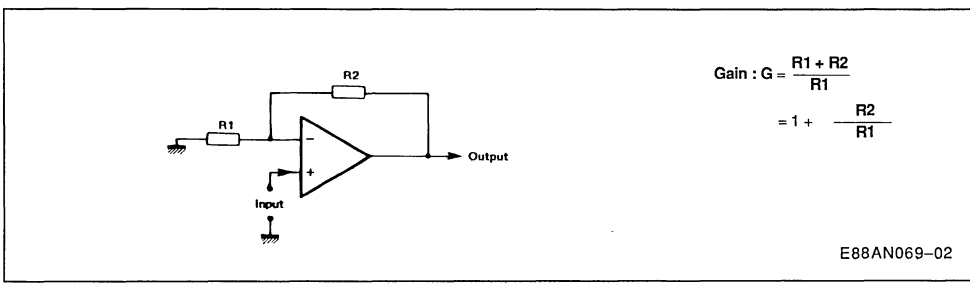


Figure 2 : Non–Inverting Configuration.

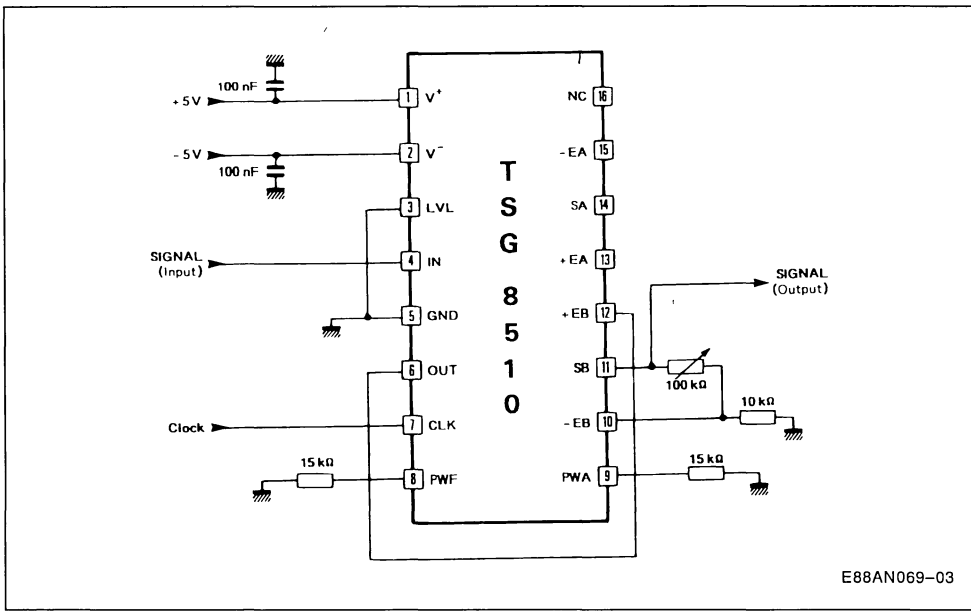


This type of configuration yields high gain values. Only limitations are those related to the electrical characteristics of the operational amplifiers such as : gain-bandwidth-product "2MHz typ." or the output voltage range "–4.2V, + 3.5V" (values measured using symmetrical – 5V, + 5V power supplies).

Figure 3 illustrates the arrangement of a non-inverting configuration.

In order to obtain an enhanced signal-to-noise ratio, the amplifier is directly coupled to the filter output which will reduce the noise spectrum.

Figure 3 : Gain Adjustment.



SALLEN-KEY CELL WITH GAIN ADJUSTMENT

In some applications, the operational amplifiers available within the filter circuit may be already used to implement anti-aliasing and smoothing filters generally required for switched capacitor filters.

In this case, the smoothing filter can be implemented using a second order Sallen-key cell with a gain higher than 1. Figure 4 depicts this arrangement and figure 5 illustrates an example of the actual configuration.

Figure 4 : General Arrangement of a Sallen–Key Cell (with gain adjustment).

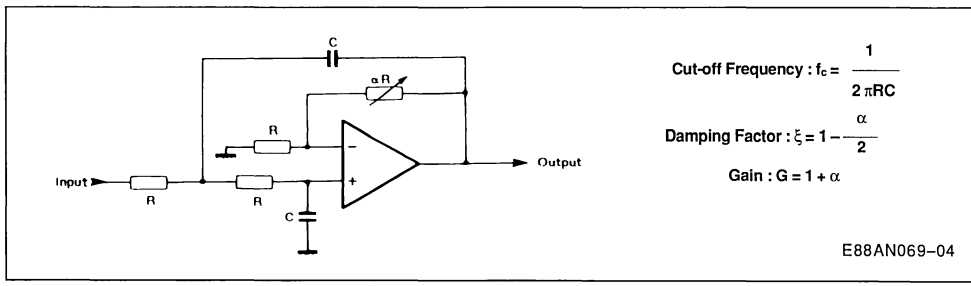


Figure 5 : Sallen–Key Cell (with gain adjustment).

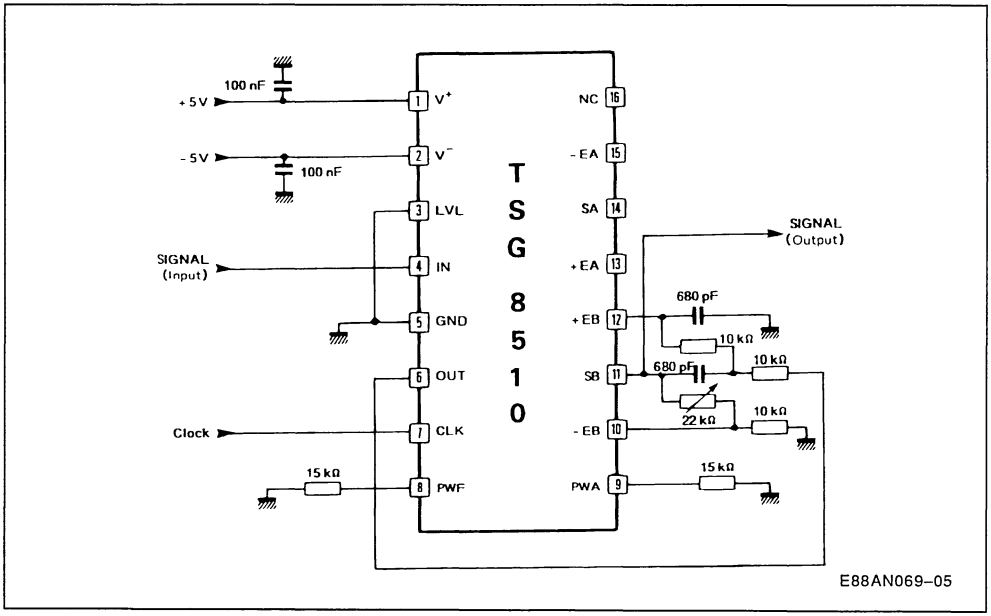
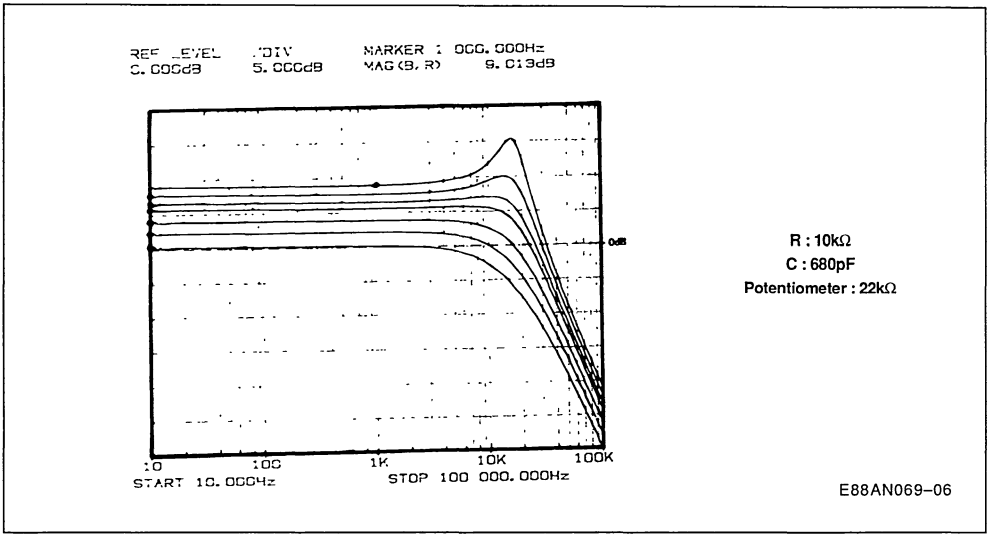


Figure 6 outlines the response curves of the Sallen-key cell obtained at various potentiometer settings, i.e. at different gain values.

Figure 6 : Frequency Response of Sallen–Key Cell (with gain adjustment).



It is clear that the damping factor varies as a function of α.

This configuration provides gain values of up to 6dB without any appreciable overshoot in the response curves.

FILTER OUTPUT DC LEVEL LOCKING

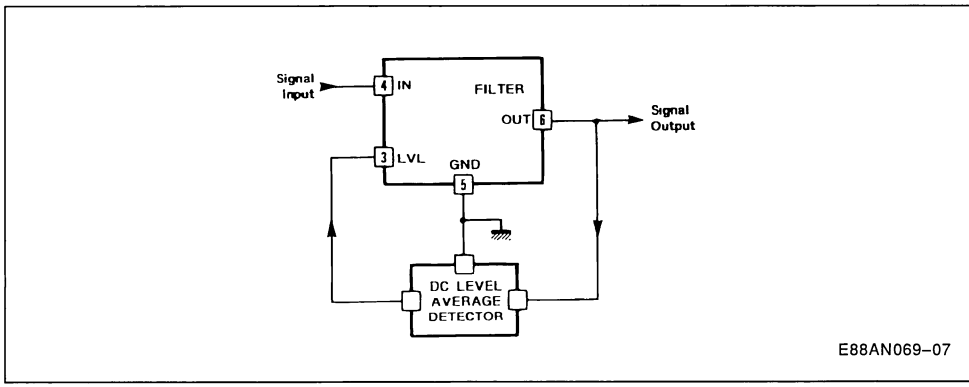
Switched capacitor filters manufactured by SGS-THOMSON feature a **"Level"** (**LVL**) terminal for the adjustment of the output dc level.

This function is accomplished by applying to this pin, a dc signal corresponding to the desired output dc level. Characteristic curves labeled "**Output voltage** versus **voltage on LVL pin**" are used to determine the value of the voltage to be applied to LVL terminal. This curve is available in each filter technical data sheet. In general, the voltage applied to "**LVL**" pin and hence the filter output level, is set by a potentiometer inserted between V^- and V^+ potentials.

The output level is generally set a 0V or at "**Ground**" (**GND**) pin potential.

In this case, an "**automatic offset compensation**" feature may be implemented as illustrated in figure 7.

Figure 7 : Automatic Offset Compensation.



The detector has a very low cut-off frequency in order to detect the output dc level and to control it through "**LVL**" pin.

According to the filter type, two cases are possible :

THE DC OUTPUT VOLTAGE IS DIRECTLY PROPORTIONAL TO THE VOLTAGE APPLIED TO "LVL" PIN

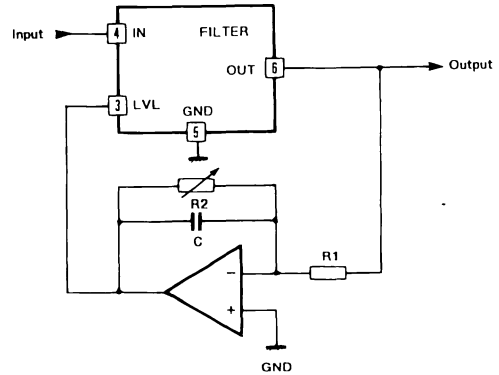
In this case, the output signal polarity should be inverted for feed-back functions.

A conventional integrator configuration using operational amplifier may be used for this purpose. This configuration is given in figure 8.

The feed-back loop behaves as an integrator at frequencies very much higher than the cut-off frequency $\frac{1}{2\pi \times R2 \times C}$

The dc gain is " $-\frac{R2}{R1}$ " and may be adjusted by modifying the value of the either resistor ; thus allowing accurate control of precision and response.

Figure 8 : Output dc Level is inverted and Feedback to "LVL" Pin for Automatic Offset Compensation.

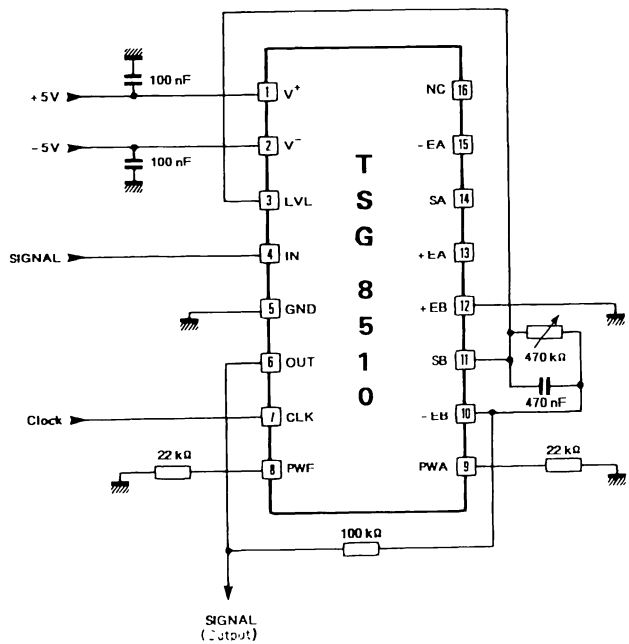


E88AN069–08

Here, we have chosen to adjust the value of R2 resistor, so that when R2 value is increased the gain also increases, but the cut-off frequency falls. Therefore, any risk of instability occurrence at high gain is eliminated.

Figure 9 depicts the practical application diagram. As shown, the feed-back network is readily implemented using one of the operational amplifiers available within the filter package.

Figure 9 : Automatic Offset Compensation.

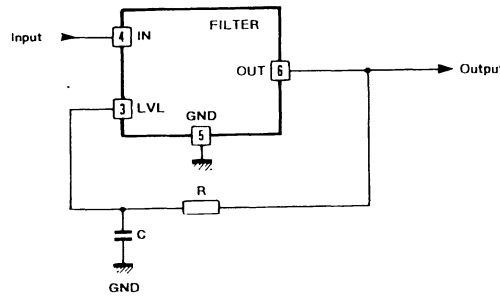


E88AN069–09

THE DC OUTPUT VOLTAGE IS INVERSELY PROPORTIONAL TO THE VOLTAGE APPLIED TO "LVL" PIN

The output signal no longer requires polarity inversion and the arrangement is simplified to a conventional RC integrator as shown in figure 10.

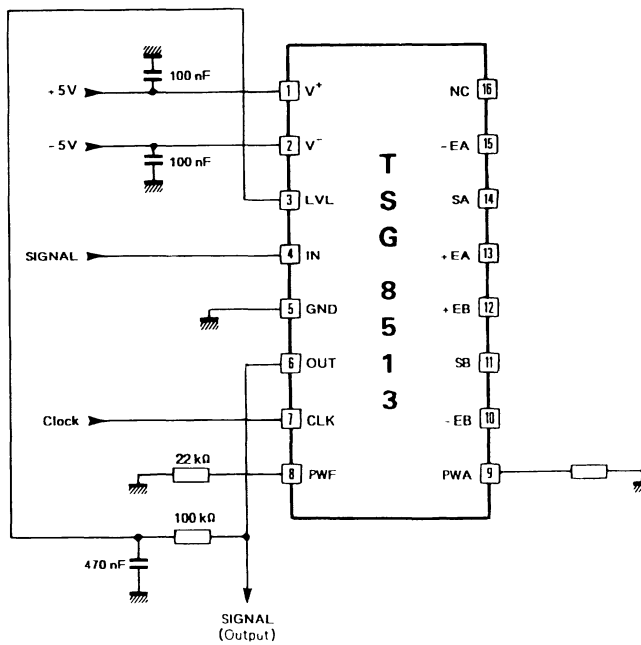
Figure 10 : Only a R–C Cell (1st order low–pass) is needed for Automatic Offset Compensation.



E88AN069–10

The RC time constant should be selected to be high in comparison to the period of the signal transmitted through filter. Due to low output filter impedance and high input impedance of R-C cell, the output signal is not subjected to any disturbance.
Figure 11 outlines the practical application diagram.

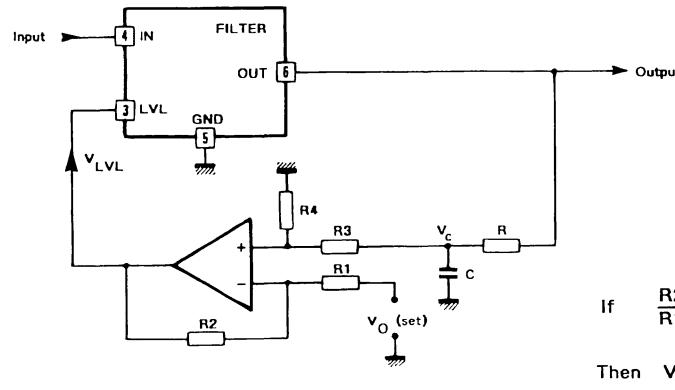
Figure 11 : Automatic Offset Compensation.



E88AN069–11

A non-inverting operational amplifier configuration may be used, if feed-back loop gain control is required.

Note : "**LVL**" pin voltage can be locked onto any variable voltage by following the same procedure as mentioned earlier - i.e. output signal detection followed by the amplification of the difference signal measured between the output voltage and the adjustable control voltage.



If $\frac{R2}{R1} = \frac{R4}{R3}$

Then $V_{LVL} = \frac{R2}{R1}(V_O - V_C)$

E88AN069–12

CLOCK OSCILLATORS

Switched capacitor filters require an external clock for operation. This clock sets the internal sampling frequency of the filter and also determines the frequency range. The clock circuit is generally implemented using logic gates.

The Mask Programmable Filters of SGS-THOMSON feature two uncommitted operational amplifiers integrated on the same silicon chip that are available for functions related to filtering.

The objective of this section is to illustrate how one of these operational amplifiers may be configured as oscillator thereby providing the clock required for the switched capacitor filters.

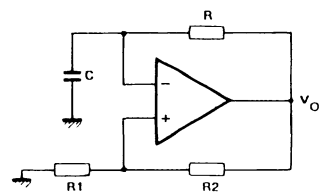
Two types of oscillator will be discussed :

- **RC-type free-running relaxation oscillators**
- **Crystal-controlled oscillators** (Quartz or Ceramic Resonator)

FREE-RUNNING RELAXATION OSCILLATORS

This type of oscillator relies on the principles of a capacitor "C" charge-up and discharge through a resistor "R" as shown in figure 12.

Figure 12 : Free–Running Multivibrator.



E88AN069–13

When the output voltage is positive, the voltage at the non-inverting terminal is $V_O \frac{R1}{R1 + R2}$ and the capacitor C begins charging through resistor R until the voltage at the inverting terminal becomes equal to the voltage at the non-inverting terminal i.e.,

$$V_O \frac{R1}{R1 + R2}$$

The amplifier is then triggered, its output falls to low saturation level, C is discharged via R until the inverting input becomes once again negative with respect to the non-inverting input. Then the output voltage returns to the high saturation value and the entire cycle is repeated. If high and low saturation levels have the same absolute values, the oscillator output signal would have the following characteristics :

- Duty Cycle : 0.5
- Period : $T = 2RC \log (1 + 2\frac{R1}{R2})$

In this case, the oscillator period is :

$$T = R\,C \log \left[1 + \frac{R1}{R2}\left(1 - \frac{V^+_{sat}}{V^-_{sat}}\right)\right] + R\,C \log \left[1 + \frac{R1}{R2}\left(1 - \frac{V^-_{sat}}{V^+_{sat}}\right)\right]$$

Where V^+_{sat} and V^+_{sat} are respectively high and low saturation voltages of the operational amplifier. V^+_{sat} and V^-_{sat} are given in data sheets :

$V^+_{sat} = +3.5V$, $V^-_{sat} = -4.5V$ for TSG85XX and + 5V, – 5V power supply.

Electrical configurations are given in figures 16 and 17 that illustrate how by using currently available components, a low-cost and perfectly stand-alone filter application is implemented.

Figure 17 illustrates the application using a single + 10V or + 5V power supply. In this case, the second operational amplifier is configured as voltage follower and used to bias "**Ground**" and "**Level**" pins.

Clock signal waveforms generated by this type of multivibrator are depicted in figures 14 and 15.

The oscillogram of figure 14 is the waveform obtained using – 5V, + 5V power supplies and shows in particular how the output signal may go negative.

Thanks to its **integrated clock shaping stage**, the filter can accept this negative going signal - thus offering an outstanding flexibility for the implementation of clock oscillators.

It is clear that since C has a fixed value, the frequency of this multivibrator is readily set by adjusting the value of R (potentiometer).

If high and low saturation voltages are not identical, these values will be taken into consideration in the above expression for period calculation and the value of the duty cycle will no longer be 0.5. In addition, the frequency and the amplitude of the output signal will both vary as a function of the operational amplifier power supply. A good frequency and amplitude stability is achieved using two zener diodes to limit the output signal excursion.

In the case of SGS-THOMSON filters, the saturation voltages have different absolute values as illustrated by the oscillogram of figure 14 and the duty cycle has a value different from 0.5 mentioned earlier. This is not however an important matter as the filter circuit contains a clock shaping stage and can therefore accept directly the operational amplifier output signal.

The **TSG8550** filter was tested in various oscillator configurations and response curves obtained are depicted in paragraph 4.4 at the end of this section.

With reference to these curves, it is observed that the filter circuit operates ideally with the free-running oscillator discussed earlier.

Some curves also illustrate the filter response characteristics obtained using an external clock generated by conventional logic gates. Note that both curves are perfectly superimposed.

The foregoing discussion demonstrated that this type of oscillator offers satisfactory results irrespective of the power supply type : – 5V, + 5V – 0V, + 10V – 0V, + 5V.

Note also that this type of oscillator can operate at relatively high frequencies. In fact, the response curves of the **TSG8550** were obtained at oscillator frequencies of up to **1.2MHz** approximately. In this case however, one should use a low value biasing resistor (here, $R_{PWA} = 10k\Omega$), to obtain appropriate "**slew rate**" at the operating frequency.

Figure 13

EXTERNAL TTL–type CLOCK
(generated by logic gates)

2volts/division
2µs/division
E88AN069–14

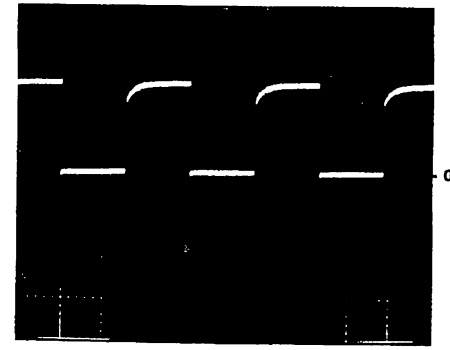


Figure 14

RC–type FREE–RUNNING OSCILLATOR
(using one of the filter op–amps)
[–5V, +5V power supplies]

2volts/division
2µs/division
E88AN069–15

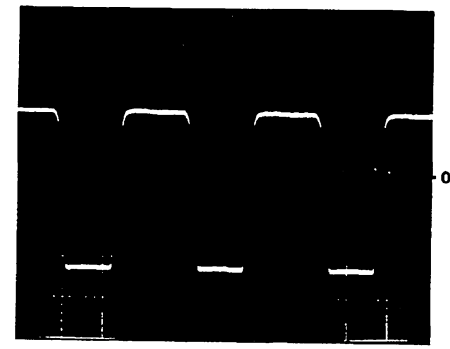


Figure 15

RC–type FREE–RUNNING OSCILLATOR
(0, +10V power supply)

2volts/division
2µs/division
E88AN069–16

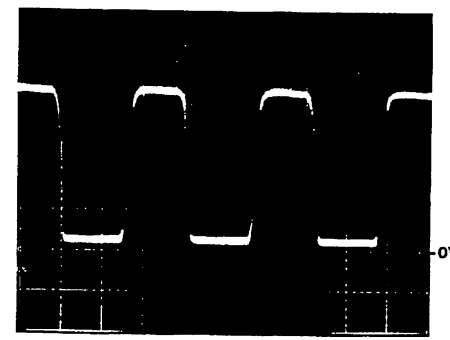


Figure 16 : RC–type Free–Running Oscillator (+5V, –5V power supplies).

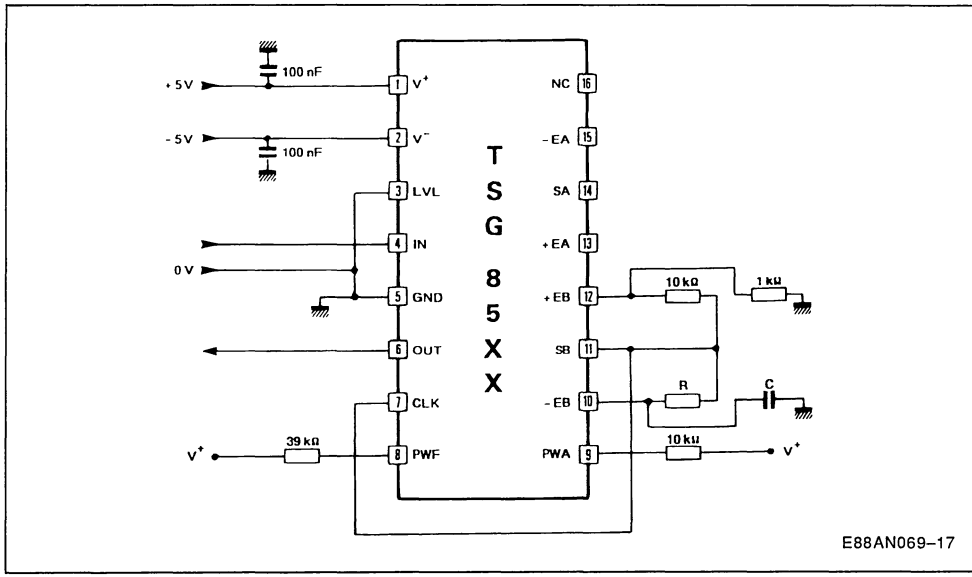
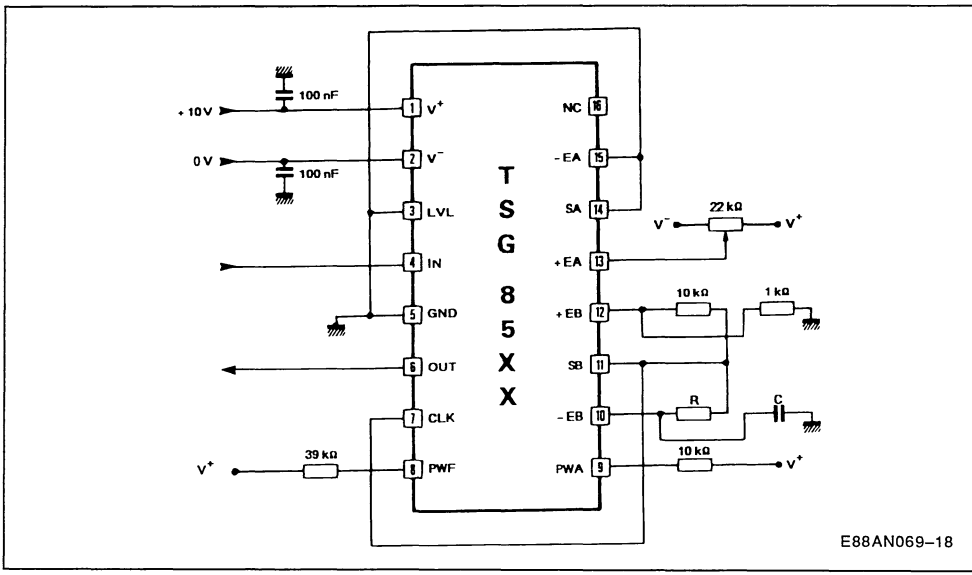


Figure 17 : RC–type Free–Running Oscillator (0, +10V or 0, +5V power supplies).



CRYSTAL-CONTROLLED OSCILLATORS (or Ceramic Resonator)

The multivibrator circuit described above is a low-cost oscillator providing satisfactory operation of the switched capacitor filters.
It has however two drawbacks :

- Frequency adjustment by a potentiometer
- Frequency variation with device power supply

Better frequency stability combined with simplicity of use will be obtained if a crystal-controlled oscillator is used for clock generation.

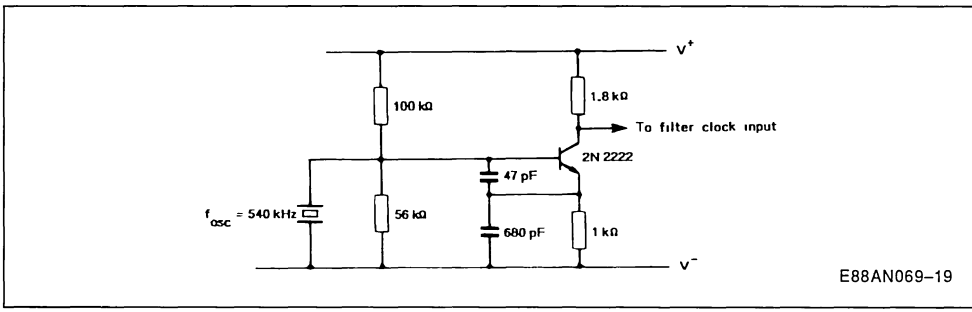
This solution is particularly interesting in applications not requiring any adjustment of the clock frequency ; as is the case of the most applications built around filters.

Note however that if frequency adjustment is required, one may either switch between various resonators or implement a master oscillator followed by a frequency divider circuit.

TRANSISTOR-BASED OSCILLATOR

In untuned oscillators, the crystal is most often operated in its fundamental mode. Figure 18 illustrates the arrangement of the oscillator to be discussed next.

Figure 18 : Crystal–controlled Oscillator.



This is a **Colpitts**-type **parallel resonance** oscillator. The operating point of the crystal is such that it behaves like a high Q choke. A capacitive bridge provides the energy required to initiate the oscillation.

This oscillator does not require any adjustment - its frequency is highly stable whatever the power supply mode (- 5V, + 5V - 0V, + 5V - 0V, + 10V).

Due to the operating frequency value of this application, a small signal "**general purpose**" transistor will be suitable.

Here, we have employed a **Ceramic Resonator** whose fundamental frequency is **fosc = 540kHz**.

This is a popular resonator used in particular as oscillator for SGS-THOMSON range of television circuits (time base, switching power supplies, chroma decoder, etc...) and is therefore available at low-cost "**consumer**" price.

The oscillogram of figure 19 illustrates the output signal waveform of this oscillator. Although its shape differs from that generated by a TTL clock as illustrated in figure 13, this is a negligible drawback as switched capacitor filters manufactured by SGS-THOMSON feature a built-in signal shaping stage on clock inputs.

Figure 19

COLPITTS OSCILLATOR WAVEFORM

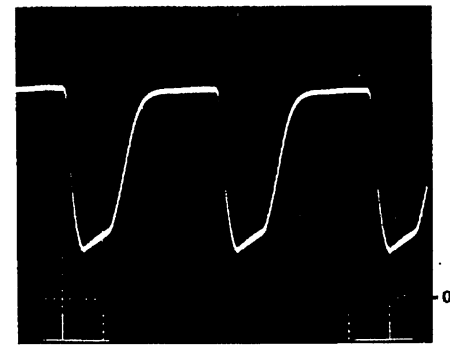
(ceramic resonator)

[0, +5V power supply]

1volt/division

0.5ms/division

E88AN069-20



Various response curves obtained employing this oscillator in combination with **TSG8550** filter operated at different power supply modes, are given at the end of this section in paragraph 4.4.

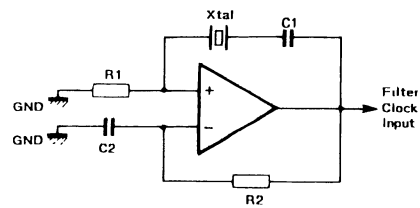
Similar procedure was applied but using an external clock generated by TTL-type logic gates. It is seen that there is no significant difference between the curves obtained in this case and those obtained previously.

It is therefore obvious that the filter operates satisfactorily with an external Colpitts-type oscillator.

OPERATIONAL AMPLIFIER-BASED OSCILLATOR

Figure 20 shows the general arrangement of this oscillator.

Figure 20 : Crystal–controlled Oscillator.



E88AN069-21

The above figure illustrates how a crystal-controlled oscillator is readily configured using one of the operational amplifiers available within the package of the switched capacitor filters of SGS-THOMSON.

The resonator is directly inserted within the positive feed-back loop. The oscillation is initiated when the transmission through crystal is at its maximum value, i.e. when the series resonance of the crystal occurs. High input impedance of the operational amplifier together with the blocking capacitor C1 contribute towards oscillator stability. The feed-back to inverting input through resistor R2 ensures oscillator start-up and dc stability.

The negative feed-back at high frequencies is attenuated by capacitor C2 whose value should be so selected to prevent the resonator from locking onto a partial mode. The non-inverting input is biased with respect to filters "Ground" pin potential.

Application diagrams are depicted in figures 21 and 23.

Figure 21 : Ceramic Resonator – Controlled Oscillator (–5V, +5V power supplies).

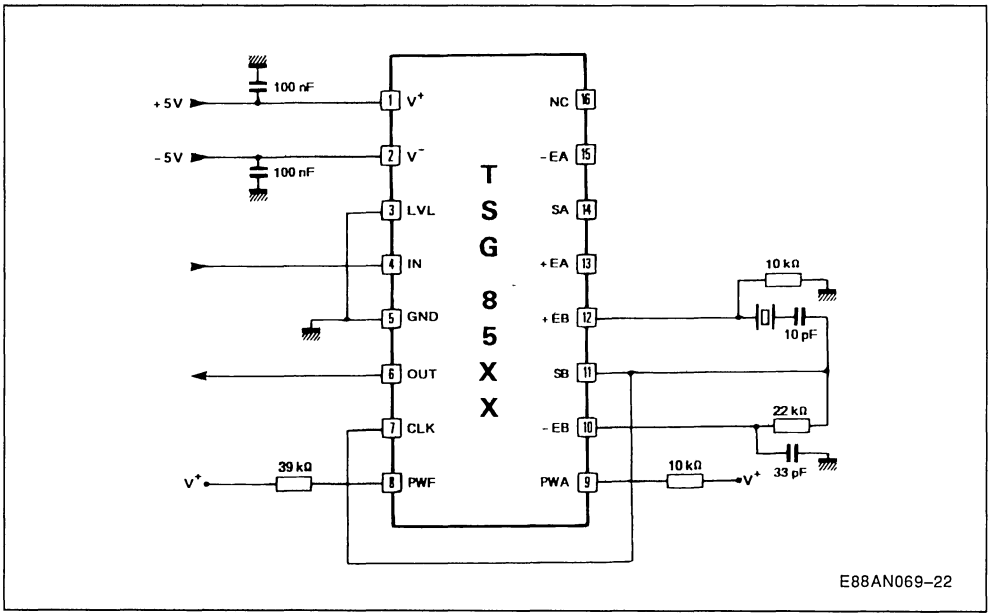
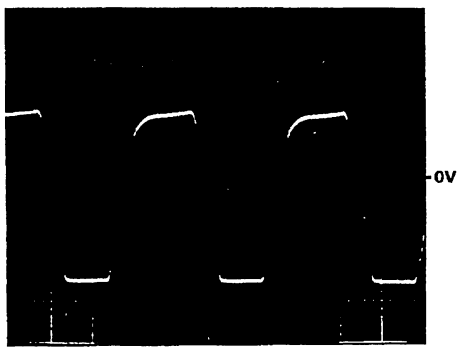


Figure 22

OSCILLATOR CONTROLLED BY CERAMIC RESONATOR

(using one of the filter op–amps)

[–5V, +5V power supplies]



2volts/division

0.5ms/division

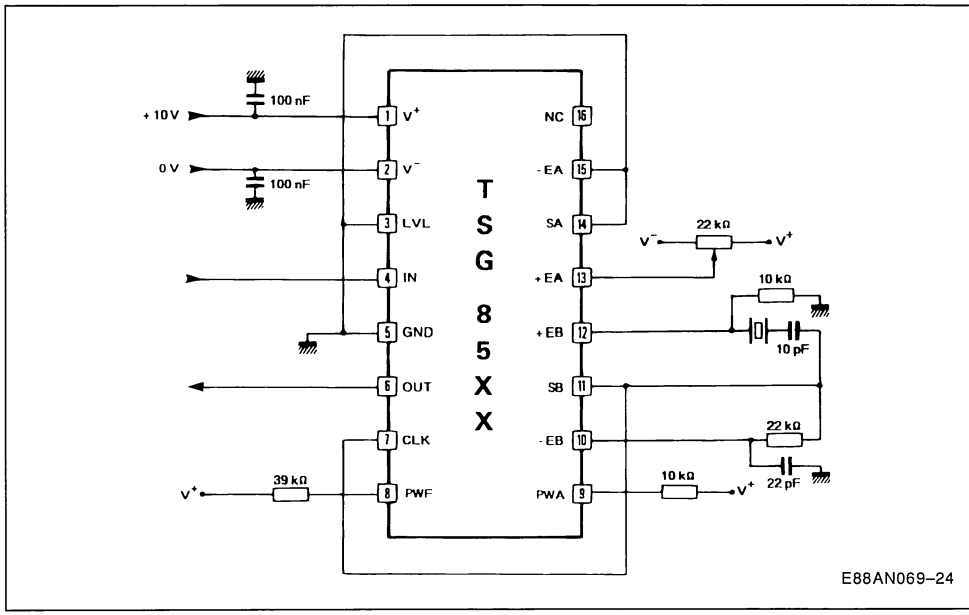
E88AN069-23

Figure 23 illustrates the application using a single power supply.

In this arrangement, the second operational amplifier configured as voltage follower is used to bias filter's "**Ground**" and "**Level**" pins.

Once again, the same "**consumer**" ceramic resonator running at f_{osc} = **540kHz** has been employed in this application.

Figure 23 : Ceramic Resonator – Controlled Oscillator (0, +10V or 0, +5V power supplies).



Oscillogram of figure 22 shows the clock signal waveform obtained from the application depicted in figure 21. Similar waveforms are obtained from the single supply voltage application illustrated in figure 23 - only the output voltage levels are different.

As shown in response curves of paragraph 4.4, the **TSG8550** filter operates satisfactorily with this type of oscillator. Once again, note that there is no difference between the curves obtained using this oscillator and those using an external TTL-type oscillator.

Obviously, operation at other frequencies is possible by using different ceramic resonators. The basic configuration remains the same however.

CONCLUSION

The discussion throughout this section demonstrated how, a clock oscillator is readily built, and a perfectly stand-alone filter implemented, using only a single integrated circuit.

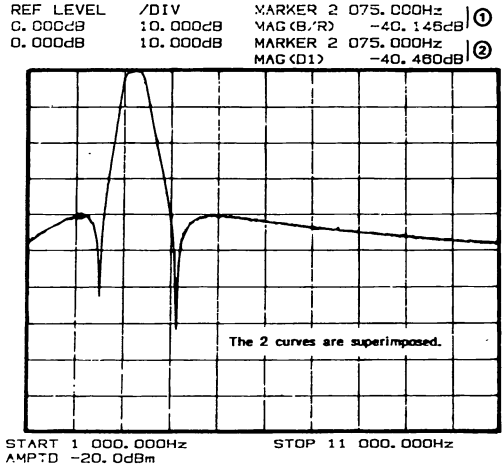
- In applications where frequency adjustment facility is required and price is the prime objective, **RC-type free-running** oscillators are recommended.
- **Crystal-controlled** oscillators are suitable for applications requiring highly stable fixed oscillator frequencies.
- Finally, the oscillator using a single **transistor** allows use of an **8-pin filter** package or to save the two operational amplifiers of the filter for other functions - thereby simplifying the application configuration.

These results have been obtained thanks to the highly efficient and flexible clock input terminal of SGS–THOMSON' **Switched Capacitor Filters**.

All of the oscillators covered in this section, are in addition to TSG8550, also suitable for use with other **standard filter** types and **semicustom filters**.

TSG8550 RESPONSE CURVES USING DIFFERENT CLOCK OSCILLATORS

Figure 24 : RC–Multivibrator Operation (at 153kHz and +5V, –5V power supply).



TSG8550

Power Supply : –5V, +5V

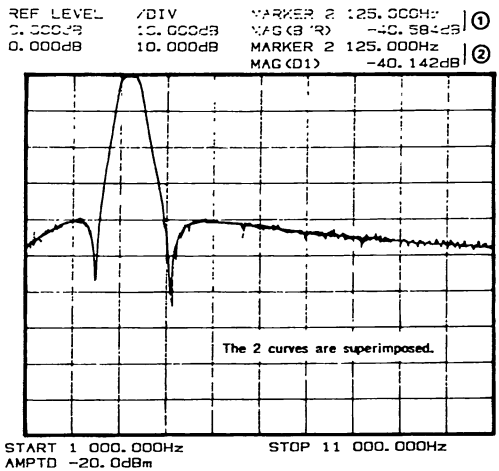
Clock Frequency : 153kHz

1– External Clock
2– Free–running Oscillator
R : 2.5kΩ
C : 3.3nF

The RC Multivibrator is implemented with an internal Operational Amplifier

E88AN069–25

Figure 25 : RC–Multivibrator Operation (at 0V, +10V power supply).



TSG8550

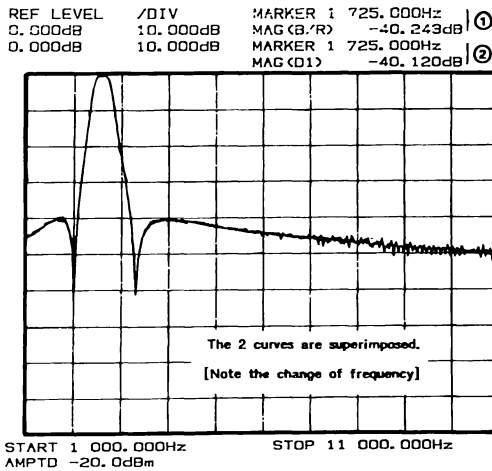
Power Supply : 0V, +10V

Clock Frequency : 153kHz

1– External Clock
2– Free–running Oscillator
R : 2.5kΩ
C : 3.3nF

E88AN069–26

Figure 26 : RC–Multivibrator Operation (at 0V, +5V power supply).



E88AN069–27

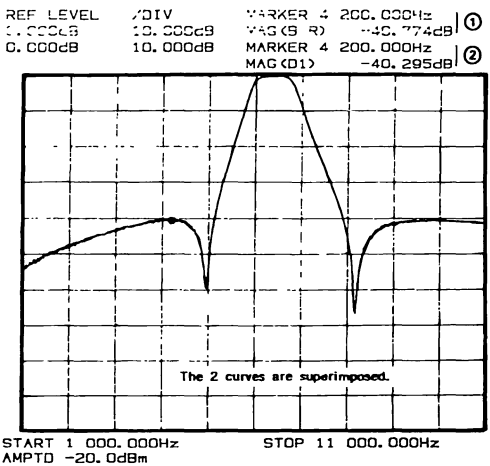
TSG8550

Power Supply : 0V, +5V

Clock Frequency : 123kHz

1– External Clock
2– Free–running Oscillator
R : 2.5kΩ
C : 3.3nF

Figure 27 : RC–Multivibrator Operation (at 307kHz clock frequency).



E88AN069–28

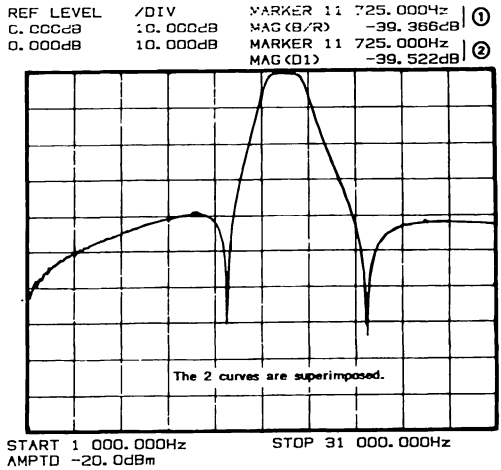
TSG8550

Power Supply : –5V, +5V

Clock Frequency : 307kHz

1– External Clock
2– Free–running Oscillator
R : 2.5kΩ
C : 1nF

Figure 28 : RC–Multivibrator Operation (at 847kHz clock frequency).



TSG8550

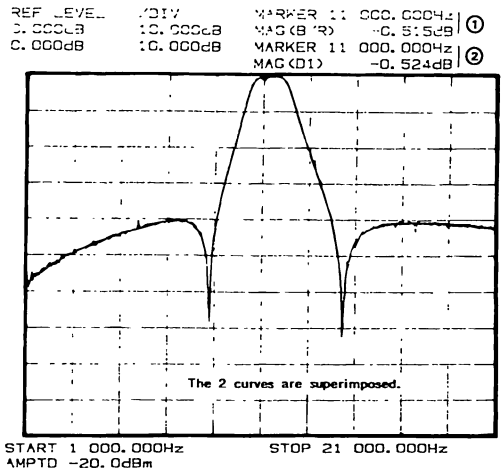
Power Supply : –5V, +5V

Clock Frequency : 847kHz

1– External Clock
2– Free–running Oscillator
R : 2.5kΩ
C : 220pF

E88AN069–29

Figure 29 : Using an External Transistor–based Oscillator (colpitts type).



TSG8550

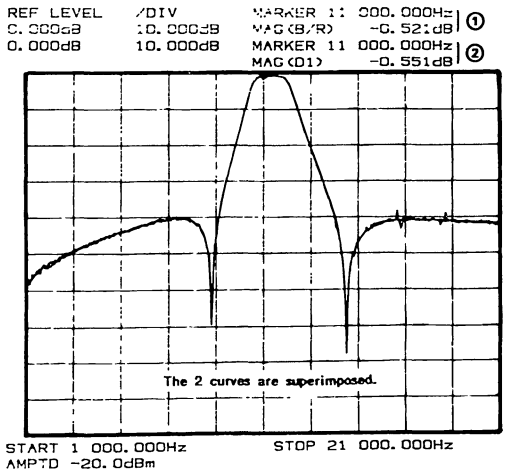
Power Supply : –5V, +5V

Clock Frequency : 540kHz

1– External Clock (TTL)
2– Colpitts Oscillator

E88AN069–30

Figure 30 : Using a Crystal–controlled Oscillator (implemented with an internal op–amp).



TSG8550

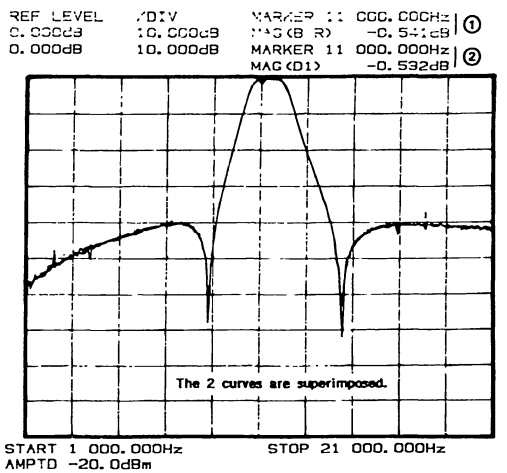
Power Supply : –5V, +5V

Clock Frequency : 540kHz

1– External Clock (TTL)
2– Operational Amplifier
+
Ceramic Resonator

E88AN069–31

Figure 31 : Operation with Crystal–controlled Oscillator (at 0V, +10V power supply).



TSG8550

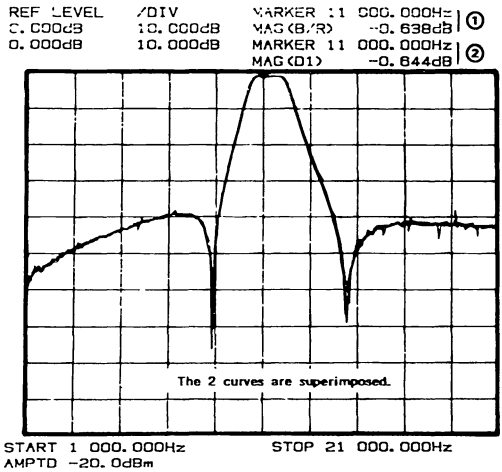
Power Supply : 0V, +10V

Clock Frequency : 540kHz

1– External Clock (TTL)
2– Operational Amplifier
+
Ceramic Resonator

E88AN069–32

Figure 32 : Operation with Crystal–controlled Oscillator (at 0V, +5V power supply).



E88AN069–33

TSG8550

Power Supply : 0V, +5V

Clock Frequency : 540kHz

1– External Clock (TTL)
2– Operational Amplifier
+
Ceramic Resonator

REGULATED POWER SUPPLIES

Some applications may require a high power supply rejection ratio. This can be achieved by regulating the filter power supply.

The objective of this section is to cover various regulation methods resorting to a minimum number of components.

The subjects discussed are the following :

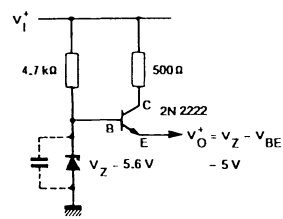
- **Zener Diode Regulation**
- **Regulation using one of the filter's operational amplifiers**

Also, the efficiency of each regulation and its influence on the power supply rejection ratio will be outlined.

ZENER DIODE REGULATION

This is the most straightforward method of voltage regulation. In general, since the current provided by the zener diode is not sufficient, it is consequently impractical to power the device directly by zener voltage. Figure 33a illustrates the solution to overcome this problem.

Figure 33a : Zener Regulation.



E88AN069–34

From the unregulated voltage V^+_I, a stable voltage independent from V^+_I variations is obtained across the zener diode. A voltage follower transistor delivers the current required by the device. The output voltage is : $V_Z - V_{BE}$ and therefore independent from V^+_I. V_{BE} varies as a function of I_E current flowing through the transistor. This variation is almost negligible due to the fact that :

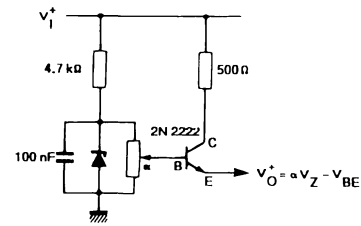
$$V_{BE} = \frac{KT}{q} \log \frac{I_E}{I\alpha}$$

(where $I\alpha$ is the base-emitter junction saturation current), that is, V_{BE} increases by **18mV** when the current doubles. The optional 500Ω resistor limits the current and protects the transistor against possible short-circuits.

A capacitor may be connected across the zener diode so as to filter the noise inherent to this type of diode.

If a variable power supply is required, a potentiometer may be connected across the zener diode as shown in figure 33b.

Figure 33b : Variable Zener Power Supply.



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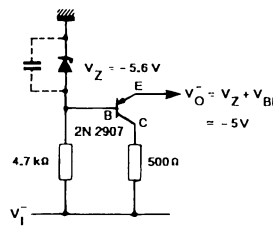
This arrangement is equally applicable to a negative power supply (V^-_I). In this case a PNP transistor is used as shown in figure 33c.

Figure 33c : Negative Zener Regulation.



E88AN069-36

A symmetrical power supply may thus be implemented using this method.

Note : This type of regulation is not temperature-compensated. One should expect an approximately + 3mV/C drift in output voltage value. Generally, this value is acceptable for the supply of integrated circuits such as SGS-THOMSON Filters.

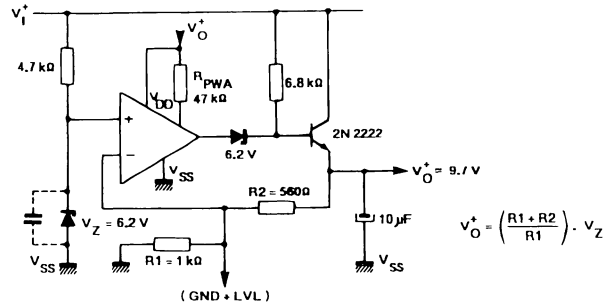
REGULATION USING AN OPERATIONAL AMPLIFIER

With the **M**ask **P**rogrammable **F**ilters (**MPF**), independent and uncommitted operational amplifiers are available to implement functions related to filtering.

One of this amplifiers can be used to achieve power supply regulation as illustrated in figure 34.

This configuration offers an excellent regulation thanks to the high open loop gain of the operational amplifier.

Figure 34 : Power Supply Regulation (using an internal op–amp).



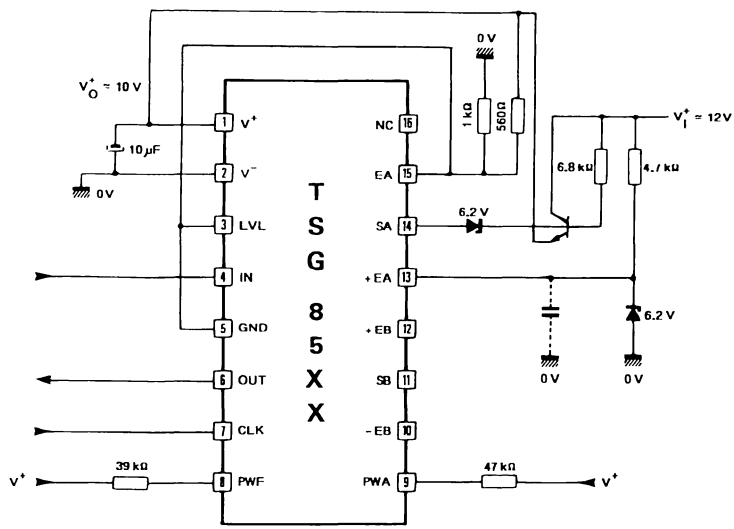
The reference voltage is generated by a zener diode. Since the amplifier is located within the filter package, it is also powered by the regulated output voltage V^+_O. The 6.8kΩ resistor connected between the collector and the base of the ballast transistor ensures start-up. This transistor does not need to be of power type as the output current value remains low. A zener diode connected in series with the amplifier output is necessary to provide for a sufficient voltage excursion to enable the regulation.

The output voltage can be accurately adjusted by setting the values of the bridge elements R1, R2 and using the relationship :

$$V^+_O = \left(\frac{R1 + R2}{R1} \right) - V_Z$$

The regulation performed following this procedure, takes into account both, the input voltage "V_I" and the "**load variations**". This power supply is therefore particularly suitable for complete applications built around SGS-THOMSON' MPFs.

Figure 35 : Filter with Single Power Supply Regulation.



A symmetrical regulated power supply can be implemented using the other operational amplifier of the filter circuit to perform negative supply regulation. One can obviously use the previous configuration and adapt the arrangement to negative voltage while also replacing the NPN ballast transistor by a PNP type.

Figure 36 illustrates the appropriate solution. The objective is to obtain two regulated V^+_O and V^-_O voltages with their absolute values as close to each other as possible. The positive regulated voltage V^+_O is obtained using the configuration described earlier. The negative voltage regulation resorts to an additional operational amplifier, operating in unity gain inverting configuration. Since the regulated V^-_O voltage follows accurately the variations of the V^+_O voltage, a unique reference voltage is sufficient.

Figure 36 : Symmetrical Regulated Power Supply.

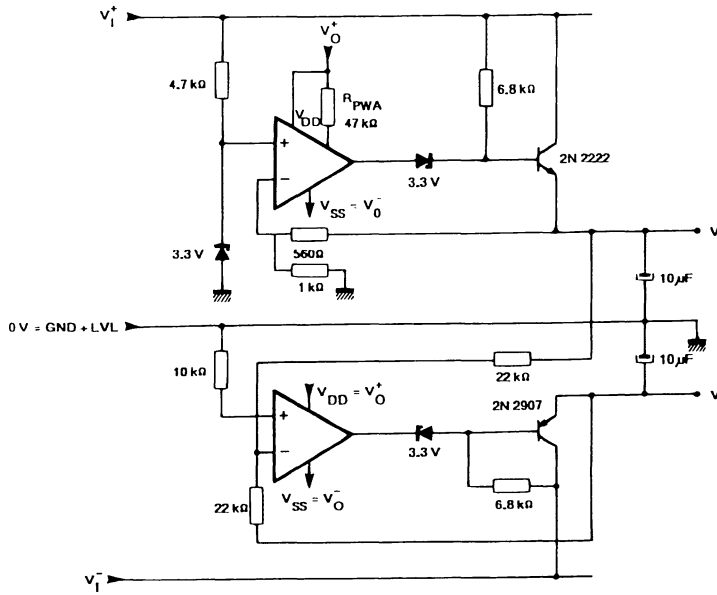
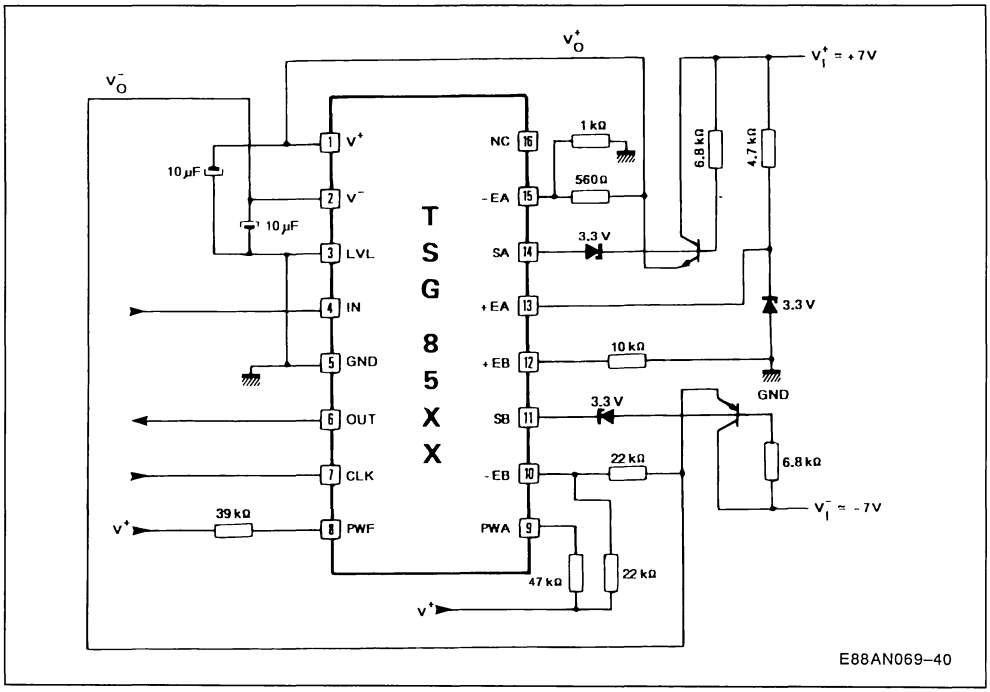
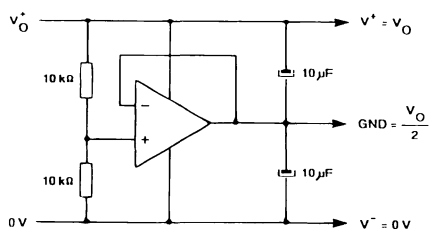


Figure 37 : Filter with Symmetrical Power Supply Regulation.



As shown in figure 38, a symmetrical power supply can be built using, a single regulated power supply, a resistor bridge and an operational amplifier configured as voltage follower. The symmetrical accuracy of this configuration is determined by the precision of the bridge.

Figure 38 : Split Power Supply.



Note : This configuration can be simplified by replacing the operational amplifier with a transistor operating as voltage follower. In this case, the resistor bridge must be readjusted taking into consideration the voltage shift due to the transistor base-emitter voltage drop.

POWER SUPPLY REJECTION RATIO

Figures 39 thru 44 given at the end of this section in paragraph 5.5 depict supply rejection characteristics of the **TSG8550** filter.

It is seen that in general V^- rejection ratios are approximately - 10dB less than those measured for V^+ supply.

A single power supply filtering capacitor (electrolytic) located close to the device will appreciably improve the rejection ratio (approximately – 15dB reduction).

A zener diode used for regulation will further improve the results and with the addition of filtering capacitor, one can obtain excellent results (up to – 60dB).

The method of using a voltage follower transistor following the zener diode results in an improved rejection ratio compared to the rejection ratio obtained with a zener diode without filtering. Note that the quality of the zener diode used has a significant influence on the results - e.g. the rejection ratios obtained using a 5.6V zener diode are much better than those obtained using a 4.7V zener diode. This is due to the fact that the 5.6V zener diodes exhibit a much steeper breakdown characteristics.

Finally, the symmetrical voltage regulator using operational amplifiers discussed earlier (figure 36) yields an excellent rejection ratio of less than - 60dB. It is a difficult task to further improve this ratio as at lower values, other sources of noise will be also measured.

CONCLUSION

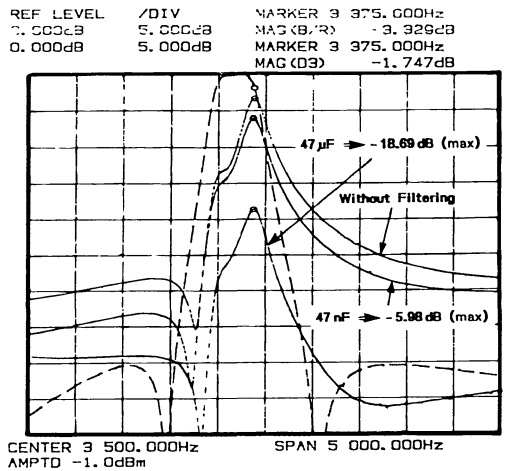
To improve power supply rejection ratio, supply voltage filtering by capacitor or using a zener diode are simple and efficient solutions.

In addition, if perfect power supply regulation for an application built around a SGS-THOMSON' MPF is also required, it would then be interesting to implement the regulator using the operational amplifiers available within the filter package.

SUPPLY REJECTION CHARACTERISTICS OF TSG8550 FILTER

The response curve of TSG8550 is drawn on each plot with a dotted line trace.

Figure 39 : V^+ Rejection Ratio (with a single filtering capacitor).



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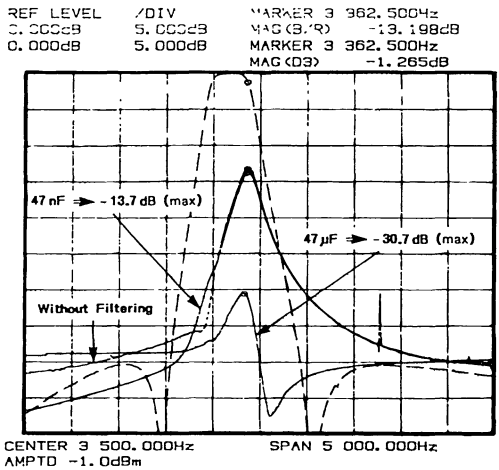
TSG8550

Symmetrical Power Supply : ± 5V

f_e : 150kHz

R_{PWF} : 39kΩ (grounded)

Figure 40 : V⁻ Rejection Ratio (with a single filtering capacitor).



TSG8550

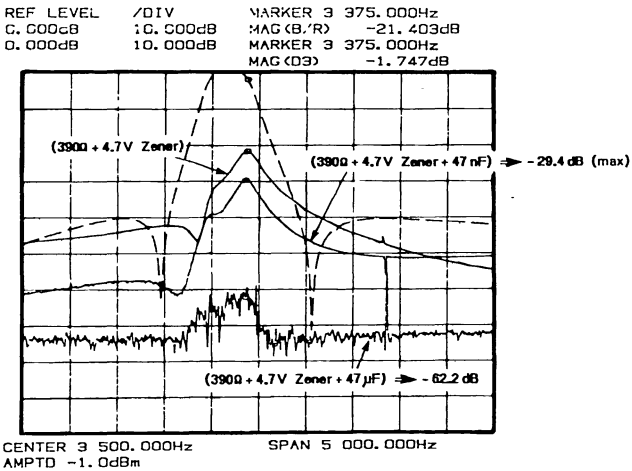
Symmetrical Power Supply : ± 5V

f_e : 150kHz

R_{PWF} : 39kΩ (grounded)

E88AN069-43

Figure 41 : V⁻ Rejection Ratio (with a zener diode and a filtering capacitor).



TSG8550

Symmetrical Power Supply : ± 5V

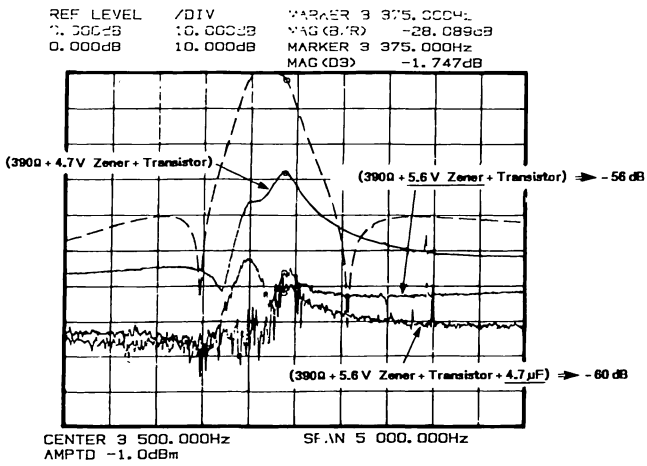
f_e : 150kHz

R_{PWF} : 39kΩ (grounded)

E88AN069-44

E88AN069-44

Figure 42 : V^+ Rejection Ratio (with a zener diode and a transistor).



TSG8550

Symmetrical Power Supply : ± 5V

f_e : 150kHz

R_{PWF} : 39kΩ (grounded)

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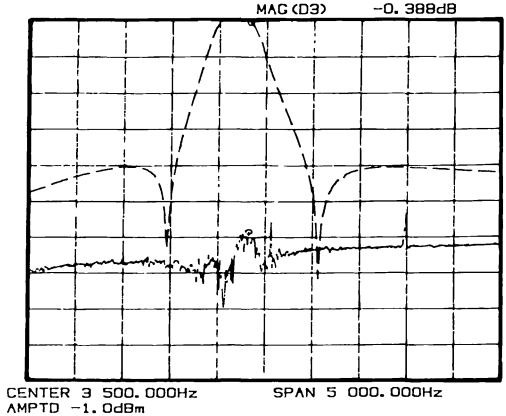
Figure 43 : V^+ Rejection Ratio (operational amplifier symmetrical regulator) [filtering capacitor : 33µF].



TSG8550

Symmetrical Power Supply : ± 5V

f_e : 150kHz

R_{PWF} : 39kΩ (grounded)

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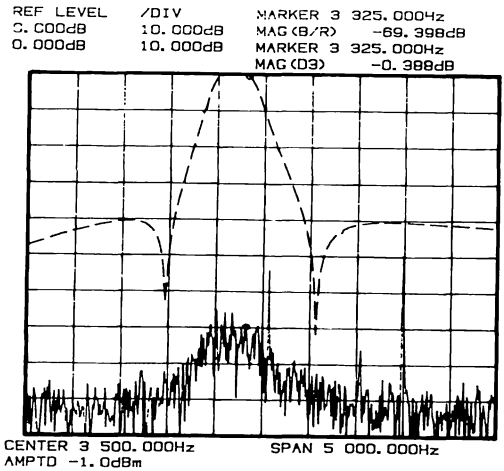
E88AN069–46

Figure 44 : V^- Rejection Ratio (operational amplifier symmetrical regulator).



E88AN069-47

TSG8550

Symmetrical Power Supply : ± 5V

f_e : 150kHz

R_{PWF} : 39kΩ (grounded)

WIRING RECOMMENDATIONS

This last section details the practical application considerations applicable to SGS-THOMSON range of **Switched Capacitor Filters**. The discussion will enable the designer to attain remarkable performances and to obtain in particular excellent signal-to-noise ratio.

Layout rules are sub-divided into 3 important sections :

- **Power supply decoupling**
- **Ground connections**
- **Operational amplifiers layout considerations**

POWER SUPPLY DECOUPLING

Power supply voltages "V^+" and "V^-" as well as "LVL" pin voltage (that in order to set the output dc level is generally amplified within the device) must be carefully decoupled.

Similarly, in the case of a single power supply operation, the dc voltage applied to "**Ground**" (GND) pin must be efficiently decoupled.

For decoupling purposes, one can use a high quality capacitor located very close to the filter package pin under consideration (V^+, V^-, LVL or GND). A capacitor of a few tens of nF will suffice.

Also, decoupling PWA and PWF pins will improve the signal-to-noise ratio. These pins determine the biasing current of, either operational amplifiers, or the filter and consequently have an influence on the overall device performance.

A capacitor of approximately **30pF** coupled to **PWF** pin and connected in parallel with the filter biasing resistor R_{PWF}', will in particular, prevent the occurrence of the so called "**clock feedthrough**" phenomenon. Clock feedthrough is defined as the "presence of the clock frequency harmonics at the filter output" and can give rise to disturbances within the stop band region.

GROUND CONNECTIONS

Conventional printed circuit board layout rules must be respected.

Ground connections must be wide enough to avoid occurrence of stray resistances that can cause ground pin (GND) voltage to fluctuate as a function of the current flowing through ground connections.

Star connection, starting from the GND pin and going to various application ground terminals, must be used as often as possible.

Particular attention must be paid to appropriate separation between the filter proper ground and the ground of complementary functions (clock, amplifier, comparator, ..) built using the on-chip operational amplifiers.

OPERATIONAL AMPLIFIERS LAYOUT CONSIDERATIONS

The two operational amplifiers available within the filter package are generally used for building anti-aliasing and smoothing filters connected to the switched capacitor filter input and output terminals.

Consequently, connections such as : common ground, too close p c board adjacent tracks, etc.. - susceptible to cause interaction between input and output signals, must be avoided.

Non-inverting terminals (+E) need special precaution. In fact, these inputs are of high impedance type and located next to each other in standard filter pinout configurations. In the case of standard Sallen-Key cells performing anti-aliasing and smoothing functions, since the filter input and output signals are routed via these two inputs, there will be risk of interaction between the signals. Therefore, tracks connecting to +E inputs must be separated by as much as possible and the capacitor values of the Sallen-Key Cell must be selected large enough so as to minimize the loading impedance on these pins. Low value resistors are used to achieve the latter requirement - R = 10k will in general enable the selection of suitable capacitor values.

CONCLUSION

Excellent application performances using SGS-THOMSON Microelectronics **Switched Capacitor Filters** will be obtained by observing the foregoing rules and recommendations.

Information contained in this application note is **applicable to any of the standard and semicustom filters** ; i.e. **the entire range of Mask Programmable Filters.**

SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE

BAND–PASS AND BAND–STOP FILTERS

INTRODUCTION

Standard switched capacitor filters currently marketed by SGS-THOMSON Microelectronics cover in particular a range of **Band-pass** and **Band-reject** filters - all of which have in general a high selectivity factor.

One may require to implement a band-pass or band-stop filter of lower Q figure.

The objective of this application note is just to demonstrate how such requirement is fulfilled by using **one low-pass** and **one high-pass standard filters.**

Throughout our discussion, we shall outline and illustrate, once again, the remarkable flexibility of use inherent to switched capacitor filters.

Subjects covered are :

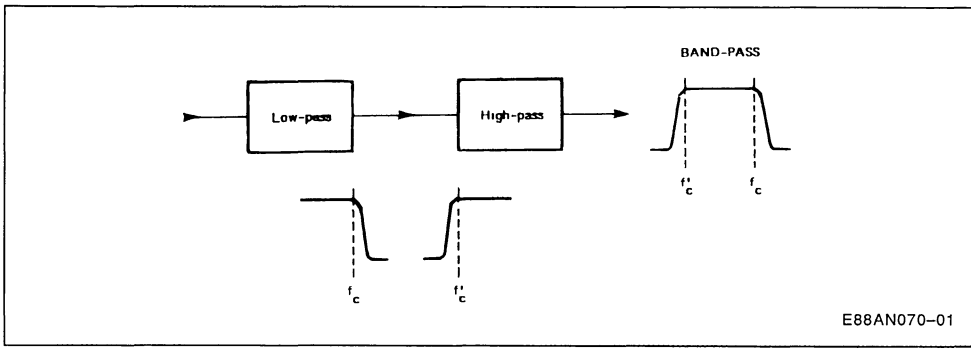
- 1 - **Band-pass Filters**
- 2 - **Band-stop or Band-reject Filters**

BAND-PASS FILTERS

FILTER SYNTHESIS FUNDAMENTALS

Cascaded combination of **one low-pass** and **one high-pass** filters yields a **band-pass** filter.

Figure 1 : Band–Pass Filter Fundamentals.



Note however that in this arrangement the low-pass filter precedes the high-pass filter so as to limit the signal frequency band as it enters the first stage, thus improving the signal-to-noise ratio.

Switched capacitor filters manufactured by SGS-THOMSON are active filters having a **high input** and a **low output impedances** of typically **"3MΩ"** and **"10Ω"** respectively, thus making them particularly suitable for cascaded combination - by coupling the output of one to the input of the other.

The following standard filters are employed throughout the present section :

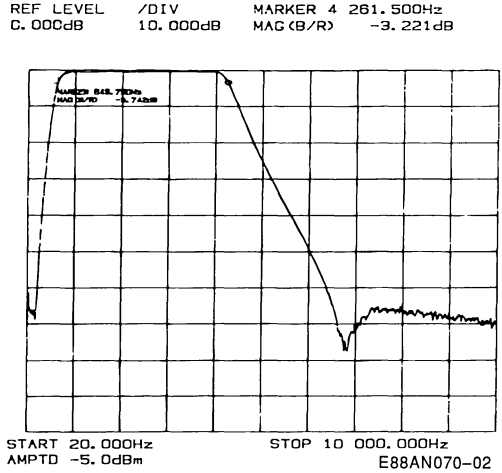
- **TSG8512** : 7th order Cauer-type low-pass filter
- **TSG8532** : 6th order Chebychev-type high-pass filter

Obviously, other standard filters may be cascaded according to requirements.

USING A COMMON CLOCK

Figure 2 depicts the frequency response of the two filters put in cascade and operating at an identical clock frequency of 400kHz.

Figure 2 : Band–Pass Filter Frequency Response.



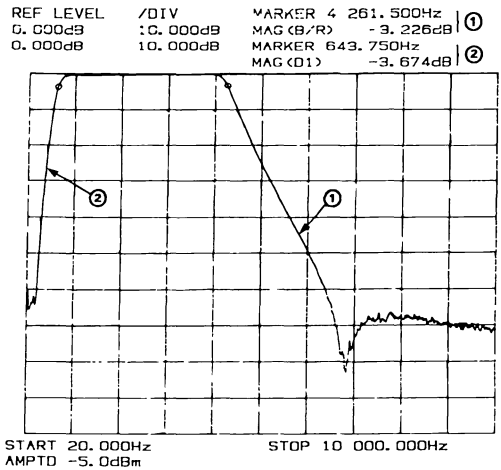
BAND–PASS FILTER

TSG8512
+
TSG8532

"Identical Clock Frequency : 400kHz"
(without anti–aliasing & smoothing filters)

It is clearly seen that there is no significant difference between this curve and the curves of figure 3 illustrating the frequency response of the filters operating separately but at the same 400kHz clock frequency.
It is thus obvious that direct cascading of the filters does not affect the operating characteristics of the either filter.

Figure 3 : Frequency Response of Low–Pass (TSG8512)& High–Pass (TSG8532) Filters [common clock frequency : 400kHz].

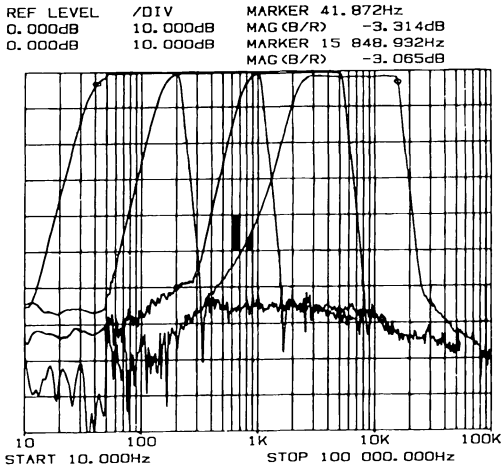


①
TSG8512 (low–pass filter)
"Clock Frequency : 400kHz"

②
TSG8532 (high–pass filter)
"Identical Clock Frequency : 400kHz"

Figure 4 outlines the interesting characteristics of a band–pass filter implemented as discussed above.

Figure 4 : Frequency Range Shifting of Band–Pass Filter.



E88AN070–04

BAND–PASS FILTER

TSG8512 (low–pass)

+

TSG8532 (high–pass)

Identical Clock Frequency :

→ **20kHz**

→ **100kHz**

→ **500kHz**

→ **1.5MHz**

Figure 4 illustrates how by simple modification of the common clock frequency, the frequency range of the band-pass filter is shifted without causing any modification to its frequency response curve.

Due to inherent characteristics of the switched capacitor filters, the clock to cut-off frequency ratio is always known. It is thus a simple matter to calculate the clock frequency as a function of the signal frequency one wishes to use.

For example, in the case of **TSG8512** filter, this ratio is :

$$\frac{fe}{fc} = 100 \pm 1\%$$

Where f_e is the **external clock frequency**.

If f_c is to be the **upper cut-off frequency** equal to **5kHz**, we shall therefore select f_e **= 500kHz.**

Also, since $\frac{f_e}{f'c}$ **= 500** ±1% for **TSG8532**, the **lower cut-off frequency f'c** will be **1kHz**.

This curve is given in figure 4.

Note that in all cases, the passband width remains constant at **4 x f'c.**

Different bandwidths are obtained by cascading other standard filter types.

Corresponding calculations are similar to those outlined above.

TWO DIFFERENT CLOCK FREQUENCIES (figure 5)

Figure 6 depicts the frequency response of a band-pass filter implemented by cascading TSG8512 and TSG8532 filters but each operating at a different frequency.

Similar to the former case, it is obvious that the frequency response characteristics of the individual filters are not modified by this configuration and remain unchanged after cascading.

Note however that in this case, the signal delivered at the output of the first filter (TSG8512) goes through a smoothing filter before entering the second filter (TSG8532).

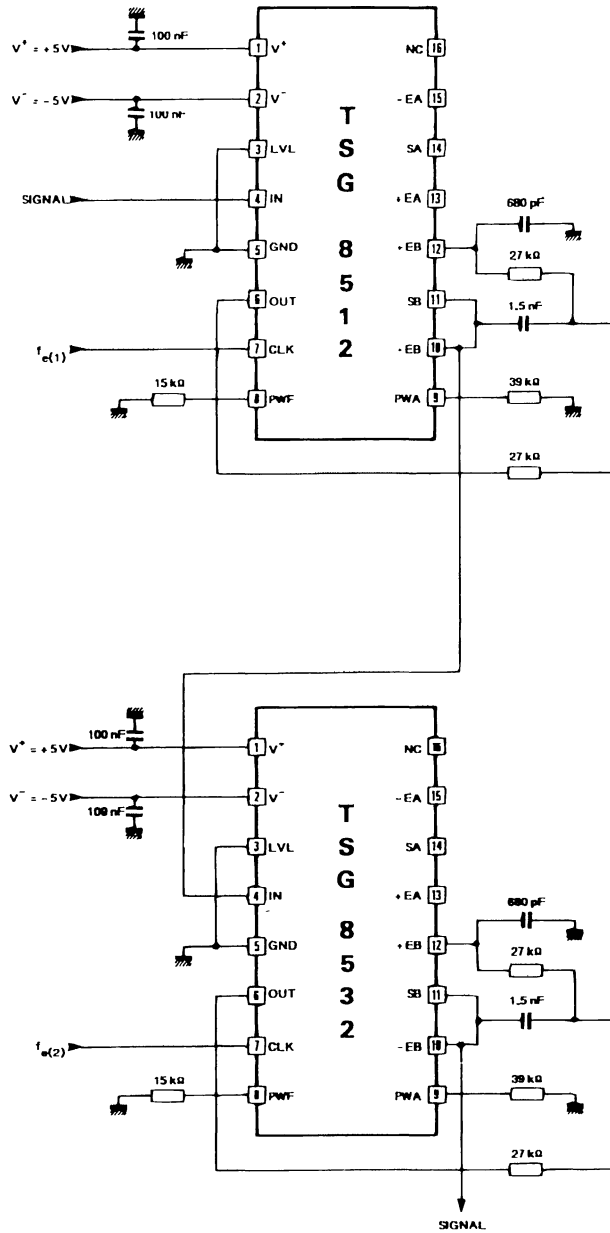
This process is necessary as the operating frequencies of the filters are different and consequently there will be lack of synchronization between the sampling performed by each individual filter.

In the absence of the signal smoothing process, this fact will give rise to disturbances within the cut-off frequency band.

Similarly, the signal delivered by the second filter goes through a smoothing filter.

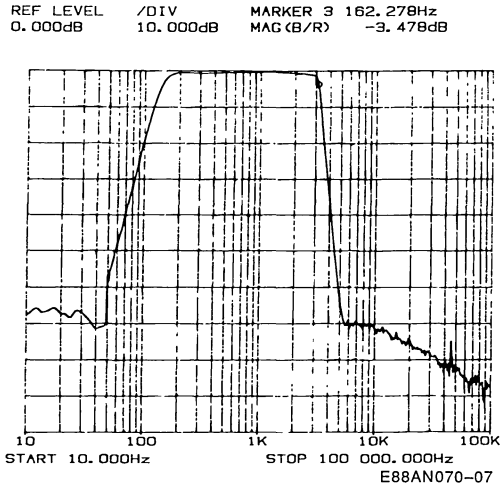
These smoothing filters are implemented by **2nd order Sallen-Key** Cells each using one of the on-chip operational amplifiers of the switched capacitor filter (figure 5).

Figure 5 : Band–Pass Filter (two separate clocks).



The cut-off frequency of these Sallen-Key Cells is chosen to be twice the upper cut-off frequency of the band-pass filter so as to eliminate any signal disturbance within the pass band region.

Figure 6 : Low Q Band–pass Frequency Response Characteristics.



E88AN070–07

BAND–PASS FILTER

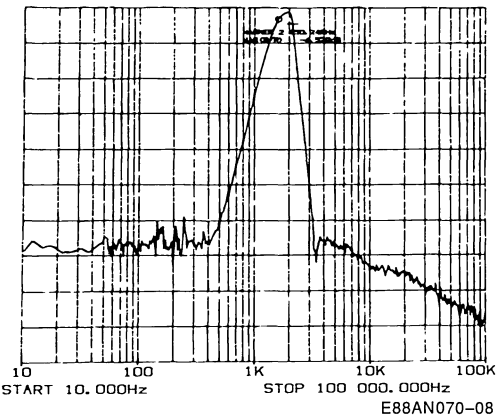
"Two different clock frequencies"

TSG8512 "Clock : 300kHz"
+
TSG8532 "Clock : 90kHz"
+
Anti–aliasing & Smoothing Filters

(f_c = 6kHz)

Figure 7 illustrates how the cascading of two filters yields an extremely steep band-pass characteristics.

Figure 7 : Steep Band–pass Frequency Response Characteristics.



E88AN070–08

STEEP BAND–PASS

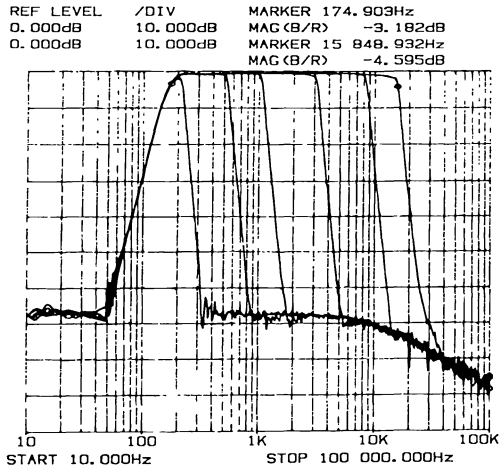
TSG8512 "Clock : 200kHz"
+
TSG8532 "Clock : 800kHz"

The band-pass obtained in this case has a selectivity factor of about 4.

Note that the clock frequencies employed (200kHz and 800kHz) allow the use of a single external oscillator running at 800kHz (or its multiple frequencies). The second clock frequency is then derived from this master clock using a counter.

In figures 8 and 9, one of the clock frequencies is maintained constant while the other is varied. This arrangement results in an adjustable band-pass filter.

Figure 8 : Shifting the Upper Cut–off Frequency.



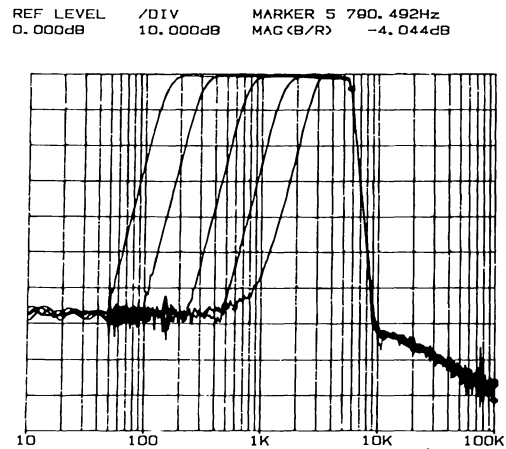
E88AN070–09

BAND–PASS FILTER

TSG8512
+
TSG8532

With Anti–aliasing & Smoothing Filters
TSG8532 "Fixed clock : 100kHz"
TSG8512 "Variable clock :"
→ 20kHz
→ 50kHz
→ 100kHz
→ 300kHz
→ 800kHz
→ 1.5MHz

Figure 9 : Shifting The Lower Cut–off Frequency.



E88AN070–10

BAND–PASS FILTER

TSG8512 "Fixed clock : 540kHz"

TSG8532 "Variable clock :"
→ 100kHz
→ 200kHz
→ 500kHz
→ 1MHz
→ 2MHz

Each cut-off frequency is adjusted with precision and if separate clocks are used, adjustments will be entirely independent.

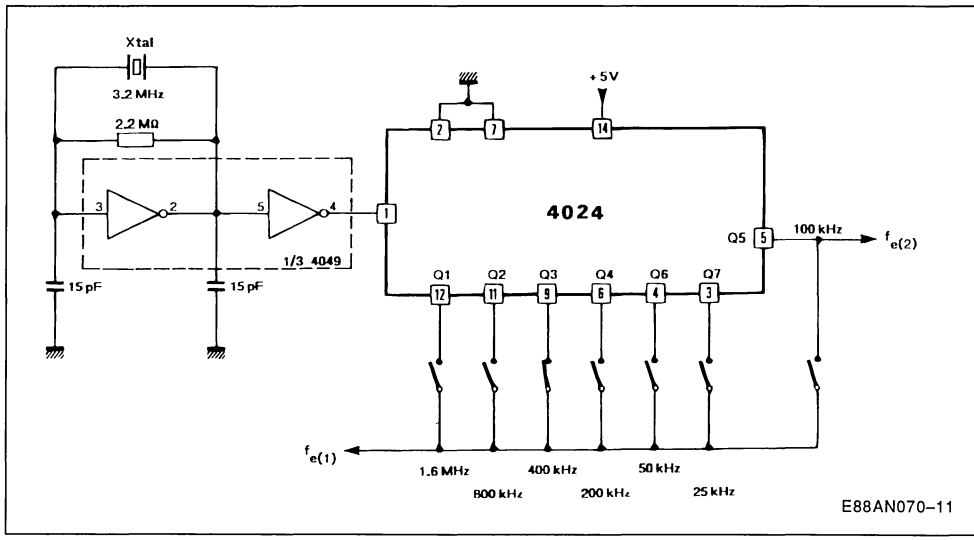
If separate clocks are not available, one may use a single master oscillator and then derive the required frequencies using a frequency divider circuit.

In this case, the frequencies would be the multiples of one another.

By appropriate selection of the division factor, the frequency bandwidth is changed.

The filter frequency response curve is readily shifted along the frequency axis by simple modification of the master oscillator frequency (figure 10).

Figure 10 : Clock Generation for Adjustable Band–pass (deriving two different clock frequencies from a master oscillator).



Illustrated example gives identical results to those depicted in figure 8.

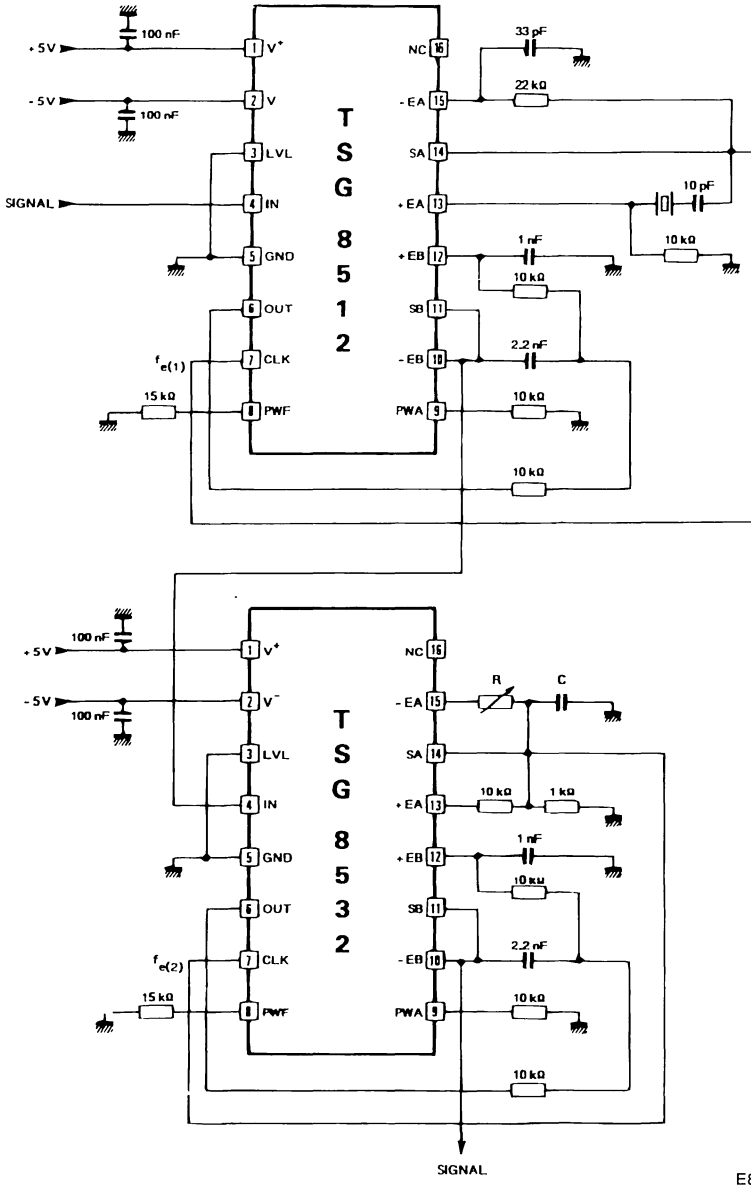
According to requirements, a single 4-bit 74163 TTL-type counter may be used as frequency divider.

For adjustable band-stop filter, either a 4020-type 14-stage counter or a 4060-type counter that also includes an on-chip crystal oscillator would be suitable alternatives.

To implement an appropriate oscillator, refer to the **"Application Note : AN-069" [A Supplement to the Utilization of Switched Capacitor Filters]** that discusses in detail how to build crystal-controlled and free-running oscillators using the on-chip operational amplifiers of the filter circuits.

For example, curves depicted in figure 9 may be obtained, in the case of TSG8512, using the ceramic resonator discussed in the application note mentioned above - and in the case of TSG8532, by adjusting the frequency of a free-running oscillator whose frequency is varied by a potentiometer as illustrated in figure 11.

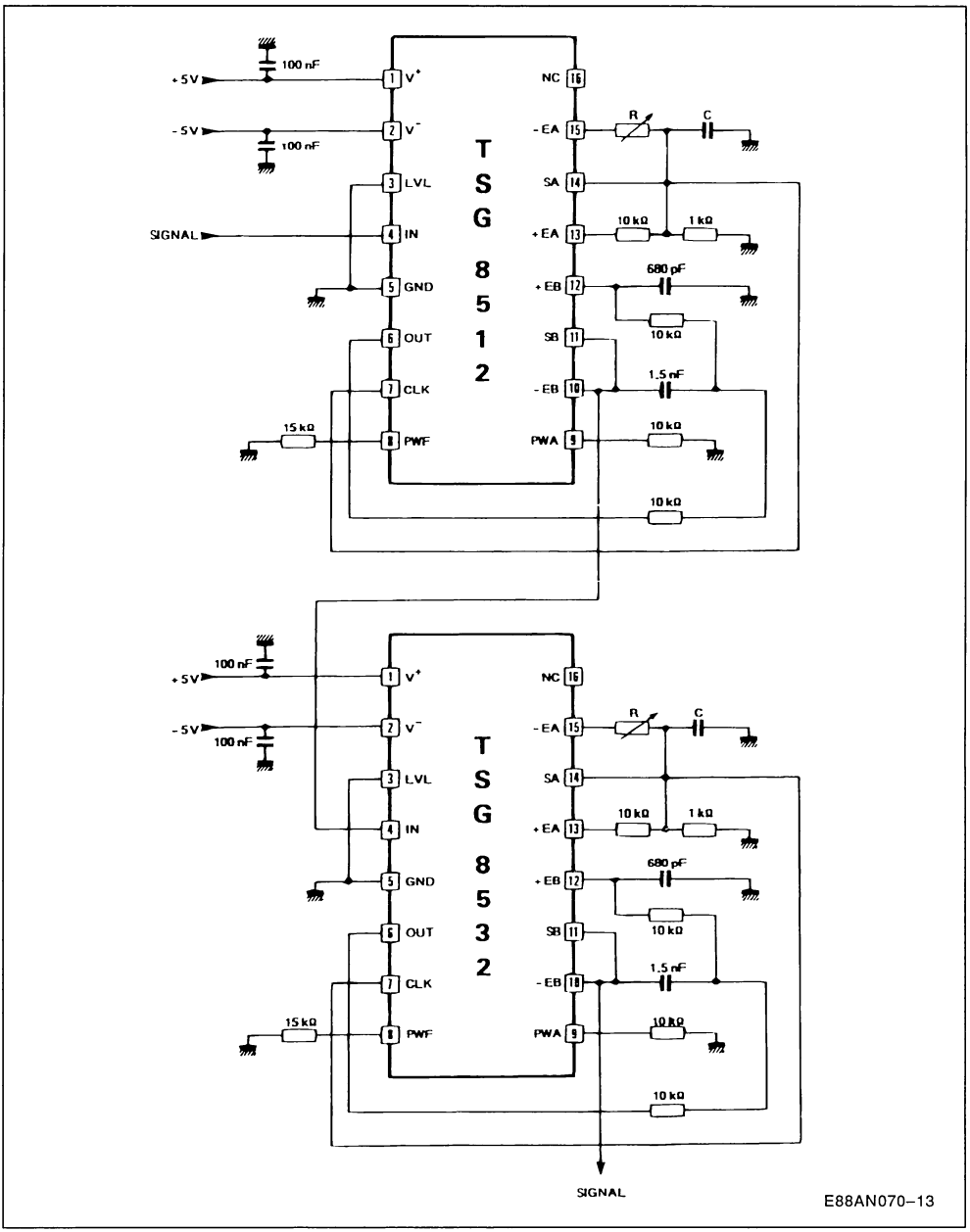
Figure 11 : Adjustable Band–pass Filter (upper cut–off frequency set by crystal–controlled oscillator).



A band-pass filter is thus implemented using only 2 switched capacitor filters of SGS-THOMSON configured as active elements.

A wide frequency adjustment range is available using RC-type free-running relaxation oscillators (figure 12).

Figure 12 : Adjustable Band–pass Filter (upper and lower cut–off frequencies are both adjustable).

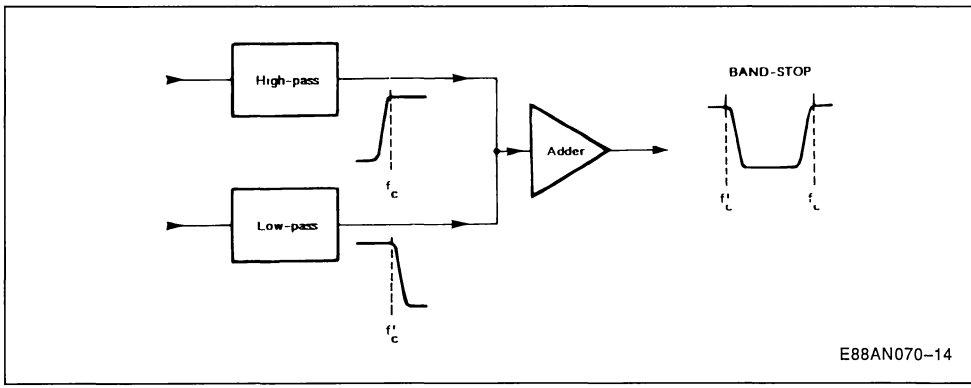


In order to obtain excellent performances and specially to improve the signal-to-noise ratio, addition of anti-aliasing and smoothing filters suited with the upper cut-off frequency of the band-pass is also necessary.

BAND–STOP FILTERS

FILTER SYNTHESIS FUNDAMENTALS (figure 16)

Figure 13 : Band–stop Filter Fundamentals.



A band-stop filter is obtained by adding the output signals of a high-pass and a low-pass filter.

The adder circuit is configured using an operational amplifier.

In the case of SGS-THOMSON switched capacitor filters, the adder circuit is readily implemented using one of the operational amplifiers contained in the same package as the filter circuitry. It is thus clear that only two packages, one low-pass and the other high-pass, are required to implement a band-stop filter.

An adder is built using either of the configurations given below :

Figure 14 : Inverting Adder.

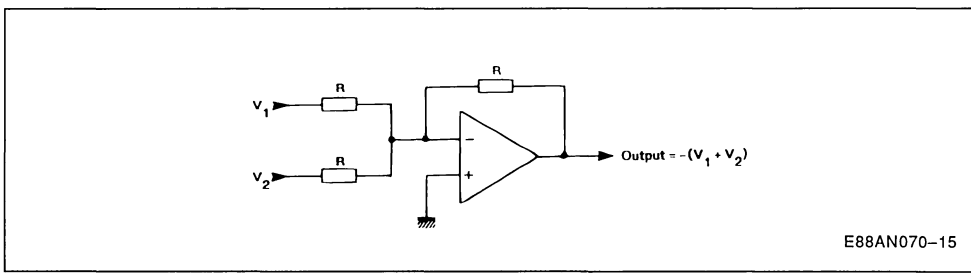


Figure 15 : Non Inverting Adder.

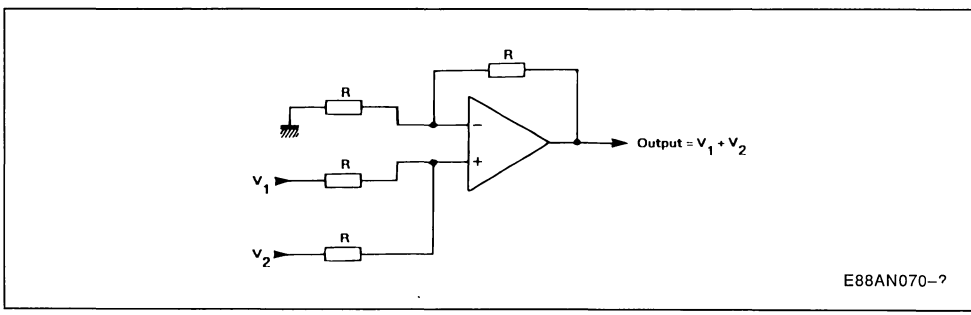
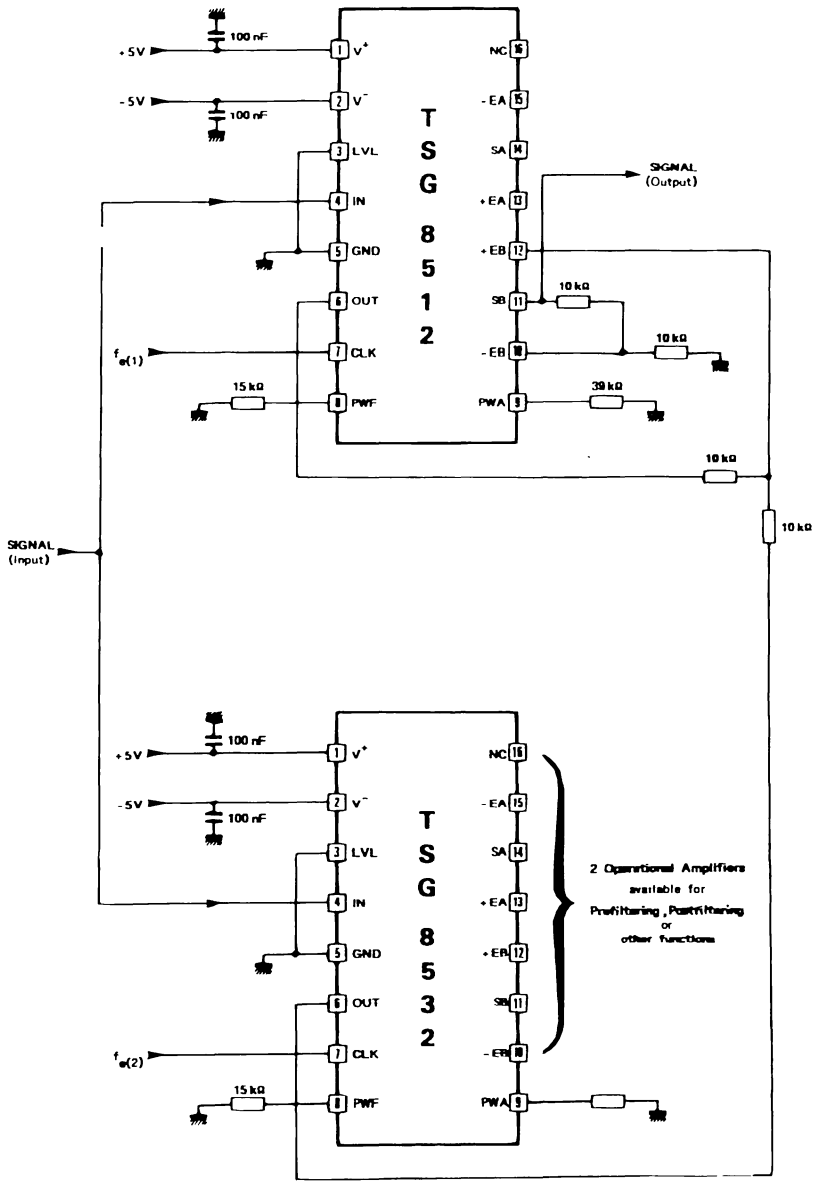


Figure 16 : Band–Stop Filter (two separate clocks).



E88AN070–16

RESULTS

Similar to band-pass discussion, the standard devices employed here are :

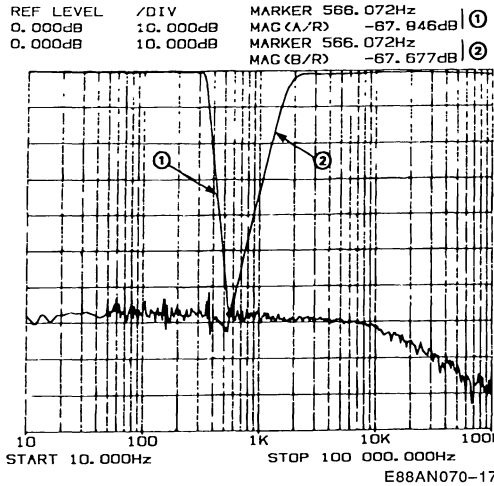
TSG8512 : Low-pass

TSG8532 : High-pass

Other standard circuits can be used according to the desired cut-off frequency slope and attenuation.

Figure 17 depicts the response curves of the individual filters.

Figure 17 : Frequency Response of Low–pass & High–pass Filters.



E88AN070–17

① *** LOW–PASS FILTER**

TSG8512 "Clock : 32kHz"

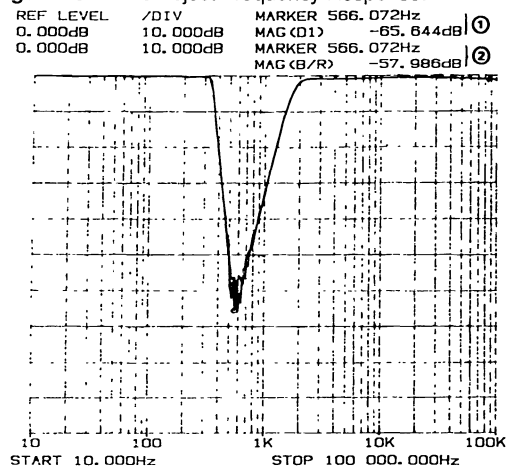
② **HIGH–PASS FILTER**

TSG8532 "Clock : 1.170MHz"

Figure 18 illustrates the frequency response curve of the band-stop filter built using these two filters operating at the same frequency as previously.

Once again, it is obvious that the operating characteristics of each filter remain unaffected by this arrangement. The response curve is obtained directly from figure 17.

Figure 18 : Band–reject Frequency Response.



E88AN070–18

BAND–REJECT FILTER

TSG8512 "Clock : 32kHz"

+

TSG8532 "Clock : 1.170MHz"

① **With non–inverting Adder**
(filter op–amp R_{PWA} = 39kΩ)

② **With inverting Adder**
(filter op–amp)

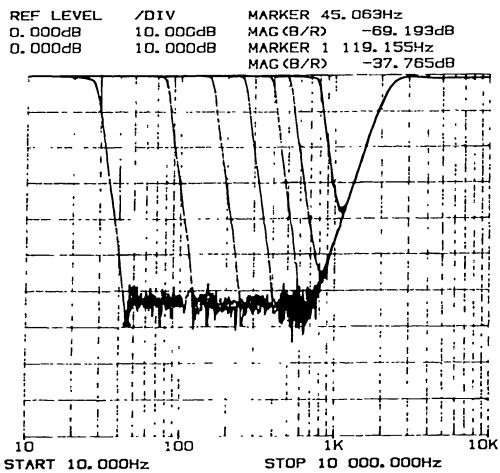
Also, there is no significant difference between an inverting and a non-inverting adder (except for output signal phase inversion).

For our present discussion, from now on, we shall use non-inverting adder arrangement. The configuration will therefore be identical to that given in figure 16 ; that illustrates how a band-stop filter is readily built using two switched capacitor filters.

In figures 19 and 20, the clock frequency of one filter is constant while the other is adjustable.

The outstanding flexibility of such band-stop filter is clearly demonstrated by observing the fact that the adjustment of one filter has no influence whatsoever on the other.

Figure 19 : Shifting the Lower Cut–off Frequency.



E88AN070–19

As discussed earlier, refer to section concerning **Oscillators** (Application Note : **AN-069**) for details on how to implement the appropriate clock circuits.

One of the operational amplifiers available may be used to build crystal-controlled or RC-type variable oscillators.

Electrical diagrams of these oscillators are identical to those given in figures 11 and 12.

Similarly, if clock frequencies are multiples of each other, a single master oscillator and frequency divider combination may be used.

Any modification of the master frequency will shift the filter response curve along the frequency axis (see figure 10).

BAND–STOP FILTER

TSG8532 "Fixed Clock : 1.5MHz"

+

TSG8512 "Variable Clock :"

→ 2.5kHz

→ 7.5kHz

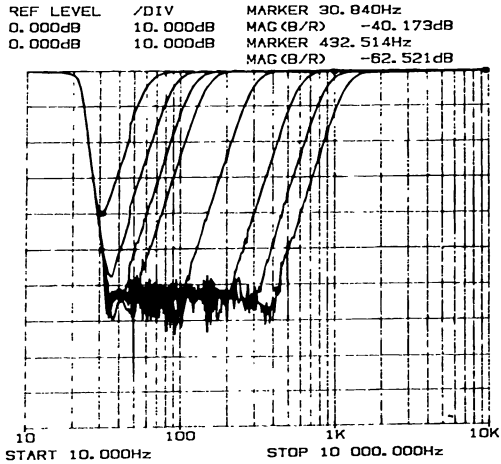
→ 15kHz

→ 25kHz

→ 50kHz

→ 70kHz

Figure 20 : Shifting the Upper Cut–off Frequency.



E88AN070–20

BAND–STOP FILTER

TSG8512 "Fixed Clock : 2kHz"
+
TSG8532 "Variable Clock :"
→ **40kHz**
→ **60kHz**
→ **80kHz**
→ **100kHz**
→ **200kHz**
→ **400kHz**
→ **600kHz**
→ **800kHz**

BAND-REJECT FILTERS (figure 21)

An interesting application of band-stop filters is implementation of frequency-reject filters, i.e. steep band-stop filters.

For this application, a low-pass TSG8512 and a high-pass TSG8531 filters are used. The **TSG8531** is a standard **6th order Cauer-type high-pass** filter and was chosen for this application due to its sharp cut-off characteristics.

Figure 21 : Band–reject Filter (adjustable center frequency).

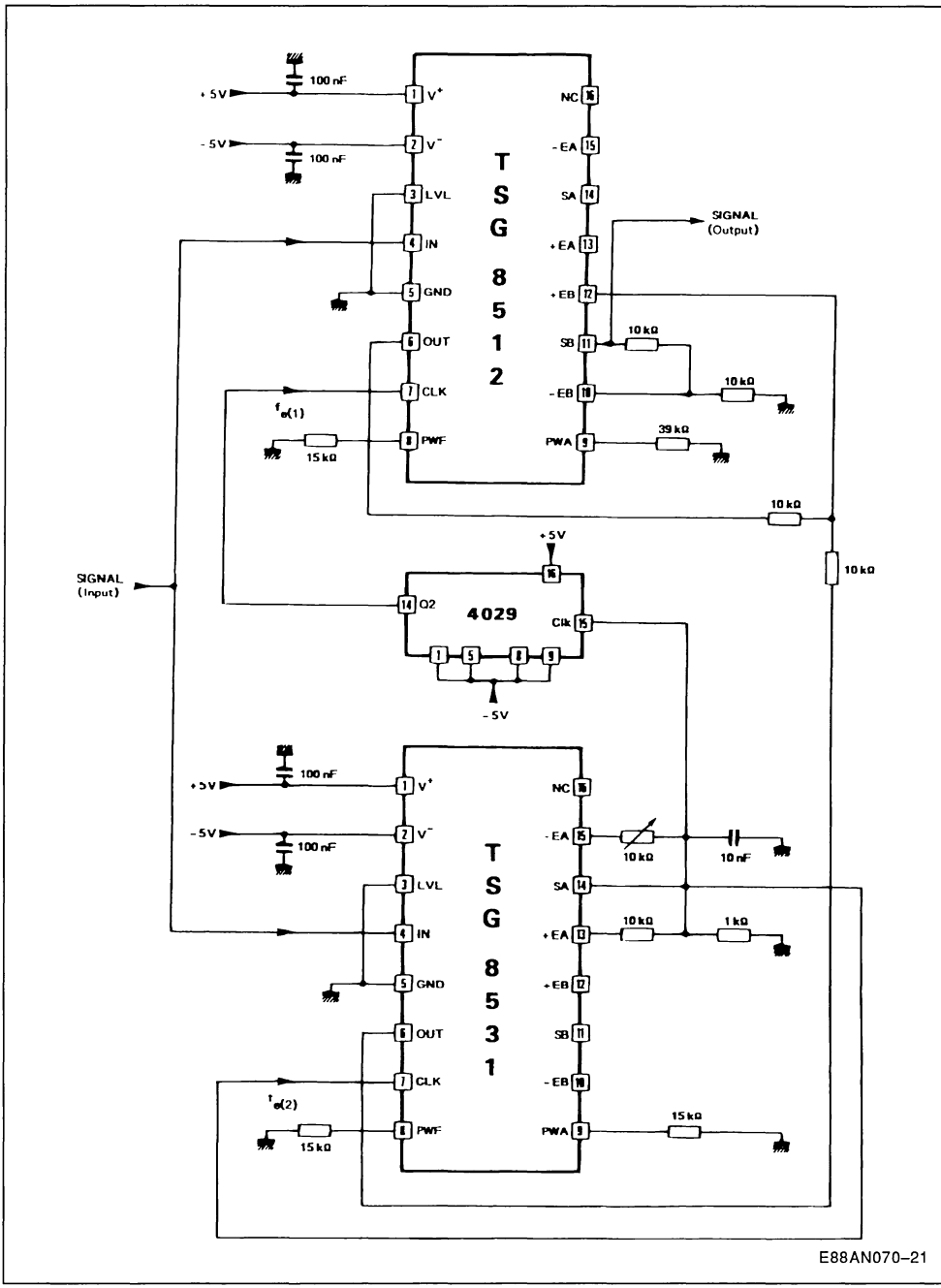
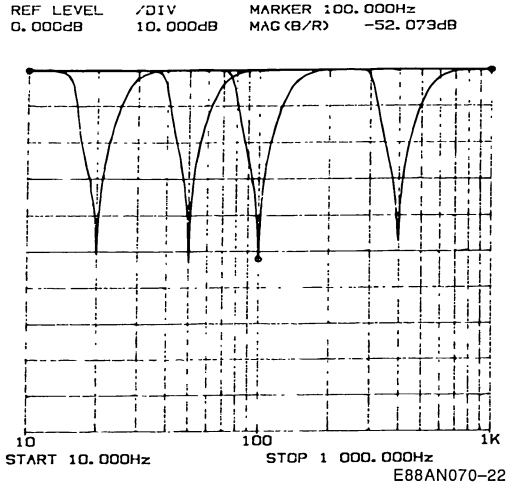


Figure 22 shows response curves obtained at different center frequencies.

Figure 22 : Shifting the Frequency Response of Band-reject Filter.



BAND-REJECT
TGS 8512 + TSG 8531
For different **center frequencies :**
20Hz, 50Hz, 100Hz, 400Hz
The two clock frequencies have a
Constant ratio of 10

The frequency ratio of the clocks was selected to be constant and equal to 10.

This allows use of a single oscillator followed by a frequency divider.

Figure 21 illustrates the electrical diagram of this band-reject filter.

This type of band-reject filter is generally employed for the suppression of mains frequency transients, i.e. 50Hz or 60Hz.

In this case, the application characteristics are as follows :

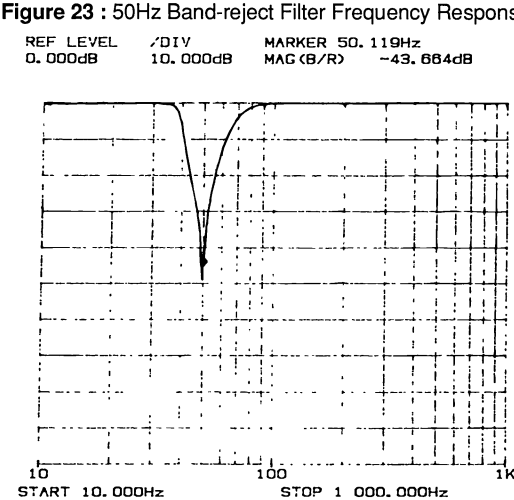
50Hz center frequency :

TSG8531 filter clock frequency : 36kHz
TSG8512 filter clock frequency : 3.6kHz
Selectivity Factor : Q 1.6
Attenuation at 50Hz : 45dB

60Hz center frequency :

TSG8531 filter clock frequency : 43kHz
TSG8512 filter clock frequency : 4.3kHz
Selectivity Factor : Q 1.6
Attenuation at 60Hz : 48dB

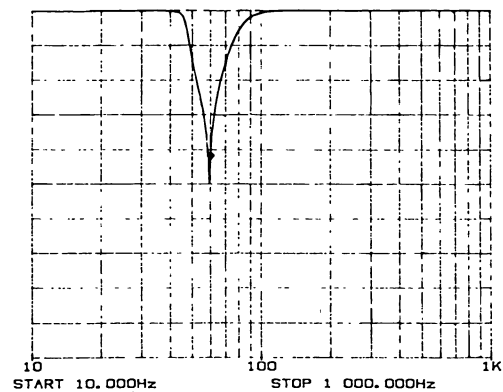
Figure 23 : 50Hz Band-reject Filter Frequency Response.



E88AN070–23

50Hz REJECT
TGS 8512 "Clock : 3.6kHz"
+
TSG 8531 "Clock : 36kHz"

Figure 24 : 60Hz Band-reject Filter Frequency Response.



E88AN070–24

60Hz REJECT
TGS 8512 "Clock : 4.3kHz"
+
TSG 8531 "Clock : 43kHz"

SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE

SWITCHED CAPACITOR FILTERS SIGNAL DETECTION & SINEWAVE GENERATION

By Jacques REBERGA

INTRODUCTION

The present note outlines the specifications of high selectivity factor (Q > 1) band-pass filters such as standard **TSG8551** and **TSG8550** devices.

Subjects covered are :

- **Signal Detection**
- **Implementation of a very low distortion sine-wave oscillator.**

These application fields cover a wide range of practical configurations built around the switched capacitor filters - few examples of which will be described in detail.

SIGNAL DETECTION

This section discusses various types of the signal detection techniques and gives an application example of each.

The following topics will be covered successively :

- **Amplitude detection**
- **Frequency detection**
- **Burst duration detection**

The **TSG8551** standard filter is best suited to this type of application. This is a selective band-pass 8th order switched capacitor filter with selectivity factor **Q** equal to **35**. In addition, it has a relatively high gain (30dB typ.) at center frequency. The attenuation within the stop band region is typically 70dB.

Consequent to the foregoing, it is obvious that the **TSG8551** is perfectly suitable for signal detection applications. Since the clock frequency to filter center frequency ratio is constant, the TSG8551 can be accurately locked onto the signal to be detected, by adjusting the external clock frequency.

AMPLITUDE DETECTION

The objective is to measure the amplitude of a given signal selected by the TSG8551 filter.

Irrespective of the signal shape, the filter delivers a sinewave frequency of which corresponds to the filter center frequency. This is particularly useful when measuring a signal super imposed on a carrier or lost within interference signals.

The detected amplitude level depends on the filter gain at center frequency. As specified in technical data sheet, the TSG8551 filter has a fixed gain - guaranteed gain value of **28** to **32dB** at **400kHz clock frequency**.

This application requires an extremely stable "**Quartz** or **Ceramic Resonator**" - controlled clock generator.

In fact, any clock frequency drift will cause center frequency displacement and thus detected signal amplitude variation.

We shall demonstrate in the present application note, how it is possible to lock the clock frequency onto the frequency of the signal to be detected (section 2.1.3).

Filter offset compensation is necessary in order to obtain an error-free measurement of the signal amplitude.

This function is easily implemented using "**LEVEL**" pin of the TSG8551 which controls the output dc level and can therefore be used to bring this level down to zero. Same as for all other SGS-THOMSON Microelectronics switched capacitor filters, an automatic offset compensation feature can be also implemented (refer to application note "AN-069" for detailed discussion of this topic).

SENSITIVITY OF SWITCHED CAPACITOR FILTERS

Minimum signal amplitude detectable by TSG8551 is around 1mV peak-to-peak. Signals of lower amplitude can be processed provided that they go through a pre-amplifier before entering the filter input. The pre-amplifier can be implemented using one of the on-chip operational amplifiers. In this case, the signal level at amplifier input must be at least 100µV peak-to-peak.

RECTIFICATION

In order to measure the amplitude, the signal is generally first rectified (half- or full-wave rectification).

Once again, the on-chip operational amplifiers can be used to perform this task.

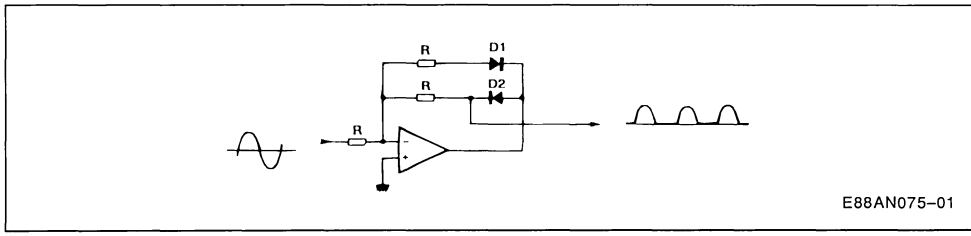
HALF-WAVE RECTIFICATION

Figure 1 illustrates the operating principles of this rectifier.

Figure 1 : Half–Wave Rectification Principles.

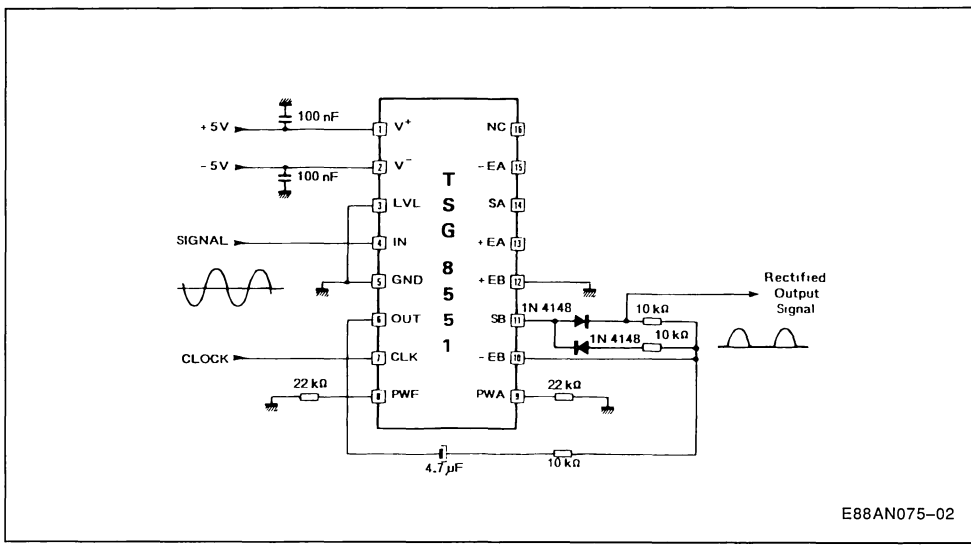
Diode D1 conducts during the input signal positive half cycle while diode D2 is reverse biased and there is therefore no signal at the output.

During the negative half cycle, diode D1 is reverse biased and diode D2 conducts - the amplifier operates in unity gain inverting configuration and consequently inverts the negative going input signal and delivers a positive output signal.



The gain of this configuration can be set by adjusting the value of the feed-back resistor - thereby allowing signal amplification if necessary.
As depicted in figure 2, practical configuration using one of the on-chip operational amplifiers is readily implemented. The output signal offset can be suppressed by routing the signal through a capacitor before its application to the rectifier.

Figure 2 : Application Configuration of the Half–wave Rectifier.

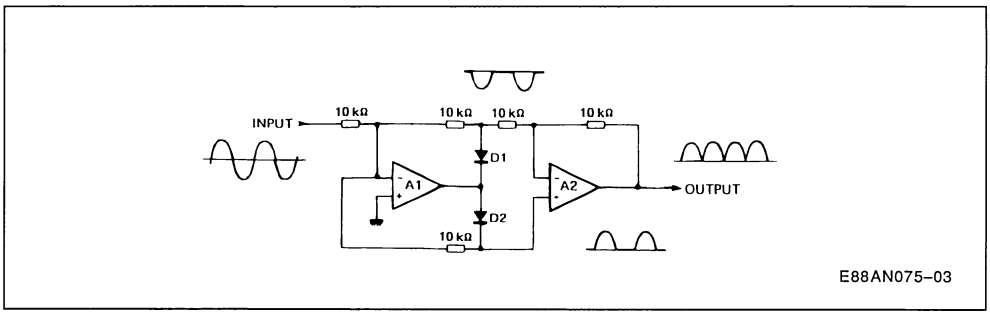


FULL-WAVE RECTIFICATION

Figure 3 depicts the operating principles of this rectifier.

Figure 3 : Full–wave Rectification Principles.

The first amplifier (A1) operates as half-wave rectifier - the two rectified half-cycles are forwarded to the second amplifier (A2) that inverts once again the positive half-cycles and transmits directly the negative half-cycles of the input signal.



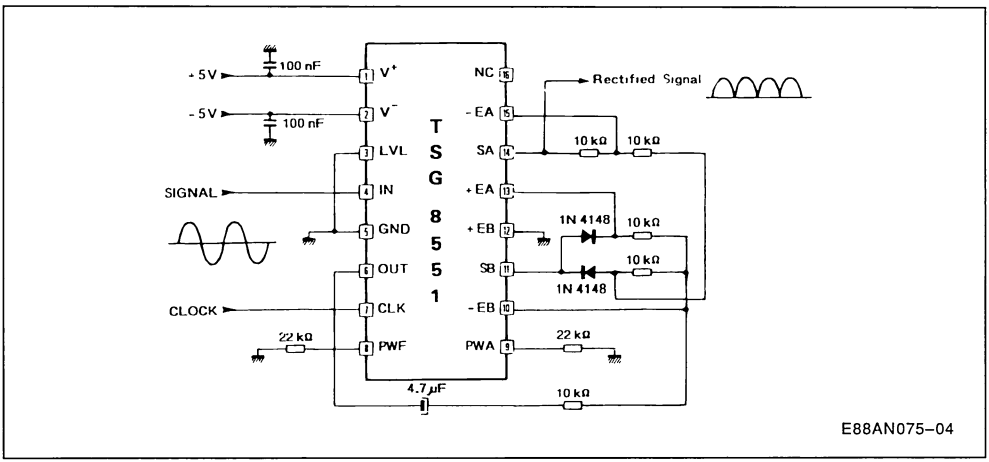
This configuration uses two operational amplifiers. The arrangement is straightforward, while resistors are of identical value and therefore easily matched - yielding accurate rectification.

Figure 4 illustrates the practical configuration using the on-chip operational amplifiers of the switched capacitor filter.

Since rectifier configurations are sensitive to input signal offset, a 4.7µF capacitor is inserted between the filter output and the rectifier.

A simple R-C network arrangement at filter output allows dc level extraction from the rectified signal.

Figure 4 : Application Configuration of the Full–Wave Rectifier.



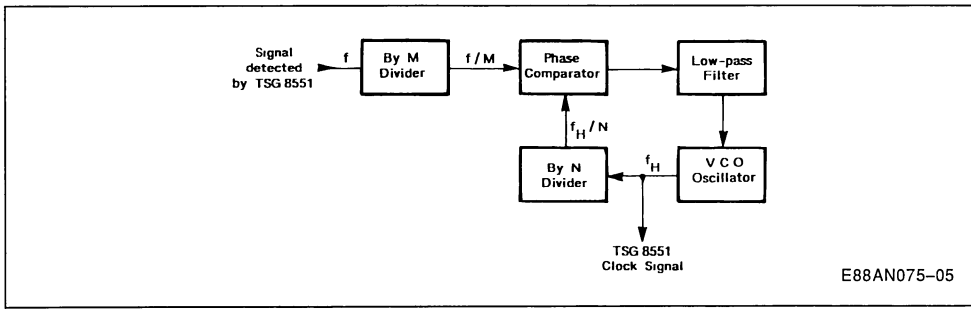
CLOCK FREQUENCY LOCKING

As mentioned earlier, amplitude detection using a highly selective filter such as TSG8551 requires perfect frequency stability of both, the signal to be detected and the filter clock frequency which determines the band-pass center frequency. Otherwise, frequency beating between the filter center frequency and the signal frequency would be produced - resulting in amplitude modulation of the filter output signal.

If the signal frequency is stable, it is an easy task to implement a clock oscillator using either of sufficiently stable quartz or ceramic resonators.

In general, the signal to be detected is also subject to frequency variations. This requires the filter center frequency to be locked onto the signal frequency. The easiest solution to achieve this requirement is to use a **P**hase **L**ocked **L**oop (**PLL**) operating principles of which are depicted in figure 5.

Figure 5 : Phase Locked Loop Block Diagram.



Phase locking yields :

$$\frac{f}{M} = \frac{fH}{N}$$

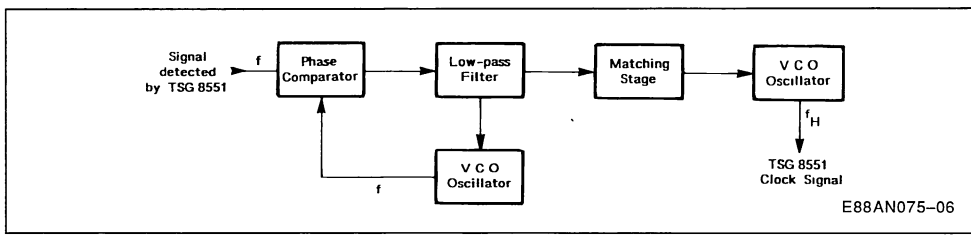
$$\text{i.e. } f_H = \frac{N}{M} f$$

The only requirement is therefore to select N and M values such as to make $\frac{N}{M}$ to correspond to the constant clock frequency-to-TSG8551 center frequency ratio - i.e. "**187.2 1%**".

Thus if one selects **M** = 5 the corresponding **N** value would be **936**.

As illustrated in figure 6, the PLL block diagram outlined in figure 5 can be simplified by removing the frequency divider networks.

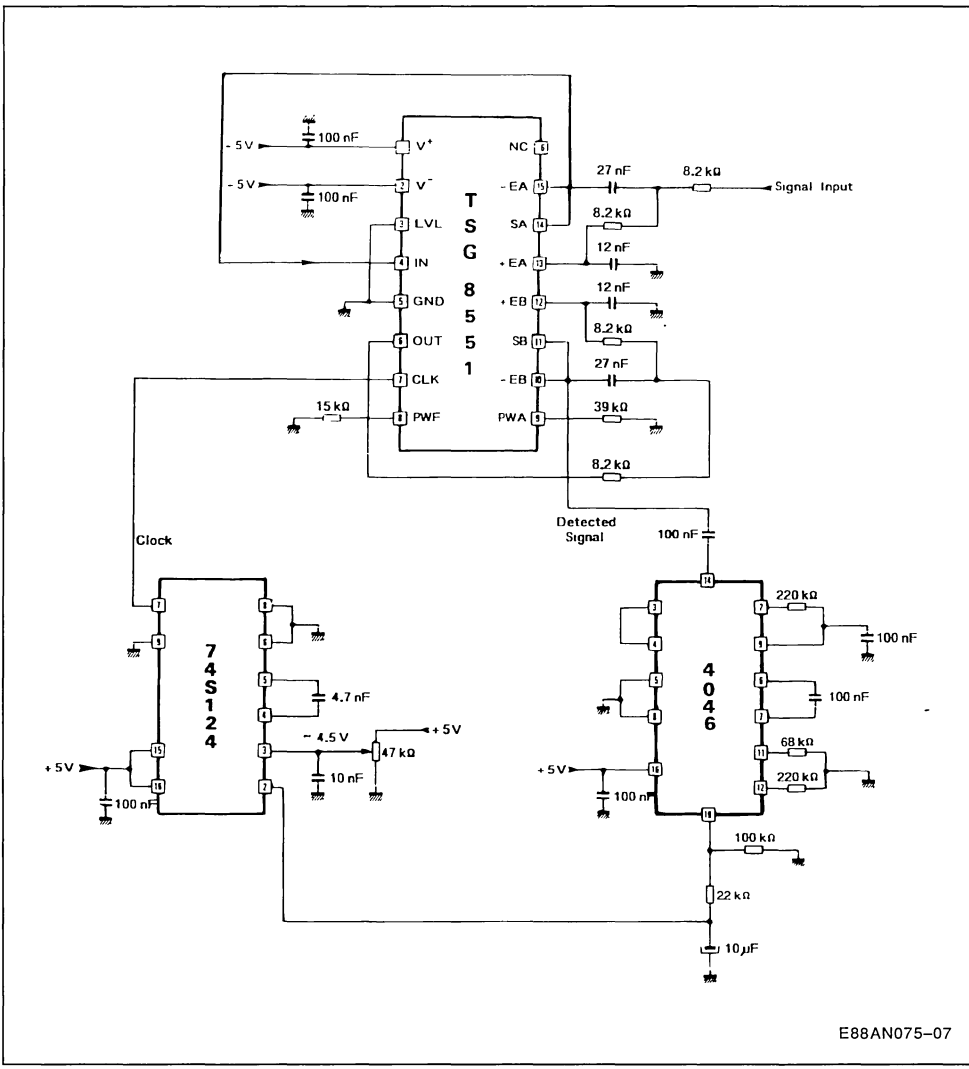
Figure 6 : Simplified PLL Block Diagram.



In this case, the phase is locked onto the frequency of the signal to be detected, and any variation of this frequency will produce an error voltage at the output of low-pass filter. This error voltage goes through a matching stage (amplification, filtering, ..) and is then applied to a **V**oltage-**C**ontrolled **O**scillator (**VCO**) output frequency of which is used as clock for the TSG8551.

Figure 7 depicts the practical application diagram of this arrangement.

Figure 7 : Locking the Clock Frequency onto the Detected Signal Frequency.



The 4046 (CMOS) device fulfils PLL functions while the 74S124 (TTL) circuit generates the clock signal. This application is well suited to amplitude detection of medium frequency signals " **190Hz ".**

The component values given in figure 7 allow the PLL to remain locked within a frequency range of ± **25Hz** around the **190Hz** - and if the input signal amplitude is constant, the amplitude of the detected signal would remain constant within a ± **10Hz** range around the **190Hz**.

It is obvious that the PLL operates ideally within the latter frequency range and as a consequence, the implemented filter is a true tracking filter.

However, filtering of the 4046 device output voltage produces a time constant of approximately 0.2 second. Consequently, the given configuration can follow only relatively low frequency variations of the signal to be detected - "about **10Hz/sec** max." - which corresponds to the characteristics of this type of application (frequency drift with aging and tem-

perature). A drawback associated to this type of PLL is the risk of locking onto an undesired interference signal the frequency of which falls within the capture range. For this reason and in order to limit the noise spectrum, the signal goes through an anti-aliasing filter before entering the filter input. Similarly, a smoothing filter is inserted between the filter output and the phase comparator input. These filters are implemented by Sallen-Key Cells using the filter operational amplifiers. If required, the PLL capture range can be readily reduced.

FREQUENCY DETECTION

The most frequent application is the detection of presence or the absence of a signal at a given frequency.

Thanks to its high selectivity and gain, the TSG8551 is particularly suitable for this type of applications.

By adjusting its clock frequency, the TSG8551 center frequency can vary from a few tens of Hertz (22Hz typ.) to few tens of kilo Hertz (20.3kHz typ.). As outlined in the previous section, a highly stable clock oscillator together with precautions to avoid parasitic signals are the major requirements for appropriate and error-free signal detection.

In general, the detected frequency must, after filtering, go through a signal shaping stage in order to become suitable for use by other devices.

The TSG8551 output signal can be made TTL-compatible by using one of the on-chip operational amplifiers configured as Schmitt Trigger.

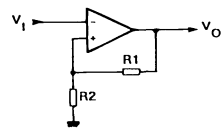
Figure 8 outlines the operating fundamentals of the Schmitt trigger. Selecting a low hysteresis ratio, the amplifier output flips between the two saturation voltages at low amplitude input signals.

Figure 8 : Schmitt Trigger Operating Fundamentals.

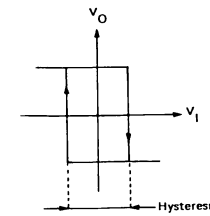
A low positive feed-back is applied to the amplifier by feeding the reference input with a fraction of the output voltage. Due to hysteresis, the output voltage level change does not occur at the same voltage level for input voltage rising or falling. The hysteresis ratio is determined by :

$$V_O \frac{R2}{R1 + R2}$$

Note that the illustrated trigger is of inverting type.



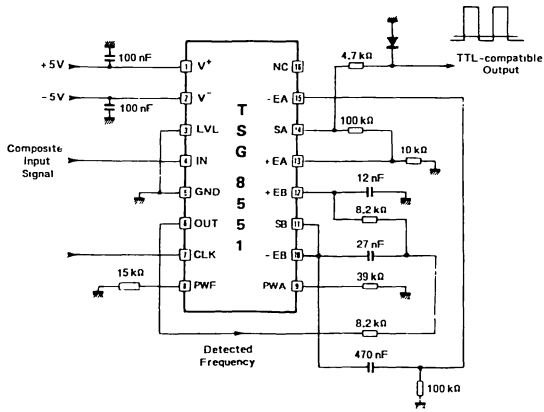
E88AN075–08



E88AN075–09

Figure 9 illustrates the practical application diagram with TSG8551 configured for frequency detection.

Figure 9 : Frequency Detection & TTL–Compatible Output (component values of the smoothing filter apply to a frequency of approximately 200Hz).



E88AN075–10

The 100kΩ and 10kΩ resistors set the hysteresis at 1/10th of the amplifier saturation voltage. Trigger thresholds are therefore **– 450mV** and **+ 300mV** approximately. Consequently, the trigger will operate satisfactorily when the TSG8551 output signal reaches **1V** peak-to-peak (500mV amplitude).

The 1V peak-to-peak output level corresponds to an approximately **30mV** peak-to-peak filter signal input. The voltage at trigger output swings between **– 5V** and **+ 3.5V** for TSG8551 symmetrical power supply of **– 5V, + 5V**.

A diode connected to the output stops the negative half-cycle and makes the signal compatible for use with TTL devices (typical levels : **– 0.6V, + 3.5V**).

Note that in order to avoid offset problems at the filter output, the signal goes through a 470nF capacitor before entering the trigger.

The output signal is sampled by the switched capacitor filter and needs smoothing before going through the Schmitt trigger for shaping.

BURST DURATION DETECTION

Another application of signal detection at a given frequency is the measurement of the signal burst duration. In this case, the burst must be detected without introducing any delay. One must therefore select a filter the group delay of which is compatible with the burst duration at the frequency under consideration. Generally, a group delay equal to 1/10 th of the burst duration is acceptable.

Oscillogram of figure 10 illustrates the burst detection of a 190Hz signal frequency using **TSG8550** filter particularly suitable for this type of application.

The **TSG8550** is a band-pass filter with its gain at center frequency and selectivity factor equal to **0dB** and **7** respectively.

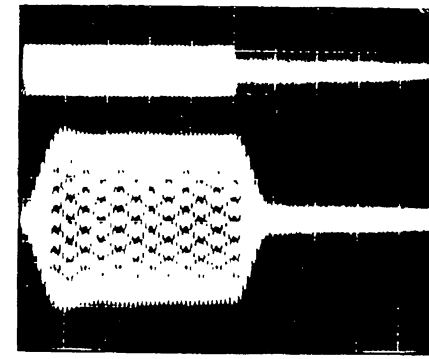
Its group delay at **190Hz** center frequency is about **22ms** - making it suitable for burst detection of at least **250ms** duration as shown in figure 10.

The application configuration used is a straightforward typical arrangement of the switched capacitor filters and does not include any anti-aliasing or smoothing filter.

Figure 10 : BURST DURATION DETECTION using **TSG8550**

- Signal Frequency : **190Hz**
- **Waveform 1** (upper)
  - Filter input : **200mV/div**
- **Waveform 2** (lower)
  - Filter output : **50mV/div**
- **t = 50ms/div**

Comment : The filter is suitable for signal detection at this frequency



E88AN075–11

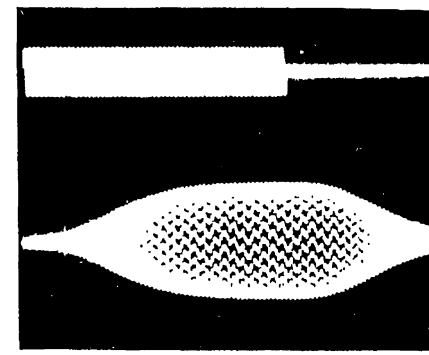
The oscillogram of figure 11 depicts the results obtained using **TSG8551** filter the group delay of which is about ten times higher than that of **TSG8550** ; i.e. about **200ms** at **190Hz** frequency.

It can be seen that the output burst is distorted because of an important delay during rising and falling phases.

Figure 11 : BURST DURATION DETECTION using **TSG8551**

- Signal Frequency : **190Hz**
- **Waveform 1** (upper)
  - Filter input : **200mV/div**
- **Waveform 2** (lower)
  - Filter output : **2V/div**
- **t = 50ms/div**

Comment : The filter exhibits a relatively high group delay for this frequency



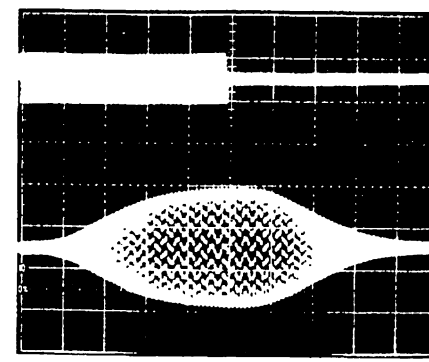
E88AN075–12

Note that the group delay is independent of the signal amplitude and inversely proportional to the signal frequency - as indicated by the oscillogram of figure 12 where the measured settling time is **20ms** for a **2kHz** signal frequency filtered by TSG8551.

Figure 12 : BURST DURATION DETECTION using **TSG8551**

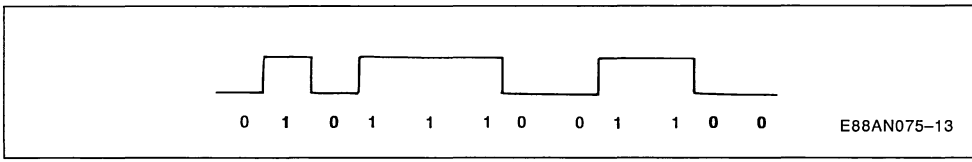
- Signal Frequency : **2kHz**
- **Waveform 1** (upper)
  - Filter input : **100mV/div**
- **Waveform 2** (lower)
  - Filter output : **1V/div**
- **t = 5ms/div**

Comment : The group delay is independent of the signal amplitude and inversely proportional to the signal frequency.



E88AN075–12

As the foregoing discussion demonstrated, a switched capacitor filter can be used to detect the presence and the burst duration of a signal. This type of application is used for data detection - e.g. detection of a binary code transmitted using on-off frequency modulation technique as shown below :



A microprocessor unit can be used to process the signal and, for example, to compare it with the contents of a ROM. After detection by switched capacitor filter, a single R-C low-pass cell is sufficient to extract the signal envelope.

Applications are numerous : remote-control, data transmission on teleprinters, etc ..

CONCLUSION

Wide range of currently available SGS-THOMSON Switched Capacitor Filters provide for appropriate selection of suitable filters meeting the requirements of every specific signal detection application.

The types most often used are standard band-pass filters, which in combination with the on-chip operational amplifiers, greatly simplify the design of signal detection applications. Also, such configuration arrangement offers the possibility of implementing additional functions related to signal detection such as rectification, signal shaping, signal amplification, etc... .

A true tracking filter is implemented by locking the filter clock onto the frequency of the signal to be detected.

The signal detection topic covers a wide range of applications - few examples of which were detailed throughout the present discussion. A single integrated filter associated to a few low-cost components, enables the design of complex functions.

VERY LOW DISTORTION SINEWAVE GENERATOR

INTRODUCTION

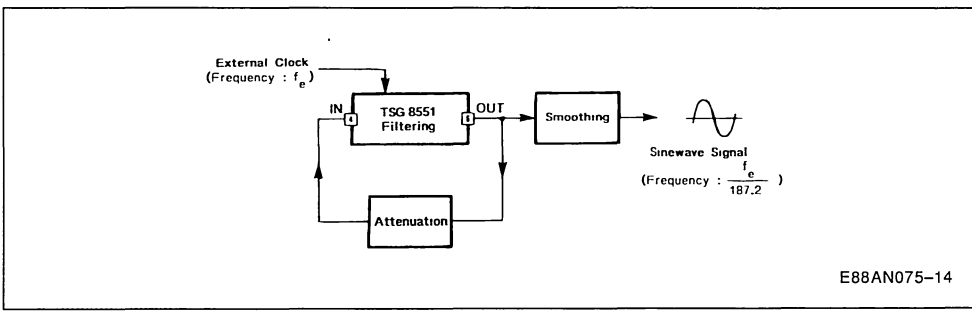
Thanks to its high coefficient of selectivity, the **TSG8551** filter is best suited to this application. This filter can extract from a complex signal, the component located at the filter center frequency.

In all cases, the TSG8551 output signal is nearly a pure frequency waveform, i.e. a sinewave.

We shall use this property to implement a sinewave generator, **using only a single TSG8551 package**.

Various configuration arrangements will be discussed and it will be demonstrated that thanks to the remarkable characteristics of the switched capacitor filters, there is a tremendous number of application possibilities for this type of oscillators.

Figure 13 : Sinewave Generator Block Diagram.



OPERATING PRINCIPLES

If a TSG8551 filter is configured in closed-loop, it begins oscillating at its center frequency.

Due to high filter gain and in order to avoid the saturation of the output stage, it is necessary to insert an attenuator within the feed-back loop.

With suitable attenuation, the filter output signal will be a sampled sinewave, and must go through a smoothing filter to obtain the final sinewave - the frequency of which will be proportional to the clock frequency.

IMPLEMENTATION

The most delicate task of this configuration is the design of the feed-back loop attenuator. In fact, an ordinary potentiometer cannot fulfil this requirement since too low an attenuation will cause the filter output signal amplitude to rise to the saturation level, while excessive attenuation will result in the signal amplitude falling gradually until the oscillator is completely halted. It is thus clear that the position of balance is quite unstable using a potentiometer.

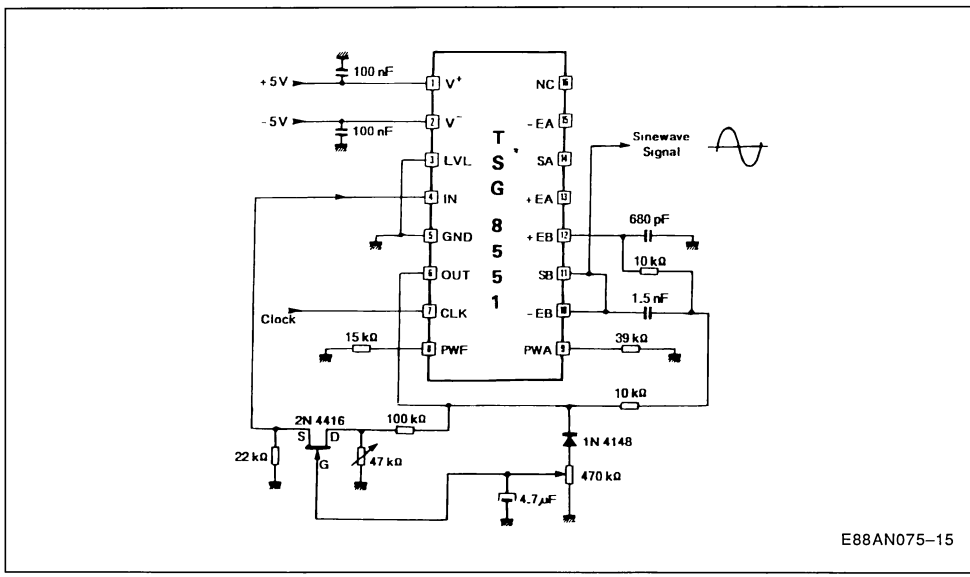
ALTERNATIVE 1 (figure 14)

The appropriate solution is to design a true **A**utomatic **G**ain **C**ontrol (**AGC**).

A simple configuration can be obtained resorting to the properties of the **F**ield **E**ffect **T**ransistors (**FET**) which behave as variable resistors as a function of the voltage applied to the gate.

The FET is used as a potentiometer, the gate biasing voltage is supplied by the negative amplitude of the output signal which is rectified by a diode and filtered by a capacitor. An N-channel FET is used here, so that, when the output signal rises, the gate voltage becomes more negative and therefore the FET conducts less, resulting in filter input signal attenuation.

Figure 14 : Sinewave Generator (with AGC).



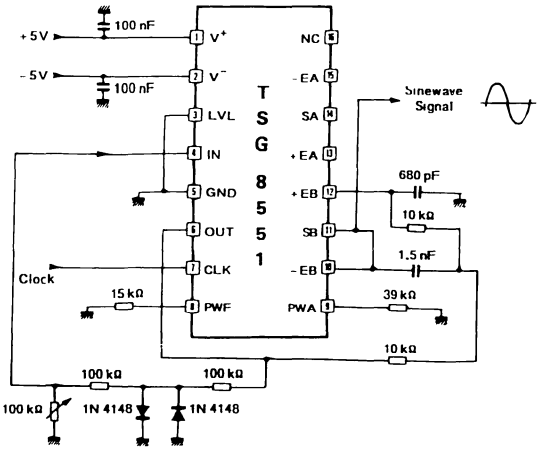
Inversely, when the output signal level falls, the transistor conducts more and as a consequence, the input signal amplitude rises. A potentiometer placed before the FET attenuates the output signal so as to enable the FET to operate at low drain-source voltage levels, i.e. within characteristic area where drain to source resistance varies linearly as a function of the gate voltage.

This configuration delivers a stable output signal amplitude of approximately 5V peak-to-peak irrespective of the clock frequency within the operating frequency range of the TSG8551 (center frequency : 20Hz to 20kHz). Sinewave smoothing is performed by one of the filter operational amplifiers configured in second-order low-pass (Sallen-key structure).

ALTERNATIVE 2 (figure 15)

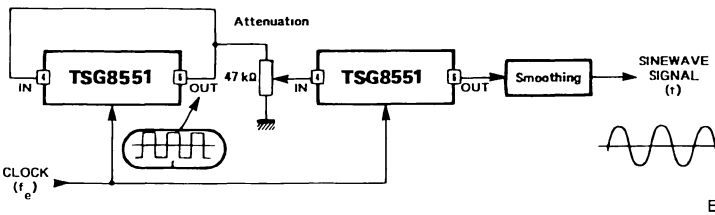
In this case, the output signal is clipped by two inverse-parallel connected diodes. This arrangement results in constant signal amplitude whatever the output signal amplitude (provided that it is higher than the diode threshold). A potentiometer allows to set the input level at a constant value and therefore adjust the output amplitude so as to avoid saturation.

Figure 15 : Sinewave Generator (with amplitude adjustment).



This simplified arrangement gives satisfactory results within the entire frequency range. The output sinewave **distortion** is about **0.2%** (total harmonic distortion).

Figure 16.



ALTERNATIVE 3

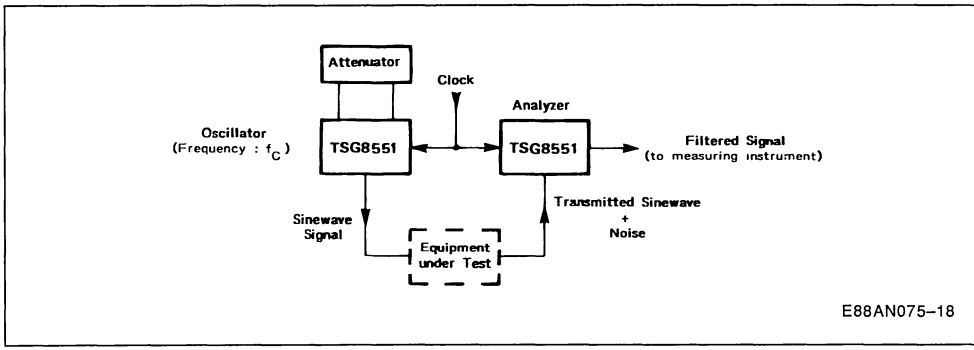
This solution if of simple implementation - attenuator adjustment does not involve any complication, but the configuration requires two TSG8551 filter packages.

The first TSG8551 is configured in closed-loop and therefore delivers a constant amplitude square waveform with its frequency equal to the filter center frequency. The filter power supply voltages determine the saturation voltages of the output amplifier and hence the signal amplitude. If this signal is sufficiently attenuated and then filtered once again by another TSG8551 centered on the same frequency, then a pure sinewave corresponding to the fundamental signal component would be obtained. Both TSG8551 filters are therefore driven by the same clock frequency and the smoothing is performed as previously using one of the filter operational amplifiers.

APPLICATIONS

- Since the frequency of the output sinewave is readily adjustable by the clock frequency, the first application of this oscillator is **Low Frequency Signal Generator.**
- Using an operational amplifier, the generated sinewave can be easily converted to **square** and **triangular waveforms.**
- If a VCO is used for clock generation, then the sinewave frequency can be modified by the voltage applied to the VCO. This property can be used for **frequency** (or **phase**) **modulation.**
- An interesting application using two TSG8551 filters is as follows :

Figure 17 : Network Analyzer.



The first filter operates as sinewave oscillator as discussed earlier while the second filter being driven by the same clock frequency, is automatically tuned at a center frequency equal to the oscillator frequency.

This configuration can be used to implement a **selective voltmeter** or a **network analyzer**. The oscillator signal is applied to the input of the device under test the output signal of which goes through the second TSG8551 and is then transmitted towards a measuring or recording instrument. Modifying the clock frequency, the entire low frequency range is scanned while the analyzing filter remains tuned on the input signal frequency.

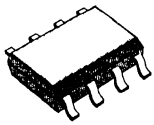
CONCLUSION

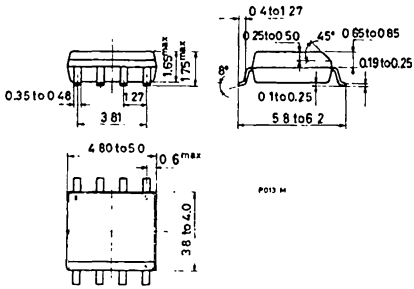
Section 3 covered original design ideas built around switched capacitor filters which depart slightly from typical applications. This should enable the designer to explore new applications by taking full advantage of the flexibility of use inherent to switched capacitor filters. These filters can be undoubtedly integrated into other application configurations thus offering **design simplification** and **performance enhancement.**

PACKAGES

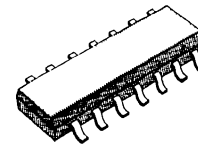
NOTES

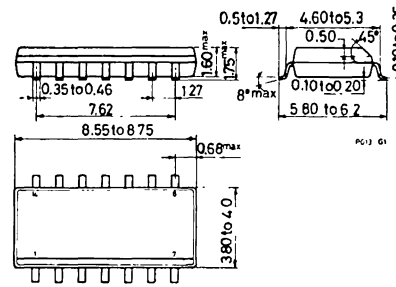
SO-8J





SO-14J





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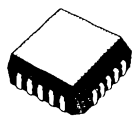

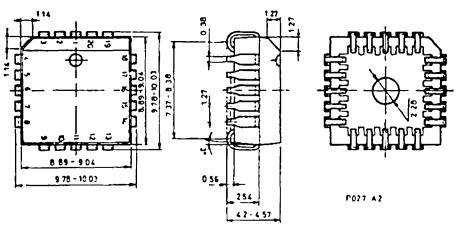

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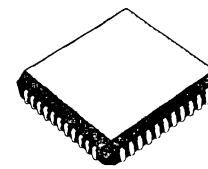
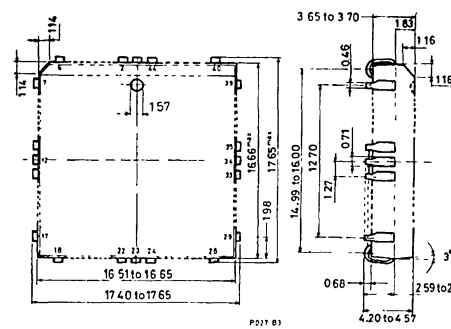
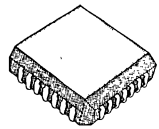
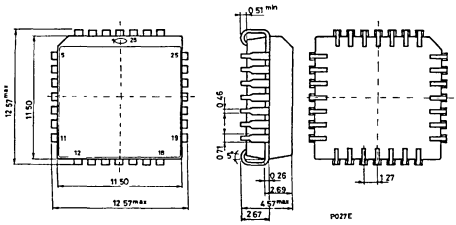


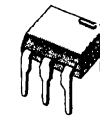


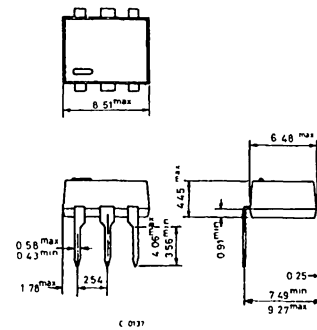
PLCC-28 Plastic Chip Carrier



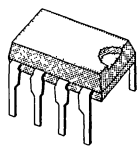


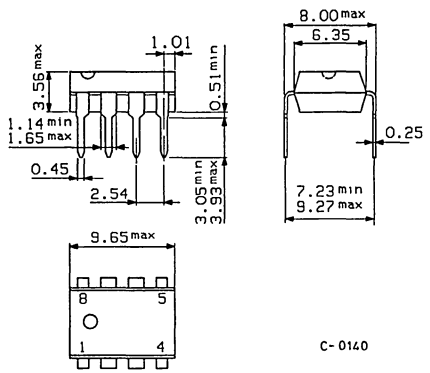
DIP-6



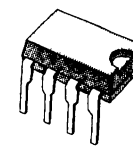


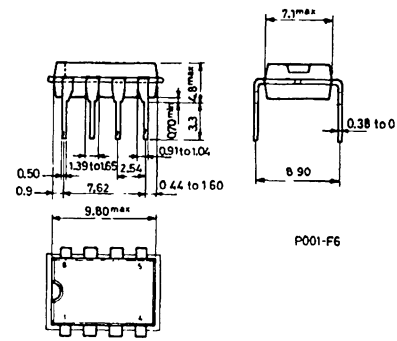
Minidip A Plastic



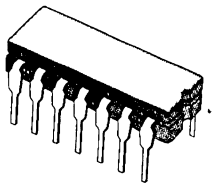


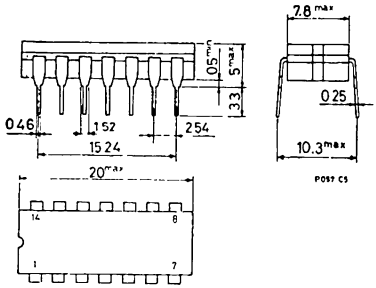
8 lead Plastic Minidip



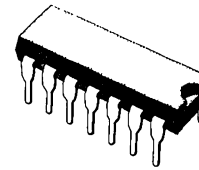


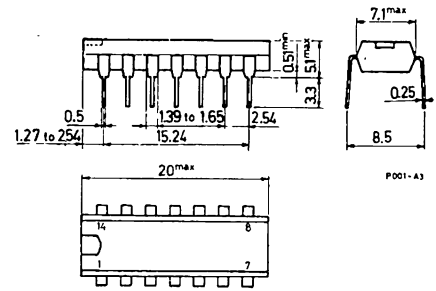
14 lead Ceramic Dip



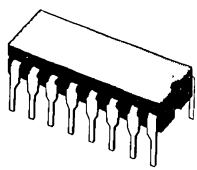


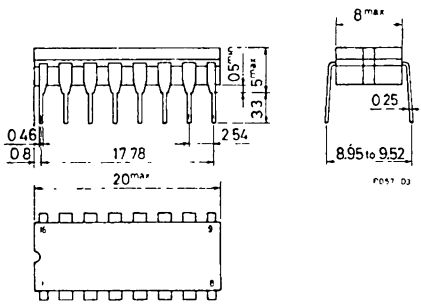
14 lead Plastic Dip



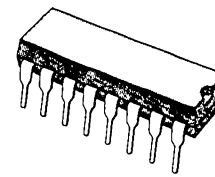


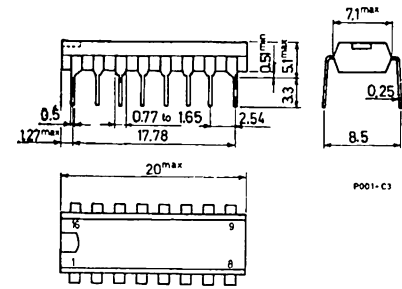
16 lead Ceramic Dip





16 lead Plastic Dip (0.25)





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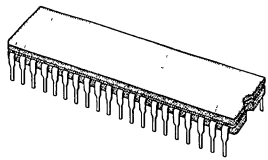
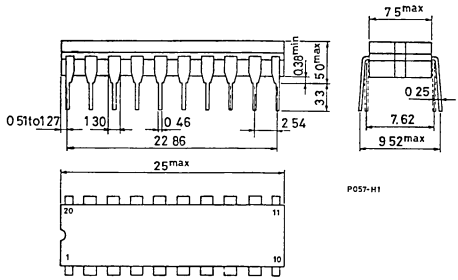
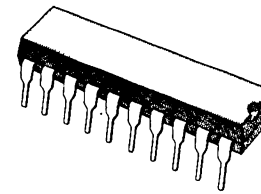
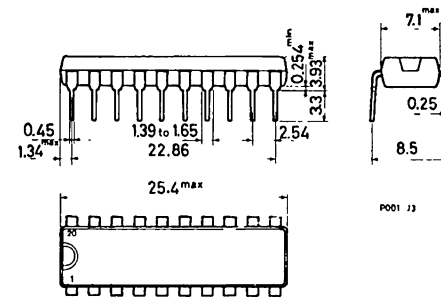




20 lead Plastic Dip (0.25)





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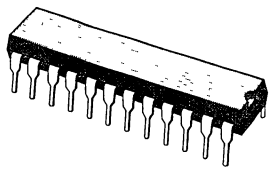
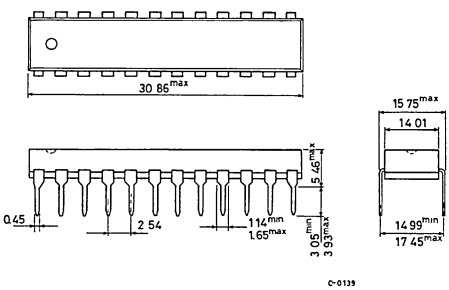
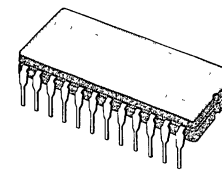
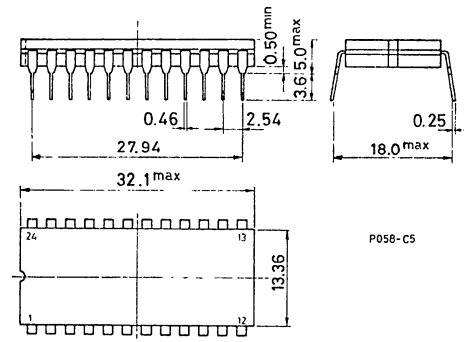


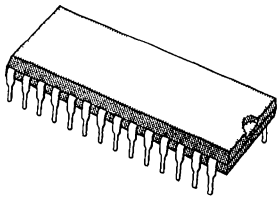


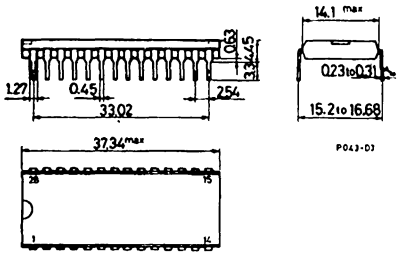
DIP-24 Ceramic (0.25)





28 lead Plastic Dip





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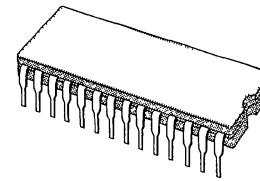
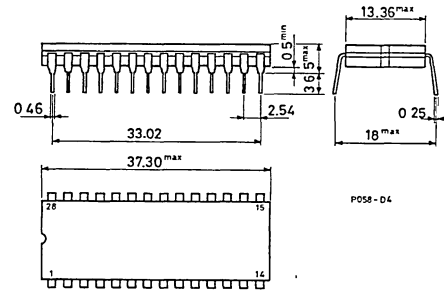
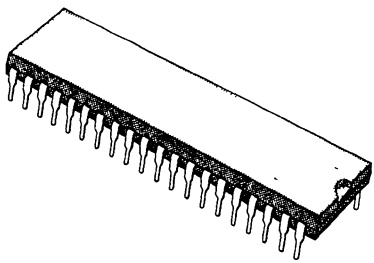
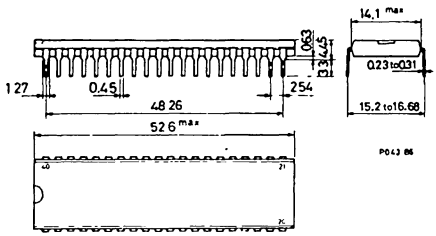


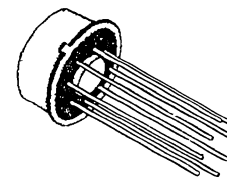


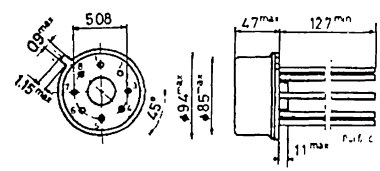
40 lead Plastic Dip





TO-99





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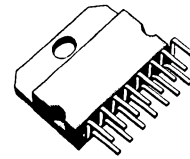

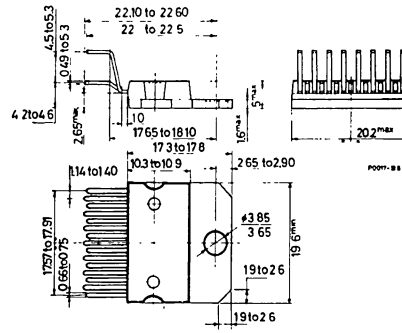

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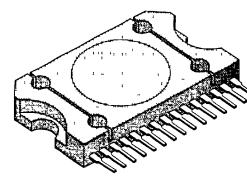

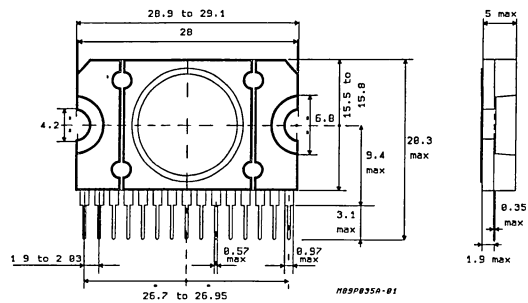

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Cover design by Keith & Koppel, Segrate, Italy
Typesetting and layout on Desk Top Publishing
by AZIMUT, Hénin Bt., France

Printed by Garzanti, Cernusco S/N, Italy

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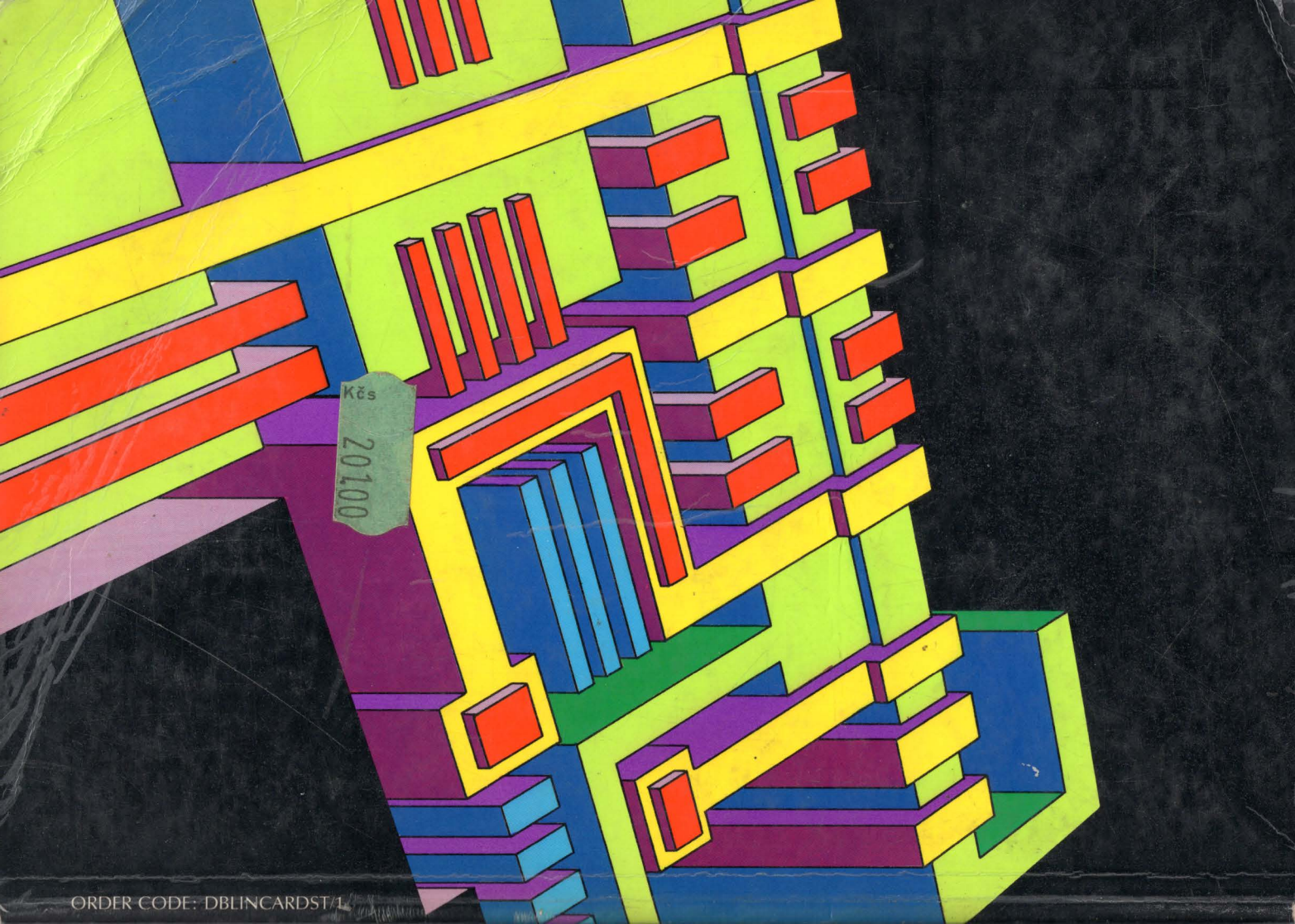

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