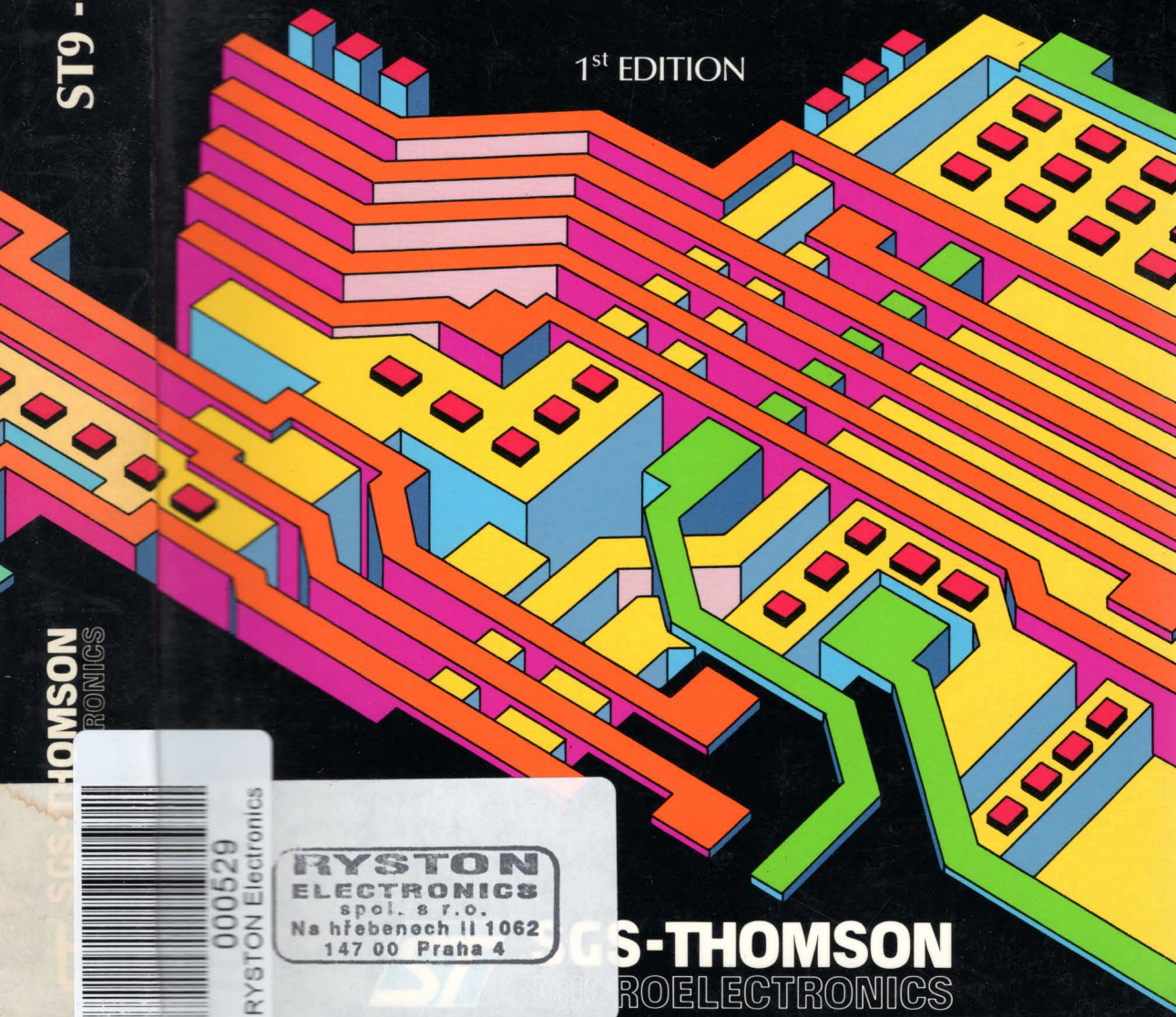
ST9 FAMILY 8/16 BIT MCU

DATABOOK

1st EDITION



SGS-THOMSON MICROELECTRONICS

ST9 - DATABOOK

ST9 FAMILY
8/16 BIT MCU

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1st EDITION

JULY 1991

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2. A critical component is any component of a life support device or system whose failure to perform can reasonably be expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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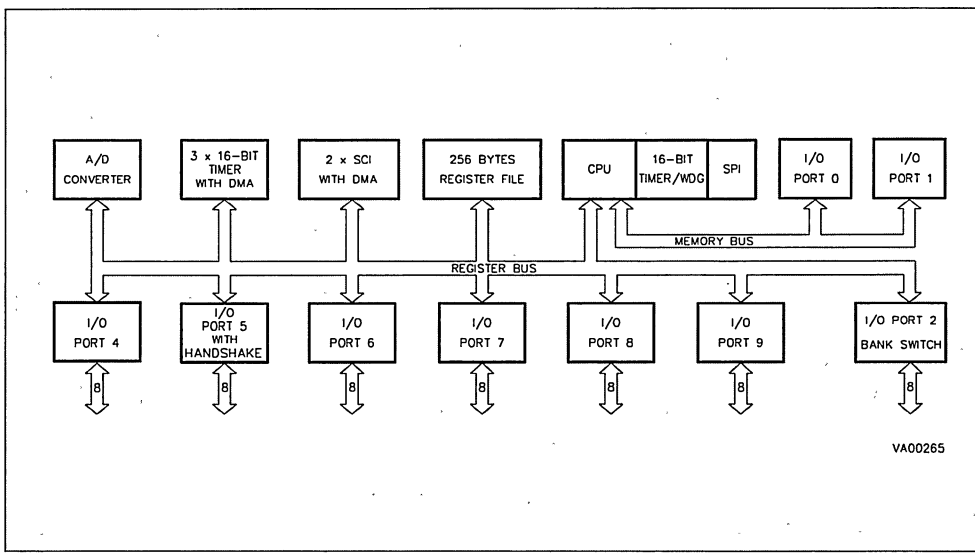
INTRODUCTION

Driven by the new advanced technologies developed internally by SGS-THOMSON Microelectronics, the ST9 family of microcontrollers offers advanced peripheral functions, an 8/16 bit core and ROM/EPROM/EEPROM plus RAM capabilities. This family of products is based on a common core of features, with variations in the peripheral organisation to suit the different requirements of the middle to high end embedded applications.

The ST9 family of microcontrollers offers a powerful CISC based Core, capable of 16 bit operations, built in Timer Watchdog functions for secure operation, Serial Peripheral Interfaces adaptable to low-cost external I^2C-bus, S-bus and IM-bus devices plus an external memory interface with full, expandable vectored interrupt and DMA facilities. The instruction set encompasses 14 addressing modes linked with 187 instruction types with special instructions added for improved efficiency of the high level language development tools.

The peripherals linked to this Core include Multifunction Timers, with operating modes to cover almost all timing requirements, including the optior of DMA to the timing constants and the triggering of other on-chip peripherals such as the Analog-to-Digital Converter. This converter, offering 8 bit resolution, includes an automatic threshold sensing watchdog on two of its 8 multiplexed input channels. Serial communication is handled (in addition to the SPI) by the Serial Communication is Interface, a fast asynchronous and byte synchronous interface with capability. This, together with the automatic DMA operation and the Address/9th bit of the character word, simplifies network operation.



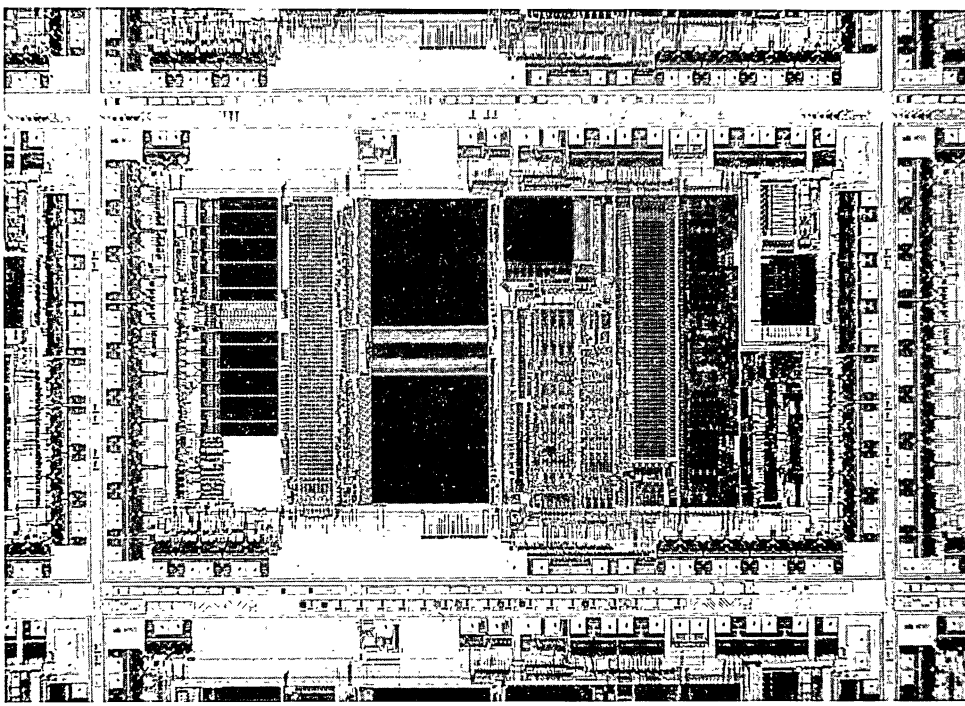
Core and megacell Library

INTRODUCTION

Memory options range from ROMLESS devices for flexibility, EPROM based prototyping vehicles, OTP for pre-production runs and ROM for volume production in the 64K program space, while the separate 64K data space (expandable to 8M bytes for both program and data spaces with the Bankswitch logic) includes RAM and high-reliability EEPROM. The RAM exists in addition to the versatile Register File - 224 General Purpose Registers all with Arithmetic (8 and 16 bit) capability, Stack, and Index pointer mechanisms, and functions as fast access RAM memory. 16 Registers hold the system functions, the two independent stack pointers and I/O port data registers for immediate access, while the top 16 bytes of the Register File is paged, with pages containing the standard peripheral data and control registers.

New peripheral functions are in development to expand the ST9 family, leading to devices suitable for applications ranging from TV and VCR to Automotive Multiplex Wiring Systems and High Security banking applications.

The selection guide which follows in the next section shows the current ST9 family members, with all the packaging options.

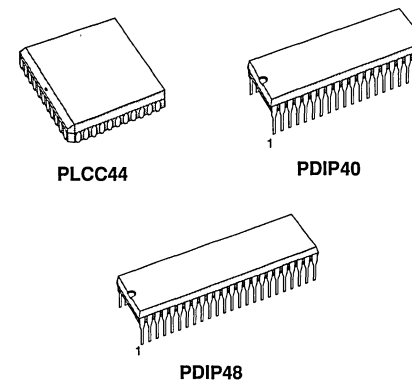


ST90E40

DATASHEETS

16K ROM HCMOS MCUs WITH RAM

- Single chip microcontroller with 16K bytes of ROM, 256 bytes of RAM and 256 bytes of register file with 224 general purpose registers available as RAM, accumulators or index pointers.
- 8/16 bit CORE with full feature DMA controller, a powerful interrupt handler and a Standard Serial Peripheral Interface (SPI) handling S-bus, I^2C-bus, IM-bus and Standard Serial Peripheral Interfaces.
- Up to 8 external interrupts edge-selectable plus 1 non-maskable interrupt.
- 16 bit programmable Timer with 8 bit Prescaler, able to be used as a Watchdog Timer for system integrity.
- A 16 bit Multifunction Timer module, with an 8 bit prescaler and 12 operating modes, allowing simple use for complex waveform generation and measurement, PWM functions and many other system timing operations.
- Full function Serial Communications Interface with 110 to 375000 baud rate generator, asynchronous and byte synchronous capability (fully programmable format) and address/wake-up bit option.
- On-chip DMA channels associated to the Multifunction Timer and the Serial Communications Interface.
- Up to five 8 bit I/O ports with programmable input thresholds and output characteristics. Alternative functions allow the full use of all pins.
- Powerful software development tools, including assembler, linker, C-compiler, archiver, software and hardware emulators.
- Windowed and One Time Programmable EPROM parts available for prototyping and pre-production development phases.
- 48-pin Dual in Line Plastic package for ST9026.
- 40-pin Dual in Line Plastic package for ST9027.
- 44-lead Plastic Leaded Chip Carrier package for ST9028.



(Ordering Information at the end of the datasheet)

Figure 1. ST9026 Pin Configuration

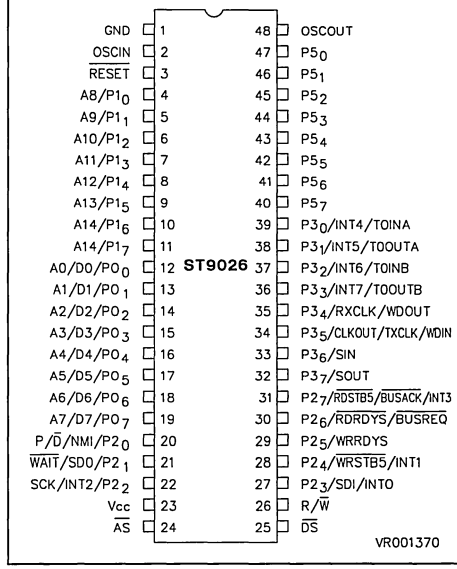


Figure 2. ST9027 Pin Configuration

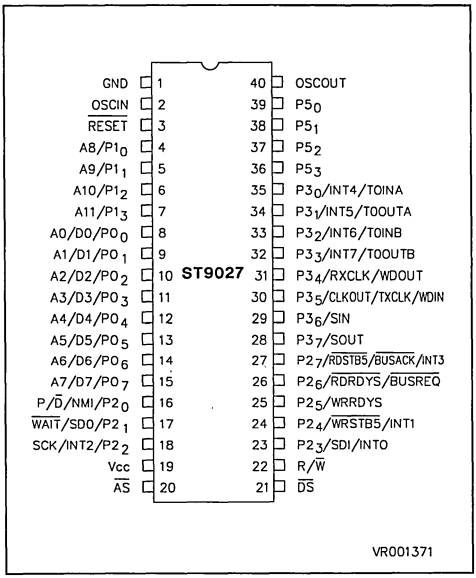


Figure 3. ST9028 Pin Configuration

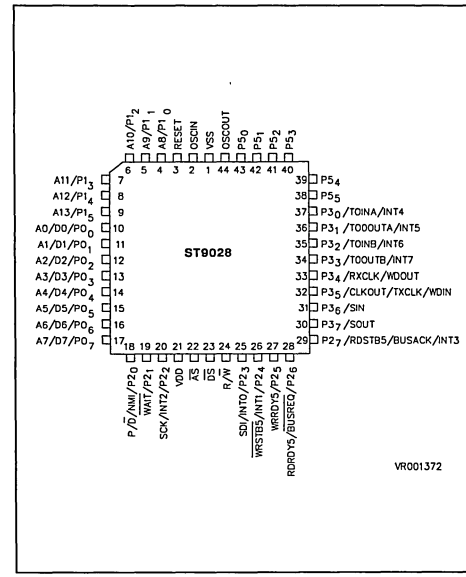
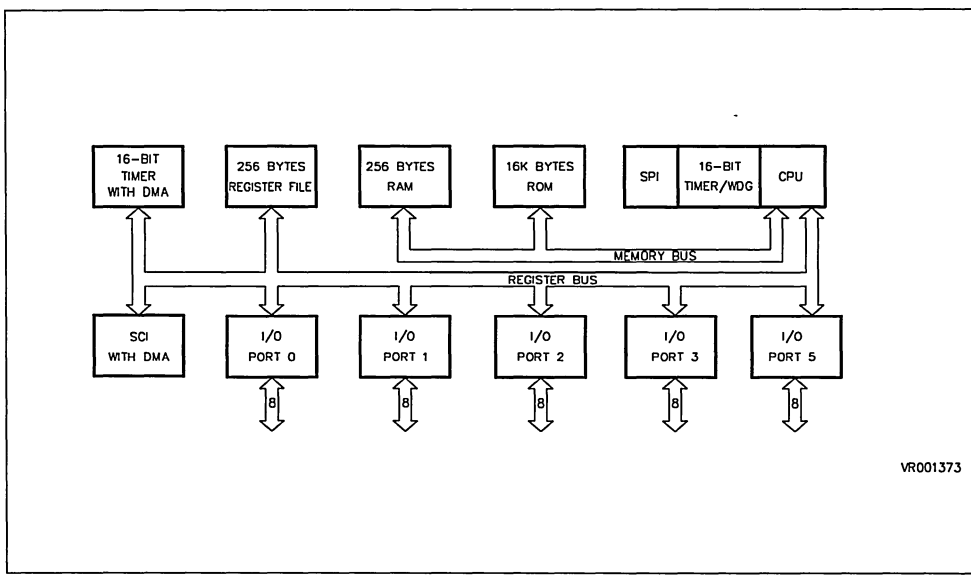


Figure 4. ST902X Block Diagram



Note : Refer to Table 1 for ST902X I/O PORT SUMMARY.

GENERAL DESCRIPTION

The ST9026, ST9027 and ST9028 (following mentioned as ST902X) are ROM members of the ST9 family of microcontrollers, completely developed and produced by SGS-THOMSON Microelectronics using a proprietary n-well HCMOS process.

The ROM parts are fully compatible with their EPROM versions, which may be used for the prototyping and pre-production phases of development, and can be configured as: standalone microcontrollers with 16K bytes of on-chip ROM, microcontrollers able to manage up to 112K bytes of external memory, or as parallel processing elements in a system with other processors and peripheral controllers.

A key point of the ST902X architecture is its modular approach which allows software commonality with all other members of the ST9 family.

The nucleus of the modular design of the ST902X is the advanced Core which includes the Central Processing Unit (CPU), the Register File, a 16 bit Timer/Watchdog with 8 bit Prescaler, a Serial Peripheral Interface supporting S-bus, I^2C-bus and IM-bus Interface, plus two 8 bit I/O ports. The Core has independent memory and register buses allowing a high degree of pipelining to add to the efficiency of the code execution speed of the extensive instruction set.

The powerful I/O capabilities demanded by microcontroller applications are fulfilled by the ST902X with up to 40 I/O lines dedicated to digital Input/Output. These lines are grouped into up to five 8 bit I/O Ports and can be configured on a bit basis under software control to provide timing, status signals, an address/data bus for interfacing external memory, timer inputs and outputs, external interrupts and serial or parallel I/O with or without handshake.

Three basic memory spaces are available to support this wide range of configurations: Program Memory (internal and external), Data Memory (external) and the Register File, which includes the control and status registers of the on-chip peripherals.

The 16 bit MultiFunction Timer, with an 8 bit Prescaler and 12 operating modes allows simple use for complex waveform generation and measurement, PWM functions and many other system timing functions by the usage of the two associated DMA channels for each timer.

Completing the device is a full duplex Serial Communications Interface with an integral 110 to 375000 baud rate generator, asynchronous and byte synchronous capability (fully programmable format) and associated address/wake-up option, plus two DMA channels.

PIN DESCRIPTION

$\overline{AS}$. *Address Strobe (output, active low, 3-state).* Address Strobe is pulsed low once at the beginning of each memory cycle. The rising edge of $\overline{AS}$ indicates that address, Read/Write (R/$\overline{W}$), and Data Memory signals are valid for program or data memory transfers. Under program control, $\overline{AS}$ can be placed in a high-impedance state along with Port 0 and Port 1, Data Strobe ($\overline{DS}$) and R/$\overline{W}$.

$\overline{DS}$. *Data Strobe (output, active low, 3-state).* Data Strobe provides the timing for data movement to or from Port 0 for each memory transfer. During a write cycle, data out is valid at the leading edge of $\overline{DS}$. During a read cycle, Data In must be valid prior to the trailing edge of $\overline{DS}$. When the ST902X accesses on-chip memory, $\overline{DS}$ is held high during the whole memory cycle. It can be placed in a high impedance state along with Port 0, Port 1, $\overline{AS}$ and R/$\overline{W}$.

R/$\overline{W}$. *Read/Write (output, 3-state).* Read/Write determines the direction of data transfer for external memory transactions. R/$\overline{W}$ is low when writing to external program or data memory, and high for all other transactions. It can be placed in a high impedance state along with Port 0, Port 1, $\overline{AS}$ and $\overline{DS}$.

$\overline{RESET}$. *Reset (input, active low).* The ST9 is initialised by the Reset signal. With the deactivation of $\overline{RESET}$, program execution begins from the Program memory location pointed to by the vector contained in program memory locations 00h and 01h.

OSCIN, OSCOUT. *Oscillator (input and output).* These pins connect a parallel-resonant crystal (24MHz maximum), or an external source to the on-chip clock oscillator and buffer. OSCIN is the input of the oscillator inverter and internal clock generator; OSCOUT is the output of the oscillator inverter.

V_{DD}. Main Power Supply Voltage (+5V ±10%)

V_{SS}. Digital Circuit Ground.

P0.0-P0.7, P1.0-P1.7, P2.0-P2.7 P3.0-P3.7, P5.0-P5.7. *I/O Port Lines (Input/Output, TTL or CMOS compatible).* 8 lines grouped into I/O ports of 8 bits, bit programmable under program control as general purpose I/O or as Alternate functions (see next section).

I/O Port Alternate Functions. Each pin of the I/O ports of the ST902X may assume software programmable Alternative Functions as shown in the Pin Configuration Drawings. Due to Bonding options for the packages, some functions may not be present, Table 1 shows the Functions allocated to each I/O Port pins and a summary of packages for which they are available.

PIN DESCRIPTION (Continued)

Table 1. ST902X I/O Port Alternate Function Summary

I/O PORT	Name	Function	Alternate Function	Pin Assignment		
Port.bit				9026	9027	9028
P0.0	A0/D0	I/O	Address/Data bit 0 mux	12	8	10
P0.1	A1/D1	I/O	Address/Data bit 1 mux	13	9	11
P0.2	A2/D2	I/O	Address/Data bit 2 mux	14	10	12
P0.3	A3/D3	I/O	Address/Data bit 3 mux	15	11	13
P0.4	A4/D4	I/O	Address/Data bit 4 mux	16	12	14
P0.5	A5/D5	I/O	Address/Data bit 5 mux	17	13	15
P0.6	A6/D6	I/O	Address/Data bit 6 mux	18	14	16
P0.7	A7/D7	I/O	Address/Data bit 7 mux	19	15	17
P1.0	A8	O	Address bit 8	4	4	4
P1.1	A9	O	Address bit 9	5	5	5
P1.2	A10	O	Address bit 10	6	6	6
P1.3	A11	O	Address bit 11	7	7	7
P1.4	A12	O	Address bit 12	8		8
P1.5	A13	O	Address bit 13	9		9
P1.6	A14	O	Address bit 14	10		
P1.7	A15	O	Address bit 15	11		
P2.0	NMI	I	Non-Maskable Interrupt	20	16	18
P2.0	P/$\overline{D}$	O	Program/Data Space Select	20	16	18
P2.0	ROMless	I	ROMless Select*	20	16	18
P2.1	SDI	I	SPI Serial Data Out	21	17	19
P2.1	$\overline{WAIT}$	I	External Wait Input	21	17	19
P2.2	INT2	I	External Interrupt 2	22	18	20
P2.2	SCK	O	SPI Serial Clock	22	18	20
P2.3	INT0	I	External Interrupt 0	27	23	25
P2.3	SDO	O	SPI Serial Data In	27	23	25
P2.4	INT1	I	External Interrupt 1	28	24	26
P2.4	$\overline{WRSTB5}$	O	Handshake Write Strobe P5	28	24	26
P2.5	WRRDY5	I	Handshake Write Ready P5	29	25	27
P2.6	RDRDY5	O	Handshake Read Ready P5	30	26	28
P2.6	$\overline{BUSREQ}$	I	External Bus Request	30	26	28

PIN DESCRIPTION (Continued)

Table 1. ST902X I/O Port Alternate Function Summary (Continued)

I/O PORT	Name	Function	Alternate Function	Pin Assignment		
Port.bit				9026	9027	9028
P2.7	INT3	I	External Interrupt 1	31	27	29
P2.7	$\overline{\text{RDSTB5}}$	I	Handshake Read Strobe P5	31	27	29
P2.7	$\overline{\text{BUSACK}}$	O	External Bus Acknowledge	31	27	29
P3.0	INT4	I	External Interrupt 4	39	35	37
P3.0	T0INA	I	MF Timer 0 Input A	39	35	37
P3.1	INT5	I	External Interrupt 5	38	34	36
P3.1	T0OUTA	O	MF Timer 0 Output A	38	34	36
P3.2	INT6	I	External Interrupt 6	37	33	35
P3.2	T0INB	I	MF Timer 0 Input B	37	33	35
P3.3	INT7	I	External Interrupt 7	36	32	34
P3.3	T0OUTB	O	MF Timer 0 Output B	36	32	34
P3.4	RXCLK	I	SCI Receive Clock Input	35	31	33
P3.4	WDOUT	O	T/WD Output	35	31	33
P3.5	CLKOUT	O	SCI Byte Sync Clock Output	34	30	32
P3.5	TXCLK	I	SCI Transmit Clock Input	34	30	32
P3.5	WDIN	I	T/WD Input	34	30	32
P3.6	SIN	I	SCI Serial Input	33	29	31
P3.7	SOUT	O	SCI Serial Output	32	28	32
P3.7	ROMless	I	ROMless Select*	32	28	32
P5.0		I/O	I/O Handshake Port 5	47	39	43
P5.1		I/O	I/O Handshake Port 5	46	38	42
P5.2		I/O	I/O Handshake Port 5	45	37	41
P5.3		I/O	I/O Handshake Port 5	44	36	40
P5.4		I/O	I/O Handshake Port 5	43		39
P5.5		I/O	I/O Handshake Port 5	42		38
P5.6		I/O	I/O Handshake Port 5	41		
P5.7		I/O	I/O Handshake Port 5	40		

*** Note :** Mask Option

ST902X CORE

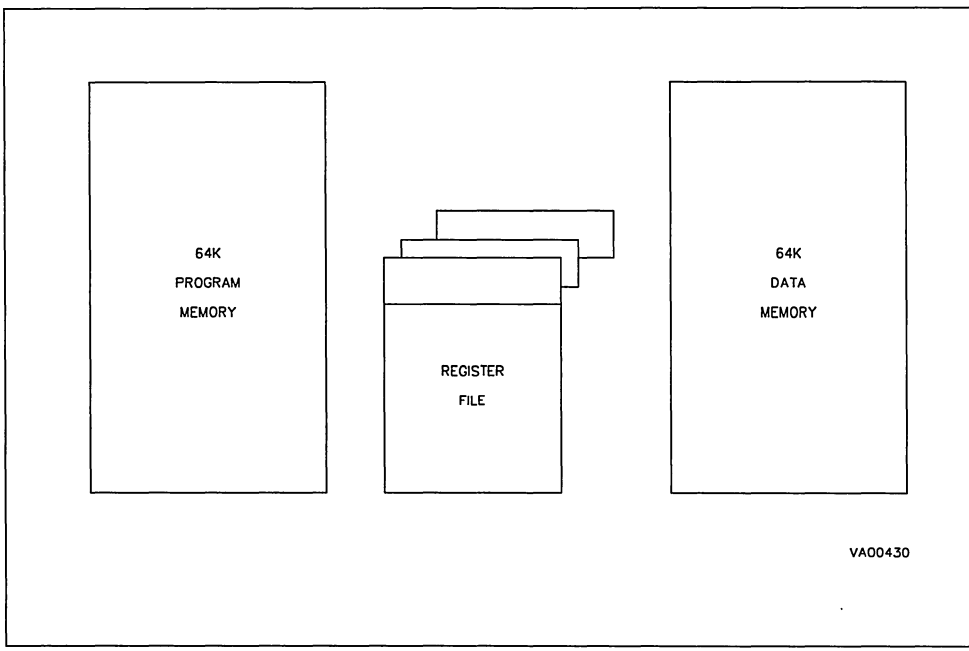
The Core or Central Processing Unit (CPU) of the ST902X includes the 8 bit Arithmetic Logic Unit and the 16 bit Program Counter, System and User Stack Pointers. The microcoded Instruction Set is highly optimised for both byte (8 bit) and word (16 bit) data, BCD and Boolean data types, with 14 addressing modes. Two 8 bit I/O ports are connected to the Core module for external memory interfacing, while a 16 bit Timer/Watchdog gives system security and timing functions, and a Serial Peripheral Interface allows for synchronous communication. Three independent buses are controlled by the Core, a 16 bit Memory bus, an 8 bit Register addressing bus and a 6 bit Interrupt/DMA bus connected to the interrupt and DMA controllers in the on-chip peripherals and the Core. This multiple bus architecture allows a high degree of pipelining and parallel operation within the ST902X, giving it its efficiency in both numerical calculations and communication with the on-chip peripherals.

MEMORY

The memory of the ST902X is functionally divided into two areas, the Register File and Memory. The Memory is divided into two spaces, each having a maximum of 65,536 bytes. The two memory spaces are separated by function, one space for Program code, the other for Data. The ST902X 16K bytes of on-chip ROM memory is selected at memory addresses 0 through 3FFFh (hexadecimal) in the PROGRAM space and the 256 bytes of on-chip RAM memory is selected at memory addresses 0 through 0FFh in the DATA space.

Off-chip memory, addressed using the multiplexed address and data buses (Ports 0 and 1) may be divided into the Program and Data spaces by the external decoding of the Program/Data select pin (P/$\overline{D}$) available as an Alternate function, allowing a full 128K byte memory. The memory spaces are selected by the execution of the SDM and SPM instructions (Set Data Memory and Set Program Memory, respectively). There is no need to use either of these instructions again until the memory

Figure 5. Memory Spaces



MEMORY (Continued)

area required is to be changed. This requirement is not necessary in two cases: first, when operating with external stacks (the Data memory is automatically selected) and, secondly, when using the memory indirect to memory indirect post-increment addressing mode (the memory types are specified in the instructions: LDPP, LDPD, LDDP, LDDD).

Either the Data Memory or the Program Memory can be addressed using any of the memory addressing modes.

Program Space

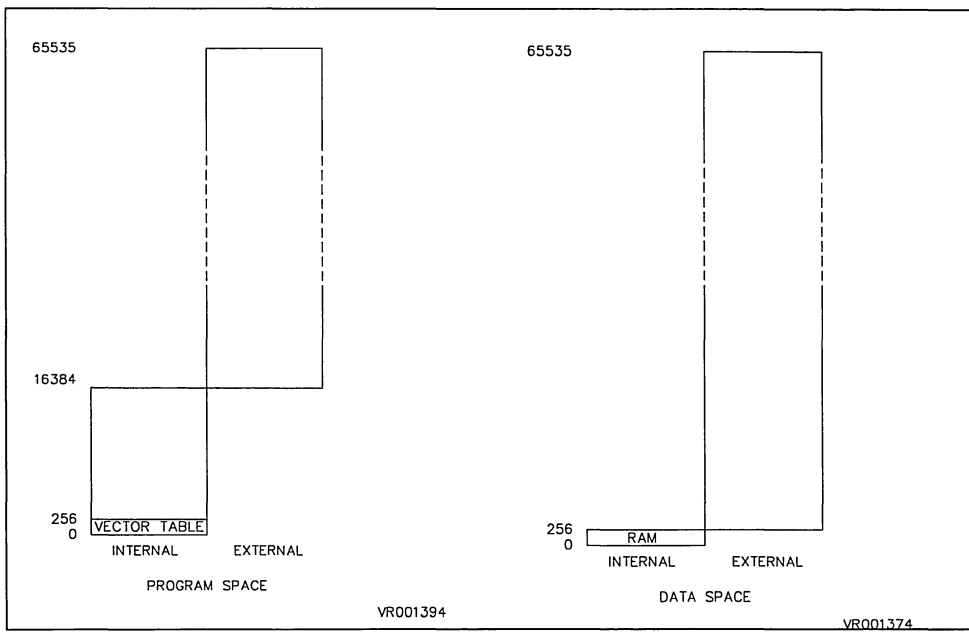
The Program memory space of the ST902X, from the 16K bytes of on-chip ROM memory to the full 64K bytes with off-chip memory expansion, is fully available to the user. At addresses greater than the first 16K bytes of program space, the ST902X executes external memory cycles for instruction fetches. The first 256 memory locations from address 0 to 0FFh (hexadecimal) hold the Reset Vector, the Top-Level (Pseudo Non-Maskable) interrupt, the Divide by Zero Trap vector and, optionally, the interrupt vector table for use with the on-chip peripherals and the external interrupt sources. Each vector is contained in two consecutive byte locations, the high order address held in the lower (even) byte, the low order address held in the upper (odd) byte, forming the address which is loaded into the Program Counter when selected by the interrupt vector provided by the interrupt source. This should point to the relevant Interrupt Service routine provided by the user for immediate response to the interrupt.

Data Space

The ST902X addresses the 256 bytes of on-chip RAM memory in the Data Space from addresses 0 to 255 (0FFh). It may also address up to 65,280 locations of External Data through the External Memory Interface when decoded with the P/$\overline{D}$ pin. The on-chip general purpose Registers may be used as additional RAM memory for minimum chip count systems.

The Data Space is selected by the execution of the SDM instruction. All subsequent memory references will access the Data Space. Data may also be stored in external RAM or ROM memory within the Program Space.

Figure 6. ST902X Program and Data Spaces



MEMORY (Continued)

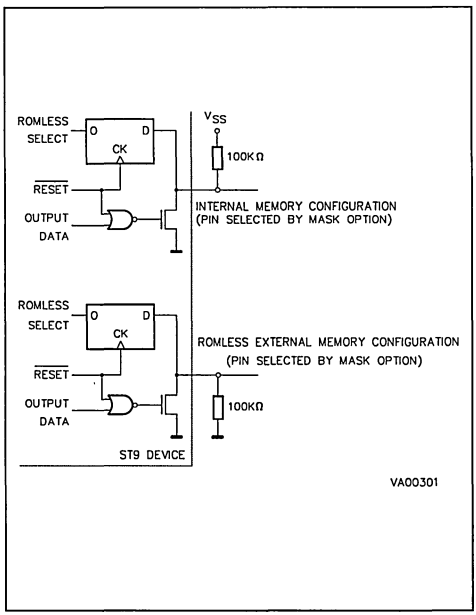
ROMless Option

In the event of a program revision being required after the development of a ROM-based ST902X, a mask option is available which enables the reconfiguration of the memory spaces to give a fully ROMless device. This means that the on-chip program ROM is disabled and ALL program memory is seen as external, allowing the use of replacement program code in external ROM memory. The on-chip memory in Data space is not affected.

To give the ROMless function (when enabled by the MASK option), the pin selected by mask for ROMless as an Alternate Function should be held to ground (V_{SS}) with a high resistance (eg 100k ohm) during the RESET cycle. The pin status is latched on the rising edge of the $\overline{RESET}$ input. After this time, the pin is free for normal operation.

If the ROMless option is enabled, and the on-chip program is to be used, the pin enabled for the ROMless function must to held to a high potential during the $\overline{RESET}$ cycle (eg with a 100k ohm resistor to V_{DD}).

Figure 7. ROMless Selection

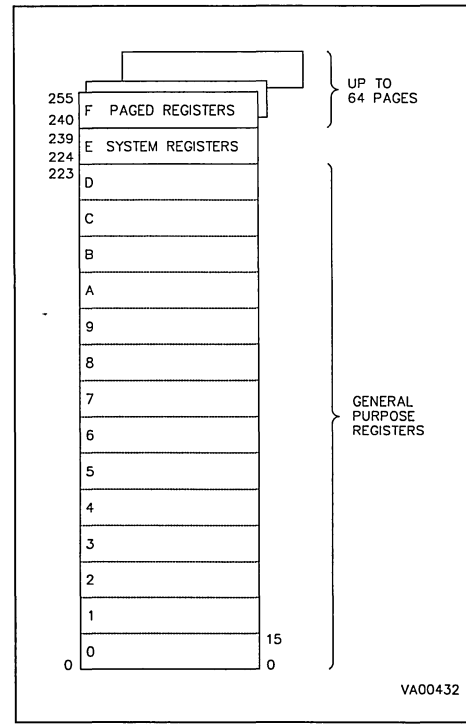


REGISTERS

The ST902X register file consists of 240 registers (224 general purpose) plus pages of 16 registers supporting the configuration and control registers for the on-chip peripherals. The 224 general purpose registers all have 8 and 16 bit arithmetic capability and may be used as accumulators, on-chip RAM, internal Stack areas (for system and/or user stacks), or, with the appropriate addressing modes, as index, offset or stack pointers.

The register file is arranged into 16 groups of 16 registers, where the general purpose registers occupy the first 14 groups. The 15th group, E, contains the system registers and Group F contains the pages of the on-chip peripheral control registers.

Figure 8. Register Grouping



REGISTERS (Continued)

Group F is paged in this manner due to the modularity of the ST9 family of microcontrollers. Each member of the family retains all general purpose and system registers, only the paged register groups changing owing to the different on-chip peripheral organizations of each device. The user can therefore generate code libraries which use the general purpose registers knowing that they will not be lost on future ST9 devices. To address a paged register, the Page Pointer (PPR, R234) within the system register group must be loaded with the relevant page number using the SPP instruction. Subsequently any access to registers in the top group (R240-R255) will refer to the selected page. This remains set until the next change to the Page Pointer register (by the SPP instruction).

The System group (Group E, registers RE0 to REF) includes the system and user stack pointers, the Mode register, the ALU FLAG register and the Page pointer register. In addition the data registers for the first 5 I/O ports are present, the configuration registers for the ports being in the paged area. This allows the immediate access to these I/O ports at all times.

Figure 9. Page Pointer Mechanism

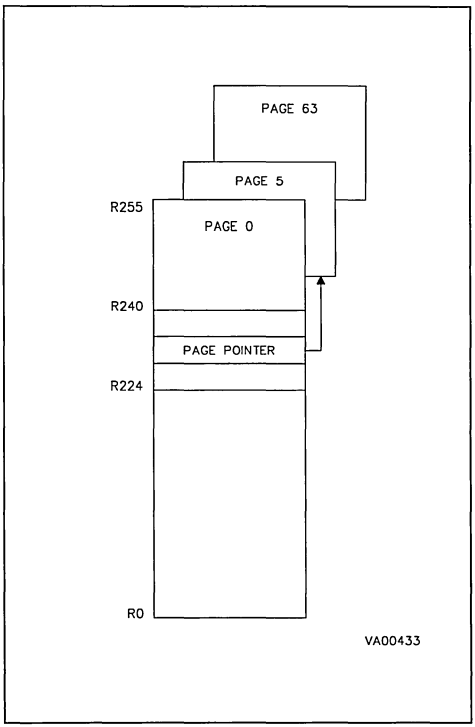
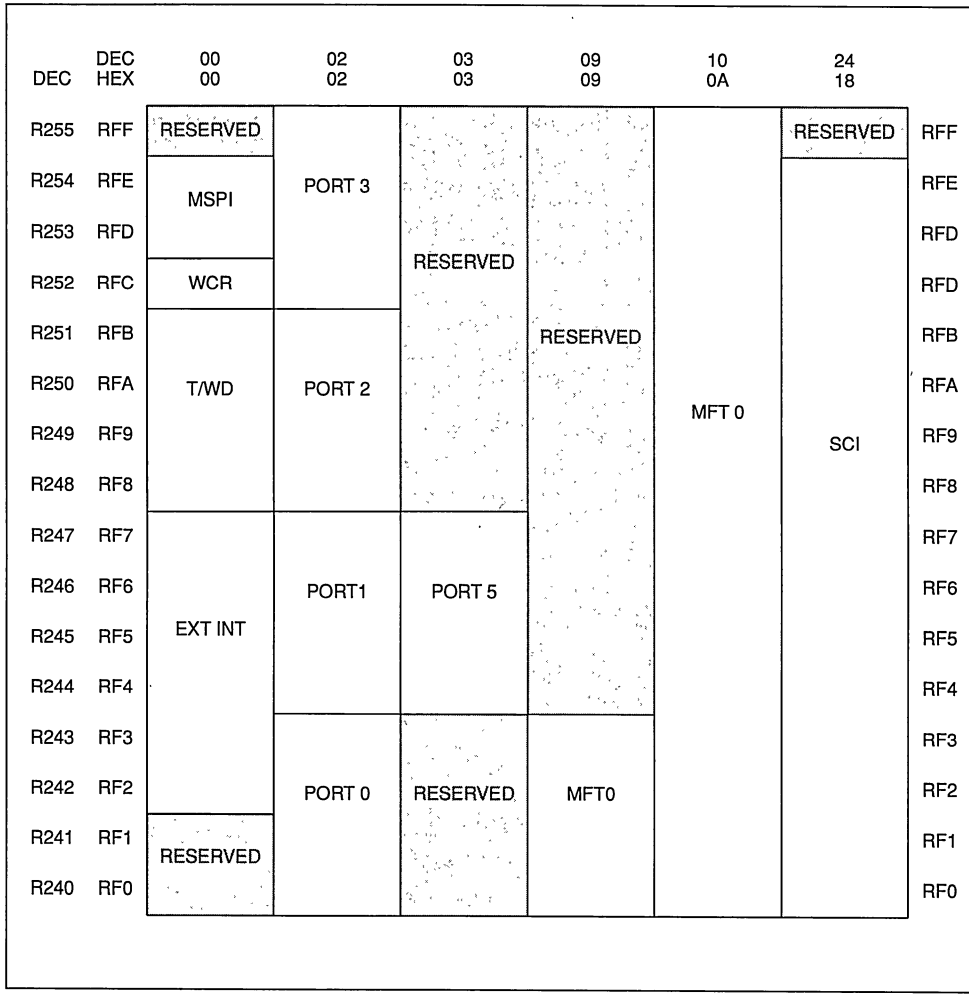


Figure 10. Group E Register Map

R239	System Stack Pointer Low (SSPLR)
R238	System Stack Pointer High (SSPHR)
R237	User Stack Pointer Low (USPLR)
R236	User Stack Pointer High (USPHR)
R235	Mode Register (MODER)
R234	Page Pointer (PPR)
R233	Register Pointer 1 (RP1R)
R232	Register Pointer 0 (RP0R)
R231	ALU Flags (FLAGR)
R230	Central Interrupts Control (CICR)
R229	Port 5 Data (P5DR)
R228	Port 4 Data (P4DR)
R227	Port 3 Data (P3DR)
R226	Port 2 Data (P2DR)
R225	Port 1 Data (P1DR)
R224	Port 0 Data (P0DR)

REGISTERS (Continued)

Figure 11. ST9026 Group F Peripheral Organisation



REGISTERS (Continued)

The Register Pointers, present in the system register group, select groups of registers as "Working Registers", which have faster addressing modes than direct Register addressing and allows smaller code size. The Register Pointers may either be used singly, creating a register group of 16 working registers, or as two independent groups of 8 working registers which may be placed at any 8 register boundary within the register file. The single and twin working register modes are automatically set by hardware when the respective SRP and either SRP0 or SRP1 instructions are executed. If working registers are used as accumulators and RAM locations for particular tasks, fast context switching on interrupts may be achieved by setting the register pointer to another group for the Interrupt Service Routine, ISR, (e.g. saving the Register pointer on the stack), using the new group in the ISR and subsequently restoring the original group before the Return from Interrupt instruction. Working registers also allow the use of the ABAR - Any Bit-Any Register Boolean operations (including directly on the I/O port data registers).

In the ST9 syntax, directly addressed Registers are indicated with a capital R e.g. R0, R224, RBF, with Register Pairs (16 bit accumulators or memory pointers) as RR0, RR24. When using Working Registers, groups of 16 registers (SRP instruction) are denoted as r0 to r15 (rr0 to rr14), while the dual working register group are addressed as r0 to r7 (rr0 to rr6), for the first group of 8 registers (SRP0), with r8 to r15 (rr8 to rr15) for the second set (SRP1).

Working register addressing requires a 4 bit field within the instruction. When packed into a byte, the upper nibble is set to Dh (1101b), this being the escape code to indicate the use of the working registers. As a result, group D CANNOT be selected with direct register addressing, it is recommended that this group be used as internal stacking area when using register file based system or user stack pointers.

Figure 12. Single Working Register Bank

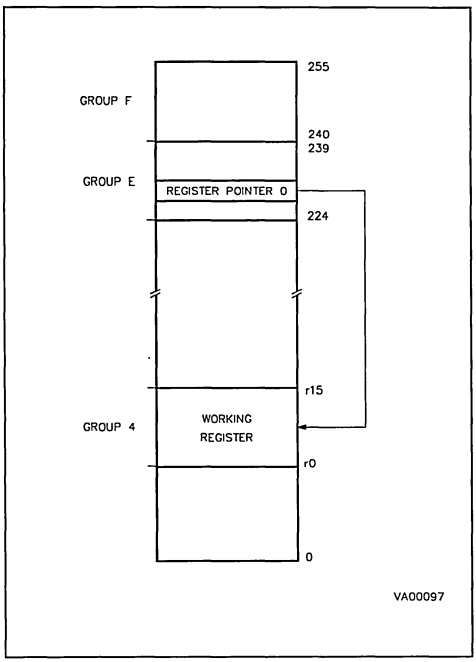
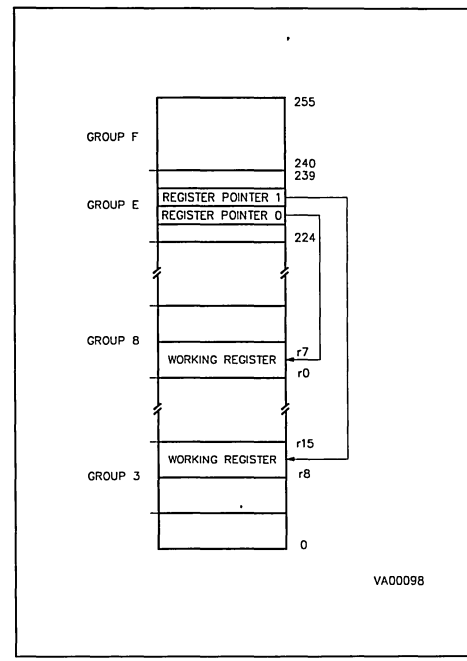


Figure 13. Dual Working Register Bank



STACK POINTERS

There are two separate, double register stack pointers available (System and User), both of which can operate in register or Data memory address spaces. These operate in a Pre-Decrement mode when data is PUSHed onto the Stack and in a Post-Increment mode when data is POPed from the stack.

The SYSTEM Stack Pointer (SSPR, R238:R239) is used for the storage of temporarily suspended system and/or control registers (ie the the Program Counter and FLAG register) while interrupts are being serviced, and is used for the storage of the Program Counter following the CALLing of a subroutine.

The USER Stack Pointer (USPR, R236:R237) is completely free from all interference from automatic operations and so provides for a totally user controlled stack area.

Both Stack pointers may operate with both byte (PUSH,POP) and word (PUSHW,POPW) data, and are differentiated by appending a "U" to the instruction mnemonic for the User Stack (PUSHU/PUSHUW, POPU/POPUW).

When the Stack Pointers are using RAM Memory as the stack areas, a full word register is used as the pointer, while when operating with the stack area within the Register File (Groups 0 to 14 only, but not the within the system and paged groups) only an 8 bit register is required for addressing and consequently only the low byte of the word registers are used (R239 for the System Stack and R237 for the User Stack). In this latter case the upper byte of the stack pointer registers (R238 and R236) must be considered as reserved. The Stack Pointers may be selected to point to RAM or Register file by the setting of the SSP (MODER.7) and USP (MODER.6) of the ST902X configuration register (MODER, R235) where a "1" denotes Register file operation (Default at Reset) and "0" causes external Data space operation.

Figure 14. Internal Stack Pointers

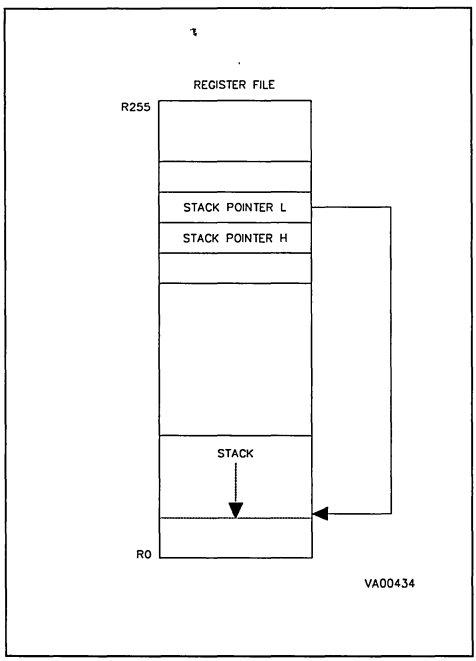
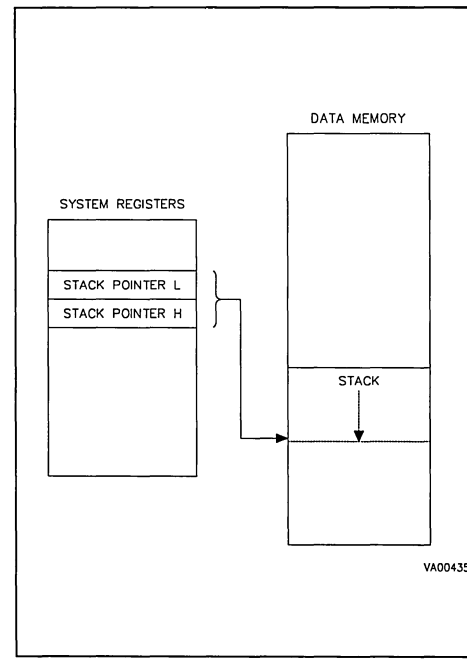


Figure 15. External Stack Pointers



INTERRUPTS

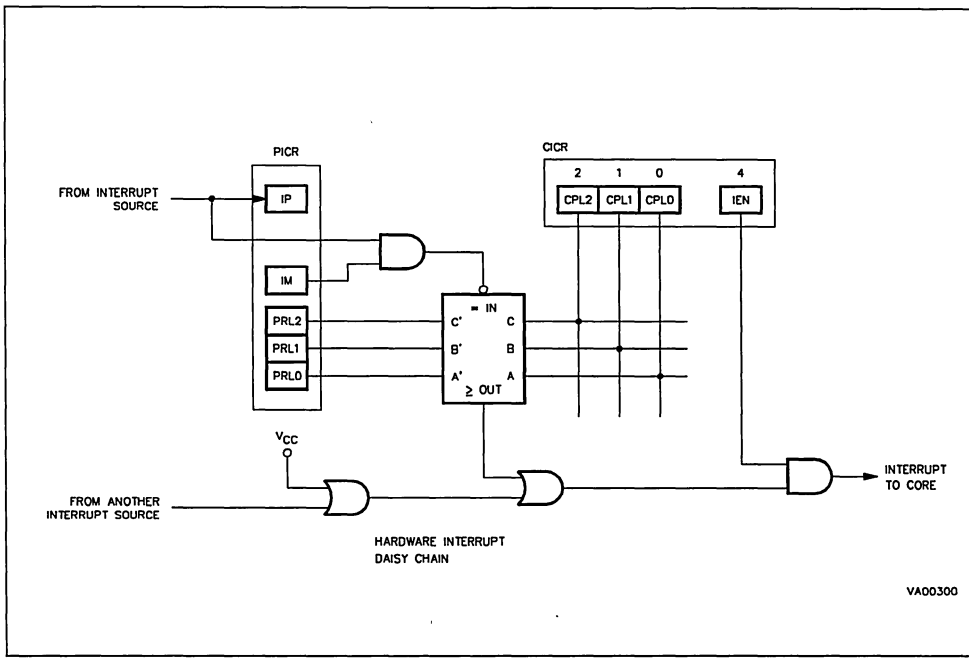
The ST902X offers a powerful solution to the response requirements of real-time systems with its advanced interrupt structure. Interrupt trigger sources can be prioritized within 8 levels to match the priorities assigned to the application. In addition a top-level or non-maskable interrupt is available.

The ST902X interrupts follow the logical flow of Figure 16.

Interrupt events (selectable with each function) cause the setting of the Interrupt Pending (IP) bit within the status register of the peripheral. This bit may also be set by software in order to generate a software interrupt, and should normally be reset by software within the interrupt service routine. If the interrupt is not Masked with the corresponding Interrupt Mask bit, the interrupt is passed to the central interrupt control logic where the priority level assigned by the user to the interrupt source is compared with the priority level of the core (user programmed dynamically in the 3 bits of the Central Priority register (CPL, CICR.0-2, Level 7 is the lowest priority and level 0 the highest). If the incoming priority level is higher than the CPL, and Global Interrupts are enabled (by the `EI` instruction, interrupts are disabled by the execution of the `DI` instruction), the interrupt is acknowledged. If interrupts are globally disabled, the priority level of the source is lower than or equal to the CPL or the Interrupt is masked, then the IP bit remains set and the interrupt is held pending until the `EI` instruction is executed, the CPL is set to a lower level AND the interrupt is un-masked. Alternatively the IP bit of a masked interrupt source may be used in a polled interrupt environment, with the IP bit being reset by software within the service routine.

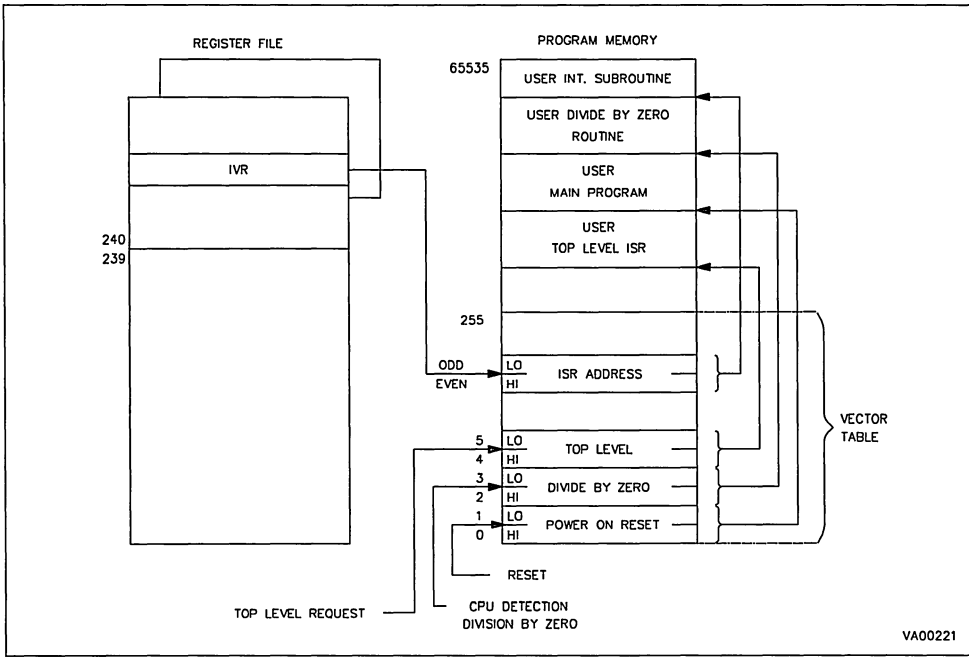
The interrupt acknowledge cycle causes the Program Counter and FLAGS register to be pushed onto the System Stack (PC low byte first, PC high byte, then FLAGS Register) and all maskable interrupts to be disabled by resetting the IEN bit (CICR.4). The peripheral Interrupt Vector, IVR, a user programmable feature of the peripheral interrupt control registers, is used as an offset into the vector table, pointing to the high byte (even address) of the 16 bit address which should contain the starting address of the interrupt service routine. Addresses 0 through 255 of the program space comprise the interrupt vector table. Where multiple

Figure 16. Interrupt Logic



INTERRUPTS (Continued)

Figure 17. Interrupt Vector Table Usage



interrupt sources may occur within a peripheral, the peripheral interrupt vector source may be encoded by hardware set bits within the IVR register. This means that the vector address defined in the peripheral IVR is the base address for a block of vectors servicing that peripheral. The address pointed to by the vector is loaded into the Program Counter and execution restarts from this point.

The interrupt service routine should clear the interrupt pending flag of the interrupt source and take the appropriate action. The last instruction of the interrupt service routine should be the IRET instruction, the action of this is to restore the Program Counter and Flags register to their value prior to the interrupt acknowledgment, and to re-enable interrupts. Within the interrupt service routine, use may be made of the working register pointer mechanism to reduce the context switching time.

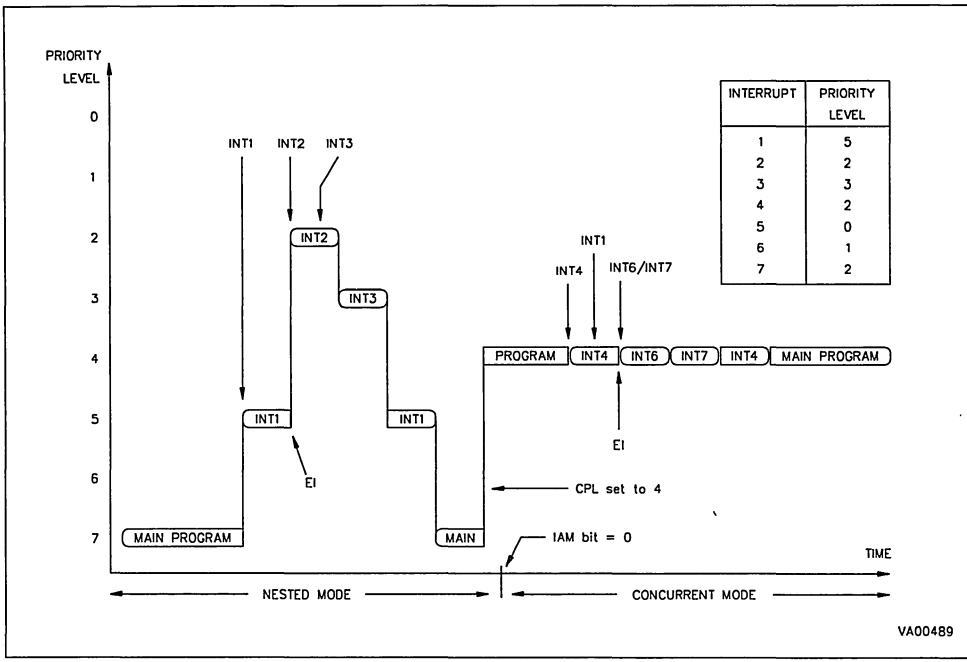
Two interrupt arbitration modes are available for use with the 8 level priority scheme, Nested and Concurrent modes. These are selected by the status of the IAM bit (CICR.3).

Concurrent mode, selected when IAM = "0" (the reset condition) is the standard interrupt arbitration mode, where the arbitration phase of every instruction acknowledges interrupts according to their priority level (if higher than the CPL) and follows the sequence shown. All pending interrupts existing or having eventually occurred during interrupt service routine execution, remain pending until the Enable Interrupt instruction (EI) (even if it is executed during the interrupt service routine). EI within the interrupt service routine is not recommended for use with the Concurrent arbitration mode as this can trigger a Last In, First Out condition where high priority interrupts are masked by lower priority interrupts which are all higher than the CPL value.

Nested mode, selected when IAM = "1", uses the same arbitration phase as concurrent mode, the difference being that the CPL is modified during the interrupt processing cycle to that of the acknowledged interrupt level. The CPL value is pushed by hardware into the Nested Interrupt Control register (NICR, R247 page 0) by setting the NICR bit corresponding to the CPL value. The interrupt service

INTERRUPTS (Continued)

Figure 18. Interrupt Modes Example of Usage



routine is entered in the normal manner. The revised CPL level is used for arbitration of further interrupts, each higher level being saved on the NICR stack, and being restored automatically by hardware with the IRET instruction. This allows the execution of the EI instruction within the interrupt service routine to operate the correct nesting of interrupts. The two modes are shown graphically in Figure 18, where the Y axis shows the CPL value. It should be noted that in the example INT1 will not be acknowledged until the CPL level is programmed to a lower level.

Interrupts coming from on-chip sources at the same instant, and at the same priority level, are resolved during the arbitration phase according to a hardware daisy-chain. This follows the priorities of the table shown in Table 2.

Table 2. ST902X Interrupt Hardware Daisy Chain

INTA	High Priority
INTB	
INTC	
INTD	
MFTIMER0	
SCI	Lowest Priority

INTERRUPTS (Continued)

External Interrupts. Up to 7 external interrupts are available on the ST902X as alternate function inputs of I/O pins. These may be selected to be triggered on rising or falling edges and can be independently masked. The eight external interrupt sources are grouped into four pairs or channels which can be assigned to independent interrupt priority levels. Within each channel the even interrupt number takes the even priority level and the odd channel the odd priority level (even+1).

Table 3. External Interrupt Channel Grouping

External Interrupt	Channel
INT7 INT6	INTD1 INTD0
INT5 INT4	INTC1 INTC0
INT3 INT2	INTB1 INTB0
INT1 INT0	INTA1 INTA0

Several of the External Interrupt channels have their inputs selectable between the external interrupt source and on-chip peripheral sources.

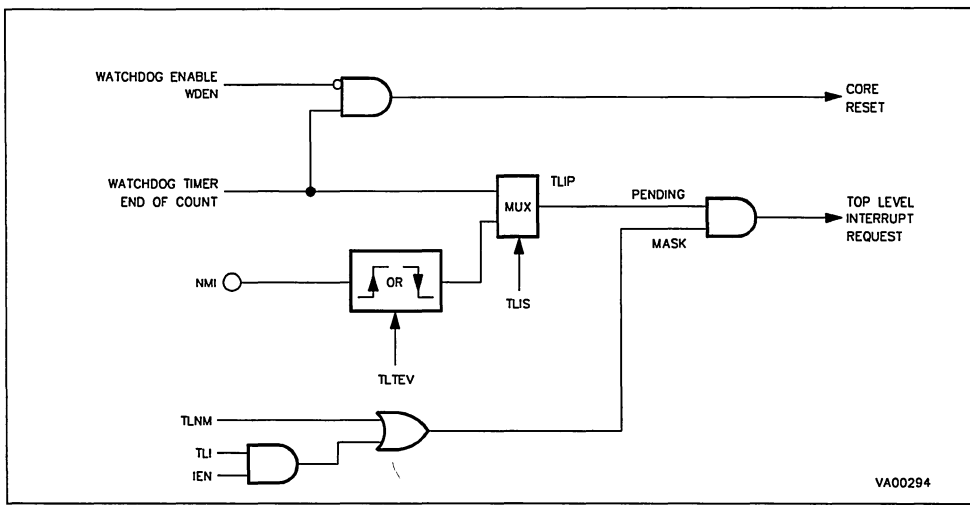
Table 4. ST902X External Interrupt Souce Selection

INT0	INTA0
Timer/Watchdog End of Count	
INT2	INTB0
SPI Interrupt	

Top Level Interrupt. The Top Level Interrupt channel can be assigned either to the external NMI pin or to the Timer/Watchdog output. When selected as the external NMI pin, the active edge may be programmed to be rising or falling. The TLI event will cause the setting of the TLIP bit (CICR.6) and according to the mask situation, a Top Level Interrupt request may be generated. Two masking conditions are available, a Maskable Mask and a Not-Maskable Mask.

The Maskable Top Level Interrupt may be enabled or disabled by software and follows the state of the Global Interrupt Enable bit IEN (CICR.4), while the Not-Maskable Mask bit (TLI, CICR.5) is a set-only mask. Once set, the Top Level Interrupt is active independently of IEN and cannot be disabled until the next Reset cycle.

Figure 19. Top-Level Interrupt Structure



DMA

The ST902X has on-chip DMA channels to provide high-speed data transaction between peripherals and Memory or Register File. Multi-channel DMA is fully supported because each peripheral can have its own DMA channel(s). Each DMA channel transfers data to/from contiguous locations of the Register File, Program Memory or Data Memory. The maximum number of transactions that each DMA channel can perform is 222 if the Register File is selected and 65536 if Program or Data Memory are selected.

DMA transfer to (or from) the Register File takes 8 INTCLK cycles, DMA transfer to (or from) Memory takes 16 INTCLK cycles. If the ST902X is in the idle mode (following the execution of the `WFI` instruction), DMA requests are acknowledged according to their priority and control is returned to the idle mode pending an interrupt, this operation increases the number of INTCLK cycles by 2 for both Register File and Memory DMA transactions.

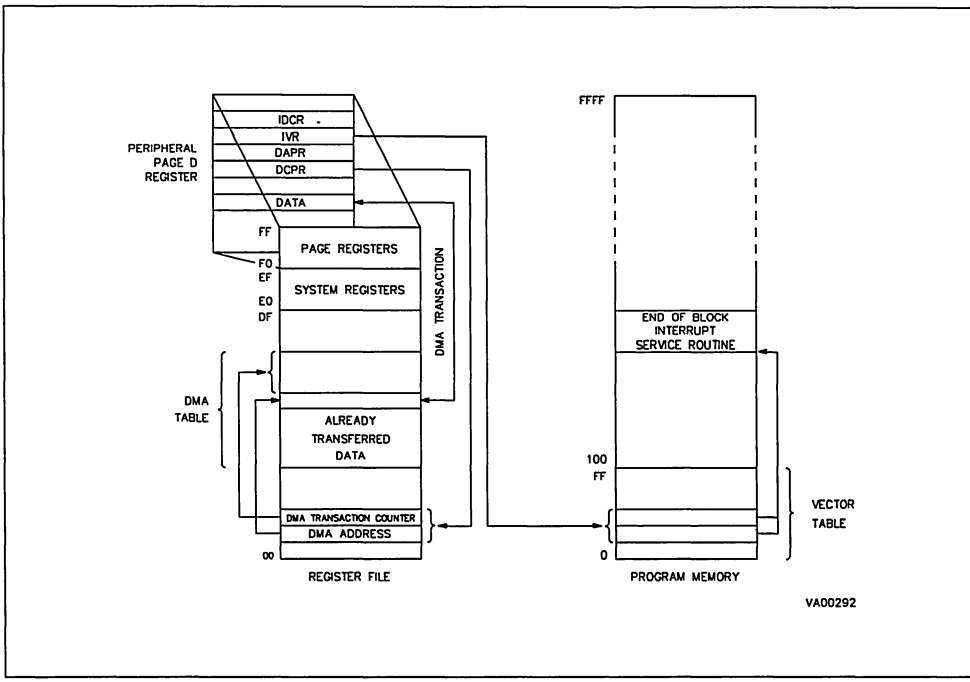
Each DMA channel has its own control registers located in the page(s) related to the peripheral.

There are two pointer registers, DAPR which points to a register or register pair containing the current DMA address to/from which data will be transferred, and DCPR, which points to a register or register pair which contain the transaction counter for the DMA operations. Each DMA transfer consists of three operations:

- A load from/to the peripheral data register to/from a location of Register File (or Memory) addressed through the DMA Address Register (or Register Pair)
- A post-increment of the DMA Address Register (or Register Pair)
- A post-decrement of the DMA transaction counter, which contains the number of transactions that have still to be performed.

When the transaction counter reaches 0 (all data has been transferred) an End of Block Interrupt event is generated to allow the processing of the DMA data block, or, by reloading the Address and counter registers and retriggering, a repeated DMA cycle.

Figure 20. DMA Between Registers and Peripheral

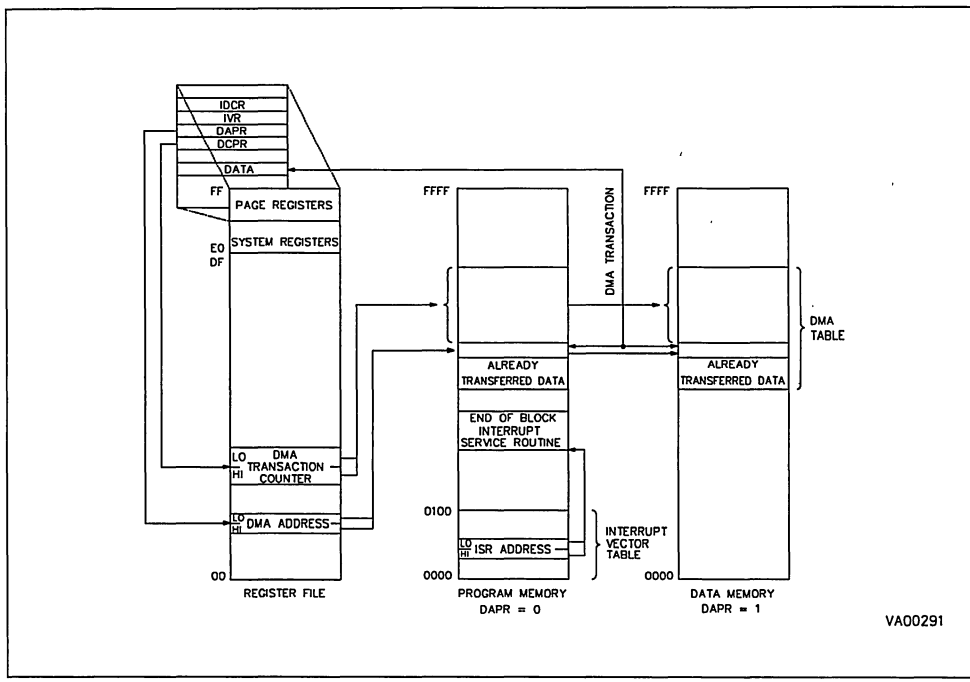


DMA (Continued)

A SWAP mode, allowing continuous DMA operation, is available for the Multifunction Timer and is described in the section relating to the Multifunction Timer.

The ST902X has DMA channels associated with the Serial Communications Interface Input and Output Serial data channels, the 16 bit Load/Capture Register 0, CAPT0R, of the Multifunction Timer allowing the timing of external signals to be captured into a table for off-line analysis or for the automatic output of PWM signals of variable width and timing, and the 16 bit Comparison Register 0, COMP0R, of the Multifunction Timer which can be programmed to cause output or input of parallel data through the handshake port 5 under DMA.

Figure 21. DMA Between Memory and Peripheral



CLOCK GENERATION, WAIT, HALT AND RESET

Clock Generation

The ST902X Clock Generator module generates the internal clock for the ST9 core and the on-chip peripherals, it may be driven by an external quartz crystal circuit, connected to the OSCIN and OSCOUT pins, or by an external pulse generator connected to OSCIN (Figure 22, Figure 23).

The conceptual schematic of the ST9 internal clock circuit is shown in Figure 24.

The maximum external frequency of the ST9 is 24 MHz, while the maximum internal operating frequency is 12 MHz, thus a programmable divide by two circuit is present, this allows the use of high frequency crystals for economy, or low frequency crystals for reduction in radiated noise. This divider is active upon exit from the reset condition, the user may bypass the divide by two circuit by setting the DIV2 bit (MODER.5). The resulting clock from this section is named INTCLK, the internal clock which drives the timebases of the on-chip clock for the ST902X peripherals (eg the Multifunction Timer, Timer/Watchdog, Serial Communications Interface) and also the input of the CPU prescaler

Figure 22. Crystal Oscillator

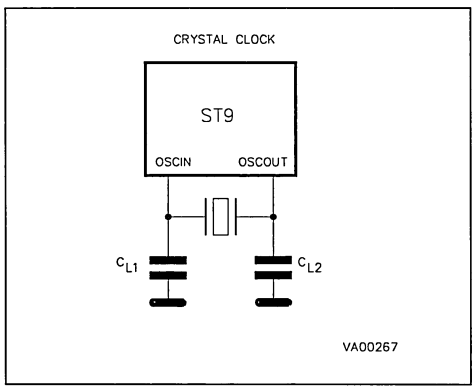


Figure 23. External Oscillator

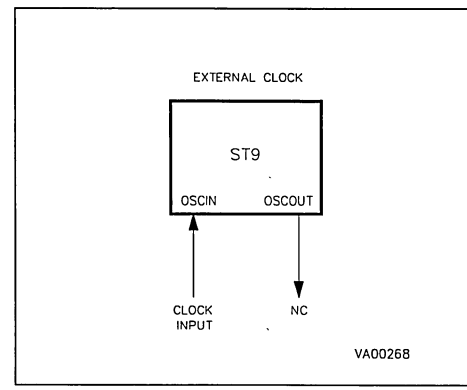
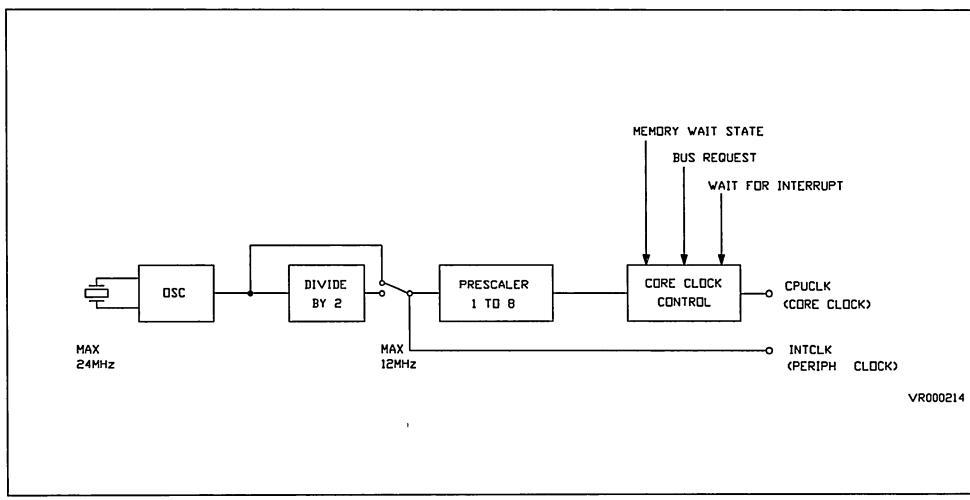


Figure 24. Internal Clock Circuit



CLOCK GENERATION, WAIT, HALT AND RESET (Continued)

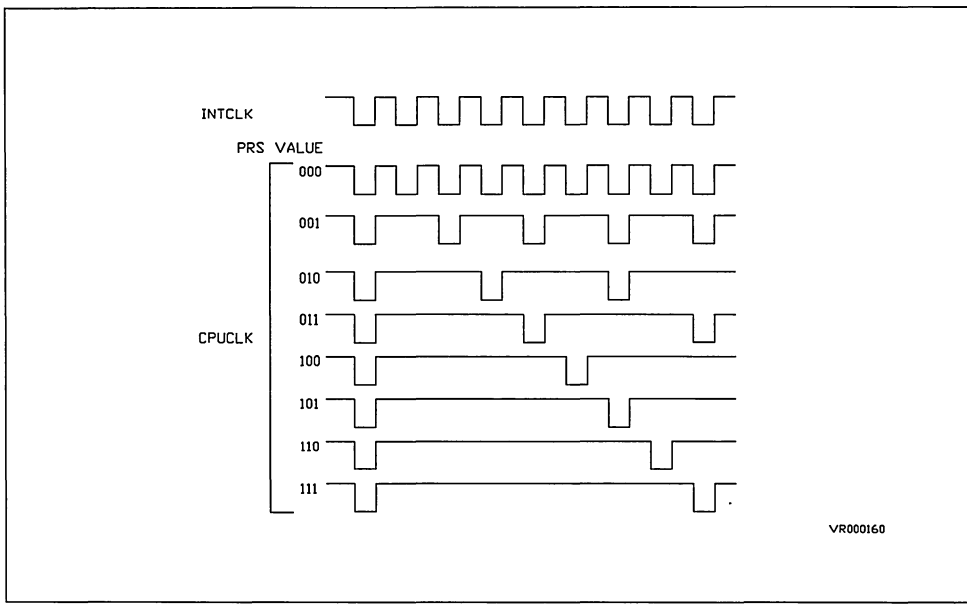
section. The CPU of the ST9 includes the instruction execution logic and may run at different rates according to the setting of the PRS2,PRS1 and PRS0 bits (MODER.4-2) (Figure 25). The resulting clock is named CPUCLK and it should be noted that this does not maintain a 50% duty cycle, but stretches the high level of the clock until completion. The CPUCLK prescaler allows the user to slow down the program execution time (eg for lower power consumption), while time-critical sections of the program may tune the CPUCLK execution speed to high speed and then restore it to its original speed.

Wait States

The output from the prescaler can also be affected by wait states. Wait states from two sources allow the user to tailor timing for slow external memories or peripherals.

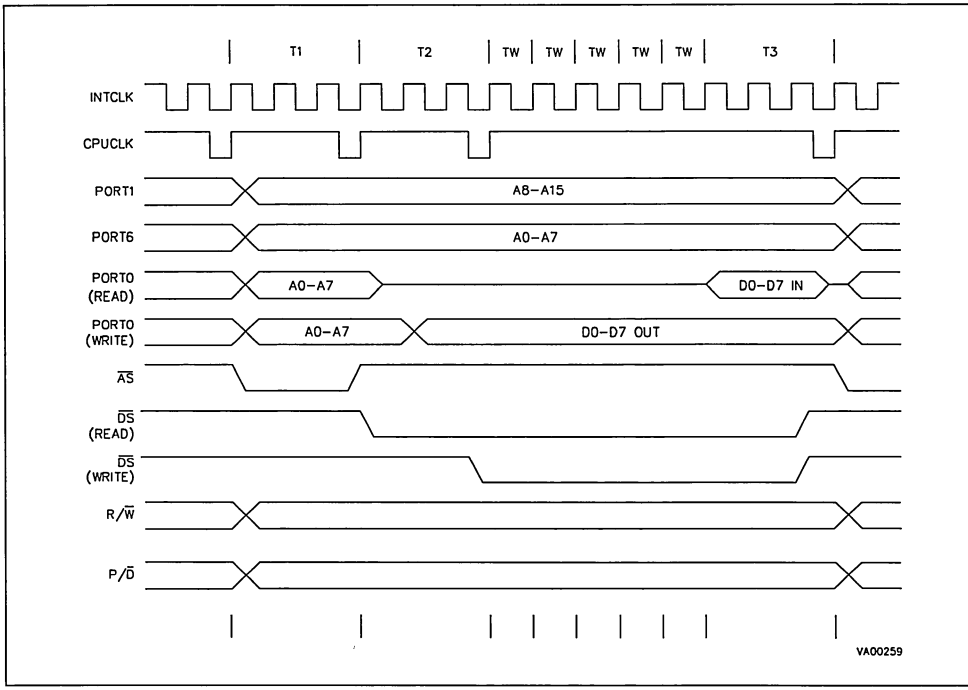
The internal Wait State generator will insert from 0 to 7 wait states, independently programmable for both Program and Data Spaces, via the Wait Control Register WCR (R252, page 0). The second source of wait states is the external Wait input pin when enabled as the Alternate Function. Figure 26 shows the External Memory Interface timing as it relates to CPUCLK prescaling of 2 and 5 added wait states. The added wait states are derived from the INTCLK clock cycle, not CPUCLK. Internal memory is always accessed with no Wait states.

Figure 25. CPUCLK Prescaler



CLOCK GENERATION, WAIT, HALT AND RESET (Continued)

Figure 26. External Memory Interface Timing with CPUCLK Prescaling and 5 Added Wait States

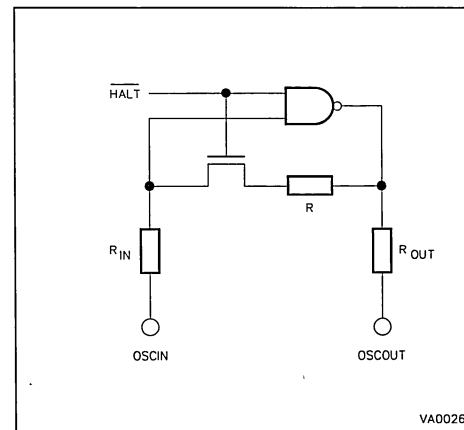


Halt and Wait for Interrupt (WFI) States

The schematic of the on-chip oscillator circuit is shown in figure 27. The HALT condition, caused by the execution of the HALT instruction, disables the oscillator, forcing OSCOUT high. This places the ST902X into the lowest power mode. The exit of the HALT condition and the restarting of the oscillator requires a RESET pulse with a minimum duration of 10ms (figure 28). It must be noted that if the TIMER/WATCHDOG has the WATCHDOG mode enabled, a HALT instruction will not disable the oscillator; this is to avoid stopping the Watchdog if, by an error, a HALT instruction is executed. If this occurs, the ST902X runs in an endless loop terminated only by the Watchdog reset (or hardware reset).

The WFI (Wait for Interrupt) instruction suspends program execution until an interrupt request is acknowledged. During this period, DMA transactions are allowed if their priority is higher than or equal to the CPL level; the ST902X returns to WFI

Figure 27. Oscillator Schematic



CLOCK GENERATION, WAIT, HALT AND RESET (Continued)

mode after completion of the DMA transfer. The CPUCLK is halted during Wait For Interrupt while INTCLK continues to run, thus the power consumption of the processor is lowered by the CORE power consumption value.

The External Memory Interface lines status during HALT and WFI modes is shown in Table 5.

Table 5. External Memory Interface Line Status During WFI and Halt

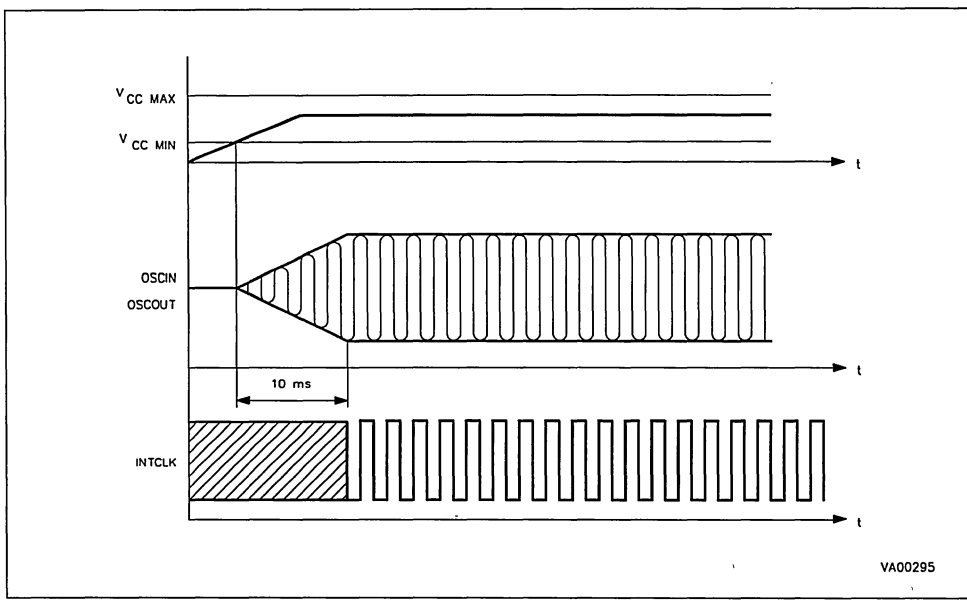
P0 (AD0-AD7)	High Impedance
P1 (A8-A15)	Forced to Address of Next Opcode
$\overline{AS}$	Forced High
$\overline{DS}$	Forced High
R/$\overline{W}$	Forced High

Reset

The processor Reset overrides all other conditions and forces the ST902X to the reset state. During Reset, the internal registers are set to their Reset values, as shown in Table 6 for the system and Page 0 Registers. The I/O Ports pins are set to the Bidirectional Weak Pull-up mode. The user must then initialize the ST902X registers to give the required functions.

The Reset condition can be generated from the external $\overline{RESET}$ pin or by the on-chip TIMER/WATCHDOG operating in Watchdog mode. To guarantee the complete reset of the ST902X, the $\overline{RESET}$ input pin must be held low for at minimum of 53 crystal periods in addition to the crystal start-up period. The Watchdog RESET will occur if the Watchdog mode is enabled (WDEN, WCR.6, is reset) and if the programmed period has elapsed without the code 0AAh,55h written to the appropriate register. The input pin $\overline{RESET}$ is not driven low by the on-chip reset generated by the TIMER/WATCHDOG.

Figure 28. Reset Timing Requirements from Halt State



CLOCK GENERATION, WAIT, HALT AND RESET (Continued)

Table 6. System and Page 0 Reset Values

Register Number	System Register Reset Value	Page 0 Register Reset Value
F	(SSPLR) = undefined	Reserved
E	(SSPHR) = undefined	(SPICR) = 00h
D	(USPLR) = undefined	(SPIDR) = undefined
C	(USPHR) = undefined	(WCR) = 7Fh
B	(MODER) = E0h	(WDTCR) = 12h
A	(Page Ptr) = undefined	(WDTPR) = undefined
9	(Reg Ptr 1) = undefined	(WDTLR) = undefined
8	(Reg Ptr 0) = undefined	(WDTHR) = undefined
7	(FLAGR) = undefined	(NICR) = 00h
6	(CICR) = 87h	(EIVR) = x2h
5	(PORT5) = FFh	(EIPLR) = FFh
4	Reserved	(EIMR) = 00h
3	(PORT3) = FFh	(EIPR) = 00h
2	(PORT2) = FFh	(EITR) = 00h
1	(PORT1) = FFh	Reserved
0	(PORT 0) = FFh	Reserved

During the RESET state, $\overline{DS}$ is held low and $\overline{AS}$ is toggled with the frequency of the crystal (OSCIN) divided by 32. This condition may be recognized by external peripherals as a Reset condition. It may also be used to enable the synchronization of multiple ST902X running from the same clock in a multi-processing or high security majority voting system.

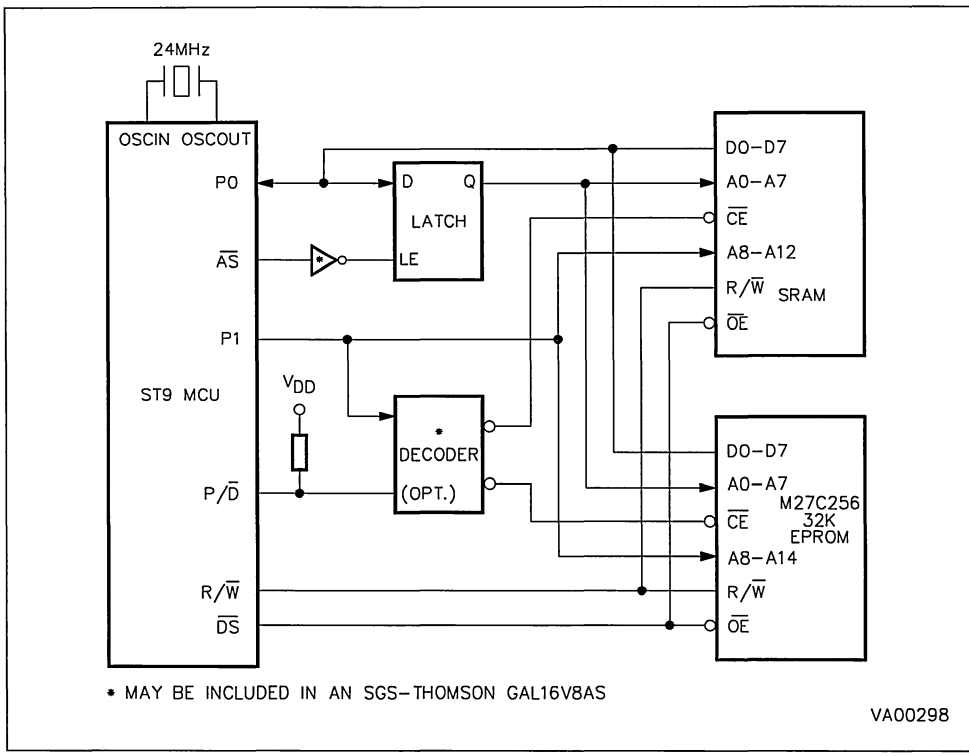
Once the Reset pin reaches a logical high, the ST902X fetches the starting address from locations 0 and 1 of the program space and begins program execution from this address after 67 crystal cycles.

INTERFACING TO EXTERNAL MEMORY

External Memory and/or peripherals may be connected to the ST902X through its External memory interface. This provides the multiplexed Address bits A0 to A7 and Data bits D0 to D7 as Alternative Functions of Port 0, and the higher order address bits A8 to A15 as Alternative Functions of Port 1, giving the full 64K bytes addressing capability. The Program/Data (P/$\overline{D}$) output, when selected as an Alternate function, allows external decoding to provide for the two independent pages of 64K bytes for Program and Data.

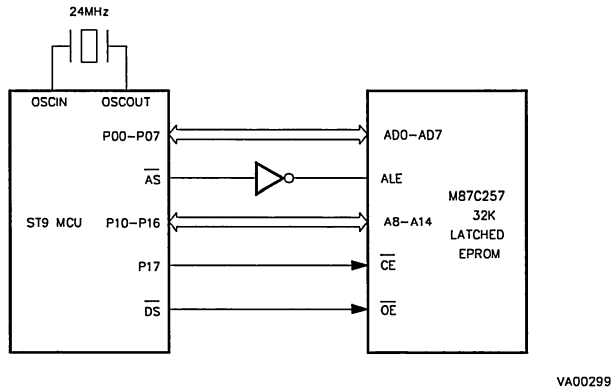
Data transfer timing is generated by the Address strobe $\overline{AS}$ and the data strobe $\overline{DS}$. Address strobe low indicates that the data present on AD0 to AD7 is the low order address and is guaranteed valid on the rising edge of $\overline{AS}$ allowing for latching of the address bits by an external latch. Data transfer direction is indicated by the status of the Read/Write (R/$\overline{W}$) pin; for write cycles (R/$\overline{W}$ low), data out is valid at the falling edge of $\overline{DS}$; for read cycles (R/$\overline{W}$ high), data in must be valid prior to the rising edge of $\overline{DS}$. The Data Strobe low period may be extended to accomodate slow external devices by the adding of internally generated wait cycles (0 to 7 cycles for program and/or data memory maps) or by an external input on the WAIT input pin also available as an Alternative Function of an I/O bit. Suggested interface circuits are shown in Figure 20 and Figure 30.

Figure 29. External Memory Addressing Circuit



INTERFACING TO EXTERNAL MEMORY (Continued)

Figure 30. External Memory Addressing Circuit



BUS CONTROL

Multi-processing or external program testing may be accomplished by disabling the I/O ports used for external memory addressing and the associated timing signals.

High Impedance Mode

The user may place the External Memory Interface (I/O ports 0 and 1, Address Strobe, Data Strobe and Read/Write) into the high impedance state by setting the HIMP bit (MODER.0). External test equipment may then drive the memory lines for automatic test, external memory validation or programming. The ST9 will continue to execute internal programs, providing no external memory is addressed, allowing the execution of security routines without showing externally the addresses used.

Bus Request/Acknowledge

The External Memory Interface address ports and timing signals may be forced to their high impedance state by utilizing the $\overline{\text{BUSREQ}}$, Bus Request, and $\overline{\text{BUSACK}}$, Bus Acknowledge, signals available as Alternate Functions of two I/O pins (please refer to the pin configuration drawings for availability of these lines for the package chosen). The signals, $\overline{\text{BUSREQ}}$ and $\overline{\text{BUSACK}}$, must be enabled by setting the BRQEN bit (MODER.1). Once enabled, a low level detected on the $\overline{\text{BUSREQ}}$ pin at the start of an internal machine cycle will cause the stretching of the CPUCLK, and $\overline{\text{BUSACK}}$ to go low indicating that the External Memory Interface is disabled. The $\overline{\text{BUSREQ}}$ pin is then continuously monitored, and when sampled high, the External Memory Interface pins are driven by the ST9 within two INTCLK cycles.

I/O PORTS

Summary of Function

For each package type of the ST902X, only eight pins have a Reserved function: V_{DD}, V_{SS}, $\overline{RESET}$, $\overline{AS}$, $\overline{DS}$, R/$\overline{W}$, OSCIN, OSCOUT. All other pins are available as Input/Output (I/O) for the user, grouped into Ports of 8 bits. These may be programmed to be Input, Output, Bidirectional or Alternate Function (Peripheral or Memory Interface), on a bit by bit basis, at any time. When programmed as an Input the pin may be set to TTL or CMOS input threshold levels, while, when programmed as Output, Push-Pull or Open Drain configuration may be selected. The Bidirectional mode sets the pin with a weak pull-up resistor to V_{DD} or to Open Drain, allowing bidirectional communication with external logic. The Alternate Function setting is predetermined for each pin as shown in the Pin Configuration Table.

The circuitry of the I/O port allows for several ST902X peripheral functions to address, as Alternate Functions, the same pin, for both input and output, the user selects which peripheral function is to be active by enabling its individual Input or Output function. This multi-function I/O capability of the ST902X allows for easy adaptation to external circuits. The options available for each bit are summarized in Table 8

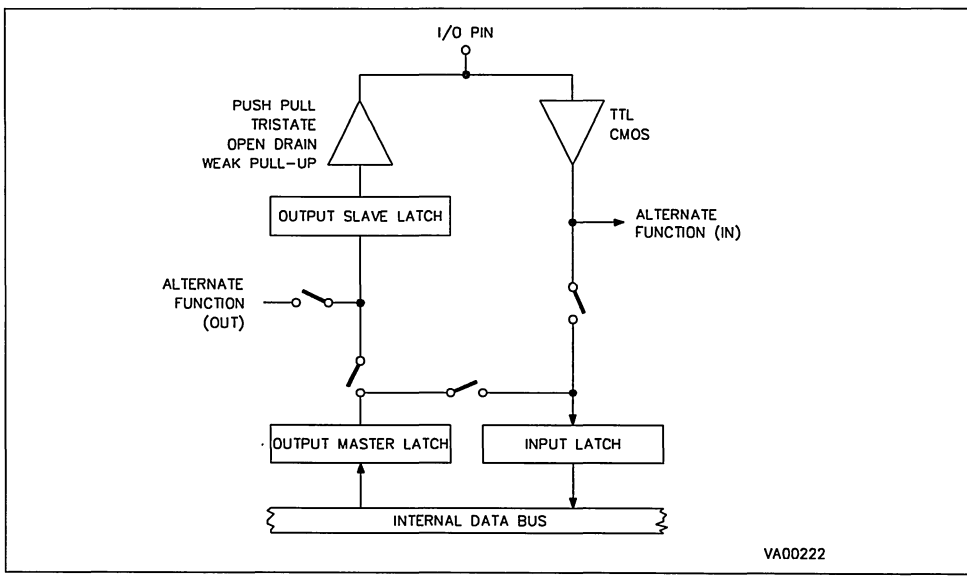
Table 7. I/O Setting Options

Input	TTL Thresholds
	CMOS Thresholds
Output	Open Drain
	Push Pull
Bidirectional	Open Drain
	Weak Pull-up
Alternate Function	Open Drain
	Push Pull

I/O Port Configuration

The configuration of each general I/O bit of the ST902X is set by the corresponding bits in three I/O Port control registers. These affect the status of the input and output buffers of the pin, and enable the Alternate function Outputs. Alternate Function inputs are always connected, and are used by enabling the function from within the configuration registers of the relevant peripheral function. The configuration of an I/O bit is shown in Figure 31. Outputs follow a Master/Slave buffer, data is transferred from the ST9 internal data bus at the beginning of the machine cycle, and, if enabled as

Figure 31. I/O Port Schematic



I/O PORTS (Continued)

output, is passed to the output latch at the end of the cycle. This synchronization allows for the Bidirectional use of the pin without potential conflicts.

Configuration Registers. Three registers are used to allow the setting of each pin, generically PxC2R, PxC1R, PxC0R, where x relates to the 8 bit I/O port in which the bit is present. The setting of the corresponding bit in each register to achieve the desired functionality of the I/O pin is shown in Table 8.

The effect of the configuration settings of Table 8 on the I/O ports structure is shown in Figures 32 to 35.

Table 8. Port Configuration Status Bits

PxC2n	0	1	0	1	0	1	0	1
PxC1n	0	0	1	1	0	0	1	1
PxC0n	0	0	0	0	1	1	1	1
Pxn Configuration	BID	BID	OUT	OUT	IN	IN	AF	AF
Pxn Output	WP	OD	PP	OD	HI	HI	PP	OD
Pxn Input	TTL	TTL	TTL	TTL	CMOS	TTL	TTL	TTL

Legend :
x = Port
n = Bit
BID = Bidirectional
OUT = Output
IN = Input
AF = Alternate Function
WP = Weak Pull-up
OD = Open Drain
PP = Push Pull
HI = High Impedance

Figure 32. I/O Port Input Configuration

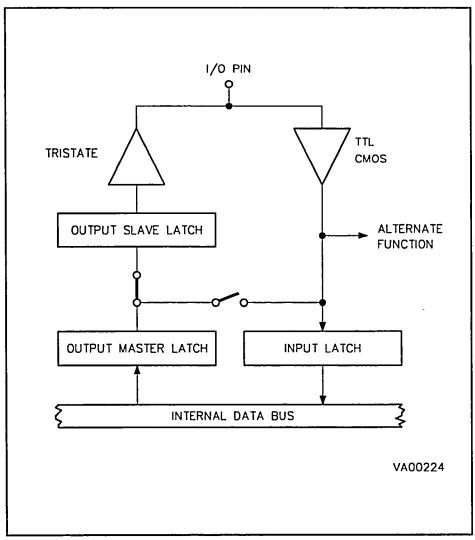
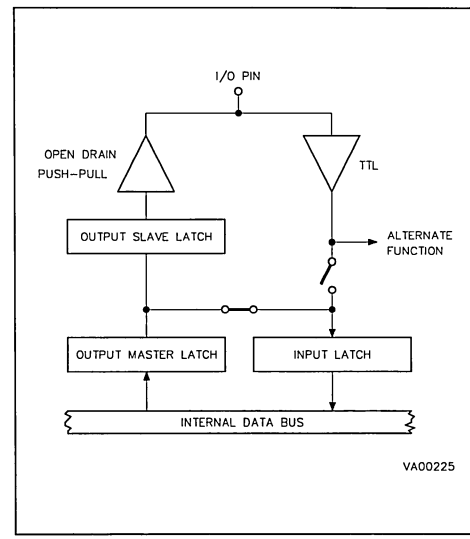


Figure 33. I/O Port Output Configuration



I/O PORTS (Continued)

Figure 34. I/O Port Bidirectional Configuration

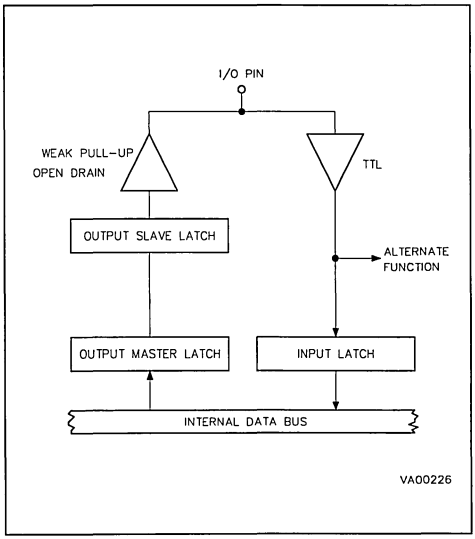
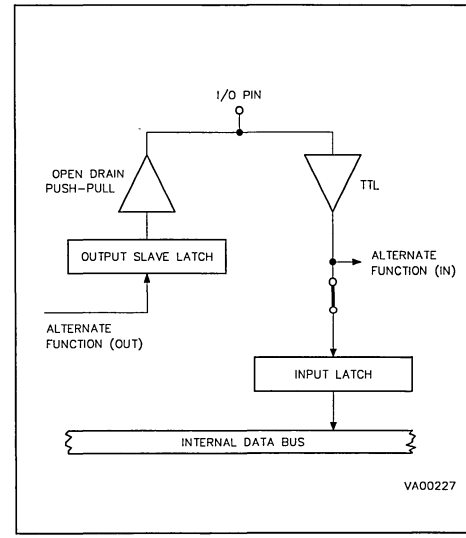


Figure 35. I/O Port Alternate Function Config.



I/O Register Map

The Data Registers which correspond to the pin status (after configuration) of I/O port 0 to 5, are found in Group E of the Register File, for immediate access at all times, while the configuration registers and the Data Registers for Additional Ports are found within I/O pages (Group F) 2 and 3.

Figure 36. I/O Register Maps

GROUP E			GROUP F		PAGE	
DEC	HEX		DEC	HEX	02	03
			R255	RFF	RESERVED	RESERVED
			R254	RFE	P3C2	RESERVED
			R253	RFD	P3C1	RESERVED
			R252	RFC	P3C0	RESERVED
			R251	RFB	RESERVED	RESERVED
			R250	RFA	P2C2	RESERVED
			R249	RF9	P2C1	RESERVED
			R248	RF8	P2C0	RESERVED
			R247	RF7	RESERVED	HDC5
			R246	RF6	P1C2	P5C2
R229	RE5	P5D	R245	RF5	P1C1	P5C1
R228	RE4	RESERVED	R244	RF4	P1C0	P5C0
R227	RE3	P3D	R243	RF3	RESERVED	RESERVED
R226	RE2	P2D	R242	RF2	P0C2	RESERVED
R225	RE1	P1D	R241	RF1	P0C1	RESERVED
R224	RE0	P0D	R240	RF0	P0C0	RESERVED

I/O PORTS (Continued)

Handshake and DMA

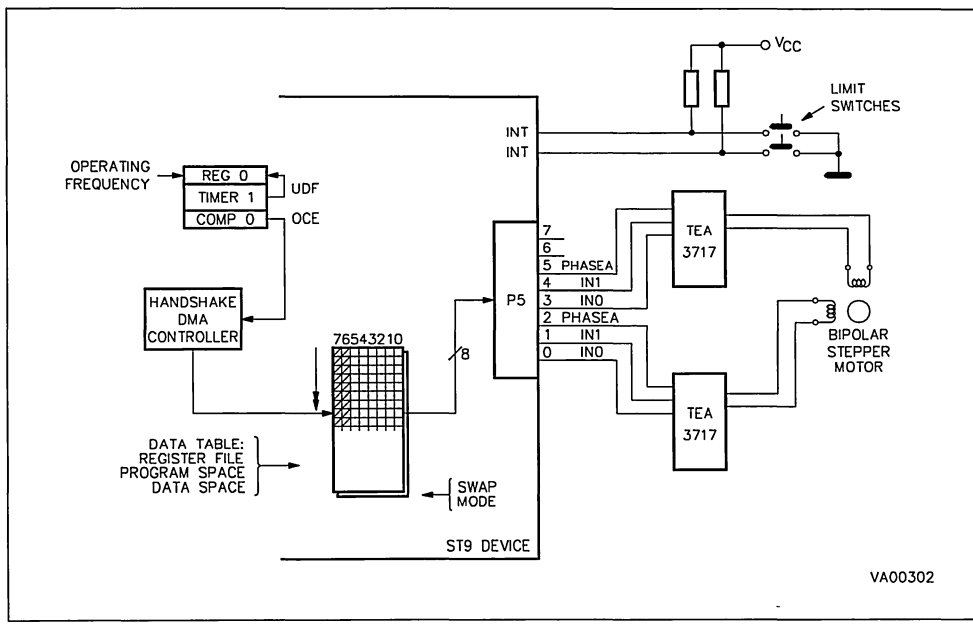
I/O Port 5 of the ST902X (please refer to the pin configuration table for the availability of all 8 bits of Port 5, as this is dependent on the package type) is able to support a parallel interface port with handshake capability. This allows one, two or four wire interconnecting handshake signals and facilitates very fast parallel transfer of data for input and output, or for the interconnection of peripheral devices requiring strobe signals for synchronization. Table 9 shows the available options for input and output status and strobe signals available as Alternate Functions of I/O port bits (see Pin Configuration). The Handshake configuration is set within the Handshake Control Register (HDCnR) for the relevant I/O port n.

Data transfer through the parallel I/O port with handshake can also be triggered through a DMA channel. Timing is generated by the ST902X TIMER ON-CHIP EVENT strobe signal (see the TIMER section for information on generating these signals), which causes the programmed transfer of data to or from the memory source which can be Register File, Program space memory or Data space memory. An example of application of this technique is shown in figure 37, a complex stepper motor timing sequence automatically being transferred from a table in the Register File (or memory spaces) to the stepper motor drivers. After initialization, this operation is transparent until the task (complex microstepping) is completed.

Table 9. Handshake Control Signal Options

Mode	Handshake Lines	Names
Input to Port	1	WRRDY
	2	$\overline{\text{WRSTB}}$ WRRDY
Output from Port	1	RDRDY
	2	$\overline{\text{RDSTB}}$ RDRDY
Bidirectional	4	$\overline{\text{WRSTB}}$ WRRDY $\overline{\text{RDSTB}}$ RDRDY

Figure 37. Handshake + DMA Used for Stepper Motor Driving



TIMER/WATCHDOG

A 16 bit down-counter, complete with 8 bit prescaler, is integrated into the ST902X core. This is able to operate both as a general purpose timer with associated input and output pins for timing functions, and also as a Watchdog Timer offering a security against possible processor malfunctions due to external events.

Timer Modes

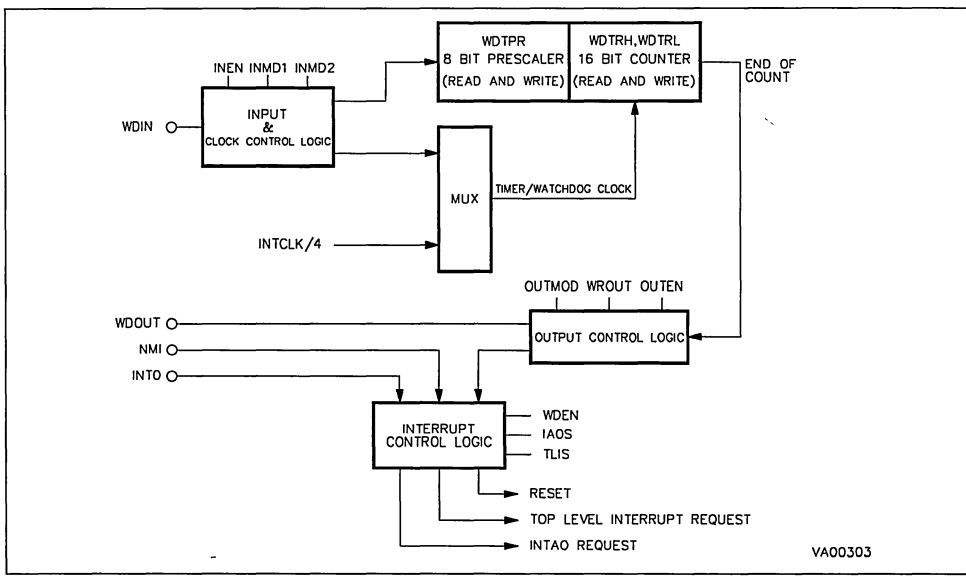
When operating as a Timer, with a timing resolution from 333ns to 5.59s (INTCLK = 12MHz), an input pin (WDIN) and output pin (WDOUT) may be selected as the Alternate Functions of two I/O pins. When WDIN is enabled by the user by setting INEN high (WDTCR.3) and the Alternate Function is set, 4 operating modes are available: The WDIN input may be programmed to act as an event counter input, with high to low transitions causing the counter to decrement (the time duration between the falling edges of the input clock must be at least 333ns, allowing a maximum input frequency of 3MHz). It may also be used for pulse width measurement by being selected as a counter clock gate signal (prescaler to the counter being driven by INTCLK/4), counting being enabled when WDIN is at a high level. Trigger and Re-trigger modes cause a reload of the timer user preset values (providing STSP, WDTCR.7 is active) for a high to low transition on WDIN at any time (Re-trigger mode) or when the counter is at the end of count (Trigger mode). The counter decrements at a rate driven by INTCLK/4.

The WDOUT pin, when set as the Alternate Function, is enabled by OUTEN high (WDTCR.0), and may either toggle the state of the I/O bit (frequency generation, OUTMD = "0", WDTCR.2) or pass the state of the WROUT bit to the output allowing PWM generation (OUTMD = "1") at the end of count (timer value = 0) condition.

Watchdog Mode

The timer functions may be disabled, and the Timer configured for a Watchdog operation by re-setting WDEN (WCR.6) to zero. Once the Watchdog has been selected it CANNOT be set back into the standard timer mode until the next Hardware Reset cycle. The user should set the watchdog timer prescaler and timer reload value before enabling the Watchdog mode. The Watchdog Timer must then be retriggered, causing the reloading of the timer value, by the operation of writing of the byte sequence 0AAh, 055h to the WDTLR register. If this is not done before the Watchdog counts to zero, the Watchdog Timeout condition occurs. This causes a Hardware Reset of the ST902X. The Watchdog reset signal is not output on the external $\overline{\text{RESET}}$ pin.

Figure 38. Timer/Watchdog Block Diagram



TIMER/WATCHDOG (Continued)

Timer/Watchdog Interrupts

The Timer/Watchdog may provide several levels of interrupts selectable by the user. The Timer mode offers two interrupt sources, triggered on the timer value reaching 0, either a prioritized level (by taking the Interrupt priority channel from the External Interrupt INTA0) or by a top level, non-maskable interrupt (taking the external NMI input channel). The interrupt channels are multiplexed from the alternative source according to the status of the IAOS (EIVR.1) and TLIS (EIVR.2) bits as shown in Figure 40. Please refer to the ST9 Technical Manual for further details on changing the interrupt sources of the Timer/Watchdog. When the Watchdog mode is set (WDEN = "0"), the timer value equal to 0 event generates a Hardware reset of the ST902X. The Timer/Watchdog control registers are located within Page 0 of the Paged I/O register group.

Figure 40. Timer/Watchdog Interrupt Sources

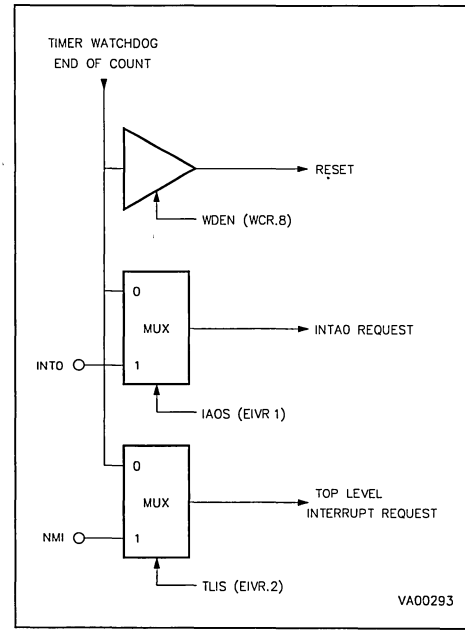
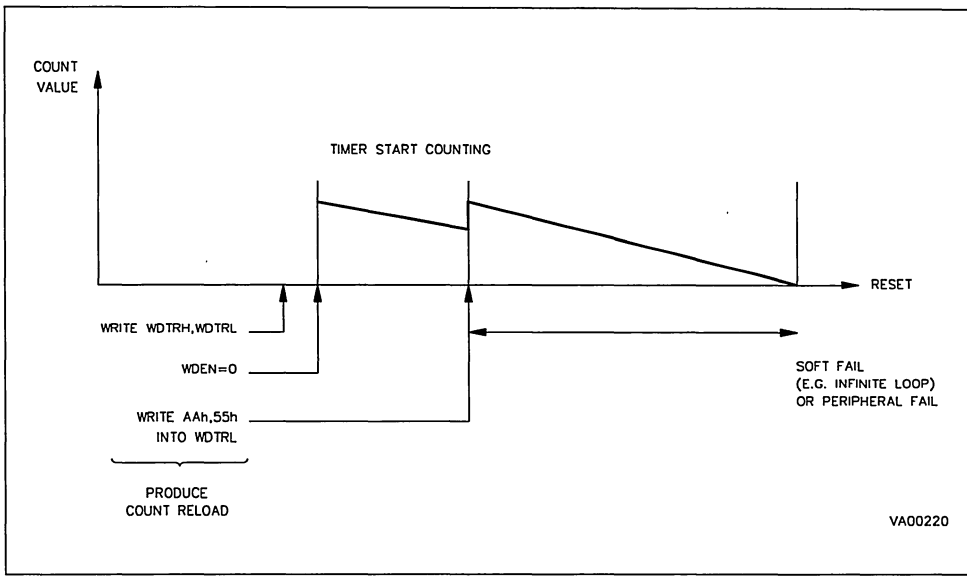


Figure 39. Timer/Watchdog in Watchdog Mode



MULTIFUNCTION TIMERS

The ST902X includes a 16 bit Multifunction Timers (MFT) in addition to the TIMER/WATCHDOG.

The Multifunction Timer is a 16 bit Up/Down counter, driven by the output of an 8 bit prescaler which may be driven by INTCLK/3 (giving a minimum timing resolution of 250ns at INTCLK = 12 MHz) or by an external source. This timer is supported by two 16 bit Comparison Registers for generating timed functions and two 16 bit Capture/Load Registers for timing and variable timebase functions. These features coupled with 2 input pins (TxINA and TxINB) and 2 output pins (TxOUTA and TxOUTB, where x = 0 or 1), available as Alternate Functions, give the timer 12 operating modes for virtually all required timing functions.

MFT Operating Modes

The operating modes are selected by the programming of the Timer Control Register (TCR Timer x) and the Timer Mode Register (TMR) as follows:

ONE-SHOT MODE. The counter stops at the End Of Count Condition (up or down count).

CONTINUOUS MODE. At End Of Count the timer is reloaded from a Load Register.

TRIGGER MODE. A Trigger causes reload from a load register only if the Timer is at End of Count.

RETRIGGER MODE. A Trigger causes reload from a load register at any time.

GATE MODE. Counting is performed only when the external gate input (TxINA or TxINB) is active (logical 0).

CAPTURE MODE. A Trigger causes the timer value to be latched into the selected Capture register.

UP/DOWN MODE. A Trigger causes a count up or down, or a change in counting direction.

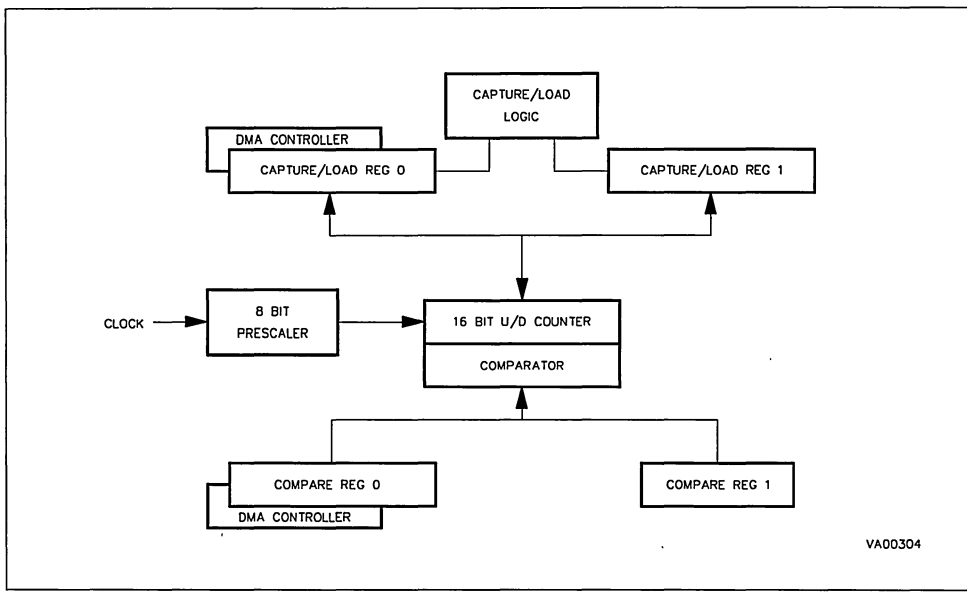
FREE-RUNNING MODE. Up or Down counting is performed to the full range with no action at End of Count. This is used in Bicapture and Capture Modes.

MONITOR MODE. One Capture register follows the contents of the timer.

AUTOCLEAR MODE. The timer is reset to 0000h or FFFFh (up or down count respectively) on a trigger. This gives delta time measurement or free running with a modulo of less than 2^{16}.

BILOAD MODE. The counter is reloaded on an End Of Count condition alternately from the two Load Registers. (PWM output).

Figure 41. Multifunction Timer Block Diagram



MULTIFUNCTION TIMER (Continued)

BICAPTURE MODE. A Trigger causes the current timer value to be transferred alternately to the two Capture registers. (Pulse width measurement).

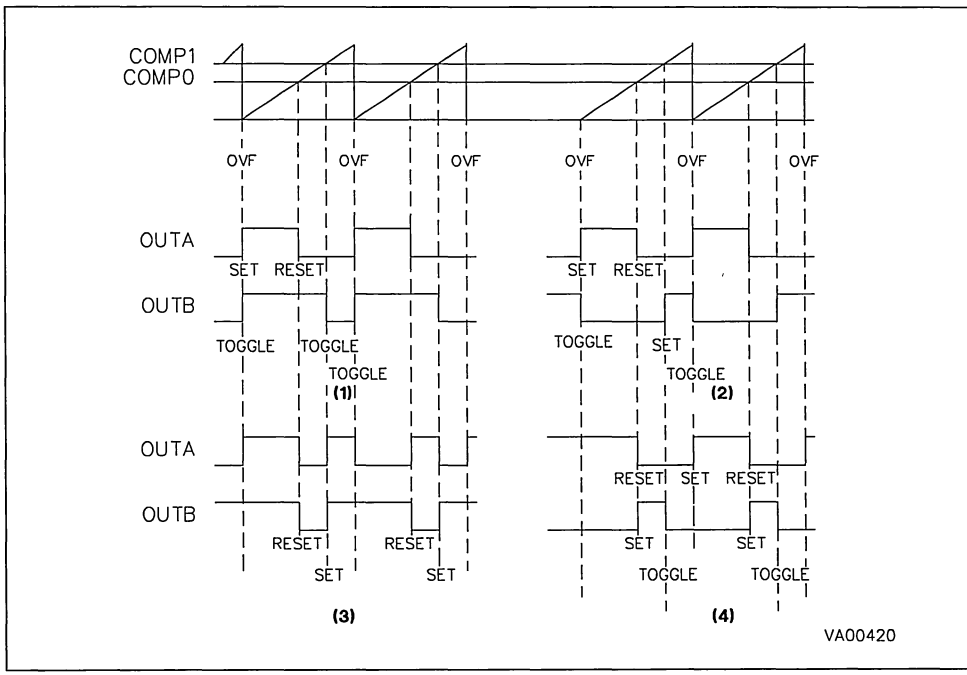
The trigger events may be either caused by software, or an action on the two input pins which may be programmed to respond to rising, falling or both edges of the input. The input modes are selected in the Input Control Register (ICR) as shown in Table 10. This includes the Autodiscriminator mode, which causes the timer to count up or down depending on the phase between the two input edges, such as the signals generated by optical encoders.

The two output pins (available as Alternate Functions) may be programmed through the Output Control Registers OACR and OBCR to be modified (Set, Reset, Toggle or No Operation) on each of Overflow/Underflow (OVF/UNF), Compare on CMP0 valid (CM0), or Compare on CMP1 (COMP1) valid events. This allows repetitive signals such as PWM drive to be output with minimum CPU overhead. Fig 42 shows some typical waveforms available from these signals.

Table 10. Input Pin Function Settings

Input Control Register IN3-IN0 bits	TOINA Input Function	TOINB Input Function
0000	I/O	I/O
0001	I/O	Trigger
0010	Gate	I/O
0011	Gate	Trigger
0100	I/O	Ext.clock
0101	Trigger	I/O
0110	Gate	Ext.clock
0111	Trigger	Trigger
1000	Clock Up	Clock Down
1001	Up/Down	Ext.clock
1010	Trigger Up	Trigger Down
1011	Up/Down	I/O
1100	Autodiscr.	Autodiscr.
1101	Trigger	Ext.clock
1110	Ext.clock	Trigger
1111	Trigger	Gate

Figure 42. Example Output Waveforms



MULTIFUNCTION TIMER (Continued)

The Overflow/Underflow event and the Compare 0 event may also be programmed to give On-chip Event timing signals to trigger other peripheral operations on the ST902X. These are as shown in Table 11.

Table 11. ST902X On-Chip Event Settings

MFT0	Handshake Trigger Port 5

The TxOUTA and TxINA lines for the timer may be connected internally, by setting of the SCx bits of the I/O Connection Register (IOCR).

The Multifunction Timer is enabled for counting by the Counter Enable bit (CEN, TCR.7). When CEN is low, both prescaler and timer are halted. CEN is logically ANDed with the Global Counter Enable bit (GCEN, CICR.7).

MFT Interrupts

The Multifunction Timer can generate interrupt requests from 5 different interrupt sources which are grouped into 3 independent groups. The Interrupt Vector has the source of the interrupt group encoded by hardware into the least significant 3 bits of the vector. This allows the programming of the base address to an 8 byte block within the interrupt vector area of the Program Space. The groups and respective addresses are shown in Table 12.

Table 12. MFT Interrupt Vectors

Interrupt Source	Vector Address
COMP0 COMP1	xxxx x110
CAPT0 CAPT1	xxxx x100
Overflow/Underflow	xxxx x000

Each source may be independently masked, in addition all Timer interrupts may be disabled by the Global Timer Interrupt enable (GTIEN, IDMR.7) control bit. If a Timer interrupt on Compare 0 or Capture 0 does not have its corresponding pending bit reset before the next interrupt, then an overrun condition occurs. This condition is flagged in two dedicated overrun bits in the Timer FLAGS register.

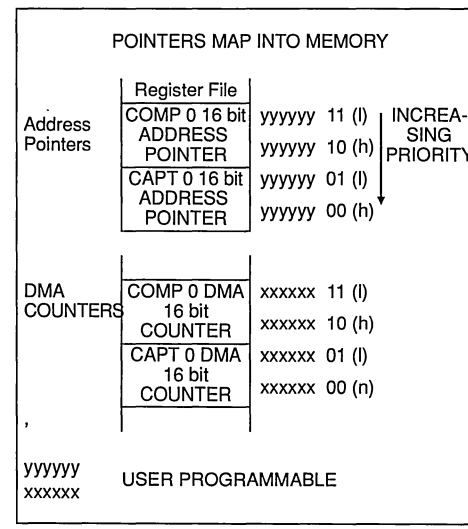
MFT DMA Channels

Two independent DMA channels are present within the MFT, associated to the Compare 0 and Capture 0 sources. This allows 16 bit DMA transactions from Register File/Memory to COMP0 registers, and from CAPT0 registers to Register File/Memory. The DMA channels allow the capture of external event timings in memory allowing off-line analysis, and creating of variable pulse width signal trains, as required by the drive of Triacs in certain modes.

The two interrupt mask sources are independently masked by two DMA mask bits, mapped in the IDMR register. The End of Block (EOB) procedures are as described in the INTERRUPT/DMA section.

The DMA counter and address pointer registers share the most significant user-programmable 6 bits for both DMA channels (COMP 0 and CAPT 0), thus the mapping of the counter and address registers use automatic offsets from the base address. The actual mapping changes dependent on whether the Register File or Memory is addressed for the transfer. The offsets are shown in Table 13.

Table 13-1. MFT DMA Address and Counter Registers for Memory DMA Transfers



MULTIFUNCTION TIMER (Continued)

Table 13-2. MFT DMA Address and Counter Registers for Register File DMA Transfers

POINTERS FOR REGISTER FILE DMA			
8 Bit COUNTER	xxxxxx	11	COMPARE 0
8 bit ADDR. POINTER	xxxxxx	10	
8 bit COUNTER	xxxxxx	01	CAPTURE 0
8 bit ADDR. POINTER	xxxxxx	00	
xxxxxx	USER PROGRAMMABLE		

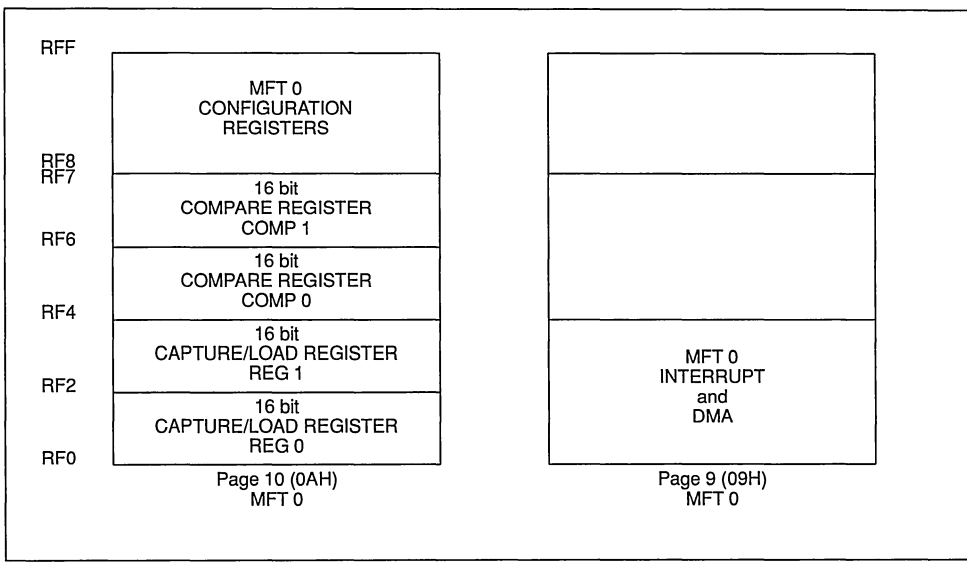
After the transfer of the complete block of data to/from the MFT, the count registers reach the zero value and an end of block interrupt occurs so that the ST9 may process the new data. In many cases, the time taken to reload the data tables and to re-trigger the DMA action causes speed limitations, especially in those applications requiring a continuous high speed data flow, because of the time consumed by the restore routine. An additional DMA function, the SWAP mode, overcomes this limitation. This is enabled by the setting of the SWEN (IDCR.3) bit. This causes hardware generated signals to replace the user address bit 2 of both the address and counter pointers. The address and counter registers are thus duplicated at an offset of 4 registers. At the End Of Block condition, the EOB interrupt is generated to signal the end of DMA, and the state of pointer address bit 2 toggles state automatically and the new address and count values are used. Thus the ST9 can safely process the previous block of data while the new block is being transferred. This will continue until the SWAP mode is disabled.

A software protection scheme is implemented to prevent non-updated pointer registers from being used if a second EOB interrupt arrives during the servicing of the first. This mechanism locks the state of the DMA mask bit to prevent further transfers from taking place. The user should check for this condition in the EOB routine to ensure that all the DMA transfers are properly serviced.

The control Registers of each MFT occupies 20 registers within the I/O paged area. These are mapped as follows:

In addition the MFT is able to trigger byte DMA transfers in both directions through an I/O port with Handshake (see I/O Handshake and DMA).

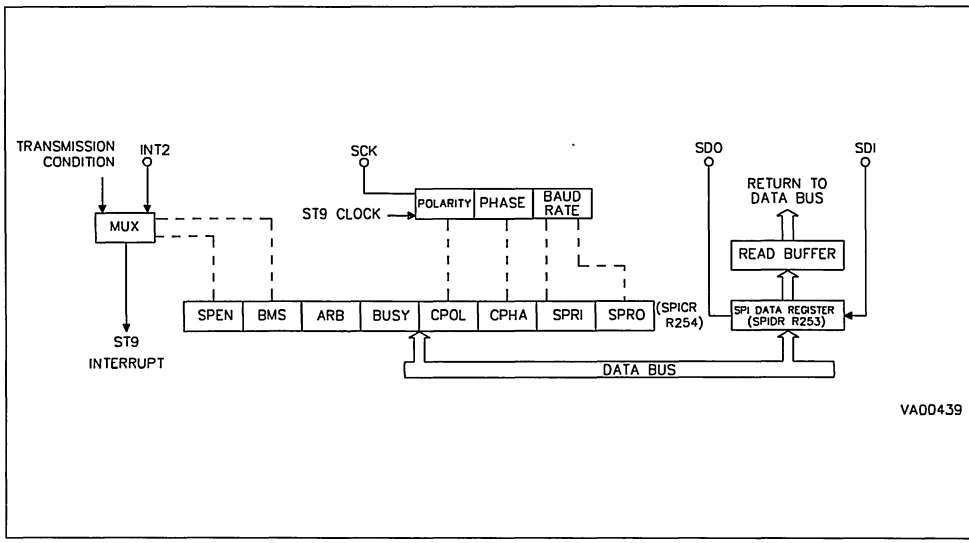
Figure 43. Multifunction Timer Page Maps



SERIAL PERIPHERAL INTERFACE (SPI)

The Serial Peripheral Interface (SPI) is integrated into the Core module of the ST902X and provides a general purpose shift register based peripheral allowing synchronous serial I/O, with special modes allowing compatibility with I^2C-bus and IM-bus Communication standards in addition to the standard serial bus protocol. The SPI uses 3 lines comprising Serial Data Out (SDO), Serial Data In (SDI) and the Synchronous Serial Clock (SCK) which are available as Alternate Functions of I/O pins. Additional I/O pins may act as device selects or IM-bus address ident signals. The functional diagram of the SPI is shown in Figure 44.

Figure 44. SPI Functional Diagram



The SPI, when enabled (SPEN, SPICR.7, high), receives input data from the ST9 internal data bus into the SPIDR, and originates the SCK to shift the data serially through SDO (Most Significant bit first) to the slave device which responds by sending data to the master device via the SDI pin. This implies full duplex transmission with both data-out and data-in synchronized with the same clock signal. Thus the byte transmitted is replaced by the byte received, eliminating the need to separate "Tx Empty" and "Rx full" status bits. After the 8 clock cycles have been concluded, the received data in SPIDR is parallel transferred to the read buffer and data becomes available for the ST902X during the next read cycle of SPIDR. The BUSY bit (SPICR.4) is set when transmission is in progress, this allows the user to monitor the status of the SPI by polling of this bit.

The SPI can operate only in master mode, i.e. the clock is always generated by the ST902X, however the SCK polarity and phase can be programmed to suit all peripheral requirements Figure 45). This, together with the 4 programmable bit rates (divided from the INTCLK, Table 14), provide the large flexibility in handling different protocols.

SERIAL PERIPHERAL INTERFACE (Continued)

Figure 45. SPI Data and Clock Timing

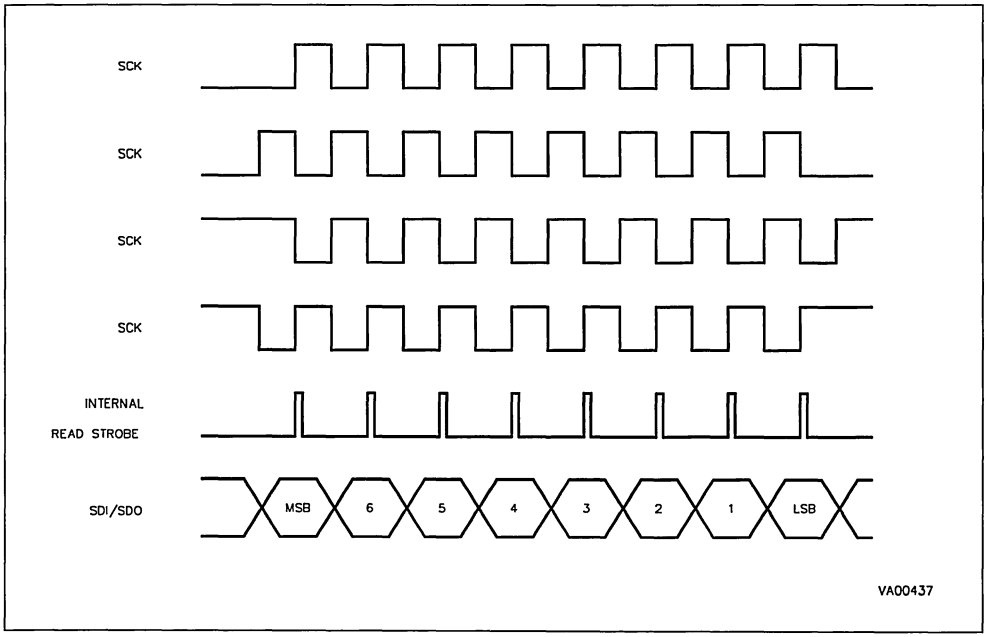


Table 14. SPI Rate Selection

SPR1	SPR0	Clock Divider	SCK Frequency (INTCLK = 12MHz)
0	0	8	1500KHz (T = 0.67µs)
0	1	16	750KHz (T = 1.33µs)
1	0	12	93.50KHz (T = 10.66µs)
1	1	256	46.87KHz (T = 21.33µs)

I²C-bus Compatibility

The SPI includes additional circuitry to enable the use of external I²C-bus peripherals. The I²C-bus mode is a 2 wire bus while the SPI operates with 3 wires, however wire-ANDing SDO and SDI gives the required signalling, while setting the BMS bit causes the enabling of the special I²C-bus features: Clock Slowdown by external devices and Arbitration Lost detection. This mode also affects the Interrupt sources as shown in the next section.

SPI Interrupts

The SPI, when enabled, uses the INT2 external interrupt channel source, using the priority selected for INT2 within the External Interrupt Priority registers. The INT2 mask bit should be set and INT2 pending bit reset before enabling the SPI through SPEN. The BMS (SPICR.6) and SPEN bits select the SPI internal interrupt source as shown in Table 15.

Table 15. SPI Interrupt Sources

SPEN	BMS	Interrupt Source
0	0	External channel INT2
0	1	S-BUS/I²C start or stop condition
1	X	End of one byte transmission

SPI Registers

The two registers controlling the SPI are located in I/O page 0, the Data Register, SPIDR, at R253 and the control register, SPICR, at R254.

SERIAL COMMUNICATIONS INTERFACE

Function

The Serial Communications Interface (SCI) of the ST902X offers a means of full-duplex serial data transfer to a wide range of external equipment with its fully programmable character format control for asynchronous and byte synchronous serial I/O, integral Baud Rate Generator, giving a maximum baud rate of 375K Baud in Asynchronous mode (Internal Clock), and two DMA channels for transparent transmission and reception of characters. Support is also present in hardware for Line Break Detection and generation, character search, network interfacing with 9th bit Address logic, and Local Loop Back and Auto echo modes for Self-Test. The control registers for the SCI exist within one I/O page within the I/O page group.

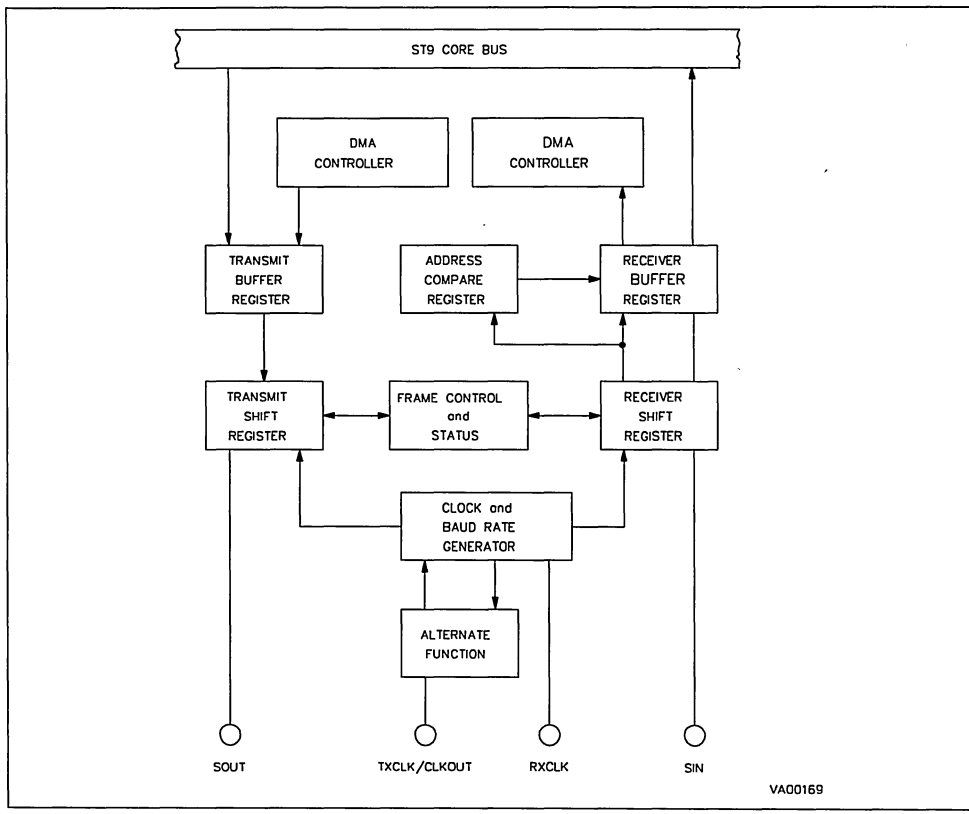
Character Formats

When used for asynchronous character transmission and reception, the character format may be changed (through the Character Control Register CHCR) to suit external equipment requirements. This is summarized in Figure 47.

The baud rate clock for asynchronous mode should be set to the ÷16 Mode and the frequency of the clock input (from an external source or the internal baud-rate generator output) set to suit this.

This format control is also available for the byte synchronous mode (Clock divider set to ÷1), when the data and clock are output in synchronism, the data being sampled once per clock period (Figure 48). For a second synchronous mode, CLKOUT is activated only for the data section of the word (Figure 49) on serial data output, and input data is

Figure 46. SCI Functional Block Diagram



SERIAL COMMUNICATION INTERFACE
(Continued)

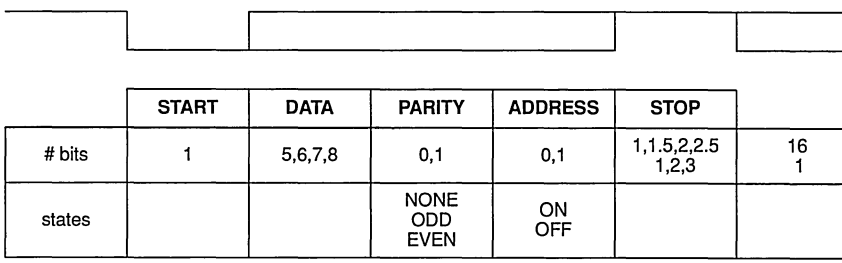
latched on the rising edge of the external synchronised clock input on the RXCLK pin. This mode may be used to access external synchronous peripherals.

The Address bit/D9 is optional and may be added to any word format, it is commonly used in network or machine control applications. When enabled (AB, CHCR.4 = "1"), an address or ninth data bit can be added to a transmitted word by setting the Set Address bit (SA, IDPR.5). This is then appended to the next word entered into the (empty) Transmitter Buffer Register and then cleared by hardware. On character input an Address Bit set can indicate that the data preceding the bit is an address which may be compared in hardware with the value in the Address Compare Register (ACR) to generate an Address Match interrupt when equal.

The Address bit and Address Comparison Register can also be combined to generate an Address Interrupt in 4 modes to suit different protocols, based upon the status of the Address Mode Enable bit (AMEN, IDPR.7) and the Address Mode bit (AM, CHCR.7) as shown in Table 16.

The character match Address Interrupt mode may be used as a powerful character search mode, giving an interrupt on reception of a predetermined character e.g. Carriage Return or End of Block codes.

Figure 47. SCI Character Format



	START	DATA	PARITY	ADDRESS	STOP	
# bits	1	5,6,7,8	0,1	0,1	1,1.5,2,2.5 1,2,3	16 1
states			NONE ODD EVEN	ON OFF		

Figure 48. Byte Synchronous Output

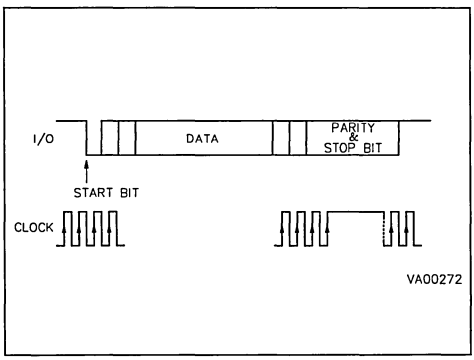
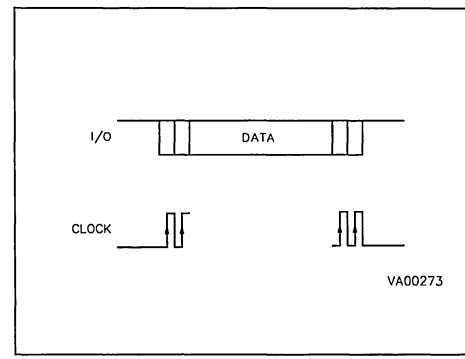


Figure 49. Serial Expansion Mode



SERIAL COMMUNICATION INTERFACE (Continued)

Table 16. Address Interrupt Modes

If 9th Data Bit = 1
If Character Match
If Character Match and 9th Data Bit = 1
If Character Match on Word Immediately Following Break

The Line Break condition is fully supported for both transmission and detection. Line Break is sent by setting the SET_BREAK bit (SB, IDPR.6). This causes the transmitter output to be held low (after all buffered data has been transmitted) for a minimum of one complete word length and until the SB bit is Reset.

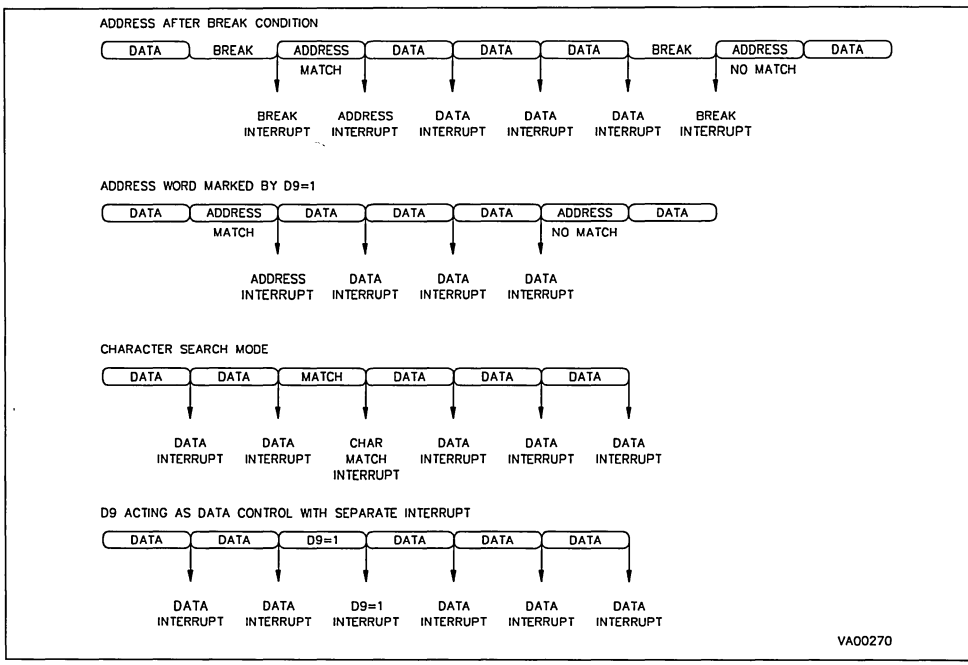
SCI Interrupts

The SCI is able to generate interrupts from multiple sources. Receive interrupts include data pending, receive errors (overrun, framing and parity), address or break pending and transmit interrupts are software selectable for either the Transmit Holding Register Empty (HSN, IMR.7 = "1") or for the Transmit Shift Register Empty (HSN = "0"). Interrupt sources are indicated by the Interrupt pending bits, shown in Table 17. These bits should be reset by the user during the Interrupt Service routine.

Table 17. SCI Interrupt Vector

Interrupt Source	Vector Address
Transmitter Buffer or Shift Register Empty/Transmit DMA end of Block	xxx x110
Received Read/ Receive DMA end of Block	xxxx x100
Break Detector Address Word Match	xxxx x001
Receiver Error	xxxx x000

Figure 50. SCI Interrupt Typical Usage



SERIAL COMMUNICATION INTERFACE (Continued)

When DMA is active the Receive Data Pending bit (RXDP, ISR.2), and the Transmit status bit interrupt sources are replaced by the DMA End Of Block Interrupt sources for transmit and receive, respectively.

Typical Usage of the Interrupts provided by the SCI are show in Figure 50.

The SCI interrupts have an internal priority structure (Table 18) in order to resolve simultaneous events.

Table 18. SCI Interrupt Internal Priority

Receive DMA Request	Highest Priority
Transmit DMA Request	
Receive Interrupt	
Transmit Interrupt	Lowest Priority

The four major levels of interrupt are encoded in hardware to provide two bits of the interrupt vector register, allowing the position of the block of pointer vectors to be resolved to a block size of 8 bytes.

SCI DMA

Two DMA channels are associated with the SCI, for transmit and for receive. These follow the register scheme as described in the DMA section. It should be noted that, after initializing the DMA counter and pointer registers and enabling DMA, data transmission is triggered by a character written into the Transmit Holding register. The DMA End Of Block Interrupts generated on completion of the DMA transfer take the place of the normal transmit and receive character interrupt vectors.

SCI Clock Generation

The communication bit frequency of the SCI transmitter and receiver sections can be provided from the integral Baud Rate Generator (allowing a maximum asynchronous bit rate of 350k Baud) or from external sources (maximum bit rate 175k Baud). This clock is divided by 16 for asynchronous mode (CD, CCR.3, = "0"), or divided by 1 for synchronous modes (CD = "1").

External Clock Sources. The External Clock input pin TXCLK may be programmed in Alternate function by bits TXCLK (CCR.7) and OCLK (CCR.6) to be: the transmit clock input (respecting the ÷16 and ÷1 timing requirements), to act as the output of the Baud Rate Generator (allowing an external divider circuit to provide the receive clock for split rate transmit and receive e.g. 1200/75 baud), or to be CLKOUT, the clock output for the synchronous mode. Receive clock input via RXCLK Alternate function is enabled by the XRX bit CCR.5, this input should be set according to the setting of the CD bit.

Baud Rate Generator. The integral Baud Rate Generator is a 16 bit divide by n circuit of the Internal Clock INTCLK. Thus INTCLK should be chosen to provide a suitable frequency for division by the Baud Rate Generator to give the required transmit and receive bit rates. Suitable INTCLK frequencies and the divider values for standard Baud rates are shown in Table 19.

The act of writing to either of the two registers comprising the 16 bit divider causes a reset of the SCI, allowing initialization of the SCI settings before the writing of the other Baud Rate Generator register.

Self Test

Testing of the communications channel may be performed using the facilities of the SCI. Auto Echo mode (SCI SOUT disconnected, SIN pin internally connected to SOUT pin) and Loopback mode (SCI transmitter and receiver sections disconnected from SOUT and SIN pins and directly connected internally) may be used individually or together.

SERIAL COMMUNICATION INTERFACE (Continued)

Table 19. SCI Baud Rate Generator Divider Values

INTCLK: 7680.000 KHz							
Baud Rate	Clock Factor	Desired Freq (kHz)	Divisor		Actual Baud Rate	Actual Freq (kHz)	Deviation
			Dec	Hex			
50.00	16 X	0.80000	9600	2580	50.00	0.80000	0.0000%
75.00	16 X	1.20000	6400	1900	75.00	1.20000	0.0000%
110.00	16 X	1.76000	4364	110C	109.99	1.75985	0.0083%
300.00	16 X	4.80000	1600	0640	300.00	4.80000	0.0000%
600.00	16 X	9.60000	800	0320	600.00	9.60000	0.0000%
1200.00	16 X	19.20000	400	0190	1200.00	19.20000	0.0000%
2400.00	16 X	38.40000	200	00C8	2400.00	38.40000	0.0000%
4800.00	16 X	76.80000	100	0064	4800.00	76.80000	0.0000%
9600.00	16 X	153.60000	50	0032	9600.00	153.60000	0.0000%
19200.00	16 X	307.20000	25	0019	19200.00	307.20000	0.0000%
38400.00	16 X	614.40000	13	000D	36923.08	590.76923	3.8462%
76800.00	16 X	1228.80000	6	0006	80000.00	1280.00000	4.1667%
INTCLK: 11059.20 KHz							
Baud Rate	Clock Factor	Desired Freq (kHz)	Divisor		Actual Baud Rate	Actual Freq (kHz)	Deviation
			Dec	Hex			
50.00	16 X	0.80000	13824	3600	50.00	0.80000	0.0000%
75.00	16 X	1.20000	9216	2400	75.00	1.20000	0.0000%
110.00	16 X	1.76000	6284	188C	109.99	1.75990	0.0058%
300.00	16 X	4.80000	2304	0900	300.00	4.80000	0.0000%
600.00	16 X	9.60000	1152	0480	600.00	9.60000	0.0000%
1200.00	16 X	19.20000	576	0240	1200.00	19.20000	0.0000%
2400.00	16 X	38.40000	288	0120	2400.00	38.40000	0.0000%
4800.00	16 X	76.80000	144	0090	4800.00	76.80000	0.0000%
9600.00	16 X	153.60000	72	0048	9600.00	153.60000	0.0000%
19200.00	16 X	307.20000	36	0024	19200.00	307.20000	0.0000%
38400.00	16 X	614.40000	18	0012	38400.00	614.40000	0.0000%
76800.00	16 X	1228.80000	9	0009	76800.00	1228.80000	0.0000%

SOFTWARE DESCRIPTION

Addressing Modes

The ST902X offers a wide variety of addressing modes and combinations to facilitate full and rapid access to the address spaces while reducing program length. Register addressing (using the working register group mechanism or directly addressed) can be used as 8 or 16 bit values for data or indirect addressing into the memory spaces or the Register File. The selection between Program Memory and Data Memory is performed through the DP bit in the FLAG Register, all subsequent actions on the memory space will affect the selected map only, apart from the memory map to memory map post-increment addressing mode which allows the map to be specified as part of the instruction for both destination and source operands. Apart from the immediate data and condition codes all operands are expressed as register file or memory addresses.

The available addressing modes, with the ST9 macro-assembler notation, are in Table 20.

Combinations of Available Addressing Modes

Table 21 describes the addressing modes available for the register file and the memory (both as a destination and as a source) for the two operand arithmetic, logic or load instructions.

Table 20. Addressing Mode

Addressing Mode	Notation
Immediate Data	#N #NN
Register Direct	R;r RR;rr
Register Indirect	(R) (r)
Register Indexed	N(r) N(rr)
Memory Direct	NN
Memory Indirect	(RR) (rr)
Memory Indirect with Post-Increment	(rr)+
Memory Indirect with Pre-Decrement	-(rr)
Memory Indexed with Immediate Short Offset	N(rr)
Memory Indexed with Immediate Long Offset	NN(rr)
Memory Indexed with Register Offset	rr(rr)
Memory Indirect Post-Increment to Indirect Register Post-Increment	(rr)+ (r)+
Memory Map to Memory Map both with Post-Increment	(rr)+ (r)+
Bit Address	r.b, (rr).b

Legend:
N = 8 bit Value
NN = 16 bit Value or Address
r = Working Register
R = Directly Addressed Register
( ) = Indirect Addressing
( )+ = Indirect with Post-Increment
-( ) = Indirect with Pre-Decrement
.b = Bit Number (0 to 7)

Table 21. Addressing Mode Permutation for Instructions

Two Operand Arithmetic and Logic Instructions	
Destination	**Source**
Register Direct	Register Direct
Register Direct	Register Indirect
Register Direct	Memory Indirect
Register Direct	Memory Indexed
Register Direct	Memory Indirect with Post- Increment
Register Direct	Memory Indirect with Pre- Decrement
Register Direct	Memory Direct
Register Indirect	Register Direct
Memory Indirect	Register Direct
Memory Indexed	Register Direct
Memory Indirect with Post- Increment	Register Direct
Memory Indirect with Pre- Decrement	Register Direct
Memory Direct	Register Direct

SOFTWARE DESCRIPTION (Continued)

Table 21. Addressing Mode Permutation for Instructions (Continued)

Two Operand Load Instructions	
Destination	**Source**
Register Direct	Register Direct
Register Direct	Register Indirect
Register Direct	Register Indexed
Register Direct	Memory Indirect
Register Direct	Memory Indexed
Register Direct	Memory Indirect with Post- Increment
Register Direct	Memory Indirect with Pre- Decrement
Register Direct	Memory Direct
Register Indirect	Register Direct
Register Indexed	Register Direct
Memory Indirect	Register Direct
Memory Indexed	Register Direct
Memory Indirect with Post- Increment	Register Direct
Memory Indirect with Pre- Decrement	Register Direct
Memory Direct	Register Direct
Two Operand Arithmetic and Logic Instructions	
Destination	**Source**
Register Direct	Immediate
Memory Direct	Immediate
Memory Indirect	Immediate
Two Operand Load Instructions	
Destination	**Source**
Register Direct	Immediate
Memory Direct	Immediate
Memory Indirect	Immediate
Long Indexed Memory (1)	Immediate

Table 21. Addressing Mode Permutation for Instructions (Continued)

Two Operand Arithmetic, Logic & Load Instructions	
Destination	**Source**
Memory Indirect	Memory Indirect
Two Operand Load Instructions (2)	
Destination	**Source**
Register Indirect with Post- Increment	Memory Indirect with Post- Increment
Memory Indirect with Post- Increment	Register Indirect with Post- Increment
Memory Indirect with Post- Increment	Memory Indirect with Post- Increment

Notes:
1. Load Word only
2. Load Byte only

Instruction Set

The ST902X instruction set consists of 87 instruction types functionally divided into eight groups as in Table 22, they are:

- Load (two operands)
- Arithmetic & Logic (two operands)
- Arithmetic Logic and Shift (one operand)
- Stack (one operand)
- Multiply & Divide (two operands)
- Boolean (one or two operands)
- Program Control (zero to three operands)
- Miscellaneous (zero to two operands)

The wide range of instructions facilitates the full use of the register file and address spaces, reducing execution times, while the register pointers mechanism allows an unmatched code efficiency and ultrafast context switching. A particularly notable feature is the comprehensive "Any Bit, Any Register" (ABAR) addressing capability of the Boolean instructions.

The ST902X can operate with a wide range of data lengths from single bit, 4-bit nibbles which can be in the form of Binary Coded Decimal (BCD) digits, 8-bit bytes and 16-bit words. The summary on Table 22 shows the instructions belonging to each group and the number of operands required for each. The source operand is "src", "dst" is the destination operand, and "cc" is the condition code selection.

SOFTWARE DESCRIPTION (Continued)

Table 22. Instruction Set Summary

Load Instructions (Two Operands)								
Mnemonic	**Operand**	**Instruction**	**Flags**					
			C	**Z**	**S**	**V**	**D**	**H**
LD LDW	dst, src dst, src	Load Load Word	– –	– –	– –	– –	– –	– –
Arithmetic and Logic (Two Operands)								
Mnemonic	**Operand**	**Instruction**	**Flags**					
			C	**Z**	**S**	**V**	**D**	**H**
ADD ADDW	dst, src dst, src	Add Add Word	Δ Δ	Δ Δ	Δ Δ	Δ Δ	0 ?	Δ ?
ADC ADCW	dst, src dst, src	Add with Carry Add Word with Carry	Δ Δ	Δ Δ	Δ Δ	Δ Δ	0 ?	Δ ?
SUB SUBW	dst, src dst, src	Subtract Subtract Word	Δ Δ	Δ Δ	Δ Δ	Δ Δ	1 ?	Δ ?
SBC SBCW	dst, src dst, src	Subtract with Carry Subtract Word with Carry	Δ Δ	Δ Δ	Δ Δ	Δ Δ	1 ?	Δ ?
AND ANDW	dst, src dst, src	Logical AND Logical Word AND	– –	Δ Δ	Δ Δ	0 0	– ?	– ?
OR ORW	dst, src dst, src	Logical OR Logical Word OR	– –	Δ Δ	Δ Δ	0 0	– –	– –
XOR XORW	dst, src dst, src	Logical Exclusive OR Logical Word Exclusive OR	– –	Δ Δ	Δ Δ	0 0	– –	– –
CP CPW	dst, src dst, src	Compare Compare Word	Δ Δ	Δ Δ	Δ Δ	Δ Δ	– –	– –
TM TMW	dst, src dst, src	Test Under Mask Test Word Under Mask	– –	Δ Δ	Δ Δ	0 0	– –	– –
TCM TCMW	dst, src dst, src	Test Complement Under Mask Test Word Complement Under Mask	– –	Δ Δ	Δ Δ	0 0	– –	– –

Legend :
0 = Bit set to zero
1 = Bit set to one
Δ = Bit affected
? = Bit status undefined
– = Bit not affected

SOFTWARE DESCRIPTION (Continued)

Table 22. Instruction Set Summary (Continued)

Arithmetic Logic and Shift (One Operand)								
Mnemonic	**Operand**	**Instruction**	**Flags**					
			C	**Z**	**S**	**V**	**D**	**H**
INC INCW	dst dst	Increment Increment Word	– –	Δ Δ	Δ Δ	Δ Δ	– –	– –
DEC DECW	dst dst	Decrement Decrement Word	– –	Δ Δ	Δ Δ	Δ Δ	– –	– –
SLA SLAW	dst dst	Shift Left Arithmetic Shift Word Left Arithmetic	Δ Δ	Δ Δ	Δ Δ	0 0	0 ?	Δ ?
SRA SRAW	dst dst	Shift Right Arithmetic Shift Word Right Arithmetic	Δ Δ	Δ ?	Δ Δ	Δ 0	0 –	Δ –
RRC RRCW	dst dst	Rotate Right through Carry Rotate Word Right through Carry	Δ Δ	Δ ?	Δ Δ	Δ Δ	– –	– –
RLC RLCW	dst dst	Rotate Left through Carry Rotate Word Left through Carry	Δ Δ	Δ ?	Δ Δ	Δ Δ	– –	– –
ROR	dst	Rotate Right	Δ	Δ	Δ	Δ	–	–
ROL	dst	Rotate Left	Δ	Δ	Δ	Δ	–	–
CLR	dst	Clear	–	–	–	–	–	–
CPL	dst	Complement Register	–	Δ	Δ	0	–	–
SWAP	dst	Swap Nibbles	?	Δ	Δ	?	–	–
DA	dst	Decimal Adjust	Δ	Δ	Δ	?	–	–
Stack Instructions (One Operand)								
Mnemonic	**Operand**	**Instruction**	**Flags**					
			C	**Z**	**S**	**V**	**D**	**H**
PUSH PUSHW PEA	src src src	Push on System Stack Push Word on System Stack Push Effective Address on System Stack	– – –	– – –	– – –	– – –	– – –	– – –
POP POPW	dst dst	Pop from System Stack Pop Word from System Stack	– –	– –	– –	– –	– –	– –
PUSHU PUSHUW PEAU	src src src	Push on User Stack Push Word on User Stack Push Effective Address on User Stack	– – –	– – –	– – –	– – –	– – –	– – –
POPU POPUW	dst dst	Pop from User Stack Pop Word from User Stack	– –	– –	– –	– –	– –	– –

SOFTWARE DESCRIPTION (Continued)

Table 22. Instruction Set Summary (Continued)

Multiply and Divide Instructions (Two Operands)								
Mnemonic	**Operand**	**Instruction**	**Flags**					
			C	**Z**	**S**	**V**	**D**	**H**
MUL	dst, src	Multiply 8x8	Δ	Δ	Δ	Δ	0	?
DIV DIVWS	dst, src	Divide 16/8 Divide Word Stepped 32/16	1 ?	Δ ?	Δ ?	? ?	1 ?	? ?
Boolean Instructions (Two Operands)								
Mnemonic	**Operand**	**Instruction**	**Flags**					
			C	**Z**	**S**	**V**	**D**	**H**
BLD	dst, src	Bit Load	–	–	–	–	–	–
BAND	dst, src	Bit AND	–	–	–	–	–	–
BOR	dst, src	Bit OR	–	–	–	–	–	–
BXOR	dst, src	Bit Exclusive OR	–	–	–	–	–	–
Boolean Instructions (One Operand)								
Mnemonic	**Operand**	**Instruction**	**Flags**					
			C	**Z**	**S**	**V**	**D**	**H**
BSET	dst	Bit Set	–	–	–	–	–	–
BRES	dst	Bit Reset	–	–	–	–	–	–
BCPL	dst	Bit Complement	–	–	–	–	–	–
BTSET	dst	Bit Test and Set	–	Δ	Δ	0	–	–
Program Control Instructions (Three Operands)								
Mnemonic	**Operand**	**Instruction**	**Flags**					
			C	**Z**	**S**	**V**	**D**	**H**
CPJFI	dst, src	Compare and Jump on False, Otherwise Post Increment	–	–	–	–	–	–
CPJTI	dst, src	Compare and Jump on True, Otherwise Post Increment	–	–	–	–	–	–

SOFTWARE DESCRIPTION (Continued)

Table 22. Instruction Set Summary (Continued)

Program Control Instructions (Two Operands)								
Mnemonic	**Operand**	**Instruction**	**Flags**					
			C	**Z**	**S**	**V**	**D**	**H**
BTJF	dst, src	Bit Test and Jump if False	–	–	–	–	–	–
BTJT	dst, src	Bit Test and Jump if True	–	–	–	–	–	–
DJNZ	dst, src	Decrement a Working Register and Jump if Not Zero	–	–	–	–	–	–
DWJNZ	dst,src	Decrement a Register Pair and Jump if Not Zero	–	–	–	–	–	–
Program Control Instructions (One Operand)								
Mnemonic	**Operand**	**Instruction**	**Flags**					
			C	**Z**	**S**	**V**	**D**	**H**
JR	cc, dst	Jump Relative if Condition is Met	–	–	–	–	–	–
JP	cc, dst	Jump if Condition is Met	–	–	–	–	–	–
JP	dst	Unconditional Jump	–	–	–	–	–	–
CALL	dst	Unconditional Call	–	–	–	–	–	–
Program Control Instructions (No Operand)								
Mnemonic	**Operand**	**Instruction**	**Flags**					
			C	**Z**	**S**	**V**	**D**	**H**
RET		Return from Subroutine	–	–	–	–	–	–
IRET		Return from Interrupt	Δ	Δ	Δ	Δ	Δ	Δ
WFI		Stop Program Execution and Wait Next Enabled Interrupt. If a DMA request is present the CPU executes the DMA service routine and returns to WFI state.	–	–	–	–	–	–
HALT		Stop Program Execution until RESET	–	–	–	–	–	–
Miscellaneous (Two Operands)								
Mnemonic	**Operand**	**Instruction**	**Flags**					
			C	**Z**	**S**	**V**	**D**	**H**
XCH	dst, src	Exchange Registers	–	–	–	–	–	–

SOFTWARE DESCRIPTION (Continued)

Table 22. Instruction Set Summary (Continued)

Miscellaneous (One Operand)								
Mnemonic	**Operand**	**Instruction**	**Flags**					
			C	**Z**	**S**	**V**	**D**	**H**
SRP	src	Set Register Pointer Long (16 Working Registers)	–	–	–	–	–	–
SRP0	src	Set Register Pointer 0 (8 LSB Working Registers)	–	–	–	–	–	–
SRP1	src	Set Register Pointer 1 (8 MSB Working Registers)	–	–	–	–	–	–
SPP	src	Set Page Pointer	–	–	–	–	–	–
EXT	src	Sign Extend	–	–	–	–	–	–
Miscellaneous (No Operand)								
Mnemonic	**Operand**	**Instruction**	**Flags**					
			C	**Z**	**S**	**V**	**D**	**H**
EI		Enable Interrupts	–	–	–	–	–	–
DI		Disable Interrupts	–	–	–	–	–	–
SCF		Set Carry Flag	1	–	–	–	–	–
RCF		Reset Carry Flag	0	–	–	–	–	–
CCF		Complement Carry Flag	Δ	–	–	–	–	–
SPM		Select Program Memory	–	–	–	–	–	–
SDM		Select Data Memory	–	–	–	–	–	–
NOP		No Operation	–	–	–	–	–	–

Processor Flags

An important aspect of any single chip microcontroller is the ability to test data and make the appropriate action based on the results. In order to provide this facility, register 231 in the Register File is used as a Flag Register. Six bits of this register are used as the following flags:

C - Carry

Z - Zero

S - Sign

V - Overflow

D - Decimal Adjust

H - Half Carry

One of the two remaining bits in the flag register is available to the user (bit 1, F1). Bit 0 is the Program/Data Memory selector bit and is operated on directly by the hardware within the ST902X. The P/$\overline{D}$ pin will follow the status of this bit.

Condition Codes. Flags C, Z, S, and V control the operation of the "conditional" Jump instructions. Table 23 shows the condition codes and the flag settings affecting the jump.

SOFTWARE DESCRIPTION (Continued)

Table 23. Condition Codes Summary

Mnemonic Code	Meaning	Flag Setting
F	Always False	—
T	Always True	—
C	Carry	C = 1
NC	No Carry	C = 0
Z	Zero	Z = 1
NZ	No Zero	Z = 0
PL	Plus	S = 0
MI	Minus	S = 1
OV	Overflow	V = 1
NOV	No Overflow	V = 0
EQ	Equal	Z = 1
NE	Not Equal	Z = 0
GE	Greater Then or Equal	(S xor V) = 0
LT	Less Than	(S xor V) = 1
GT	Greater Than	(Z or (S xor V)) = 0
LE	Less Than or Equal	(Z or (S xor V)) = 1
UGE	Unsigned Greater Than or Equal	C = 0
UL	Unsigned Less Than	C = 1
UGT	Unsigned Greater Than	(C = 0 and Z = 0) = 1
ULE	Unsigned Less Than or Equal	(C or Z) = 1

POWERFUL DEVELOPMENT ENVIRONMENT

ST9 Software Tools

The following Software Tools are available for MS-DOS, SUN-3 and SUN-4 operating systems:

AST9 high-level macro assembler with predefinited macro instructions (IF/ELSE, WHILE, DO, LOOP, SWITCH, BREAK, PROCEDURE, RESTURN).

LST9 Incremental Linker/Loader.

CST9 Optimised C-Compiler (ANSI STANDARD).

ARST9 Library Archiver.

SIMST9 Software Simulator with realtime emulation executor

ST902X Hardware Emulator. Realtime emulation of the ST902X in all packaging options is performed by a modular emulation system, interfaced to the host computer through an RS232 channel, whit powerful hardware breakpoints, on-line assembler/disassembler, emulation and trace memory. The emulator is fully supported by a simbolic on-line debugger and help facility.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	– 0.3 to 7.0	V
AV_{DD}, AV_{SS}	Analog Supply Voltage	$V_{SS} \le AV_{SS} < AV_{DD} \le V_{DD}$	V
V_I	Input Voltage	V_{SS} – 0.3 to V_{DD} +0.3	V
V_O	Output Voltage	V_{SS} – 0.3 to V_{DD} +0.3	V
T_{STG}	Storage Temperature	– 55 to + 150	°C

Note: Stresses above those listed as "absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value		Unit
		Min.	Max.	
T_A	Operating Temperature	– 40	85	C
V_{DD}	Operating Supply Voltage	4.5	5.5	V
f_{OSCE}	External Oscillator Frequency		24	MHz
f_{OSCI}	Internal Oscillator Frequency		12	MHz

DC ELECTRICAL CHARACTERISTICS

(V_{DD} = 5V ± 10% T_A = – 40 °C to + 85°C, unless otherwise specified)

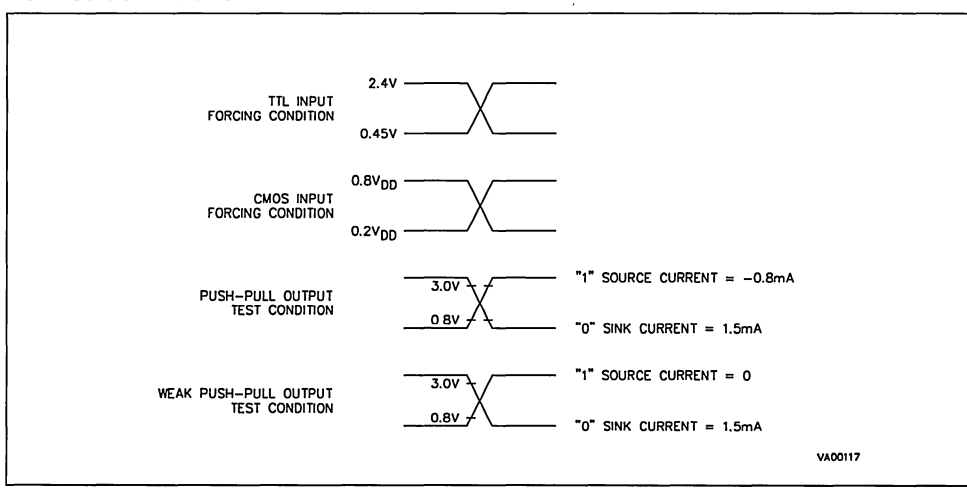
Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
V_{IHCK}	Clock Input High Level	External Clock	0.7 V_{DD}		V_{DD} + 0.3	V
V_{ILCK}	Clock Input Low Level	External Clock	– 0.3		0.3 V_{DD}	V
V_{IH}	Input High Level	TTL	2.0		V_{DD} + 0.3	V
		CMOS	0.7 V_{DD}		VDD + 0.3	V
V_{IL}	Input Low Level	TTL	– 0.3		0.8	V
		CMOS	– 0.3		0.3 V_{DD}	V
V_{IHRS}	Reset Input High Level		0.7 V_{DD}		V_{DD} + 0.3	V
V_{ILRS}	Reset Input Low Level		–0.3		0.3 V_{DD}	V
V_{HYRS}	Reset Input Hysteresis		0.3		1.5	V
V_{OH}	Output High Level	Push Pull, Iload = – 0.8mA	V_{DD} – 0.8			V
V_{OL}	Output Low Level	Push Pull or Open Drain, Iload = – 1.6mA			0.4	V

DC ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
I_{WPU}	Weak Pull-up Current	Bidirectional Weak Pull-up, V_{OL} = 0V	– 80	– 200	– 420	µA
I_{APU}	Active Pull-up Current, for INT0 and INT7 only	V_{IN} < 0.8V	– 80	– 200	– 420	µA
I_{LKIO}	I/O Pin Input Leakage	Input/Tri-State, 0V < V_{IN} < V_{DD}	– 10		+ 10	µA
I_{LKRS}	Reset Pin Input Leakage	0V < V_{IN} < V_{DD}	– 30		+ 30	µA
I_{LKAD}	A/D Pin Input Leakage	Alternate Function, Open Drain, 0V < V_{IN} < V_{DD}	– 3		+ 3	µA
I_{LKAP}	Active Pull-up Input Leakage	0V < V_{IN} < 0.8V	– 10		+ 10	µA
I_{LKOS}	OSCIN Pin Input Leakage	0V < V_{IN} < V_{DD}	– 10		+ 10	µA
I_{DD}	Run Mode Current	24MHz, Note 1		32	70	mA
		4MHz, Note 1		6	12	mA
I_{DP2}	Run Mode Current Prescale by 2	24MHz, Note 1		19	40	mA
		4MHz, Note 1		4	8	mA
I_{WFI}	WFI Mode Current	24MHz, Note 1		9	18	mA
		4MHz, Note 1		2.5	5	mA
I_{HALT}	HALT Mode Current	24MHz, Note 1			100	µA

Note:
1. All I/O Ports are configured in Bidirectional Weak Pull-up Mode with no DC load, External Clock pin (OSCIN) is driven by square wave external clock. No peripheral working. External interface not active (Internal Program Execution).

DC TEST CONDITIONS



AC ELECTRICAL CHARACTERISTICS

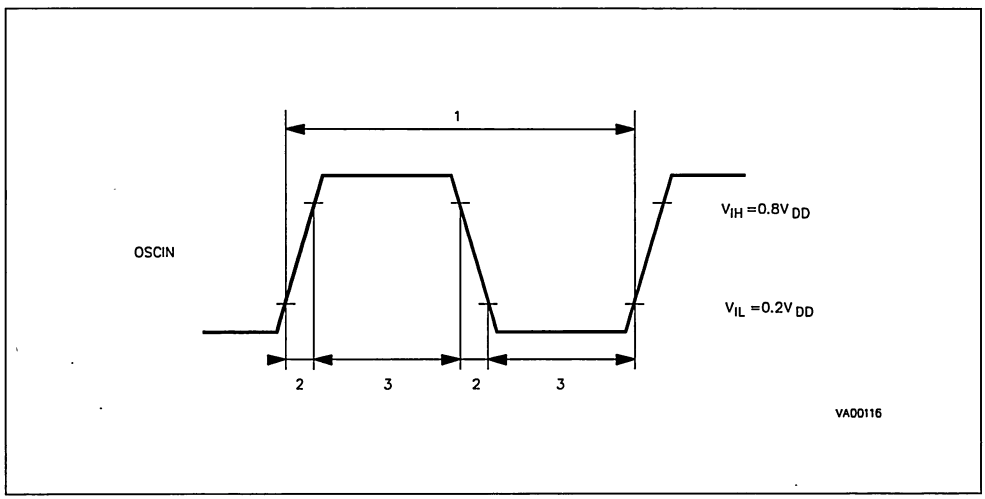
CLOCK TIMING TABLE

(V_{DD} = 5V ± 10%, T_A = − 40°C to + 85°C, unless otherwise specified)

N°	Symbol	Parameter	Value		Unit	Note
			Min.	Max.		
1	TpC	OSCIN Clock Period	41.5		ns	1
			83		ns	2
2	TrC, TfC	OSCIN Rise and Fall Time		12	ns	
3	TwCL, TwCH	OSCIN Low and High Width	25	12	ns	1
			38		ns	2

Notes:
1. Clock divided by 2 internally (MODER.DIV2=1)
2. Clock not divided by 2 internally (MODER.DIV2=0)

CLOCK TIMING



EXTERNAL BUS TIMING TABLE

(V_{DD} = 5V ± 10%, T_A = – 40 °C to + 85 °C, Cload = 50pF, CPUCLK = 12MHz, unless otherwise specified)

N°	Symbol	Parameter	Value (Note)				Unit
			OSCIN Divided By 2	OSCIN Not Divided By 2	Min.	Max.	
1	TsA (AS)	Address Set-up Time before $\overline{AS}$ ↑	TpC (2P+1) –22	TWCH+PTpC –18	20		ns
2	ThAS (A)	Address Hold Time after $\overline{AS}$ ↑	TpC –17	TwCL –13	25		ns
3	TdAS (DR)	$\overline{AS}$ ↑ to Data Available (read)	TpC (4P+2W+4) –52	TpC (2P+W+2) –51		115	ns
4	TwAS	$\overline{AS}$ Low Pulse Width	TpC (2P+1) –7	TwCH+PTpC –3	35		ns
5	TdAz (DS)	Address Float to $\overline{DS}$ ↓	0	0	0		ns
6	TwDSR	$\overline{DS}$ Low Pulse Width (read)	TpC (4P+2W+3) –20	TwCH+TpC (2P+W+1) –16	105		ns
7	TwDSW	$\overline{DS}$ Low Pulse Width (write)	TpC (2P+2W+2) –13	TpC (P+W+1) –13	70		ns
8	TdDSR (DR)	$\overline{DS}$ ↓ to Data Valid Delay (read)	TpC (4P+2W-3) –50	TwCH+TpC(2P+W+1) – 46		75	ns
9	ThDR (DS)	Data to $\overline{DS}$ ↑ Hold Time (read)	0	0	0		ns
10	TdDS (A)	$\overline{DS}$ ↑ to Address Active Delay	TpC –7	TwCL –3	35		ns
11	TdDS (AS)	$\overline{DS}$ ↑ to $\overline{AS}$ ↓ Delay	TpC –18	TwCL –14	24		ns
12	TsR/W (AS)	R/$\overline{W}$ Set-up Time before $\overline{AS}$ ↑	TpC (2P+1) –22	TwCH+PTpC –18	20		ns
13	TdDSR (R/W)	$\overline{DS}$ ↑ to R/$\overline{W}$ and Address Not Valid Delay	TpC –9	TwCL –5	33		ns
14	TdDW (DSW)	Write Data Valid to $\overline{DS}$ ↓ Delay (write)	TpC (2P+1) –32	TwCH+PTpC –28	10		ns
15	ThDS (DW)	Data Hold Time after DS ↑ (write)	TpC –9	TwCL –5	33		ns
16	TdA (DR)	Address Valid to Data Valid Delay (read)	TpC (6P+2W+5) –68	TwCH+TpC (3P+W+2) –64		140	ns
17	TdAs (DS)	$\overline{AS}$ ↑ to $\overline{DS}$ ↓ Delay	TpC –18	TwCL –14	24		ns

Note: The value left hand two columns show the formula used to calculate the timing minimum or maximum from the oscillator clock period, prescale value and number of wait cycles inserted.
The value right hand two columns show the timing minimum and maximum for an external clock at 24 MHz divided by 2, prescaler value of zero and zero wait status.

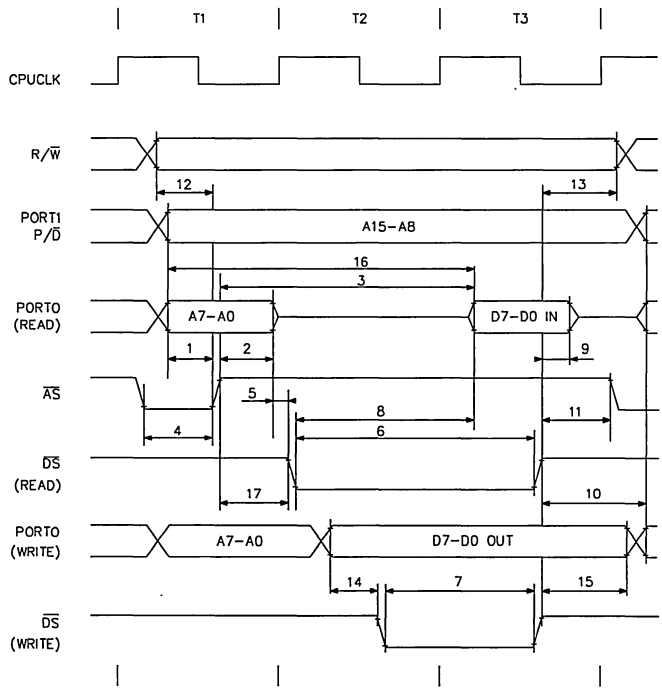
Legend:
P = Clock Prescaling Value
W = Wait Cycles
TpC = OSCIN Period
TwCH = High Level OSCIN half period
TwCL = Low Level OSCIN half period

EXTERNAL WAIT TIMING TABLE (V_{DD} = 5V ± 10%, T_A = –40°C to +85°C, Cload = 50pF, INTCLK = 12MHz, Push-pull output configuration, unless otherwise specified)

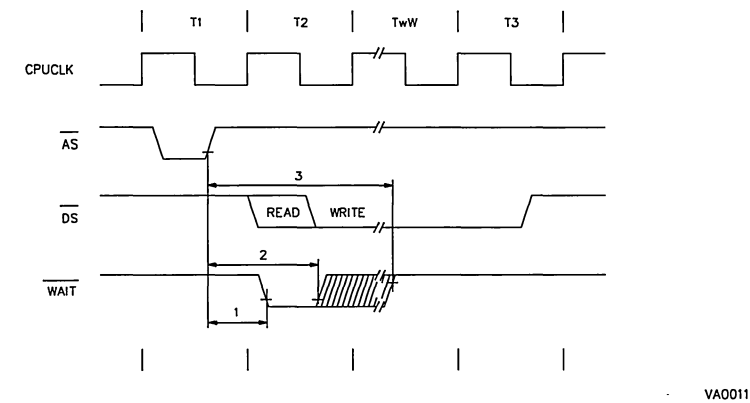
N°	Symbol	Parameter	Value (Note)				Unit
			OSCIN Divided By 2	OSCIN Not Divided By 2	Min.	Max.	
1	TdAS (WAIT)	$\overline{AS}$ ↑ to $\overline{WAIT}$ ↓ Delay	2(P+1)TpC –29	(P+1)TpC –29		40	ns
2	TdAS (WAIT)	$\overline{AS}$ ↑ to $\overline{WAIT}$ ↑ Minimum Delay	2(P+W+1)TpC –4	(P+W+1)TpC –4	80		ns
3	TdAS (WAIT)	$\overline{AS}$ ↑ to $\overline{WAIT}$ ↑ Maximum Delay	2(P+W+1)TpC – 29	(P+W+1)TpC –29		83W+40	ns

Note: The value left hand two columns show the formula used to calculate the timing minimum or maximum from the oscillator clock period, prescale value and number of wait cycles inserted.
The value right hand two columns show the timing minimum and maximum for an external clock at 24 MHz divided by 2, prescale value of zero and zero wait status.

EXTERNAL BUS TIMING



EXTERNAL WAIT TIMING

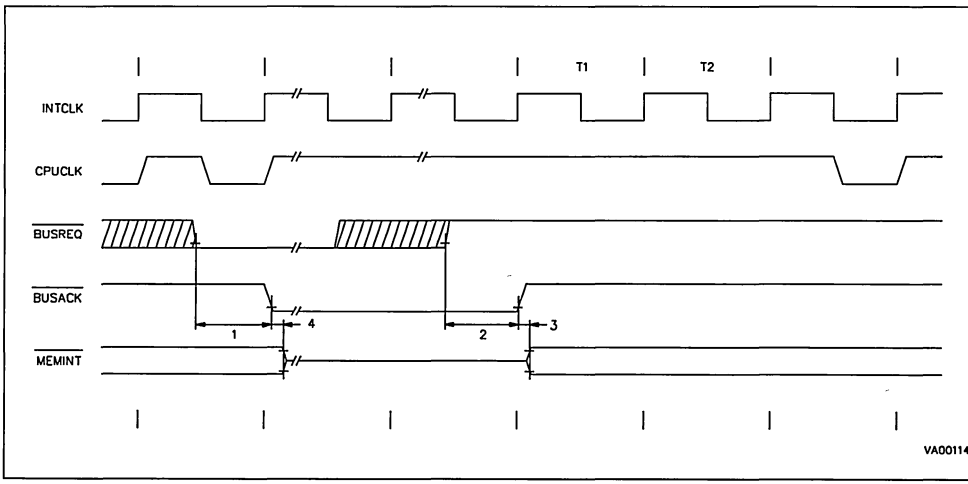


BUS REQUEST/ACKNOWLEDGE TIMING TABLE (V_{DD} = 5V ± 10%, T_A = −40°C to +85°C, Cload = 50pF, INTCLK = 12MHz, Push-pull output configuration, unless otherwise specified)

N°	Symbol	Parameter	Value (Note)				Unit
			OSCIN Divided By 2	OSCIN Not Divided By 2	Min.	Max.	
1	TdBR (BACK)	$\overline{BREQ}$ ↓ to $\overline{BUSACK}$ ↓	TpC+8	TwCL+12	50		ns
			TpC(6P+2W+7)+65	TpC(3P+W+3)+TwCL+65		360	ns
2	TdBR (BACK)	$\overline{BREQ}$ ↑ to $\overline{BUSACK}$ ↑	3TpC+60	TpC+TwCL+60		185	ns
3	TdBACK (BREL)	$\overline{BUSACK}$ ↓ to Bus Release	20	20		20	ns
4	TdBACK (BACT)	$\overline{BUSACK}$ ↑ to Bus Active	20	20		20	ns

Note: The value left hand two columns show the formula used to calculate the timing minimum or maximum from the oscillator clock period, prescale value and number of wait cycles inserted.
The value right hand two columns show the timing minimum and maximum for an external clock at 24 MHz divided by 2, prescale value of zero and zero wait status.

BUS REQUEST/ACKNOWLEDGE TIMING



Note : MEMINT = group of memory interface signals : $\overline{AS}$, $\overline{DS}$, R/$\overline{W}$, P00-P07, P10-P17.

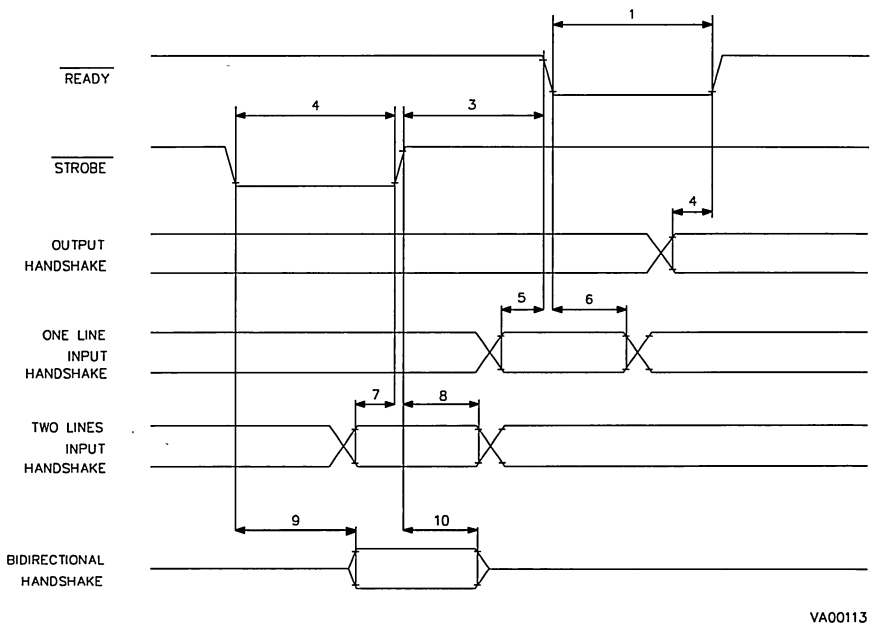
HANDSHAKE TIMING TABLE (V_{DD} = 5V ± 10%, T_A = –40°C to +85°C, Cload = 50pF, INTCLK = 12MHz, Push-pull output configuration, unless otherwise specified)

N°	Symbol	Parameter	Value (Note)				Min.	Max.	Unit
			OSCIN Divided By 2		OSCIN Not Divided By 2				
			Min.	Max.	Min.	Max.			
1	TwRDY	RDRDY, WRRDY Pulse Width in One Line Handshake	2TpC (P+W+1) –18		Tp (P+W+1) – 18		65		ns
2	TwSTB	$\overline{\text{RDSTB}}$, $\overline{\text{WRSTB}}$ Pulse Width	2TpC+12		TpC+12		95		ns
3	TdST (RDY)	$\overline{\text{RDSTB}}$, or $\overline{\text{WRSTB}}$ ↑ to RDRDY or WRRDY ↓		TpC+45		(TpC-TwCL) +45		87	ns
4	TsPD (RDY)	Port Data to RDRDY ↑ Set-up Time	(2P+2W+1) TpC –25		TwCH+(W+P) TpC –25		16		ns
5	TsPD (RDY)	Port Data to WRRDY ↓ Set-up Time in One Line Handshake	43		43		43		ns
6	ThPD (RDY)	Port Data to WRRDY ↓ Hold Time in One Line Handshake	0		0		0		ns
7	TsPD (STB)	Port Data to $\overline{\text{WRSTB}}$ ↑ Set-up Time	10		10		10		ns
8	ThPD (STB)	Port Data to WRSTB ↑ Hold Time	25		25		25		ns
9	TdSTB (PD)	$\overline{\text{RDSTBD}}$ ↑ to Port Data Delay Time in Bidirectional Handshake		35		35		35	ns
10	TdSTB (PHZ)	$\overline{\text{RDSTB}}$ ↑ to Port High-Z Delay Time in Bidirectional Handshake		25		25		25	ns

Note: The value left hand two columns show the formula used to calculate the timing minimum or maximum from the oscillator clock period, prescale value and number of wait cycles inserted.
The value right hand two columns show the timing minimum and maximum for an external clock at 24 MHz divided by 2, prescaler value of zero and zero wait status.

Legend:
P = Clock Prescaling Value (R235.4,3,2)
W = Programmable Wait Cycles (R252.2.1.0/5,4,3) + External Wait Cycles

HANDSHAKE TIMING

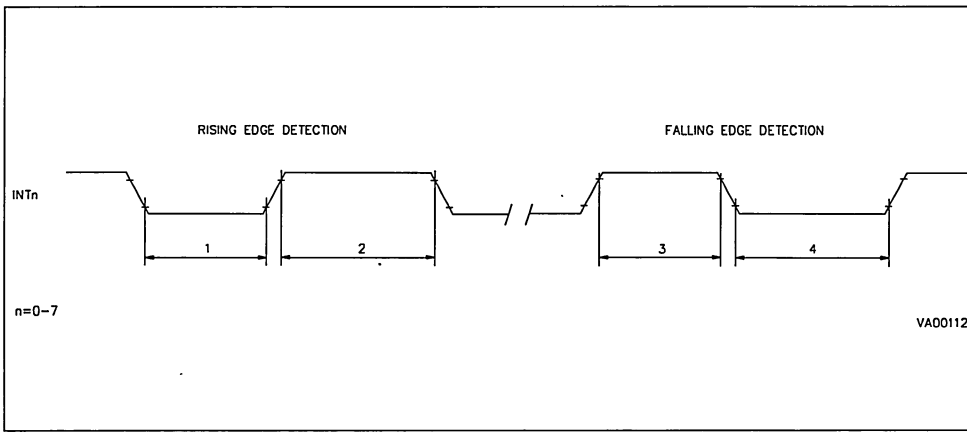


EXTERNAL INTERRUPT TIMING TABLE (V_{DD} = 5V ± 10%, T_A = –40°C to +85°C, Cload = 50pF, INTCLK = 12MHz, Push-pull output configuration, unless otherwise specified)

N°	Symbol	Parameter	Value (Note)				Unit
			OSCIN Divided By 2 Min.	OSCIN Not Divided By 2 Min.	Min.	Max.	
1	TwLR	Low Level Minimum Pulse Width in Rising Edge Mode	2TpC+12	TpC+12	95		ns
2	TwHR	High Level Minimum Pulse Width in Rising Edge Mode	2TpC+12	TpC+12	95		ns
3	TwHF	High Level Minimum Pulse Width in Falling Edge Mode	2TpC+12	TpC+12	95		ns
4	TwLF	Low Level Minimum Pulse Width in Falling Edge Mode	2TpC+12	TpC+12	95		ns

Note: The value left hand two columns show the formula used to calculate the timing minimum or maximum from the oscillator clock period, prescale value and number of wait cycles inserted.
The value right hand two columns show the timing minimum and maximum for an external clock at 24 MHz divided by 2, prescale value of zero and zero wait status.

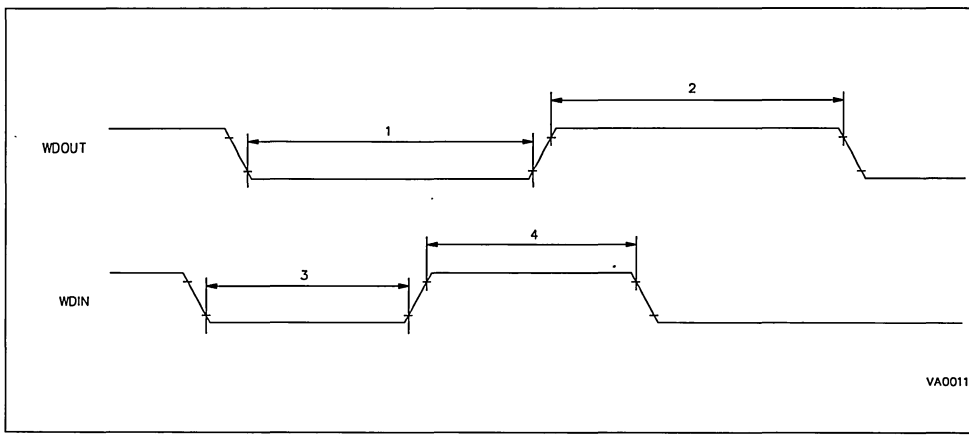
EXTERNAL INTERRUPT TIMING



WATCHDOG TIMING TABLE (V_{DD} = 5V ± 10%, T_A = –40°C to +85°C, Cload = 50pF, INTCLK =12MHz, Output Alternate Function set as Push-pull)

N°	Symbol	Parameter	Value		Unit
			Min.	Max.	
1	TwWDOL	WDOUT Low Pulse Width	620		ns
2	TwWDOH	WDOUT High Pulse Width	620		ns
3	TwWDIL	WDIN Low Pulse Width	350		ns
4	TwWDIH	WDIN High Pulse Width	350		ns

WATCHDOG TIMING

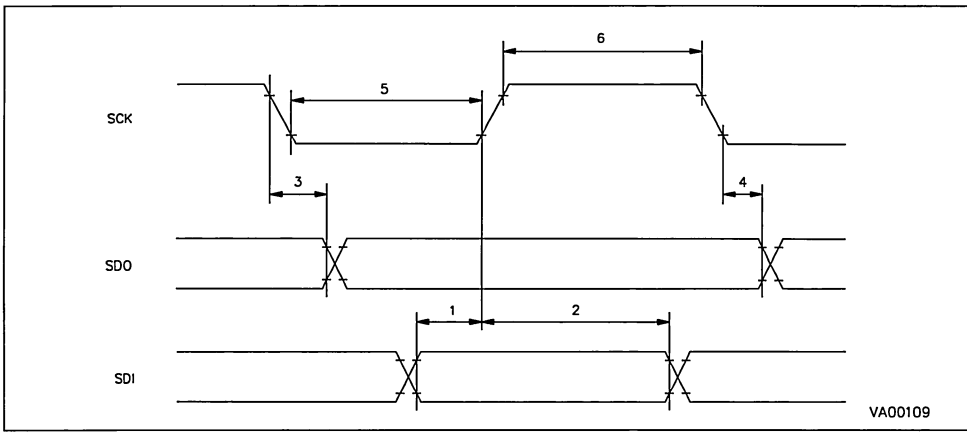


SPI TIMING TABLE (V_{DD} = 5V ± 10%, T_A = –40°C to +85°C, Cload = 50pF, INTCLK = 12MHz, Output Alternate Function set as Push-pull)

N°	Symbol	Parameter	Value		Unit
			Min.	Max.	
1	TsDI	Input Data Set-up Time	100		ns
2	ThDI (1)	Input Data Hold Time	1/2 TpC+100		ns
3	TdOV	SCK to Output Data Valid		100	ns
4	ThDO	Output Data Hold Time	-20		ns
5	TwSKL	SCK Low Pulse Width	300		ns
6	TwSKH	SCK High Pulse Width	300		ns

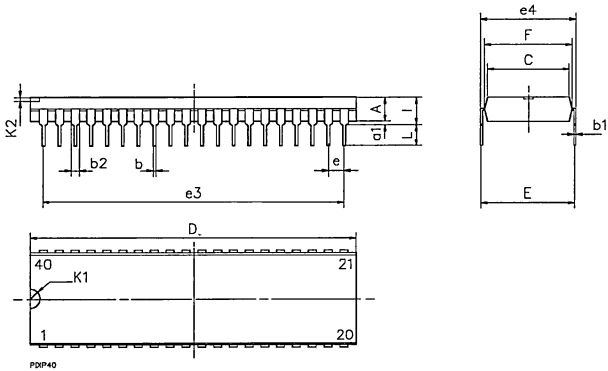
Note: 1. TpC is the Clock period.

SPI TIMING



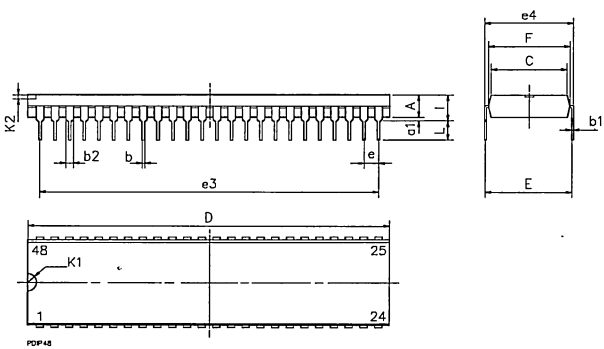
PACKAGE MECHANICAL DATA

Figure 51. 40-Pin Plastic Dual In Line (B)



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A	–	–	–	–	–	–
a1		0.63			0.025	
b		0.45			0.018	
b1	0.23		0.31	0.009		0.012
b2		1.27			0.050	
C	–	–	–	–	–	–
D			52.58			2.070
E	15.20		16.68	0.598		0.656
e		2.54			0.100	
e3		48.26			1.900	
e4	–	–	–	–	–	–
F			14.10			0.555
I		4.45			0.175	
L		3.30			0.129	

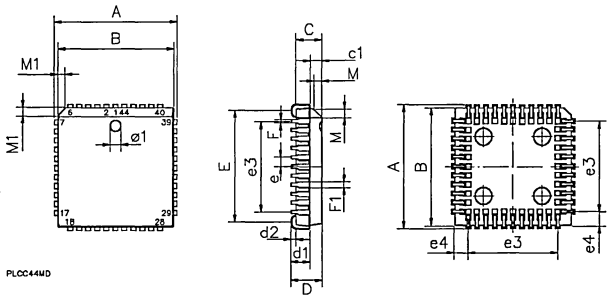
Figure 52. 48-Pin Plastic Dual In Line (B)



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A	–	–	–	–	–	–
a1		0.63			0.024	
b		0.45			0.017	
b1	0.23		0.31	0.009		0.012
b2		1.27			0.050	
C	–	–	–	–	–	–
D			62.74			2.470
E	15.20		16.68	0.598		0.656
e		2.54			0.100	
e3		58.42			2.300	
e4	–	–	–	–	–	–
F			14.10			0.555
I		4.45			0.175	
L		3.30			0.129	

PACKAGE MECHANICAL DATA (Continued)

Figure 53. 44-Lead Plastic Leaded Chip Carrier (C)



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A	17.40		17.65	0.685		0.694
B	16.51		16.65	0.650		0.655
C	3.56		3.70	0.140		0.145
c1	–	–	–	–	–	–
D	4.20		4.57	0.165		0.179
d1	2.59		2.74	0.101		0.107
d2		0.68			0.026	
E	14.99		16.00	0.590		0.629
e		1.27			0.050	
e3		12.70			0.500	
e4			1.98			0.077
F		0.46			0.018	
F1		0.71			0.027	
G			0.101		0.003	
M		1.16			0 045	
M1		1.14			0.044	
Ø1		1.57			0.061	

ORDERING INFORMATION

Sales Type	Frequency	Temperature Range	Package
ST9026B1/XX	24MHz	0°C to +70°C	PDIP48
ST9027B1/XX	24MHz	0C to +70C	PDIP40
ST9028C1/XX	24MHz	0C to +70C	PLCC44
ST9026B6/XX	24MHz	– 40°C to + 85°C	PDIP48
ST9027B6/XX	24MHz	– 40°C to + 85°C	PDIP40
ST9028C6/XX	24MHz	– 40°C to + 85°C	PLCC44

ST9026,ST9027,ST9028 OPTION LIST

Please copy this page (enlarge if possible) and complete ALL sections. Send the form, with the ROM code image required, to your local SGS-THOMSON sales office.

Customer Company : [.....]

Company Address : [.....]

[.....]

Telephone : [.....]

FAX : [.....]

Contact : [.....] Telephone (Direct) : [.....]

Please confirm device required :

Device [ ] (d) Package [ ] (p) Temperature Range [ ] (t)

Special Marking [ ] (y/n) 11 characters for ST9026 [| | | | | | | | | | |] (N)

13 characters for ST9027 [| | | | | | | | | | | | |] (N)

2 x 11 characters for ST9028 [| | | | | | | | | | |] (N)
[| | | | | | | | | | |] (N)

Notes :
(d) 1 = ST9026, 2 = ST9027, 3 = ST9028
(p) B = Dual In Line Plastic, C = Chip Carrier Plastic
(t) 1 = 0 to +70°C, 6 = -40 to +85°C
(N) Available : ASCII 020h - 05Fh

Please consult your local SGS-THOMSON sales office for other marking details

ROMLESS OPTION (consult text)
[ ] YES [ ] NO
If yes, identify required pin (Port.bit)
[ ] P3.7 [ ] P2.0

Code : [ ] EPROM (27128, 27256)
[ ] HEX format files on IBM-PC® compatible disk
filename : [.....]

Confirmation : [ ] Code checked with EPROM device in application

Yearly Quantity forecast : [.....] k units
- for a period of : [.....] years
Preferred Production start dates : [.....] (YY/MM/DD)

Customer Signature : [.....]

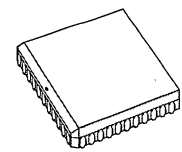
Date : [.....]

SGS-THOMSON MICROELECTRONICS

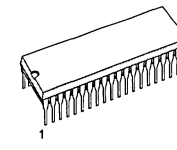
ST90E26,E27,E28
ST90T26,T27,T28

16K EPROM HCMOS MCUs WITH RAM

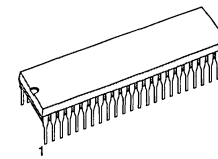
- Single chip microcontroller with 16K bytes of EPROM, 256 bytes of RAM and 256 bytes of register file with 224 general purpose registers available as RAM, accumulators or index pointers.
- 8/16 bit CORE with full feature DMA controller, a powerful interrupt handler and a Standard Serial Peripheral Interface (SPI) handling S-bus, I^2C-bus, IM-bus.
- Up to 7 external interrupts edge-selectable plus 1 non-maskable interrupt.
- 16 bit programmable Timer with 8 bit Prescaler, able to be used as a Watchdog Timer for system integrity.
- A 16 bit Multifunction Timer module, with an 8 bit prescaler and 12 operating modes, allowing simple use for complex waveform generation and measurement, PWM functions and many other system timing operations.
- Full function Serial Communications Interface with 110 to 375000 baud rate generator, asynchronous and byte synchronous capability (fully programmable format) and address/wake-up bit option.
- On-chip DMA channels associated to the Multifunction Timer and the Serial Communications Interface.
- Up to five 8 bit I/O ports with programmable input thresholds and output characteristics. Alternative functions allow the full use of all pins.
- Powerful software development tools, including assembler, linker, C-compiler, archiver, software and hardware emulators.
- Windowed and One Time Programmable EPROM parts available for prototyping and pre-production development phases.
- 48-pin Window Dual in Line Ceramic Multilayer package for ST90E26.
- 40-pin Window Dual in Line Ceramic Multilayer package for ST90E27.
- 44-lead Window Ceramic Leaded Chip Carrier package for ST90E28.
- 48-pin Dual in Line Plastic package for ST90T26.
- 40-pin Dual in Line Plastic package for ST90T27.
- 44-lead Plastic Leaded Chip Carrier package for ST90T28.



PLCC 44

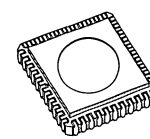


PDIP40

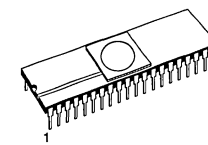


PDIP48

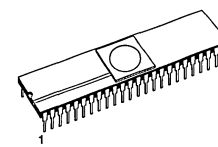
(Ordering Information at the end of the datasheet)



CLCC44W



CDIP40W



CDIP48W

Figure 1. ST90E26,T26 Pin Configuration

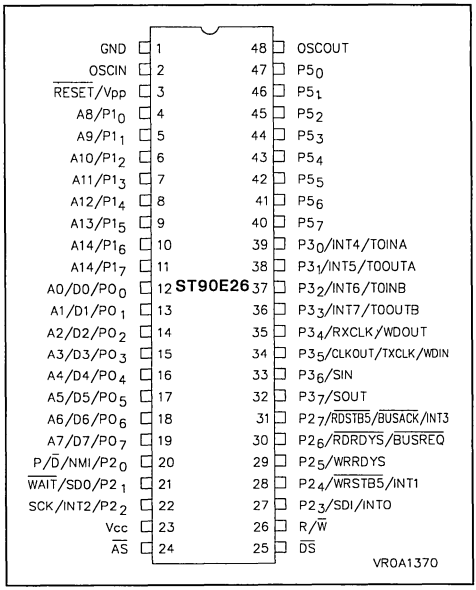


Figure 2. ST90E27,T27 Pin Configuration

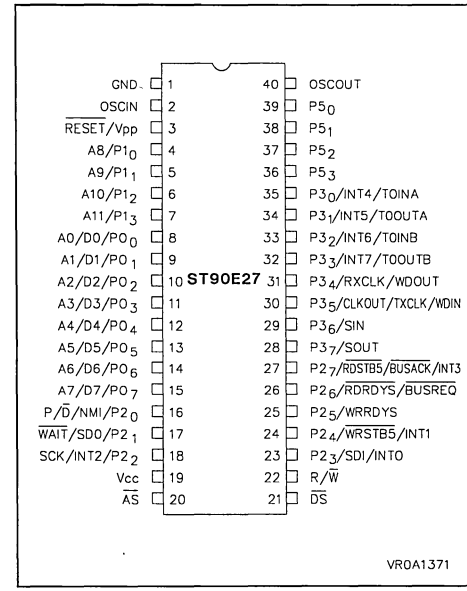


Figure 3. ST90E28,T28 Pin Configuration

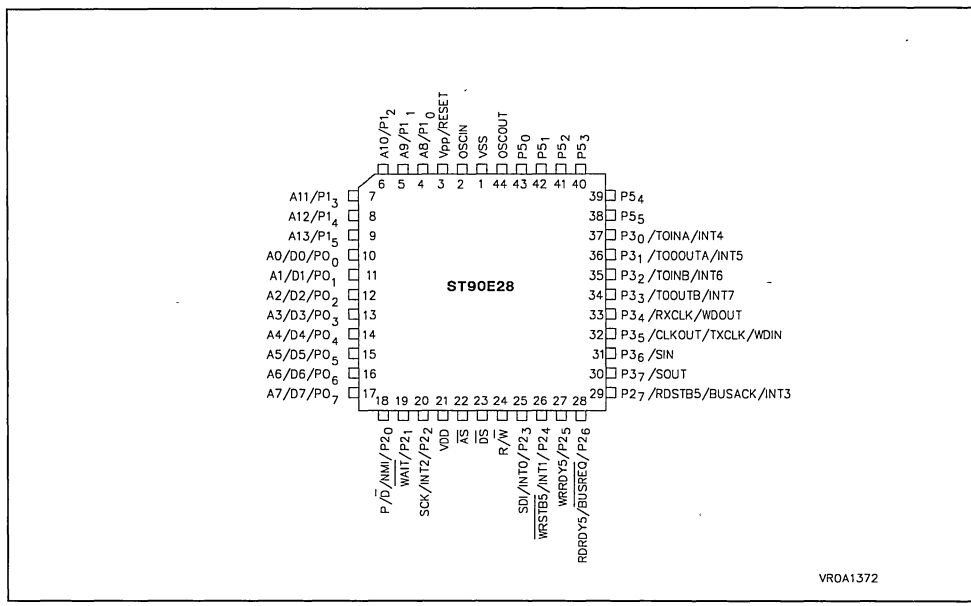
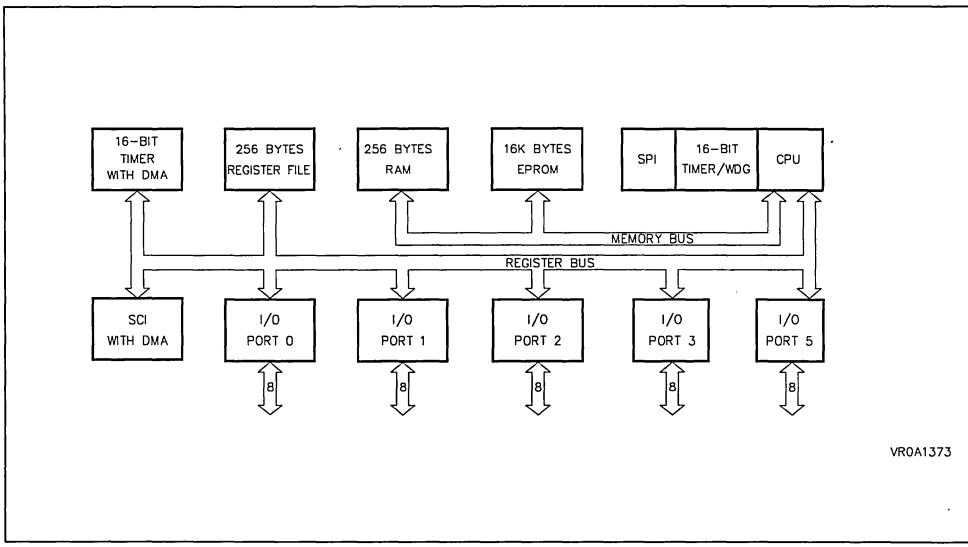


Figure 4. ST90E2X Block Diagram



GENERAL DESCRIPTION

The ST90E26, ST90E27 and ST90E28, ST90T26, ST90T27 and ST90T28 (following mentioned as ST90E2X) are EPROM members of the ST9 family of microcontrollers, in windowed ceramic (E) and plastic OTP (T) packages respectively, completely developed and produced by SGS-THOMSON Microelectronics using a proprietary n-well HCMOS process.

The EPROM parts are fully compatible with their ROM versions and this datasheet will thus provide only information specific to the EPROM based devices.

THE READER IS ASKED TO REFER TO THE DATASHEET OF THE ST9030 ROM-BASED DEVICE FOR FURTHER DETAILS.

The EPROM ST90E2X may be used for the prototyping and pre-production phases of development, and can be configured as: standalone microcontrollers with 16K bytes of on-chip ROM, microcontrollers able to manage up to 120K bytes of external memory, or as parallel processing elements in a system with other processors and peripheral controllers.

A key point of the ST90E2X architecture is its modular approach which allows software commonality with all other members of the ST9 family.

The nucleus of the modular design of the ST90E2X is the advanced Core which includes the Central Processing Unit (CPU), the Register File, a 16 bit Timer/Watchdog with 8 bit Prescaler, a Serial Peripheral Interface supporting S-bus, I^2C-bus and IM-bus Interface, plus two 8 bit I/O ports. The Core has independent memory and register buses allowing a high degree of pipelining to add to the efficiency of the code execution speed of the extensive instruction set.

The powerful I/O capabilities demanded by microcontroller applications are fulfilled by the ST90E2X with up to 40 I/O lines dedicated to digital Input/Output. These lines are grouped into up to five 8 bit I/O Ports and can be configured on a bit basis under software control to provide timing, status signals, an address/data bus for interfacing external memory, timer inputs and outputs, external interrupts and serial or parallel I/O with or without handshake.

Three basic memory spaces are available to support this wide range of configurations: Program Memory (internal and external), Data Memory (internal and external) and the Register File, which includes the control and status registers of the on-chip peripherals.

The 16 bit MultiFunction Timer, with an 8 bit Prescaler and 12 operating modes allows simple use for complex waveform generation and measurement, PWM functions and many other system timing functions by the usage of the two associated DMA channels for each timer.

GENERAL DESCRIPTION (Continued)

Completing the device is a full duplex Serial Communications Interface with an integral 110 to 375000 baud rate generator, asynchronous and byte synchronous capability (fully programmable format) and associated address/wake-up option, plus two DMA channels.

PIN DESCRIPTION

$\overline{AS}$. *Address Strobe (output, active low, 3-state).* Address Strobe is pulsed low once at the beginning of each memory cycle. The rising edge of $\overline{AS}$ indicates that address, Read/Write (R/$\overline{W}$), and Data Memory signals are valid for program or data memory transfers. Under program control, $\overline{AS}$ can be placed in a high-impedance state along with Port 0 and Port 1, Data Strobe ($\overline{DS}$) and R/$\overline{W}$.

$\overline{DS}$. *Data Strobe (output, active low, 3-state).* Data Strobe provides the timing for data movement to or from Port 0 for each memory transfer. During a write cycle, data out is valid at the leading edge of $\overline{DS}$. During a read cycle, Data In must be valid prior to the trailing edge of $\overline{DS}$. When the ST90E2X accesses on-chip memory, $\overline{DS}$ is held high during the whole memory cycle. It can be placed in a high impedance state along with Port 0, Port 1, $\overline{AS}$ and R/$\overline{W}$.

R/$\overline{W}$. *Read/Write (output, 3-state).* Read/Write determines the direction of data transfer for external memory transactions. R/$\overline{W}$ is low when writing to external program or data memory, and high for all other transactions. It can be placed in a high impedance state along with Port 0, Port 1, $\overline{AS}$ and $\overline{DS}$.

$\overline{RESET}$/V_{PP}. *Reset (input, active low) or V_{PP} (input).* The ST9 is initialised by the Reset signal. With the deactivation of $\overline{RESET}$, program execution begins from the Program memory location pointed to by the vector contained in program memory locations 00h and 01h. In the EPROM programming Mode, this pin acts as the programming voltage input VPP.

OSCIN, OSCOUT. *Oscillator (input and output).* These pins connect a parallel-resonant crystal (24MHz maximum), or an external source to the on-chip clock oscillator and buffer. OSCIN is the input of the oscillator inverter and internal clock generator; OSCOUT is the output of the oscillator inverter.

V_{DD}. Main Power Supply Voltage (+5V ±10%)

V_{SS}. Digital Circuit Ground.

P0.0-P0.7, P1.0-P1.7, P2.0-P2.7 P3.0-P3.7, P5.0-P5.7. *I/O Port Lines (Input/Output, TTL or CMOS compatible).* 8 lines grouped into I/O ports of 8 bits, bit programmable under program control as general purpose I/O or as Alternate functions (see next section).

I/O Port Alternate Functions.

Each pin of the I/O ports of the ST90E2X may assume software programmable Alternative Functions as shown in the Pin Configuration Drawings. Due to Bonding options for the packages, some functions may not be present, Table 1 shows the Functions allocated to each I/O Port pins and a summary of packages for which they are available.

PIN DESCRIPTION (Continued)

Table 1. ST90E26X I/O Port Alternate Function Summary

I/O PORT	Name	Function IN/OUT	Alternate Function	Pin Number		
Port.bit				90E26	90E27	90E28
P0.0	A0/D0	I/O	Address/Data bit 0 mux	12	8	10
P0.1	A1/D1	I/O	Address/Data bit 1 mux	13	9	11
P0.2	A2/D2	I/O	Address/Data bit 2 mux	14	10	12
P0.3	A3/D3	I/O	Address/Data bit 3 mux	15	11	13
P0.4	A4/D4	I/O	Address/Data bit 4 mux	16	12	14
P0.5	A5/D5	I/O	Address/Data bit 5 mux	17	13	15
P0.6	A6/D6	I/O	Address/Data bit 6 mux	18	14	16
P0.7	A7/D7	I/O	Address/Data bit 7 mux	19	15	17
P1.0	A8	O	Address bit 8	4	4	4
P1.1	A9	O	Address bit 9	5	5	5
P1.2	A10	O	Address bit 10	6	6	6
P1.3	A11	O	Address bit 11	7	7	7
P1.4	A12	O	Address bit 12	8		8
P1.5	A13	O	Address bit 13	9		9
P1.6	A14	O	Address bit 14	10		
P1.7	A15	O	Address bit 15	11		
P2.0	NMI	I	Non-Maskable Interrupt	20	16	18
P2.0	P/$\overline{D}$	O	Program/Data Space Select	20	16	18
P2.1	SDI	I	SPI Serial Data Out	21	17	19
P2.1	$\overline{WAIT}$	I	External Wait Input	21	17	19
P2.2	INT2	I	External Interrupt 2	22	18	20
P2.2	SCK	O	SPI Serial Clock	22	18	20
P2.3	INT0	I	External Interrupt 0	27	23	25
P2.3	SDO	O	SPI Serial Data In	27	23	25
P2.4	INT1	I	External Interrupt 1	28	24	26
P2.4	$\overline{WRSTB5}$	O	Handshake Write Strobe P5	28	24	26
P2.5	WRRDY5	I	Handshake Write Ready P5	29	25	27
P2.6	RDRDY5	O	Handshake Read Ready P5	30	26	28

PIN DESCRIPTION (Continued)

Table 1. ST90E26X I/O Port Alternate Function Summary (Continued)

I/O PORT	Name	Function IN/OUT	Alternate Function	Pin Number		
Port.bit				90E26	90E27	90E28
P2.6	$\overline{\text{BUSREQ}}$	I	External Bus Request	30	26	28
P2.7	INT3	I	External Interrupt 1	31	27	29
P2.7	$\overline{\text{RDSTB5}}$	I	Handshake Read Strobe P5	31	27	29
P2.7	$\overline{\text{BUSACK}}$	O	External Bus Acknowledge	31	27	29
P3.0	INT4	I	External Interrupt 4	39	35	37
P3.0	T0INA	I	MF Timer 0 Input A	39	35	37
P3.1	INT5	I	External Interrupt 5	38	34	36
P3.1	T0OUTA	O	MF Timer 0 Output A	38	34	36
P3.2	INT6	I	External Interrupt 6	37	33	35
P3.2	T0INB	I	MF Timer 0 Input B	37	33	35
P3.3	INT7	I	External Interrupt 7	36	32	34
P3.3	T0OUTB	O	MF Timer 0 Output B	36	32	34
P3.4	RXCLK	I	SCI Receive Clock Input	35	31	33
P3.4	WDOUT	O	T/WD Output	35	31	33
P3.5	CLKOUT	O	SCI Byte Sync Clock Output	34	30	32
P3.5	TXCLK	I	SCI Transmit Clock Input	34	30	32
P3.5	WDIN	I	T/WD Input	34	30	32
P3.6	SIN	I	SCI Serial Input	33	29	31
P3.7	SOUT	O	SCI Serial Output	32	28	32
P5.0		I/O	I/O Handshake Port 5	47	39	43
P5.1		I/O	I/O Handshake Port 5	46	38	42
P5.2		I/O	I/O Handshake Port 5	45	37	41
P5.3		I/O	I/O Handshake Port 5	44	36	40
P5.4		I/O	I/O Handshake Port 5	43		39
P5.5		I/O	I/O Handshake Port 5	42		38
P5.6		I/O	I/O Handshake Port 5	41		
P5.7		I/O	I/O Handshake Port 5	40		

MEMORY

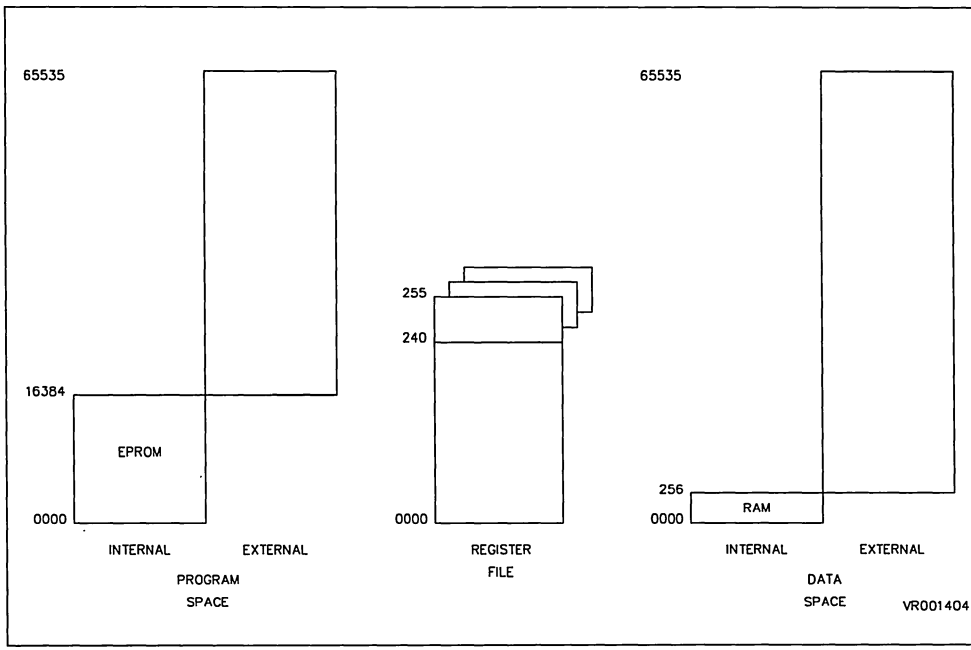
The memory of the ST90E2X is functionally divided into two areas, the Register File and Memory. The Memory is divided into two spaces, each having a maximum of 65,536 bytes. The two memory spaces are separated by function, one space for Program code, the other for Data. The ST90E2X 16K bytes of on-chip ROM memory is selected at memory addresses 0 through 3FFFh (hexadecimal) in the PROGRAM space, while the ST90T2X OTP version has the top 64 bytes of the program space reserved by SGS-THOMSON for testing purposes. The 256 bytes of on-chip RAM memory is selected at memory addresses 0 through 0FFh in the DATA space.

External memory may be addressed using the multiplexed address and data buses (Alternate Functions of Ports 0 and 1). At addresses greater than the first 16K of program space, the ST90E2X executes external memory cycles for instruction fetches. External Data Memory may be decoded by using the P/$\overline{D}$ Alternate Function output. The on-chip general purpose (GP) Registers may be used as RAM memory in addition to the on-chip RAM.

EPROM PROGRAMMING

The 16384 bytes of EPROM memory of the ST90E2X (16320 for the ST90T2X) may be programmed by using the EPROM Programming Boards (EPB) available from SGS-THOMSON.

Figure 5. Memory Spaces



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	– 0.3 to 7.0	V
AV_{DD}, AV_{SS}	Analog Supply Voltage	$V_{SS} \le AV_{SS} < AV_{DD} \le V_{DD}$	V
V_I	Input Voltage	V_{SS} – 0.3 to V_{DD} +0.3	V
V_O	Output Voltage	V_{SS} – 0.3 to V_{DD} +0.3	V
V_{PP}	Input Voltage on V_{PP} Pin	– 0.3 to 13.5	V
T_{STG}	Storage Temperature	– 55 to + 150	°C

Note: Stresses above those listed as "absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value		Unit
		Min.	Max.	
T_A	Operating Temperature	– 40	85	°C
V_{DD}	Operating Supply Voltage	4.5	5.5	V
f_{OSCE}	External Oscillator Frequency		24	MHz
f_{OSCI}	Internal Oscillator Frequency		12	MHz

DC ELECTRICAL CHARACTERISTICS

(V_{DD} = 5V ± 10% T_A = – 40 °C to + 85°C, unless otherwise specified)

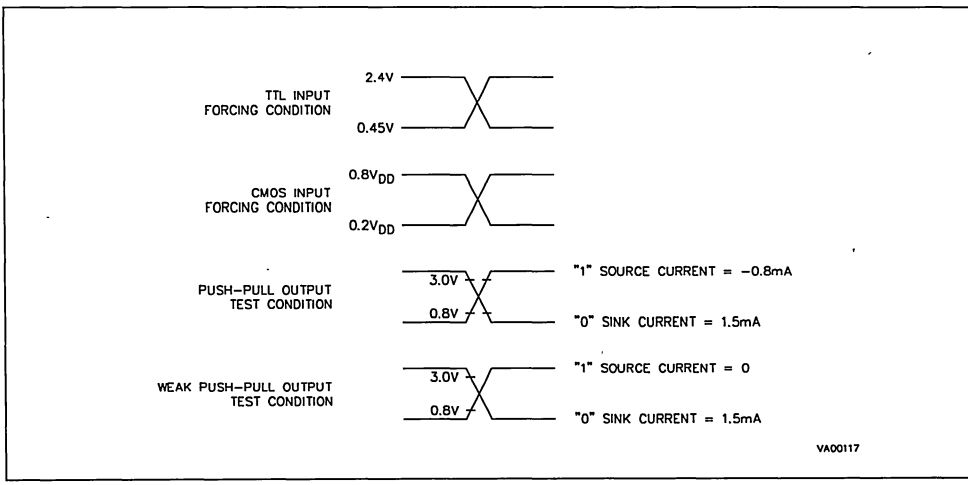
Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
V_{IHCK}	Clock Input High Level	External Clock	0.7 V_{DD}		V_{DD} + 0.3	V
V_{ILCK}	Clock Input Low Level	External Clock	– 0.3		0.3 V_{DD}	V
V_{IH}	Input High Level	TTL	2.0		V_{DD} + 0.3	V
		CMOS	0.7 V_{DD}		VDD + 0.3	V
V_{IL}	Input Low Level	TTL	– 0.3		0.8	V
		CMOS	– 0.3		0.3 V_{DD}	V
V_{IHRS}	Reset Input High Level		0.7 V_{DD}		V_{DD} + 0.3	V
V_{ILRS}	Reset Input Low Level		–0.3		0.3 V_{DD}	V
V_{HYRS}	Reset Input Hysteresis		0.3		1.5	V
V_{OH}	Output High Level	Push Pull, Iload = – 0.8mA	V_{DD} – 0.8			V
V_{OL}	Output Low Level	Push Pull or Open Drain, Iload = – 1.6mA			0.4	V
I_{WPU}	Weak Pull-up Current	Bidirectional Weak Pull-up, V_{OL} = 0V	– 80	– 200	– 420	µA

DC ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
I_{APU}	Active Pull-up Current, for INT0 and INT7 only	$V_{IN} < 0.8V$	– 80	– 200	– 420	µA
I_{LKIO}	I/O Pin Input Leakage	Input/Tri-State, $0V < V_{IN} < V_{DD}$	– 10		+ 10	µA
I_{LKRS}	Reset Pin Input Leakage	$0V < V_{IN} < V_{DD}$	– 30		+ 30	µA
I_{LKAD}	A/D Pin Input Leakage	Alternate Function, Open Drain, $0V < V_{IN} < V_{DD}$	– 3		+ 3	µA
I_{LKAP}	Active Pull-up Input Leakage	$0V < V_{IN} < 0.8V$	– 10		+ 10	µA
I_{LKOS}	OSCIN Pin Input Leakage	$0V < V_{IN} < V_{DD}$	– 10		+ 10	µA
I_{DD}	Run Mode Current	24MHz, Note 1		32	70	mA
		4MHz, Note 1		6	12	mA
I_{DP2}	Run Mode Current Prescale by 2	24MHz, Note 1		19	40	mA
		4MHz, Note 1		4	8	mA
I_{WFI}	WFI Mode Current	24MHz, Note 1		9	18	mA
		4MHz, Note 1		2.5	5	mA
I_{HALT}	HALT Mode Current	24MHz, Note 1			100	µA
V_{PP}	EPROM Programming Voltage		12.2	12.5	12.8	V
I_{PP}	EPROM Programming Current				30	mA

Note: 1. All I/O Ports are configured in Bidirectional Weak Pull-up Mode with no DC load, External Clock pin (OSCIN) is driven by square wave external clock. No peripheral working. External interface not active (Internal Program Execution).

DC TEST CONDITIONS



AC ELECTRICAL CHARACTERISTICS

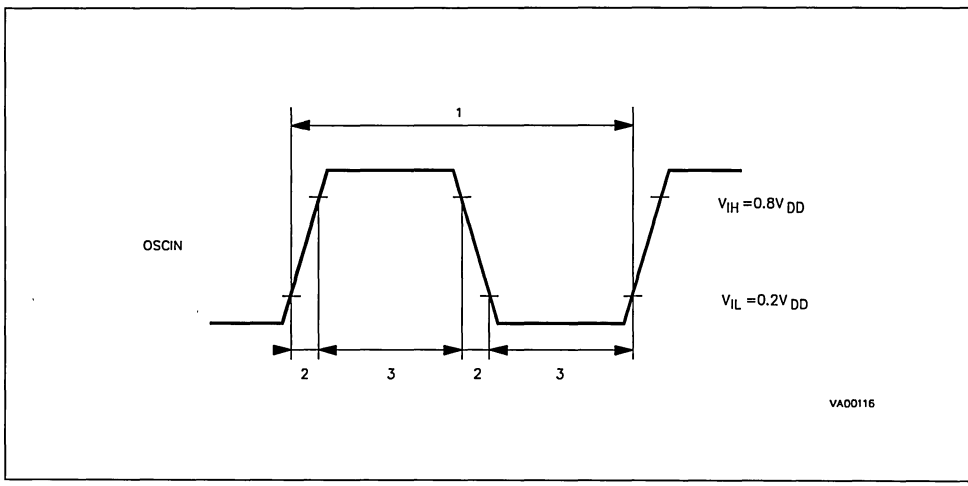
CLOCK TIMING TABLE

(V_{DD} = 5V ± 10%, T_A = − 40°C to + 85°C, unless otherwise specified)

N°	Symbol	Parameter	Value		Unit	Note
			Min.	Max.		
1	TpC	OSCIN Clock Period	41.5		ns	a
			83		ns	b
2	TrC, TfC	OSCIN Rise and Fall Time		12	ns	
3	TwCL, TwCH	OSCIN Low and High Width	25	12	ns	a
			38		ns	b

Notes:
a. Clock divided by 2 internally (MODER.DIV2=1)
b. Clock not divided by 2 internally (MODER.DIV2=0)

CLOCK TIMING



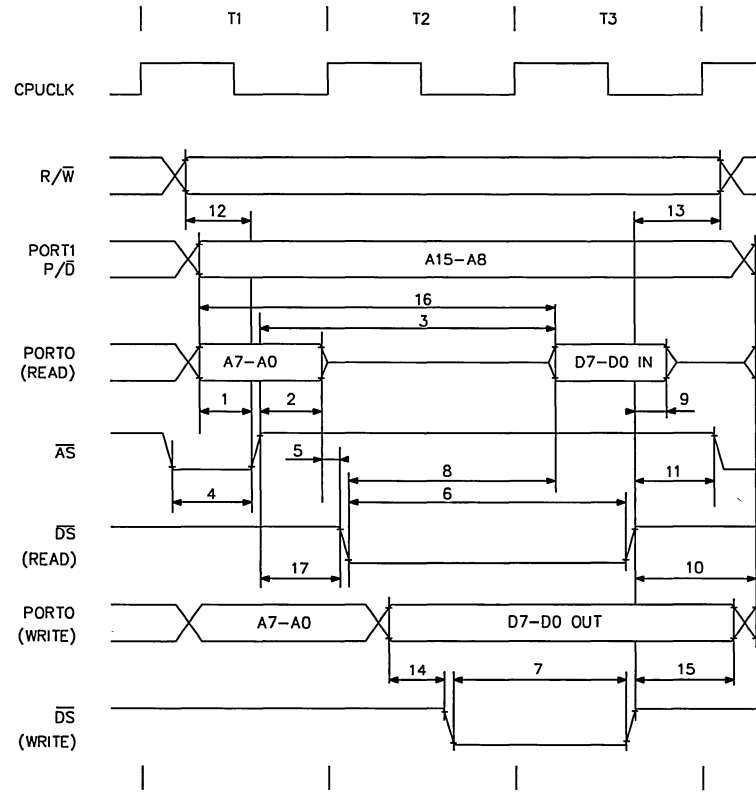
EXTERNAL BUS TIMING TABLE (V_{DD} = 5V ± 10%, T_A = – 40 °C to + 85 °C, Cload = 50pF, CPUCLK = 12MHz, unless otherwise specified)

N°	Symbol	Parameter	Value (Note)				Unit
			OSCIN Divided By 2	OSCIN Not Divided By 2	Min.	Max.	
1	TsA (AS)	Address Set-up Time before $\overline{AS}$ ↑	TpC (2P+1) –22	TwCH+PTpC –18	20		ns
2	ThAS (A)	Address Hold Time after $\overline{AS}$ ↑	TpC –17	TwCL –13	25		ns
3	TdAS (DR)	$\overline{AS}$ ↑ to Data Available (read)	TpC (4P+2W+4) –52	TpC (2P+W+2) –51		115	ns
4	TwAS	$\overline{AS}$ Low Pulse Width	TpC (2P+1) –7	TwCH+PTpC –3	35		ns
5	TdAz (DS)	Address Float to $\overline{DS}$ ↓	0	0	0		ns
6	TwDSR	$\overline{DS}$ Low Pulse Width (read)	TpC (4P+2W+3) –20	TwCH+TpC (2P+W+1) – 16	105		ns
7	TwDSW	$\overline{DS}$ Low Pulse Width (write)	TpC (2P+2W+2) –13	TpC (P+W+1) –13	70		ns
8	TdDSR (DR)	$\overline{DS}$ ↓ to Data Valid Delay (read)	TpC (4P+2W-3) –50	TwCH+TpC(2P+W+1) – 46		75	ns
9	ThDR (DS)	Data to $\overline{DS}$ ↑ Hold Time (read)	0	0	0		ns
10	TdDS (A)	$\overline{DS}$ ↑ to Address Active Delay	TpC –7	TwCL –3	35		ns
11	TdDS (AS)	$\overline{DS}$ ↑ to $\overline{AS}$ ↓ Delay	TpC –18	TwCL –14	24		ns
12	TsR/W (AS)	R/$\overline{W}$ Set-up Time before $\overline{AS}$ ↑	TpC (2P+1) –22	TwCH+PTpC –18	20		ns
13	TdDSR (R/W)	$\overline{DS}$ ↑ to R/$\overline{W}$ and Address Not Valid Delay	TpC –9	TwCL –5	33		ns
14	TdDW (DSW)	Write Data Valid to $\overline{DS}$ ↓ Delay (write)	TpC (2P+1) –32	TwCH+PTpC –28	10		ns
15	ThDS (DW)	Data Hold Time after DS ↑ (write)	TpC –9	TwCL –5	33		ns
16	TdA (DR)	Address Valid to Data Valid Delay (read)	TpC (6P+2W+5) –68	TwCH+TpC (3P+W+2) – 64		140	ns
17	TdAs (DS)	$\overline{AS}$ ↑ to $\overline{DS}$ ↓ Delay	TpC –18	TwCL –14	24		ns

Note: The value left hand two columns show the formula used to calculate the timing minimum or maximum from the oscillator clock period, prescale value and number of wait cycles inserted.
The value right hand two columns show the timing minimum and maximum for an external clock at 24 MHz divided by 2, prescaler value of zero and zero wait status.

Legend:
P = Clock Prescaling Value
W = Wait Cycles
TpC = OSCIN Period
TwCH = High Level OSCIN half period
TwCL = Low Level OSCIN half period

EXTERNAL BUS TIMING

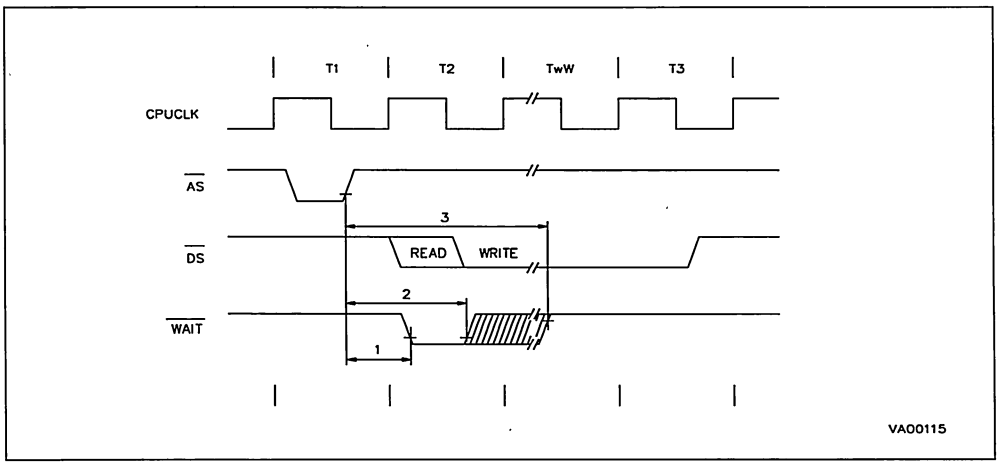


EXTERNAL WAIT TIMING TABLE (V_{DD} = 5V ± 10%, T_A = –40°C to +85°C, Cload = 50pF, INTCLK = 12MHz, Push-pull output configuration, unless otherwise specified)

N°	Symbol	Parameter	Value (Note)				Unit
			OSCIN Divided By 2	OSCIN Not Divided By 2	Min.	Max.	
1	TdAS (WAIT)	$\overline{AS}$ ↑ to $\overline{WAIT}$ ↓ Delay	2(P+1)TpC –29	(P+1)TpC –29		40	ns
2	TdAS (WAIT)	$\overline{AS}$ ↑ to $\overline{WAIT}$ ↑ Minimum Delay	2(P+W+1)TpC –4	(P+W+1)TpC –4	80		ns
3	TdAS (WAIT)	$\overline{AS}$ ↑ to $\overline{WAIT}$ ↑ Maximum Delay	2(P+W+1)TpC –29	(P+W+1)TpC –29		83W+40	ns

Note: The value left hand two columns show the formula used to calculate the timing minimum or maximum from the oscillator clock period, prescale value and number of wait cycles inserted.
The value right hand two columns show the timing minimum and maximum for an external clock at 24 MHz divided by 2, prescale value of zero and zero wait status.

EXTERNAL WAIT TIMING

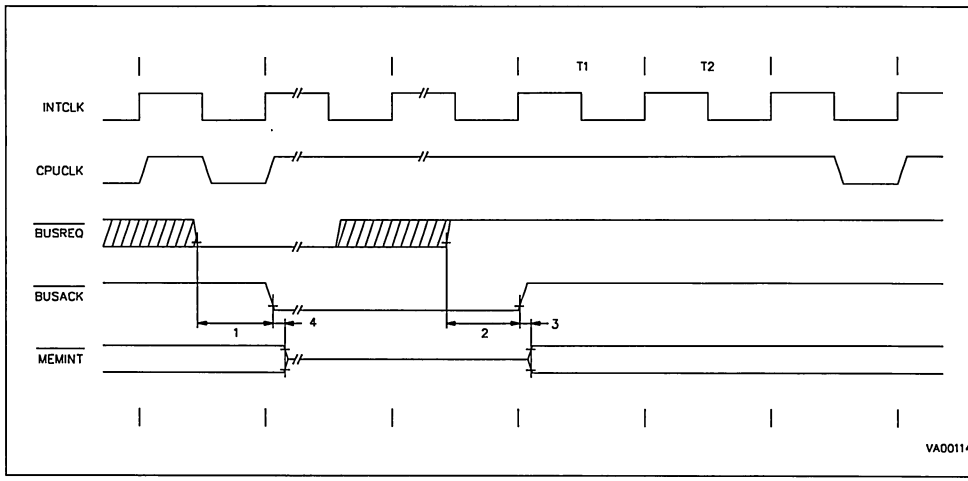


BUS REQUEST/ACKNOWLEDGE TIMING TABLE (V_{DD} = 5V ± 10%, T_A = −40°C to +85°C, Cload = 50pF, INTCLK = 12MHz, Push-pull output configuration, unless otherwise specified)

N°	Symbol	Parameter	Value (Note)				Unit
			OSCIN Divided By 2	OSCIN Not Divided By 2	Min.	Max.	
1	TdBR (BACK)	$\overline{BREQ}$ ↓ to $\overline{BUSACK}$ ↓	TpC+8	TwCL+12	50		ns
			TpC(6P+2W+7)+65	TpC(3P+W+3)+TwCL+65		360	ns
2	TdBR (BACK)	$\overline{BREQ}$ ↑ to $\overline{BUSACK}$ ↑	3TpC+60	TpC+TwCL+60		185	ns
3	TdBACK (BREL)	$\overline{BUSACK}$ ↓ to Bus Release	20	20		20	ns
4	TdBACK (BACT)	$\overline{BUSACK}$ ↑ to Bus Active	20	20		20	ns

Note: The value left hand two columns show the formula used to calculate the timing minimum or maximum from the oscillator clock period, prescale value and number of wait cycles inserted.
The value right hand two columns show the timing minimum and maximum for an external clock at 24 MHz divided by 2, prescale value of zero and zero wait status.

BUS REQUEST/ACKNOWLEDGE TIMING



Note : MEMINT = group of memory interface signals : $\overline{AS}$, $\overline{DS}$, R/$\overline{W}$, P00-P07, P10-P17.

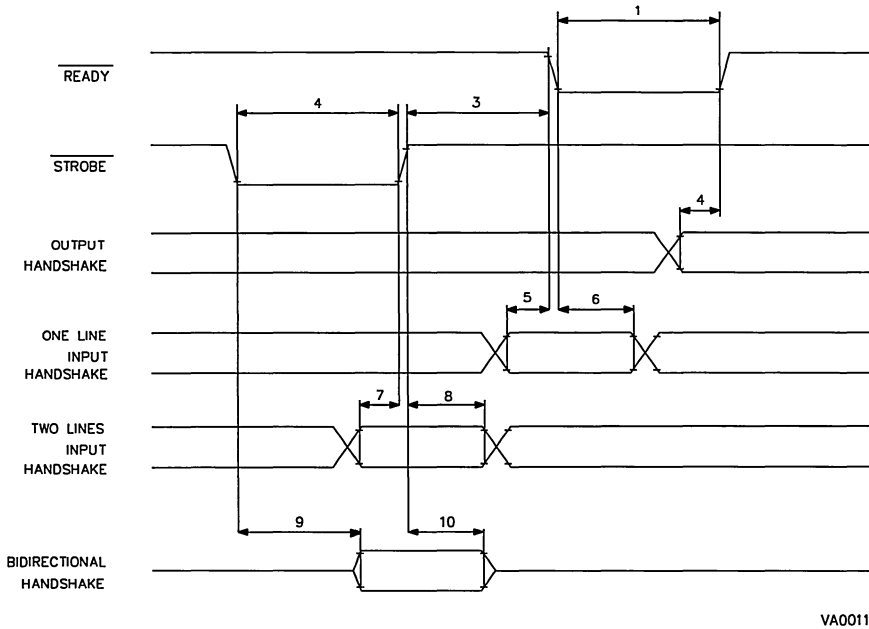
HANDSHAKE TIMING TABLE (V_{DD} = 5V ± 10%, T_A = –40°C to +85°C, Cload = 50pF, INTCLK = 12MHz, Push-pull output configuration, unless otherwise specified)

N°	Symbol	Parameter	Value (Note)				Min.	Max.	Unit
			OSCIN Divided By 2		OSCIN Not Divided By 2				
			Min.	Max.	Min.	Max.			
1	TwRDY	RDRDY, WRRDY Pulse Width in One Line Handshake	2TpC (P+W+1) –18		TpC (P+W+1) –18		65		ns
2	TwSTB	$\overline{RDSTB}$, $\overline{WRSTB}$ Pulse Width	2TpC+12		TpC+12		95		ns
3	TdST (RDY)	$\overline{RDSTB}$, or $\overline{WRSTB}$ ↑ to RDRDY or WRRDY ↓		TpC+45		(TpC-TwCL) +45		87	ns
4	TsPD (RDY)	Port Data to RDRDY ↑ Set-up Time	(2P+2W+1) TpC –25		TwCH+(W+P) TpC –25		16		ns
5	TsPD (RDY)	Port Data to WRRDY ↓ Set-up Time in One Line Handshake	43		43		43		ns
6	ThPD (RDY)	Port Data to WRRDY ↓ Hold Time in One Line Handshake	0		0		0		ns
7	TsPD (STB)	Port Data to $\overline{WRSTB}$ ↑ Set-up Time	10		10		10		ns
8	ThPD (STB)	Port Data to WRSTB ↑ Hold Time	25		25		25		ns
9	TdSTB (PD)	$\overline{RDSTBD}$ ↑ to Port Data Delay Time in Bidirectional Hand-shake		35		35		35	ns
10	TdSTB (PHZ)	$\overline{RDSTB}$ ↑ to Port High-Z Delay Time in Bidirectional Hand-shake		25		25		25	ns

Note: The value left hand two columns show the formula used to calculate the timing minimum or maximum from the oscillator clock period, prescale value and number of wait cycles inserted.
The value right hand two columns show the timing minimum and maximum for an external clock at 24 MHz divided by 2, prescaler value of zero and zero wait status.

Legend:
P = Clock Prescaling Value (R235.4,3,2)
W = Programmable Wait Cycles (R252.2.1.0/5,4,3) + External Wait Cycles

HANDSHAKE TIMING

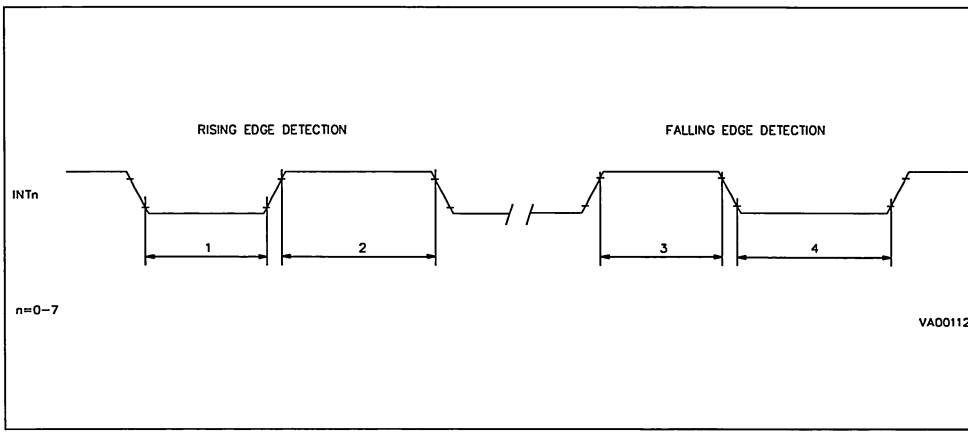


EXTERNAL INTERRUPT TIMING TABLE (V_{DD} = 5V ± 10%, T_A = –40°C to +85°C, Cload = 50pF, INTCLK = 12MHz, Push-pull output configuration, unless otherwise specified)

N°	Symbol	Parameter	Value (Note)				Unit
			OSCIN Divided By 2 Min.	OSCIN Not Divided By 2 Min.	Min.	Max.	
1	TwLR	Low Level Minimum Pulse Width in Rising Edge Mode	2TpC+12	TpC+12	95		ns
2	TwHR	High Level Minimum Pulse Width in Rising Edge Mode	2TpC+12	TpC+12	95		ns
3	TwHF	High Level Minimum Pulse Width in Falling Edge Mode	2TpC+12	TpC+12	95		ns
4	TwLF	Low Level Minimum Pulse Width in Falling Edge Mode	2TpC+12	TpC+12	95		ns

Note: The value left hand two columns show the formula used to calculate the timing minimum or maximum from the oscillator clock period, prescale value and number of wait cycles inserted.
The value right hand two columns show the timing minimum and maximum for an external clock at 24 MHz divided by 2, prescale value of zero and zero wait status.

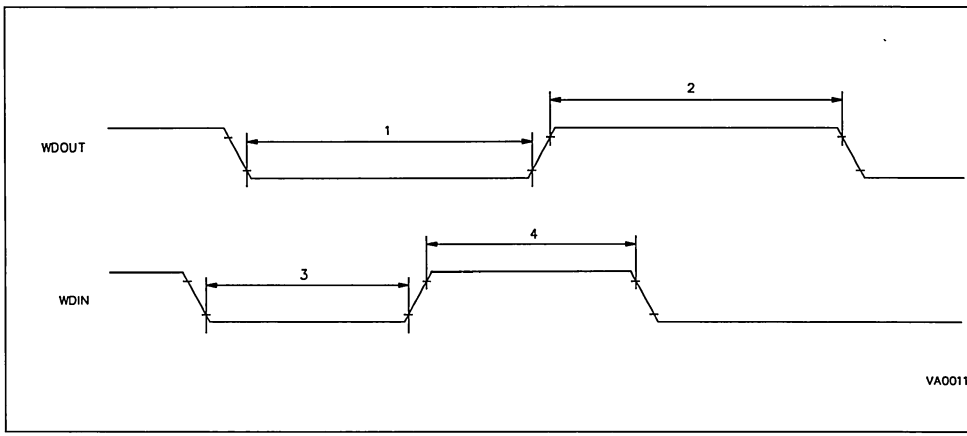
EXTERNAL INTERRUPT TIMING



WATCHDOG TIMING TABLE (V_{DD} = 5V ± 10%, T_A = –40°C to +85°C, Cload = 50pF, INTCLK = 12MHz, Output Alternate Function set as Push-pull)

N°	Symbol	Parameter	Value		Unit
			Min.	Max.	
1	TwWDOL	WDOUT Low Pulse Width	620		ns
2	TwWDOH	WDOUT High Pulse Width	620		ns
3	TwWDIL	WDIN Low Pulse Width	350		ns
4	TwWDIH	WDIN High Pulse Width	350		ns

WATCHDOG TIMING

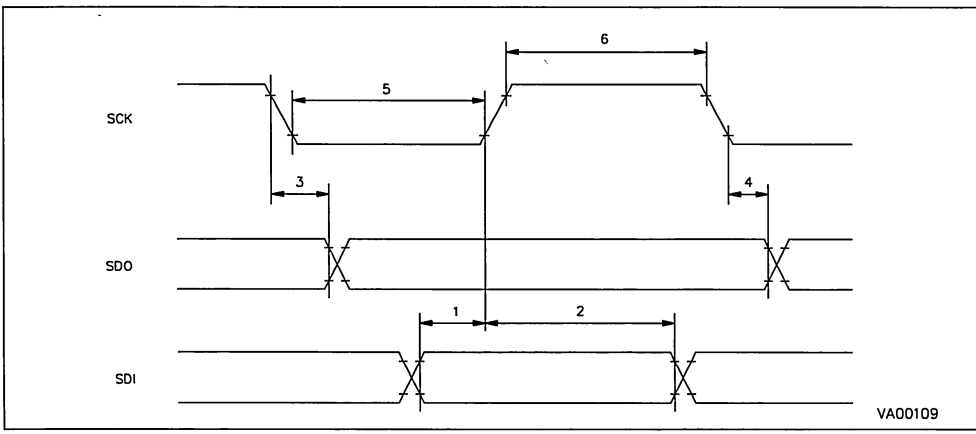


SPI TIMING TABLE (V_{DD} = 5V ± 10%, T_A = –40°C to +85°C, Cload = 50pF, INTCLK = 12MHz, Output Alternate Function set as Push-pull)

N°	Symbol	Parameter	Value		Unit
			Min.	Max.	
1	TsDI	Input Data Set-up Time	100		ns
2	ThDI (1)	Input Data Hold Time	1/2 TpC+100		ns
3	TdOV	SCK to Output Data Valid		100	ns
4	ThDO	Output Data Hold Time	-20		ns
5	TwSKL	SCK Low Pulse Width	300		ns
6	TwSKH	SCK High Pulse Width	300		ns

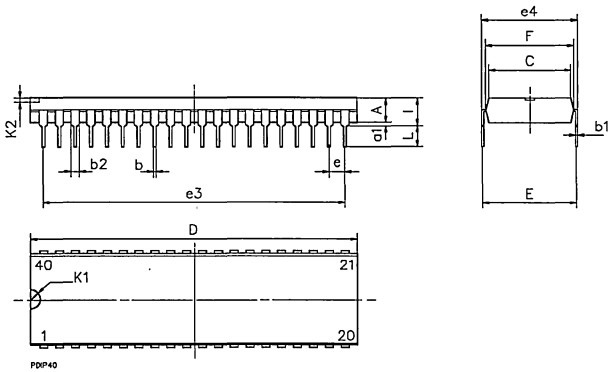
Note: 1. TpC is the Clock period.

SPI TIMING



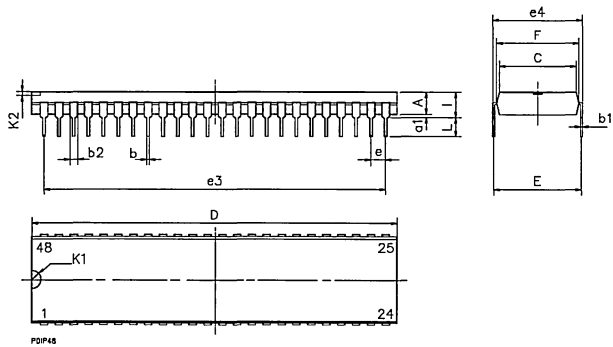
PACKAGES MECHANICAL DATA

Figure 51. 40-Pin Plastic Dual In Line (B)



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A	–	–	–	–	–	–
a1		0.63			0.025	
b		0.45			0.018	
b1	0.23		0.31	0.009		0.012
b2		1.27			0.050	
C	–	–	–	–	–	–
D			52.58			2.070
E	15.20		16.68	0.598		0.656
e		2.54			0.100	
e3		48.26			1.900	
e4	–	–	–	–	–	–
F			14.10			0.555
I		4.45			0.175	
L		3.30			0.129	

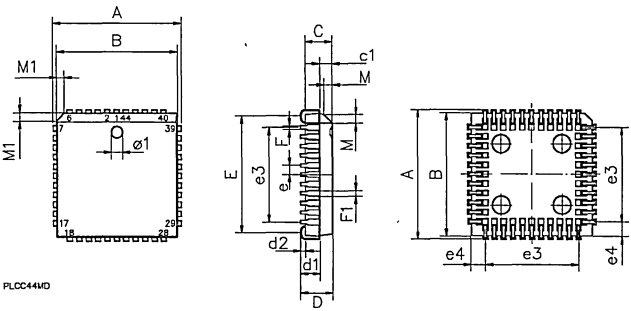
Figure 52. 48-Pin Plastic Dual In LIne (B)



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A	–	–	–	–	–	–
a1		0.63			0.024	
b		0.45			0.017	
b1	0.23		0 31	0.009		0.012
b2		1.27			0.050	
C	–	–	–	–	–	–
D			62.74			2.470
E	15.20		16.68	0.598		0.656
e		2.54			0.100	
e3		58 42			2.300	
e4	–	–	–	–	–	–
F			14.10			0.555
I		4.45			0.175	
L		3.30			0.129	

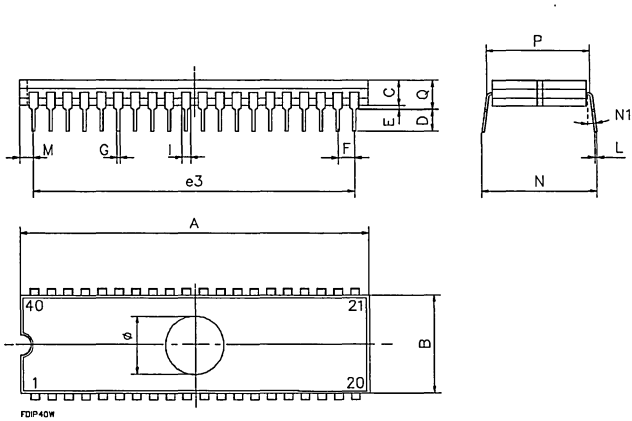
PACKAGE MECHANICAL DATA (Continued)

Figure 53. 44-Lead Plastic Leaded Chip Carrier (C)



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A	17.40		17.65	0.685		0.694
B	16.51		16.65	0.650		0.655
C	3.56		3.70	0.140		0.145
c1	–	–	–	–	–	–
D	4.20		4.57	0.165		0.179
d1	2.59		2.74	0.101		0.107
d2		0.68			0.026	
E	14.99		16.00	0.590		0.629
e		1.27			0.050	
e3		12.70			0.500	
e4			1.98			0.077
F		0.46			0.018	
F1		0.71			0.027	
G			0.101		0.003	
M		1.16			0.045	
M1		1.14			0.044	
Ø1		1.57			0.061	

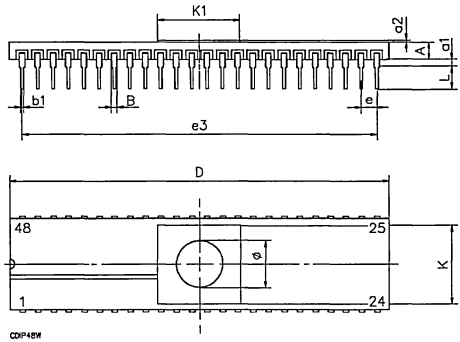
Figure 54. 40-Lead WindowCeramic Dual in Line



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A			53.40			2.102
B	14.50		14.90	0.571		0.587
C	3.90		5.08	0.154		0.200
D	3.40			0.134		
E	0.50		1.78	0.020		0.070
e3		48.26			1.900	
F	2.29		2.79	0.090		0.110
G	0.40		0.55	0.016		0.022
I	1.27		1.52	0.050		0.060
L	0.22		0.31	0.009		0.012
M	1.52		2.49	0.060		0.098
N	–	–	–	–	–	–
N1	0°		10°	0°		10°
P	15.40		15.80	0.606		0.622
Q			5.71			0.225
Ø	9.45		9.85	0.372		0.388

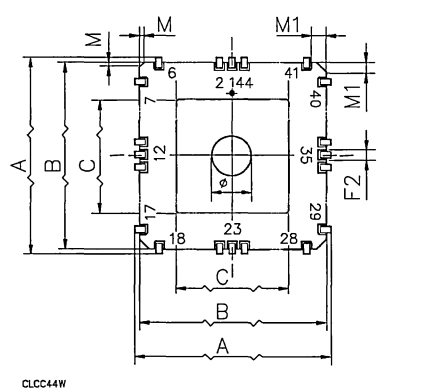
PACKAGE MECHANICAL DATA (Continued)

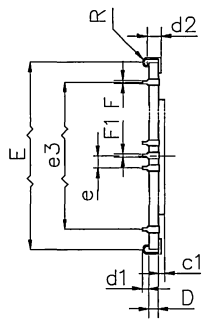
Figure 55. 48-Lead Window Ceramic Dual In Line



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A	–	–	–	–	–	
a1		1.27			0.050	
a2			1.30			0.051
B		1.02			0.040	
b1		0.45			0.017	
b2		0.25			0.010	
C		3.50			0.137	
D			61.59			2.424
E		15.24			0.600	
e		2.54			0.100	
e3		58.42			2.300	
F			15.34			0.604
L		3.30			0.130	
K		13.46			0.530	
K1		13.46			0.530	
Ø		7.62			0.300	

Figure 56. 44-Lead Window Ceramic Leaded Chip Carrier





Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A	17.27		17.78	0.670		0.700
B	16.33		16.81	0.643		0.662
C			12.01			0.473
C1			1.30			0.051
D	1.82		2.23	0.071		0.088
d1	–	–	–	–	–	–
d2	–	–	–	–	–	–
E	–	–	–	–	–	–
e		1.27				0.050
e3	–	–	–	–	–	–
F		0.43			0.017	
F1		0.76			0.030	
F2	–	–	–	–	–	–
M	–	–	–	–	–	–
M1	–	–	–	–	–	–
R		0.76			0.030	
Ø		7.62			0.300	

ORDERING INFORMATION

Sales Type	Frequency	Temperature Range	Package
ST90E26D6	24MHz	– 40°C to + 85°C	CDIP48-W
ST90E27D6	24MHz	0°C to + 85°C	CDIP40-W
ST90T28L6	24MHz	– 40°C to + 85°C	CLCC44-W
ST90E26D1	24MHz	0°C to + 70°C	CDIP48-W
ST90E27D1	24MHz	0°C to +70°C	CDIP40-W
ST90E28L1	24MHz	0°C to +70°C	CLCC-W
ST90T26B6	24MHz	– 40°C to + 85°C	PDIP48
ST90T27B6	24MHz	– 40°C to + 85°C	PDIP40
ST90T28C6	24MHz	– 40°C to + 85°C	PLCC44
ST90T26B1	24MHz	0°C to +70°C	PDIP48
ST90T27B1	24MHz	0°C to +70°C	PDIP40
ST90T28C1	24MHz	0°C to +70°C	PLCC44

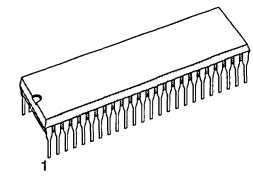
SGS-THOMSON MICROELECTRONICS

ST90R26

ROMLESS HCMOS MCU WITH RAM AND A/D CONVERTER

ADVANCE DATA

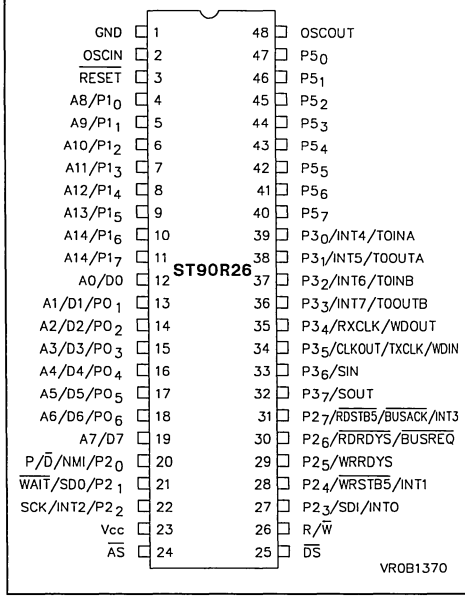
- Single chip microcontroller with 256 bytes of RAM and 256 bytes of Register File with 224 general purpose registers available as RAM, accumulators or index pointers.
- Romless to allow maximum external memory flexibility in development and production phases.
- 8/16 bit CORE with full feature DMA controller, a powerful interrupt handler and a Standard Serial Peripheral Interface (SPI) handling S-BUS, I^2C-bus, IM-bus and Standard Serial Peripheral Interfaces.
- Up to 8 external interrupts edge-selectable plus 1 non-maskable interrupt.
- 16 bit programmable Timer with 8 bit Prescaler, able to be used as a Watchdog Timer for system integrity.
- A 16 bit Multifunction Timer module, with an 8 bit prescaler and 13 operating modes, allowing simple use for complex waveform generation and measurement, PWM functions and many other system timing operations.
- Full function Serial Communications Interface with 110 to 375000 baud rate generator, asynchronous and byte synchronous capability (fully programmable format) and address/wake-up bit option.
- On-chip DMA channels associated to the Multifunction Timer and the Serial Communications Interface.
- Up to four 8 bit I/O ports with programmable input thresholds and output characteristics. Alternative functions allow the full use of all pins.
- Powerful software development tools, including assembler, linker, C-compiler, archiver, software and hardware emulators.
- Compatible with ST9026, 16k ROM devices (also available in windowed and One Time Programmable EPROM packages).
- 48-lead Plastic Dual in Line package for ST90R26.



PDIP48

(Ordering Information at the end of the datasheet)

Figure 1. ST90R26 Pin Configuration



GENERAL DESCRIPTION

The ST90R26 is a ROMLESS member of the ST9 family of microcontrollers, completely developed and produced by SGS-THOMSON Microelectronics using a proprietary n-well HCMOS process.

The ROMLESS part may be used for the prototyping and pre-production phases of development, and offers the maximum in program flexibility in production systems.

The ST90R26 is fully compatible with the ST9026 ROM version and this datasheet will thus provide only information specific to the ROMLESS device.

THE READER IS ASKED TO REFER TO THE DATASHEET OF THE ST9026 ROM-BASED DEVICE FOR FURTHER DETAILS.

The ROMLESS ST90R26 can be configured as a microcontroller able to manage up to 128K bytes of external memory, or as a parallel processing element in a system with other processors and peripheral controllers.

A key point of the ST90R26 architecture is related to its modular approach which allows software commonality with all other members of the ST9 family.

The nucleus of the modular design of the ST90R26 is the advanced Core which includes the Central Processing Unit (CPU), the Register File, a 16 bit Timer/Watchdog with 8 bit Prescaler, a Serial Peripheral Interface supporting S-BUS, I^2C-bus and IM-bus Interface, plus two 8 bit I/O ports. The Core has independent memory and register buses allowing a high degree of pipelining to add to the efficiency of the code execution speed of the extensive instruction set.

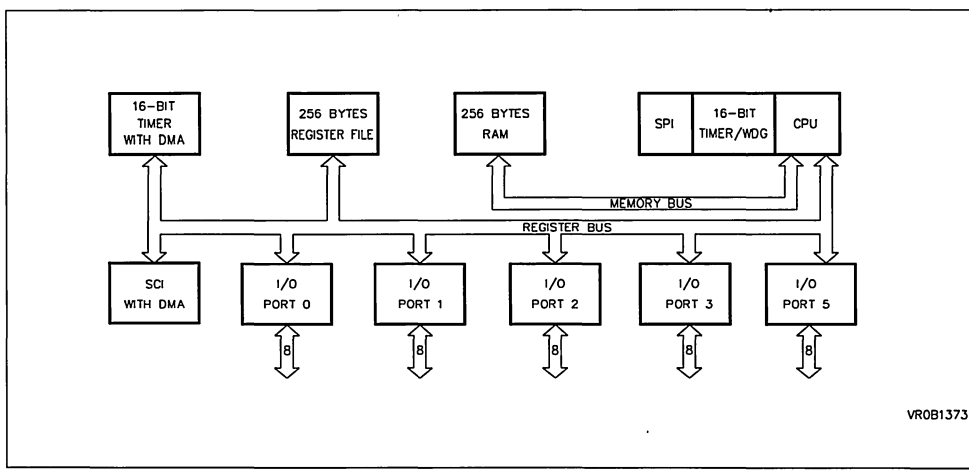
The powerful I/O capabilities demanded by microcontroller applications are fulfilled by the ST90R26 with up to 32 I/O lines dedicated to digital Input/Output. These lines are grouped into up to four 8 bit I/O Ports and can be configured on a bit basis under software control to provide timing and status signals, address lines, timer inputs and outputs, analog inputs, external interrupts and serial or parallel I/O with or without handshake.

Three memory spaces are available: Program Memory (external), Data Memory (internal and external) and the Register File, which includes the control and status registers of the on-chip peripherals.

The 16 bit MultiFunction Timer, with an 8 bit Prescaler and 12 operating modes allow simple use for complex waveform generation and measurement, PWM functions and many other system timing functions by the usage of the two associated DMA channels.

Completing the device is a full duplex Serial Communications Interface with an integral 110 to 375000 baud rate generator, asynchronous and byte synchronous capability (fully programmable format) and associated address/wake-up option, plus two DMA channels.

Figure 2. ST90R26 Block Diagram



PIN DESCRIPTION

$\overline{AS}$. *Address Strobe (output, active low, 3-state).* Address Strobe is pulsed low once at the beginning of each memory cycle. The rising edge of $\overline{AS}$ indicates that address, Read/Write (R/$\overline{W}$), and Data Memory signals are valid for program or data memory transfers. Under program control, $\overline{AS}$ can be placed in a high-impedance state along with Port 0 and Port 1, Data Strobe ($\overline{DS}$) and R/$\overline{W}$.

$\overline{DS}$. *Data Strobe (output, active low, 3-state).* Data Strobe provides the timing for data movement to or from Port 0 for each memory transfer. During a write cycle, data out is valid at the leading edge of $\overline{DS}$. During a read cycle, Data In must be valid prior to the trailing edge of $\overline{DS}$. When the ST90R26 accesses on-chip Data memory, $\overline{DS}$ is held high during the whole memory cycle. It can be placed in a high impedance state along with Port 0, Port 1, $\overline{AS}$ and R/$\overline{W}$.

R/$\overline{W}$. *Read/Write (output, 3-state).* Read/Write determines the direction of data transfer for memory transactions. R/$\overline{W}$ is low when writing to program or data memory, and high for all other transactions. It can be placed in a high impedance state along with Port 0, Port 1, $\overline{AS}$ and $\overline{DS}$.

$\overline{RESET}$. *Reset (input, active low).* The ST9 is initialised by the Reset signal. With the deactivation of $\overline{RESET}$, program execution begins from the Program memory location pointed to by the vector contained in program memory locations 00h and 01h.

OSCIN, OSCOUT. *Oscillator (input and output).* These pins connect a parallel-resonant crystal (24MHz maximum), or an external source to the on-chip clock oscillator and buffer. OSCIN is the input of the oscillator inverter and internal clock generator; OSCOUT is the output of the oscillator inverter.

V_{DD}. Main Power Supply Voltage (5V±10%)

V_{SS}. Digital Circuit Ground.

AD0-AD7, (P0.0-P0.7) *Address/Data Lines (Input/Output, TTL or CMOS compatible).* 8 lines providing a multiplexed address and data bus, under control of the $\overline{AS}$ and $\overline{DS}$ timing signals.

P1.0-P1.7, P2.0-P2.7 P3.0-P3.7, P5.0-P5.7 *I/O Port Lines (Input/Output, TTL or CMOS compatible).* 32 lines grouped into I/O ports of 8 bits, bit programmable under program control as general purpose I/O or as Alternate functions (see next section).

I/O Port Alternate Functions.

Each pin of the I/O ports of the ST90R26 may assume software programmable Alternative Functions as shown in the Pin Configuration Drawings. Figure 1.2 shows the Functions allocated to each I/O Port pins.

PIN DESCRIPTION (Continued)

Table 1. ST90R26 I/O Port Alternate Function Summary

I/O PORT Port.bit	Name	Function IN/OUT	Alternate Function	Pin Number
P0.0	A0/D0	I/O	Address/Data bit 0 mux	12
P0.1	A1/D1	I/O	Address/Data bit 1 mux	13
P0.2	A2/D2	I/O	Address/Data bit 2 mux	14
P0.3	A3/D3	I/O	Address/Data bit 3 mux	15
P0.4	A4/D4	I/O	Address/Data bit 4 mux	16
P0.5	A5/D5	I/O	Address/Data bit 5 mux	17
P0.6	A6/D6	I/O	Address/Data bit 6 mux	18
P0.7	A7/D7	I/O	Address/Data bit 7 mux	19
P1.0	A8	O	Address bit 8	4
P1.1	A9	O	Address bit 9	5
P1.2	A10	O	Address bit 10	6
P1.3	A11	O	Address bit 11	7
P1.4	A12	O	Address bit 12	8
P1.5	A13	O	Address bit 13	9
P1.6	A14	O	Address bit 14	10
P1.7	A15	O	Address bit 15	11
P2.0	NMI	I	Non-Maskable Interrupt	20
P2.0	P/$\overline{D}$	O	Program/Data Space Select	20
P2.1	SDI	I	SPI Serial Data Out	21
P2.1	$\overline{WAIT}$	I	External Wait Input	21
P2.2	INT2	I	External Interrupt 2	22
P2.2	SCK	O	SPI Serial Clock	22
P2.3	INT0	I	External Interrupt 0	27
P2.3	SDO	O	SPI Serial Data In	27
P2.4	INT1	I	External Interrupt 1	28
P2.4	$\overline{WRSTB5}$	O	Handshake Write Strobe P5	28
P2.5	WRRDY5	I	Handshake Write Ready P5	29
P2.6	RDRDY5	O	Handshake Read Ready P5	30
P2.6	$\overline{BUSREQ}$	I	External Bus Request	30
P2.7	INT3	I	External Interrupt 1	31

PIN DESCRIPTION (Continued)

Table 1. ST90R26 I/O Port Alternate Function Summary (Continued)

I/O PORT Port.bit	Name	Function IN/OUT	Alternate Function	Pin Number
P2.7	$\overline{\text{RDSTB5}}$	I	Handshake Read Strobe P5	31
P2.7	$\overline{\text{BUSACK}}$	O	External Bus Acknowledge	31
P3.0	INT4	I	External Interrupt 4	39
P3.0	T0INA	I	MF Timer 0 Input A	39
P3.1	INT5	I	External Interrupt 5	38
P3.1	T0OUTA	O	MF Timer 0 Output A	38
P3.2	INT6	I	External Interrupt 6	37
P3.2	T0INB	I	MF Timer 0 Input B	37
P3.3	INT7	I	External Interrupt 7	36
P3.3	T0OUTB	O	MF Timer 0 Output B	36
P3.4	RXCLK	I	SCI Receive Clock Input	35
P3.4	WDOUT	O	T/WD Output	35
P3.5	CLKOUT	O	SCI Byte Sync Clock Output	34
P3.5	TXCLK	I	SCI Transmit Clock Input	34
P3.5	WDIN	I	T/WD Input	34
P3.6	SIN	I	SCI Serial Input	33
P3.7	SOUT	O	SCI Serial Output	32
P5.0		I/O	I/O Handshake Port 5	47
P5.1		I/O	I/O Handshake Port 5	46
P5.2		I/O	I/O Handshake Port 5	45
P5.3		I/O	I/O Handshake Port 5	44
P5.4		I/O	I/O Handshake Port 5	43
P5.5		I/O	I/O Handshake Port 5	42
P5.6		I/O	I/O Handshake Port 5	41
P5.7		I/O	I/O Handshake Port 5	40

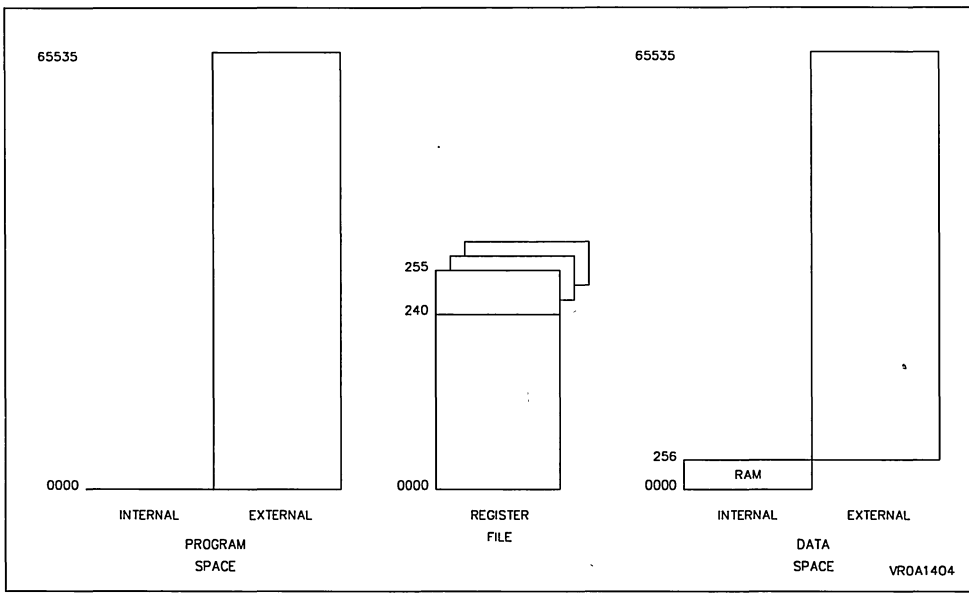
MEMORY

The memory of the ST90R26 is functionally divided into two areas, the Register File and Memory. The Memory may optionally be divided into two spaces, each having a maximum of 65,536 bytes. The two memory spaces are separated by function, one space for Program code, the other for Data. The ST90R26 addresses all program memory in the external PROGRAM space. The 256 bytes of on-chip RAM memory is selected at memory addresses 0 through 0FFh in the DATA space.

The External Memory spaces are addressed using the multiplexed address and data buses on Ports 0 and 1. Additional Data Memory may be decoded externally by using the P/$\overline{D}$ Alternate Function output. The on-chip general purpose (GP) Registers may be used as RAM memory.

MEMORY (Continued)

Figure 3. Memory Spaces



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	– 0.3 to 7.0	V
AV_{DD}, AV_{SS}	Analog Supply Voltage	$V_{SS} \le AV_{SS} < AV_{DD} \le V_{DD}$	V
V_I	Input Voltage	V_{SS} – 0.3 to V_{DD} +0.3	V
V_O	Output Voltage	V_{SS} – 0.3 to V_{DD} +0.3	V
T_{STG}	Storage Temperature	– 55 to + 150	°C

Note: Stresses above those listed as "absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value		Unit
		Min.	Max.	
T_A	Operating Temperature	– 40	85	°C
V_{DD}	Operating Supply Voltage	4.5	5.5	V
f_{OSCE}	External Oscillator Frequency		24	MHz
f_{OSCI}	Internal Oscillator Frequency		12	MHz

DC ELECTRICAL CHARACTERISTICS

(V_{DD} = 5V ± 10% T_A = – 40 °C to + 85°C, unless otherwise specified)

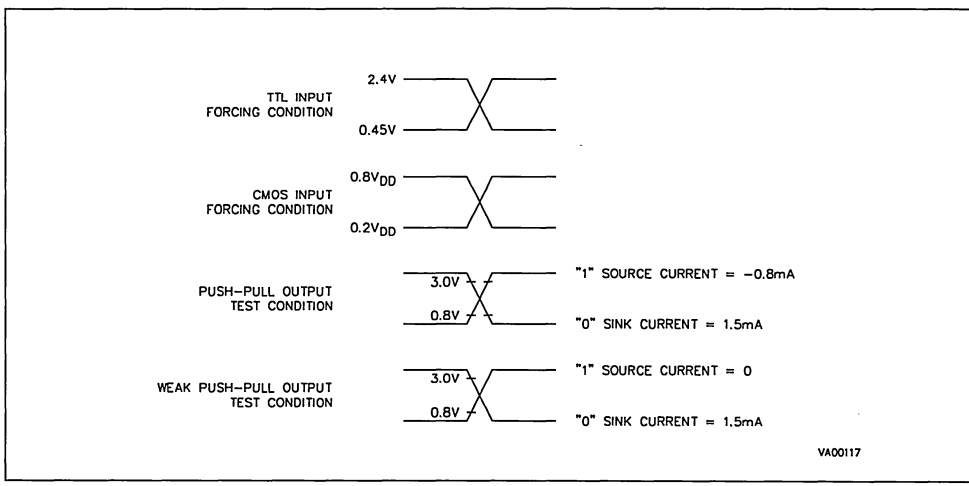
Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
V_{IHCK}	Clock Input High Level	External Clock	0.7 V_{DD}		V_{DD} + 0.3	V
V_{ILCK}	Clock Input Low Level	External Clock	– 0.3		0.3 V_{DD}	V
V_{IH}	Input High Level	TTL	2.0		V_{DD} + 0.3	V
		CMOS	0.7 V_{DD}		VDD + 0.3	V
V_{IL}	Input Low Level	TTL	– 0.3		0.8	V
		CMOS	– 0.3		0.3 V_{DD}	V
V_{IHRS}	Reset Input High Level		0.7 V_{DD}		V_{DD} + 0.3	V
V_{ILRS}	Reset Input Low Level		–0.3		0.3 V_{DD}	V
V_{HYRS}	Reset Input Hysteresis		0.3		1.5	V
V_{OH}	Output High Level	Push Pull, Iload = – 0.8mA	V_{DD} – 0.8			V
V_{OL}	Output Low Level	Push Pull or Open Drain, Iload = – 1.6mA			0.4	V

DC ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
I_{WPU}	Weak Pull-up Current	Bidirectional Weak Pull-up, V_{OL} = 0V	– 80	– 200	– 420	µA
I_{APU}	Active Pull-up Current, for INT0 and INT7 only	V_{IN} < 0.8V	– 80	– 200	– 420	µA
I_{LKIO}	I/O Pin Input Leakage	Input/Tri-State, 0V < V_{IN} < V_{DD}	– 10		+ 10	µA
I_{LKRS}	Reset Pin Input Leakage	0V < V_{IN} < V_{DD}	– 30		+ 30	µA
I_{LKAD}	A/D Pin Input Leakage	Alternate Function, Open Drain, 0V < V_{IN} < V_{DD}	– 3		+ 3	µA
I_{LKAP}	Active Pull-up Input Leakage	0V < V_{IN} < 0.8V	– 10		+ 10	µA
I_{LKOS}	OSCIN Pin Input Leakage	0V < V_{IN} < V_{DD}	– 10		+ 10	µA
I_{DD}	Run Mode Current	24MHz, Note 1		32	70	mA
		4MHz, Note 1		6	12	mA
I_{DP2}	Run Mode Current Prescale by 2	24MHz, Note 1		19	40	mA
		4MHz, Note 1		4	8	mA
I_{WFI}	WFI Mode Current	24MHz, Note 1		9	18	mA
		4MHz, Note 1		2.5	5	mA
I_{HALT}	HALT Mode Current	24MHz, Note 1			100	µA

Note:
1. All I/O Ports are configured in Bidirectional Weak Pull-up Mode with no DC load, External Clock pin (OSCIN) is driven by square wave external clock. No peripheral working. External interface not active (Internal Program Execution).

DC TEST CONDITIONS



AC ELECTRICAL CHARACTERISTICS

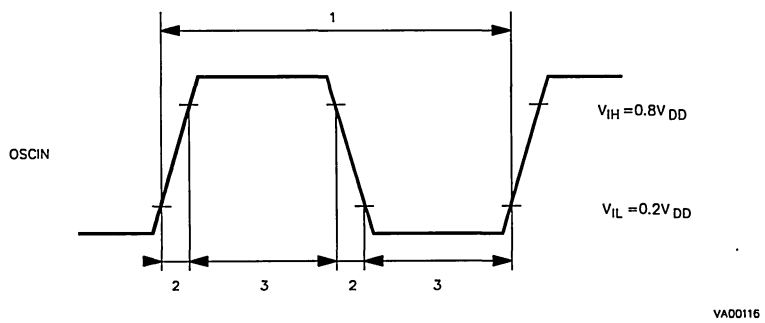
CLOCK TIMING TABLE

(V_{DD} = 5V ± 10%, T_A = − 40°C to + 85°C, unless otherwise specified)

N°	Symbol	Parameter	Value		Unit	Note
			Min.	Max.		
1	TpC	OSCIN Clock Period	41.5		ns	1
			83		ns	2
2	TrC, TfC	OSCIN Rise and Fall Time		12	ns	
3	TwCL, TwCH	OSCIN Low and High Width	25	12	ns	1
			38		ns	2

Notes:
1. Clock divided by 2 internally (MODER.DIV2=1)
2. Clock not divided by 2 internally (MODER.DIV2=0)

CLOCK TIMING



EXTERNAL BUS TIMING TABLE

(V_{DD} = 5V ± 10%, T_A = – 40 °C to + 85 °C, Cload = 50pF, CPUCLK = 12MHz, unless otherwise specified)

N°	Symbol	Parameter	Value (Note)				Unit
			OSCIN Divided By 2	OSCIN Not Divided By 2	Min.	Max.	
1	TsA (AS)	Address Set-up Time before $\overline{AS}$ ↑	TpC (2P+1) –22	TWCH+PTpC –18	20		ns
2	ThAS (A)	Address Hold Time after $\overline{AS}$↑	TpC –17	TwCL –13	25		ns
3	TdAS (DR)	$\overline{AS}$ ↑ to Data Available (read)	TpC (4P+2W+4) –52	TpC (2P+W+2) –51		115	ns
4	TwAS	$\overline{AS}$ Low Pulse Width	TpC (2P+1) –7	TwCH+PTpC –3	35		ns
5	TdAz (DS)	Address Float to $\overline{DS}$ ↓	0	0	0		ns
6	TwDSR	$\overline{DS}$ Low Pulse Width (read)	TpC (4P+2W+3) –20	TwCH+TpC (2P+W+1) –16	105		ns
7	TwDSW	$\overline{DS}$ Low Pulse Width (write)	TpC (2P+2W+2) –13	TpC (P+W+1) –13	70		ns
8	TdDSR (DR)	$\overline{DS}$ ↓ to Data Valid Delay (read)	TpC (4P+2W-3) –50	TwCH+TpC(2P+W+1) – 46		75	ns
9	ThDR (DS)	Data to $\overline{DS}$ ↑ Hold Time (read)	0	0	0		ns
10	TdDS (A)	$\overline{DS}$ ↑ to Address Active Delay	TpC –7	TwCL –3	35		ns
11	TdDS (AS)	$\overline{DS}$ ↑ to $\overline{AS}$ ↓ Delay	TpC –18	TwCL –14	24		ns
12	TsR/W (AS)	R/$\overline{W}$ Set-up Time before $\overline{AS}$↑	TpC (2P+1) –22	TwCH+PTpC –18	20		ns
13	TdDSR (R/W)	$\overline{DS}$ ↑ to R/$\overline{W}$ and Address Not Valid Delay	TpC –9	TwCL –5	33		ns
14	TdDW (DSW)	Write Data Valid to $\overline{DS}$ ↓ Delay (write)	TpC (2P+1) –32	TwCH+PTpC –28	10		ns
15	ThDS (DW)	Data Hold Time after DS ↑ (write)	TpC –9	TwCL –5	33		ns
16	TdA (DR)	Address Valid to Data Valid Delay (read)	TpC (6P+2W+5) –68	TwCH+TpC (3P+W+2) –64		140	ns
17	TdAs (DS)	$\overline{AS}$ ↑ to $\overline{DS}$ ↓ Delay	TpC –18	TwCL –14	24		ns

Note: The value left hand two columns show the formula used to calculate the timing minimum or maximum from the oscillator clock period, prescale value and number of wait cycles inserted.
The value right hand two columns show the timing minimum and maximum for an external clock at 24 MHz divided by 2, prescaler value of zero and zero wait status.

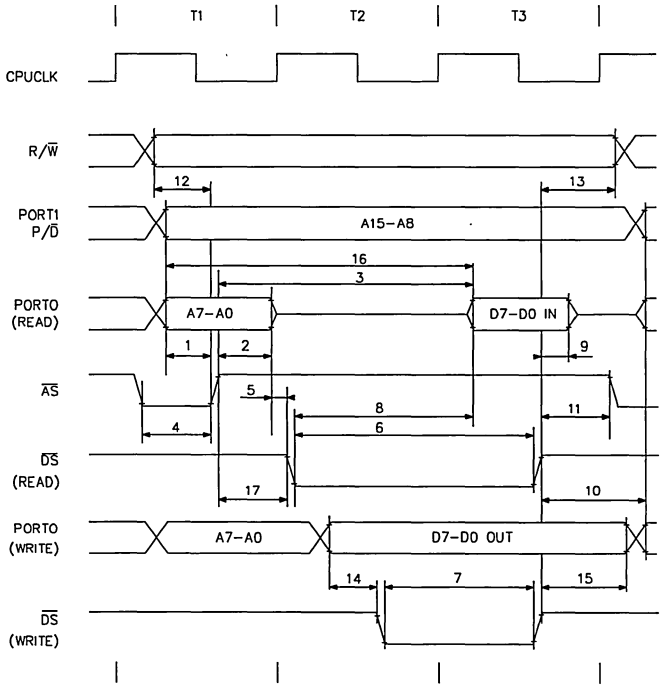
Legend:
P = Clock Prescaling Value
W = Wait Cycles
TpC = OSCIN Period
TwCH = High Level OSCIN half period
TwCL = Low Level OSCIN half period

EXTERNAL WAIT TIMING TABLE (V_{DD} = 5V ± 10%, T_A = –40°C to +85°C, Cload = 50pF, INTCLK = 12MHz, Push-pull output configuration, unless otherwise specified)

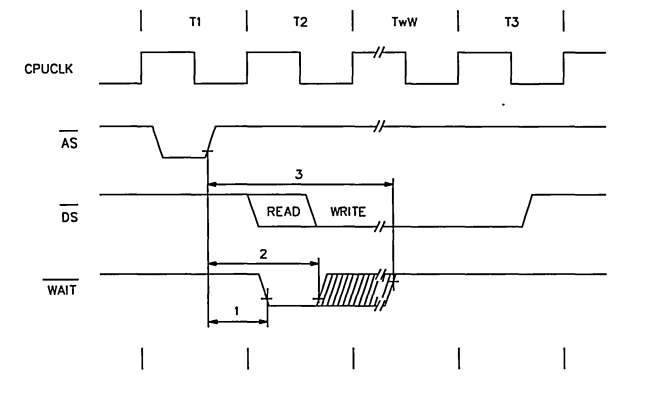
N°	Symbol	Parameter	Value (Note)				Unit
			OSCIN Divided By 2	OSCIN Not Divided By 2	Min.	Max.	
1	TdAS (WAIT)	$\overline{AS}$ ↑ to $\overline{WAIT}$ ↓ Delay	2(P+1)TpC –29	(P+1)TpC –29		40	ns
2	TdAS (WAIT)	$\overline{AS}$ ↑ to $\overline{WAIT}$ ↑ Minimum Delay	2(P+W+1)TpC –4	(P+W+1)TpC –4	80		ns
3	TdAS (WAIT)	$\overline{AS}$ ↑ to $\overline{WAIT}$ ↑ Maximum Delay	2(P+W+1)TpC – 29	(P+W+1)TpC –29		83W+40	ns

Note: The value left hand two columns show the formula used to calculate the timing minimum or maximum from the oscillator clock period, prescale value and number of wait cycles inserted.
The value right hand two columns show the timing minimum and maximum for an external clock at 24 MHz divided by 2, prescale value of zero and zero wait status.

EXTERNAL BUS TIMING



EXTERNAL WAIT TIMING

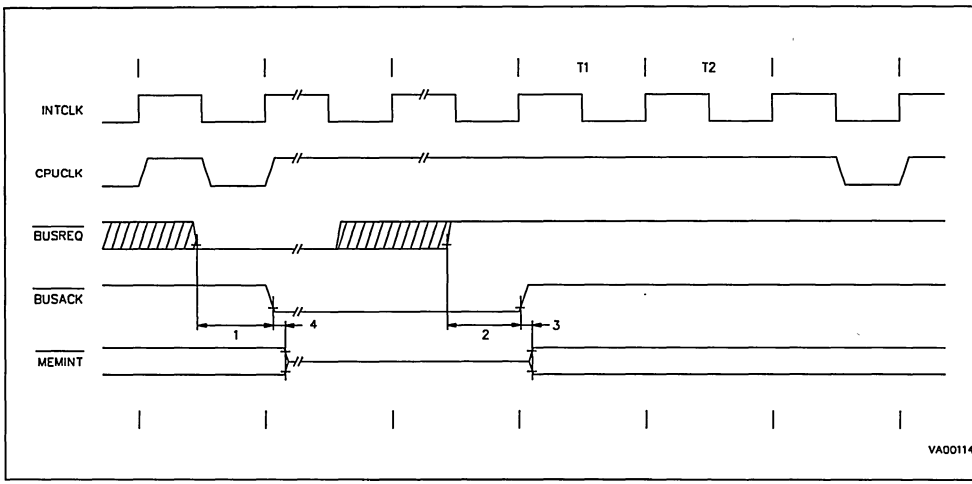


BUS REQUEST/ACKNOWLEDGE TIMING TABLE (V_{DD} = 5V ± 10%, T_A = −40°C to +85°C, Cload = 50pF, INTCLK = 12MHz, Push-pull output configuration, unless otherwise specified)

N°	Symbol	Parameter	Value (Note)				Unit
			OSCIN Divided By 2	OSCIN Not Divided By 2	Min.	Max.	
1	TdBR (BACK)	$\overline{BREQ}$ ↓ to $\overline{BUSACK}$ ↓	TpC+8	TwCL+12	50		ns
			TpC(6P+2W+7)+65	TpC(3P+W+3)+TwCL+65		360	ns
2	TdBR (BACK)	$\overline{BREQ}$ ↑ to $\overline{BUSACK}$ ↑	3TpC+60	TpC+TwCL+60		185	ns
3	TdBACK (BREL)	$\overline{BUSACK}$ ↓ to Bus Release	20	20		20	ns
4	TdBACK (BACT)	$\overline{BUSACK}$ ↑ to Bus Active	20	20		20	ns

Note: The value left hand two columns show the formula used to calculate the timing minimum or maximum from the oscillator clock period, prescale value and number of wait cycles inserted.
The value right hand two columns show the timing minimum and maximum for an external clock at 24 MHz divided by 2, prescale value of zero and zero wait status.

BUS REQUEST/ACKNOWLEDGE TIMING



Note : MEMINT = group of memory interface signals : $\overline{AS}$, $\overline{DS}$, R/$\overline{W}$, P00-P07, P10-P17.

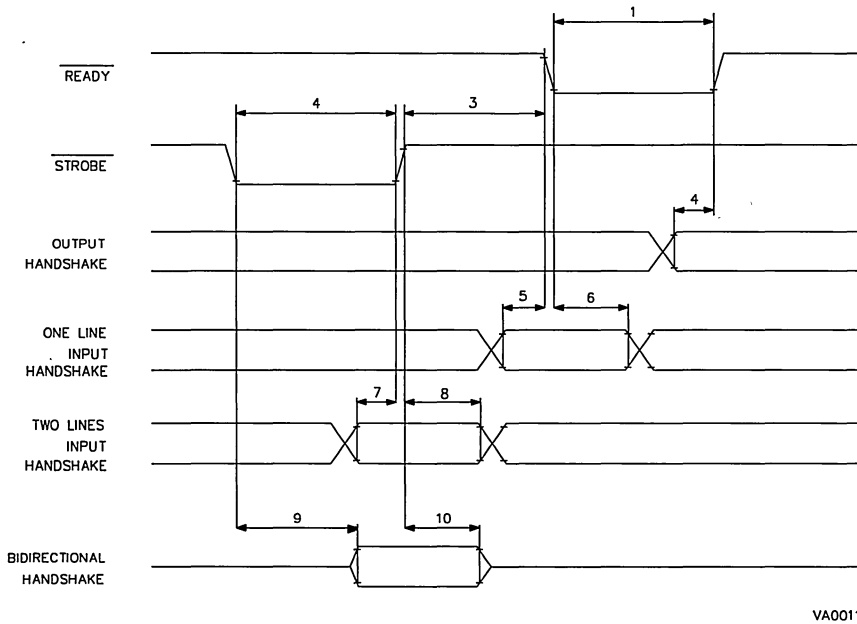
HANDSHAKE TIMING TABLE (V_{DD} = 5V ± 10%, T_A = –40°C to +85°C, Cload = 50pF, INTCLK = 12MHz, Push-pull output configuration, unless otherwise specified)

N°	Symbol	Parameter	Value (Note)				Min.	Max.	Unit
			OSCIN Divided By 2		OSCIN Not Divided By 2				
			Min.	Max.	Min.	Max.			
1	TwRDY	RDRDY, WRRDY Pulse Width in One Line Handshake	2TpC (P+W+1) –18		Tp (P+W+1) – 18		65		ns
2	TwSTB	$\overline{RDSTB}$, $\overline{WRSTB}$ Pulse Width	2TpC+12		TpC+12		95		ns
3	TdST (RDY)	$\overline{RDSTB}$, or $\overline{WRSTB}$ ↑ to RDRDY or WRRDY ↓		TpC+45		(TpC-TwCL) +45		87	ns
4	TsPD (RDY)	Port Data to RDRDY ↑ Set-up Time	(2P+2W+1) TpC –25		TwCH+(W+P) TpC –25		16		ns
5	TsPD (RDY)	Port Data to WRRDY ↓ Set-up Time in One Line Handshake	43		43		43		ns
6	ThPD (RDY)	Port Data to WRRDY ↓ Hold Time in One Line Handshake	0		0		0		ns
7	TsPD (STB)	Port Data to $\overline{WRSTB}$ ↑ Set-up Time	10		10		10		ns
8	ThPD (STB)	Port Data to WRSTB ↑ Hold Time	25		25		25		ns
9	TdSTB (PD)	$\overline{RDSTBD}$ ↑ to Port Data Delay Time in Bidirectional Handshake		35		35		35	ns
10	TdSTB (PHZ)	$\overline{RDSTB}$ ↑ to Port High-Z Delay Time in Bidirectional Handshake		25		25		25	ns

Note: The value left hand two columns show the formula used to calculate the timing minimum or maximum from the oscillator clock period, prescale value and number of wait cycles inserted.
The value right hand two columns show the timing minimum and maximum for an external clock at 24 MHz divided by 2, prescaler value of zero and zero wait status.

Legend:
P = Clock Prescaling Value (R235.4,3,2)
W = Programmable Wait Cycles (R252.2.1.0/5,4,3) + External Wait Cycles

HANDSHAKE TIMING

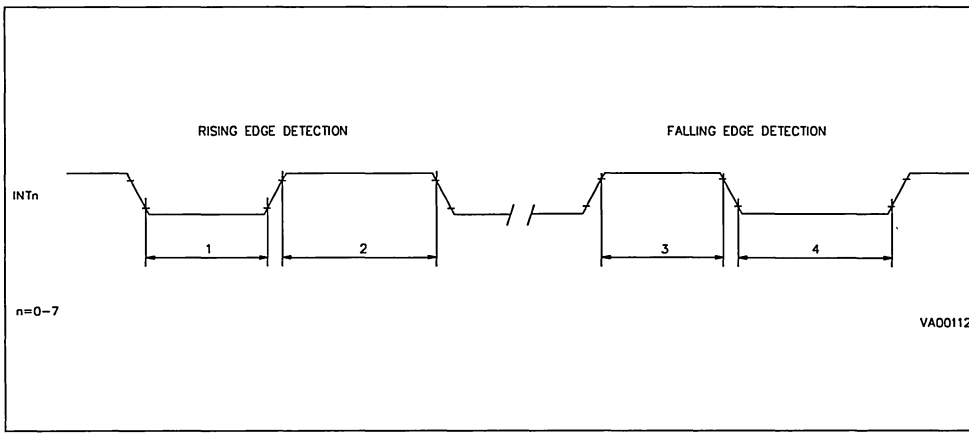


EXTERNAL INTERRUPT TIMING TABLE (V_{DD} = 5V ± 10%, T_A = –40°C to +85°C, Cload = 50pF, INTCLK = 12MHz, Push-pull output configuration, unless otherwise specified)

N°	Symbol	Parameter	Value (Note)				Unit
			OSCIN Divided By 2 Min.	OSCIN Not Divided By 2 Min.	Min.	Max.	
1	TwLR	Low Level Minimum Pulse Width in Rising Edge Mode	2TpC+12	TpC+12	95		ns
2	TwHR	High Level Minimum Pulse Width in Rising Edge Mode	2TpC+12	TpC+12	95		ns
3	TwHF	High Level Minimum Pulse Width in Falling Edge Mode	2TpC+12	TpC+12	95		ns
4	TwLF	Low Level Minimum Pulse Width in Falling Edge Mode	2TpC+12	TpC+12	95		ns

Note: The value left hand two columns show the formula used to calculate the timing minimum or maximum from the oscillator clock period, prescale value and number of wait cycles inserted.
The value right hand two columns show the timing minimum and maximum for an external clock at 24 MHz divided by 2, prescale value of zero and zero wait status.

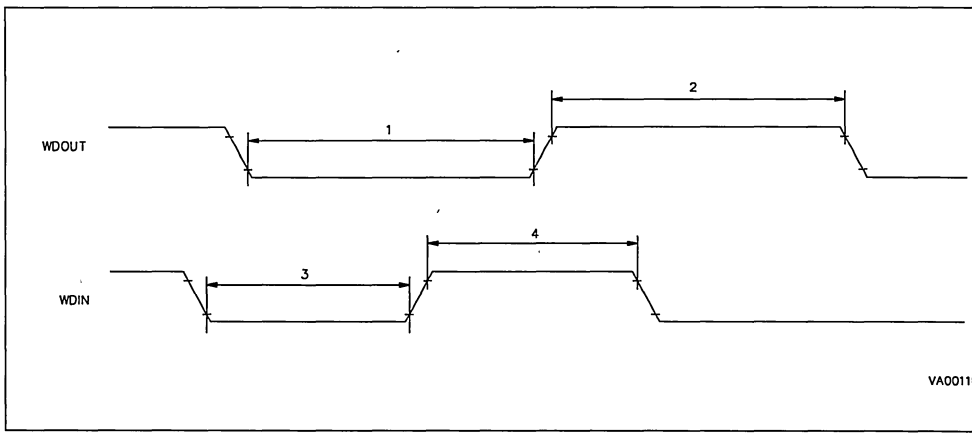
EXTERNAL INTERRUPT TIMING



WATCHDOG TIMING TABLE (V_{DD} = 5V ± 10%, T_A = –40°C to +85°C, Cload = 50pF, INTCLK =12MHz, Output Alternate Function set as Push-pull)

N°	Symbol	Parameter	Value		Unit
			Min.	Max.	
1	TwWDOL	WDOUT Low Pulse Width	620		ns
2	TwWDOH	WDOUT High Pulse Width	620		ns
3	TwWDIL	WDIN Low Pulse Width	350		ns
4	TwWDIH	WDIN High Pulse Width	350		ns

WATCHDOG TIMING

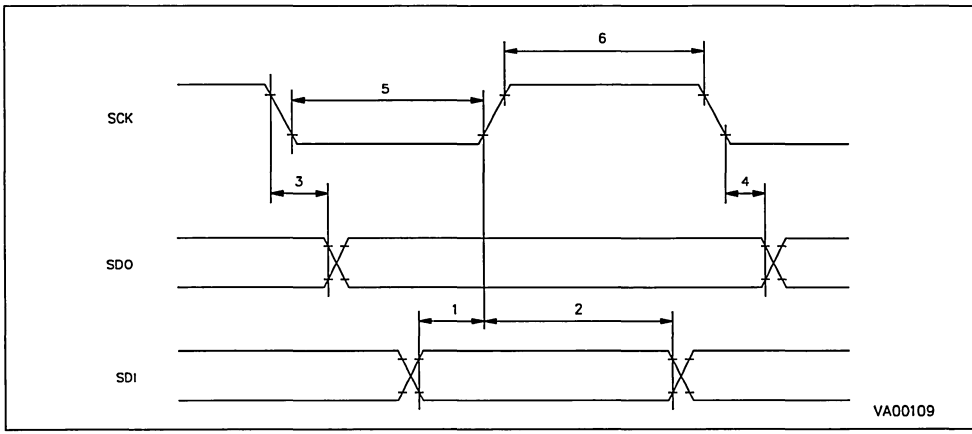


SPI TIMING TABLE (V_{DD} = 5V ± 10%, T_A = –40°C to +85°C, Cload = 50pF, INTCLK = 12MHz, Output Alternate Function set as Push-pull)

N°	Symbol	Parameter	Value		Unit
			Min.	Max.	
1	TsDI	Input Data Set-up Time	100		ns
2	ThDI (1)	Input Data Hold Time	1/2 TpC+100		ns
3	TdOV	SCK to Output Data Valid		100	ns
4	ThDO	Output Data Hold Time	-20		ns
5	TwSKL	SCK Low Pulse Width	300		ns
6	TwSKH	SCK High Pulse Width	300		ns

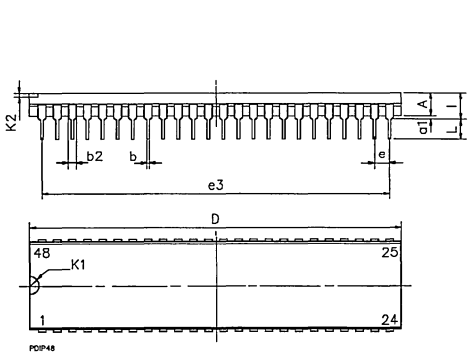
Note: 1. TpC is the Clock period.

SPI TIMING



PACKAGE MECHANICAL DATA

Figure 57. 48 Lead Plastic DIP



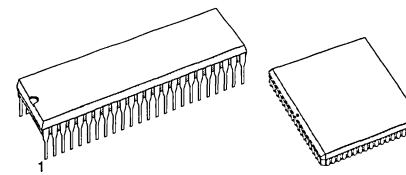
Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A	–	–	–	–	–	–
a1		0.63			0.024	
b		0.45			0.017	
b1	0.23		0.31	0.009		0.012
b2		1.27			0.050	
C	–	–	–	–	–	–
D			62.74			2.470
E	15.20		16.68	0.598		0.656
e		2.54			0.100	
e3		58.42			2.300	
e4	–	–	–	–	–	–
F			14.10			0.555
I		4.45			0.175	
L		3.30			0.129	

ORDERING INFORMATION

Sales Type	Frequency	Temperature Range	Package
ST90R26B6	24MHz	-40°C to +85°C	PDIP48
ST90R26B1	24MHz	0°C to +70°C	PDIP48

8K ROM HCMOS MCUs WITH A/D CONVERTER

- Single chip microcontroller, 8K bytes of ROM and 256 bytes of register file with 224 general purpose registers available as RAM, accumulator or index pointers.
- 8/16 bit CORE with full feature DMA controller and powerful interrupt handler and a standard Serial Peripheral Interface (SPI) handling S-BUS/I^2C Bus and IM BUS.
- Up to 8 external interrupts edge selectable plus 1 non-maskable interrupt.
- 16 bit programmable Timer with 8 bit Prescaler, able to be used as a Timer/Watchdog for system integrity.
- Two 16 bit Multifunction Timer modules, each with an 8 bit Prescaler and 13 operating modes, allowing simple use for complex waveform generation and measurement, PWM functions and many other system timing operations.
- 8 channel Analog to Digital Converter, with integral sample and hold, fast 11µs conversion time and 8 bit ± 1/2 LSB resolution with Analog Watchdog on two channels.
- Full function Serial Communication Interface with 110 to 375000 baud rate generator, asynchronous and byte synchronous capability (fully programmable format) and address/wake-up bit option.
- On-chip DMA channels associated with the Multifunction Timers and the Serial Communication Interface.
- Up to seven 8 bit I/O ports with programmable input thresholds and output characteristics. Alternative functions allow the full use of all pins.
- Powerful software development tools, including assembler, linker, C-compiler, archiver, software and hardware emulators.
- Windowed and One Time Programmable EPROM parts available for prototyping and preproduction development phases.
- 68-lead Plastic Leaded Chip Carrier package for ST9030.
- 48-pin Dual in Line Plastic package for ST9031



PDIP48 **PLCC68**

(Ordering Information at the end of the datasheet)

Figure 1. ST9031 Pin Configuration

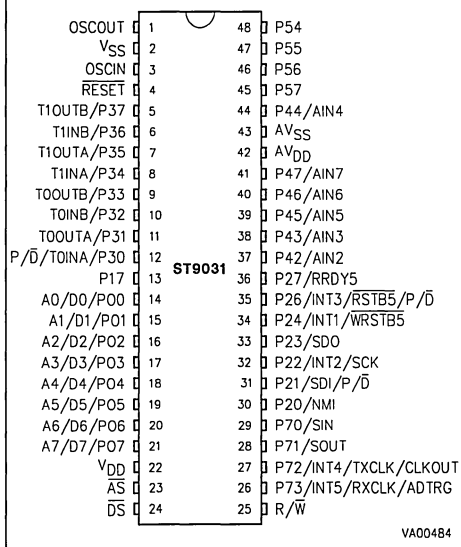


Figure 2. ST9030 Pin Configuration

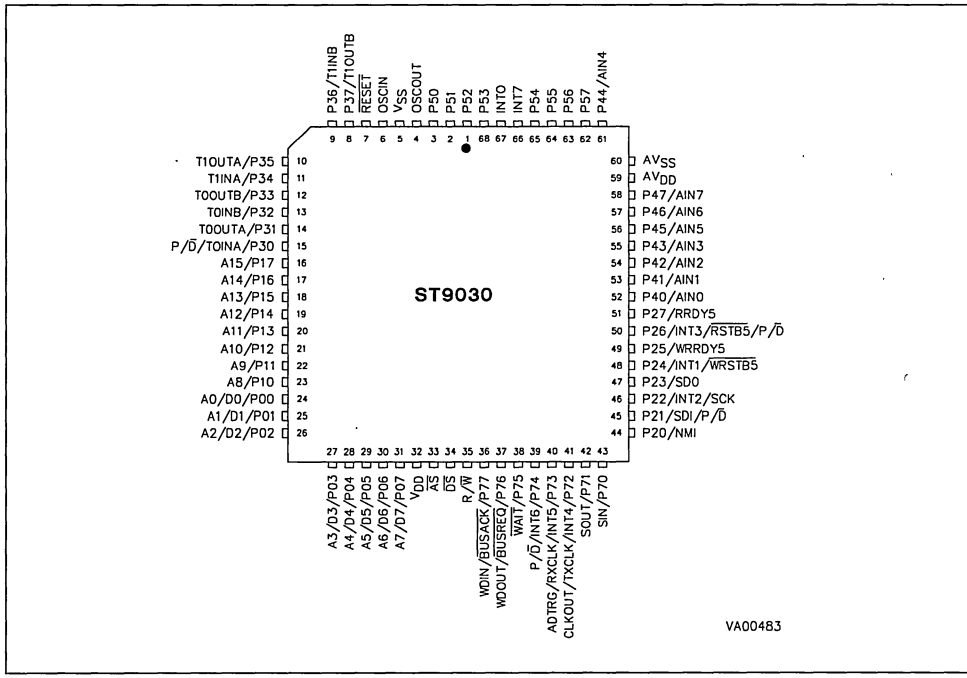
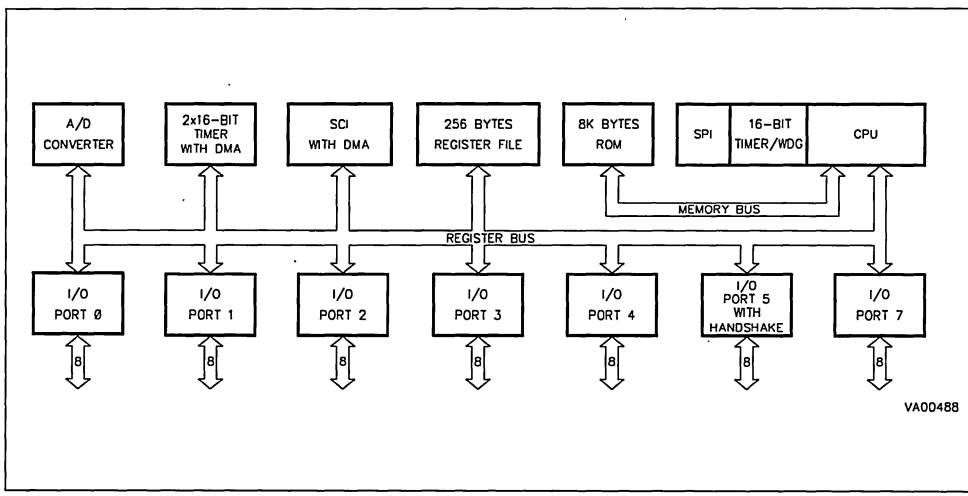


Figure 3. ST903X Block Diagram



Note : Refer to Table 1 for ST903X I/O Port Summary

GENERAL DESCRIPTION

The ST9030 and ST9031 devices (following mentioned as ST903X) are ROM members of the ST9 family of microcontrollers, completely developed and produced by SGS-THOMSON Microelectronics using a proprietary n-well HCMOS process.

The ROM parts are fully compatible with their EPROM versions, which may be used for the prototyping and pre-production phases of development, and can be configured as standalone microcontrollers with 8K bytes of on-chip ROM, microcontrollers able to manage up to 120K bytes of external memory, or as parallel processing elements in a system with other processors and peripheral controllers.

A key point of the ST903X architecture is its modular approach which allows software commonality with all other members of the ST9 family.

The nucleus of the modular design of the ST903X is the advanced Core which includes the Central Processing Unit (CPU), the Register File, a 16 bit Timer/Watchdog with 8 bit Prescaler, a Serial Peripheral Interface supporting S-BUS, I^2C Bus and IM BUS Interface, plus two 8 bit I/O ports. The Core has independent memory and register buses allowing a high degree of pipelining to add to the efficiency of the code execution speed of the extensive instruction set. The powerful I/O capabilities demanded by microcontroller applications are fulfilled by the ST903X with up to 56 I/O lines dedicated to digital Input/Output. These lines are grouped into up to seven 8 bit I/O Ports and can be configured on a bit basis under software control to provide timing, status signals, an address/data bus for interfacing external memory, timer inputs and outputs, analog inputs, external interrupts and serial or parallel I/O with or without handshake.
Three memory spaces are available: Program Memory (internal and external), Data Memory (external) and the Register File, which includes the control and status registers of the on-chip peripherals.

Two 16 bit MultiFunction Timers, each with an 8 bit Prescaler and 13 operating modes allow simple use for complex waveform generation and measurement, PWM functions and many other system timing functions by the usage of the two associated DMA channels for each timer. In addition there is an 8 channel Analog to Digital Converter with integral sample and hold, fast 11µs conversion time and 8 bit ± 1/2 LSB resolution. An Analog Watchdog feature is included for two input channels.

Completing the device is a full duplex Serial Communications Interface with an integral 110 to 375000 baud rate generator, asynchronous and byte synchronous capability (fully programmable format) and associated address/wake-up option, plus two DMA channels.

PIN DESCRIPTION

$\overline{AS}$. *Address Strobe (output, active low, 3-state).* Address Strobe is pulsed low once at the beginning of each memory cycle.
The rising edge of $\overline{AS}$ indicates that address, Read/Write (R/$\overline{W}$), and Data Memory signals are valid for program or data memory transfers. Under program control, $\overline{AS}$ can be placed in a high-impedance state along with Port 0 and Port 1, Data Strobe ($\overline{DS}$) and R/$\overline{W}$.

$\overline{DS}$. *Data Strobe (output, active low, 3-state).* Data Strobe provides the timing for data movement to or from Port 0 for each memory transfer. During a write cycle, data out is valid at the leading edge of $\overline{DS}$. During a read cycle, Data In must be valid prior to the trailing edge of $\overline{DS}$. When the ST903X accesses on-chip memory, $\overline{DS}$ is held high during the whole memory cycle. It can be placed in a high impedance state along with Port 0, Port 1, $\overline{AS}$ and R/$\overline{W}$.

R/$\overline{W}$. *Read/Write (output, 3-state).* Read/Write determines the direction of data transfer for external memory transactions. R/$\overline{W}$ is low when writing to external program or data memory, and high for all other transactions. It can be placed in a high impedance state along with Port 0, Port 1, $\overline{AS}$ and $\overline{DS}$.

$\overline{RESET}$. *Reset (input, active low).* The ST9 is initialised by the Reset signal. With the deactivation of $\overline{RESET}$, program execution begins from the Program memory location pointed to by the vector contained in program memory locations 00h and 01h.

OSCIN, OSCOUT. *Oscillator (input and output).* These pins connect a parallel-resonant crystal (24MHz maximum), or an external source to the on-chip clock oscillator and buffer. OSCIN is the input of the oscillator inverter and internal clock generator; OSCOUT is the output of the oscillator inverter.

AV_{DD}. Analog V_{DD} of the Analog to Digital Converter.

AV_{SS}. Analog V_{SS} of the Analog to Digital Converter.

V_{DD}. Main Power Supply Voltage (5V ± 10%).

V_{SS}. Digital Circuit Ground.

P00-P07, P10-P17, P20-P27, P30-P37,P40-P47, P50-P57, P70-P77. *I/O Port Lines (Input/Output, TTL or CMOS compatible).* 8 lines grouped into I/O ports of 8 bits, bit programmable under program control as general purpose I/O or as Alternate Functions (see next section).

I/O Port Alternate Functions. Each pin of the I/O ports of the ST903X may assume Alternative Functions as shown in the Pin Configuration Drawings. Due to Bonding options for the packages, some functions may not be present, Table 1 shows the Functions allocated to the I/O port pins and a summary of packages for which they are available.

PIN DESCRIPTION (Continued)

Table 1. ST903X I/O Port Alternate Function Summary

I/O PORT	Name	Function	Alternate Function	Pin Assignment	
Port. bit				9030	9031
P0.0	A0/D0	I/O	Address/Data bit 0 mux	24	14
P0.1	A1/D1	I/O	Address/Data bit 1 mux	25	15
P0.2	A2/D2	I/O	Address/Data bit 2 mux	26	16
P0.3	A3/D3	I/O	Address/Data bit 3 mux	27	17
P0.4	A4/D4	I/O	Address/Data bit 4 mux	28	18
P0.5	A5/D5	I/O	Address/Data bit 5 mux	29	19
P0.6	A6/D6	I/O	Address/Data bit 6 mux	30	20
P0.7	A7/D7	I/O	Address/Data bit 7 mux	31	21
P1.0	A8	O	Address bit 8	23	–
P1.1	A9	O	Address bit 9	22	–
P1.2	A10	O	Address bit 10	21	–
P1.3	A11	O	Address bit 11	20	–
P1.4	A12	O	Address bit 12	19	–
P1.5	A13	O	Address bit 13	18	–
P1.6	A14	O	Address bit 14	17	–
P1.7	A15	O	Address bit 15	16	13
P2.0	NMI	I	Non-Maskable Interrupt	44	30
P2.0	ROMless	I	ROMless Select (Mask option)	44	30
P2.1	P/$\overline{D}$	O	Program/Data Space Select	45	31
P2.1	SDI	I	SPI Serial Data Out	45	31
P2.2	INT2	I	External Interrupt 2	46	32
P2.2	SCK	O	SPI Serial Clock	46	32
P2.3	SDO	O	SPI Serial Data In	47	33
P2.4	INT1	I	External Interrupt 1	48	34
P2.4	$\overline{WRSTB5}$	O	Handshake Write Strobe P5	48	34
P2.5	WRRDY5	I	Handshake Write Ready P5	49	–
P2.6	INT3	I	External Interrupt 3	50	35
P2.6	$\overline{RDSTB5}$	I	Handshake Read Strobe P5	50	35
P2.6	P/$\overline{D}$	O	Program/Data Space Select	50	35
P2.7	RDRDY5	O	Handshake Read Ready P5	51	36
P3.0	T0INA	I	MF Timer 0 Input A	15	12
P3.0	P/$\overline{D}$	O	Program/Data Space Select	15	12
P3.1	T0OUTA	O	MF Timer 0 Output A	14	11
P3.2	T0INB	I	MF Timer 0 Input B	13	10
P3.3	T0OUTB	O	MF Timer 0 Output B	12	9
P3.4	T1INA	I	MF Timer 1 Input A	11	8

PIN DESCRIPTION (Continued)

Table 1. ST903X I/O Port Alternate Function Summary (Continued)

I/O PORT	Name	Function	Alternate Function	Pin Assignment	
Port. bit				9030	9031
P3.5	T1OUTA	O	MF Timer 1 Output A	10	7
P3.6	T1INB	I	MF Timer 1 Input B	9	6
P3.7	T1OUTB	O	MF Timer 1 Output B	8	5
P4.0	AIN0	I	A/D Analog Input 0	52	–
P4.1	AIN1	I	A/D Analog Input 1	53	–
P4.2	AIN2	I	A/D Analog Input 2	54	37
P4.3	AIN3	I	A/D Analog Input 3	55	38
P4.4	AIN4	I	A/D Analog Input 4	61	44
P4.5	AIN5	I	A/D Analog Input 5	56	39
P4.6	AIN6	I	A/D Analog Input 6	57	40
P4.7	AIN7	I	A/D Analog Input 7	58	41
P5.0		I/O	I/O Handshake Port 5	3	–
P5.1		I/O	I/O Handshake Port 5	2	–
P5.2		I/O	I/O Handshake Port 5	1	–
P5.3		I/O	I/O Handshake Port 5	68	–
P5.4		I/O	I/O Handshake Port 5	65	48
P5.5		I/O	I/O Handshake Port 5	64	47
P5.6		I/O	I/O Handshake Port 5	63	46
P5.7		I/O	I/O Handshake Port 5	62	45
P7.0	SIN	I	SCI Serial Input	43	29
P7.1	SOUT	O	SCI Serial Output	42	28
P7.1	ROMless	I	ROMless Select (Mask option)	42	28
P7.2	INT4	I	External Interrupt 4	41	27
P7.2	TXCLK	I	SCI Transmit Clock Input	41	27
P7.2	CLKOUT	O	SCI Byte Sync Clock Output	41	27
P7.3	INT5	I	External Interrupt 5	40	26
P7.3	RXCLK	I	SCI Receive Clock Input	40	26
P7.3	ADTRG	I	A/D Conversion Trigger	40	26
P7.4	INT6	I	External Interrupt 6	39	–
P7.4	P/$\overline{D}$	O	Program/Data Space Select	39	–
P7.5	$\overline{WAIT}$	I	External Wait Input	38	–
P7.6	WDOUT	O	T/WD Output	37	–
P7.6	$\overline{BUSREQ}$	I	External Bus Request	37	–
P7.7	WDIN	I	T/WD Input	36	–
P7.7	$\overline{BUSACK}$	O	External Bus Acknowledge	36	–

ST903X CORE

The Core or Central Processing Unit of the ST903X includes the 8 bit Arithmetic Logic Unit and the 16 bit Program Counter, System and User Stack Pointers. The microcoded Instruction Set is highly optimised for both byte (8 bit) and word (16 bit) data, BCD and Boolean data types, with 14 addressing modes. Two 8 bit I/O Ports are connected to the Core module for external memory interfacing, while a 16 bit Timer/Watchdog gives system security and timing functions, and a Serial Peripheral Interface allows for synchronous communication. Three independent buses are controlled by the Core, a 16 bit Memory bus, an 8 bit Register addressing bus and a 6 bit Interrupt/DMA bus connected to the interrupt and DMA controllers in the on-chip peripherals and the Core. This multiple bus architecture allows a high degree of pipelining and parallel operation within the ST903X, giving it its efficiency in both numerical calculations and communication with the on-chip peripherals.

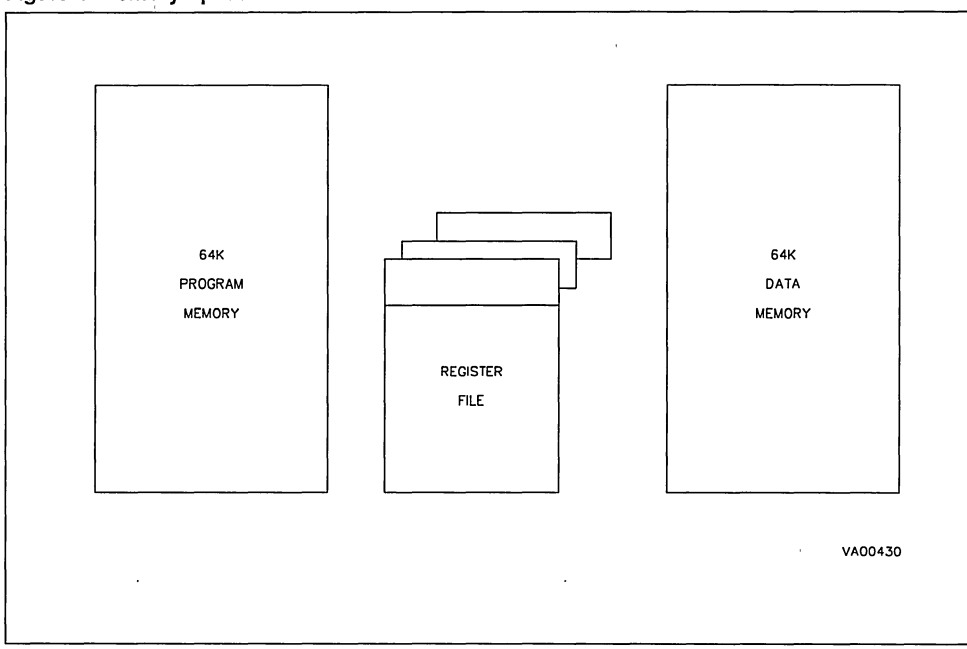
MEMORY

The memory of the ST903X is functionally divided into two areas, the Register File and Memory. The Memory may optionally be divided into two spaces, each having a maximum of 65,536 bytes. The two memory spaces are separated by function, one space for Program code, the other for Data. The ST903X 8K bytes of on-chip ROM memory is selected at memory addresses 0 through 1FFFh (hexadecimal) in the PROGRAM space.

External memory, addressed using the multiplexed address and data buses (Port 0 and Port 1) may be divided into the Program and Data spaces by the external decoding of the Program/Data select pin (P/$\overline{D}$) available as an Alternate function, allowing a full 128K byte memory. The memory spaces are selected by the execution of the `SDM` and `SPM` instructions (Set Data Memory and Set Program Memory, respectively). There is no need to use either of these instructions again until the memory area required is to be changed. This requirement is not necessary in two cases: first, when operating with external stacks (the Data Memory is automatically selected) and, secondly, when using the memory indirect to memory indirect post-increment addressing mode (the memory types are specified in the instructions: `LDPP, LDPD. LDDP, LDDD`).

Either the Data Memory or the Program Memory can be addressed using any of the memory addressing modes.

Figure 4. Memory Spaces



MEMORY (Continued)

Program Space

The Program Memory space of the ST903X, from the 8K bytes of on-chip ROM memory to the full 64K bytes with off-chip memory expansion is fully available to the user. At addresses greater than the first 8K of program space, the ST903X executes external memory cycles for instruction fetches. The first 256 memory locations from address 0 to 0FFh (hexadecimal) hold the Reset Vector, the Top-Level (Pseudo Non-Maskable) interrupt, the Divide by Zero Trap vector and, optionally, the interrupt vector table for use with the on-chip peripherals and the external interrupt sources. Each vector is contained in two consecutive byte locations, the high order address held in the lower (even) byte, the low order address held in the upper (odd) byte, forming the address which is loaded into the Program Counter when selected by the interrupt vector provided by the interrupt source. This should point to the relevant Interrupt Service routine provided by the user for immediate response to the interrupt.

Data Space

The ST903X may address the full 65,536 locations of External Data through the External Memory Interface when decoded with the P/$\overline{D}$ pin. The on-chip Registers may be used as RAM memory for minimum chip count systems.

The Data Space is selected by the execution of the SDM instruction. All subsequent memory references will access the Data Space. When a separate Data Space is not required, data may be stored in external RAM or ROM memory within the Program Space.

ROMless Option

In the event of a program revision being required after the development of a ROM-based ST903X, a mask option is available which enables the reconfiguration of the memory spaces to give a fully ROMless device. This means that the on-chip program ROM is disabled and ALL memory is seen as external, allowing the use of replacement program code in external ROM memory.

To give the ROMless function (when enabled by the MASK option), either pin marked ROMless as an Alternate Function should be held to ground (V_{SS}) with a high resistance (eg 100K ohm) during the RESET cycle. The pin status is latched on the rising edge of the RESET input. After this time, the pin is free for normal operation. If the ROMless option is enabled, and the on-chip program is to be used, the pin enabled for the ROMless function must to held to a high potential during the RESET cycle (eg with a 100K ohm resistor to V_{DD}.

Figure 5. Program Memory Space

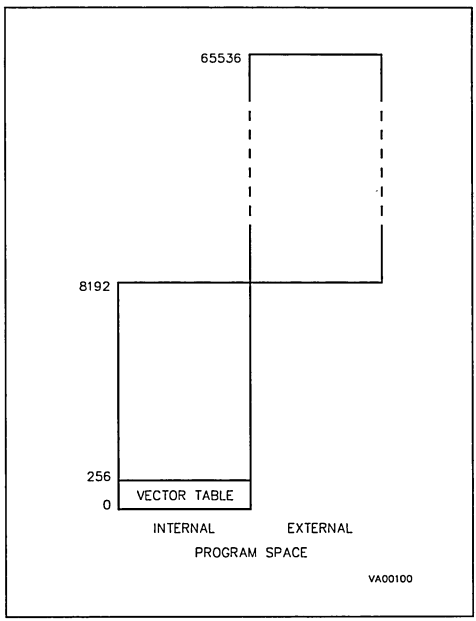
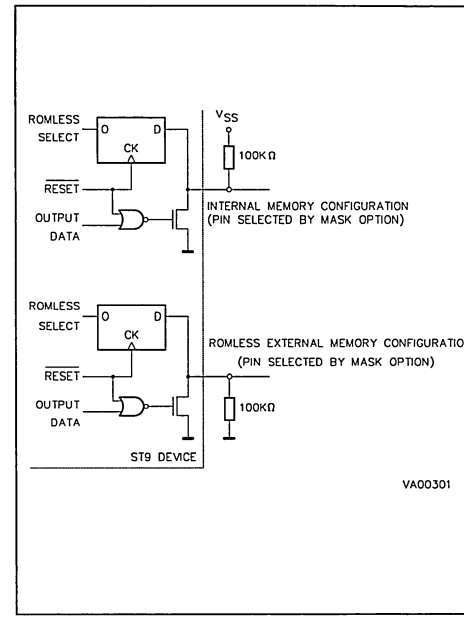


Figure 6. ROMless Selection



REGISTERS

The ST903X Register File consists of 240 registers (224 general purpose) plus pages of 16 registers supporting the configuration and control registers for the on-chip peripherals. The 224 general purpose registers all have 8 and 16 bit arithmetic capability and may be used as accumulators, on-chip RAM, internal Stack areas (for system and/or user stacks), or, with the appropriate addressing modes, as index, offset or stack pointers.

The register file is arranged into 16 groups of 16 registers, where the general purpose registers occupy the first 14 groups. The 15th group, E, contains the system registers and Group F contains the pages of the on-chip peripheral control registers.

Group F is paged in this manner due to the modularity of the ST9 family of microcontrollers. Each member of the family retains all general purpose and system registers, only the paged register groups changing owing to the different on-chip peripheral organizations of each device. The user can therefore generate code libraries which use the general purpose registers knowing that they will not be lost on future ST9 devices. To address a paged register, the Page Pointer (PPR, R234) within the system register group must be loaded with the relevant page number using the SPP instruction. Subsequently any access to registers in the top group (R240-R255) will refer to the selected page. This remains set until the next change to the Page Pointer register (by the SPP instruction).

Figure 7. Register Grouping

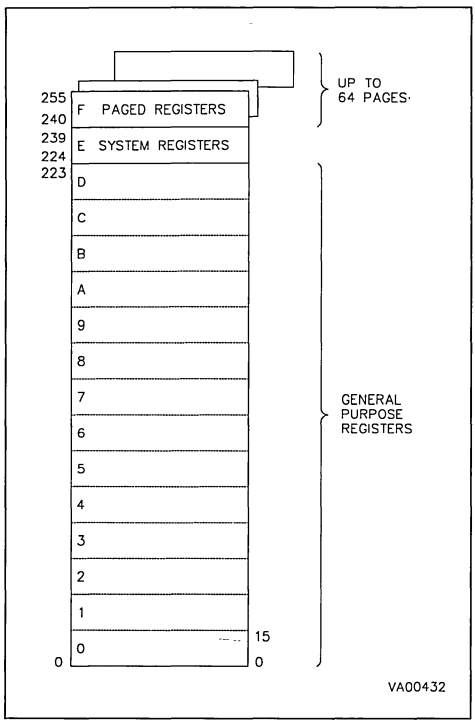
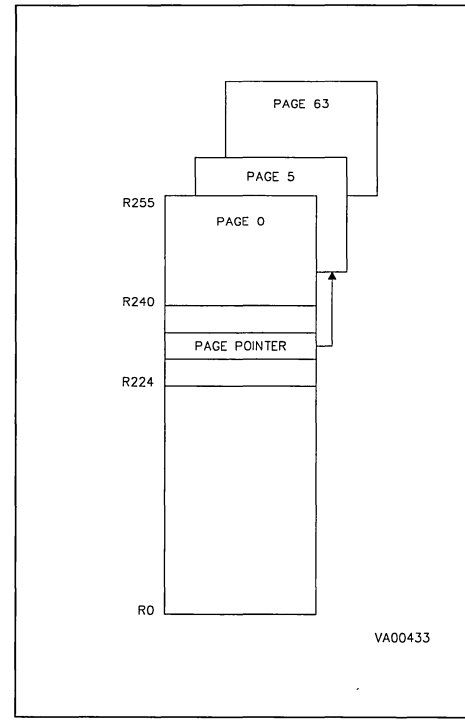
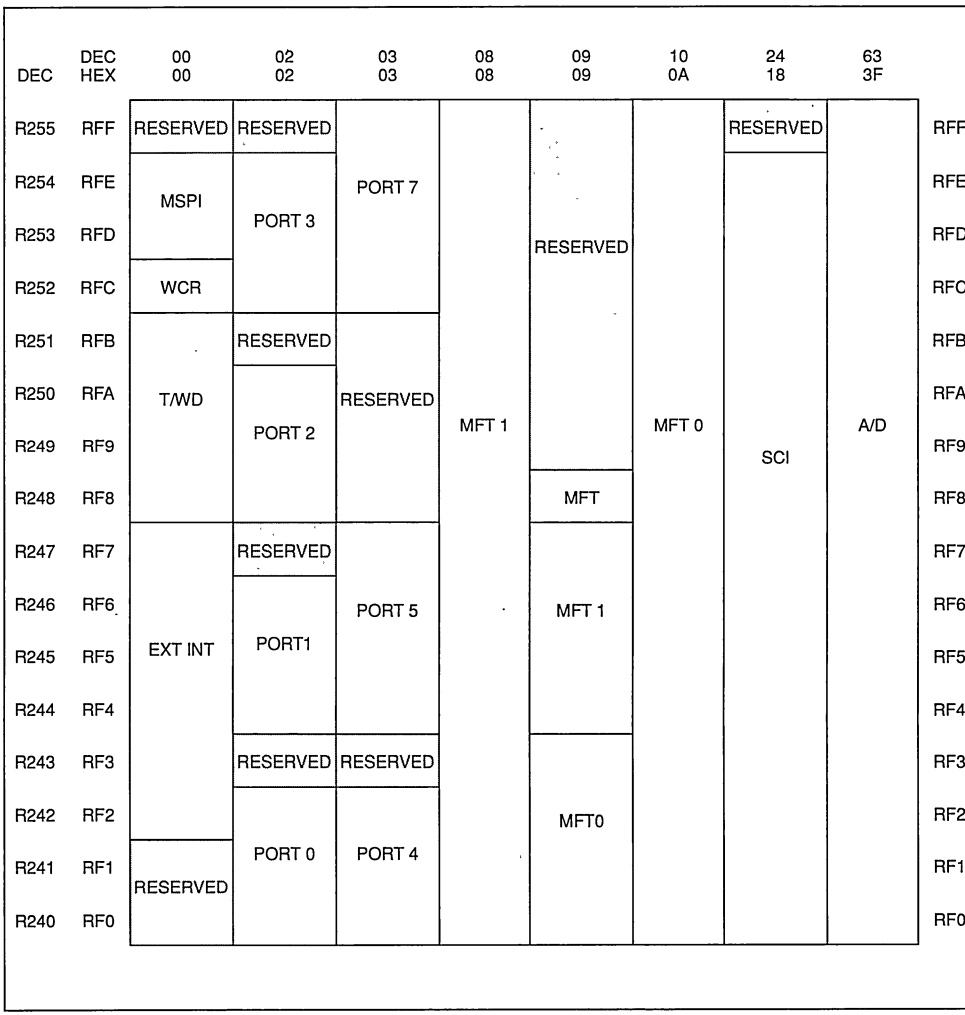


Figure 8. Page Pointer Mechanism



REGISTERS (Continued)

Figure 9. ST9030 Group F Peripheral Organisation



REGISTERS (Continued)

The System group (Group E, registers RE0 to REF) includes the system and user stack pointers, the Mode register, the ALU FLAGS register and the Page pointer register. In addition the data registers for the first 6 I/O ports are present, the configuration registers for the ports being in the paged area. This allows the immediate access to these I/O ports at all times.

Table 2. Group E Register Map

R239	System Stack Pointer Low (SSPLR)
R238	System Stack Pointer High (SSPHR)
R237	User Stack Pointer Low (USPLR)
R236	User Stack Pointer High (USPHR)
R235	Mode Register (MODER)
R234	Page Pointer (PPR)
R233	Register Pointer 1 (RP1R)
R232	Register Pointer 0 (RP0R)
R231	ALU Flags (FLAGR)
R230	Central Interrupts Control (CICR)
R229	Port 5 Data (P5DR)
R228	Port 4 Data (P4DR)
R227	Port 3 Data (P3DR)
R226	Port 2 Data (P2DR)
R225	Port 1 Data (P1DR)
R224	Port 0 Data (P0DR)

The Register Pointers, present in the system register group, select groups of registers as "Working Registers", which have faster addressing modes than direct Register addressing and allows smaller code size. The Register Pointers may either be used singly, creating a register group of 16 working registers, or as two independent groups of 8 working registers which may be placed at any 8 register boundary within the register file. The single and twin working register modes are automatically set by hardware when the respective SRP and either SRP0 or SRP1 instructions are executed. If working registers are used as accumulators and RAM locations for particular tasks, fast context switching on interrupts may be achieved by setting the register pointer to another group for the Interrupt Service Routine, ISR, (e.g. saving the Register pointer on the stack), using the new group in the ISR and subsequently restoring the original group before the Return from Interrupt instruction.Working registers also allow the use of the ABAR - Any Bit-Any Register Boolean operations (including directly on the I/O port data registers).

Figure 10. Single Working Register Bank

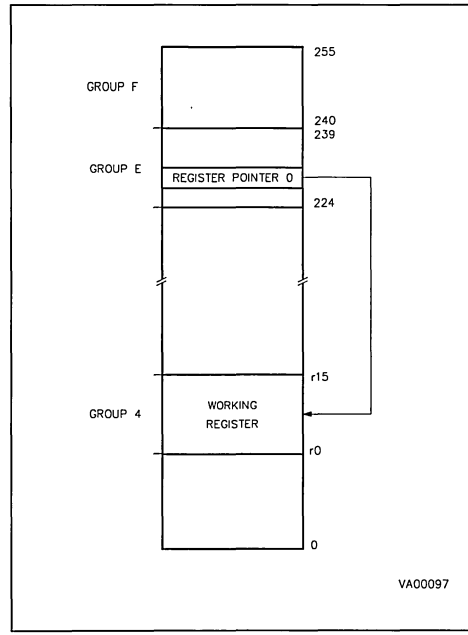
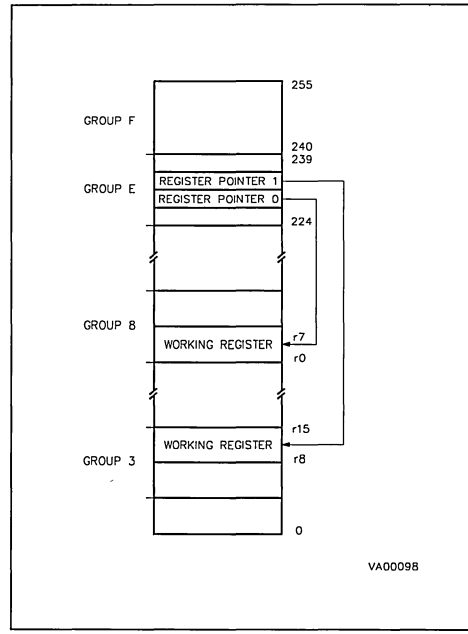


Figure 11. Dual Working Register Banks



REGISTERS (Continued)

In the ST9 syntax, directly addressed Registers are indicated with a capital R e.g. R0, R224, RBF, with Register Pairs (16 bit accumulators or memory pointers) as RR0, RR24. When using Working Registers, groups of 16 registers (SRP instruction) are denoted as r0 to r15 (rr0 to rr14), while the dual working register group are addressed as r0 to r7 (rr0 to rr6), for the first group of 8 registers (SRP0), with r8 to r15 (rr8 to rr15) for the second set (SRP1). Working register addressing requires a 4 bit field within the instruction. When packed into a byte, the upper nibble is set to Dh (1101b), this being the escape code to indicate the use of the working registers. As a result, group D cannot be selected with direct register addressing, it is recommended that this group be used as internal stacking area when using register file based system or user stack pointers.

STACK POINTERS

There are two separate, double register stack pointers available (System and User), both of which can operate in register or Data memory address spaces. These operate in a Pre-Decrement mode when data is PUSHed onto the Stack and in a Post-Increment mode when data is POPed from the stack.
The system Stack Pointer (SSPR, R238:R239) is used for the storage of temporarily suspended system and/or control registers (ie the Program Counter and FLAG register) while interrupts are being serviced, and is used for the storage of the Program Counter following the CALLing of a subroutine. The user Stack Pointer (USPR, R236:R237) is completely free from all interference from automatic operations and so provides for a totally user controlled stack area.

Both Stack pointers may operate with both byte (PUSH,POP) and word (PUSHW, POPW) data, and are differentiated by appending a "U" to the instruction mnemonic for the User Stack (PUSHU/PUSHUW, POPU/POPUW).

When the Stack Pointers are using RAM Memory as the stack areas, a full word register is used as the pointer, while when operating with the stack area within the Register File (Groups 0 to 14 only, but not the within the system and paged groups) only an 8 bit register is required for addressing and consequently only the low byte of the word registers are used (R239 for the System Stack and R237 for the User Stack). In this latter case the upper byte of the stack pointer registers (R238 and R236) must be considered as reserved. The Stack Pointers may be selected to point to RAM or Register file by the setting of the SSP (MODER.7) and USP (MODER.6) of the ST903X configuration register (MODER, R235) where a "1" denotes Register file operation (Default at Reset) and "0" causes external Data space operation.

Figure 12. Internal Stack Pointers

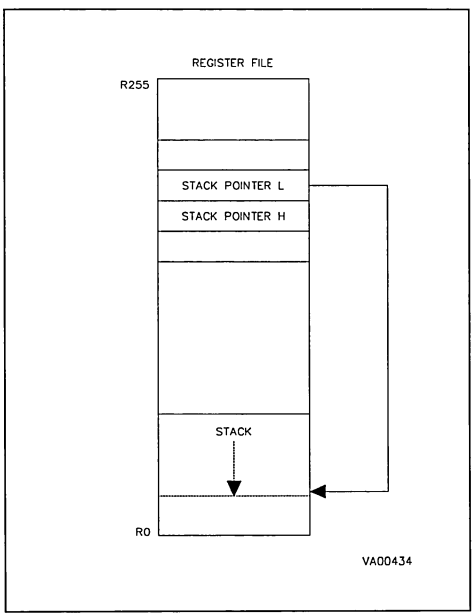
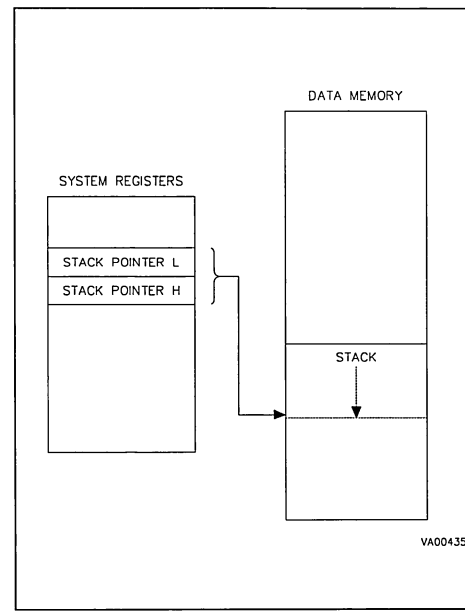


Figure 13. External Stack Pointers



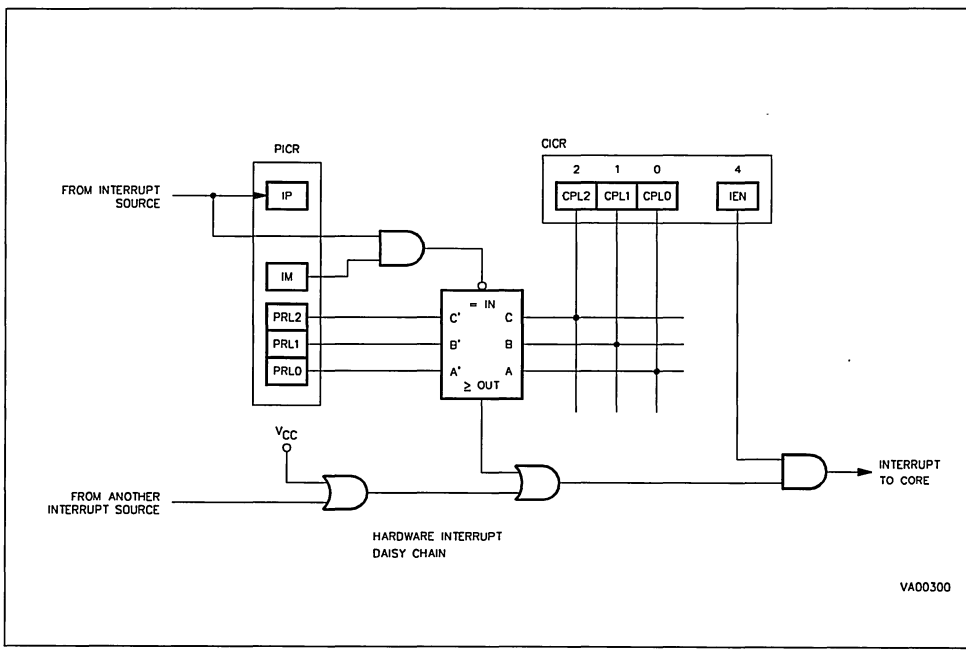
INTERRUPTS

The ST903X offers a powerful solution to the response requirements of real-time systems with its advanced interrupt structure. Interrupt trigger sources can be prioritized within 8 levels to match the priorities assigned to the application. In addition a top-level or non-maskable interrupt is available. The ST903X interrupts follow the logical flow of Figure 14.

Interrupt events (selectable with each function) cause the setting of the Interrupt Pending (IP) bit within the status register of the peripheral. This bit may also be set by software in order to generate a software interrupt, and should normally be reset by software within the interrupt service routine. If the interrupt is not Masked with the corresponding Interrupt Mask bit, the interrupt is passed to the central interrupt control logic where the priority level assigned by the programmer to the interrupt source is compared with the priority level of the core (user programmed dynamically in the 3 bits of the Central Priority register (CPL, CICR.0-2, level 7 is the lowest priority and level 0 the highest). If the incoming priority level is higher than the CPL, and Global Interrupts are enabled (by the `EI` instruction, interrupts are disabled by the execution of the `DI` instruction), the interrupt is acknowledged. If interrupts are globally disabled, the priority level of the source is lower than or equal to the CPL or the Interrupt is masked, then the IP bit remains set and the interrupt is held pending until the `EI` instruction is executed, the CPL is set to a lower level and the interrupt is un-masked. Alternatively the IP bit of a masked interrupt source may be used in a polled interrupt environment, with the IP bit being reset by software within the service routine.

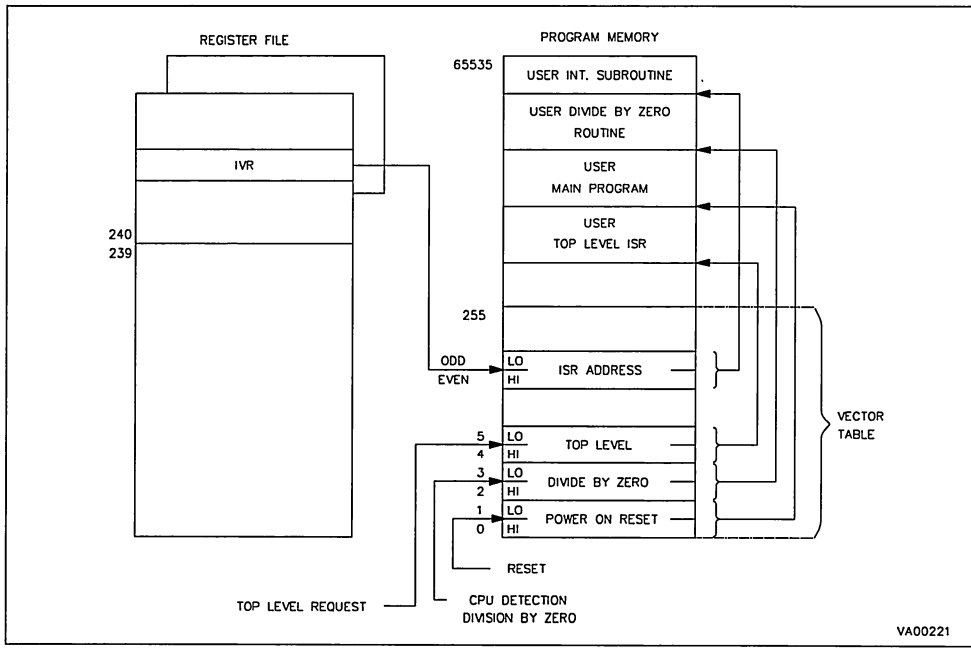
The interrupt acknowledge cycle causes the Program Counter and FLAGS register to be pushed onto the System Stack (PC low byte first, PC high byte, then FLAGS Register) and all maskable interrupts to be disabled by resetting the IEN bit. The peripheral Interrupt Vector, IVR, a user programmable feature of the peripheral interrupt control registers, is used as an offset into the vector table, pointing to the high byte (even address) of the 16 bit address which should contain the starting address of the interrupt service routine. Addresses 0 through 255 of the program space comprise the interrupt vector table. Where multiple interrupt sources may occur within a peripheral, the peripheral interrupt vector source may be encoded by hardware set bits within the IVR register. This means that the vector address defined in the peripheral IVR is the base address for a block of vectors servicing that peripheral. The address pointed to by the vector is loaded into the Program Counter and execution restarts from this point.

Figure 14. Interrupt Logic



INTERRUPTS (Continued)

Figure 15. Interrupt Vector Table Usage



The interrupt service routine should clear the interrupt pending flag of the interrupt source and take the appropriate action. The last instruction of the interrupt service routine should be the IRET instruction, the action of this is to restore the Program Counter and Flags register to their value prior to the interrupt acknowledgment, and to re-enable interrupts. Within the interrupt service routine, use may be made of the working register pointer mechanism to reduce the context switching time.

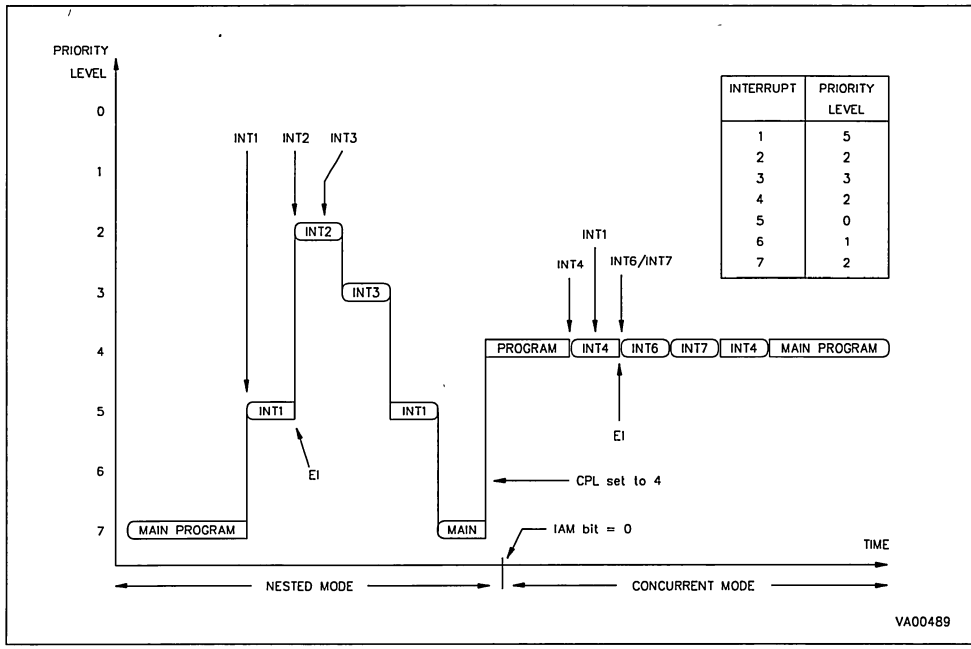
Two interrupt arbitration modes are available for use with the 8 level priority scheme, Nested and Concurrent modes. These are selected by the status of the IAM bit (CICR.3).

Concurrent mode, selected when IAM = "0" (the reset condition) is the standard interrupt arbitration mode, where the arbitration phase of every instruction acknowledges interrupts according to their priority level (if higher than the CPL) and follows the sequence shown. All pending interrupts existing or having eventually occurred during interrupt service routine execution, remain pending until the Enable Interrupt instruction (EI) (even if it is executed during the interrupt service routine). EI within the interrupt service routine is not recommended for use with the Concurrent arbitration mode as this can trigger a Last In, First Out condition where high priority interrupts are masked by lower priority interrupts which are all higher than the CPL value.

Nested Mode, selected when IAM = "1", uses the same arbitration phase as concurrent mode, the difference being that the CPL is modified during the interrupt processing cycle to that of the acknowledged interrupt level. The CPL value is pushed by hardware into the Nested Interrupt Control register (NICR, R247 page 0) by setting the NICR bit corresponding to the CPL value. The interrupt service routine is entered in the normal manner. The revised CPL level is used for arbitration of further interrupts, each higher level being saved on the NICR stack, and being restored automatically by hardware with the RETI instruction. This allows the execution of the EI instruction within the interrupt service routine to operate the correct nesting of interrupts. The two modes are shown graphically in figure 16, where the Y axis shows the CPL value. It should be noted that within the concurrent mode INT1 will not be acknowledged until the CPL level is programmed to a lower level.

INTERRUPTS (Continued)

Figure 16. Interrupt Modes Example of Usage



Interrupts coming from on-chip sources at the same instant and priority level are resolved during the arbitration phase according to a hardware daisy-chain. This follows the priorities of the table 3.

Table 3. ST903X Interrupt Hardware Daisy Chain

INTA	High Priority
INTB	
INTC	
INTD	
MFTIMER0	
SCI	
A/D	
MFTIMER1	Lowest Priority

External Interrupts. Up to 8 external interrupts are available on the ST903X as alternate function inputs of I/O pins.

These may be selected to be triggered on rising or falling edges and can be independently masked. The eight external interrupt sources are grouped

Table 4. External Interrupt Channel Grouping

External Interrupt	Channel
INT7 INT6	INTD1 INTD0
INT5 INT4	INTC1 INTC0
INT3 INT2	INTB1 INTB0
INT1 INT0	INTA1 INTA0

INTERRUPTS (Continued)

into four pairs or channels which can be assigned to independent interrupt priority levels. Within each channel the even interrupt number takes the even priority level and the odd channel the odd priority level (even+1).

Several of the External Interrupt channels have their inputs selectable between the external interrupt source and on-chip peripheral sources.

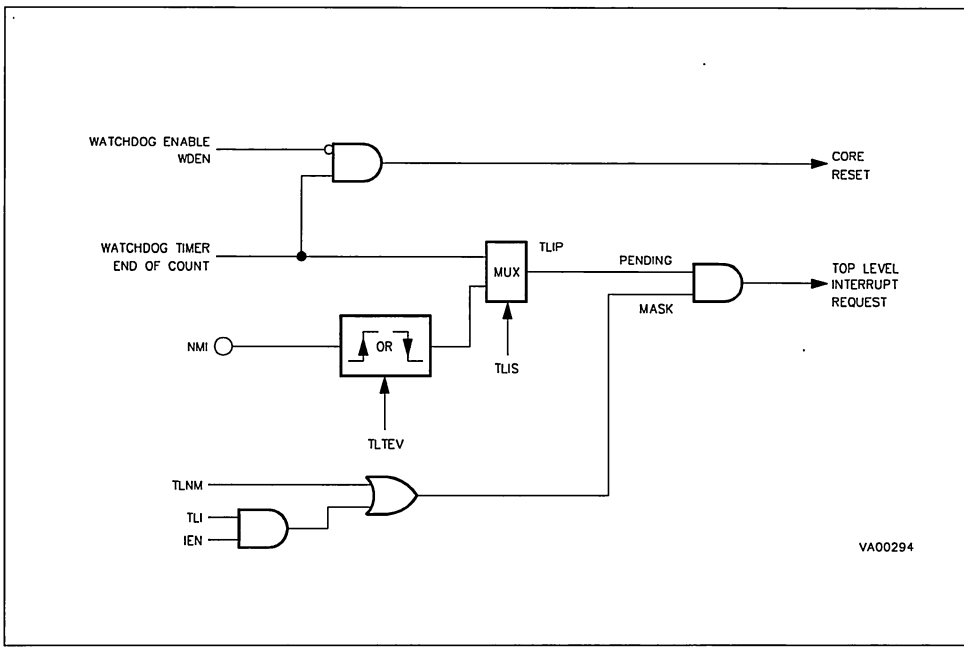
Table 5. ST903X External Interrupt Source Selection

INT0	INTA0
Timer/Watchdog End of Count	
INT2	INTB0
SPI Interrupt	

Top Level Interrupt. The Top Level Interrupt channel can be assigned either to the external NMI pin or to the Timer/Watchdog output. When selected as the external NMI pin, the active edge may be programmed to be rising or falling. The TLI event will cause the setting of the TLIP bit (CICR.6) and according to the mask situation, a Top Level Interrupt request may be generated. Two masking conditions are available, a Maskable Mask and a Not-Maskable Mask.

The Maskable Top Level Interrupt may be enabled or disabled by software and follows the state of the Global Interrupt Enable bit IEN (CICR.4), while the Not-Maskable Mask bit (TLNM) is a set-only mask. Once set, the Top Level Interrupt is active independently of IEN and cannot be disabled until the next Reset cycle.

Figure 17. Top-Level Interrupt Structure



DMA

The ST903X has on-chip DMA channels to provide high-speed data transaction between peripherals and Memory or Register File. Multi-channel DMA is fully supported because each peripheral can have its own DMA channel(s). Each DMA channel transfers data to/from contiguous locations of the Register File, Program Memory or Data Memory. The maximum number of transactions that each DMA channel can perform is 222 if the Register File is selected and 65536 if Program or Data Memory are selected.
DMA transfer to (or from) the Register File takes 8 INTCLK cycles ; DMA transfer to (or from) Memory takes 16 INTCLK cycles. If the ST903X is in the idle mode (following the execution of the `WFI` instruction), DMA requests are acknowledged according to their priority and control is returned to the idle mode pending an interrupt, this operation increases the number of INTCLK cycles by 2 for both Register File and Memory DMA transactions.

Each DMA channel has its own control registers located in the page(s) related to the peripheral.

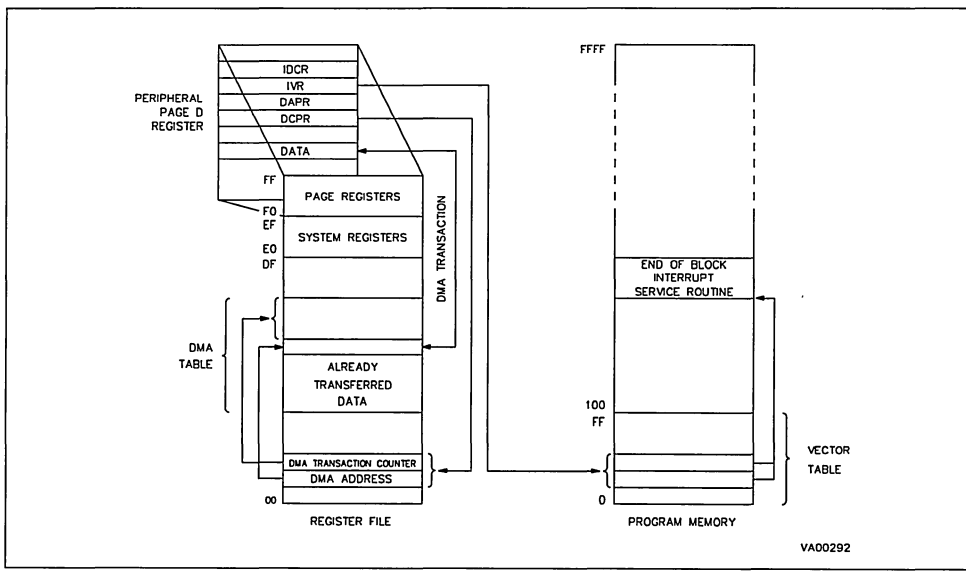
There are two pointer registers, DAPR which points to a register or register pair containing the current DMA address to/from which data will be transferred, and DCPR, which points to a register or register pair which contain the transaction counter for the DMA operations.

Each DMA transfer consists of three operations:

- A load from/to the peripheral data register to/from a location of Register File (or Memory) addressed through the DMA Address Register (or Register Pair)
- A post-increment of the DMA Address Register (or Register Pair)
- A post-decrement of the DMA transaction counter, which contains the number of transactions that have still to be performed.

When the transaction counter reaches 0 (all data has been transferred) an End of Block Interrupt event is generated to allow the processing of the DMA data block, or, by reloading the Address and counter registers and retriggering, a repeated DMA cycle.

Figure 18. DMA Between Registers and Peripheral

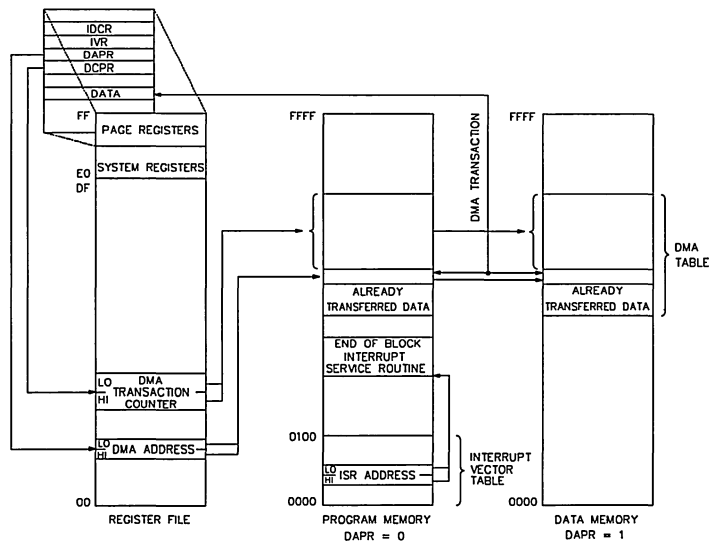


DMA (Continued)

A SWAP mode, allowing continuous DMA operation, is available for the Multifunction Timer and is described in the section relating to the Multifunction Timer.

The ST903X has DMA channels associated with the Serial Communications Interface Input and Output Serial data channels, the 16 bit Load/Capture Register 0, CAPT0R, of each Multifunction Timer allowing the timing of external signals to be captured into a table for off-line analysis or for the automatic output of PWM signals of variable width and timing, and the 16 bit Comparison Register 0, COMP0R, of each Multifunction Timer which can be programmed to cause output or input of parallel data through the handshake Port 5 under DMA.

Figure 19. DMA Between Memory and Peripheral



CLOCK GENERATION, WAIT, HALT AND RESET

Clock Generation

The ST903X Clock Generator module generates the internal clock for the ST9 core and the on-chip peripherals, it may be driven by an external quartz crystal circuit, connected to the OSCIN and OSCOUT pins, or by an external pulse generator connected to OSCIN (Figure 20, Figure 21). The conceptual schematic of the ST9 internal clock circuit is shown in Figure 22.

Figure 20. Crystal Oscillator

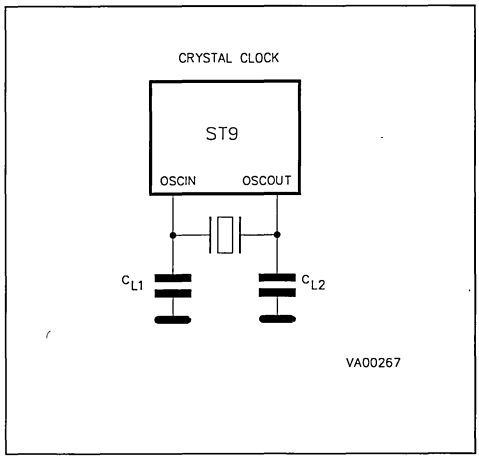


Figure 21. External Oscillator

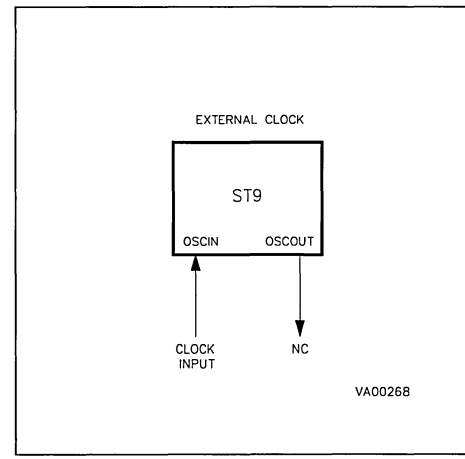
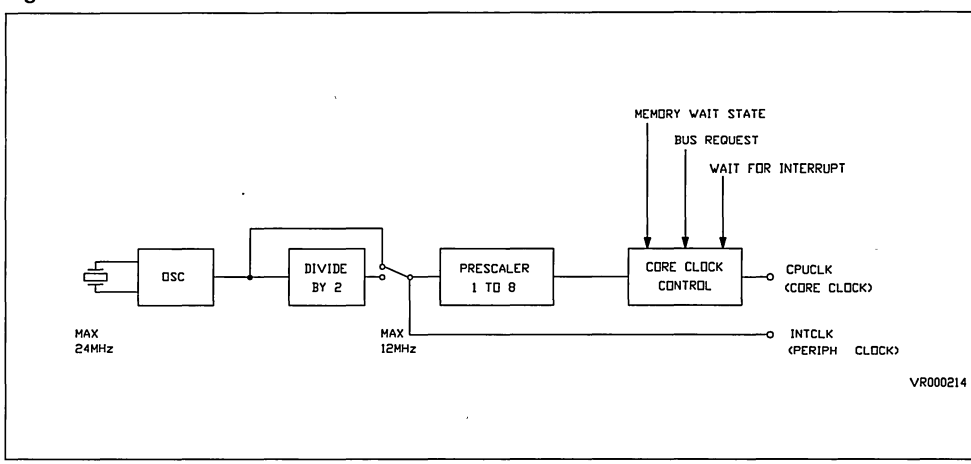


Figure 22. Internal Clock Circuit



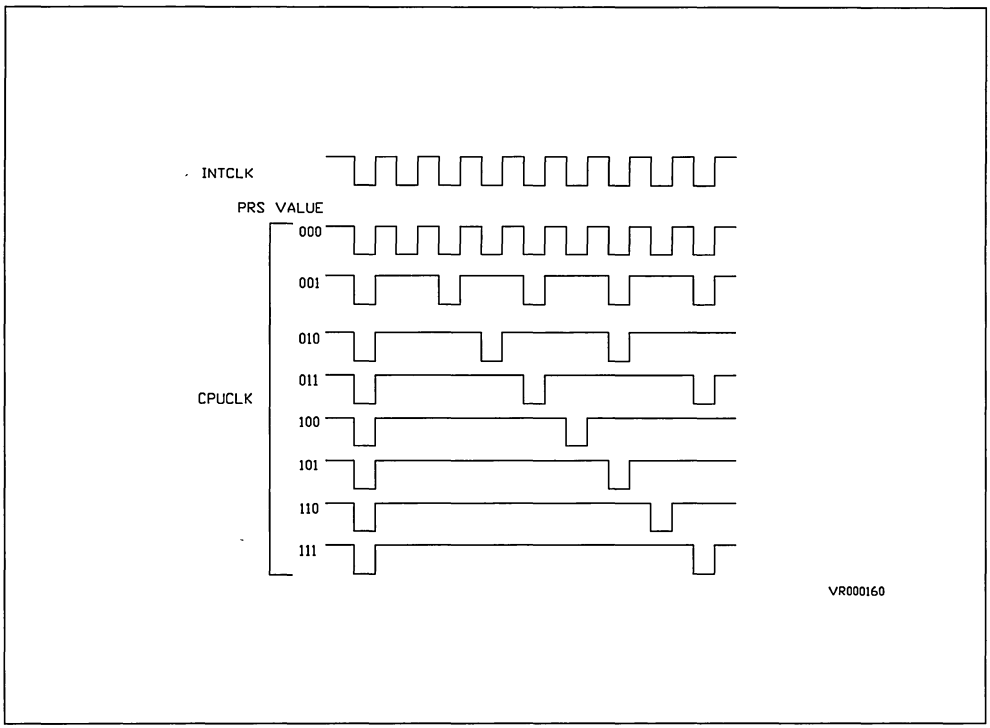
CLOCK GENERATION, WAIT, HALT AND RESET (Continued)

The maximum external frequency of the ST9 is 24 MHz, while the maximum internal operating frequency is 12 MHz, thus a programmable divide by two circuit is present, this allows the use of high frequency crystals for economy, or low frequency crystals for reduction in radiated noise. This divider is active upon exit from the reset condition, the user may bypass the divide by two circuit by setting the DIV2 bit of the MODER Register.

The resulting clock from this section is named INTCLK, the internal clock which drives the time-bases of the on-chip clock for the ST903X peripherals (eg the Multifunction Timer, Timer/Watchdog, Serial Communications Interface) and also the input of the CPU prescaler section. The CPU of the ST9 includes the instruction execution logic and may run at different rates according to the setting of the PRS2,PRS1 and PRS0 bits of the MODER Register (figure 23). The resulting clock is named CPUCLK and it should be noted that this does not maintain a 50% duty cycle, but stretches the high level of the clock until completion.

The CPUCLK prescaler allows the user to slow down the program execution time (eg for lower power consumption), while time-critical sections of the program may tune the CPUCLK execution speed to high speed and then restore it to its original speed.

Figure 23. CPUCLK Prescaler



CLOCK GENERATION, WAIT, HALT AND RESET (Continued)

Wait States

The output from the prescaler can also be affected by wait states. Wait states from two sources allow the user to tailor timing for slow external memories or peripherals.

The internal Wait State generator will insert from 0 to 7 wait states, independently programmable for both Program and Data Spaces, via the Wait Control Register WCR. The second source of wait states is the external Wait input pin when enabled as the Alternate Function. Figure 24 shows the External Memory Interface timing as it relates to CPUCLK prescaling of 2 and 5 added wait states. The added wait states are derived from the INTCLK clock cycle, not CPUCLK. Internal memory is always accessed with no Wait states.

Halt and Wait for Interrupt (WFI) States

The schematic of the on-chip oscillator circuit is shown in Figure 25. The HALT condition, caused by the execution of the HALT instruction, disables the oscillator, forcing OSCOUT high. This places the ST903X into the lowest power mode. The exit of the HALT condition and the restarting of the oscillator requires a RESET pulse with a minimum duration of 10ms (figure 26). It must be noted that if the TIMER/WATCHDOG has the WATCHDOG mode enabled, a HALT instruction will not disable the oscillator; this is to avoid stopping the Watchdog if, by an error, a HALT instruction is executed. When this occurs, the ST903X runs in an endless loop terminated only by the Watchdog reset (or hardware reset).

Figure 25. Oscillator Schematic

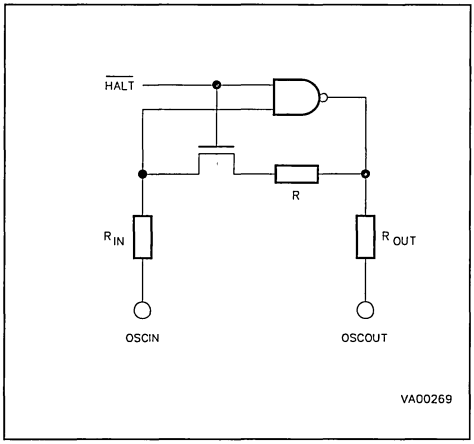
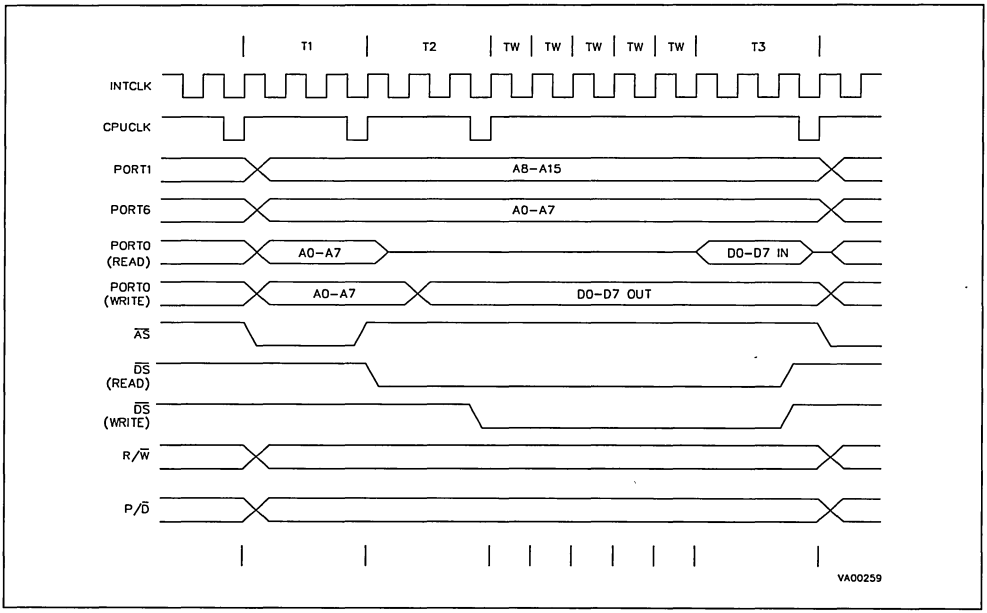


Figure 24. External Memory Interface Timing with CPUCLK Prescaling and 5 Added Wait States



CLOCK GENERATION, WAIT, HALT AND RESET (Continued)

The WFI (Wait for Interrupt) instruction suspends program execution until an interrupt request is acknowledged. During this period, DMA transactions are allowed if their priority is higher than or equal to the CPL level ; the ST903X returns to WFI mode after completion of the DMA transfer.

The CPUCLK is halted during Wait For Interrupt while INTCLK continues to run, thus the power consumption of the processor is lowered by the CORE power consumption value. The External Memory Interface lines status during HALT and WFI modes is shown in Table 6.

Table 6. External Memory Interface Line Status During WFI and Halt

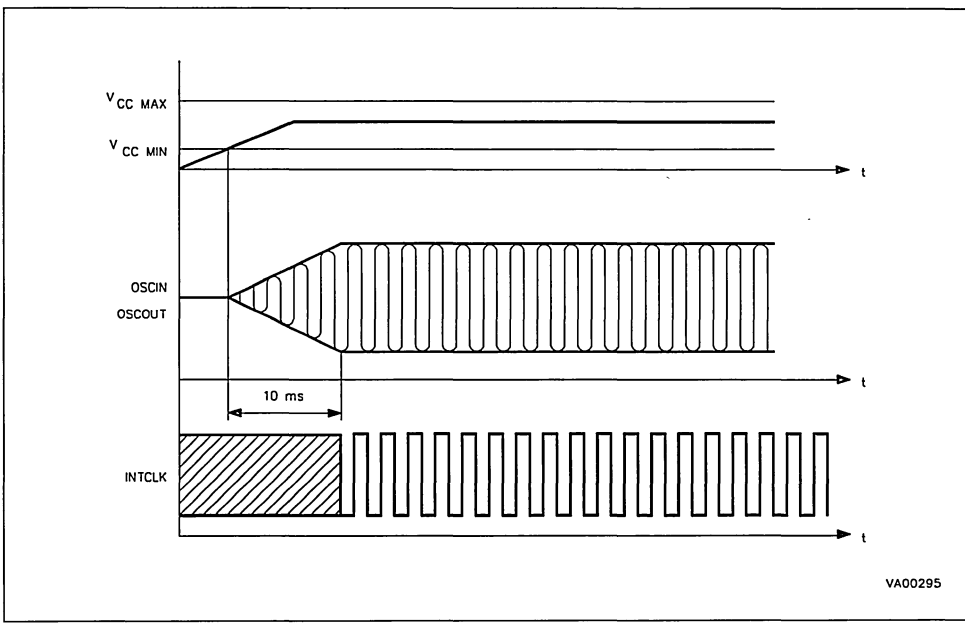
P0 (AD0-AD7)	High Impedance
P1 (A8-A15)	Forced to Address of Next Opcode
$\overline{AS}$	Forced High
$\overline{DS}$	Forced High
R/$\overline{W}$	Forced High

Reset

The processor Reset overrides all other conditions and forces the ST903X to the reset state. During Reset, the internal registers are set to their Reset values, as shown in Table 7 for the System and Page 0 Registers. The I/O Ports pins are set to the Bidirectional Weak Pull-up mode. The programmer must then initialize the ST903X registers to give the required functions.

The Reset condition can be generated from the $\overline{RESET}$ pin or by the on-chip TIMER/WATCHDOG operating in Watchdog mode. To guarantee the complete reset of the ST903X, the $\overline{RESET}$ input pin must be held low for at minimum of 53 crystal periods in addition to the crystal start-up period. The Watchdog Reset will occur if the Watchdog mode is enabled (WCR.WDEN is reset) and if the programmed period has elapsed without the code 0AAh,55h written to the appropriate register. The input pin $\overline{RESET}$ is not driven low by the on-chip reset generated by the TIMER/WATCHDOG.

Figure 26. Reset Timing Requirements from Halt State



CLOCK GENERATION, WAIT, HALT AND RESET (Continued)

Table 7. System and Page 0 Reset Values

Register Number	System Register Reset Value	Page 0 Register Reset Value
F	(SSPLR) = undefined	Reserved
E	(SSPHR) = undefined	(SPICR) = 00h
D	(USPLR) = undefined	(SPIDR) = undefined
C	(USPHR) = undefined	(WCR) = 7Fh0h
B	(MODER) = E0h	(WDTCR) = 12h
A	(Page Ptr) = undefined	(WDTPR) = undefined
9	(Reg Ptr 1) = undefined	(WDTLR) = undefined
8	(Reg Ptr 0) = undefined	(WDTHR) = undefined
7	(FLAGR) = undefined	(NICR) = 00h
6	(CICR) = 87h	(EIVR) = x2h
5	(PORT5) = FFh	(EIPLR) = FFh
4	(PORT4) = FFh	(EIMR) = 00h
3	(PORT3) = FFh	(EIPR) = 0
2	(PORT2) = FFh	(EITR) = 00h
1	(PORT1) = FFh	Reserved
0	(PORT 0) = FFh	Reserved

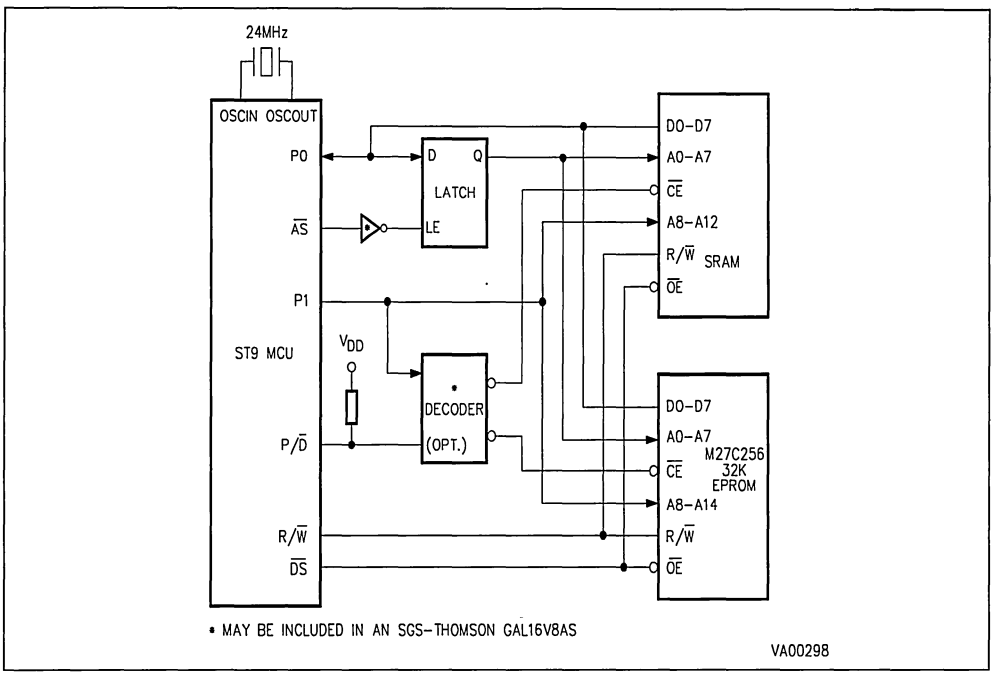
During the Reset state, $\overline{DS}$ is held low and $\overline{AS}$ is toggled with the frequency of the crystal (OSCIN) divided by 32. This condition may be recognized by external peripherals as a Reset condition. It may also be used to enable the synchronization of multiple ST903X running from the same clock in a multi-processing or high security majority voting system.

Once the $\overline{RESET}$ pin reaches a logical high, the ST903X fetches the starting address from locations 0 and 1 of the program space and begins program execution from this address after 67 crystal cycles.

INTERFACING TO EXTERNAL MEMORY

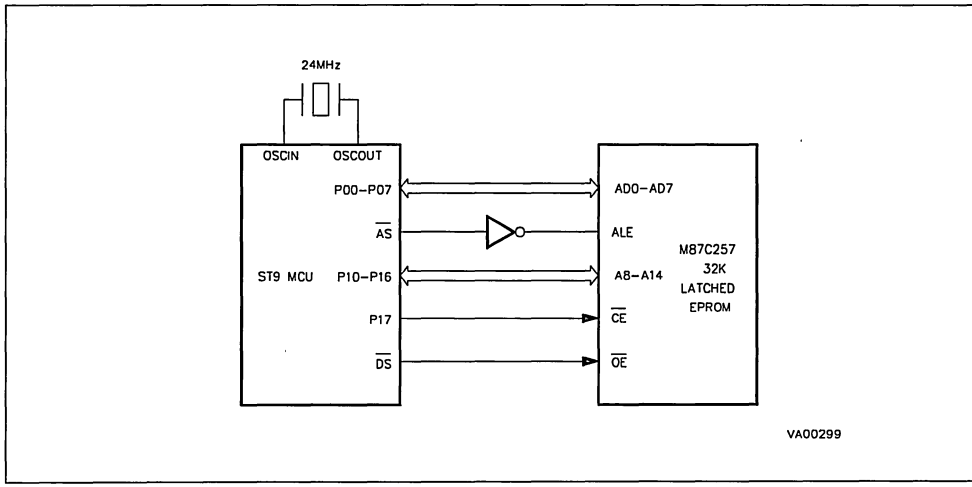
External Memory and/or peripherals may be connected to the ST903X through its External memory interface. This provides the multiplexed Address bits A0 to A7 and Data bits D0 to D7 as Alternative Functions of Port 0, and the higher order address bits A8 to A15 as Alternative Functions of Port 1, giving the full 64K bytes addressing capability. The Program/Data (P/$\overline{D}$) output, when selected as an Alternate function, allows external decoding to provide for the two independent pages of 64K bytes for Program and Data. Data transfer timing is generated by the Address strobe $\overline{AS}$ and the data strobe $\overline{DS}$. Address strobe low indicates that the data present on AD0 to AD7 is the low order address and is guaranteed valid on the rising edge of $\overline{AS}$ allowing for latching of the address bits by an external latch. Data transfer direction is indicated by the status of the Read/Write (R/$\overline{W}$) pin; for write cycles (R/$\overline{W}$ low), data out is valid at the falling edge of $\overline{DS}$; for read cycles (R/$\overline{W}$ high), data in must be valid prior to the rising edge of $\overline{DS}$. The Data Strobe low period may be extended to accomodate slow external devices by the adding of internally generated wait cycles (0 to 7 cycles for program and/or data memory maps) or by an external input on the $\overline{WAIT}$ input pin also available as an Alternative Function of an I/O bit. Suggested interface circuits are shown in Figure 27 and Figure 28.

Figure 27. External Memory Addressing Circuit



INTERFACING TO EXTERNAL MEMORY (Continued)

Figure 28. External Memory Addressing Circuit



BUS CONTROL

Multi-processing or external program testing may be accomplished by disabling the I/O ports used for external memory addressing and the associated timing signals.

High Impedance Mode

The User may place the External Memory Interface (I/O Port 0 and Port 1, Address Strobe, Data Strobe and Read/Write) into the high impedance state by setting the HIMP bit in the MODER Register. External test equipment may then drive the memory lines for automatic test, external memory validation or programming. The ST9 will continue to execute internal programs, providing no external memory is addressed, allowing the execution of security routines without showing the externally addresses used.

Bus Request/Acknowledge

The External Memory Interface address ports and timing signals may be forced to their high impedance state by utilizing the BUSREQ, Bus Request, and BUSACK, Bus Acknowledge, signals available as Alternate Functions of two I/O pins (please refer to the pin configuration drawings for availability of these lines for the package chosen). The signals, BUSREQ and BUSACK, must be enabled by setting the BRQEN bit in the MODER register. Once enabled, a low level detected on the BUSREQ pin at the start of an internal machine cycle will cause the stretching of the CPUCLK, and BUSACK to go low indicating that the External Memory Interface is disabled. The BUSREQ pin is then continuously monitored, and when sampled high, the External Memory Interface pins are driven by the ST9 within two INTCLK cycles.

I/O PORTS

Summary of Function

For each package type of the ST903X, only ten pins have a Reserved function: Vdd, Vss, $\overline{RESET}$, $\overline{AS}$, $\overline{DS}$, R/$\overline{W}$, OSCIN, OSCOUT, the Analog to Digital Converter Voltage references, plus, depending on package type, the External Interrupt 0 and 7 input pins. All other pins are available as Input/Output (I/O) for the user, grouped into Ports of 8 bits.

These may be programmed to be Input, Output, Bidirectional or Alternate Function (Peripheral or Memory Interface), on a bit by bit basis, at any time. When programmed as an Input the pin may be set to TTL or CMOS input threshold levels, while, when programmed as Output, Push-Pull or Open Drain configuration may be selected. The Bidirectional mode sets the pin with a weak pull-up resistor to Vdd or to Open Drain, allowing bidirectional communication with external logic. The Alternate Function setting is predetermined for each pin as shown in the Pin Configuration Table. The circuitry of the I/O port allows for several ST903X peripheral functions to address, as Alternate Functions, the same pin, for both input and output, the programmer selects which peripheral function is to be active by enabling its individual Input or Output function. This multi-function I/O capability of the ST903X allows for easy adaptation to external circuits. The options available for each bit are summarized in Table 8.

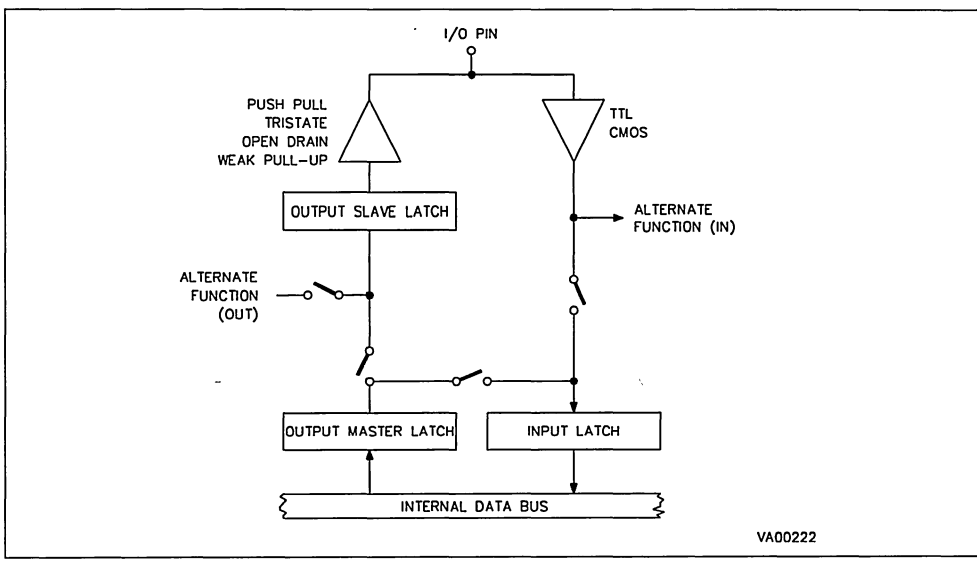
Table 8. I/O Port Schematic

Input	TTL Thresholds
	CMOS Thresholds
Output	Open Drain
	Push-Pull
Bidirectional	Open Drain
	Weak Pull-up
Alternate Function	Open Drain
	Push Pull

I/O Port Configuration

The configuration of each general I/O bit of the ST903X is set by the corresponding bits in three I/O Port control registers. These affect the status of the input and output buffers of the pin, and enable the Alternate function Outputs. Alternate Function inputs are always connected, and are used by enabling the function from within the configuration registers of the relevant peripheral function. The configuration of an I/O bit is shown in Figure 28. Outputs follow a Master/Slave buffer, data is transferred from the ST9 internal data bus at the beginning of the machine cycle, and, if enabled as output, is passed to the output latch at the end of the cycle. This synchronization allows for the Bidirectional use of the pin without potential conflicts (see Figure 29).

Figure 29. I/O Port Schematic



I/O PORTS (Continued)

Configuration Registers. Three registers are used to allow the setting of each pin, generically PxC2, PxC1, PxC0, where x relates to the 8 bit I/O port in which the bit is present. The setting of the corresponding bit in each register to achieve the desired functionality of the I/O pin is shown in Table 9.

The effect of the configuration settings of Table 9 on the I/O ports structure is shown in Figures 30 to 33.

Table 9. Port Configuration Status Bits

PxC2n	0	1	0	1	0	1	0	1
PxC1n	0	0	1	1	0	0	1	1
PxC0n	0	0	0	0	1	1	1	1
Pxn Configuration	BID	BID	OUT	OUT	IN	IN	AF	AF
Pxn Output	WP	OD	PP	OD	HI	HI	PP	OD
Pxn Input	TTL	TTL	TTL	TTL	CMOS	TTL	TTL	TTL

Legend:
x = Port
n = Bit
BID = Bidirectional
OUT = Output
IN = Input
AF = Alternate Function
WP = Weak Pull-up
OD = Open Drain
PP = Push-Pull
HI = High Impedance

Figure 30. I/O Port Input Configuration

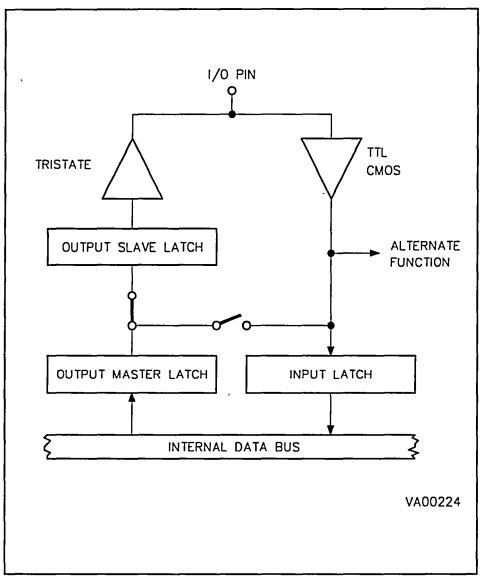
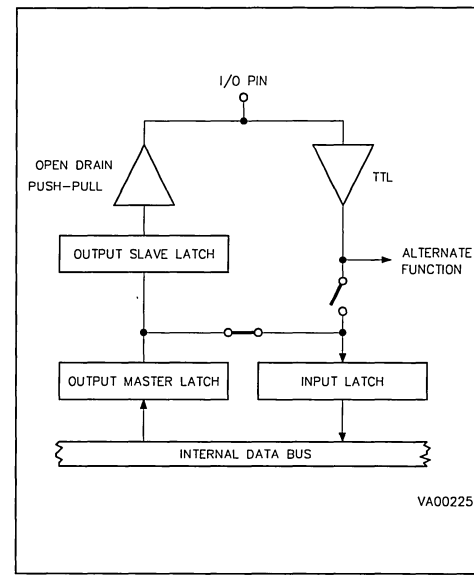


Figure 31. I/O Port Output Configuration



I/O PORTS (Continued)

Figure 32. I/O Bidirectional Configuration

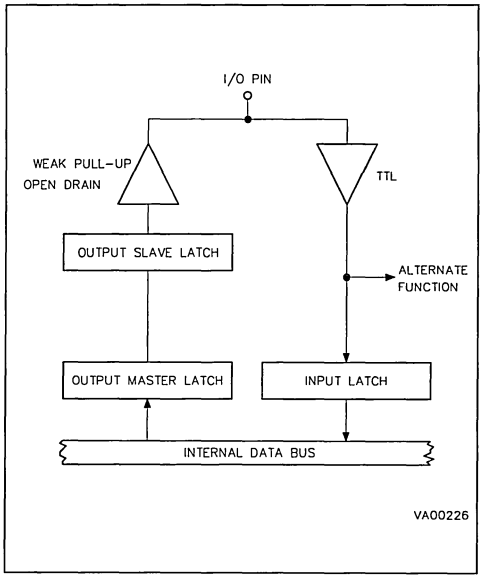
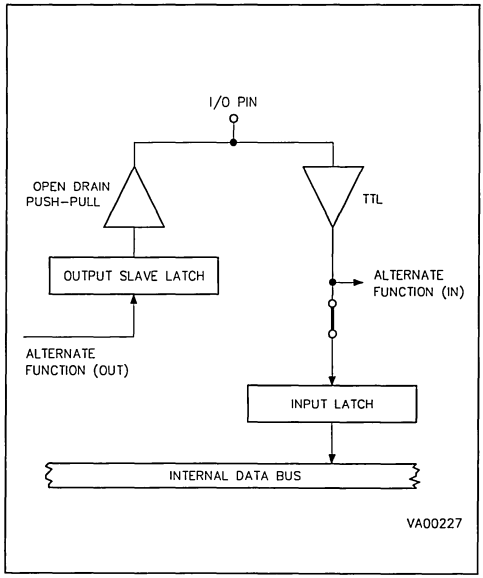


Figure 33. I/O Port Alternate Function Config.



I/O Register Map

The Data Registers which correspond to the pin status (after configuration) of I/O Port 0 to Port 5, are found in Group E of the Register File, for immediate access at all times, while the configuration registers and the Data Registers for Additional Ports are found within I/O pages (Group F) 2 and 3.

Figure 34. I/O Register Maps

GROUP E			GROUP F		PAGE	
DEC	HEX		DEC	HEX	02	03
			R255	RFF	RESERVED	P7D
			R254	RFE	P3C2	P7C2
			R253	RFD	P3C1	P7C1
			R252	RFC	P3C0	P7C0
			R251	RFB	RESERVED	RESERVED
			R250	RFA	P2C2	RESERVED
			R249	RF9	P2C1	RESERVED
			R248	RF8	P2C0	RESERVED
			R247	RF7	RESERVED	HDC5
			R246	RF6	P1C2	P5C2
R229	RE5	P5D	R245	RF5	P1C1	P5C1
R228	RE4	P4D	R244	RF4	P1C0	P5C0
R227	RE3	P3D	R243	RF3	RESERVED	RESERVED
R226	RE2	P2D	R242	RF2	P0C2	P4C2
R225	RE1	P1D	R241	RF1	P0C1	P4C1
R224	RE0	P0D	R240	RF0	P0C0	P4C0

I/O PORTS (Continued)

Handshake and DMA

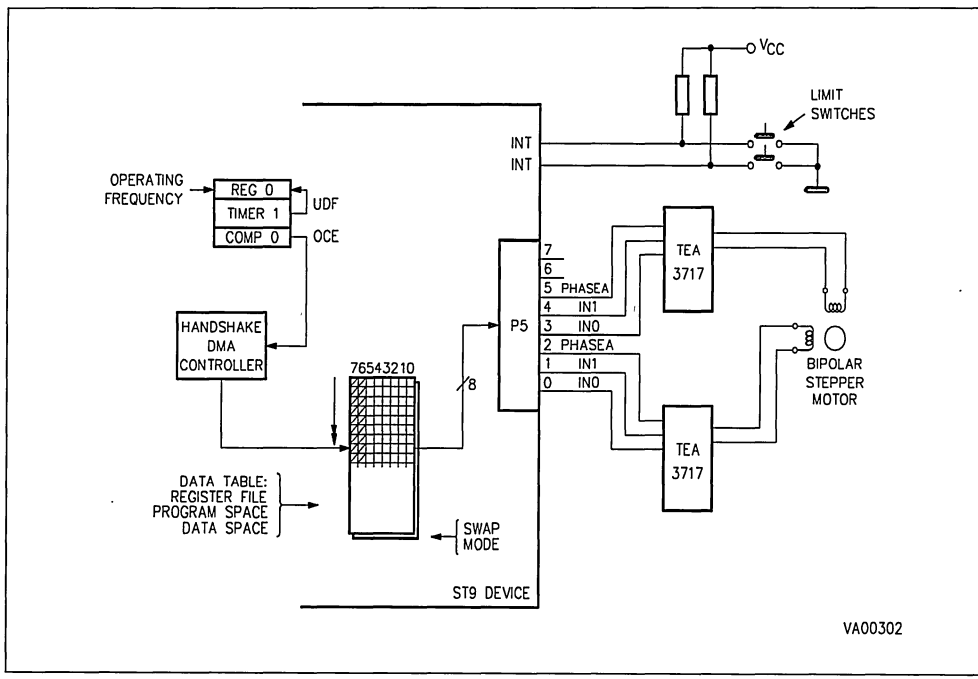
I/O Port 5 of the ST903X (please refer to the pin configuration table for the availability of all 8 bits of Port 5, as this is dependent on the package type) is able to support a parallel interface port with handshake capability. This allows one, two or four wire interconnecting handshake signals and facilitates very fast parallel transfer of data for input and output, or for the interconnection of peripheral devices requiring strobe signals for synchronization. Table 10 shows the available options for input and output status and strobe signals available as Alternate Functions of I/O port bits (see Pin Configuration). The Handshake configuration is set within the Handshake Control Register (HDCnR) for the relevant I/O port n.

Data transfer through the parallel I/O port with handshake can also be triggered through a DMA channel. Timing is generated by the ST903X TIMER ON-CHIP EVENT strobe signal (see the TIMER section for information on generating these signals), which causes the programmed transfer of data to or from the memory source which can be Register File, Program space memory or Data space memory. An example of application of this technique is shown in Figure 35, a complex stepper motor timing sequence automatically being transferred from a table in the Register File (or memory spaces) to the stepper motor drivers. After initialization, this operation is transparent until the task (complex microstepping) is completed.

Table 10. Handshake Control Signal Options

Mode	Handshake Lines	Names
Input to Port	1	WRRDY
	2	$\overline{\text{WRSTB}}$ WRRDY
Output from Port	1	RDRDY
	2	$\overline{\text{RDSTB}}$ RDRDY
Bidirectional	4	$\overline{\text{WRSTB}}$ WRRDY $\overline{\text{RDSTB}}$ RDRDY

Figure 35. Handshake + DMA Used for Stepper Motor Driving



TIMER/WATCHDOG

A 16 bit down-counter, complete with 8 bit prescaler, is integrated into the ST903X core. This is able to operate both as a general purpose timer with associated input and output pins for timing functions, and also as a Watchdog Timer offering a security against possible processor malfunctions due to external events.

Timer Modes

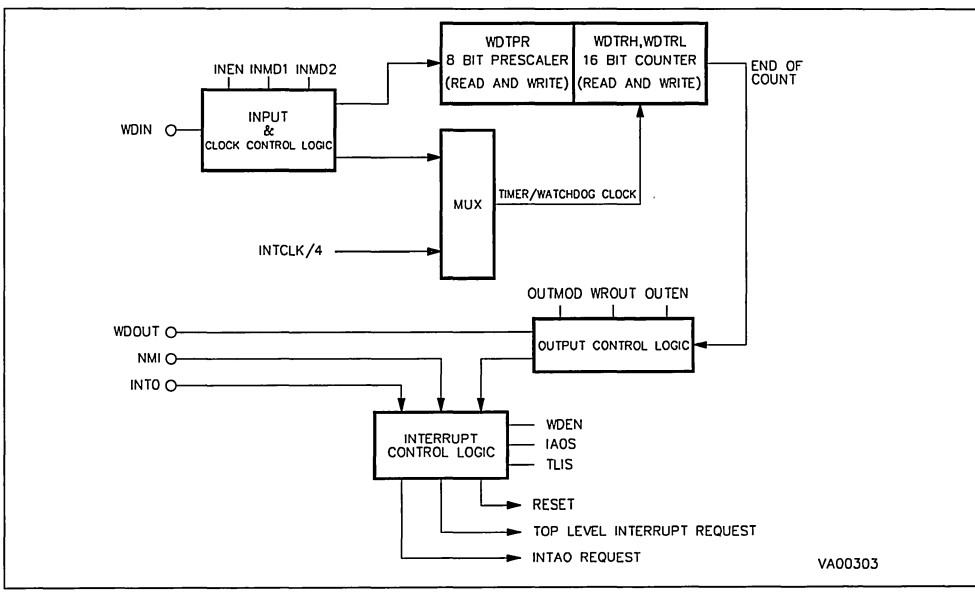
When operating as a Timer, with a timing resolution from 333ns to 5.59s (INTCLK = 12MHz), an input pin (WDIN) and output pin (WDOUT) may be selected as the Alternate Functions of two I/O pins. When WDIN is enabled by the user by setting INEN high and the Alternate Function is set, 4 operating modes are available: The WDIN input may be programmed to act as an event counter input, with high to low transitions causing the counter to decrement. The time duration between the falling edges of the input clock must be at least 333ns (allowing a maximum input frequency of 3MHz). It may also be used for pulse width measurement by being selected as a counter clock gate signal (prescaler to the counter being driven by INTCLK/4), counting being enabled when WDIN is at a high level. Trigger and Re-trigger modes cause a reload of the timer user preset values (START/STOP is active) for a high to low transition on WDIN at any time (Re-trigger mode) or when the counter is at the end of count (Trigger mode). The counter decrements at a rate driven by INTCLK/4.

The WDOUT pin, when set as the Alternate Function, is enabled by OUTEN high, and may either toggle the state of the I/O bit (frequency generation, OUTMD = "0") or pass the state of the WROUT bit to the output allowing PWM generation (OUTMD = "1") at the end of count (Timer value = 0) condition.

Watchdog Mode

The timer functions may be disabled, and the Timer configured for a Watchdog operation by re-setting WDGEN to zero. Once the Watchdog has been selected it cannot be set back into the standard timer mode until the next Hardware Reset cycle. The programmer should set the watchdog timer prescaler and timer reload value before enabling the Watchdog mode. The Watchdog Timer must then be retriggered, causing the reloading of the timer value, by the operation of writing of the byte sequence 0AAh, 055h to the WDTRL register. If this is not done before the Watchdog counts to zero, the Watchdog Timeout condition occurs. This causes a Hardware Reset of the ST903X. The Watchdog reset signal is not output on the external $\overline{\text{RESET}}$ pin.

Figure 36. Timer/Watchdog Block Diagram



TIMER/WATCHDOG (Continued)

Timer/Watchdog Interrupts

The Timer/Watchdog may provide several levels of interrupts selectable by the programmer.

The Timer mode offers two interrupt sources, triggered on the timer value reaching 0, either a prioritized level (by taking the Interrupt priority channel from the External Interrupt INTA0) or by a top level, non-maskable interrupt (taking the external NMI input channel).
The interrupt channels are multiplexed from the alternative source according to the status of the IAOS and TLIS bits as shown in figure 38. Please refer to the ST9 Technical Manual for further details on changing the interrupt sources of the Timer/Watchdog.When the Watchdog mode is set (WDEN = "0"), the timer value equal to 0 event generates a Hardware reset of the ST903X. The Timer/Watchdog control registers are located within Page 0 of the Paged I/O register group.

Figure 38. Timer/Watchdog Interrupt Sources

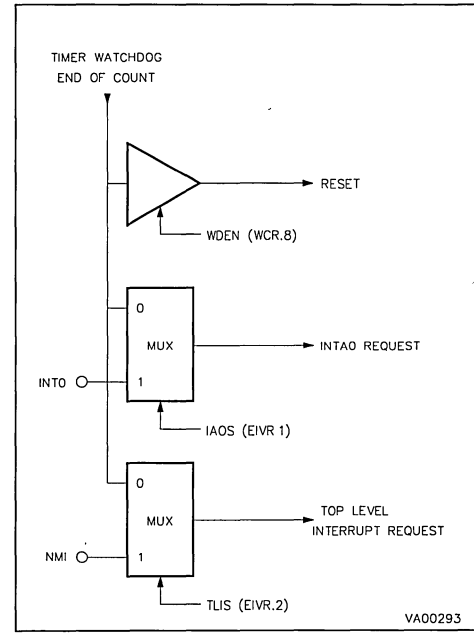
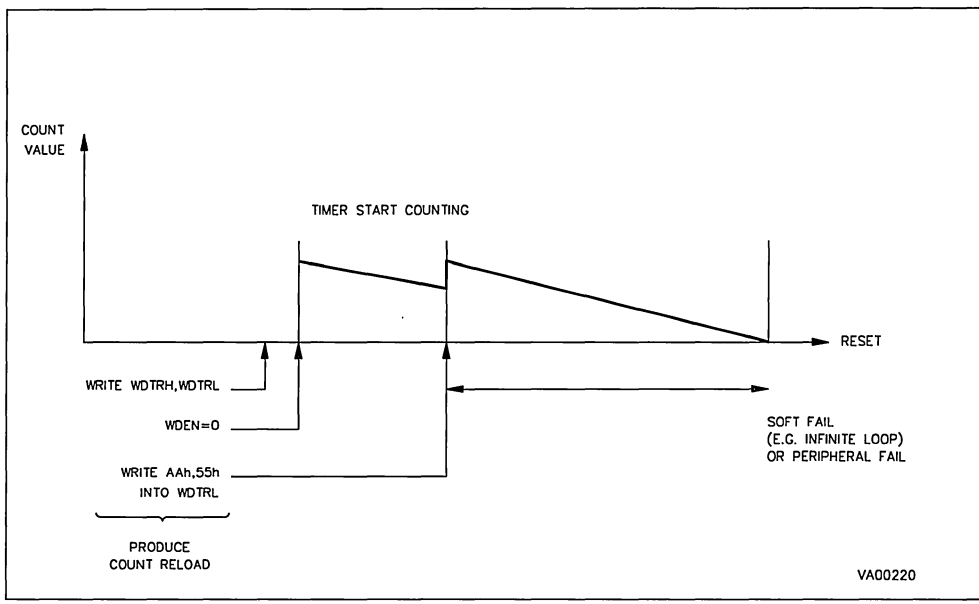


Figure 37. Timer/Watchdog in Watchdog Mode



MULTIFUNCTION TIMER

The ST903X includes two identical 16 bit Multifunction Timers (MFT) in addition to the TIMER/WATCHDOG. The following description applies to both Timer 0 and Timer 1.

Each timer is a 16 bit Up/Down counter, driven by the output of an 8 bit prescaler which may be driven by INTCLK/3 (giving a minimum timing resolution of 250ns at INTCLK = 12 MHz) or by an external source. This timer is supported by two 16 bit Comparison Registers for generating timed functions and two 16 bit Capture/Load Registers for timing and variable timebase functions. These features coupled with 2 input pins (TxINA and TxINB) and 2 output pins (TxOUTA and TxOUTB, where x = 0 or 1), available as Alternate Functions, giving the timer 13 operating modes for virtually all required timing functions.

MFT Operating Modes

The operating modes selected by the programming of the Timer Control Register (TCR Timer x) and the Timer Mode Register (TMR) are as follows:

One-Shot Mode. The counter stops at the End Of Count Condition (up or down count).

Continuous Mode. At End Of Count the timer is reloaded from a Load Register.

Trigger Mode. A Trigger causes reload from a load register only if the Timer is at End of Count.

Retrigger Mode. A Trigger causes reload from a load register at any time.

Gate Mode. Counting is performed only when the external gate input (TxINA or TxINB) is active (logical 0).

Capture Mode. A Trigger causes the timer value to be latched into the selected Capture register.

Up/Down Mode. A Trigger causes a count up or down, or a change in counting direction.

Free-Running Mode. Up or Down counting is performed to the full range with no action at End of Count. This is used in Bicapture and Capture Modes.

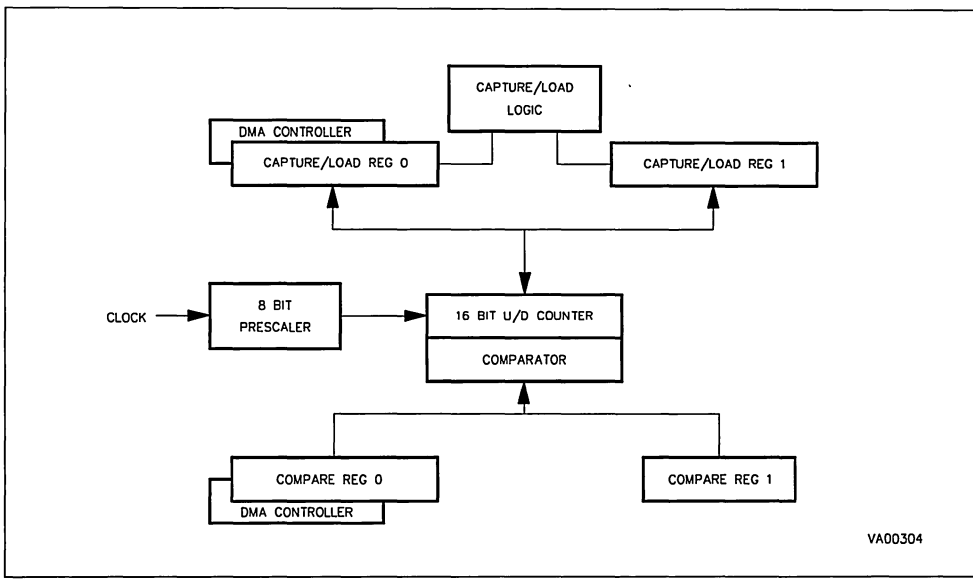
Monitor Mode. One Capture register follows the contents of the timer.

Autoclear Mode. The timer is reset to 0000h or FFFFh (up or down count respectively) on a trigger. This gives delta time measurement or free running with a modulo of less than 2^{16}.

Biload Mode. The counter is reloaded on an End Of Count condition alternately from the two Load Registers. (PWM output).

Bicapture Mode. A Trigger causes the current timer value to be transferred alternately to the two Capture registers (pulse width measurement).

Figure 39. Multifunction Timer Block Diagram



MULTIFUNCTION TIMER (Continued)

Parallel Mode. The prescaler output of Timer 0 is internally connected to the input of the prescaler of Timer 1, if this is then set to 00h (= divide by 1), then the two timers may be run in parallel.

The trigger events may be either caused by software, or an action on the two input pins which may be programmed to respond to rising, falling or both edges of the input. The input modes are selected in the Input Control Register (ICR) as shown in Table 11.

This includes the Autodiscriminator mode, which causes the timer to count up or down depending on the phase between the two input edges, such as the signals generated by optical encoders.

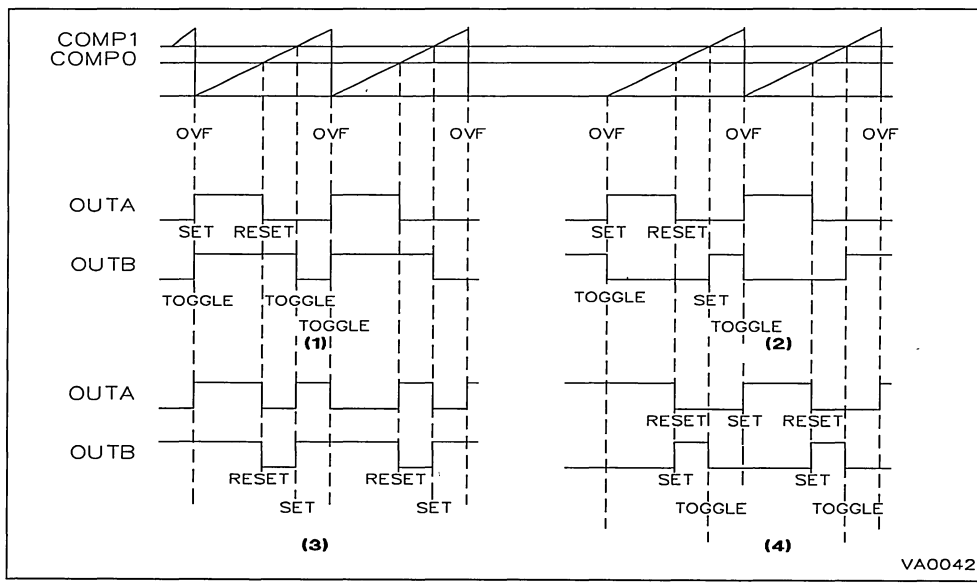
The two output pins (available as Alternate Functions) may be programmed through the Output Control Registers OCR0 and OCR1 to be modified (Set, Reset, Toggle or No Operation) on each of Overflow/Underflow (OVF/UNF), Compare on CMP0 valid (CM0), or Compare on CMP1 (COMP1) valid events.

This allows repetitive signals such as PWM drive to be output with minimum CPU overhead. Figure 40 shows some typical waveforms available from these signals.

Table 11. Input Pin Function Settings

Input Control Register IN3-IN0 bits	TxINA Input Function	TxINB Input Function
0000	I/O	I/O
0001	I/O	Trigger
0010	Gate	I/O
0011	Gate	Trigger
0100	I/O	Ext.clock
0101	Trigger	I/O
0110	Gate	Ext.clock
0111	Trigger	Trigger
1000	Clock Up	Clock Down
1001	Up/Down	Ext.clock
1010	Trigger Up	Trigger Down
1011	Up/Down	I/O
1100	Autodiscr.	Autodiscr.
1101	Trigger	Ext.clock
1110	Ext.clock	Trigger
1111	Trigger	Gate

Figure 40. Example Output Waveforms



MULTIFUNCTION TIMER (Continued)

The Overflow/Underflow event and the Compare 0 event may also be programmed to give On-chip Event timing signals to trigger other peripheral operations on the ST903X. These are as shown in Table 12.

Table 12. ST903X On-Chip Event Setting

MFT0	A/D Conversion Trigger
MFT1	Handshake Trigger Port

The TxOUTA and TxINA lines for each timer may be connected together internally, by setting of the SCx bits of the I/O Connection Register (IOCR).

The Multifunction Timers are enabled for counting by the Counter Enable bit (CEN, TCR.7) of the respective timer unit. When CEN is low, both prescaler and timer are halted. CEN is logically ANDed with the Global Counter Enable bit (GCE, CICR.7), so that both timers may be started in synchronism, i.e. when the timers are set into Parallel mode, this allows initialization of both Timers before triggering at the same instant.

MFT Interrupts

Each Multifunction Timer can generate interrupt requests from 5 different interrupt sources which are grouped into 3 independent groups.

The Interrupt Vector has the source of the interrupt group encoded by hardware into the least significant 3 bits of the vector. This allows the programming of the base address to an 8 byte block within the interrupt vector area of the Program Space. The groups and respective addresses are shown in Table 13.

Table 13. MFT Interrupt Vectors

Interrupt Source	Vector Address
COMP0 COMP1	xxxx x110
CAPT0 CAPT1	xxxx x100
Overflow/Underflow	xxxx x000

Each source may be independently masked, in addition all Timer interrupts may be disabled by the Global Timer Interrupt enable (GTIEN, IDMR.7) control bit. If a Timer interrupt on Compare 0 or Capture 0 does not have its corresponding pending bit reset before the next interrupt, then an overrun condition occurs. This condition is flagged in two dedicated overrun bits in the Timer FLAGS register.

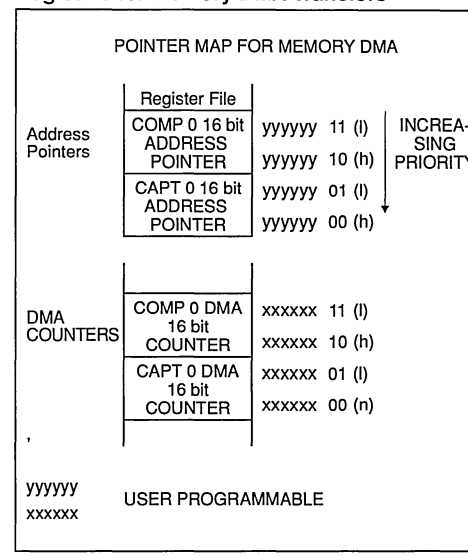
MFT DMA Channels

Two independent DMA channels are present within each MFT, associated to the Compare 0 and Capture 0 sources. This allows 16 bit DMA transactions from Register File/Memory to COMP0 registers, and from CAPT0 registers to Register File/Memory. The DMA channels allow the capture of external event timings in memory allowing off-line analysis, and creating of variable pulse width signal trains, as required by the drive of Triacs in certain modes.

The two interrupt mask sources are independently masked by two DMA mask bits, mapped in the IDMR register. The End of Block (EOB) procedures are as described in the INTERRUPT/DMA section.

The DMA counter and address pointer registers share the most significant user-programmable 6 bits for both DMA channels (COMP 0 and CAPT 0), thus the mapping of the counter and address registers use automatic offsets from the base address. The actual mapping changes dependent on whether the Register File or Memory is addressed for the transfer. The offsets are shown in Table 14.

Table 14-1. MFT DMA Address and Counter Registers for Memory DMA Transfers



MULTIFUNCTION TIMER (Continued)

Table 14-2. MFT DMA Address and Counter Registers for Register File DMA Transfers

POINTERS FOR REGISTER FILE DMA			
8 Bit COUNTER	xxxxxx	11	COMPARE 0
8 bit ADDR. POINTER	xxxxxx	10	
8 bit COUNTER	xxxxxx	01	CAPTURE 0
8 bit ADDR. POINTER	xxxxxx	00	
xxxxxx	USER PROGRAMMABLE		

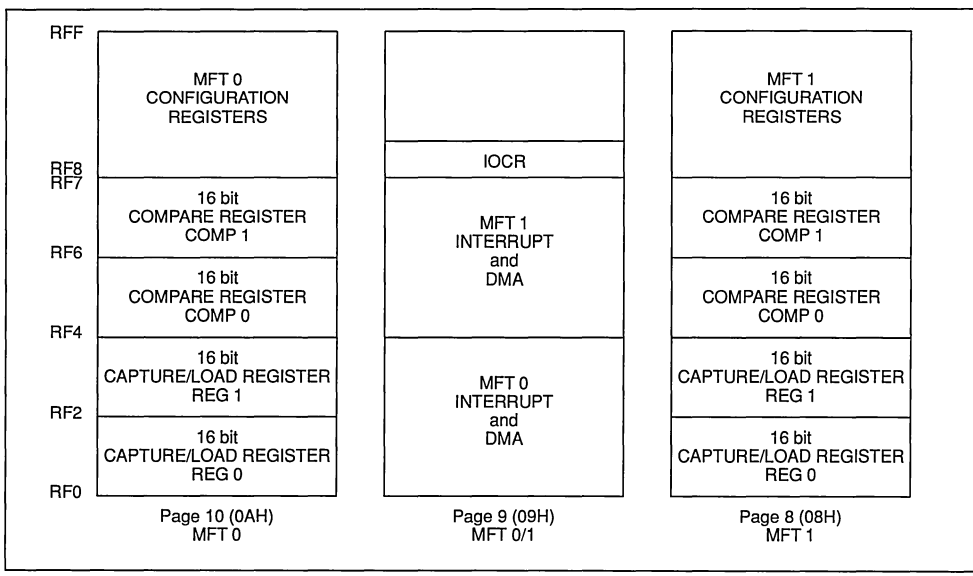
After the transfer of the complete block of data to/from the MFT, the count registers reach the zero value and an end of block interrupt occurs so that the ST9 may process the new data. In many cases, the time taken to reload the data tables and to re-trigger the DMA action causes speed limitations, especially in those applications requiring a continuous high speed data flow, because of the time consumed by the restore routine. An additional DMA function, the SWAP mode, overcomes this limitation. This is enabled by the setting of the SWEN (IDCR.3) bit.

This causes hardware generated signals to replace the user address bit 2 of both the address and counter pointers. The address and counter registers are thus duplicated at an offset of 4 registers. At the End Of Block condition, the EOB interrupt is generated to signal the end of DMA, and the state of pointer address bit 2 toggles state automatically and the new address and count values are used. Thus the ST9 can safely process the previous block of data while the new block is being transferred. This will continue until the SWAP mode is disabled. A software protection scheme is implemented to prevent non-updated pointer registers from being used if a second EOB interrupt arrives during the servicing of the first. This mechanism locks the state of the DMA mask bit to prevent further transfers from taking place. The user should check for this condition in the EOB routine to ensure that all the DMA transfers are properly serviced.

The control Registers of each MFT occupies 20 registers within the I/O paged area. These are mapped as shown in Figure 41:

In addition the MFT is able to trigger byte DMA transfers in both directions through an I/O port with Handshake (see I/O Handshake and DMA).

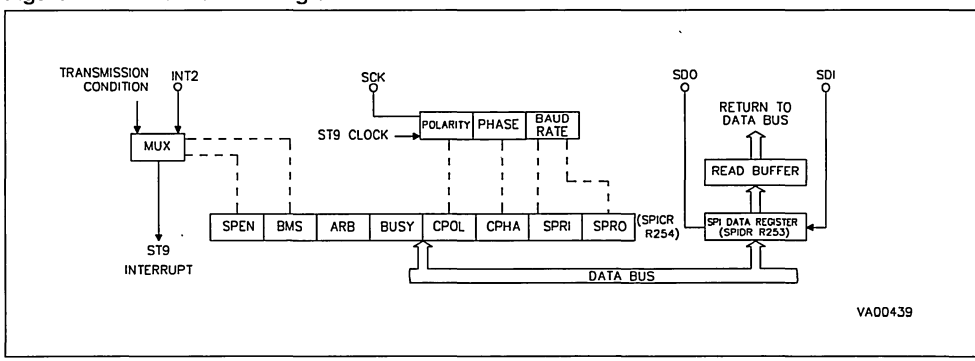
Figure 41. Multifunction Timer Page Maps



SERIAL PERIPHERAL INTERFACE

The Serial Peripheral Interface (SPI) is integrated into the Core module of the ST9 and provides a general purpose shift register based peripheral allowing synchronous serial I/O, with special modes allowing compatibility with I^2C-bus and IM Bus Communication standards in addition to the standard serial bus protocol. The SPI uses 3 lines comprising Serial Data Out (SDO), Serial Data In (SDI) and the Synchronous Serial Clock (SCK) which are available as Alternate Functions of I/O pins. Additional I/O pins may act as device selects or IM Bus address ident signals. The functional diagram of the SPI is shown in figure 42.

Figure 42. SPI Functional Diagram



The SPI (when enabled, SPEN high) receives input data from the ST9 internal data bus into the SPIDR, and originates the SCK to shift the data serially through SDO (Most Significant bit first) to the slave device which responds by sending data to the master device via the SDI pin. This implies full duplex transmission with both data-out and data-in synchronized with the same clock signal. Thus the byte transmitted is replaced by the byte received, eliminating the need to separate "Tx Empty" and "Rx full" status bits. After the 8 clock cycles have been concluded, the received data in SPIDR is parallel transferred to the read buffer and data becomes available for the ST903X during the next read cycle of SPIDR. The TXBUSY bit is set when transmission is in progress, this allows the user to monitor the status of the SPI by polling of this bit.

The SPI can operate only in master mode, i.e. the clock is always generated by the ST903X, however the SCK polarity and phase can be programmed to suit all peripheral requirements (Figure 43). This, together with the 4 programmable bit rates (divided from the INTCLK, Table 15, provide the large flexibility in handling different protocols.

SERIAL PERIPHERAL INTERFACE (Continued)

Figure 43. SPI Data and Clock Timing

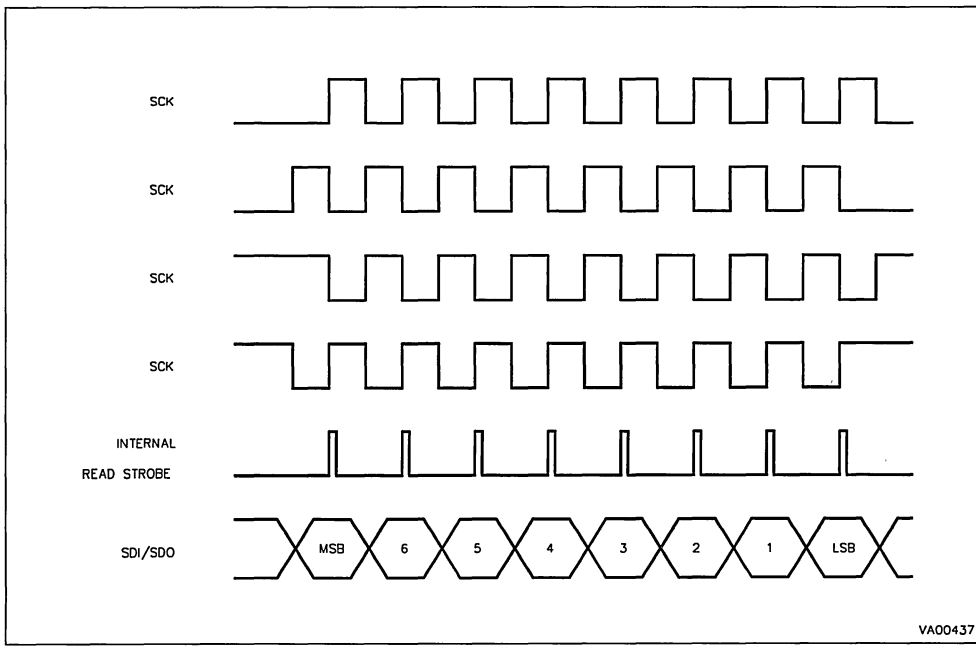


Table 15. SPI Rate Selection

SPR1	SPR0	Clock Divider	SCK Frequency (INTCLK = 12 MHz)
0	0	8	1500 KHz (T= 0.67 µs)
0	1	16	750 KHz (T= 1.33 µs)
1	0	12	93.75 KHz (T= 10.66 µs)
1	1	256	46.87 KHz (T= 21.33 µs)

I²C-bus Compatibility

The SPI includes additional circuitry to enable the use of external I²C-Bus peripherals. The I²C-Bus mode is a 2 wire bus while the SPI operates with 3 wires, however wire-ANDing SDO and SDI gives the required signalling, while setting the BMS bit causes the enabling of the special I2C-bus features: Clock Slowdown by external devices and Arbitration Lost detection. This mode also affects the Interrupt sources as shown in the next section.

SPI Interrupts

The SPI, when enabled, uses the INT2 external interrupt channel source, using the priority selected for INT2 within the External Interrupt Priority registers. The INT2 mask bit should be set and INT2 pending bit reset before enabling the SPI through SPEN. The BMS and SPEN bits select the SPI internal interrupt source as shown in Table 16.

Table 16. SPI Interrupt Sources

SPEN	BMS	Interrupt Source
0	0	External channel INT2
0	1	S-BUS/I²C bus start or stop condition
1	X	End of one byte transmission

SPI Registers

The two registers controlling the SPI are located in I/O page 0, the Data Register, SPIDR, at R253 and the control register, SPICR, at R254.

SERIAL COMMUNICATIONS INTERFACE

Function

The Serial Communications Interface (SCI) of the ST903X offers a means of full-duplex serial data transfer to a wide range of external equipment with its fully programmable character format control for asynchronous and byte synchronous serial I/O, integral Baud Rate Generator, giving a maximum baud rate of 375K Baud in Asynchronous mode (Internal Clock), and two DMA channels for transparent transmission and reception of characters. Support is also present in hardware for Line Break Detection and generation, character search, network interfacing with 9th bit Address logic, and Local Loop Back and Auto echo modes for Self-Test. The control registers for the SCI exist within one I/O page within the I/O page group.

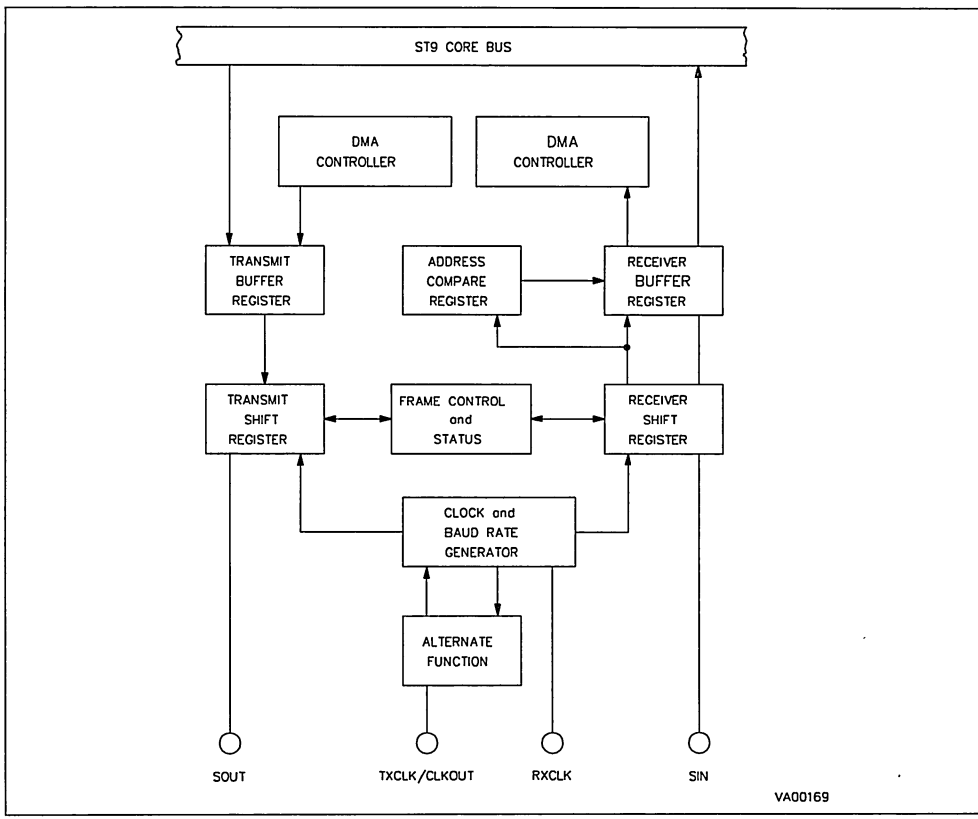
Character Formats

When used for asynchronous character transmission and reception, the character format may be changed (through the Character Control Register CHCR) to suit external equipment requirements. This is summarized in Figure 45.

The baud rate clock for asynchronous mode should be set to the ÷ 16 Mode and the frequency of the clock input (from an external source or the internal baud-rate generator output) set to suit this.

This format control is also available for the byte synchronous mode (Clock divider set to ÷ 1), when the data and clock are output in synchronism, the data being sampled once per clock period (Figure 46). For a second synchronous mode, CLKOUT is activated only for the data section of the word (figure 47) on serial data output, and input data is latched

Figure 44. SCI Functional Block Diagram



SERIAL COMMUNICATION INTERFACE
(Continued)

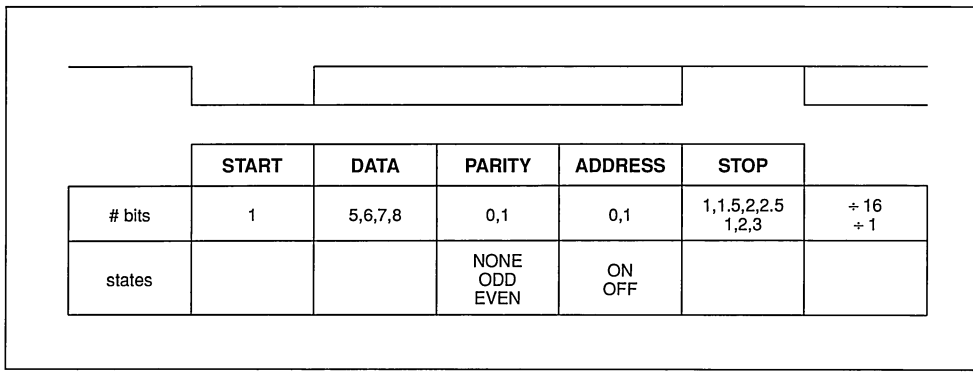
on the rising edge of the external synchronised clock input on the RXCLK pin. This mode may be used to access external synchronous peripherals.

The Address bit/D9 is optional and may be added to any word format, it is commonly used in network or machine control applications. When enabled (AB = "1"), an address or ninth data bit can be added to a transmitted word by setting the Set Address bit (SA). This is then appended to the next word entered into the (empty) Transmitter Buffer Register and then cleared by hardware. On character input an Address Bit set can indicate that the data preceding the bit is an address which may be compared in hardware with the value in the Address Compare Register (ACR) to generate an Address Match interrupt when equal.

The Address bit and Address Comparison Register can also be combined to generate an Address Interrupt in 4 modes to suit different protocols, based upon the status of the Address Mode Enable bit (AME) and the Address Mode bit (AM) as shown in Table 17.

The character match Address Interrupt mode may be used as a powerful character search mode, giving an interrupt on reception of a predetermined character e.g. Carriage Return or End of Block codes.

Figure 45. SCI Character Format



	START	DATA	PARITY	ADDRESS	STOP	
# bits	1	5,6,7,8	0,1	0,1	1,1.5,2,2.5 1,2,3	÷16 ÷1
states			NONE ODD EVEN	ON OFF		

Figure 46. Byte Synchronous Output

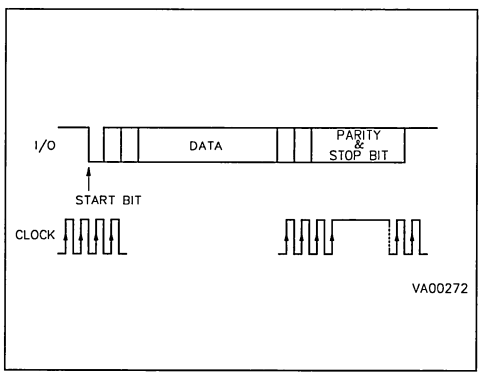
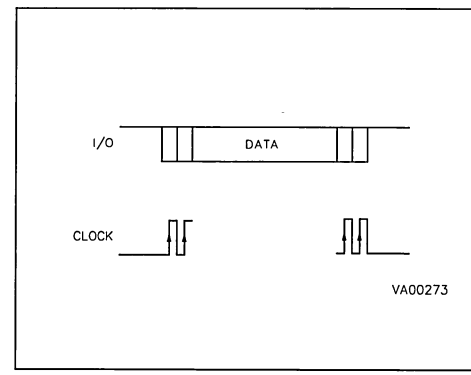


Figure 47. Serial Expansion Mode



SERIAL COMMUNICATION INTERFACE (Continued)

Table 17. Address Interrupt Modes

If 9th Data Bit = 1
If Character Match
If Character Match and 9th Data Bit = 1
If Character Match on Word Immediately Following Break

The Line Break condition is fully supported for both transmission and detection. Line Break is sent by setting the SET_BREAK bit (SB). This causes the transmitter output to be held low (after all buffered data has been transmitted) for a minimum of one complete word length and until the SB bit is Reset.

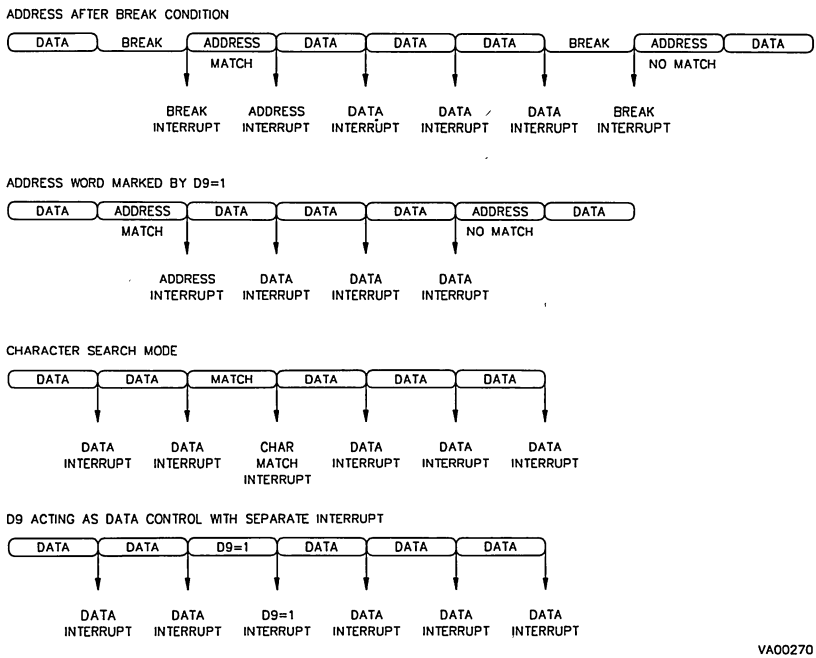
SCI Interrupts

The SCI is able to generate interrupts from multiple sources. Receive interrupts include data pending, receive errors (overrun, framing and parity), address or break pending and transmit interrupts are software selectable for either the Transmit Holding Register Empty (HSN = 1) or for the Transmit Shift Register Empty (HSN = 0). Interrupt sources are indicated by the Interrupt pending bits, shown in Table 18. These bits should be reset by the programmer during the Interrupt Service routine.

Table 18. SCI Interrupt Vector

Interrupt Source	Vector Address
Transmitter Buffer or Shift Register Empty/ Transmit DMA end of Block	xxx x110
Received Ready/ Receive DMA end of Block	xxxx X100
Break Detector Address Word Match	xxxx x001
Receiver Error	xxxx x000

Figure 48. SCI Interrupt Typical Usage



SERIAL COMMUNICATION INTERFACE (Continued)

When DMA is active the Receive Data Pending bit (RDP), and the Transmit status bit (THE/TSE) interrupt sources are replaced by the DMA End Of Block Interrupt sources for transmit and receive, respectively.

Typical Usage of the Interrupts provided by the SCI are shown in Figure 48.

The SCI interrupts have an internal priority structure in order to resolve simultaneous events (Table 19).

The four major levels of interrupt are encoded in hardware to provide two bits of the interrupt vector register, allowing the position of the block of pointer vectors to be resolved to a block size of 8 bytes.

Table 19. SCI Interrupt Internal Priority

Receive DMA Request	Highest Priority
Transmit DMA Request	
Receive Interrupt	
Transmit Interrupt	Lowest Priority

SCI DMA

Two DMA channels are associated with the SCI, for transmit and for receive. These follow the register scheme as described in DMA section. It should be noted that, after initializing the DMA counter and pointer registers and enabling DMA, data transmission is triggered by a character written into the Transmit Holding register. The DMA End Of Block Interrupts generated on completion of the DMA transfer take the place of the normal transmit and receive character interrupt vectors.

SCI Clock Generation

The communication bit frequency of the SCI transmitter and receiver sections can be provided from the integral Baud Rate Generator (allowing a maximum asynchronous bit rate of 350K Baud) or from external sources (maximum bit rate 175K Baud). This clock is divided by 16 for asynchronous mode (CD=0), or divided by 1 for synchronous modes (CD=1).

External Clock Sources The External Clock input pin TXCLK may be programmed in Alternate function by bits XT and OB to be the transmit clock input (respecting the ÷ 16 and ÷ 1 timing requirements), to act as the output of the Baud Rate Generator (allowing an external divider circuit to provide the receive clock for split rate transmit and receive e.g. 1200/75 baud), or to be CLKOUT, the clock output for the synchronous mode. Receive clock input via RXCLK Alternate function is enabled by the XR bit, this input should be set according to the setting of the CD bit.

Baud Rate Generator. The integral Baud Rate Generator is a 16 bit divide by *n* circuit of the Internal Clock INTCLK. Thus INTCLK should be chosen to provide a suitable frequency for division by the Baud Rate Generator to give the required transmit and receive bit rates.

Suitable INTCLK frequencies and the divider values for standard Baud rates are shown in Table 20.

The act of writing to either of the two registers comprising the 16 bit divider causes a reset of the SCI, allowing initialization of the SCI settings before the writing of the other Baud Rate Generator register.

Self Test

Testing of the communications channel may be performed using the facilities of the SCI. Auto Echo mode (SCI SOUT disconnected, SIN pin internally connected to SOUT pin) and Loopback mode (SCI transmitter and receiver sections disconnected from SOUT and SIN pins and directly connected internally) may be used individually or together.

SERIAL COMMUNICATION INTERFACE (Continued)

Table 20. SCI Baud Rate Generator Divider Values

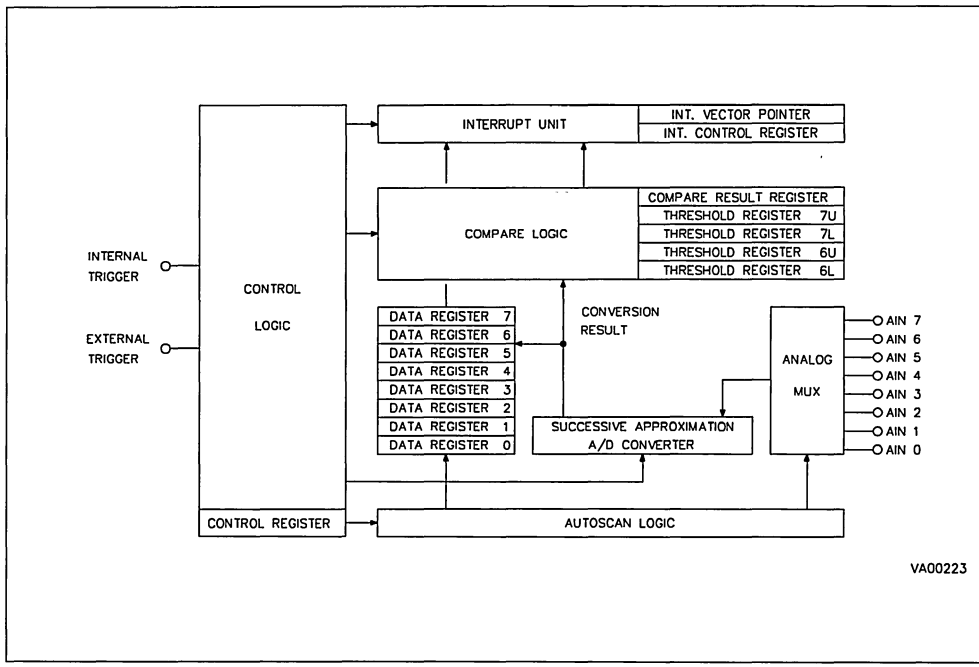
INTCLK: 7680.000 KHz							
Baud Rate	Clock Factor	Desired Freq (kHz)	Divisor		Actual Baud Rate	Actual Freq (kHz)	Deviation
			Dec	Hex			
50.00	16 X	0.80000	9600	2580	50.00	0.80000	0.0000%
75.00	16 X	1.20000	6400	1900	75.00	1.20000	0.0000%
110.00	16 X	1.76000	4364	110C	109.99	1.75985	0.0083%
300.00	16 X	4.80000	1600	0640	300.00	4.80000	0.0000%
600.00	16 X	9.60000	800	0320	600.00	9.60000	0.0000%
1200.00	16 X	19.20000	400	0190	1200.00	19.20000	0.0000%
2400.00	16 X	38.40000	200	00C8	2400.00	38.40000	0.0000%
4800.00	16 X	76.80000	100	0064	4800.00	76.80000	0.0000%
9600.00	16 X	153.60000	50	0032	9600.00	153.60000	0.0000%
19200.00	16 X	307.20000	25	0019	19200.00	307.20000	0.0000%
38400.00	16 X	614.40000	13	000D	36923.08	590.76923	3.8462%
76800.00	16 X	1228.80000	6	0006	80000.00	1280.00000	4.1667%
INTCLK: 11059.20 kHz							
Baud Rate	Clock Factor	Desired Freq (kHz)	Divisor		Actual Baud Rate	Actual Freq (kHz)	Deviation
			Dec	Hex			
50.00	16 X	0.80000	13824	3600	50.00	0.80000	0.0000%
75.00	16 X	1.20000	9216	2400	75.00	1.20000	0.0000%
110.00	16 X	1.76000	6284	188C	109.99	1.75990	0.0058%
300.00	16 X	4.80000	2304	0900	300.00	4.80000	0.0000%
600.00	16 X	9.60000	1152	0480	600.00	9.60000	0.0000%
1200.00	16 X	19.20000	576	0240	1200.00	19.20000	0.0000%
2400.00	16 X	38.40000	288	0120	2400.00	38.40000	0.0000%
4800.00	16 X	76.80000	144	0090	4800.00	76.80000	0.0000%
9600.00	16 X	153.60000	72	0048	9600.00	153.60000	0.0000%
19200.00	16 X	307.20000	36	0024	19200.00	307.20000	0.0000%
38400.00	16 X	614.40000	18	0012	38400.00	614.40000	0.0000%
76800.00	16 X	1228.80000	9	0009	76800.00	1228.80000	0.0000%

ANALOG TO DIGITAL CONVERTER

The ST903X Analog to Digital Converter (A/D) is comprised of an 8 channel multiplexed input selector and a Successive Approximation converter. The conversion time is a function of the INTCLK frequency; at the maximum 12MHz clock rate, conversion of the selected channel takes 11µs. This time also includes the 3µs setting time of the integral Sample and Hold circuitry, which minimizes need for external components. The resolution of the converted channel is 8 bits ±1/2 lsb between the Analog V_{SS} and Vdd references which occupy two pins of the ST903X (AV_{SS} and AV_{DD} respectively). This allows the full 256 bit resolution to apply over a reduced input range such as provided by various sensors and allows the best supply noise rejection.

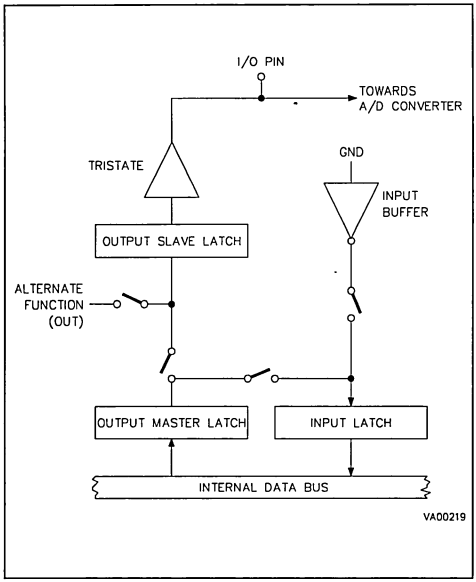
The input Analog channel is selected by using the Alternate Function setting as shown in the I/O ports section. The I/O bit structure of the port connected to the A/D converter (Port 4) is modified as shown in Figure 50 to prevent the Analog voltage present at the I/O pin from causing high power dissipation across the input buffer. Un-selected analog channels should also be maintained in the Alternate function mode for this reason. A Power Down mode is available for applications which require low power dissipation, this is selected by setting to zero the POW bit which turns off all Analog functions within the A/D converter.

Figure 49. A/D Block Diagram



ANALOG DIGITAL CONVERTER (Continued)

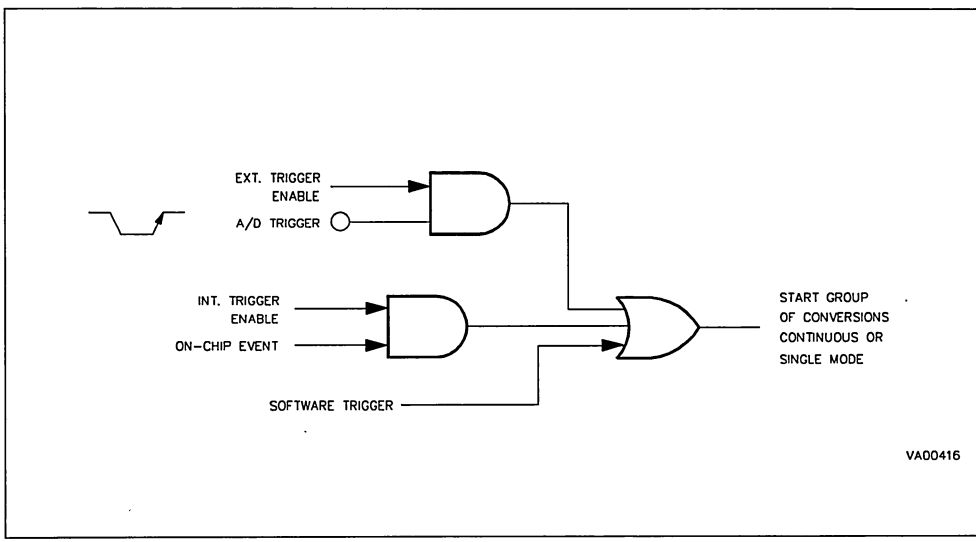
Figure 50. A/D Input Configuration



Conversion

Each of the input Analog channels (AIN0-7) can be converted singly or continuously. In single mode (CONT = "0") conversions are triggered by setting the Start/Stop bit ST, this is reset by hardware at the end of a group of conversions and conversion stops. The Autoscan mode (CONT = "1") converts each input channel in sequence, starting from the channel number selected in the Start Conversion Address (SC1-3) bits and increasing to channel 7 (AIN7), repeating so that the data registers will be maintained with the latest converted result. Conversion start is triggered by internal or external events. An external trigger (enabled by EXTG = "1") is caused by a pulse on the ADTRG pin available as an Input Alternate Function. This should have a minimum length of 80ns and of a period greater than the conversion time. The Internal trigger is enabled by setting INTG to "1" (this is ORed with EXTG to prevent hardware conflicts, but the correct procedure is to enable only one source at a time), in this case triggering is either by setting the ST bit by software or by enabling the ON-CHIP EVENT signal from the TIMER module to provide a trigger,from the timer.

Figure 51. A/D Trigger Sources

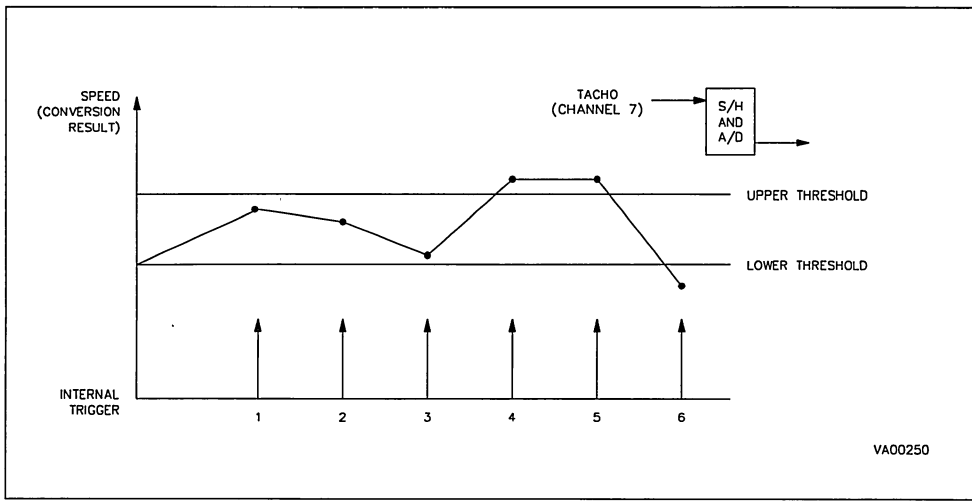


ANALOG DIGITAL CONVERTER (Continued)

The resulting data from the converted Analog channel AINx is stored in the appropriate Data Register DxR. Two channels AIN6 and AIN7 have a special feature known as the Analog Watchdog, by the use of two Threshold Registers for each channel. The Upper, (C6U, C7U), and lower, (C6L, C7L), registers contain user preset values.

These values are automatically compared to the value in the Data Registers D6 and D7 following each new conversion. If the resulting data is less than the corresponding Lower Threshold Register, or higher than the contents of the corresponding Upper Threshold Register, then an interrupt may be generated. This hardware feature minimizes analog monitoring overhead and is particularly useful in motor control applications as shown in Figure 52.

Figure 52. Analog Watchdog used in motor speed control



A/D Interrupts

The ST903X A/D converter provides two interrupt sources, End of Conversion and an Analog Watchdog Request. The interrupt vector register (IVR) provides 1 bit automatically generated in hardware to follow the interrupt source, allowing the user to select the base address of a four byte area of the interrupt vector table in which to store the A/D Interrupt Service Routines. The Analog Watchdog Request requires the user to poll within the Compare Result Register (CRR) to determine which of the four thresholds has been exceeded, the threshold status bits should be reset by software in the service routine. The interrupt pending flags, ECV (End of Conversion) and AWD (Analog Watchdog) should also be reset by the User in the Interrupt service routine before the return. The ST903X Analog to Digital converter occupies I/O page 63 (Group F).

SOFTWARE DESCRIPTION

Addressing Modes

The ST903X offers a wide variety of addressing modes and combinations to facilitate full and rapid access to the address spaces while reducing program length. Register addressing (using the working register group mechanism or directly addressed) can be used as 8 or 16 bit values for data or indirect addressing into the memory spaces or the Register File. The selection between Program Memory and Data Memory is performed through the DP bit in the FLAG Register, all subsequent actions on the memory space will affect the selected map only, apart from the memory map to memory map post-increment addressing mode which allows the map to be specified as part of the instruction for both destination and source operands. Apart from the immediate data and condition codes all operands are expressed as register file or memory addresses.

The available addressing modes, with the ST9 macro-assembler notation, are in Table 21

Table 21. Addressing Mode

Addressing Mode	Notation	
Immediate Data	#N	#NN
Register Direct	r	R
Register Indirect	(r)	(R)
Register Indirect with Post-Increment	(r)+	(R)+
Register Indexed	N(r)	N(R)
Register Bit	r.b	
Memory Direct	NN	
Memory Indirect	(rr)	
Memory Indirect with Post-Increment	(rr)+	
Memory Indirect with Pre-Decrement	-(rr)	
Memory Indexed with Immediate Short Offset	N(rr)	
Memory Indexed with Immediate Long Offset	NN(rr)	
Memory Indexed with Register Offset	rr(rr)	
Memory Indirect Bit	(rr).b	

Legend: N = 8 bit Value
NN = 16 bit Value or Address
r = Working Register
R = Directly Addressed Register
( ) = Indirect Addressing
( )+ = Indirect with Post-Increment
-( ) = Indirect with Pre-Decrement
.b = Bit Number (0 to 7)

Combinations of Available Addressing Modes.

Table 22 describes the addressing modes available for the Register File and the memory (as a destination or a source) for a two operand arithmetic, logic or load instruction, while the other operand is a directly addressed register.
Addressing modes are also available for the destination operand of these instructions, when the source operand is immediate data contained in the instruction.

Memory to memory operations can be performed by using the memory indirect addressing mode for both the source and the destination operands of instructions.
In order to allow easy block operations, addressing combinations are provided for the load byte instructions.
One operand arithmetic, logic and shift byte instructions as well as push and pop byte instructions have direct register and indirect register addressing modes. Most other instructions have direct register addressing mode only, with the exception of the program control instructions and the bit set and test instructions.

Table 22. Addressing Mode Permutation for Instructions

Two Operand Arithmetic and Logic Instructions	
Destination	**Source**
Register Direct	Register Direct
Register Direct	Register Indirect
Register Direct	Memory Indirect
Register Direct	Memory Indexed
Register Direct	Memory Indirect with Post- Increment
Register Direct	Memory Indirect with Pre- Decrement
Register Direct	Memory Direct
Register Indirect	Register Direct
Memory Indirect	Register Direct
Memory Indexed	Register Direct
Memory Indirect with Post- Increment	Register Direct
Memory Indirect with Pre- Decrement	Register Direct
Memory Direct	Register Direct

SOFTWARE DESCRIPTION (Continued)

Table 22. Addressing Mode Permutation for Instructions (Continued)

Two Operand Load Instructions	
Destination	**Source**
Register Direct	Register Direct
Register Direct	Register indirect
Register Direct	Register Indexed
Register Direct	Memory Indirect
Register Direct	Memory Indexed
Register Direct	Memory Indirect With Post-increment
Register Direct	Memory Indirect With Pre-Decrement
Register Direct	Memory Direct
Register indirect	Register Direct
Register Indexed	Register Direct
Memory Indirect	Register Direct
Memory Indexed	Register Direct
Memory Indirect With Post-increment	Register Direct
Memory Indirect With Pre-Decrement	Register Direct
Memory Direct	Register Direct
Two Operand Arithmetic and Logic Instructions	
Destination	**Source**
Register Direct	Immediate
Memory Direct	Immediate
Memory Indirect	Immediate
Two Operand Load Instructions	
Destination	**Source**
Register Direct	Immediate
Memory Direct	Immediate
Memory Indirect	Immediate
Long Indexed Memory (1)	Immediate
Two Operand Arithmetic, Logic & Load Instructions	
Destination	**Source**
Memory Indirect	Memory Indirect

Table 22. Addressing Mode Permutation for Instructions (Continued)

Two Operand Load Instructions (2)	
Destination	**Source**
Register Indirect with Post- Increment	Memory Indirect with Post- Increment
Memory Indirect with Post- Increment	Register Indirect with Post- Increment
Memory Indirect with Post- Increment	Memory Indirect with Post- Increment

Notes:
1. Load Word only
2. Load Byte only

Instruction Set

The ST903X instruction set consists of 87 instruction types functionally divided into eight groups as in Table 23, they are:

- Load (two operands)
- Arithmetic & Logic (two operands)
- Arithmetic Logic and Shift (one operand)
- Stack (one operand)
- Multiply & Divide (two operands)
- Boolean (one or two operands)
- Program Control (zero to three operands)
- Miscellaneous (zero to two operands)

The wide range of instructions facilitates the full use of the register file and address spaces, reducing execution times, while the register pointers mechanism allows an unmatched code efficiency and ultrafast context switching. A particularly notable feature is the comprehensive "Any Bit, Any Register" (ABAR) addressing capability of the Boolean instructions.

The ST903X can operate with a wide range of data lengths from single bit, 4-bit nibbles which can be in the form of Binary Coded Decimal (BCD) digits, 8-bit bytes and 16-bit words. The summary on Table 23 shows the instructions belonging to each group and the number of operands required for each.

The source operand is "src", "dst" is the destination operand, and "cc" is the condition code selection.

SOFTWARE DESCRIPTION (Continued)

Table 23. Instruction Set Summary

Load Instructions (Two Operands)								
Mnemonic	Operand	Instruction	Flags					
			C	Z	S	V	D	H
LD LDW	dst, src dst, src	Load Load Word	– –	– –	– –	– –	– –	– –
Arithmetic and Logic (Two Operands)								
Mnemonic	Operand	Instruction	Flags					
			C	Z	S	V	D	H
ADD ADDW	dst, src dst, src	Add Add Word	Δ Δ	Δ Δ	Δ Δ	Δ Δ	0 ?	Δ ?
ADC ADCW	dst, src dst, src	Add with Carry Add Word with Carry	Δ Δ	Δ Δ	Δ Δ	Δ Δ	0 ?	Δ ?
SUB SUBW	dst, src dst, src	Subtract Subtract Word	Δ Δ	Δ Δ	Δ Δ	Δ Δ	1 ?	Δ ?
SBC SBCW	dst, src dst, src	Subtract with Carry Subtract Word with Carry	Δ Δ	Δ Δ	Δ Δ	Δ Δ	1 ?	Δ ?
AND ANDW	dst, src dst, src	Logical AND Logical Word AND	– –	Δ Δ	Δ Δ	0 0	– ?	– ?
OR ORW	dst, src dst, src	Logical OR Logical Word OR	– –	Δ Δ	Δ Δ	0 0	– –	– –
XOR XORW	dst, src dst, src	Logical Exclusive OR Logical Word Exclusive OR	– –	Δ Δ	Δ Δ	0 0	– –	– –
CP CPW	dst, src dst, src	Compare Compare Word	Δ Δ	Δ Δ	Δ Δ	Δ Δ	– –	– –
TM TMW	dst, src dst, src	Test Under Mask Test Word Under Mask	– –	Δ Δ	Δ Δ	0 0	– –	– –
TCM TCMW	dst, src dst, src	Test Complement Under Mask Test Word Complement Under Mask	– –	Δ Δ	Δ Δ	0 0	– –	– –

Legend: 0 = Bit set to zero
1 = Bit set to one
Δ = Bit affected
? = Bit status undefined
– = Bit not affected

SOFTWARE DESCRIPTION (Continued)

Table 23. Instruction Set Summary (Continued)

Arithmetic Logic and Shift (One Operand)									
Mnemonic	Operand	Instruction	Flags						
			C	Z	S	V	D	H	
INC INCW	dst dst	Increment Increment Word	– –	Δ Δ	Δ Δ	Δ Δ	– –	– –	
DEC DECW	dst dst	Decrement Decrement Word	– –	Δ Δ	Δ Δ	Δ Δ	– –	– –	
SLA SLAW	dst dst	Shift Left Arithmetic Shift Word Left Arithmetic	Δ Δ	Δ Δ	Δ Δ	Δ Δ	0 ?	Δ ?	
SRA SRAW	dst dst	Shift Right Arithmetic Shift Word Right Arithmetic	Δ Δ	Δ ?	Δ Δ	Δ 0	0 –	Δ –	
RRC RRCW	dst dst	Rotate Right through Carry Rotate Word Right through Carry	Δ Δ	Δ ?	Δ Δ	Δ Δ	– –	– –	
RLC RLCW	dst dst	Rotate Left through Carry Rotate Word Left through Carry	Δ Δ	Δ ?	Δ Δ	Δ Δ	– –	– –	
ROR	dst	Rotate Right	Δ	Δ	Δ	Δ	–	–	
ROL	dst	Rotate Left	Δ	Δ	Δ	Δ	–	–	
CLR	dst	Clear	–	–	–	–	–	–	
CPL	dst	Complement Register	–	Δ	Δ	0	–	–	
SWAP	dst	Swap Nibbles	?	Δ	Δ	?	–	–	
DA	dst	Decimal Adjust	Δ	Δ	Δ	?	–	–	
Stack Instructions (One Operand)									
Mnemonic	Operand	Instruction	Flags						
			C	Z	S	V	D	H	
PUSH PUSHW PEA	src src src	Push on System Stack Push Word on System Stack Push Effective Address on System Stack	– – –	– – –	– – –	– – –	– – –	– – –	
POP POPW	dst dst	Pop from System Stack Pop Word from System Stack	– –	– –	– –	– –	– –	– –	
PUSHU PUSHUW PEAU	src src src	Push on User Stack Push Word on User Stack Push Effective Address on User Stack	– – –	– – –	– – –	– – –	– – –	– – –	
POPU POPUW	dst dst	Pop from User Stack Pop Word from User Stack	– –	– –	– –	– –	– –	– –	

SOFTWARE DESCRIPTION (Continued)

Table 23. Instruction Set Summary (Continued)

Multiply and Divide Instructions (Two Operands)									
Mnemonic	**Operand**	**Instruction**	**Flags**						
			C	**Z**	**S**	**V**	**D**	**H**
MUL	dst, src	Multiply 8x8	Δ	Δ	Δ	Δ	0	?
DIV DIVWS	dst, src	Divide 16/8 Divide Word Stepped 32/16	1 ?	Δ ?	Δ ?	? ?	1 ?	? ?
Boolean Instructions (Two Operands)									
Mnemonic	**Operand**	**Instruction**	**Flags**						
			C	**Z**	**S**	**V**	**D**	**H**
BLD	dst, src	Bit Load	–	–	–	–	–	–
BAND	dst, src	Bit AND	–	–	–	–	–	–
BOR	dst, src	Bit OR	–	–	–	–	–	–
BXOR	dst, src	Bit Exclusive OR	–	–	–	–	–	–
Boolean Instructions (One Operand)									
Mnemonic	**Operand**	**Instruction**	**Flags**						
			C	**Z**	**S**	**V**	**D**	**H**
BSET	dst	Bit Set	–	–	–	–	–	–
BRES	dst	Bit Reset	–	–	–	–	–	–
BCPL	dst	Bit Complement	–	–	–	–	–	–
BTSET	dst	Bit Test and Set	–	Δ	Δ	0	–	–
Program Control Instructions (Three Operands)									
Mnemonic	**Operand**	**Instruction**	**Flags**						
			C	**Z**	**S**	**V**	**D**	**H**
CPJFI	dst, src	Compare and Jump on False, Otherwise Post Increment	–	–	–	–	–	–
CPJTI	dst, src	Compare and Jump on True, Otherwise Post Increment	–	–	–	–	–	–

SOFTWARE DESCRIPTION (Continued)

Table 23. Instruction Set Summary (Continued)

Program Control Instructions (Two Operands)								
Mnemonic	Operand	Instruction	Flags					
			C	Z	S	V	D	H
BTJF	dst, src	Bit Test and Jump if False	–	–	–	–	–	–
BTJT	dst, src	Bit Test and Jump if True	–	–	–	–	–	–
DJNZ	dst, src	Decrement a Working Register and Jump if Not Zero	–	–	–	–	–	–
DWJNZ	dst,src	Decrement a Register Pair and Jump if Not Zero	–	–	–	–	–	–
Program Control Instructions (One Operand)								
Mnemonic	Operand	Instruction	Flags					
			C	Z	S	V	D	H
JR	cc, dst	Jump Relative if Condition is Met	–	–	–	–	–	–
JP	cc, dst	Jump if Condition is Met	–	–	–	–	–	–
JP	dst	Unconditional Jump	–	–	–	–	–	–
CALL	dst	Unconditional Call	–	–	–	–	–	–
Program Control Instructions (No Operand)								
Mnemonic	Operand	Instruction	Flags					
			C	Z	S	V	D	H
RET		Return from Subroutine	–	–	–	–	–	–
IRET		Return from Interrupt	Δ	Δ	Δ	Δ	Δ	Δ
WFI		Stop Program Execution and Wait Next Enabled Interrupt. If a DMA request is present the CPU executes the DMA service routine and returns to WFI state.	–	–	–	–	–	–
HALT		Stop Program Execution until RESET	–	–	–	–	–	–
Miscellaneous (Two Operands)								
Mnemonic	Operand	Instruction	Flags					
			C	Z	S	V	D	H
XCH	dst, src	Exchange Registers	–	–	–	–	–	–

SOFTWARE DESCRIPTION (Continued)

Table 23. Instruction Set Summary (Continued)

Miscellaneous (One Operand)								
Mnemonic	**Operand**	**Instruction**	**Flags**					
			C	**Z**	**S**	**V**	**D**	**H**
SRP	src	Set Register Pointer Long (16 Working Registers)	–	–	–	–	–	–
SRP0	src	Set Register Pointer 0 (8 LSB Working Registers)	–	–	–	–	–	–
SRP1	src	Set Register Pointer 1 (8 MSB Working Registers)	–	–	–	–	–	–
SPP	src	Set Page Pointer	–	–	–	–	–	–
EXT	src	Sign Extend	–	–	–	–	–	–
Miscellaneous (No Operand)								
Mnemonic	**Operand**	**Instruction**	**Flags**					
			C	**Z**	**S**	**V**	**D**	**H**
EI		Enable Interrupts	–	–	–	–	–	–
DI		Disable Interrupts	–	–	–	–	–	–
SCF		Set Carry Flag	1	–	–	–	–	–
RCF		Reset Carry Flag	0	–	–	–	–	–
CCF		Complement Carry Flag	Δ	–	–	–	–	–
SPM		Select Program Memory	–	–	–	–	–	–
SDM		Select Data Memory	–	–	–	–	–	–
NOP		No Operation	–	–	–	–	–	–

SOFTWARE DESCRIPTION (Continued)

Processor Flags

An important aspect of any single chip microcontroller is the ability to test data and make the appropriate action based on the results. In order to provide this facility, register 231 in the Register File is used as a Flag Register. Six bits of this register are used as the following flags:

C - Carry
Z - Zero
S - Sign
V - Overflow
D - Decimal Adjust
H - Half Carry
One of the two remaining bits in the flag register is available to the user (bit 1, F1). Bit 0 is the Program/Data Memory selector bit and is operated on directly by the hardware within the ST903X. The P/$\overline{D}$ pin will follow the status of this bit.

Condition Codes. Flags C, Z, S, and V control the operation of the "conditional" Jump instructions. Table 24 shows the condition codes and the flag settings affecting the jump.

POWERFUL DEVELOPMENT ENVIRONMENT

ST9 Software Tools

The following Software Tools are available for MS-DOS, SUN-3 and SUN-4 operating systems:

AST9 high-level macro assembler with predefined macro instructions (IF/ELSE, WHILE, DO, LOOP, SWITCH, BREAK, PROCEDURE, RETURN).

LST9 Incremental Linker/Loader.

CST9 Optimised C-Compiler (ANSI STANDARD).

ARST9 Library Archiver.

SIMST9 Software Simulator with realtime emulation executor

ST903X Hardware Emulator. Realtime emulation of the ST903X in all packaging options is performed by a modular emulation system, interfaced to the host computer through an RS232 channel, with powerful hardware breakpoints, on-line assembler/disassembler, emulation and trace memory. The emulator is fully supported by a symbolic on-line debugger and help facility.

Table 24. Condition Codes Summary

Mnemonic Code	Meaning	Flag Setting
F	Always False	—
T	Always True	—
C	Carry	C = 1
NC	No Carry	C = 0
Z	Zero	Z = 1
NZ	No Zero	Z = 0
PL	Plus	S = 0
MI	Minus	S = 1
OV	Overflow	V = 1
NOV	No Overflow	V = 0
EQ	Equal	Z = 1
NE	Not Equal	Z = 0
GE	Greater Than or Equal	(S xor V) = 0
LT	Less Than	(S xor V) = 1
GT	Greater Than	(Z or (S xor V)) = 0
LE	Less Than or Equal	(Z or (S xor V)) = 1
UGE	Unsigned Greater Than or Equal	C = 0
UL	Unsigned Less Than	C = 1
UGT	Unsigned Greater Than	(C = 0 and Z = 0) = 1
ULE	Unsigned Less Than or Equal	(C or Z) = 1

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	– 0.3 to 7.0	V
AV_{DD}, AV_{SS}	Analog Supply Voltage	$V_{SS} \le AV_{SS} < AV_{DD} \le V_{DD}$	V
V_I	Input Voltage	V_{SS} – 0.3 to V_{DD} +0.3	V
V_O	Output Voltage	V_{SS} – 0.3 to V_{DD} +0.3	V
T_{STG}	Storage Temperature	– 55 to + 150	°C

Note: Stresses above those listed as "absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value		Unit
		Min.	Max.	
T_A	Operating Temperature	– 40	85	°C
V_{DD}	Operating Supply Voltage	4.5	5.5	V
f_{OSCE}	External Oscillator Frequency		24	MHz
f_{OSCI}	Internal Oscillator Frequency		12	MHz

DC ELECTRICAL CHARACTERISTICS

(V_{DD} = 5V ± 10% T_A = – 40 °C to + 85°C, unless otherwise specified)

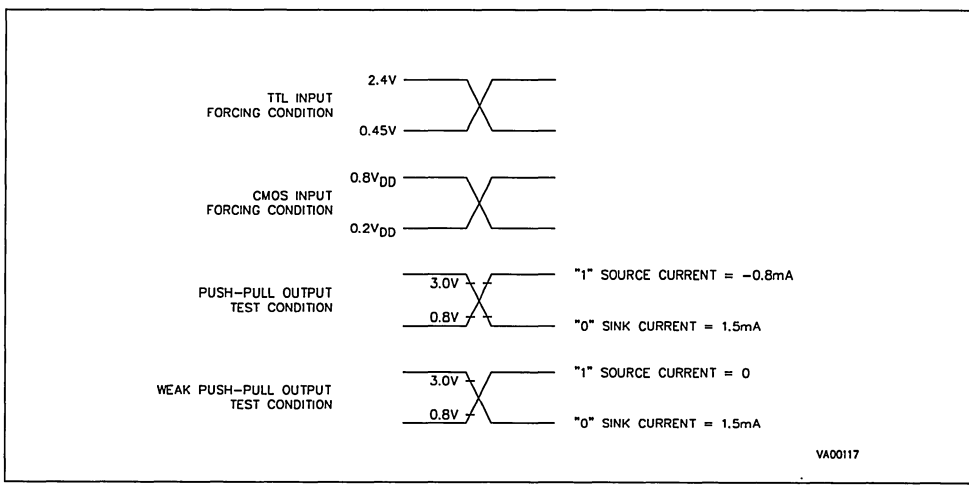
Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
V_{IHCK}	Clock Input High Level	External Clock	0.7 V_{DD}		V_{DD} + 0.3	V
V_{ILCK}	Clock Input Low Level	External Clock	– 0.3		0.3 V_{DD}	V
V_{IH}	Input High Level	TTL	2.0		V_{DD} + 0.3	V
		CMOS	0.7 V_{DD}		VDD + 0.3	V
V_{IL}	Input Low Level	TTL	– 0.3		0.8	V
		CMOS	– 0.3		0.3 V_{DD}	V
V_{IHRS}	Reset Input High Level		0.7 V_{DD}		V_{DD} + 0.3	V
V_{ILRS}	Reset Input Low Level		–0.3		0.3 V_{DD}	V
V_{HYRS}	Reset Input Hysteresis		0.3		1.5	V
V_{OH}	Output High Level	Push Pull, Iload = – 0.8mA	V_{DD} – 0.8			V
V_{OL}	Output Low Level	Push Pull or Open Drain, Iload = – 1.6mA			0.4	V
I_{WPU}	Weak Pull-up Current	Bidirectional Weak Pull-up, V_{OL} = 0V	– 80	– 200	– 420	µA

DC ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
I_{APU}	Active Pull-up Current, for INT0 and INT7 only	$V_{IN} < 0.8V$	– 80	– 200	– 420	µA
I_{LKIO}	I/O Pin Input Leakage	Input/Tri-State, $0V < V_{IN} < V_{DD}$	– 10		+ 10	µA
I_{LKRS}	Reset Pin Input Leakage	$0V < V_{IN} < V_{DD}$	– 30		+ 30	µA
I_{LKAD}	A/D Pin Input Leakage	Alternate Function, Open Drain, $0V < V_{IN} < V_{DD}$	– 3		+ 3	µA
I_{LKAP}	Active Pull-up Input Leakage	$0V < V_{IN} < 0.8V$	– 10		+ 10	µA
I_{LKOS}	OSCIN Pin Input Leakage	$0V < V_{IN} < V_{DD}$	– 10		+ 10	µA
I_{DD}	Run Mode Current	24MHz, Note 1		32	70	mA
		4MHz, Note 1		6	12	mA
I_{DP2}	Run Mode Current Prescale by 2	24MHz, Note 1		19	40	mA
		4MHz, Note 1		4	8	mA
I_{WFI}	WFI Mode Current	24MHz, Note 1		9	18	mA
		4MHz, Note 1		2.5	5	mA
I_{HALT}	HALT Mode Current	24MHz, Note 1			100	µA

Note:
1. All I/O Ports are configured in Bidirectional Weak Pull-up Mode with no DC load, External Clock pin (OSCIN) is driven by square wave external clock. No peripheral working. External interface not active (Internal Program Execution).

DC TEST CONDITIONS



AC ELECTRICAL CHARACTERISTICS

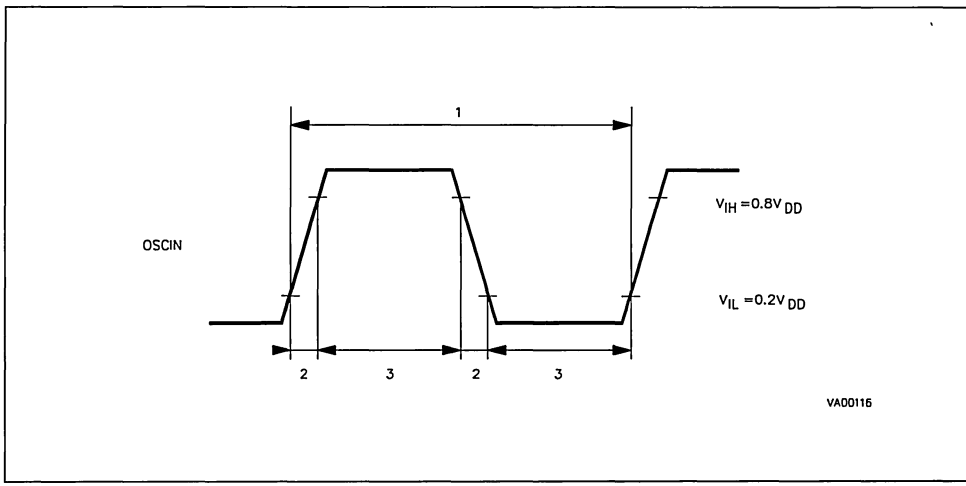
CLOCK TIMING TABLE

(V_{DD} = 5V ± 10%, T_A = − 40°C to + 85°C, unless otherwise specified)

N°	Symbol	Parameter	Value		Unit	Note
			Min.	Max.		
1	TpC	OSCIN Clock Period	41.5		ns	1
			83		ns	2
2	TrC, TfC	OSCIN Rise and Fall Time		12	ns	
3	TwCL, TwCH	OSCIN Low and High Width	25	12	ns	1
			38		ns	2

Note: 1. Clock divided by 2 internally (MODER.DIV2=1)
2. Clock not divided by 2 internally (MODER.DIV2=0)

CLOCK TIMING



EXTERNAL BUS TIMING TABLE

(V_{DD} = 5V ± 10%, T_A = – 40 °C to + 85 °C, Cload = 50pF, CPUCLK = 12MHz, unless otherwise specified)

N°	Symbol	Parameter	Value (Note)				Unit
			OSCIN Divided By 2	OSCIN Not Divided By 2	Min.	Max.	
1	TsA (AS)	Address Set-up Time before $\overline{AS}$ ↑	TpC (2P+1) –22	TWCH+PTpC –18	20		ns
2	ThAS (A)	Address Hold Time after $\overline{AS}$ ↑	TpC –17	TwCL –13	25		ns
3	TdAS (DR)	$\overline{AS}$ ↑ to Data Available (read)	TpC (4P+2W+4) –52	TpC (2P+W+2) –51		115	ns
4	TwAS	$\overline{AS}$ Low Pulse Width	TpC (2P+1) –7	TwCH+PTpC –3	35		ns
5	TdAz (DS)	Address Float to $\overline{DS}$ ↓	0	0	0		ns
6	TwDSR	$\overline{DS}$ Low Pulse Width (read)	TpC (4P+2W+3) –20	TwCH+TpC (2P+W+1) – 16	105		ns
7	TwDSW	$\overline{DS}$ Low Pulse Width (write)	TpC (2P+2W+2) –13	TpC (P+W+1) –13	70		ns
8	TdDSR (DR)	$\overline{DS}$ ↓ to Data Valid Delay (read)	TpC (4P+2W-3) –50	TwCH+TpC(2P+W+1) – 46		75	ns
9	ThDR (DS)	Data to $\overline{DS}$ ↑ Hold Time (read)	0	0	0		ns
10	TdDS (A)	$\overline{DS}$ ↑ to Address Active Delay	TpC –7	TwCL –3	35		ns
11	TdDS (AS)	$\overline{DS}$ ↑ to $\overline{AS}$ ↓ Delay	TpC –18	TwCL –14	24		ns
12	TsR/W (AS)	R/$\overline{W}$ Set-up Time before $\overline{AS}$ ↑	TpC (2P+1) –22	TwCH+PTpC –18	20		ns
13	TdDSR (R/W)	$\overline{DS}$ ↑ to R/$\overline{W}$ and Address Not Valid Delay	TpC –9	TwCL –5	33		ns
14	TdDW (DSW)	Write Data Valid to $\overline{DS}$ ↓ Delay (write)	TpC (2P+1) –32	TwCH+PTpC –28	10		ns
15	ThDS (DW)	Data Hold Time after DS ↑ (write)	TpC –9	TwCL –5	33		ns
16	TdA (DR)	Address Valid to Data Valid Delay (read)	TpC (6P+2W+5) –68	TwCH+TpC (3P+W+2) – 64		140	ns
17	TdAs (DS)	$\overline{AS}$ ↑ to $\overline{DS}$ ↓ Delay	TpC –18	TwCL –14	24		ns

Note: The value left hand two columns show the formula used to calculate the timing minimum or maximum from the oscillator clock period, prescale value and number of wait cycles inserted.
The value right hand two columns show the timing minimum and maximum for an external clock at 24 MHz divided by 2, prescaler value of zero and zero wait status.

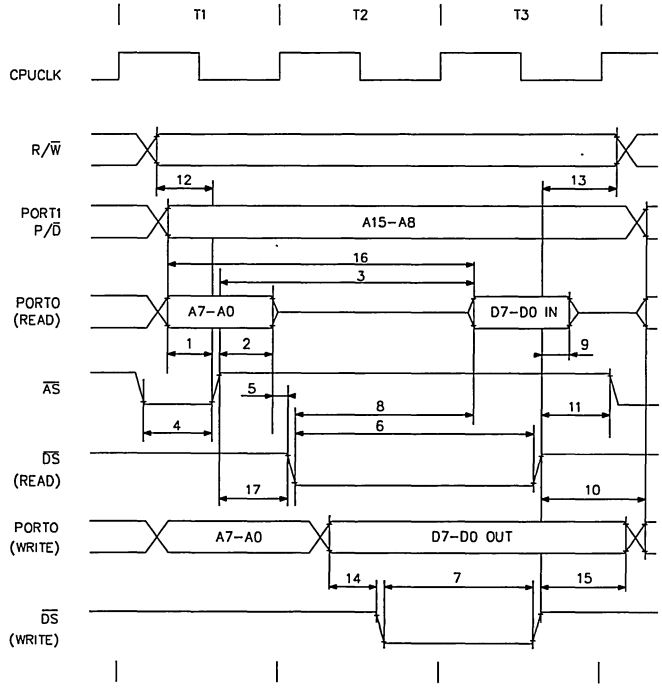
Legend:
P = Clock Prescaling Value
W = Wait Cycles
TpC = OSCIN Period
TwCH = High Level OSCIN half period
TwCL = Low Level OSCIN half period

EXTERNAL WAIT TIMING TABLE (V_{DD} = 5V ± 10%, T_A = –40°C to +85°C, Cload = 50pF, INTCLK = 12MHz, Push-pull output configuration, unless otherwise specified)

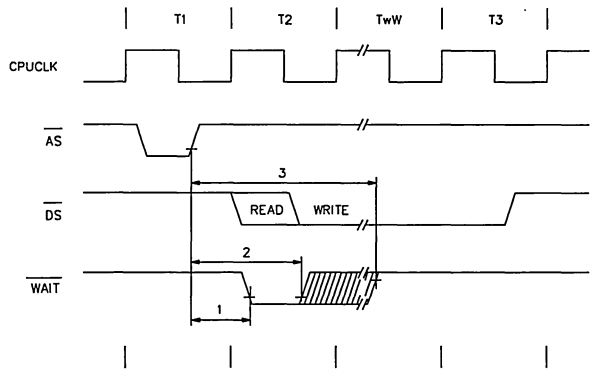
N°	Symbol	Parameter	Value (Note)				Unit
			OSCIN Divided By 2	OSCIN Not Divided By 2	Min.	Max.	
1	TdAS (WAIT)	$\overline{AS}$ ↑ to $\overline{WAIT}$ ↓ Delay	2(P+1)TpC –29	(P+1)TpC –29		40	ns
2	TdAS (WAIT)	$\overline{AS}$ ↑ to $\overline{WAIT}$ ↑ Minimum Delay	2(P+W+1)TpC –4	(P+W+1)TpC –4	80		ns
3	TdAS (WAIT)	$\overline{AS}$ ↑ to $\overline{WAIT}$ ↑ Maximum Delay	2(P+W+1)TpC –29	(P+W+1)TpC –29		83W+40	ns

Note: The value left hand two columns show the formula used to calculate the timing minimum or maximum from the oscillator clock period, prescale value and number of wait cycles inserted.
The value right hand two columns show the timing minimum and maximum for an external clock at 24 MHz divided by 2, prescale value of zero and zero wait status.

EXTERNAL BUS TIMING



EXTERNAL WAIT TIMING

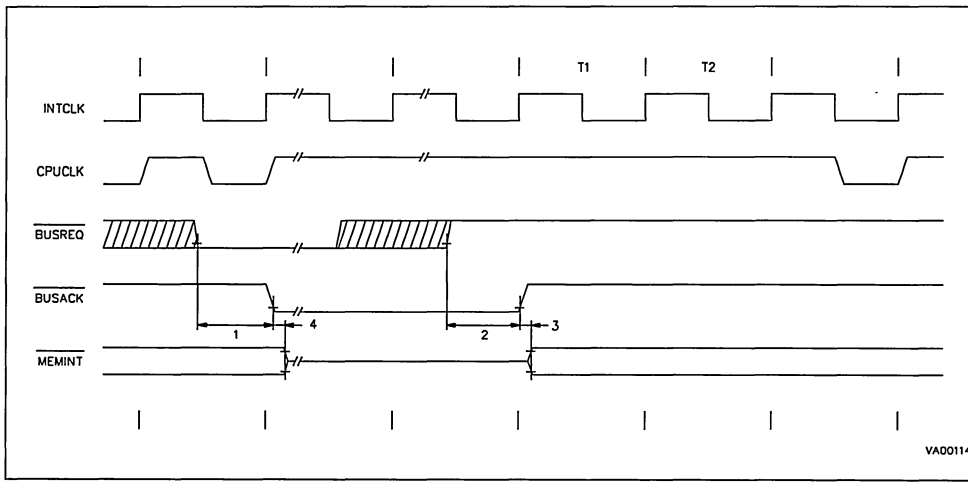


BUS REQUEST/ACKNOWLEDGE TIMING TABLE (V_{DD} = 5V ± 10%, T_A = −40°C to +85°C, Cload = 50pF, INTCLK = 12MHz, Push-pull output configuration, unless otherwise specified)

N°	Symbol	Parameter	Value (Note)				Unit
			OSCIN Divided By 2	OSCIN Not Divided By 2	Min.	Max.	
1	TdBR (BACK)	$\overline{BREQ}$ ↓ to $\overline{BUSACK}$ ↓	TpC+8	TwCL+12	50		ns
			TpC(6P+2W+7)+65	TpC(3P+W+3)+TwCL+65		360	ns
2	TdBR (BACK)	$\overline{BREQ}$ ↑ to $\overline{BUSACK}$ ↑	3TpC+60	TpC+TwCL+60		185	ns
3	TdBACK (BREL)	$\overline{BUSACK}$ ↓ to Bus Release	20	20		20	ns
4	TdBACK (BACT)	$\overline{BUSACK}$ ↑ to Bus Active	20	20		20	ns

Note: The value left hand two columns show the formula used to calculate the timing minimum or maximum from the oscillator clock period, prescale value and number of wait cycles inserted.
The value right hand two columns show the timing minimum and maximum for an external clock at 24 MHz divided by 2, prescale value of zero and zero wait status.

BUS REQUEST/ACKNOWLEDGE TIMING



Note : MEMINT = group of memory interface signals : $\overline{AS}$, $\overline{DS}$, R/$\overline{W}$, P00-P07, P10-P17.

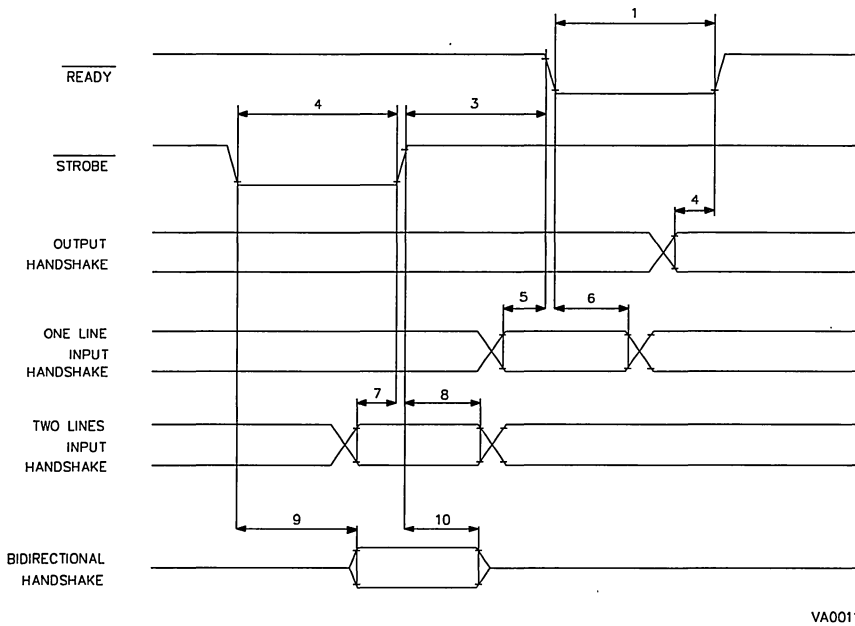
HANDSHAKE TIMING TABLE (V_{DD} = 5V ± 10%, T_A = –40°C to +85°C, Cload = 50pF, INTCLK = 12MHz, Push-pull output configuration, unless otherwise specified)

N°	Symbol	Parameter	Value (Note)				Min.	Max.	Unit
			OSCIN Divided By 2		OSCIN Not Divided By 2				
			Min.	Max.	Min.	Max.			
1	TwRDY	RDRDY, WRRDY Pulse Width in One Line Handshake	2TpC (P+W+1) –18		TpC (P+W+1) –18		65		ns
2	TwSTB	$\overline{RDSTB}$, $\overline{WRSTB}$ Pulse Width	2TpC+12		TpC+12		95		ns
3	TdST (RDY)	$\overline{RDSTB}$, or $\overline{WRSTB}$ ↑ to RDRDY or WRRDY ↓		TpC+45		(TpC-TwCL) +45		87	ns
4	TsPD (RDY)	Port Data to RDRDY ↑ Set-up Time	(2P+2W+1) TpC –25		TwCH+(W+P) TpC –25		16		ns
5	TsPD (RDY)	Port Data to WRRDY ↓ Set-up Time in One Line Handshake	43		43		43		ns
6	ThPD (RDY)	Port Data to WRRDY ↓ Hold Time in One Line Handshake	0		0		0		ns
7	TsPD (STB)	Port Data to $\overline{WRSTB}$ ↑ Set-up Time	10		10		10		ns
8	ThPD (STB)	Port Data to WRSTB ↑ Hold Time	25		25		25		ns
9	TdSTB (PD)	$\overline{RDSTBD}$ ↑ to Port Data Delay Time in Bidirectional Hand-shake		35		35		35	ns
10	TdSTB (PHZ)	$\overline{RDSTB}$ ↑ to Port High-Z Delay Time in Bidirectional Hand-shake		25		25		25	ns

Note: The value left hand two columns show the formula used to calculate the timing minimum or maximum from the oscillator clock period, prescale value and number of wait cycles inserted.
The value right hand two columns show the timing minimum and maximum for an external clock at 24 MHz divided by 2, prescaler value of zero and zero wait status.

Legend:
P = Clock Prescaling Value (R235.4,3,2)
W = Programmable Wait Cycles (R252.2.1.0/5,4,3) + External Wait Cycles

HANDSHAKE TIMING

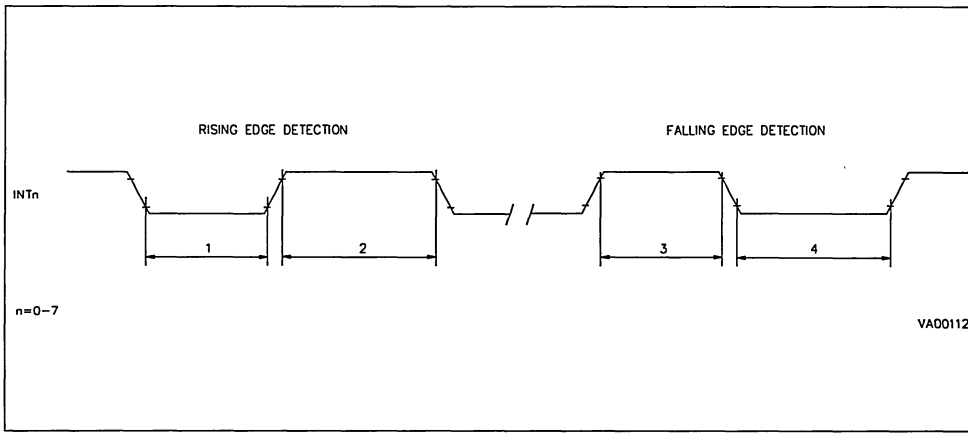


EXTERNAL INTERRUPT TIMING TABLE (V_{DD} = 5V ± 10%, T_A = –40°C to +85°C, Cload = 50pF, INTCLK = 12MHz, Push-pull output configuration, unless otherwise specified)

N°	Symbol	Parameter	Value (Note)				Unit
			OSCIN Divided By 2 Min.	OSCIN Not Divided By 2 Min.	Min.	Max.	
1	TwLR	Low Level Minimum Pulse Width in Rising Edge Mode	2TpC+12	TpC+12	95		ns
2	TwHR	High Level Minimum Pulse Width in Rising Edge Mode	2TpC+12	TpC+12	95		ns
3	TwHF	High Level Minimum Pulse Width in Falling Edge Mode	2TpC+12	TpC+12	95		ns
4	TwLF	Low Level Minimum Pulse Width in Falling Edge Mode	2TpC+12	TpC+12	95		ns

Note: The value left hand two columns show the formula used to calculate the timing minimum or maximum from the oscillator clock period, prescale value and number of wait cycles inserted.
The value right hand two columns show the timing minimum and maximum for an external clock at 24 MHz divided by 2, prescale value of zero and zero wait status.

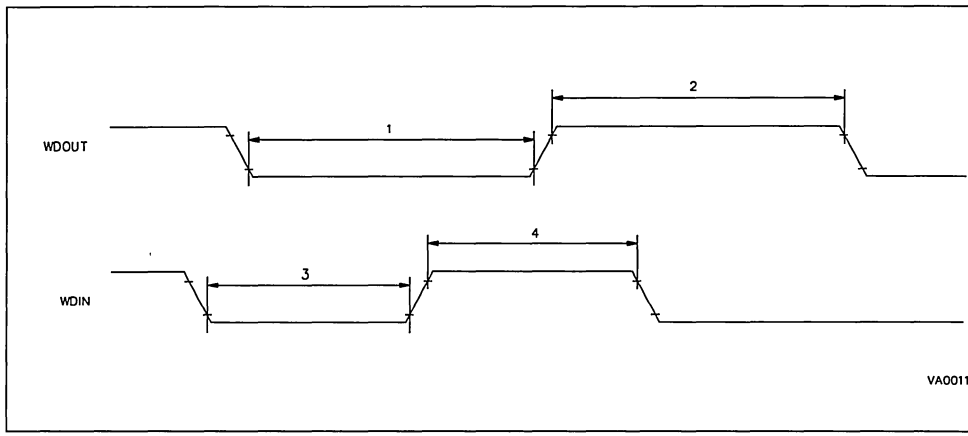
EXTERNAL INTERRUPT TIMING



WATCHDOG TIMING TABLE (V_{DD} = 5V ± 10%, T_A = –40°C to +85°C, Cload = 50pF, INTCLK =12MHz, Output Alternate Function set as Push-pull)

N°	Symbol	Parameter	Value		Unit
			Min.	Max.	
1	TwWDOL	WDOUT Low Pulse Width	620		ns
2	TwWDOH	WDOUT High Pulse Width	620		ns
3	TwWDIL	WDIN Low Pulse Width	350		ns
4	TwWDIH	WDIN High Pulse Width	350		ns

WATCHDOG TIMING

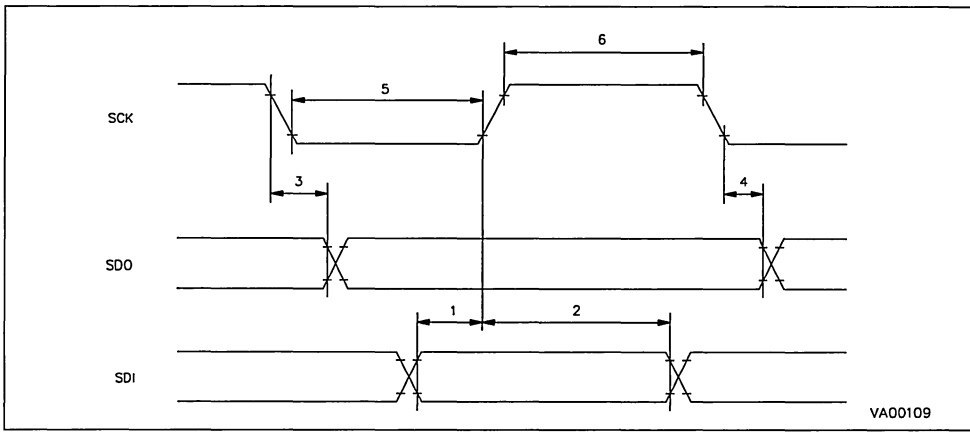


SPI TIMING TABLE (V_{DD} = 5V ± 10%, T_A = –40°C to +85°C, Cload = 50pF, INTCLK = 12MHz, Output Alternate Function set as Push-pull)

N°	Symbol	Parameter	Value		Unit
			Min.	Max.	
1	TsDI	Input Data Set-up Time	100		ns
2	ThDI (1)	Input Data Hold Time	1/2 TpC+100		ns
3	TdOV	SCK to Output Data Valid		100	ns
4	ThDO	Output Data Hold Time	-20		ns
5	TwSKL	SCK Low Pulse Width	300		ns
6	TwSKH	SCK High Pulse Width	300		ns

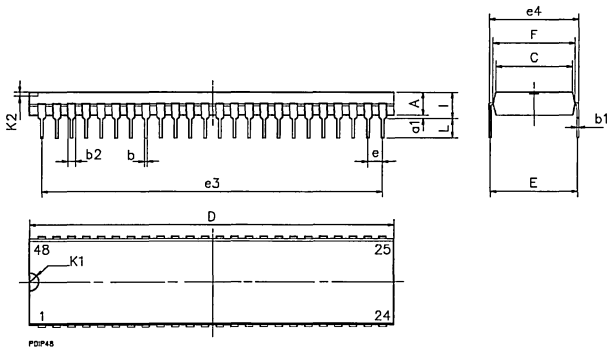
Note: 1. TpC is the Clock period.

SPI TIMING



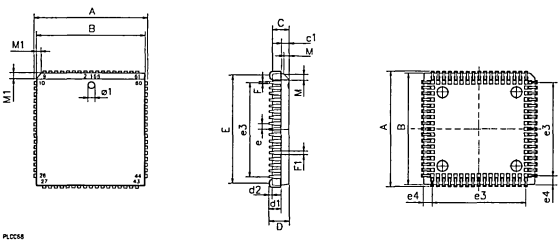
PACKAGE MECHANICAL DATA

Figure 53. 48-Pin Plastic Dual In Line (B)



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A	–	–	–	–	–	–
a1		0.63			0.024	
b		0.45			0.017	
b1	0.23		0.31	0.009		0.012
b2		1.27			0.050	
C	–	–	–	–	–	–
D			62.74			2.470
E	15.20		16.68	0.598		0.656
e		2.54			0.100	
e3		58.42			2.300	
e4	–	–	–	–	–	–
F			14.10			0.555
I		4.45			0.175	
L		3.30			0.129	

Figure 54. 68-Lead Plastic Leaded Chip Carrier (C)



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A	25.02		25.27	0.985		0.995
B	24.13		24.33	0.950		0.958
D	4.20		5.08	0.165		0.200
d1		2.54			0.100	
d2		0.56			0.022	
E	22.61		23.62	0.890		0.930
e		1.27			0.050	
F		0.38			0.015	
G			0.10			0.004
M		1.27			0.050	
M1		1.14			0.044	
Ø1		7.36			0.289	

ORDERING INFORMATION

Sales Type	Frequency	Temperature Range	Package
ST9030C6/XX	24MHz	– 40°C to + 85°C	PLCC68
ST9031B6/XX	24MHz	– 40°C to + 85°C	PDIP48
ST9030C1/XX	24MHz	0°C to + 70°C	PLCC68
ST9031B1/XX	24MHz	0°C to + 70°C	PDIP48

Note: "XX" is the ROM code identifier that is allocated by SGS-THOMSON after receipt of all required options and the related ROM file.

ST9030, ST9031 OPTION LIST

Please copy this page (enlarge if possible) and complete ALL sections. Send the form, with the ROM code image required, to your local SGS-THOMSON sales office.

Customer Company : [.....]

Company Address : [.....]

[.....]

Telephone : [.....]

FAX : [.....]

Contact : [.....] Telephone (Direct) : [.....]

Please confirm device required :

Device [ ] (d) Package [ ] (p) Temperature Range [ ] (t)

Special Marking [ ] (y/n) 11 characters for ST9030 [| | | | | | | | | | |] (N)

13 characters for ST9031 [| | | | | | | | | | | | |] (N)

Notes :

(d) 1 = ST9030, 2 = ST9031
(p) B = Dual In Line Package, C = Chip Carrier Plastic
(t) 1 = 0 to +70°C, 6 = -40 to +85°C
(N) Available : ASCII 020h - 05Fh

Please consult your local SGS-THOMSON sales office for other marking details

ROMLESS OPTION (consult text)
[ ] YES [ ] NO
If yes, identify required pin (Port.bit)
[ ] P3.7 [ ] P2.0

Code : [ ] EPROM (2764)
[ ] HEX format files on IBM-PC® compatible disk
filename : [.....]

Confirmation : [ ] Code checked with EPROM device in application

Yearly Quantity forecast : [.....] k units
- for a period of : [.....] years
Preferred Production start dates : [.....] (YY/MM/DD)

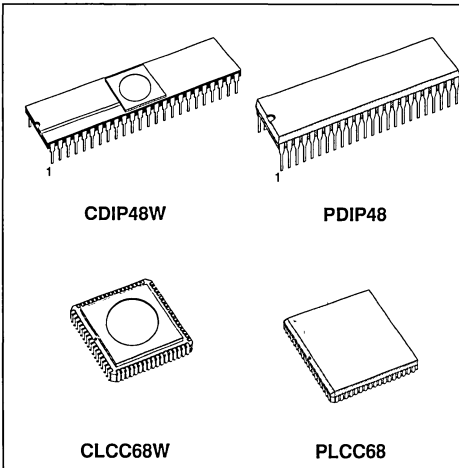
Customer Signature : [.....]

Date : [.....]

ST90E30-ST90E31
ST90T30-ST90T31

8K EPROM HCMOS MCUs WITH A/D CONVERTER

- Single chip microcontroller, 8K bytes of EPROM and 256 bytes of register file with 224 general purpose registers available as RAM, accumulator or index pointers.
- 8/16 bit CORE with full feature DMA controller and powerful interrupt handler and a standard Serial Peripheral Interface (SPI) handling S-BUS/I^2C Bus and IM BUS.
- Up to 8 external interrupts edge selectable plus 1 non-maskable interrupt.
- 16 bit programmable Timer with 8 bit Prescaler, able to be used as a Timer/Watchdog for system integrity.
- Two 16 bit Multifunction Timer modules, each with an 8 bit Prescaler and 13 operating modes, allowing simple use for complex waveform generation and measurement, PWM functions and many other system timing operations.
- 8 channel Analog to Digital Converter, with integral sample and hold, fast 11µs conversion time and 8 bit ± 1/2 LSB resolution with Analog Watchdog on two channels.
- Full function Serial Communication Interface with 110 to 375000 baud rate generator, asynchronous and byte synchronous capability (fully programmable format) and address/wake-up bit option.
- On-chip DMA channels associated with the Multifunction Timers and the Serial Communication Interface.
- Up to seven 8 bit I/O ports with programmable input thresholds and output characteristics. Alternative functions allow the full use of all pins.
- Powerful software development tools, including assembler, linker, C-compiler, archiver, software and hardware emulators.
- 68-lead Window Ceramic Leaded Chip Carrier package for ST90E30.
- 48-pin Window Dual in Line Ceramic Multilayer package for ST90E31.
- 68-lead Plastic Leaded Chip Carrier package for ST90T30.
- 48-pin Dual in Line Plastic package for ST90T31



CDIP48W PDIP48

CLCC68W PLCC68

(Ordering Information at the end of the datasheet)

Figure 1. ST90E31,T31 Pin Configuration

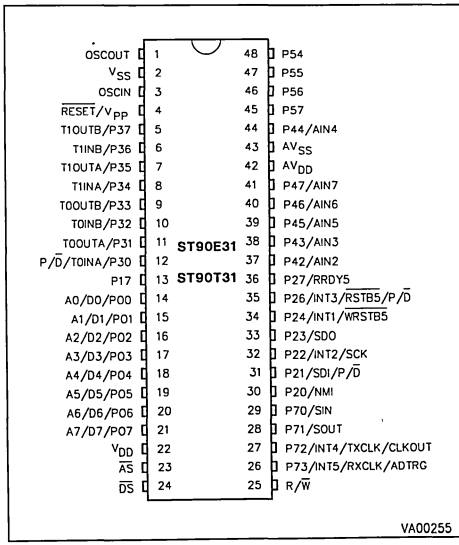


Figure 2. ST90E30,T30 Pin Configuration

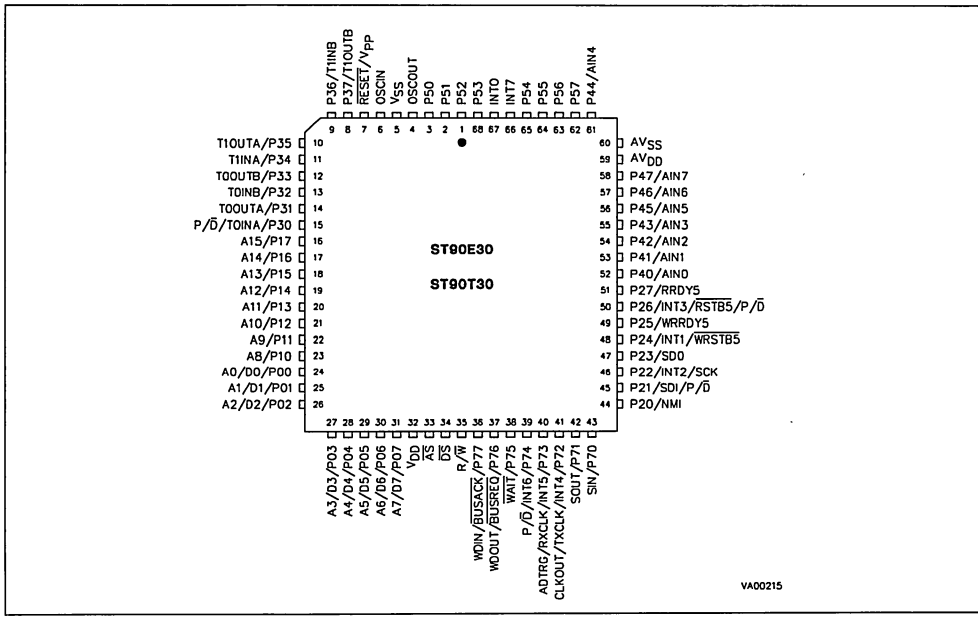
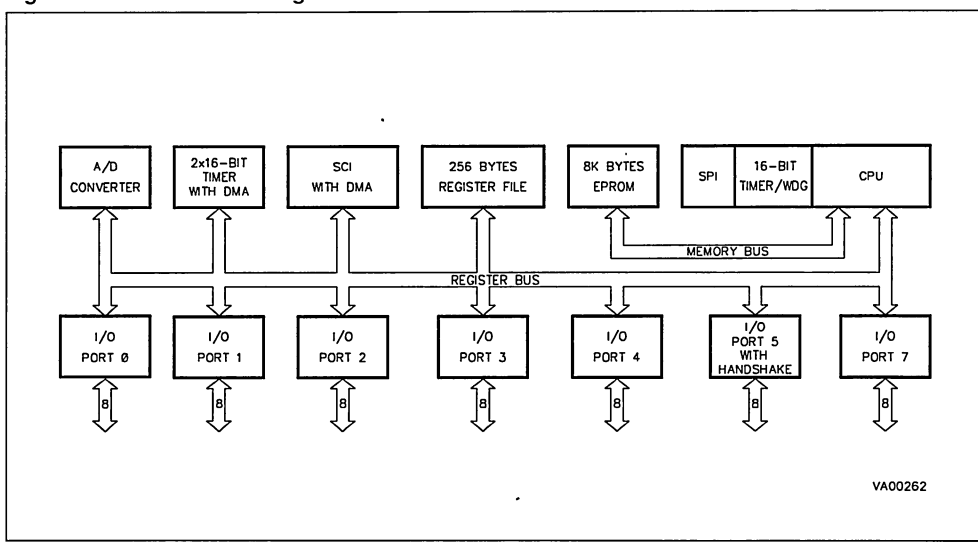


Figure 3. ST90E3X Block Diagram



GENERAL DESCRIPTION

The ST90E30, ST90E31, ST90T30 and ST90T31 (following mentioned as ST90E3X) are EPROM members of the ST9 family of microcontrollers, in windowed ceramic (E) and plastic OTP (T) packages respectively, completely developed and produced by SGS-THOMSON Microelectronics using a proprietary n-well HCMOS process.

The EPROM parts are fully compatible with their ROM versions and this datasheet will thus provide only information specific to the EPROM based devices.

THE READER IS ASKED TO REFER TO THE DATASHEET OF THE ST9030 ROM-BASED DEVICE FOR FURTHER DETAILS.

The EPROM ST90E3X may be used for the prototyping and pre-production phases of development, and can be configured as: standalone microcontrollers with 8K bytes of on-chip ROM, microcontrollers able to manage up to bytes of external memory, or as parallel processing elements in a system with other processors and peripheral controllers.

A key point of the ST90E3X architecture is related to its modular approach which allows software commonality with all other members of the ST9 family.

The nucleus of the modular design of the ST90E3X is the advanced Core which includes the Central Processing Unit (CPU), the Register File, a 16 bit Timer/Watchdog with 8 bit Prescaler, a Serial Peripheral Interface supporting S-BUS, I^2C Bus and IM BUS Interface, plus two 8 bit I/O ports. The Core has independent memory and register buses allowing a high degree of pipelining to add to the efficiency of the code execution speed of the extensive instruction set.

The powerful I/O capabilities demanded by microcontroller applications are fulfilled by the ST90E3X with up to 56 I/O lines dedicated to digital Input/Output. These lines are grouped into up to seven 8 bit I/O Ports and can be configured on a bit basis under software control to provide timing, status signals, an address/data bus for interfacing external memory, timer inputs and outputs, analog inputs, external interrupts and serial or parallel I/O with or without handshake.

Three memory spaces are available: Program Memory (internal and external), Data Memory (external) and the Register File, which includes the control and status registers of the on-chip peripherals.

Two 16 bit MultiFunction Timers, each with an 8 bit Prescaler and 13 operating modes allow simple use for complex waveform generation and measurement, PWM functions and many other system timing functions by the usage of the two associated DMA channels for each timer.

In addition there is an 8 channel Analog to Digital Converter with integral sample and hold, fast 11µs conversion time and 8 bit ±1/2 LSB resolution. An Analog Watchdog feature is included for two input channels.

Completing the device is a full duplex Serial Communications Interface with an integral 110 to 375000 baud rate generator, asynchronous and byte synchronous capability (fully programmable format) and associated address/wake-up option, plus two DMA channels.

PIN DESCRIPTION

$\overline{AS}$. *Address Strobe (output, active low, 3-state).* Address Strobe is pulsed low once at the beginning of each memory cycle. The rising edge of $\overline{AS}$ indicates that address, Read/Write (R/$\overline{W}$), and Data Memory signals are valid for program or data memory transfers. Under program control, $\overline{AS}$ can be placed in a high-impedance state along with Port 0 and Port 1, Data Strobe ($\overline{DS}$) and R/$\overline{W}$.

$\overline{DS}$. *Data Strobe (output, active low, 3-state).* Data Strobe provides the timing for data movement to or from Port 0 for each memory transfer. During a write cycle, data out is valid at the leading edge of $\overline{DS}$. During a read cycle, Data In must be valid prior to the trailing edge of $\overline{DS}$. When the ST90E3X accesses on-chip memory, $\overline{DS}$ is held high during the whole memory cycle. It can be placed in a high impedance state along with Port 0, Port 1, $\overline{AS}$ and R/$\overline{W}$.

R/$\overline{W}$. *Read/Write (output, 3-state).* Read/Write determines the direction of data transfer for external memory transactions. R/$\overline{W}$ is low when writing to external program or data memory, and high for all other transactions. It can be placed in a high impedance state along with Port 0, Port 1, $\overline{AS}$ and $\overline{DS}$.

$\overline{RESET}$/V_{PP}. *Reset (input, active low) or V_{PP} (input).* The ST9 is initialised by the Reset signal. With the deactivation of $\overline{RESET}$, program execution begins from the Program memory location pointed to by the vector contained in program memory locations 00h and 01h. In the EPROM programming Mode, this pin acts as the programming voltage input V_{PP}.

OSCIN, OSCOUT. *Oscillator (input and output).* These pins connect a parallel-resonant crystal (24MHz maximum), or an external source to the on-chip clock oscillator and buffer. OSCIN is the input of the oscillator inverter and internal clock generator; OSCOUT is the output of the oscillator inverter.

AV_{DD}. Analog V_{DD} of the Analog to Digital Converter.

AV_{SS}. Analog V_{SS} of the Analog to Digital Converter.

V_{DD}. Main Power Supply Voltage (5V ± 10%).

V_{SS}. Digital Circuit Ground.

PIN DESCRIPTION (Continued)

P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P70-P77. *I/O Port Lines (Input/Output, TTL or CMOS compatible).* 8 lines grouped into I/O ports of 8 bits, bit programmable under program control as general purpose I/O or as Alternate Functions (see next section).

I/O Port Alternate Functions. Each pin of the I/O ports of the ST90E3X may assume Alternative Functions as shown in the Pin Configuration Drawings. Due to Bonding options for the packages, some functions may not be present, Table 1 shows the Functions allocated to the I/O port pins and a summary of packages for which they are available.

Table 1. ST90E3X I/O Port Alternate Function Summary

I/O PORT	Name	Function	Alternate Function	Pin Assignment	
Port. bit				90E30	90E31
P0.0	A0/D0	I/O	Address/Data bit 0 mux	24	14
P0.1	A1/D1	I/O	Address/Data bit 1 mux	25	15
P0.2	A2/D2	I/O	Address/Data bit 2 mux	26	16
P0.3	A3/D3	I/O	Address/Data bit 3 mux	27	17
P0.4	A4/D4	I/O	Address/Data bit 4 mux	28	18
P0.5	A5/D5	I/O	Address/Data bit 5 mux	29	19
P0.6	A6/D6	I/O	Address/Data bit 6 mux	30	20
P0.7	A7/D7	I/O	Address/Data bit 7 mux	31	21
P1.0	A8	O	Address bit 8	23	–
P1.1	A9	O	Address bit 9	22	–
P1.2	A10	O	Address bit 10	21	–
P1.3	A11	O	Address bit 11	20	–
P1.4	A12	O	Address bit 12	19	–
P1.5	A13	O	Address bit 13	18	–
P1.6	A14	O	Address bit 14	17	–
P1.7	A15	O	Address bit 15	16	13
P2.0	NMI	I	Non-Maskable Interrupt	44	30
P2.1	P/$\overline{D}$	O	Program/Data Space Select	45	31
P2.1	SDI	I	SPI Serial Data Out	45	31
P2.2	INT2	I	External Interrupt 2	46	32
P2.2	SCK	O	SPI Serial Clock	46	32
P2.3	SDO	O	SPI Serial Data In	47	33
P2.4	INT1	I	External Interrupt 1	48	34
P2.4	$\overline{WRSTB5}$	O	Handshake Write Strobe P5	48	34
P2.5	WRRDY5	I	Handshake Write Ready P5	49	–
P2.6	INT3	I	External Interrupt 3	50	35
P2.6	$\overline{RDSTB5}$	I	Handshake Read Strobe P5	50	35
P2.6	P/$\overline{D}$	O	Program/Data Space Select	50	35
P2.7	RDRDY5	O	Handshake Read Ready P5	51	36
P3.0	T0INA	I	MF Timer 0 Input A	15	12
P3.0	P/$\overline{D}$	O	Program/Data Space Select	15	12
P3.1	T0OUTA	O	MF Timer 0 Output A	14	11

PIN DESCRIPTION (Continued)

Table 1. ST90E3X I/O Port Alternate Function Summary (Continued)

I/O PORT	Name	Function	Alternate Function	Pin Assignment	
Port. bit				90E30	90E31
P3.2	T0INB	I	MF Timer 0 Input B	13	10
P3.3	T0OUTB	O	MF Timer 0 Output B	12	9
P3.4	T1INA	I	MF Timer 1 Input A	11	8
P3.5	T1OUTA	O	MF Timer 1 Output A	10	7
P3.6	T1INB	I	MF Timer 1 Input B	9	6
P3.7	T1OUTB	O	MF Timer 1 Output B	8	5
P4.0	AIN0	I	A/D Analog Input 0	52	–
P4.1	AIN1	I	A/D Analog Input 1	53	–
P4.2	AIN2	I	A/D Analog Input 2	54	37
P4.3	AIN3	I	A/D Analog Input 3	55	38
P4.4	AIN4	I	A/D Analog Input 4	61	44
P4.5	AIN5	I	A/D Analog Input 5	56	39
P4.6	AIN6	I	A/D Analog Input 6	57	40
P4.7	AIN7	I	A/D Analog Input 7	58	41
P5.0		I/O	I/O Handshake Port 5	3	–
P5.1		I/O	I/O Handshake Port 5	2	–
P5.2		I/O	I/O Handshake Port 5	1	–
P5.3		I/O	I/O Handshake Port 5	68	–
P5.4		I/O	I/O Handshake Port 5	65	48
P5.5		I/O	I/O Handshake Port 5	64	47
P5.6		I/O	I/O Handshake Port 5	63	46
P5.7		$\overline{I/O}$	I/O Handshake Port 5	62	45
P7.0	SIN	I	SCI Serial Input	43	29
P7.1	SOUT	O	SCI Serial Output	42	28
P7.2	INT4	I	External Interrupt 4	41	27
P7.2	TXCLK	I	SCI Transmit Clock Input	41	27
P7.2	CLKOUT	O	SCI Byte Sync Clock Output	41	27
P7.3	INT5	I	External Interrupt 5	40	26
P7.3	RXCLK	I	SCI Receive Clock Input	40	26
P7.3	ADTRG	I	A/D Conversion Trigger	40	26
P7.4	INT6	I	External Interrupt 6	39	–
P7.4	$P/\overline{D}$	O	Program/Data Space Select	39	–
P7.5	$\overline{WAIT}$	I	External Wait Input	38	–
P7.6	WDOUT	O	T/WD Output	37	–
P7.6	$\overline{BUSREQ}$	I	External Bus Request	37	–
P7.7	WDIN	I	T/WD Input	36	–
P7.7	$\overline{BUSACK}$	O	External Bus Acknowledge	36	–

MEMORY

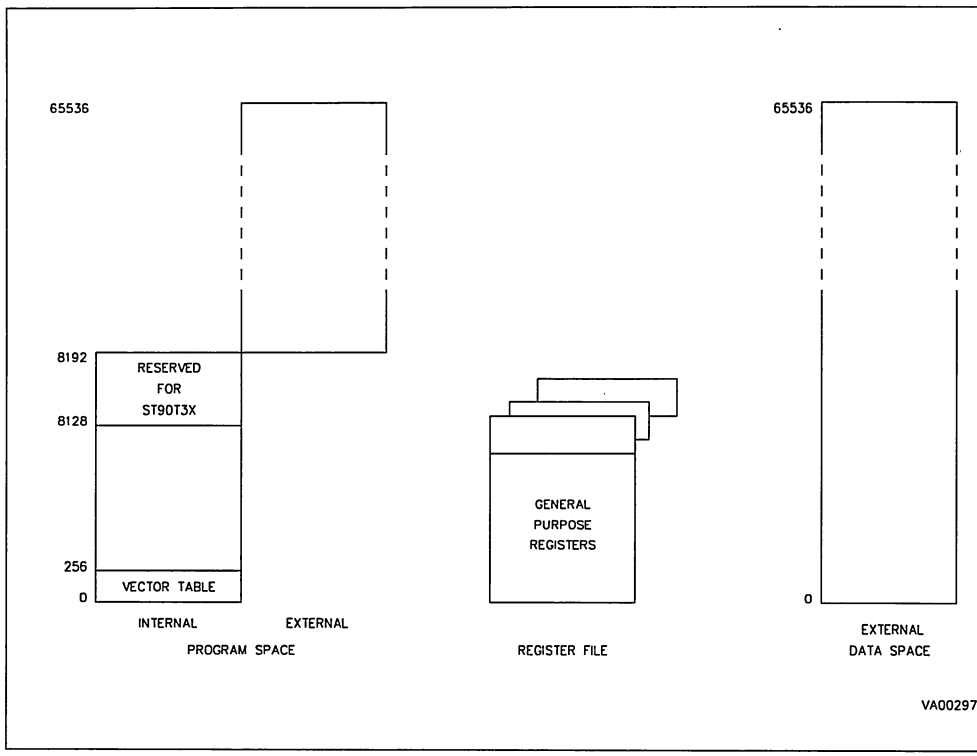
The memory of the ST90E3X is functionally divided into two areas, the Register File and Memory. The Memory may optionally be divided into two spaces, each having a maximum of 65,536 bytes. The two memory spaces are separated by function, one space for Program code, the other for Data. The ST90E3X 8K bytes of on-chip EPROM memory is selected at memory addresses 0 through 1FFFh (hexadecimal) in the Program Space, while the ST90T30 OTP version has the top 64 bytes of the program space reserved by SGS-THOMSON for testing purposes.

External memory may be addressed using the multiplexed address and data buses (Alternate Functions of Port 0 and Port 1). At addresses greater than the first 8K of program space, the ST90E3X executes external memory cycles for instruction fetches. Data Memory may be decoded externally by using the P/$\overline{D}$ Alternate Function output. The on-chip general purpose (GP) Registers may be used as RAM memory for minimum chip count systems.

EPROM PROGRAMMING

The 8192 bytes of EPROM memory of the ST90E30 and ST90E31 (8128 for the ST90T3X) may be programmed by using the EPROM Programming Boards (EPB) available from SGS-THOMSON.

Figure 4. Memory Spaces



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	– 0.3 to 7.0	V
AV_{DD}, AV_{SS}	Analog Supply Voltage	$V_{SS} \le AV_{SS} < AV_{DD} \le V_{DD}$	V
V_I	Input Voltage	V_{SS} – 0.3 to V_{DD} +0.3	V
V_O	Output Voltage	V_{SS} – 0.3 to V_{DD} +0.3	V
V_{PP}	Input Voltage on V_{PP} Pin	– 0.3 to 13.5	V
T_{STG}	Storage Temperature	– 55 to + 150	°C

Note: Stresses above those listed as "absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value		Unit
		Min.	Max.	
T_A	Operating Temperature	– 40	85	°C
V_{DD}	Operating Supply Voltage	4.5	5.5	V
f_{OSCE}	External Oscillator Frequency		24	MHz
f_{OSCI}	Internal Oscillator Frequency		12	MHz

DC ELECTRICAL CHARACTERISTICS

(V_{DD} = 5V ± 10% T_A = – 40 °C to + 85°C, unless otherwise specified)

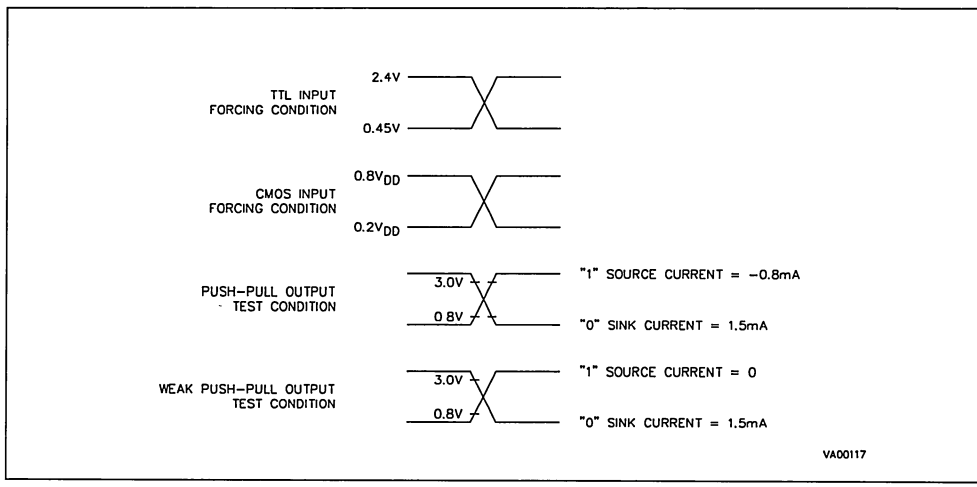
Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
V_{IHCK}	Clock Input High Level	External Clock	0.7 V_{DD}		V_{DD} + 0.3	V
V_{ILCK}	Clock Input Low Level	External Clock	– 0.3		0.3 V_{DD}	V
V_{IH}	Input High Level	TTL	2.0		V_{DD} + 0.3	V
		CMOS	0.7 V_{DD}		VDD + 0.3	V
V_{IL}	Input Low Level	TTL	– 0.3		0.8	V
		CMOS	– 0.3		0.3 V_{DD}	V
V_{IHRS}	Reset Input High Level		0.7 V_{DD}		V_{DD} + 0.3	V
V_{ILRS}	Reset Input Low Level		–0.3		0.3 V_{DD}	V
V_{HYRS}	Reset Input Hysteresis		0.3		1.5	V
V_{OH}	Output High Level	Push Pull, Iload = – 0.8mA	V_{DD} – 0.8			V
V_{OL}	Output Low Level	Push Pull or Open Drain, Iload = – 1.6mA			0.4	V
I_{WPU}	Weak Pull-up Current	Bidirectional Weak Pull-up, V_{OL} = 0V	– 80	– 200	– 420	µA

DC ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
I_{APU}	Active Pull-up Current, for INT0 and INT7 only	$V_{IN} < 0.8V$	– 80	– 200	– 420	µA
I_{LKIO}	I/O Pin Input Leakage	Input/Tri-State, $0V < V_{IN} < V_{DD}$	– 10		+ 10	µA
I_{LKRS}	Reset Pin Input Leakage	$0V < V_{IN} < V_{DD}$	– 30		+ 30	µA
I_{LKAD}	A/D Pin Input Leakage	Alternate Function, Open Drain, $0V < V_{IN} < V_{DD}$	– 3		+ 3	µA
I_{LKAP}	Active Pull-up Input Leakage	$0V < V_{IN} < 0.8V$	– 10		+ 10	µA
I_{LKOS}	OSCIN Pin Input Leakage	$0V < V_{IN} < V_{DD}$	– 10		+ 10	µA
I_{DD}	Run Mode Current	24MHz, Note 1		32	70	mA
		4MHz, Note 1		6	12	mA
I_{DP2}	Run Mode Current Prescale by 2	24MHz, Note 1		19	40	mA
		4MHz, Note 1		4	8	mA
I_{WFI}	WFI Mode Current	24MHz, Note 1		9	18	mA
		4MHz, Note 1		2.5	5	mA
I_{HALT}	HALT Mode Current	24MHz, Note 1			100	µA
V_{PP}	EPROM Programming Voltage		12.2	12.5	12.8	V
I_{PP}	EPROM Programming Current				30	mA

Note: 1. All I/O Ports are configured in Bidirectional Weak Pull-up Mode with no DC load, External Clock pin (OSCIN) is driven by square wave external clock. No peripheral working. External interface not active (Internal Program Execution).

DC TEST CONDITIONS



AC ELECTRICAL CHARACTERISTICS

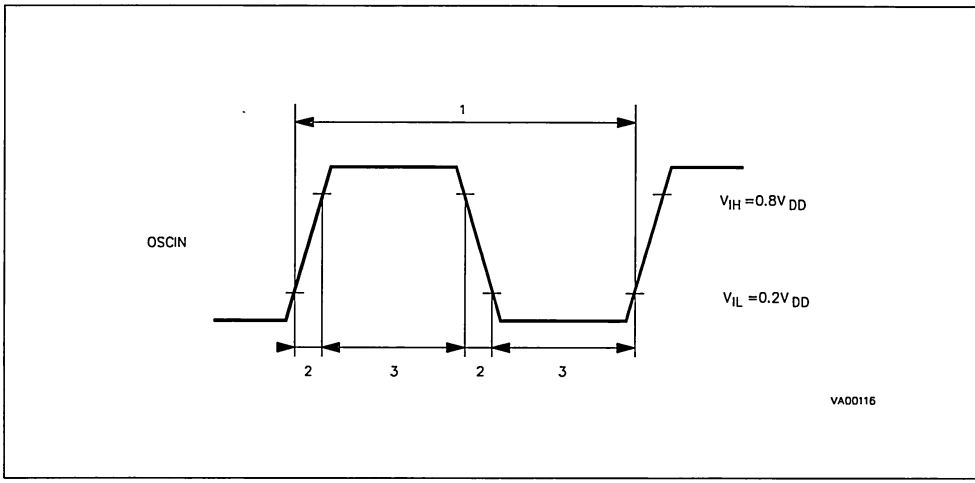
CLOCK TIMING TABLE

(V_{DD} = 5V ± 10%, T_A = − 40°C to + 85°C, unless otherwise specified)

N°	Symbol	Parameter	Value		Unit	Note
			Min.	Max.		
1	TpC	OSCIN Clock Period	41.5		ns	a
			83		ns	b
2	TrC, TfC	OSCIN Rise and Fall Time		12	ns	
3	TwCL, TwCH	OSCIN Low and High Width	25	12	ns	a
			38		ns	b

Notes:
a. Clock divided by 2 internally (MODER.DIV2=1)
b. Clock not divided by 2 internally (MODER.DIV2=0)

CLOCK TIMING



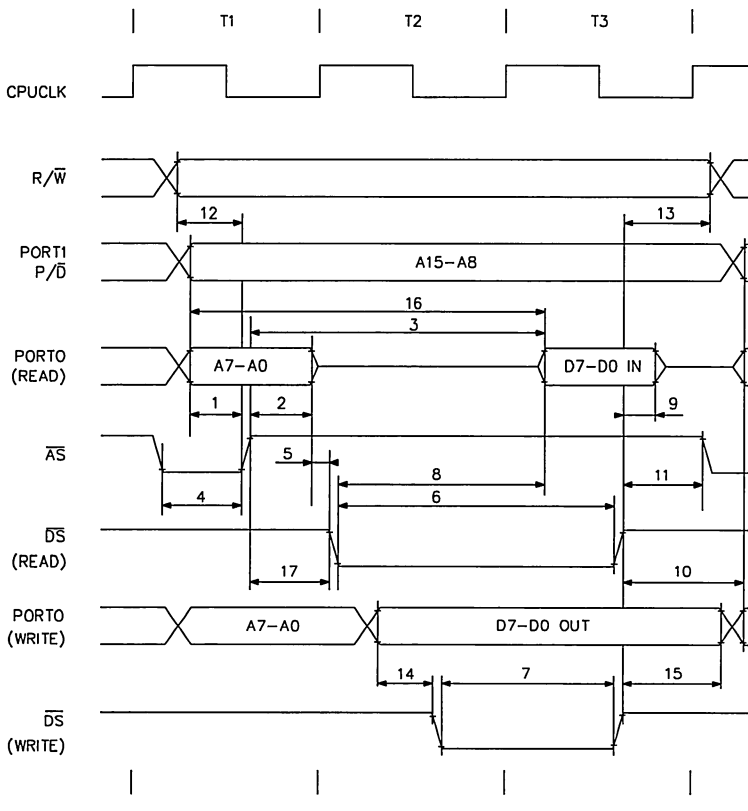
EXTERNAL BUS TIMING TABLE (V_{DD} = 5V ± 10%, T_A = – 40 °C to + 85 °C, Cload = 50pF, INTCLK = 12MHz, unless otherwise specified)

N°	Symbol	Parameter	Value (Note)				Unit
			OSCIN Divided By 2	OSCIN Not Divided By 2	Min.	Max.	
1	TsA (AS)	Address Set-up Time before $\overline{AS}$ ↑	TpC (2P+1) –22	TwCH+PTpC –18	20		ns
2	ThAS (A)	Address Hold Time after $\overline{AS}$ ↑	TpC –17	TwCL –13	25		ns
3	TdAS (DR)	$\overline{AS}$ ↑ to Data Available (read)	TpC (4P+2W+4) –52	TpC (2P+W+2) –51		115	ns
4	TwAS	$\overline{AS}$ Low Pulse Width	TpC (2P+1) –7	TwCH+PTpC –3	35		ns
5	TdAz (DS)	Address Float to $\overline{DS}$ ↓	0	0	0		ns
6	TwDSR	$\overline{DS}$ Low Pulse Width (read)	TpC (4P+2W+3) –20	TwCH+TpC (2P+W+1) –16	105		ns
7	TwDSW	$\overline{DS}$ Low Pulse Width (write)	TpC (2P+2W+2) –13	TpC (P+W+1) –13	70		ns
8	TdDSR (DR)	$\overline{DS}$ ↓ to Data Valid Delay (read)	TpC (4P+2W-3) –50	TwCH+TpC(2P+W+1) –46		75	ns
9	ThDR (DS)	Data to $\overline{DS}$ ↑ Hold Time (read)	0	0	0		ns
10	TdDS (A)	$\overline{DS}$ ↑ to Address Active Delay	TpC –7	TwCL –3	35		ns
11	TdDS (AS)	$\overline{DS}$ ↑ to $\overline{AS}$ ↓ Delay	TpC –18	TwCL –14	24		ns
12	TsR/W (AS)	R/$\overline{W}$ Set-up Time before $\overline{AS}$ ↑	TpC (2P+1) –22	TwCH+PTpC –18	20		ns
13	TdDSR (R/W)	$\overline{DS}$ ↑ to R/$\overline{W}$ and Address Not Valid Delay	TpC –9	TwCL –5	33		ns
14	TdDW (DSW)	Write Data Valid to $\overline{DS}$ ↓ Delay (write)	TpC (2P+1) –32	TwCH+PTpC –28	10		ns
15	ThDS (DW)	Data Hold Time after DS ↑ (write)	TpC –9	TwCL –5	33		ns
16	TdA (DR)	Address Valid to Data Valid Delay (read)	TpC (6P+2W+5) –68	TwCH+TpC (3P+W+2) –64		140	ns
17	TdAs (DS)	$\overline{AS}$ ↑ to $\overline{DS}$ ↓ Delay	TpC –18	TwCL –14	24		ns

Note: The value left hand two columns show the formula used to calculate the timing minimum or maximum from the oscillator clock period, prescale value and number of wait cycles inserted.
The value right hand two columns show the timing minimum and maximum for an external clock at 24 MHz divided by 2, prescaler value of zero and zero wait status.

Legend:
P = Clock Prescaling Value
W = Wait Cycles
TpC = OSCIN Period
TwCH = High Level OSCIN half period
TwCL = Low Level OSCIN half period

EXTERNAL BUS TIMING

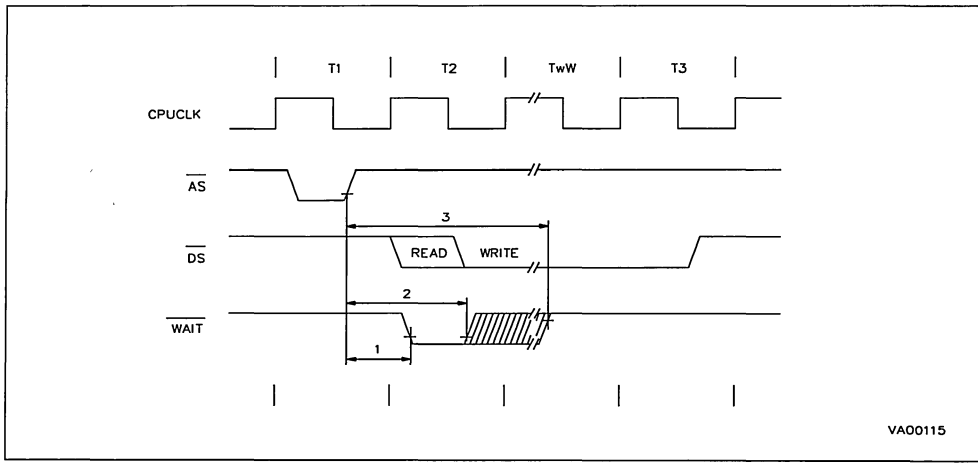


EXTERNAL WAIT TIMING TABLE (V_{DD} = 5V ± 10%, T_A = –40°C to +85°C, Cload = 50pF, INTCLK = 12MHz, Push-pull output configuration, unless otherwise specified)

N°	Symbol	Parameter	Value (Note)				Unit
			OSCIN Divided By 2	OSCIN Not Divided By 2	Min.	Max.	
1	TdAS (WAIT)	$\overline{AS}$ ↑ to $\overline{WAIT}$ ↓ Delay	2(P+1)TpC –29	(P+1)TpC –29		40	ns
2	TdAS (WAIT)	$\overline{AS}$ ↑ to $\overline{WAIT}$ ↑ Minimum Delay	2(P+W+1)TpC –4	(P+W+1)TpC –4	80		ns
3	TdAS (WAIT)	$\overline{AS}$ ↑ to $\overline{WAIT}$ ↑ Maximum Delay	2(P+W+1)TpC –29	(P+W+1)TpC –29		83W+40	ns

Note: The value left hand two columns show the formula used to calculate the timing minimum or maximum from the oscillator clock period, prescale value and number of wait cycles inserted.
The value right hand two columns show the timing minimum and maximum for an external clock at 24 MHz divided by 2, prescale value of zero and zero wait status.

EXTERNAL WAIT TIMING

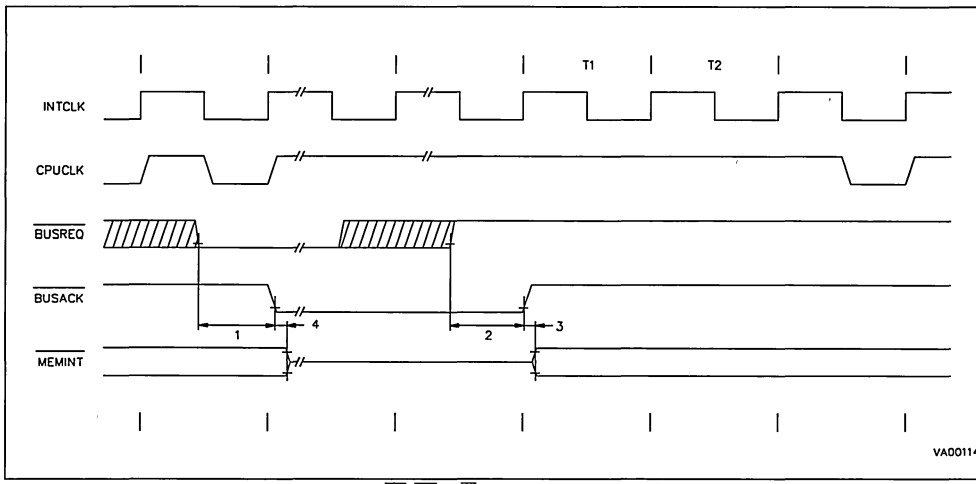


BUS REQUEST/ACKNOWLEDGE TIMING TABLE (V_{DD} = 5V ± 10%, T_A = −40°C to +85°C, Cload = 50pF, INTCLK = 12MHz, Push-pull output configuration, unless otherwise specified)

N°	Symbol	Parameter	Value (Note)				Unit
			OSCIN Divided By 2	OSCIN Not Divided By 2	Min.	Max.	
1	TdBR (BACK)	$\overline{BREQ}$ ↓ to $\overline{BUSACK}$ ↓	TpC+8	TwCL+12	50		ns
			TpC(6P+2W+7)+65	TpC(3P+W+3)+TwCL+65		360	ns
2	TdBR (BACK)	$\overline{BREQ}$ ↑ to $\overline{BUSACK}$ ↑	3TpC+60	TpC+TwCL+60		185	ns
3	TdBACK (BREL)	$\overline{BUSACK}$ ↓ to Bus Release	20	20		20	ns
4	TdBACK (BACT)	$\overline{BUSACK}$ ↑ to Bus Active	20	20		20	ns

Note: The value left hand two columns show the formula used to calculate the timing minimum or maximum from the oscillator clock period, prescale value and number of wait cycles inserted.
The value right hand two columns show the timing minimum and maximum for an external clock at 24 MHz divided by 2, prescale value of zero and zero wait status.

BUS REQUEST/ACKNOWLEDGE TIMING



Note : MEMINT = group of memory interface signals : $\overline{AS}$, $\overline{DS}$, R/$\overline{W}$, P00-P07, P10-P17.

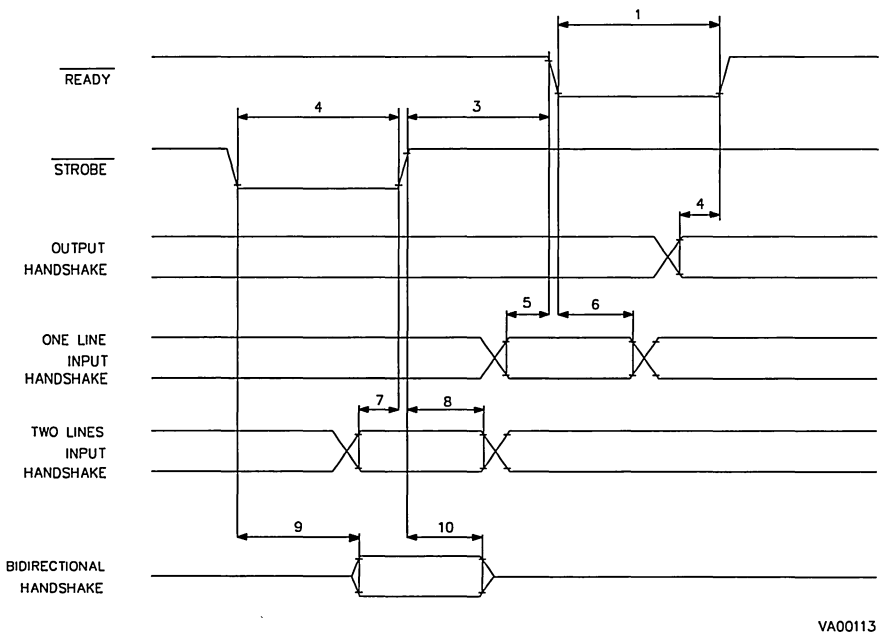
HANDSHAKE TIMING TABLE (V_{DD} = 5V ± 10%, T_A = –40°C to +85°C, Cload = 50pF, INTCLK = 12MHz, Push-pull output configuration, unless otherwise specified)

N°	Symbol	Parameter	Value (Note)				Min.	Max.	Unit
			OSCIN Divided By 2		OSCIN Not Divided By 2				
			Min.	Max.	Min.	Max.			
1	TwRDY	RDRDY, WRRDY Pulse Width in One Line Handshake	2TpC (P+W+1) –18		TpC (P+W+1) –18		65		ns
2	TwSTB	$\overline{RDSTB}$, $\overline{WRSTB}$ Pulse Width	2TpC+12		TpC+12		95		ns
3	TdST (RDY)	$\overline{RDSTB}$, or $\overline{WRSTB}$ ↑ to RDRDY or WRRDY ↓		TpC+45		(TpC-TwCL) +45		87	ns
4	TsPD (RDY)	Port Data to RDRDY ↑ Set-up Time	(2P+2W+1) TpC –25		TwCH+(W+P) TpC –25		16		ns
5	TsPD (RDY)	Port Data to WRRDY ↓ Set-up Time in One Line Handshake	43		43		43		ns
6	ThPD (RDY)	Port Data to WRRDY ↓ Hold Time in One Line Handshake	0		0		0		ns
7	TsPD (STB)	Port Data to $\overline{WRSTB}$ ↑ Set-up Time	10		10		10		ns
8	ThPD (STB)	Port Data to WRSTB ↑ Hold Time	25		25		25		ns
9	TdSTB (PD)	$\overline{RDSTBD}$ ↑ to Port Data Delay Time in Bidirectional Handshake		35		35		35	ns
10	TdSTB (PHZ)	$\overline{RDSTB}$ ↑ to Port High-Z Delay Time in Bidirectional Handshake		25		25		25	ns

Note: The value left hand two columns show the formula used to calculate the timing minimum or maximum from the oscillator clock period, prescale value and number of wait cycles inserted.
The value right hand two columns show the timing minimum and maximum for an external clock at 24 MHz divided by 2, prescaler value of zero and zero wait status.

Legend:
P = Clock Prescaling Value (R235.4,3,2)
W = Programmable Wait Cycles (R252.2.1.0/5,4,3) + External Wait Cycles

HANDSHAKE TIMING

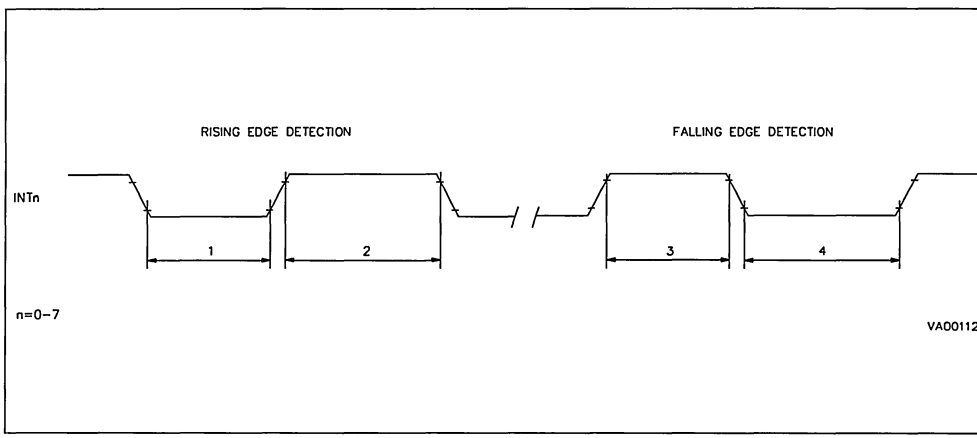


EXTERNAL INTERRUPT TIMING TABLE (V_{DD} = 5V ± 10%, T_A = –40°C to +85°C, Cload = 50pF, INTCLK = 12MHz, Push-pull output configuration, unless otherwise specified)

N°	Symbol	Parameter	Value (Note)				Unit
			OSCIN Divided By 2 Min.	OSCIN Not Divided By 2 Min.	Min.	Max.	
1	TwLR	Low Level Minimum Pulse Width in Rising Edge Mode	2TpC+12	TpC+12	95		ns
2	TwHR	High Level Minimum Pulse Width in Rising Edge Mode	2TpC+12	TpC+12	95		ns
3	TwHF	High Level Minimum Pulse Width in Falling Edge Mode	2TpC+12	TpC+12	95		ns
4	TwLF	Low Level Minimum Pulse Width in Falling Edge Mode	2TpC+12	TpC+12	95		ns

Note: The value left hand two columns show the formula used to calculate the timing minimum or maximum from the oscillator clock period, prescale value and number of wait cycles inserted.
The value right hand two columns show the timing minimum and maximum for an external clock at 24 MHz divided by 2, prescale value of zero and zero wait status.

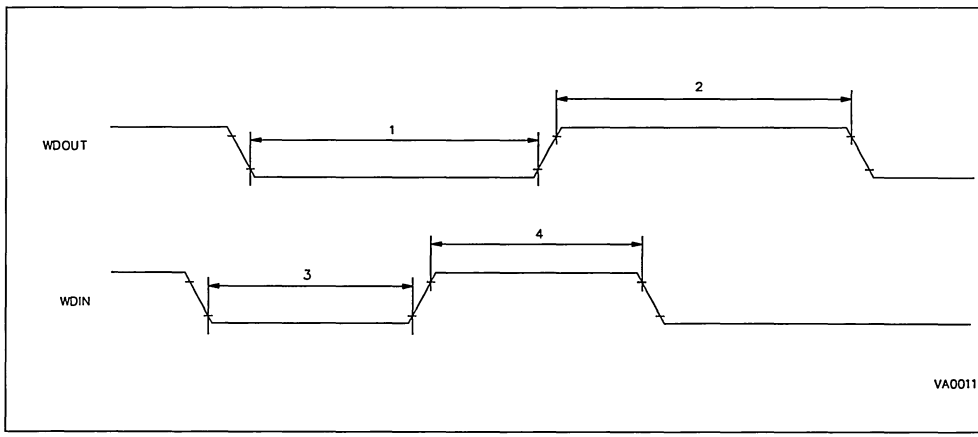
EXTERNAL INTERRUPT TIMING



WATCHDOG TIMING TABLE (V_{DD} = 5V ± 10%, T_A = –40°C to +85°C, Cload = 50pF, INTCLK = 12MHz, Output Alternate Function set as Push-pull)

N°	Symbol	Parameter	Value		Unit
			Min.	Max.	
1	TwWDOL	WDOUT Low Pulse Width	620		ns
2	TwWDOH	WDOUT High Pulse Width	620		ns
3	TwWDIL	WDIN Low Pulse Width	350		ns
4	TwWDIH	WDIN High Pulse Width	350		ns

WATCHDOG TIMING

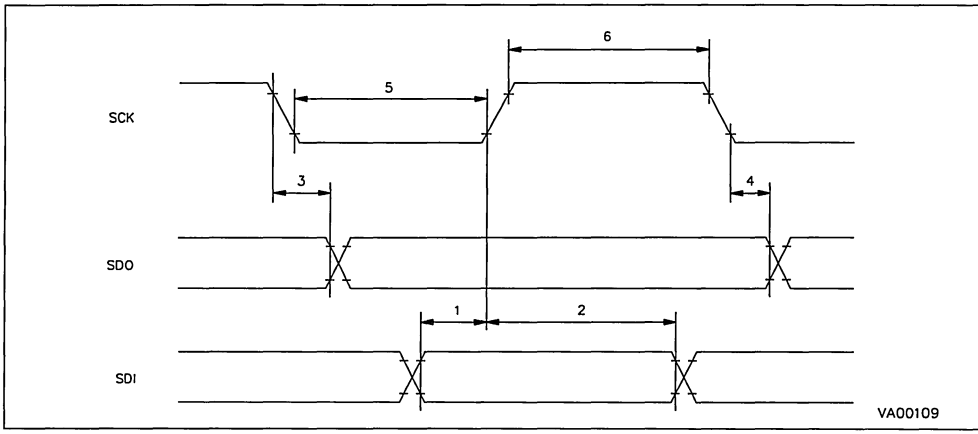


SPI TIMING TABLE (V_{DD} = 5V ± 10%, T_A = –40°C to +85°C, Cload = 50pF, INTCLK = 12MHz, Output Alternate Function set as Push-pull)

N°	Symbol	Parameter	Value		Unit
			Min.	Max.	
1	TsDI	Input Data Set-up Time	100		ns
2	ThDI (1)	Input Data Hold Time	1/2 TpC+100		ns
3	TdOV	SCK to Output Data Valid		100	ns
4	ThDO	Output Data Hold Time	-20		ns
5	TwSKL	SCK Low Pulse Width	300		ns
6	TwSKH	SCK High Pulse Width	300		ns

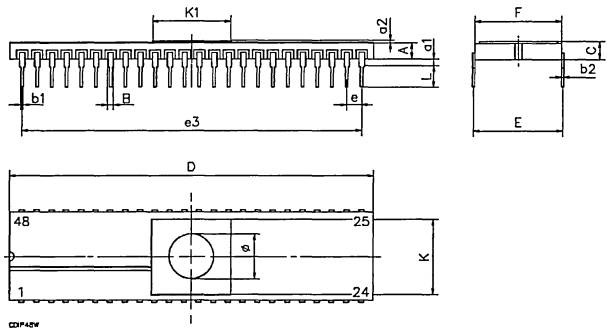
Note: 1. TpC is the Clock period.

SPI TIMING



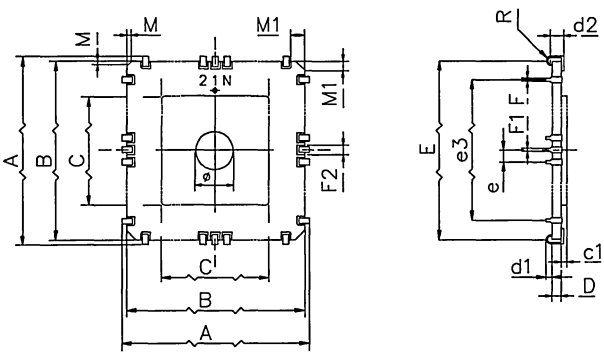
PACKAGES MECHANICAL DATA

Figure 5. 48-Pin Window Dual In Line Ceramic Multilayer (D), 600-Mil Width



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A	–	–	–	–	–	–
a1		1.27			0.050	
a2			1.30			0.051
B		1.02			0.040	
b1		0.45			0.017	
b2		0.25			0.010	
C		3.50			0.137	
D			61.59			2.424
E		15.24			0.600	
e		2.54			0.100	
e3		58.42			2.300	
F			15.34			0.604
L		3.30			0.130	
K		13.46			0.530	
K1		13.46			0.530	
Ø		7.62			0.300	

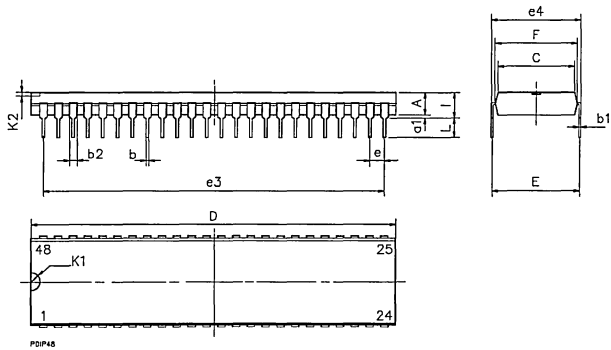
Figure 6. 68-Lead Window Ceramic Leaded Chip Carrier (L)



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A		25.14			0.989	
B	23.87		24.51	0.939		0.964
C			15.45			0.608
C1			1.30			0.051
D	1.82		2.23	0.071		0.087
d1	–	–	–	–	–	–
d2	–	–	–	–	–	–
E	–	–	–	–	–	–
e		1.27			0.050	
e3	–	–	–	–	–	–
F		0.45			0 017	
F1		0.63			0.025	
F2	–	–	–	–	–	–
M	–	–	–	–	–	–
M1	–	–	–	–	–	–
R		0.76			0.030	
Ø		8.89			0.350	

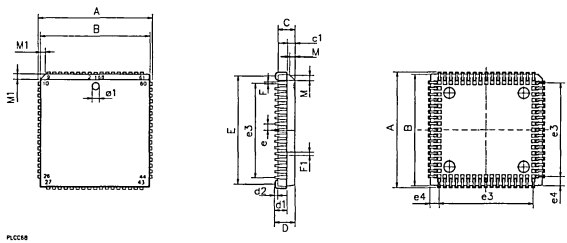
PACKAGES MECHANICAL DATA (continued)

Figure 7. 48-Pin Dual In Line Plastic (B), 600-Mil Width



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A	–	–	–	–	–	–
a1		0.63			0.024	
b		0.45			0.017	
b1	0.23		0.31	0.009		0.012
b2		1.27			0.050	
C	–	–	–	–	–	–
D			62.74			2.470
E	15.20		16.68	0.598		0.656
e		2.54			0.100	
e3		58.42			2.300	
e4	–	–	–	–	–	–
F			14.10			0.555
I		4.45			0.175	
L		3.30			0.129	

Figure 8. 68-Lead Plastic Leaded Chip Carrier (C)



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A	25.02		25.27	0.985		0.995
B	24.13		24.33	0.950		0.958
D	4.20		5.08	0.165		0.200
d1		2.54			0.100	
d2		0.56			0.022	
E	22.61		23.62	0.890		0.930
e		1.27			0.050	
F		0.38			0.015	
G			0.10			0.004
M		1.27			0.050	
M1		1.14			0.044	
Ø1		7.36			0.289	

ORDERING INFORMATION

Sales Type	Frequency	Temperature Range	Package
ST90E30L6	24MHz	– 40°C to + 85°C	CLCC68W
ST90T30C6	24MHz	– 40°C to + 85°C	PLCC68
ST90E31D6	24MHz	– 40°C to + 85°C	CDIP48W
ST90T31B6	24MHz	– 40°C to + 85°C	PDIP48
ST90E30L1	24MHz	0°C to +70°C	CLCC68W
ST90T30C1	24MHz	0°C to +70°C	PLCC68
ST90E31D1	24MHz	0°C to +70°C	CDIP48W
ST90T31B1	24MHz	0°C to +70°C	PDIP48

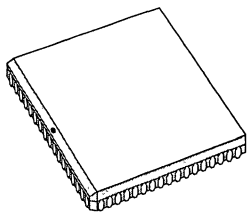
SGS-THOMSON MICROELECTRONICS

ST90R30

ROMLESS HCMOS MCU WITH A/D CONVERTER

ADVANCE DATA

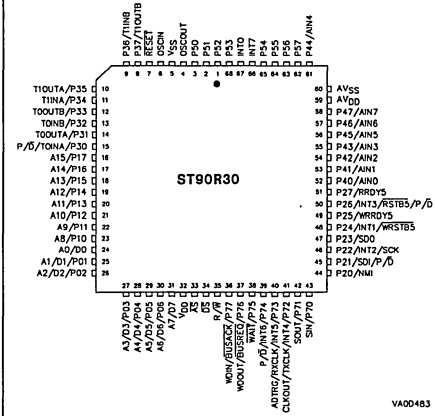
- Single chip microcontroller with 256 bytes of register file with 224 general purpose registers available as RAM, accumulators or index pointers.
- Romless to allow maximum external memory flexibility in development and production phases.
- 8/16 bit CORE with full feature DMA controller, a powerful interrupt handler and a Standard Serial Peripheral Interface (SPI) handling S-BUS, I^2C-bus, IM-bus and Standard Serial Peripheral Interfaces.
- Up to 8 external interrupts edge-selectable plus 1 non-maskable interrupt.
- 16 bit programmable Timer with 8 bit Prescaler, able to be used as a Watchdog Timer for system integrity.
- Two 16 bit Multifunction Timer modules, each with an 8 bit prescaler and 13 operating modes, allowing simple use for complex waveform generation and measurement, PWM functions and many other system timing operations.
- 8 channel Analog to Digital Converter, with integral sample and hold, fast 11µs conversion time, 8 bit ±1/2 LSB resolution with Analog Watchdog on two channels.
- Full function Serial Communications Interface with 110 to 375000 baud rate generator, asynchronous and byte synchronous capability (fully programmable format) and address/wake-up bit option.
- On-chip DMA channels associated to the Multifunction Timers and the Serial Communications Interface.
- Up to six 8 bit I/O ports with programmable input thresholds and output characteristics. Alternative functions allow the full use of all pins.
- Powerful software development tools, including assembler, linker, C-compiler, archiver, software and hardware emulators.
- Compatible with ST9030, 8k ROM devices (also available in windowed and One Time Programmable EPROM packages).
- 68-lead Plastic Leaded Chip Carrier package for ST90R30.



PLCC68

(Ordering Information at the end of the datasheet)

Figure 1. ST90R30 Pin Configuration



GENERAL DESCRIPTION

The ST90R30 is a ROMLESS member of the ST9 family of microcontrollers, completely developed and produced by SGS-THOMSON Microelectronics using a proprietary n-well HCMOS process.

The ROMLESS part may be used for the prototyping and pre-production phases of development, and offers the maximum in program flexibility in production systems.

The ST90R30 is fully compatible with the ST9030 ROM version and this datasheet will thus provide only information specific to the ROMLESS device.

THE READER IS ASKED TO REFER TO THE DATASHEET OF THE ST9030 ROM-BASED DEVICE FOR FURTHER DETAILS.

The ROMLESS ST90R30 can be configured as a microcontroller able to manage up to 128K bytes of external memory, or as a parallel processing element in a system with other processors and peripheral controllers.

A key point of the ST90R30 architecture is related to its modular approach which allows software commonality with all other members of the ST9 family.

The nucleus of the modular design of the ST90R30 is the advanced Core which includes the Central Processing Unit (CPU), the Register File, a 16 bit Timer/Watchdog with 8 bit Prescaler, a Serial Peripheral Interface supporting S-BUS, I^2C-bus and IM-bus Interface, plus two 8 bit I/O ports. The Core has independent memory and register buses allowing a high degree of pipelining to add to the efficiency of the code execution speed of the extensive instruction set.

The powerful I/O capabilities demanded by microcontroller applications are fulfilled by the ST90R30 with up to 48 I/O lines dedicated to digital Input/Output. These lines are grouped into up to six 8 bit I/O Ports and can be configured on a bit basis under software control to provide timing and status signals, address lines, timer inputs and outputs, analog inputs, external interrupts and serial or parallel I/O with or without handshake.

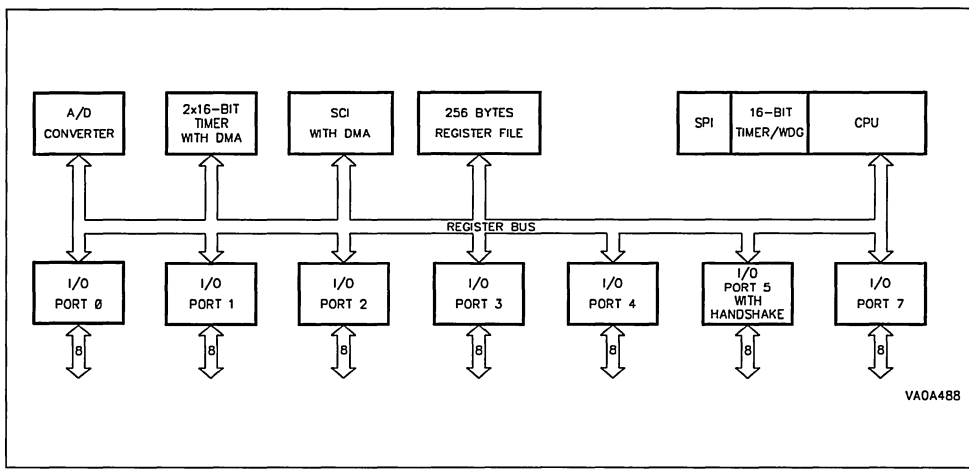
Three memory spaces are available: Program Memory (external), Data Memory (external) and the Register File, which includes the control and status registers of the on-chip peripherals.

Two 16 bit MultiFunction Timers, each with an 8 bit Prescaler and 13 operating modes allow simple use for complex waveform generation and measurement, PWM functions and many other system timing functions by the usage of the two associated DMA channels for each timer.

In addition there is an 8 channel Analog to Digital Converter with integral sample and hold, fast 11µs conversion time and 8 bit ±1/2 LSB resolution. An Analog Watchdog feature is included for two input channels.

Completing the device is a full duplex Serial Communications Interface with an integral 110 to 375000 baud rate generator, asynchronous and byte synchronous capability (fully programmable format) and associated address/wake-up option, plus two DMA channels.

Figure 2. ST90R30 Block Diagram



PIN DESCRIPTION

$\overline{AS}$. *Address Strobe (output, active low, 3-state).* Address Strobe is pulsed low once at the beginning of each memory cycle. The rising edge of $\overline{AS}$ indicates that address, Read/Write (R/$\overline{W}$), and Data Memory signals are valid for program or data memory transfers. Under program control, $\overline{AS}$ can be placed in a high-impedance state along with Port 0 and Port 1, Data Strobe ($\overline{DS}$) and R/$\overline{W}$.

$\overline{DS}$. *Data Strobe (output, active low, 3-state).* Data Strobe provides the timing for data movement to or from Port 0 for each memory transfer. During a write cycle, data out is valid at the leading edge of $\overline{DS}$. During a read cycle, Data In must be valid prior to the trailing edge of $\overline{DS}$. It can be placed in a high impedance state along with Port 0, Port 1, $\overline{AS}$ and R/$\overline{W}$.

R/$\overline{W}$. *Read/Write (output, 3-state).* Read/Write determines the direction of data transfer for memory transactions. R/$\overline{W}$ is low when writing to program or data memory, and high for all other transactions. It can be placed in a high impedance state along with Port 0, Port 1, $\overline{AS}$ and $\overline{DS}$.

$\overline{RESET}$. *Reset (input, active low).* The ST9 is initialised by the Reset signal. With the deactivation of $\overline{RESET}$, program execution begins from the Program memory location pointed to by the vector contained in program memory locations 00h and 01h.

OSCIN, OSCOUT. *Oscillator (input and output).* These pins connect a parallel-resonant crystal (24MHz maximum), or an external source to the on-chip clock oscillator and buffer. OSCIN is the input of the oscillator inverter and internal clock generator; OSCOUT is the output of the oscillator inverter.

AV_{DD}. Analog V_{DD} of the Analog to Digital Converter.

AV_{SS}. Analog V_{SS} of the Analog to Digital Converter.

V_{DD}. Main Power Supply Voltage (5V±10%)

V_{SS}. Digital Circuit Ground.

AD0-AD7, (P0.0-P0.7) *Address/Data Lines (Input/Output, TTL or CMOS compatible).* 8 lines providing a multiplexed address and data bus, under control of the $\overline{AS}$ and $\overline{DS}$ timing signals.

P1.0-P1.7, P2.0-P2.7 P3.0-P3.7, P4.0-P4.7, P5.0-P5.7, P7.0-P7.7 *I/O Port Lines (Input/Output, TTL or CMOS compatible).* 48 lines grouped into I/O ports of 8 bits, bit programmable under program control as general purpose I/O or as Alternate functions (see next section).

I/O Port Alternate Functions.

Each pin of the I/O ports of the ST90R30 may assume software programmable Alternative Functions as shown in the Pin Configuration Drawings. Figure 1.2 shows the Functions allocated to each I/O Port pins.

PIN DESCRIPTION (Continued)

Table 1. ST90R30 I/O Port Alternate Function Summary

I/O PORT Port.bit	Name	Function IN/OUT	Alternate Function	Pin Number
P0.0	A0/D0	I/O	Address/Data bit 0 mux	24
P0.1	A1/D1	I/O	Address/Data bit 1 mux	25
P0.2	A2/D2	I/O	Address/Data bit 2 mux	26
P0.3	A3/D3	I/O	Address/Data bit 3 mux	27
P0.4	A4/D4	I/O	Address/Data bit 4 mux	28
P0.5	A5/D5	I/O	Address/Data bit 5 mux	29
P0.6	A6/D6	I/O	Address/Data bit 6 mux	30
P0.7	A7/D7	I/O	Address/Data bit 7 mux	31
P1.0	A8	O	Address bit 8	23
P1.1	A9	O	Address bit 9	22
P1.2	A10	O	Address bit 10	21
P1.3	A11	O	Address bit 11	20
P1.4	A12	O	Address bit 12	19
P1.5	A13	O	Address bit 13	18
P1.6	A14	O	Address bit 14	17
P1.7	A15	O	Address bit 15	16
P2.0	NMI	I	Non-Maskable Interrupt	44
P2.1	P/$\overline{D}$	O	Program/Data Space Select	45
P2.1	SDI	I	SPI Serial Data Out	45
P2.2	INT2	I	External Interrupt 2	46
P2.2	SCK	O	SPI Serial Clock	46
P2.3	SDO	O	SPI Serial Data In	47
P2.4	INT1	I	External Interrupt 1	48
P2.4	$\overline{WRSTB5}$	O	Handshake Write Strobe P5	48
P2.5	WRRDY5	I	Handshake Write Ready P5	49
P2.6	INT3	I	External Interrupt 3	50
P2.6	$\overline{RDSTB5}$	I	Handshake Read Strobe P5	50
P2.6	P/$\overline{D}$	O	Program/Data Space Select	50
P2.7	RDRDY5	O	Handshake Read Ready P5	51

PIN DESCRIPTION (Continued)

Table 1. ST90R30 I/O Port Alternate Function Summary (Continued)

I/O PORT Port.bit	Name	Function IN/OUT	Alternate Function	Pin Number
P3.0	T0INA	I	MF Timer 0 Input A	15
P3.0	P/$\overline{D}$	O	Program/Data Space Select	15
P3.1	T0OUTA	O	MF Timer 0 Output A	14
P3.2	T0INB	I	MF Timer 0 Input B	13
P3.3	T0OUTB	O	MF Timer 0 Output B	12
P3.4	T1INA	I	MF Timer 1 Input A	11
P3.5	T1OUTA	O	MF Timer 1 Output A	10
P3.6	T1INB	I	MF Timer 1 Input B	9
P3.7	T1OUTB	O	MF Timer 1 Output B	8
P4.0	AIN0	I	A/D Analog Input 0	52
P4.1	AIN1	I	A/D Analog Input 1	53
P4.2	AIN2	I	A/D Analog Input 2	54
P4.3	AIN3	I	A/D Analog Input 3	55
P4.4	AIN4	I	A/D Analog Input 4	61
P4.5	AIN5	I	A/D Analog Input 5	56
P4.6	AIN6	I	A/D Analog Input 6	57
P4.7	AIN7	I	A/D Analog Input 7	58
P5.0		I/O	I/O Handshake Port 5	3
P5.1		I/O	I/O Handshake Port 5	2
P5.2		I/O	I/O Handshake Port 5	1
P5.3		I/O	I/O Handshake Port 5	68
P5.4		I/O	I/O Handshake Port 5	65
P5.5		I/O	I/O Handshake Port 5	64
P5.6		I/O	I/O Handshake Port 5	63
P5.7		I/O	I/O Handshake Port 5	62
P7.0	SIN	I	SCI Serial Input	43
P7.1	SOUT	O	SCI Serial Output	42
P7.2	INT4	I	External Interrupt 4	41
P7.2	TXCLK	I	SCI Transmit Clock Input	41

PIN DESCRIPTION (Continued)

Table 1. ST90R30 I/O Port Alternate Function Summary (Continued)

I/O PORT Port.bit	Name	Function IN/OUT	Alternate Function	Pin Number
P7.2	CLKOUT	O	SCI Byte Sync Clock Output	41
P7.3	INT5	I	External Interrupt 5	40
P7.3	RXCLK	I	SCI Receive Clock Input	40
P7.3	ADTRG	I	A/D Conversion Trigger	40
P7.4	INT6	I	External Interrupt 6	39
P7.4	P/$\overline{D}$	O	Program/Data Space Select	39
P7.5	$\overline{WAIT}$	I	External Wait Input	38
P7.6	WDOUT	O	T/WD Output	37
P7.6	$\overline{BUSREQ}$	I	External Bus Request	37
P7.7	WDIN	I	T/WD Input	36
P7.7	$\overline{BUSACK}$	O	External Bus Acknowledge	36

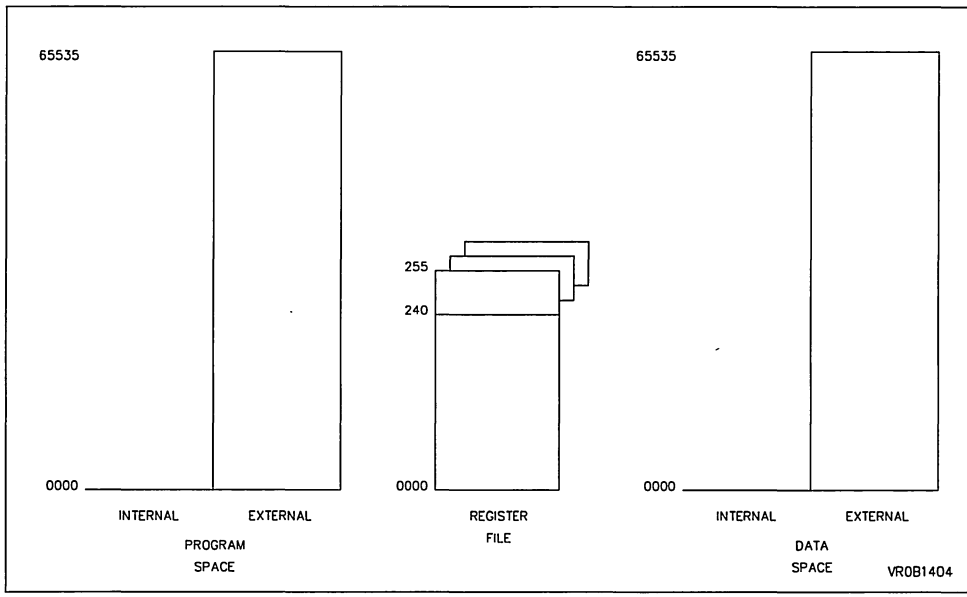
MEMORY

The memory of the ST90R30 is functionally divided into two areas, the Register File and Memory. The Memory may optionally be divided into two spaces, each having a maximum of 65,536 bytes. The two memory spaces are separated by function, one space for Program code, the other for Data. The ST90R30 addresses all program memory in the external PROGRAM space.

The Memory spaces are addressed using the multiplexed address and data buses on Ports 0 and 1. Data Memory may be decoded externally by using the P/$\overline{D}$ Alternate Function output. The on-chip general purpose (GP) Registers may be used as RAM memory.

MEMORY (Continued)

Figure 3. Memory Spaces



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	– 0.3 to 7.0	V
AV_{DD}, AV_{SS}	Analog Supply Voltage	$V_{SS} \le AV_{SS} < AV_{DD} \le V_{DD}$	V
V_I	Input Voltage	V_{SS} – 0.3 to V_{DD} +0.3	V
V_O	Output Voltage	V_{SS} – 0.3 to V_{DD} +0.3	V
T_{STG}	Storage Temperature	– 55 to + 150	°C

Note: Stresses above those listed as "absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value		Unit
		Min.	Max.	
T_A	Operating Temperature	– 40	85	°C
V_{DD}	Operating Supply Voltage	4.5	5.5	V
f_{OSCE}	External Oscillator Frequency		24	MHz
f_{OSCI}	Internal Oscillator Frequency		12	MHz

DC ELECTRICAL CHARACTERISTICS

(V_{DD} = 5V ± 10% T_A = – 40 °C to + 85°C, unless otherwise specified)

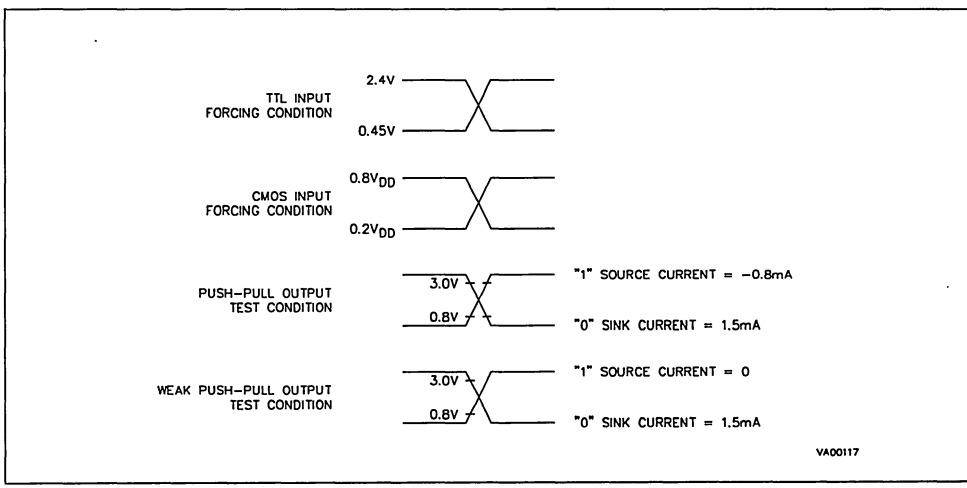
Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
V_{IHCK}	Clock Input High Level	External Clock	0.7 V_{DD}		V_{DD} + 0.3	V
V_{ILCK}	Clock Input Low Level	External Clock	– 0.3		0.3 V_{DD}	V
V_{IH}	Input High Level	TTL	2.0		V_{DD} + 0.3	V
		CMOS	0.7 V_{DD}		VDD + 0.3	V
V_{IL}	Input Low Level	TTL	– 0.3		0.8	V
		CMOS	– 0.3		0.3 V_{DD}	V
V_{IHRS}	Reset Input High Level		0.7 V_{DD}		V_{DD} + 0.3	V
V_{ILRS}	Reset Input Low Level		–0.3		0.3 V_{DD}	V
V_{HYRS}	Reset Input Hysteresis		0.3		1.5	V
V_{OH}	Output High Level	Push Pull, Iload = – 0.8mA	V_{DD} – 0.8			V
V_{OL}	Output Low Level	Push Pull or Open Drain, Iload = – 1.6mA			0.4	V

DC ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
I_{WPU}	Weak Pull-up Current	Bidirectional Weak Pull-up, V_{OL} = 0V	– 80	– 200	– 420	µA
I_{APU}	Active Pull-up Current, for INT0 and INT7 only	V_{IN} < 0.8V	– 80	– 200	– 420	µA
I_{LKIO}	I/O Pin Input Leakage	Input/Tri-State, 0V < V_{IN} < V_{DD}	– 10		+ 10	µA
I_{LKRS}	Reset Pin Input Leakage	0V < V_{IN} < V_{DD}	– 30		+ 30	µA
I_{LKAD}	A/D Pin Input Leakage	Alternate Function, Open Drain, 0V < V_{IN} < V_{DD}	– 3		+ 3	µA
I_{LKAP}	Active Pull-up Input Leakage	0V < V_{IN} < 0.8V	– 10		+ 10	µA
I_{LKOS}	OSCIN Pin Input Leakage	0V < V_{IN} < V_{DD}	– 10		+ 10	µA
I_{DD}	Run Mode Current	24MHz, Note 1		32	70	mA
		4MHz, Note 1		6	12	mA
I_{DP2}	Run Mode Current Prescale by 2	24MHz, Note 1		19	40	mA
		4MHz, Note 1		4	8	mA
I_{WFI}	WFI Mode Current	24MHz, Note 1		9	18	mA
		4MHz, Note 1		2.5	5	mA
I_{HALT}	HALT Mode Current	24MHz, Note 1			100	µA

Note:
1. All I/O Ports are configured in Bidirectional Weak Pull-up Mode with no DC load, External Clock pin (OSCIN) is driven by square wave external clock. No peripheral working. External interface not active (Internal Program Execution).

DC TEST CONDITIONS



AC ELECTRICAL CHARACTERISTICS

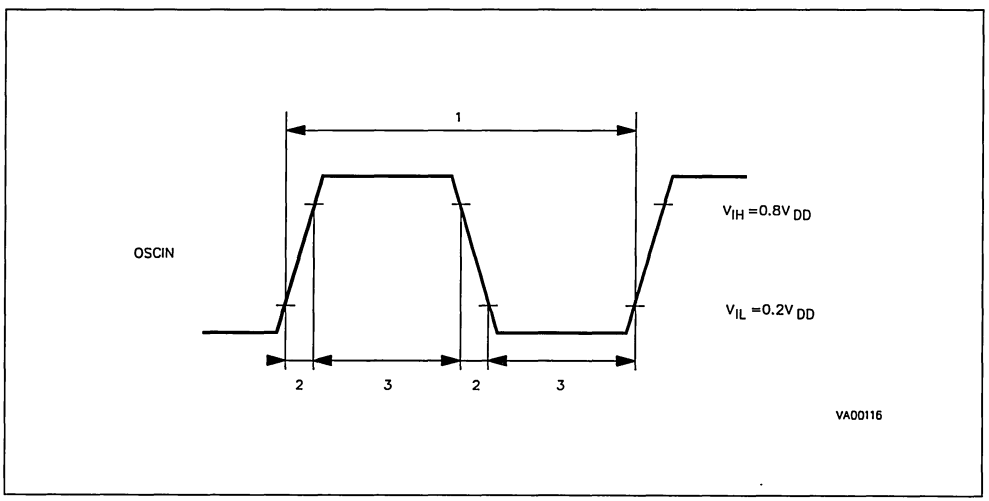
CLOCK TIMING TABLE

(V_{DD} = 5V ± 10%, T_A = − 40°C to + 85°C, unless otherwise specified)

N°	Symbol	Parameter	Value		Unit	Note
			Min.	Max.		
1	TpC	OSCIN Clock Period	41.5		ns	1
			83		ns	2
2	TrC, TfC	OSCIN Rise and Fall Time		12	ns	
3	TwCL, TwCH	OSCIN Low and High Width	25	12	ns	1
			38		ns	2

Notes:
1. Clock divided by 2 internally (MODER.DIV2=1)
2. Clock not divided by 2 internally (MODER.DIV2=0)

CLOCK TIMING



EXTERNAL BUS TIMING TABLE

(V_{DD} = 5V ± 10%, T_A = – 40 °C to + 85 °C, Cload = 50pF, CPUCLK = 12MHz, unless otherwise specified)

N°	Symbol	Parameter	Value (Note)				Unit
			OSCIN Divided By 2	OSCIN Not Divided By 2	Min.	Max.	
1	TsA (AS)	Address Set-up Time before $\overline{AS}$ ↑	TpC (2P+1) –22	TWCH+PTpC –18	20		ns
2	ThAS (A)	Address Hold Time after $\overline{AS}$↑	TpC –17	TwCL –13	25		ns
3	TdAS (DR)	$\overline{AS}$ ↑ to Data Available (read)	TpC (4P+2W+4) –52	TpC (2P+W+2) –51		115	ns
4	TwAS	$\overline{AS}$ Low Pulse Width	TpC (2P+1) –7	TwCH+PTpC –3	35		ns
5	TdAz (DS)	Address Float to $\overline{DS}$ ↓	0	0	0		ns
6	TwDSR	$\overline{DS}$ Low Pulse Width (read)	TpC (4P+2W+3) –20	TwCH+TpC (2P+W+1) –16	105		ns
7	TwDSW	$\overline{DS}$ Low Pulse Width (write)	TpC (2P+2W+2) –13	TpC (P+W+1) –13	70		ns
8	TdDSR (DR)	$\overline{DS}$ ↓ to Data Valid Delay (read)	TpC (4P+2W-3) –50	TwCH+TpC(2P+W+1) – 46		75	ns
9	ThDR (DS)	Data to $\overline{DS}$ ↑ Hold Time (read)	0	0	0		ns
10	TdDS (A)	$\overline{DS}$ ↑ to Address Active Delay	TpC –7	TwCL –3	35		ns
11	TdDS (AS)	$\overline{DS}$ ↑ to $\overline{AS}$ ↓ Delay	TpC –18	TwCL –14	24		ns
12	TsR/W (AS)	R/$\overline{W}$ Set-up Time before $\overline{AS}$↑	TpC (2P+1) –22	TwCH+PTpC –18	20		ns
13	TdDSR (R/W)	$\overline{DS}$ ↑ to R/$\overline{W}$ and Address Not Valid Delay	TpC –9	TwCL –5	33		ns
14	TdDW (DSW)	Write Data Valid to $\overline{DS}$ ↓ Delay (write)	TpC (2P+1) –32	TwCH+PTpC –28	10		ns
15	ThDS (DW)	Data Hold Time after DS ↑ (write)	TpC –9	TwCL –5	33		ns
16	TdA (DR)	Address Valid to Data Valid Delay (read)	TpC (6P+2W+5) –68	TwCH+TpC (3P+W+2) –64		140	ns
17	TdAs (DS)	$\overline{AS}$ ↑ to $\overline{DS}$ ↓ Delay	TpC –18	TwCL –14	24		ns

Note: The value left hand two columns show the formula used to calculate the timing minimum or maximum from the oscillator clock period, prescale value and number of wait cycles inserted.
The value right hand two columns show the timing minimum and maximum for an external clock at 24 MHz divided by 2, prescaler value of zero and zero wait status.

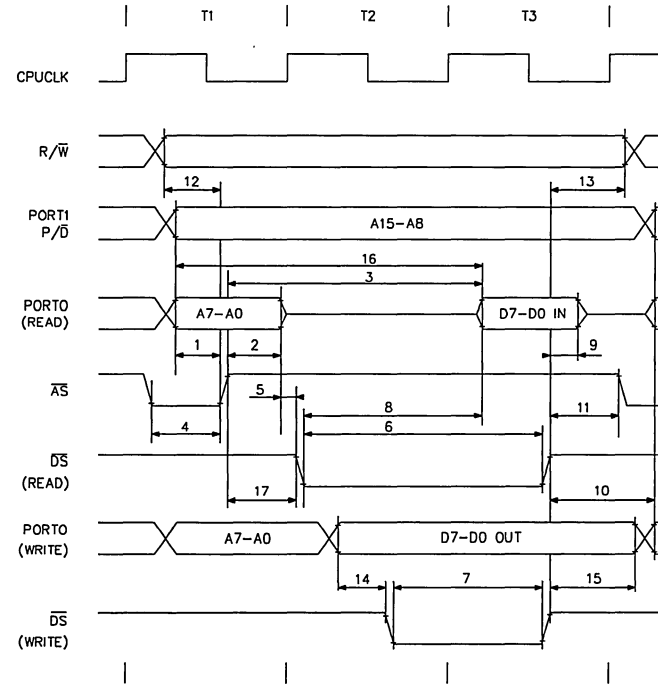
Legend:
P = Clock Prescaling Value
W = Wait Cycles
TpC = OSCIN Period
TwCH = High Level OSCIN half period
TwCL = Low Level OSCIN half period

EXTERNAL WAIT TIMING TABLE (V_{DD} = 5V ± 10%, T_A = –40°C to +85°C, Cload = 50pF, INTCLK = 12MHz, Push-pull output configuration, unless otherwise specified)

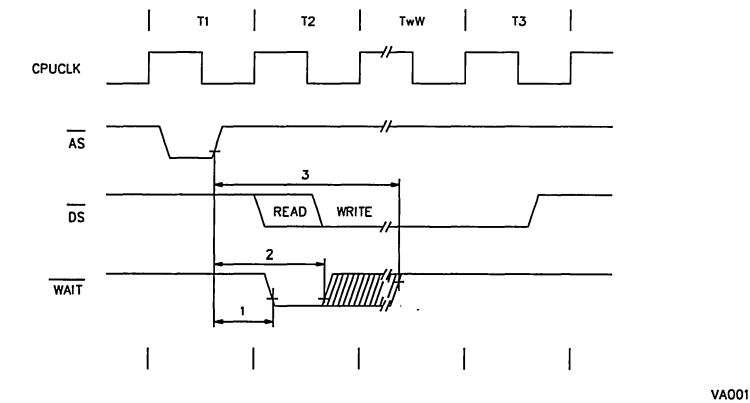
N°	Symbol	Parameter	Value (Note)				Unit
			OSCIN Divided By 2	OSCIN Not Divided By 2	Min.	Max.	
1	TdAS (WAIT)	$\overline{AS}$ ↑ to $\overline{WAIT}$ ↓ Delay	2(P+1)TpC –29	(P+1)TpC –29		40	ns
2	TdAS (WAIT)	$\overline{AS}$ ↑ to $\overline{WAIT}$ ↑ Minimum Delay	2(P+W+1)TpC –4	(P+W+1)TpC –4	80		ns
3	TdAS (WAIT)	$\overline{AS}$ ↑ to $\overline{WAIT}$ ↑ Maximum Delay	2(P+W+1)TpC – 29	(P+W+1)TpC –29		83W+40	ns

Note: The value left hand two columns show the formula used to calculate the timing minimum or maximum from the oscillator clock period, prescale value and number of wait cycles inserted.
The value right hand two columns show the timing minimum and maximum for an external clock at 24 MHz divided by 2, prescale value of zero and zero wait status.

EXTERNAL BUS TIMING



EXTERNAL WAIT TIMING

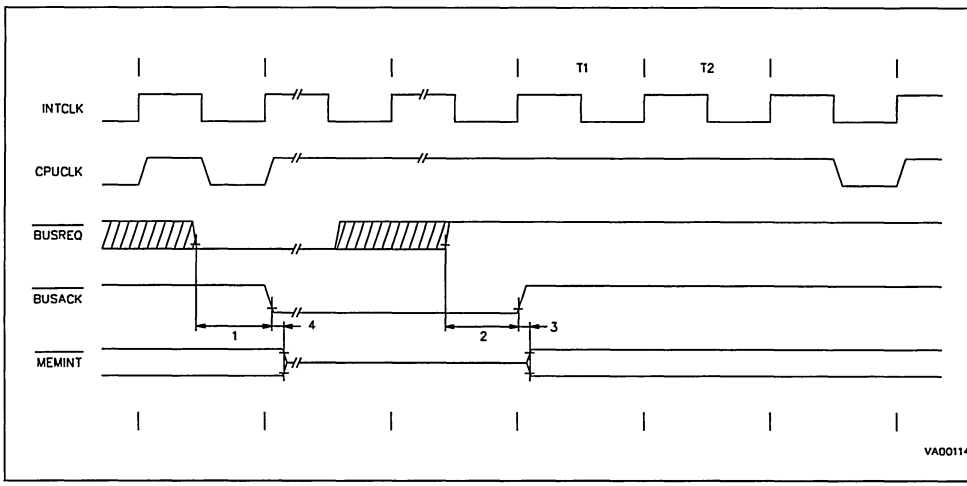


BUS REQUEST/ACKNOWLEDGE TIMING TABLE (V_{DD} = 5V ± 10%, T_A = −40°C to +85°C, Cload = 50pF, INTCLK = 12MHz, Push-pull output configuration, unless otherwise specified)

N°	Symbol	Parameter	Value (Note)				Unit
			OSCIN Divided By 2	OSCIN Not Divided By 2	Min.	Max.	
1	TdBR (BACK)	$\overline{BREQ}$ ↓ to $\overline{BUSACK}$ ↓	TpC+8	TwCL+12	50		ns
			TpC(6P+2W+7)+65	TpC(3P+W+3)+TwCL+65		360	ns
2	TdBR (BACK)	$\overline{BREQ}$ ↑ to $\overline{BUSACK}$ ↑	3TpC+60	TpC+TwCL+60		185	ns
3	TdBACK (BREL)	$\overline{BUSACK}$ ↓ to Bus Release	20	20		20	ns
4	TdBACK (BACT)	$\overline{BUSACK}$ ↑ to Bus Active	20	20		20	ns

Note: The value left hand two columns show the formula used to calculate the timing minimum or maximum from the oscillator clock period, prescale value and number of wait cycles inserted.
The value right hand two columns show the timing minimum and maximum for an external clock at 24 MHz divided by 2, prescale value of zero and zero wait status.

BUS REQUEST/ACKNOWLEDGE TIMING



Note : MEMINT = group of memory interface signals : $\overline{AS}$, $\overline{DS}$, R/$\overline{W}$, P00-P07, P10-P17.

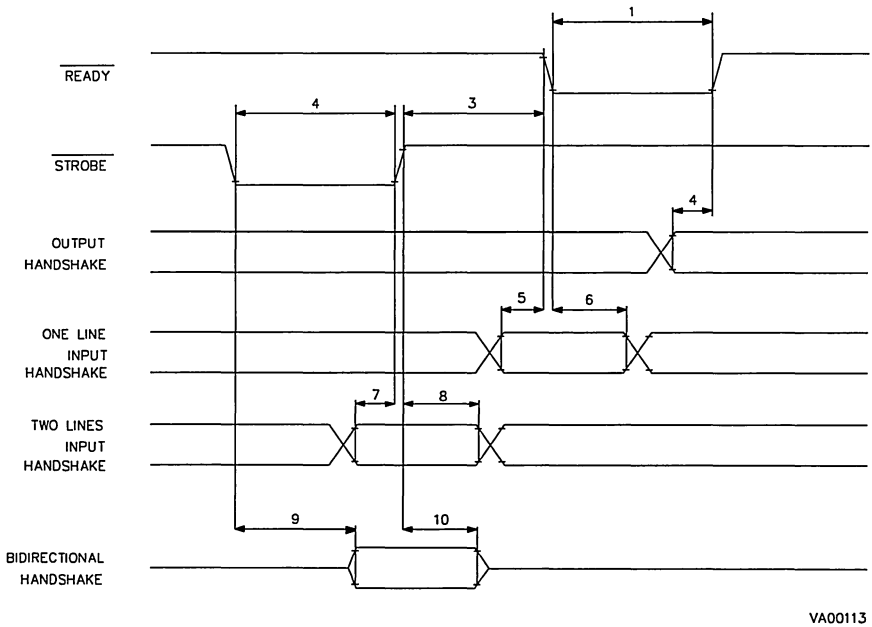
HANDSHAKE TIMING TABLE (V_{DD} = 5V ± 10%, T_A = –40°C to +85°C, Cload = 50pF, INTCLK = 12MHz, Push-pull output configuration, unless otherwise specified)

N°	Symbol	Parameter	Value (Note)				Min.	Max.	Unit
			OSCIN Divided By 2		OSCIN Not Divided By 2				
			Min.	Max.	Min.	Max.			
1	TwRDY	RDRDY, WRRDY Pulse Width in One Line Handshake	2TpC (P+W+1) –18		Tp (P+W+1) – 18		65		ns
2	TwSTB	$\overline{RDSTB}$, $\overline{WRSTB}$ Pulse Width	2TpC+12		TpC+12		95		ns
3	TdST (RDY)	$\overline{RDSTB}$, or $\overline{WRSTB}$ ↑ to RDRDY or WRRDY ↓		TpC+45		(TpC-TwCL) +45		87	ns
4	TsPD (RDY)	Port Data to RDRDY ↑ Set-up Time	(2P+2W+1) TpC –25		TwCH+(W+P) TpC –25		16		ns
5	TsPD (RDY)	Port Data to WRRDY ↓ Set-up Time in One Line Handshake	43		43		43		ns
6	ThPD (RDY)	Port Data to WRRDY ↓ Hold Time in One Line Handshake	0		0		0		ns
7	TsPD (STB)	Port Data to $\overline{WRSTB}$ ↑ Set-up Time	10		10		10		ns
8	ThPD (STB)	Port Data to WRSTB ↑ Hold Time	25		25		25		ns
9	TdSTB (PD)	$\overline{RDSTBD}$ ↑ to Port Data Delay Time in Bidirectional Handshake		35		35		35	ns
10	TdSTB (PHZ)	$\overline{RDSTB}$ ↑ to Port High-Z Delay Time in Bidirectional Handshake		25		25		25	ns

Note: The value left hand two columns show the formula used to calculate the timing minimum or maximum from the oscillator clock period, prescale value and number of wait cycles inserted.
The value right hand two columns show the timing minimum and maximum for an external clock at 24 MHz divided by 2, prescaler value of zero and zero wait status.

Legend:
P = Clock Prescaling Value (R235.4,3,2)
W = Programmable Wait Cycles (R252.2.1.0/5,4,3) + External Wait Cycles

HANDSHAKE TIMING

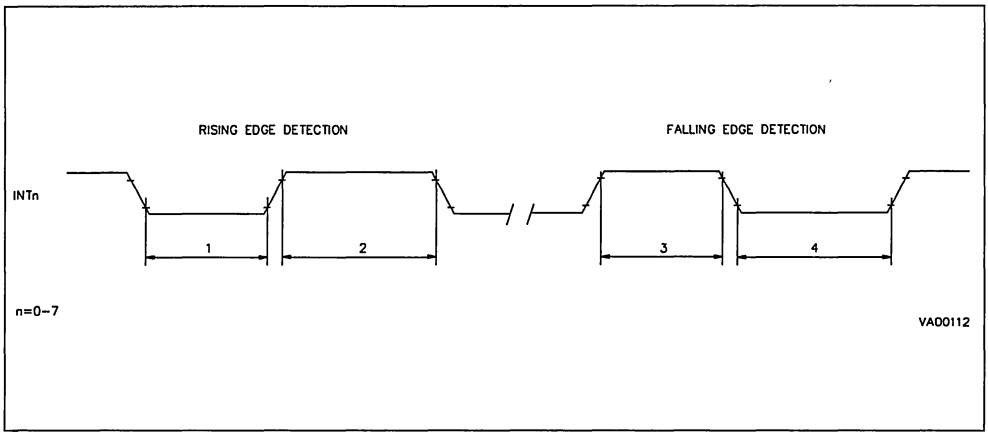


EXTERNAL INTERRUPT TIMING TABLE (V_{DD} = 5V ± 10%, T_A = –40°C to +85°C, Cload = 50pF, INTCLK = 12MHz, Push-pull output configuration, unless otherwise specified)

N°	Symbol	Parameter	Value (Note)				Unit
			OSCIN Divided By 2 Min.	OSCIN Not Divided By 2 Min.	Min.	Max.	
1	TwLR	Low Level Minimum Pulse Width in Rising Edge Mode	2TpC+12	TpC+12	95		ns
2	TwHR	High Level Minimum Pulse Width in Rising Edge Mode	2TpC+12	TpC+12	95		ns
3	TwHF	High Level Minimum Pulse Width in Falling Edge Mode	2TpC+12	TpC+12	95		ns
4	TwLF	Low Level Minimum Pulse Width in Falling Edge Mode	2TpC+12	TpC+12	95		ns

Note: The value left hand two columns show the formula used to calculate the timing minimum or maximum from the oscillator clock period, prescale value and number of wait cycles inserted.
The value right hand two columns show the timing minimum and maximum for an external clock at 24 MHz divided by 2, prescale value of zero and zero wait status.

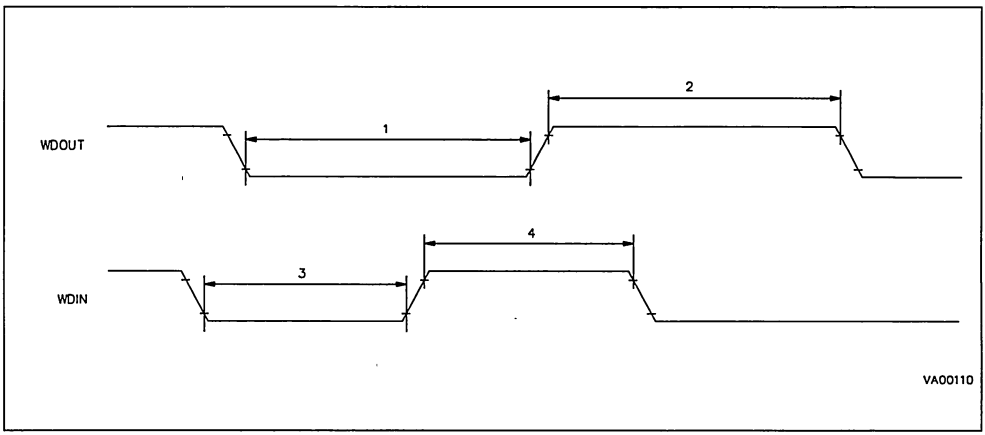
EXTERNAL INTERRUPT TIMING



WATCHDOG TIMING TABLE (V_{DD} = 5V ± 10%, T_A = –40°C to +85°C, Cload = 50pF, INTCLK =12MHz, Output Alternate Function set as Push-pull)

N°	Symbol	Parameter	Value		Unit
			Min.	Max.	
1	TwWDOL	WDOUT Low Pulse Width	620		ns
2	TwWDOH	WDOUT High Pulse Width	620		ns
3	TwWDIL	WDIN Low Pulse Width	350		ns
4	TwWDIH	WDIN High Pulse Width	350		ns

WATCHDOG TIMING

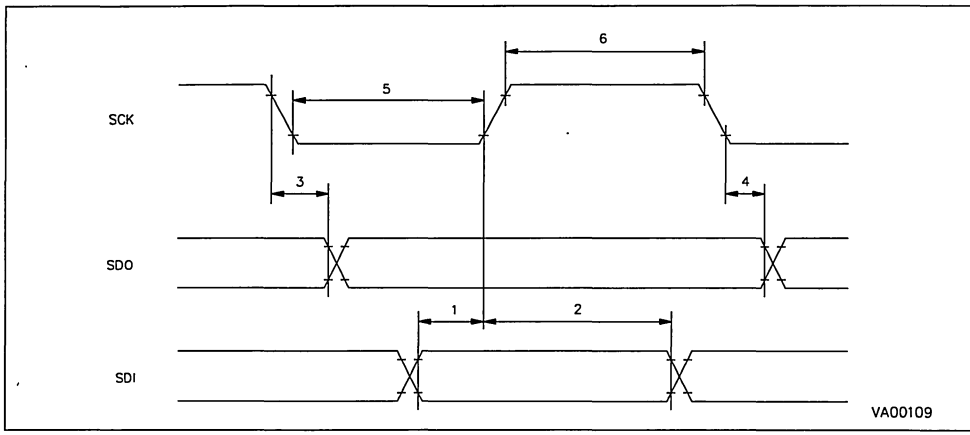


SPI TIMING TABLE (V_{DD} = 5V ± 10%, T_A = –40°C to +85°C, Cload = 50pF, INTCLK = 12MHz, Output Alternate Function set as Push-pull)

N°	Symbol	Parameter	Value		Unit
			Min.	Max.	
1	TsDI	Input Data Set-up Time	100		ns
2	ThDI (1)	Input Data Hold Time	1/2 TpC+100		ns
3	TdOV	SCK to Output Data Valid		100	ns
4	ThDO	Output Data Hold Time	-20		ns
5	TwSKL	SCK Low Pulse Width	300		ns
6	TwSKH	SCK High Pulse Width	300		ns

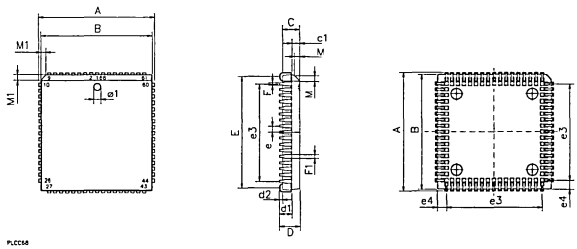
Note: 1. TpC is the Clock period.

SPI TIMING



PACKAGE MECHANICAL DATA

Figure 57. 68-Lead Plastic Leaded Chip Carrier



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A	25.02		25.27	0.985		0.995
B	24.13		24.33	0.950		0.958
D	4.20		5.08	0.165		0.200
d1		2.54			0.100	
d2		0.56			0.022	
E	22.61		23.62	0.890		0.930
e		1.27			0.050	
F		0.38			0.015	
G			0.10			0.004
M		1.27			0.050	
M1		1.14			0.044	
Ø1		7.36			0.289	

ORDERING INFORMATION

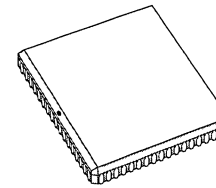
Sales Type	Frequency	Temperature Range	Package
ST90R30C6	24MHz	-40°C to +85°C	PLCC68
ST90R30C1	24 MHz	0°C to +70°C	PLCC68

SGS-THOMSON MICROELECTRONICS

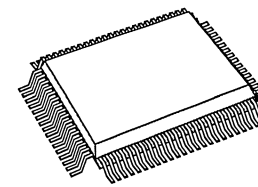
ST9036

16K ROM HCMOS MCU WITH EEPROM

- Single chip microcontroller with 16K bytes of ROM, 256 bytes of RAM and 256 bytes of register file with 224 general purpose registers available as RAM, accumulators or index pointers.
- On-chip programmable security protection against external reading of internal memory.
- 8/16 bit CORE with full feature DMA controller, a powerful interrupt handler and a Standard Serial Peripheral Interface (SPI) handling S-bus, I^2C-bus, IM-bus and Standard Serial Peripheral Interfaces.
- Up to 8 external interrupts edge-selectable plus 1 non-maskable interrupt.
- 16 bit programmable Timer with 8 bit Prescaler, able to be used as a Watchdog Timer for system integrity.
- Two 16 bit Multifunction Timer modules, each with an 8 bit prescaler and 13 operating modes, allowing simple use for complex waveform generation and measurement, PWM functions and many other system timing operations.
- 8 channel Analog to Digital Converter, with integral sample and hold, fast 11µs conversion time, 8 bit ±1/2 LSB resolution with Analog Watchdog on two channels.
- Full function Serial Communications Interface with 110 to 375,000 baud rate generator, asynchronous and byte synchronous capability (fully programmable format) and address/wake-up bit option.
- On-chip DMA channels associated to the Multifunction Timers and the Serial Communications Interface.
- Up to seven 8 bit I/O ports with programmable input thresholds and output characteristics. Alternative functions allow the full use of all pins.
- Powerful software development tools, including assembler, linker, C-compiler, archiver, software and hardware emulators.
- Windowed and One Time Programmable EPROM parts available for prototyping and preproduction development phases.
- 68-lead Plastic Leaded Chip Carrier package for ST9036C6.
- 80-pin Plastic Quad Flat Pack package for ST9036Q6



PLCC68



PQFP80

(Ordering Information at the end of the datasheet)

Figure 1. ST9036 Pin Configuration

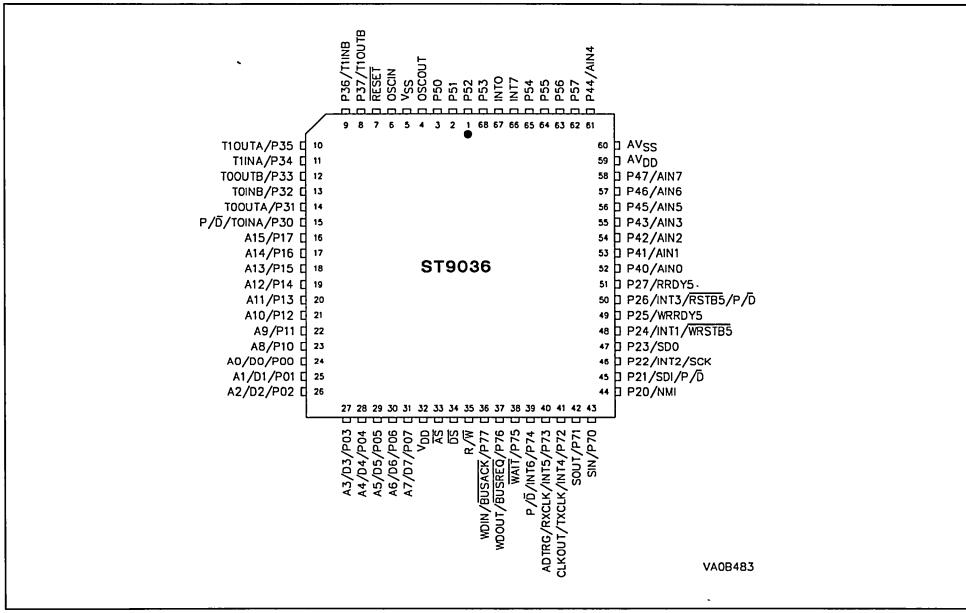


Figure 2. ST9036 Pin Configuration

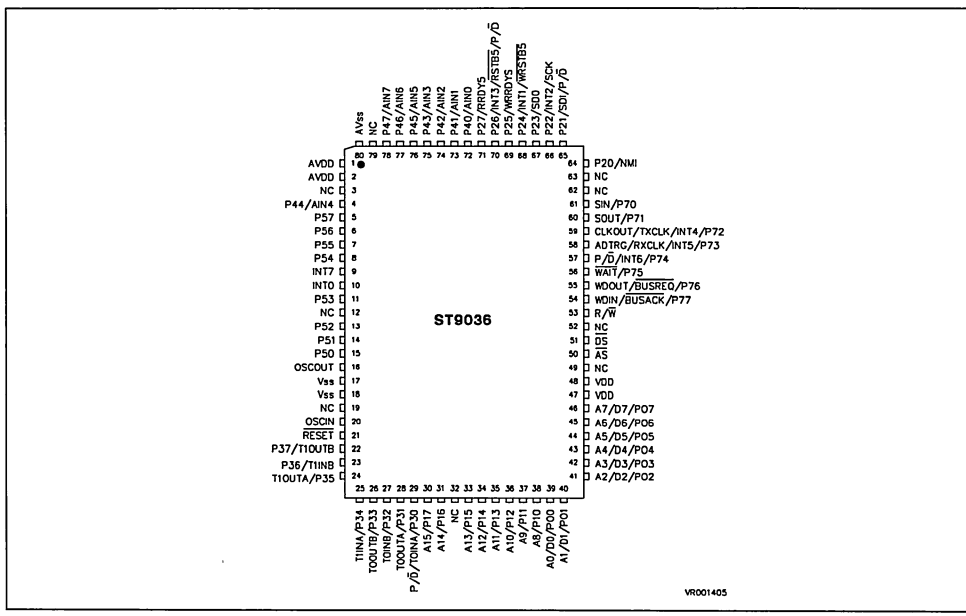
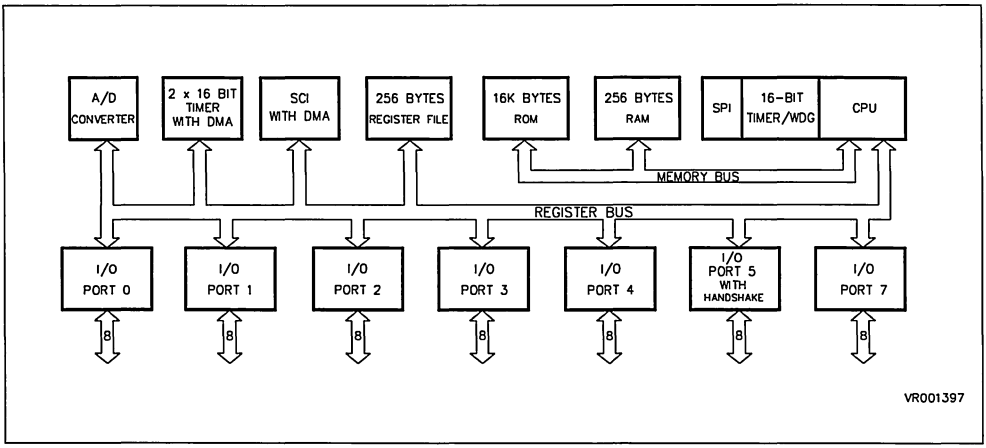


Figure 3. ST9036 Block Diagram



GENERAL DESCRIPTION

The ST9036 is a ROM member of the ST9 family of microcontrollers, completely developed and produced by SGS-THOMSON Microelectronics using a proprietary n-well HCMOS process.

The ROM device is fully compatible with the EPROM version (ST90E40), which may be used for the prototyping and pre-production phases of development, and can be configured as: a standalone microcontroller with 16K bytes of on-chip ROM, a microcontroller able to manage up to 112K bytes of external memory, or as a parallel processing element in a system with other processors and peripheral controllers.

A key point of the ST9036 architecture is its modular approach which allows software commonality with all other members of the ST9 family.

The nucleus of the modular design of the ST9036 is the advanced Core which includes the Central Processing Unit (CPU), the Register File, a 16 bit Timer/Watchdog with 8 bit Prescaler, a Serial Peripheral Interface supporting S-bus, I^2C-bus and IM-bus Interface, plus two 8 bit I/O ports. The Core has independent memory and register buses allowing a high degree of pipelining to add to the efficiency of the code execution speed of the extensive instruction set.

The powerful I/O capabilities demanded by microcontroller applications are fulfilled by the ST9036 with up to 56 I/O lines dedicated to digital Input/Output. These lines are grouped into up to seven 8 bit I/O Ports and can be configured on a bit basis under software control to provide timing, status signals, an address/data bus for interfacing external memory, timer inputs and outputs, analog inputs, external interrupts and serial or parallel I/O with or without handshake.

Three basic memory spaces are available to support this wide range of configurations: Program Memory (internal and external), Data Memory (internal and external) and the Register File, which includes the control and status registers of the on-chip peripherals.

Two 16 bit MultiFunction Timers, each with an 8 bit Prescaler and 13 operating modes allow simple use for complex waveform generation and measurement, PWM functions and many other system timing functions by the usage of the two associated DMA channels for each timer.

In addition there is an 8 channel Analog to Digital Converter with integral sample and hold, fast 11µs conversion time and 8 bit ±1/2 LSB resolution. An Analog Watchdog feature is included for two input channels.

Completing the device is a full duplex Serial Communications Interface with an integral 110 to 375,000 baud rate generator, asynchronous and byte synchronous capability (fully programmable format) and associated address/wake-up option, plus two DMA channels.

PIN DESCRIPTION

$\overline{AS}$. Address Strobe (output, active low, 3-state). Address Strobe is pulsed low once at the beginning of each memory cycle. The rising edge of $\overline{AS}$ indicates that address, Read/Write (R/$\overline{W}$), and Data Memory signals are valid for program or data memory transfers. Under program control, $\overline{AS}$ can be placed in a high-impedance state along with Port 0 and Port 1, Data Strobe ($\overline{DS}$) and R/$\overline{W}$.

$\overline{DS}$. Data Strobe (output, active low, 3-state). Data Strobe provides the timing for data movement to or from Port 0 for each memory transfer. During a write cycle, data out is valid at the leading edge of $\overline{DS}$. During a read cycle, Data In must be valid prior to the trailing edge of $\overline{DS}$. When the ST9036 accesses on-chip memory, $\overline{DS}$ is held high during the whole memory cycle. It can be placed in a high impedance state along with Port 0, Port 1, $\overline{AS}$ and R/$\overline{W}$.

R/$\overline{W}$. Read/Write (output, 3-state). Read/Write determines the direction of data transfer for external memory transactions. R/$\overline{W}$ is low when writing to external program or data memory, and high for all other transactions. It can be placed in a high impedance state along with Port 0, Port 1, $\overline{AS}$ and $\overline{DS}$.

$\overline{RESET}$. Reset (input, active low). The ST9 is initialised by the Reset signal. With the deactivation of $\overline{RESET}$, program execution begins from the Program memory location pointed to by the vector contained in program memory locations 00h and 01h.

OSCIN, OSCOUT. Oscillator (input and output). These pins connect a parallel-resonant crystal (24MHz maximum), or an external source to the on-chip clock oscillator and buffer. OSCIN is the input of the oscillator inverter and internal clock generator; OSCOUT is the output of the oscillator inverter.

AV_{DD}. Analog V_{DD} of the Analog to Digital Converter.

AV_{SS}. Analog V_{SS} of the Analog to Digital Converter.

V_{DD}. Main Power Supply Voltage (5V±10%)

V_{SS}. Digital Circuit Ground.

P0.0-P0.7, P1.0-P1.7, P2.0-P2.7 P3.0-P3.7, P4.0-P4.7, P5.0-P5.7, P7.0-P7.7 I/O Port Lines (Input/Output, TTL or CMOS compatible). 8 lines grouped into I/O ports of 8 bits, bit programmable under program control as general purpose I/O or as Alternate functions (see next section).

I/O Port Alternate Functions.

Each pin of the I/O ports of the ST9030 and ST9031 may assume software programmable Alternative Functions as shown in the Pin Configuration Drawings. Due to Bonding options for the packages, some functions may not be present, figure 1.2 shows the Functions allocated to each I/O Port pins and a summary of packages for which they are available.

PIN DESCRIPTION (Continued)

Table 1. ST9040 I/O Port Alternate Function Summary

I/O PORT Port. bit	Name	Function	Alternate Function	Pin Assignment
P0.0	A0/D0	I/O	Address/Data bit 0 mux	24
P0.1	A1/D1	I/O	Address/Data bit 1 mux	25
P0.2	A2/D2	I/O	Address/Data bit 2 mux	26
P0.3	A3/D3	I/O	Address/Data bit 3 mux	27
P0.4	A4/D4	I/O	Address/Data bit 4 mux	28
P0.5	A5/D5	I/O	Address/Data bit 5 mux	29
P0.6	A6/D6	I/O	Address/Data bit 6 mux	30
P0.7	A7/D7	I/O	Address/Data bit 7 mux	31
P1.0	A8	O	Address bit 8	23
P1.1	A9	O	Address bit 9	22
P1.2	A10	O	Address bit 10	21
P1.3	A11	O	Address bit 11	20
P1.4	A12	O	Address bit 12	19
P1.5	A13	O	Address bit 13	18
P1.6	A14	O	Address bit 14	17
P1.7	A15	O	Address bit 15	16
P2.0	NMI	I	Non-Maskable Interrupt	44
P2.0	ROMless	I	ROMless Select (Mask option)	44
P2.1	P/$\overline{D}$	O	Program/Data Space Select	45
P2.1	SDI	I	SPI Serial Data Out	45
P2.2	INT2	I	External Interrupt 2	46
P2.2	SCK	O	SPI Serial Clock	46
P2.3	SDO	O	SPI Serial Data In	47
P2.4	INT1	I	External Interrupt 1	48
P2.4	$\overline{WRSTB5}$	O	Handshake Write Strobe P5	48
P2.5	WRRDY5	I	Handshake Write Ready P5	49
P2.6	INT3	I	External Interrupt 3	50
P2.6	$\overline{RDSTB5}$	I	Handshake Read Strobe P5	50
P2.6	P/$\overline{D}$	O	Program/Data Space Select	50
P2.7	RDRDY5	O	Handshake Read Ready P5	51
P3.0	T0INA	I	MF Timer 0 Input A	15
P3.0	P/$\overline{D}$	O	Program/Data Space Select	15
P3.1	T0OUTA	O	MF Timer 0 Output A	14
P3.2	T0INB	I	MF Timer 0 Input B	13
P3.3	T0OUTB	O	MF Timer 0 Output B	12
P3.4	T1INA	I	MF Timer 1 Input A	11

PIN DESCRIPTION (Continued)

Table 1. ST9040 I/O Port Alternate Function Summary (Continued)

I/O PORT Port. bit	Name	Function	Alternate Function	Pin Assignment
P3.5	T1OUTA	O	MF Timer 1 Output A	10
P3.6	T1INB	I	MF Timer 1 Input B	9
P3.7	T1OUTB	O	MF Timer 1 Output B	8
P4.0	AIN0	I	A/D Analog Input 0	52
P4.1	AIN1	I	A/D Analog Input 1	53
P4.2	AIN2	I	A/D Analog Input 2	54
P4.3	AIN3	I	A/D Analog Input 3	55
P4.4	AIN4	I	A/D Analog Input 4	61
P4.5	AIN5	I	A/D Analog Input 5	56
P4.6	AIN6	I	A/D Analog Input 6	57
P4.7	AIN7	I	A/D Analog Input 7	58
P5.0		I/O	I/O Handshake Port 5	3
P5.1		I/O	I/O Handshake Port 5	2
P5.2		I/O	I/O Handshake Port 5	1
P5.3		I/O	I/O Handshake Port 5	68
P5.4		I/O	I/O Handshake Port 5	65
P5.5		I/O	I/O Handshake Port 5	64
P5.6		I/O	I/O Handshake Port 5	63
P5.7		I/O	I/O Handshake Port 5	62
P7.0	SIN	I	SCI Serial Input	43
P7.1	SOUT	O	SCI Serial Output	42
P7.1	ROMless	I	ROMless Select (Mask option)	42
P7.2	INT4	I	External Interrupt 4	41
P7.2	TXCLK	I	SCI Transmit Clock Input	41
P7.2	CLKOUT	O	SCI Byte Sync Clock Output	41
P7.3	INT5	I	External Interrupt 5	40
P7.3	RXCLK	I	SCI Receive Clock Input	40
P7.3	ADTRG	I	A/D Conversion Trigger	40
P7.4	INT6	I	External Interrupt 6	39
P7.4	P/$\overline{D}$	O	Program/Data Space Select	39
P7.5	$\overline{WAIT}$	I	External Wait Input	38
P7.6	WDOUT	O	T/WD Output	37
P7.6	$\overline{BUSREQ}$	I	External Bus Request	37
P7.7	WDIN	I	T/WD Input	36
P7.7	$\overline{BUSACK}$	O	External Bus Acknowledge	36

ST9036 CORE

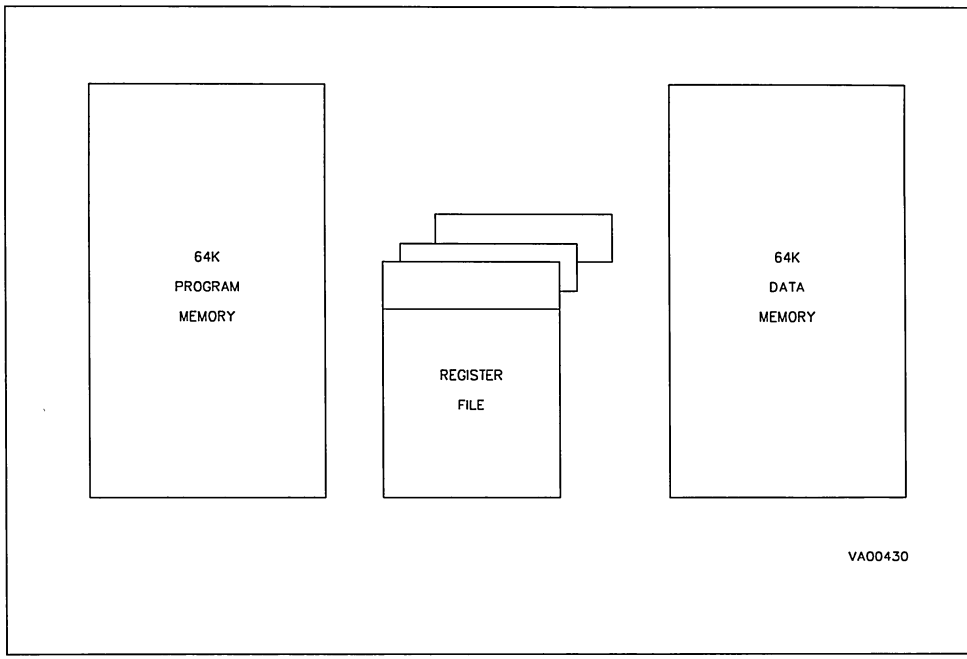
The Core or Central Processing Unit (CPU) of the ST9036 includes the 8 bit Arithmetic Logic Unit and the 16 bit Program Counter, System and User Stack Pointers. The microcoded Instruction Set is highly optimised for both byte (8 bit) and word (16 bit) data, BCD and Boolean data types, with 14 addressing modes. Two 8 bit I/O ports are connected to the Core module for external memory interfacing, while a 16 bit Timer/Watchdog gives system security and timing functions, and a Serial Peripheral Interface allows for synchronous communication. Three independent buses are controlled by the Core, a 16 bit Memory bus, an 8 bit Register addressing bus and a 6 bit Interrupt/DMA bus connected to the interrupt and DMA controllers in the on-chip peripherals and the Core. This multiple bus architecture allows a high degree of pipelining and parallel operation within the ST9036, giving it its efficiency in both numerical calculations and communication with the on-chip peripherals.

MEMORY

The memory of the ST9036 is functionally divided into two areas, the Register File and Memory. The Memory is divided into two spaces, each having a maximum of 65,536 bytes. The two memory spaces are separated by function, one space for Program code, the other for Data. The ST9036 16K bytes of on-chip ROM memory are selected at memory addresses 0 through 3FFFh (hexadecimal) in the PROGRAM space and the 256 bytes of on-chip RAM memory is selected at memory addresses 200h through 2FFh in the DATA space.

Off-chip memory, addressed using the multiplexed address and data buses (Ports 0 and 1) may be divided into the Program and Data spaces by the external decoding of the Program/Data select pin ($P/\overline{D}$) available as an Alternate function, allowing a full 128K byte memory. The memory spaces are selected by the execution of the SDM and SPM instructions (Set Data Memory and Set Program

Figure 4. Memory Spaces



MEMORY (Continued)

Memory, respectively). There is no need to use either of these instructions again until the memory area required is to be changed. This requirement is not necessary in two cases: first, when operating with external stacks (the Data memory is automatically selected) and, secondly, when using the memory indirect to memory indirect post-increment addressing mode (the memory types are specified in the instructions: LDPP, LDPD, LDDP, LDDD).

Either the Data Memory or the Program Memory can be addressed using any of the memory addressing modes.

Program Space

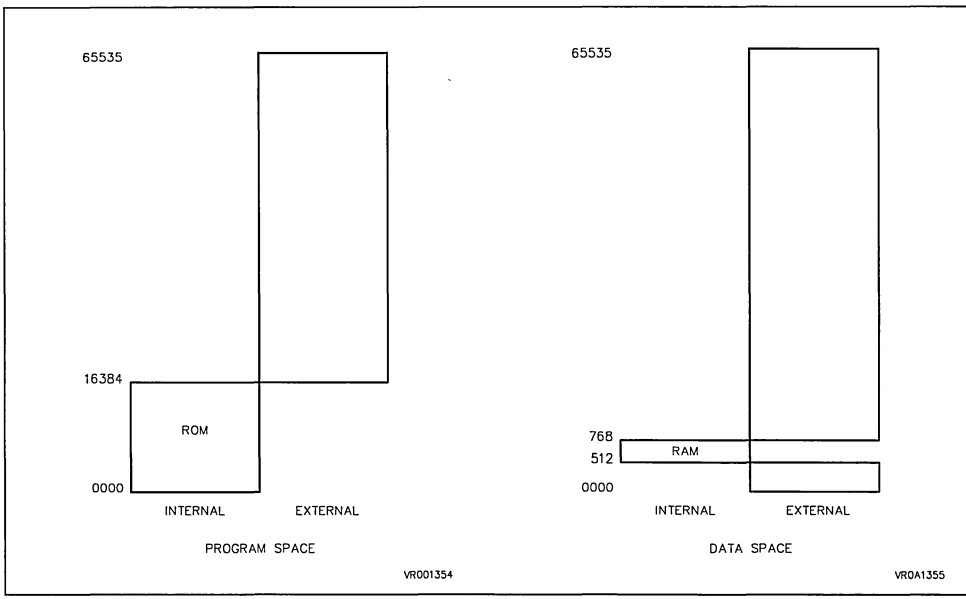
The Program memory space of the ST9036, from the 16K bytes of on-chip ROM memory to the full 64K bytes with off-chip memory expansion is fully available to the user. At addresses greater than the first 16K of program space, the ST9036 executes external memory cycles for instruction fetches. The first 256 memory locations from address 0 to 0FFh (hexadecimal) hold the Reset Vector, the Top-Level (Pseudo Non-Maskable) interrupt, the Divide by Zero Trap vector and, optionally, the interrupt vector table for use with the on-chip peripherals and the external interrupt sources. Each vector is contained in two consecutive byte locations, the high order address held in the lower (even) byte, the low order address held in the upper (odd) byte, forming the address which is loaded into the Program Counter when selected by the interrupt vector provided by the interrupt source. This should point to the relevant Interrupt Service routine provided by the user for immediate response to the interrupt.

Data Space

The ST9036 addresses the 256 bytes of on-chip RAM memory in the Data Space from addresses 512 to 768 (200h to 2FFh). It may also address up to 65,280 locations of External Data through the External Memory Interface when decoded with the P/$\overline{D}$ pin. The on-chip general purpose Registers may be used as additional RAM memory for minimum chip count systems.

The Data Space is selected by the execution of the SDM instruction. All subsequent memory references will access the Data Space. When a separate Data Space is not required, data may stored in external RAM or ROM memory within the Program Space.

Figure 5. Memory Map



MEMORY (Continued)

ROMless Option

In the event of a program revision being required after the development of a ROM-based ST9036, a mask option is available which enables the reconfiguration of the memory spaces to give a fully ROMless device. This means that the on-chip program ROM is disabled and ALL PROGRAM memory is seen as external, allowing the use of replacement program code in external ROM memory. The on-chip RAM memory in DATA space is not affected.

To give the ROMless function (when enabled by the MASK option), the enabled pin, marked ROMless as an Alternate Function, should be held to ground (V_{SS}) with a high resistance (eg 100k ohm) during the $\overline{RESET}$ cycle. The pin status is latched on the rising edge of the $\overline{RESET}$ input. After this time, the pin is free for normal operation.

If the ROMless option is enabled, and the on-chip program is to be used, the pin enabled for the ROMless function must to held to a high potential during the $\overline{RESET}$ cycle (eg with a 100k ohm resistor to V_{DD}).

REGISTERS

The ST9036 Register File consists of 240 registers (224 general purpose) plus pages of 16 registers supporting the configuration and control registers for the on-chip peripherals. The 224 general purpose registers all have 8 and 16 bit arithmetic capability and may be used as accumulators, on-chip RAM, internal Stack areas (for system and/or user stacks), or, with the appropriate addressing modes, as index, offset or stack pointers.

The register file is arranged into 16 groups of 16 registers, where the general purpose registers occupy the first 14 groups. The 15th group, E, contains the system registers and Group F contains the pages of the on-chip peripheral control registers.

Group F is paged in this manner due to the modularity of the ST9 family of microcontrollers. Each member of the family retains all general purpose and system registers, only the paged register groups changing owing to the different on-chip peripheral organizations of each device. The user can therefore generate code libraries which use the general purpose registers knowing that they will not be lost on future ST9 devices. To address a paged

Figure 6. ROMless Selection

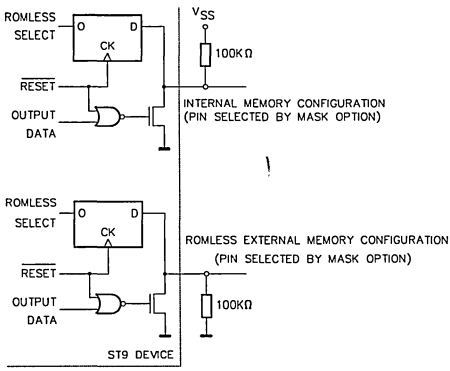


Table 2. Group E Register Map

R239	System Stack Pointer Low (SSPLR)
R238	System Stack Pointer High (SSPHR)
R237	User Stack Pointer Low (USPLR)
R236	User Stack Pointer High (USPHR)
R235	Mode Register (MODER)
R234	Page Pointer (PPR)
R233	Register Pointer 1 (RP1R)
R232	Register Pointer 0 (RP0R)
R231	ALU Flags (FLAGR)
R230	Central Interrupts Control (CICR)
R229	Port 5 Data (P5DR)
R228	Port 4 Data (P4DR)
R227	Port 3 Data (P3DR)
R226	Port 2 Data (P2DR)
R225	Port 1 Data (P1DR)
R224	Port 0 Data (P0DR)

REGISTERS (Continued)

Figure 7. Register Grouping

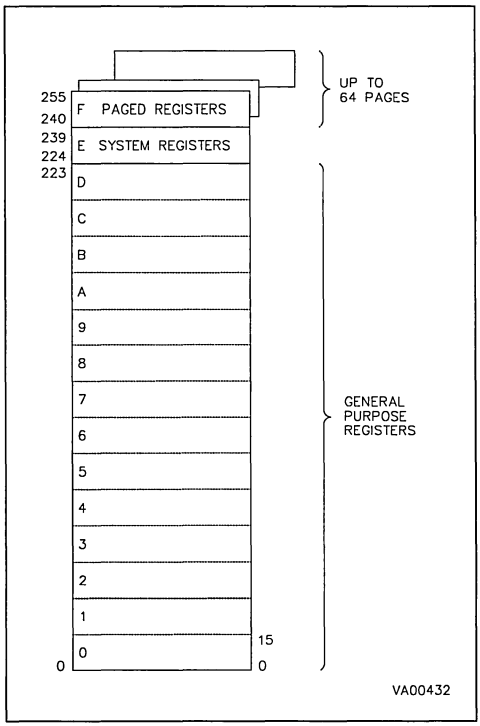
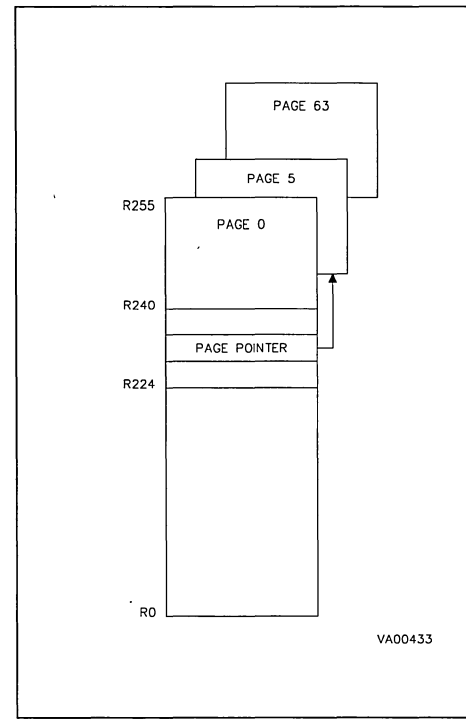


Figure 8. Page Pointer Mechanism



register, the Page Pointer (PPR, R234) within the system register group must be loaded with the relevant page number using the SPP instruction. Subsequently any access to registers in the top group (R240-R255) will refer to the selected page. This remains set until the next change to the Page Pointer register (by the SPP instruction).

The System group (Group E, registers RE0 to REF) includes the system and user stack pointers, the Mode register, the ALU FLAG register and the Page pointer register. In addition the data registers for the first 6 I/O ports are present, the configuration registers for the ports being in the paged area. This allows the immediate access to these I/O ports at all times.

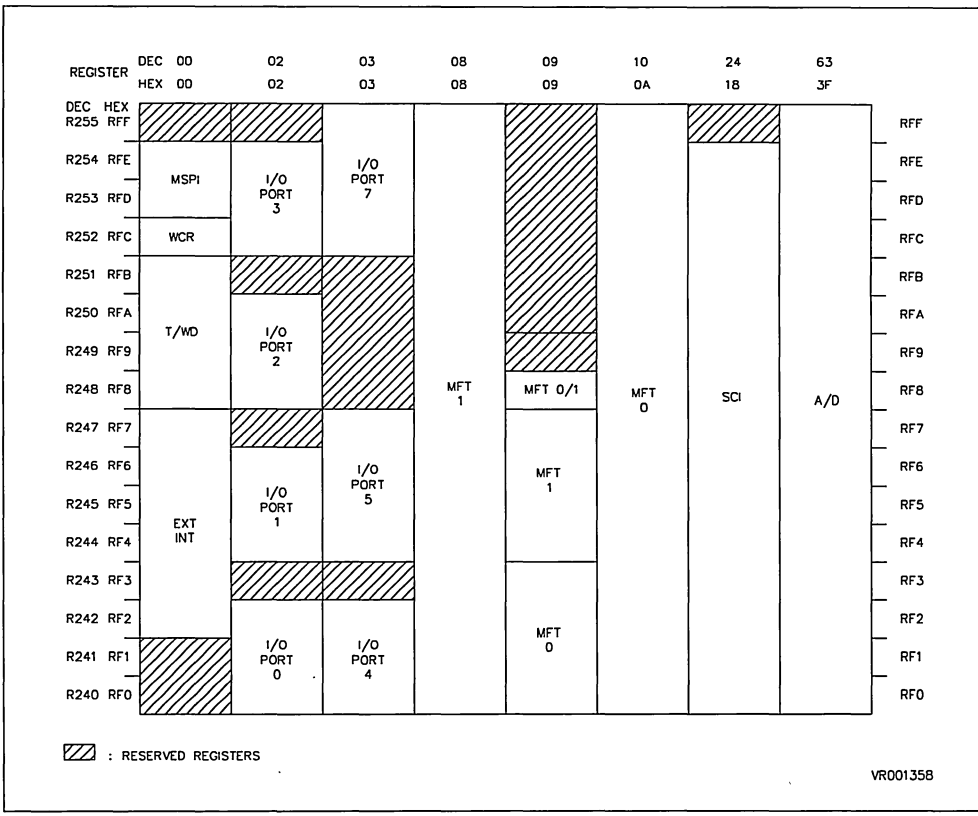
The Register Pointers, present in the system register group, select groups of registers as "Working Registers", which have faster addressing modes than direct Register addressing and allows smaller code size. The Register Pointers may either be used singly, creating a register group as 16 working registers, or as two independent groups of 8 working registers which may be placed at any 8 register boundary within the register file. The single and twin working register modes are automatically set by hardware when the respective SRP and either SRP0 or SRP1 instructions are executed. If working registers are used as accumulators and RAM locations for particular tasks, fast context switching on interrupts may be achieved by setting the register pointer to another group for the Interrupt Service Routine, ISR, (e.g. saving the Register pointer on the stack), using the new group in the ISR and subsequently restoring the original group before the return from Interrupt instruction. Working registers also allow the use of the ABAR - Any Bit-Any Register Boolean operations (including directly on the I/O port data registers).

REGISTERS (Continued)

In the ST9 syntax, directly addressed Registers are indicated with a capital R e.g. R0, R224, RBF, with Register Pairs (16 bit accumulators or memory pointers) as RR0, RR24. When using Working Registers, groups of 16 registers (SRP instruction) are denoted as r0 to r15 (rr0 to rr14), while the dual working register group are addressed as r0 to r7 (rr0 to rr6), for the first group of 8 registers (SRP0), with r8 to r15 (rr8 to rr15) for the second set (SRP1).

Working register addressing requires a 4 bit field within the instruction. When packed into a byte, the upper nibble is set to Dh (1101b), this being the escape code to indicate the use of the working registers. As a result, group D CANNOT be selected with direct register addressing, it is recommended that this group be used as internal stacking area when using register file based system or user stack pointers.

Figure 9. ST9036 Group F Peripheral Organisation



REGISTERS (Continued)

Figure 10. Single Working Register Bank

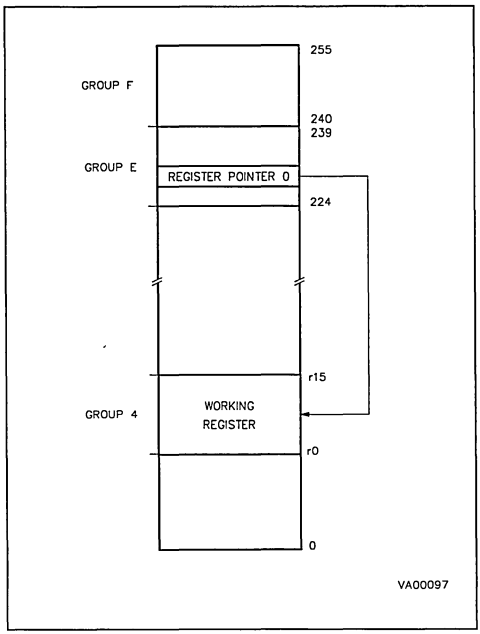
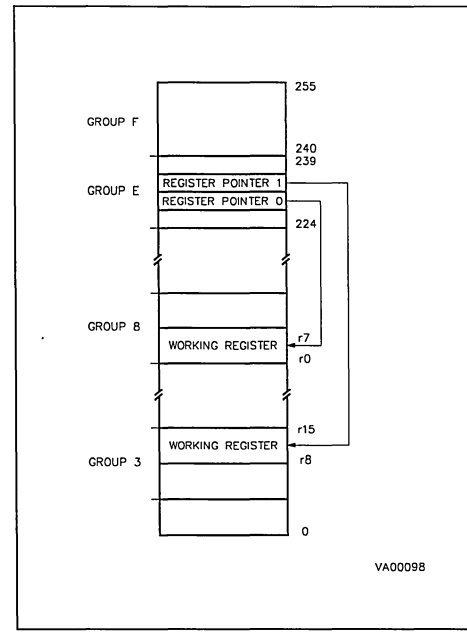


Figure 11. Dual Working Register Banks



STACK POINTERS

There are two separate, double register stack pointers available (System and User), both of which can operate in register or Data memory address spaces. These operate in a Pre-Decrement mode when data is PUSHed onto the Stack and in a Post-Increment mode when data is POPed from the stack.

The SYSTEM Stack Pointer (SSPR, R238:R239) is used for the storage of temporarily suspended system and/or control registers (ie the the Program Counter and FLAG register) while interrupts are being serviced, and is used for the storage of the Program Counter following the CALLing of a subroutine.

The USER Stack Pointer (USPR, R236:R237) is completely free from all interference from automatic operations and so provides for a totally user controlled stack area.

Both Stack pointers may operate with both byte (PUSH,POP) and word (PUSHW,POPW) data, and are differentiated by appending a "U" to the instruction mnemonic for the User Stack (PUSHU/PUSHUW, POPU/POPUW).

When the Stack Pointers are using RAM Memory as the stack areas, a full word register is used as the pointer, while when operating with the stack area within the Register File (Groups 0 to 14 only, but not the within the system and paged groups) only an 8 bit register is required for addressing and consequently only the low byte of the word registers are used (R239 for the System Stack and R237 for the User Stack). In this latter case the upper byte of the stack pointer registers (R238 and R236) must be considered as reserved. The Stack Pointers may be selected to point to RAM or Register File by the setting of the SSP (MODER.7) and USP (MODER.6) of the ST9036 configuration register (MODER, R235) where a "1" denotes Register file operation (Default at Reset) and "0" causes Data space operation.

STACK POINTERS (Continued)

Figure 12. Internal Stack Pointer

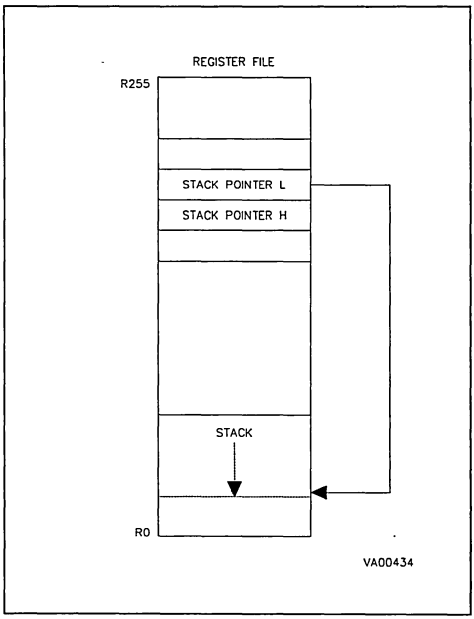
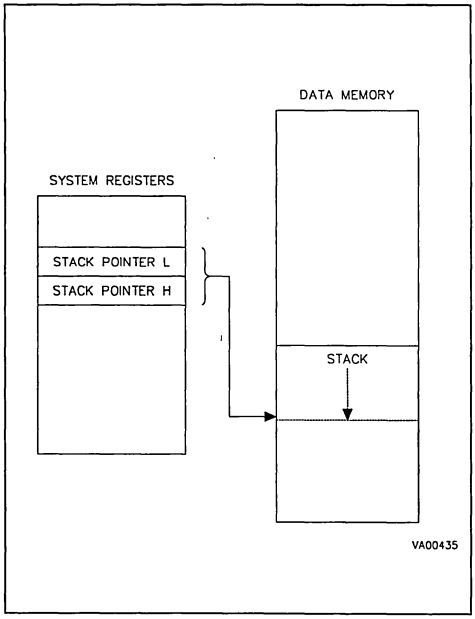


Figure 13. External Stack Pointer



INTERRUPTS

The ST9036 offers a powerful solution to the response requirements of real-time systems with its advanced interrupt structure. Interrupt trigger sources can be prioritized within 8 levels to match the priorities assigned to the application. In addition a top-level or non-maskable interrupt is available.

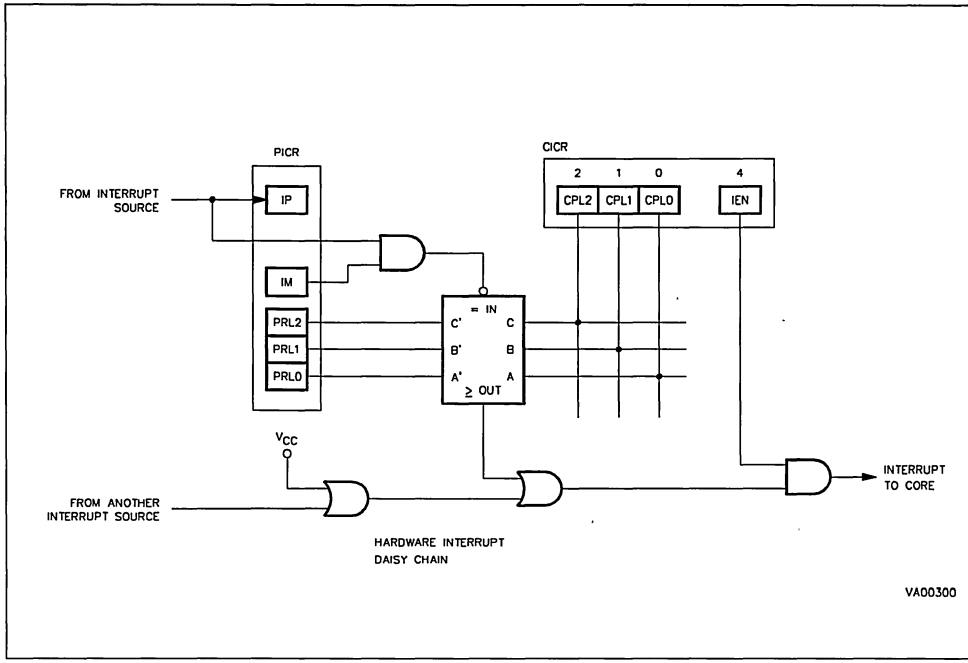
The ST9036 interrupts follow the logical flow of figure 14.

Interrupt events (selectable with each function) cause the setting of the Interrupt Pending (IP) bit within the status register of the peripheral. This bit may also be set by software in order to generate a software interrupt, and should normally be reset by software within the interrupt service routine. If the interrupt is not Masked with the corresponding Interrupt Mask bit, the interrupt is passed to the central interrupt control logic where the priority level assigned by the programmer to the interrupt source is compared with the priority level of the core (user programmed dynamically in the 3 bits of the Central Priority register (CPL, CICR.0-2, Level 7 is the lowest priority and level 0 the highest). If the incoming priority level is higher than the CPL, and Global Interrupts are enabled (by the `EI` instruction, interrupts are disabled by the execution of the `DI` instruction), the interrupt is acknowledged. If interrupts are globally disabled, the priority level of the source is lower than or equal to the CPL or the Interrupt is masked, then the IP bit remains set and the interrupt is held pending until the `EI` instruction is executed, the CPL is set to a lower level AND the interrupt is un-masked. Alternatively the IP bit of a masked interrupt source may be used in a polled interrupt environment, with the IP bit being reset by software within the service routine.

The interrupt acknowledge cycle causes the Program Counter and FLAGS register to be pushed onto the System Stack (PC low byte first, PC high byte, then FLAGS Register) and all maskable interrupts to be disabled by resetting the IEN bit (CICR.4). The peripheral Interrupt Vector, IVR, a user programmable feature of the peripheral interrupt control registers, is used as an offset into the

INTERRUPTS (Continued)

Figure 14. Interrupt Logic



vector table, pointing to the high byte (even address) of the 16 bit address which should contain the starting address of the interrupt service routine. Addresses 0 through 255 of the program space comprise the interrupt vector table. Where multiple interrupt sources may occur within a peripheral, the peripheral interrupt vector source may be encoded by hardware set bits within the IVR register. This means that the vector address defined in the peripheral IVR is the base address for a block of vectors servicing that peripheral. The address pointed to by the vector is loaded into the Program Counter and execution restarts from this point.

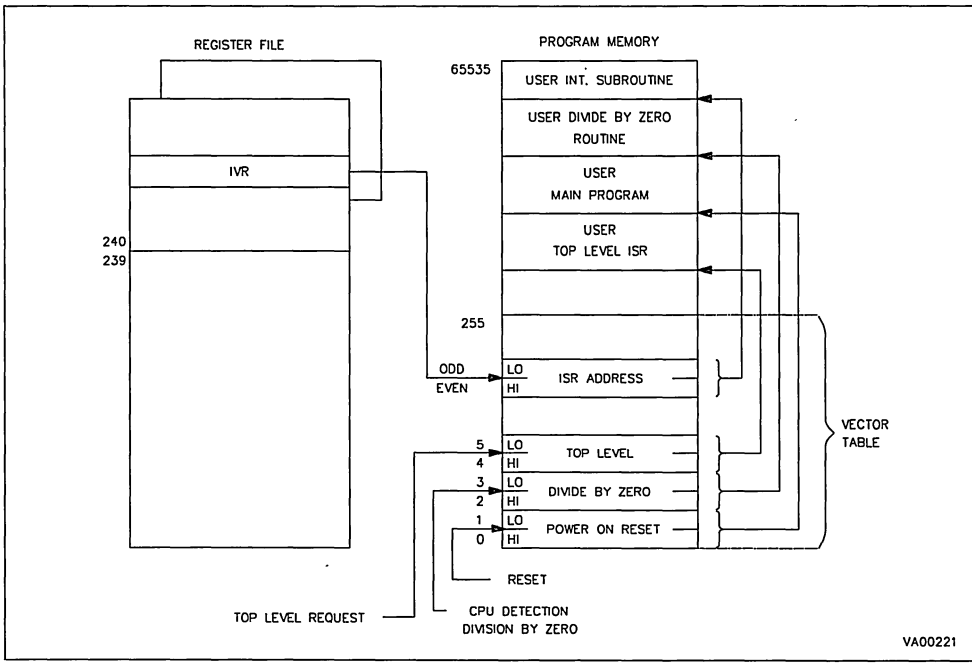
The interrupt service routine should clear the interrupt pending flag of the interrupt source and take the appropriate action. The last instruction of the interrupt service routine should be the `IRET` instruction, the action of this is to restore the Program Counter and Flags register to their value prior to the interrupt acknowledgment, and to re-enable interrupts. Within the interrupt service routine, use may be made of the working register pointer mechanism to reduce the context switching time.

Two interrupt arbitration modes are available for use with the 8 level priority scheme, Nested and Concurrent modes. These are selected by the status of the IAM bit (CICR.3).

Concurrent mode, selected when IAM = "0" (the reset condition) is the standard interrupt arbitration mode, where the arbitration phase of every instruction acknowledges interrupts according to their priority level (if higher than the CPL) and follows the sequence shown above. All pending interrupts existing or having eventually occurred during interrupt service routine execution, remain pending until the Enable Interrupt instruction (`EI`) (even if it is executed during the interrupt service routine). `EI` within the interrupt service routine is not recommended for use with the Concurrent arbitration mode as this can trigger a Last In, First Out condition where high priority interrupts are masked by lower priority interrupts which are all higher than the CPL value.

INTERRUPTS (Continued)

Figure 15. Interrupt Vector Table Usage



Nested mode, selected when IAM = "1", uses the same arbitration phase as concurrent mode, the difference being that the CPL is modified during the interrupt processing cycle to that of the acknowledged interrupt level. The CPL value is pushed by hardware into the Nested Interrupt Control register (NICR, R247 page 0) by setting the NICR bit corresponding to the CPL value. The interrupt service routine is entered in the normal manner. The revised CPL level is used for arbitration of further interrupts, each higher level being saved on the NICR stack, and being restored automatically by hardware with the `IRET` instruction. This allows the execution of the `EI` instruction within the interrupt service routine to operate the correct nesting of interrupts. The two modes are shown graphically in figure 15, where the Y axis shows the CPL value. It should be noted that in the example INT1 will not be acknowledged until the CPL level is programmed to a lower level.

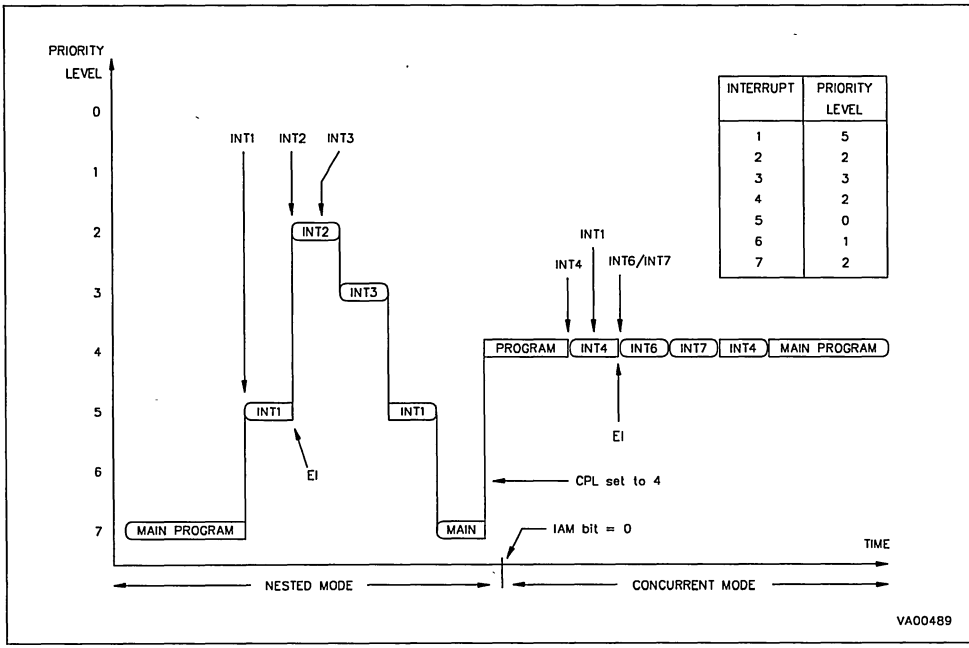
Interrupts coming from on-chip sources at the same instant are resolved during the arbitration phase according to a hardware daisy-chain. This follows the priorities of the table shown in Table 3.

Table 3. ST9036 Interrupt Hardware Daisy Chain

INTA	High Priority
INTB	Lowest Priority
INTC	
INTD	
MFTIMER0	
SCI	
A/D	
MFTIMER1	

INTERRUPTS (Continued)

Figure 16. Interrupt Modes Example of Usage



External Interrupts. Up to 8 external interrupts are available on the ST9036 as alternate function inputs of I/O pins. These may be selected to be triggered on rising or falling edges and can be independently masked. The eight interrupt sources are grouped into four pairs or channels which can be assigned to independent interrupt priority levels. Within each channel the even interrupt number takes the even priority level and the odd channel the odd priority level (even+1).

Several of the External Interrupt channels have their inputs selectable between the external interrupt source and on-chip peripheral sources.

Table 4. External Interrupt Channel Grouping

External Interrupt	Channel
INT7 INT6	INTD1 INTD0
INT5 INT4	INTC1 INTC0
INT3 INT2	INTB1 INTB0
INT1 INT0	INTA1 INTA0

Table 5. ST9040 External Interrupt Source Selection

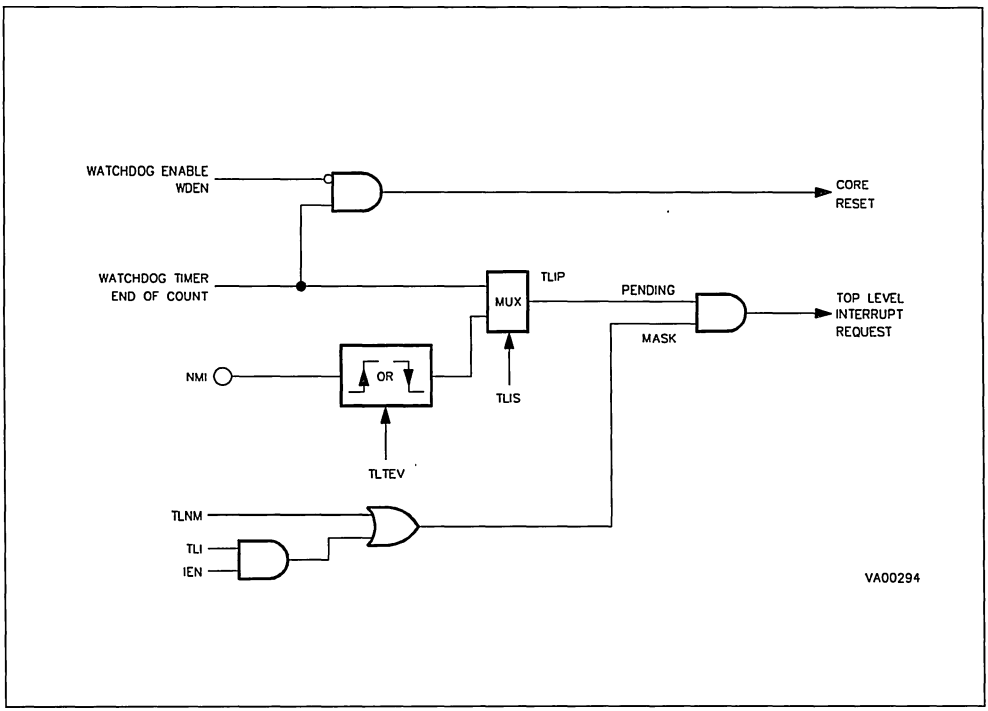
INT0	INTA0
Timer/Watchdog End of Count	
INT2	INTB0
SPI Interrupt	

INTERRUPTS (Continued)

Top Level Interrupt. The Top Level Interrupt.channel can be assigned either to the external NMI pin or to the Timer/Watchdog output. When selected as the external NMI pin, the active edge may be programmed to be rising or falling. The TLI event will cause the setting of the TLIP bit (CICR.6) and according to the mask situation, a Top Level Interrupt request may be generated. Two masking conditions are available, a Maskable Mask and a Not-Maskable Mask.

The Maskable Top Level Interrupt.may be enabled or disabled by software and follows the state of the Global Interrupt Enable bit IEN (CICR.4), while the Not-Maskable Mask bit (TLI, CICR.5) is a set-only mask. Once set, the Top Level Interrupt.is active independently of IEN and cannot be disabled until the next Reset cycle.

Figure 17. Top-Level Interrupt Structure



DMA

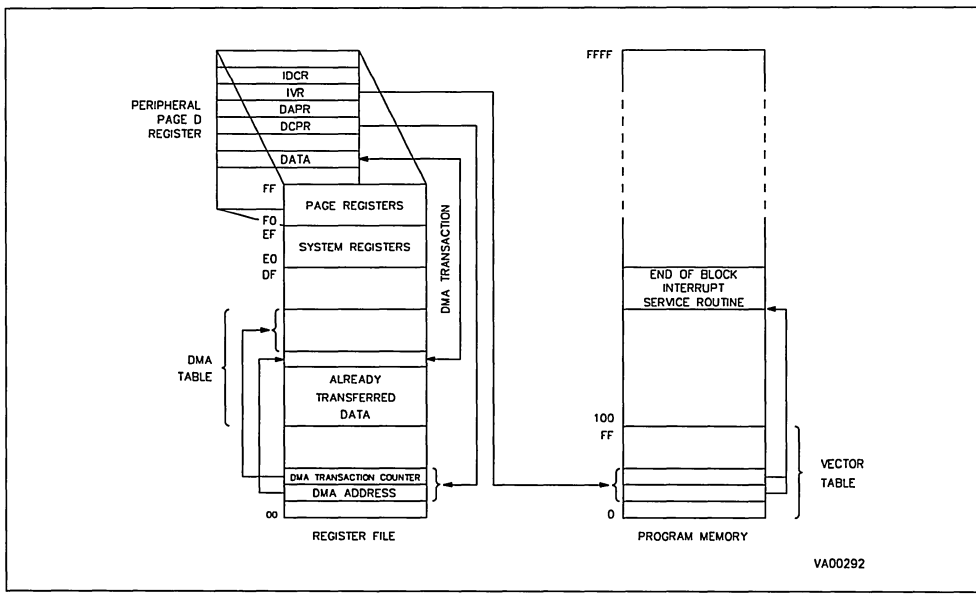
The ST9036 has on-chip DMA channels to provide high-speed data transaction between peripherals and Memory or Register File. Multi-channel DMA is fully supported because each peripheral can have its own DMA channel(s). Each DMA channel transfers data to/from contiguous locations of the Register File, Program Memory or Data Memory. The maximum number of transactions that each DMA channel can perform is 222 if the Register File is selected and 65536 if Program or Data Memory are selected.

DMA transfer to (or from) the Register File takes 8 INTCLK cycles, DMA transfer to (or from) Memory takes 16 INTCLK cycles. If the ST9036 is in the idle mode (following the execution of the `WFI` instruction), DMA requests are acknowledged according to their priority and control is returned to the idle mode pending an interrupt, this operation increases the number of INTCLK cycles by 2 for both Register File and Memory DMA transactions.

Each DMA channel has its own control registers located in the page(s) related to the peripheral. There are two pointer registers, DAPR which points to a register or register pair containing the current DMA address to/from which data will be transferred, and DCPR, which points to a register or register pair which contain the transaction counter for the DMA operations. Each DMA transfer consists of three operations:

- A load from/to the peripheral data register to a location of Register File (or Memory) addressed through the DMA Address Register (or Register Pair)
- A post-increment of the DMA Address Register (or Register Pair)
- A post-decrement of the DMA transaction counter, which contains the number of transactions that have still to be performed.

Figure 18. DMA Between Registers and Peripheral



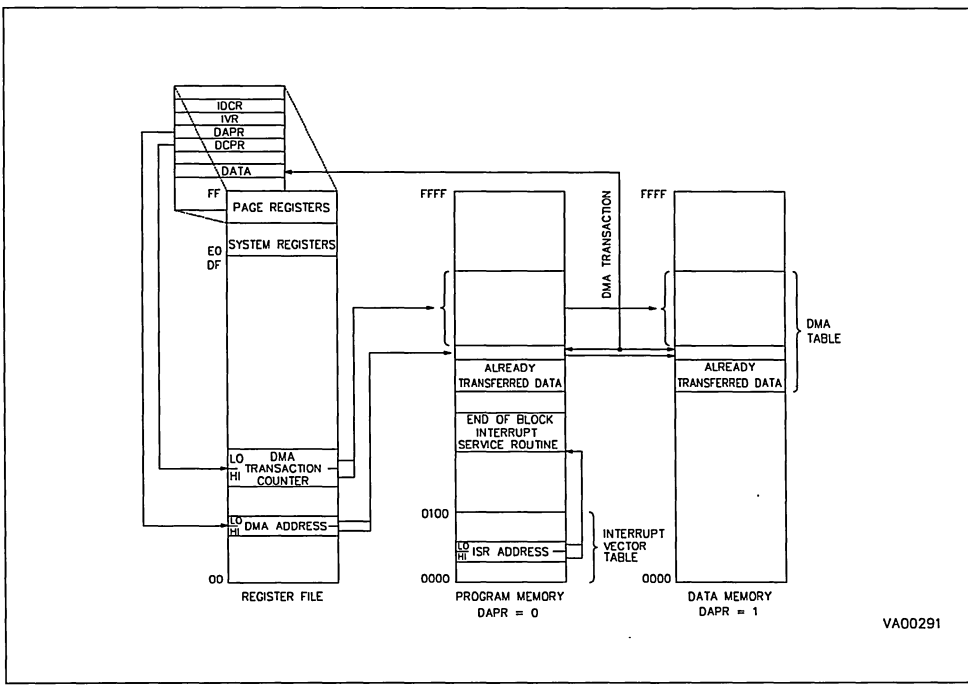
DMA (Continued)

When the transaction counter reaches 0 (all data has been transferred) an End of Block Interrupt is generated to allow the processing of the DMA data block, or, by reloading the Address and counter registers and retriggering, a repeated DMA cycle.

A SWAP mode, allowing continuous DMA operation, is available for the Multifunction Timer and is described in the section relating to the Multifunction Timer.

The ST9036 has DMA channels associated with the Serial Communications Interface Input and Output Serial data channels, the 16 bit Load/Capture Register 0, CAPT0R, of each Multifunction Timer allowing the timing of external signals to be captured into a table for off-line analysis or for the automatic output of PWM signals of variable width and timing, and the 16 bit Comparison Register 0, COMP0R, of each Multifunction Timer which can be programmed to cause output or input of parallel data through the handshake port 5 under DMA.

Figure 19. DMA Between Memory and Peripheral



CLOCK GENERATION, WAIT, HALT AND RESET

Clock Generation

The ST9036 Clock Generator module generates the internal clock for the ST9 core and the on-chip peripherals, it may be driven by an external quartz crystal circuit, connected to the OSCIN and OSCOUT pins, or by an external pulse generator connected to OSCIN (figures 20, 22).

The conceptual schematic of the ST9 internal clock circuit is shown in figure 22.

The maximum external frequency of the ST9 is 24 MHz, while the maximum internal operating frequency is 12 MHz, thus a programmable divide by two circuit is present, this allows the use of high frequency crystals for economy, or low frequency crystals for reduction in radiated noise. This divider is active upon exit from the reset condition, the user may bypass the divide by two circuit by setting the DIV2 bit (MODER.5). The resulting clock from this

Figure 20. Crystal Oscillator

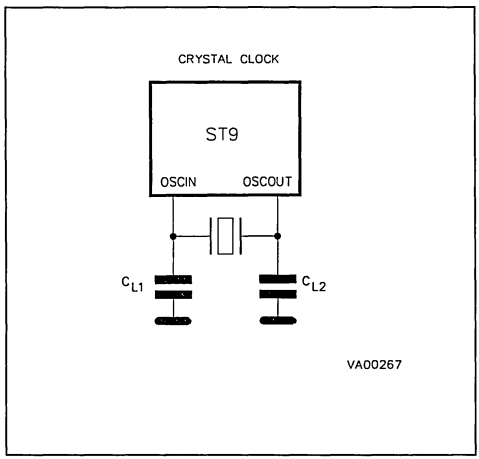


Figure 21. External Oscillator

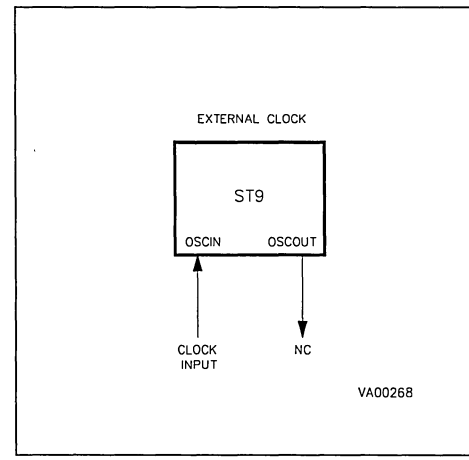
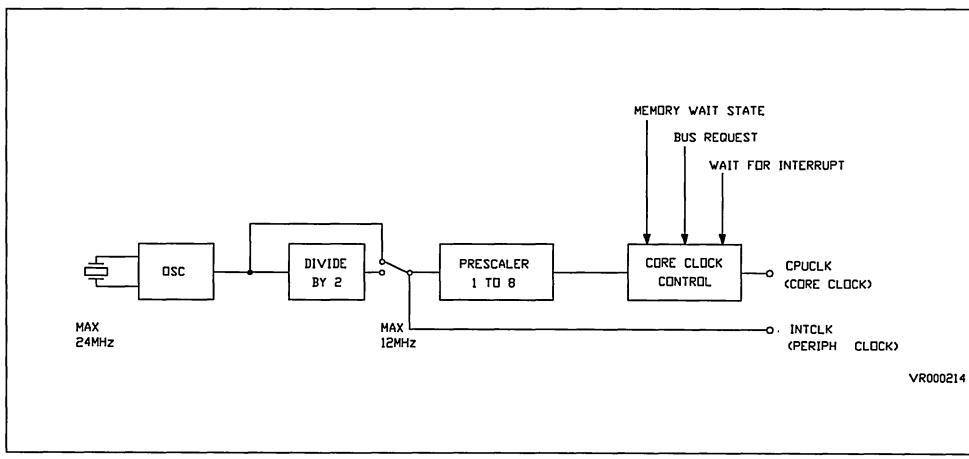


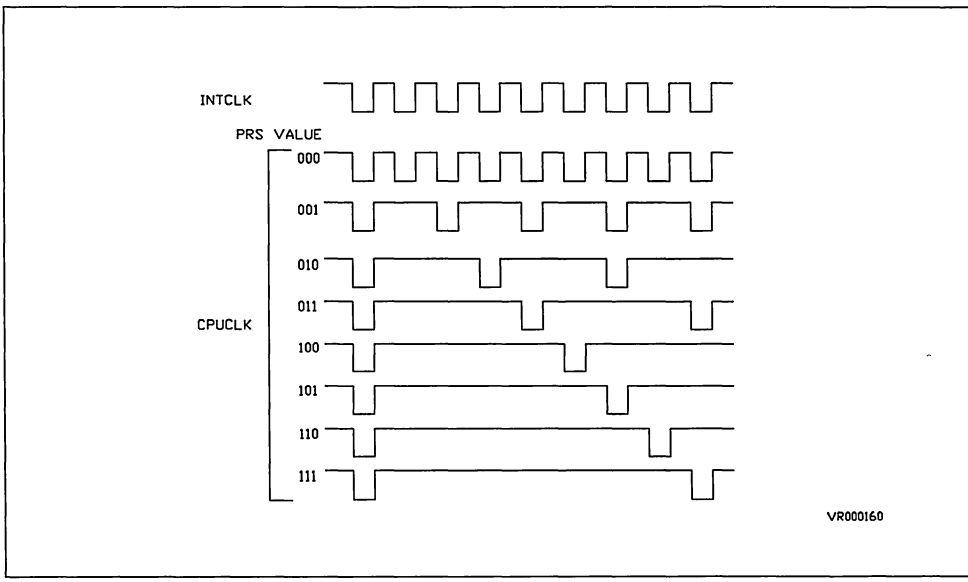
Figure 22. Internal Clock Circuit



CLOCK GENERATION, WAIT, HALT AND RESET (Continued)

section is named INTCLK, the internal clock which drives the timebases of the on-chip clock for the ST9036 peripherals (eg the Multifunction Timer, Timer/Watchdog, Serial Communications Interface) and also the input of the CPU prescaler section. The CPU of the ST9 includes the instruction execution logic and may run at different rates according to the setting of the PRS2,PRS1 and PRS0 bits (MODER.4-2) (figure 23). The resulting clock is named CPUCLK and it should be noted that this does not maintain a 50% duty cycle, but stretches the high level of the clock until completion. The CPUCLK prescaler allows the user to slow down the program execution time (eg for lower power consumption), while time-critical sections of the program may tune the CPUCLK execution speed to high speed and then restore it to its original speed.

Figure 23. CPUCLK Prescaler



CLOCK GENERATION, WAIT, HALT AND RESET (Continued)

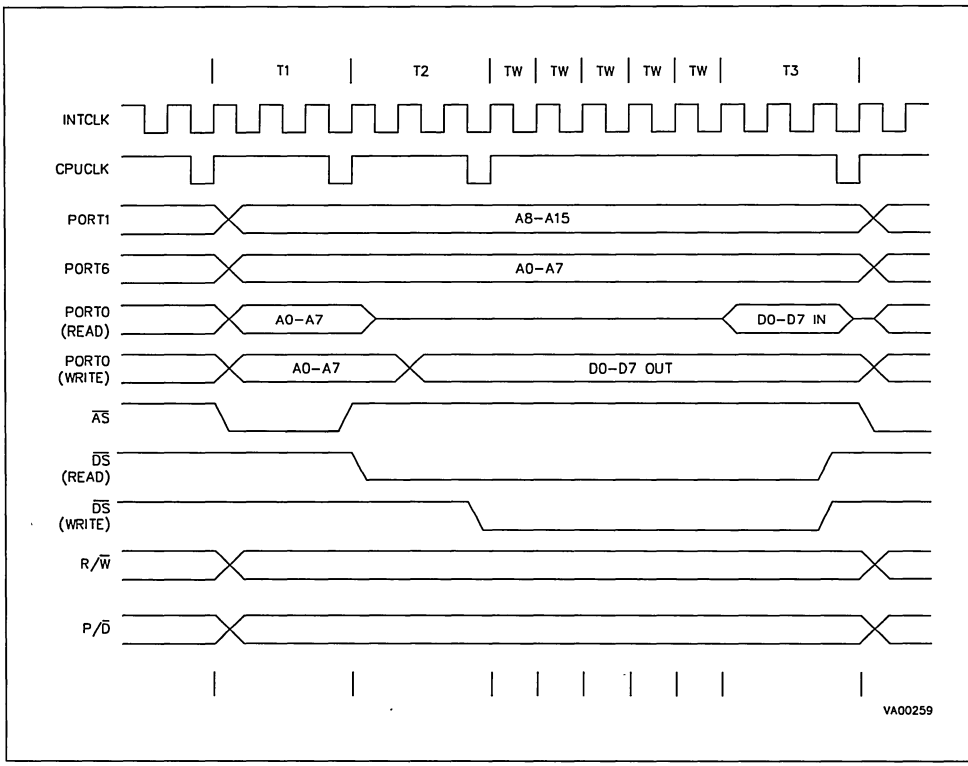
Wait States

The output from the prescaler can also be affected by wait states. Wait states from two sources allow the user to tailor timing for slow external memories or peripherals. The internal Wait State generator will insert from 0 to 7 wait states, independently programmable for both Program and Data Spaces via the Wait Control Register WCR (R252, page 0). The second source of wait states is the external Wait input pin when enabled as the Alternate Function. Fig 24 shows the External Memory Interface timing as it relates to CPUCLK prescaling of 2 and 5 added wait states. The added wait states are derived from the INTCLK clock cycle, not CPUCLK. Internal memory is always accessed with no Wait states.

Halt and Wait for Interrupt(WFI) States

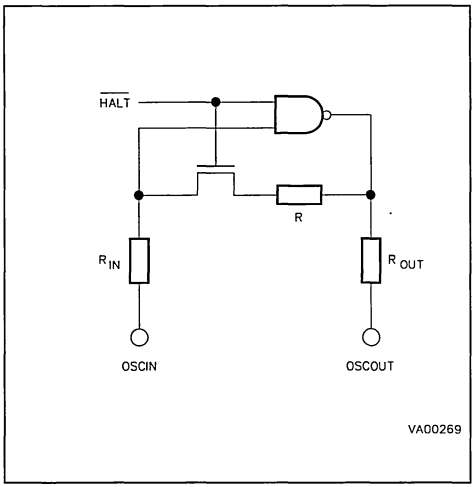
The schematic of the on-chip oscillator circuit is shown in figure 25. The HALT condition, caused by the execution of the HALT instruction, disables the oscillator, forcing OSCOUT high. This places the ST9036 into the lowest power mode. The exit of the HALT condition and the restarting of the oscillator requires a $\overline{\text{RESET}}$ pulse with a minimum duration of 10ms (figure 26). It must be noted that if the TIMER/WATCHDOG has the WATCHDOG mode enabled, a HALT instruction will not disable the oscillator; this is to avoid stopping the Watchdog if, by an error, a HALT instruction is executed. When this occurs, the ST9036 runs in an endless loop ended by the Watchdog reset.

Figure 24. External Memory Interface Timing with CPUCLK Prescaling and 5 Added Wait States



CLOCK GENERATION, WAIT, HALT AND RESET (Continued)

Figure 25. Oscillator Schematic



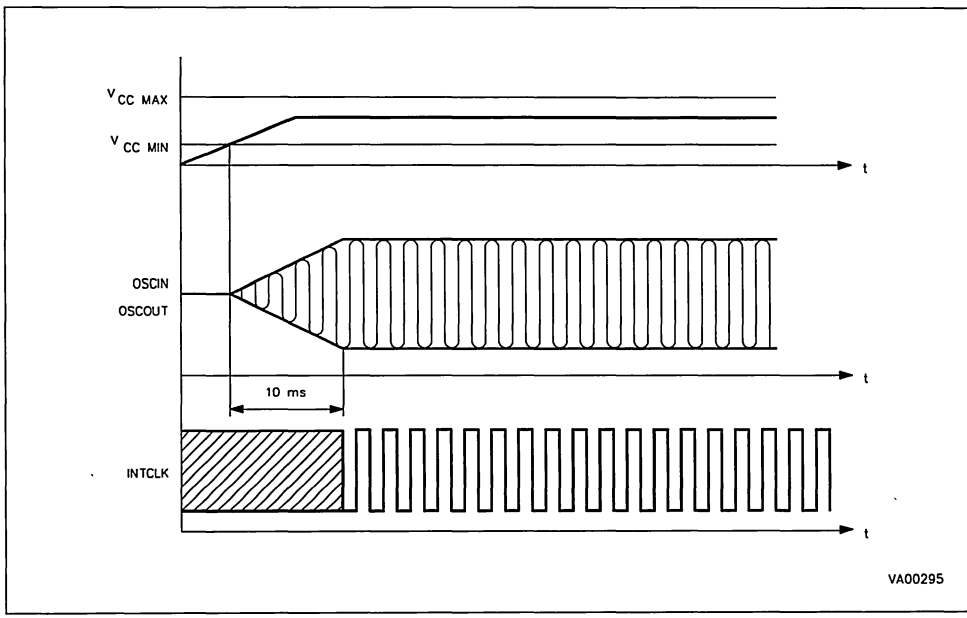
The WFI (Wait for Interrupt) instruction suspends program execution until an interrupt request is acknowledged. During this period, DMA transactions are allowed if their priority is higher or equal to the CPL level, the ST9036 returns to WFI mode after completion of the DMA transfer. The CPUCLK is halted during Wait For Interrupt while INTCLK continues to run, thus the power consumption of the processor is lowered by the CORE power consumption value.

The External Memory Interface lines status during HALT and WFI modes is shown in Table 6.

Table 6. External Memory Interface Line Status During WFI and Halt

P0 (AD0-AD7)	High Impedance
P1 (A8-A15)	Forced to Address of Next Opcode
$\overline{AS}$	Forced High
$\overline{DS}$	Forced High
R/$\overline{W}$	Forced High

Figure 26. Reset Timing Requirements from Halt State



CLOCK GENERATION, WAIT, HALT AND RESET (Continued)

Reset

The processor Reset overrides all other conditions and forces the ST9036 to the reset state. During Reset, the internal registers are set to their Reset values, as shown in Table 7 for the system and Page 0 Registers. The I/O Ports pins are set to the Bidirectional Weak Pull-up mode. The programmer must then initialize the ST9036 registers to give the required functions.

The Reset condition can be generated from the external $\overline{\text{RESET}}$ pin or by the on-chip TIMER/WATCHDOG operating in Watchdog mode. To guarantee the complete reset of the ST9036, the $\overline{\text{RESET}}$ input pin must be held low for at minimum of 53 crystal periods in addition to the crystal start-up period. The Watchdog $\overline{\text{RESET}}$ will occur if the Watchdog mode is enabled (WDEN, WCR.6, is reset) and if the programmed period has elapsed without the code 0AAh,55h written to the appropriate register. The input pin $\overline{\text{RESET}}$ is not driven low by the on-chip reset generated by the TIMER/WATCHDOG.

During the $\overline{\text{RESET}}$ state, $\overline{\text{DS}}$ is held low and $\overline{\text{AS}}$ is toggled with the frequency of the crystal (OSCIN) divided by 32. This condition may be recognized by external peripherals as a Reset condition. It may also be used to enable the synchronization of multiple ST9036s running from the same clock in a multi-processing or high security majority voting system.

Once the Reset pin reaches a logical high, the ST9036 fetches the starting address from locations 0 and 1 of the program space and begins program execution from this address after 67 crystal cycles.

Table 7. System and Page 0 Reset Values

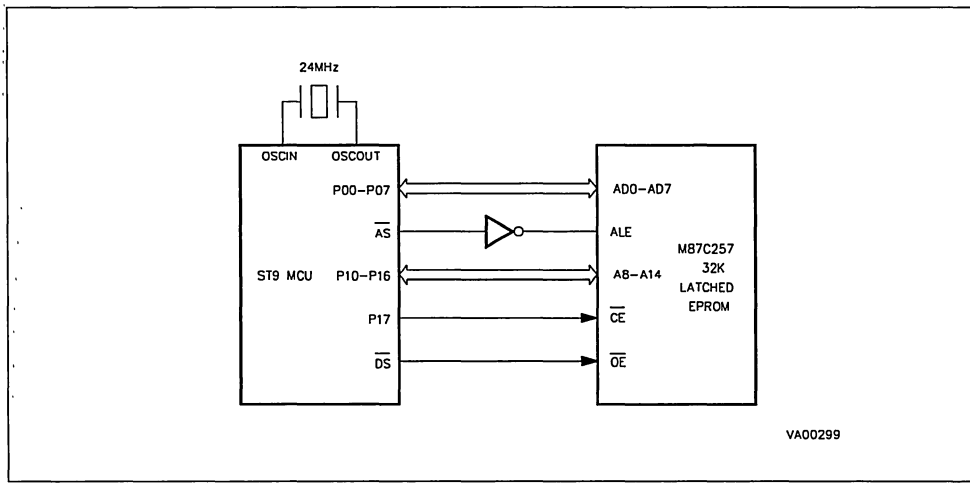
Register Number	System Register Reset Value	Page 0 Register Reset Value
F	(SSPLR) = undefined	Reserved
E	(SSPHR) = undefined	(SPICR) = 00h
D	(USPLR) = undefined	(SPIDR) = undefined
C	(USPHR) = undefined	(WCR) = 7Fh
B	(MODER) = E0h	(WDTCR) = 12h
A	(Page Ptr) = undefined	(WDTPR) = undefined
9	(Reg Ptr 1) = undefined	(WDTLR) = undefined
8	(Reg Ptr 0) = undefined	(WDTHR) = undefined
7	(FLAGR) = undefined	(NICR) = 00h
6	(CICR) = 87h	(EIVR) = x2h
5	(PORT5) = FFh	(EIPLR) = FFh
4	(PORT4) = FFh	(EIMR) = 00h
3	(PORT3) = FFh	(EIPR) = 00h
2	(PORT2) = FFh	(EITR) = 00h
1	(PORT1) = FFh	Reserved
0	Reserved	Reserved

INTERFACING TO EXTERNAL MEMORY

External Memory and/or peripherals may be connected to the ST9036 through its External memory interface. This provides the multiplexed Address bits A0 to A7 and Data bits D0 to D7 as Alternative Functions of Port 0, and the higher order address bits A8 to A15 as Alternative Functions of Port 1, giving the full 64K bytes addressing capability. The Program/Data (P/$\overline{D}$) output, when selected as an Alternate function, allows external decoding to provide for the two independent pages of 64K bytes for Program and Data.

Data transfer timing is generated by the Address strobe $\overline{AS}$ and the data strobe $\overline{DS}$. Address strobe low indicates that the data present on AD0 to AD7 is the low order address and is guaranteed valid on the rising edge of $\overline{AS}$ allowing for latching of the address bits by an external latch. Data transfer direction is indicated by the status or the Read/Write (R/$\overline{W}$) pin; for write cycles (R/$\overline{W}$ low), data out is valid at the falling edge of $\overline{DS}$; for read cycles (R/$\overline{W}$ high), data in must be valid prior to the rising edge of $\overline{DS}$. The Data Strobe low period may be extended to accomodate slow external devices by the adding of internally generated wait cycles (0 to 7 cycles for both program and/or data memory maps) or by an external input on the WAIT input pin also available as an Alternative Function of an I/O bit. Suggested interface circuits are shown in figure 27.

Figure 27. External Memory Addressing Circuit



BUS CONTROL

Multi-processing or external program testing may be accomplished by disabling the I/O ports used for external memory addressing and the associated timing signals.

High Impedance Mode

The programmer may place the External Memory Interface (I/O ports 0 and 1, Address Strobe, Data Strobe and Read/Write) into the high impedance state by setting the HIMP bit (MODER.0). External test equipment may then drive the memory lines for automatic test, external memory validation or programming. The ST9 will continue to execute internal programs, providing no external memory is addressed, allowing the execution of security routines without showing the externally the addresses used.

Bus Request/acknowledge

The External Memory Interface address ports and timing signals may be forced to their high impedance state by utilizing the $\overline{BUSREQ}$, Bus Request, and $\overline{BUSACK}$, Bus Acknowledge, signals available as Alternate Functions of two I/O pins (please refer to the pin configuration drawings for availability of these lines for the package chosen). The signals, $\overline{BUSREQ}$ and $\overline{BUSACK}$, must be enabled by setting the BRQEN bit (MODER.1). Once enabled, a low level detected on the $\overline{BUSREQ}$ pin at the start of an internal machine cycle will cause the stretching of the CPUCLK, and $\overline{BUSACK}$ to go low indicating that the External Memory Interface is disabled. The $\overline{BUSREQ}$ pin is then continuously monitored, and when sampled high, the External Memory Interface pins are driven by the ST9 within two INTCLK cycles.

I/O PORTS

Summary of Function

For the ST9036, only twelve pins have a Reserved function: V_{DD}, V_{SS}, $\overline{RESET}$, $\overline{AS}$, $\overline{DS}$, R/$\overline{W}$, OSCIN, OSCOUT, the Analog to Digital Converter Voltage references, and the External Interrupt 0 and 7 input pins. All other pins are available as Input/Output (I/O) for the user, grouped into Ports of 8 bits. These may be programmed to be Input, Output, Bidirectional or Alternate Function (Peripheral or Memory Interface), on a bit by bit basis, at any time. When programmed as an Input the pin may be set to TTL or CMOS input threshold levels, while, when programmed as Output, Push-Pull or Open Drain configuration may be selected. The Bidirectional mode sets the pin with a weak pull-up resistor to V_{DD} or to Open Drain, allowing bidirectional communication with external logic. The Alternate Function setting is predetermined for each pin as shown in the Pin Configuration Table.

The circuitry of the I/O port allows for several ST9036 peripheral functions to address, as Alternate Functions, the same pin, for both input and output, the programmer selects which peripheral function is to be active by enabling its individual Input or Output function. This multi-function I/O capability of the ST9036 allows for easy adaptation to external circuits. The options available for each bit are summarized in Table 8 :

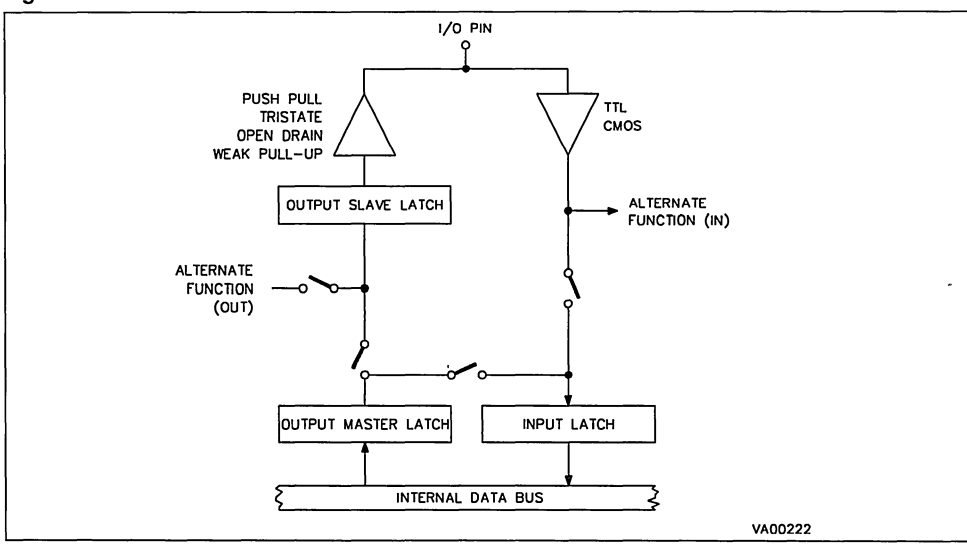
Table 8. I/O Setting Options

Input	TTL Thresholds
	CMOS Thresholds
Output	Open Drain
	Push-Pull
Bidirectional	Open Drain
	Weak Push-Pull
Alternate Function	Open Drain
	Push Pull

I/O Port Configuration

The configuration of each general I/O bit of the ST9036 is set by the corresponding bits in three I/O Port control registers. These affect the status of the input and output buffers of the pin, and enable the Alternate function Outputs. Alternate Function inputs are always connected, and are used by enabling the function from within the configuration registers of the relevant peripheral function. The configuration of an I/O bit is shown in figure 3.1.2. Outputs follow a Master/Slave buffer, data is transferred from the ST9 internal data bus at the beginning of the machine cycle, and, if enabled as output, is passed to the output latch at the end of the cycle. This synchronization allows for the Bidirectional use of the pin without potential conflicts.

Figure 28. I/O Port Schematic



I/O PORTS (Continued)

Configuration Registers.

Three registers are used to allow the setting of each pin, generically PxC2R, PxC1R, PxC0R, where x relates to the 8 bit I/O port in which the bit is present.

The setting of the corresponding bit in each register to achieve the desired functionality of the I/O pin is shown in Table 9.

The effect of the configuration settings of Table 9 on the I/O ports structure is shown in figures 31 to 32

Table 9. Port Configuration Status Bits

PxC2n	0	1	0	1	0	1	0	1
PxC1n	0	0	1	1	0	0	1	1
PxC0n	0	0	0	0	1	1	1	1
Pxn Configuration	BID	BID	OUT	OUT	IN	IN	AF	AF
Pxn Output	WP	OD	PP	OD	HI	HI	PP	OD
Pxn Input	TTL	TTL	TTL	TTL	CMOS	TTL	TTL	TTL

Legend:
x = Port
n = Bit
BID = Bidirectional
OUT = Output
IN = Input
AF = Alternate Function

WP = Weak Push-Pull
OD = Open Drain
PP = Push-Pull
HI = High Impedance
TTL = TTL Std Input
CMOS = CMOS Std Input

Figure 29. I/O Port Input Configuration

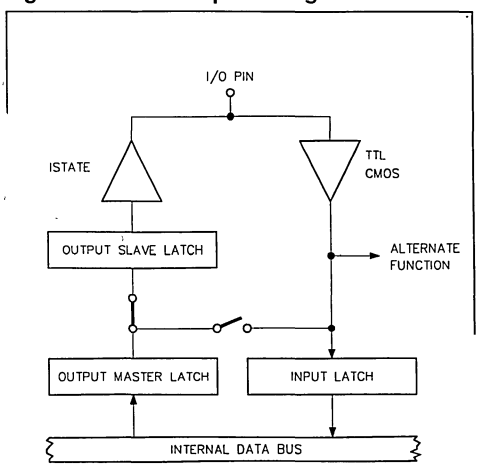
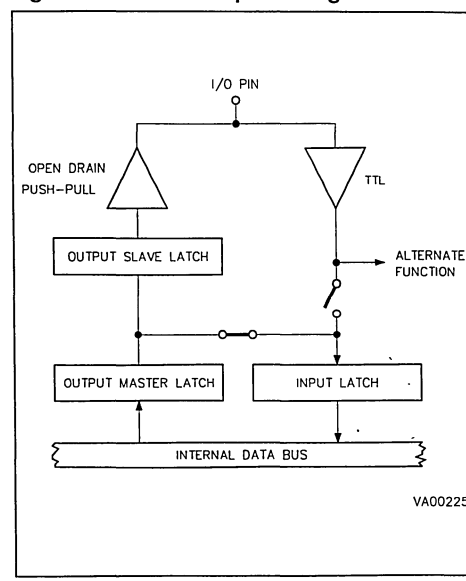


Figure 30. I/O Port Output Configuration



I/O PORTS (Continued)

Figure 31. I/O Port Bidirectional Configuration Setting

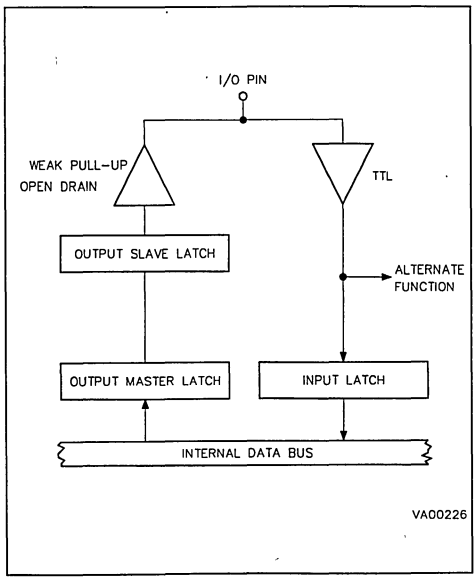
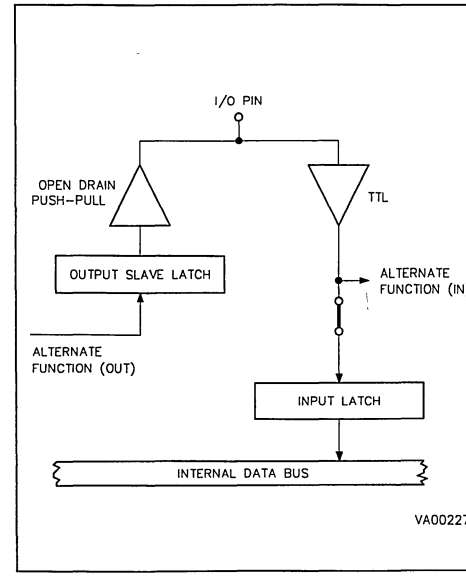


Figure 32. I/O Port Alternate Function Configuration



I/O Register Map

The Data Registers which correspond to the pin status (after configuration) of I/O port 0 to 5, are found in Group E of the Register File, for immediate access at all times, while the configuration registers and the Data Registers for Additional Ports are found within I/O pages (Group F) 2 and 3.

Figure 33. I/O Register Maps

GROUP E			GROUP F		PAGE	
DEC	HEX		DEC	HEX	02	03
			R255	RFF	RESERVED	P7D
			R254	RFE	P3C2	P7C2
			R253	RFD	P3C1	P7C1
			R252	RFC	P3C0	P7C0
			R251	RFB	RESERVED	RESERVED
			R250	RFA	P2C2	RESERVED
			R249	RF9	P2C1	RESERVED
			R248	RF8	P2C0	RESERVED
			R247	RF7	RESERVED	HDC5
			R246	RF6	P1C2	P5C2
R229	RE5	P5D	R245	RF5	P1C1	P5C1
R228	RE4	P4D	R244	RF4	P1C0	P5C0
R227	RE3	P3D	R243	RF3	RESERVED	RESERVED
R226	RE2	P2D	R242	RF2	P0C2	P4C2
R225	RE1	P1D	R241	RF1	P0C1	P4C1
R224	RE0	P0D	R240	RF0	P0C0	P4C0

I/O PORTS (Continued)

Handshake and DMA

I/O Port 5 of the ST9036 is able to support a parallel interface port with handshake capability. This allows one, two or four wire interconnecting handshake signals and facilitates very fast parallel transfer of data for input and output, or for the interconnection of peripheral devices requiring strobe signals for synchronization. Table 9 shows the available options for input and output status and strobe signals available as Alternate Functions of I/O port bits (see Pin Configuration). The Handshake configuration is set within the Handshake Control Register (HDC*n*R) for the relevant I/O port *n*.

Data transfer through the parallel I/O port with handshake can also be triggered through a DMA channel. Timing is generated by the ST9036 TIMER ON-CHIP EVENT strobe signal (see the MULTIFUNCTION TIMER section for information on generating these signals), which causes the programmed transfer of data to or from the memory source which can be Register File, Program space memory or Data space memory. An example of application of this technique is shown in figure 34, a complex stepper motor timing sequence automatically being transferred from a table in the Register File (or memory spaces) to the stepper motor drivers. After initialization, this operation is transparent until the task (complex microstepping) is completed.

Table 10. Handshake Control Signal Options

Mode	Handshake Lines	Names
Input to Port	1	WRRDY
	2	$\overline{\text{WRSTB}}$ WRRDY
Output from Port	1	RDRDY
	2	$\overline{\text{RDSTB}}$ RDRDY
Bidirectional	4	$\overline{\text{WRSTB}}$ WRRDY $\overline{\text{RDSTB}}$ RDRDY

Figure 34. Handshake + DMA Used for Stepper Motor Driving

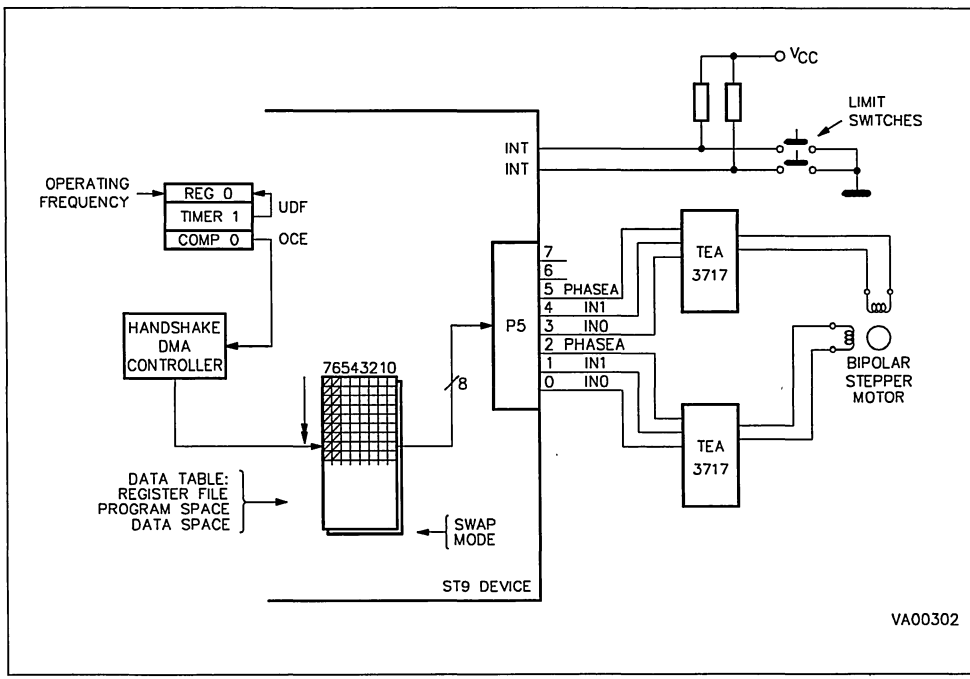
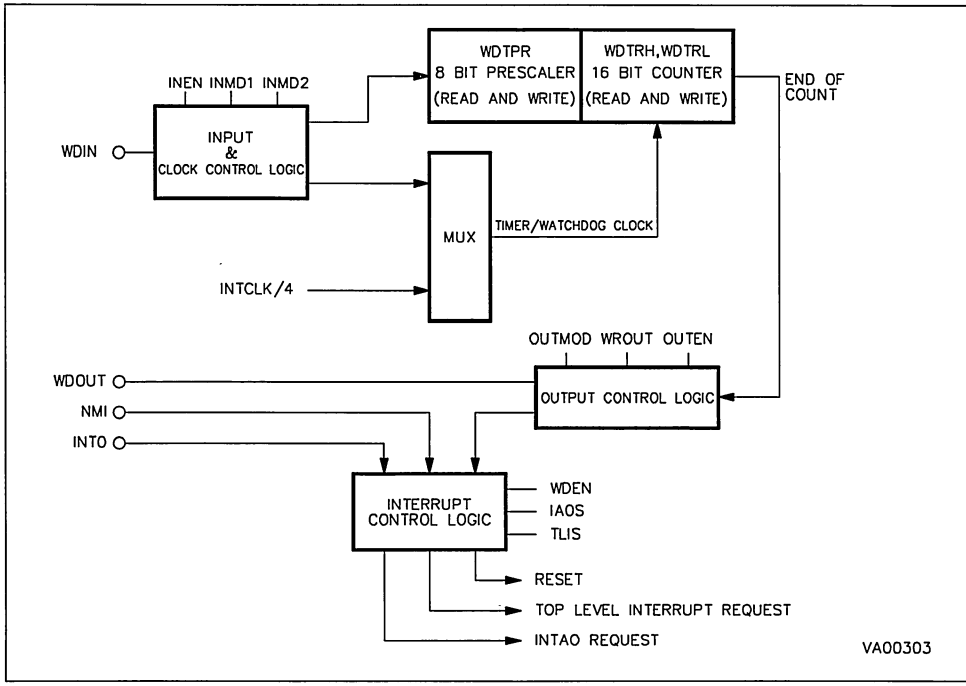


Figure 35. Timer/Watchdog Block Diagram



TIMER/WATCHDOG

A 16 bit down-counter, complete with 8 bit prescaler, is integrated into the ST9036 core. This is able to operate both as a general purpose timer with associated input and output pins for timing functions, and also as a Watchdog Timer offering a security against possible processor malfunctions due to external events.

Timer Modes

When operating as a Timer, with a timing resolution from 333ns to 5.59s (INTCLK = 12MHz), an input pin (WDIN) and output pin (WDOUT) may be selected as the Alternate Functions of two I/O pins. When WDIN is enabled by the user by setting INEN high (WDTCR.3) and the Alternate Function is set, 4 operating modes are available: The WDIN input may be programmed to act as an event counter input, with high to low transitions causing the counter to decrement (the time duration between the falling edges of the input clock must be at least 333ns, allowing a maximum input frequency of 3MHz). It may also be used for pulse width measurement by being selected as a counter clock gate signal (prescaler to the counter being driven by INTCLK/4), counting being enabled when WDIN is at a high level. Trigger and Re-trigger modes cause a reload of the timer user preset values (providing STSP, WDTCR.7 is active) for a high to low transition on WDIN at any time (Re-trigger mode) or when the counter is at the end of count (Trigger mode). The counter decrements at a rate driven by INTCLK/4.

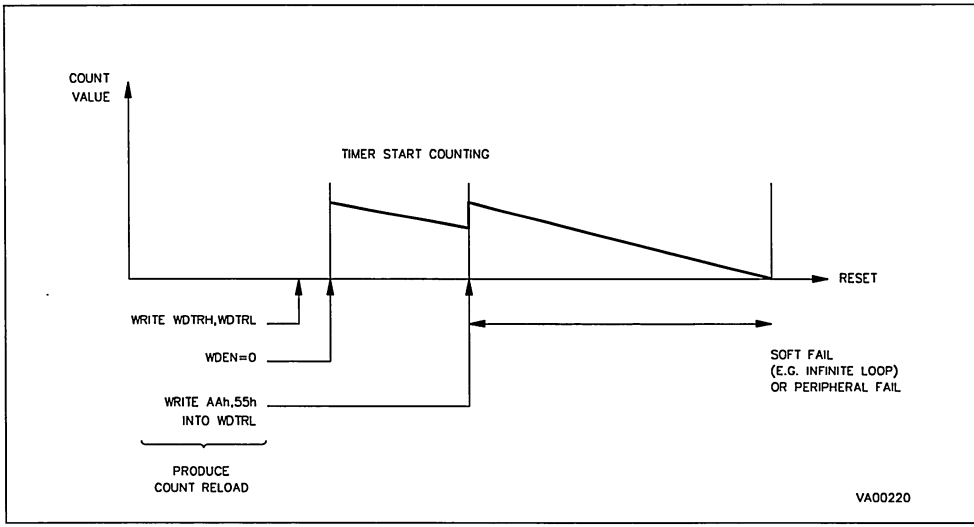
The WDOUT pin, when set as the Alternate Function, is enabled by OUTEN high (WDTCR.0), and may either toggle the state of the I/O bit (frequency generation, OUTMD = "0", WDTCR.2) or pass the state of the WROUT bit to the output allowing PWM generation (OUTMD = "1") at the end of count (timer value = "0") condition.

Watchdog Mode

The timer functions may be disabled, and the Timer configured for a Watchdog operation by re-setting WDEN (WCR.6) to zero. Once the Watchdog has been selected it CANNOT be set back into the standard timer mode until the next Hardware Reset cycle. The programmer should set the watchdog

TIMER/WATCHDOG (Continued)

Figure 36. Timer/Watchdog in Watchdog Mode



timer prescaler and timer reload value before enabling the Watchdog mode. The Watchdog Timer must then be retriggered, causing the reloading of the timer value, by the operation of writing of the byte sequence 0AAh, 055h to the WDTLR register. If this is not done before the Watchdog counts to zero, the Watchdog Timeout condition occurs. This causes a Hardware Reset of the ST9036. The Watchdog reset signal is not output on the external Reset pin.

Timer/Watchdog Interrupts

The Timer/Watchdog may provide several levels of interrupts selectable by the programmer. The Timer mode offers two interrupt sources, triggered on the timer value reaching 0, either a prioritized level (by taking the Interrupt priority channel from the External Interrupt INTA0) or by a top level, non-maskable interrupt (taking the external NMI input channel). The interrupt channels are multiplexed from the alternative source according to the status of the IAOS (EIVR.1) and TLIS (EIVR.2) bits as shown in figure 37. Please refer to the ST9 Technical Manual for further details on changing the interrupt sources of the Timer/Watchdog. When the Watchdog mode is set (WDEN = "0"), the timer value equal to 0 event generates a Hardware reset of the ST9036. The Timer/Watchdog control registers are located within Page 0 of the Paged I/O register group.

Figure 37. Timer/Watchdog Interrupt Sources

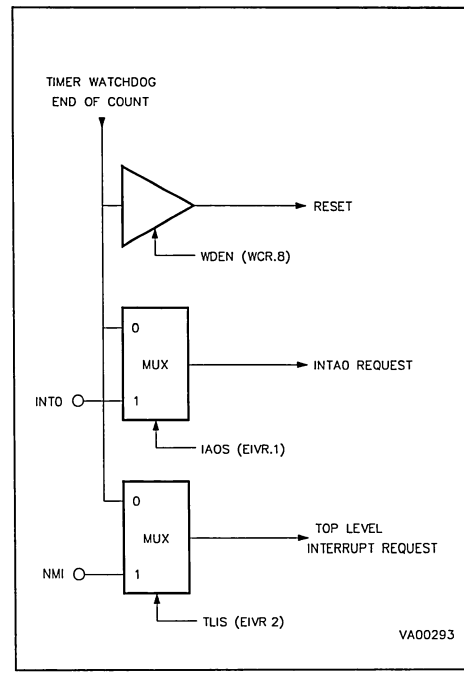
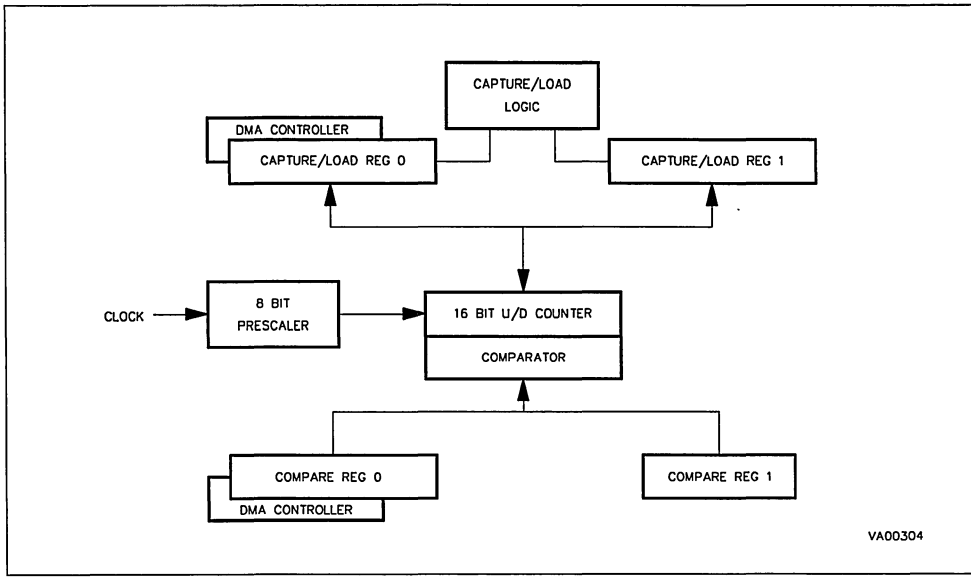


Figure 38. Multifunction Timer Block Diagram



MULTIFUNCTION TIMER

The ST9036 includes two identical 16 bit Multifunction Timers (MFT) in addition to the TIMER/WATCHDOG. The following description applies to both Timer 0 and Timer 1.

Each timer is a 16 bit Up/Down counter, driven by the output of an 8 bit prescaler which may be driven by INTCLK/3 (giving a minimum timing resolution of 250ns at INTCLK = 12 MHz) or by an external source. This timer is supported by two 16 bit Comparison Registers for generating timed functions and two 16 bit Capture/Load Registers for timing and variable timebase functions. These features coupled with 2 input pins (TxINA and TxINB) and 2 output pins (TxOUTA and TxOUTB, where x = 0 or 1), available as Alternate Functions, giving the timer 13 operating modes for virtually all required timing functions.

MFT Operating Modes

The operating modes are selected by the programming of the Timer Control Register (TCR Timer x) and the Timer Mode Register (TMR) as follows:

table: **One-Shot Mode.** The counter stops at the End Of Count Condition (up or down count).

Continuous Mode. At End Of Count the timer is reloaded from a Load Register.

Trigger Mode. A Trigger causes reload from a load register only if the Timer is at End of Count.

RETrigger Mode. A Trigger causes reload from a load register at any time.

Gate Mode. Counting is performed only when the external gate input (TxINA or TxINB) is active (logical 0).

Capture Mode. A Trigger causes the timer value to be latched into the selected Capture register.

Up/Down Mode. A Trigger causes a count up or down, or a change in counting direction.

Free-Running Mode. Up or Down counting is performed to the full range with no action at End of Count. This is used in Bicapture and Capture Modes.

Monitor Mode. One Capture register follows the contents of the timer.

Autoclear Mode. The timer is reset to 0000h or FFFFh (up or down count respectively) on a trigger. This gives delta time measurement or free running with a modulo of less than 2^{16}.

Biload Mode. The counter is reloaded on an End Of Count condition alternately from the two Load Registers. (PWM output).

BI**Capture Mode.** A Trigger causes the current timer value to be transferred alternately to the two Capture registers. (Pulse width measurement).

MULTIFUNCTION TIMER (Continued)

Parallel Mode. The prescaler output of Timer 0 is internally connected to the input of the prescaler of Timer 1, if this is then set to 00h (= divide by 1), then the two timers may be run in parallel.

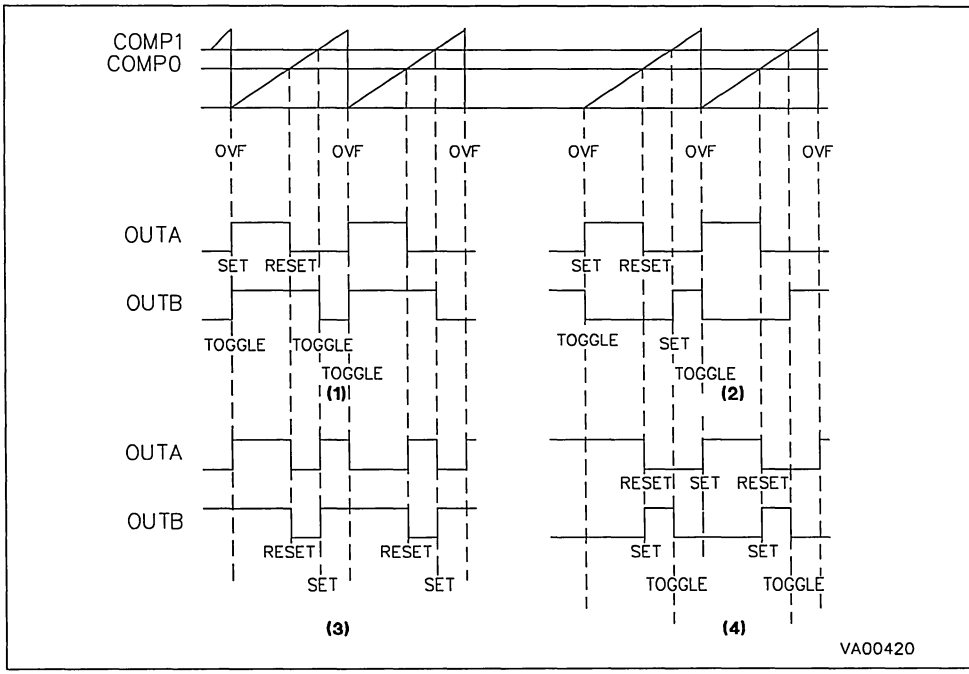
The trigger events may be either caused by software, or an action on the two input pins which may be programmed to respond to rising, falling or both edges of the input. The input modes are selected in the Input Control Register (ICR) as shown in Table 11. This includes the Autodiscriminator mode, which causes the timer to count up or down depending on the phase between the two input edges, such as generated by optical encoders.

The two output pins (available as Alternate Functions) may be programmed through the Output Control Registers OACR and OBCR to be modified (Set, Reset, Toggle or No Operation) on each of Overflow/Underflow (OVF/UNF), Compare on CMP0 valid (CM0), or Compare on CMP1 (COMP1) valid events. This allows repetitive signals such as PWM drive to be output with minimum CPU overhead. Fig 39 shows some typical waveforms available from these signals.

Table 11. Input Pin Function Settings

Input Control Register IN3-IN0 bits	TxINA Input Function	TxINB Input Function
0000	I/O	I/O
0001	I/O	Trigger
0010	Gate	I/O
0011	Gate	Trigger
0100	I/O	Ext.clock
0101	Trigger	I/O
0110	Gate	Ext.clock
0111	Trigger	Trigger
1000	Clock Up	Clock Down
1001	Up/Down	Ext.clock
1010	Trigger Up	Trigger Down
1011	Up/Down	I/O
1100	Autodiscr.	Autodiscr.
1101	Trigger	Ext.clock
1110	Ext.clock	Trigger
1111	Trigger	Gate

Figure 39. Example Output Waveforms



MULTIFUNCTION TIMER (Continued)

The Overflow/Underflow event and the Compare 0 event may also be programmed to give On-chip Event timing signals to trigger other peripheral operations on the ST9036. These are as shown in Table 12

Table 12. ST9036 On-Chip Event Settins

MFT0	A/D Conversion Trigger
MFT1	Handshake Trigger Port

The TxOUTA and TxINA lines for each timer may be connected internally, by setting of the SCx bits of the I/O Connection Register (IOCR).

The Multifunction Timers are enabled for counting by the Counter Enable bit (CEN, TCR.7) of the respective timer unit. When CEN is low, both prescaler and timer are halted. CEN is logically ANDed with the Global Counter Enable bit (GCEN, CICR.7), so that both timers may be started in synchronism, i.e. when the timers are set into Parallel mode, this allows initialization of both Timers before triggering at the same instant.

MFT Interrupts

The Multifunction Timer can generate interrupt requests from 5 different interrupt sources which are grouped into 3 independent groups. The Interrupt Vector has the source of the interrupt group encoded by hardware into the least significant 3 bits of the vector. This allows the programming of the base address to an 8 byte block within the interrupt vector area of the Program Space. The groups and respective addresses are shown in Table 13.

Table 13. MFT Interrupt Vectors

Interrupt Source	Vector Address
COMP0 COMP1	xxxx x110
CAPT0 CAPT1	xxxx x100
Overflow/Underflow	xxxx x000

Each source may be independently masked, in addition all Timer interrupts may be disabled by the Global Timer Interrupt enable (GTIEN, IDMR.7) control bit. If a Timer interrupt on Compare 0 or Capture 0 does not have its corresponding pending bit reset before the next interrupt, then an overrun condition occurs. This condition is flagged in two dedicated overrun bits in the Timer FLAGS register.

MFT DMA Channels

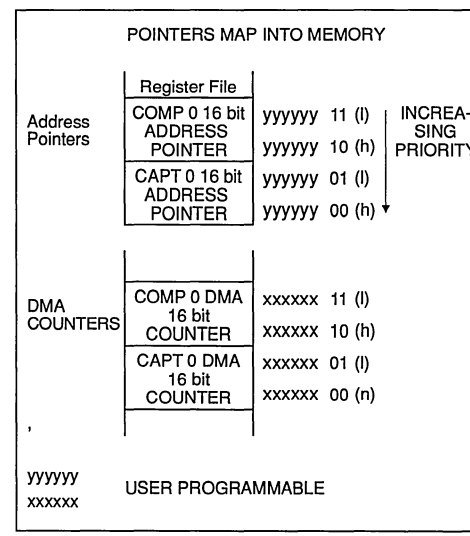
Two independent DMA channels are present within each MFT, associated to the Compare 0 and Capture 0 sources. This allows 16 bit DMA transactions from Register File/Memory to COMP0 registers, and from CAPT0 registers to Register File/Memory. The DMA channels allow the capture of external event timings in memory allowing off-line analysis, and creating of variable pulse width signal trains, as required by the drive of Triacs in certain modes.

The two interrupt mask sources are independently masked by two DMA mask bits, mapped in the IDMR register. The End of Block (EOB) procedures are as described in the INTERRUPT/DMA section.

The DMA counter and address pointer registers share the most significant user-programmable 6 bits for both DMA channels (COMP 0 and CAPT 0), thus the mapping of the counter and address registers use automatic offsets from the base address. The actual mapping changes dependent on whether the Register File or Memory is addressed for the transfer. The offsets are shown in Table 14.

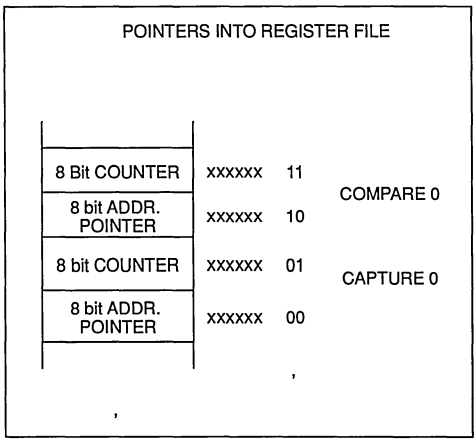
After the transfer of the complete block of data to/from the MFT, the count registers reach the zero

Table 14-1. MFT DMA Address and Counter Registers for Memory DMA Transfers



MULTIFUNCTION TIMER (Continued)

Table 14-2. MFT DMA Address and Counter Registers for register file DMA Transfers



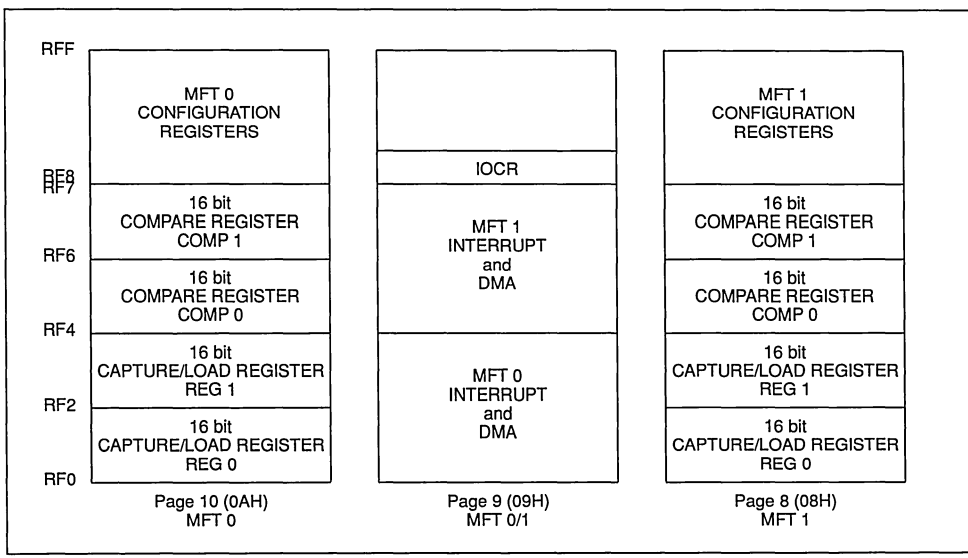
value and an end of block interrupt occurs so that the ST9 may process the new data. In many cases, the time taken to reload the data tables and to re-trigger the DMA action causes speed limitations, especially in those applications requiring a continuous high speed data flow, because of the time consumed by the restore routine. An additional DMA function, the SWAP mode, overcomes this limitation. This is enabled by the setting of the SWEN (IDCR.3) bit. This causes hardware generated signals to replace the user address bit 2 of both the address and counter pointers. The address and counter registers are thus duplicated at an offset of 4 registers. At the End Of Block condition, the EOB interrupt is generated to signal the end of DMA, and the state of pointer address bit 2 toggles state automatically and the new address and count values are used. Thus the ST9 can safely process the previous block of data while the new block is being transferred. This will continue until the SWAP mode is disabled.

A software protection scheme is implemented to prevent non-updated pointer registers from being used if a second EOB interrupt arrives during the servicing of the first. This mechanism locks the state of the DMA mask bit to prevent further transfers from taking place. The user should check for this condition in the EOB routine to ensure that all the DMA transfers are properly serviced.

The control Registers of each MFT occupies 20 registers within the I/O paged area. These are mapped as follows:

In addition the MFT is able to trigger byte DMA transfers in both directions through an I/O port with Handshake (see I/O Handshake and DMA).

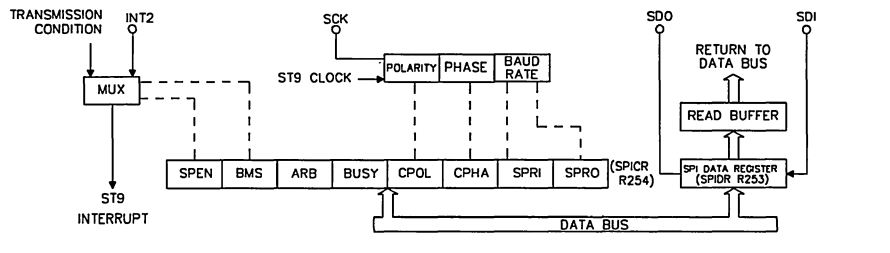
Figure 40. Multifunction Timer Page Maps



SERIAL PERIPHERAL INTERFACE (SPI)

The Serial Peripheral Interface (SPI) is integrated into the Core module of the ST9 and provides a general purpose shift register based peripheral allowing synchronous serial I/O, with special modes allowing compatibility with I^2C-bus and IM-bus Communication standards in addition to the standard serial bus protocol. The SPI uses 3 lines comprising Serial Data Out (SDO), Serial Data In (SDI) and the Synchronous Serial Clock (SCK) which are available as Alternate Functions of I/O pins. Additional I/O pins may act as device selects or IM-bus address ident signals. The functional diagram of the SPI is shown in figure 41.

Figure 41. SPI Functional Diagram



The SPI, when enabled (SPEN, SPICR.7, high), receives input data from the ST9 internal data bus into the SPIDR, and originates the SCK to shift the data serially through SDO (Most Significant bit first) to the slave device which responds by sending data to the master device via the SDI pin. This implies full duplex transmission with both data-out and data-in synchronized with the same clock signal. Thus the byte transmitted is replaced by the byte received, eliminating the need to separate "Tx Empty" and "Rx full" status bits. After the 8 clock cycles have been concluded, the received data in SPIDR is parallel transferred to the read buffer and data becomes available for the ST9036 during the next read cycle of SPIDR. The BUSY bit (SPICR.4) is set when transmission is in progress, this allows the user to monitor the status of the SPI by polling of this bit.

The SPI can operate only in master mode, i.e. the clock is always generated by the ST9036, however the SCK polarity and phase can be programmed to suit all peripheral requirements (figure 42). This, together with the 4 programmable bit rates (divided from the INTCLK, Table 15), provide the large flexibility in handling different protocols.

SERIAL PERIPHERAL INTERFACE (SPI) (Continued)

Figure 42. SPI Data and Clock Timing

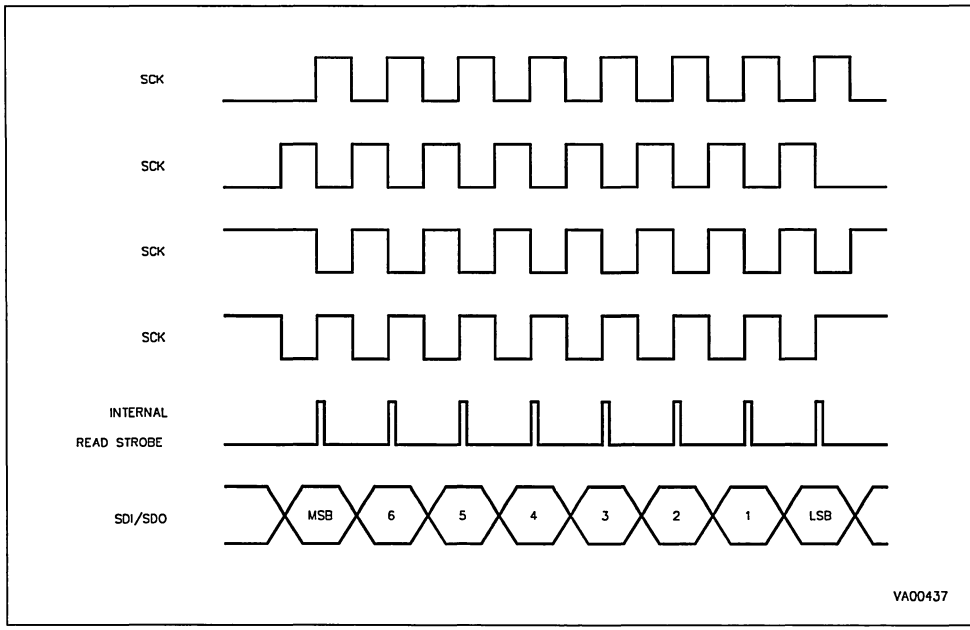


Table 15. SPI Rate Selection

SPR1	SPR0	Clock Divider	SCK Frequency (INTCLK = 12 MHz)
0	0	8	1500 KHz (T= 0.67 µs)
0	1	16	750 KHz (T= 1.33 µs)
1	0	12	93.75 KHz (T= 10.66 µs)
1	1	256	46.87 KHz (T= 21.33 µs)

I^2C-bus Compatibility

The SPI includes additional circuitry to enable the use of external I^2C-bus peripherals. The I^2C-bus mode is a 2 wire bus while the SPI operates with 3 wires, however wire-ANDing SDO and SDI gives the required signalling, while setting the BMS bit causes the enabling of the special I^2C-bus features: Clock Slowdown by external devices and Arbitration Lost detection. This mode also affects the Interrupt sources as shown in the next section.

SPI Interrupts

The SPI, when enabled, uses the INT2 external interrupt channel source, using the priority selected for INT2 within the External Interrupt Priority registers. The INT2 mask bit should be set and INT2 pending bit reset before enabling the SPI through SPEN. The BMS (SPICR.6) and SPEN bits select the SPI internal interrupt source as shown in Table 16.

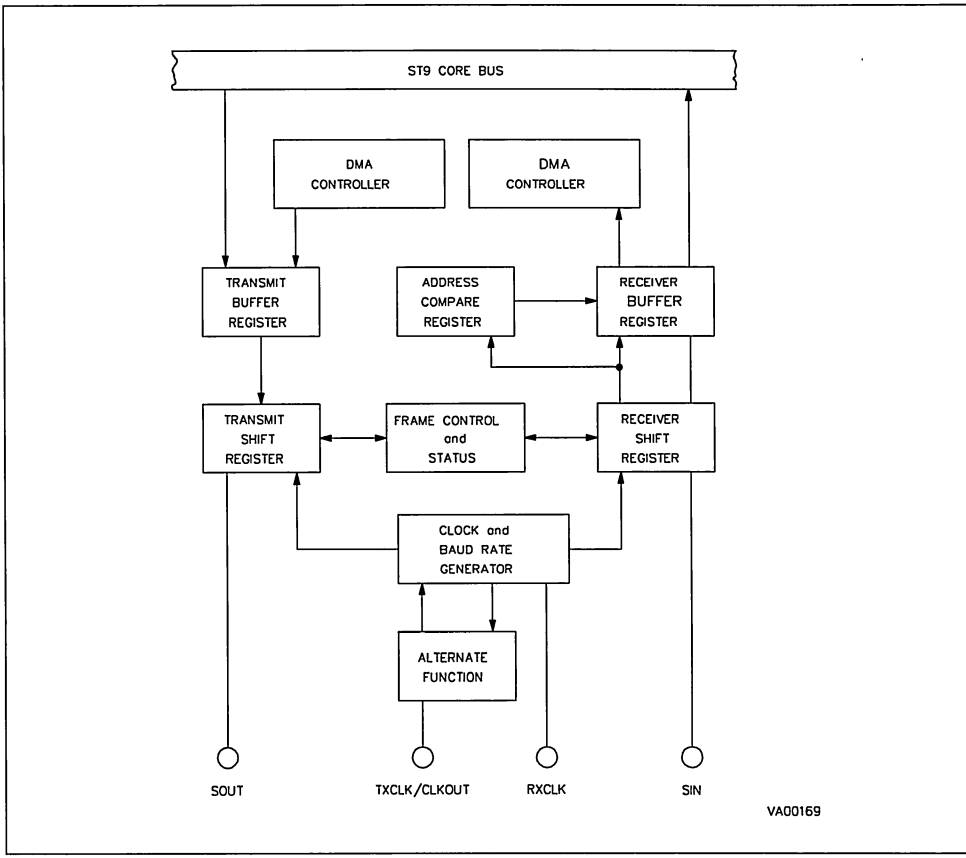
Table 16. SPI Interrupt Sources

SPEN	BMS	Interrupt Source
0	0	External channel INT2
0	1	S-BUS/I^2C bus start or stop condition
1	X	End of one byte transmission

SPI Registers

The two registers controlling the SPI are located in I/O page 0, the Data Register, SPIDR, at R253 and the control register, SPICR, at R254.

Figure 43. SCI Functional Block Diagram



SERIAL COMMUNICATIONS INTERFACE

Function

The Serial Communications Interface (SCI) of the ST9036 offers a means of full-duplex serial data transfer to a wide range of external equipment with its fully programmable character format control for asynchronous and byte synchronous serial I/O, integral Baud Rate Generator, giving a maximum baud rate of 375K Baud in Asynchronous mode (Internal Clock), and two DMA channels for transparent transmission and reception of characters. Support is also present in hardware for Line Break Detection and generation, character search, network interfacing with 9th bit Address logic, and Local Loop Back and Auto echo modes for Self-Test. The control registers for the SCI exist within one I/O page within the I/O page group.

Character Formats

When used for asynchronous character transmission and reception, the character format may be changed (through the Character Control Register CHCR) to suit external equipment requirements. This is summarized in figure 44.

The baud rate clock for asynchronous mode should be set to the ÷16 Mode and the frequency of the clock input (from an external source or the internal baud-rate generator output) set to suit this.

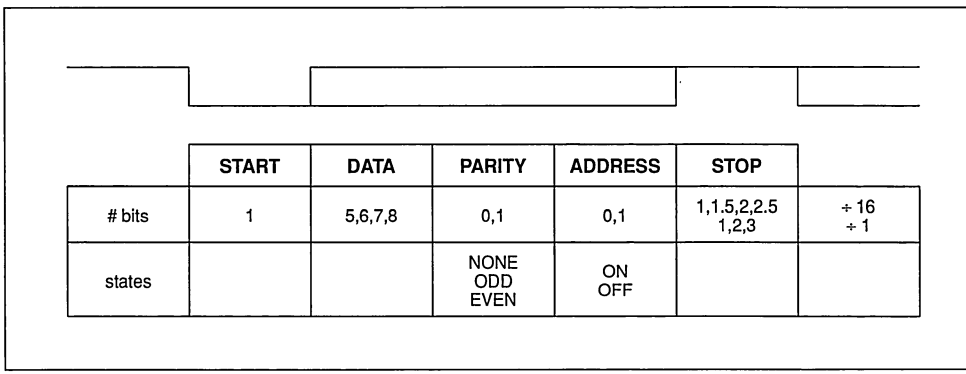
SERIAL COMMUNICATION INTERFACE (Continued)

This format control is also available for the byte synchronous mode (Clock divider set to ÷1), when the data and clock are output in synchronism, the data being sampled once per clock period (figure 45). For a second synchronous mode, CLKOUT is activated only for the data section of the word (figure 46) on serial data output, and input data is latched on the rising edge of the external synchronised clock input on the RXCLK pin. This mode may be used to access external synchronous peripherals.

The Address bit/D9 is optional and may be added to any word format, it is commonly used in network or machine control applications. When enabled (AB, CHCR.4 = 1), an address or ninth data bit can be added to a transmitted word by setting the Set Address bit (SA, IDPR.5). This is then appended to the next word entered into the (empty) Transmitter Buffer Register and then cleared by hardware. On character input an Address Bit set can indicate that the data preceding the bit is an address which may be compared in hardware with the value in the Address Compare Register (ACR) to generate an Address Match interrupt when equal.

The Address bit and Address Comparison Register can also be combined to generate an Address Interrupt in 4 modes to suit different protocols, based upon the status of the Address Mode Enable bit (AMEN, IDPR.7) and the Address Mode bit (AM, CHCR.7) as shown in Table 17.

Figure 44. SCI Character Format



	START	DATA	PARITY	ADDRESS	STOP	
# bits	1	5,6,7,8	0,1	0,1	1,1.5,2,2.5 1,2,3	÷ 16 ÷ 1
states			NONE ODD EVEN	ON OFF		

Figure 45. Byte Synchronous Output

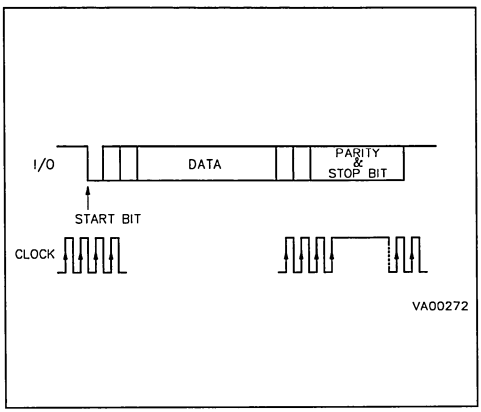
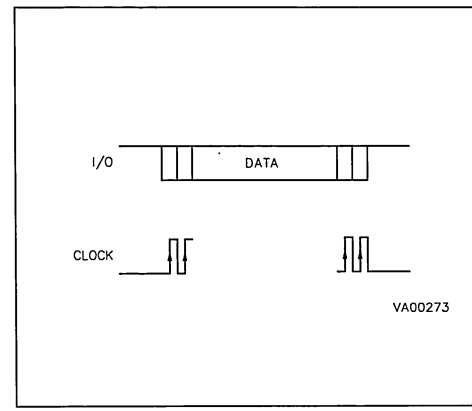


Figure 46. Serial Expansion Mode



SERIAL COMMUNICATION INTERFACE (Continued)

Table 17. Address Interrupt Modes

If 9th Data Bit = 1
If Character Match
If Character Match and 9th Data Bit = 1
If Character Match on Word Immediately Following Break

The character match Address Interrupt mode may be used as a powerful character search mode, giving an interrupt on reception of a predetermined character e.g. Carriage Return or End of Block codes.

The Line Break condition is fully supported for both transmission and detection. Line Break is sent by setting the SET_BREAK bit (SB, IDPR.6). This causes the transmitter output to be held low (after all buffered data has been transmitted) for a minimum of one complete word length and until the SB bit is Reset.

SCI Interrupts

The SCI is able to generate interrupts from multiple sources. Receive interrupts include data pending, receive errors (overrun, framing and parity), address or break pending and transmit interrupts are software selectable for either the Transmit Holding Register Empty (HSN, IMR.7 = "1") or for the Transmit Shift Register Empty (HSN = "0"). Interrupt sources are indicated by the Interrupt pending bits, shown in Table 18. These bits should be reset by the programmer during the Interrupt Service routine.

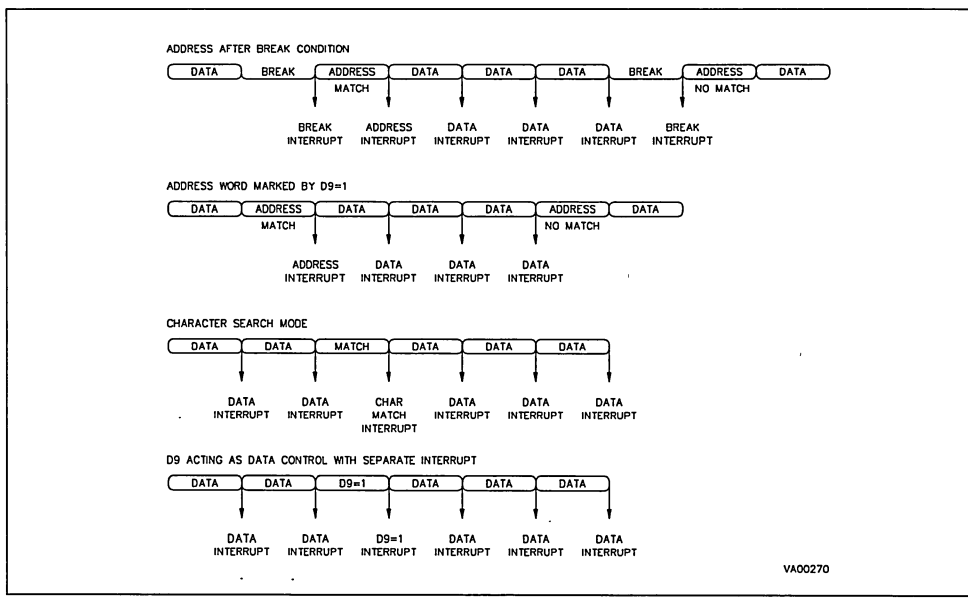
Table 18. SCI Interrupt Vector

Interrupt Source	Vector Address
Transmitter Buffer or Shift Register Empty/ Transmit DMA end of Block	xxx x110
Received Ready/ Receive DMA end of Block	xxxx x100
Break Detector Address Word Match	xxxx x001
Receiver Error	xxxx x000

When DMA is active the Receive Data Pending bit (RXDP, ISR.2), and the Transmit status bit interrupt sources are replaced by the DMA End Of Block Interrupt sources for transmit and receive, respectively.

Typical Usage of the Interrupts provided by the SCI are show in figure 47.

Figure 47. SCI Interrupt Typical Usage



SERIAL COMMUNICATION INTERFACE (Continued)

The SCI interrupts have an internal priority structure (Table 19) in order to resolve simultaneous events.

The four major levels of interrupt are encoded in hardware to provide two bits of the interrupt vector register, allowing the position of the block of pointer vectors to be resolved to a block size of 8 bytes.

Table 19. SCI Interrupt Internal Priority

Receive DMA Request	Highest Priority
Transmit DMA Request	Lower Priority
Receive Interrupt	
Transmit Interrupt	

SCI DMA

Two DMA channels are associated with the SCI, for transmit and for receive. These follow the register scheme as described in the DMA section. It should be noted that, after initializing the DMA counter and pointer registers and enabling DMA, data transmission is triggered by a character written into the Transmit Holding register. The DMA End Of Block Interrupts generated on completion of the DMA transfer take the place of the normal transmit and receive character interrupt vectors.

SCI Clock Generation

The communication bit frequency of the SCI transmitter and receiver sections can be provided from the integral Baud Rate Generator (allowing a maximum asynchronous bit rate of 350k Baud) or from external sources (maximum bit rate 175k Baud). This clock is divided by 16 for asynchronous mode (CD, CCR.3, = "0"), or divided by 1 for synchronous modes (CD = "1").

External Clock Sources.

The External Clock input pin TXCLK may be programmed in Alternate function by bits TXCLK (CCR.7) and OCLK (CCR.6) to be: the transmit clock input (respecting the %16 and %1 timing requirements), to act as the output of the Baud Rate Generator (allowing an external divider circuit to provide the receive clock for split rate transmit and receive e.g. 1200/75 baud), or to be CLKOUT, the clock output for the synchronous mode. Receive clock input via RXCLK Alternate function is enabled by the XRX bit CCR.5, this input should be set according to the setting of the CD bit.

Baud Rate Generator.

The integral Baud Rate Generator is a 16 bit divide by n circuit of the Internal Clock INTCLK. Thus INTCLK should be chosen to provide a suitable frequency for division by the Baud Rate Generator to give the required transmit and receive bit rates. Suitable INTCLK frequencies and the divider values for standard Baud rates are shown in Table 20.

The act of writing to either of the two registers comprising the 16 bit divider causes a reset of the SCI, allowing initialization of the SCI settings before the writing of the other Baud Rate Generator register.

Self Test

Testing of the communications channel may be performed using the facilities of the SCI. Auto Echo mode (SCI SOUT disconnected, SIN pin internally connected to SOUT pin) and Loopback mode (SCI transmitter and receiver sections disconnected from SOUT and SIN pins and directly connected internally) may be used individually or together.

SERIAL COMMUNICATION INTERFACE (Continued)

Table 20. SCI Baud Rate Generator Divider Values

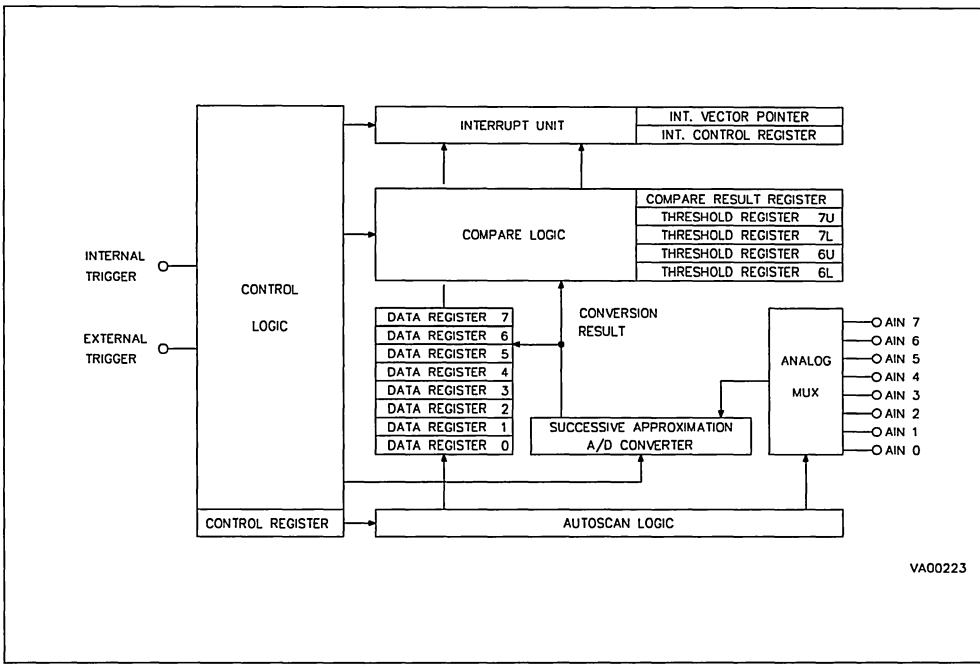
INTCLK: 7680.000 KHz							
Baud Rate	Clock Factor	Desired Freq (kHz)	Divisor		Actual Baud Rate	Actual Freq (kHz)	Deviation
			Dec	Hex			
50.00	16 X	0.80000	9600	2580	50.00	0.80000	0.0000%
75.00	16 X	1.20000	6400	1900	75.00	1.20000	0.0000%
110.00	16 X	1.76000	4364	110C	109.99	1.75985	0.0083%
300.00	16 X	4.80000	1600	0640	300.00	4.80000	0.0000%
600.00	16 X	9.60000	800	0320	600.00	9.60000	0.0000%
1200.00	16 X	19.20000	400	0190	1200.00	19.20000	0.0000%
2400.00	16 X	38.40000	200	00C8	2400.00	38.40000	0.0000%
4800.00	16 X	76.80000	100	0064	4800.00	76.80000	0.0000%
9600.00	16 X	153.60000	50	0032	9600.00	153.60000	0.0000%
19200.00	16 X	307.20000	25	0019	19200.00	307.20000	0.0000%
38400.00	16 X	614.40000	13	000D	36923.08	590.76923	3.8462%
76800.00	16 X	1228.80000	6	0006	80000.00	1280.00000	4.1667%
INTCLK: 11059.20 kHz							
Baud Rate	Clock Factor	Desired Freq (kHz)	Divisor		Actual Baud Rate	Actual Freq (kHz)	Deviation
			Dec	Hex			
50.00	16 X	0.80000	13824	3600	50.00	0.80000	0.0000%
75.00	16 X	1.20000	9216	2400	75.00	1.20000	0.0000%
110.00	16 X	1.76000	6284	188C	109.99	1.75990	0.0058%
300.00	16 X	4.80000	2304	0900	300.00	4.80000	0.0000%
600.00	16 X	9.60000	1152	0480	600.00	9.60000	0.0000%
1200.00	16 X	19.20000	576	0240	1200.00	19.20000	0.0000%
2400.00	16 X	38.40000	288	0120	2400.00	38.40000	0.0000%
4800.00	16 X	76.80000	144	0090	4800.00	76.80000	0.0000%
9600.00	16 X	153.60000	72	0048	9600.00	153.60000	0.0000%
19200.00	16 X	307.20000	36	0024	19200.00	307.20000	0.0000%
38400.00	16 X	614.40000	18	0012	38400.00	614.40000	0.0000%
76800.00	16 X	1228.80000	9	0009	76800.00	1228.80000	0.0000%

ANALOG TO DIGITAL CONVERTER

The ST9036 Analog to Digital Converter (A/D) is comprised of an 8 channel multiplexed input selector and a Successive Approximation converter. The conversion time is a function of the INTCLK frequency; for the maximum 12MHz clock rate, conversion of the selected channel requires 11µs. This time also includes the 3µs of the integral Sample and Hold circuitry, which minimizes need for external components. The resolution of the converted channel is 8 bits ±1/2 LSB between the Analog V_{SS} and V_{DD} references which occupy two pins of the ST9036 (AV_{SS} and AV_{DD} respectively). These allow the full 256 bit resolution to apply over a reduced input range such as provided by various sensors and allows the best supply noise rejection.

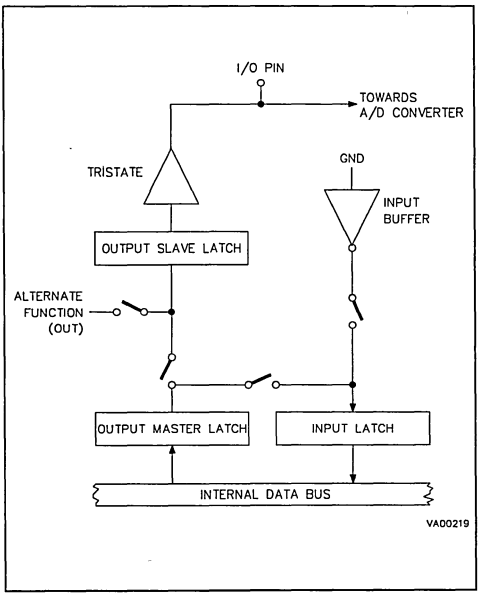
The input Analog channel is selected by using the Alternate Function setting as shown in the I/O ports section. The I/O bit structure of the port connected to the A/D converter (Port 4) is modified as shown in figure 49 to prevent the Analog voltage present at the I/O pin from causing high power dissipation across the input buffer. Un-selected analog channels should also be maintained in the Alternate function mode for this reason. A Power Down mode is available for applications which require low power dissipation, this is selected by setting to zero the POW bit (CLR.2) which turns off all Analog functions within the A/D converter.

Figure 48. A/D Block Diagram



ANALOG DIGITAL CONVERTER (Continued)

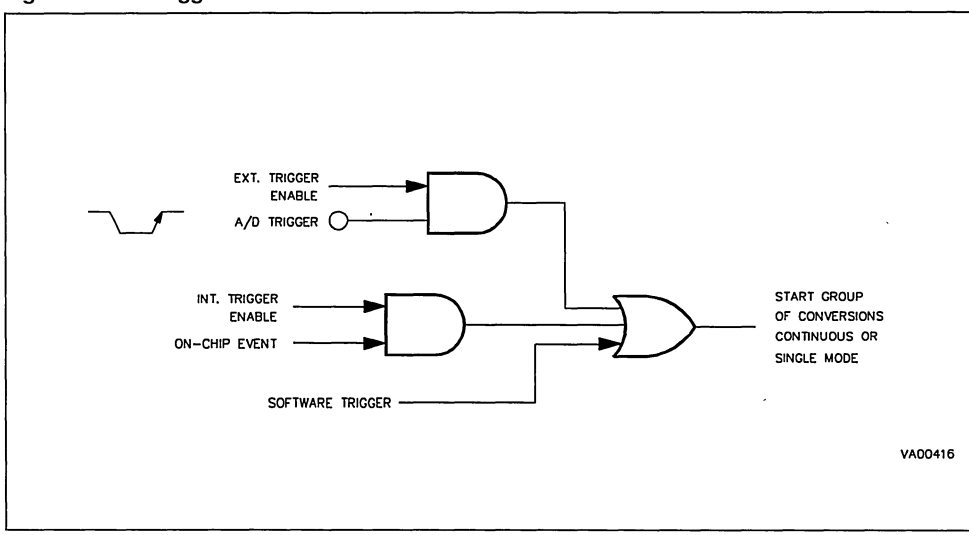
Figure 49. A/D Input Configuration



Conversion

Each of the input Analog channels (AIN0-7) can be converted singly or continuously. In single mode (CONT, CLR.1, = "0") conversions are triggered by setting the Start/Stop bit ST (CLR.0), this is reset by hardware at the end of a group of conversions and conversion stops. The Autoscan mode (CONT = "1") converts each input channel in sequence, starting from the channel number selected in the Start Conversion Address (SC1-3) bits and increasing to channel 7 (AIN7), repeating so that the data registers will be maintained with the latest converted result. Conversion start is triggered by internal or external events. An external trigger (enabled by EXTG, CLR.4, = "1") is caused by a pulse on the ADTRG pin available as an Input Alternate Function. This should have a minimum length of 80 nS and of a period greater than the conversion time. The Internal trigger is enabled by setting INTG, CLR.3, to "1" (this is ORed with EXTG to prevent hardware conflicts, but the correct procedure is to enable only one source at a time), in this case triggering is either by setting the ST bit by software or by enabling the ON-CHIP EVENT signal from the TIMER module.

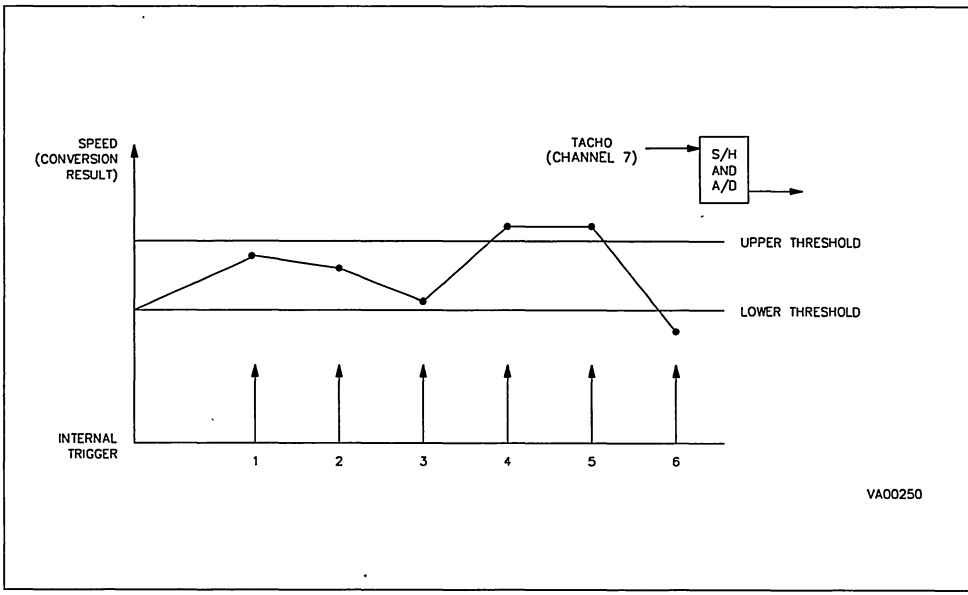
Figure 50. A/D Trigger Sources



ANALOG DIGITAL CONVERTER (Continued)

The resulting data from the converted Analog channel AINx is stored in the appropriate Data Register DxR. Two channels AIN6 and AIN7 have a special feature known as the Analog Watchdog, by the use of two Threshold Registers for each channel. The Upper, (HT6R, HT7R), and lower, (LT6R, LT7R), registers contain user preset values. These values are automatically compared to the value in the Data Registers D6R and D7R following each new conversion. If the resulting data is less than the corresponding Lower Threshold Register, or higher than the contents of the corresponding Upper Threshold Register, then an interrupt may be generated. This hardware feature minimizes analog monitoring overhead and is particularly useful in motor control applications as shown in figure 51.

Figure 51. Analog Watchdog Used in Motor Speed Control



A/D Interrupts

The ST9036 A/D converter provides two interrupt sources, End of Conversion and an Analog Watchdog Request. The interrupt vector register (IVR) provides 1 bit automatically generated in hardware to follow the interrupt source, allowing the user to select the base address of a four byte area of the interrupt vector table in which to store the A/D Interrupt Service Routines. The Analog Watchdog Request requires the user to poll within the Compare Result Register (CRR) to determine which of the four thresholds has been exceeded, the threshold status bits should be reset by software in the service routine. The interrupt pending flags, ECV (End of Conversion, ICR.7) and AWD (Analog Watchdog, ICR.6) should also be reset by the User in the Interrupt service routine before the return.

The ST9036 Analog to Digital converter occupies I/O page 63 (Group F).

SOFTWARE DESCRIPTION

Addressing Modes

The ST9036 offers a wide variety of addressing modes and combinations to facilitate full and rapid access to the address spaces while reducing program length. Register addressing (using the working register group mechanism or directly addressed) can be used as 8 or 16 bit values for data or indirect addressing into the memory spaces or the Register File. The selection between Program Memory and Data Memory is performed through the P/$\overline{D}$ bit in the FLAG Register, all subsequent actions on the memory space will affect the selected map only, apart from the memory map to memory map post-increment addressing mode which allows the map to be specified as part of the instruction for both destination and source operands. Apart from the immediate data and condition codes all operands are expressed as register file or memory addresses.

The available addressing modes, with the ST9 macro-assembler notation, are shown in Table 21.

Combinations Of Available Addressing Modes

Table 22 describes the addressing modes available for the register file and the memory (both as a destination and as a source) for the two operand arithmetic, logic or load instructions.

Table 21. Addressing Mode

Addressing Mode	Notation	
Immediate Data	#N	#NN
Register Direct	R;r	RR;rr
Register Indirect	(R)	(r)
Register Indexed	N(r)	N(rr)
Memory Direct	NN	
Memory Indirect	(RR)	(rr)
Memory Indirect with Post-Increment	(rr)+	
Memory Indirect with Pre-Decrement	-(rr)	
Memory Indexed with Immediate Short Offset	N(rr)	
Memory Indexed with Immediate Long Offset	NN(rr)	
Memory Indexed with Register Offset	rr(rr)	
Memory Indirect Post-Increment to Indirect Register Post-Increment	(rr)+	(r)+
Memory Map to Memory Map both with Post-Increment	(rr)+	(r)+
Bit Address	r.b, (rr).b	

Legend:
N = 8 bit Value
NN = 16 bit Value or Address
r = Working Register
R = Directly Addressed Register
( ) = Indirect Addressing
( )+ = Indirect with Post-Increment
-( ) = Indirect with Pre-Decrement
.b = Bit Number (0 to 7)

Table 22. Addressing Mode Permutation for Instructions

Two Operand Arithmetic and Logic Instructions	
Destination	**Source**
Register Direct	Register Direct
Register Direct	Register Indirect
Register Direct	Memory Indirect
Register Direct	Memory Indexed
Register Direct	Memory Indirect with Post- Increment
Register Direct	Memory Indirect with Pre- Decrement
Register Direct	Memory Direct
Register Indirect	Register Direct
Memory Indirect	Register Direct
Memory Indexed	Register Direct
Memory Indirect with Post- Increment	Register Direct
Memory Indirect with Pre- Decrement	Register Direct
Memory Direct	Register Direct

SOFTWARE DESCRIPTION (Continued)

Table 22. Addressing Mode Permutation for Instructions (Continued)

Two Operand Load Instructions	
Destination	**Source**
Register Direct	Register Direct
Register Direct	Register Indirect
Register Direct	Register Indexed
Register Direct	Memory Indirect
Register Direct	Memory Indexed
Register Direct	Memory Indirect with Post- Increment
Register Direct	Memory Indirect with Pre- Decrement
Register Direct	Memory Direct
Register Indirect	Register Direct
Register Indexed	Register Direct
Memory Indirect	Register Direct
Memory Indexed	Register Direct
Memory Indirect with Post- Increment	Register Direct
Memory Indirect with Pre- Decrement	Register Direct
Memory Direct	Register Direct
Two Operand Arithmetic and Logic Instructions	
Destination	**Source**
Register Direct	Immediate
Memory Direct	Immediate
Memory Indirect	Immediate
Two Operand Load Instructions	
Destination	**Source**
Register Direct	Immediate
Memory Direct	Immediate
Memory Indirect	Immediate
Long Indexed Memory (1)	Immediate

Table 22 . Addressing Mode Permutation for Instructions (Continued)

Two Operand Arithmetic, Logic & Load Instructions	
Destination	**Source**
Memory Indirect	Memory Indirect
Two Operand Load Instructions (2)	
Destination	**Source**
Register Indirect with Post- Increment	Memory Indirect with Post- Increment
Memory Indirect with Post- Increment	Register Indirect with Post- Increment
Memory Indirect with Post- Increment	Memory Indirect with Post- Increment

Notes:
1. Load Word only
2. Load Byte only

Instruction Set

The ST9036 instruction set consists of 87 instruction types functionally divided into eight groups as in Table 23, they are:

- Load (two operands)
- Arithmetic & Logic (two operands)
- Arithmetic Logic and Shift (one operand)
- Stack (one operand)
- Multiply & Divide (two operands)
- Boolean (one or two operands)
- Program Control (zero to three operands)
- Miscellaneous (zero to two operands)

The wide range of instructions facilitates the full use of the register file and address spaces, reducing execution times, while the register pointers mechanism allows an unmatched code efficiency and ultrafast context switching. A particularly notable feature is the comprehensive "Any Bit, Any Register" (ABAR) addressing capability of the Boolean instructions.

The ST9036 can operate with a wide range of data lengths from single bit, 4-bit nibbles which can be in the form of Binary Coded Decimal (BCD) digits, 8-bit bytes and 16-bit words. The summary on Table 23 shows the instructions belonging to each group and the number of operands required for each. The source operand is "src", "dst" is the destination operand, and "cc" is the condition code selection.

SOFTWARE DESCRIPTION (Continued)

Table 23. Instruction Set Summary

Load Instructions (Two Operands)								
Mnemonic	**Operand**	**Instruction**	**Flags**					
			C	**Z**	**S**	**V**	**D**	**H**
LD LDW	dst, src dst, src	Load Load Word	– –	– –	– –	– –	– –	– –
Arithmetic and Logic (Two Operands)								
Mnemonic	**Operand**	**Instruction**	**Flags**					
			C	**Z**	**S**	**V**	**D**	**H**
ADD ADDW	dst, src dst, src	Add Add Word	Δ Δ	Δ Δ	Δ Δ	Δ Δ	0 ?	Δ ?
ADC ADCW	dst, src dst, src	Add with Carry Add Word with Carry	Δ Δ	Δ Δ	Δ Δ	Δ Δ	0 ?	Δ ?
SUB SUBW	dst, src dst, src	Subtract Subtract Word	Δ Δ	Δ Δ	Δ Δ	Δ Δ	1 ?	Δ ?
SBC SBCW	dst, src dst, src	Subtract with Carry Subtract Word with Carry	Δ Δ	Δ Δ	Δ Δ	Δ Δ	1 ?	Δ ?
AND ANDW	dst, src dst, src	Logical AND Logical Word AND	– –	Δ Δ	Δ Δ	0 0	– ?	– ?
OR ORW	dst, src dst, src	Logical OR Logical Word OR	– –	Δ Δ	Δ Δ	0 0	– –	– –
XOR XORW	dst, src dst, src	Logical Exclusive OR Logical Word Exclusive OR	– –	Δ Δ	Δ Δ	0 0	– –	– –
CP CPW	dst, src dst, src	Compare Compare Word	Δ Δ	Δ Δ	Δ Δ	Δ Δ	– –	– –
TM TMW	dst, src dst, src	Test Under Mask Test Word Under Mask	– –	Δ Δ	Δ Δ	0 0	– –	– –
TCM TCMW	dst, src dst, src	Test Complement Under Mask Test Word Complement Under Mask	– –	Δ Δ	Δ Δ	0 0	– –	– –

Legend :
0 = Bit set to zero
1 = Bit set to one
Δ = Bit affected
? = Bit status undefined
– = Bit not affected

SOFTWARE DESCRIPTION (Continued)

Table 23. Instruction Set Summary (Continued)

Arithmetic Logic and Shift (One Operand)									
Mnemonic	**Operand**	**Instruction**	**Flags**						
			C	**Z**	**S**	**V**	**D**	**H**
INC	dst	Increment	–	Δ	Δ	Δ	–	–
INCW	dst	Increment Word	–	Δ	Δ	Δ	–	–
DEC	dst	Decrement	–	Δ	Δ	Δ	–	–
DECW	dst	Decrement Word	–	Δ	Δ	Δ	–	–
SLA	dst	Shift Left Arithmetic	Δ	Δ	Δ	0	0	Δ
SLAW	dst	Shift Word Left Arithmetic	Δ	Δ	Δ	0	?	?
SRA	dst	Shift Right Arithmetic	Δ	Δ	Δ	Δ	0	Δ
SRAW	dst	Shift Word Right Arithmetic	Δ	?	Δ	0	–	–
RRC	dst	Rotate Right through Carry	Δ	Δ	Δ	Δ	–	–
RRCW	dst	Rotate Word Right through Carry	Δ	?	Δ	Δ	–	–
RLC	dst	Rotate Left through Carry	Δ	Δ	Δ	Δ	–	–
RLCW	dst	Rotate Word Left through Carry	Δ	?	Δ	Δ	–	–
ROR	dst	Rotate Right	Δ	Δ	Δ	Δ	–	–
ROL	dst	Rotate Left	Δ	Δ	Δ	Δ	–	–
CLR	dst	Clear	–	–	–	–	–	–
CPL	dst	Complement Register	–	Δ	Δ	0	–	–
SWAP	dst	Swap Nibbles	?	Δ	Δ	?	–	–
DA	dst	Decimal Adjust	Δ	Δ	Δ	?	–	–
Stack Instructions (One Operand)									
Mnemonic	**Operand**	**Instruction**	**Flags**						
			C	**Z**	**S**	**V**	**D**	**H**
PUSH	src	Push on System Stack	–	–	–	–	–	–
PUSHW	src	Push Word on System Stack	–	–	–	–	–	–
PEA	src	Push Effective Address on System Stack	–	–	–	–	–	–
POP	dst	Pop from System Stack	–	–	–	–	–	–
POPW	dst	Pop Word from System Stack	–	–	–	–	–	–
PUSHU	src	Push on User Stack	–	–	–	–	–	–
PUSHUW	src	Push Word on User Stack	–	–	–	–	–	–
PEAU	src	Push Effective Address on User Stack	–	–	–	–	–	–
POPU	dst	Pop from User Stack	–	–	–	–	–	–
POPUW	dst	Pop Word from User Stack	–	–	–	–	–	–

SOFTWARE DESCRIPTION (Continued)

Table 23. Instruction Set Summary (Continued)

Multiply and Divide Instructions (Two Operands)								
Mnemonic	**Operand**	**Instruction**	**Flags**					
			C	**Z**	**S**	**V**	**D**	**H**
MUL	dst, src	Multiply 8x8	Δ	Δ	Δ	Δ	0	?
DIV DIVWS	dst, src	Divide 16/8 Divide Word Stepped 32/16	1 ?	Δ ?	Δ ?	? ?	1 ?	? ?
Boolean Instructions (Two Operands)								
Mnemonic	**Operand**	**Instruction**	**Flags**					
			C	**Z**	**S**	**V**	**D**	**H**
BLD	dst, src	Bit Load	–	–	–	–	–	–
BAND	dst, src	Bit AND	–	–	–	–	–	–
BOR	dst, src	Bit OR	–	–	–	–	–	–
BXOR	dst, src	Bit Exclusive OR	–	–	–	–	–	–
Boolean Instructions (One Operand)								
Mnemonic	**Operand**	**Instruction**	**Flags**					
			C	**Z**	**S**	**V**	**D**	**H**
BSET	dst	Bit Set	–	–	–	–	–	–
BRES	dst	Bit Reset	–	–	–	–	–	–
BCPL	dst	Bit Complement	–	–	–	–	–	–
BTSET	dst	Bit Test and Set	–	Δ	Δ	0	–	–
Program Control Instructions (Three Operands)								
Mnemonic	**Operand**	**Instruction**	**Flags**					
			C	**Z**	**S**	**V**	**D**	**H**
CPJFI	dst, src	Compare and Jump on False, Otherwise Post Increment	–	–	–	–	–	–
CPJTI	dst, src	Compare and Jump on True, Otherwise Post Increment	–	–	–	–	–	–

SOFTWARE DESCRIPTION (Continued)

Table 23. Instruction Set Summary (Continued)

Program Control Instructions (Two Operands)									
Mnemonic	**Operand**	**Instruction**	**Flags**						
			C	**Z**	**S**	**V**	**D**	**H**
BTJF	dst, src	Bit Test and Jump if False	–	–	–	–	–	–
BTJT	dst, src	Bit Test and Jump if True	–	–	–	–	–	–
DJNZ	dst, src	Decrement a Working Register and Jump if Not Zero	–	–	–	–	–	–
DWJNZ	dst,src	Decrement a Register Pair and Jump if Not Zero	–	–	–	–	–	–
Program Control Instructions (One Operand)									
Mnemonic	**Operand**	**Instruction**	**Flags**						
			C	**Z**	**S**	**V**	**D**	**H**
JR	cc, dst	Jump Relative if Condition is Met	–	–	–	–	–	–
JP	cc, dst	Jump if Condition is Met	–	–	–	–	–	–
JP	dst	Unconditional Jump	–	–	–	–	–	–
CALL	dst	Unconditional Call	–	–	–	–	–	–
Program Control Instructions (No Operand)									
Mnemonic	**Operand**	**Instruction**	**Flags**						
			C	**Z**	**S**	**V**	**D**	**H**
RET		Return from Subroutine	–	–	–	–	–	–
IRET		Return from Interrupt	Δ	Δ	Δ	Δ	Δ	Δ
WFI		Stop Program Execution and Wait Next Enabled Interrupt. If a DMA request is present the CPU executes the DMA service routine and returns to WFI state.	–	–	–	–	–	–
HALT		Stop Program Execution until RESET	–	–	–	–	–	–
Miscellaneous (Two Operands)									
Mnemonic	**Operand**	**Instruction**	**Flags**						
			C	**Z**	**S**	**V**	**D**	**H**
XCH	dst, src	Exchange Registers	–	–	–	–	–	–

SOFTWARE DESCRIPTION (Continued)

Table 23. Instruction Set Summary (Continued)

Miscellaneous (One Operand)								
Mnemonic	**Operand**	**Instruction**	**Flags**					
			C	**Z**	**S**	**V**	**D**	**H**
SRP	src	Set Register Pointer Long (16 Working Registers)	–	–	–	–	–	–
SRP0	src	Set Register Pointer 0 (8 LSB Working Registers)	–	–	–	–	–	–
SRP1	src	Set Register Pointer 1 (8 MSB Working Registers)	–	–	–	–	–	–
SPP	src	Set Page Pointer	–	–	–	–	–	–
EXT	src	Sign Extend	–	–	–	–	–	–
Miscellaneous (No Operand)								
Mnemonic	**Operand**	**Instruction**	**Flags**					
			C	**Z**	**S**	**V**	**D**	**H**
EI		Enable Interrupts	–	–	–	–	–	–
DI		Disable Interrupts	–	–	–	–	–	–
SCF		Set Carry Flag	1	–	–	–	–	–
RCF		Reset Carry Flag	0	–	–	–	–	–
CCF		Complement Carry Flag	Δ	–	–	–	–	–
SPM		Select Program Memory	–	–	–	–	–	–
SDM		Select Data Memory	–	–	–	–	–	–
NOP		No Operation	–	–	–	–	–	–

Processor Flags

An important aspect of any single chip microcontroller is the ability to test data and make the appropriate action based on the results. In order to provide this facility, register 231 in the Register File is used as a Flag Register. Six bits of this register are used as the following flags:

C - Carry

Z - Zero

S - Sign

V - Overflow

D - Decimal Adjust

H - Half Carry

One of the two remaining bits in the flag register is available to the user (bit 1, F1). Bit 0 is the Program/Data Memory selector bit and is operated on directly by the hardware within the ST902X. The P/$\overline{D}$ pin will follow the status of this bit.

Condition Codes. Flags C, Z, S, and V control the operation of the "conditional" Jump instructions. Table 24 shows the condition codes and the flag settings affecting the jump.

SOFTWARE DESCRIPTION (Continued)

Table 24. Condition Codes Summary

Mnemonic Code	Meaning	Flag Setting
F	Always False	—
T	Always True	—
C	Carry	C = 1
NC	No Carry	C = 0
Z	Zero	Z = 1
NZ	No Zero	Z = 0
PL	Plus	S = 0
MI	Minus	S = 1
OV	Overflow	V = 1
NOV	No Overflow	V = 0
EQ	Equal	Z = 1
NE	Not Equal	Z = 0
GE	Greater Then or Equal	(S xor V) = 0
LT	Less Than	(S xor V) = 1
GT	Greater Than	(Z or (S xor V)) = 0
LE	Less Than or Equal	(Z or (S xor V)) = 1
UGE	Unsigned Greater Than or Equal	C = 0
UL	Unsigned Less Than	C = 1
UGT	Unsigned Greater Than	(C = 0 and Z = 0) = 1
ULE	Unsigned Less Than or Equal	(C or Z) = 1

POWERFUL DEVELOPMENT ENVIRONMENT

ST9 Software Tools

The following Software Tools are available for MS-DOS, SUN-3 and SUN-4 operating systems:

AST9 high-level macro assembler with predefinited macro instructions (IF/ELSE, WHILE, DO, LOOP, SWITCH, BREAK, PROCEDURE, RESTURN).

LST9 Incremental Linker/Loader.

CST9 Optimised C-Compiler (ANSI STANDARD).

ARST9 Library Archiver.

SIMST9 Software Simulator with realtime emulation executor

ST9036 Hardware Emulator. Realtime emulation of the ST9036 in all packaging options is performed by a modular emulation system, interfaced to the host computer through an RS232 channel, whit powerful hardware breakpoints, on-line assembler/disassembler, emulation and trace memory. The emulator is fully supported by a simbolic on-line debugger and help facility.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	– 0.3 to 7.0	V
AV_{DD}, AV_{SS}	Analog Supply Voltage	$V_{SS} \le AV_{SS} < AV_{DD} \le V_{DD}$	V
V_I	Input Voltage	V_{SS} – 0.3 to V_{DD} +0.3	V
V_O	Output Voltage	V_{SS} – 0.3 to V_{DD} +0.3	V
T_{STG}	Storage Temperature	– 55 to + 150	°C

Note: Stresses above those listed as "absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value		Unit
		Min.	Max.	
T_A	Operating Temperature	– 40	85	°C
V_{DD}	Operating Supply Voltage	4.5	5.5	V
f_{OSCE}	External Oscillator Frequency		24	MHz
f_{OSCI}	Internal Oscillator Frequency		12	MHz

DC ELECTRICAL CHARACTERISTICS

(V_{DD} = 5V ± 10% T_A = – 40 °C to + 85°C, unless otherwise specified)

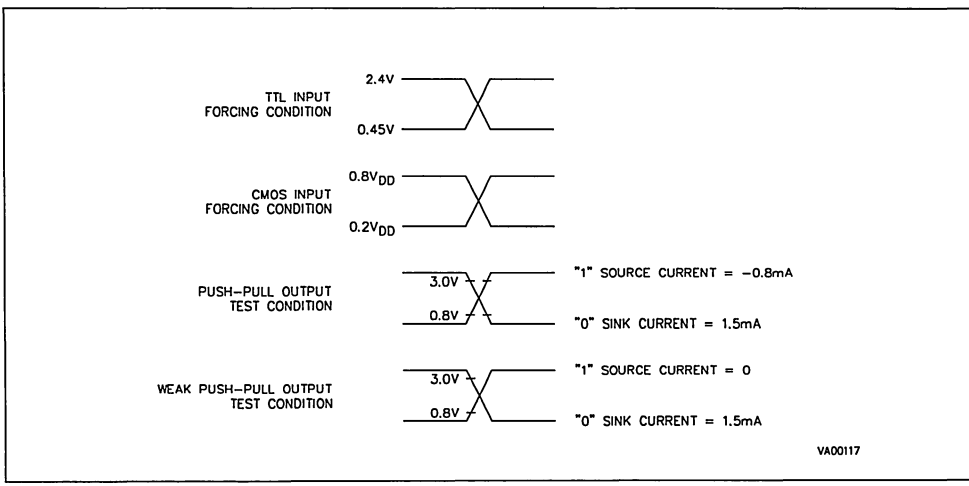
Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
V_{IHCK}	Clock Input High Level	External Clock	0.7 V_{DD}		V_{DD} + 0.3	V
V_{ILCK}	Clock Input Low Level	External Clock	– 0.3		0.3 V_{DD}	V
V_{IH}	Input High Level	TTL	2.0		V_{DD} + 0.3	V
		CMOS	0.7 V_{DD}		VDD + 0.3	V
V_{IL}	Input Low Level	TTL	– 0.3		0.8	V
		CMOS	– 0.3		0.3 V_{DD}	V
V_{IHRS}	Reset Input High Level		0.7 V_{DD}		V_{DD} + 0.3	V
V_{ILRS}	Reset Input Low Level		–0.3		0.3 V_{DD}	V
V_{HYRS}	Reset Input Hysteresis		0.3		1.5	V
V_{OH}	Output High Level	Push Pull, Iload = – 0.8mA	V_{DD} – 0.8			V
V_{OL}	Output Low Level	Push Pull or Open Drain, Iload = – 1.6mA			0.4	V
I_{WPU}	Weak Pull-up Current	Bidirectional Weak Pull-up, V_{OL} = 0V	– 80	– 200	– 420	µA

DC ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
I_{APU}	Active Pull-up Current, for INT0 and INT7 only	$V_{IN} < 0.8V$	– 80	– 200	– 420	µA
I_{LKIO}	I/O Pin Input Leakage	Input/Tri-State, $0V < V_{IN} < V_{DD}$	– 10		+ 10	µA
I_{LKRS}	Reset Pin Input Leakage	$0V < V_{IN} < V_{DD}$	– 30		+ 30	µA
I_{LKAD}	A/D Pin Input Leakage	Alternate Function, Open Drain, $0V < V_{IN} < V_{DD}$	– 3		+ 3	µA
I_{LKAP}	Active Pull-up Input Leakage	$0V < V_{IN} < 0.8V$	– 10		+ 10	µA
I_{LKOS}	OSCIN Pin Input Leakage	$0V < V_{IN} < V_{DD}$	– 10		+ 10	µA
I_{DD}	Run Mode Current	24MHz, Note 1		32	70	mA
		4MHz, Note 1		6	12	mA
I_{DP2}	Run Mode Current Prescale by 2	24MHz, Note 1		19	40	mA
		4MHz, Note 1		4	8	mA
I_{WFI}	WFI Mode Current	24MHz, Note 1		9	18	mA
		4MHz, Note 1		2.5	5	mA
I_{HALT}	HALT Mode Current	24MHz, Note 1			100	µA

Note:
1. All I/O Ports are configured in Bidirectional Weak Pull-up Mode with no DC load, External Clock pin (OSCIN) is driven by square wave external clock. No peripheral working. External interface not active (Internal Program Execution).

DC TEST CONDITIONS



AC ELECTRICAL CHARACTERISTICS

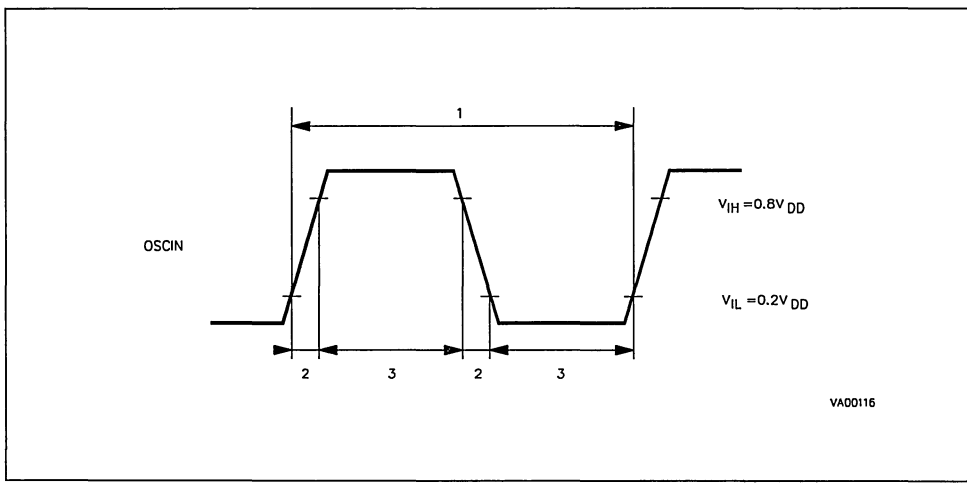
CLOCK TIMING TABLE

(V_{DD} = 5V ± 10%, T_A = − 40°C to + 85°C, unless otherwise specified)

N°	Symbol	Parameter	Value		Unit	Note
			Min.	Max.		
1	TpC	OSCIN Clock Period	41.5		ns	1
			83		ns	2
2	TrC, TfC	OSCIN Rise and Fall Time		12	ns	
3	TwCL, TwCH	OSCIN Low and High Width	25	12	ns	1
			38		ns	2

Note: 1. Clock divided by 2 internally (MODER.DIV2=1)
2. Clock not divided by 2 internally (MODER.DIV2=0)

CLOCK TIMING



EXTERNAL BUS TIMING TABLE

(V_{DD} = 5V ± 10%, T_A = – 40 °C to + 85 °C, Cload = 50pF, CPUCLK = 12MHz, unless otherwise specified)

N°	Symbol	Parameter	Value (Note)				Unit
			OSCIN Divided By 2	OSCIN Not Divided By 2	Min.	Max.	
1	TsA (AS)	Address Set-up Time before $\overline{AS}$ ↑	TpC (2P+1) –22	TWCH+PTpC –18	20		ns
2	ThAS (A)	Address Hold Time after $\overline{AS}$ ↑	TpC –17	TwCL –13	25		ns
3	TdAS (DR)	$\overline{AS}$ ↑ to Data Available (read)	TpC (4P+2W+4) –52	TpC (2P+W+2) –51		115	ns
4	TwAS	$\overline{AS}$ Low Pulse Width	TpC (2P+1) –7	TwCH+PTpC –3	35		ns
5	TdAz (DS)	Address Float to $\overline{DS}$ ↓	0	0	0		ns
6	TwDSR	$\overline{DS}$ Low Pulse Width (read)	TpC (4P+2W+3) –20	TwCH+TpC (2P+W+1) – 16	105		ns
7	TwDSW	$\overline{DS}$ Low Pulse Width (write)	TpC (2P+2W+2) –13	TpC (P+W+1) –13	70		ns
8	TdDSR (DR)	$\overline{DS}$ ↓ to Data Valid Delay (read)	TpC (4P+2W-3) –50	TwCH+TpC(2P+W+1) – 46		75	ns
9	ThDR (DS)	Data to $\overline{DS}$ ↑ Hold Time (read)	0	0	0		ns
10	TdDS (A)	$\overline{DS}$ ↑ to Address Active Delay	TpC –7	TwCL –3	35		ns
11	TdDS (AS)	$\overline{DS}$ ↑ to $\overline{AS}$ ↓ Delay	TpC –18	TwCL –14	24		ns
12	TsR/W (AS)	R/$\overline{W}$ Set-up Time before $\overline{AS}$ ↑	TpC (2P+1) –22	TwCH+PTpC –18	20		ns
13	TdDSR (R/W)	$\overline{DS}$ ↑ to R/$\overline{W}$ and Address Not Valid Delay	TpC –9	TwCL –5	33		ns
14	TdDW (DSW)	Write Data Valid to $\overline{DS}$ ↓ Delay (write)	TpC (2P+1) –32	TwCH+PTpC –28	10		ns
15	ThDS (DW)	Data Hold Time after DS ↑ (write)	TpC –9	TwCL –5	33		ns
16	TdA (DR)	Address Valid to Data Valid Delay (read)	TpC (6P+2W+5) –68	TwCH+TpC (3P+W+2) – 64		140	ns
17	TdAs (DS)	$\overline{AS}$ ↑ to $\overline{DS}$ ↓ Delay	TpC –18	TwCL –14	24		ns

Note: The value left hand two columns show the formula used to calculate the timing minimum or maximum from the oscillator clock period, prescale value and number of wait cycles inserted.
The value right hand two columns show the timing minimum and maximum for an external clock at 24 MHz divided by 2, prescaler value of zero and zero wait status.

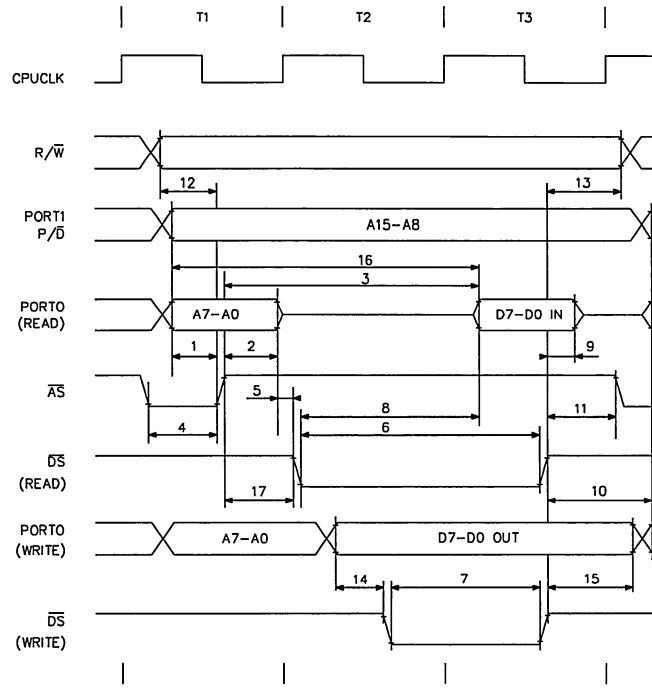
Legend:
P = Clock Prescaling Value
W = Wait Cycles
TpC = OSCIN Period
TwCH = High Level OSCIN half period
TwCL = Low Level OSCIN half period

EXTERNAL WAIT TIMING TABLE (V_{DD} = 5V ± 10%, T_A = –40°C to +85°C, Cload = 50pF, INTCLK = 12MHz, Push-pull output configuration, unless otherwise specified)

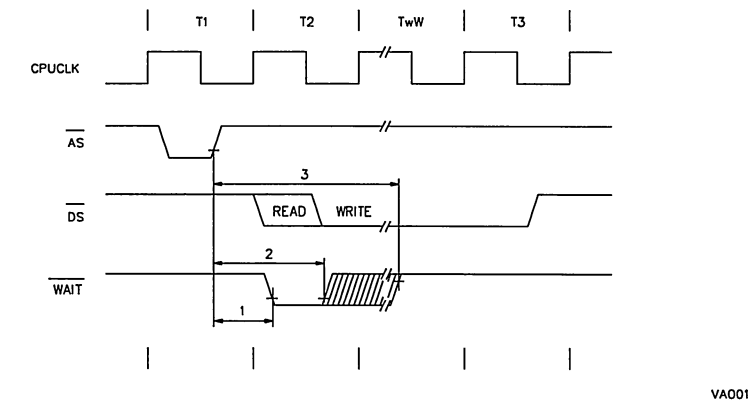
N°	Symbol	Parameter	Value (Note)				Unit
			OSCIN Divided By 2	OSCIN Not Divided By 2	Min.	Max.	
1	TdAS (WAIT)	$\overline{AS}$ ↑ to $\overline{WAIT}$ ↓ Delay	2(P+1)TpC –29	(P+1)TpC –29		40	ns
2	TdAS (WAIT)	$\overline{AS}$ ↑ to $\overline{WAIT}$ ↑ Minimum Delay	2(P+W+1)TpC –4	(P+W+1)TpC –4	80		ns
3	TdAS (WAIT)	$\overline{AS}$ ↑ to $\overline{WAIT}$ ↑ Maximum Delay	2(P+W+1)TpC –29	(P+W+1)TpC –29		83W+40	ns

Note: The value left hand two columns show the formula used to calculate the timing minimum or maximum from the oscillator clock period, prescale value and number of wait cycles inserted.
The value right hand two columns show the timing minimum and maximum for an external clock at 24 MHz divided by 2, prescale value of zero and zero wait status.

EXTERNAL BUS TIMING



EXTERNAL WAIT TIMING

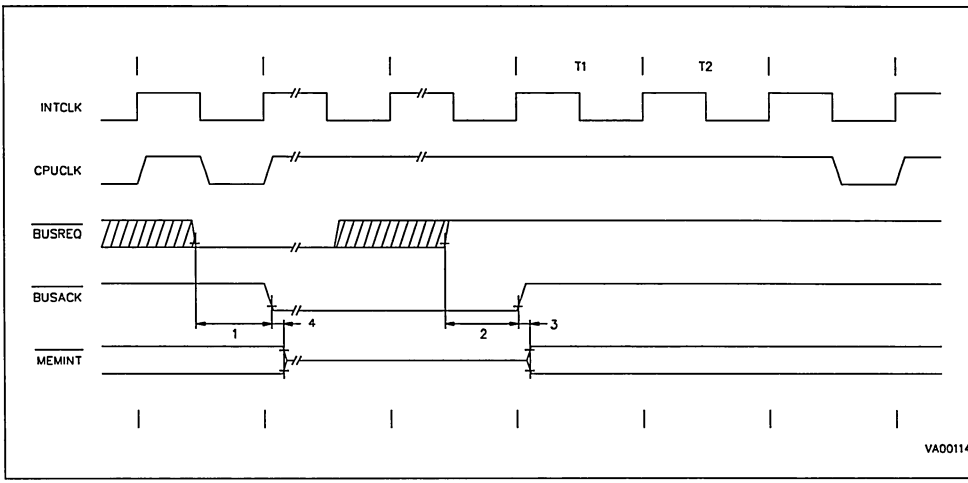


BUS REQUEST/ACKNOWLEDGE TIMING TABLE (V_{DD} = 5V ± 10%, T_A = −40°C to +85°C, Cload = 50pF, INTCLK = 12MHz, Push-pull output configuration, unless otherwise specified)

N°	Symbol	Parameter	Value (Note)				Unit
			OSCIN Divided By 2	OSCIN Not Divided By 2	Min.	Max.	
1	TdBR (BACK)	$\overline{BREQ}$ ↓ to $\overline{BUSACK}$ ↓	TpC+8	TwCL+12	50		ns
			TpC(6P+2W+7)+65	TpC(3P+W+3)+TwCL+65		360	ns
2	TdBR (BACK)	$\overline{BREQ}$ ↑ to $\overline{BUSACK}$ ↑	3TpC+60	TpC+TwCL+60		185	ns
3	TdBACK (BREL)	$\overline{BUSACK}$ ↓ to Bus Release	20	20		20	ns
4	TdBACK (BACT)	$\overline{BUSACK}$ ↑ to Bus Active	20	20		20	ns

Note: The value left hand two columns show the formula used to calculate the timing minimum or maximum from the oscillator clock period, prescale value and number of wait cycles inserted.
The value right hand two columns show the timing minimum and maximum for an external clock at 24 MHz divided by 2, prescale value of zero and zero wait status.

BUS REQUEST/ACKNOWLEDGE TIMING



Note : MEMINT = group of memory interface signals : $\overline{AS}$, $\overline{DS}$, R/$\overline{W}$, P00-P07, P10-P17.

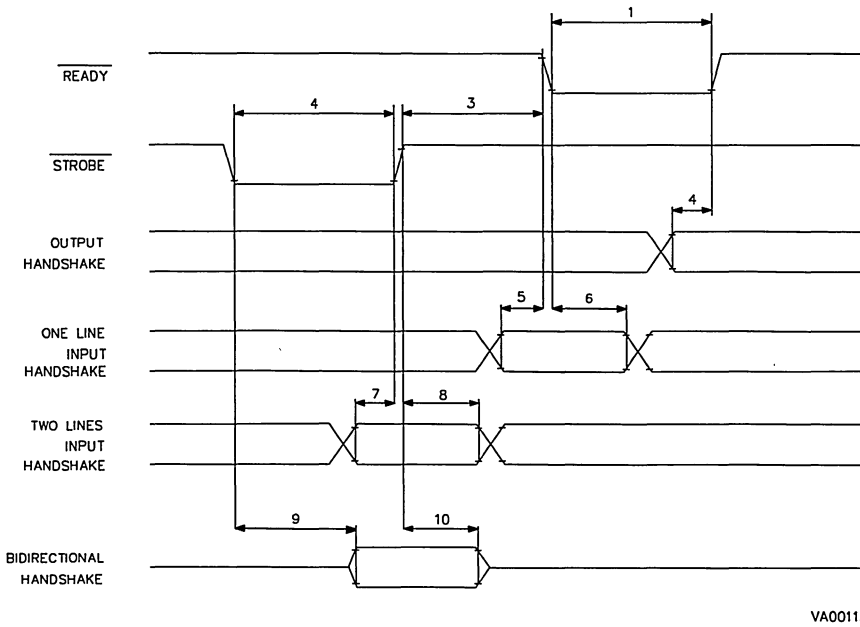
HANDSHAKE TIMING TABLE (V_{DD} = 5V ± 10%, T_A = –40°C to +85°C, Cload = 50pF, INTCLK = 12MHz, Push-pull output configuration, unless otherwise specified)

N°	Symbol	Parameter	Value (Note)				Min.	Max.	Unit
			OSCIN Divided By 2		OSCIN Not Divided By 2				
			Min.	Max.	Min.	Max.			
1	TwRDY	RDRDY, WRRDY Pulse Width in One Line Handshake	2TpC (P+W+1) –18		TpC (P+W+1) –18		65		ns
2	TwSTB	$\overline{RDSTB}$, $\overline{WRSTB}$ Pulse Width	2TpC+12		TpC+12		95		ns
3	TdST (RDY)	$\overline{RDSTB}$, or $\overline{WRSTB}$ ↑ to RDRDY or WRRDY ↓		TpC+45		(TpC-TwCL) +45		87	ns
4	TsPD (RDY)	Port Data to RDRDY ↑ Set-up Time	(2P+2W+1) TpC –25		TwCH+(W+P) TpC –25		16		ns
5	TsPD (RDY)	Port Data to WRRDY ↓ Set-up Time in One Line Handshake	43		43		43		ns
6	ThPD (RDY)	Port Data to WRRDY ↓ Hold Time in One Line Handshake	0		0		0		ns
7	TsPD (STB)	Port Data to $\overline{WRSTB}$ ↑ Set-up Time	10		10		10		ns
8	ThPD (STB)	Port Data to WRSTB ↑ Hold Time	25		25		25		ns
9	TdSTB (PD)	$\overline{RDSTBD}$ ↑ to Port Data Delay Time in Bidirectional Hand-shake		35		35		35	ns
10	TdSTB (PHZ)	$\overline{RDSTB}$ ↑ to Port High-Z Delay Time in Bidirectional Hand-shake		25		25		25	ns

Note: The value left hand two columns show the formula used to calculate the timing minimum or maximum from the oscillator clock period, prescale value and number of wait cycles inserted.
The value right hand two columns show the timing minimum and maximum for an external clock at 24 MHz divided by 2, prescaler value of zero and zero wait status.

Legend:
P = Clock Prescaling Value (R235.4,3,2)
W = Programmable Wait Cycles (R252.2.1.0/5,4,3) + External Wait Cycles

HANDSHAKE TIMING

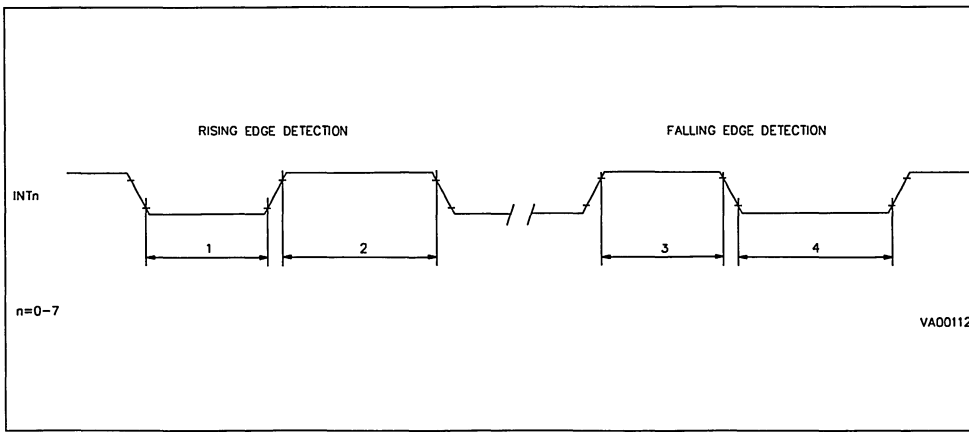


EXTERNAL INTERRUPT TIMING TABLE (V_{DD} = 5V ± 10%, T_A = –40°C to +85°C, Cload = 50pF, INTCLK = 12MHz, Push-pull output configuration, unless otherwise specified)

N°	Symbol	Parameter	Value (Note)				Unit
			OSCIN Divided By 2 Min.	OSCIN Not Divided By 2 Min.	Min.	Max.	
1	TwLR	Low Level Minimum Pulse Width in Rising Edge Mode	2TpC+12	TpC+12	95		ns
2	TwHR	High Level Minimum Pulse Width in Rising Edge Mode	2TpC+12	TpC+12	95		ns
3	TwHF	High Level Minimum Pulse Width in Falling Edge Mode	2TpC+12	TpC+12	95		ns
4	TwLF	Low Level Minimum Pulse Width in Falling Edge Mode	2TpC+12	TpC+12	95		ns

Note: The value left hand two columns show the formula used to calculate the timing minimum or maximum from the oscillator clock period, prescale value and number of wait cycles inserted.
The value right hand two columns show the timing minimum and maximum for an external clock at 24 MHz divided by 2, prescale value of zero and zero wait status.

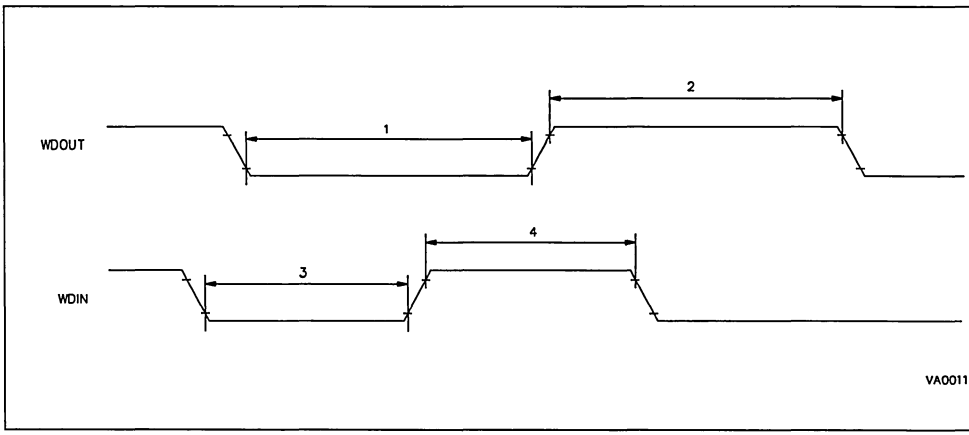
EXTERNAL INTERRUPT TIMING



WATCHDOG TIMING TABLE (V_{DD} = 5V ± 10%, T_A = –40°C to +85°C, Cload = 50pF, INTCLK =12MHz, Output Alternate Function set as Push-pull)

N°	Symbol	Parameter	Value		Unit
			Min.	Max.	
1	TwWDOL	WDOUT Low Pulse Width	620		ns
2	TwWDOH	WDOUT High Pulse Width	620		ns
3	TwWDIL	WDIN Low Pulse Width	350		ns
4	TwWDIH	WDIN High Pulse Width	350		ns

WATCHDOG TIMING

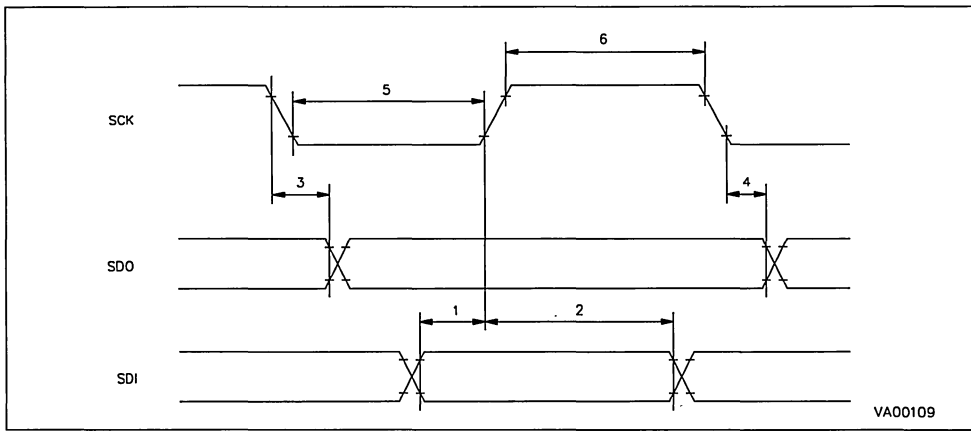


SPI TIMING TABLE (V_{DD} = 5V ± 10%, T_A = –40°C to +85°C, Cload = 50pF, INTCLK = 12MHz, Output Alternate Function set as Push-pull)

N°	Symbol	Parameter	Value		Unit
			Min.	Max.	
1	TsDI	Input Data Set-up Time	100		ns
2	ThDI (1)	Input Data Hold Time	1/2 TpC+100		ns
3	TdOV	SCK to Output Data Valid		100	ns
4	ThDO	Output Data Hold Time	-20		ns
5	TwSKL	SCK Low Pulse Width	300		ns
6	TwSKH	SCK High Pulse Width	300		ns

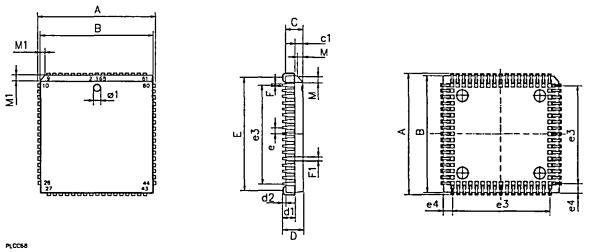
Note: 1. TpC is the Clock period.

SPI TIMING



PACKAGE MECHANICAL DATA

Figure 53. 68-Lead Plastic Leaded Chip Carrier (C)



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A	25.02		25.27	0.985		0.995
B	24.13		24.33	0.950		0.958
D	4.20		5.08	0.165		0.200
d1		2.54			0.100	
d2		0.56			0.022	
E	22.61		23.62	0.890		0.930
e		1.27			0.050	
F		0.38			0.015	
G			0.10			0.004
M		1.27			0.050	
M1		1.14			0.044	
Ø1		7.36			0.289	

Figure 54. 80-Lead Plastic Quad Flat Package (q)

Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A			3.40			.134
A1	0.25			.010		
A2	2.55	2.80	3.05	.100	.110	.120
D	22.95	23.20	23.45	.904	.913	.923
D1	19.90	20.00	20.10	.783	.787	.791
D3	18.40 REF			.724 REF.		
Zd	0.80 REF.			.031 REF.		
E	16.95	17.20	17.45	.667	.677	.687
E1	13.90	14.00	14.10	.547	.551	.555
E3	12.00 REF.			.472 REF.		
Ze	1.00 REF.			.039 REF.		
L	0.65	0.80	0.95	.026	.031	.037
N	80			80		
e	0.80 BSC.			.032 BSC.		
B	0.30		0.45	.012		.018
B1	0.30	0.35	0.40	.012	.014	.016
aaa	0.20			.008		
Nd	24			24		
Ne	16			16		

ORDERING INFORMATION

Sales Type	Frequency	Temperature Range	Package
ST9036C6/XX	24MHz	-40°C to + 85°C	PLCC68
ST9036C1/XX	24MHz	0°C to +70°C	PLCC68
ST9036Q6/XX	24MHz	-40°C to +85°C	PQFP80
ST9036Q1/XX	24MHz	0°C to +70°C	PQFP80

Note: "XX" is the ROM code identifier that is allocated by SGS-THOMSON after receipt of all required options and the related ROM file.

ST9036 OPTION LIST

Please copy this page (enlarge if possible) and complete ALL sections. Send the form, with the ROM code image required, to your local SGS-THOMSON sales office.

Customer Company : [.....]

Company Address : [.....]

[.....]

Telephone : [.....]

FAX : [.....]

Contact : [.....] Telephone (Direct) : [.....]

Please confirm device required :

Package [ ] (p) Temperature Range [ ] (t)

Special Marking [ ] (y/n) 11 characters [| | | | | | | | | |] (N)

Notes:

(p) C = Chip Carrier Plastic, Q = Quad Flat Package Plastic
(t) 1 = 0 to +70°C, 6 = -40 to +85°C
(N) Available : ASCII 020h - 05Fh

Please consult your local SGS-THOMSON sales office for other marking details

ROMLESS OPTION (consult text)
[ ] YES [ ] NO
If yes, identify required pin (Port.bit)
[ ] P3.7 [ ] P2.0

Code : [ ] EPROM (27128 or 27256)
[ ] HEX format files on IBM-PC® compatible disk
filename : [.....]

Confirmation : [ ] Code checked with EPROM device in application

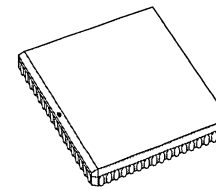
Yearly Quantity forecast : [.....] k units
- for a period of : [.....] years
Preferred Production start dates : [.....] (YY/MM/DD)

Customer Signature : [.....]

Date : [.....]

16K ROM HCMOS MCU WITH EEPROM, RAM AND A/D

- Single chip microcontroller with 16K bytes of ROM, 256 bytes of RAM and 256 bytes of register file with 224 general purpose registers available as RAM, accumulators or index pointers.
- 512 bytes of high-reliability EEPROM on-chip, with 300,000 erase/write cycle capability and 10 year data retention.
- On-chip programmable security protection against external reading of internal memory.
- 8/16 bit CORE with full feature DMA controller, a powerful interrupt handler and a Standard Serial Peripheral Interface (SPI) handling S-bus, I^2C-bus, IM-bus and Standard Serial Peripheral Interfaces.
- Up to 8 external interrupts edge-selectable plus 1 non-maskable interrupt.
- 16 bit programmable Timer with 8 bit Prescaler, able to be used as a Watchdog Timer for system integrity.
- Two 16 bit Multifunction Timer modules, each with an 8 bit prescaler and 13 operating modes, allowing simple use for complex waveform generation and measurement, PWM functions and many other system timing operations.
- 8 channel Analog to Digital Converter, with integral sample and hold, fast 11µs conversion time, 8 bit ± 1/2 LSB resolution with Analog Watchdog on two channels.
- Full function Serial Communications Interface with 110 to 375,000 baud rate generator, asynchronous and byte synchronous capability (fully programmable format) and address/wake-up bit option.
- On-chip DMA channels associated to the Multifunction Timers and the Serial Communications Interface.
- Up to seven 8 bit I/O ports with programmable input thresholds and output characteristics. Alternative functions allow the full use of all pins.
- Powerful software development tools, including assembler, linker, C-compiler, archiver, software and hardware emulators.
- Windowed and One Time Programmable EPROM parts available for prototyping and preproduction development phases.
- 68-lead Plastic Leaded Chip Carrier package.



PLCC68

(Ordering Information at the end of the datasheet)

Figure 1. ST9040 Block Diagram

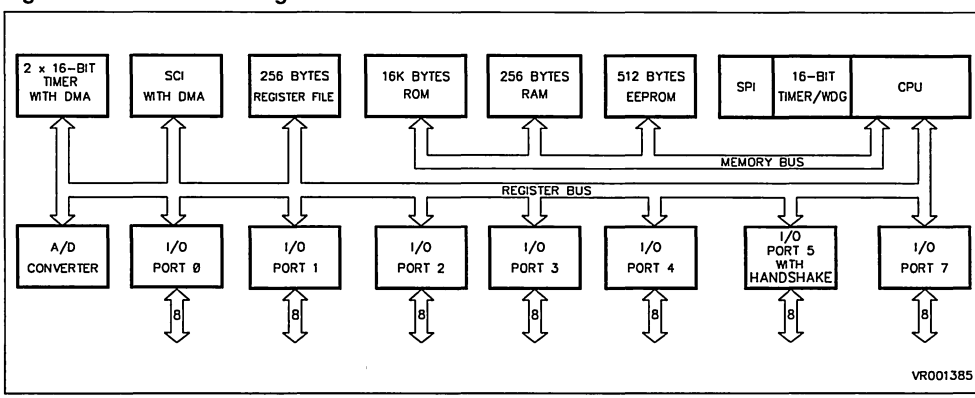
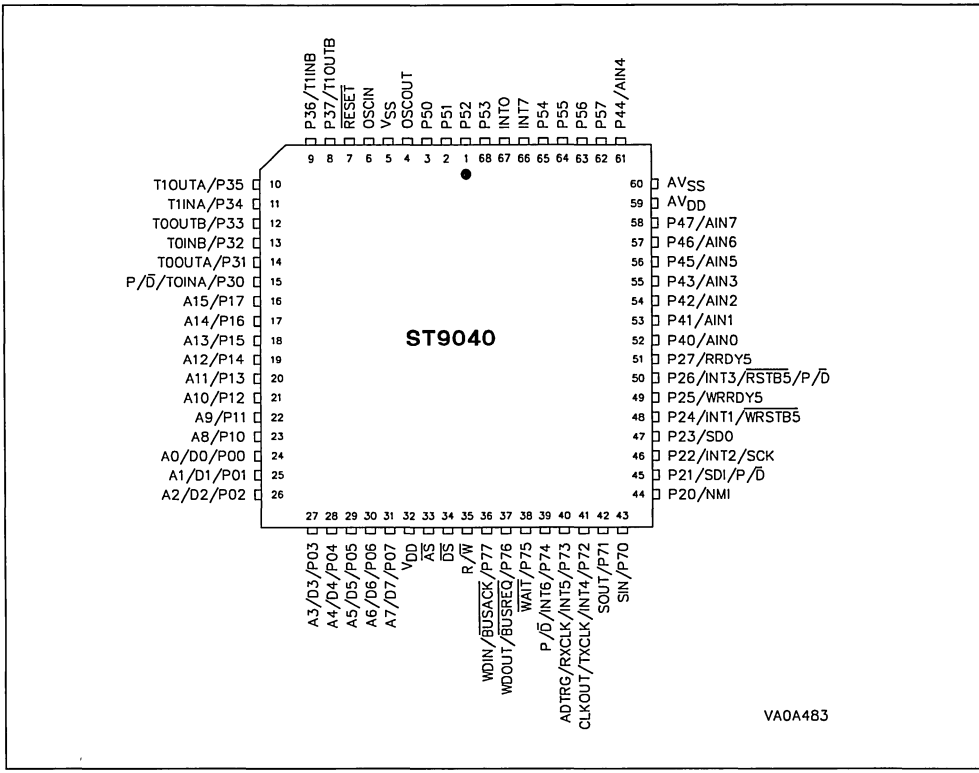


Figure 2. ST9040 Pin Configuration



GENERAL DESCRIPTION

The ST9040 is a ROM member of the ST9 family of microcontrollers, completely developed and produced by SGS-THOMSON Microelectronics using a proprietary n-well HCMOS process.

The ROM device is fully compatible with its EPROM version, which may be used for the prototyping and pre-production phases of development, and can be configured as: a standalone microcontroller with 16K bytes of on-chip ROM, a microcontroller able to manage up to 112K bytes of external memory, or as a parallel processing element in a system with other processors and peripheral controllers.

A key point of the ST9040 architecture is related to its modular approach which allows software commonality with all other members of the ST9 family.

The nucleus of the modular design of the ST9040 is the advanced Core which includes the Central Processing Unit (CPU), the Register File, a 16 bit Timer/Watchdog with 8 bit Prescaler, a Serial Peripheral Interface supporting S-bus, I^2C-bus and IM-bus Interface, plus two 8 bit I/O ports. The Core has independent memory and register buses allowing a high degree of pipelining to add to the efficiency of the code execution speed of the extensive instruction set. The powerful I/O capabilities demanded by microcontroller applications are fulfilled by the ST9040 with up to 56 I/O lines dedicated to digital Input/Output. These lines are grouped into up to seven 8 bit I/O Ports and can be configured on a bit basis under software control to provide timing, status signals, an address/data bus for interfacing external memory, timer inputs and outputs, analog inputs, external interrupts and serial or parallel I/O with or without handshake.

Three basic memory spaces are available to support this wide range of configurations: Program Memory (internal and external), Data Memory (external) and the Register File, which includes the control and status registers of the on-chip peripherals.

GENERAL DESCRIPTION (Continued)

Two 16 bit MultiFunction Timers, each with an 8 bit Prescaler and 13 operating modes allow simple use for complex waveform generation and measurement, PWM functions and many other system timing functions by the usage of the two associated DMA channels for each timer. In addition there is an 8 channel Analog to Digital Converter with integral sample and hold, fast 11µs conversion time and 8 bit ± 1/2 LSB resolution. An Analog Watchdog feature is included for two input channels.

Completing the device is a full duplex Serial Communications Interface with an integral 110 to 375,000 baud rate generator, asynchronous and byte synchronous capability (fully programmable format) and associated address/wake-up option, plus two DMA channels.

PIN DESCRIPTION

$\overline{AS}$. *Address Strobe (output, active low, 3-state).* Address Strobe is pulsed low once at the beginning of each memory cycle. The rising edge of $\overline{AS}$ indicates that address, Read/Write (R/$\overline{W}$), and Data Memory signals are valid for program or data memory transfers. Under program control, $\overline{AS}$ can be placed in a high-impedance state along with Port 0 and Port 1, Data Strobe ($\overline{DS}$) and R/$\overline{W}$.

$\overline{DS}$. *Data Strobe (output, active low, 3-state).* Data Strobe provides the timing for data movement to or from Port 0 for each memory transfer. During a write cycle, data out is valid at the leading edge of $\overline{DS}$. During a read cycle, Data In must be valid prior to the trailing edge of $\overline{DS}$. When the ST9040 accesses on-chip memory, $\overline{DS}$ is held high during the whole memory cycle. It can be placed in a high impedance state along with Port 0, Port 1, $\overline{AS}$ and R/$\overline{W}$.

R/$\overline{W}$. *Read/Write (output, 3-state).* Read/Write determines the direction of data transfer for external memory transactions. R/$\overline{W}$ is low when writing to external program or data memory, and high for all other transactions. It can be placed in a high impedance state along with Port 0, Port 1, $\overline{AS}$ and $\overline{DS}$.

$\overline{RESET}$. *Reset (input, active low).* The ST9 is initialised by the Reset signal. With the deactivation of $\overline{RESET}$, program execution begins from the Program memory location pointed to by the vector contained in program memory locations 00h and 01h.

OSCIN, OSCOUT. *Oscillator (input and output).* These pins connect a parallel-resonant crystal (24MHz maximum), or an external source to the on-chip clock oscillator and buffer. OSCIN is the input of the oscillator inverter and internal clock generator; OSCOUT is the output of the oscillator inverter.

AV_{DD}. Analog V_{DD} of the Analog to Digital Converter.

AV_{SS}. Analog V_{SS} of the Analog to Digital Converter.

V_{DD}. Main Power Supply Voltage (5V ± 10%)

V_{SS}. Digital Circuit Ground.

P0.0-P0.7, P1.0-P1.7, P2.0-P2.7 P3.0-P3.7, P4.0-P4.7, P5.0-P5.7, P7.0-P7.7 *I/O Port Lines (Input/Output, TTL or CMOS compatible).* 8 lines grouped into I/O ports of 8 bits, bit programmable under program control as general purpose I/O or as Alternate functions (see next section).

I/O Port Alternate Functions

Each pin of the I/O ports of the ST9030 and ST9031 may assume software programmable Alternative Functions as shown in the Pin Configuration Drawings. Due to Bonding options for the packages, some functions may not be present, Table 1 shows the Functions allocated to each I/O Port pins and a summary of packages for which they are available.

PIN DESCRIPTION (Continued)

Table 1. ST9040 I/O Port Alternate Function Summary

I/O PORT Port. bit	Name	Function	Alternate Function	Pin Assignment
P0.0	A0/D0	I/O	Address/Data bit 0 mux	24
P0.1	A1/D1	I/O	Address/Data bit 1 mux	25
P0.2	A2/D2	I/O	Address/Data bit 2 mux	26
P0.3	A3/D3	I/O	Address/Data bit 3 mux	27
P0.4	A4/D4	I/O	Address/Data bit 4 mux	28
P0.5	A5/D5	I/O	Address/Data bit 5 mux	29
P0.6	A6/D6	I/O	Address/Data bit 6 mux	30
P0.7	A7/D7	I/O	Address/Data bit 7 mux	31
P1.0	A8	O	Address bit 8	23
P1.1	A9	O	Address bit 9	22
P1.2	A10	O	Address bit 10	21
P1.3	A11	O	Address bit 11	20
P1.4	A12	O	Address bit 12	19
P1.5	A13	O	Address bit 13	18
P1.6	A14	O	Address bit 14	17
P1.7	A15	O	Address bit 15	16
P2.0	NMI	I	Non-Maskable Interrupt	44
P2.0	ROMless	I	ROMless Select (Mask option)	44
P2.1	P/$\overline{D}$	O	Program/Data Space Select	45
P2.1	SDI	I	SPI Serial Data Out	45
P2.2	INT2	I	External Interrupt 2	46
P2.2	SCK	O	SPI Serial Clock	46
P2.3	SDO	O	SPI Serial Data In	47
P2.4	INT1	I	External Interrupt 1	48
P2.4	$\overline{WRSTB5}$	O	Handshake Write Strobe P5	48
P2.5	WRRDY5	I	Handshake Write Ready P5	49
P2.6	INT3	I	External Interrupt 3	50
P2.6	$\overline{RDSTB5}$	I	Handshake Read Strobe P5	50
P2.6	P/$\overline{D}$	O	Program/Data Space Select	50
P2.7	RDRDY5	O	Handshake Read Ready P5	51
P3.0	T0INA	I	MF Timer 0 Input A	15
P3.0	P/$\overline{D}$	O	Program/Data Space Select	15
P3.1	T0OUTA	O	MF Timer 0 Output A	14
P3.2	T0INB	I	MF Timer 0 Input B	13
P3.3	T0OUTB	O	MF Timer 0 Output B	12
P3.4	T1INA	I	MF Timer 1 Input A	11

PIN DESCRIPTION (Continued)

Table 1. ST9040 I/O Port Alternate Function Summary (Continued)

I/O PORT Port. bit	Name	Function	Alternate Function	Pin Assignment
P3.5	T1OUTA	O	MF Timer 1 Output A	10
P3.6	T1INB	I	MF Timer 1 Input B	9
P3.7	T1OUTB	O	MF Timer 1 Output B	8
P4.0	AIN0	I	A/D Analog Input 0	52
P4.1	AIN1	I	A/D Analog Input 1	53
P4.2	AIN2	I	A/D Analog Input 2	54
P4.3	AIN3	I	A/D Analog Input 3	55
P4.4	AIN4	I	A/D Analog Input 4	61
P4.5	AIN5	I	A/D Analog Input 5	56
P4.6	AIN6	I	A/D Analog Input 6	57
P4.7	AIN7	I	A/D Analog Input 7	58
P5.0		I/O	I/O Handshake Port 5	3
P5.1		I/O	I/O Handshake Port 5	2
P5.2		I/O	I/O Handshake Port 5	1
P5.3		I/O	I/O Handshake Port 5	68
P5.4		I/O	I/O Handshake Port 5	65
P5.5		I/O	I/O Handshake Port 5	64
P5.6		I/O	I/O Handshake Port 5	63
P5.7		I/O	I/O Handshake Port 5	62
P7.0	SIN	I	SCI Serial Input	43
P7.1	SOUT	O	SCI Serial Output	42
P7.1	ROMless	I	ROMless Select (Mask option)	42
P7.2	INT4	I	External Interrupt 4	41
P7.2	TXCLK	I	SCI Transmit Clock Input	41
P7.2	CLKOUT	O	SCI Byte Sync Clock Output	41
P7.3	INT5	I	External Interrupt 5	40
P7.3	RXCLK	I	SCI Receive Clock Input	40
P7.3	ADTRG	I	A/D Conversion Trigger	40
P7.4	INT6	I	External Interrupt 6	39
P7.4	P/$\overline{D}$	O	Program/Data Space Select	39
P7.5	$\overline{WAIT}$	I	External Wait Input	38
P7.6	WDOUT	O	T/WD Output	37
P7.6	$\overline{BUSREQ}$	I	External Bus Request	37
P7.7	WDIN	I	T/WD Input	36
P7.7	$\overline{BUSACK}$	O	External Bus Acknowledge	36

ST9040 CORE

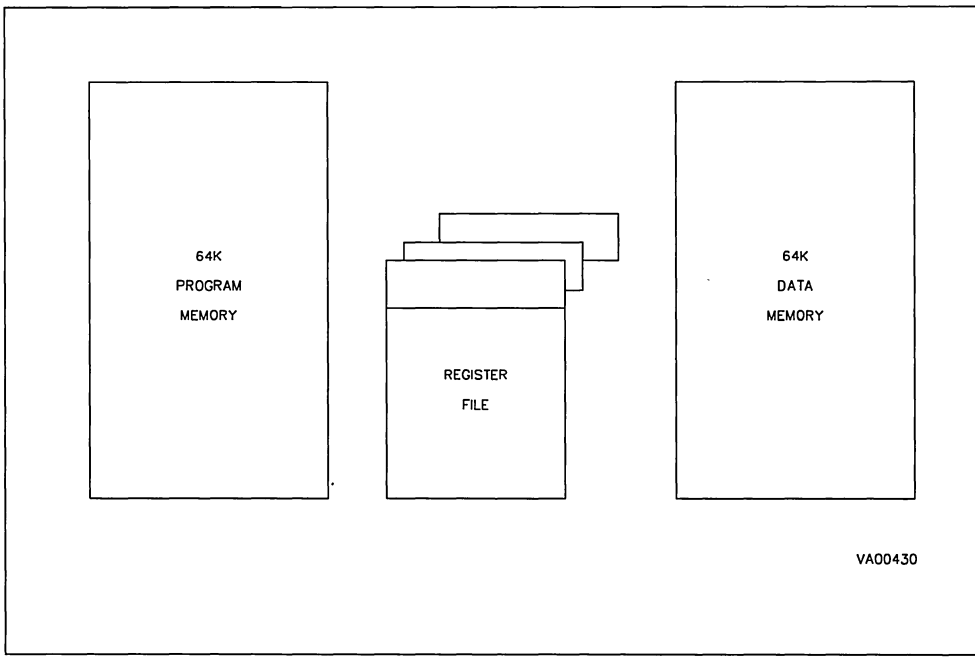
The Core or Central Processing Unit (CPU) of the ST9040 includes the 8 bit Arithmetic Logic Unit and the 16 bit Program Counter, System and User Stack Pointers. The microcoded Instruction Set is highly optimised for both byte (8 bit) and word (16 bit) data, BCD and Boolean data types, with 14 addressing modes. Two 8 bit I/O ports are connected to the Core module for external memory interfacing, while a 16 bit Timer/Watchdog gives system security and timing functions, and a Serial Peripheral Interface allows for synchronous communication. Three independent buses are controlled by the Core, a 16 bit Memory bus, an 8 bit Register addressing bus and a 6 bit Interrupt/DMA bus connected to the interrupt and DMA controllers in the on-chip peripherals and the Core. This multiple bus architecture allows a high degree of pipelining and parallel operation within the ST9040, giving it its efficiency in both numerical calculations and communication with the on-chip peripherals.

MEMORY

The memory of the ST9040 is functionally divided into two areas, the Register File and Memory. The Memory is divided into two spaces, each having a maximum of 65,536 bytes. The two memory spaces are separated by function, one space for Program code, the other for Data. The ST9040 16K bytes of on-chip ROM memory are selected at memory addresses 0 through 3FFFh (hexadecimal) in the PROGRAM space. The DATA space includes the 512 bytes of on-chip EEPROM at addresses 0 through 1FFh and the 256 bytes of on-chip RAM memory at memory addresses 200h through 2FFh.

Off-chip memory, addressed using the multiplexed address and data buses (Ports 0 and 1) may be divided into the Program and Data spaces by the external decoding of the Program/Data select pin (P/$\overline{D}$) available as an Alternate function, allowing a full 128K byte memory.

Figure 3. Memory Spaces



MEMORY (Continued)

The memory spaces are selected by the execution of the SDM and SPM instructions (Set Data Memory and Set Program Memory, respectively). There is no need to use either of these instructions again until the memory area required is to be changed. This requirement is not necessary in two cases: first, when operating with external stacks (the Data memory is automatically selected) and, secondly, when using the memory indirect to memory indirect post-increment addressing mode (the memory types are specified in the instructions: LDPP, LDPD, LDDP, LDDD).

Either the Data Memory or the Program Memory can be addressed using any of the memory addressing modes.

Program Space Definition

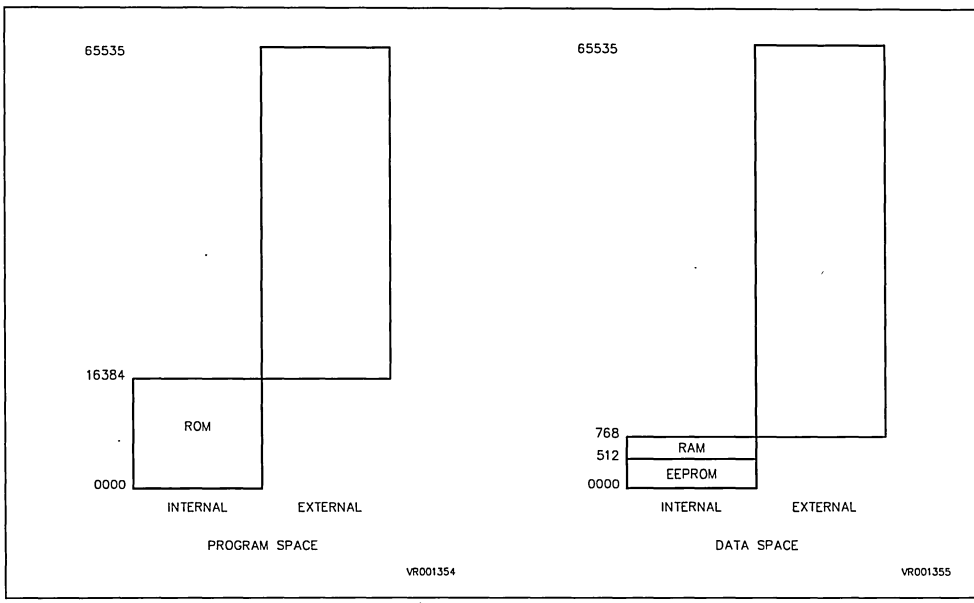
The Program memory space of the ST9040, from the 16K bytes of on-chip ROM memory to the full 64K bytes with off-chip memory expansion is fully available to the user. At addresses greater than the first 16K of program space, the ST9040 executes external memory cycles for instruction fetches. The first 256 memory locations from address 0 to 0FFh (hexadecimal) hold the Reset Vector, the Top-Level (Pseudo Non-Maskable) interrupt, the Divide by Zero Trap vector and, optionally, the interrupt vector table for use with the on-chip peripherals and the external interrupt sources. Each vector is contained in two consecutive byte locations, the high order address held in the lower (even) byte, the low order address held in the upper (odd) byte, forming the address which is loaded into the Program Counter when selected by the interrupt vector provided by the interrupt source. This should point to the relevant Interrupt Service routine provided by the user for immediate response to the interrupt.

Data Space Definition

The ST9040 addresses the 512 bytes of on-chip EEPROM memory in the Data Space from addresses 0 to 511 (00h to 1FFh) and the 256 bytes of on-chip RAM memory from addresses 512 to 768 (200h to 2FFh). It may also address up to 64,768 locations of External Data through the External Memory Interface when decoded with the P/$\overline{D}$ pin. The on-chip general purpose Registers may be used as additional RAM memory for minimum chip count systems.

The Data Space is selected by the execution of the SDM instruction. All subsequent memory references will access the Data Space. When a separate Data Space is not required, data may stored in external RAM or ROM memory within the Program Space.

Figure 5. ST9040 Memory Map



MEMORY (Continued)

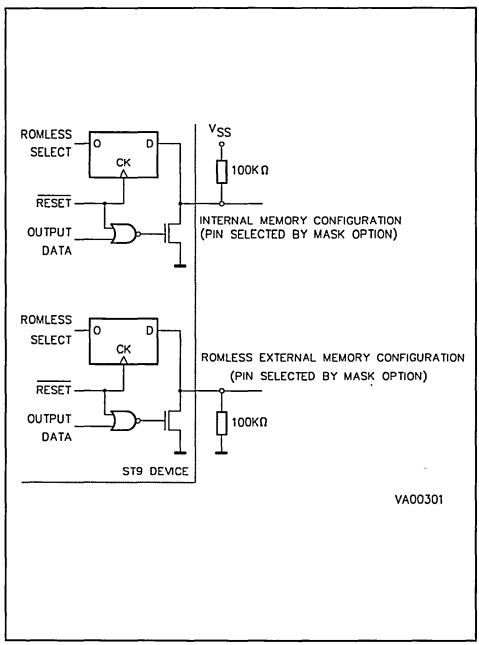
ROMless Option

In the event of a program revision being required after the development of a ROM-based ST9040, a mask option is available which enables the reconfiguration of the memory spaces to give a fully ROMless device. This means that the on-chip program ROM is disabled and ALL PROGRAM memory is seen as external, allowing the use of replacement program code in external ROM memory. The on-chip EEPROM and RAM memory in DATA space is not affected.

To give the ROMless function (when enabled by the MASK option), the enabled pin, marked ROMless as an Alternate Function, should be held to ground (V_{SS}) with a high resistance (eg 100k ohm) during the RESET cycle. The pin status is latched on the rising edge of the RESET input. After this time, the pin is free for normal operation.

If the ROMless option is enabled, and the on-chip program is to be used, the pin enabled for the ROMless function must to held to a high potential during the RESET cycle (eg with a 100k ohm resistor to V_{DD}).

Figure 6. ROMless Selection

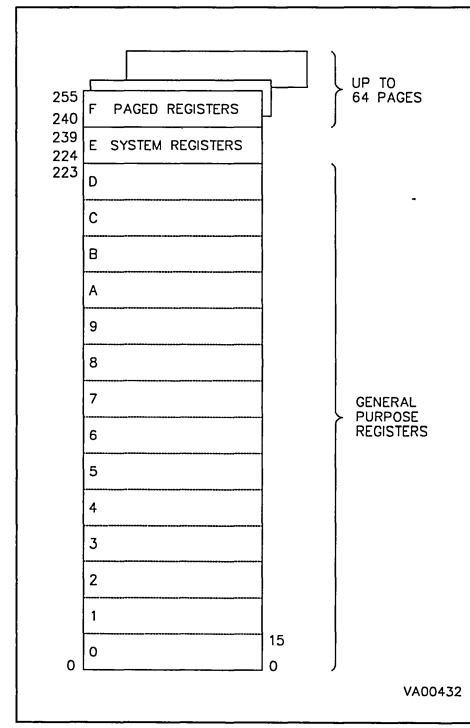


REGISTERS

The ST9040 Register File consists of 240 registers (224 general purpose) plus pages of 16 registers supporting the configuration and control registers for the on-chip peripherals. The 224 general purpose registers all have 8 and 16 bit arithmetic capability and may be used as accumulators, on-chip RAM, internal Stack areas (for system and/or user stacks), or, with the appropriate addressing modes, as index, offset or stack pointers.

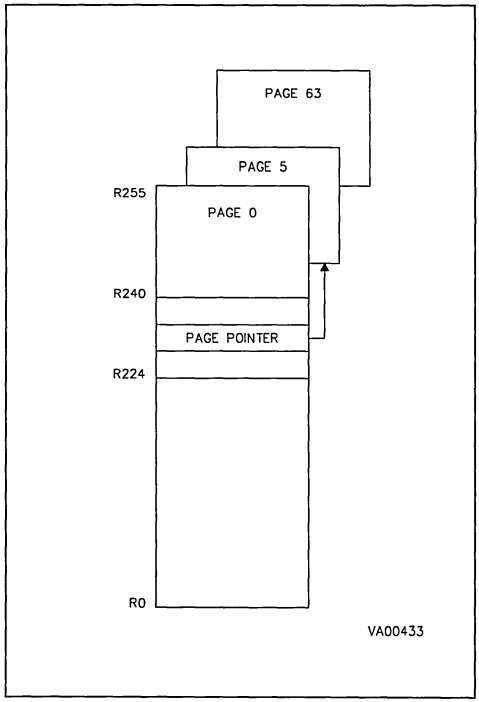
The register file is arranged into 16 groups of 16 registers, where the general purpose registers occupy the first 14 groups. The 15th group, E, contains the system registers and Group F contains the pages of the on-chip peripheral control registers.

Figure 7. Register Grouping



REGISTERS (Continued)

Figure 8. Page Pointer Mechanism



Group F is paged in this manner due to the modularity of the ST9 family of microcontrollers. Each member of the family retains all general purpose and system registers, only the paged register groups changing owing to the different on-chip peripheral organizations of each device. The user can therefore generate code libraries which use the general purpose registers knowing that they will not be lost on future ST9 devices. To address a paged register, the Page Pointer (PPR, R234) within the system register group must be loaded with the relevant page number using the SPP instruction. Subsequently any access to registers in the top group (R240-R255) will refer to the selected page. This remains set until the next change to the Page Pointer register (by the SPP instruction).

The System group (Group E, registers RE0 to REF) includes the system and user stack pointers, the Mode register, the ALU FLAG register and the Page pointer register. In addition the data registers for the first 5 I/O ports are present, the configuration registers for the ports being in the paged area. This allows the immediate access to the I/O ports at all times.

The Register Pointers, present in the system register group, select groups of registers as "Working Registers", which have faster addressing modes than direct Register addressing and allows smaller code size. The Register Pointers may either be used singly, creating a register group as 16 working registers, or as two independent groups of 8 working registers which may be placed at any 8 register boundary within the register file. The single and twin working register modes are automatically set by hardware when the respective SRP and either SRP0 or SRP1 instructions are executed. If working registers are used as accumulators and RAM locations for particular tasks, fast context switching on interrupts may be achieved by setting the register pointer to another group for the Interrupt Service Routine, ISR, (e.g. saving the Register pointer on the stack), using the new group in the ISR and subsequently restoring the original group before the return from Interrupt instruction. Working registers also allow the use of the ABAR - Any Bit-Any Register Boolean operations (including directly on the I/O port data registers).

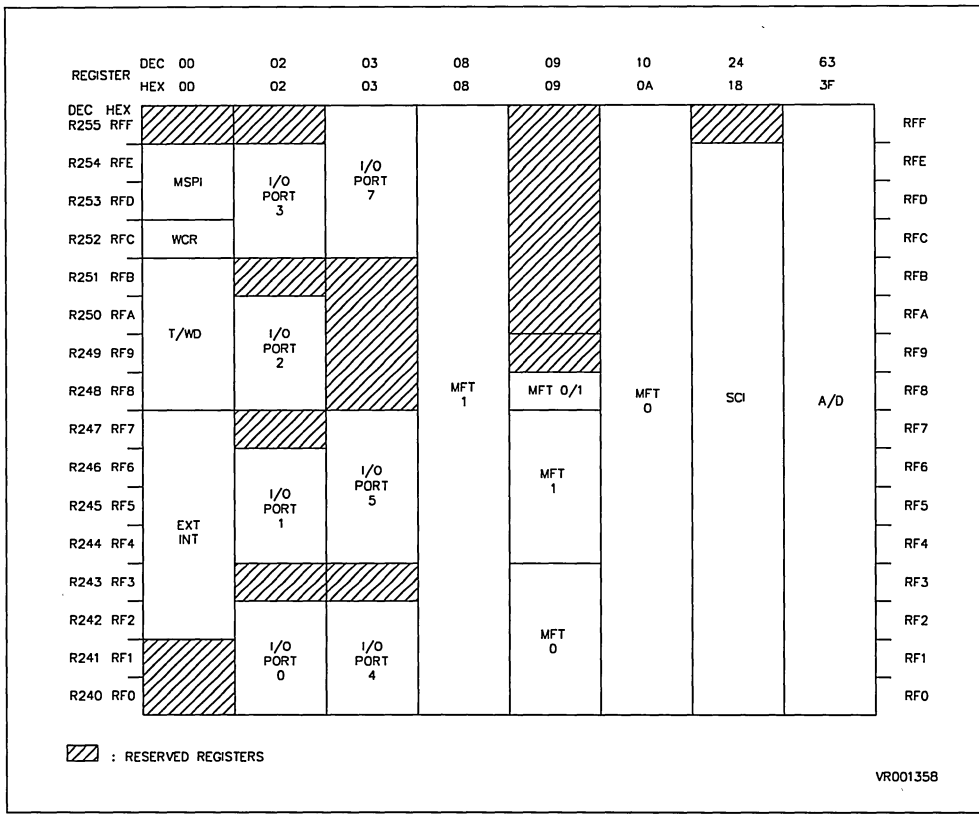
Table 2. Group E Register Map

R239	System Stack Pointer Low (SSPLR)
R238	System Stack Pointer High (SSPHR)
R237	User Stack Pointer Low (USPLR)
R236	User Stack Pointer High (USPHR)
R235	Mode Register (MODER)
R234	Page Pointer (PPR)
R233	Register Pointer 1 (RP1R)
R232	Register Pointer 0 (RP0R)
R231	ALU Flags (FLAGR)
R230	Central Interrupts Control (CICR)
R229	Port 5 Data (P5DR)
R228	Port 4 Data (P4DR)
R227	Port 3 Data (P3DR)
R226	Port 2 Data (P2DR)
R225	Port 1 Data (P1DR)
R224	Port 0 Data (P0DR)

REGISTERS (Continued)

In the ST9 syntax, directly addressed Registers are indicated with a capital R e.g. R0, R224, RBF, with Register Pairs (16 bit accumulators or memory pointers) as RR0, RR24. When using Working Registers, groups of 16 registers (SRP instruction) are denoted as r0 to r15 (rr0 to rr14), while the dual working register group are addressed as r0 to r7 (rr0 to rr6), for the first group of 8 registers (SRP0), with r8 to r15 (rr8 to rr15) for the second set (SRP1). Working register addressing requires a 4 bit field within the instruction. When packed into a byte, the upper nibble is set to Dh (1101b), this being the escape code to indicate the use of the working registers. As a result, group D CANNOT be selected with direct register addressing, it is recommended that this group be used as internal stacking area when using register file based system or user stack pointers.

Figure 9. ST9040 Group F Peripheral Organisation



REGISTERS (Continued)

Figure 10. Single Working Register Bank

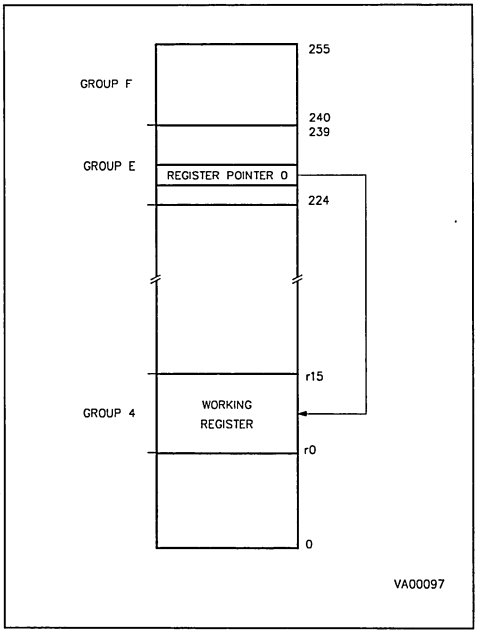
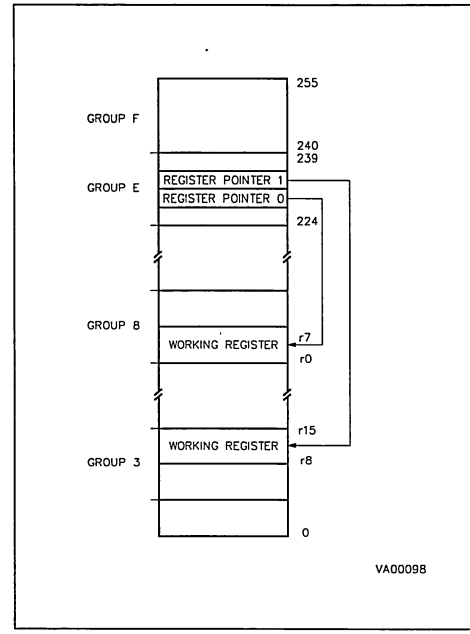


Figure 11. Dual Working Register Banks



STACK POINTERS

There are two separate, double register stack pointers available (System and User), both of which can operate in register or Data memory address spaces. These operate in a Pre-Decrement mode when data is PUSHed onto the Stack and in a Post-Increment mode when data is POPed from the stack.

The SYSTEM Stack Pointer (SSPR, R238:R239) is used for the storage of temporarily suspended system and/or control registers (ie the the Program Counter and FLAG register) while interrupts are being serviced, and is used for the storage of the Program Counter following the CALLing of a subroutine. The USER Stack Pointer (USPR, R236:R237) is completely free from all interference from automatic operations and so provides for a totally user controlled stack area.

Both Stack pointers may operate with both byte (PUSH, POP) and word (PUSHW, POPW) data, and are differentiated by appending a "U" to the instruction mnemonic for the User Stack (PUSHU/PUSHUW, POPU/POPUW).

When the Stack Pointers are using RAM Memory as the stack areas, a full word register is used as the pointer, while when operating with the stack area within the Register File (Groups 0 to 14 only, but not the within the system and paged groups) only an 8 bit register is required for addressing and consequently only the low byte of the word registers are used (R239 for the System Stack and R237 for the User Stack). In this latter case the upper byte of the stack pointer registers (R238 and R236) must be considered as reserved.The Stack Pointers may be selected to point to RAM or Register File by the setting of the SSP (MODER.7) and USP (MODER.6) of the ST9040 configuration register (MODER, R235) where a 1 denotes Register file operation (Default at Reset) and 0 causes Data space operation.

STACK POINTERS (Continued)

Figure 12. Internal Stack Pointers

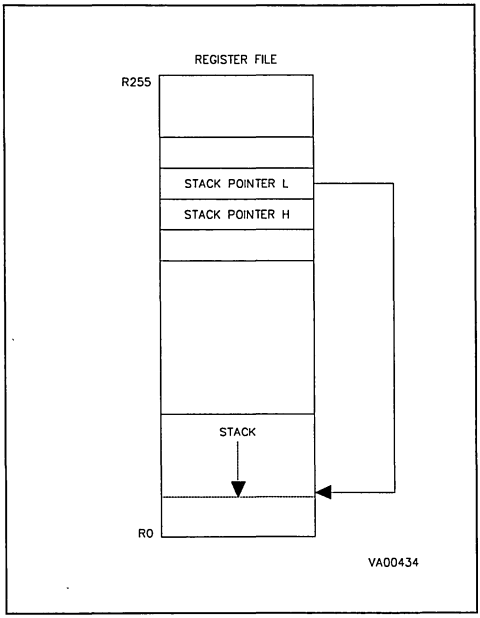
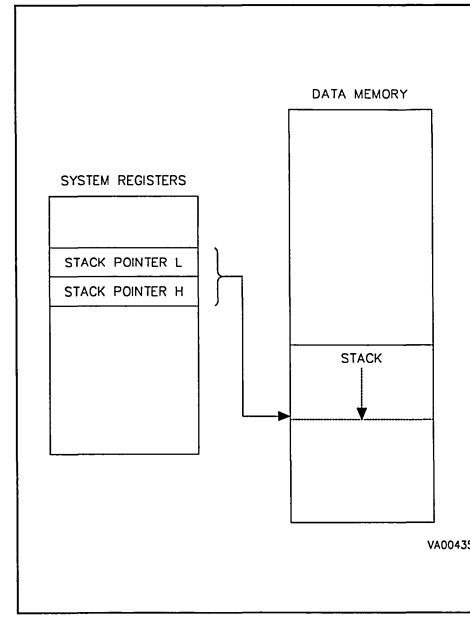


Figure 13. External Stack Pointers



INTERRUPTS

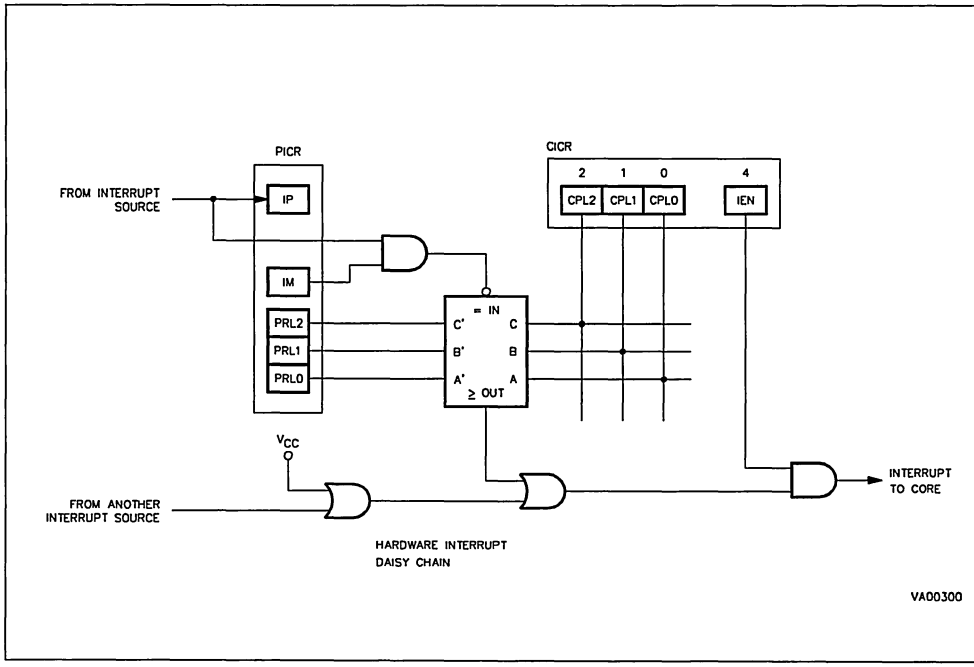
The ST9040 offers a powerful solution to the response requirements of real-time systems with its advanced interrupt structure. Interrupt trigger sources can be prioritized within 8 levels to match the priorities assigned to the application. In addition a top-level or non-maskable interrupt is available. The ST9040 interrupts follow the logical flow of Figure 14.

Interrupt events (selectable with each function) cause the setting of the Interrupt Pending (IP) bit within the status register of the peripheral. This bit may also be set by software in order to generate a software interrupt, and should normally be reset by software within the interrupt service routine. If the interrupt is not Masked with the corresponding Interrupt Mask bit, the interrupt is passed to the central interrupt control logic where the priority level assigned by the programmer to the interrupt source is compared with the priority level of the core (user programmed dynamically in the 3 bits of the Central Priority register (CPL, CICR.0-2, Level 7 is the lowest priority and level 0 the highest). If the incoming priority level is higher than the CPL, and Global Interrupts are enabled (by the `EI` instruction, interrupts are disabled by the execution of the `DI` instruction), the interrupt is acknowledged. If interrupts are globally disabled, the priority level of the source is lower than or equal to the CPL or the Interrupt is masked, then the IP bit remains set and the interrupt is held pending until the `EI` instruction is executed, the CPL is set to a lower level AND the interrupt is un-masked. Alternatively the IP bit of a masked interrupt source may be used in a polled interrupt environment, with the IP bit being reset by software within the service routine.

The interrupt acknowledge cycle causes the Program Counter and FLAGS register to be pushed onto the System Stack (PC low byte first, PC high byte, then FLAGS Register) and all maskable interrupts to be disabled by resetting the IEN bit (CICR.4). The peripheral Interrupt Vector, IVR, a user programmable feature of the peripheral interrupt control registers, is used as an offset into the

INTERRUPTS (Continued)

Figure 14. Interrupt Logic



vector table, pointing to the high byte (even address) of the 16 bit address which should contain the starting address of the interrupt service routine. Addresses 0 through 255 of the program space comprise the interrupt vector table. Where multiple interrupt sources may occur within a peripheral, the peripheral interrupt vector source may be encoded by hardware set bits within the IVR register. This means that the vector address defined in the peripheral IVR is the base address for a block of vectors servicing that peripheral. The address pointed to by the vector is loaded into the Program Counter and execution restarts from this point.

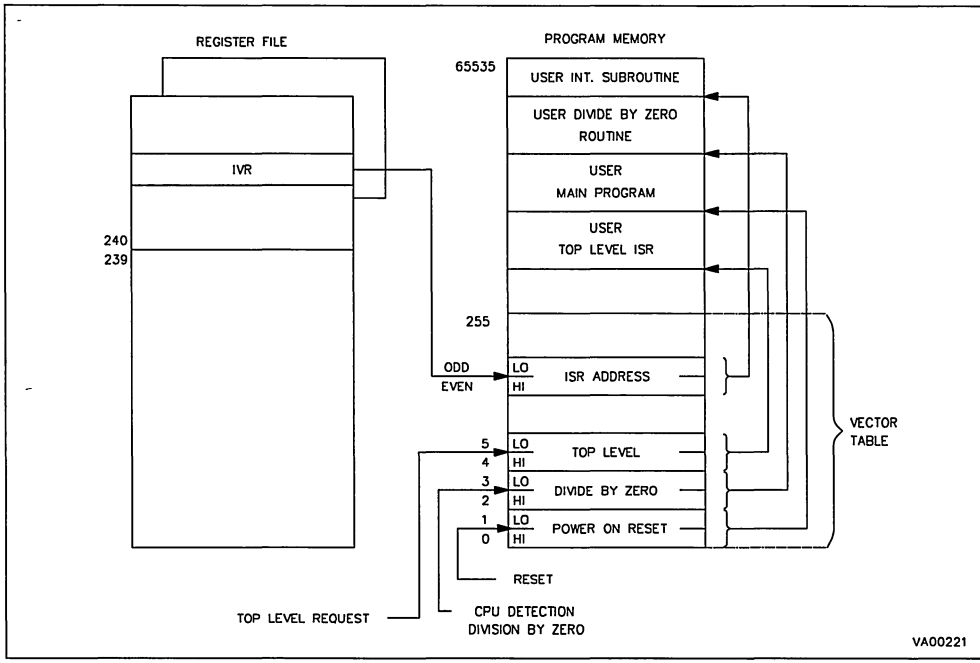
The interrupt service routine should clear the interrupt pending flag of the interrupt source and take the appropriate action. The last instruction of the interrupt service routine should be the `IRET` instruction, the action of this is to restore the Program Counter and Flags register to their value prior to the interrupt acknowledgment, and to re-enable interrupts. Within the interrupt service routine, use may be made of the working register pointer mechanism to reduce the context switching time.

Two interrupt arbitration modes are available for use with the 8 level priority scheme, Nested and Concurrent modes. These are selected by the status of the IAM bit (CICR.3).

Concurrent mode, selected when IAM = 0 (the reset condition) is the standard interrupt arbitration mode, where the arbitration phase of every instruction acknowledges interrupts according to their priority level (if higher than the CPL) and follows the sequence shown above. All pending interrupts existing or having eventually occurred during interrupt service routine execution, remain pending until the Enable Interrupt instruction (`EI`) (even if it is executed during the interrupt service routine). `EI` within the interrupt service routine is not recommended for use with the Concurrent arbitration mode as this can trigger a Last In, First Out condition where high priority interrupts are masked by lower priority interrupts which are all higher than the CPL value.

INTERRUPTS (Continued)

Figure 15. Interrupt Vector Table Usage



Nested Mode, selected when IAM = 1, uses the same arbitration phase as concurrent mode, the difference being that the CPL is modified during the interrupt processing cycle to that of the acknowledged interrupt level. The CPL value is pushed by hardware into the Nested Interrupt Control register (NICR, R247 page 0) by setting the NICR bit corresponding to the CPL value. The interrupt service routine is entered in the normal manner. The revised CPL level is used for arbitration of further interrupts, each higher level being saved on the NICR stack, and being restored automatically by hardware with the `RETI` instruction. This allows the execution of the `EI` instruction within the interrupt service routine to operate the correct nesting of interrupts. The two modes are shown graphically in Figure 16, where the Y axis shows the CPL value. It should be noted that the INT1 will not be acknowledged until the CPL level is programmed to a lower level.

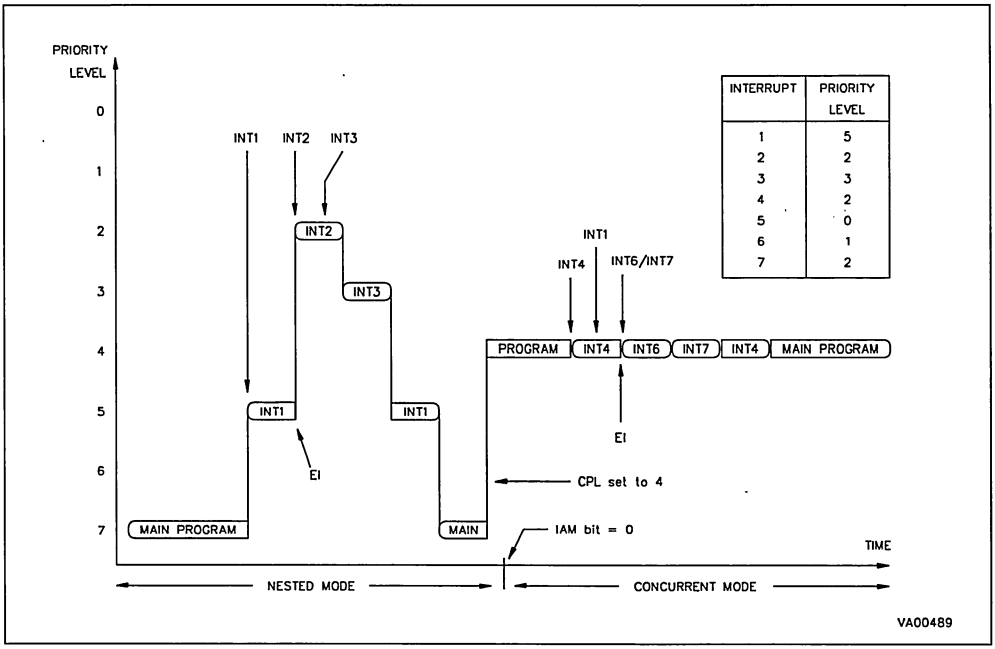
Interrupts coming from on-chip sources at the same instant are resolved during the arbitration phase according to a hardware daisy-chain. This follows the priorities of the table 3.

Table 3. ST9040 Interrupt Hardware Daisy Chain

INTA	High Priority
INTB	Lowest Priority
INTC	
INTD	
MFTIMER0	
SCI	
A/D	
MFTIMER1	

INTERRUPTS (Continued)

Figure 16. Interrupt Modes Example of Usage



External Interrupts. Up to 8 external interrupts are available on the ST9040 as alternate function inputs of I/O pins. These may be selected to be triggered on rising or falling edges and can be independently masked. The eight interrupt sources are grouped into four pairs or channels which can be assigned to independent interrupt priority levels.

Within each channel the even interrupt number takes the even priority level and the odd channel the odd priority level (even+1).

Several of the External Interrupt channels have their inputs selectable between the external interrupt source and on-chip peripheral sources.

Table 4. External Interrupt Channel Grouping

External Interrupt	Channel
INT7 INT6	INTD1 INTD0
INT5 INT4	INTC1 INTC0
INT3 INT2	INTB1 INTB0
INT1 INT0	INTA1 INTA0

Table 5. ST9040 External Interrupt Source Selection

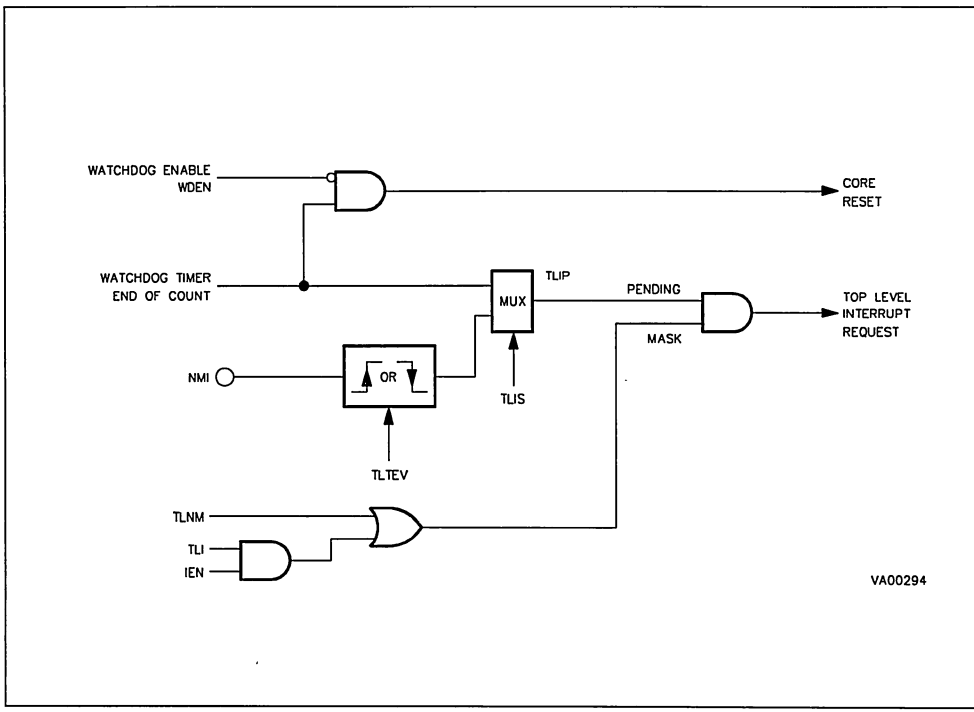
INT0	INTA0
Timer/Watchdog End of Count	
INT2	INTB0
SPI Interrupt	
INT4	INTC0
EEPROM Interrupt	

INTERRUPTS (Continued)

Top Level Interrupt. The Top Level Interrupt channel can be assigned either to the external NMI pin or to the Timer/Watchdog output. When selected as the external NMI pin, the active edge may be programmed to be rising or falling. The TLI event will cause the setting of the TLIP bit (CICR.6) and according to the mask situation, a Top Level Interrupt request may be generated. Two masking conditions are available, a Maskable Mask and a Not-Maskable Mask.

The Maskable Top Level Interrupt may be enabled or disabled by software and follows the state of the Global Interrupt Enable bit IEN (CICR.4), while the Not-Maskable Mask bit (TLI, CICR.5) is a set-only mask. Once set, the Top Level Interrupt is active independently of IEN and cannot be disabled until the next Reset cycle.

Figure 17. Top-Level Interrupt Structure



DMA

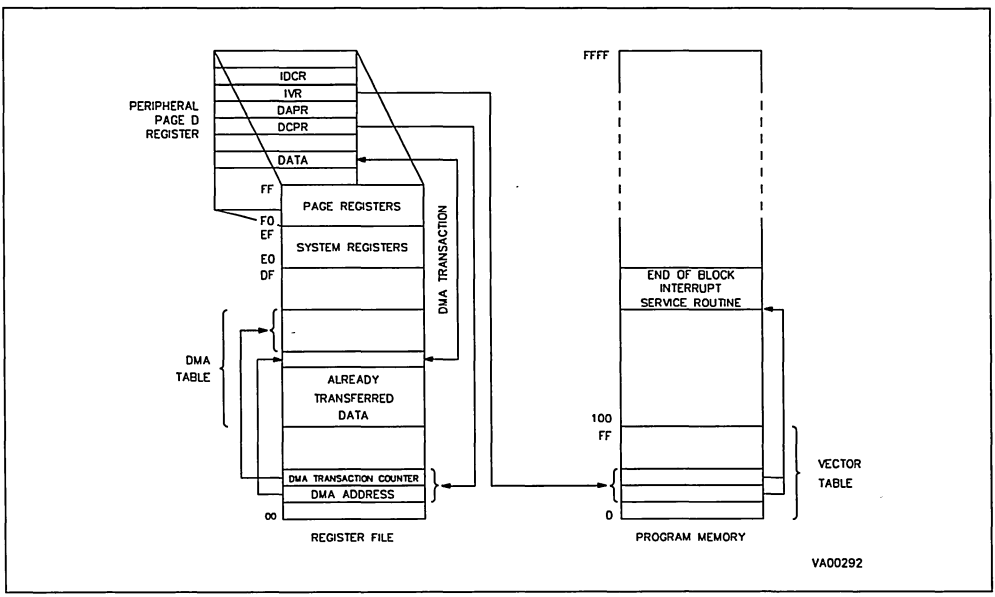
The ST9040 has on-chip DMA channels to provide high-speed data transaction between peripherals and Memory or Register File. Multi-channel DMA is fully supported because each peripheral can have its own DMA channel(s). Each DMA channel transfers data to/from contiguous locations of the Register File, Program Memory or Data Memory. The maximum number of transactions that each DMA channel can perform is 222 if the Register File is selected and 65536 if Program or Data Memory are selected.

DMA transfer to (or from) the Register File takes 8 INTCLK cycles, DMA transfer to (or from) Memory takes 16 INTCLK cycles. If the ST9040 is in the idle mode (following the execution of the `WFI` instruction), DMA requests are acknowledged according to their priority and control is returned to the idle mode pending an interrupt, this operation increases the number of INTCLK cycles by 2 for both Register File and Memory DMA transactions.

Each DMA channel has its own control registers located in the page(s) related to the peripheral. There are two pointer registers, DAPR which points to a register or register pair containing the current DMA address to/from which data will be transferred, and DCPR, which points to a register or register pair which contain the transaction counter for the DMA operations. Each DMA transfer consists of three operations:

- A load from/to the peripheral data register to a location of Register File (or Memory) addressed through the DMA Address Register (or Register Pair)
- A post-increment of the DMA Address Register (or Register Pair)
- A post-decrement of the DMA transaction counter, which contains the number of transactions that have still to be performed.

Figure 18. DMA Between Registers and Peripheral



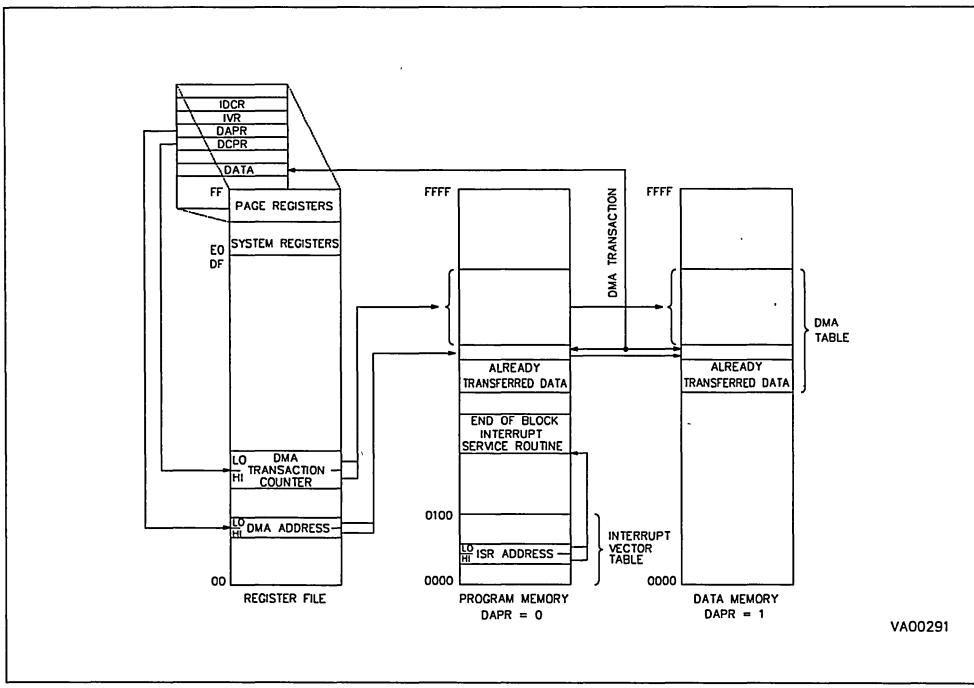
DMA (Continued)

When the transaction counter reaches 0 (all data has been transferred) an End of Block Interrupt is generated to allow the processing of the DMA data block, or, by reloading the Address and counter registers and retriggering, a repeated DMA cycle.

A SWAP mode, allowing continuous DMA operation, is available for the Multifunction Timer and is described in the section relating to the Multifunction Timer.

The ST9040 has DMA channels associated with the Serial Communications Interface Input and Output Serial data channels, the 16 bit Load/Capture Register 0, CAPT0R, of each Multifunction Timer allowing the timing of external signals to be captured into a table for off-line analysis or for the automatic output of PWM signals of variable width and timing, and the 16 bit Comparison Register 0, COMP0R, of each Multifunction Timer which can be programmed to cause output or input of parallel data through the handshake port 5 under DMA.

Figure 19. DMA Between Memory and Peripheral



CLOCK GENERATION, WAIT, HALT AND RESET

Clock Generation

The ST9040 Clock Generator module generates the internal clock for the ST9 core and the on-chip peripherals, it may be driven by an external quartz crystal circuit, connected to the OSCIN and OSCOUT pins, or by an external pulse generator connected to OSCIN (Figure 19, Figure 20).

The conceptual schematic of the ST9 internal clock circuit is shown in Figure 21.

The maximum external frequency of the ST9 is 24MHz, while the maximum internal operating frequency is 12MHz, thus a programmable divide by two circuit is present, this allows the use of high frequency crystals for economy, or low frequency crystals for reduction in radiated noise. This divider is active upon exit from the reset condition, the user may bypass the divide by two circuit by setting the DIV2 bit (MODER.5).

Figure 19. Crystal Oscillator

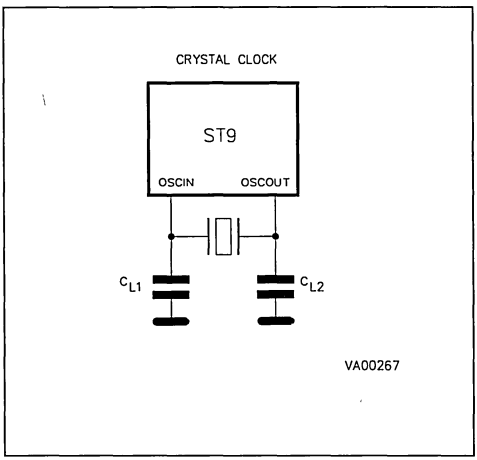


Figure 20. External Oscillator

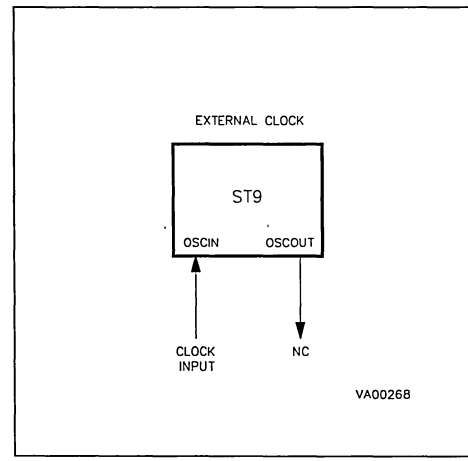
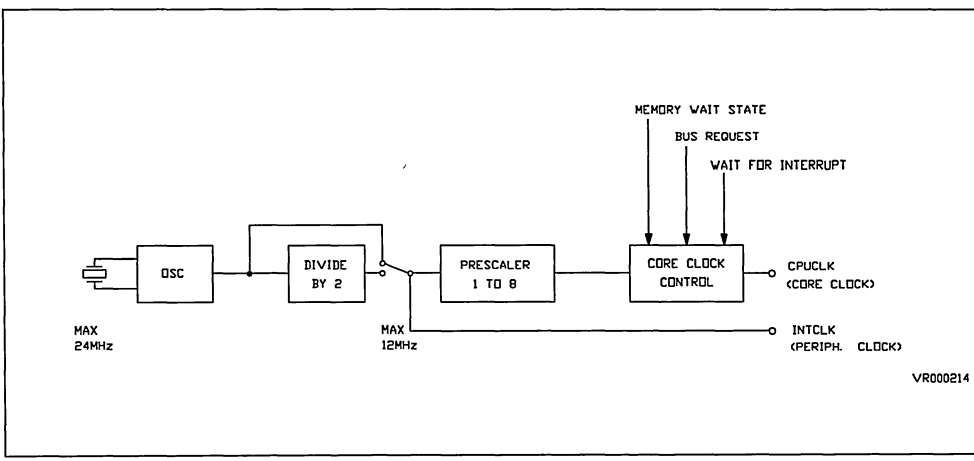


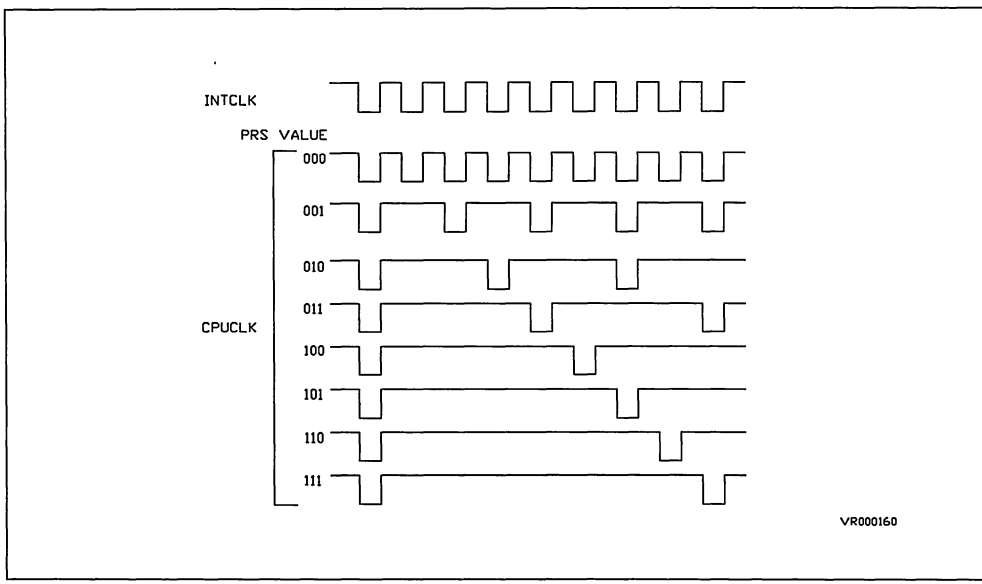
Figure 21. Internal Clock Circuit



CLOCK GENERATION, WAIT, HALT AND RESET (Continued)

The resulting clock from this section is named INTCLK, the internal clock which drives the time-bases of the on-chip clock for the ST9040 peripherals (eg the Multifunction Timer, Timer/Watchdog, Serial Communications Interface) and also the input of the CPU prescaler section. The CPU of the ST9 includes the instruction execution logic and may run at different rates according to the setting of the PRS2, PRS1 and PRS0 bits (MODER.4-2) (Figure 22). The resulting clock is named CPUCLK and it should be noted that this does not maintain a 50% duty cycle, but stretches the high level of the clock until completion. The CPUCLK prescaler allows the user to slow down the program execution time (eg for lower power consumption), while time-critical sections of the program may tune the CPUCLK execution speed to high speed and then restore it to its original speed.

Figure 22. CPUCLK Prescaler



CLOCK GENERATION, WAIT, HALT AND RESET (Continued)

Wait States

The output from the prescaler can also be affected by wait states. Wait states from two sources allow the user to tailor timing for slow external memories or peripherals.

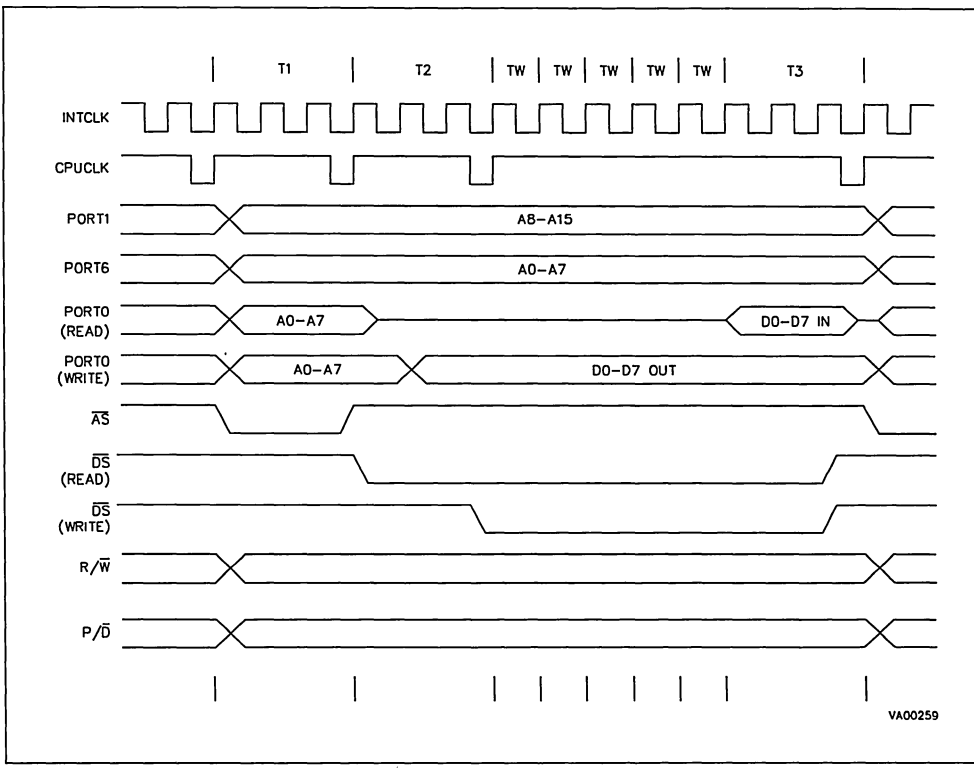
The internal Wait State generator will insert from 0 to 7 wait states, independently programmable for both Program and Data Spaces via the Wait Control Register WCR (R252, page 0). The second source of wait states is the external Wait input pin when enabled as the Alternate Function. Figure 23 shows the External Memory Interface timing as it relates to CPUCLK prescaling of 2 and 5 added wait states. The added wait states are derived from the INTCLK clock cycle, not CPUCLK. Internal memory is always accessed with no Wait states.

Halt And Wait For Interrupt (WFI) States

The schematic of the on-chip oscillator circuit is shown in Figure 24. The HALT condition, caused by the execution of the HALT instruction, disables the oscillator, forcing OSCOUT high. This places the ST9040 into the lowest power mode. The exit of the HALT condition and the restarting of the oscillator requires a RESET pulse with a minimum duration of 10ms (Figure 25). It must be noted that if the TIMER/WATCHDOG has the WATCHDOG mode enabled, a `HALT` instruction will not disable the oscillator; this is to avoid stopping the Watchdog if, by an error, a `HALT` instruction is executed.

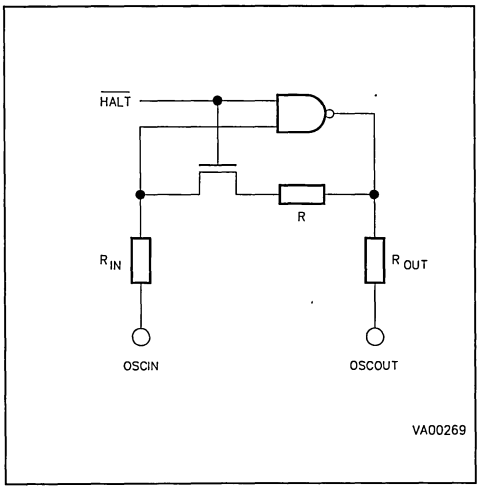
When this occurs, the ST9040 runs in an endless loop ended by the Watchdog reset.

Figure 23. External Memory Interface Timing with CPUCLK Prescaling and 5 Added Wait States



CLOCK GENERATION, WAIT, HALT AND RESET (Continued)

Figure 24. Oscillator Schematic

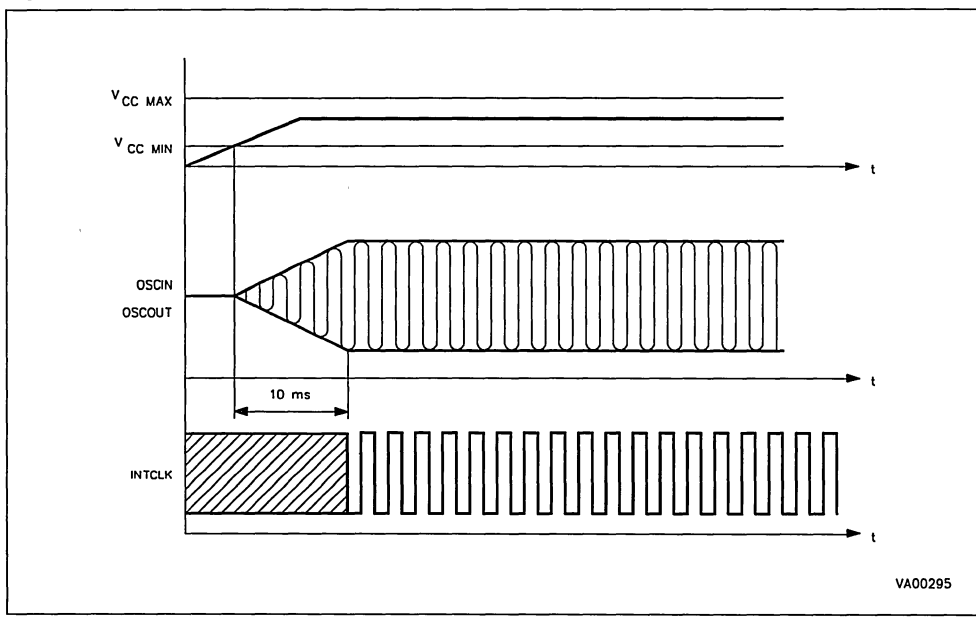


The WFI (Wait for Interrupt) instruction suspends program execution until an interrupt request is acknowledged. During this period, DMA transactions are allowed if their priority is higher or equal to the CPL level, the ST9040 returns to WFI mode after completion of the DMA transfer. The CPUCLK is halted during Wait For Interrupt while INTCLK continues to run, thus the power consumption of the processor is lowered by the CORE power consumption value. The External Memory Interface lines status during HALT and WFI modes is shown in Table 6.

Table 6. External Memory Interface Line Status During WFI and Halt

P0 (AD0-AD7)	High Impedance
P1 (A8-A15)	Forced to Address of Next Opcode
$\overline{AS}$	Forced High
$\overline{DS}$	Forced High
R/$\overline{W}$	Forced High

Figure 25. Reset Timing Requirements from Halt State



RESET

The processor Reset overrides all other conditions and forces the ST9040 to the reset state. During Reset, the internal registers are set to their Reset values, as shown in Table 7 for the system and Page 0 Registers. The I/O Ports pins are set to the Bidirectional Weak Pull-up mode. The programmer must then initialize the ST9040 registers to give the required functions.

The Reset condition can be generated from the external $\overline{\text{RESET}}$ pin or by the on-chip TIMER/WATCHDOG operating in Watchdog mode. To guarantee the complete reset of the ST9040, the $\overline{\text{RESET}}$ input pin must be held low for at minimum of 53 crystal periods in addition to the crystal start-up period. The Watchdog $\overline{\text{RESET}}$ will occur if the Watchdog mode is enabled (WDEN, WCR.6, is reset) and if the programmed period has elapsed without the code 0AAh,55h written to the appropriate register. The input pin $\overline{\text{RESET}}$ is not driven low by the on-chip reset generated by the TIMER/WATCHDOG.

During the RESET state, $\overline{\text{DS}}$ is held low and $\overline{\text{AS}}$ is toggled with the frequency of the crystal (OSCIN) divided by 32. This condition may be recognized by external peripherals as a Reset condition. It may also be used to enable the synchronization of multiple ST9040 running from the same clock in a multi-processing or high security majority voting system.

Once the $\overline{\text{RESET}}$ pin reaches a logical high, the ST9040 fetches the starting address from locations 0 and 1 of the program space and begins program execution from this address after 67 crystal cycles.

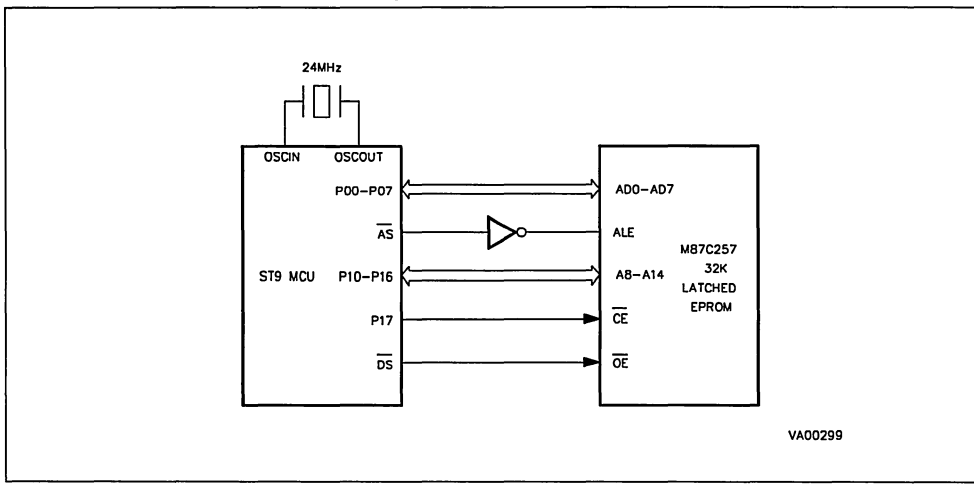
Table 7. System and Page 0 Reset Values

Register Number	System Register Reset Value	Page 0 Register Reset Value
F	(SSPLR) = undefined	Reserved
E	(SSPHR) = undefined	(SPICR) = 00h
D	(USPLR) = undefined	(SPIDR) = undefined
C	(USPHR) = undefined	(WCR) = 7Fh
B	(MODER) = E0h	(WDTCR) = 12h
A	(Page Ptr) = undefined	(WDTPR) = undefined
9	(Reg Ptr 1) = undefined	(WDTLR) = undefined
8	(Reg Ptr 0) = undefined	(WDTHR) = undefined
7	(FLAGR) = undefined	(NICR) = 00h
6	(CICR) = 87h	(EIVR) = x2h
5	(PORT5) = FFh	(EIPLR) = FFh
4	(PORT4) = FFh	(EIMR) = 00h
3	(PORT3) = FFh	(EIPR) = 00h
2	(PORT2) = FFh	(EITR) = 00h
1	(PORT1) = FFh	(EEPROM) = xx00 0000b
0	Reserved	Reserved

INTERFACING TO EXTERNAL MEMORY

External Memory and/or peripherals may be connected to the ST9040 through its External memory interface. This provides the multiplexed Address bits A0 to A7 and Data bits D0 to D7 as Alternative Functions of Port 0, and the higher order address bits A8 to A15 as Alternative Functions of Port 1, giving the full 64K bytes addressing capability. The Program/Data (P/$\overline{D}$) output, when selected as an Alternate function, allows external decoding to provide for the two independent pages of 64K bytes for Program and Data. Data transfer timing is generated by the Address strobe $\overline{AS}$ and the data strobe $\overline{DS}$. Address strobe low indicates that the data present on AD0 to AD7 is the low order address and is guaranteed valid on the rising edge of $\overline{AS}$ allowing for latching of the address bits by an external latch. Data transfer direction is indicated by the status or the Read/Write (R/$\overline{W}$) pin, for write cycles (R/$\overline{W}$ low), data out is valid at the falling edge of $\overline{DS}$, for read cycles (R/$\overline{W}$ high), data in must be valid prior to the rising edge of $\overline{DS}$. The Data Strobe low period may be extended to accomodate slow external devices by the adding of internally generated wait cycles (0 to 7 cycles for both program and data memory maps) or by an external input on the $\overline{WAIT}$ input pin also available as an Alternative Function of an I/O bit. Suggested interface circuits are shown in Figure 26.

Figure 26. External Memory Addressing Circuit



BUS CONTROL

Multi-processing or external program testing may be accomplished by disabling the I/O ports used for external memory addressing and the associated timing signals.

High Impedance Mode

The programmer may place the External Memory Interface (I/O ports 0 and 1, Address Strobe, Data Strobe and Read/Write) into the high impedance state by setting the HIMP bit (MODER.0). External test equipment may then drive the memory lines for automatic test, external memory validation or programming. The ST9 will continue to execute internal programs, providing no external memory is addressed, allowing the execution of security routines without showing the externally the addresses used.

Bus Request/acknowledge

The External Memory Interface address ports and timing signals may be forced to their high impedance state by utilizing the $\overline{BUSREQ}$, Bus Request, and $\overline{BUSACK}$, Bus Acknowledge, signals available as Alternate Functions of two I/O pins (please refer to the pin configuration drawings for availability of these lines for the package chosen). The signals, $\overline{BUSREQ}$ and $\overline{BUSACK}$, must be enabled by setting the BRQEN bit (MODER.1).

Once enabled, a low level detected on the $\overline{BUSREQ}$ pin at the start of an internal machine cycle will cause the stretching of the CPUCLK, and $\overline{BUSACK}$ to go low indicating that the External Memory Interface is disabled. The $\overline{BUSREQ}$ pin is then continuously monitored, and when sampled high, the External Memory Interface pins are driven by the ST9 within two INTCLK cycles.

EEPROM

The EEPROM of the ST9040 has been implemented in a high reliability technology developed by SGS-THOMSON, this, together with the double bit structure, allow the 300k Erase/Write cycles and 10 year data retention to be achieved on a microcontroller.

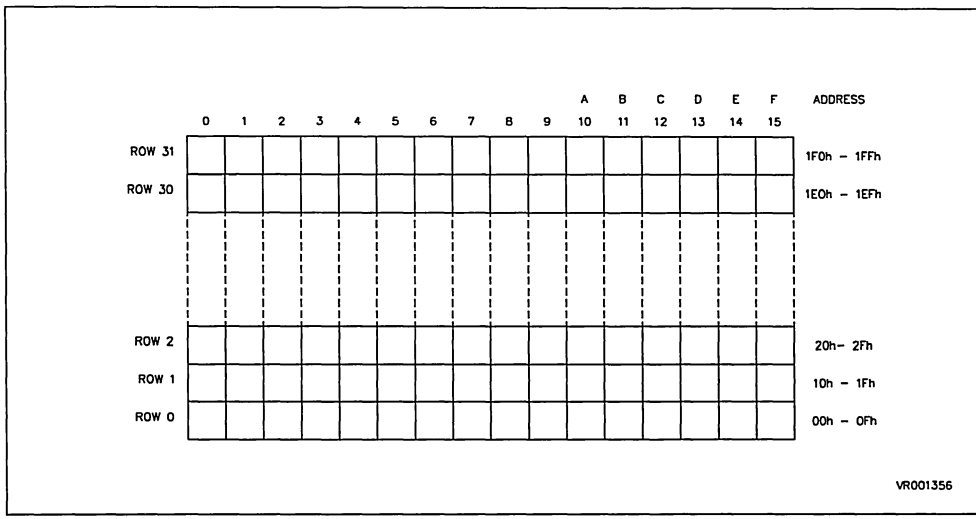
Control of the EEPROM is performed through one register mapped at register address R241 in Page 0. The EEPROM memory is read as normal RAM memory at Data Space addresses 0 to 1FFh, while a byte write cycle to the EEPROM will cause the start of an ERASE/WRITE cycle at the addressed location. The programming cycle is self-timed, with a typical programming time of 6 msec. The voltage necessary for programming the EEPROM is internally generated with a +18V charge pump circuit. Word (16 bit) writes are not allowed.

The EEPROM ENABLE bit EEWEN must first be set before writing to the EEPROM. When this bit is low, attempts to write data to the EEPROM have no affect, this prevents any spurious memory accesses from affecting the data in the EEPROM.

Termination of the write operation can be detected by polling on the BUSY status bit, or by interrupt, taking the interrupt vector from the External Interrupt 4 channel. The selection of the interrupt is made by EEPROM Interrupt enable bit IEN. It should be noted that the Mask bit of External Interrupt 4 should be set, and the Interrupt Pending bit reset, before the setting of IEN to prevent unwanted interrupts. A delay (eg a NOP instruction) should also be included between the operations on the mask and pending bits of External Interrupt 4. If polling on BUSY is used, a delay of 6 INTCLK clock cycles is necessary after the end of programming, this can be a NOP instruction or, normally, the required time to test the BUSY bit and to branch to the next instruction will be sufficient. While BUSY is active, any attempt to access the EEPROM matrix will be aborted and the data read will be invalid. BUSY is a read only bit and cannot be reset by the user if active.

Up to 16 bytes of data may be programmed into the EEPROM during the same write cycle by using the PARALLEL WRITE function. The constraint is that each of the bytes occur in the same ROW of the EEPROM memory (A4 constant, A3-A0 variable), Figure 27. To operate this mode, the Parallel Mode enable bit, PLLEN, must be set. The data written is then latched into buffers (at the addresses specified, which may be non-sequential) and then transferred to the EEPROM memory by the setting of the PLLST bit of the control register. Both PLLST and PLLEN are internally reset at the end of the programming cycle. Any attempt to read the EEPROM memory when PLLEN is set will give invalid data. In the event that the data in the buffer latches is not required to be written into the memory by the setting of PLLST, the correct way to terminate the operation is to reset PLLEN and to perform a dummy read of the EEPROM memory. This termination will clear all data present in the latches.

Figure 27. EEPROM Row Mapping Structure



EEPROM (Continued)

An erased bit of the EEPROM memory will read as a logic "0", while a programmed cell will be read as a logic "1". For applications requiring the highest level of reliability, the Verify Mode, set by EEPROM control register bit VRFY, allows the reading of the EEPROM memory cells with a reduced gate voltage (typically 20%). If the EEPROM memory cell has been correctly programmed, a logic "1" will be read with the reduced voltage, otherwise a logic "0" will be read. A standby mode is also available which disables all power consumption sources within the EEPROM for low power requirements. When STBY is high, any attempt to access the EPPROM memory will produce unpredictable errors. After the re-enabling of the EEPROM (STBY = "0"), a delay of 6 INTCLK cycles must be allowed before the selection of the EEPROM.

SECURITY FEATURES

The ST9040 allows the prevention of external program sources from reading the on-chip memories through its Security Register. This allows the programmable disabling of the buffers between the on-chip memory and the external address and data lines and prevention of DMA from operation with internal memory sources.

Two levels of hardware protection are available allowing the user to select the level of security required in the application. Each memory element on-chip (ROM, RAM, EEPROM) has an independent protection enable selectable for each level.

The protection enable options are selectable by metal mask during manufacture and are activated by the programming of fuses present in the Security Register mapped at register 0FFh of I/O page 59 decimal (3Bh). These fuses are based on EEPROM technology and require a high voltage to program the fuse. In the ST9040, this is supplied by the charge pump present in the EEPROM memory, so that the EEPROM must be in an active state (STBY low), before security fuse programming is activated. The Security fuses are TESTLOCK (TLCK) and HARDWARE LOCK (HLCK). These are both one-time programmable, once these are programmed THE PROTECTION CANNOT BE DISABLED, so care must be made in the use of this feature.

Testlock

The TESTLOCK protection level may be programmed by SGS-THOMSON during the manufacturing cycle, if requested, or may be programmed by the user before the release of the end equipment. If programmed by SGS-THOMSON, the user must include in the masked ROM the routines to program the RAM and EEPROM. The Reset vector must also be provided. There is no possibility to test the ST9040, or to use external memory to program the RAM and EEPROM (unless a ROMLESS option is enabled), once this bit is programmed. The TLCK bit may also be programmed by the user after the internal read/write memory has been programmed. This may be achieved by using an external program with the ST9040 set into its test mode (consult SGS-THOMSON for further information).

The TESTLOCK level of protection allows the basic protection of the user-designated on-chip memory e.g. the ROM contents, while, optionally, allowing the further programming of the RAM and EEPROM memory from external programs.

Hardware Lock

The HARDWARE lock protection level is provided to give a final high security protection after the programming of the internal memory (e.g. access codes, serial numbers or PIN codes). If the on-chip memory has been mask selected for protection by this level, then the programming of the HLCK bit will give the full protection.

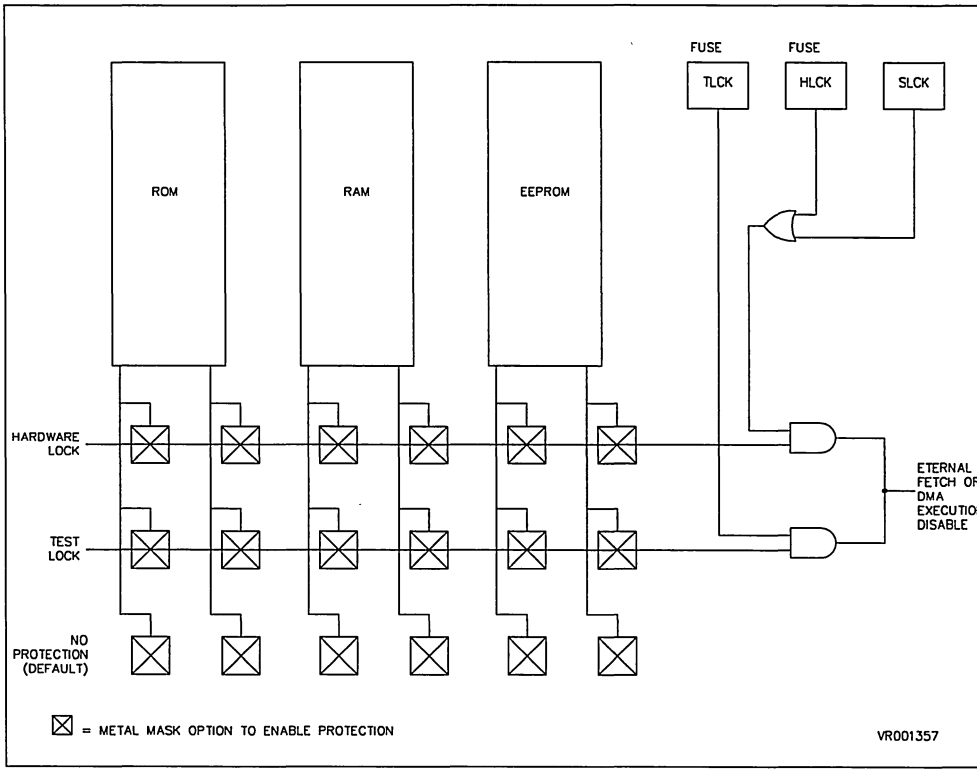
WARNING: THIS IS TOTAL PROTECTION, there is no method to access or test on-chip memory from any external source once this level is programmed.

A third fuse is present in parallel with HLCK, and is used by SGS-THOMSON as part of the final device check to test the security functions. This fuse bit is selected by setting F2TST, which can allow the verification of the hardware security protection before resetting F2TST to allow the programming of the Hardware lock.

When the Testlock and Hardware lock bits are virgin, the value read from the bits are the value previously written, allowing verification of the operation of the protection mechanism. The fuses are programmed by setting the appropriate Write Fuse bit (WF1 for TLCK and WF2 for HLCK) and making

SECURITY FEATURES (Continued)

Figure 28. ST9040 Security Mask Options



a dummy read from the EEPROM memory (STBY must be active). This triggers the charge pump to generate the high voltage necessary to program the fuse. The Write Fuse bits must be held to a "1" state for the whole of the programming cycle, the end of programming may be monitored on the TLCK or HLCK bit.

Software Lock

A third level of security may be achieved by the latching of a third bit, SLCK which provides an additional level of security in parallel with the Hardware lock. This is provided in the case of a failure, by externally induced means, of the EEPROM OTP hardware locks. It should also be noted that the ST9040 on-chip programmable memories (RAM and EEPROM) are mapped into Data Space, preventing the operation of "Trojan Horse" programs (external programs loaded into internal memory to bypass the read out protection), and that the High Impedance mode can be activated to prevent the external address lines of the ST9040 from echoing the addresses used by the internal security program.

I/O PORTS

Summary Of Function

For the ST9040, only twelve pins have a Reserved function: V_{DD}, V_{SS}, $\overline{RESET}$, $\overline{AS}$, $\overline{DS}$, R/$\overline{W}$, OSCIN, OSCOUT, the Analog to Digital Converter Voltage references, and the External Interrupt 0 and 7 input pins. All other pins are available as Input/Output (I/O) for the user, grouped into Ports of 8 bits.

These may be programmed to be Input, Output, Bidirectional or Alternate Function (Peripheral or Memory Interface), on a bit by bit basis, at any time. When programmed as an Input the pin may be set to TTL or CMOS input threshold levels, while, when programmed as Output, Push-Pull or Open Drain configuration may be selected. The Bidirectional mode sets the pin with a weak pull-up resistor to V_{DD} or to Open Drain, allowing bidirectional communication with external logic. The Alternate Function setting is predetermined for each pin as shown in the Pin Configuration Table. The circuitry of the I/O port allows for several ST9040 peripheral functions to address, as Alternate Functions, the same pin, for both input and output, the programmer selects which peripheral function is to be active by enabling its individual Input or Output function. This multi-function I/O capability of the ST9040 allows for easy adaptation to external circuits. The options available for each bit are summarized in Table 8.

Table 8. I/O Setting Options

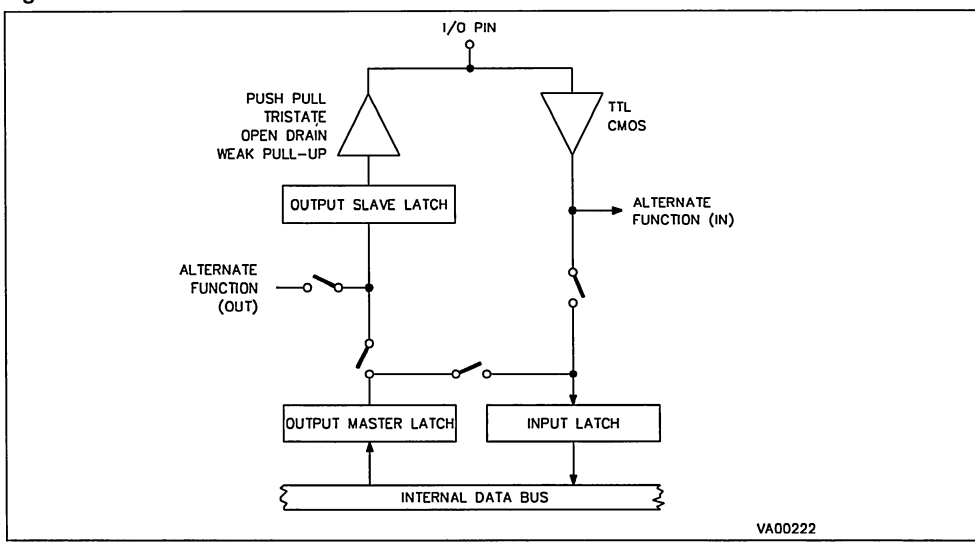
Input	TTL Thresholds
	CMOS Thresholds
Output	Open Drain
	Push-Pull
Bidirectional	Open Drain
	Weak Push-Pull
Alternate Function	Open Drain
	Push Pull

I/O Port Configuration

The configuration of each general I/O bit of the ST9040 is set by the corresponding bits in three I/O Port control registers. These affect the status of the input and output buffers of the pin, and enable the Alternate function Outputs. Alternate Function inputs are always connected, and are used by enabling the function from within the configuration registers of the relevant peripheral function.

The configuration of an I/O bit is shown in Figure 29. Outputs follow a Master/Slave buffer, data is transferred from the ST9 internal data bus at the beginning of the machine cycle, and, if enabled as output, is passed to the output latch at the end of the cycle. This synchronization allows for the Bidirectional use of the pin without potential conflicts.

Figure 29. I/O Port Schematic



I/O PORTS (Continued)

Configuration Registers. Three registers are used to allow the setting of each pin, generically PxC2R, PxC1R, PxC0R, where x relates to the 8 bit I/O port in which the bit is present. The setting of the corresponding bit in each register to achieve the desired functionality of the I/O pin is shown in Table 9.

The effect of the configuration settings of Table 9 on the I/O ports structure is shown in Figure 30.

Table 9. Port Configuration Status Bits

PxC2n	0	1	0	1	0	1	0	1
PxC1n	0	0	1	1	0	0	1	1
PxC0n	0	0	0	0	1	1	1	1
Pxn Configuration	BID	BID	OUT	OUT	IN	IN	AF	AF
Pxn Output	WP	OD	PP	OD	HI	HI	PP	OD
Pxn Input	TTL	TTL	TTL	TTL	CMOS	TTL	TTL	TTL

Legend:
x = Port
n = Bit
BID = Bidirectional
OUT = Output
IN = Input
AF = Alternate Function

WP = Weak Push-Pull
OD = Open Drain
PP = Push-Pull
HI = High Impedance
TTL = TTL Std Input
CMOS = CMOS Std Input

Figure 30. I/O Port Input Configuration

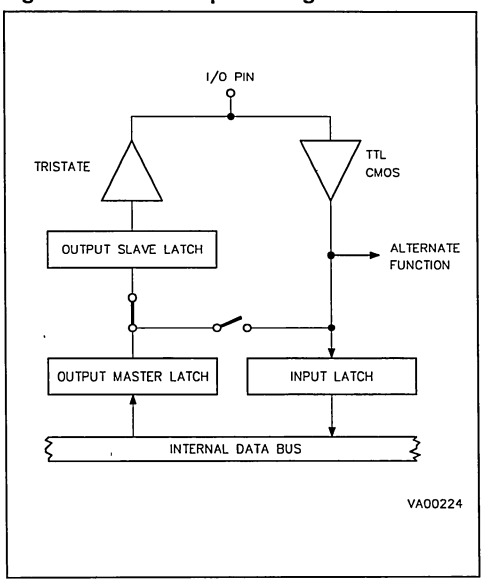
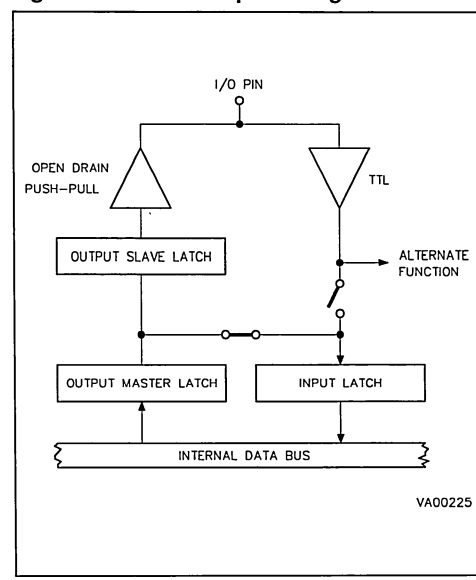


Figure 31. I/O Port Output Configuration



I/O PORTS (Continued)

Figure 32. I/O Bidirectional Configuration

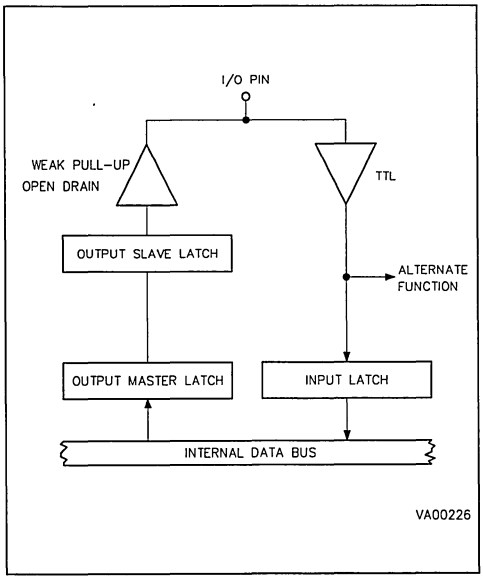
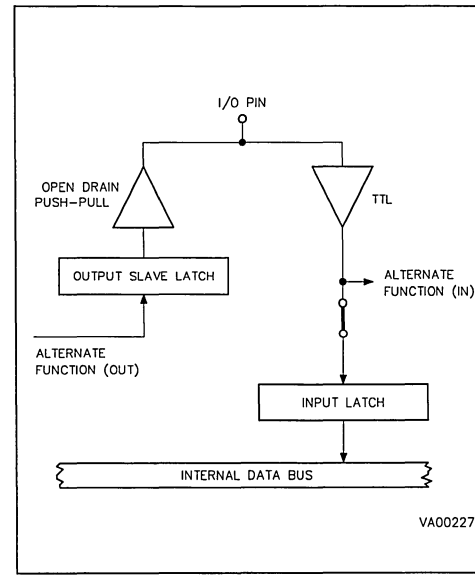


Figure 33. I/O Port Alternate Function Config.



I/O Register Map

The Data Registers which correspond to the pin status (after configuration) of I/O port 0 to 5, are found in Group E of the Register File, for immediate access at all times, while the configuration registers and the Data Registers for Additional Ports are found within I/O pages (Group F) 2 and 3.

Figure 34. I/O Register Maps

GROUP E			GROUP F		PAGE	
DEC	HEX		DEC	HEX	02	03
			R255	RFF	RESERVED	P7D
			R254	RFE	P3C2	P7C2
			R253	RFD	P3C1	P7C1
			R252	RFC	P3C0	P7C0
			R251	RFB	RESERVED	RESERVED
			R250	RFA	P2C2	RESERVED
			R249	RF9	P2C1	RESERVED
			R248	RF8	P2C0	RESERVED
			R247	RF7	RESERVED	HDC5
			R246	RF6	P1C2	P5C2
R229	RE5	P5D	R245	RF5	P1C1	P5C1
R228	RE4	P4D	R244	RF4	P1C0	P5C0
R227	RE3	P3D	R243	RF3	RESERVED	RESERVED
R226	RE2	P2D	R242	RF2	P0C2	P4C2
R225	RE1	P1D	R241	RF1	P0C1	P4C1
R224	RE0	P0D	R240	RF0	P0C0	P4C0

I/O PORTS (Continued)

Handshake and DMA

I/O Port 5 of the ST9040 is able to support a parallel interface port with handshake capability. This allows one, two or four wire interconnecting signals and facilitates very fast parallel transfer of data for input and output, or for the interconnection of peripheral devices requiring strobe signals for synchronization. Table 10 shows the available options for input and output status and strobe signals available as Alternate Functions of I/O port bits (see Pin Configuration). The Handshake configuration is set within the Handshake Control Register (HDCnR) for the relevant I/O port n.

Data transfer through the parallel I/O port with handshake can also be triggered through a DMA channel. Timing is generated by the ST9040 TIMER ON-CHIP EVENT strobe signal (see the MULTIFUNCTION TIMER section for information on generating these signals), which causes the programmed transfer of data to or from the memory source which can be Register File, Program space memory or Data space memory. An example of application of this technique is shown in Figure 35 a complex stepper motor timing sequence automatically being transferred from a table in the Register File (or memory spaces) to the stepper motor drivers. This operation being transparent, after initialization, until the task (complex microstepping) is completed.

Table 10. Handshake Control Signal Options

Mode	Handshake Lines	Names
Input to Port	1	WRRDY
	2	$\overline{\text{WRSTB}}$ WRRDY
Output from Port	1	RDRDY
	2	$\overline{\text{RDSTB}}$ RDRDY
Bidirectional	4	$\overline{\text{WRSTB}}$ $\overline{\text{WRRDY}}$ $\overline{\text{RDSTB}}$ RDRDY

Figure 35. Handshake + DMA Used for Stepper Motor Driving

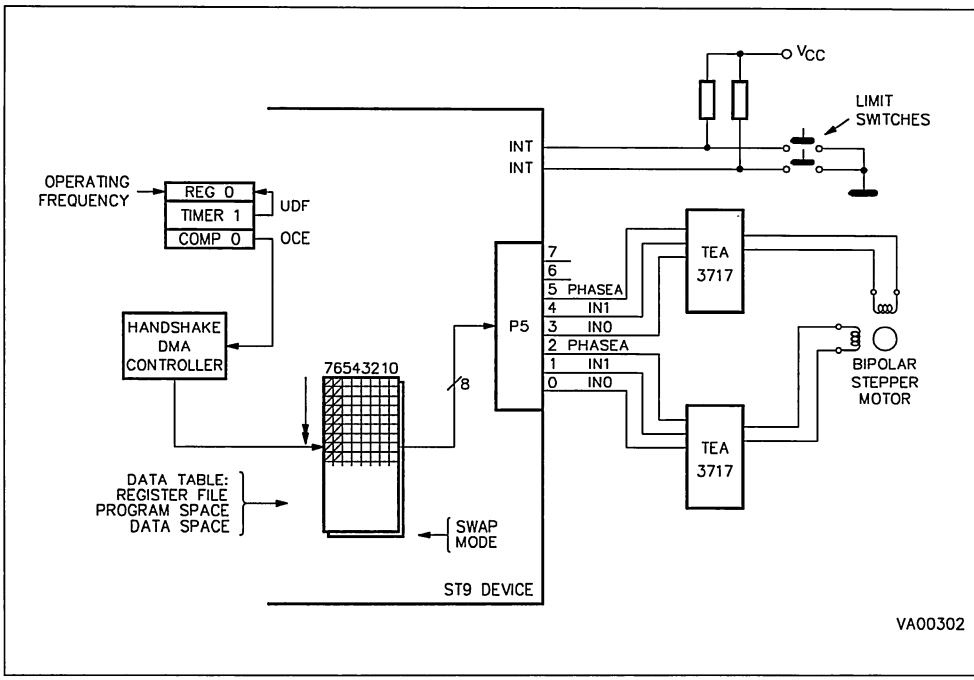
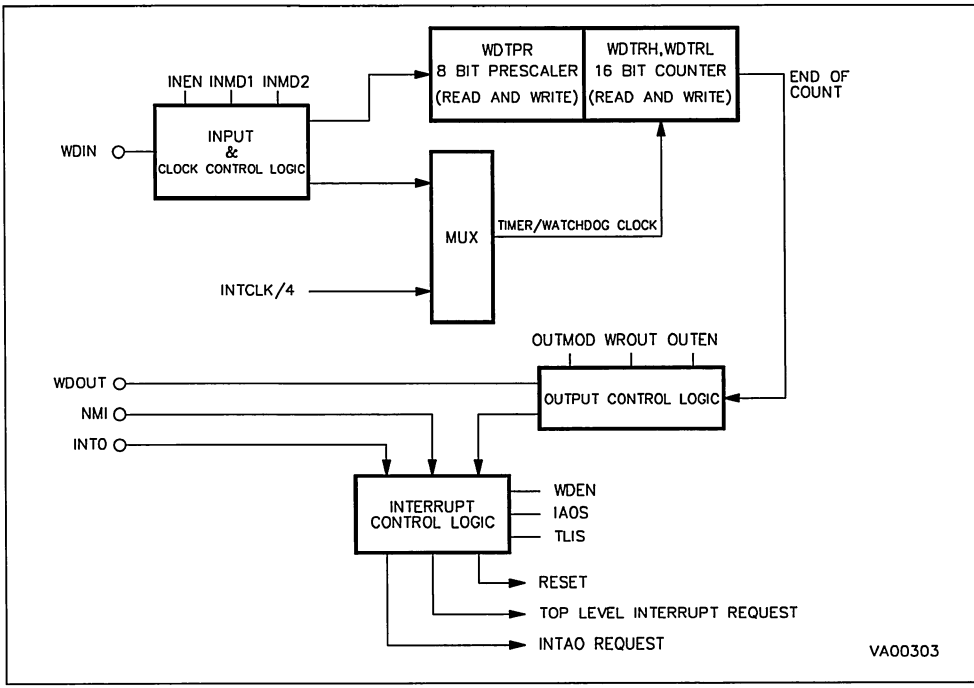


Figure 36. Timer/Watchdog Block Diagram



TIMER/WATCHDOG

A 16 bit down-counter, complete with 8 bit prescaler, is integrated into the ST9040 core. This is able to operate both as a general purpose timer with associated input and output pins for timing functions, and also as a Watchdog Timer offering a security against possible processor malfunctions due to external events.

Timer Modes

When operating as a Timer, with a timing resolution from 333ns to 5.59s (INTCLK = 12MHz), an input pin (WDIN) and output pin (WDOUT) may be selected as the Alternate Functions of two I/O pins. When WDIN is enabled by the user by setting INEN high (WDTCR.3) and the Alternate Function is set, 4 operating modes are available: The WDIN input may be programmed to act as an event counter input, with high to low transitions causing the counter to decrement (the time duration between the falling edges of the input clock must be at least 333ns, allowing a maximum input frequency of 3MHz). It may also be used for pulse width measurement by being selected as a counter clock gate signal (prescaler to the counter being driven by INTCLK/4), counting being enabled when WDIN is at a high level. Trigger and Re-trigger modes cause a reload of the timer user preset values (providing STSP, WDTCR.7 is active) for a high to low transition on WDIN at any time (Re-trigger mode) or when the counter is at the end of count (Trigger mode). The counter decrements at a rate driven by INTCLK/4.

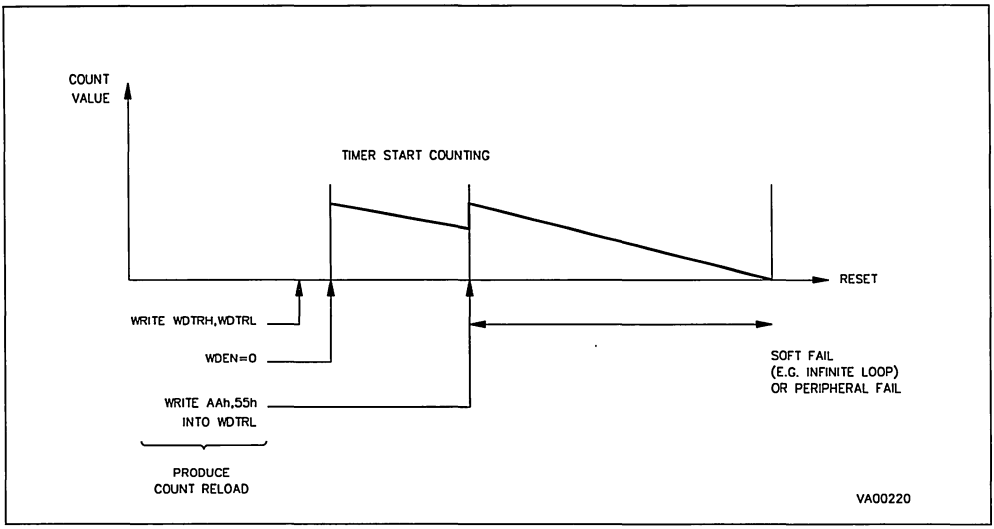
The WDOUT pin, when set as the Alternate Function, is enabled by OUTEN high (WDTCR.0), and may either toggle the state of the I/O bit (frequency generation, OUTMD = "0", WDTCR.2) or pass the state of the WROUT bit to the output allowing PWM generation (OUTMD = "1") at the end of count (timer value = 0) condition.

Watchdog Mode

The timer functions may be disabled, and the Timer configured for a Watchdog operation by re-setting WDEN (WCR.6) to zero. Once the Watchdog has been selected it CANNOT be set back into the standard timer mode until the next Hardware Reset cycle. The programmer should set the watchdog timer prescaler and timer reload value before enabling the Watchdog mode. The Watchdog Timer must

TIMER/WATCHDOG (Continued)

Figure 37. Timer/Watchdog in Watchdog Mode



then be retriggered, causing the reloading of the timer value, by the operation of writing of the byte sequence 0AAh, 055h to the WDTLR register. If this is not done before the Watchdog counts to zero, the Watchdog Timeout condition occurs. This causes a Hardware Reset of the ST9040. The Watchdog reset signal is not output on the external RESET pin.

Timer/watchdog Interrupts

The Timer/Watchdog may provide several levels of interrupts selectable by the programmer.

The Timer mode offers two interrupt sources, triggered on the timer value reaching 0, either a prioritized level (by taking the Interrupt priority channel from the External Interrupt INTA0) or by a top level, non-maskable interrupt (taking the external NMI input channel).

The interrupt channels are multiplexed from the alternative source according to the status of the IAOS (EIVR.1) and TLIS (EIVR.2) bits as shown in Figure 38. Please refer to the ST9 Technical Manual for further details on changing the interrupt sources of the Timer/Watchdog. When the Watchdog mode is set (WDEN = "0"), the timer value equal to 0 event generates a Hardware reset of the ST9040. The Timer/Watchdog control registers are located within Page 0 of the Paged I/O register group.

Figure 38. Timer/Watchdog Interrupt Sources

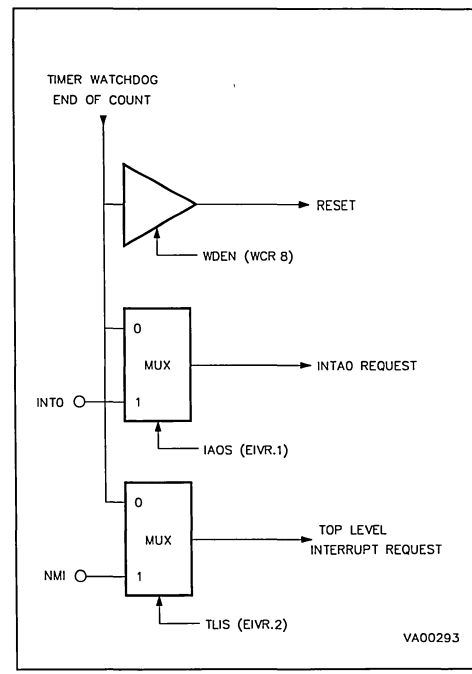
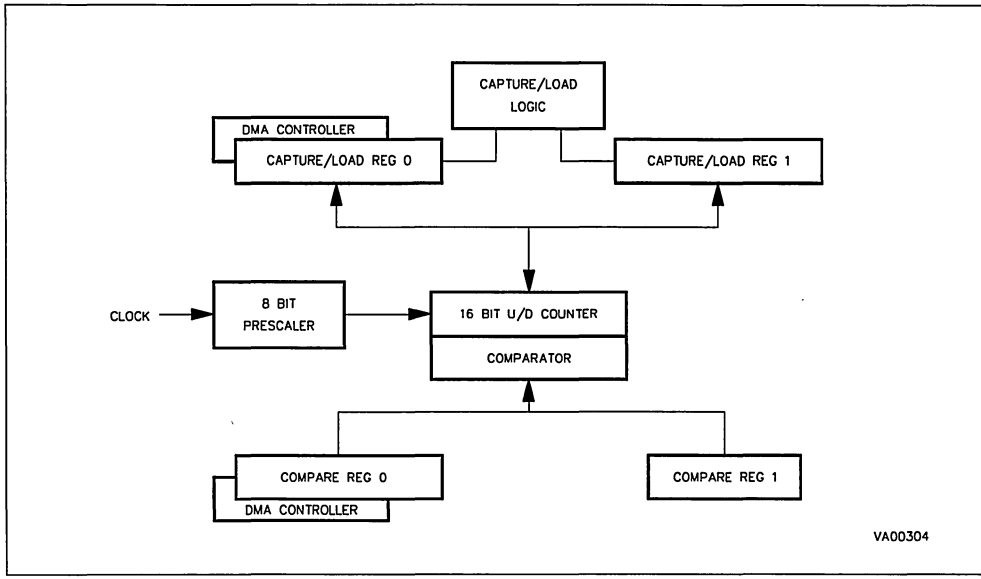


Figure 39. Multifunction Timer Block Diagram



MULTIFUNCTION TIMERS

The ST9040 includes two identical 16 bit Multifunction Timers (MFT) in addition to the TIMER/WATCHDOG. The following description applies to both Timer 0 and Timer 1.

Each timer is a 16 bit Up/Down counter, driven by the output of an 8 bit prescaler which may be driven by INTCLK/3 (giving a minimum timing resolution of 250ns at INTCLK = 12MHz) or by an external source. This timer is supported by two 16 bit Comparison Registers for generating timed functions and two 16 bit Capture/Load Registers for timing and variable timebase functions. These features coupled with 2 input pins (TxINA and TxINB) and 2 output pins (TxOUTA and TxOUTB, where x = 0 or 1), available as Alternate Functions, giving the timer 13 operating modes for virtually all required timing functions.

MFT Operating Modes

The operating modes are selected by the programming of the Timer Control Register (TCR Timer x) and the Timer Mode Register (TMR) as follows:

One-Shot Mode. The counter stops at the End Of Count Condition (up or down count).

Continuous Mode. At End Of Count the timer is reloaded from a Load Register.

Trigger Mode. A Trigger causes reload from a load register only if the Timer is at End of Count.

Retrigger Mode. A Trigger causes reload from a load register at any time.

Gate Mode. Counting is performed only when the external gate input (TxINA, TxINB or TxETCK) is active (logical 0).

Capture Mode. A Trigger causes the timer value to be latched into the selected Capture register.

Up/Down Mode. A Trigger causes a count up or down, or a change in counting direction.

Free-Running Mode. Up or Down counting is performed to the full range with no action at End of Count. This is used in Bicapture and Capture Modes.

Monitor Mode. One Capture register follows the contents of the timer.

Autoclear Mode. The timer is reset to 0000h or FFFFh (up or down count respectively) on a trigger. This gives delta time measurement or free running with a modulo of less than 2^{16}.

Biload Mode. The counter is reloaded on an End Of Count condition alternately from the two Load Registers. (PWM output).

Bicapture Mode. A Trigger causes the current timer value to be transferred alternately to the two Capture registers.

Parallel Mode. The prescaler output of Timer 0 is internally connected to the input of the prescaler of

MULTIFUNCTION TIMER (Continued)

Timer 1, if this is then set to 00h (= divide by 1), then the two timers may be run in parallel.

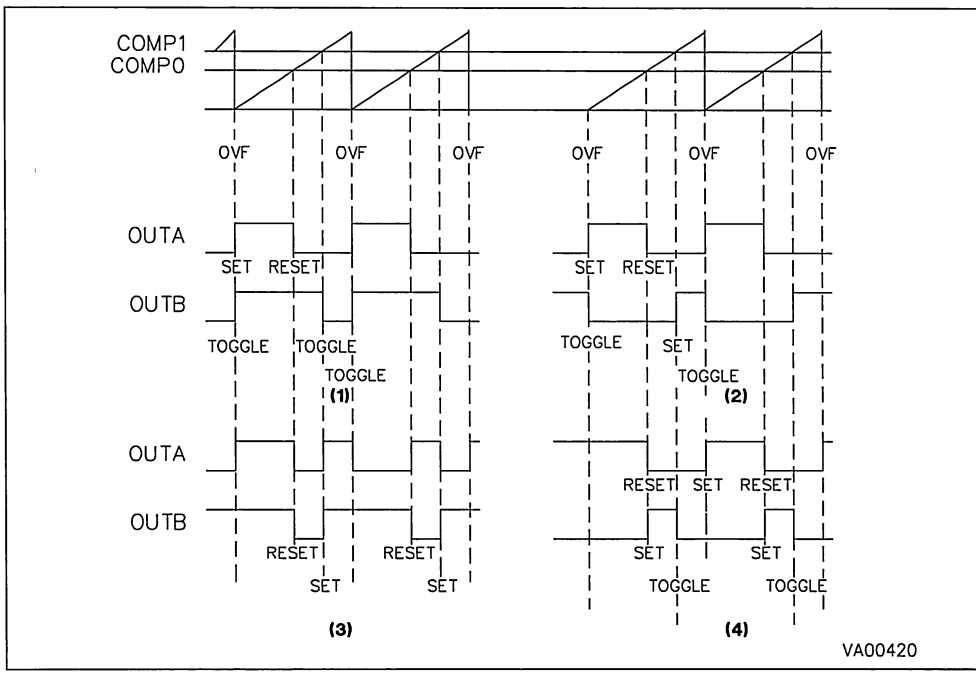
The trigger events may be either caused by software, or an action on the two input pins which may be programmed to respond to rising, falling or both edges of the input. The input modes are selected in the Input Control Register (ICR) as shown in Table 11. This includes the Autodiscriminator mode, which causes the timer to count up or down depending on the phase between the two input edges, such as generated by optical encoders.

The two output pins (available as Alternate Functions) may be programmed through the Output Control Registers OACR and OBCR to be modified (Set, Reset, Toggle or No Operation) on each of Overflow/Underflow (OVF/UNF), Compare on CMP0 valid (CM0), or Compare on CMP1 (COMP1) valid events. This allows repetitive signals such as PWM drive to be output with minimum CPU overhead. Figure 40 shows some typical waveforms available from these signals.

Table 11. Input Pin Function Settings

Input Control Register IN3-IN0 bits	TOINA Input Function	TOINB Input Function
0000	I/O	I/O
0001	I/O	Trigger
0010	Gate	I/O
0011	Gate	Trigger
0100	I/O	Ext.clock
0101	Trigger	I/O
0110	Gate	Ext.clock
0111	Trigger	Trigger
1000	Clock Up	Clock Down
1001	Up/Down	Ext.clock
1010	Trigger Up	Trigger Down
1011	Up/Down	I/O
1100	Autodiscr.	Autodiscr.
1101	Trigger	Ext.clock
1110	Ext.clock	Trigger
1111	Trigger	Gate

Figure 40. Output Waveforms Example



MULTIFUNCTION TIMER (Continued)

The Overflow/Underflow event and the Compare 0 event may also be programmed to give On-chip Event timing signals to trigger other peripheral operations on the ST9040. These are as shown in Table 12.

Table 12. ST903X On-Chip Event Settins

MFT0	A/D Conversion Trigger
MFT1	Handshake Trigger Port

The TxOUTA and TxINA lines for each timer may be connected internally, by setting of the SCx bits of the I/O Connection Register (IOCR).

The Multifunction Timers are enabled for counting by the Counter Enable bit (CEN, TCR.7) of the respective timer unit. When CEN is low, both prescaler and timer are halted. CEN is logically ANDed with the Global Counter Enable bit (GCEN, CICR.7), so that both timers may be started in synchronism, i.e. when the timers are set into Parallel mode, this allows initialization of both Timers before triggering at the same instant. The ETCK input Alternate Function may be used to gate the clock to MFT 0, used, for example, when external clock and trigger signals are required in addition to the gate function.

MFT Interrupts

The Multifunction Timer can generate interrupt requests from 5 different interrupt sources which are grouped into 3 independent groups. The Interrupt Vector has the source of the interrupt group encoded by hardware into the least significant 3 bits of the vector. This allows the programming of the base address to an 8 byte block within the interrupt vector area of the Program Space. The groups and respective addresses are shown in Table 13.

Table 13. MFT Interrupt Vectors

Interrupt Source	Vector Address
COMP0 COMP1	xxxx x110
CAPT0 CAPT1	xxxx x100
Overflow/Underflow	xxxx x000

Each source may be independently masked, in addition all Timer interrupts may be disabled by the Global Timer Interrupt enable (GTIEN, IDMR.7) control bit. If a Timer interrupt on Compare 0 or Capture 0 does not have its corresponding pending bit reset before the next interrupt, then an overrun condition occurs. This condition is flagged in two dedicated overrun bits in the Timer FLAGS register.

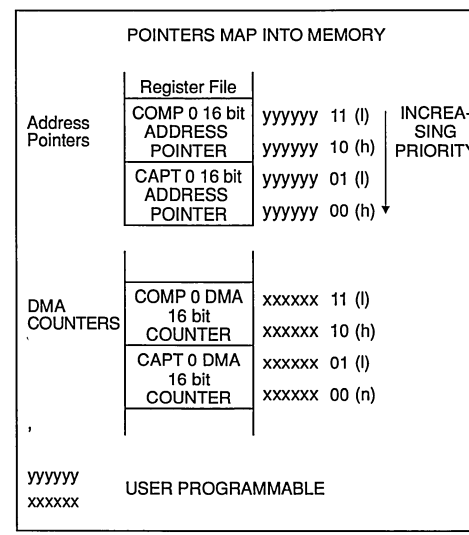
MFT DMA Channels

Two independent DMA channels are present within each MFT, associated to the Compare 0 and Capture 0 sources. This allows 16 bit DMA transactions from Register File/Memory to COMP0 registers, and from CAPT0 registers to Register File/Memory. The DMA channels allow the capture of external event timings in memory allowing off-line analysis, and creating of variable pulse width signal trains, as required by the drive of Triacs in certain modes.

The two interrupt mask sources are independently masked by two DMA mask bits, mapped in the IDMR register. The End of Block (EOB) procedures are as described in the INTERRUPT/DMA section.

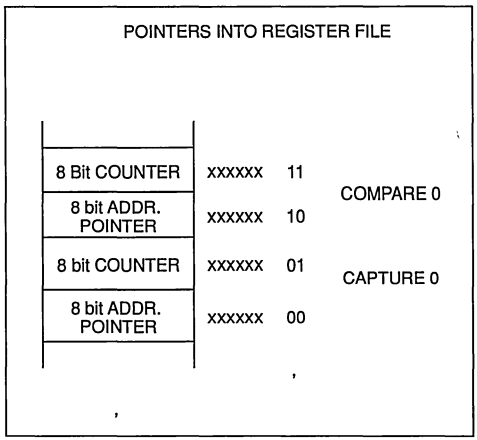
The DMA counter and address pointer registers share the most significant user-programmable 6 bits for both DMA channels (COMP 0 and CAPT 0), thus the mapping of the counter and address registers use automatic offsets from the base address. The actual mapping changes dependent on whether the Register File or Memory is addressed for the transfer. The offsets are shown in Table 14.

Table 14-1. MFT DMA Address and Counter Registers for Memory DMA Transfers



MULTIFUNCTION TIMER (Continued)

Table 14-2. MFT DMA Address and Counter Registers for register file DMA Transfers



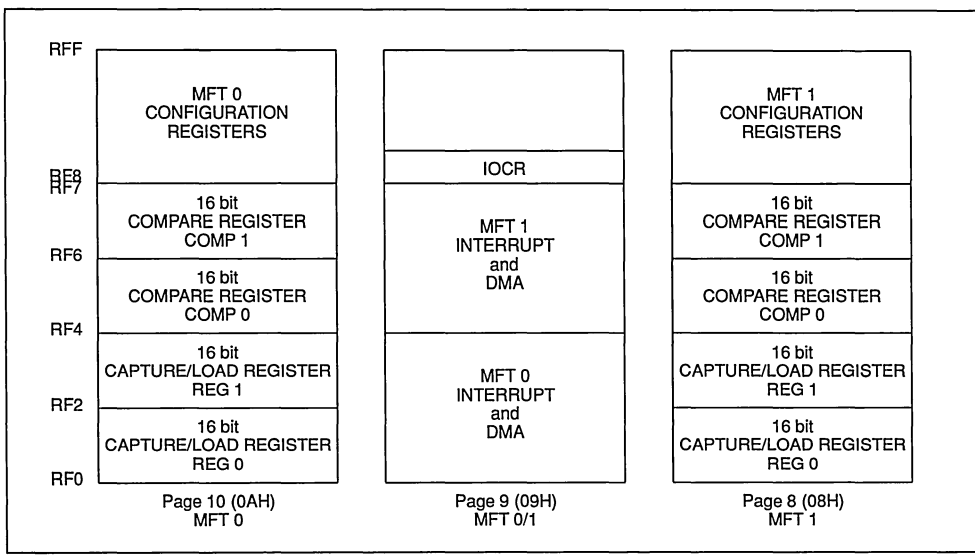
After the transfer of the complete block of data to/from the MFT, the count registers reach the zero value and an end of block interrupt occurs so that the ST9 may process the new data. In many cases, the time taken to reload the data tables and to re-trigger the DMA action causes speed limitations, especially in those applications requiring a continuous high speed data flow, because of the time consumed by the restore routine. An additional DMA function, the SWAP mode, overcomes this limitation. This is enabled by the setting of the SWEN (IDCR.3) bit. This causes hardware generated signals to replace the user address bit 2 of both the address and counter pointers. The address and counter registers are thus duplicated at an offset of 4 registers. At the End Of Block condition, the EOB interrupt is generated to signal the end of DMA, and the state of pointer address bit 2 toggles state automatically and the new address and count values are used. Thus the ST9 can safely process the previous block of data while the new block is being transferred. This will continue until the SWAP mode is disabled.

A software protection scheme is implemented to prevent non-updated pointer registers from being used if a second EOB interrupt arrives during the servicing of the first. This mechanism locks the state of the DMA mask bit to prevent further transfers from taking place. The user should check for this condition in the EOB routine to ensure that all the DMA transfers are properly serviced.

The control Registers of each MFT occupies 20 registers within the I/O paged area. These are mapped as follows:

In addition the MFT is able to trigger byte DMA transfers in both directions through an I/O port with Handshake (see I/O Handshake and DMA).

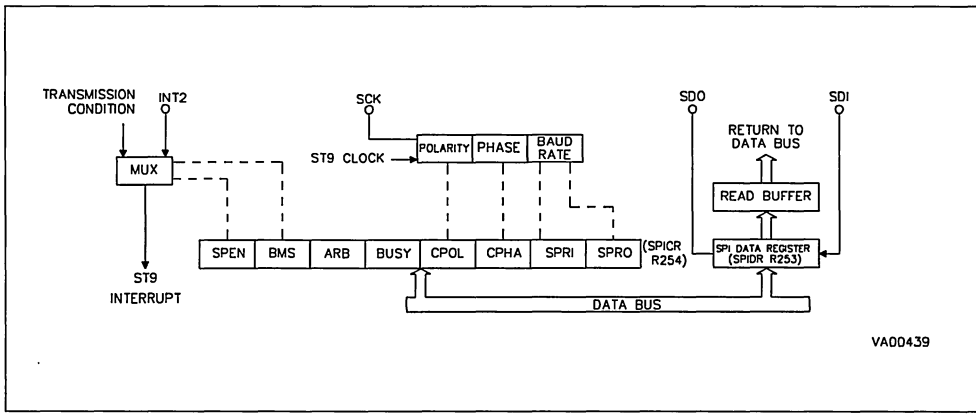
Figure 41. Multifunction Timer Page Maps



SERIAL PERIPHERAL INTERFACE (SPI)

The Serial Peripheral Interface (SPI) is integrated into the Core module of the ST9 and provides a general purpose shift register based peripheral allowing synchronous serial I/O, with special modes allowing compatibility with I^2C-bus and IM-bus Communication standards in addition to the standard serial bus protocol. The SPI uses 3 lines comprising Serial Data Out (SDO), Serial Data In (SDI) and the Synchronous Serial Clock (SCK) which are available as Alternate Functions of I/O pins. Additional I/O pins may act as device selects or IM-bus address ident signals. The functional diagram of the SPI is shown in Figure 42.

Figure 42. SPI Functional Diagram



The SPI, when enabled (SPEN, SPICR.7, high), receives input data from the ST9 internal data bus into the SPIDR, and originates the SCK to shift the data serially through SDO (Most Significant bit first) to the slave device which responds by sending data to the master device via the SDI pin. This implies full duplex transmission with both data-out and data-in synchronized with the same clock signal. Thus the byte transmitted is replaced by the byte received, eliminating the need to separate "Tx Empty" and "Rx full" status bits. After the 8 clock cycles have been concluded, the received data in SPIDR is parallel transferred to the read buffer and data becomes available for the ST9040 during the next read cycle of SPIDR. The BUSY bit (SPICR.4) is set when transmission is in progress, this allows the user to monitor the status of the SPI by polling of this bit.

The SPI can operate only in master mode, i.e. the clock is always generated by the ST9040, however the SCK polarity and phase can be programmed to suit all peripheral requirements (Figure 43). This, together with the 4 programmable bit rates (divided from the INTCLK, Table 15), provide the large flexibility in handling different protocols.

SERIAL PERIPHERAL INTERFACE (SPI) (Continued)

Figure 43. SPI Data and Clock Timing

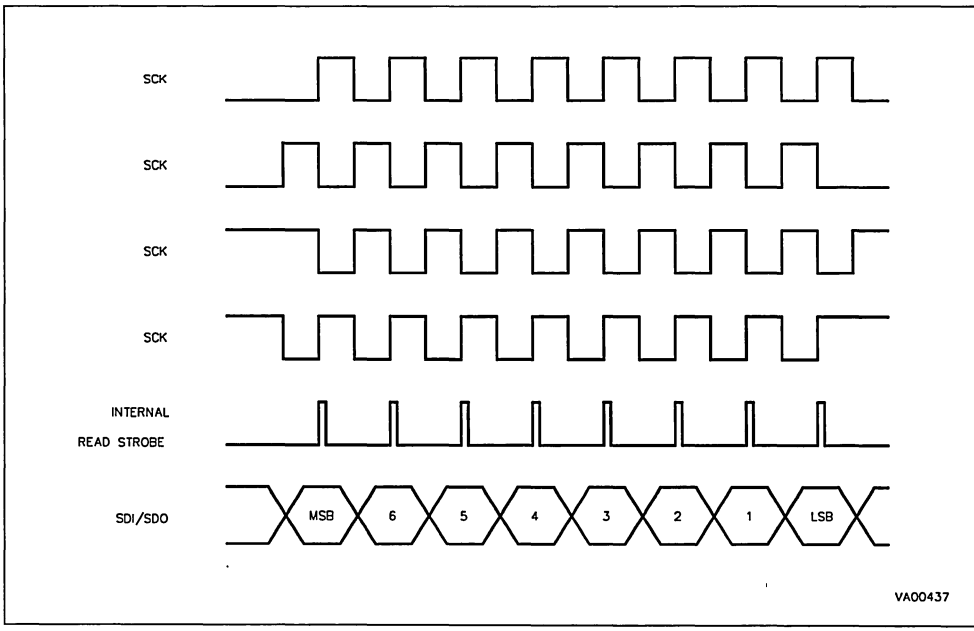


Table 15. SPI Rate Selection

SPR1	SPR0	Clock Divider	SCK Frequency (INTCLK = 12 MHz)
0	0	8	1500 KHz (T= 0.67 µs)
0	1	16	750 KHz (T= 1.33 µs)
1	0	12	93.75 KHz (T= 10.66 µs)
1	1	256	46.87 KHz (T= 21.33 µs)

I²C-bus Compatibility

The SPI includes additional circuitry to enable the use of external I²C-bus peripherals. The I²C-bus mode is a 2 wire bus while the SPI operates with 3 wires, however wire-ANDing SDO and SDI gives the required signalling, while setting the BMS bit causes the enabling of the special I²C-bus features: Clock Slowdown by external devices and Arbitration Lost detection. This mode also affects the Interrupt sources as shown in the next section.

SPI Interrupts

The SPI, when enabled, uses the INT2 external interrupt channel source, using the priority selected for INT2 within the External Interrupt Priority registers. The INT2 mask bit should be set and INT2 pending bit reset before enabling the SPI through SPEN. The BMS (SPICR.6) and SPEN bits select the SPI internal interrupt source as shown in Table 16.

Table 16. SPI Interrupt Sources

SPEN	BMS	Interrupt Source
0	0	External channel INT2
0	1	S-BUS/I²C bus start or stop condition
1	X	End of one byte transmission

SPI Registers

The two registers controlling the SPI are located in I/O page 0, the Data Register, SPIDR, at R253 and the control register, SPICR, at R254.

SERIAL COMMUNICATIONS INTERFACE

Function

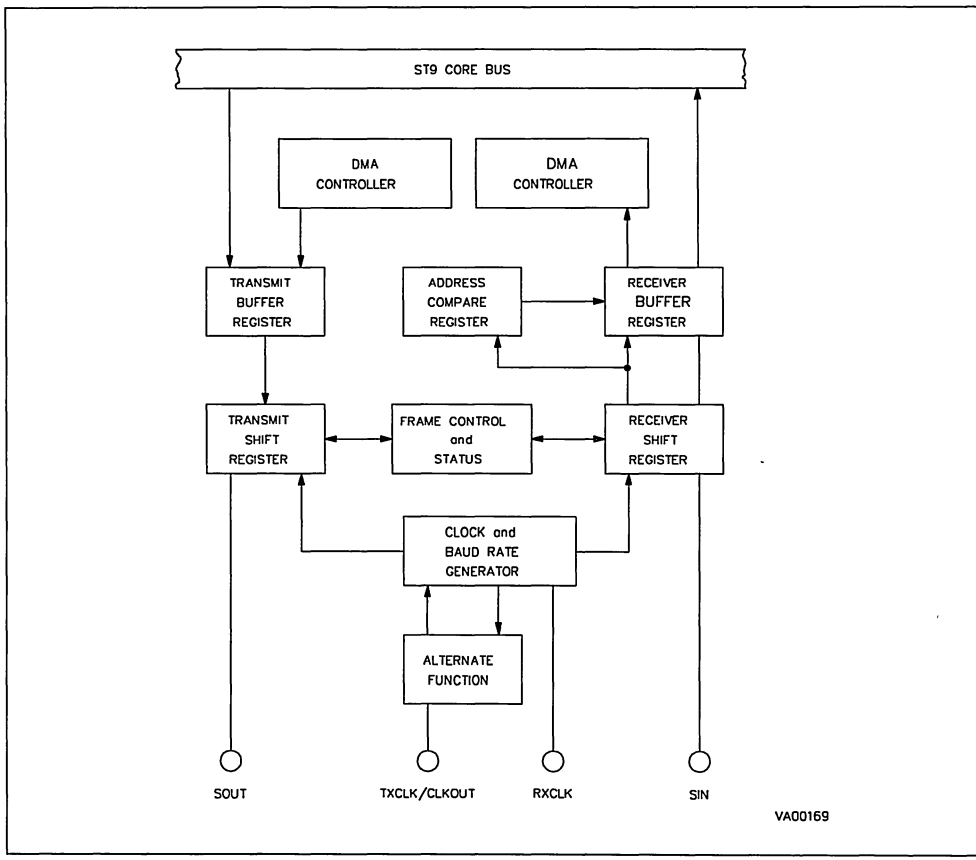
The Serial Communications Interface (SCI) of the ST9040 offers a means of full-duplex serial data transfer to a wide range of external equipment with its fully programmable character format control for asynchronous and byte synchronous serial I/O, integral Baud Rate Generator, giving a maximum baud rate of 375K Baud in Asynchronous mode (Internal Clock), and two DMA channels for transparent transmission and reception of characters. Support is also present in hardware for Line Break Detection and generation, character search, network interfacing with 9th bit Address logic, and Local Loop Back and Auto echo modes for Self-Test. The control registers for the SCI exist within one I/O page within the I/O page group.

Character Formats

When used for asynchronous character transmission and reception, the character format may be changed (through the Character Control Register CHCR) to suit external equipment requirements. This is summarized in Figure 45.

The baud rate clock for asynchronous mode should be set to the /16 Mode and the frequency of the clock input (from an external source or the internal baud-rate generator output) set to suit this.

Figure 44. SCI Functional Block Diagram



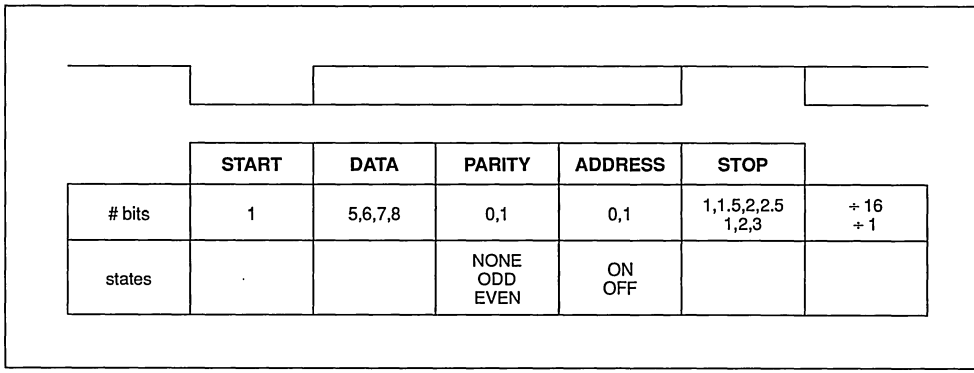
SERIAL COMMUNICATION INTERFACE (Continued)

This format control is also available for the byte synchronous mode (Clock divider set to /1), when the data and clock are output in synchronism, the data being sampled once per clock period (Figure 46). For a second synchronous mode, CLKOUT is activated only for the data section of the word Figure 47) on serial data output, and input data is latched on the rising edge of the external synchronised clock input on the RXCLK pin. This mode may be used to access external synchronous peripherals.

The Address bit/D9 is optional and may be added to any word format, it is commonly used in network or machine control applications. When enabled (AB, CHCR.4 = 1), an address or ninth data bit can be added to a transmitted word by setting the Set Address bit (SA, IDPR.5). This is then appended to the next word entered into the (empty) Transmitter Buffer Register and then cleared by hardware. On character input an Address Bit set can indicate that the data preceding the bit is an address which may be compared in hardware with the value in the Address Compare Register (ACR) to generate an Address Match interrupt when equal.

The Address bit and Address Comparison Register can also be combined to generate an Address Interrupt in 4 modes to suit different protocols, based upon the status of the Address Mode Enable bit (AMEN, IDPR.7) and the Address Mode bit (AM, CHCR.7) as shown in Table 17.

Figure 45. SCI Character Format



	START	DATA	PARITY	ADDRESS	STOP	
# bits	1	5,6,7,8	0,1	0,1	1,1.5,2,2.5 1,2,3	÷ 16 ÷ 1
states			NONE ODD EVEN	ON OFF		

Figure 46. Byte Synchronous Output

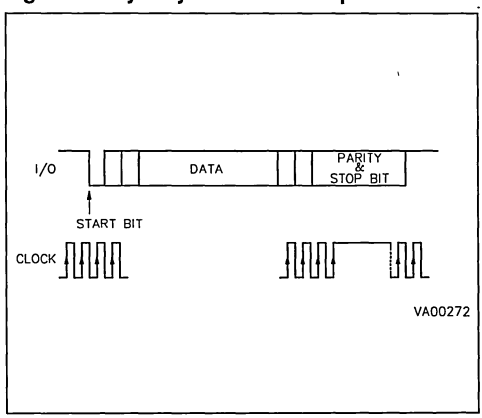
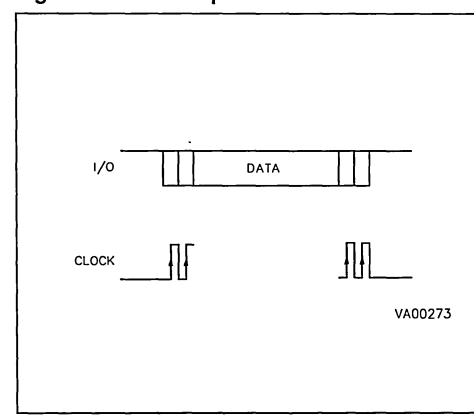


Figure 47. Serial Expansion Mode



SERIAL COMMUNICATION INTERFACE (Continued)

Table 17. Address Interrupt Modes

If 9th Data Bit = 1
If Character Match
If Character Match and 9th Data Bit = 1
If Character Match on Word Immediately Following Break

The character match Address Interrupt mode may be used as a powerful character search mode, giving an interrupt on reception of a predetermined character e.g. Carriage Return or End of Block codes.

The Line Break condition is fully supported for both transmission and detection. Line Break is sent by setting the SET_BREAK bit (SB, IDPR.6). This causes the transmitter output to be held low (after all buffered data has been transmitted) for a minimum of one complete word length and until the SB bit is Reset.

SCI Interrupts

The SCI is able to generate interrupts from multiple sources. Receive interrupts include data pending, receive errors (overrun, framing and parity), address or break pending and transmit interrupts are software selectable for either the Transmit Holding Register Empty (HSN, IMR.7 = 1) or for the Transmit Shift Register Empty (HSN = 0). Interrupt sources are indicated by the Interrupt pending bits, shown in Table 18. These bits should be reset by the programmer during the Interrupt Service routine.

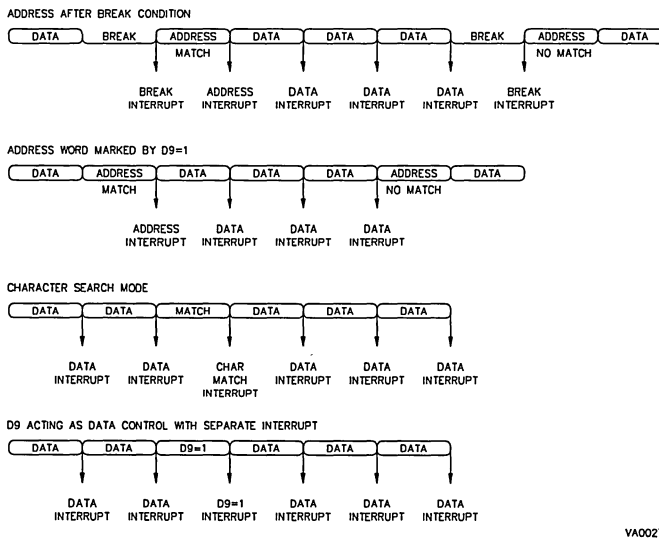
Table 18. SCI Interrupt Vector

Interrupt Source	Vector Address
Transmitter Buffer or Shift Register Empty/ Transmit DMA end of Block	xxx x110
Received Ready/ Receive DMA end of Block	xxxx x100
Break Detector Address Word Match	xxxx x001
Receiver Error	xxxx x000

When DMA is active the Receive Data Pending bit (RXDP, ISR.2), and the Transmit status bit interrupt sources are replaced by the DMA End Of Block Interrupt sources for transmit and receive, respectively.

Typical Usage of the Interrupts provided by the SCI are show in Figure 48.

Figure 48. SCI Interrupt Typical Usage



SERIAL COMMUNICATION INTERFACE (Continued)

The SCI interrupts have an internal priority structure (Table 19) in order to resolve simultaneous events.

The four major levels of interrupt are encoded in hardware to provide two bits of the interrupt vector register, allowing the position of the block of pointer vectors to be resolved to a block size of 8 bytes.

Table 19. SCI Interrupt Internal Priority

Receive DMA Request	Highest Priority
Transmit DMA Request	Lower Priority
Receive Interrupt	
Transmit Interrupt	

SCI DMA

Two DMA channels are associated with the SCI, for transmit and for receive. These follow the register scheme as described in DMA section. It should be noted that, after initializing the DMA counter and pointer registers and enabling DMA, data transmission is triggered by a character written into the Transmit Holding register. The DMA End Of Block Interrupts generated on completion of the DMA transfer take the place of the normal transmit and receive character interrupt vectors.

SCI Clock Generation

The communication bit frequency of the SCI transmitter and receiver sections can be provided from the integral Baud Rate Generator (allowing a maximum asynchronous bit rate of 350k Baud) or from external sources (maximum bit rate 175k Baud). This clock is divided by 16 for asynchronous mode (CD, CCR.3, =0), or divided by 1 for synchronous modes (CD=1).

External Clock Sources. The External Clock input pin TXCLK may be programmed in Alternate function by bits TXCLK (CCR.7) and OCLK (CCR.6) to be: the transmit clock input (respecting the %16 and %1 timing requirements), to act as the output of the Baud Rate Generator (allowing an external divider circuit to provide the receive clock for split rate transmit and receive e.g. 1200/75 baud), or to be CLKOUT, the clock output for the synchronous mode. Receive clock input via RXCLK Alternate function is enabled by the XRX bit CCR.5, this input should be set according to the setting of the CD bit.

Baud Rate Generator. The integral Baud Rate Generator is a 16 bit divide by n circuit of the Internal Clock INTCLK. Thus INTCLK should be chosen to provide a suitable frequency for division by the Baud Rate Generator to give the required transmit and receive bit rates.

Suitable INTCLK frequencies and the divider values for standard Baud rates are shown in Table 20.

The act of writing to either of the two registers comprising the 16 bit divider causes a reset of the SCI, allowing initialization of the SCI settings before the writing of the other Baud Rate Generator register.

Self Test

Testing of the communications channel may be performed using the facilities of the SCI. Auto Echo mode (SCI SOUT disconnected, SIN pin internally connected to SOUT pin) and Loopback mode (SCI transmitter and receiver sections disconnected from SOUT and SIN pins and directly connected internally) may be used individually or together.

SERIAL COMMUNICATION INTERFACE (Continued)

Table 20. SCI Baud Rate Generator Divider Values

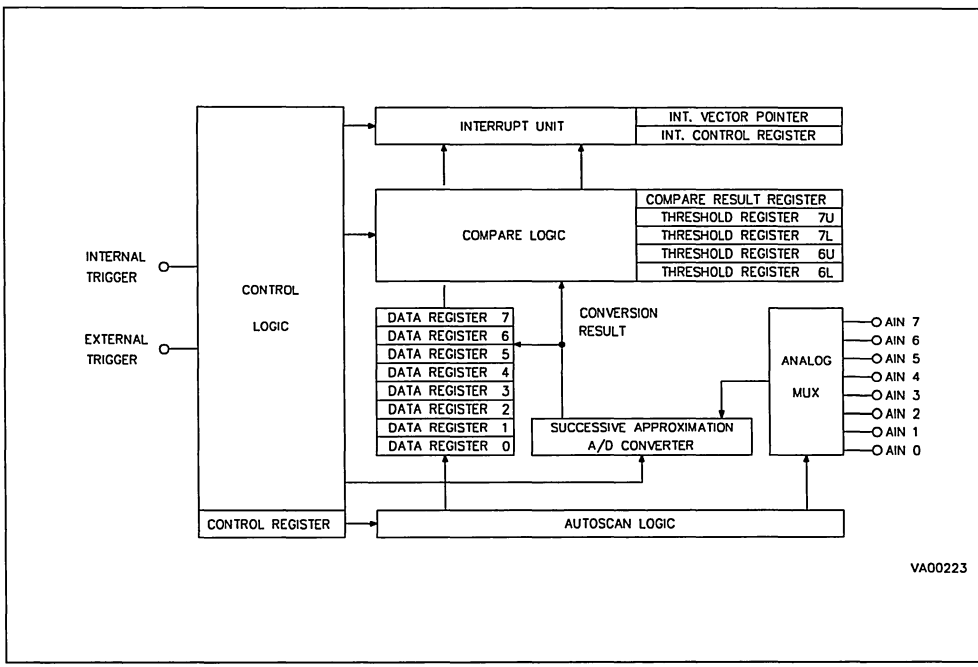
INTCLK: 7680.000 KHz							
Baud Rate	Clock Factor	Desired Freq (kHz)	Divisor		Actual Baud Rate	Actual Freq (kHz)	Deviation
			Dec	Hex			
50.00	16 X	0.80000	9600	2580	50.00	0.80000	0.0000%
75.00	16 X	1.20000	6400	1900	75.00	1.20000	0.0000%
110.00	16 X	1.76000	4364	110C	109.99	1.75985	0.0083%
300.00	16 X	4.80000	1600	0640	300.00	4.80000	0.0000%
600.00	16 X	9.60000	800	0320	600.00	9.60000	0.0000%
1200.00	16 X	19.20000	400	0190	1200.00	19.20000	0.0000%
2400.00	16 X	38.40000	200	00C8	2400.00	38.40000	0.0000%
4800.00	16 X	76.80000	100	0064	4800.00	76.80000	0.0000%
9600.00	16 X	153.60000	50	0032	9600.00	153.60000	0.0000%
19200.00	16 X	307.20000	25	0019	19200.00	307.20000	0.0000%
38400.00	16 X	614.40000	13	000D	36923.08	590.76923	3.8462%
76800.00	16 X	1228.80000	6	0006	80000.00	1280.00000	4.1667%
INTCLK: 11059.20 kHz							
Baud Rate	Clock Factor	Desired Freq (kHz)	Divisor		Actual Baud Rate	Actual Freq (kHz)	Deviation
			Dec	Hex			
50.00	16 X	0.80000	13824	3600	50.00	0.80000	0.0000%
75.00	16 X	1.20000	9216	2400	75.00	1.20000	0.0000%
110.00	16 X	1.76000	6284	188C	109.99	1.75990	0.0058%
300.00	16 X	4.80000	2304	0900	300.00	4.80000	0.0000%
600.00	16 X	9.60000	1152	0480	600.00	9.60000	0.0000%
1200.00	16 X	19.20000	576	0240	1200.00	19.20000	0.0000%
2400.00	16 X	38.40000	288	0120	2400.00	38.40000	0.0000%
4800.00	16 X	76.80000	144	0090	4800.00	76.80000	0.0000%
9600.00	16 X	153.60000	72	0048	9600.00	153.60000	0.0000%
19200.00	16 X	307.20000	36	0024	19200.00	307.20000	0.0000%
38400.00	16 X	614.40000	18	0012	38400.00	614.40000	0.0000%
76800.00	16 X	1228.80000	9	0009	76800.00	1228.80000	0.0000%

ANALOG TO DIGITAL CONVERTER

The ST9040 Analog to Digital Converter (A/D) is comprised of an 8 channel multiplexed input selector and a Successive Approximation converter. The conversion time is a function of the INTCLK frequency; for the maximum 12MHz clock rate, conversion of the selected channel requires 11µs. This time also includes the 3µs of the integral Sample and Hold circuitry, which minimizes need for external components. The resolution of the converted channel is 8 bits ± 1/2 LSB between the Analog V_{SS} and V_{DD} references which occupy two pins of the ST9040 (AV_{SS} and AV_{DD} respectively). These allow the full 256 bit resolution to apply over a reduced input range such as provided by various sensors and allows the best supply noise rejection.

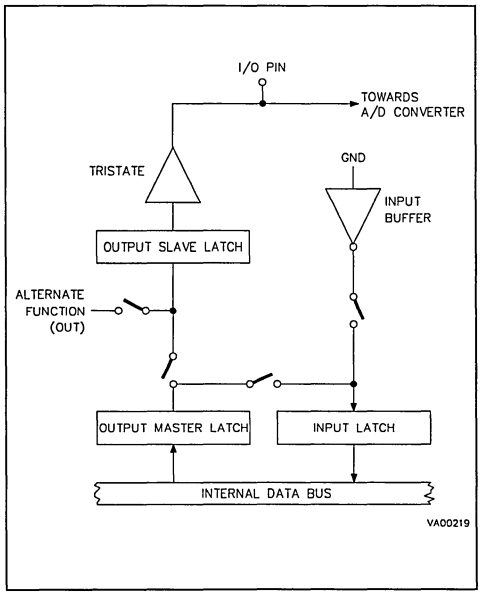
The input Analog channel is selected by using the Alternate Function setting as shown in the I/O ports section. The I/O bit structure of the port connected to the A/D converter (Port 4) is modified as shown in Figure 50 to prevent the Analog voltage present at the I/O pin from causing high power dissipation across the input buffer. Un-selected analog channels should also be maintained in the Alternate function mode for this reason. A Power Down mode is available for applications which require low power dissipation, this is selected by setting to zero the POW bit (CLR.2) which turns off all Analog functions within the A/D converter.

Figure 49. A/D Block Diagram



ANALOG DIGITAL CONVERTER (Continued)

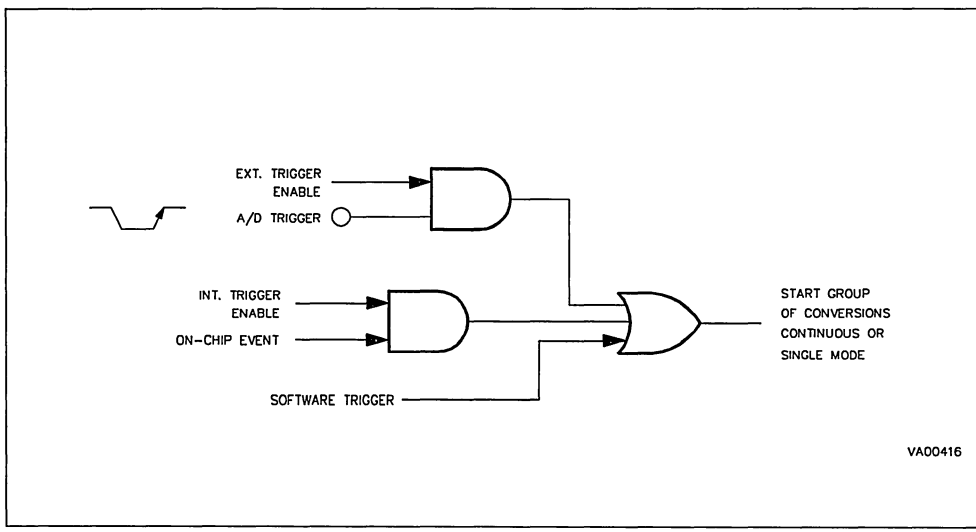
Figure 50. A/D Input Configuration



Conversion

Each of the input Analog channels (AIN0-7) can be converted singly or continuously. In single mode (CONT, CLR.1, = "0") conversions are triggered by setting the Start/Stop bit ST (CLR.0), this is reset by hardware at the end of a group of conversions and conversion stops. The Autoscan mode (CONT = "1") converts each input channel in sequence, starting from the channel number selected in the Start Conversion Address (SC1-3) bits and increasing to channel 7 (AIN7), repeating so that the data registers will be maintained with the latest converted result. Conversion start is triggered by internal or external events. An external trigger (enabled by EXTG, CLR.4, = "1") is caused by a pulse on the ADTRG pin available as an Input Alternate Function. This should have a minimum length of 80ns and of a period greater than the conversion time. The Internal trigger is enabled by setting INTG, CLR.3, to "1" (this is ORed with EXTG to prevent hardware conflicts, but the correct procedure is to enable only one source at a time), in this case triggering is either by setting the ST bit by software or by enabling the ON-CHIP EVENT signal from the TIMER module.

Figure 51. A/D Trigger Sources

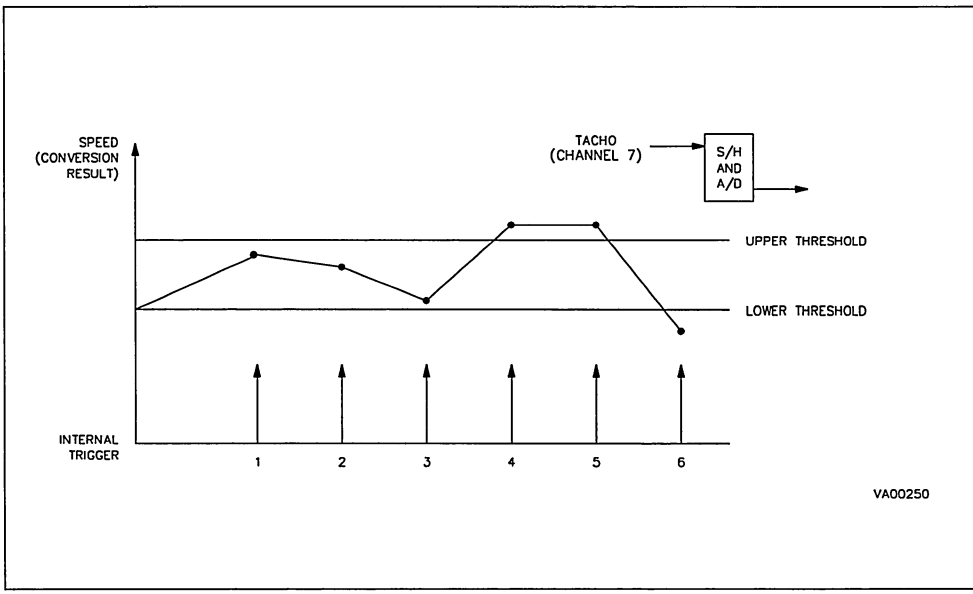


ANALOG DIGITAL CONVERTER (Continued)

The resulting data from the converted Analog channel AINx is stored in the appropriate Data Register DxR. Two channels AIN6 and AIN7 have a special feature known as the Analog Watchdog, by the use of two Threshold Registers for each channel. The Upper, (HT6R, HT7R), and lower, (LT6R, LT7R), registers contain user preset values.

These values are automatically compared to the value in the Data Registers D6R and D7R following each new conversion. If the resulting data is less than the corresponding Lower Threshold Register, or higher than the contents of the corresponding Upper Threshold Register, then an interrupt may be generated. This hardware feature minimizes analog monitoring overhead and is particularly useful in motor control applications as shown in Figure 52.

Figure 52. Analog Watchdog used in motor speed control



A/D Interrupts

The ST9040 A/D converter provides two interrupt sources, End of Conversion and an Analog Watchdog Request. The interrupt vector register (IVR) provides 1 bit automatically generated in hardware to follow the interrupt source, allowing the user to select the base address of a four byte area of the interrupt vector table in which to store the A/D Interrupt Service Routines. The Analog Watchdog Request requires the user to poll within the Compare Result Register (CRR) to determine which of the four thresholds has been exceeded, the threshold status bits should be reset by software in the service routine. The interrupt pending flags, ECV (End of Conversion, ICR.7) and AWD (Analog Watchdog, ICR.6) should also be reset by the User in the Interrupt service routine before the return.

The ST9040 Analog to Digital converter occupies I/O page 63 (Group F).

SOFTWARE DESCRIPTION

Addressing Modes

The ST9040 offers a wide variety of addressing modes and combinations to facilitate full and rapid access to the address spaces while reducing program length. Register addressing (using the working register group mechanism or directly addressed) can be used as 8 or 16 bit values for data or indirect addressing into the memory spaces or the Register File. The selection between Program Memory and Data Memory is performed through the P/D bit in the FLAG Register, all subsequent actions on the memory space will affect the selected map only, apart from the memory map to memory map post-increment addressing mode which allows the map to be specified as part of the instruction for both destination and source operands. Apart from the immediate data and condition codes all operands are expressed as register file or memory addresses.

The available addressing modes, with the ST9 macro-assembler notation, are in Table 21 :

Combinations Of Available Addressing Modes

Table 22 describes the addressing modes available for the register file and the memory (both as a destination and as a source) for the two operand arithmetic, logic or load instructions .

Table 21. Addressing Mode

Addressing Mode	Notation	
Immediate Data	#N	#NN
Register Direct	R, r	RR, rr
Register Indirect	(R)	(r)
Register Indexed	N(r)	N(rr)
Memory Direct	NN	
Memory Indirect	(RR)	(rr)
Memory Indirect with Post-Increment	(rr)+	
Memory Indirect with Pre-Decrement	-(rr)	
Memory Indexed with Immediate Short Offset	N(rr)	
Memory Indexed with Immediate Long Offset	NN(rr)	
Memory Indexed with Register Offset	rr(rr)	
Memory Indirect Post-Increment to Indirect Register Post Increment	(rr)+	(r)+
Memory Map to Memory Map both with Post-Increment	(rr)+	(rr)+
Bit Address	(rr).b	(rr).b

Legend: N = 8 bit Value
NN = 16 bit Value or Address
r = Working Register
R = Directly Addressed Register
( ) = Indirect Addressing
( )+ = Indirect with Post-Increment
-( ) = Indirect with Pre-Decrement
.b = Bit Number (0 to 7)

Table 22. Addressing Mode Permutation for Instructions

Two Operand Arithmetic and Logic Instructions	
Destination	**Source**
Register Direct	Register Direct
Register Direct	Register Indirect
Register Direct	Memory Indirect
Register Direct	Memory Indexed
Register Direct	Memory Indirect with Post-Increment
Register Direct	Memory Indirect whit Pre-Decrement
Register Direct	Memory Direct
Register Indirect	Register Direct
Memory Indirect	Register Direct
Memory Indexed	Register Direct
Memory Indirect with Post-Increment	Register Direct
Memory Indirect with Pre-Decrement	Register Direct
Memory Direct	Register Direct
Register Indirect	Register Direct
Memory Indirect	Register Direct
Memory Indexed	Register Direct
Memory Indirect with Post-Increment	Register Direct
Memory Indirect with Pre-Decrement	Register Direct
Memory Direct	Register Direct

SOFTWARE DESCRIPTION (Continued)

Table 22. Addressing Mode Permutation for Instructions (Continued)

Two Operand Arithmetic and Logic Instructions	
Destination	**Source**
Register Direct	Register Direct
Register Direct	Register Indirect
Register Direct	Register Indexed
Register Direct	Memory Indirect
Register Direct	Memory Indexed
Register Direct	Memory Indirect with Post- Increment
Register Direct	Memory Indirect with Pre- Decrement
Register Direct	Memory Direct
Register Indirect	Register Direct
Register Indexed	Register Direct
Memory Indirect	Register Direct
Memory Indexed	Register Direct
Memory Indirect with Post- Increment	Register Direct
Memory Indirect with Pre- Decrement	Register Direct
Memory Direct	Register Direct
Register Direct	Immediate
Memory Direct	Immediate
Memory Indirect	Immediate
Two Operand Load Instructions	
Destination	**Source**
Register Direct	Immediate
Memory Direct	Immediate
Memory Indirect	Immediate
Long Indexed Memory (1)	Immediate
Two Operand Arithmetic, Logic & Load Instructions	
Destination	**Source**
Memory Indirect	Memory Indirect

Two Operand Load Instructions (1)	
Destination	**Source**
Register Indirect with Post- Increment	Memory Indirect with Post- Increment
Memory Indirect with Post- Increment	Register Indirect with Post- Increment
Memory Indirect with Post- Increment	Memory Indirect with Post- Increment

Note: 1. Load Byte only

INSTRUCTION SET

The ST9040 instruction set consists of 87 groups of instruction types functionally divided into eight groups as shown in Table 23, they are:

- Load (two operands)
- Arithmetic & Logic (two operands)
- Arithmetic Logic and Shift (one operand)
- Stack (one operand)
- Multiply and Divide (two operands)
- Boolean (one or two operands)
- Program Control (zero to three operands)
- Miscellaneous (zero to two operands)

The wide range of instructions facilitates the full use of the register file and address spaces, reducing execution times, while the register pointers mechanism allows an unmatched code efficiency and fast context switching. A notable feature is the comprehensive "Any Bit, Any Register" (ABAR) addressing capability of the Boolean instructions.

The ST9040 can operate with a wide range of data lengths, from single bits, 4 bit nibbles which can be in the form of Binary Coded Decimal (BCD), 8 bit bytes and 16 bit words. The summary in Table 23 shows the instructions belonging to each group and the number of operands required for each. The source operand is "src", "dst" is the destination operand and "cc" is the condition code selection.

INSTRUCTION SET (Continued)

Table 23. Instruction Set Summary

Load Instructions (Two Operands)								
Mnemonic	Operand	Instruction	Flags					
			C	Z	S	V	D	H
LD LDW	dst, src dst, src	Load Load Word	– –	– –	– –	– –	– –	– –
Arithmetic and Logic (Two Operands)								
Mnemonic	Operand	Instruction	Flags					
			C	Z	S	V	D	H
ADD ADDW	dst, src dst, src	Add Add Word	Δ Δ	Δ Δ	Δ Δ	Δ Δ	0 ?	Δ ?
ADC ADCW	dst, src dst, src	Add with Carry Add Word with Carry	Δ Δ	Δ Δ	Δ Δ	Δ Δ	0 ?	Δ ?
SUB SUBW	dst, src dst, src	Subtract Subtract Word	Δ Δ	Δ Δ	Δ Δ	Δ Δ	1 ?	Δ ?
SBC SBCW	dst, src dst, src	Subtract with Carry Subtract Word with Carry	Δ Δ	Δ Δ	Δ Δ	Δ Δ	1 ?	Δ ?
AND ANDW	dst, src dst, src	Logical AND Logical Word AND	– –	Δ Δ	Δ Δ	0 0	– ?	– ?
OR ORW	dst, src dst, src	Logical OR Logical Word OR	– –	Δ Δ	Δ Δ	0 0	– –	– –
XOR XORW	dst, src dst, src	Logical Exclusive OR Logical Word Exclusive OR	– –	Δ Δ	Δ Δ	0 0	– –	– –
CP CPW	dst, src dst, src	Compare Compare Word	Δ Δ	Δ Δ	Δ Δ	Δ Δ	– –	– –
TM TMW	dst, src dst, src	Test Under Mask Test Word Under Mask	– –	Δ Δ	Δ Δ	0 0	– –	– –
TCM TCMW	dst, src dst, src	Test Complement Under Mask Test Word Complement Under Mask	– –	Δ Δ	Δ Δ	0 0	– –	– –

Legend : 0 = Bit set to zero
1 = Bit set to one
Δ = Bit affected
? = Bit status undefined
- = Bit not affected

INSTRUCTION SET (Continued)

Table 23.Instruction Set Summary (Continued)

Arithmetic Logic and Shift (One Operand)									
Mnemonic	**Operand**	**Instruction**	**Flags**						
			C	**Z**	**S**	**V**	**D**	**H**
INC INCW	dst dst	Increment Increment Word	– –	Δ Δ	Δ Δ	Δ Δ	– –	– –
DEC DECW	dst dst	Decrement Decrement Word	– –	Δ Δ	Δ Δ	Δ Δ	– –	– –
SLA SLAW	dst dst	Shift Left Arithmetic Shift Word Left Arithmetic	Δ Δ	Δ Δ	Δ Δ	Δ Δ	0 ?	Δ ?
SRA SRAW	dst dst	Shift Right Arithmetic Shift Word Right Arithmetic	Δ Δ	Δ ?	Δ Δ	Δ 0	0 –	Δ –
RRC RRCW	dst dst	Rotate Right through Carry Rotate Word Right through Carry	Δ Δ	Δ ?	Δ Δ	Δ Δ	– –	– –
RLC RLCW	dst dst	Rotate Left through Carry Rotate Word Left through Carry	Δ Δ	Δ ?	Δ Δ	Δ Δ	– –	– –
ROR	dst	Rotate Right	Δ	Δ	Δ	Δ	–	–
ROL	dst	Rotate Left	Δ	Δ	Δ	Δ	–	–
CLR	dst	Clear	–	–	–	–	–	–
CPL	dst	Complement Register	–	Δ	Δ	0	–	–
SWAP	dst	Swap Nibbles	?	Δ	Δ	?	–	–
DA	dst	Decimal Adjust	Δ	Δ	Δ	?	–	–
Stack Instructions (One Operand)									
Mnemonic	**Operand**	**Instruction**	**Flags**						
			C	**Z**	**S**	**V**	**D**	**H**
PUSH PUSHW PEA	src src src	Push on System Stack Push Word on System Stack Push Effective Address on System Stack	– – –	– – –	– – –	– – –	– – –	– – –
POP POPW	dst dst	Pop from System Stack Pop Word from System Stack	– –	– –	– –	– –	– –	– –
PUSHU PUSHUW PEAU	src src src	Push on User Stack Push Word on User Stack Push Effective Address on User Stack	– – –	– – –	– – –	– – –	– – –	– – –
POPU POPUW	dst dst	Pop from User Stack Pop Word from User Stack	– –	– –	– –	– –	– –	– –
Multiply and Divide Instructions (Two Operands)									

INSTRUCTION SET (Continued)

Table 23. Instruction Set Summary (Continued)

Mnemonic	Operand	Instruction	Flags					
			C	Z	S	V	D	H
MUL	dst, src	Multiply 8x8	Δ	Δ	Δ	Δ	0	?
DIV DIVWS	dst, src	Divide 16/8 Divide Word Stepped 32/16	1 ?	Δ ?	Δ ?	? ?	1 ?	? ?
Boolean Instructions (Two Operands)								
Mnemonic	**Operand**	**Instruction**	**Flags**					
			C	**Z**	**S**	**V**	**D**	**H**
BLD	dst, src	Bit Load	–	–	–	–	–	–
BAND	dst, src	Bit AND	–	–	–	–	–	–
BOR	dst, src	Bit OR	–	–	–	–	–	–
BXOR	dst, src	Bit Exclusive OR	–	–	–	–	–	–
Boolean Instructions (One Operand)								
Mnemonic	**Operand**	**Instruction**	**Flags**					
			C	**Z**	**S**	**V**	**D**	**H**
BSET	dst	Bit Set	–	–	–	–	–	–
BRES	dst	Bit Reset	–	–	–	–	–	–
BCPL	dst	Bit Complement	–	–	–	–	–	–
BTSET	dst	Bit Test and Set	–	Δ	Δ	0	–	–
Program Control Instructions (Three Operands)								
Mnemonic	**Operand**	**Instruction**	**Flags**					
			C	**Z**	**S**	**V**	**D**	**H**
CPJFI	dst, src	Compare and Jump on False, Otherwise Post Increment	–	–	–	–	–	–
CPJTI	dst, src	Compare and Jump on True, Otherwise Post Increment	–	–	–	–	–	–
Program Control Instructions (Two Operands)								

INSTRUCTION SET (Continued)

Table 23. Instruction Set Summary (Continued)

Mnemonic	Operand	Instruction	Flags					
			C	Z	S	V	D	H
BTJF	dst, src	Bit Test and Jump if False	–	–	–	–	–	–
BTJT	dst, src	Bit Test and Jump if True	–	–	–	–	–	–
DJNZ	dst, src	Decrement a Working Register and Jump if Not Zero	–	–	–	–	–	–
DWJNZ	dst,src	Decrement a Register Pair and Jump if Not Zero	–	–	–	–	–	–
Program Control Instructions (One Operand)								
Mnemonic	**Operand**	**Instruction**	**Flags**					
			C	**Z**	**S**	**V**	**D**	**H**
JR	cc, dst	Jump Relative if Condition is Met	–	–	–	–	–	–
JP	cc, dst	Jump if Condition is Met	–	–	–	–	–	–
JP	dst	Unconditional Jump	–	–	–	–	–	–
CALL	dst	Unconditional Call	–	–	–	–	–	–
Program Control Instructions (No Operand)								
Mnemonic	**Operand**	**Instruction**	**Flags**					
			C	**Z**	**S**	**V**	**D**	**H**
RET		Return from Subroutine	–	–	–	–	–	–
IRET		Return from Interrupt	Δ	Δ	Δ	Δ	Δ	Δ
WFI		Stop Program Execution and Wait Next Enabled Interrupt. If a DMA request is present the CPU executes the DMA service routine and returns to WFI state.	–	–	–	–	–	–
HALT		Stop Program Execution until RESET	–	–	–	–	–	–
Miscellaneous (Two Operands)								
Mnemonic	**Operand**	**Instruction**	**Flags**					
			C	**Z**	**S**	**V**	**D**	**H**
XCH	dst, src	Exchange Registers	–	–	–	–	–	–
Miscellaneous (One Operand)								

INSTRUCTION SET (Continued)

Table 23. Instruction Set Summary (Continued)

Mnemonic	Operand	Instruction	Flags					
			C	Z	S	V	D	H
SRP	src	Set Register Pointer Long (16 Working Registers)	–	–	–	–	–	–
SRP0	src	Set Register Pointer 0 (8 LSB Working Registers)	–	–	–	–	–	–
SRP1	src	Set Register Pointer 1 (8 MSB Working Registers)	–	–	–	–	–	–
SPP	src	Set Page Pointer	–	–	–	–	–	–
EXT	src	Sign Extend	–	–	–	–	–	–
Miscellaneous (No Operand)								
Mnemonic	**Operand**	**Instruction**	**Flags**					
			C	**Z**	**S**	**V**	**D**	**H**
EI		Enable Interrupts	–	–	–	–	–	–
DI		Disable Interrupts	–	–	–	–	–	–
SCF		Set Carry Flag	1	–	–	–	–	–
RCF		Reset Carry Flag	0	–	–	–	–	–
CCF		Complement Carry Flag	Δ	–	–	–	–	–
SPM		Select Program Memory	–	–	–	–	–	–
SDM		Select Data Memory	–	–	–	–	–	–
NOP		No Operation	–	–	–	–	–	–

Mnemonic Code	Meaning	Flag Setting

PROCESSOR FLAGS

An important aspect of any single-chip microcontroller is the ability to test data and make the appropriate action based on the results. In order to provide this facility, register 231 in the Register File is used as a flag register. Six bits of this register are used as the following flags:

C - Carry
Z - Zero
S - Sign
V - Overflow
D - Decimal Adjust
H - Half Carry

One of the two remaining bits in the FLAG register is available to the user (bit 1, F1). Bit 0 is the Program/Data Memory selector bit and is operated on directly by the hardware within the ST9040. The P/D pin will follow the status of this bit.

CONDITION JUMP FLAGS

The flags C, Z, S and V control the operation of the Conditional Jump instructions. Figure 4.5 shows the conditional codes and the flag settings affecting the jump.

Table 24. Condition Codes Summary

F	Always False	—
T	Always True	—
C	Carry	C = 1
NC	No Carry	C = 0
Z	Zero	Z = 1
NZ	No Zero	Z = 0
PL	Plus	S = 0
MI	Minus	S = 1
OV	Overflow	V = 1
NOV	No Overflow	V = 0
EQ	Equal	Z = 1
NE	Not Equal	Z = 0
GE	Greater Than or Equal	(S xor V) = 0
LT	Less Than	(S xor V) = 1
GT	Greater Than	(Z or (S xor V)) = 0
LE	Less Than or Equal	(Z or (S xor V)) = 1
UGE	Unsigned Greater Than or Equal	C = 0
UL	Unsigned Less Than	C = 1
UGT	Unsigned Greater Than	(C = 0 and Z = 0) = 1
ULE	Unsigned Less Than or Equal	(C or Z) = 1

POWERFUL DEVELOPMENT ENVIRONMENT

ST9 SOFTWARE TOOLS. The following Software Tools are available for MS-DOS, VAX under VMS, SUN-3 and SUN-4 operating systems:

AST9 high-level macro assembler with predefined macro instructions(IF/ELSE, WHILE, DO, LOOP, SWITCH, BREAK, PROCEDURE, RETURN).

LST9 Incremental Linker/Loader.

CST9 Optimised C-Compiler (ANSI STANDARD).

ARST9 Library Archiver.

SIMST9 Software Simulator with realtime emulation executor.

ST9040 HARDWARE EMULATOR. Realtime Emulation of the ST9040 is performed by a modular emulation system, interfaced to the host computer through an RS232 channel, with powerful hardware breakpoints, on-line assembler/disassembler, emulation and trace memory. The emulator is fully supported by a symbolic on-line debugger and help facility.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	– 0.3 to 7.0	V
AV_{DD}, AV_{SS}	Analog Supply Voltage	$V_{SS} \le AV_{SS} < AV_{DD} \le V_{DD}$	V
V_I	Input Voltage	V_{SS} – 0.3 to V_{DD} +0.3	V
V_O	Output Voltage	V_{SS} – 0.3 to V_{DD} +0.3	V
T_{STG}	Storage Temperature	– 55 to + 150	°C

Note: Stresses above those listed as "absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value		Unit
		Min.	Max.	
T_A	Operating Temperature	– 40	85	°C
V_{DD}	Operating Supply Voltage	4.5	5.5	V
f_{OSCE}	External Oscillator Frequency		24	MHz
f_{OSCI}	Internal Oscillator Frequency		12	MHz

DC ELECTRICAL CHARACTERISTICS

(V_{DD} = 5V ± 10% T_A = – 40 °C to + 85°C, unless otherwise specified)

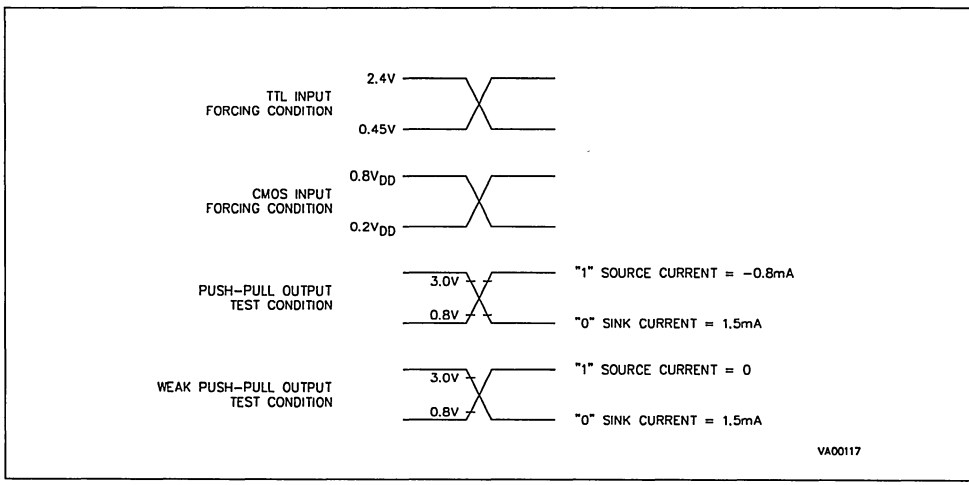
Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
V_{IHCK}	Clock Input High Level	External Clock	0.7 V_{DD}		V_{DD} + 0.3	V
V_{ILCK}	Clock Input Low Level	External Clock	– 0.3		0.3 V_{DD}	V
V_{IH}	Input High Level	TTL	2.0		V_{DD} + 0.3	V
		CMOS	0.7 V_{DD}		VDD + 0.3	V
V_{IL}	Input Low Level	TTL	– 0.3		0.8	V
		CMOS	– 0.3		0.3 V_{DD}	V
V_{IHRS}	Reset Input High Level		0.7 V_{DD}		V_{DD} + 0.3	V
V_{ILRS}	Reset Input Low Level		–0.3		0.3 V_{DD}	V
V_{HYRS}	Reset Input Hysteresis		0.3		1.5	V
V_{OH}	Output High Level	Push Pull, Iload = – 0.8mA	V_{DD} – 0.8			V
V_{OL}	Output Low Level	Push Pull or Open Drain, Iload = – 1.6mA			0.4	V
I_{WPU}	Weak Pull-up Current	Bidirectional Weak Pull-up, V_{OL} = 0V	– 80	– 200	– 420	µA

DC ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
I_{APU}	Active Pull-up Current, for INT0 and INT7 only	$V_{IN} < 0.8V$	– 80	– 200	– 420	µA
I_{LKIO}	I/O Pin Input Leakage	Input/Tri-State, $0V < V_{IN} < V_{DD}$	– 10		+ 10	µA
I_{LKRS}	Reset Pin Input Leakage	$0V < V_{IN} < V_{DD}$	– 30		+ 30	µA
I_{LKAD}	A/D Pin Input Leakage	Alternate Function, Open Drain, $0V < V_{IN} < V_{DD}$	– 3		+ 3	µA
I_{LKAP}	Active Pull-up Input Leakage	$0V < V_{IN} < 0.8V$	– 10		+ 10	µA
I_{LKOS}	OSCIN Pin Input Leakage	$0V < V_{IN} < V_{DD}$	– 10		+ 10	µA
I_{DD}	Run Mode Current	24MHz, Note 1		32	70	mA
		4MHz, Note 1		6	12	mA
I_{DP2}	Run Mode Current Prescale by 2	24MHz, Note 1		19	40	mA
		4MHz, Note 1		4	8	mA
I_{WFI}	WFI Mode Current	24MHz, Note 1		9	18	mA
		4MHz, Note 1		2.5	5	mA
I_{HALT}	HALT Mode Current	24MHz, Note 1			100	µA

Note:
1. All I/O Ports are configured in Bidirectional Weak Pull-up Mode with no DC load, External Clock pin (OSCIN) is driven by square wave external clock. No peripheral working. External interface not active (Internal Program Execution).

DC TEST CONDITIONS



AC ELECTRICAL CHARACTERISTICS

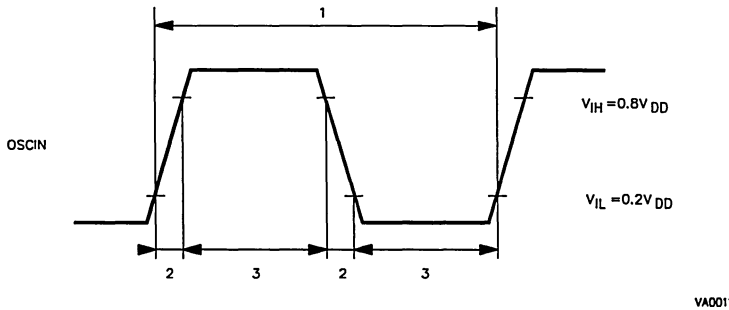
CLOCK TIMING TABLE

(V_{DD} = 5V ± 10%, T_A = − 40°C to + 85°C, unless otherwise specified)

N°	Symbol	Parameter	Value		Unit	Note
			Min.	Max.		
1	TpC	OSCIN Clock Period	41.5		ns	1
			83		ns	2
2	TrC, TfC	OSCIN Rise and Fall Time		12	ns	
3	TwCL, TwCH	OSCIN Low and High Width	25	12	ns	1
			38		ns	2

Note: 1. Clock divided by 2 internally (MODER.DIV2=1)
2. Clock not divided by 2 internally (MODER.DIV2=0)

CLOCK TIMING



EXTERNAL BUS TIMING TABLE

(V_{DD} = 5V ± 10%, T_A = – 40 °C to + 85 °C, Cload = 50pF, CPUCLK = 12MHz, unless otherwise specified)

N°	Symbol	Parameter	Value (Note)				Unit
			OSCIN Divided By 2	OSCIN Not Divided By 2	Min.	Max.	
1	TsA (AS)	Address Set-up Time before $\overline{AS}$ ↑	TpC (2P+1) –22	TWCH+PTpC –18	20		ns
2	ThAS (A)	Address Hold Time after $\overline{AS}$ ↑	TpC –17	TwCL –13	25		ns
3	TdAS (DR)	$\overline{AS}$ ↑ to Data Available (read)	TpC (4P+2W+4) –52	TpC (2P+W+2) –51		115	ns
4	TwAS	$\overline{AS}$ Low Pulse Width	TpC (2P+1) –7	TwCH+PTpC –3	35		ns
5	TdAz (DS)	Address Float to $\overline{DS}$ ↓	0	0	0		ns
6	TwDSR	$\overline{DS}$ Low Pulse Width (read)	TpC (4P+2W+3) –20	TwCH+TpC (2P+W+1) – 16	105		ns
7	TwDSW	$\overline{DS}$ Low Pulse Width (write)	TpC (2P+2W+2) –13	TpC (P+W+1) –13	70		ns
8	TdDSR (DR)	$\overline{DS}$ ↓ to Data Valid Delay (read)	TpC (4P+2W-3) –50	TwCH+TpC(2P+W+1) – 46		75	ns
9	ThDR (DS)	Data to $\overline{DS}$ ↑ Hold Time (read)	0	0	0		ns
10	TdDS (A)	$\overline{DS}$ ↑ to Address Active Delay	TpC –7	TwCL –3	35		ns
11	TdDS (AS)	$\overline{DS}$ ↑ to $\overline{AS}$ ↓ Delay	TpC –18	TwCL –14	24		ns
12	TsR/W (AS)	R/$\overline{W}$ Set-up Time before $\overline{AS}$ ↑	TpC (2P+1) –22	TwCH+PTpC –18	20		ns
13	TdDSR (R/W)	$\overline{DS}$ ↑ to R/$\overline{W}$ and Address Not Valid Delay	TpC –9	TwCL –5	33		ns
14	TdDW (DSW)	Write Data Valid to $\overline{DS}$ ↓ Delay (write)	TpC (2P+1) –32	TwCH+PTpC –28	10		ns
15	ThDS (DW)	Data Hold Time after DS ↑ (write)	TpC –9	TwCL –5	33		ns
16	TdA (DR)	Address Valid to Data Valid Delay (read)	TpC (6P+2W+5) –68	TwCH+TpC (3P+W+2) – 64		140	ns
17	TdAs (DS)	$\overline{AS}$ ↑ to $\overline{DS}$ ↓ Delay	TpC –18	TwCL –14	24		ns

Note: The value left hand two columns show the formula used to calculate the timing minimum or maximum from the oscillator clock period, prescale value and number of wait cycles inserted.
The value right hand two columns show the timing minimum and maximum for an external clock at 24 MHz divided by 2, prescaler value of zero and zero wait status.

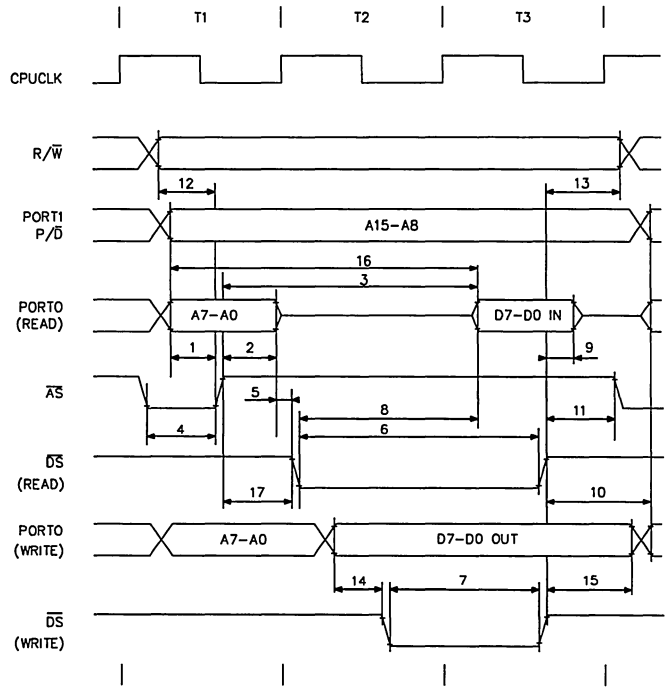
Legend:
P = Clock Prescaling Value
W = Wait Cycles
TpC = OSCIN Period
TwCH = High Level OSCIN half period
TwCL = Low Level OSCIN half period

EXTERNAL WAIT TIMING TABLE (V_{DD} = 5V ± 10%, T_A = –40°C to +85°C, Cload = 50pF, INTCLK = 12MHz, Push-pull output configuration, unless otherwise specified)

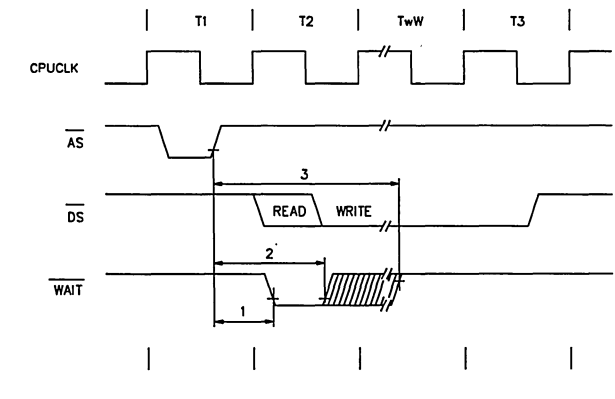
N°	Symbol	Parameter	Value (Note)				Unit
			OSCIN Divided By 2	OSCIN Not Divided By 2	Min.	Max.	
1	TdAS (WAIT)	$\overline{AS}$ ↑ to $\overline{WAIT}$ ↓ Delay	2(P+1)TpC –29	(P+1)TpC –29		40	ns
2	TdAS (WAIT)	$\overline{AS}$ ↑ to $\overline{WAIT}$ ↑ Minimum Delay	2(P+W+1)TpC –4	(P+W+1)TpC –4	80		ns
3	TdAS (WAIT)	$\overline{AS}$ ↑ to $\overline{WAIT}$ ↑ Maximum Delay	2(P+W+1)TpC –29	(P+W+1)TpC –29		83W+40	ns

Note: The value left hand two columns show the formula used to calculate the timing minimum or maximum from the oscillator clock period, prescale value and number of wait cycles inserted.
The value right hand two columns show the timing minimum and maximum for an external clock at 24 MHz divided by 2, prescale value of zero and zero wait status.

EXTERNAL BUS TIMING



EXTERNAL WAIT TIMING

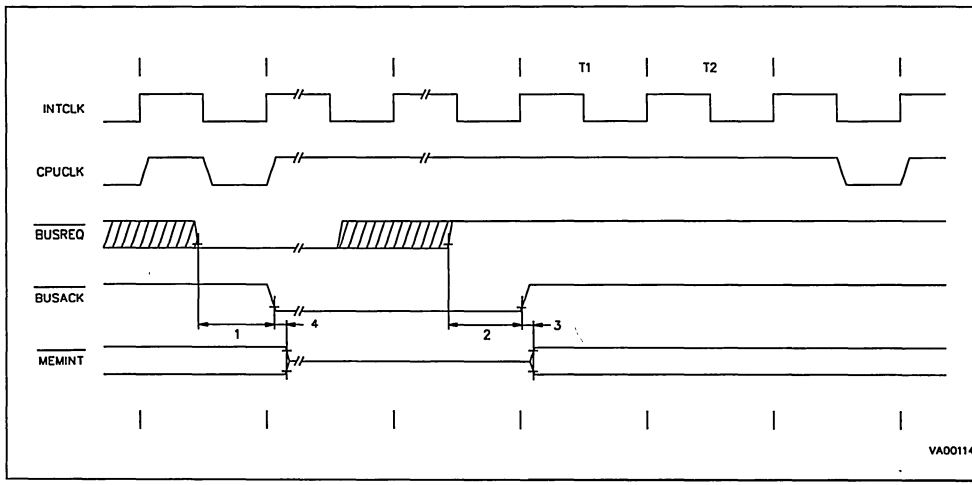


BUS REQUEST/ACKNOWLEDGE TIMING TABLE (V_{DD} = 5V ± 10%, T_A = −40°C to +85°C, Cload = 50pF, INTCLK = 12MHz, Push-pull output configuration, unless otherwise specified)

N°	Symbol	Parameter	Value (Note)				Unit
			OSCIN Divided By 2	OSCIN Not Divided By 2	Min.	Max.	
1	TdBR (BACK)	$\overline{BREQ}$ ↓ to $\overline{BUSACK}$ ↓	TpC+8	TwCL+12	50		ns
			TpC(6P+2W+7)+65	TpC(3P+W+3)+TwCL+65		360	ns
2	TdBR (BACK)	$\overline{BREQ}$ ↑ to $\overline{BUSACK}$ ↑	3TpC+60	TpC+TwCL+60		185	ns
3	TdBACK (BREL)	$\overline{BUSACK}$ ↓ to Bus Release	20	20		20	ns
4	TdBACK (BACT)	$\overline{BUSACK}$ ↑ to Bus Active	20	20		20	ns

Note: The value left hand two columns show the formula used to calculate the timing minimum or maximum from the oscillator clock period, prescale value and number of wait cycles inserted.
The value right hand two columns show the timing minimum and maximum for an external clock at 24 MHz divided by 2, prescale value of zero and zero wait status.

BUS REQUEST/ACKNOWLEDGE TIMING



Note : MEMINT = group of memory interface signals : $\overline{AS}$, $\overline{DS}$, R/$\overline{W}$, P00-P07, P10-P17.

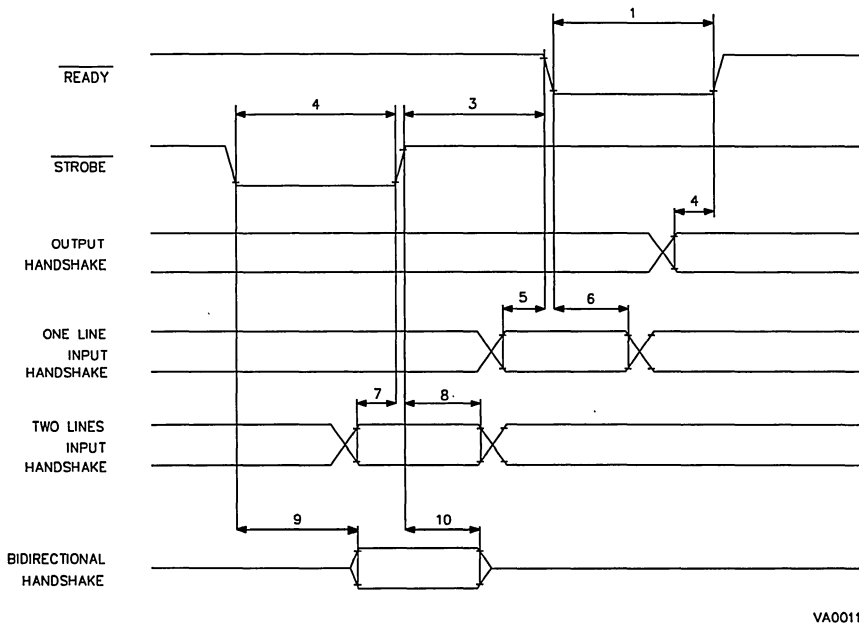
HANDSHAKE TIMING TABLE (V_{DD} = 5V ± 10%, T_A = –40°C to +85°C, Cload = 50pF, INTCLK = 12MHz, Push-pull output configuration, unless otherwise specified)

N°	Symbol	Parameter	Value (Note)				Min.	Max.	Unit
			OSCIN Divided By 2		OSCIN Not Divided By 2				
			Min.	Max.	Min.	Max.			
1	TwRDY	RDRDY, WRRDY Pulse Width in One Line Handshake	2TpC (P+W+1) –18		TpC (P+W+1) –18		65		ns
2	TwSTB	$\overline{RDSTB}$, $\overline{WRSTB}$ Pulse Width	2TpC+12		TpC+12		95		ns
3	TdST (RDY)	$\overline{RDSTB}$, or $\overline{WRSTB}$ ↑ to RDRDY or WRRDY ↓		TpC+45		(TpC-TwCL) +45		87	ns
4	TsPD (RDY)	Port Data to RDRDY ↑ Set-up Time	(2P+2W+1) TpC –25		TwCH+(W+P) TpC –25		16		ns
5	TsPD (RDY)	Port Data to WRRDY ↓ Set-up Time in One Line Handshake	43		43		43		ns
6	ThPD (RDY)	Port Data to WRRDY ↓ Hold Time in One Line Handshake	0		0		0		ns
7	TsPD (STB)	Port Data to $\overline{WRSTB}$ ↑ Set-up Time	10		10		10		ns
8	ThPD (STB)	Port Data to WRSTB ↑ Hold Time	25		25		25		ns
9	TdSTB (PD)	$\overline{RDSTBD}$ ↑ to Port Data Delay Time in Bidirectional Hand-shake		35		35		35	ns
10	TdSTB (PHZ)	$\overline{RDSTB}$ ↑ to Port High-Z Delay Time in Bidirectional Hand-shake		25		25		25	ns

Note: The value left hand two columns show the formula used to calculate the timing minimum or maximum from the oscillator clock period, prescale value and number of wait cycles inserted.
The value right hand two columns show the timing minimum and maximum for an external clock at 24 MHz divided by 2, prescaler value of zero and zero wait status.

Legend:
P = Clock Prescaling Value (R235.4,3,2)
W = Programmable Wait Cycles (R252.2.1.0/5,4,3) + External Wait Cycles

HANDSHAKE TIMING

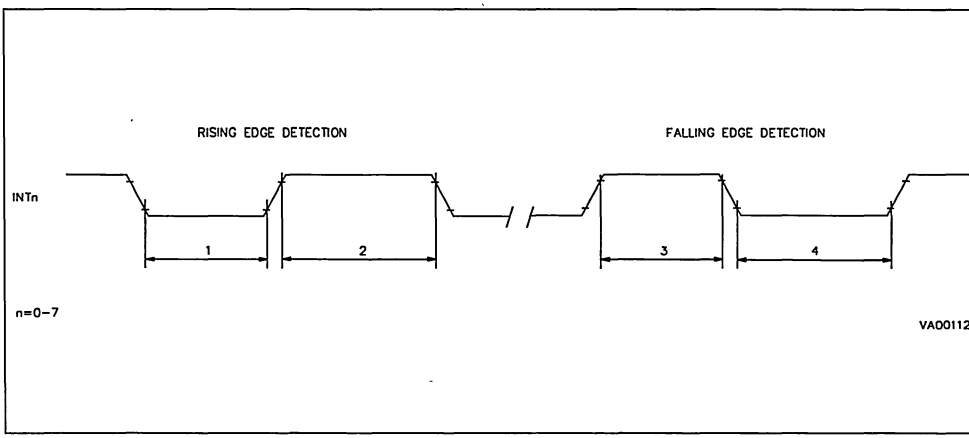


EXTERNAL INTERRUPT TIMING TABLE (V_{DD} = 5V ± 10%, T_A = –40°C to +85°C, Cload = 50pF, INTCLK = 12MHz, Push-pull output configuration, unless otherwise specified)

N°	Symbol	Parameter	Value (Note)				Unit
			OSCIN Divided By 2 Min.	OSCIN Not Divided By 2 Min.	Min.	Max.	
1	TwLR	Low Level Minimum Pulse Width in Rising Edge Mode	2TpC+12	TpC+12	95		ns
2	TwHR	High Level Minimum Pulse Width in Rising Edge Mode	2TpC+12	TpC+12	95		ns
3	TwHF	High Level Minimum Pulse Width in Falling Edge Mode	2TpC+12	TpC+12	95		ns
4	TwLF	Low Level Minimum Pulse Width in Falling Edge Mode	2TpC+12	TpC+12	95		ns

Note: The value left hand two columns show the formula used to calculate the timing minimum or maximum from the oscillator clock period, prescale value and number of wait cycles inserted.
The value right hand two columns show the timing minimum and maximum for an external clock at 24 MHz divided by 2, prescale value of zero and zero wait status.

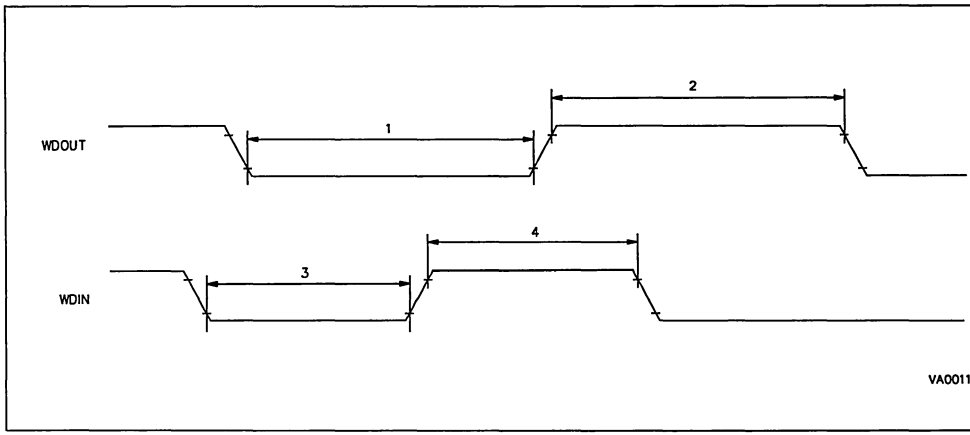
EXTERNAL INTERRUPT TIMING



WATCHDOG TIMING TABLE (V_{DD} = 5V ± 10%, T_A = –40°C to +85°C, Cload = 50pF, INTCLK =12MHz, Output Alternate Function set as Push-pull)

N°	Symbol	Parameter	Value		Unit
			Min.	Max.	
1	TwWDOL	WDOUT Low Pulse Width	620		ns
2	TwWDOH	WDOUT High Pulse Width	620		ns
3	TwWDIL	WDIN Low Pulse Width	350		ns
4	TwWDIH	WDIN High Pulse Width	350		ns

WATCHDOG TIMING

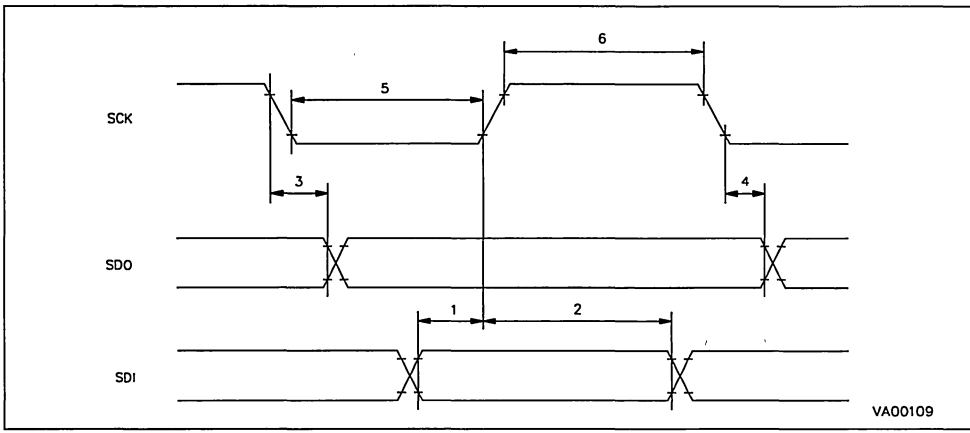


SPI TIMING TABLE (V_{DD} = 5V ± 10%, T_A = –40°C to +85°C, Cload = 50pF, INTCLK = 12MHz, Output Alternate Function set as Push-pull)

N°	Symbol	Parameter	Value		Unit
			Min.	Max.	
1	TsDI	Input Data Set-up Time	100		ns
2	ThDI (1)	Input Data Hold Time	1/2 TpC+100		ns
3	TdOV	SCK to Output Data Valid		100	ns
4	ThDO	Output Data Hold Time	-20		ns
5	TwSKL	SCK Low Pulse Width	300		ns
6	TwSKH	SCK High Pulse Width	300		ns

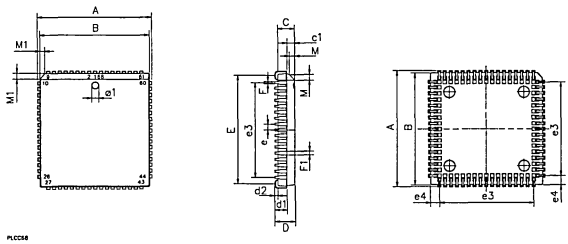
Note: 1. TpC is the Clock period.

SPI TIMING



PACKAGE MECHANICAL DATA

Figure 53. 68-Lead Plastic Leaded Chip Carrier (C)



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A	25.02		25.27	0.985		0.995
B	24.13		24.33	0.950		0.958
D	4.20		5.08	0.165		0.200
d1		2.54			0.100	
d2		0.56			0.022	
E	22.61		23.62	0.890		0.930
e		1.27			0.050	
F		0.38			0.015	
G			0.10			0.004
M		1.27			0.050	
M1		1.14			0.044	
Ø1		7.36			0.289	

ORDERING INFORMATION

Sales Type	Frequency	Temperature Range	Package
ST9040C6/XX	24MHz	– 40°C to + 85°C	PLCC68
ST9040C1/XX	24MHz	0°C to +70°C	PLCC68

Note: "XX" is the ROM code identifier that is allocated by SGS-THOMSON after receipt of all required options and the related ROM file.

ST9040 OPTION LIST

Please copy this page (enlarge if possible) and complete ALL sections. Send the form, with the ROM code image required, to your local SGS-THOMSON sales office.

Customer Company : [.....]

Company Address : [.....]

[.....]

Telephone : [.....]

FAX : [.....]

Contact : [.....] Telephone (Direct) : [.....]

Please confirm device required :

Temperature Range [ ] (t)

Special Marking [ ] (y/n) 11 characters [| | | | | | | | | | |] (N)

Notes :

(t) 1 = 0 to +70°C, 6 = -40 to +85°C
(N) Available : ASCII 020h - 05Fh

Please consult your local SGS-THOMSON sales office for other marking details

ROMLESS OPTION (consult text)
[ ] YES [ ] NO
If yes, identify required pin (Port.bit)
[ ] P3.7 [ ] P2.0

Code : [ ] EPROM (27128, 27256)
[ ] HEX format files on IBM-PC® compatible disk
filename : [.....]

Confirmation : [ ] Code checked with EPROM device in application

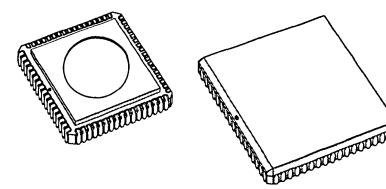
Yearly Quantity forecast : [.....] k units
- for a period of : [.....] years
Preferred Production start dates : [.....] (YY/MM/DD)

Customer Signature : [.....]

Date : [.....]

16K EPROM HCMOS MCUs WITH RAM AND EEPROM

- Single chip microcontroller with 16K bytes of EPROM, 256 bytes of RAM and 256 bytes of register file with 224 general purpose registers available as RAM, accumulators or index pointers.
- 512 bytes of high-reliability EEPROM on-chip, with 300,000 erase/write cycle capability and 10 year data retention.
- On-chip programmable security protection against external reading of internal memory.
- 8/16 bit CORE with full feature DMA controller, a powerful interrupt handler and a Standard Serial Peripheral Interface (SPI) handling S-bus, I^2C-bus, IM-bus and Standard Serial Peripheral Interfaces.
- Up to 8 external interrupts edge-selectable plus 1 non-maskable interrupt.
- 16 bit programmable Timer with 8 bit Prescaler, able to be used as a Watchdog Timer for system integrity.
- Two 16 bit Multifunction Timer modules, each with an 8 bit prescaler and 13 operating modes, allowing simple use for complex waveform generation and measurement, PWM functions and many other system timing operations.
- 8 channel Analog to Digital Converter, with integral sample and hold, fast 11µs conversion time, 8 bit ±1/2 LSB resolution with Analog Watchdog on two channels.
- Full function Serial Communications Interface with 110 to 375,000 baud rate generator, asynchronous and byte synchronous capability (fully programmable format) and address/wake-up bit option.
- On-chip DMA channels associated to the Multifunction Timers and the Serial Communications Interface.
- Up to seven 8 bit I/O ports with programmable input thresholds and output characteristics. Alternative functions allow the full use of all pins.
- Powerful software development tools, including assembler, linker, C-compiler, archiver, software and hardware emulators.
- Windowed and One Time Programmable EPROM parts available for prototyping and preproduction development phases.
- 68-lead Ceramic Windowed package for ST90E40



CLCC68W PLCC68

(Ordering Information at the end of the datasheet)

Figure 1. ST90E40 Block Diagram

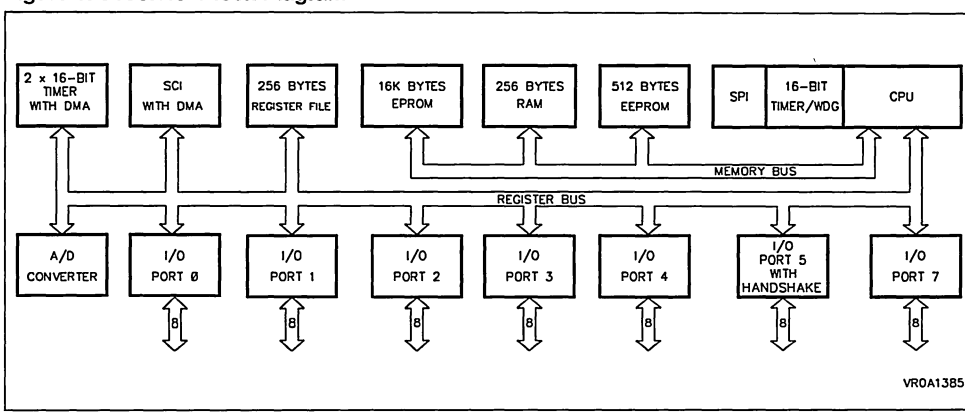
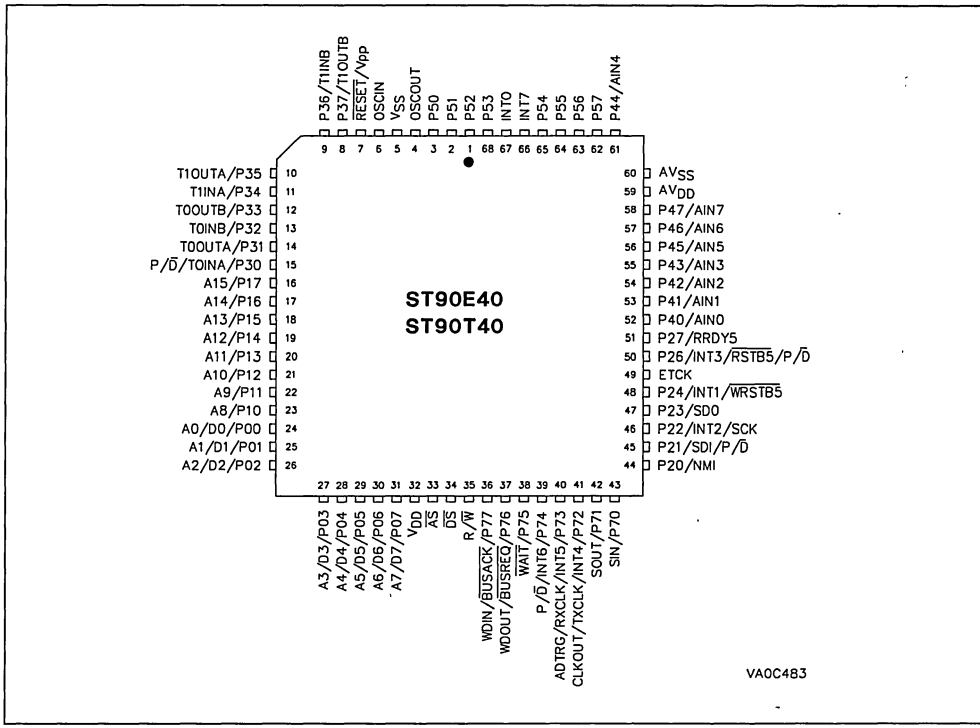


Figure 2. ST90E40 Pin Configuration



GENERAL DESCRIPTION

The ST90E40 and ST90T40 are EPROM members with EEPROM of the ST9 family of microcontrollers, in windowed ceramic (E) and plastic OTP (T) packages respectively, completely developed and produced by SGS-THOMSON Microelectronics using a n-well proprietary HCMOS process.

The EPROM parts are fully compatible with their ROM versions and this datasheet will thus provide only information specific to the EPROM based devices.

THE READER IS ASKED TO REFER TO THE DATASHEET OF THE ST9040 ROM-BASED DEVICE FOR FURTHER DETAILS.

The EPROM ST90E40 may be used for the prototyping and pre-production phases of development, and can be configured as: a standalone microcontroller with 16K bytes of on-chip ROM, a microcontroller able to manage up to 112K bytes of external memory, or as a parallel processing element in a system with other processors and peripheral controllers.

A key point of the ST90E40 architecture is its modular approach which allows software commonality with all other members of the ST9 family.

The nucleus of the modular design of the ST90E40 is the advanced Core which includes the Central Processing Unit (CPU), the Register File, a 16 bit Timer/Watchdog with 8 bit Prescaler, a Serial Peripheral Interface supporting S-bus, I^2C-bus and IM-bus Interface, plus two 8 bit I/O ports. The Core has independent memory and register buses allowing a high degree of pipelining to add to the efficiency of the code execution speed of the extensive instruction set.

The powerful I/O capabilities demanded by microcontroller applications are fulfilled by the ST90E40 with up to 56 I/O lines dedicated to digital Input/Output. These lines are grouped into up to seven 8 bit I/O Ports and can be configured on a bit basis under software control to provide timing, status signals, an address/data bus for interfacing external memory, timer inputs and outputs, analog inputs, external interrupts and serial or parallel I/O with or without handshake.

GENERAL DESCRIPTION (Continued)

Three basic memory spaces are available to support this wide range of configurations: Program Memory (internal and external), Data Memory (external) and the Register File, which includes the control and status registers of the on-chip peripherals.

Two 16 bit MultiFunction Timers, each with an 8 bit Prescaler and 13 operating modes allow simple use for complex waveform generation and measurement, PWM functions and many other system timing functions by the usage of the two associated DMA channels for each timer.

In addition there is an 8 channel Analog to Digital Converter with integral sample and hold, fast 11µs conversion time and 8 bit ±1/2 LSB resolution. An Analog Watchdog feature is included for two input channels.

Completing the device is a full duplex Serial Communications Interface with an integral 110 to 375,000 baud rate generator, asynchronous and byte synchronous capability (fully programmable format) and associated address/wake-up option, plus two DMA channels.

PIN DESCRIPTION

$\overline{AS}$. *Address Strobe (output, active low, 3-state).* Address Strobe is pulsed low once at the beginning of each memory cycle. The rising edge of $\overline{AS}$ indicates that address, Read/Write (R/$\overline{W}$), and Data Memory signals are valid for program or data memory transfers. Under program control, $\overline{AS}$ can be placed in a high-impedance state along with Port 0 and Port 1, Data Strobe ($\overline{DS}$) and R/$\overline{W}$.

$\overline{DS}$. *Data Strobe (output, active low, 3-state).* Data Strobe provides the timing for data movement to or from Port 0 for each memory transfer. During a write cycle, data out is valid at the leading edge of $\overline{DS}$. During a read cycle, Data In must be valid prior to the trailing edge of $\overline{DS}$. When the ST90E40 accesses on-chip memory, $\overline{DS}$ is held high during the whole memory cycle. It can be placed in a high impedance state along with Port 0, Port 1, $\overline{AS}$ and R/$\overline{W}$.

R/$\overline{W}$. *Read/Write (output, 3-state).* Read/Write determines the direction of data transfer for external memory transactions. R/$\overline{W}$ is low when writing to external program or data memory, and high for all other transactions. It can be placed in a high impedance state along with Port 0, Port 1, $\overline{AS}$ and $\overline{DS}$.

$\overline{RESET}$/V_{PP}. *Reset (input, active low) or V_{PP} (input).* The ST9 is initialised by the Reset signal. With the deactivation of $\overline{RESET}$, program execution begins from the Program memory location pointed to by the vector contained in program memory locations 00h and 01h. In the EPROM programming Mode, this pin acts as the programming voltage input VPP.

OSCIN, OSCOUT. *Oscillator (input and output).* These pins connect a parallel-resonant crystal (24MHz maximum), or an external source to the on-chip clock oscillator and buffer. OSCIN is the input of the oscillator inverter and internal clock generator; OSCOUT is the output of the oscillator inverter.

AV_{DD}. Analog V_{DD} of the Analog to Digital Converter.

AV_{SS}. Analog V_{SS} of the Analog to Digital Converter.

V_{DD}. Main Power Supply Voltage (5V±10%)

V_{SS}. Digital Circuit Ground.

P0.0-P0.7, P1.0-P1.7, P2.0-P2.7 P3.0-P3.7, P4.0-P4.7, P5.0-P5.7, P7.0-P7.7 *I/O Port Lines (Input/Output, TTL or CMOS compatible).* 8 lines grouped into I/O ports of 8 bits, bit programmable under program control as general purpose I/O or as Alternate functions (see next section).

I/O Port Alternate Functions.

Each pin of the I/O ports of the ST90E40 may assume software programmable Alternative Functions as shown in the Pin Configuration Drawings. figure 1.2 shows the Functions allocated to each I/O Port pins.

PIN DESCRIPTION (Continued)

Table 1. ST90E40 I/O Port Alternate Function Summary

I/O PORT Port.bit	Name	Function IN/OUT	Alternate Function	Pin Number
P0.0	A0/D0	I/O	Address/Data bit 0 mux	24
P0.1	A1/D1	I/O	Address/Data bit 1 mux	25
P0.2	A2/D2	I/O	Address/Data bit 2 mux	26
P0.3	A3/D3	I/O	Address/Data bit 3 mux	27
P0.4	A4/D4	I/O	Address/Data bit 4 mux	28
P0.5	A5/D5	I/O	Address/Data bit 5 mux	29
P0.6	A6/D6	I/O	Address/Data bit 6 mux	30
P0.7	A7/D7	I/O	Address/Data bit 7 mux	31
P1.0	A8	O	Address bit 8	23
P1.1	A9	O	Address bit 9	22
P1.2	A10	O	Address bit 10	21
P1.3	A11	O	Address bit 11	20
P1.4	A12	O	Address bit 12	19
P1.5	A13	O	Address bit 13	18
P1.6	A14	O	Address bit 14	17
P1.7	A15	O	Address bit 15	16
P2.0	NMI	I	Non-Maskable Interrupt	44
P2.1	$P/\overline{D}$	O	Program/Data Space Select	45
P2.1	SDI	I	SPI Serial Data Out	45
P2.2	INT2	I	External Interrupt 2	46
P2.2	SCK	O	SPI Serial Clock	46
P2.3	SDO	O	SPI Serial Data In	47
P2.4	INT1	I	External Interrupt 1	48
P2.4	$\overline{WRSTB5}$	O	Handshake Write Strobe P5	48
P2.5	WRRDY5	I	Handshake Write Ready P5	49
P2.6	INT3	I	External Interrupt 3	50
P2.6	$\overline{RDSTB5}$	I	Handshake Read Strobe P5	50

PIN DESCRIPTION (Continued)

Table 1. ST90E40 I/O Port Alternate Function Summary (Continued)

I/O PORT Port.bit	Name	Function IN/OUT	Alternate Function	Pin Number
P2.6	P/D	O	Program/Data Space Select	50
P2.7	RDRDY5	O	Handshake Read Ready P5	51
P3.0	T0INA	I	MF Timer 0 Input A	15
P3.0	P/$\overline{D}$	O	Program/Data Space Select	15
P3.1	T0OUTA	O	MF Timer 0 Output A	14
P3.2	T0INB	I	MF Timer 0 Input B	13
P3.3	T0OUTB	O	MF Timer 0 Output B	12
P3.4	T1INA	I	MF Timer 1 Input A	11
P3.5	T1OUTA	O	MF Timer 1 Output A	10
P3.6	T1INB	I	MF Timer 1 Input B	9
P3.7	T1OUTB	O	MF Timer 1 Output B	8
P4.0	AIN0	I	A/D Analog Input 0	52
P4.1	AIN1	I	A/D Analog Input 1	53
P4.2	AIN2	I	A/D Analog Input 2	54
P4.3	AIN3	I	A/D Analog Input 3	55
P4.4	AIN4	I	A/D Analog Input 4	61
P4.5	AIN5	I	A/D Analog Input 5	56
P4.6	AIN6	I	A/D Analog Input 6	57
P4.7	AIN7	I	A/D Analog Input 7	58
P5.0		I/O	I/O Handshake Port 5	3
P5.1		I/O	I/O Handshake Port 5	2
P5.2		I/O	I/O Handshake Port 5	1
P5.3		I/O	I/O Handshake Port 5	68
P5.4		I/O	I/O Handshake Port 5	65
P5.5		I/O	I/O Handshake Port 5	64
P5.6		I/O	I/O Handshake Port 5	63
P5.7		I/O	I/O Handshake Port 5	62

PIN DESCRIPTION (Continued)

Table 1. ST90E40 I/O Port Alternate Function Summary (Continued)

I/O PORT Port.bit	Name	Function IN/OUT	Alternate Function	Pin Number
P7.0	SIN	I	SCI Serial Input	43
P7.1	SOUT	O	SCI Serial Output	42
P7.2	INT4	I	External Interrupt 4	41
P7.2	TXCLK	I	SCI Transmit Clock Input	41
P7.2	CLKOUT	O	SCI Byte Sync Clock Output	41
P7.3	INT5	I	External Interrupt 5	40
P7.3	RXCLK	I	SCI Receive Clock Input	40
P7.3	ADTRG	I	A/D Conversion Trigger	40
P7.4	INT6	I	External Interrupt 6	39
P7.4	P/$\overline{D}$	O	Program/Data Space Select	39
P7.5	$\overline{WAIT}$	I	External Wait Input	38
P7.6	WDOUT	O	T/WD Output	37
P7.6	$\overline{BUSREQ}$	I	External Bus Request	37
P7.7	WDIN	I	T/WD Input	36
P7.7	$\overline{BUSACK}$	O	External Bus Acknowledge	36

MEMORY

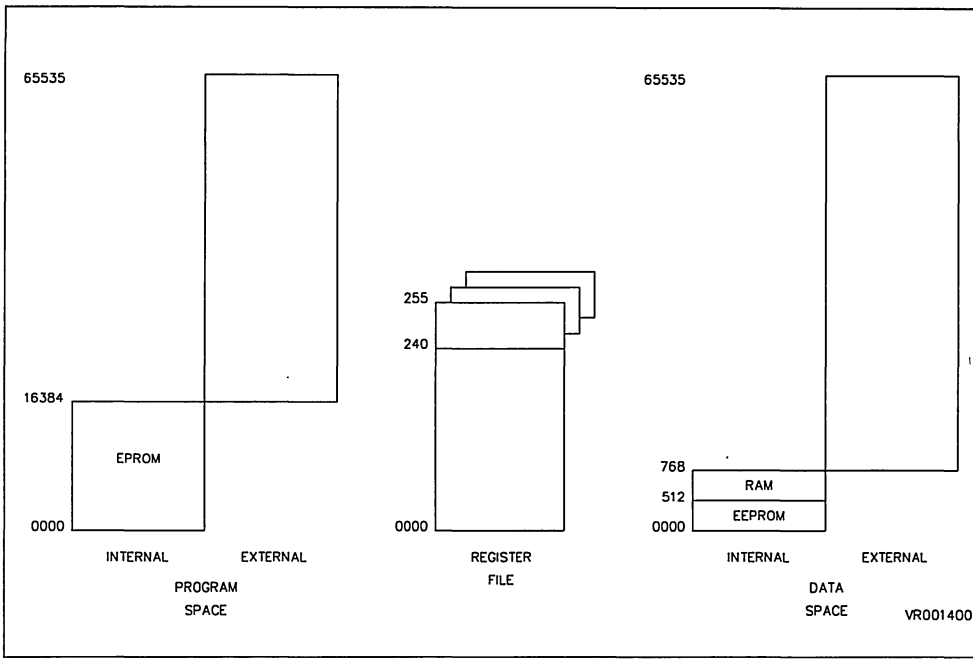
The memory of the ST90E40 is functionally divided into two areas, the Register File and Memory. The Memory is divided into two spaces, each having a maximum of 65,536 bytes. The two memory spaces are separated by function, one space for Program code, the other for Data. The ST90E40 16K bytes of on-chip EPROM memory are selected at memory addresses 0 through 3FFFh (hexadecimal) in the PROGRAM space, while the ST90T40 OTP version has the top 64 bytes of the EPROM reserved by SGS-THOMSON for testing purposes. The DATA space includes the 512 bytes of on-chip EEPROM at addresses 0 through 1FFh and the 256 bytes of on-chip RAM memory at memory addresses 200h through 2FFh.

External memory may be addressed using the multiplexed address and data buses (Alternate Functions of Ports 0 and 1). At addresses greater than the first 16K of program space, the ST90E40 executes external memory cycles for instruction fetches. Additional Data Memory may be decoded externally by using the P/$\overline{D}$ Alternate Function output. The on-chip general purpose (GP) Registers may also be used as RAM memory for minimum chip count systems.

EPROM PROGRAMMING

The 16384 bytes of EPROM memory of the ST90E40 (16320 for the ST90T40) may be programmed by using the EPROM Programming Boards (EPB) available from SGS-THOMSON.

Figure 3. Memory Spaces



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	– 0.3 to 7.0	V
AV_{DD}, AV_{SS}	Analog Supply Voltage	$V_{SS} \le AV_{SS} < AV_{DD} \le V_{DD}$	V
V_I	Input Voltage	V_{SS} – 0.3 to V_{DD} +0.3	V
V_O	Output Voltage	V_{SS} – 0.3 to V_{DD} +0.3	V
V_{PP}	Input Voltage on V_{PP} Pin	– 0.3 to 13.5	V
T_{STG}	Storage Temperature	– 55 to + 150	°C

Note: Stresses above those listed as "absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value		Unit
		Min.	Max.	
T_A	Operating Temperature	– 40	85	°C
V_{DD}	Operating Supply Voltage	4.5	5.5	V
f_{OSCE}	External Oscillator Frequency		24	MHz
f_{OSCI}	Internal Oscillator Frequency		12	MHz

DC ELECTRICAL CHARACTERISTICS

(V_{DD} = 5V ± 10% T_A = – 40 °C to + 85°C, unless otherwise specified)

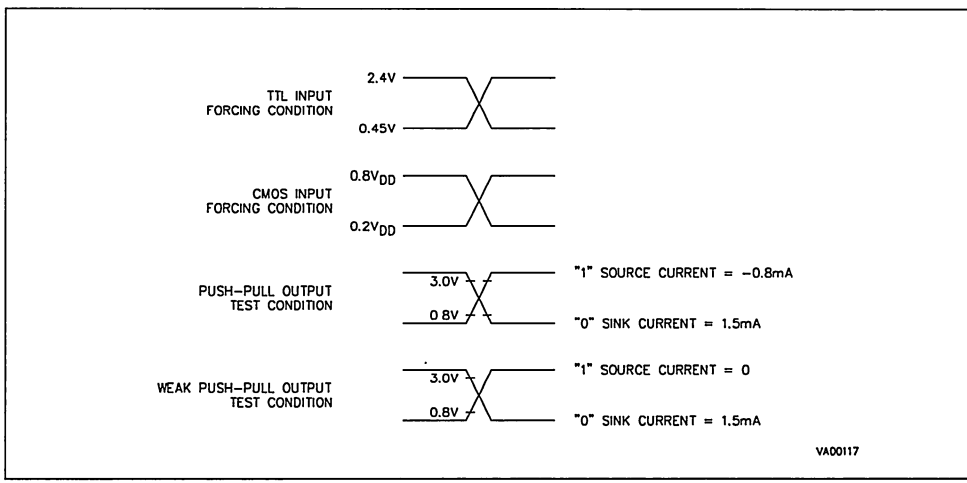
Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
V_{IHCK}	Clock Input High Level	External Clock	0.7 V_{DD}		V_{DD} + 0.3	V
V_{ILCK}	Clock Input Low Level	External Clock	– 0.3		0.3 V_{DD}	V
V_{IH}	Input High Level	TTL	2.0		V_{DD} + 0.3	V
		CMOS	0.7 V_{DD}		VDD + 0.3	V
V_{IL}	Input Low Level	TTL	– 0.3		0.8	V
		CMOS	– 0.3		0.3 V_{DD}	V
V_{IHRS}	Reset Input High Level		0.7 V_{DD}		V_{DD} + 0.3	V
V_{ILRS}	Reset Input Low Level		–0.3		0.3 V_{DD}	V
V_{HYRS}	Reset Input Hysteresis		0.3		1.5	V
V_{OH}	Output High Level	Push Pull, Iload = – 0.8mA	V_{DD} – 0.8			V
V_{OL}	Output Low Level	Push Pull or Open Drain, Iload = – 1.6mA			0.4	V
I_{WPU}	Weak Pull-up Current	Bidirectional Weak Pull-up, V_{OL} = 0V	– 80	– 200	– 420	µA

DC ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
I_{APU}	Active Pull-up Current, for INT0 and INT7 only	$V_{IN} < 0.8V$	– 80	– 200	– 420	µA
I_{LKIO}	I/O Pin Input Leakage	Input/Tri-State, $0V < V_{IN} < V_{DD}$	– 10		+ 10	µA
I_{LKRS}	Reset Pin Input Leakage	$0V < V_{IN} < V_{DD}$	– 30		+ 30	µA
I_{LKAD}	A/D Pin Input Leakage	Alternate Function, Open Drain, $0V < V_{IN} < V_{DD}$	– 3		+ 3	µA
I_{LKAP}	Active Pull-up Input Leakage	$0V < V_{IN} < 0.8V$	– 10		+ 10	µA
I_{LKOS}	OSCIN Pin Input Leakage	$0V < V_{IN} < V_{DD}$	– 10		+ 10	µA
I_{DD}	Run Mode Current	24MHz, Note 1		32	70	mA
		4MHz, Note 1		6	12	mA
I_{DP2}	Run Mode Current Prescale by 2	24MHz, Note 1		19	40	mA
		4MHz, Note 1		4	8	mA
I_{WFI}	WFI Mode Current	24MHz, Note 1		9	18	mA
		4MHz, Note 1		2.5	5	mA
I_{HALT}	HALT Mode Current	24MHz, Note 1			100	µA
V_{PP}	EPROM Programming Voltage		12.2	12.5	12.8	V
I_{PP}	EPROM Programming Current				30	mA

Note: 1. All I/O Ports are configured in Bidirectional Weak Pull-up Mode with no DC load, External Clock pin (OSCIN) is driven by square wave external clock. No peripheral working. External interface not active (Internal Program Execution).

DC TEST CONDITIONS



AC ELECTRICAL CHARACTERISTICS

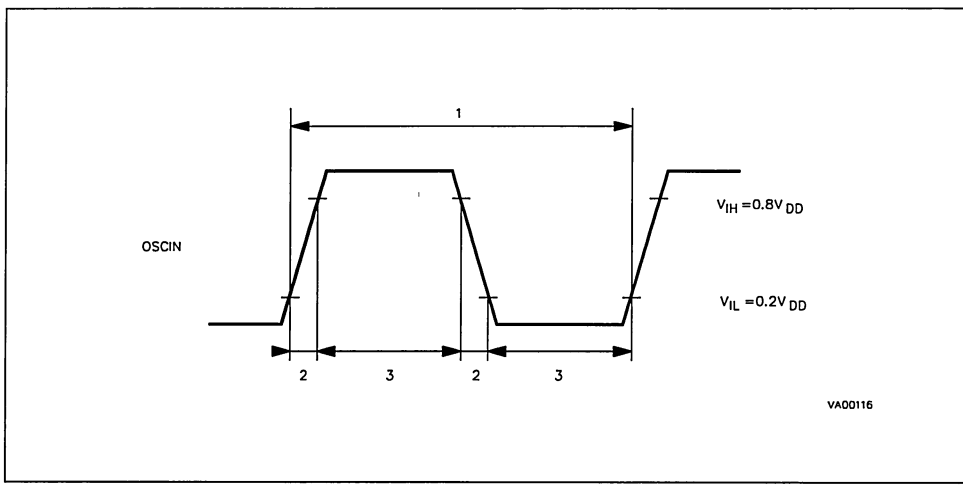
CLOCK TIMING TABLE

(V_{DD} = 5V ± 10%, T_A = − 40°C to + 85°C, unless otherwise specified)

N°	Symbol	Parameter	Value		Unit	Note
			Min.	Max.		
1	TpC	OSCIN Clock Period	41.5		ns	a
			83		ns	b
2	TrC, TfC	OSCIN Rise and Fall Time		12	ns	
3	TwCL, TwCH	OSCIN Low and High Width	25	12	ns	a
			38		ns	b

Notes:
a. Clock divided by 2 internally (MODER.DIV2=1)
b. Clock not divided by 2 internally (MODER.DIV2=0)

CLOCK TIMING



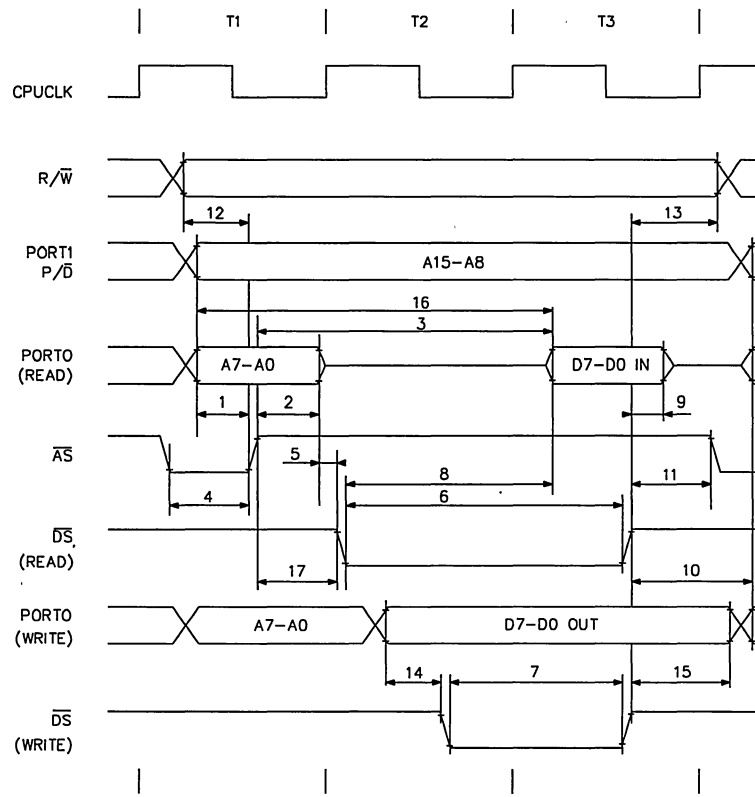
EXTERNAL BUS TIMING TABLE (V_{DD} = 5V ± 10%, T_A = – 40 °C to + 85 °C, Cload = 50pF, CPUCLK = 12MHz, unless otherwise specified)

N°	Symbol	Parameter	Value (Note)				Unit
			OSCIN Divided By 2	OSCIN Not Divided By 2	Min.	Max.	
1	TsA (AS)	Address Set-up Time before $\overline{AS}$ ↑	TpC (2P+1) –22	TwCH+PTpC –18	20		ns
2	ThAS (A)	Address Hold Time after $\overline{AS}$ ↑	TpC –17	TwCL –13	25		ns
3	TdAS (DR)	$\overline{AS}$ ↑ to Data Available (read)	TpC (4P+2W+4) –52	TpC (2P+W+2) –51		115	ns
4	TwAS	$\overline{AS}$ Low Pulse Width	TpC (2P+1) –7	TwCH+PTpC –3	35		ns
5	TdAz (DS)	Address Float to $\overline{DS}$ ↓	0	0	0		ns
6	TwDSR	$\overline{DS}$ Low Pulse Width (read)	TpC (4P+2W+3) –20	TwCH+TpC (2P+W+1) – 16	105		ns
7	TwDSW	$\overline{DS}$ Low Pulse Width (write)	TpC (2P+2W+2) –13	TpC (P+W+1) –13	70		ns
8	TdDSR (DR)	$\overline{DS}$ ↓ to Data Valid Delay (read)	TpC (4P+2W-3) –50	TwCH+TpC(2P+W+1) – 46		75	ns
9	ThDR (DS)	Data to $\overline{DS}$ ↑ Hold Time (read)	0	0	0		ns
10	TdDS (A)	$\overline{DS}$ ↑ to Address Active Delay	TpC –7	TwCL –3	35		ns
11	TdDS (AS)	$\overline{DS}$ ↑ to $\overline{AS}$ ↓ Delay	TpC –18	TwCL –14	24		ns
12	TsR/W (AS)	R/$\overline{W}$ Set-up Time before $\overline{AS}$ ↑	TpC (2P+1) –22	TwCH+PTpC –18	20		ns
13	TdDSR (R/W)	$\overline{DS}$ ↑ to R/$\overline{W}$ and Address Not Valid Delay	TpC –9	TwCL –5	33		ns
14	TdDW (DSW)	Write Data Valid to $\overline{DS}$ ↓ Delay (write)	TpC (2P+1) –32	TwCH+PTpC –28	10		ns
15	ThDS (DW)	Data Hold Time after DS ↑ (write)	TpC –9	TwCL –5	33		ns
16	TdA (DR)	Address Valid to Data Valid Delay (read)	TpC (6P+2W+5) –68	TwCH+TpC (3P+W+2) – 64		140	ns
17	TdAs (DS)	$\overline{AS}$ ↑ to $\overline{DS}$ ↓ Delay	TpC –18	TwCL –14	24		ns

Note: The value left hand two columns show the formula used to calculate the timing minimum or maximum from the oscillator clock period, prescale value and number of wait cycles inserted.
The value right hand two columns show the timing minimum and maximum for an external clock at 24 MHz divided by 2, prescaler value of zero and zero wait status.

Legend:
P = Clock Prescaling Value
W = Wait Cycles
TpC = OSCIN Period
TwCH = High Level OSCIN half period
TwCL = Low Level OSCIN half period

EXTERNAL BUS TIMING

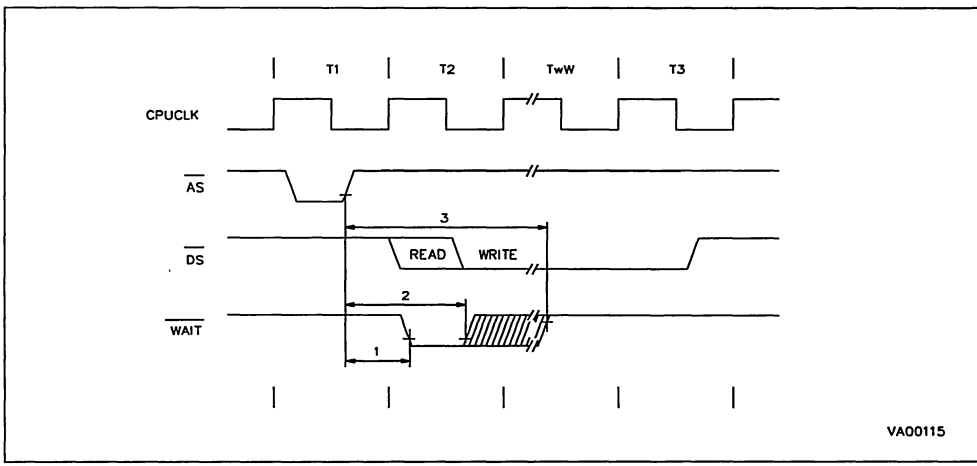


EXTERNAL WAIT TIMING TABLE (V_{DD} = 5V ± 10%, T_A = –40°C to +85°C, Cload = 50pF, INTCLK = 12MHz, Push-pull output configuration, unless otherwise specified)

N°	Symbol	Parameter	Value (Note)				Unit
			OSCIN Divided By 2	OSCIN Not Divided By 2	Min.	Max.	
1	TdAS (WAIT)	$\overline{AS}$ ↑ to $\overline{WAIT}$ ↓ Delay	2(P+1)TpC –29	(P+1)TpC –29		40	ns
2	TdAS (WAIT)	$\overline{AS}$ ↑ to $\overline{WAIT}$ ↑ Minimum Delay	2(P+W+1)TpC –4	(P+W+1)TpC –4	80		ns
3	TdAS (WAIT)	$\overline{AS}$ ↑ to $\overline{WAIT}$ ↑ Maximum Delay	2(P+W+1)TpC –29	(P+W+1)TpC –29		83W+40	ns

Note: The value left hand two columns show the formula used to calculate the timing minimum or maximum from the oscillator clock period, prescale value and number of wait cycles inserted.
The value right hand two columns show the timing minimum and maximum for an external clock at 24 MHz divided by 2, prescale value of zero and zero wait status.

EXTERNAL WAIT TIMING

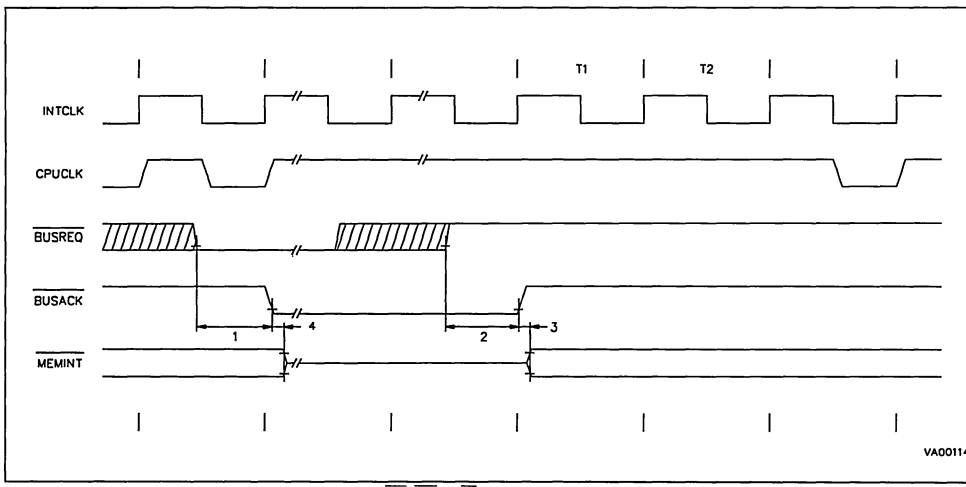


BUS REQUEST/ACKNOWLEDGE TIMING TABLE (V_{DD} = 5V ± 10%, T_A = −40°C to +85°C, Cload = 50pF, INTCLK = 12MHz, Push-pull output configuration, unless otherwise specified)

N°	Symbol	Parameter	Value (Note)				Unit
			OSCIN Divided By 2	OSCIN Not Divided By 2	Min.	Max.	
1	TdBR (BACK)	$\overline{BREQ}$ ↓ to $\overline{BUSACK}$ ↓	TpC+8	TwCL+12	50		ns
			TpC(6P+2W+7)+65	TpC(3P+W+3)+TwCL+65		360	ns
2	TdBR (BACK)	$\overline{BREQ}$ ↑ to $\overline{BUSACK}$ ↑	3TpC+60	TpC+TwCL+60		185	ns
3	TdBACK (BREL)	$\overline{BUSACK}$ ↓ to Bus Release	20	20		20	ns
4	TdBACK (BACT)	$\overline{BUSACK}$ ↑ to Bus Active	20	20		20	ns

Note: The value left hand two columns show the formula used to calculate the timing minimum or maximum from the oscillator clock period, prescale value and number of wait cycles inserted.
The value right hand two columns show the timing minimum and maximum for an external clock at 24 MHz divided by 2, prescale value of zero and zero wait status.

BUS REQUEST/ACKNOWLEDGE TIMING



Note : MEMINT = group of memory interface signals : $\overline{AS}$, $\overline{DS}$, R/$\overline{W}$, P00-P07, P10-P17.

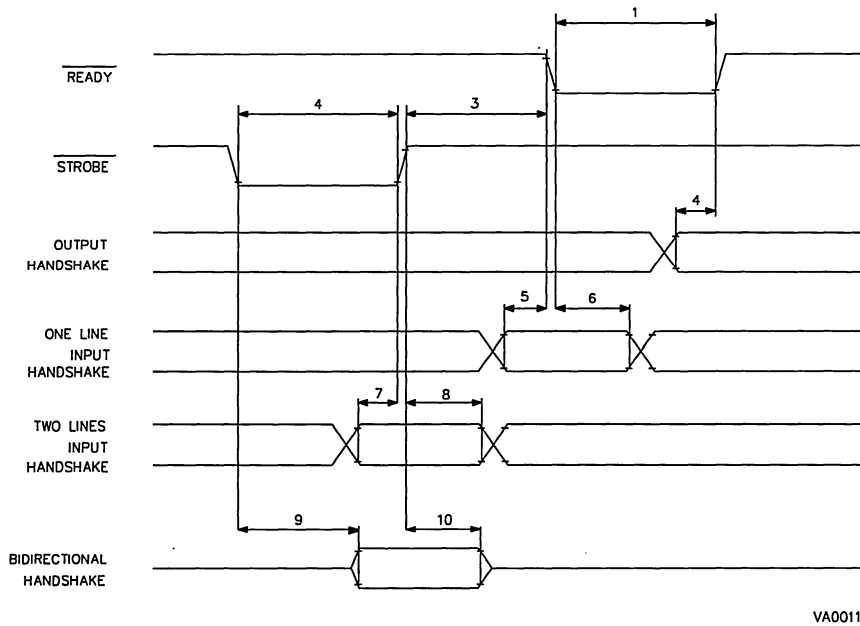
HANDSHAKE TIMING TABLE (V_{DD} = 5V ± 10%, T_A = –40°C to +85°C, Cload = 50pF, INTCLK = 12MHz, Push-pull output configuration, unless otherwise specified)

N°	Symbol	Parameter	Value (Note)				Min.	Max.	Unit
			OSCIN Divided By 2		OSCIN Not Divided By 2				
			Min.	Max.	Min.	Max.			
1	TwRDY	RDRDY, WRRDY Pulse Width in One Line Handshake	2TpC (P+W+1) –18		TpC (P+W+1) –18		65		ns
2	TwSTB	$\overline{RDSTB}$, $\overline{WRSTB}$ Pulse Width	2TpC+12		TpC+12		95		ns
3	TdST (RDY)	$\overline{RDSTB}$, or $\overline{WRSTB}$ ↑ to RDRDY or WRRDY ↓		TpC+45		(TpC-TwCL) +45		87	ns
4	TsPD (RDY)	Port Data to RDRDY ↑ Set-up Time	(2P+2W+1) TpC –25		TwCH+(W+P) TpC –25		16		ns
5	TsPD (RDY)	Port Data to WRRDY ↓ Set-up Time in One Line Handshake	43		43		43		ns
6	ThPD (RDY)	Port Data to WRRDY ↓ Hold Time in One Line Handshake	0		0		0		ns
7	TsPD (STB)	Port Data to $\overline{WRSTB}$ ↑ Set-up Time	10		10		10		ns
8	ThPD (STB)	Port Data to WRSTB ↑ Hold Time	25		25		25		ns
9	TdSTB (PD)	$\overline{RDSTBD}$ ↑ to Port Data Delay Time in Bidirectional Hand-shake		35		35		35	ns
10	TdSTB (PHZ)	$\overline{RDSTB}$ ↑ to Port High-Z Delay Time in Bidirectional Hand-shake		25		25		25	ns

Note: The value left hand two columns show the formula used to calculate the timing minimum or maximum from the oscillator clock period, prescale value and number of wait cycles inserted.
The value right hand two columns show the timing minimum and maximum for an external clock at 24 MHz divided by 2, prescaler value of zero and zero wait status.

Legend:
P = Clock Prescaling Value (R235.4,3,2)
W = Programmable Wait Cycles (R252.2.1.0/5,4,3) + External Wait Cycles

HANDSHAKE TIMING

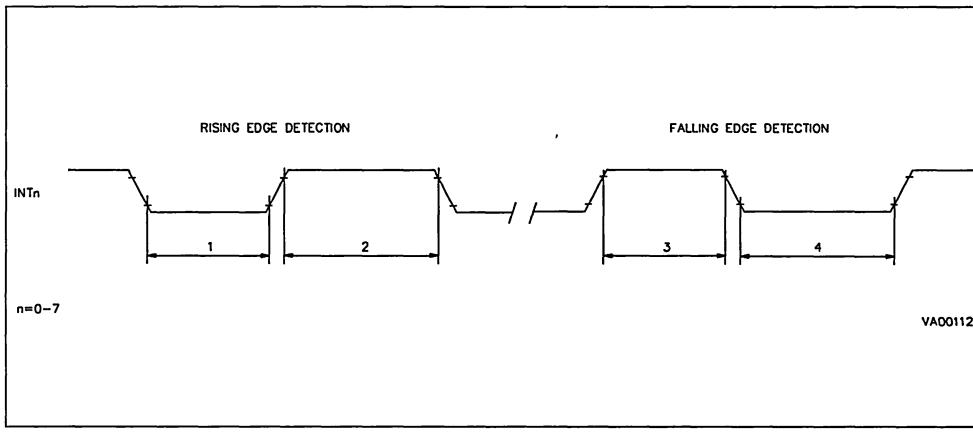


EXTERNAL INTERRUPT TIMING TABLE (V_{DD} = 5V ± 10%, T_A = –40°C to +85°C, Cload = 50pF, INTCLK = 12MHz, Push-pull output configuration, unless otherwise specified)

N°	Symbol	Parameter	Value (Note)				Unit
			OSCIN Divided By 2 Min.	OSCIN Not Divided By 2 Min.	Min.	Max.	
1	TwLR	Low Level Minimum Pulse Width in Rising Edge Mode	2TpC+12	TpC+12	95		ns
2	TwHR	High Level Minimum Pulse Width in Rising Edge Mode	2TpC+12	TpC+12	95		ns
3	TwHF	High Level Minimum Pulse Width in Falling Edge Mode	2TpC+12	TpC+12	95		ns
4	TwLF	Low Level Minimum Pulse Width in Falling Edge Mode	2TpC+12	TpC+12	95		ns

Note: The value left hand two columns show the formula used to calculate the timing minimum or maximum from the oscillator clock period, prescale value and number of wait cycles inserted.
The value right hand two columns show the timing minimum and maximum for an external clock at 24 MHz divided by 2, prescale value of zero and zero wait status.

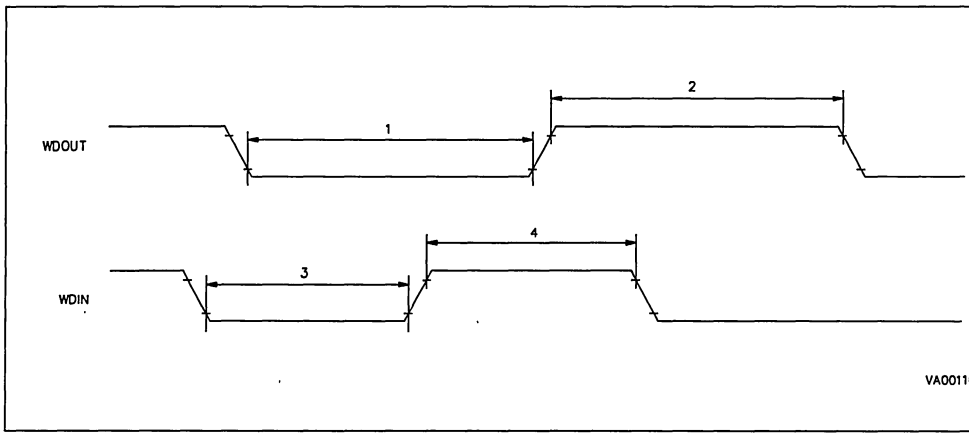
EXTERNAL INTERRUPT TIMING



WATCHDOG TIMING TABLE (V_{DD} = 5V ± 10%, T_A = −40°C to +85°C, Cload = 50pF, INTCLK = 12MHz, Output Alternate Function set as Push-pull)

N°	Symbol	Parameter	Value		Unit
			Min.	Max.	
1	TwWDOL	WDOUT Low Pulse Width	620		ns
2	TwWDOH	WDOUT High Pulse Width	620		ns
3	TwWDIL	WDIN Low Pulse Width	350		ns
4	TwWDIH	WDIN High Pulse Width	350		ns

WATCHDOG TIMING

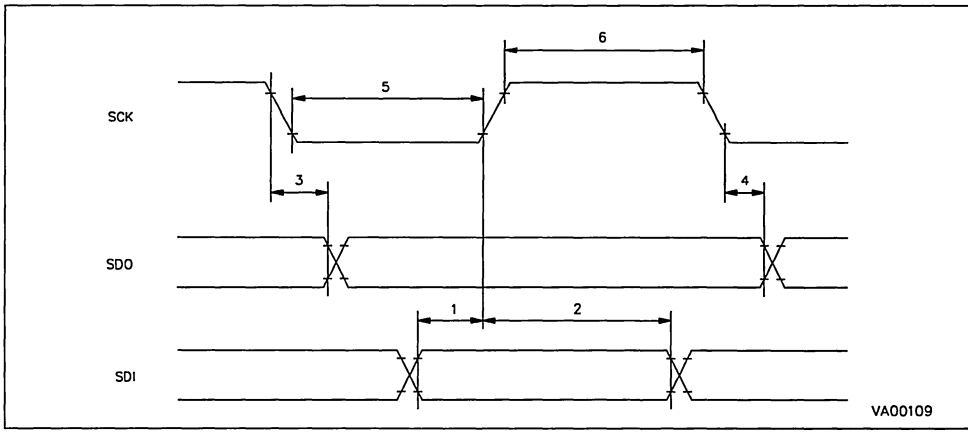


SPI TIMING TABLE (V_{DD} = 5V ± 10%, T_A = –40°C to +85°C, Cload = 50pF, INTCLK = 12MHz, Output Alternate Function set as Push-pull)

N°	Symbol	Parameter	Value		Unit
			Min.	Max.	
1	TsDI	Input Data Set-up Time	100		ns
2	ThDI (1)	Input Data Hold Time	1/2 TpC+100		ns
3	TdOV	SCK to Output Data Valid		100	ns
4	ThDO	Output Data Hold Time	-20		ns
5	TwSKL	SCK Low Pulse Width	300		ns
6	TwSKH	SCK High Pulse Width	300		ns

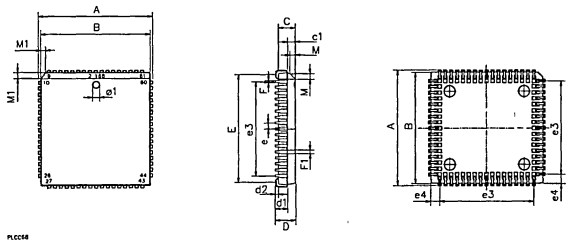
Note: 1. TpC is the Clock period.

SPI TIMING



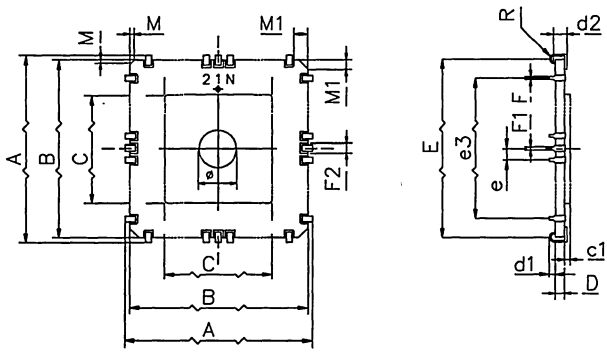
PACKAGES MECHANICAL DATA

Figure 5. 68-Lead Plastic Leaded Chip Carrier (C)



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A	25.02		25.27	0.985		0.995
B	24.13		24.33	0.950		0.958
D	4.20		5.08	0.165		0.200
d1		2.54			0.100	
d2		0.56			0.022	
E	22.61		23.62	0.890		0.930
e		1.27			0.050	
F		0.38			0.015	
G			0.10			0.004
M		1.27			0.050	
M1		1.14			0.044	
Ø1		7.36			0.289	

Figure 6. 68-Lead Window Ceramic Leaded Chip Carrier (L)



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A		25.14			0.989	
B	23.87		24.51	0.939		0.964
C			15.45			0.608
C1			1.30			0.051
D	1.82		2.23	0.071		0.087
d1	–	–	–	–	–	–
d2	–	–	–	–	–	–
E	–	–	–	–	–	–
e		1.27			0.050	
e3	–	–	–	–	–	–
F		0.45			0.017	
F1		0.63			0.025	
F2	–	–	–	–	–	–
M	–	–	–	–	–	–
M1	–	–	–	–	–	–
R		0.76			0.030	
Ø		8.89			0.350	

ORDERING INFORMATION

Sales Type	Frequency	Temperature Range	Package
ST90E40L6	24MHz	– 40°C to + 85°C	CLCC68-W
ST90E40L1	24MHz	0°C to + 85°C	CLCC68-W
ST90T40C6	24MHz	– 40°C to + 85°C	PLCC68
ST90T40C1	24MHz	0°C to + 70°C	PLCC68

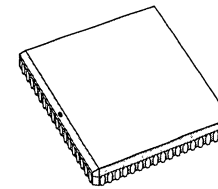
SGS-THOMSON MICROELECTRONICS

ST90R40

ROMLESS HCMOS MCU WITH EEPROM, RAM AND A/D

ADVANCE DATA

- Single chip microcontroller with 256 bytes of RAM and 256 bytes of Register File with 224 general purpose registers available as RAM, accumulators or index pointers.
- Romless to allow maximum external memory flexibility in development and production phases.
- 512 bytes of high-reliability EEPROM on-chip, with 300,000 erase/write cycle capability and 10 year data retention.
- 8/16 bit CORE with full feature DMA controller, a powerful interrupt handler and a Standard Serial Peripheral Interface (SPI) handling S-BUS, I^2C-bus, IM-bus and Standard Serial Peripheral Interfaces.
- Up to 8 external interrupts edge-selectable plus 1 non-maskable interrupt.
- 16 bit programmable Timer with 8 bit Prescaler, able to be used as a Watchdog Timer for system integrity.
- Two 16 bit Multifunction Timer modules, each with an 8 bit prescaler and 13 operating modes, allowing simple use for complex waveform generation and measurement, PWM functions and many other system timing operations.
- 8 channel Analog to Digital Converter, with integral sample and hold, fast 11µs conversion time, 8 bit ±1/2 LSB resolution with Analog Watchdog on two channels.
- Full function Serial Communications Interface with 110 to 375000 baud rate generator, asynchronous and byte synchronous capability (fully programmable format) and address/wake-up bit option.
- On-chip DMA channels associated to the Multifunction Timers and the Serial Communications Interface.
- Up to six 8 bit I/O ports with programmable input thresholds and output characteristics. Alternative functions allow the full use of all pins.
- Powerful software development tools, including assembler, linker, C-compiler, archiver, software and hardware emulators.
- Compatible with ST9040, 16k ROM devices (also available in windowed and One Time Programmable EPROM packages).
- 68-lead Plastic Leaded Chip Carrier package for ST90R40.



PLCC68

(Ordering Information at the end of the datasheet)

Figure 1. ST90R40 Block Diagram

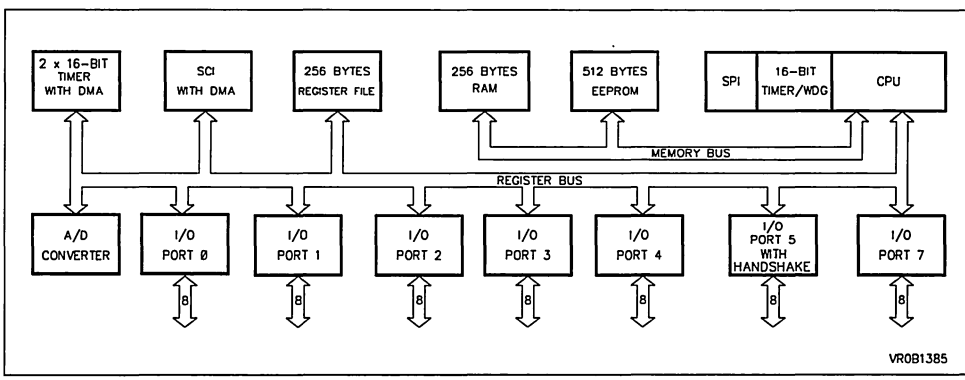
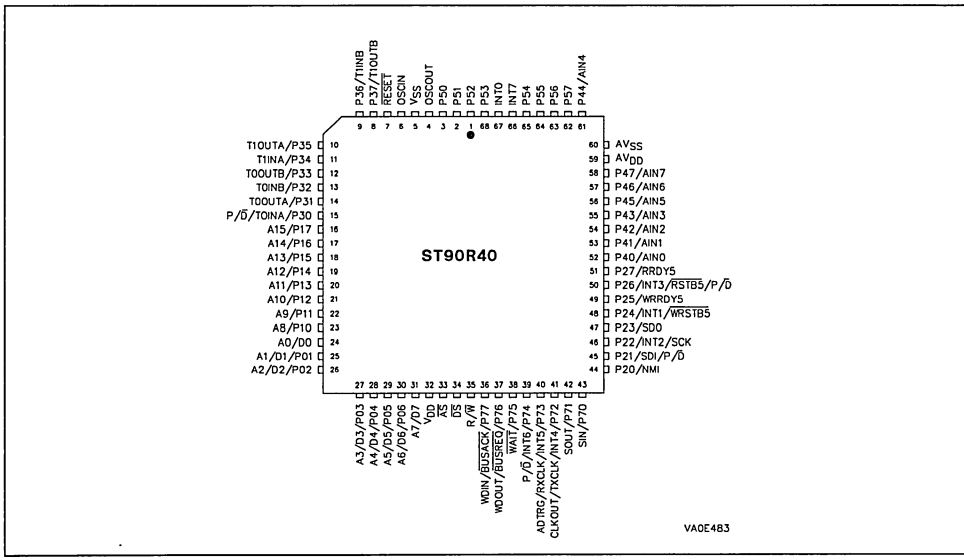


Figure 2. ST90R40 Pin Configuration



GENERAL DESCRIPTION

The ST90R40 is a ROMLESS member of the ST9 family of microcontrollers, completely developed and produced by SGS-THOMSON Microelectronics using a proprietary n-well HCMOS process.

The ROMLESS part may be used for the prototyping and pre-production phases of development, and offers the maximum in program flexibility in production systems.

The ST90R40 is fully compatible with the ST9040 ROM version and this datasheet will thus provide only information specific to the ROMLESS device.

THE READER IS ASKED TO REFER TO THE DATASHEET OF THE ST9040 ROM-BASED DEVICE, OR ST90R50 FOR FURTHER DETAILS.

The ROMLESS ST90R40 can be configured as a microcontroller able to manage up to 128K bytes of external memory, or as a parallel processing element in a system with other processors and peripheral controllers.

A key point of the ST90R40 architecture is related to its modular approach which allows software commonality with all other members of the ST9 family.

The nucleus of the modular design of the ST90R40 is the advanced Core which includes the Central Processing Unit (CPU), the Register File, a 16 bit Timer/Watchdog with 8 bit Prescaler, a Serial Peripheral Interface supporting S-BUS, I^2C-bus and IM-bus Interface, plus two 8 bit I/O ports. The Core has independent memory and register buses allowing a high degree of pipelining to add to the efficiency of the code execution speed of the extensive instruction set.

The powerful I/O capabilities demanded by microcontroller applications are fulfilled by the ST90R40 with up to 48 I/O lines dedicated to digital Input/Output. These lines are grouped into up to six 8 bit I/O Ports and can be configured on a bit basis under software control to provide timing and status signals, address lines, timer inputs and outputs, analog inputs, external interrupts and serial or parallel I/O with or without handshake.

Three memory spaces are available: Program Memory (external), Data Memory (internal and external) and the Register File, which includes the control and status registers of the on-chip peripherals.

Two 16 bit MultiFunction Timers, each with an 8 bit Prescaler and 13 operating modes allow simple use for complex waveform generation and measurement, PWM functions and many other system timing functions by the usage of the two associated DMA channels for each timer.

GENERAL DESCRIPTION (Continued)

In addition there is an 8 channel Analog to Digital Converter with integral sample and hold, fast 11µs conversion time and 8 bit ±1/2 LSB resolution. An Analog Watchdog feature is included for two input channels.

Completing the device is a full duplex Serial Communications Interface with an integral 110 to 375000 baud rate generator, asynchronous and byte synchronous capability (fully programmable format) and associated address/wake-up option, plus two DMA channels.

PIN DESCRIPTION

$\overline{AS}$. *Address Strobe (output, active low, 3-state).* Address Strobe is pulsed low once at the beginning of each memory cycle. The rising edge of $\overline{AS}$ indicates that address, Read/Write (R/$\overline{W}$), and Data Memory signals are valid for program or data memory transfers. Under program control, $\overline{AS}$ can be placed in a high-impedance state along with Port 0 and Port 1, Data Strobe ($\overline{DS}$) and R/$\overline{W}$.

$\overline{DS}$. *Data Strobe (output, active low, 3-state).* Data Strobe provides the timing for data movement to or from Port 0 for each memory transfer. During a write cycle, data out is valid at the leading edge of $\overline{DS}$. During a read cycle, Data In must be valid prior to the trailing edge of $\overline{DS}$. When the ST90R40 accesses on-chip Data memory, $\overline{DS}$ is held high during the whole memory cycle. It can be placed in a high impedance state along with Port 0, Port 1, $\overline{AS}$ and R/$\overline{W}$.

R/$\overline{W}$. *Read/Write (output, 3-state).* Read/Write determines the direction of data transfer for memory transactions. R/$\overline{W}$ is low when writing to program or data memory, and high for all other transactions. It can be placed in a high impedance state along with Port 0, Port 1, $\overline{AS}$ and $\overline{DS}$.

$\overline{RESET}$. *Reset (input, active low).* The ST9 is initialised by the Reset signal. With the deactivation of $\overline{RESET}$, program execution begins from the Program memory location pointed to by the vector contained in program memory locations 00h and 01h.

OSCIN, OSCOUT. *Oscillator (input and output).* These pins connect a parallel-resonant crystal (24MHz maximum), or an external source to the on-chip clock oscillator and buffer. OSCIN is the input of the oscillator inverter and internal clock generator; OSCOUT is the output of the oscillator inverter.

AV_{DD}. Analog V_{DD} of the Analog to Digital Converter.

AV_{SS}. Analog V_{SS} of the Analog to Digital Converter.

V_{DD}. Main Power Supply Voltage (5V±10%)

V_{SS}. Digital Circuit Ground.

AD0-AD7, (P0.0-P0.7) *Address/Data Lines (Input/Output, TTL or CMOS compatible).* 8 lines providing a multiplexed address and data bus, under control of the $\overline{AS}$ and $\overline{DS}$ timing signals.

P1.0-P1.7, P2.0-P2.7 P3.0-P3.7, P4.0-P4.7, P5.0-P5.7, P7.0-P7.7 *I/O Port Lines (Input/Output, TTL or CMOS compatible).* 48 lines grouped into I/O ports of 8 bits, bit programmable under program control as general purpose I/O or as Alternate functions (see next section).

I/O Port Alternate Functions.

Each pin of the I/O ports of the ST90R40 may assume software programmable Alternative Functions as shown in the Pin Configuration Drawings. Figure 1.2 shows the Functions allocated to each I/O Port pins.

PIN DESCRIPTION (Continued)

Table 1. ST90R40 I/O Port Alternate Function Summary

I/O PORT Port.bit	Name	Function IN/OUT	Alternate Function	Pin Number
P0.0	A0/D0	I/O	Address/Data bit 0 mux	24
P0.1	A1/D1	I/O	Address/Data bit 1 mux	25
P0.2	A2/D2	I/O	Address/Data bit 2 mux	26
P0.3	A3/D3	I/O	Address/Data bit 3 mux	27
P0.4	A4/D4	I/O	Address/Data bit 4 mux	28
P0.5	A5/D5	I/O	Address/Data bit 5 mux	29
P0.6	A6/D6	I/O	Address/Data bit 6 mux	30
P0.7	A7/D7	I/O	Address/Data bit 7 mux	31
P1.0	A8	O	Address bit 8	23
P1.1	A9	O	Address bit 9	22
P1.2	A10	O	Address bit 10	21
P1.3	A11	O	Address bit 11	20
P1.4	A12	O	Address bit 12	19
P1.5	A13	O	Address bit 13	18
P1.6	A14	O	Address bit 14	17
P1.7	A15	O	Address bit 15	16
P2.0	NMI	I	Non-Maskable Interrupt	44
P2.1	P/$\overline{D}$	O	Program/Data Space Select	45
P2.1	SDI	I	SPI Serial Data Out	45
P2.2	INT2	I	External Interrupt 2	46
P2.2	SCK	O	SPI Serial Clock	46
P2.3	SDO	O	SPI Serial Data In	47
P2.4	INT1	I	External Interrupt 1	48
P2.4	$\overline{WRSTB5}$	O	Handshake Write Strobe P5	48
P2.5	WRRDY5	I	Handshake Write Ready P5	49
P2.6	INT3	I	External Interrupt 3	50
P2.6	$\overline{RDSTB5}$	I	Handshake Read Strobe P5	50
P2.6	P/$\overline{D}$	O	Program/Data Space Select	50
P2.7	RDRDY5	O	Handshake Read Ready P5	51

PIN DESCRIPTION (Continued)

Table 1. ST90R40 I/O Port Alternate Function Summary (Continued)

I/O PORT Port.bit	Name	Function IN/OUT	Alternate Function	Pin Number
P3.0	T0INA	I	MF Timer 0 Input A	15
P3.0	P/$\overline{D}$	O	Program/Data Space Select	15
P3.1	T0OUTA	O	MF Timer 0 Output A	14
P3.2	T0INB	I	MF Timer 0 Input B	13
P3.3	T0OUTB	O	MF Timer 0 Output B	12
P3.4	T1INA	I	MF Timer 1 Input A	11
P3.5	T1OUTA	O	MF Timer 1 Output A	10
P3.6	T1INB	I	MF Timer 1 Input B	9
P3.7	T1OUTB	O	MF Timer 1 Output B	8
P4.0	AIN0	I	A/D Analog Input 0	52
P4.1	AIN1	I	A/D Analog Input 1	53
P4.2	AIN2	I	A/D Analog Input 2	54
P4.3	AIN3	I	A/D Analog Input 3	55
P4.4	AIN4	I	A/D Analog Input 4	61
P4.5	AIN5	I	A/D Analog Input 5	56
P4.6	AIN6	I	A/D Analog Input 6	57
P4.7	AIN7	I	A/D Analog Input 7	58
P5.0		I/O	I/O Handshake Port 5	3
P5.1		I/O	I/O Handshake Port 5	2
P5.2		I/O	I/O Handshake Port 5	1
P5.3		I/O	I/O Handshake Port 5	68
P5.4		I/O	I/O Handshake Port 5	65
P5.5		I/O	I/O Handshake Port 5	64
P5.6		I/O	I/O Handshake Port 5	63
P5.7		I/O	I/O Handshake Port 5	62
P7.0	SIN	I	SCI Serial Input	43
P7.1	SOUT	O	SCI Serial Output	42
P7.2	INT4	I	External Interrupt 4	41
P7.2	TXCLK	I	SCI Transmit Clock Input	41

PIN DESCRIPTION (Continued)

Table 1. ST90R40 I/O Port Alternate Function Summary (Continued)

I/O PORT Port.bit	Name	Function IN/OUT	Alternate Function	Pin Number
P7.2	CLKOUT	O	SCI Byte Sync Clock Output	41
P7.3	INT5	I	External Interrupt 5	40
P7.3	RXCLK	I	SCI Receive Clock Input	40
P7.3	ADTRG	I	A/D Conversion Trigger	40
P7.4	INT6	I	External Interrupt 6	39
P7.4	P/$\overline{D}$	O	Program/Data Space Select	39
P7.5	$\overline{WAIT}$	I	External Wait Input	38
P7.6	WDOUT	O	T/WD Output	37
P7.6	$\overline{BUSREQ}$	I	External Bus Request	37
P7.7	WDIN	I	T/WD Input	36
P7.7	$\overline{BUSACK}$	O	External Bus Acknowledge	36

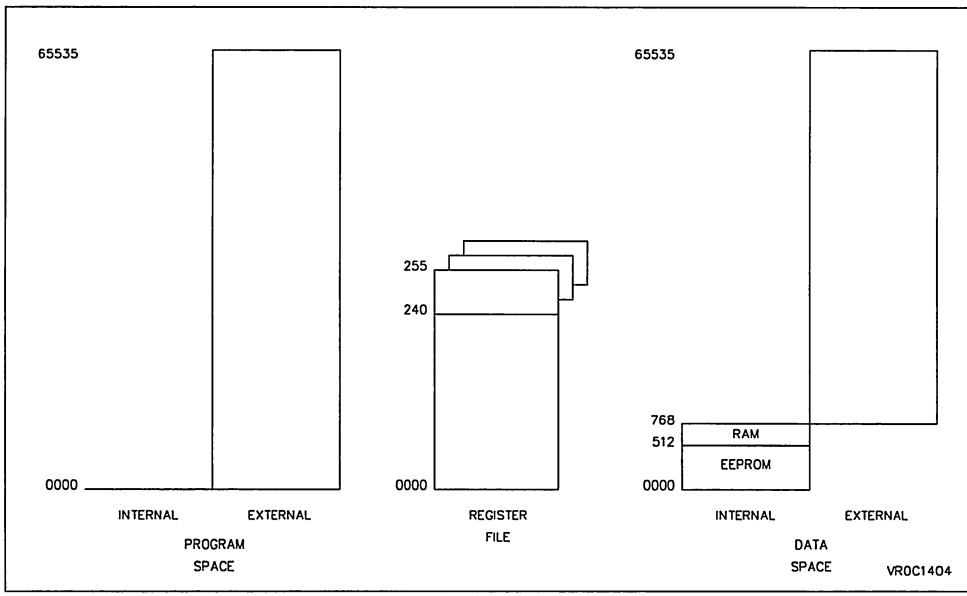
MEMORY

The memory of the ST90R40 is functionally divided into two areas, the Register File and Memory. The Memory may optionally be divided into two spaces, each having a maximum of 65,536 bytes. The two memory spaces are separated by function, one space for Program code, the other for Data. The ST90R40 addresses all program memory in the external PROGRAM space. The DATA space includes the 512 bytes of on-chip EEPROM at addresses 0 through 1FFh and the 256 bytes of on-chip RAM memory at memory addresses 200h through 2FFh.

The External Memory spaces are addressed using the multiplexed address and data buses on Ports 0 and 1. Additional Data Memory may be decoded externally by using the P/$\overline{D}$ Alternate Function output. The on-chip general purpose (GP) Registers may be used as RAM memory.

MEMORY (Continued)

Figure 3. Memory Spaces



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	– 0.3 to 7.0	V
AV_{DD}, AV_{SS}	Analog Supply Voltage	$V_{SS} \leq AV_{SS} < AV_{DD} \leq V_{DD}$	V
V_I	Input Voltage	V_{SS} – 0.3 to V_{DD} +0.3	V
V_O	Output Voltage	V_{SS} – 0.3 to V_{DD} +0.3	V
T_{STG}	Storage Temperature	– 55 to + 150	°C

Note: Stresses above those listed as "absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value		Unit
		Min.	Max.	
T_A	Operating Temperature	– 40	85	°C
V_{DD}	Operating Supply Voltage	4.5	5.5	V
f_{OSCE}	External Oscillator Frequency		24	MHz
f_{OSCI}	Internal Oscillator Frequency		12	MHz

DC ELECTRICAL CHARACTERISTICS

(V_{DD} = 5V ± 10% T_A = – 40 °C to + 85°C, unless otherwise specified)

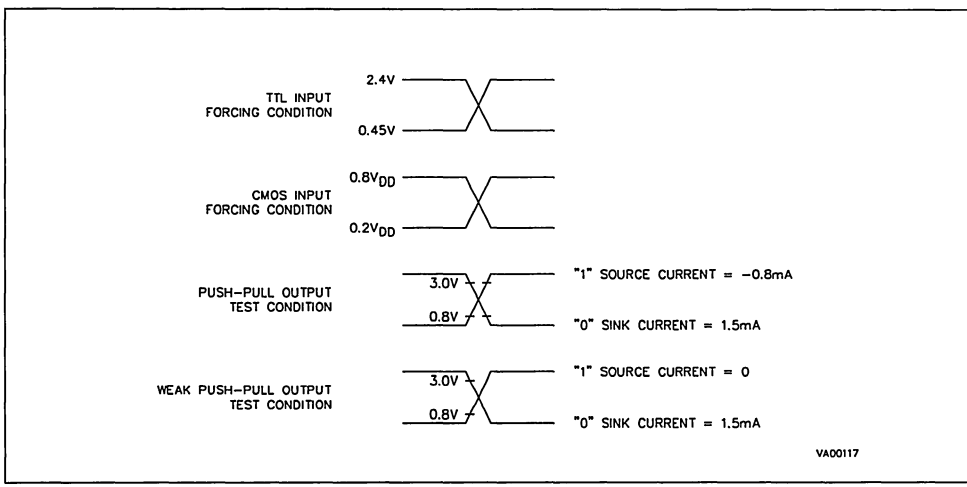
Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
V_{IHCK}	Clock Input High Level	External Clock	0.7 V_{DD}		V_{DD} + 0.3	V
V_{ILCK}	Clock Input Low Level	External Clock	– 0.3		0.3 V_{DD}	V
V_{IH}	Input High Level	TTL	2.0		V_{DD} + 0.3	V
		CMOS	0.7 V_{DD}		VDD + 0.3	V
V_{IL}	Input Low Level	TTL	– 0.3		0.8	V
		CMOS	– 0.3		0.3 V_{DD}	V
V_{IHRS}	Reset Input High Level		0.7 V_{DD}		V_{DD} + 0.3	V
V_{ILRS}	Reset Input Low Level		–0.3		0.3 V_{DD}	V
V_{HYRS}	Reset Input Hysteresis		0.3		1.5	V
V_{OH}	Output High Level	Push Pull, Iload = – 0.8mA	V_{DD} – 0.8			V
V_{OL}	Output Low Level	Push Pull or Open Drain, Iload = – 1.6mA			0.4	V

DC ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
I_{WPU}	Weak Pull-up Current	Bidirectional Weak Pull-up, V_{OL} = 0V	– 80	– 200	– 420	µA
I_{APU}	Active Pull-up Current, for INT0 and INT7 only	V_{IN} < 0.8V	– 80	– 200	– 420	µA
I_{LKIO}	I/O Pin Input Leakage	Input/Tri-State, 0V < V_{IN} < V_{DD}	– 10		+ 10	µA
I_{LKRS}	Reset Pin Input Leakage	0V < V_{IN} < V_{DD}	– 30		+ 30	µA
I_{LKAD}	A/D Pin Input Leakage	Alternate Function, Open Drain, 0V < V_{IN} < V_{DD}	– 3		+ 3	µA
I_{LKAP}	Active Pull-up Input Leakage	0V < V_{IN} < 0.8V	– 10		+ 10	µA
I_{LKOS}	OSCIN Pin Input Leakage	0V < V_{IN} < V_{DD}	– 10		+ 10	µA
I_{DD}	Run Mode Current	24MHz, Note 1		32	70	mA
		4MHz, Note 1		6	12	mA
I_{DP2}	Run Mode Current Prescale by 2	24MHz, Note 1		19	40	mA
		4MHz, Note 1		4	8	mA
I_{WFI}	WFI Mode Current	24MHz, Note 1		9	18	mA
		4MHz, Note 1		2.5	5	mA
I_{HALT}	HALT Mode Current	24MHz, Note 1			100	µA

Note:
1. All I/O Ports are configured in Bidirectional Weak Pull-up Mode with no DC load, External Clock pin (OSCIN) is driven by square wave external clock. No peripheral working. External interface not active (Internal Program Execution).

DC TEST CONDITIONS



AC ELECTRICAL CHARACTERISTICS

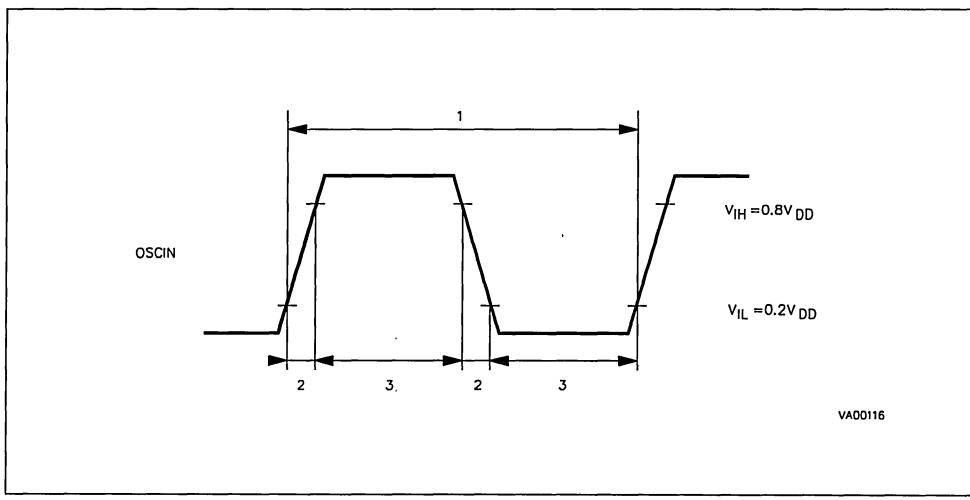
CLOCK TIMING TABLE

(V_{DD} = 5V ± 10%, T_A = − 40°C to + 85°C, unless otherwise specified)

N°	Symbol	Parameter	Value		Unit	Note
			Min.	Max.		
1	TpC	OSCIN Clock Period	41.5		ns	1
			83		ns	2
2	TrC, TfC	OSCIN Rise and Fall Time		12	ns	
3	TwCL, TwCH	OSCIN Low and High Width	25	12	ns	1
			38		ns	2

Notes:
1. Clock divided by 2 internally (MODER.DIV2=1)
2. Clock not divided by 2 internally (MODER.DIV2=0)

CLOCK TIMING



EXTERNAL BUS TIMING TABLE

(V_{DD} = 5V ± 10%, T_A = – 40 °C to + 85 °C, Cload = 50pF, CPUCLK = 12MHz, unless otherwise specified)

N°	Symbol	Parameter	Value (Note)				Unit
			OSCIN Divided By 2	OSCIN Not Divided By 2	Min.	Max.	
1	TsA (AS)	Address Set-up Time before $\overline{AS}$ ↑	TpC (2P+1) –22	TWCH+PTpC –18	20		ns
2	ThAS (A)	Address Hold Time after $\overline{AS}$↑	TpC –17	TwCL –13	25		ns
3	TdAS (DR)	$\overline{AS}$ ↑ to Data Available (read)	TpC (4P+2W+4) –52	TpC (2P+W+2) –51		115	ns
4	TwAS	$\overline{AS}$ Low Pulse Width	TpC (2P+1) –7	TwCH+PTpC –3	35		ns
5	TdAz (DS)	Address Float to $\overline{DS}$ ↓	0	0	0		ns
6	TwDSR	$\overline{DS}$ Low Pulse Width (read)	TpC (4P+2W+3) –20	TwCH+TpC (2P+W+1) –16	105		ns
7	TwDSW	$\overline{DS}$ Low Pulse Width (write)	TpC (2P+2W+2) –13	TpC (P+W+1) –13	70		ns
8	TdDSR (DR)	$\overline{DS}$ ↓ to Data Valid Delay (read)	TpC (4P+2W-3) –50	TwCH+TpC(2P+W+1) – 46		75	ns
9	ThDR (DS)	Data to $\overline{DS}$ ↑ Hold Time (read)	0	0	0		ns
10	TdDS (A)	$\overline{DS}$ ↑ to Address Active Delay	TpC –7	TwCL –3	35		ns
11	TdDS (AS)	$\overline{DS}$ ↑ to $\overline{AS}$ ↓ Delay	TpC –18	TwCL –14	24		ns
12	TsR/W (AS)	R/$\overline{W}$ Set-up Time before $\overline{AS}$↑	TpC (2P+1) –22	TwCH+PTpC –18	20		ns
13	TdDSR (R/W)	$\overline{DS}$ ↑ to R/$\overline{W}$ and Address Not Valid Delay	TpC –9	TwCL –5	33		ns
14	TdDW (DSW)	Write Data Valid to $\overline{DS}$ ↓ Delay (write)	TpC (2P+1) –32	TwCH+PTpC –28	10		ns
15	ThDS (DW)	Data Hold Time after DS ↑ (write)	TpC –9	TwCL –5	33		ns
16	TdA (DR)	Address Valid to Data Valid Delay (read)	TpC (6P+2W+5) –68	TwCH+TpC (3P+W+2) –64		140	ns
17	TdAs (DS)	$\overline{AS}$ ↑ to $\overline{DS}$ ↓ Delay	TpC –18	TwCL –14	24		ns

Note: The value left hand two columns show the formula used to calculate the timing minimum or maximum from the oscillator clock period, prescale value and number of wait cycles inserted.
The value right hand two columns show the timing minimum and maximum for an external clock at 24 MHz divided by 2, prescaler value of zero and zero wait status.

Legend:
P = Clock Prescaling Value
W = Wait Cycles

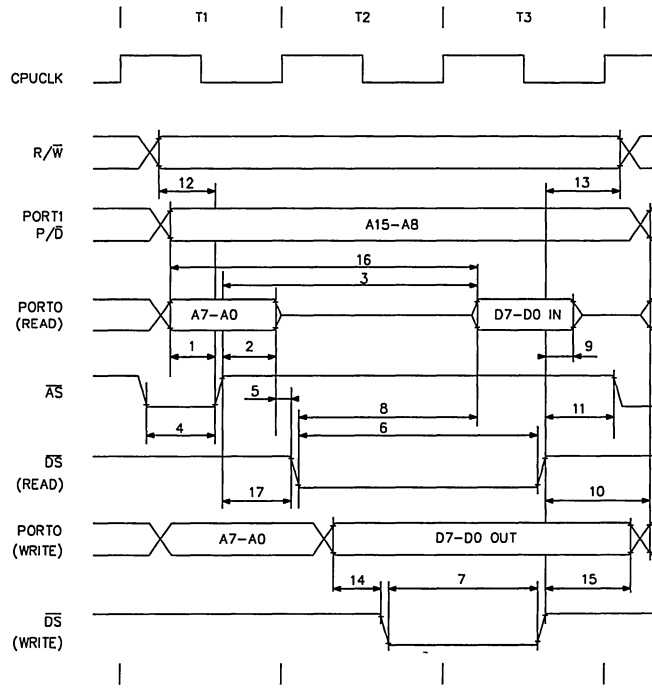
TpC = OSCIN Period
TwCH = High Level OSCIN half period
TwCL = Low Level OSCIN half period

EXTERNAL WAIT TIMING TABLE (V_{DD} = 5V ± 10%, T_A = –40°C to +85°C, Cload = 50pF, INTCLK = 12MHz, Push-pull output configuration, unless otherwise specified)

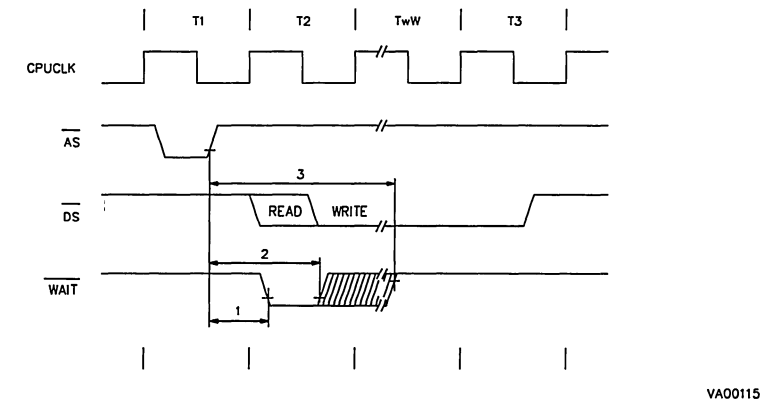
N°	Symbol	Parameter	Value (Note)				Unit
			OSCIN Divided By 2	OSCIN Not Divided By 2	Min.	Max.	
1	TdAS (WAIT)	$\overline{AS}$ ↑ to $\overline{WAIT}$ ↓ Delay	2(P+1)TpC –29	(P+1)TpC –29		40	ns
2	TdAS (WAIT)	$\overline{AS}$ ↑ to $\overline{WAIT}$ ↑ Minimum Delay	2(P+W+1)TpC –4	(P+W+1)TpC –4	80		ns
3	TdAS (WAIT)	$\overline{AS}$ ↑ to $\overline{WAIT}$ ↑ Maximum Delay	2(P+W+1)TpC – 29	(P+W+1)TpC –29		83W+40	ns

Note: The value left hand two columns show the formula used to calculate the timing minimum or maximum from the oscillator clock period, prescale value and number of wait cycles inserted.
The value right hand two columns show the timing minimum and maximum for an external clock at 24 MHz divided by 2, prescale value of zero and zero wait status.

EXTERNAL BUS TIMING



EXTERNAL WAIT TIMING

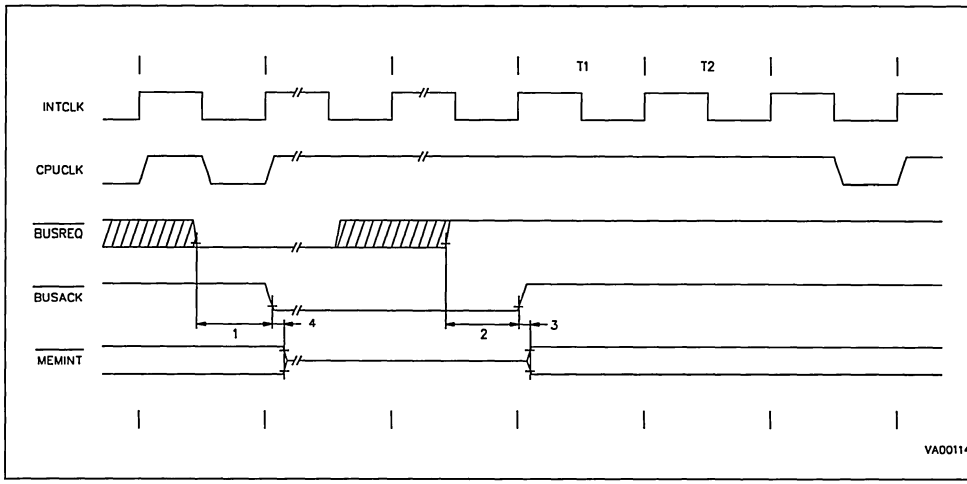


BUS REQUEST/ACKNOWLEDGE TIMING TABLE (V_{DD} = 5V ± 10%, T_A = −40°C to +85°C, Cload = 50pF, INTCLK = 12MHz, Push-pull output configuration, unless otherwise specified)

N°	Symbol	Parameter	Value (Note)				Unit
			OSCIN Divided By 2	OSCIN Not Divided By 2	Min.	Max.	
1	TdBR (BACK)	$\overline{BREQ}$ ↓ to $\overline{BUSACK}$ ↓	TpC+8	TwCL+12	50		ns
			TpC(6P+2W+7)+65	TpC(3P+W+3)+TwCL+65		360	ns
2	TdBR (BACK)	$\overline{BREQ}$ ↑ to $\overline{BUSACK}$ ↑	3TpC+60	TpC+TwCL+60		185	ns
3	TdBACK (BREL)	$\overline{BUSACK}$ ↓ to Bus Release	20	20		20	ns
4	TdBACK (BACT)	$\overline{BUSACK}$ ↑ to Bus Active	20	20		20	ns

Note: The value left hand two columns show the formula used to calculate the timing minimum or maximum from the oscillator clock period, prescale value and number of wait cycles inserted.
The value right hand two columns show the timing minimum and maximum for an external clock at 24 MHz divided by 2, prescale value of zero and zero wait status.

BUS REQUEST/ACKNOWLEDGE TIMING



Note : MEMINT = group of memory interface signals : $\overline{AS}$, $\overline{DS}$, R/$\overline{W}$, P00-P07, P10-P17.

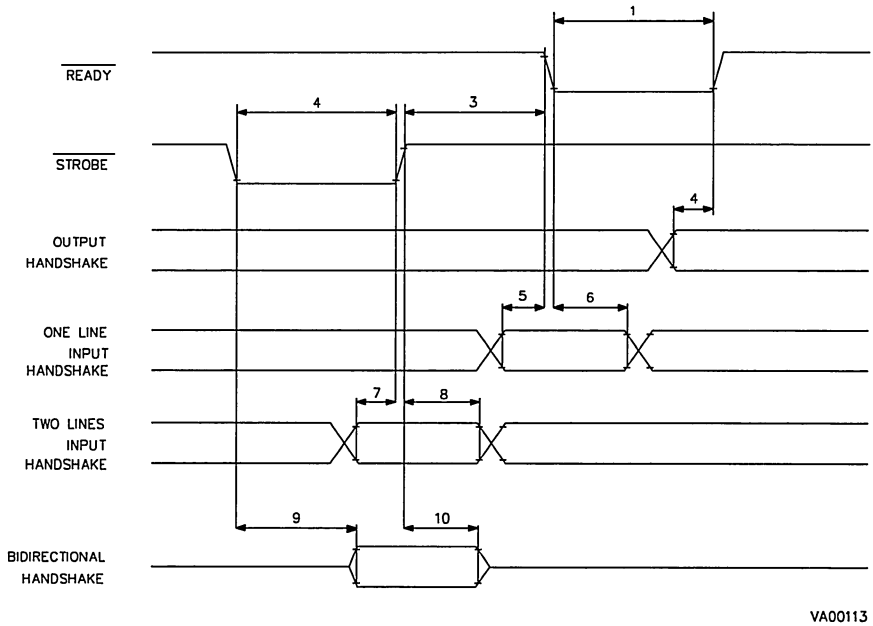
HANDSHAKE TIMING TABLE (V_{DD} = 5V ± 10%, T_A = –40°C to +85°C, Cload = 50pF, INTCLK = 12MHz, Push-pull output configuration, unless otherwise specified)

N°	Symbol	Parameter	Value (Note)				Min.	Max.	Unit
			OSCIN Divided By 2		OSCIN Not Divided By 2				
			Min.	Max.	Min.	Max.			
1	TwRDY	RDRDY, WRRDY Pulse Width in One Line Handshake	2TpC (P+W+1) –18		Tp (P+W+1) – 18		65		ns
2	TwSTB	$\overline{RDSTB}$, $\overline{WRSTB}$ Pulse Width	2TpC+12		TpC+12		95		ns
3	TdST (RDY)	$\overline{RDSTB}$, or $\overline{WRSTB}$ ↑ to RDRDY or WRRDY ↓		TpC+45		(TpC-TwCL) +45		87	ns
4	TsPD (RDY)	Port Data to RDRDY ↑ Set-up Time	(2P+2W+1) TpC –25		TwCH+(W+P) TpC –25		16		ns
5	TsPD (RDY)	Port Data to WRRDY ↓ Set-up Time in One Line Handshake	43		43		43		ns
6	ThPD (RDY)	Port Data to WRRDY ↓ Hold Time in One Line Handshake	0		0		0		ns
7	TsPD (STB)	Port Data to $\overline{WRSTB}$ ↑ Set-up Time	10		10		10		ns
8	ThPD (STB)	Port Data to WRSTB ↑ Hold Time	25		25		25		ns
9	TdSTB (PD)	$\overline{RDSTBD}$ ↑ to Port Data Delay Time in Bidirectional Handshake	-	35		35		35	ns
10	TdSTB (PHZ)	$\overline{RDSTB}$ ↑ to Port High-Z Delay Time in Bidirectional Handshake		25		25		25	ns

Note: The value left hand two columns show the formula used to calculate the timing minimum or maximum from the oscillator clock period, prescale value and number of wait cycles inserted.
The value right hand two columns show the timing minimum and maximum for an external clock at 24 MHz divided by 2, prescaler value of zero and zero wait status.

Legend:
P = Clock Prescaling Value (R235.4,3,2)
W = Programmable Wait Cycles (R252.2.1.0/5,4,3) + External Wait Cycles

HANDSHAKE TIMING

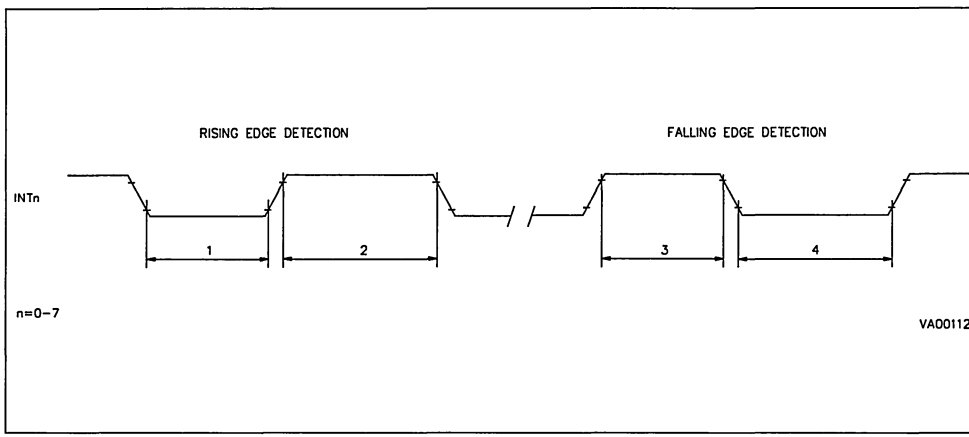


EXTERNAL INTERRUPT TIMING TABLE (V_{DD} = 5V ± 10%, T_A = –40°C to +85°C, Cload = 50pF, INTCLK = 12MHz, Push-pull output configuration, unless otherwise specified)

N°	Symbol	Parameter	Value (Note)				Unit
			OSCIN Divided By 2 Min.	OSCIN Not Divided By 2 Min.	Min.	Max.	
1	TwLR	Low Level Minimum Pulse Width in Rising Edge Mode	2TpC+12	TpC+12	95		ns
2	TwHR	High Level Minimum Pulse Width in Rising Edge Mode	2TpC+12	TpC+12	95		ns
3	TwHF	High Level Minimum Pulse Width in Falling Edge Mode	2TpC+12	TpC+12	95		ns
4	TwLF	Low Level Minimum Pulse Width in Falling Edge Mode	2TpC+12	TpC+12	95		ns

Note: The value left hand two columns show the formula used to calculate the timing minimum or maximum from the oscillator clock period, prescale value and number of wait cycles inserted.
The value right hand two columns show the timing minimum and maximum for an external clock at 24 MHz divided by 2, prescale value of zero and zero wait status.

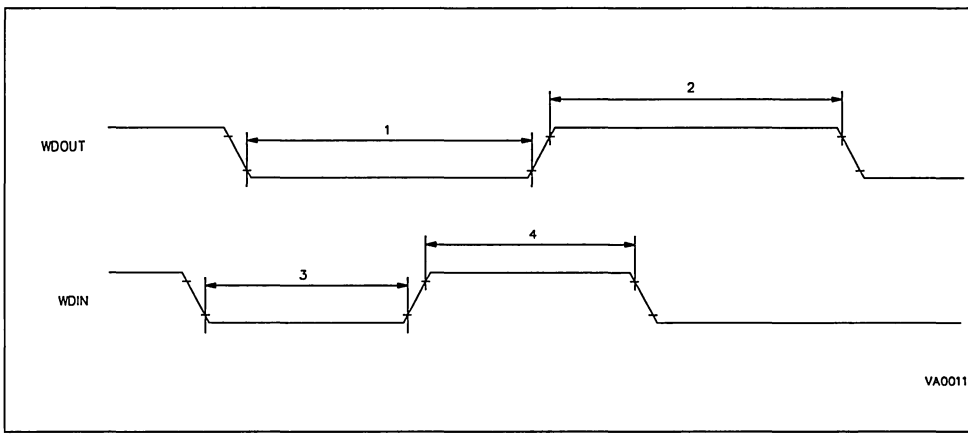
EXTERNAL INTERRUPT TIMING



WATCHDOG TIMING TABLE (V_{DD} = 5V ± 10%, T_A = –40°C to +85°C, Cload = 50pF, INTCLK =12MHz, Output Alternate Function set as Push-pull)

N°	Symbol	Parameter	Value		Unit
			Min.	Max.	
1	TwWDOL	WDOUT Low Pulse Width	620		ns
2	TwWDOH	WDOUT High Pulse Width	620		ns
3	TwWDIL	WDIN Low Pulse Width	350		ns
4	TwWDIH	WDIN High Pulse Width	350		ns

WATCHDOG TIMING

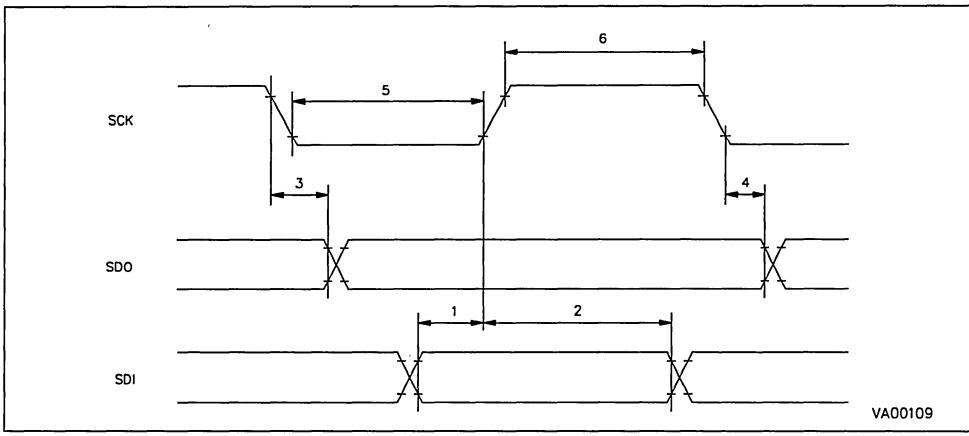


SPI TIMING TABLE (V_{DD} = 5V ± 10%, T_A = –40°C to +85°C, Cload = 50pF, INTCLK = 12MHz, Output Alternate Function set as Push-pull)

N°	Symbol	Parameter	Value		Unit
			Min.	Max.	
1	TsDI	Input Data Set-up Time	100		ns
2	ThDI (1)	Input Data Hold Time	1/2 TpC+100		ns
3	TdOV	SCK to Output Data Valid		100	ns
4	ThDO	Output Data Hold Time	-20		ns
5	TwSKL	SCK Low Pulse Width	300		ns
6	TwSKH	SCK High Pulse Width	300		ns

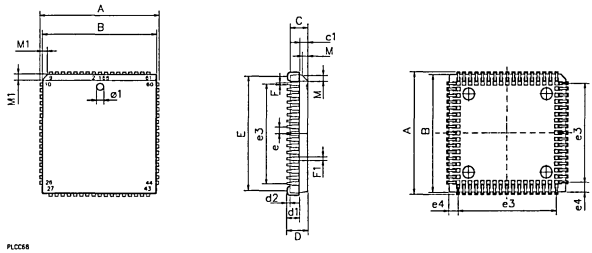
Note: 1. TpC is the Clock period.

SPI TIMING



PACKAGE MECHANICAL DATA

Figure 57. 68-Lead Plastic Leaded Chip Carrier



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A	25.02		25.27	0.985		0.995
B	24.13		24.33	0.950		0.958
D	4.20		5.08	0.165		0.200
d1		2.54			0.100	
d2		0.56			0.022	
E	22.61		23.62	0.890		0.930
e		1.27			0.050	
F		0.38			0.015	
G			0.10			0.004
M		1.27			0.050	
M1		1.14			0.044	
Ø1		7.36			0.289	

ORDERING INFORMATION

Sales Type	Frequency	Temperature Range	Package
ST90R40C6	24MHz	-40°C to +85°C	PLCC68
ST90R40C1	24MHz	0°C to +70°C	PLCC68

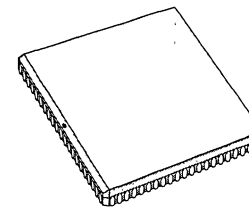
SGS-THOMSON MICROELECTRONICS

ST90R50

ROMLESS HCMOS MCU WITH BANKSWITCH AND A/D CONVERTER

ADVANCE DATA

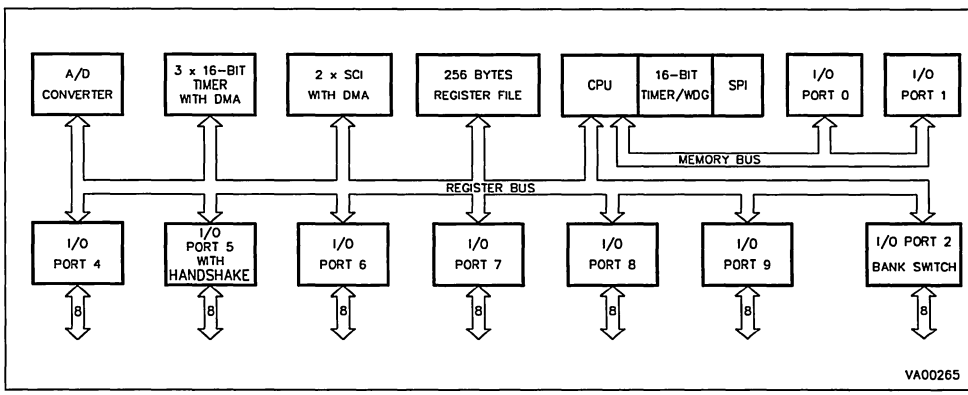
- Single chip microcontroller with 256 bytes of register file with 224 general purpose registers available as RAM, accumulators or index pointers.
- Romless to allow maximum external memory flexibility in development and production phases.
- BankSwitch logic allowing a maximum addressing capability of 8M bytes for program and data spaces (16M byte total).
- 8/16 bit CORE with full feature DMA controller, a powerful interrupt handler and a Standard Serial Peripheral Interface (SPI) handling S-bus, I^2C-bus, IM-bus and Standard Serial Peripheral Interfaces.
- Up to 8 external interrupts edge-selectable plus 1 non-maskable interrupt.
- 16 bit programmable Timer with 8 bit Prescaler, able to be used as a Watchdog Timer for system integrity.
- Three 16 bit Multifunction Timer modules, each with an 8 bit prescaler and 13 operating modes, allowing simple use for complex waveform generation and measurement, PWM functions and many other system timing operations.
- 8 channel Analog to Digital Converter, with integral sample and hold, fast 11µs conversion time, 8 bit ±1/2 LSB resolution with Analog Watchdog on two channels.
- Two full function Serial Communications Interfaces with 110 to 375000 baud rate generator, asynchronous and byte synchronous capability (fully programmable format) and address/wake-up bit option.
- On-chip DMA channels associated to the Multifunction Timers and the Serial Communications Interface.
- Up to nine 8 bit I/O ports with programmable input thresholds and output characteristics. Alternative functions allow the full use of all pins.
- Powerful software development tools, including assembler, linker, C-compiler, archiver, software and hardware emulators.
- Compatible with ST9054, 32k ROM devices (also available in windowed and One Time Programmable EPROM packages).



PLCC84

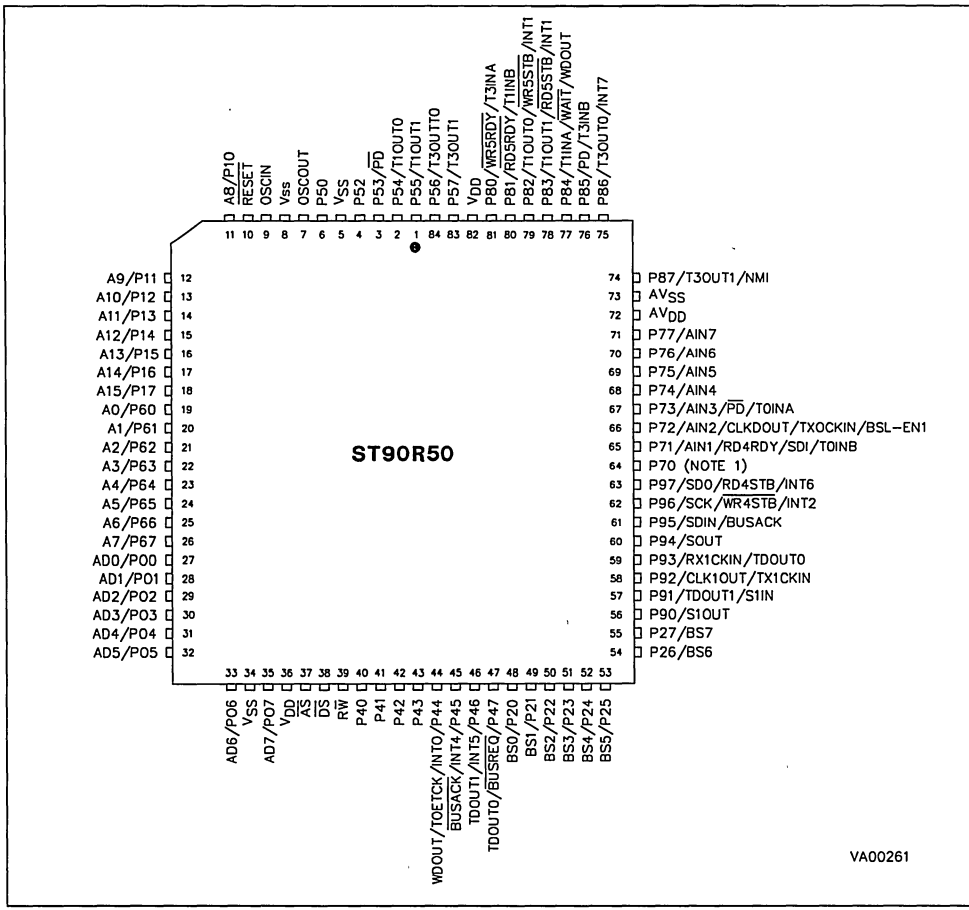
(Ordering Information at the end of the datasheet)

Figure 1. ST90R50 Block Diagram



This is advanced information on a new product now in development or undergoing evalution. Details are subject to change without notice.

Figure 2. ST90R50 Pin Configuration



Note 1 : P70/AIN0/ADTRG/WR4DRDY/RX0CKIN/WDIN/BSH_EN1.

GENERAL DESCRIPTION

The ST90R50 is a ROMLESS member of the ST9 family of microcontrollers, completely developed and produced by SGS-THOMSON Microelectronics using a proprietary n-well HCMOS process.

The ROMLESS part may be used for the prototyping and pre-production phases of development, and offers the maximum in program flexibility in production systems with its 16M byte addressing space when using the Bankswitch memory expansion.

A key point of the ST90R50 architecture is its modular approach which allows software commonality with all other members of the ST9 family.

The nucleus of the modular design of the ST90R50 is the advanced Core which includes the Central Processing Unit (CPU), the Register File, a 16 bit Timer/Watchdog with 8 bit Prescaler, a Serial Peripheral Interface supporting S-bus, I^2C-bus and IM-bus Interface, plus two 8 bit I/O ports. The Core has independent memory and register buses allowing a high degree of pipelining to add to the efficiency of the code execution speed of the extensive instruction set.

GENERAL DESCRIPTION (Continued)

The powerful I/O capabilities demanded by microcontroller applications are fulfilled by the ST90R50 with up to 72 I/O lines dedicated to digital Input/Output. These lines are grouped into up to nine 8 bit I/O Ports and can be configured on a bit basis under software control to provide timing, status signals, address and data buses for interfacing external memory, timer inputs and outputs, analog inputs, external interrupts and serial or parallel I/O with or without handshake.

Three basic memory spaces are available to support this wide range of configurations: Program Memory (external), Data Memory (internal and external) and the Register File, which includes the control and status registers of the on-chip peripherals.

Three 16 bit MultiFunction Timers, each with an 8 bit Prescaler and 13 operating modes allow simple use for complex waveform generation and measurement, PWM functions and many other system timing functions by the usage of the two associated DMA channels for each timer.

In addition there is an 8 channel Analog to Digital Converter with integral sample and hold, fast 11µs conversion time and 8 bit ±1/2 LSB resolution. An Analog Watchdog feature is included for two input channels.

Completing the device are two full duplex Serial Communications Interfaces, each with an integral 110 to 375000 baud rate generator, asynchronous and byte synchronous capability (fully programmable format) and associated address/wake-up option, plus two DMA channels.

PIN DESCRIPTION

$\overline{AS}$. *Address Strobe (output, active low, 3-state).* Address Strobe is pulsed low once at the beginning of each memory cycle. The rising edge of $\overline{AS}$ indicates that address, Read/Write (R/$\overline{W}$), and Data Memory signals are valid for program or data memory transfers. Under program control, $\overline{AS}$ can be placed in a high-impedance state along with Port 0, Port 1, Port 6, Data Strobe ($\overline{DS}$) and R/$\overline{W}$.

$\overline{DS}$. *Data Strobe (output, active low, 3-state).* Data Strobe provides the timing for data movement to or from Port 0 for each memory transfer. During a write cycle, data out is valid at the leading edge of $\overline{DS}$. During a read cycle, Data In must be valid prior to the trailing edge of $\overline{DS}$. When the ST90R50 accesses on-chip RAM memory, $\overline{DS}$ is held high during the whole memory cycle. It can be placed in a high impedance state along with Port 0, Port 1, Port 6, $\overline{AS}$ and R/$\overline{W}$.

R/$\overline{W}$. *Read/Write (output, 3-state).* Read/Write determines the direction of data transfer for external memory transactions. R/$\overline{W}$ is low when writing to external program or data memory, and high for all other transactions. The timing of R/$\overline{W}$ may be modified when using the Bank Switch Logic memory expansion to prevent external timing conflicts. R/$\overline{W}$ can be placed in a high impedance state along with Port 0, Port 1, Port 6, $\overline{AS}$ and $\overline{DS}$.

$\overline{RESET}$. *Reset (input, active low).* The ST9 is initialised by the Reset signal. With the deactivation of $\overline{RESET}$, program execution begins from the Program memory location pointed to by the vector contained in program memory locations 00h and 01h.

OSCIN, OSCOUT. *Oscillator (input and output).* These pins connect a parallel-resonant crystal (24MHz maximum), or an external source to the on-chip clock oscillator and buffer. OSCIN is the input of the oscillator inverter and internal clock generator; OSCOUT is the output of the oscillator inverter.

AV_{DD}. Analog V_{DD} of the Analog to Digital Converter.

AV_{SS}. Analog V_{SS} of the Analog to Digital Converter.

V_{DD}. Main Power Supply Voltage (5V±10%)

V_{SS}. Digital Circuit Ground.

P0.0-P0.7, P1.0-P1.7, P6.0-P6.7 *(Input/Output, TTL or CMOS compatible).* 8 lines grouped into I/O ports of 8 bits providing the external memory interface to address the external program memory.

P2.0-P2.7, P4.0-P4.7, P5.0-P5.7, P7.0-P7.7, P8.0-P8.7, P9.0-P9.7 *I/O Port Lines (Input/Output, TTL or CMOS compatible).* 8 lines grouped into I/O ports of 8 bits, bit programmable under program control as general purpose I/O or as Alternate functions (see next section).

I/O Port Alternate Functions.

Each pin of the I/O ports of the ST90R50 may assume software programmable Alternative Functions as shown in the Pin Configuration Drawings. Table 1 shows the Functions allocated to each I/O Port pins

PIN DESCRIPTION (Continued)

Table 1. ST90R50 I/O Port Alternate Function Summary

I/O PORT Port.bit	Name	Function IN/OUT	Alternate Function	Pin Number
P0.0	A0/D0	I/O	Address/Data bit 0 mux	27
P0.1	A1/D1	I/O	Address/Data bit 1 mux	28
P0.2	A2/D2	I/O	Address/Data bit 2 mux	29
P0.3	A3/D3	I/O	Address/Data bit 3 mux	30
P0.4	A4/D4	I/O	Address/Data bit 4 mux	31
P0.5	A5/D5	I/O	Address/Data bit 5 mux	32
P0.6	A6/D6	I/O	Address/Data bit 6 mux	33
P0.7	A7/D7	I/O	Address/Data bit 7 mux	35
P1.0	A8	O	Address bit 8	11
P1.1	A9	O	Address bit 9	12
P1.2	A10	O	Address bit 10	13
P1.3	A11	O	Address bit 11	14
P1.4	A12	O	Address bit 12	15
P1.5	A13	O	Address bit 13	16
P1.6	A14	O	Address bit 14	17
P1.7	A15	O	Address bit 15	18
P2.0	BS0	O	Bank Switch Address 0 (A16)	48
P2.1	BS1	O	Bank Switch Address 1 (A17)	49
P2.2	BS2	O	Bank Switch Address 2 (A18)	50
P2.3	BS3	O	Bank Switch Address 3 (A19)	51
P2.4	BS4	O	Bank Switch Address 4 (A20)	52
P2.5	BS5	O	Bank Switch Address 5 (A21)	53
P2.6	BS6	O	Bank Switch Address 6 (A22)	54
P2.7	BS7	O	Bank Switch Address 7 (A23)	55
P4.0		I/O	I/O Handshake Port 4	40
P4.1		I/O	I/O Handshake Port 4	41
P4.2		I/O	I/O Handshake Port 4	42
P4.3		I/O	I/O Handshake Port 4	43
P4.4	INT0	I	External interrupt 0	44
P4.4	WDOUT	O	T/WD output	44
P4.4		I/O	I/O Handshake Port 4	44
P4.5	INT4	I	External interrupt 4	45
P4.5	$\overline{\text{BUSACK}}$	O	External Bus Acknowledge	45
P4.5		I/O	I/O Handshake Port 4	45

PIN DESCRIPTION (Continued)

Table 1. ST90R50 I/O Port Alternate Function Summary (Continued)

I/O PORT Port.bit	Name	Function IN/OUT	Alternate Function	Pin Number
P4.6	INT5	I	External interrupt 5	46
P4.6	T0OUTB	O	MF Timer 0 output B	46
P4.6		I/O	I/O Handshake Port 4	46
P4.7	T0OUTA	O	MF Timer 0 output A	47
P4.7	$\overline{\text{BUSREQ}}$	I	External Bus Request	47
P4.7		I/O	I/O Handshake Port 4	47
P5.0		I/O	I/O Handshake Port 5	6
P5.1		I/O	I/O Handshake Port 5	5
P5.2		I/O	I/O Handshake Port 5	4
P5.3		I/O	I/O Handshake Port 5	3
P5.3	P/$\overline{\text{D}}$	O	Program/Data space select	3
P5.4	T1OUTA	O	MF Timer 1 output A	2
P5.4		I/O	I/O Handshake Port 5	2
P5.5	T1OUTB	O	MF Timer 1 output B	1
P5.5		I/O	I/O Handshake Port 5	1
P5.6	T3OUTA	O	MF Timer 3 output A	84
P5.6		I/O	I/O Handshake Port 5	84
P5.7	T3OUTB	O	MF Timer 3 output B	83
P5.7		I/O	I/O Handshake Port 5	83
P6.0	A0	O	Address bit 0 (non mux)	19
P6.1	A1	O	Address bit 1 (non mux)	20
P6.2	A2	O	Address bit 2 (non mux)	21
P6.3	A3	O	Address bit 3 (non mux)	22
P6.4	A4	O	Address bit 4 (non mux)	23
P6.5	A5	O	Address bit 5 (non mux)	24
P6.6	A6	O	Address bit 6 (non mux)	25
P6.7	A7	O	Address bit 7 (non mux)	26
P7.0	AIN0	I	A/D Analog input 0	64
P7.0	ADTRG	I	A/D conversion trigger	64
P7.0	WRRDY4	I	Handshake Write Ready P4	64
P7.0	RX0CKIN	I	SCI0 Receive Clock input	64
P7.0	WDIN	I	T/WD input	64
P7.0	BSH_EN1	I	Bank Switch High Nibble Enable	64
P7.1	AIN1	I	A/D Analog input 1	65

PIN DESCRIPTION (Continued)

Table 1. ST90R50 I/O Port Alternate Function Summary (Continued)

I/O PORT Port.bit	Name	Function IN/OUT	Alternate Function	Pin Number
P7.1	RDRDY4	O	Handshake Read Ready P4	65
P7.1	SDI	I	SPI Serial Data In	65
P7.1	T0INB	I	MF Timer 0 input B	65
P7.2	AIN2	I	A/D Analog input 2	66
P7.2	CLK0OUT	O	SCI0 Byte Sync Clock output	66
P7.2	TX0CKIN	I	SCI0 Transmit Clock input	66
P7.2	BSL_EN1	I	Bank Switch Low Nibble Enable	66
P7.3	AIN3	I	A/D Analog input 3	67
P7.3	P/$\overline{D}$	O	Program/data space select	67
P7.3	T0INA	I	MF Timer 0 input A	67
P7.4	AIN4	I	A/D Analog input 4	68
P7.5	AIN5	I	A/D Analog input 5	69
P7.6	AIN6	I	A/D Analog input 6	70
P7.7	AIN7	I	A/D Analog input 7	71
P8.0	WRRDY5	I	Handshake Write Ready P5	61
P8.0	T3INA	I	MF Timer 3 input A	61
P8.1	RDRDY5	O	Handshake Read Ready P5	60
P8.1	T1INB	I	MF Timer 1 input B	60
P8.2	INT1	I	External interrupt 1	79
P8.2	T1OUTA	O	MF Timer 1 output A	79
P8.2	$\overline{WRSTB5}$	O	Handshake Write Strobe P5	79
P8.3	INT3	I	External interrupt 3	78
P8.3	T1OUTB	O	MF Timer 1 output B	78
P8.3	$\overline{RDSTB5}$	I	Handshake Read Strobe P5	78
P8.4	T1INA	I	MF Timer 1 input A	77
P8.4	$\overline{WAIT}$	I	External Wait input	77
P8.4	WDOUT	O	T/WD output	77
P8.5	P/$\overline{D}$	O	Program/Data space select	76
P8.5	T3INB	I	MF Timer 3 input B	76
P8.6	INT7	I	External interrupt 7	75
P8.6	T3OUTA	O	MF Timer 3 output A	75
P8.7	NMI	I	Non-Maskable Interrupt	74
P8.7	T3OUTB	O	MF Timer 3 output B	74
P9.0	S1OUT	O	SCI1 Serial Output	56

PIN DESCRIPTION (Continued)

Table 1. ST90R50 I/O Port Alternate Function Summary (Continued)

I/O PORT Port.bit	Name	Function IN/OUT	Alternate Function	Pin Number
P9.1	T0OUTB	O	MF Timer 0 output B	57
P9.1	S1IN	I	SCI1 Serial Input	57
P9.2	CLK1OUT	O	SCI1 Byte Sync Clock output	58
P9.2	TX1CKIN	I	SCI1 Transmit Clock input	58
P9.3	RX1CKIN	I	SCI1 Receive Clock input	59
P9.3	T0OUTA	O	MF Timer 0 output A	59
P9.4	S0OUT	O	SCI0 Serial Output	60
P9.5	S0IN	I	SCI0 Serial Input	61
P9.5	$\overline{\text{BUSACK}}$	O	External Bus Acknowledge	61
P9.6	INT2	I	External interrupt 2	62
P9.6	SCK	O	SPI Serial Clock	62
P9.6	WRSTB4	O	Handshake Write Strobe P4	62
P9.7	INT6	I	External interrupt 6	63
P9.7	SDO	O	SPI Serial Data Out	63
P9.7	$\overline{\text{RDSTB4}}$	I	Handshake Read Strobe P4	63

ST90R50 CORE

The Core or Central Processing Unit (CPU) of the ST90R50 includes the 8 bit Arithmetic Logic Unit and the 16 bit Program Counter, System and User Stack Pointers. The microcoded Instruction Set is highly optimised for both byte (8 bit) and word (16 bit) data, BCD and Boolean data types, with 14 addressing modes. Two 8 bit I/O ports are connected to the Core module for external memory interfacing, while a 16 bit Timer/Watchdog gives system security and timing functions, and a Serial Peripheral Interface allows for synchronous communication. Three independent buses are controlled by the Core, a 16 bit Memory bus, an 8 bit Register addressing bus and a 6 bit Interrupt/DMA bus connected to the interrupt and DMA controllers in the on-chip peripherals and the Core. This multiple bus architecture allows a high degree of pipelining and parallel operation within the ST90R50, giving it its efficiency in both numerical calculations and communication with the on-chip peripherals.

MEMORY

The memory of the ST90R50 is functionally divided into two areas, the Register File and Memory. The Memory may optionally be divided into two spaces, each having a maximum of 65,536 bytes. The Memory may be expanded with the Bankswitch logic to give paging of the top 32K bytes of each space to expand the ST90R50 addressing capability to 8M bytes in each space. The two memory spaces are separated by function, one space for Program code, the other for Data. The ST90R50 addresses all program memory in the external PROGRAM space.

Off-chip memory, addressed using the address and data buses (Port 0, Port 1 and Port 6) and may be divided into the Program and Data spaces by the external decoding of the Program/Data select pin (P/$\overline{\text{D}}$) available as an Alternate function. The memory spaces are selected by the execution of the SDM and SPM instructions (Set Data Memory and Set Program Memory, respectively).

MEMORY (Continued)

Figure 3. Memory Spaces, Bankswitch Disabled

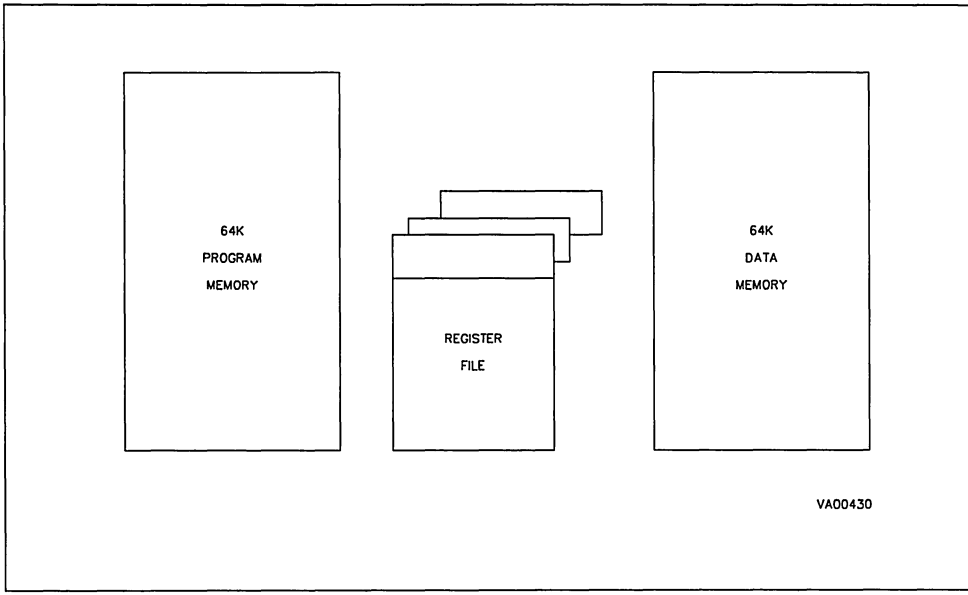
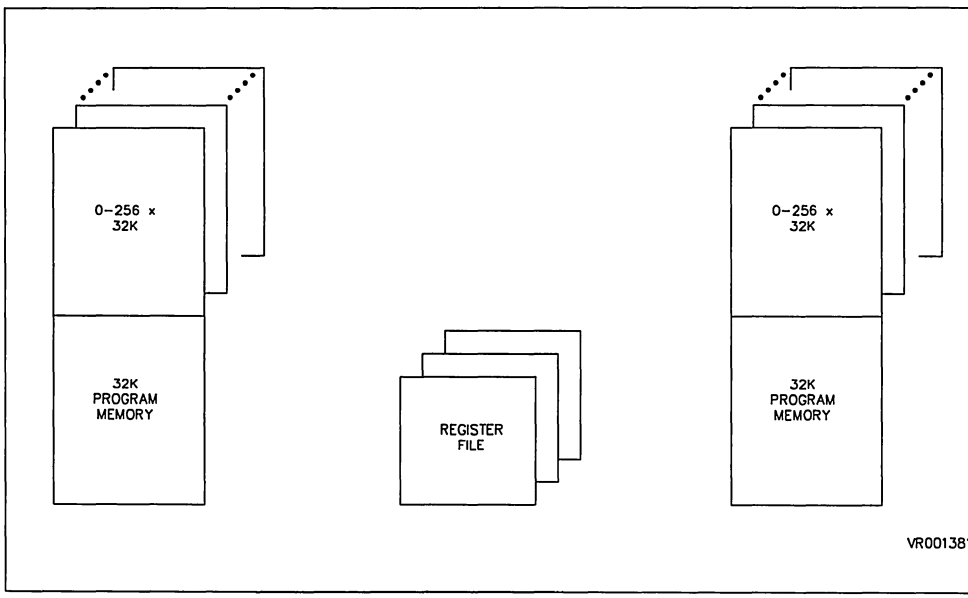


Figure 4. Memory Spaces, Bankswitch Enabled



MEMORY (Continued)

There is no need to use either of these instructions again until the memory area required is to be changed. This requirement is not necessary in two cases: first, when operating with external stacks (the Data memory is automatically selected) and, secondly, when using the memory indirect to memory indirect post-increment addressing mode (the memory types are specified in the instructions: LDPP, LDPD, LDDP, LDDD).

Either the Data Memory or the Program Memory can be addressed using any of the memory addressing modes.

Program Space

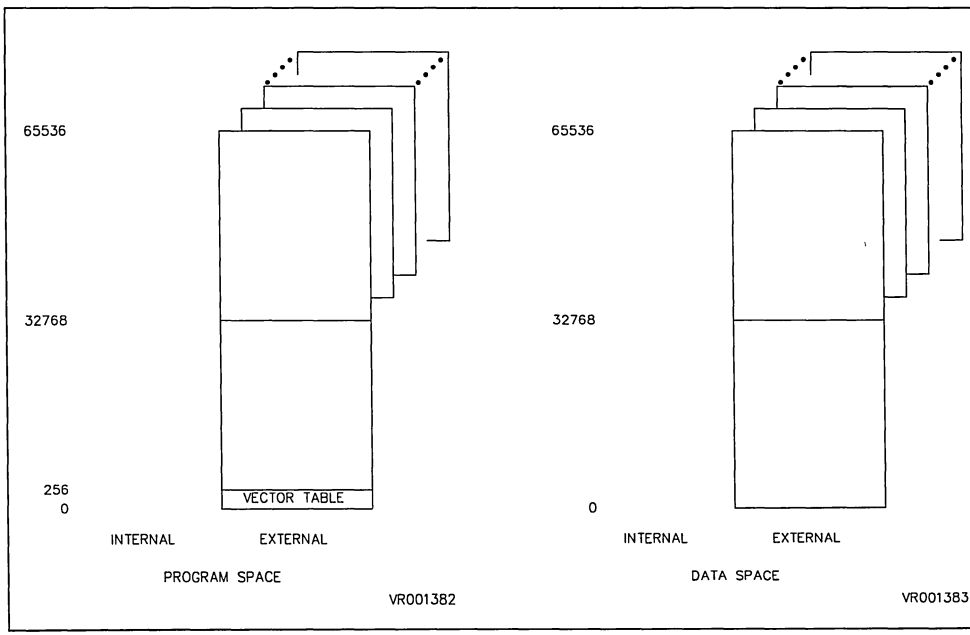
The Program memory space of the ST90R50, 64K bytes of off-chip memory is fully available to the User. The ST90R50 executes external memory cycles for instruction fetches. The first 256 memory locations from address 0 to 0FFh (hexadecimal) hold the Reset Vector, the Top-Level (Pseudo Non-Maskable) interrupt, the Divide by Zero Trap vector and, optionally, the interrupt vector table for use with the on-chip peripherals and the external interrupt sources. Each vector is contained in two consecutive byte locations, the high order address held in the lower (even) byte, the low order address held in the upper (odd) byte, forming the address which is loaded into the Program Counter when selected by the interrupt vector provided by the interrupt source. This should point to the relevant Interrupt Service routine provided by the User for immediate response to the interrupt.

Data Space

The ST90R50 addresses External Data through the External Memory Interface when decoded with the P/$\overline{D}$ pin. On-chip general purpose Registers may be used as additional RAM memory for minimum chip count systems.

The Data Space is selected by the execution of the SDM instruction. All subsequent memory references will access the Data Space. When a separate Data Space is not required, data may stored in external RAM or ROM memory within the Program Space.

Figure 5. Program and Data Spaces



REGISTERS

The ST90R50 register file consists of 240 registers (224 general purpose) plus pages of 16 registers supporting the configuration and control registers for the on-chip peripherals. The 224 general purpose registers all have 8 and 16 bit arithmetic capability and may be used as accumulators, on-chip RAM, internal Stack areas (for system and/or user stacks), or, with the appropriate addressing modes, as index, offset or stack pointers.

The register file is arranged into 16 groups of 16 registers, where the general purpose registers occupy the first 14 groups. The 15th group, E, contains the system registers and Group F contains the pages of the on-chip peripheral control registers.

Group F is paged in this manner due to the modularity of the ST9 family of microcontrollers. Each member of the family retains all general purpose and system registers, only the paged register groups changing owing to the different on-chip peripheral organizations of each device. The User can therefore generate code libraries which use the general purpose registers knowing that they will not be lost on future ST9 devices. To address a paged register, the Page Pointer (PPR, R234) within the system register group must be loaded with the relevant page number using the SPP instruction. Subsequently any access to registers in the top group (R240-R255) will refer to the selected page. This remains set until the next change to the Page Pointer register (by the SPP instruction).

The System group (Group E, registers RE0 to REF) includes the system and user stack pointers, the Mode register, the ALU FLAG register and the Page pointer register. In addition the data registers for the first 6 I/O ports are present, the configuration registers for the ports being in the paged area. This allows the immediate access to these I/O ports at all times.

Figure 6. Register Grouping

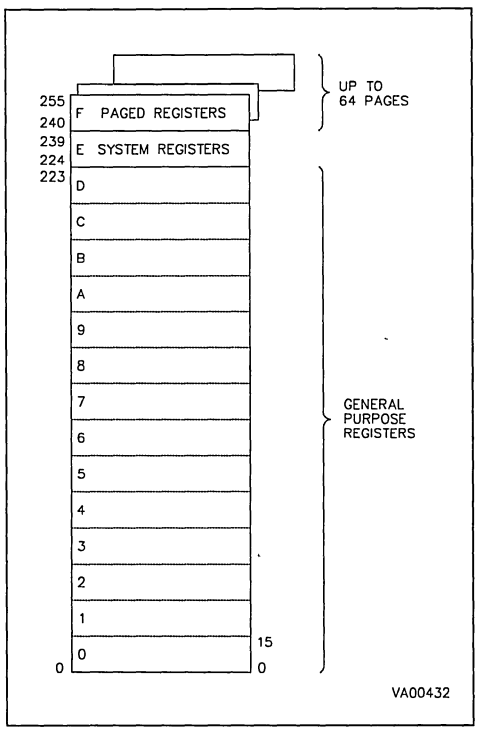
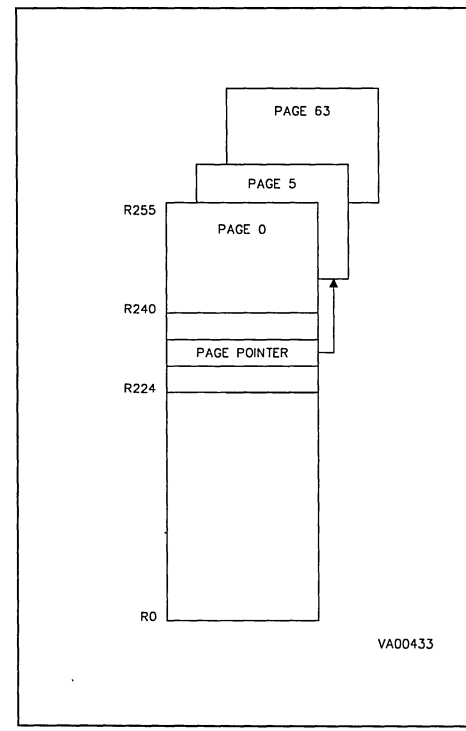
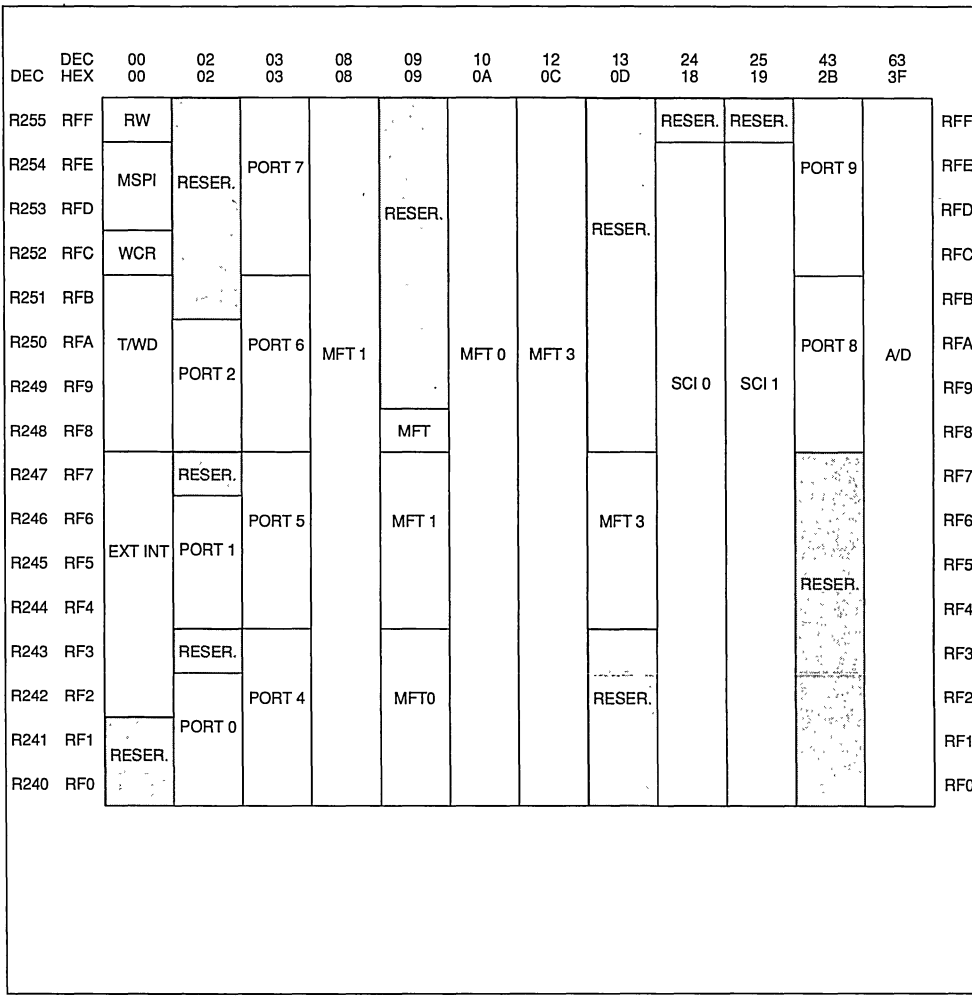


Figure 7. Page Pointer Mechanism



REGISTERS (Continued)

Figure 8. ST90R50 Group F Peripheral Organisation



The Register Pointers, present in the system register group, select groups of registers as "Working Registers", which have faster addressing modes than direct Register addressing and allows smaller code size. The Register Pointers may either be used singly, creating a register group of 16 working registers, or as two independent groups of 8 working registers which may be placed at any 8 register boundary within the register file. The single and twin working register modes are automatically set by hardware when the respective `SRP` and either `SRP0` or `SRP1` instructions are executed. If working registers are used as accumulators and RAM locations for particular tasks, fast context switching on interrupts may be achieved by setting the register pointer to another group for the Interrupt Service

REGISTERS (Continued)

Routine, ISR, (e.g. saving the Register pointer on the stack), using the new group in the ISR and subsequently restoring the original group before the Return from Interrupt instruction. Working registers also allow the use of the ABAR - Any Bit-Any Register Boolean operations (including directly on the I/O port data registers).

In the ST9 syntax, directly addressed Registers are indicated with a capital R e.g. R0, R224, RBF, with Register Pairs (16 bit accumulators or memory pointers) as RR0, RR24. When using Working Registers, groups of 16 registers (SRP instruction) are denoted as r0 to r15 (rr0 to rr14), while the dual working register group are addressed as r0 to r7 (rr0 to rr6), for the first group of 8 registers (SRP0), with r8 to r15 (rr8 to rr14) for the second set (SRP1).

Working register addressing requires a 4 bit field within the instruction. When packed into a byte, the upper nibble is set to Dh (1101b), this being the escape code to indicate the use of the working registers. As a result, group D CANNOT be selected with direct register addressing, it is recommended that this group be used as internal stacking area when using register file based system or user stack pointers.

Figure 9. Groupe E Register Map

R239	System Stack Pointer Low (SSPLR)
R238	System Stack Pointer High (SSPHR)
R237	User Stack Pointer Low (USPLR)
R236	User Stack Pointer High (USPHR)
R235	Mode Register (MODER)
R234	Page Pointer (PPR)
R233	Register Pointer 1 (RP1R)
R232	Register Pointer 0 (RP0R)
R231	ALU Flags (FLAGR)
R230	Central Interrupts Control (CICR)
R229	Port 5 Data (P5DR)
R228	Port 4 Data (P4DR)
R227	Port 3 Data (P3DR)
R226	Port 2 Data (P2DR)
R225	Port 1 Data (P1DR)
R224	Port 0 Data (P0DR)

Figure 10. Single Working Register Bank

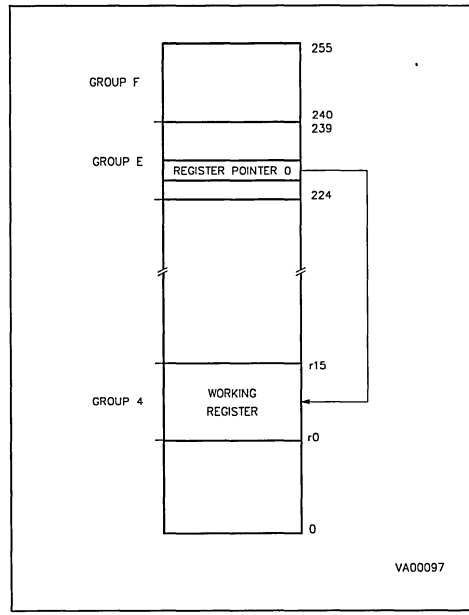
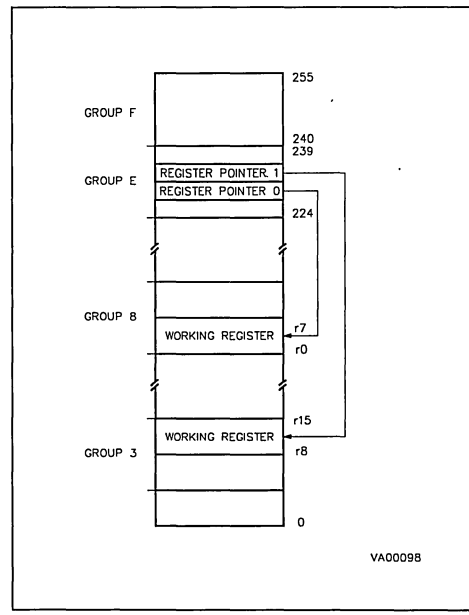


Figure 11. Dual Working Register Banks



STACK POINTERS

There are two separate, double register stack pointers available (System and User), both of which can operate in register or Data memory address spaces. These operate in a Pre-Decrement mode when data is PUSHed onto the Stack and in a Post-Increment mode when data is POPed from the stack.

The SYSTEM Stack Pointer (SSPR, R238:R239) is used for the storage of temporarily suspended system and/or control registers (ie the the Program Counter and FLAG register) while interrupts are being serviced, and is used for the storage of the Program Counter following the CALLing of a subroutine.

The USER Stack Pointer (USPR, R236:R237) is completely free from all interference from automatic operations and so provides for a totally User controlled stack area.

Both Stack pointers may operate with both byte (PUSH,POP) and word (PUSHW,POPW) data, and are differentiated by appending a "U" to the instruction mnemonic for the User Stack (PUSHU/PUSHUW, POPU/POPUW).

When the Stack Pointers are using RAM Memory as the stack areas, a full word register is used as the pointer, while when operating with the stack area within the Register File (Groups 0 to 14 only, but not the within the system and paged groups) only an 8 bit register is required for addressing and consequently only the low byte of the word registers are used (R239 for the System Stack and R237 for the User Stack). In this latter case the upper byte of the stack pointer registers (R238 and R236) must be considered as reserved. The Stack Pointers may be selected to point to RAM or Register file by the setting of the SSP (MODER.7) and USP (MODER.6) of the ST90R50 configuration register (MODER, R235) where a "1" denotes Register file operation (Default at Reset) and "0" causes external Data space operation.

Figure 12. Internal Stack Pointers

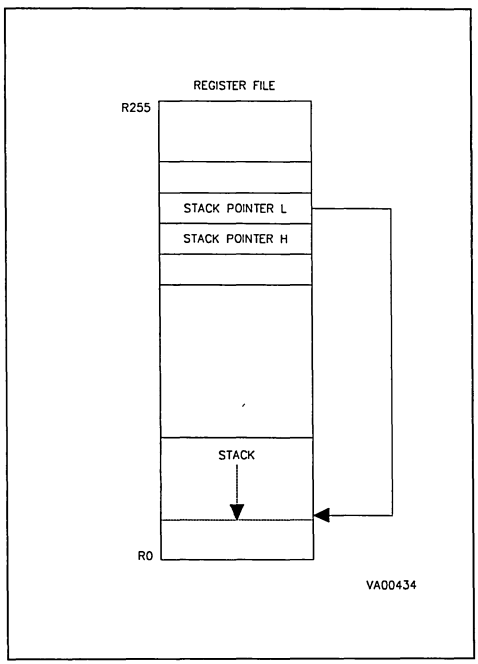
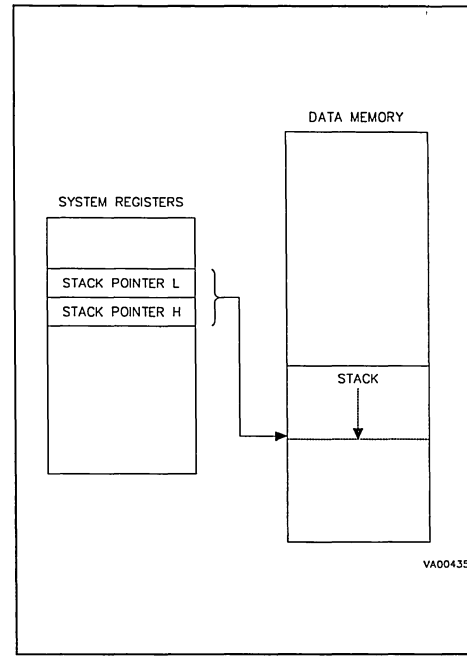


Figure 13. External Stack Pointers



INTERRUPTS

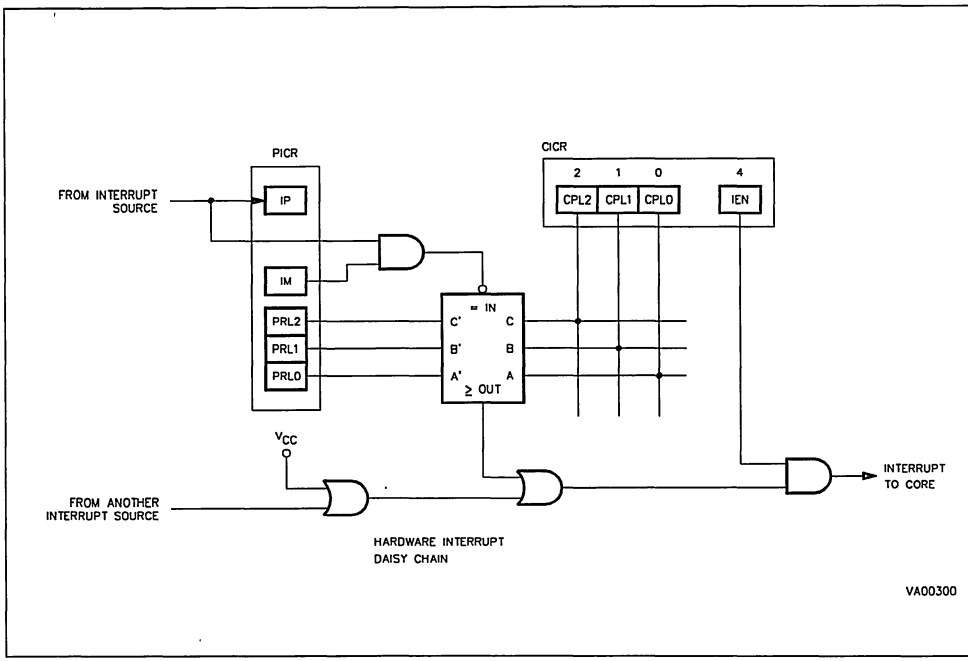
The ST90R50 offers a powerful solution to the response requirements of real-time systems with its advanced interrupt structure. Interrupt trigger sources can be prioritized within 8 levels to match the priorities assigned to the application. In addition a top-level or non-maskable interrupt is available.

The ST90R50 interrupts follow the logical flow of Figure 14.

Interrupt events (selectable with each function) cause the setting of the Interrupt Pending (IP) bit within the status register of the peripheral. This bit may also be set by software in order to generate a software interrupt, and should normally be reset by software within the interrupt service routine. If the interrupt is not Masked with the corresponding Interrupt Mask bit, the interrupt is passed to the central interrupt control logic where the priority level assigned by the User to the interrupt source is compared with the priority level of the core (User programmed dynamically in the 3 bits of the Central Priority register (CPL, CICR.0-2, Level 7 is the lowest priority and level 0 the highest). If the incoming priority level is higher than the CPL, and Global Interrupts are enabled (by the `EI` instruction, interrupts are disabled by the execution of the `DI` instruction), the interrupt is acknowledged. If interrupts are globally disabled, the priority level of the source is lower than or equal to the CPL or the Interrupt is masked, then the IP bit remains set and the interrupt is held pending until the `EI` instruction is executed, the CPL is set to a lower level AND the interrupt is un-masked. Alternatively the IP bit of a masked interrupt source may be used in a polled interrupt environment, with the IP bit being reset by software within the service routine.

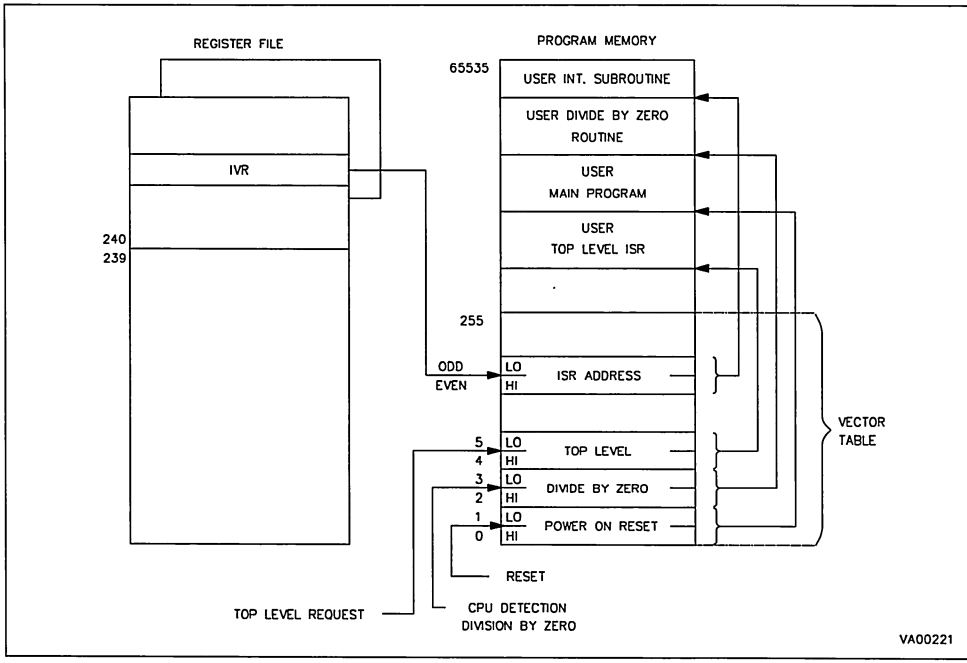
The interrupt acknowledge cycle causes the Program Counter and FLAGS register to be pushed onto the System Stack (PC low byte first, PC high byte, then FLAGS Register) and all maskable interrupts to be disabled by resetting the IEN bit (CICR.4). The peripheral Interrupt Vector, IVR, a User programmable feature of the peripheral interrupt control registers, is used as an offset into the vector table, pointing to the high byte (even address) of the 16 bit address which should contain the starting address of the interrupt service routine. Addresses 0 through 255 of the program space comprise the interrupt vector table. Where multiple

Figure 14. Interrupt Logic



INTERRUPTS (Continued)

Figure 15. Interrupt Vector Table Usage



interrupt sources may occur within a peripheral, the peripheral interrupt vector source may be encoded by hardware set bits within the IVR register. This means that the vector address defined in the peripheral IVR is the base address for a block of vectors servicing that peripheral. The address pointed to by the vector is loaded into the Program Counter and execution restarts from this point.

The interrupt service routine should clear the interrupt pending flag of the interrupt source and take the appropriate action. The last instruction of the interrupt service routine should be the `IRET` instruction, the action of this is to restore the Program Counter and Flags register to their value prior to the interrupt acknowledgment, and to re-enable interrupts. Within the interrupt service routine, use may be made of the working register pointer mechanism to reduce the context switching time.

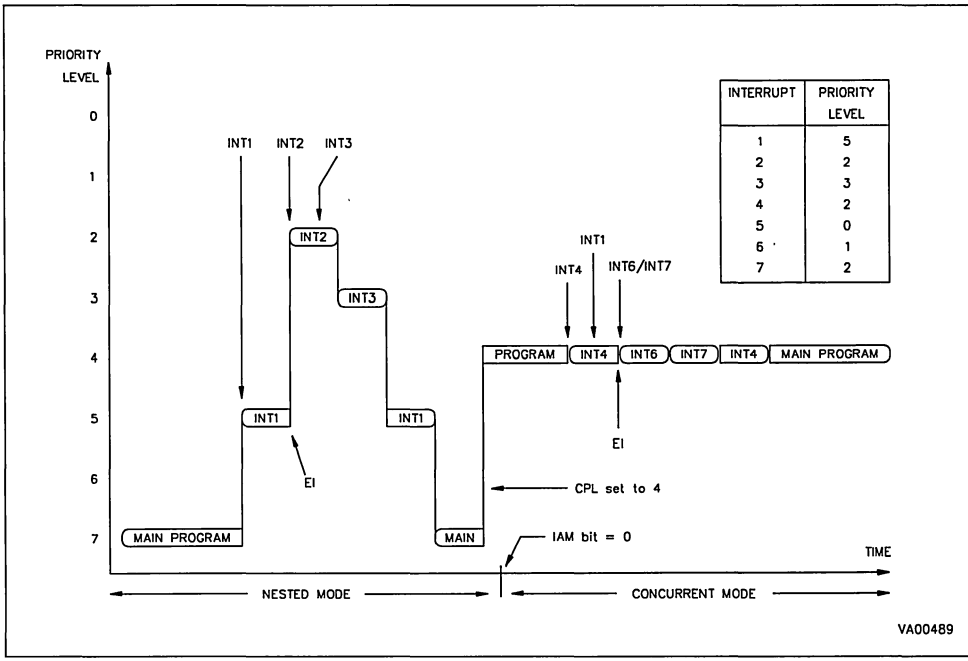
Two interrupt arbitration modes are available for use with the 8 level priority scheme, Nested and Concurrent modes. These are selected by the status of the IAM bit (CICR.3).

Concurrent mode, selected when IAM = "0" (the reset condition) is the standard interrupt arbitration mode, where the arbitration phase of every instruction acknowledges interrupts according to their priority level (if higher than the CPL) and follows the sequence shown. All pending interrupts existing or having eventually occurred during interrupt service routine execution, remain pending until the Enable Interrupt instruction (`EI`) (even if it is executed during the interrupt service routine). `EI` within the interrupt service routine is not recommended for use with the Concurrent arbitration mode as this can trigger a Last In, First Out condition where high priority interrupts are masked by lower priority interrupts which are all higher than the CPL value.

Nested mode, selected when IAM = "1", uses the same arbitration phase as concurrent mode, the difference being that the CPL is modified during the interrupt processing cycle to that of the acknowledged interrupt level. The CPL value is pushed by hardware into the Nested Interrupt Control register (NICR, R247 page 0) by setting the NICR bit corresponding to the CPL value. The interrupt service

INTERRUPTS (Continued)

Figure 16. Interrupt Modes Example of Usage



routine is entered in the normal manner. The revised CPL level is used for arbitration of further interrupts, each higher level being saved on the NICR stack, and being restored automatically by hardware with the `IRET` instruction. This allows the execution of the `EI` instruction within the interrupt service routine to operate the correct nesting of interrupts. The two modes are shown graphically in Figure 16, where the Y axis shows the CPL value. It should be noted that in the example INT1 will not be acknowledged until the CPL level is programmed to a lower level.

Interrupts coming from on-chip sources at the same instant, and at the same priority level, are resolved during the arbitration phase according to a hardware daisy-chain. This follows the priorities of the table shown in Table 2.

Table 2. ST90R50 Interrupt Hardware Daisy Chain

INTA	High Priority
INTB	
INTC	
INTD	
MFTIMER0	
SCI 0	
SCI 1	
A/D	
MFTIMER3	
MFTIMER1	Lowest Priority

INTERRUPTS (Continued)

External Interrupts. Up to 8 external interrupts are available on the ST90R50 as alternate function inputs of I/O pins. These may be selected to be triggered on rising or falling edges and can be independently masked. The eight external interrupt sources are grouped into four pairs or channels which can be assigned to independent interrupt priority levels. Within each channel the even interrupt number takes the even priority level and the odd channel the odd priority level (even+1).

Table 3. External Interrupt Channel Grouping

External Interrupt	Channel
INT7 INT6	INTD1 INTD0
INT5 INT4	INTC1 INTC0
INT3 INT2	INTB1 INTB0
INT1 INT0	INTA1 INTA0

Several of the External Interrupt channels have their inputs selectable between the external interrupt source and on-chip peripheral sources.

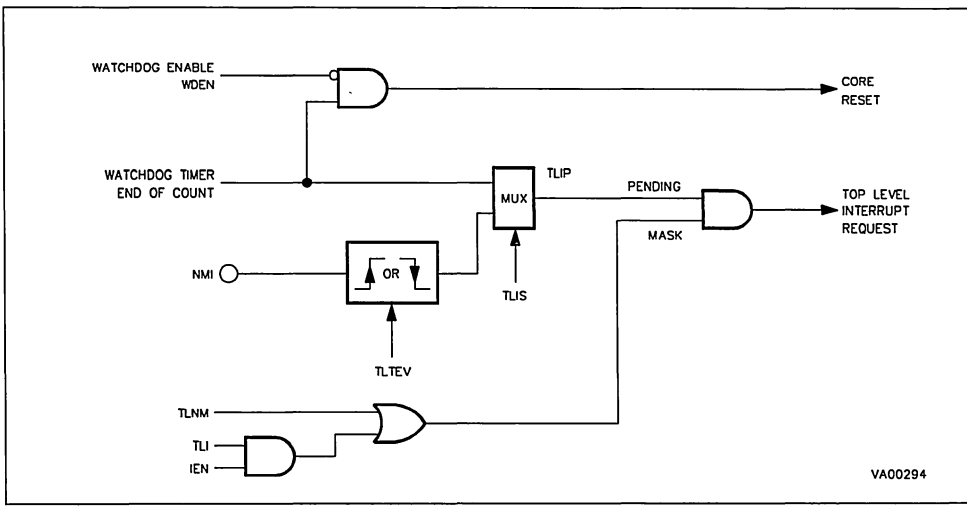
Table 4. ST90R50 External Interrupt Souce Selection

INT0	INTA0
Timer/Watchdog End of Count	
INT2	INTB0
SPI Interrupt	

Top Level Interrupt. The Top Level Interrupt channel can be assigned either to the external NMI pin or to the Timer/Watchdog output. When selected as the external NMI pin, the active edge may be programmed to be rising or falling. The TLI event will cause the setting of the TLIP bit (CICR.6) and according to the mask situation, a Top Level Interrupt request may be generated. Two masking conditions are available, a Maskable Mask and a Not-Maskable Mask.

The Maskable Top Level Interrupt may be enabled or disabled by software and follows the state of the Global Interrupt Enable bit IEN (CICR.4), while the Not-Maskable Mask bit (TLI, CICR.5) is a set-only mask. Once set, the Top Level Interrupt is active independently of IEN and cannot be disabled until the next Reset cycle.

Figure 17. Top-Level Interrupt Structure



DMA

The ST90R50 has on-chip DMA channels to provide high-speed data transaction between peripherals and Memory or Register File. Multi-channel DMA is fully supported because each peripheral can have its own DMA channel(s). Each DMA channel transfers data to/from contiguous locations of the Register File, Program Memory or Data Memory. The maximum number of transactions that each DMA channel can perform is 222 if the Register File is selected and 65536 if Program or Data Memory are selected.

DMA transfer to (or from) the Register File takes 8 INTCLK cycles, DMA transfer to (or from) Memory takes 16 INTCLK cycles. If the ST90R50 is in the idle mode (following the execution of the `WFI` instruction), DMA requests are acknowledged according to their priority and control is returned to the idle mode pending an interrupt, this operation increases the number of INTCLK cycles by 2 for both Register File and Memory DMA transactions.

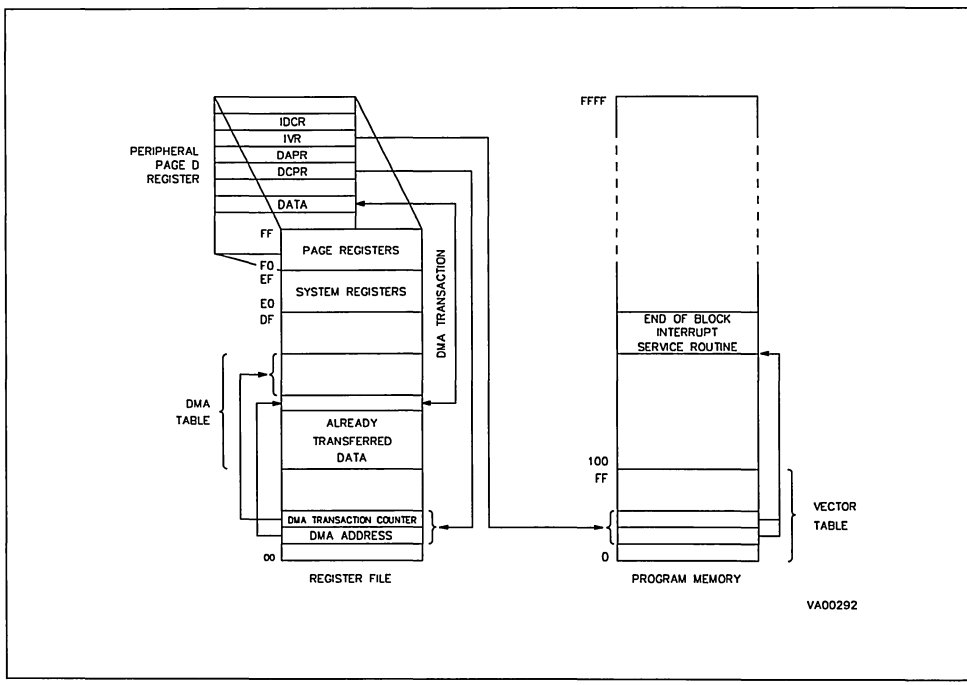
Each DMA channel has its own control registers located in the page(s) related to the peripheral.

There are two pointer registers, DAPR which points to a register or register pair containing the current DMA address to/from which data will be transferred, and DCPR, which points to a register or register pair which contain the transaction counter for the DMA operations. Each DMA transfer consists of three operations:

- A load from/to the peripheral data register to/from a location of Register File (or Memory) addressed through the DMA Address Register (or Register Pair)
- A post-increment of the DMA Address Register (or Register Pair)
- A post-decrement of the DMA transaction counter, which contains the number of transactions that have still to be performed.

When the transaction counter reaches 0 (all data has been transferred) an End of Block Interrupt event is generated to allow the processing of the DMA data block, or, by reloading the Address and counter registers and retriggering, a repeated DMA cycle.

Figure 18. DMA Between Registers and Peripheral

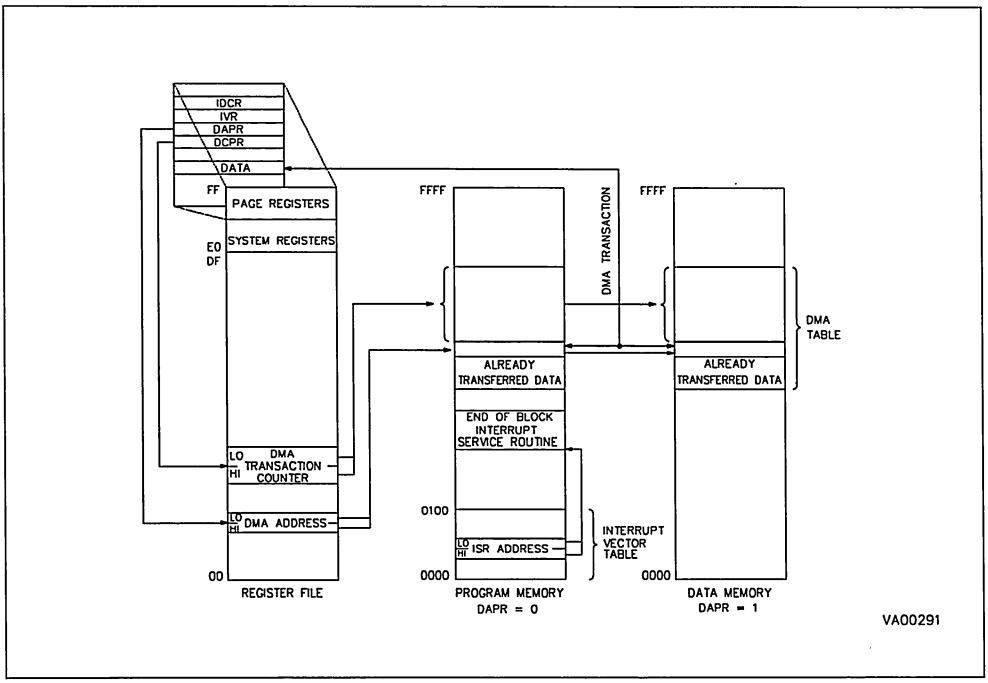


DMA (Continued)

A SWAP mode, allowing continuous DMA operation, is available for the Multifunction Timer and is described in the section relating to the Multifunction Timer.

The ST90R50 has DMA channels associated with the Serial Communications Interface Input and Output Serial data channels; the 16 bit Load/Capture Register 0, CAPT0R, of each Multifunction Timer allowing the timing of external signals to be captured into a table for off-line analysis or for the automatic output of PWM signals of variable width and timing; and the 16 bit Comparison Register 0, COMP0R, of each Multifunction Timer which can be programmed to cause output or input of parallel data through the handshake ports under DMA.

Figure 19. DMA Between Memory and Peripheral



CLOCK GENERATION, WAIT, HALT AND RESET

Clock Generation

The ST90R50 Clock Generator module generates the internal clock for the ST9 core and the on-chip peripherals, it may be driven by an external quartz crystal circuit, connected to the OSCIN and OSCOUT pins, or by an external pulse generator connected to OSCIN (Figures 20, 21).

The conceptual schematic of the ST9 internal clock circuit is shown in Figure 22.

The maximum external frequency of the ST9 is 24 MHz, while the maximum internal operating frequency is 12 MHz, thus a programmable divide by two circuit is present, this allows the use of high frequency crystals for economy, or low frequency crystals for reduction in radiated noise. This divider is active upon exit from the reset condition, the User may bypass the divide by two circuit by setting the DIV2 bit (MODER.5). The resulting clock from this section is named INTCLK, the internal clock which drives the timebases of the on-chip clock for the ST90R50 peripherals (eg the Multifunction Timer,

Figure 20. Crystal Oscillator

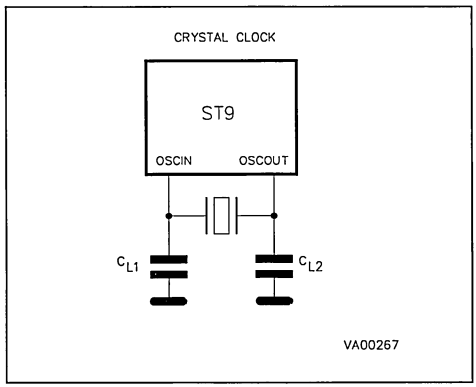


Figure 21. External Oscillator

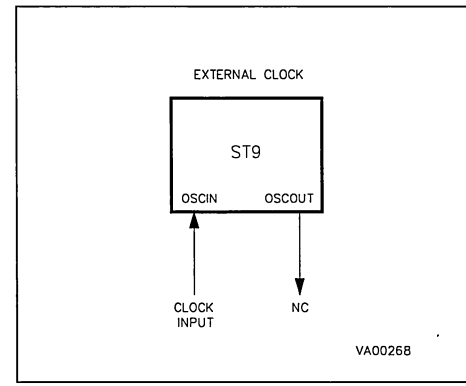
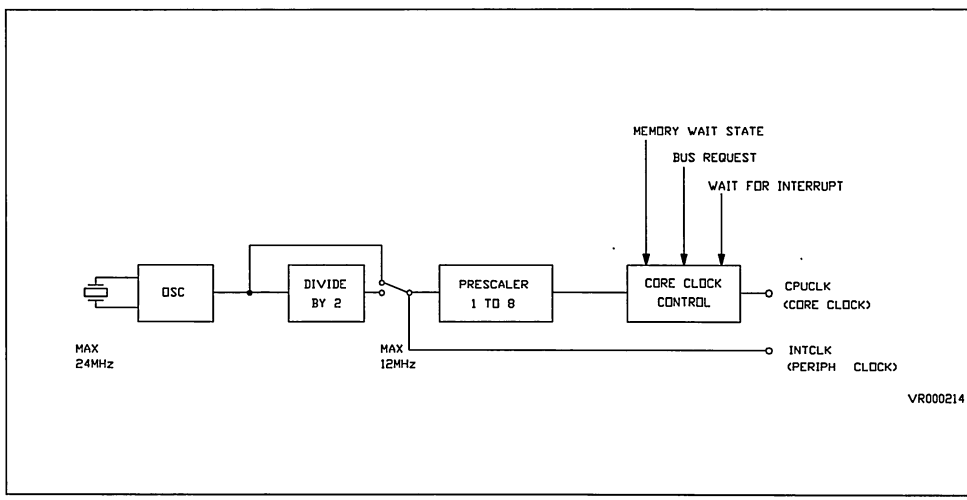


Figure 22. Internal Clock Circuit



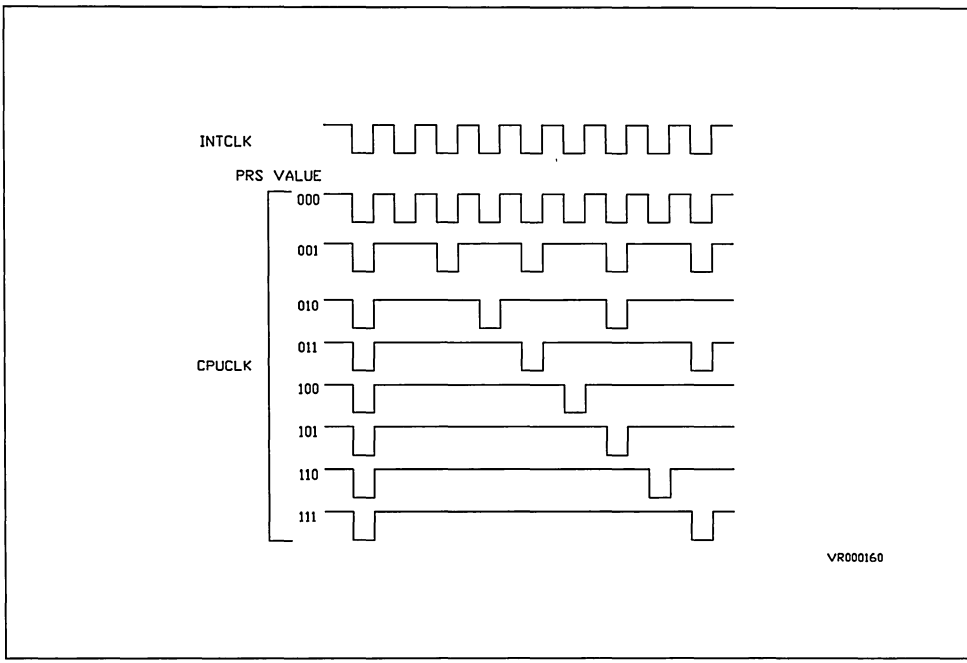
CLOCK GENERATION, WAIT, HALT AND RESET (Continued)

Timer/Watchdog, Serial Communications Interface) and also the input of the CPU prescaler section. The CPU of the ST9 includes the instruction execution logic and may run at different rates according to the setting of the PRS2,PRS1 and PRS0 bits (MODER.4-2) (figure 23). The resulting clock is named CPUCLK and it should be noted that this does not maintain a 50% duty cycle, but stretches the high level of the clock until completion. The CPUCLK prescaler allows the User to slow down the program execution time (eg for lower power consumption), while time-critical sections of the program may tune the CPUCLK execution speed to high speed and then restore it to its original speed.

Wait States

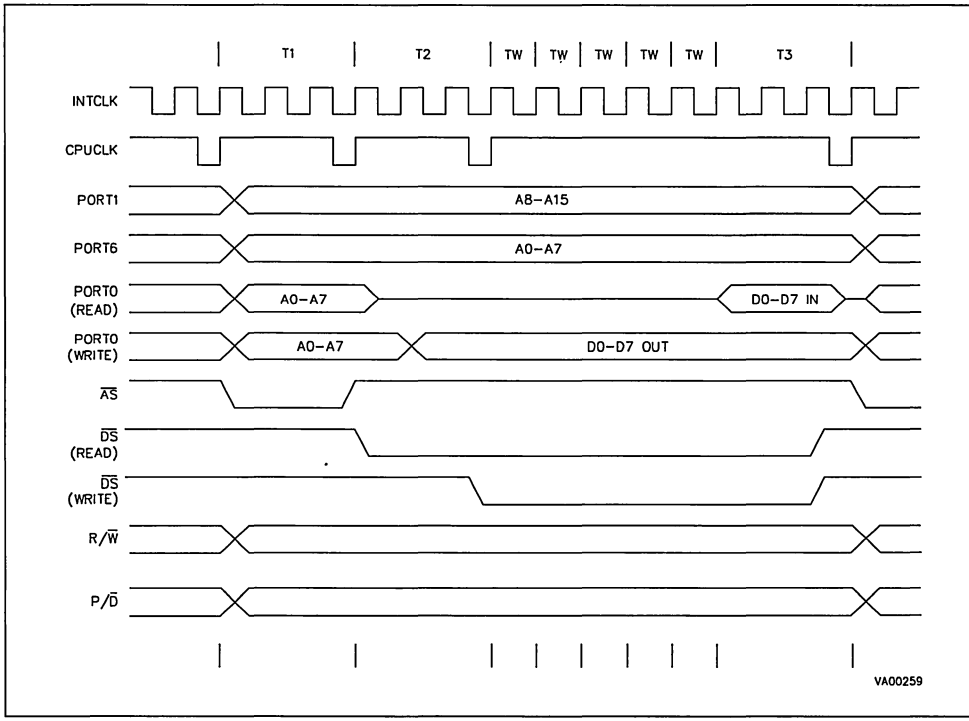
The output from the prescaler can also be affected by wait states. Wait states from two sources allow the User to tailor timing for slow external memories or peripherals. The internal Wait State generator will insert from 0 to 7 wait states, independently programmable for both Program and Data Spaces, via the Wait Control Register WCR (R252, page 0). The second source of wait states is the external Wait input pin when enabled as the Alternate Function. Fig 24 shows the External Memory Interface timing as it relates to CPUCLK prescaling of 2 and 5 added wait states. The added wait states are derived from the INTCLK clock cycle, not CPUCLK. Internal memory is always accessed with no Wait states.

Figure 23. CPUCLK Prescaler



CLOCK GENERATION, WAIT, HALT AND RESET (Continued)

Figure 24. External Memory Interface Timing with CPUCLK Prescaling and 5 Added Wait States

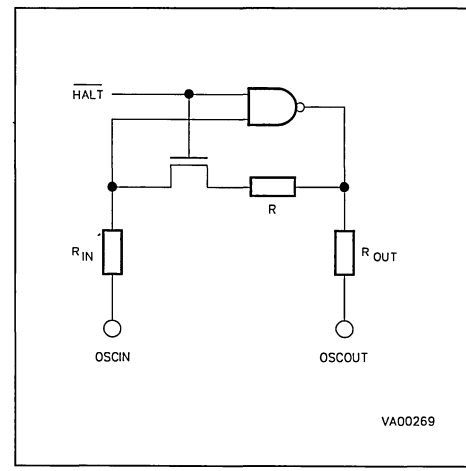


Halt and Wait for Interrupt (WFI) States

The schematic of the on-chip oscillator circuit is shown in figure 25. The HALT condition, caused by the execution of the HALT instruction, disables the oscillator, forcing OSCOUT high. This places the ST90R50 into the lowest power mode. The exit of the HALT condition and the restarting of the oscillator requires a RESET pulse with a minimum duration of 10ms (figure 26). It must be noted that if the TIMER/WATCHDOG has the WATCHDOG mode enabled, a HALT instruction will not disable the oscillator; this is to avoid stopping the Watchdog if, by an error, a HALT instruction is executed. If this occurs, the ST90R50 runs in an endless loop terminated only by the Watchdog reset (or hardware reset).

The WFI (Wait for Interrupt) instruction suspends program execution until an interrupt request is acknowledged. During this period, DMA transactions are allowed if their priority is higher than or equal to the CPL level; the ST90R50 returns to WFI

Figure 25. Oscillator Schematic



CLOCK GENERATION, WAIT, HALT AND RESET (Continued)

mode after completion of the DMA transfer. The CPUCLK is halted during Wait For Interrupt while INTCLK continues to run, thus the power consumption of the processor is lowered by the CORE power consumption value.

The External Memory Interface lines status during HALT and WFI modes is shown in Table 5.

Table 5. External Memory Interface Line Status During WFI and Halt

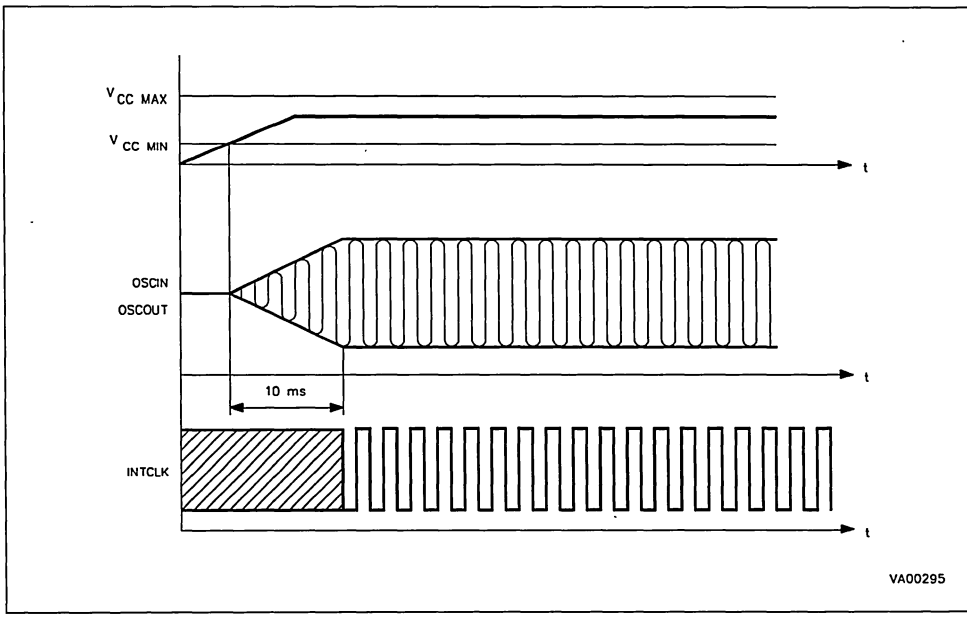
P0 (AD0-AD7)	High Impedance
P1 (A8-A15)	Forced to Address of Next Opcode
$\overline{AS}$	Forced High
$\overline{DS}$	Forced High
R/$\overline{W}$	Forced High

Reset

The processor Reset overrides all other conditions and forces the ST90R50 to the reset state. During Reset, the internal registers are set to their Reset values, as shown in Table 6 for the system and Page 0 Registers. The I/O Ports pins are set to the Bidirectional Weak Pull-up mode. The User must then initialize the ST90R50 registers to give the required functions.

The Reset condition can be generated from the external $\overline{RESET}$ pin or by the on-chip TIMER/WATCHDOG operating in Watchdog mode. To guarantee the complete reset of the ST90R50, the $\overline{RESET}$ input pin must be held low for at minimum of 53 crystal periods in addition to the crystal start-up period. The Watchdog $\overline{RESET}$ will occur if the Watchdog mode is enabled (WDEN, WCR.6, is reset) and if the programmed period has elapsed without the code 0AAh,55h written to the appropriate register. The input pin $\overline{RESET}$ is not driven low by the on-chip reset generated by the TIMER/WATCHDOG.

Figure 26. Reset Timing Requirements from Halt State



CLOCK GENERATION, WAIT, HALT AND RESET (Continued)

Table 6. System and Page 0 Reset Values

Register Number	System Register Reset Value	Page 0 Register Reset Value
F	(SSPLR) = undefined	Reserved
E	(SSPHR) = undefined	(SPICR) = 00h
D	(USPLR) = undefined	(SPIDR) = undefined
C	(USPHR) = undefined	(WCR) = 7Fh
B	(MODER) = E0h	(WDTCR) = 12h
A	(Page Ptr) = undefined	(WDTPR) = undefined
9	(Reg Ptr 1) = undefined	(WDTLR) = undefined
8	(Reg Ptr 0) = undefined	(WDTHR) = undefined
7	(FLAGR) = undefined	(NICR) = 00h
6	(CICR) = 87h	(EIVR) = x2h
5	(PORT5) = FFh	(EIPLR) = FFh
4	(PORT4) = FFh	(EIMR) = 00h
3	(PORT3) = FFh	(EIPR) = 00h
2	(PORT2) = FFh	(EITR) = 00h
1	(PORT1) = FFh	Reserved
0	(PORT 0) = FFh	Reserved

During the $\overline{\text{RESET}}$ state, $\overline{\text{DS}}$ is held low and $\overline{\text{AS}}$ is toggled with the frequency of the crystal (OSCIN) divided by 32. This condition may be recognized by external peripherals as a Reset condition. It may also be used to enable the synchronization of multiple ST90R50 running from the same clock in a multi-processing or high security majority voting system.

Once the Reset pin reaches a logical high, the ST90R50 fetches the starting address from locations 0 and 1 of the program space and begins program execution from this address after 67 crystal cycles.

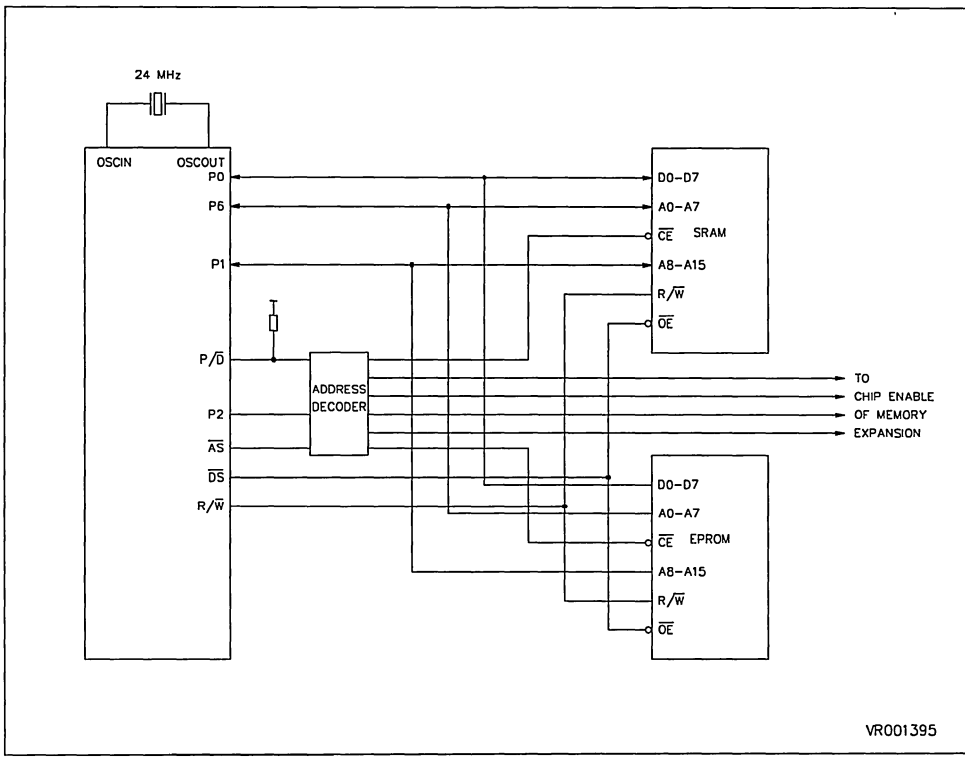
INTERFACING TO EXTERNAL MEMORY

External Memory and/or peripherals may be connected to the ST90R50 through its External Memory Interface. This provides the multiplexed Address bits A0 to A7 and Data bits D0 to D7 on Port 0, and the higher order address bits A8 to A15 on Port 1, giving the full 64K bytes addressing capability. Port 6 is available to be programmed as non-multiplexed address outputs A0 to A7 to reduce the requirement for an external latch to demultiplex the low order addresses. Port 0, in this case, becomes solely the Data I/O port. The Program/Data (P/$\overline{D}$) output, when selected as an Alternate function, allows external decoding to provide for the two independent pages for Program and Data.

Data transfer timing is generated by the Address strobe $\overline{AS}$ and the data strobe $\overline{DS}$. Address strobe low indicates that the data present on AD0 to AD7 is the low order address and is guaranteed valid on the rising edge of $\overline{AS}$ allowing for latching of the address bits by an external latch (if Port 6 is not used). Data transfer direction is indicated by the status of the Read/Write (R/$\overline{W}$) pin; for write cycles (R/$\overline{W}$ low), data out is valid at the falling edge of $\overline{DS}$; for read cycles (R/$\overline{W}$ high), data in must be valid prior to the rising edge of $\overline{DS}$. The timing of the R/$\overline{W}$ signal may be modified by the setting of the RW bit (bit 0 Register 0FFh, page 0) in order to accomodate different types of external memories. In addition, when the Bank Switch logic is enabled, the timing of the Bank Switch outputs may be modified by software to prevent potential conflicts on the data bus. Please refer to following sections for further details.

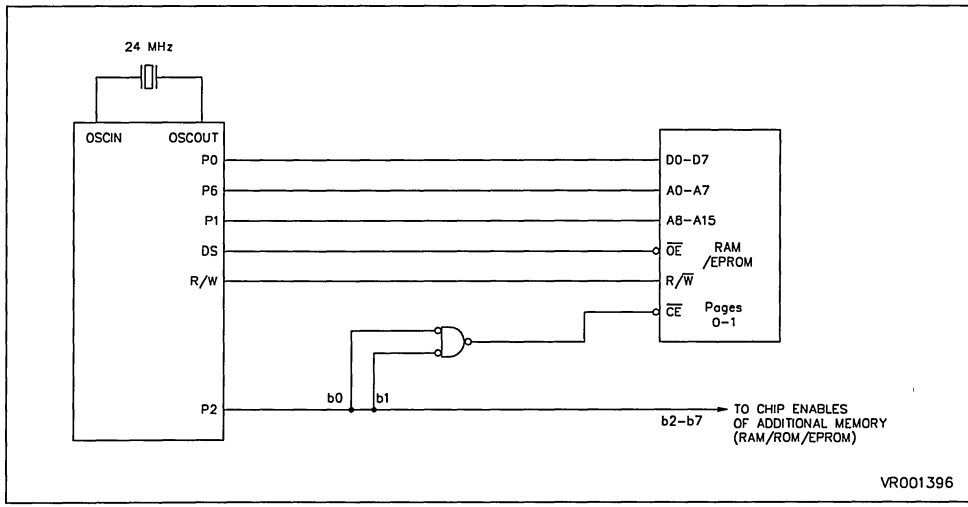
The Data Strobe low period may be extended to accomodate slow external devices by the adding of internally generated wait cycles (0 to 7 cycles for both program and data memory maps) or by an external input on the WAIT input pin also available as an Alternative Function of an I/O bit. Suggested interface circuits are shown in figures 27 and 28.

Figure 27. External Memory Addressing Circuit



INTERFACING TO EXTERNAL MEMORY (Continued)

Figure 28. External Memory Addressing Circuit



BANKSWITCH LOGIC

Port 2 of the ST90R50 may be programmed by the User to become extended address lines allowing expansion of the memory to a maximum of 8M bytes in both program and data pages. This is achieved by paging of the top 32K bytes of memory (A15 high, addresses 8000h to FFFFh), with the lower 32K bytes (A15 low addresses 0000h to 7FFFh) remaining static. The static area, segment 0, allows for the direct access to interrupt service and page change routines, and other common sub-routines, while the paged segments (1 to 256) of 32K bytes may contain additional program code, database entries, printer fonts, buffer space, or any other function requiring a large amount of memory.

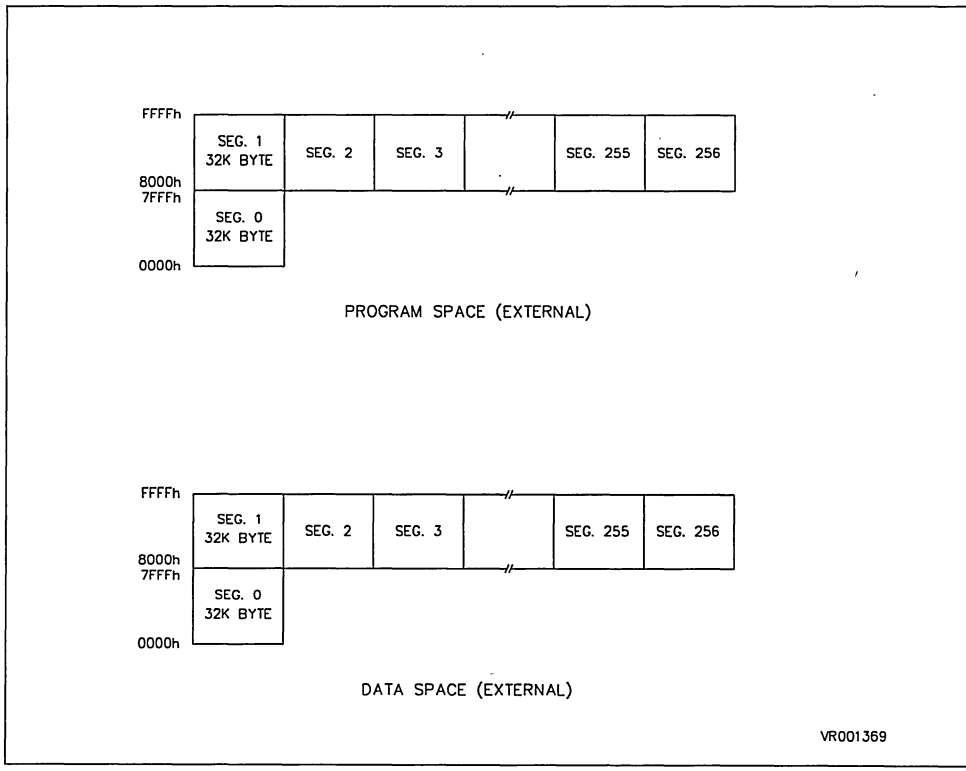
The setting of Port 2 is made during the Reset cycle, by the latched status of the signals BSH_EN1 and BSL_EN1. These control the high and low nibbles of Port 2 between Address Expansion lines and normal I/O lines as shown in Table 7.

Table 7. Port 2 Nibble Programming For Bank Switch and I/O

BSH_EN1	BSL_EN1	BS Port Nibble		BS Port Reset Value	
		High	Low	High	Value
O	O	I/O	I/O	--	--
O	I	I/O	BS	--	0FEh
I	O	I/O	BS	--	0FEh
I	I	BS	BS	0FEh	0FEh

In order to program the functions, weak pull-up/down resistors (100k ohm) on the BSH_EN1 and BSL_EN1 designated lines are used to generate the logic level latched on the rising edge of the Reset input. After this event, these lines may be used as I/O and be programmed in the normal way.

Figure 29. Bank Switch Memory Maps

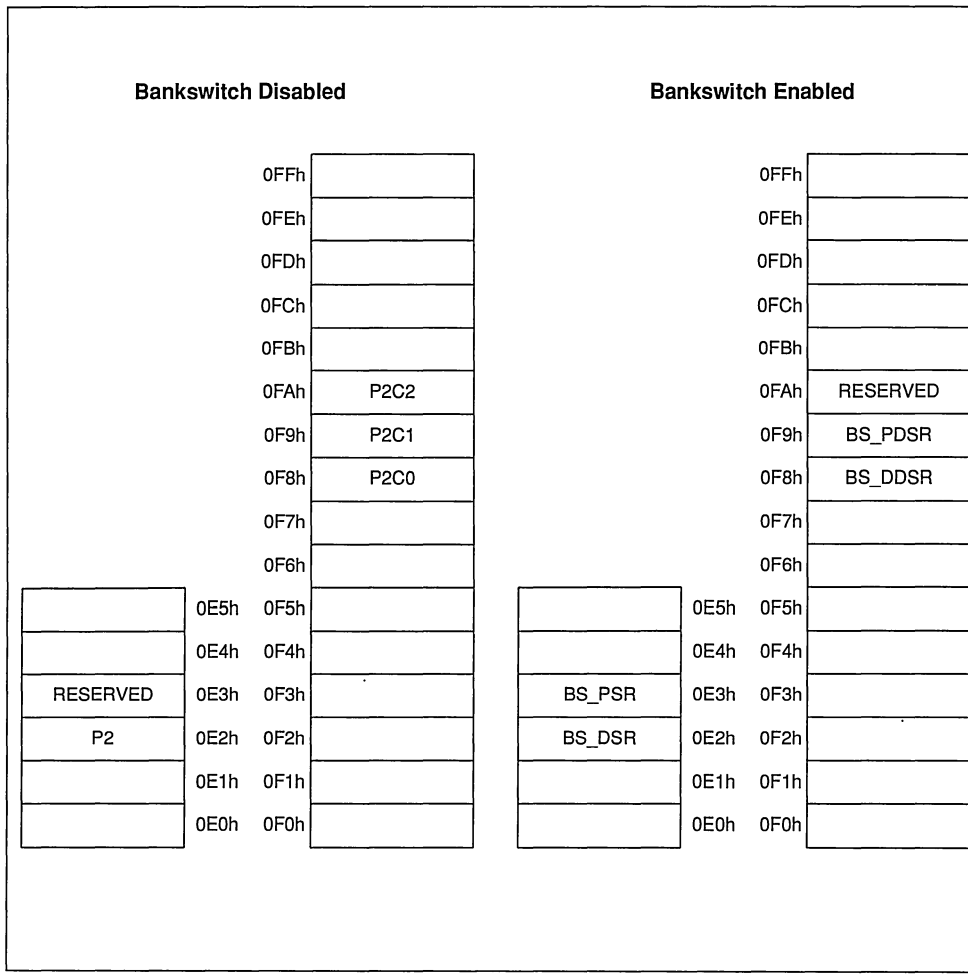


When the Address Expansion is selected, several I/O port configuration registers take an alternative function. The Port Data Registers for I/O ports 2 and 3 (Registers E2h and E3h) become the Bank Switch Data Segment Register and Bank Switch Program Segment Register respectively. The values held in these registers are output on Port 2 whenever a memory access is made to either data or program spaces with A15 high. This allows Port 2 bits to represent either extended address lines A16 to A23 or to output chip-selects to external memories. For this second option the reset value for these registers, and the value output whenever A15 is low, is 0FEh, generating the selection of a standard "startup" page automatically. Port 2 Configuration registers P2C0 and P2C1 contained in I/O Page 2 hold the User programmed values output on Port 2 for DMA cycles with addresses in the the high 32K byte of the memory for data and program spaces respectively.

Warning: The Bankswitch Program DMA register occupies the same register as Port 2 Control Register 2 (P2CR), so caution must be taken in writing to BS_PDSR when the high nibble is used as I/O and the low nibble is used for the Bankswitch output as P2C2 is used for the port configuration. The Program and Data Segment Registers are located in the direct Register file within the System Register group in order to be immediately accessible, while the DMA Segment Registers are held within an I/O page as, once programmed, they do not need constant service.

BANKSWITCH LOGIC (Continued)

Figure 30. Bank Switch Register Mapping



BANKSWITCH LOGIC (Continued)

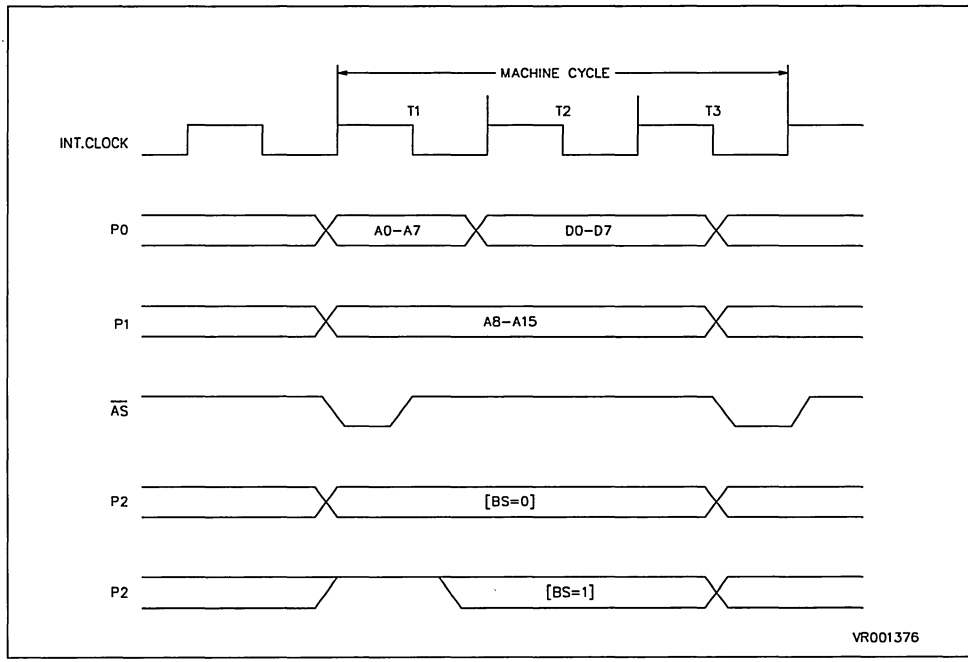
Output Timing

In order to prevent potential bus conflicts on Port 0 (Address/Data multiplexed) during the address strobe time when using the Bankswitch logic, the timing of the Bankswitch outputs may be modified by software. This is achieved by setting to "1" bit 1 of Register 0FFh in I/O page 0. This causes the Bankswitch outputs to be all high during the address strobe period. The reset condition provides normal timing and status.

The timing of the Read/Write signal may be modified as shown in the next figure by setting to "1" bit 0 of Register 0FFh in I/O page 0. This allows the use of different types of external memories. When this bit is "0" (the reset state) normal timing is generated.

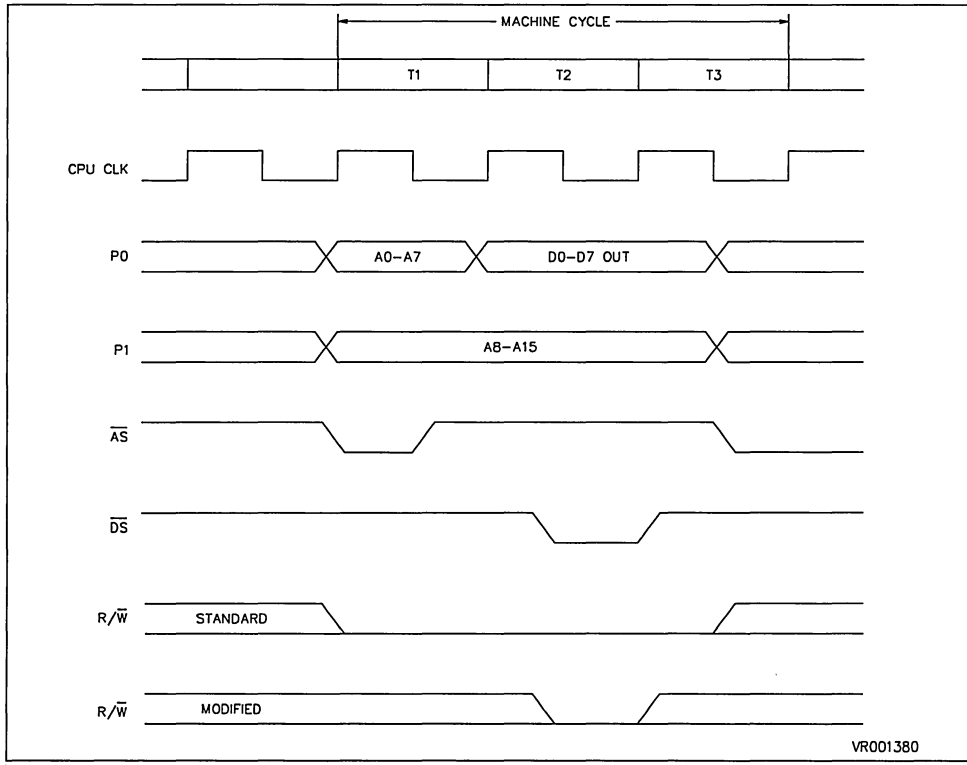
Note : The LST9 ST9 Incremental Linker supports the paging mechanism of the ST90R50 and is able to allocate program and data code into specific segments if required.

Figure 31. Bankswitch Output Timing Modification



BANKSWITCH LOGIC (Continued)

Figure 32. R/$\overline{W}$ Output Timing Modification



BUS CONTROL

Multi-processing or external program testing may be accomplished by disabling the I/O ports used for external memory addressing and the associated timing signals.

High Impedance Mode

The User may place the External Memory Interface (I/O Port 0, Port 1 and Port 6, Address Strobe, Data Strobe and Read/Write) into the high impedance state by setting the HIMP bit (MODER.0). External test equipment may then drive the memory lines for automatic test, external memory validation or programming. The ST9 will continue to execute internal programs, providing no external memory is addressed, allowing the execution of security routines without showing externally the addresses used.

Bus Request/Acknowledge

The External Memory Interface address ports and timing signals may be forced to their high impedance state by utilizing the $\overline{BUSREQ}$, Bus Request, and $\overline{BUSACK}$, Bus Acknowledge, signals available as Alternate Functions of two I/O pins. The signals, $\overline{BUSREQ}$ and $\overline{BUSACK}$, must be enabled by setting the BRQEN bit (MODER.1). Once enabled, a low level detected on the $\overline{BUSREQ}$ pin at the start of an internal machine cycle will cause the stretching of the CPUCLK, and $\overline{BUSACK}$ to go low indicating that the External Memory Interface is disabled. The $\overline{BUSREQ}$ pin is then continuously monitored, and when sampled high, the External Memory Interface pins are driven by the ST9 within two INTCLK cycles.

I/O PORTS

Summary of Function

For the ST90R50 84 pin package, only twelve pins have a Reserved function: V_{DD}(x2), V_{SS}(x2), $\overline{RESET}$, $\overline{AS}$, $\overline{DS}$, R/$\overline{W}$, OSCIN, OSCOUT, the Analog to Digital Converter Voltage references. All other pins are available as Input/Output (I/O) for the User, grouped into Ports of 8 bits. These may be programmed to be Input, Output, Bidirectional or Alternate Function (Peripheral or Memory Interface), on a bit by bit basis, at any time. When programmed as an Input the pin may be set to TTL or CMOS input threshold levels, while, when programmed as Output, Push-Pull or Open Drain configuration may be selected. The Bidirectional mode sets the pin with a weak pull-up resistor to V_{DD} or to Open Drain, allowing bidirectional communication with external logic. The Alternate Function setting is predetermined for each pin as shown in the Pin Configuration Table.

The circuitry of the I/O port allows for several ST90R50 peripheral functions to address, as Alternate Functions, the same pin, for both input and output, the User selects which peripheral function is to be active by enabling its individual Input or Output function. This multi-function I/O capability of the ST90R50 allows for easy adaptation to external circuits. The options available for each bit are summarized in Table 8.

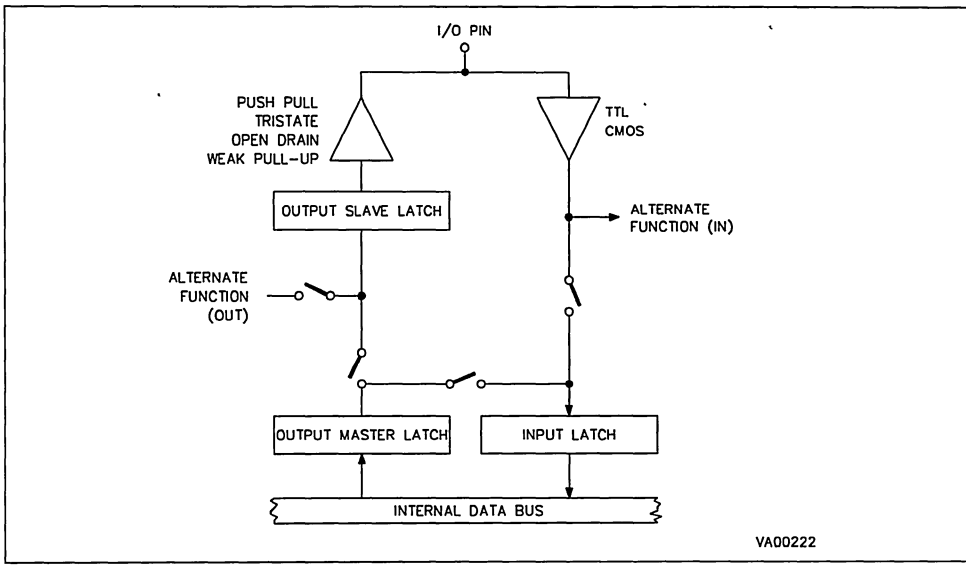
Table 8. I/O Setting Options

Input	TTL Thresholds
	CMOS Thresholds
Output	Open Drain
	Push Pull
Bidirectional	Open Drain
	Weak Pull-up
Alternate Function	Open Drain
	Push Pull

I/O Port Configuration

The configuration of each general I/O bit of the ST90R50 is set by the corresponding bits in three I/O Port control registers. These affect the status of the input and output buffers of the pin, and enable the Alternate function Outputs. Alternate Function inputs are always connected, and are used by enabling the function from within the configuration registers of the relevant peripheral function. The configuration of an I/O bit is shown in figure 33. Outputs follow a Master/Slave buffer, data is tran-

Figure 33. I/O Port Schematic



I/O PORTS (Continued)

ferred from the ST9 internal data bus at the beginning of the machine cycle, and, if enabled as output, is passed to the output latch at the end of the cycle. This synchronization allows for the Bidirectional use of the pin without potential conflicts.

Configuration Registers.

Three registers are used to allow the setting of each pin, generically PxC2R, PxC1R, PxC0R, where x relates to the 8 bit I/O port in which the bit is present. The setting of the corresponding bit in each register to achieve the desired functionality of the I/O pin is shown in Table 9.

The effect of the configuration settings of Table 9 on the I/O ports structure is shown in Figures 34 to 37.

I/O Register Map

The Data Registers which correspond to the pin status (after configuration) of I/O port 0 to 5, are found in Group E of the Register File, for immediate access at all times, while the configuration registers and the Data Registers for Additional Ports are found within I/O pages (Group F) 2, 3 and 43 (2Bh).

Table 9. Port Configuration Status Bits

PxC2n	0	1	0	1	0	1	0	1
PxC1n	0	0	1	1	0	0	1	1
PxC0n	0	0	0	0	1	1	1	1
Pxn Configuration	BID	BID	OUT	OUT	IN	IN	AF	AF
Pxn Output	WP	OD	PP	OD	HI	HI	PP	OD
Pxn Input	TTL	TTL	TTL	TTL	CMOS	TTL	TTL	TTL

Legend :
x = Port
n = Bit
BID = Bidirectional
OUT = Output
IN = Input
AF = Alternate Function
WP = Weak Pull-up
OD = Open Drain
PP = Push Pull
HI = High Impedance

Figure 34. I/O Port Input Configuration

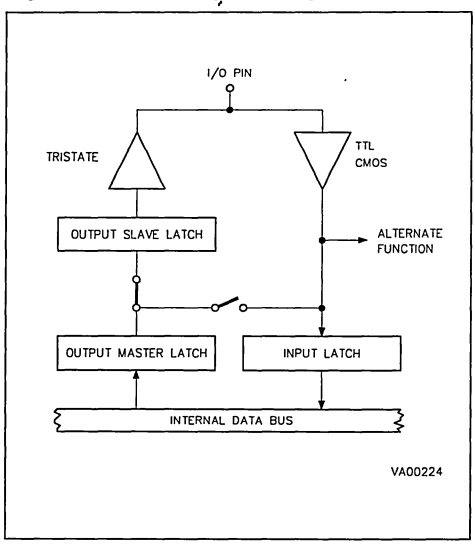
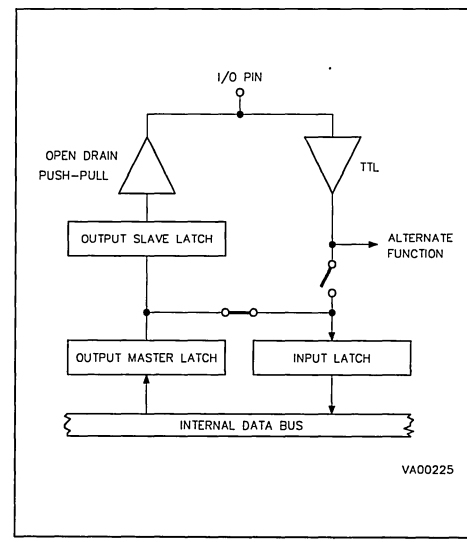


Figure 35. I/O Port Output Configuration



I/O PORTS (Continued)

Figure 36. I/O Port Bidirectional Configuration

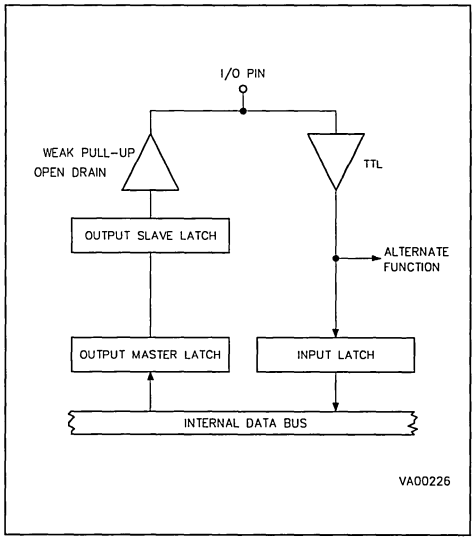


Figure 37. I/O Port Alternate Function Config.

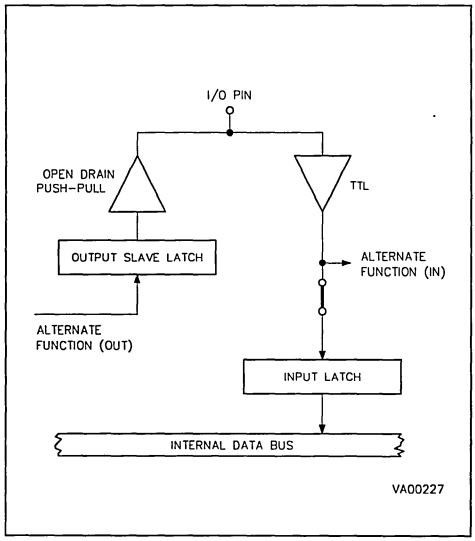


Figure 38. I/O Register Maps

GROUP E			GROUP F		PAGE		
DEC	HEX		DEC	HEX	02	03	43
			R255	RFF	RESERVED	P7D	P9D
			R254	RFE	P3C2	P7C2	P9C2
			R253	RFD	P3C1	P7C1	P9C1
			R252	RFC	P3C0	P7C0	P9C0
			R251	RFB	RESERVED	RESERVED	P8D
			R250	RFA	P2C2	RESERVED	P8C2
			R249	RF9	P2C1	RESERVED	P8C1
			R248	RF8	P2C0	RESERVED	P8C0
			R247	RF7	RESERVED	HDC5	RESERVED
			R246	RF6	P1C2	P5C2	RESERVED
R229	RE5	P5D	R245	RF5	P1C1	P5C1	RESERVED
R228	RE4	P4D	R244	RF4	P1C0	P5C0	RESERVED
R227	RE3	P3D	R243	RF3	RESERVED	RESERVED	RESERVED
R226	RE2	P2D	R242	RF2	P0C2	P4C2	RESERVED
R225	RE1	P1D	R241	RF1	P0C1	P4C1	RESERVED
R224	RE0	P0D	R240	RF0	P0C0	P4C0	RESERVED

I/O PORTS (Continued)

Handshake and DMA

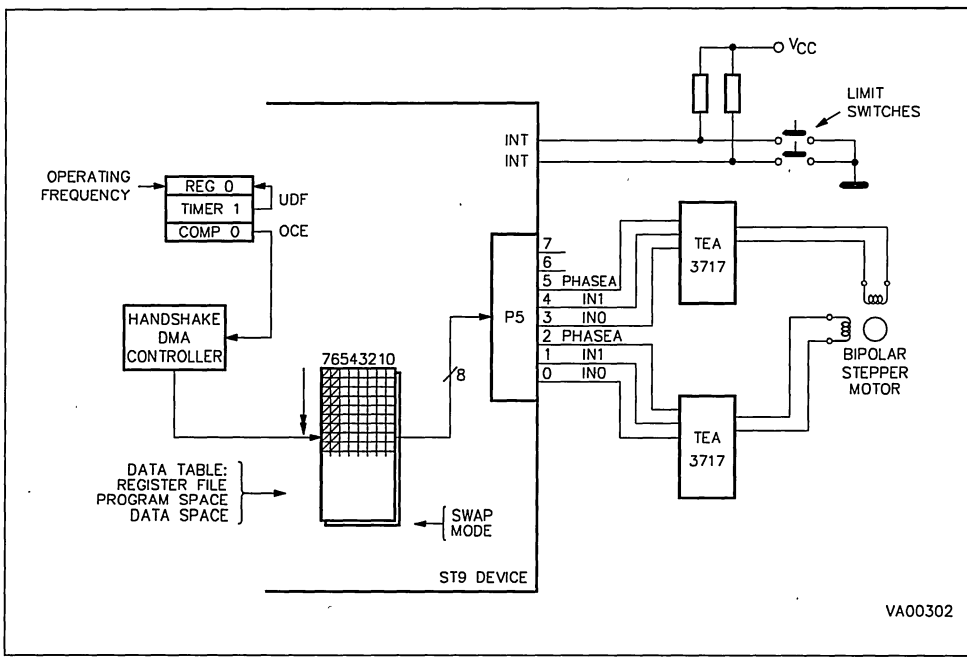
I/O Ports 4 and 5 of the ST90R50 are able to support a parallel interface with handshake capability. This allows one, two or four wire interconnecting handshake signals and facilitates very fast parallel transfer of data for input and output, or for the interconnection of peripheral devices requiring strobe signals for synchronization. Table 10 shows the available options for input and output status and strobe signals available as Alternate Functions of I/O port bits (see Pin Configuration). The Handshake configuration is set within the Handshake Control Register (HDC*n*R) for the relevant I/O port *n*.

Data transfer through a parallel I/O port with handshake can also be triggered through a DMA channel. Timing is generated by the ST90R50 TIMER ON-CHIP EVENT strobe signal (see the TIMER section for information on generating these signals), which causes the programmed transfer of data to or from the memory source which can be Register File, Program space memory or Data space memory. An example of application of this technique is shown in figure 39, a complex stepper motor timing sequence automatically being transferred from a table in the Register File (or memory spaces) to the stepper motor drivers. After initialization, this operation is transparent until the task (complex microstepping) is completed.

Table 10. Handshake Control Signal Options

Mode	Handshake Lines	Names
Input to Port	1	WRRDY
	2	$\overline{\text{WRSTB}}$ WRRDY
Output from Port	1	RDRDY
	2	$\overline{\text{RDSTB}}$ RDRDY
Bidirectional	4	$\overline{\text{WRSTB}}$ WRRDY $\overline{\text{RDSTB}}$ RDRDY

Figure 39. Handshake + DMA Used for Stepper Motor Driving



TIMER/WATCHDOG

A 16 bit down-counter, complete with 8 bit prescaler, is integrated into the ST90R50 core. This is able to operate both as a general purpose timer with associated input and output pins for timing functions, and also as a Watchdog Timer offering a security against possible processor malfunctions due to external events.

Timer Modes

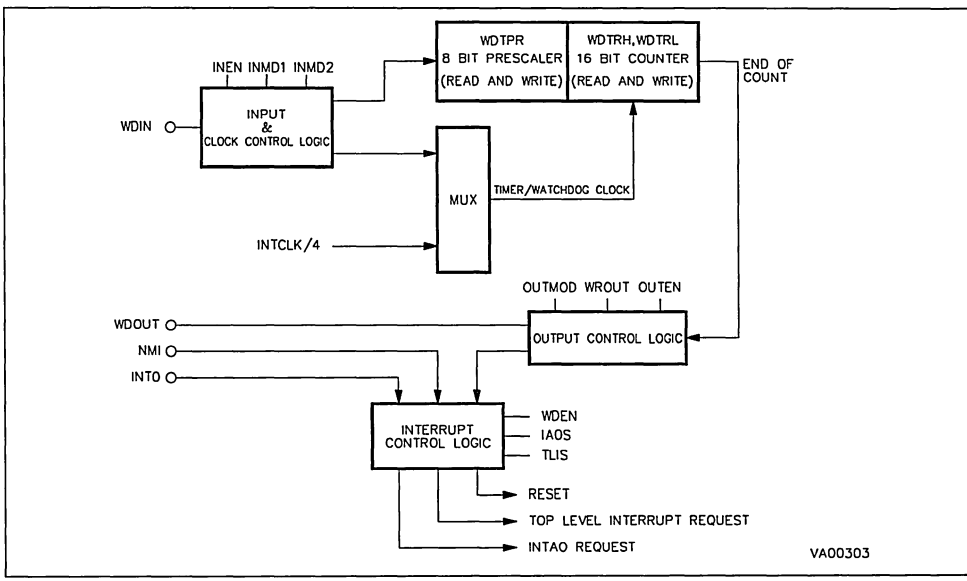
When operating as a Timer, with a timing resolution from 333ns to 5.59s (INTCLK = 12MHz), an input pin (WDIN) and output pin (WDOUT) may be selected as the Alternate Functions of two I/O pins. When WDIN is enabled by the User by setting INEN high (WDTCR.3) and the Alternate Function is set, 4 operating modes are available: The WDIN input may be programmed to act as an event counter input, with high to low transitions causing the counter to decrement (the time duration between the falling edges of the input clock must be at least 333ns, allowing a maximum input frequency of 3MHz). It may also be used for pulse width measurement by being selected as a counter clock gate signal (prescaler to the counter being driven by INTCLK/4), counting being enabled when WDIN is at a high level. Trigger and Re-trigger modes cause a reload of the timer User preset values (providing STSP, WDTCR.7 is active) for a high to low transition on WDIN at any time (Re-trigger mode) or when the counter is at the end of count (Trigger mode). The counter decrements at a rate driven by INTCLK/4.

The WDOUT pin, when set as the Alternate Function, is enabled by OUTEN high (WDTCR.0), and may either toggle the state of the I/O bit (frequency generation, OUTMD = "0", WDTCR.2) or pass the state of the WROUT bit to the output allowing PWM generation (OUTMD = "1") at the end of count (timer value = 0) condition.

Watchdog Mode

The timer functions may be disabled, and the Timer configured for a Watchdog operation by re-setting WDEN (WCR.6) to zero. Once the Watchdog has been selected it CANNOT be set back into the standard timer mode until the next Hardware Reset cycle. The User should set the watchdog timer prescaler and timer reload value before enabling the Watchdog mode. The Watchdog Timer must then be retriggered, causing the reloading of the timer value, by the operation of writing of the byte sequence 0AAh, 055h to the WDTLR register. If this is not done before the Watchdog counts to zero, the Watchdog Timeout condition occurs. This causes a Hardware Reset of the ST90R50. The Watchdog reset signal is not output on the external Reset pin.

Figure 40. Timer/Watchdog Block Diagram



TIMER/WATCHDOG (Continued)

Timer/Watchdog Interrupts

The Timer/Watchdog may provide several levels of interrupts selectable by the User. The Timer mode offers two interrupt sources, triggered on the timer value reaching 0, either a prioritized level (by taking the Interrupt priority channel from the External Interrupt INTA0) or by a top level, non-maskable interrupt (taking the external NMI input channel). The interrupt channels are multiplexed from the alternative source according to the status of the IAOS (EIVR.1) and TLIS (EIVR.2) bits as shown in figure 42. Please refer to the ST9 Technical Manual for further details on changing the interrupt sources of the Timer/Watchdog. When the Watchdog mode is set (WDEN = "0"), the timer value equal to 0 event generates a Hardware reset of the ST90R50. The Timer/Watchdog control registers are located within Page 0 of the Paged I/O register group.

Figure 42. Timer/Watchdog Interrupt Sources

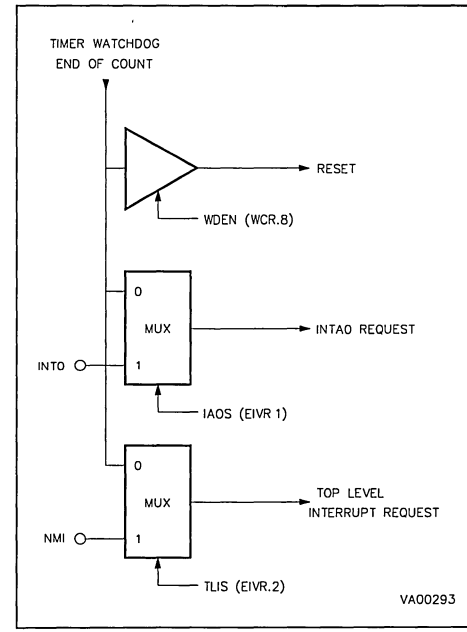
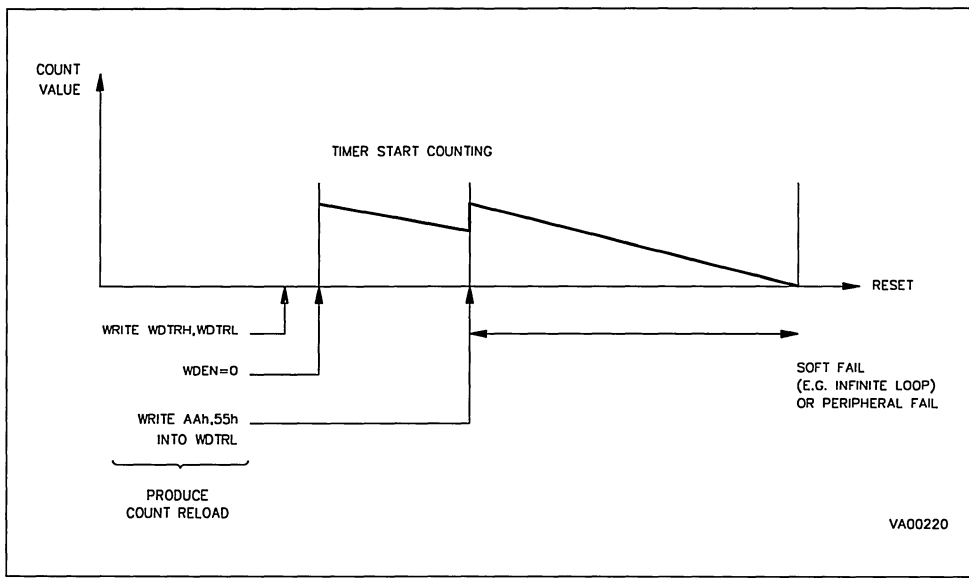


Figure 41. Timer/Watchdog in Watchdog Mode



MULTIFUNCTION TIMER

The ST90R50 includes three identical 16 bit Multifunction Timers (MFT) in addition to the TIMER/WATCHDOG. The following description applies to Timer 0, Timer 1 and Timer 3.

Each timer is a 16 bit Up/Down counter, driven by the output of an 8 bit prescaler which may be driven by INTCLK/3 (giving a minimum timing resolution of 250ns at INTCLK = 12 MHz) or by an external source. This timer is supported by two 16 bit Comparison Registers for generating timed functions and two 16 bit Capture/Load Registers for timing and variable timebase functions. These features coupled with 2 input pins (TxINA and TxINB) and 2 output pins (TxOUTA and TxOUTB, where x = 0 or 1), available as Alternate Functions, giving the timer 13 operating modes for virtually all required timing functions.

MFT Operating Modes

The operating modes are selected by the programming of the Timer Control Register (TCR Timer x) and the Timer Mode Register (TMR) as follows:

One-Shot Mode. The counter stops at the End Of Count Condition (up or down count).

Continuous Mode. At End Of Count the timer is reloaded from a Load Register.

Trigger Mode. A Trigger causes reload from a load register only if the Timer is at End of Count.

RETrigger Mode. A Trigger causes reload from a load register at any time.

Gate Mode. Counting is performed only when the external gate input (TxINA or TxINB) is active (logical 0).

Capture Mode. A Trigger causes the timer value to be latched into the selected Capture register.

Up/Down Mode. A Trigger causes a count up or down, or a change in counting direction.

Free-Running Mode. Up or Down counting is performed to the full range with no action at End of Count. This is used in Bicapture and Capture Modes.

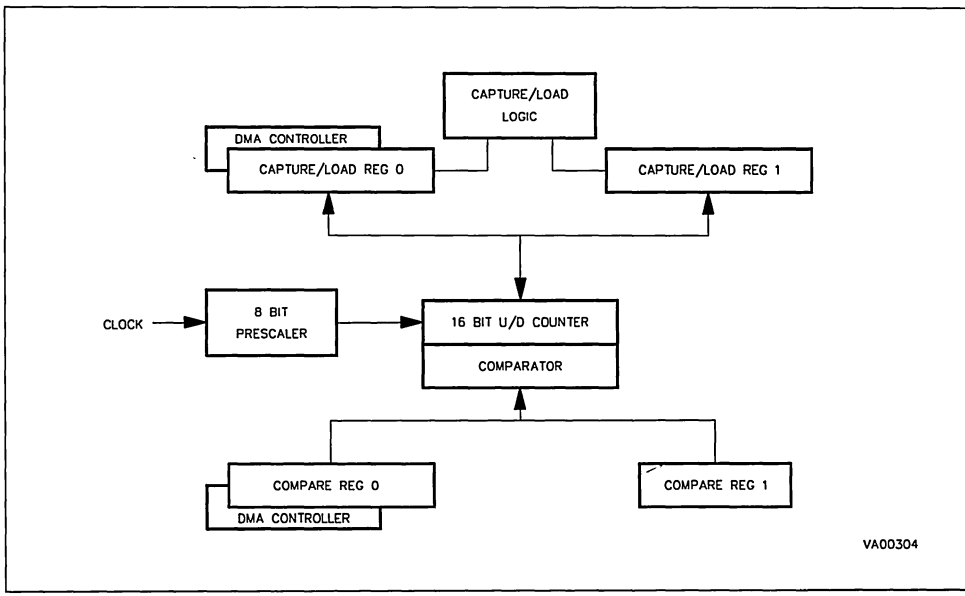
Monitor Mode. One Capture register follows the contents of the timer.

Autoclear Mode. The timer is reset to 0000h or FFFFh (up or down count respectively) on a trigger. This gives delta time measurement or free running with a modulo of less than 2^{16}.

Biload Mode. The counter is reloaded on an End Of Count condition alternately from the two Load Registers. (PWM output).

BICapture Mode. A Trigger causes the current timer value to be transferred alternately to the two Capture registers. (Pulse width measurement).

Figure 43. Multifunction Timer Block Diagram



MULTIFUNCTION TIMER (Continued)

Parallel Mode. The prescaler output of Timer 0 is internally connected to the input of the prescaler of Timer 1, if this is then set to 00h (= divide by 1), then the two timers may be run in parallel.

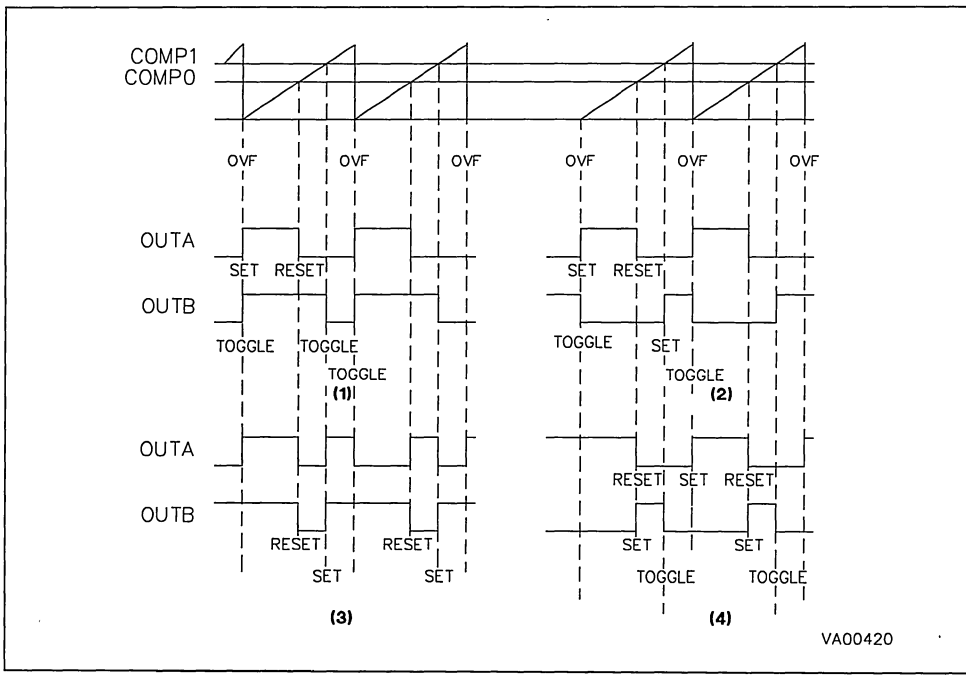
The trigger events may be either caused by software, or an action on the two input pins which may be programmed to respond to rising, falling or both edges of the input. The input modes are selected in the Input Control Register (ICR) as shown in Table 11. This includes the Autodiscriminator mode, which causes the timer to count up or down depending on the phase between the two input edges, such as the signals generated by optical encoders.

The two output pins (available as Alternate Functions) may be programmed through the Output Control Registers OACR and OBCR to be modified (Set, Reset, Toggle or No Operation) on each of Overflow/Underflow (OVF/UNF), Compare on CMP0 valid (CM0), or Compare on CMP1 (COMP1) valid events. This allows repetitive signals such as PWM drive to be output with minimum CPU overhead. Fig 44 shows some typical waveforms available from these signals.

Table 11. Input Pin Function Settings

Input Control Register IN3-IN0 bits	TxINA Input Function	TxINB Input Function
0000	I/O	I/O
0001	I/O	Trigger
0010	Gate	I/O
0011	Gate	Trigger
0100	I/O	Ext.clock
0101	Trigger	I/O
0110	Gate	Ext.clock
0111	Trigger	Trigger
1000	Clock Up	Clock Down
1001	Up/Down	Ext.clock
1010	Trigger Up	Trigger Down
1011	Up/Down	I/O
1100	Autodiscr.	Autodiscr.
1101	Trigger	Ext.clock
1110	Ext.clock	Trigger
1111	Trigger	Gate

Figure 44. Example Output Waveforms



MULTIFUNCTION TIMER (Continued)

The Overflow/Underflow event and the Compare 0 event may also be programmed to give On-chip Event timing signals to trigger other peripheral operations on the ST90R50. These are as shown in Table 12.

Table 12. ST90R50 On-Chip Event Settings

MFT0	Handshake Trigger Port 4
MFT1	Handshake Trigger Port 5
MFT3	A/D Conversion Trigger

The TxOUTA and TxINA lines for each timer may be connected internally, by setting of the SCx bits of the I/O Connection Register (IOCR).

The Multifunction Timers are enabled for counting by the Counter Enable bit (CEN, TCR.7) of the respective timer unit. When CEN is low, both prescaler and timer are halted. CEN is logically ANDed with the Global Counter Enable bit (GCEN, CICR.7), so that all timers may be started in synchronism, i.e. when the timers are set into Parallel mode, this allows initialization of the Timers before triggering at the same instant.

MFT Interrupts

Each Multifunction Timer can generate interrupt requests from 5 different interrupt sources which are grouped into 3 independent groups. The Interrupt Vector has the source of the interrupt group encoded by hardware into the least significant 3 bits of the vector. This allows the programming of the base address to an 8 byte block within the interrupt vector area of the Program Space. The groups and respective addresses are shown in Table 13.

Table 13. MFT Interrupt Vectors

Interrupt Source	Vector Address
COMP0 COMP1	xxxx x110
CAPT0 CAPT1	xxxx x100
Overflow/Underflow	xxxx x000

Each source may be independently masked, in addition all Timer interrupts may be disabled by the Global Timer Interrupt enable (GTIEN, IDMR.7) control bit. If a Timer interrupt on Compare 0 or Capture 0 does not have its corresponding pending bit reset before the next interrupt, then an overrun condition occurs. This condition is flagged in two dedicated overrun bits in the Timer FLAGS register.

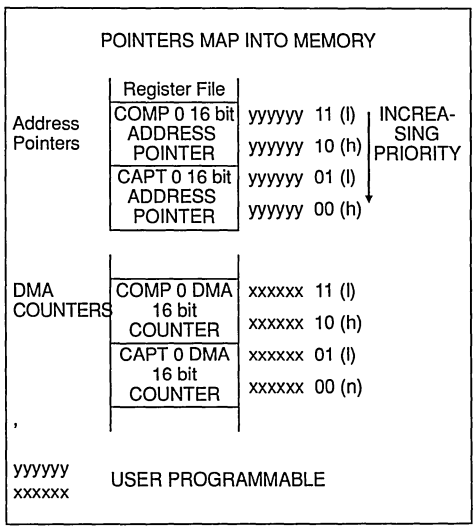
MFT DMA Channels

Two independent DMA channels are present within each MFT, associated to the Compare 0 and Capture 0 sources. This allows 16 bit DMA transactions from Register File/Memory to COMP0 registers, and from CAPT0 registers to Register File/Memory. The DMA channels allow the capture of external event timings in memory allowing off-line analysis, and creating of variable pulse width signal trains, as required by the drive of Triacs in certain modes.

The two interrupt mask sources are independently masked by two DMA mask bits, mapped in the IDMR register. The End of Block (EOB) procedures are as described in the INTERRUPT/DMA section.

The DMA counter and address pointer registers share the most significant User-programmable 6 bits for both DMA channels (COMP 0 and CAPT 0), thus the mapping of the counter and address registers use automatic offsets from the base address. The actual mapping changes dependent on whether the Register File or Memory is addressed for the transfer. The offsets are shown in Table 14.

Table 14-1. MFT DMA Address and Counter Registers for Memory DMA Transfers



MULTIFUNCTION TIMER (Continued)

Table 14-2. MFT DMA Address and Counter Registers for Register File DMA Transfers

POINTERS FOR REGISTER FILE DMA			
8 Bit COUNTER	xxxxxx	11	COMPARE 0
8 bit ADDR. POINTER	xxxxxx	10	
8 bit COUNTER	xxxxxx	01	CAPTURE 0
8 bit ADDR. POINTER	xxxxxx	00	
xxxxxx	USER PROGRAMMABLE		

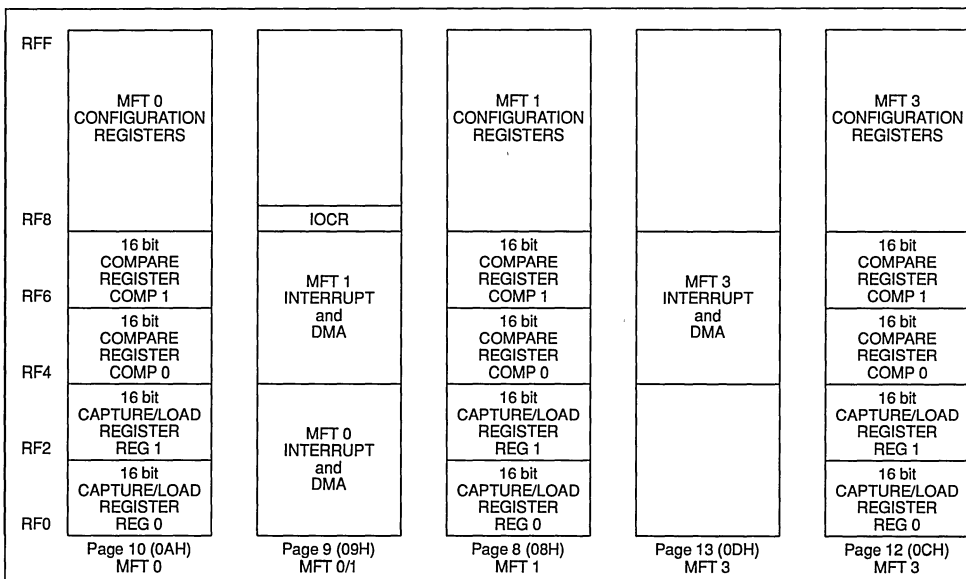
After the transfer of the complete block of data to/from the MFT, the count registers reach the zero value and an end of block interrupt occurs so that the ST9 may process the new data. In many cases, the time taken to reload the data tables and to re-trigger the DMA action causes speed limitations, especially in those applications requiring a continuous high speed data flow, because of the time consumed by the restore routine. An additional DMA function, the SWAP mode, overcomes this limitation. This is enabled by the setting of the SWEN (IDCR.3) bit. This causes hardware generated signals to replace the User address bit 2 of both the address and counter pointers. The address and counter registers are thus duplicated at an offset of 4 registers. At the End Of Block condition, the EOB interrupt is generated to signal the end of DMA, and the state of pointer address bit 2 toggles state automatically and the new address and count values are used. Thus the ST9 can safely process the previous block of data while the new block is being transferred. This will continue until the SWAP mode is disabled.

A software protection scheme is implemented to prevent non-updated pointer registers from being used if a second EOB interrupt arrives during the servicing of the first. This mechanism locks the state of the DMA mask bit to prevent further transfers from taking place. The User should check for this condition in the EOB routine to ensure that all the DMA transfers are properly serviced.

The control Registers of each MFT occupy 20 registers within the I/O paged area. These are mapped as shown in Figure 45.

In addition the MFT is able to trigger byte DMA transfers in both directions through an I/O port with Handshake (see I/O Handshake and DMA).

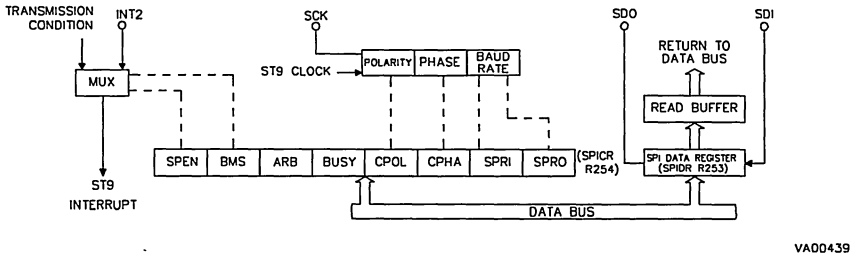
Figure 45. Multifunction Timer Page Maps



SERIAL PERIPHERAL INTERFACE (SPI)

The Serial Peripheral Interface (SPI) is integrated into the Core module of the ST9 and provides a general purpose shift register based peripheral allowing synchronous serial I/O, with special modes allowing compatibility with I^2C-bus and IM-bus Communication standards in addition to the standard serial bus protocol. The SPI uses 3 lines comprising Serial Data Out (SDO), Serial Data In (SDI) and the Synchronous Serial Clock (SCK) which are available as Alternate Functions of I/O pins. Additional I/O pins may act as device selects or IM-bus address ident signals. The functional diagram of the SPI is shown in figure 46.

Figure 46. SPI Functional Diagram



The SPI, when enabled (SPEN, SPICR.7, high), receives input data from the ST9 internal data bus into the SPIDR, and originates the SCK to shift the data serially through SDO (Most Significant bit first), to the slave device which responds by sending data to the master device via the SDI pin. This implies full duplex transmission with both data-out and data-in synchronized with the same clock signal. Thus the byte transmitted is replaced by the byte received, eliminating the need to separate "Tx Empty" and "Rx full" status bits. After the 8 clock cycles have been concluded, the received data in SPIDR is parallel transferred to the read buffer and data becomes available for the ST90R50 during the next read cycle of SPIDR. The BUSY bit (SPICR.4) is set when transmission is in progress, this allows the User to monitor the status of the SPI by polling of this bit.

The SPI can operate only in master mode, i.e. the clock is always generated by the ST90R50, however the SCK polarity and phase can be programmed to suit all peripheral requirements (figure 47). This, together with the 4 programmable bit rates (divided from the INTCLK, Table 15), provide the large flexibility in handling different protocols.

SERIAL PERIPHERAL INTERFACE (Continued)

Figure 47. SPI Data and Clock Timing

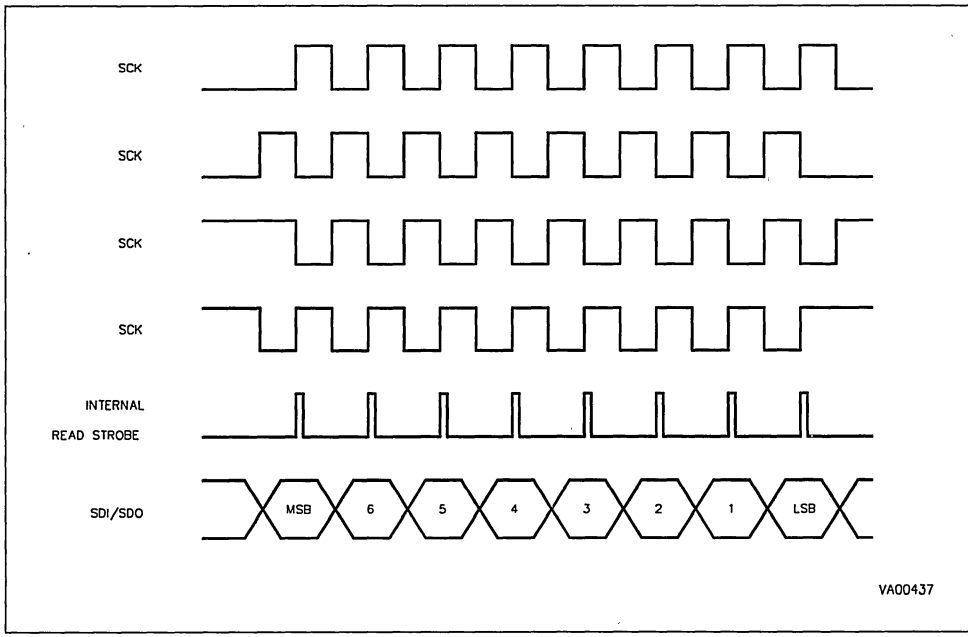


Table 15. SPI Rate Selection

SPR1	SPR0	Clock Divider	SCK Frequency (INTCLK = 12MHz)
0	0	8	1500KHz (T = 0.67µs)
0	1	16	750KHz (T = 1.33µs)
1	0	12	93.50KHz (T = 10.66µs)
1	1	256	46.87KHz (T = 21.33µs)

I^2C-bus COMPATIBILITY

The SPI includes additional circuitry to enable the use of external I^2C-bus peripherals. The I^2C-bus mode is a 2 wire bus while the SPI operates with 3 wires, however wire-ANDing SDO and SDI gives the required signalling, while setting the BMS bit causes the enabling of the special I^2C-bus features: Clock Slowdown by external devices and Arbitration Lost detection. This mode also affects the Interrupt sources as shown in the next section.

SPI Interrupts

The SPI, when enabled, uses the INT2 external interrupt channel source, using the priority selected for INT2 within the External Interrupt Priority registers. The INT2 mask bit should be set and INT2 pending bit reset before enabling the SPI through SPEN. The BMS (SPICR.6) and SPEN bits select the SPI internal interrupt source as shown in Table 6.

Table 16. SPI Interrupt Sources

SPEN	BMS	Interrupt Source
0	0	External channel INT2
0	1	S-BUS/I^2C start or stop condition
1	X	End of one byte transmission

SPI Registers

The two registers controlling the SPI are located in I/O page 0, the Data Register, SPIDR, at R253 and the control register, SPICR, at R254.

SERIAL COMMUNICATIONS INTERFACE

Function

The two Serial Communications Interfaces (SCIs) of the ST90R50 offers a means of full-duplex serial data transfer to a wide range of external equipment. Each has a fully programmable character format control for asynchronous and byte synchronous serial I/O, an integral Baud Rate Generator, giving a maximum baud rate of 375K Baud in Asynchronous mode (Internal Clock), and two DMA channels for transparent transmission and reception of characters. Support is also present in hardware for Line Break Detection and generation, character search, network interfacing with 9th bit Address logic, and Local Loop Back and Auto echo modes for Self- Test. The control registers for an SCI exist within one I/O page within the I/O page group.

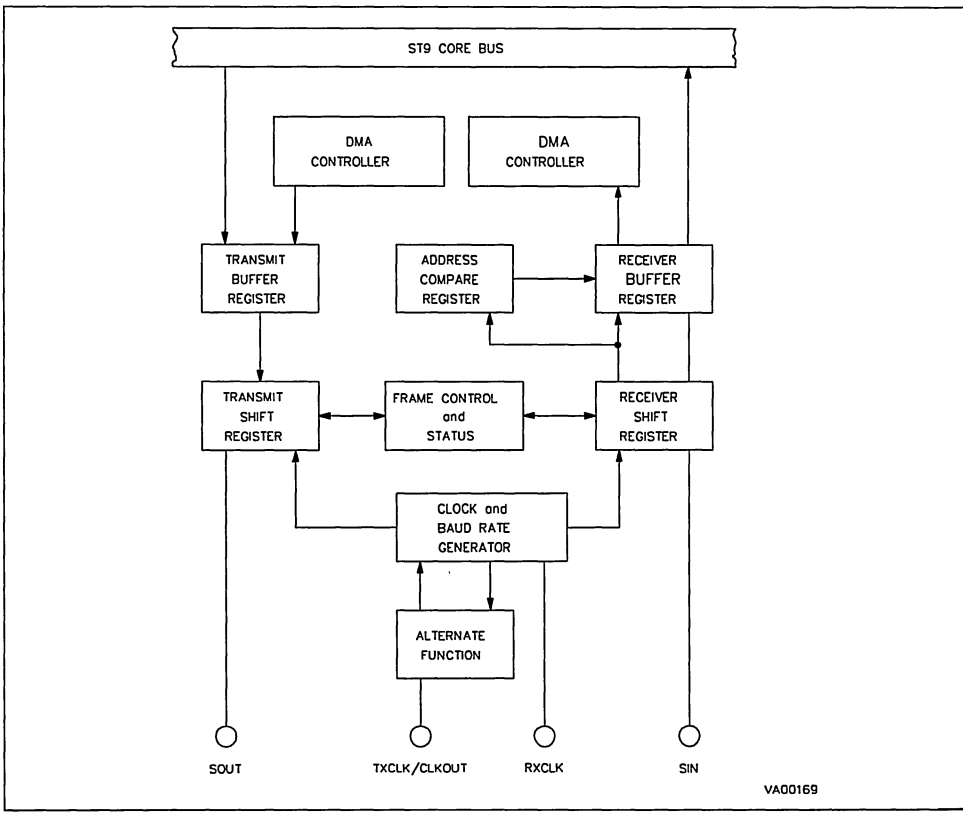
Character Formats

When used for asynchronous character transmission and reception, the character format may be changed (through the Character Control Register CHCR) to suit external equipment requirements. This is summarized in figure 49.

The baud rate clock for asynchronous mode should be set to the ÷16 Mode and the frequency of the clock input (from an external source or the internal baud-rate generator output) set to suit this.

This format control is also available for the byte synchronous mode (Clock divider set to ÷1), when the data and clock are output in synchronism, the data being sampled once per clock period (figure

Figure 48. SCI Functional Block Diagram



SERIAL COMMUNICATION INTERFACE
(Continued)

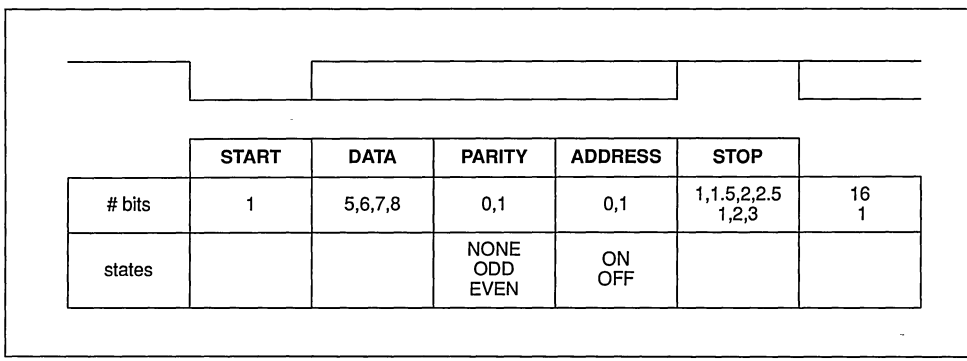
50). For a second synchronous mode, CLKOUT is activated only for the data section of the word (figure 51) on serial data output, and input data is latched on the rising edge of the external synchronised clock input on the RXCLK pin. This mode may be used to access external synchronous peripherals.

The Address bit/D9 is optional and may be added to any word format, it is commonly used in network or machine control applications. When enabled (AB, CHCR.4 = "1"), an address or ninth data bit can be added to a transmitted word by setting the Set Address bit (SA, IDPR.5). This is then appended to the next word entered into the (empty) Transmitter Buffer Register and then cleared by hardware. On character input an Address Bit set can indicate that the data preceding the bit is an address which may be compared in hardware with the value in the Address Compare Register (ACR) to generate an Address Match interrupt when equal.

The Address bit and Address Comparison Register can also be combined to generate an Address Interrupt in 4 modes to suit different protocols, based upon the status of the Address Mode Enable bit (AMEN, IDPR.7) and the Address Mode bit (AM, CHCR.7) as shown in Table 17.

The character match Address Interrupt mode may be used as a powerful character search mode, giving an interrupt on reception of a predetermined

Figure 49. SCI Character Format



	START	DATA	PARITY	ADDRESS	STOP	
# bits	1	5,6,7,8	0,1	0,1	1,1.5,2,2.5 1,2,3	16 1
states			NONE ODD EVEN	ON OFF		

Figure 50. Byte Synchronous Output

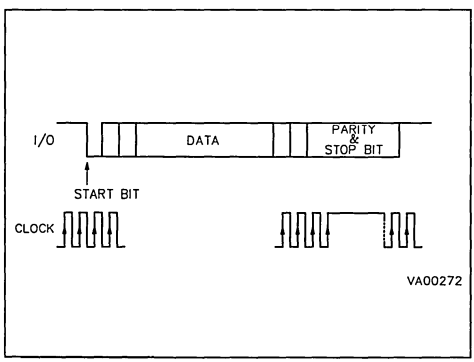
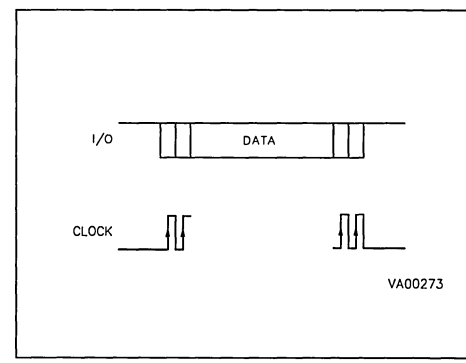


Figure 51. Serial Expansion Mode



SERIAL COMMUNICATION INTERFACE (Continued)

Table 17. Address Interrupt Modes

If 9th Data Bit = 1
If Character Match
If Character Match and 9th Data Bit = 1
If Character Match on Word Immediately Following Break

character e.g. Carriage Return or End of Block codes.

The Line Break condition is fully supported for both transmission and detection. Line Break is sent by setting the SET_BREAK bit (SB, IDPR.6). This causes the transmitter output to be held low (after all buffered data has been transmitted) for a minimum of one complete word length and until the SB bit is Reset.

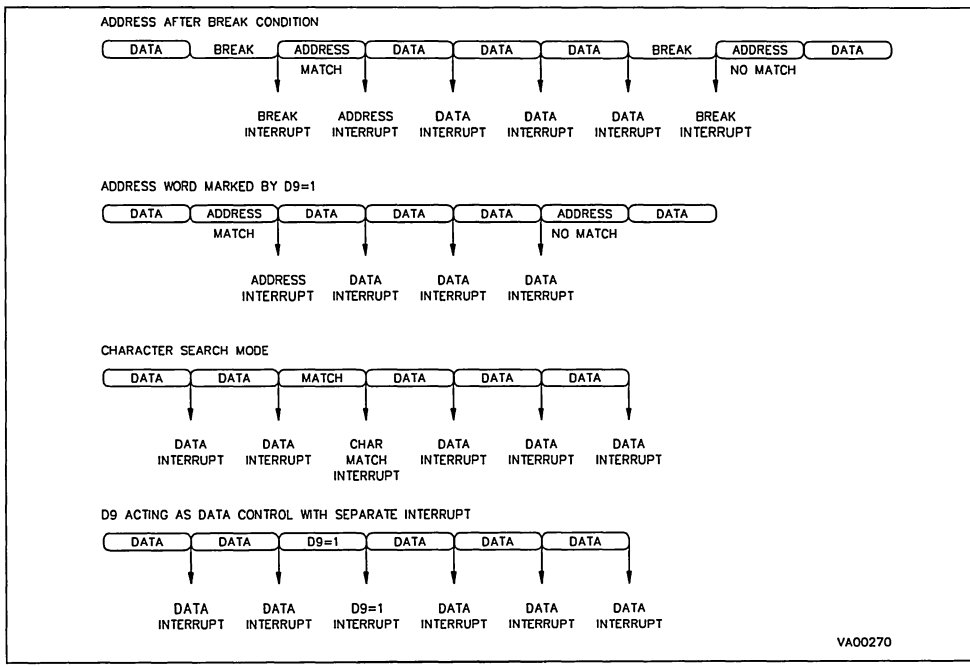
SCI Interrupts

Each SCI is able to generate interrupts from multiple sources. Receive interrupts include data pending, receive errors (overrun, framing and parity), address or break pending and transmit interrupts are software selectable for either the Transmit Holding Register Empty (HSN, IMR.7 = "1") or for the Transmit Shift Register Empty (HSN = "0"). Interrupt sources are indicated by the Interrupt pending bits, shown in Table 18. These bits

Table 18. SCI Interrupt Vector

Interrupt Source	Vector Address
Transmitter Buffer or Shift Register Empty/Transmit DMA end of Block	xxx x110
Received Read/ Receive DMA end of Block	xxxx x100
Break Detector Address Word Match	xxxx x001
Receiver Error	xxxx x000

Figure 52. SCI Interrupt Typical Usage



SERIAL COMMUNICATION INTERFACE
(Continued)

should be reset by the User during the Interrupt Service routine.

When DMA is active the Receive Data Pending bit (RXDP, ISR.2), and the Transmit status bit interrupt sources are replaced by the DMA End Of Block Interrupt sources for transmit and receive, respectively.

Typical Usage of the Interrupts provided by the SCI are show in figure 52.

Table 19. SCI Interrupt Internal Priority

Receive DMA Request	Highest Priority
Transmit DMA Request	
Receive Interrupt	
Transmit Interrupt	Lowest Priority

The SCI interrupts have an internal priority structure (Table 19) in order to resolve simultaneous events.

The four major levels of interrupt are encoded in hardware to provide two bits of the interrupt vector register, allowing the position of the block of pointer vectors to be resolved to a block size of 8 bytes.

SCI DMA

Two DMA channels are associated with each SCI, for transmit and for receive. These follow the register scheme as described in the DMA Section. It should be noted that, after initializing the DMA counter and pointer registers and enabling DMA, data transmission is triggered by a character written into the Transmit Holding register. The DMA End Of Block Interrupts generated on completion of the DMA transfer take the place of the normal transmit and receive character interrupt vectors.

SCI Clock Generation

The communication bit frequency of the SCI transmitter and receiver sections can be provided from the integral Baud Rate Generator (allowing a maximum asynchronous bit rate of 350k Baud) or from external sources (maximum bit rate 175k Baud). This clock is divided by 16 for asynchronous mode (CD, CCR.3, = "0"), or divided by 1 for synchronous modes (CD = "1").

External Clock Sources.

The External Clock input pin TXCLK may be programmed in Alternate function by bits TXCLK (CCR.7) and OCLK (CCR.6) to be: the transmit clock input (respecting the ÷16 and ÷1 timing requirements), to act as the output of the Baud Rate Generator (allowing an external divider circuit to provide the receive clock for split rate transmit and receive e.g. 1200/75 baud), or to be CLKOUT, the clock output for the synchronous mode. Receive clock input via RXCLK Alternate function is enabled by the XRX bit CCR.5, this input should be set according to the setting of the CD bit.

Baud Rate Generator.

The integral Baud Rate Generator is a 16 bit divide by n circuit of the Internal Clock INTCLK. Thus INTCLK should be chosen to provide a suitable frequency for division by the Baud Rate Generator to give the required transmit and receive bit rates. Suitable INTCLK frequencies and the divider values for standard Baud rates are shown in Table 20.

The act of writing to either of the two registers comprising the 16 bit divider causes a reset of the SCI, allowing initialization of the SCI settings before the writing of the other Baud Rate Generator register.

Self Test

Testing of the communications channel may be performed using the facilities of the SCI. Auto Echo mode (SCI SOUT disconnected, SIN pin internally connected to SOUT pin) and Loopback mode (SCI transmitter and receiver sections disconnected

SERIAL COMMUNICATION INTERFACE (Continued)

Table 20. SCI Baud Rate Generator Divider Values

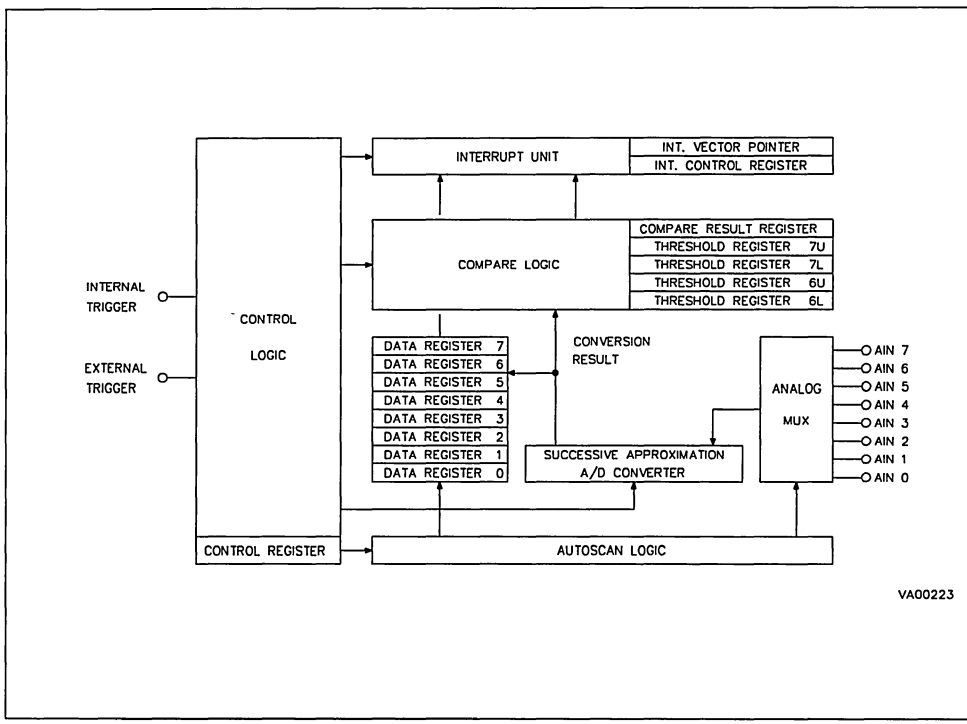
INTCLK: 7680.000 KHz							
Baud Rate	Clock Factor	Desired Freq (kHz)	Divisor		Actual Baud Rate	Actual Freq (kHz)	Deviation
			Dec	Hex			
50.00	16 X	0.80000	9600	2580	50.00	0.80000	0.0000%
75.00	16 X	1.20000	6400	1900	75.00	1.20000	0.0000%
110.00	16 X	1.76000	4364	110C	109.99	1.75985	0.0083%
300.00	16 X	4.80000	1600	0640	300.00	4.80000	0.0000%
600.00	16 X	9.60000	800	0320	600.00	9.60000	0.0000%
1200.00	16 X	19.20000	400	0190	1200.00	19.20000	0.0000%
2400.00	16 X	38.40000	200	00C8	2400.00	38.40000	0.0000%
4800.00	16 X	76.80000	100	0064	4800.00	76.80000	0.0000%
9600.00	16 X	153.60000	50	0032	9600.00	153.60000	0.0000%
19200.00	16 X	307.20000	25	0019	19200.00	307.20000	0.0000%
38400.00	16 X	614.40000	13	000D	36923.08	590.76923	3.8462%
76800.00	16 X	1228.80000	6	0006	80000.00	1280.00000	4.1667%
INTCLK: 11059.20 KHz							
Baud Rate	Clock Factor	Desired Freq (kHz)	Divisor		Actual Baud Rate	Actual Freq (kHz)	Deviation
			Dec	Hex			
50.00	16 X	0.80000	13824	3600	50.00	0.80000	0.0000%
75.00	16 X	1.20000	9216	2400	75.00	1.20000	0.0000%
110.00	16 X	1.76000	6284	188C	109.99	1.75990	0.0058%
300.00	16 X	4.80000	2304	0900	300.00	4.80000	0.0000%
600.00	16 X	9.60000	1152	0480	600.00	9.60000	0.0000%
1200.00	16 X	19.20000	576	0240	1200.00	19.20000	0.0000%
2400.00	16 X	38.40000	288	0120	2400.00	38.40000	0.0000%
4800.00	16 X	76.80000	144	0090	4800.00	76.80000	0.0000%
9600.00	16 X	153.60000	72	0048	9600.00	153.60000	0.0000%
19200.00	16 X	307.20000	36	0024	19200.00	307.20000	0.0000%
38400.00	16 X	614.40000	18	0012	38400.00	614.40000	0.0000%
76800.00	16 X	1228.80000	9	0009	76800.00	1228.80000	0.0000%

from SOUT and SIN pins and directly connected internally) may be used individually or together.

ANALOG TO DIGITAL CONVERTER

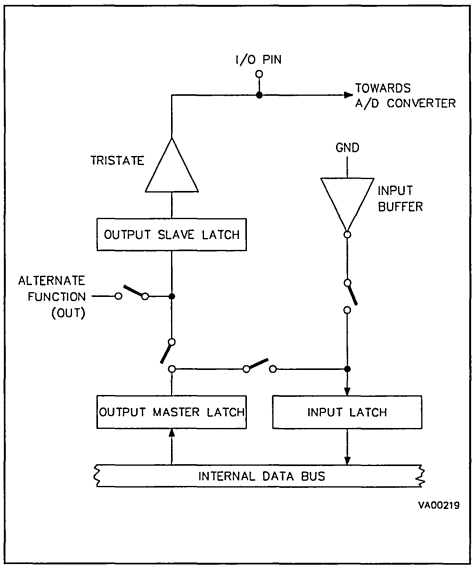
The ST90R50 Analog to Digital Converter (A/D) is comprised of an 8 channel multiplexed input selector and a Successive Approximation converter. The conversion time is a function of the INTCLK frequency; for the maximum 12MHz clock rate, conversion of the selected channel requires 11µs. This time also includes the 3µs of the integral Sample and Hold circuitry, which minimizes need for external components. The resolution of the converted channel is 8 bits ±1/2 LSB between the Analog V_{SS} and V_{DD} references which occupy two pins of the ST90R50 (AV_{SS} and AV_{DD} respectively). This allows the full 256 bit resolution to apply over a reduced input range such as provided by various sensors and allows the best supply noise rejection. The input Analog channel is selected by using the Alternate Function setting as shown in the I/O ports section. The I/O bit structure of the port connected to the A/D converter (Port 4) is modified as shown in figure 55 to prevent the Analog voltage present at the I/O pin from causing high power dissipation across the input buffer. Un-selected analog channels should also be maintained in the Alternate function mode for this reason. A Power Down mode is available for applications which require low power dissipation, this is selected by setting to zero

Figure 53. A/D Block Diagram



ANALOG TO DIGITAL CONVERTER (Continued)

Figure 54. A/D Input Configuration Status

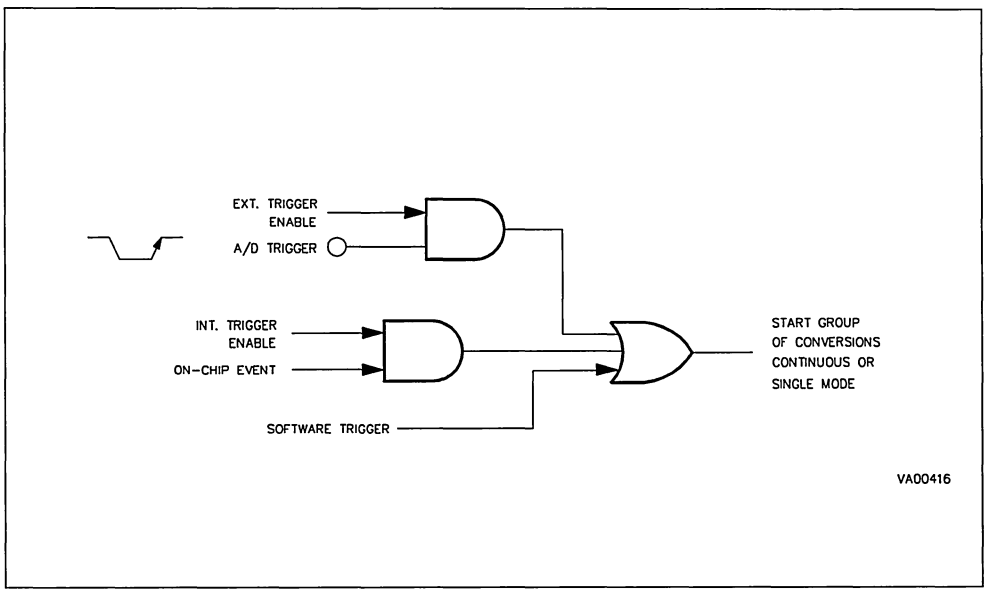


the POW bit (CLR.2) which turns off all Analog functions within the A/D converter.

Conversion

Each of the input Analog channels (AIN0-7) can be converted singly or continuously. In single mode (CONT, CLR.1, = "0") conversions are triggered by setting the Start/Stop bit ST (CLR.0), this is reset by hardware at the end of a group of conversions and conversion stops. The Autoscan mode (CONT = "1") converts each input channel in sequence, starting from the channel number selected in the Start Conversion Address (SC1-3) bits and increasing to channel 7 (AIN7), repeating so that the data registers will be maintained with the latest converted result. Conversion start is triggered by internal or external events. An external trigger (enabled by EXTG, CLR.4, = "1") is caused by a pulse on the ADTRG pin available as an Input Alternate Function. This should have a minimum length of 80 nS and of a period greater than the conversion time. The Internal trigger is enabled by setting INTG, CLR.3, to "1" (this is ORed with EXTG to prevent hardware conflicts, but the correct procedure is to enable only one source at a time), in this case

Figure 55. A/D Trigger Sources



ANALOG DIGITAL CONVERTER (Continued)

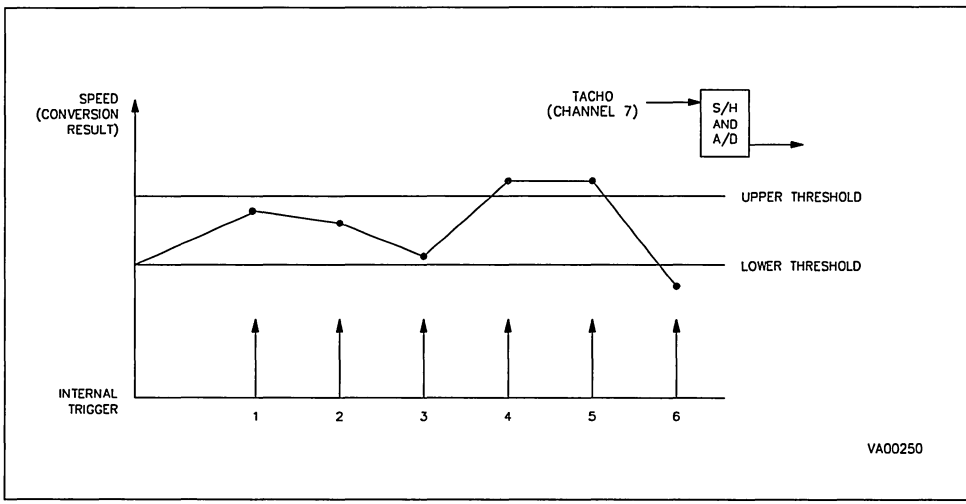
triggering is either by setting the ST bit by software or by enabling the ON-CHIP EVENT signal from the TIMER module.

The resulting data from the converted Analog channel AINx is stored in the appropriate Data Register DxR. Two channels AIN6 and AIN7 have a special feature known as the Analog Watchdog, by the use of two Threshold Registers for each channel. The Upper, (UT6R, UT7R), and lower, (LT6R, LT7R), registers contain User preset values. These values are automatically compared to the value in the Data Registers D6R and D7R following each new conversion. If the resulting data is less than the corresponding Lower Threshold Register, or higher than the contents of the corresponding Upper Threshold Register, then an interrupt may be generated. This hardware feature minimizes analog monitoring overhead and is particularly useful in motor control applications as shown in figure 56.

A/D Interrupts

The ST90R50 A/D converter provides two interrupt sources, End of Conversion and an Analog Watchdog Request. The interrupt vector register (IVR) provides 1 bit automatically generated in hardware to follow the interrupt source, allowing the User to select the base address of a four byte area of the interrupt vector table in which to store the A/D Interrupt Service Routines. The Analog Watchdog Request requires the User to poll within the Compare Result Register (CRR) to determine which of the four thresholds has been exceeded, the threshold status bits should be reset by software in the service routine. The interrupt pending flags, ECV (End of Conversion, ICR.7) and AWD (Analog

Figure 56. Analog Watchdog Used in Motor Speed Control



Watchdog, ICR.6) should also be reset by the User in the Interrupt service routine before the return.

The ST90R50 Analog to Digital converter occupies I/O page 63 (Group F).

SOFTWARE DESCRIPTION

Addressing Modes

The ST90R50 offers a wide variety of addressing modes and combinations to facilitate full and rapid access to the address spaces while reducing program length. Register addressing (using the working register group mechanism or directly addressed) can be used as 8 or 16 bit values for data or indirect addressing into the memory spaces or the Register File. The selection between Program Memory and Data Memory is performed through the DP bit in the FLAG Register, all subsequent actions on the memory space will affect the selected map only, apart from the memory map to memory map post-increment addressing mode which allows the map to be specified as part of the instruction for both destination and source operands. Apart from the immediate data and condition codes all operands are expressed as register file or memory addresses.

The available addressing modes, with the ST9 macro-assembler notation, are in Table 21.

Combinations of Available Addressing Modes

Table 21. Addressing Mode

Addressing Mode	Notation
Immediate Data	#N #NN
Register Direct	R;r RR;rr
Register Indirect	(R) (r)
Register Indexed	N(r) N(rr)
Memory Direct	NN
Memory Indirect	(RR) (rr)
Memory Indirect with Post-Increment	(rr)+
Memory Indirect with Pre-Decrement	-(rr)
Memory Indexed with Immediate Short Offset	N(rr)
Memory Indexed with Immediate Long Offset	NN(rr)
Memory Indexed with Register Offset	rr(rr)
Memory Indirect Post-Increment to Indirect Register Post-Increment	(rr)+ (r)+
Memory Map to Memory Map both with Post-Increment	(rr)+ (r)+
Bit Address	r.b, (rr).b

Legend:
N = 8 bit Value
NN = 16 bit Value or Address
r = Working Register
R = Directly Addressed Register
( ) = Indirect Addressing
( )+ = Indirect with Post-Increment
-( ) = Indirect with Pre-Decrement
.b = Bit Number (0 to 7)

Table 22. Addressing Mode Permutation for Instructions

Two Operand Arithmetic and Logic Instructions	
Destination	**Source**
Register Direct	Register Direct
Register Direct	Register Indirect
Register Direct	Memory Indirect
Register Direct	Memory Indexed
Register Direct	Memory Indirect with Post- Increment
Register Direct	Memory Indirect with Pre- Decrement
Register Direct	Memory Direct
Register Indirect	Register Direct
Memory Indirect	Register Direct
Memory Indexed	Register Direct
Memory Indirect with Post- Increment	Register Direct
Memory Indirect with Pre- Decrement	Register Direct
Memory Direct	Register Direct

SOFTWARE DESCRIPTION (Continued)

Table 22. Addressing Mode Permutation for Instructions (Continued)

Two Operand Load Instructions	
Destination	**Source**
Register Direct	Register Direct
Register Direct	Register Indirect
Register Direct	Register Indexed
Register Direct	Memory Indirect
Register Direct	Memory Indexed
Register Direct	Memory Indirect with Post- Increment
Register Direct	Memory Indirect with Pre- Decrement
Register Direct	Memory Direct
Register Indirect	Register Direct
Register Indexed	Register Direct
Memory Indirect	Register Direct
Memory Indexed	Register Direct
Memory Indirect with Post- Increment	Register Direct
Memory Indirect with Pre- Decrement	Register Direct
Memory Direct	Register Direct
Two Operand Arithmetic and Logic Instructions	
Destination	**Source**
Register Direct	Immediate
Memory Direct	Immediate
Memory Indirect	Immediate
Two Operand Load Instructions	
Destination	**Source**
Register Direct	Immediate
Memory Direct	Immediate
Memory Indirect	Immediate
Long Indexed Memory (1)	Immediate

Table 22. Addressing Mode Permutation for Instructions (Continued)

Two Operand Arithmetic, Logic & Load Instructions	
Destination	**Source**
Memory Indirect	Memory Indirect
Two Operand Load Instructions (2)	
Destination	**Source**
Register Indirect with Post- Increment	Memory Indirect with Post- Increment
Memory Indirect with Post- Increment	Register Indirect with Post- Increment
Memory Indirect with Post- Increment	Memory Indirect with Post- Increment

Notes:
1. Load Word only
2. Load Byte only

Table 22 describes the addressing modes available for the register file and the memory (both as a destination and as a source) for the two operand arithmetic, logic or load instructions.

Instruction Set

The ST90R50 instruction set consists of 87 instruction types functionally divided into eight groups as in Table 23, they are:

- Load (two operands)
- Arithmetic & Logic (two operands)
- Arithmetic Logic and Shift (one operand)
- Stack (one operand)
- Multiply & Divide (two operands)
- Boolean (one or two operands)
- Program Control (zero to three operands)
- Miscellaneous (zero to two operands)

The wide range of instructions facilitates the full use of the register file and address spaces, reducing execution times, while the register pointers mechanism allows an unmatched code efficiency and ultrafast context switching. A particularly notable feature is the comprehensive "Any Bit, Any Register" (ABAR) addressing capability of the Boolean instructions.

The ST90R50 can operate with a wide range of data lengths from single bit, 4-bit nibbles which can be in the form of Binary Coded Decimal (BCD) digits, 8-bit bytes and 16-bit words. The summary on Table 22 shows the instructions belonging to

SOFTWARE DESCRIPTION (Continued)

Table 23. Instruction Set Summary

Load Instructions (Two Operands)								
Mnemonic	**Operand**	**Instruction**	**Flags**					
			C	**Z**	**S**	**V**	**D**	**H**
LD LDW	dst, src dst, src	Load Load Word	– –	– –	– –	– –	– –	– –
Arithmetic and Logic (Two Operands)								
Mnemonic	**Operand**	**Instruction**	**Flags**					
			C	**Z**	**S**	**V**	**D**	**H**
ADD ADDW	dst, src dst, src	Add Add Word	Δ Δ	Δ Δ	Δ Δ	Δ Δ	0 ?	Δ ?
ADC ADCW	dst, src dst, src	Add with Carry Add Word with Carry	Δ Δ	Δ Δ	Δ Δ	Δ Δ	0 ?	Δ ?
SUB SUBW	dst, src dst, src	Subtract Subtract Word	Δ Δ	Δ Δ	Δ Δ	Δ Δ	1 ?	Δ ?
SBC SBCW	dst, src dst, src	Subtract with Carry Subtract Word with Carry	Δ Δ	Δ Δ	Δ Δ	Δ Δ	1 ?	Δ ?
AND ANDW	dst, src dst, src	Logical AND Logical Word AND	– –	Δ Δ	Δ Δ	0 0	– ?	– ?
OR ORW	dst, src dst, src	Logical OR Logical Word OR	– –	Δ Δ	Δ Δ	0 0	– –	– –
XOR XORW	dst, src dst, src	Logical Exclusive OR Logical Word Exclusive OR	– –	Δ Δ	Δ Δ	0 0	– –	– –
CP CPW	dst, src dst, src	Compare Compare Word	Δ Δ	Δ Δ	Δ Δ	Δ Δ	– –	– –
TM TMW	dst, src dst, src	Test Under Mask Test Word Under Mask	– –	Δ Δ	Δ Δ	0 0	– –	– –
TCM TCMW	dst, src dst, src	Test Complement Under Mask Test Word Complement Under Mask	– –	Δ Δ	Δ Δ	0 0	– –	– –

Legend :
0 = Bit set to zero
1 = Bit set to one
Δ = Bit affected
? = Bit status undefined
– = Bit not affected

SOFTWARE DESCRIPTION (Continued)

Table 23. Instruction Set Summary (Continued)

Arithmetic Logic and Shift (One Operand)								
Mnemonic	**Operand**	**Instruction**	**Flags**					
			C	**Z**	**S**	**V**	**D**	**H**
INC INCW	dst dst	Increment Increment Word	– –	Δ Δ	Δ Δ	Δ Δ	– –	– –
DEC DECW	dst dst	Decrement Decrement Word	– –	Δ Δ	Δ Δ	Δ Δ	– –	– –
SLA SLAW	dst dst	Shift Left Arithmetic Shift Word Left Arithmetic	Δ Δ	Δ Δ	Δ Δ	0 0	0 ?	Δ ?
SRA SRAW	dst dst	Shift Right Arithmetic Shift Word Right Arithmetic	Δ Δ	Δ ?	Δ Δ	Δ 0	0 –	Δ –
RRC RRCW	dst dst	Rotate Right through Carry Rotate Word Right through Carry	Δ Δ	Δ ?	Δ Δ	Δ Δ	– –	– –
RLC RLCW	dst dst	Rotate Left through Carry Rotate Word Left through Carry	Δ Δ	Δ ?	Δ Δ	Δ Δ	– –	– –
ROR	dst	Rotate Right	Δ	Δ	Δ	Δ	–	–
ROL	dst	Rotate Left	Δ	Δ	Δ	Δ	–	–
CLR	dst	Clear	–	–	–	–	–	–
CPL	dst	Complement Register	–	Δ	Δ	0	–	–
SWAP	dst	Swap Nibbles	?	Δ	Δ	?	–	–
DA	dst	Decimal Adjust	Δ	Δ	Δ	?	–	–
Stack Instructions (One Operand)								
Mnemonic	**Operand**	**Instruction**	**Flags**					
			C	**Z**	**S**	**V**	**D**	**H**
PUSH PUSHW PEA	src src src	Push on System Stack Push Word on System Stack Push Effective Address on System Stack	– – –	– – –	– – –	– – –	– – –	– – –
POP POPW	dst dst	Pop from System Stack Pop Word from System Stack	– –	– –	– –	– –	– –	– –
PUSHU PUSHUW PEAU	src src src	Push on User Stack Push Word on User Stack Push Effective Address on User Stack	– – –	– – –	– – –	– – –	– – –	– – –
POPU POPUW	dst dst	Pop from User Stack Pop Word from User Stack	– –	– –	– –	– –	– –	– –

SOFTWARE DESCRIPTION (Continued)

Table 23. Instruction Set Summary (Continued)

Multiply and Divide Instructions (Two Operands)								
Mnemonic	**Operand**	**Instruction**	**Flags**					
			C	**Z**	**S**	**V**	**D**	**H**
MUL	dst, src	Multiply 8x8	Δ	Δ	Δ	Δ	0	?
DIV DIVWS	dst, src	Divide 16/8 Divide Word Stepped 32/16	1 ?	Δ ?	Δ ?	? ?	1 ?	? ?
Boolean Instructions (Two Operands)								
Mnemonic	**Operand**	**Instruction**	**Flags**					
			C	**Z**	**S**	**V**	**D**	**H**
BLD	dst, src	Bit Load	–	–	–	–	–	–
BAND	dst, src	Bit AND	–	–	–	–	–	–
BOR	dst, src	Bit OR	–	–	–	–	–	–
BXOR	dst, src	Bit Exclusive OR	–	–	–	–	–	–
Boolean Instructions (One Operand)								
Mnemonic	**Operand**	**Instruction**	**Flags**					
			C	**Z**	**S**	**V**	**D**	**H**
BSET	dst	Bit Set	–	–	–	–	–	–
BRES	dst	Bit Reset	–	–	–	–	–	–
BCPL	dst	Bit Complement	–	–	–	–	–	–
BTSET	dst	Bit Test and Set	–	Δ	Δ	0	–	–
Program Control Instructions (Three Operands)								
Mnemonic	**Operand**	**Instruction**	**Flags**					
			C	**Z**	**S**	**V**	**D**	**H**
CPJFI	dst, src	Compare and Jump on False, Otherwise Post Increment	–	–	–	–	–	–
CPJTI	dst, src	Compare and Jump on True, Otherwise Post Increment	–	–	–	–	–	–

SOFTWARE DESCRIPTION (Continued)

Table 23. Instruction Set Summary (Continued)

Program Control Instructions (Two Operands)								
Mnemonic	**Operand**	**Instruction**	**Flags**					
			C	**Z**	**S**	**V**	**D**	**H**
BTJF	dst, src	Bit Test and Jump if False	–	–	–	–	–	–
BTJT	dst, src	Bit Test and Jump if True	–	–	–	–	–	–
DJNZ	dst, src	Decrement a Working Register and Jump if Not Zero	–	–	–	–	–	–
DWJNZ	dst,src	Decrement a Register Pair and Jump if Not Zero	–	–	–	–	–	–
Program Control Instructions (One Operand)								
Mnemonic	**Operand**	**Instruction**	**Flags**					
			C	**Z**	**S**	**V**	**D**	**H**
JR	cc, dst	Jump Relative if Condition is Met	–	–	–	–	–	–
JP	cc, dst	Jump if Condition is Met	–	–	–	–	–	–
JP	dst	Unconditional Jump	–	–	–	–	–	–
CALL	dst	Unconditional Call	–	–	–	–	–	–
Program Control Instructions (No Operand)								
Mnemonic	**Operand**	**Instruction**	**Flags**					
			C	**Z**	**S**	**V**	**D**	**H**
RET		Return from Subroutine	–	–	–	–	–	–
IRET		Return from Interrupt	Δ	Δ	Δ	Δ	Δ	Δ
WFI		Stop Program Execution and Wait Next Enabled Interrupt. If a DMA request is present the CPU executes the DMA service routine and returns to WFI state.	–	–	–	–	–	–
HALT		Stop Program Execution until RESET	–	–	–	–	–	–
Miscellaneous (Two Operands)								
Mnemonic	**Operand**	**Instruction**	**Flags**					
			C	**Z**	**S**	**V**	**D**	**H**
XCH	dst, src	Exchange Registers	–	–	–	–	–	–

SOFTWARE DESCRIPTION (Continued)

Table 23. Instruction Set Summary (Continued)

Miscellaneous (One Operand)								
Mnemonic	Operand	Instruction	Flags					
			C	Z	S	V	D	H
SRP	src	Set Register Pointer Long (16 Working Registers)	–	–	–	–	–	–
SRP0	src	Set Register Pointer 0 (8 LSB Working Registers)	–	–	–	–	–	–
SRP1	src	Set Register Pointer 1 (8 MSB Working Registers)	–	–	–	–	–	–
SPP	src	Set Page Pointer	–	–	–	–	–	–
EXT	src	Sign Extend	–	–	–	–	–	–
Miscellaneous (No Operand)								
Mnemonic	Operand	Instruction	Flags					
			C	Z	S	V	D	H
EI		Enable Interrupts	–	–	–	–	–	–
DI		Disable Interrupts	–	–	–	–	–	–
SCF		Set Carry Flag	1	–	–	–	–	–
RCF		Reset Carry Flag	0	–	–	–	–	–
CCF		Complement Carry Flag	Δ	–	–	–	–	–
SPM		Select Program Memory	–	–	–	–	–	–
SDM		Select Data Memory	–	–	–	–	–	–
NOP		No Operation	–	–	–	–	–	–

each group and the number of operands required for each. The source operand is "src", "dst" is the destination operand, and "cc" is the condition code selection.

Processor Flags

An important aspect of any single chip microcontroller is the ability to test data and make the appropriate action based on the results. In order to provide this facility, register 231 in the Register File is used as a Flag Register. Six bits of this register are used as the following flags:

C - Carry

Z - Zero

S - Sign

V - Overflow

D - Decimal Adjust

H - Half Carry

One of the two remaining bits in the flag register is available to the user (bit 1, F1). Bit 0 is the Program/Data Memory selector bit and is operated on directly by the hardware within the ST90R50. The P/$\overline{D}$ pin will follow the status of this bit.

SOFTWARE DESCRIPTION (Continued)

Table 24. Condition Codes Summary

Mnemonic Code	Meaning	Flag Setting
F	Always False	—
T	Always True	—
C	Carry	C = 1
NC	No Carry	C = 0
Z	Zero	Z = 1
NZ	No Zero	Z = 0
PL	Plus	S = 0
MI	Minus	S = 1
OV	Overflow	V = 1
NOV	No Overflow	V = 0
EQ	Equal	Z = 1
NE	Not Equal	Z = 0
GE	Greater Then or Equal	(S xor V) = 0
LT	Less Than	(S xor V) = 1
GT	Greater Than	(Z or (S xor V)) = 0
LE	Less Than or Equal	(Z or (S xor V)) = 1
UGE	Unsigned Greater Than or Equal	C = 0
UL	Unsigned Less Than	C = 1
UGT	Unsigned Greater Than	(C = 0 and Z = 0) = 1
ULE	Unsigned Less Than or Equal	(C or Z) = 1

Condition Codes. Flags C, Z, S, and V control the operation of the "conditional" Jump instructions. Table 24 shows the condition codes and the flag settings affecting the jump.

POWERFUL DEVELOPMENT ENVIRONMENT

ST9 Software Tools

The following Software Tools are available for MS-DOS, SUN-3 and SUN-4 operating systems:

AST9 high-level macro assembler with predefinited macro instructions (IF/ELSE, WHILE, DO, LOOP, SWITCH, BREAK, PROCEDURE, RESTURN).

LST9 Incremental Linker/Loader.

CST9 Optimised C-Compiler (ANSI STANDARD).

ARST9 Library Archiver.

SIMST9 Software Simulator with realtime emulation executor

ST90R50 Hardware Emulator. Realtime emulation of the ST90R50 in all packaging options is performed by a modular emulation system, interfaced to the host computer through an RS232

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	– 0.3 to 7.0	V
AV_{DD}, AV_{SS}	Analog Supply Voltage	$V_{SS} \le AV_{SS} < AV_{DD} \le V_{DD}$	V
V_I	Input Voltage	V_{SS} – 0.3 to V_{DD} +0.3	V
V_O	Output Voltage	V_{SS} – 0.3 to V_{DD} +0.3	V
T_{STG}	Storage Temperature	– 55 to + 150	°C

Note: Stresses above those listed as "absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value		Unit
		Min.	Max.	
T_A	Operating Temperature	– 40	85	°C
V_{DD}	Operating Supply Voltage	4.5	5.5	V
f_{OSCE}	External Oscillator Frequency		24	MHz
f_{OSCI}	Internal Oscillator Frequency		12	MHz

DC ELECTRICAL CHARACTERISTICS

(V_{DD} = 5V ± 10% T_A = – 40 °C to + 85°C, unless otherwise specified)

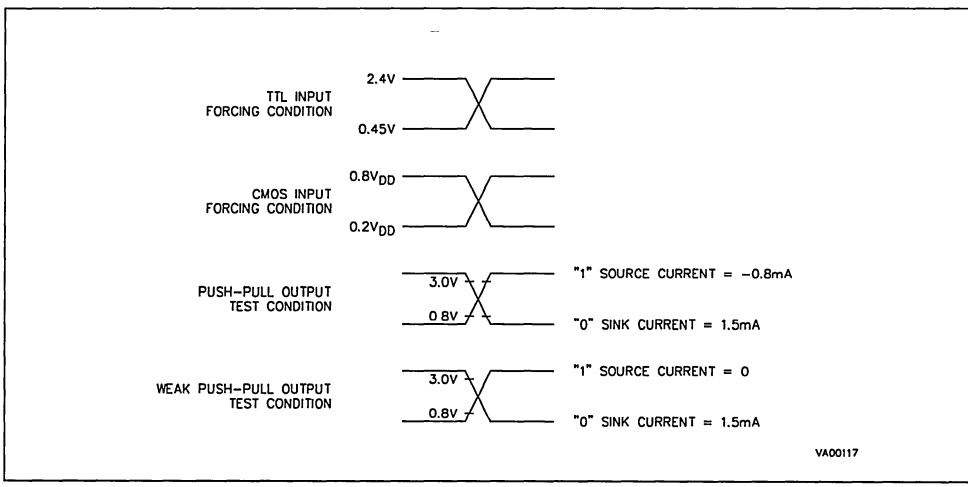
Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
V_{IHCK}	Clock Input High Level	External Clock	0.7 V_{DD}		V_{DD} + 0.3	V
V_{ILCK}	Clock Input Low Level	External Clock	– 0.3		0.3 V_{DD}	V
V_{IH}	Input High Level	TTL	2.0		V_{DD} + 0.3	V
		CMOS	0.7 V_{DD}		VDD + 0.3	V
V_{IL}	Input Low Level	TTL	– 0.3		0.8	V
		CMOS	– 0.3		0.3 V_{DD}	V
V_{IHRS}	Reset Input High Level		0.7 V_{DD}		V_{DD} + 0.3	V
V_{ILRS}	Reset Input Low Level		–0.3		0.3 V_{DD}	V
V_{HYRS}	Reset Input Hysteresis		0.3		1.5	V
V_{OH}	Output High Level	Push Pull, Iload = – 0.8mA	V_{DD} – 0.8			V
V_{OL}	Output Low Level	Push Pull or Open Drain, Iload = – 1.6mA			0.4	V

DC ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
I_{WPU}	Weak Pull-up Current	Bidirectional Weak Pull-up, V_{OL} = 0V	– 80	– 200	– 420	µA
I_{APU}	Active Pull-up Current, for INT0 and INT7 only	V_{IN} < 0.8V	– 80	– 200	– 420	µA
I_{LKIO}	I/O Pin Input Leakage	Input/Tri-State, 0V < V_{IN} < V_{DD}	– 10		+ 10	µA
I_{LKRS}	Reset Pin Input Leakage	0V < V_{IN} < V_{DD}	– 30		+ 30	µA
I_{LKAD}	A/D Pin Input Leakage	Alternate Function, Open Drain, 0V < V_{IN} < V_{DD}	– 3		+ 3	µA
I_{LKAP}	Active Pull-up Input Leakage	0V < V_{IN} < 0.8V	– 10		+ 10	µA
I_{LKOS}	OSCIN Pin Input Leakage	0V < V_{IN} < V_{DD}	– 10		+ 10	µA
I_{DD}	Run Mode Current	24MHz, Note 1		32	70	mA
		4MHz, Note 1		6	12	mA
I_{DP2}	Run Mode Current Prescale by 2	24MHz, Note 1		19	40	mA
		4MHz, Note 1		4	8	mA
I_{WFI}	WFI Mode Current	24MHz, Note 1		9	18	mA
		4MHz, Note 1		2.5	5	mA
I_{HALT}	HALT Mode Current	24MHz, Note 1			100	µA

Note:
1. All I/O Ports are configured in Bidirectional Weak Pull-up Mode with no DC load, External Clock pin (OSCIN) is driven by square wave external clock. No peripheral working. External interface not active (Internal Program Execution).

DC TEST CONDITIONS



AC ELECTRICAL CHARACTERISTICS

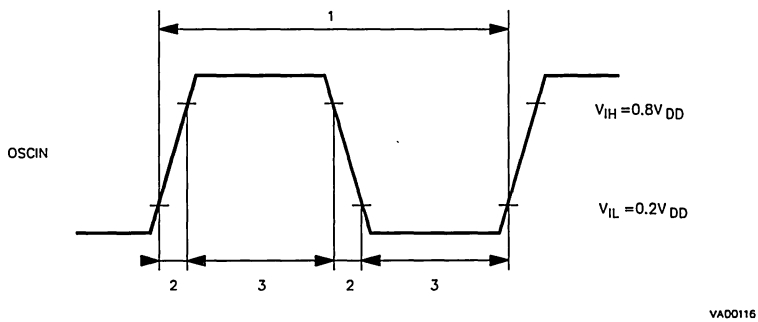
CLOCK TIMING TABLE

(V_{DD} = 5V ± 10%, T_A = − 40°C to + 85°C, unless otherwise specified)

N°	Symbol	Parameter	Value		Unit	Note
			Min.	Max.		
1	TpC	OSCIN Clock Period	41.5		ns	1
			83		ns	2
2	TrC, TfC	OSCIN Rise and Fall Time		12	ns	
3	TwCL, TwCH	OSCIN Low and High Width	25	12	ns	1
			38		ns	2

Notes:
1. Clock divided by 2 internally (MODER.DIV2=1)
2. Clock not divided by 2 internally (MODER.DIV2=0)

CLOCK TIMING



EXTERNAL BUS TIMING TABLE

(V_{DD} = 5V ± 10%, T_A = – 40 °C to + 85 °C, Cload = 50pF, CPUCLK = 12MHz, unless otherwise specified)

N°	Symbol	Parameter	Value (Note)				Unit
			OSCIN Divided By 2	OSCIN Not Divided By 2	Min.	Max.	
1	TsA (AS)	Address Set-up Time before $\overline{AS}$ ↑	TpC (2P+1) –22	TWCH+PTpC –18	20		ns
2	ThAS (A)	Address Hold Time after $\overline{AS}$ ↑	TpC –17	TwCL –13	25		ns
3	TdAS (DR)	$\overline{AS}$ ↑ to Data Available (read)	TpC (4P+2W+4) –52	TpC (2P+W+2) –51		115	ns
4	TwAS	$\overline{AS}$ Low Pulse Width	TpC (2P+1) –7	TwCH+PTpC –3	35		ns
5	TdAz (DS)	Address Float to $\overline{DS}$ ↓	0	0	0		ns
6	TwDSR	$\overline{DS}$ Low Pulse Width (read)	TpC (4P+2W+3) –20	TwCH+TpC (2P+W+1) –16	105		ns
7	TwDSW	$\overline{DS}$ Low Pulse Width (write)	TpC (2P+2W+2) –13	TpC (P+W+1) –13	70		ns
8	TdDSR (DR)	$\overline{DS}$ ↓ to Data Valid Delay (read)	TpC (4P+2W-3) –50	TwCH+TpC(2P+W+1) – 46		75	ns
9	ThDR (DS)	Data to $\overline{DS}$ ↑ Hold Time (read)	0	0	0		ns
10	TdDS (A)	$\overline{DS}$ ↑ to Address Active Delay	TpC –7	TwCL –3	35		ns
11	TdDS (AS)	$\overline{DS}$ ↑ to $\overline{AS}$ ↓ Delay	TpC –18	TwCL –14	24		ns
12	TsR/W (AS)	R/$\overline{W}$ Set-up Time before $\overline{AS}$ ↑	TpC (2P+1) –22	TwCH+PTpC –18	20		ns
13	TdDSR (R/W)	$\overline{DS}$ ↑ to R/$\overline{W}$ and Address Not Valid Delay	TpC –9	TwCL –5	33		ns
14	TdDW (DSW)	Write Data Valid to $\overline{DS}$ ↓ Delay (write)	TpC (2P+1) –32	TwCH+PTpC –28	10		ns
15	ThDS (DW)	Data Hold Time after DS ↑ (write)	TpC –9	TwCL –5	33		ns
16	TdA (DR)	Address Valid to Data Valid Delay (read)	TpC (6P+2W+5) –68	TwCH+TpC (3P+W+2) –64		140	ns
17	TdAs (DS)	$\overline{AS}$ ↑ to $\overline{DS}$ ↓ Delay	TpC –18	TwCL –14	24		ns

Note: The value left hand two columns show the formula used to calculate the timing minimum or maximum from the oscillator clock period, prescale value and number of wait cycles inserted.
The value right hand two columns show the timing minimum and maximum for an external clock at 24 MHz divided by 2, prescaler value of zero and zero wait status.

Legend:
P = Clock Prescaling Value
W = Wait Cycles

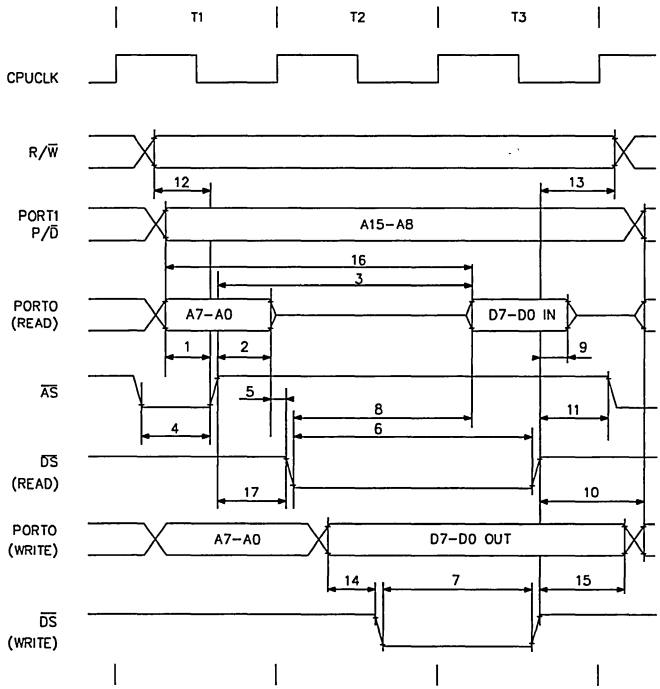
TpC = OSCIN Period
TwCH = High Level OSCIN half period
TwCL = Low Level OSCIN half period

EXTERNAL WAIT TIMING TABLE (V_{DD} = 5V ± 10%, T_A = –40°C to +85°C, Cload = 50pF, INTCLK = 12MHz, Push-pull output configuration, unless otherwise specified)

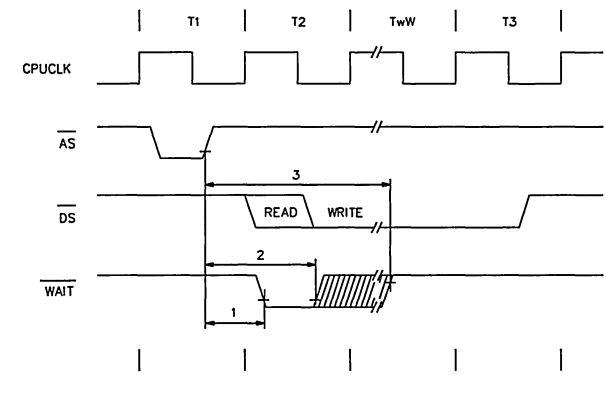
N°	Symbol	Parameter	Value (Note)				Unit
			OSCIN Divided By 2	OSCIN Not Divided By 2	Min.	Max.	
1	TdAS (WAIT)	$\overline{AS}$ ↑ to $\overline{WAIT}$ ↓ Delay	2(P+1)TpC –29	(P+1)TpC –29		40	ns
2	TdAS (WAIT)	$\overline{AS}$ ↑ to $\overline{WAIT}$ ↑ Minimum Delay	2(P+W+1)TpC –4	(P+W+1)TpC –4	80		ns
3	TdAS (WAIT)	$\overline{AS}$ ↑ to $\overline{WAIT}$ ↑ Maximum Delay	2(P+W+1)TpC – 29	(P+W+1)TpC –29		83W+40	ns

Note: The value left hand two columns show the formula used to calculate the timing minimum or maximum from the oscillator clock period, prescale value and number of wait cycles inserted.
The value right hand two columns show the timing minimum and maximum for an external clock at 24 MHz divided by 2, prescale value of zero and zero wait status.

EXTERNAL BUS TIMING



EXTERNAL WAIT TIMING

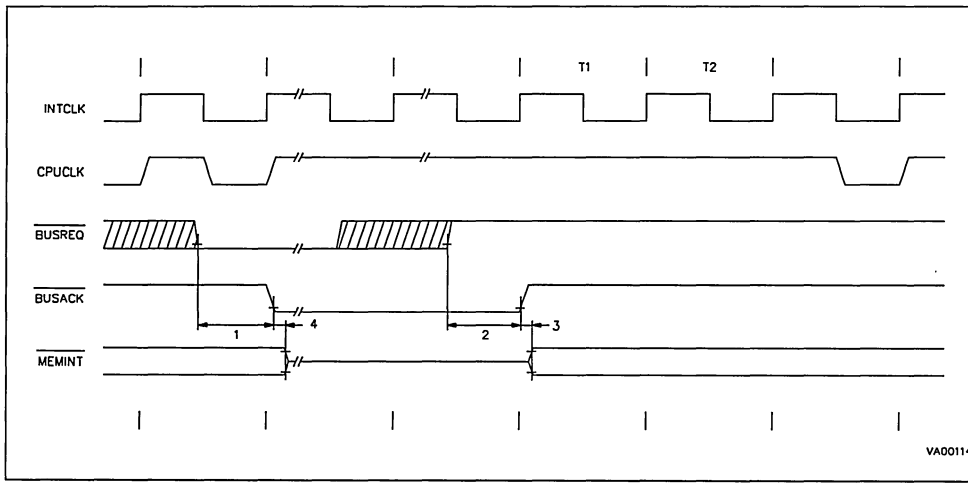


BUS REQUEST/ACKNOWLEDGE TIMING TABLE (V_{DD} = 5V ± 10%, T_A = −40°C to +85°C, Cload = 50pF, INTCLK = 12MHz, Push-pull output configuration, unless otherwise specified)

N°	Symbol	Parameter	Value (Note)				Unit
			OSCIN Divided By 2	OSCIN Not Divided By 2	Min.	Max.	
1	TdBR (BACK)	$\overline{BREQ}$ ↓ to $\overline{BUSACK}$ ↓	TpC+8	TwCL+12	50		ns
			TpC(6P+2W+7)+65	TpC(3P+W+3)+TwCL+65		360	ns
2	TdBR (BACK)	$\overline{BREQ}$ ↑ to $\overline{BUSACK}$ ↑	3TpC+60	TpC+TwCL+60		185	ns
3	TdBACK (BREL)	$\overline{BUSACK}$ ↓ to Bus Release	20	20		20	ns
4	TdBACK (BACT)	$\overline{BUSACK}$ ↑ to Bus Active	20	20		20	ns

Note: The value left hand two columns show the formula used to calculate the timing minimum or maximum from the oscillator clock period, prescale value and number of wait cycles inserted.
The value right hand two columns show the timing minimum and maximum for an external clock at 24 MHz divided by 2, prescale value of zero and zero wait status.

BUS REQUEST/ACKNOWLEDGE TIMING



Note : MEMINT = group of memory interface signals : $\overline{AS}$, $\overline{DS}$, R/$\overline{W}$, P00-P07, P10-P17.

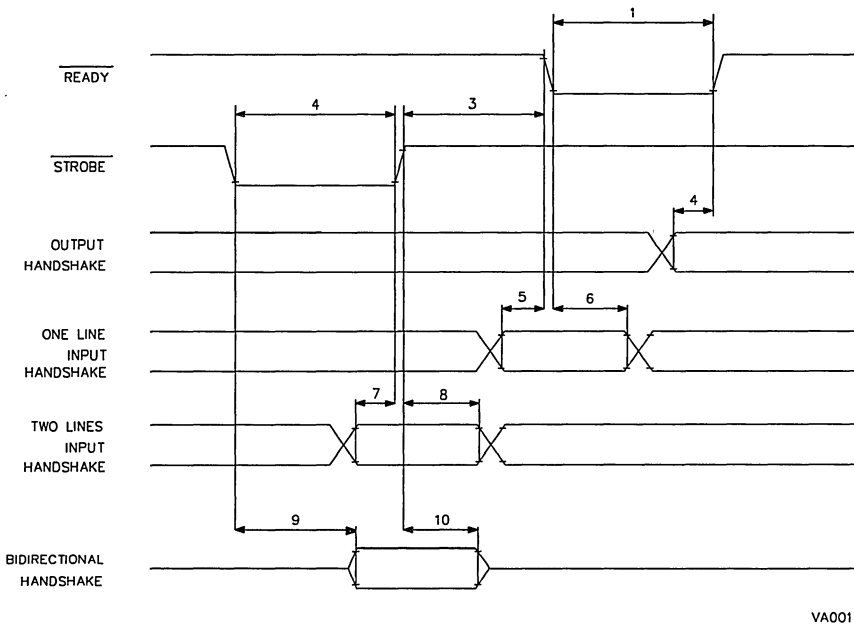
HANDSHAKE TIMING TABLE (V_{DD} = 5V ± 10%, T_A = –40°C to +85°C, Cload = 50pF, INTCLK = 1.2MHz, Push-pull output configuration, unless otherwise specified)

N°	Symbol	Parameter	Value (Note)				Min.	Max.	Unit
			OSCIN Divided By 2		OSCIN Not Divided By 2				
			Min.	Max.	Min.	Max.			
1	TwRDY	RDRDY, WRRDY Pulse Width in One Line Handshake	2TpC (P+W+1) –18		Tp (P+W+1) – 18		65		ns
2	TwSTB	$\overline{RDSTB}$, $\overline{WRSTB}$ Pulse Width	2TpC+12		TpC+12		95		ns
3	TdST (RDY)	$\overline{RDSTB}$, or $\overline{WRSTB}$ ↑ to RDRDY or WRRDY ↓		TpC+45		(TpC-TwCL) +45		87	ns
4	TsPD (RDY)	Port Data to RDRDY ↑ Set-up Time	(2P+2W+1) TpC –25		TwCH+(W+P) TpC –25		16		ns
5	TsPD (RDY)	Port Data to WRRDY ↓ Set-up Time in One Line Handshake	43		43		43		ns
6	ThPD (RDY)	Port Data to WRRDY ↓ Hold Time in One Line Handshake	0		0		0		ns
7	TsPD (STB)	Port Data to $\overline{WRSTB}$ ↑ Set-up Time	10		10		10		ns
8	ThPD (STB)	Port Data to WRSTB ↑ Hold Time	25		25		25		ns
9	TdSTB (PD)	$\overline{RDSTBD}$ ↑ to Port Data Delay Time in Bidirectional Handshake		35		35		35	ns
10	TdSTB (PHZ)	$\overline{RDSTB}$ ↑ to Port High-Z Delay Time in Bidirectional Handshake		25		25		25	ns

Note: The value left hand two columns show the formula used to calculate the timing minimum or maximum from the oscillator clock period, prescale value and number of wait cycles inserted.
The value right hand two columns show the timing minimum and maximum for an external clock at 24 MHz divided by 2, prescaler value of zero and zero wait status.

Legend:
P = Clock Prescaling Value (R235.4,3,2)
W = Programmable Wait Cycles (R252.2.1.0/5,4,3) + External Wait Cycles

HÁNDSHAKE TIMING

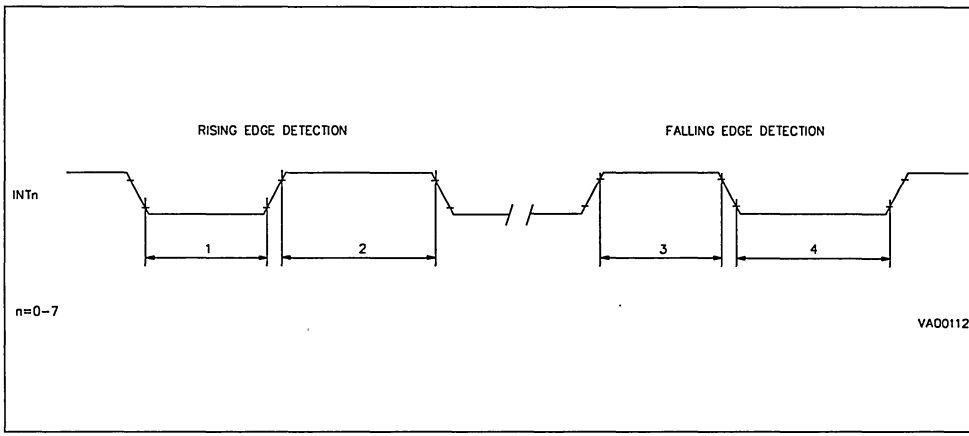


EXTERNAL INTERRUPT TIMING TABLE (V_{DD} = 5V ±10%, T_A = –40°C to +85°C, Cload = 50pF, INTCLK = 12MHz, Push-pull output configuration, unless otherwise specified)

N°	Symbol	Parameter	Value (Note)				Unit
			OSCIN Divided By 2 Min.	OSCIN Not Divided By 2 Min.	Min.	Max.	
1	TwLR	Low Level Minimum Pulse Width in Rising Edge Mode	2TpC+12	TpC+12	95		ns
2	TwHR	High Level Minimum Pulse Width in Rising Edge Mode	2TpC+12	TpC+12	95		ns
3	TwHF	High Level Minimum Pulse Width in Falling Edge Mode	2TpC+12	TpC+12	95		ns
4	TwLF	Low Level Minimum Pulse Width in Falling Edge Mode	2TpC+12	TpC+12	95		ns

Note: The value left hand two columns show the formula used to calculate the timing minimum or maximum from the oscillator clock period, prescale value and number of wait cycles inserted.
The value right hand two columns show the timing minimum and maximum for an external clock at 24 MHz divided by 2, prescale value of zero and zero wait status.

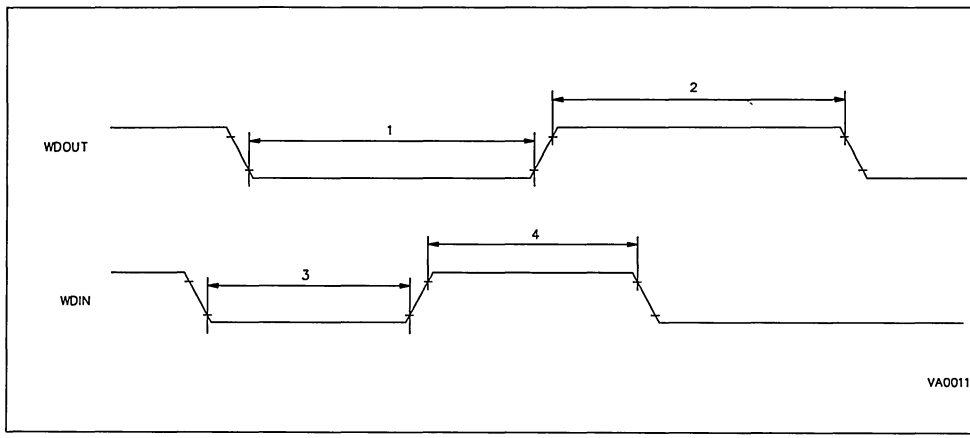
EXTERNAL INTERRUPT TIMING



WATCHDOG TIMING TABLE (V_{DD} = 5V ± 10%, T_A = –40°C to +85°C, Cload = 50pF, INTCLK =12MHz, Output Alternate Function set as Push-pull)

N°	Symbol	Parameter	Value		Unit
			Min.	Max.	
1	TwWDOL	WDOUT Low Pulse Width	620		ns
2	TwWDOH	WDOUT High Pulse Width	620		ns
3	TwWDIL	WDIN Low Pulse Width	350		ns
4	TwWDIH	WDIN High Pulse Width	350		ns

WATCHDOG TIMING

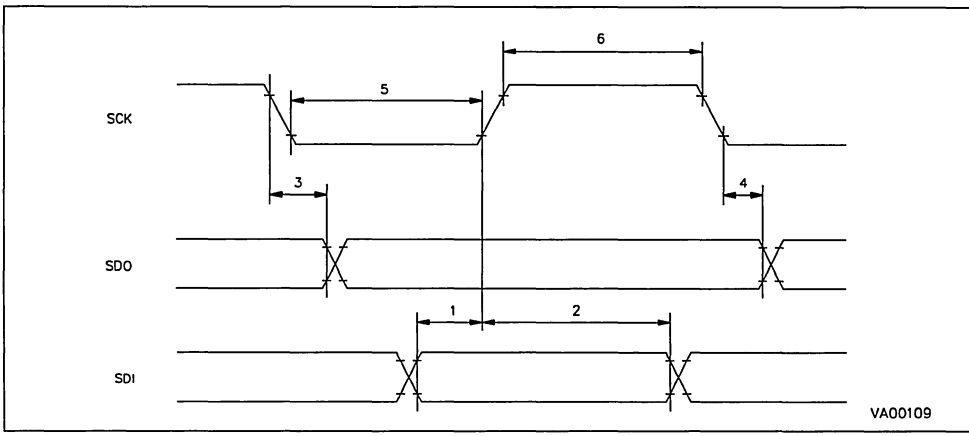


SPI TIMING TABLE (V_{DD} = 5V ± 10%, T_A = –40°C to +85°C, Cload = 50pF, INTCLK = 12MHz, Output Alternate Function set as Push-pull)

N°	Symbol	Parameter	Value		Unit
			Min.	Max.	
1	TsDI	Input Data Set-up Time	100		ns
2	ThDI (1)	Input Data Hold Time	1/2 TpC+100		ns
3	TdOV	SCK to Output Data Valid		100	ns
4	ThDO	Output Data Hold Time	-20		ns
5	TwSKL	SCK Low Pulse Width	300		ns
6	TwSKH	SCK High Pulse Width	300		ns

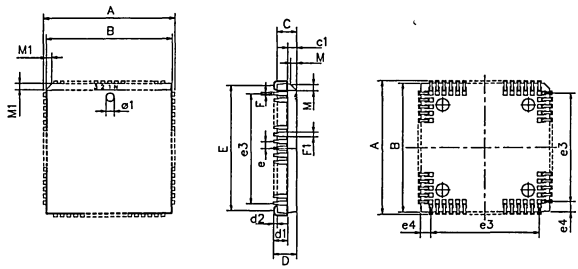
Note: 1. TpC is the Clock period.

SPI TIMING



PACKAGE MECHANICAL DATA

Figure 57. 84-Lead Plastic Leaded Chip Carrier



DIM	MM			INCHES		
	Min	Typ	Max	Min	Typ	Max
A	30.10		30.35	1.18		1.19
B	29.20		29.41	1.14		1.15
C						
C1						
D	4.20		5.08	0.16		0.19
D1		2.54			0.02	
D2		0.56				
D3				1.09		1.12
E	27.69		28.70		0.04	
e		1.27				
e3					0.01	
F		0.38				
F1						0.003
G			0.101			
H		1.27			0.04	
H1		1.14			0.04	

ORDERING INFORMATION

Sales Type	Frequency	Temperature Range	Package
ST90R50C6	24MHz	-40°C to +85°C	PLCC84
ST90R50C1	24MHz	0°C to +70°C	PLCC84

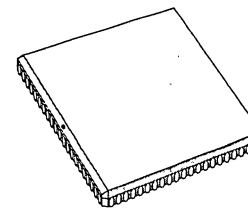
SGS-THOMSON MICROELECTRONICS

ST9054

32K ROM HCMOS MCU WITH BANKSWITCH AND A/D CONVERTER

ADVANCE DATA

- Single chip microcontroller with 32K bytes of ROM, 1,280 bytes of static RAM and 256 bytes of register file with 224 general purpose registers available as RAM, accumulators or index pointers.
- Bank-Switch logic allowing a maximum addressing capability of 8M bytes in both program and data spaces (16M byte total).
- 8/16 bit CORE with full feature DMA controller, a powerful interrupt handler and a Standard Serial Peripheral Interface (SPI) handling S-bus, I^2C-bus, IM-bus and Standard Serial Peripheral Interfaces.
- Up to 8 external interrupts edge-selectable plus 1 non-maskable interrupt.
- 16 bit programmable Timer with 8 bit Prescaler, able to be used as a Watchdog Timer for system integrity.
- Three 16 bit Multifunction Timer modules, each with an 8 bit prescaler and 13 operating modes, allowing simple use for complex waveform generation and measurement, PWM functions and many other system timing operations.
- 8 channel Analog to Digital Converter, with integral sample and hold, fast 11us conversion time, 8 bit ±1/2 LSB resolution with Analog Watchdog on two channels.
- Two full function Serial Communications Interfaces with 110 to 375000 baud rate generator, asynchronous and byte synchronous capability (fully programmable format) and address/wake-up bit option.
- On-chip DMA channels associated to the Multifunction Timers and the Serial Communications Interface.
- Up to nine 8 bit I/O ports with programmable input thresholds and output characteristics. Alternative functions allow the full use of all pins.
- Powerful software development tools, including assembler, linker, C-compiler, archiver, software and hardware emulators.
- Windowed and One Time Programmable EPROM parts available for prototyping and pre-production development phases.



PLCC84

(Ordering Information at the end of the datasheet)

Figure 1. ST9054 Block Diagram

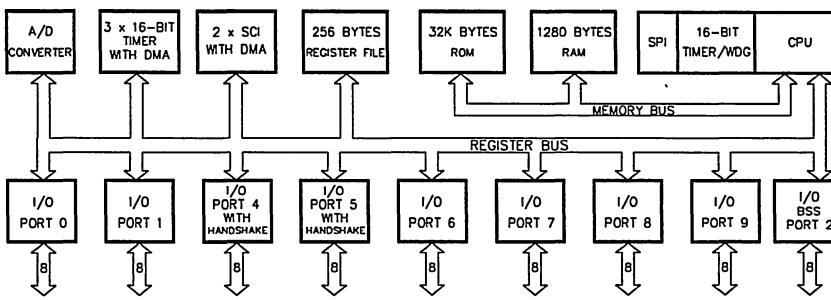
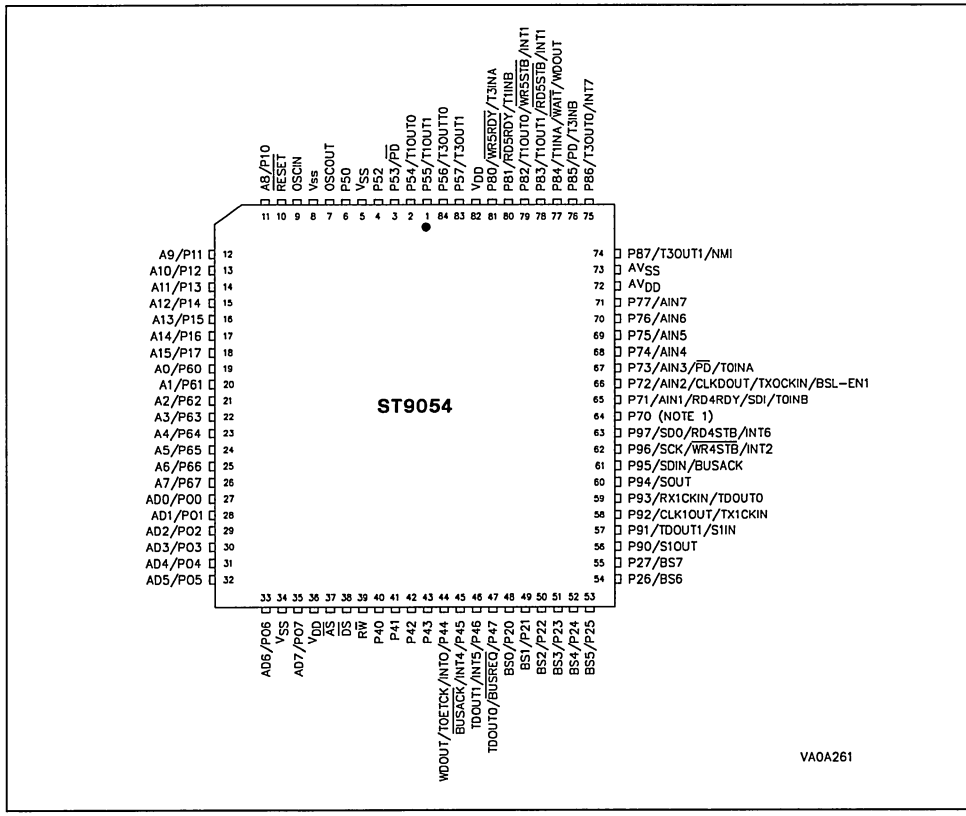


Figure 2. ST9054 Pin Configuration



Note 1 : P70/AIN0/ADTRG/$\overline{\text{WR4DRDY}}$/RX0CKIN/WDIN/BSH_EN1.

GENERAL DESCRIPTION

The ST9054 is a ROM member of the ST9 family of microcontrollers, completely developed and produced by SGS-THOMSON Microelectronics using a proprietary n-well HCMOS process.

The ROM part is fully compatible with its EPROM versions, which may be used for the prototyping and pre-production phases of development, and can be configured as: standalone microcontrollers with 32K bytes of on-chip ROM, microcontrollers able to manage up to 120K bytes of external memory, (16M byte with the Bankswitch logic), or as parallel processing elements in a system with other processors and peripheral controllers.

A key point of the ST9054 architecture is its modular approach which allows software commonality with all other members of the ST9 family.

The nucleus of the modular design of the ST9054 is the advanced Core which includes the Central Processing Unit (CPU), the Register File, a 16 bit Timer/Watchdog with 8 bit Prescaler, a Serial Peripheral Interface supporting S-bus, I^2C-bus and IM-bus Interface, plus two 8 bit I/O ports. The Core has independent memory and register buses allowing a high degree of pipelining to add to the efficiency of the code execution speed of the extensive instruction set.

GENERAL DESCRIPTION (Continued)

The powerful I/O capabilities demanded by microcontroller applications are fulfilled by the ST9054 with up to 72 I/O lines dedicated to digital Input/Output. These lines are grouped into up to nine 8 bit I/O Ports and can be configured on a bit basis under software control to provide timing, status signals, address and data buses for interfacing external memory, timer inputs and outputs, analog inputs, external interrupts and serial or parallel I/O with or without handshake.

Three basic memory spaces are available to support this wide range of configurations: Program Memory (internal and external), Data Memory (internal and external) and the Register File, which includes the control and status registers of the on-chip peripherals.

Three 16 bit MultiFunction Timers, each with an 8 bit Prescaler and 13 operating modes allow simple use for complex waveform generation and measurement, PWM functions and many other system timing functions by the usage of the two associated DMA channels for each timer.

In addition there is an 8 channel Analog to Digital Converter with integral sample and hold, fast 11µs conversion time and 8 bit ±1/2 LSB resolution. An Analog Watchdog feature is included for two input channels.

Completing the device are two full duplex Serial Communications Interfaces, each with an integral 110 to 375000 baud rate generator, asynchronous and byte synchronous capability (fully programmable format) and associated address/wake-up option, plus two DMA channels.

PIN DESCRIPTION

$\overline{AS}$. *Address Strobe (output, active low, 3-state).* Address Strobe is pulsed low once at the beginning of each memory cycle. The rising edge of $\overline{AS}$ indicates that address, Read/Write (R/$\overline{W}$), and Data Memory signals are valid for program or data memory transfers. Under program control, $\overline{AS}$ can be placed in a high-impedance state along with Port 0, Port 1, Port 6, Data Strobe ($\overline{DS}$) and R/$\overline{W}$.

$\overline{DS}$. *Data Strobe (output, active low, 3-state).* Data Strobe provides the timing for data movement to or from Port 0 for each memory transfer. During a write cycle, data out is valid at the leading edge of $\overline{DS}$. During a read cycle, Data In must be valid prior to the trailing edge of $\overline{DS}$. When the ST9054 accesses on-chip memory, $\overline{DS}$ is held high during the whole memory cycle. It can be placed in a high impedance state along with Port 0, Port 1, Port 6, $\overline{AS}$ and R/$\overline{W}$.

R/$\overline{W}$. *Read/Write (output, 3-state).* Read/Write determines the direction of data transfer for external memory transactions. R/$\overline{W}$ is low when writing to external program or data memory, and high for all other transactions. The timing of R/$\overline{W}$ may be modified when using the Bank Switch Logic memory expansion to prevent external timing conflicts. R/$\overline{W}$ can be placed in a high impedance state along with Port 0, Port 1, Port 6, $\overline{AS}$ and $\overline{DS}$.

$\overline{RESET}$. *Reset (input, active low).* The ST9 is initialised by the Reset signal. With the deactivation of $\overline{RESET}$, program execution begins from the Program memory location pointed to by the vector contained in program memory locations 00h and 01h.

OSCIN, OSCOUT. *Oscillator (input and output).* These pins connect a parallel-resonant crystal (24MHz maximum), or an external source to the on-chip clock oscillator and buffer. OSCIN is the input of the oscillator inverter and internal clock generator; OSCOUT is the output of the oscillator inverter.

AV_{DD}. Analog V_{DD} of the Analog to Digital Converter.

AV_{SS}. Analog V_{SS} of the Analog to Digital Converter.

V_{DD}. Main Power Supply Voltage (5V±10%)

V_{SS}. Digital Circuit Ground.

P0.0-P0.7, P1.0-P1.7, P2.0-P2.7, P4.0-P4.7, P5.0-P5.7, P6.0-P6.7, P7.0-P7.7, P8.0-P8.7, P9.0-P9.7 *I/O Port Lines (Input/Output, TTL or CMOS compatible).* 8 lines grouped into I/O ports of 8 bits, bit programmable under program control as general purpose I/O or as Alternate functions (see next section).

I/O Port Alternate Functions.

Each pin of the I/O ports of the ST9054 may assume software programmable Alternative Functions as shown in the Pin Configuration Drawings. Table 1 shows the Functions allocated to each I/O Port pins

PIN DESCRIPTION (Continued)

Table 1. ST9054 I/O Port Alternate Function Summary

I/O PORT Port.bit	Name	Function IN/OUT	Alternate Function	Pin Number
P0.0	A0/D0	I/O	Address/Data bit 0 mux	27
P0.1	A1/D1	I/O	Address/Data bit 1 mux	28
P0.2	A2/D2	I/O	Address/Data bit 2 mux	29
P0.3	A3/D3	I/O	Address/Data bit 3 mux	30
P0.4	A4/D4	I/O	Address/Data bit 4 mux	31
P0.5	A5/D5	I/O	Address/Data bit 5 mux	32
P0.6	A6/D6	I/O	Address/Data bit 6 mux	33
P0.7	A7/D7	I/O	Address/Data bit 7 mux	35
P1.0	A8	O	Address bit 8	11
P1.1	A9	O	Address bit 9	12
P1.2	A10	O	Address bit 10	13
P1.3	A11	O	Address bit 11	14
P1.4	A12	O	Address bit 12	15
P1.5	A13	O	Address bit 13	16
P1.6	A14	O	Address bit 14	17
P1.7	A15	O	Address bit 15	18
P2.0	BS0	O	Bank Switch Address 0 (A16)	48
P2.1	BS1	O	Bank Switch Address A17	49
P2.2	BS2	O	Bank Switch Address A18	50
P2.3	BS3	O	Bank Switch Address A19	51
P2.4	BS4	O	Bank Switch Address A20	52
P2.5	BS5	O	Bank Switch Address A21	53
P2.6	BS6	O	Bank Switch Address A22	54
P2.7	BS7	O	Bank Switch Address A23	55
P4.0		I/O	I/O Handshake Port 4	40
P4.1		I/O	I/O Handshake Port 4	41
P4.2		I/O	I/O Handshake Port 4	42
P4.3		I/O	I/O Handshake Port 4	43
P4.4	INT0	I	External interrupt 0	44
P4.4	WDOUT	O	T/WD output	44
P4.4		I/O	I/O Handshake Port 4	44
P4.5	INT4	I	External interrupt 4	45
P4.5	$\overline{\text{BUSACK}}$	O	External Bus Acknowledge	45
P4.5		I/O	I/O Handshake Port 4	45
P4.6	INT5	I	External interrupt 5	46
P4.6	T0OUTB	O	MF Timer 0 output B	46

PIN DESCRIPTION (Continued)

Table 1. ST9054 I/O Port Alternate Function Summary (Continued)

I/O PORT Port.bit	Name	Function IN/OUT	Alternate Function	Pin Number
P4.6		I/O	I/O Handshake Port 4	46
P4.7	T0OUTA	O	MF Timer 0 output A	47
P4.7	$\overline{\text{BUSREQ}}$	I	External Bus Request	47
P4.7		I/O	I/O Handshake Port 4	47
P5.0		I/O	I/O Handshake Port 5	6
P5.1		I/O	I/O Handshake Port 5	5
P5.2		I/O	I/O Handshake Port 5	4
P5.3		I/O	I/O Handshake Port 5	3
P5.3	P/$\overline{\text{D}}$	O	Program/Data space select	3
P5.4	T1OUTA	O	MF Timer 1 output A	2
P5.4		I/O	I/O Handshake Port 5	2
P5.5	T1OUTB	O	MF Timer 1 output B	1
P5.5		I/O	I/O Handshake Port 5	1
P5.6	T3OUTA	O	MF Timer 3 output A	84
P5.6		I/O	I/O Handshake Port 5	84
P5.7	T3OUTB	O	MF Timer 3 output B	83
P5.7		I/O	I/O Handshake Port 5	83
P6.0	A0	O	Address bit 0 (non mux)	19
P6.1	A1	O	Address bit 1 (non mux)	20
P6.2	A2	O	Address bit 2 (non mux)	21
P6.3	A3	O	Address bit 3 (non mux)	22
P6.4	A4	O	Address bit 4 (non mux)	23
P6.5	A5	O	Address bit 5 (non mux)	24
P6.6	A6	O	Address bit 6 (non mux)	25
P6.7	A7	O	Address bit 7 (non mux)	26
P7.0	AIN0	I	A/D Analog input 0	64
P7.0	ADTRG	I	A/D conversion trigger	64
P7.0	WRRDY4	I	Handshake Write Ready P4	64
P7.0	RX0CKIN	I	SCI0 Receive Clock input	64
P7.0	WDIN	I	T/WD input	64
P7.0	BSH_EN1	I	Bank Switch High Nibble Enable	64
P7.1	AIN1	I	A/D Analog input 1	65
P7.1	RDRDY4	O	Handshake Read Ready P4	65
P7.1	SDI	I	SPI Serial Data In	65
P7.1	T0INB	I	MF Timer 0 input B	65
P7.2	AIN2	I	A/D Analog input 2	66
P7.2	CLK0OUT	O	SCI0 Byte Sync Clock output	66

PIN DESCRIPTION (Continued)

Table 1. ST9054 I/O Port Alternate Function Summary (Continued)

I/O PORT Port.bit	Name	Function IN/OUT	Alternate Function	Pin Number
P7.2	TX0CKIN	I	SCI0 Transmit Clock input	66
P7.2	BSL_EN1	I	Bank Switch Low Nibble Enable	66
P7.3	AIN3	I	A/D Analog input 3	67
P7.3	P/$\overline{D}$	O	Program/Data space select	67
P7.3	T0INA	I	MF Timer 0 input A	67
P7.4	AIN4	I	A/D Analog input 4	68
P7.5	AIN5	I	A/D Analog input 5	69
P7.6	AIN6	I	A/D Analog input 6	70
P7.7	AIN7	I	A/D Analog input 7	71
P8.0	WRRDY5	I	Handshake Write Ready P5	61
P8.0	T3INA	I	MF Timer 3 input A	61
P8.1	RDRDY5	O	Handshake Read Ready P5	60
P8.1	T1INB	I	MF Timer 1 input B	60
P8.2	INT1	I	External interrupt 1	79
P8.2	T1OUTA	O	MF Timer 1 output A	79
P8.2	$\overline{WRSTB5}$	O	Handshake Write Strobe P5	79
P8.3	INT3	I	External interrupt 3	78
P8.3	T1OUTB	O	MF Timer 1 output B	78
P8.3	$\overline{RDSTB5}$	I	Handshake Read Strobe P5	78
P8.4	T1INA	I	MF Timer 1 input A	77
P8.4	$\overline{WAIT}$	I	External Wait input	77
P8.4	WDOUT	O	T/WD output	77
P8.5	P/$\overline{D}$	O	Program/Data space select	76
P8.5	T3INB	I	MF Timer 3 input B	76
P8.6	INT7	I	External interrupt 7	75
P8.6	T3OUTA	O	MF Timer 3 output A	75
P8.7	NMI	I	Non-Maskable Interrupt	74
P8.7	T3OUTB	O	MF Timer 3 output B	74
P8.7	ROMless	I	ROMless Select (Mask Option)	74
P9.0	S1OUT	O	SCI1 Serial Output	56
P9.1	T0OUTB	O	MF Timer 0 output B	57
P9.1	S1IN	I	SCI1 Serial Input	57
P9.2	CLK1OUT	O	SCI1 Byte Sync Clock output	58
P9.2	TX1CKIN	I	SCI1 Transmit Clock input	58
P9.3	RX1CKIN	I	SCI1 Receive Clock input	59
P9.3	T0OUTA	O	MF Timer 0 output A	59

PIN DESCRIPTION (Continued)

Table 1. ST9054 I/O Port Alternate Function Summary (Continued)

I/O PORT Port.bit	Name	Function IN/OUT	Alternate Function	Pin Number
P9.4	S0OUT	O	SCI0 Serial Output	60
P9.5	S0IN	I	SCI0 Serial Input	61
P9.5	$\overline{\text{BUSACK}}$	O	External Bus Acknowledge	61
P9.6	INT2	I	External interrupt 2	62
P9.6	SCK	O	SPI Serial Clock	62
P9.6	WRSTB4	O	Handshake Write Strobe P4	62
P9.7	INT6	I	External interrupt 6	63
P9.7	SDO	O	SPI Serial Data Out	63
P9.7	$\overline{\text{RDSTB4}}$	I	Handshake Read Strobe P4	63

ST9054 CORE

The Core or Central Processing Unit (CPU) of the ST9054 includes the 8 bit Arithmetic Logic Unit and the 16 bit Program Counter, System and User Stack Pointers. The microcoded Instruction Set is highly optimised for both byte (8 bit) and word (16 bit) data, BCD and Boolean data types, with 14 addressing modes. Two 8 bit I/O ports are connected to the Core module for external memory interfacing, while a 16 bit Timer/Watchdog gives system security and timing functions, and a Serial Peripheral Interface allows for synchronous communication. Three independent buses are controlled by the Core, a 16 bit Memory bus, an 8 bit Register addressing bus and a 6 bit Interrupt/DMA bus connected to the interrupt and DMA controllers in the on-chip peripherals and the Core. This multiple bus architecture allows a high degree of pipelining and parallel operation within the ST9054, giving it its efficiency in both numerical calculations and communication with the on-chip peripherals.

MEMORY

The memory of the ST9054 is functionally divided into two areas, the Register File and Memory. The Memory may optionally be divided into two spaces, each having a maximum of 65,536 bytes. The Memory may be expanded with the Bankswitch logic to give paging of the top 32K bytes of each space to expand the ST9054 addressing capability to 8M bytes in each space. The two memory spaces are separated by function, one space for Program code, the other for Data. The ST9054 32K bytes of on-chip ROM memory is selected at memory addresses 0 through 7FFFh (hexadecimal) in the PROGRAM space. The Data space includes the 1,280 bytes of on-chip RAM at addresses 0 through 04FFh.

Off-chip memory, addressed using the address and data buses (Port 0, Port 1 and Port 6) and may be divided into the Program and Data spaces by the external decoding of the Program/Data select pin (P/$\overline{\text{D}}$) available as an Alternate function. The memory spaces are selected by the execution of the SDM and SPM instructions (Set Data Memory and Set Program Memory, respectively). There is no need to use either of these instructions again until the memory area required is to be changed. This requirement is not necessary in two cases: first, when operating with external stacks (the Data memory is automatically selected) and, secondly, when using the memory indirect to memory indirect post-increment addressing mode (the memory types are specified in the instructions: LDPP, LDPD, LDDP, LDDD).

Either the Data Memory or the Program Memory can be addressed using any of the memory addressing modes.

Program Space

The Program memory space of the ST9054, from the 32K bytes of on-chip ROM memory to the full 64K bytes with off-chip memory expansion is fully available to the User. At addresses greater than the first 32K of program space, the ST9054 executes external memory cycles for instruction fetches. The first 256 memory locations from address 0 to 0FFh (hexadecimal) hold the Reset Vector, the Top-Level

MEMORY (Continued)

Figure 3. Memory Spaces, Bankswitch Disabled

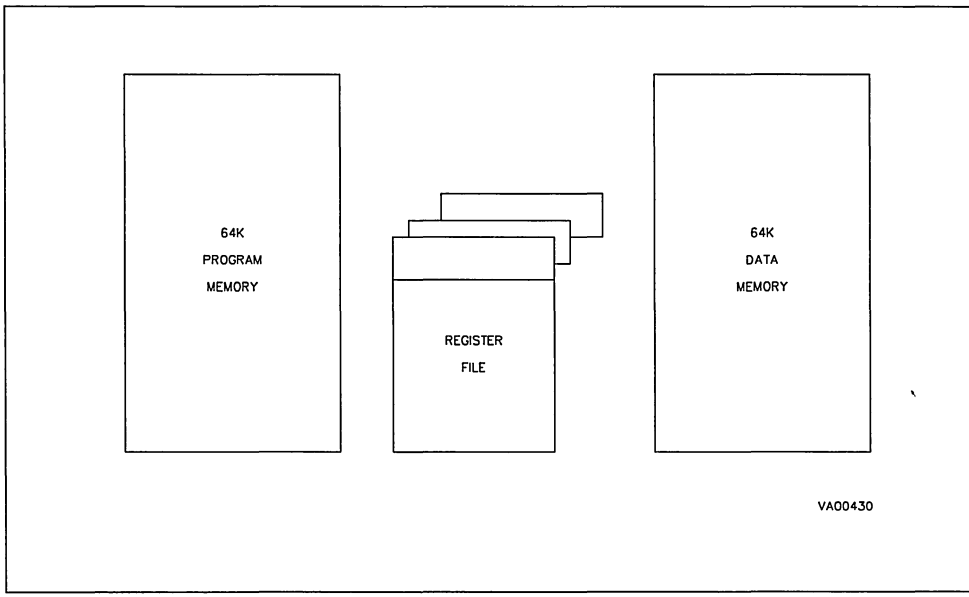
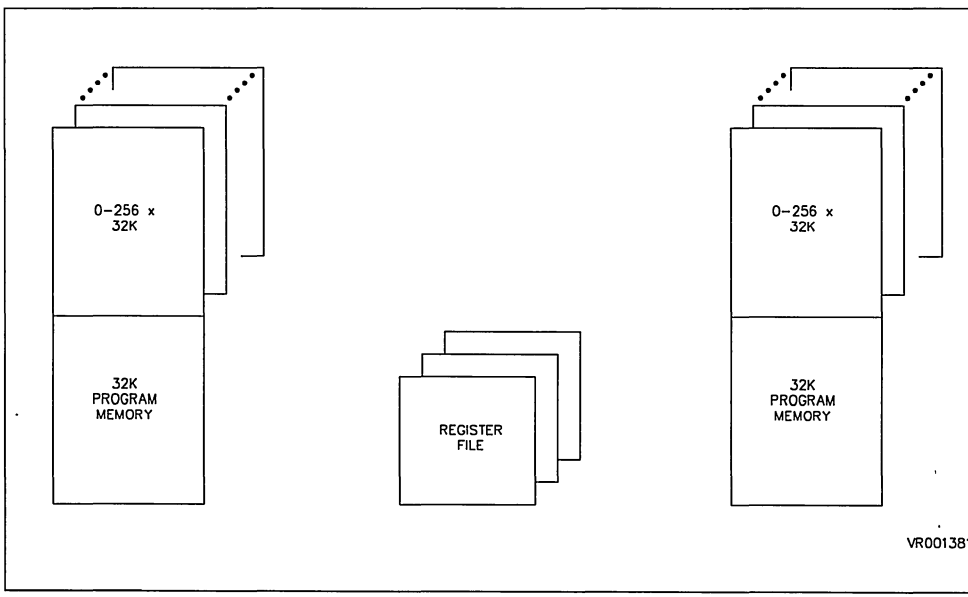


Figure 4. Memory Spaces, Bankswitch Enabled



MEMORY (Continued)

(Pseudo Non-Maskable) interrupt, the Divide by Zero Trap vector and, optionally, the interrupt vector table for use with the on-chip peripherals and the external interrupt sources. Each vector is contained in two consecutive byte locations, the high order address held in the lower (even) byte, the low order address held in the upper (odd) byte, forming the address which is loaded into the Program Counter when selected by the interrupt vector provided by the interrupt source. This should point to the relevant Interrupt Service routine provided by the User for immediate response to the interrupt.

Data Space

The ST9054 addresses the 1,280 bytes of on-chip RAM memory from addresses 0 to 4FFh in the Data Space. It may also address External Data through the External Memory Interface when decoded with the P/$\overline{D}$ pin. The Data Strobe $\overline{DS}$ will not be generated when accessing the internal memory. On-chip general purpose Registers may be used as additional RAM memory for minimum chip count systems.

The Data Space is selected by the execution of the SDM instruction. All subsequent memory references will access the Data Space. When a separate Data Space is not required, data may stored in external RAM or ROM memory within the Program Space.

ROMless Option

In the event of a program revision being required after the development of a ROM-based ST9054, a mask option is available which enables the reconfiguration of the memory spaces to give a fully ROMless device. This means that the on-chip program ROM is disabled and ALL program memory is seen as external, allowing the use of replacement program code in external ROM memory. The on-chip memory in Data space is not affected.

To give the ROMless function (when enabled by the MASK option), the pin selected by mask for ROMless as an Alternate Function should be held to ground (V_{SS}) with a high resistance (eg 100k ohm) during the $\overline{RESET}$ cycle. The pin status is latched on the rising edge of the $\overline{RESET}$ input. After this time, the pin is free for normal operation.

If the ROMless option is enabled, and the on-chip program is to be used, the pin enabled for the ROMless function must to held to a high potential during the $\overline{RESET}$ cycle (eg with a 100k ohm resistor to V_{DD}).

Figure 5. Program Memory Space

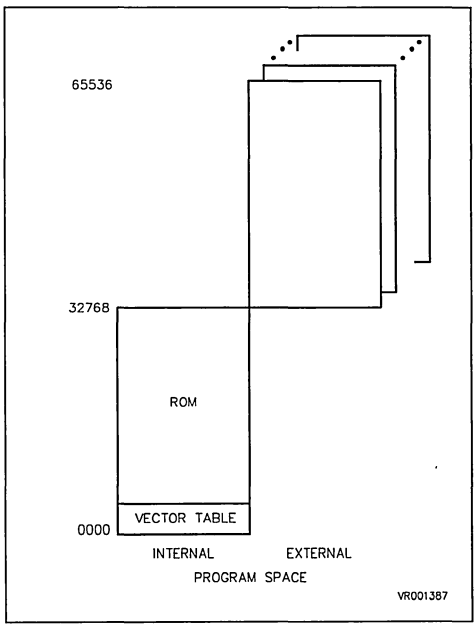
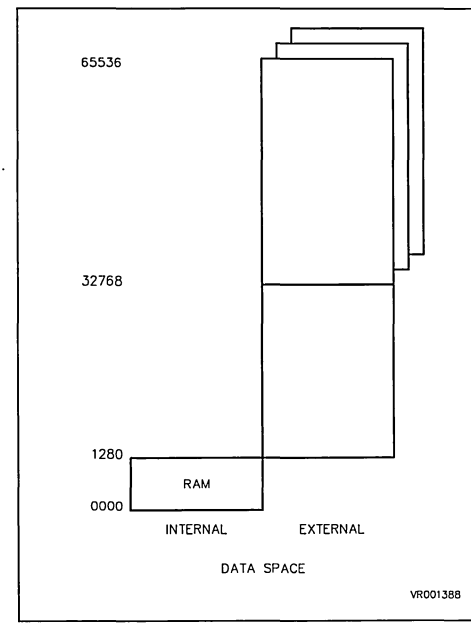


Figure 6. Data Memory Space



REGISTERS

The ST9054 register file consists of 240 registers (224 general purpose) plus pages of 16 registers supporting the configuration and control registers for the on-chip peripherals. The 224 general purpose registers all have 8 and 16 bit arithmetic capability and may be used as accumulators, on-chip RAM, internal Stack areas (for system and/or user stacks), or, with the appropriate addressing modes, as index, offset or stack pointers.

The register file is arranged into 16 groups of 16 registers, where the general purpose registers occupy the first 14 groups. The 15th group, E, contains the system registers and Group F contains the pages of the on-chip peripheral control registers.

Group F is paged in this manner due to the modularity of the ST9 family of microcontrollers. Each member of the family retains all general purpose and system registers, only the paged register groups changing owing to the different on-chip peripheral organizations of each device. The User can therefore generate code libraries which use the general purpose registers knowing that they will not be lost on future ST9 devices. To address a paged register, the Page Pointer (PPR, R234) within the system register group must be loaded with the relevant page number using the SPP instruction. Subsequently any access to registers in the top group (R240-R255) will refer to the selected page. This remains set until the next change to the Page Pointer register (by the SPP instruction).

The System group (Group E, registers RE0 to REF) includes the system and user stack pointers, the Mode register, the ALU FLAG register and the Page pointer register. In addition the data registers for the first 6 I/O ports are present, the configuration registers for the ports being in the paged area. This allows the immediate access to these I/O ports at all times.

Figure 7. Register Grouping

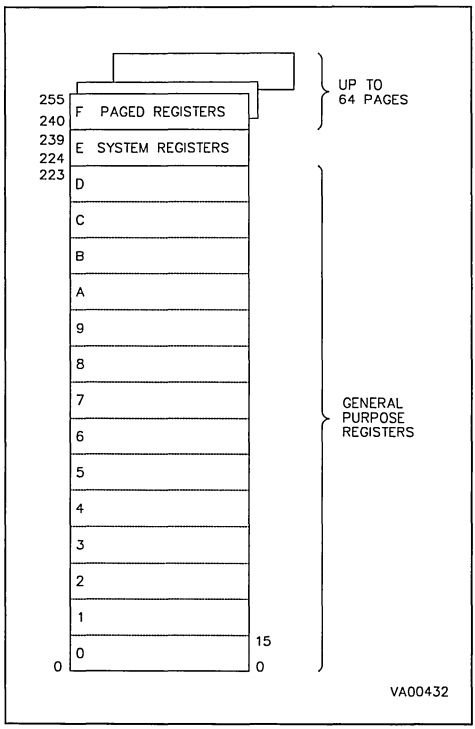
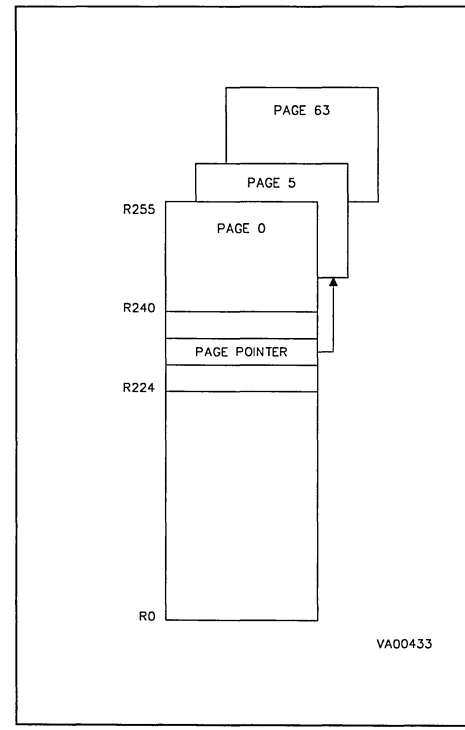
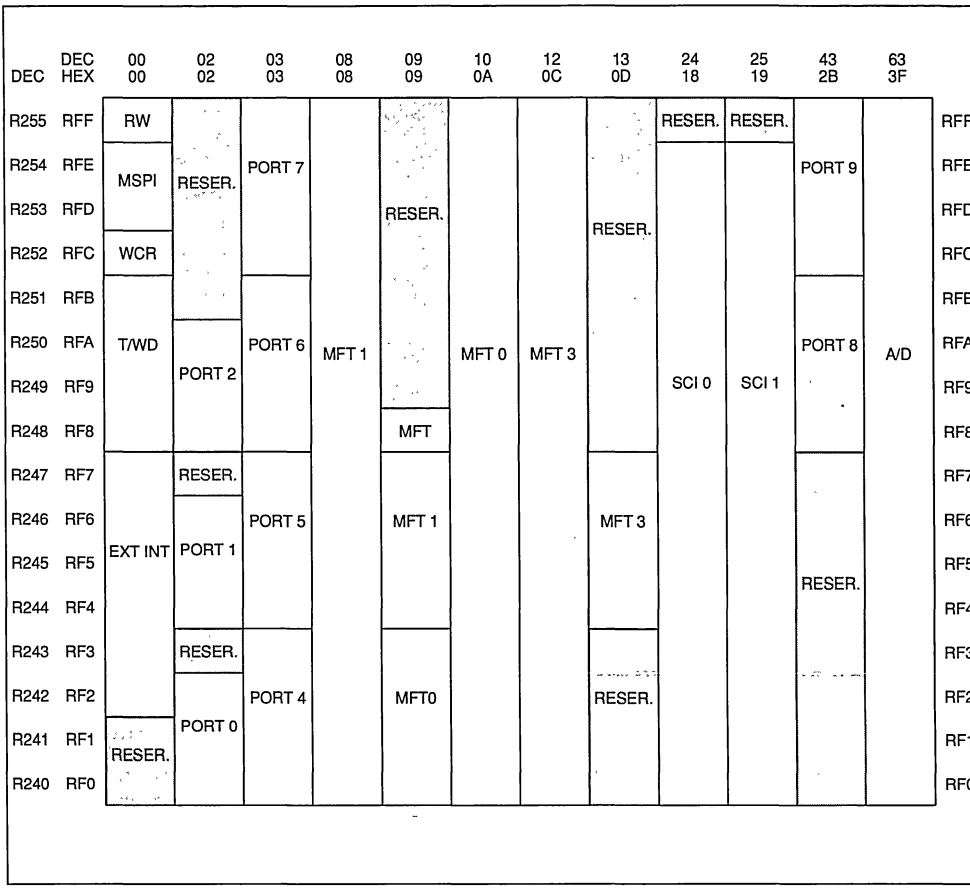


Figure 8. Page Pointer Mechanism



REGISTERS (Continued)

Figure 9. ST9054 Group F Peripheral Organisation



The Register Pointers, present in the system register group, select groups of registers as "Working Registers", which have faster addressing modes than direct Register addressing and allows smaller code size. The Register Pointers may either be used singly, creating a register group of 16 working registers, or as two independent groups of 8 working registers which may be placed at any 8 register boundary within the register file. The single and twin working register modes are automatically set by hardware when the respective `SRP` and either `SRP0` or `SRP1` instructions are executed. If working registers are used as accumulators and RAM locations for particular tasks, fast context switching on interrupts may be achieved by setting the register pointer to another group for the Interrupt Service

REGISTERS (Continued)

Routine, ISR, (e.g. saving the Register pointer on the stack), using the new group in the ISR and subsequently restoring the original group before the Return from Interrupt instruction. Working registers also allow the use of the ABAR - Any Bit-Any Register Boolean operations (including directly on the I/O port data registers).

In the ST9 syntax, directly addressed Registers are indicated with a capital R e.g. R0, R224, RBF, with Register Pairs (16 bit accumulators or memory pointers) as RR0, RR24. When using Working Registers, groups of 16 registers (SRP instruction) are denoted as r0 to r15 (rr0 to rr14), while the dual working register group are addressed as r0 to r7 (rr0 to rr6), for the first group of 8 registers (SRP0), with r8 to r15 (rr8 to rr14) for the second set (SRP1).

Working register addressing requires a 4 bit field within the instruction. When packed into a byte, the upper nibble is set to Dh (1101b), this being the escape code to indicate the use of the working registers. As a result, group D CANNOT be selected with direct register addressing, it is recommended that this group be used as internal stacking area when using register file based system or user stack pointers.

Figure 10. Groupe E Register Map

R239	System Stack Pointer Low (SSPLR)
R238	System Stack Pointer High (SSPHR)
R237	User Stack Pointer Low (USPLR)
R236	User Stack Pointer High (USPHR)
R235	Mode Register (MODER)
R234	Page Pointer (PPR)
R233	Register Pointer 1 (RP1R)
R232	Register Pointer 0 (RP0R)
R231	ALU Flags (FLAGR)
R230	Central Interrupts Control (CICR)
R229	Port 5 Data (P5DR)
R228	Port 4 Data (P4DR)
R227	Port 3 Data (P3DR)
R226	Port 2 Data (P2DR)
R225	Port 1 Data (P1DR)
R224	Port 0 Data (P0DR)

Figure 11. Single Working Register Bank

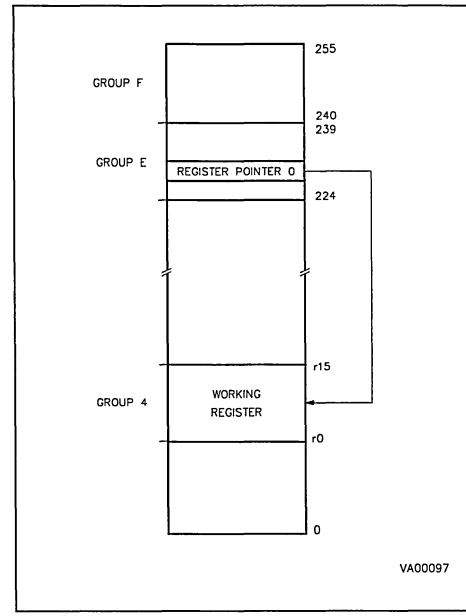
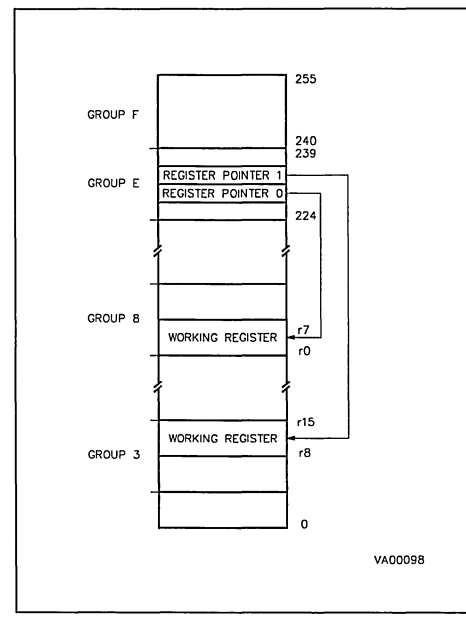


Figure 12. Dual Working Register Banks



STACK POINTERS

There are two separate, double register stack pointers available (System and User), both of which can operate in register or Data memory address spaces. These operate in a Pre-Decrement mode when data is PUSHed onto the Stack and in a Post-Increment mode when data is POPed from the stack.

The SYSTEM Stack Pointer (SSPR, R238:R239) is used for the storage of temporarily suspended system and/or control registers (ie the the Program Counter and FLAG register) while interrupts are being serviced, and is used for the storage of the Program Counter following the CALLing of a subroutine.

The USER Stack Pointer (USPR, R236:R237) is completely free from all interference from automatic operations and so provides for a totally User controlled stack area.

Both Stack pointers may operate with both byte (PUSH,POP) and word (PUSHW,POPW) data, and are differentiated by appending a "U" to the instruction mnemonic for the User Stack (PUSHU/PUSHUW, POPU/POPUW).

When the Stack Pointers are using RAM Memory as the stack areas, a full word register is used as the pointer, while when operating with the stack area within the Register File (Groups 0 to 14 only, but not the within the system and paged groups) only an 8 bit register is required for addressing and consequently only the low byte of the word registers are used (R239 for the System Stack and R237 for the User Stack). In this latter case the upper byte of the stack pointer registers (R238 and R236) must be considered as reserved. The Stack Pointers may be selected to point to RAM or Register file by the setting of the SSP (MODER.7) and USP (MODER.6) of the ST9054 configuration register (MODER, R235) where a "1" denotes Register file operation (Default at Reset) and "0" causes external Data space operation.

Figure 13. Internal Stack Pointers

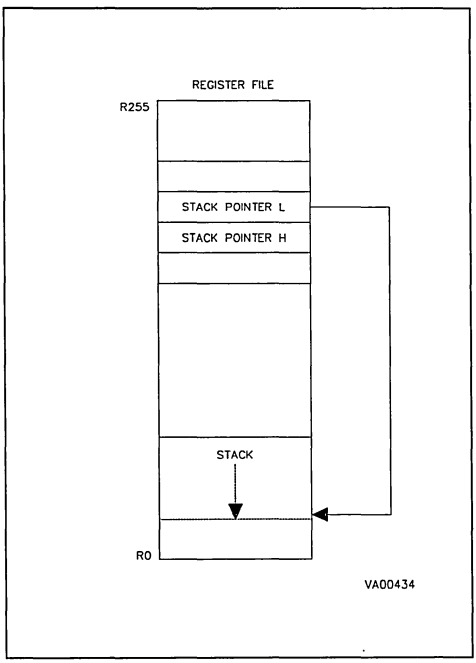
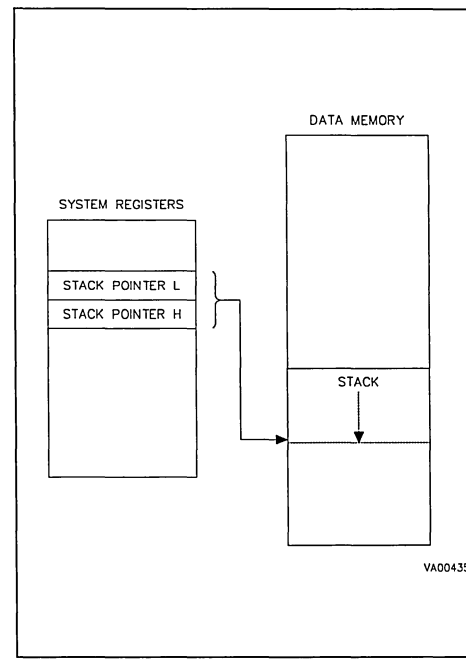


Figure 14. External Stack Pointers



INTERRUPTS

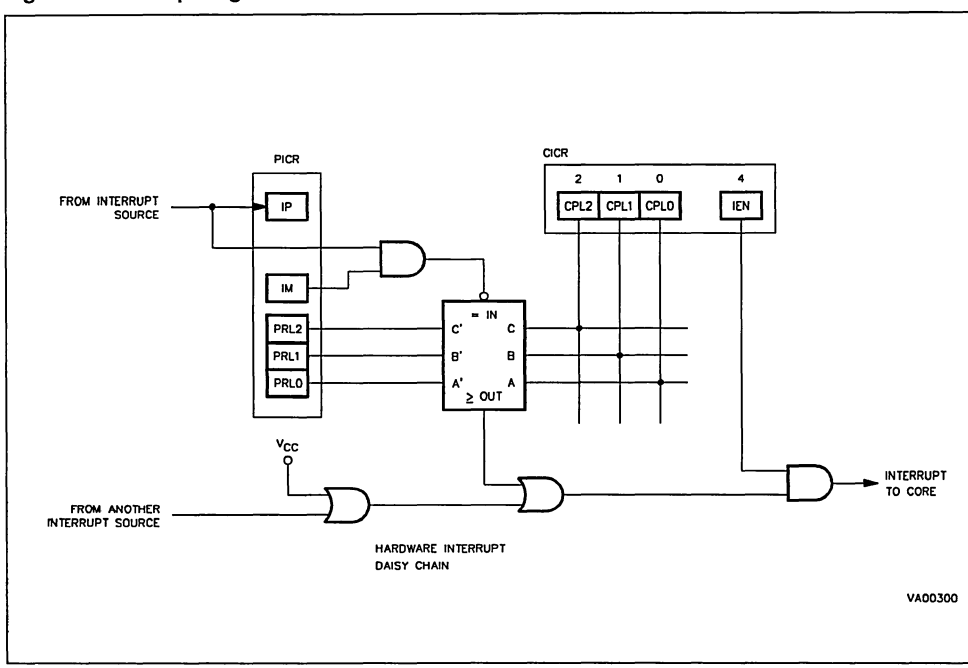
The ST9054 offers a powerful solution to the response requirements of real-time systems with its advanced interrupt structure. Interrupt trigger sources can be prioritized within 8 levels to match the priorities assigned to the application. In addition a top-level or non-maskable interrupt is available.

The ST9054 interrupts follow the logical flow of figure 15.

Interrupt events (selectable with each function) cause the setting of the Interrupt Pending (IP) bit within the status register of the peripheral. This bit may also be set by software in order to generate a software interrupt, and should normally be reset by software within the interrupt service routine. If the interrupt is not Masked with the corresponding Interrupt Mask bit, the interrupt is passed to the central interrupt control logic where the priority level assigned by the User to the interrupt source is compared with the priority level of the core (User programmed dynamically in the 3 bits of the Central Priority register (CPL, CICR.0-2, Level 7 is the lowest priority and level 0 the highest). If the incoming priority level is higher than the CPL, and Global Interrupts are enabled (by the `EI` instruction, interrupts are disabled by the execution of the `DI` instruction), the interrupt is acknowledged. If interrupts are globally disabled, the priority level of the source is lower than or equal to the CPL or the Interrupt is masked, then the IP bit remains set and the interrupt is held pending until the `EI` instruction is executed, the CPL is set to a lower level AND the interrupt is un-masked. Alternatively the IP bit of a masked interrupt source may be used in a polled interrupt environment, with the IP bit being reset by software within the service routine.

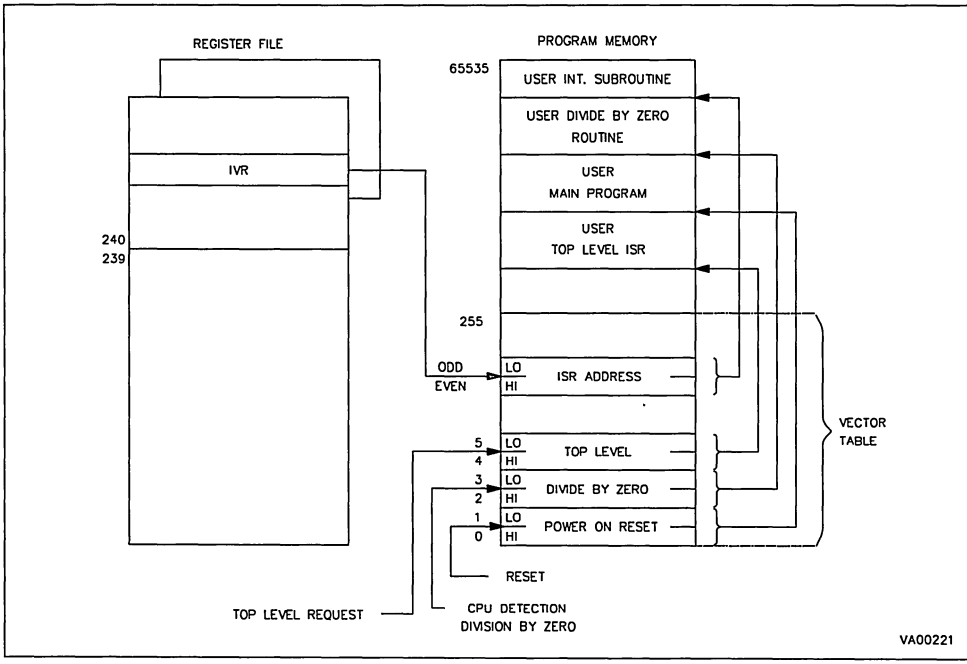
The interrupt acknowledge cycle causes the Program Counter and FLAGS register to be pushed onto the System Stack (PC low byte first, PC high byte, then FLAGS Register) and all maskable interrupts to be disabled by resetting the IEN bit (CICR.4). The peripheral Interrupt Vector, IVR, a User programmable feature of the peripheral interrupt control registers, is used as an offset into the vector table, pointing to the high byte (even address) of the 16 bit address which should contain the starting address of the interrupt service routine. Addresses 0 through 255 of the program space comprise the interrupt vector table. Where multiple

Figure 15. Interrupt Logic



INTERRUPTS (Continued)

Figure 16. Interrupt Vector Table Usage



interrupt sources may occur within a peripheral, the peripheral interrupt vector source may be encoded by hardware set bits within the IVR register. This means that the vector address defined in the peripheral IVR is the base address for a block of vectors servicing that peripheral. The address pointed to by the vector is loaded into the Program Counter and execution restarts from this point.

The interrupt service routine should clear the interrupt pending flag of the interrupt source and take the appropriate action. The last instruction of the interrupt service routine should be the `IRET` instruction, the action of this is to restore the Program Counter and Flags register to their value prior to the interrupt acknowledgment, and to re-enable interrupts. Within the interrupt service routine, use may be made of the working register pointer mechanism to reduce the context switching time.

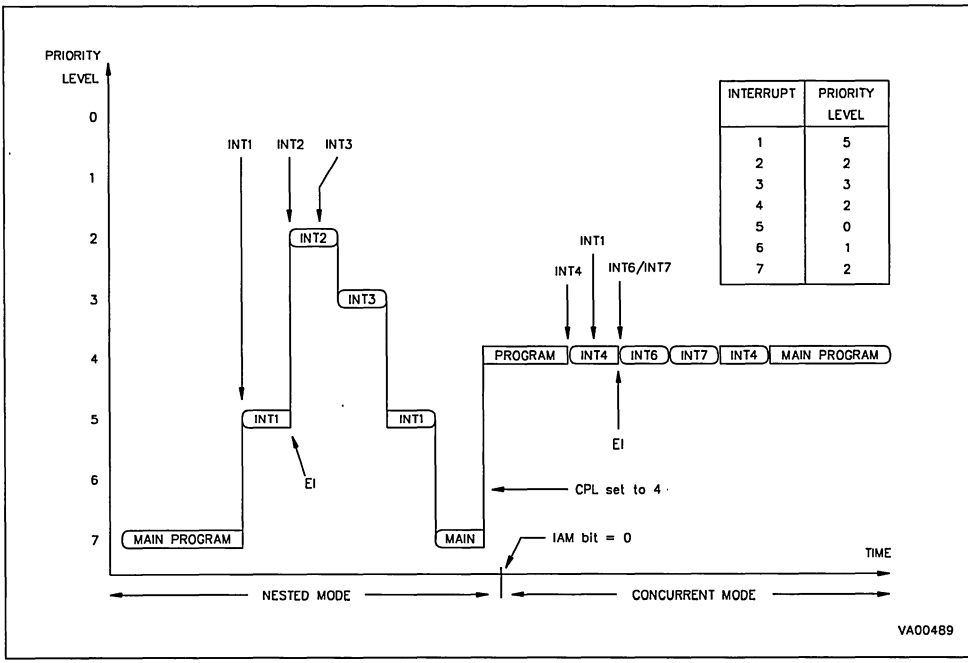
Two interrupt arbitration modes are available for use with the 8 level priority scheme, Nested and Concurrent modes. These are selected by the status of the IAM bit (CICR.3).

Concurrent mode, selected when IAM = "0" (the reset condition) is the standard interrupt arbitration mode, where the arbitration phase of every instruction acknowledges interrupts according to their priority level (if higher than the CPL) and follows the sequence shown. All pending interrupts existing or having eventually occurred during interrupt service routine execution, remain pending until the Enable Interrupt instruction (`EI`) (even if it is executed during the interrupt service routine). `EI` within the interrupt service routine is not recommended for use with the Concurrent arbitration mode as this can trigger a Last In, First Out condition where high priority interrupts are masked by lower priority interrupts which are all higher than the CPL value.

Nested mode, selected when IAM = "1", uses the same arbitration phase as concurrent mode, the difference being that the CPL is modified during the interrupt processing cycle to that of the acknowledged interrupt level. The CPL value is pushed by hardware into the Nested Interrupt Control register (NICR, R247 page 0) by setting the NICR bit corresponding to the CPL value. The interrupt service

INTERRUPTS (Continued)

Figure 17. Interrupt Modes Example of Usage



routine is entered in the normal manner. The revised CPL level is used for arbitration of further interrupts, each higher level being saved on the NICR stack, and being restored automatically by hardware with the `IRET` instruction. This allows the execution of the `EI` instruction within the interrupt service routine to operate the correct nesting of interrupts. The two modes are shown graphically in figure 16, where the Y axis shows the CPL value. It should be noted that in the example INT1 will not be acknowledged until the CPL level is programmed to a lower level.

Interrupts coming from on-chip sources at the same instant, and at the same priority level, are resolved during the arbitration phase according to a hardware daisy-chain. This follows the priorities of the table shown in Table 2.

Table 2. ST9054 Interrupt Hardware Daisy Chain

INTA	High Priority
INTB	
INTC	
INTD	
MFTIMER0	
SCI 0	
SCI 1	
A/D	
MFTIMER3	
MFTIMER1	Lowest Priority

INTERRUPTS (Continued)

External Interrupts. Up to 8 external interrupts are available on the ST9054 as alternate function inputs of I/O pins. These may be selected to be triggered on rising or falling edges and can be independently masked. The eight external interrupt sources are grouped into four pairs or channels which can be assigned to independent interrupt priority levels. Within each channel the even interrupt number takes the even priority level and the odd channel the odd priority level (even+1).

Table 3. External Interrupt Channel Grouping

External Interrupt	Channel
INT7 INT6	INTD1 INTD0
INT5 INT4	INTC1 INTC0
INT3 INT2	INTB1 INTB0
INT1 INT0	INTA1 INTA0

Several of the External Interrupt channels have their inputs selectable between the external interrupt source and on-chip peripheral sources.

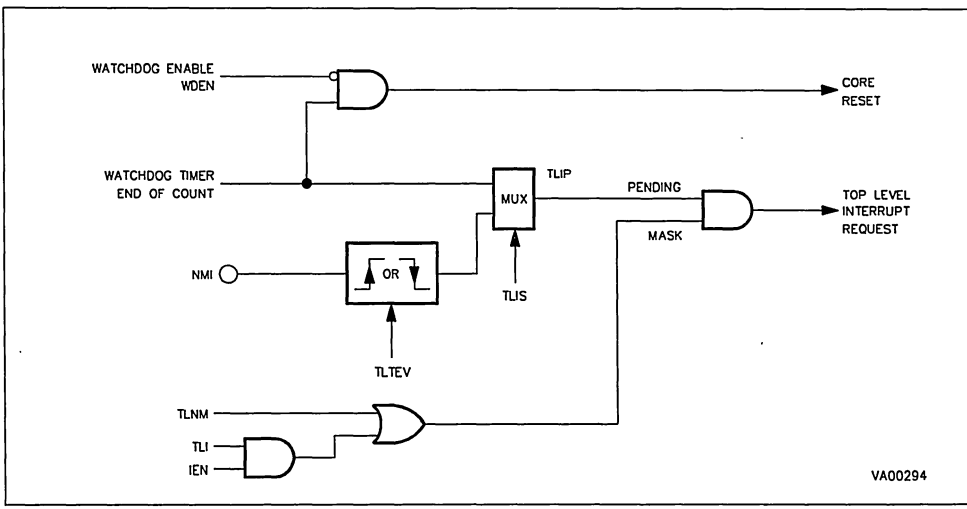
Table 4. ST9054 External Interrupt Souce Selection

INT0	INTA0
Timer/Watchdog End of Count	
INT2	INTB0
SPI Interrupt	

Top Level Interrupt. The Top Level Interrupt channel can be assigned either to the external NMI pin or to the Timer/Watchdog output. When selected as the external NMI pin, the active edge may be programmed to be rising or falling. The TLI event will cause the setting of the TLIP bit (CICR.6) and according to the mask situation, a Top Level Interrupt request may be generated. Two masking conditions are available, a Maskable Mask and a Not-Maskable Mask.

The Maskable Top Level Interrupt.may be enabled or disabled by software and follows the state of the Global Interrupt Enable bit IEN (CICR.4), while the Not-Maskable Mask bit (TLI, CICR.5) is a set-only mask. Once set, the Top Level Interrupt is active independently of IEN and cannot be disabled until the next Reset cycle.

Figure 18. Top-Level Interrupt Structure



DMA

The ST9054 has on-chip DMA channels to provide high-speed data transaction between peripherals and Memory or Register File. Multi-channel DMA is fully supported because each peripheral can have its own DMA channel(s). Each DMA channel transfers data to/from contiguous locations of the Register File, Program Memory or Data Memory. The maximum number of transactions that each DMA channel can perform is 222 if the Register File is selected and 65536 if Program or Data Memory are selected.

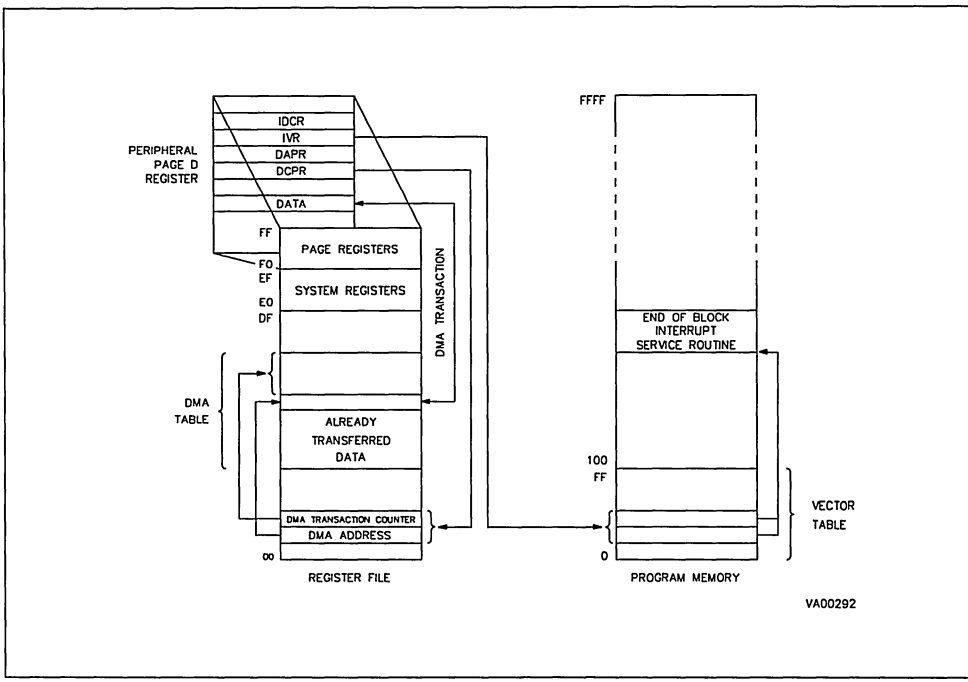
DMA transfer to (or from) the Register File takes 8 INTCLK cycles, DMA transfer to (or from) Memory takes 16 INTCLK cycles. If the ST9054 is in the idle mode (following the execution of the WFI instruction), DMA requests are acknowledged according to their priority and control is returned to the idle mode pending an interrupt, this operation increases the number of INTCLK cycles by 2 for both Register File and Memory DMA transactions.

Each DMA channel has its own control registers located in the page(s) related to the peripheral. There are two pointer registers, DAPR which points to a register or register pair containing the current DMA address to/from which data will be transferred, and DCPR, which points to a register or register pair which contain the transaction counter for the DMA operations. Each DMA transfer consists of three operations:

- A load from/to the peripheral data register to/from a location of Register File (or Memory) addressed through the DMA Address Register (or Register Pair)
- A post-increment of the DMA Address Register (or Register Pair)
- A post-decrement of the DMA transaction counter, which contains the number of transactions that have still to be performed.

When the transaction counter reaches 0 (all data has been transferred) an End of Block Interrupt event is generated to allow the processing of the DMA data block, or, by reloading the Address and counter registers and retriggering, a repeated DMA cycle.

Figure 19. DMA Between Registers and Peripheral

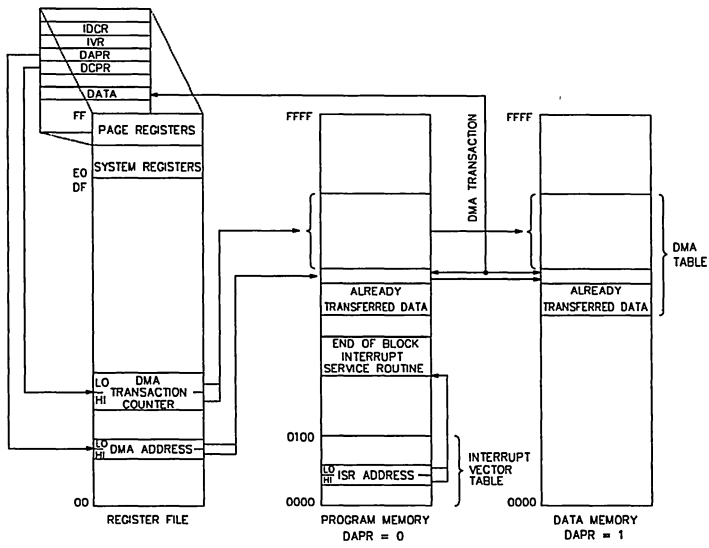


DMA (Continued)

A SWAP mode, allowing continuous DMA operation, is available for the Multifunction Timer and is described in the section relating to the Multifunction Timer.

The ST9054 has DMA channels associated with the Serial Communications Interface Input and Output Serial data channels; the 16 bit Load/Capture Register 0, CAPT0R, of each Multifunction Timer, allowing the timing of external signals to be captured into a table for off-line analysis or for the automatic output of PWM signals of variable width and timing; and the 16 bit Comparison Register 0, COMP0R, of each Multifunction Timer which can be programmed to cause output or input of parallel data through the handshake ports under DMA.

Figure 20. DMA Between Memory and Peripheral



CLOCK GENERATION, WAIT, HALT AND RESET

Clock Generation

The ST9054 Clock Generator module generates the internal clock for the ST9 core and the on-chip peripherals, it may be driven by an external quartz crystal circuit, connected to the OSCIN and OSCOUT pins, or by an external pulse generator connected to OSCIN (figure 21, figure 22).

The conceptual schematic of the ST9 internal clock circuit is shown in figure 23.

The maximum external frequency of the ST9 is 24 MHz, while the maximum internal operating frequency is 12 MHz, thus a programmable divide by two circuit is present, this allows the use of high frequency crystals for economy, or low frequency crystals for reduction in radiated noise. This divider is active upon exit from the reset condition, the User may bypass the divide by two circuit by setting the DIV2 bit (MODER.5). The resulting clock from this section is named INTCLK, the internal clock which drives the timebases of the on-chip clock for the ST9054 peripherals (eg the Multifunction Timer,

Figure 21. Crystal Oscillator

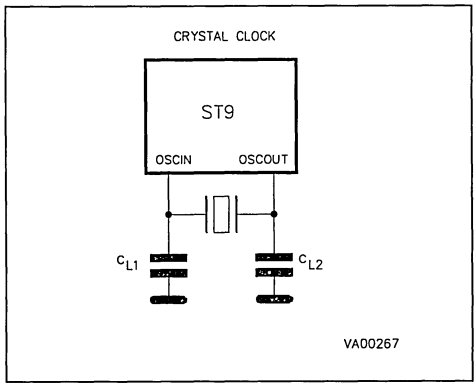


Figure 22. External Oscillator

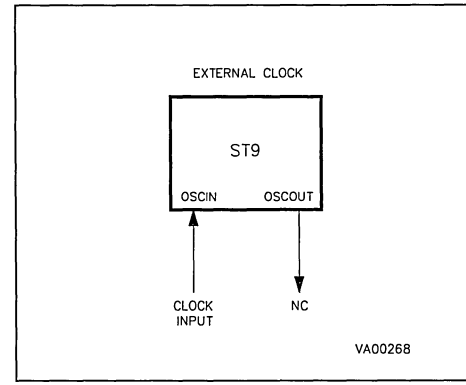
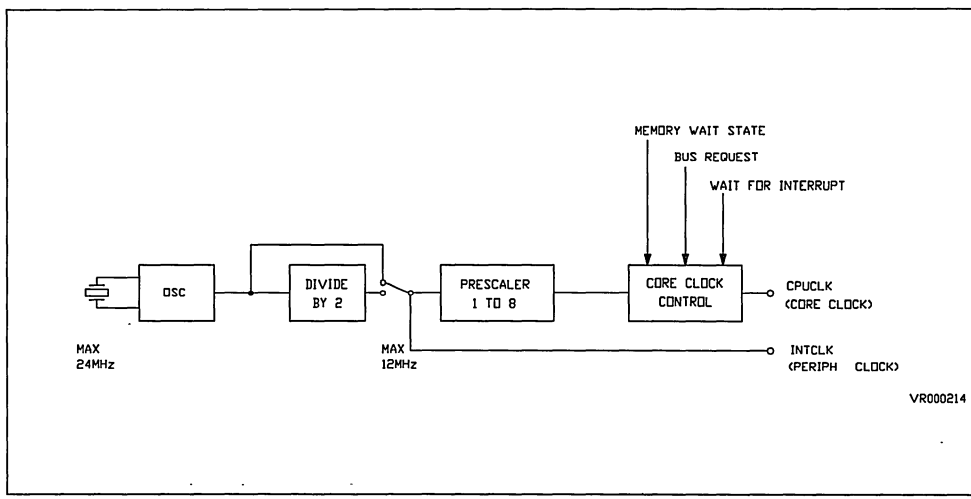


Figure 23. Internal Clock Circuit



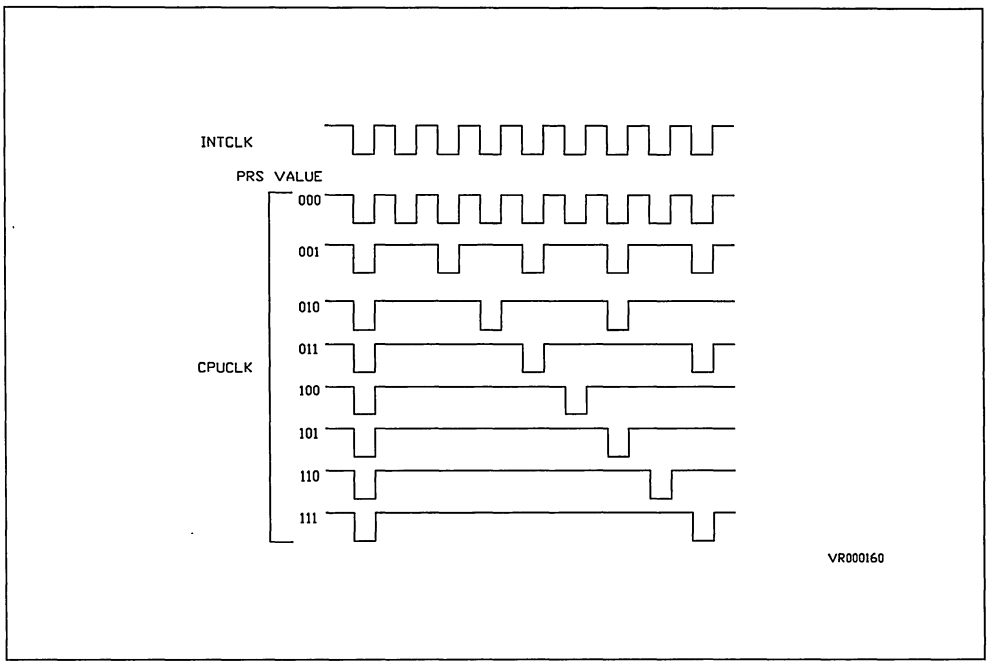
CLOCK GENERATION, WAIT, HALT AND RESET (Continued)

Timer/Watchdog, Serial Communications Interface) and also the input of the CPU prescaler section. The CPU of the ST9 includes the instruction execution logic and may run at different rates according to the setting of the PRS2,PRS1 and PRS0 bits (MODER.4-2) (figure 24). The resulting clock is named CPUCLK and it should be noted that this does not maintain a 50% duty cycle, but stretches the high level of the clock until completion. The CPUCLK prescaler allows the User to slow down the program execution time (eg for lower power consumption), while time-critical sections of the program may tune the CPUCLK execution speed to high speed and then restore it to its original speed.

Wait States

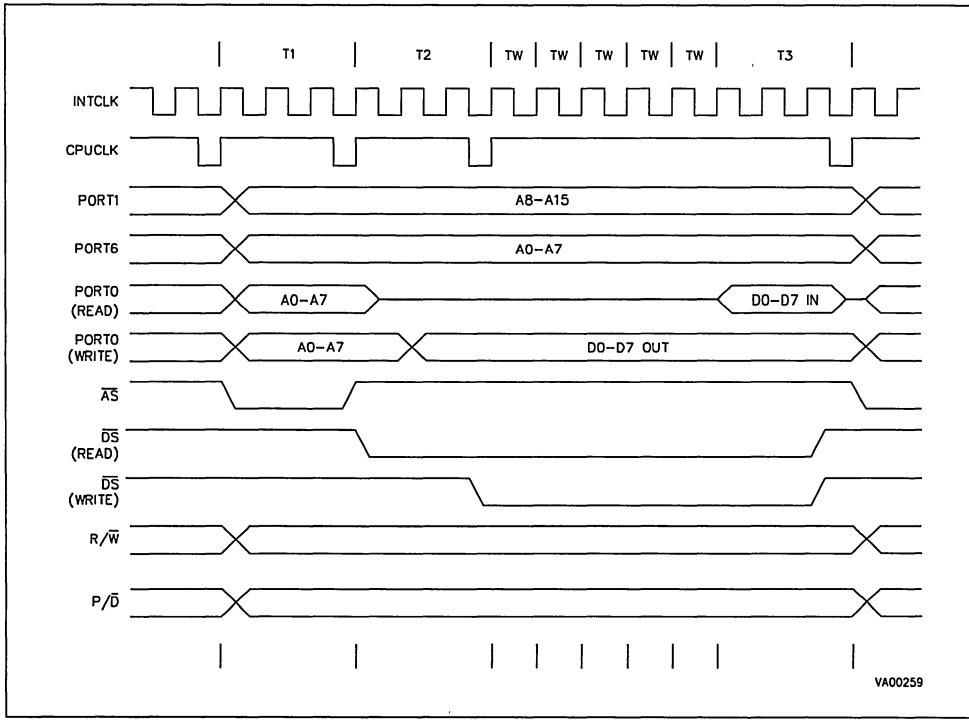
The output from the prescaler can also be affected by wait states. Wait states from two sources allow the User to tailor timing for slow external memories or peripherals. The internal Wait State generator will insert from 0 to 7 wait states, independently programmable for both Program and Data Spaces, via the Wait Control Register WCR (R252, page 0). The second source of wait states is the external Wait input pin when enabled as the Alternate Function. Fig 25 shows the External Memory Interface timing as it relates to CPUCLK prescaling of 2 and 5 added wait states. The added wait states are derived from the INTCLK clock cycle, not CPUCLK. Internal memory is always accessed with no Wait states.

Figure 24. CPUCLK Prescaler



CLOCK GENERATION, WAIT, HALT AND RESET (Continued)

Figure 25. External Memory Interface Timing with CPUCLK Prescaling and 5 Added Wait States

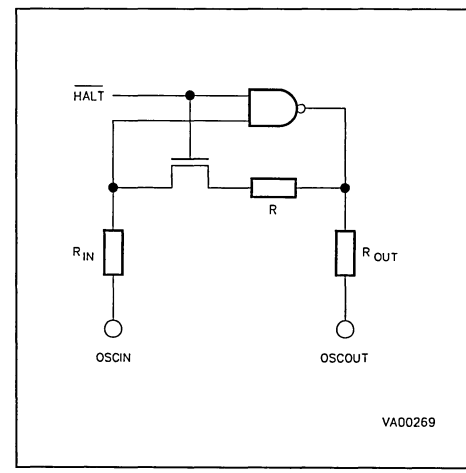


Halt and Wait for Interrupt (WFI) States

The schematic of the on-chip oscillator circuit is shown in figure 26. The HALT condition, caused by the execution of the HALT instruction, disables the oscillator, forcing OSCOUT high. This places the ST9054 into the lowest power mode. The exit of the HALT condition and the restarting of the oscillator requires a RESET pulse with a minimum duration of 10ms (figure 27). It must be noted that if the TIMER/WATCHDOG has the WATCHDOG mode enabled, a HALT instruction will not disable the oscillator; this is to avoid stopping the Watchdog if, by an error, a HALT instruction is executed. If this occurs, the ST9054 runs in an endless loop terminated only by the Watchdog reset (or hardware reset).

The WFI (Wait for Interrupt) instruction suspends program execution until an interrupt request is acknowledged. During this period, DMA transactions are allowed if their priority is higher than or equal to the CPL level; the ST9054 returns to WFI

Figure 26. Oscillator Schematic



CLOCK GENERATION, WAIT, HALT AND RESET (Continued)

mode after completion of the DMA transfer. The CPUCLK is halted during Wait For Interrupt while INTCLK continues to run, thus the power consumption of the processor is lowered by the CORE power consumption value.

The External Memory Interface lines status during HALT and WFI modes is shown in Table 5.

Table 5. External Memory Interface Line Status During WFI and Halt

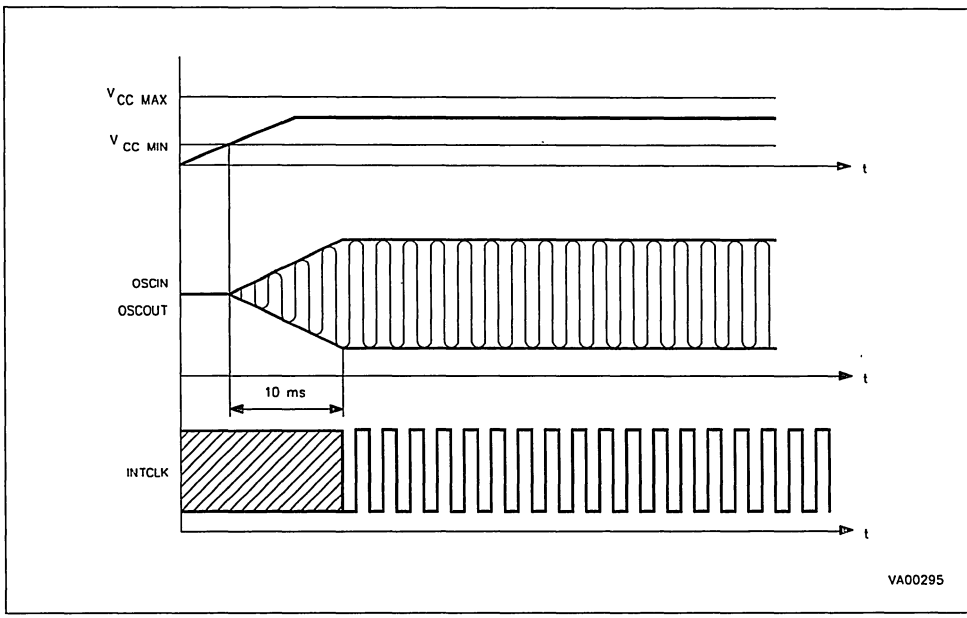
P0 (AD0-AD7)	High Impedance
P1 (A8-A15)	Forced to Address of Next Opcode
$\overline{AS}$	Forced High
$\overline{DS}$	Forced High
R/$\overline{W}$	Forced High

Reset

The processor Reset overrides all other conditions and forces the ST9054 to the reset state. During Reset, the internal registers are set to their Reset values, as shown in Table 6 for the system and Page 0 Registers. The I/O Ports pins are set to the Bidirectional Weak Pull-up mode. The User must then initialize the ST9054 registers to give the required functions.

The Reset condition can be generated from the external $\overline{RESET}$ pin or by the on-chip TIMER/WATCHDOG operating in Watchdog mode. To guarantee the complete reset of the ST9054, the $\overline{RESET}$ input pin must be held low for at minimum of 53 crystal periods in addition to the crystal start-up period. The Watchdog $\overline{RESET}$ will occur if the Watchdog mode is enabled (WDEN, WCR.6, is reset) and if the programmed period has elapsed without the code 0AAh,55h written to the appropriate register. The input pin $\overline{RESET}$ is not driven low by the on-chip reset generated by the TIMER/WATCHDOG.

Figure 27. Reset Timing Requirements from Halt State



CLOCK GENERATION, WAIT, HALT AND RESET (Continued)

Table 6. System and Page 0 Reset Values

Register Number	System Register Reset Value	Page 0 Register Reset Value
F	(SSPLR) = undefined	Reserved
E	(SSPHR) = undefined	(SPICR) = 00h
D	(USPLR) = undefined	(SPIDR) = undefined
C	(USPHR) = undefined	(WCR) = 7Fh
B	(MODER) = E0h	(WDTCR) = 12h
A	(Page Ptr) = undefined	(WDTPR) = undefined
9	(Reg Ptr 1) = undefined	(WDTLR) = undefined
8	(Reg Ptr 0) = undefined	(WDTHR) = undefined
7	(FLAGR) = undefined	(NICR) = 00h
6	(CICR) = 87h	(EIVR) = x2h
5	(PORT5) = FFh	(EIPLR) = FFh
4	(PORT4) = FFh	(EIMR) = 00h
3	(PORT3) = FFh	(EIPR) = 00h
2	(PORT2) = FFh	(EITR) = 00h
1	(PORT1) = FFh	Reserved
0	(PORT 0) = FFh	Reserved

During the $\overline{\text{RESET}}$ state, $\overline{\text{DS}}$ is held low and $\overline{\text{AS}}$ is toggled with the frequency of the crystal (OSCIN) divided by 32. This condition may be recognized by external peripherals as a Reset condition. It may also be used to enable the synchronization of multiple ST9054 running from the same clock in a multi-processing or high security majority voting system.

Once the Reset pin reaches a logical high, the ST9054 fetches the starting address from locations 0 and 1 of the program space and begins program execution from this address after 67 crystal cycles.

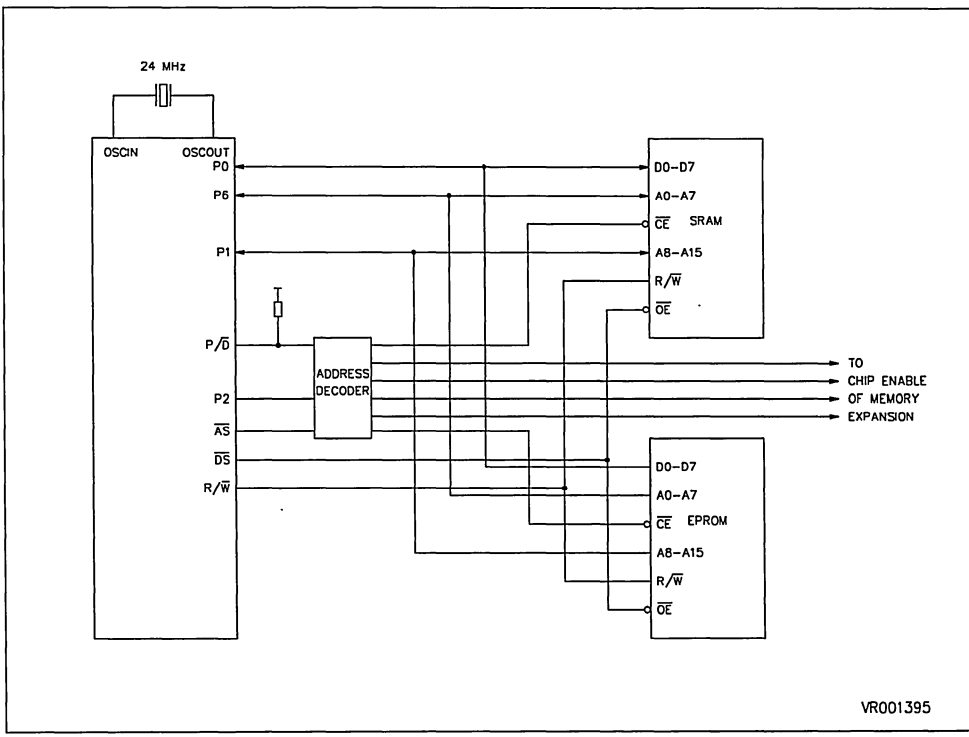
INTERFACING TO EXTERNAL MEMORY

External Memory and/or peripherals may be connected to the ST9054 through its External Memory Interface. This provides the multiplexed Address bits A0 to A7 and Data bits D0 to D7 as Alternative Functions of Port 0, and the higher order address bits A8 to A15 as Alternative Functions of Port 1, giving the full 64K bytes addressing capability. Port 6 is available to be programmed as non-multiplexed address outputs A0 to A7 to reduce the requirement for an external latch to de-multiplex the low order addresses. Port 0, in this case, becomes solely the Data I/O port. The Program/Data (P/$\overline{D}$) output, when selected as an Alternate function, allows external decoding to provide for the two independent pages for Program and Data.

Data transfer timing is generated by the Address strobe $\overline{AS}$ and the data strobe $\overline{DS}$. Address strobe low indicates that the data present on AD0 to AD7 is the low order address and is guaranteed valid on the rising edge of $\overline{AS}$ allowing for latching of the address bits by an external latch (if Port 6 is not used). Data transfer direction is indicated by the status of the Read/Write (R/$\overline{W}$) pin; for write cycles (R/$\overline{W}$ low), data out is valid at the falling edge of $\overline{DS}$; for read cycles (R/$\overline{W}$ high), data in must be valid prior to the rising edge of $\overline{DS}$. The timing of the R/$\overline{W}$ signal may be modified by the setting of the RW bit (bit 0 Register 0FFh, page 0) in order to accomodate different types of external memories. In addition, when the Bank Switch logic is enabled, the timing of the Bank Switch outputs may be modified by software to prevent potential conflicts on the data bus. Please refer to following sections for further details.

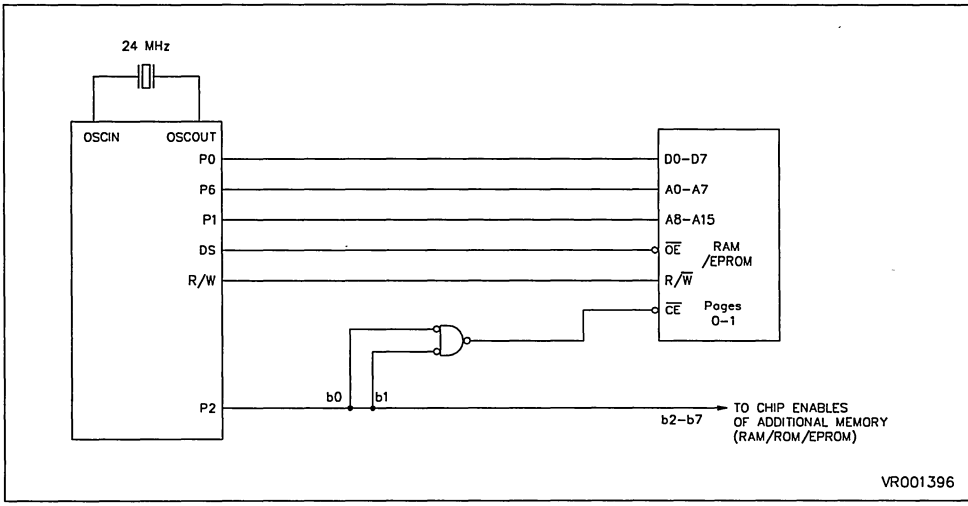
The Data Strobe low period may be extended to accomodate slow external devices by the adding of internally generated wait cycles (0 to 7 cycles for program and/or data memory maps) or by an external input on the WAIT input pin also available as an Alternative Function of an I/O bit. The Data Strobe is not generated when the ST9054 is addressing internal memory. Suggested interface circuits are shown in figures 28 and 29.

Figure 28. External Memory Addressing Circuit



INTERFACING TO EXTERNAL MEMORY (Continued)

Figure 29. External Memory Addressing Circuit



BANKSWITCH LOGIC

Port 2 of the ST9054 may be programmed by the User to become extended address lines allowing expansion of the memory to a maximum of 8M bytes in both program and data pages. This is achieved by paging of the top 32K bytes of memory (A15 high, addresses 8000h to FFFFh), with the lower 32K bytes (A15 low addresses 0000h to 7FFFh) remaining static. The static area, segment 0, allows for the direct access to interrupt service and page change routines, and other common sub-routines, while the paged segments (1 to 256) of 32K bytes may contain additional program code, database entries, printer fonts, buffer space, or any other function requiring a large amount of memory.

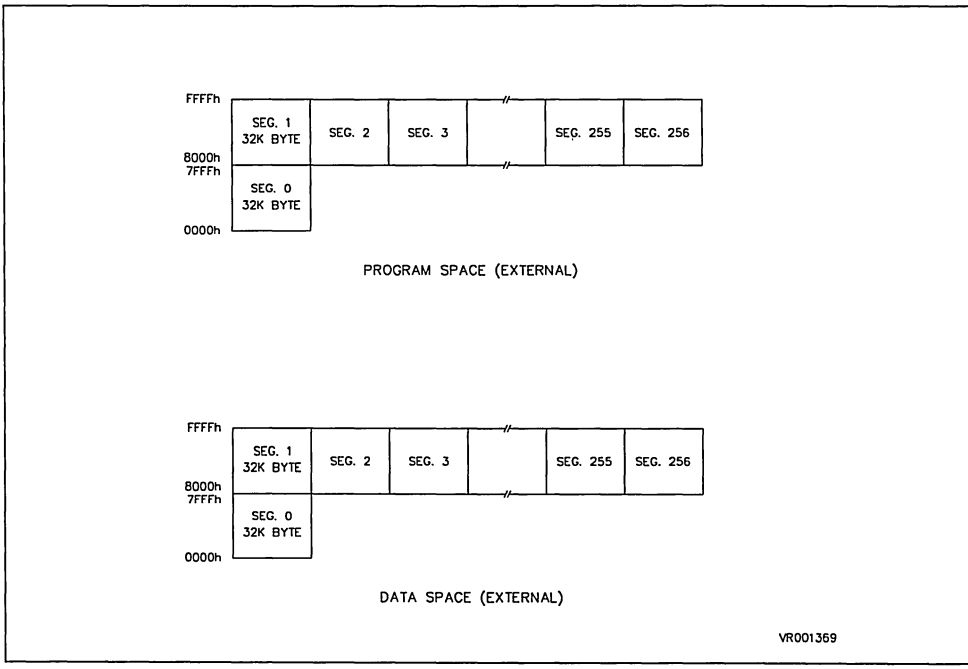
The setting of Port 2 is made during the Reset cycle, by the latched status of the signals BSH_EN1 and BSL_EN1. These control the high and low nibbles of Port 2 between Address Expansion lines and normal I/O lines as shown in Table 7.

Table 7. Port 2 Nibble Programming For Bank Switch and I/O

BSH_EN1	BSL_EN1	BS Port Nibble		BS Port Reset Value
		High	Low	
O	O	I/O	I/O	0FFh
O	I	I/O	BS	0FFh
I	O	I/O	BS	0FFh
I	I	BS	BS	0FFh

In order to program the functions, weak pull-up/down resistors (100k ohm) on the BSH_EN1 and BSL_EN1 designated lines are used to generate the logic level latched on the rising edge of the Reset input. After this event, these lines may be used as I/O and be programmed in the normal way.

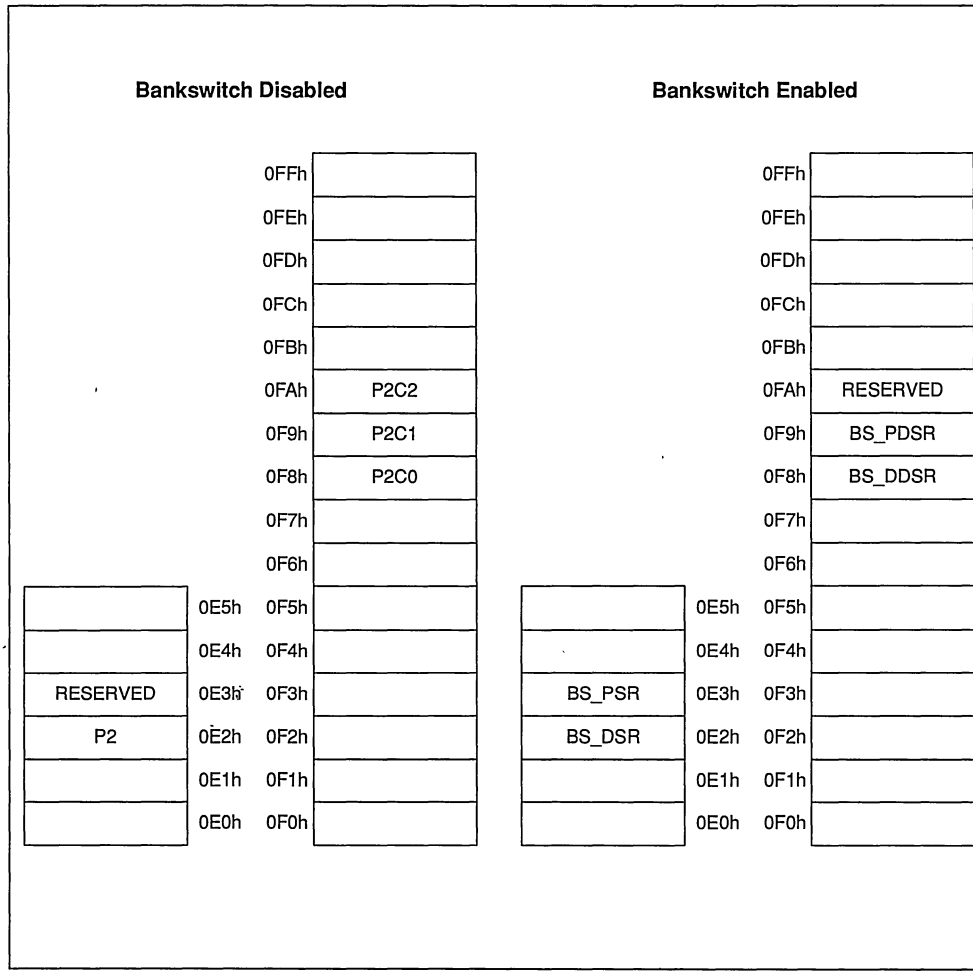
Figure 30. Bank Switch Memory Maps



When the Address Expansion is selected, several I/O port configuration registers take an alternative function. The Port Data Registers for I/O ports 2 and 3 (Registers E2h and E3h) become the Bank Switch Data Segment Register and Bank Switch Program Segment Register respectively. The values held in these registers are output on Port 2 whenever a memory access is made to either data or program spaces with A15 high. This allows Port 2 bits to represent either extended address lines A16 to A23 or to output chip-selects to external memories. For this second option the reset value for these registers, and the value output whenever A15 is low, is 0FEh, generating the selection of a standard "startup" page automatically. Port 2 Configuration registers P2C0 and P2C1 contained in I/O Page 2 hold the User programmed values output on Port 2 for DMA cycles with addresses in the the high 32K byte of the memory for data and program spaces respectively.

BANKSWITCH LOGIC (Continued)

Figure 31. Bank Switch Register Mapping



Warning: The Bankswitch Program DMA register occupies the same register as Port 2 Control Register 2 (P2CR), so caution must be taken in writing to BS_PDSR when the high nibble is used as I/O and the low nibble is used for the Bankswitch output as P2C2 is used for the port configuration. The Program and Data Segment Registers are located in the direct Register file within the System Register group in order to be immediately accessible, while the DMA Segment Registers are held within an I/O page as, once programmed, they do not need constant service.

BANKSWITCH LOGIC (Continued)

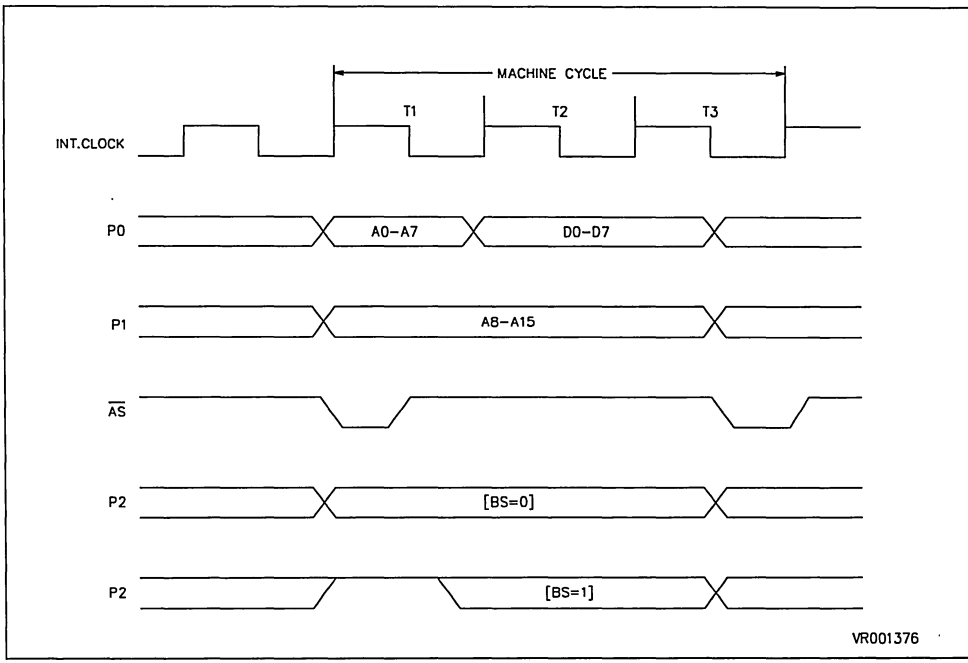
Output Timing

In order to prevent potential bus conflicts on Port 0 (Address/Data multiplexed) during the address strobe time when using the Bankswitch logic, the timing of the Bankswitch outputs may be modified by software. This is achieved by setting to "1" bit 1 of Register 0FFh in I/O page 0. This causes the Bankswitch outputs to be all high during the address strobe period. The reset condition provides normal timing and status.

The timing of the Read/Write signal may be modified as shown in the next figure by setting to "1" bit 0 of Register 0FFh in I/O page 0. This allows the use of different types of external memories. When this bit is "0" (the reset state) normal timing is generated.

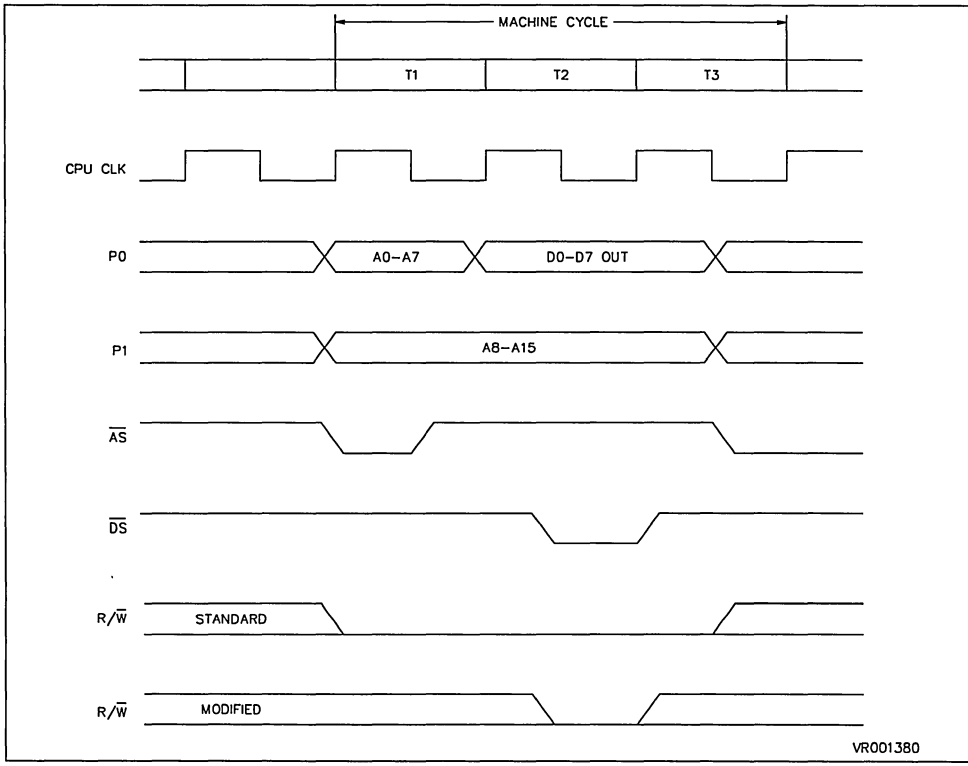
Note: The LST9 ST9 Incremental Linker supports the paging mechanism of the ST9054 and is able to allocate program and data code into specific segments if required.

Figure 32. Bankswitch Output Timing Modification



BANKSWITCH LOGIC (Continued)

Figure 33. R/$\overline{W}$ Output Timing Modification



BUS CONTROL

Multi-processing or external program testing may be accomplished by disabling the I/O ports used for external memory addressing and the associated timing signals.

High Impedance Mode

The User may place the External Memory Interface (I/O Port 0, Port 1 and Port 6, Address Strobe, Data Strobe and Read/Write) into the high impedance state by setting the HIMP bit (MODER.0). External test equipment may then drive the memory lines for automatic test, external memory validation or programming. The ST9 will continue to execute internal programs, providing no external memory is addressed, allowing the execution of security routines without showing externally the addresses used.

Bus Request/Acknowledge

The External Memory Interface address ports and timing signals may be forced to their high impedance state by utilizing the $\overline{\text{BUSREQ}}$, Bus Request, and $\overline{\text{BUSACK}}$, Bus Acknowledge, signals available as Alternate Functions of two I/O pins. The signals, $\overline{\text{BUSREQ}}$ and $\overline{\text{BUSACK}}$, must be enabled by setting the BRQEN bit (MODER.1). Once enabled, a low level detected on the $\overline{\text{BUSREQ}}$ pin at the start of an internal machine cycle will cause the stretching of the CPUCLK, and $\overline{\text{BUSACK}}$ to go low indicating that the External Memory Interface is disabled. The $\overline{\text{BUSREQ}}$ pin is then continuously monitored, and when sampled high, the External Memory Interface pins are driven by the ST9 within two INTCLK cycles.

I/O PORTS

Summary of Function

For the ST9054 84 pin package, only twelve pins have a Reserved function: V_{DD}(x2), V_{SS}(x2), $\overline{RESET}$, $\overline{AS}$, $\overline{DS}$, R/$\overline{W}$, OSCIN, OSCOUT, the Analog to Digital Converter Voltage references. All other pins are available as Input/Output (I/O) for the User, grouped into Ports of 8 bits. These may be programmed to be Input, Output, Bidirectional or Alternate Function (Peripheral or Memory Interface), on a bit by bit basis, at any time. When programmed as an Input the pin may be set to TTL or CMOS input threshold levels, while, when programmed as Output, Push-Pull or Open Drain configuration may be selected. The Bidirectional mode sets the pin with a weak pull-up resistor to V_{DD} or to Open Drain, allowing bidirectional communication with external logic. The Alternate Function setting is predetermined for each pin as shown in the Pin Configuration Table.

The circuitry of the I/O port allows for several ST9054 peripheral functions to address, as Alternate Functions, the same pin, for both input and output, the User selects which peripheral function is to be active by enabling its individual Input or Output function. This multi-function I/O capability of the ST9054 allows for easy adaptation to external circuits. The options available for each bit are summarized in Table 8.

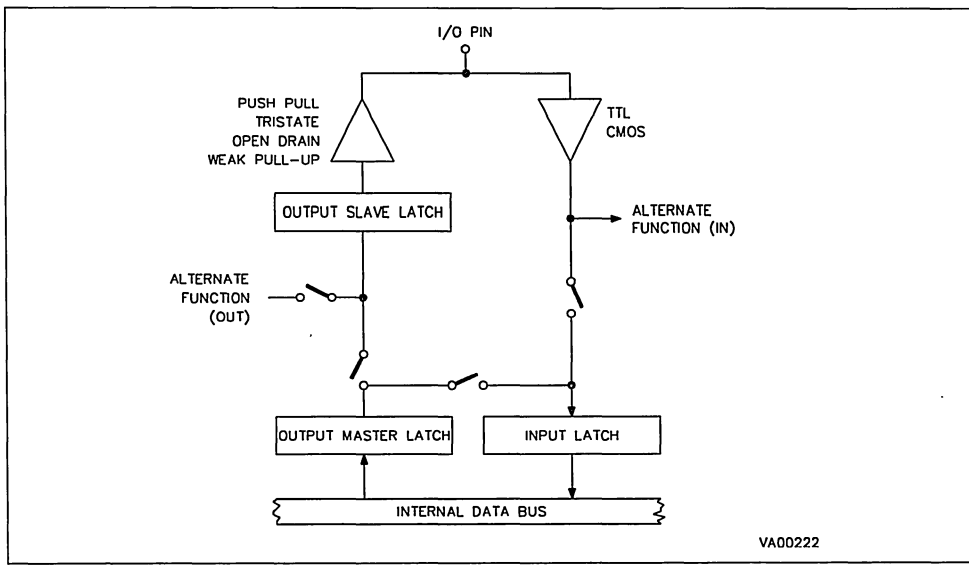
Table 8. I/O Setting Options

Input	TTL Thresholds
	CMOS Thresholds
Output	Open Drain
	Push Pull
Bidirectional	Open Drain
	Weak Pull-up
Alternate Function	Open Drain
	Push Pull

I/O Port Configuration

The configuration of each general I/O bit of the ST9054 is set by the corresponding bits in three I/O Port control registers. These affect the status of the input and output buffers of the pin, and enable the Alternate function Outputs. Alternate Function inputs are always connected, and are used by enabling the function from within the configuration registers of the relevant peripheral function. The configuration of an I/O bit is shown in figure 35.

Figure 34. I/O Port Schematic



I/O PORTS (Continued)

Outputs follow a Master/Slave buffer, data is transferred from the ST9 internal data bus at the beginning of the machine cycle, and, if enabled as output, is passed to the output latch at the end of the cycle. This synchronization allows for the Bidirectional use of the pin without potential conflicts.

Configuration Registers.

Three registers are used to allow the setting of each pin, generically PxC2R, PxC1R, PxC0R, where x relates to the 8 bit I/O port in which the bit is present. The setting of the corresponding bit in each register to achieve the desired functionality of the I/O pin is shown in Table 9.

The effect of the configuration settings of Table 9 on the I/O ports structure is shown in figure 36 to figure 39.

I/O Register Map

The Data Registers which correspond to the pin status (after configuration) of I/O port 0 to 5, are found in Group E of the Register File, for immediate access at all times, while the configuration registers and the Data Registers for Additional Ports are found within I/O pages (Group F) 2, 3 and 43 (2Bh).

Table 9. Port Configuration Status Bits

PxC2n	0	1	0	1	0	1	0	1
PxC1n	0	0	1	1	0	0	1	1
PxC0n	0	0	0	0	1	1	1	1
Pxn Configuration	BID	BID	OUT	OUT	IN	IN	AF	AF
Pxn Output	WP	OD	PP	OD	HI	HI	PP	OD
Pxn Input	TTL	TTL	TTL	TTL	CMOS	TTL	TTL	TTL

Legend :
x = Port
n = Bit
BID = Bidirectional
OUT = Output
IN = Input
AF = Alternate Function
WP = Weak Pull-up
OD = Open Drain
PP = Push Pull
HI = High Impedance

Figure 35. I/O Port Input Configuration

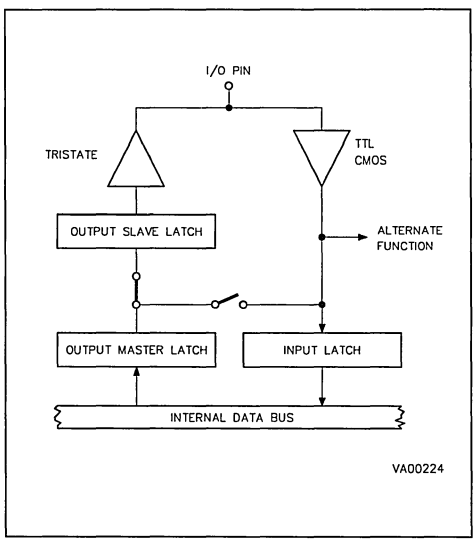
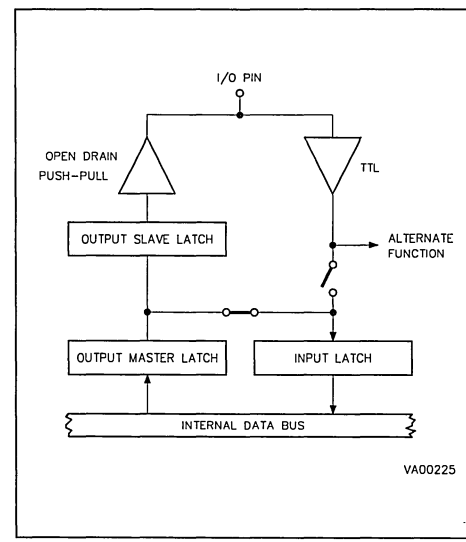


Figure 36. I/O Port Output Configuration



I/O PORTS (Continued)

Figure 37. I/O Port Bidirectional Configuration

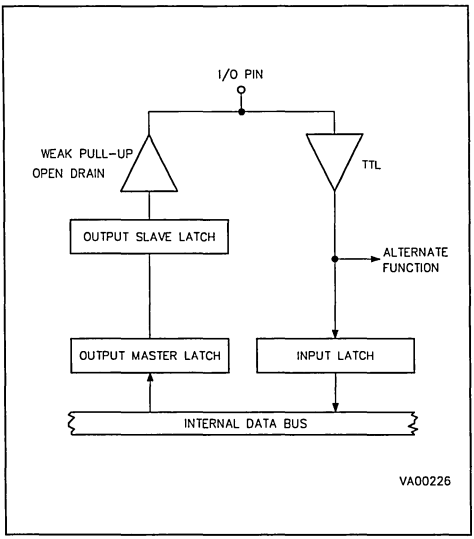


Figure 38. I/O Port Alternate Function Config.

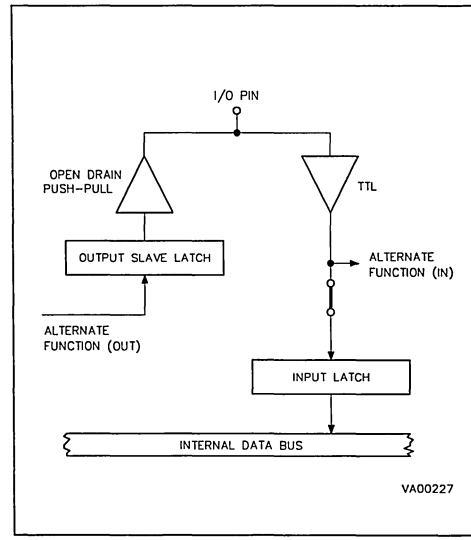


Figure 39. I/O Register Maps

GROUP E			GROUP F		PAGE		
DEC	HEX		DEC	HEX	02	03	43
			R255	RFF	RESERVED	P7D	P9D
			R254	RFE	P3C2	P7C2	P9C2
			R253	RFD	P3C1	P7C1	P9C1
			R252	RFC	P3C0	P7C0	P9C0
			R251	RFB	RESERVED	RESERVED	P8D
			R250	RFA	P2C2	RESERVED	P8C2
			R249	RF9	P2C1	RESERVED	P8C1
			R248	RF8	P2C0	RESERVED	P8C0
			R247	RF7	RESERVED	HDC5	RESERVED
			R246	RF6	P1C2	P5C2	RESERVED
R229	RE5	P5D	R245	RF5	P1C1	P5C1	RESERVED
R228	RE4	P4D	R244	RF4	P1C0	P5C0	RESERVED
R227	RE3	P3D	R243	RF3	RESERVED	RESERVED	RESERVED
R226	RE2	P2D	R242	RF2	P0C2	P4C2	RESERVED
R225	RE1	P1D	R241	RF1	P0C1	P4C1	RESERVED
R224	RE0	P0D	R240	RF0	P0C0	P4C0	RESERVED

I/O PORTS (Continued)

Handshake and DMA

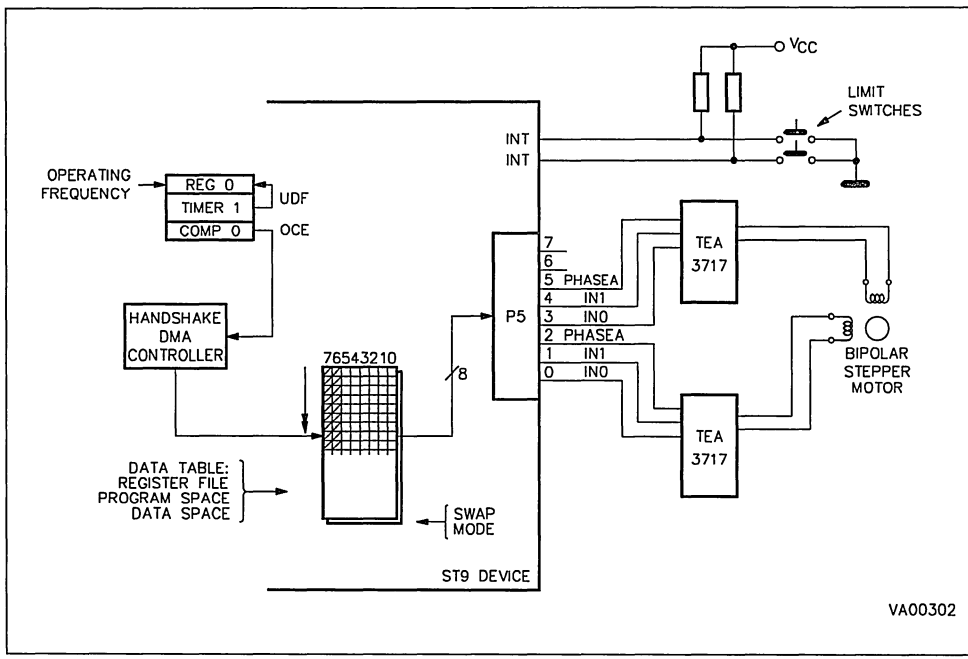
I/O Ports 4 and 5 of the ST9054 are able to support a parallel interface with handshake capability. This allows one, two or four wire interconnecting handshake signals and facilitates very fast parallel transfer of data for input and output, or for the interconnection of peripheral devices requiring strobe signals for synchronization. Table 10 shows the available options for input and output status and strobe signals available as Alternate Functions of I/O port bits (see Pin Configuration). The Handshake configuration is set within the Handshake Control Register (HDC*n*R) for the relevant I/O port *n*.

Data transfer through a parallel I/O port with handshake can also be triggered through a DMA channel. Timing is generated by the ST9054 TIMER ON-CHIP EVENT strobe signal (see the TIMER section for information on generating these signals), which causes the programmed transfer of data to or from the memory source which can be Register File, Program space memory or Data space memory. An example of application of this technique is shown in figure 41, a complex stepper motor timing sequence automatically being transferred from a table in the Register File (or memory spaces) to the stepper motor drivers. After initialisation, this operation is transparent until the task (complex microstepping) is completed.

Table 10. Handshake Control Signal Options

Mode	Handshake Lines	Names
Input to Port	1	WRRDY
	2	$\overline{\text{WRSTB}}$ WRRDY
Output from Port	1	RDRDY
	2	$\overline{\text{RDSTB}}$ RDRDY
Bidirectional	4	$\overline{\text{WRSTB}}$ WRRDY $\overline{\text{RDSTB}}$ RDRDY

Figure 40. Handshake + DMA Used for Stepper Motor Driving



TIMER/WATCHDOG

A 16 bit down-counter, complete with 8 bit prescaler, is integrated into the ST9054 core. This is able to operate both as a general purpose timer with associated input and output pins for timing functions, and also as a Watchdog Timer offering a security against possible processor malfunctions due to external events.

Timer Modes

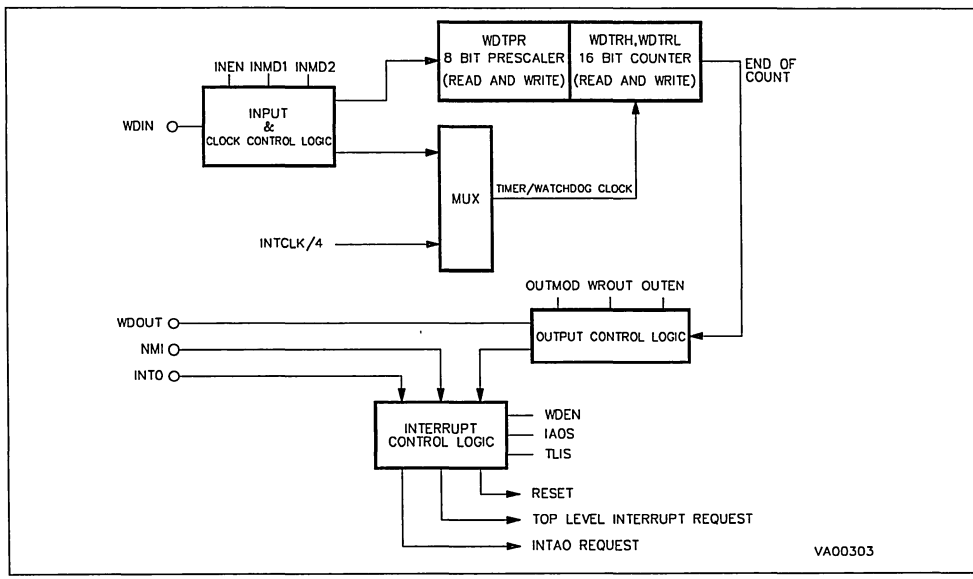
When operating as a Timer, with a timing resolution from 333ns to 5.59s (INTCLK = 12MHz), an input pin (WDIN) and output pin (WDOUT) may be selected as the Alternate Functions of two I/O pins. When WDIN is enabled by the User by setting INEN high (WDTCR.3) and the Alternate Function is set, 4 operating modes are available: The WDIN input may be programmed to act as an event counter input, with high to low transitions causing the counter to decrement (the time duration between the falling edges of the input clock must be at least 333ns, allowing a maximum input frequency of 3MHz). It may also be used for pulse width measurement by being selected as a counter clock gate signal (prescaler to the counter being driven by INTCLK/4), counting being enabled when WDIN is at a high level. Trigger and Re-trigger modes cause a reload of the timer User preset values (providing STSP, WDTCR.7 is active) for a high to low transition on WDIN at any time (Re-trigger mode) or when the counter is at the end of count (Trigger mode). The counter decrements at a rate driven by INTCLK/4.

The WDOUT pin, when set as the Alternate Function, is enabled by OUTEN high (WDTCR.0), and may either toggle the state of the I/O bit (frequency generation, OUTMD = "0", WDTCR.2) or pass the state of the WROUT bit to the output allowing PWM generation (OUTMD = "1") at the end of count (timer value = 0) condition.

Watchdog Mode

The timer functions may be disabled, and the Timer configured for a Watchdog operation by re-setting WDEN (WCR.6) to zero. Once the Watchdog has been selected it CANNOT be set back into the standard timer mode until the next Hardware Reset cycle. The User should set the watchdog timer prescaler and timer reload value before enabling the Watchdog mode. The Watchdog Timer must then be retriggered, causing the reloading of the timer value, by the operation of writing of the byte sequence 0AAh, 055h to the WDTLR register. If this is not done before the Watchdog counts to zero, the Watchdog Timeout condition occurs. This causes a Hardware Reset of the ST9054. The Watchdog reset signal is not output on the external Reset pin.

Figure 41. Timer/Watchdog Block Diagram



TIMER/WATCHDOG (Continued)

Timer/Watchdog Interrupts

The Timer/Watchdog may provide several levels of interrupts selectable by the User. The Timer mode offers two interrupt sources, triggered on the timer value reaching 0, either a prioritized level (by taking the Interrupt priority channel from the External Interrupt INTA0) or by a top level, non-maskable interrupt (taking the external NMI input channel). The interrupt channels are multiplexed from the alternative source according to the status of the IAOS (EIVR.1) and TLIS (EIVR.2) bits as shown in figure 44. Please refer to the ST9 Technical Manual for further details on changing the interrupt sources of the Timer/Watchdog. When the Watchdog mode is set (WDEN = "0"), the timer value equal to 0 event generates a Hardware reset of the ST9054. The Timer/Watchdog control registers are located within Page 0 of the Paged I/O register group.

Figure 43. Timer/Watchdog Interrupt Sources

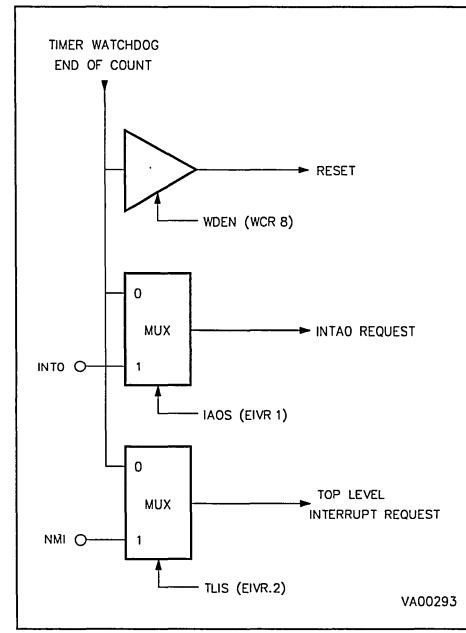
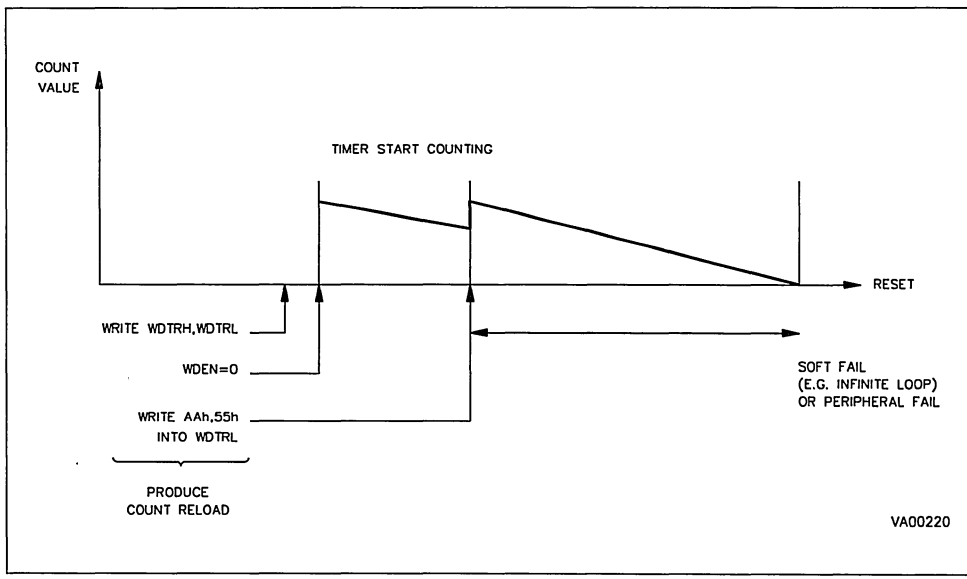


Figure 42. Timer/Watchdog in Watchdog Mode



MULTIFUNCTION TIMER

The ST9054 includes three identical 16 bit Multifunction Timers (MFT) in addition to the TIMER/WATCHDOG. The following description applies to Timer 0, Timer 1 and Timer 3.

Each timer is a 16 bit Up/Down counter, driven by the output of an 8 bit prescaler which may be driven by INTCLK/3 (giving a minimum timing resolution of 250ns at INTCLK = 12 MHz) or by an external source. This timer is supported by two 16 bit Comparison Registers for generating timed functions and two 16 bit Capture/Load Registers for timing and variable timebase functions. These features coupled with 2 input pins (TxINA and TxINB) and 2 output pins (TxOUTA and TxOUTB, where x = 0 or 1), available as Alternate Functions, giving the timer 13 operating modes for virtually all required timing functions.

MFT Operating Modes

The operating modes are selected by the programming of the Timer Control Register (TCR Timer x) and the Timer Mode Register (TMR) as follows:

One-Shot Mode. The counter stops at the End Of Count Condition (up or down count).

Continuous Mode. At End Of Count the timer is reloaded from a Load Register.

Trigger Mode. A Trigger causes reload from a load register only if the Timer is at End of Count.

RETrigger Mode. A Trigger causes reload from a load register at any time.

Gate Mode. Counting is performed only when the external gate input (TxINA or TxINB) is active (logical 0).

Capture Mode. A Trigger causes the timer value to be latched into the selected Capture register.

Up/Down Mode. A Trigger causes a count up or down, or a change in counting direction.

Free-Running Mode. Up or Down counting is performed to the full range with no action at End of Count. This is used in Bicapture and Capture Modes.

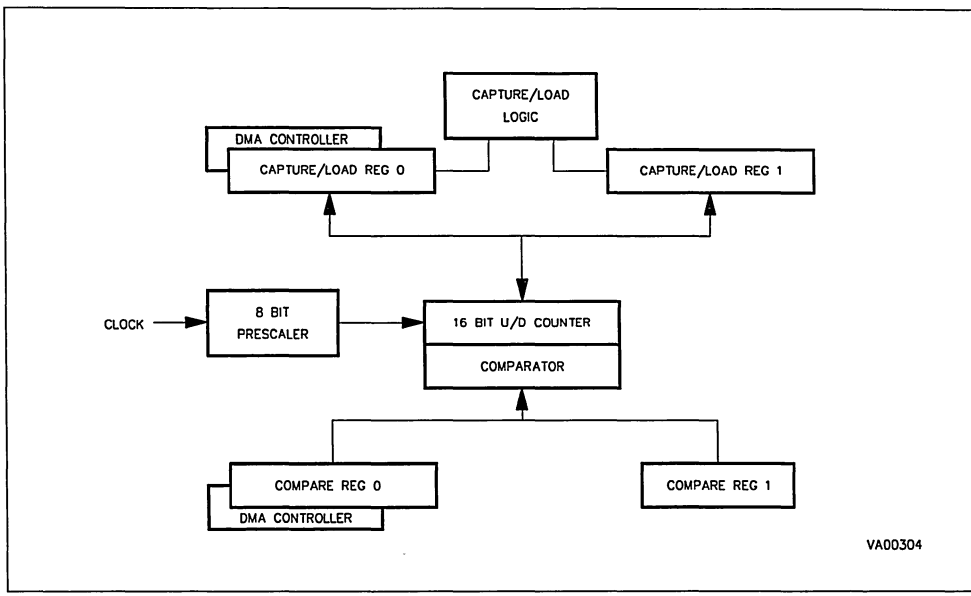
Monitor Mode. One Capture register follows the contents of the timer.

Autoclear Mode. The timer is reset to 0000h or FFFFh (up or down count respectively) on a trigger. This gives delta time measurement or free running with a modulo of less than 2^{16}.

Biload Mode. The counter is reloaded on an End Of Count condition alternately from the two Load Registers. (PWM output).

BICapture Mode. A Trigger causes the current timer value to be transferred alternately to the two Capture registers. (Pulse width measurement).

Figure 44. Multifunction Timer Block Diagram



MULTIFUNCTION TIMER (Continued)

Parallel Mode. The prescaler output of Timer 0 is internally connected to the input of the prescaler of Timer 1, if this is then set to 00h (= divide by 1), then the two timers may be run in parallel.

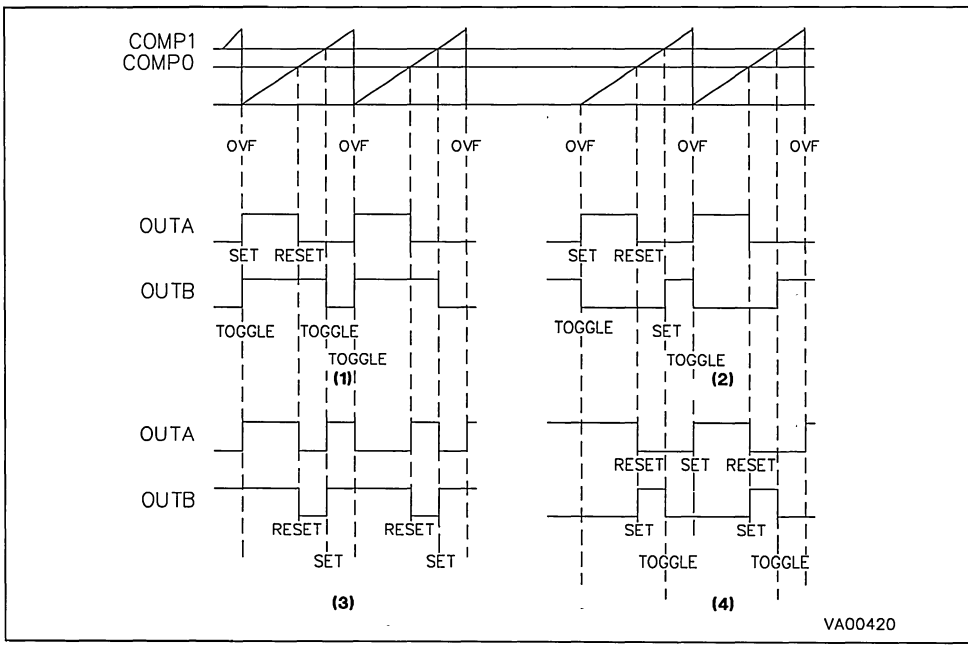
The trigger events may be either caused by software, or an action on the two input pins which may be programmed to respond to rising, falling or both edges of the input. The input modes are selected in the Input Control Register (ICR) as shown in Table 11. This includes the Autodiscriminator mode, which causes the timer to count up or down depending on the phase between the two input edges, such as the signals generated by optical encoders.

The two output pins (available as Alternate Functions) may be programmed through the Output Control Registers OACR and OBCR to be modified (Set, Reset, Toggle or No Operation) on each of Overflow/Underflow (OVF/UNF), Compare on CMP0 valid (CM0), or Compare on CMP1 (COMP1) valid events. This allows repetitive signals such as PWM drive to be output with minimum CPU overhead. Figure 46 shows some typical waveforms available from these signals.

Table 11. Input Pin Function Settings

Input Control Register IN3-IN0 bits	TxINA Input Function	TxINB Input Function
0000	I/O	I/O
0001	I/O	Trigger
0010	Gate	I/O
0011	Gate	Trigger
0100	I/O	Ext.clock
0101	Trigger	I/O
0110	Gate	Ext.clock
0111	Trigger	Trigger
1000	Clock Up	Clock Down
1001	Up/Down	Ext.clock
1010	Trigger Up	Trigger Down
1011	Up/Down	I/O
1100	Autodiscr.	Autodiscr.
1101	Trigger	Ext.clock
1110	Ext.clock	Trigger
1111	Trigger	Gate

Figure 45. Example Output Waveforms



MULTIFUNCTION TIMER (Continued)

The Overflow/Underflow event and the Compare 0 event may also be programmed to give On-chip Event timing signals to trigger other peripheral operations on the ST9054. These are as shown in Table 12.

Table 12. ST90R50 On-Chip Event Settings

MFT0	Handshake Trigger Port 4
MFT1	Handshake Trigger Port 5
MFT3	A/D Conversion Trigger

The TxOUTA and TxINA lines for each timer may be connected together internally, by setting of the SCx bits of the I/O Connection Register (IOCR).

The Multifunction Timers are enabled for counting by the Counter Enable bit (CEN, TCR.7) of the respective timer unit. When CEN is low, both prescaler and timer are halted. CEN is logically ANDed with the Global Counter Enable bit (GCEN, CICR.7), so that all timers may be started in synchronism, i.e. when the timers are set into Parallel mode, this allows initialization of the Timers before triggering at the same instant.

MFT Interrupts

Each Multifunction Timer can generate interrupt requests from 5 different interrupt sources which are grouped into 3 independent groups. The Interrupt Vector has the source of the interrupt group encoded by hardware into the least significant 3 bits of the vector. This allows the programming of the base address to an 8 byte block within the interrupt vector area of the Program Space. The groups and respective addresses are shown in Table 13.

Table 13. MFT Interrupt Vectors

Interrupt Source	Vector Address
COMP0 COMP1	xxxx x110
CAPT0 CAPT1	xxxx x100
Overflow/Underflow	xxxx x000

Each source may be independently masked, in addition all Timer interrupts may be disabled by the Global Timer Interrupt enable (GTIEN, IDMR.7) control bit. If a Timer interrupt on Compare 0 or Capture 0 does not have its corresponding pending bit reset before the next interrupt, then an overrun condition occurs. This condition is flagged in two dedicated overrun bits in the Timer FLAGS register.

MFT DMA Channels

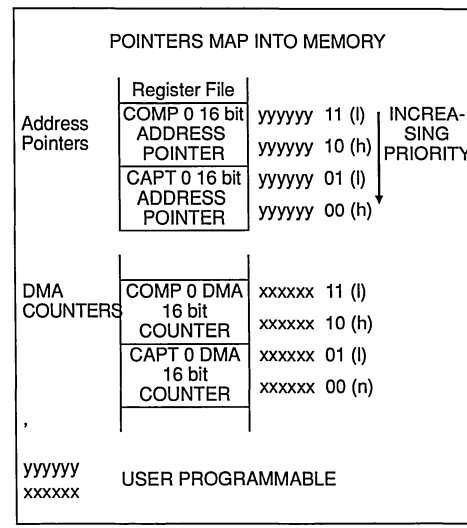
Two independent DMA channels are present within each MFT, associated to the Compare 0 and Capture 0 sources. This allows 16 bit DMA transactions from Register File/Memory to COMP0 registers, and from CAPT0 registers to Register File/Memory. The DMA channels allow the capture of external event timings in memory allowing off-line analysis, and creating of variable pulse width signal trains, as required by the drive of Triacs in certain modes.

The two interrupt mask sources are independently masked by two DMA mask bits, mapped in the IDMR register. The End of Block (EOB) procedures are as described in the INTERRUPT/DMA section.

The DMA counter and address pointer registers share the most significant User-programmable 6 bits for both DMA channels (COMP 0 and CAPT 0), thus the mapping of the counter and address registers use automatic offsets from the base address. The actual mapping changes dependent on whether the Register File or Memory is addressed for the transfer. The offsets are shown in Table 14.

After the transfer of the complete block of data to/from the MFT, the count registers reach the zero value and an end of block interrupt occurs so that the ST9 may process the new data. In many cases, the time taken to reload the data tables and to

Table 14-1. MFT DMA Address and Counter Registers for Memory DMA Transfers



MULTIFUNCTION TIMER (Continued)

Table 14-2. MFT DMA Address and Counter Registers for Register File DMA Transfers

POINTERS FOR REGISTER FILE DMA			
8 Bit COUNTER	xxxxxx	11	COMPARE 0
8 bit ADDR. POINTER	xxxxxx	10	
8 bit COUNTER	xxxxxx	01	CAPTURE 0
8 bit ADDR. POINTER	xxxxxx	00	
xxxxxx	USER PROGRAMMABLE		

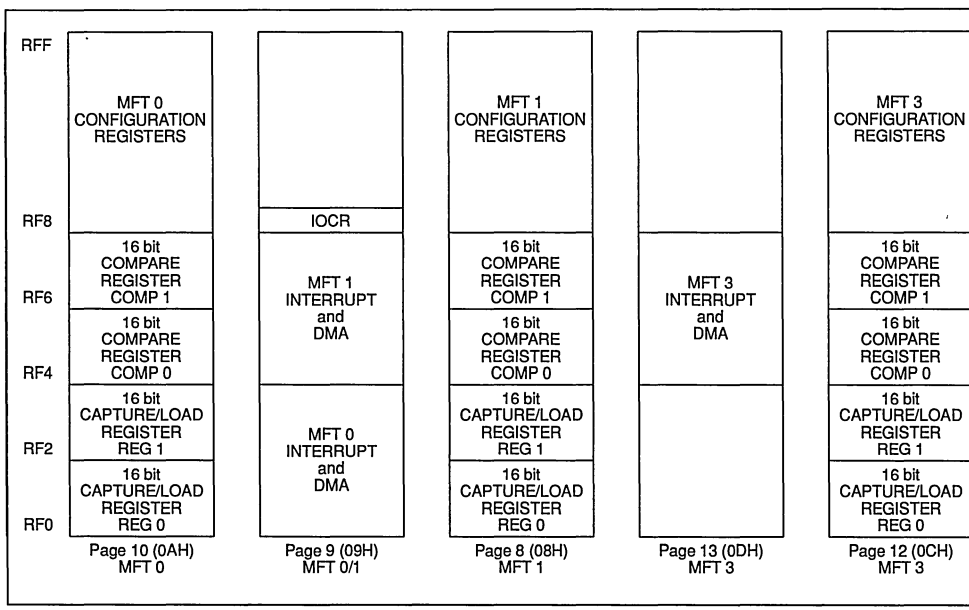
re-trigger the DMA action causes speed limitations, especially in those applications requiring a continuous high speed data flow, because of the time consumed by the restore routine. An additional DMA function, the SWAP mode, overcomes this limitation. This is enabled by the setting of the SWEN (IDCR.3) bit. This causes hardware generated signals to replace the User address bit 2 of both the address and counter pointers. The address and counter registers are thus duplicated at an offset of 4 registers. At the End Of Block condition, the EOB interrupt is generated to signal the end of DMA, and the state of pointer address bit 2 toggles state automatically and the new address and count values are used. Thus the ST9 can safely process the previous block of data while the new block is being transferred. This will continue until the SWAP mode is disabled.

A software protection scheme is implemented to prevent non-updated pointer registers from being used if a second EOB interrupt arrives during the servicing of the first. This mechanism locks the state of the DMA mask bit to prevent further transfers from taking place. The User should check for this condition in the EOB routine to ensure that all the DMA transfers are properly serviced.

The control Registers of each MFT occupy 20 registers within the I/O paged area. These are mapped as shown in figure 47.

In addition the MFT is able to trigger byte DMA transfers in both directions through an I/O port with Handshake (see I/O Handshake and DMA).

Figure 46. Multifunction Timer Page Maps



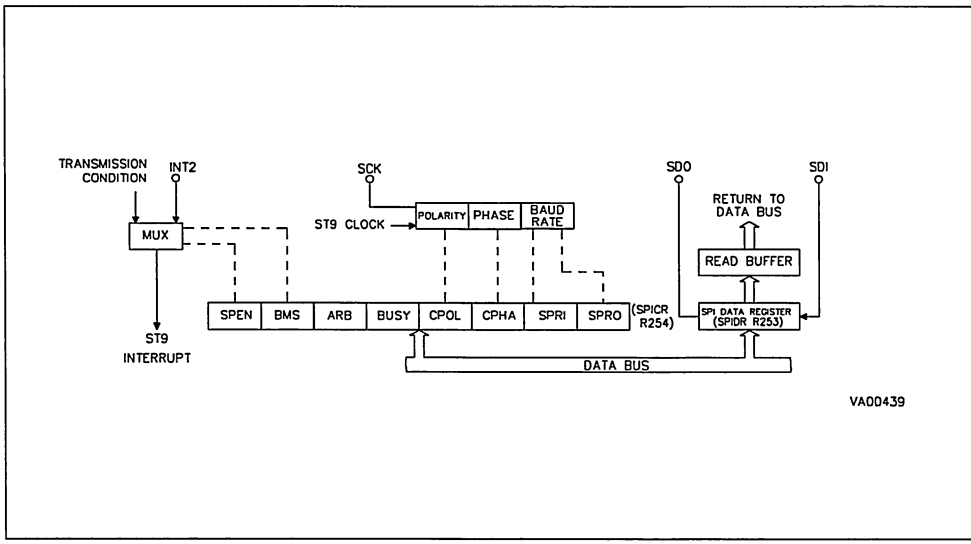
SERIAL PERIPHERAL INTERFACE (SPI)

The Serial Peripheral Interface (SPI) is integrated into the Core module of the ST9 and provides a general purpose shift register based peripheral allowing synchronous serial I/O, with special modes allowing compatibility with I^2C-bus and IM-bus Communication standards in addition to the standard serial bus protocol. The SPI uses 3 lines comprising Serial Data Out (SDO), Serial Data In (SDI) and the Synchronous Serial Clock (SCK) which are available as Alternate Functions of I/O pins. Additional I/O pins may act as device selects or IM-bus address ident signals. The functional diagram of the SPI is shown in figure 48.

The SPI, when enabled (SPEN, SPICR.7, high), receives input data from the ST9 internal data bus into the SPIDR, and originates the SCK to shift the data serially through SDO (Most Significant bit first) to the slave device which responds by sending data to the master device via the SDI pin. This implies full duplex transmission with both data-out and data-in synchronized with the same clock signal. Thus the byte transmitted is replaced by the byte received, eliminating the need to separate "Tx Empty" and "Rx full" status bits. After the 8 clock cycles have been concluded; the received data in SPIDR is parallel transferred to the read buffer and data becomes available for the ST9054 during the next read cycle of SPIDR. The BUSY bit (SPICR.4) is set when transmission is in progress, this allows the User to monitor the status of the SPI by polling of this bit.

The SPI can operate only in master mode, i.e. the clock is always generated by the ST9054, however the SCK polarity and phase can be programmed to suit all peripheral requirements (figure 48). This, together with the 4 programmable bit rates (divided from the INTCLK, table 15), provide the large flexibility in handling different protocols.

Figure 47. SPI Functional Diagram



SERIAL PERIPHERAL INTERFACE (Continued)

Figure 48. SPI Data and Clock Timing

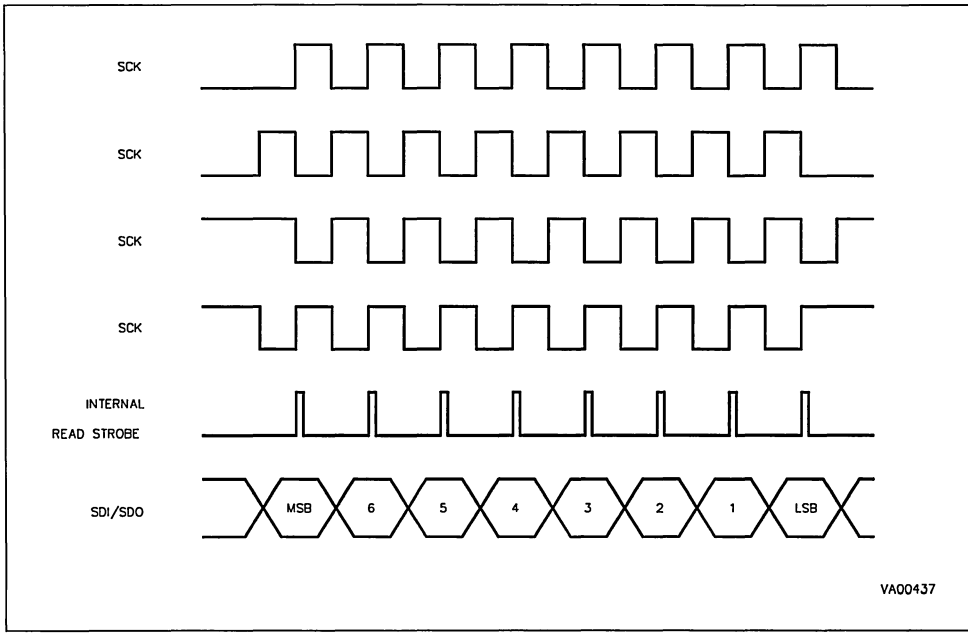


Table 15. SPI Rate Selection

SPR1	SPR0	Clock Divider	SCK Frequency (INTCLK = 12MHz)
0	0	8	1500KHz (T = 0.67µs)
0	1	16	750KHz (T = 1.33µs)
1	0	12	93.50KHz (T = 10.66µs)
1	1	256	46.87KHz (T = 21.33µs)

I²C-bus Compatibility

The SPI includes additional circuitry to enable the use of external I²C-bus peripherals. The I²C-bus mode is a 2 wire bus while the SPI operates with 3 wires, however wire-ANDing SDO and SDI gives the required signalling, while setting the BMS bit causes the enabling of the special I²C-bus features: Clock Slowdown by external devices and Arbitration Lost detection. This mode also affects the Interrupt sources as shown in the next section.

SPI Interrupts

The SPI, when enabled, uses the INT2 external interrupt channel source, using the priority selected for INT2 within the External Interrupt Priority registers. The INT2 mask bit should be set and INT2 pending bit reset before enabling the SPI through SPEN. The BMS (SPICR.6) and SPEN bits select the SPI internal interrupt source as shown in Table 16

Table 16. SPI Interrupt Sources

SPEN	BMS	Interrupt Source
0	0	External channel INT2
0	1	S-BUS/I²C start or stop condition
1	X	End of one byte transmission

SPI Registers

The two registers controlling the SPI are located in I/O page 0, the Data Register, SPIDR, at R253 and the control register, SPICR, at R254.

SERIAL COMMUNICATIONS INTERFACE

Function

The two Serial Communications Interfaces (SCIs) of the ST9054 offers a means of full-duplex serial data transfer to a wide range of external equipment. Each has a fully programmable character format control for asynchronous and byte synchronous serial I/O, an integral Baud Rate Generator, giving a maximum baud rate of 375K Baud in Asynchronous mode (Internal Clock), and two DMA channels for transparent transmission and reception of characters. Support is also present in hardware for Line Break Detection and generation, character search, network interfacing with 9th bit Address logic, and Local Loop Back and Auto echo modes for Self-Test. The control registers for an SCI exist within one I/O page within the I/O page group.

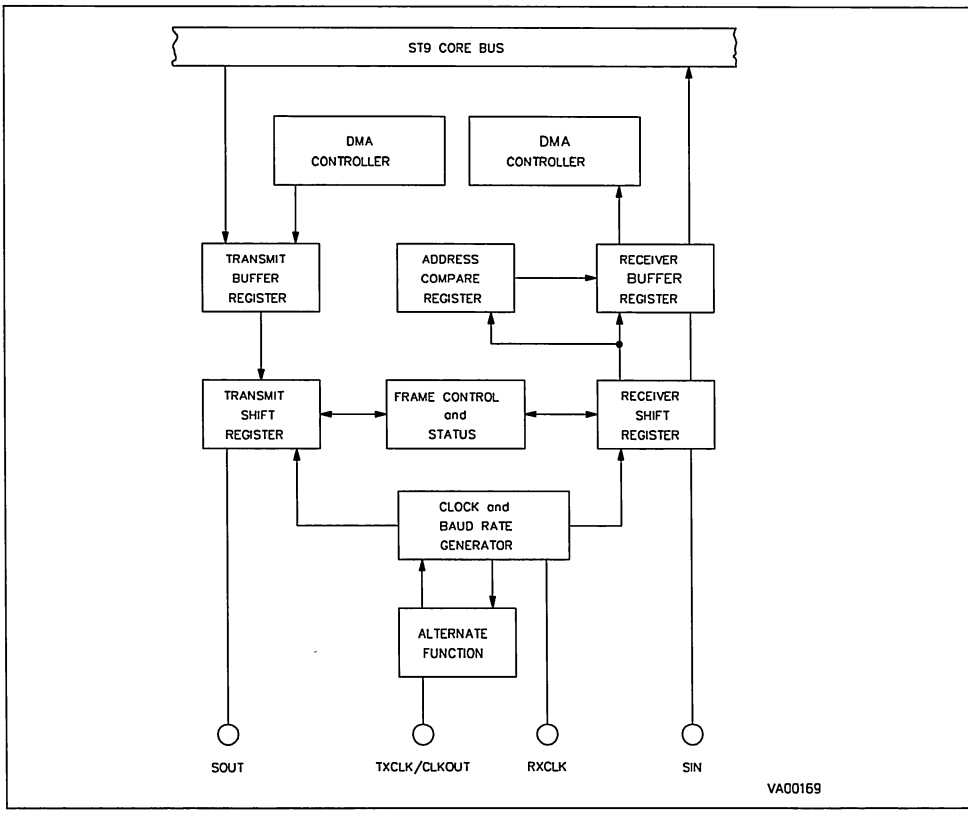
Character Formats

When used for asynchronous character transmission and reception, the character format may be changed (through the Character Control Register CHCR) to suit external equipment requirements. This is summarized in figure 51.

The baud rate clock for asynchronous mode should be set to the ÷16 Mode and the frequency of the clock input (from an external source or the internal baud-rate generator output) set to suit this.

This format control is also available for the byte synchronous mode (Clock divider set to ÷1), when the data and clock are output in synchronism, the data being sampled once per clock period (Figure 52). For a second synchronous mode, CLKOUT is activated only for the data section of the word (Figure 53) on serial data output, and input data is

Figure 50. SCI Functional Block Diagram



SERIAL COMMUNICATION INTERFACE (Continued)

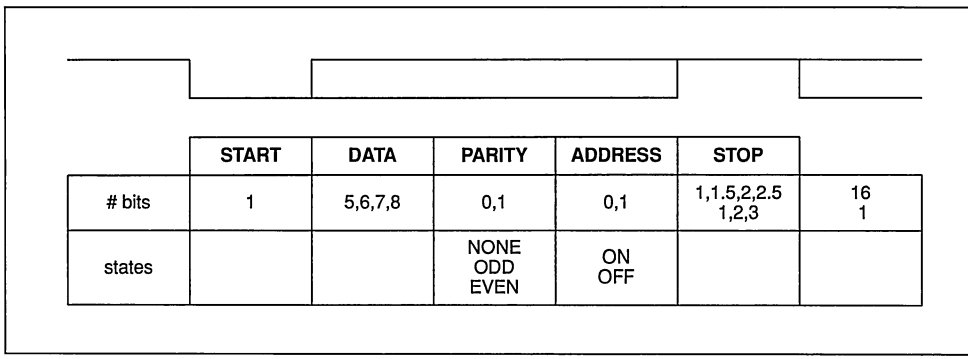
latched on the rising edge of the external synchronised clock input on the RXCLK pin. This mode may be used to access external synchronous peripherals.

The Address bit/D9 is optional and may be added to any word format, it is commonly used in network or machine control applications. When enabled (AB, CHCR.4 = "1"), an address or ninth data bit can be added to a transmitted word by setting the Set Address bit (SA, IDPR.5). This is then appended to the next word entered into the (empty) Transmitter Buffer Register and then cleared by hardware. On character input an Address Bit set can indicate that the data preceding the bit is an address which may be compared in hardware with the value in the Address Compare Register (ACR) to generate an Address Match interrupt when equal.

The Address bit and Address Comparison Register can also be combined to generate an Address Interrupt in 4 modes to suit different protocols, based upon the status of the Address Mode Enable bit (AMEN, IDPR.7) and the Address Mode bit (AM, CHCR.7) as shown in Table 17.

The character match Address Interrupt mode may be used as a powerful character search mode, giving an interrupt on reception of a predetermined character e.g. Carriage Return or End of Block codes.

Figure 51. SCI Character Format



	START	DATA	PARITY	ADDRESS	STOP	
# bits	1	5,6,7,8	0,1	0,1	1,1.5,2,2.5 1,2,3	16 1
states			NONE ODD EVEN	ON OFF		

Figure 52. Byte Synchronous Output

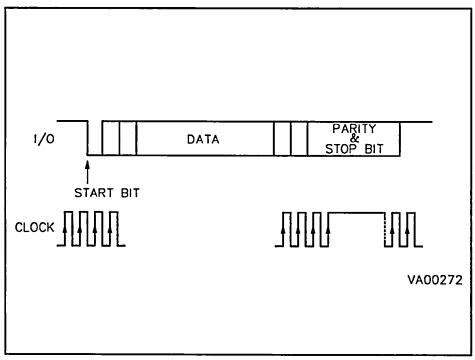
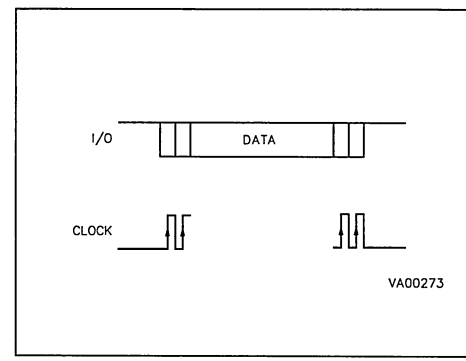


Figure 53. Serial Expansion Mode



SERIAL COMMUNICATION INTERFACE (Continued)

Table 17. Address Interrupt Modes

If 9th Data Bit = 1
If Character Match
If Character Match and 9th Data Bit = 1
If Character Match on Word Immediately Following Break

The Line Break condition is fully supported for both transmission and detection. Line Break is sent by setting the SET_BREAK bit (SB, IDPR.6). This causes the transmitter output to be held low (after all buffered data has been transmitted) for a minimum of one complete word length and until the SB bit is Reset.

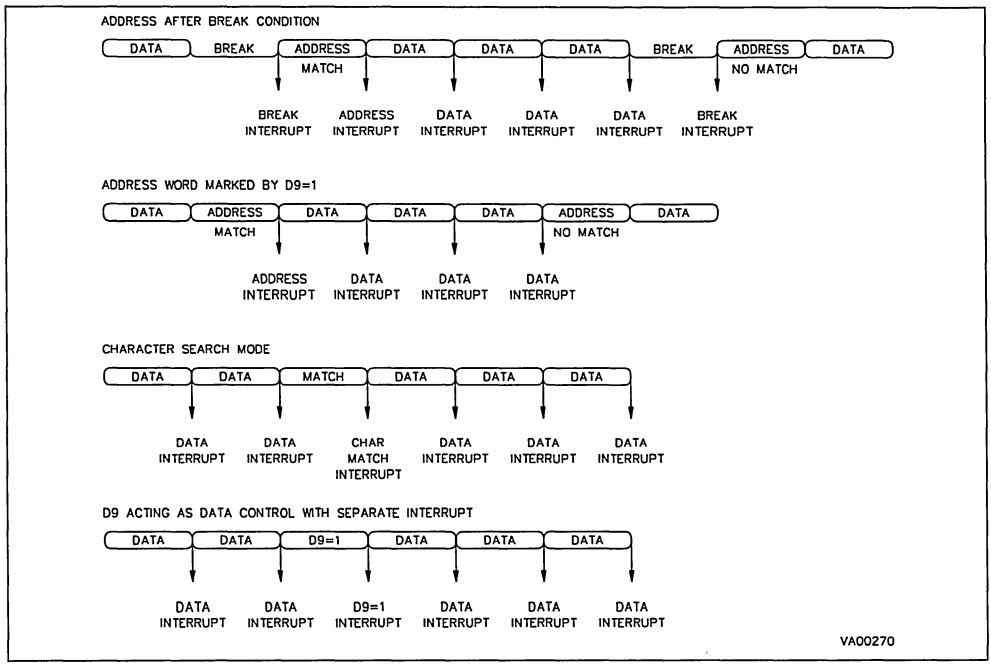
SCI Interrupts

Each SCI is able to generate interrupts from multiple sources. Receive interrupts include data pending, receive errors (overrun, framing and parity), address or break pending and transmit interrupts are software selectable for either the Transmit Holding Register Empty (HSN, IMR.7 = "1") or for the Transmit Shift Register Empty (HSN = "0"). Interrupt sources are indicated by the Interrupt pending bits, shown in Table 18. These bits should be reset by the User during the Interrupt Service routine.

Table 18. SCI Interrupt Vector

Interrupt Source	Vector Address
Transmitter Buffer or Shift Register Empty/Transmit DMA end of Block	xxx x110
Received Read/ Receive DMA end of Block	xxxx x100
Break Detector Address Word Match	xxxx x001
Receiver Error	xxxx x000

Figure 54. SCI Interrupt Typical Usage



SERIAL COMMUNICATION INTERFACE (Continued)

When DMA is active the Receive Data Pending bit (RXDP, ISR.2), and the Transmit status bit interrupt sources are replaced by the DMA End Of Block Interrupt sources for transmit and receive, respectively.

Typical Usage of the Interrupts provided by the SCI are show in figure 54.

The SCI interrupts have an internal priority structure (Table 19) in order to resolve simultaneous events.

Table 19. SCI Interrupt Internal Priority

Receive DMA Request	Highest Priority
Transmit DMA Request	
Receive Interrupt	
Transmit Interrupt	Lowest Priority

The four major levels of interrupt are encoded in hardware to provide two bits of the interrupt vector register, allowing the position of the block of pointer vectors to be resolved to a block size of 8 bytes.

SCI DMA

Two DMA channels are associated with each SCI, for transmit and for receive. These follow the register scheme as described in the DMA Section. It should be noted that, after initializing the DMA counter and pointer registers and enabling DMA, data transmission is triggered by a character written into the Transmit Holding register. The DMA End Of Block Interrupts generated on completion of the DMA transfer take the place of the normal transmit and receive character interrupt vectors.

SCI Clock Generation

The communication bit frequency of the SCI transmitter and receiver sections can be provided from the integral Baud Rate Generator (allowing a maximum asynchronous bit rate of 350k Baud) or from external sources (maximum bit rate 175k Baud). This clock is divided by 16 for asynchronous mode (CD, CCR.3, = "0"), or divided by 1 for synchronous modes (CD = "1").

External Clock Sources.

The External Clock input pin TXCLK may be programmed in Alternate function by bits TXCLK (CCR.7) and OCLK (CCR.6) to be: the transmit clock input (respecting the ÷16 and ÷1 timing requirements), to act as the output of the Baud Rate Generator (allowing an external divider circuit to provide the receive clock for split rate transmit and receive e.g. 1200/75 baud), or to be CLKOUT, the clock output for the synchronous mode. Receive clock input via RXCLK Alternate function is enabled by the XRX bit CCR.5, this input should be set according to the setting of the CD bit.

Baud Rate Generator.

The integral Baud Rate Generator is a 16 bit divide by n circuit of the Internal Clock INTCLK. Thus INTCLK should be chosen to provide a suitable frequency for division by the Baud Rate Generator to give the required transmit and receive bit rates. Suitable INTCLK frequencies and the divider values for standard Baud rates are shown in Table 20.

The act of writing to either of the two registers comprising the 16 bit divider causes a reset of the SCI, allowing initialization of the SCI settings before the writing of the other Baud Rate Generator register.

Self Test

Testing of the communications channel may be performed using the facilities of the SCI. Auto Echo mode (SCI SOUT disconnected, SIN pin internally connected to SOUT pin) and Loopback mode (SCI transmitter and receiver sections disconnected from SOUT and SIN pins and directly connected internally) may be used individually or together.

SERIAL COMMUNICATION INTERFACE (Continued)

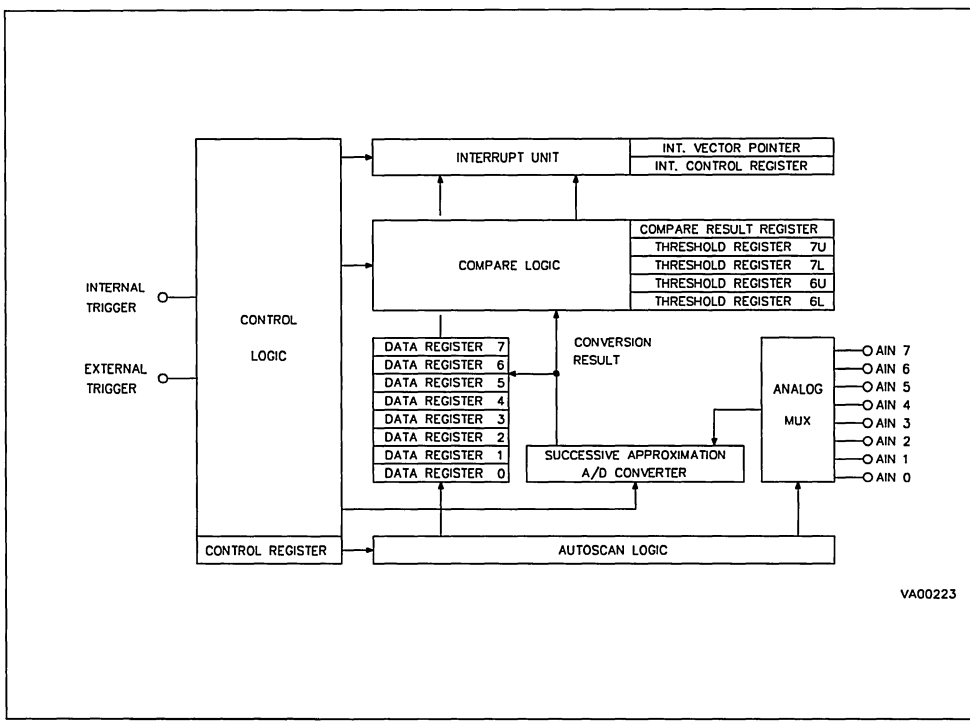
Table 20. SCI Baud Rate Generator Divider Values

INTCLK: 7680.000 KHz							
Baud Rate	Clock Factor	Desired Freq (kHz)	Divisor		Actual Baud Rate	Actual Freq (kHz)	Deviation
			Dec	Hex			
50.00	16 X	0.80000	9600	2580	50.00	0.80000	0.0000%
75.00	16 X	1.20000	6400	1900	75.00	1.20000	0.0000%
110.00	16 X	1.76000	4364	110C	109.99	1.75985	0.0083%
300.00	16 X	4.80000	1600	0640	300.00	4.80000	0.0000%
600.00	16 X	9.60000	800	0320	600.00	9.60000	0.0000%
1200.00	16 X	19.20000	400	0190	1200.00	19.20000	0.0000%
2400.00	16 X	38.40000	200	00C8	2400.00	38.40000	0.0000%
4800.00	16 X	76.80000	100	0064	4800.00	76.80000	0.0000%
9600.00	16 X	153.60000	50	0032	9600.00	153.60000	0.0000%
19200.00	16 X	307.20000	25	0019	19200.00	307.20000	0.0000%
38400.00	16 X	614.40000	13	000D	36923.08	590.76923	3.8462%
76800.00	16 X	1228.80000	6	0006	80000.00	1280.00000	4.1667%
INTCLK: 11059.20 KHz							
Baud Rate	Clock Factor	Desired Freq (kHz)	Divisor		Actual Baud Rate	Actual Freq (kHz)	Deviation
			Dec	Hex			
50.00	16 X	0.80000	13824	3600	50.00	0.80000	0.0000%
75.00	16 X	1.20000	9216	2400	75.00	1.20000	0.0000%
110.00	16 X	1.76000	6284	188C	109.99	1.75990	0.0058%
300.00	16 X	4.80000	2304	0900	300.00	4.80000	0.0000%
600.00	16 X	9.60000	1152	0480	600.00	9.60000	0.0000%
1200.00	16 X	19.20000	576	0240	1200.00	19.20000	0.0000%
2400.00	16 X	38.40000	288	0120	2400.00	38.40000	0.0000%
4800.00	16 X	76.80000	144	0090	4800.00	76.80000	0.0000%
9600.00	16 X	153.60000	72	0048	9600.00	153.60000	0.0000%
19200.00	16 X	307.20000	36	0024	19200.00	307.20000	0.0000%
38400.00	16 X	614.40000	18	0012	38400.00	614.40000	0.0000%
76800.00	16 X	1228.80000	9	0009	76800.00	1228.80000	0.0000%

ANALOG TO DIGITAL CONVERTER

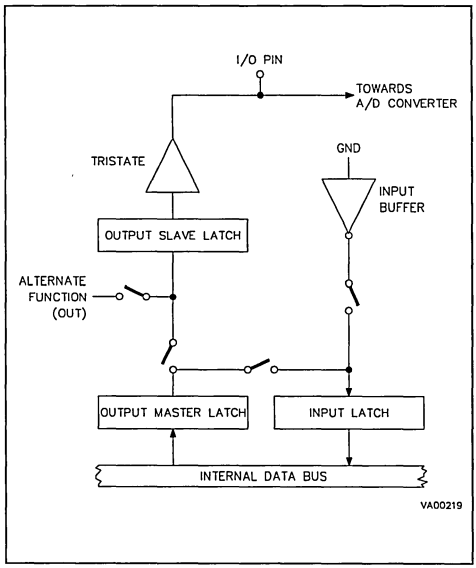
The ST9054 Analog to Digital Converter (A/D) is comprised of an 8 channel multiplexed input selector and a Successive Approximation converter. The conversion time is a function of the INTCLK frequency; for the maximum 12MHz clock rate, conversion of the selected channel requires 11µs. This time also includes the 3µs of the integral Sample and Hold circuitry, which minimizes need for external components. The resolution of the converted channel is 8 bits ±1/2 LSB between the Analog V_{SS} and V_{DD} references which occupy two pins of the ST9054 (AV_{SS} and AV_{DD} respectively). This allows the full 256 bit resolution to apply over a reduced input range such as provided by various sensors and allows the best supply noise rejection. The input Analog channel is selected by using the Alternate Function setting as shown in the I/O ports section. The I/O bit structure of the port connected to the A/D converter (Port 4) is modified as shown in figure 56 to prevent the Analog voltage present at the I/O pin from causing high power dissipation across the input buffer. Un-selected analog channels should also be maintained in the Alternate function mode for this reason. A Power Down mode is available for applications which require low power dissipation, this is selected by setting to zero the POW bit (CLR.2) which turns off all Analog functions within the A/D converter.

Figure 55. A/D Block Diagram



ANALOG TO DIGITAL CONVERTER (Continued)

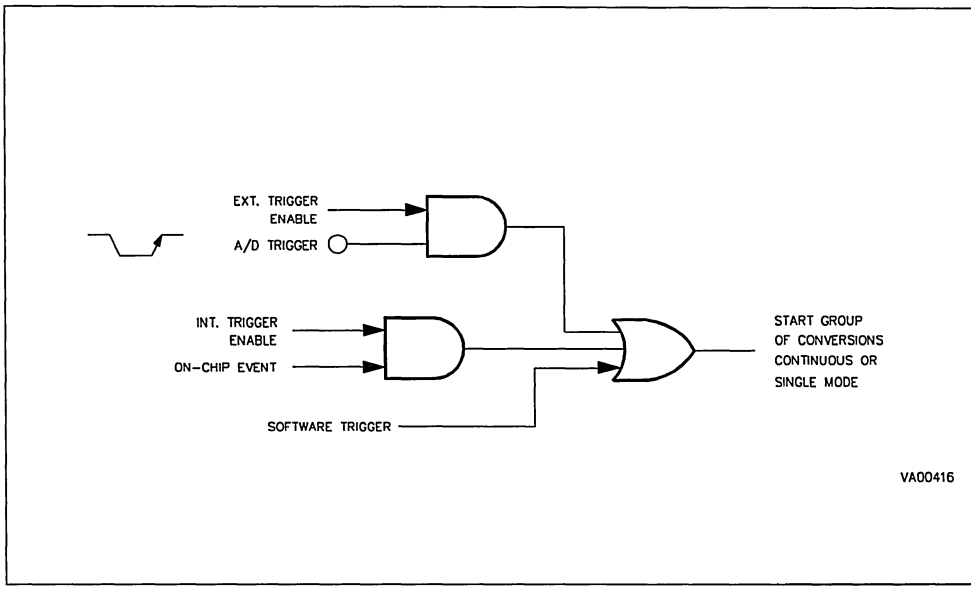
Figure 56. A/D Input Configuration Status



Conversion

Each of the input Analog channels (AIN0-7) can be converted singly or continuously. In single mode (CONT, CLR.1, = "0") conversions are triggered by setting the Start/Stop bit ST (CLR.0), this is reset by hardware at the end of a group of conversions and conversion stops. The Autoscan mode (CONT = "1") converts each input channel in sequence, starting from the channel number selected in the Start Conversion Address (SC1-3) bits and increasing to channel 7 (AIN7), repeating so that the data registers will be maintained with the latest converted result. Conversion start is triggered by internal or external events. An external trigger (enabled by EXTG, CLR.4, = "1") is caused by a pulse on the ADTRG pin available as an Input Alternate Function. This should have a minimum length of 80 nS and of a period greater than the conversion time. The Internal trigger is enabled by setting INTG, CLR.3, to "1" (this is ORed with EXTG to prevent hardware conflicts, but the correct procedure is to enable only one source at a time), in this case triggering is either by setting the ST bit by software or by enabling the ON-CHIP EVENT signal from the TIMER module.

Figure 57. A/D Trigger Sources



ANALOG DIGITAL CONVERTER (Continued)

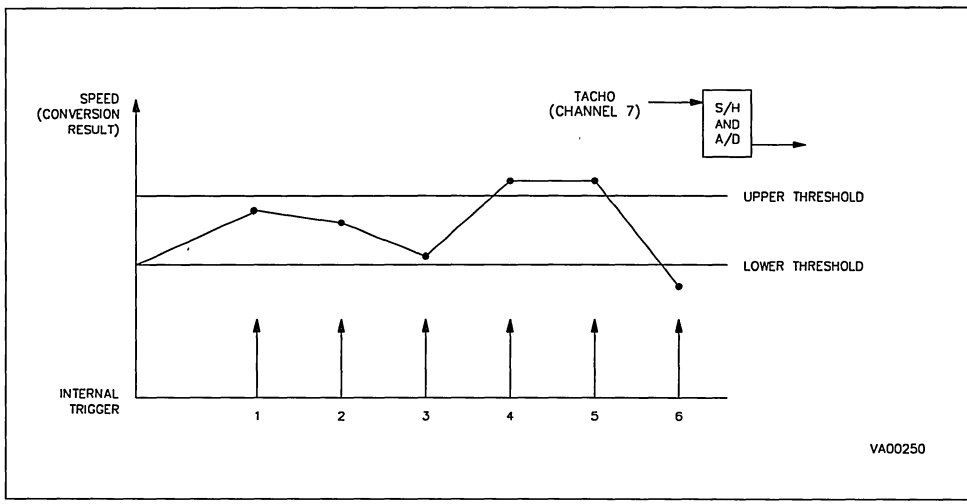
The resulting data from the converted Analog channel AINx is stored in the appropriate Data Register DxR. Two channels AIN6 and AIN7 have a special feature known as the Analog Watchdog, by the use of two Threshold Registers for each channel. The Upper, (UT6R, UT7R), and lower, (LT6R, LT7R), registers contain User preset values. These values are automatically compared to the value in the Data Registers D6R and D7R following each new conversion. If the resulting data is less than the corresponding Lower Threshold Register, or higher than the contents of the corresponding Upper Threshold Register, then an interrupt may be generated. This hardware feature minimizes analog monitoring overhead and is particularly useful in motor control applications as shown in figure 58.

A/D Interrupts

The ST9054 A/D converter provides two interrupt sources, End of Conversion and an Analog Watchdog Request. The interrupt vector register (IVR) provides 1 bit automatically generated in hardware to follow the interrupt source, allowing the User to select the base address of a four byte area of the interrupt vector table in which to store the A/D Interrupt Service Routines. The Analog Watchdog Request requires the User to poll within the Compare Result Register (CRR) to determine which of the four thresholds has been exceeded, the threshold status bits should be reset by software in the service routine. The interrupt pending flags, ECV (End of Conversion, ICR.7) and AWD (Analog Watchdog, ICR.6) should also be reset by the User in the Interrupt service routine before the return.

The ST9054 Analog to Digital converter occupies I/O page 63 (Group F).

Figure 58. Analog Watchdog Used in Motor Speed Control



SOFTWARE DESCRIPTION

Addressing Modes

The ST9054 offers a wide variety of addressing modes and combinations to facilitate full and rapid access to the address spaces while reducing program length. Register addressing (using the working register group mechanism or directly addressed) can be used as 8 or 16 bit values for data or indirect addressing into the memory spaces or the Register File. The selection between Program Memory and Data Memory is performed through the DP bit in the FLAG Register, all subsequent actions on the memory space will affect the selected map only, apart from the memory map to memory map post-increment addressing mode which allows the map to be specified as part of the instruction for both destination and source operands. Apart from the immediate data and condition codes all operands are expressed as register file or memory addresses.

The available addressing modes, with the ST9 macro-assembler notation, are in Table 21.

Combinations Of Available Addressing Modes

Table 22 describes the addressing modes available for the register file and the memory (both as a destination and as a source) for the two operand arithmetic, logic or load instructions.

Table 21. Addressing Mode

Addressing Mode	Notation
Immediate Data	#N #NN
Register Direct	R;r RR;rr
Register Indirect	(R) (r)
Register Indexed	N(r) N(rr)
Memory Direct	NN
Memory Indirect	(RR) (rr)
Memory Indirect with Post-Increment	(rr)+
Memory Indirect with Pre-Decrement	-(rr)
Memory Indexed with Immediate Short Offset	N(rr)
Memory Indexed with Immediate Long Offset	NN(rr)
Memory Indexed with Register Offset	rr(rr)
Memory Indirect Post-Increment to Indirect Register Post-Increment	(rr)+ (r)+
Memory Map to Memory Map both with Post-Increment	(rr)+ (r)+
Bit Address	r.b, (rr).b

Legend:
N = 8 bit Value
NN = 16 bit Value or Address
r = Working Register
R = Directly Addressed Register
( ) = Indirect Addressing
( )+ = Indirect with Post-Increment
-( ) = Indirect with Pre-Decrement
.b = Bit Number (0 to 7)

Table 22. Addressing Mode Permutation for Instructions

Two Operand Arithmetic and Logic Instructions	
Destination	**Source**
Register Direct	Register Direct
Register Direct	Register Indirect
Register Direct	Memory Indirect
Register Direct	Memory Indexed
Register Direct	Memory Indirect with Post- Increment
Register Direct	Memory Indirect with Pre- Decrement
Register Direct	Memory Direct
Register Indirect	Register Direct
Memory Indirect	Register Direct
Memory Indexed	Register Direct
Memory Indirect with Post- Increment	Register Direct
Memory Indirect with Pre- Decrement	Register Direct
Memory Direct	Register Direct

SOFTWARE DESCRIPTION (Continued)

Table 22. Addressing Mode Permutation for Instructions (Continued)

Two Operand Load Instructions	
Destination	**Source**
Register Direct	Register Direct
Register Direct	Register Indirect
Register Direct	Register Indexed
Register Direct	Memory Indirect
Register Direct	Memory Indexed
Register Direct	Memory Indirect with Post- Increment
Register Direct	Memory Indirect with Pre- Decrement
Register Direct	Memory Direct
Register Indirect	Register Direct
Register Indexed	Register Direct
Memory Indirect	Register Direct
Memory Indexed	Register Direct
Memory Indirect with Post- Increment	Register Direct
Memory Indirect with Pre- Decrement	Register Direct
Memory Direct	Register Direct
Two Operand Arithmetic and Logic Instructions	
Destination	**Source**
Register Direct	Immediate
Memory Direct	Immediate
Memory Indirect	Immediate
Two Operand Load Instructions	
Destination	**Source**
Register Direct	Immediate
Memory Direct	Immediate
Memory Indirect	Immediate
Long Indexed Memory (1)	Immediate

Table 22. Addressing Mode Permutation for Instructions (Continued)

Two Operand Arithmetic, Logic & Load Instructions	
Destination	**Source**
Memory Indirect	Memory Indirect
Two Operand Load Instructions (2)	
Destination	**Source**
Register Indirect with Post- Increment	Memory Indirect with Post- Increment
Memory Indirect with Post- Increment	Register Indirect with Post- Increment
Memory Indirect with Post- Increment	Memory Indirect with Post- Increment

Notes:
1. Load Word only
2. Load Byte only

Instruction Set

The ST9054 instruction set consists of 87 instruction types functionally divided into eight groups as in Table 23, they are:

- Load (two operands)
- Arithmetic & Logic (two operands)
- Arithmetic Logic and Shift (one operand)
- Stack (one operand)
- Multiply & Divide (two operands)
- Boolean (one or two operands)
- Program Control (zero to three operands)
- Miscellaneous (zero to two operands)

The wide range of instructions facilitates the full use of the register file and address spaces, reducing execution times, while the register pointers mechanism allows an unmatched code efficiency and ultrafast context switching. A particularly notable feature is the comprehensive "Any Bit, Any Register" (ABAR) addressing capability of the Boolean instructions.

The ST9054 can operate with a wide range of data lengths from single bit, 4-bit nibbles which can be in the form of Binary Coded Decimal (BCD) digits, 8-bit bytes and 16-bit words. The summary on Table 23 shows the instructions belonging to each group and the number of operands required for each. The source operand is "src", "dst" is the destination operand, and "cc" is the condition code selection.

SOFTWARE DESCRIPTION (Continued)

Table 23. Instruction Set Summary

Load Instructions (Two Operands)								
Mnemonic	Operand	Instruction	Flags					
			C	Z	S	V	D	H
LD LDW	dst, src dst, src	Load Load Word	– –	– –	– –	– –	– –	– –
Arithmetic and Logic (Two Operands)								
Mnemonic	Operand	Instruction	Flags					
			C	Z	S	V	D	H
ADD ADDW	dst, src dst, src	Add Add Word	Δ Δ	Δ Δ	Δ Δ	Δ Δ	0 ?	Δ ?
ADC ADCW	dst, src dst, src	Add with Carry Add Word with Carry	Δ Δ	Δ Δ	Δ Δ	Δ Δ	0 ?	Δ ?
SUB SUBW	dst, src dst, src	Subtract Subtract Word	Δ Δ	Δ Δ	Δ Δ	Δ Δ	1 ?	Δ ?
SBC SBCW	dst, src dst, src	Subtract with Carry Subtract Word with Carry	Δ Δ	Δ Δ	Δ Δ	Δ Δ	1 ?	Δ ?
AND ANDW	dst, src dst, src	Logical AND Logical Word AND	– –	Δ Δ	Δ Δ	0 0	– ?	– ?
OR ORW	dst, src dst, src	Logical OR Logical Word OR	– –	Δ Δ	Δ Δ	0 0	– –	– –
XOR XORW	dst, src dst, src	Logical Exclusive OR Logical Word Exclusive OR	– –	Δ Δ	Δ Δ	0 0	– –	– –
CP CPW	dst, src dst, src	Compare Compare Word	Δ Δ	Δ Δ	Δ Δ	Δ Δ	– –	– –
TM TMW	dst, src dst, src	Test Under Mask Test Word Under Mask	– –	Δ Δ	Δ Δ	0 0	– –	– –
TCM TCMW	dst, src dst, src	Test Complement Under Mask Test Word Complement Under Mask	– –	Δ Δ	Δ Δ	0 0	– –	– –

Legend :
0 = Bit set to zero
1 = Bit set to one
Δ = Bit affected
? = Bit status undefined
– = Bit not affected

SOFTWARE DESCRIPTION (Continued)

Table 23. Instruction Set Summary (Continued)

Arithmetic Logic and Shift (One Operand)									
Mnemonic	**Operand**	**Instruction**	**Flags**						
			C	**Z**	**S**	**V**	**D**	**H**
INC INCW	dst dst	Increment Increment Word	– –	Δ Δ	Δ Δ	Δ Δ	– –	– –
DEC DECW	dst dst	Decrement Decrement Word	– –	Δ Δ	Δ Δ	Δ Δ	– –	– –
SLA SLAW	dst dst	Shift Left Arithmetic Shift Word Left Arithmetic	Δ Δ	Δ Δ	Δ Δ	0 0	0 ?	Δ ?
SRA SRAW	dst dst	Shift Right Arithmetic Shift Word Right Arithmetic	Δ Δ	Δ ?	Δ Δ	Δ 0	0 –	Δ –
RRC RRCW	dst dst	Rotate Right through Carry Rotate Word Right through Carry	Δ Δ	Δ ?	Δ Δ	Δ Δ	– –	– –
RLC RLCW	dst dst	Rotate Left through Carry Rotate Word Left through Carry	Δ Δ	Δ ?	Δ Δ	Δ Δ	– –	– –
ROR	dst	Rotate Right	Δ	Δ	Δ	Δ	–	–
ROL	dst	Rotate Left	Δ	Δ	Δ	Δ	–	–
CLR	dst	Clear	–	–	–	–	–	–
CPL	dst	Complement Register	–	Δ	Δ	0	–	–
SWAP	dst	Swap Nibbles	?	Δ	Δ	?	–	–
DA	dst	Decimal Adjust	Δ	Δ	Δ	?	–	–
Stack Instructions (One Operand)									
Mnemonic	**Operand**	**Instruction**	**Flags**						
			C	**Z**	**S**	**V**	**D**	**H**
PUSH PUSHW PEA	src src src	Push on System Stack Push Word on System Stack Push Effective Address on System Stack	– – –	– – –	– – –	– – –	– – –	– – –
POP POPW	dst dst	Pop from System Stack Pop Word from System Stack	– –	– –	– –	– –	– –	– –
PUSHU PUSHUW PEAU	src src src	Push on User Stack Push Word on User Stack Push Effective Address on User Stack	– – –	– – –	– – –	– – –	– – –	– – –
POPU POPUW	dst dst	Pop from User Stack Pop Word from User Stack	– –	– –	– –	– –	– –	– –

SOFTWARE DESCRIPTION (Continued)

Table 23. Instruction Set Summary (Continued)

Multiply and Divide Instructions (Two Operands)									
Mnemonic	**Operand**	**Instruction**	**Flags**						
			C	**Z**	**S**	**V**	**D**	**H**
MUL	dst, src	Multiply 8x8	Δ	Δ	Δ	Δ	0	?
DIV DIVWS	dst, src	Divide 16/8 Divide Word Stepped 32/16	1 ?	Δ ?	Δ ?	? ?	1 ?	? ?
Boolean Instructions (Two Operands)									
Mnemonic	**Operand**	**Instruction**	**Flags**						
			C	**Z**	**S**	**V**	**D**	**H**
BLD	dst, src	Bit Load	–	–	–	–	–	–
BAND	dst, src	Bit AND	–	–	–	–	–	–
BOR	dst, src	Bit OR	–	–	–	–	–	–
BXOR	dst, src	Bit Exclusive OR	–	–	–	–	–	–
Boolean Instructions (One Operand)									
Mnemonic	**Operand**	**Instruction**	**Flags**						
			C	**Z**	**S**	**V**	**D**	**H**
BSET	dst	Bit Set	–	–	–	–	–	–
BRES	dst	Bit Reset	–	–	–	–	–	–
BCPL	dst	Bit Complement	–	–	–	–	–	–
BTSET	dst	Bit Test and Set	–	Δ	Δ	0	–	–
Program Control Instructions (Three Operands)									
Mnemonic	**Operand**	**Instruction**	**Flags**						
			C	**Z**	**S**	**V**	**D**	**H**
CPJFI	dst, src	Compare and Jump on False, Otherwise Post Increment	–	–	–	–	–	–
CPJTI	dst, src	Compare and Jump on True, Otherwise Post Increment	–	–	–	–	–	–

SOFTWARE DESCRIPTION (Continued)

Table 23. Instruction Set Summary (Continued)

Program Control Instructions (Two Operands)								
Mnemonic	**Operand**	**Instruction**	**Flags**					
			C	**Z**	**S**	**V**	**D**	**H**
BTJF	dst, src	Bit Test and Jump if False	–	–	–	–	–	–
BTJT	dst, src	Bit Test and Jump if True	–	–	–	–	–	–
DJNZ	dst, src	Decrement a Working Register and Jump if Not Zero	–	–	–	–	–	–
DWJNZ	dst,src	Decrement a Register Pair and Jump if Not Zero	–	–	–	–	–	–
Program Control Instructions (One Operand)								
Mnemonic	**Operand**	**Instruction**	**Flags**					
			C	**Z**	**S**	**V**	**D**	**H**
JR	cc, dst	Jump Relative if Condition is Met	–	–	–	–	–	–
JP	cc, dst	Jump if Condition is Met	–	–	–	–	–	–
JP	dst	Unconditional Jump	–	–	–	–	–	–
CALL	dst	Unconditional Call	–	–	–	–	–	–
Program Control Instructions (No Operand)								
Mnemonic	**Operand**	**Instruction**	**Flags**					
			C	**Z**	**S**	**V**	**D**	**H**
RET		Return from Subroutine	–	–	–	–	–	–
IRET		Return from Interrupt	Δ	Δ	Δ	Δ	Δ	Δ
WFI		Stop Program Execution and Wait Next Enabled Interrupt. If a DMA request is present the CPU executes the DMA service routine and returns to WFI state.	–	–	–	–	–	–
HALT		Stop Program Execution until RESET	–	–	–	–	–	–
Miscellaneous (Two Operands)								
Mnemonic	**Operand**	**Instruction**	**Flags**					
			C	**Z**	**S**	**V**	**D**	**H**
XCH	dst, src	Exchange Registers	–	–	–	–	–	–

SOFTWARE DESCRIPTION (Continued)

Table 23. Instruction Set Summary (Continued)

Miscellaneous (One Operand)								
Mnemonic	**Operand**	**Instruction**	**Flags**					
			C	**Z**	**S**	**V**	**D**	**H**
SRP	src	Set Register Pointer Long (16 Working Registers)	–	–	–	–	–	–
SRP0	src	Set Register Pointer 0 (8 LSB Working Registers)	–	–	–	–	–	–
SRP1	src	Set Register Pointer 1 (8 MSB Working Registers)	–	–	–	–	–	–
SPP	src	Set Page Pointer	–	–	–	–	–	–
EXT	src	Sign Extend	–	–	–	–	–	–
Miscellaneous (No Operand)								
Mnemonic	**Operand**	**Instruction**	**Flags**					
			C	**Z**	**S**	**V**	**D**	**H**
EI		Enable Interrupts	–	–	–	–	–	–
DI		Disable Interrupts	–	–	–	–	–	–
SCF		Set Carry Flag	1	–	–	–	–	–
RCF		Reset Carry Flag	0	–	–	–	–	–
CCF		Complement Carry Flag	Δ	–	–	–	–	–
SPM		Select Program Memory	–	–	–	–	–	–
SDM		Select Data Memory	–	–	–	–	–	–
NOP		No Operation	–	–	–	–	–	–

Processor Flags

An important aspect of any single chip microcontroller is the ability to test data and make the appropriate action based on the results. In order to provide this facility, register 231 in the Register File is used as a Flag Register. Six bits of this register are used as the following flags:

C - Carry

Z - Zero

S - Sign

V - Overflow

D - Decimal Adjust

H - Half Carry

One of the two remaining bits in the flag register is available to the user (bit 1, F1). Bit 0 is the Program/Data Memory selector bit and is operated on directly by the hardware within the ST9054. The P/$\overline{D}$ pin will follow the status of this bit.

Condition Codes. Flags C, Z, S, and V control the operation of the "conditional" Jump instructions. Table 24 shows the condition codes and the flag settings affecting the jump.

SOFTWARE DESCRIPTION (Continued)

Table 24. Condition Codes Summary

Mnemonic Code	Meaning	Flag Setting
F	Always False	—
T	Always True	—
C	Carry	C = 1
NC	No Carry	C = 0
Z	Zero	Z = 1
NZ	No Zero	Z = 0
PL	Plus	S = 0
MI	Minus	S = 1
OV	Overflow	V = 1
NOV	No Overflow	V = 0
EQ	Equal	Z = 1
NE	Not Equal	Z = 0
GE	Greater Then or Equal	(S xor V) = 0
LT	Less Than	(S xor V) = 1
GT	Greater Than	(Z or (S xor V)) = 0
LE	Less Than or Equal	(Z or (S xor V)) = 1
UGE	Unsigned Greater Than or Equal	C = 0
UL	Unsigned Less Than	C = 1
UGT	Unsigned Greater Than	(C = 0 and Z = 0) = 1
ULE	Unsigned Less Than or Equal	(C or Z) = 1

POWERFUL DEVELOPMENT ENVIRONMENT

ST9 Software Tools

The following Software Tools are available for MS-DOS, SUN-3 and SUN-4 operating systems:

AST9 high-level macro assembler with predefinited macro instructions (IF/ELSE, WHILE, DO, LOOP, SWITCH, BREAK, PROCEDURE, RESTURN).

LST9 Incremental Linker/Loader.

CST9 Optimised C-Compiler (ANSI STANDARD).

ARST9 Library Archiver.

SIMST9 Software Simulator with realtime emulation executor

ST9054 Hardware Emulator. Realtime emulation of the ST9054 in all packaging options is performed by a modular emulation system, interfaced to the host computer through an RS232 channel, whit powerful hardware breakpoints, on-line assembler/disassembler, emulation and trace memory. The emulator is fully supported by a simbolic on-line debugger and help facility.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	– 0.3 to 7.0	V
AV_{DD}, AV_{SS}	Analog Supply Voltage	$V_{SS} \le AV_{SS} < AV_{DD} \le V_{DD}$	V
V_I	Input Voltage	V_{SS} – 0.3 to V_{DD} +0.3	V
V_O	Output Voltage	V_{SS} – 0.3 to V_{DD} +0.3	V
T_{STG}	Storage Temperature	– 55 to + 150	°C

Note: Stresses above those listed as "absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value		Unit
		Min.	Max.	
T_A	Operating Temperature	– 40	85	°C
V_{DD}	Operating Supply Voltage	4.5	5.5	V
f_{OSCE}	External Oscillator Frequency		24	MHz
f_{OSCI}	Internal Oscillator Frequency		12	MHz

DC ELECTRICAL CHARACTERISTICS

(V_{DD} = 5V ± 10% T_A = – 40 °C to + 85°C, unless otherwise specified)

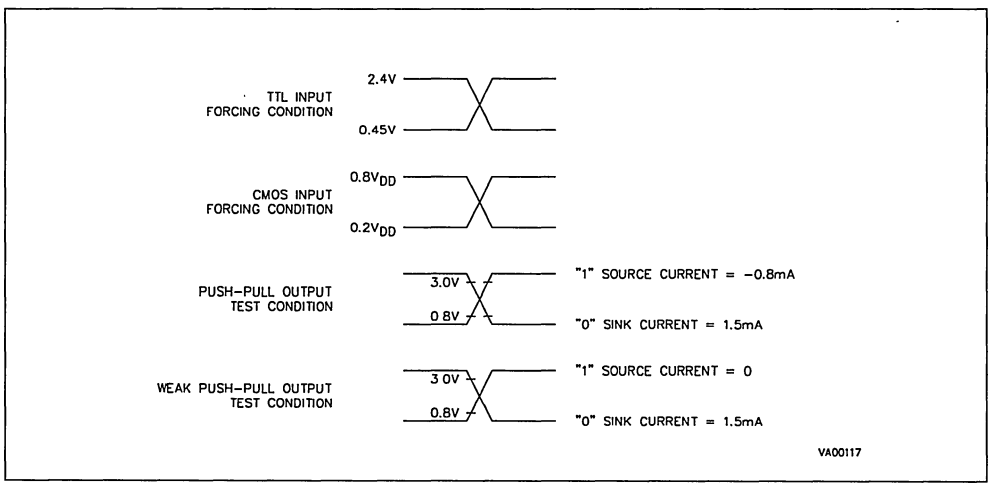
Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
V_{IHCK}	Clock Input High Level	External Clock	0.7 V_{DD}		V_{DD} + 0.3	V
V_{ILCK}	Clock Input Low Level	External Clock	– 0.3		0.3 V_{DD}	V
V_{IH}	Input High Level	TTL	2.0		V_{DD} + 0.3	V
		CMOS	0.7 V_{DD}		VDD + 0.3	V
V_{IL}	Input Low Level	TTL	– 0.3		0.8	V
		CMOS	– 0.3		0.3 V_{DD}	V
V_{IHRS}	Reset Input High Level		0.7 V_{DD}		V_{DD} + 0.3	V
V_{ILRS}	Reset Input Low Level		–0.3		0.3 V_{DD}	V
V_{HYRS}	Reset Input Hysteresis		0.3		1.5	V
V_{OH}	Output High Level	Push Pull, Iload = – 0.8mA	V_{DD} – 0.8			V
V_{OL}	Output Low Level	Push Pull or Open Drain, Iload = – 1.6mA			0.4	V

DC ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
I_{WPU}	Weak Pull-up Current	Bidirectional Weak Pull-up, V_{OL} = 0V	– 80	– 200	– 420	µA
I_{APU}	Active Pull-up Current, for INT0 and INT7 only	V_{IN} < 0.8V	– 80	– 200	– 420	µA
I_{LKIO}	I/O Pin Input Leakage	Input/Tri-State, 0V < V_{IN} < V_{DD}	– 10		+ 10	µA
I_{LKRS}	Reset Pin Input Leakage	0V < V_{IN} < V_{DD}	– 30		+ 30	µA
I_{LKAD}	A/D Pin Input Leakage	Alternate Function, Open Drain, 0V < V_{IN} < V_{DD}	– 3		+ 3	µA
I_{LKAP}	Active Pull-up Input Leakage	0V < V_{IN} < 0.8V	– 10		+ 10	µA
I_{LKOS}	OSCIN Pin Input Leakage	0V < V_{IN} < V_{DD}	– 10		+ 10	µA
I_{DD}	Run Mode Current	24MHz, Note 1		32	70	mA
		4MHz, Note 1		6	12	mA
I_{DP2}	Run Mode Current Prescale by 2	24MHz, Note 1		19	40	mA
		4MHz, Note 1		4	8	mA
I_{WFI}	WFI Mode Current	24MHz, Note 1		9	18	mA
		4MHz, Note 1		2.5	5	mA
I_{HALT}	HALT Mode Current	24MHz, Note 1			100	µA

Note:
1. All I/O Ports are configured in Bidirectional Weak Pull-up Mode with no DC load, External Clock pin (OSCIN) is driven by square wave external clock. No peripheral working. External interface not active (Internal Program Execution).

DC TEST CONDITIONS



AC ELECTRICAL CHARACTERISTICS

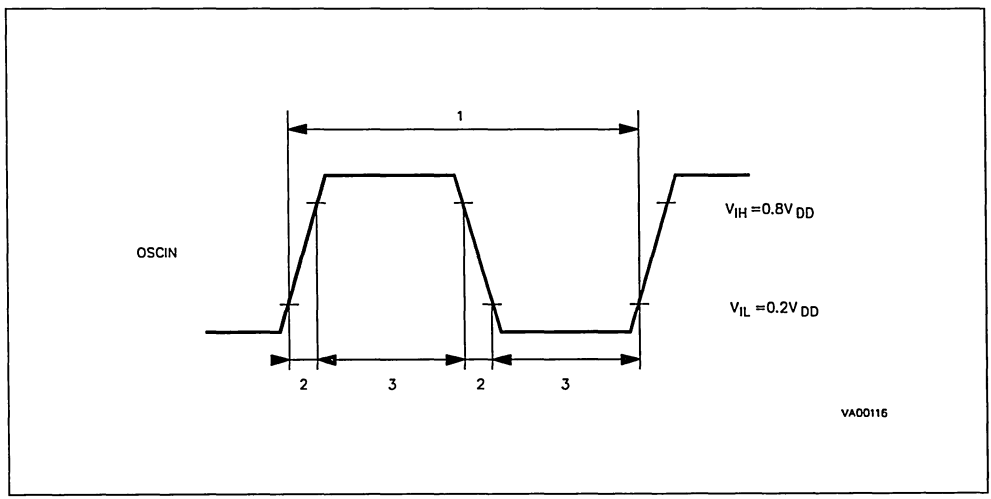
CLOCK TIMING TABLE

(V_{DD} = 5V ± 10%, T_A = − 40°C to + 85°C, unless otherwise specified)

N°	Symbol	Parameter	Value		Unit	Note
			Min.	Max.		
1	TpC	OSCIN Clock Period	41.5		ns	1
			83		ns	2
2	TrC, TfC	OSCIN Rise and Fall Time		12	ns	
3	TwCL, TwCH	OSCIN Low and High Width	25	12	ns	1
			38		ns	2

Notes:
1. Clock divided by 2 internally (MODER.DIV2=1)
2. Clock not divided by 2 internally (MODER.DIV2=0)

CLOCK TIMING



EXTERNAL BUS TIMING TABLE

(V_{DD} = 5V ± 10%, T_A = – 40 °C to + 85 °C, Cload = 50pF, CPUCLK = 12MHz, unless otherwise specified)

N°	Symbol	Parameter	Value (Note)				Unit
			OSCIN Divided By 2	OSCIN Not Divided By 2	Min.	Max.	
1	TsA (AS)	Address Set-up Time before $\overline{AS}$ ↑	TpC (2P+1) –22	TWCH+PTpC –18	20		ns
2	ThAS (A)	Address Hold Time after $\overline{AS}$ ↑	TpC –17	TwCL –13	25		ns
3	TdAS (DR)	$\overline{AS}$ ↑ to Data Available (read)	TpC (4P+2W+4) –52	TpC (2P+W+2) –51		115	ns
4	TwAS	$\overline{AS}$ Low Pulse Width	TpC (2P+1) –7	TwCH+PTpC –3	35		ns
5	TdAz (DS)	Address Float to $\overline{DS}$ ↓	0	0	0		ns
6	TwDSR	$\overline{DS}$ Low Pulse Width (read)	TpC (4P+2W+3) –20	TwCH+TpC (2P+W+1) –16	105		ns
7	TwDSW	$\overline{DS}$ Low Pulse Width (write)	TpC (2P+2W+2) –13	TpC (P+W+1) –13	70		ns
8	TdDSR (DR)	$\overline{DS}$ ↓ to Data Valid Delay (read)	TpC (4P+2W-3) –50	TwCH+TpC(2P+W+1) – 46		75	ns
9	ThDR (DS)	Data to $\overline{DS}$ ↑ Hold Time (read)	0	0	0		ns
10	TdDS (A)	$\overline{DS}$ ↑ to Address Active Delay	TpC –7	TwCL –3	35		ns
11	TdDS (AS)	$\overline{DS}$ ↑ to $\overline{AS}$ ↓ Delay	TpC –18	TwCL –14	24		ns
12	TsR/W (AS)	R/$\overline{W}$ Set-up Time before $\overline{AS}$ ↑	TpC (2P+1) –22	TwCH+PTpC –18	20		ns
13	TdDSR (R/W)	$\overline{DS}$ ↑ to R/$\overline{W}$ and Address Not Valid Delay	TpC –9	TwCL –5	33		ns
14	TdDW (DSW)	Write Data Valid to $\overline{DS}$ ↓ Delay (write)	TpC (2P+1) –32	TwCH+PTpC –28	10		ns
15	ThDS (DW)	Data Hold Time after DS ↑ (write)	TpC –9	TwCL –5	33		ns
16	TdA (DR)	Address Valid to Data Valid Delay (read)	TpC (6P+2W+5) –68	TwCH+TpC (3P+W+2) –64		140	ns
17	TdAs (DS)	$\overline{AS}$ ↑ to $\overline{DS}$ ↓ Delay	TpC –18	TwCL –14	24		ns

Note: The value left hand two columns show the formula used to calculate the timing minimum or maximum from the oscillator clock period, prescale value and number of wait cycles inserted.
The value right hand two columns show the timing minimum and maximum for an external clock at 24 MHz divided by 2, prescaler value of zero and zero wait status.

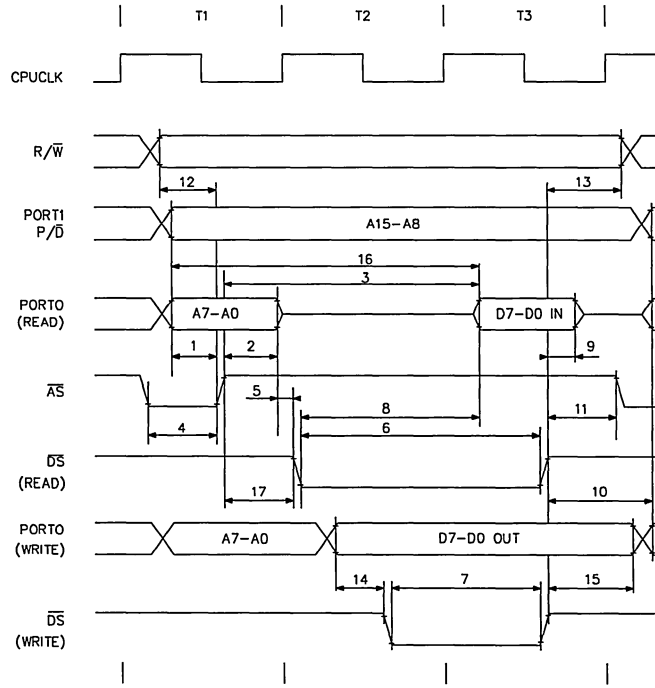
Legend:
P = Clock Prescaling Value
W = Wait Cycles
TpC = OSCIN Period
TwCH = High Level OSCIN half period
TwCL = Low Level OSCIN half period

EXTERNAL WAIT TIMING TABLE (V_{DD} = 5V ± 10%, T_A = –40°C to +85°C, Cload = 50pF, INTCLK = 12MHz, Push-pull output configuration, unless otherwise specified)

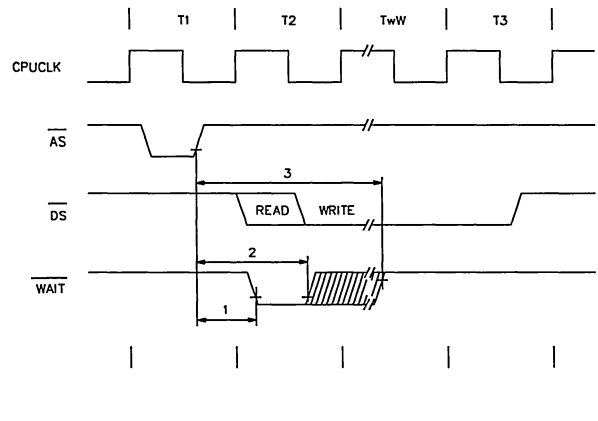
N°	Symbol	Parameter	Value (Note)				Unit
			OSCIN Divided By 2	OSCIN Not Divided By 2	Min.	Max.	
1	TdAS (WAIT)	$\overline{AS}$ ↑ to $\overline{WAIT}$ ↓ Delay	2(P+1)TpC –29	(P+1)TpC –29		40	ns
2	TdAS (WAIT)	$\overline{AS}$ ↑ to $\overline{WAIT}$ ↑ Minimum Delay	2(P+W+1)TpC –4	(P+W+1)TpC –4	80		ns
3	TdAS (WAIT)	$\overline{AS}$ ↑ to $\overline{WAIT}$ ↑ Maximum Delay	2(P+W+1)TpC – 29	(P+W+1)TpC –29		83W+40	ns

Note: The value left hand two columns show the formula used to calculate the timing minimum or maximum from the oscillator clock period, prescale value and number of wait cycles inserted.
The value right hand two columns show the timing minimum and maximum for an external clock at 24 MHz divided by 2, prescale value of zero and zero wait status.

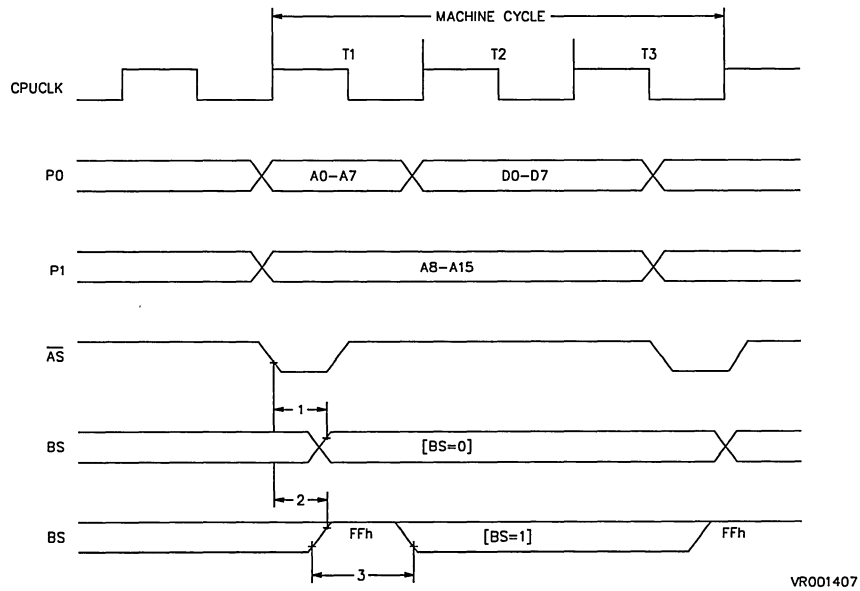
EXTERNAL BUS TIMING



EXTERNAL WAIT TIMING



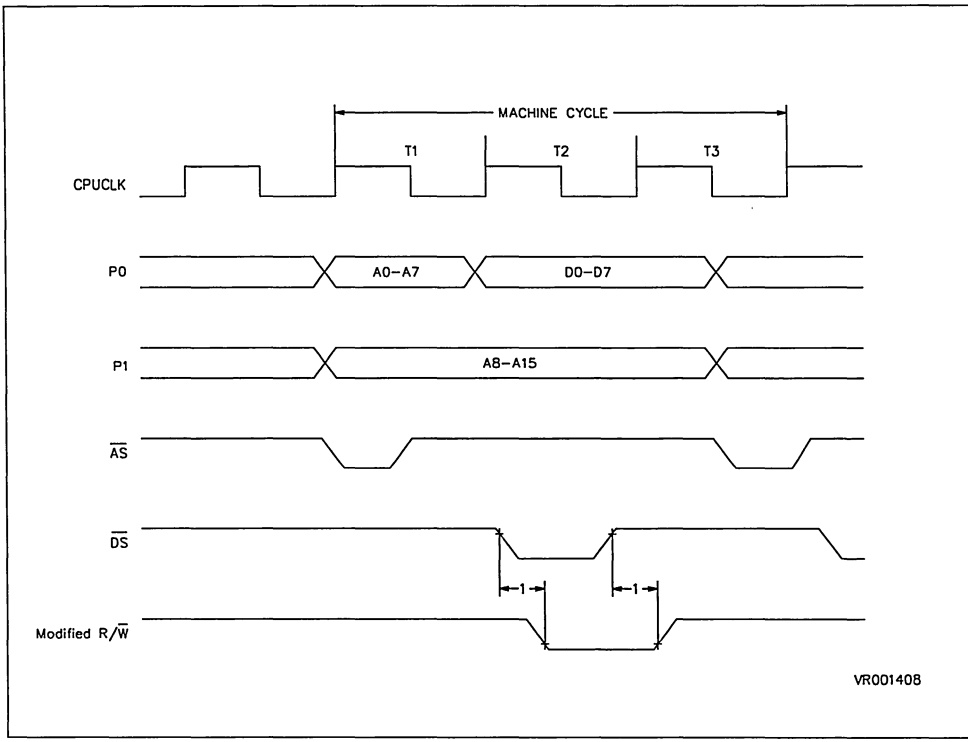
BANK SWITCH, AC-TIMING



N°	Symbol	Parameter	Value		Unit	Note
			Min.	Max.		
1	tBAS	Bank switch from $\overline{AS}$ High to low transition		45	nS	1
2	tBLH	Bank switch rising edge from $\overline{AS}$ High to Low transition		40	nS	2
3	tBSW	Bank switch -FFh- pulse width		cpuclk	nS	1

Notes :
1 Page 0 R255.BS=0
2 Page0 R255.BS=0

R/$\overline{W}$ MODIFIED FROM $\overline{DS}$ DELAY



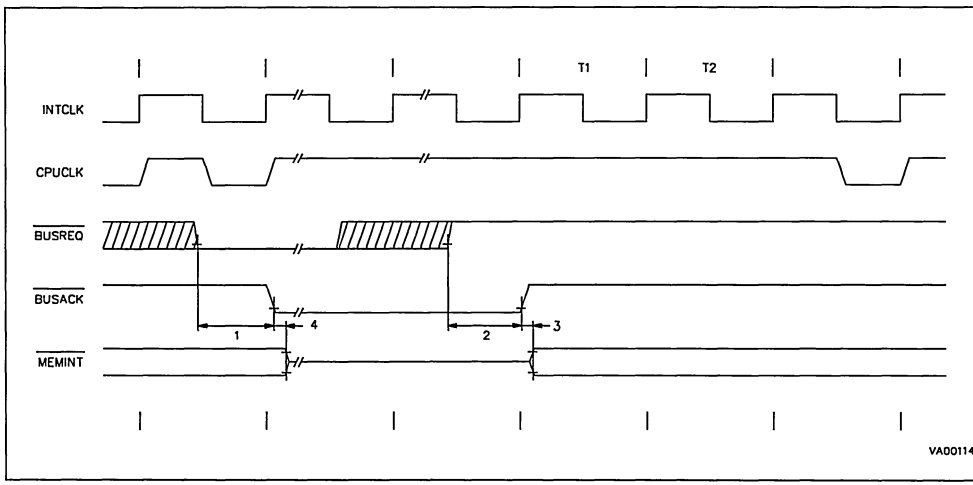
N°	Symbol	Parameter	Value		Unit
			Min.	Max.	
1	tRMD	R/$\overline{W}$ modified from $\overline{DS}$ delay		35	nS

BUS REQUEST/ACKNOWLEDGE TIMING TABLE (V_{DD} = 5V ± 10%, T_A = −40°C to +85°C, Cload = 50pF, INTCLK = 12MHz, Push-pull output configuration, unless otherwise specified)

N°	Symbol	Parameter	Value (Note)				Unit
			OSCIN Divided By 2	OSCIN Not Divided By 2	Min.	Max.	
1	TdBR (BACK)	$\overline{BREQ}$ ↓ to $\overline{BUSACK}$ ↓	TpC+8	TwCL+12	50		ns
			TpC(6P+2W+7)+65	TpC(3P+W+3)+TwCL+65		360	ns
2	TdBR (BACK)	$\overline{BREQ}$ ↑ to $\overline{BUSACK}$ ↑	3TpC+60	TpC+TwCL+60		185	ns
3	TdBACK (BREL)	$\overline{BUSACK}$ ↓ to Bus Release	20	20		20	ns
4	TdBACK (BACT)	$\overline{BUSACK}$ ↑ to Bus Active	20	20		20	ns

Note: The value left hand two columns show the formula used to calculate the timing minimum or maximum from the oscillator clock period, prescale value and number of wait cycles inserted.
The value right hand two columns show the timing minimum and maximum for an external clock at 24 MHz divided by 2, prescale value of zero and zero wait status.

BUS REQUEST/ACKNOWLEDGE TIMING



Note : MEMINT = group of memory interface signals : $\overline{AS}$, $\overline{DS}$, R/$\overline{W}$, P00-P07, P10-P17.

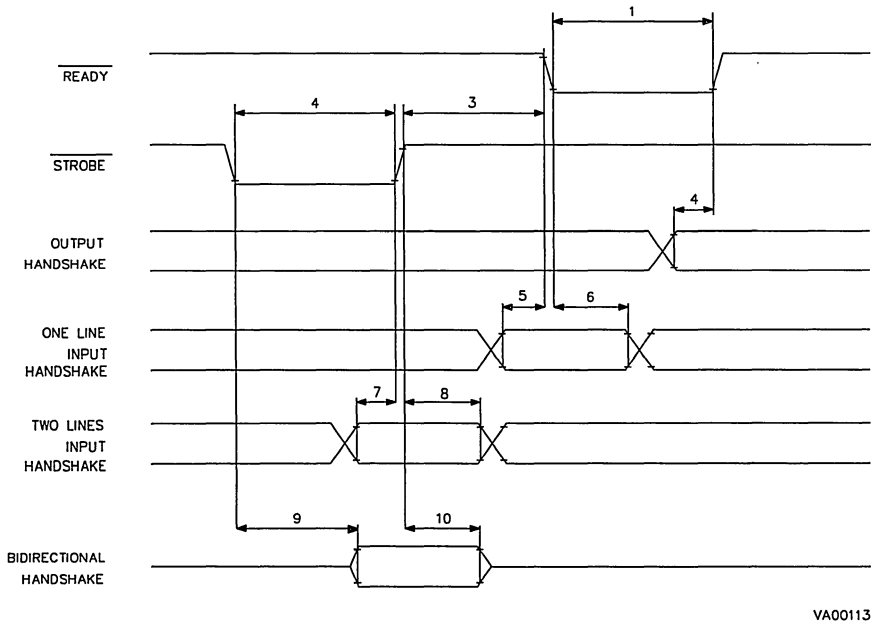
HANDSHAKE TIMING TABLE (V_{DD} = 5V ± 10%, T_A = –40°C to +85°C, Cload = 50pF, INTCLK = 12MHz, Push-pull output configuration, unless otherwise specified)

N°	Symbol	Parameter	Value (Note)				Min.	Max.	Unit
			OSCIN Divided By 2		OSCIN Not Divided By 2				
			Min.	Max.	Min.	Max.			
1	TwRDY	RDRDY, WRRDY Pulse Width in One Line Handshake	2TpC (P+W+1) –18		Tp (P+W+1) – 18		65		ns
2	TwSTB	$\overline{RDSTB}$, $\overline{WRSTB}$ Pulse Width	2TpC+12		TpC+12		95		ns
3	TdST (RDY)	$\overline{RDSTB}$, or $\overline{WRSTB}$ ↑ to RDRDY or WRRDY ↓		TpC+45		(TpC-TwCL) +45		87	ns
4	TsPD (RDY)	Port Data to RDRDY ↑ Set-up Time	(2P+2W+1) TpC –25		TwCH+(W+P) TpC –25		16		ns
5	TsPD (RDY)	Port Data to WRRDY ↓ Set-up Time in One Line Handshake	43		43		43		ns
6	ThPD (RDY)	Port Data to WRRDY ↓ Hold Time in One Line Handshake	0		0		0		ns
7	TsPD (STB)	Port Data to $\overline{WRSTB}$ ↑ Set-up Time	10		10		10		ns
8	ThPD (STB)	Port Data to WRSTB ↑ Hold Time	25		25		25		ns
9	TdSTB (PD)	$\overline{RDSTBD}$ ↑ to Port Data Delay Time in Bidirectional Handshake		35		35		35	ns
10	TdSTB (PHZ)	$\overline{RDSTB}$ ↑ to Port High-Z Delay Time in Bidirectional Handshake		25		25		25	ns

Note: The value left hand two columns show the formula used to calculate the timing minimum or maximum from the oscillator clock period, prescale value and number of wait cycles inserted.
The value right hand two columns show the timing minimum and maximum for an external clock at 24 MHz divided by 2, prescaler value of zero and zero wait status.

Legend:
P = Clock Prescaling Value (R235.4,3,2)
W = Programmable Wait Cycles (R252.2.1.0/5,4,3) + External Wait Cycles

HANDSHAKE TIMING

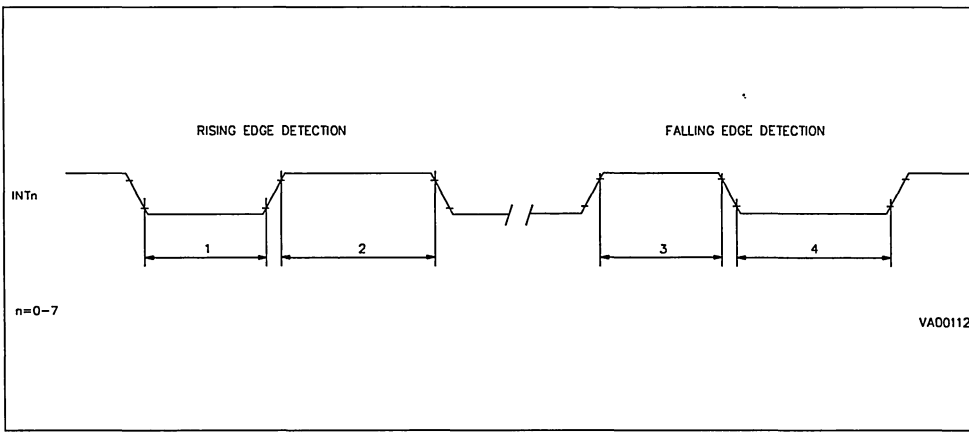


EXTERNAL INTERRUPT TIMING TABLE (V_{DD} = 5V ± 10%, T_A = –40°C to +85°C, Cload = 50pF, INTCLK = 12MHz, Push-pull output configuration, unless otherwise specified)

N°	Symbol	Parameter	Value (Note)				Unit
			OSCIN Divided By 2 Min.	OSCIN Not Divided By 2 Min.	Min.	Max.	
1	TwLR	Low Level Minimum Pulse Width in Rising Edge Mode	2TpC+12	TpC+12	95		ns
2	TwHR	High Level Minimum Pulse Width in Rising Edge Mode	2TpC+12	TpC+12	95		ns
3	TwHF	High Level Minimum Pulse Width in Falling Edge Mode	2TpC+12	TpC+12	95		ns
4	TwLF	Low Level Minimum Pulse Width in Falling Edge Mode	2TpC+12	TpC+12	95		ns

Note: The value left hand two columns show the formula used to calculate the timing minimum or maximum from the oscillator clock period, prescale value and number of wait cycles inserted.
The value right hand two columns show the timing minimum and maximum for an external clock at 24 MHz divided by 2, prescale value of zero and zero wait status.

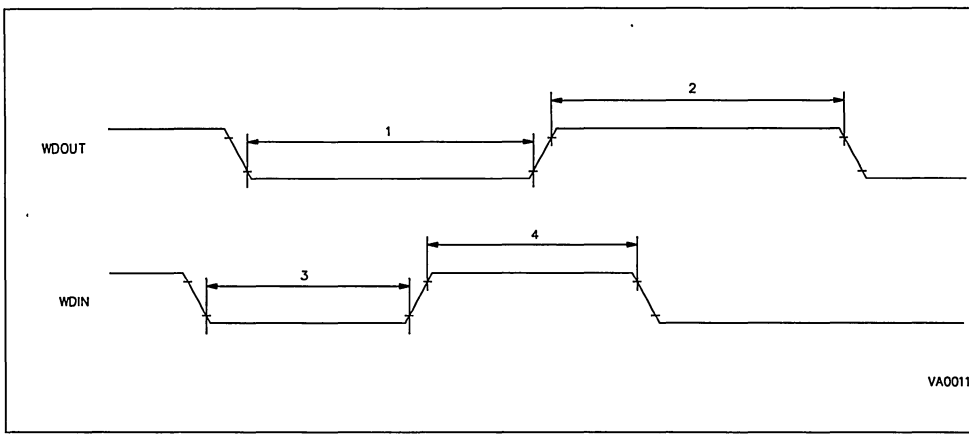
EXTERNAL INTERRUPT TIMING



WATCHDOG TIMING TABLE (V_{DD} = 5V ± 10%, T_A = −40°C to +85°C, Cload = 50pF, INTCLK =12MHz, Output Alternate Function set as Push-pull)

N°	Symbol	Parameter	Value		Unit
			Min.	Max.	
1	TwWDOL	WDOUT Low Pulse Width	620		ns
2	TwWDOH	WDOUT High Pulse Width	620		ns
3	TwWDIL	WDIN Low Pulse Width	350		ns
4	TwWDIH	WDIN High Pulse Width	350		ns

WATCHDOG TIMING

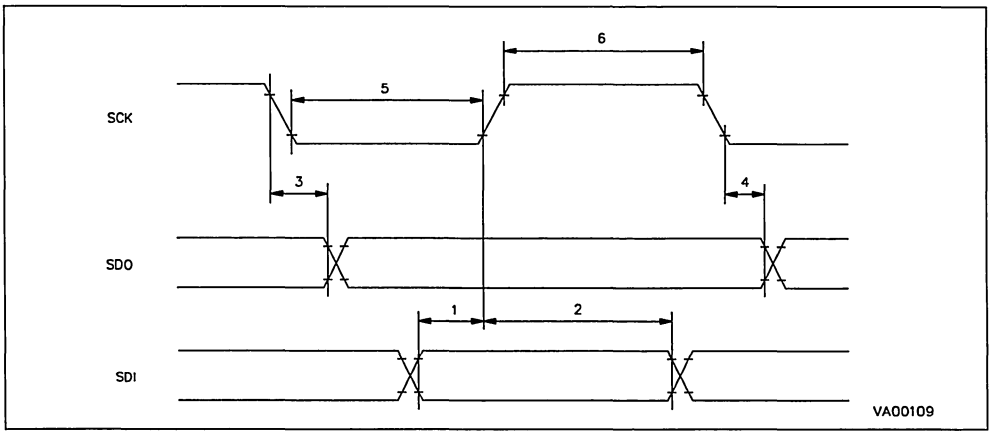


SPI TIMING TABLE (V_{DD} = 5V ± 10%, T_A = –40°C to +85°C, Cload = 50pF, INTCLK = 12MHz, Output Alternate Function set as Push-pull)

N°	Symbol	Parameter	Value		Unit
			Min.	Max.	
1	TsDI	Input Data Set-up Time	100		ns
2	ThDI (1)	Input Data Hold Time	1/2 TpC+100		ns
3	TdOV	SCK to Output Data Valid		100	ns
4	ThDO	Output Data Hold Time	-20		ns
5	TwSKL	SCK Low Pulse Width	300		ns
6	TwSKH	SCK High Pulse Width	300		ns

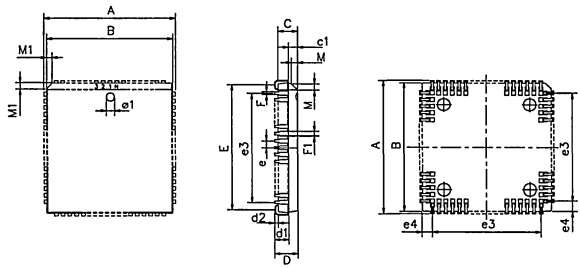
Note: 1. TpC is the Clock period.

SPI TIMING



PACKAGE MECHANICAL DATA

Figure 57. 84-Lead Plastic Leaded Chip Carrier



DIM	MM			INCHES		
	Min	Typ	Max	Min	Typ	Max
A	30.10		30.35	1.18		1.19
B	29.20		29.41	1.14		1.15
C						
C1						
D	4.20		5.08	0.16		0.19
D1		2.54			0.02	
D2		0.56				
D3				1.09		1.12
E	27.69		28.70		0.04	
e		1.27				
e3					0.01	
F		0.38				
F1						0.003
G			0.101			
H		1.27			0.04	
H1		1.14			0.04	

ORDERING INFORMATION

Sales Type	Frequency	Temperature Range	Package
ST9054C6/XX	24MHz	-40°C to +85°C	PLCC84
ST9054C1/XX	24MHz	0°C to 70°C	PLCC84

Note : "XX" is the ROM code identifier that is allocated by SGS-THOMSON after receipt of all required options and the related ROM file.

ST9054 OPTION LIST

Please copy this page (enlarge if possible) and complete ALL sections. Send the form, with the ROM code image required, to your local SGS-THOMSON sales office.

Customer Company : [.....]

Company Address : [.....]
[.....]

Telephone : [.....]

FAX : [.....]

Contact : [.....] Telephone (Direct) : [.....]

Please confirm device required :

Temperature Range [ ] (t)

Special Marking [ ] (y/n) 11 characters [| | | | | | | | | | |] (N)

Notes :

(t) 1 = 0 to +70°C, 6 = -40 to +85°C
(N) Available : ASCII 020h - 05Fh

Please consult your local SGS-THOMSON sales office for other marking details

ROMLESS OPTION (consult text)
[ ] YES [ ] NO
If yes, identify required pin (Port.bit)
[ ] P3.7 [ ] P2.0

Code : [ ] EPROM (27256)
[ ] HEX format files on IBM-PC® compatible disk
filename : [.....]

Confirmation : [ ] Code checked with EPROM device in application

Yearly Quantity forecast : [.....] k units
- for a period of : [.....] years
Preferred Production start dates : [.....] (YY/MM/DD)

Customer Signature : [.....]

Date : [.....]

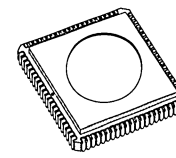
SGS-THOMSON MICROELECTRONICS

ST90E54
ST90T54

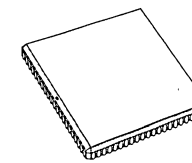
32K EPROM HCMOS MCUs WITH BANKSWITCH AND A/D CONVERTER

ADVANCE DATA

- Single chip microcontroller with 32K bytes of EPROM, 1,280 bytes of static RAM and 256 bytes of register file with 224 general purpose registers available as RAM, accumulators or index pointers.
- Bank-Switch logic allowing a maximum addressing capability of 8M bytes in both program and data spaces (16M byte total).
- 8/16 bit CORE with full feature DMA controller, a powerful interrupt handler and a Standard Serial Peripheral Interface (SPI) handling S-bus, I^2C-bus, IM-bus and Standard Serial Peripheral Interfaces.
- Up to 8 external interrupts edge-selectable plus 1 non-maskable interrupt.
- 16 bit programmable Timer with 8 bit Prescaler, able to be used as a Watchdog Timer for system integrity.
- Three 16 bit Multifunction Timer modules, each with an 8 bit prescaler and 13 operating modes, allowing simple use for complex waveform generation and measurement, PWM functions and many other system timing operations.
- 8 channel Analog to Digital Converter, with integral sample and hold, fast 11µs conversion time, 8 bit ±1/2 LSB resolution with Analog Watchdog on two channels.
- Two full function Serial Communications Interfaces with 110 to 375000 baud rate generator, asynchronous and byte synchronous capability (fully programmable format) and address/wake-up bit option.
- On-chip DMA channels associated to the Multifunction Timers and the Serial Communications Interface.
- Up to nine 8 bit I/O ports with programmable input thresholds and output characteristics. Alternative functions allow the full use of all pins.
- Powerful software development tools, including assembler, linker, C-compiler, archiver, software and hardware emulators.
- 84-lead Window Ceramic Leaded Chip Carrier package for ST90E54.
- 84-lead Plastic Leaded Chip Carrier package for ST90T54.



CLCC84-W



PLCC84

(Ordering Information at the end of the datasheet)

Figure 1. ST90E54 Block Diagram

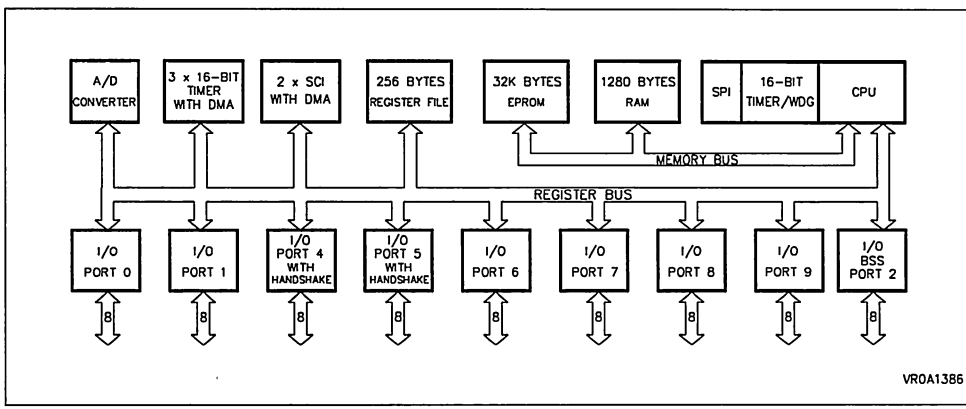
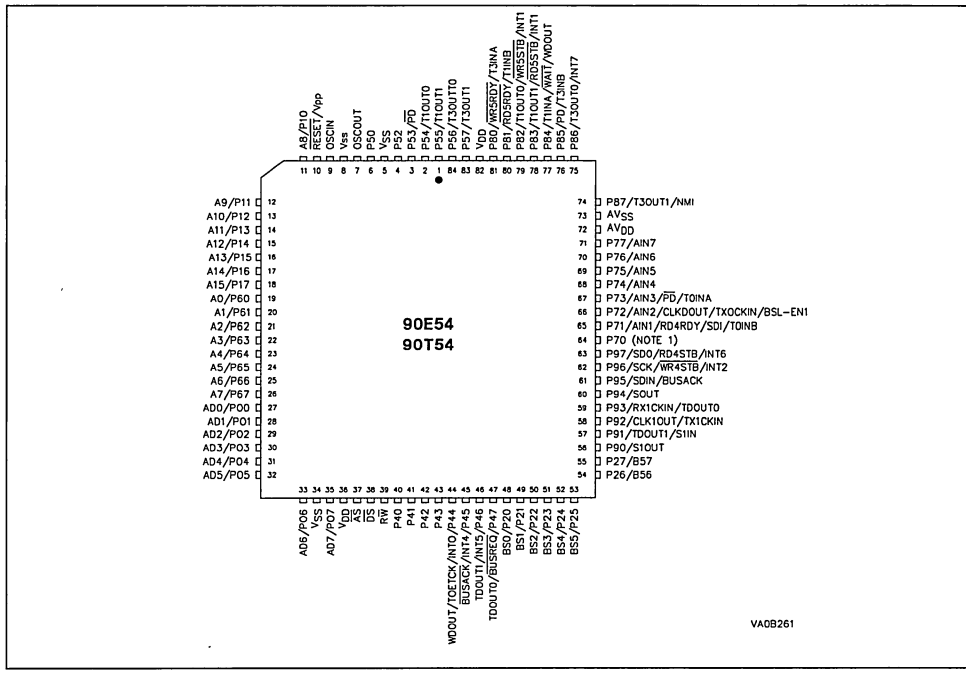


Figure 2. ST90E54,T54 Pin Configuration



Note 1 : P70/AIN0/ADTRG/$\overline{WR4DRDY}$/RX0CKIN/WDIN/BSH_EN1.

GENERAL DESCRIPTION

The ST90E54 and ST90T54 (following mentioned as ST90E54) are EPROM members of the ST9 family of microcontrollers, in windowed ceramic (E) and plastic OTP (T) packages respectively, completely developed and produced by SGS-THOMSON Microelectronics using a proprietary n-well HCMOS process.

The EPROM parts are fully compatible with their ROM versions and this datasheet will thus provide only information specific to the EPROM based devices.

THE READER IS ASKED TO REFER TO THE DATASHEET OF THE ST9054 ROM-BASED DEVICE FOR FURTHER DETAILS.

The EPROM ST90E54 may be used for the prototyping and pre-production phases of development, and can be configured as: standalone microcontrollers with 32K bytes of on-chip EPROM, microcontrollers able to manage up to 120K bytes of external memory, (16M byte with the Bankswitch logic), or as parallel processing elements in a system with other processors and peripheral controllers.

A key point of the ST90E54 architecture is its modular approach which allows software commonality with all other members of the ST9 family.

The nucleus of the modular design of the ST90E54 is the advanced Core which includes the Central Processing Unit (CPU), the Register File, a 16 bit Timer/Watchdog with 8 bit Prescaler, a Serial Peripheral Interface supporting S-bus, I^2C-bus and IM-bus Interface, plus two 8 bit I/O ports. The Core has independent memory and register buses allowing a high degree of pipelining to add to the efficiency of the code execution speed of the extensive instruction set.

GENERAL DESCRIPTION (Continued)

The powerful I/O capabilities demanded by microcontroller applications are fulfilled by the ST90E54 with up to 72 I/O lines dedicated to digital Input/Output. These lines are grouped into up to nine 8 bit I/O Ports and can be configured on a bit basis under software control to provide timing, status signals, address and data buses for interfacing external memory, timer inputs and outputs, analog inputs, external interrupts and serial or parallel I/O with or without handshake.

Three basic memory spaces are available to support this wide range of configurations: Program Memory (internal and external), Data Memory (internal and external) and the Register File, which includes the control and status registers of the on-chip peripherals.

Three 16 bit MultiFunction Timers, each with an 8 bit Prescaler and 13 operating modes allow simple use for complex waveform generation and measurement, PWM functions and many other system timing functions by the usage of the two associated DMA channels for each timer.

In addition there is an 8 channel Analog to Digital Converter with integral sample and hold, fast 11µs conversion time and 8 bit ±1/2 LSB resolution. An Analog Watchdog feature is included for two input channels.

Completing the device are two full duplex Serial Communications Interfaces, each with an integral 110 to 375000 baud rate generator, asynchronous and byte synchronous capability (fully programmable format) and associated address/wake-up option, plus two DMA channels.

PIN DESCRIPTION

$\overline{AS}$. *Address Strobe (output, active low, 3-state).* Address Strobe is pulsed low once at the beginning of each memory cycle. The rising edge of $\overline{AS}$ indicates that address, Read/Write (R/$\overline{W}$), and Data Memory signals are valid for program or data memory transfers. Under program control, $\overline{AS}$ can be placed in a high-impedance state along with Port 0, Port 1, Port 6, Data Strobe ($\overline{DS}$) and R/$\overline{W}$.

$\overline{DS}$. *Data Strobe (output, active low, 3-state).* Data Strobe provides the timing for data movement to or from Port 0 for each memory transfer. During a write cycle, data out is valid at the leading edge of $\overline{DS}$. During a read cycle, Data In must be valid prior to the trailing edge of $\overline{DS}$. When the ST90E54 accesses on-chip memory, $\overline{DS}$ is held high during the whole memory cycle. It can be placed in a high impedance state along with Port 0, Port 1, Port 6, $\overline{AS}$ and R/$\overline{W}$.

R/$\overline{W}$. *Read/Write (output, 3-state).* Read/Write determines the direction of data transfer for external memory transactions. R/$\overline{W}$ is low when writing to external program or data memory, and high for all other transactions. The timing of R/$\overline{W}$ may be modified when using the Bank Switch Logic memory expansion to prevent external timing conflicts. R/$\overline{W}$ can be placed in a high impedance state along with Port 0, Port 1, Port 6, $\overline{AS}$ and $\overline{DS}$.

$\overline{RESET}$/V_{PP}. *Reset (input, active low) or V_{PP} (input).* The ST9 is initialised by the Reset signal. With the deactivation of $\overline{RESET}$, program execution begins from the Program memory location pointed to by the vector contained in program memory locations 00h and 01h. In the EPROM programming Mode, this pin acts as the programming voltage input VPP.

OSCIN, OSCOUT. *Oscillator (input and output).* These pins connect a parallel-resonant crystal (24MHz maximum), or an external source to the on-chip clock oscillator and buffer. OSCIN is the input of the oscillator inverter and internal clock generator; OSCOUT is the output of the oscillator inverter.

AV_{DD}. Analog V_{DD} of the Analog to Digital Converter.

AV_{SS}. Analog V_{SS} of the Analog to Digital Converter.

V_{DD}. Main Power Supply Voltage (5V±10%)

V_{SS}. Digital Circuit Ground.

P0.0-P0.7, P1.0-P1.7, P2.0-P2.7, P4.0-P4.7, P5.0-P5.7, P6.0-P6.7, P7.0-P7.7, P8.0-P8.7, P9.0-P9.7 *I/O Port Lines (Input/Output, TTL or CMOS compatible).* 8 lines grouped into I/O ports of 8 bits, bit programmable under program control as general purpose I/O or as Alternate functions (see next section).

I/O Port Alternate Functions.

Each pin of the I/O ports of the ST90E54 may assume software programmable Alternative Functions as shown in the Pin Configuration Drawings. Table 1 shows the Functions allocated to each I/O Port pins.

PIN DESCRIPTION (Continued)

Table 1. ST90E54,T54 I/O Port Alternate Function Summary

I/O PORT Port.bit	Name	Function IN/OUT	Alternate Function	Pin
P0.0	A0/D0	I/O	Address/Data bit 0 mux	27
P0.1	A1/D1	I/O	Address/Data bit 1 mux	28
P0.2	A2/D2	I/O	Address/Data bit 2 mux	29
P0.3	A3/D3	I/O	Address/Data bit 3 mux	30
P0.4	A4/D4	I/O	Address/Data bit 4 mux	31
P0.5	A5/D5	I/O	Address/Data bit 5 mux	32
P0.6	A6/D6	I/O	Address/Data bit 6 mux	33
P0.7	A7/D7	I/O	Address/Data bit 7 mux	35
P1.0	A8	O	Address bit 8	11
P1.1	A9	O	Address bit 9	12
P1.2	A10	O	Address bit 10	13
P1.3	A11	O	Address bit 11	14
P1.4	A12	O	Address bit 12	15
P1.5	A13	O	Address bit 13	16
P1.6	A14	O	Address bit 14	17
P1.7	A15	O	Address bit 15	18
P2.0	BS0	O	Bank Switch Address 0 (A16)	48
P2.1	BS1	O	Bank Switch Address A17	49
P2.2	BS2	O	Bank Switch Address A18	50
P2.3	BS3	O	Bank Switch Address A19	51
P2.4	BS4	O	Bank Switch Address A20	52
P2.5	BS5	O	Bank Switch Address A21	53
P2.6	BS6	O	Bank Switch Address A22	54
P2.7	BS7	O	Bank Switch Address A23	55
P4.0		I/O	I/O Handshake Port 4	40
P4.1		I/O	I/O Handshake Port 4	41
P4.2		I/O	I/O Handshake Port 4	42
P4.3		I/O	I/O Handshake Port 4	43
P4.4	INT0	I	External interrupt 0	44

PIN DESCRIPTION (Continued)

Table 1. ST90E54,T54 I/O Port Alternate Function Summary (Continued)

I/O PORT Port.bit	Name	Function IN/OUT	Alternate Function	Pin
P4.4	WDOUT	O	T/WD output	44
P4.4		I/O	I/O Handshake Port 4	44
P4.5	INT4	I	External interrupt 4	45
P4.5	$\overline{\text{BUSACK}}$	O	External Bus Acknowledge	45
P4.5		I/0	I/O Handshake Port 4	45
P4.6	INT5	I	External interrupt 5	46
P4.6	T0OUTB	O	MF Timer 0 output B	46
P4.6		I/O	I/O Handshake Port 4	46
P4.7	T0OUTA	O	MF Timer 0 output A	47
P4.7	$\overline{\text{BUSREQ}}$	I	External Bus Request	47
P4.7		I/O	I/O Handshake Port 4	47
P5.0		I/O	I/O Handshake Port 5	6
P5.1		I/O	I/O Handshake Port 5	5
P5.2		I/O	I/O Handshake Port 5	4
P5.3		I/O	I/O Handshake Port 5	3
P5.3	P/$\overline{\text{D}}$	O	Program/data space select	3
P5.4	T1OUTA	O	MF Timer 1 output A	2
P5.4		I/0	I/O Handshake Port 5	2
P5.5	T1OUTB	O	MF Timer 1 output B	1
P5.5		I/O	I/O Handshake Port 5	1
P5.6	T3OUTA	O	MF Timer 3 output A	84
P5.6		I/0	I/O Handshake Port 5	84
P5.7	T3OUTB	O	MF Timer 3 output B	83
P5.7		I/O	I/O Handshake Port 5	83
P6.0	A0	O	Address bit 0 (non mux)	19
P6.1	A1	O	Address bit 1 (non mux)	20
P6.2	A2	O	Address bit 2 (non mux)	21
P6.3	A3	O	Address bit 3 (non mux)	22
P6.4	A4	O	Address bit 4 (non mux)	23

PIN DESCRIPTION (Continued)

Table 1. ST90E54,T54 I/O Port Alternate Function Summary (Continued)

I/O PORT Port.bit	Name	Function IN/OUT	Alternate Function	Pin
P6.5	A5	O	Address bit 5 (non mux)	24
P6.6	A6	O	Address bit 6 (non mux)	25
P6.7	A7	O	Address bit 7 (non mux)	26
P7.0	AIN0	I	A/D Analog input 0	64
P7.0	ADTRG	I	A/D conversion trigger	64
P7.0	WRRDY4	I	Handshake Write Ready P4	64
P7.0	RX0CKIN	I	SCI0 Receive Clock input	64
P7.0	WDIN	I	T/WD input	64
P7.0	BSH_EN1	I	Bank Switch High Nibble Enable	64
P7.1	AIN1	I	A/D Analog input 1	65
P7.1	RDRDY4	O	Handshake Read Ready P4	65
P7.1	SDI	I	SPI Serial Data In	65
P7.1	T0INB	I	MF Timer 0 input B	65
P7.2	AIN2	I	A/D Analog input 2	66
P7.2	CLK0OUT	O	SCI0 Byte Sync Clock output	66
P7.2	TX0CKIN	I	SCI0 Transmit Clock input	66
P7.2	BSL_EN1	I	Bank Switch Low Nibble Enable	66
P7.3	AIN3	I	A/D Analog input 3	67
P7.3	$P/\overline{D}$	O	Program/data space select	67
P7.3	T0INA	I	MF Timer 0 input A	67
P7.4	AIN4	I	A/D Analog input 4	68
P7.5	AIN5	I	A/D Analog input 5	69
P7.6	AIN6	I	A/D Analog input 6	70
P7.7	AIN7	I	A/D Analog input 7	71
P8.0	WRRDY5	I	Handshake Write Ready P5	61
P8.0	T3INA	I	MF Timer 3 input A	61
P8.1	RDRDY5	O	Handshake Read Ready P5	60
P8.1	T1INB	I	MF Timer 1 input B	60
P8.2	INT1	I	External interrupt 1	79

PIN DESCRIPTION (Continued)

Table 1. ST9054 I/O Port Alternate Function Summary (Continued)

I/O PORT Port.bit	Name	Function IN/OUT	Alternate Function	Pin
P8.2	T1OUTA	O	MF Timer 1 output A	79
P8.2	$\overline{\text{WRSTB5}}$	O	Handshake Write Strobe P5	79
P8.3	INT3	I	External interrupt 3	78
P8.3	T1OUTB	O	MF Timer 1 output B	78
P8.3	$\overline{\text{RDSTB5}}$	I	Handshake Read Strobe P5	78
P8.4	T1INA	I	MF Timer 1 input A	77
P8.4	$\overline{\text{WAIT}}$	I	External Wait input	77
P8.4	WDOUT	O	T/WD output	77
P8.5	P/D	O	Program/data space select	76
P8.5	T3INB	I	MF Timer 3 input B	76
P8.6	INT7	I	External interrupt 7	75
P8.6	T3OUTA	O	MF Timer 3 output A	75
P8.7	NMI	I	Non-Maskable Interrupt	74
P8.7	T3OUTB	O	MF Timer 3 output B	74
P9.0	S1OUT	O	SCI1 Serial Output	56
P9.1	T0OUTB	O	MF Timer 0 output B	57
P9.1	S1IN	I	SCI1 Serial Input	57
P9.2	CLK1OUT	O	SCI1 Byte Sync Clock output	58
P9.2	TX1CKIN	I	SCI1 Transmit Clock input	58
P9.3	RX1CKIN	I	SCI1 Receive Clock input	59
P9.3	T0OUTA	O	MF Timer 0 output A	59
P9.4	S0OUT	O	SCI0 Serial Output	60
P9.5	S0IN	I	SCI0 Serial Input	61
P9.5	$\overline{\text{BUSACK}}$	O	External Bus Acknowledge	61
P9.6	INT2	I	External interrupt 2	62
P9.6	SCK	O	SPI Serial Clock	62
P9.6	WRSTB4	O	Handshake Write Strobe P4	62
P9.7	INT6	I	External interrupt 6	63
P9.7	SDO	O	SPI Serial Data Out	63

ST90E54 CORE

The Core or Central Processing Unit (CPU) of the ST90E54 includes the 8 bit Arithmetic Logic Unit and the 16 bit Program Counter, System and User Stack Pointers. The microcoded Instruction Set is highly optimised for both byte (8 bit) and word (16 bit) data, BCD and Boolean data types, with 14 addressing modes. Two 8 bit I/O ports are connected to the Core module for external memory interfacing, while a 16 bit Timer/Watchdog gives system security and timing functions, and a Serial Peripheral Interface allows for synchronous communication. Three independent buses are controlled by the Core, a 16 bit Memory bus, an 8 bit Register addressing bus and a 6 bit Interrupt/DMA bus connected to the interrupt and DMA controllers in the on-chip peripherals and the Core. This multiple bus architecture allows a high degree of pipelining and parallel operation within the ST90E54, giving it its efficiency in both numerical calculations and communication with the on-chip peripherals.

MEMORY

The memory of the ST90E54 is functionally divided into two areas, the Register File and Memory. The Memory may optionally be divided into two spaces, each having a maximum of 65,536 bytes. The Memory may be expanded with the Bankswitch logic to give paging of the top 32K bytes of each space to expand the ST90E54 addressing capability to 8M bytes in each space. The two memory spaces are separated by function, one space for Program code, the other for Data. The ST90E54 32K bytes of on-chip EPROM memory is selected at memory addresses 0 through 7FFFh (hexadecimal) in the PROGRAM space, while the ST90T54 OTP version has the top 64 bytes of the program space reserved by SGS-THOMSON for testing purposes. The Data space includes the 1,280 bytes of on-chip RAM at addresses 0 through 04FFh.

Off-chip memory, addressed using the address and data buses (Port 0, Port 1 and Port 6), may be divided into the Program and Data spaces by the external decoding of the Program/Data select pin (P/$\overline{D}$) available as an Alternate function. At addresses greater than the first 32K of program space, the ST90E54 executes external memory cycles for instruction fetches. The Data Strobe $\overline{DS}$ will not be generated when accessing the internal memory. The on-chip general purpose Registers may be used as additional RAM memory for minimum chip count systems.

EPROM PROGRAMMING

The 32,768 of EPROM memory of the ST90E54 (32,704 for the ST90T54) may be programmed by using the EPROM Programming Boards (EPB) available from SGS-THOMSON.

FIGURE 3. Memory Spaces, Bankswitch Disable

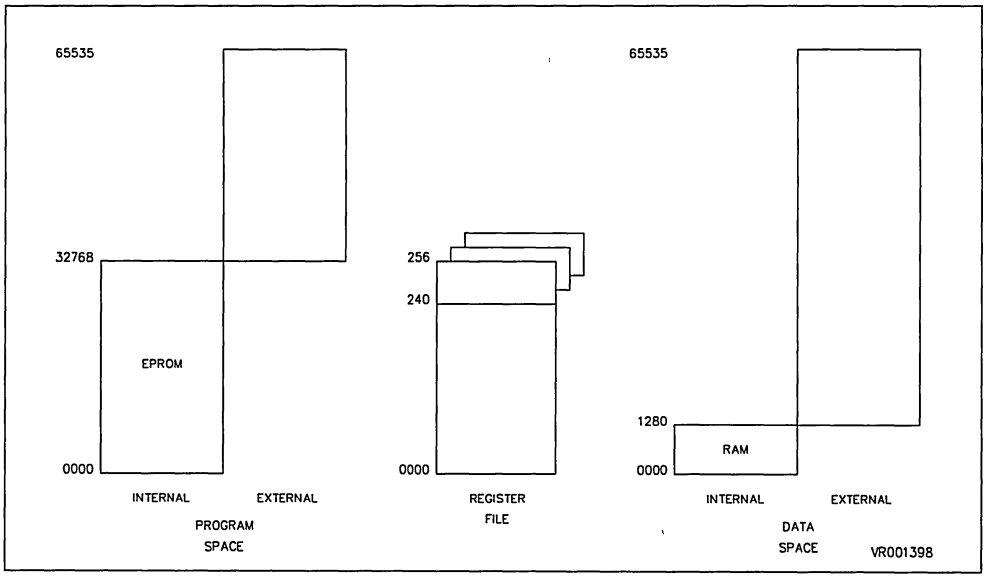
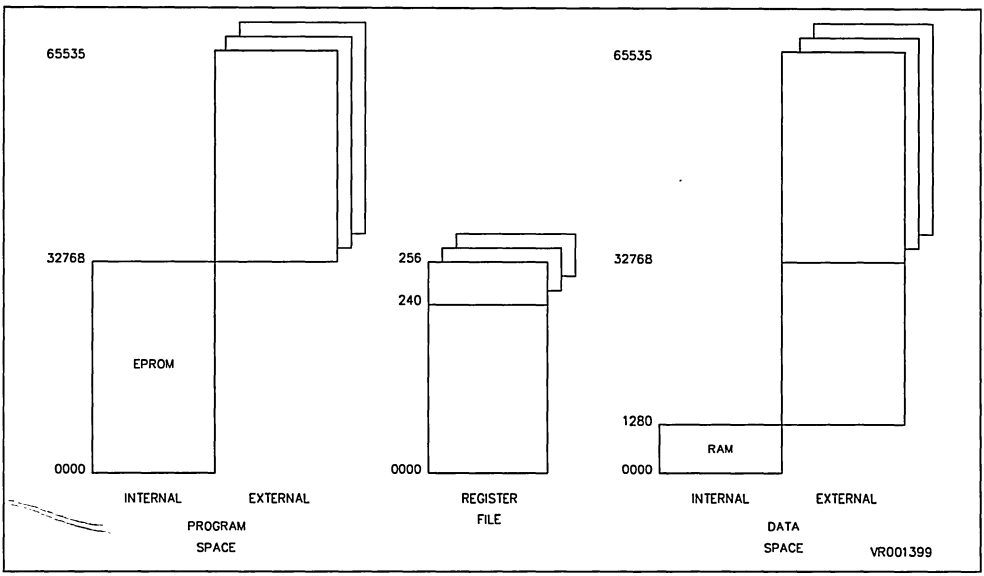


Figure 4. Memory Spaces, Bankswitch Enabled



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	– 0.3 to 7.0	V
AV_{DD}, AV_{SS}	Analog Supply Voltage	$V_{SS} \le AV_{SS} < AV_{DD} \le V_{DD}$	V
V_I	Input Voltage	V_{SS} – 0.3 to V_{DD} +0.3	V
V_O	Output Voltage	V_{SS} – 0.3 to V_{DD} +0.3	V
V_{PP}	Input Voltage on V_{PP} Pin	– 0.3 to 13.5	V
T_{STG}	Storage Temperature	– 55 to + 150	°C

Note: Stresses above those listed as "absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value		Unit
		Min.	Max.	
T_A	Operating Temperature	– 40	85	°C
V_{DD}	Operating Supply Voltage	4.5	5.5	V
f_{OSCE}	External Oscillator Frequency		24	MHz
f_{OSCI}	Internal Oscillator Frequency		12	MHz

DC ELECTRICAL CHARACTERISTICS

(V_{DD} = 5V ± 10% T_A = – 40 °C to + 85°C, unless otherwise specified)

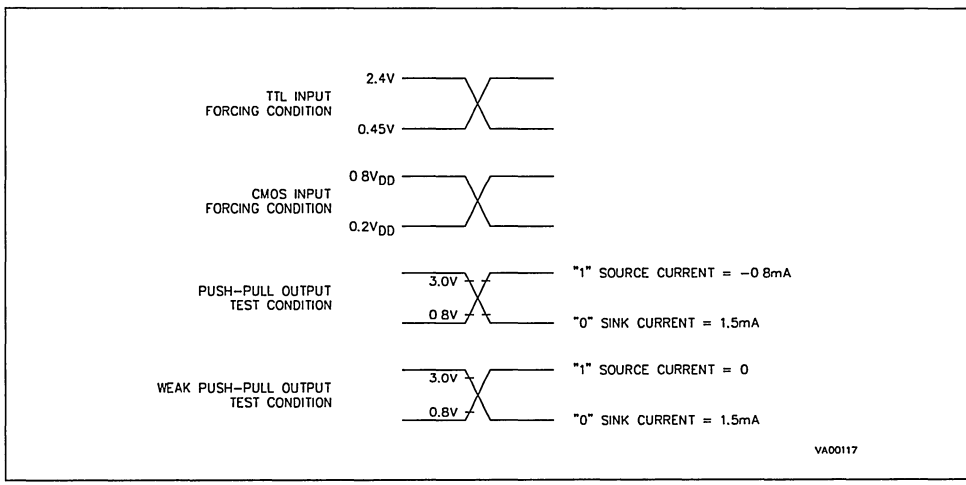
Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
V_{IHCK}	Clock Input High Level	External Clock	0.7 V_{DD}		V_{DD} + 0.3	V
V_{ILCK}	Clock Input Low Level	External Clock	– 0.3		0.3 V_{DD}	V
V_{IH}	Input High Level	TTL	2.0		V_{DD} + 0.3	V
		CMOS	0.7 V_{DD}		VDD + 0.3	V
V_{IL}	Input Low Level	TTL	– 0.3		0.8	V
		CMOS	– 0.3		0.3 V_{DD}	V
V_{IHRS}	Reset Input High Level		0.7 V_{DD}		V_{DD} + 0.3	V
V_{ILRS}	Reset Input Low Level		–0.3		0.3 V_{DD}	V
V_{HYRS}	Reset Input Hysteresis		0.3		1.5	V
V_{OH}	Output High Level	Push Pull, Iload = – 0.8mA	V_{DD} – 0.8			V
V_{OL}	Output Low Level	Push Pull or Open Drain, Iload = – 1.6mA			0.4	V
I_{WPU}	Weak Pull-up Current	Bidirectional Weak Pull-up, V_{OL} = 0V	– 80	– 200	– 420	µA

DC ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
I_{APU}	Active Pull-up Current, for INT0 and INT7 only	$V_{IN} < 0.8V$	– 80	– 200	– 420	µA
I_{LKIO}	I/O Pin Input Leakage	Input/Tri-State, $0V < V_{IN} < V_{DD}$	– 10		+ 10	µA
I_{LKRS}	Reset Pin Input Leakage	$0V < V_{IN} < V_{DD}$	– 30		+ 30	µA
I_{LKAD}	A/D Pin Input Leakage	Alternate Function, Open Drain, $0V < V_{IN} < V_{DD}$	– 3		+ 3	µA
I_{LKAP}	Active Pull-up Input Leakage	$0V < V_{IN} < 0.8V$	– 10		+ 10	µA
I_{LKOS}	OSCIN Pin Input Leakage	$0V < V_{IN} < V_{DD}$	– 10		+ 10	µA
I_{DD}	Run Mode Current	24MHz, Note 1		32	70	mA
		4MHz, Note 1		6	12	mA
I_{DP2}	Run Mode Current Prescale by 2	24MHz, Note 1		19	40	mA
		4MHz, Note 1		4	8	mA
I_{WFI}	WFI Mode Current	24MHz, Note 1		9	18	mA
		4MHz, Note 1		2.5	5	mA
I_{HALT}	HALT Mode Current	24MHz, Note 1			100	µA
V_{PP}	EPROM Programming Voltage		12.2	12.5	12.8	V
I_{PP}	EPROM Programming Current				30	mA

Note: 1. All I/O Ports are configured in Bidirectional Weak Pull-up Mode with no DC load, External Clock pin (OSCIN) is driven by square wave external clock. No peripheral working. External interface not active (Internal Program Execution).

DC TEST CONDITIONS



AC ELECTRICAL CHARACTERISTICS

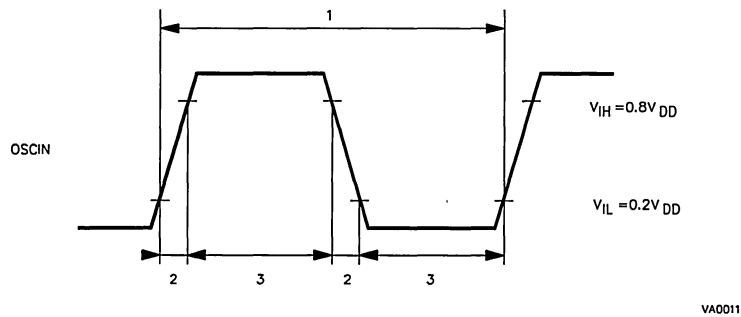
CLOCK TIMING TABLE

(V_{DD} = 5V ± 10%, T_A = − 40°C to + 85°C, unless otherwise specified)

N°	Symbol	Parameter	Value		Unit	Note
			Min.	Max.		
1	TpC	OSCIN Clock Period	41.5		ns	a
			83		ns	b
2	TrC, TfC	OSCIN Rise and Fall Time		12	ns	
3	TwCL, TwCH	OSCIN Low and High Width	25	12	ns	a
			38		ns	b

Notes:
a. Clock divided by 2 internally (MODER.DIV2=1)
b. Clock not divided by 2 internally (MODER.DIV2=0)

CLOCK TIMING



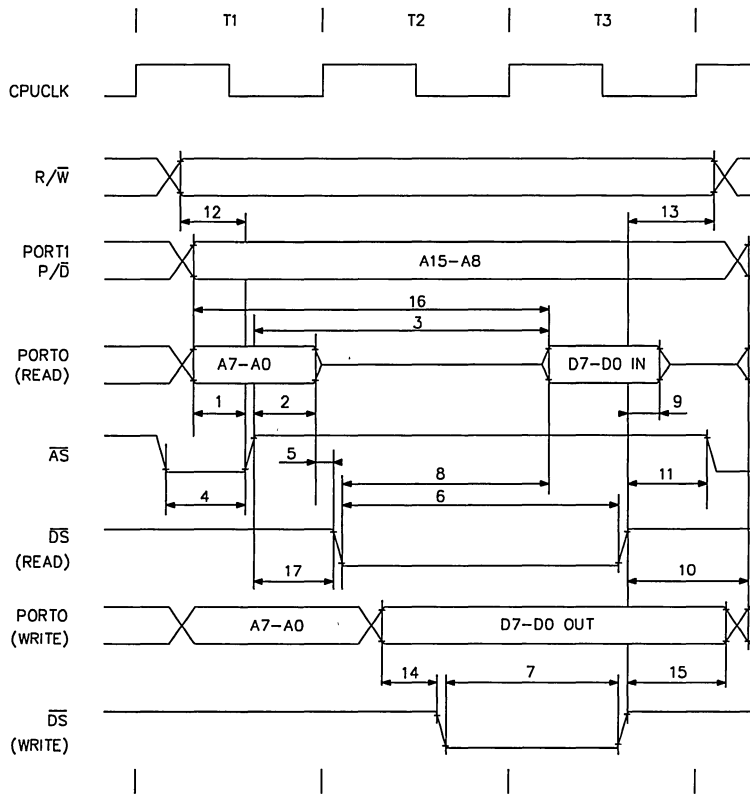
EXTERNAL BUS TIMING TABLE (V_{DD} = 5V ± 10%, T_A = – 40 °C to + 85 °C, Cload = 50pF, CPUCLK = 12MHz, unless otherwise specified)

N°	Symbol	Parameter	Value (Note)				Unit
			OSCIN Divided By 2	OSCIN Not Divided By 2	Min.	Max.	
1	TsA (AS)	Address Set-up Time before $\overline{AS}$ ↑	TpC (2P+1) –22	TwCH+PTpC –18	20		ns
2	ThAS (A)	Address Hold Time after $\overline{AS}$ ↑	TpC –17	TwCL –13	25		ns
3	TdAS (DR)	$\overline{AS}$ ↑ to Data Available (read)	TpC (4P+2W+4) –52	TpC (2P+W+2) –51		115	ns
4	TwAS	$\overline{AS}$ Low Pulse Width	TpC (2P+1) –7	TwCH+PTpC –3	35		ns
5	TdAz (DS)	Address Float to $\overline{DS}$ ↓	0	0	0		ns
6	TwDSR	$\overline{DS}$ Low Pulse Width (read)	TpC (4P+2W+3) –20	TwCH+TpC (2P+W+1) – 16	105		ns
7	TwDSW	$\overline{DS}$ Low Pulse Width (write)	TpC (2P+2W+2) –13	TpC (P+W+1) –13	70		ns
8	TdDSR (DR)	$\overline{DS}$ ↓ to Data Valid Delay (read)	TpC (4P+2W-3) –50	TwCH+TpC(2P+W+1) – 46		75	ns
9	ThDR (DS)	Data to $\overline{DS}$ ↑ Hold Time (read)	0	0	0		ns
10	TdDS (A)	$\overline{DS}$ ↑ to Address Active Delay	TpC –7	TwCL –3	35		ns
11	TdDS (AS)	$\overline{DS}$ ↑ to $\overline{AS}$ ↓ Delay	TpC –18	TwCL –14	24		ns
12	TsR/W (AS)	R/$\overline{W}$ Set-up Time before $\overline{AS}$ ↑	TpC (2P+1) –22	TwCH+PTpC –18	20		ns
13	TdDSR (R/W)	$\overline{DS}$ ↑ to R/$\overline{W}$ and Address Not Valid Delay	TpC –9	TwCL –5	33		ns
14	TdDW (DSW)	Write Data Valid to $\overline{DS}$ ↓ Delay (write)	TpC (2P+1) –32	TwCH+PTpC –28	10		ns
15	ThDS (DW)	Data Hold Time after DS ↑ (write)	TpC –9	TwCL –5	33		ns
16	TdA (DR)	Address Valid to Data Valid Delay (read)	TpC (6P+2W+5) –68	TwCH+TpC (3P+W+2) – 64		140	ns
17	TdAs (DS)	$\overline{AS}$ ↑ to $\overline{DS}$ ↓ Delay	TpC –18	TwCL –14	24		ns

Note: The value left hand two columns show the formula used to calculate the timing minimum or maximum from the oscillator clock period, prescale value and number of wait cycles inserted.
The value right hand two columns show the timing minimum and maximum for an external clock at 24 MHz divided by 2, prescaler value of zero and zero wait status.

Legend:
P = Clock Prescaling Value
W = Wait Cycles
TpC = OSCIN Period
TwCH = High Level OSCIN half period
TwCL = Low Level OSCIN half period

EXTERNAL BUS TIMING

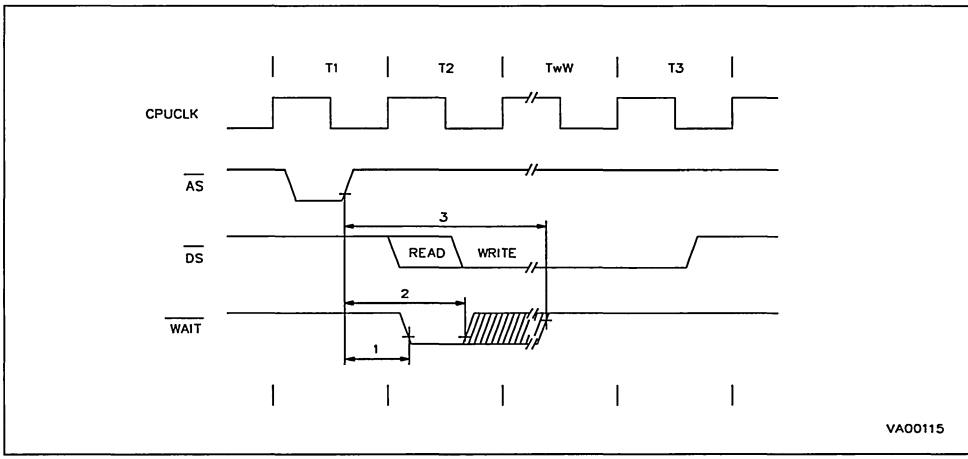


EXTERNAL WAIT TIMING TABLE (V_{DD} = 5V ± 10%, T_A = –40°C to +85°C, Cload = 50pF, INTCLK = 12MHz, Push-pull output configuration, unless otherwise specified)

N°	Symbol	Parameter	Value (Note)				Unit
			OSCIN Divided By 2	OSCIN Not Divided By 2	Min.	Max.	
1	TdAS (WAIT)	$\overline{AS}$ ↑ to $\overline{WAIT}$ ↓ Delay	2(P+1)TpC –29	(P+1)TpC –29		40	ns
2	TdAS (WAIT)	$\overline{AS}$ ↑ to $\overline{WAIT}$ ↑ Minimum Delay	2(P+W+1)TpC –4	(P+W+1)TpC –4	80		ns
3	TdAS (WAIT)	$\overline{AS}$ ↑ to $\overline{WAIT}$ ↑ Maximum Delay	2(P+W+1)TpC –29	(P+W+1)TpC –29		83W+40	ns

Note: The value left hand two columns show the formula used to calculate the timing minimum or maximum from the oscillator clock period, prescale value and number of wait cycles inserted.
The value right hand two columns show the timing minimum and maximum for an external clock at 24 MHz divided by 2, prescale value of zero and zero wait status.

EXTERNAL WAIT TIMING

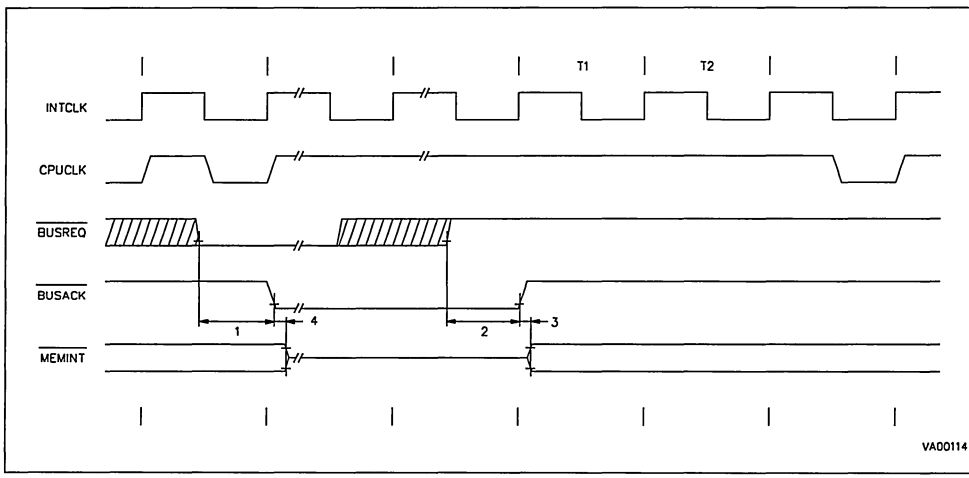


BUS REQUEST/ACKNOWLEDGE TIMING TABLE (V_{DD} = 5V ± 10%, T_A = −40°C to +85°C, Cload = 50pF, INTCLK = 12MHz, Push-pull output configuration, unless otherwise specified)

N°	Symbol	Parameter	Value (Note)				Unit
			OSCIN Divided By 2	OSCIN Not Divided By 2	Min.	Max.	
1	TdBR (BACK)	$\overline{BREQ}$ ↓ to $\overline{BUSACK}$ ↓	TpC+8	TwCL+12	50		ns
			TpC(6P+2W+7)+65	TpC(3P+W+3)+TwCL+65		360	ns
2	TdBR (BACK)	$\overline{BREQ}$ ↑ to $\overline{BUSACK}$ ↑	3TpC+60	TpC+TwCL+60		185	ns
3	TdBACK (BREL)	$\overline{BUSACK}$ ↓ to Bus Release	20	20		20	ns
4	TdBACK (BACT)	$\overline{BUSACK}$ ↑ to Bus Active	20	20		20	ns

Note: The value left hand two columns show the formula used to calculate the timing minimum or maximum from the oscillator clock period, prescale value and number of wait cycles inserted.
The value right hand two columns show the timing minimum and maximum for an external clock at 24 MHz divided by 2, prescale value of zero and zero wait status.

BUS REQUEST/ACKNOWLEDGE TIMING



Note : MEMINT = group of memory interface signals : $\overline{AS}$, $\overline{DS}$, R/$\overline{W}$, P00-P07, P10-P17.

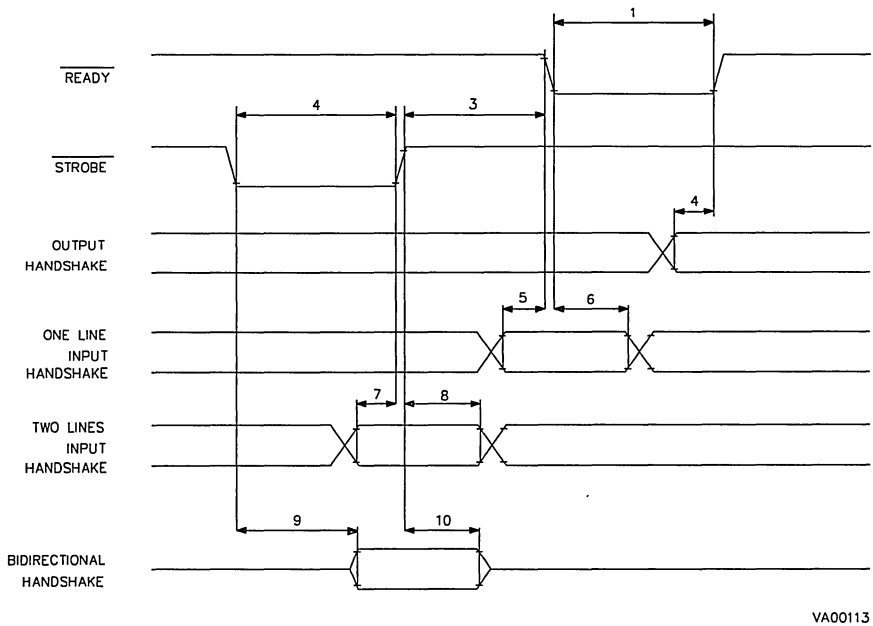
HANDSHAKE TIMING TABLE (V_{DD} = 5V ± 10%, T_A = –40°C to +85°C, Cload = 50pF, INTCLK = 12MHz, Push-pull output configuration, unless otherwise specified)

N°	Symbol	Parameter	Value (Note)				Min.	Max.	Unit
			OSCIN Divided By 2		OSCIN Not Divided By 2				
			Min.	Max.	Min.	Max.			
1	TwRDY	RDRDY, WRRDY Pulse Width in One Line Handshake	2TpC (P+W+1) –18		TpC (P+W+1) –18		65		ns
2	TwSTB	$\overline{RDSTB}$, $\overline{WRSTB}$ Pulse Width	2TpC+12		TpC+12		95		ns
3	TdST (RDY)	$\overline{RDSTB}$, or $\overline{WRSTB}$ ↑ to RDRDY or WRRDY ↓		TpC+45		(TpC-TwCL) +45		87	ns
4	TsPD (RDY)	Port Data to RDRDY ↑ Set-up Time	(2P+2W+1) TpC –25		TwCH+(W+P) TpC –25		16		ns
5	TsPD (RDY)	Port Data to WRRDY ↓ Set-up Time in One Line Handshake	43		43		43		ns
6	ThPD (RDY)	Port Data to WRRDY ↓ Hold Time in One Line Handshake	0		0		0		ns
7	TsPD (STB)	Port Data to $\overline{WRSTB}$ ↑ Set-up Time	10		10		10		ns
8	ThPD (STB)	Port Data to WRSTB ↑ Hold Time	25		25		25		ns
9	TdSTB (PD)	$\overline{RDSTBD}$ ↑ to Port Data Delay Time in Bidirectional Handshake		35		35		35	ns
10	TdSTB (PHZ)	$\overline{RDSTB}$ ↑ to Port High-Z Delay Time in Bidirectional Handshake		25		25		25	ns

Note: The value left hand two columns show the formula used to calculate the timing minimum or maximum from the oscillator clock period, prescale value and number of wait cycles inserted.
The value right hand two columns show the timing minimum and maximum for an external clock at 24 MHz divided by 2, prescaler value of zero and zero wait status.

Legend:
P = Clock Prescaling Value (R235.4,3,2)
W = Programmable Wait Cycles (R252.2.1.0/5,4,3) + External Wait Cycles

HANDSHAKE TIMING

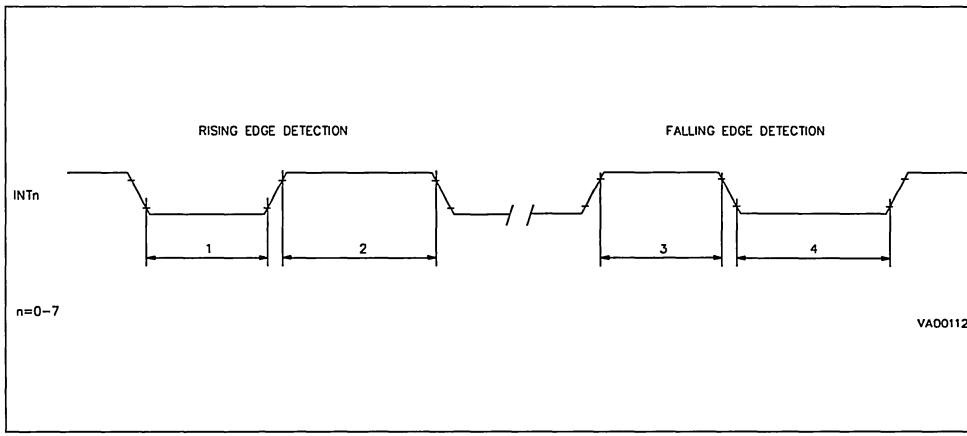


EXTERNAL INTERRUPT TIMING TABLE (V_{DD} = 5V ± 10%, T_A = –40°C to +85°C, Cload = 50pF, INTCLK = 12MHz, Push-pull output configuration, unless otherwise specified)

N°	Symbol	Parameter	Value (Note)				Unit
			OSCIN Divided By 2 Min.	OSCIN Not Divided By 2 Min.	Min.	Max.	
1	TwLR	Low Level Minimum Pulse Width in Rising Edge Mode	2TpC+12	TpC+12	95		ns
2	TwHR	High Level Minimum Pulse Width in Rising Edge Mode	2TpC+12	TpC+12	95		ns
3	TwHF	High Level Minimum Pulse Width in Falling Edge Mode	2TpC+12	TpC+12	95		ns
4	TwLF	Low Level Minimum Pulse Width in Falling Edge Mode	2TpC+12	TpC+12	95		ns

Note: The value left hand two columns show the formula used to calculate the timing minimum or maximum from the oscillator clock period, prescale value and number of wait cycles inserted.
The value right hand two columns show the timing minimum and maximum for an external clock at 24 MHz divided by 2, prescale value of zero and zero wait status.

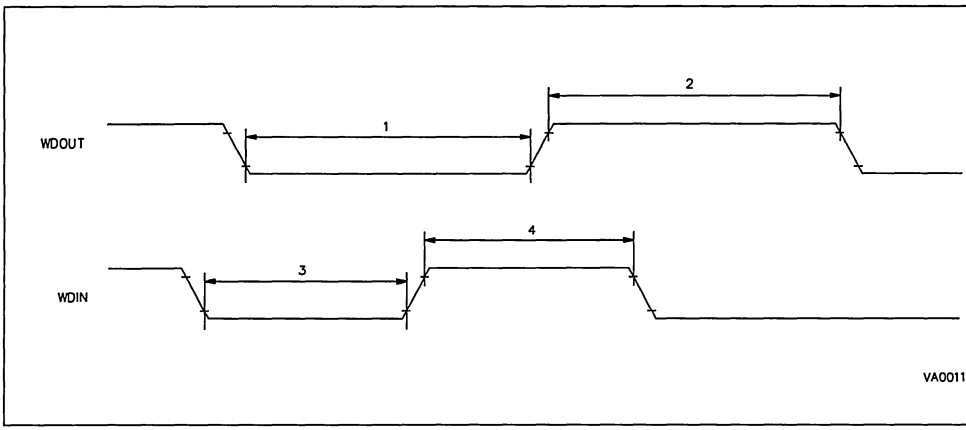
EXTERNAL INTERRUPT TIMING



WATCHDOG TIMING TABLE (V_{DD} = 5V ± 10%, T_A = –40°C to +85°C, Cload = 50pF, INTCLK = 12MHz, Output Alternate Function set as Push-pull)

N°	Symbol	Parameter	Value		Unit
			Min.	Max.	
1	TwWDOL	WDOUT Low Pulse Width	620		ns
2	TwWDOH	WDOUT High Pulse Width	620		ns
3	TwWDIL	WDIN Low Pulse Width	350		ns
4	TwWDIH	WDIN High Pulse Width	350		ns

WATCHDOG TIMING

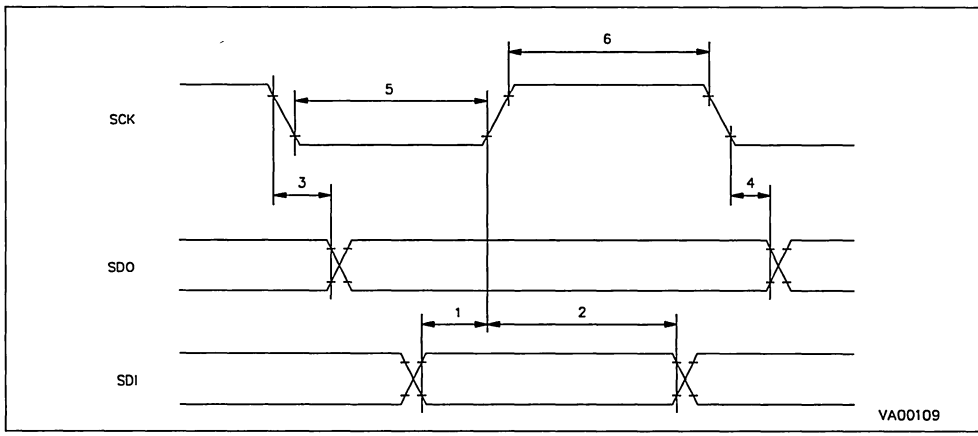


SPI TIMING TABLE (V_{DD} = 5V ± 10%, T_A = –40°C to +85°C, Cload = 50pF, INTCLK = 12MHz, Output Alternate Function set as Push-pull)

N°	Symbol	Parameter	Value		Unit
			Min.	Max.	
1	TsDI	Input Data Set-up Time	100		ns
2	ThDI (1)	Input Data Hold Time	1/2 TpC+100		ns
3	TdOV	SCK to Output Data Valid		100	ns
4	ThDO	Output Data Hold Time	-20		ns
5	TwSKL	SCK Low Pulse Width	300		ns
6	TwSKH	SCK High Pulse Width	300		ns

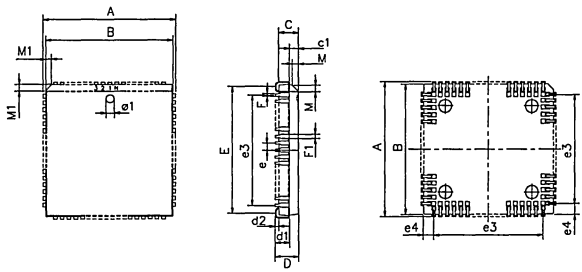
Note: 1. TpC is the Clock period.

SPI TIMING



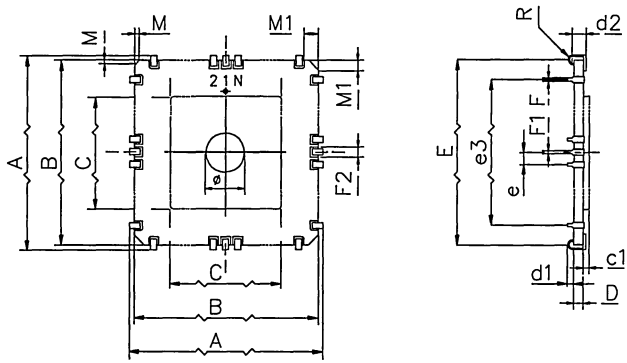
PACKAGES MECHANICAL DATA

Figure 5. 84-Lead Plastic Leaded Chip Carrier



DIM	MM			INCHES		
	Min	Typ	Max	Min	Typ	Max
A	30.10		30.35	1.18		1.19
B	29.20		29.41	1.14		1.15
C						
C1						
D	4.20		5.08	0.16		0.19
D1		2.54			0.02	
D2		0.56				
D3				1.09		1.12
E	27.69		28.70		0.04	
e		1.27				
e3					0.01	
F		0.38				
F1						0.003
G			0.101			
H		1.27			0.04	
H1		1.14			0.04	

Figure 6. 84-Lead Window Ceramic Leaded Chip Carrier (L)



DIM	MM			INCHES		
	Min	Typ	Max	Min	Typ	Max
A	29.37		30.48	1.15		1.19
B	28.83		29.59	1.13		1.16
C			18.92			0.74
C1			0.30			0.01
D	1.37		1.68	0.05		0.06
d1						
d2		2.23			0.08	
E	28.19		29.21	1.10		1.14
e		1.27			0.04	
e3	25.15		25.65	0.91		1
F		0.45			0.01	
F1		0.63			0.02	
F2						
M						
M1						
R		0.76			0.02	

ORDERING INFORMATION

Sales Type	Frequency	Temperature Range	Package
ST90E54L6	24MHz	– 40°C to + 85°C	CLCC84-W
ST90E54L1	24MHz	0°C to + 70°C	CLCC84-W
ST90T54C6	24MHz	– 40°C to + 85°C	PLCC84
ST90T54C1	24MHz	0°C to + 70°C	PLCC84

DEVELOPMENT TOOLS

SGS-THOMSON MICROELECTRONICS

ST9-EVM

EVALUATION MODULE FOR ST9 MCU FAMILY

- Designed to communicate with any IBM PC/XT/AT or compatible computer through an RS-232 serial communication link.
- Software Development and Debugging Package running under MS-DOS operating system (EVMST9)
- Emulation of the ST9 Microcontroller family.
- 128K bytes of fast static memory.
- RS-232 serial interface for connection with a host computer or console terminal.
- Programmable crystal oscillator to control baud rate of the serial I/O channels.
- Two Counter/Timer and Parallel I/O Units completely free for operation by the user.
- Single step circuitry.
- Automatic hardware self test executed every time the emulator is powered on.
- Requires the use of an external 5V power supply
- Three Configuration Modes: The evaluation module may be configured in stand alone mode, remote tty mode, or remote Host mode. Remote host mode allows the use of a more powerful debugger program.

GENERAL DESCRIPTION

The ST9-EVM interfaces with any user-designed ST9 system and assists in the debugging and development of that system. The complete ST9-EVM consists of the evaluation module, an RS232 Serial Communication cable providing the interface with an optional Host computer, an ICE Probe and Adapter which may be plugged directly into the user's application, and a powerful software debugger. The evaluation module requires an external 5V power supply to function.

The ST9-EVM allows the designer to emulate the system in real time or single step mode. A set of 128 user programmable software breakpoints may be used to stop execution upon access to any program memory address.

Furthermore, a wide range of debug commands are available when operating in remote Host mode and provide the user with full control of the Evaluation Board hardware and feature several commands for controlling the execution of programs. Memory and

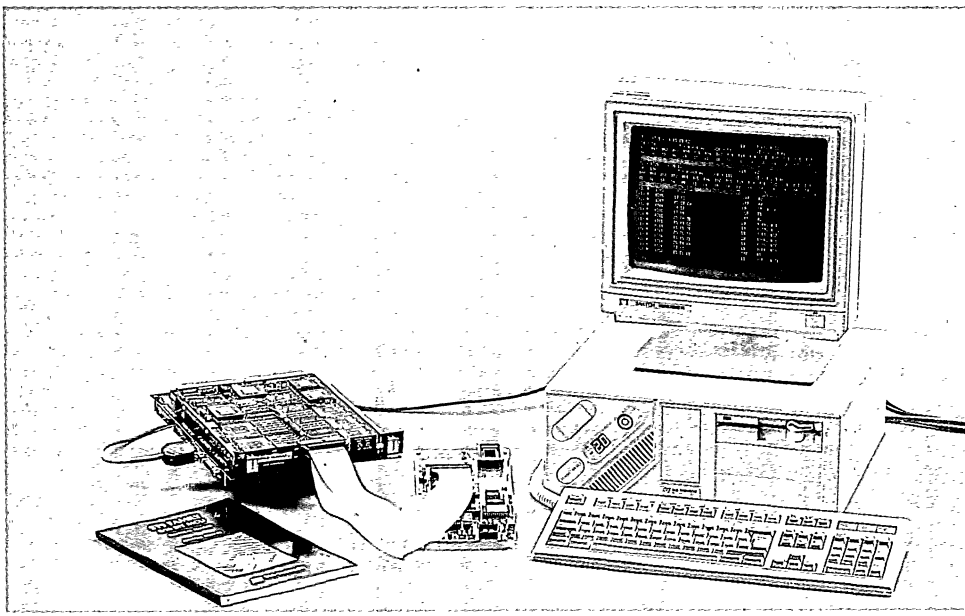
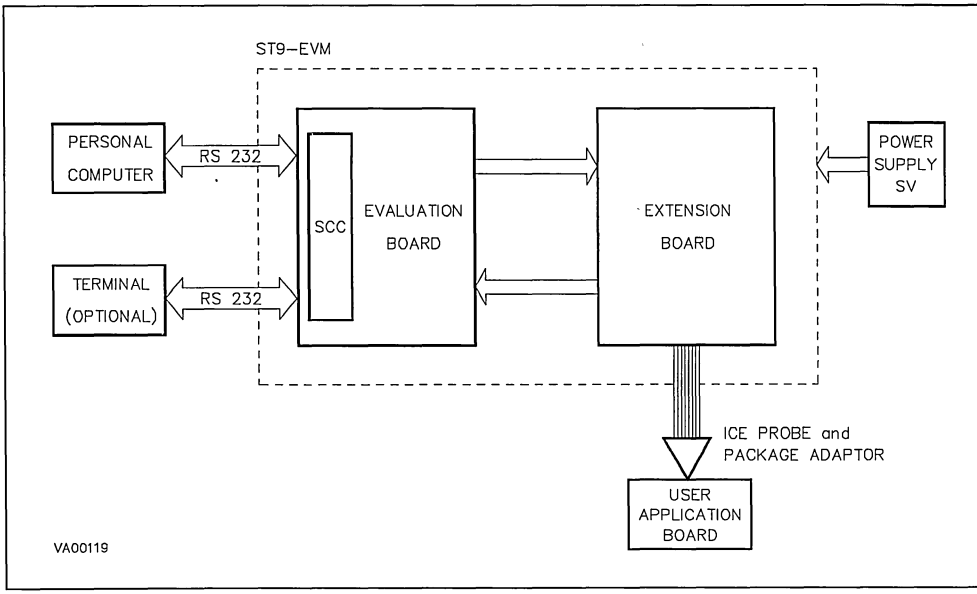


Figure 1. ST9-EVM Hardware Configuration



registers may be read and written in a number of different formats, while macro commands and conditional block constructs are available for use in automated debugging sessions.

HARDWARE DESCRIPTION

Evaluation Module Hardware Includes: The Evaluation Board which provides the extra circuitry needed by the emulated CPU in order to control the single step logic and the serial and parallel interfaces, as well as the memory necessary for use by both the system and the user.

The ST90xx Extension Board which contains the emulated ST9 (Core, I/O Ports, and Peripherals). The Extension Board is different for each ST9 version.

The Evaluation Module shares the emulated ST9 microcontroller with the user. Consequently, the Extension Board manages the operation of the Evaluation Module by means of the emulated ST9, while the Evaluation Board provides any of the necessary external circuitry including 128K of memory and single step circuitry.

The Evaluation Board contains 128K of memory, out of this, 32K of Program Memory and 56K of Data Memory are available to the user. The first 32K of Program Memory and the last 8K of Data Memory are reserved for system use. The Evaluation Board also contains special circuitry to allow the user to execute a program in single step mode.

The Serial I/O Units, which control communication with either a host computer or a console terminal, are located on the Evaluation Board and have their own crystal oscillator which may be programmed by adjusting a set of jumpers on the Evaluation Board. The Evaluation Board also provides two Counter/Timer and Parallel I/O Units which are completely free for operation by the user. Each unit has two 8 bit and one 4 bit parallel I/O ports and three 16 bit counter/timers.

The Extension Board contains the circuitry which emulates the ST9, along with all the special functions and peripherals of the specific ST9 being emulated. Since each version of the ST9 has different peripherals and access to different I/O ports, the Extension Board will be different for each version of the ST9.

However, the basic design of the Extension Board will remain the same, allowing the extension board to be easily configured for any future or existing version of the ST9. In general, the Extension Board contains the components and circuitry which emulate the ST9 (Core, I/O ports, and peripherals), interfaces with the ICE Connectors, and sends information to the Evaluation Board.

A 5V Power Supply must be provided by the user in order to use the Evaluation Module.

SOFTWARE DEVELOPMENT AND DEBUGGING PACKAGE

The ST9 Evaluation Module Debugger is a software tool which allows the user to have complete control of the ST9 Evaluation Module. The Debugger must be used on an IBM PC/XT/AT or compatible that is connected to the ST9-EVM by means of an RS-232 serial communication cable. The following features are provided by the ST9 Evaluation Module Debugger:

The debugger available when in Remote Host mode has a command line syntax compatible with the SIMST9 Software Simulator and SDBST9 (the Debugger for the ST9 Hardware Development System). A wide range of commands are available for displaying and setting memory and registers according to different formats. The debugger has a powerful symbol handler which allows the user to define symbols and macros, extract them from symbol table files, and save them in symbol table files.

The debugger provides a symbolic on-line assembler and disassembler. Full screen video modes are available for Memory, Register, and Single Step Display when using the debugger. Macro commands and conditional block constructs are available for use in automated debugging sessions.

An On-line help facility is available in the debugger to give a listing of the complete command set as well as specific information on any of the commands. Log, dump and command file capability allows for easy documentation and configuration when using the debugger.

The debugger contains a powerful command interpreter which allows the evaluation of complex expressions involving numbers, addresses, memory and register contents, and I/O channel data.

128 software breakpoints are available to the user and may be set on any program address accessible by the user.

Figure 2. EVMST9 Command Summary

ARCHIVE	Archive symbols and macros
ASM	On-line assembler
BASE	Change base of numbers
BYE	Exit from debugger program
CLOSE	Close I/O channel
CM	Compare memory
DEFINE	Define symbols and macros
DISASM	On-line symbolic disassembler
DM	Display memory
DO	Execute macro
DR	Display register
DUMP	Save current setup
FM	Fill memory
FR	Fill registers
GO	Execute program
HELP	On-line help
HOST	Enter Transparent Mode
IF	Conditional command execution
LISTSYMBOL	List symbols and macros
LOAD	Load program/data from file
MM	Move block of memory
NEXT	Execute program steps
OPEN	Open I/O channel
PRINT	Print strings and values
PUNCH	Save program/data to control terminal
QUIT	Terminate command execution

Figure 2. EVMST9 Command Summary (continued)

READ	Read program/data from control terminal
RESET	Reset emulated CPU
SAVE	Save program/data into file
SB	Set/display memory breakpoints
SEARCH	Search a pattern in memory
SET	Set/reset options
SM	Set memory
SR	Set/display registers
UNDEFINE	Remove symbols
USE	Execute commands from a file
VE	View execution (video mode)
VM	View memory (video mode)
VR	View registers (video mode)
WR	Display current working register set
<value>	Evaluate expression
?	Display symbols having a given value

ORDERING INFORMATION

Part Number	Description
ST902X-EVM	Evaluation Module for emulation of ST902X subfamily devices
ST903X-EVM	Evaluation Module for emulation of ST903X and ST904X subfamilies devices
ST905X-EVM	Evaluation Module for emulation of ST905X subfamily devices
ST902X-DBE	Extension Board for ST902X devices (upgrade part)
ST903X-DBE	Extension Board for ST903X devices (upgrade part)
ST904X-DBE	Extension Board for ST904X devices (upgrade part)
ST905X-DBE	Extension Board for ST905X devices (upgrade part)

SGS-THOMSON MICROELECTRONICS

ST9-EPB

EPROM PROGRAMMING BOARD FOR ST9 MCU FAMILY

- Programming tool for EPROM and OTP members of the ST9 Microcontroller Family
- Stand-alone operation mode
- Device EPROM capacity self-identified
- 3 functions performed
- All device packages type supported
- Single Power Supply

GENERAL DESCRIPTION

This board is designed for programming the EPROM versions of the ST9 microcontroller family, including both the ceramic windowed and plastic OTP packages.

The EPROM size of the ST9 microcontroller to be programmed is recognised automatically by the on-board software and three sockets are provided to accept the different existing packages types.

The ST9-EPB board uses a reference EPROM including the customer's code directly generated by the ST9 assembler-linker. The ST9 EPROM device will be programmed from the contents of the reference EPROM. Jumpers allow the selection of different types of reference EPROM (2732, 2764, 27128, 27256).

On board regulation requires only a single power supply of +18 V_{DC} – 0.5A to produce the different voltages necessary for the board functioning.

The board can perform 3 operations:

– Verifying the blank state of the microcontroller EPROM.

– Programming microcontroller with the content of the reference EPROM.

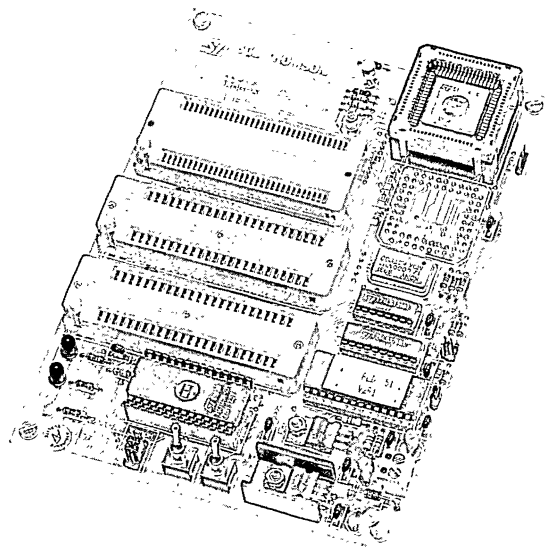
– Verifying the microcontroller against the reference EPROM.

The required function is selected by two switches.

During the running procedure the program/verify LED flashes and at the end of operation, the result is displayed on LEDs:

– Green OK LED for succesful operation.

– Red error LED for a programming error.



ORDERING INFORMATION

Part Number	Target Devices	Type	Packages
ST90E2X-EPB	ST90E26D6	EPROM	CDIP48W
	ST90E27D6	EPROM	CDIP40W
	ST90E28L6	EPROM	CLCC44W
	ST90T26B6	OTP	PDIP48
	ST90T27B6	OTP	PDIP40
	ST90T28C6	OTP	PLCC44
ST90E4X-EPB	ST90E40L6	EPROM	CLCC68W
	ST90E30L6	EPROM	CDIP68W
	ST90E31D6	EPROM	CDIP48W
	ST90T30B6	OTP	PLCC68
	ST90T31B6	OTP	PDIP48
ST90E5X-EPB	ST90E54L6	EPROM	CLCC84W

SGS-THOMSON MICROELECTRONICS

ST9-HDS

HARDWARE DEVELOPMENT SYSTEM FOR ST9 MCU FAMILY

- Designed to communicate with any IBM PC/XT/AT or compatible computer through an RS-232 serial communication link.
- Emulation capability of all present and future members of the ST9 Microcontroller family, ROM and ROMless devices by dedicated option boards
- 128K bytes of system mappable fast static memory, which may be mapped in pages of 512 bytes each
- 4 maskable hardware controlled memory breakpoints and 2 maskable hardware controlled register breakpoints
- Real time trace memory (2048 events)
- Programmable crystal oscillator and external clock option allow an emulated CPU clock frequency ranging from 2 to 24 MHz
- Automatic hardware self test executed every time the emulator is powered on
- 8 User Probes available and included in the trace and breakpoint logic
- The Emulator may be used in Standalone Mode without a Personal Computer control

GENERAL DESCRIPTION

The ST9 Hardware Development System (ST9-HDS) is an intelligent and powerful In Circuit Real Time Emulation System configurable for all current and future members of the ST9 family of microcontrollers. The complete ST9-HDS consists of the emulator, an RS232 Serial Communication Cable providing the interface with an optional Host computer, an ICE Probe and Adapter which may be plugged directly into the user's application, a set of 8 user probes, and a powerful software debugger. The ST9-HDS allows the designer to emulate the system in real time or single step mode. A set of 4 user programmable memory breakpoints which may be logically combined in AND, OR, SEQUENTIAL, or DELAY mode and 2 user programmable register breakpoints allow the user to stop emulation upon very specific conditions, while trace circuitry will collect the latest 2K (by 40 bit) events. Furthermore, a wide range of debug commands provides the user with full control of the Emulator hardware and features several commands for con-

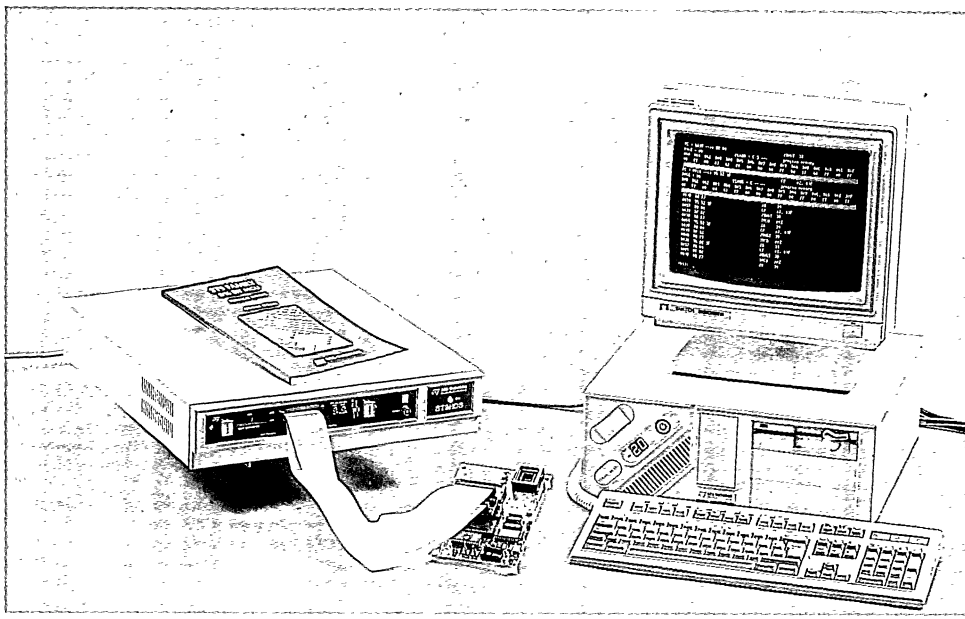
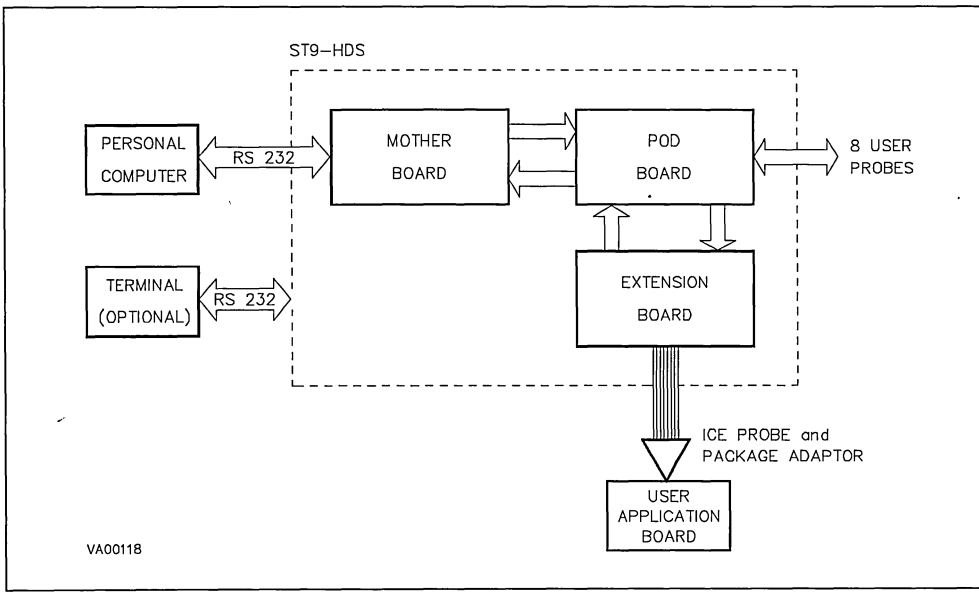


Figure 1. ST9-HDS System Configuration



trolling the execution of programs. Memory and registers may be read and written in a number of different formats, while macro commands and conditional block constructs are available for use in automated debugging sessions.

HARDWARE DESCRIPTION

The Interface and Control Unit (ICU) contains most of the circuitry necessary to control the ST9-HDS, with the exception of the circuits specifically related to the ST9 family of microcontrollers. The ICU provides the control logic for monitoring the execution of programs, setting memory breakpoints, recording signal events, and handling the communication with the host computer. The board contains the following hardware resources:

- Private Microcontroller: A private microcontroller controls the operation of the emulator, allowing execution of an emulated program to run without interference.
- 128K of Fast Static Memory: 128 Kbytes of fast static memory are available for use by the emulated microcontroller.
- Memory Management Circuitry: Memory may be mapped in groups of 512 bytes as Internal/External to the Emulated ST9 or, System/User Supplied, and ReadOnly/ReadWrite, or as Non Existent. (Certain versions also allow memory to be mapped as EEPROM memory.)
- Memory Breakpoints: 4 Hardware controlled memory breakpoints are available to the user and may be combined in AND, OR, SEQUENTIAL, or DELAY mode. Each of the four breakpoints is associated with a breakpoint counter which may be used simply as a counter or used to flag an event only after the associated event has occurred n times.
- Real Time Trace Circuitry: Real Time Trace Circuitry keeps track of a 2K by 40 bit buffer.

The ST9 Emulator POD contains the core of the circuits required to emulate any member of the ST9 family of microcontrollers. This board is responsible for providing the interface with the Extension Board, providing the interface with the Interface Control Unit, sending out signals on reset identifying the emulated device as a ROM-less or ROM-maskable device, managing the opcode fetch signals, generating the clock for the Extension Board, controlling the standalone mode option, decoding the pod addresses, managing the register breakpoints, controlling the idle/run logic, generating wait cycles, and accessing the 8 user probes. The Pod Board contains the following features:

- Programmable Crystal Oscillator: An on board programmable crystal oscillator, as well as the possibility of using an external clock via a BNC connector, allow the user the option of selecting the emulated CPU clock frequency.

HARDWARE DESCRIPTION (continued)

- Standalone Logic: The Hardware Development System may be operated in Standalone Mode, that is independently of the Host computer.
- Wait Cycle Generator: A Wait Cycle Generator allows the user to assign from 0 to 7 wait cycles to any block of 512 memory bytes defined as external.
- Register Breakpoints: 2 Hardware controlled register breakpoints are available to the user and may be combined in AND or OR mode.

The Extension Board contains the circuitry controlling all the special functions and peripherals of the ST9 being emulated. Since each version of the ST9 has different peripherals and access to different I/O ports, the Extension Board will be different for each version of the ST9.

However, the basic design of the Extension Board will remain the same, allowing the extension board to be easily configured for any future or existing version of the ST9. In general, the Extension Board contains the components and circuitry which emulate the ST9 (Core, I/O ports, and peripherals), interfaces with the ICE Connectors, and sends information to the Pod Board.Either a 220V/50Hz or 110V/60Hz Power Supply is included in the emulator to provide the emulator with all necessary power.

SOFTWARE DEBUGGING PACKAGE

The ST9 Symbolic Debugger is a software tool which allows the user to have complete control of the ST9 Hardware Development System. The Debugger must be used on an IBM PC/XT/AT or compatible that is connected to the ST9-HDS by means of an RS-232 serial communication cable. The following features are provided by the ST9 Symbolic Debugger:

- Debugger Compatibility: The debugger has a command line syntax compatible with the SIMST9 Software Simulator and SDBST9, the debugger for the ST9 Evaluation Module.
- Commands: A wide range of commands are available for displaying and setting memory and registers according to different formats.
- Powerful Symbol Handler: A Powerful Symbol Handler allows the user to define symbols and macros, extract them from symbol table files, and save them in symbol table files.
- Symbolic On-Line Assembler/Disassembler: The debugger provides a symbolic on-line assembler and disassembler.
- Full Screen Video Mode: Full screen video modes are available for Memory, Register, and Single Step Display.
- Symbolic Trace: Trace memory is disassembled into assembler mnemonics.
- Macros and Conditional Block Constructs: Macro commands and conditional block constructs are available for use in automated debugging sessions.
- On-Line Help: An On-line help facility is available in the debugger to give a listing of the complete command set as well as specific information on any of the commands.
- Configuration and Documentation: Log, dump and command file capability allows for easy documentation and configuration.
- Powerful Command Interpreter: A powerful command interpreter allows for the evaluation of complex expressions involving numbers, addresses, memory and register contents, and I/O channel data.

The ST9 Symbolic Debugger accepts inputs from the Software Development Package which includes the following:

- ST9 Macro Assembler (AST9)
- ST9 Linker/Loader (LST9)
- ST9 Library Archiver (ARST9)
- ST9 Software Simulator (SIMST9)

The Software Development Package is available separately, or with the Hardware Development System.

Figure 2. SDBST9 Command Summary

ARCHIVE	Archive symbols and macros
ASM	On-line assembler
BASE	Change base of numbers
BYE	Exit from debugger program
CLOSE	Close I/O channel
CM	Compare memory
DEFINE	Define symbols and macros
DISASM	On-line symbolic disassembler
DM	Display memory
DO	Execute macro
DR	Display register
DUMP	Save current setup
FM	Fill memory
FR	Fill registers
GO	Execute program
HELP	On-line help
IF	Conditional command execution
LISTSYMBOL	List symbols and macros
LOAD	Load program/data from file
MAP	Set/display memory mapping
MB	Modify breakpoint
MM	Move block of memory
MRB	Modify register breakpoint
NEXT	Execute program steps
OPEN	Open I/O channel
PRINT	Print strings and values
QUIT	Terminate command execution
RESET	Reset emulated CPU
SAVE	Save program/data into file
SB	Set/display memory breakpoints
SEARCH	Search a pattern in memory
SET	Set/reset options
SM	Set memory
SR	Set/display registers
SRB	Set/display register breakpoints
TRACE	Display trace
UNDEFINE	Remove symbols
USE	Execute commands from a file
VE	View execution (video mode)
VM	View memory (video mode)
VR	View registers (video mode)
WR	Display current working register set
<value>	Evaluate expression
?	Display symbols having a given value

ORDERING INFORMATION

Part Number	Description
ST902X-EMU/220 ST902X-EMU/110	Complete Emulator for ST902X devices with Extension Board, including Software Tools (not C compiler) for MS-DOS operating system
ST903X-EMU/220 ST903X-EMU/110	Complete Emulator for ST903X devices with Extension Board, including Software Tools (not C compiler) for MS-DOS operating system
ST904X-EMU/220 ST904X-EMU/110	Complete Emulator for ST904X devices with Extension Board, including Software Tools (not C compiler) for MS-DOS operating system
ST905X-EMU/220 ST905X-EMU/110	Complete Emulator for ST905X devices with Extension Board, including Software Tools (not C compiler) for MS-DOS operating system
ST902X-HDS/220 ST902X-HDS/110	Hardware Development System for ST902X devices with Debugger only
ST903X-HDS/220 ST903X-HDS/110	Hardware Development System for ST903X devices with Debugger only
ST904X-HDS/220 ST904X-HDS/110	Hardware Development System for ST904X devices with Debugger only
ST905X-HDS/220 ST905X-HDS/110	Hardware Development System for ST905X devices with Debugger only
ST902X-DBE	Extension Board for ST902X devices (upgrade part)
ST903X-DBE	Extension Board for ST903X devices (upgrade part)
ST904X-DBE	Extension Board for ST904X devices (upgrade part)
ST905X-DBE	Extension Board for ST905X devices (upgrade part)

SOFTWARE DEVELOPMENT TOOLS FOR ST9 MCU FAMILY

- ST9 Macro Assembler
- ST9 Linker/Loader
- ST9 Library Archiver
- ST9 Software Simulation

GENERAL DESCRIPTION

Full software development is achieved using the ST9 Software Development Tools. This follows for the optional C Compiler, through the High Level Macro Assembler, Linker/Loader, Library Archiver and Software Simulator.

ST9 Macro Assembler

The ST9 Macro Assembler accepts one or more source files written in ST9 assembly language and transforms them into linkable object files. The assembler recognizes the use of symbols, macros, pseudo-instructions, pseudo-macros, and conditional assembly directives.

ST9 Linker/Loader

The ST9 Linker/Loader combines a number of object files into a single program, associating an absolute address to each section of code, and resolving any external references. LST9 may be used to generate: a binary or hexadecimal output module, a map file, and an object file.

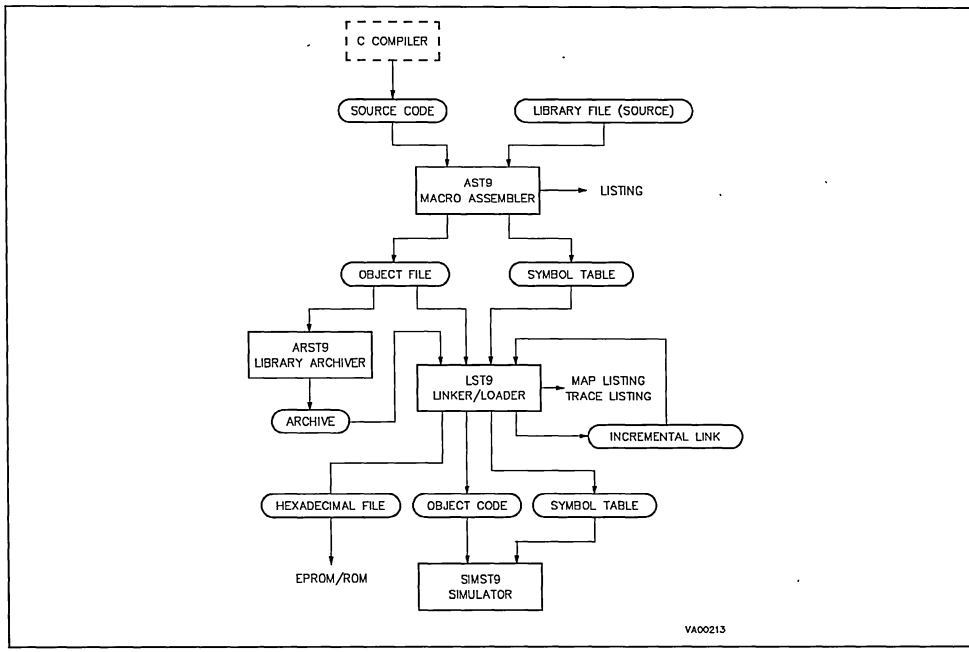
ST9 Library Archiver

The ST9 Library Archiver maintains libraries of software object files, allowing the user to develop standard modules for repetitive use.

ST9 Software Simulator

The ST9 Software Simulator allows the user to debug and execute any program written for any member of the ST9 family of microncontrollers without the aid of additional hardware. The simulator functionally duplicates the operation of the ST9 and completely supports the instruction set.

Figure 1. Development Flow Chart



AST9 - ST9 MACRO ASSEMBLER

- Accepts one or more source files written in ST9 assembly language and produces an object file, a listing file, an alphabetical symbol table, and error diagnostics
- Resulting object files are linkable and relocatable
- Supports program segmenting directives
- Recognizes user defined macros, macro libraries, Conditional assembly directives, pseudo-instructions, and pseudo-macros
- Supports indirect command files

General Description

The ST9 Macro Assembler (AST9) accepts one or more source files written in ST9 assembly language and transforms them into linkable object files. Modules written in assembly language are much easier to write, read, and debug than the equivalent machine code. Furthermore, the assemblers use of symbols, macros, pseudo-instructions, pseudo-macros, and conditional assembly directives, allows for even easier program development.

Figure 2. AST9 Pseudo-Instructions

```
.ascii          stores a string as a sequence of ascii codes
.asciz          same as above followed by a null character
.blkb           allocate bytes of data storage
.blkw           allocate words of data storage
.bss            defines segment as type bss (uninitialized data)
.byte           stores successive bytes of data
.data           defines segment as type data
.defstr         defines a string identifier
.endc           end of a conditional assembly block
.endm           end of a macro
.error          user defined assembly error
.extern         defines symbols as external
.global         defines specified symbols as global
.ifc            beginning of a conditional assembly block
.library        add files to macro-library file list
.list           enables listing of specified fields
.macro          defines a macro
.mcall          specifies which macros must be called from library
.mnarg          assigns to a symbol the number of arguments defined in a
                macro call
.mexit          end of a macro expansion
.nlist          disables listing of specified fields
.org            set current location counter
.page           start a new listing page
.pl             set listing page length
.sbttl          assign subtitle to current section
.text           define segment of type text
.title          assign title to the document
.word           store successive words of data
```

Figure 3. AST9 Pseudo Macros

```
jxcc symbol
if [conditional expression] {macrobody}
if [cond expr] {macrobody} else {macro2}
while [cond expr] {macro}
do {macro} while [cond expr]
loop [loopvar] {macro}
switch [cp] {
        case cp1: macro
        case cp2: macro
        default: macro
}
break
begin [arg1,arg2,...] {macro}
proc procname [arg1,arg2,...] {macro}
return
```

LST9 - ST9 LINKER/IOADER

- Links modules generated by the ST9 Macro Assembler (AST9) encourages modular programming
- Supports indirect command files
- Supports 3 sections (text, data, and bss) which may be relocated and loaded at different addresses. Allows the user to specify the mapping of object files into different pages (supports 8Mbyte addressing of the ST9050).
- Extensive symbol manipulation. produces alphabetically or numerically sorted symbol tables for addresses, registers, or specifically for SIMST9 and SDBST9, strips the symbol table of local symbols, global symbols, or both, allows definition and tracing of symbols.
- Produces binary or hexadecimal output modules
- Generates a map file
- Supports incremental linking
- Resolves references to external symbols and searches libraries for necessary modules
- Provides self explanatory error and warning messages.
- Displays the version number and information about the various phases of linking

General Description

The ST9 Linker/Loader (LST9) is responsible for combining a number of object files into a single program, associating an absolute address to each section of code, and resolving any external references.

LST9 can be used to create either a binary or hexadecimal output module to be used by the ST9. The linker/loader will also produce a map file of the resulting object which gives information about the registers, pages, modules, and labels, or an object file which may be used as an input to another call to the linker.

This software program allows the user to develop modular programs, which may then be combined and addressed as defined by the user. Program modularity allows for easier design and testing, as well as promotes re-use of standard modules.

ARST9 - ST9 LIBRARY ARCHIVER

- Edits libraries by adding, deleting, moving, or replacing files
- Prints a listing of the names of all files in a library, or the table of contents for each file in a library
- Prints a file contained in a library, or extracts it for use without modifying the library
- Libraries may be called by LST9 to resolve external references.

General Description

The ST9 Library Archiver (ARST9) maintains libraries of software object files, allowing the user to develop standard modules for repetitive use. Once a module has been inserted into a library, any application may call the module. The ST9 Linker/Loader (LST9) will only call the portions of each library that are needed to resolve any external references.

SIMST9 - ST9 SOFTWARE SIMULATOR

- Supports symbolic debugging and execution of any program written for the ST9 family of microcontrollers on an IBM PC/XT/AT or compatible computer, without the aid of additional hardware.
- Functionally duplicates the operation of the ST9 family of microcontrollers, and supports the complete instruction set.
- Host Memory may be mapped in groups of 1K byte as Read-only, Read-write, or Non Existent.
- A series of simulator status commands give the user the option of selecting the simulated CPU clock frequency, creating a log of the simulator session, tracing the executed instructions, or enabling the breakpoints and traps.
- The simulator has a command line syntax compatible with SDBST9, the debugger for the ST9-HDS Hardware Development System, and EVMST9, the debugger for the ST9-EVM Evaluation Module.
- A powerful symbol handler allows the user to define symbols and macros, extract them from symbol table files, and save them in symbol table files.

SIMST9 - ST9 SOFTWARE SIMULATOR (Cont'd)

- Full screen video modes are available for Memory, Register, and Single Step Display.
- An On-line help facility is available to give a listing of the complete command set as well as specific information on any of the commands.
- Dump and command file capability allow for simulator session retrieval and easy configuration.
- The simulator provides a symbolic on-line assembler and disassembler.
- A powerful command interpreter allows for the evaluation of complex expressions involving numbers, addresses, memory and register contents, and I/O channel data.
- 128 software breakpoints and 128 software traps are available to the user.
- A trace is kept during program execution which may be displayed afterwards with the traced instructions disassembled into assembler mnemonics.
- A wide range of commands are available for displaying and setting memory and registers according to different formats.
- Macro commands and conditional block constructs are available for use in automated debugging sessions.
- I/O channels can be opened for simulation of I/O peripheral functions.
- Interrupts may be defined and set pending to simulate the occurrence of an interrupt.
- A simulated clock will use the user assigned clock frequency to calculate the real time execution of a program. The clock may be displayed or changed by the user to perform time measurements.

General Description

SIMST9 allows the user to debug and execute any program written for any of the current and future members of the ST9 family of microcontrollers, without the aid of additional hardware. The simulator functionally duplicates the operation of the ST9 and completely supports the instruction set. I/O channels may be opened, read, and written, in order to simulate the I/O functions of peripherals, while interrupts may be set, and then set pending, in order to simulate the handling of interrupts. The simulator uses the clock frequency assigned by the user, along with the number of clock cycles needed by each instruction to keep track of the real time execution speed.

Figure 4. SIMST9 Command Summary

ARCHIVE	Archive symbols and macros
ASM	On-line assembler
BASE	Change base of numbers
BYE	Exit from simulator program
CLOSE	Close I/O channel
CM	Compare memory
DEFINE	Define symbols and macros
DEFINT	Define Interrupts
DISASM	On-line symbolic disassembler
DM	Display memory
DO	Execute macro
DR	Display register
DUMP	Save simulator status
FM	Fill memory
FR	Fill registers
GO	Execute program
HELP	On-line help
IF	Conditional command execution
INTERRUPT	Simulate interrupt
LISTSYMBOL	List symbols and macros
LOAD	Load program/data from file
MAP	Set/display memory mapping
MB	Modify breakpoint
MM	Move block of memory

Figure 4. SIMST9 Command Summary (Continued)

MT	Modify trap
NEXT	Execute program steps
OPEN	Open I/O channel
PRINT	Print strings and values
QUIT	Terminate command execution
RESET	Reset simulated CPU
RESTORE	Restore dump file
SAVE	Save program/data into file
SB	Set/display memory breakpoints
SEARCH	Search a pattern in memory
SET	Set/reset options
SM	Set memory
SR	Set/display registers
ST	Set/display traps
TIME	Set/display user clock counter
TRACE	Display trace
UNDEFINE	Remove symbols
USE	Execute commands from a file
VE	View execution (video mode)
VM	View memory (video mode)
VR	View registers (video mode)
WR	Display current working register set
<value>	Evaluate expression
?	Display symbols having a given value

ORDERING INFORMATION

Part Number	Description	Media
ST9-SW/PC	Macro-assembler/Linker/Simulator on IBM PC XT AT compatibles, under MS-DOS operating system	5 1/4 FD 360K
ST9-SW/VMS	Macro-assembler/Linker/Simulator on VAX and MicroVax systems, under VMS operating system	5 1/4 FD 360K
ST9-SW/SUN3	Macro-assembler/Linker/Simulator on SUN 3, under the UNIX operating system	5 1/4 FD 360K
ST9-SW/SUN4	Macro-assembler/Linker/Simulator on SUN 4 (SPARC station), under the UNIX operating system	5 1/4 FD 360K

ANSI C COMPILER FOR ST9 MCU FAMILY

- Upgraded KERNIGHAN AND RITCHIE C definition, respecting ANSI standard X3.159.
- Optimisation stages using artificial intelligence techniques (calculation of costs in terms of code size and execution time).
- Versions available for IBM PC or compatible under MS-DOS 3.1 and higher, SUN 3 and SUN 4 (SPARC station) under the UNIX operating system and for VAX and microVax under the VMS operating system.
- All standard types allowed (char, int, short, long, signed or unsigned).
- "Float" respecting IEEE 754 standard and "Double" types allowed.
- Many library functions implemented in assembler code for increased code and execution time efficiency e.g. string handling, conversion, I/O routines.
- Generates an assembly language source file, interleaving C lines and assembly language lines.
- Direct access to the Register File of the ST9, allowing access to all on-chip peripherals and features of the ST9.
- Extensions for Real Time Interrupt handling.
- Pre-processor included for standardisation and increased readabilty and portability.
- Available with Macro-Assembler, Linker and Symbolic Software Simulator.
- Fully compatible with the ST9 Hardware Development System supporting symbolic debug and source code high-level debugger.

GENERAL DESCRIPTION

The ST9 ANSI C Compiler allows the programmer to write C source code and produce assembly langage source programs. Used with the assembler/linker, it allows the possibility to generate object code executable for all members of the ST9 microcontroller family. The generated object code may be used for symbolic debugging with the software simulator and hardware debugger/emulator, to generate test EPROM devices for prototyping, or to produce ROM mask data. It takes into account all the advanced features of the ST9 family (interrupt, Register File access, memory pages access). The high-level language C Compiler has been designed to provide the greatest flexibility of use.

The user can either run the complete software with only one simple command, or run each step of the compiler separately: pre-processor, analyser, coder, optimizer.

The ST9 ANSI C Compiler is delivered with a standard initialisation file to be linked with the customer application. This file allows the setting of BSS and DATA sections and stack pointers, as well as peripheral startup code.

STANDARD

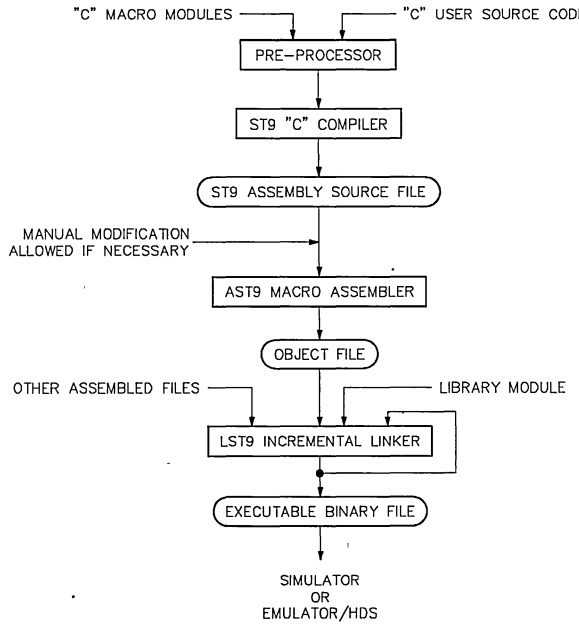
The ST9 ANSI C Compiler is an implementation of the X3.159 ANSI standard (issued from X3J11 draft proposal), which includes and exceeds the Kernighan and Ritchie specification. For example : "CONST" and "VOLATILE" qualifiers and function prototyping.

The ST9 ANSI C Compiler implements the features most often needed by microcontroller developments: interrupt handling, Register File access, far function declarations.

LICENSE

The ST9 ANSI C Compiler is delivered under license for one user only. Upgrading of new releases will be made to each registered user, free of charge, for a duration of 12 months starting from the date of the return of the Registration Card.

Figure 1. ST9-C Flow Chart



ORDERING INFORMATION

Part Number	Description	Media
ST9-SWC/PC	C Compiler/Macro-assembler/Linker/Simulator on IBM PC XT, AT and compatibles, under MS-DOS operating system	$5^1/_4$ FD 360K
ST9-SWC/VMS	C Compiler/Macro-assembler/Linker/Simulator on VAX and MicroVax systems, under VMS operating system	$5^1/_4$ FD 360K
ST9-SWC/SUN3	C Compiler/Macro-assembler/Linker/Simulator on SUN 3, under the UNIX operating system	$5^1/_4$ FD 360K
ST9-SWC/SUN4	C Compiler/Macro-assembler/Linker/Simulator on SUN 4 (SPARC station), under the UNIX operating system	$5^1/_4$ FD 360K
ST9-C/PC	C Compiler Only for IBM PC XT, AT and compatibles, under MS-DOS operating system.	$5^1/_4$ FD 360K
ST9-C/VMS	C Compiler Only for VAX and MicroVax systems, under VMS operating system.	$5^1/_4$ FD 360K
ST9-C/SUN3	C Compiler Only for SUN 3, under UNIX operating system.	$5^1/_4$ FD 360K
ST9-C/SUN4	C Compiler Only for SUN 4 (SPARC station), under UNIX operating system.	$5^1/_4$ FD 360K

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GENERAL INDEX

SELECTION GUIDE

DEVICE	ROM	EPROM	RAM	EEPROM	TWD	SPI	MFT	SCI	A/D	BSS	MAX I/O	HSHK	PACKAGE
ST9026	16K		256		1	1	1	1			40	1	PDIP48
ST9027	16K		256		1	1	1	1			32	1	PDIP40
ST9028	16K		256		1	1	1	1			36	1	PLCC44
ST90E26		16K	256		1	1	1	1			40	1	CDIP48-W
ST90E27		16K	256		1	1	1	1			32	1	CDIP40-W
ST90E28		16K	256		1	1	1	1			36	1	CLCC44-W
ST90T26		16K	256		1	1	1	1			40	1	PDIP48
ST90T27		16K	256		1	1	1	1			32	1	PDIP40
ST90T28		16K	256		1	1	1	1			36	1	PLCC44
ST90R26	–	–	256		1	1	1	1			32	1	PDIP48
ST9030	8K				1	1	2	1	1		56	1	PLCC68
ST9031	8K				1	1	2	1	1		38	1	PDIP48
ST90E30		8K			1	1	2	1	1		56	1	CLCC68-W
ST90E31		8K			1	1	2	1	1		38	1	CDIP48-W
ST90T30		8K			1	1	2	1	1		56	1	PLCC68
ST90T31		8K			1	1	2	1	1		38	1	PDIP48
ST90R30	–	–			1	1	2	1	1		40	1	PLCC68
ST9036	16K		256		1	1	2	1	1		40	1	PLCC68/QFP80
ST9040	16K		256	512	1	1	2	1	1		56	1	PLCC68
ST90E40		16K	256	512	1	1	2	1	1		56	1	CLCC68-W
ST90T40		16K	256	512	1	1	2	1	1		56	1	PLCC68
ST90R40	–	–	256	512	1	1	2	1	1		40	1	PLCC68
ST90R50	–	–			1	1	3	2	1	1	56	2	PLCC84
ST9054	32K		1280		1	1	3	2	1	1	72	2	PLCC84
ST90E54		32K	1280		1	1	3	2	1	1	72	2	CLCC84-W
ST90T54		32K	1280		1	1	3	2	1	1	72	2	PLCC84

Note: All devices have 256 byte Register File with 224 General Purpose Registers (Accumulators/RAM).

Key: TWD Timer/Watchdog
SPI Serial Peripheral Interface
MFT Multi-Function Timer
I/O in: TLL/CMOS, Out: OD/PP
Alternate Functional Peripheral
SCI Serial Communications Interface
A/D 8 bit 8 channel A/D Converter
BSS Bankswitch logic 16M byte address range
HSHK # Ports with Handshake capability