SHARP

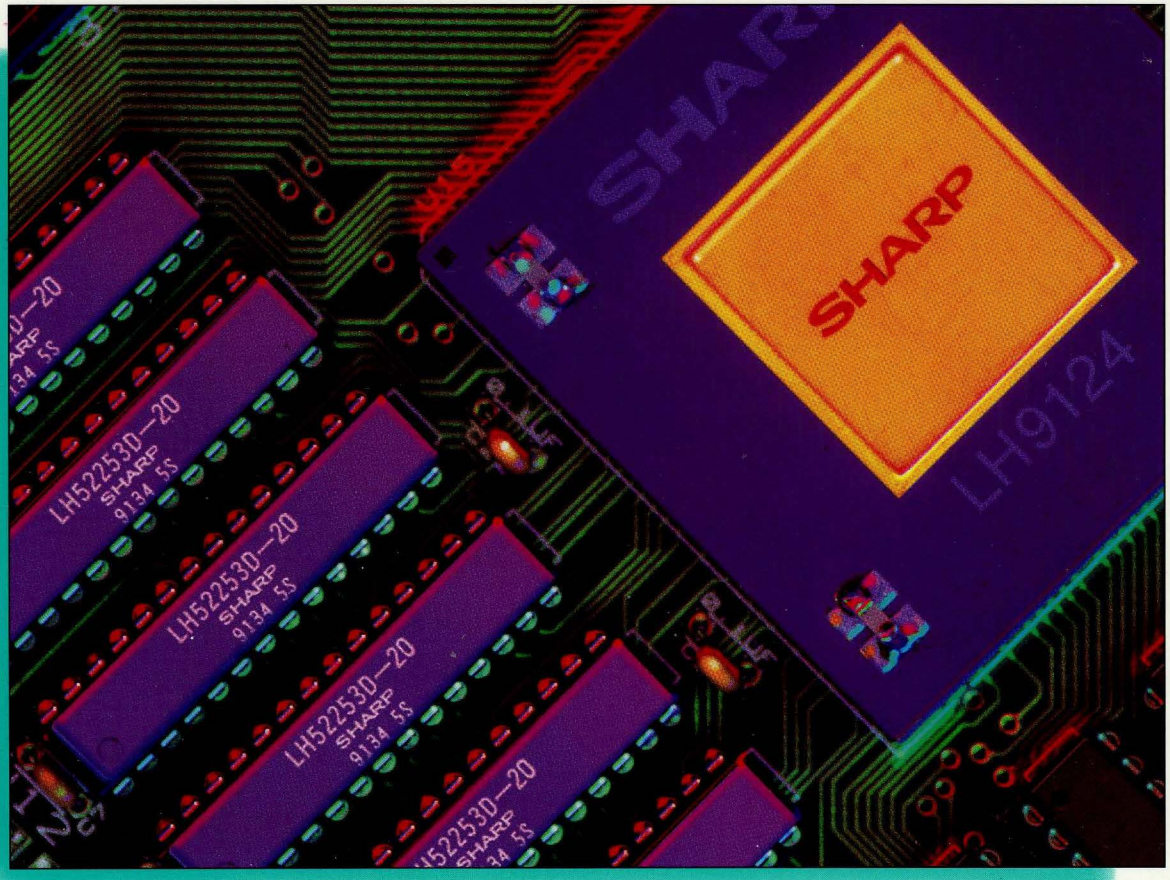
Memory Data Book 1993/1994

UPDATED

1993/1994

UPDATED

MEMORY DATA BOOK



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NOTICE

The specifications contained within this Sharp Memory Data Book are current as of the publication date.

The product data provided is classified and labeled as follows:

CLASSIFICATION *	DESCRIPTION
Product Preview	Contains information about a device that is in the planning stage or the soon to be in-development stage.
Advance Information	Contains information about a device that is in development. Includes design specifications for device development.
Preliminary	Contains information for device soon to be, or recently, released to production.
No label is used for this classification.	Contains information about a device that is in full production.

* Note: occasionally certain product data information may be classified and labeled differently than the main classification label. For example, a main label may be 'Preliminary,' but the 15 ns version of that part may be labeled 'Advance Information.'

Sharp reserves the right to make changes in the circuitry or specifications described herein at any time without notice in order to improve design or reliability. The information in this Memory Data Book has been carefully checked to be accurate, however, Sharp makes no warranty for any errors which may appear in this document. Contact Sharp to obtain the latest version of device specifications before placing your order.

Sharp makes no representations that circuitry described herein is free from infringement of patent or other rights of third parties which may result from its use. No license is granted by implication under any patent rights or other rights of Sharp Corporation.

PREFACE

As we become more and more an information-oriented society, memory products have come to play a major role in both home and office equipment. On the one hand, computer-related services are growing ever more sophisticated and diverse; on the other, they are becoming much more accessible to each of us in our daily lives. Along with this increase in the importance of the information processing in our lives, we are faced with a growing demand for memory products using the most advanced technology.

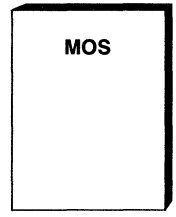
To keep pace with this rapid progress, we at Sharp will continue to direct our efforts at understanding the crucial trends of the moment in this area and supply our customers with products that truly meet their needs. In short, to contribute to a better life for all of us in this age of expanding technology.

Sharp has developed a wide range of memory units including PSRAMs, SRAMs, Mask-Programmable ROMs, and FIFO Memories for use in numerous areas of application. Sharp memory units are used extensively in personal computers, advanced office automation and measuring control equipment, video games, as well as in character processing and dictionary ROMs.

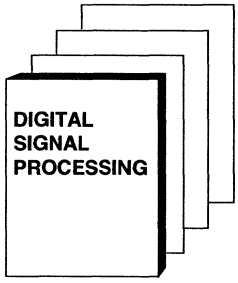
This data book has been especially compiled for the use of our customers. Listed here is the entire range of memory products developed and manufactured by Sharp, with detailed explanations of their many functions and outstanding features. We hope that you find this book useful in determining which Sharp products are best suited to your needs. Please contact us directly if you have any further questions.

SHARP'S INTEGRATED CIRCUIT DOCUMENTATION

- 4-Bit Single-Chip Microcomputers
- 8-Bit Single-Chip Microcomputers
- Development Support Tools

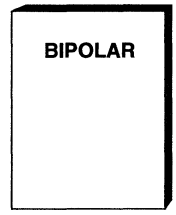


- Gate Arrays/Standard Cells
- Display Drivers, Telecommunications
- MODEMs, CCDs/CCD Peripherals
- ICs for Audio/Visual Equipment
- Voice/Melody Generators, ICs for Clock, etc.

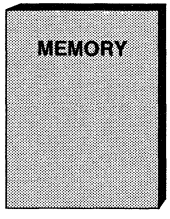


24-Bit Real Time Digital Signal Processing

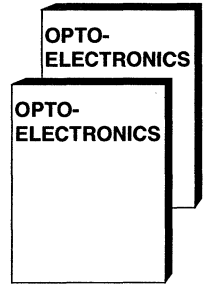
- Data Sheets
- User's Guides
- Simulator Guides
- Application Notes
- Evaluation Modules/Boards



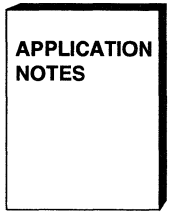
- Operational Amplifiers/Comparators
- Transistor Arrays, Voltage Regulators
- A/D, D/A Converters, Bus Interfaces
- ICs for Audio/Visual Equipment
- CCD Peripherals, ICs for Telephone, etc.



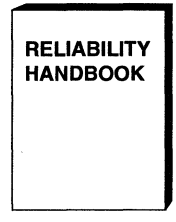
- Pseudo-Static RAMs
- Static RAMs
- Mask-Programmable ROMs
- FIFO Memories
- Application Notes



- LEDs: Infrared Lamps, Panel Displays, Alphanumeric, Numeric, Symbolic, Dot Matrix, Bar-Graphic Displays, High-Resolution Arrays
- Photodiodes, Phototransistors, Photocouplers, Photointerrupters
- Solid-State Relays
- Light-Detecting Units/OPIC Sensors



- Integrated Circuits
- RF Components
- Optoelectronics
- Liquid Crystal Displays



- Quality and Reliability Assurance System
- How Sharp Views Semiconductor Device Reliability and Reliability Prediction
- Reliability Testing
- Failure Analysis
- Proper Handling of Semiconductor Devices

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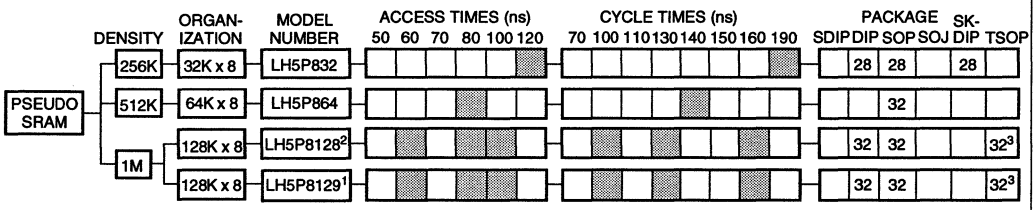
PSEUDO STATIC RAMs



CAPACITY	CONFIG-URATION (WORDS x BITS)	MODEL NO.	ACCESS TIME (ns) MAX.	CYCLE TIME (ns) MIN.	POWER CONSUMPTION OPERATING/ STANDBY (mW) MAX.	OPERATING MODE	PACKAGE
256K	32,768 x 8	LH5P832	100 120	160 190	357.5/16.5 303/16.5	PSEUDO SRAM	28DIP/ 28SK-DIP/ 28SOP
512K	65,536 x 8	LH5P864	80	140	440/5.5	PSEUDO SRAM	32 SOP
1M	131,072 x 8	LH5P8128	60	100	572/5.5	PSEUDO SRAM	32DIP/ 32SOP/ 32TSOP[3]
			80	130	440/5.5		
			100	160	358/5.5		
		LH5P8129	60	100	572/5.5		
			80	130	385/5.5		
			100	160	358/5.5		

NOTES:

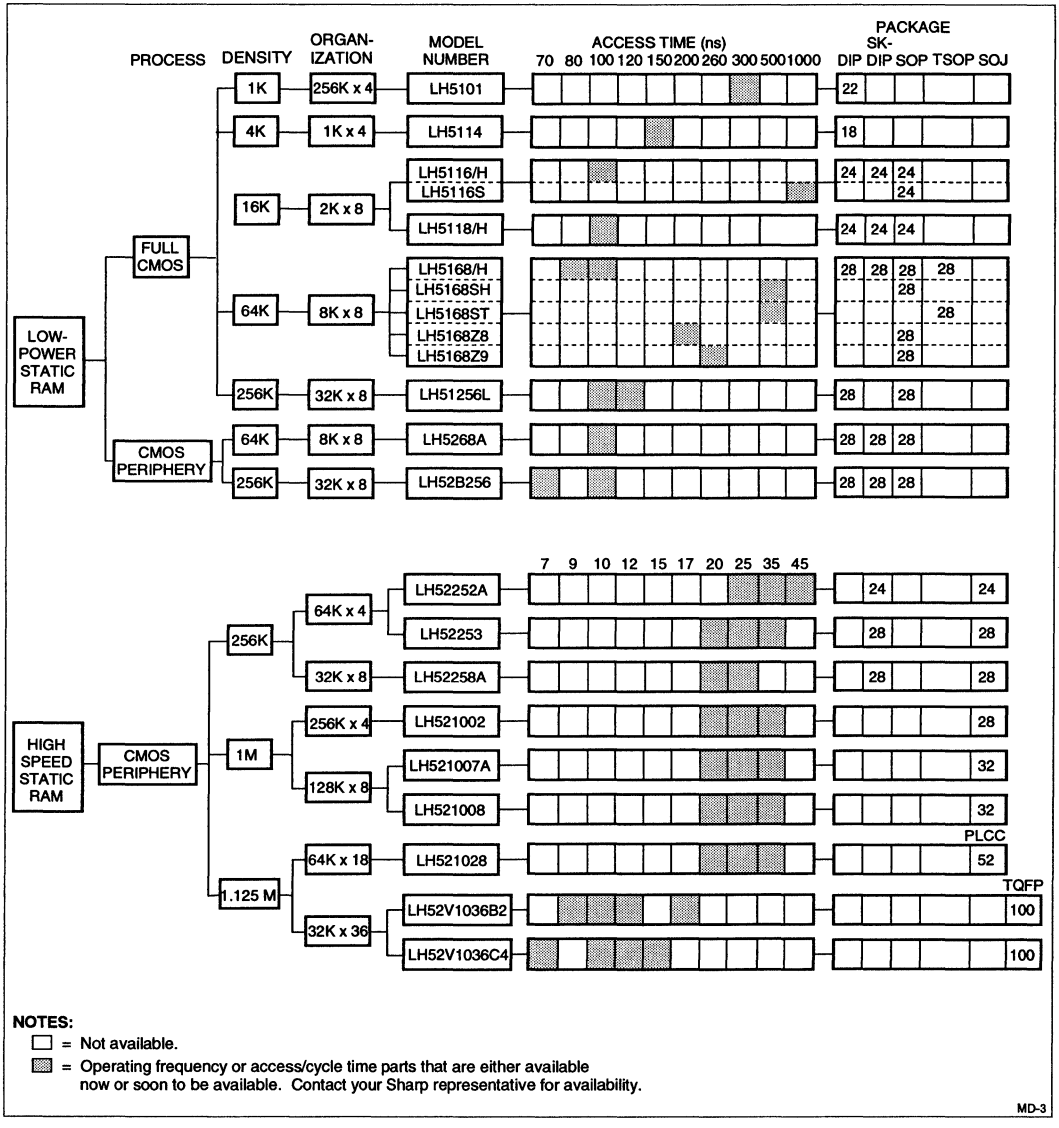
☐ = Not available.

▨ = Operating frequency or access/cycle time parts that are either available now or soon to be available. Contact your Sharp representative for availability.

1. $\overline{CS}$ Control
2. $\overline{CE}$ Control
3. TSOP(I)
4. TSOP(II) - Consult factory for availability.

MD-7A

STATIC RAMs



NOTES:

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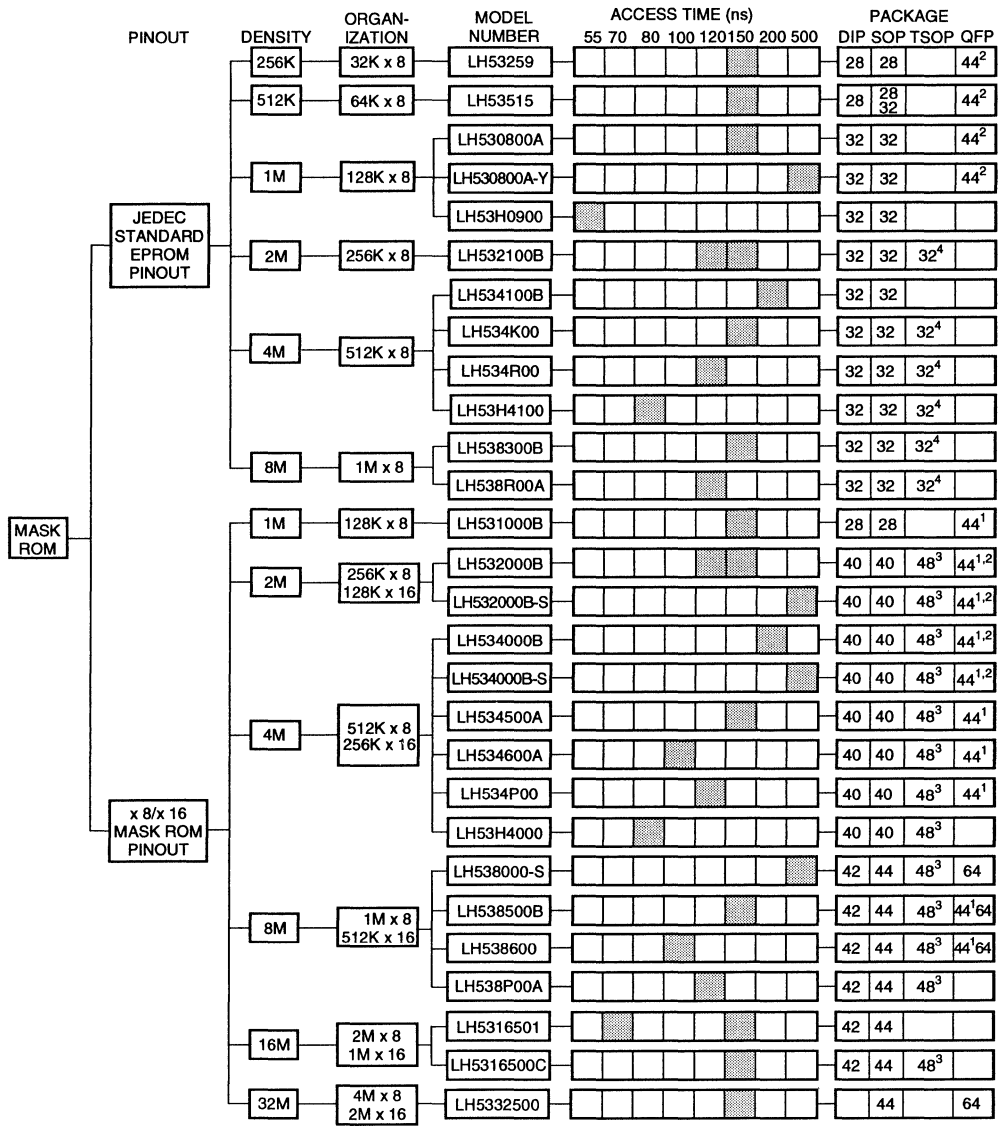
STATIC RAMs

PROCESS	DENSITY	ORGANIZATION (WORDS × BITS)	MODEL NO.	ACCESS TIME (ns) MAX.	CYCLE TIME (ns) MIN.	POWER CONSUMPTION OPERATING/ STANDBY (mW/μW) MAX.	PACKAGE
FULL CMOS	1K	256 × 4	LH5101	300	300	137.5/55	22DIP
	4K	1,024 × 4	LH5114	150	150	110/27.5	18DIP
	16K	2,048 × 8	LH5116	100	100	220/5.5	24DIP/24SOP/24SK-DIP
			LH5116H [1]	100	100	220/5.5	
			LH5116S [4]	1000	1000	33/3.3	24SOP
			LH5118	100	100	220/5.5	24DIP/24SOP/24SK-DIP
			LH5118H [1]	100	100	220/5.5	
	64K	8,192 × 8	LH5168	100	100	248/5.5	28DIP/28SOP/28SK-DIP/ 28TSOP(I)
			LH5168H [1]	100	100	275/16.5	28DIP/28SOP/28SK-DIP
			LH5168SH [1, 4]	500	500	60/9 (3V)	28SOP
			LH5168ST	500	500	60/3 (3V)	28TSOP(I)
			LH5168Z8	200	200	60/3 (3V)	28SOP
			LH5168Z9	260	260	60/3 (3V)	28SOP
	256K	32,768 × 8	LH51256L [1]	100	100	248/27.5	28DIP/28SOP
				120	120		
CMOS PERIPHERY	64K	8,192 × 8	LH5268A	100	100	220/220	28DIP/28SK-DIP/28SOP
	256K	65,536 × 4	LH52252A	25	25	825/5500	24SK-DIP/24SOJ
				35	35	660/5500	
				45	45	550/5500	
			LH52253	20	20	800/5500	28SK-DIP/28SOJ
				25	25	745/5500	
				35	35	745/5500	
		32,768 × 8	LH52B256	70	70	440/550	28DIP/28SOP/28SK-DIP/ 28TSOP(I)
				100	100	385/550	
			LH52258A	20	20	825/5500	28SK-DIP/28SOJ
				25	25	745/5500	
	1M	262,144 × 4	LH521002	20	20	715/11000	28SOJ
				25	25	660/11000	
				35	35	550/11000	
		131,072 × 8	LH521008	20	20	825/11000	32SOJ
				25	25	770/11000	
				35	35	660/11000	
			LH521007A	20	20	770/27500	32SOJ
				25	25	688/27500	
				35	35	633/27500	
	1.125M	65,536 × 18	LH521028	20	20	1650/275000	52PLCC
				25	25	1650/275000	
				35	35	1650/275000	
		32,768 × 36	LH52V1036B2	9	15	866/295	100TQFP
				10	15	866/295	
				12	20	728/243	
				17	25	624/208	
			LH52V1036C4	7	15	866/295	
				10	20	728/243	
				12	25	624/208	
				15	30	572/191	

NOTES:

1. T_{OPR} = -40 to +85°C
2. T TSOP (Type I) Forward bend
   TR TSOP (Type I) Reverse bend
3. Supply Voltage (V) = 3 ± 10%
4. Supply Voltage (V) = 2.5 to 5.5

MASK-PROGRAMMABLE ROMs



NOTES:

□ = Not available.

▨ = Operating frequency or access/cycle time parts that are either available now or soon to be available. Contact your Sharp representative for availability.

LH5XXX: CMOS

1. 14 x 14 mm² package
2. QFP also available in 10 x 10 mm² package
3. TSOP (Type I)
4. TSOP (Type II)

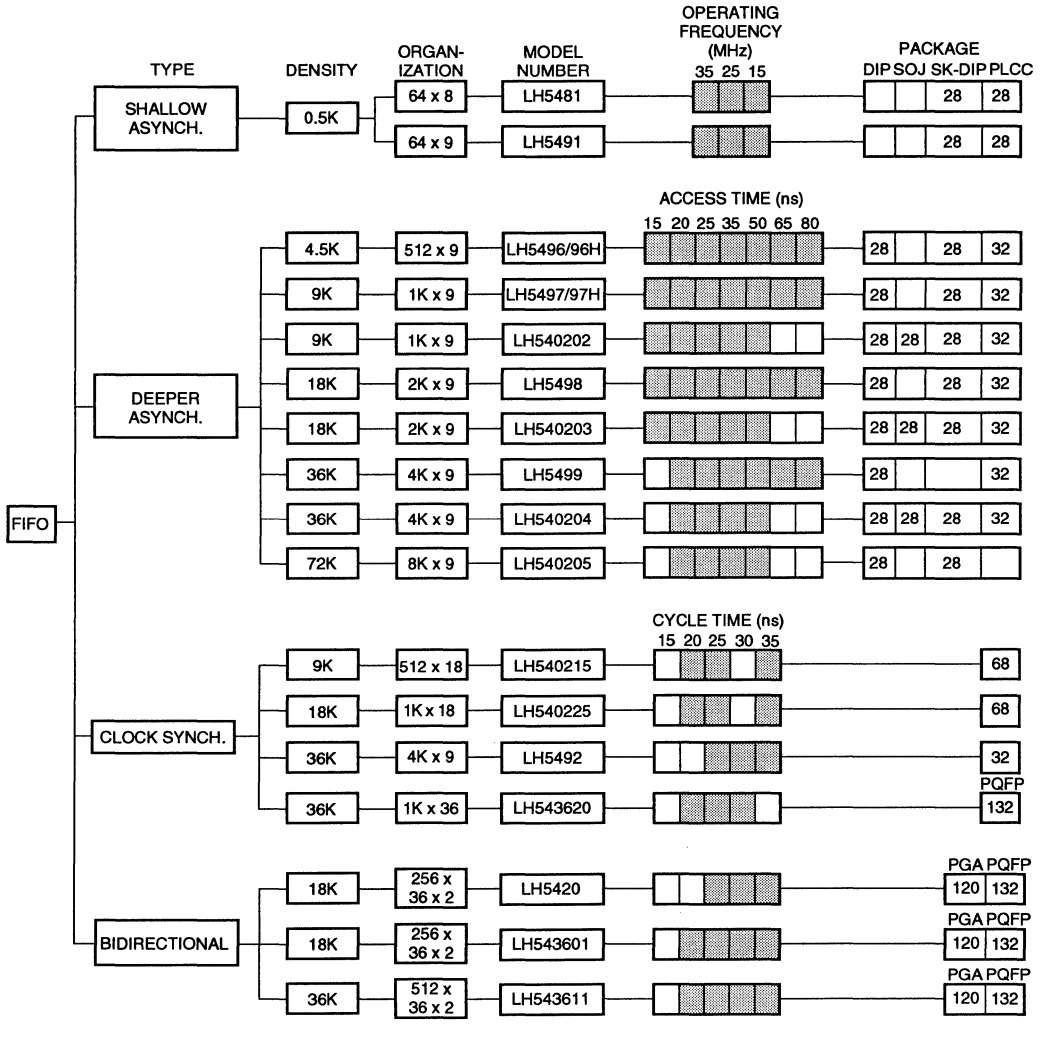
MASK-PROGRAMMABLE ROMs

DENSITY	ORGANIZATION (WORDS × BITS)	MODEL NO.	USERS NO.	ACCESS TIME (ns) MAX. CYCLE TIME (ns) MIN.	POWER CONSUMPTION (mW) MAX.	PACKAGE
256K	32,768 × 8	LH53259	LH5359XX	150	110	28DIP/28SOP/44QFP [2]
512K	65,536 × 8	LH53515	LH5315XX	150	195	28DIP/28SOP/44QFP [2] /32SOP
1M	131,072 × 8	LH53H0900	LH5H09XX	55	660	32DIP/32SOP
		LH530800A	LH531HXX	150	195	32DIP/32SOP/44QFP [2]
		LH530800A-Y	LH531YXX	500	193	32DIP/32SOP/44QFP [2]
		LH531000B	LH531GXX	150	195	28DIP/28SOP/44QFP [1]
2M	262,144 × 8	LH532100B	LH532HXX	120/150	275	32DIP/32SOP/32TSOP(II)
	262,144 × 8 131,072 × 16	LH532000B	LH532GXX	120/150	275	40DIP/40SOP/44QFP [1,2] /48TSOP(I)
		LH532000B-S	LH532SXX	500	225/275	40DIP/40SOP/44QFP [1,2] /48TSOP(I)
4M	524,288 × 8	LH53H4100	LH5H41XX	80	550	32DIP/32SOP/32TSOP(II)
		LH534K00	LH534KXX	150	330	32DIP/32SOP/32TSOP(II)
		LH534R00	LH534RXX	120	358	32DIP/32SOP/32TSOP(II)
		LH534100B	LH534HXX	200	275	32DIP/32SOP
	524,288 × 8 262,144 × 16	LH53H4000	LH5H40XX	80	550	40DIP/40SOP/48TSOP(I)
		LH534P00	LH534PXX	120	358	40DIP/40SOP/44QFP [1] /48TSOP(I)
		LH534600A	LH534UXX	100	550	40DIP/40SOP/44QFP [1] /48TSOP(I)
		LH534500A	LH534FXX	150	275	40DIP/40SOP/44QFP [1] /48TSOP(I)
		LH534000B	LH534GXX	200	275	40DIP/40SOP/44QFP [1,2] /48TSOP(I)
		LH534000B-S	LH534SXX	500	225/275	40DIP/40SOP/44QFP [1,2] /48TSOP(I)
8M	1,048,576 × 8	LH538R00A	LH538HXX	120	330	32DIP/32SOP/32TSOP(II)
		LH538300B	LH5383XX	150	275	32DIP/32SOP/32TSOP(II)
	1,048,576 × 8 524,288 × 16	LH538P00A	LH538PXX	120	330	42DIP/44SOP/48TSOP(I)
		LH538000-S	LH538SXX	500	225/275	42DIP/44SOP/48TSOP(I)/64QFP
		LH538500B	LH5385XX	150	275	42DIP/44SOP/44QFP [1] /64QFP/48TSOP(I)
		LH538600	LH5386XX	100	385	42DIP/44SOP/44QFP [1] /64QFP/48TSOP(I)
16M	2,097,152 × 8 1,048,576 × 16	LH5316500C	LH5370XX	150	275	42DIP/44SOP/48TSOP(I)
		LH5316501	LH5371XX	150/70 [3]	385	42DIP/44SOP
32M	4,194,304 × 8 2,097,152 × 16	LH5332500	LH5355XX	150	275	44SOP/64QFP

NOTES:

1. 14 × 14 mm^2 package
2. QFP also available in 10 × 10 mm^2 package
3. Page Mode only available in 70 ns

FIFO MEMORIES



NOTES:

☐ = Contact your Sharp representative for availability.

▨ = Operating frequency or access/cycle time parts which either are available now or are soon to be available. Contact your Sharp representative for availability. Asychronous parts are specified according to access time or operating frequency; synchronous parts are specified according to cycle time.

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FIFO MEMORIES

DENSITY	ORGANIZATION (WORDS × BITS)	MODEL NO.	OPERATING FREQUENCY (MHz)	ACCESS TIME (ns) MAX.	CYCLE TIME (ns) MIN.	POWER CONSUMPTION (mW) MAX. ACTIVE/ STANDBY	PACKAGE
0.5K	64 × 8	LH5481	15	26	67	248/ –	28SK-DIP/28PLCC
			25	22	40		
			35	20	28		
	64 × 9	LH5491	15	26	67	248/ –	28SK-DIP/28PLCC
			25	22	40		
			35	20	28		
4.5K	512 × 9	LH5496	40	15	25	550/28	28SK-DIP/28DIP/32PLCC
		LH5496/96H	33	20	30		
			28	25	35		
			22	35	45		
			15	50	65		
			12	65	80		
			10	80	100		
9K	1,024 × 9	LH5497	40	15	25	550/28	28SK-DIP/28DIP/32PLCC
		LH5497/97H	33	20	30		
			28	25	35		
			22	35	45		
			15	50	65		
			12	65	80		
			10	80	100		
		LH540202 *	40	15	25	550/28	28SK-DIP/28DIP/28SOJ/ 32PLCC
			33	20	30		
			28	25	35		
			22	35	45		
			15	50	65		
	512 × 18	LH540215 *	50	12	20	550/28	68PLCC
			40	15	25		
			28	20	35		
18K	256 × 36 × 2	LH5420	40	15	25	1540/ –	120PGA/132PQFP
			33	20	30		
			28	25	35		
		LH543601 *	50	12	20	1540/ –	120PGA/132PQFP
			40	15	25		
			33	18	30		
			28	21	35		
	2,048 × 9	LH5498	40	15	25	550/28	28SK-DIP/28DIP/32PLCC
			33	20	30		
			28	25	35		
			22	35	45		
			15	50	65		
			12	65	80		
			10	80	100		

▒ Primary parameter for speed-grade specification.

* Contact your Sharp representative for availability.

FIFO MEMORIES (cont'd)

DENSITY	ORGANIZATION (WORDS × BITS)	MODEL NO.	OPERATING FREQUENCY (MHz)	ACCESS TIME (ns) MAX.	CYCLE TIME (ns) MIN.	POWER CONSUMPTION (mW) MAX. ACTIVE/ STANDBY	PACKAGE
18K	2,048 × 9	LH540203 *	40	15	25	550/28	28SK-DIP/28DIP/28SOJ/ 32PLCC
			33	20	30		
			28	25	35		
			22	35	45		
			15	50	65		
	1,024 × 18	LH540225 *	50	12	20	550/28	68PLCC
			40	15	25		
			28	20	35		
			20	25	50		
36K	512 × 36 × 2	LH543611 *	50	12	20	1540/ –	120PGA/132PQFP
			40	15	25		
			33	18	30		
			28	21	35		
	4,096 × 9	LH5499	33	20	30	605/44	28DIP/32PLCC
			28	25	35		
			22	35	45		
			15	50	65		
			12	65	80		
			10	80	100		
		LH540204 *	33	20	30	605/44	28SK-DIP/28DIP/28SOJ/ 32PLCC
			28	25	35		
			22	35	45		
			15	50	65		
		LH5492	40	20	25	825/138	32PLCC
			33	22	30		
			28	25	35		
	1,024 × 36	LH543620 *	50	14	20	TBD	132PQFP
			40	15	25		
			33	21	30		
72K	8,192 × 9	LH540205 *	33	20	30	605/44	28SK-DIP/28DIP
			28	25	35		
			22	35	45		
			15	50	65		

▒ Primary parameter for speed-grade specification.

* Contact your Sharp representative for availability.

QUALITY ASSURANCE

Quality Assurance System

Sharp develops and produces a wide range of consumer and industrial-use semiconductor products.

In recent years, the applications of ICs have expanded significantly, into fields where extremely high levels of quality are critical.

In response, Sharp has implemented a total quality assurance system that encompasses the entire production process from planning to after-sales service. This system ensures that quality is a priority in the planning development and production and guarantees product reliability through rigorous reliability testing. We compiled the "Sharp Semiconductor Reliability Handbook, IC Edition" to introduce you to the results of some of our research and to our quality and reliability philosophy and programs. We hope that it is informative and that it will help Sharp customers develop and refine their quality and reliability assurance and control activities. We will introduce a part of this system here.

Sharp's quality and reliability assurance activities are based on the following guidelines:

- All personnel should participate in quality assurance by continually cultivating a higher level of quality awareness.
- In the design and development stages of new products, create reliable designs that consider reliability in every respect.
- Quality control in all production processes, all working environments, materials, equipment, and measuring devices should be carefully monitored to ensure quality and reliability from the very beginning of the production process.
- Confirm long-term reliability and obtain a thorough understanding of practical limits through reliability testing.
- Continually work to improve quality through application of data from process inspections, reliability testing, and market surveys.

Quality Assurance During New Product Development

New product development ***(Figure 1)*** begins with an accurate grasp of the purpose, environment, and manners in which customers will use the product as well as the required reliability. A development plan is then drafted, clarifying the price, quantity, sales period and target reliability of the product to be manufactured.

Quality and reliability are built into the product from the beginning of the product cycle by introducing design review (DR) and reliability planning in the development and design stage. The first tasks undertaken in this stage are process development and circuitry design, by which a prototype, or technical sample (TS), is made. An evaluation of the technical sample is conducted, centering on the function and performance of the sample under conditions in which the final product will be used (TS evaluation).

Next, an engineering sample (ES) is made, based on the results of the TS evaluation, and it is subjected to ES evaluation. The ES evaluation consists of determining, under mass production conditions, whether the product functions and performs as intended during development and design. Reliability testing is also used to decide whether the engineering sample has the required degree of reliability.

In the final stage, the transfer of the product to mass production is discussed - based on the results of the TS and ES evaluations. Once TS and ES are accepted, preproduction begins. At this time, it is determined whether the quality and reliability obtained during development and design can be maintained, whether there are any discrepancies in the production process and what yields will be. The manufacturability of the product is determined, based on these results.

DR (Design Review) is performed to prevent faulty operation and to enhance the functions, usability, quality and reliability, upon completion of structural design, logic design, software design, circuit design, TS/ES evaluation and reliability tests.

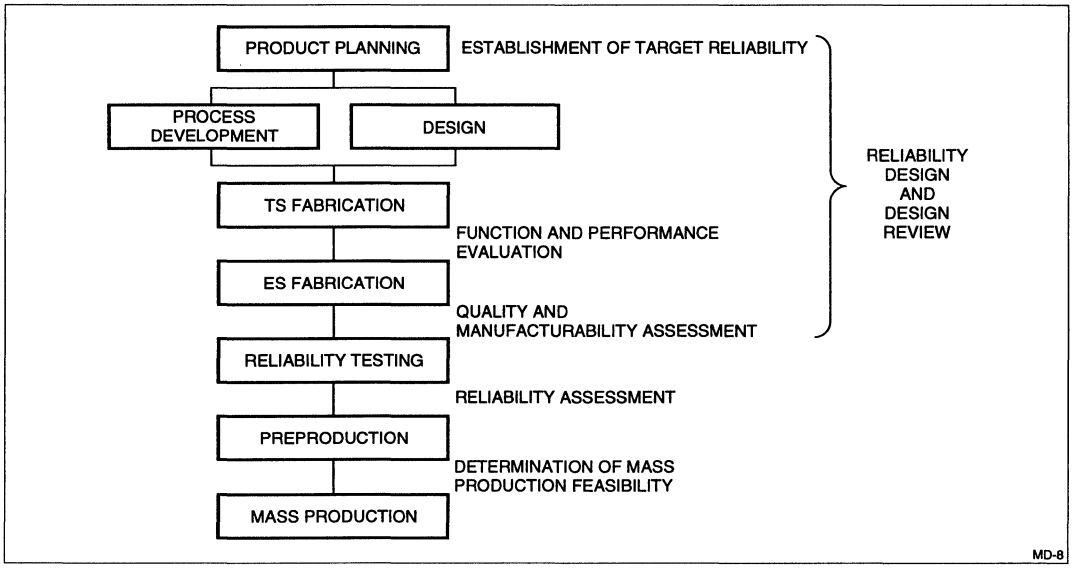

Figure 1. New Product Development Steps

PROCESS	CHARACTERISTIC(S) CONTROLLED	PURPOSE OF CONTROL
SILICON WAFER INCOMING INSPECTION	EXTERNAL APPEARANCE, DIMENSIONS, SHEET RESISTIVITY	REMOVE PRODUCTS HAVING IMPROPER DIMENSIONS, FLAWS AND CRYSTAL DEFECTS. ENSURE PROPER SHEET RESISTANCE VALUES
OXIDATION		
OXIDE INSPECTION MONITORING	EXTERNAL APPEARANCE, FILM THICKNESS, SURFACE CLEANLINESS	FIND PINHOLES, CHECK SURFACE CLEANLINESS AND CONTROL FILM THICKNESS
PHOTOLITHOGRAPHY		
VISUAL INSPECTION MONITORING	DEVELOPABILITY, ETCHABILITY, LINE WIDTH	CHECK FOR PROPER DEVELOPMENT AND ETCHING. CONTROL LINE WIDTH
ION IMPLANTATION		
ELECTRICAL INSPECTION OF CHIP MONITORING	ELECTRICAL CHARACTERISTICS, MAJOR DEVICE CHARACTERISTICS	REMOVE PRODUCTS HAVING POOR ELECTRICAL CHARACTERISTICS. ENSURE PROPER DEVICE CHARACTERISTICS
FRAME DICING		
BREAK, SORTING		
DIE INSPECTION	EXTERNAL APPEARANCE	REMOVE CRACKED AND CHIPPED ITEMS.
DIE BONDS		
WIRE DIE BOND INSPECTION MONITORING	EXTERNAL APPEARANCE ADHESIVE STRENGTH	ENSURE QUALITY OF DIE BONDS
WIRE BONDS		
MOLDING COMPOUNDS WIRE BOND INSPECTION MONITORING	EXTERNAL APPEARANCE TENSILE STRENGTH	CHECK POSITION AND SHAPE OF BONDS. ENSURE PROPER WIRE TENSILE STRENGTH
ENCAPSULATION/MOLD MONITORING	TEMPERATURE, TIME, STRESS WIRE CONDUCTIVITY	ENSURE MOLDABILITY. ENSURE PROPER WIRE CONFIGURATION
STABILIZED BAKE		
LEAD SURFACE FINISHING	INGREDIENTS, TEMPERATURE, CONTAMINATION	MAINTAIN FINISH QUALITY
FINISHING INSPECTION MONITORING	THICKNESS, UNIFORMITY (SOLDERABILITY) PLATED LAYER COMPOSITION PLATED LAYER THICKNESS	REMOVE PRODUCTS HAVING PLATING IRREGULARITIES. MAINTAIN PLATING QUALITY
MARKING	TEMPERATURE, TIME, MARKING MATERIAL	MAINTAIN MARK QUALITY
LEAD CUT FORMING	TOOLING SHARPNESS TOOLING DIMENSIONS	PREVENT ABNORMAL STRESS ON PLASTIC MOLD RESULTING IN DAMAGE

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Figure 2. Example of the Quality Control Process

Raw Materials Control

The level of product quality and reliability is largely governed by the quality of the materials originally making up the production process and environment.

It is the responsibility of the vendor to execute the quality assurance of basic materials purchased by Sharp. Raw material quality assurance is conducted according to the following system:

- Initial selections of a raw material manufacturer.
- Quality qualification for each new material put into use (quality and reliability assessments of devices in which such new materials are used).
- Periodic quality consultations based on quality information obtained during mass production.

Acceptance inspections are carried out as necessary based on acceptance criteria derived from product specifications and approved drawings.

Control of the Manufacturing Environment

Integrated circuit devices are manufactured in a clean room where there is minimal airborne particulates. The use of ultrapure water also aids cleanliness. Such conditions are necessary due to the adhesion of even small bits of foreign particles (0.1 μm or less), no more than 1/5 - 1/10 the size of the smallest IC pattern, can result in defects later in the process.

Particulates not only affects chip yields, but can also have a lethal affect on the quality and reliablity of a device. Therefore, the cleanliness of every piece of equipment and facility in the plant as well as that of work clothes and work articles are controlled. Degree of cleanliness is usually expressed numerically as the number of particles over 0.5 μm per cubic foot of air.

The degree of cleanliness maintained in Sharp clean rooms, where wafers come in direct contact with air, is Class 1. Temperature and humidity are maintained at constant levels by continuous computer-controlled monitoring ***(Table 1).***

The ultrapure de-ionized (DI) water used in the wafer process is manufactured with an ultrapurification equipment, employing ion-exchange treatment, ultraviolet irradiation and ultrafiltration systems.

Table 1.
Clean Room Temperature & Humidity Standards

Temperature	24 ± 0.5°C
Humidity	45 ± 5% RH

Control of Facilities and Instrumentation

Intregrated circuit device technology is experiencing rapid revolutionary change, and advances in IC production facilities and equipment are equally impressive.

Process automation is promoted by using the latest CIM (Computer Intregrated Manufacturing) system to create devices having stable quality and to reduce variance of characteristics. In addition, production facilities maintenance control, and precision control for various instrumentation devices are implemented by both daily and periodic spot inspections.

Facilities' control is conceptually based on Total Productive Maintenance (TPM), in which all concerned employees systematically participate in facilities maintenance activities. Sharp's goal is to create a highly skilled human resource through activities such as:

- operator-initiated maintenance;
- scheduled maintenance;
- corrective maintenance.

Control of instrumentation devices is in accordance with Japanese national standards. Regular calibration by overseeing public agencies also helps maintain a high level of accuracy in these devices.

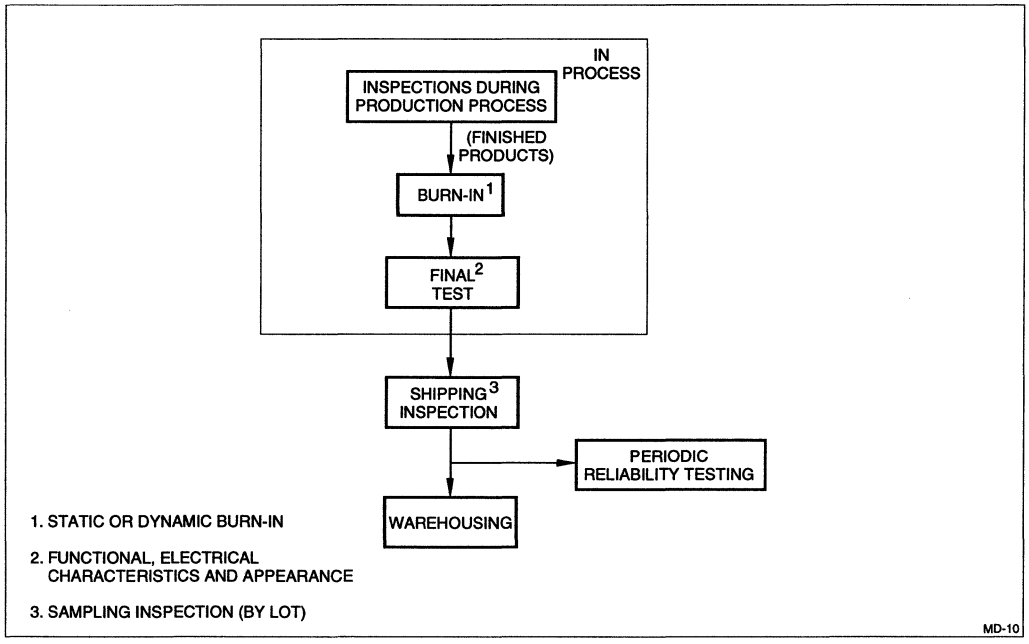


Figure 3. Product Inspection System

Quality Control During the Production Process

Designed-in quality and reliability must be faithfully built into a device during production to manufacture consistently high-quality and high-reliability products.

Production Operations are therefore based on specific, established operational standards. Checks are performed at each process step to decide whether specific characteristics have been obtained and quality has been built in. Each process is monitored to ensure that defectives are not sent to the next process. This is done by rigorously carrying out various standardized controls, appropriate to each process, such as monitoring, visual inspections and sampling inspections.

Sharp strongly promotes the automation of production facilities and equipment. Sharp works to prevent quality problems before they occur and to stabilize quality. Operations that required human skills in the past are now automated. Computer Integrated Manufacturing (CIM) is being introduced into the wafer process. CIM is used to implement comprehensive production control, including conveyance within a process, equipment monitoring and progress control. CIM enables several types of process data to be processed together. Control charts and process capacity index (Cpk) are computed in real time for individual pieces of equipment. Even minute fluctuations in characteristics are fed back to improve control.

Reliability is also being assessed by periodic sampling. This test is a long-term reliability assessment, and the results are fed back to the related divisions.

While quality assurance tests and inspections are conducted for improving and maintaining quality, they also are used to predict the probable reliability a product will have in the marketplace. They provide a multi-faceted approach to ensuring product quality.

Table 2.
Reliability Test Items

CLASSIFICATION	TEST	PURPOSE &CONDITIONS	REFERENCE STANDARDS
Thermal Environment Tests	Soldering Heat	To determine soldering heat resistance. Standard test conditions: Solder bath temperature: 260 ± 5°C Time: 10 ± 1 sec. Solder composition: Pb:Sn = 4:6	JIS C 7022: A-1 MIL-STD-750 C 2031 IEC Pub. 68 Test Tb
	Temperature Cycling	To determine resistance to high and low temperatures and to temperature changes between these extremes. Standard test conditions: $T_a = T_{stg\ MIN} \sim T_{stg\ MAX}$ [gas environment]	JIS C 7022: A-4 MIL-STD-883 C 1010 IEC Pub. 68 Test Na, Nb
	Thermal Shock	To determine resistance to sudden changes in temperature. Standard test conditions: $T_a = T_{stg\ MIN} \sim T_{stg\ MAX}$ [liquid environment]	JIS C 7022: A-3 MIL-STD-883 C 1011 IEC Pub. 68 Test Nc
Mechanical Environment Tests	Variable Frequency Vibration	To determine resistance to vibration during transportation and use. Standard test conditions: Cycle: 100 ~ 2000 Hz in 4 min. Peak acceleration: 20 G Orientation: four (4) times in each of the orientations of ± X, ± Y and ± Z	JIS C 7022: A-10 MIL-STD-883 C 2007 IEC Pub. 68 Test Fc
	Mechanical Shock	To determine resistance to shocks during transportation & use. Standard test conditions: Peak acceleration: 1500 G Pulse duration: 0.5 ms Orientation: three (3) pulses in each of the orientations ± X, ± Y and ± Z	JIS C 7022: A-7 MIL-STD-883 C 2002 IEC Pub. 68 Test Ea
	Constant Acceleration	To determine resistance to constant acceleration. Standard test conditions: Stress level: 20,000 G, Orientation: applied for one (1) min. in each of the orientations ± X, ± Y and ± Z	JIS C 7022: A-9 MIL-STD-883 C 2001 IEC Pub. 68 Test Ga
	Lead Integrity	To determine resistance to installation and handling such as wiring. (1) Tensile strength. Standard test conditions: A specified load is applied in a direction parallel to the lead axis for 10 ± 1 sec. (2) Bending strength. Standard test conditions: A specified load is applied to the tip of each lead and the lead is bent once each through a + and - 90° arc and back. (The specified load is determined by nominal cross section or nominal section modulus.) *TCP (tape carrier package): N/A	JIS C 7002: A-11 IEC Pub. 68 Test U

Table 2. (cont'd)
Reliability Test Items

CLASSIFICATION	TEST	PURPOSE &CONDITIONS	REFERENCE STANDARDS
Mechanical Environment Tests	Solderability	To determine the solderability of leads which are connected by soldering. Standard test conditions: Solder bath temperature: 230 ± 5°C, Dip time: 5 ± 0.5 sec. Solder composition: Pb:Sn = 4:6, used with rosin flux.	JIS C 7022: A-2 MIL-STD-883 C 2003
	Seal (Hermeticity)	To determine the effectiveness of the seal of hermetically sealed devices. (1) Fine leak detection (helium): measured with a helium detector after storage in an He atmosphere at a prescribed pressure for a designated time period. (2) Gross leak observation (bubbles): observation of bubbles formed by a fluorocarbon or silicone oil.	JIS C 7022: A-6 MIL-STD-883 C 1014 IEC Pub. 68 Test Q
Life Tests	High Temperature Operation	To determine resistance to prolonged operating stress, electrical and thermal. Standard test conditions: $T_a = T_{op\ MAX}$ Operating source voltage = Max. operating voltage	JIS C 7022: B-1 MIL-STD-883 C 1005
	High Temperature Storage	To determine resistance to prolonged high temperature storage. Standard test conditions: $T_a = T_{stg\ MAX}$	JIS C 7022: B-3 MIL-STD-883 C 1008
	Low Temperature Storage	To determine resistance to prolonged low temperature storage. Standard test conditions: $T_a = T_{stg\ MIN}$	JIS C 7022: B-4 IEC Pub. 68 Test A
	High Temperature/ High Humidity Bias	To determine resistance to prolonged temperature, humidity and electrical stress. Standard test conditions: 85°C, 85% RH Applied voltage = $V_{TYPICAL}$	JIS C 7022: B-5 IEC Pub. 68 Test C

Table 2. (cont'd)
Reliability Test Items

CLASSIFICATION	TEST	PURPOSE &CONDITIONS	REFERENCE STANDARDS
Miscellaneous	Pressure Cooker (PCT)	To evaluate moisture resistance in a short period of time. Standard test conditions: 121°C, 2atm, no electrical load. 100% RH	EIAJ IC-121: 18
	Composite Test	Several tests (selected from those listed above) performed in series to effectively evaluate product. Example: for a surface mount device: High-Temperature/High-Humidity Storage→Soldering Heat Resistance→Pressure cooker (PCT)	
	Electrostatic Discharge Strength	To determine resistance to electrostatic stress. Standard test conditions: (1) Human body model: Earth capacity C = 100 pF, equivalent Resistance R = 1.5 kΩ (2) Machine model: Earth capacity C = 200 pF, equivalent Resistance R = 0Ω	MIL-STD-883 C 3015 EIAJ IC-121:20
	Latch-Up Strength	To determine resistance to latch-up. Standard test conditions: (1) Condenser charge (2) Current application (3) V_{CC} overvoltage application	

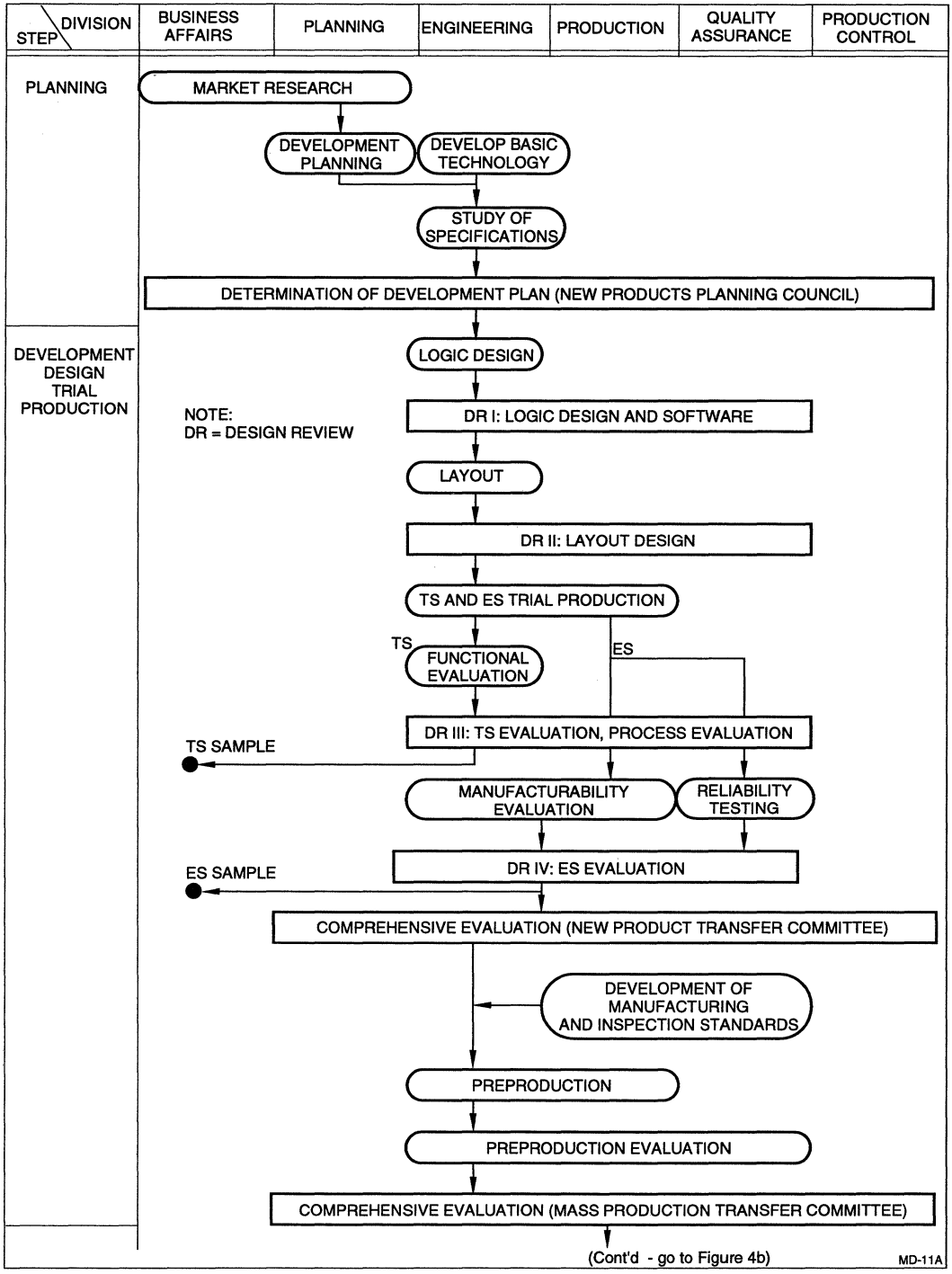


Figure 4a. Quality Assurance System

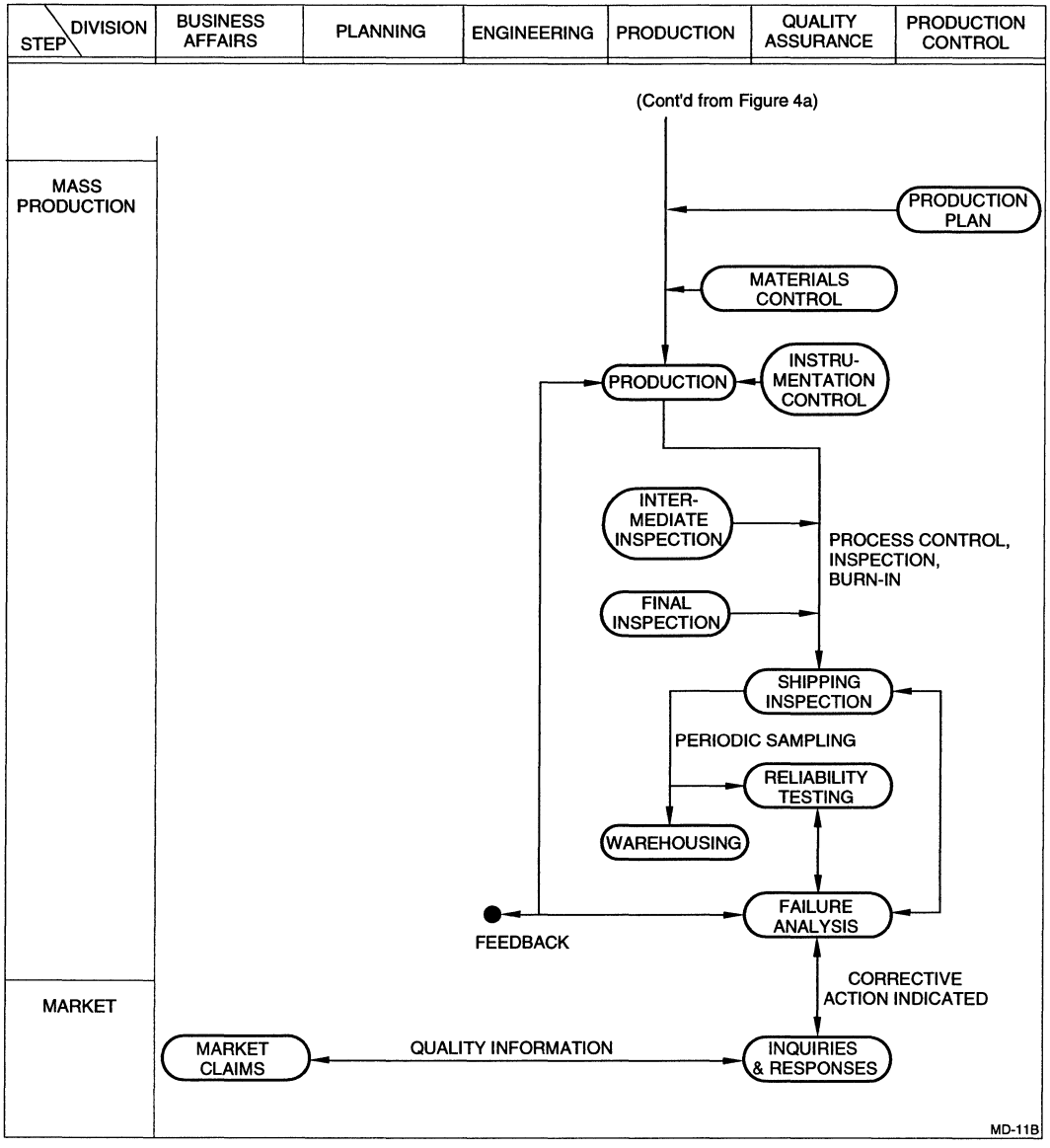


Figure 4b. Quality Assurance System

Reliability Tests

Reliability Test Methods

Reliability tests should always have good reproducibility. Thus, reliability tests for IC devices are based on standardized test methods. Such uniform testing standards include those established by JIS (Japanese Industrial Standard), MIL (U.S. MILitary Standard), EIAJ (Electronic Industries Association of Japan) and IEC (International Electrotechnical Commission). As indicated in ***Table 2***, however, Sharp has established its own testing method based on these standards.

Advances in semiconductor device technology are astonishing, and they call for higher quality and reliability standards. Improved failure analysis techniques are therefore necessary to ensure semiconductor device reliablity.

The causes of semiconductor device failure are becoming increasingly diverse. This diversity is the result of element and interconnect miniaturization required for higher integration. It is also due to an increasingly complex manufacturing process with an increased number of steps from the wafer fabrication process to the assembly process.

Failure analysis is the use of human, physical and electrical analytical procedures to clarify the failure mechanisms of defective parts. It is used to evaluate defective items appearing throughout the life of parts: during the semiconductor manufacturing process, outgoing inspections and reliability testing; during the user's incoming inspections, processing and reliability testing; and during operation in the field.

The ultimate goal of failure analysis is to prevent the recurrence of failure. It is necessary to establish various measures based on the results of failure analysis and to feed those measures back to the manufacturing process and product users.

Sharp has an on-going program of supplying users with our own quality data, reliability test data, etc., upon request. It is just one of Sharp's efforts to maintain a high degree of user service. ***Figure 5*** illustrates Sharp's Quality Information Routes.

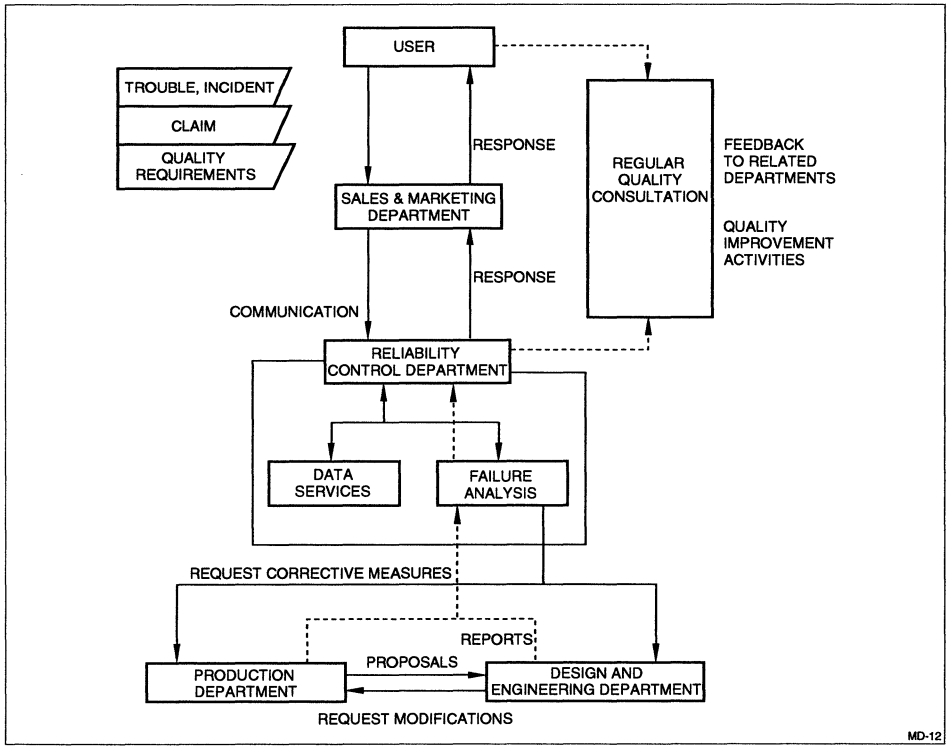


Figure 5. Routes Through Which Malfunctions Outside the Company are Handled.

Handling Precautions

All the semiconductor products listed in this data book are manufactured based on exacting designs and under comprehensive quality control. However, to take full advantage of the features offered and to assure each products' long-life service, please refer to the following items.

Maximum Ratings

It is generally known that the failure rate of semiconductor products increases as the temperature increases. It is therefore necessary that the ambient temperature be within the maximum rated temperature. Further, it is desirable from the stand-point of reliability that the ambient temperature be lowered as much as possible. The voltage, current, and electric power used are also factors that significantly influence the life of semiconductor products. Voltage or current that exceeds the rated level may damage the semiconductor product; even if applied only momentarily and the unit continues to operate properly, excessive voltage or current will likely increase the failure rate.

Therefore, in actual circuit design, it is important that the semiconductor products have an allowance with respect to the voltage, current and temperature conditions under which they will be used. The greater this allowance, the fewer the failures that will occur.

To keep failures to a minimum, the circuit should be designed so that under all conditions to absolute maximum, the ratings are not exceeded even momentarily and so that the maximum values for any two or more items are not achieved simultaneously. In addition, remember that the circuit functions of semiconductor products are guaranteed within the operating temperature range (Topr) or the absolute maximum ratings, but that storage temperature (Tstg) is the range in a non-operating condition.

Storage Precautions

General Storage Precautions

a. Storing product in the packing in which it is shipped is recommended. If transferred to a different container, use one that will not readily carry an electrostatic charge.

b. Store at conditions of normal temperature (5 - 35°C) and normal humidity (45 - 75% RH).

c. Avoid storing product in the presence of corrosive gases or dusty areas.

d. Avoid storing product in areas of direct sunlight or where sudden temperature changes will occur.

e. Avoid stacking product or otherwise applying heavy loads.

f. In the case of extended storage, take particular care against corrosion and deterioration in lead solderability. Inspecting such product before use is recommended.

Basic Electrostatic Discharge Countermeasures

Semiconductor device mounting requires exacting precautions to avoid applying excessive static electricity to the semiconductor. Item (a) - (c) below are basic electrostatic discharge countermeasures.

a. Use humidifiers and the like to ensure against excessively low relative humidity in the work environment. (Maintaining relative humidity consistently above 50% is ideal).

b. To prevent sudden electrostatic discharge, spread high-resistance electroconductive mats (about $10^6\Omega$) over workbenches and have workers wear wrist (ground) straps.

Have workers wear clothing made of charge-resistant cotton, noncharging materials (10^9 - 10^{14} Ω) or static electricity dissipating materials (10^5 - 10^9 Ω). Anti-static foot apparel is also effective.

c. Ionizers (ionized air blowers) are effective when it is difficult to discharge static electricity from mounting equipment, contacting dielectrics and semiconductors.

Sharp recommends using static electricity measuring devices to quantify electrostatic charges and develop effective countermeasures.

When forming the lead wires of semiconductor products to be mounted, forceps or a similar tool that will prevent stress from being applied to the base of the wires should be used.

To prevent the input terminals of semiconductor products on completed printed circuit boards from becoming open during storage or transport, the terminals of the circuit board should be shortcircuited or the entire circuit board itself should be wrapped in aluminium foil.

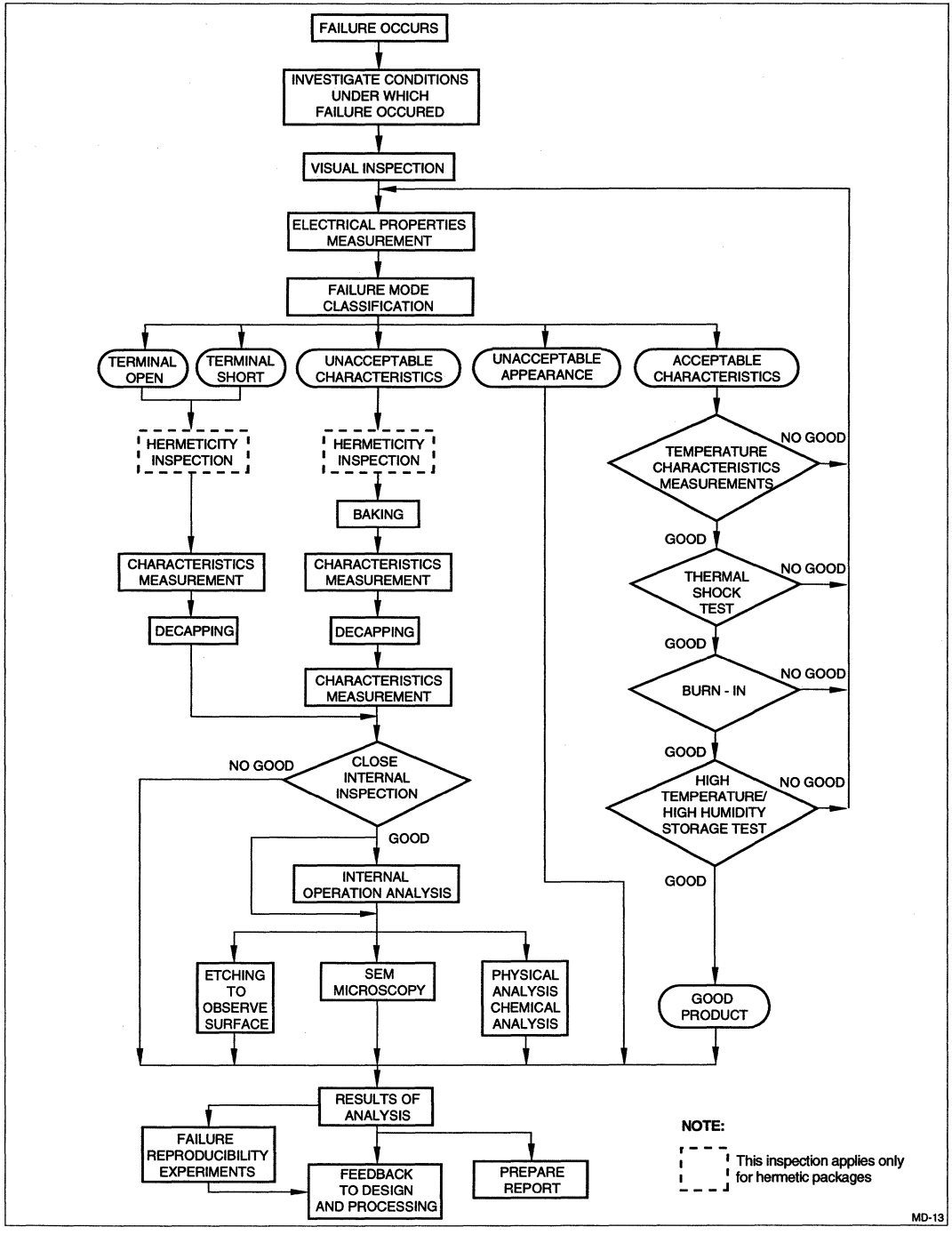


Figure 6. Failure Analysis Procedure

Soldering and Cleaning

When a semiconductor product is solder-bonded, specify the best conditions according to ***Table 4.*** If using a soldering iron, use one that doesn't leak from the soldering tip. An 'A Class' soldering iron with an insulation resistance of less than 10 MΩ is recommended. When using a solder bath, it should be grounded to prevent an unstable electric potential.

Using a strongly acidic or alkaline flux for soldering can cause corrosion of the lead wires. A rosin flux is ideal for this type of soldering.

To assure the reliability of a system, removal of the solder flux is generally required.

To prevent stress of semiconductor products and circuit boards when using ultrasonic cleaning, a cleaning method must be used that will shadow the main unit from the vibrator and specify the best conditions according to the following:

Table 3.
Recommended Conditions for PC Board Cleaning

Ultrasonic Power	less than 25 W/l
Cleaning Conditions	less than one minute total
Cleaning Solution Temperature	15 to 40°C

Adjustment and Tests

When the set is to be adjusted and tested upon completion of the printed circuit board, the printed circuit board must be checked to ensure that there are no solder bridges or cracks before the power is turned on. Also, if the market-rated voltage and current are to be used, it is wise to use a current limiter.

Whenever a printed circuit board is to be removed or mounted, or mounted on a socket, the power must be turned off.

When testing with a probe, care must be taken to assure that the probe does not come in contact with other signals or the power supply. If the test location has been decided beforehand, it is wise to set up a specially designed test-pin for testing.

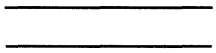
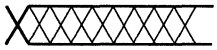
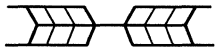
When testing in high and low temperatures, the constant-temperature bath must be grounded and measures taken to protect the set inside the bath from static electricity.

Table 4 outlines the semiconductor bonding and testing methods.

Table 4.
Semiconductor Bonding and Testing Methods

BONDING METHOD	TEMPERATURE AND TIME	TEST POSITION
Infrared reflow	Peak temp. 240°C or less 230°C or more within 15 sec. Heating speed: 1 to 4°C/sec.	Surface IC package
Flow dipping	245°C or less Within 3 sec./cycle Within 5 sec. in total	Solder bath
VPS	215°C or less 250°C or less, within 40 sec.	Steam
Hand soldering	260°C or less, within 10 sec.	IC outer lead

TIMING DIAGRAM CONVENTIONS

TIMING DIAGRAM	INPUT FUNCTIONS	OUTPUT FUNCTIONS
	HIGH or LOW	HIGH or LOW
	HIGH-to-LOW transitions allowed	HIGH-to-LOW transitions during designated interval
	LOW-to-HIGH transitions allowed	LOW-to-HIGH transitions during designated interval
	Don't care	State unknown or changing
	(Does not apply)	Centerline is high-impedance

MD-14

PSEUDO-STATIC RAMs

LH5P832

CMOS 256K (32K × 8) Pseudo-Static RAM

FEATURES

- 32,768 × 8 bit organization
- Access time: 100/120 ns (MAX.)
- Cycle time: 160/190 ns (MIN.)
- Power consumption:
  Operating: 357.5/303 mW
  Standby: 16.5 mW
- TTL compatible I/O
- 256 refresh cycle/4 ms
- Auto refresh is executed by internal counter (controlled by $\overline{OE}/\overline{RFSH}$ pin)
- Self refresh is executed by internal timer
- Single +5 V power supply
- Packages:
  28-pin, 600-mil DIP
  28-pin, 300-mil SK-DIP
  28-pin, 450-mil SOP

DESCRIPTION

The LH5P832 is a 256K bit Pseudo-Static RAM organized as 32,768 × 8 bits. It is fabricated using silicon-gate CMOS process technology.

The LH5P832 uses convenient on-chip refresh circuitry with a DRAM memory cell for pseudo static operation. This simplifies external clock inputs, while providing the same simple, non-multiplexed pinout as industry standard SRAMs. Moreover, due to the functional similarities between PSRAMs and SRAMs, many 32K × 8 SRAM sockets can be filled with the LH5P832 with little or no changes. The advantage is the cost savings realized with the lower cost PSRAM.

The LH5P832 PSRAM has the ability to fill the gap between DRAM and SRAM by offering low cost, low standby power, and a simple interface.

Three methods of refresh control are provided for maximum versatility. A 'CE-Only' refresh cycle refreshes the addressed row of memory cells transparently. All 256 rows must be refreshed or accessed every four milliseconds. 'Auto Refresh' automatically cycles through a different row on every OE/RFSH clock pulse, accomplishing the row refreshes without the need to supply row addresses externally. 'Self Refresh' further simplifies the refresh requirements by eliminating the need for address inputs and clock pulses entirely. An automatic timer senses time periods when memory accesses have ceased, and provides full refresh of all rows of memory without any external assistance.

PIN CONNECTIONS

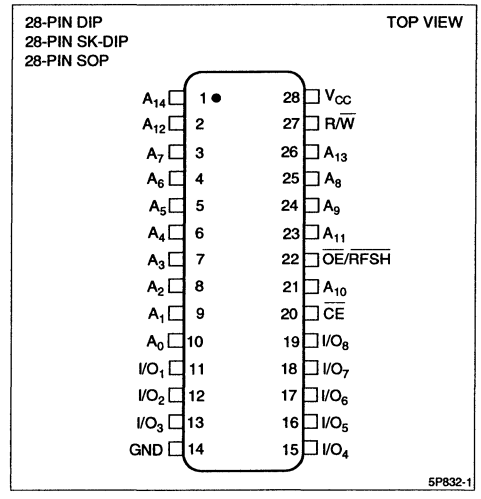


Figure 1. Pin Connections for DIP, SK-DIP, and SOP Packages

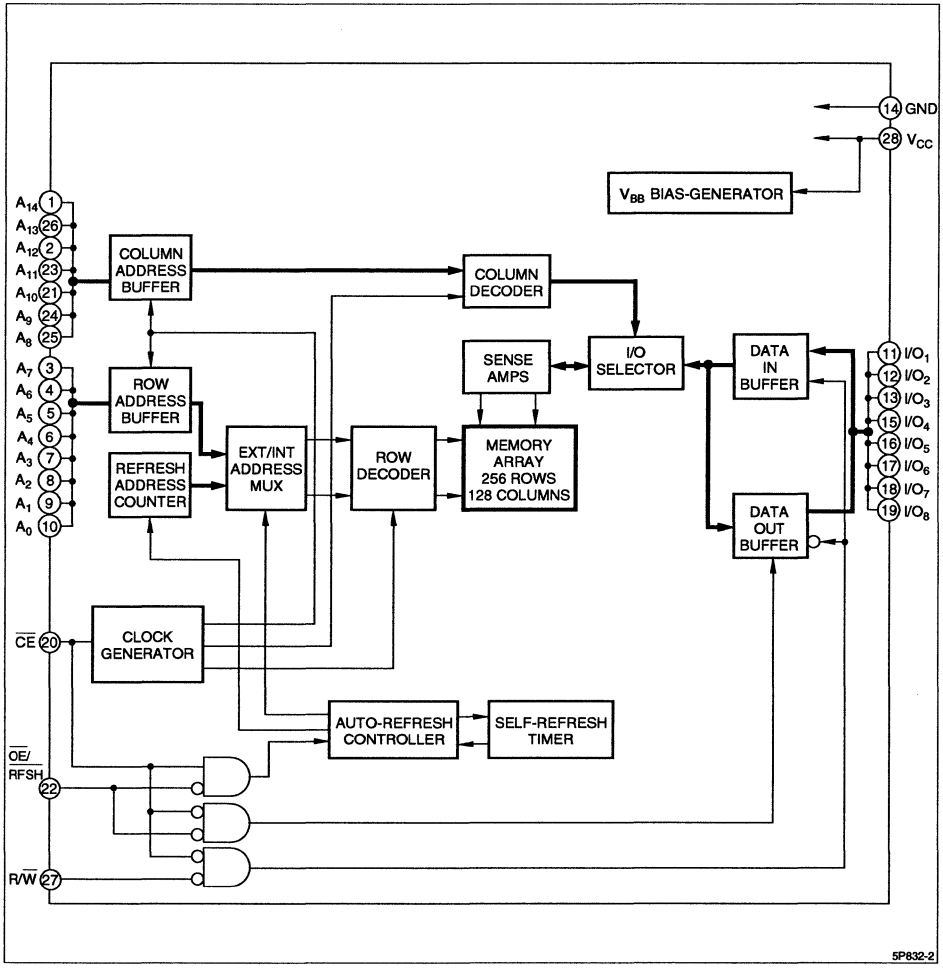


Figure 2. LH5P832 Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME
R/$\overline{W}$	Read/Write input
$\overline{OE}$/$\overline{RFSH}$	Output Enable/Refresh input
I/O_1 - I/O_8	Data inputs and outputs
A_0 - A_7	Row address inputs

SIGNAL	PIN NAME
A_8 - A_{14}	Column Address inputs
$\overline{CE}$	Chip Enable input
V_{CC}	Power supply
GND	Ground

TRUTH TABLE

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$/$\overline{RFSH}$	MODE	I/O_1 - I/O_8	I_{CC}	NOTE
L	L	X	Write	Data in	Operating (I_{CC})	1
L	H	L	Read	Data out	Operating (I_{CC})	
L	H	H	$\overline{CE}$-Only Refresh	High-Z	Operating (I_{CC})	
H	X	L	Auto Refresh	High-Z	Operating	1, 2
H	X	L	Self Refresh	High-Z	Standby	1, 3

NOTES:
1. X = H or L 2. $\overline{OE}$ Pulsewidth < 8 µs 3. $\overline{OE}$ Pulsewidth ≥ 8 µs

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Applied voltage on any pin	V_T	-1.0 to +7.0	V	1
Output short circuit current	I_O	50	mA	
Power consumption	P_D	600	mW	
Operating temperature	Topr	0 to +70	°C	
Storage temperature	Tstg	-65 to +150	°C	

NOTE:
1. Referenced to GND

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage	V_{IH}	2.4		V_{CC} + 0.3	V
	V_{IL}	-1.0		+0.8	V

CAPACITANCE (V_{CC} = 5.0 V ±10%, T_A = 0 to +70°C, f = 1MHz)

PARAMETER		SYMBOL	MIN.	MAX.	UNIT
Input capacitance	A_0 - A_{14}, R/$\overline{W}$	C_{IN1}		8	pF
	$\overline{CE}$, $\overline{OE}$/$\overline{RFSH}$	C_{IN2}		5	pF
Input/output capacitance	I/O_1 - I/O_8	C_{OUT1}		12	pF

DC CHARACTERISTICS (V_{CC} = 5 V ±10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	MAX.	UNIT	NOTE
Operating current	I_{CC1}	t_{RC} = 160 ns		65	mA	1
Operating current	I_{CC1}	t_{RC} = 190 ns		55	mA	1
Standby current	I_{CC2}	$\overline{CE}$ = V_{IH}, $\overline{OE}$/$\overline{RFSH}$ = V_{IH}		3	mA	1
Self refresh average current	I_{CC3}	$\overline{CE}$ = V_{IH}, $\overline{OE}$/$\overline{RFSH}$ = V_{IL}		3	mA	
CPU internal cycle average current	I_{CC4}	t_{RC} = 160 ns		65	mA	1, 2
CPU internal cycle average current	I_{CC4}	t_{RC} = 190 ns		55	mA	1, 2
Input leakage current	I_{LI}	0 V ≤ V_{IN} ≤ 6.5 V	-10	10	µA	
Output leakage current	I_{LO}	0 V ≤ V_{OUT} ≤ V_{CC} + 0.3 V	-10	10	µA	1
Output High voltage	V_{OH}	I_{OUT} = -1 mA	2.4		V	
Output Low voltage	V_{OL}	I_{OUT} = 4 mA		0.4	V	

NOTES:
1. The output pins are in high-impedance state.
2. I_{CC1} and I_{CC4} depend on the cycle time.

AC TEST CONDITIONS

PARAMETER	MODE
Input voltage amplitude	0.6 to 2.4 V
Input rise/fall time	5 ns
Timing reference level	1.5 V
Output load conditions	1TTL gate, C_L = 100 pF (Includes scope and jig capacitance)

AC CHARACTERISTICS

READ AND WRITE CYCLES [1,2] (V_{CC} = 5.0 V ±10%, T_A = 0 to 70°C)

PARAMETER	SYMBOL	160 ns		190 ns		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.		
Random read, write cycle time	t_{RC}	160		190		ns	
Read modify write cycle time	t_{RMW}	225		280		ns	
$\overline{CE}$ pulse width	t_{CE}	100	10,000	120	10,000	ns	
$\overline{CE}$ precharge time	t_P	50		60		ns	
Address setup time	t_{AS}	0		0		ns	
Address hold time	t_{AH}	20		30		ns	
Read command hold time	t_{RCH}	0		0		ns	
Read command setup time	t_{RCS}	0		0		ns	
$\overline{CE}$ access time	t_{CEA}		100		120	ns	3
$\overline{OE}$ access time	t_{OEA}		40		50	ns	3
$\overline{CE}$ to output in Low-Z	t_{CLZ}	10		10		ns	
$\overline{OE}$ to output in Low-Z	t_{OLZ}	0		0		ns	
Output enable from end of write	t_{WLZ}	0		0		ns	
Chip disable to output in High-Z	t_{CHZ}	0	30	0	35	ns	2
Output disable to output in High-Z	t_{OHZ}	0	30	0	35	ns	2
Write enable to output in High-Z	t_{WHZ}	0	30	0	35	ns	2
$\overline{OE}$ setup time	t_{OES}	10		10		ns	
$\overline{OE}$ hold time	t_{OEH}	0		0		ns	
$\overline{OE}$ lead time	t_{OEL}	10		10		ns	
Write command pulse width	t_{WCP}	60		85		ns	
Write command setup time	t_{WCS}	60		85		ns	
Write command hold time	t_{WCH}	60		85		ns	
Data setup time from write	t_{DSW}	40		50		ns	
Data setup time from $\overline{CE}$	t_{DSC}	40		50		ns	
Data hold time from write	t_{DHW}	0		0		ns	
Data hold time from $\overline{CE}$	t_{DHC}	0		0		ns	
Transition time (rise and fall)	t_T	3	35	3	35	ns	
Refresh time interval	t_{REF}		4		4	ms	

REFRESH CYCLE

Auto refresh cycle time	t_{FC}	160		190		ns	
Refresh delay time from $\overline{CE}$	t_{RFD}	50		60		ns	
Refresh pulse width (Auto refresh)	t_{FAP}	60	8,000	80	8,000	ns	
Refresh precharge time (Auto refresh)	t_{FP}	30		30		ns	
$\overline{CE}$ delay time from refresh active (Auto refresh)	t_{FCE}	190		225		ns	
Refresh pulse width (Self refresh)	t_{FAS}	8,000		8,000		ns	
$\overline{CE}$ delay time from refresh precharge (Self refresh)	t_{FRS}	190		225		ns	

NOTES:

1. At least 1 ms of pause time after power on should be given for proper device operation. $\overline{CE}$ and $\overline{OE}$/$\overline{RFSH}$ must be fixed at V_{IH} for 1 ms from the V_{DD} reached to the specified voltage level.
2. Active output to high-Z and high-Z to output active tests specified for a ±500 mV transition from steady state levels into the test load. C_{LOAD} = 5 pF.
3. Measured with a load circuit equivalent to 1TTL loads and 100 pF.

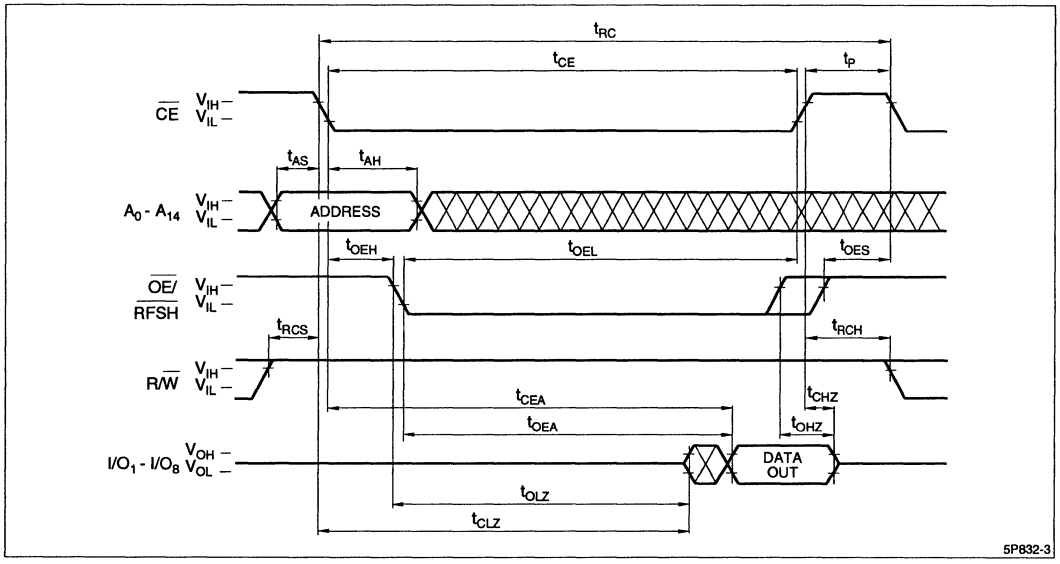


Figure 3. Read Cycle

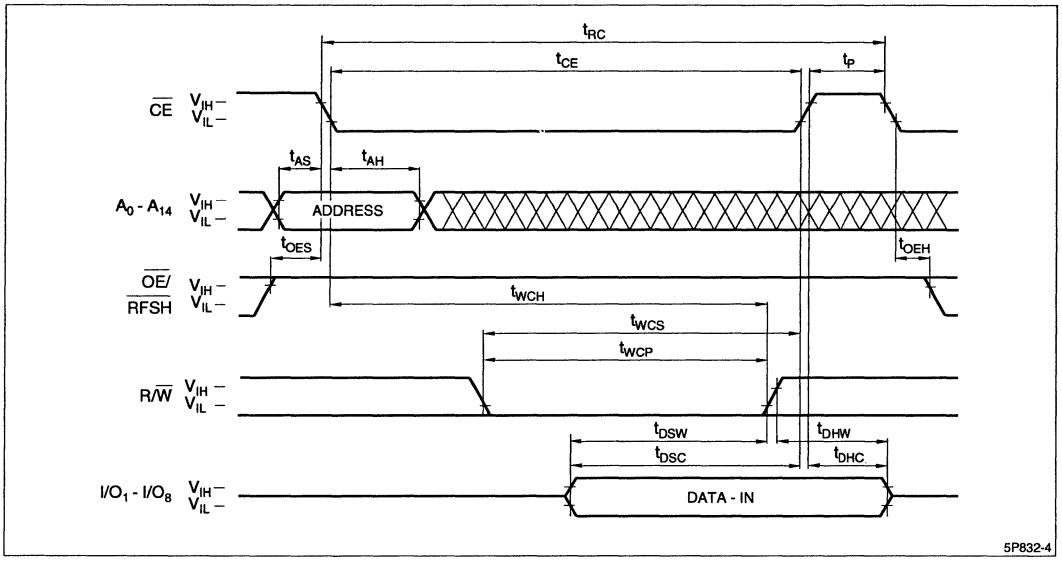


Figure 4. Write Cycle

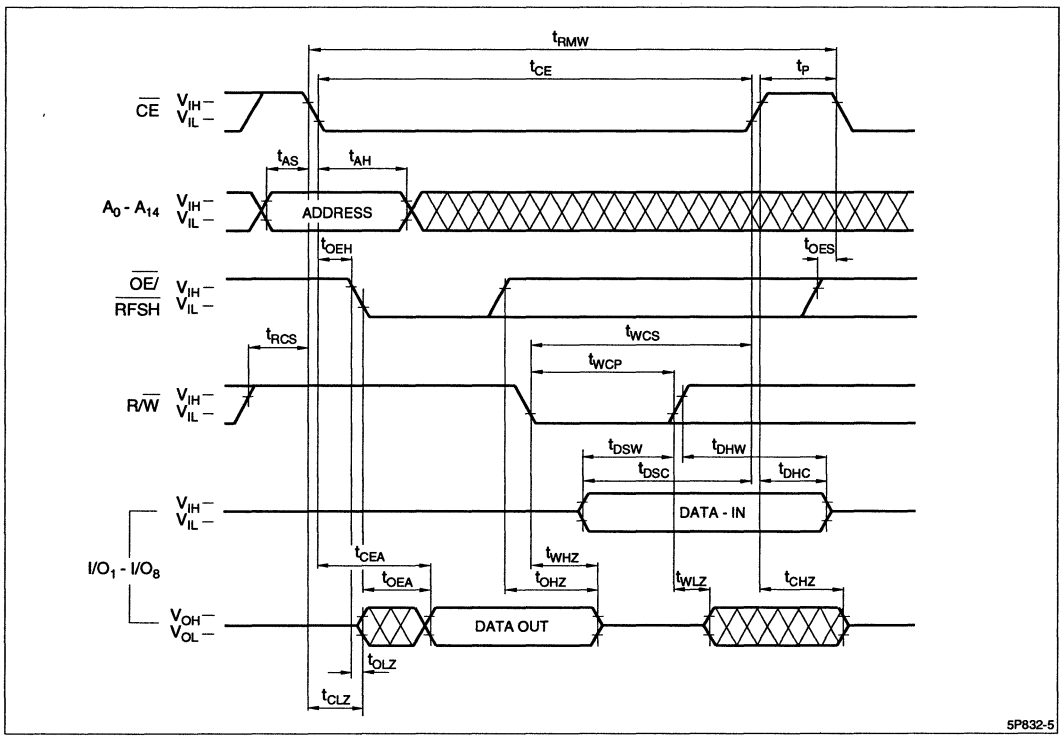


Figure 5. Read/Write Cycle

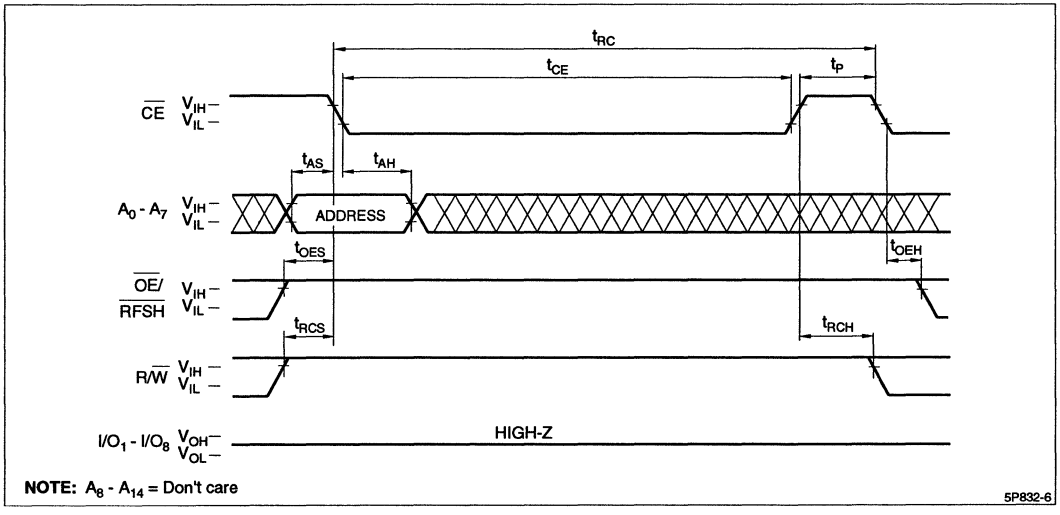


Figure 6. $\overline{CE}$ Only Refresh Cycle

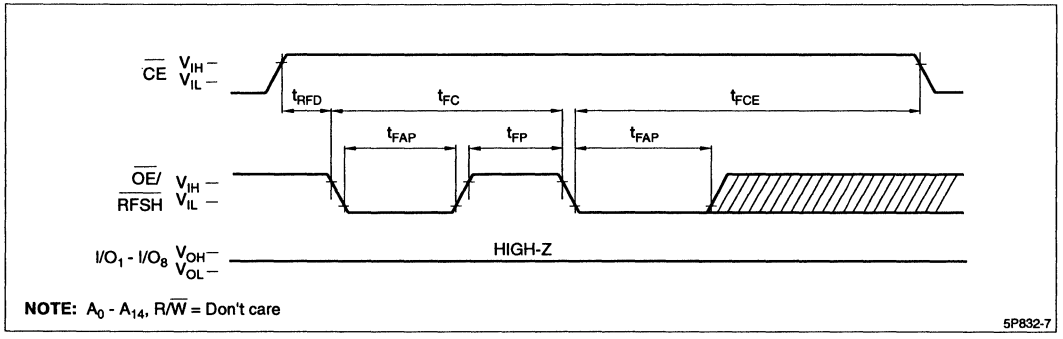


Figure 7. Auto Refresh Cycle

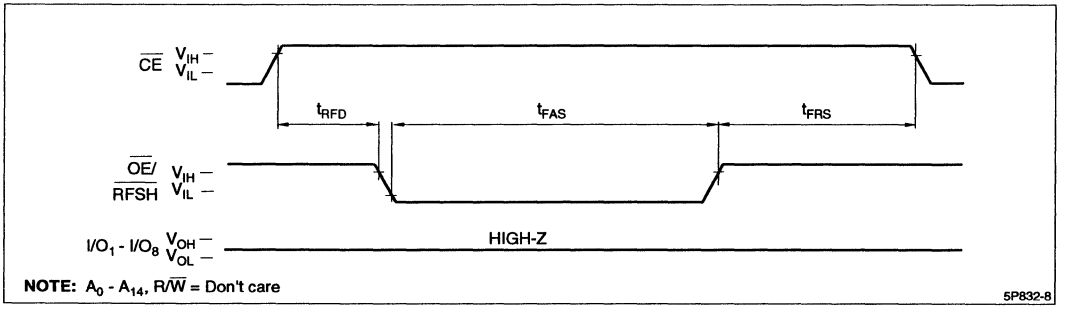
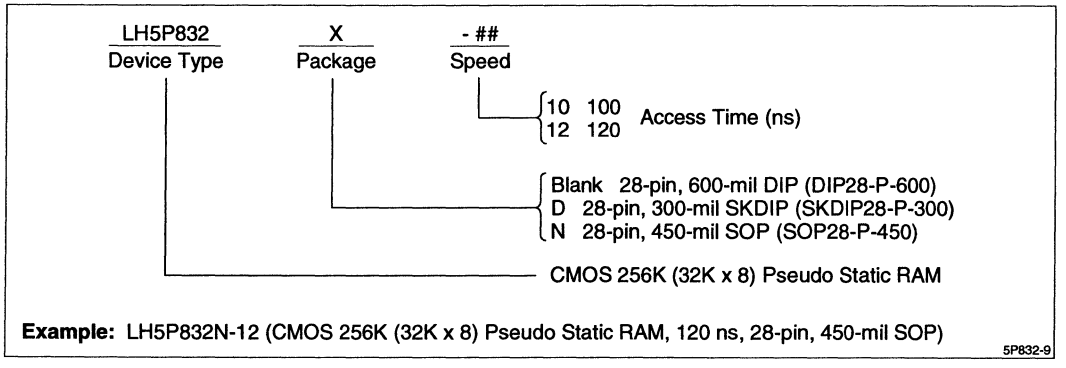


Figure 8. Self Refresh Cycle

ORDERING INFORMATION



LH5P864

CMOS 512K (64K × 8) Pseudo-Static RAM

FEATURES

- 65,536 × 8 bit organization
- Access time: 80 ns (MAX.)
- Cycle time: 140 ns (MIN.)
- Power supply:
  5 V ± 10%
- Power consumption: 440 mW (MAX.)
- Operating temperature:
  0 to 70°C
- TTL compatible I/O
- Average supply current in self refresh cycle: 1 mA
- 512 refresh cycles/8 ms (MAX.)
- Available for auto-refresh and self-refresh modes
- Package: 32-pin, 525-mil SOP

DESCRIPTION

The LH5P862 is a 512K-bit Pseudo-Static RAM organized as 65,536 × 8 bits. It is fabricated using silicon-gate CMOS process technology. With its built-in oscillator, it is easy to refresh memories without an external clock.

PIN CONNECTIONS

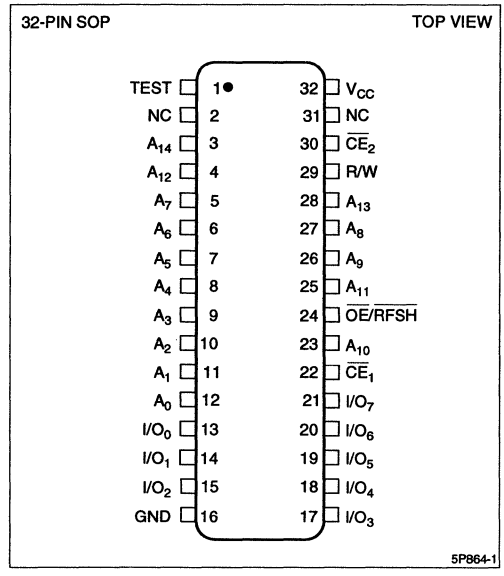


Figure 1. Pin Connections for SOP Package

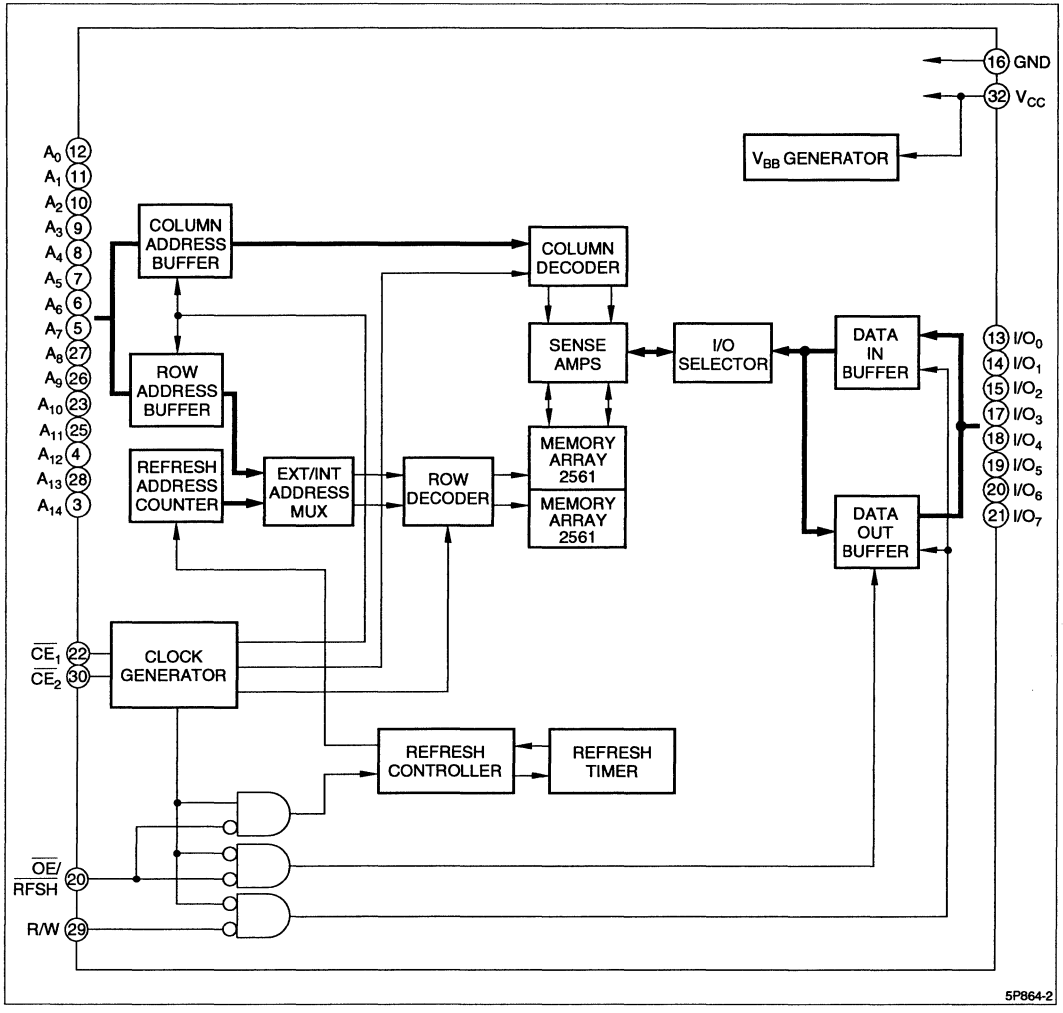


Figure 2. LH5P864 Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME
A_0 - A_{14}	Address input
R/W	Read/Write Enable input
$\overline{OE}/\overline{RFSH}$	Output Enable input/Refresh input
$\overline{CE}_1$, $\overline{CE}_2$	Chip Enable input
I/O_0 - I/O_7	Data input/output

SIGNAL	PIN NAME
V_{CC}	Power Supply
GND	Ground
Test	Test Input
NC	No Connection

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Applied voltage on any pin	V_T	-1.0 to +7.0	V	1
Output short circuit current	I_O	50	mA	
Operating temperature	Topr	0 to +70	°C	
Storage temperature	Tstg	-65 to +150	°C	

NOTE:
1. The maximum applicable voltage on any pin with respect to GND.

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	4.5	5.0	5.5	V
	GND	0	0	0	V
Input voltage	V_{IH}	2.4		V_{CC} + 0.5	V
	V_{IL}	-1.0		0.8	V

CAPACITANCE (T_A = 0 to +70°C, f = 1M, V_{CC} = 5.0 V ±10%)

PARAMETER	CONDITION	SYMBOL	MIN.	MAX.	UNIT
Input capacitance	A_0 - A_{14}	C_{IN1}		8	pF
	R/W, $\overline{OE}$/$\overline{RFSH}$	C_{IN2}		5	pF
	$\overline{CE}_1$, $\overline{CE}_2$	C_{IN3}		5	pF
Input/Output capacitance	I/O_0 - I/O_7	C_{OUT1}		10	pF

DC CHARACTERISTICS (T_A = 0 to +70°C, V_{CC} = 5.0 V ±10%)

PARAMETER	SYMBOL	CONDITIONS	MIN.	MAX.	UNIT	NOTE
Operating current	I_{CC1}	t_{RC} = t_{RC} (MIN.)		80	mA	1,2
Standby current	I_{CC2}			1.0	mA	1,3
Self refresh average current	I_{CC3}			1.0	mA	1,4
Input leakage current	I_{LI}	0 V ≤ V_{IN} ≤ 6.5 V, 0 V except on test pins	-10	10	µA	
Output leakage current	I_{LO}	0 V ≤ V_{OUT} ≤ V_{CC} + 0.3 V, Outputs in High-Z state	-10	10	µA	
Output HIGH voltage	V_{OH}	I_{OH} = -1.0 mA	2.4		V	
Output LOW voltage	V_{OL}	I_{OUT} = 4.0 mA		0.4	V	

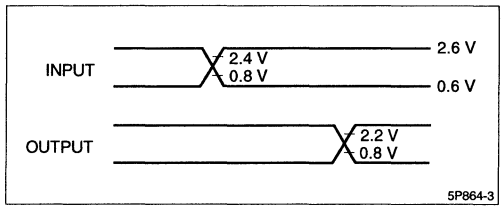
NOTES:
1. The output pins are in high-impedance state.
2. I_{CC1} depends on the cycle time.
3. $\overline{CE}_1$ = $\overline{CE}_2$ = V_{IH}, $\overline{OE}$/$\overline{RFSH}$ = V_{IH}
4. $\overline{CE}_1$ = $\overline{CE}_2$ = V_{IH}, $\overline{OE}$/$\overline{RFSH}$ = V_{IL}

AC CHARACTERISTICS [1,2,3] (T_A = 0 to +70°C, V_{CC} = 5.0 V ±10%)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT	NOTE
Random read, write cycle time	t_{RC}	140		ns	
Read modify write cycle time	t_{RMW}	205		ns	
$\overline{CE}$ pulse width	t_{CE}	80	10,000	ns	
$\overline{CE}$ precharge time	t_P	50		ns	
Address setup time	t_{AS}	0		ns	4
Address hold time	t_{AH}	20		ns	4
Read command setup time	t_{RCS}	0		ns	
Read command hold time	t_{RCH}	0		ns	
$\overline{CE}$ access time	t_{CEA}		80	ns	5
$\overline{OE}$ access time	t_{OEA}		30	ns	5
$\overline{CE}$ to output in Low-Z	t_{CLZ}	20		ns	
$\overline{OE}$ to output in Low-Z	t_{OLZ}	0		ns	
R/W to output in Low-Z	t_{WLZ}	0		ns	
Chip disable to output in High-Z	t_{CHZ}		25	ns	
Output disable to output in High-Z	t_{OHZ}		25	ns	
Write enable to output in High-Z	t_{WHZ}		25	ns	
$\overline{OE}$ setup time	t_{OES}	10		ns	
$\overline{OE}$ hold time	t_{OEH}	10		ns	
$\overline{OE}$ lead time	t_{OEL}	10		ns	
Write command pulse width	t_{WP}	30		ns	
Write command setup time	t_{WCS}	30		ns	
Write command hold time	t_{WCH}	50		ns	
Data setup time from write	t_{DSW}	30		ns	6
Data setup time from $\overline{CE}$	t_{DSC}	30		ns	6
Data hold time from write	t_{DHW}	0		ns	6
Data hold time from $\overline{CE}$	t_{DHC}	0		ns	6
Transition time (rise and fall)	t_T	3	35	ns	
Refresh time interval	t_{REF}		8	ms	
Auto refresh cycle time	t_{FC}	130		ns	
Refresh delay time from $\overline{CE}$	t_{RFD}	50		ns	
Refresh pulse width (Auto refresh)	t_{FAP}	30	8,000	ns	
Refresh precharge time (Auto refresh)	t_{FP}	30		ns	
$\overline{CE}$ delay time from refresh precharge (Auto refresh)	t_{FRS}	30		ns	
Refresh pulse width (Self refresh)	t_{FAS}	8,000		ns	
$\overline{CE}$ delay time from refresh precharge (Self refresh)	t_{FRS}	160		ns	

NOTES:

1. In order to initialize the circuit, $\overline{CE}_1$, $\overline{CE}_2$ and $\overline{OE}$/$\overline{RFSH}$ should be kept in V_{IH} for 100 µs after power-up and followed by at least 8 dummy cycles.
2. AC characteristics are measured at t_T = 5 ns.
3. AC characteristics are measured at the following condition (see figure at right):
4. Address is latched at the negative edge of $\overline{CE}_1$ or $\overline{CE}_2$.
5. Measured with a load equivalent to 2TTL + 100 pF.
6. Data is latched at the positive edge of R/W or at the positive edge of $\overline{CE}_1$ or $\overline{CE}_2$.



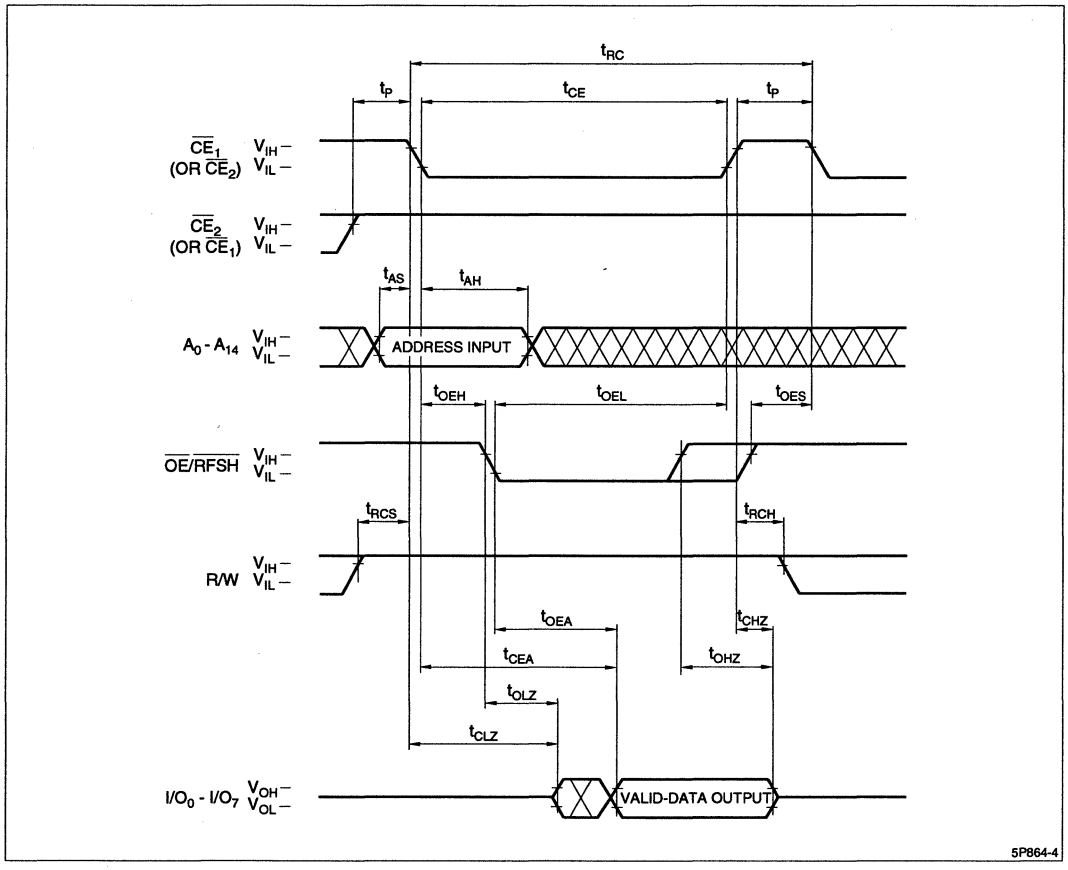


Figure 3. Read Cycle

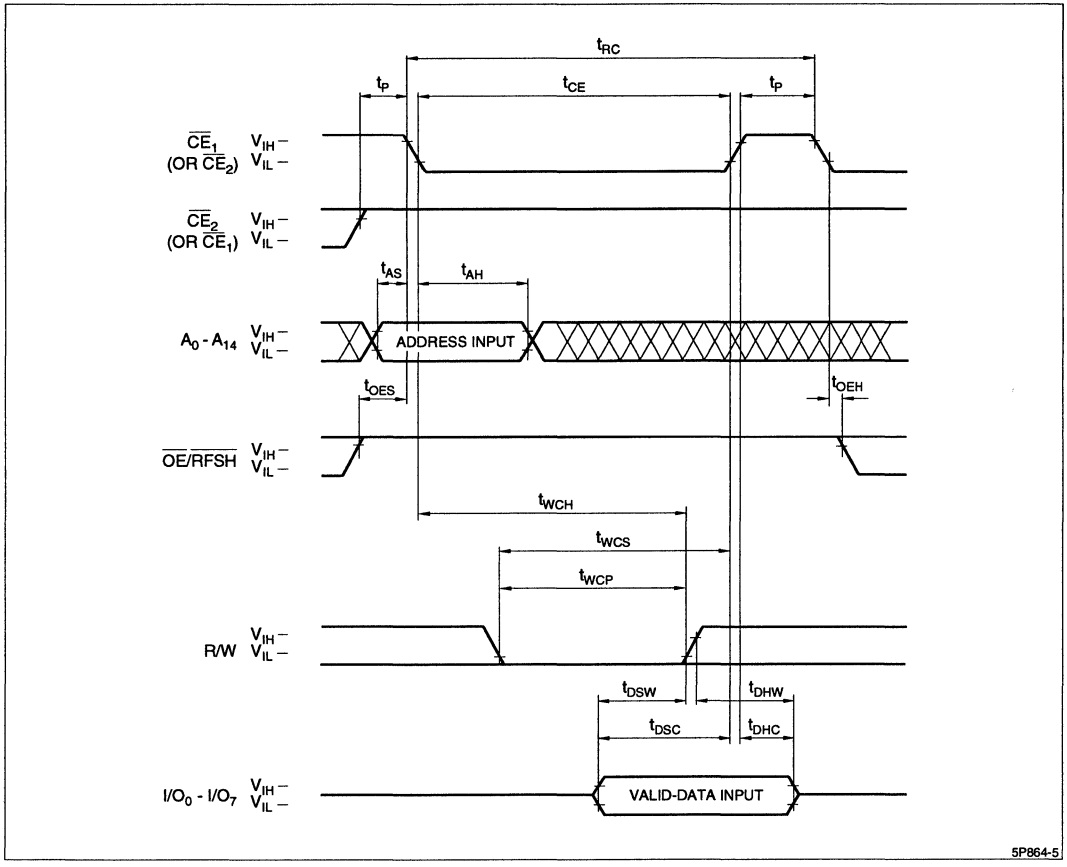


Figure 4. Write Cycle

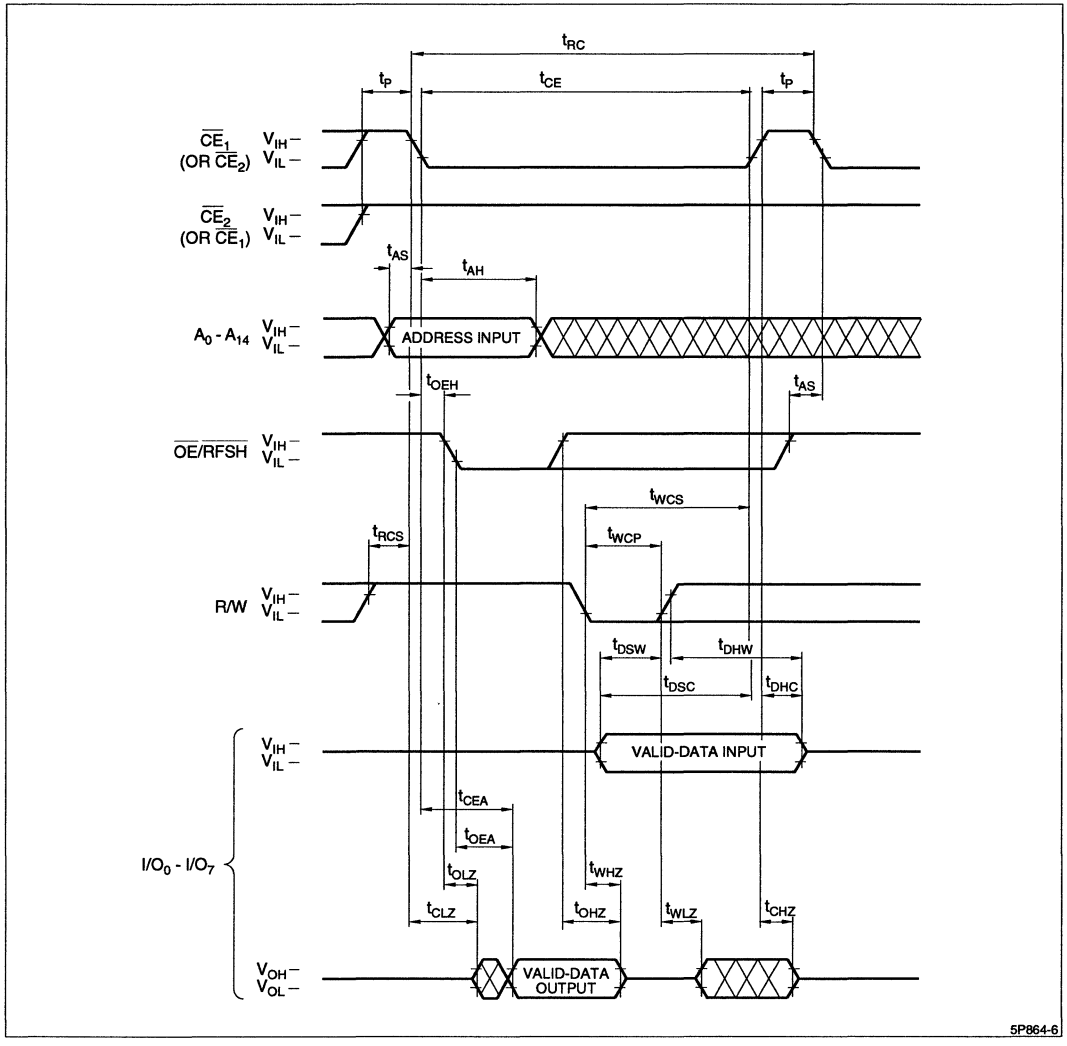


Figure 5. Read-Modify-Write Cycle

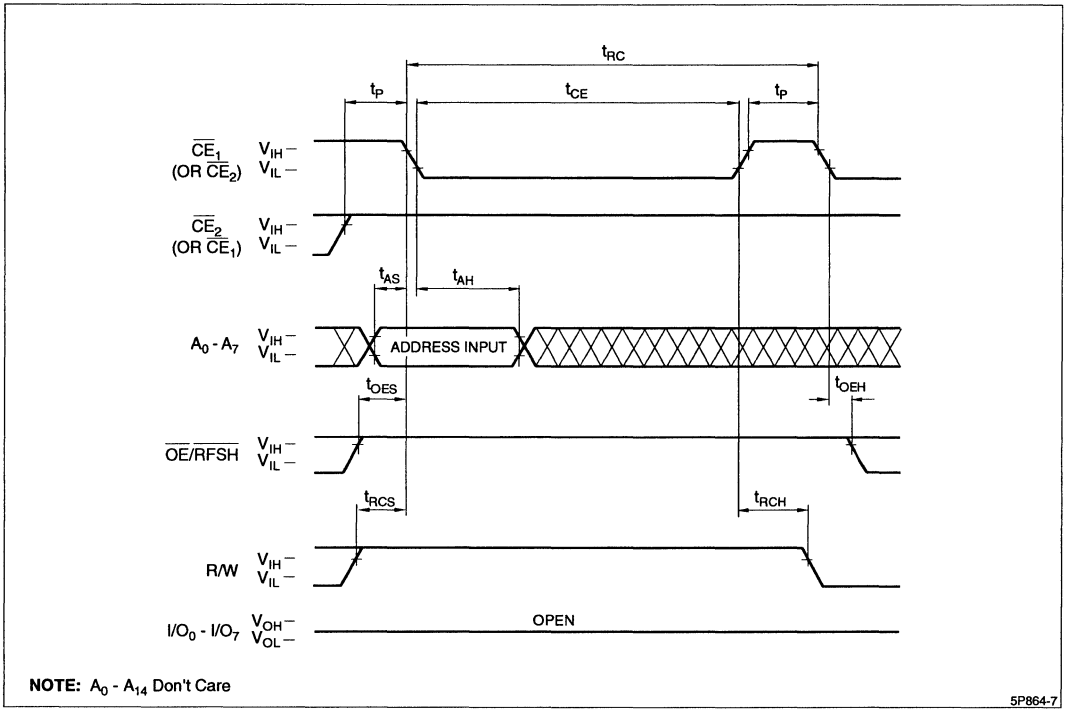


Figure 6. $\overline{CE}$ Only Refresh Cycle

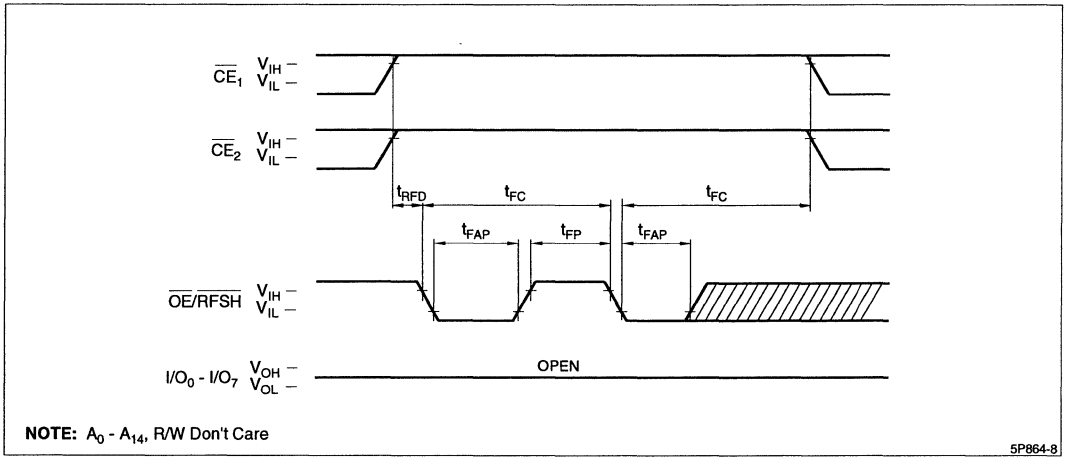


Figure 7. Auto Refresh Cycle

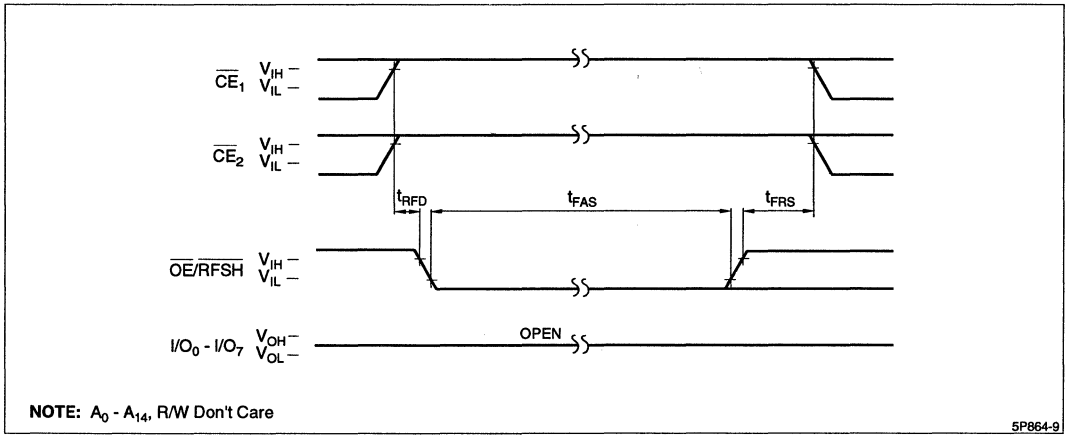
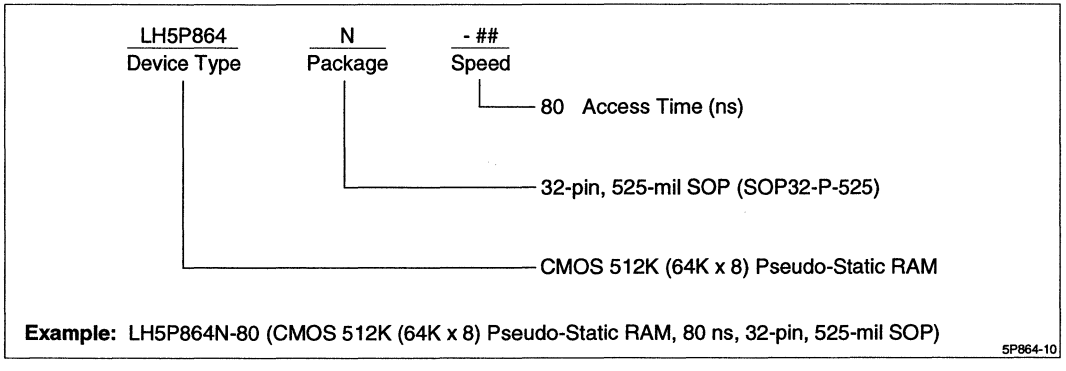


Figure 8. Self Refresh Cycle

ORDERING INFORMATION



LH5P8128

CMOS 1M (128K × 8) Pseudo-Static RAM

FEATURES

- 131,072 × 8 bit organization
- Access times (MAX.): 60/80/100 ns
- Cycle times (MIN.): 100/130/160 ns
- Power consumption:
  Operating: 572/440/358 mW (MAX.)
  Standby: 275 µW (MAX.) in self-refresh mode
- TTL compatible I/O
- Available for auto-refresh and self-refresh modes
- 512 refresh cycles/8 ms
- Compatible with JEDEC standard 1M SRAM pinout
- Packages:
  32-pin, 600-mil DIP
  32-pin, 525-mil SOP
  32-pin, 8 × 20 mm^2 TSOP (Type I)
  (normal and reverse bend pins)

DESCRIPTION

The LH5P8128 is a 1M bit Pseudo-Static RAM organized as 131,072 × 8 bits. It is fabricated using silicon-gate CMOS process technology.

A PSRAM uses on-chip refresh circuitry with a DRAM memory cell for pseudo static operation which eliminates external clock inputs, while having the same pinout as industry standard SRAMs. Moreover, due to the functional similarities between PSRAMs and SRAMs, existing 128K × 8 SRAM sockets can be filled with the LH5P8128 with little or no changes. The advantage is the cost savings realized with the lower cost PSRAM.

The LH5P8128 PSRAM has the ability to fill the gap between DRAM and SRAM by offering low cost, low power standby and a simple interface.

PIN CONNECTIONS

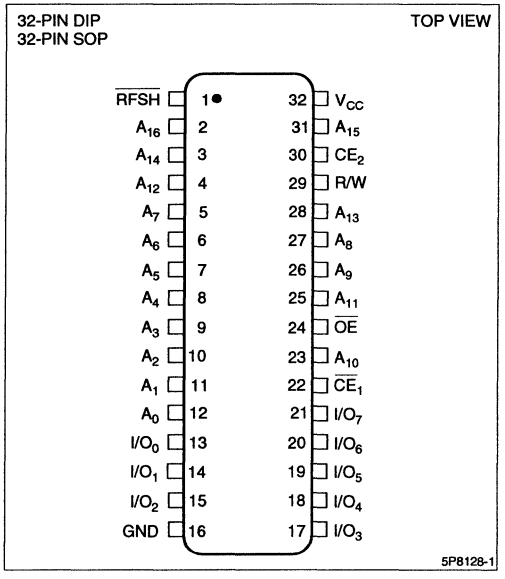


Figure 1. Pin Connections for DIP and SOP Packages

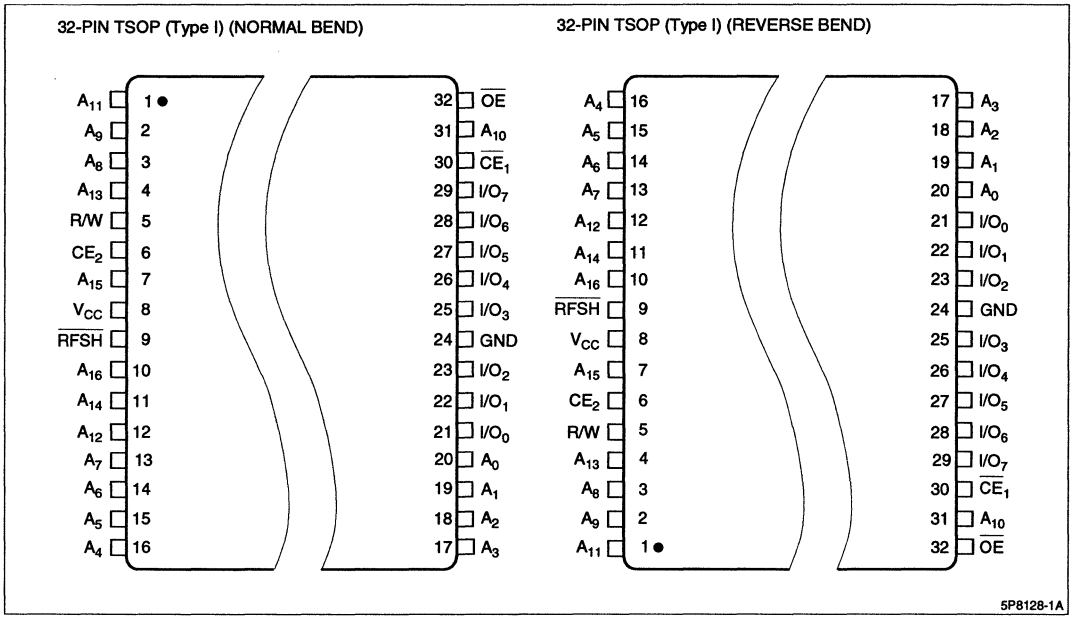


Figure 2. Pin Connections for TSOP Packages

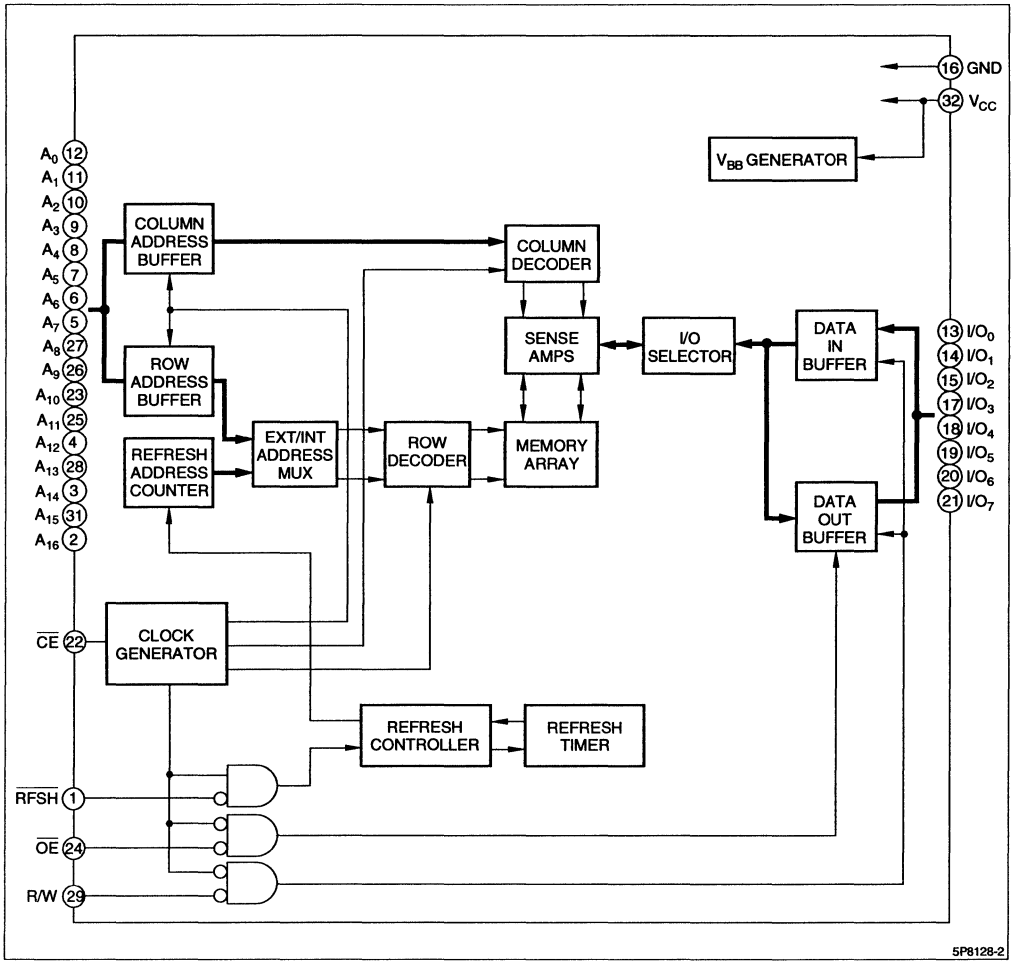


Figure 3. LH5P8128 Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME
A_0 - A_{16}	Address input
R/W	Read/Write input
$\overline{OE}$	Output Enable Input

SIGNAL	PIN NAME
$\overline{CE}_1$, CE_2	Chip Enable input
$\overline{RFSH}$	Refresh input
I/O_0 - I/O_7	Data input/output

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Applied voltage on any pins	V_T	-1.0 to +7.0	V	1
Operating temperature	Topr	0 to +70	°C	
Storage temperature	Tstg	-55 to +150	°C	
Output short circuit current	I_O	50	mA	
Power consumption	P_D	600	mW	

NOTE:
1. The maximum applicable voltage on any pin with respect to GND.

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	4.5	5.0	5.5	V
	GND	0	0	0	V
Input voltage	V_{IH}	2.4		V_{CC} + 0.3	V
	V_{IL}	-1.0		0.8	V

CAPACITANCE (T_A = 0 to +70°C, f = 1MHz, V_{CC} = 5.0 V ±10%)

PARAMETER		SYMBOL	MIN.	MAX.	UNIT
Input capacitance	A_0 - A_{16}	C_{IN1}		8	pF
	R/W, $\overline{OE}$	C_{IN2}		5	pF
	$\overline{CE}_1$, CE_2	C_{IN3}		5	pF
	$\overline{RFSH}$	C_{IN4}		5	pF
Input/output capacitance	I/O_0 - I/O_7	C_{OUT1}		10	pF

DC CHARACTERISTICS (T_A = 0 to +70°C, V_{CC} = 5.0 V ±10%)

PARAMETER		SYMBOL	CONDITIONS	MIN.	MAX.	UNIT	NOTE
Operating current	LH5P8128-60	I_{CC1}	t_{RC} = t_{RC} (MIN)		104	mA	1, 2
	LH5P8128-80				80		
	LH5P8128-10				65		
Standby current	TTL Input	I_{CC2}			1	mA	1, 3
	CMOS Input				0.05		1, 4
Self-refresh average current	TTL Input	I_{CC3}			1	mA	1, 5
	CMOS Input				0.05		1, 6
CPU internal cycle average current	LH5P8128-60	I_{CC4}	(R/W = $\overline{OE}$ = V_{IH})		104	mA	1, 2
	LH5P8128-80				80		
	LH5P8128-10				65		
Input leakage current		I_{LI}	0 V ≤ V_{IN} ≤ 6.5 V 0 V on all other test pins	-10	10	µA	
I/O leakage current		I_{LO}	0 V ≤ V_{OUT} ≤ V_{CC} + 0.3 V Output in high-impedance state	-10	10	µA	
Output HIGH voltage		V_{OH}	I_{OUT} = 1 mA	2.4		V	
Output LOW voltage		V_{OL}	I_{OUT} = 4 mA		0.4	V	

NOTES:

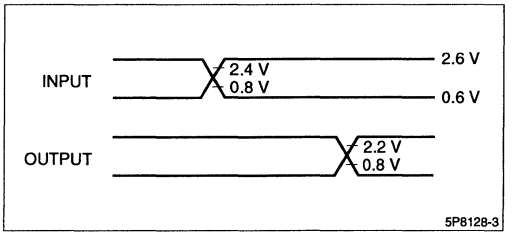
1. The output pins are in high-impedance state
2. I_{CC1} and I_{CC4} depend on the cycle time
3. $\overline{CE}_1$ = V_{IH}, $\overline{RFSH}$ = V_{IH}
4. $\overline{CE}_1$ = V_{CC} - 0.2 V, $\overline{RFSH}$ = V_{CC} - 0.2 V
5. $\overline{CE}_1$ = V_{IH}, $\overline{RFSH}$ = V_{IL}
6. $\overline{CE}_1$ = V_{CC} - 0.2 V, $\overline{RFSH}$ = 0.2 V

AC ELECTRICAL CHARACTERISTICS [1,2,3] (T_A = 0 to +70°C, V_{CC} = 5.0 V ±10%)

PARAMETER	SYMBOL	LH5P8128-60		LH5P8128-80		LH5P8128-10		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Random read, write cycle time	t_{RC}	100		130		160		ns	
Read modify write cycle time	t_{RMW}	155		195		235		ns	
$\overline{CE}$ pulse width	t_{CE}	60	10,000	80	10,000	100	10,000	ns	
$\overline{CE}$ precharge time	t_P	30		40		50		ns	
Address setup time	t_{AS}	0		0		0		ns	4
Address hold time	t_{AH}	15		20		25		ns	4
Read command setup time	t_{RCS}	0		0		0		ns	
Read command hold time	t_{RCH}	0		0		0		ns	
$\overline{CE}$ access time	t_{CEA}		60		80		100	ns	5
$\overline{OE}$ access time	t_{OEA}		25		30		35	ns	5
$\overline{CE}$ to output in Low-Z	t_{CLZ}	20		20		20		ns	
$\overline{OE}$ to output in Low-Z	t_{OLZ}	0		0		0		ns	
Output enable from end of write	t_{WLZ}	0		0		0		ns	
Chip disable to output in High-Z	t_{CHZ}		20		25		30	ns	
Output disable to output in High-Z	t_{OHZ}		20		25		30	ns	
Write enable to output in High-Z	t_{WHZ}		20		25		30	ns	
$\overline{OE}$ setup time	t_{OES}	0		0		0		ns	
$\overline{OE}$ hold time	t_{OEH}	10		10		10		ns	
Write command pulse width	t_{WP}	30		30		30		ns	
Write command setup time	t_{WCS}	30		30		30		ns	
Write command hold time	t_{WCH}	40		50		60		ns	
Data setup time from write	t_{DSW}	25		30		35		ns	6
Data setup time from $\overline{CE}$	t_{DSC}	25		30		35		ns	6
Data hold time from write	t_{DHW}	0		0		0		ns	6
Data hold time from $\overline{CE}$	t_{DHC}	0		0		0		ns	6
Transition time (rise and fall)	t_T	3	35	3	35	3	35	ns	
Refresh time interval	t_{REF}		8		8		8	ms	
Refresh command hold time	t_{RHC}	15		15		15		ns	
Auto refresh cycle time	t_{FC}	100		130		160		ns	
Refresh delay time from $\overline{CE}$	t_{RFD}	30		40		50		ns	
Refresh pulse width (Auto refresh)	t_{FAP}	30	8,000	30	8,000	30	8,000	ns	
Refresh precharge time (Auto refresh)	t_{FP}	30		30		30		ns	
Refresh pulse width (Self refresh)	t_{FAS}	8,000		8,000		8,000		ns	
$\overline{CE}$ delay time from refresh precharge (Self refresh)	t_{FRS}	140		160		190		ns	

NOTES:

1. In order to initialize the circuit, $\overline{CE}_1$ should be kept at V_{IH} or CE_2 should be kept at V_{IL} for 100 µs after power-up.
2. AC characteristics are measured at t_T = 5 ns.
3. AC characteristics are measured at the following condition (see figure at right).
4. Address is latched at the negative edge of $\overline{CE}_1$ or at the positive edge of CE_2.
5. Measured with a load equivalent to 2TTL + 100 pF.
6. Data is latched at the positive edge of W/R or at the positive edge of $\overline{CE}_1$ or at the negative edge of CE_2.



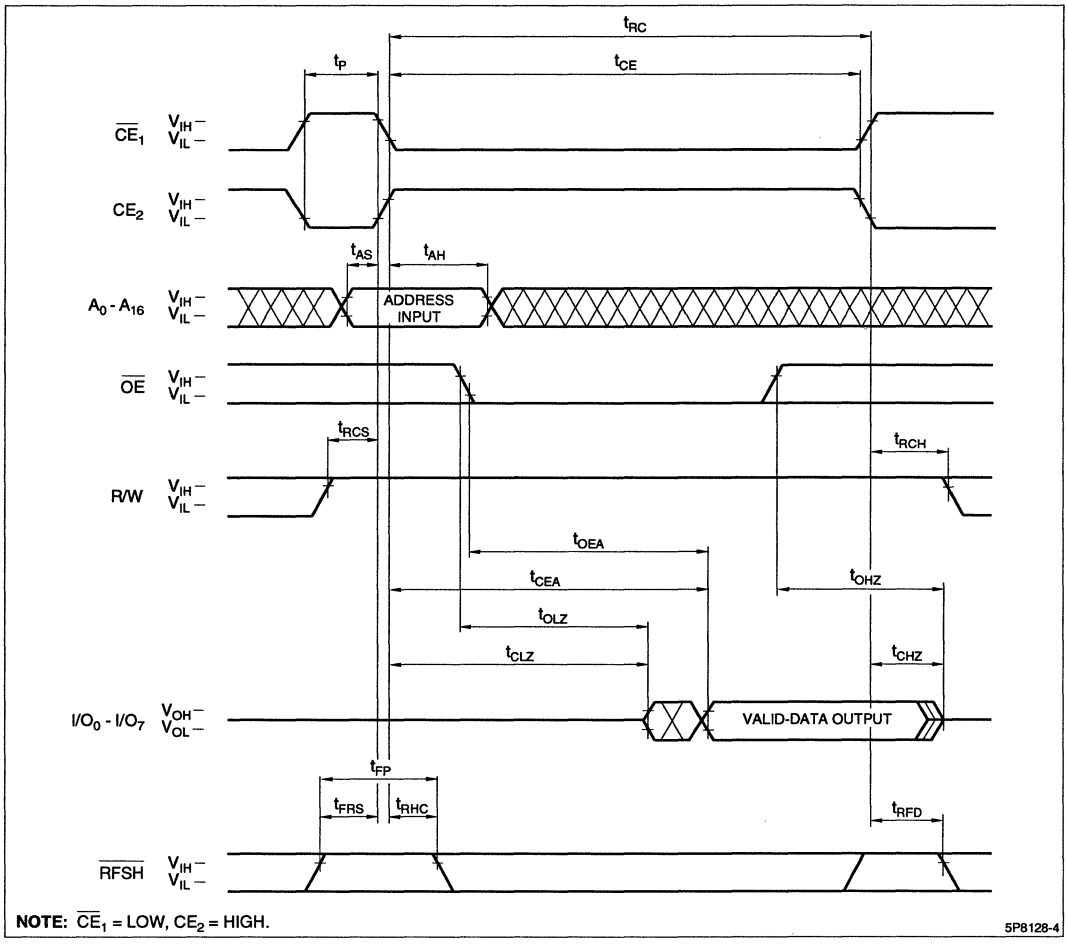


Figure 4. Read Cycle

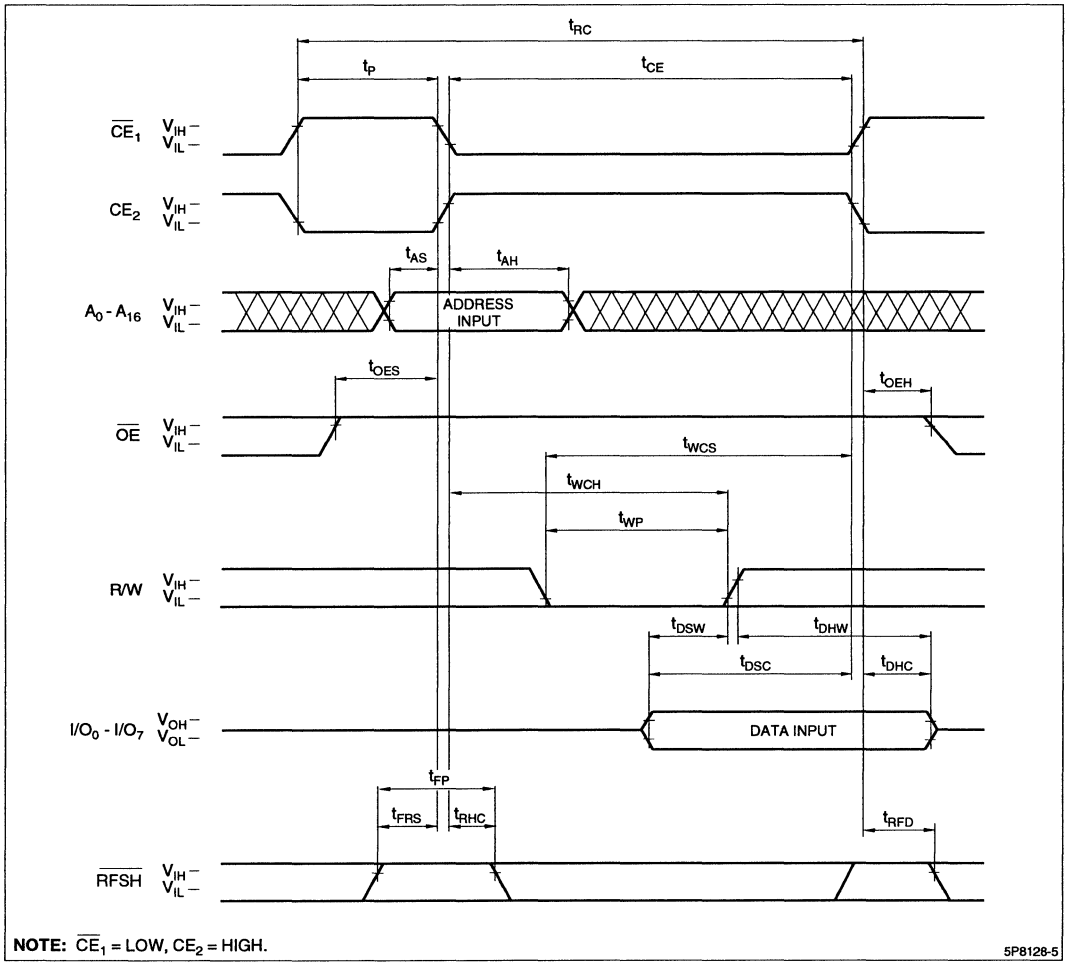


Figure 5. Write Cycle 1 ($\overline{OE}$ = HIGH)

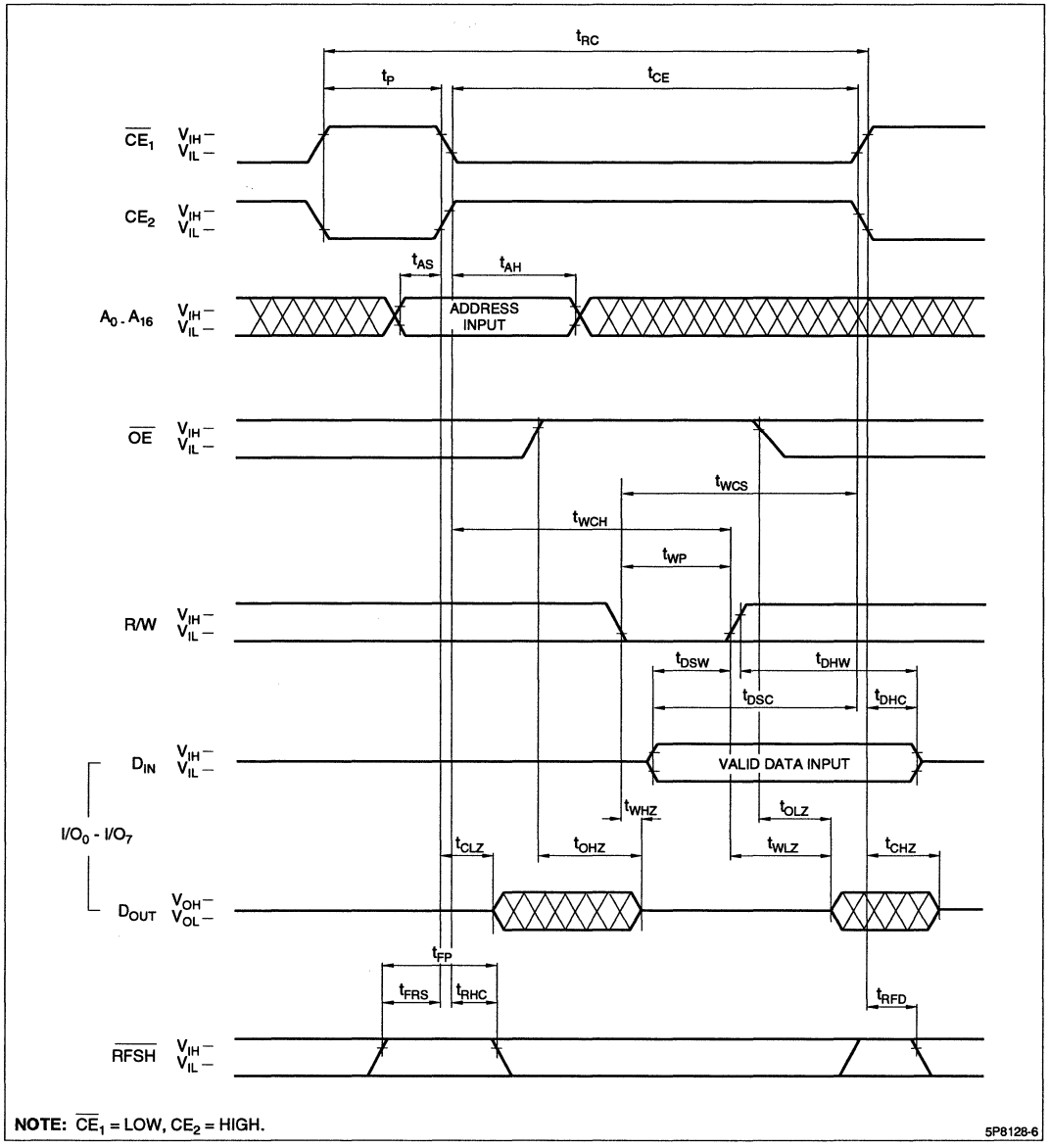


Figure 6. Write Cycle 2 ($\overline{OE}$ Clock)

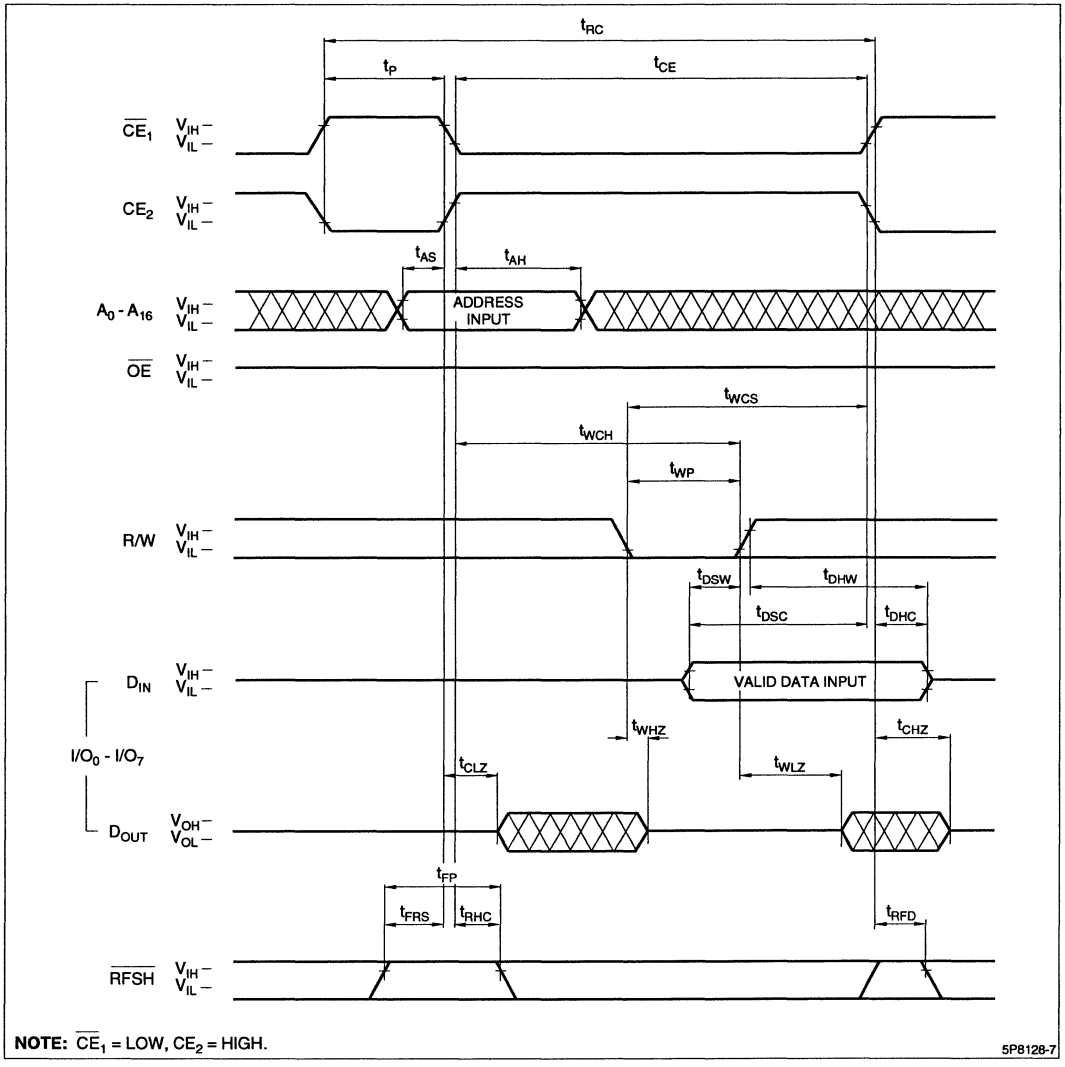


Figure 7. Write Cycle 3 ($\overline{OE}$ = LOW)

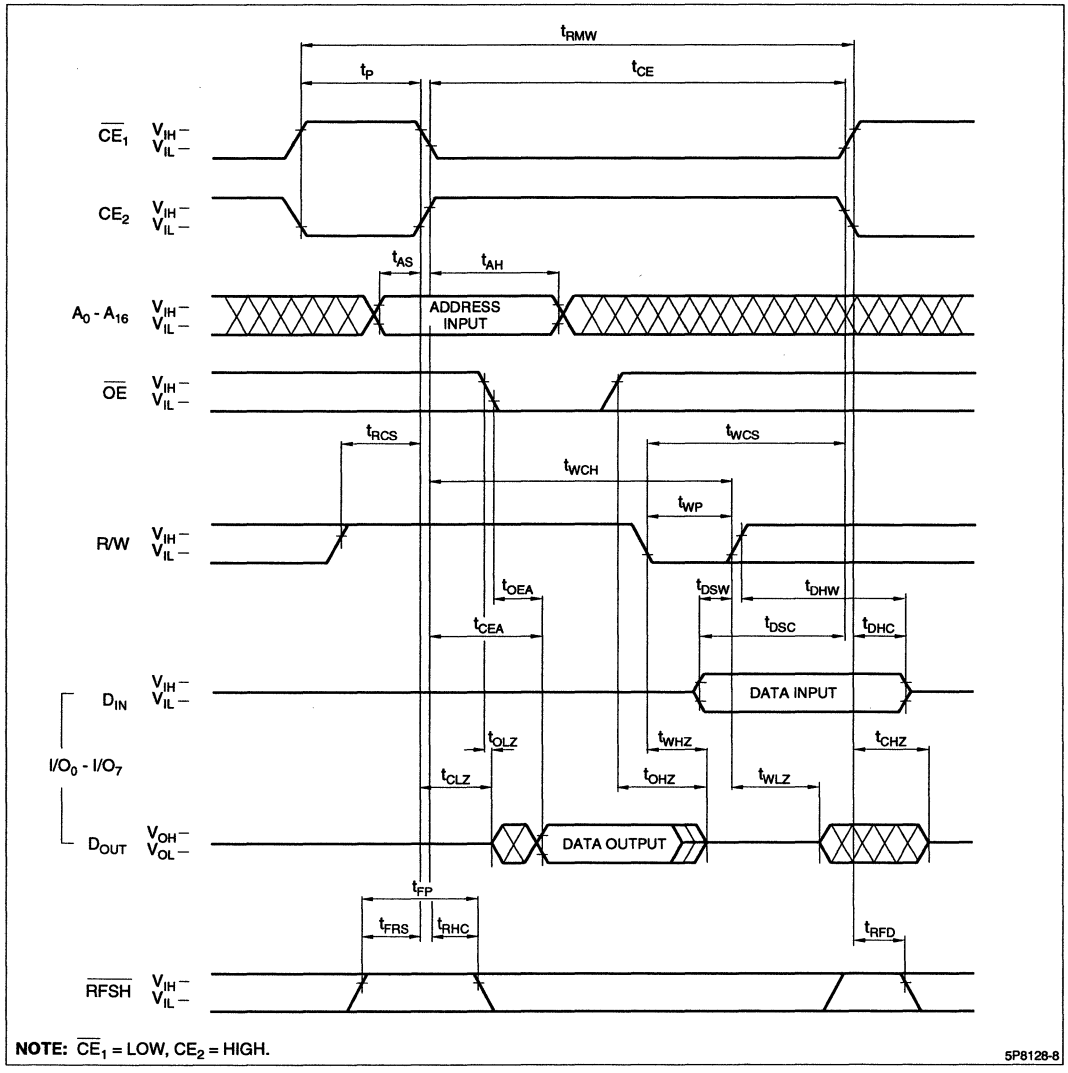


Figure 8. Read-Modify-Write Cycle

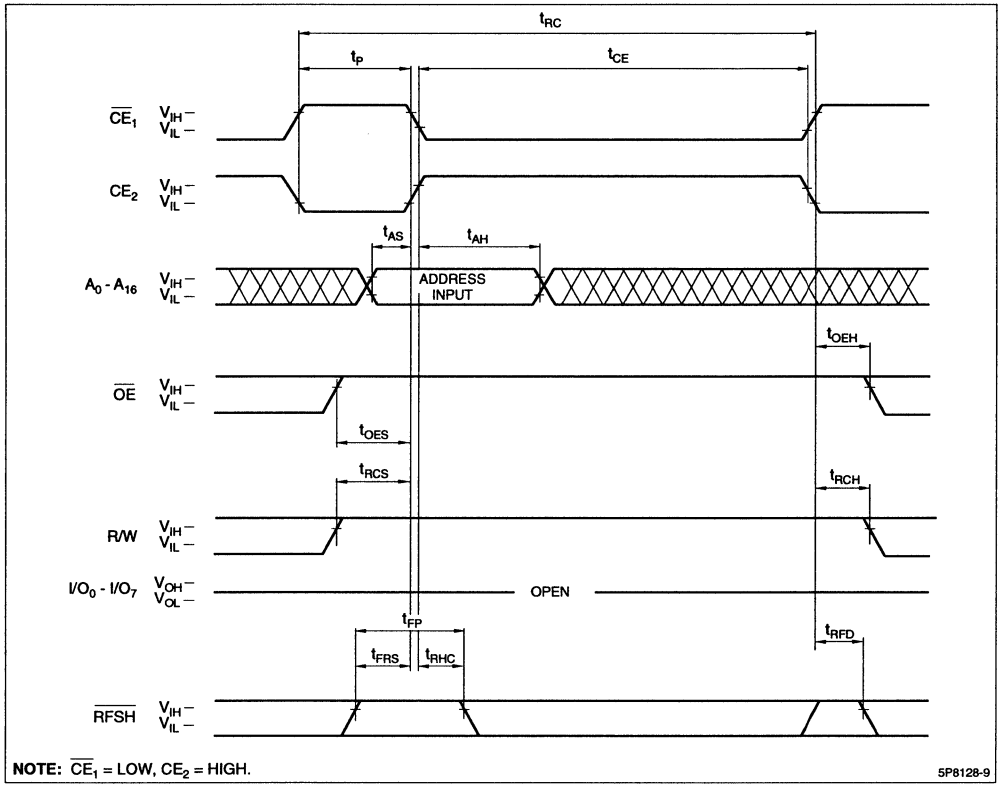


Figure 9. $\overline{CE}$ Only Refresh

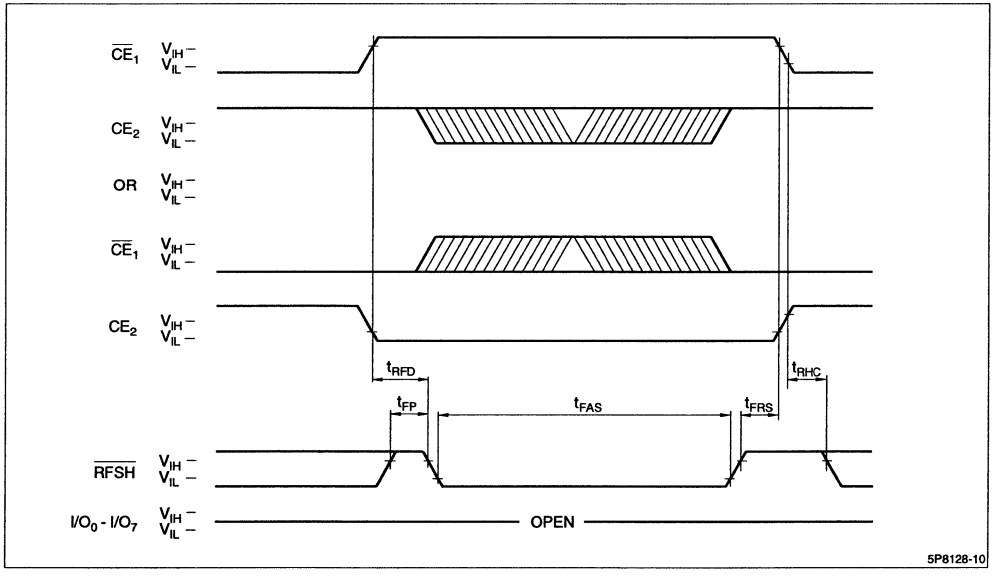


Figure 10. Self Refresh Cycle

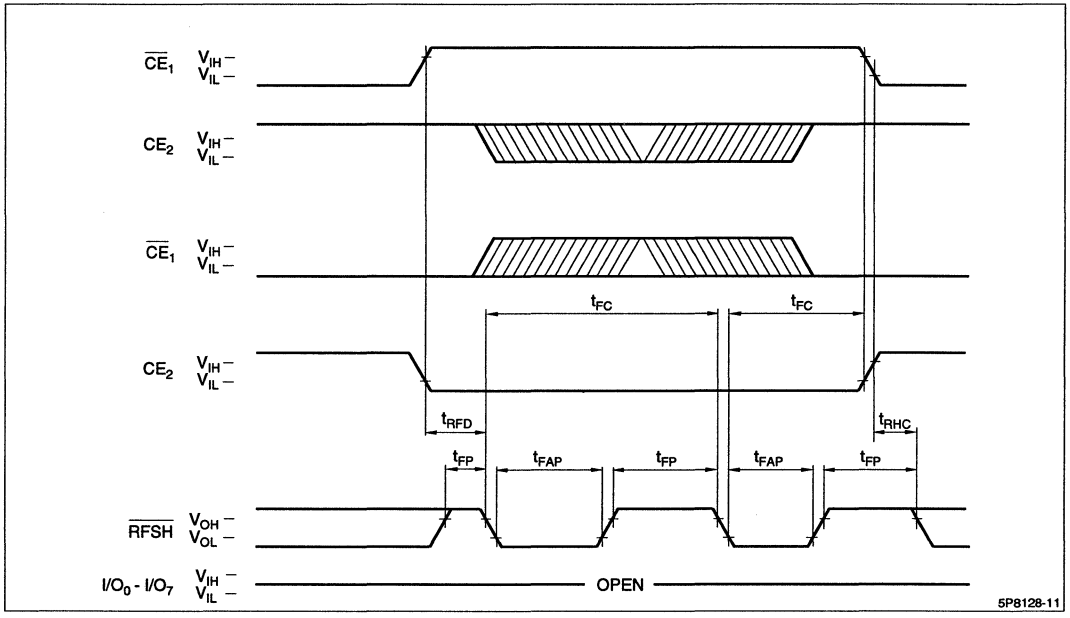
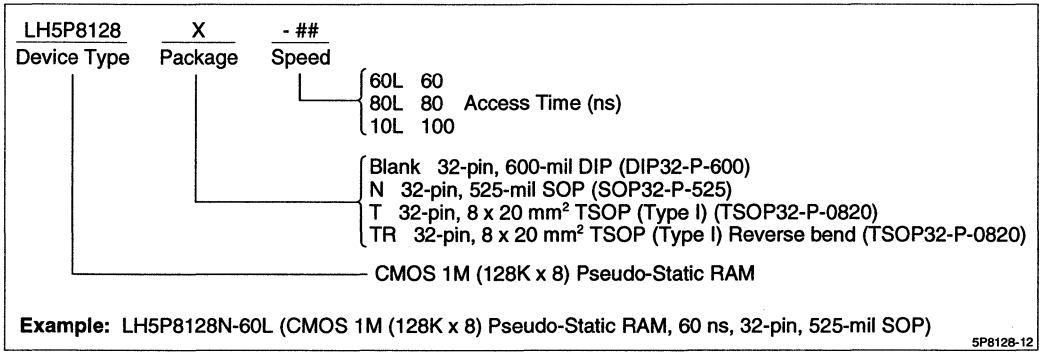


Figure 11. Auto Refresh Cycle

ORDERING INFORMATION



LH5P8129

CMOS 1M (128K × 8)
CS-Control Pseudo-Static RAM

FEATURES

- 131,072 × 8 bit organization
- Access times (MAX.): 60/80/100 ns
- Cycle times (MIN.): 100/130/160 ns
- Power supply: +5 V ±10%
- Pin compatible with 1M standard SRAM
- Power consumption:
  Operating: 572/385/358 mW (MAX.)
  Standby (TTL level): 5.5 mW (MAX.)
  Standby (CMOS level): 0.55 mW (MAX.)
- TTL compatible I/O
- Available for auto-refresh and self-refresh modes
- 512 refresh cycles/8 ms
- Packages:
  32-pin, 600-mil DIP
  32-pin, 525-mil SOP
  32-pin, 8 × 20 mm^2 TSOP (Type I)
  (normal and reverse bend pins)

DESCRIPTION

The LH5P8129 is a 1M bit Pseudo-Static RAM organized as 131,072 × 8 bits. It is fabricated using silicon-gate CMOS process technology.

A PSRAM uses on-chip refresh circuitry with a DRAM memory cell for pseudo static operation which eliminates external clock inputs, while considering the pinout compatibility with industry standard SRAMs. The advantage is the cost savings realized with the lower cost PSRAM.

The LH5P8129 PSRAM has a built-in oscillator, which makes it easy to refresh memories without external clocks.

PIN CONNECTIONS

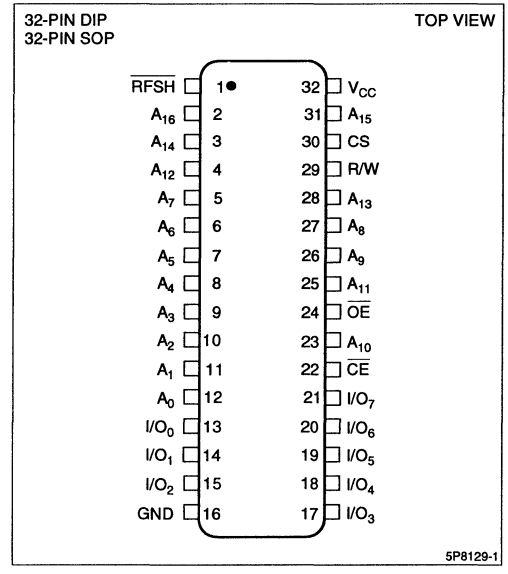


Figure 1. Pin Connections for DIP and SOP Packages

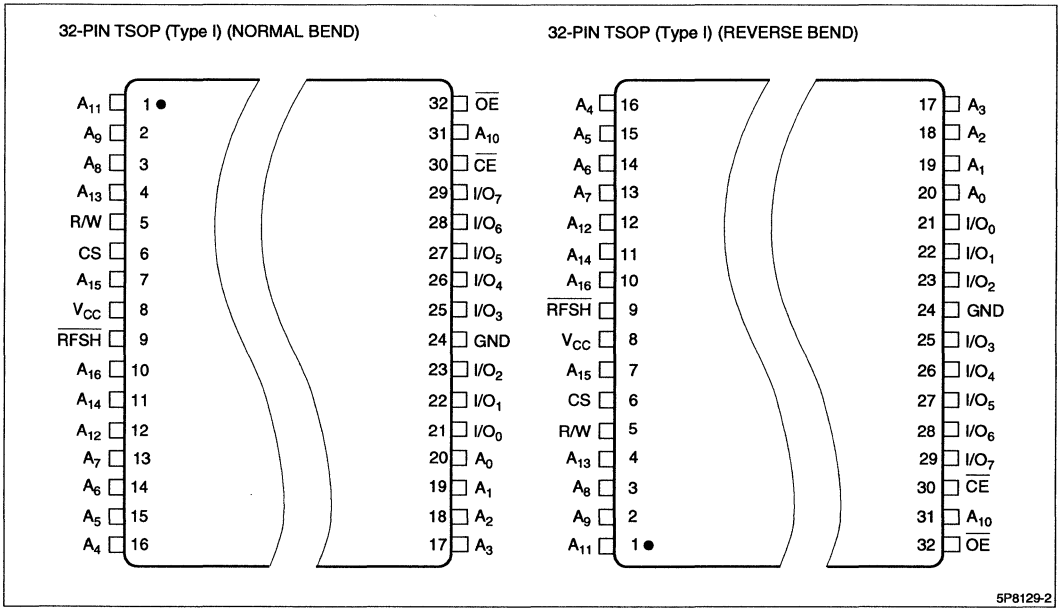


Figure 2. Pin Connections for TSOP Packages

TRUTH TABLE

$\overline{CE}$	CS	$\overline{OE}$	R/W	$\overline{RFSH}$	A_0 - A_{16}	I/O_1 - I/O_8	MODE
L	H	L	H	H	VX	D_{OUT}	Read
L	H	X	L	H	VX	D_{IN}	Write
L	H	H	H	H	VY	High-Z	$\overline{CE}$ only refresh
L	L	X	X	X	X	High-Z	CS standby
H	X	X	X	L	X	High-Z	Auto/Self refresh
H	X	X	X	H	X	High-Z	Standby

NOTES:

H = High at $V_{IN} = V_{CC} + 0.3$ V to V_{IH} (MIN.)

L = Low at $V_{IN} = V_{IL}$ (MAX.) to -1.0 V

X = Don't care at $V_{CC} + 0.3$ V to -1.0 V

VX = A_0-A_{16} address input when $\overline{CE}$ = L, then Don't Care

VY = A_0-A_8 address input when $\overline{CE}$ = L, then Don't Care, and A_9-A_{16} address = Don't Care at $V_{CC} + 0.3$ V to -1.0 V

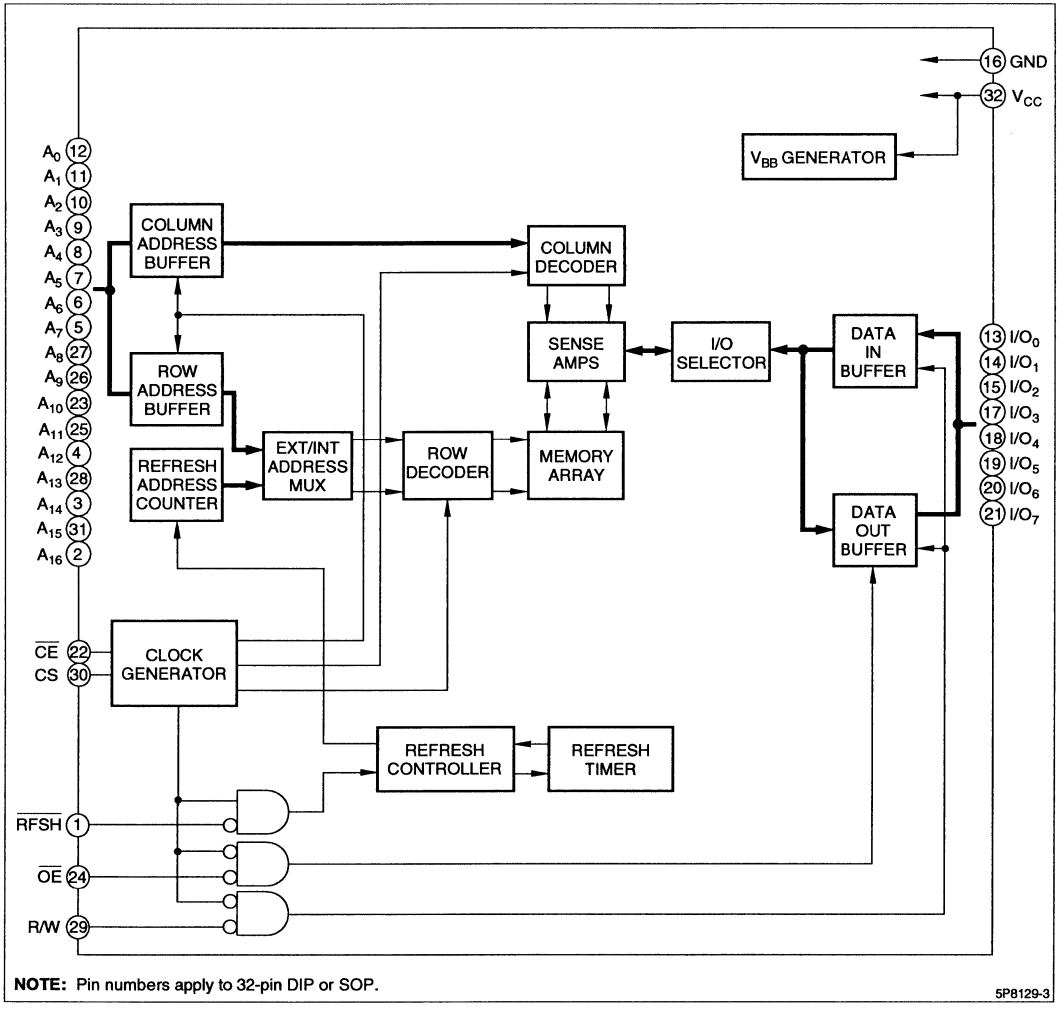


Figure 3. LH5P8129 Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME
A_0 - A_{16}	Address input
R/W	Read/Write input
$\overline{OE}$	Output Enable input
$\overline{CE}$	Chip Enable input

SIGNAL	PIN NAME
CS	Chip Select input
$\overline{RFSH}$	Refresh input
I/O_0 - I/O_7	Data input/output

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Applied voltage on any pins	V_T	-1.0 to +7.0	V	1
Operating temperature	Topr	0 to +70	°C	
Storage temperature	Tstg	-65 to +150	°C	
Output short circuit current	I_O	50	mA	
Power consumption	P_D	600	mW	

NOTE:
1. The maximum applicable voltage on any pin with respect to GND.

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	4.5	5.0	5.5	V
	GND	0	0	0	V
Input voltage	V_{IH}	2.4		V_{CC} + 0.3	V
	V_{IL}	-1.0		0.8	V

CAPACITANCE (T_A = 0 to +70°C, f = 1 MHz, V_{CC} = 5.0 V ±10%)

PARAMETER		SYMBOL	MIN.	MAX.	UNIT
Input capacitance	A_0 - A_{16}	C_{IN1}		8	pF
	R/W, $\overline{OE}$	C_{IN2}		5	pF
	$\overline{CE}$, CS	C_{IN3}		5	pF
	$\overline{RFSH}$	C_{IN4}		5	pF
Input/output capacitance	I/O_1 - I/O_7	C_{OUT1}		10	pF

DC CHARACTERISTICS (T_A = 0 to +70°C, V_{CC} = 5.0 V ±10%)

PARAMETER		SYMBOL	CONDITIONS	MIN.	MAX.	UNIT	NOTE
Operating current	LH5P8129-60	I_{CC1}	tRC = t_{RC} (MIN)		104	mA	1, 2
	LH5P8129-80				70		
	LH5P8129-10				65		
Standby current	TTL Input	I_{CC2}			1	mA	1, 3
	CMOS Input				0.1		1, 4
Self-refresh average current	TTL Input	I_{CC3}			1	mA	1, 5
	CMOS Input				0.1		1, 6
Input leakage current		I_{LI}	0 V ≤ V_{IN} ≤ 6.5 V 0 V except on test pins	-10	10	µA	
I/O leakage current		I_{LO}	0 V ≤ V_{OUT} ≤ V_{CC} + 0.3 V Output in high-impedance state	-10	10	µA	
Output HIGH voltage		V_{OH}	I_{OUT} = 1 mA	2.4		V	
Output LOW voltage		V_{OL}	I_{OUT} = 4 mA		0.4	V	

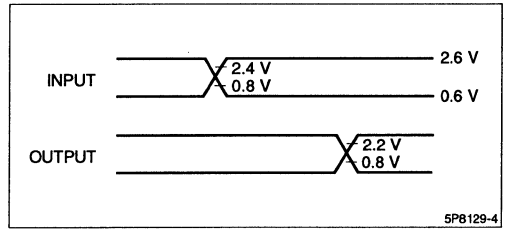
NOTES:
1. The output pins are in high-impedance state
2. I_{CC1} depends on the cycle time
3. $\overline{CE}$ = V_{IH}, $\overline{RFSH}$ = V_{IH}
4. $\overline{CE}$ = V_{CC} - 0.2 V, $\overline{RFSH}$ = V_{CC} - 0.2 V
5. $\overline{CE}$ = V_{IH}, $\overline{RFSH}$ = V_{IL}
6. $\overline{CE}$ = V_{CC} - 0.2 V, $\overline{RFSH}$ = 0.2 V

AC ELECTRICAL CHARACTERISTICS [1,2,3] (T_A = 0 to +70°C, V_{CC} = 5.0 V ±10%)

PARAMETER	SYMBOL	LH5P8129-60		LH5P8129-80		LH5P8129-10		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Random read, write cycle time	t_{RC}	100		130		160		ns	
Read modify write cycle time	t_{RMW}	155		195		235		ns	
$\overline{CE}$ pulse width	t_{CE}	60	10,000	80	10,000	100	10,000	ns	
$\overline{CE}$ precharge time	t_P	30		40		50		ns	
CS setup time	t_{CSS}	0		0		0		ns	
CS hold time	t_{CSH}	15		20		25		ns	
Address setup time	t_{AS}	0		0		0		ns	4
Address hold time	t_{AH}	15		20		25		ns	4
Read command setup time	t_{RCS}	0		0		0		ns	
Read command hold time	t_{RCH}	0		0		0		ns	
$\overline{CE}$ access time	t_{CEA}		60		80		100	ns	5
$\overline{OE}$ access time	t_{OEA}		25		30		35	ns	5
$\overline{CE}$ to output in Low-Z	t_{CLZ}	20		20		20		ns	
$\overline{OE}$ to output in Low-Z	t_{OLZ}	0		0		0		ns	
Output enable from end of write	t_{WLZ}	0		0		0		ns	
Chip disable to output in High-Z	t_{CHZ}		20		25		30	ns	
Output disable to output in High-Z	t_{OHZ}		20		25		30	ns	
Write enable to output in High-Z	t_{WHZ}		20		25		30	ns	
$\overline{OE}$ setup time	t_{OES}	0		0		0		ns	
$\overline{OE}$ hold time	t_{OEH}	10		10		10		ns	
Write command pulse width	t_{WP}	30		30		30		ns	
Write command setup time	t_{WCS}	30		30		30		ns	
Write command hold time	t_{WCH}	40		50		60		ns	
Data setup time from write	t_{DSW}	25		30		35		ns	6
Data setup time from $\overline{CE}$	t_{DSC}	25		30		35		ns	6
Data hold time from write	t_{DHW}	0		0		0		ns	6
Data hold time from $\overline{CE}$	t_{DHC}	0		0		0		ns	6
Transition time (rise and fall)	t_T	3	35	3	35	3	35	ns	
Refresh time interval	t_{REF}		8		8		8	ms	
Refresh command hold time	t_{RHC}	15		15		15		ns	
Auto refresh cycle time	t_{FC}	100		130		160		ns	
Refresh delay time from $\overline{CE}$	t_{RFD}	30		40		50		ns	
Refresh pulse width (Auto refresh)	t_{FAP}	30	8,000	30	8,000	30	8,000	ns	
Refresh precharge time (Auto refresh)	t_{FP}	30		30		30		ns	
Refresh pulse width (Self refresh)	t_{FAS}	8,000		8,000		8,000		ns	
$\overline{CE}$ delay time from refresh precharge (Self refresh)	t_{FRS}	140		160		190		ns	

NOTES:

1. In order to initialize the circuit, an initial pause of 100 µs with $\overline{CE}$ = V_{IH}, RFSH = V_{IH} after power-up, followed by at least 8 dummy cycles.
2. AC characteristics are measured at t_T = 5 ns.
3. AC characteristics are measured at the following condition (see figure at right).
4. Measured with a load equivalent to 2TTL + 100 pF.
5. Address is latched at the negative edge of $\overline{CE}$.
6. Data is latched at the positive edge of R/W or at the positive edge of $\overline{CE}$.



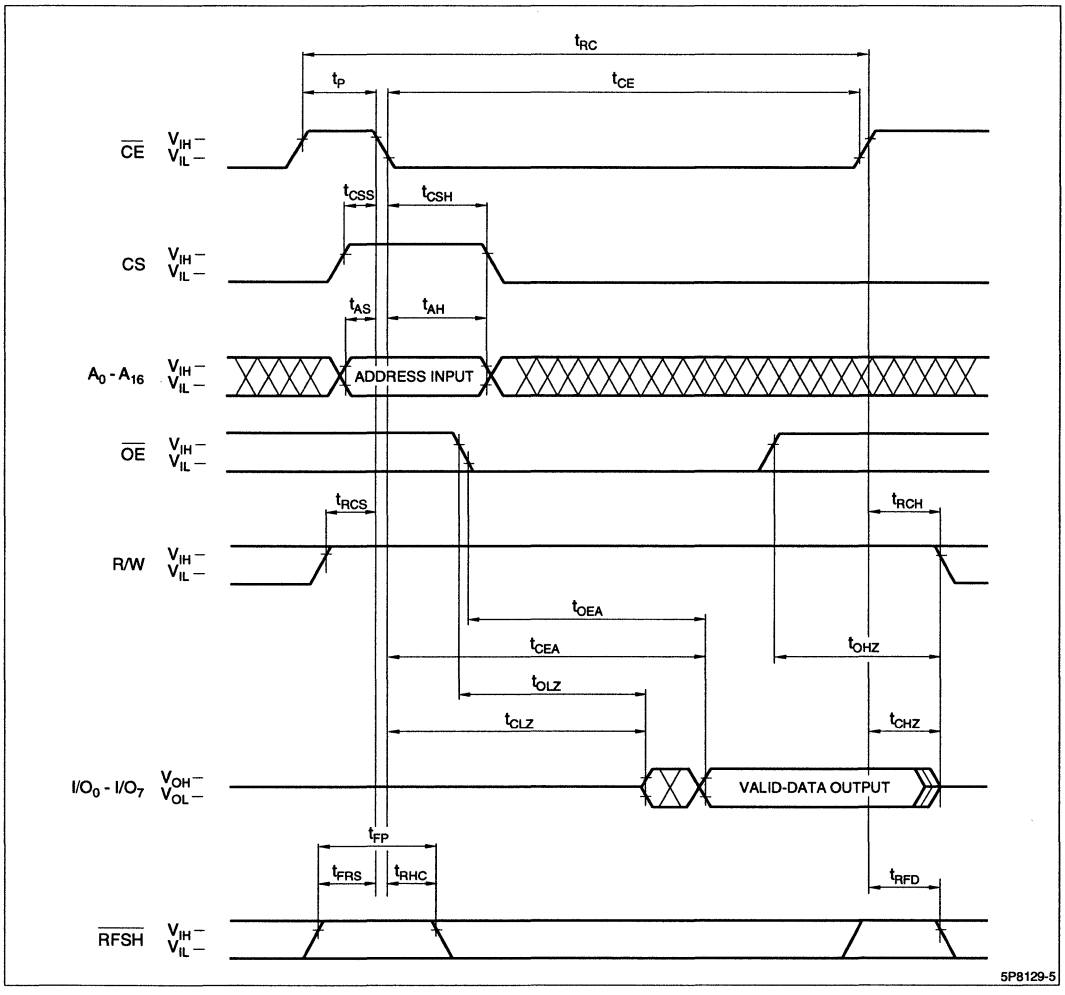


Figure 3. Read Cycle

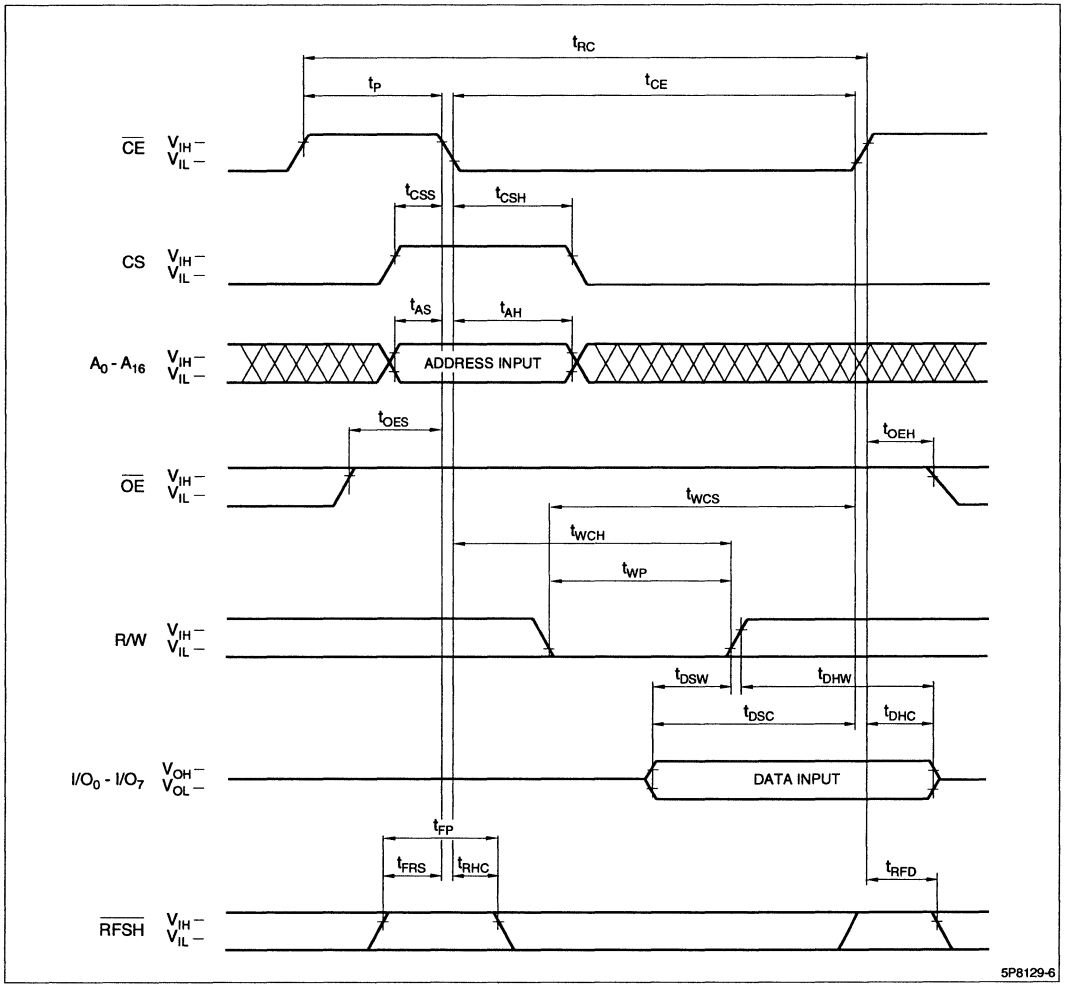


Figure 4. Write Cycle 1 ($\overline{OE}$ = HIGH)

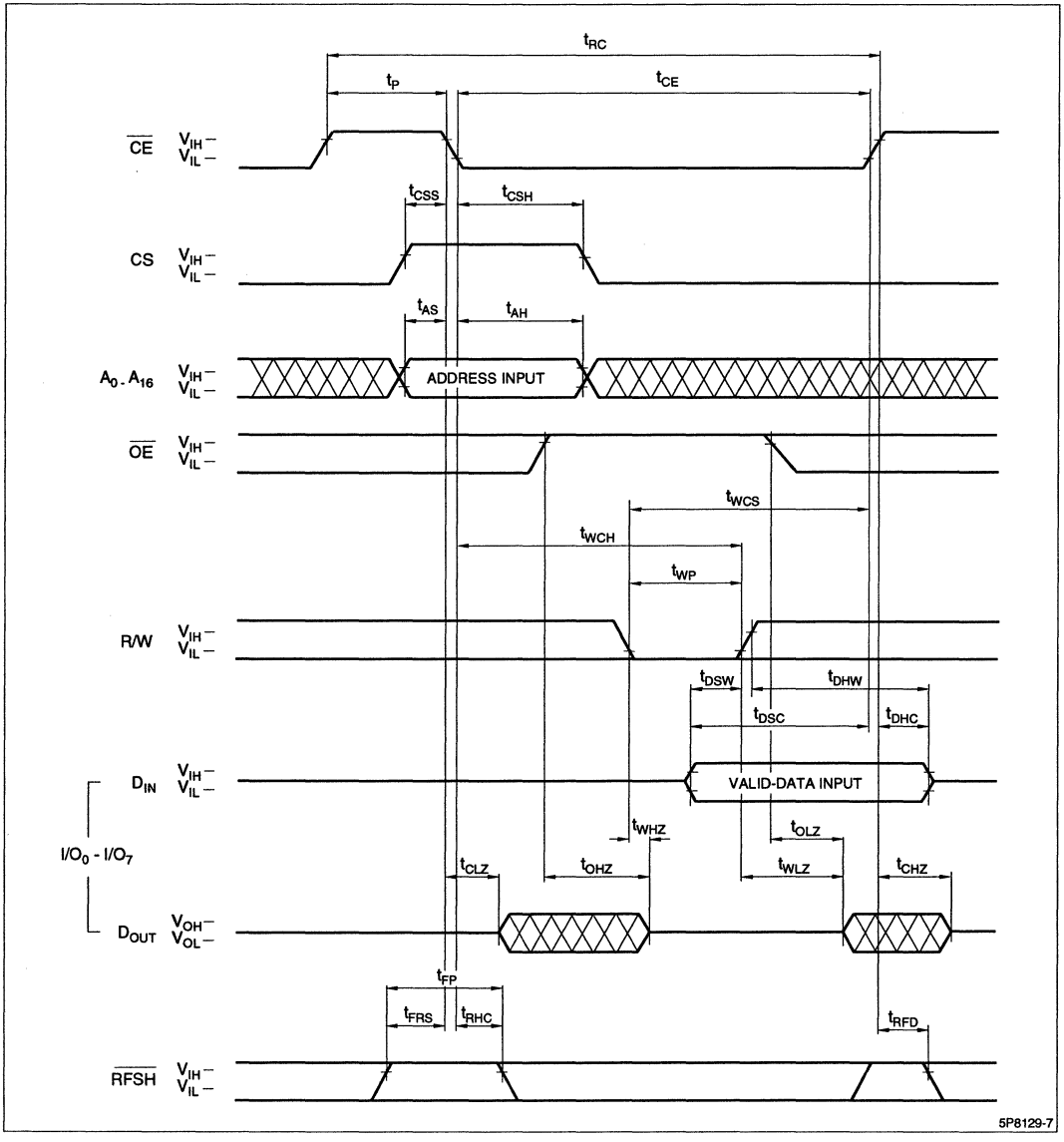


Figure 5. Write Cycle 2 ($\overline{OE}$ Clock)

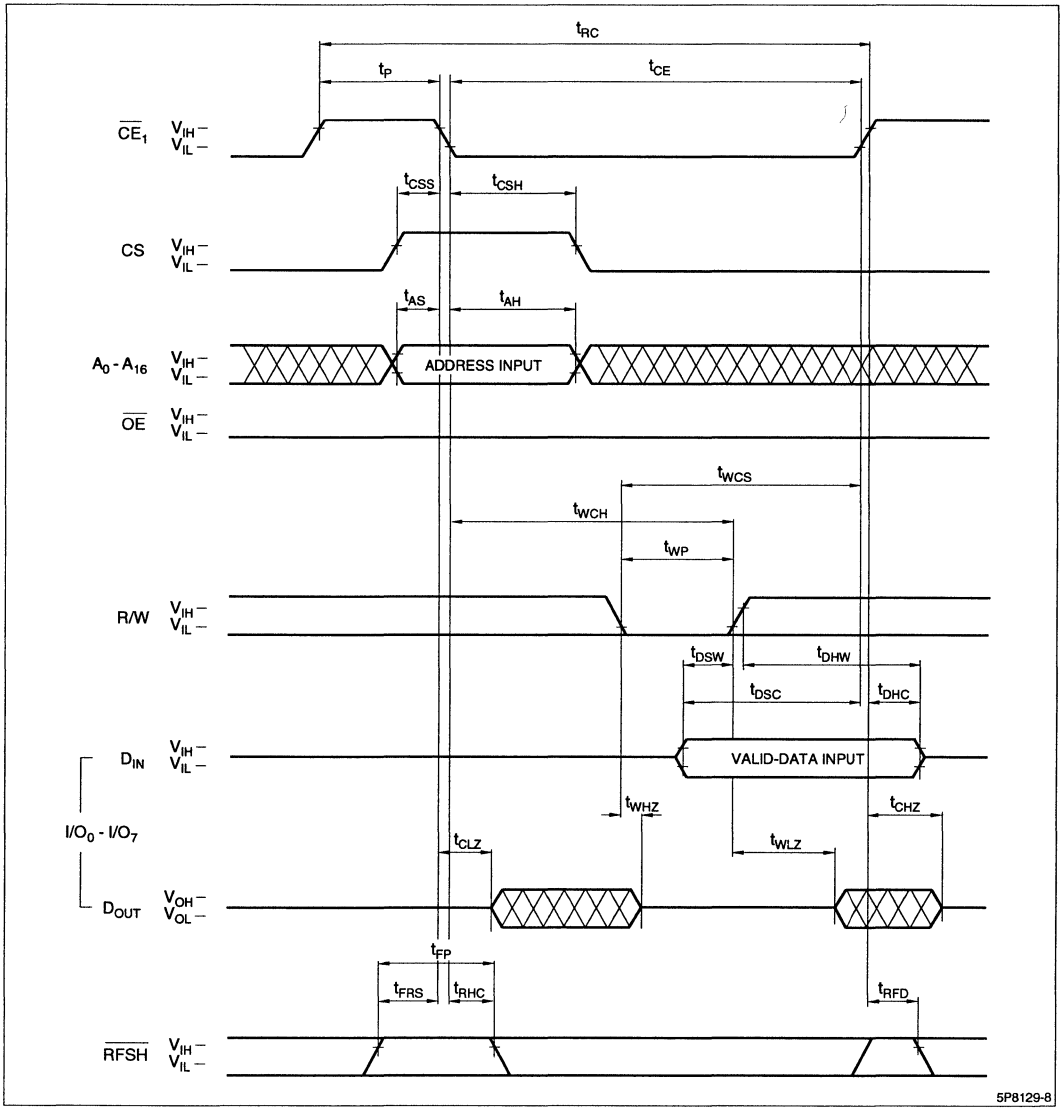


Figure 6. Write Cycle 3 ($\overline{OE}$ = LOW)

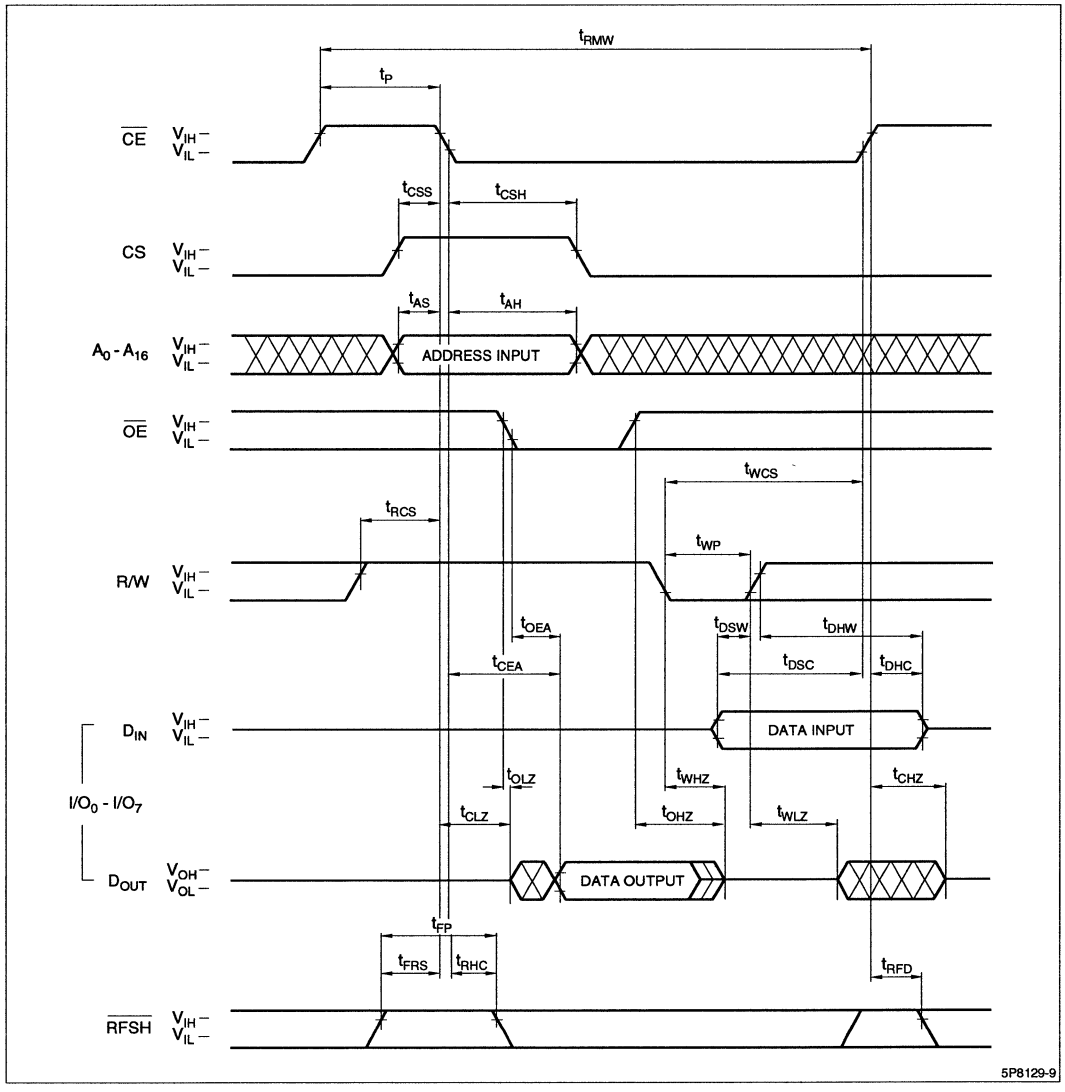


Figure 7. Read-Modify-Write Cycle

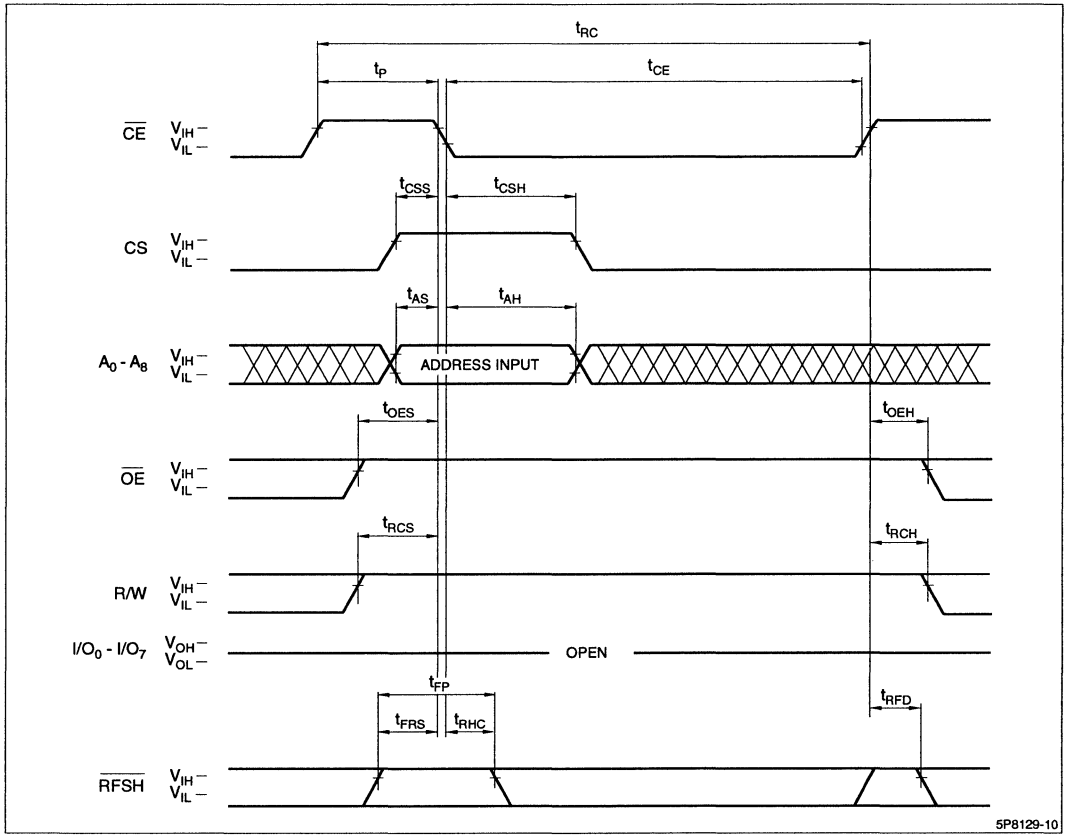


Figure 8. $\overline{CE}$ Only Refresh

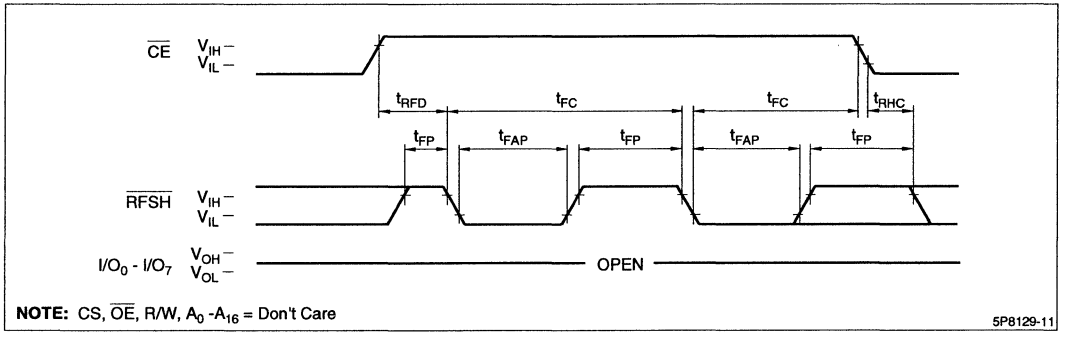


Figure 9. Auto Refresh Cycle

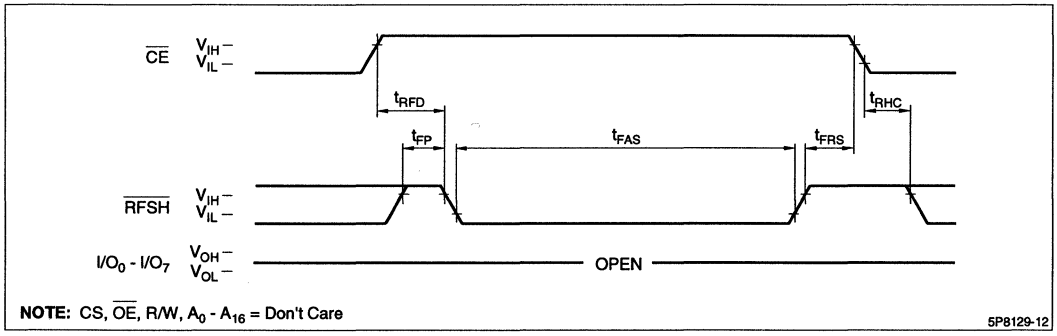


Figure 11. Self Refresh Cycle

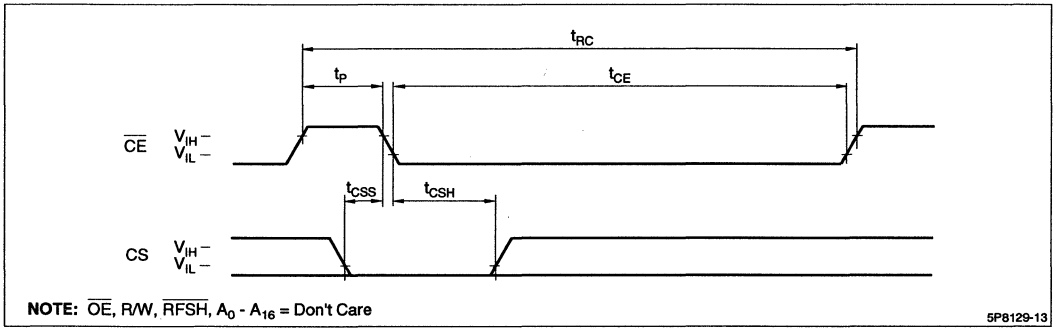


Figure 12. CS Standby Mode

ORDERING INFORMATION

LH5P8129 — Device Type

X — Package
- Blank 32-pin, 600-mil DIP (DIP32-P-600)
- N 32-pin, 525-mil SOP (SOP32-P-525)
- T 32-pin, 8 x 20 mm² TSOP (Type I) (TSOP32-P-0820)
- TR 32-pin, 8 x 20 mm² TSOP (Type I) Reverse bend (TSOP32-P-0820)

- ## — Speed
  - 60L 60
  - 80L 80 Access Time (ns)
  - 10L 100

CMOS 1M (128K x 8) Pseudo-Static RAM

Example: LH5P8129N-60L (CMOS 1M (128K x 8) Pseudo-Static RAM, 60 ns, 32-pin, 525-mil SOP)

5P8129-14

PSEUDO-STATIC RAM CROSS REFERENCE

ORGANIZATIONAL STRUCTURE	SHARP MODEL	COMPETITIVE VENDOR	COMPETITIVE MODEL	ACCESS TIME	PACKAGE OPTIONS
32K × 8	LH5P832	Hitachi	HM65256B	100/120 ns	DIP/SKDIP/SOP
		Toshiba	TC51832		
64K × 8	LH5P864	–	–	80 ns	SOP
		–	–		
128K × 8	LH5P8128	Hitachi	HM658128A	60/80/100 ns	DIP/SOP/TSOP-I
		Toshiba	TC518128A		
128K × 8 w/CS	LH5P8129	Toshiba	TC518129A	60/80/100 ns	DIP/SOP/TSOP-I

STATIC RAMs

LH5101

CMOS 1K (256 × 4) Static RAM

FEATURES

- 256 × 4 bit organization
- Access time: 300 ns (MAX.)
- Low-power consumption:
  Operating: 137.5 mW
  Standby: 55 μW
- Single +5 V power supply
- Fully-static operation
- TTL compatible I/O
- Three-state outputs
- Two Chip Enables for ease of use
- CE_2 signal enables the device to operate on a minimum standby current
- Data retention is possible with low supply voltage (2.0 V)
- Pin-to-pin equivalent to the Intel 5101
- Package: 22-pin, 300-mil DIP

DESCRIPTION

The LH5101 is a static RAM organized as 256 × 4 bits. It is fabricated using silicon-gate CMOS process technology.

PIN CONNECTIONS

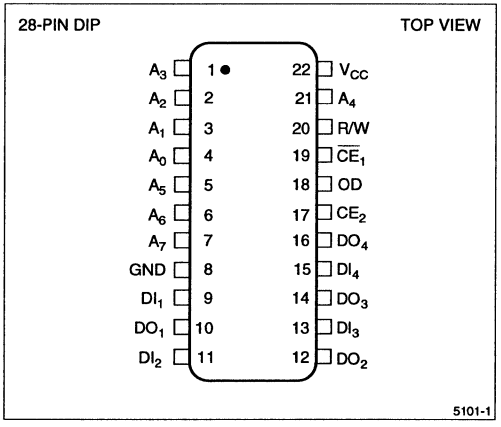


Figure 1. Pin Connections for DIP Package

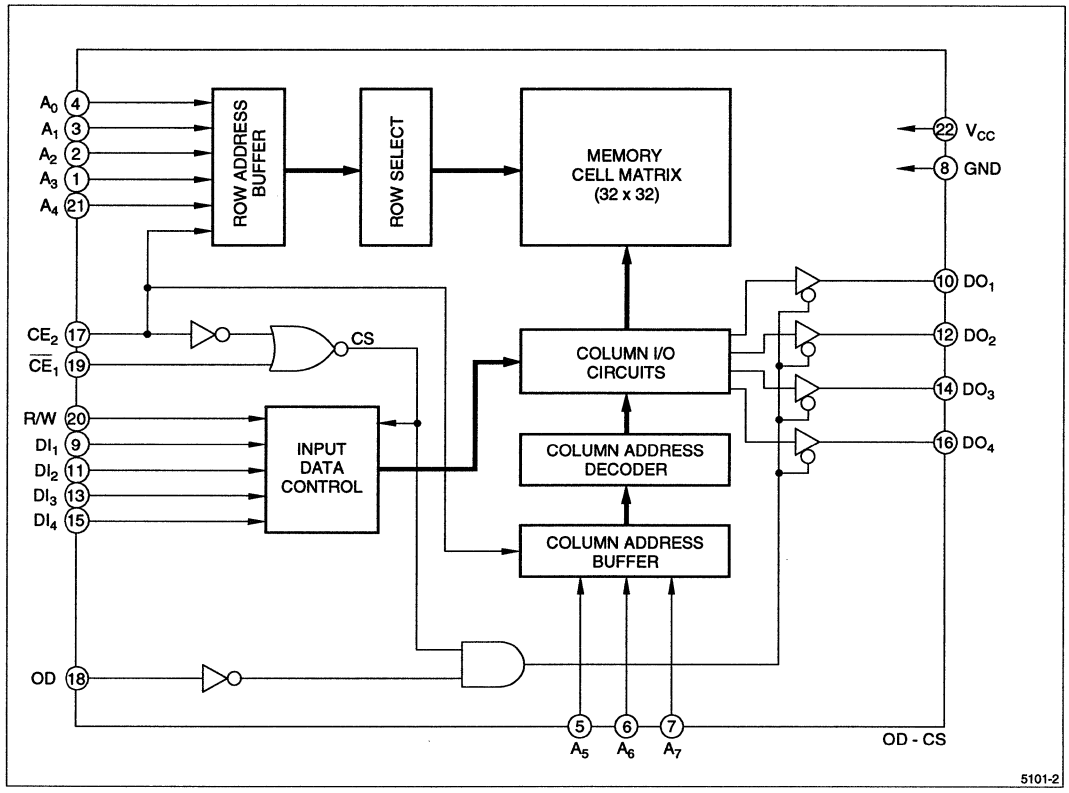


Figure 2. LH5101 Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME
A_0 - A_7	Address input
DI_1 - DI_4	Data input
DO_1 - DO_4	Data output
R/W	Read/write Enable input
$\overline{CE}_1$	Chip Enable input 1

SIGNAL	PIN NAME
CE_2	Chip Enable input 2
OD	Output disable
V_{CC}	Power supply
GND	Ground (0 V)

TRUTH TABLE

$\overline{CE}_1$	CE_2	OD	R/W	D_{IN}	OUTPUT	MODE
H	X	X	X	X	High-Z	Deselect
X	L	X	X	X	High-Z	Deselect
X	X	H	H	X	High-Z	Output deselect
L	H	H	L	X	High-Z	Write
L	H	L	L	X	D_{IN}	Write
L	H	L	H	X	D_{OUT}	Read

NOTE:
1. X = H or L

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Supply voltage	V_{CC}	-0.3 to +7.0	V	1
Input voltage	V_{IN}	-0.3 to V_{CC} + 0.3	V	1
Output voltage	V_{OUT}	-0.3 to V_{CC} + 0.3	V	1
Operating temperature	Topr	0 to +70	°C	
Storage temperature	Tstg	-55 to +150	°C	

NOTE:
1. The maximum applicable voltage on any pin with respect to GND.

DC CHARACTERISTICS (T_A = 0 to 70°C, V_{CC} = 5 V ±10%)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input 'LOW' voltage	V_{IL}				0.65	V
Input 'HIGH' voltage	V_{IH}		2.2			V
Output 'LOW' voltage	V_{OL}	I_{OL} = 2.0 mA			0.4	V
Output 'HIGH' voltage	V_{OH}	I_{OH} = -1.0 mA	2.4			V
Input leakage current	$\lvert I_{LI} \rvert$	V_I = 0 V to V_{CC}			1.0	µA
Output leakage current	$\lvert I_{LO} \rvert$	V_I = 0 V to V_{CC}, $\overline{CE}_1$ = 2.2 V			1.0	µA
Operating current	I_{CC1}	Outputs open, V_I = V_{CC}, $\overline{CE}_1$ = 0.65 V			20	mA
	I_{CC2}	Outputs open, V_I = 2.2 V, $\overline{CE}_1 \leq$ 0.65 V			25	mA
Standby current	I_{SB}	V_I = 0 V to V_{CC}, $\overline{CE}_2$ = 0.2 V			10	µA

AC CHARACTERISTICS

(1) READ CYCLE (T_A = 0 to 70°C, V_{CC} = 5 V ±10%)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Read cycle time	t_{RC}	300			ns
Address access time	t_{AA}			300	ns
Chip enable access time 1	t_{CO1}			250	ns
Chip enable access time 2	t_{CO2}			350	ns
Output disable to output	t_{OD}			180	ns
Data output to high-Z state	t_{DF}			100	ns
Previous read data valid with respect to address change	t_{OH1}	0			ns
Previous read data valid with respect to chip enable	t_{OH2}	0			ns

(2) WRITE CYCLE (T_A = 0 to 70°C, V_{CC} = 5 V ±10%)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Write cycle time	t_{WC}	300			ns
Chip enable (CE_1) to end of write	t_{CW1}	250			ns
Chip enable (CE_2) to end of write	t_{CW2}	250			ns
Address valid time	t_{AW}	60			ns
Data valid to end of write	t_{DW}	150			ns
Data hold time	t_{DH}	40			ns
Write recovery time	t_{WR}	40			ns
OD setup time	t_{OD}	100			ns

AC TEST CONDITIONS

PARAMETER	MODE
Input voltage amplitude	0.65 V to 2.2 V
Input rise/fall time	10 ns
Timing reference level	1.5 V
Output load condition	1TTL + 100 pF

DATA RETENTION CHARACTERISTICS [1]

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Data retention voltage	V_{CCDR}	$V_{CE2} \leq 0.2$ V	2.0			V	
Data retention current	I_{CCDR}	$V_{CE2} \leq 0.2$ V, $V_{CCDR} = 2.0$ V			10	µA	
Chip disable to data retention	t_{CDR}		0			ns	
Recovery time	t_R		t_{RC}			ns	2

NOTES:
1. In the data hold mode, voltage on any I/O pin should be lower than V_{DR}.
2. t_{RC} = Read cycle time

CAPACITANCE (f = 1MHz, T_A = 25°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input capacitance	C_{IN}	$V_{IN} = 0$ V		3.5	6	pF
Input/output capacitance	$C_{I/O}$	$V_{I/O} = 0$ V		9	12	pF

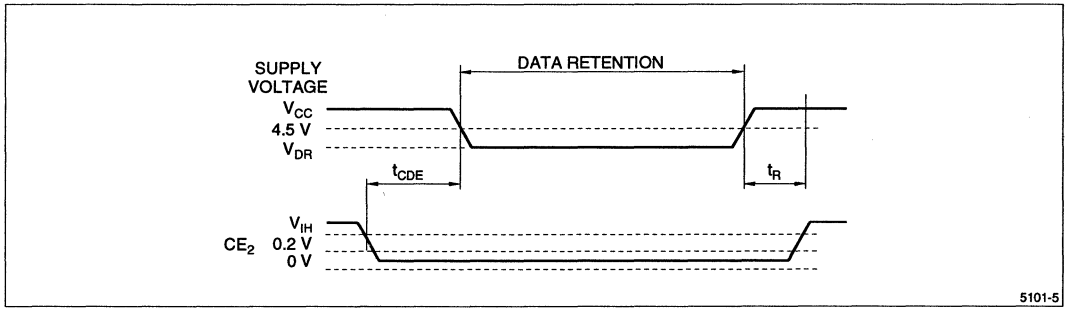
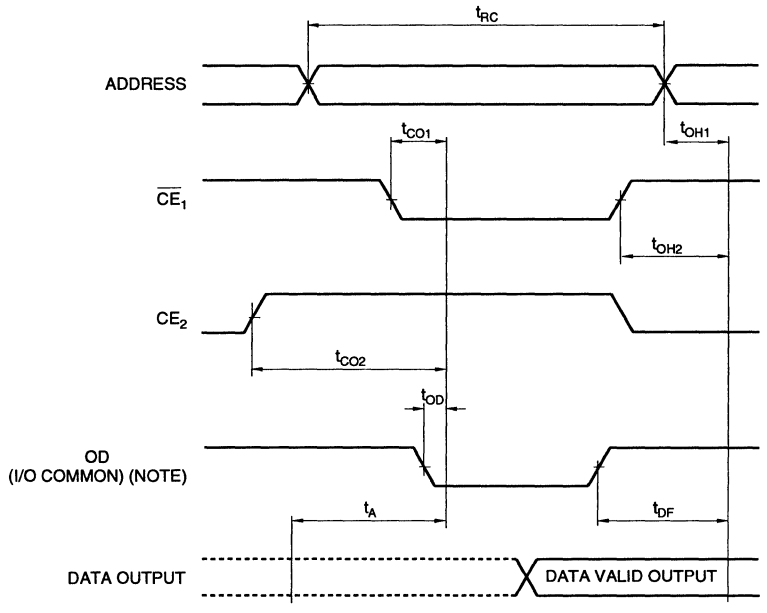


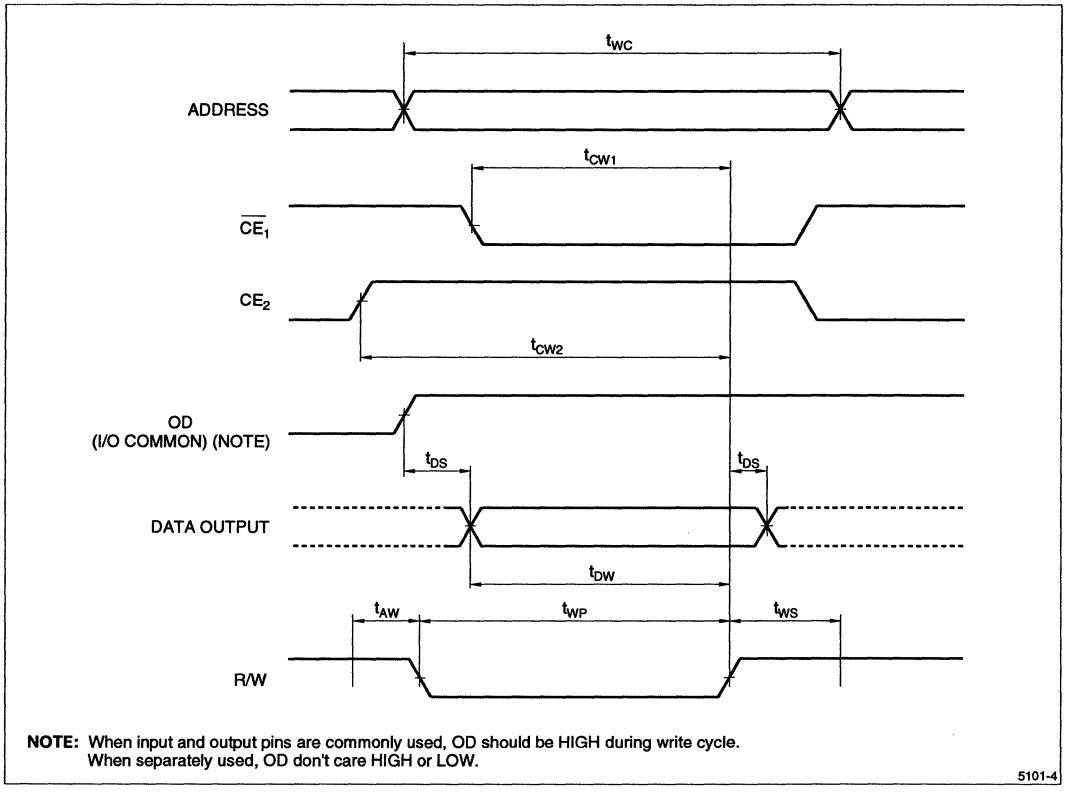
Figure 3. Low Voltage Data Retention



NOTES:
1. When data input and output are separately used, OD should be LOW.
2. During read cycle, R/W should be HIGH.

5101-3

Figure 4. Read Cycle

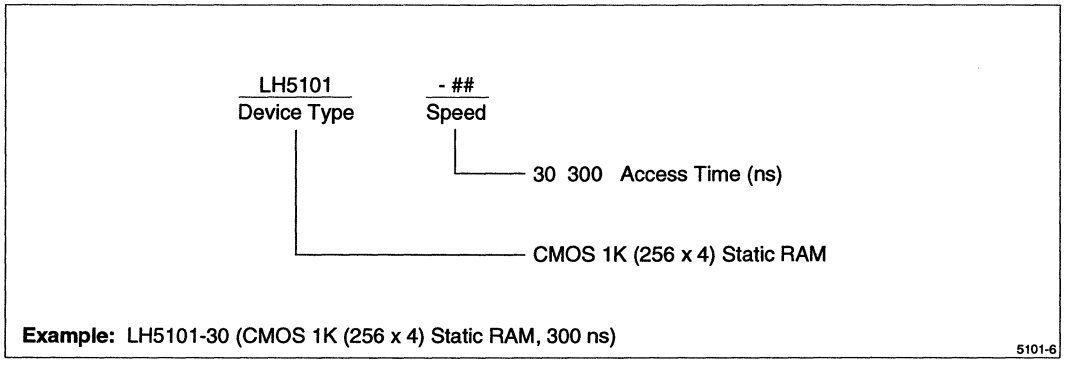


NOTE: When input and output pins are commonly used, OD should be HIGH during write cycle.
When separately used, OD don't care HIGH or LOW.

5101-4

Figure 5. Write Cycle

ORDERING INFORMATION



Example: LH5101-30 (CMOS 1K (256 x 4) Static RAM, 300 ns)

5101-6

LH5114

CMOS 4K (1K × 4) Static RAM

FEATURES

- 1,024 × 4 bit organization
- Access time: 150 ns (MAX.)
- Power consumption:
  Operating: 110 mW (MAX.)
  Standby: 27.5 μW (MAX.)
- Single +5 V power supply
- Low V_{CC} (2.0 V) data retention capability
- No need for external clock and refreshing
- TTL compatible I/O
- Three-state outputs
- Easy expansion of memory capacity through chip select signal
- Data pins common to input and output
- Package: 18-pin, 300-mil DIP

DESCRIPTION

The LH5114H is a static RAM organized as 1,024 × 4 bits. It is fabricated using silicon-gate CMOS process technology.

PIN CONNECTIONS

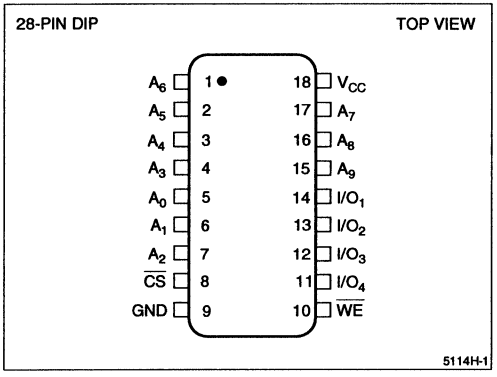


Figure 1. Pin Connections for DIP Package

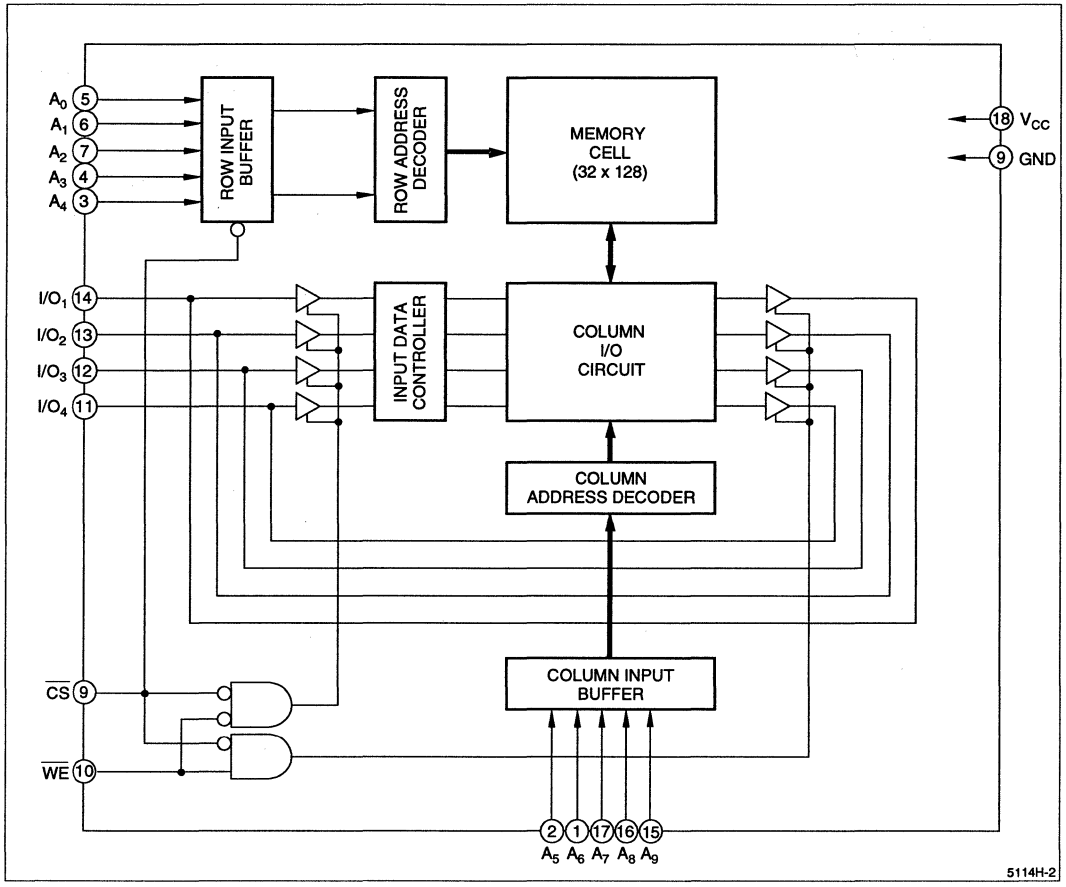


Figure 2. LH5114H Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME
A_0 - A_9	Address input
$\overline{WE}$	Write Enable input
$\overline{CS}$	Chip Select input

SIGNAL	PIN NAME
I/O_1 - I/O_4	Data input/output
V_{CC}	Power supply (5 V or 2 V)
GND	Ground

TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	MODE	I/O_1 - I/O_4	NOTE
H	X	Deselect	High-Z	1
L	L	Write	D_{IN}	
L	H	Read	D_{OUT}	

NOTE:
1. X = H or L

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Supply voltage	V_{CC}	-0.3 to +7.0	V
Input voltage	V_{IN}	-0.3 to V_{CC} + 0.3	V
Output Voltage	V_{OUT}	-0.3 to V_{CC} + 0.3	V
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	-55 to +150	°C

DC CHARACTERISTICS (T_A = 0 to +70°C, V_{CC} = 5 V ±10%)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input 'Low' voltage	V_{IL}				0.8	V
Input 'High' voltage	V_{IH}		2.2			V
Output 'Low' voltage	V_{OL}	I_{OL} = 2.0 mA			0.4	V
Output 'High' voltage	V_{OH}	I_{OH} = -1.0 mA	2.4			V
Input leakage current	$\lvert I_{LI} \rvert$	V_{IN} = 0 V to V_{CC}			1.0	µA
Output leakage current	$\lvert I_{LO} \rvert$	$\overline{CS}$ = V_{IH}, $V_{I/O}$ = 0.4 V to V_{CC}			1.0	µA
Operating current	I_{CC}	$\overline{CS}$ = V_{IL}, Minimum cycle		10	20	mA
Standby current	I_{SB}	$\overline{CS}$ = V_{CC}, V_{IN} = 0 V to V_{CC}			5.0	µA

AC CHARACTERISTICS

(1) READ CYCLE (T_A = 0 to +70°C, V_{CC} = 5 V ±10%)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Read cycle time	t_{RC}	150			ns
Address access time	t_{AA}			150	ns
Chip enable access time	t_{ACE}			150	ns
Output hold time	t_{OH}	15			ns
Output to Chip Select	t_{OC}	15			ns
Output floating to Chip Select	t_{CZ}			40	ns

(2) WRITE CYCLE (T_A = 0 to +70°C, V_{CC} = 5 V ±10%)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Write cycle time	t_{WC}	150			ns
Chip enable to end of write	t_{CW}	110			ns
Address valid time	t_{AW}	110			ns
Address setup time	t_{AS}	0			ns
Write pulse width	t_{WP}	110			ns
Write recovery time	t_{WR}	20			ns
Data valid to end of write	t_{DW}	70			ns
Data hold time	t_{DH}	20			ns
$\overline{WE}$ to output in High-Z	t_{WZ}			40	ns
Output active from end of write	t_{OW}	15			ns

AC TEST CONDITIONS

PARAMETER	MODE
Input voltage amplitude	0.8 V to 2.2 V
Input rise/fall time	10 ns
Timing reference level	1.5 V
Output load condition	1TTL + 100 pF

DATA RETENTION CHARACTERISTICS (T_A = 0°C to 70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Data retention voltage	V_{CCDR}		2.0			V
Data retention $\overline{CS}$ voltage	$V_{I(\overline{CS})}$	$2.2\ V \le V_{CC(PD)} \le V_{CC}$	2.2			V
		$2.0\ V \le V_{CC(PD)} \le 2.2\ V$	$V_{CC(PD)}$			V
Data retention current	I_{CCDR}	$V_I = V_{CC} = 2.0\ V$		0.5	10	µA
Chip disable to data retention	t_{CDR}		t_{RC}			ns
Recovery time	t_R		t_{RC}			ns

CAPACITANCE (f = 1 MHz, T_A = 25°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Input capacitance	C_{IN}			5	pF
Input/output capacitance	$C_{I/O}$			8	pF

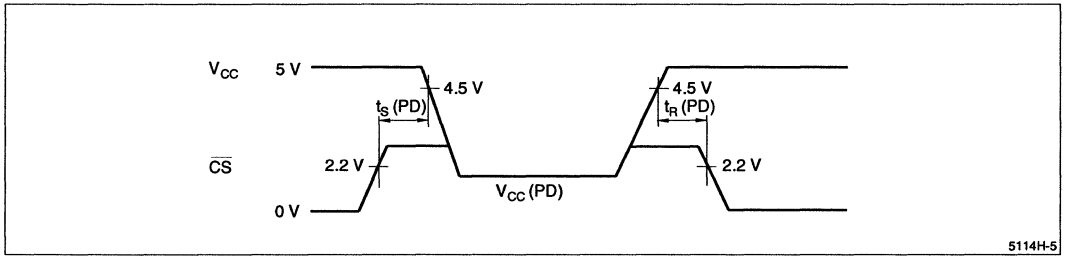


Figure 3. Low Voltage Data Retention

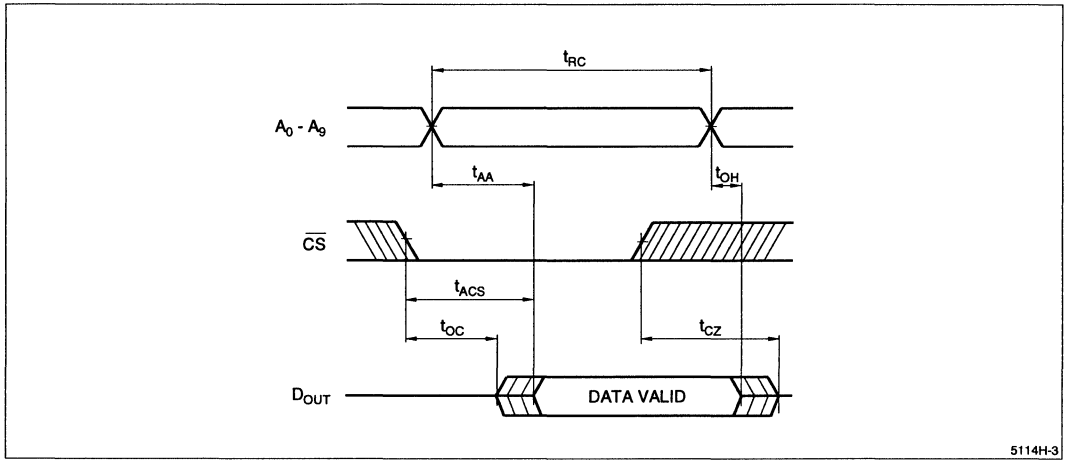


Figure 4. Read Cycle

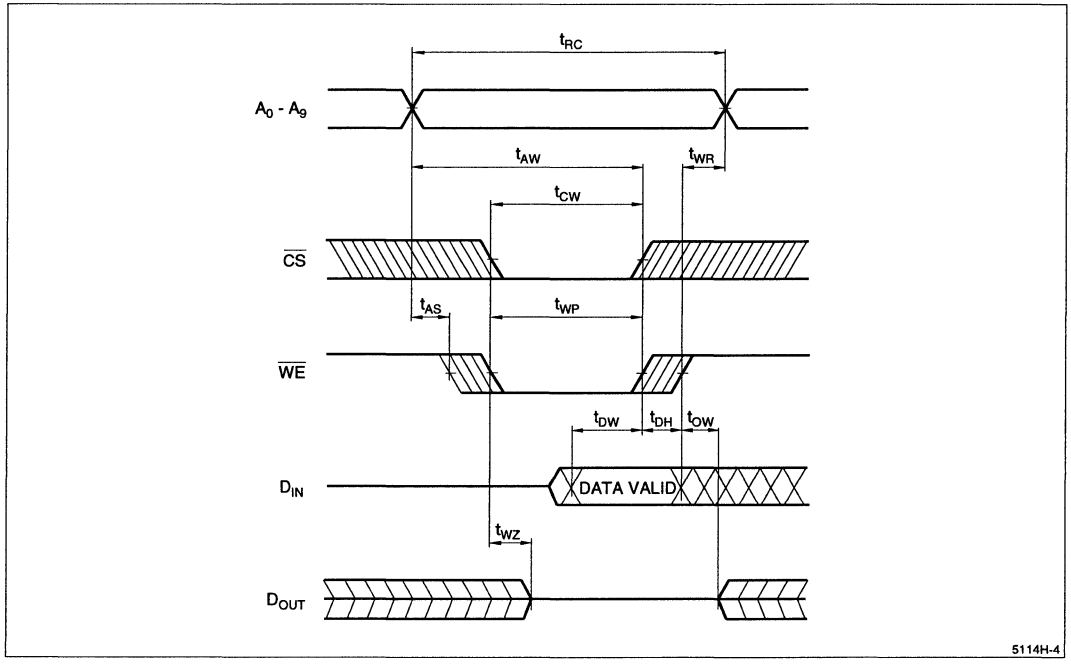
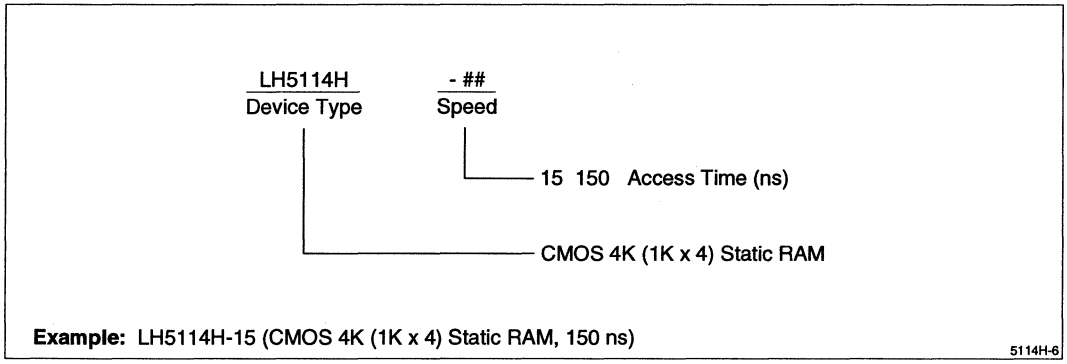


Figure 5. Write Cycle

ORDERING INFORMATION



Example: LH5114H-15 (CMOS 4K (1K x 4) Static RAM, 150 ns)

5114H-6

LH5116

CMOS 16K (2K × 8) Static RAM

FEATURES

- 2,048 × 8 bit organization
- Access time: 100 ns (MAX.)
- Power consumption:
  Operating: 220 mW (MAX.)
  Standby: 5.5 µW (MAX.)
- Single +5 V power supply
- Fully-static operation
- TTL compatible I/O
- Three-state outputs
- Wide temperature range available
  LH5116H: -40 to +85°C
- Packages:
  24-pin, 600-mil DIP
  24-pin, 300-mil SK-DIP
  24-pin, 450-mil, SOP
- Compatible with 16K EPROM and mask ROM pinout

DESCRIPTION

The LH5116 is a static RAM organized as 2,048 × 8 bits. It is fabricated using silicon-gate CMOS process technology. It features high speed access in read mode using output enable (t_{OE}).

PIN CONNECTIONS

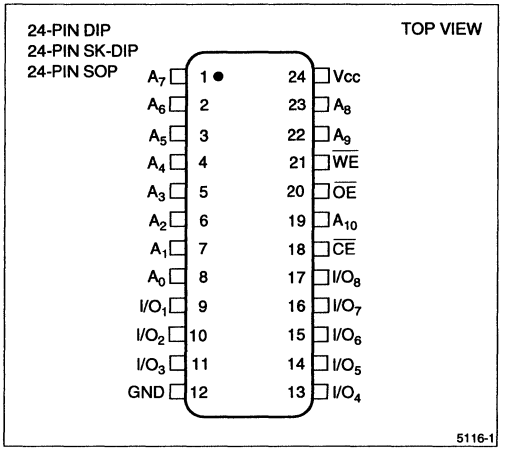


Figure 1. Pin Connections for DIP, SK-DIP, and SOP Packages

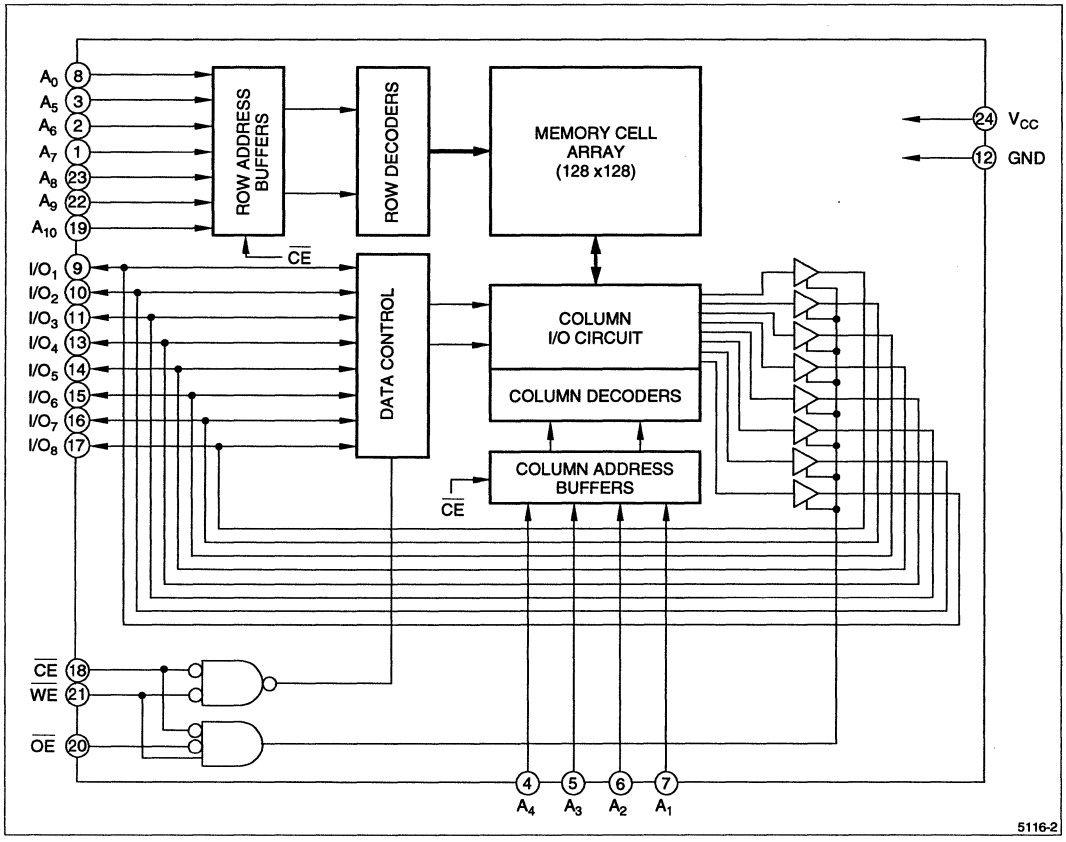


Figure 2. LH5116 Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME
A_0 - A_{10}	Address input
$\overline{CE}$	Chip Enable input
$\overline{OE}$	Output Enable input
$\overline{WE}$	Write Enable input

SIGNAL	PIN NAME
I/O_1 - I/O_8	Data input/output
V_{CC}	Power supply
GND	Ground

TRUTH TABLE

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	MODE	I/O_1 - I/O_8	SUPPLY CURRENT	NOTE
L	X	L	Write	D_{IN}	Operating (I_{CC})	1
L	L	H	Read	D_{OUT}	Operating (I_{CC})	
H	X	X	Deselect	High-Z	Standby (I_{SB})	1
L	H	X	Outputs disable	High-Z	Operating (I_{CC})	1

NOTE:
1. X = H or L

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Supply voltage	V_{CC}	-0.3 to +7.0	V	1
Input voltage	V_{IN}	-0.3 to V_{CC} + 0.3	V	1
Operating temperature	Topr	0 to +70	°C	2
		-40 to +85		3
Storage temperature	Tstg	-55 to +150	°C	

NOTES:
1. The maximum applicable voltage on any pin with respect to GND.
2. Applied to the LH5116/D/NA
3. Applied to the LH5116H/HD/HN

RECOMMENDED OPERATING CONDITIONS [1]

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage	V_{IH}	2.2		V_{CC} + 0.3	V
	V_{IL}	-0.3		0.8	V

NOTE:
1. T_A = 0 to 70°C (LH5116/D/NA), T_A = -40 to +85°C (LH5116H/HD/HN)

DC CHARACTERISTICS [1] (V_{CC} = 5 V ±10%)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Output 'LOW' voltage	V_{OL}	I_{OL} = 2.1 mA			0.4	V	
Output 'HIGH' voltage	V_{OH}	I_{OH} = -1.0 mA	2.4			V	
Input leakage current	$\|I_{LI}\|$	V_{IN} = 0 V to V_{CC}			1.0	µA	
Output leakage current	$\|I_{LO}\|$	$\overline{CE}$ = V_{IH}, $V_{I/O}$ = 0 V to V_{CC}			1.0	µA	
Operating current	I_{CC1}	Outputs open ($\overline{OE}$ = V_{CC})		25	30	mA	2
	I_{CC2}	Outputs open ($\overline{OE}$ = V_{IH})		30	40	mA	3
Standby current	I_{SB}	$\overline{CE}$ ≥ V_{CC} - 0.2 V All other input pins = 0 V to V_{CC}			1.0	µA	
					0.2		4

NOTES:
1. T_A = 0 to 70°C (LH5116/D/NA), T_A = -40 to +85°C (LH5116H/HD/HN)
2. $\overline{CE}$ = 0 V; all other input pins = 0 V to V_{CC}
3. $\overline{CE}$ = V_{IL}; all other input pins = V_{IL} to V_{IH}
4. T_A = 25°C

AC CHARACTERISTICS [1]

(1) READ CYCLE (V_{CC} = 5 V ±10%)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Read cycle time	t_{RC}	100			ns	
Address access time	t_{AA}			100	ns	
Chip enable access time	t_{ACE}			100	ns	
$\overline{CE}$ Low to output in Low-Z	t_{CLZ}	10			ns	1
Output enable access time	t_{OE}			40	ns	
Output enable Low to output in Low-Z	t_{OLZ}	10			ns	1
Chip disable to output in High-Z	t_{CHZ}	0		40	ns	1
Output disable to output in High-Z	t_{OHZ}	0		40	ns	1
Output hold time	t_{OH}	10			ns	

NOTE:
1. Active output to high-impedance and high-impedance to output active tests specified for a ±500 mV transition from steady state levels into the test load. C_{LOAD} = 5 pF.

(2) WRITE CYCLE [1] (V_{CC} = 5 V ±10%)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Write cycle time	t_{WC}	100			ns	
Chip enable to end of write	t_{CW}	80			ns	
Address valid time	t_{AW}	80			ns	
Address setup time	t_{AS}	0			ns	
Write pulse width	t_{WP}	60			ns	
Write recovery time	t_{WR}	10			ns	
Output active from end of write	t_{OW}	10			ns	2
$\overline{WE}$ Low to output in High-Z	t_{WHZ}			30	ns	2
Data valid to end of write	t_{DW}	30			ns	
Data hold time	t_{DH}	10			ns	
Output enable to output in High-Z	t_{OHZ}			40	ns	2
Output active from end of write	t_{OW}	10			ns	2

NOTES:

1. T_A = 0 to +70°C (LH5116/D/NA), T_A = -40 to +85°C (LH5116H/HD/HN)
2. Active output to high-impedance and high-impedance to output active tests specified for a ±500 mV transition from steady state levels into the test load. C_{LOAD} = 5 pF.

AC TEST CONDITIONS

PARAMETER	MODE
Input voltage amplitude	0.8 V to 2.2 V
Input rise/fall time	10 ns
Timing reference level	1.5 V
Output load condition	1TTL + 100 pF

DATA RETENTION CHARACTERISTICS [1]

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Data retention voltage	V_{CCDR}	$\overline{CE} \geq V_{CCRC}$ - 0.2 V	2.0			V	
Data retention current	I_{CCDR}	$\overline{CE} \geq V_{CCDR}$ - 0.2 V, V_{CCDR} = 3.0 V			1.0	µA	
					0.2		2
Chip disable to data retention	t_{CDR}		0			ns	
Recovery time	t_R		t_{RC}			ns	3

NOTES:

1. T_A = 0 to +70°C (LH5116/D/NA), T_A = -40 to +85°C (LH5116H/HD/HN)
2. T_A = 25°C
3. t_{RC} = Read cycle time

CAPACITANCE [1] (f = 1MHz, T_A = 25°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input capacitance	C_{IN}	V_{IN} = 0 V			7	pF
Input/output capacitance	$C_{I/O}$	$V_{I/O}$ = 0 V			10	pF

NOTE:

1. This parameter is sampled and not production tested.

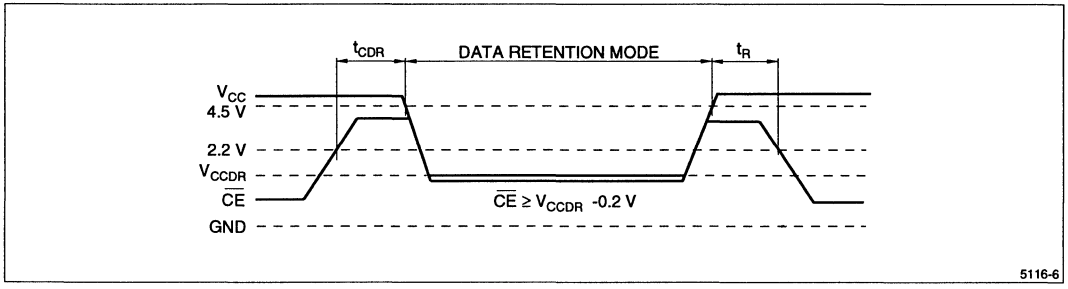


Figure 3. Low Voltage Data Retention

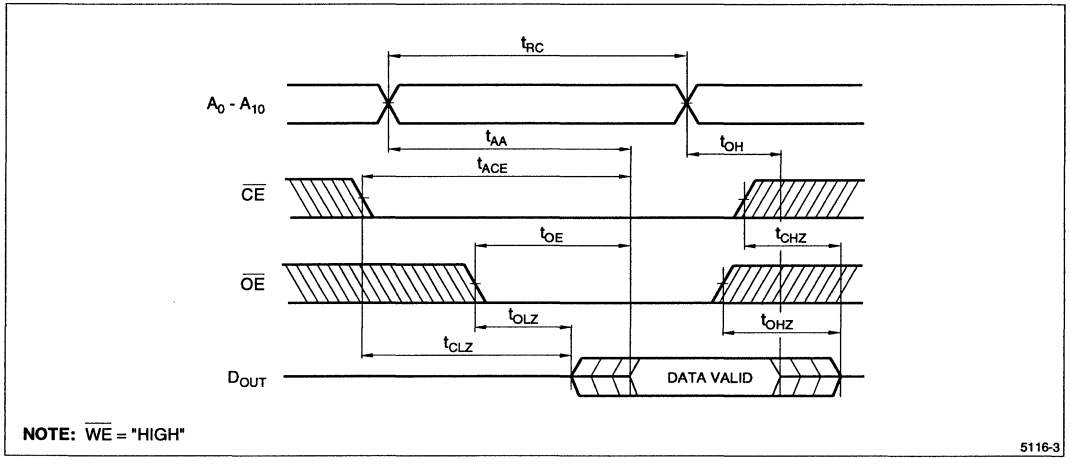
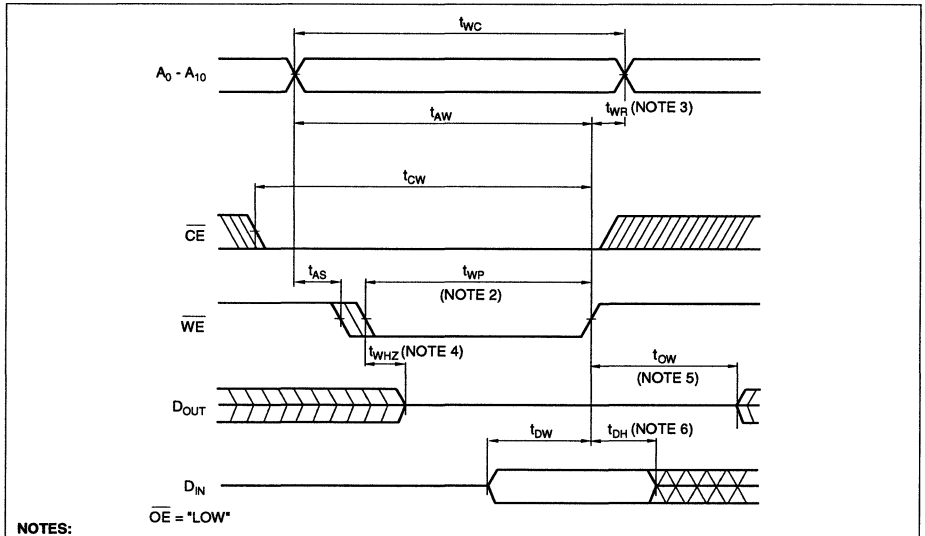


Figure 4. Read Cycle

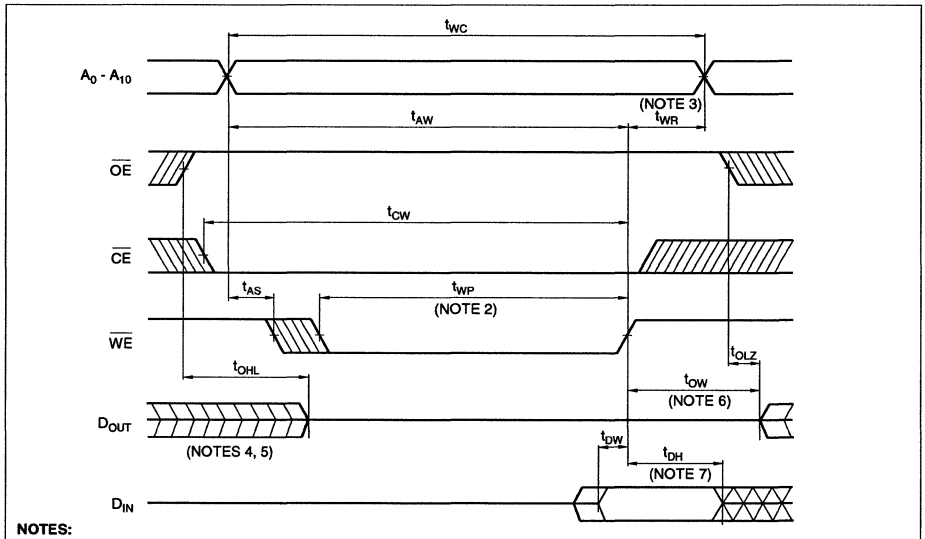


NOTES:

1. $\overline{WE}$ must be HIGH when there is a change in A_0 - A_{10}.
2. When $\overline{CE}$ and $\overline{WE}$ are all LOW at the same time, write occurs during the period t_{WP}.
3. t_{WR} is the time from the rise of $\overline{CE}$ or $\overline{WE}$, whichever is first, to the end of the write cycle.
4. If $\overline{CE}$ LOW transition occurs at the same time or before $\overline{WE}$ LOW transition, the outputs will remain high-impedance.
5. D_{OUT} outputs data with the same logic level as the input data of this write cycle.
6. If $\overline{CE}$ is LOW during this period, the input/output pin is in the output state. During this state, input signals of opposite logic level must not be applied.

5116-4

Figure 5. Write Cycle 1



NOTES:

1. $\overline{WE}$ must be HIGH when there is a change in A_0 - A_{10}.
2. When $\overline{CE}$ and $\overline{WE}$ are all LOW at the same time, write occurs during the period t_{WP}.
3. t_{WR} is the time from the rise of $\overline{CE}$ or $\overline{WE}$, whichever is first, to the end of the write cycle.
4. If $\overline{CE}$ LOW transition occurs at the same time or before $\overline{WE}$ LOW transition, the outputs will remain high-impedance.
5. D_{OUT} outputs data with the same logic level as the input data of this write cycle.
6. If $\overline{CE}$ is LOW during this period, the input/output pin is in the output state. During this state, input signals of opposite logic level must not be applied.

5116-5

Figure 6. Write Cycle 2 (Note 1)

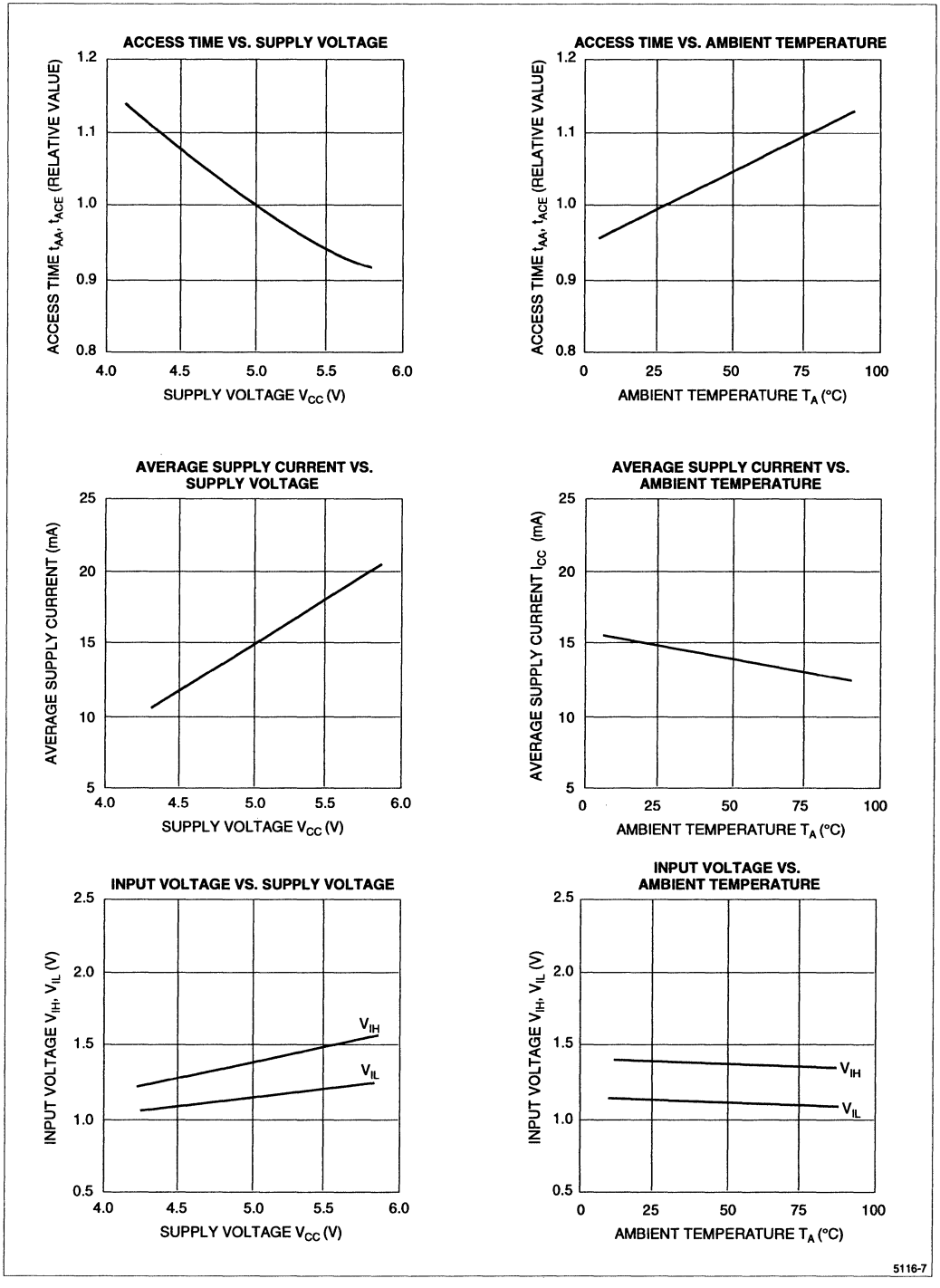
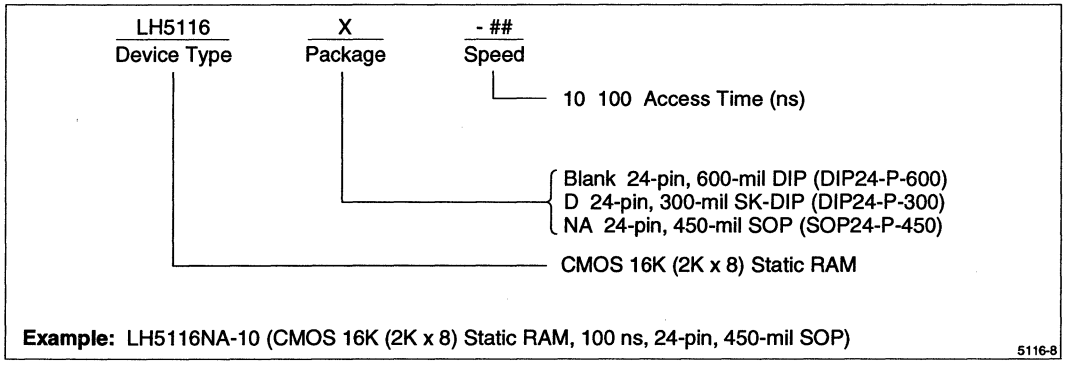


Figure 7. Electrical Characteristic Curves (V_{CC} = 5 V, T_A = 25°C unless otherwise specified)

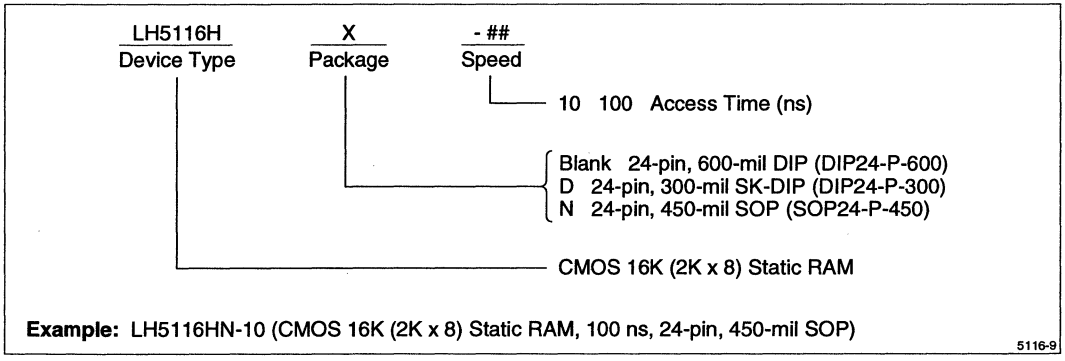
ORDERING INFORMATION (T_A = 0°C to 70°C)



Example: LH5116NA-10 (CMOS 16K (2K x 8) Static RAM, 100 ns, 24-pin, 450-mil SOP)

5116-8

ORDERING INFORMATION (T_A = -40°C to +85°C)



Example: LH5116HN-10 (CMOS 16K (2K x 8) Static RAM, 100 ns, 24-pin, 450-mil SOP)

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LH5116S

CMOS 16K (2K × 8) Static RAM

FEATURES

- 2,048 × 8 bit organization
- Access time: 1000 ns (MAX.)
- Low-power consumption:
  Operating: 33 mW (MAX.)
  Standby: 3.3 μW (MAX.)
- Fully-static operation
- Three-state outputs
- Single +3 V power supply
- Package: 24-pin, 450-mil SOP

DESCRIPTION

The LH5116S is a static RAM organized as 2,048 × 8 bits. It is fabricated using silicon-gate CMOS process technology. It operates at a low supply voltage of 3 V ±10%.

PIN CONNECTIONS

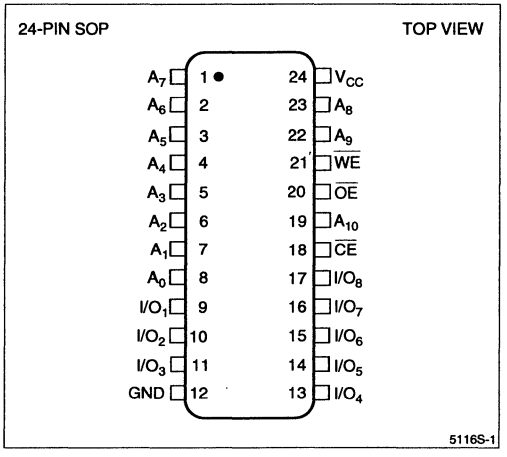


Figure 1. Pin Connections for SOP Package

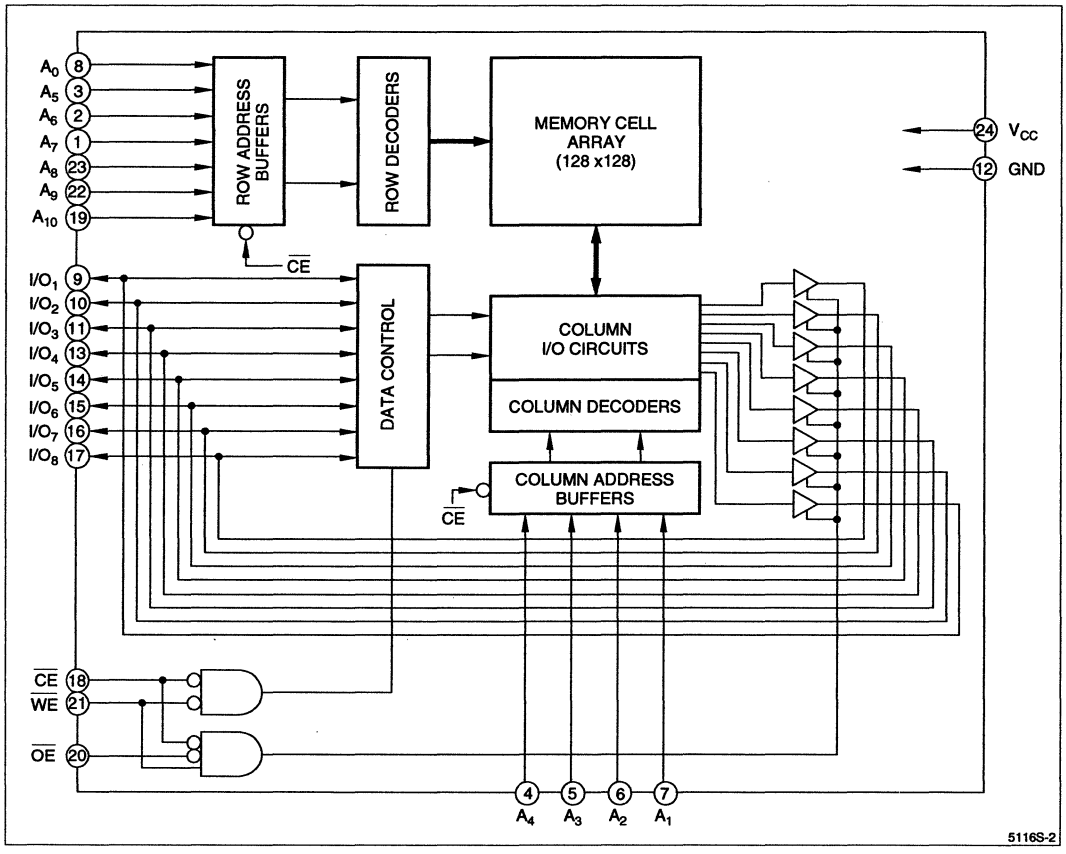


Figure 2. LH5116S Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME
A_0 - A_{10}	Address input
$\overline{CE}$	Chip Enable input
$\overline{OE}$	Output Enable input
$\overline{WE}$	Write Enable input

SIGNAL	PIN NAME
I/O_1 - I/O_8	Data input/output
V_{CC}	Power supply
GND	Ground

TRUTH TABLE

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	MODE	I/O_1 - I/O_8	SUPPLY CURRENT	NOTE
L	X	L	Write	D_{IN}	Operating (I_{CC})	1
L	L	H	Read	D_{OUT}	Operating (I_{CC})	
H	X	X	Deselected	High-Z	Standby (I_{SB})	1
L	H	X	Output disable	High-Z	Operating (I_{CC})	1

NOTE:
1. X = H or L

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Supply voltage	V_{CC}	-0.3 to +7.0	V	1
Input voltage	V_{IN}	-0.3 to V_{CC} +0.3	V	1
Operating temperature	Topr	0 to +50	°C	
Storage temperature	Tstg	-55 to +150	°C	

NOTE:
1. The maximum applicable voltage on any pin with respect to GND.

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to +50°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	2.7	3.0	3.3	V
Input voltage	V_{IH}	2.2		V_{CC} + 0.3	V
	V_{IL}	-0.3		0.8	V

DC CHARACTERISTICS (V_{CC} = 3 V ±10%, T_A = 0 to +50°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Output 'LOW' voltage	V_{OL}	I_{OL} = 2.1 mA			0.5	V	
Output 'HIGH' voltage	V_{OH}	I_{OH} = -1.0 mA	V_{CC} - 0.5			V	
Input leakage current	$\|I_{LI}\|$	V_{IN} = 0 V to V_{CC}			1.0	µA	
Output leakage current	$\|I_{LO}\|$	$\overline{CE}$ = V_{IH}, $V_{I/O}$ = 0 V to V_{CC}			1.0	µA	
Operating current	I_{CC1}	Outputs open ($\overline{OE}$ = V_{CC})		8	10	mA	1
	I_{CC2}	Outputs open ($\overline{OE}$ = V_{IH})		8	10	mA	2
Standby current	I_{CCL}	$\overline{CE}$ ≥ V_{CC} - 0.2 V All other input pins = 0 V to V_{CC}			1.0	µA	

NOTES:
1. $\overline{CE}$ = 0 V; all other input pins = 0 V to V_{CC}
2. $\overline{CE}$ = V_{IL}; all other input pins = V_{IL} to V_{IH}

AC CHARACTERISTICS (V_{CC} = 3 V ±10%, T_A = 0 to +50°C)

(1) READ CYCLE

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Read cycle time	t_{RC}	1000			ns	
Address access time	t_{AA}			1000	ns	
Chip enable access time	t_{ACE}			1000	ns	
$\overline{CE}$ Low to output in Low-Z	t_{CLZ}	10			ns	1
Output enable access time	t_{OE}			100	ns	
Output enable Low to output in Low-Z	t_{OLZ}	10			ns	1
Chip disable to output in High-Z	t_{CHZ}	0		40	ns	1
Output enable to output in High-Z	t_{OHZ}	0		40	ns	1
Output hold time	t_{OH}	10			ns	

NOTE:
1. Active output to high-impedance and high-impedance to output active tests specified for a ±500 mV transition from steady state levels into the test load. C_{LOAD} = 5 pF.

(2) WRITE CYCLE (V_{CC} = 3 V ±10%, T_A = 0 to +50°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Write cycle time	t_{WC}	1000			ns	
Chip enable to end of write	t_{CW}	100			ns	
Address valid time	t_{AW}	100			ns	
Address setup time	t_{AS}	0			ns	
Write pulse width	t_{WP}	100			ns	
Write recovery time	t_{WR}	20			ns	
$\overline{WE}$ Low to output in High-Z	t_{WHZ}			30	ns	1
Data valid to end of write	t_{DW}	50			ns	
Data hold time	t_{DH}	20			ns	
Output active from end of write	t_{OW}	10			ns	1
Output enable to output in High-Z	t_{OHZ}			40	ns	1

NOTE:

1. Active output to high-impedance and high-impedance to output active tests specified for a ±500 mV transition from steady state levels into the test load. C_{LOAD} = 5 pF.

AC TEST CONDITIONS

PARAMETER	MODE
Input voltage amplitude	0 to V_{CC}
Input rise/fall time	10 ns
Timing reference level	1.5 V
Output load conditions	1TTL + 100 pF

DATA RETENTION CHARACTERISTICS (T_A = 0 to +50°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Data retention voltage	V_{CCDR}	$\overline{CE} \geq V_{CCDR}$ - 0.2 V	2.0			V	
Data retention current	I_{CCDR}	$\overline{CE} \geq V_{CCDR}$ - 0.2 V, V_{CCDR} = 2.0 V			1.0	µA	
					0.2		1
Chip disable to data retention	t_{CDR}		0			ns	
Recovery time	t_R		t_{RC}			ns	2

NOTES:

1. T_A = 25°C
2. t_{RC} = Read cycle time

CAPACITANCE [1] (T_A = 25°C, f = 1MHz)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input capacitance	C_{IN}	V_{IN} = 0 V			7	pF
Input/output capacitance	$C_{I/O}$	$V_{I/O}$ = 0 V			10	pF

NOTE:

1. This parameter is sampled and not production tested.

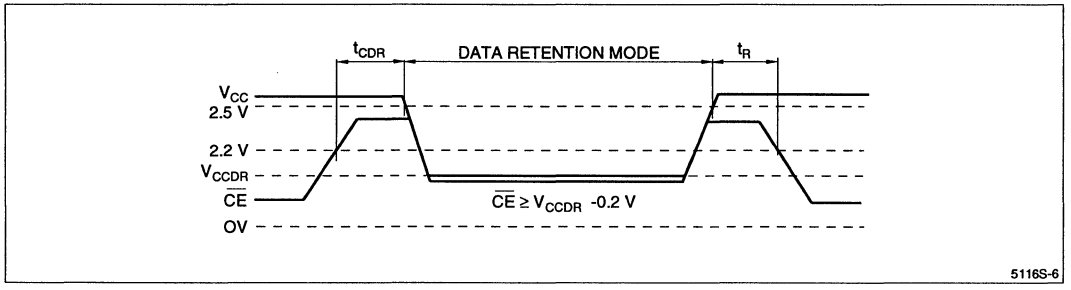


Figure 3. Low Voltage Data Retention

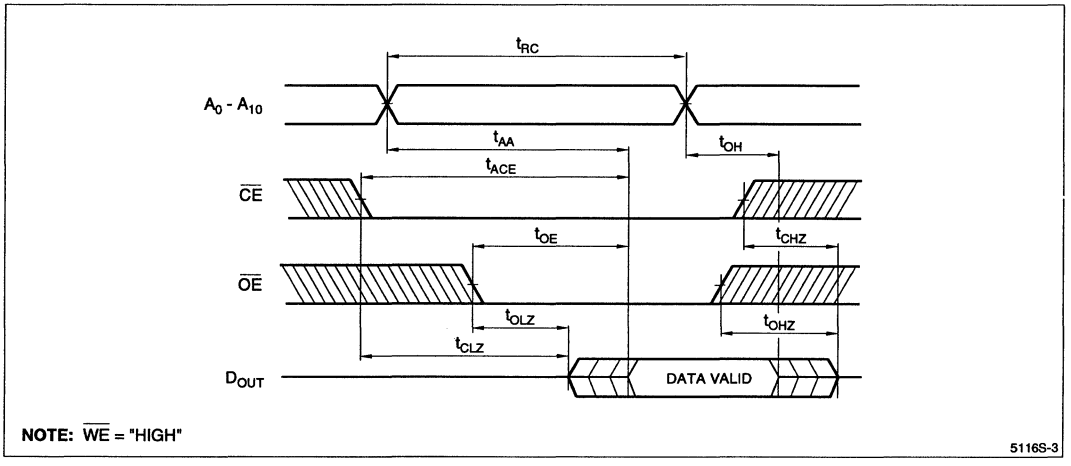
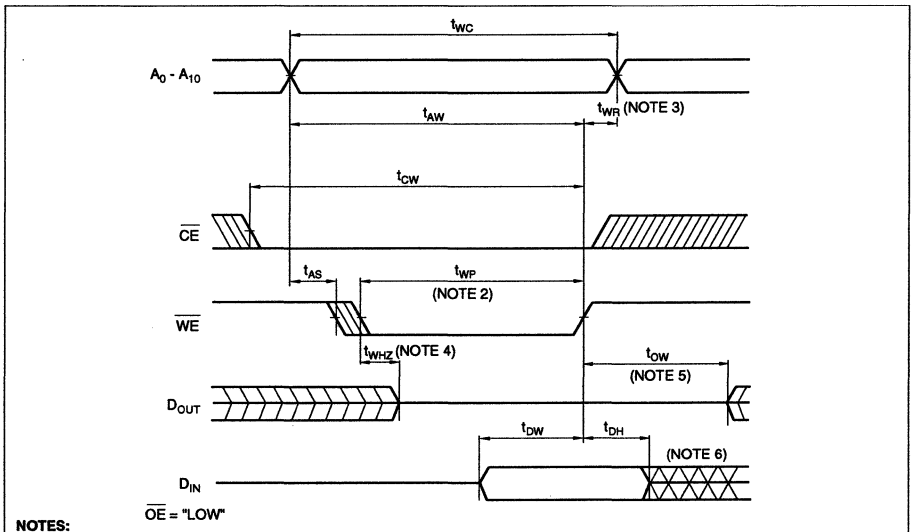


Figure 4. Read Cycle



NOTES:

1. $\overline{WE}$ must be HIGH when there is a change in A_0 - A_{10}.
2. When $\overline{CE}$ and $\overline{WE}$ are both LOW at the same time, write occurs during the period t_{WP}.
3. t_{WR} is the time from the rise of $\overline{CE}$ or $\overline{WE}$, whichever is first, to the end of the write cycle.
4. If $\overline{CE}$ LOW transition occurs at the same time or before $\overline{WE}$ LOW transition, the output will remain high-impedance.
5. D_{OUT} outputs data with the same logic level as the input data of this write cycle.
6. If $\overline{CE}$ is LOW during this period, the input/output pins are in the output state. During this state, input signals of opposite logic level must not be applied.

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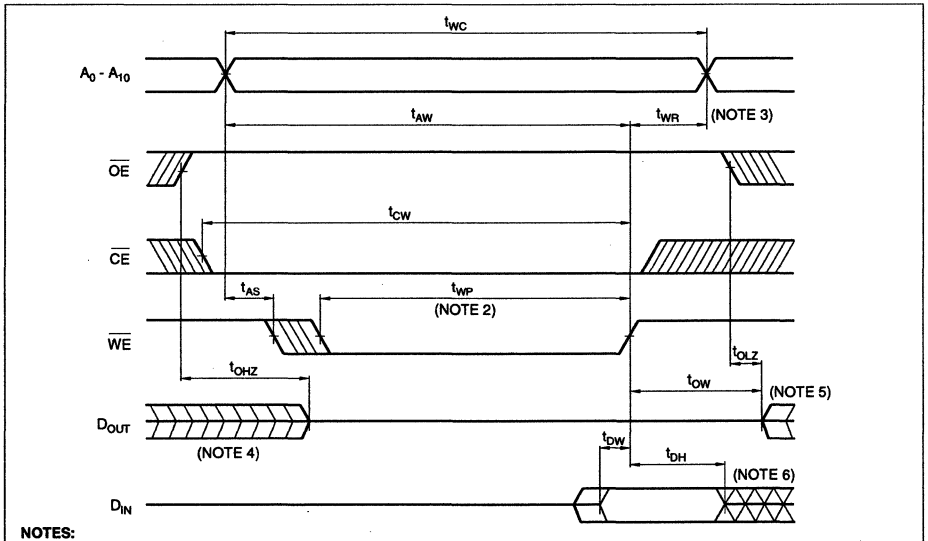
Figure 5. Write Cycle 1



NOTES:

1. $\overline{WE}$ must be HIGH when there is a change in A_0 - A_{10}.
2. When $\overline{CE}$ and $\overline{WE}$ are both LOW at the same time, write occurs during the period t_{WP}.
3. t_{WR} is the time from the rise of $\overline{CE}$ or $\overline{WE}$, whichever is first, to the end of the write cycle.
4. If $\overline{CE}$ LOW transition occurs at the same time or before $\overline{WE}$ LOW transition, the output will remain high-impedance.
5. D_{OUT} outputs data with the same logic level as the input data of this write cycle.
6. If $\overline{CE}$ and $\overline{OE}$ are LOW during this period, the input/output pins are in the output state. During this state, input signals of opposite logic level must not be applied.

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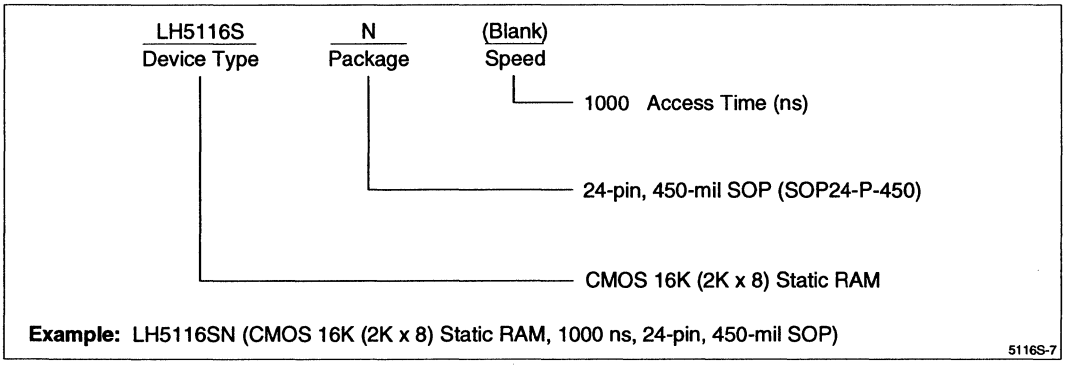
Figure 6. Write Cycle 2

ORDERING INFORMATION



LH5118

CMOS 16K (2K × 8) Static RAM

FEATURES

- 2,048 × 8 bit organization
- Access time: 100 ns (MAX.)
- Power consumption:
  Operating: 220 mW (MAX.)
  Standby: 5.5 µW (MAX.)
- Single +5 V power supply
- Fully-static operation
- TTL compatible I/O
- Three-state outputs
- Wide temperature range available
  LH5118H: -40 to +85°C
- Packages:
  24-pin, 600-mil DIP
  24-pin, 300-mil SK-DIP
  24-pin, 450-mil SOP

DESCRIPTION

The LH5118 is a static RAM organized as 2,048 × 8 bits. It is fabricated using silicon-gate CMOS process technology.

The LH5118 accepts two chip-enables. These allow data to be held with battery back-up for memory expansion (used in systems with multiple memory devices).

Low power mode (I_{SB}) is available with $\overline{CE}_1$ and $\overline{CE}_2$ deactivated.

PIN CONNECTIONS

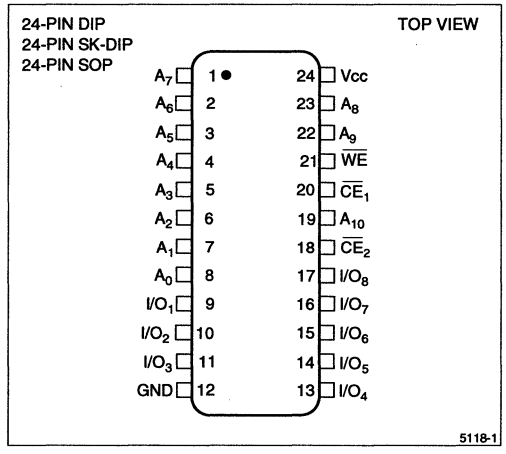


Figure 1. Pin Connections for DIP, SK-DIP, and SOP Packages

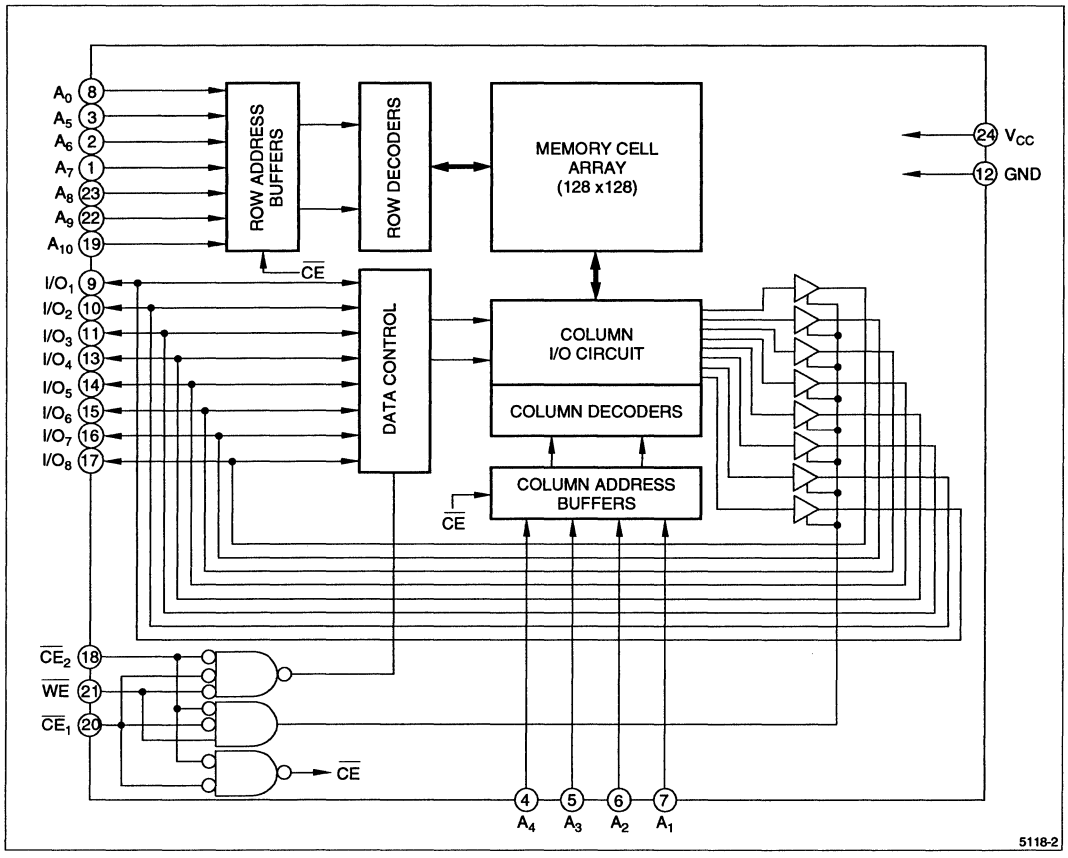


Figure 2. LH5118 Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME
A_0 - A_{10}	Address input
$\overline{CE}_2$	Chip Enable input no. 2
$\overline{CE}_1$	Chip Enable input no. 1
$\overline{WE}$	Write Enable input

SIGNAL	PIN NAME
I/O_1 - I/O_8	Data Input/Output
V_{CC}	Power supply
GND	Ground

TRUTH TABLE

$\overline{CE}_1$	$\overline{CE}_2$	$\overline{WE}$	MODE	I/O_1 - I/O_8	SUPPLY CURRENT	NOTE
X	H	X	Deselect	High-Z	Standby (I_{SB})	1
H	X	X	Deselect	High-Z	Standby (I_{SB})	1
L	L	L	Write	D_{IN}	Operating (I_{CC})	
L	L	H	Read	D_{OUT}	Operating (I_{CC})	

NOTE:
1. X = H or L

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Supply voltage	V_{CC}	-0.3 to +7.0	V	1
Input voltage	V_{IN}	-0.3 to V_{CC} + 0.3	V	1
Operating temperature	Topr	0 to +70	°C	2
		-40 to +85		3
Storage temperature	Tstg	-55 to +150	°C	

NOTES:
1. The maximum applicable voltage on any pin with respect to GND.
2. Applied to the LH5118/D/N
3. Applied to the LH5118H/HD/HN

RECOMMENDED OPERATING CONDITIONS [1]

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage	V_{IH}	2.2		V_{CC} + 0.3	V
	V_{IL}	-0.3		0.8	V

NOTE:
1. T_A = 0 to +70°C (LH5118/D/NA), T_A = -40 to +85°C (LH5118H/HD/HN)

DC CHARACTERISTICS [1] (V_{CC} = 5 V ±10%)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Output 'LOW' voltage	V_{OL}	I_{OL} = 2.1 mA			0.4	V	
Output 'HIGH' voltage	V_{OH}	I_{OH} = -1.0 mA	2.4			V	
Input leakage current	$\lvert I_{LI} \rvert$	V_{IN} = 0 V to V_{CC}			1.0	µA	
Output leakage current	$\lvert I_{LO} \rvert$	$\overline{CE}_2 = V_{IH}$ or $\overline{CE}_1 = V_{IH}$, $V_{I/O}$ = 0 V to V_{CC}			1.0	µA	
Operating current	I_{CC1}	Outputs open ($\overline{WE} = V_{CC}$)		25	30	mA	2
	I_{CC2}	Outputs open ($\overline{WE} = V_{IH}$)		30	40	mA	3
Standby current	I_{SB}	(1) $\overline{CE}_2 \geq V_{CC}$ - 0.2 V, and ($\overline{CE}_1 \geq V_{CC}$ - 0.2 V or $\overline{CE}_1 \leq$ 0.2 V) or			1.0	µA	
		(2) $\overline{CE}_1 \geq V_{CC}$ - 0.2 V, and ($\overline{CE}_2 \geq V_{CC}$ - 0.2 V or $\overline{CE}_2 \leq$ 0.2 V)			0.2	µA	4
		All other inputs = 0 V to V_{CC}					

NOTES:
1. T_A = 0 to +70°C (LH5118/D/N), T_A = -40 to +85°C (LH5118H/HD/HN)
2. $\overline{CE}_2 = \overline{CE}_1$ = 0 V; all other input pins = 0 V to V_{CC}
3. $\overline{CE}_2 = \overline{CE}_1 = V_{IL}$; all other input pins = V_{IL} to V_{IH}
4. T_A = 25°C

AC CHARACTERISTICS [1]

(1) READ CYCLE (V_{CC} = 5 V ±10%)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Read cycle time	t_{RC}	100			ns	
Address access time	t_{AA}			100	ns	
$\overline{CE}_1$ access time	t_{ACE1}			100	ns	
$\overline{CE}_2$ access time	t_{ACE2}			100	ns	
$\overline{CE}_1$ Low to output in Low-Z	t_{CLZ1}	10			ns	2
$\overline{CE}_2$ Low to output in Low-Z	t_{CLZ2}	10			ns	2
$\overline{CE}_1$ to output in High-Z	t_{CHZ1}	0		40	ns	2
$\overline{CE}_2$ to output in High-Z	t_{CHZ2}	0		40	ns	2
Data hold time	t_{OH}	10			ns	

(2) WRITE CYCLE (V_{CC} = 5 V ±10%)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Write cycle time	t_{WC}	100			ns	
Chip enable to end of write	t_{CW}	80			ns	
Address valid time	t_{AW}	80			ns	
Address setup time	t_{AS}	0			ns	
Write pulse width	t_{WP}	60			ns	
Write recovery time	t_{WR}	10			ns	
$\overline{WE}$ Low to output in High-Z	t_{WHZ}			30	ns	2
Data valid to end of write	t_{DW}	30			ns	
Data hold time	t_{DH}	10			ns	
Output active from end of write	t_{OW}	10			ns	2

NOTES:

1. T_A = 0 to +70°C (LH5118/D/N), T_A = -40 to +85°C (LH5118H/HD/HN)
2. Active output to high-impedance and high-impedance to output active tests specified for a ±500 mV transition from steady state levels into the test load. C_{LOAD} = 5 pF.

AC TEST CONDITIONS

PARAMETER	MODE
Input voltage amplitude	0.8 V to 2.2 V
Input rise/fall time	10 ns
Input reference level	1.5 V
Output load condition	1TTL + 100 pF

DATA RETENTION CHARACTERISTICS [1]

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Data retention voltage	V_{CCDR}	$\overline{CE_1} \geq V_{CCDR}$ - 0.2 V or $\overline{CE_2} \geq V_{CCDR}$ - 0.2 V	2.0			V	
Data retention current	I_{CCDR}	$\overline{CE_1} \geq V_{CCDR}$ - 0.2 V, and ($\overline{CE_2} \geq V_{CCDR}$ - 0.2 V or $\overline{CE_2} \leq$ 0.2 V) or			1.0	µA	
		$\overline{CE_2} \geq V_{CCDR}$ - 0.2 V, and ($\overline{CE_1} \geq V_{CCDR}$ - 0.2 V or $\overline{CE_1} \leq$ 0.2 V) V_{CCDR} = 3.0 V			0.2		2
Chip disable to data retention	t_{CDR}		0			ns	
Recovery time	t_R		t_{RC}			ns	3

NOTES:

1. T_A = 0 to +70°C (LH5118/D/N), T_A = -40 to +85°C (LH5118H/HD/HN)
2. T_A = 25°C
3. t_{RC} = Read cycle time

CAPACITANCE [1] (f = 1MHz, T_A = 25°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input capacitance	C_{IN}	V_{IN} = 0 V			7	pF
Input/output capacitance	$C_{I/O}$	$V_{I/O}$ = 0 V			10	pF

NOTE:

1. This parameter is sampled and not production tested.

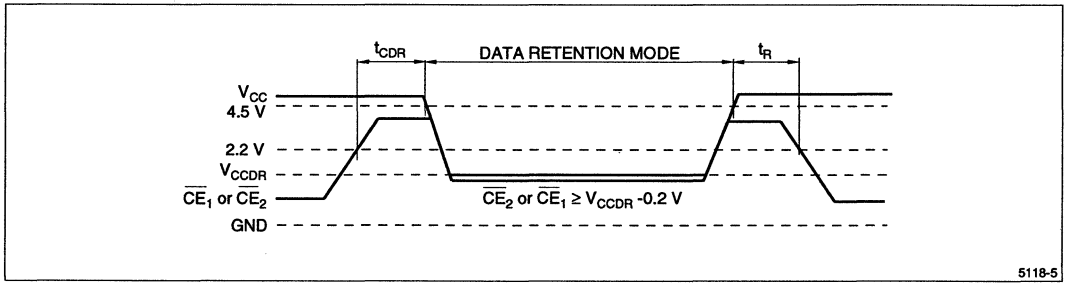
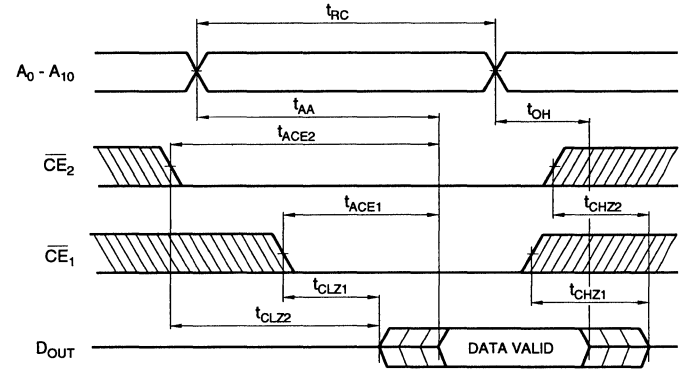


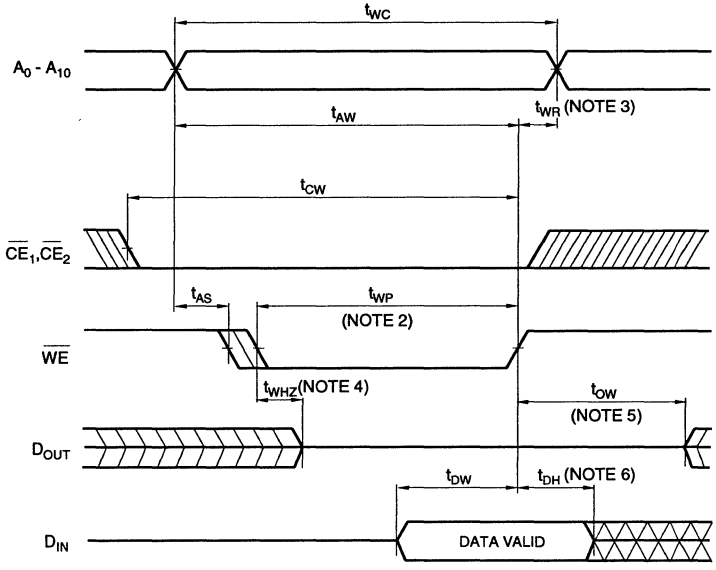
Figure 3. Low Voltage Data Retention



NOTE: $\overline{WE}$ = "HIGH"

5118-3

Figure 4. Read Cycle



NOTES:

1. $\overline{WE}$ must be HIGH when there is a change in A_0 - A_{10}.
2. When $\overline{CE}_2$,$\overline{CE}_1$ and $\overline{WE}$ are all LOW at the same time, write occurs during the period t_{WP}.
3. t_{WR} is the time from the rise of $\overline{CE}_2$,$\overline{CE}_1$ or $\overline{WE}$, whichever is first, to the end of the write cycle.
4. If $\overline{CE}_2$ or $\overline{CE}_1$ should drop at the same time as $\overline{WE}$ or later, the output buffer is maintained at high-impedance.
5. D_{OUT} outputs data with the same logic level as the input data of this write cycle.
6. If both $\overline{CE}_1$ and $\overline{CE}_2$ are LOW during this period, the input/output pin is in the output condition. During this condition, a data input signal with a logic level opposite that of the output is not permitted.

5118-4

Figure 5. Write Cycle (Note 1)

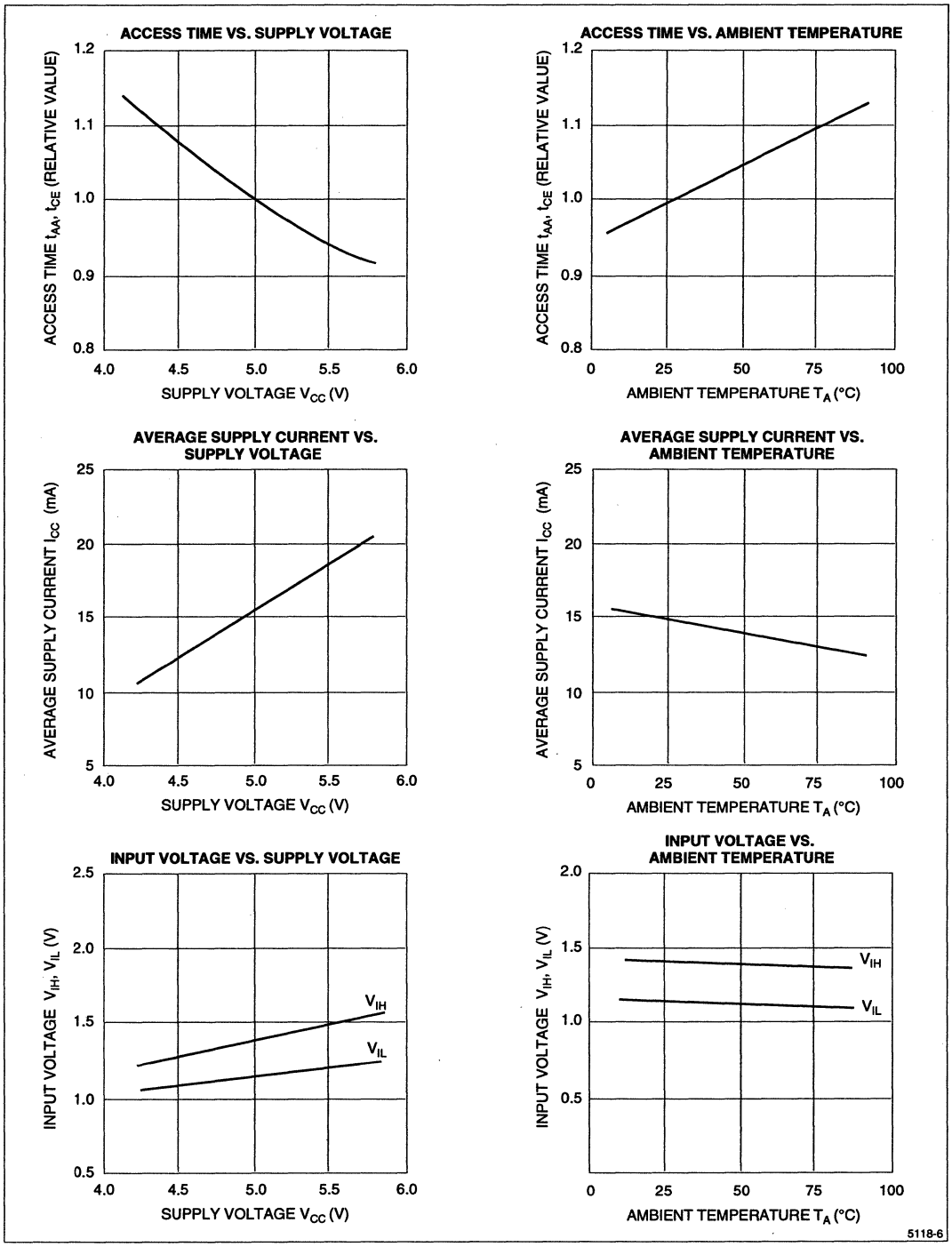
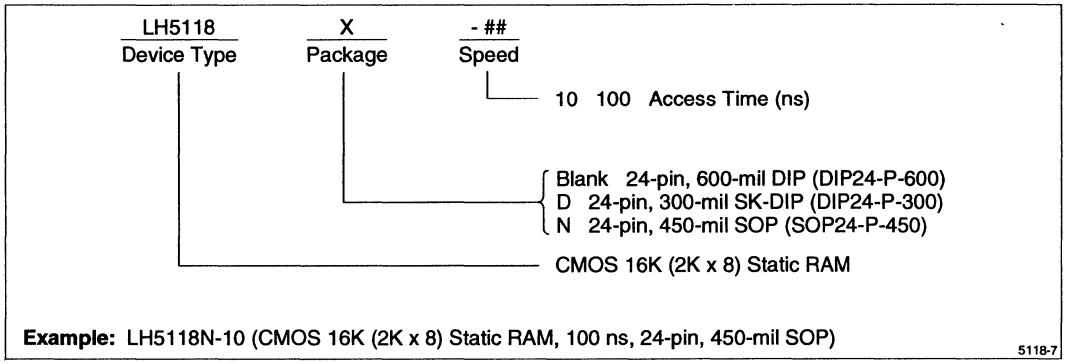
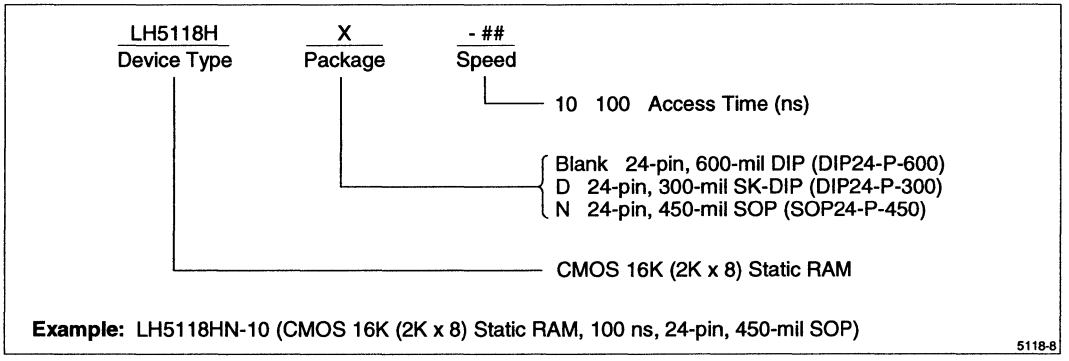


Figure 6. Electrical Characteristic Curves
(V_{CC} = 5 V, T_A = 25°C Unless Otherwise Specified)

ORDERING INFORMATION (T_A = 0 to +70°C)



ORDERING INFORMATION (T_A = -40 to +85°C)



LH5168

CMOS 64K (8K × 8) Static Ram

FEATURES

- 8,192 × 8 bit organization
- Access times: 80/100 ns (MAX.)
- Low-power consumption:
  - Operating:
    - 303 mW (MAX.) LH5168/D/N @ 80 ns
    - 248 mW (MAX.) LH5168/D/N/T/TR @ 100 ns
    - 275 mW (MAX.) LH5168H/HD/HN @ 100 ns
  - Standby:
    - 5.5 µW (MAX.) LH5168/D/N/T/TR
    - 16.5 µW (MAX.) LH5168H/HD/HN
- Fully-static operation
- Three-state outputs
- Single +5 V power supply
- TTL compatible I/O
- Pin compatible to 64K bit EPROM
- Wide temp. range available
  - LH5168: -10 to +70°C
  - LH5168H: -40 to +85°C
- Packages:
  - 28-pin, 600-mil DIP
  - 28-pin, 300-mil SK-DIP
  - 28-pin, 450-mil SOP
  - 28-pin, 8 × 13 mm^2 TSOP (Type I)

DESCRIPTION

The LH5168 is a static RAM organized as 8,192 × 8 bits. It is fabricated using silicon-gate CMOS process technology.

The LH5168H is designed for wide temperature range from -40 to +85°C.

PIN CONNECTIONS

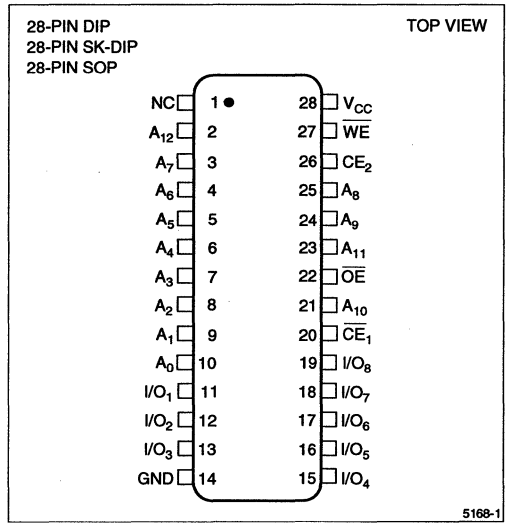


Figure 1. Pin Connections for DIP, SK-DIP, and SOP Packages

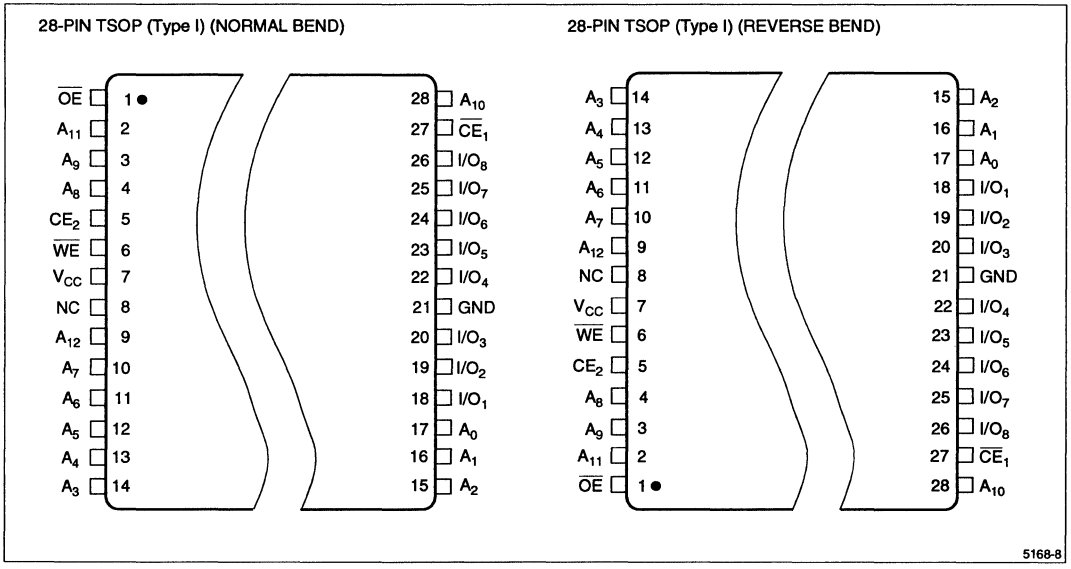


Figure 2. Pin Connections for TSOP Packages

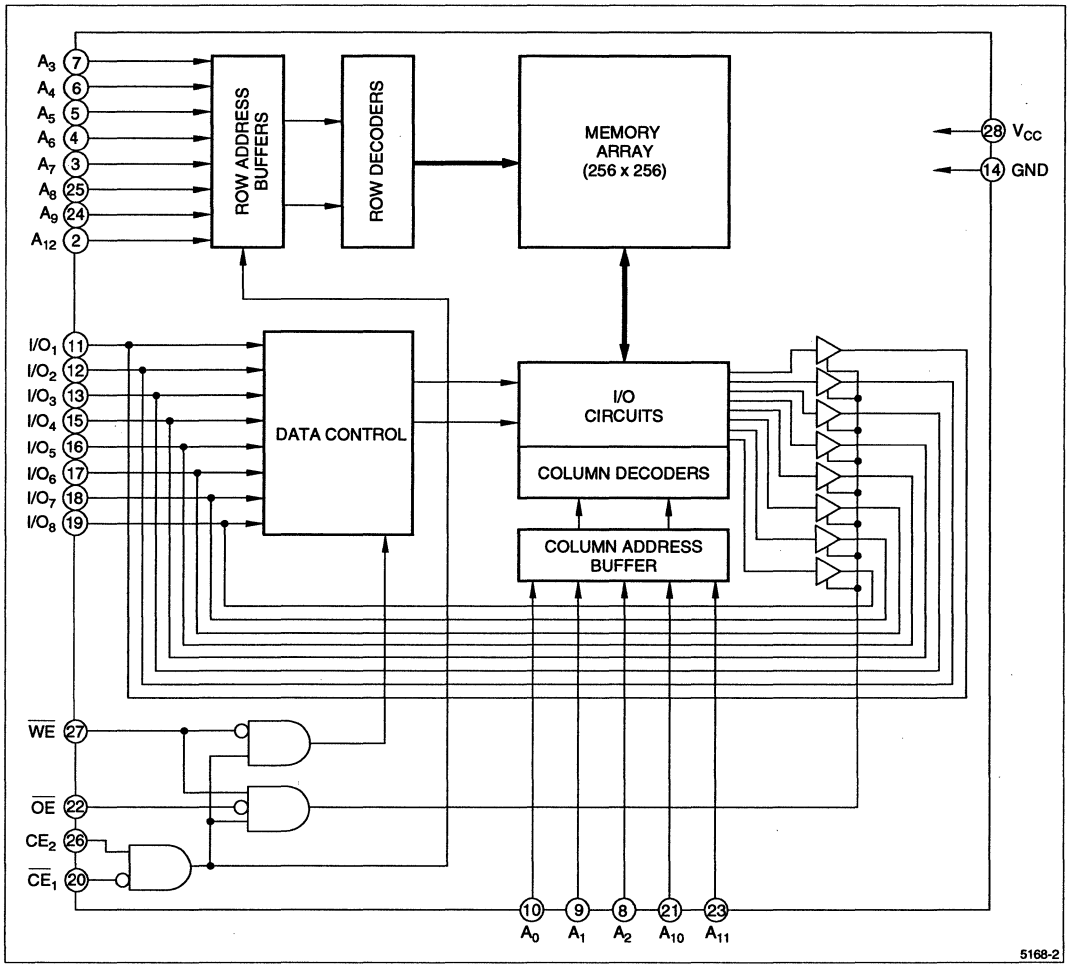


Figure 3. LH5168 Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME
A_0 - A_{12}	Address inputs
$\overline{CE_1}$ - CE_2	Chip Enable input
$\overline{WE}$	Write Enable input
$\overline{OE}$	Output Enable input

SIGNAL	PIN NAME
I/O_1 - I/O_8	Data inputs and outputs
V_{CC}	Power supply
GND	Ground
NC	Non-connection

TRUTH TABLE

$\overline{CE_1}$	CE_2	$\overline{WE}$	$\overline{OE}$	MODE	I/O_1 - I/O_8	SUPPLY CURRENT	NOTE
H	X	X	X	Deselect	High-Z	Standby (I_{SB})	1
X	L	X	X	Deselect	High-Z	Standby (I_{SB})	1
L	H	L	X	Write	D_{IN}	Operating (I_{CC})	
L	H	H	L	Read	D_{OUT}	Operating (I_{CC})	
L	H	H	H	Output disable	High-Z	Operating (I_{CC})	

NOTE:
1. X = H or L

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	80 ns RATING	100 ns RATING	UNIT	NOTE
Supply voltage	V_{CC}	-0.3 to +7.0	-0.3 to +7.0	V	1
Input voltage	V_{IN}	-0.5 to V_{CC} +0.5	-0.3 to V_{CC} +0.3	V	1
Operating temperature	Topr	-10 to +70	-10 to +70	°C	2
			-40 to +85	°C	3
Storage temperature	Tstg	-55 to +150	-55 to +150	°C	

NOTES:
1. The maximum applicable voltage on any pin with respect to GND.
2. LH5168/D/N
3. LH5168H/HD/HN

RECOMMENDED OPERATING CONDITIONS (Note 1)

PARAMETER	SYMBOL	80 ns			100 ns			UNIT
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply voltage	V_{CC}	4.5	5.0	5.5	4.5	5.0	5.5	V
Input voltage	V_{IH}	2.2		V_{CC} + 0.5	2.2		V_{CC} + 0.3	V
	V_{IL}	-0.5		0.8	-0.3		0.8	V

NOTE:
1. T_A = -10 to +70°C (LH5168/D/N), T_A = -40 to +85°C (LH5168H/HD/HN).

DC CHARACTERISTICS [1] (V_{CC} = 5 V ±10%)

PARAMETER	SYMBOL	CONDITIONS		MIN.	MAX.	UNIT	NOTE
Input leakage current	I_{LI}	V_{IN} = 0 to V_{CC}			1.0	µA	
Output leakage current	I_{LO}	$\overline{CE_1}$ = V_{IH} or CE_2 = V_{IL} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL} $V_{I/O}$ = 0 to V_{CC}			1.0	µA	
Operating current	I_{CC}	$\overline{CE_1}$ = V_{IL}, V_{IN} = V_{IL} to V_{IH} CE_2 = V_{IH}, Outputs open	t_{CYCLE} = 80 ns		55	mA	
		$\overline{CE_1}$ = V_{IL}, V_{IN} = V_{IL} to V_{IH} CE_2 = V_{IH}, Outputs open	t_{CYCLE} = 100 ns		45	mA	2
					50		3
		$\overline{CE_1}$ = V_{IL}, V_{IN} = 0.2 V to V_{CC} - 0.2 V CE_2 = V_{IH}, Outputs open	t_{CYCLE} = 1.0 µs		10		
Standby current	I_{SB1}	$\overline{CE_1}$ = V_{IH} or CE_2 = V_{IL}			10	mA	
	I_{SB}	CE_2 ≤ 0.2 V or $\overline{CE_1}$, CE_2 ≥ V_{CC} - 0.2 V	T_A ≤ 70°C		1.0	µA	2
			T_A ≤ 85°C		3.0	µA	3
Output voltage	V_{OL}	I_{OL} = 2.1 mA			0.4	V	
	V_{OH}	I_{OH} = -1 mA		2.4		V	

NOTES:
1. T_A = -10 to 70°C (LH5168/D/N/T/TR), T_A = -40 to +85°C (LH5168H/HD/HN)
2. LH5168/D/N/T/TR
3. LH5168H/HD/HN

AC CHARACTERISTICS [1]

(1) READ CYCLE (V_{CC} = 5 V ±10%)

PARAMETER		SYMBOL	80 ns		100 ns		UNIT	NOTE
			MIN.	MAX.	MIN.	MAX.		
Read cycle		t_{RC}	80		100		ns	
Address access time		t_{AA}		80		100	ns	
Chip enable access time	($\overline{CE}_1$)	t_{ACE1}		80		100	ns	
	(CE_2)	t_{ACE2}		80		100	ns	
Output enable access time		t_{OE}		40		40	ns	
Output hold time		t_{OH}	10		10		ns	
Chip enable to output in Low-Z	($\overline{CE}_1$)	t_{LZ1}	10		10		ns	2
	(CE_2)	t_{LZ2}	10		10		ns	2
Output enable to output in Low-Z		t_{OLZ}	5		5		ns	2
Chip enable to output in High-Z	($\overline{CE}_1$)	t_{HZ1}	0	30	0	30	ns	2
	(CE_2)	t_{HZ2}	0	30	0	30	ns	2
Output disable to output in High-Z		t_{OHZ}	0	20	0	20	ns	2

NOTES:

1. T_A = -10 to +70°C (LH5168/D/N/T/TR), T_A = -40 to +85°C (LH5168H/HD/HN)
2. Active output to high-impedance and high-impedance to output active tests specified for a ±500 mV transition from steady state levels into the test load. C_{LOAD} = 5 pF.

(2) WRITE CYCLE (V_{CC} = 5 V ±10%)

PARAMETER	SYMBOL	80 ns		100 ns		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.		
Write cycle time	t_{WC}	80		100		ns	
Chip enable to end of write	t_{CW}	70		80		ns	
Address valid to end of write	t_{AW}	70		80		ns	
Address setup time	t_{AS}	0		0		ns	
Write pulse width	t_{WP}	60		60		ns	
Write recovery time	t_{WR}	0		0		ns	
Data valid to end of write	t_{DW}	40		40		ns	
Data hold time	t_{DH}	0		0		ns	
Output active from end of write	t_{OW}	10		10		ns	1
$\overline{WE}$ to output in High-Z	t_{WZ}	0	30	0	30	ns	1
$\overline{OE}$ to output in High-Z	t_{OHZ}	0	20	0	20	ns	1

NOTE:

1. Active output to high-impedance and high-impedance to output active tests specified for a ±500 mV transition from steady state levels into the test load. C_{LOAD} = 5 pF.

AC TEST CONDITIONS

PARAMETER	MODE
Input voltage amplitude	0.6 to 2.4 V
Input rise/fall time	10 ns
Timing reference level	1.5 V
Output load conditions	(1TTL + C_L = 100 pF)

CAPACITANCE [1] (T_A = 25°C, f = 1MHz)

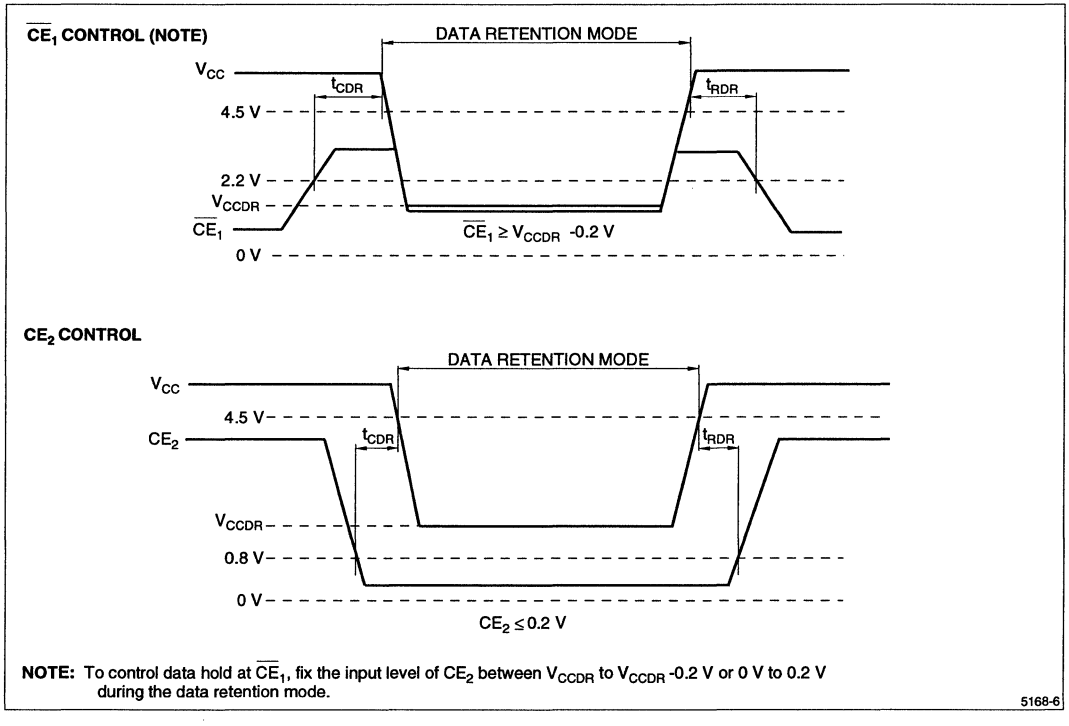
PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input capacitance	C_{IN}	V_{IN} = 0 V			7	pF
Input/output capacitance	$C_{I/O}$	$V_{I/O}$ = 0 V			10	pF

NOTE:
1. This parameter is sampled and not production tested.

DATA RETENTION CHARACTERISTICS [1]

PARAMETER	SYMBOL	CONDITIONS	MIN.	MAX.	UNIT	NOTE
Data retention voltage	V_{CCDR}	$CE_2 \le 0.2$ V or $\overline{CE}_1$, $CE_2 \ge V_{CC}$ - 0.2 V	2.0		V	
Data retention current	I_{CCDR}	V_{CCDR} = 3 V, $CE_2 \le 0.2$ V or $\overline{CE}_1$, $CE_2 \ge V_{CCDR}$ - 0.2 V		0.6	µA	2
				1.5	µA	3
Chip disable to data retention	t_{CDR}		0		ns	
Recovery time	t_{RDR}		t_{RC}		ns	4

NOTES:
1. T_A = -10 to +70°C (LH5168/D/N/T/TR), T_A = -40 to +85°C (LH5168H/HD/HN)
2. LH5168/D/N/T/TR at $T_A \le 70$°C
3. LH5168H/HD/HN at $T_A \le 85$°C
4. t_{RC} = Read cycle time



NOTE: To control data hold at $\overline{CE}_1$, fix the input level of CE_2 between V_{CCDR} to V_{CCDR} -0.2 V or 0 V to 0.2 V during the data retention mode.

5168-6

Figure 4. Low Voltage Data Retention

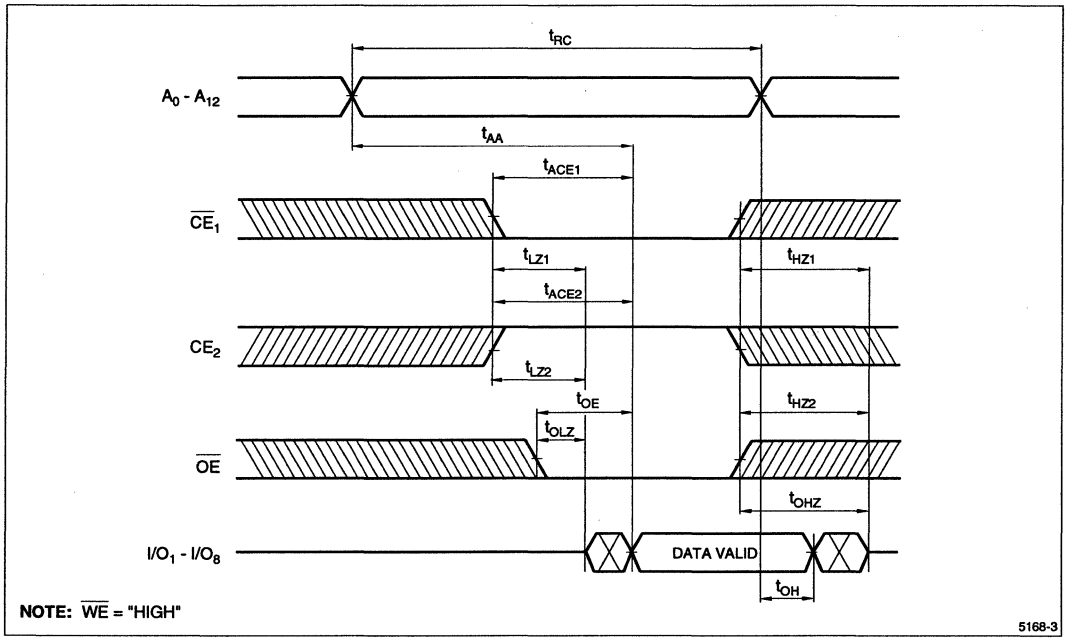
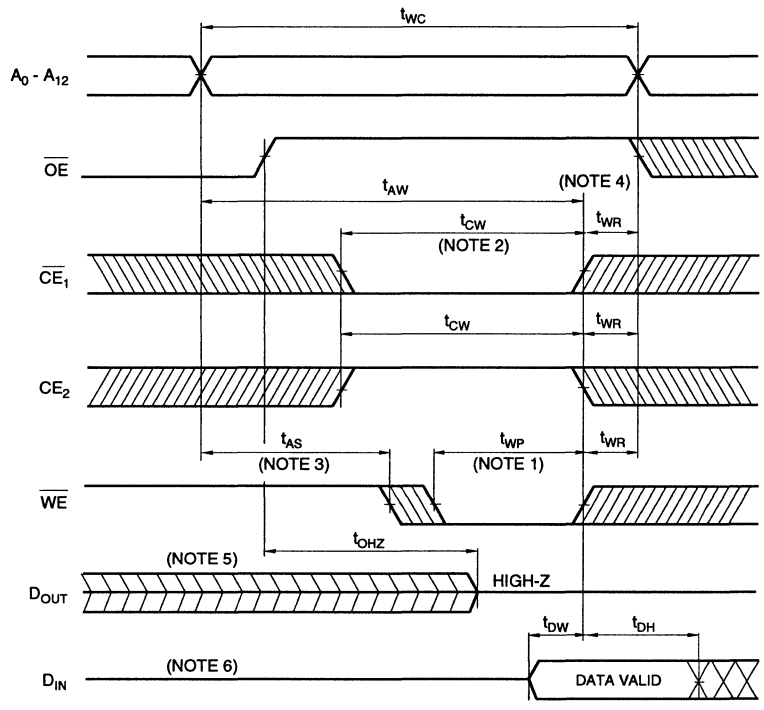


Figure 5. Read Cycle

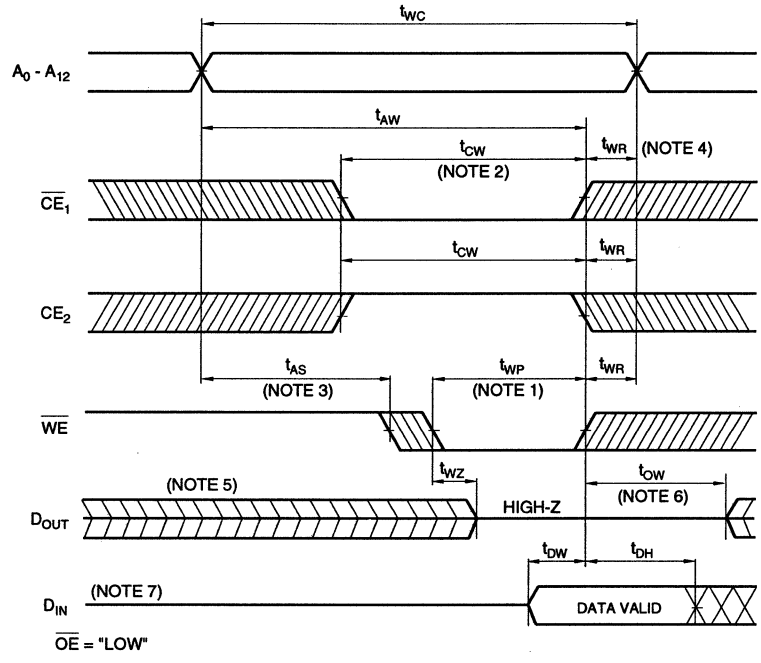


NOTES:

1. The writing occurs during the overlap (t_{WP}) of $\overline{CE_1}$ ="LOW", CE_2 = "HIGH", and $\overline{WE}$ = "LOW".
2. t_{CW} is defined as the time from the last occuring transition, either $\overline{CE_1}$ LOW transition or CE_2 HIGH transition, to the time when the writing is finished.
3. t_{AS} is defined as the time from address change to writing start.
4. t_{WR} is defined as the time from writing finish to address change.
5. If $\overline{CE_1}$ LOW transition or CE_2 HIGH transition occurs at the same time or after $\overline{WE}$ LOW transition, the output will remain high-impedance.
6. While the I/O pins are in the output state, input signals with the opposite logic level must not be applied.

5168-4

Figure 6. Write Cycle 1



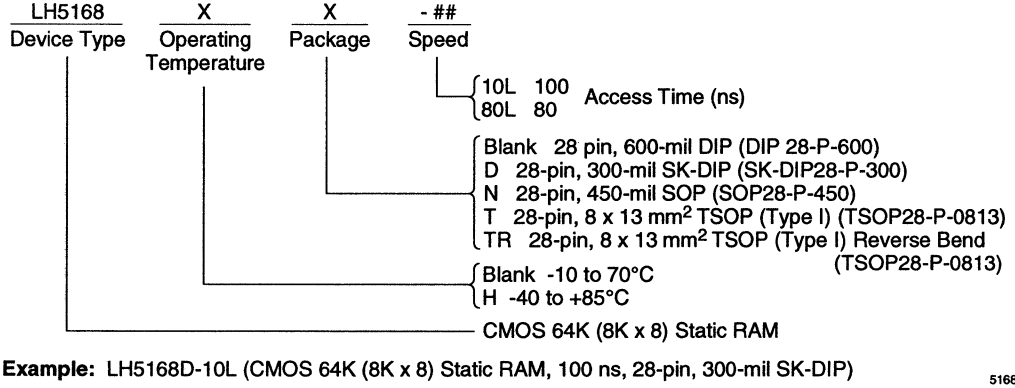
NOTES:

1. The writing occurs during the overlap (t_{WP}) of $\overline{CE_1}$ ="LOW", CE_2 = "HIGH", and $\overline{WE}$ = "LOW".
2. t_{CW} is defined as the time from the last occuring transition, either $\overline{CE_1}$ LOW transition or CE_2 HIGH transition, to the time when the writing is finished.
3. t_{AS} is defined as the time from address change to writing start.
4. t_{WR} is defined as the time from writing finish to address change.
5. If $\overline{CE_1}$ LOW transition or CE_2 HIGH transition occurs at the same time or after $\overline{WE}$ LOW transition, the output will remain high-impedance.
6. If $\overline{CE_1}$ HIGH transition or CE_2 LOW transition occurs at the same time or before $\overline{WE}$ HIGH transition, the output will remain high-impedance.
7. While the I/O pins are in the output state, input signals with the opposite logic level must not be applied.

5168-5

Figure 7. Write Cycle 2

ORDERING INFORMATION



Example: LH5168D-10L (CMOS 64K (8K x 8) Static RAM, 100 ns, 28-pin, 300-mil SK-DIP)

5168-7

LH5168SH

CMOS 64K (8K × 8) Static Ram

FEATURES

- 8,192 × 8 bit organization
- Access time: 500 ns (MAX.)
- Power consumption:
  Operating:
  60 mW (MAX.) @ 3 V
  Standby:
  3 µW (MAX.) @ 70°C @ 3 V
  9 µW (MAX.) @ 85°C @ 3 V
- Fully-static operation
- Three-state outputs
- Single 2.5 to 5.5 V power supply
- TTL compatible I/O
- Wide temp. range
  t_{OPR}: -40 to +85°C
- Package: 28-pin, 450-mil SOP

DESCRIPTION

The LH5168SH is a static RAM organized as 8,192 × 8 bits. It is fabricated using silicon-gate CMOS process technology.

It is designed for 2.5 to 5.5 V low voltage operation and wide temperature range from -40 to +85°C.

PIN CONNECTIONS

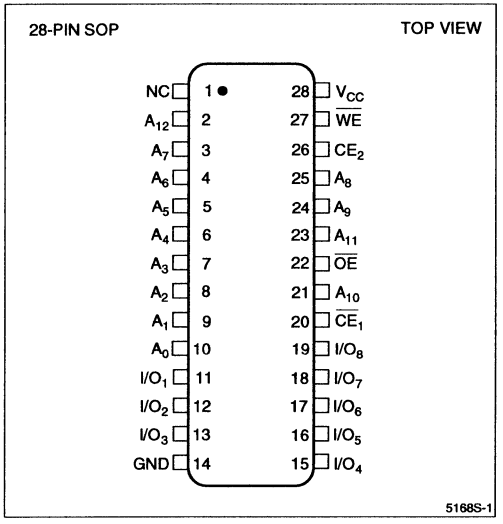


Figure 1. Pin Connections for SOP Package

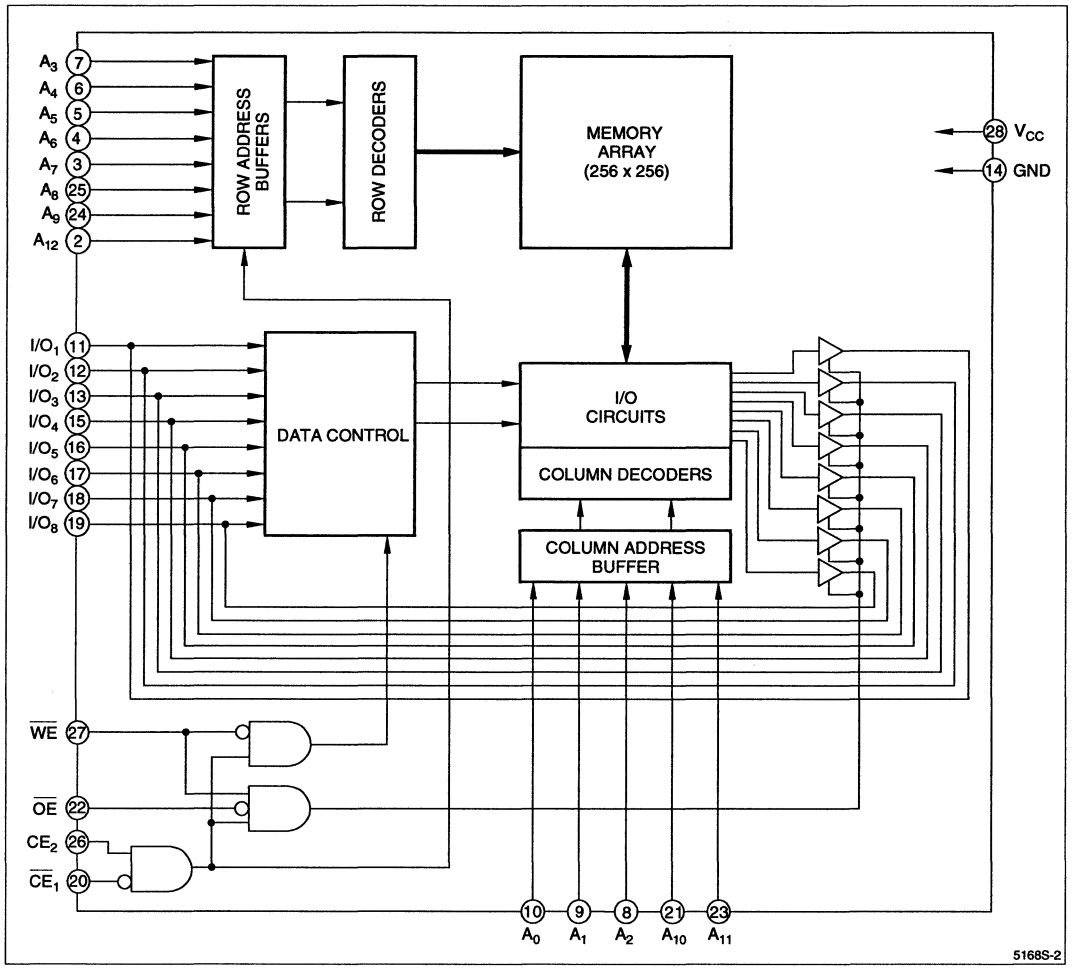


Figure 2. LH5168SH Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME
A_0 - A_{12}	Address inputs
$\overline{CE}_1$ - CE_2	Chip Enable input
$\overline{WE}$	Write Enable input
$\overline{OE}$	Output Enable input

SIGNAL	PIN NAME
I/O_1 - I/O_8	Data inputs and outputs
V_{CC}	Power supply
GND	Ground
NC	Non connection

TRUTH TABLE

$\overline{CE_1}$	CE_2	$\overline{WE}$	$\overline{OE}$	MODE	I/O_1 - I/O_8	SUPPLY CURRENT	NOTE
H	X	X	X	Deselect	High-Z	Standby (I_{SB})	1
X	L	X	X	Deselect	High-Z	Standby (I_{SB})	1
L	H	L	X	Write	D_{IN}	Operating (I_{CC})	
L	H	H	L	Read	D_{OUT}	Operating (I_{CC})	
L	H	H	H	Output disable	High-Z	Operating (I_{CC})	

NOTE:
1. X = H or L

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Supply voltage	V_{CC}	-0.3 to +7.0	V	1
Input voltage	V_{IN}	-0.3 to V_{CC} +0.3	V	1
Operating temperature	Topr	-40 to +85	°C	
Storage temperature	Tstg	-55 to +150	°C	

NOTE:
1. The maximum applicable voltage on any pin with respect to GND.

RECOMMENDED OPERATING CONDITIONS (T_A = -40 to +85°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	2.5	3.0	5.5	V
Input voltage (V_{CC} = 2.5 to 4.5 V)	V_{IH}	V_{CC} - 0.2		V_{CC} + 0.3	V
	V_{IL}	-0.3		0.2	V
Input voltage (V_{CC} = 4.5 to 5.5 V)	V_{IH}	2.2		V_{CC} + 0.3	V
	V_{IL}	-0.3		0.8	V

DC CHARACTERISTICS (T_A = -40 to +85°C, V_{CC} = 2.5 to 5.5 V)

PARAMETER	SYMBOL	CONDITIONS		MIN.	MAX.	UNIT	NOTE
Input leakage current	$\lvert I_{LI} \rvert$	V_{IN} = 0 to V_{CC}		-1.0	1.0	µA	
Output leakage current	$\lvert I_{LO} \rvert$	$\overline{CE_1}$ = V_{IH} or CE_2 = V_{IL} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL} $V_{I/O}$ = 0 to V_{CC}		-1.0	1.0	µA	
Operating supply current	I_{CC}	$\overline{CE_1}$ = 0.2 V, V_{IN} = 0.2 V or V_{CC} - 0.2 V CE_2 = V_{CC} - 0.2 V, Output open	t_{CYCLE} = 500 ns		20	mA	
		$\overline{CE_1}$ = 0.2 V, V_{IN} = 0.2 V or V_{CC} - 0.2 V CE_2 = V_{CC} - 0.2 V, Output open	t_{CYCLE} = 1.0 µs		10		
		$\overline{CE_1}$ = 0.2 V, V_{IN} = 0.2 V or V_{CC} - 0.2 V CE_2 = V_{CC} - 0.2 V, Output open, V_{CC} = 3.3 V	t_{CYCLE} = 1.0 µs		8		
Standby current	I_{SB}	CE_2 ≤ 0.2 V or $\overline{CE_1}$ ≥ V_{CC} - 0.2 V	~ +70°C		1.0	µA	
			~ +85°C		3.0		1
	I_{SB1}	$\overline{CE_1}$ = V_{IH} or CE_2 = V_{IL}			5	mA	
Output Low voltage	V_{OL}	I_{OL} = 500 µA			0.5	V	
Output High voltage	V_{OH}	I_{OH} = -500 µA		V_{CC} - 0.5		V	2

NOTES:
1. CE_2 should be ≥ V_{CC} - 0.2 V or ≤ 0.2 V.
2. V_{OH} is 4.5 V (Min.) at V_{CC} > 5 V.

AC CHARACTERISTICS

(1) READ CYCLE (T_A = -40 to +85°C, V_{CC} = 2.5 to 5.5 V)

PARAMETER		SYMBOL	MIN.	MAX.	UNIT	NOTE
Read cycle		t_{RC}	500		ns	
Address access time		t_{AA}		500	ns	
Chip enable access time	($\overline{CE}_1$)	t_{ACE1}		500	ns	
	(CE_2)	t_{ACE2}		500	ns	
Output enable access time		t_{OE}		200	ns	
Output hold time		t_{OH}	10		ns	
Chip enable to output in Low-Z	($\overline{CE}_1$)	t_{LZ1}	20		ns	1
	(CE_2)	t_{LZ2}	20		ns	1
Output enable to output in Low-Z		t_{OLZ}	10		ns	1
Chip enable to output in High-Z	($\overline{CE}_1$)	t_{HZ1}	0	60	ns	1
	(CE_2)	t_{HZ2}	0	60	ns	1
Output disable to output in High-Z		t_{OHZ}	0	40	ns	1

(2) WRITE CYCLE (T_A = -40 to +85°C, V_{CC} = 2.5 to 5.5 V)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT	NOTE
Write cycle time	t_{WC}	500		ns	
Chip enable to end of write	t_{CW}	250		ns	
Address valid to end of write	t_{AW}	250		ns	
Address setup time	t_{AS}	100		ns	
Write pulse width	t_{WP}	150		ns	
Write recovery time	t_{WR}	50		ns	
Data valid to end of write	t_{DW}	100		ns	
Data hold time	t_{DH}	0		ns	
Output active from end of write	t_{OW}	20		ns	
$\overline{WE}$ to output in High-Z	t_{WZ}	0	60	ns	1
$\overline{OE}$ to output in High-Z	t_{OHZ}	0	40	ns	1

NOTE:

1. Active output to high-impedance and high-impedance to output active tests specified for a ±500 mV transition from steady state levels into the test load. C_{LOAD} = 5 pF.

AC TEST CONDITIONS

PARAMETER	MODE
Input voltage amplitude	0 to V_{CC}
Input rise/fall time	10 ns
Timing reference level	1.5 V
Output load conditions	No load

CAPACITANCE (T_A = 25°C, f = 1MHz)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input capacitance	C_{IN}	V_{IN} = 0 V			7	pF
Input/output capacitance	$C_{I/O}$	$V_{I/O}$ = 0 V			10	pF

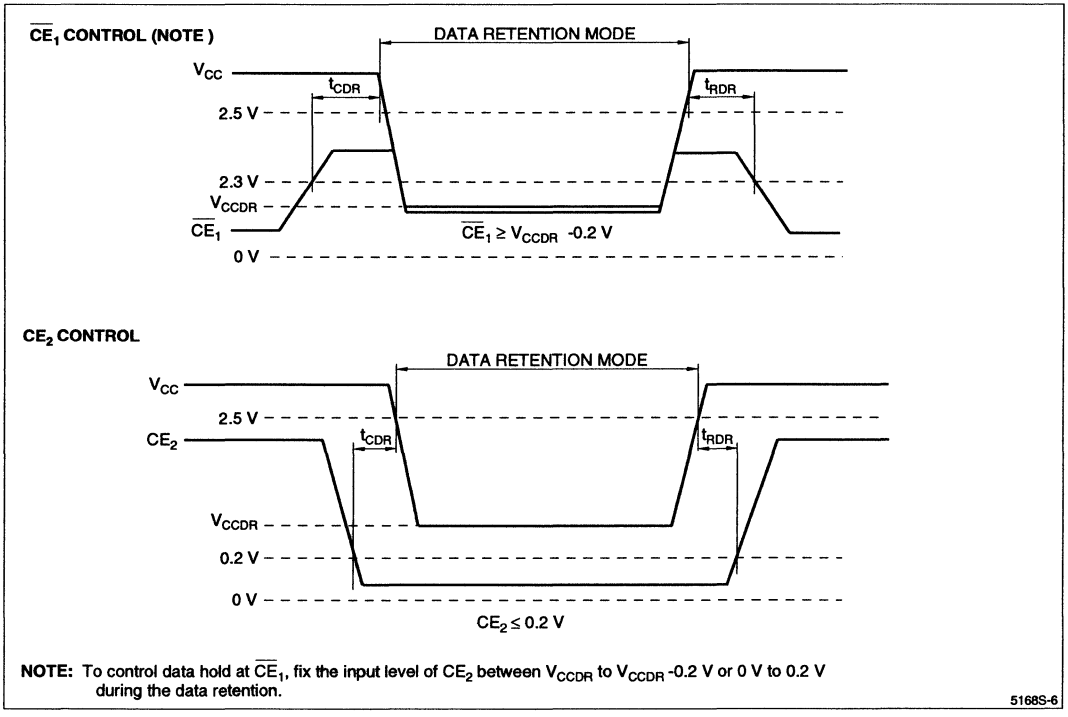
NOTE:

This parameter is sampled and not production tested.

DATA RETENTION CHARACTERISTICS (T_A = -40 to +85°C)

PARAMETER	SYMBOL	CONDITIONS		MIN.	MAX.	UNIT	NOTE
Data retention voltage	V_{CCDR}	$CE_2 \le 0.2$ V or $\overline{CE_1} \ge V_{CCDR}$ - 0.2 V		2.0		V	1
Data retention current	I_{CCDR}	V_{CCDR} = 3.0 V	T_A = 25°C		0.2	µA	
		$CE_2 \le 0.2$ V or	T_A = 70°C		0.6		
		$\overline{CE_1} \ge V_{CCDR}$ - 0.2 V			1.5		1
Chip disable to data retention	t_{CDR}			0		ns	
Recovery time	t_{RDR}			t_{RC}		ns	2

NOTES:
1. CE_2 should be ≥ V_{CCDR} - 0.2 V or ≤ 0.2 V.
2. t_{RC} = Read cycle time



NOTE: To control data hold at $\overline{CE_1}$, fix the input level of CE_2 between V_{CCDR} to V_{CCDR} -0.2 V or 0 V to 0.2 V during the data retention.

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Figure 3. Low Voltage Data Retention

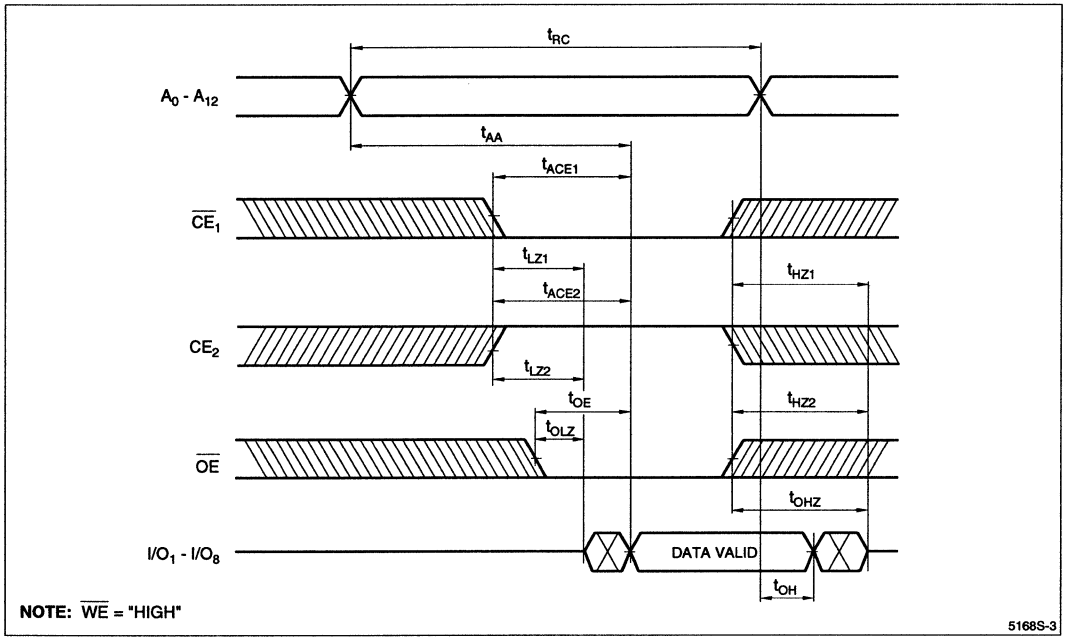
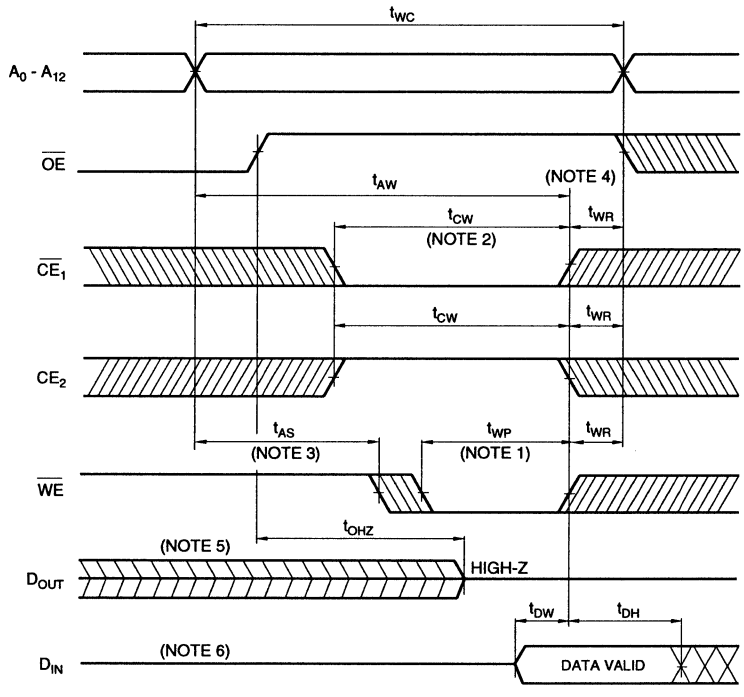


Figure 4. Read Cycle



NOTES:

1. The writing occurs during the overlap (t_{WP}) of $\overline{CE_1}$ ="LOW", CE_2 = "HIGH", and $\overline{WE}$ = "LOW".
2. t_{CW} is defined as the time from the last occuring transition, either $\overline{CE_1}$ LOW transition or CE_2 HIGH transition, to the time when the writing is finished.
3. t_{AS} is defined as the time from address change to writing start.
4. t_{WR} is defined as the time from writing finish to address change.
5. If $\overline{CE_1}$ LOW transition or CE_2 HIGH transition occurs at the same time or after $\overline{WE}$ LOW transition, the output will remain high-impedance.
6. While the I/O pins are in the output state, input signals with the opposite logic level must not be applied.

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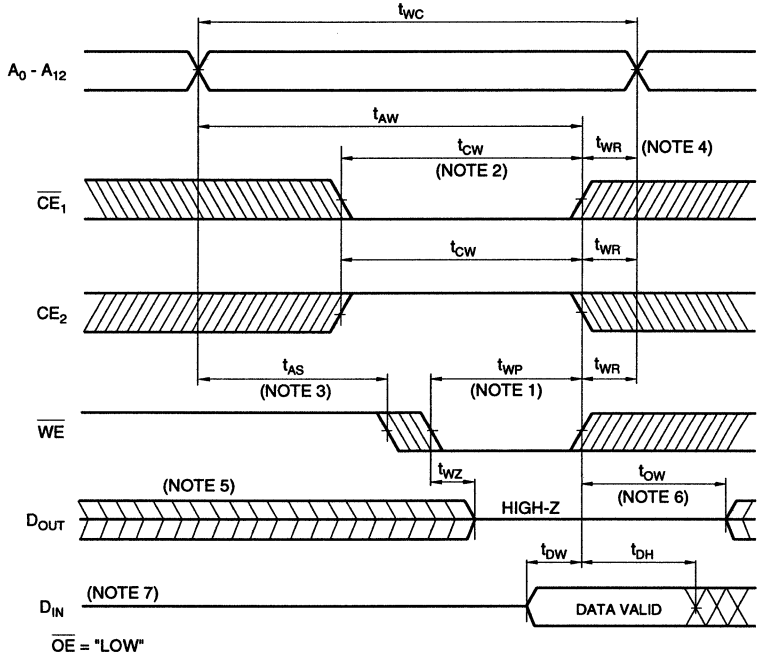
Figure 5. Write Cycle 1



NOTES:

1. The writing occurs during the overlap (t_{WP}) of $\overline{CE_1}$ ="LOW", CE_2 = "HIGH", and $\overline{WE}$ = "LOW".
2. t_{CW} is defined as the time from the last occuring transition, either $\overline{CE_1}$ LOW transition or CE_2 HIGH transition, to the time when the writing is finished.
3. t_{AS} is defined as the time from address change to writing start.
4. t_{WR} is defined as the time from writing finish to address change.
5. If $\overline{CE_1}$ LOW transition or CE_2 HIGH transition occurs at the same time or after $\overline{WE}$ LOW transition, the output will remain high-impedance.
6. If $\overline{CE_1}$ HIGH transition or CE_2 LOW transition occurs at the same time or before $\overline{WE}$ HIGH transition, the output will remain high-impedance.
7. While the I/O pins are in the output state, input signals with the opposite logic level must not be applied.

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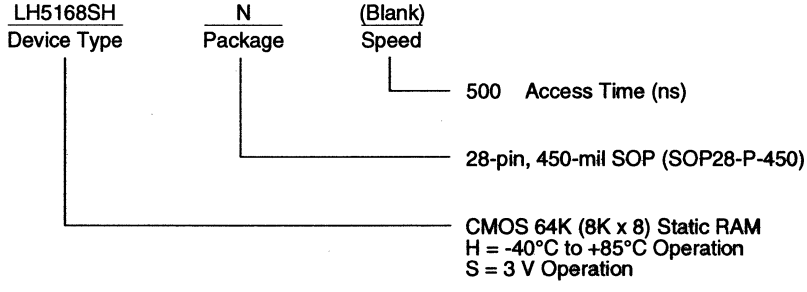
Figure 6. Write Cycle 2

ORDERING INFORMATION



Example: LH5168SHN (CMOS 64K (8K x 8) Static RAM, 500 ns, 28-pin, 450-mil SOP)

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LH5168ST

CMOS 64K (8K × 8) Static RAM

FEATURES

- 8,192 × 8 bit organization
- Access times:
  500 ns (MAX.)
- Power consumption:
  Operating:
  60 mW (MAX.) @ 3 V
  Standby:
  3 µW (MAX.) @ 3 V
  Data hold
  0.2 µA (V_{CC} = 3 V, T_A = 25°C)
- Wide operating voltage range:
  2.5 V to 5.5 V
- Fully-static operation
- TTL compatible I/O
- Three-state outputs
- Operating temperature:
  -10 to +70°C
- Package: 28-pin, 8 × 13 mm^2 TSOP (Type I)

DESCRIPTION

The LH5168ST is a static RAM organized as 8,192 × 8 bits. It is fabricated using silicon-gate CMOS process technology.

PIN CONNECTIONS

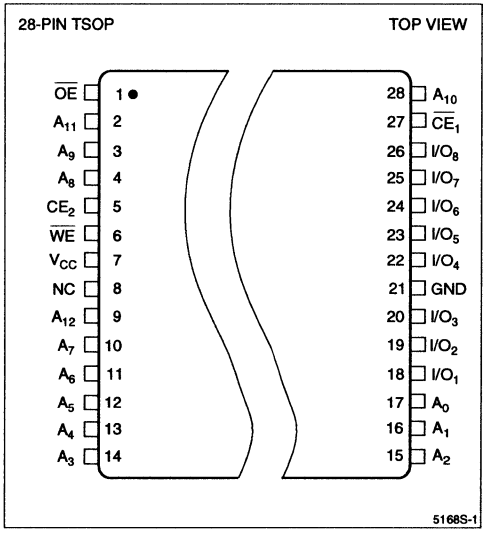


Figure 1. Pin Connections for TSOP Package

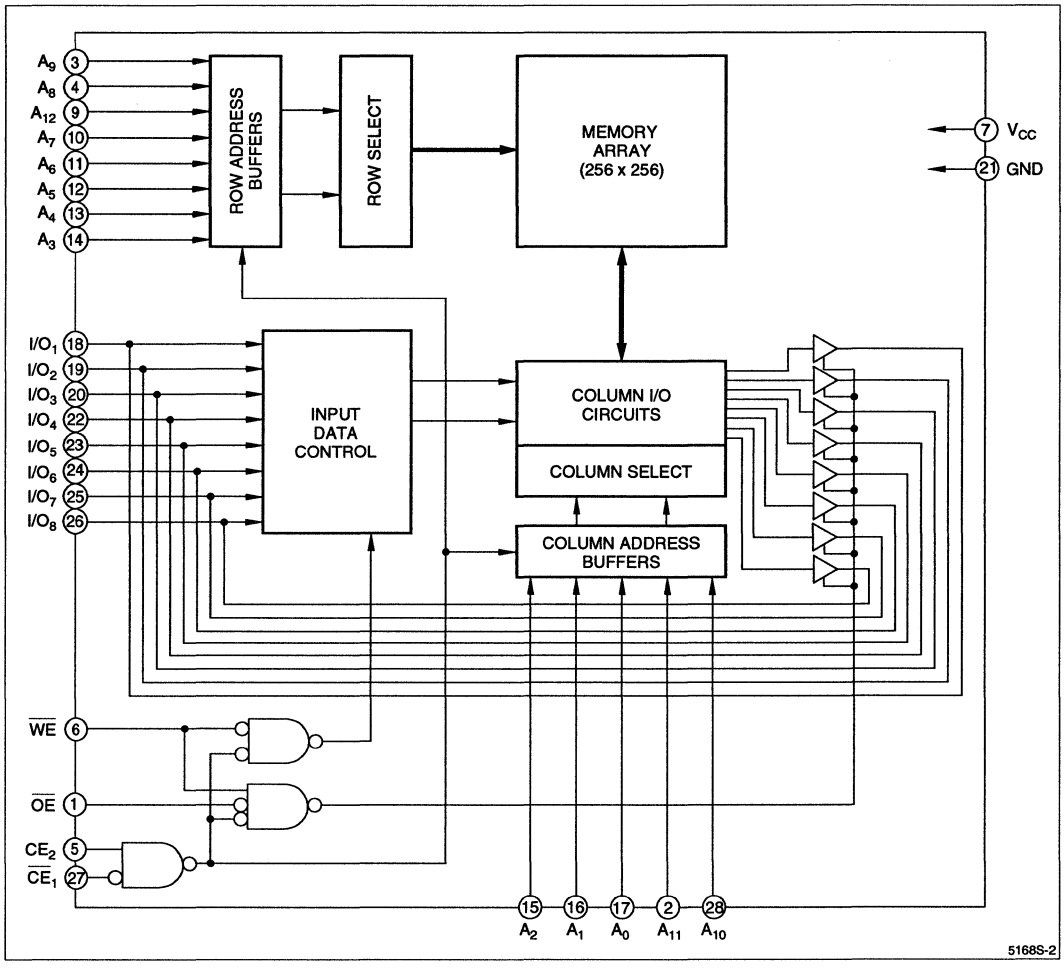


Figure 2. LH5168ST Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME
A_0 - A_{12}	Address inputs
$\overline{CE}_1$ - CE_2	Chip Enable input
$\overline{WE}$	Write Enable input
$\overline{OE}$	Output Enable input

SIGNAL	PIN NAME
I/O_1 - I/O_8	Data inputs and outputs
V_{CC}	Power supply
GND	Ground
NC	Non connection

TRUTH TABLE

$\overline{CE_1}$	CE_2	$\overline{WE}$	$\overline{OE}$	MODE	I/O_1 - I/O_8	SUPPLY CURRENT	NOTE
H	X	X	X	Standby	High-Z	Standby (I_{SB})	1
X	L	X	X	Standby	High-Z	Standby (I_{SB})	1
L	H	L	X	Write	D_{IN}	Operating (I_{CC})	1
L	H	H	L	Read	D_{OUT}	Operating (I_{CC})	
L	H	H	H	Output deselect	High-Z	Operating (I_{CC})	

NOTE:
1. X = H or L

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Supply voltage	V_{CC}	-0.3 to +7.0	V	1
Input voltage	V_{IN}	-0.3 to V_{CC} +0.3	V	1
Operating temperature	Topr	-10 to +70	°C	
Storage temperature	Tstg	-65 to +150	°C	

NOTE:
1. The maximum applicable voltage on any pin with respect to GND.

RECOMMENDED OPERATING CONDITIONS (T_A = -10 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	2.4	3.0	5.5	V
Input voltage (V_{CC} = 2.5 to 4.5 V)	V_{IH}	V_{CC} - 0.5		V_{CC} + 0.3	V
	V_{IL}	-0.3		0.2	V
Input voltage (V_{CC} = 4.5 to 5.5 V)	V_{IH}	2.2		V_{CC} + 0.3	V
	V_{IL}	-0.3		0.8	V

DC CHARACTERISTICS (T_A = -10 to +70°C, V_{CC} = 2.4 to 5.5 V)

PARAMETER	SYMBOL	CONDITIONS		MIN.	MAX.	UNIT	NOTE
Input leakage current	I_{LI}	V_{IN} = 0 to V_{CC}		-1.0	1.0	µA	
Output leakage current	I_{LO}	$\overline{CE_1}$ = V_{IH} or CE_2 = V_{IL} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL} $V_{I/O}$ = 0 to V_{CC}		-1.0	1.0	µA	
Operating current		$\overline{CE_1}$ = 0.2 V, V_{IN} = 0.2 V or V_{CC} - 0.2 V CE_2 = V_{CC} - 0.2 V, Outputs open	t_{CYCLE} = 500 ns		20	mA	
		$\overline{CE_1}$ = 0.2 V, V_{IN} = 0.2 V or V_{CC} - 0.2 V CE_2 = V_{CC} - 0.2 V, Outputs open	t_{CYCLE} = 1.0 µs		10		
		$\overline{CE_1}$ = 0.2 V, V_{IN} = 0.2 V or V_{CC} - 0.2 V CE_2 = V_{CC} - 0.2 V, Outputs open, V_{CC} = 3.3 V	t_{CYCLE} = 1.0 µs		8		
Standby current	I_{SB}	CE_2 ≤ 0.2 V or $\overline{CE_1}$ ≥ V_{CC} - 0.2 V			1.0	µA	1
	I_{SB1}	$\overline{CE_1}$ = V_{IH} or CE_1 = V_{IL}			5	mA	
Output Low voltage	V_{OL}	I_{OL} = 500 µA			0.5	V	
Output High voltage	V_{OH}	I_{OH} = -500 µA		V_{CC} - 0.5		V	2

NOTES:
1. CE_2 should be ≥ V_{CC} - 0.2 V or ≤ 0.2 V.
2. V_{OH} is 4.5 V (Min.) at V_{CC} > 5 V.

AC CHARACTERISTICS

(1) READ CYCLE (T_A = -10 to +70°C, V_{CC} = 2.5 to 5.5 V)

PARAMETER		SYMBOL	MIN.	MAX.	UNIT
Read cycle		t_{RC}	500		ns
Address access time		t_{AA}		500	ns
Chip enable access time	($\overline{CE}_1$)	t_{ACE1}		500	ns
	(CE_2)	t_{ACE2}		500	ns
Output enable access time		t_{OE}		200	ns
Output hold time		t_{OH}	10		ns
Chip enable to output in Low-Z	($\overline{CE}_1$)	t_{LZ1}	20		ns
	(CE_2)	t_{LZ2}	20		ns
Output enable to output in Low-Z		t_{OLZ}	10		ns
Chip enable to output in High-Z	($\overline{CE}_1$)	t_{HZ1}	0	60	ns
	(CE_2)	t_{HZ2}	0	60	ns
Output disable to output in High-Z		t_{OHZ}	0	40	ns

(2) WRITE CYCLE (T_A = -10 to +70°C, V_{CC} = 2.5 to 5.5 V)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
Write cycle time	t_{WC}	500		ns
Chip enable to end of write	t_{CW}	250		ns
Address valid to end of write	t_{AW}	250		ns
Address setup time	t_{AS}	100		ns
Write pulse width	t_{WP}	150		ns
Write recovery time	t_{WR}	50		ns
Data valid to end of write	t_{DW}	100		ns
Data hold time	t_{DH}	0		ns
Output active from end of write	t_{OW}	20		ns
$\overline{WE}$ to output in High-Z	t_{WZ}	0	60	ns
$\overline{OE}$ to output in High-Z	t_{OHZ}	0	40	ns

AC TEST CONDITIONS

PARAMETER	MODE
Input voltage amplitude	0 to V_{CC}
Input rise/fall time	10 ns
Timing reference level	1.5 V
Output load conditions	No load

CAPACITANCE (T_A = 25°C, f = 1 MHz)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input capacitance	C_{IN}	V_{IN} = 0 V			7	pF
Input/output capacitance	$C_{I/O}$	$V_{I/O}$ = 0 V			10	pF

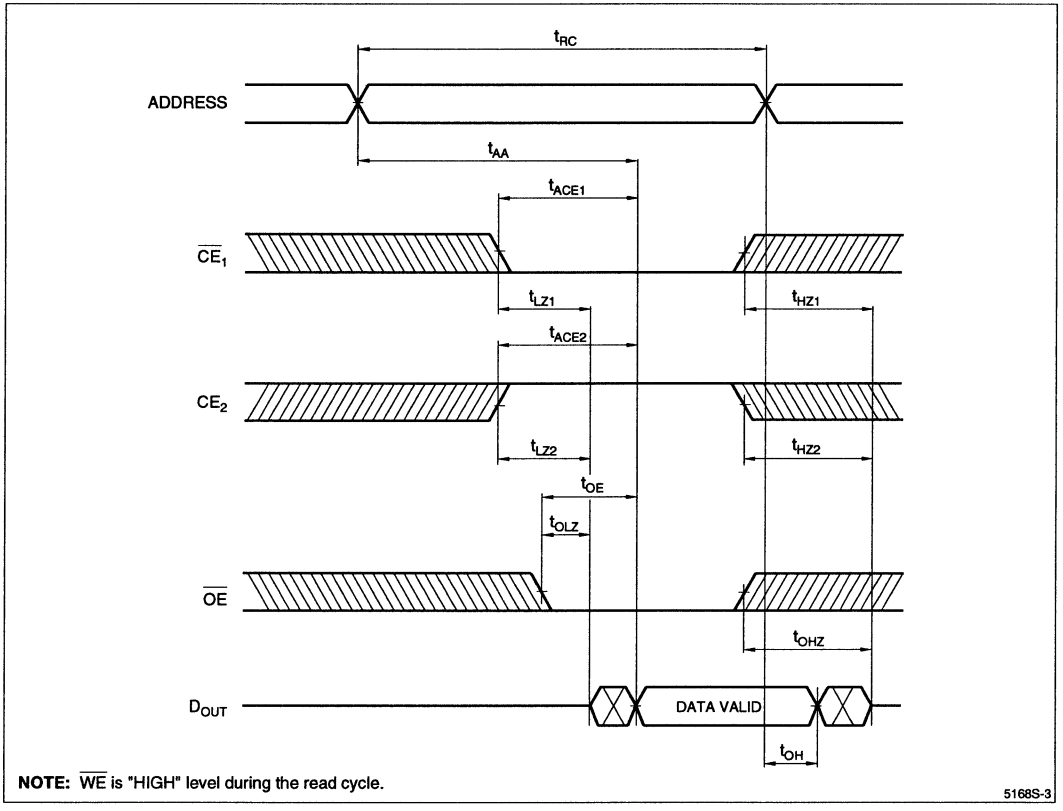
NOTE:
This parameter is sampled and not production tested.

DATA RETENTION CHARACTERISTICS (T_A = -10 to +70°C)

PARAMETER	SYMBOL	CONDITIONS		MIN.	MAX.	UNIT	NOTE
Data retention voltage	V_{CCDR}	$CE_2 \le 0.2$ V or $\overline{CE}_1 \ge V_{CCDR}$ - 0.2 V		1.8		V	1
Data retention current	I_{CCDR}	V_{CCDR} = 3.0 V	T_A = 25°C		0.2	µA	
		$CE_2 \le 0.2$ V or	T_A = 40°C		0.4		
		$\overline{CE}_1 \ge V_{CCDR}$ - 0.2 V			0.6		1
Chip disable to data retention	t_{CDR}			0		ns	
Recovery time	t_{RDR}			t_{RC}		ns	2

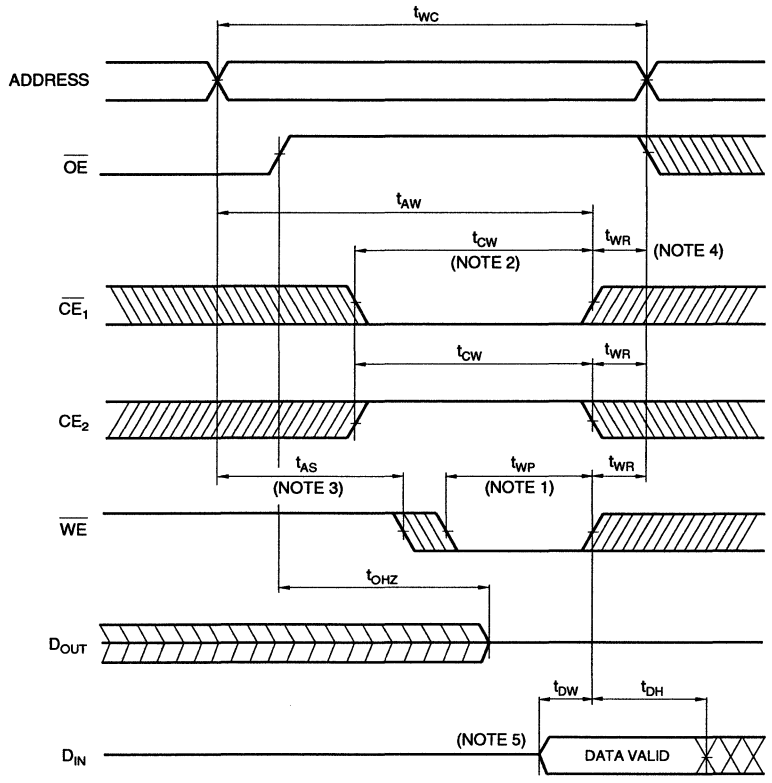
NOTES:

1. CE_2 should be $\ge V_{CCDR}$ - 0.2 V or $\le$ 0.2 V.
2. t_{RC} = Read cycle time.



NOTE: $\overline{WE}$ is "HIGH" level during the read cycle.

Figure 3. Read Cycle



NOTES:

1. The writing occurs during an overlapping period of $\overline{CE_1}$ = "LOW," CE_2 = "HIGH," and $\overline{WE}$ = "LOW" (t_{WP}).
2. t_{CW} is defined as the time from the last occuring transit, either $\overline{CE_1}$ LOW transit or CE_2 HIGH transit, to the time when the writing is finished.
3. t_{AS} is defined as the time from address change to writing start.
4. t_{WR} is defined as the time from writing finish to address change.
5. The input signals of opposite phase to the outputs must not be applied while I/O pins are in the output state.

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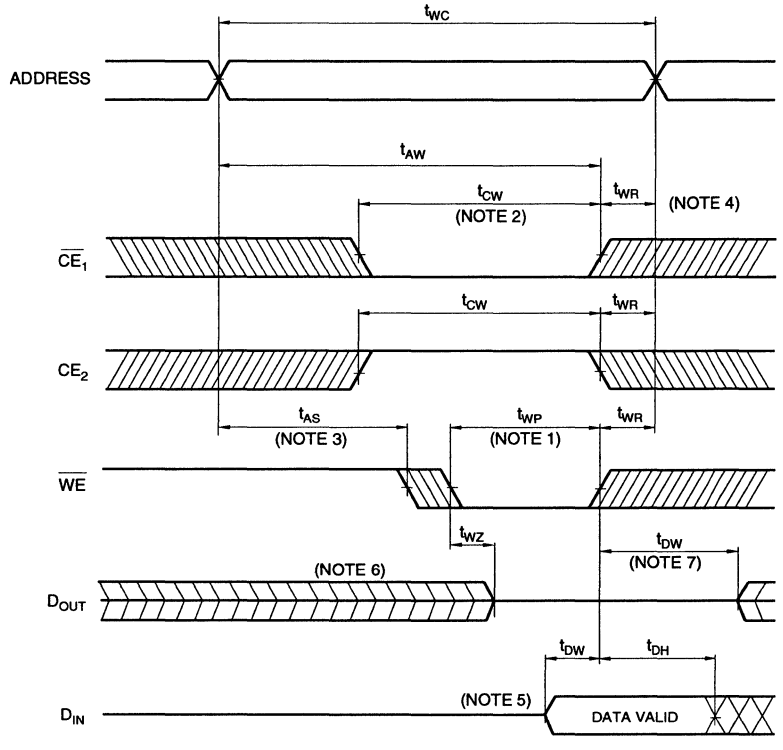
Figure 4. Write Cycle 1



NOTES:

1. The writing occurs during an overlapping period of $\overline{CE_1}$ = "LOW," CE_2 = "HIGH," and $\overline{WE}$ = "LOW" (t_{WP}).
2. t_{CW} is defined as the time from the last occuring transit, either $\overline{CE_1}$ LOW transit or CE_2 HIGH transit, to the time when the writing is finished.
3. t_{AS} is defined as the time from address change to writing start.
4. t_{WR} is defined as the time from writing finish to address change.
5. The input signals of opposite phase to the outputs must not be applied while I/O pins are in the output state.
6. If $\overline{CE_1}$ LOW transit or CE_2 HIGH transit occurs at the same time or after $\overline{WE}$ LOW transit, the output will remain high-impedance.
7. If $\overline{CE_1}$ HIGH transit or CE_2 LOW transit occurs at the same time or before $\overline{WE}$ HIGH transit, the output will remain high-impedance.

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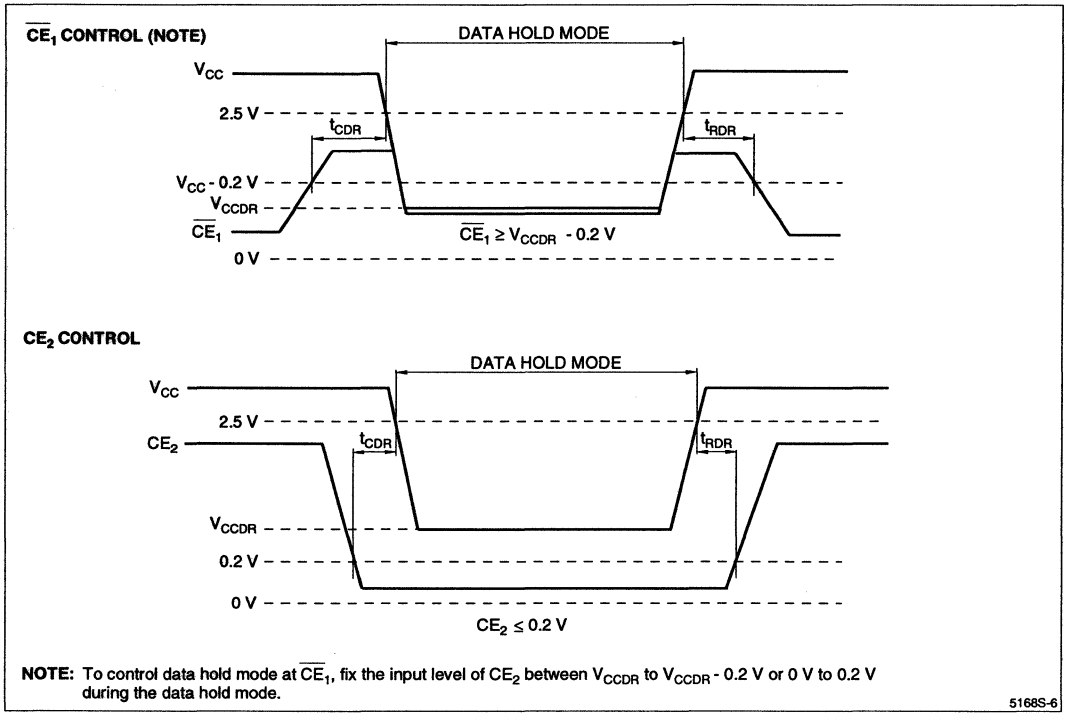
Figure 5. $\overline{OE}$ Low Fixed



NOTE: To control data hold mode at $\overline{CE_1}$, fix the input level of CE_2 between V_{CCDR} to V_{CCDR} - 0.2 V or 0 V to 0.2 V during the data hold mode.

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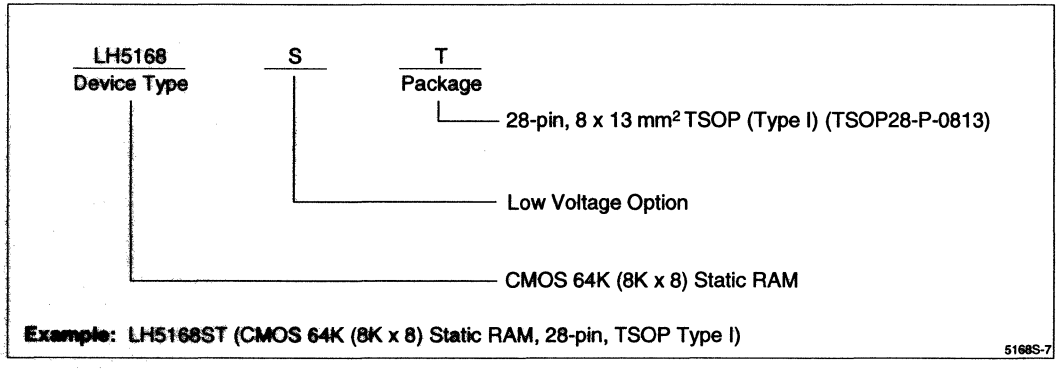
Figure 6. Low Voltage Data Retention

ORDERING INFORMATION



Example: LH5168ST (CMOS 64K (8K x 8) Static RAM, 28-pin, TSOP Type I)

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LH5168Z8

CMOS 64K (8K × 8) Static RAM

FEATURES

- 8,192 × 8 bit organization
- Access time:
  200 ns (V_{CC} = 3.0 V MAX.)
- Power consumption:
  Operating:
  60 mW (MAX.) @ 3 V
  Standby (to 60°C):
  3 µW (MAX.) @ 3 V
  Data hold
  0.6 µA (V_{CC} = 3 V, T_A = 60°C)
- Operating voltage range:
  3.0 V to 3.6 V
- Wide operating temperature range:
  -30 to 60°C
- Fully-static operation
- TTL compatible I/O
- Three-state outputs
- Package: 28-pin, 450-mil SOP

DESCRIPTION

The LH5168Z8 is a static RAM organized as 8,192 × 8 bits. It is fabricated using silicon-gate CMOS process technology.

PIN CONNECTIONS

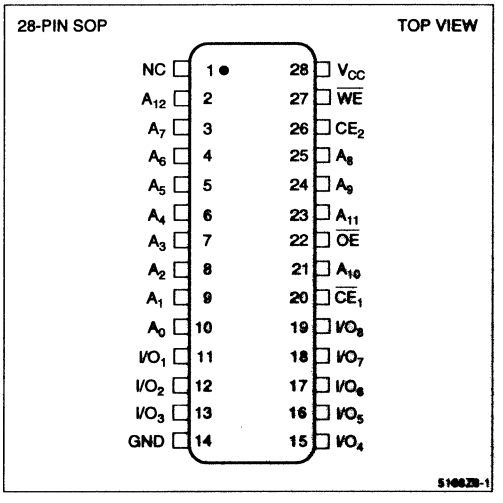


Figure 1. Pin Connections for SOP Package

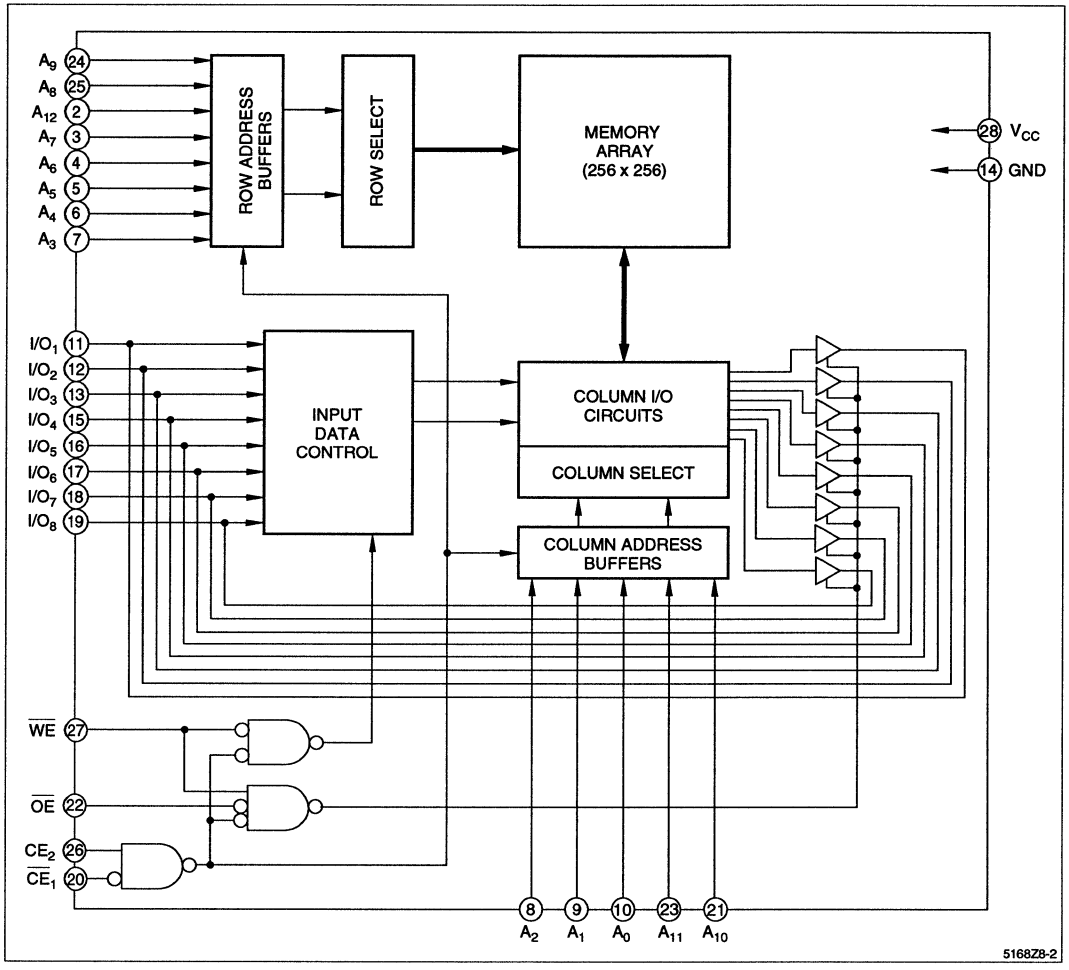


Figure 2. LH5168Z8 Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME
A_0 - A_{12}	Address inputs
$\overline{CE}_1$ - CE_2	Chip Enable input
$\overline{WE}$	Write Enable input
$\overline{OE}$	Output Enable input

SIGNAL	PIN NAME
I/O_1 - I/O_8	Data inputs and outputs
V_{CC}	Power supply
GND	Ground
NC	Non connection

TRUTH TABLE

$\overline{CE_1}$	CE_2	$\overline{WE}$	$\overline{OE}$	MODE	I/O_1 - I/O_8	SUPPLY CURRENT	NOTE
H	X	X	X	Standby	High-Z	Standby (I_{SB})	1
X	L	X	X	Standby	High-Z	Standby (I_{SB})	1
L	H	L	X	Write	D_{IN}	Operating (I_{CC})	1
L	H	H	L	Read	D_{OUT}	Operating (I_{CC})	
L	H	H	H	Output deselect	High-Z	Operating (I_{CC})	

NOTE:
1. X = H or L

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Supply voltage	V_{CC}	-0.3 to +7.0	V	1
Input voltage	V_{IN}	-0.3 to V_{CC} + 0.3	V	1
Operating temperature	Topr	-30 to +60	°C	
Storage temperature	Tstg	-65 to +150	°C	

NOTE:
1. The maximum applicable voltage on any pin with respect to GND.

RECOMMENDED OPERATING CONDITIONS (T_A = -30 to +60°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	3.0		3.6	V
Input voltage (V_{CC} = 3.0 to 3.6 V)	V_{IH}	V_{CC} - 0.5		V_{CC} + 0.3	V
	V_{IL}	-0.3		0.2	V

DC CHARACTERISTICS (T_A = -30 to +60°C, V_{CC} = 3.0 to 3.6 V)

PARAMETER	SYMBOL	CONDITIONS		MIN.	MAX.	UNIT	NOTE
Input leakage current	$\lvert I_{LI} \rvert$	V_{IN} = 0 to V_{CC}		-1.0	1.0	µA	
Output leakage current	$\lvert I_{LO} \rvert$	$\overline{CE_1}$ = V_{IH} or CE_2 = V_{IL} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL} $V_{I/O}$ = 0 to V_{CC}		-1.0	1.0	µA	
Operating current	I_{CC}	$\overline{CE_1}$ = 0.2 V, V_{IN} = 0.2 V or V_{CC} - 0.2 V CE_2 = V_{CC} - 0.2 V, Outputs open	t_{CYCLE} = 200 ns		20	mA	
		$\overline{CE_1}$ = 0.2 V, V_{IN} = 0.2 V or V_{CC} - 0.2 V CE_2 = V_{CC} - 0.2 V, Outputs open	t_{CYCLE} = 1.0 µs		10		
		$\overline{CE_1}$ = 0.2 V, V_{IN} = 0.2 V or V_{CC} - 0.2 V CE_2 = V_{CC} - 0.2 V, Outputs open, V_{CC} = 3.3 V	t_{CYCLE} = 1.0 µs		8		
Standby current	I_{SB}	CE_2 ≤ 0.2 V or $\overline{CE_1}$ ≥ V_{CC} - 0.2 V	To +60°C		1.0	µA	1
	I_{SB1}	$\overline{CE_1}$ = V_{IH} or CE_2 = V_{IL}			5	mA	
Output voltage	V_{OL}	I_{OL} = 500 µA			0.5	V	
	V_{OH}	I_{OH} = -500 µA		V_{CC} - 0.5		V	

NOTE:
1. CE_2 should be ≥ V_{CC} - 0.2 V or ≤ 0.2 V.

AC CHARACTERISTICS

(1) READ CYCLE (T_A = -30 to +60°C, V_{CC} = 3.0 to 3.6 V)

PARAMETER		SYMBOL	MIN.	MAX.	UNIT
Read cycle		t_{RC}	200		ns
Address access time		t_{AA}		200	ns
Chip enable access time	($\overline{CE}_1$)	t_{ACE1}		200	ns
	(CE_2)	t_{ACE2}		200	ns
Output enable access time		t_{OE}		150	ns
Output hold time		t_{OH}	10		ns
Chip enable to output in Low-Z	($\overline{CE}_1$)	t_{LZ1}	20		ns
	(CE_2)	t_{LZ2}	20		ns
Output enable to output in Low-Z		t_{OLZ}	10		ns
Chip enable to output in High-Z	($\overline{CE}_1$)	t_{HZ1}	0	60	ns
	(CE_2)	t_{HZ2}	0	60	ns
Output disable to output in High-Z		t_{OHZ}	0	40	ns

(2) WRITE CYCLE (T_A = -30 to +60°C, V_{CC} = 3.0 to 3.6 V)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
Write cycle time	t_{WC}	200		ns
Chip enable to end of write	t_{CW}	180		ns
Address valid to end of write	t_{AW}	180		ns
Address setup time	t_{AS}	0		ns
Write pulse width	t_{WP}	150		ns
Write recovery time	t_{WR}	0		ns
Data valid to end of write	t_{DW}	100		ns
Data hold time	t_{DH}	0		ns
Output active from end of write	t_{OW}	20		ns
$\overline{WE}$ to output in High-Z	t_{WZ}	0	60	ns
$\overline{OE}$ to output in High-Z	t_{OHZ}	0	40	ns

AC TEST CONDITIONS

PARAMETER	MODE
Input voltage amplitude	0 to V_{CC}
Input rise/fall time	10 ns
Timing reference level	1.5 V
Output load conditions	No load

CAPACITANCE (T_A = 25°C, f = 1 MHz)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input capacitance	C_{IN}	V_{IN} = 0 V			7	pF
Input/output capacitance	$C_{I/O}$	$V_{I/O}$ = 0 V			10	pF

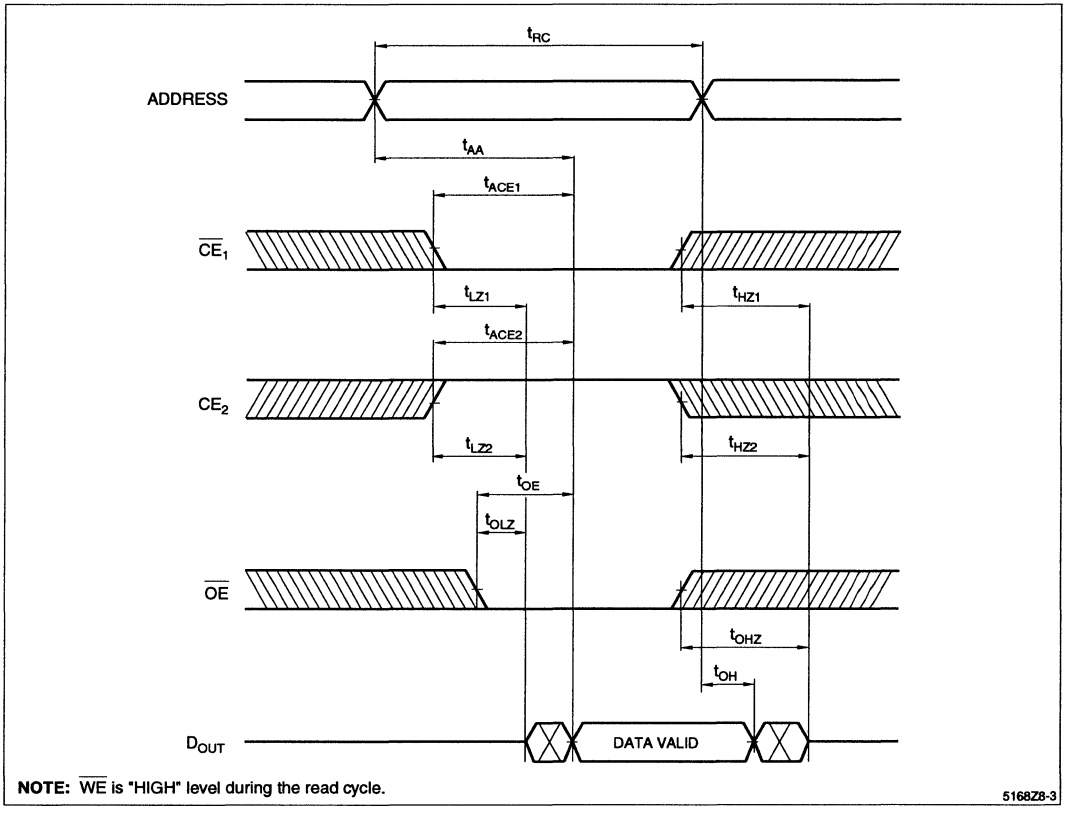
NOTE:
This parameter is sampled and not production tested.

DATA RETENTION CHARACTERISTICS (T_A = -30 to +60°C)

PARAMETER	SYMBOL	CONDITIONS		MIN.	MAX.	UNIT	NOTE
Data retention voltage	V_{CCDR}	$CE_2 \le 0.2$ V or $\overline{CE_1} \ge V_{CCDR}$ - 0.2 V		2.0		V	1
Data retention current	I_{CCDR}	V_{CCDR} = 3.0 V	T_A = 25°C		0.2	µA	
		$CE_2 \le 0.2$ V or $\overline{CE_1} \ge V_{CCDR}$ - 0.2 V	T_A = 60°C		0.6		1
Chip disable to data retention	t_{CDR}			0		ns	
Recovery time	t_{RDR}			t_{RC}		ns	2

NOTES:

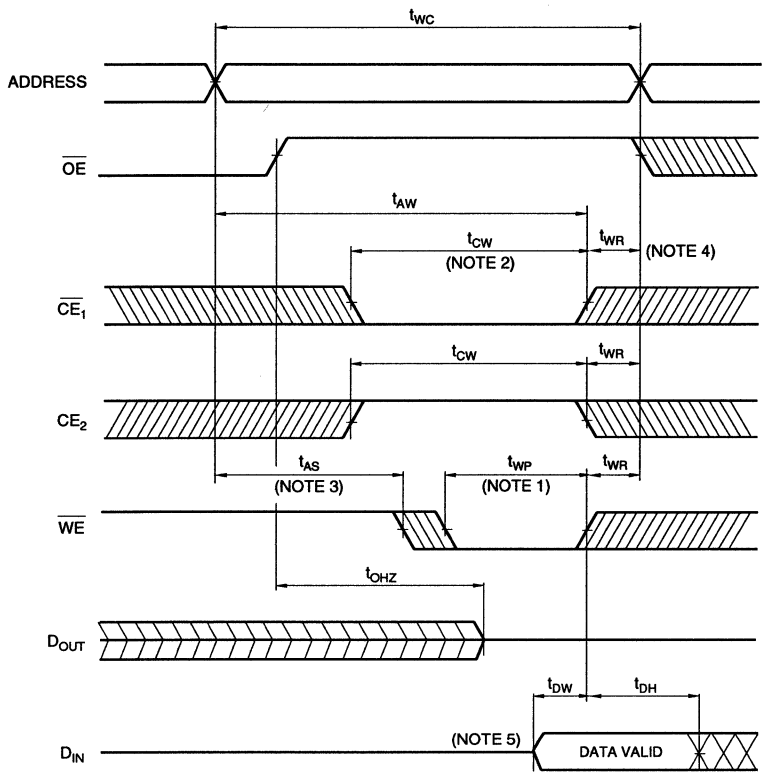
1. CE_2 should be $\ge V_{CCDR}$ - 0.2 V or $\le$ 0.2 V.
2. t_{RC} = Read cycle time



NOTE: $\overline{WE}$ is "HIGH" level during the read cycle.

5168Z8-3

Figure 3. Read Cycle

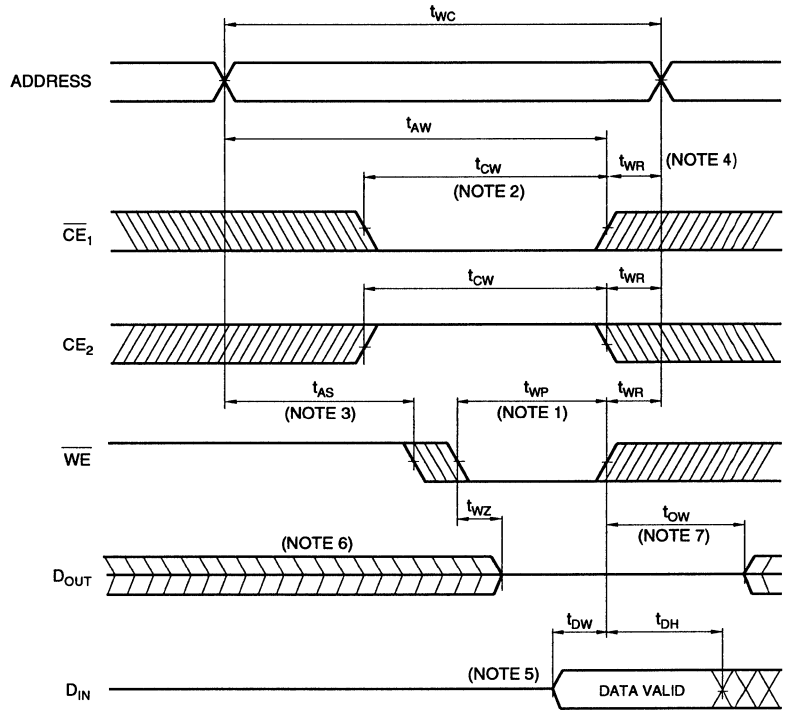


NOTES:

1. The writing occurs during an overlapping period of $\overline{CE_1}$ = "LOW," CE_2 = "HIGH," and $\overline{WE}$ = "LOW" (t_{WP}).
2. t_{CW} is defined as the time from the last occuring transit, either $\overline{CE_1}$ LOW transit or CE_2 HIGH transit, to the time when the writing is finished.
3. t_{AS} is defined as the time from address change to writing start.
4. t_{WR} is defined as the time from writing finish to address change.
5. The input signals of opposite phase to the outputs must not be applied while I/O pins are in the output state.

5168Z8-4

Figure 4. Write Cycle

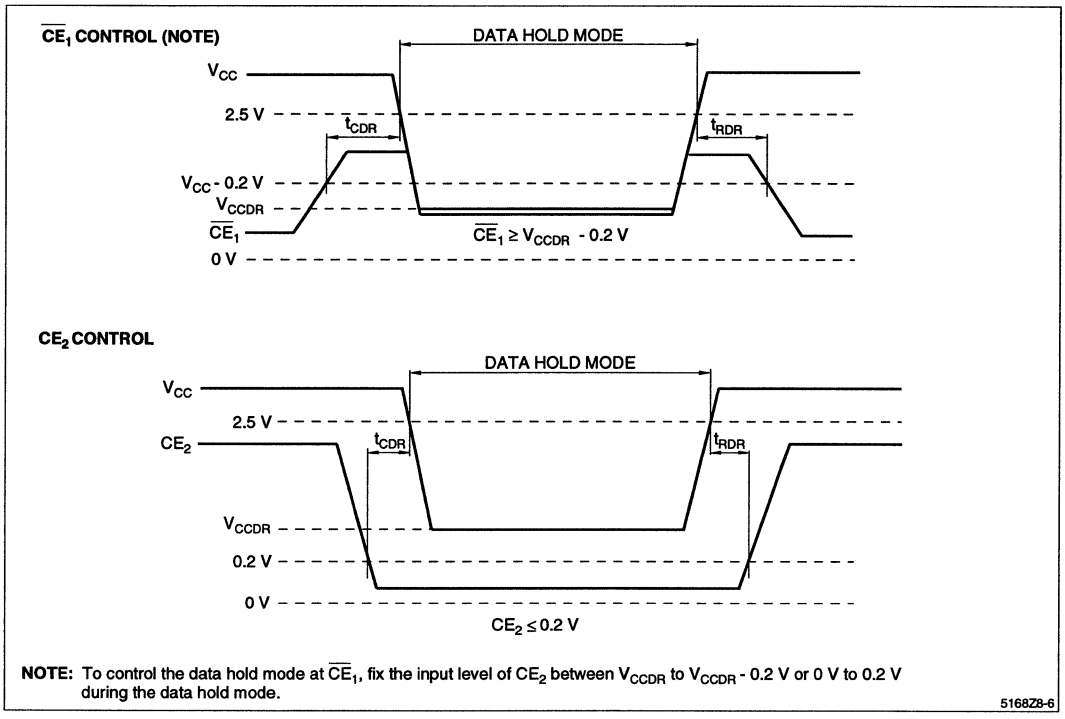


NOTES:

1. The writing occurs during an overlapping period of $\overline{CE}_1$ = "LOW," CE_2 = "HIGH," and $\overline{WE}$ = "LOW" (t_{WP}).
2. t_{CW} is defined as the time from the last occuring transit, either $\overline{CE}_1$ LOW transit or CE_2 HIGH transit, to the time when the writing is finished.
3. t_{AS} is defined as the time from address change to writing start.
4. t_{WR} is defined as the time from writing finish to address change.
5. The input signals of opposite phase to the outputs must not be applied while I/O pins are in the output state.
6. If $\overline{CE}_1$ LOW transit or CE_2 HIGH transit occurs at the same time or after $\overline{WE}$ LOW transit, the output will remain high-impedance.
7. If $\overline{CE}_1$ HIGH transit or CE_2 LOW transit occurs at the same time or before $\overline{WE}$ HIGH transit, the output will remain high-impedance.

5168Z8-5

Figure 5. $\overline{OE}$ Low Fixed

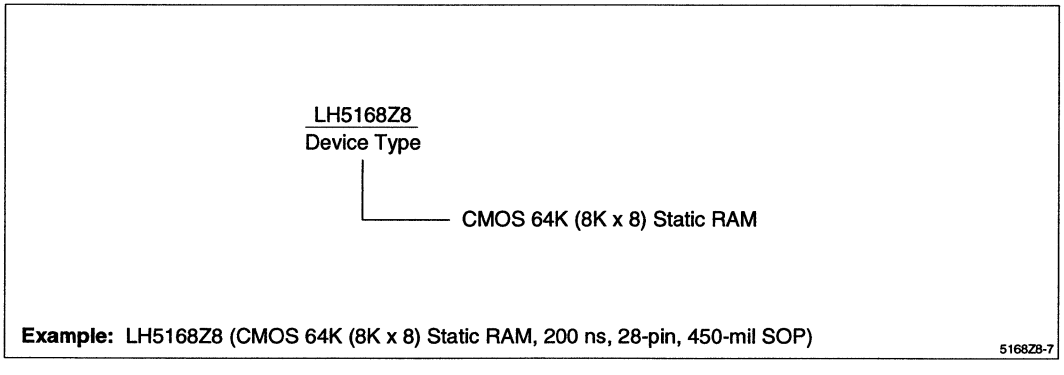


NOTE: To control the data hold mode at $\overline{CE_1}$, fix the input level of CE_2 between V_{CCDR} to V_{CCDR} - 0.2 V or 0 V to 0.2 V during the data hold mode.

5168Z8-6

Figure 6. Low Voltage Data Retention

ORDERING INFORMATION



Example: LH5168Z8 (CMOS 64K (8K x 8) Static RAM, 200 ns, 28-pin, 450-mil SOP)

5168Z8-7

LH5168Z9

ADVANCE INFORMATION

CMOS 64K (8K × 8) Static Ram

FEATURES

- 8,192 × 8 bit organization
- Access time: 260 ns
- Power consumption:
  Operating:
  60 mW (MAX.) @ 3 V
  Standby (to 60°C):
  3 µW (MAX.) @ 3 V
  Data hold
  0.6 µA (V_{CC} = 3 V, T_A = 60°C)
- Operating voltage range:
  2.7 V to 3.6 V
- Operating temperature range:
  -10 to 60°C
- Fully-static operation
- TTL compatible I/O
- Three-state outputs
- Package: 28-pin, 450-mil SOP

DESCRIPTION

The LH5168Z9 is a static RAM organized as 8,192 × 8 bits. It is fabricated using silicon-gate CMOS process technology.

PIN CONNECTIONS

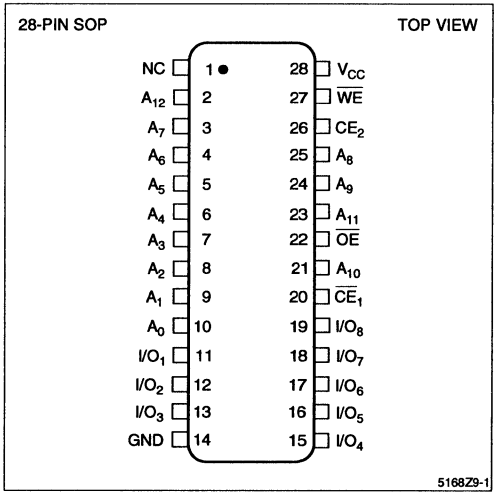


Figure 1. Pin Connections for SOP Package

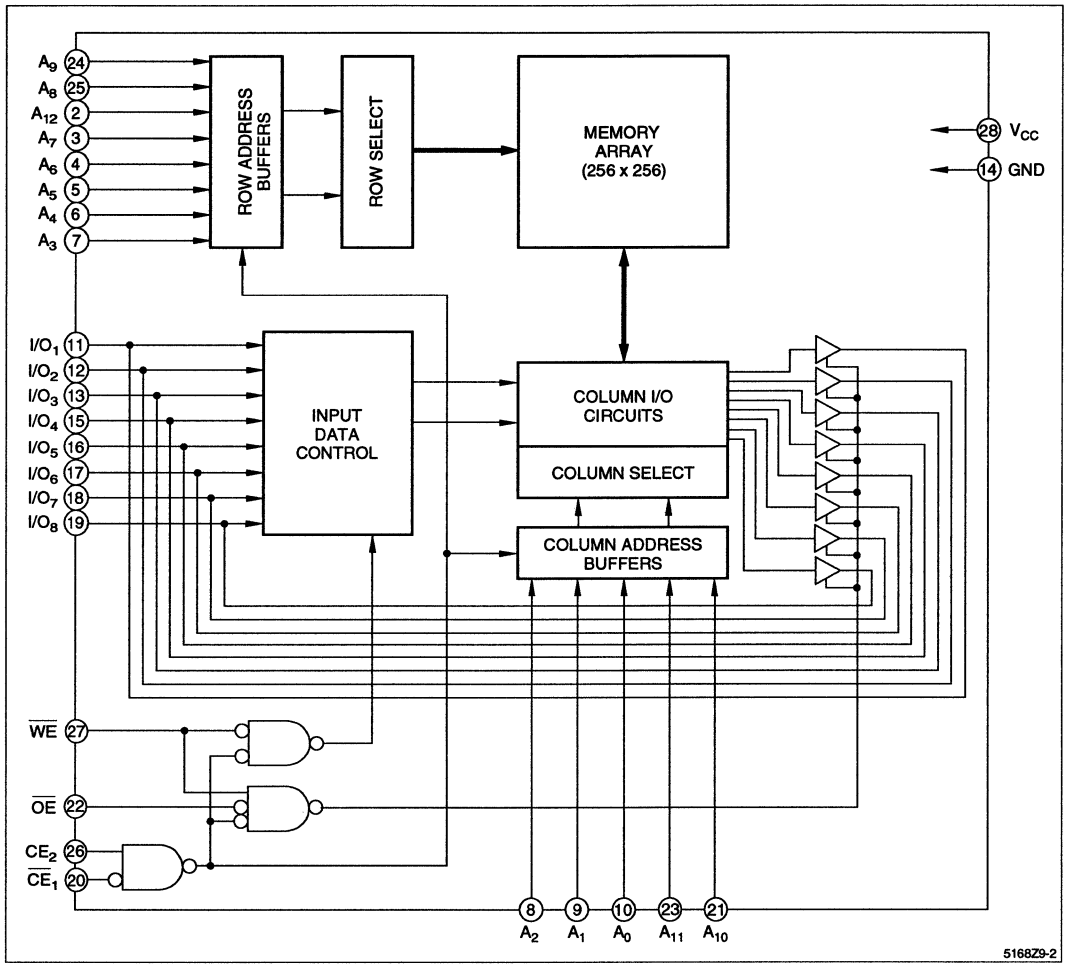


Figure 2. LH5168Z9 Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME
A_0 - A_{12}	Address inputs
$\overline{CE_1}/CE_2$	Chip Enable input
$\overline{WE}$	Write Enable input
$\overline{OE}$	Output Enable input

SIGNAL	PIN NAME
I/O_1 - I/O_8	Data inputs and outputs
V_{CC}	Power supply
GND	Ground
NC	Non connection

TRUTH TABLE

$\overline{CE_1}$	CE_2	$\overline{WE}$	$\overline{OE}$	MODE	I/O_1 - I/O_8	SUPPLY CURRENT	NOTE
H	X	X	X	Standby	High-Z	Standby (I_{SB})	1
X	L	X	X	Standby	High-Z	Standby (I_{SB})	1
L	H	L	X	Write	D_{IN}	Operating (I_{CC})	1
L	H	H	L	Read	D_{OUT}	Operating (I_{CC})	
L	H	H	H	Output deselect	High-Z	Operating (I_{CC})	

NOTE:
1. X = H or L

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Supply voltage	V_{CC}	-0.3 to +7.0	V	1
Input voltage	V_{IN}	-0.3 to V_{CC} + 0.3	V	1
Operating temperature	Topr	-10 to +60	°C	
Storage temperature	Tstg	-65 to +150	°C	

NOTE:
1. The maximum applicable voltage on any pin with respect to GND.

RECOMMENDED OPERATING CONDITIONS (T_A = -10 to +60°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	2.0		3.6	V
Input voltage (V_{CC} = 3.0 to 3.6 V)	V_{IH}	V_{CC} - 0.5		V_{CC} + 0.3	V
	V_{IL}	-0.3		0.2	V

DC CHARACTERISTICS (T_A = -10 to +60°C, V_{CC} = 2.7 to 3.6 V)

PARAMETER	SYMBOL	CONDITIONS		MIN.	MAX.	UNIT	NOTE
Input leakage current	$\lvert I_{LI} \rvert$	V_{IN} = 0 to V_{CC}		-1.0	1.0	µA	
Output leakage current	$\lvert I_{LO} \rvert$	$\overline{CE_1}$ = V_{IH} or CE_2 = V_{IL} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL} $V_{I/O}$ = 0 to V_{CC}		-1.0	1.0	µA	
Operating current	I_{CC}	$\overline{CE_1}$ = 0.2 V, V_{IN} = 0.2 V or V_{CC} - 0.2 V CE_2 = V_{CC} - 0.2 V, Outputs open	t_{CYCLE} = 200 ns		20	mA	
		$\overline{CE_1}$ = 0.2 V, V_{IN} = 0.2 V or V_{CC} - 0.2 V CE_2 = V_{CC} - 0.2 V, Outputs open	t_{CYCLE} = 1.0 µs		10		
		$\overline{CE_1}$ = 0.2 V, V_{IN} = 0.2 V or V_{CC} - 0.2 V CE_2 = V_{CC} - 0.2 V, Outputs open, V_{CC} = 3.3 V	t_{CYCLE} = 1.0 µs		8		
Standby current	I_{SB}	CE_2 ≤ 0.2 V or $\overline{CE_1}$ ≥ V_{CC} - 0.2 V	To +60°C		1.0	µA	1
	I_{SB1}	$\overline{CE_1}$ = V_{IH} or CE_2 = V_{IL}			5	mA	
Output Low voltage	V_{OL}	I_{OL} = 500 µA			0.5	V	
Output High voltage	V_{OH}	I_{OH} = -500 µA		V_{CC} - 0.5		V	

NOTE:
1. CE_2 should be ≥ V_{CC} - 0.2 V or ≤ 0.2 V.

AC CHARACTERISTICS

(1) READ CYCLE (T_A = -10 to +60°C, V_{CC} = 2.7 to 3.6 V)

PARAMETER		SYMBOL	MIN.	MAX.	UNIT
Read cycle		t_{RC}	260		ns
Address access time		t_{AA}		260	ns
Chip enable access time	($\overline{CE}_1$)	t_{ACE1}		260	ns
	(CE_2)	t_{ACE2}		260	ns
Output enable access time		t_{OE}		200	ns
Output hold time		t_{OH}	10		ns
Chip enable to output in Low-Z	($\overline{CE}_1$)	t_{LZ1}	20		ns
	(CE_2)	t_{LZ2}	20		ns
Output enable to output in Low-Z		t_{OLZ}	10		ns
Chip enable to output in High-Z	($\overline{CE}_1$)	t_{HZ1}	0	60	ns
	(CE_2)	t_{HZ2}	0	60	ns
Output disable to output in High-Z		t_{OHZ}	0	40	ns

(2) WRITE CYCLE (T_A = -10 to +60°C, V_{CC} = 2.7 to 3.6 V)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
Write cycle time	t_{WC}	260		ns
Chip enable to end of write	t_{CW}	200		ns
Address valid to end of write	t_{AW}	200		ns
Address setup time	t_{AS}	0		ns
Write pulse width	t_{WP}	150		ns
Write recovery time	t_{WR}	0		ns
Data valid to end of write	t_{DW}	100		ns
Data hold time	t_{DH}	0		ns
Output active from end of write	t_{OW}	20		ns
$\overline{WE}$ to output in High-Z	t_{WZ}	0	60	ns
$\overline{OE}$ to output in High-Z	t_{OHZ}	0	40	ns

AC TEST CONDITIONS

PARAMETER	MODE
Input voltage amplitude	0 V to V_{CC}
Input rise/fall time	10 ns
Timing reference level	1.5 V
Output load conditions	No load

CAPACITANCE (T_A = 25°C, f = 1 MHz)

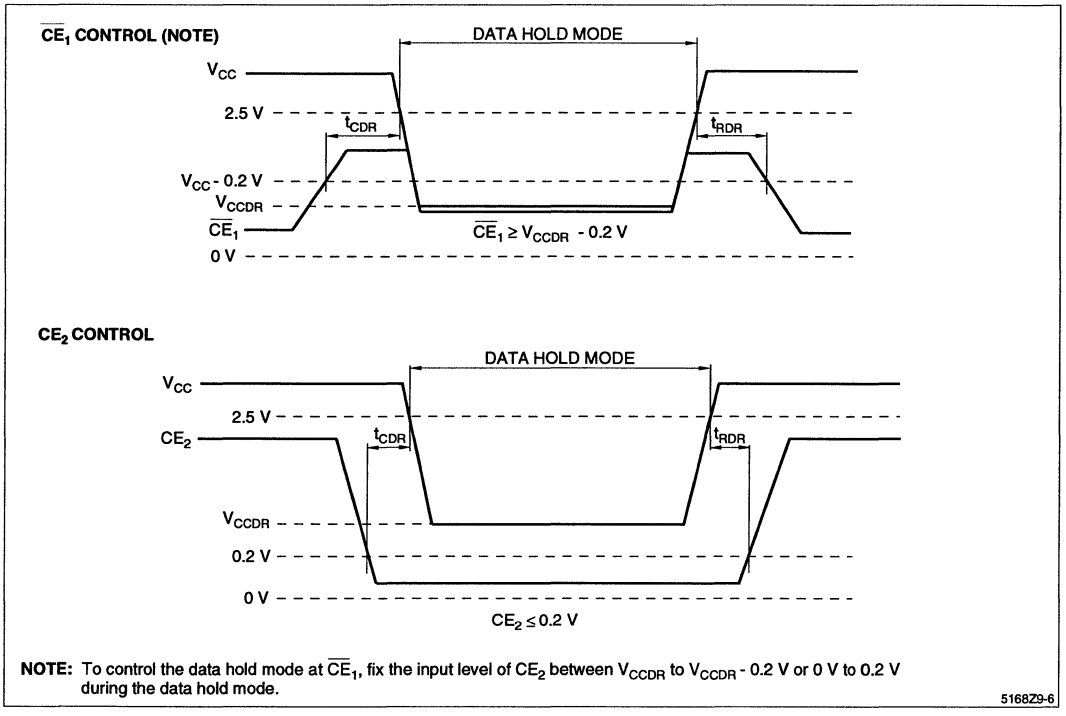
PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input capacitance	C_{IN}	V_{IN} = 0 V			7	pF
Input/output capacitance	$C_{I/O}$	$V_{I/O}$ = 0 V			10	pF

NOTE:
This parameter is sampled and not production tested.

DATA RETENTION CHARACTERISTICS (T_A = -10 to +60°C)

PARAMETER	SYMBOL	CONDITIONS		MIN.	MAX.	UNIT	NOTE
Data retention voltage	V_{CCDR}	$\overline{CE_1} \geq V_{CCDR}$ - 0.2 V $CE_2 \leq 0.2$ V		2.0		V	1
Data retention current	I_{CCDR}	V_{CCDR} = 3 V	T_A = 25°C		0.2	µA	
		$\overline{CE_1} \geq V_{CCDR}$ - 0.2 V $CE_2 \leq 0.2$ V	T_A = 60°C		0.6		1
Chip disable to data retention	t_{CDR}			0		ns	
Recovery time	t_{RDR}			t_{RC}		ns	2

NOTES:
1. CE_2 should be ≥ V_{CCDR} - 0.2 V or ≤ 0.2 V.
2. t_{RC} = Read cycle time



NOTE: To control the data hold mode at $\overline{CE_1}$, fix the input level of CE_2 between V_{CCDR} to V_{CCDR} - 0.2 V or 0 V to 0.2 V during the data hold mode.

5168Z9-6

Figure 3. Low Voltage Data Retention

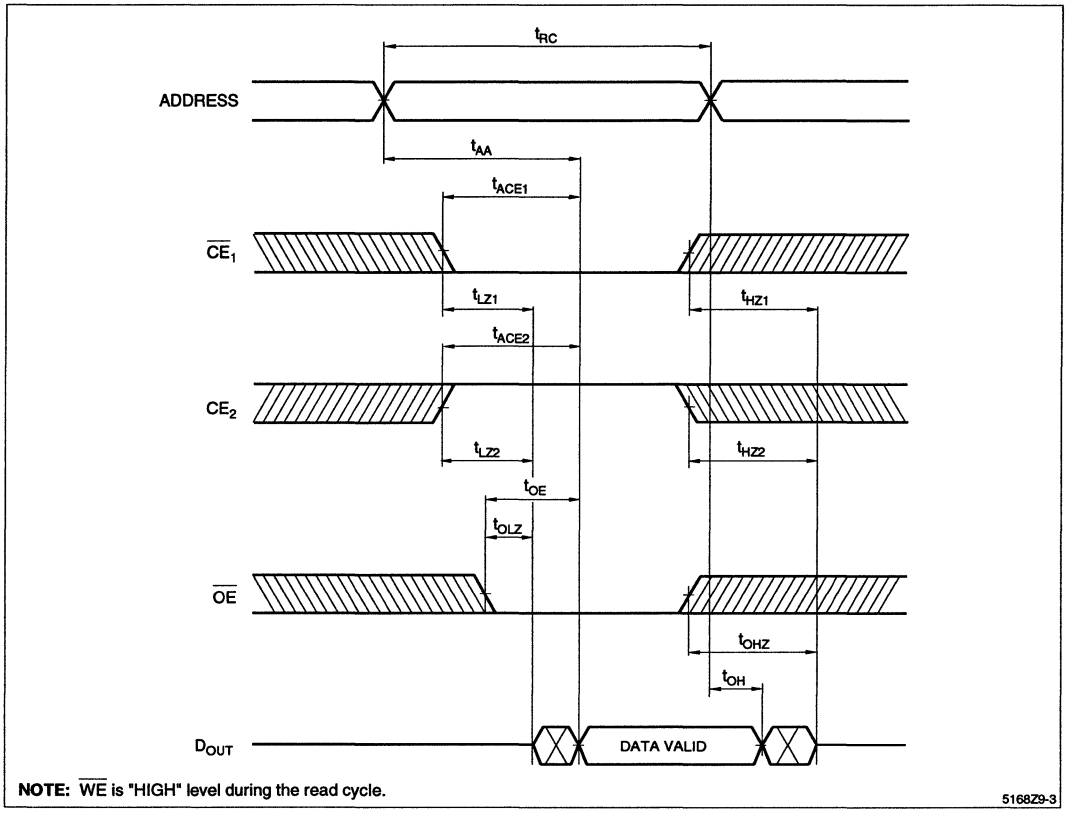
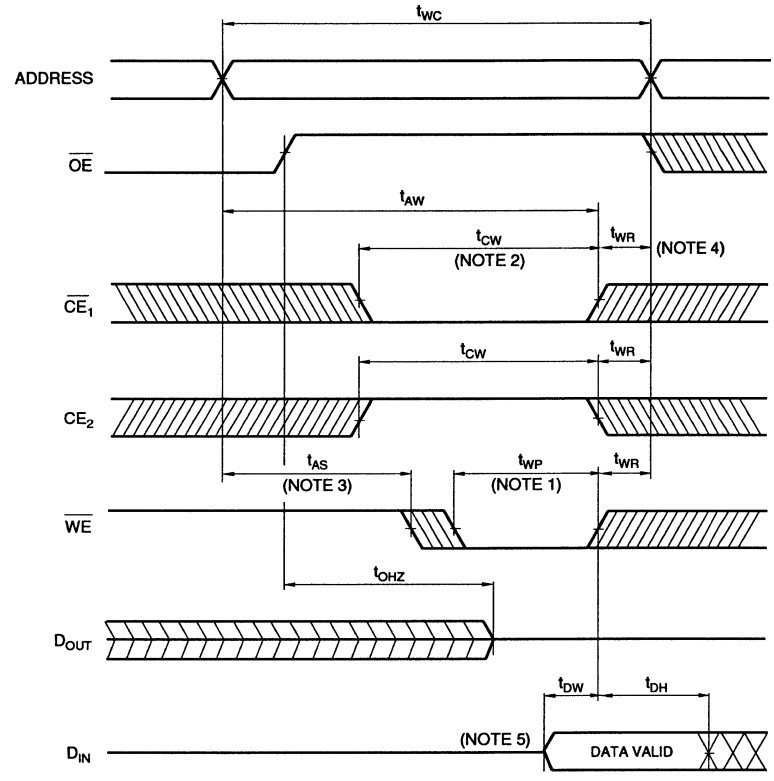


Figure 4. Read Cycle

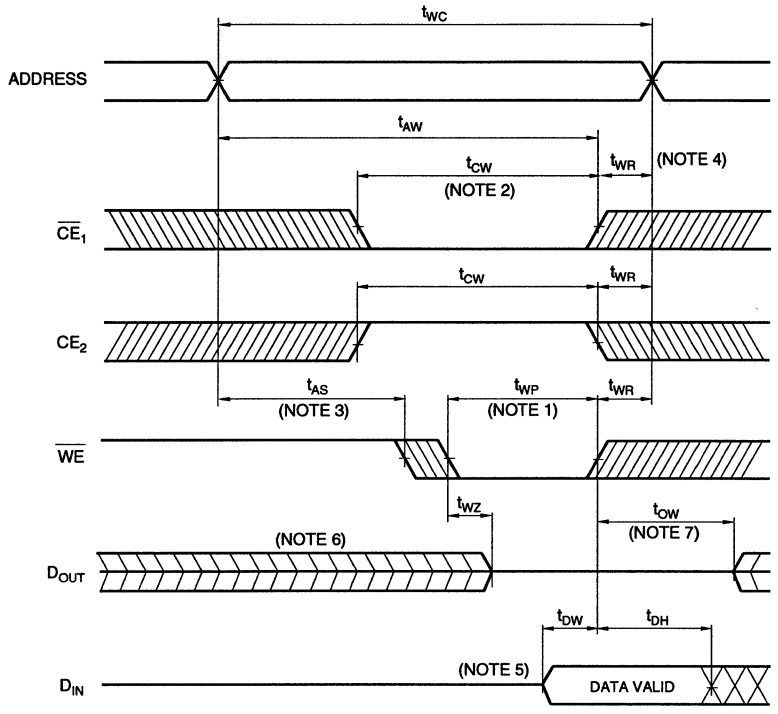


NOTES:

1. The writing occurs during an overlapping period of $\overline{CE_1}$ = "LOW," CE_2 = "HIGH," and $\overline{WE}$ = "LOW" (t_{WP}).
2. t_{CW} is defined as the time from the last occuring transit, either $\overline{CE_1}$ LOW transit or CE_2 HIGH transit, to the time when the writing is finished.
3. t_{AS} is defined as the time from address change to writing start.
4. t_{WR} is defined as the time from writing finish to address change.
5. The input signals of opposite phase to the outputs must not be applied while I/O pins are in the output state.

5168Z9-4

Figure 5. Write Cycle



NOTES:

1. The writing occurs during an overlapping period of $\overline{CE_1}$ = "LOW," CE_2 = "HIGH," and $\overline{WE}$ = "LOW" (t_{WP}).
2. t_{CW} is defined as the time from the last occuring transit, either $\overline{CE_1}$ LOW transit or CE_2 HIGH transit, to the time when the writing is finished.
3. t_{AS} is defined as the time from address change to writing start.
4. t_{WR} is defined as the time from writing finish to address change.
5. The input signals of opposite phase to the outputs must not be applied while I/O pins are in the output state.
6. If $\overline{CE_1}$ LOW transit or CE_2 HIGH transit occurs at the same time or after $\overline{WE}$ LOW transit, the output will remain high-impedance.
7. If $\overline{CE_1}$ HIGH transit or CE_2 LOW transit occurs at the same time or before $\overline{WE}$ HIGH transit, the output will remain high-impedance.

5168Z9-5

Figure 6. $\overline{OE}$ Low Fixed

ORDERING INFORMATION

LH5168Z9
Device Type

CMOS 64K (8K x 8) Static RAM

Example: LH5168Z9 (CMOS 64K (8K x 8) Static RAM)

5168Z9-7

LH5268A

CMOS 64K (8K × 8) Static Ram

FEATURES

- 8,192 × 8 bit organization
- Access times: 100 ns (MAX.)
- Power consumption:
  - Operating:
    - 220 mW (MAX.)
    - 55 mW (MAX.) (t_{RC}, t_{WC} = 1 µs)
  - Standby:
    - 220 µW (MAX.)
  - Data retention:
    - 5.5 µW (V_{CC} = 3 V, T_A = 25°C)
- Operating temperature:
  - 0°C to 70°C
- Fully-static operation
- Three-state outputs
- Single +5 V power supply (5 V ± 10%)
- TTL compatible I/O
- Packages:
  - 28-pin, 600-mil DIP
  - 28-pin, 300-mil SK-DIP
  - 28-pin, 450-mil SOP

DESCRIPTION

The LH5268A is a static RAM organized as 8,192 × 8 bits. It is fabricated using silicon-gate CMOS process technology.

PIN CONNECTIONS

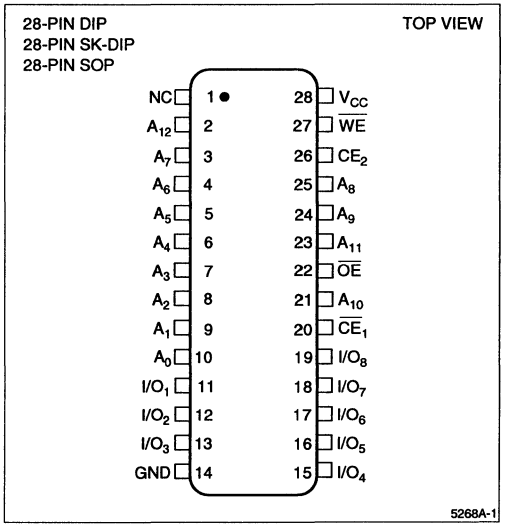


Figure 1. Pin Connections for DIP, SK-DIP, and SOP Packages

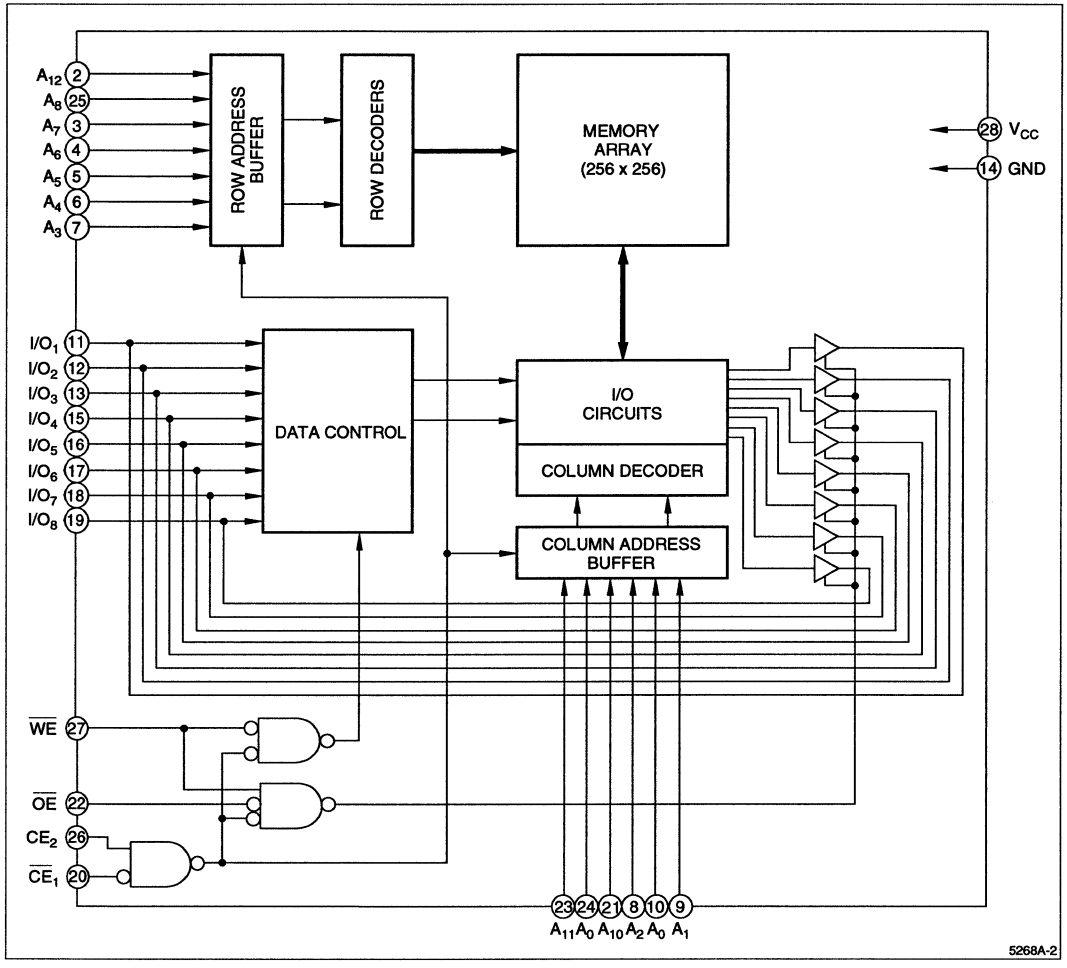


Figure 2. LH5268A Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME
A_0 - A_{12}	Address inputs
$\overline{CE}_1$ - CE_2	Chip Enable input
$\overline{WE}$	Write Enable input
$\overline{OE}$	Output Enable input

SIGNAL	PIN NAME
I/O_1 - I/O_8	Data inputs and outputs
V_{CC}	Power supply
GND	Ground
NC	Non-connection

TRUTH TABLE

$\overline{CE_1}$	CE_2	$\overline{WE}$	$\overline{OE}$	MODE	I/O_1 - I/O_8	SUPPLY CURRENT	NOTE
H	X	X	X	Standby	High-Z	Standby (I_{SB})	1
X	L	X	X	Standby	High-Z	Standby (I_{SB})	1
L	H	L	X	Write	D_{IN}	Operating (I_{CC})	1
L	H	H	L	Read	D_{OUT}	Operating (I_{CC})	
L	H	H	H	Output disable	High-Z	Operating (I_{CC})	

NOTE:
1. X = H or L

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING		UNIT	NOTE
		70 ns	100 ns		
Supply voltage	V_{CC}	-0.5 to +7.0	-0.3 to +7.0	V	1
Input voltage	V_{IN}	-0.5 to V_{CC} +0.5	-0.3 to V_{CC} +0.5	V	1,2
Operating temperature	Topr	0 to +70	0 to +70	°C	
Storage temperature	Tstg	-55 to +150	-65 to +150	°C	

NOTES:
1. The maximum applicable voltage on any pin with respect to GND.
2. Undershoot of -3.0 V is allowed once per cycle.

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Supply voltage	V_{CC}	4.5	5.0	5.5	V	
Input voltage	V_{IH}	2.2		V_{CC} + 0.5	V	
	V_{IL}	-0.3		0.8	V	1

NOTE:
1. Undershoot of -3.0 V is allowed once per cycle.

DC CHARACTERISTICS (T_A = 0 to +70°C, V_{CC} = 5 V ±10%)

PARAMETER	SYMBOL	CONDITIONS		MIN.	MAX.	UNIT	NOTE
Input leakage current	I_{LI}	V_{IN} = 0 to V_{CC}		-1	1	µA	
Output leakage current	I_{LO}	$\overline{CE_1}$ = V_{IH} or CE_2 = V_{IL} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL} $V_{I/O}$ = 0 V to V_{CC}		-1	1	µA	
Operating current	I_{CC}	$\overline{CE_1}$ = V_{IL}, V_{IN} = V_{IL} or V_{IH} CE_2 = V_{IH}, $I_{I/O}$ = 0 mA	t_{CYCLE} = 100 ns		40		
		CE_1 = 0.2 V, V_{IN} = 0.2 V or V_{CC} - 0.2 V CE_2 = V_{CC} - 0.2 V, $I_{I/O}$ = 0 mA	t_{CYCLE} = 1.0 µs		10		
Standby current	I_{SB1}	$\overline{CE_1}$ = V_{IH} or CE_2 = V_{IL}			3	mA	
	I_{SB}	$CE2 \leq 0.2$ V or $\overline{CE_1} \geq V_{CC}$ - 0.2 V			40	µA	1
Output voltage	V_{OL}	I_{OL} = 2.1 mA			0.4	V	
	V_{OH}	I_{OH} = -1.0 mA		2.4		V	

NOTE:
1. $CE_2 \geq V_{CC}$ - 0.2 V or $CE_2 \leq 0.2$ V

AC CHARACTERISTICS

(1) READ CYCLE (T_A = 0 to +70°C, V_{CC} = 5 V ±10%)

PARAMETER		SYMBOL	MIN.	MAX.	UNIT	NOTE
Read cycle		t_{RC}	100		ns	
Address access time		t_{AA}		100	ns	
Chip enable access time	($\overline{CE}_1$)	t_{ACE1}		100	ns	
	(CE_2)	t_{ACE2}		100	ns	
Output enable access time		t_{OE}		40	ns	
Output hold time		t_{OH}	10		ns	
Chip enable to output in Low-Z	($\overline{CE}_1$)	t_{LZ1}	10		ns	1
	(CE_2)	t_{LZ2}	10		ns	1
Output enable to output in Low-Z		t_{OLZ}	5		ns	1
Chip enable to output in High-Z	($\overline{CE}_1$)	t_{HZ1}	0	30	ns	1
	(CE_2)	t_{HZ2}	0	30	ns	1
Output disable to output in High-Z		t_{OHZ}	0	20	ns	1

NOTE:

1. Active output to high-impedance and high-impedance to output active tests specified for a ±200 mV transition from steady state levels into the test load.

(2) WRITE CYCLE (T_A = 0 to +70°C, V_{CC} = 5 V ±10%)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT	NOTE
Write cycle time	t_{WC}	100		ns	
Chip enable to end of write	t_{CW}	80		ns	
Address valid to end of write	t_{AW}	80		ns	
Address setup time	t_{AS}	0		ns	
Write pulse width	t_{WP}	60		ns	
Write recovery time	t_{WR}	0		ns	
Data valid to end of write	t_{DW}	40		ns	
Data hold time	t_{DH}	0		ns	
Output active from end of write	t_{OW}	10		ns	1
$\overline{WE}$ to output in High-Z	t_{WZ}	0	30	ns	1
$\overline{OE}$ to output in High-Z	t_{OHZ}	0	20	ns	1

NOTE:

1. Active output to high-impedance and high-impedance to output active tests specified for a ±200 mV transition from steady state levels into the test load.

AC TEST CONDITIONS

PARAMETER	MODE
Input voltage amplitude	0.6 to 2.4 V
Input rise/fall time	10 ns
Timing reference level	1.5 V
Output load conditions	1TTL + C_L (100 pF)

CAPACITANCE (T_A = 25°C, f = 1MHz)

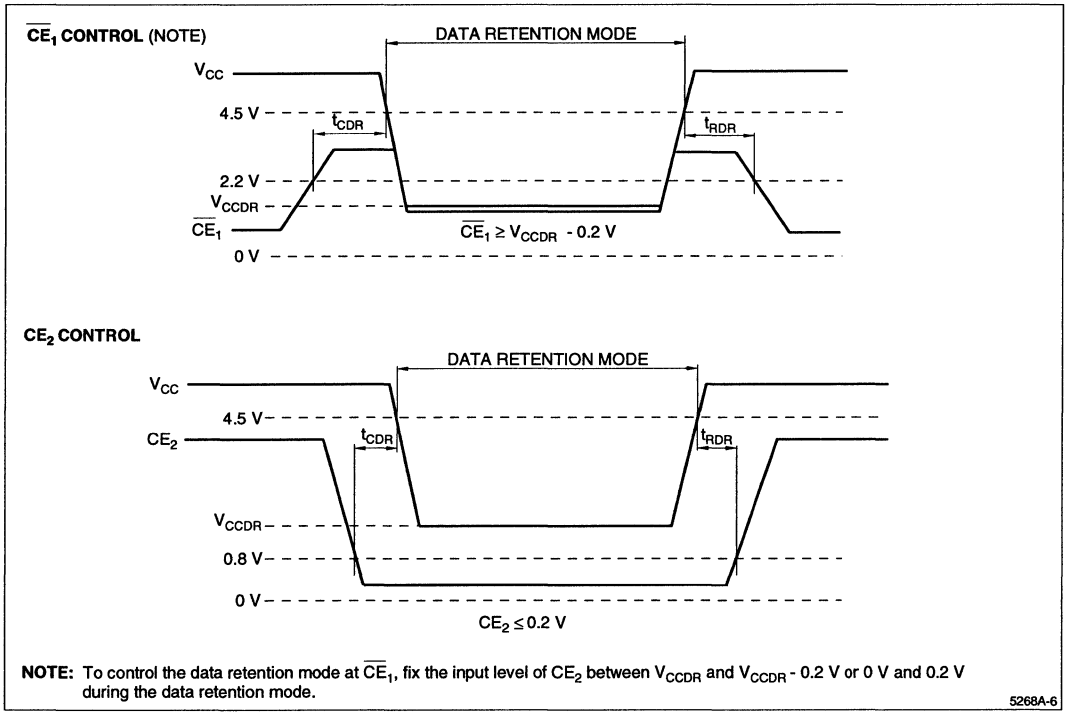
PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	
Input capacitance	C_{IN}	V_{IN} = 0 V			7	pF
Input/output capacitance	$C_{I/O}$	VI/O = 0 V			10	pF

NOTE:
1. This parameter is sampled and not production tested.

DATA RETENTION CHARACTERISTICS (T_A = 0 to +70°C)

PARAMETER	SYMBOL	CONDITIONS		MIN.	MAX.	UNIT	NOTE
Data retention voltage	V_{CCDR}	$CE_2 \le 0.2$ V or $\overline{CE}_1 \ge V_{CCDR}$ - 0.2 V		2.0	5.5	V	
Data retention current	I_{CCDR}	V_{CCDR} = 3 V, $CE_2 \le 0.2$ V or $\overline{CE}_1 \ge V_{CCDR}$ - 0.2 V	t_A = 25°C		1	µA	1
					20	µA	
Chip disable to data retention	t_{CDR}			0		ns	
Recovery time	t_{RDR}			t_{RC}		ns	2

NOTES:
1. $CE_2 \ge V_{CCDR}$ - 0.2 V or $CE_2 \le 0.2$ V
2. t_{RC} = Read cycle time



NOTE: To control the data retention mode at $\overline{CE}_1$, fix the input level of CE_2 between V_{CCDR} and V_{CCDR} - 0.2 V or 0 V and 0.2 V during the data retention mode.

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Figure 3. Low Voltage Data Retention

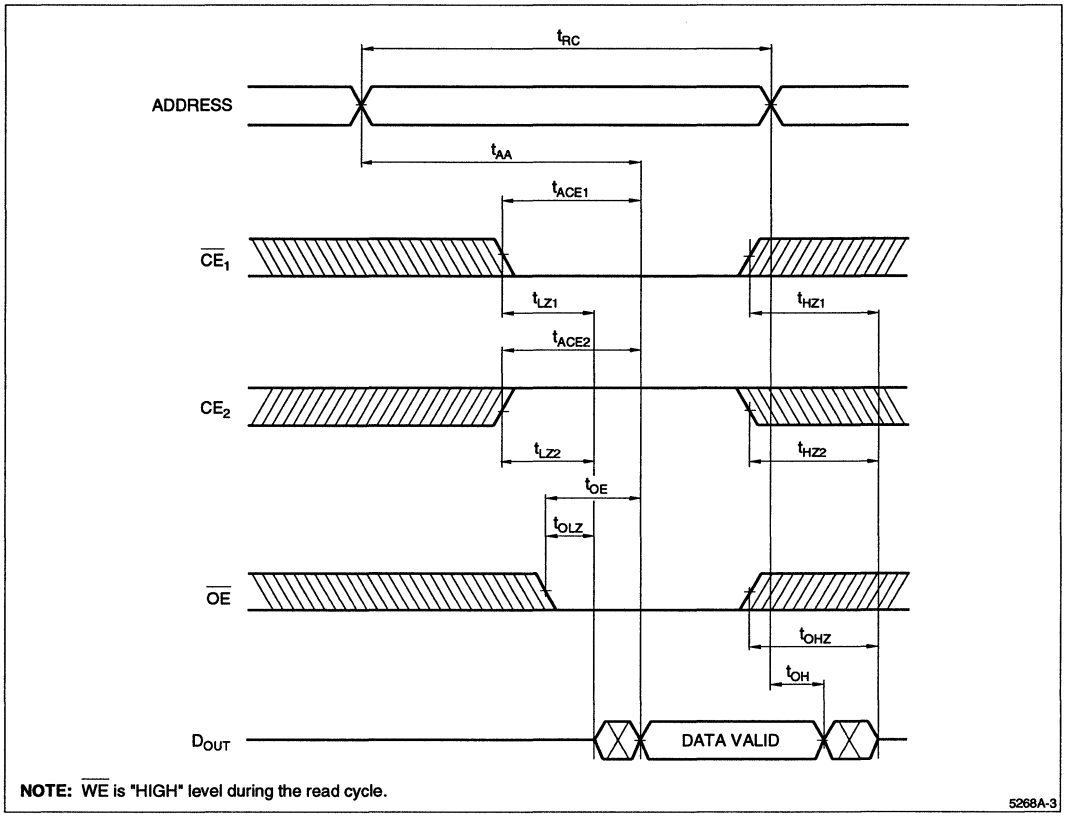
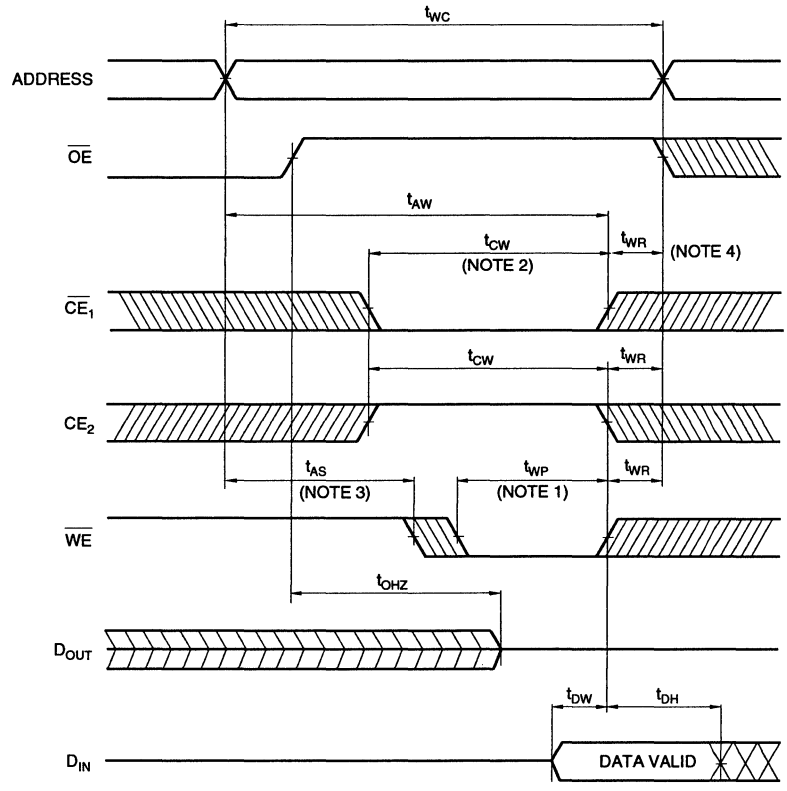


Figure 4. Read Cycle



NOTES:

1. The writing occurs during an overlapping period of $\overline{CE_1}$ = "LOW," CE_2 = "HIGH," and $\overline{WE}$ = "LOW" (t_{WP}).
2. t_{CW} is defined as the time from the last occuring transition, either $\overline{CE_1}$ LOW transition or CE_2 HIGH transition, to the time when the writing is finished.
3. t_{AS} is defined as the time from address change to writing start.
4. t_{WR} is defined as the time from writing finish to address change.

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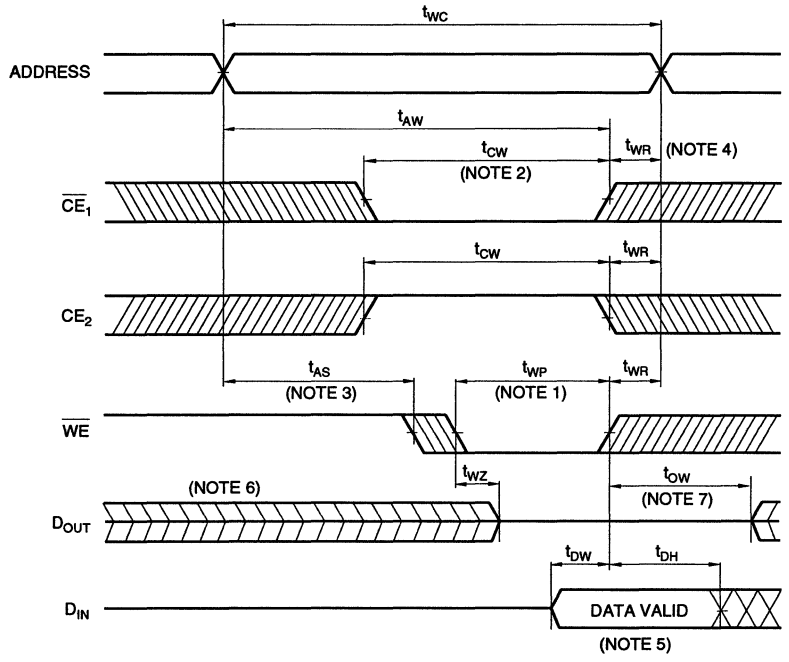
Figure 5. Write Cycle 1



NOTES:

1. The writing occurs during an overlapping period of $\overline{CE_1}$ = "LOW," CE_2 = "HIGH," and $\overline{WE}$ = "LOW" (t_{WP}).
2. t_{CW} is defined as the time from the last occuring transition, either $\overline{CE_1}$ LOW transition or CE_2 HIGH transition, to the time when the writing is finished.
3. t_{AS} is defined as the time from address change to writing start.
4. t_{WR} is defined as the time from writing finish to address change.
5. When I/O pins are in the output state, input signals with the opposite logic level must not be applied.
6. If $\overline{CE_1}$ LOW transition or CE_2 high-transition occurs at the same time or after $\overline{WE}$ LOW transition, the outputs will remain high-impedance.
7. If $\overline{CE_1}$ HIGH transition or CE_2 LOW transition occurs at the same time or before $\overline{WE}$ HIGH transit, the outputs will remain high-impedance.

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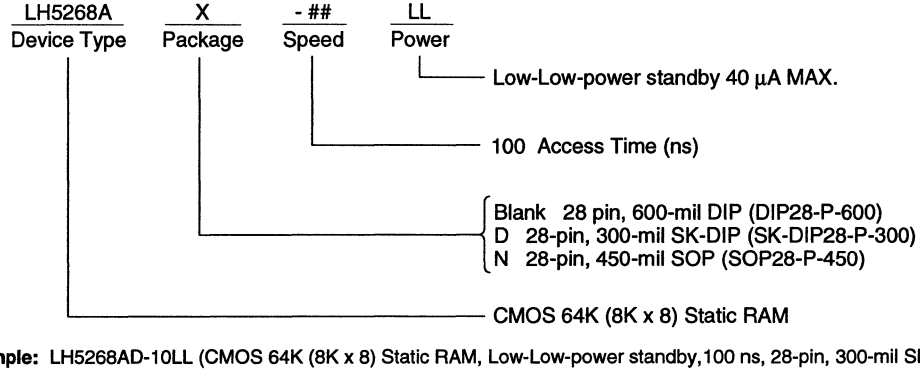
Figure 6. Write Cycle 2

ORDERING INFORMATION



Example: LH5268AD-10LL (CMOS 64K (8K x 8) Static RAM, Low-Low-power standby,100 ns, 28-pin, 300-mil SK-DIP)

5268A-7

LH51256L

CMOS 256K (32K × 8) Static RAM

FEATURES

- 32,768 × 8 bit organization
- Access times: 100/120 ns (MAX.)
- Power consumption:
  Operating: 248 mW (MAX.)
  (T_A = -40 to 85°C, minimum cycle)
  Standby: 5.5 µW (MAX.)
  (T_A = 0 to 60°C)
- Fully-static operation
- TTL compatible I/O
- Three-state outputs
- Single +5 V power supply
- Packages:
  28-pin, 600-mil DIP
  28-pin, 450-mil SOP

DESCRIPTION

The LH51256L is a 256K bit static RAM organized as 32,768 × 8 bits which provides low-power standby mode. It is fabricated using silicon-gate CMOS process technology.

PIN CONNECTIONS

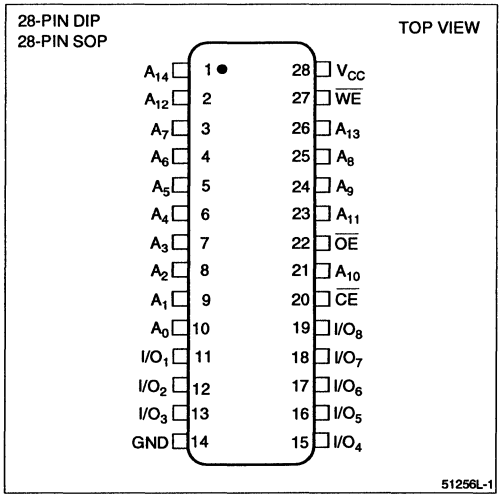


Figure 1. Pin Connections for DIP and SOP Packages

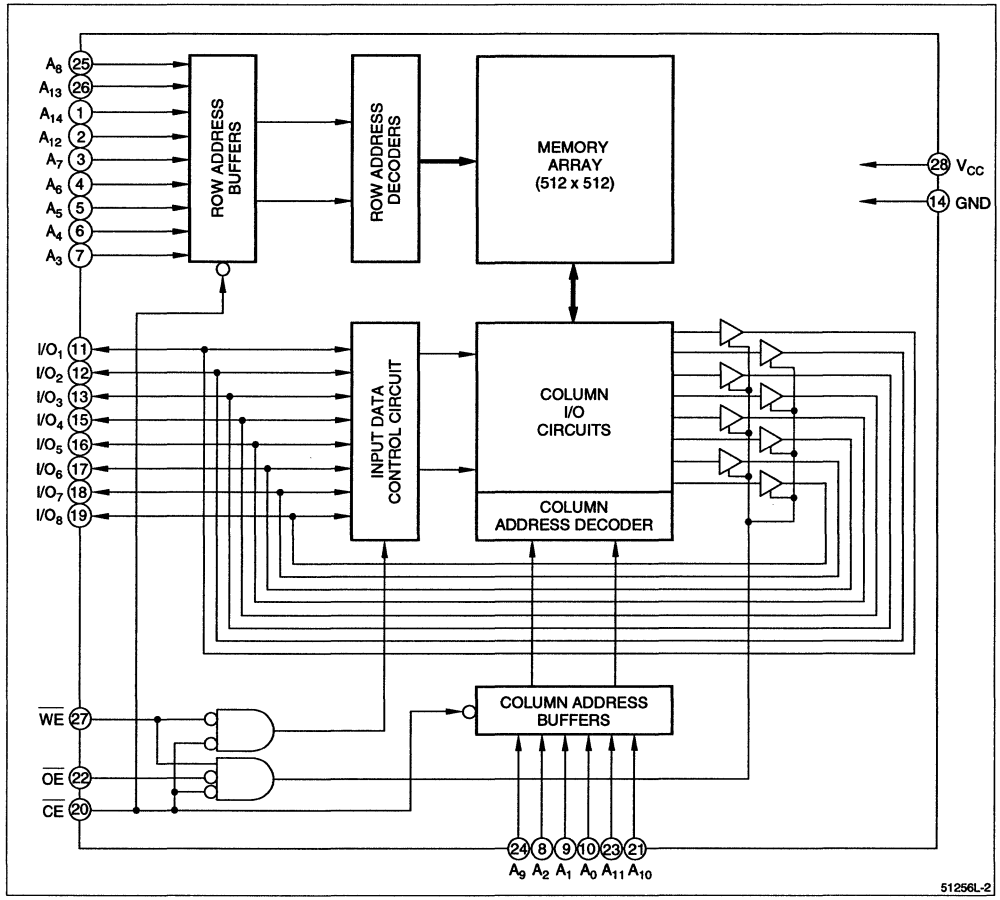


Figure 2. LH51256L Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME
A_0 - A_{14}	Address input
$\overline{CE}$	Chip Enable input
$\overline{WE}$	Write Enable input
$\overline{OE}$	Output Enable input

SIGNAL	PIN NAME
I/O_1 - I/O_8	Data Input/Output
V_{CC}	Power supply
GND	Ground

TRUTH TABLE

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	MODE	I/O_1 - I/O_8	SUPPLY CURRENT	NOTE
H	X	X	Non selected	High-Z	Standby (I_{SB})	1
L	L	X	Write	D_{IN}	Operating (I_{CC})	1
L	H	L	Read	D_{OUT}	Operating (I_{CC})	
L	H	H	Output disable	High-Z	Operating (I_{CC})	

NOTE:
1. X = H or L

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Supply voltage	V_{CC}	-0.3 to +7.0	V	1
Input voltage	V_{IN}	-0.3 to +7.0	V	1
Operating temperature	Topr	-40 to +85	°C	
Storage temperature	Tstg	-55 to +150	°C	

NOTE:
1. The maximum applicable voltage on any pin with respect to GND.

RECOMMENDED OPERATING CONDITIONS (T_A = -40 to +85°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage	V_{IH}	2.2		V_{CC} + 0.3	V
	V_{IL}	-0.3		0.8	V

DC CHARACTERISTICS (V_{CC} = 5 V ±10%, T_A = -40 to +85°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input leakage current	$\|I_{LI}\|$	V_{CC} = 5.5 V V_{IN} = 0 to V_{CC}			1	µA
Output leakage current	$\|I_{LO}\|$	$\overline{CE}$ or $\overline{OE}$ = V_{IH}, $V_{I/O}$ = 0 to V_{CC}			1	µA
Operating current	I_{CC}	$\overline{CE}$ = V_{IL}, Outputs open			45	mA
Standby current	I_{SB1}	$\overline{CE}$ = V_{IH}			10	mA
	I_{SB}	$\overline{CE}$ ≥ V_{CC} - 0.2 V T_A = 0 to +60°C			1	µA
		$\overline{CE}$ ≥ V_{CC} - 0.2 V T_A = -40 to +85°C			5	µA
Output voltage	V_{OL}	I_{OL} = 2.1 mA			0.4	V
	V_{OH}	I_{OH} = -1.0 mA	2.4			V

AC CHARACTERISTICS

(1) READ CYCLE (V_{CC} = 5 V ±10%, T_A = -40 to +85°C)

PARAMETER	SYMBOL	LH51256/N-10L		LH51256/N-12L		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.		
Read cycle time	t_{RC}	100		120		ns	
Address access time	t_{AA}		100		120	ns	
Chip enable access time	t_{ACE}		100		120	ns	
Output enable access time	t_{OE}		50		60	ns	
Output hold time	t_{OH}	5		5		ns	
$\overline{CE}$ Low to output in Low-Z	t_{LZ}	5		5		ns	1
$\overline{OE}$ Low to output in Low-Z	t_{OLZ}	5		5		ns	1
$\overline{CE}$ High to output in High-Z	t_{HZ}	0	30	0	30	ns	1
$\overline{OE}$ High to output in High-Z	t_{OHZ}	0	30	0	30	ns	1

(2) WRITE CYCLE (V_{CC} = 5 V ±10%, T_A = -40 to +85°C)

PARAMETER	SYMBOL	LH51256/N-10L		LH51256/N-12L		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.		
Write cycle time	t_{WC}	100		120		ns	
$\overline{CE}$ Low to end of write	t_{CW}	90		100		ns	
Address valid to end of write	t_{AW}	90		100		ns	
Address setup time	t_{AS}	5		5		ns	
Write recovery time	t_{WR}	15		15		ns	
Write pulse width	t_{WP}	50		50		ns	
Input data setup time	t_{DW}	30		30		ns	
Input data hold time	t_{DH}	10		10		ns	
$\overline{WE}$ High to output in High-Z	t_{OW}	0		0		ns	1
$\overline{WE}$ Low to output in High-Z	t_{WZ}	0	30	0	30	ns	1
$\overline{OE}$ High to output in High-Z	t_{OHZ}	0	30	0	30	ns	1

NOTE:

1. Active output to high-impedance and high-impedance to output active tests specified for a ±500 mV transition from steady state levels into the test load. C_{LOAD} = 5 pF.

AC TEST CONDITIONS

PARAMETER	MODE
Input voltage amplitude	0.6 V to 2.4 V
Input rise/fall time	10 ns
Timing reference level	1.5 V
Output load conditions	1TTL + C_L = 100 pF (Includes scope and jig capacitance)

CAPACITANCE [1] (T_A = 25°C, f = 1MHz)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input capacitance	C_{IN}	V_{IN} = 0 V			7	pF
Input/output capacitance	$C_{I/O}$	$V_{I/O}$ = 0 V			10	pF

NOTE:

1. This parameter is sampled and not production tested.

DATA RETENTION CHARACTERISTICS (T_A = -40 TO +85°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Data retention voltage	V_{CCDR}	$\overline{CE} \geq V_{CCDR}$ - 0.2 V	2.0			V	
Data retention current	I_{CCDR}	V_{CCDR} = 3.0 V, $\overline{CE} \geq V_{CCDR}$ - 0.2 V, T_A = 0 to +60°C, V_{IN} = 0 to V_{CCDR}			0.6	µA	
		V_{CCDR} = 3.0 V $\overline{CE} \geq V_{CCDR}$ - 0.2 V, T_A = -40 to +85°C, V_{IN} = 0 to V_{CCDR}			3.0	µA	
$\overline{CE}$ setup time	t_{CDR}		0			ns	
$\overline{CE}$ hold time	t_{RDR}		t_{RC}			ns	1

NOTE:

1. t_{RC} = Read cycle time

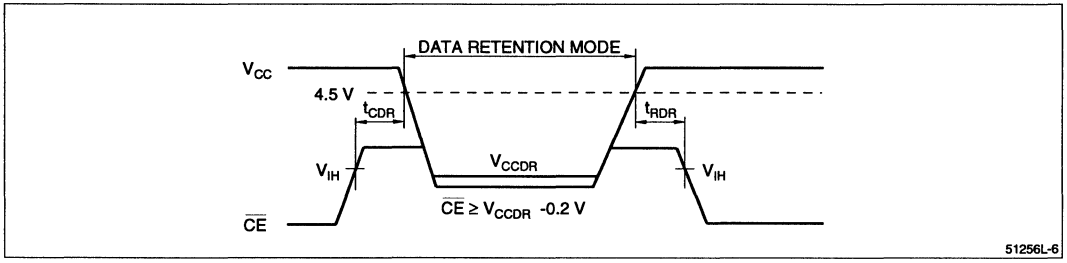


Figure 3. Data Retention Characteristics

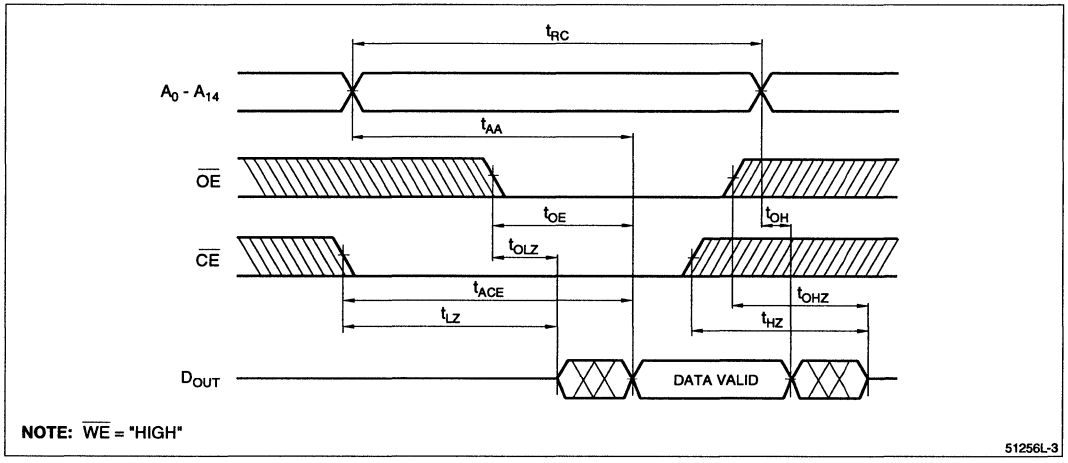
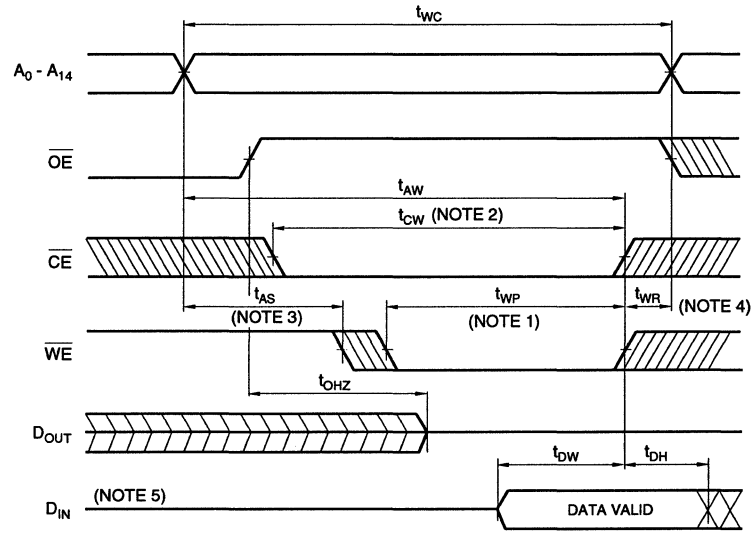


Figure 4. Read Cycle



NOTES:

1. The write pulse occurs during the overlap (t_{WP}) of $\overline{CE}$ = LOW and $\overline{WE}$ = LOW.
2. t_{CW} is defined as the time from $\overline{CE}$ LOW transition to the end of writing.
3. t_{AS} is defined as the time from address change to the start of writing.
4. t_{WR} is defined as the time from the end of writing to the address change.
5. When the I/O pins are in the output state, input signals with the opposite logic level must not be applied.

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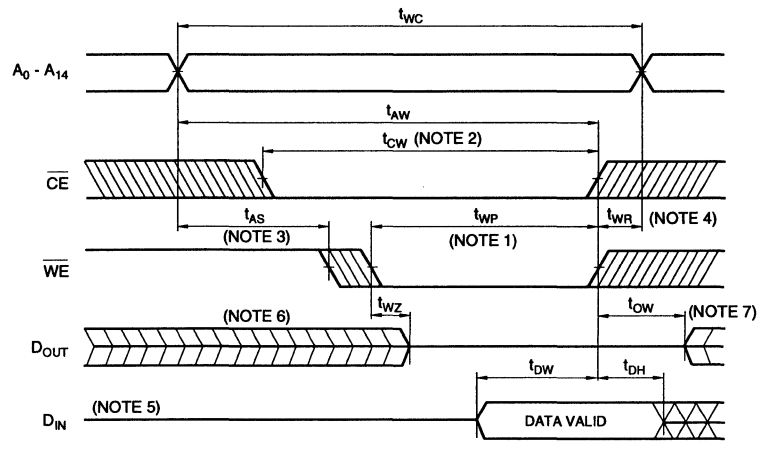
Figure 5. Write Cycle 1 ($\overline{OE}$ Clock)



NOTES:

1. The write pulse occurs during the overlap (t_{WP}) of $\overline{CE}$ = LOW and $\overline{WE}$ = LOW.
2. t_{CW} is defined as the time from $\overline{CE}$ LOW transition to the end of writing.
3. t_{AS} is defined as the time from address change to the start of writing.
4. t_{WR} is defined as the time from the end of writing to the address change.
5. When the I/O pins are in the output state, input signals with the opposite logic level must not be applied.
6. If $\overline{CE}$ LOW transition occurs at the same time or after $\overline{WE}$ LOW transition, the output will remain high-impedance.
7. If $\overline{CE}$ HIGH transition occurs at the same time or prior to the $\overline{WE}$ HIGH transition, the output will remain high-impedance.

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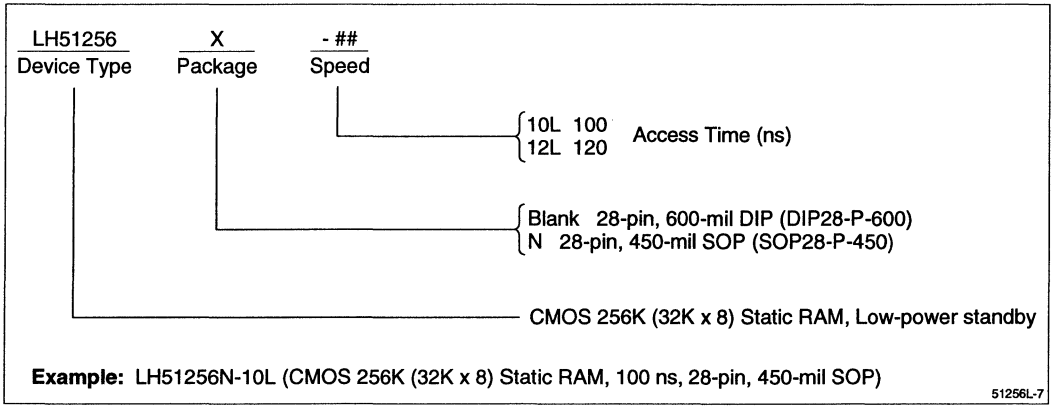
Figure 6. Write Cycle 2 ($\overline{OE}$ Low)

ORDERING INFORMATION



Example: LH51256N-10L (CMOS 256K (32K x 8) Static RAM, 100 ns, 28-pin, 450-mil SOP)

51256L-7

LH52B256

CMOS 32K × 8 Static RAM

FEATURES

- Access Times: 70/100 ns
- Automatic Power Down During Long Read Cycles
- Low-Power Standby When Deselected
- TTL Compatible I/O
- 5 V ± 10% Supply
- Fully-Static Operation
- 2 V Data Retention
- Packages:
  - 28-Pin, 300-mil DIP
  - 28-Pin, 600-mil DIP
  - 28-Pin, 450-mil SOP
  - 28-Pin, 8 × 13 mm^2 TSOP (Type I)

FUNCTIONAL DESCRIPTION

The LH52B256 is a high-density 262,144 bit static RAM organized as 32K×8. An efficient design is obtained with a CMOS periphery and a matrix constructed with polysilicon load memory cells.

This RAM is fully static in operation. The Chip Enable ($\overline{E}$) control permits Read and Write operations when active (LOW) or places the RAM in a low-power standby mode when inactive (HIGH). Standby power (I_{SB1}) drops to its lowest level if $\overline{E}$ is raised to within 0.2 V of V_{CC}.

Write cycles occur when both Chip Enable ($\overline{E}$) and Write Enable ($\overline{W}$) are LOW. Data is transferred from the DQ pins to the memory location specified by the 15 address lines. The proper use of the Output Enable control ($\overline{G}$) can prevent bus contention.

When $\overline{E}$ is LOW and $\overline{W}$ is HIGH, a static Read will occur at the memory location specified by the address lines. $\overline{G}$ must be brought LOW to enable the outputs. Since the device is fully static in operation, new Read cycles can be performed by simply changing the address. An Automatic Power Down feature decreases current consumption when Read cycles extend beyond their minimum cycle time.

High-frequency design techniques should be employed to obtain the best performance from this device. Solid, low-impedance power and ground planes, with high-frequency decoupling capacitors, are recommended. Series termination of the inputs should be considered when transmission line effects occur.

PIN CONNECTIONS

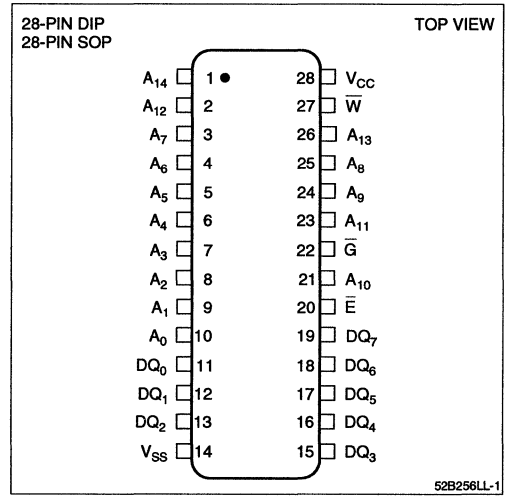


Figure 1. Pin Connections for DIP and SOP Packages

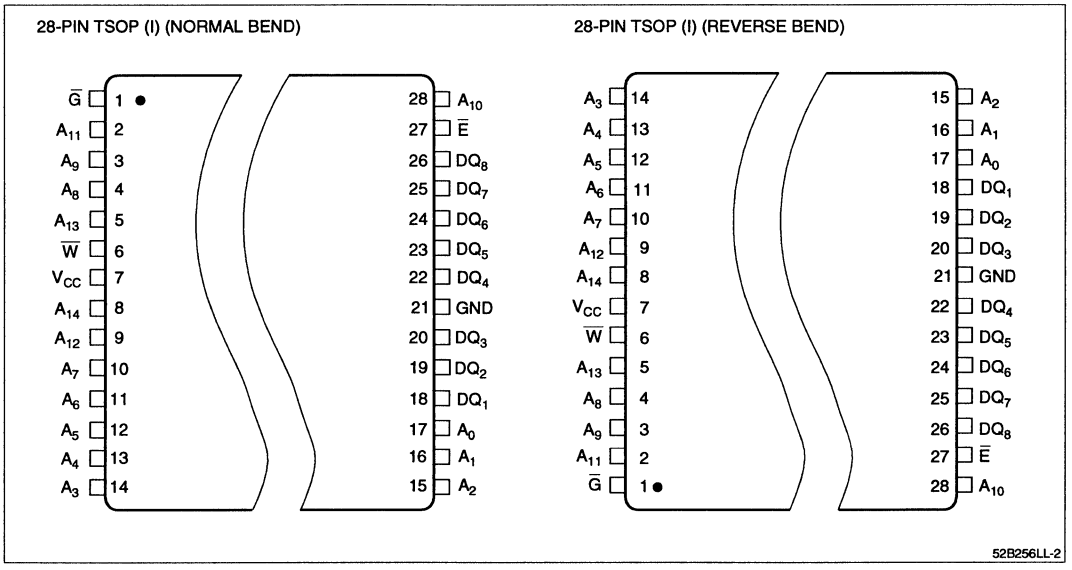


Figure 2. Pin Connections for TSOP Packages

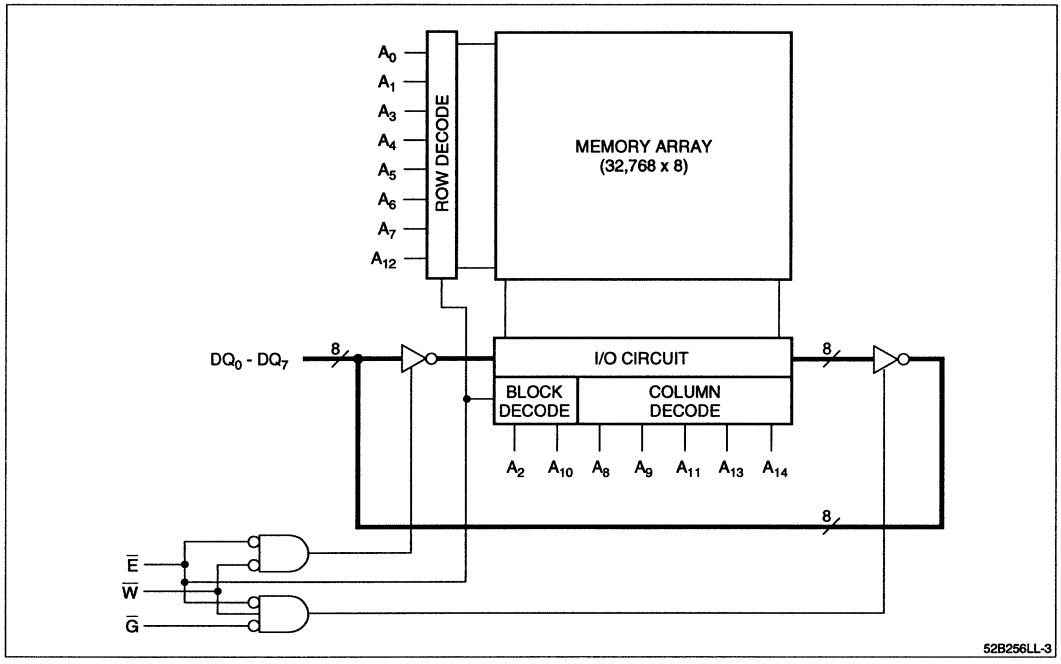


Figure 3. LH52B256 Block Diagram

TRUTH TABLE

$\overline{E}$	$\overline{G}$	$\overline{W}$	MODE	DQ	Icc
H	X	X	Standby	High-Z	Standby
L	H	H	Read	High-Z	Active
L	L	H	Read	Data Out	Active
L	X	L	Write	Data In	Active

NOTE:
X = Don't Care, L = LOW, H = HIGH

PIN DESCRIPTIONS

PIN	DESCRIPTION
$A_0 - A_{14}$	Address Inputs
$DQ_0 - DQ_7$	Data Inputs/Outputs
$\overline{E}$	Chip Enable input
$\overline{G}$	Output Enable input
$\overline{W}$	Write Enable input
V_{CC}	Positive Power Supply
V_{SS}	Ground

ABSOLUTE MAXIMUM RATINGS [1]

PARAMETER	RATING
V_{CC} to V_{SS} Potential	−0.5 V to 7 V
Input Voltage Range	−0.5 V to V_{CC} + 0.5 V
DC Output Current [2]	± 40 mA
Storage Temperature Range	−65°C to 150°C
Power Dissipation (Package Limit)	1.0 W

NOTES:

1. Stresses greater than those listed under 'Absolute Maximum Ratings' may cause permanent damage to the device. This is a stress rating for transient conditions only. Functional operation of the device at these or any other conditions above those indicated in the 'Operating Range' of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Outputs should not be shorted for more than 30 seconds. No more than one output should be shorted at any time.

OPERATING RANGES

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
T_A	Temperature, Ambient	0		70	°C
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
V_{SS}	Supply Voltage	0	0	0	V
V_{IL}	Logic '0' Input Voltage [1]	−0.5		0.8	V
V_{IH}	Logic '1' Input Voltage	2.2		V_{CC} + 0.5	V

NOTE:

1. Negative undershoot of up to 3.0 V is permitted once per cycle.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC1}	Operating Current [1]	t_{RC} = 70 ns			70	mA
I_{CC1}	Operating Current [1]	t_{RC} = 100 ns			70	mA
I_{SB1}	Standby Current	$\overline{E} \geq V_{CC} - 0.2$ V			40	µA
I_{SB2}	Standby Current	$\overline{E} \geq V_{IH}$			3	mA
I_{LI}	Input Leakage Current	V_{IN} = 0 V to V_{CC}	−1		1	µA
I_{LO}	I/O Leakage Current	V_{IN} = 0 V to V_{CC}	−1		1	µA
V_{OH}	Output High Voltage	I_{OH} = −1.0 mA	2.4			V
V_{OL}	Output Low Voltage	I_{OL} = 2.0 mA			0.4	V
V_{DR}	Data Retention Voltage	$\overline{E} \geq V_{CC} - 0.2$ V	2		5.5	V
I_{DR}	Data Retention Current	VCC = 3 V, $\overline{E} \geq V_{CC} - 0.2$ V		6	20	µA

NOTE:

1. I_{CC} is dependent upon output loading and cycle rates. Specified values are with outputs open, operating at specified cycle times.

AC TEST CONDITIONS

PARAMETER	RATING
Input Pulse Levels	0.6 to 2.4 V
Input Rise and Fall Times	10 ns
Input and Output Timing Ref. Levels	1.5 V
Output Load, Timing Tests	Figure 3

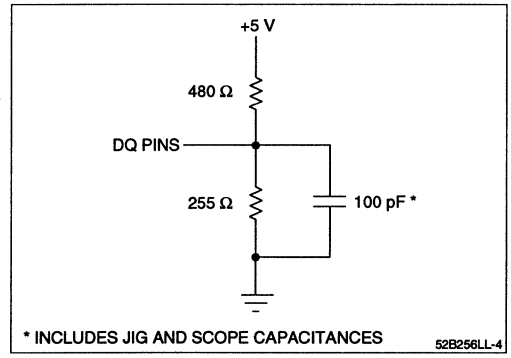


Figure 4. Output Load Circuit

CAPACITANCE [1,2]

PARAMETER	RATING
C_{IN} (Input Capacitance)	7 pF
C_{DQ} (I/O Capacitance)	10 pF

NOTES:

1. Capacitances are maximum values at 25°C measured at 1.0 MHz with V_{Bias} = 0 V and V_{CC} = 5.0 V.
2. Sample tested only.

DATA RETENTION TIMING

$\overline{E}$ must be held above the lesser of V_{IH} or V_{CC} – 0.2 V to assure proper operation when V_{CC} < 4.5 V. $\overline{E}$ must be V_{CC} – 0.2 V or greater to meet I_{DR} specification. All other inputs are 'Don't Care.'

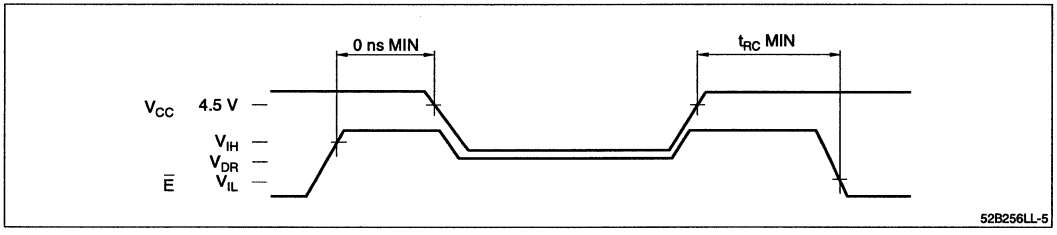


Figure 5. Data Retention Timing

AC ELECTRICAL CHARACTERISTICS [1] (Over Operating Range)

SYMBOL	DESCRIPTION	-70		-10		UNITS
		MIN	MAX	MIN	MAX	
	READ CYCLE					
t_{RC}	Read Cycle Time	70		100		ns
t_{AA}	Address Access Time		70		100	ns
t_{OH}	Output Hold from Address Change	10		10		ns
t_{EA}	$\overline{E}$ Low to Valid Data		70		100	ns
t_{ELZ}	$\overline{E}$ Low to Output Active [2,3]	10		5		ns
t_{EHZ}	$\overline{E}$ High to Output High-Z [2,3]	0	35	0	45	ns
t_{GA}	$\overline{G}$ Low to Valid Data		40		60	ns
t_{GLZ}	$\overline{G}$ Low to Output Active [2,3]	5		5		ns
t_{GHZ}	$\overline{G}$ High to Output High-Z [2,3]	0	35	0	45	ns
	WRITE CYCLE					
t_{WC}	Write Cycle Time	70		100		ns
t_{EW}	$\overline{E}$ Low to End of Write	60		65		ns
t_{AW}	Address Valid to End of Write	60		90		ns
t_{AS}	Address Setup	0		0		ns
t_{WR}	Address Hold from End of Write	0		0		ns
t_{WP}	$\overline{W}$ Pulse Width	55		65		ns
t_{DW}	Input Data Setup Time	30		35		ns
t_{DH}	Input Data Hold Time	0		0		ns
t_{WHZ}	$\overline{W}$ Low to Output High-Z [2,3]	0	40	0	45	ns
t_{WLZ}	$\overline{W}$ High to Output Active [2,3]	5		5		ns

NOTES:

1. AC Electrical Characteristics specified at 'AC Test Conditions' levels.
2. Active output to High-Z and High-Z to output active tests specified for a ±200 mV transition from steady state levels into the test load.
3. Sample tested only.

TIMING DIAGRAMS – READ CYCLE

Read Cycle No. 1

Chip is in Read Mode: $\overline{W}$ is HIGH, $\overline{E}$ is LOW and $\overline{G}$ is LOW. Read Cycle timing is referenced from when all addresses are stable until the first address transition. Crosshatched portion of Data Out implies that data lines are in the Low-Z state but the data is not guaranteed to be valid until t_{AA}.

Read Cycle No. 2

Chip is in Read Mode: $\overline{W}$ is HIGH. Timing illustrated for the case when addresses are valid before $\overline{E}$ goes LOW. Data Out is not specified to be valid until t_{EA} or t_{GA}, but may become valid as soon as t_{ELZ} or t_{GLZ}. Outputs will transition directly from High-Z to Valid Data Out. Valid Data will be present following t_{GA} only if t_{EA} timing is met.

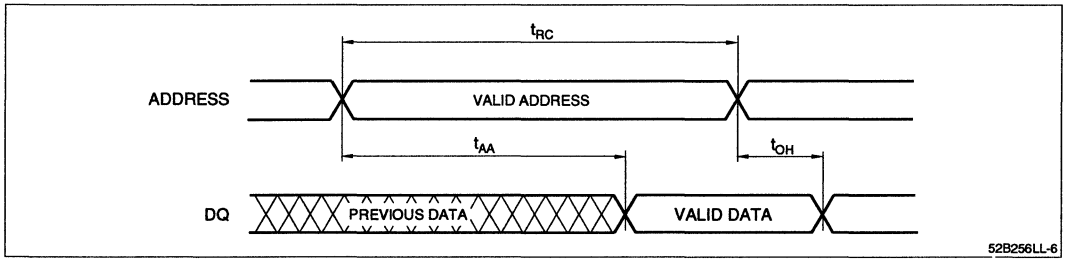


Figure 6. Read Cycle No. 1

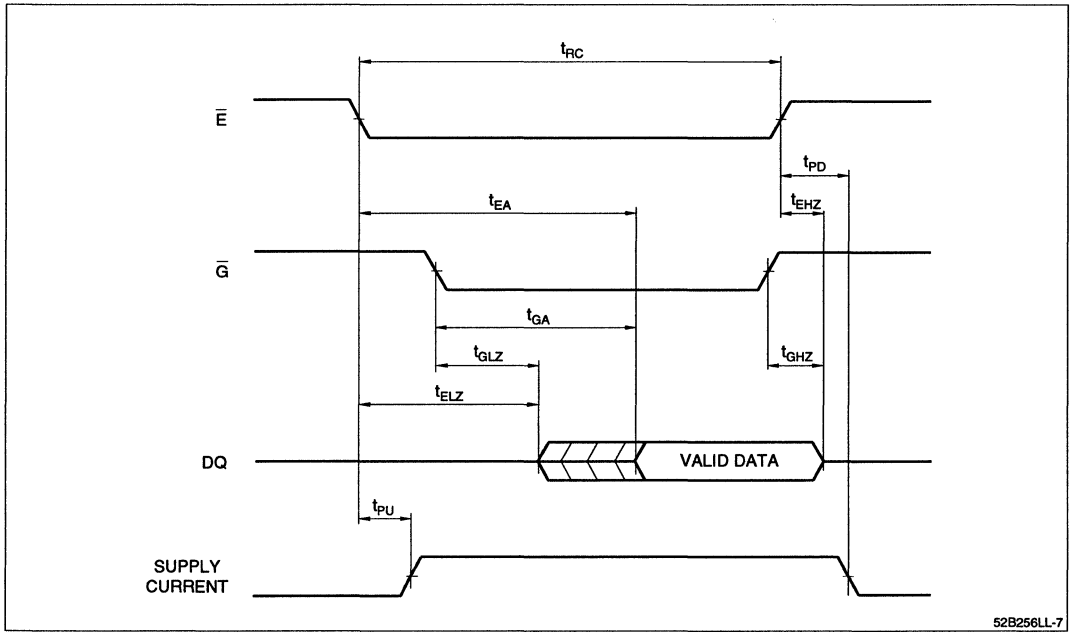


Figure 7. Read Cycle No. 2

TIMING DIAGRAMS – WRITE CYCLE

Addresses must be stable during Write Cycles. The outputs will remain in the High-Z state if $\overline{W}$ is LOW when $\overline{E}$ goes LOW. If $\overline{G}$ is HIGH, the outputs will remain in the High-Z state. Although these examples illustrate timing with $\overline{G}$ active, it is recommended that $\overline{G}$ be held HIGH for all Write cycles. This will prevent the LH52B256LL's outputs from becoming active, preventing bus contention, thereby reducing system noise.

Write Cycle No. 1 ($\overline{W}$ Controlled)

Chip is selected: $\overline{E}$ is LOW, $\overline{G}$ is LOW. Using only $\overline{W}$ to control Write Cycles may not offer the best performance since both t_{WHZ} and t_{DW} timing specifications must be met.

Write Cycle No. 2 ($\overline{E}$ Controlled)

$\overline{G}$ is LOW. DQ lines may transition to Low-Z if the falling edge of $\overline{W}$ occurs after the falling edge of $\overline{E}$.

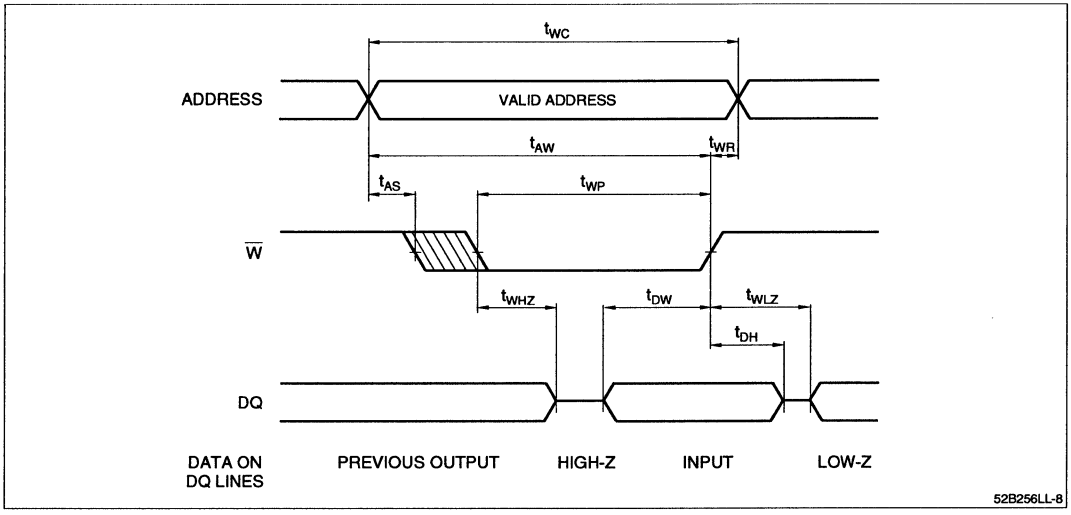


Figure 8. Write Cycle No. 1

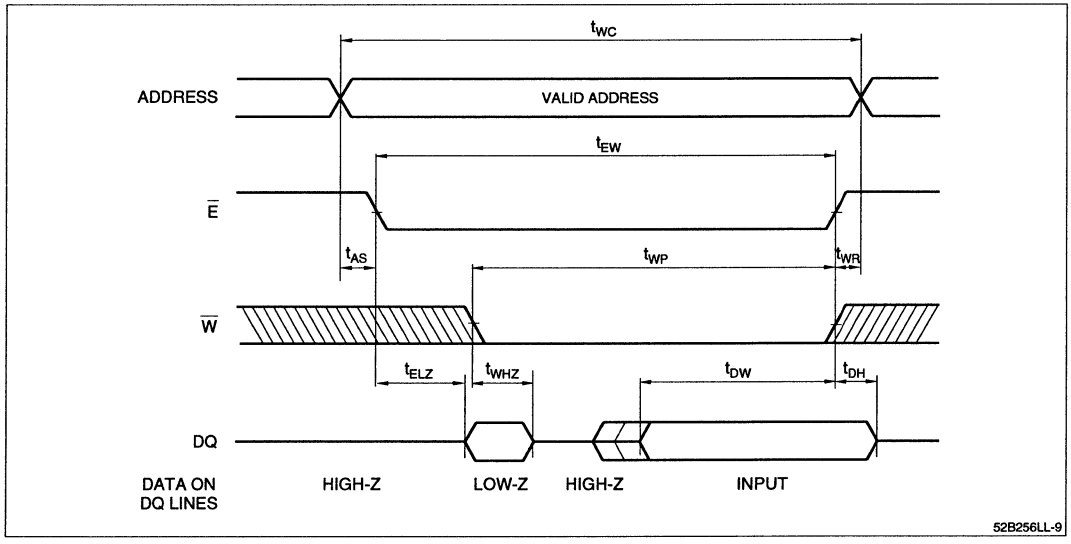
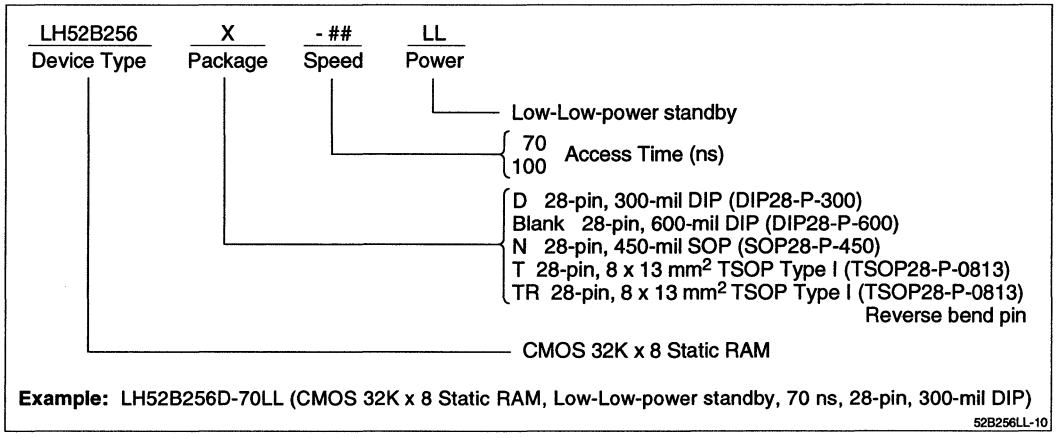


Figure 9. Write Cycle No. 2

ORDERING INFORMATION



Example: LH52B256D-70LL (CMOS 32K x 8 Static RAM, Low-Low-power standby, 70 ns, 28-pin, 300-mil DIP)

52B256LL-10

LH52252A

CMOS 64K × 4 Static RAM

FEATURES

- Fast Access Times: 25/35/45 ns
- Low-Power Standby When Deselected
- TTL Compatible I/O
- 5 V ± 10% Supply
- Fully-Static Operation
- Common I/O for Low Pin Count
- JEDEC Standard Pinouts
- Packages:
  - 24-Pin, 300-mil DIP
  - 24-Pin, 300-mil SOJ

FUNCTIONAL DESCRIPTION

The LH52252A is a high-speed 262,144 bit static RAM organized as 64K × 4. A fast, efficient design is obtained with a CMOS periphery and a matrix constructed with polysilicon load memory cells.

This RAM is fully static in operation. The Chip Enable ($\overline{E}$) reduces power to the chip when $\overline{E}$ is HIGH. Standby power (I_{SB1}) drops to its lowest level when $\overline{E}$ is raised to within 0.2 V of V_{CC}.

Write cycles occur when both $\overline{E}$ and Write Enable ($\overline{W}$) are LOW. Data is transferred from the DQ pins to the memory location specified by the 16 address lines.

Read cycles occur when $\overline{E}$ is LOW and $\overline{W}$ is HIGH. A Read cycle will begin upon an address transition, on a falling edge of $\overline{E}$, or on a rising edge of $\overline{W}$.

High-frequency design techniques should be employed to obtain the best performance from this device. Solid, low-impedance power and ground planes, with high-frequency decoupling capacitors, are recommended. Series termination of the inputs should be considered when transmission line effects occur.

PIN CONNECTIONS

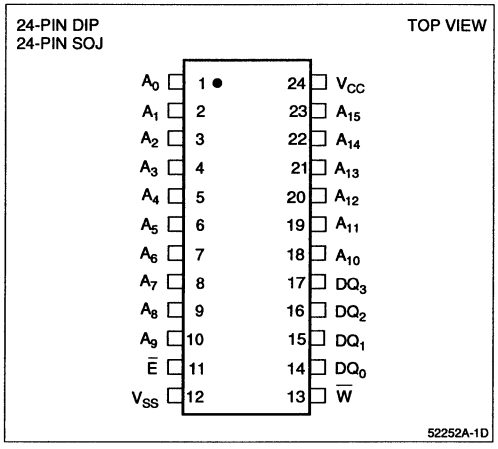


Figure 1. Pin Connections for DIP and SOJ Packages

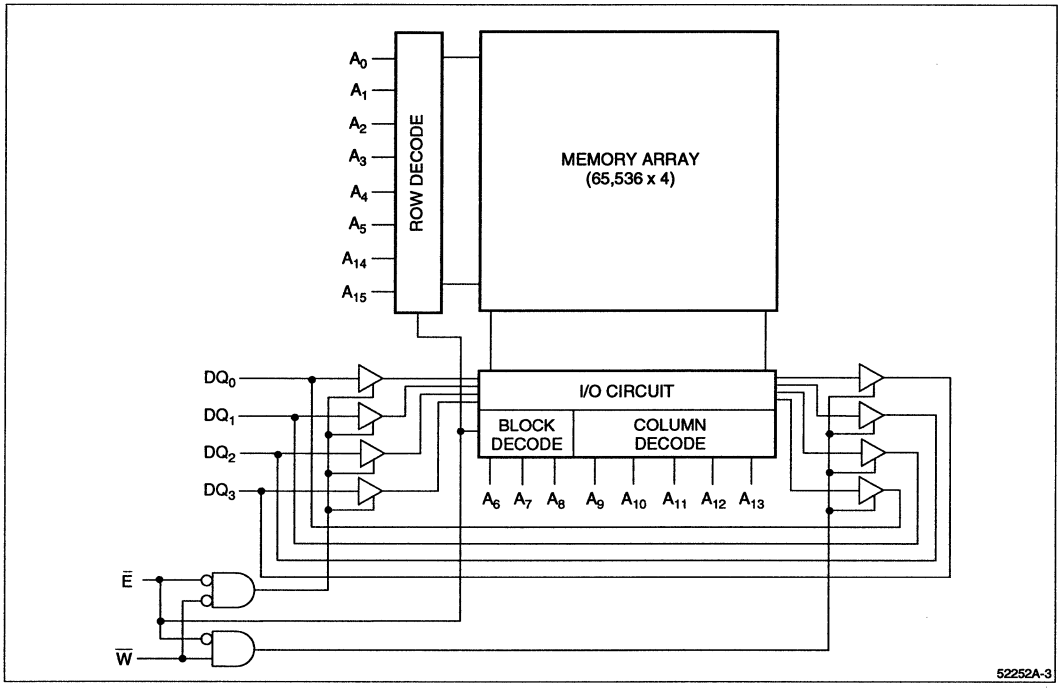


Figure 2. LH52252A Block Diagram

TRUTH TABLE

$\overline{E}$	$\overline{W}$	MODE	DQ	I_{CC}
H	X	Not Selected	High-Z	Standby
L	H	Read	Data Out	Active
L	L	Write	Data In	Active

NOTE:
X = Don't Care, L = LOW, H = HIGH

PIN DESCRIPTIONS

PIN	DESCRIPTION
$A_0 - A_{15}$	Address Inputs
$DQ_0 - DQ_3$	Data Inputs/Outputs
$\overline{E}$	Chip Enable input
$\overline{W}$	Write Enable input
V_{CC}	Positive Power Supply
V_{SS}	Ground

ABSOLUTE MAXIMUM RATINGS [1]

PARAMETER	RATING
V_{CC} to V_{SS} Potential	−0.5 V to 7 V
Input Voltage Range	−0.5 V to V_{CC}+0.5 V
DC Output Current [2]	± 40 mA
Storage Temperature Range	−65°C to 150°C
Power Dissipation (Package Limit)	1.0 W

NOTES:

1. Stresses greater than those listed under 'Absolute Maximum Ratings' may cause permanent damage to the device. This is a stress rating for transient conditions only. Functional operation of the device at these or any other conditions above those indicated in the 'Operating Range' of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Outputs should not be shorted for more than 30 seconds. No more than one output should be shorted at any time.

OPERATING RANGES

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
T_A	Temperature, Ambient	0		70	°C
V_{CC}	Supply Voltage	4.5		5.5	V
V_{SS}	Supply Voltage	0		0	V
V_{IL}	Logic '0' Input Voltage [1]	−0.5		0.8	V
V_{IH}	Logic '1' Input Voltage	2.2		V_{CC} + 0.5	V

NOTE:

1. Negative undershoot of up to 3.0 V is permitted once per cycle.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP [1]	MAX	UNIT
I_{CC1}	Operating Current [2]	Outputs open, t_{RC} = 25 ns		110	150	mA
I_{CC1}	Operating Current [2]	Outputs open, t_{RC} = 35 ns		95	120	mA
I_{CC1}	Operating Current [2]	Outputs open, t_{RC} = 45 ns		85	100	mA
I_{SB1}	Standby Current	$\overline{E} \geq V_{CC} - 0.2$ V		0.02	1	mA
I_{SB2}	Standby Current	$\overline{E} \geq V_{IH}$		3	5	mA
I_{LI}	Input Leakage Current	V_{IN} = 0 V to V_{CC}	−2		2	µA
I_{LO}	I/O Leakage Current	V_{IN} = 0 V to V_{CC}	−2		2	µA
V_{OH}	Output High Voltage	I_{OH} = −4.0 mA	2.4			V
V_{OL}	Output Low Voltage	I_{OL} = 8.0 mA			0.4	V

NOTES:

1. Typical values at V_{CC} = 5 V, T_A = 25°C.
2. I_{CC} is dependent upon output loading and cycle rates. Specified values are with outputs open, operating at specified cycle times.

AC TEST CONDITIONS

PARAMETER	RATING
Input Pulse Levels	V_{SS} to 3 V
Input Rise and Fall Times	5 ns
Input and Output Timing Ref. Levels	1.5 V
Output Load, Timing Tests	Figure 3

CAPACITANCE [1,2]

PARAMETER	RATING
C_{IN} (Input Capacitance)	6 pF
C_{DQ} (I/O Capacitance)	8 pF

NOTES:

1. Capacitances are maximum values at 25°C measured at 1.0 MHz with V_{Bias} = 0 V and V_{CC} = 5.0 V.
2. Sample tested only.

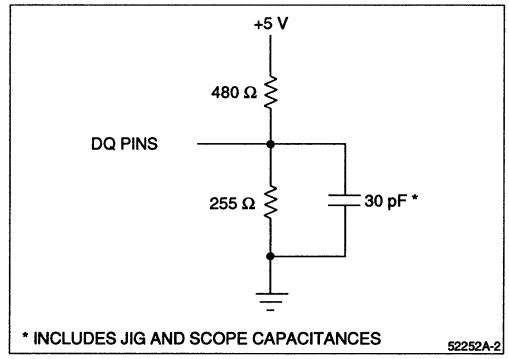


Figure 3. Output Load Circuit

AC ELECTRICAL CHARACTERISTICS [1] (Over Operating Range)

SYMBOL	DESCRIPTION	-25		-35		-45		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	
READ CYCLE								
t_{RC}	Read Cycle Timing	25		35		45		ns
t_{AA}	Address Access Time		25		35		45	ns
t_{OH}	Output Hold from Address Change	3		3		3		ns
t_{EA}	$\overline{E}$ Low to Valid Data		25		35		45	ns
t_{ELZ}	$\overline{E}$ Low to Output Active [3]	5		5		5		ns
t_{EHZ}	$\overline{E}$ High to Output High-Z [2,3]		12		15		20	ns
t_{PU}	$\overline{E}$ Low to Power Up Time [4]	0		0		0		ns
t_{PD}	$\overline{E}$ High to Power Down Time [4]		30		35		40	ns
WRITE CYCLE								
t_{WC}	Write Cycle Time	25		35		45		ns
t_{EW}	$\overline{E}$ Low to End of Write	20		30		35		ns
t_{AW}	Address Valid to End of Write	20		30		35		ns
t_{AS}	Address Setup	0		0		0		ns
t_{AH}	Address Hold from End of Write	0		0		0		ns
t_{WP}	$\overline{W}$ Pulse Width	20		25		35		ns
t_{DW}	Input Data Setup Time	12		15		20		ns
t_{DH}	Input Data Hold Time	0		0		0		ns
t_{WHZ}	$\overline{W}$ Low to Output High-Z [2,3]		8		10		15	ns
t_{WLZ}	$\overline{W}$ High to Output Active [3]	0		0		0		ns

NOTES:

1. AC Electrical Characteristics specified at 'AC Test Conditions' levels.
2. Active output to High-Z and High-Z to output active tests specified for a ±200 mV transition from steady state levels into the test load.
3. Sample tested only.
4. Guaranteed but not tested.

TIMING DIAGRAMS – READ CYCLE

Read Cycle No. 1

Chip is in Read Mode: $\overline{W}$ is HIGH, and $\overline{E}$ is LOW. Read cycle timing is referenced from when all addresses are stable until the first address transition. Crosshatched portion of DQ implies that data lines are in the Low-Z state and the data may not be valid.

Read Cycle No. 2

Chip is in Read Mode: $\overline{W}$ is HIGH. Timing illustrated for the case when addresses are valid while $\overline{E}$ goes LOW. Data Out is not specified to be valid until t_{EA}, but may become valid as soon as t_{ELZ}. Outputs will transition from High-Z to Valid Data Out.

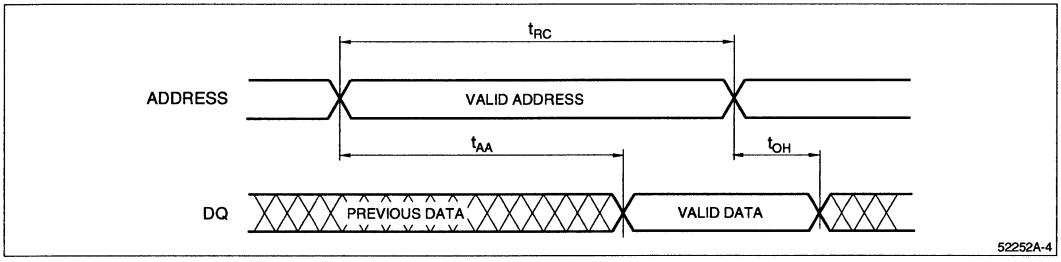


Figure 4. Read Cycle No. 1

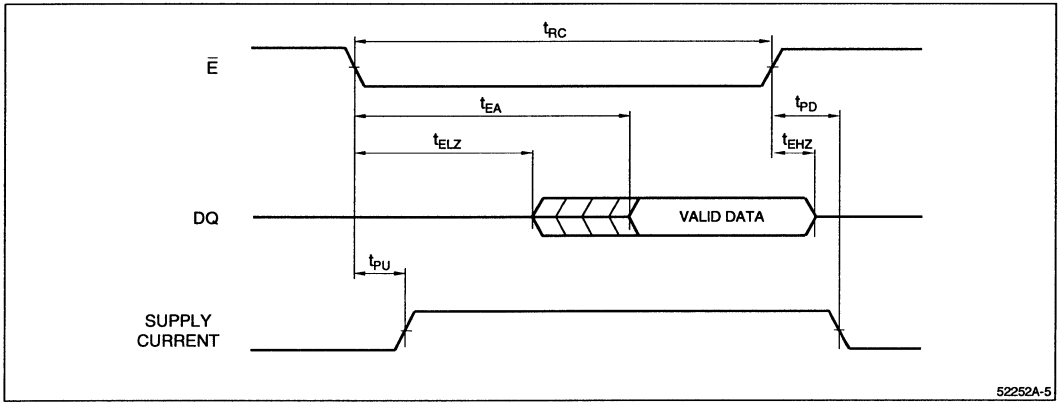


Figure 5. Read Cycle No. 2

TIMING DIAGRAMS – WRITE CYCLE

Addresses must be stable during Write cycles. $\overline{E}$ or $\overline{W}$ must be high during address transitions. The outputs will remain in the High-Z state if $\overline{W}$ is LOW when $\overline{E}$ goes LOW. Care should be taken so that the output drivers are disabled prior to placing the Input Data on the DQ lines. This will prevent bus contention, reducing system noise.

Write Cycle No. 1 ($\overline{W}$ Controlled)

Chip is selected: $\overline{E}$ is LOW. Using only $\overline{W}$ to control Write cycles may not offer the best device performance, since both t_{WHZ} and t_{DW} timing specifications must be met.

Write Cycle No. 2 ($\overline{E}$ Controlled)

DQ lines may transition to Low-Z if the falling edge of $\overline{W}$ occurs after the falling edge of $\overline{E}$.

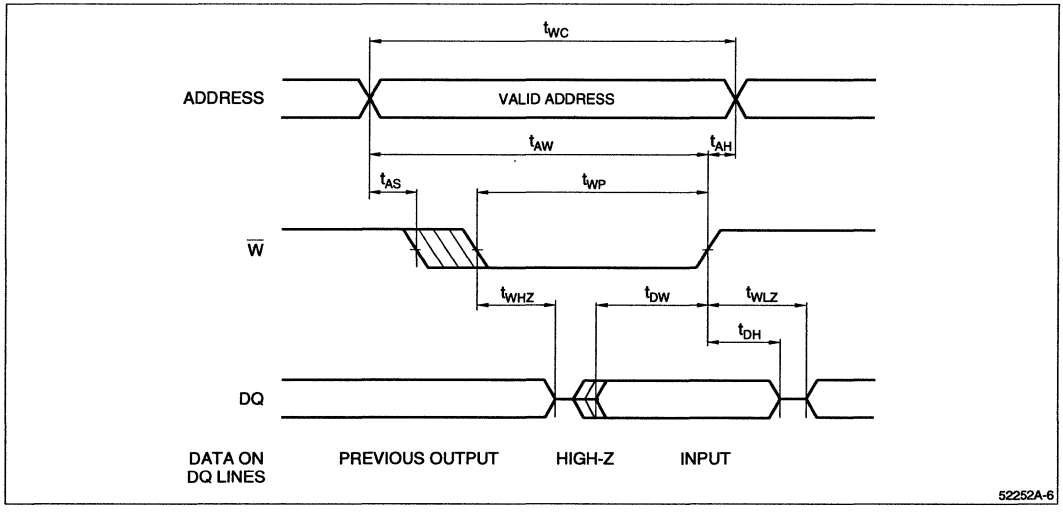


Figure 6. Write Cycle No. 1

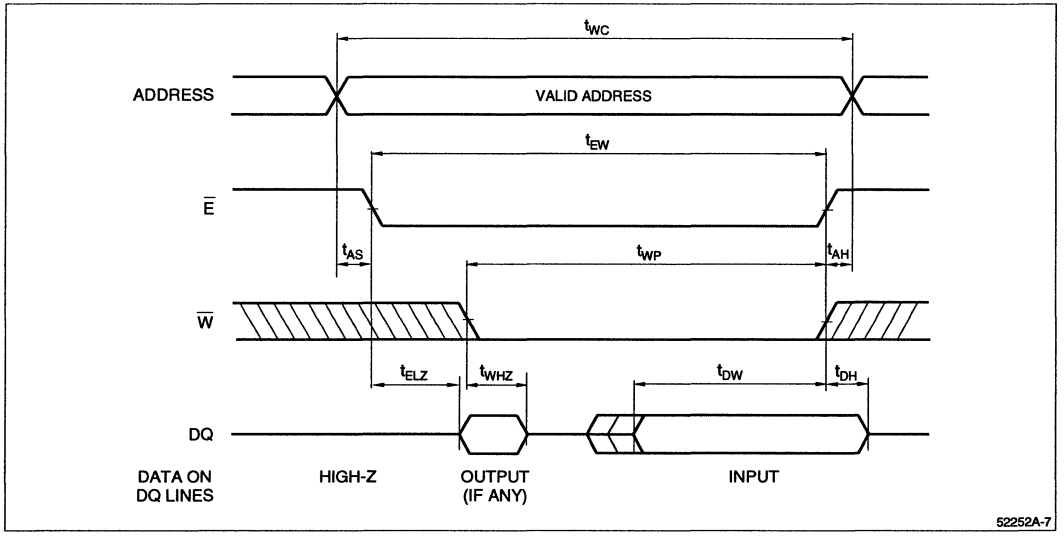
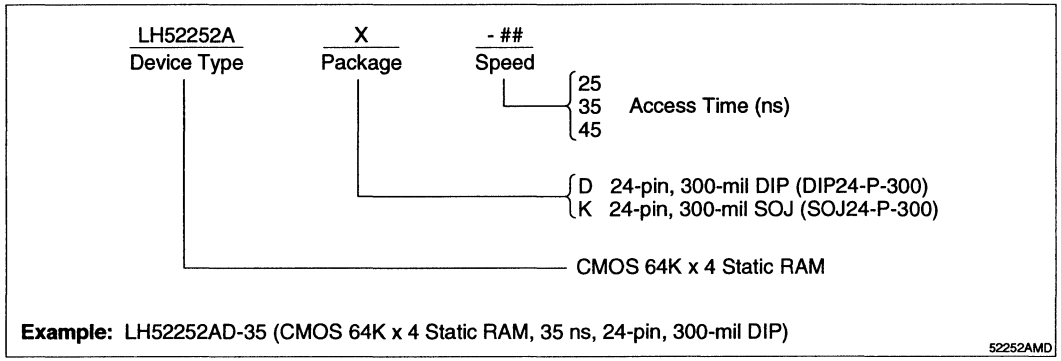


Figure 7. Write Cycle No. 2

ORDERING INFORMATION



LH52253

CMOS 64K × 4 Static RAM

FEATURES

- Fast Access Times: 20/25/35 ns
- Low-Power Standby when Deselected
- TTL Compatible I/O
- 5 V ± 10% Supply
- Fully-Static Operation
- Common I/O for Low Pin Count
- JEDEC Standard Pinouts
- Packages:
  28-Pin, 300-mil DIP
  28-Pin, 300-mil SOJ

FUNCTIONAL DESCRIPTION

The LH52253 is a very high-speed 256K-bit static RAM organized as 64K × 4. This RAM is fully static in operation. The Chip Enable ($\overline{E}$) reduces power to the chip when $\overline{E}$ is inactive (HIGH). The combination of $\overline{E}$ and $\overline{W}$ control the mode of operation of the LH52253.

Write cycles occur when both $\overline{E}$ and Write Enable ($\overline{W}$) are LOW. Data is transferred from the DQ pins to the memory location specified by the 16 address lines.

When $\overline{E}$ is LOW and $\overline{W}$ is HIGH, a static read of the memory location specified by the address lines will occur. Since the device is fully static in operation, new read cycles can be performed by simply changing the address. An Automatic Power Down feature reduces the current consumption when Read and Write cycles extend beyond their minimum cycle times.

The LH52253 offers an Output Enable ($\overline{G}$) for use in managing the Data Bus. Bus contention during Write cycles may be easily avoided by using the $\overline{G}$ input in the LH52253.

High-frequency design techniques should be employed to obtain the best performance from these devices. Solid, low-impedance power and ground planes, with high-frequency decoupling capacitors, are recommended. Series termination of the inputs should be considered when transmission line effects occur.

PIN CONNECTIONS

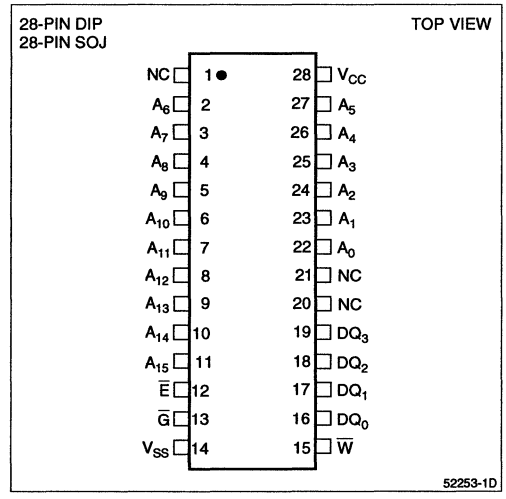


Figure 1. Pin Connections for DIP and SOJ Packages

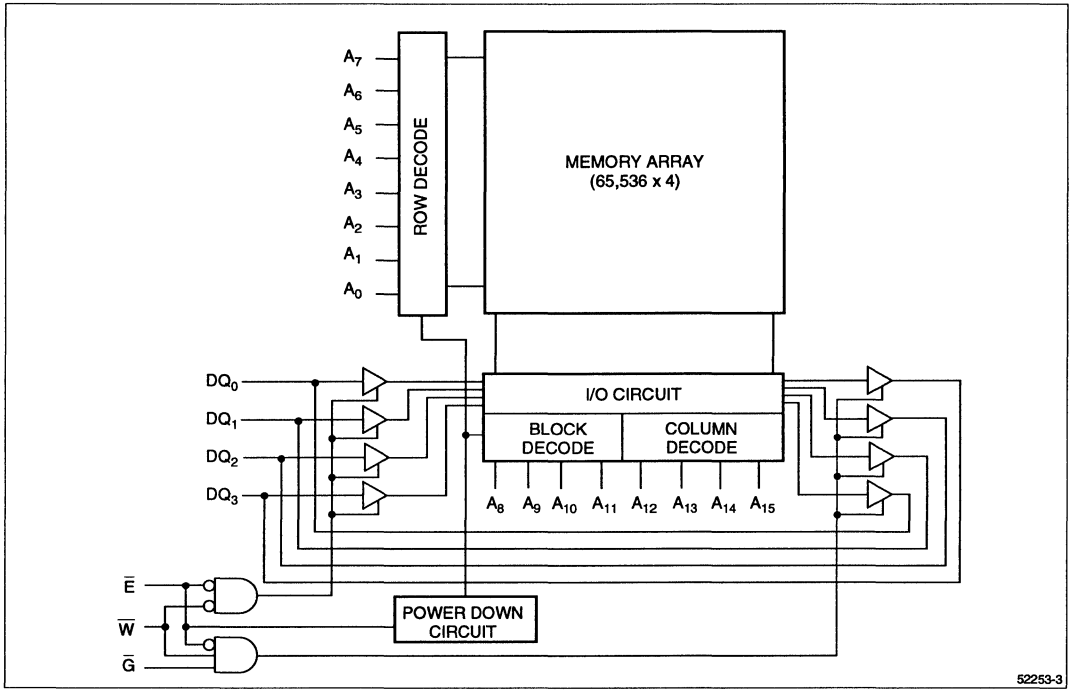


Figure 2. LH52253 Block Diagram

TRUTH TABLE

$\overline{E}$	$\overline{W}$	$\overline{G}$	MODE	DQ	Icc
H	X	X	Not Selected	High-Z	Standby
L	H	L	Read	Data Out	Active
L	H	H	Read	High-Z	Active
L	L	X	Write	Data In	Active

NOTE:
X = Don't Care, L = LOW, H = HIGH

PIN DESCRIPTIONS

PIN	DESCRIPTION
$A_0 - A_{15}$	Address Inputs
$DQ_0 - DQ_3$	Data Inputs/Outputs
$\overline{E}$	Chip Enable input
$\overline{W}$	Write Enable input
$\overline{G}$	Output Enable input
V_{CC}	Positive Power Supply
V_{SS}	Ground

ABSOLUTE MAXIMUM RATINGS [1]

PARAMETER	RATING
V_{CC} to V_{SS} Potential	−0.5 V to 7 V
Input Voltage Range	−0.5 V to V_{CC} + 0.5 V
DC Output Current [2]	± 40 mA
Storage Temperature Range	−65°C to 150°C
Power Dissipation (Package Limit)	1.0 W

NOTES:

1. Stresses greater than those listed under 'Absolute Maximum Ratings' may cause permanent damage to the device. This is a stress rating for transient conditions only. Function operation of the device at these or any other conditions above those indicated in the 'Operating Range' of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Outputs should not be shorted for more than 30 seconds. No more than one output should be shorted at any time.

OPERATING RANGES

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
T_A	Temperature, Ambient	0		70	°C
V_{CC}	Supply Voltage	4.5		5.5	V
V_{SS}	Supply Voltage	0		0	V
V_{IL}	Logic '0' Input Voltage [1]	−0.5		0.8	V
V_{IH}	Logic '1' Input Voltage	2.2		V_{CC} + 0.5	V

NOTE:

1. Negative undershoot of up to 3.0 V is permitted once per cycle.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP [1]	MAX	UNIT
I_{CC1}	Operating Current [2]	Outputs open, t_{CYCLE} = 20 ns $\overline{G}$ = V_{IH}, $\overline{CE}$ = V_{IL}, $\overline{WE}$ = V_{IL} or V_{IH}		70	145	mA
I_{CC1}	Operating Current [2]	Outputs open, t_{CYCLE} = 25 ns $\overline{G}$ = V_{IH}, $\overline{CE}$ = V_{IL}, $\overline{WE}$ = V_{IL} or V_{IH}		60	135	mA
I_{CC1}	Operating Current [2]	Outputs open, t_{RC} = 35 ns $\overline{G}$ = V_{IH}, $\overline{CE}$ = V_{IL}, $\overline{WE}$ = V_{IL} or V_{IH}		50	135	mA
I_{SB1}	Standby Current	$\overline{E} \geq V_{CC} - 0.2$ V		0.005	1	mA
I_{SB2}	Standby Current	$\overline{E} \geq V_{IH}$ min		5	10	mA
I_{LI}	Input Leakage Current	V_{CC} = 5.5 V, V_{IN} = 0 V to V_{CC}	−2		2	µA
I_{LO}	I/O Leakage Current	V_{CC} = 5.5 V, V_{IN} = 0 V to V_{CC}	−2		2	µA
V_{OH}	Output High Voltage	I_{OH} = −4.0 mA	2.4			V
V_{OL}	Output Low Voltage	I_{OL} = 8.0 mA			0.4	V

NOTES:

1. Typical values at V_{CC} = 5 V, T_A = 25°C.
2. I_{CC} is dependent upon output loading and cycle rates. Specified values are with outputs open, operating at specified cycle times.

AC TEST CONDITIONS

PARAMETER	RATING
Input Pulse Levels	V_{SS} to 3 V
Input Rise and Fall Times	5 ns
Input and Output Timing Ref. Levels	1.5 V
Output Load, Timing Tests	Figure 3

CAPACITANCE [1,2]

PARAMETER	RATING
C_{IN} (Input Capacitance)	8 pF
C_{DQ} (Input/Output Capacitance)	8 pF

NOTES:

1. Capacitances are maximum values at 25°C measured at 1.0 MHz with V_{Bias} = 0 V and V_{CC} = 5.0 V.
2. Guaranteed but not tested.

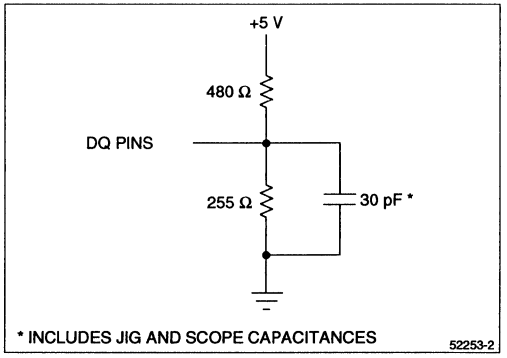


Figure 3. Output Load Circuit

AC ELECTRICAL CHARACTERISTICS [1] (Over Operating Range)

SYMBOL	DESCRIPTION	-20		-25		-35		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	
	READ CYCLE							
t_{RC}	Read Cycle Timing	20		25		35		ns
t_{AA}	Address Access Time		20		25		35	ns
t_{OH}	Output Hold From Address Change	3		3		3		ns
t_{EA}	$\overline{E}$ Low to Valid Data		20		25		35	ns
t_{ELZ}	$\overline{E}$ Low to Output Active [2,3]	4		4		4		ns
t_{EHZ}	$\overline{E}$ High to Output High-Z [2,3]		10		10		12	ns
t_{GA}	$\overline{G}$ Low to Valid Data		10		12		15	ns
t_{GLZ}	$\overline{G}$ Low to Output Active [2,3]	0		0		0		ns
t_{GHZ}	$\overline{G}$ High to Output High-Z [2,3]	0	9	0	10	0	12	ns
t_{PU}	$\overline{E}$ Low to Power Up Time [3]	0		0		0		ns
t_{PD}	$\overline{E}$ High to Power Down Time [3]		25		30		35	ns
	WRITE CYCLE							
t_{WC}	Write Cycle Time	20		25		35		ns
t_{EW}	$\overline{E}$ Low to End of Write	15		20		25		ns
t_{AW}	Address Valid to End of Write	15		20		25		ns
t_{AS}	Address Setup	0		0		0		ns
t_{AH}	Address Hold From End of Write	0		0		0		ns
t_{WP}	$\overline{W}$ Pulse Width	12		15		20		ns
t_{DW}	Input Data Setup Time	10		10		12		ns
t_{DH}	Input Data Hold Time	0		0		0		ns
t_{WLZ}	$\overline{W}$ High to Output Active [2,3]	4		4		4		ns
t_{WHZ}	$\overline{W}$ Low to Output High-Z [2,3]		7		8		10	ns

NOTES:

1. AC Electrical Characteristics specified at 'AC Test Conditions' levels.
2. Active output to High-Z and High-Z to output active tests specified for a ±500 mV transition from steady state levels into the test load. C_{LOAD} = 5 pF.
3. Guaranteed but not tested.

TIMING DIAGRAMS – READ CYCLE

Read Cycle No. 1

Chip is in Read Mode: $\overline{W}$ is HIGH, $\overline{E}$ and $\overline{G}$ are LOW. Read cycle timing is referenced from when all addresses are stable until the first address transition. Crosshatched portion of DQ implies that data lines are in the Low-Z state and the data may not be valid.

Read Cycle No. 2

Chip is in the Read Mode: $\overline{W}$ is HIGH. Timing illustrated for the case when addresses are valid when $\overline{E}$ goes LOW. Data Out is not specified to be valid until t_{EA}, but may become valid as soon as t_{ELZ}. Valid Data will be present following t_{GA} only if t_{EA} timing has been met.

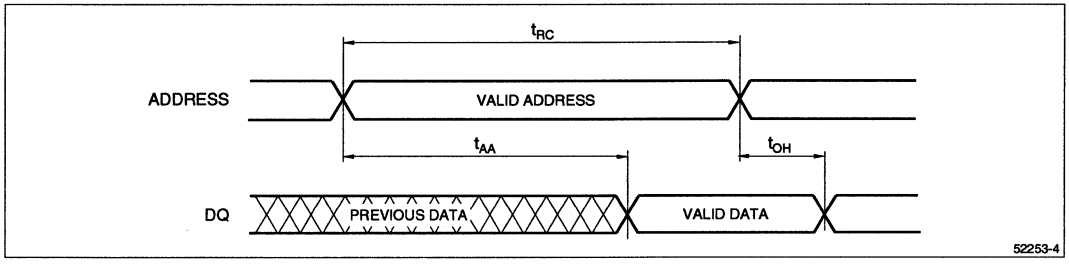


Figure 4. Read Cycle No. 1

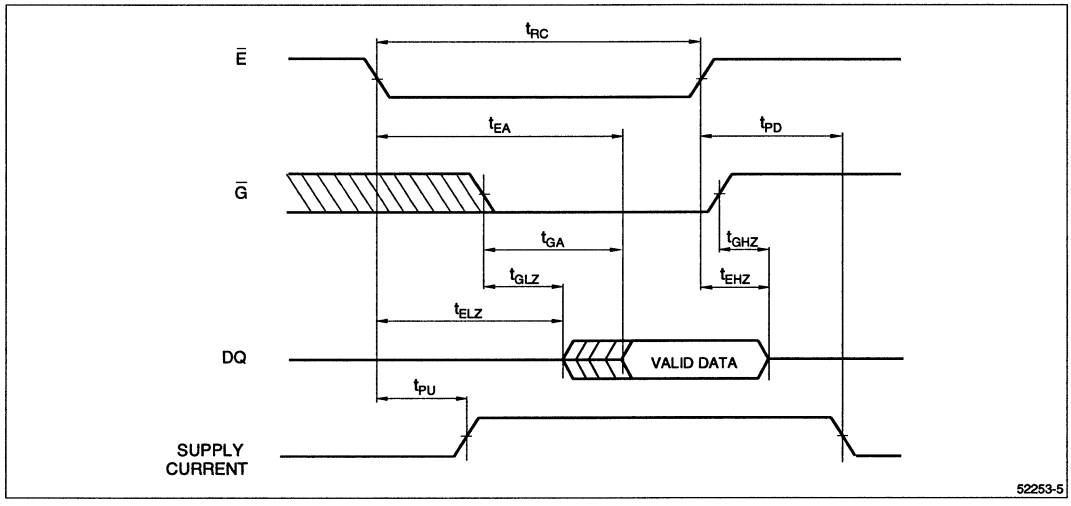


Figure 5. Read Cycle No. 2

TIMING DIAGRAMS – WRITE CYCLE

Addresses must be stable during Write cycles. $\overline{E}$ or $\overline{W}$ must be HIGH during address transitions. The outputs will remain in the High-Z state if $\overline{W}$ is LOW when $\overline{E}$ goes LOW. Care should be taken so that the output drivers are disabled prior to placing the Input Data on the DQ lines. This will prevent bus contention, reducing system noise. These timing diagrams assume $\overline{G}$ is LOW, but it should be kept HIGH during Write cycles to insure that the output drivers are disabled.

Write Cycle No. 1 ($\overline{W}$ Controlled)

Chip is selected: $\overline{E}$ and $\overline{G}$ are LOW. Using only $\overline{W}$ to control Write cycles may not offer the best device performance, since both t_{WHZ} and t_{DW} timing specifications must be met.

Write Cycle No. 2 ($\overline{E}$ Controlled)

DQ lines may transition to Low-Z if the falling edge of $\overline{W}$ occurs after the falling edge of $\overline{E}$.

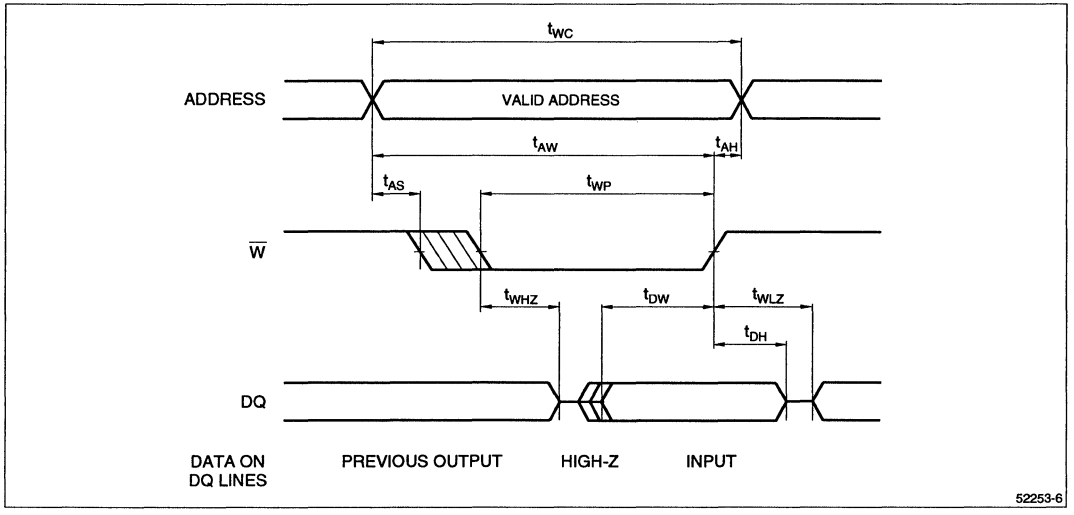


Figure 6. Write Cycle No. 1

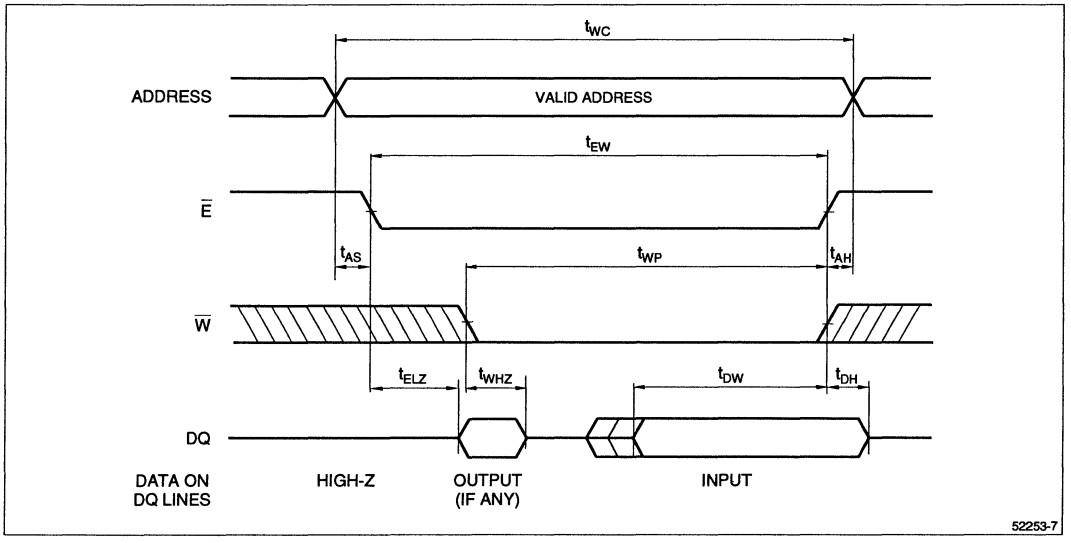
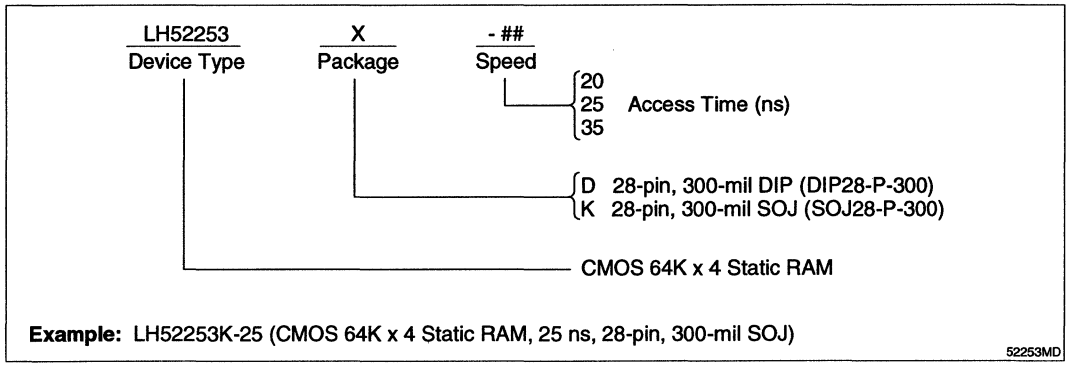


Figure 7. Write Cycle No. 2

ORDERING INFORMATION



Example: LH52253K-25 (CMOS 64K x 4 Static RAM, 25 ns, 28-pin, 300-mil SOJ)

52253MD

LH52258A

CMOS 32K × 8 Static RAM

FEATURES

- Fast Access Times: 20/25 ns
- Low-Power Standby when Deselected
- TTL Compatible I/O
- 5 V ± 10% Supply
- Fully-Static Operation
- JEDEC Standard Pinout
- Packages:
  28-Pin, 300-mil DIP
  28-Pin, 300-mil SOJ

FUNCTIONAL DESCRIPTION

The LH52258A is a high-speed 262,144 bit static RAM organized as 32K × 8. A fast, efficient design is obtained with a CMOS periphery and a matrix constructed with polysilicon load memory cells.

This RAM is fully static in operation. The Chip Enable ($\overline{E}$) control permits Read and Write operations when active (LOW) or places the RAM in a low-power standby mode when inactive (HIGH). Standby power (I_{SB1}) drops to its lowest level if $\overline{E}$ is raised to within 0.2 V of V_{CC}.

Write cycles occur when both Chip Enable ($\overline{E}$) and Write Enable ($\overline{W}$) are LOW. Data is transferred from the DQ pins to the memory location specified by the 15 address lines. The proper use of the Output Enable control ($\overline{G}$) can prevent bus contention.

When $\overline{E}$ is LOW and $\overline{W}$ is HIGH, a static Read will occur at the memory location specified by the address lines. $\overline{G}$ must be brought LOW to enable the outputs. Since the device is fully static in operation, new Read cycles can be performed by simply changing the address.

High-frequency design techniques should be employed to obtain the best performance from this device. Solid, low-impedance power and ground planes, with high-frequency decoupling capacitors, are recommended. Series termination of the inputs should be considered when transmission line effects occur.

PIN CONNECTIONS

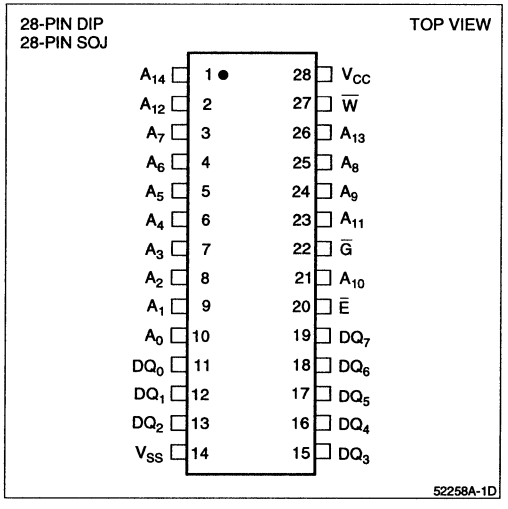


Figure 1. Pin Connections for DIP and SOJ Packages

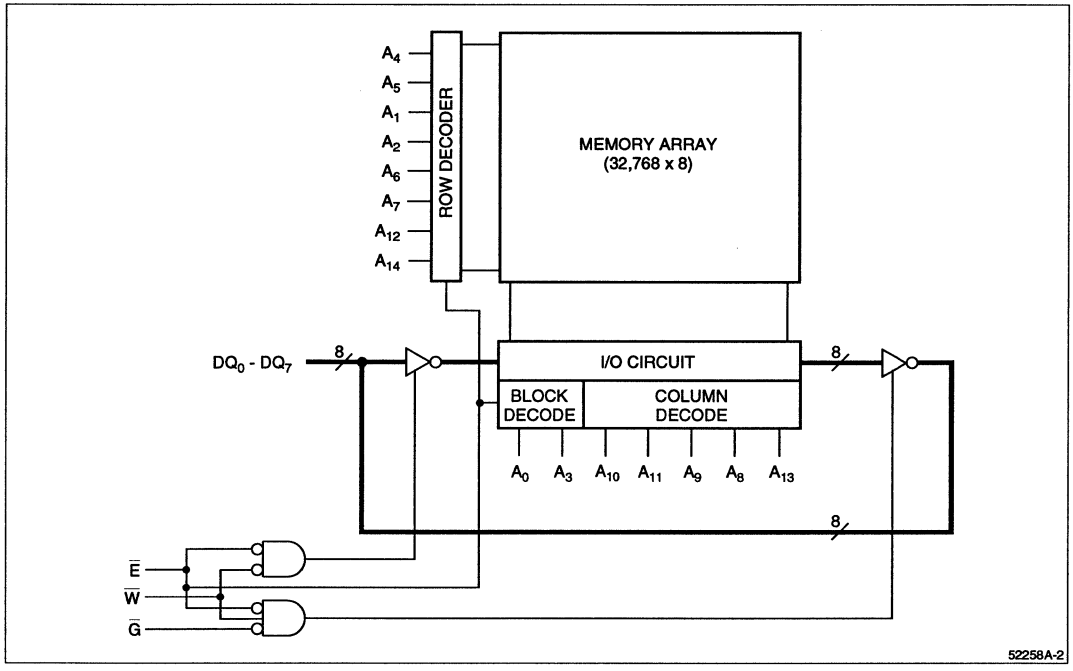


Figure 2. LH52258A Block Diagram

TRUTH TABLE

$\overline{E}$	$\overline{G}$	$\overline{W}$	MODE	DQ	Icc
H	X	X	Not Selected	High-Z	Standby
L	H	H	Selected	High-Z	Active
L	L	H	Read	Data Out	Active
L	X	L	Write	Data In	Active

PIN DESCRIPTIONS

PIN	DESCRIPTION
$A_0 - A_{14}$	Address Inputs
$DQ_0 - DQ_7$	Data Inputs/Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
V_{CC}	Positive Power Supply
V_{SS}	Ground

ABSOLUTE MAXIMUM RATINGS [1]

PARAMETER	RATING
V_{CC} to V_{SS} Potential	−0.5 V to 7 V
Input Voltage Range	−0.5 V to V_{CC} + 0.5 V
DC Output Current [2]	± 40 mA
Storage Temperature Range	−65° to 150°C
Power Dissipation (Package Limit)	1.0 W

NOTES:

1. Stresses greater than those listed under 'Absolute Maximum Ratings' may cause permanent damage to the device. This is a stress rating for transient conditions only. Functional operation of the device at these or any other conditions above those indicated in the 'Operating Range' section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Outputs should not be shorted for more than 30 seconds. No more than one output should be shorted at any time.

OPERATING RANGES

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
T_A	Temperature, Ambient	0		70	°C
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
V_{SS}	Supply Voltage	0	0	0	V
V_{IL}	Logic '0' Input Voltage [1]	−0.5		0.8	V
V_{IH}	Logic '1' Input Voltage	2.2		V_{CC} + 0.5	V

NOTE:

1. Negative undershoot of up to 3.0 V is permitted once per cycle.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP [1]	MAX	UNIT
I_{CC1}	Operating Current [2]	t_{RC} = 20 ns $\overline{G} \geq V_{IH}$, $\overline{E} \leq V_{IL}$, I_{OUT} = 0 mA, t_{CYCLE} = 20 ns		95	150	mA
I_{CC1}	Operating Current [2]	t_{RC} = 25 ns $\overline{G} \geq V_{IH}$, $\overline{E} \leq V_{IL}$, I_{OUT} = 0 mA, t_{CYCLE} = 25 ns		90	140	mA
I_{SB1}	Standby Current	$\overline{E} \geq V_{CC}$ − 0.2 V		0.005	1	mA
I_{SB2}	Standby Current	$\overline{E} \geq V_{IH}$		6	15	mA
I_{LI}	Input Leakage Current	V_{CC} = 5.5 V, V_{IN} = 0 V to V_{CC}	−2		2	µA
I_{LO}	I/O Leakage Current	V_{CC} = 5.5 V, V_{IN} = 0 V to V_{CC}	−2		2	µA
V_{OH}	Output High Voltage	I_{OH} = −4.0 mA	2.4			V
V_{OL}	Output Low Voltage	I_{OL} = 8.0 m A			0.4	V
V_{DR}	Data Retention Voltage	$\overline{E} \geq V_{CC}$ − 0.2 V	2		5.5	V
I_{DR}	Data Retention Current	V_{CC} = 3 V, $\overline{E} \geq V_{CC}$ − 0.2 V			250	µA

NOTES:

1. Typical values at V_{CC} = 5 V, T_A = 25°C.
2. I_{CC} is dependent upon output loading and cycle rates. Specified values are with outputs open, operating at specified cycle times.

AC TEST CONDITIONS

PARAMETER	RATING
Input Pulse Levels	V_{SS} to 3 V
Input Rise and Fall Times	3 ns
Input and Output Timing Ref. Levels	1.5 V
Output Load, Timing Tests	Figure 3

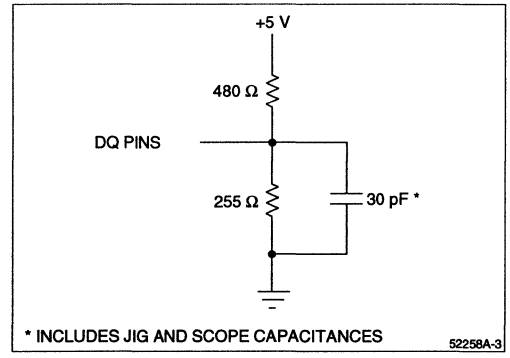


Figure 3. Output Load Circuit

CAPACITANCE [1,2]

PARAMETER	RATING
C_{IN} (Input Capacitance)	7 pF
C_{DQ} (I/O Capacitance)	8 pF

NOTES:

1. Capacitances are maximum values at 25°C measured at 1.0 MHz with V_{Bias} = 0 V and V_{CC} = 5.0 V.
2. Guaranteed but not tested.

DATA RETENTION TIMING

$\overline{E}$ must be held above the lesser of V_{IH} or V_{CC} – 0.2 V to prevent improper operation when V_{CC} < 4.5 V. $\overline{E}$ must be V_{CC} – 0.2 V or greater to meet I_{DR} specification. All other inputs are 'Don't Care.'

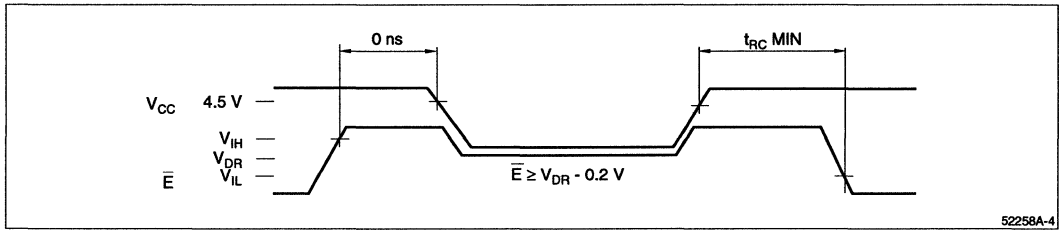


Figure 4. Data Retention Timing

AC ELECTRICAL CHARACTERISTICS [1] (Over Operating Range)

SYMBOL	DESCRIPTION	-20		-25		UNITS
		MIN	MAX	MIN	MAX	
	READ CYCLE					
t_{RC}	Read Cycle Time	20		25		ns
t_{AA}	Address Access Time		20		25	ns
t_{OH}	Output Hold from Address Change	4		4		ns
t_{EA}	$\overline{E}$ Low to Valid Data		20		25	ns
t_{ELZ}	$\overline{E}$ Low to Output Active [2,3]	4		4		ns
t_{EHZ}	$\overline{E}$ High to Output High-Z [2,3]	0	10	0	12	ns
t_{GA}	$\overline{G}$ Low to Valid Data		10		12	ns
t_{GLZ}	$\overline{G}$ Low to Output Active [2,3]	0		0		ns
t_{GHZ}	$\overline{G}$ High to Output High-Z [2,3]	0	9	0	10	ns
t_{PU}	$\overline{E}$ Low to Power Up Time [3]	0		0		ns
t_{PD}	$\overline{E}$ High to Power Down Time [3]		25		30	ns
	WRITE CYCLE					
t_{WC}	Write Cycle Time	20		25		ns
t_{EW}	$\overline{E}$ Low to End of Write	15		20		ns
t_{AW}	Address Valid to End of Write	15		20		ns
t_{AS}	Address Setup	0		0		ns
t_{AH}	Address Hold from End of Write	0		0		ns
t_{WP}	$\overline{W}$ Pulse Width	12		15		ns
t_{DW}	Input Data Setup Time	10		12		ns
t_{DH}	Input Data Hold Time	0		0		ns
t_{WHZ}	$\overline{W}$ Low to Output High-Z [2,3]		8		10	ns
t_{WLZ}	$\overline{W}$ High to Output Active [2,3]	0		0		ns

NOTES:

1. AC Electrical Characteristics specified at 'AC Test Conditions' levels.
2. Active output to High-Z and High-Z to output active tests specified for a ±500 mV transition from steady state levels into the test load. The test load has 5 pF capacitances.
3. Guaranteed by design but not tested.

TIMING DIAGRAMS – READ CYCLE

Read Cycle No. 1

Chip is in Read Mode: $\overline{W}$ is HIGH, $\overline{E}$ is LOW and $\overline{G}$ is LOW. Read cycle timing is referenced from when all addresses are stable until the first address transition. Crosshatched portion of Data Out implies that data lines are in the Low-Z state but the data is not guaranteed to be valid until t_{AA}.

Read Cycle No. 2

Chip is in Read Mode: $\overline{W}$ is HIGH. Timing illustrated for the case when addresses are valid before $\overline{E}$ goes LOW. Data Out is not specified to be valid until t_{EA} or t_{GA}, but may become valid as soon as t_{ELZ} or t_{GLZ}. Outputs will transition from High-Z to Valid Data Out. Valid data will be present following t_{GA} only if t_{EA} timing is met.

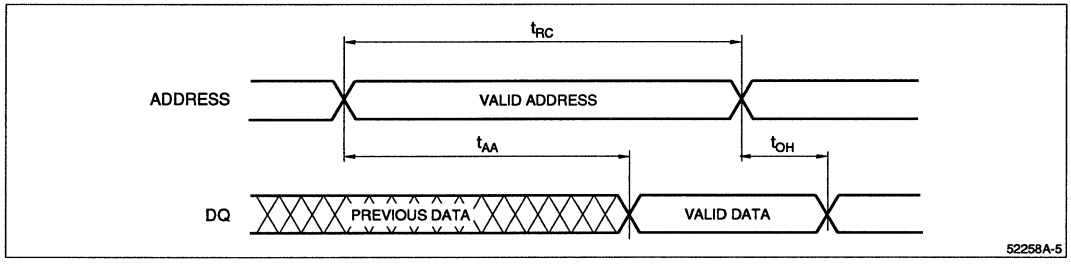


Figure 5. Read Cycle No. 1

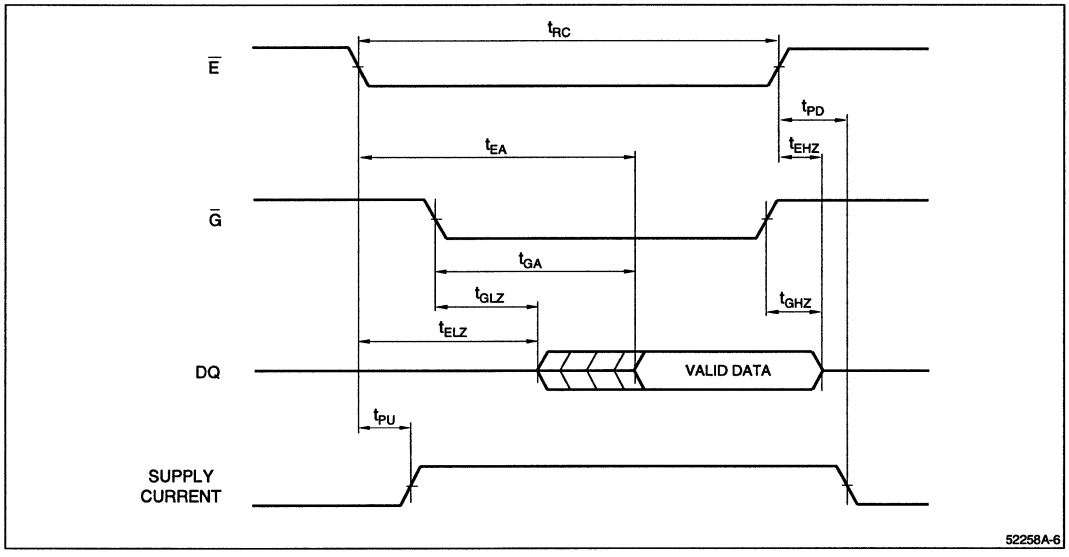


Figure 6. Read Cycle No. 2

TIMING DIAGRAMS – WRITE CYCLE

Addresses must be stable during Write cycles. The outputs will remain in the High-Z state if $\overline{W}$ is LOW when $\overline{E}$ goes LOW. If $\overline{G}$ is HIGH, the outputs will remain in the High-Z state. Although these examples illustrate timing with $\overline{G}$ active, it is recommended that $\overline{G}$ be held HIGH for all Write cycles. This will prevent the LH52258A's outputs from becoming active, preventing bus contention, thereby reducing system noise.

Write Cycle No. 1 ($\overline{W}$ Controlled)

Chip is selected: $\overline{E}$ is LOW, $\overline{G}$ is LOW. Using only $\overline{W}$ to control Write cycles may not offer the best performance since both t_{WHZ} and t_{DW} timing specifications must be met.

Write Cycle No. 2 ($\overline{E}$ Controlled)

$\overline{G}$ is LOW. DQ lines may transition to Low-Z if the falling edge of $\overline{W}$ occurs after the falling edge of $\overline{E}$.

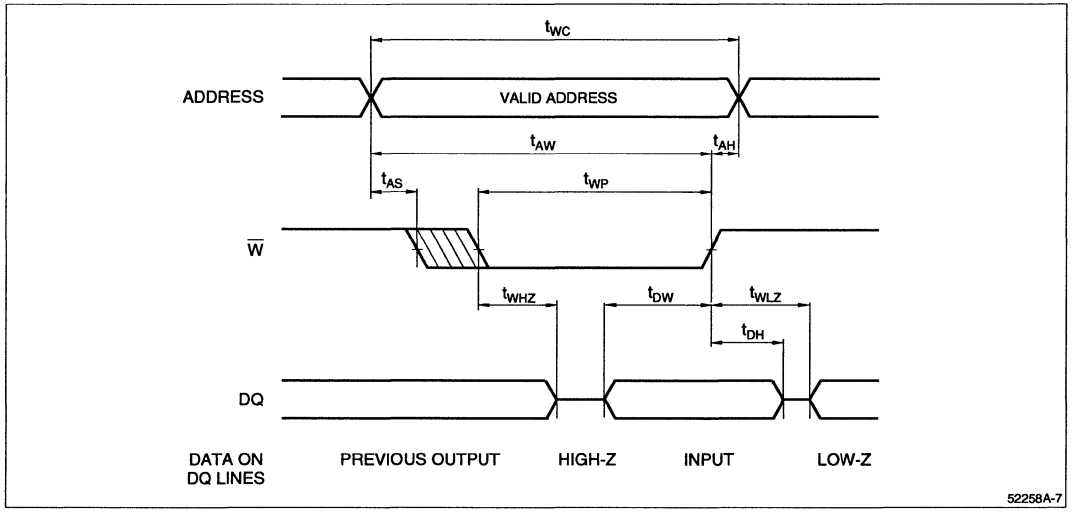


Figure 7. Write Cycle No. 1

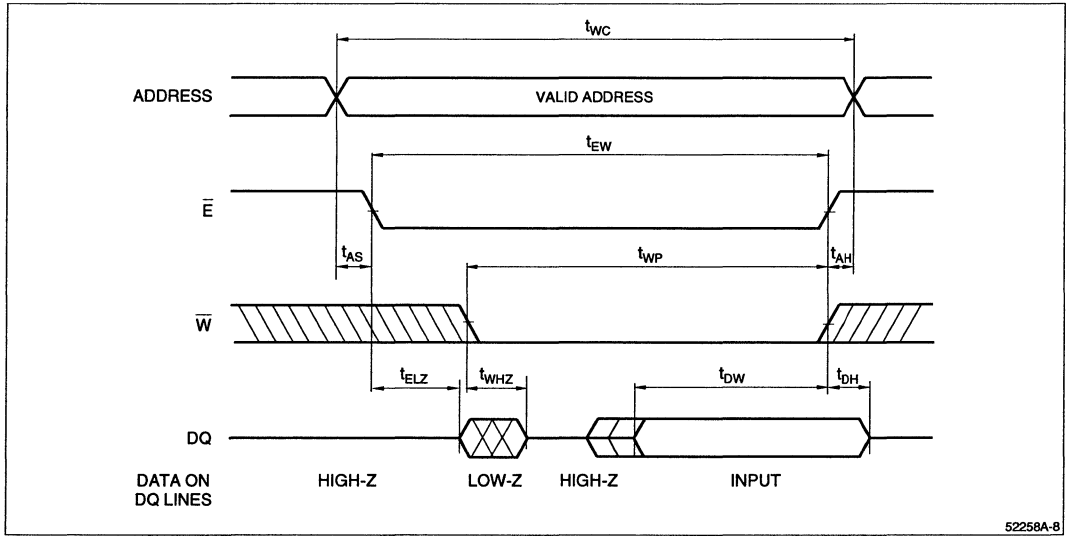
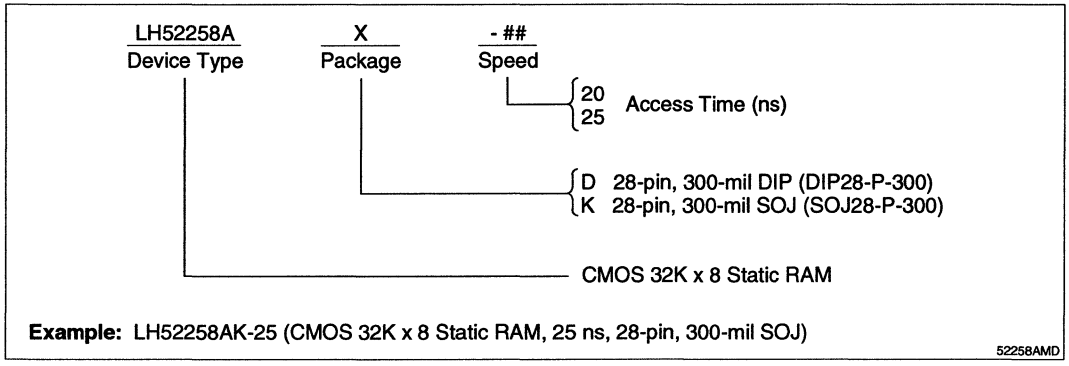


Figure 8. Write Cycle No. 2

ORDERING INFORMATION



LH521002

CMOS 256K × 4 Static RAM

FEATURES

- Fast Access Times: 20/25/35 ns
- JEDEC Standard Pinouts
- Low Power Standby when Deselected
- TTL Compatible I/O
- 5 V ±10% Supply
- Fully Static Operation
- Common I/O for Low Pin Count
- Package: 28-Pin, 400-mil SOJ

FUNCTIONAL DESCRIPTION

The LH521002 is a high-speed 1M-bit static RAM organized as 256K × 4. A fast, efficient design is obtained with a CMOS periphery and a matrix constructed with polysilicon load memory cells.

This RAM is fully static in operation. The Chip Enable ($\overline{E}$) reduces power to the chip when $\overline{E}$ is HIGH. Standby power drops to its lowest level (I_{SB1}) when $\overline{E}$ is raised to within 0.2 V of V_{CC}.

Write cycles occur when both ($\overline{E}$) and Write Enable ($\overline{W}$) are LOW. Data is transferred from the DQ pins to the memory location specified by the 18 address lines.

Read cycles occur when $\overline{E}$ is LOW and $\overline{W}$ is HIGH. A Read cycle will begin upon an address transition, on a falling edge of $\overline{E}$, or on a rising edge of $\overline{W}$.

High-frequency design techniques should be employed to obtain the best performance from this device. Solid, low-impedance power and ground planes, with high-frequency decoupling capacitors, are desirable. Series termination of the inputs should be considered when transmission line effects occur.

PIN CONNECTIONS

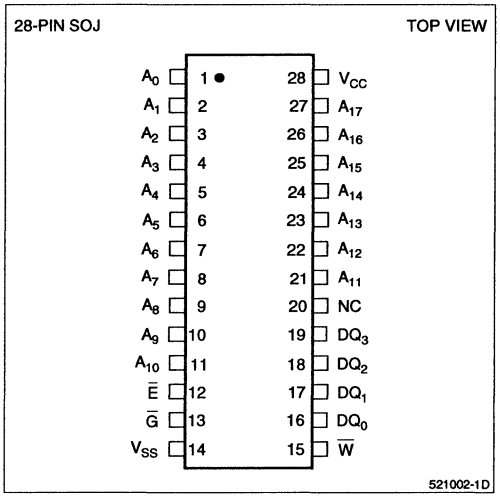


Figure 1. Pin Connections for SOJ Package

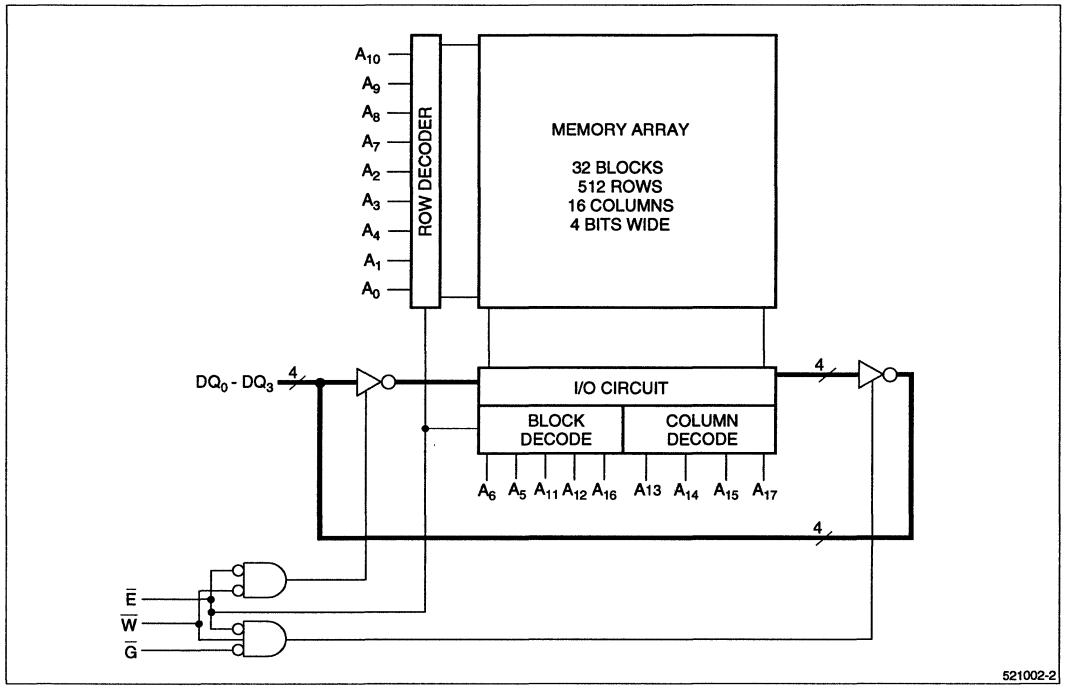


Figure 2. LH521002 Block Diagram

TRUTH TABLE

$\overline{E}$	$\overline{G}$	$\overline{W}$	MODE	DQ	Icc
H	X	X	Standby	High-Z	Standby
L	H	H	Selected	High-Z	Active
L	L	H	Read	Data Out	Active
L	X	L	Write	Data In	Active

PIN DESCRIPTIONS

PIN	DESCRIPTION
$A_0 - A_{17}$	Address Inputs
$DQ_0 - DQ_3$	Data Inputs/Outputs
$\overline{E}$	Chip Enable
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
V_{CC}	Positive Power Supply
V_{SS}	Ground

ABSOLUTE MAXIMUM RATINGS [1]

PARAMETER	RATING
V_{CC} to V_{SS} Potential	−0.5 V to 7 V
Input Voltage Range	−0.5 V to V_{CC} + 0.5 V
DC Output Current [2]	± 40 mA
Storage Temperature Range	−65°C to 150°C
Power Dissipation (Package Limit)	1.0 W

NOTES:

1. Stresses greater than those listed under 'Absolute Maximum Ratings' may cause permanent damage to the device. This is a stress rating for transient conditions only. Functional operation of the device at these or any other conditions above those indicated in the 'Operating Range' of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Outputs should not be shorted for more than 30 seconds. No more than one output should be shorted at any time.

OPERATING RANGES

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
T_A	Temperature, Ambient	0		70	°C
V_{CC}	Supply Voltage	4.5		5.5	V
V_{SS}	Supply Voltage	0		0	V
V_{IL}	Logic '0' Input Voltage [1]	−0.5		0.8	V
V_{IH}	Logic '1' Input Voltage	2.2		V_{CC} + 0.5	V

NOTE:

1. Outputs should not be shorted for more than 30 seconds. No more than one output should be shorted at any time.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC1}	Operating Current [1]	t_{CYCLE} = 20 ns $\overline{E}$ = V_{IL}, $\overline{W}$ = V_{IL} or V_{IH}			180	mA
I_{CC1}	Operating Current [1]	t_{CYCLE} = 25 ns $\overline{E}$ = V_{IL}, $\overline{W}$ = V_{IL} or V_{IH}			180	mA
I_{CC1}	Operating Current [1]	t_{CYCLE} = 35 ns $\overline{E}$ = V_{IL}, $\overline{W}$ = V_{IL} or V_{IH}			150	mA
I_{SB1}	Standby Current	$\overline{E} \geq V_{CC} - 0.2$ V		0.4	2	mA
I_{SB2}	Standby Current	$\overline{E} \geq V_{IH}$			20	mA
I_{LI}	Input Leakage Current	V_{IN} = 0 V to V_{CC}	−2		2	µA
I_{LO}	I/O Leakage Current	V_{IN} = 0 V to V_{CC}	−2		2	µA
V_{OH}	Output High Voltage	I_{OH} = −4.0 mA	2.4			V
V_{OL}	Output Low Voltage	I_{OL} = 8.0 mA			0.4	V
V_{DR}	Data Retention Voltage	$\overline{E} \geq V_{CC} - 0.2$ V	2		5.5	V
I_{DR}	Data Retention Current	V_{CC} = 3 V, $\overline{E} \geq V_{CC} - 0.2$ V			500	µA

NOTE:

1. I_{CC} is dependent upon output loading and cycle rates. Specified values are with outputs open.

AC TEST CONDITIONS

PARAMETER	RATING
Input Pulse Levels	V_{SS} to 3 V
Input Rise and Fall Times	5 ns
Input and Output Timing Ref. Levels	1.5 V
Output Load, Timing Tests	Figure 3

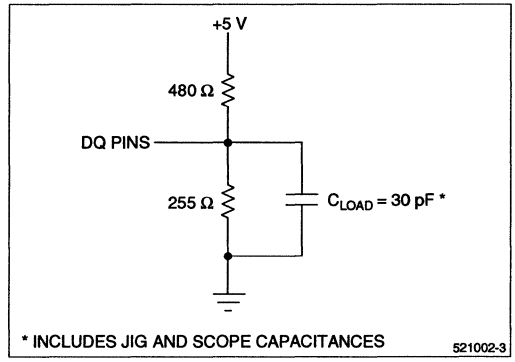


Figure 3. Output Load Circuit

CAPACITANCE [1,2]

PARAMETER	RATING
C_{IN} (Input Capacitance)	6 pF
C_{DQ} (I/O Capacitance)	8 pF

NOTES:

1. Capacitances are maximum values at 25°C measured at 1.0 MHz with V_{Bias} = 0 V and V_{CC} = 5.0 V.
2. This parameter is sampled and not production tested.

DATA RETENTION TIMING

$\overline{E}$ must be held above the lesser of V_{IH} or V_{CC} – 0.2 V to prevent improper operation when V_{CC} < 4.5 V. $\overline{E}$ must be V_{CC} – 0.2 V or greater to meet I_{DR} specification. All other inputs are 'Don't Care.'

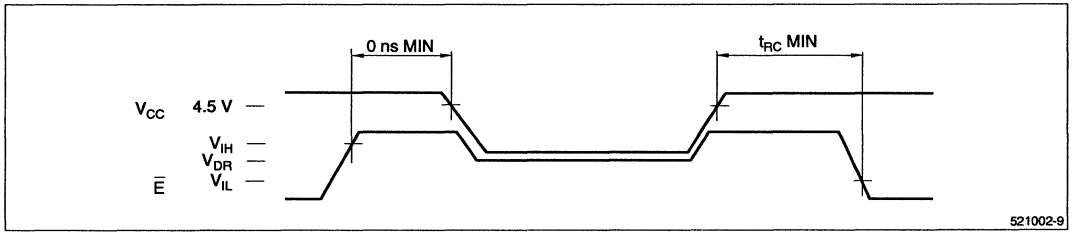


Figure 4. Data Retention Timing

AC ELECTRICAL CHARACTERISTICS [6] (Over Operating Range)

SYMBOL	DESCRIPTION	-20		-25		-35		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	
READ CYCLE								
t_{RC}	Read Cycle Timing	20		25		35		ns
t_{AA}	Address Access Time		20		25		35	ns
t_{OH}	Output Hold from Address Change	3		3		3		ns
t_{EA}	$\overline{E}$ Low to Valid Data		20		25		35	ns
t_{ELZ}	$\overline{E}$ Low to Output Active [7,8]	3		3		3		ns
t_{EHZ}	$\overline{E}$ High to Output High-Z [7,8]		10		12		20	ns
t_{GA}	$\overline{G}$ Low to Valid Data		8		10		20	ns
t_{GLZ}	$\overline{G}$ Low to Output Active [7,8]	0		0		0		ns
t_{GHZ}	$\overline{G}$ High to Output High-Z [7,8]		8		10		20	ns
t_{PU}	$\overline{E}$ Low to Power Up Time [8]	0		0		0		ns
t_{PD}	$\overline{E}$ High to Power Down Time [8]		20		25		35	ns
WRITE CYCLE								
t_{WC}	Write Cycle Time	20		25		35		ns
t_{EW}	$\overline{E}$ Low to End of Write	15		20		30		ns
t_{AW}	Address Valid to End of Write	15		20		30		ns
t_{AS}	Address Setup	0		0		0		ns
t_{AH}	Address Hold From End of Write	0		0		0		ns
t_{WP}	$\overline{W}$ Pulse Width	15		20		25		ns
t_{DW}	Input Data Setup Time	12		15		15		ns
t_{DH}	Input Data Hold Time	0		0		0		
t_{WHZ}	$\overline{W}$ Low to Output High-Z [7,8]		8		10		15	ns
t_{WLZ}	$\overline{W}$ High to Output Active [7,8]	3		3		3		ns

NOTES:

1. AC Electrical Characteristics specified at 'AC Test Conditions' levels.
2. Active output to High-Z and High-Z to output active tests specified for a ±500 mV transition from steady state levels into the test load. C_{Load} = 5 pF.
3. This parameter is sampled and not production tested.

TIMING DIAGRAMS – READ CYCLE

Read Cycle No. 1

Chip is in Read Mode: $\overline{W}$ is HIGH, $\overline{E}$ and $\overline{G}$ are LOW. Read cycle timing is referenced from when all addresses are stable until the first address transition. Following an Address transition, Data Out is guaranteed valid at t_{AA}.

Read Cycle No. 2

Chip is in Read Mode: $\overline{W}$ is HIGH. Timing illustrated for the case when addresses are valid while $\overline{E}$ goes LOW. Data Out is not specified to be valid until t_{EA}, but may become valid as soon as t_{ELZ}. Outputs will transition from High-Z to Valid Data Out. Data Out is valid after both t_{EA} and t_{GA} are met.

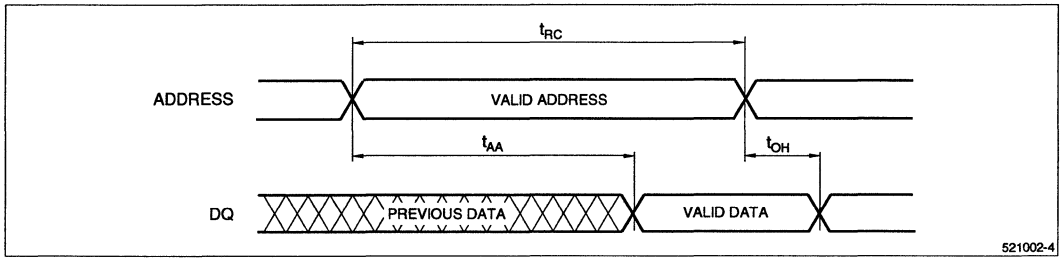


Figure 5. Read Cycle No. 1

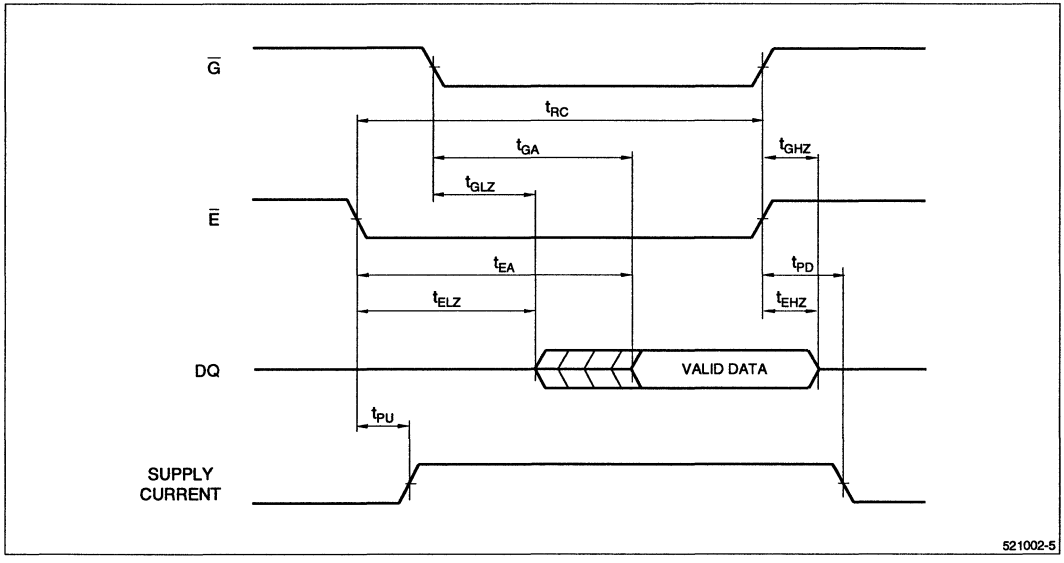


Figure 6. Read Cycle No. 2

TIMING DIAGRAMS – WRITE CYCLE

Addresses must be stable during Write cycles. $\overline{E}$ or $\overline{W}$ must be HIGH during address transitions. The outputs will remain in the High-Z state if $\overline{W}$ is LOW when $\overline{E}$ goes LOW. Care should be taken so that the output drivers are disabled prior to placing the Input Data on the DQ lines. This will prevent bus contention, reducing system noise.

Write Cycle No. 1 ($\overline{W}$ Controlled)

Chip is selected: $\overline{E}$ and $\overline{G}$ are LOW. Using only $\overline{W}$ to control Write cycles may not offer the best device performance, since both t_{WHZ} and t_{DW} timing specifications must be met.

Write Cycle No. 2 ($\overline{E}$ Controlled)

$\overline{G}$ is LOW. DQ lines may transition to Low-Z if the falling edge of $\overline{W}$ occurs after the falling edge of $\overline{E}$.

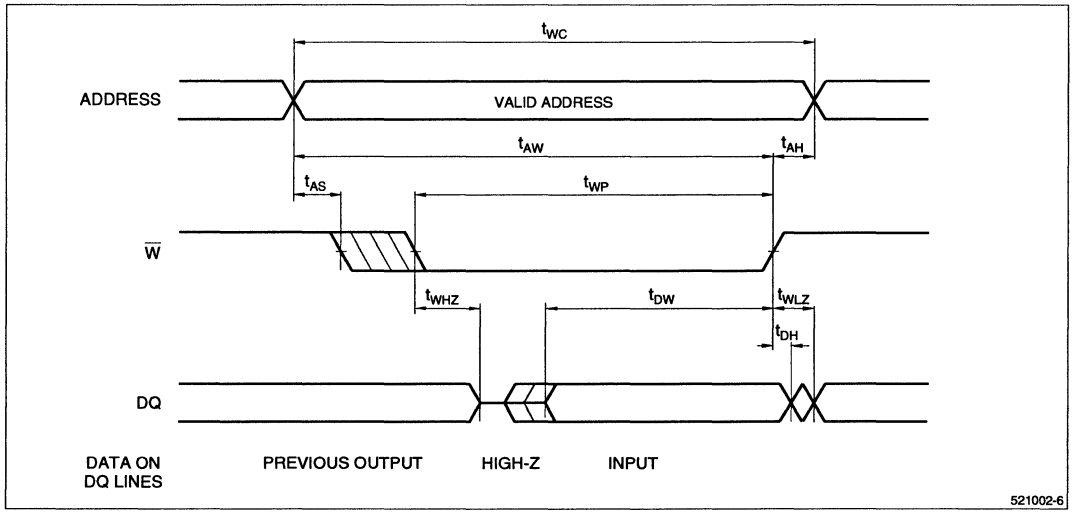


Figure 7. Write Cycle No. 1

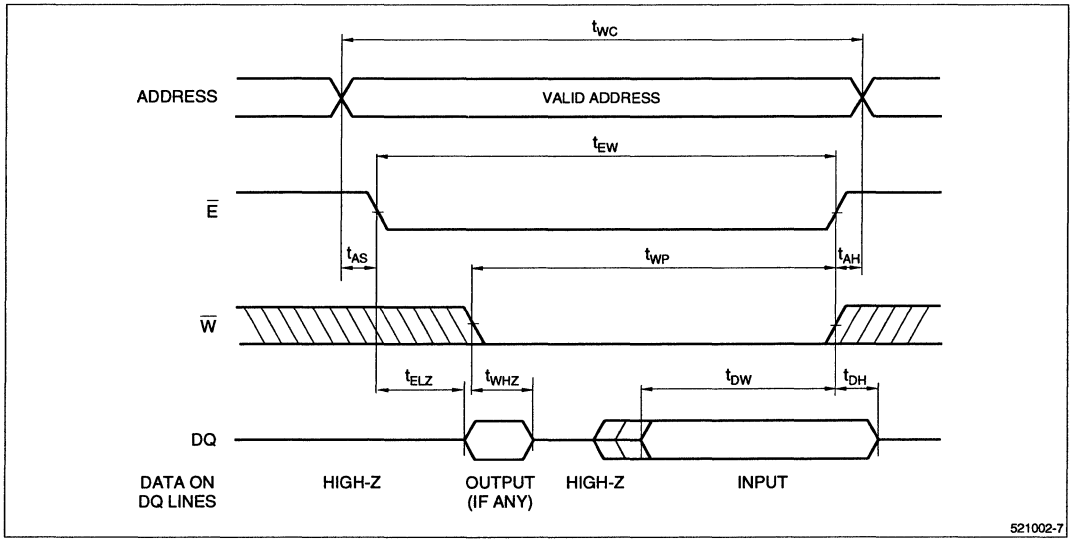
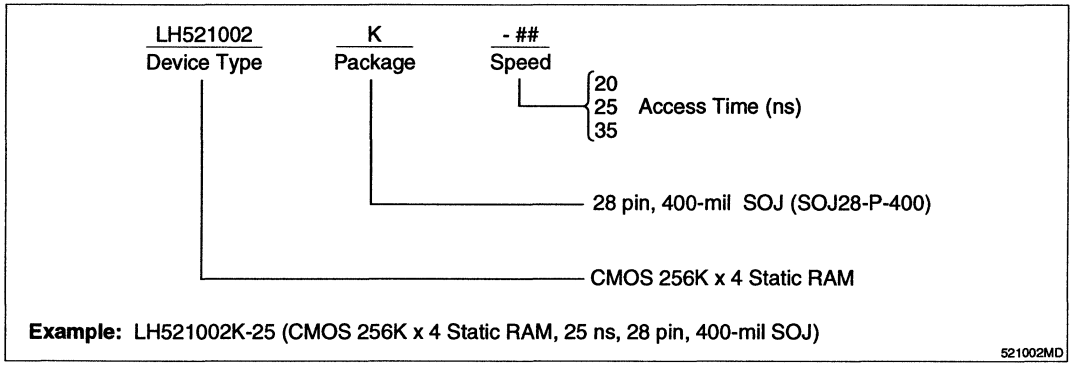


Figure 8. Write Cycle No. 2

ORDERING INFORMATION



Example: LH521002K-25 (CMOS 256K x 4 Static RAM, 25 ns, 28 pin, 400-mil SOJ)

521002MD

LH521007A

CMOS 128K × 8 Static RAM

FEATURES

- Fast Access Times: 20/25/35 ns
- Two Chip Enable Controls
- Low-Power Standby When Deselected
- TTL Compatible I/O
- 5 V ±10% Supply
- Fully-Static Operation
- 2 V Data Retention
- Package: 32-Pin, 400-mil SOJ

FUNCTIONAL DESCRIPTION

The LH521007A is a high-speed 1,048,576-bit static RAM organized as 128K × 8. A fast, efficient design is obtained with a CMOS periphery and a matrix constructed with polysilicon load memory cells.

This RAM is fully static in operation. The Chip Enables ($\overline{E}_1$, E_2) permit Read and Write operations when active ($\overline{E}_1$ = LOW and E_2 = HIGH) or place the RAM in a low-power standby mode when inactive ($\overline{E}_1$ = HIGH or E_2 = LOW). Standby power drops to its lowest level when all inputs are stable and are at CMOS levels, while the chip is in standby mode.

Write cycles occur when both Chip Enables and Write Enable are active. Data is transferred from the DQ pins to the memory location specified by the 17 address lines. The proper use of the Output Enable control ($\overline{G}$) can prevent bus contention.

When both Chip Enables are active and $\overline{W}$ is inactive, a static Read will occur at the memory location specified by the address lines. $\overline{G}$ must be brought LOW to enable the outputs. Since the device is fully static in operation, new Read cycles can be performed by simply changing the address.

High-frequency design techniques should be employed to obtain the best performance from this device. Solid, low-impedance power and ground planes, with high-frequency decoupling capacitors, are recommended. Series termination of the inputs should be considered when transmission line effects occur.

PIN CONNECTIONS

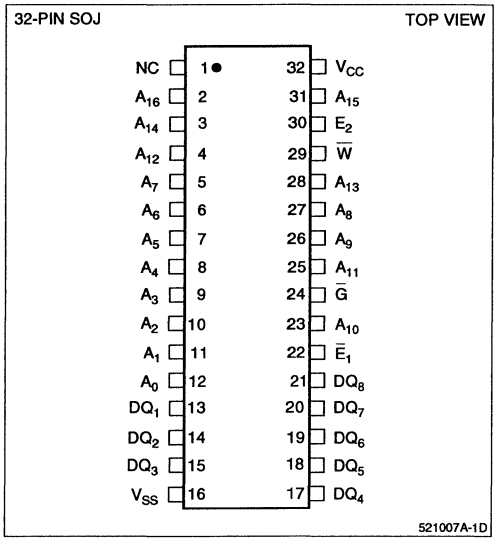


Figure 1. Pin Connections for SOJ Package

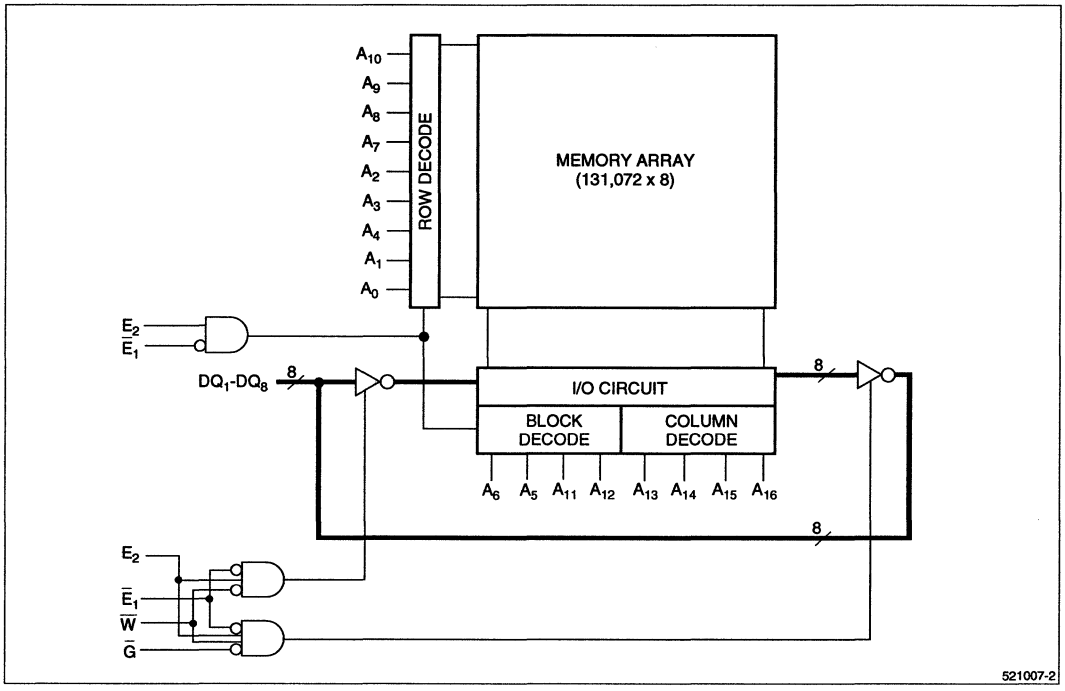


Figure 2. LH521007A Block Diagram

TRUTH TABLE

$\overline{E}_1$	E_2	$\overline{G}$	$\overline{W}$	MODE	DQ	I_{CC}
H	X	X	X	Standby	High-Z	Standby
X	L	X	X	Standby	High-Z	Standby
L	H	H	H	Read	High-Z	Active
L	H	L	H	Read	Data Out	Active
L	H	X	L	Write	Data In	Active

NOTE:
X = Don't Care, L = LOW, H = HIGH

PIN DESCRIPTIONS

PIN	DESCRIPTION
$A_0 - A_{16}$	Address Inputs
$DQ_1 - DQ_8$	Data Inputs/Outputs
$\overline{E}_1$, E_2	Chip Enable input
$\overline{G}$	Output Enable input
$\overline{W}$	Write Enable input
V_{CC}	Positive Power Supply
V_{SS}	Ground

ABSOLUTE MAXIMUM RATINGS [1]

PARAMETER	RATING
V_{CC} to V_{SS} Potential	−0.5 V to 7 V
Input Voltage Range	−0.5 V to V_{CC} + 0.5 V
DC Output Current [2]	± 40 mA
Storage Temperature Range	−65°C to 150°C
Power Dissipation (Package Limit)	1.0 W

NOTES:

1. Stresses greater than those listed under 'Absolute Maximum Ratings' may cause permanent damage to the device. This is a stress rating for transient conditions only. Functional operation of the device at these or any other conditions above those indicated in the 'Operating Range' of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Outputs should not be shorted for more than 30 seconds. No more than one output should be shorted at any time.

OPERATING RANGES

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
T_A	Temperature, Ambient	0		70	°C
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
V_{SS}	Supply Voltage	0	0	0	V
V_{IL}	Logic '0' Input Voltage [1]	−0.5		0.8	V
V_{IH}	Logic '1' Input Voltage	2.2		V_{CC} + 0.5	V

NOTE:

1. Negative undershoot of up to 3.0 V is permitted once per cycle.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP [1]	MAX	UNIT
I_{CC1}	Operating Current [2]	t_{CYCLE} = 20 ns		115	180	mA
I_{CC1}	Operating Current [2]	t_{CYCLE} = 25 ns		105	175	mA
I_{CC1}	Operating Current [2]	t_{CYCLE} = 35 ns		95	165	mA
I_{SB1}	Standby Current	$\overline{E}_1 \geq V_{IH}$ or $E_2 \leq V_{IL}$ t_{CYC} = min, I_{OUT} = 0		12	25	mA
I_{SB2}	Standby Current	$\overline{E}_1 \geq V_{CC}$ − 0.2 V or $E_2 \leq$ 0.2 V, t_{CYC} = min, I_{OUT} = 0		0.5	2	mA
I_{LI}	Input Leakage Current	V_{IN} = 0 V to V_{CC}	−2		2	µA
I_{LO}	I/O Leakage Current	V_{IN} = 0 V to V_{CC}	−2		2	µA
V_{OH}	Output High Voltage	I_{OH} = −4.0 mA	2.4			V
V_{OL}	Output Low Voltage	I_{OL} = 8.0 mA			0.4	V
V_{DR}	Data Retention Voltage	$\overline{E}_1 \geq V_{CC}$ − 0.2 V and $E_2 \leq$ 0.2 V	2		5.5	V
I_{DR}	Data Retention Current	V_{CC} = 3 V, $\overline{E}_1 \geq V_{CC}$ − 0.2 V and $E_2 \leq$ 0.2 V			500	µA

NOTES:

1. Typical values at V_{CC} = 5 V, T_A = 25°C.
2. I_{CC} is dependent upon output loading and cycle rates. Specified values are with outputs open.

AC TEST CONDITIONS

PARAMETER	RATING
Input Pulse Levels	V_{SS} to 3 V
Input Rise and Fall Times	5 ns
Input and Output Timing Ref. Levels	1.5 V
Output Load, Timing Tests	Figure 3

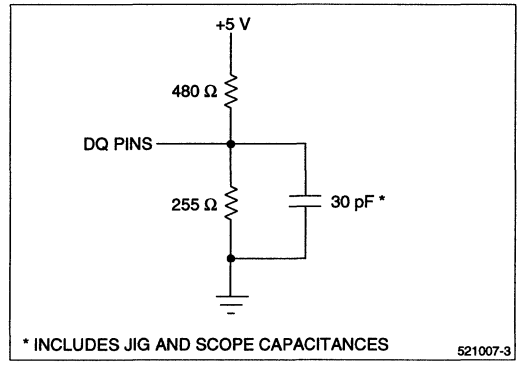


Figure 3. Output Load Circuit

CAPACITANCE [1,2]

PARAMETER	RATING
C_{IN} (Input Capacitance)	7 pF
C_{DQ} (I/O Capacitance)	8 pF

NOTES:

1. Capacitances are maximum values at 25°C measured at 1.0 MHz with V_{Bias} = 0 V and V_{CC} = 5.0 V.
2. Sample tested only.

DATA RETENTION TIMING

For data retention mode, either $\overline{E}_1 \geq V_{CC} - 0.2$ V or $E_2 \leq 0.2$ V. The other control signals must be at valid CMOS levels ($V_{CC} - 0.2\ V \leq V_{IN} \leq 0.2$ V). The address and data buses are 'Don't Care.'

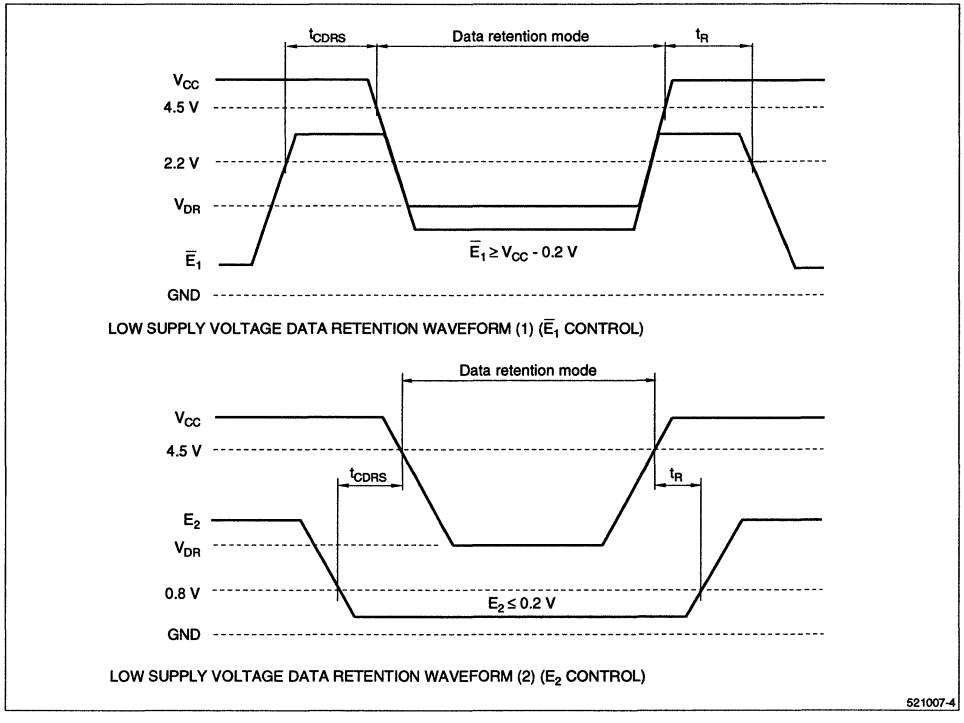


Figure 4. Data Retention Timing

AC ELECTRICAL CHARACTERISTICS [1] (Over Operating Range)

SYMBOL	DESCRIPTION	-20		-25		-35		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	
READ CYCLE								
t_{RC}	Read Cycle Timing	20		25		35		ns
t_{AA}	Address Access Time		20		25		35	ns
t_{OH}	Output Hold from Address Change	5		5		5		ns
t_{EA}	Chip Enable to Valid Data		20		25		35	ns
t_{ELZ}	Chip Enable to Output Active [2,3]	5		5		5		ns
t_{EHZ}	Chip Disable to Output High-Z [2,3]		8		10		15	ns
t_{GA}	$\overline{G}$ Low to Valid Data		7		8		12	ns
t_{GLZ}	$\overline{G}$ Low to Output Active [2,3]	0		0		0		ns
t_{GHZ}	$\overline{G}$ High to Output High-Z [2,3]		8		10		20	ns
t_{PU}	Chip Enable to Power Up Time [4]	0		0		0		ns
t_{PD}	Chip Disable to Power Down Time [4]		20		25		35	ns
WRITE CYCLE								
t_{WC}	Write Cycle Time	20		25		35		ns
t_{EW}	Chip Enable to End of Write	13		15		20		ns
t_{AW}	Address Valid to End of Write	13		15		20		ns
t_{AS}	Address Setup	0		0		0		ns
t_{AH}	Address Hold from End of Write	0		0		0		ns
t_{WP}	$\overline{W}$ Pulse Width	13		15		20		ns
t_{DW}	Input Data Setup Time	9		10		12		ns
t_{DH}	Input Data Hold Time	0		0		0		ns
t_{WHZ}	$\overline{W}$ Low to Output High-Z [2,3]	0	8	0	10	0	15	ns
t_{WLZ}	$\overline{W}$ High to Output Active [2,3]	5		5		5		ns

NOTES:

1. AC Electrical Characteristics specified at 'AC Test Conditions' levels.
2. Active output to High-Z and High-Z to output active tests specified for a ±500 mV transition from steady state levels into the test load. C_{Load} = 5 pF.
3. Sample tested only.
4. Guaranteed but not tested.

TIMING DIAGRAMS – READ CYCLE

Read Cycle No. 1

Chip is in Read Mode: $\overline{W}$ and E_2 are HIGH, $\overline{E}_1$ and $\overline{G}$ are LOW. Read cycle timing is referenced from when all addresses are stable until the first address transition. Crosshatched portion of Data Out implies that data lines are in the Low-Z state but the data is not guaranteed to be valid until t_{AA}.

Read Cycle No. 2

Chip is in Read Mode: $\overline{W}$ is HIGH. Timing illustrated for the case when addresses are valid before $\overline{E}_1$ and E_2 are both active. Data Out is not specified to be valid until t_{EA} or t_{GA}, but may become valid as soon as t_{ELZ} or t_{GLZ}. Outputs will transition directly from High-Z to Valid Data Out. Valid data will be present following t_{GA} only if t_{EA} timing is met.

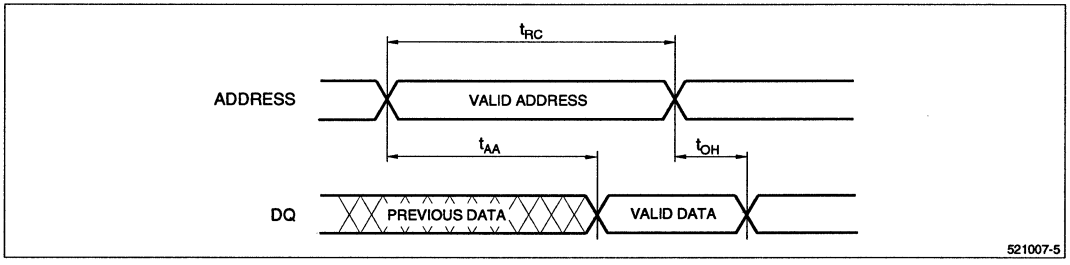


Figure 5. Read Cycle No. 1

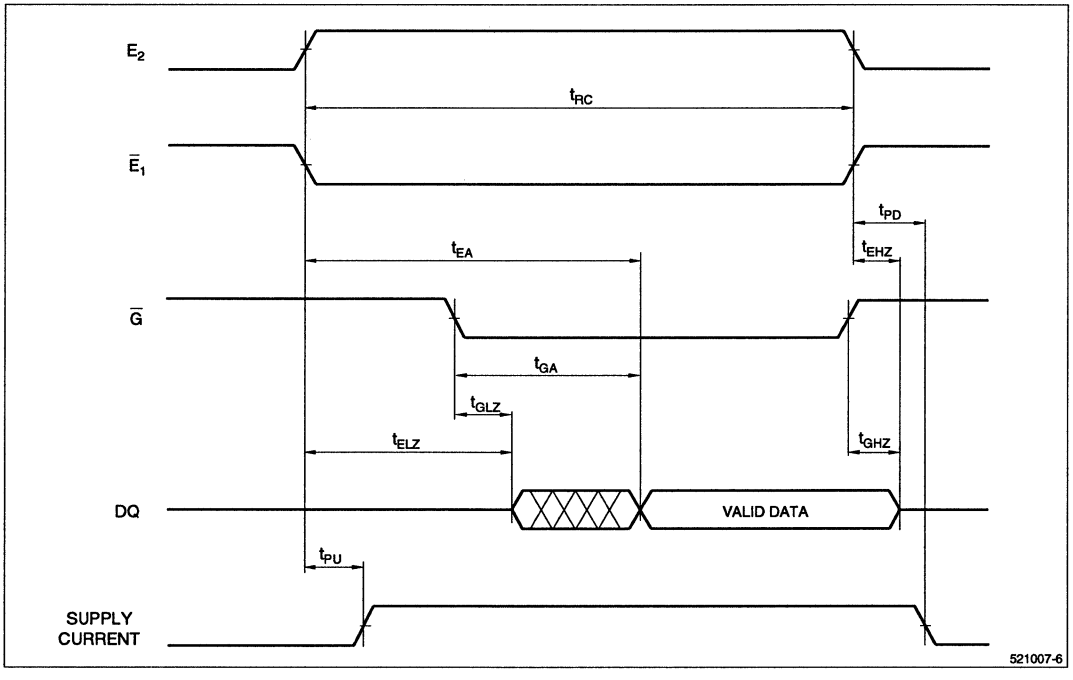


Figure 6. Read Cycle No. 2

TIMING DIAGRAMS – WRITE CYCLE

Addresses must be stable during Write cycles. The outputs will remain in the High-Z state if $\overline{W}$ is LOW when both $\overline{E}_1$ and E_2 are active. If $\overline{G}$ is HIGH, the outputs will remain in the High-Z state. Although these examples illustrate timing with $\overline{G}$ active, it is recommended that $\overline{G}$ be held HIGH for all Write cycles. This will prevent outputs from becoming active, preventing bus contention, thereby reducing system noise.

Write Cycle No. 1 ($\overline{W}$ Controlled)

Chip is selected: $\overline{E}_1$ and $\overline{G}$ are LOW, E_2 is HIGH. Using only $\overline{W}$ to control Write cycles may not offer the best performance since both t_{WHZ} and t_{DW} timing specifications must be met.

Write Cycle No. 2 ($\overline{E}$ Controlled)

$\overline{G}$ is LOW. DQ lines may transition to Low-Z if the falling edge of $\overline{W}$ occurs after the falling edge of $\overline{E}$.

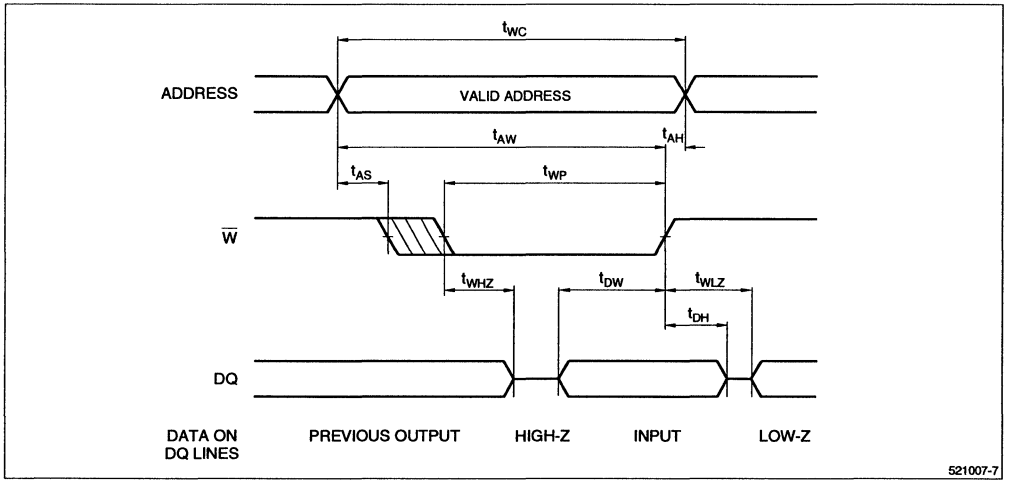


Figure 7. Write Cycle No. 1

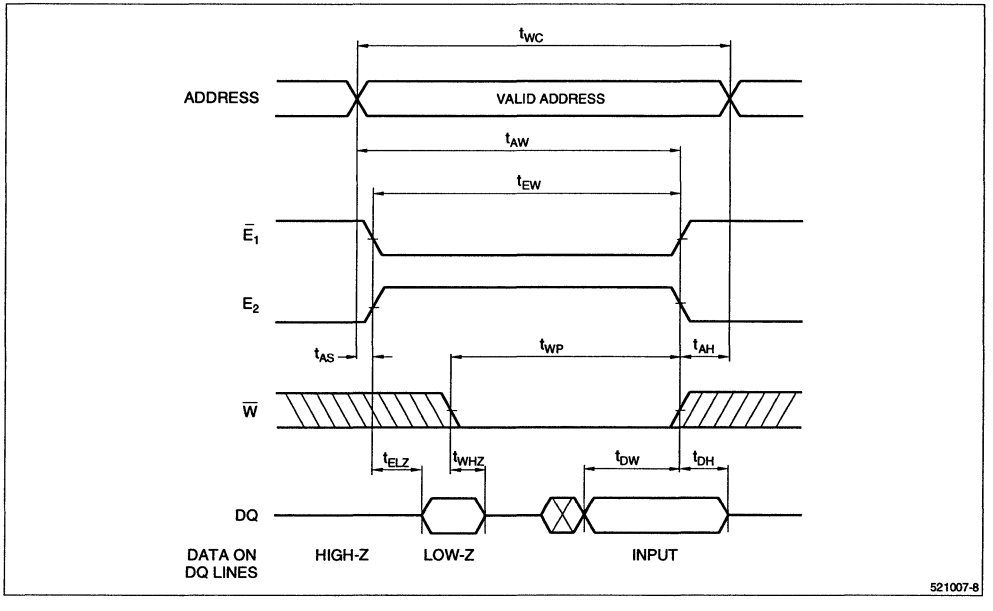
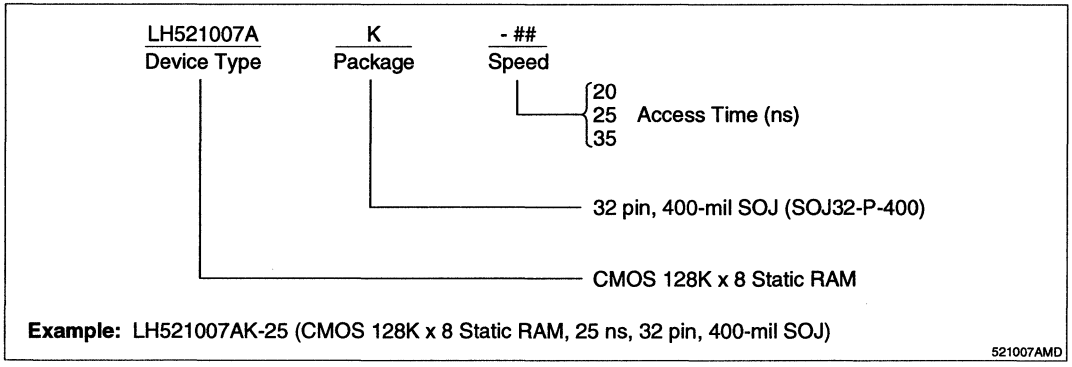


Figure 8. Write Cycle No. 2

ORDERING INFORMATION



LH521008

CMOS 128K × 8 Static RAM

FEATURES

- Fast Access Times: 20/25/35 ns
- Low-Power Standby when Deselected
- TTL Compatible I/O
- 5 V ±10% Supply
- Fully-Static Operation
- 2 V Data Retention
- JEDEC Standard Pinout
- Package: 32-Pin, 400-mil SOJ

FUNCTIONAL DESCRIPTION

The LH521008 is a high-speed 1,048,576-bit static RAM organized as 128K × 8. A fast, efficient design is obtained with a CMOS periphery and a matrix constructed with polysilicon load memory cells.

This RAM is fully static in operation. The Chip Enable ($\overline{E}$) control permits Read and Write operations when active (LOW) or places the RAM in a low-power standby mode when inactive (HIGH). Standby power drops to its lowest level (I_{SB1}) if $\overline{E}$ is raised to within 0.2 V of V_{CC}.

Write cycles occur when both Chip Enable ($\overline{E}$) and Write Enable ($\overline{W}$) are LOW. Data is transferred from the DQ pins to the memory location specified by the 17 address lines. The proper use of the Output Enable control ($\overline{G}$) can prevent bus contention.

When $\overline{E}$ is LOW and $\overline{W}$ is HIGH, a static Read will occur at the memory location specified by the address lines. $\overline{G}$ must be brought LOW to enable the outputs. Since the device is fully static in operation, new Read cycles can be performed by simply changing the address.

High-frequency design techniques should be employed to obtain the best performance from this device. Solid, low-impedance power and ground planes, with high-frequency decoupling capacitors, are recommended. Series termination of the inputs should be considered when transmission line effects occur.

PIN CONNECTIONS

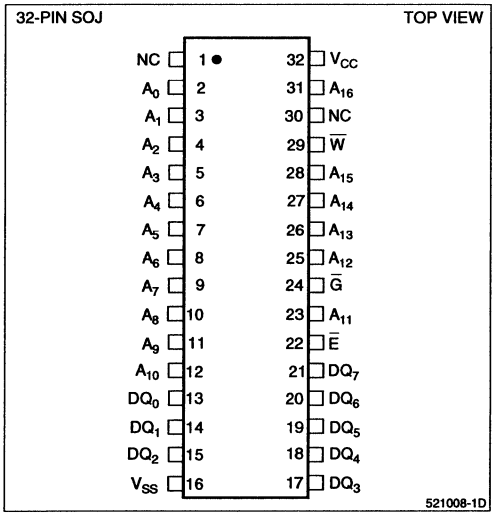


Figure 1. Pin Connections for SOJ Package

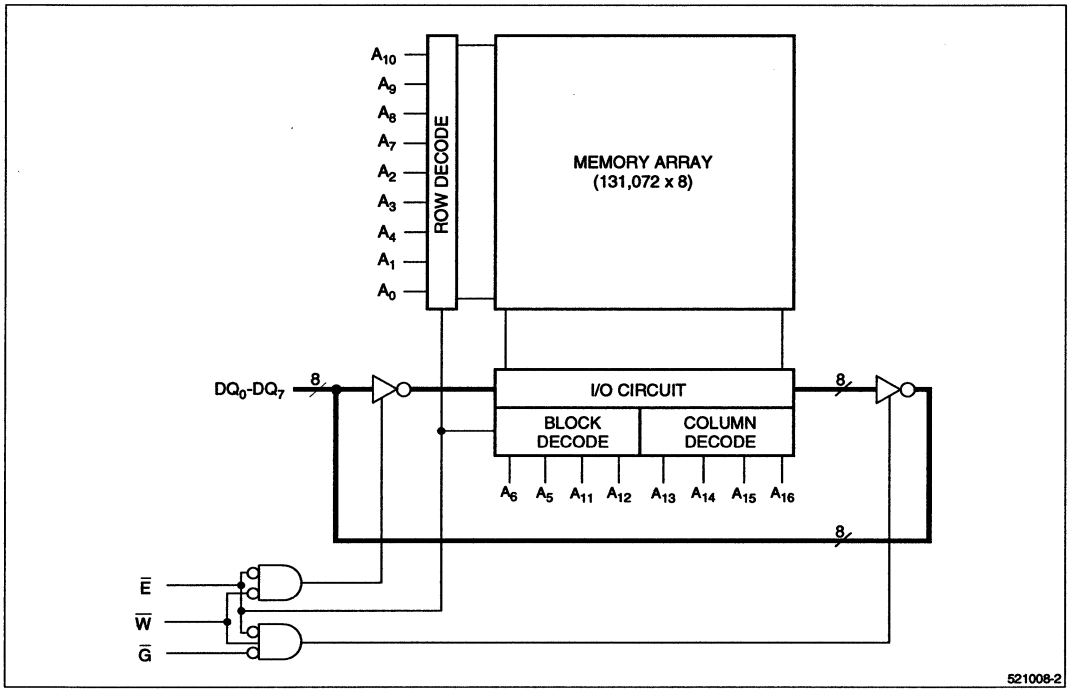


Figure 2. LH521008 Block Diagram

TRUTH TABLE

$\overline{E}$	$\overline{G}$	$\overline{W}$	MODE	DQ	Icc
H	X	X	Standby	High-Z	Standby
L	H	H	Read	High-Z	Active
L	L	H	Read	Data Out	Active
L	X	L	Write	Data In	Active

NOTE:
X = Don't Care, L = LOW, H = HIGH

PIN DESCRIPTIONS

PIN	DESCRIPTION
$A_0 - A_{16}$	Address Inputs
$DQ_0 - DQ_7$	Data Inputs/Outputs
$\overline{E}$	Chip Enable input
$\overline{G}$	Output Enable input
$\overline{W}$	Write Enable input
V_{CC}	Positive Power Supply
V_{SS}	Ground

ABSOLUTE MAXIMUM RATINGS [1]

PARAMETER	RATING
V_{CC} to V_{SS} Potential	−0.5 V to 7 V
Input Voltage Range	−0.5 V to V_{CC} + 0.5 V
DC Output Current [2]	± 40 mA
Storage Temperature Range	−65° C to 150° C
Power Dissipation (Package Limit)	1.0 W

NOTES:

1. Stresses greater than those listed under 'Absolute Maximum Ratings' may cause permanent damage to the device. This is a stress rating for transient conditions only. Functional operation of the device at these or any other conditions above those indicated in the 'Operating Range' of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Outputs should not be shorted for more than 30 seconds. No more than one output should be shorted at any time.

OPERATING RANGES

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
T_A	Temperature, Ambient	0		70	°C
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
V_{SS}	Supply Voltage	0	0	0	V
V_{IL}	Logic '0' Input Voltage [1]	−0.5		0.8	V
V_{IH}	Logic '1' Input Voltage	2.2		V_{CC} + 0.5	V

NOTE:

1. Negative undershoot of up to 3.0 V is permitted once per cycle.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP [1]	MAX	UNIT
I_{CC1}	Operating Current [2]	t_{CYCLE} = 20 ns $\overline{E} = V_{IL}$, $\overline{W} = V_{IL}$ or V_{IH}		110	180	mA
I_{CC1}	Operating Current [2]	t_{CYCLE} = 25 ns $\overline{E} = V_{IL}$, $\overline{W} = V_{IL}$ or V_{IH}		100	180	mA
I_{CC1}	Operating Current [2]	t_{CYCLE} = 35 ns $\overline{E} = V_{IL}$, $\overline{W} = V_{IL}$ or V_{IH}		80	150	mA
I_{SB1}	Standby Current	$\overline{E} \geq V_{CC} - 0.2$ V		0.005	2	mA
I_{SB2}	Standby Current	$\overline{E} \geq V_{IH}$		8	20	mA
I_{LI}	Input Leakage Current	V_{IN} = 0 V to V_{CC}	−2		2	µA
I_{LO}	I/O Leakage Current	V_{IN} = 0 V to V_{CC}	−2		2	µA
V_{OH}	Output High Voltage	I_{OH} = −4.0 mA	2.4			V
V_{OL}	Output Low Voltage	I_{OL} = 8.0 mA			0.4	V
V_{DR}	Data Retention Voltage	$\overline{E} \geq V_{CC} - 0.2$ V	2		5.5	V
I_{DR}	Data Retention Current	V_{CC} = 3 V, $\overline{E} \geq V_{CC} - 0.2$ V			500	µA

NOTES:

1. Typical values at V_{CC} = 5 V, T_A = 25°C.
2. I_{CC} is dependent upon output loading and cycle rates. Specified values are with outputs open.

AC TEST CONDITIONS

PARAMETER	RATING
Input Pulse Levels	V_{SS} to 3 V
Input Rise and Fall Times	5 ns
Input and Output Timing Ref. Levels	1.5 V
Output Load, Timing Tests	Figure 3

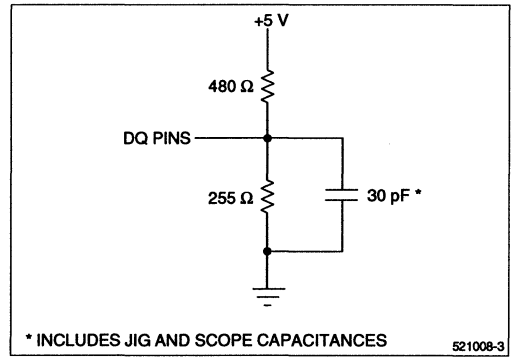


Figure 3. Output Load Circuit

CAPACITANCE [1,2]

PARAMETER	RATING
C_{IN} (Input Capacitance)	6 pF
C_{DQ} (I/O Capacitance)	8 pF

NOTES:

1. Capacitances are maximum values at 25°C measured at 1.0 MHz with V_{Bias} = 0 V and V_{CC} = 5.0 V.
2. Guaranteed but not tested.

DATA RETENTION TIMING

$\overline{E}$ must be held above the lesser of V_{IH} or V_{CC} – 0.2 V to assure proper operation when V_{CC} < 4.5 V. $\overline{E}$ must be V_{CC} – 0.2 V or greater to meet I_{DR} specification. All other inputs are 'Don't Care.'

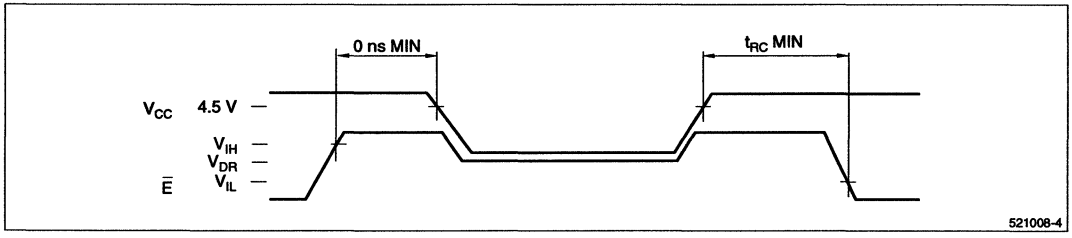


Figure 4. Data Retention Timing

AC ELECTRICAL CHARACTERISTICS [1] (Over Operating Range)

SYMBOL	DESCRIPTION	-20		-25		-35		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	
READ CYCLE								
t_{RC}	Read Cycle Timing	20		25		35		ns
t_{AA}	Address Access Time		20		25		35	ns
t_{OH}	Output Hold from Address Change	3		3		3		ns
t_{EA}	$\overline{E}$ Low to Valid Data		20		25		35	ns
t_{ELZ}	$\overline{E}$ Low to Output Active [2,3]	3		3		3		ns
t_{EHZ}	$\overline{E}$ High to Output High-Z [2,3]		10		12		20	ns
t_{GA}	$\overline{G}$ Low to Valid Data		8		10		20	ns
t_{GLZ}	$\overline{G}$ Low to Output Active [2,3]	0		0		0		ns
t_{GHZ}	$\overline{G}$ High to Output High-Z [2,3]		8		10		20	ns
t_{PU}	$\overline{E}$ Low to Power Up Time [3]	0		0		0		ns
t_{PD}	$\overline{E}$ High to Power Down Time [3]		20		25		35	ns
WRITE CYCLE								
t_{WC}	Write Cycle Time	20		25		35		ns
t_{EW}	$\overline{E}$ Low to End of Write	15		20		30		ns
t_{AW}	Address Valid to End of Write	15		20		30		ns
t_{AS}	Address Setup	0		0		0		ns
t_{AH}	Address Hold from End of Write	0		0		0		ns
t_{WP}	$\overline{W}$ Pulse Width	15		20		25		ns
t_{DW}	Input Data Setup Time	12		15		15		ns
t_{DH}	Input Data Hold Time	0		0		0		ns
t_{WHZ}	$\overline{W}$ Low to Output High-Z [2,3]		8		10		15	ns
t_{WLZ}	$\overline{W}$ High to Output Active [2,3]	3		3		3		ns

NOTES:

1. AC Electrical Characteristics specified at 'AC Test Conditions' levels.
2. Active output to High-Z and High-Z to output active tests specified for a ±500 mV transition from steady state levels into the test load. C_{Load} = 5 pF.
3. Guaranteed but not tested.

TIMING DIAGRAMS – READ CYCLE

Read Cycle No. 1

Chip is in Read Mode: $\overline{W}$ is HIGH, $\overline{E}$ is LOW and $\overline{G}$ is LOW. Read cycle timing is referenced from when all addresses are stable until the first address transition. Crosshatched portion of Data Out implies that data lines are in the Low-Z state but the data is not guaranteed to be valid until t_{AA}.

Read Cycle No. 2

Chip is in Read Mode: $\overline{W}$ is HIGH. Timing illustrated for the case when addresses are valid before $\overline{E}$ goes LOW. Data Out is not specified to be valid until t_{EA} or t_{GA}, but may become valid as soon as t_{ELZ} or t_{GLZ}. Outputs will transition directly from High-Z to Valid Data Out. Valid data will be present when both t_{GA} and t_{EA} timing are met.

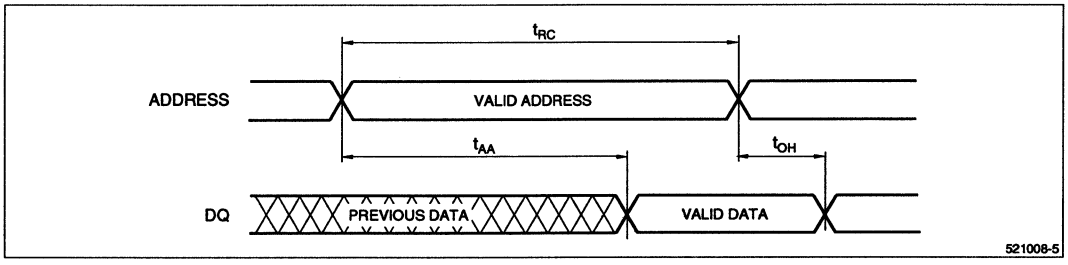


Figure 5. Read Cycle No. 1

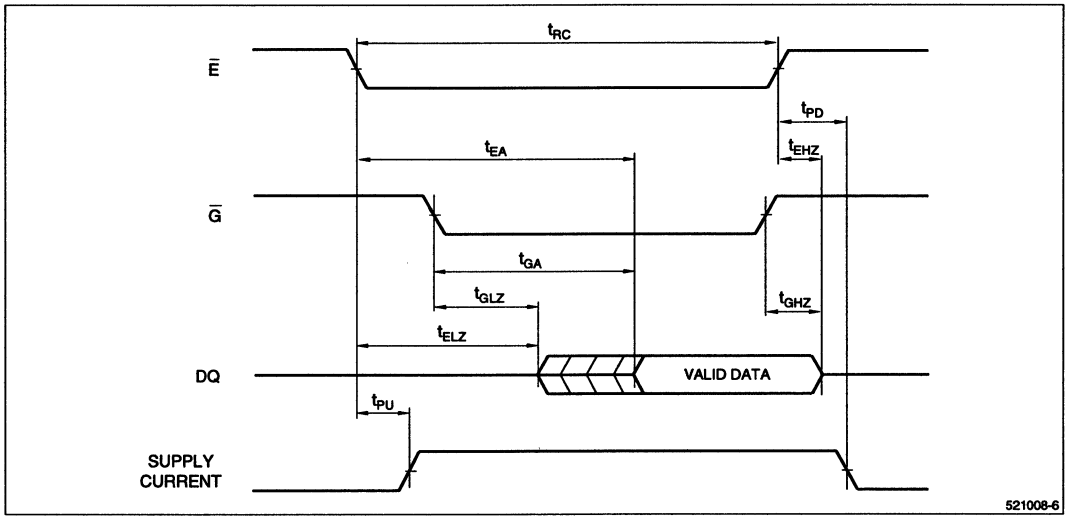


Figure 6. Read Cycle No. 2

TIMING DIAGRAMS – WRITE CYCLE

Addresses must be stable during Write cycles. The outputs will remain in the High-Z state if $\overline{W}$ is LOW when $\overline{E}$ goes LOW. If $\overline{G}$ is HIGH, the outputs will remain in the High-Z state. Although these examples illustrate timing with $\overline{G}$ active, it is recommended that $\overline{G}$ be held HIGH for all Write cycles. This will prevent the outputs from becoming active, preventing bus contention, thereby reducing system noise.

Write Cycle No. 1 ($\overline{W}$ Controlled)

Chip is selected: $\overline{E}$ is LOW, $\overline{G}$ is LOW. Using only $\overline{W}$ to control Write cycles may not offer the best performance since both t_{WHZ} and t_{DW} timing specifications must be met.

Write Cycle No. 2 ($\overline{E}$ Controlled)

$\overline{G}$ is LOW. DQ lines may transition to Low-Z if the falling edge of $\overline{W}$ occurs after the falling edge of $\overline{E}$.

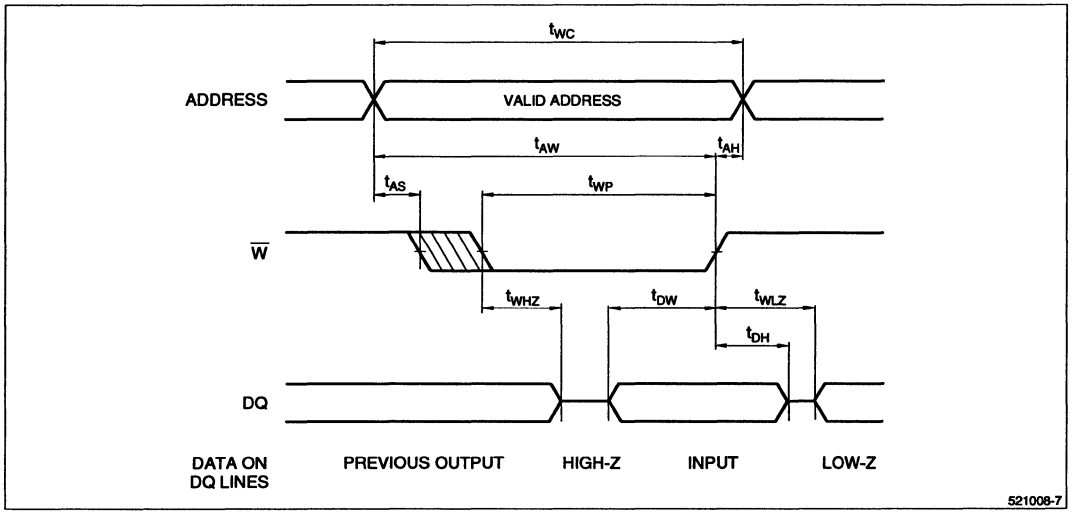


Figure 7. Write Cycle No. 1

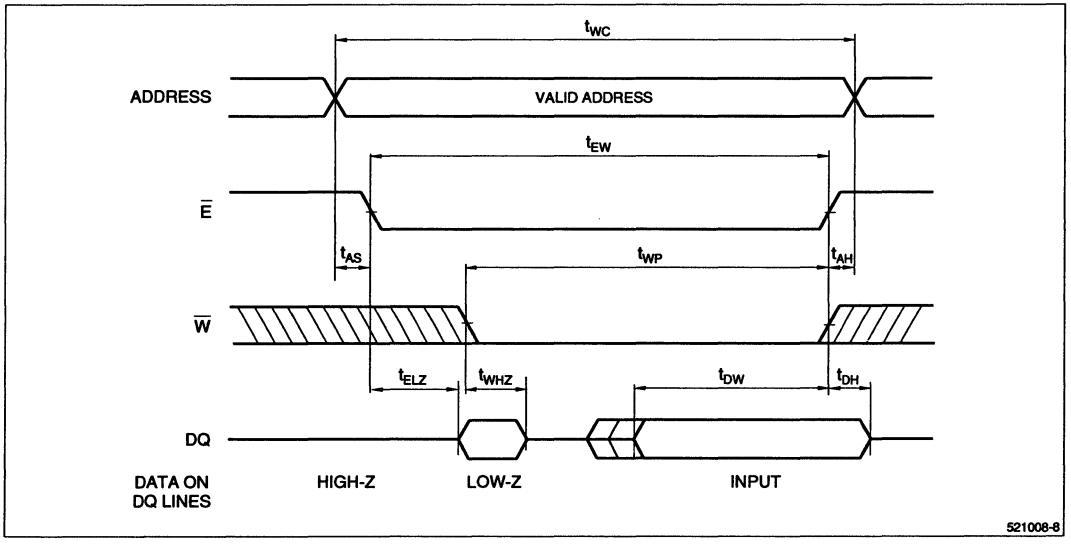
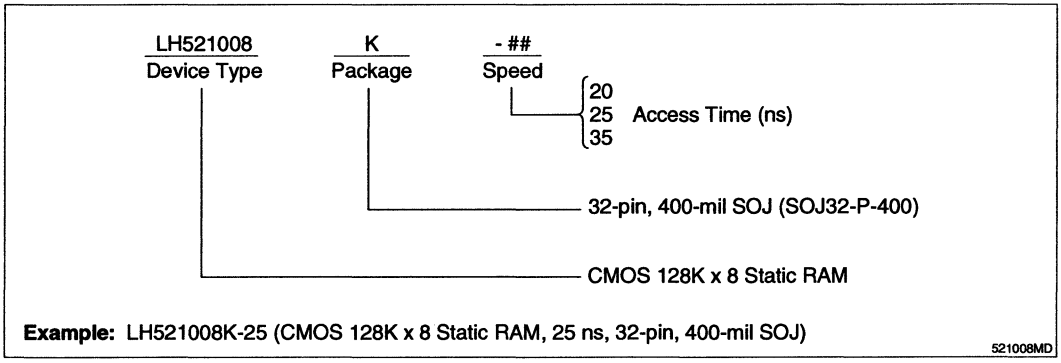


Figure 8. Write Cycle No. 2

ORDERING INFORMATION



LH521028

CMOS 64K × 18 Static RAM

FEATURES

- Fast Access Times: 20/25/35 ns
- Wide Word (18-Bits) for:
  - Improved Performance
  - Reduced Component Count
  - Nine-bit Byte for Parity
- Transparent Address Latch
- Reduced Loading on Address Bus
- Low-Power Stand-by Mode when Deselected
- TTL Compatible I/O
- 5 V ± 10% Supply
- 2 V Data Retention
- JEDEC Standard Pinout
- Package: 52-Pin PLCC

FUNCTIONAL DESCRIPTION

The LH521028 is a high-speed 1,179,648-bit CMOS SRAM organized as 64K × 18. A fast, efficient design is obtained with a CMOS periphery and a matrix constructed with polysilicon load memory cells. The LH521028 is available in a compact 52-Pin PLCC, which along with the six pairs of supply terminals, provide for reliable operation.

The control signals include Write Enable ($\overline{W}$), Chip Enable ($\overline{E}$), High and Low Byte Select ($\overline{S}_L$ and $\overline{S}_H$), Output Enable ($\overline{G}$) and Address Latch Enable (ALE). The wide word provides for reduced component count, improved density, reduced Address bus loading and improved performance. The wide word also allows for byte-parity with no additional RAM required.

This RAM is fully static in operation. The Chip Enable ($\overline{E}$) control permits Read and Write operations when active (LOW) or places the RAM in a low-power standby mode when inactive (HIGH). The Byte-select controls, $\overline{S}_H$ and $\overline{S}_L$, are also used to enable or disable Read and Write operations on the high and the low bytes. The Address Latches are transparent when ALE is HIGH (for applications not requiring a latch), and are latched when ALE is LOW. The Address Latches and the wide word help to eliminate the need for external Address bus buffers and/or latches.

Write cycles occur when Chip Enable ($\overline{E}$), $\overline{S}_H$ and/or $\overline{S}_L$, and Write Enable ($\overline{W}$) are LOW. The Byte-select signals can be used for Byte-write operations by disabling the other byte during the Write operation. Data is transferred from the DQ pins to the memory location specified by the 16 address lines. The proper use of the Output Enable control ($\overline{G}$) can prevent bus contention.

When $\overline{E}$ and either $\overline{S}_H$ or $\overline{S}_L$ are LOW and $\overline{W}$ is HIGH, a static Read will occur at the memory location specified by the address lines. $\overline{G}$ must be brought LOW to enable the outputs. Since the device is fully static in operation, new Read cycles can be performed by simply changing the address with ALE HIGH.

PIN CONNECTIONS

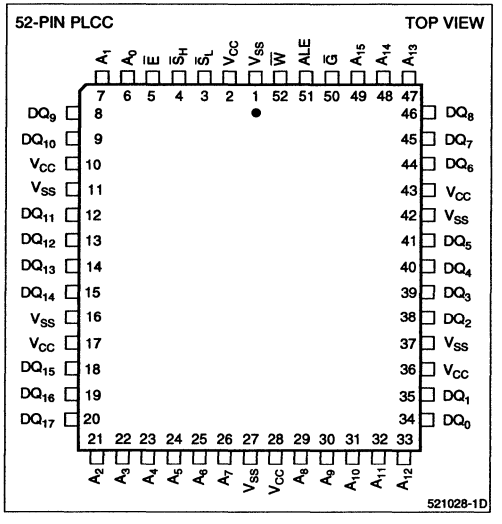


Figure 1. Pin Connections for PLCC Package

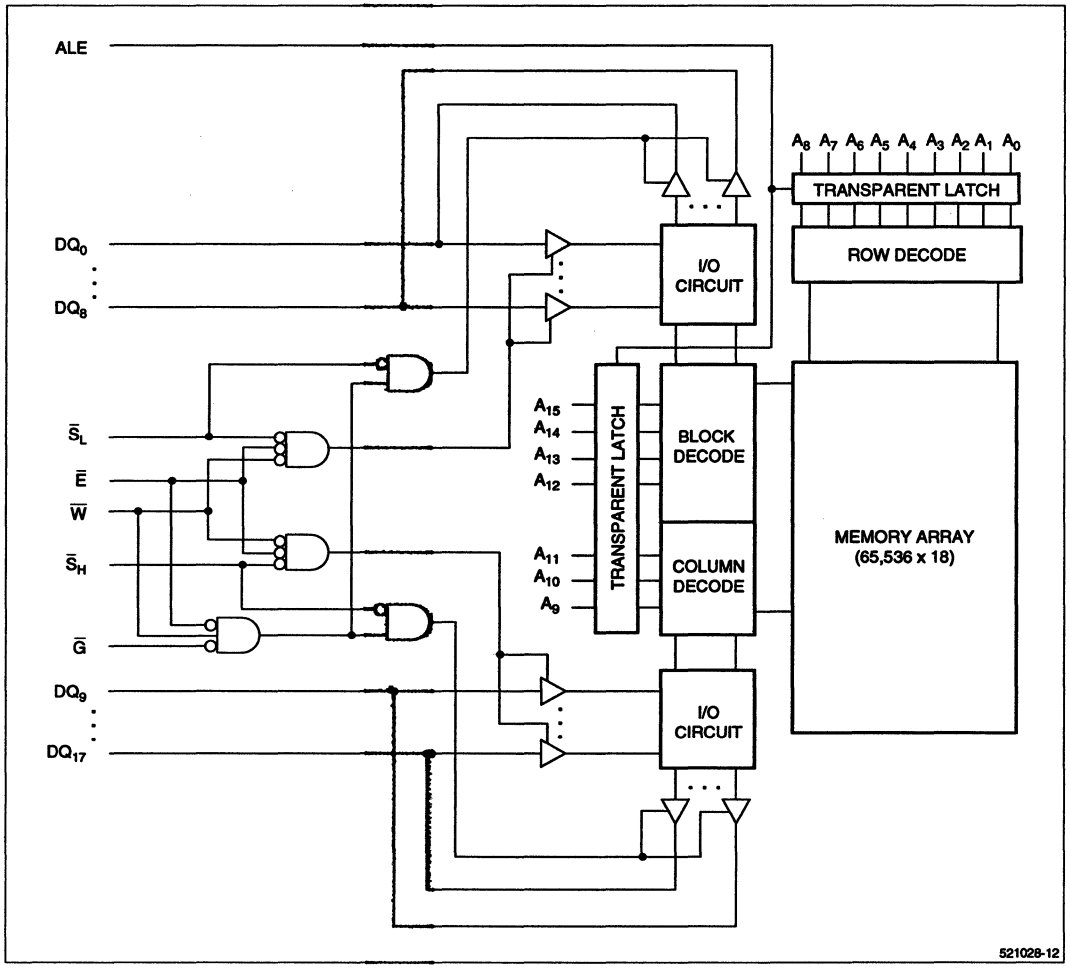


Figure 2. LH521028 Block Diagram

TRUTH TABLE

ADDRESS	$\overline{E}$	$\overline{S}_H$	$\overline{S}_L$	ALE	$\overline{G}$	$\overline{W}$	DQ_0-DQ_8	DQ_9-DQ_{17}	MODE	I_{CC}
Don't Care	H	X	X	H	X	X	High-Z	High-Z	Standby	I_{SB}
Valid	L	L	H	H	L	H	Active	High-Z	Read	I_{CC1}
Valid	L	H	L	H	L	H	High-Z	Active	Read	I_{CC1}
Valid	L	L	L	H	L	H	Active	Active	Read	I_{CC1}
Valid	L	L	L	H	H	H	High-Z	High-Z	Read	I_{CC1}
Don't Care	L	L	L	L	L	H	Data Out	Data Out	Read	I_{CC1}
Valid	L	L	H	H	X	L	Data In	Don't Care	Write, low byte	I_{CC1}
Valid	L	H	L	H	X	L	Don't Care	Data In	Write, high byte	I_{CC1}
Valid	L	L	L	H	X	L	Data In	Data In	Write, both bytes	I_{CC1}
Valid	L	H	H	H	X	L	Don't Care	Don't Care	Write, inhibited	I_{CC1}
Don't Care	L	L	L	L	X	L	Data In	Data In	Write, both bytes	I_{CC1}

NOTE:
X = Don't Care, L = LOW, H = HIGH

PIN DESCRIPTIONS

PIN	SIGNAL
1	V_{SS}
2	V_{CC}
3	$\overline{S}_L$
4	$\overline{S}_H$
5	$\overline{E}$
6	A_0
7	A_1
8	DQ_9
9	DQ_{10}
10	V_{CC}
11	V_{SS}
12	DQ_{11}
13	DQ_{12}

PIN	SIGNAL
14	DQ_{13}
15	DQ_{14}
16	V_{SS}
17	V_{CC}
18	DQ_{15}
19	DQ_{16}
20	DQ_{17}
21	A_2
22	A_3
23	A_4
24	A_5
25	A_6
26	A_7

PIN	SIGNAL
27	V_{SS}
28	V_{CC}
29	A_8
30	A_9
31	A_{10}
32	A_{11}
33	A_{12}
34	DQ_0
35	DQ_1
36	V_{CC}
37	V_{SS}
38	DQ_2
39	DQ_3

PIN	SIGNAL
40	DQ_4
41	DQ_5
42	V_{SS}
43	V_{CC}
44	DQ_6
45	DQ_7
46	DQ_8
47	A_{13}
48	A_{14}
49	A_{15}
50	$\overline{G}$
51	ALE
52	$\overline{W}$

PIN DEFINITIONS

V_{CC} Positive Supply Voltage Terminals

V_{SS} Reference Terminals

$A_0 - A_{15}$ Address Bus Input

The Address bus is decoded to select one 18-bit word out of the total 64K words for Read and Write operations.

$\overline{E}$ Chip Enable Active LOW Input

Chip Enable is used to enable the device for Read and Write operations. When HIGH, both Read and Write operations are disabled and the device is in a reduced power state. When LOW, a Read or Write operation is enabled.

$\overline{W}$ Write Enable Active LOW Input

Write Enable is used to select either Read or Write operations when the device is enabled. When Write Enable is HIGH and the device is Enabled, a Read operation is selected. When Write Enable is LOW and the device is enabled, a Write operation is selected. A Byte-write operation is available by using the Byte-select controls.

$\overline{S}_H$, $\overline{S}_L$ Select High Select Low Active LOW Inputs

The Select High and Select Low signals, in conjunction with the Chip Enable and Write Enable signals, allow the selection of the individual bytes for Read and Write operations. When High, the Select signal will deselect its byte and prevent Read or Write operations. When the Select signal is LOW and Chip Enable is LOW, a Read or Write operation is performed at the location determined by the contents of the Address bus. When Chip Enable is HIGH, the Select signals are Don't Care. Select Low ($\overline{S}_L$) is assigned to $DQ_0 - DQ_8$ and Select High ($\overline{S}_H$) is assigned to $DQ_9 - DQ_{17}$.

ALE Address Latch Enable Active High Input

The Address Latch Enable signal is used to control the Transparent latches on the Address bus. The Latches are transparent when HIGH and are latched when LOW. If not required, Address Latch Enable may be tied HIGH, leaving the Address bus in a transparent condition.

$DQ_0 - DQ_{17}$ Data Bus Input/Output

$DQ_0 - DQ_8$ comprise the Low byte, selected by $\overline{S}_L$, and $DQ_9 - DQ_{17}$ comprise the High Data byte, selected by $\overline{S}_H$. The Data Bus is in a high impedance input mode during Write operations and standby. The Data bus is in a low-impedance output mode during Read operations.

$\overline{G}$ Output Enable Active LOW Input

The Output Enable signal is used to control the output buffers on the Data Input/Output bus. When $\overline{G}$ is HIGH, all output buffers are forced to a high impedance condition. When $\overline{G}$ is LOW, the output buffers will become active only during a Read operation ($\overline{E}$ and $\overline{S}_H$ / $\overline{S}_L$ are LOW, $\overline{W}$ is HIGH).

ABSOLUTE MAXIMUM RATINGS [1]

PARAMETER	RATING
V_{CC} to V_{SS} Potential	−0.5 V to 7 V
Input Voltage Range	−0.5 V to V_{CC} + 0.5 V
DC Output Current [2]	± 40 mA
Storage Temperature Range	−65°C to 150°C
Power Dissipation (Package Limit)	2 W

NOTES:

1. Stresses greater than those listed under 'Absolute Maximum Ratings' may cause permanent damage to the device. This is a stress rating for transient conditions only. Functional operation of the device at these or any other conditions above those indicated in the 'Operating Range' of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Outputs should not be shorted for more than 30 seconds. No more than one output should be shorted at any time.

OPERATING RANGES

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
T_A	Temperature, Ambient	0		70	°C
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
V_{SS}	Supply Voltage	0	0	0	V
V_{IL}	Logic '0' Input Voltage [1]	−0.5		0.8	V
V_{IH}	Logic '1' Input Voltage	2.2		V_{CC} + 0.5	V

NOTE:

1. Negative undershoot of up to 3.0 V is permitted once per cycle.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC1}	Operating Current [1]	t_{CYCLE} = minimum			300	mA
I_{SB1}	Standby Current	$\overline{E} \geq V_{CC} - 0.2$ V $V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V f = 0			4	mA
I_{SB2}	Standby Current	$\overline{E} \geq V_{IH}$ $V_{IN} = V_{IH}$ or V_{IL}			50	mA
I_{LI}	Input Leakage Current	V_{IN} = 0 V to V_{CC}	−2		2	µA
I_{LO}	I/O Leakage Current	V_{IN} = 0 V to V_{CC}	−2		2	µA
V_{OH}	Output High Voltage	I_{OH} = −4.0 mA	2.4			V
V_{OL}	Output Low Voltage	I_{OL} = 8.0 mA			0.4	V

NOTE:

1. I_{CC} is dependent upon output loading and cycle rates. Specified values are with outputs open.

AC TEST CONDITIONS

PARAMETER	RATING
Input Pulse Levels	Vss to 3 V
Input Rise and Fall Times	5 ns
Input and Output Timing Ref. Levels	1.5 V
Output Load, Timing Tests	Figure 3

CAPACITANCE [1,2]

PARAMETER	RATING
C_{IN} (Input Capacitance)	5 pF
C_{DQ} (I/O Capacitance)	7 pF

NOTES:

1. Capacitances are maximum values at 25°C measured at 1.0 MHz with V_{Bias} = 0 V and V_{CC} = 5.0 V.
2. Guaranteed but not tested.

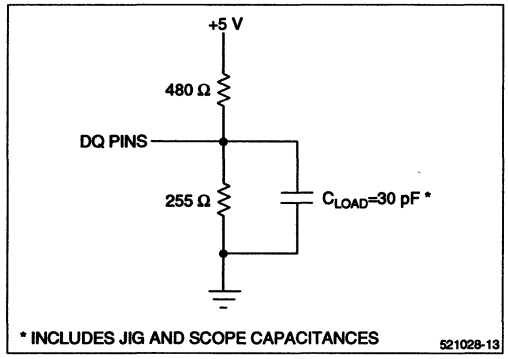


Figure 3. Output Load Circuit

AC ELECTRICAL CHARACTERISTICS [1] (Over Operating Range)

SYMBOL	DESCRIPTION	-20		-25		-35		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	
	READ CYCLE							
t_{RC}	Read Cycle Timing	20		25		35		ns
t_{AA}	Address Access Time		20		25		35	ns
t_{ASL}	Address Setup to Latch Enable	3		3		3		ns
t_{AHL}	Address Hold from Latch Enable	5		6		6		ns
t_{LEA}	Latch Enable to Data Valid		22		27		37	ns
t_{LHM}	Latch Enable High Pulse Width	5		6		6		ns
t_{OH}	Output Hold from Address Change	5		5		5		ns
t_{LH}	Output Hold from Latch High	7		7		7		ns
t_{EA}	$\overline{E}$ Low to Valid Data		20		25		35	ns
t_{ELZ}	$\overline{E}$ Low to Output Active [2,3]	3		3		3		ns
t_{EHZ}	$\overline{E}$ High to Output High-Z [2,3]		10		12		20	ns
t_{SA}	$\overline{S}$ Low to Valid Data		10		12		20	ns
t_{SLZ}	$\overline{S}$ Low to Output Active [2,3]	2		3		3		ns
t_{SHZ}	$\overline{S}$ High to Output High-Z [2,3]		10		12		20	ns
t_{GA}	$\overline{G}$ Low to Valid Data		9		12		20	ns
t_{GLZ}	$\overline{G}$ Low to Output Active [2,3]	0		0		0		ns
t_{GHZ}	$\overline{G}$ High to Output High-Z [2,3]		8		10		20	ns
t_{RCS}	Read Setup from $\overline{W}$ High	0		0		0		ns
t_{RCH}	Read Hold from $\overline{W}$ Low	0		0		0		ns
t_{PU}	$\overline{E}$ LOW to Power Up Time [3]	0		0		0		ns
t_{PD}	$\overline{E}$ HIGH to Power Down Time [3]		20		25		35	ns
t_{WA}	Access Time From Write Enable HIGH		25		28		35	ns
	WRITE CYCLE							
t_{WC}	Write Cycle Time	20		25		35		ns
t_{EW}	$\overline{E}$ Low to End of Write	15		20		30		ns
t_{SW}	$\overline{S}$ LOW to End of Write	15		20		30		ns
t_{AW}	Address Valid to End of Write	15		20		30		ns
t_{AS}	Address Setup to Start of Write	0		0		0		ns
t_{AH}	Address Hold from End of Write	0		0		0		ns
t_{ASL}	Address Setup to Latch Enable	3		3		3		ns
t_{AHL}	Address Hold from Latch Enable	4		4		5		ns
t_{LHW}	Latch Hold from $\overline{W}$ High	0		0		0		ns
t_{LHM}	Latch Enable HIGH Pulse Width	5		6		6		ns
t_{WP}	$\overline{W}$ Pulse Width	15		20		30		ns
t_{DW}	Input Data Setup Time	12		13		15		ns
t_{DH}	Input Data Hold Time	0		0		0		ns
t_{WHZ}	$\overline{W}$ Low to Output High-Z [2,3]		8		10		14	ns
t_{WLZ}	$\overline{W}$ High to Output Active [2,3]	3		3		3		ns

NOTES:

1. AC Electrical Characteristics specified at 'AC Test Conditions' levels.
2. Active output to High-Z and High-Z to output active tests specified for a ±500 mV transition from steady state levels into the test load. C_{Load} = 5 pF.
3. Guaranteed but not tested.

TIMING DIAGRAMS – READ CYCLE

Read Cycle No. 1 (Unlatched Address Controlled Read)

Chip is in Read Mode: ALE is HIGH (transparent mode), $\overline{E}$ and $\overline{G}$ are LOW. Read cycle timing is referenced from when all addresses are stable until the first address transition. Following a $\overline{W}$-controlled Write cycle, t_{WA} and t_{AA} must both be satisfied to ensure valid data. Cross-hatched portion of Data Out implies that data lines are in the Low-Z state but the data is not guaranteed to be valid until t_{AA}.

Read Cycle No. 2 (Unlatched Chip Enable Controlled Read)

Chip is in Read Mode: ALE is HIGH (transparent mode). Read cycle timing is referenced from when $\overline{E}$, $\overline{S}$, and $\overline{G}$ are stable until the first address transition. Cross-hatched portion of Data Out implies that data lines are in the Low-Z state but the data is not guaranteed to be valid.

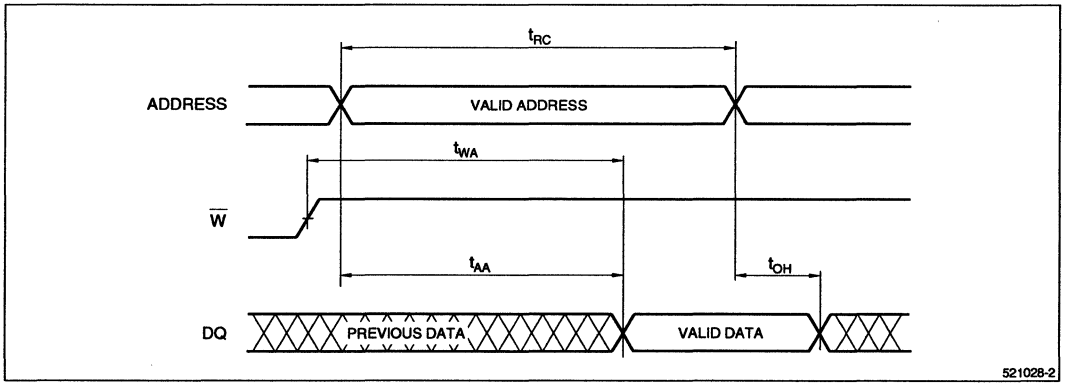


Figure 4. Read Cycle No. 1

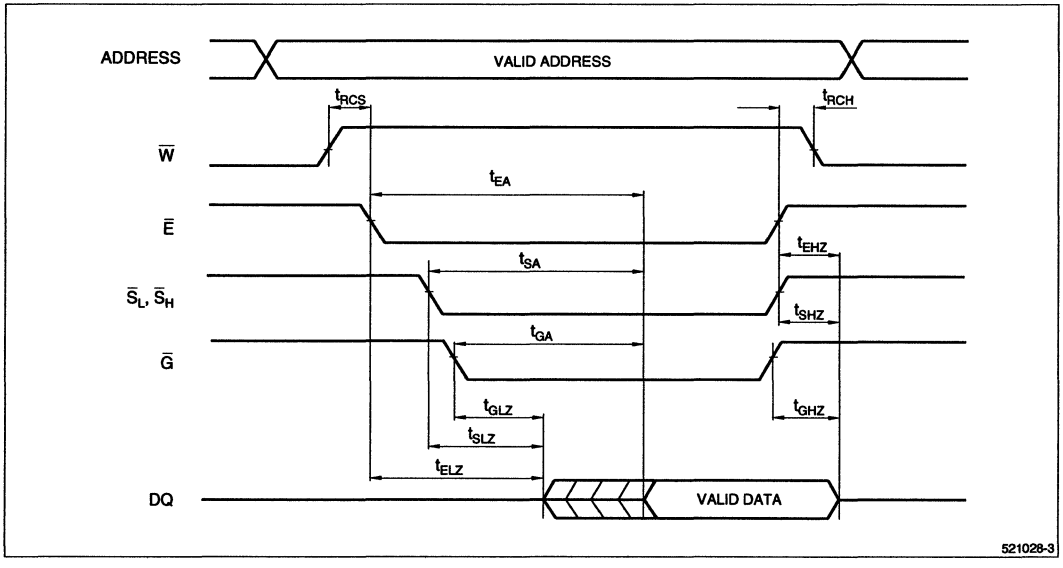


Figure 5. Read Cycle No. 2

TIMING DIAGRAMS – READ CYCLE (cont'd)

Read Cycle No. 3 (Latched Address Controlled Read)

Chip is in Read Mode: $\overline{W}$ is HIGH, $\overline{E}$, $\overline{S}_H$, $\overline{S}_L$ and $\overline{G}$ are LOW. Both t_{AA} and t_{LEA} must be met before valid data is available. If the address is valid prior to the rising edge of ALE, then the access time is t_{LEA}. If the address is valid after ALE is HIGH (or if ALE is tied HIGH) then the access time is t_{AA}. Crosshatched portion of Data Out implies that data lines are in the Low-Z state but the data is not guaranteed to be valid until t_{AA}.

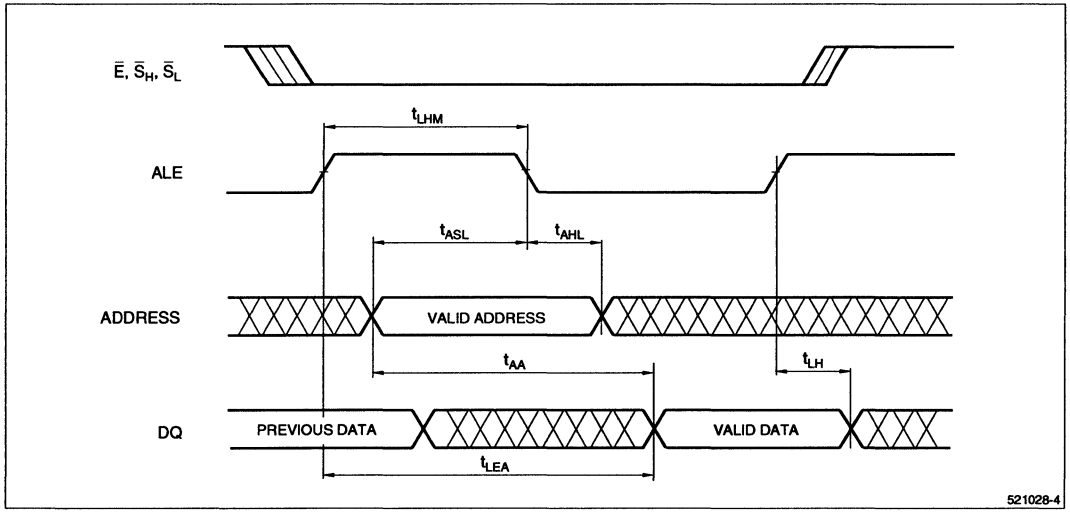


Figure 6. Read Cycle No. 3

TIMING DIAGRAMS – READ CYCLE (cont'd)

Read Cycle No. 4

Chip is in Read Mode: Timing illustrated for the case when addresses are valid before $\overline{E}$ goes LOW. Data Out is not specified to be valid until t_{EA}, t_{SA} and t_{GA}, but may become active as early as t_{ELZ}, t_{SLZ} or t_{GLZ}.

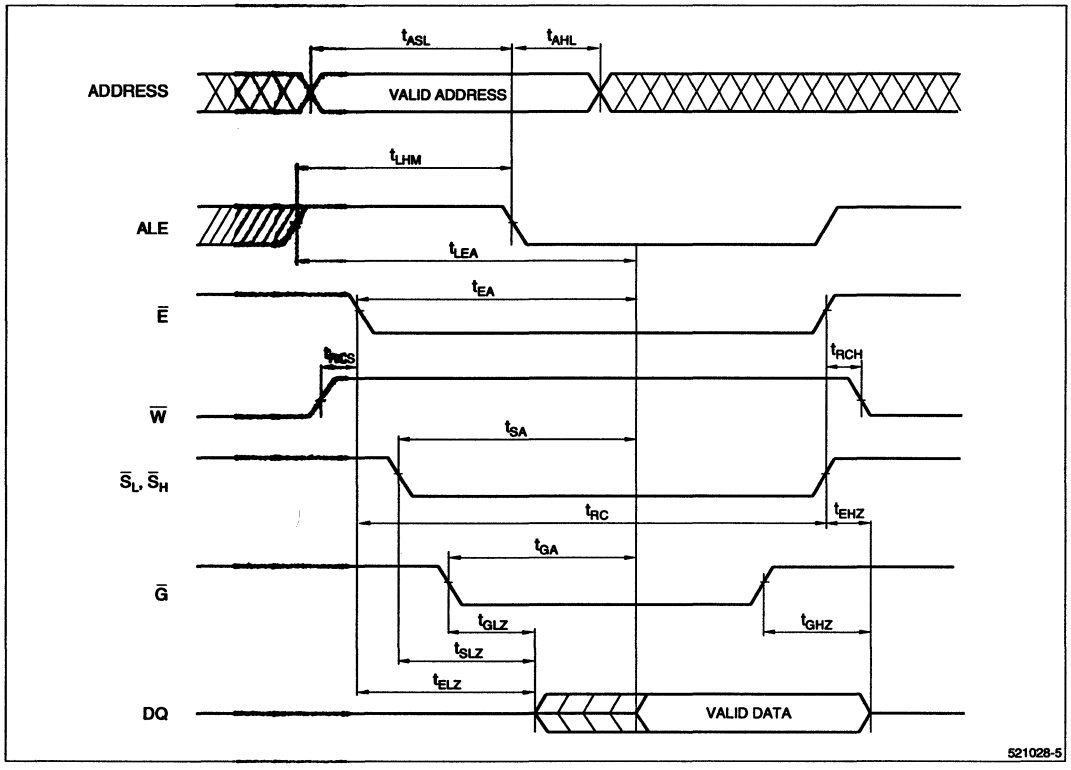


Figure 7. Read Cycle No. 4

TIMING DIAGRAMS – WRITE CYCLE

Addresses must be stable during unlatched Write cycles. The outputs will remain in the High-Z state if $\overline{W}$ is LOW when $\overline{E}$ and $\overline{S}_H$ / $\overline{S}_L$ go LOW. If $\overline{G}$ is HIGH, the outputs will remain in the High-Z state. Although these examples illustrate timing with $\overline{G}$ active, it is recommended that $\overline{G}$ be held HIGH for all Write cycles. This will prevent the LH521028's outputs from becoming active, preventing bus contention, thereby reducing system noise.

Write Cycle No. 1 (Unlatched $\overline{W}$ Controlled Write)

Chip is selected: $\overline{E}$, $\overline{G}$, and $\overline{S}_H$ / $\overline{S}_L$ are LOW, ALE is High. Using only $\overline{W}$ to control Write cycles may not offer the best performance since both t_{WHZ} and t_{DW} timing specifications must be met.

Write Cycle No. 2 ($\overline{E}$, $\overline{S}_L$, $\overline{S}_H$ Controlled Write)

$\overline{G}$ is LOW. DQ lines may transition to Low-Z if the falling edge of $\overline{W}$ occurs after the falling edge of $\overline{E}$, $\overline{S}_H$/$\overline{S}_L$ if $\overline{G}$ is LOW.

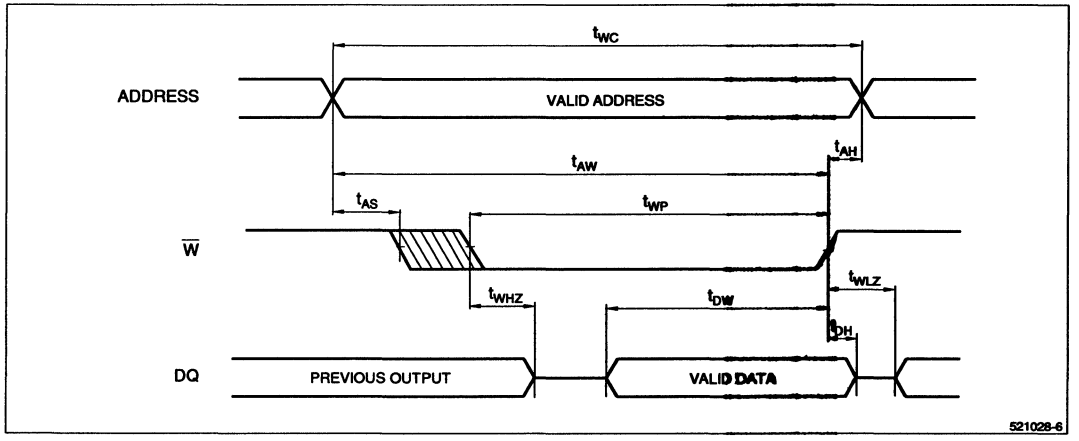


Figure 8. Write Cycle No. 1

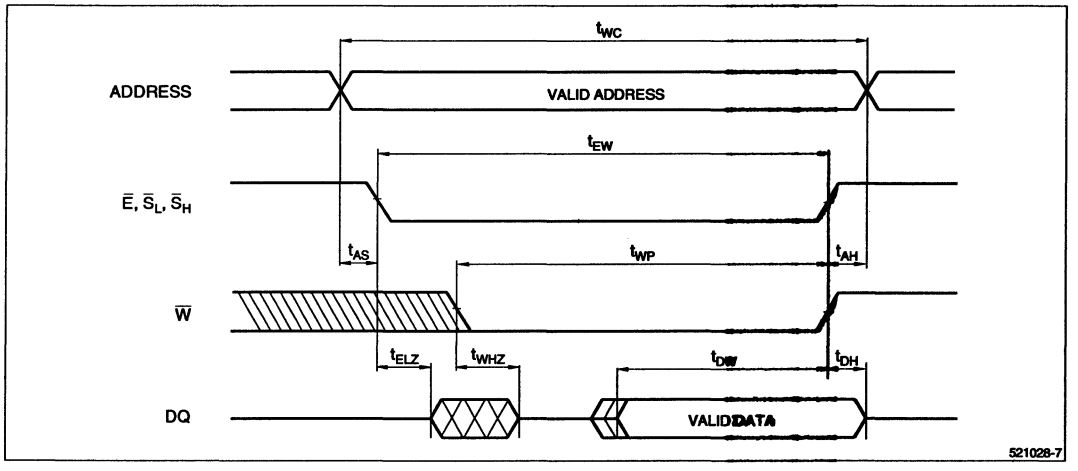


Figure 9. Write Cycle No. 2

TIMING DIAGRAMS – WRITE CYCLE (cont'd)

Write Cycle No. 3 (Latched $\overline{W}$ Controlled Write)

Chip is selected: $\overline{E}$, $\overline{G}$, and $\overline{S}_H$ / $\overline{S}_L$ are LOW.

Write Cycle No. 4 ($\overline{E}$ Controlled)

$\overline{G}$ is LOW. DQ lines may transition to Low-Z if the falling edge of $\overline{W}$ occurs after the falling edges of $\overline{E}$ and $\overline{S}_H/\overline{S}_L$.

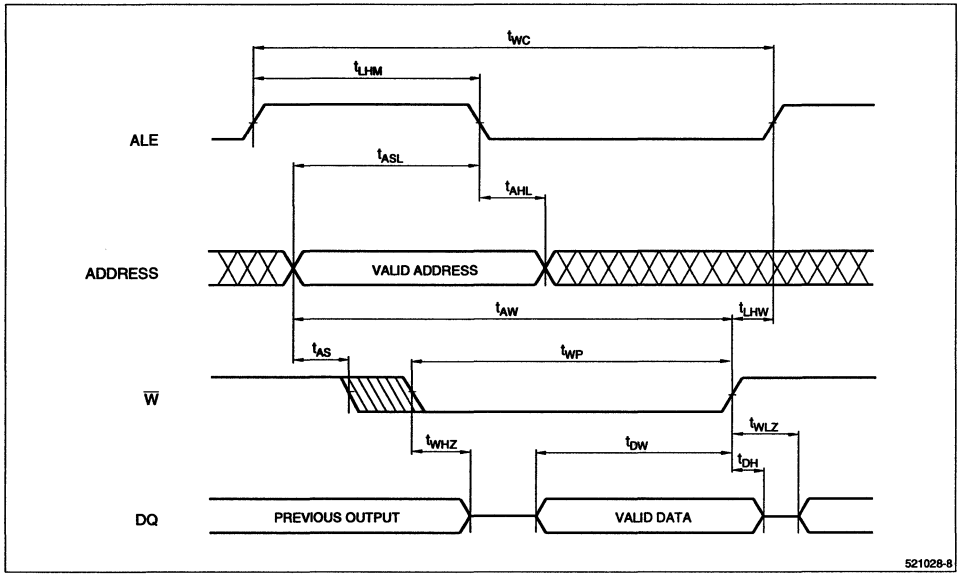


Figure 10. Write Cycle No. 3

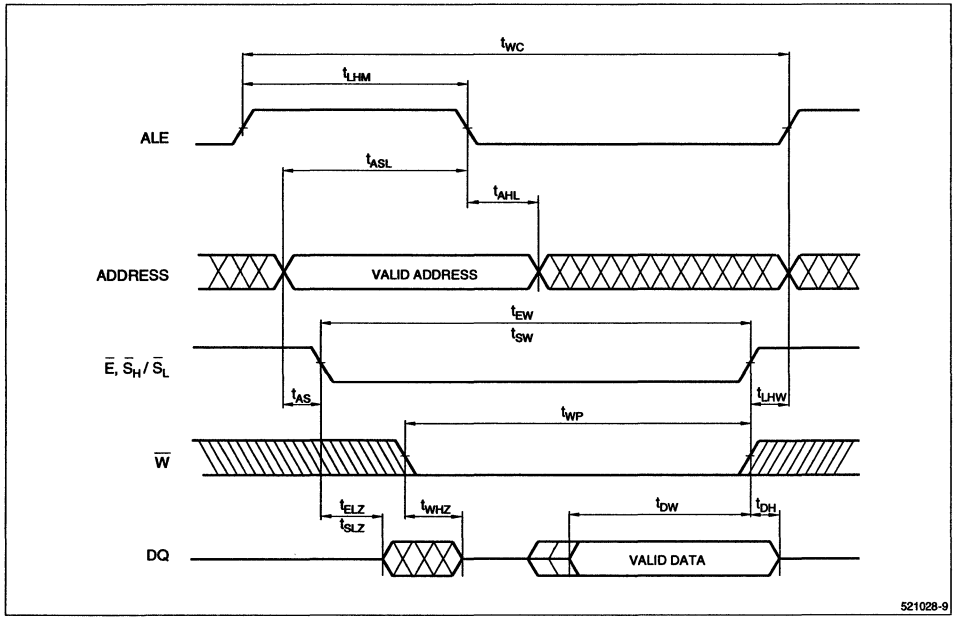


Figure 11. Write Cycle No. 4

BYTE OPERATIONS

Byte Read Description (Figure 12)

To read individual bytes, the device must be enabled ($\overline{E}$ is LOW), $\overline{W}$ must be HIGH, the outputs must be enabled ($\overline{G}$ is LOW) and the addresses must be either stable or latched with ALE. Figure 12 is one example of the byte read capabilities of this device. The example shows two read operations. The first is a read of the high byte of the current memory location and the second is a read of the low byte of the memory location.

(1) At the beginning of the cycle both $\overline{S}_L$ and $\overline{S}_H$ are HIGH.

(2) $\overline{S}_H$ goes LOW initiating a Read on the upper byte $DQ_{H(9\text{-}17)}$. $\overline{S}_L$ remains HIGH keeping the lower byte $DQ_{L(0\text{-}8)}$ disabled and in a high-impedance mode.

(3) $\overline{S}_L$ goes LOW activating $DQ_{L(0\text{-}8)}$. Valid data is available in t_{SA} following $\overline{S}_L$ going LOW.

(4) When $\overline{S}_H$ goes HIGH, $DQ_{H(9\text{-}17)}$ remains valid for t_{SHZ} before returning to a high-impedance condition.

(5) Finally, the Read for the lower byte is terminated by deasserting $\overline{S}_L$ (HIGH). $DQ_{L(0\text{-}8)}$ remains active for t_{SHZ} following $\overline{S}_L$ going HIGH.

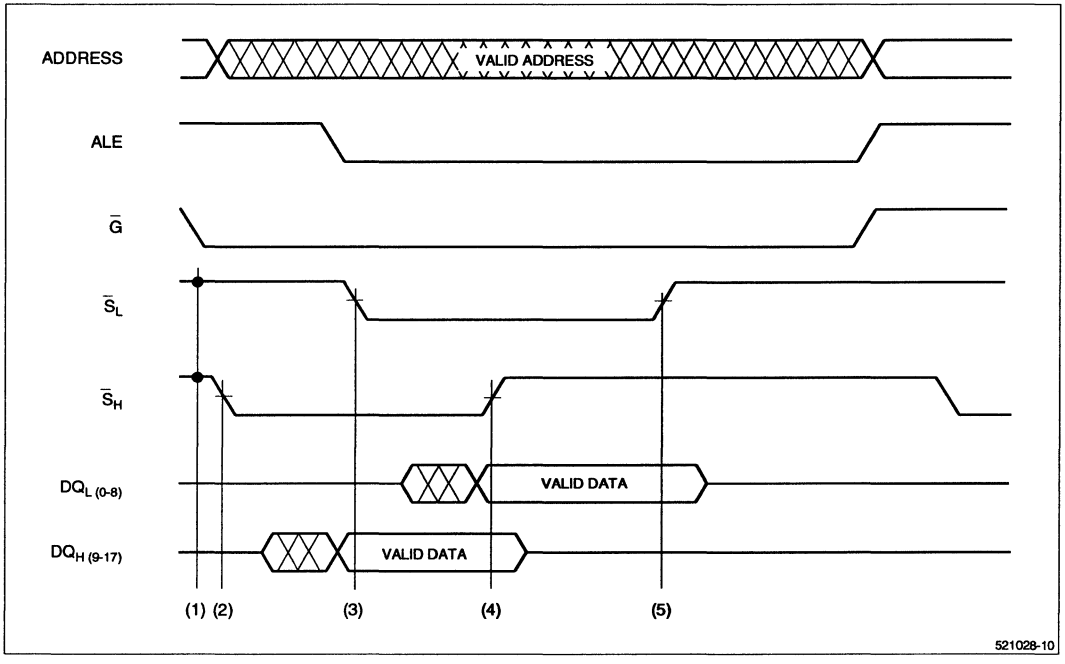


Figure 12. Byte Read ($\overline{E}$ is LOW and $\overline{W}$ is HIGH)

BYTE OPERATIONS (cont'd)

Byte Write Description (Figure 13)

To do individual byte-write operations, the device must be enabled ($\overline{E}$ is LOW, $\overline{G}$ is don't care) and addresses must be either stable or latched. Figure 13 is one example of the byte-write capabilities of this device. The diagram shows two write operations with unlatched addresses. The first is a write to the low byte of memory location N and the second is a write to the high byte of memory location M.

(1) $\overline{W}$ goes LOW while $\overline{S}_L$ and $\overline{S}_H$ remain HIGH.

(2) $\overline{S}_L$ goes LOW initiating a Write into the lower byte $DQ_{L(0-8)}$ of memory location N. $\overline{S}_H$ remains HIGH preventing a Write into the upper byte $DQ_{L(9-17)}$ of memory location N.

(3) $\overline{S}_L$ now goes HIGH terminating the Write operation on the lower byte of memory location N.

(4) Address N is changed to M.

(5) The Write operation is now initiated on the upper byte $DQ_{H(9-17)}$ by bringing $\overline{S}_H$ LOW. $\overline{S}_L$ remains HIGH preventing a Write operation from occurring in the lower byte $DQ_{L(0-8)}$ of memory location N+ 1.

(6) $\overline{S}_H$ now goes HIGH terminating the Write operation on the upper byte of address M.

(7) $\overline{W}$ goes HIGH, ending the Write operation.

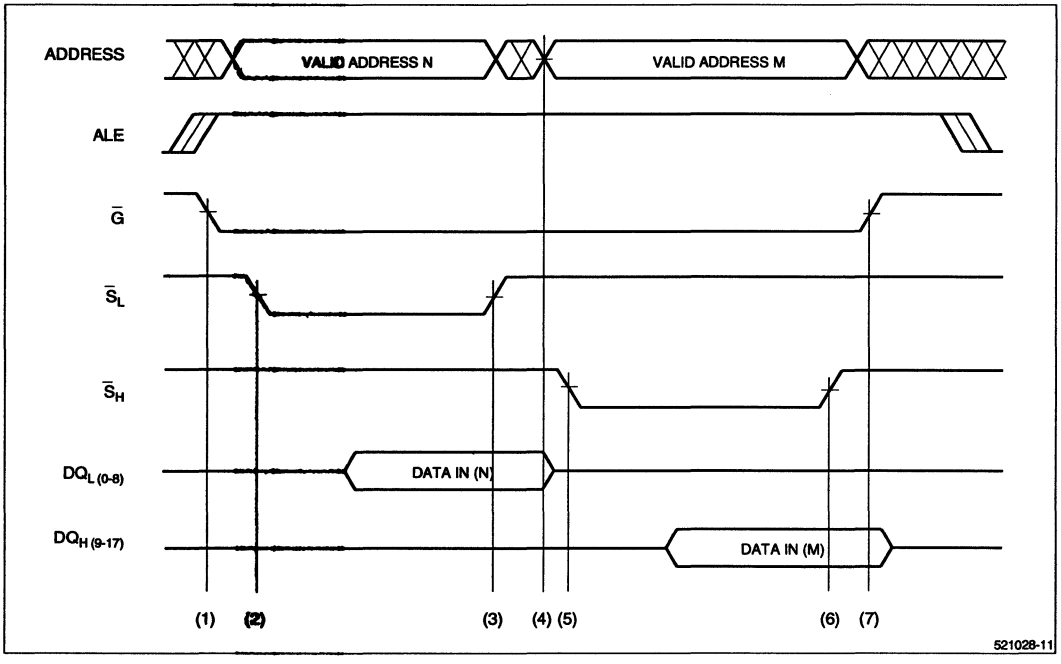
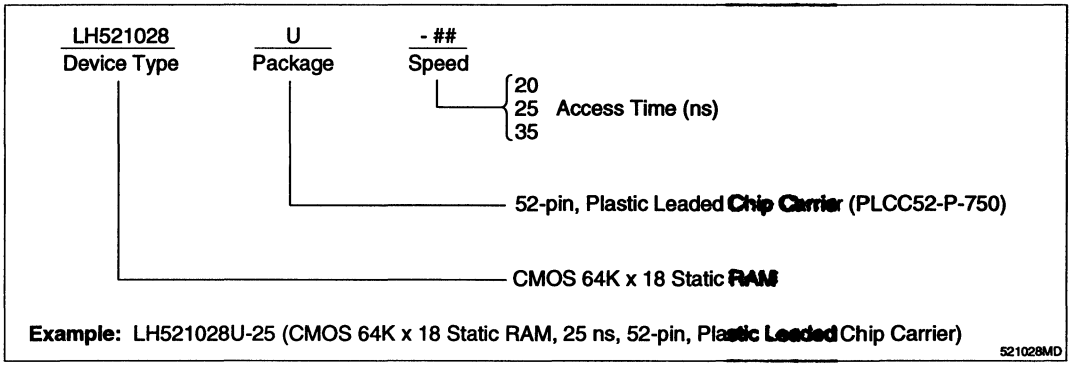


Figure 13. Byte Write ($\overline{E}$ is LOW)

ORDERING INFORMATION



Example: LH521028U-25 (CMOS 64K x 18 Static RAM, 25 ns, 52-pin, Plastic Leaded Chip Carrier)

521028MD

LH52V1036B2

ADVANCE INFORMATION

32K × 36 Synchronous SRAM

+3.3 V Supply With Clocked, Registered Inputs and Burst Counter

FEATURES

- Fast Access Times: 9, 10, 12, and 17 ns
- Fast $\overline{OE}$: 5, 6, and 7 ns
- Single +3.3 V ±5% Power Supply
- 5 V-Tolerant I/O
- Common Data Inputs and Data Outputs
- Individual BYTE WRITE Control
- Three Chip Enables for Simple Depth Expansion
- Clock Controlled, Registered, Address, Data and Control
- Internally Self-Timed WRITE Cycle
- Burst Control Pins (486/Pentium™ Burst Sequence)
- 100-Lead TQFP Package for High Density, High Speed
- Low Capacitive Bus Loading
- High 30 pF Output Drive Capability at Rated Access Time
- Parity Disable Function for 32-Bit Operation
- Timing
  - 9 ns Access/15 ns Cycle
  - 10 ns Access/15 ns Cycle
  - 12 ns Access/20 ns Cycle
  - 17 ns Access/25 ns Cycle
- Package: 100-pin TQFP

FUNCTIONAL DESCRIPTION

The Sharp Synchronous SRAM family employs high-speed, low-power CMOS designs using a thin-film transistor memory cell. Sharp SRAMs are fabricated using double-layer metal, three-layer polysilicon technology.

The LH52V1036B2 SRAM integrates a 32K × 36 SRAM core with advanced synchronous peripheral circuitry and a 2-bit burst counter. All synchronous inputs pass through registers controlled by a positive-edge-triggered single clock input (CLK). The synchronous inputs include all addresses, all data inputs, active LOW chip enable ($\overline{CE}$), two additional chip enables for easy depth expansion ($\overline{CE_2}$, CE_2), burst control inputs ($\overline{ADSC}$, $\overline{ADSP}$, $\overline{ADV}$) and byte write enables ($\overline{BW_1}$, $\overline{BW_2}$, $\overline{BW_3}$, $\overline{BW_4}$).

Asynchronous inputs include the output enable ($\overline{OE}$) and the clock (CLK). The Data-out (Q), enabled by $\overline{OE}$, is also asynchronous. WRITE cycles can be from one to four bytes wide as controlled by the byte write enables.

Burst operation can be initiated with either address status processor ($\overline{ADSP}$) or address status controller ($\overline{ADSC}$) input pins. Subsequent burst addresses can be internally generated as controlled by the burst advance pin ($\overline{ADV}$).

Address and write control are registered on-chip to simplify WRITE cycles. This allows self-timed WRITE cycles. Individual byte enables allow individual bytes to be written. $\overline{BW_1}$ controls DQ_1-DQ_8 and DQP_1, $\overline{BW_2}$ controls DQ_9-DQ_{16} and DQP_2, $\overline{BW_3}$ controls DQ_{17}-DQ_{24} and DQP_3, and $\overline{BW_4}$ controls DQ_{25}-DQ_{32} and DQP_4.

The LH52V1036B2 operates from a +3.3 V power supply and all inputs and outputs are TTL compatible. The device is ideally suited for 486 and Pentium (P5) systems and those systems which benefit from a very wide data bus. The device is also ideal in 32, 64 and 72-bit wide applications.

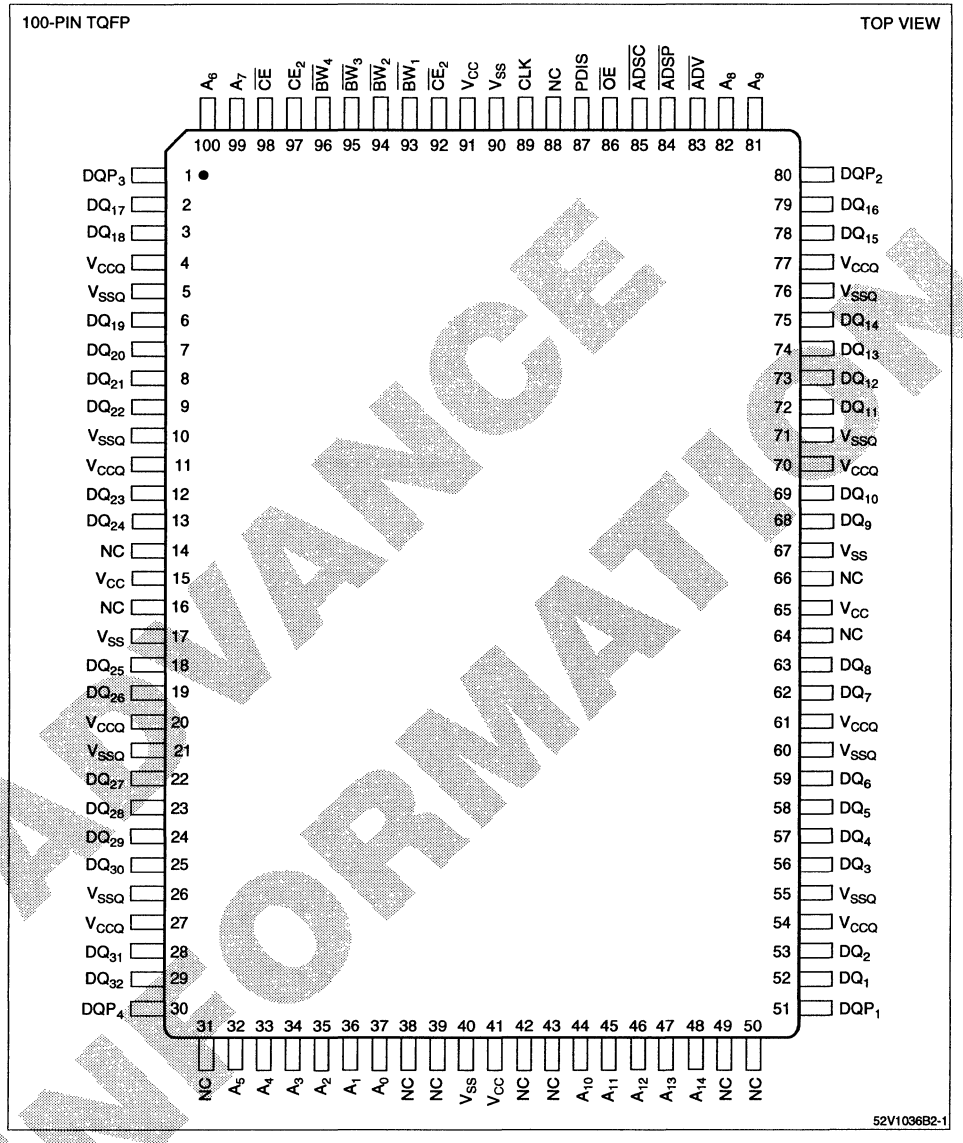


Figure 1. Pin Connections for TQFP Package

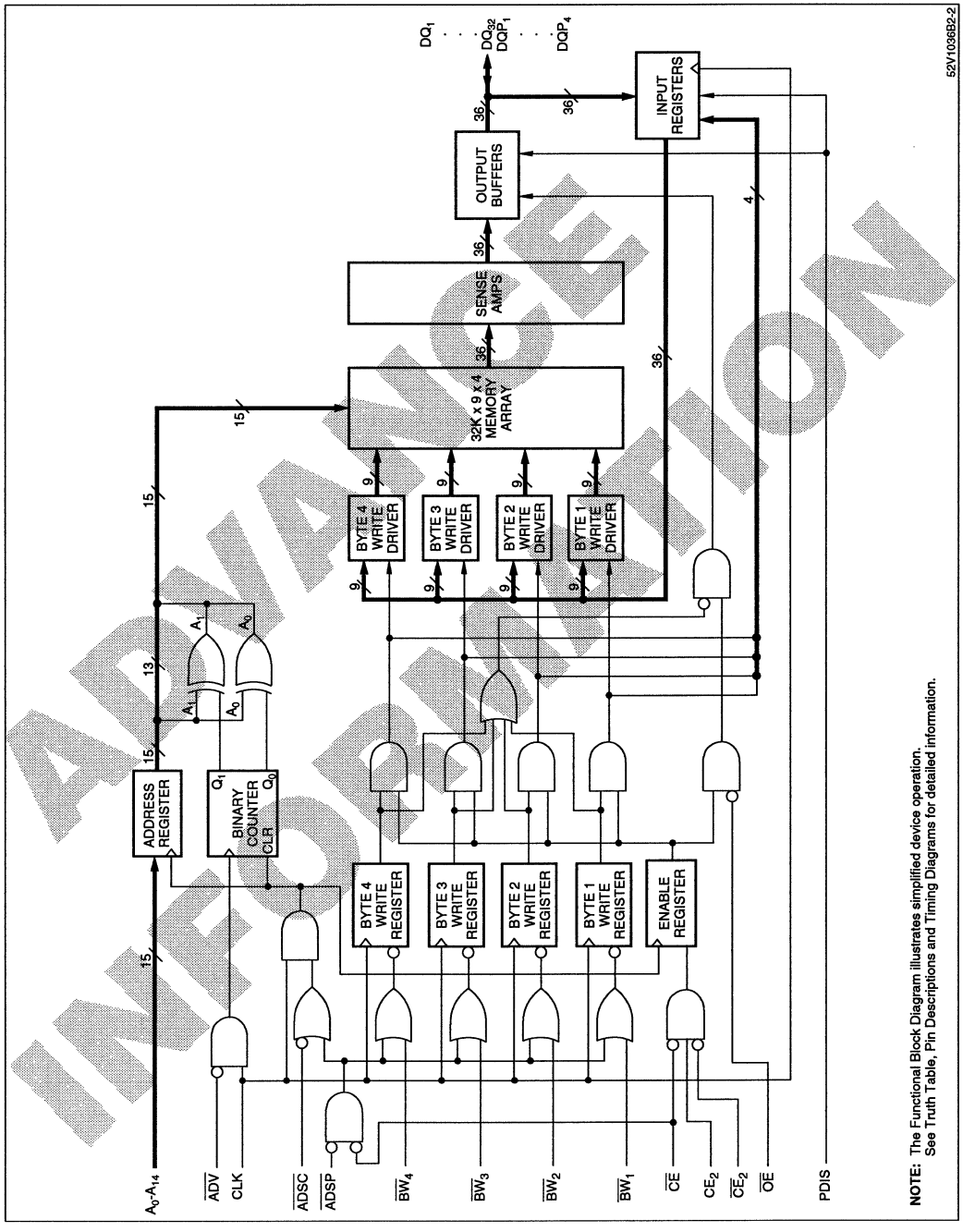


Figure 2. LH52V1036B2 Block Diagram

PIN DESCRIPTIONS

TQFP PIN NUMBER(S)	SYMBOL	TYPE	DESCRIPTION
37, 36, 35, 34, 33, 32, 100, 99, 82, 81, 44, 45, 46, 47, 48	A_0-A_{14}	Input	Synchronous Address Inputs: These inputs are registered and must meet the setup and hold times around the rising edge of CLK.
93, 94, 95, 96	$\overline{BW}_1$, $\overline{BW}_2$, $\overline{BW}_3$, $\overline{BW}_4$	Input	Synchronous Byte Write Enables: These active LOW inputs allow individual bytes to be written and must meet the setup and hold times around the rising edge of CLK. A BYTE WRITE enable is LOW for a WRITE cycle and HIGH for a READ cycle. $\overline{BW}_1$ controls DQ_1-DQ_8 and DQP_1. $\overline{BW}_2$ controls DQ_9-DQ_{16} and DQP_2. $\overline{BW}_3$ controls DQ_{17}-DQ_{24} and DQP_3. $\overline{BW}_4$ controls DQ_{25}-DQ_{32} and DQP_4. Data I/O are tristated if any of these four inputs are LOW.
89	CLK	Input	Clock: This signal latches the address, data, chip enables, byte write enables and burst control inputs on its rising edge. All synchronous inputs must meet setup and hold times around the clock's rising edge.
98	$\overline{CE}$	Input	Synchronous Chip Enable: This active LOW input is used to enable the device and conditions internal use of $\overline{ADSP}$. This input is sampled only when a new external address is loaded.
92	$\overline{CE}_2$	Input	Synchronous Chip Enable: This active LOW input is used to enable the device. This input is sampled only when a new external address is loaded. This input can be used for memory depth expansion.
97	CE_2	Input	Synchronous Chip Enable: This active HIGH input is used to enable the device. This input is sampled only when a new external address is loaded. This input can be used for memory depth expansion.
86	$\overline{OE}$	Input	Output Enable: This active LOW asynchronous input enables the data I/O output drivers.
83	$\overline{ADV}$	Input	Synchronous Address Advance: This active LOW input is used to advance the internal burst counter, controlling burst access after the external address is loaded. A HIGH on this pin effectively causes wait states to be generated (no address advance). This pin must be HIGH at the rising edge of the first clock after an $\overline{ADSP}$ cycle is initiated if a WRITE cycle is desired (to ensure use of correct address).
84	$\overline{ADSP}$	Input	Synchronous Address Status Processor: This active LOW input interrupts any ongoing burst, causing a new external address to be latched. A READ is performed using the new address, independent of the byte write enables and $\overline{ADSC}$ but dependent upon CE_2 and $\overline{CE}_2$. $\overline{ADSP}$ is ignored if $\overline{CE}$ is HIGH. Power-down state is entered if CE_2 is LOW or $\overline{CE}_2$ is HIGH.
85	$\overline{ADSC}$	Input	Synchronous Address Status Controller. This active LOW input interrupts any ongoing burst and causes a new external address to be latched. A READ or WRITE is performed using the new address if all chip enables are active. Power-down state is entered if one or more chip enables are inactive.

PIN DESCRIPTIONS (cont'd)

TQFP PIN NUMBER(S)	SYMBOL	TYPE	DESCRIPTION
14, 16, 31, 38, 39, 42, 43, 49, 50, 64, 66, 88	NC	–	No Connect: These signals are not internally connected.
52, 53, 56, 57, 58, 59, 62, 63, 68, 69, 72, 73, 74, 75, 78, 79, 2, 3, 6, 7, 8, 9, 12, 13, 18, 19, 22, 23, 24, 25, 28, 29	DQ_1-DQ_{32}	Input/Output	SRAM Data I/O: Byte 1 is DQ_1-DQ_8; Byte 2 is DQ_9-DQ_{16}; Byte 3 is DQ_{17}-DQ_{24}; Byte 4 is DQ_{25}-DQ_{32}. Input data must meet setup and hold times around the rising edge of CLK.
51, 80, 1, 30	DQP_1-DQP_4	Input/Output	Parity Data I/O: Byte 1 Parity is DQP_1; Byte 2 Parity is DQP_2; Byte 3 Parity is DQP_3; Byte 4 Parity is DQP_4.
87	PDIS	Input	Parity Disable: When HIGH, this input disables DQP_1 through DQP_4 for 32-bit data bus width. A LOW on PDIS enables control of DQP_1 through DQP_4 in the same manner as DQ_1-DQ_{32} are controlled.
15, 41, 65, 91	V_{CC}	Supply	Power Supply: +3.3 V ±5%
17, 40, 67, 90	V_{SS}	Supply	Ground: GND
4, 11, 20, 27, 54, 61, 70, 77	$V_{CC}Q$	Supply	Isolated Output Buffer Supply: +3.3 V ±5%

BURST SEQUENCE TABLE

OPERATION	ADDRESS USED		
	A_{14}-A_2	A_1	A_0
First access, latch external address	A_{14}-A_2	A_1	A_0
Second access (first burst address)	Latched A_{14}-A_2	Latched A_1	Latched $\overline{A}_0$
Third access (second burst address)	Latched A_{14}-A_2	Latched $\overline{A}_1$	Latched A_0
Fourth access (third burst address)	Latched A_{14}-A_2	Latched $\overline{A}_1$	Latched $\overline{A}_0$

NOTE:
The burst sequence wraps around to its initial state upon completion.

BURST ADDRESS TABLE

FIRST ADDRESS	SECOND ADDRESS	THIRD ADDRESS	FOURTH ADDRESS
X . . . X00	X . . . X01	X . . . X10	X . . . X11
X . . . X01	X . . . X00	X . . . X11	X . . . X10
X . . . X10	X . . . X11	X . . . X00	X . . . X01
X . . . X11	X . . . X10	X . . . X01	X . . . X00

TRUTH TABLE

OPERATION	ADDRESS USED	$\overline{CE}$	$\overline{CE_2}$	CE_2	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{WRITE}$	$\overline{OE}$	CLK	DQ
Deselected Cycle, Power-down	None	H	X	X	X	L	X	X	X	L-H	High-Z
Deselected Cycle, Power-down	None	L	X	L	L	X	X	X	X	L-H	High-Z
Deselected Cycle, Power-down	None	L	H	X	L	X	X	X	X	L-H	High-Z
Deselected Cycle, Power-down	None	L	X	L	H	L	X	X	X	L-H	High-Z
Deselected Cycle, Power-down	None	L	H	X	H	L	X	X	X	L-H	High-Z
READ Cycle, Begin Burst	External	L	L	H	L	X	X	X	L	L-H	Q
READ Cycle, Begin Burst	External	L	L	H	L	X	X	X	H	L-H	High-Z
WRITE Cycle, Begin Burst	External	L	L	H	H	L	X	L	X	L-H	D
READ Cycle, Begin Burst	External	L	L	H	H	L	X	H	L	L-H	Q
READ Cycle, Begin Burst	External	L	L	H	H	L	X	H	H	L-H	High-Z
READ Cycle, Continue Burst	Next	X	X	X	H	H	L	H	L	L-H	Q
READ Cycle, Continue Burst	Next	X	X	X	H	H	L	H	H	L-H	High-Z
READ Cycle, Continue Burst	Next	H	X	X	X	H	L	H	L	L-H	Q
READ Cycle, Continue Burst	Next	H	X	X	X	H	L	H	H	L-H	High-Z
WRITE Cycle, Continue Burst	Next	X	X	X	H	H	L	L	X	L-H	D
WRITE Cycle, Continue Burst	Next	H	X	X	X	H	L	L	X	L-H	D
READ Cycle, Suspend Burst	Current	X	X	X	H	H	H	H	L	L-H	Q
READ Cycle, Suspend Burst	Current	X	X	X	H	H	H	H	H	L-H	High-Z
READ Cycle, Suspend Burst	Current	H	X	X	X	H	H	H	L	L-H	Q
READ Cycle, Suspend Burst	Current	H	X	X	X	H	H	H	H	L-H	High-Z
WRITE Cycle, Suspend Burst	Current	X	X	X	H	H	H	L	X	L-H	D
WRITE Cycle, Suspend Burst	Current	H	X	X	X	H	H	L	X	L-H	D

NOTES:

1. X means 'don't care.' H means logic HIGH. L means logic LOW. $\overline{WRITE}$ = L means any one or more byte write enable signals ($\overline{BW_1}$, $\overline{BW_2}$, $\overline{BW_3}$ or $\overline{BW_4}$) are LOW. $\overline{WRITE}$ = H means all byte write enable signals are HIGH.
2. $\overline{BW_1}$ enables writes to Byte 1 (DQ_1-DQ_8, DQP_1). $\overline{BW_2}$ enables writes to Byte 2 (DQ_9-DQ_{16}, DQP_2). $\overline{BW_3}$ enables writes to Byte 3 (DQ_{17}-DQ_{24}, DQP_3). $\overline{BW_4}$ enables writes to Byte 4 (DQ_{25}-DQ_{32}, DQP_4).
3. All inputs except $\overline{OE}$ must meet setup and hold times around the rising edge (LOW to HIGH) of CLK.
4. Wait states are inserted by suspending burst.
5. For a write operation following a read operation, $\overline{OE}$ must be HIGH before the input data required setup time and held HIGH throughout the input data hold time.
6. This is device contains circuitry that will ensure the outputs will be in High-Z during power-up.
7. PDIS disables the DQP lines when HIGH and enables the DQP lines when LOW.
8. $\overline{ADSP}$ LOW always initiates an internal READ at the L-H edge of CLK. A WRITE is performed by setting one or more byte write enable signals LOW for the subsequent L-H edge of CLK. Refer to WRITE timing diagram for clarification.

ABSOLUTE MAXIMUM RATINGS [1]

PARAMETER	RATING
Voltage on V_{CC} Supply Relative to V_{SS}	–0.5 V to +4.6 V
V_{IN}	–0.5 V to V_{CC} + 0.5 V
Storage Temperature (Plastic)	–55°C to +150°C
Junction Temperature	+150°C
Power Dissipation	1.6 W
Short Circuit Output Current	100 mA

NOTE:

1. Stresses greater than those listed under 'Absolute Maximum Ratings' may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS
($0°C \le T_A \le 70°C$; $T_C \le 110°C$; $V_{CC} = 3.3\ V \pm 5\%$ unless otherwise noted)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.0	V_{CC} + 0.5 V	V	1, 2
Input Low (Logic 0) Voltage		V_{IL}	–0.3	0.8	V	1, 2
Input Leakage Current	$0\ V \le V_{IN} \le V_{CC}$	I_{LI}	–1	1	µA	
Output Leakage Current	Output(s) Disabled, $0\ V \le V_{OUT} \le V_{CC}$	I_{LO}	–1	1	µA	
Output High Voltage	$I_{OH} = -4.0$ mA	V_{OH}	2.4		V	1
Output Low Voltage	$I_{OL} = 8.0$ mA	V_{OL}		0.4	V	1
Supply Voltage		V_{CC}	3.1	3.5	V	1

NOTES:

1. All voltages referenced to V_{SS} (GND).
2. Overshoot: $V_{IH} \le V_{CC} + 2.0$ V for $t \le t_{KC}/2$. Undershoot: $V_{IL} \ge -2.0$ V for $t \le t_{KC}/2$. Power-up: $V_{IH} \le V_{CC} + 2.0$ V and $V_{CC} \le 3.1$ V for $t \le 200$ msec.

RECOMMENDED DC OPERATING CONDITIONS
($0°C \le T_A \le 70°C$; $T_C \le 110°C$; $V_{CC} = 3.3\ V \pm 5\%$ unless otherwise noted)

DESCRIPTION	CONDITIONS	SYMBOL	TYPICAL	MAX.				UNITS	NOTES
				–9	–10	–12	–17		
Power Supply Current: Operating	Device Selected; all inputs ≤ V_{IL} or ≥ V_{IH}; cycle time ≥ t_{KC} min; V_{CC} = MAX; outputs open	I_{CC}	170	250	250	210	180	mA	1, 2, 3
Power Supply Current: Idle	Device Selected; $\overline{ADSC}$, $\overline{ADSP}$, $\overline{ADV}$ ≥ V_{IH}; all inputs ≤ V_{IL} or ≥ V_{IH}; V_{CC} = MAX; cycle time ≥ t_{KC} min	I_{SB1}	55	85	85	70	60	mA	2, 3
CMOS Standby	Device Deselected; V_{CC} = MAX; all inputs ≤ V_{SS} +0.2 or ≥ V_{CC} –0.2; all inputs static; CLK frequency = 0	I_{SB2}	0.2	2	2	2	2	mA	2, 3
TTL Standby	Device Deselected; all inputs ≤ V_{IL} or ≥ V_{IH}; all inputs static; V_{CC} = MAX; CLK frequency = 0	I_{SB3}	10	18	18	18	18	mA	2, 3
Clock Running	Device Deselected; all inputs ≤ V_{IL} or ≥ V_{IH}; V_{CC} = MAX; CLK cycle time ≥ t_{KC} min	I_{SB4}	20	35	35	30	25	mA	2, 3

NOTES:

1. I_{CC} is given with no output current. I_{CC} increases with greater output loading and faster cycle times.
2. 'Device Deselected' means device is in POWER-DOWN mode as defined in the truth table. 'Device Selected' means device is active (not in POWER-DOWN mode).
3. Typical values are measured at 3.3 V, 25°C and 20 ns cycle time.

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	TYP	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1 MHz V_{CC} = 3.3 V	C_I	3	4	pF	1
Input/Output Capacitance (DQ)		C_O	5	6	pF	1

NOTE:

1. This parameter is sampled.

THERMAL CONSIDERATIONS

DESCRIPTION	CONDITIONS	SYMBOL	TYP	UNITS	NOTES
Thermal Resistance – Junction to Ambient	Still Air	θ_{JA}	65	°C/W	
Thermal Resistance – Junction to Case		θ_{JC}	6	°C/W	
Maximum Case Temperature		TC	110	°C	1

NOTE:

1. Sharp does not warrant the functionality or reliability of any product in which the case temperature exceeds 110°C. Care should be taken to limit case temperature to acceptable levels.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS [1]
(0°C ≤ T_A ≤ 70°C; V_{CC} = 3.3 V ±5%)

DESCRIPTION	SYMBOL	-9		-10		-12		-17		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
CLOCK											
Clock Cycle Time	t_{KC}	15		15		20		25		ns	
Clock HIGH Time	t_{KH}	4		5		6		8		ns	
Clock LOW Time	t_{KL}	4		5		6		8		ns	
OUTPUT TIMES											
Clock to Output Valid	t_{KQ}		9		10		12		17	ns	
Clock to Output Invalid	t_{KQX}	3		3		3		3		ns	
Clock to Output in Low-Z	t_{KQLZ}	5		5		6		6		ns	2, 3
Clock to Output in High-Z	t_{KQHZ}		5		5		6		6	ns	2, 3
$\overline{OE}$ to Output Valid	t_{OEQ}		5		5		6		7	ns	4
$\overline{OE}$ to Output in Low-Z	t_{OELZ}	0		0		0		0		ns	2, 3
$\overline{OE}$ to Output in High-Z	t_{OEHZ}		5		5		6		6	ns	2, 3
SETUP TIMES											
Address	t_{AS}	2.5		3		3		3		ns	5, 6
Address Status ($\overline{ADSC}$, $\overline{ADSP}$)	t_{ADSS}	2.5		3		3		3		ns	5, 6
Address Advance ($\overline{ADV}$)	t_{AAS}	2.5		3		3		3		ns	5, 6
Byte Write Enables ($\overline{BW_1}$, $\overline{BW_2}$, $\overline{BW_3}$, $\overline{BW_4}$)	t_{WS}	2.5		3		3		3		ns	5, 6
Data In	t_{DS}	2.5		3		3		3		ns	5, 6
Chip Enables ($\overline{CE}$, $\overline{CE_2}$, CE_2)	t_{CES}	2.5		3		3		3		ns	5, 6
HOLD TIMES											
Address	t_{AH}	0.5		0.5		0.5		0.5		ns	5, 6
Address Status ($\overline{ADSC}$, $\overline{ADSP}$)	t_{ADSH}	0.5		0.5		0.5		0.5		ns	5, 6
Address Advance ($\overline{ADV}$)	t_{AAH}	0.5		0.5		0.5		0.5		ns	5, 6
Byte Write Enables ($\overline{BW_1}$, $\overline{BW_2}$, $\overline{BW_3}$, $\overline{BW_4}$)	t_{WH}	0.5		0.5		0.5		0.5		ns	5, 6
Data In	t_{DH}	0.5		0.5		0.5		0.5		ns	5, 6
Chip Enables ($\overline{CE}$, $\overline{CE_2}$, CE_2)	t_{CEH}	0.5		0.5		0.5		0.5		ns	5, 6

NOTES:

1. Test conditions as specified with the output loading as shown in Figure 3 unless otherwise noted.
2. Output loading is specified with CL = 5 pF as in Figure 4. Transition is measured ±500 mV from steady state voltage.
3. At any given temperature and voltage condition, t_{KQHZ} is less than t_{KQLZ} and t_{OEHZ} is less than t_{OELZ}.
4. $\overline{OE}$ is a 'don't care' when a byte write enable is sampled LOW.
5. A READ cycle is defined by byte write enables all HIGH or $\overline{ADSP}$ LOW for the required setup and hold times. A WRITE cycle is defined by at least one byte write enable LOW and $\overline{ADSP}$ HIGH for the required setup and hold times.
6. This is a synchronous device. All addresses must meet the specified setup and hold times for all rising edges of CLK when either $\overline{ADSP}$ or $\overline{ADSC}$ is LOW and chip enabled. All other synchronous inputs must meet the setup and hold times with stable logic levels for all rising edges of clock (CLK) when chip is enabled. Chip enable must be valid at each rising edge of CLK (when either $\overline{ADSP}$ or $\overline{ADSC}$ is LOW) to remain enabled.

AC TEST CONDITIONS

PARAMETER	RATING
Input Pulse Levels	V_{SS} to 3.0 V
Input Rise and Fall Times	1.5 ns
Input Timing Reference Levels	1.5 V
Output Reference Levels	1.5 V
Output Load	See Figures 3 and 4

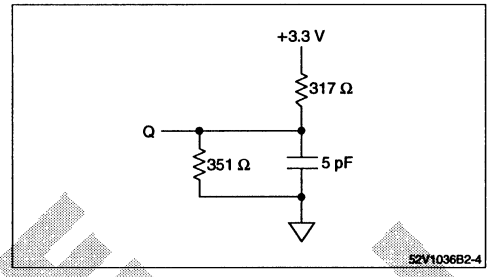


Figure 4. Output Load Equivalent

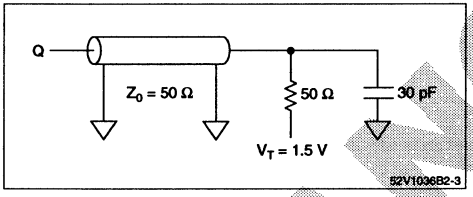
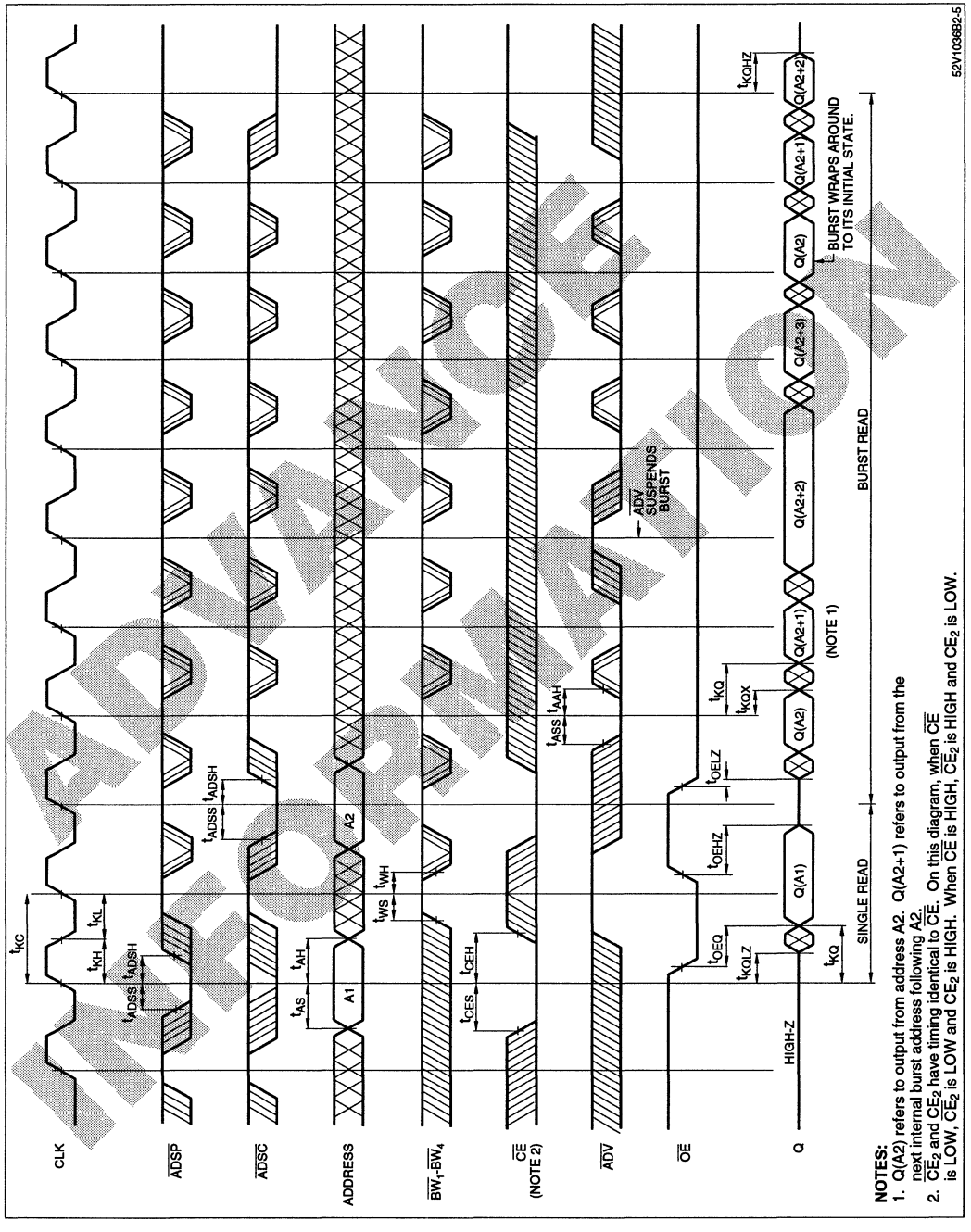


Figure 3. Output Load Equivalent



NOTES:
1. Q(A2) refers to output from address A2. Q(A2+1) refers to output from the next internal burst address following A2.
2. $\overline{CE}_2$ and $\overline{CE}_2$ have timing identical to $\overline{CE}$. On this diagram, when $\overline{CE}$ is LOW, $\overline{CE}_2$ is LOW and CE_2 is HIGH. When $\overline{CE}$ is HIGH, $\overline{CE}_2$ is HIGH and CE_2 is LOW.

Figure 5. Read Timing

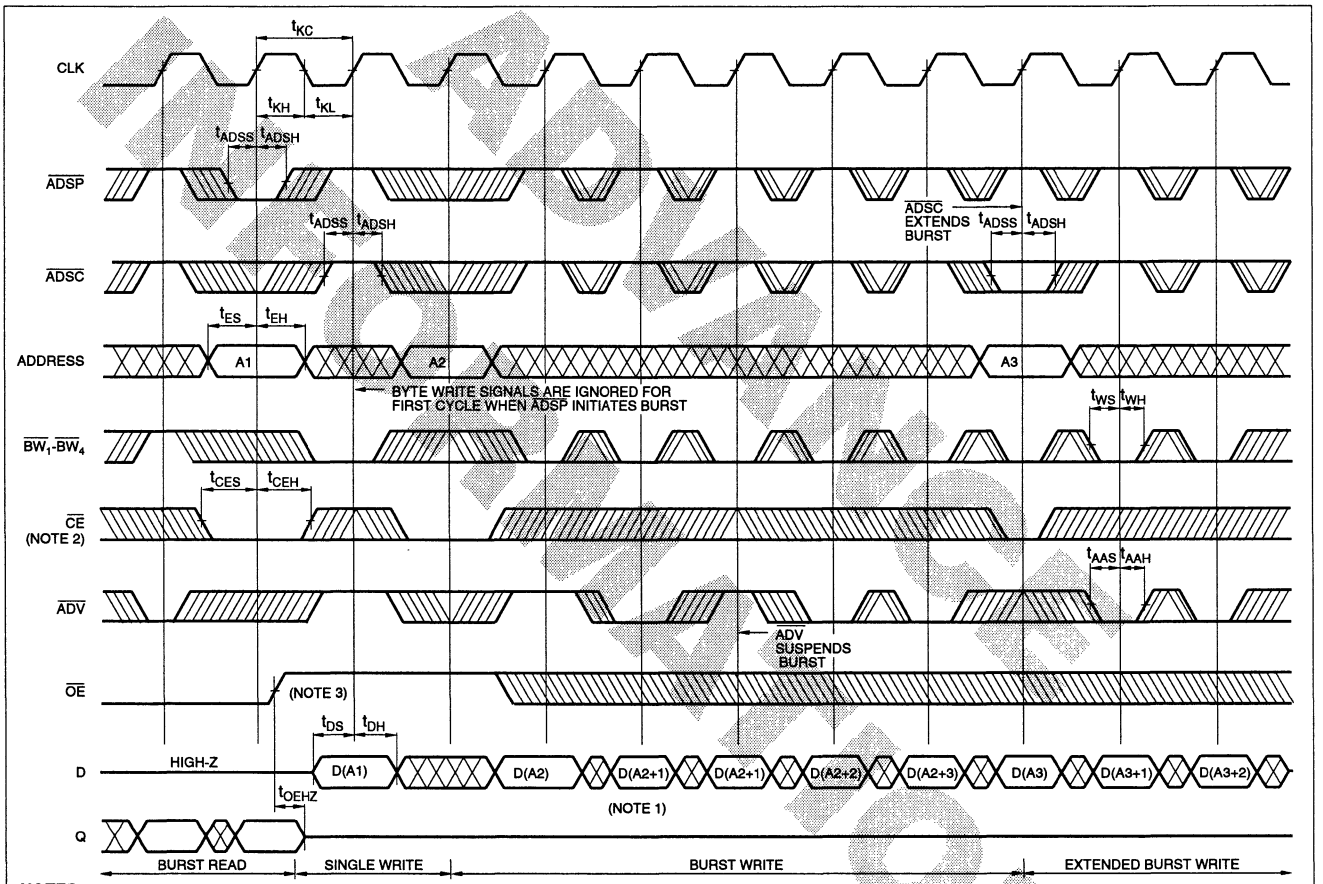
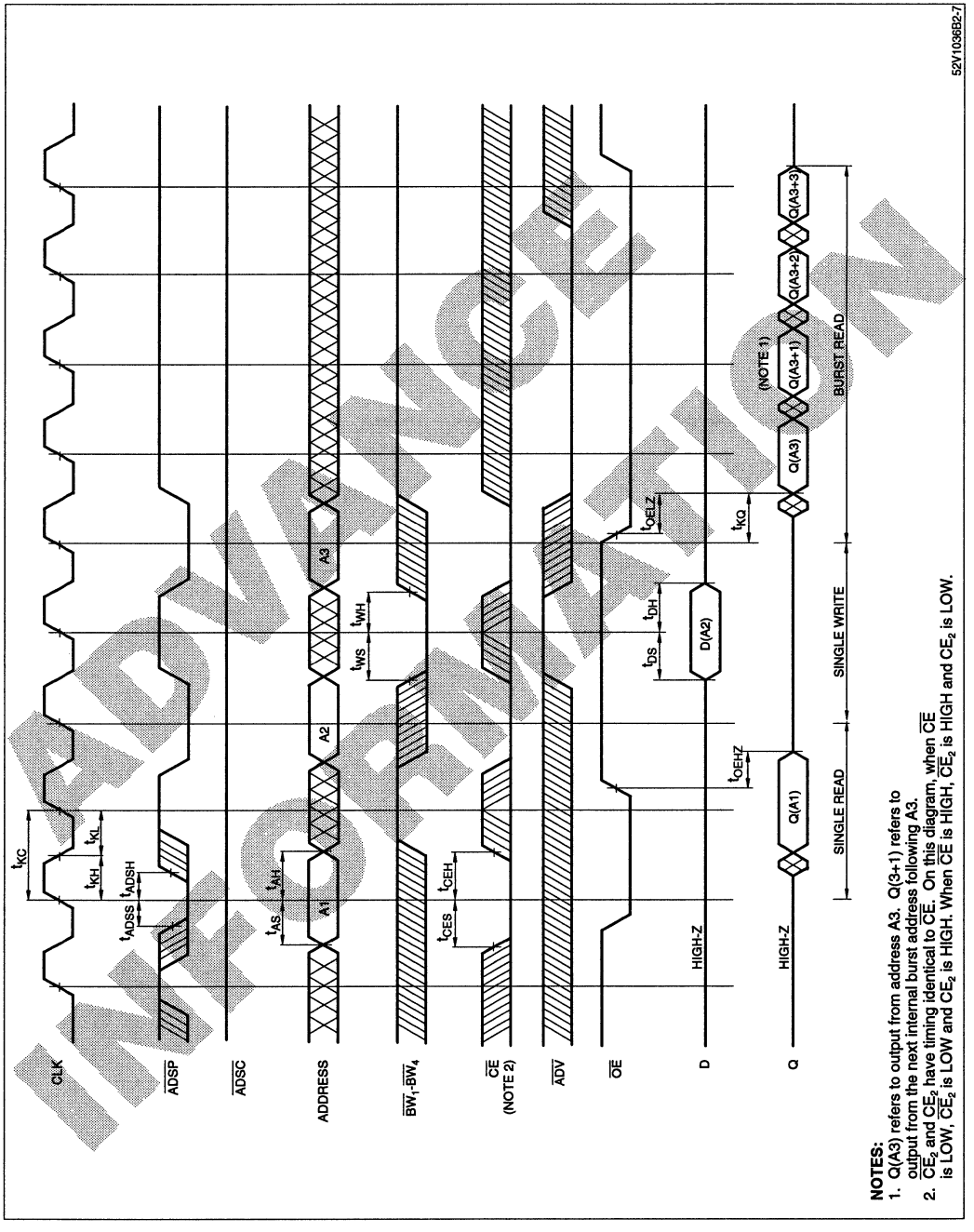


Figure 6. Write Timing

NOTES:

1. Q(A2) refers to output from address A2. Q(A2+1) refers to output from the next internal burst address following A2.
2. $\overline{CE}_2$ and CE_2 have timing identical to $\overline{CE}$. On this diagram, when $\overline{CE}$ is LOW, $\overline{CE}_2$ is LOW and CE_2 is HIGH. When $\overline{CE}$ is HIGH, $\overline{CE}_2$ is HIGH and CE_2 is LOW.
3. $\overline{OE}$ must be HIGH before the input data setup and held HIGH throughout the data hold time. This prevents input/output data contention for the time period prior to the byte write enable inputs being sampled.
4. $\overline{ADV}$ must be HIGH to permit a WRITE to the loaded address.

52V1036B2-6



NOTES:
1. Q(A3) refers to output from address A3. Q(3+1) refers to output from the next internal burst address following A3.
2. $\overline{CE}_2$ and $\overline{CE}_2$ have timing identical to $\overline{CE}$. On this diagram, when $\overline{CE}$ is LOW, $\overline{CE}_2$ is LOW and CE_2 is HIGH. When $\overline{CE}$ is HIGH, $\overline{CE}_2$ is HIGH and CE_2 is LOW.

Figure 7. Read/Write Timing

APPLICATION INFORMATION

32-Bit Wide Systems

The Sharp 32K × 36 Synchronous SRAM may be used in a 32-bit-wide system without the use of any external components by connecting PDIS to V_{CC}. This disables the output buffer on the data parity input/output lines (DQP_1, DQP_2, DQP_3 and DQP_4).

Load Derating Curves

The Sharp 32K × 36 Synchronous SRAM timing is dependent upon the capacitive loading on the outputs. The data sheet is written assuming a load of 30 pF. Access time changes with load capacitance as follows:

$\Delta t_{KQ} = 0.03$ ns/pF × ΔC_L pF

NOTE: this is preliminary information subject to change.

For example, if the SRAM loading is 22 pF, ΔC_L is −8 pF (8 pF less than rated load). The clock to valid output time of the SRAM is reduced by 0.03 × 8 = 0.24 ns. If the device is a 12 ns part, the worse case t_{KQ} becomes 11.76 ns.

Consult the factory for copies of I/O current versus voltage curves and SPICE models.

Depth Expansion

The Sharp 32K × 36 Synchronous SRAM incorporates two additional chip enables to facilitate simple depth expansion. This permits easy cache upgrades from 32K depth to 64K depth with no extra logic as shown in Figure 8.

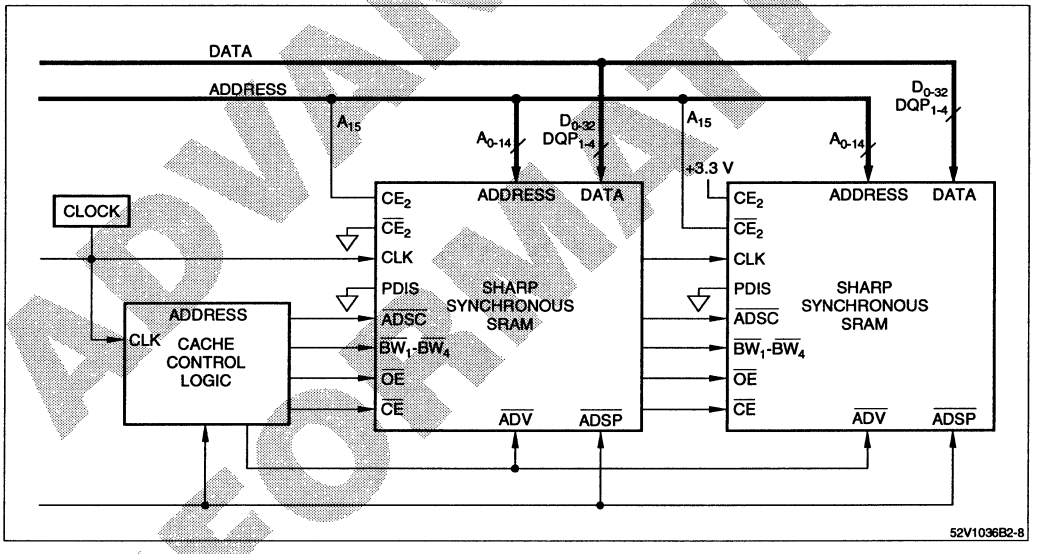


Figure 8. Depth Expansion From 32K x 36 to 64K x 36

APPLICATION EXAMPLES

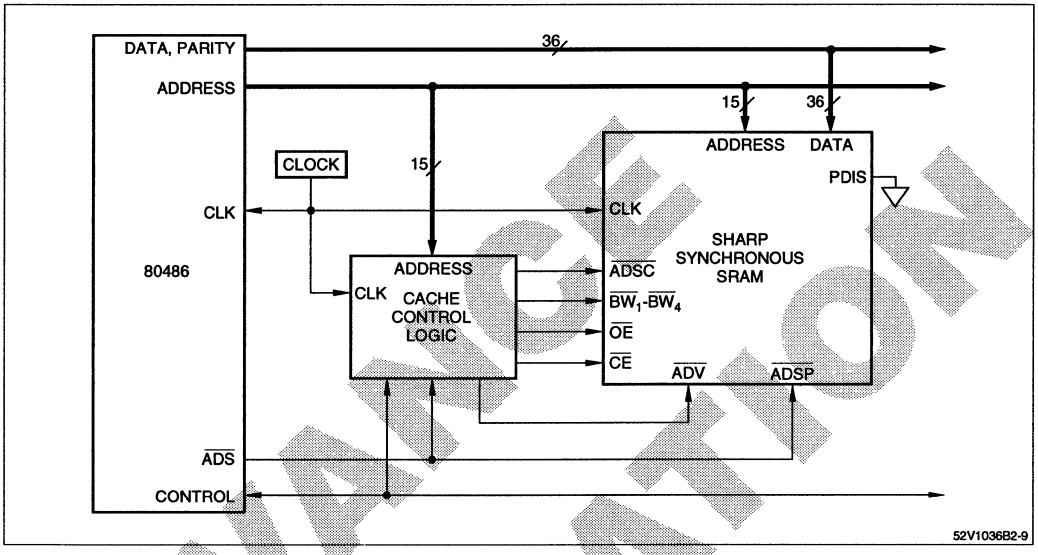


Figure 9. 128K Byte Secondary Cache With Parity and Burst for 50 MHz 80486 Using One LH52V1036B2-12 Synchronous SRAM

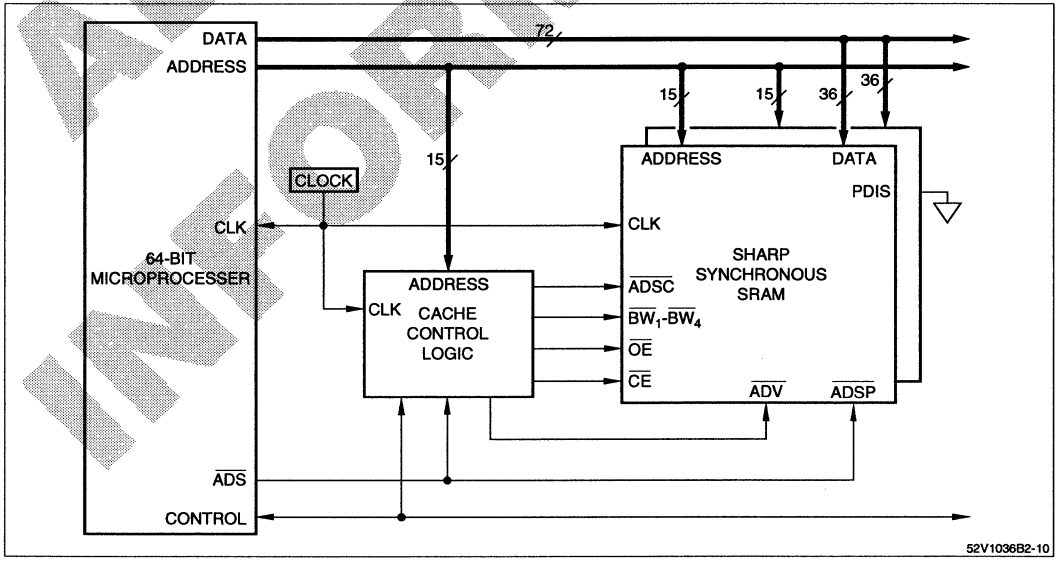
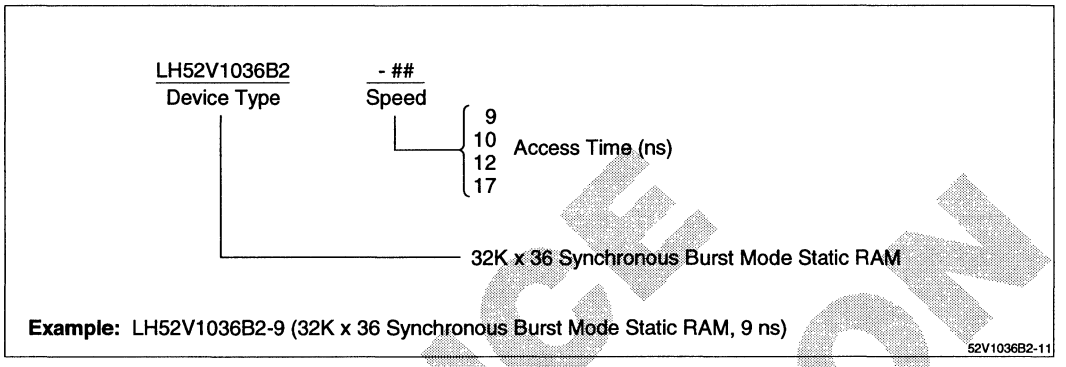


Figure 10. 256K Byte Secondary Cache With Parity and Burst for 66 MHz Pentium™ Using Two LH52V1036B2-9 Synchronous SRAMs

ORDERING INFORMATION



LH52V1036C4

ADVANCE INFORMATION

32K × 36 Synchronous SRAM

+3.3 V Supply, Fully Registered Inputs, Outputs, and Burst Counter

FEATURES

- Fast Access Times: 7, 10, 12, and 15 ns
- Fast $\overline{OE}$: 5, 6, 7, and 8 ns
- Single +3.3 V ±5% Power Supply
- 5 V-Tolerant I/O
- Common Data Inputs and Data Outputs
- Individual BYTE WRITE Control
- Three Chip Enables for Simple Depth Expansion
- Clock Controlled, Registered, Address, Data I/O and Control for Fully Pipelined Applications
- Internally Self-Timed WRITE Cycle
- WRITE Pass-Through Capability
- Burst Control Pins (486/Pentium™ Burst Sequence)
- 100-Lead TQFP Package for High Density, High Speed
- Low Capacitive Bus Loading
- High 30 pF Output Drive Capability at Rated Access Time
- Parity Disable Function for 32-Bit Operation
- Timing
  - 7 ns Access/15 ns Cycle
  - 10 ns Access/20 ns Cycle
  - 12 ns Access/25 ns Cycle
  - 15 ns Access/30 ns Cycle
- Package: 100-pin TQFP

FUNCTIONAL DESCRIPTION

The Sharp Synchronous SRAM family employs high-speed, low-power CMOS designs using a thin-film transistor memory cell. Sharp SRAMs are fabricated using double-layer metal, three-layer polysilicon technology.

The LH52V1036C4 SRAM integrates a 32K × 36 SRAM core with advanced synchronous peripheral circuitry, a 2-bit burst counter and output register. All synchronous inputs pass through registers controlled by a positive-edge-triggered single clock input (CLK). The synchronous inputs include all addresses, all data inputs, active LOW chip enable, two additional chip enables for easy depth expansion ($\overline{CE_2}$, CE_2), burst control inputs ($\overline{ADSC}$, $\overline{ADSP}$, $\overline{ADV}$) and the byte write enables ($\overline{BW_1}$, $\overline{BW_2}$, $\overline{BW_3}$, $\overline{BW_4}$).

Asynchronous inputs include the output enable ($\overline{OE}$) and the clock (CLK). The data-out (Q), enabled by $\overline{OE}$, is also asynchronous. The output register is controlled by the clock. WRITE cycles can be from one to four bytes wide as controlled by the byte write enables.

Burst operation can be initiated with either address status processor ($\overline{ADSP}$) or address status controller ($\overline{ADSC}$) input pins. Subsequent burst addresses can be internally generated as controlled by the burst advance pin ($\overline{ADV}$).

Address and write control are registered on-chip to simplify WRITE cycles. This allows self-timed WRITE cycles. Individual byte enables allow individual bytes to be written. WRITE pass-through makes written data immediately available at the output register during the READ cycle following a WRITE as controlled solely by $\overline{OE}$ to improve cache system response.

The LH52V1036C4 operates from a +3.3 V power supply and all inputs and outputs are TTL compatible. The device is ideal for Pentium (P5) pipelined applications and 32, 64 and 72-bit wide applications.

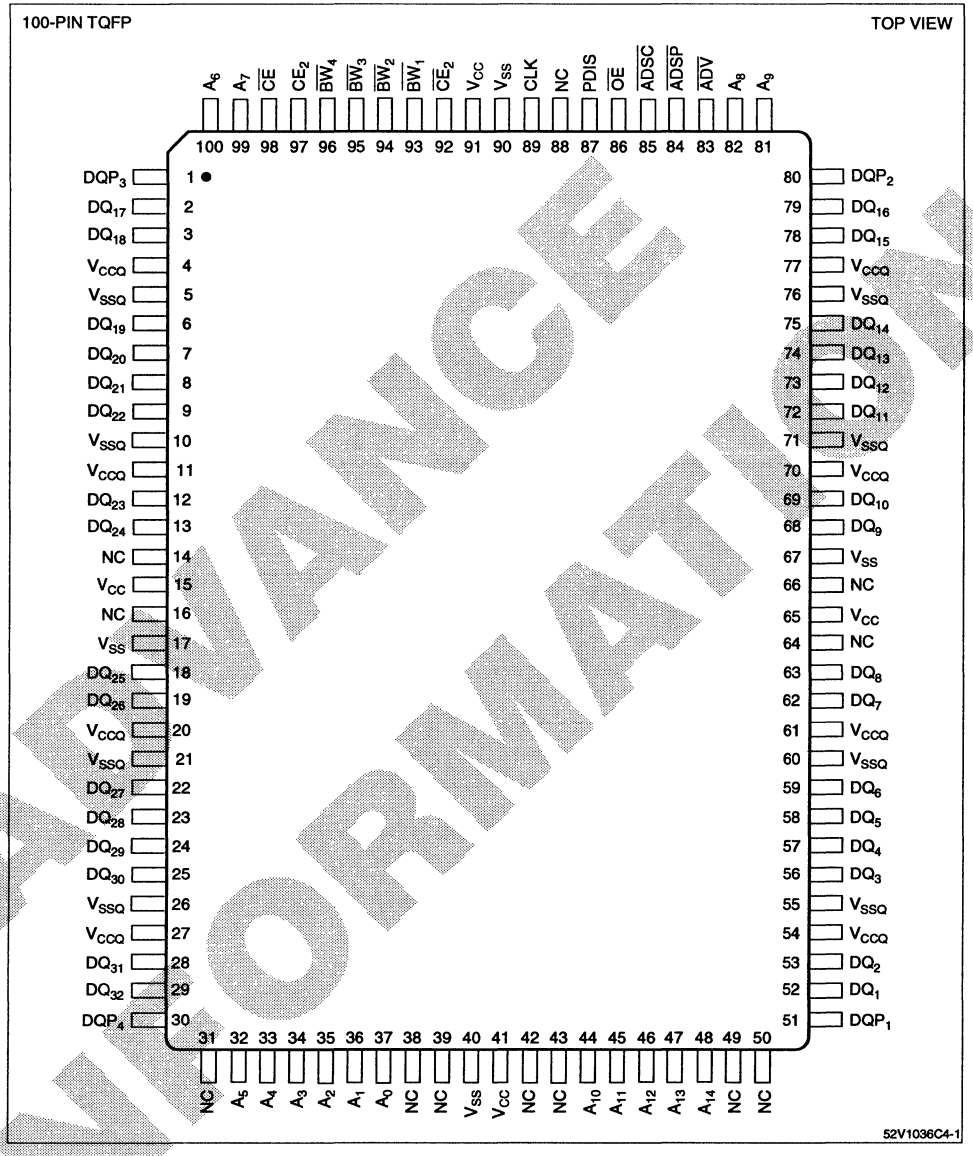


Figure 1. Pin Connections for TQFP Package

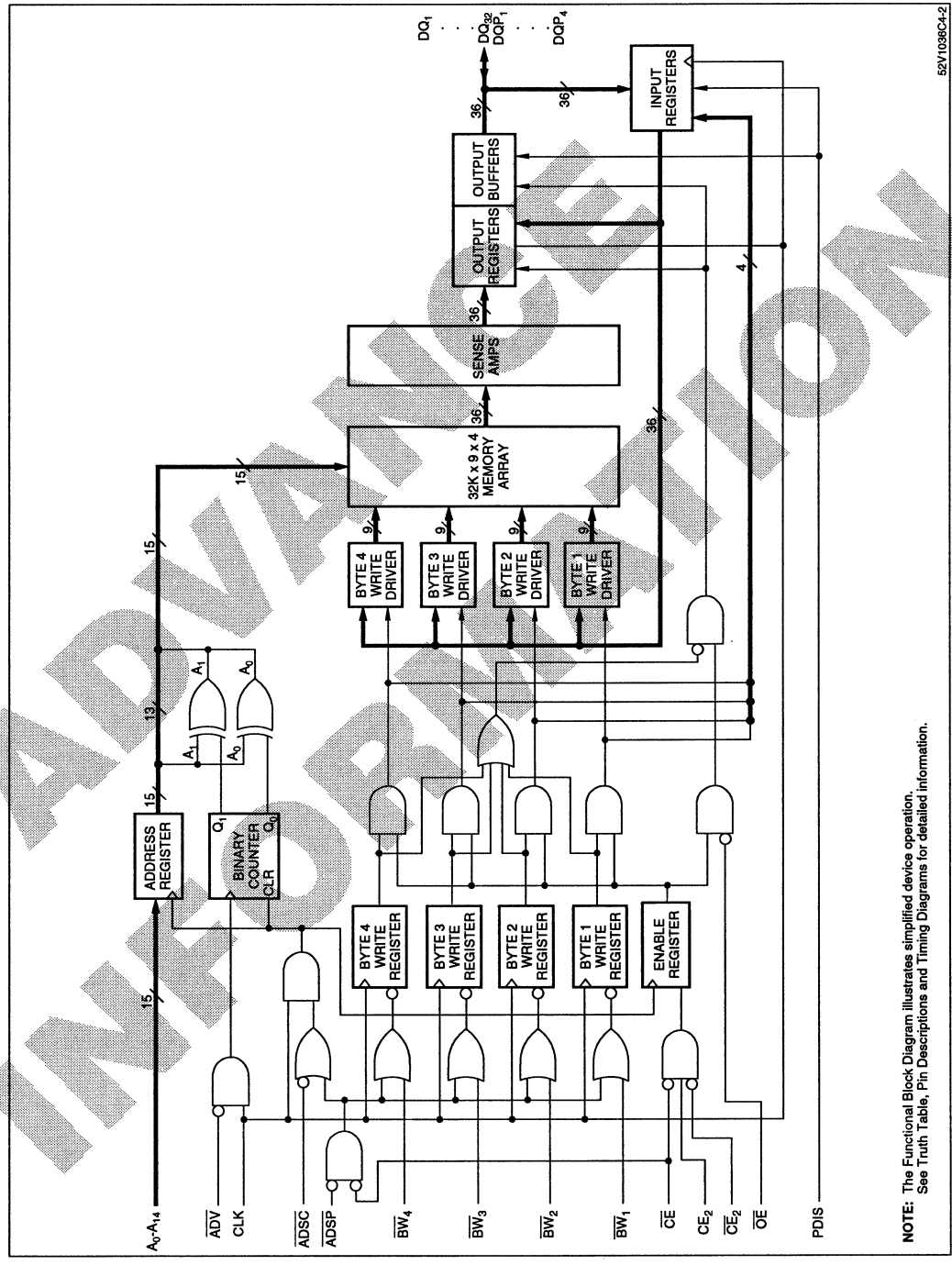


Figure 2. LH52V1036C4 Block Diagram

PIN DESCRIPTIONS

TQFP PIN NUMBER(S)	SYMBOL	TYPE	DESCRIPTION
37, 36, 35, 34, 33, 32, 100, 99, 82, 81, 44, 45, 46, 47, 48	A_0-A_{14}	Input	Synchronous Address Inputs: These inputs are registered and must meet the setup and hold times around the rising edge of CLK.
93, 94, 95, 96	$\overline{BW}_1$, $\overline{BW}_2$, $\overline{BW}_3$, $\overline{BW}_4$	Input	Synchronous Byte Write Enables: These active LOW inputs allow individual bytes to be written and must meet the setup and hold times around the rising edge of CLK. A BYTE WRITE enable is LOW for a WRITE cycle and HIGH for a READ cycle. $\overline{BW}_1$ controls DQ_1-DQ_8 and DQP_1. $\overline{BW}_2$ controls DQ_9-DQ_{16} and DQP_2. $\overline{BW}_3$ controls DQ_{17}-DQ_{24} and DQP_3. $\overline{BW}_4$ controls DQ_{25}-DQ_{32} and DQP_4. Data I/O are tristated if any of these four inputs are LOW.
89	CLK	Input	Clock: This signal latches the address, data, chip enables, byte write enables and burst control inputs on its rising edge. All synchronous inputs must meet setup and hold times around the clock's rising edge.
98	$\overline{CE}$	Input	Synchronous Chip Enable: This active LOW input is used to enable the device and conditions internal use of $\overline{ADSP}$. This input is sampled only when a new external address is loaded.
92	$\overline{CE}_2$	Input	Synchronous Chip Enable: This active LOW input is used to enable the device. This input is sampled only when a new external address is loaded. This input can be used for memory depth expansion.
97	CE_2	Input	Synchronous Chip Enable: This active HIGH input is used to enable the device. This input is sampled only when a new external address is loaded. This input can be used for memory depth expansion.
86	$\overline{OE}$	Input	Output Enable: This active LOW asynchronous input enables the data I/O output drivers.
83	$\overline{ADV}$	Input	Synchronous Address Advance: This active LOW input is used to advance the internal burst counter, controlling burst access after the external address is loaded. A HIGH on this pin effectively causes wait states to be generated (no address advance). This pin must be HIGH at the rising edge of the first clock after an $\overline{ADSP}$ cycle is initiated if a WRITE cycle is desired (to ensure use of correct address).
84	$\overline{ADSP}$	Input	Synchronous Address Status Processor: This active LOW input interrupts any ongoing burst, causing a new external address to be latched. A READ is performed using the new address, independent of the byte write enables and $\overline{ADSC}$ but dependent upon CE_2 and $\overline{CE}_2$. $\overline{ADSP}$ is ignored if $\overline{CE}$ is HIGH. Power-down state is entered if CE_2 is LOW or $\overline{CE}_2$ is HIGH.
85	$\overline{ADSC}$	Input	Synchronous Address Status Controller. This active LOW input interrupts any ongoing burst and causes a new external address to be latched. A READ or WRITE is performed using the new address if all chip enables are active. Power-down state is entered if one or more chip enables are inactive.

TQFP PIN NUMBER(S)	SYMBOL	TYPE	DESCRIPTION
14, 16, 31, 38, 39, 42, 43, 49, 50, 64, 66, 88	NC	–	No Connect: These signals are not internally connected.
52, 53, 56, 57, 58, 59, 62, 63, 68, 69, 72, 73, 74, 75, 78, 79, 2, 3, 6, 7, 8, 9, 12, 13, 18, 19, 22, 23, 24, 25, 28, 29	DQ_1-DQ_{32}	Input/Output	SRAM Data I/O: Byte 1 is DQ_1-DQ_8; Byte 2 is DQ_9-DQ_{16}; Byte 3 is DQ_{17}-DQ_{24}; Byte 4 is DQ_{25}-DQ_{32}. Input data must meet setup and hold times around the rising edge of CLK.
51, 80, 1, 30	DQP_1-DQP_4	Input/Output	Parity Data I/O: Byte 1 Parity is DQP_1; Byte 2 Parity is DQP_2; Byte 3 Parity is DQP_3; Byte 4 Parity is DQP_4.
87	PDIS	Input	Parity Disable: When HIGH, this input disables DQP_1 through DQP_4 for 32-bit data bus width. A LOW on PDIS enables control of DQP_1 through DQP_4 in the same manner as DQ_1-DQ_{32} are controlled.
15, 41, 65, 91	V_{CC}	Supply	Power Supply: +3.3 V ±5%
17, 40, 67, 90	V_{SS}	Supply	Ground: GND
4, 11, 20, 27, 54, 61, 70, 77	$V_{CC}Q$	Supply	Isolated Output Buffer Supply: +3.3 V ±5%
5, 10, 21, 26, 55, 60, 71, 76	$V_{SS}Q$	Supply	Isolated Output Buffer Ground: GND

PASS-THROUGH TRUTH TABLE

PREVIOUS CYCLE		PRESENT CYCLE				NEXT CYCLE
OPERATION	$\overline{BWs}$	OPERATION	$\overline{CE}$	$\overline{BWs}$	$\overline{OE}$	OPERATION
Initiate WRITE cycle, all bytes Address = A(n-1), data = D(n-1)	All L	Initiate READ cycle Register A(n), Q = D (n-1)	L	H	L	Read D(n)
Initiate WRITE cycle, all bytes Address = A(n-1), data = D(n-1)	All L	No new cycle Q = D(n-1)	H	H	L	No carryover from previous cycle
Initiate WRITE cycle, all bytes Address = A(n-1), data = D(n-1)	All L	No new cycle Q = HIGH-Z	H	H	H	No carryover from previous cycle
Initiate WRITE cycle, one byte Address = A(n-1), data = D(n-1)	One L	No new cycle Q = D(n-1) for one byte	H	H	L	No carryover from previous cycle

NOTE:
Previous cycle may be either BURST or NONBURST cycle.

BURST SEQUENCE TABLE

OPERATION	ADDRESS USED		
	A_{14}-A_2	A_1	A_0
First access, latch external address	A_{14}-A_2	A_1	A_0
Second access (first burst address)	Latched A_{14}-A_2	Latched A_1	Latched $\overline{A}_0$
Third access (second burst address)	Latched A_{14}-A_2	Latched $\overline{A}_1$	Latched A_0
Fourth access (third burst address)	Latched A_{14}-A_2	Latched $\overline{A}_1$	Latched $\overline{A}_0$

NOTE:
The burst sequence wraps around to its initial state upon completion.

BURST ADDRESS TABLE

FIRST ADDRESS	SECOND ADDRESS	THIRD ADDRESS	FOURTH ADDRESS
X . . . X00	X . . . X01	X . . . X10	X . . . X11
X . . . X01	X . . . X00	X . . . X11	X . . . X10
X . . . X10	X . . . X11	X . . . X00	X . . . X01
X . . . X11	X . . . X10	X . . . X01	X . . . X00

TRUTH TABLE

OPERATION	ADDRESS USED	$\overline{CE}$	$\overline{CE_2}$	CE_2	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{WRITE}$	$\overline{OE}$	CLK	DQ
Deselected Cycle, Power-down	None	H	X	X	X	L	X	X	X	L-H	High-Z
Deselected Cycle, Power-down	None	L	X	L	L	X	X	X	X	L-H	High-Z
Deselected Cycle, Power-down	None	L	H	X	L	X	X	X	X	L-H	High-Z
Deselected Cycle, Power-down	None	L	X	L	H	L	X	X	X	L-H	High-Z
Deselected Cycle, Power-down	None	L	H	X	H	L	X	X	X	L-H	High-Z
READ Cycle, Begin Burst	External	L	L	H	L	X	X	X	L	L-H	Q
READ Cycle, Begin Burst	External	L	L	H	L	X	X	X	H	L-H	High-Z
WRITE Cycle, Begin Burst	External	L	L	H	H	L	X	L	X	L-H	D
READ Cycle, Begin Burst	External	L	L	H	H	L	X	H	L	L-H	Q
READ Cycle, Begin Burst	External	L	L	H	H	L	X	H	H	L-H	High-Z
READ Cycle, Continue Burst	Next	X	X	X	H	H	L	H	L	L-H	Q
READ Cycle, Continue Burst	Next	X	X	X	H	H	L	H	H	L-H	High-Z
READ Cycle, Continue Burst	Next	H	X	X	X	H	L	H	L	L-H	Q
READ Cycle, Continue Burst	Next	H	X	X	X	H	L	H	H	L-H	High-Z
WRITE Cycle, Continue Burst	Next	X	X	X	H	H	L	L	X	L-H	D
WRITE Cycle, Continue Burst	Next	H	X	X	X	H	L	L	X	L-H	D
READ Cycle, Suspend Burst	Current	X	X	X	H	H	H	H	L	L-H	Q
READ Cycle, Suspend Burst	Current	X	X	X	H	H	H	H	H	L-H	High-Z
READ Cycle, Suspend Burst	Current	H	X	X	X	H	H	H	L	L-H	Q
READ Cycle, Suspend Burst	Current	H	X	X	X	H	H	H	H	L-H	High-Z
WRITE Cycle, Suspend Burst	Current	X	X	X	H	H	H	L	X	L-H	D
WRITE Cycle, Suspend Burst	Current	H	X	X	X	H	H	L	X	L-H	D

NOTES:

1. X means 'don't care.' H means logic HIGH. L means logic LOW. $\overline{WRITE}$ = L means any one or more byte write enable signals ($\overline{BW_1}$, $\overline{BW_2}$, $\overline{BW_3}$ or $\overline{BW_4}$) are LOW. $\overline{WRITE}$ = H means all byte write enable signals are HIGH.
2. $\overline{BW_1}$ enables writes to Byte 1 (DQ_1-DQ_8, DQP_1). $\overline{BW_2}$ enables writes to Byte 2 (DQ_9-DQ_{16}, DQP_2). $\overline{BW_3}$ enables writes to Byte 3 (DQ_{17}-DQ_{24}, DQP_3). $\overline{BW_4}$ enables writes to Byte 4 (DQ_{25}-DQ_{32}, DQP_4).
3. All inputs except $\overline{OE}$ must meet setup and hold times around the rising edge (LOW to HIGH) of CLK.
4. Wait states are inserted by suspending burst.
5. For a write operation following a read operation, $\overline{OE}$ must be HIGH before the input data required setup time and held HIGH throughout the input data hold time.
6. This is device contains circuitry that will ensure the outputs will be in High-Z during power-up.
7. PDIS disables the DQP lines when HIGH and enables the DQP lines when LOW.
8. $\overline{ADSP}$ LOW always initiates an internal READ at the L-H edge of CLK. A WRITE is performed by setting one or more byte write enable signals LOW for the subsequent L-H edge of CLK. Refer to WRITE timing diagram for clarification.

ABSOLUTE MAXIMUM RATINGS [1]

PARAMETER	RATING
Voltage on V_{CC} Supply Relative to V_{SS}	–0.5 V to +4.6 V
V_{IN}	–0.5 V to V_{CC} + 0.5 V
Storage Temperature (Plastic)	–55°C to +150°C
Junction Temperature	+150°C
Power Dissipation	1.6 W
Short Circuit Output Current	100 mA

NOTE:

1. Stresses greater than those listed under 'Absolute Maximum Ratings' may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS
($0°C \le T_A \le 70°C$; $T_C \le 110°C$; $V_{CC} = 3.3\ V \pm 5\%$ unless otherwise noted)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.0	V_{CC} + 0.5 V	V	1, 2
Input Low (Logic 0) Voltage		V_{IL}	–0.3	0.8	V	1, 2
Input Leakage Current	$0\ V \le V_{IN} \le V_{CC}$	I_{LI}	–1	1	µA	
Output Leakage Current	Output(s) Disabled, $0\ V \le V_{OUT} \le V_{CC}$	I_{LO}	–1	1	µA	
Output High Voltage	I_{OH} = –4.0 mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0 mA	V_{OL}		0.4	V	1
Supply Voltage		V_{CC}	3.1	3.5	V	1

NOTES:

1. All voltages referenced to V_{SS} (GND).
2. Overshoot: $V_{IH} \le V_{CC} + 2.0$ V for $t \le t_{KC}/2$. Undershoot: $V_{IL} \ge -2.0$ V for $t \le t_{KC}/2$. Power-up: $V_{IH} \le V_{CC} + 2.0$ V and $V_{CC} \le 3.1$ V for $t \le 200$ msec.

RECOMMENDED DC OPERATING CONDITIONS
(0°C ≤ T_A ≤ 70°C; T_C ≤ 110°C; V_{CC} = 3.3 V ±5% unless otherwise noted)

DESCRIPTION	CONDITIONS	SYMBOL	TYPICAL	MAX.				UNITS	NOTES
				-7	-10	-12	-15		
Power Supply Current: Operating	Device Selected; all inputs ≤ V_{IL} or ≥ V_{IH}; cycle time ≥ t_{KC} min; V_{CC} = MAX; outputs open	I_{CC}	150	250	210	180	165	mA	1, 2, 3
Power Supply Current: Idle	Device Selected; $\overline{ADSC}$, $\overline{ADSP}$, $\overline{ADV}$ ≥ V_{IH}; all inputs ≤ V_{IL} or ≥ V_{IH}; V_{CC} = MAX; cycle time ≥ t_{KC} min	I_{SB1}	50	85	70	60	55	mA	2, 3
CMOS Standby	Device Deselected; V_{CC} = MAX; all inputs ≤ V_{SS} +0.2 or ≥ V_{CC} -0.2; all inputs static; CLK frequency = 0	I_{SB2}	0.2	2	2	2	2	mA	2, 3
TTL Standby	Device Deselected; all inputs ≤ V_{IL} or ≥ V_{IH}; all inputs static; V_{CC} = MAX; CLK frequency = 0	I_{SB3}	10	18	18	18	18	mA	2, 3
Clock Running	Device Deselected; all inputs ≤ V_{IL} or ≥ V_{IH}; V_{CC} = MAX; CLK cycle time ≥ t_{KC} min	I_{SB4}	20	35	30	25	20	mA	2, 3

NOTES:

1. I_{CC} is given with no output current. I_{CC} increases with greater output loading and faster cycle times.
2. 'Device Deselected' means device is in POWER-DOWN mode as defined in the truth table. 'Device Selected' means device is active (not in POWER-DOWN mode).
3. Typical values are measured at 3.3 V, 25°C and 20 ns cycle time.

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	TYP	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1 MHz V_{CC} = 3.3 V	C_I	3	4	pF	1
Input/Output Capacitance (DQ)		C_O	5	6	pF	1

NOTE:

1. This parameter is sampled.

THERMAL CONSIDERATIONS

DESCRIPTION	CONDITIONS	SYMBOL	TYP	UNITS	NOTES
Thermal Resistance – Junction to Ambient	Still Air	θ_{JA}	65	°C/W	
Thermal Resistance – Junction to Case		θ_{JC}	6	°C/W	
Maximum Case Temperature		TC	110	°C	1

NOTE:

1. Sharp does not warrant the functionality or reliability of any product in which the case temperature exceeds 110°C. Care should be taken to limit case temperature to acceptable levels.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS [1]
($O°C \le T_A \le 70°C$; $V_{CC} = 3.3\ V \pm 5\%$)

DESCRIPTION	SYMBOL	-7		-10		-12		-15		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
CLOCK											
Clock Cycle Time	t_{KC}	15		20		25		30		ns	
Clock HIGH Time	t_{KH}	5		7		9		11		ns	
Clock LOW Time	t_{KL}	5		7		9		11		ns	
OUTPUT TIMES											
Clock to Output Valid	t_{KQ}		7		10		12		15	ns	
Clock to Output Invalid	t_{KQX}	3		3		3		3		ns	
Clock to Output in Low-Z	t_{KQLZ}	5		6		6		6		ns	2, 3
Clock to Output in High-Z	t_{KQHZ}		5		6		6		6	ns	2, 3
OE to Output Valid	t_{OEQ}		5		6		7		8	ns	4
OE to Output in Low-Z	t_{OELZ}	0		0		0		0		ns	2, 3
OE to Output in High-Z	t_{OEHZ}		5		6		6		6	ns	2, 3
SETUP TIMES											
Address	t_{AS}	2.5		3		3		3		ns	5, 6
Address Status ($\overline{ADSC}$, $\overline{ADSP}$)	t_{ADSS}	2.5		3		3		3		ns	5, 6
Address Advance ($\overline{ADV}$)	t_{AAS}	2.5		3		3		3		ns	5, 6
Byte Write Enables ($\overline{BW_1}$, $\overline{BW_2}$, $\overline{BW_3}$, $\overline{BW_4}$)	t_{WS}	2.5		3		3		3		ns	5, 6
Data In	t_{DS}	2.5		3		3		3		ns	5, 6
Chip Enables ($\overline{CE}$, $\overline{CE_2}$, CE_2)	t_{CES}	2.5		3		3		3		ns	5, 6
HOLD TIMES											
Address	t_{AH}	0.5		0.5		0.5		0.5		ns	5, 6
Address Status ($\overline{ADSC}$, $\overline{ADSP}$)	t_{ADSH}	0.5		0.5		0.5		0.5		ns	5, 6
Address Advance ($\overline{ADV}$)	t_{AAH}	0.5		0.5		0.5		0.5		ns	5, 6
Byte Write Enables ($\overline{BW_1}$, $\overline{BW_2}$, $\overline{BW_3}$, $\overline{BW_4}$)	t_{WH}	0.5		0.5		0.5		0.5		ns	5, 6
Data In	t_D	0.5		0.5		0.5		0.5		ns	5, 6
Chip Enables ($\overline{CE}$, $\overline{CE_2}$, CE_2)	t_{CEH}	0.5		0.5		0.5		0.5		ns	5, 6

NOTES:

1. Test conditions as specified with the output loading as shown in Figure 3 unless otherwise noted.
2. Output loading is specified with CL = 5 pF as in Figure 4. Transition is measured ±500 mV from steady state voltage.
3. At any given temperature and voltage condition, t_{KQHZ} is less than t_{KQLZ} and t_{OEHZ} is less than t_{OELZ}.
4. $\overline{OE}$ is a 'don't care' when a byte write enable is sampled LOW.
5. A READ cycle is defined by byte write enables all HIGH or $\overline{ADSP}$ LOW for the required setup and hold times. A WRITE cycle is defined by at least one byte write enable LOW and $\overline{ADSP}$ HIGH for the required setup and hold times.
6. This is a synchronous device. All addresses must meet the specified setup and hold times for all rising edges of CLK when either $\overline{ADSP}$ or $\overline{ADSC}$ is LOW and chip enabled. All other synchronous inputs must meet the setup and hold times with stable logic levels for all rising edges of clock (CLK) when chip is enabled. Chip enable must be valid at each rising edge of CLK (when either $\overline{ADSP}$ or $\overline{ADSC}$ is LOW) to remain enabled.

AC TEST CONDITIONS

PARAMETER	RATING
Input Pulse Levels	Vss to 3.0 V
Input Rise and Fall Times	1.5 ns
Input Timing Reference Levels	1.5 V
Output Reference Levels	1.5 V
Output Load	See Figures 3 and 4

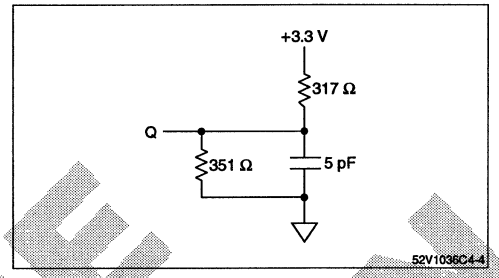


Figure 4. Output Load Equivalent

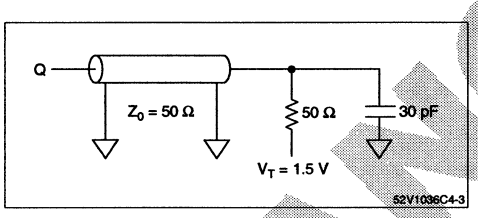


Figure 3. Output Load Equivalent

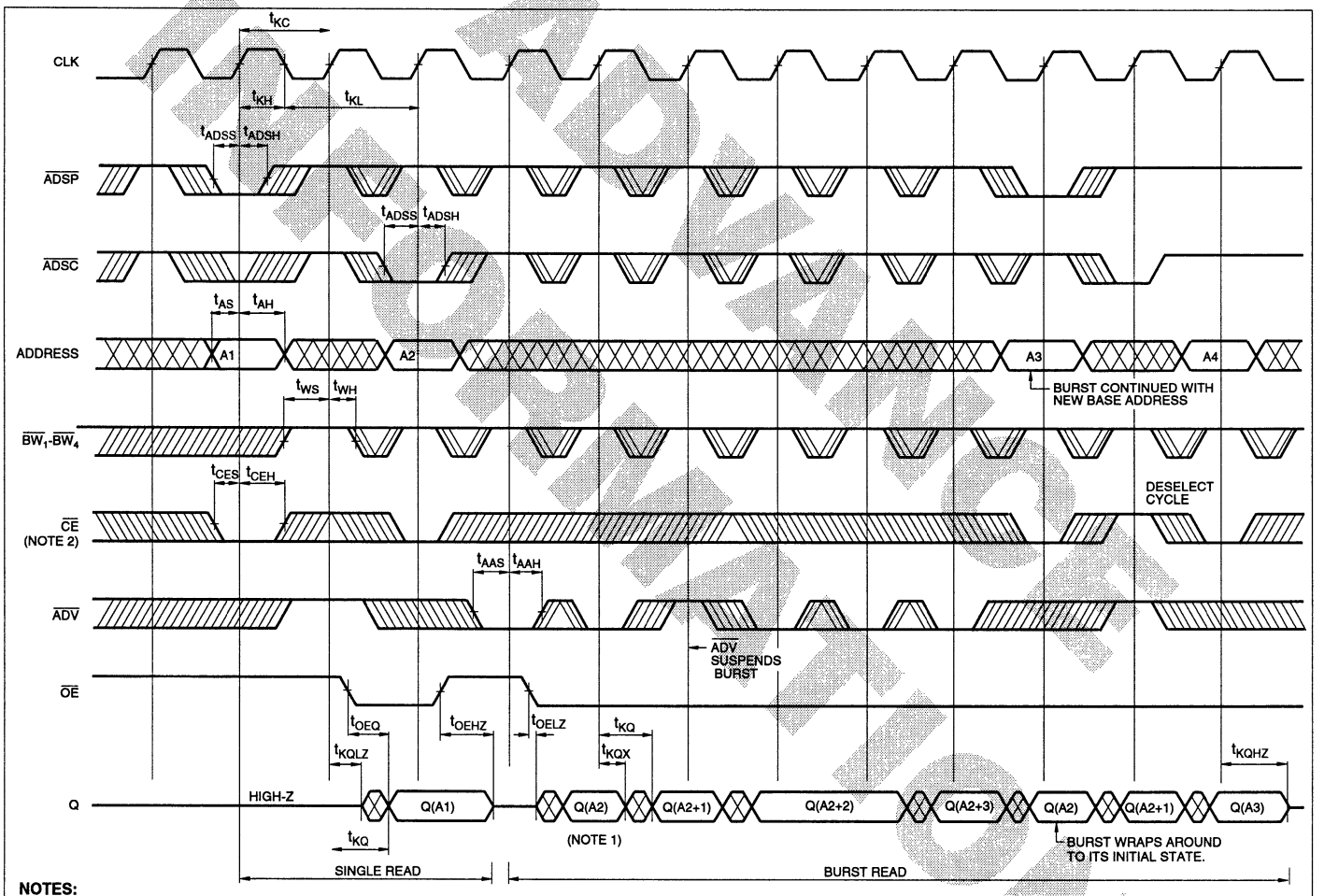


Figure 5. Read Timing

NOTES:

1. Q(A2) refers to output from address A2. Q(A2+1) refers to output from the next internal burst address following A2.
2. $\overline{CE}_2$ and $\underline{CE}_2$ have timing identical to $\overline{CE}$. On this diagram, when $\overline{CE}$ is LOW, $\overline{CE}_2$ is LOW and CE_2 is HIGH. When $\overline{CE}$ is HIGH, $\overline{CE}_2$ is HIGH and CE_2 is LOW.

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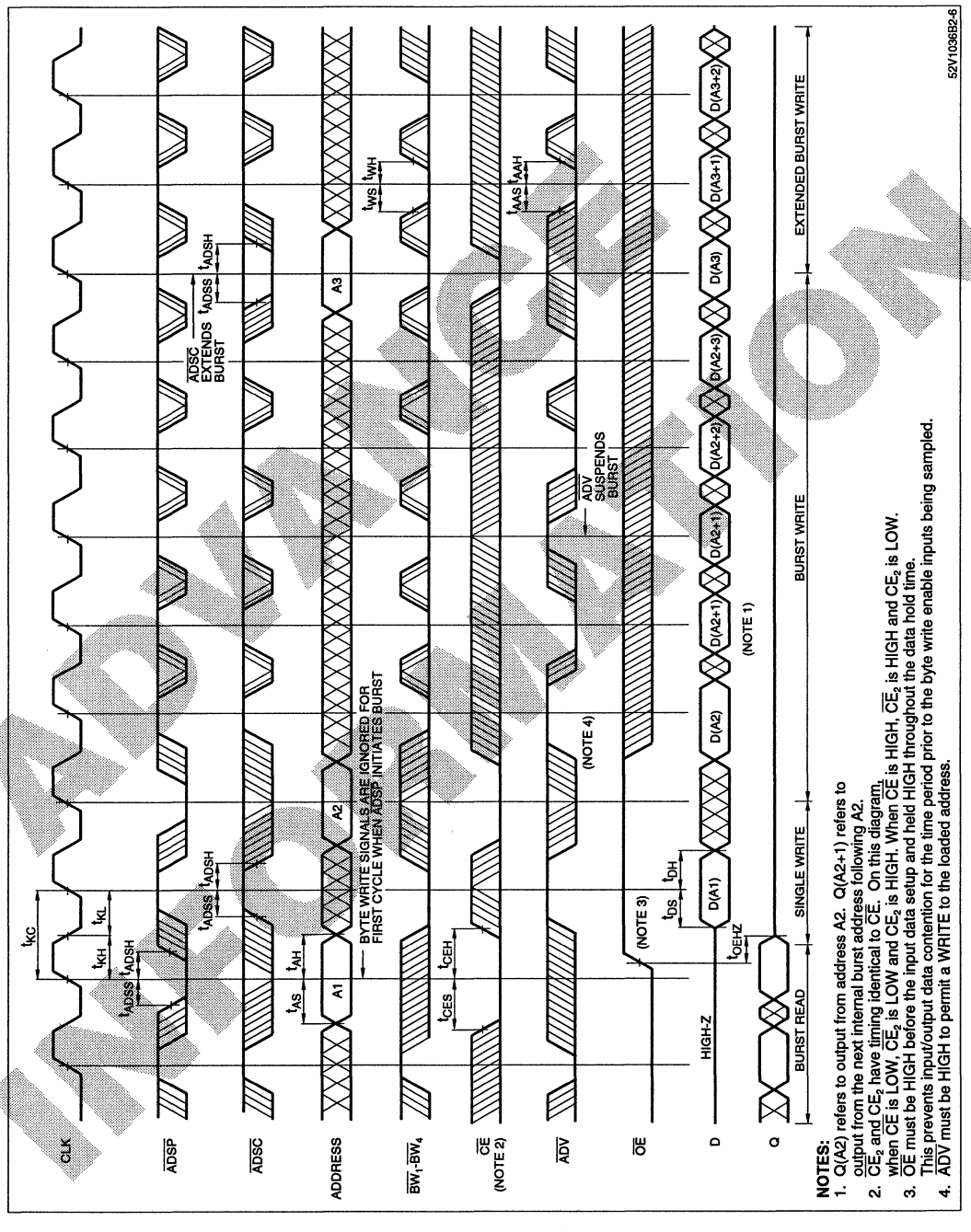
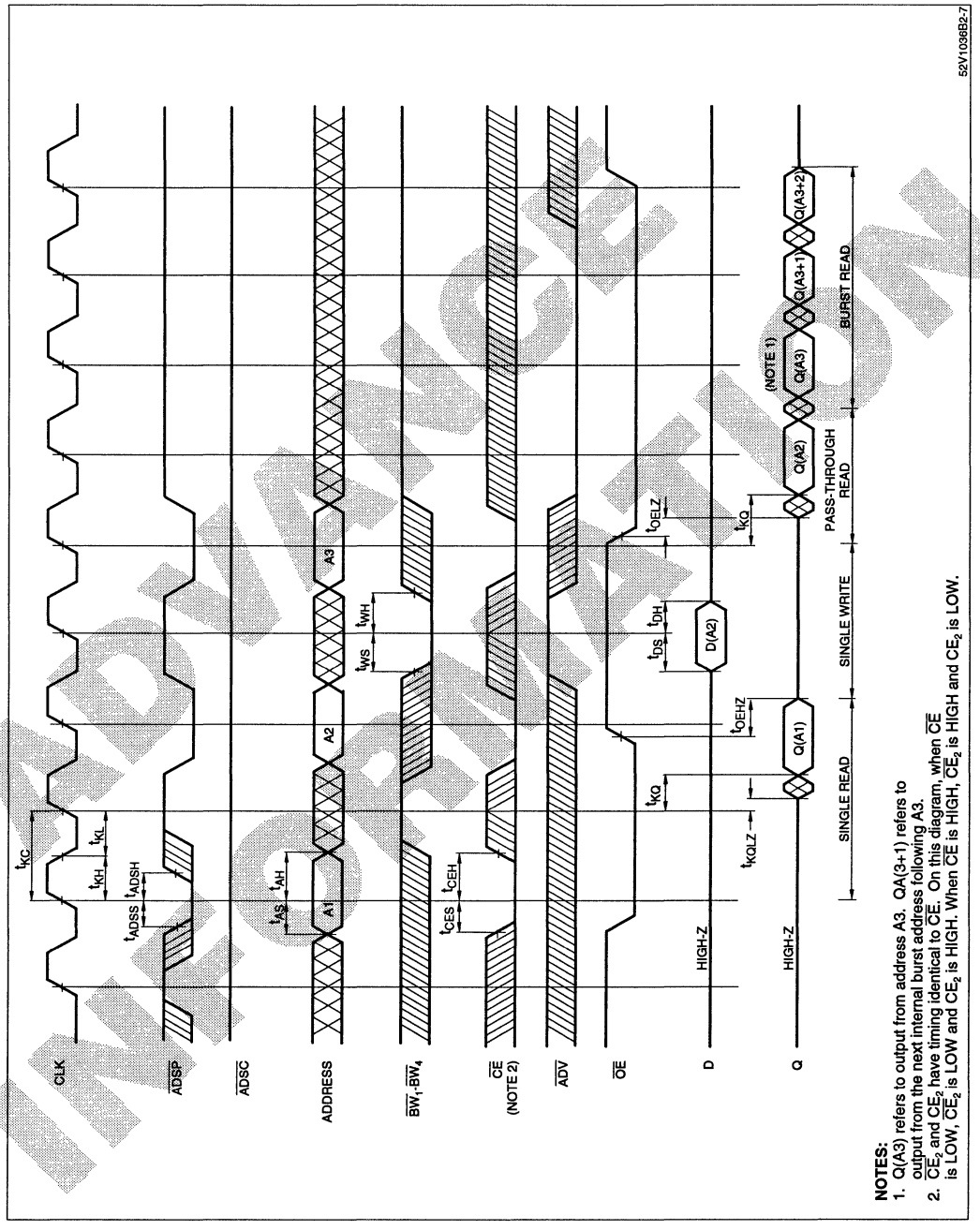


NOTES:
1. Q(A2) refers to output from address A2. Q(A2+1) refers to output from the next internal burst address following A2.
2. $\overline{CE}_2$ and CE_2 have timing identical to $\overline{CE}$. On this diagram, when $\overline{CE}$ is LOW, $\overline{CE}_2$ is LOW and CE_2 is HIGH. When $\overline{CE}$ is HIGH, $\overline{CE}_2$ is HIGH and CE_2 is LOW.
3. $\overline{OE}$ must be HIGH before the input data setup and held HIGH throughout the data hold time. This prevents input/output data contention for the time period prior to the byte write enable inputs being sampled.
4. $\overline{ADV}$ must be HIGH to permit a WRITE to the loaded address.

Figure 6. Write Timing



NOTES:
1. Q(A3) refers to output from address A3. QA(3+1) refers to output from the next internal burst address following A3.
2. $\overline{CE}_2$ and CE_2 have timing identical to $\overline{CE}$. On this diagram, when $\overline{CE}$ is LOW, $\overline{CE}_2$ is LOW and CE_2 is HIGH. When $\overline{CE}$ is HIGH, $\overline{CE}_2$ is HIGH and CE_2 is LOW.

Figure 7. Read/Write Timing

APPLICATION INFORMATION

32-Bit Wide Systems

The Sharp 32K × 36 Synchronous SRAM may be used in a 32-bit-wide system without the use of any external components by connecting PDIS to V_{CC}. This disables the output buffer on the data parity input/output lines (DQP_1, DQP_2, DQP_3 and DQP_4).

Load Derating Curves

The Sharp 32K × 36 Synchronous SRAM timing is dependent upon the capacitive loading on the outputs. The data sheet is written assuming a load of 30 pF. Access time changes with load capacitance as follows:

$Dt_{KQ} = 0.03$ ns/pF × ΔC_L pF

NOTE: this is preliminary information subject to change.

For example, if the SRAM loading is 22 pF, ΔC_L is −8 pF (8 pF less than rated load). The clock to valid output time of the SRAM is reduced by 0.03 × 8 = 0.24 ns. If the device is a 7 ns part, the worse case t_{KC} becomes 6.76 ns.

Consult the factory for copies of I/O current versus voltage curves and SPICE models.

Depth Expansion

The Sharp 32K × 36 Synchronous SRAM incorporates two additional chip enables to facilitate simple depth expansion. This permits easy cache upgrades from 32K depth to 64K depth with no extra logic as shown in Figure 8.

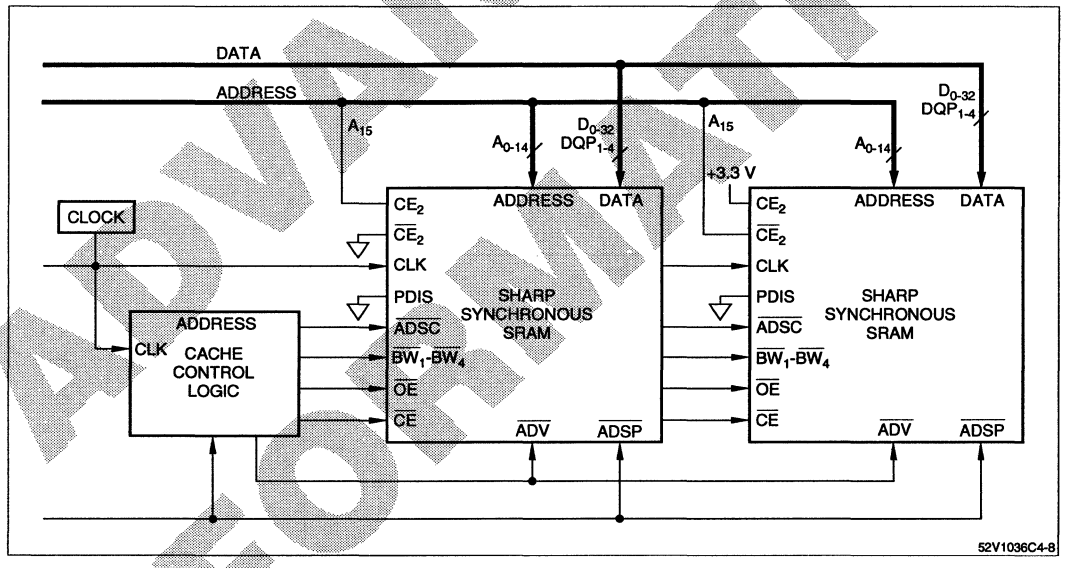


Figure 8. Depth Expansion from 32K x 36 to 64K x 36

APPLICATION EXAMPLES

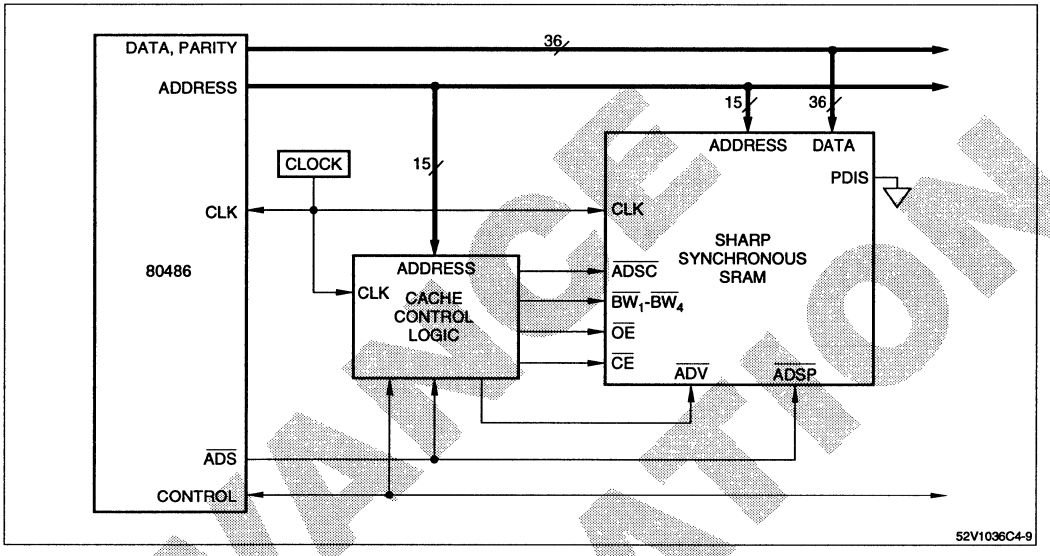


Figure 9. 128K Byte Secondary Cache with Parity and Burst for 50 MHz 80486 Using One LH52V1036-10 Synchronous SRAM

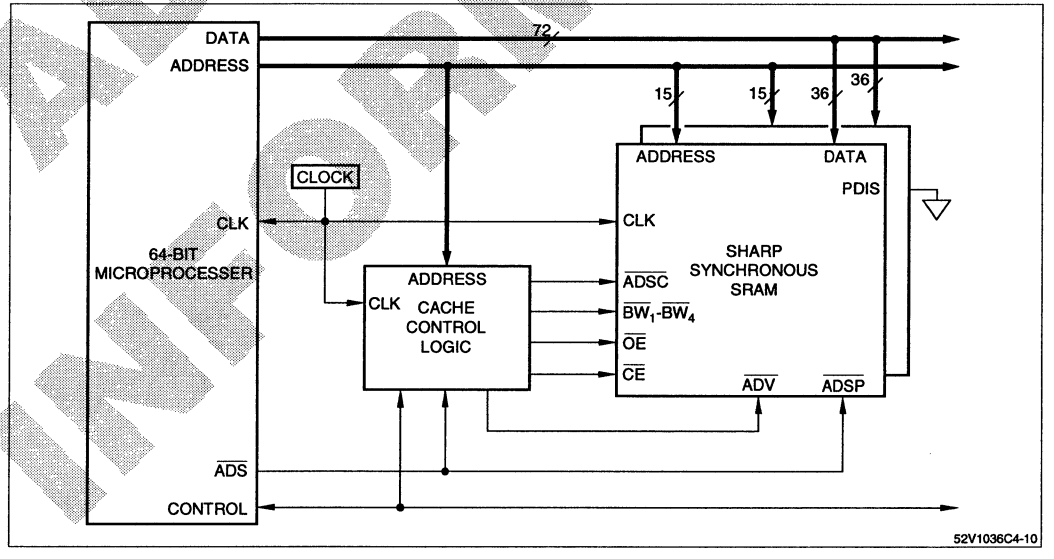
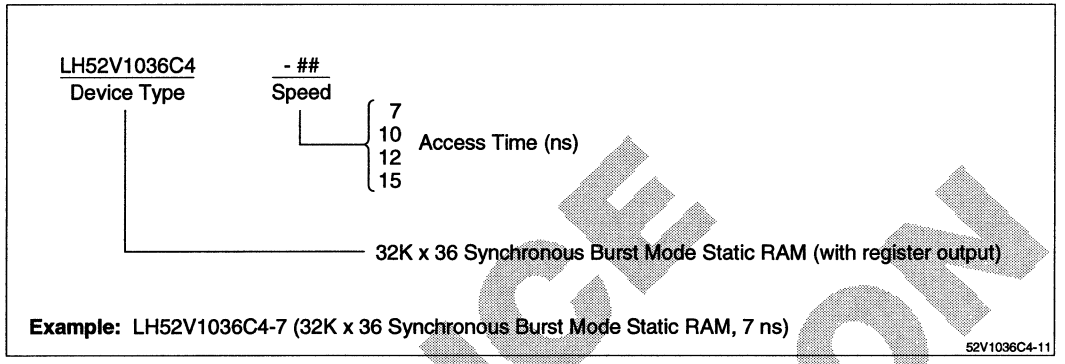


Figure 10. 256K Byte Secondary Cache with Parity and Burst for 66 MHz Pentium Microprocessor Using Two LH52V1036-7 Synchronous SRAMs

ORDERING INFORMATION



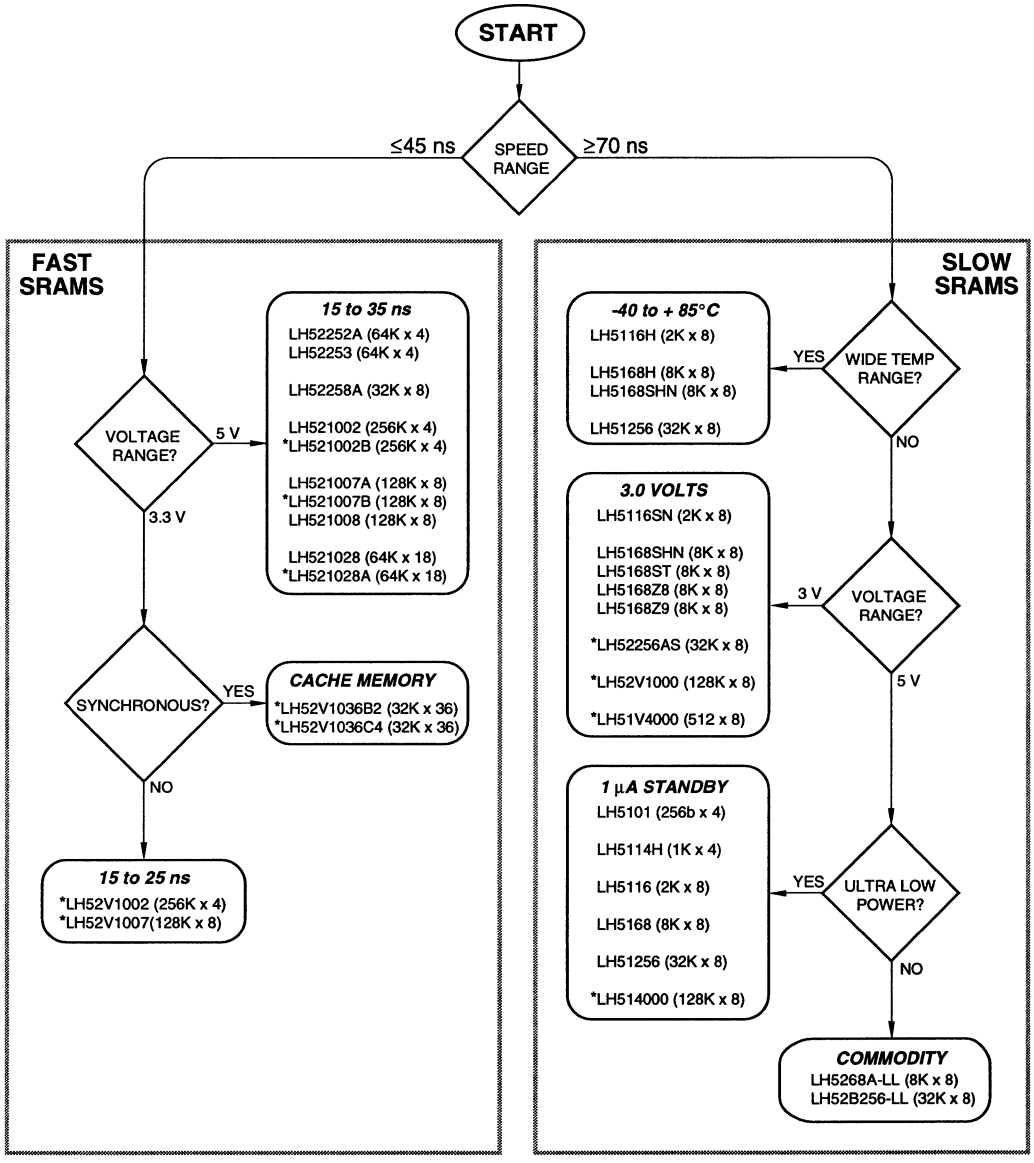
STATIC RAM CROSS REFERENCE

ORGANIZATIONAL STRUCTURE	SHARP MODEL	COMPETITIVE VENDOR	COMPETITIVE MODEL	ACCESS TIME	PACKAGE OPTIONS
256 x 4	LH5101	Harris	MWS5101	300 ns	DIP
		Intel	2101		
		Philips	PCD5101		
1K x 4	LH5114H	AMD	Am9114	150 ns	DIP
		Harris	MWS5114		
		Intel	2114		
		Philips	PCD5114		
		S-MOS	SRM2114		
		UMC	UM6104		
2K x 8 w/CE, OE	LH5116	AMD	Am9128	100 ns	DIP/SKDIP/SOP
		Harris	CDM6116		
		Hitachi	HM6116A		
		Hyundai	HY6116		
		Intel	5116		
		Matra HMS	HM6116		
		Mosel	MS6516		
		S-MOS	SRM2016		
		SGS-Thomson	MK6116		
		Sony	CXK5816		
		Toshiba	TC5516		
		UMC	UM6116		
2K x 8 w/CE1, CE2	LH5118	S-MOS	SRM2018	100 ns	DIP/SKDIP/SOP
		Toshiba	TC5518		
32K x 8 Slow	LH51256	Oki	MSM51256	100/120 ns	DIP/SOP
		Quality	QS83285		
		Sony	CXK58267		
		Toshiba	TC55258		
8K x 8 Slow	LH5168	Fujitsu	MB8464	80/100 ns	DIP/SKDIP/SOP/TSOP(I)
		Harris	CDM6264		
		Hitachi	HM6264A		
		Hyundai	HY6264		
		Intel	5164		
		Mitsubishi	M5M5165		
		Mosel	MS6264L		
		Motorola	MCM60L64		
		NEC	uPD4464		
		Oki	MSM5165A		
		S-MOS	SRM2264		
		Samsung	KM6264		
		SGS-Thomson	IMS1630		
		SGS-Thomson	MK6264		
		Sony	CXK5864B		
		Toshiba	TC5563		
		Toshiba	TC5564		
		Toshiba	TC5565		
		UMC	UM6264		

ORGANIZATIONAL STRUCTURE	SHARP MODEL	COMPETITIVE VENDOR	COMPETITIVE MODEL	ACCESS TIME	PACKAGE OPTIONS
8K x 8 Slow	LH5268A	Fujitsu	MB8464	100 ns	DIP/SKDIP/SOP
		Harris	CDM6264		
		Hitachi	HM6264A		
		Hyundai	HY6264		
		Intel	5164		
		Mitsubishi	M5M5165		
		Mosel	MS6264L		
		Motorola	MCM60L64		
		NEC	uPD4464		
		Oki	MSM5165A		
		S-MOS	SRM2264		
		Samsung	KM6264		
		SGS-Thomson	IMS1630		
		SGS-Thomson	MK6264		
		Sony	CXK5864B		
		Toshiba	TC5563		
		Toshiba	TC5564		
		Toshiba	TC5565		
		UMC	UM6264		
256K x 4 Fast	LH521002	Cypress	CY7C106	20/25/35 ns	SOJ
		EDI	EDI84256		
		Hitachi	HM624256		
		IDT	IDT71028		
		Micron	MT5C1005		
		Mitsubishi	M5M51004		
		Motorola	MCM6229		
		National	NMS1024X4		
		NEC	uPD431004		
		Sony	CXK541000		
128K x 8 Fast	LH521007A/08	Cypress	CY7C109	20/25/35 ns	SOJ
		EDI	EDI88128		
		EDI	EDI88130		
		IDT	IDT71024		
		Micron	MT5C1008		
		Micron	MT5C1009		
		Motorola	MCM6226		
		National	NMS1024X8		
		Paradigm	PDM41024		
		Philips	FCB61C1025		
		Quality	QS812880		
		Sony	CXK581020		
64K x 18 Fast	LH521028	National	NMS1024X18	20/25/35 ns	PLCC

ORGANIZATIONAL STRUCTURE	SHARP MODEL	COMPETITIVE VENDOR	COMPETITIVE MODEL	ACCESS TIME	PACKAGE OPTIONS
32K x 8 Slow	LH52B256	Catalyst	CAT71C256	70/100 ns	DIP/SKDIP/SOP/TSOP(I)
		EDI	EDI8832		
		Fujitsu	MB84256		
		Harris	CDM62256		
		Hitachi	HM62256		
		Hyundai	HY62C256		
		IDT	IDT71256		
		Intel	51256SL		
		ISSI	IS61C256		
		Mitsubishi	M5M5255		
		Mitsubishi	M5M5256		
		Mosel	MS62256L		
		Motorola	MCM60L256A		
		NEC	uPD43256		
		NEC	uPD43257		
		Oki	MSM51257		
		Panasonic	MN44256		
		Philips	FCB61C257		
		S-MOS	SRM20256		
		Samsung	KM62256		
		SGS-Thomson	MK48256		
		Sony	CXK58257		
		Toshiba	TC55256		
		Toshiba	TC55257		
		UMC	UM62256		
64K x 4 w/OE	LH52253	Cypress	CY7C195	20/25/35 ns	DIP/SOJ
		EDI	EDI8466		
		Hitachi	HM6709		
		IDT	IDT61298		
		Matra MHS	HM65799		
		Micron	MT5C2565		
		Motorola	MCM6209		
		Philips	FCB61C253		
		Toshiba	TC55465		
32K x 8 Fast	LH52258A	Cypress	CY7C199	20/25/35/45 ns	DIP/SOJ
		EDI	EDI8834		
		Fujitsu	MB5298		
		Hitachi	HM62832		
		Hyundai	HY63C256		
		Intel	51256		
		ISSI	IS61C256		
		Matra MHS	HM65756		
		Matra MHS	M65656		
		Micron	MT5C2568		
		Motorola	MCM6206		
		National	NMS256X8		
		NEC	uPD43258		
		Panasonic	MN44251		
		Paradigm	PDM41256		
		Quality	QS83280		
		Samsung	KM68257		
		Sony	CXK58258		
		Toshiba	TC55328		
		VLSI	VT62832		

CHOOSING A SHARP STATIC RAM



NOTE: *PRODUCT IN DEVELOPMENT

MASK-PROGRAMMABLE ROMs

LH53259

CMOS 256K (32K × 8) Mask-Programmable ROM

FEATURES

- 32,768 × 8 bit organization
- Access time: 150 ns (MAX.)
- Low-power consumption:
  Operating: 110 mW (MAX.)
  Standby: 82.5 μW (MAX.)
- Programmable output enable
- Static operation (Internal sync. system)
- TTL compatible I/O
- Three-state outputs
- Single +5 V power supply
- Packages:
  28-pin, 600-mil DIP
  28-pin, 450-mil SOP
  44-pin, 10 × 10 mm^2 QFP
- JEDEC standard EPROM pinout (DIP)

DESCRIPTION

The LH53259 is a mask-programmable ROM organized as 32,768 × 8 bits. It is fabricated using silicon-gate CMOS process technology.

PIN CONNECTIONS

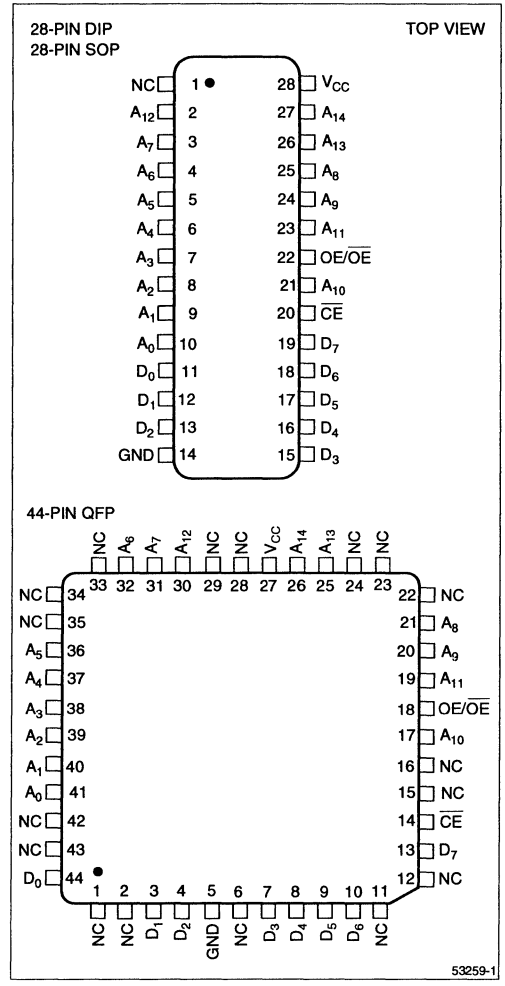


Figure 1. Pin Connections for DIP, SOP, and QFP Packages

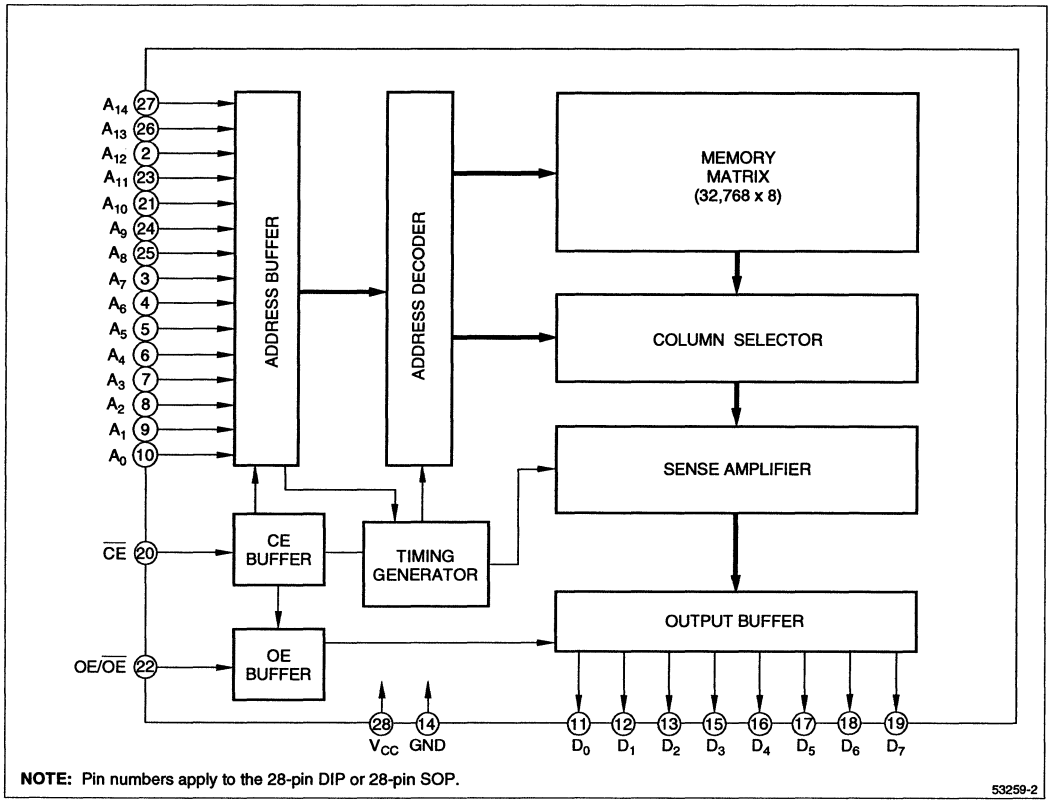


Figure 2. LH53259 Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME	NOTE
A_0 - A_{14}	Address input	
D_0 - D_7	Data output	
$\overline{CE}$	Chip enable input	
OE/$\overline{OE}$	Output enable input	1

SIGNAL	PIN NAME	NOTE
V_{CC}	Power supply (+5 V)	
GND	Ground	
NC	Non connection	

NOTE:
1. The active level of OE/$\overline{OE}$ is mask-programmable.

TRUTH TABLE

$\overline{CE}$	OE/$\overline{OE}$	MODE	D_0 - D_7	SUPPLY CURRENT	NOTE
H	X	Non selected	High-Z	Standby	1
L	L/H			Operating	
	H/L	Selected	D_{OUT}		

NOTE:
1. X = H or L

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Supply voltage	V_{CC}	-0.3 to +7.0	V	1
Input voltage	V_{IN}	-0.3 to V_{CC} +0.3	V	
Output voltage	V_{OUT}	-0.3 to V_{CC} +0.3	V	
Operating temperature	Topr	0 to +70	°C	
Storage temperature	Tstg	-55 to +150	°C	

NOTE:
1. The maximum applicable voltage on any pin with respect to GND.

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	4.5	5.0	5.5	V

DC CHARACTERISTICS (V_{CC} = 5 V ±10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Input 'Low' voltage	V_{IL}		-0.3		0.8	V	
Input 'High' voltage	V_{IH}		2.2		V_{CC} +0.3	V	
Output 'Low' voltage	V_{OL}	I_{OL} = 1.6 mA			0.4	V	
Output 'High' voltage	V_{OH}	I_{OH} = -400 µA	2.4			V	
Input leakage current	$\lvert I_{LI} \rvert$	V_{IN} = 0 V to V_{CC}			10	µA	
Output leakage current	$\lvert I_{LO} \rvert$	V_{OUT} = 0 V to V_{CC}			10	µA	1
Operating current	I_{CC1}	t_{RC} = 150 ns			20	mA	2
	I_{CC2}	t_{RC} = 1 µs			15		
	I_{CC3}	t_{RC} = 150 ns			15	mA	3
	I_{CC4}	t_{RC} = 1 µs			10		
Standby current	I_{SB1}	$\overline{CE}$ = V_{IH}			2	mA	
	I_{SB2}	$\overline{CE}$ = V_{CC} - 0.2 V			15	µA	

NOTES:
1. $\overline{CE}/\overline{OE}$ = V_{IH} or OE = VIL
2. V_{IN} = V_{IH}/V_{IL}, $\overline{CE}$ = V_{IL}, outputs open
3. V_{IN} = (V_{CC} - 0.2 V) or 0.2 V, $\overline{CE}$ = 0.2 V, outputs open

AC CHARACTERISTICS (V_{CC} = 5 V ±10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Read cycle time	t_{RC}	150			ns	
Address access time	t_{AA}			150	ns	
Chip enable access time	t_{ACE}			150	ns	
Output enable time	t_{OE}	10		80	ns	
Output hold time	t_{OH}	5			ns	
$\overline{CE}$ to output in High-Z	t_{CHZ}			70	ns	1
OE to output in High-Z	t_{OHZ}			70	ns	

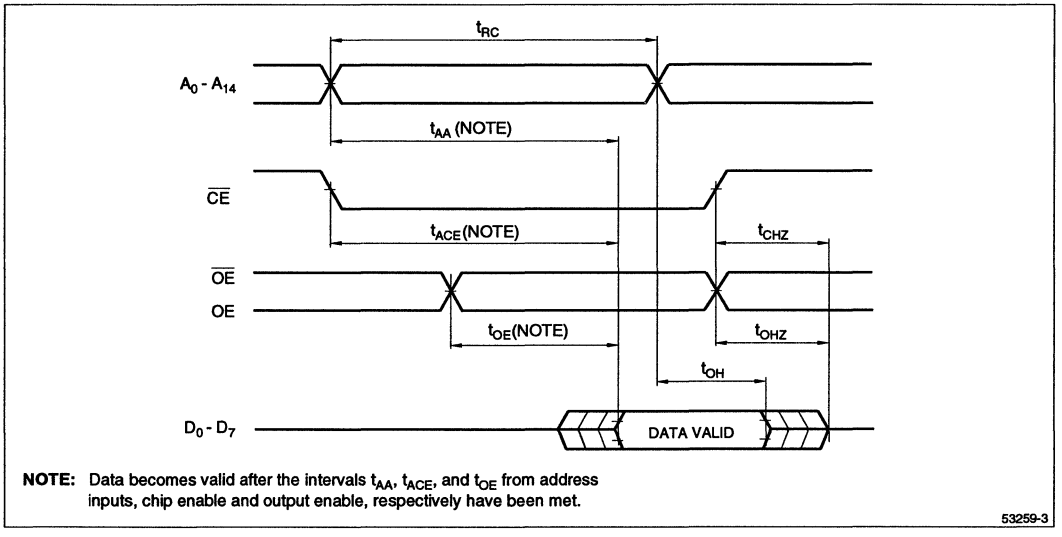
NOTE:
1. This is the time required for the output to become high impedance.

AC TEST CONDITIONS

PARAMETER	RATING
Input voltage amplitude	0.6 V to 2.4 V
Input rise/fall time	10 ns
Input reference level	1.5 V
Output reference level	0.8 V and 2.2 V
Output load condition	1TTL +100 pF

CAPACITANCE (V_{CC} = 5 V ±10%, f = 1 MHz, T_A = 25°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Input capacitance	C_{IN}			10	pF
Output capacitance	C_{OUT}			10	pF

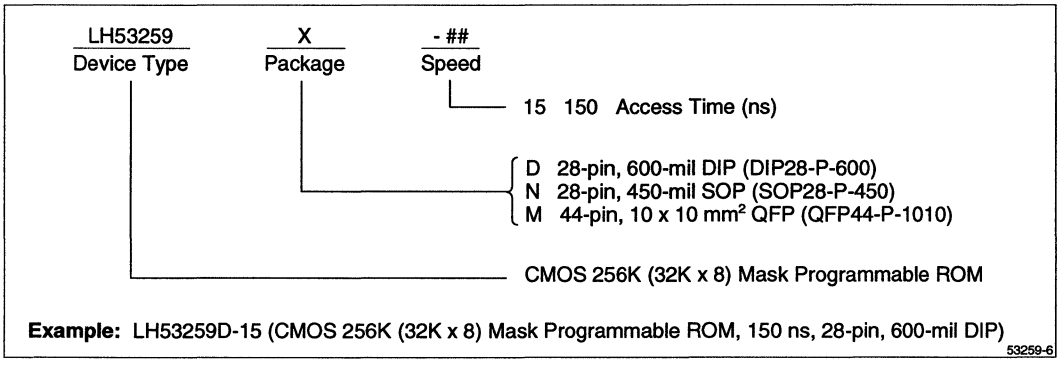


NOTE: Data becomes valid after the intervals t_{AA}, t_{ACE}, and t_{OE} from address inputs, chip enable and output enable, respectively have been met.

53259-3

Figure 3. Timing Diagram

ORDERING INFORMATION



Example: LH53259D-15 (CMOS 256K (32K x 8) Mask Programmable ROM, 150 ns, 28-pin, 600-mil DIP)

53259-6

LH53515

CMOS 512K (64K × 8) Mask-Programmable ROM

FEATURES

- 65,536 × 8 bit organization
- Access time: 150 ns (MAX.)
- Low-power consumption:
  Operating: 195 mW (MAX.)
  Standby: 550 μW (MAX.)
- Programmable output enable
- Static operation (Internal sync. system)
- TTL compatible I/O
- Three-state outputs
- Single +5 V power supply
- Packages:
  28-pin, 600-mil DIP
  28-pin, 450-mil SOP
  32-pin, 525-mil SOP
  44-pin, 10 × 10 mm^2 QFP
- JEDEC standard EPROM pinout (DIP)

PIN CONNECTIONS

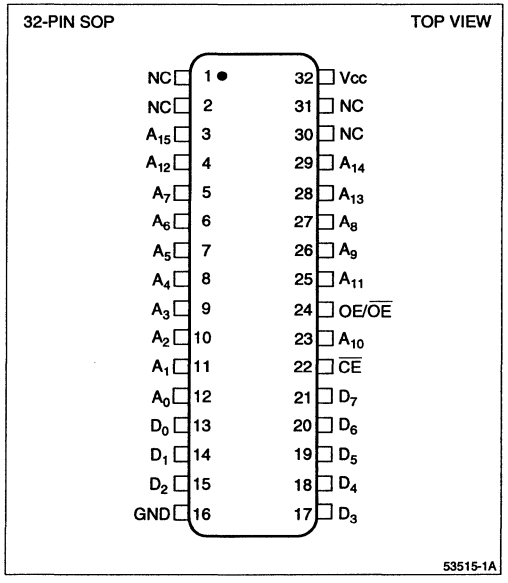


Figure 1. Pin Connections for SOP Package

DESCRIPTION

The LH53515 is a mask-programmable ROM organized as 65,536 × 8 bits. It is fabricated using silicon-gate CMOS process technology.

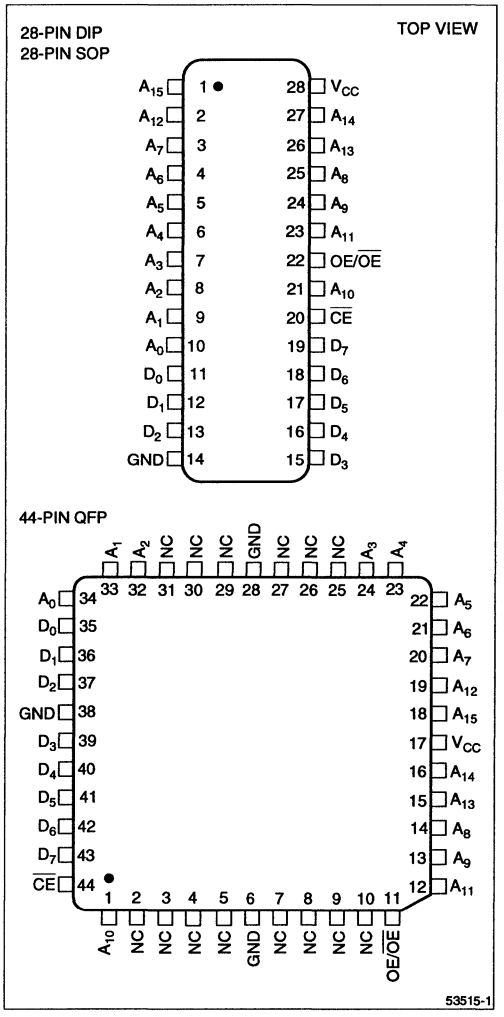


Figure 2. Pin Connections for DIP, SOP, and QFP Packages

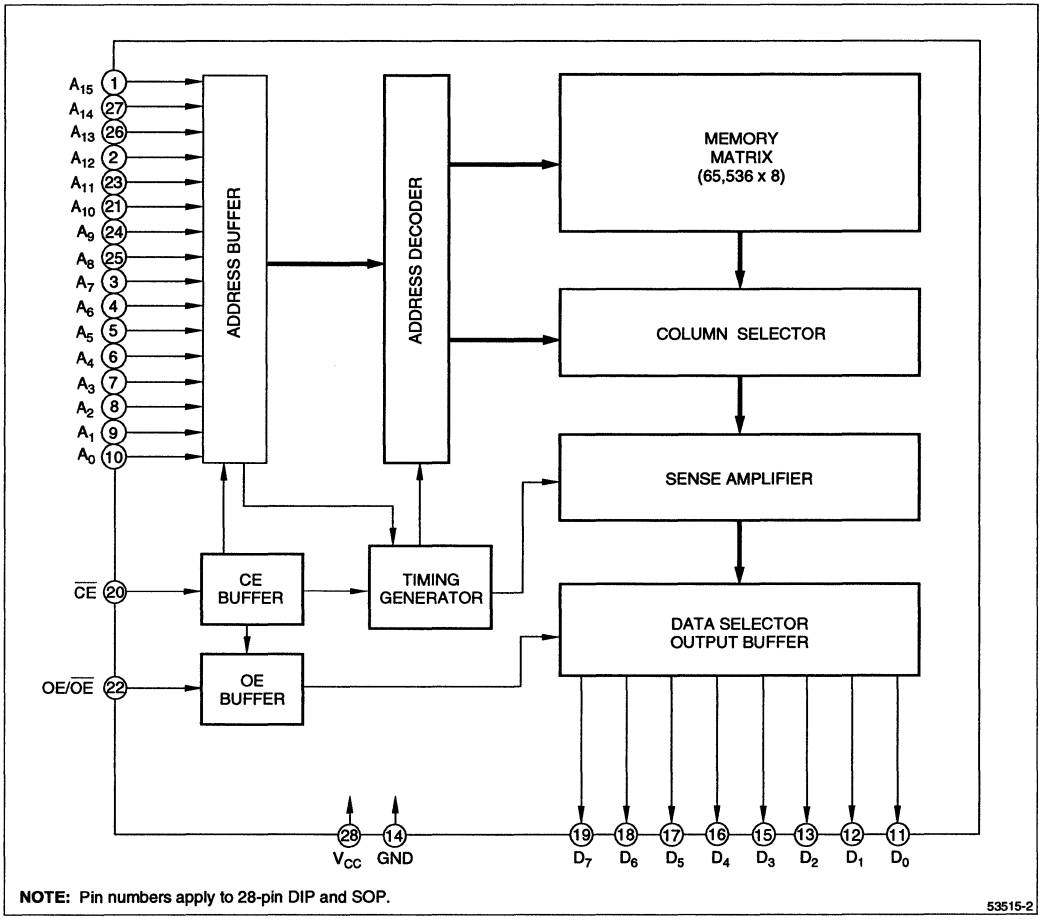


Figure 3. LH53515 Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME	NOTE
A_0 - A_{15}	Address input	
D_0 - D_7	Data output	
$\overline{CE}$	Chip enable input	

SIGNAL	PIN NAME	NOTE
OE/$\overline{OE}$	Output enable input	1
V_{CC}	Power supply (+5 V)	
GND	Ground	

NOTE:
1. Active level of OE/$\overline{OE}$ is mask-programmable.

TRUTH TABLE

$\overline{CE}$	OE/$\overline{OE}$	MODE	D_0 - D_7	CURRENT CONSUMPTION	NOTE
H	X	Non selected	High-Z	Standby(I_{SB})	1
L	L/H			Operating(I_{CC})	
	H/L	Selected	D_{OUT}		

NOTE:
1. X = H or L

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Supply voltage	V_{CC}	-0.3 to +7.0	V	1
Input voltage	V_{IN}	-0.3 to V_{CC} +0.3	V	1
Output voltage	V_{OUT}	-0.3 to V_{CC} +0.3	V	1
Operating temperature	Topr	0 to +70	°C	
Storage temperature	Tstg	-55 to +150	°C	

NOTE:
1. The maximum applicable voltage on any pin with respect to GND.

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	4.5	5.0	5.5	V

DC CHARACTERISTICS (V_{CC} = 5 V ±10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Input 'Low' voltage	V_{IL}		-0.3		0.8	V	
Input 'High' voltage	V_{IH}		2.2		V_{CC} +0.3	V	
Output 'Low' voltage	V_{OL}	I_{OL} = 1.6 mA			0.4	V	
Output 'High' voltage	V_{OH}	I_{OH} = -400 µA	2.4			V	
Input leakage current	$\|I_{LI}\|$	V_{IN} = 0 V to V_{CC}			10	µA	
Output leakage current	$\|I_{LO}\|$	V_{OUT} = 0 V to V_{CC}			10	µA	1
Operating current	I_{CC1}	t_{RC} = 150 ns			35	mA	2
	I_{CC2}	t_{RC} = 1 µs			25		
	I_{CC3}	t_{RC} = 150 ns			30	mA	3
	I_{CC4}	t_{RC} = 1 µs			20		
Standby current	I_{SB1}	$\overline{CE}$ = V_{IH}			2	mA	
	I_{SB2}	$\overline{CE}$ = V_{CC} - 0.2 V			100	µA	

NOTES:
1. OE = V_{IL} or $\overline{CE}/\overline{OE}$ = V_{IH}
2. V_{IN} = V_{IH}/V_{IL}, $\overline{CE}$ = V_{IL}, outputs open
3. V_{IN} = (V_{CC} - 0.2 V) or 0.2 V, $\overline{CE}$ = 0.2 V, outputs open

AC CHARACTERISTICS (V_{CC} = 5 V ±10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Read cycle time	t_{RC}		150			ns	
Address access time	t_{AA}				150	ns	
Chip enable access time	t_{ACE}				150	ns	
Output enable time	t_{OE}		10		80	ns	
Output hold time	t_{OH}		5			ns	
$\overline{CE}$ to output in High-Z	t_{CHZ}				70	ns	1
OE to output in High-Z	t_{OHZ}				70	ns	1

NOTE:
1. This is the time required for the output to become high-impedance.

AC TEST CONDITIONS

PARAMETER	RATING
Input voltage amplitude	0.6 V to 2.4 V
Input rise/fall time	10 ns
Input reference level	1.5 V
Output reference level	0.8 V and 2.2 V
Output load condition	1TTL +100 pF

CAPACITANCE (V_{CC} = 5 V ±10%, f = 1 MHz, T_A = 25°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Input capacitance	C_{IN}			10	pF
Output capacitance	C_{OUT}			10	pF

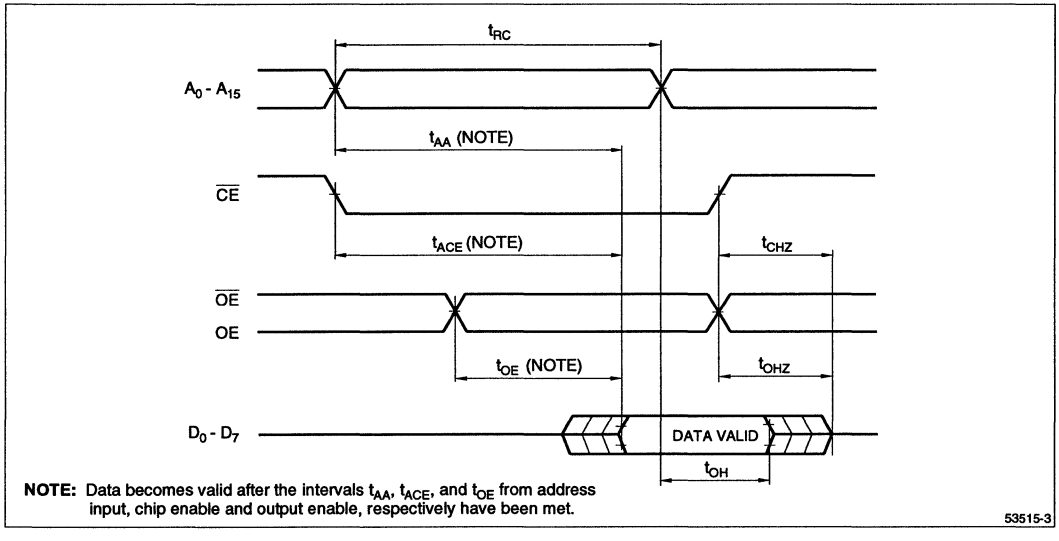
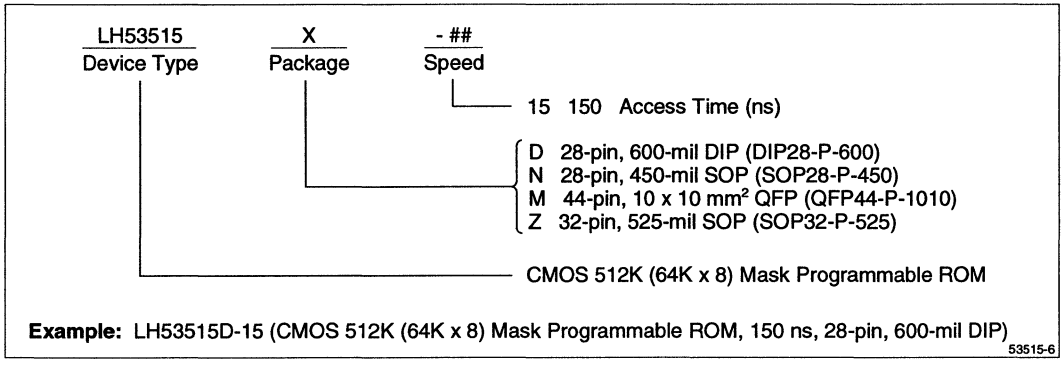


Figure 4. Timing Diagram

ORDERING INFORMATION



LH53H0900

PRELIMINARY

CMOS 1M (128K × 8) Mask-Programmable ROM

FEATURES

- 131,072 × 8 bit organization
- Access time: 55 ns (MAX.)
- Power consumption:
  Operating: 660 mW (MAX.)
  Standby: 440 mW (MAX.)
- Fully-static operation
- TTL compatible I/O
- Three-state outputs
- Single +5 V power supply
- Packages:
  32-pin, 600-mil DIP
  32-pin, 525-mil SOP
- JEDEC standard EPROM pinout (DIP)

DESCRIPTION

The LH53H0900 is a high speed mask-programmable ROM organized as 131,072 × 8 bits (1,048,576 bits). It is fabricated using silicon-gate CMOS process technology.

PIN CONNECTIONS

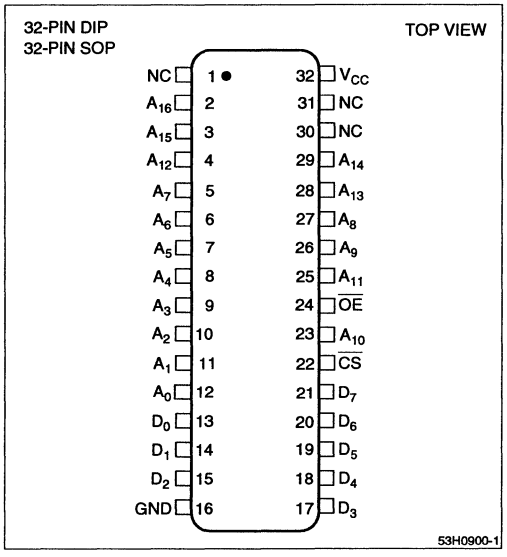


Figure 1. Pin Connections for DIP and SOP Packages

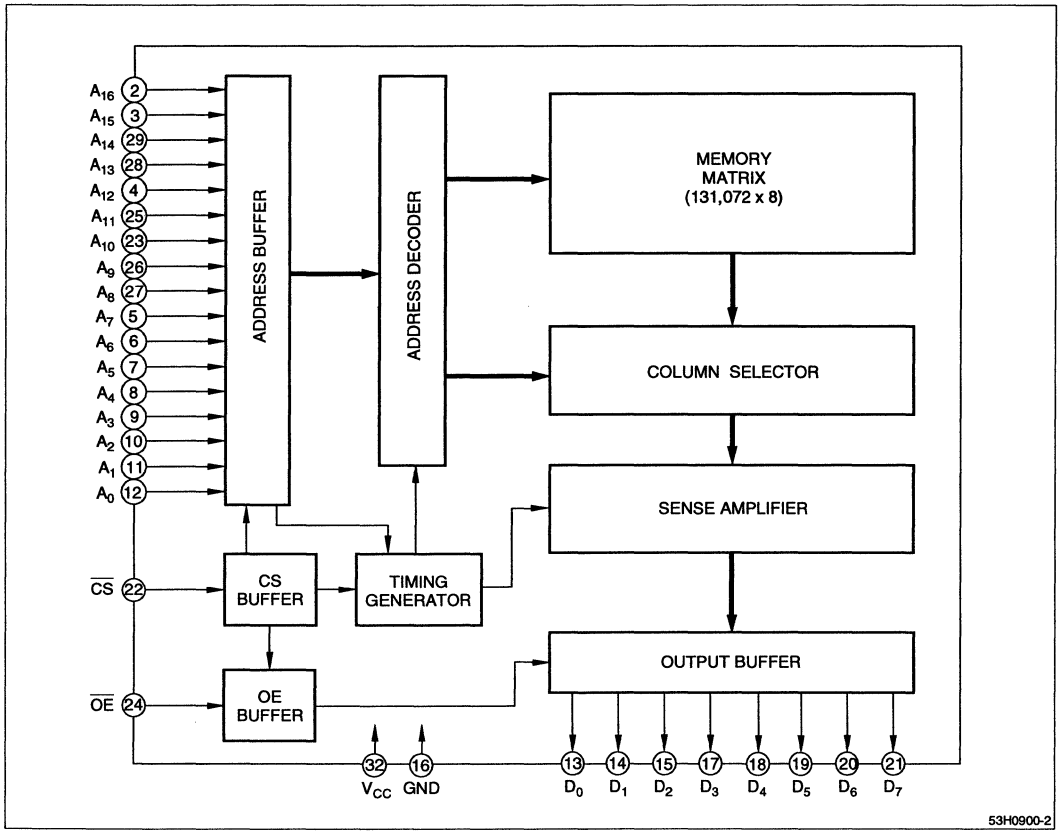


Figure 2. LH53H0900 Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME
A_0 - A_{16}	Address input
D_0 - D_7	Data output
$\overline{CS}$	Chip Select input

SIGNAL	PIN NAME
$\overline{OE}$	Output Enable input
V_{CC}	Power supply (+5 V)
GND	Ground

TRUTH TABLE

$\overline{CS}$	$\overline{OE}$	MODE	D_0 - D_7	SUPPLY CURRENT	NOTE
H	X	Non selected	High-Z	Standby (I_{SB})	1
L	H	Non selected	High-Z	Operating (I_{CC})	
L	L	Selected	D_{OUT}	Operating (I_{CC})	

NOTE:
1. X = H or L

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Supply voltage	V_{CC}	-0.3 to +7.0	V	1
Input voltage	V_{IN}	-0.3 to V_{CC} +0.3	V	
Output voltage	V_{OUT}	-0.3 to V_{CC} +0.3	V	
Operating temperature	Topr	0 to +70	°C	
Storage temperature	Tstg	-55 to +150	°C	

NOTE:
1. The maximum applicable voltage on any pin with respect to GND.

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	4.5	5.0	5.5	V

DC CHARACTERISTICS (V_{CC} = 5 V ±10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Input 'Low' voltage	V_{IL}		-0.3		0.8	V	
Input 'High' voltage	V_{IH}		2.2		V_{CC} +0.3	V	
Output 'Low' voltage	V_{OL}	I_{OL} = 3.2 mA			0.4	V	
Output 'High' voltage	V_{OH}	I_{OH} = -1.0 mA	2.4			V	
Input leakage current	$\|I_{LI}\|$	V_{IN} = 0 V or V_{CC}			10	µA	
Output leakage current	$\|I_{LO}\|$	V_{OUT} = 0 V or V_{CC}			10	µA	1
Operating current	I_{CC1}	t_{RC} = 55 ns			120	mA	2
	I_{CC2}	t_{RC} = 55 ns			110	mA	3
Standby current	I_{SB}	$\overline{CS}$ = V_{IH}			80	mA	

NOTES:
1. $\overline{CS}/\overline{OE}$ = V_{IH}
2. V_{IN} = V_{IH}/V_{IL}, $\overline{CS}$ = V_{IL}, outputs open
3. V_{IN} = (V_{CC} – 0.2 V), 0.2 V, $\overline{CS}$ = 0.2 V, outputs open

AC CHARACTERISTICS (V_{CC} = 5 V ±10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Read cycle time	t_{RC}	55			ns	
Address access time	t_{AA}			55	ns	
Chip select time	t_{ACS}			55	ns	
Output enable time	t_{OE}			25	ns	
Output hold time	t_{OH}	0			ns	
CE to output in High-Z	t_{CHZ}			25	ns	1
OE to output in High-Z	t_{OHZ}			25	ns	

NOTE:
1. This is the time required for the outputs to become high-impedance.

AC TEST CONDITIONS

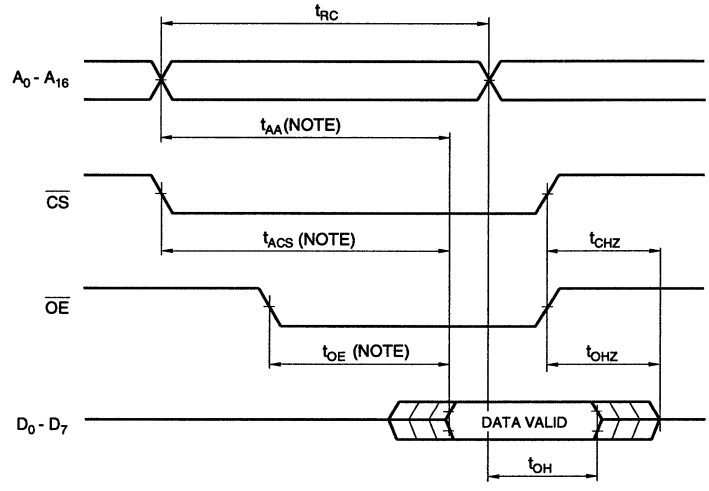
PARAMETER	RATING
Input voltage amplitude	0 V to 3.0 V
Input rise/fall time	5 ns
Input reference level	1.5 V
Output load condition	1TTL + 30 pF

CAPACITANCE (V_{CC} = 5 V ±10%, f = 1 MHz, T_A = 25°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Input capacitance	C_{IN}			10	pF
Output capacitance	C_{OUT}			10	pF

CAUTION

To stablize the power supply, it is recommended that a high-frequency bypass capacitor be connected between the V_{CC} pin and the GND pin.

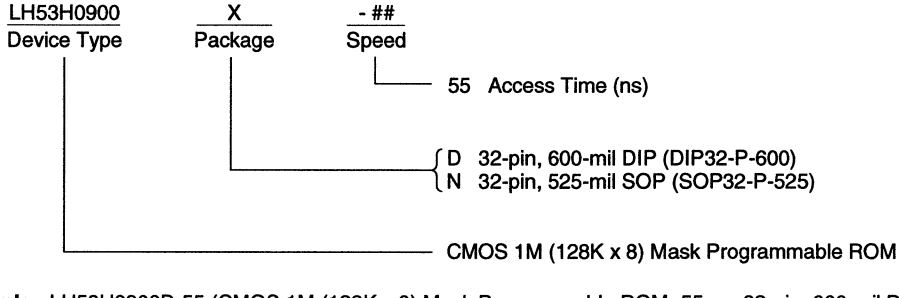


NOTE: Data becomes valid after the intervals t_{AA}, t_{ACS}, and t_{OE} from address input and output enable input respectively, have been met.

53H0900-3

Figure 3. Timing Diagram

ORDERING INFORMATION



Example: LH53H0900D-55 (CMOS 1M (128K x 8) Mask Programmable ROM, 55 ns, 32-pin, 600-mil DIP)

53H0900-4

LH530800A CMOS 1M (128K × 8) Mask-Programmable ROM

FEATURES

- 131,072 × 8 bit organization
- Access time: 150 ns (MAX.)
- Power consumption:
  Operating: 193 mW (MAX.)
  Standby: 550 μW (MAX.)
- Fully-static operation
- TTL compatible I/O
- Three-state outputs
- Single +5 V power supply
- Packages:
  32-pin, 600-mil DIP
  32-pin, 525-mil SOP
  44-pin, 10 × 10 mm^2 QFP
- JEDEC standard EPROM pinout (DIP)

DESCRIPTION

The LH530800A is a mask-programmable ROM organized as 131,072 × 8 bits (1,048,576 bits). It is fabricated using silicon-gate CMOS process technology.

PIN CONNECTIONS

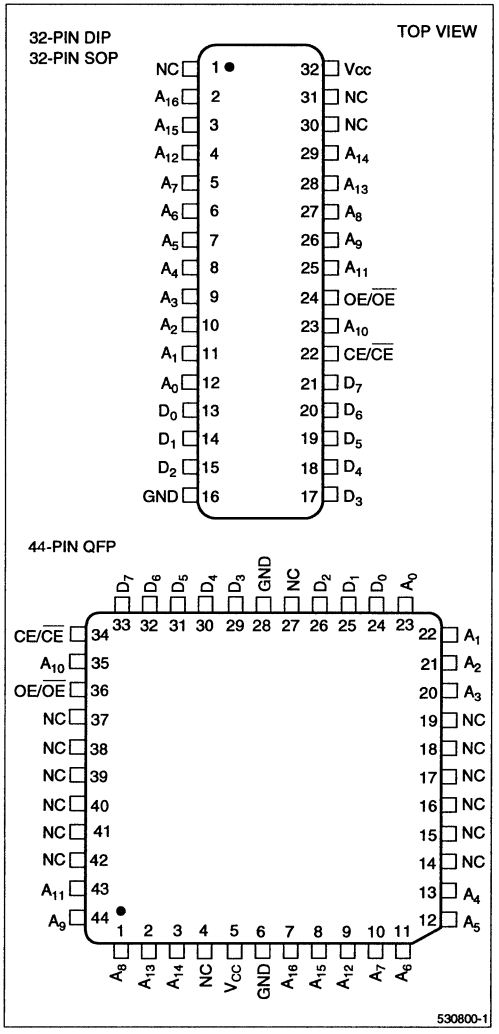


Figure 1. Pin Connections for DIP, SOP, and QFP Packages

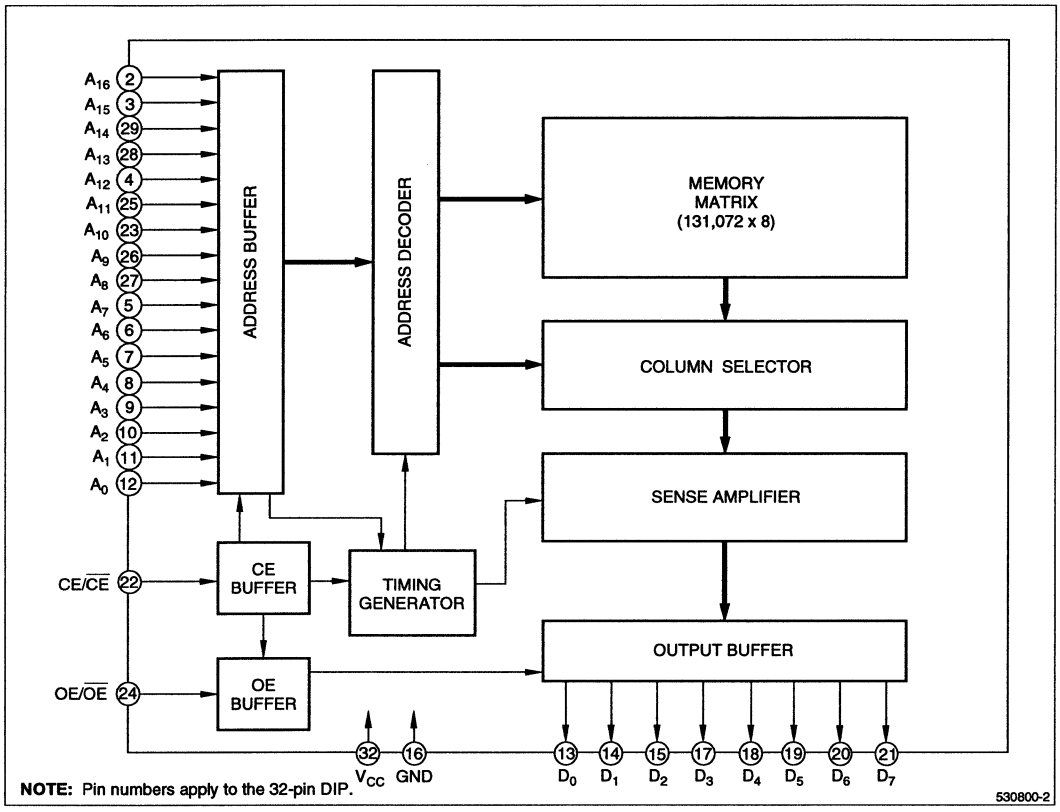


Figure 2. LH530800A Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME	NOTE
A_0 - A_{16}	Address input	
D_0 - D_7	Data Output	
CE/$\overline{CE}$	Chip enable input	1

SIGNAL	PIN NAME	NOTE
OE/$\overline{OE}$	Output enable input	1
V_{CC}	Power supply (+5 V)	
GND	Ground	

NOTE:
1. Active levels of CE/$\overline{CE}$ and OE/$\overline{OE}$ are mask-programmable.

TRUTH TABLE

CE/$\overline{CE}$	OE/$\overline{OE}$	MODE	D_0 - D_7	SUPPLY CURRENT	NOTE
L/H	X	Non selected	High-Z	Standby (I_{SB})	1
H/L	L/H	Non selected	High-Z	Operating (I_{CC})	
H/L	H/L	Selected	D_{OUT}	Operating (I_{CC})	

NOTE:
1. X = H or L

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Supply voltage	V_{CC}	-0.3 to +7.0	V	1
Input voltage	V_{IN}	-0.3 to V_{CC} +0.3	V	
Output voltage	V_{OUT}	-0.3 to V_{CC} +0.3	V	
Operating temperature	Topr	0 to +70	°C	
Storage temperature	Tstg	-55 to +150	°C	

NOTE:
1. The maximum applicable voltage on any pin with respect to GND.

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	4.5	5.0	5.5	V

DC CHARACTERISTICS (V_{CC} = 5 V ±10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Input 'Low' voltage	V_{IL}		-0.3		0.8	V	
Input 'High' voltage	V_{IH}		2.2		V_{CC} + 0.3	V	
Output 'Low' voltage	V_{OL}	I_{OL} = 1.6 mA			0.4	V	
Output 'High' voltage	V_{OH}	I_{OH} = -400 µA	2.4			V	
Input leakage current	$\|I_{LI}\|$	V_{IN} = 0 V to V_{CC}			10	µA	
Output leakage current	$\|I_{LO}\|$	V_{OUT} = 0 V to V_{CC}			10	µA	1
Operating current	I_{CC1}	t_{RC} = 150 ns			35	mA	2
	I_{CC2}	t_{RC} = 1 µs			25		
	I_{CC3}	t_{RC} = 150 ns			30	mA	3
	I_{CC4}	t_{RC} = 1 µs			20		
Standby current	I_{SB1}	CE = V_{IL}, $\overline{CE}$ = V_{IH}			2	mA	
	I_{SB2}	$\overline{CE}$ = V_{CC} - 0.2 V, CE = 0.2 V			100	µA	

NOTES:
1. $\overline{CE}/\overline{OE}$ = V_{IH} or CE/OE = V_{IL}
2. V_{IN} = V_{IH}/V_{IL}, $\overline{CE}$ = V_{IL}, CE = V_{IH}, outputs open
3. V_{IN} = (V_{CC} - 0.2 V) or 0.2 V, $\overline{CE}$ = 0.2 V, CE = V_{CC} - 0.2 V, outputs open

AC CHARACTERISTICS (V_{CC} = 5 V ±10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Read cycle time	t_{RC}	150			ns	
Address access time	t_{AA}			150	ns	
Chip enable time	t_{ACE}			150	ns	
Output enable time	t_{OE}	10		80	ns	
Output hold time	t_{OH}	5			ns	
CE to output in High-Z	t_{CHZ}			70	ns	1
OE to output in High-Z	t_{OHZ}			70	ns	

NOTE:
1. This is the time required for the output to become high-impedance.

AC TEST CONDITIONS

PARAMETER	RATING
Input voltage amplitude	0.6 V to 2.4 V
Input rise/fall time	10 ns
Input reference level	1.5 V
Output reference level	0.8 V and 2.2 V
Output load condition	1TTL +100 pF

CAPACITANCE (V_{CC} = 5 V ±10%, f = 1 MHz, T_A = 25°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Input capacitance	C_{IN}			10	pF
Output capacitance	C_{OUT}			10	pF

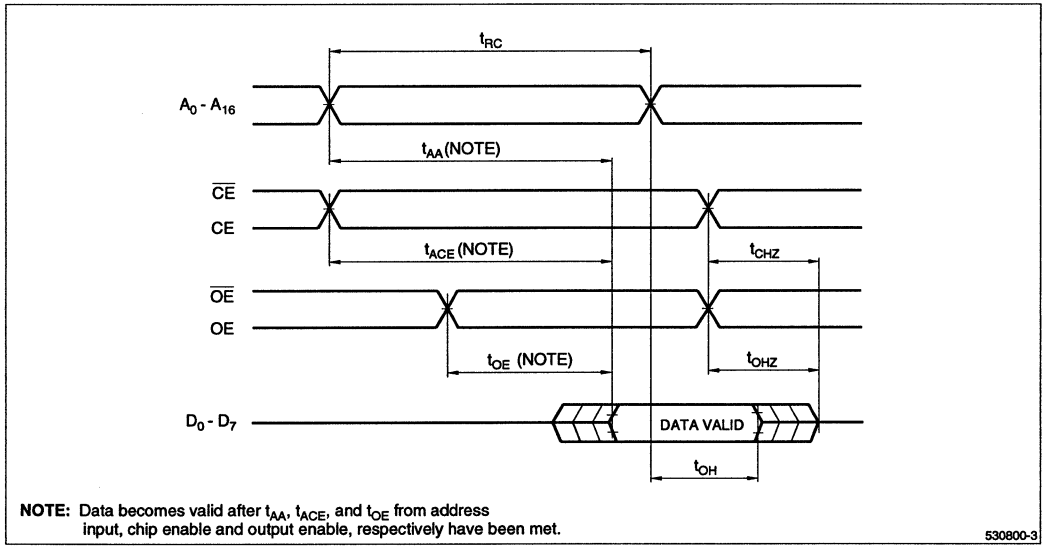
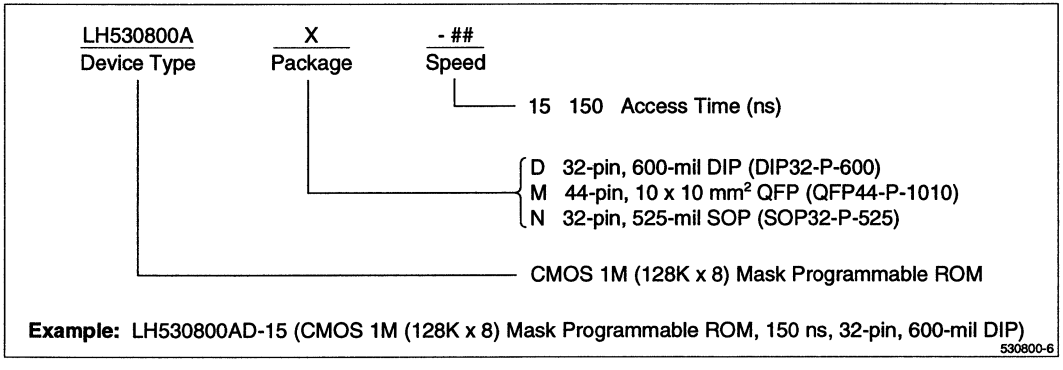


Figure 3. Timing Diagram

ORDERING INFORMATION



PRELIMINARY

LH530800A-Y

CMOS 1M (128K × 8)
Mask-Programmable ROM

FEATURES

- 131,072 × 8 bit organization
- Access time:
  500 ns (MAX.) at 2.6 V ≤ V_{CC} < 4.5 V
  150 ns (MAX.) at 4.5 V ≤ V_{CC} < 5.5 V
- Low-power consumption:
  Operating: 193 mW (MAX.)
  Standby: 550 µW (MAX.)
- Fully-static operation
- Three-state outputs
- Mask-programmable control pin:
  Pin 24 = OE/$\overline{OE}$
- Wide range power supply:
  2.6 V to 5.5 V
- Packages:
  32-pin, 600-mil DIP
  32-pin, 525-mil SOP
  44-pin, 10 × 10 mm^2 QFP

DESCRIPTION

The LH530800A-Y is a 1M-bit mask-programmable ROM organized as 131,072 × 8 bits. It is fabricated using silicon-gate CMOS process technology.

PIN CONNECTIONS

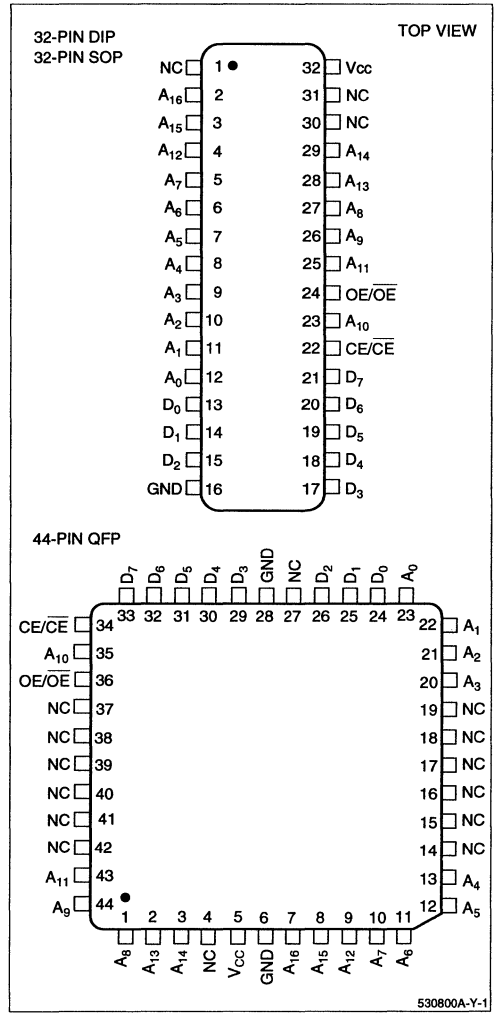


Figure 1. Pin Connections for DIP, SOP, and QFP Packages

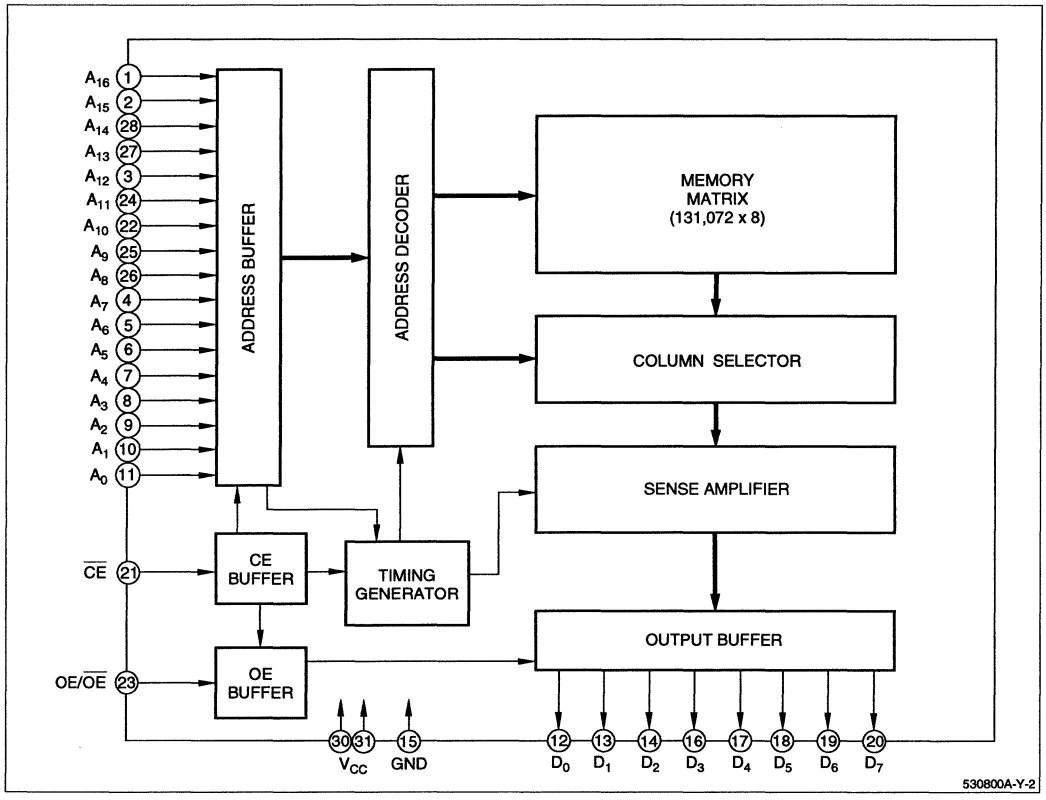


Figure 2. LH530800A-Y Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME	NOTE
A_0 - A_{16}	Address input	
D_0 - D_7	Data Output	
CE	Chip enable input	
OE/$\overline{OE}$	Output enable input	1

SIGNAL	PIN NAME	NOTE
V_{CC}	Power supply	
GND	Ground	
NC	Non connection	

NOTE:
1. Active levels of OE/$\overline{OE}$ are mask-programmable.

TRUTH TABLE

CE	OE/$\overline{OE}$	D_0 - D_7	SUPPLY CURRENT	NOTE
H	X	High-Z	Standby (I_{SB})	1
L	L/H	High-Z	Operating (I_{CC})	
L	H/L	D_{OUT}	Operating (I_{CC})	

NOTE:
1. X = H or L

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Supply voltage	V_{CC}	-0.3 to +7.0	V
Input voltage	V_{IN}	-0.3 to V_{CC} +0.3	V
Output voltage	V_{OUT}	-0.3 to V_{CC} +0.3	V
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to +70°C)

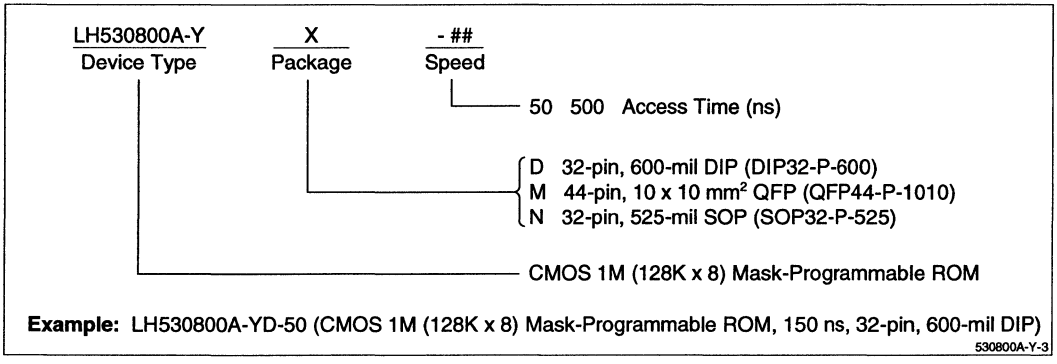
PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	2.6		5.5	V

DC CHARACTERISTICS (V_{CC} = 2.6 V to 5.5 V, T_A = 0 to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Input 'Low' voltage	V_{IL}		-0.3		0.4	V	
Input 'High' voltage	V_{IH}		0.8 × V_{CC}		V_{CC} + 0.3	V	
Output 'Low' voltage	V_{OL}	I_{OL} = 400 µA			0.4	V	
Output 'High' voltage	V_{OH}	I_{OH} = -100 µA	0.8 × V_{CC}			V	
Input leakage current	$\|I_{LI}\|$	V_{IN} = 0 V to V_{CC}			10	µA	
Output leakage current	$\|I_{LO}\|$	V_{OUT} = 0 V to V_{CC}			10	µA	1
Operating current	I_{CC1}	t_{RC} = 150 ns			35	mA	2
	I_{CC2}	t_{RC} = 500 ns			18	mA	3
	I_{CC3}	t_{RC} = 500 ns			12	mA	4
Standby current	I_{SB1}	$\overline{CE}$ = V_{IH}			2	mA	
	I_{SB2}	$\overline{CE}$ = V_{CC} - 0.2 V			100	µA	
Input capacitance	C_{IN}	f = 1 MHz, t_A = 25°C			10	pF	
Output capacitance	C_{OUT}				10	pF	

NOTES:
1. $\overline{CE}/\overline{OE}$ = V_{IH}, OE = V_{IL}, outputs open
2. 4.5 V ≤ V_{CC} ≤ 5.5 V
3. 3.4 V < V_{CC} < 4.5 V
4. 2.6 V ≤ V_{CC} ≤ 3.4 V

ORDERING INFORMATION



Example: LH530800A-YD-50 (CMOS 1M (128K x 8) Mask-Programmable ROM, 150 ns, 32-pin, 600-mil DIP)

530800A-Y-3

LH531000B CMOS 1M (128K × 8) Mask-Programmable ROM

FEATURES

- 131,072 × 8 bit organization
- Access time: 150 ns (MAX.)
- Low power consumption:
  Operating: 192.5 mW (MAX.)
  Standby: 550 μW (MAX.)
- Programmable CE/$\overline{CE}$ or OE/$\overline{OE}$
- Static operation (Internal sync. system)
- TTL compatible I/O
- Three-state outputs
- Single +5 V power supply
- Packages:
  28-pin, 600-mil DIP
  28-pin, 450-mil SOP
  44-pin, 14 × 14 mm^2 QFP
- Mask ROM specific pinout

DESCRIPTION

The LH531000B is a mask-programmable ROM organized as 131,072 × 8 bits. It is fabricated using silicon-gate CMOS process technology.

PIN CONNECTIONS

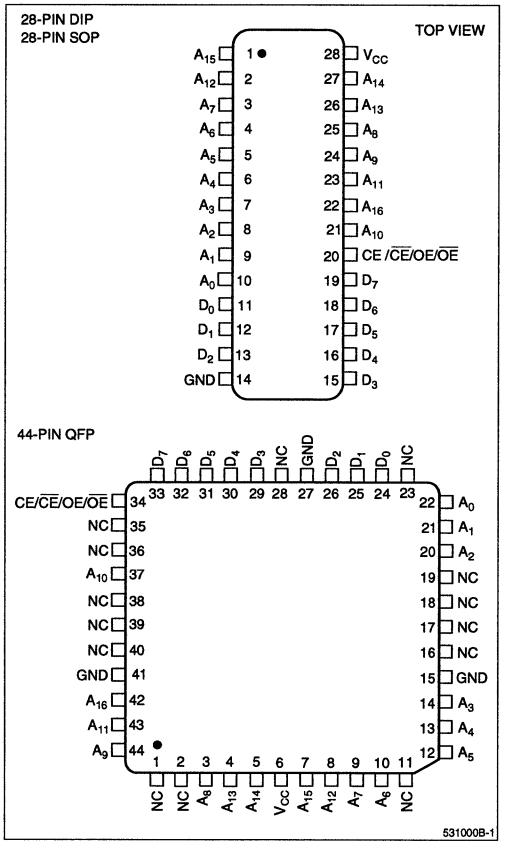


Figure 1. Pin Connections for DIP, SOP, and QFP Packages

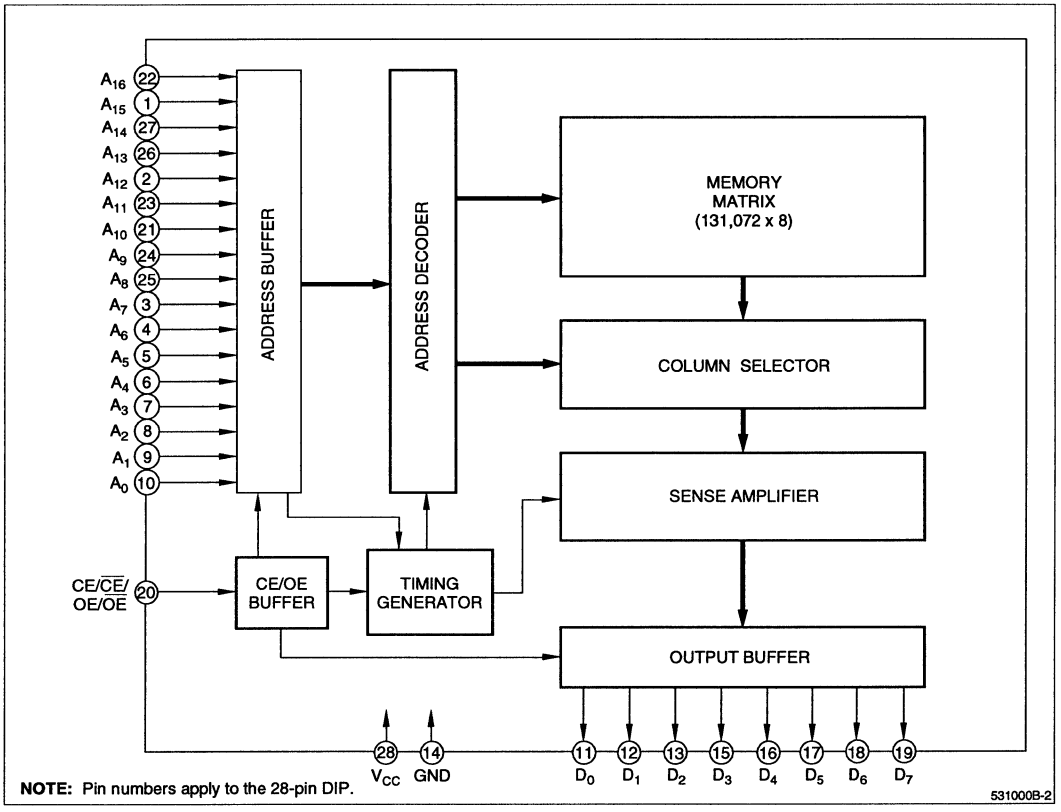


Figure 2. LH531000B Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME	NOTE
A_0 - A_{16}	Address input	
D_0 - D_7	Data output	
CE/$\overline{CE}$/OE/$\overline{OE}$	Chip Enable input or Output Enable input	1

SIGNAL	PIN NAME	NOTE
V_{CC}	Power supply (+5 V)	
GND	Ground	

NOTE:
1. Active level of CE/$\overline{CE}$ or OE/$\overline{OE}$ is mask-programmable.

TRUTH TABLE

PIN 20 (DIP/SOP) or PIN 34 (QFP)	CE/$\overline{CE}$	OE/$\overline{OE}$	MODE	D_0 - D_7	SUPPLY CURRENT
CE type	H/L	—	Selected	D_{OUT}	Operating (ICC)
	L/H	—	Non selected	High-Z	Standby (I_{SB})
OE type	—	H/L	Selected	D_{OUT}	Operating (ICC)
	—	L/H	Non selected	High-Z	

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Supply voltage	V_{CC}	-0.3 to +7.0	V	1
Input voltage	V_{IN}	-0.3 to V_{CC} +0.3	V	
Output voltage	V_{OUT}	-0.3 to V_{CC} +0.3	V	
Operating temperature	Topr	0 to +70	°C	
Storage temperature	Tstg	-55 to +150	°C	

NOTE:
1. The maximum applicable voltage on any pin with respect to GND.

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	4.5	5.0	5.5	V

DC CHARACTERISTICS (V_{CC} = 5 V ±10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Input 'Low' voltage	V_{IL}		-0.3		0.8	V	
Input 'High' voltage	V_{IH}		2.2		V_{CC} +0.3	V	
Output 'Low' voltage	V_{OL}	I_{OL} = 1.6 mA			0.4	V	
Output 'High' voltage	V_{OH}	I_{OH} = -400 µA	2.4			V	
Input leakage current	$\|I_{LI}\|$	V_{IN} = 0 V to V_{CC}			10	µA	
Output leakage current	$\|I_{LO}\|$	V_{OUT} = 0 V to V_{CC}			10	µA	1
Operating current	I_{CC1}	t_{RC} = 150 ns			35	mA	2
	I_{CC2}	t_{RC} = 1 µs			25		
	I_{CC3}	t_{RC} = 150 ns			30	mA	3
	I_{CC4}	t_{RC} = 1 µs			20		
Standby current	I_{SB1}	$\overline{CE}$ = V_{IH}, CE = V_{IL}			2	mA	4
	I_{SB2}	$\overline{CE}$ = V_{CC} - 0.2 V, CE = 0.2 V			100	µA	

NOTES:
1. CE/$\overline{OE}$ = V_{IL}, $\overline{CE}$/$\overline{OE}$ = V_{IH}
2. V_{IN} = V_{IH}/V_{IL}, CE = V_{IH}, $\overline{CE}$ = V_{IL} (CE type), outputs open
3. V_{IN} = (V_{CC} - 0.2 V) or 0.2 V. CE = V_{CC} - 0.2 V, $\overline{CE}$ = 0.2 V (CE type), outputs open
4. CE type only

AC CHARACTERISTICS (V_{CC} = 5 V ±10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Read cycle time	t_{RC}		150			ns	
Address access time	t_{AA}				150	ns	
Chip enable access time	t_{ACE}	CE type			150	ns	
Output enable time	t_{OE}	OE type	10		80	ns	
Output hold time	t_{OH}		5			ns	
CE to output in High-Z	t_{CHZ}	CE type			70	ns	1
OE to output in High-Z	t_{OHZ}	OE type			70	ns	

NOTE:
1. This is the time required for the output to become high-impedance.

AC TEST CONDITIONS

PARAMETER	RATING
Input voltage amplitude	0.6 V to 2.4 V
Input rise/fall time	10 ns
Input reference level	1.5 V
Output reference level	0.8 V and 2.2 V
Output load condition	1TTL +100 pF

CAPACITANCE (V_{CC} = 5 V ±10%, f = 1 MHz, T_A = 25°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Input capacitance	C_{IN}			10	pF
Output capacitance	C_{OUT}			10	pF

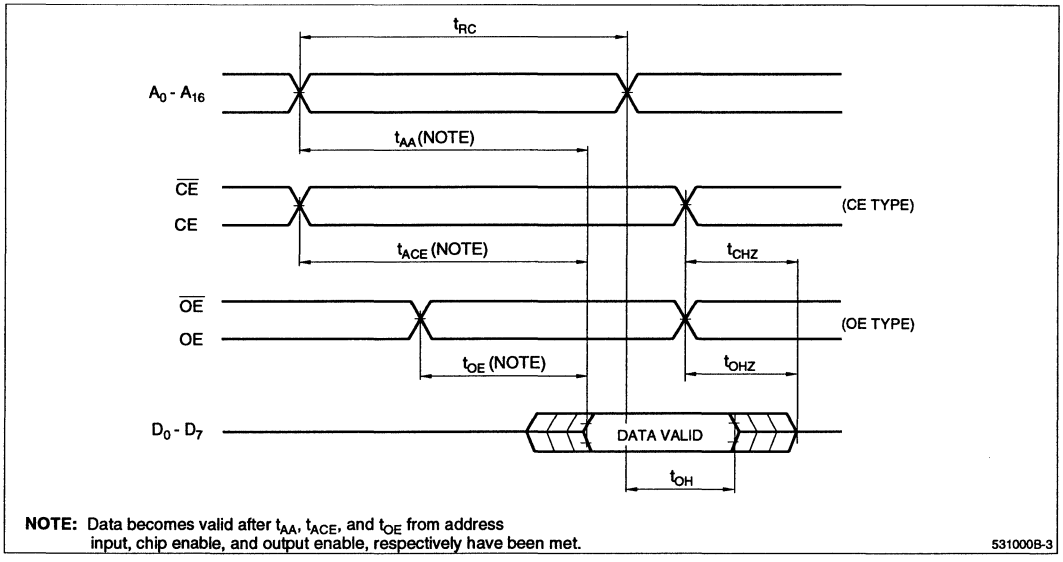
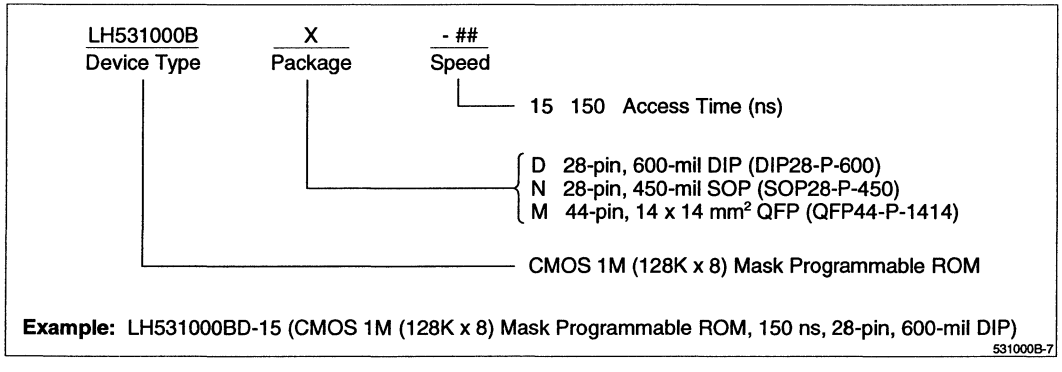


Figure 3. Timing Diagram

ORDERING INFORMATION



LH532000B

CMOS 2M (256K × 8/128K × 16) Mask-Programmable ROM

FEATURES

- Selectable memory organization:
  262,144 × 8 bit (byte mode)
  131,072 × 16 bit (word mode)
- $\overline{\text{BYTE}}$ input pin selects bit configuration
- Access time: 120/150 ns (MAX.)
- Low-power consumption:
  Operating: 275 mW (MAX.)
  Standby: 550 μW (MAX.)
- Programmable OE/$\overline{\text{OE}}$ and OE_1/$\overline{\text{OE}_1}$/DC
- Static operation (Internal sync. system)
- TTL compatible I/O
- Three-state outputs
- Single +5 V power supply
- Packages:
  40-pin, 600-mil DIP
  40-pin, 525-mil SOP
  48-pin, 12 × 18 mm^2 TSOP (Type I)
  44-pin, 14 × 14 mm^2 QFP
  44-pin, 10 × 10 mm^2 QFP
- ×16 word-wide pinout

DESCRIPTION

The LH532000B is a 2M bit mask-programmable ROM with two programmable memory organizations, byte and word modes. It is fabricated using silicon-gate CMOS process technology.

PIN CONNECTIONS

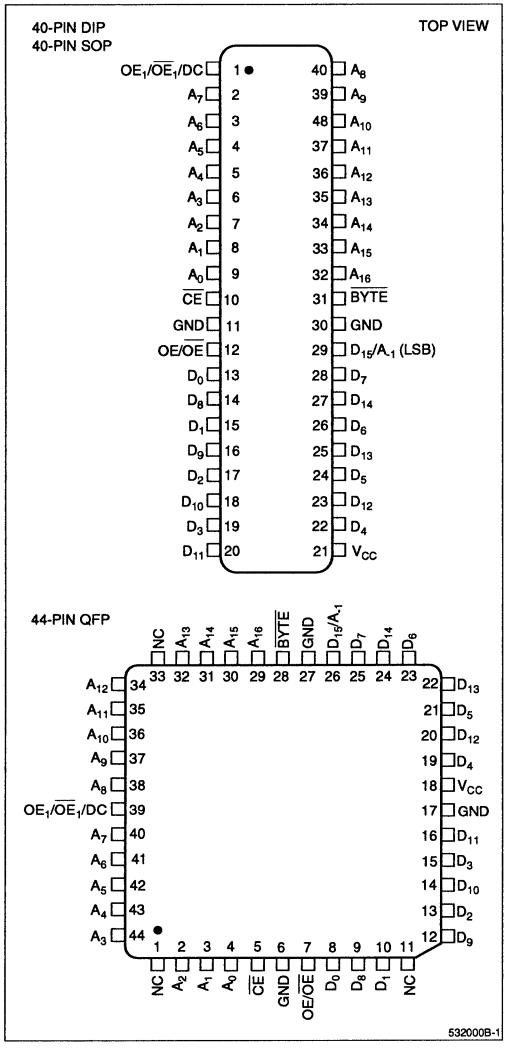


Figure 1. Pin Connections for DIP, SOP, and QFP Packages

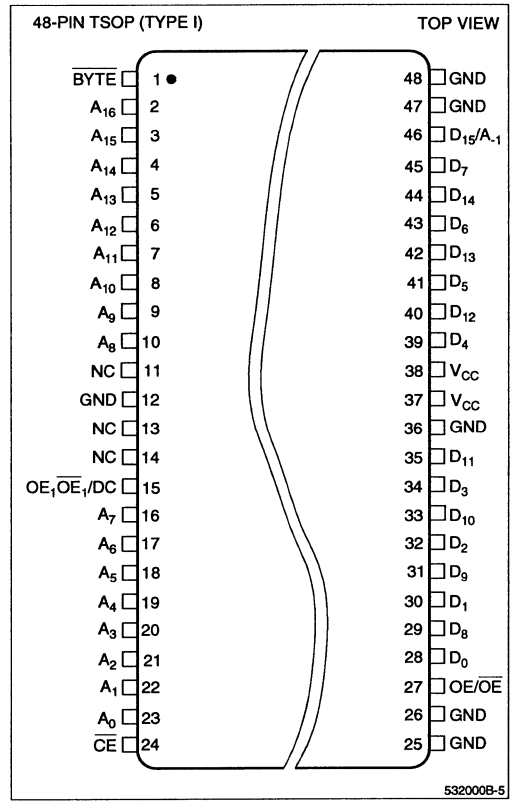


Figure 2. Pin Connections for TSOP Package

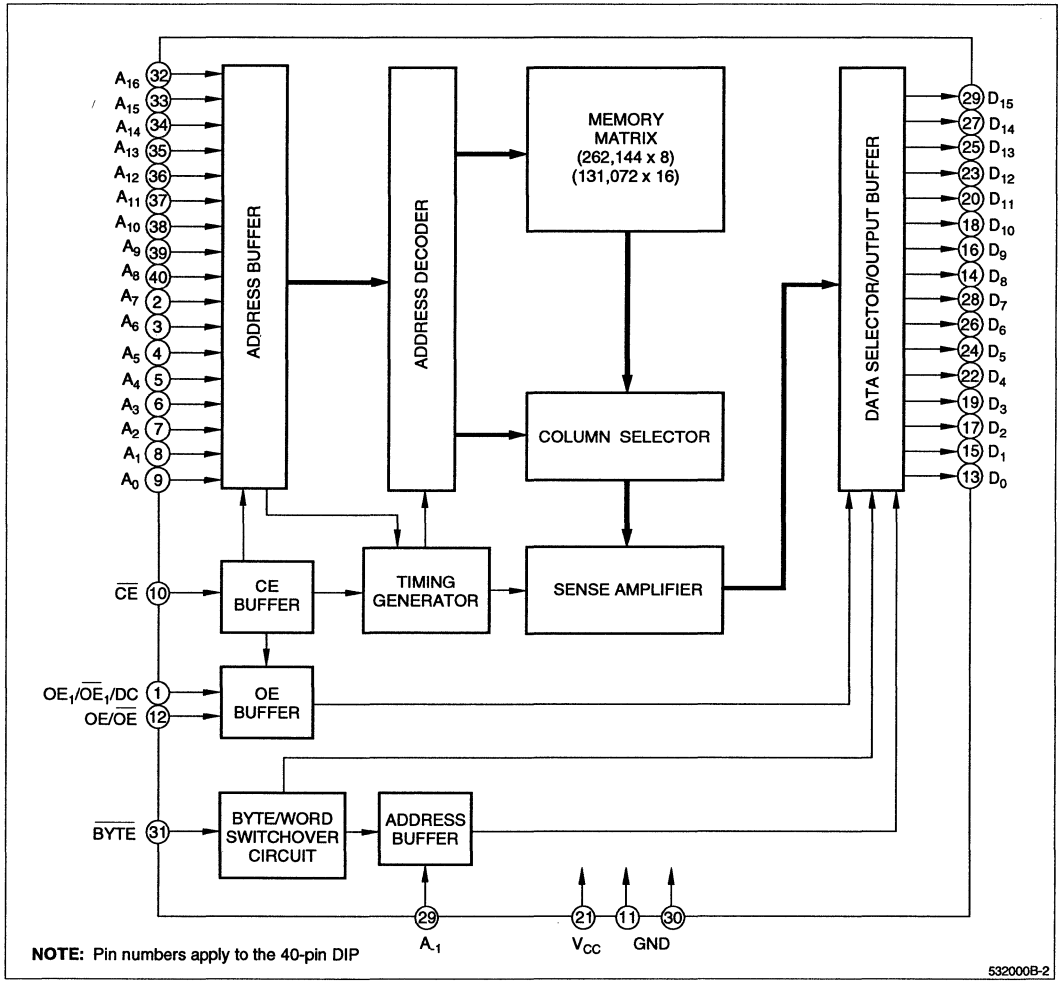


Figure 3. LH532000B Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME	NOTE
A_{-1}	Address input (BYTE mode)	1
A_0 - A_{16}	Address input	
D_0 - D_{15}	Data output	
$\overline{CE}$	Chip enable input	
OE/$\overline{OE}$	Output enable input	2

SIGNAL	PIN NAME	NOTE
$OE_1/\overline{OE_1}$/DC	Output enable input or Don't care	2
$\overline{BYTE}$	$\overline{BYTE}$/WORD switch	
V_{CC}	Power supply (+5 V)	
GND	Ground	

NOTES:

1. D_{15}/A_{-1} pin becomes LSB address input (A_{-1}) when the bit configuration is set in byte mode, and data output (D_{15}) when in word mode. $\overline{BYTE}$ input pin selects bit configuration.
2. The active levels of OE/$\overline{OE}$ and $OE_1/\overline{OE_1}$/DC are mask-programmable. Selecting DC allows the outputs to be active for both high and low levels applied to this pin. It is recommended to apply either a HIGH or a LOW to the DC pin.

TRUTH TABLE

$\overline{CE}$	$OE/\overline{OE}$	$OE_1/\overline{OE_1}$	$\overline{BYTE}$	A_{-1}	MODE	D_0 - D_7	D_8 - D_{15}	SUPPLY CURRENT
H	X	X	X	X	Non selected	High-Z		Standby (I_{SB})
L	L/H	X	X	X	Non selected	High-Z		Operating (I_{CC})
L	X	L/H	X	X	Non selected	High-Z		Operating (I_{CC})
L	H/L	H/L	H	Inhibit	Word	D_0 - D_7	D_8 - D_{15}	Operating (I_{CC})
L	H/L	H/L	L	L	Byte	D_0 - D_7	High-Z	Operating (I_{CC})
L	H/L	H/L	L	H	Byte	D_8 - D_{15}	High-Z	Operating (I_{CC})

NOTE:
1. X = H or L

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Supply voltage	V_{CC}	-0.3 to +7.0	V	1
Input voltage	V_{IN}	-0.3 to V_{CC} +0.3	V	
Output voltage	V_{OUT}	-0.3 to V_{CC} +0.3	V	
Operating temperature	Topr	0 to +70	°C	
Storage temperature	Tstg	-55 to +150	°C	

NOTE:
1. The maximum applicable voltage on any pin with respect to GND.

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	4.5	5.0	5.5	V

DC CHARACTERISTICS (V_{CC} = 5 V ±10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Input 'Low' voltage	V_{IL}		-0.3		0.8	V	
Input 'High' voltage	V_{IH}		2.2		V_{CC} +0.3	V	
Output 'Low' voltage	V_{OL}	I_{OL} = 2.0 mA			0.4	V	
Output 'High' voltage	V_{OH}	I_{OH} = -400 µA	2.4			V	
Input leakage current	$\lvert I_{LI} \rvert$	V_{IN} = 0 V to V_{CC}			10	µA	
Output leakage current	$\lvert I_{LO} \rvert$	V_{OUT} = 0 V to V_{CC}			10	µA	1
Operating current	I_{CC1}	t_{RC} = t_{RC} (MIN.)			50	mA	2
	I_{CC2}	t_{RC} = 1 µs			45		
	I_{CC3}	t_{RC} = t_{RC} (MIN.)			45	mA	3
	I_{CC4}	t_{RC} = 1 µs			40		
Standby current	I_{SB1}	$\overline{CE}$ = V_{IH}			3	mA	
	I_{SB2}	$\overline{CE}$ = V_{CC} - 0.2 V			100	µA	

NOTES:
1. OE/OE_1= V_{IL}, $\overline{CE}/\overline{OE}/\overline{OE_1}$= V_{IH}
2. V_{IN} = V_{IH}/V_{IL}, $\overline{CE}$ = V_{IL}, outputs open
3. V_{IN} = (V_{CC} - 0.2 V) or 0.2 V, $\overline{CE}$ = 0.2 V, outputs open

CAUTION

To stabilize the power supply, it is recommended that a high-frequency bypass capacitor be connected between the V_{CC} pin and the GND pin.

AC CHARACTERISTICS (V_{CC} = 5 V ±10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	MAX.	MIN.	MAX.	UNIT	NOTE
Read cycle time	t_{RC}	120		150		ns	
Address access time	t_{AA}		120		150	ns	
Chip enable access time	t_{ACE}		120		150	ns	
Output enable delay time	t_{OE}		55	10	70	ns	
Output hold time	t_{OH}	5		10		ns	
CE to output in High-Z	t_{CHZ}		55		70	ns	1
OE to output in High-Z	t_{OHZ}		55		70	ns	

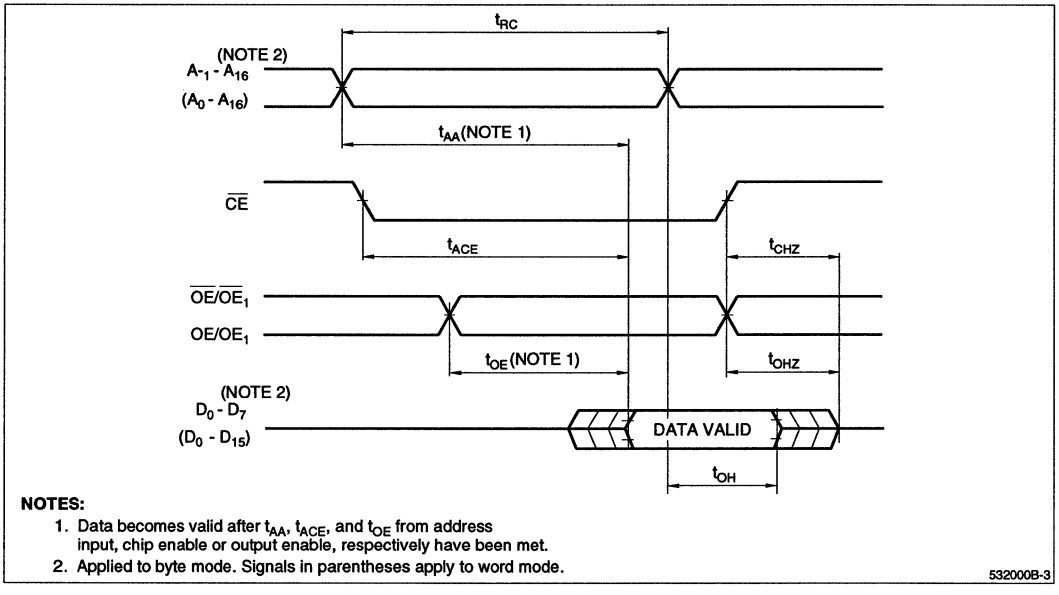
NOTE:
1. This is the time required for the output to become high-impedance.

AC TEST CONDITIONS

PARAMETER	RATING
Input voltage amplitude	0.6 V to 2.4 V
Input rise/fall time	10 ns
Input reference level	1.5 V
Output reference level	0.8 V and 2.2 V
Output load condition	1TTL +100 pF

CAPACITANCE (V_{CC} = 5 V ±10%, f = 1 MHz, T_A = 25°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Input capacitance	C_{IN}			10	pF
Output capacitance	C_{OUT}			10	pF

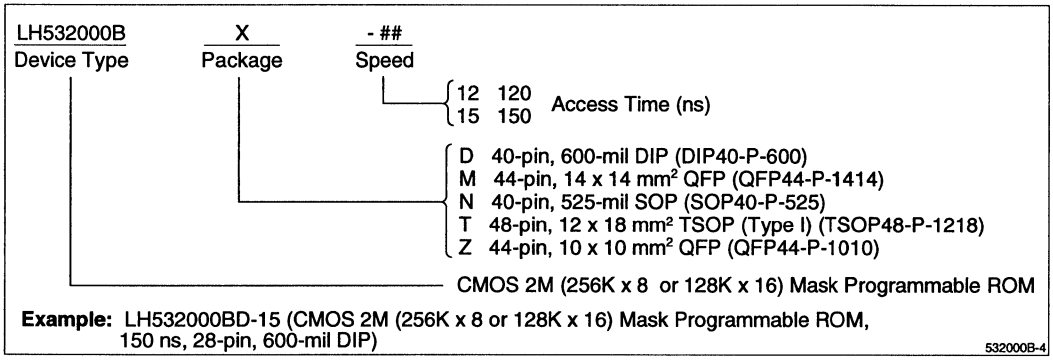


NOTES:
1. Data becomes valid after t_{AA}, t_{ACE}, and t_{OE} from address input, chip enable or output enable, respectively have been met.
2. Applied to byte mode. Signals in parentheses apply to word mode.

532000B-3

Figure 4. Timing Diagram

ORDERING INFORMATION



PRELIMINARY

LH532000B-S

CMOS 2M (256K × 8/128K × 16)
3 V-Drive Mask-Programmable ROM

FEATURES

- Low-power supply:
  2.6 to 5.5 V
- 262,144 × 8 bit organization
  (Byte mode)
  131,072 × 16 bit organization
  (Word mode)
- Access time:
  500 ns (MAX.) at 2.6 V ≤ V_{CC} < 4.5 V
  150 ns (MAX.) at 4.5 V ≤ V_{CC} ≤ 5.5 V
- Static operation
- Three-state outputs
- Packages:
  40-pin, 600-mil DIP
  40-pin, 525-mil SOP
  44-pin, 10 × 10 mm^2 QFP
  44-pin, 14 × 14 mm^2 QFP
  48-pin, 12 × 18 mm^2 TSOP (Type I)

DESCRIPTION

The LH532000B-S is a CMOS 4M-bit mask-programmable ROM organized as 262,144 × 8 bits (Byte mode) or 131,072 × 16 bits (Word mode) that can be selected by $\overline{BYTE}$ input pin.

It is suited for use in compact battery back-up systems due to be operated on 3 V power supply.

PIN CONNECTIONS

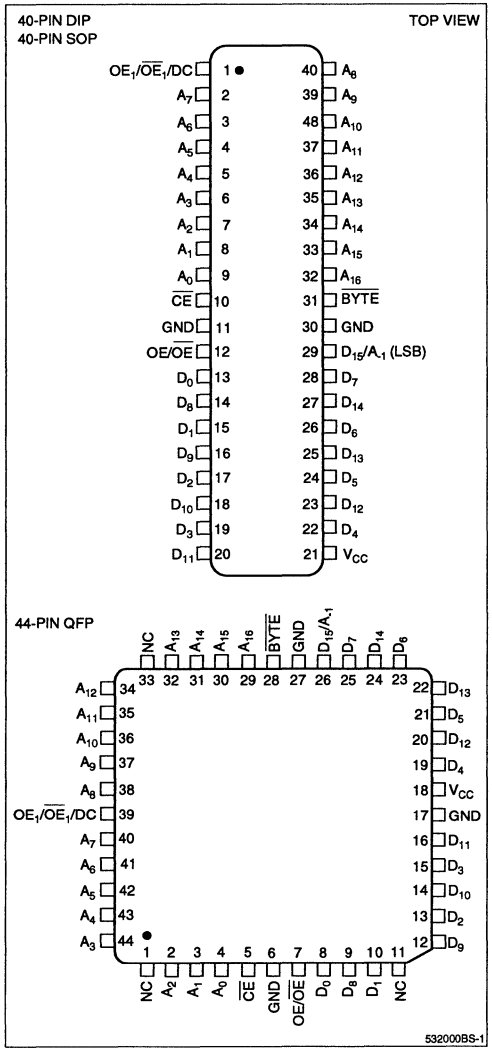


Figure 1. Pin Connections for DIP, SOP, and QFP Packages

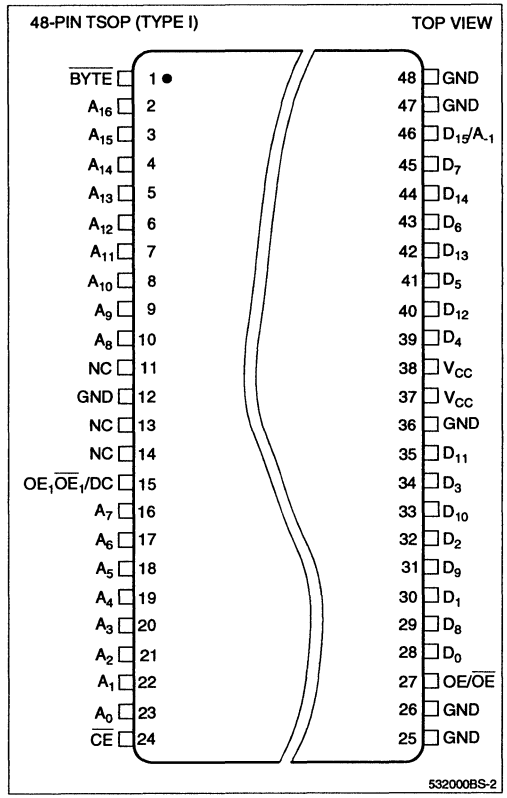


Figure 2. Pin Connections for TSOP Package

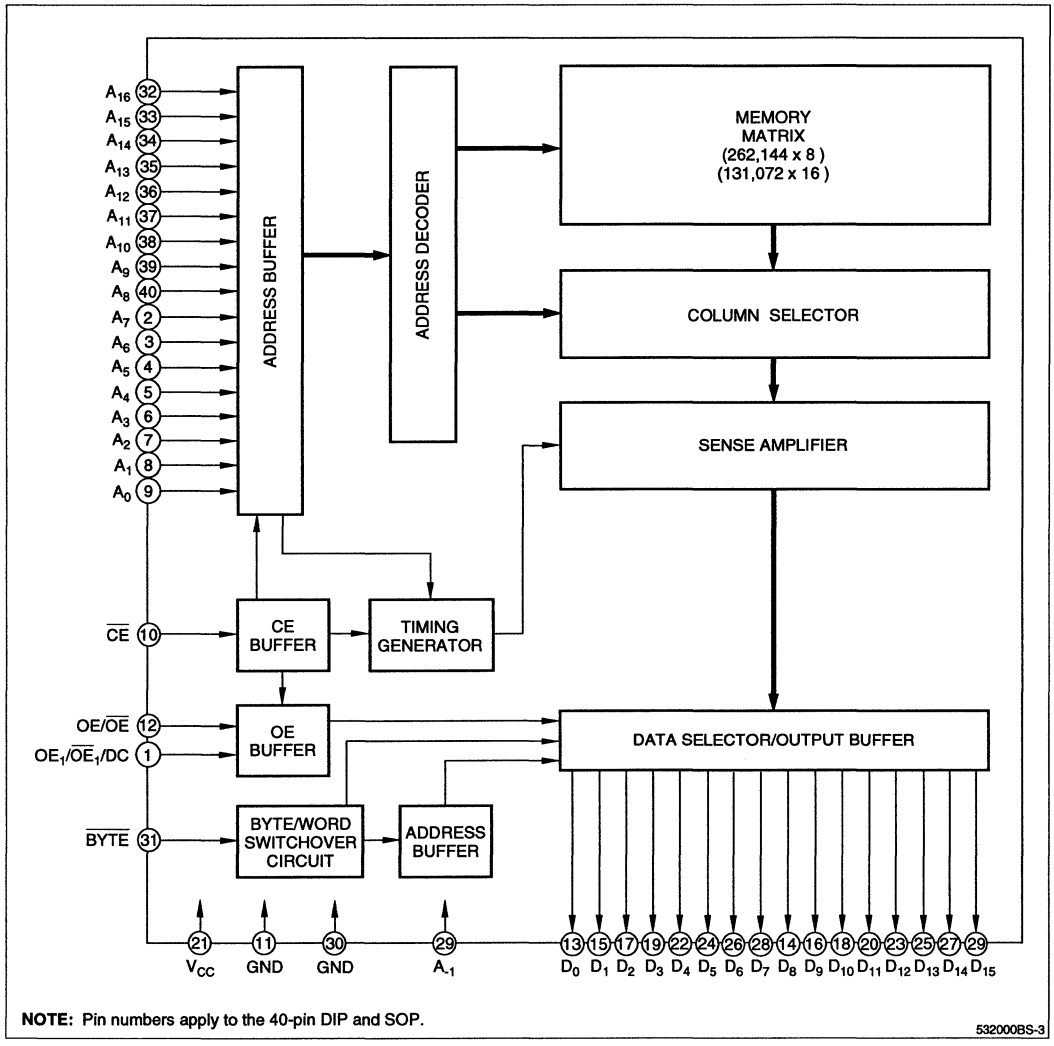


Figure 3. LH532000B-S Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME	NOTE
A_{-1} - A_{16}	Address input	
D_0 - D_{15}	Data output	
$\overline{BYTE}$	Byte/word switch	1
$\overline{CE}$	Chip enable input	2

SIGNAL	PIN NAME	NOTE
OE/$\overline{OE}$	Output enable input	2
$OE_1/\overline{OE}_1$/DC	Output enable input	2
V_{CC}	Power supply	
GND	Ground	

NOTES:

1. The D_{15}/A_{-1} pin becomes LSB address input (A_{-1}) when the $\overline{BYTE}$ pin is set to be LOW in byte mode, and data output (D_{15}) when set to be HIGH in word mode.
2. Active levels of OE/$\overline{OE}$ and $OE_1/\overline{OE}_1$/DC are mask-programmable.

TRUTH TABLE

$\overline{CE}$	OE/$\overline{OE}$	$OE_1/\overline{OE_1}$	$\overline{BYTE}$	A_{-1} (D_{15})	DATA OUTPUT		ADDRESS INPUT		SUPPLY CURRENT
					D_0 - D_7	D_8 - D_{15}	LSB	MSB	
H	X	X	X	X	High-Z	High-Z	–	–	Standby
L	L/H	X	X	X	High-Z	High-Z	–	–	Operating
L	X	L/H	X	X	High-Z	High-Z	–	–	Operating
L	H/L	H/L	H	–	D_0 - D_7	D_8 - D_{15}	A_0	A_{16}	Operating
L	H/L	H/L	L	L	D_0 - D_7	High-Z	A_{-1}	A_{16}	Operating
L	H/L	H/L	L	H	D_8 - D_{15}	High-Z	A_{-1}	A_{16}	Operating

NOTE:
X = Don't care, High-Z = High-impedance

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Supply voltage	V_{CC}	-0.3 to +7.0	V
Input voltage	V_{IN}	-0.3 to V_{CC} + 0.3	V
Output voltage	V_{OUT}	-0.3 to V_{CC} + 0.3	V
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	2.6		5.5	V

DC CHARACTERISTICS (V_{CC} = 2.6 to 5.5 V, T_A = 0 to +70°C)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	MAX.	UNIT	NOTE
Input 'High' voltage	V_{IH}		0.8V_{CC}	V_{CC} + 0.3	V	
Input 'Low' voltage	V_{IL}		-0.3	0.4	V	
Output 'High' voltage	V_{OH}	I_{OH} = -100 µA	0.8V_{CC}		V	
Output 'Low' voltage	V_{OL}	I_{OL} = 400 µA		0.4	V	
Input leakage current	$\lvert I_{LI} \rvert$	V_{IN} = 0 V to V_{CC}		10	µA	
Output leakage current	$\lvert I_{LO} \rvert$	V_{OUT} = 0 V to V_{CC}		10	µA	1
Operating current	I_{CC1}	t_{RC} = 150 ns		50	mA	2
	I_{CC2}	t_{RC} = 500 ns		35	mA	3
	I_{CC3}	t_{RC} = 500 ns		15	mA	4
Standby current	I_{SB1}	$\overline{CE}$ = V_{IH}		3	mA	
	I_{SB2}	$\overline{CE}$ = V_{CC} - 0.2 V		100	µA	
Input capacitance	C_{IN}	f = 1 MHz, T_A = +25°C		10	pF	
Output capacitance	C_{OUT}			10	pF	

NOTES:
1. $\overline{CE}$, $\overline{OE}$, $\overline{OE_1}$ = V_{IH}, OE, OE_1 = V_{IL}, outputs open
2. 4.5 V ≤ V_{CC} ≤ 5.5 V
3. 3.4 V < V_{CC} < 4.5 V
4. 2.6 V ≤ V_{CC} ≤ 3.4 V

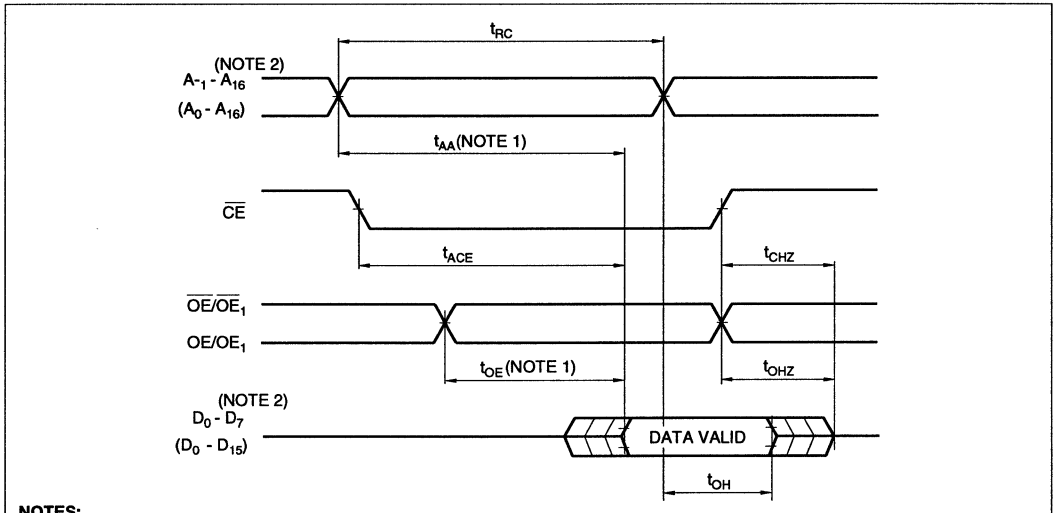
AC CHARACTERISTICS (V_{CC} = 2.6 to 5.5 V, T_A = 0 to +70°C)

PARAMETER	SYMBOL	2.6 ≤ V_{CC} < 4.5		4.5 ≤ V_{CC} ≤ 5.5		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.		
Read cycle time	t_{RC}	500		150		ns	
Address access time	t_{AA}		500		150	ns	
Chip enable time	t_{ACE}		500		150	ns	
Output enable time	t_{OE}		150		80	ns	
Output hold time	t_{OH}	10		10		ns	
CE to output in High-Z	t_{CHZ}		150		80	ns	1
OE to output in High-Z	t_{OHZ}		150		80	ns	

NOTE:
1. This is the time required for the outputs to become high-impedance.

AC TEST CONDITIONS

PARAMETER	RATING
Input voltage amplitude	0.4 to (0.8 × V_{CC}) V
Input rise/fall time	10 ns
Input/output reference level	1.5 V
Output load condition	1 TTL + 100 pF

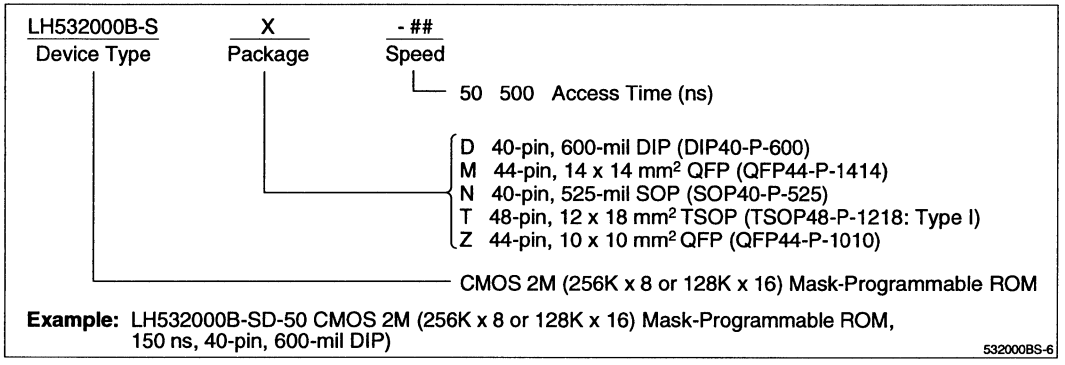


NOTES:
1. Data becomes valid after t_{AA}, t_{ACE}, and t_{OE} from address input, chip enable or output enable, respectively have been met.
2. Applied to byte mode. Signals in parentheses apply to word mode.

532000BS-4

Figure 4. Timing Diagram

ORDERING INFORMATION



LH532100B CMOS 2M (256K × 8) Mask-Programmable ROM

FEATURES

- 262,144 × 8 bit organization
- Access time: 120/150 ns (MAX.)
- Low-power consumption:
  Operating: 275 mW (MAX.)
  Standby: 550 µW (MAX.)
- Static operation (Internal sync. system)
- Mask-programmable OE/$\overline{OE}$ and $OE_1/\overline{OE_1}$
- TTL compatible I/O
- Three-state outputs
- Single +5 V power supply
- Packages:
  32-pin, 600-mil DIP
  32-pin, 525-mil SOP
  32-pin, 8 × 20 mm^2 TSOP (Type II)
- JEDEC standard EPROM pinout (DIP)

DESCRIPTION

The LH532100B is a mask-programmable ROM organized as 262,144 × 8 bits. It is fabricated using silicon-gate CMOS process technology.

PIN CONNECTIONS

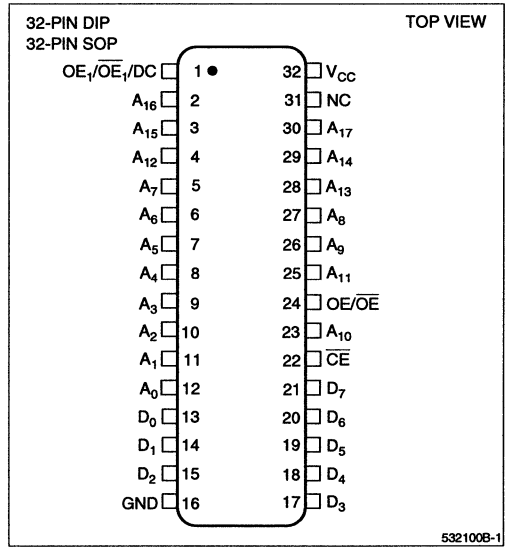


Figure 1. Pin Connections for DIP and SOP Packages

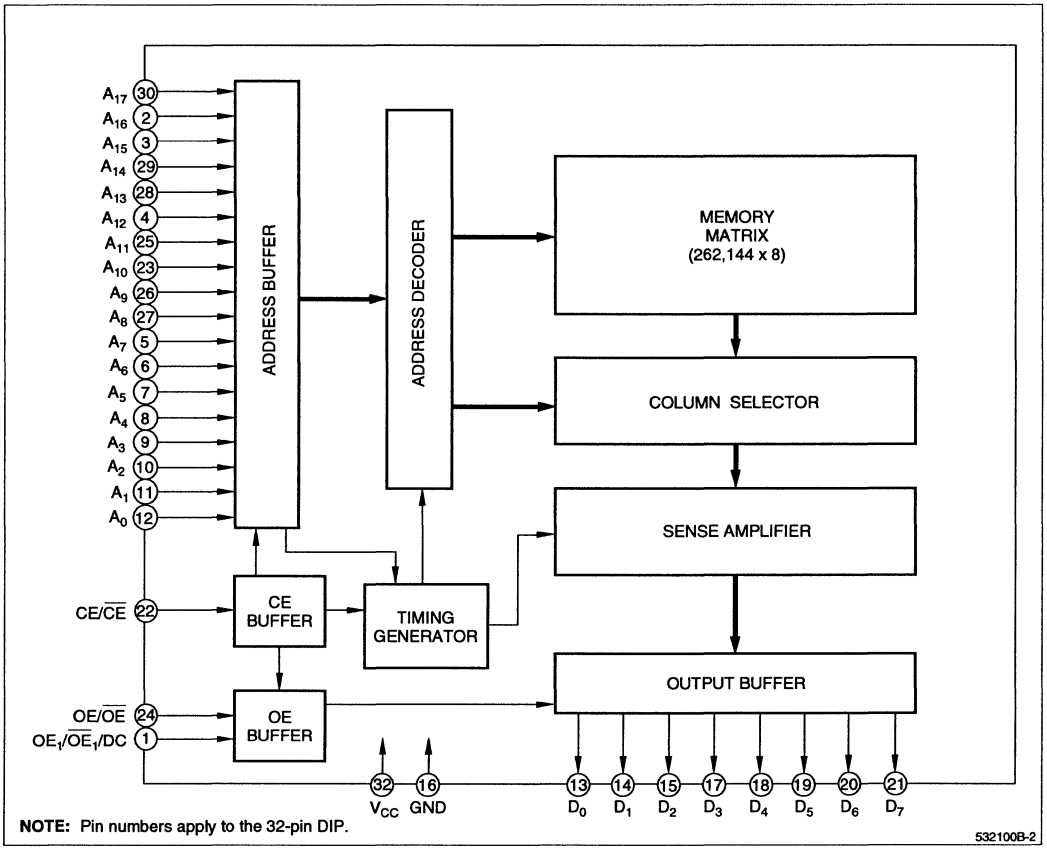


Figure 2. LH532100B Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME	NOTE
A_0 - A_{17}	Address input	
D_0 - D_7	Data output	
$\overline{CE}$	Chip Enable input	
OE/$\overline{OE}$	Output Enable input	1

SIGNAL	PIN NAME	NOTE
$OE_1/\overline{OE_1}$/DC	Output Enable input/ Don't Care connection	1
V_{CC}	Power supply (+5 V)	
GND	Ground	

NOTE:

1. Active levels of OE/$\overline{OE}$ and $OE_1/\overline{OE_1}$/DC are mask-programmable. Selecting DC allows the outputs to be active for both high and low levels applied to this pin. It is recommended to apply either a HIGH or a LOW to the DC pin.

TRUTH TABLE

$\overline{CE}$	OE/$\overline{OE}$	$OE_1/\overline{OE_1}$	MODE	D_0 - D_7	SUPPLY CURRENT
H	X	X	Non selected	High-Z	Standby (I_{SB})
L	L/H	X	Non selected	High-Z	Operating (I_{CC})
L	X	L/H	Non selected	High-Z	Operating (I_{CC})
L	H/L	H/L	Selected	D_{OUT}	Operating (I_{CC})

NOTE:
X = H or L

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Supply voltage	V_{CC}	-0.3 to +7.0	V	1
Input voltage	V_{IN}	-0.3 to V_{CC} +0.3	V	
Output voltage	V_{OUT}	-0.3 to V_{CC} +0.3	V	
Operating temperature	Topr	0 to +70	°C	
Storage temperature	Tstg	-55 to +150	°C	

NOTE:
1. The maximum applicable voltage on any pin with respect to GND.

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	4.5	5.0	5.5	V

DC CHARACTERISTICS (V_{CC} = 5 V ±10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Input 'Low' voltage	V_{IL}		-0.3		0.8	V	
Input 'High' voltage	V_{IH}		2.2		V_{CC} +0.3	V	
Output 'Low' voltage	V_{OL}	I_{OL} = 2.0 mA			0.4	V	
Output 'High' voltage	V_{OH}	I_{OH} = -400 µA	2.4			V	
Input leakage current	$\|I_{LI}\|$	V_{IN} = 0 V to V_{CC}			10	µA	
Output leakage current	$\|I_{LO}\|$	V_{OUT} = 0 V to V_{CC}			10	µA	1
Operating current	I_{CC1}	t_{RC} = 150 ns			50	mA	2
	I_{CC2}	t_{RC} = 1 µs			45		
	I_{CC3}	t_{RC} = 150 ns			45	mA	3
	I_{CC4}	t_{RC} = 1 µs			40		
Standby current	I_{SB1}	CE = V_{IL}, $\overline{CE}$ = V_{IH}			3	mA	
	I_{SB2}	$\overline{CE}$ = 0.2 V, $\overline{CE}$ = V_{CC} - 0.2 V			100	µA	

NOTES:
1. $\overline{CE}/\overline{OE}/\overline{OE}_1 = V_{IH}$ or $OE/OE_1 = V_{IL}$
2. $V_{IN} = V_{IH}/V_{IL}$, $\overline{CE} = V_{IL}$, outputs open
3. $V_{IN} = (V_{CC} - 0.2\ V)$ or 0.2 V, $\overline{CE}$ = 0.2 V, outputs open

AC CHARACTERISTICS (V_{CC} = 5 V ±10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	MAX.	MIN.	MAX.	UNIT	NOTE
Read cycle time	t_{RC}	120		150		ns	
Address access time	t_{AA}		120		150	ns	
Chip enable access time	t_{ACE}		120		150	ns	
Output enable delay time	t_{OE}		50	10	70	ns	
Output hold time	t_{OH}	5		10		ns	
CE to output in High-Z	t_{CHZ}		50		70	ns	1
OE to output in High-Z	t_{OHZ}		50		70	ns	

NOTE:
1. This is the time required for the outputs to become high-impedance.

CAUTION

To stabilize the power supply, it is recommended that a high-frequency bypass capacitor be connected between the V_{CC} pin and the GND pin.

AC TEST CONDITIONS

PARAMETER	RATING
Input voltage amplitude	0.6 V to 2.4 V
Input rise/fall time	10 ns
Input reference level	1.5 V
Output reference level	0.8 V and 2.2 V
Output load condition	1TTL +100 pF

CAPACITANCE (V_{CC} = 5 V ±10%, f = 1 MHz, T_A = 25°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Input capacitance	C_{IN}			10	pF
Output capacitance	C_{OUT}			10	pF

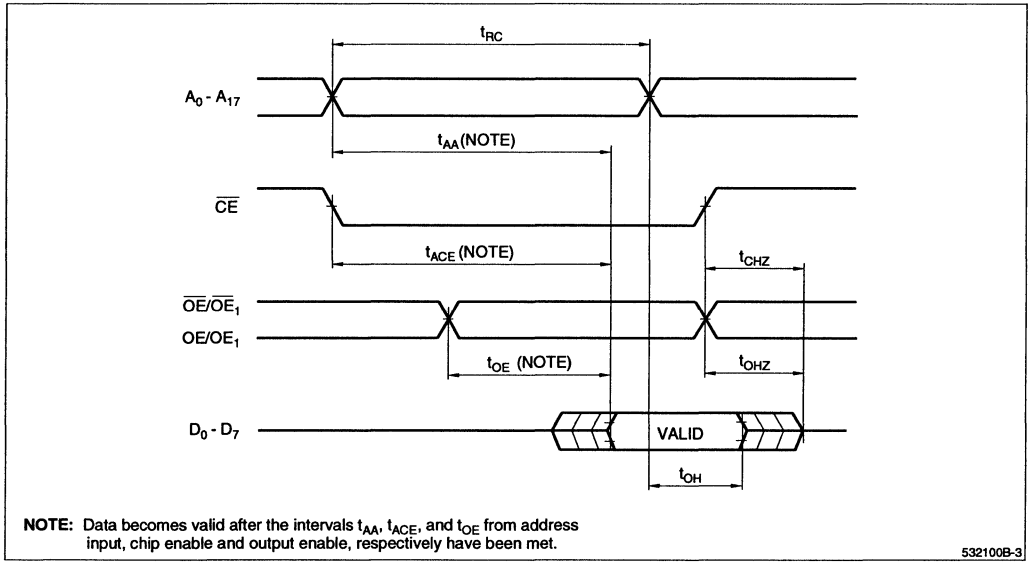
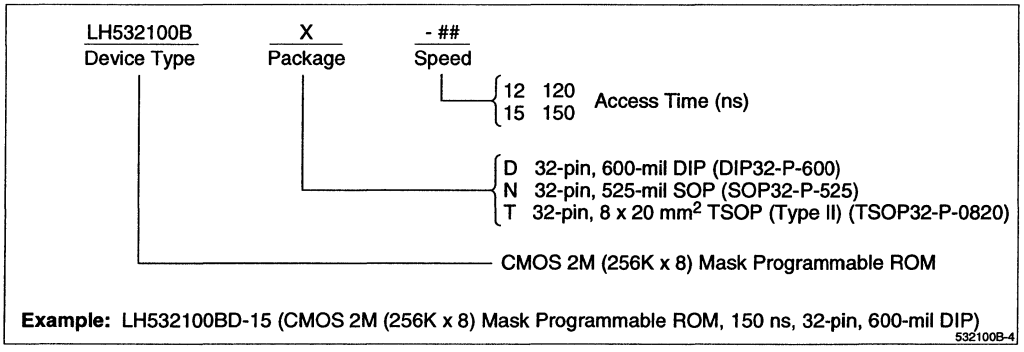


Figure 3. Timing Diagram

ORDERING INFORMATION



PRELIMINARY

LH53H4000/ LH53H4100

CMOS 4M (512K × 8 / 256K × 16) High-Speed Mask-Programmable ROM

CMOS 4M (512K × 8) High-Speed Mask-Programmable ROM

FEATURES

- LH53H4000
  524,288 × 8 / 262,144 × 16 bit organization
  LH53H4100
  524,288 × 8 bit organization
- Pin connections:
  LH53H4000 – × 8 / × 16 bit electrically-selectable type
  LH53H4100 – JEDEC standard pinout type
- TTL compatible I/O
- Three-state outputs
- Supply voltage: 5 V ±10%
- Access time: 80 ns (MAX.)
- Power consumption:
  Operating – 100 mA (MAX.)
  Standby – 100 µA (MAX.)
- Operating temperature:
  0 to +70°C
- Packages:
  LH53H4000
  40-pin, 600-mil DIP
  40-pin, 525-mil SOP
  48-pin, 12 × 18 mm^2 TSOP (Type I) (normal/reverse bend)
- Packages (cont'd)
  LH53H4100
  32-pin, 600-mil DIP
  32-pin, 525-mil SOP
  32-pin, 8 × 20 mm^2 TSOP (Type II) (normal/reverse bend)

DESCRIPTION

The required access time in the mask ROM market is now shifting from 150 ns to 120 ns, but some applications require a still faster access time of 100 ns or less.

The LH53H4000/LH53H4100 is a 4M mask-programmable ROM with access time of 80 ns, which is most suitable for those applications which require fast access time. The LH53H4000 is electrically switched between × 8/× 16 bit forms; the LH53H4100 conforms to the pin assignment specified by JEDEC.

APPLICATIONS

- Program memory and font memory in laser beam printers, ink jet printers, and word processors
- Program memory in personal computers
- Waveform data memory in electronic musical instruments
- Program memory and character memory in arcade games.

LH534K00 CMOS 4M (512K × 8) Mask-Programmable ROM

FEATURES

- 524,288 × 8 bit organization
- Access time: 150 ns (MAX.)
- Low-power consumption:
  Operating: 330 mW (MAX.)
  Standby: 550 µW (MAX.)
- Mask-programmable control pin:
  Pin 1 – $OE_1/\overline{OE}_1$/DC
  Pin 24 – OE/$\overline{OE}$
- Fully-static operation
- TTL compatible I/O
- Three-state outputs
- Single +5 V power supply
- Packages:
  32-pin, 600-mil DIP
  32-pin, 525 mil SOP
  32-pin, 8 × 20 mm^2 TSOP (Type II)

DESCRIPTION

The LH534K00 is a 4M-bit mask-programmable ROM organized as 524,288 × 8 bits. It is fabricated using silicon-gate CMOS process technology.

PIN CONNECTIONS

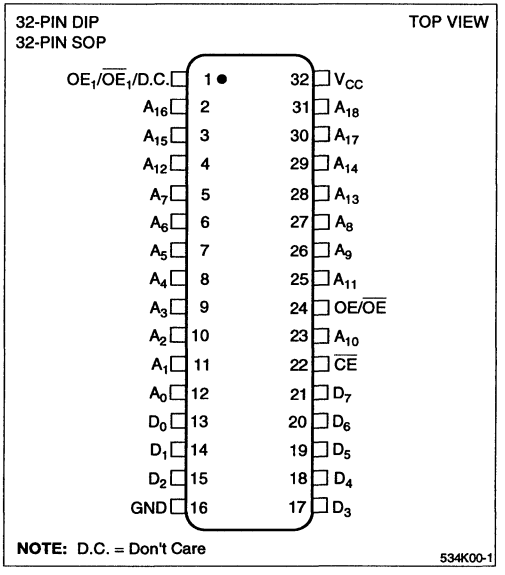


Figure 1. Pin Connections for DIP and SOP Packages

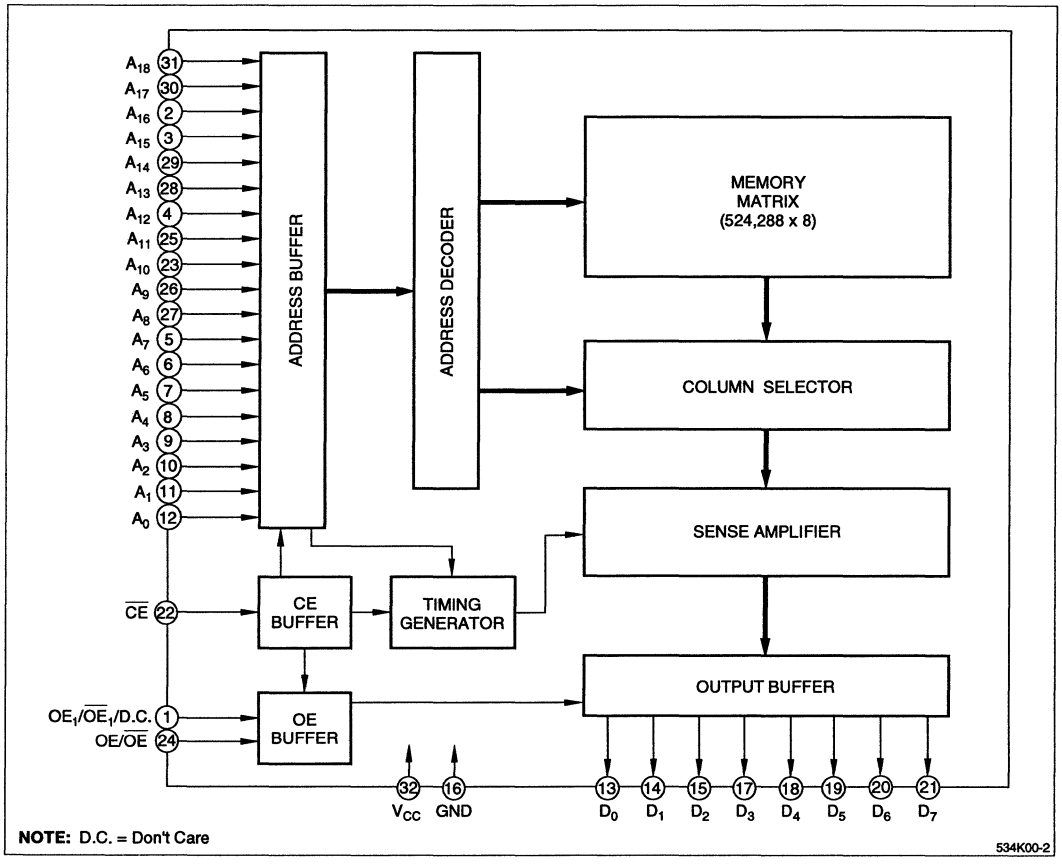


Figure 2. LH534K00 Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME	NOTE
A_0 - A_{18}	Address input	
D_0 - D_7	Data output	
$\overline{CE}$	Chip Enable input	
OE/$\overline{OE}$	Output Enable input	1

SIGNAL	PIN NAME	NOTE
$OE_1/\overline{OE}_1$/DC	Output Enable input/ Don't Care	1
V_{CC}	Power supply (+5 V)	
GND	Ground	

NOTES:

1. Active levels of $OE_1/\overline{OE}_1$/DC and OE/$\overline{OE}$ are mask-programmable. Selecting DC allows the outputs to be active for both high and low levels applied to this pin. It is recommended to apply either a HIGH or a LOW to the DC pin.

TRUTH TABLE

$\overline{CE}$	OE/$\overline{OE}$	$OE_1/\overline{OE_1}$	D_0 - D_7	SUPPLY CURRENT
H	X	X	High-Z	Standby (I_{SB})
L	L/H	X		Operating (I_{CC})
	X	L/H		
	H/L	H/L	Output	

NOTE:
X = H or L

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Supply voltage	V_{CC}	-0.3 to +7.0	V
Input voltage	V_{IN}	-0.3 to V_{CC} +0.3	V
Output voltage	V_{OUT}	-0.3 to V_{CC} +0.3	V
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	-55 to +150	°C

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	4.5	5.0	5.5	V

DC CHARACTERISTICS (V_{CC} = 5 V ±10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Input 'Low' voltage	V_{IL}		-0.3		0.8	V	
Input 'High' voltage	V_{IH}		2.2		V_{CC} +0.3	V	
Output 'Low' voltage	V_{OL}	I_{OL} = 2.0 mA			0.4	V	
Output 'High' voltage	V_{OH}	I_{OH} = -400 µA	2.4			V	
Input leakage current	$\lvert I_{LI} \rvert$	V_{IN} = 0 V to V_{CC}			10	µA	
Output leakage current	$\lvert I_{LO} \rvert$	V_{OUT} = 0 V to V_{CC}			10	µA	1
Operating current	I_{CC1}	t_{RC} = 150 ns			60	mA	2
	I_{CC2}	t_{RC} = 1 µs			50		
	I_{CC3}	t_{RC} = 150 ns			55	mA	3
	I_{CC4}	t_{RC} = 1 µs			45		
Standby current	I_{SB1}	$\overline{CE}$ = V_{IH}			3	mA	
	I_{SB2}	$\overline{CE}$ = V_{CC} - 0.2 V			100	µA	
Input capacitance	C_{IN}	f = 1 MHz, t_A = 25°C			10	pF	
Output capacitance	C_{OUT}				10	pF	

NOTES:
1. $\overline{CE}/\overline{OE}/\overline{OE_1}$ = V_{IH}, outputs open; OE/OE_1 = V_{IL}
2. V_{IN} = V_{IH}/V_{IL}, $\overline{CE}$ = V_{IL}, outputs open
3. V_{IN} = (V_{CC} - 0.2 V) or 0.2 V, $\overline{CE}$ = 0.2 V

CAUTION

To stabilize the power supply, it is recommended that a high-frequency bypass capacitor be connected between the V_{CC} pin and the GND pin.

AC CHARACTERISTICS (V_{CC} = 5 V ±10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT	NOTE
Read cycle time	t_{RC}	150		ns	
Address access time	t_{AA}		150	ns	
Chip enable time	t_{ACE}		150	ns	
Output enable time	t_{OE}		70	ns	
Output hold time	t_{OH}	5		ns	
CE to output in High-Z	t_{CHZ}		70	ns	1
OE to output in High-Z	t_{OHZ}		70	ns	

NOTE:
1. This is the time required for the outputs to become high-impedance.

AC TEST CONDITIONS

PARAMETER	RATING
Input voltage amplitude	0.6 V to 2.4 V
Input rise/fall time	10 ns
Input reference level	1.5 V
Output reference level	0.8 V and 2.2 V
Output load condition	1TTL + 100 pF

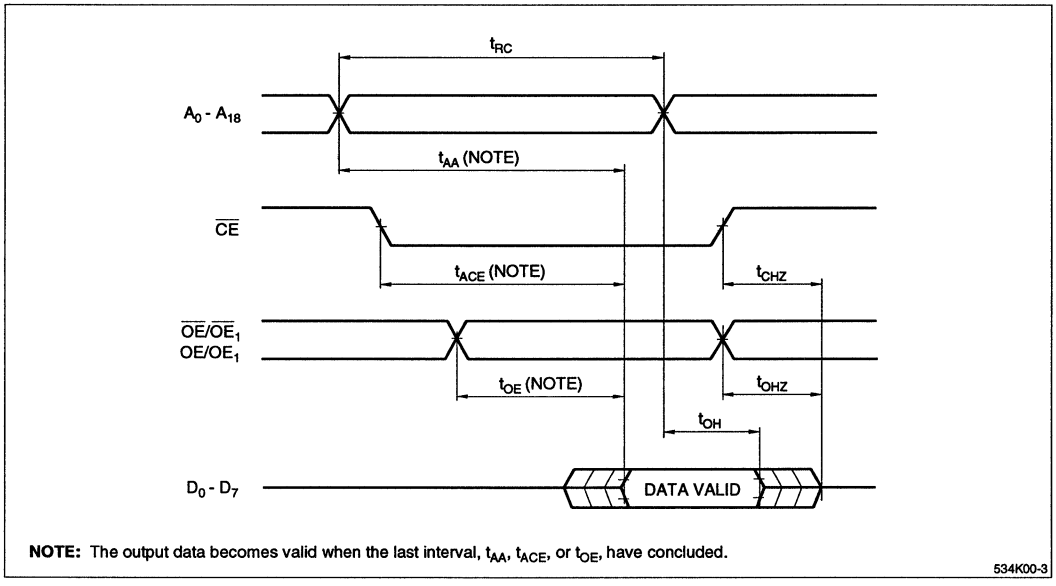
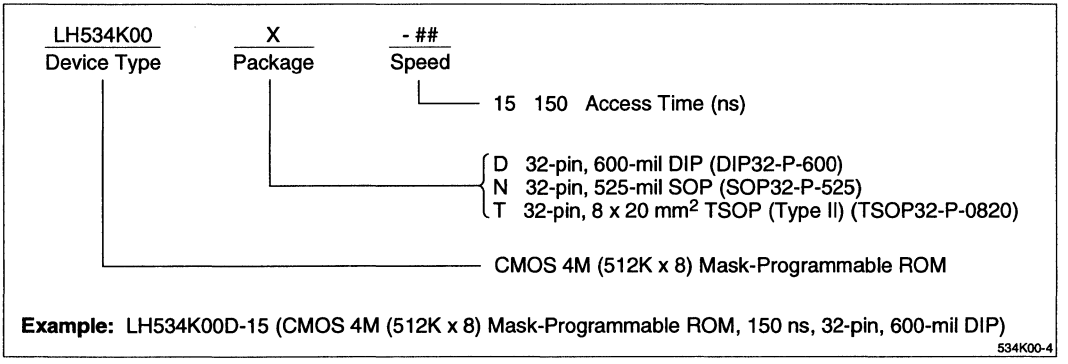


Figure 3. Timing Diagram

ORDERING INFORMATION



Example: LH534K00D-15 (CMOS 4M (512K x 8) Mask-Programmable ROM, 150 ns, 32-pin, 600-mil DIP)

534K00-4

LH534P00

CMOS 4M (512K × 8/256K × 16) Mask-Programmable ROM

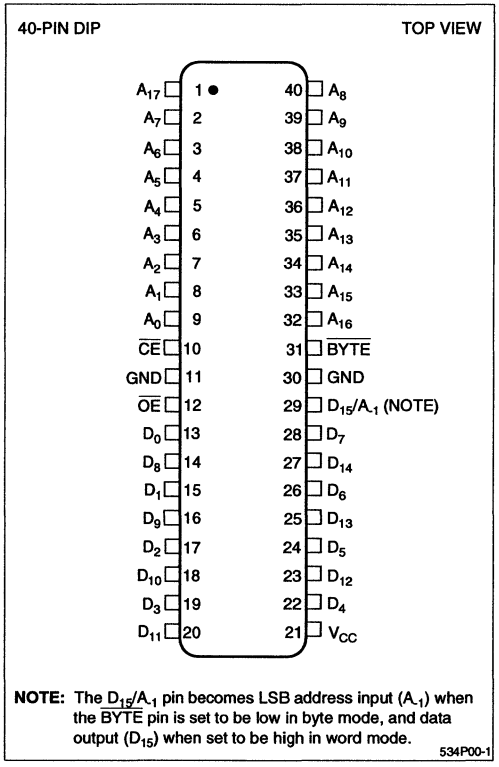
FEATURES

- 524,288 × 8 bit organization
  (Byte mode)
  262,144 × 16 bit organization
  (Word mode)
- Access time: 120 ns (MAX.)
- Power consumption:
  Operating: 358 mW (MAX.)
  Standby: 550 μW (MAX.)
- Static operation
- Three-state outputs
- Single +5 V power supply
- Packages:
  40-pin, 600-mil DIP
  40-pin, 525-mil SOP
  44-pin, 14 × 14 mm^2 QFP
  48-pin, 12 × 18 mm^2 TSOP (Type I)

DESCRIPTION

The LH534P00 is a CMOS 4M-bit mask-programmable ROM organized as 524,288 × 8 bits (Byte mode) or 262,144 × 16 bits (Word mode) that can be selected by $\overline{BYTE}$ input pin. It is fabricated using silicon-gate CMOS process technology.

PIN CONNECTIONS



NOTE: The D_{15}/A_{-1} pin becomes LSB address input (A_{-1}) when the $\overline{BYTE}$ pin is set to be low in byte mode, and data output (D_{15}) when set to be high in word mode.

534P00-1

Figure 1. Pin Connections for DIP Package

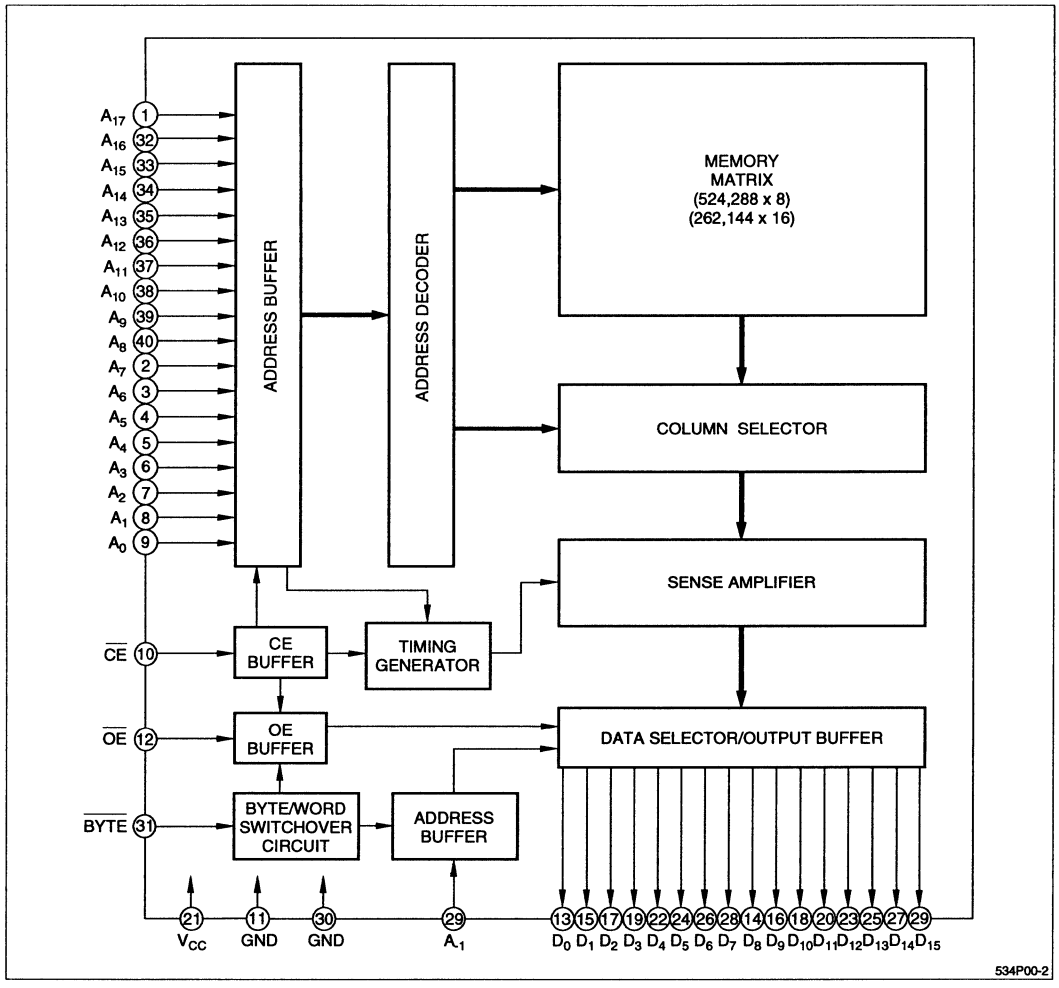


Figure 2. LH534P00 Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME
A_1 - A_{17}	Address input
D_0 - D_{15}	Data output
$\overline{CE}$	Chip enable input
$\overline{OE}$	Output enable input

SIGNAL	PIN NAME
$\overline{BYTE}$	Byte/word switch
V_{CC}	Power supply (+5 V)
GND	Ground

TRUTH TABLE

$\overline{CE}$	$\overline{OE}$	$\overline{BYTE}$	DATA OUTPUT		ADDRESS INPUT		SUPPLY CURRENT
			D_0 - D_7	D_8 - D_{15}	LSB	MSB	
H	X	X	High-Z	High-Z	–	–	Standby (I_{SB})
L	H	X	High-Z	High-Z	–	–	Operating (I_{CC})
L	L	H	D_0 - D_7	D_8 - D_{15}	A_0	A_{17}	Operating (I_{CC})
L	L	L	D_0 - D_7	High-Z	A_{-1}	A_{17}	Operating (I_{CC})

NOTE:
X = H or L

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Supply voltage	V_{CC}	-0.3 to +7.0	V
Input voltage	V_{IN}	-0.3 to V_{CC} +0.3	V
Output voltage	V_{OUT}	-0.3 to V_{CC} +0.3	V
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	4.5	5.0	5.5	V

DC CHARACTERISTICS (V_{CC} = 5 V ±10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Input 'Low' voltage	V_{IL}		-0.3		0.8	V	
Input 'High' voltage	V_{IH}		2.2		V_{CC} +0.3	V	
Output 'Low' voltage	V_{OL}	I_{OL} = 2.0 mA			0.4	V	
Output 'High' voltage	V_{OH}	I_{OH} = -400 µA	2.4			V	
Input leakage current	$\lvert I_{LI} \rvert$	V_{IN} = 0 V to V_{CC}			10	µA	
Output leakage current	$\lvert I_{LO} \rvert$	V_{OUT} = 0 V to V_{CC}			10	µA	1
Operating current	I_{CC1}	t_{RC} = 120 ns			65	mA	2
	I_{CC2}	t_{RC} = 1 µs			50		
	I_{CC3}	t_{RC} = 120 ns			60	mA	3
	I_{CC4}	t_{RC} = 1 µs			45		
Standby current	I_{SB1}	$\overline{CE}$ = V_{IH}			3	mA	
	I_{SB2}	$\overline{CE}$ = V_{CC} - 0.2 V			100	µA	
Input capacitance	C_{IN}	f = 1 MHz, t_A = 25°C			10	pF	
Output capacitance	C_{OUT}				10	pF	

NOTES:
1. $\overline{OE}$ = V_{IH}, $\overline{CE}$ = V_{IH}, outputs open
2. V_{IN} = V_{IH}/V_{IL}, $\overline{CE}$ = V_{IL}, outputs open
3. V_{IN} = (V_{CC} - 0.2 V) or 0.2 V, $\overline{CE}$ = 0.2 V, outputs open

CAUTION

To stabilize the power supply, it is recommended that a high-frequency bypass capacitor be connected between the V_{CC} pin and the GND pin.

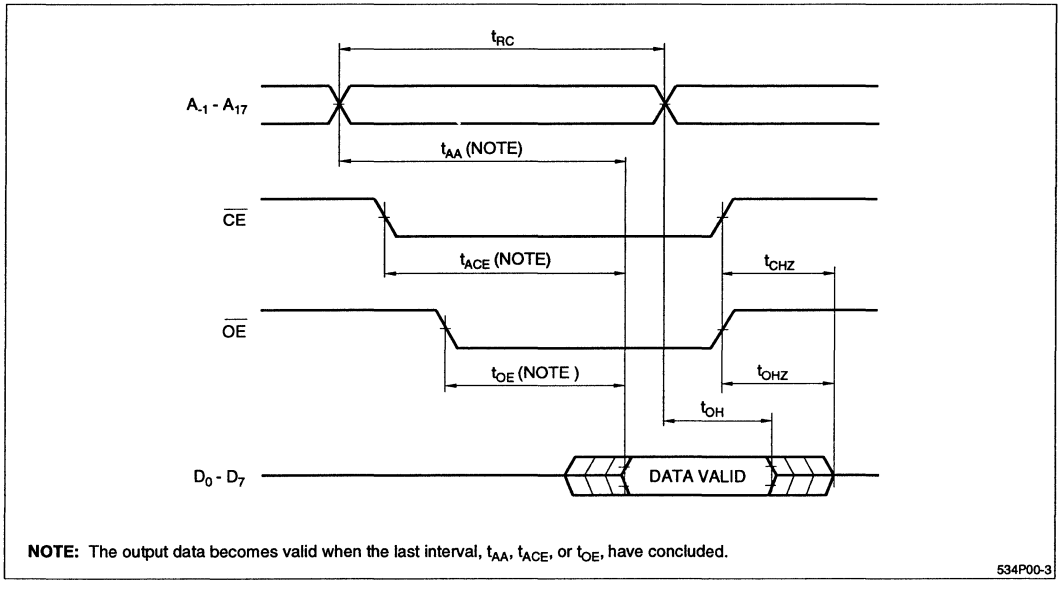
AC CHARACTERISTICS (V_{CC} = 5 V ±10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Read cycle time	t_{RC}	120			ns	
Address access time	t_{AA}			120	ns	
Chip enable time	t_{ACE}			120	ns	
Output enable time	t_{OE}			60	ns	
Output hold time	t_{OH}	5			ns	
CE to output in High-Z	t_{CHZ}			60	ns	1
OE to output in High-Z	t_{OHZ}			60	ns	

NOTE:
1. This is the time required for the outputs to become high-impedance.

AC TEST CONDITIONS

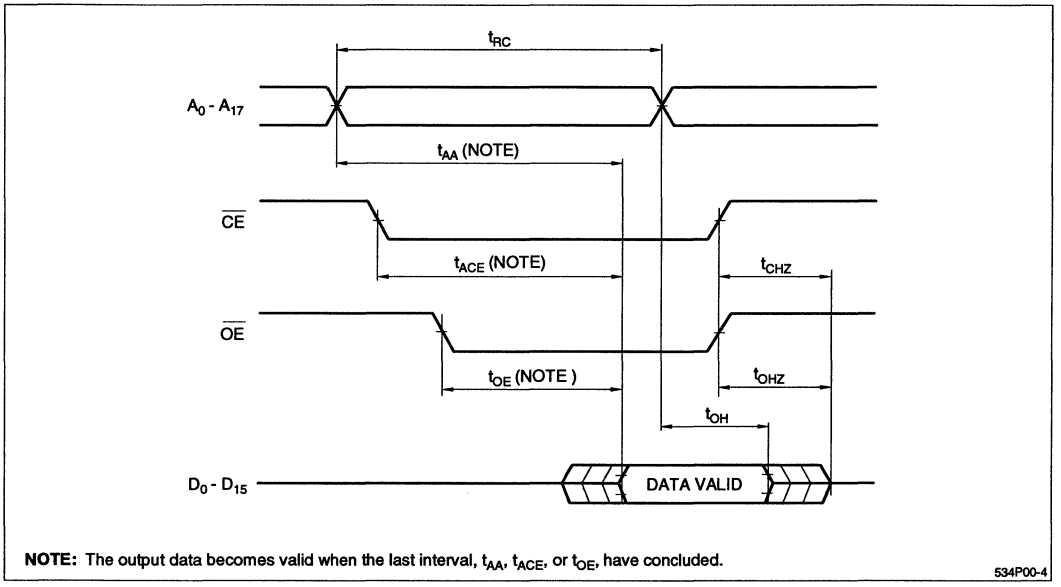
PARAMETER	RATING
Input voltage amplitude	0.4 V to 2.6 V
Input rise/fall time	10 ns
Input reference level	1.5 V
Output reference level	1.5 V
Output load condition	1TTL + 100 pF



NOTE: The output data becomes valid when the last interval, t_{AA}, t_{ACE}, or t_{OE}, have concluded.

534P00-3

Figure 3. Byte Mode ($\overline{BYTE}$ = V_{IL})



NOTE: The output data becomes valid when the last interval, t_{AA}, t_{ACE}, or t_{OE}, have concluded.

534P00-4

Figure 4. Word Mode ($\overline{BYTE}$ = V_{IH})

ORDERING INFORMATION

LH534P00	X	- ##
Device Type	Package	Speed

Speed: 12 120 Access Time (ns)

Package:
- D 40-pin, 600-mil DIP (DIP40-P-600)
- M 44-pin, 14 x 14 mm² QFP (QFP44-P-1414)
- N 40-pin, 525-mil SOP (SOP40-P-525)
- T 48-pin, 12 x 18 mm² TSOP (Type I) (TSOP48-P-1218)

Device Type: CMOS 4M (512K x 8 OR 256K x 16) Mask-Programmable ROM

Example: LH534P00D-12 (CMOS 4M (512K x 8) Mask-Programmable ROM, 120 ns, 40-pin, 600-mil DIP)

534P00-5

LH534R00

CMOS 4M (512K × 8) Mask-Programmable ROM

FEATURES

- 524,288 × 8 bit organization
- Access time: 120 ns (MAX.)
- Power consumption:
  Operating: 358 mW (MAX.)
  Standby: 550 µW (MAX.)
- Mask-programmable control pin:
  Pin 1 – $OE_1/\overline{OE}_1/DC$
  Pin 24 – $OE/\overline{OE}$
- Fully-static operation
- TTL compatible I/O
- Three-state outputs
- Single +5 V power supply
- Packages:
  32-pin, 600-mil DIP
  32-pin, 525-mil SOP
  32-pin, 8 × 20 mm^2 TSOP (Type II)

DESCRIPTION

The LH534R00 is a 4M-bit mask-programmable ROM organized as 524,288 × 8 bits. It is fabricated using silicon-gate CMOS process technology.

PIN CONNECTIONS

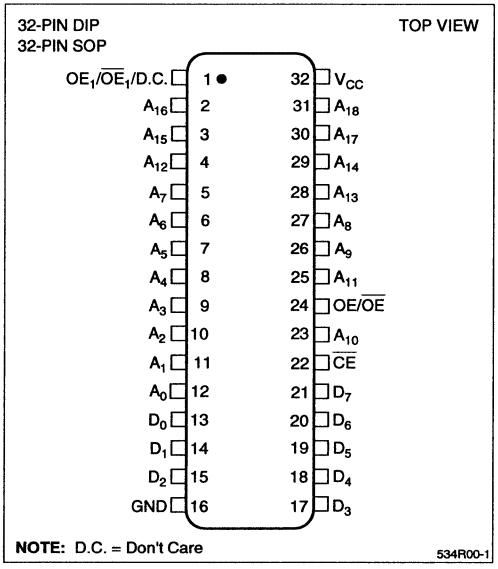


Figure 1. Pin Connections for DIP and SOP Packages

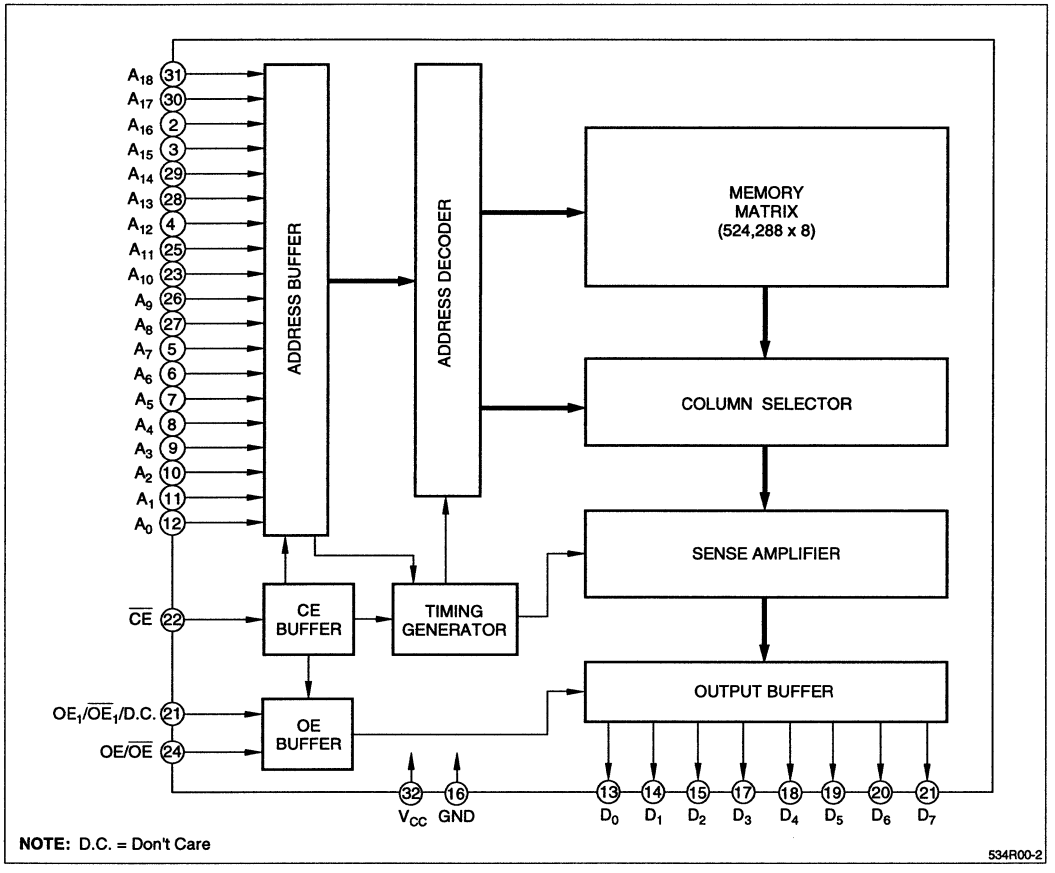


Figure 2. LH534R00 Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME	NOTE
A_0 - A_{18}	Address input	
D_0 - D_7	Data output	
$\overline{CE}$	Chip Enable input	
OE/$\overline{OE}$	Output Enable input	1

SIGNAL	PIN NAME	NOTE
$OE_1/\overline{OE_1}$/DC	Output Enable input/ Don't Care	1
V_{CC}	Power supply (+5 V)	
GND	Ground	

NOTE:

1. Active levels of $OE_1/\overline{OE_1}$/DC and OE/$\overline{OE}$ are mask-programmable. Selecting DC allows the outputs to be active for both high and low levels applied to this pin. It is recommended to apply either a HIGH or a LOW to the DC pin.

TRUTH TABLE

$\overline{CE}$	$OE_1/\overline{OE_1}$	$OE/\overline{OE}$	D_0 - D_7	SUPPLY CURRENT
H	X	X	High-Z	Standby (I_{SB})
L	L/H	X	High-Z	Operating (I_{CC})
L	X	L/H	High-Z	
L	H/L	H/L	Output	

NOTE:
X = H or L

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Supply voltage	V_{CC}	-0.3 to +7.0	V
Input voltage	V_{IN}	-0.3 to V_{CC} +0.3	V
Output voltage	V_{OUT}	-0.3 to V_{CC} +0.3	V
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	4.5	5.0	5.5	V

DC CHARACTERISTICS (V_{CC} = 5 V ±10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Input 'Low' voltage	V_{IL}		-0.3		0.8	V	
Input 'High' voltage	V_{IH}		2.2		V_{CC} +0.3	V	
Output 'Low' voltage	V_{OL}	I_{OL} = 2.0 mA			0.4	V	
Output 'High' voltage	V_{OH}	I_{OH} = -400 µA	2.4			V	
Input leakage current	$\lvert I_{LI} \rvert$	V_{IN} = 0 V to V_{CC}			10	µA	
Output leakage current	$\lvert I_{LO} \rvert$	V_{OUT} = 0 V to V_{CC}			10	µA	1
Operating current	I_{CC1}	t_{RC} = 120 ns			65	mA	2
	I_{CC2}	t_{RC} = 1 µs			50		
	I_{CC3}	t_{RC} = 120 ns			60	mA	3
	I_{CC4}	t_{RC} = 1 µs			45		
Standby current	I_{SB1}	$\overline{CE}$ = V_{IH}			3	mA	
	I_{SB2}	$\overline{CE}$ = V_{CC} - 0.2 V			100	µA	
Input capacitance	C_{IN}	f = 1 MHz, t_A = 25°C			10	pF	
Output capacitance	C_{OUT}				10	pF	

NOTES:
1. $\overline{OE}/\overline{OE_1}$ = V_{IH}, OE/OE_1 = V_{IL}, $\overline{CE}$ = V_{IH}, outputs open
2. V_{IN} = V_{IH}/V_{IL}, $\overline{CE}$ = V_{IL}, outputs open
3. V_{IN} = (V_{CC} - 0.2 V) or 0.2 V, $\overline{CE}$ = 0.2 V, outputs open

CAUTION

To stabilize the power supply, it is recommended that a high-frequency bypass capacitor be connected between the V_{CC} pin and the GND pin.

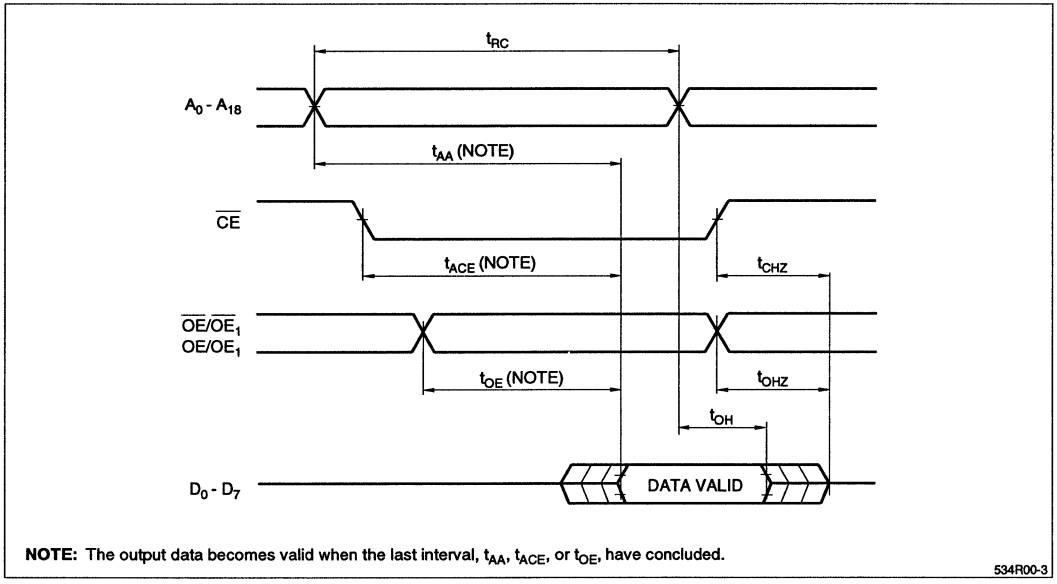
AC CHARACTERISTICS (V_{CC} = 5 V ±10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT	NOTE
Read cycle time	t_{RC}	120		ns	
Address access time	t_{AA}		120	ns	
Chip enable time	t_{ACE}		120	ns	
Output enable time	t_{OE}		60	ns	
Output hold time	t_{OH}	0		ns	
CE to output in High-Z	t_{CHZ}		60	ns	1
OE to output in High-Z	t_{OHZ}		60	ns	

NOTE:
1. This is the time required for the outputs to become high-impedance.

AC TEST CONDITIONS

PARAMETER	RATING
Input voltage amplitude	0.4 V to 2.6 V
Input rise/fall time	10 ns
Input reference level	1.5 V
Output reference level	1.5V
Output load condition	1TTL + 100 pF

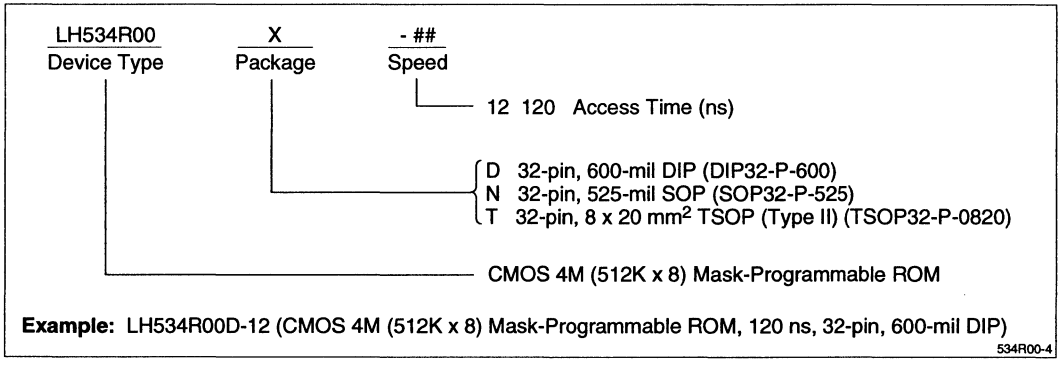


NOTE: The output data becomes valid when the last interval, t_{AA}, t_{ACE}, or t_{OE}, have concluded.

534R00-3

Figure 3. Timing Diagram

ORDERING INFORMATION



LH534000B

CMOS 4M (512K × 8/256K × 16) Mask-Programmable ROM

FEATURES

- Memory organization selection:
  524,288 × 8 bit (byte mode)
  262,144 × 16 bit (word mode)
- $\overline{\text{BYTE}}$ input pin selects bit configuration
- Access time: 200 ns (MAX.)
- Low-power consumption:
  Operating: 275 mW (MAX.)
  Standby: 550 μW (MAX.)
- Static operation (Internal sync. system)
- TTL compatible I/O
- Three-state outputs
- Single +5 V power supply
- Packages:
  40-pin, 600-mil DIP
  40-pin, 525-mil SOP
  48-pin, 12 × 18 mm^2 TSOP (Type I)
  44-pin, 14 × 14 mm^2 QFP
  44-pin, 10 × 10 mm^2 QFP
- ×16 word-wide pinout

DESCRIPTION

The LH534000B is a 4M bit mask-programmable ROM with two programmable memory organizations of byte and word modes. It is fabricated using silicon-gate CMOS process technology.

PIN CONNECTIONS

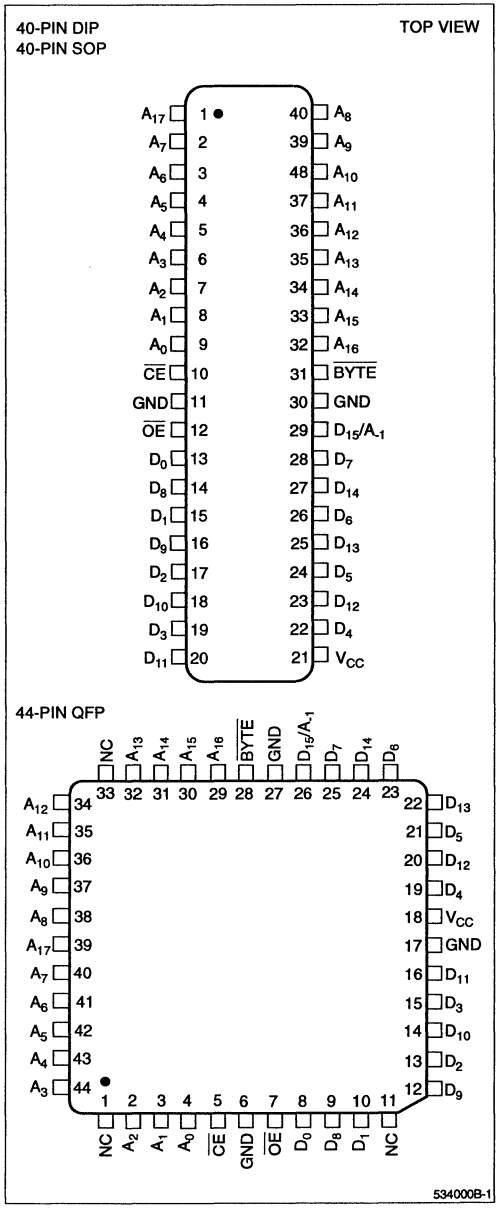


Figure 1. Pin Connections for DIP, SOP, and QFP Packages

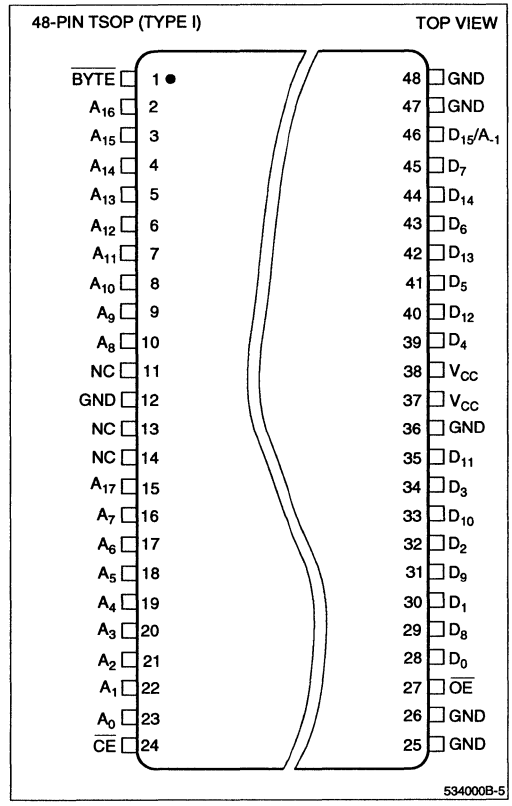


Figure 2. Pin Connections for TSOP Package

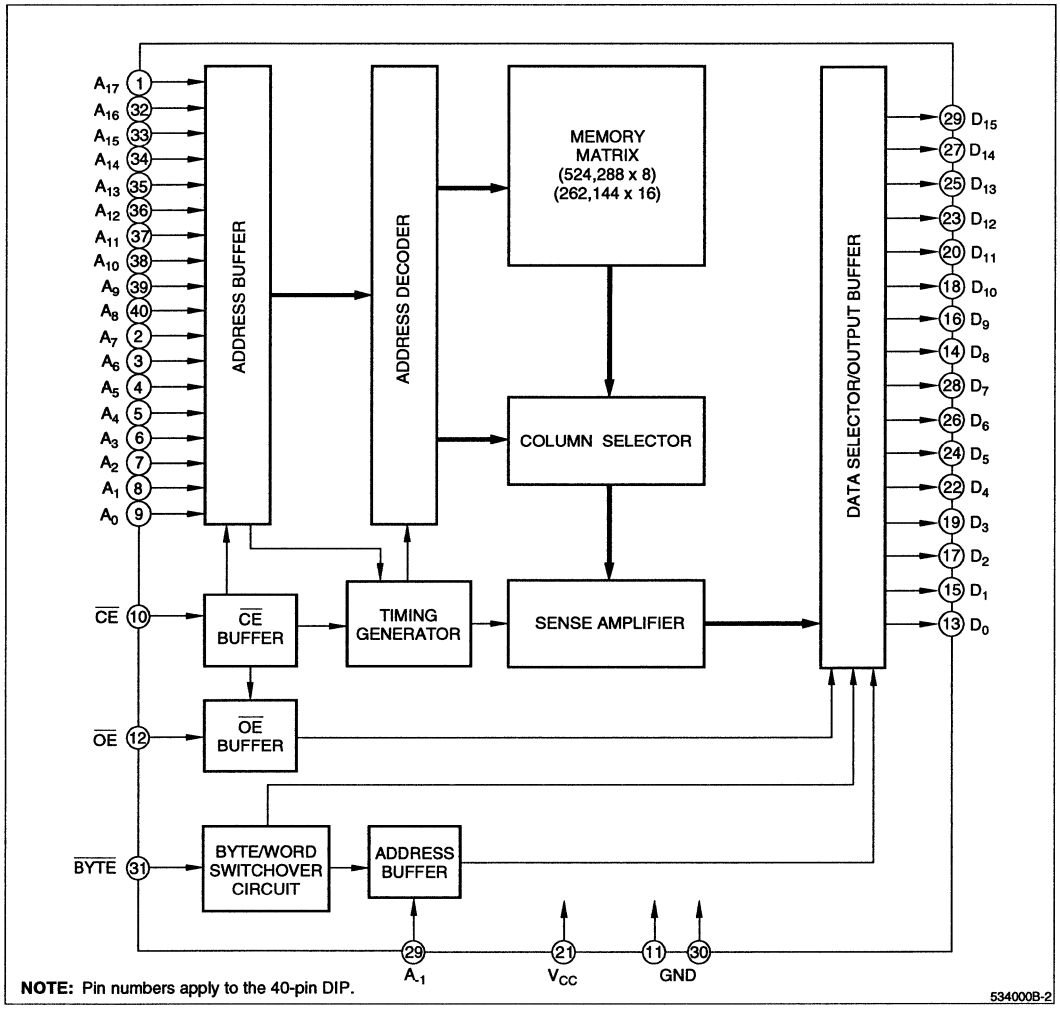


Figure 3. LH534000B Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME	NOTE
A_{-1}	Address input (BYTE mode)	1
A_0 - A_{17}	Address input	
D_0 - D_{15}	Data output	
$\overline{CE}$	Chip enable input	

SIGNAL	PIN NAME	NOTE
$\overline{OE}$	Chip enable input	
$\overline{BYTE}$	Byte/word mode switch	
V_{CC}	Power supply (+5 V)	
GND	Ground	

NOTE:

1. D_{15}/A_{-1} pin becomes LSB address input (A_{-1}) when the bit configuration is set in byte mode, and data output (D_{15}) when in word mode. $\overline{BYTE}$ input pin selects bit configuration.

TRUTH TABLE

$\overline{CE}$	$\overline{OE}$	$\overline{BYTE}$	A-1	MODE	D_0 - D_7	D_8 - D_{15}	SUPPLY CURRENT
H	X	X	X	Non selected	High-Z		Standby (I_{SB})
L	H	X	X	Non selected	High-Z		Operating (I_{CC})
L	L	H	Inhibit	Word	D_0 - D_7	D_8 - D_{15}	Operating (I_{CC})
L	L	L	L	Byte	D_0 - D_7	High-Z	Operating (I_{CC})
L	L	L	H	Byte	D_8 - D_{15}	High-Z	Operating (I_{CC})

NOTES:
1. X = H or L
2. The input state of $\overline{BYTE}$ must not be changed during operation. The $\overline{BYTE}$ pin must be set to either HIGH or LOW.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Supply voltage	V_{CC}	-0.3 to +7.0	V	1
Input voltage	V_{IN}	-0.3 to V_{CC} +0.3	V	
Output voltage	V_{OUT}	-0.3 to V_{CC} +0.3	V	
Operating temperature	Topr	0 to +70	°C	
Storage temperature	Tstg	-55 to +150	°C	

NOTE:
1. The maximum applicable voltage on any pin with respect to GND.

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	4.5	5.0	5.5	V

DC CHARACTERISTICS (V_{CC} = 5 V ±10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Input 'Low' voltage	V_{IL}		-0.3		0.8	V	
Input 'High' voltage	V_{IH}		2.2		V_{CC} +0.3	V	
Output 'Low' voltage	V_{OL}	I_{OL} = 2.0 mA			0.4	V	
Output 'High' voltage	V_{OH}	I_{OH} = -400 µA	2.4			V	
Input leakage current	$\|I_{LI}\|$	V_{IN} = 0 V to V_{CC}			10	µA	
Output leakage current	$\|I_{LO}\|$	V_{OUT} = 0 V to V_{CC}			10	µA	1
Operating current	I_{CC1}	t_{RC} = 200 ns			50	mA	2
	I_{CC2}	t_{RC} = 1 µs			45		
	I_{CC3}	t_{RC} = 200 ns			45	mA	3
	I_{CC4}	t_{RC} = 1 µs			40		
Standby current	I_{SB1}	$\overline{CE}$ = V_{IH}			3	mA	
	I_{SB2}	$\overline{CE}$ = V_{CC} - 0.2 V			100	µA	

NOTES:
1. OE = V_{IL}, $\overline{CE}$ = V_{IH}
2. V_{IN} = V_{IH}/V_{IL}, $\overline{CE}$ = V_{IL}, outputs open
3. V_{IN} = (V_{CC} - 0.2 V) or 0.2 V, $\overline{CE}$ = 0.2 V, outputs open

CAUTION

To stabilize the power supply, it is recommended that a high-frequency bypass capacitor be connected between the V_{CC} pin and the GND pin.

AC CHARACTERISTICS (V_{CC} = 5 V ±10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Read cycle time	t_{RC}	200			ns	
Address access time	t_{AA}			200	ns	
Chip enable access time	t_{ACE}			200	ns	
Output enable delay time	t_{OE}			80	ns	
Output hold time	t_{OH}	10			ns	
CE to output in High-Z	t_{CHZ}			80	ns	1
OE to output in High-Z	t_{OHZ}			80	ns	

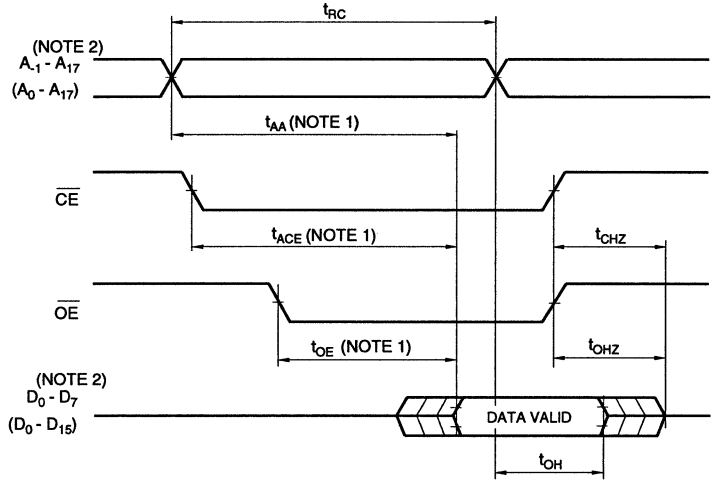
NOTE:
1. This is the time required for the outputs to become high-impedance.

AC TEST CONDITIONS

PARAMETER	RATING
Input voltage amplitude	0.6 V to 2.4 V
Input rise/fall time	10 ns
Input reference level	1.5 V
Output reference level	0.8 V and 2.2 V
Output load condition	1TTL +100 pF

CAPACITANCE (V_{CC} = 5 V ±10%, f = 1 MHz, T_A = 25°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Input capacitance	C_{IN}			10	pF
Output capacitance	C_{OUT}			10	pF

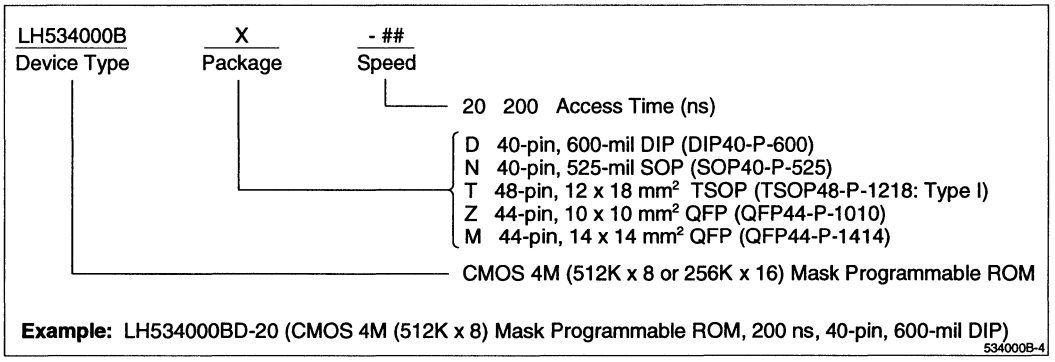


NOTES:
1. Data becomes valid after the intervals t_{AA}, t_{ACE} and t_{OE} from address input, chip enable, and output enable, respectively have been met.
2. Applies to byte mode. Signals in parentheses apply to word mode.

534000B-3

Figure 4. Timing Diagram

ORDERING INFORMATION



LH534000B-S

CMOS 4M (512K × 8/256K × 16)
3V-Drive Mask-Programmable ROM

FEATURES

- Low-power supply:
  2.6 to 5.5 V
- 524,288 × 8 bit organization
  (Byte mode)
  262,144 × 16 bit organization
  (Word mode)
- Access time:
  500 ns (2.6 V ≤ V_{CC} < 4.5 V)
  200 ns (4.5 V ≤ V_{CC} ≤ 5.5 V)
- Static operation
- Three-state outputs
- Packages:
  40-pin, 600-mil DIP
  40-pin, 525-mil SOP
  44-pin, 10 × 10 mm^2 QFP
  44-pin, 14 × 14 mm^2 QFP
  48-pin, 12 × 18 mm^2 TSOP (Type I)

DESCRIPTION

The LH534000B-S is a CMOS 4M-bit mask-programmable ROM organized as 524,288 × 8 bits (Byte mode) or 262,144 × 16 bits (Word mode) that can be selected by $\overline{BYTE}$ input pin.

It is suited for use in compact battery back-up systems due to be operated on 3 V power supply.

PIN CONNECTIONS

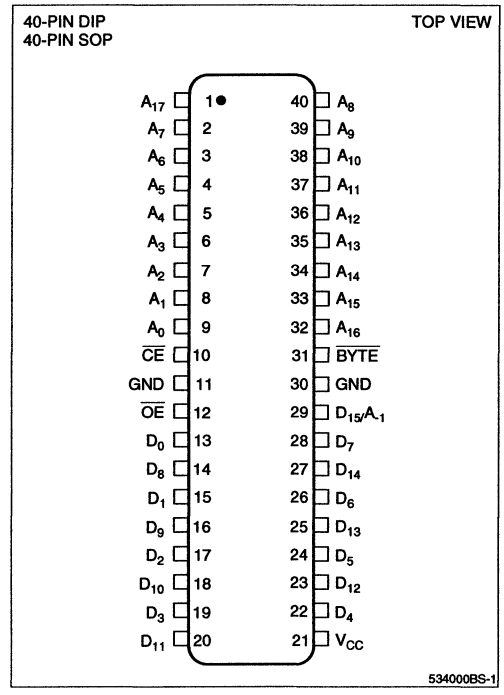


Figure 1. Pin Connections for DIP, SOP Packages

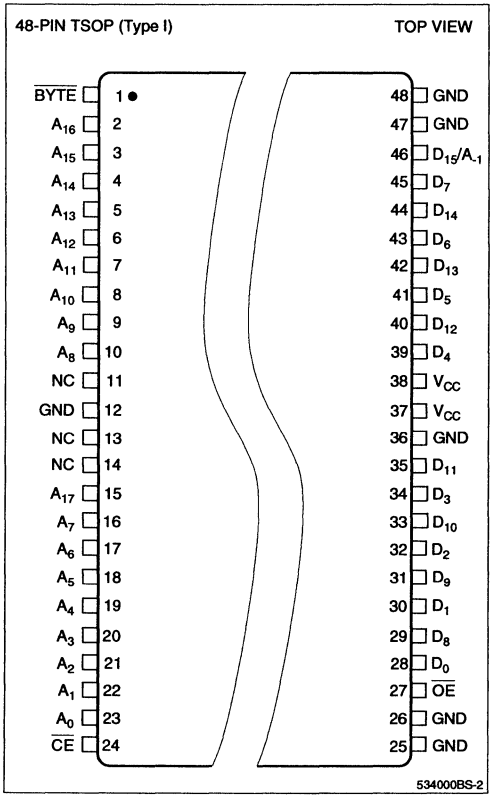


Figure 2. Pin Connections for TSOP Package

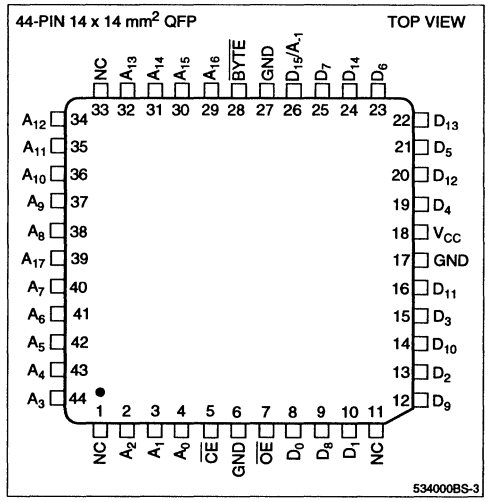


Figure 3. Pin Connections for 44-Pin, 14 × 14 mm^2 QFP Package

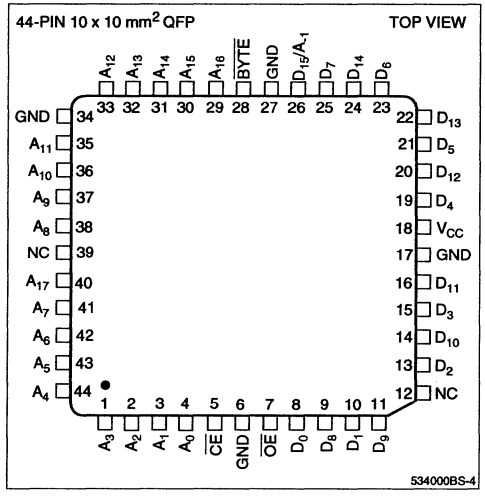


Figure 4. Pin Connections for 44-Pin, 10 × 10 mm^2 QFP Package

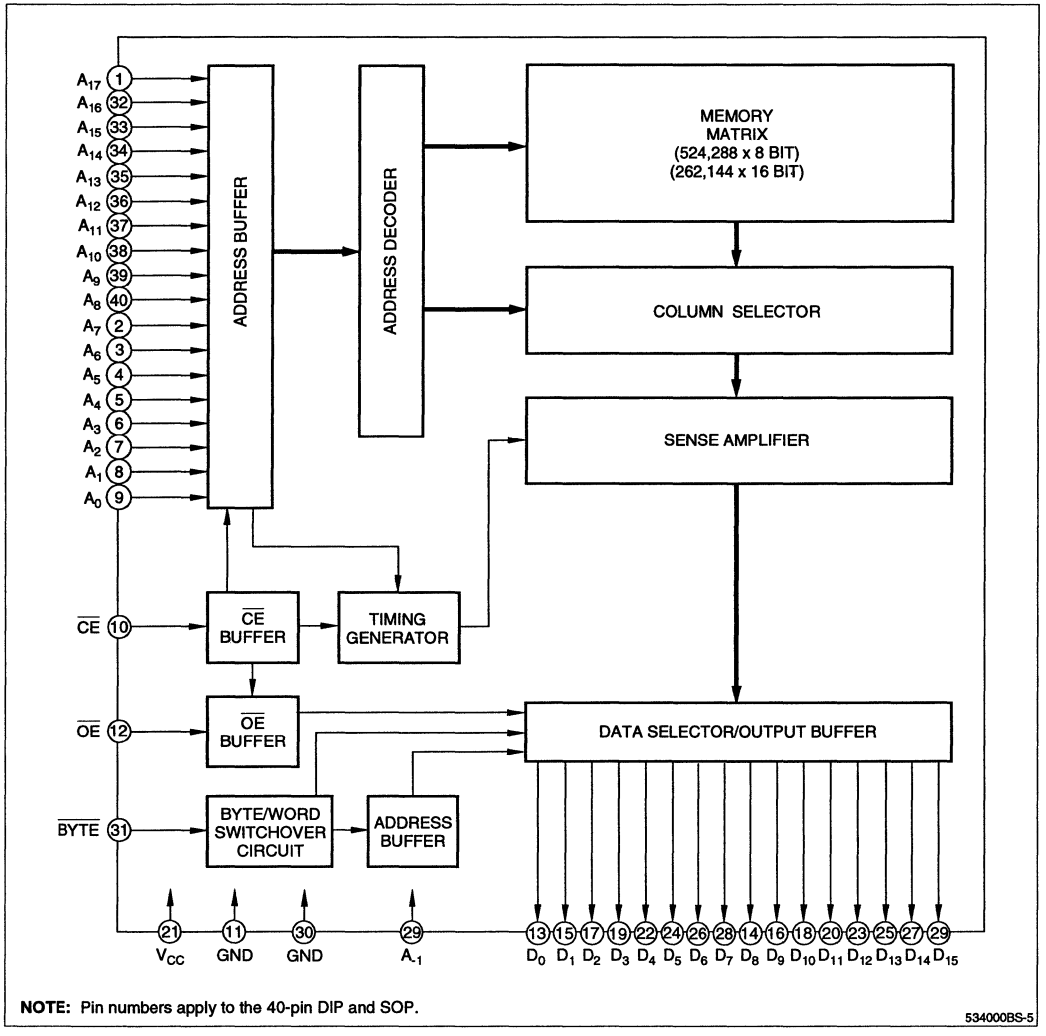


Figure 5. LH534000B-S Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME
A_{-1} - A_{17}	Address input
D_0 - D_{15}	Data output
$\overline{BYTE}$	Byte/word switch
$\overline{CE}$	Chip enable input

SIGNAL	PIN NAME
$\overline{OE}$	Output enable input
V_{CC}	Power supply
GND	Ground

NOTE:

1. The D_{15}/A_{-1} pin becomes LSB address input (A_{-1}) when the bit configuration is set to byte mode, and data output (D_{15}) when in word mode. The $\overline{BYTE}$ input pin selects bit configuration.

TRUTH TABLE

$\overline{CE}$	$\overline{OE}$	$\overline{BYTE}$	DATA OUTPUT		ADDRESS INPUT		SUPPLY CURRENT
			D_0 - D_7	D_8 - D_{15}	LSB	MSB	
H	X	X	High-Z	High-Z	–	–	Standby
L	H	X	High-Z	High-Z	–	–	Operating
L	L	H	D_0 - D_7	D_8 - D_{15}	A_0	A_{17}	Operating
L	L	L	D_0 - D_7	High-Z	A_{-1}	A_{17}	Operating

NOTE:
X = Don't care, High-Z = High-impedance

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Supply voltage	V_{CC}	-0.3 to +7.0	V
Input voltage	V_{IN}	-0.3 to V_{CC} + 0.3	V
Output voltage	V_{OUT}	-0.3 to V_{CC} + 0.3	V
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	-55 to +150	°C

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	2.6		5.5	V

DC CHARACTERISTICS (V_{CC} = 2.6 to 5.5 V, T_A = 0 to +70°C)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	MAX.	UNIT	NOTE
Input 'High' voltage	V_{IH}		0.8V_{CC}	V_{CC} + 0.3	V	
Input 'Low' voltage	V_{IL}		-0.3	0.4	V	
Output 'High' voltage	V_{OH}	I_{OH} = -100 µA	0.8V_{CC}		V	
Output 'Low' voltage	V_{OL}	I_{OL} = 400 µA		0.4	V	
Input leakage current	$\lvert I_{LI} \rvert$	V_{IN} = 0 V to V_{CC}		10	µA	
Output leakage current	$\lvert I_{LO} \rvert$	V_{OUT} = 0 V to V_{CC}		10	µA	1
Operating current	I_{CC1}	t_{RC} = 200 ns		50	mA	2
	I_{CC2}	t_{RC} = 1 µs		45	mA	2
	I_{CC3}	t_{RC} = 200 ns		45	mA	3
	I_{CC4}	t_{RC} = 1 µs		40	mA	3
Standby current	I_{SB1}	$\overline{CE}$ = V_{IH}		3	mA	
	I_{SB2}	$\overline{CE}$ = V_{CC} - 0.2 V		100	µA	
Input capacitance	C_{IN}	f = 1 MHz, T_A = +25°C		10	pF	
Output capacitance	C_{OUT}			10	pF	

NOTES:
1. $\overline{CE}$ = V_{IH}, $\overline{OE}$ = V_{IH}
2. V_{IN} = V_{IH}, V_{IL}, $\overline{CE}$ = V_{IL}, outputs open
3. V_{IN} = (V_{CC} - 0.2 V), 0.2 V, $\overline{CE}$ = 0.2 V, outputs open

AC CHARACTERISTICS (T_A = 0 to +70°C)

PARAMETER	SYMBOL	2.6 ≤ V_{CC} < 4.5		4.5 ≤ V_{CC} ≤ 5.5		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.		
Read cycle time	t_{RC}	500		200		ns	
Address access time	t_{AA}		500		200	ns	
Chip enable time	t_{ACE}		500		200	ns	
Output enable time	t_{OE}		150		80	ns	
Output hold time	t_{OH}	10		10		ns	
CE to output in High-Z	t_{CHZ}		150		80	ns	1
OE to output in High-Z	t_{OHZ}		150		80	ns	

NOTE:
1. This is the time required for the outputs to become high-impedance.

AC TEST CONDITIONS

PARAMETER	RATING
Input voltage amplitude	0.4 to 2.6 V
Input rise/fall time	10 ns
Input/output reference level	1.5 V
Output load condition	1 TTL + 100 pF

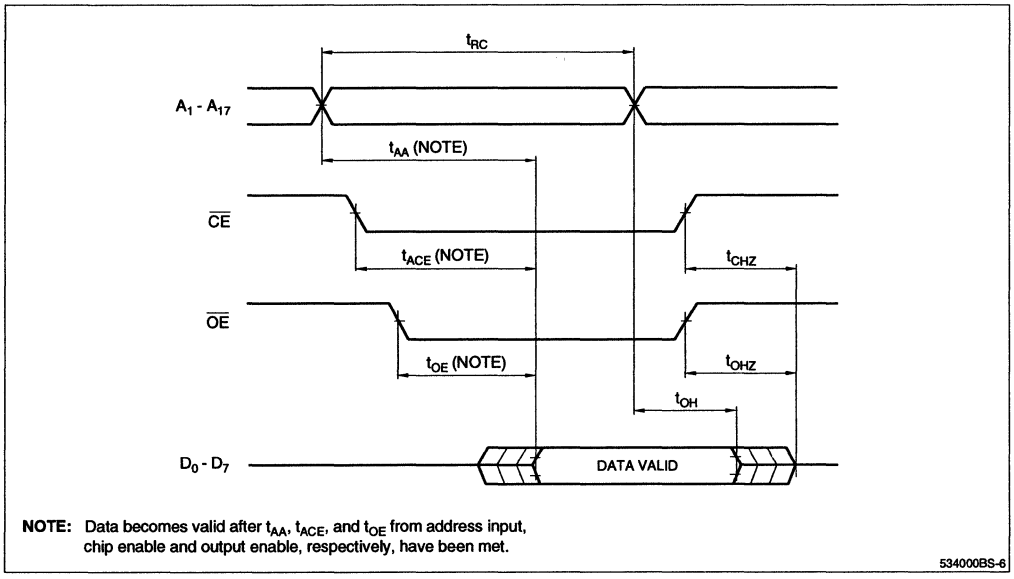


Figure 6. Byte Mode ($\overline{BYTE}$ = V_{IL})

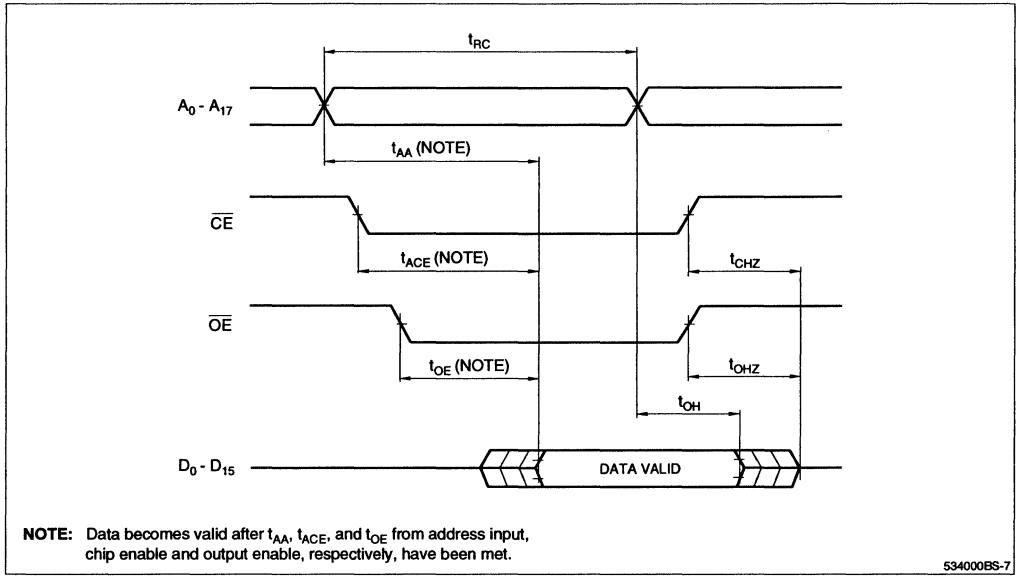
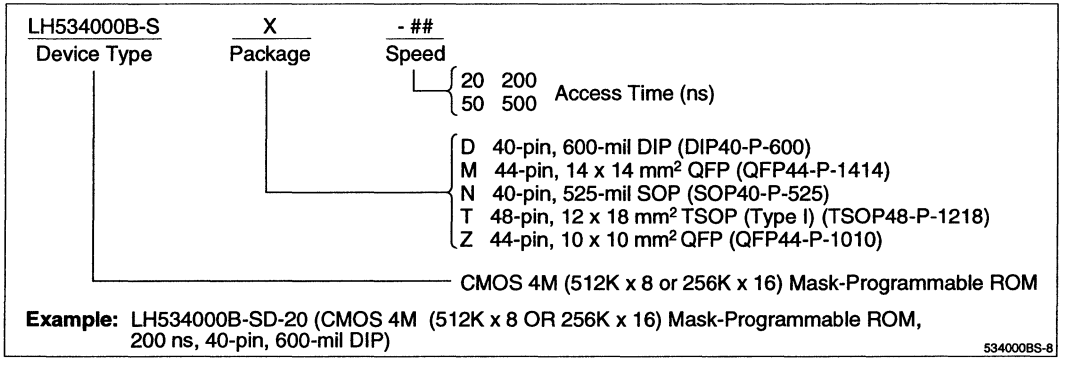


Figure 7. Word Mode ($\overline{BYTE}$ = V_{IH})

ORDERING INFORMATION



LH534100B CMOS 4M (512K × 8) Mask-Programmable ROM

FEATURES

- 524,288 × 8 bit organization
- Access time: 200 ns (MAX.)
- Power consumption:
  Operating: 275 mW (MAX.)
  Standby: 550 µW (MAX.)
- Mask-programmable OE/$\overline{OE}$ and $OE_1/\overline{OE}_1$/DC
- Fully-static operation
- TTL compatible I/O
- Three-state outputs
- Single +5 V power supply
- Packages:
  32-pin, 600-mil DIP
  32-pin, 525-mil SOP
- JEDEC standard EPROM pinout (DIP)

DESCRIPTION

The LH534100B is a 4M-bit mask-programmable ROM organized as 524,288 × 8 bits. It is fabricated using silicon-gate CMOS process technology.

PIN CONNECTIONS

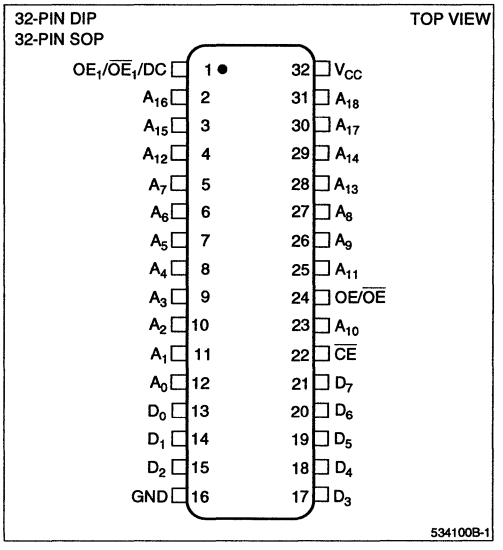


Figure 1. Pin Connections for DIP and SOP Packages

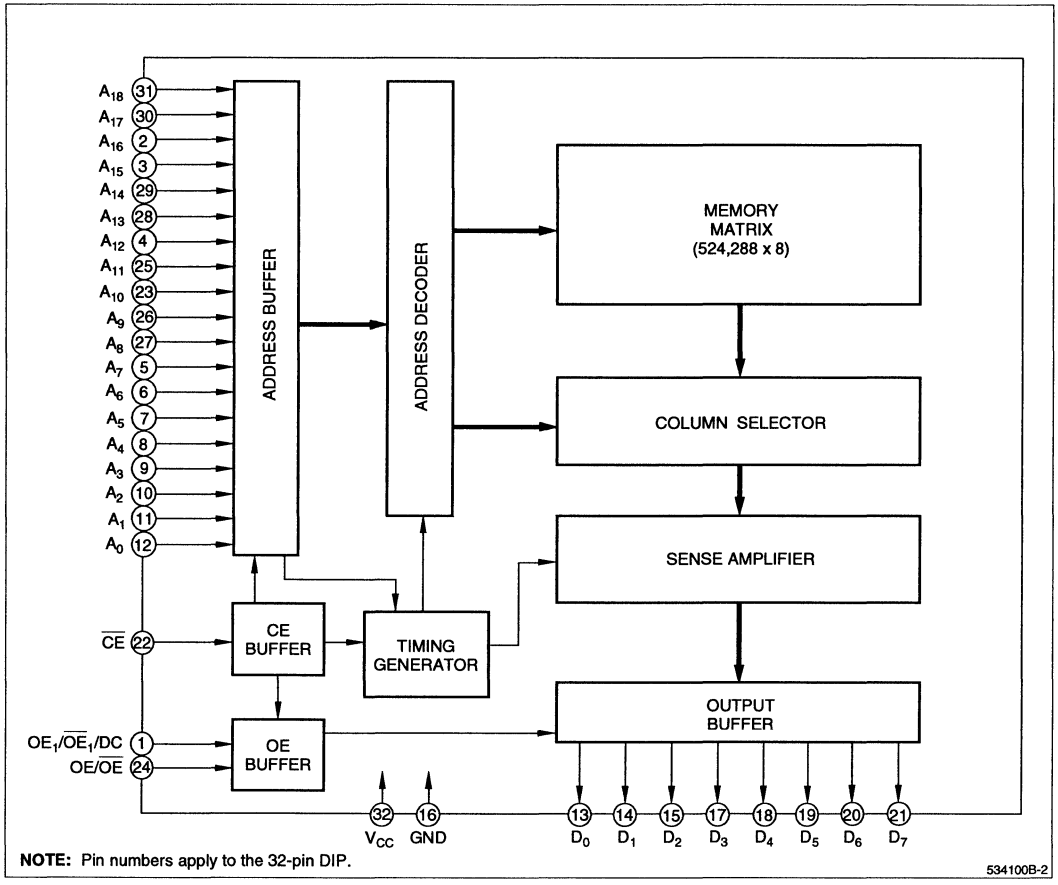


Figure 2. LH534100B Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME	NOTE
A_0 - A_{18}	Address input	
D_0 - D_7	Data output	
$\overline{CE}$	Chip Enable input	
OE/$\overline{OE}$	Output Enable input	1

SIGNAL	PIN NAME	NOTE
$OE_1/\overline{OE_1}$/DC	Output Enable input/ Don't Care	1
V_{CC}	Power supply (+5 V)	
GND	Ground	

NOTE:

1. Active levels of $OE_1/\overline{OE_1}$/DC and OE/$\overline{OE}$ are mask-programmable.
   Selecting DC allows the outputs to be active for both high and low levels applied to this pin.
   It is recommended to apply either a HIGH or a LOW to the DC pin.

TRUTH TABLE

$\overline{CE}$	OE/$\overline{OE}$	$OE_1/\overline{OE_1}$	MODE	D_0 - D_7	SUPPLY CURRENT
H	X	X	Non selected	High-Z	Standby (I_{SB})
L	X	L/H	Non selected	High-Z	Operating (I_{CC})
L	L/H	X	Non selected	High-Z	Operating (I_{CC})
L	H/L	H/L	Selected	D_{OUT}	Operating (I_{CC})

NOTE:
X = H or L

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Supply voltage	V_{CC}	-0.3 to +7.0	V	1
Input voltage	V_{IN}	-0.3 to V_{CC} +0.3	V	
Output voltage	V_{OUT}	-0.3 to V_{CC} +0.3	V	
Operating temperature	Topr	0 to +70	°C	
Storage temperature	Tstg	-55 to +150	°C	

NOTE:
1. The maximum applicable voltage on any pin with respect to GND.

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	4.5	5.0	5.5	V

DC CHARACTERISTICS (V_{CC} = 5 V ±10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Input 'Low' voltage	V_{IL}		-0.3		0.8	V	
Input 'High' voltage	V_{IH}		2.2		V_{CC} +0.3	V	
Output 'Low' voltage	V_{OL}	I_{OL} = 2.0 mA			0.4	V	
Output 'High' voltage	V_{OH}	I_{OH} = -400 µA	2.4			V	
Input leakage current	$\lvert I_{LI} \rvert$	V_{IN} = 0 V to V_{CC}			10	µA	
Output leakage current	$\lvert I_{LO} \rvert$	V_{OUT} = 0 V to V_{CC}			10	µA	1
Operating current	I_{CC1}	t_{RC} = 200 ns			50	mA	2
	I_{CC2}	t_{RC} = 1 µs			45		
	I_{CC3}	t_{RC} = 200 ns			45	mA	3
	I_{CC4}	t_{RC} = 1 µs			40		
Standby current	I_{SB1}	$\overline{CE}$ = V_{IH}			3	mA	
	I_{SB2}	$\overline{CE}$ = V_{CC} - 0.2 V			100	µA	

NOTES:
1. $\overline{CE}/\overline{OE}/\overline{OE_1}$ = V_{IH} or OE/OE_1 = V_{IL}
2. V_{IN} = V_{IH}/V_{IL}, $\overline{CE}$ = V_{IL}, outputs open
3. V_{IN} = (V_{CC} - 0.2 V) or 0.2 V, $\overline{CE}$ = 0.2 V, outputs open

CAUTION

To stabilize the power supply, it is recommended that a high-frequency bypass capacitor be connected between the V_{CC} pin and the GND pin.

AC CHARACTERISTICS (V_{CC} = 5 V ±10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT	NOTE
Read cycle time	t_{RC}	200		ns	
Address access time	t_{AA}		200	ns	
Chip enable time	t_{ACE}		200	ns	
Output enable time	t_{OE}		80	ns	
Output hold time	t_{OH}	10		ns	
CE to output in High-Z	t_{CHZ}		80	ns	1
OE to output in High-Z	t_{OHZ}		80	ns	

NOTE:
1. This is the time required for the outputs to become high-impedance.

AC TEST CONDITIONS

PARAMETER	RATING
Input voltage amplitude	0.6 V to 2.4 V
Input rise/fall time	10 ns
Input reference level	1.5 V
Output reference level	0.8 V and 2.2 V
Output load condition	1TTL +100 pF

CAPACITANCE (V_{CC} = 5 V ±10%, f = 1 MHz, T_A = 25°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Input capacitance	C_{IN}			10	pF
Output capacitance	C_{OUT}			10	pF

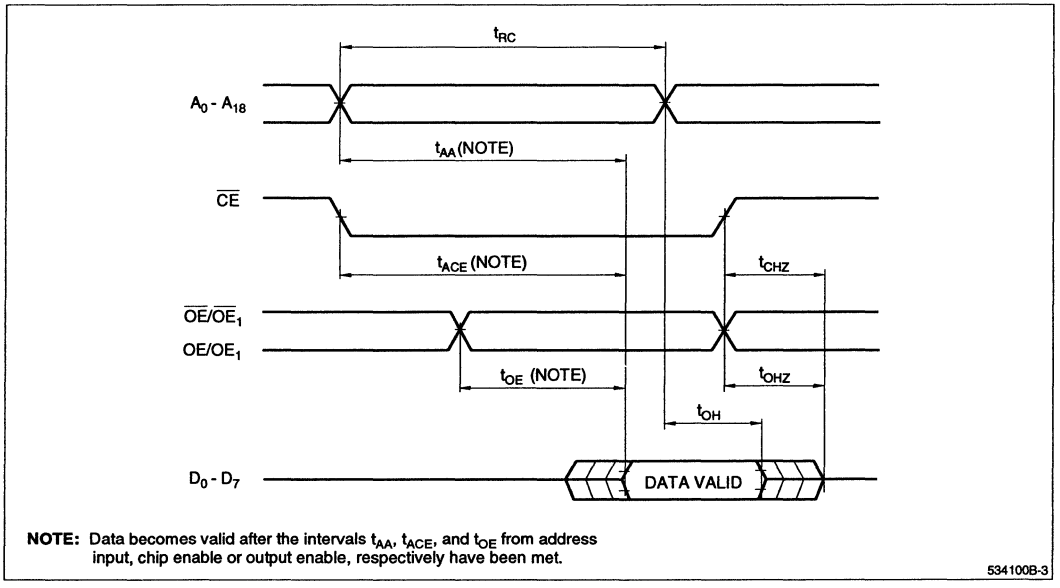
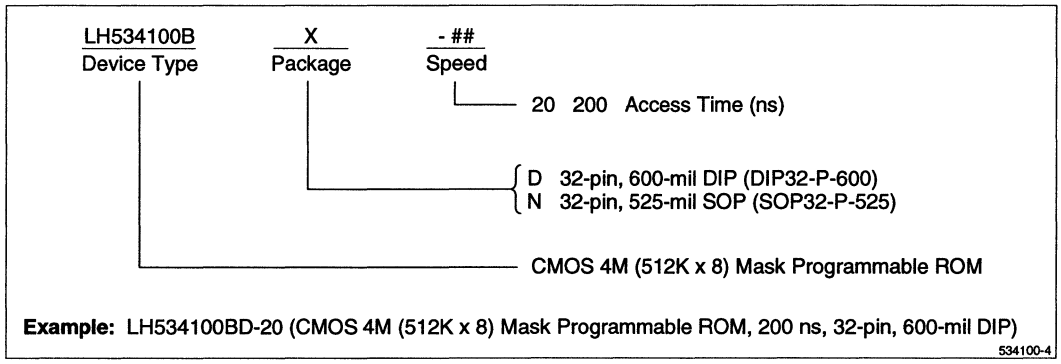


Figure 3. Timing Diagram

ORDERING INFORMATION



Example: LH534100BD-20 (CMOS 4M (512K x 8) Mask Programmable ROM, 200 ns, 32-pin, 600-mil DIP)

534100-4

LH534500A

CMOS 4M (512K × 8/256K × 16)
Mask-Programmable ROM

FEATURES

- Memory organization selection:
  524,288 × 8 bit (byte mode)
  262,144 × 16 bit (word mode)
- $\overline{\text{BYTE}}$ input pin selects bit configuration
- Access time: 150 ns (MAX.)
- Low-power consumption:
  Operating: 275 mW (MAX.)
  Standby: 550 µW (MAX.)
- Static operation (Internal sync. system)
- TTL compatible I/O
- Three-state outputs
- Single +5 V power supply
- Packages:
  40-pin, 600-mil DIP
  40-pin, 525-mil SOP
  48-pin, 12 × 18 mm^2 TSOP (Type I)
  44-pin, 14 × 14 mm^2 QFP
- ×16 word-wide pinout

DESCRIPTION

The LH534500A is a 4M bit mask-programmable ROM with two programmable memory organizations of byte and word modes. It is fabricated using silicon-gate CMOS process technology.

PIN CONNECTIONS

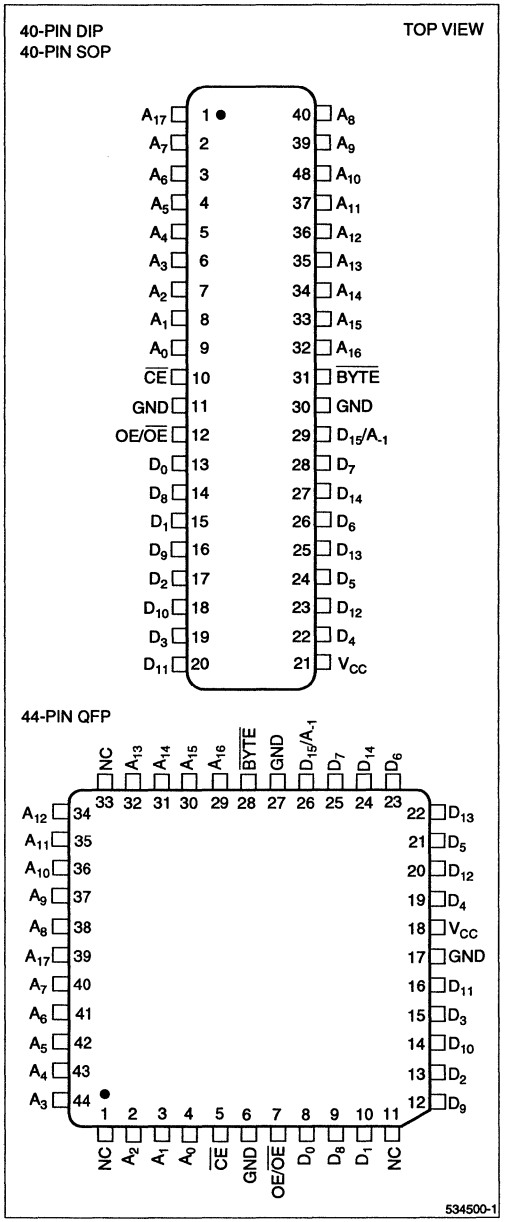


Figure 1. Pin Connections for DIP, SOP, and QFP Packages

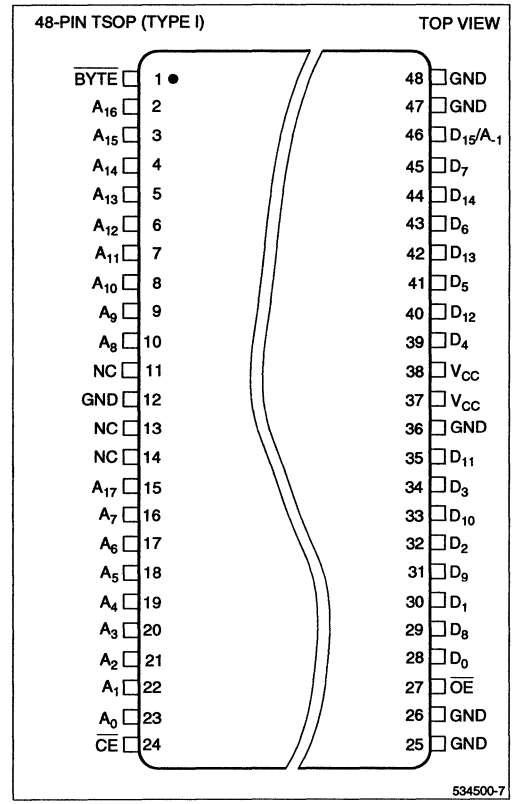


Figure 2. Pin Connections for TSOP Package

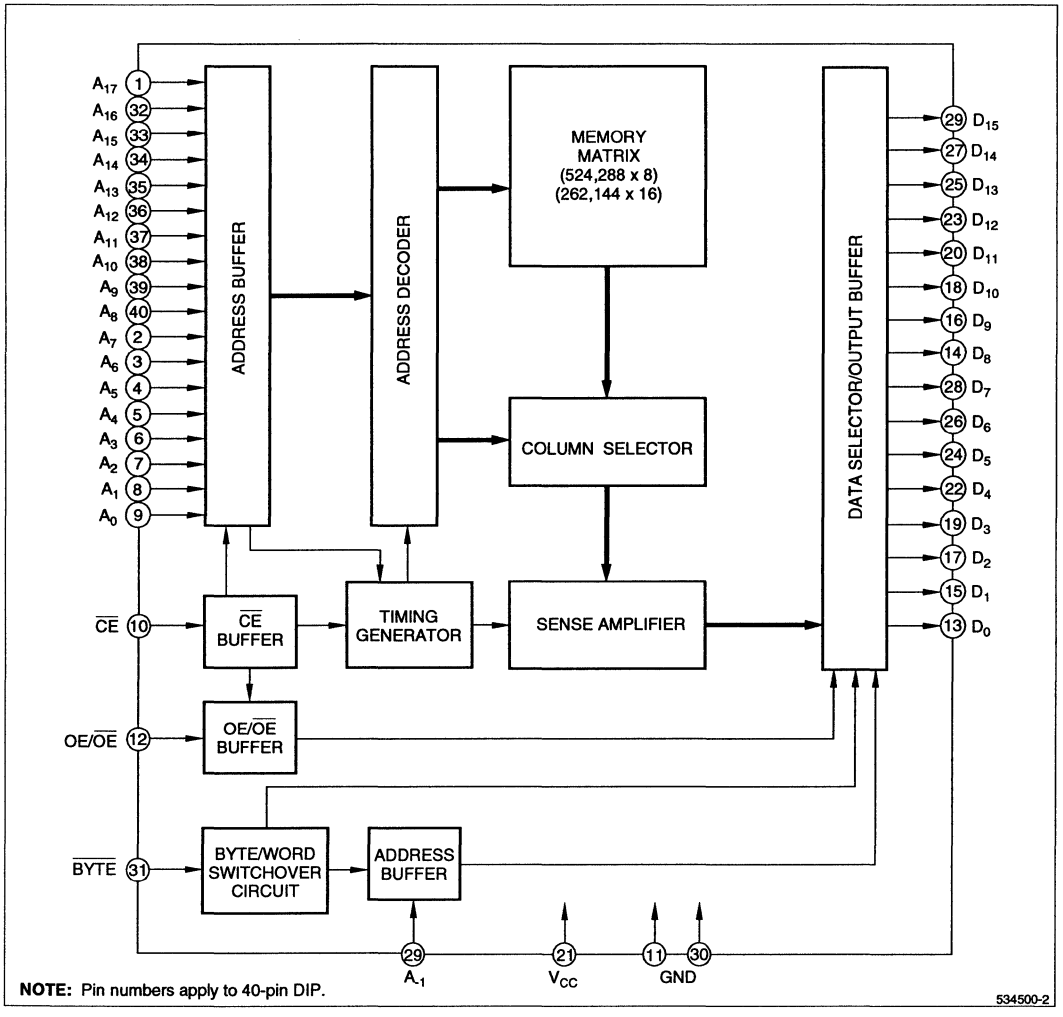


Figure 3. LH534500A Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME	NOTE
A_{-1}	Address input	1
A_0 - A_{17}	Address input	
D_0 - D_{15}	Data output	
$\overline{CE}$	Chip Enable input	

SIGNAL	PIN NAME	NOTE
OE/$\overline{OE}$	Chip Enable input	2
$\overline{BYTE}$	Byte/word mode switch	
V_{CC}	Power supply (+5 V)	
GND	Ground	

NOTES:

1. D_{15}/A_{-1} pin becomes LSB address input (A_{-1}) when the bit configuration is set in byte mode, and data output (D_{15}) when in word mode. $\overline{BYTE}$ input pin selects bit configuration.
2. Active level of OE/$\overline{OE}$ is mask-programmable.

TRUTH TABLE

$\overline{CE}$	OE/$\overline{OE}$	$\overline{BYTE}$	A_{-1}	MODE	D_0 - D_7	D_8 - D_{15}	SUPPLY CURRENT
H	X	X	X	Non selected	High-Z		Standby (I_{SB})
L	L/H	X	X	Non selected	High-Z		Operating (I_{CC})
L	H/L	H	Inhibit	Word	D_0 - D_7	D_8 - D_{15}	Operating (I_{CC})
L	H/L	L	L	Byte	D_0 - D_7	High-Z	Operating (I_{CC})
L	H/L	L	H	Byte	D_8 - D_{15}	High-Z	Operating (I_{CC})

NOTE:

X = High or Low

The input state of $\overline{BYTE}$ must not be changed during operation. The $\overline{BYTE}$ pin must be set to either High or Low.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Supply voltage	V_{CC}	-0.3 to +7.0	V	1
Input voltage	V_{IN}	-0.3 to V_{CC} +0.3	V	
Output voltage	V_{OUT}	-0.3 to V_{CC} +0.3	V	
Operating temperature	Topr	0 to +70	°C	
Storage temperature	Tstg	-55 to +150	°C	

NOTE:

1. The maximum applicable voltage on any pin with respect to GND

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	4.5	5.0	5.5	V

DC CHARACTERISTICS (V_{CC} = 5 V ±10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Input 'Low' voltage	V_{IL}		-0.3		0.8	V	
Input 'High' voltage	V_{IH}		2.2		V_{CC} +0.3	V	
Output 'Low' voltage	V_{OL}	I_{OL} = 2.0 mA			0.4	V	
Output 'High' voltage	V_{OH}	I_{OH} = -400 µA	2.4			V	
Input leakage current	$\lvert I_{LI} \rvert$	V_{IN} = 0 V to V_{CC}			10	µA	
Output leakage current	$\lvert I_{LO} \rvert$	V_{OUT} = 0 V to V_{CC}			10	µA	1
Operating current	I_{CC1}	t_{RC} = 150 ns			50	mA	2
	I_{CC2}	t_{RC} = 1 µs			45		
	I_{CC3}	t_{RC} = 150 ns			45	mA	3
	I_{CC4}	t_{RC} = 1 µs			40		
Standby current	I_{SB1}	$\overline{CE}$ = V_{IH}			5	mA	
	I_{SB2}	$\overline{CE}$ = V_{CC} - 0.2 V			100	µA	

NOTES:

1. OE = V_{IL}, $\overline{CE}$/$\overline{OE}$ = V_{IH}
2. V_{IN} = V_{IH}/V_{IL}, $\overline{CE}$ = V_{IL}, outputs open
3. V_{IN} = (V_{CC} - 0.2 V) or 0.2 V, $\overline{CE}$ = 0.2 V, outputs open

AC CHARACTERISTICS (V_{CC} = 5 V ±10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Read cycle time	t_{RC}	150			ns	
Address access time	t_{AA}			150	ns	
Chip enable access time	t_{ACE}			150	ns	
Output enable delay time	t_{OE}			70	ns	
Output hold time	t_{OH}	5			ns	
CE to output in High-Z	t_{CHZ}			70	ns	1
OE to output in High-Z	t_{OHZ}			70	ns	

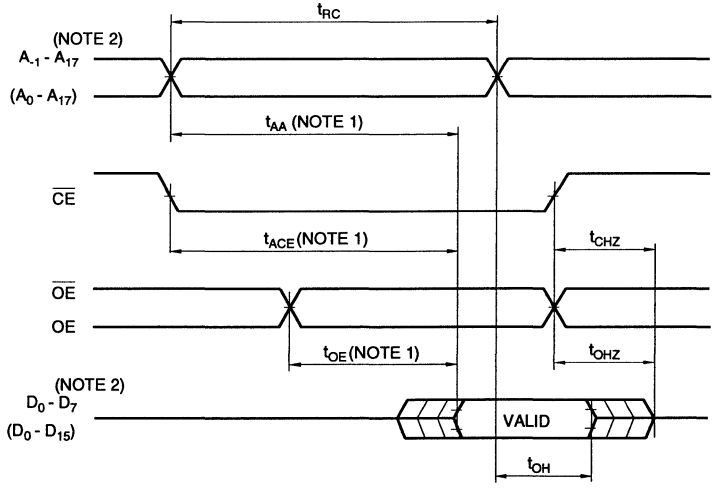
NOTE:
1. This is the time required for the outputs to become high-impedance.

AC TEST CONDITIONS

PARAMETER	RATING
Input voltage amplitude	0.6 V to 2.4 V
Input rise/fall time	10 ns
Input reference level	1.5 V
Output reference level	0.8 V and 2.2 V
Output load condition	1TTL +100 pF

CAPACITANCE (V_{CC} = 5 V ±10%, f = 1 MHz, T_A = 25°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Input capacitance	C_{IN}			10	pF
Output capacitance	C_{OUT}			10	pF

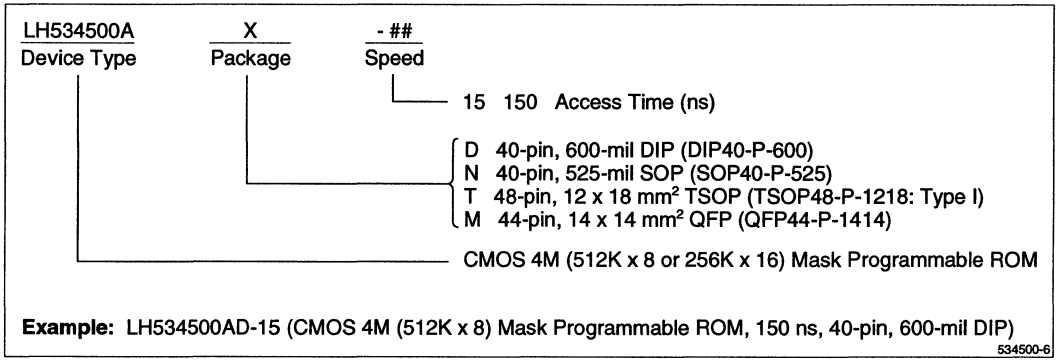


NOTES:
1. Data becomes valid after the intervals t_{AA}, t_{ACE} and t_{OE} from address input, chip enable, and output enable, respectively have been met.
2. Applies to byte mode. Signals in parentheses apply to word mode.

534500-3

Figure 4. Timing Diagram

ORDERING INFORMATION



LH534600A

CMOS 4M (512K × 8/256K × 16) Mask-Programmable ROM

FEATURES

- 524,288 × 8 bit organization
  (Byte mode)
  262,144 × 16 bit organization
  (Word mode)
- $\overline{\text{BYTE}}$ input pin selects bit configuration
- Access time: 100 ns (MAX.)
- Low-power consumption:
  Operating: 550 mW (MAX.)
  Standby: 1.65 mW (MAX.)
- Static operation (Internal sync. system)
- Automatic power-down mode
- TTL compatible I/O
- Three-state outputs
- Single +5 V power supply
- Packages:
  40-pin, 600-mil DIP
  40-pin, 525-mil SOP
  44-pin, 14 × 14 mm^2 QFP
  48-pin, 12 × 18 mm^2 TSOP (Type I)
- ×16 word-wide pinout

DESCRIPTION

The LH534600A is a 4M bit mask-programmable ROM with two programmable memory organizations of byte and word modes. It is fabricated using silicon-gate CMOS process technology.

PIN CONNECTIONS

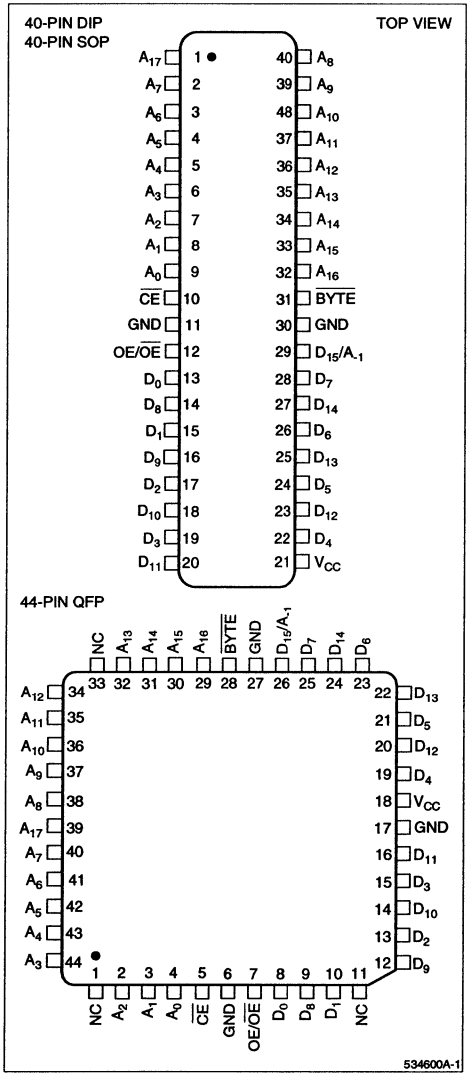


Figure 1. Pin Connections for DIP, SOP, and QFP Packages

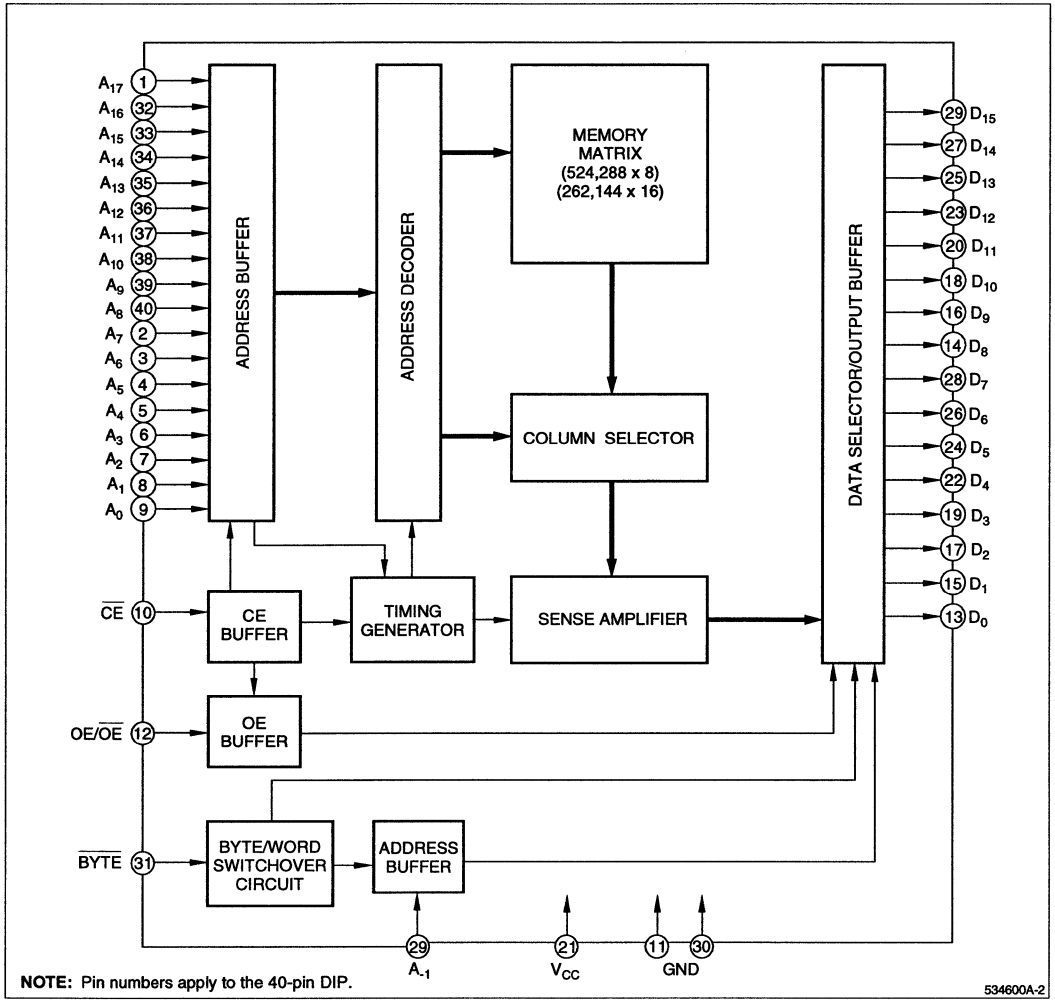


Figure 2. LH534600A Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME	NOTE
A_{-1}	Address input ($\overline{BYTE}$ MODE)	1
A_0 - A_{17}	Address input	
D_0 - D_{15}	Data output	
$\overline{CE}$	Chip Enable input	

SIGNAL	PIN NAME	NOTE
OE/$\overline{OE}$	Output Enable input	2
$\overline{BYTE}$	Byte/word switch	
V_{CC}	Power supply (+5 V)	
GND	Ground	

NOTES:

1. D_{15}/A_{-1} pin becomes LSB address input (A_{-1}) when the bit configuration is set in byte mode, and data output (D_{15}) when in word mode. $\overline{BYTE}$ input pin selects bit configuration.
2. Active level of OE/$\overline{OE}$ is mask-programmable.

TRUTH TABLE

$\overline{CE}$	$\overline{OE}$	$\overline{BYTE}$	A_{-1}	MODE	D_0 - D_7	D_8 - D_{15}	SUPPLY CURRENT	NOTE
H	X	X	X	Non selected	High-Z		Standby (I_{SB})	1
L	H	X	X	Non selected	High-Z		Operating (I_{CC})	
L	L	H	Input inhibit	Word	D_0 - D_7	D_8 - D_{15}	Operating (I_{CC})	
L	L	L	L	Byte	D_0 - D_7	High-Z	Operating (I_{CC})	
L	L	L	H	Byte	D_8 - D_{15}	High-Z	Operating (I_{CC})	

NOTE:
1. The input state of $\overline{BYTE}$ pin must not be changed during operation. The $\overline{BYTE}$ pin must be set to either High or Low. X = H or L

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Supply voltage	V_{CC}	-0.3 to +7.0	V	1
Input voltage	V_{IN}	-0.3 to V_{CC} +0.3	V	
Output voltage	V_{OUT}	-0.3 to V_{CC} +0.3	V	
Operating temperature	Topr	0 to +70	°C	
Storage temperature	Tstg	-55 to +150	°C	

NOTE:
1. The maximum applicable voltage on any pin with respect to GND.

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	4.5	5.0	5.5	V

DC CHARACTERISTICS (V_{CC} = 5 V ±10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Input 'Low' voltage	V_{IL}		-0.3		0.8	V	
Input 'High' voltage	V_{IH}		2.2		V_{CC} +0.3	V	
Output 'Low' voltage	V_{OL}	I_{OL} = 2.0 mA			0.4	V	
Output 'High' voltage	V_{OH}	I_{OH} = -400 µA	2.4			V	
Input leakage current	$\lvert I_{LI} \rvert$	V_{IN} = 0 V to V_{CC}			10	µA	
Output leakage current	$\lvert I_{LO} \rvert$	V_{OUT} = 0 V to V_{CC}			10	µA	1
Operating current	I_{CC1}	t_{RC} = 100 ns			100	mA	2
	I_{CC2}	t_{RC} = 1 µs			70		
	I_{CC3}	t_{RC} = 100 ns			100	mA	3
	I_{CC4}	t_{RC} = 1 µs			70		
Standby current	I_{SB1}	$\overline{CE}$ = V_{IH}			3	mA	
	I_{SB2}	$\overline{CE}$ = V_{CC} - 0.2 V			300	µA	

NOTES:
1. OE = V_{IL}, $\overline{CE}$/$\overline{OE}$ = V_{IH}
2. V_{IN} = V_{IH}/V_{IL}, $\overline{CE}$ = V_{IL}, outputs open
3. V_{IN} = (V_{CC} - 0.2 V) or 0.2 V, $\overline{CE}$ = 0.2 V, outputs open

AC CHARACTERISTICS (V_{CC} = 5 V ±10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	LH534600			UNIT	NOTE
		MIN.	TYP.	MAX.		
Read cycle time	t_{RC}	100			ns	
Address access time	t_{AA}			100	ns	
Chip enable access time	t_{ACE}			100	ns	
Output enable delay time	t_{OE}			40	ns	
Output hold time	t_{OH}	5			ns	
CE to output in High-Z	t_{CHZ}			40	ns	1
OE to ouput in High-Z	t_{OHZ}			40	ns	

NOTE:
1. This is the time required for the outputs to become high-impedance.

AC TEST CONDITIONS

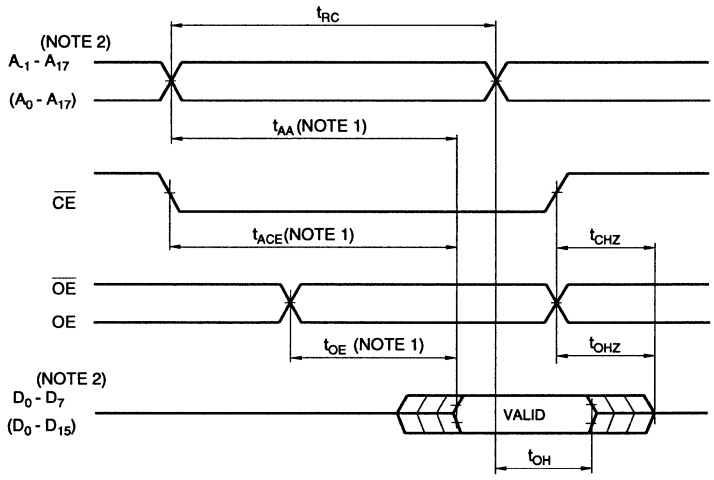
PARAMETER	RATING
Input voltage amplitude	0.6 V to 2.4 V
Input rise/fall time	10 ns
Input reference level	1.5 V
Output reference level	1.5 V
Output load condition	1TTL +100 pF

CAPACITANCE (V_{CC} = 5 V ±10%, f = 1 MHz, T_A = 25°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Input capacitance	C_{IN}			10	pF
Output capacitance	C_{OUT}			10	pF

CAUTION

To stabilize the power supply, it is recommended that a high-frequency bypass capacitor be connected between the V_{CC} pin and the GND pin.

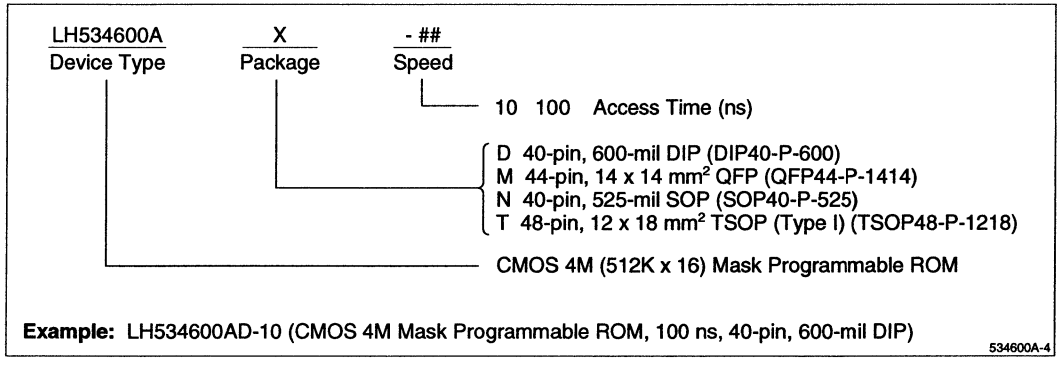


NOTES:
1. Data becomes valid after the intervals t_{AA}, t_{ACE} and t_{OE} from address input and output enable input, respectively have been met.
2. Apply to byte mode. Signals in parentheses apply to word mode.

534600A-3

Figure 3. Timing Diagram

ORDERING INFORMATION



Example: LH534600AD-10 (CMOS 4M Mask Programmable ROM, 100 ns, 40-pin, 600-mil DIP)

534600A-4

LH538P00A

CMOS 8M (1M × 8/512K × 16)
Mask-Programmable ROM

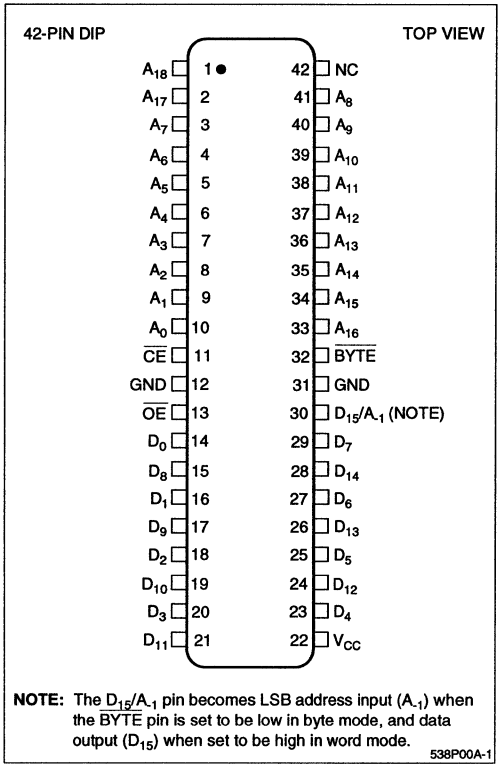
FEATURES

- 1,048,576 × 8 bit organization
  (Byte mode)
  524,288 × 16 bit organization
  (Word mode)
- Access time: 120 ns (MAX.)
- Power consumption:
  Operating: 330 mW (MAX.)
  Standby: 550 µW (MAX.)
- Static operation
- TTL compatible I/O
- Three-state outputs
- Single +5 V power supply
- Packages:
  42-pin, 600-mil DIP
  44-pin, 600-mil SOP
  48-pin, 12 × 18 mm^2 TSOP (Type I)

DESCRIPTION

The LH538P00A is an 8M-bit mask-programmable ROM organized as 1,048,576 × 8 bits (Byte mode) or 524,288 × 16 bits (Word mode) that can be selected by $\overline{BYTE}$ input pin. It is fabricated using silicon-gate CMOS process technology.

PIN CONNECTIONS



NOTE: The D_{15}/A_{-1} pin becomes LSB address input (A_{-1}) when the $\overline{BYTE}$ pin is set to be low in byte mode, and data output (D_{15}) when set to be high in word mode.

538P00A-1

Figure 1. Pin Connections for DIP Package

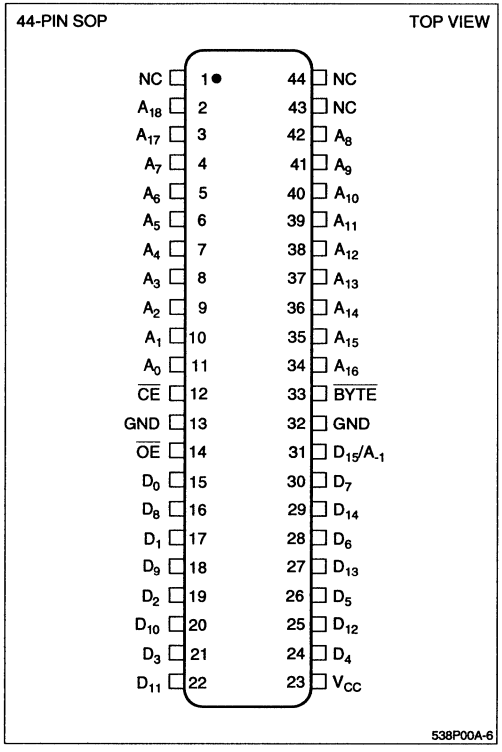


Figure 2. Pin Connections for SOP Package

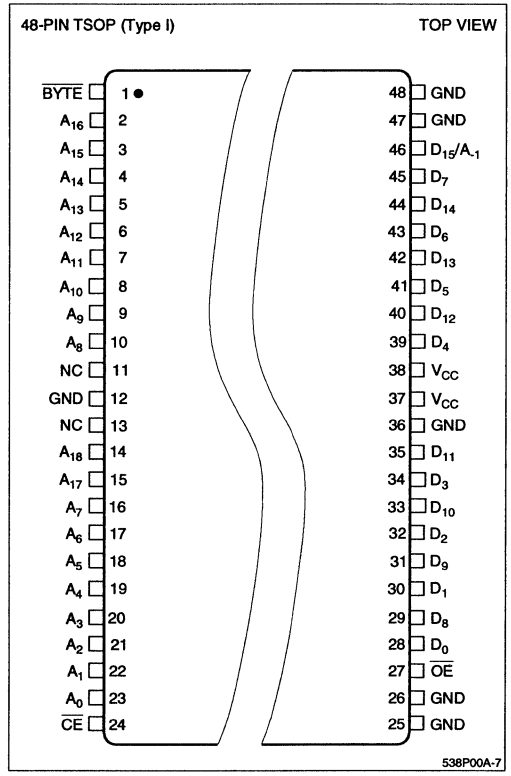


Figure 3. Pin Connections for TSOP Package

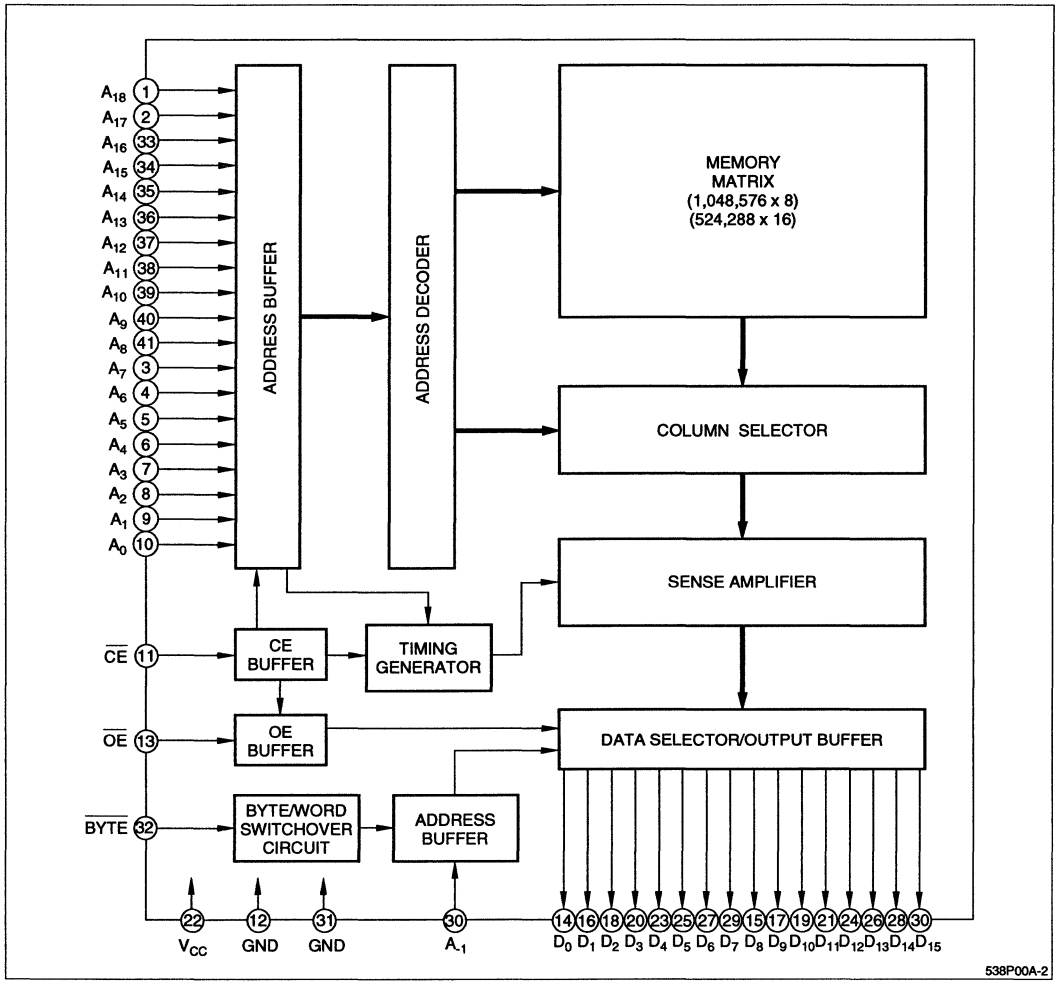


Figure 4. LH538P00A Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME
A_1 - A_{18}	Address input
D_0 - D_{15}	Data output
$\overline{CE}$	Chip enable input
$\overline{OE}$	Output enable input

SIGNAL	PIN NAME
$\overline{BYTE}$	Byte/word switch
V_{CC}	Power supply (+5 V)
GND	Ground

TRUTH TABLE

$\overline{CE}$	$\overline{OE}$	$\overline{BYTE}$	A_{-1} (D_{15})	DATA OUTPUT		ADDRESS INPUT		SUPPLY CURRENT
				D_0 - D_7	D_8 - D_{15}	LSB	MSB	
H	X	X	X	High-Z	High-Z	–	–	Standby (I_{SB})
L	H	X	X	High-Z	High-Z	–	–	Operating (I_{CC})
L	L	H	–	D_0 - D_7	D_8 - D_{15}	A_0	A_{18}	Operating (I_{CC})
L	L	L	L	D_0 - D_7	High-Z	A_{-1}	A_{18}	Operating (I_{CC})
L	L	L	H	D_8 - D_{15}	High-Z	A_{-1}	A_{18}	Operating (I_{CC})

NOTE:
X = H or L

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Supply voltage	V_{CC}	-0.3 to +7.0	V
Input voltage	V_{IN}	-0.3 to V_{CC} +0.3	V
Output voltage	V_{OUT}	-0.3 to V_{CC} +0.3	V
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	4.5	5.0	5.5	V

DC CHARACTERISTICS (V_{CC} = 5 V ±10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Input 'Low' voltage	V_{IL}		-0.3		0.8	V	
Input 'High' voltage	V_{IH}		2.2		V_{CC} +0.3	V	
Output 'Low' voltage	V_{OL}	I_{OL} = 2.0 mA			0.4	V	
Output 'High' voltage	V_{OH}	I_{OH} = -400 µA	2.4			V	
Input leakage current	$\lvert I_{LI} \rvert$	V_{IN} = 0 V to V_{CC}			10	µA	
Output leakage current	$\lvert I_{LO} \rvert$	V_{OUT} = 0 V to V_{CC}			10	µA	1
Operating current	I_{CC1}	t_{RC} = 120 ns			60	mA	2
	I_{CC2}	t_{RC} = 1 µs			45		
Standby current	I_{SB1}	$\overline{CE}$ = V_{IH}			2	mA	
	I_{SB2}	$\overline{CE}$ = V_{CC} - 0.2 V			100	µA	
Input capacitance	C_{IN}	f = 1 MHz, t_A = 25°C			10	pF	
Output capacitance	C_{OUT}				10	pF	

NOTES:
1. $\overline{CE}$ = V_{IH}, $\overline{OE}$ = V_{IH}, outputs open
2. V_{IN} = V_{IH}/V_{IL}, $\overline{CE}$ = V_{IL}, outputs open

CAUTION

To stabilize the power supply, it is recommended that a high-frequency bypass capacitor be connected between the V_{CC} pin and the GND pin.

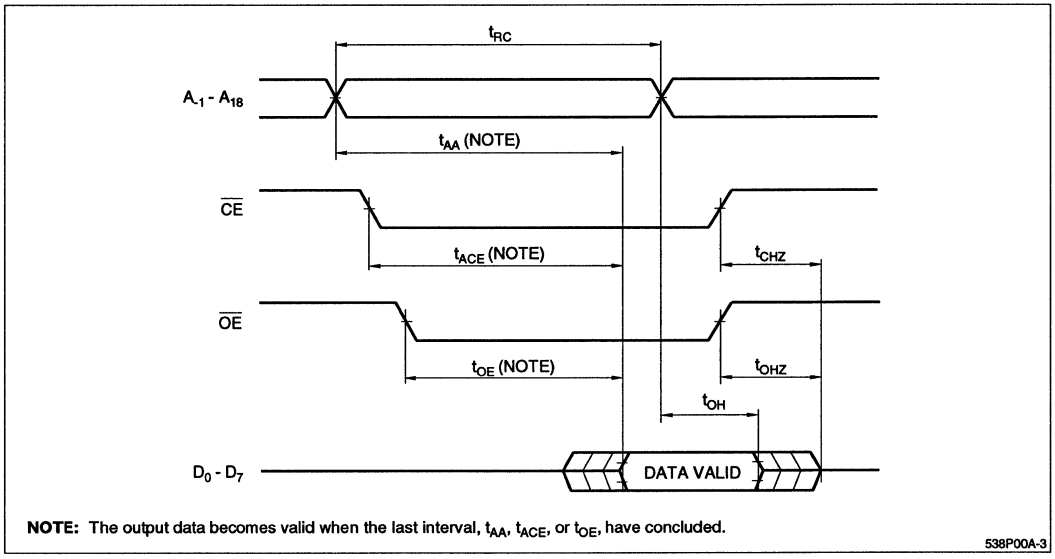
AC CHARACTERISTICS (V_{CC} = 5 V ±10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Read cycle time	t_{RC}	120			ns	
Address access time	t_{AA}			120	ns	
Chip enable time	t_{ACE}			120	ns	
Output enable time	t_{OE}			55	ns	
Output hold time	t_{OH}	5			ns	
CE to output in High-Z	t_{CHZ}			50	ns	1
OE to output in High-Z	t_{OHZ}			50	ns	

NOTE:
1. This is the time required for the outputs to become high-impedance.

AC TEST CONDITIONS

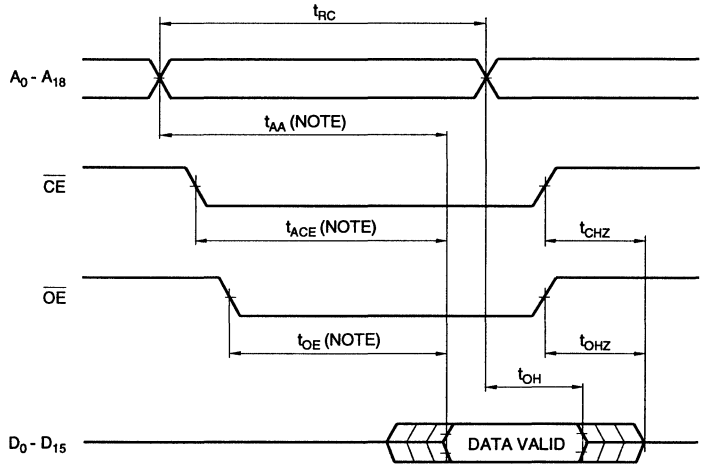
PARAMETER	RATING
Input voltage amplitude	0.6 V to 2.4 V
Input rise/fall time	10 ns
Input reference level	1.5 V
Output reference level	1.5 V
Output load condition	1TTL + 100 pF



NOTE: The output data becomes valid when the last interval, t_{AA}, t_{ACE}, or t_{OE}, have concluded.

538P00A-3

Figure 5. Byte Mode ($\overline{BYTE}$ = V_{IL})

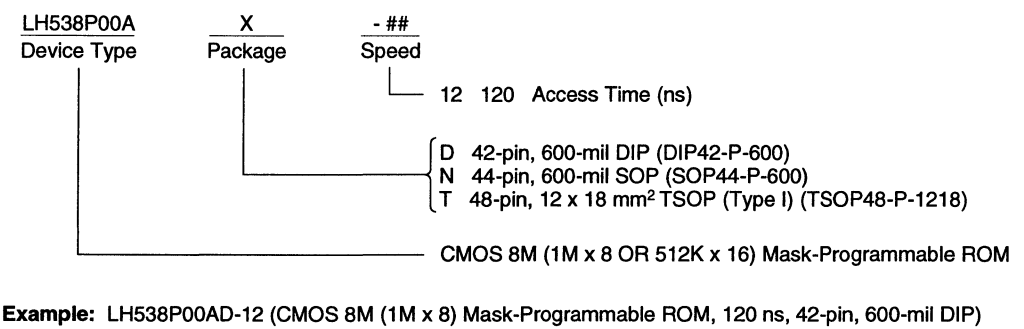


NOTE: The output data becomes valid when the last interval, t_{AA}, t_{ACE}, or t_{OE}, have concluded.

538P00A-4

Figure 6. Word Mode ($\overline{BYTE}$ = V_{IH})

ORDERING INFORMATION



Example: LH538P00AD-12 (CMOS 8M (1M x 8) Mask-Programmable ROM, 120 ns, 42-pin, 600-mil DIP)

538P00A-5

LH538R00A CMOS 8M (1M × 8) Mask-Programmable ROM

FEATURES

- 1,048,576 × 8 bit organization
- Access time: 120 ns (MAX.)
- Low-power consumption:
  Operating: 330 mW (MAX.)
  Standby: 550 µW (MAX.)
- Programmable output enable
- Fully-static operation
- TTL compatible I/O
- Three-state outputs
- Single +5 V power supply
- Packages:
  32-pin, 600-mil DIP
  32-pin, 525-mil SOP
  32-pin, 8 × 20 mm^2 TSOP (Type II)

DESCRIPTION

The LH538R00A is a mask-programmable ROM organized as 1,048,576 × 8 bits. It is fabricated using silicon-gate CMOS process technology.

PIN CONNECTIONS

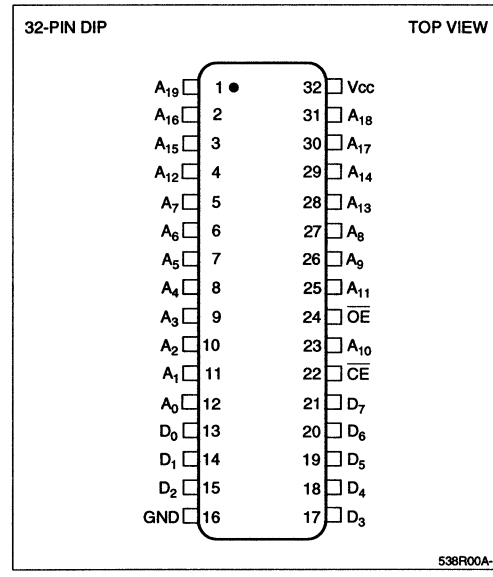


Figure 1. Pin Connections for DIP Package

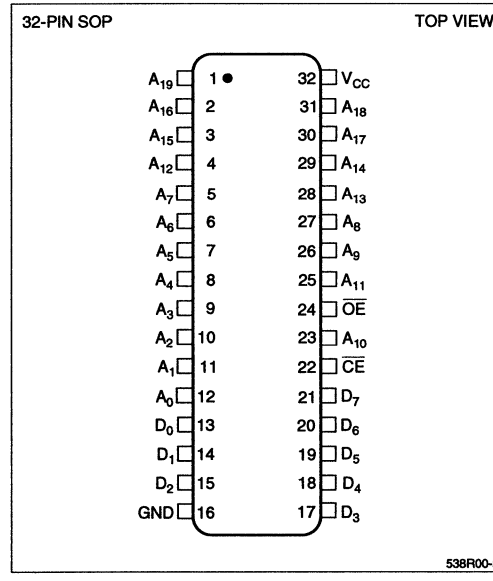


Figure 2. Pin Connections for SOP Package

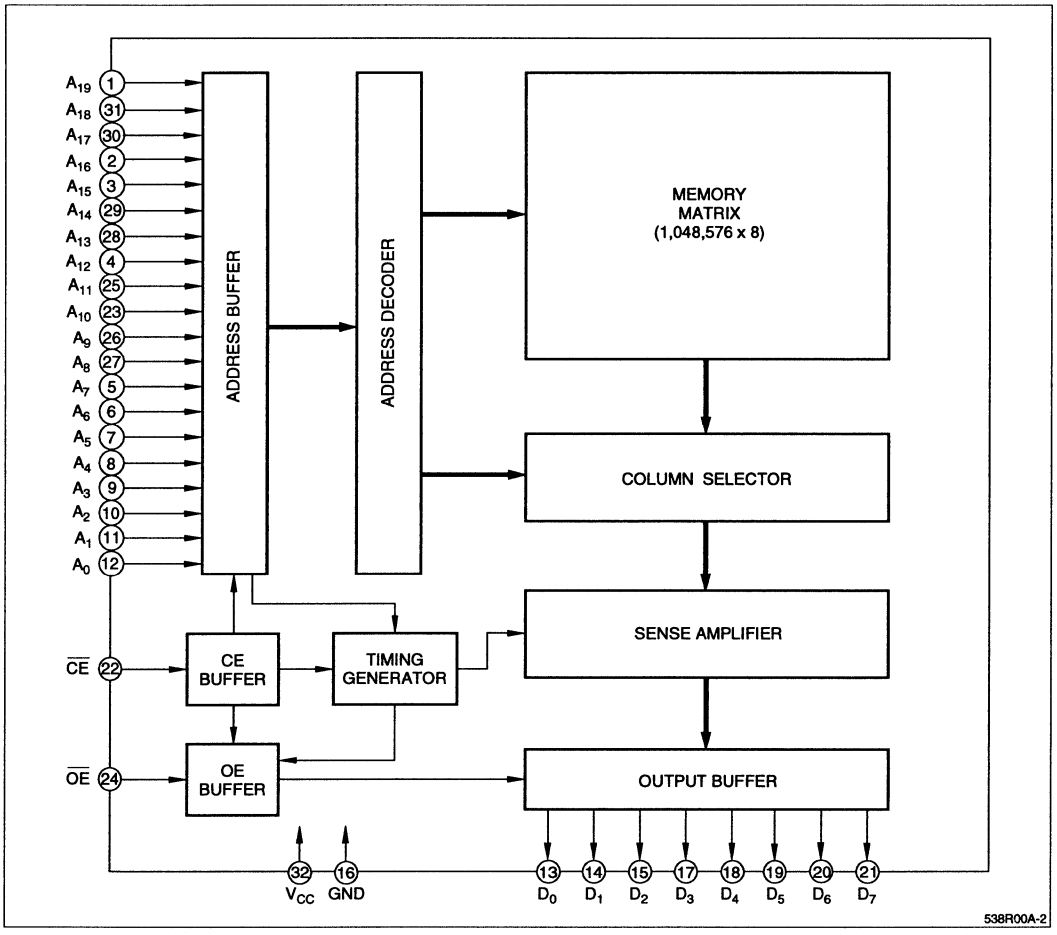


Figure 3. LH538R00A Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME
A_0 - A_{19}	Address input
D_0 - D_7	Data output
$\overline{CE}$	Chip Enable input

SIGNAL	PIN NAME
$\overline{OE}$	Output Enable input
V_{CC}	Power supply (+5 V)
GND	Ground

TRUTH TABLE

$\overline{CE}$	$\overline{OE}$	D_0 - D_7	SUPPLY CURRENT
H	X	High-Z	Standby (I_{SB})
L	H	High-Z	Operating (I_{CC})
L	L	D_{OUT}	Operating (I_{CC})

NOTE:
X = H or L

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Supply voltage	V_{CC}	-0.3 to +7.0	V
Input voltage	V_{IN}	-0.3 to V_{CC} +0.3	V
Output voltage	V_{OUT}	-0.3 to V_{CC} +0.3	V
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	4.5	5.0	5.5	V

DC CHARACTERISTICS (V_{CC} = 5 V ±10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Input 'Low' voltage	V_{IL}		-0.3		0.8	V	
Input 'High' voltage	V_{IH}		2.2		V_{CC} +0.3	V	
Output 'Low' voltage	V_{OL}	I_{OL} = 2.0 mA			0.4	V	
Output 'High' voltage	V_{OH}	I_{OH} = -400 µA	2.4			V	
Input leakage current	$\lvert I_{LI} \rvert$	V_{IN} = 0 V to V_{CC}			10	µA	
Output leakage current	$\lvert I_{LO} \rvert$	V_{OUT} = 0 V to V_{CC}			10	µA	1
Operating current	I_{CC1}	t_{RC} = 120 ns			60	mA	2
	I_{CC2}	t_{RC} = 1 µs			45		
Standby current	I_{SB1}	$\overline{CE}$ = V_{IH}			3	mA	
	I_{SB2}	$\overline{CE}$ = V_{CC} - 0.2 V			100	µA	
Input capacitance	C_{IN}	f = 1 MHz, t_A = 25°C			10	pF	
Output capacitance	C_{OUT}				10	pF	

NOTES:
1. $\overline{OE}$ = V_{IH}, $\overline{CE}$ = V_{IH}, outputs open
2. V_{IN} = V_{IH}/V_{IL}, $\overline{CE}$ = V_{IL}, outputs open

AC CHARACTERISTICS (V_{CC} = 5 V ±10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Read cycle time	t_{RC}	120			ns	
Address access time	t_{AA}			120	ns	
Chip enable time	t_{ACE}			120	ns	
Output enable time	t_{OE}			55	ns	
Output hold time	t_{OH}	5			ns	
CE to output in High-Z	t_{CHZ}			50	ns	1
OE to output in High-Z	t_{OHZ}			50	ns	

NOTE:
1. This is the time required for the outputs to become high-impedance.

AC TEST CONDITIONS

PARAMETER	RATING
Input voltage amplitude	0.6 V to 2.4 V
Input rise/fall time	10 ns
Input reference level	1.5 V
Output reference level	1.5 V
Output load condition	1TTL + 100 pF

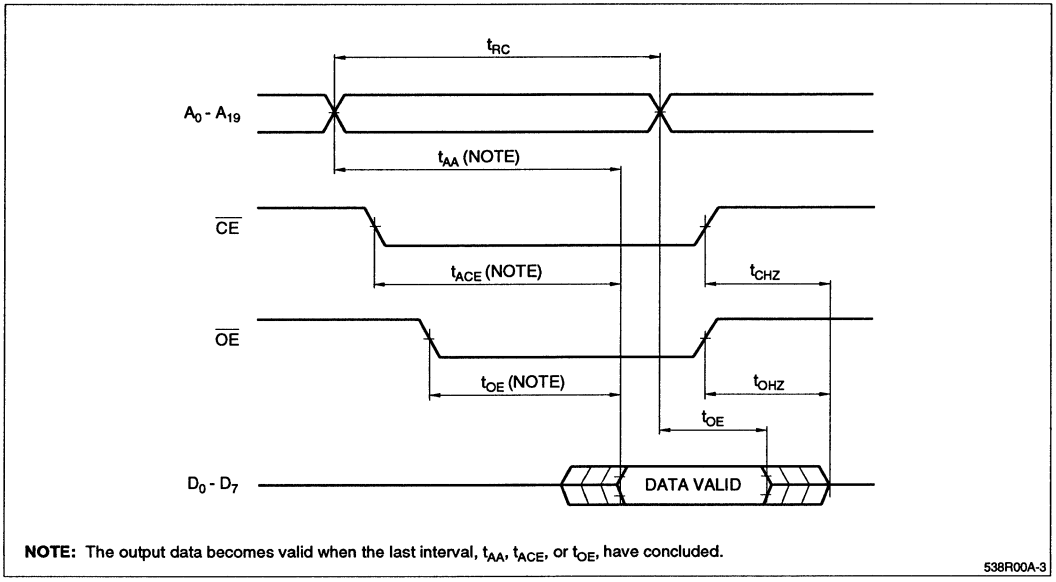
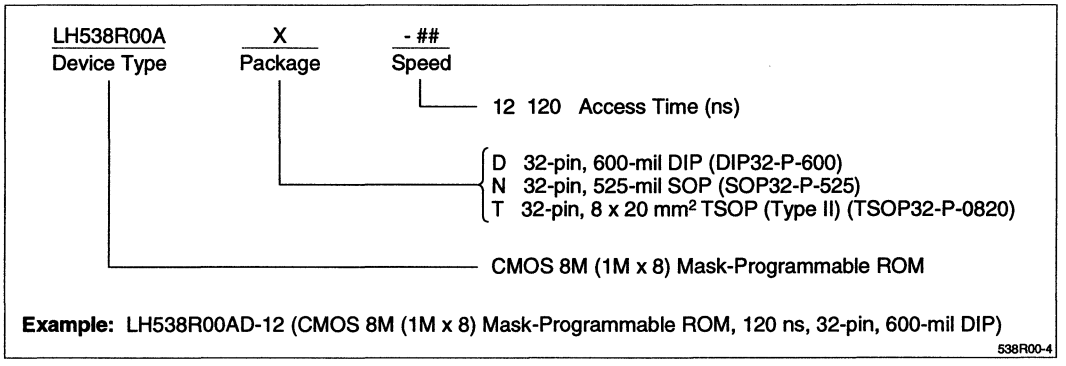


Figure 4. Timing Diagram

CAUTION

To stabilize the power supply, it is recommended that a high-frequency bypass capacitor be connected between the V_{CC} pin and the GND pin.

ORDERING INFORMATION



Example: LH538R00AD-12 (CMOS 8M (1M x 8) Mask-Programmable ROM, 120 ns, 32-pin, 600-mil DIP)

538R00-4

PRELIMINARY

LH538000-S

CMOS 8M (1M × 8/512K × 16)
3 V-Drive Mask-Programmable ROM

FEATURES

- Low power supply:
  2.6 to 5.5 V
- 1,048,576 × 8 bit organization
  (Byte mode)
  524,288 × 16 bit organization
  (Word mode)
- Access time:
  500 ns (MAX.) at 2.6 V ≤ V_{CC} < 4.5 V
  200 ns (MAX.) at 4.5 V ≤ V_{CC} ≤ 5.5 V
- Static operation
- Three-state output
- Packages:
  42-pin, 600-mil DIP
  44-pin, 600-mil SOP
  64-pin, 14 × 20 mm^2 QFP
  48-pin, 12 × 18 mm^2 TSOP (Type I)

DESCRIPTION

The LH538000-S is a CMOS 8M-bit mask-programmable ROM organized as 1,048,576 × 8 bits (Byte mode) or 524,288 × 16 bits (Word mode) that can be selected by $\overline{BYTE}$ input pin.

It is suited for use in compact battery back-up systems due to be operated on 3 V power supply.

PIN CONNECTIONS

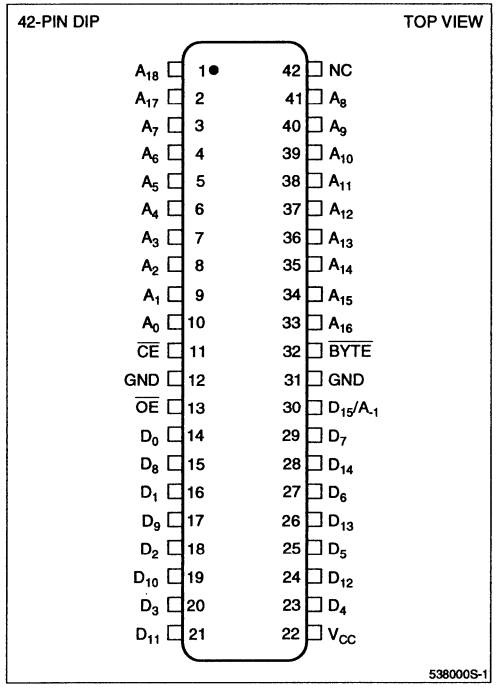


Figure 1. Pin Connections for DIP Package

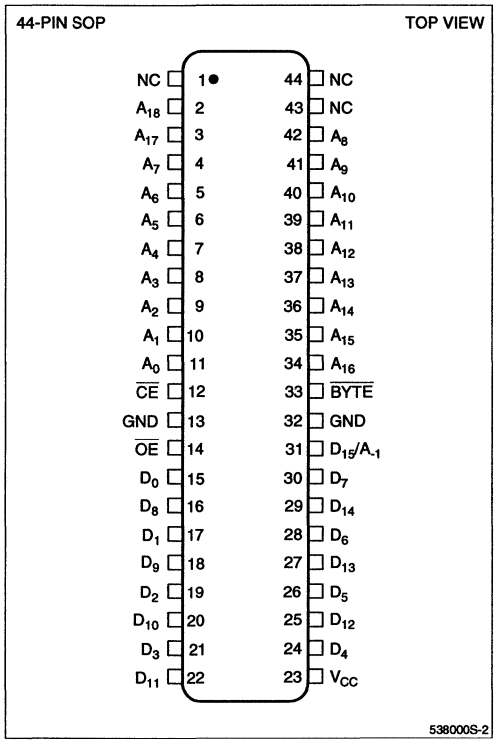


Figure 2. Pin Connections for SOP Package

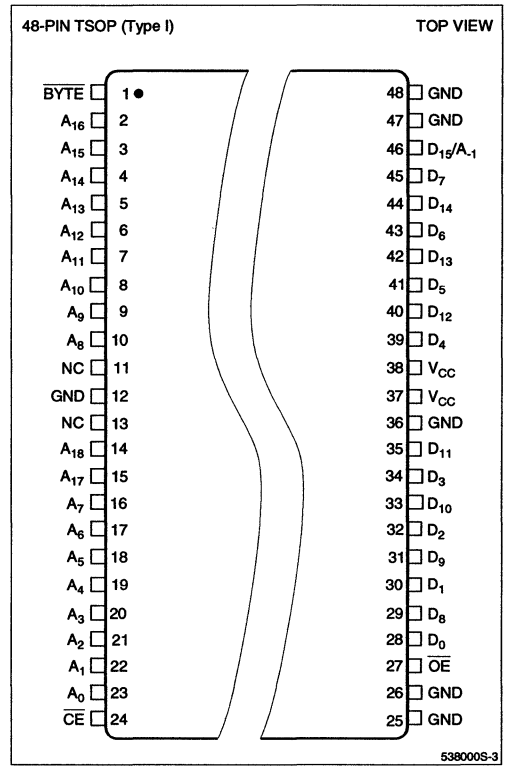


Figure 3. Pin Connections for TSOP Package

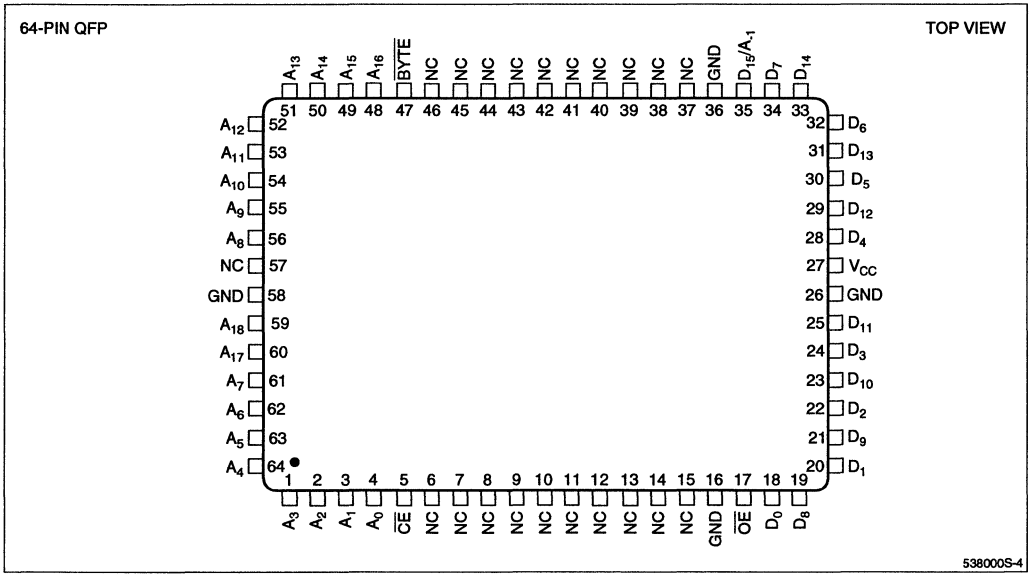


Figure 4. Pin Connections for QFP Package

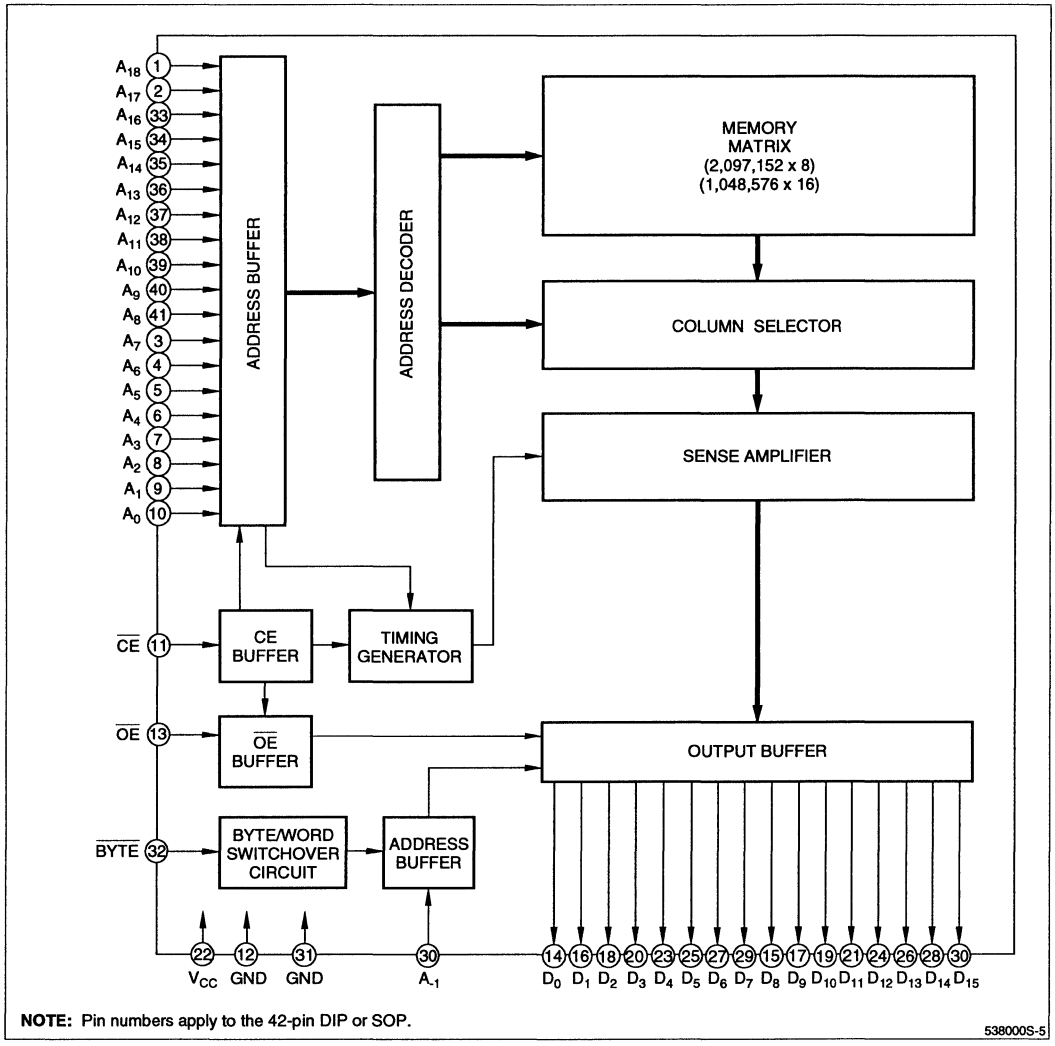


Figure 5. LH538000-S Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME
A_{-1} - A_{18}	Address input
D_0 - D_{15}	Data output
$\overline{BYTE}$	Byte/Word switch
$\overline{CE}$	Chip enable input

SIGNAL	PIN NAME
$\overline{OE}$	Output enable input
V_{CC}	Power supply
GND	Ground

NOTE:

The D_{15}/A_{-1} pin becomes LSB address input (A_{-1}) when the bit configuration is set to byte mode, and data output (D_{15}) when in word mode. The $\overline{BYTE}$ input pin selects bit configuration.

TRUTH TABLE

$\overline{CE}$	$\overline{OE}$	$\overline{BYTE}$	A_{-1} (D_{15})	DATA OUTPUT		MODE	ADDRESS INPUT		SUPPLY CURRENT
				D_0 - D_7	D_8 - D_{15}		LSB	MSB	
H	X	X	X	High-Z	High-Z	High-Z	–	–	Standby (I_{SB})
L	H	X	X	High-Z	High-Z		–	–	Operating (I_{CC})
L	L	H	Inhibit	D_0 - D_7	D_8 - D_{15}	16-bit	A_0	A_{18}	Operating (I_{CC})
L	L	L	L	D_0 - D_7	High-Z	8-bit	A_{-1}	A_{18}	Operating (I_{CC})
L	L	L	H	D_8 - D_{15}	High-Z	8-bit	A_{-1}	A_{18}	Operating (I_{CC})

NOTE:
X = Don't care, High-Z = High-impedance

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Supply voltage	V_{CC}	-0.3 to +7.0	V
Input voltage	V_{IN}	-0.3 to V_{CC} + 0.3	V
Output voltage	V_{OUT}	-0.3 to V_{CC} + 0.3	V
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	-55 to +150	°C

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to + 70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	2.6		5.5	V

DC CHARACTERISTICS (V_{CC} = 2.6 to 5.5 V, T_A = 0 to +70°C)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	MAX.	UNIT	NOTE
Input 'High' voltage	V_{IH}		0.8V_{CC}	V_{CC} + 0.3	V	
Input 'Low' voltage	V_{IL}		-0.3	0.4	V	
Output 'High' voltage	V_{OH}	I_{OH} = -100 µA	0.8V_{CC}		V	
Output 'Low' voltage	V_{OL}	I_{OL} = 400 µA		0.4	V	
Input leakage current	$\lvert I_{LI} \rvert$	V_{IN}= 0 V to V_{CC}		10	µA	
Output leakage current	$\lvert I_{LO} \rvert$	V_{OUT} = 0 V to V_{CC}		10	µA	1
Operating current	I_{CC1}	t_{RC} = 200 ns		50	mA	2
	I_{CC2}	t_{RC} = 1 µs		40	mA	2
	I_{CC3}	t_{RC} = 200 ns		45	mA	3
	I_{CC4}	t_{RC} = 1 µs		35	mA	3
Standby current	I_{SB1}	$\overline{CE}$ = V_{IH}		3	mA	
	I_{SB2}	$\overline{CE}$ = V_{CC} - 0.2 V		100	µA	
Input capacitance	C_{IN}	f = 1 MHz, T_A = +25°C		10	pF	
Output capacitance	C_{OUT}			10	pF	

NOTES:
1. $\overline{CE}$ = V_{IH}, $\overline{OE}$ = V_{IH}, outputs open
2. V_{IN} = V_{IH}, V_{IL}, $\overline{CE}$ = V_{IL}, outputs open
3. V_{IN} = (V_{CC} - 0.2 V), 0.2 V, $\overline{CE}$ = 0.2 V, outputs open

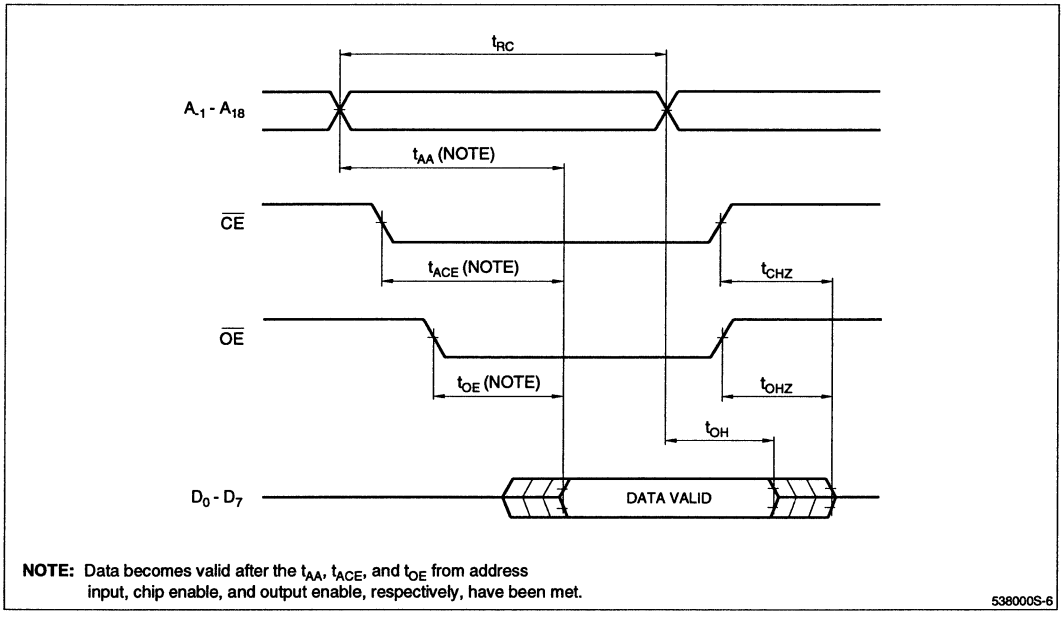
AC CHARACTERISTICS (T_A = 0 to +70°C)

PARAMETER	SYMBOL	2.6 ≤ Vcc < 4.5		4.5 ≤ Vcc ≤ 5.5		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.		
Read cycle time	t_{RC}	500		200		ns	
Address access time	t_{AA}		500		200	ns	
Chip enable time	t_{ACE}		500		200	ns	
Output enable time	t_{OE}		150		80	ns	
Output hold time	t_{OH}	10		5		ns	
CE to output in High-Z	t_{CHZ}		150		70	ns	1
OE to output in High-Z	t_{OHZ}		150		70	ns	

NOTE:
1. This is the time required for the outputs to become high-impedance.

AC TEST CONDITIONS

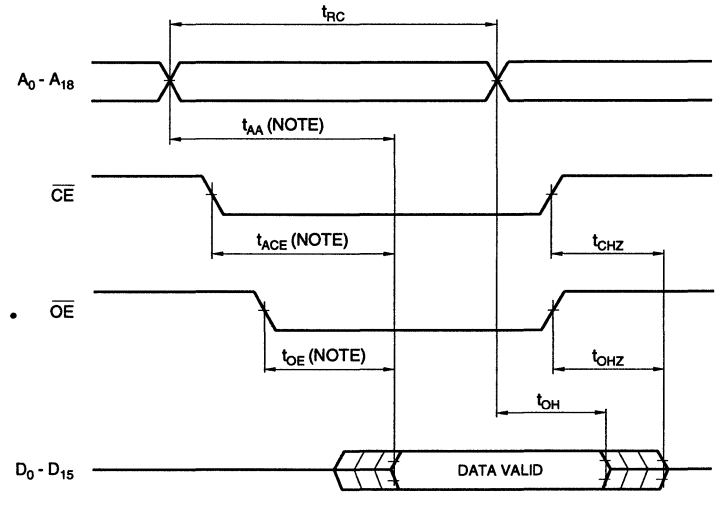
PARAMETER	RATING
Input voltage amplitude	0.4 to 2.6 V
Input rise/fall time	10 ns
Input/output reference level	1.5 V
Output load condition	1 TTL + 100 pF



NOTE: Data becomes valid after the t_{AA}, t_{ACE}, and t_{OE} from address input, chip enable, and output enable, respectively, have been met.

538000S-6

Figure 6. Byte Mode ($\overline{BYTE}$ = V_{IL})



NOTE: Data becomes valid after the t_{AA}, t_{ACE}, and t_{OE} from address input, chip enable, and output enable, respectively, have been met.

538000S-7

Figure 7. Word Mode ($\overline{BYTE}$ = V_{IH})

ORDERING INFORMATION

LH538000-S — Device Type
X — Package
- ## — Speed

50 500 Access Time (ns)

- D 42-pin, 600-mil DIP (DIP42-P-600)
- M 64-pin, 14 x 20 mm² QFP (QFP64-P-1420)
- N 44-pin, 600-mil SOP (SOP44-P-600)
- T 48-pin, 12 x 18 mm² TSOP (TSOP48-P-1218: Type I)

CMOS 8M (1M x 8 OR 512K x 16) Mask-Programmable ROM

Example: LH538000-SD-50 (CMOS 8M (1M x 8) Mask-Programmable ROM, 200 ns, 42-pin, 600-mil DIP)

538000S-8

LH538300B

CMOS 8M (1M × 8) Mask-Programmable ROM

FEATURES

- 1,048,576 × 8 bit organization
- Access time: 150 ns (MAX.)
- Low-power consumption:
  Operating: 275 mW (MAX.)
  Standby: 550 µW (MAX.)
- Fully-static operation
- TTL compatible I/O
- Three-state outputs
- Single +5 V power supply
- Packages:
  32-pin, 600-mil DIP
  32-pin, 525-mil SOP
  32-pin, 8 × 20 mm^2 TSOP (Type II)

DESCRIPTION

The LH538300B is a mask-programmable ROM organized as 1,048,576 × 8 bits. It is fabricated using silicon-gate CMOS process technology.

PIN CONNECTIONS

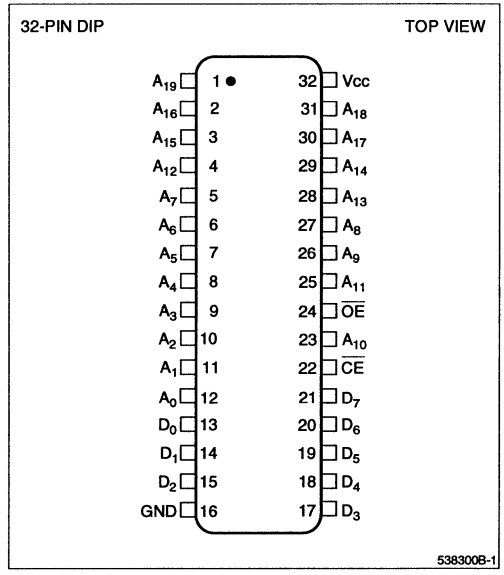


Figure 1. Pin Connections for DIP Package

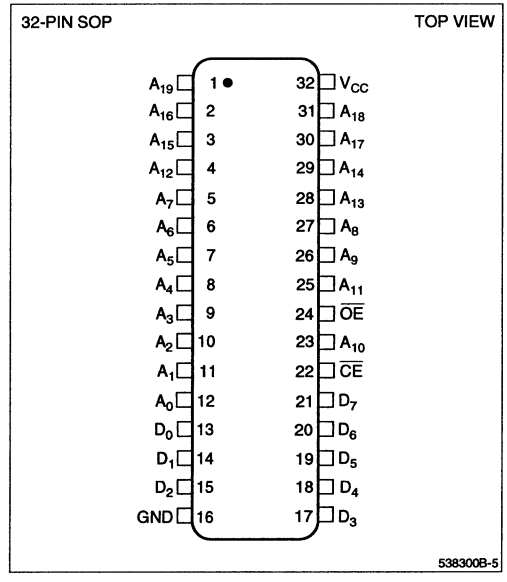


Figure 2. Pin Connections for SOP Package

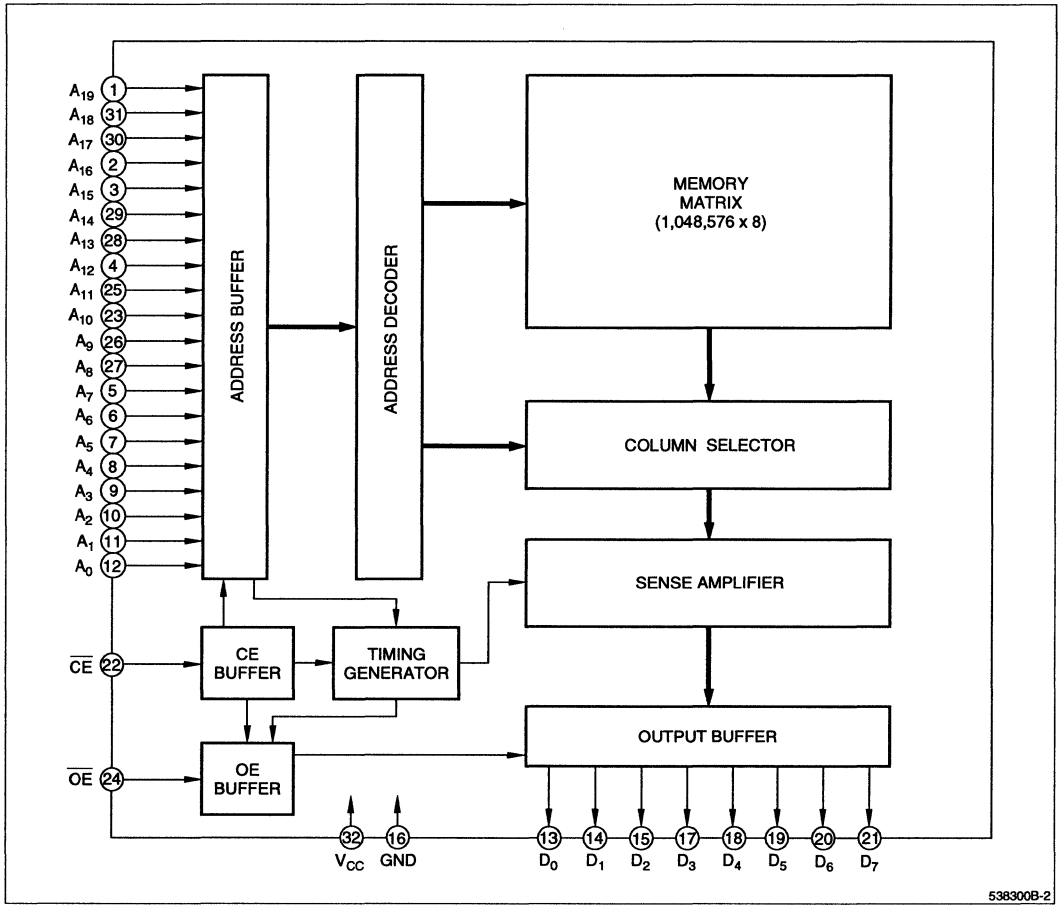


Figure 3. LH538300B Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME
A_0 - A_{19}	Address input
D_0 - D_7	Data output
$\overline{CE}$	Chip Enable input

SIGNAL	PIN NAME
$\overline{OE}$	Output Enable input
V_{CC}	Power supply (+5 V)
GND	Ground

TRUTH TABLE

$\overline{CE}$	$\overline{OE}$	D_0 - D_7	SUPPLY CURRENT
H	X	High-Z	Standby (I_{SB})
L	H	High-Z	Operating (I_{CC})
L	L	D_{OUT}	Operating (I_{CC})

NOTE:
X = H or L

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Supply voltage	V_{CC}	-0.3 to +7.0	V
Input voltage	V_{IN}	-0.3 to V_{CC} +0.3	V
Output voltage	V_{OUT}	-0.3 to V_{CC} +0.3	V
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	4.5	5.0	5.5	V

DC CHARACTERISTICS (V_{CC} = 5 V ±10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Input 'Low' voltage	V_{IL}		-0.3		0.8	V	
Input 'High' voltage	V_{IH}		2.2		V_{CC} +0.3	V	
Output 'Low' voltage	V_{OL}	I_{OL} = 2.0 mA			0.4	V	
Output 'High' voltage	V_{OH}	I_{OH} = -400 µA	2.4			V	
Input leakage current	$\lvert I_{LI} \rvert$	V_{IN} = 0 V to V_{CC}			10	µA	
Output leakage current	$\lvert I_{LO} \rvert$	V_{OUT} = 0 V to V_{CC}			10	µA	1
Operating current	I_{CC1}	t_{RC} = 150 ns			50	mA	2
	I_{CC2}	t_{RC} = 1 µs			40		
Standby current	I_{SB1}	$\overline{CE}$ = V_{IH}			3	mA	
	I_{SB2}	$\overline{CE}$ = V_{CC} - 0.2 V			100	µA	
Input capacitance	C_{IN}	f = 1 MHz, t_A = 25°C			10	pF	
Output capacitance	C_{OUT}				10	pF	

NOTES:
1. $\overline{OE}$ = V_{IH}, $\overline{CE}$ = V_{IH}, outputs open
2. V_{IN} = V_{IH}/V_{IL}, $\overline{CE}$ = V_{IL}, outputs open

AC CHARACTERISTICS (V_{CC} = 5 V ±10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Read cycle time	t_{RC}	150			ns	
Address access time	t_{AA}			150	ns	
Chip enable time	t_{ACE}			150	ns	
Output enable time	t_{OE}			70	ns	
Output hold time	t_{OH}	5			ns	
CE to output in High-Z	t_{CHZ}			60	ns	1
OE to output in High-Z	t_{OHZ}			60	ns	

NOTE:
1. This is the time required for the outputs to become high-impedance.

AC TEST CONDITIONS

PARAMETER	RATING
Input voltage amplitude	0.6 V to 2.4 V
Input rise/fall time	10 ns
Input reference level	1.5 V
Output reference level	0.8 V and 2.2 V
Output load condition	1TTL +100 pF

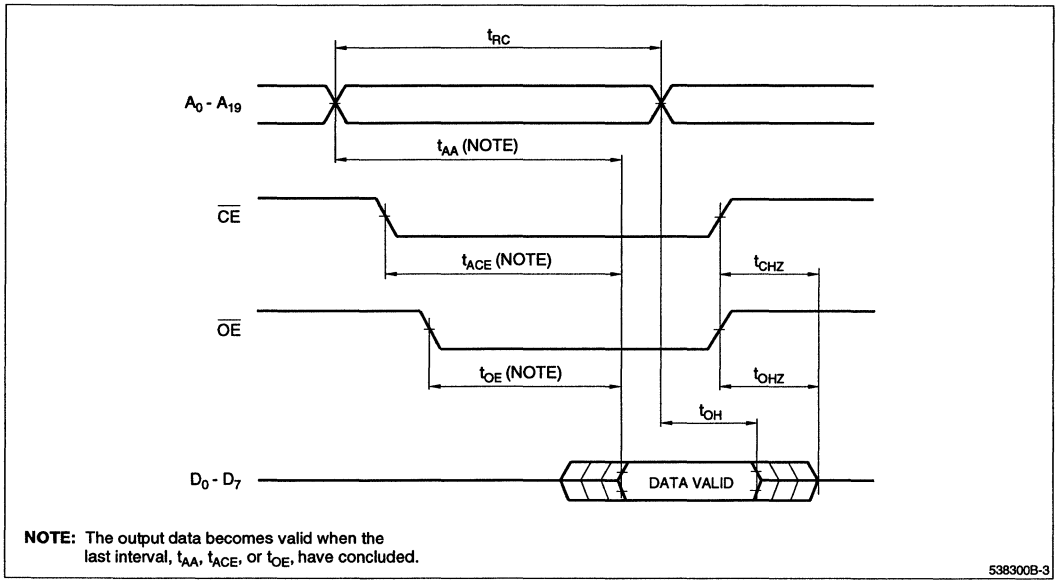
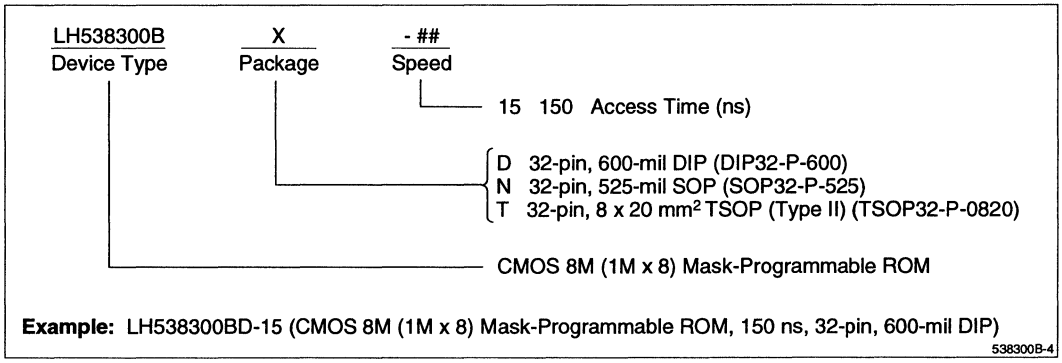


Figure 4. Timing Diagram

CAUTION

To stabilize the power supply, it is recommended that a high-frequency bypass capacitor be connected between the V_{CC} pin and the GND pin.

ORDERING INFORMATION



Example: LH538300BD-15 (CMOS 8M (1M x 8) Mask-Programmable ROM, 150 ns, 32-pin, 600-mil DIP)

538300B-4

LH538500B

CMOS 8M (1M × 8/512K × 16) Mask-Programmable ROM

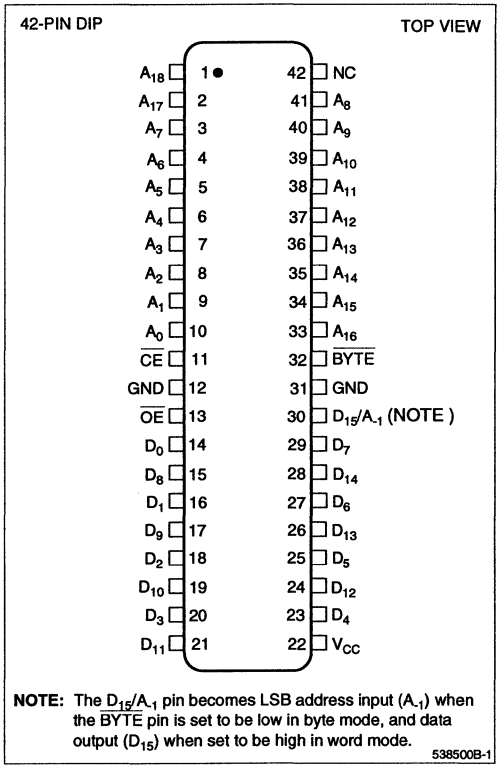
FEATURES

- 1,048,576 × 8 bit organization
  (Byte mode)
  524,288 × 16 bit organization
  (Word mode)
- Access time: 150 ns (MAX.)
- Power consumption:
  Operating: 275 mW (MAX.)
  Standby: 550 µW (MAX.)
- Static operation
- TTL compatible I/O
- Three-state outputs
- Single +5 V power supply
- Packages:
  42-pin, 600-mil DIP
  44-pin, 600-mil SOP
  44-pin, 14 × 14 mm^2 QFP
  64-pin, 14 × 20 mm^2 QFP
  48-pin, 12 × 18 mm^2 TSOP (Type I)

DESCRIPTION

The LH538500B is an 8M-bit mask-programmable ROM organized as 1,048,576 × 8 bits (Byte mode) or 524,288 × 16 bits (Word mode) that can be selected by $\overline{BYTE}$ input pin. It is fabricated using silicon-gate CMOS process technology.

PIN CONNECTIONS



NOTE: The D_{15}/A_{-1} pin becomes LSB address input (A_{-1}) when the $\overline{BYTE}$ pin is set to be low in byte mode, and data output (D_{15}) when set to be high in word mode.

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Figure 1. Pin Connections for DIP Package

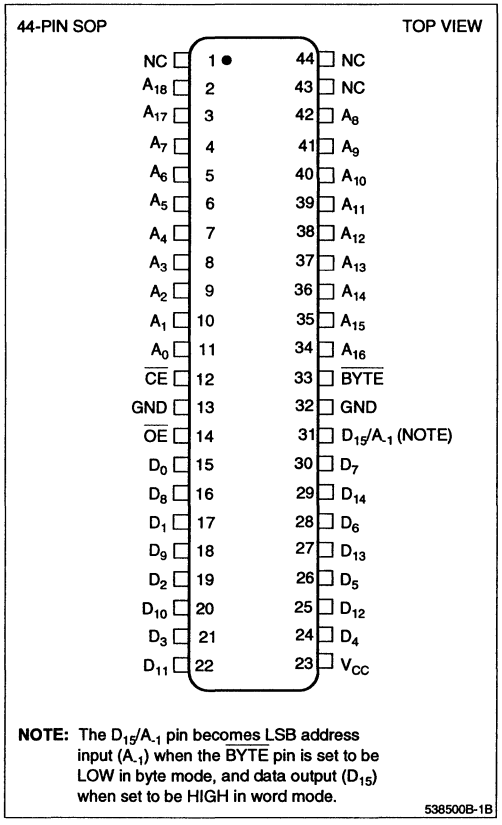


Figure 2. Pin Connections for SOP Package

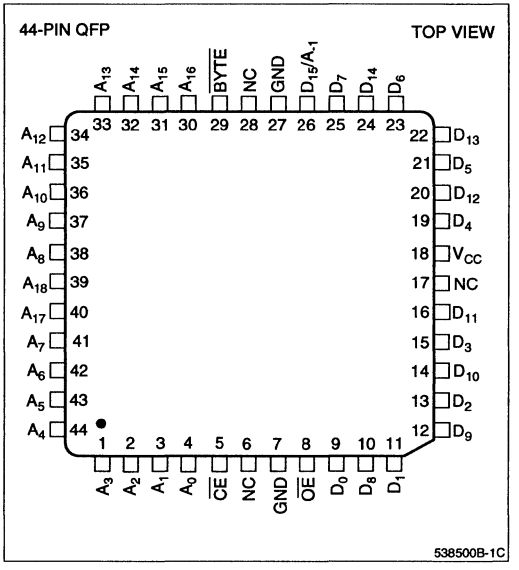


Figure 3. Pin Connections for 44-Pin QFP Package

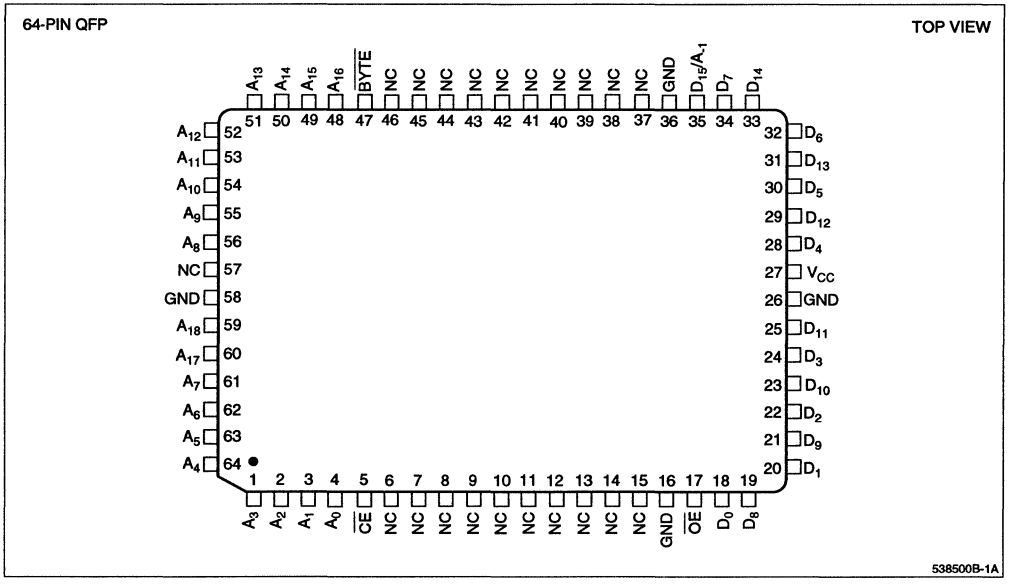


Figure 4. Pin Connections for 64-Pin QFP Package

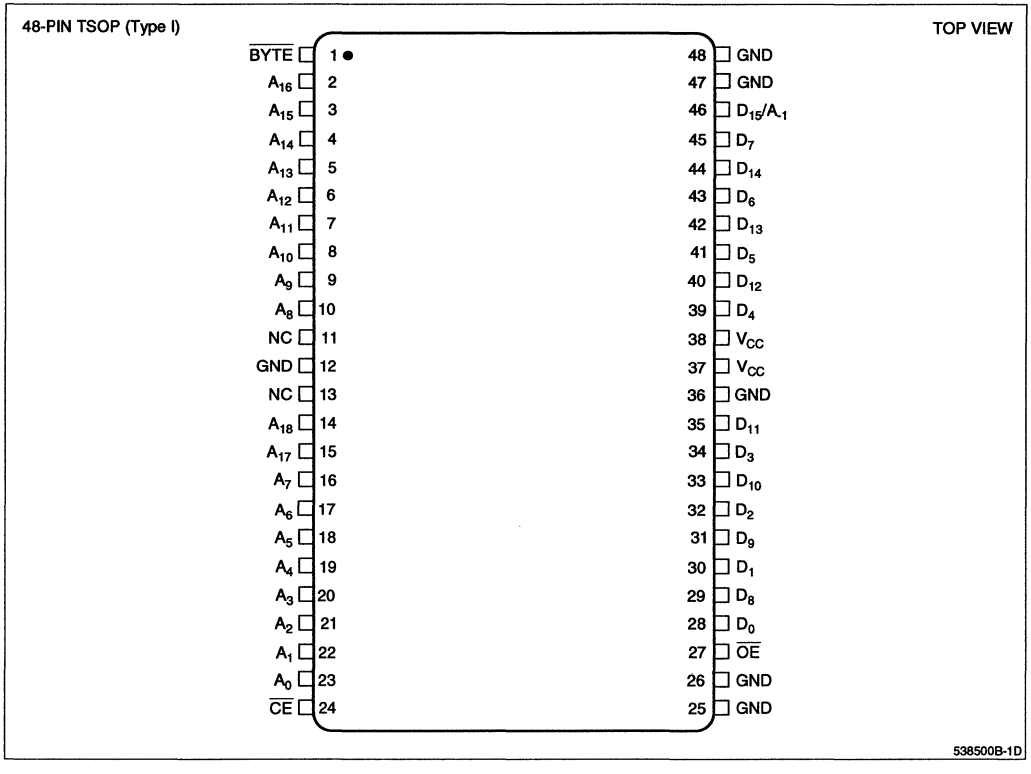


Figure 5. Pin Connections for TSOP Package

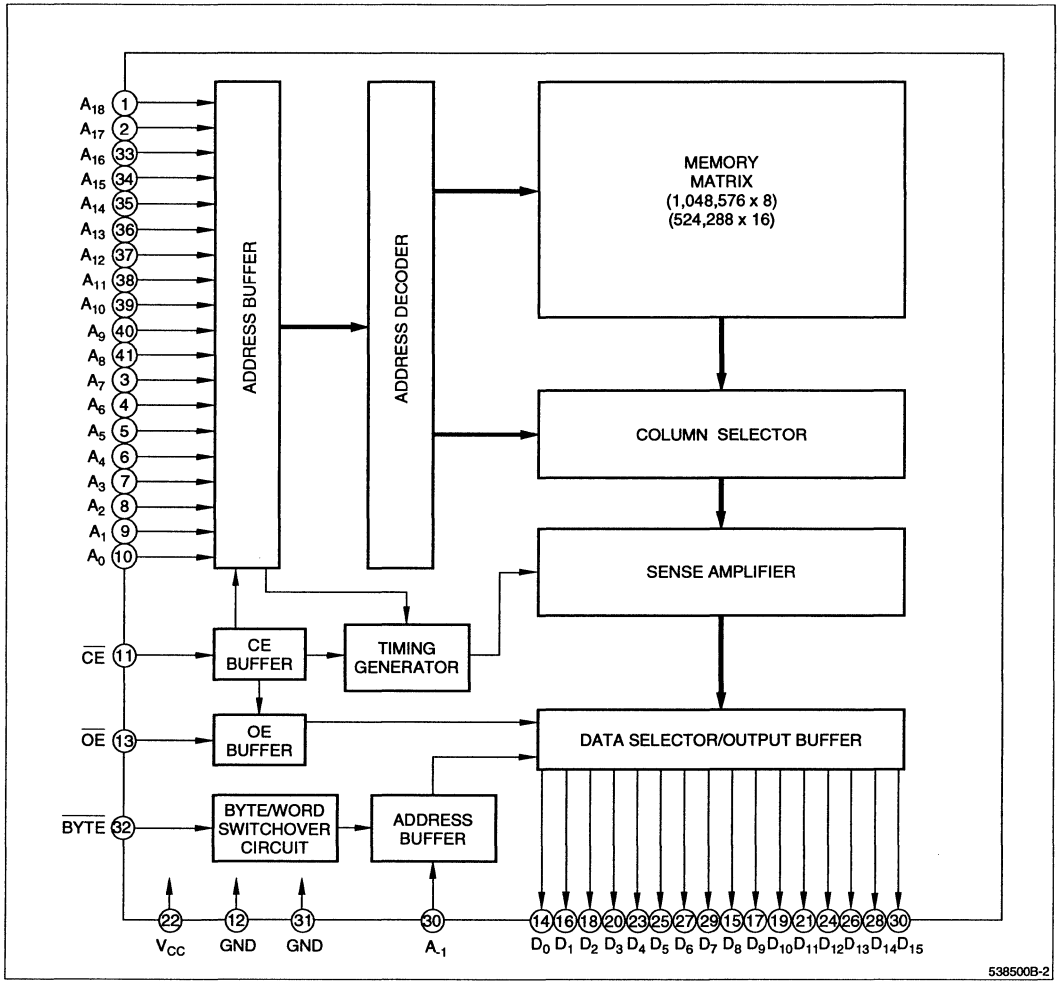


Figure 6. LH538500B Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME
A_{-1} - A_{18}	Address input
D_0 - D_{15}	Data output
$\overline{CE}$	Chip enable input
$\overline{OE}$	Output enable input

SIGNAL	PIN NAME
$\overline{BYTE}$	Byte/word switch
V_{CC}	Power supply (+5 V)
GND	Ground
NC	Non connection

TRUTH TABLE

$\overline{CE}$	$\overline{OE}$	$\overline{BYTE}$	A_{-1} (D_{15})	DATA OUTPUT		ADDRESS INPUT		SUPPLY CURRENT
				D_0 - D_7	D_8 - D_{15}	LSB	MSB	
H	X	X	X	High-Z	High-Z	–	–	Standby (I_{SB})
L	H	X	X	High-Z	High-Z	–	–	Operating (I_{CC})
L	L	H	–	D_0 - D_7	D_8 - D_{15}	A_0	A_{18}	Operating (I_{CC})
L	L	L	L	D_0 - D_7	High-Z	A_{-1}	A_{18}	Operating (I_{CC})
L	L	L	H	D_8 - D_{15}	High-Z	A_{-1}	A_{18}	Operating (I_{CC})

NOTE:
X = H or L

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Supply voltage	V_{CC}	-0.3 to +7.0	V
Input voltage	V_{IN}	-0.3 to V_{CC} +0.3	V
Output voltage	V_{OUT}	-0.3 to V_{CC} +0.3	V
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	4.5	5.0	5.5	V

DC CHARACTERISTICS (V_{CC} = 5 V ±10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Input 'Low' voltage	V_{IL}		-0.3		0.8	V	
Input 'High' voltage	V_{IH}		2.2		V_{CC} +0.3	V	
Output 'Low' voltage	V_{OL}	I_{OL} = 2.0 mA			0.4	V	
Output 'High' voltage	V_{OH}	I_{OH} = -400 µA	2.4			V	
Input leakage current	$\lvert I_{LI} \rvert$	V_{IN} = 0 V to V_{CC}			10	µA	
Output leakage current	$\lvert I_{LO} \rvert$	V_{OUT} = 0 V to V_{CC}			10	µA	1
Operating current	I_{CC1}	t_{RC} = 150 ns			50	mA	2
	I_{CC2}	t_{RC} = 1 µs			40		
Standby current	I_{SB1}	$\overline{CE}$ = V_{IH}			2	mA	
	I_{SB2}	$\overline{CE}$ = V_{CC} - 0.2 V			100	µA	
Input capacitance	C_{IN}	f = 1 MHz, t_A = 25°C			10	pF	
Output capacitance	C_{OUT}				10	pF	

NOTES:
1. $\overline{CE}$ = V_{IH}, $\overline{OE}$ = V_{IH}, outputs open
2. V_{IN} = V_{IH}/V_{IL}, $\overline{CE}$ = V_{IL}, outputs open

CAUTION

To stabilize the power supply, it is recommended that a high-frequency bypass capacitor be connected between the V_{CC} pin and the GND pin.

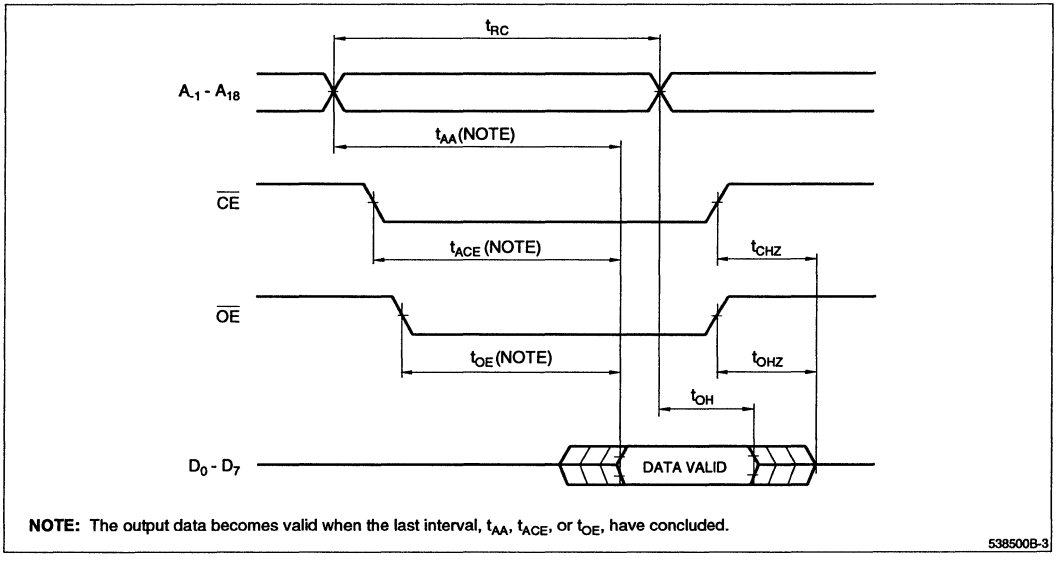
AC CHARACTERISTICS (V_{CC} = 5 V ±10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Read cycle time	t_{RC}	150			ns	
Address access time	t_{AA}			150	ns	
Chip enable time	t_{ACE}			150	ns	
Output enable time	t_{OE}			70	ns	
Output hold time	t_{OH}	5			ns	
CE to output in High-Z	t_{CHZ}			60	ns	1
OE to output in High-Z	t_{OHZ}			60	ns	

NOTE:
1. This is the time required for the outputs to become high-impedance.

AC TEST CONDITIONS

PARAMETER	RATING
Input voltage amplitude	0.6 V to 2.4 V
Input rise/fall time	10 ns
Input reference level	1.5 V
Output reference level	0.8 V and 2.2 V
Output load condition	1TTL + 100 pF



NOTE: The output data becomes valid when the last interval, t_{AA}, t_{ACE}, or t_{OE}, have concluded.

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Figure 7. Byte Mode ($\overline{BYTE}$ = V_{IL})

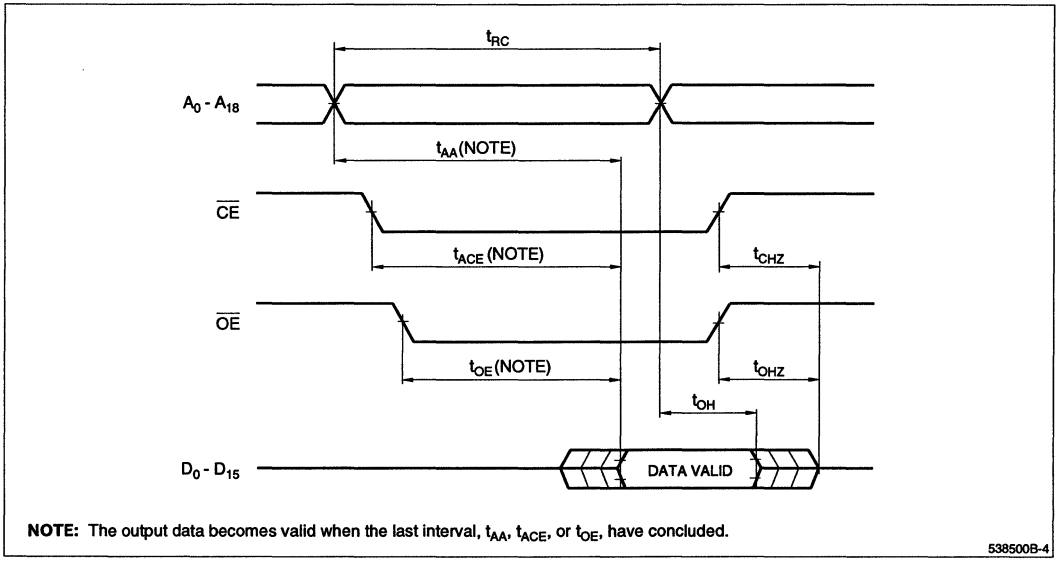
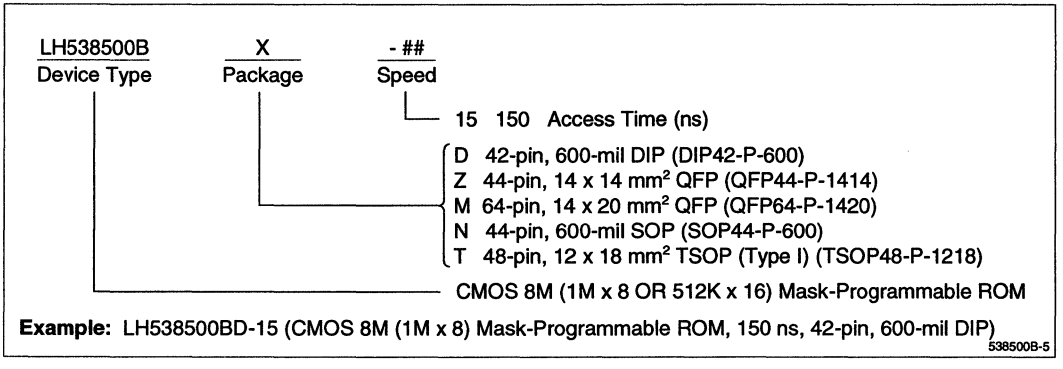


Figure 8. Word Mode ($\overline{BYTE}$ = V_{IH})

ORDERING INFORMATION



LH538600

CMOS 8M (1M × 8/512K × 16)
High-Speed Mask-Programmable ROM

FEATURES

- 1,048,576 × 8 bit organization
  (Byte mode)
  524,288 × 16 bit organization
  (Word mode)
- $\overline{\text{BYTE}}$ input pin selects bit configuration
- Access time: 100 ns (MAX.)
- Power consumption:
  Operating: 385 mW (MAX.)
  Standby: 550 µW (MAX.)
- Static operation (internal sync. system)
- TTL compatible I/O
- Three-state output
- Single +5 V power supply
- Packages:
  42-pin, 600-mil DIP
  44-pin, 600-mil SOP
  48-pin, 12 × 18 mm^2 TSOP (Type I)
  44-pin, 14 × 14 mm^2 QFP
  64-pin, 14 × 20 mm^2 QFP

DESCRIPTION

The LH538600 is a CMOS 8M-bit mask-programmable ROM organized as 1,048,576 × 8 bits (Byte mode) or 524,288 × 16 bits (Word mode) that can be selected by $\overline{\text{BYTE}}$ input pin. Due to its high-speed access of 100 ns, it is suited to high-speed laser printer, quality sound electronic musical instruments, etc.

PIN CONNECTIONS

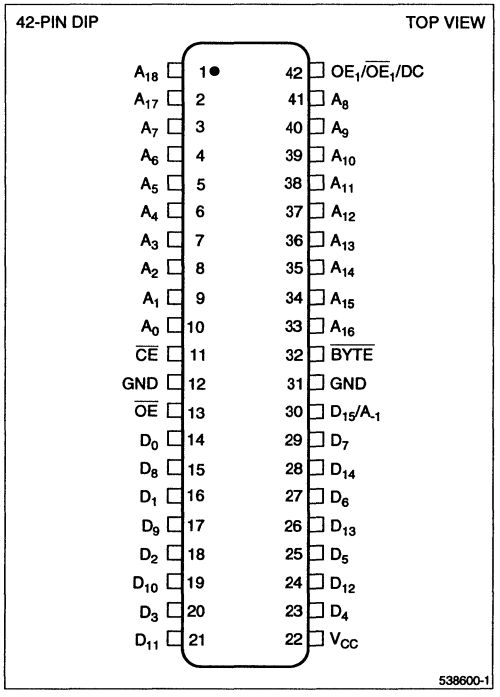


Figure 1. Pin Connections for DIP Package

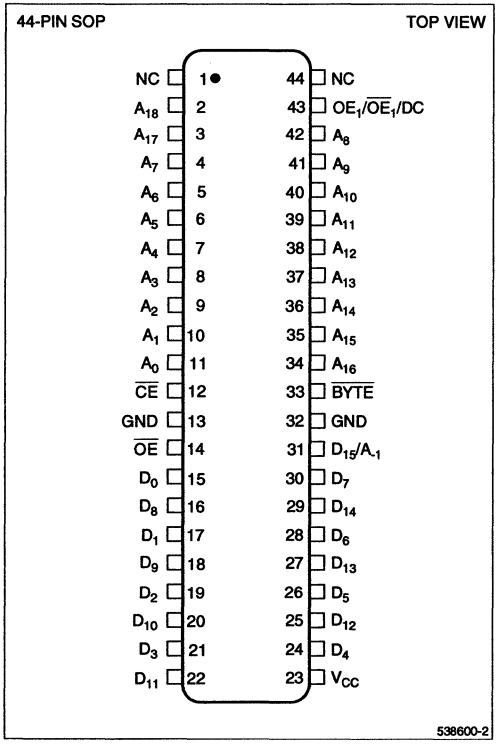


Figure 2. Pin Connections for SOP Package

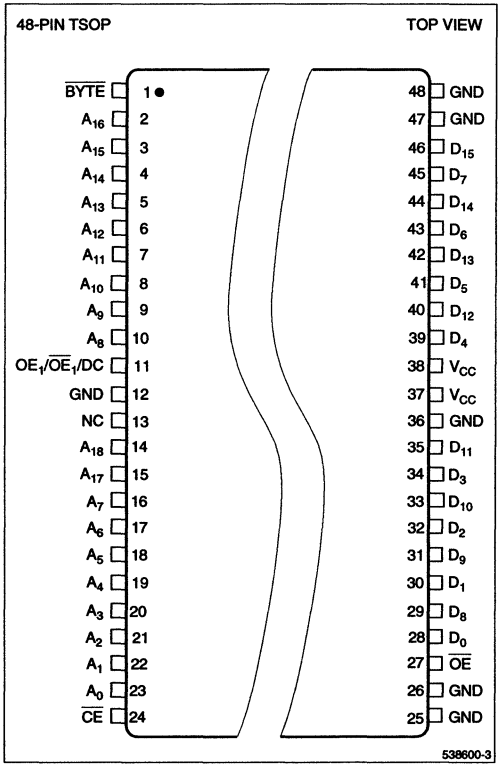


Figure 3. Pin Connections for TSOP Package

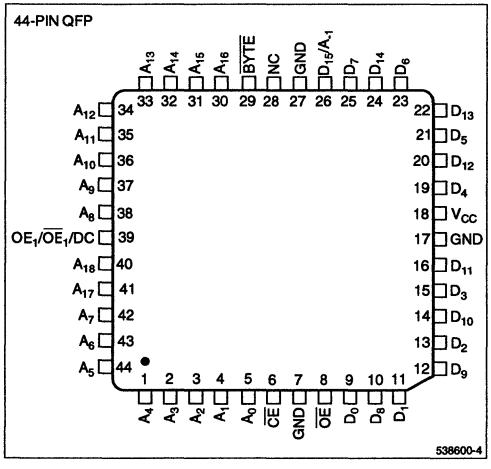


Figure 4. Pin Connections for 44-Pin QFP Package

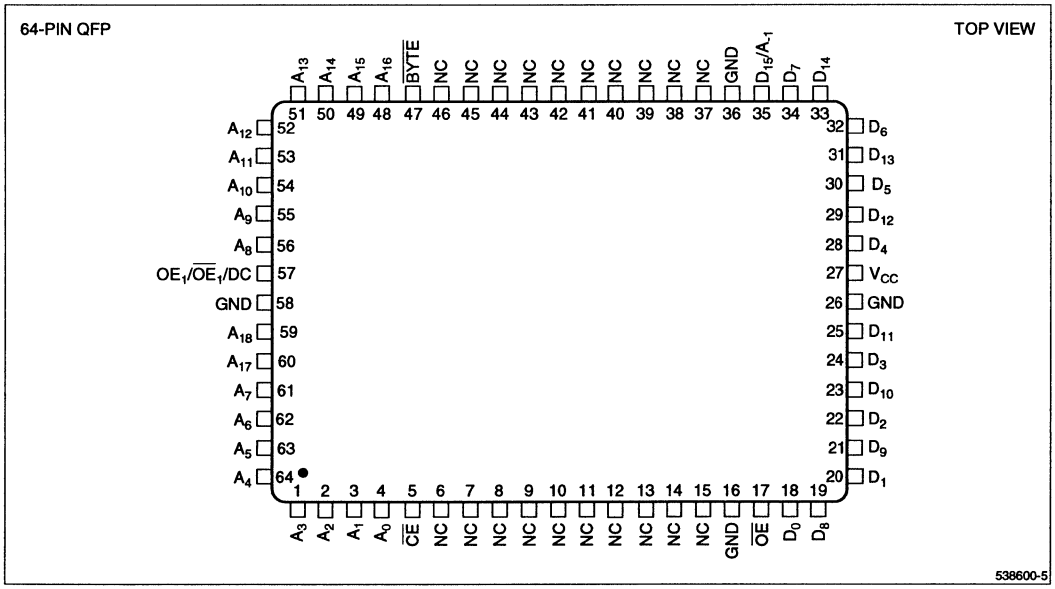


Figure 5. Pin Connections for 64-Pin QFP Package

PIN DESCRIPTION

SIGNAL	PIN NAME	NOTE
A_{-1}	Address input (BYTE mode)	1
A_0 - A_{18}	Address input	
D_0 - D_{15}	Data output	
$\overline{BYTE}$	8/16-bit Byte/Word mode switch input	
$\overline{CE}$	Chip enable input	

SIGNAL	PIN NAME	NOTE
$\overline{OE}$	Output enable input	
$OE_1/\overline{OE}_1/DC$	Output enable input/Don't care	2
V_{CC}	Power supply (+5 V)	
GND	Ground	

NOTES:
1. D_{15}/A_{-1} pin becomes LSB address input (A_{-1}) when the bit configuration is set in byte mode, and data output (D_{15}) when in word mode. The $\overline{BYTE}$ input pin selects bit configuration.
2. An active level of $OE_1/\overline{OE}_1/DC$ is mask-programmable.

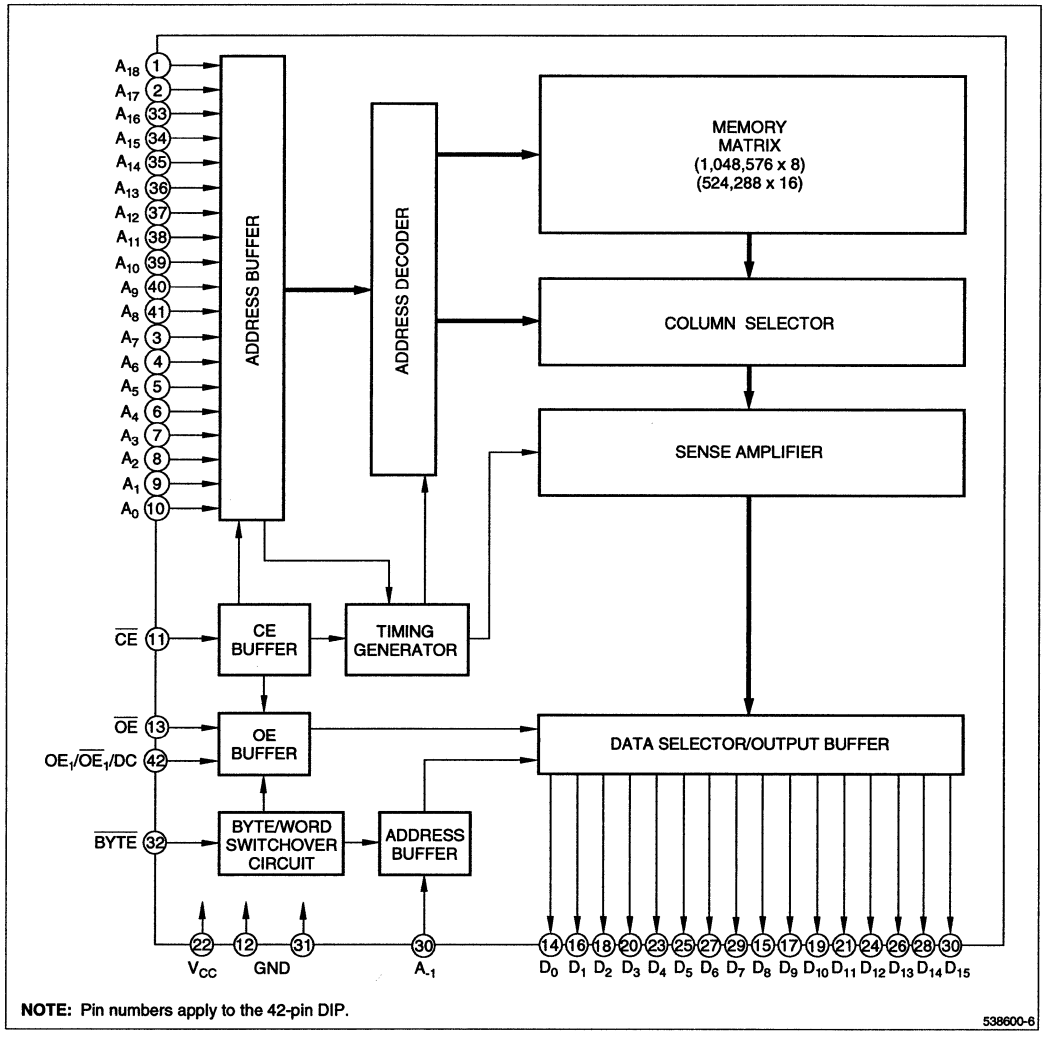


Figure 6. LH538600 Block Diagram

TRUTH TABLE

$\overline{CE}$	$\overline{OE}$/ $OE_1/\overline{OE_1}$	$\overline{BYTE}$	A_{-1} (D_{15})	DATA OUTPUT		MODE	ADDRESS INPUT		SUPPLY CURRENT
				D_0 - D_7	D_8 - D_{15}		LSB	MSB	
H	X	X	X	High-Z	High-Z	–	–	–	Standby
L	L/H	X	X	High-Z	High-Z		–	–	Operating
L	H/L	H	Inhibit	D_0 - D_7	D_8 - D_{15}	16-bit	A_0	A_{18}	Operating
L	H/L	L	L	D_0 - D_7	High-Z	8-bit	A_{-1}	A_{18}	Operating
L	H/L	L	H	D_8 - D_{15}	High-Z	8-bit	A_{-1}	A_{18}	Operating

NOTE:
X = Don't care, High-Z = High-impedance

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Supply voltage	V_{CC}	-0.3 to +7.0	V
Input voltage	V_{IN}	-0.3 to V_{CC} + 0.3	V
Output voltage	V_{OUT}	-0.3 to V_{CC} + 0.3	V
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	-55 to +150	°C

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to + 70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	4.5	5.0	5.5	V

DC CHARACTERISTICS (V_{CC} = 5 V ±10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	MAX.	UNIT	NOTE
Input 'High' voltage	V_{IH}		2.2	V_{CC} + 0.3	V	
Input 'Low' voltage	V_{IL}		-0.3	0.8	V	
Output 'High' voltage	V_{OH}	I_{OH} = -400 µA	2.4		V	
Output 'Low' voltage	V_{OL}	I_{OL} = 2.0 mA		0.4	V	
Input leakage current	$\lvert I_{LI} \rvert$	V_{IN}= 0 V, V_{CC}		10	µA	
Output leakage current	$\lvert I_{LO} \rvert$	V_{OUT} = 0 V, V_{CC}		10	µA	1
Operating current	I_{CC1}	t_{RC} = 100 ns		70	mA	2
	I_{CC2}	t_{RC} = 1 µs		60	mA	2
	I_{CC3}	t_{RC} = 100 ns		65	mA	3
	I_{CC4}	t_{RC} = 1 µs		55	mA	3
Standby current	I_{SB1}	$\overline{CE}$ = V_{IH}		3	mA	
	I_{SB2}	$\overline{CE}$ = V_{CC} - 0.2 V		100	µA	
Input capacitance	C_{IN}	f = 1 MHz, T_A = 25°C		10	pF	
Output capacitance	C_{OUT}			10	pF	

NOTES:
1. $\overline{CE}$ = V_{IH}, $\overline{OE}$ = V_{IH}, OE_1 = V_{IL}, $\overline{OE_1}$ = V_{IH}
2. V_{IN} = V_{IH}/V_{IL}, $\overline{CE}$ = V_{IL}, outputs open
3. V_{IH} = V_{CC} - 0.2 V/0.2 V, $\overline{CE}$ = 0.2 V, outputs open

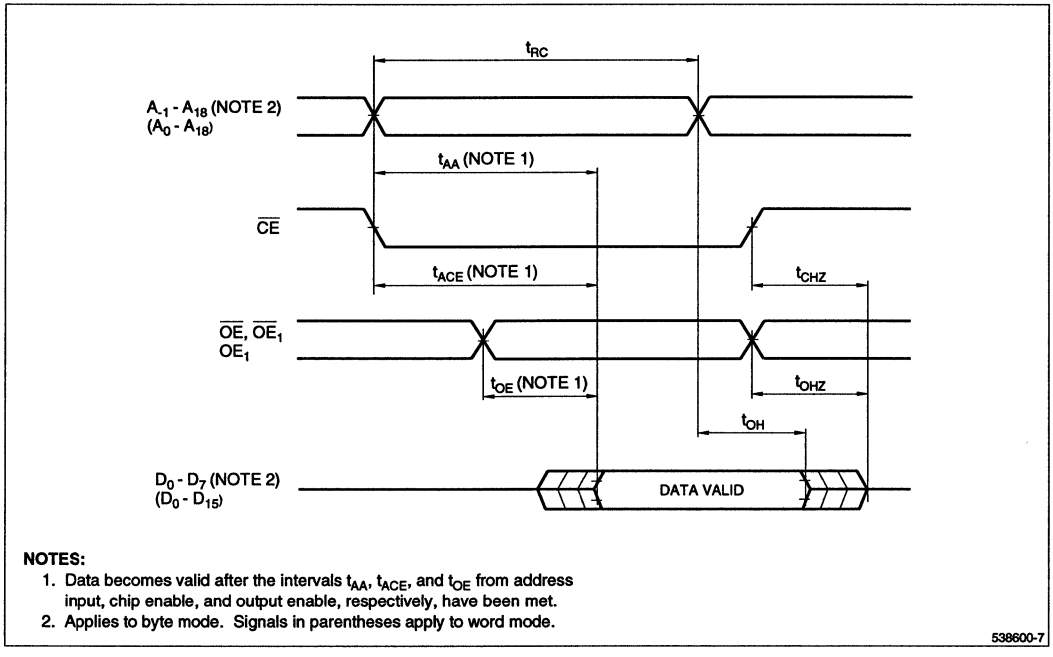
AC CHARACTERISTICS (V_{CC} = 5 V ±10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT	NOTE
Read cycle time	t_{RC}	100		ns	
Address access time	t_{AA}		100	ns	
Chip enable time	t_{ACE}		100	ns	
Output enable time	t_{OE}		40	ns	
Output hold time	t_{OH}	5		ns	
CE to output in High-Z	t_{CHZ}		40	ns	1
OE to output in High-Z	t_{OHZ}		40	ns	

NOTE:
1. This is the time required for the outputs to become high-impedance.

AC TEST CONDITIONS

PARAMETER	RATING
Input voltage amplitude	0.6 to 2.4 V
Input rise/fall time	10 ns
Input reference level	1.5 V
Output reference level	1.5 V
Output load	1 TTL + 100 pF

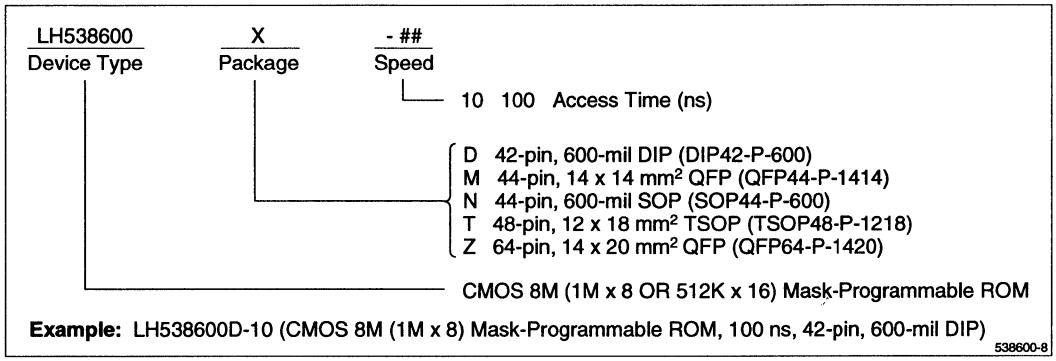


NOTES:
1. Data becomes valid after the intervals t_{AA}, t_{ACE}, and t_{OE} from address input, chip enable, and output enable, respectively, have been met.
2. Applies to byte mode. Signals in parentheses apply to word mode.

538600-7

Figure 4-7. Timing Diagram

ORDERING INFORMATION



Example: LH538600D-10 (CMOS 8M (1M x 8) Mask-Programmable ROM, 100 ns, 42-pin, 600-mil DIP)

LH5316500C

CMOS 16M (2M × 8/1M × 16)
Mask-Programmable ROM

FEATURES

- 2,097,152 × 8 bit organization
  (Byte mode)
  1,048,576 × 16 bit organization
  (Word mode)
- Access time: 150 ns (MAX.)
- Power consumption:
  Operating: 275 mW (MAX.)
  Standby: 550 µW (MAX.)
- Fully-static operation
- TTL compatible I/O
- Three-state outputs
- Single +5 V power supply
- Packages:
  42-pin, 600-mil DIP
  44-pin, 600-mil SOP
  48-pin, 12 × 18 mm^2 TSOP (Type I)

DESCRIPTION

The LH5316500C is a 16M-bit mask-programmable ROM organized as 2,097,152 × 8 bits (Byte mode) or 1,048,576 × 16 bits (Word mode) that can be selected by a $\overline{BYTE}$ input pin. It is fabricated using silicon-gate CMOS process technology.

PIN CONNECTIONS

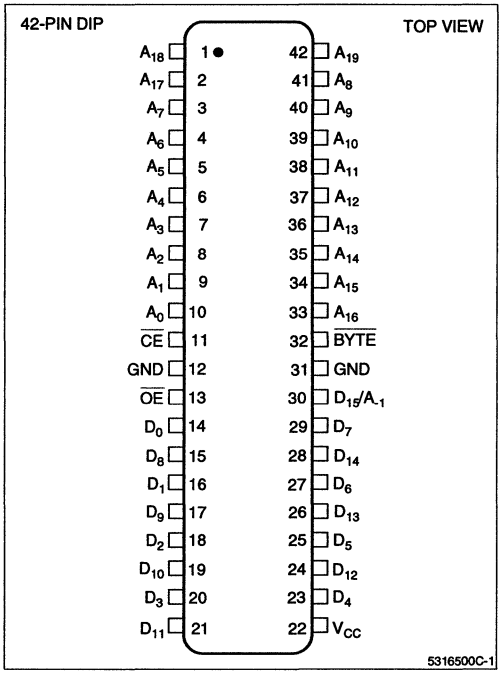


Figure 1. Pin Connections for DIP Package

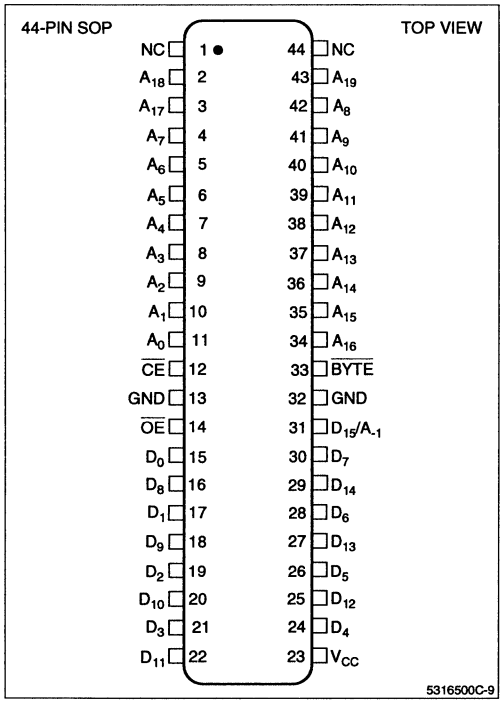


Figure 2. Pin Connections for SOP Package

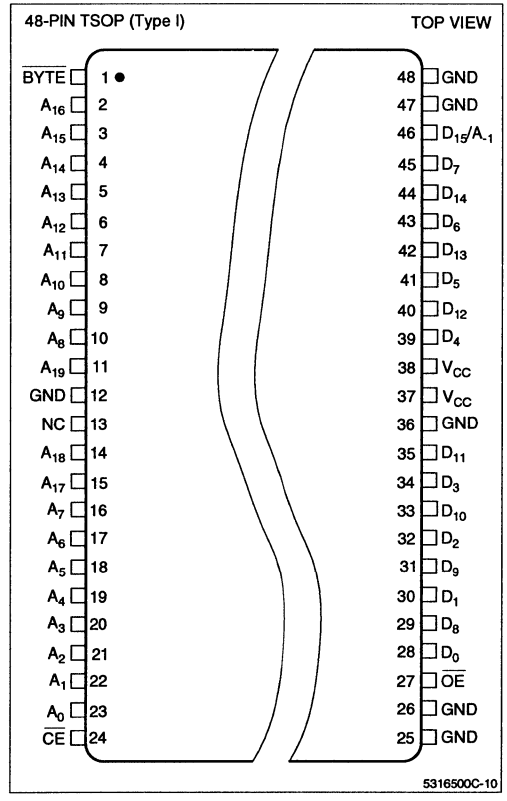


Figure 3. Pin Connections for TSOP Package

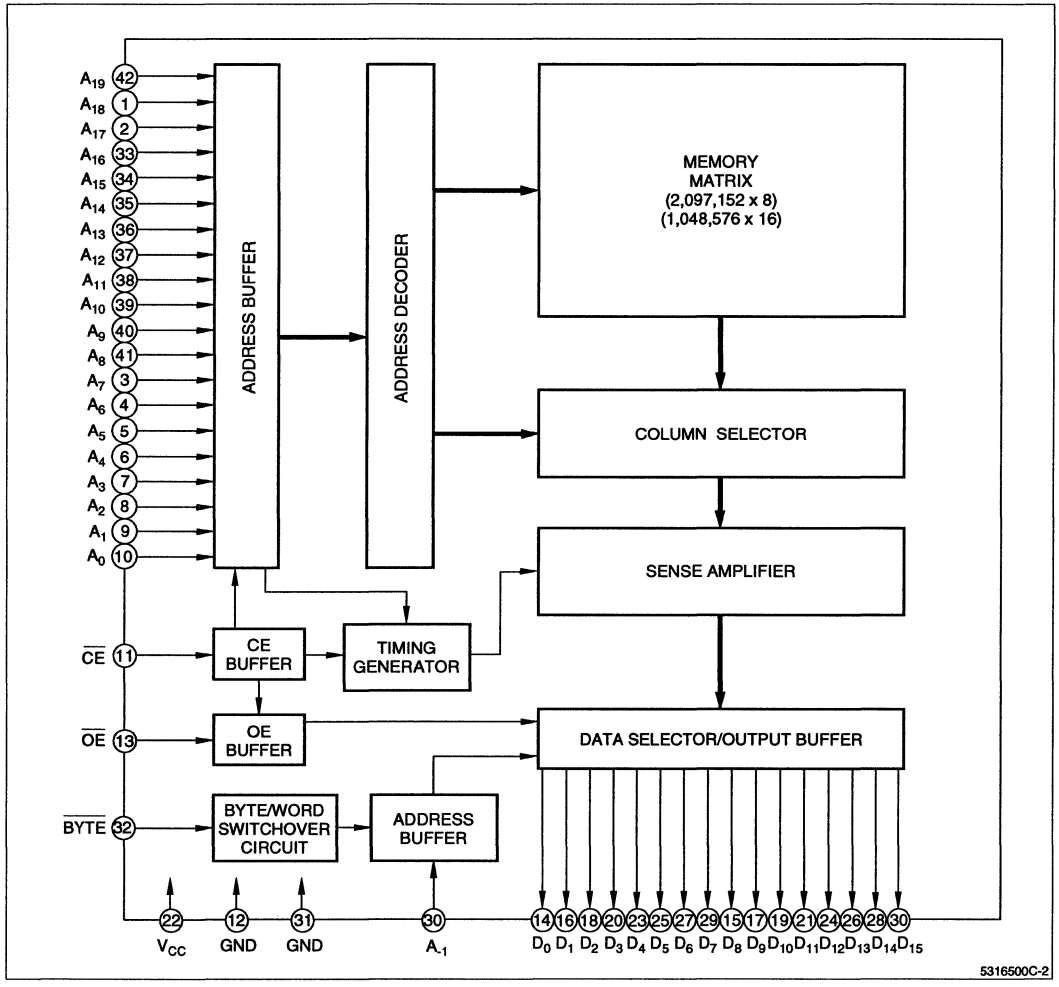


Figure 4. LH5316500C Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME
A_{-1} - A_{19}	Address input
D_0 - D_{15}	Data output
$\overline{BYTE}$	Byte/word switch
$\overline{CE}$	Chip Enable input

SIGNAL	PIN NAME
$\overline{OE}$	Output Enable input
V_{CC}	Power supply (+5 V)
GND	Ground

TRUTH TABLE

$\overline{CE}$	$\overline{OE}$	$\overline{BYTE}$	A-1 (D_{15})	DATA OUTPUT		ADDRESS INPUT		SUPPLY CURRENT
				D_0 - D_7	D_8 - D_{15}	LSB	MSB	
H	X	X	X	High-Z	High-Z	–	–	Standby (I_{SB})
L	H	X	X	High-Z	High-Z	–	–	Operating (I_{CC})
L	L	H	–	D_0 - D_7	D_8 - D_{15}	A_0	A_{19}	Operating (I_{CC})
L	L	L	L	D_0 - D_7	High-Z	A_{-1}	A_{19}	Operating (I_{CC})
L	L	L	H	D_8 - D_{15}	High-Z	A_{-1}	A_{19}	Operating (I_{CC})

NOTES:
X = H or L; High-Z = High-impedance

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Supply voltage	V_{CC}	-0.3 to +7.0	V
Input voltage	V_{IN}	-0.3 to V_{CC} + 0.3	V
Output voltage	V_{OUT}	-0.3 to V_{CC} + 0.3	V
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	4.5	5.0	5.5	V

DC CHARACTERISTICS (V_{CC} = 5 V ±10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	MAX.	UNIT	NOTE
Input 'High' voltage	V_{IH}		2.2	V_{CC} +0.3	V	
Input 'Low' voltage	V_{IL}		-0.3	0.8	V	
Output 'High' voltage	V_{OH}	I_{OH} = -400 µA	2.4		V	
Output 'Low' voltage	V_{OL}	I_{OL} = 2.0 mA		0.4	V	
Input leakage current	$\lvert I_{LI} \rvert$	V_{IN} = 0 V to V_{CC}		10	µA	
Output leakage current	$\lvert I_{LO} \rvert$	V_{OUT} = 0 V to V_{CC}		10	µA	1
Operating current	I_{CC1}	t_{RC} = 150 ns		50	mA	2
	I_{CC2}	t_{RC} = 1 µs		40		
Standby current	I_{SB1}	$\overline{CE}$ = V_{IH}		2	mA	
	I_{SB2}	$\overline{CE}$ = V_{CC} - 0.2 V		100	µA	
Input capacitance	C_{IN}	f = 1 MHz, t_A = 25°C		10	pF	
Output capacitance	C_{OUT}			10	pF	

NOTES:
1. $\overline{CE}$ = V_{IH}, $\overline{OE}$ = V_{IH}, outputs open
2. V_{IN} = V_{IH}/V_{IL}, $\overline{CE}$ = V_{IL}, outputs open

AC CHARACTERISTICS (V_{CC} = 5 V ±10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT	NOTE
Read cycle time	t_{RC}	150		ns	
Address access time	t_{AA}		150	ns	
Chip enable time	t_{ACE}		150	ns	
Output enable time	t_{OE}		70	ns	
Output hold time	t_{OH}	5		ns	
CE to output in High-Z	t_{CHZ}		60	ns	1
OE to output in High-Z	t_{OHZ}		60	ns	

NOTE:
1. This is the time required for the outputs to become high-impedance.

AC TEST CONDITIONS

PARAMETER	RATING
Input voltage amplitude	0.6 V to 2.4 V
Input rise/fall time	10 ns
Input reference level	1.5 V
Output reference level	0.8 V and 2.2 V
Output load condition	1TTL + 100 pF

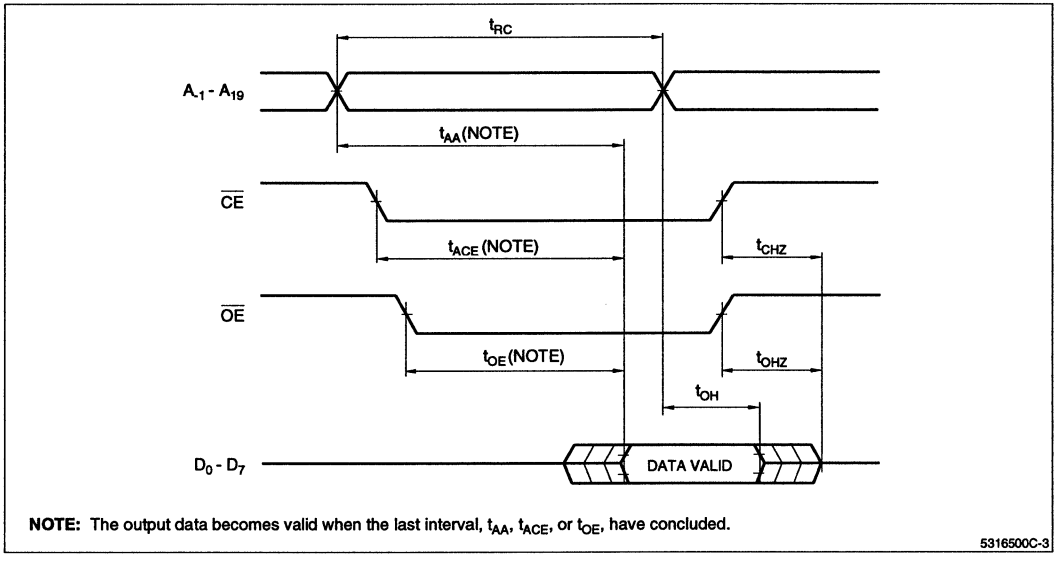
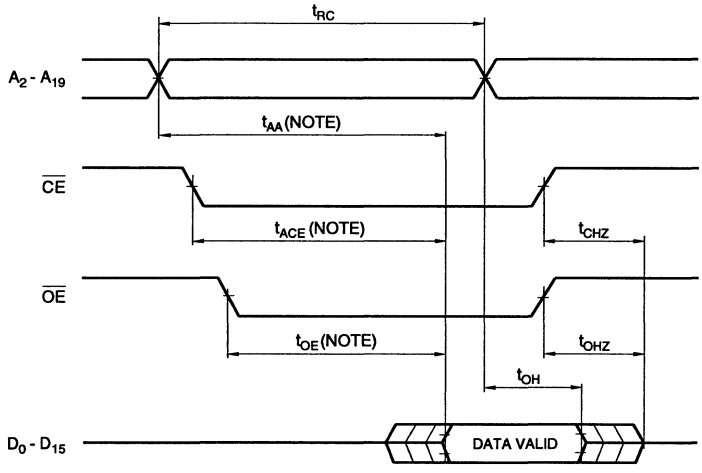


Figure 5. Byte Mode ($\overline{BYTE}$ = V_{IL})

CAUTION

To stabilize the power supply, it is recommended that a high-frequency bypass capacitor be connected between the V_{CC} pin and the GND pin.



NOTE: The output data becomes valid when the last interval, t_{AA}, t_{ACE}, or t_{OE}, have concluded.

5316500C-4

Figure 6. Word Mode ($\overline{BYTE}$ = V_{IH})

ORDERING INFORMATION

LH5316500C	X	- ##
Device Type	Package	Speed

- Speed: 15 150 Access Time (ns)
- Package:
  - D 42-pin, 600-mil DIP (DIP42-P-600)
  - N 44-pin, 600-mil SOP (SOP44-P-600)
  - T 48-pin, 12 x 18 mm² TSOP (Type I) (TSOP48-P-1218)
- Device Type: CMOS 16M (2M x 8 OR 1M x 16) Mask-Programmable ROM

Example: LH5316500CD-15 (CMOS 16M (2M x 8) Mask-Programmable ROM, 150 ns, 42-pin, 600-mil DIP)

5316500C-5

LH5316501

PRELIMINARY

CMOS 16M (2M × 8/1M × 16)
Mask-Programmable ROM

FEATURES

- 2,097,152 × 8 bit organization
  (Byte mode)
  1,048,576 × 16 bit organization
  (Word mode)
- Access time: 150 ns (MAX.)
  Page mode: 70 ns (MAX.)
- Addressable page: 4 words or 8 bytes
- Power consumption:
  Operating: 385 mW (MAX.)
  Standby: 550 µW (MAX.)
- Fully-static operation
- TTL compatible I/O
- Three-state outputs
- Single +5 V power supply
- Packages:
  42-pin, 600-mil DIP
  44-pin, 600-mil SOP

DESCRIPTION

The LH5316501 is a 16M-bit mask-programmable ROM organized as 2,097,152 × 8 bits (Byte mode) or 1,048,576 × 16 bits (Word mode) that can be selected by a $\overline{BYTE}$ input pin. It is fabricated using silicon-gate CMOS process technology.

PIN CONNECTIONS

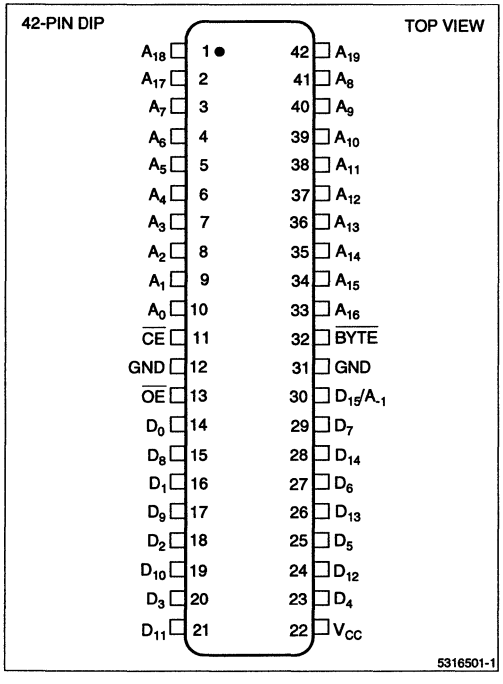


Figure 1. Pin Connections for DIP Package

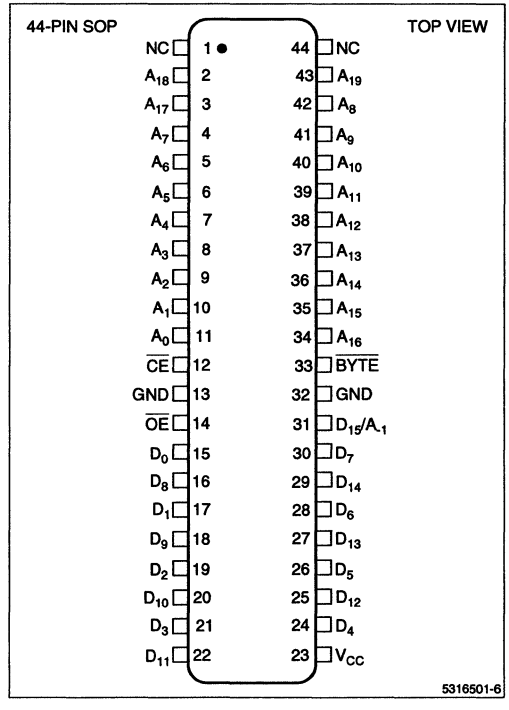


Figure 2. Pin Connections for SOP Package

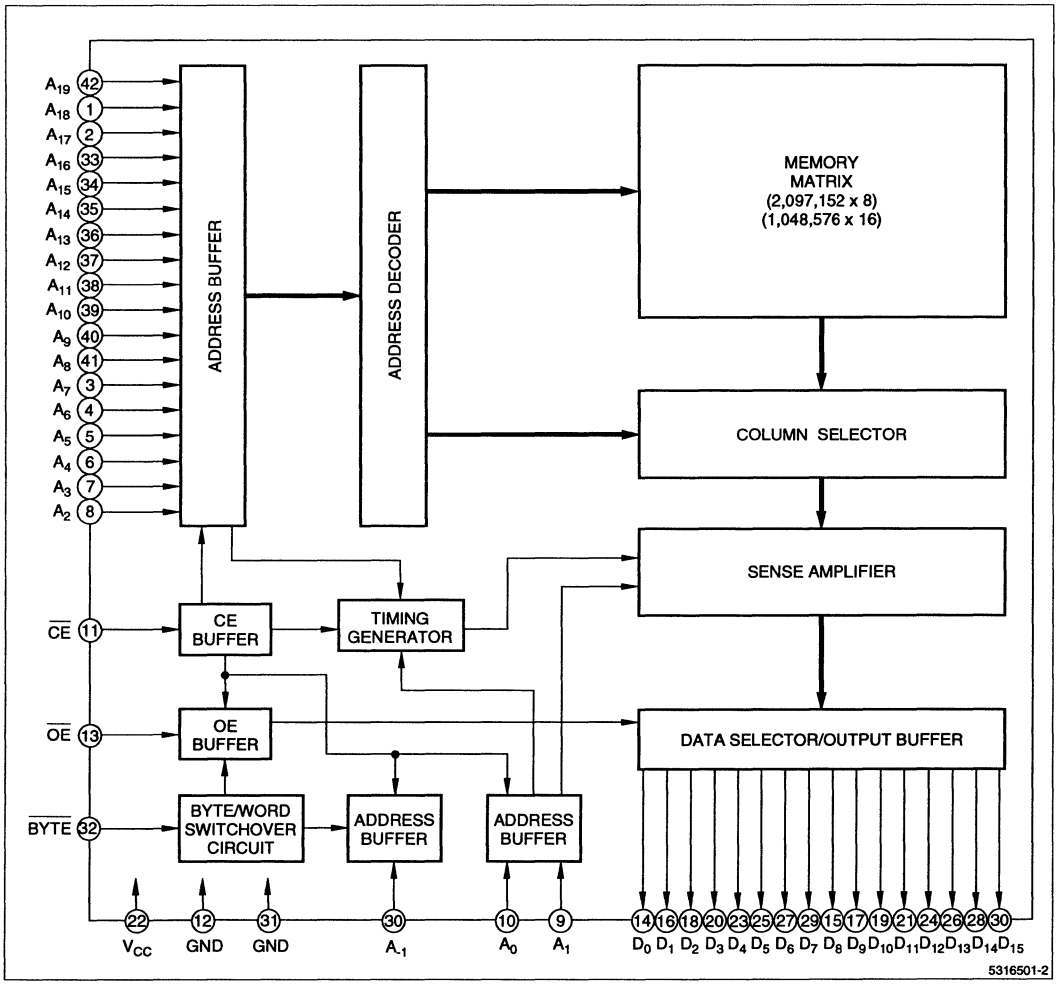


Figure 3. LH5316501 Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME
A_{-1} - A_1	Address input (page mode operation)
A_2 - A_{19}	Address input
D_0 - D_{15}	Data output
$\overline{BYTE}$	Byte/word switch

SIGNAL	PIN NAME
$\overline{CE}$	Chip Enable input
$\overline{OE}$	Output Enable input
V_{CC}	Power supply (+5 V)
GND	Ground

TRUTH TABLE

$\overline{CE}$	$\overline{OE}$	$\overline{BYTE}$	A-1 (D_{15})	DATA OUTPUT		ADDRESS INPUT		SUPPLY CURRENT
				D_0 - D_7	D_8 - D_{15}	LSB	MSB	
H	X	X	X	High-Z	High-Z	–	–	Standby (I_{SB})
L	H	X	X	High-Z	High-Z	–	–	Operating (I_{CC})
L	L	H	Inhibit	D_0 - D_7	D_8 - D_{15}	A_0	A_{19}	Operating (I_{CC})
L	L	L	L	D_0 - D_7	High-Z	A_{-1}	A_{19}	Operating (I_{CC})
L	L	L	L	D_8 - D_{15}	High-Z	A_{-1}	A_{19}	Operating (I_{CC})

NOTE:
X = H or L; High-Z = High-impedance

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Supply voltage	V_{CC}	-0.3 to +7.0	V
Input voltage	V_{IN}	-0.3 to V_{CC} + 0.3	V
Output voltage	V_{OUT}	-0.3 to V_{CC} + 0.3	V
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	4.5	5.0	5.5	V

DC CHARACTERISTICS (V_{CC} = 5 V ±10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	MAX.	UNIT	NOTE
Input 'High' voltage	V_{IH}		2.2	V_{CC} +0.3	V	
Input 'Low' voltage	V_{IL}		-0.3	0.8	V	
Output 'High' voltage	V_{OH}	I_{OH} = -400 µA	2.4		V	
Output 'Low' voltage	V_{OL}	I_{OL} = 2.0 mA		0.4	V	
Input leakage current	$\lvert I_{LI} \rvert$	V_{IN} = 0 V to V_{CC}		10	µA	
Output leakage current	$\lvert I_{LO} \rvert$	V_{OUT} = 0 V to V_{CC}		10	µA	1
Operating current	I_{CC1}	t_{RC} = 150 ns		70	mA	2
	I_{CC2}	t_{RC} = 1 µs		50		
Standby current	I_{SB1}	$\overline{CE}$ = V_{IH}		2	mA	
	I_{SB2}	$\overline{CE}$ = V_{CC} - 0.2 V		100	µA	
Input capacitance	C_{IN}	f = 1 MHz, t_A = 25°C		10	pF	
Output capacitance	C_{OUT}			10	pF	

NOTES:
1. $\overline{CE}$ = V_{IH}, $\overline{OE}$ = V_{IH}, outputs open
2. V_{IN} = V_{IH}/V_{IL}, $\overline{CE}$ = V_{IL}, outputs open

AC CHARACTERISTICS (V_{CC} = 5 V ±10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT	NOTE
Read cycle time	t_{RC}	150		ns	
Address access time	t_{AA}		150	ns	
Chip enable time	t_{ACE}		150	ns	
Page address access time	t_{APA}		70	ns	
Output enable time	t_{OE}		70	ns	
Output hold time	t_{OH}	5		ns	
CE to output in High-Z	t_{CHZ}		60	ns	1
OE to output in High-Z	t_{OHZ}		60	ns	

NOTE:
1. Determined by the time for the output to be opened, irrespective of output voltage.

AC TEST CONDITIONS

PARAMETER	RATING
Input voltage amplitude	0.6 V to 2.4 V
Input rise/fall time	10 ns
Input reference level	1.5 V
Output reference level	0.8 V and 2.2 V
Output load condition	1TTL + 100 pF

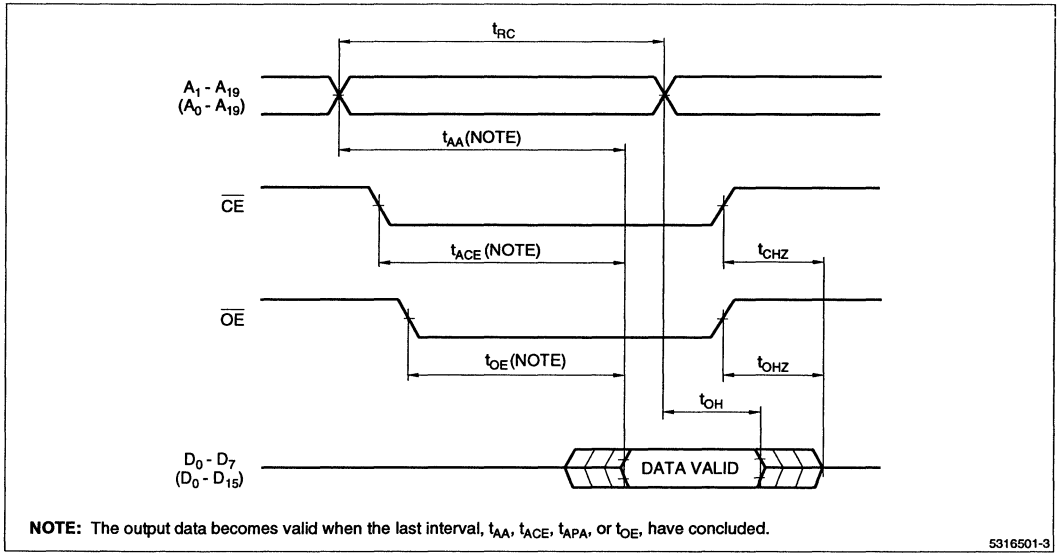


Figure 4. Read Cycle

CAUTION

To stabilize the power supply, it is recommended that a high-frequency bypass capacitor be connected between the V_{CC} pin and the GND pin.

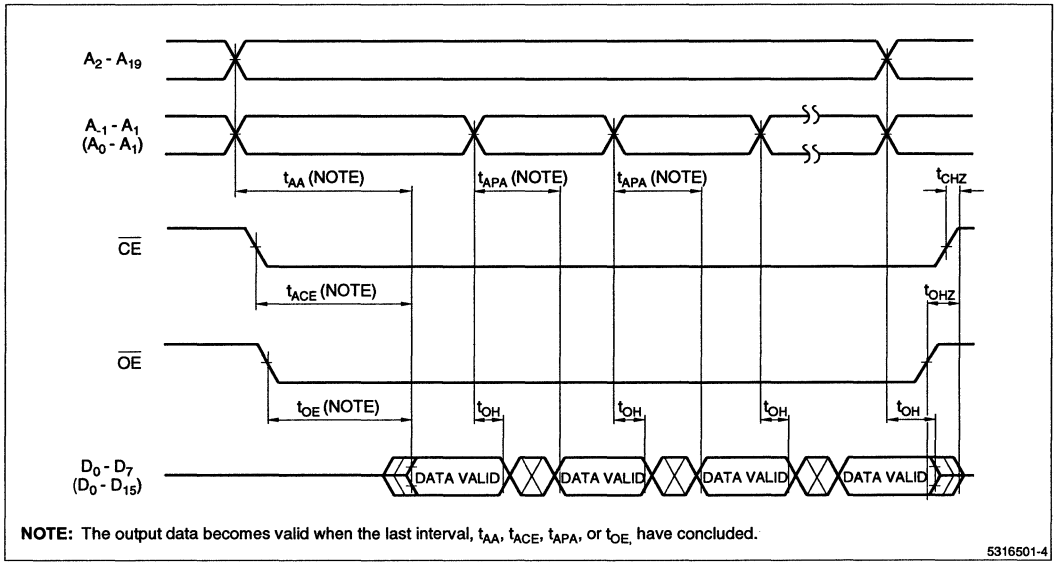
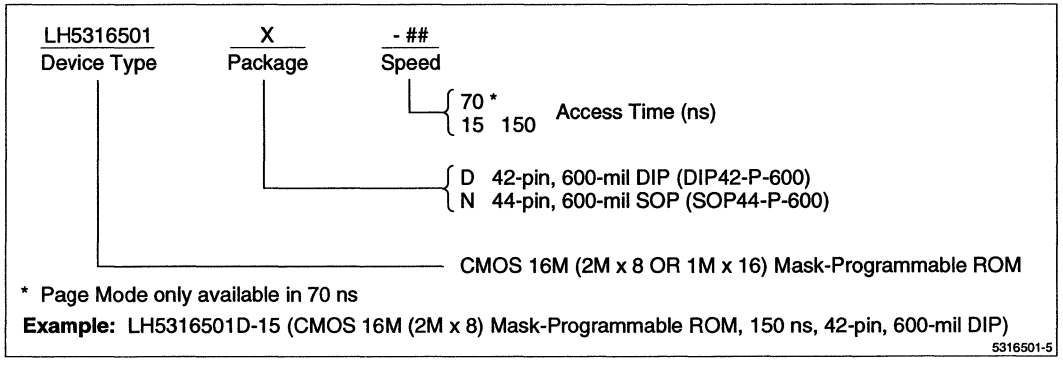


Figure 5. Page Mode Read Cycle

ORDERING INFORMATION



PRELIMINARY

LH5332500

CMOS 32M (4M × 8/2M × 16)
Mask-Programmable ROM

FEATURES

- 4,194,304 × 8 bit organization
  (Byte mode)
  2,097,152 × 16 bit organization
  (Word mode)
- $\overline{\text{BYTE}}$ input pin selects bit configuration
- Access time: 150 ns (MAX.)
- Power consumption:
  Operating: 275 mW (MAX.)
  Standby: 550 µW (MAX.)
- Fully-static operation
- TTL compatible I/O
- Three-state outputs
- Single +5 V power supply
- Packages:
  44-pin, 600-mil SOP
  64-pin, 14 × 20 mm^2 QFP
- ×16 word-wide pinout

DESCRIPTION

The LH5332500 is a mask-programmable ROM organized as 4,194,304 × 8 bits (Byte mode) or 2,097,152 × 16 bits (Word mode) that can be selected by input pin. It is fabricated using silicon-gate CMOS process technology.

PIN CONNECTIONS

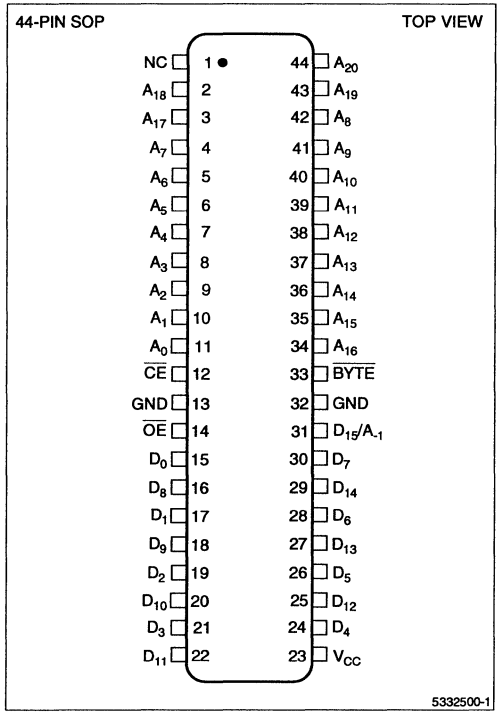


Figure 1. Pin Connections for SOP Package

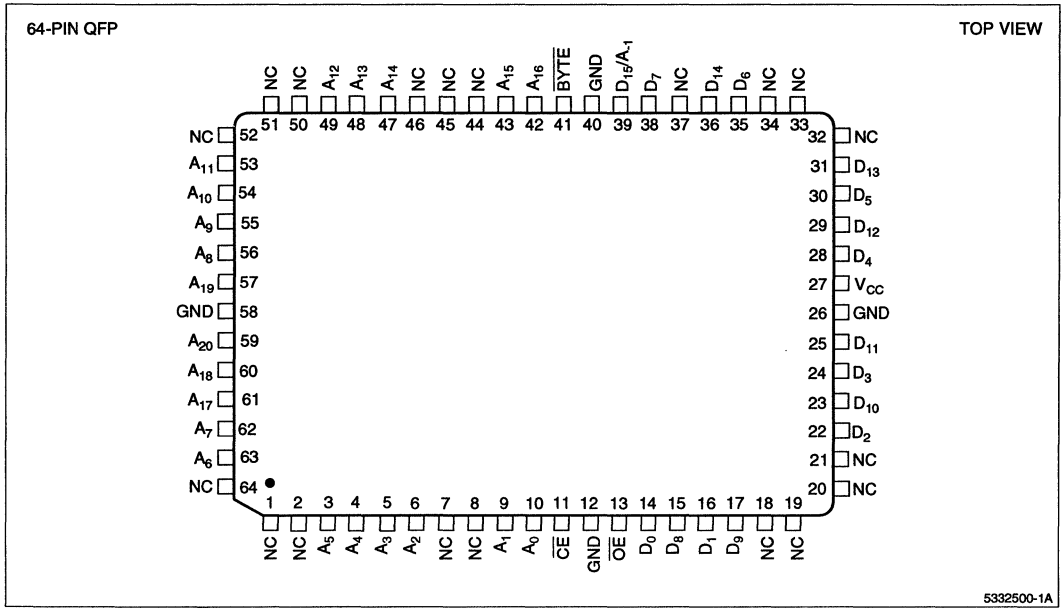


Figure 2. Pin Connections for QFP Package

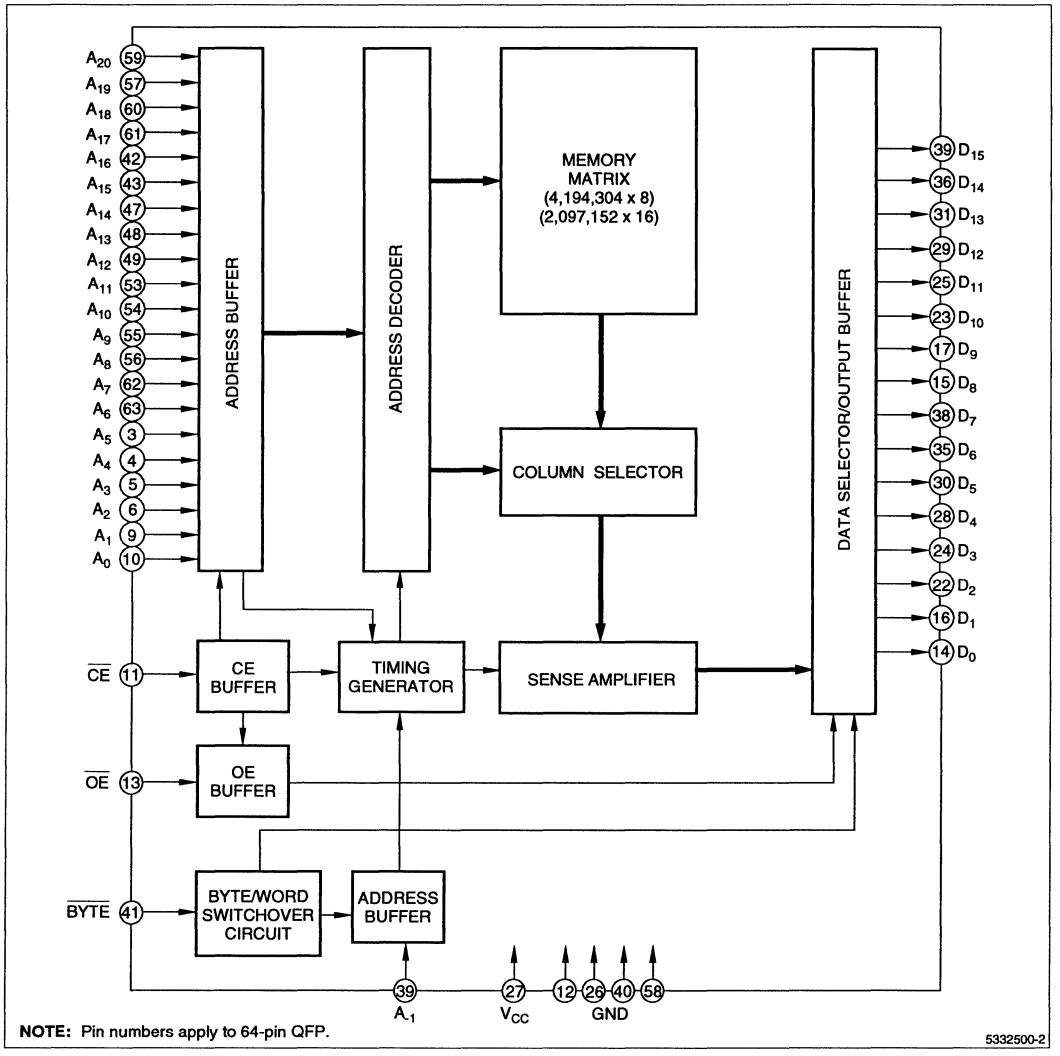


Figure 3. LH5332500 Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME	NOTE
A_{-1}	Address input (Byte mode)	1
A_0 - A_{20}	Address input	
D_0 - D_{15}	Data output	
$\overline{CE}$	Chip Enable input	

SIGNAL	PIN NAME	NOTE
$\overline{OE}$	Output Enable input	
$\overline{BYTE}$	Byte/word switch	
V_{CC}	Power supply (+5 V)	
GND	Ground	

NOTE:

1. D_{15}/A_{-1} pin becomes LSB address input (A_{-1}) when the bit configuration is set to byte mode, and data output (D_{15}) when in word mode. $\overline{BYTE}$ input pin selects bit configuration.

TRUTH TABLE

$\overline{CE}$	$\overline{OE}$	$\overline{BYTE}$ *	A_{-1}	MODE	D_0 - D_7	D_8 - D_{15}	SUPPLY CURRENT	NOTE
H	X	X	X	Non selected	High-Z		Standby (I_{SB})	1
L	H	X	X	Non selected	High-Z		Operating (I_{CC})	
L	L	H	Input inhibit	Word	D_0 - D_7	D_8 - D_{15}		
L	L	L	L	Byte	D_0 - D_7	High-Z		
L	L	L	H	Byte	D_8 - D_{15}	High-Z		

NOTE:
1. X = H or L
   * $\overline{BYTE}$ input state must be set to H or L which must not be changed during operation.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Supply voltage	V_{CC}	-0.3 to +7.0	V	1
Input voltage	V_{IN}	-0.3 to V_{CC} +0.3	V	
Output voltage	V_{OUT}	-0.3 to V_{CC} +0.3	V	
Operating temperature	Topr	0 to +70	°C	
Storage temperature	Tstg	-55 to +150	°C	

NOTE:
1. The maximum applicable voltage on any pin with respect to GND.

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	4.5	5.0	5.5	V

DC CHARACTERISTICS (V_{CC} = 5 V ±10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	MAX.	UNIT	NOTE
Input 'Low' voltage	V_{IL}		-0.3	0.8	V	
Input 'High' voltage	V_{IH}		2.2	V_{CC} +0.3	V	
Output 'Low' voltage	V_{OL}	I_{OL} = 2.0 mA		0.4	V	
Output 'High' voltage	V_{OH}	I_{OH} = -400 µA	2.4		V	
Input leakage current	$\lvert I_{LI} \rvert$	V_{IN} = 0 V or V_{CC}		10	µA	
Output leakage current	$\lvert I_{LO} \rvert$	V_{OUT} = 0 V or V_{CC}		10	µA	1
Operating current	I_{CC1}	t_{RC} = 200 ns		50	mA	2
	I_{CC2}	t_{RC} = 1 µs		40		
Standby current	I_{SB1}	$\overline{CE}$ = V_{IH}		2	mA	
	I_{SB2}	$\overline{CE}$ = V_{CC} - 0.2 V		100	µA	

NOTES:
1. $\overline{CE}/\overline{OE}$ = V_{IH}
2. V_{IN} = V_{IH}/V_{IL}, $\overline{CE}$ = V_{IL}, outputs open

AC CHARACTERISTICS (V_{CC} = 5 V ±10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT	NOTE
Read cycle time	t_{RC}	150		ns	
Address access time	t_{AA}		150	ns	
Chip enable time	t_{ACE}		150	ns	
Output enable time	t_{OE}		70	ns	
Output hold time	t_{OH}	5		ns	
CE to output in High-Z	t_{CHZ}		70	ns	1
OE to output in High-Z	t_{OHZ}		70	ns	

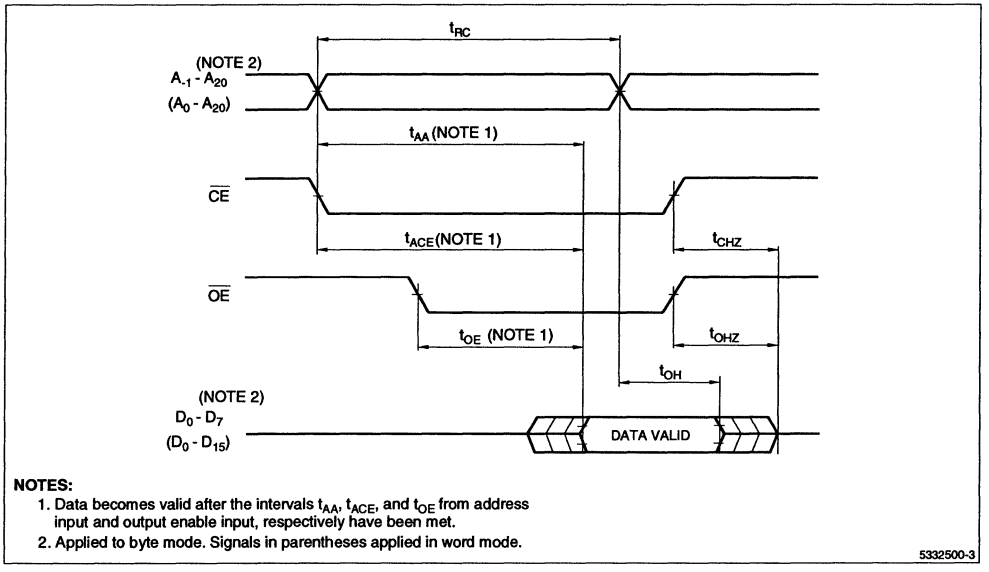
NOTE:
1. This is the time required for the outputs to become high-impedance.

AC TEST CONDITIONS

PARAMETER	RATING
Input voltage amplitude	0.6 V to 2.4 V
Input rise/fall time	10 ns
Input reference level	1.5 V
Output reference level	0.8 V and 2.2 V
Output load condition	1TTL +100 pF

CAPACITANCE (V_{CC} = 5 V ±10%, f = 1 MHz, T_A = 25°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Input capacitance	C_{IN}			10	pF
Output capacitance	C_{OUT}			10	pF



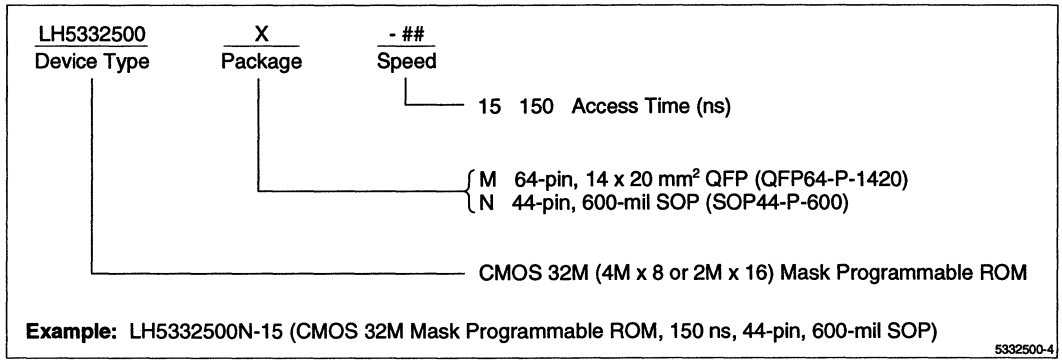
NOTES:
1. Data becomes valid after the intervals t_{AA}, t_{ACE}, and t_{OE} from address input and output enable input, respectively have been met.
2. Applied to byte mode. Signals in parentheses applied in word mode.

Figure 4. Timing Diagram

CAUTION

To stabilize the power supply, it is recommended that a high-frequency bypass capacitor be connected between the V_{CC} pin and the GND pin.

ORDERING INFORMATION

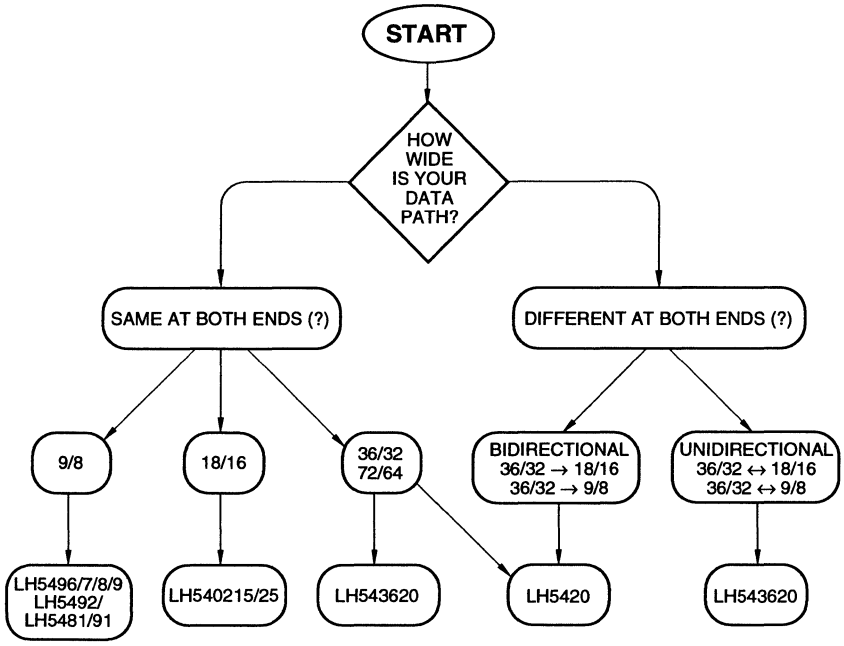


Example: LH5332500N-15 (CMOS 32M Mask Programmable ROM, 150 ns, 44-pin, 600-mil SOP)

5332500-4

FIFO MEMORIES

CHOOSING A SHARP FIFO



LH5481
LH5491

Cascadable 64 × 8 FIFO
Cascadable 64 × 9 FIFO

FEATURES

- Fastest 64 × 8/9 Cascadable FIFO 35/25/15 MHz
- Expandable in Word Width and FIFO Depth
- Almost-Full/Almost-Empty and Half-Full Flags
- Fully Independent Asynchronous Inputs and Outputs
- LH5481 Output Enable forces Data Outputs to High-Impedance State
- Pin-Compatible Replacements for Cypress CY7C408A/09A or Logic Devices L8C408/09 FIFOs
- Industry Standard Pinout
- Packages:
  28-Pin, 300-mil DIP
  28-Pin PLCC

FUNCTIONAL DESCRIPTION

The LH5481 and LH5491 are high-performance, asynchronous First-In, First-Out (FIFO) memories organized 64 words deep by eight or nine bits wide. The eight-bit LH5481 has an Output Enable ($\overline{OE}$) function, which can be used to force the eight data outputs (DO) to a high-impedance state. The LH5491 has nine data outputs.

These FIFOs accept eight or nine-bit data at the Data Inputs (DI). A Shift In (SI) signal writes the DI data into the FIFO. A Shift Out (SO) signal shifts stored data to the Data Outputs (DO). The Output Ready (OR) signal indicates when valid data is present on the DO outputs.

If the FIFO is full and unable to accept more DI data, Input Ready (IR) will not return HIGH, and SI pulses will be ignored. If the FIFO is empty and unable to shift data to the DO outputs, OR will not return HIGH, and SO pulses will be ignored. The Almost-Full/Almost-Empty (AFE) flag is asserted (HIGH) when the FIFO is almost-full (56 words or more) or almost- empty (eight words or less). The Half-Full (HF) flag is asserted (HIGH) when the FIFO contains 32 words or more.

Reading and writing operations may be asynchronous, allowing these FIFOs to be used as buffers between digital machines of different operating frequencies. The high speed makes these FIFOs ideal for high performance communication and controller applications.

PIN CONNECTIONS

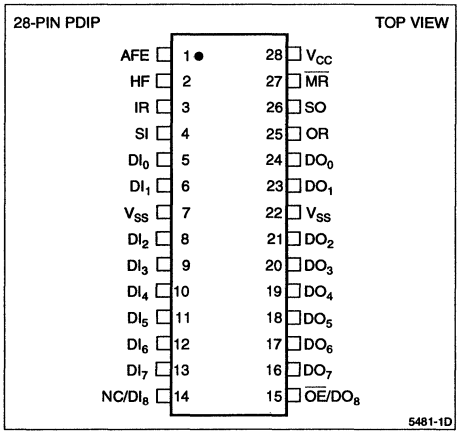


Figure 1. Pin Connections for DIP Package

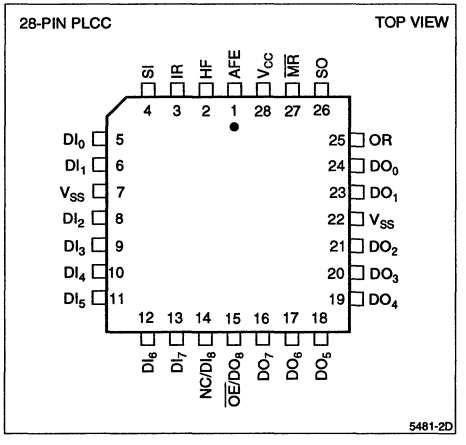


Figure 2. Pin Connections for PLCC Package

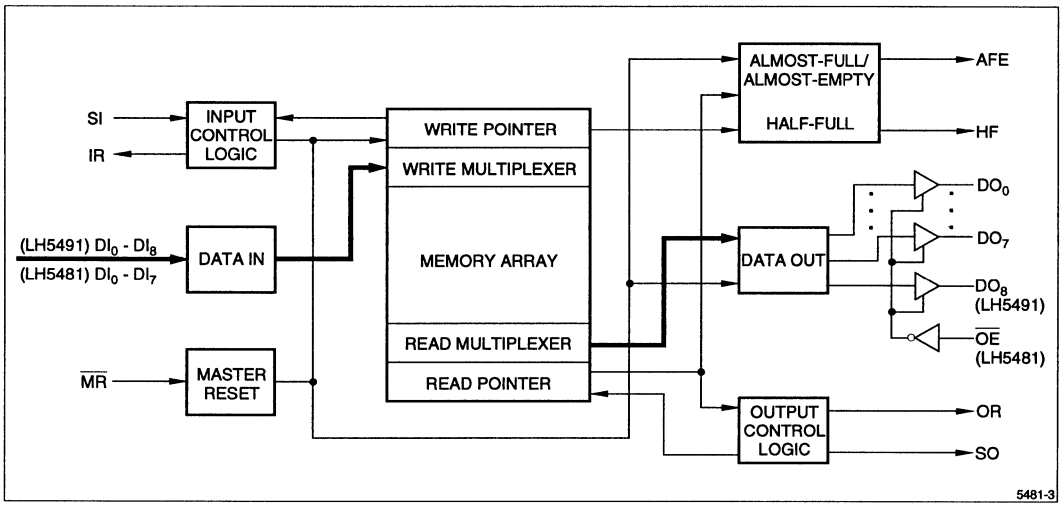


Figure 3. LH5481/91 Block Diagram

PIN DESCRIPTIONS

PIN	PIN TYPE *	DESCRIPTION
$DI_0 - DI_7$	I	Data Inputs, LH5481
$DO_0 - DO_7$	O/Z	Data Outputs, LH5481
$DI_0 - DI_8$	I	Data Inputs, LH5491
$DO_0 - DO_8$	O	Data Outputs, LH5491
SI	I	Shift In
SO	I	Shift Out
IR	O	Input Ready
OR	O	Output Ready

* I=Input, O=Output, Z=High-Impedance, V=Power Voltage Level

PIN	PIN TYPE *	DESCRIPTION
HF	O	Half-Full Flag
AFE	O	Almost-Full / Almost-Empty
$\overline{MR}$	I	Master Reset
$\overline{OE}$	I	Output Enable (LH5481 only)
V_{CC}	V	Positive Power Supply
V_{SS}	V	Ground

ABSOLUTE MAXIMUM RATINGS [1,2]

PARAMETER	RATING
Vcc Range	−0.5 V to 7 V
Input Voltage Range	−0.5 V to Vcc + 0.5 V (not to exceed 7 V)
DC Output Current [3]	± 40 mA
Storage Temperature	−65°C to 150°C
DC Voltage Applied To Outputs In High-Z state	−0.5 V to Vcc + 0.5 V (not to exceed 7 V)
Static Discharge Voltage [4]	> 2000 V
Power Dissipation (Package Limit)	1.0 W

NOTES:

1. All voltages are measured with respect to Vss.
2. Stresses greater than those listed under 'Absolute Maximum Ratings' may cause permanent damage to the device. This is a stress rating for transient conditions only. Functional operation of the device at these or any other conditions above those indicated in the 'Operating Range' of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
3. Outputs should not be shorted for more than 30 seconds. No more than one output should be shorted at any time.
4. Sample tested only.

OPERATING RANGE [1]

PARAMETER	DESCRIPTION	MIN	MAX	UNIT
T_A	Temperature, Ambient	0.0	70	°C
V_{CC}	Supply Voltage	4.5	5.5	V
Vss	Ground	0.0	0.0	V
V_{IL}	Input Low Voltage (Logic '0') [2]	−0.5	0.8	V
V_{IH}	Input High Voltage (Logic '1')	2.0	Vcc + 0.5	V

NOTES:

1. All voltages are measured with respect to Vss.
2. FIFO inputs are able to withstand a −1.5 V undershoot for less than 10 ns per cycle.

DC ELECTRICAL CHARACTERISTICS [1] (Over Operating Range Unless Otherwise Noted)

PARAMETER	DESCRIPTION	TEST CONDITIONS	MIN	MAX	UNIT
I_{LI}	Input Leakage Current	V_{CC} = 5.5 V, V_{IN} = 0 V to V_{CC}	−10	10	µA
I_{LO}	Output Leakage Current (High-Z)	V_{CC} = 5.5 V, V_{OUT} = 0 V to V_{CC}	−10	10	µA
V_{OH}	Output High Voltage	V_{CC} = 4.5 V, I_{OH} = −4 mA	2.4		V
V_{OL}	Output Low Voltage	V_{CC} = 4.5 V, I_{OL} = 8.0 mA		0.4	V
I_{CCQ}	Power Supply Quiescent Current	V_{CC} = 5.5 V, I_{OUT} = 0 mA $V_{IN} \leq V_{IL}$, $V_{IN} \geq V_{IH}$		25	mA
I_{CC}	Power Supply Current [2]	fsi = 35 MHz, fso = 35 MHz		45	mA

NOTES:

1. All voltages are measured with respect to Vss.
2. Icc is dependent upon actual output loading and cycle rates. Specified values are with outputs open.

AC TEST CONDITIONS [1]

PARAMETER	RATING
Input Pulse Levels	0 to 3 V
Input Rise and Fall Times (10% / 90%)	Figure 4a
Input Timing Reference Levels	1.5 V
Output Timing Reference Levels	1.5 V
Output Load for AC Timing Tests	Figure 4b

NOTE:
1. All voltages are measured with respect to Vss.

CAPACITANCE [1,2]

PARAMETER	DESCRIPTION	TEST CONDITIONS	RATING
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 4.5 V	5 pF
C_{OUT}	Output Capacitance	T_A = 25°C, f = 1 MHz, Vcc = 4.5 V	7 pF

NOTES:
1. All voltages are measured with respect to Vss.
2. Sample tested only.

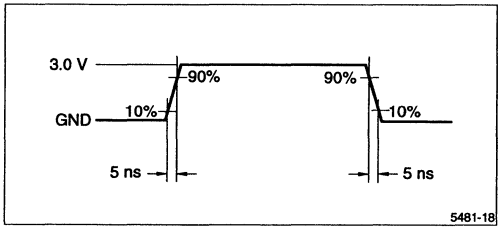


Figure 4a. Input Rise and Fall Times

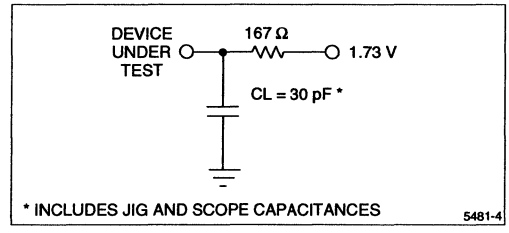


Figure 4b. Output Load Circuit

AC ELECTRICAL CHARACTERISTICS [1] (Over Operating Range)

SYMBOL	PARAMETER	15MHz		25MHz		35MHz		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	
f_O	Operating Frequency [2]		15		25		35	MHz
t_{PHSI}	SI HIGH Time [3,8]	15		11		9		ns
t_{PLSI}	SI LOW Time [3,8]	20		18		17		ns
t_{SSI}	Data Setup to SI [4]	–1		–1		–1		ns
t_{HSI}	Data Hold from SI [4]	14		12		10		ns
t_{DLIR}	Delay, SI HIGH to IR LOW		20		18		16	ns
t_{DHIR}	Delay, SI LOW to IR HIGH		24		20		18	ns
t_{PHSO}	SO HIGH Time [3]	15		11		9		ns
t_{PLSO}	SO LOW Time [3]	20		18		17		ns
t_{DLOR}	Delay, SO HIGH to OR LOW		20		18		16	ns
t_{DHOR}	Delay, SO LOW to OR HIGH		24		20		18	ns
t_{SOR}	Data Setup to OR HIGH	–1		–1		–1		ns
t_{HSO}	Data Hold from SO LOW	0		0		0		ns
t_{FT}	Fallthrough Time		36		34		30	ns
t_{BT}	Bubblethrough Time		28		26		25	ns
t_{SIR}	Data Setup to IR [5]	5		5		5		ns
t_{HIR}	Data Hold from IR [5]	5		5		5		ns
t_{PIR}	Input Ready Pulse HIGH [8]	7		7		7		ns
t_{POR}	Output Ready Pulse HIGH [8]	7		7		7		ns
t_{DLZOE}	OE LOW to LOW Z (LH5481) [6,9]		35		30		25	ns
t_{DHZOE}	OE HIGH to HIGH Z (LH5481) [6,9]		35		30		25	ns
t_{DHHF}	SI LOW to HF HIGH		40		40		36	ns
t_{DLHF}	SO LOW to HF LOW		40		40		36	ns
t_{DLAFE}	SO or SI LOW to AFE LOW		40		40		36	ns
t_{DHAFE}	SO or SI LOW to AFE HIGH		40		40		36	ns
t_{PMR}	$\overline{MR}$ Pulse Width	35		35		35		ns
t_{DSI}	$\overline{MR}$ HIGH to SI HIGH		25		25		22	ns
t_{DOR}	$\overline{MR}$ LOW to OR LOW [7]		25		25		20	ns
t_{DIR}	$\overline{MR}$ LOW to IR HIGH [7]		25		25		20	ns
t_{LXMR}	$\overline{MR}$ LOW to Output LOW [7]		25		25		20	ns
t_{AFE}	$\overline{MR}$ LOW to AFE HIGH		30		30		30	ns
t_{HF}	$\overline{MR}$ LOW to HF LOW		30		30		30	ns
t_{OD}	SO LOW to Next Data Out Valid		26		22		20	ns

NOTES:

1. All time measurements performed at 'AC Test Conditions.'
2. $f_O = f_{SI} = f_{SO}$.
3. $t_{PHSI} + t_{PLSI} = t_{PHSO} + t_{PLSO} = 1/f_O$.
4. t_{SSI} and t_{HSI} apply when memory is not full.
5. t_{SIR} and t_{HIR} apply when memory is full and SI is HIGH.
6. High-Z transitions are referenced to the steady-state V_{OH} – 500 mV and V_{OL} + 500 mV levels on the output.
7. After reset goes LOW, all Data outputs will be at LOW level, IR goes HIGH and OR goes LOW.
8. Common dash number devices are guaranteed by design to function properly in a cascaded configuration.
9. Sample tested only.

OPERATIONAL DESCRIPTION

Unlike earlier versions of FIFOs, the LH5481 and LH5491 use dual-port Random-Access-Memory, write and read pointers, and special control logic. The write pointer is incremented by the falling edge of the Shift In (SI) signal, while the read pointer is incremented by the falling edge of the Shift Out (SO) signal. The Input Ready (IR) signal enables data writing to the FIFO. The Output Ready (OR) signal indicates valid read information is available on the Data Output (DO) pins.

Resetting The FIFO

The FIFO must be reset, upon power-up, using the Master Reset ($\overline{MR}$) signal. This causes the FIFO to enter an empty state, indicated by the Output Ready (OR) being LOW and Input Ready (IR) being HIGH. All Data Output (DO) pins will be LOW in this state. The AFE flag will be HIGH, and the HF flag will be LOW.

If Shift In (SI) is HIGH, when the Master Reset ($\overline{MR}$) signal is ended, then the data on the Data Input (DI) pins will be written into the FIFO, and Input Ready (IR) will return LOW until Shift In (SI) is brought LOW.

If Shift In (SI) is LOW when the Master Reset ($\overline{MR}$) is deasserted, then Input Ready (IR) goes HIGH, but the data on the Data Input (DI) pins does not enter the FIFO until Shift In (SI) goes HIGH.

Shifting Data In

Data Input (DI) is shifted into the FIFO on the rising edge of Shift In (SI). This loads input data into the FIFO, and causes Input Ready (IR) to go LOW. When a falling edge of Shift In (SI) occurs,the write pointer increments to the next word position, and Input Ready (IR) goes HIGH, indicating that the FIFO is ready to accept new data. When the FIFO is full, Input Ready (IR) remains LOW after the negative edge of Shift In (SI) signal; Shift Out (SO) action is required to unload a word of data and bring Input Ready (IR) HIGH. (See 'Bubblethrough Condition' description.)

Shifting Data Out

Data is shifted out of the FIFO on the falling edge of Shift Out (SO). The read pointer increments to the next word location; FIFO data, if present, appears on the Data Output (DO) pins; and the Output Ready (OR) signal goes HIGH. If FIFO data is not present, Output Ready (OR) stays LOW, indicating that the FIFO is empty; in this case, the last valid data read from the FIFO remains on the Data Output (DO) pins. When the FIFO is not empty, Output Ready (OR) goes LOW after the rising edge of Shift Out (SO). The previous data remains on the Data Output (DO) pins until a falling edge of Shift Out (SO).

Fallthrough Condition

When the FIFO is empty, a data word entering through the Shift In (SI) action follows one of two sequences.

If Shift Out (SO) is LOW, the data propagates to the Data Output (DO) pins; and Output Ready (OR) goes HIGH and stays HIGH until the next rising edge of Shift Out (SO).

If Shift Out (SO) is held HIGH while data is shifted into an empty FIFO as occurs in depth cascading of FIFOs, data propagates to the Data Output (DO) pins, and Output Ready (OR) pulses HIGH for a minimum time duration specified by t_{POR} and then goes back LOW again. The stored word remains on the Data Output (DO) pins. If more words are written into the FIFO, they line up behind the first word, and do not appear on the Data Output (DO) pins until Shift Out (SO) has returned LOW.

Bubblethrough Condition

When the FIFO is full, Shift Out (SO) action initiates one of the following two sequences:

If Shift In (SI) is LOW, Input Ready (IR) goes HIGH and stays HIGH until the next rising edge of Shift In (SI).

If Shift In (SI) is held HIGH while data is shifted out of a full FIFO, as occurs in depth cascading of FIFOs, Input Ready (IR) pulses HIGH for a minimum time duration specified by t_{PIR}, and then goes back LOW again. Special Data Input (DI) setup and hold times (t_{SIR} and t_{HIR}, respectively) are defined for this condition.

TIMING DIAGRAMS

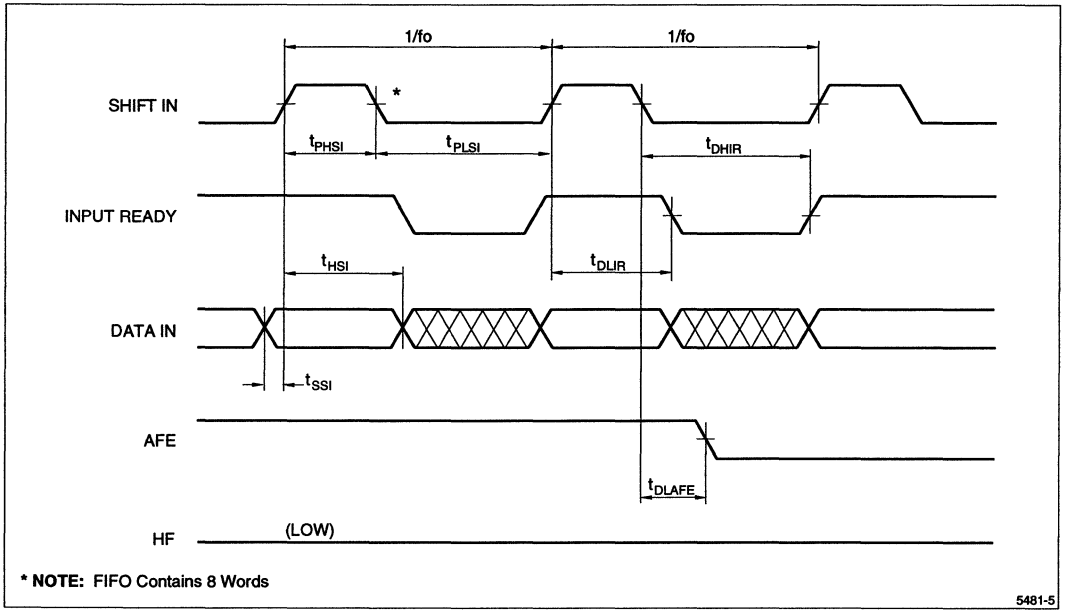


Figure 5. Data In Timing

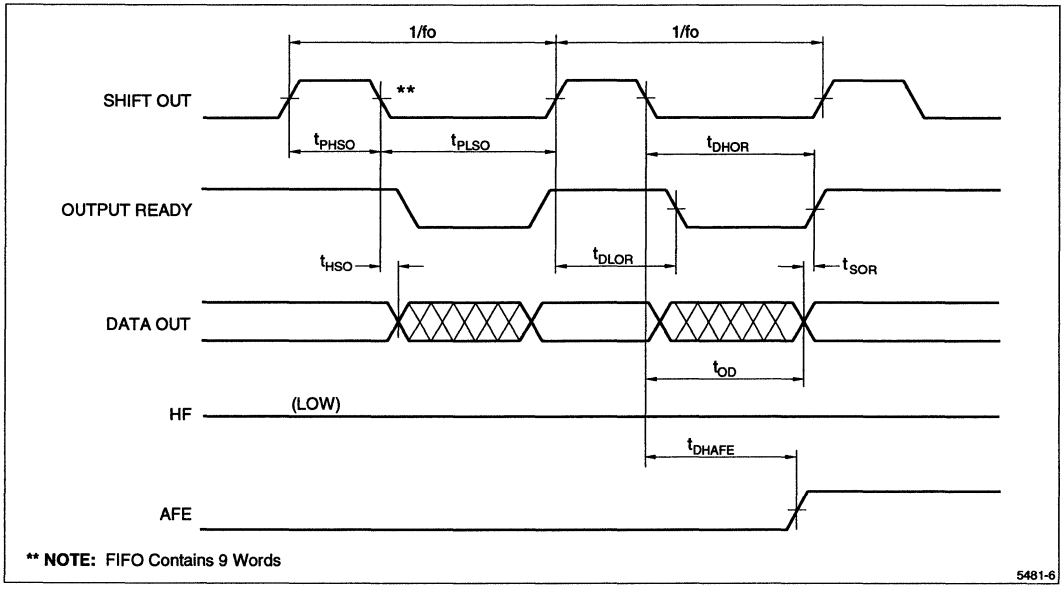


Figure 6. Data Out Timing

TIMING DIAGRAMS (cont'd)

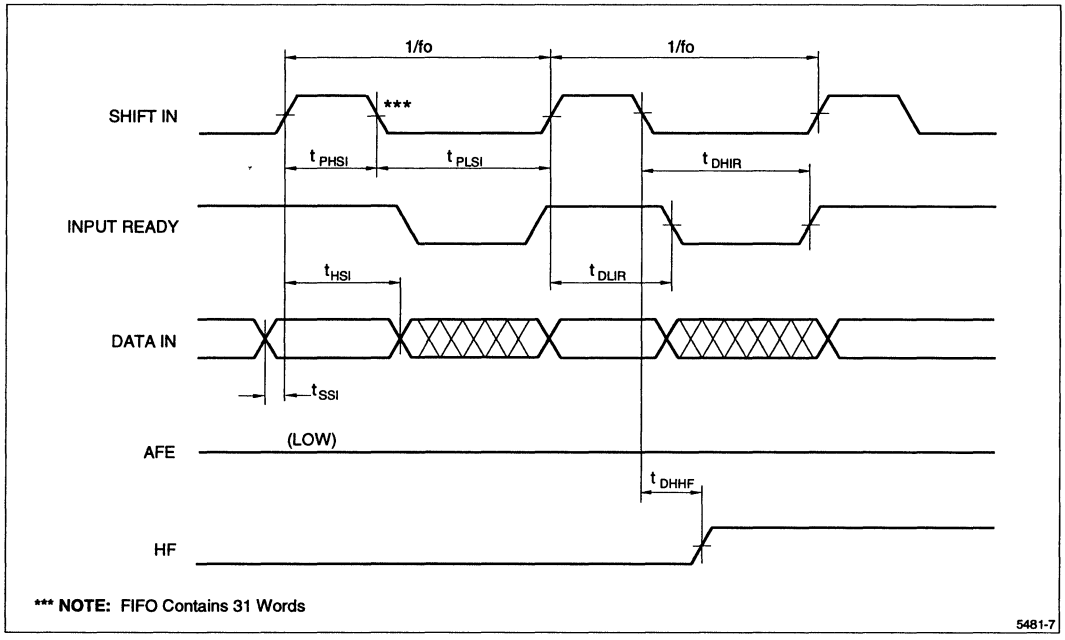


Figure 7. Data In Timing

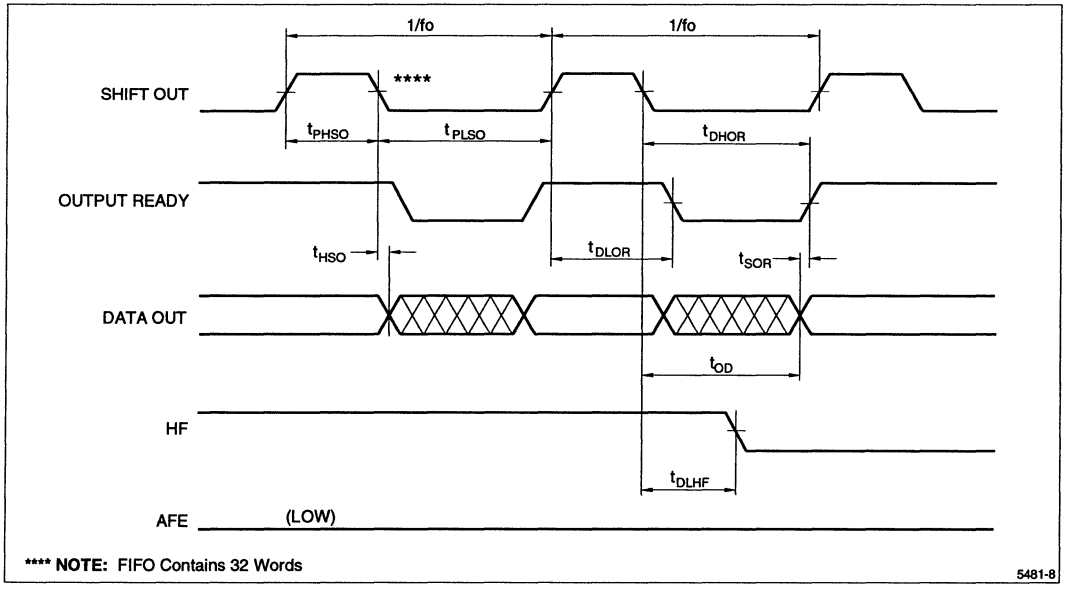


Figure 8. Data Out Timing

TIMING DIAGRAMS (cont'd)

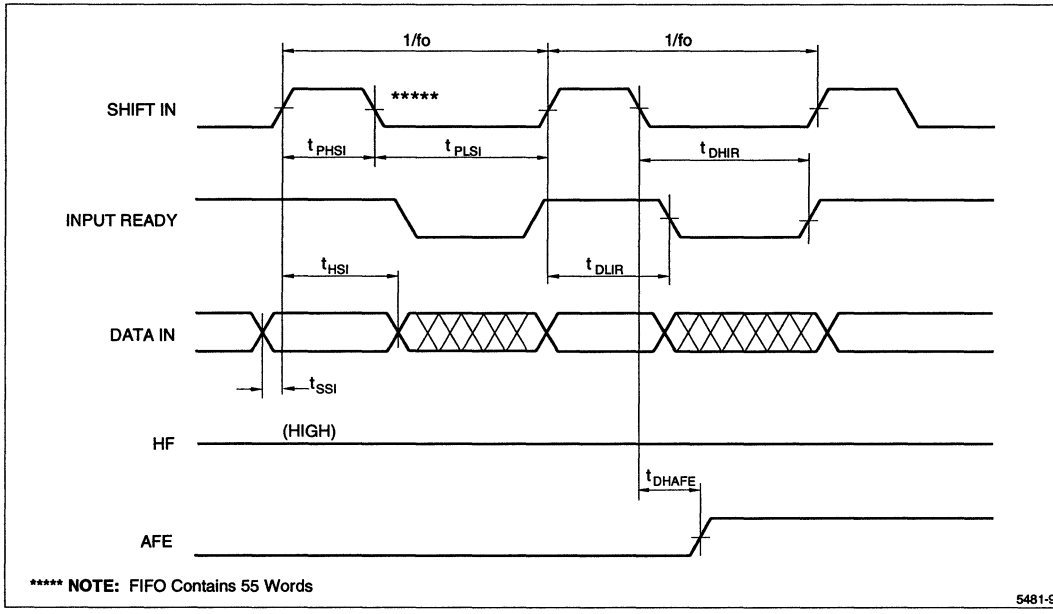


Figure 9. Data In Timing

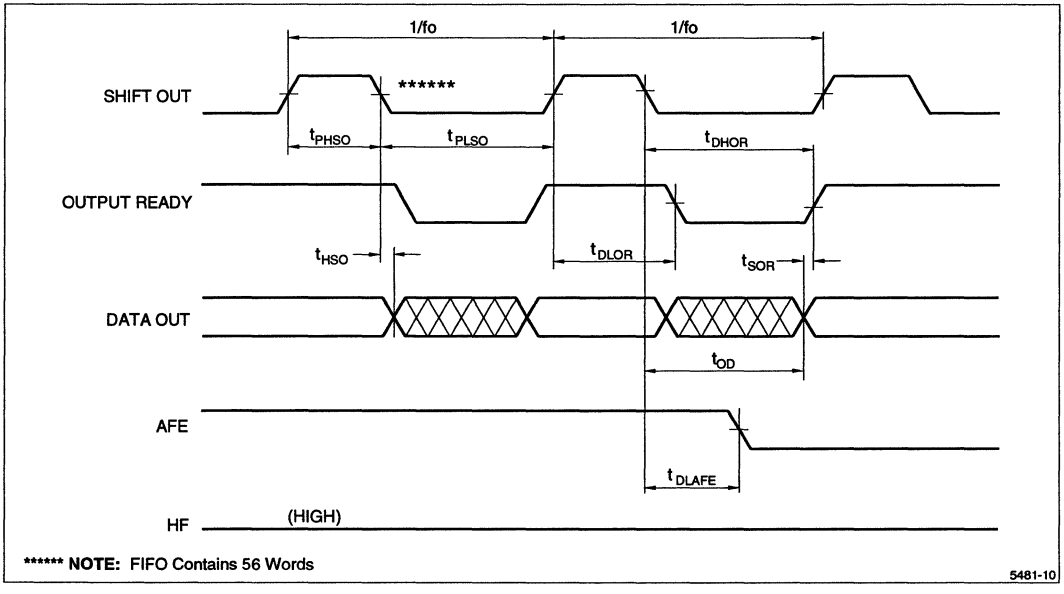


Figure 10. Data Out Timing

TIMING DIAGRAMS (cont'd)

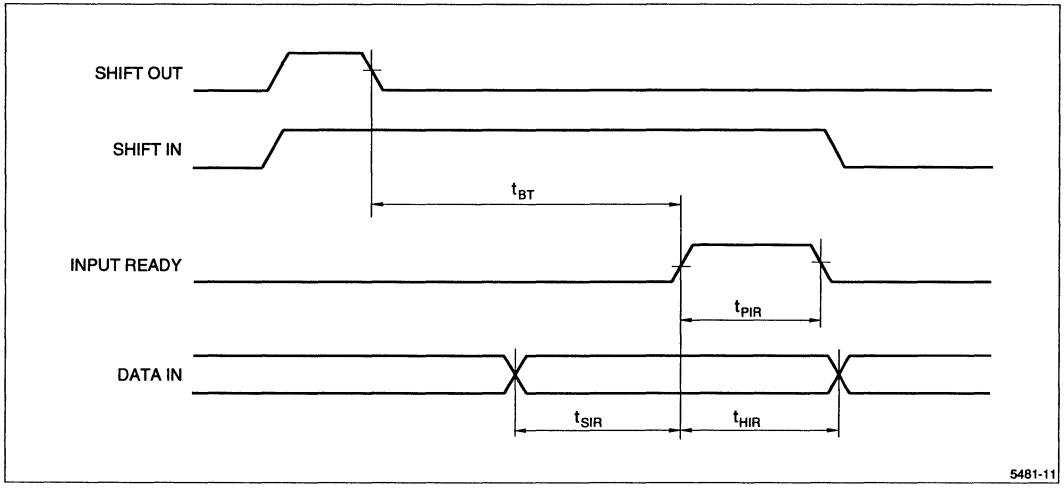


Figure 11. Bubblethrough Timing (Reading a Full FIFO)

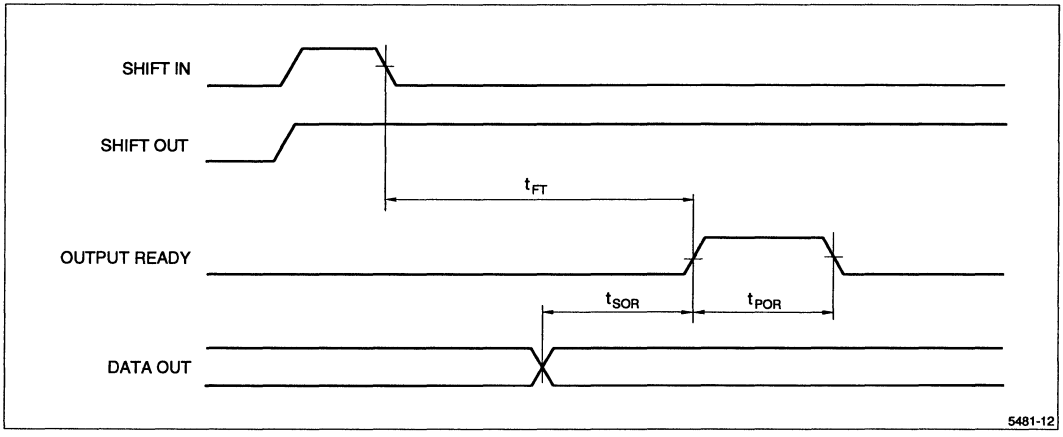


Figure 12. Fallthrough Timing (Writing an Empty FIFO)

TIMING DIAGRAMS (cont'd)

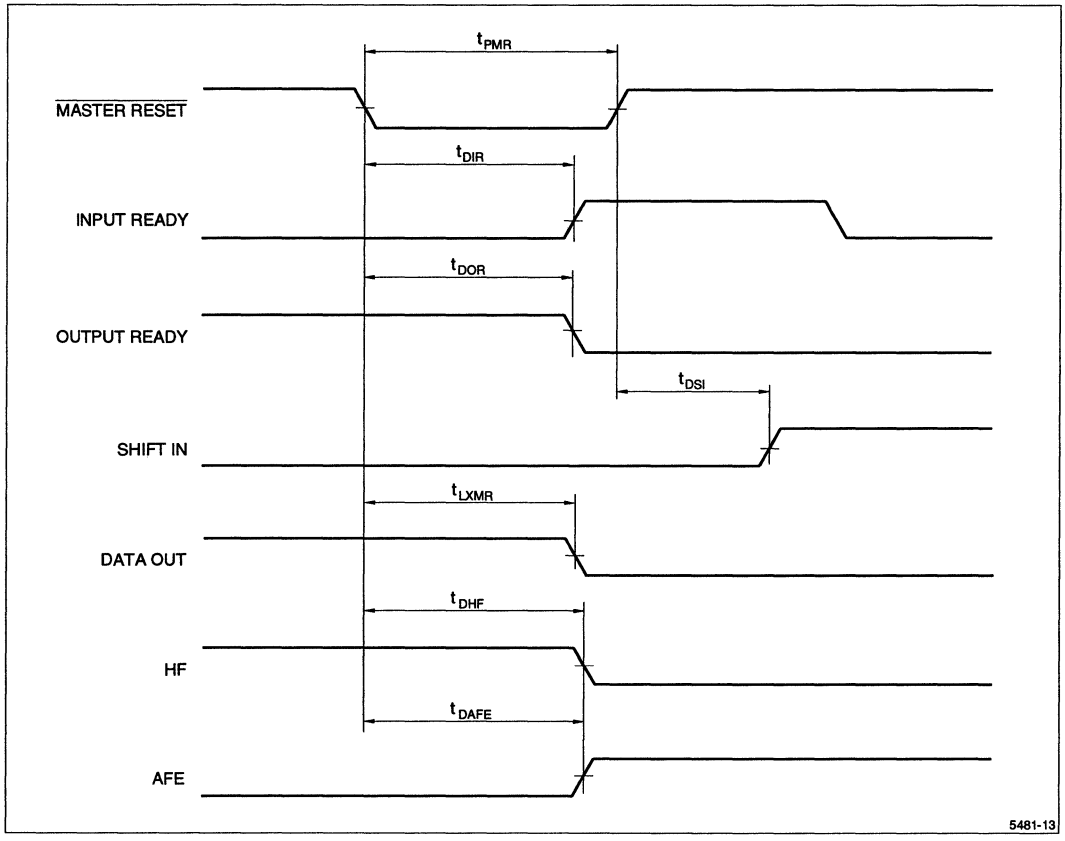


Figure 13. Master Reset Timing

TIMING DIAGRAMS (cont'd)

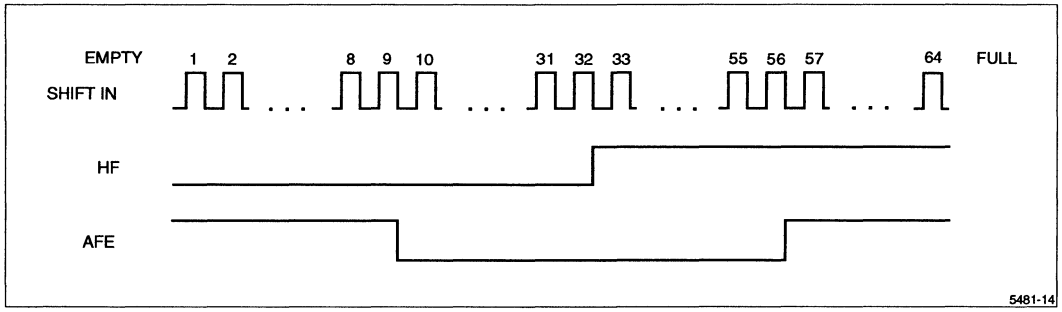


Figure 14. Shifting Words In

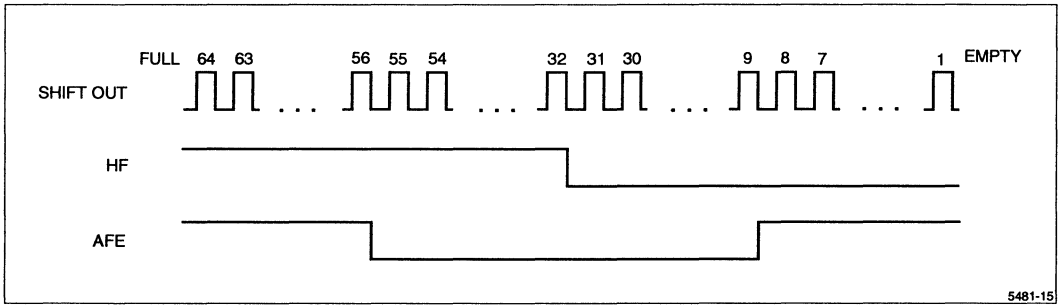


Figure 15. Shifting Words Out

FIFO EXPANSION

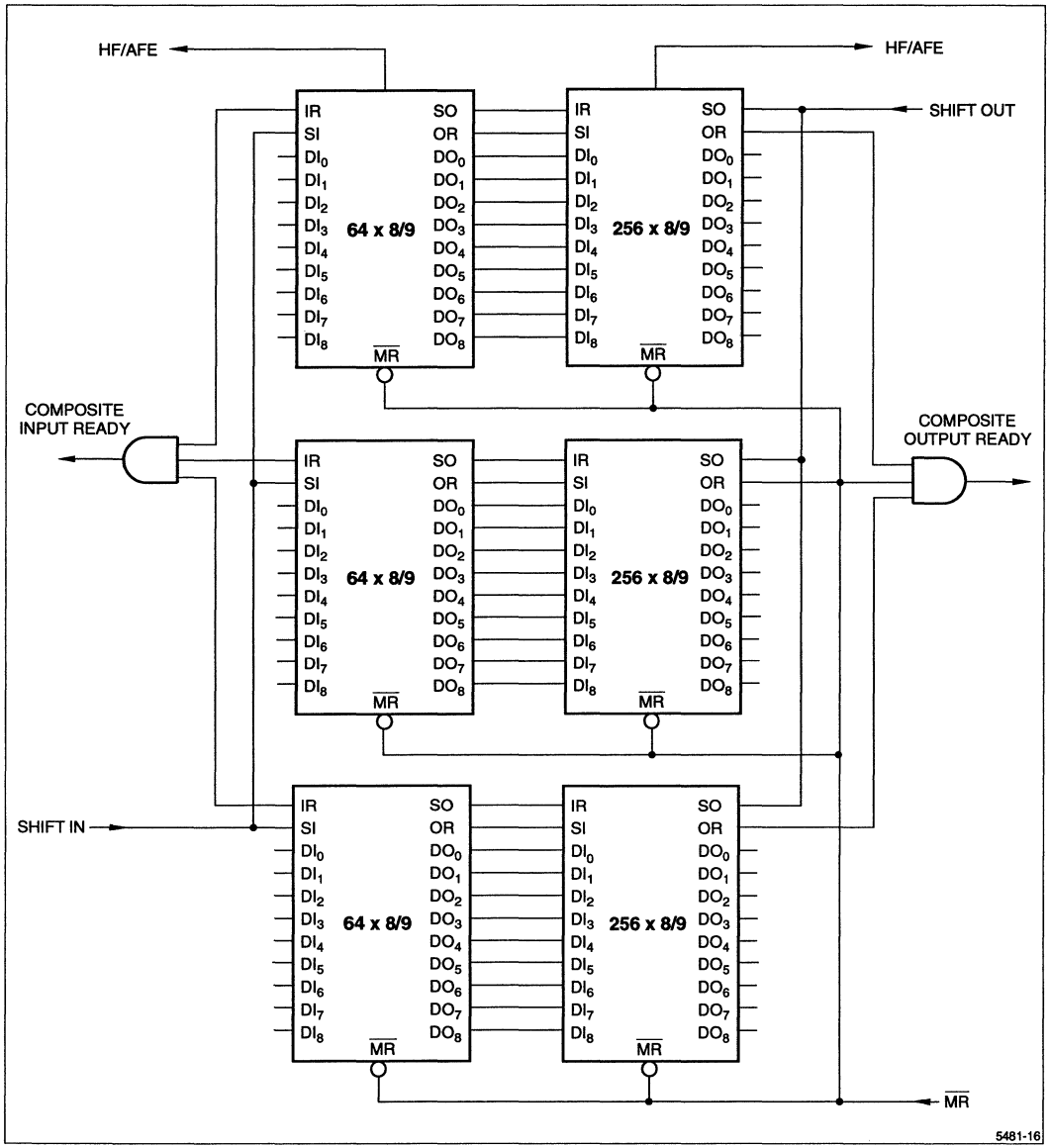


Figure 16. 320 × 24/27 Configuration Using 64 × 8/9 (LH5481/91) & 256 × 8/9 (LH5485/95) FIFOs

FIFO EXPANSION (cont'd)

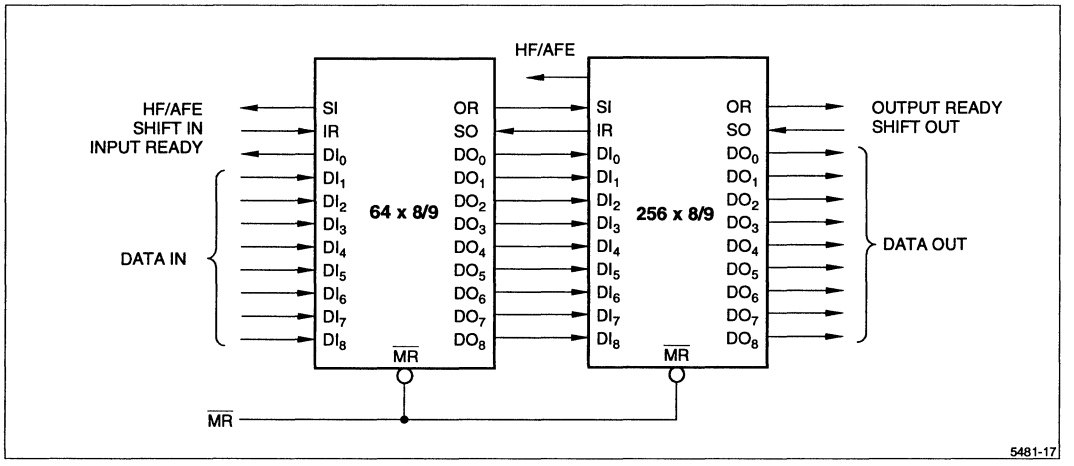


Figure 17. 128 × 8/9 Configuration

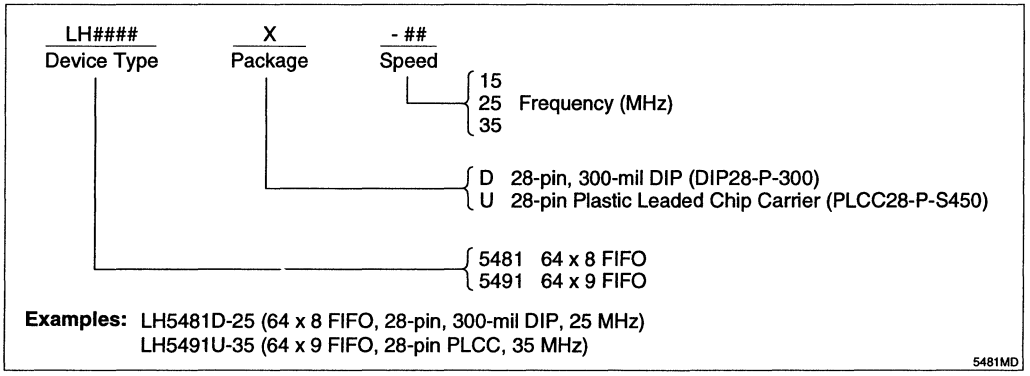
FIFOs are expandable in depth and width. However, in forming wider words, external logic is required to generate composite Input Ready and Output Ready flags. This is due to the variation of delays of the FIFOs. For example, the circuit of Figure 16 uses simple AND gates as the external IR and OR generators. More complex logic may be required if fallthrough and bubblethrough pulses are needed by the external system.

FIFOs can be easily cascaded to any desired depth, as illustrated in Figure 17. The handshaking and associated timing between the FIFOs are handled by the inherent timing of the devices.

NOTES:

1. When the memory is empty, the last word read remains on the outputs until Master Reset is strobed, or a new data word bubbles through to the output. However, OR remains LOW, indicating that the data word at the output is not valid.
2. When the output data word changes as a result of a pulse on SO, the OR signal always goes LOW before the output data word changes and stays LOW until a new data word has appeared at the outputs. Anytime OR is HIGH, there is valid stable data on the outputs.
3. All SHARP FIFOs can be cascaded with other SHARP FIFOs of the same architecture (i.e., 64 × 8/9 with 64 × 8/9). However, they may not cascade with FIFOs from other manufacturers.

ORDERING INFORMATION



LH5492

4K × 9 Clocked FIFO

FEATURES

- Fast Cycle Times: 25/30/35 ns
  Frequency: 40/33/28.5 MHz
- Parallel Data In; Parallel Data Out
- Two Read Enable Inputs and Two Write Enable Inputs, Sampled on Rising Edge of the Appropriate Clock
- Fast-Fall-Through Time Internal Architecture Based on CMOS Dual-Port SRAM Technology, 4096 × 9
- Independently-Synchronized Operation of Input Port and Output Port
- Full, Half-Full, Almost-Empty/Full, and Empty Flags
- Three-State Outputs with Output Enable
- May be Used for Bidirectional Bus Interfaces
- May be Used to Interface between Buses of Different Word Widths
- Reset/Reread Capability
- TTL and CMOS Compatible I/O
- Package: 32-Pin PLCC

FUNCTIONAL DESCRIPTION

The LH5492 is a FIFO (First-In, First-Out) memory device, based on fully-static CMOS dual-port RAM technology, capable of containing up to 4096 nine-bit words. A single LH5492 FIFO can input and output nine-bit bytes; it has one nine-bit parallel input (write) port, and one nine-bit parallel output (read) port. Multiple write enables and read enables support paralleling LH5492s for greater-word-width operation, in order to achieve a *wider* 'effective FIFO.' The paralleled LH5492 combination remains capable of performing all of the operations which a standalone LH5492 can perform. Thus, if two LH5492s are paralleled, the combination can input and output 18-bit halfwords. This paralleling scheme extends to an *arbitrary* number of paralleled LH5492s, although some external logic is required for more than two.

The LH5492 architecture supports synchronous operation, tied to two independent free-running clocks at the input and output ports respectively. However, these 'clocks' also may be aperiodic, asynchronous 'demand' signals; they do not need to be synchronized with each other in any way. Almost all control input signals and status output signals are synchronized to these clocks, to simplify system design. The input and output ports operate altogether independently of each other, except when the FIFO becomes either totally full or else totally empty.

Two edge-sampled enable control inputs, WEN_1 and WEN_2, are provided for the input port; and two more such control inputs, REN_1 and REN_2, are provided for the output port. These synchronous control inputs may be used as write demands and read demands respectively, when an LH5492 is interfaced to continuously-clocked synchronous systems. Data flow is initiated at a port by the rising edge of the clock signal corresponding to that port, and is gated only by the appropriate edge-sampled enable control input signal(s).

The following FIFO status flags monitor the extent to which the internal memory has been filled: Full, Half-Full, Almost-Empty/Full, and Empty. The Almost-Empty/Full flag is asserted whenever the internal memory is either within eight locations of 'empty,' or else within eight locations of 'full.' The Half-Full flag serves to distinguish the 'almost-empty' condition from the 'almost-full' condition. Also, during fully-synchronous operation, the Full flag may be tied directly to WEN_1 or to WEN_2, and the Empty flag likewise may be tied directly to REN_1 or REN_2, in order to prevent overrunning or underrunning the internal FIFO boundaries. (See Figure 10.)

PIN CONNECTIONS

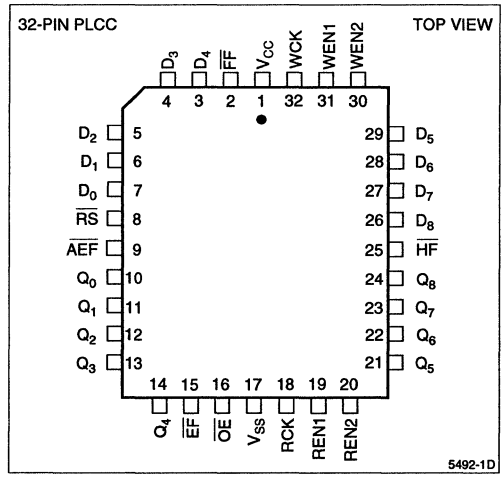


Figure 1. Pin Connections for PLCC Package

FUNCTIONAL DESCRIPTION (cont'd)

Alternatively, the enabling of write or read operations may be controlled entirely by external system logic, while the flags serve strictly as system interrupts. This design approach works well when the input port clock and the output port clock are not synchronized to each other.

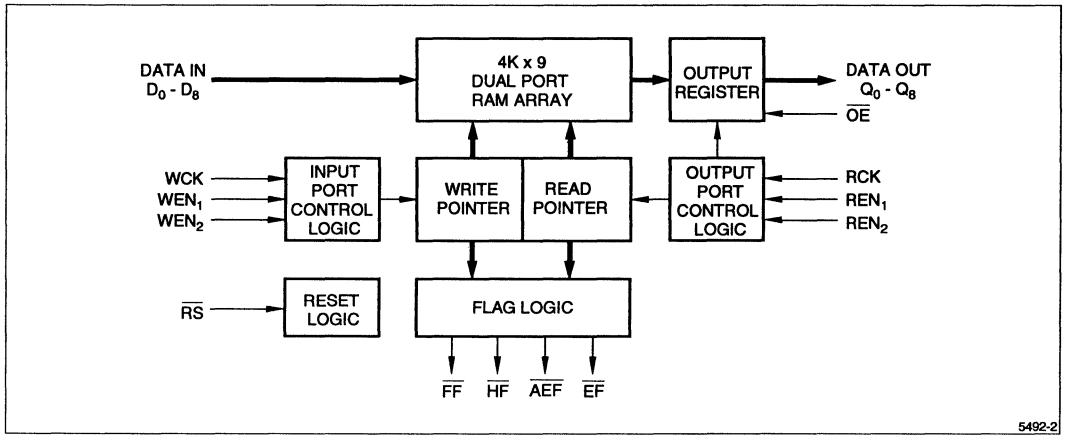


Figure 2. LH5492 Block Diagram

SIGNAL/PIN DESCRIPTIONS

PIN	SIGNAL NAME/DESCRIPTION
$\overline{RS}$	Reset. An assertive-LOW input which initializes the internal address pointers and flags.
WCK	Write Clock. A free-running clock input for write operations.
RCK	Read Clock. A free-running clock input for read operations.
$D_0 - D_8$	Data Inputs. $D_0 - D_8$ are sampled on the rising edge of WCK, whenever both WEN_1 and WEN_2 are being asserted.
$Q_0 - Q_8$	Data Outputs. $Q_0 - Q_8$ are updated following the rising edge of RCK, whenever both REN_1 and REN_2 are being asserted.
WEN_1	Write Enable 1. An assertive-HIGH input signal which is sampled on the rising edge of WCK to control the flow of data into the FIFO. Both WEN_1 and WEN_2 must be asserted in order to enable a write operation.
WEN_2	Write Enable 2. An assertive-HIGH input signal which is sampled on the rising edge of WCK to control the flow of data into the FIFO. Both WEN_1 and WEN_2 must be asserted in order to enable a write operation.
REN_1	Read Enable 1. An assertive-HIGH input signal which is sampled on the rising edge of RCK to control the flow of data out of the FIFO. Both REN_1 and REN_2 must be asserted in order to enable a read operation.
REN_2	Read Enable 2. An assertive-HIGH input signal which is sampled on the rising edge of RCK to control the flow of data out of the FIFO. Both REN_1 and REN_2 must be asserted in order to enable a read operation.
$\overline{FF}$	Full Flag. An assertive-LOW output indicating when the FIFO is full.
$\overline{HF}$	Half-Full Flag. An assertive-LOW output indicating when the FIFO is more than half full.
$\overline{AEF}$	Almost-Empty/Full. An assertive-LOW output indicating when the FIFO either is within eight locations of full, or else is within eight locations of empty.
$\overline{EF}$	Empty Flag. An assertive-LOW output indicating when the FIFO is empty.
$\overline{OE}$	Output Enable. An assertive-LOW signal which, when asserted, places the data outputs $Q_0 - Q_8$ in a low-impedance state.

ABSOLUTE MAXIMUM RATINGS [1]

PARAMETER	RATING
Supply Voltage to V_{SS} Potential	−0.5 V to 7 V
Signal Pin Voltage to V_{SS} Potential[3]	−0.5 V to V_{CC} + 0.5 V
DC Output Current [2]	± 40 mA
Storage Temperature Range	−65°C to 150°C
Power Dissipation (Package Limit)	1.0 W

NOTES:

1. Stresses greater than those listed under 'Absolute Maximum Ratings' may cause permanent damage to the device. This is a stress rating for transient conditions only. Functional operation of the device at these or any other conditions outside those indicated in the 'Operating Range' of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Outputs should not be shorted for more than 30 seconds. No more than one output should be shorted at any time.
3. Negative undershoots of 1.5 V in amplitude are permitted for up to 10 ns, once per cycle.

OPERATING RANGE

SYMBOL	PARAMETER	MIN	MAX	UNIT
T_A	Temperature, Ambient	0	70	°C
V_{CC}	Supply Voltage	4.5	5.5	V
V_{SS}	Supply Voltage	0	0	V
V_{IL}	Logic LOW Input Voltage [1]	−0.5	0.8	V
V_{IH}	Logic HIGH Input Voltage	2.2	V_{CC} + 0.5	V

NOTE:

1. Negative undershoots of 1.5 V in amplitude are permitted for up to 10 ns once per cycle.

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
I_{LI}	Input Leakage Current	V_{CC} = 5.5 V, V_{IN} = 0 V to V_{CC}	−10	10	µA
I_{LO}	Output Leakage Current	$\overline{OE} \geq V_{IH}$, 0 V ≤ V_{OUT} ≤ V_{CC}	−10	10	µA
V_{OL}	Output LOW Voltage	I_{OL} = 8.0 mA		0.4	V
V_{OH}	Output HIGH Voltage	I_{OH} = −2.0 mA	2.4		V
I_{CC}	Average Supply Current [1]	Measured at f_C = max		150	mA
I_{CC2}	Average Standby Current [1]	All Inputs = V_{IH}		35	mA

NOTE:

1. I_{CC} and I_{CC2} are dependent upon actual output loading and cycle rates. Specified values are with outputs open; and, for I_{CC}, operating at minimum cycle times.

AC TEST CONDITIONS

PARAMETER	RATING
Input Pulse Levels	V_{SS} to 3 V
Input Rise and Fall Times (10% to 90%)	5 ns
Input Timing Reference Levels	1. 5 V
Output Reference Levels	1.5 V
Output Load, Timing Tests	Figure 3

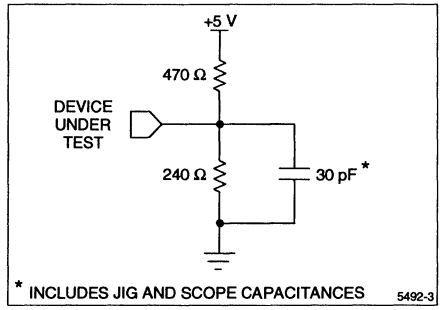


Figure 3. Output Load Circuit

CAPACITANCE [1,2]

PARAMETER	RATING
C_{IN} (Input Capacitance)	7 pF
C_{OUT} (Output Capacitance)	7 pF

NOTES:

1. Sample tested only.
2. Capacitances are maximum values at 25°C, measured at 1.0 MHz with V_{IN} = 0 V.

AC ELECTRICAL CHARACTERISTICS [1] (V_{CC} = 5 V ± 10%, T_A = 0°C to 70°C)

SYMBOL	DESCRIPTION	-25		-30		-35		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
f_C	Cycle Frequency	–	40	–	33.3	–	28.5	MHz
t_{WC}	Write Clock Cycle Time	25	–	30	–	35	–	ns
t_{WH}	Write Clock HIGH Time	10	–	12	–	14	–	ns
t_{WL}	Write Clock LOW Time	10	–	12	–	14	–	ns
t_{RC}	Read Clock Cycle Time	25	–	30	–	35	–	ns
t_{RH}	Read Clock HIGH Time	10	–	12	–	14	–	ns
t_{RL}	Read Clock LOW Time	10	–	12	–	14	–	ns
t_{DS}	Data Setup Time to Rising Clock	10	–	10	–	10	–	ns
t_{DH}	Data Hold Time from Rising Clock	0	–	0	–	0	–	ns
t_{ES}	Enable Setup Time to Rising Clock	10	–	10	–	10	–	ns
t_{EH}	Enable Hold Time from Rising Clock	0	–	0	–	0	–	ns
t_A	Data Output Access Time	–	20	–	22	–	25	ns
t_{OH}	Output Hold Time from Rising RCK	5	–	5	–	5	–	ns
t_{QL}	$\overline{OE}$ to Data Outputs Low-Z [2]	1	–	1	–	1	–	ns
t_{QZ}	$\overline{OE}$ to Data Outputs High-Z [2]	–	10	–	11	–	12	ns
t_{OE}	Output Enable to Data Valid	–	10	–	11	–	12	ns
t_{EF}	Clock to Empty Flag Valid	–	20	–	22	–	25	ns
t_{FF}	Clock to Full Flag Valid	–	20	–	22	–	25	ns
t_{HF}	Clock to Half Flag Valid	–	35	–	37	–	40	ns
t_{AEF}	Clock to AEF Flag Valid	–	35	–	37	–	40	ns
t_{RS}	Reset Pulse Width	25	–	30	–	35	–	ns
t_{RSS}	Reset Setup Time [3]	10	–	12	–	15	–	ns
t_{RF}	Reset LOW to Flag Valid	–	30	–	32	–	35	ns
t_{RQ}	Reset to Data Outputs LOW	–	20	–	22	–	25	ns
t_{FRL}	First Read Latency [4]	18	–	19	–	20	–	ns
t_{FWL}	First Write Latency [5]	18	–	19	–	20	–	ns

NOTES:

1. All timing measurements performed at 'AC Test Condition' levels.
2. Value guaranteed by design; not currently production tested.
3. t_{RSS} need not be met *unless* either a rising edge of WCK occurs while WEN_1 and WEN_2 both are being asserted, or else a rising edge of RCK occurs while REN_1 and REN_2 both are being asserted.
4. t_{FRL} is the minimum first-write-to-first read delay, following an empty condition, which is required to assure valid read data.
5. t_{FWL} is the minimum first-read-to-first-write delay, following a full condition, which is required to assure successful writing of data.

OPERATIONAL DESCRIPTION

Reset

The device is reset whenever the asynchronous reset input ($\overline{RS}$) is asserted, i.e., taken to a LOW state. A reset operation is required after power up, before the first write operation occurs. The reset operation initializes both the read and write address pointers to the first physical memory location. After the falling edge of $\overline{RS}$, the status flags ($\overline{FF}$, $\overline{HF}$, $\overline{AEF}$, and $\overline{EF}$) are updated to indicate a valid empty condition.

Write and/or read operations need not be deactivated during a reset operation, but failure to do so requires observance of the Reset Setup Time (t_{RSS}) to assure that the first write and/or first read following reset will occur predictably.

If no read operations have been performed following a reset operation, then the 'previous data' word being held in the output register consists of all zeroes. This data word is seen on the output bus ($Q_0 - Q_8$) whenever the output enable ($\overline{OE}$) is being held LOW.

Write

A write operation consists of storing parallel data from the data inputs to the FIFO memory array. A write operation is initiated on the rising edge of the Write Clock input (WCK), whenever both of the edge-sampled Write Enable inputs (WEN_1 and WEN_2) are held HIGH for the prescribed setup times and hold times. Setup times and hold times must also be observed for the Data In pins (D_0–D_8).

When a full condition is reached, write operations should be ceased, in order to prevent overwriting unread data. The state of the four status flags has no direct effect on write operations; that is, the execution of write operations is gated only by WEN_1 and WEN_2, and the internal logic of the LH5492 itself has no interlock to prevent overrunning valid data after the internal write pointer 'wraps around' and catches up to the read pointer – and passes it, if writing is continued. Figure 10 illustrates how such an interlock may be implemented by means of external connections.

Following the first read operation from a full FIFO, another memory location becomes freed up, and the Full Flag is deasserted ($\overline{FF}$ = HIGH). The next write operation should begin no earlier than a First Write Latency time (t_{FWL}) after the first read operation from a full FIFO, in order to assure that a correct data word is written into the FIFO memory.

Read

A read operation consists of loading parallel data from the FIFO memory array to the output register. A read operation is initiated on the rising edge of the Read Clock input (RCK), whenever both of the edge-sampled Read Enable inputs (REN_1 and REN_2) are held HIGH for the prescribed setup times and hold times. Read data becomes valid on the Data Out pins ($Q_0 - Q_8$) by a time t_A after the rising edge of RCK, provided that the Output Enable ($\overline{OE}$) is being held LOW. $\overline{OE}$ is an assertive-LOW asynchronous input. When $\overline{OE}$ is taken LOW, the $Q_0 - Q_8$ outputs are driven (i.e., are in a low-Z state) within a minimum time t_{OL}. When $\overline{OE}$ is taken HIGH, the $Q_0 - Q_8$ outputs are in a high-Z state within a maximum time t_{OZ}.

When an empty condition is reached, read operations should be ceased, until a valid write operation(s) has loaded additional data into the FIFO. The state of the four status flags has no direct effect on read operations; that is, the execution of read operations is gated only by REN_1 and REN_2, and the internal logic of the LH5492 itself has no interlock to prevent underrunning valid data after the internal read pointer 'wraps around' and catches up to the write pointer – and passes it, if reading is continued. Figure 10 illustrates how such an interlock may be implemented by means of external connections.

Following the first write to an empty FIFO, the Empty Flag ($\overline{EF}$) is deasserted ($\overline{EF}$ = HIGH). The next read operation should begin no earlier than a First Read Latency time (t_{FRL}) from the first write operation into an empty FIFO, in order to ensure that correct read data is retrieved.

Status Flags

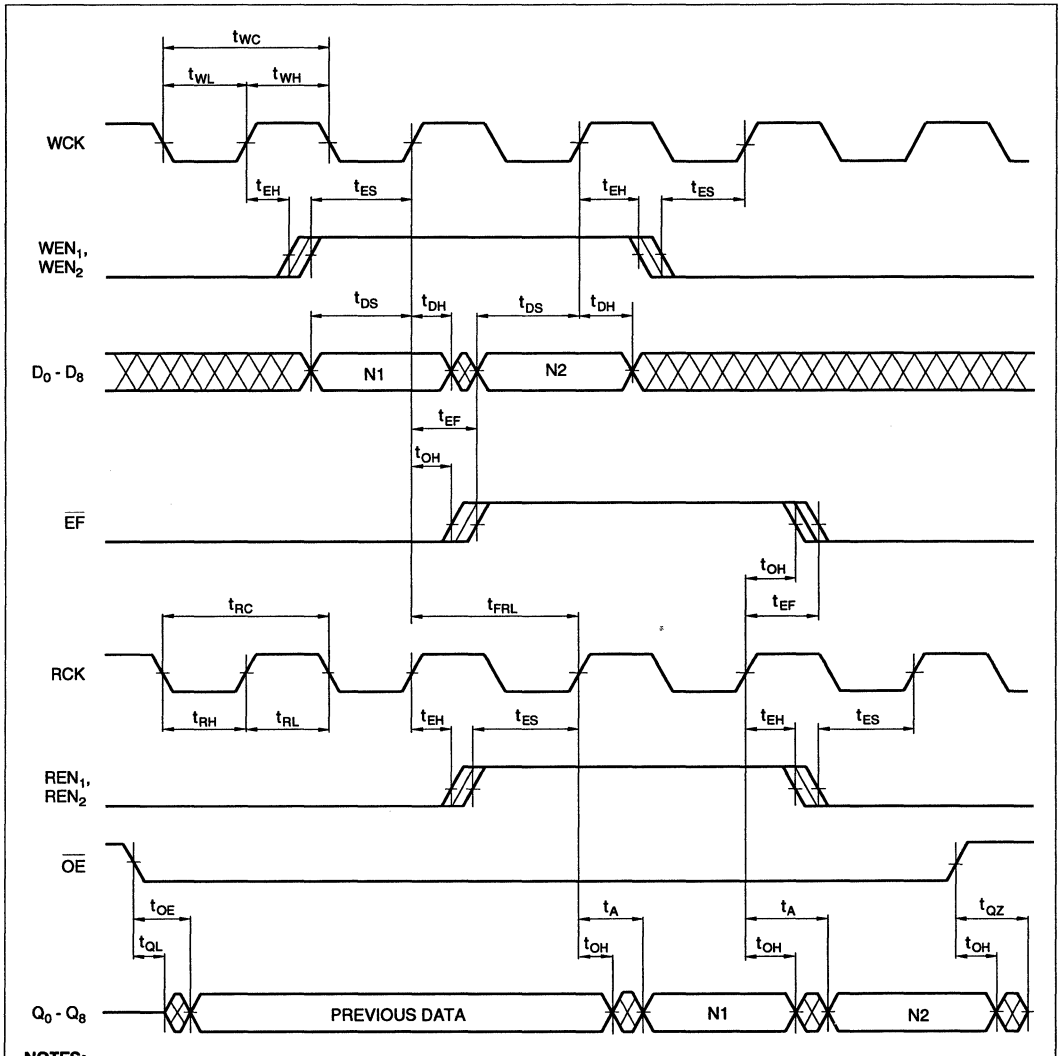
Status Flags are included for Full ($\overline{FF}$), Half-Full ($\overline{HF}$), Almost-Empty/Full ($\overline{AEF}$), and Empty ($\overline{EF}$). These flags are updated at the boundary conditions given in Table 1. Flag transitions follow the appropriate rising clock edge during an enabled read or write operation. The $\overline{AEF}$ flag is asserted whenever the FIFO either is less than eight locations away from an empty boundary, or else is less than eight locations away from a full boundary.

A separate indicator for Almost-Empty may be generated by a logical NOR of $\overline{AEF}$ with the inversion of $\overline{HF}$. An indicator for Almost-Full may be generated by a NOR of $\overline{AEF}$ with $\overline{HF}$. From an assertive-HIGH perspective, the NOR gate effectively is performing an AND operation in both of these cases.

Reset, Reread

The FIFO can be made to reread previously read data through a reset operation, which initializes the internal read-address and write-address pointers to the first physical location in the FIFO memory (location zero). The status flags are updated to indicate an empty condition; but up to 4096 data words which previously had been written into and/or read from the FIFO still then remain in the FIFO memory array. The status flags may be ignored, and data may be reaccessed by subsequent read operations. The First Read Latency (t_{FRL}) specification does not apply to reset/reread operations, since no new data words are being written to the FIFO following the reset operation.

TIMING DIAGRAMS



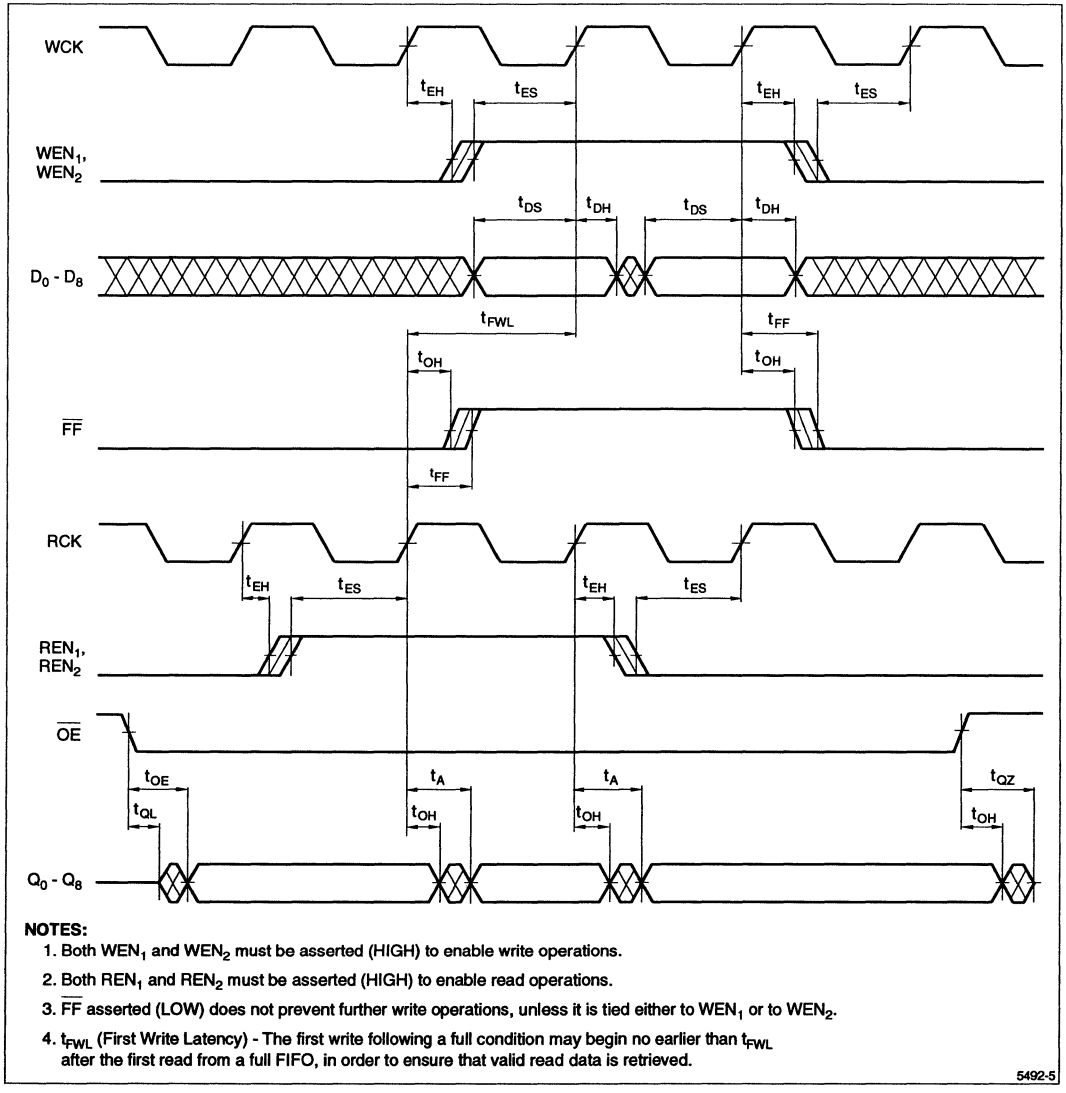
NOTES:

1. Both WEN_1 and WEN_2 must be asserted (HIGH) to enable write operations.
2. Both REN_1 and REN_2 must be asserted (HIGH) to enable read operations.
3. $\overline{EF}$ asserted (LOW) does not prevent further read operations, unless it is tied either to REN_1 or to REN_2.
4. t_{FRL} (First Read Latency) - The first read following an empty condition may begin no earlier than t_{FRL} after the first write to an empty FIFO, to assure valid data is retrieved. This specification does not apply to reset/reread applications, in which the status of FIFO flags is ignored.
5. Immediately following a reset operation, the 'previous data' will be all bits LOW.

5492-4

Figure 4. Write and Read Operation in a Near-Empty Condition

TIMING DIAGRAMS (cont'd)



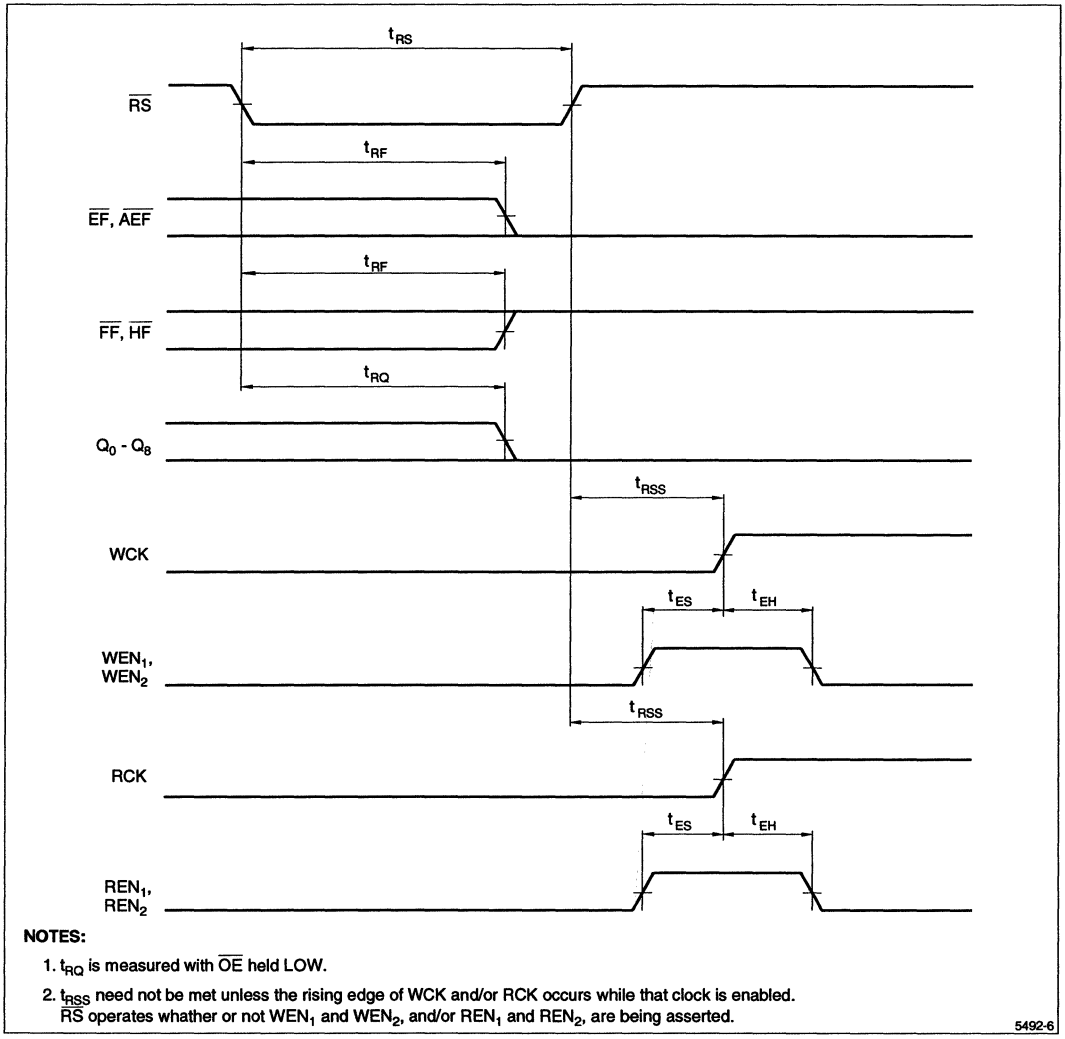
NOTES:

1. Both WEN_1 and WEN_2 must be asserted (HIGH) to enable write operations.
2. Both REN_1 and REN_2 must be asserted (HIGH) to enable read operations.
3. $\overline{FF}$ asserted (LOW) does not prevent further write operations, unless it is tied either to WEN_1 or to WEN_2.
4. t_{FWL} (First Write Latency) - The first write following a full condition may begin no earlier than t_{FWL} after the first read from a full FIFO, in order to ensure that valid read data is retrieved.

5492-5

Figure 5. Read and Write Operation in a Near-Full Condition

TIMING DIAGRAMS (cont'd)



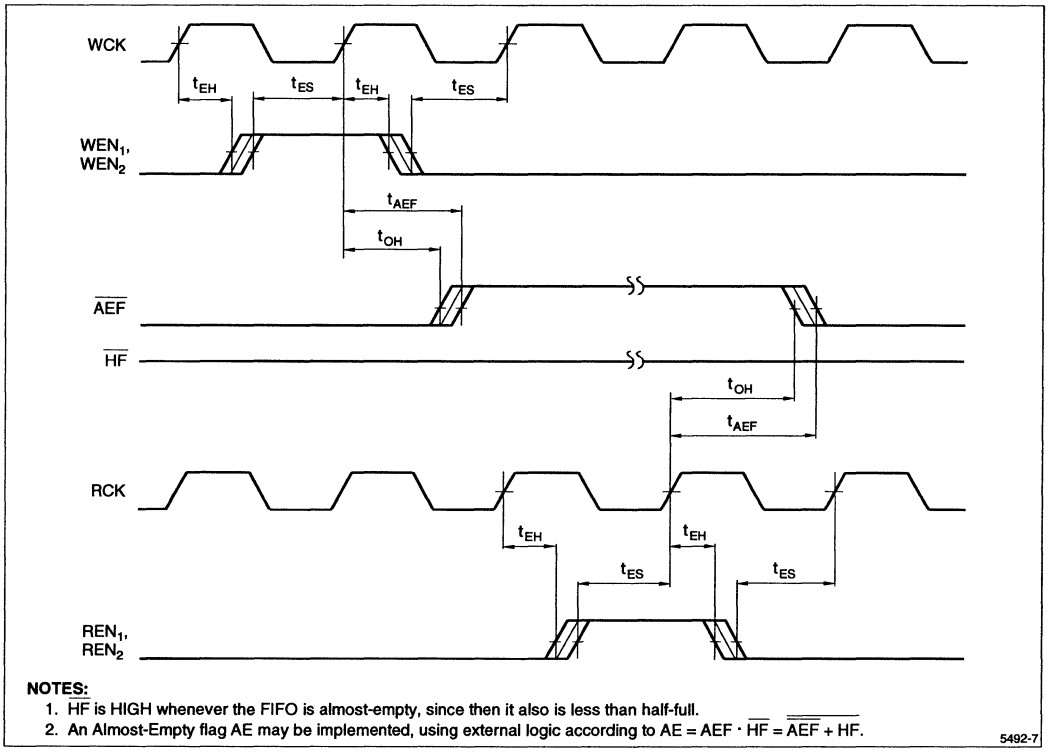
NOTES:

1. t_{RQ} is measured with $\overline{OE}$ held LOW.
2. t_{RSS} need not be met unless the rising edge of WCK and/or RCK occurs while that clock is enabled. $\overline{RS}$ operates whether or not WEN_1 and WEN_2, and/or REN_1 and REN_2, are being asserted.

5492-6

Figure 6. Reset Timing

TIMING DIAGRAMS (cont'd)



NOTES:
1. $\overline{HF}$ is HIGH whenever the FIFO is almost-empty, since then it also is less than half-full.
2. An Almost-Empty flag AE may be implemented, using external logic according to $AE = AEF \cdot \overline{HF} = \overline{\overline{AEF} + HF}$.

5492-7

Figure 7. Almost-Empty Flag Timing

Table 1. Flag Definitions

FLAG STATUS				VALID WRITE CYCLES REMAINING		VALID READ CYCLES REMAINING	
$\overline{EF}$	AEF	$\overline{HF}$	$\overline{FF}$	min	max	min	max
0	0	1	1	4096	4096	0	0
1	0	1	1	4089	4095	1	7
1	1	1	1	2048	4088	8	2047
1	1	0	1	8	2047	2048	4088
1	0	0	1	1	7	4089	4095
1	0	0	0	0	0	4096	4096

TIMING DIAGRAMS (cont'd)

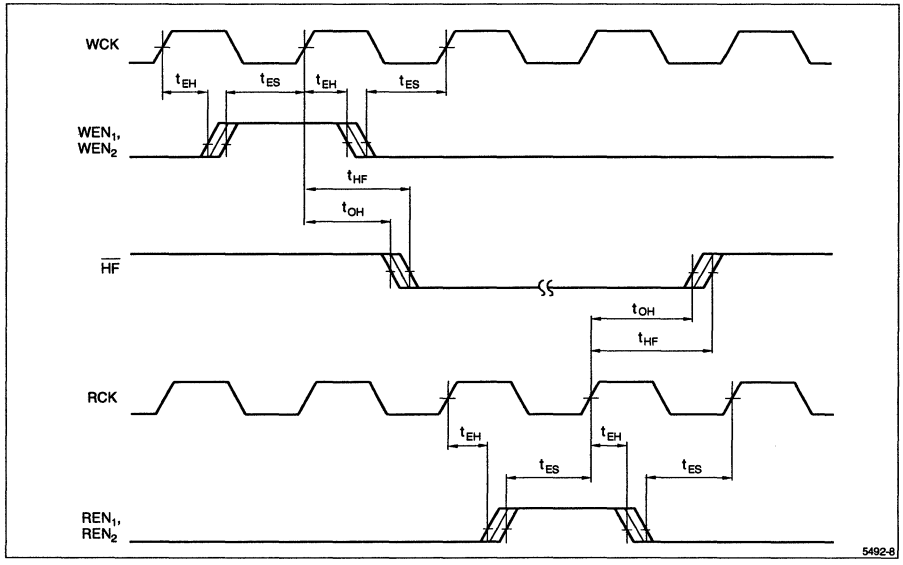


Figure 8. Half-Full Flag Timing

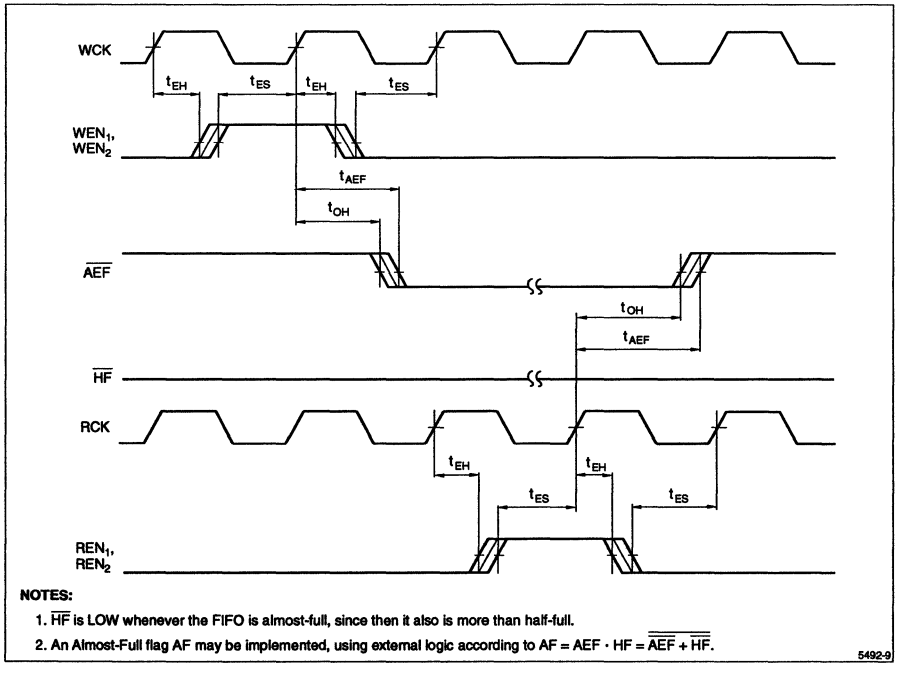


Figure 9. Almost-Full Flag Timing

OPERATIONAL MODES

Synchronous Read and Write Operations

Read and Write operations may be performed in synchronism with each other by deriving WCK and RCK from a *common* system clock. In this case, the Write Enable (WEN_1 and WEN_2) and Read Enable (REN_1 and REN_2) inputs all get sampled at the same clock rising edge.

This type of synchronous read/write operation ensures that flag outputs always satisfy the required setup and hold times for the WEN_1, WEN_2, REN_1, and REN_2 inputs. Thus, the Full Flag output ($\overline{FF}$) may be tied directly to either WEN_1 or WEN_2, to prevent 'overrun' write operations when the full condition is reached, while the other Write Enable input remains available for system control. Likewise, the Empty Flag output ($\overline{EF}$) may be tied directly to either REN_1 or REN_2, to prevent 'underrun' read operations when the empty condition is reached, while the other Read Enable input remains available for system control.

Asynchronous Read and Write Operations

Write operations and read operations also may be performed completely asynchronously, relative to each other, when the WCK input and the RCK input are derived from the clock signals of *different* systems. Under these conditions, status-flag transitions occur relative to two unpredictably-related clock edges. Therefore, these flags should not be used to drive Write Enable or Read Enable inputs directly, since they do not always satisfy valid setup times and hold times.

Instead, it is recommended that these enable signals be *controlled* by the user, in order to ensure that adequate setup times and hold times are maintained. If the FIFO becomes either completely full or completely empty, then some synchronization between read and write operations at the full or empty boundaries becomes necessary to prevent timing violations.

When the FIFO is operating in this manner, the Almost-Empty/Full flag and the Half-Full flag should be used to provide some advance warning, to avoid overrunning or underruning a FIFO internal boundary. Typically, these flags are used as system interrupts. When an interrupt is received by the faster of the two systems, a predefined block of data then may be transferred at the maximum data rate, as long as there is known to be sufficient room for it. In this way the full and empty boundaries are never reached, and yet maximum data throughput is maintained.

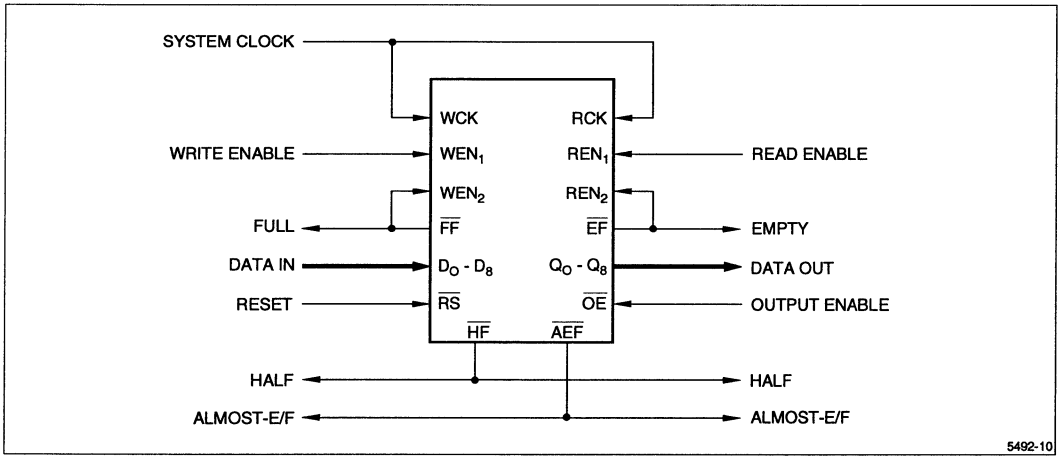


Figure 10. Synchronous Operation

OPERATIONAL MODES (cont'd)

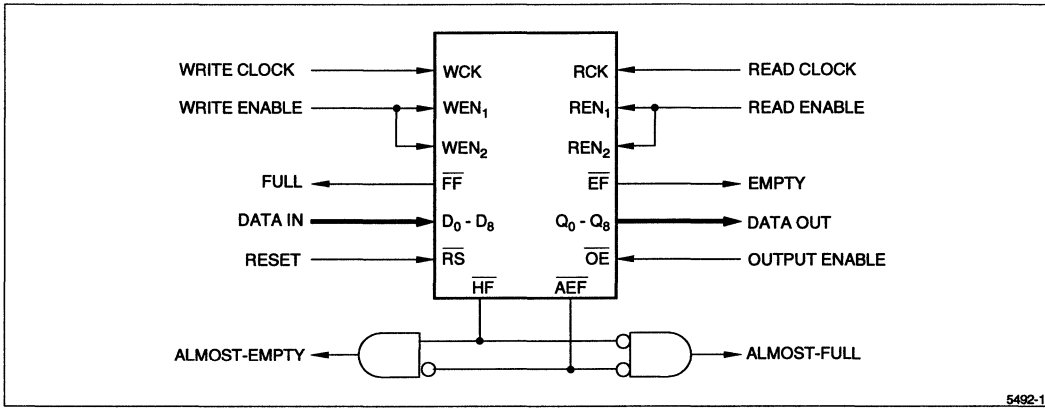


Figure 11. Asynchronous Operation

OPERATIONAL MODES (cont'd)

Depth Expansion

Increased FIFO depth may be realized by using multiple LH5492 devices. The availability of two enable control inputs for each port assists in this expansion. For either the input port or the output port, one enable input may be used for system control, while the other is driven by decode logic to direct the flow of data. Typically, this decode logic alternates accesses sequentially from one device to the next. Status flags are then derived from the last device in the sequence. The simplest form of this decode logic consists of a single toggle flipflop, which alternates access between two devices for every enabled clock cycle as shown in Figure 13.

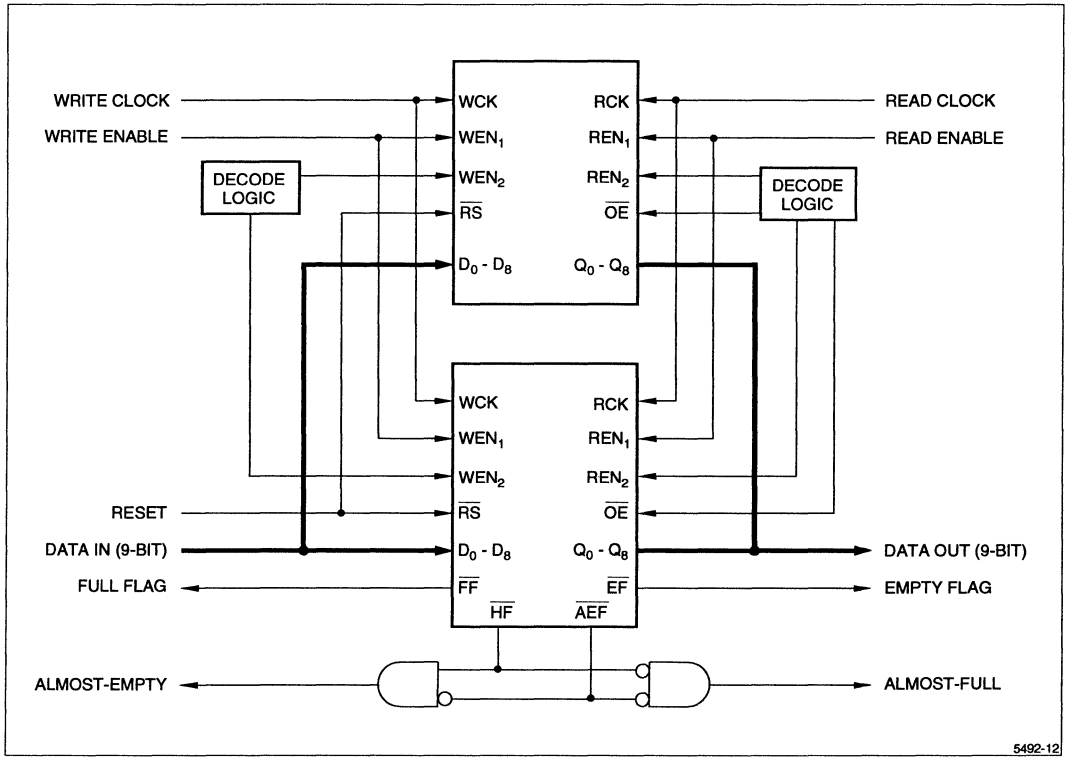


Figure 12. FIFO Depth Expansion (8192 × 9)

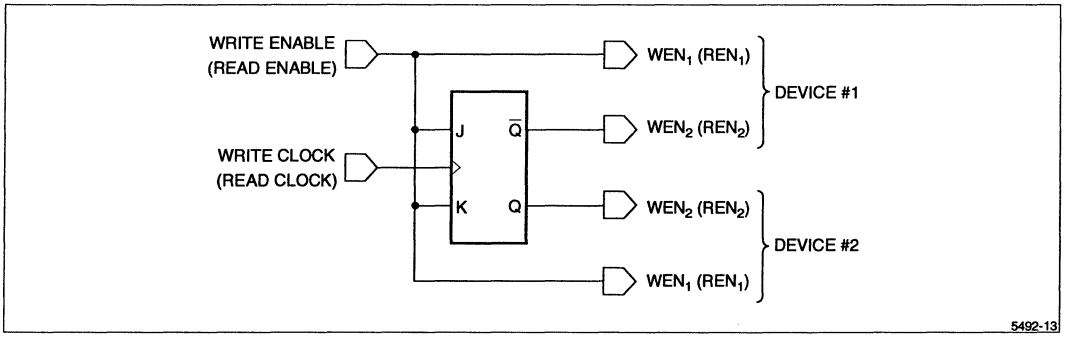


Figure 13. Simple Decode Logic

OPERATIONAL MODES (cont'd)

Interface Between Different Bus Widths

Applications which require interface between system buses of different word widths also may be implemented with multiple LH5492 devices. Essentially, one port may be configured for greater FIFO depth, while the other port is configured for greater word width. Referring to Figures 14 and 15, the wide-word port accesses data simultaneously from multiple devices, while the narrow-word port uses decode logic to direct the flow of data between two or more devices.

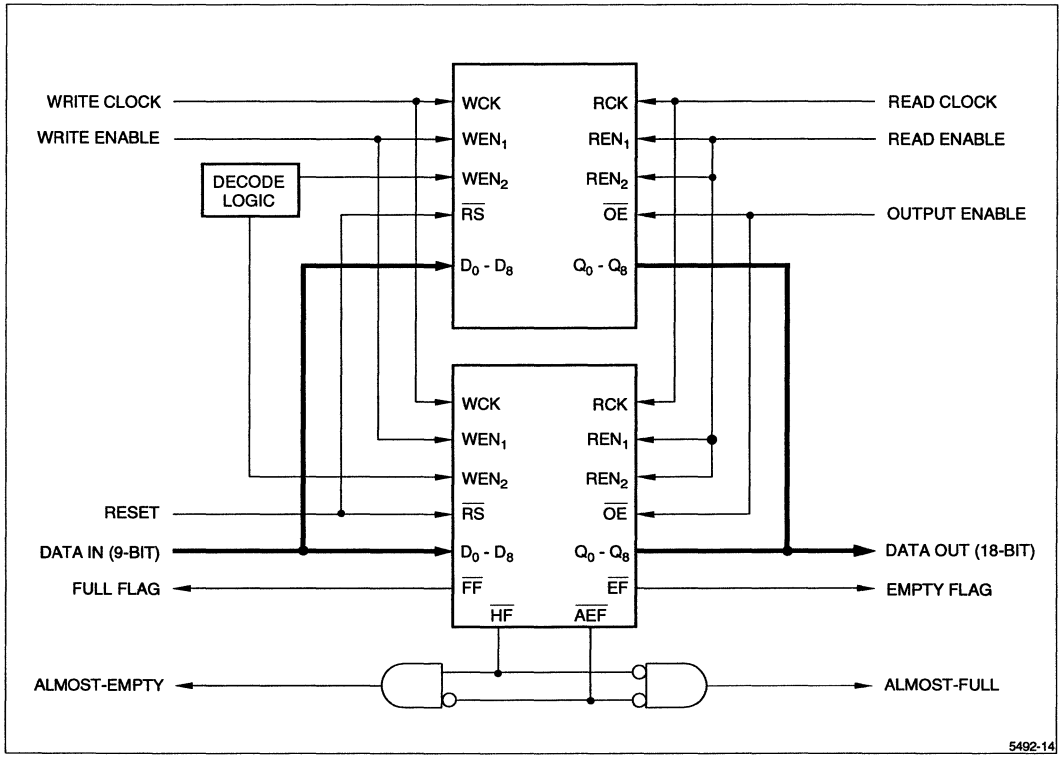


Figure 14. 8K × 9-Bit to 4K × 18-Bit Bus

OPERATIONAL MODES (cont'd)

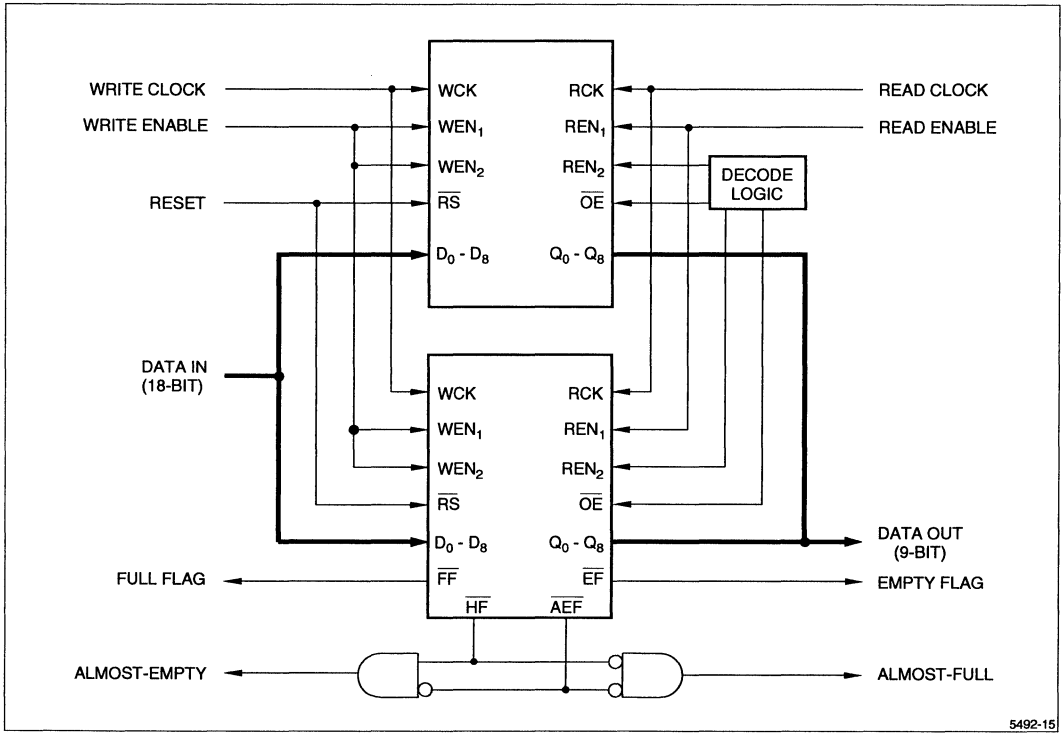


Figure 15. 4K × 18-Bit to 8K × 9-Bit Bus

OPERATIONAL MODES (cont'd)

Bidirectional Operation

Applications which require bidirectional data buffering between two systems may be realized by operating LH5492 devices in parallel, but in opposite directions. The Data In pins of one device may be tied to the corresponding Data Out pins of another device operating in the opposite direction, to form a single bidirectional bus interface. Care must be taken to assure that the appropriate clock, enable, and flag signals are routed to each system. The extra enable control signals may be used to extend FIFO depth, or to interface bidirectional buses of different word widths.

Width Expansion

Any of the previously described applications can be extended in word width by operating groups of these device configurations in parallel. The enable setup and hold times should be satisfied for *all* devices, in order to ensure that all width-expanded devices respond *identically* to the same sequence of events.

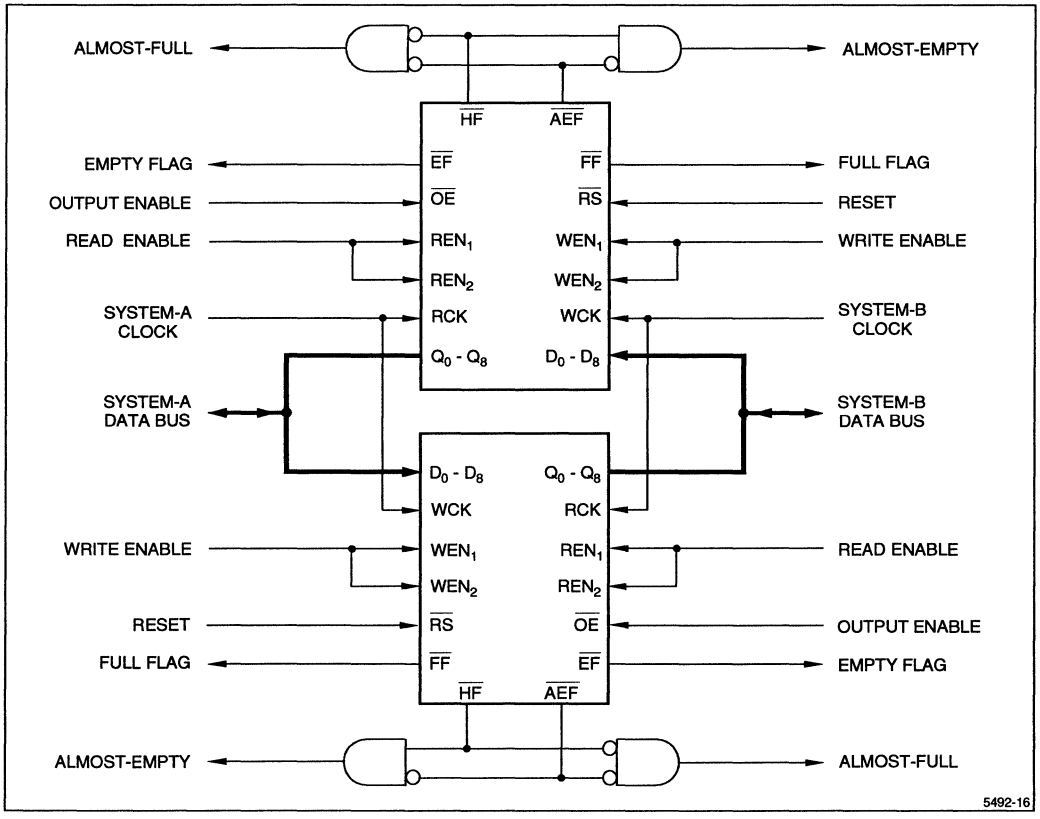
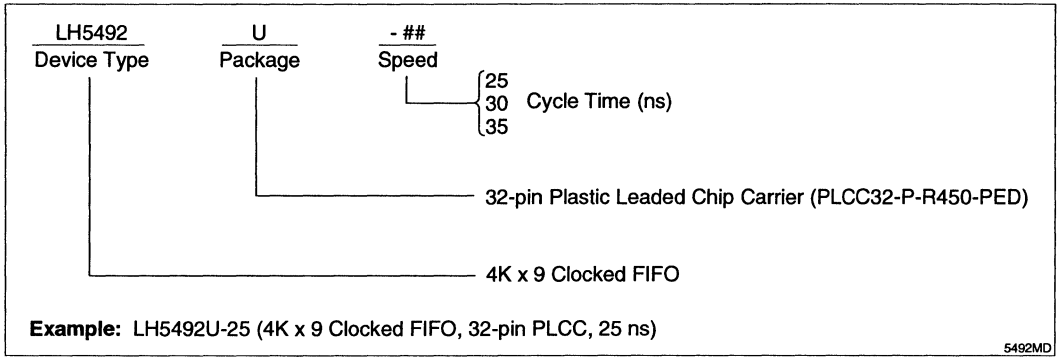


Figure 16. Bidirectional Operation

ORDERING INFORMATION



LH5496/96H

CMOS 512 × 9 FIFO

FEATURES

- Fast Access Times:
  15 */20/25/35/50/65/80 ns
- Full CMOS Dual Port Memory Array
- Fully Asynchronous Read and Write
- Expandable-in Width and Depth
- Full, Half-Full, and Empty Status Flags
- Read Retransmit Capability
- TTL Compatible I/O
- Packages:
  28-Pin, 300-mil DIP
  28-Pin, 600-mil DIP
  32-Pin PLCC
- Pin and Functionally Compatible with IDT7201

FUNCTIONAL DESCRIPTION

The LH5496/96H are dual port memories with internal addressing to implement a First-In, First-Out algorithm. Through an advanced dual port architecture, they provide fully asynchronous read/write operation. Empty, Full, and Half-Full status flags are provided to prevent data overflow and underflow. In addition, internal logic provides for unlimited expansion in both word size and depth.

Read and write operations automatically access sequential locations in memory in that data is read out in the same order that it was written, that is on a First-In, First-Out basis. Since the address sequence is internally predefined, no external address information is required for the operation of this device. A ninth data bit is provided for parity or control information often needed in communication applications.

Empty, Full, and Half-Full status flags monitor the extent to which data has been written into the FIFO, and prevent improper operations (i.e., Read if the FIFO is empty, or Write if the FIFO is full). A retransmit feature resets the Read address pointer to its initial position, thereby allowing repetitive readout of the same data. Expansion In and Expansion Out pins implement an expansion scheme that allows individual FIFOs to be cascaded to greater depth without incurring additional latency (bubblethrough) delays.

* LH5496 only.

PIN CONNECTIONS

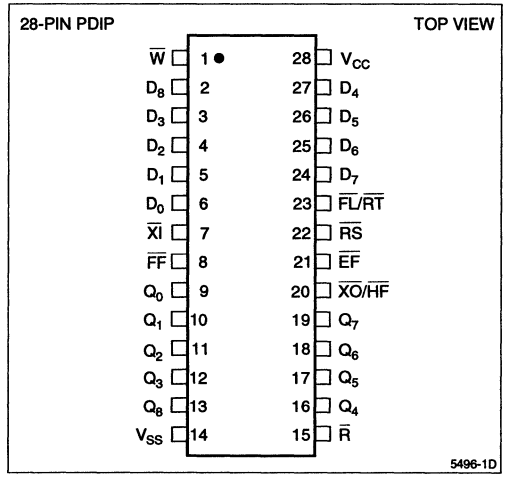


Figure 1. Pin Connections for PDIP Packages

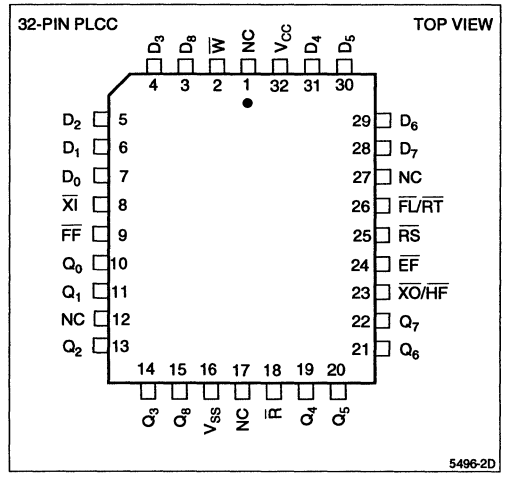


Figure 2. Pin Connections for PLCC Package

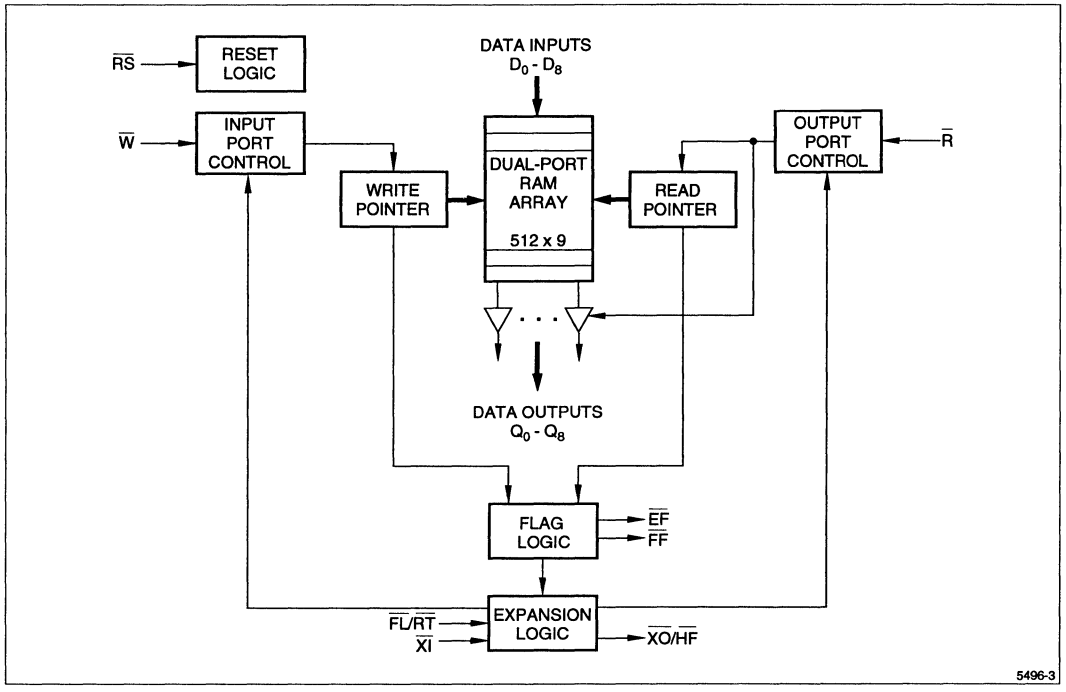


Figure 3. LH5496/96H Block Diagram

PIN DESCRIPTIONS

PIN	PIN TYPE *	DESCRIPTION
$D_0 - D_8$	I	Input Data Bus
$Q_0 - Q_8$	O/Z	Output Data Bus
$\overline{W}$	I	Write Request
$\overline{R}$	I	Read Request
$\overline{EF}$	O	Empty Flag
$\overline{FF}$	O	Full Flag

PIN	PIN TYPE *	DESCRIPTION
$\overline{XO}/\overline{HF}$	O	Expansion Out/Half-Full Flag
$\overline{XI}$	I	Expansion In
$\overline{FL}/\overline{RT}$	I	First Load/Retransmit
$\overline{RS}$	I	Reset
V_{CC}	V	Positive Power Supply
V_{SS}	V	Ground

* I = Input, O = Output, Z = High-Impedance, V = Power Voltage Level

ABSOLUTE MAXIMUM RATINGS [1]

PARAMETER	RATING
Supply Voltage to V_{SS} Potential	−0.5 V to 7 V
Signal Pin Voltage to V_{SS} Potential [3]	−0.5 V to V_{CC} + 0.5 V (not to exceed 7 V)
DC Output Current [2]	± 50 mA
Storage Temperature Range	−65°C to 150°C
Power Dissipation (Package Limit)	1.0 W
DC Voltage Applied To Outputs In High-Z State	−0.5 V to Vcc + 0.5 V (not to exceed 7 V)

NOTES:

1. Stresses greater than those listed under 'Absolute Maximum Ratings' may cause permanent damage to the device. This is a device stress rating for transient conditions only. Functional operation at these or any other conditions above those indicated in the 'Operating Range' of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Outputs should not be shorted for more than 30 seconds. No more than one output should be shorted at any time.
3. Negative undershoots of 1.5 V in amplitude are permitted for up to 10 ns once per cycle.

OPERATING RANGE

SYMBOL	PARAMETER	MIN	MAX	UNIT
T_A	Temperature, Ambient, LH5496	0	70	°C
T_{AH}	Temperature, Ambient, LH5496H	−40	85	°C
V_{CC}	Supply Voltage	4.5	5.5	V
V_{SS}	Supply Voltage	0	0	V
V_{IL}	Logic '0' Input Voltage [1]	−0.5	0.8	V
V_{IH}	Logic '1' Input Voltage	2.0	V_{CC} + 0.5	V

NOTE:

1. Negative undershoots of 1.5 V in amplitude are permitted for up to 10 ns once per cycle.

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
I_{LI}	Input Leakage Current	V_{CC} = 5.5 V, V_{IN} = 0 V to V_{CC}	−10	10	µA
I_{LO}	Output Leakage Current	$\overline{R} \geq V_{IH}$, 0 V ≤ V_{OUT} ≤ V_{CC}	−10	10	µA
V_{OH}	Output High Voltage	I_{OH} = −2.0 mA	2.4		V
V_{OL}	Output Low Voltage	I_{OL} = 8.0 mA		0.4	V
I_{CC}	Average Supply Current [1]	Measured at f = 40 MHz		100	mA
I_{CC2}	Average Standby Current [1]	All Inputs = V_{IH}		15	mA
I_{CC3}	Power Down Current [1]	All Inputs = V_{CC} − 0.2 V		5	mA

NOTE:

1. I_{CC}, I_{CC2}, and I_{CC3} are dependent upon actual output loading and cycle rates. Specified values are with outputs open.

AC TEST CONDITIONS

PARAMETER	RATING
Input Pulse Levels	V_{SS} to 3 V
Input Rise and Fall Times (10% to 90%)	5 ns
Input Timing Reference Levels	1.5 V
Output Reference Levels	1.5 V
Output Load, Timing Tests	Figure 4

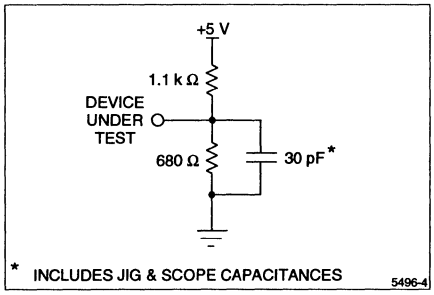


Figure 4. Output Load Circuit

CAPACITANCE [1,2]

PARAMETER	RATING
C_{IN} (Input Capacitance)	5 pF
C_{OUT} (Output Capacitance)	7 pF

NOTES:

1. Sample tested only.
2. Capacitances are maximum values at 25°C measured at 1.0 MHz with V_{IN} = 0 V.

AC ELECTRICAL CHARACTERISTICS [1] (Over Operating Range)

SYMBOL	PARAMETER	t_A = 15 ns [5]		t_A = 20 ns		t_A = 25 ns		t_A = 35 ns		t_A = 50 ns		t_A = 65 ns		t_A = 80 ns		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
READ CYCLE TIMING																
t_{RC}	Read Cycle Time	25	–	30	–	35	–	45	–	65	–	80	–	100	–	ns
t_A	Access Time	–	15	–	20	–	25	–	35	–	50	–	65	–	80	ns
t_{RR}	Read Recover Time	10	–	10	–	10	–	10	–	15	–	15	–	15	–	ns
t_{RPW}	Read Pulse Width [2]	15	–	20	–	25	–	35	–	50	–	65	–	80	–	ns
t_{RLZ}	Data Bus Active from Read LOW [3]	5	–	5	–	5	–	5	–	5	–	5	–	10	–	ns
t_{WLZ}	Data Bus Active from Write HIGH [3,4]	10	–	10	–	10	–	10	–	10	–	10	–	20	–	ns
t_{DV}	Data Valid from Read Pulse HIGH	5	–	5	–	5	–	5	–	5	–	5	–	5	–	ns
t_{RHZ}	Data Bus High-Z from Read HIGH [3]	–	15	–	15	–	15	–	15	–	20	–	30	–	30	ns
WRITE CYCLE TIMING																
t_{WC}	Write Cycle Time	25	–	30	–	35	–	45	–	65	–	80	–	100	–	ns
t_{WPW}	Write Pulse Width [2]	15	–	20	–	25	–	35	–	50	–	65	–	80	–	ns
t_{WR}	Write Recovery Time	10	–	10	–	10	–	10	–	15	–	15	–	15	–	ns
t_{DS}	Data Setup Time	10	–	10	–	10	–	15	–	20	–	20	–	20	–	ns
t_{DH}	Data Hold Time	0	–	0	–	0	–	0	–	0	–	5	–	5	–	ns
RESET TIMING																
t_{RSC}	Reset Cycle Time	25	–	30	–	35	–	45	–	65	–	80	–	100	–	ns
t_{RS}	Reset Pulse Width [2]	15	–	20	–	25	–	35	–	50	–	65	–	80	–	ns
t_{RSR}	Reset Recovery Time	10	–	10	–	10	–	10	–	15	–	15	–	15	–	ns
t_{RRSS}	Read HIGH to $\overline{RS}$ HIGH	15	–	20	–	25	–	35	–	50	–	65	–	80	–	ns
t_{WRSS}	Write HIGH to $\overline{RS}$ HIGH	15	–	20	–	25	–	35	–	50	–	65	–	80	–	ns
RETRANSMIT TIMING																
t_{RTC}	Retransmit Cycle Time	25	–	30	–	35	–	45	–	65	–	80	–	100	–	ns
t_{RT}	Retransmit Pulse Width [2]	15	–	20	–	25	–	35	–	50	–	65	–	80	–	ns
t_{RTR}	Retransmit Recovery Time	10	–	10	–	10	–	10	–	15	–	15	–	15	–	ns
FLAG TIMING																
t_{EFL}	Reset LOW to Empty Flag LOW	–	25	–	30	–	35	–	45	–	65	–	80	–	100	ns
$t_{HFH,FFH}$	Reset LOW to Half-Full and Full Flags HIGH	–	25	–	30	–	35	–	45	–	65	–	80	–	100	ns
t_{REF}	Read LOW to Empty Flag LOW	–	20	–	25	–	25	–	35	–	45	–	60	–	60	ns
t_{RFF}	Read HIGH to Full Flag HIGH	–	20	–	25	–	25	–	35	–	45	–	60	–	60	ns
t_{WEF}	Write HIGH to Empty Flag HIGH	–	20	–	25	–	25	–	35	–	45	–	60	–	60	ns
t_{WFF}	Write LOW to Full Flag LOW	–	20	–	25	–	25	–	35	–	45	–	60	–	60	ns
t_{WHF}	Write LOW to Half-Full Flag LOW	–	25	–	30	–	35	–	45	–	65	–	80	–	100	ns
t_{RHF}	Read HIGH to Half-Full Flag HIGH	–	25	–	30	–	35	–	45	–	65	–	80	–	100	ns
EXPANSION TIMING																
t_{XOL}	Expansion Out LOW	–	18	–	20	–	25	–	35	–	50	–	65	–	80	ns
t_{XOH}	Expansion Out HIGH	–	18	–	20	–	25	–	35	–	50	–	65	–	80	ns
t_{XI}	Expansion In Pulse Width	15	–	20	–	25	–	35	–	50	–	65	–	80	–	ns
t_{XIR}	Expansion In Recovery Time	10	–	10	–	10	–	10	–	10	–	10	–	10	–	ns
t_{XIS}	Expansion in Setup Time	7	–	10	–	10	–	15	–	15	–	15	–	15	–	ns

NOTES:

1. All timing measurements performed at 'AC Test Condition' levels.
2. Pulse widths less than minimum value are not allowed.
3. Values guaranteed by design not currently tested.
4. Only applies to read data flow-through mode.
5. LH5496 only.

OPERATIONAL DESCRIPTION

Reset

The device is reset whenever the Reset pin ($\overline{RS}$) is taken to a LOW state. The reset operation initializes both the read and write address pointers to the first memory location. The $\overline{XI}$ and $\overline{FL}$ pins are also sampled at this time to determine whether the device is in Single mode or Depth Expansion mode. A reset pulse is required when the device is first powered up. The Read ($\overline{R}$) and Write ($\overline{W}$) pins may be in any state when reset is initiated, but must be brought to a HIGH state t_{RPW} and t_{WPW} before the rising edge of $\overline{RS}$.

Write

A write cycle is initiated on the falling edge of the Write ($\overline{W}$) pin. Data setup and hold times must be observed on the data in (D_0 – D_8) pins. A write operation is only possible if the FIFO is not full, (i.e. the Full flag pin is HIGH). Writes may occur independently of any ongoing read opertations.

At the falling edge of the first write after the memory is half filled, the Half-Full flag will be asserted ($\overline{HF}$ = LOW) and will remain asserted until the difference between the write pointer and read pointer indicates that the remaining data in the device is less than or equal to one half the total capacity of the FIFO. The Half-Full flag is deasserted ($\overline{HF}$ = HIGH) by the appropriate rising edge of $\overline{R}$.

The Full flag is asserted ($\overline{FF}$ = LOW) at the falling edge of the write operation which fills the last available location in the FIFO memory array. The Full flag will inhibit further writes until cleared by a valid read. The Full flag is deasserted ($\overline{FF}$ = HIGH) after the next rising edge of $\overline{R}$ releases another memory location.

Read

A read cycle is initiated on the falling edge of the Read ($\overline{R}$) pin. Read data becomes valid on the data out (Q_0–Q_8) pins after a time t_A from the falling edge of $\overline{R}$. After $\overline{R}$ goes HIGH, the data out pins return to a high-impedance state. Reads may occur independent of any ongoing write operations. A read is only possible if the FIFO is not empty ($\overline{EF}$ = HIGH).

The internal read and write address pointers are maintained by the device such that consecutive read operations will access data in the same order as it was written. The Empty flag is asserted ($\overline{EF}$ = LOW) after the falling edge of $\overline{R}$ which accesses the last available data in the FIFO memory. $\overline{EF}$ is deasserted ($\overline{EF}$ = HIGH) after the next rising edge of $\overline{W}$ loads another word of valid data.

Data Flow-Through

Read flow-through mode occurs when the Read ($\overline{R}$) pin is brought LOW while the FIFO is empty, and held LOW in anticipation of a write cycle. At the end of the next write cycle, the Empty flag will be momentarily deasserted, and the data just written will become available on the data out pins after a maximum time of $t_{WEF} + t_A$. Additional writes may occur while the $\overline{R}$ pin remains LOW, but only data from the first write flows through to the outputs. Additional data, if any, can only be accessed by toggling $\overline{R}$.

Write flow-through mode occurs when the Write ($\overline{W}$) pin is brought LOW while the FIFO is full, and held LOW in anticipation of a read cycle. At the end of the read cycle, the Full flag will be momentarily deasserted, but then immediately reasserted in response to $\overline{W}$ held LOW. Data is written into the FIFO on the rising edge of $\overline{W}$ which may occur $t_{RFF} + t_{WPW}$ after the read.

Retransmit

The FIFO can be made to reread previously read data through the retransmit function. Retransmit is initiated by pulsing $\overline{RT}$ LOW. This resets the internal read address pointer to the first physical location in the memory while leaving the internal write address pointer unchanged. Data between the read and write pointers may be reaccessed by subsequent reads. Both $\overline{R}$ and $\overline{W}$ must be inactive (HIGH) during the retransmit pulse. Retransmit is useful if no more than 512 writes are performed between resets. Retransmit may affect the status of $\overline{EF}$, $\overline{HF}$, and $\overline{FF}$ flags, depending on the relocation of the read pointer. This function is not available in depth expansion mode.

TIMING DIAGRAMS

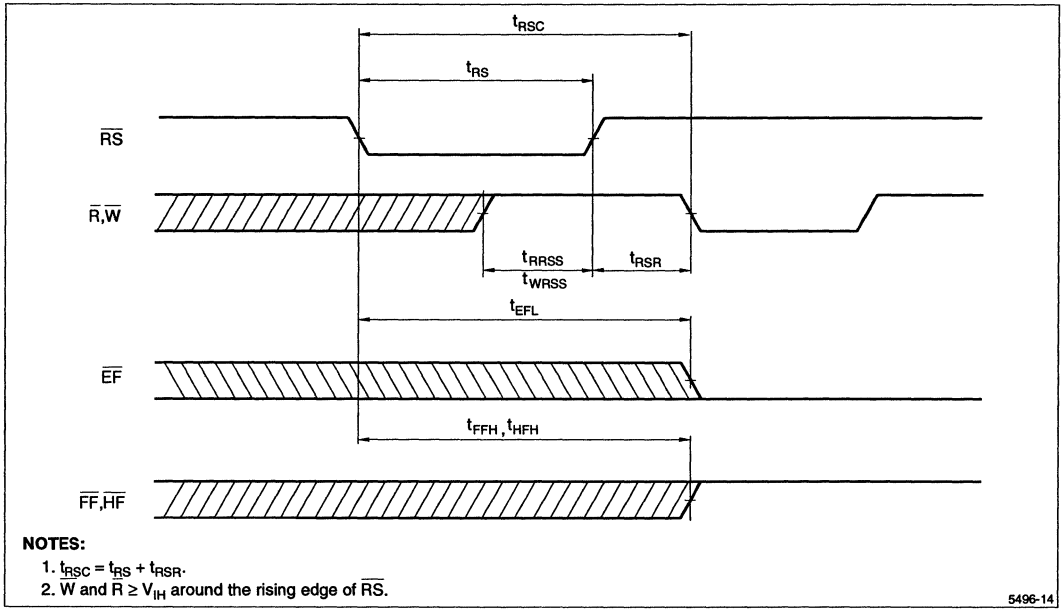


Figure 5. Reset Timing

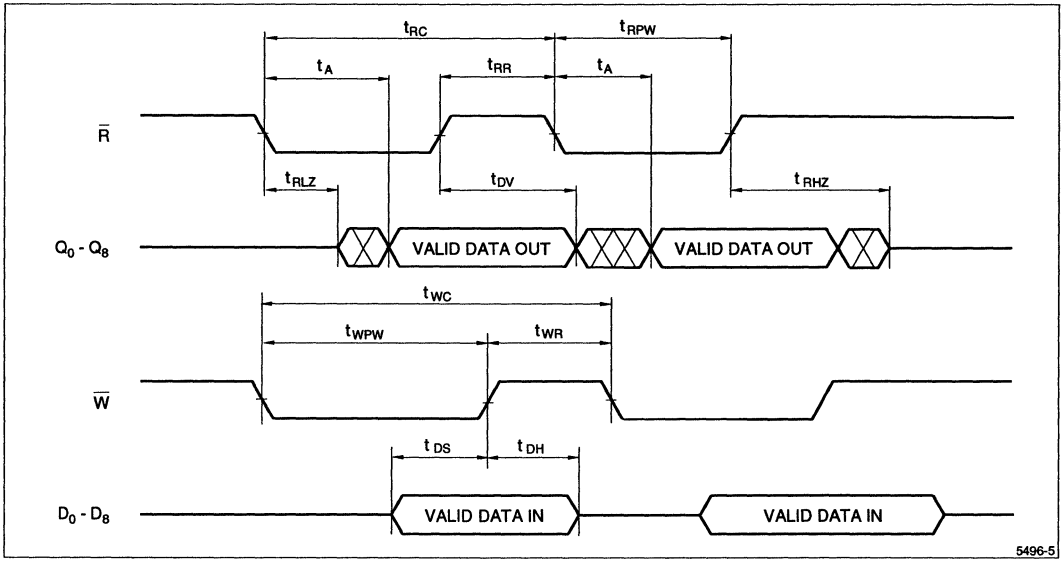


Figure 6. Asynchronous Write and Read Operation

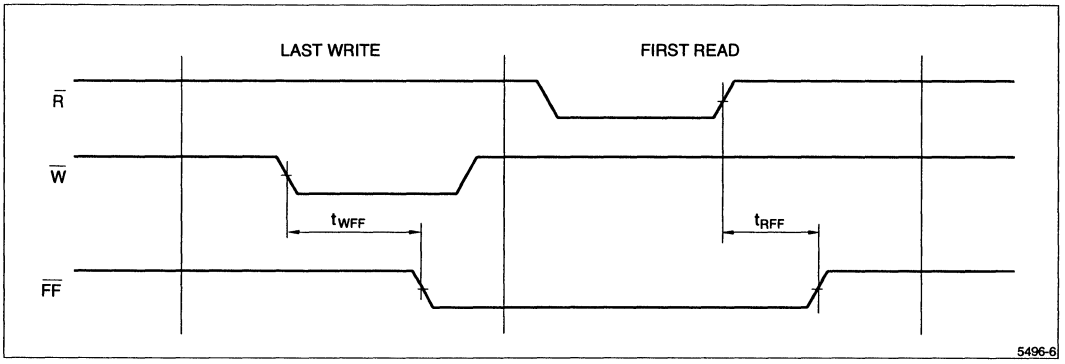


Figure 7. Full Flag from Last Write to First Read

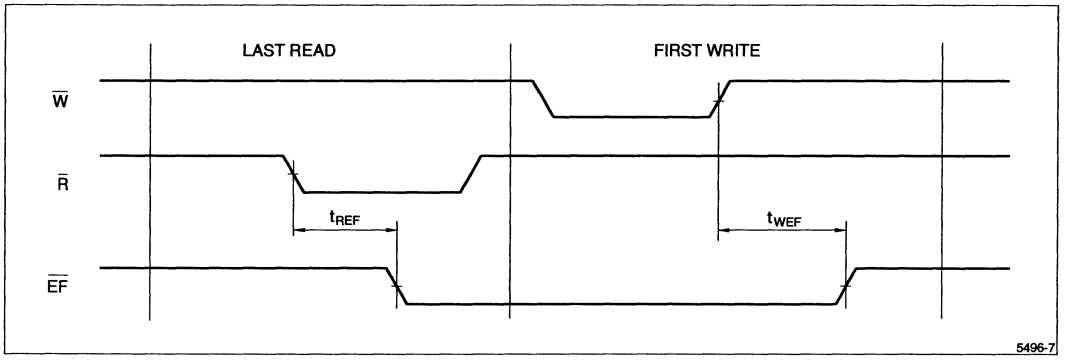


Figure 8. Empty Flag from Last Read to First Write

TIMING DIAGRAMS (cont'd)

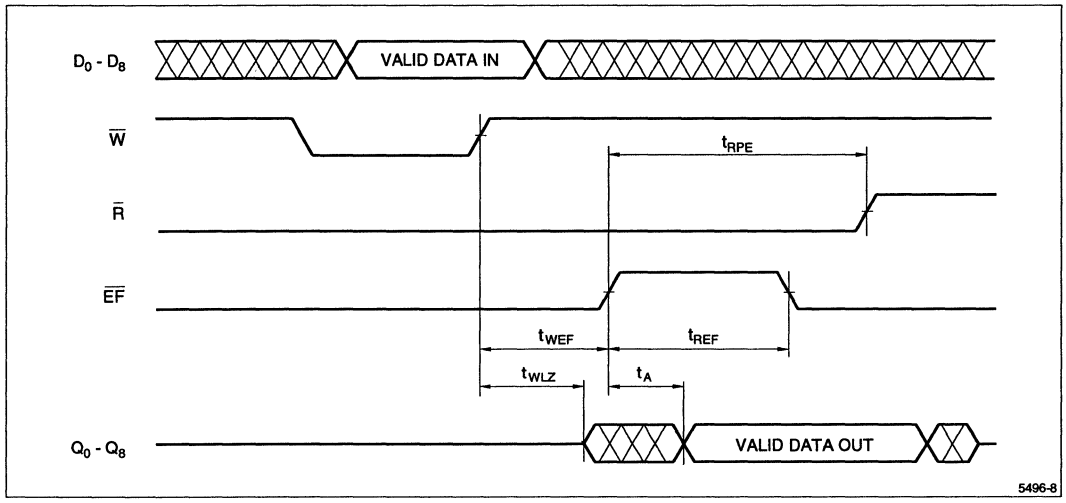


Figure 9. Read Data Flow-Through

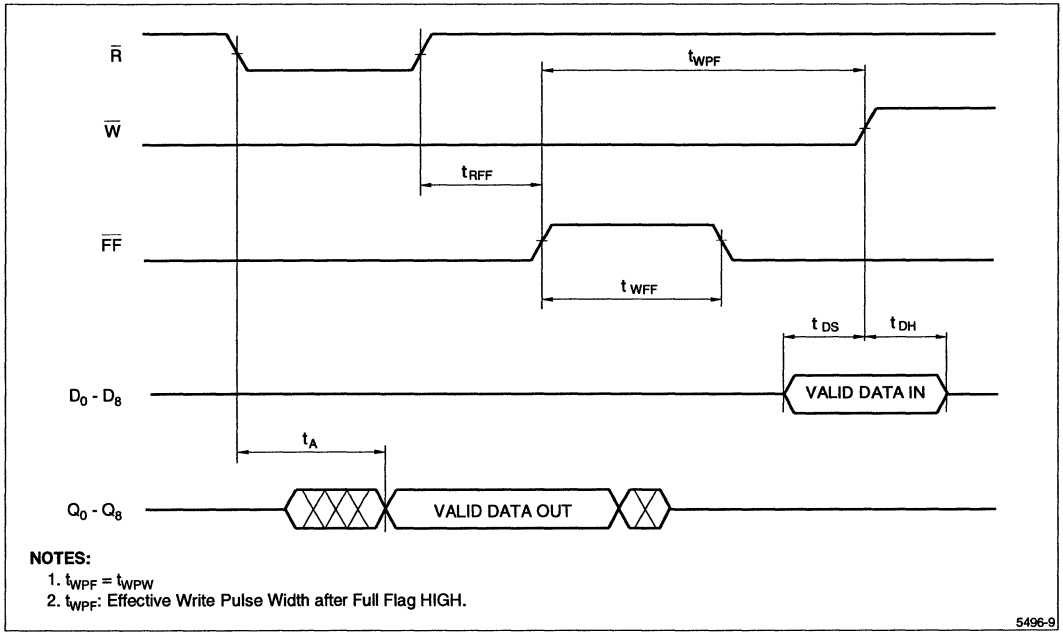


Figure 10. Write Data Flow-Through

TIMING DIAGRAMS (cont'd)

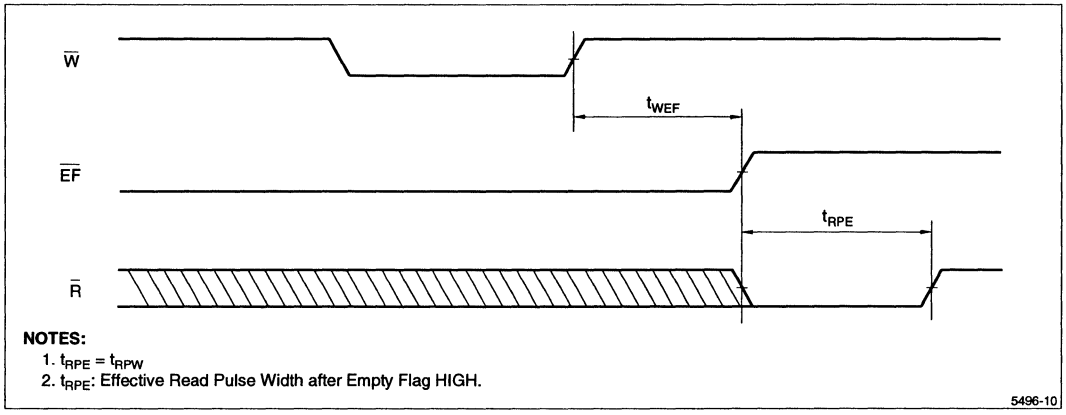


Figure 11. Empty Flag Timing

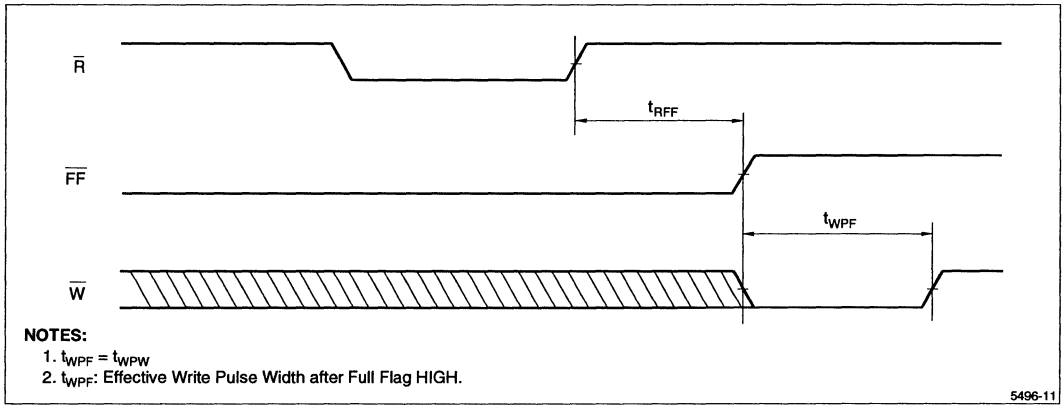


Figure 12. Full Flag Timing

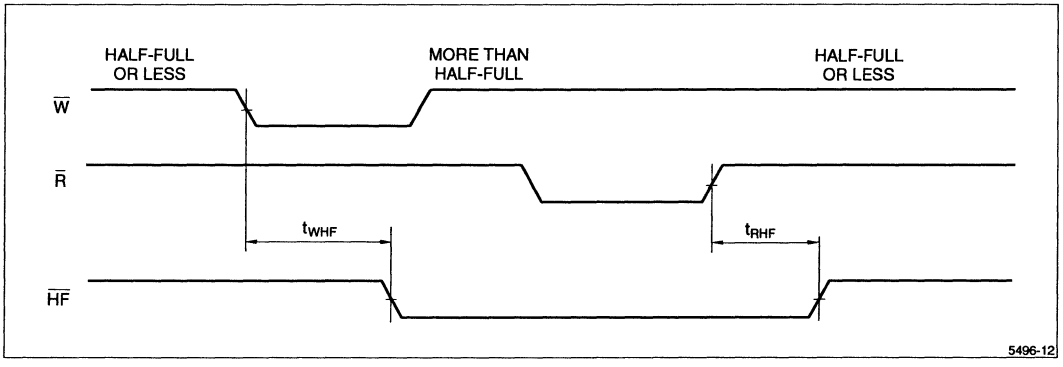


Figure 13. Half-Full Flag Timing

TIMING DIAGRAMS (cont'd)

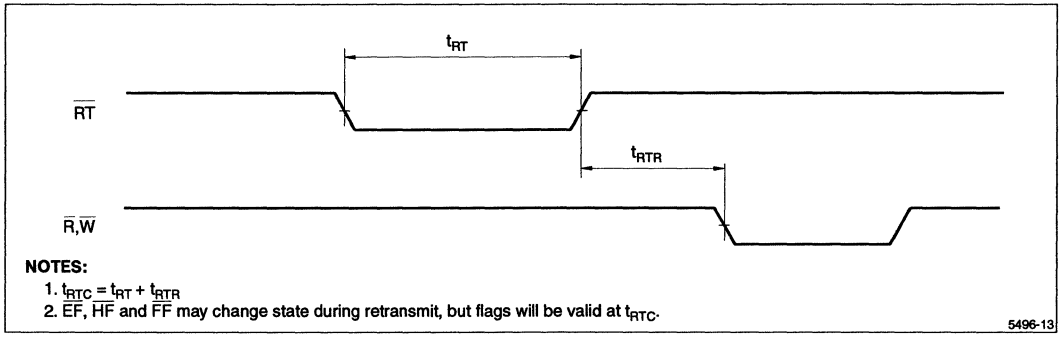


Figure 14. Retransmit Timing

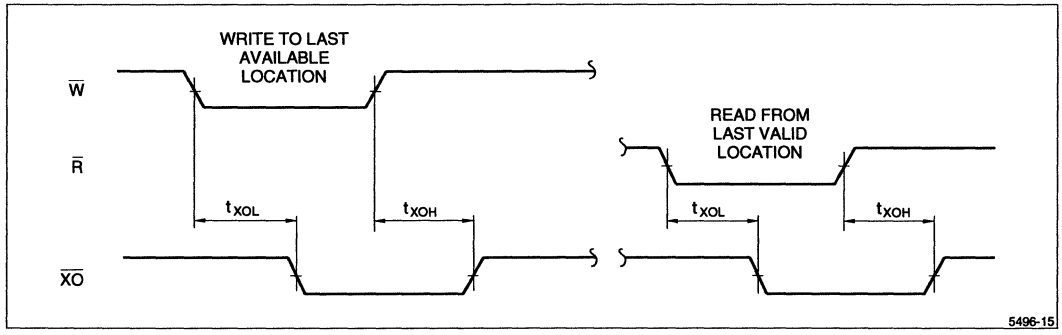


Figure 15. Expansion Out Timing

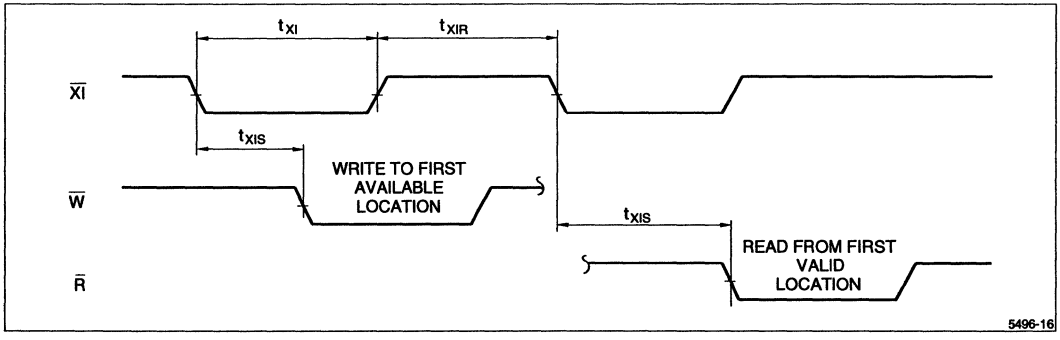


Figure 16. Expansion In Timing

OPERATIONAL MODES

Single Device Configuration

When depth expansion is not required for the given application, the device is placed in Single mode by tying the Expansion In pin ($\overline{XI}$) to ground. This pin is internally sampled during reset.

Width Expansion

Word-width expansion is implemented by placing multiple LH5496/96H devices in parallel. Each LH5496/96H should be configured for standalone mode. In this arrangement, the behavior of the status flags is identical for all devices; so, in principle, a representative value for each of these flags could be derived from any one device. In practice, it is better to derive 'composite' flag values using external logic, since there may be minor speed variations between different actual devices. (See Figures 17 and 18.)

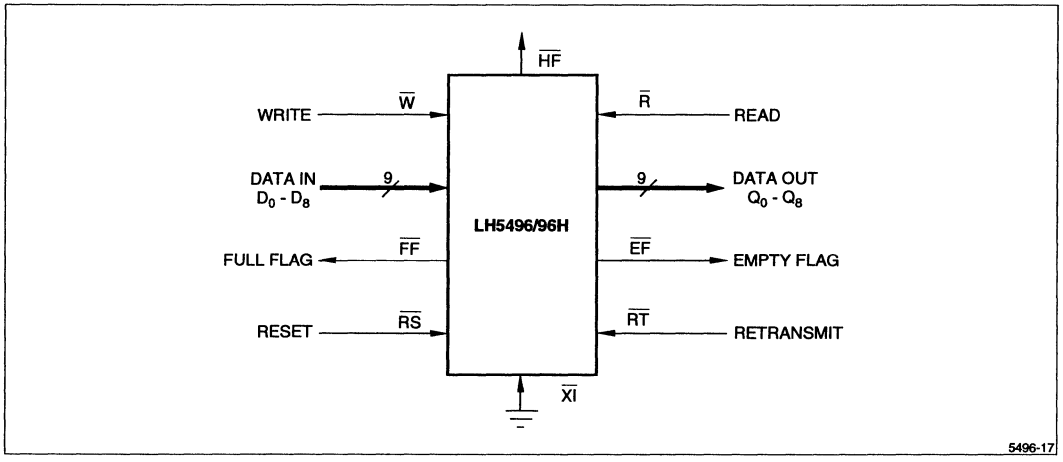


Figure 17. Single FIFO (512 × 9)

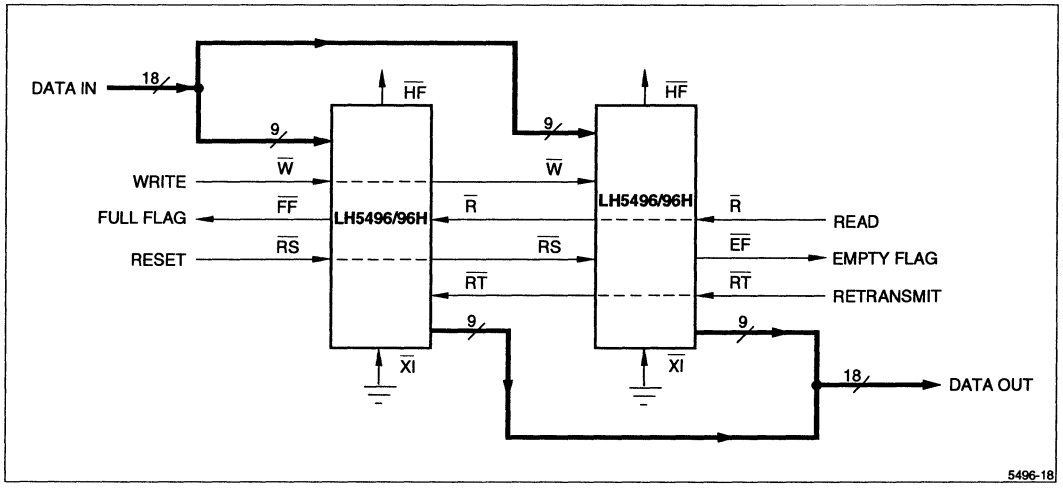


Figure 18. FIFO Width Expansion (512 × 18)

OPERATIONAL MODES (cont'd)

Depth Expansion

Depth expansion is implemented by configuring the required number of FIFOs in Expansion mode. In this arrangement, the FIFOs are connected in a circular fashion with the Expansion Out pin ($\overline{XO}$) of each device tied to the Expansion In pin ($\overline{XI}$) of the next device. One FIFO in this group must be designated as the first load device. This is accomplished by tying the First Load pin ($\overline{FL}$) of this device to ground. All other devices must have their $\overline{FL}$ pin tied to a high level. In this mode, $\overline{W}$ and $\overline{R}$ signals are shared by all devices, while internal logic controls the steering of data. Only one FIFO will be enabled for any given read cycle, so the common Data Out pins of all devices are wire-ORed together. Likewise, the common Data In pins of all devices are tied together.

In Expansion mode, external logic is required to generate a composite Full or Empty flag. This is achieved by ORing the $\overline{FF}$ pins of all devices and ORing the $\overline{EF}$ pins of all devices respectively. The Half-Full flag and Retransmit functions are not available in Depth Expansion mode.

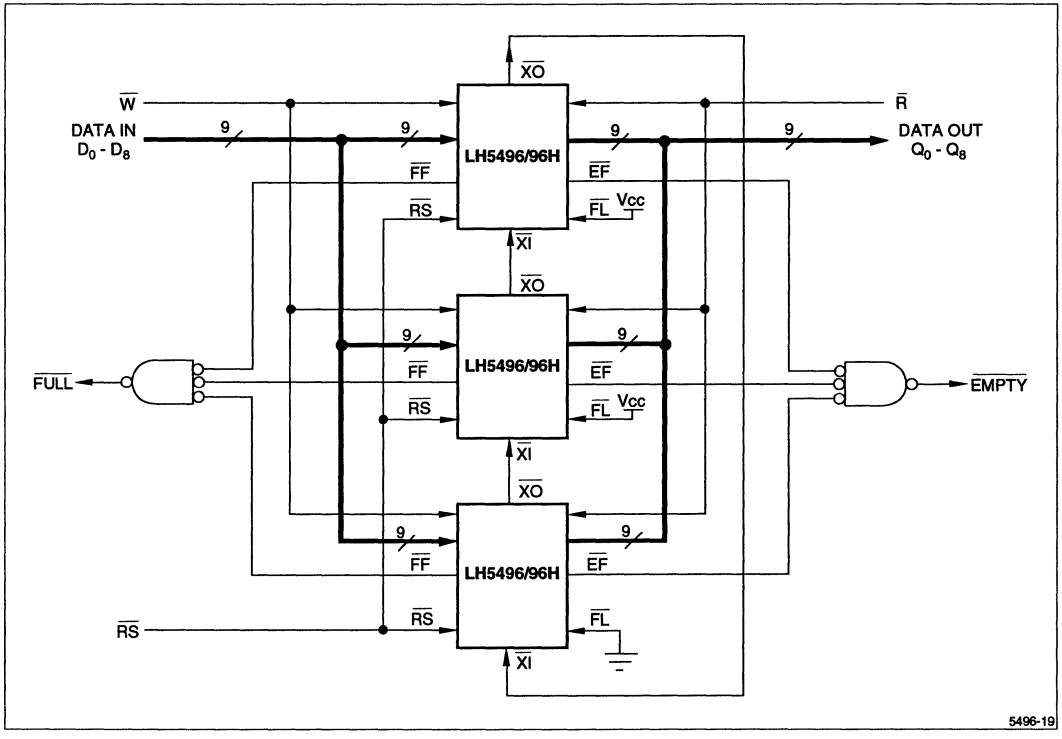


Figure 19. FIFO Depth Expansion (1536 × 9)

OPERATIONAL MODES (cont'd)

Compound Expansion

A combination of width and depth expansion can be easily implemented by operating groups of depth expanded FIFOs in parallel.

Bidirectional Operation

Applications which require bidirectional data buffering between two systems can be realized by operating LH5496/96H devices in parallel but opposite directions. The Data In pins of a device may be tied to the corresponding Data Out pins of another device operating in the opposite direction to form a single bidirectional bus interface. Care must be taken to assure that the appropriate read, write, and flag signals are routed to each system. Both depth and width expansion may be used in this configuration.

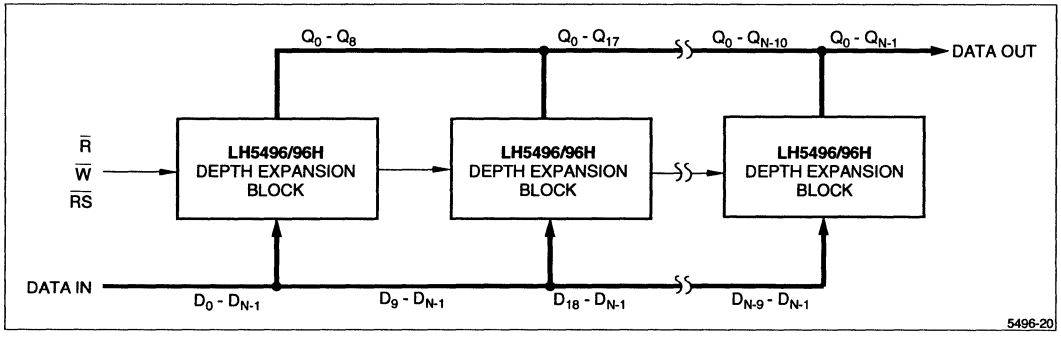


Figure 20. Compound FIFO Expansion

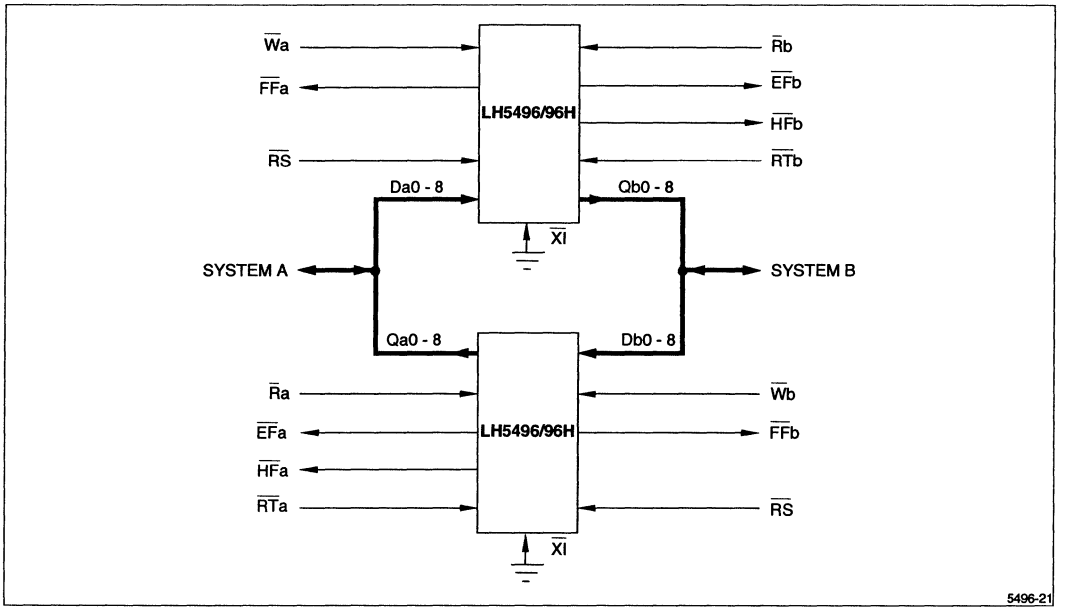
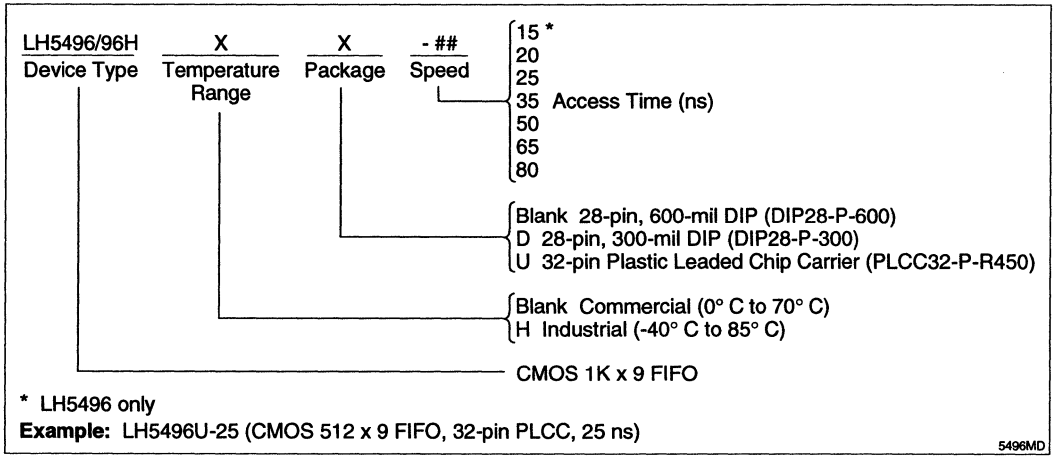


Figure 21. Bidirectional FIFO Buffer

ORDERING INFORMATION



LH5497/97H

CMOS 1K × 9 FIFO

FEATURES

- Fast Access Times:
  15 */20/25/35/50/65/80 ns
- Full CMOS Dual Port Memory Array
- Fully Asynchronous Read and Write
- Expandable in Width and Depth
- Full, Half-Full, and Empty Status Flags
- Read Retransmit Capability
- TTL Compatible I/O
- Packages:
  28-Pin, 300-mil DIP
  28-Pin, 600-mil DIP
  32-Pin PLCC
- Pin and Functionally Compatible with IDT7202

FUNCTIONAL DESCRIPTION

The LH5497/97H are dual port memories with internal addressing to implement a First-In, First-Out algorithm. Through an advanced dual port architecture, they provide fully asynchronous read/write operation. Empty, Full, and Half-Full status flags are provided to prevent data overflow and underflow. In addition, internal logic is provided for unlimited expansion in both word size and depth.

Read and Write operations automatically access sequential locations in memory in such a way that data is read out in the same order that it was written, that is on a First-In, First-Out basis. Since the address sequence is internally predefined, no external address information is required for the operation of this device. A ninth data bit is provided for parity or control information often needed in communication applications.

Empty, Full, and Half-Full status flags monitor the extent to which data has been written into the FIFO, and prevent improper operations (i.e. Read if the FIFO is empty, or Write if the FIFO is full). A retransmit feature resets the Read address pointer to its initial position, thereby allowing repetitive readout of the same data. Expansion In and Expansion Out pins implement an expansion scheme that allows individual FIFOs to be cascaded to greater depth without incurring additional latency (bubblethrough) delays.

* LH5497 only.

PIN CONNECTIONS

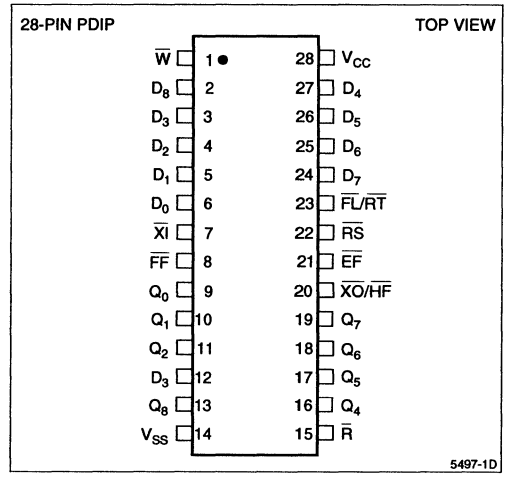


Figure 1. Pin Connections for DIP Packages

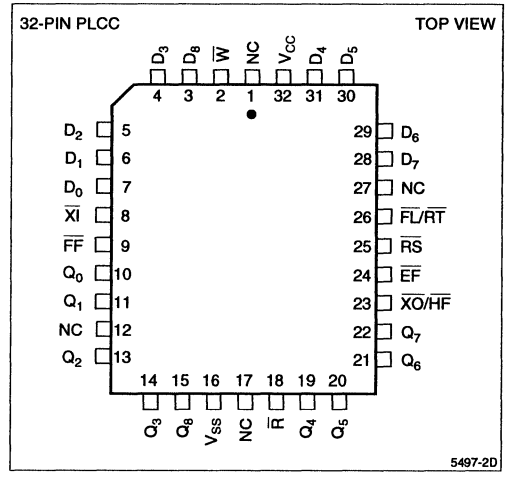


Figure 2. Pin Connections for PLCC Package

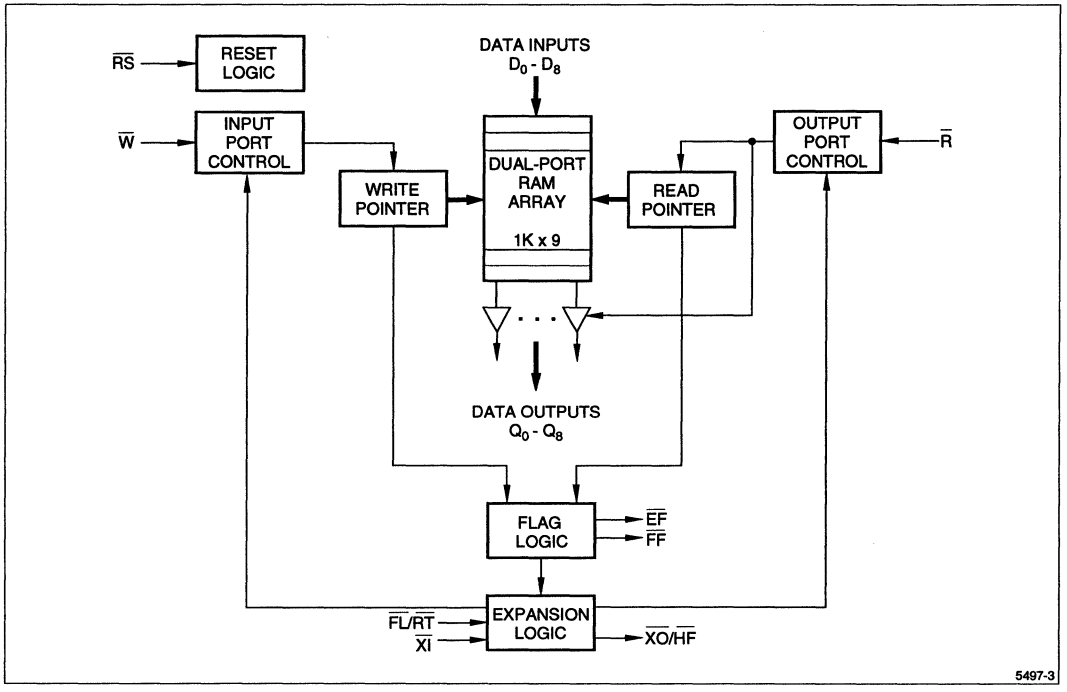


Figure 3. LH5497/97H Block Diagram

PIN DESCRIPTIONS

PIN	PIN TYPE *	DESCRIPTION
$D_0 - D_8$	I	Input Data Bus
$Q_0 - Q_8$	O/Z	Output Data Bus
$\overline{W}$	I	Write Request
$\overline{R}$	I	Read Request
$\overline{EF}$	O	Empty Flag
$\overline{FF}$	O	Full Flag

PIN	PIN TYPE *	DESCRIPTION
$\overline{XO}/\overline{HF}$	O	Expansion Out/Half-Full Flag
$\overline{XI}$	I	Expansion In
$\overline{FL}/\overline{RT}$	I	First Load/Retransmit
$\overline{RS}$	I	Reset
V_{CC}	V	Positive Power Supply
V_{SS}	V	Ground

* I = Input, O = Output, Z = High-Impedance, V = Power Voltage Level

ABSOLUTE MAXIMUM RATINGS [1]

PARAMETER	RATING
Supply Voltage to V_{SS} Potential	−0.5 V to 7 V
Signal Pin Voltage to V_{SS} Potential [3]	−0.5 V to V_{CC} + 0.5 V (not to exceed 7 V)
DC Output Current [2]	± 50 mA
Storage Temperature Range	−65°C to 150°C
Power Dissipation (Package Limit)	1.0 W
DC Voltage Applied to Outputs in High-Z State	−0.5 V to V_{CC} + 0.5 V (not to exceed 7 V)

NOTES:

1. Stresses greater than those listed under 'Absolute Maximum Ratings' may cause permanent damage to the device. This is a stress rating for transient conditions only. Functional operation of the device at these or any other conditions above those indicated in the 'Operating Range' of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Outputs should not be shorted for more than 30 seconds. No more than one output should be shorted at any time.
3. Negative undershoots of 1.5 V in amplitude are permitted for up to 10 ns once per cycle.

OPERATING RANGE

SYMBOL	PARAMETER	MIN	MAX	UNIT
T_A	Temperature, Ambient, LH5497	0	70	°C
T_{AH}	Temperature, Ambient, LH5497H	−40	85	°C
V_{CC}	Supply Voltage	4.5	5.5	V
V_{SS}	Supply Voltage	0	0	V
V_{IL}	Logic '0' Input Voltage[1]	−0.5	0.8	V
V_{IH}	Logic '1' Input Voltage	2.0	V_{CC} + 0.5	V

NOTE:

1. Negative undershoots of 1.5 V in amplitude are permitted for up to 10 ns once per cycle.

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
I_{LI}	Input Leakage Current	V_{CC} = 5.5 V, V_{IN} = 0 V to V_{CC}	−10	10	µA
I_{LO}	Output Leakage Current	$\overline{R} \geq V_{IH}$, 0 V ≤ V_{OUT} ≤ V_{CC}	−10	10	µA
V_{OH}	Output High Voltage	I_{OH} = −2.0 mA	2.4	—	V
V_{OL}	Output Low Voltage	I_{OL} = 8.0 mA	—	0.4	V
I_{CC}	Average Supply Current [1]	Measured at f = 40MHz	—	100	mA
I_{CC2}	Average Standby Current [1]	All Inputs = V_{IH}	—	15	mA
I_{CC3}	Power Down Current [1]	All Inputs = V_{CC} − 0.2V	—	5	mA

NOTE:

1. I_{CC}, I_{CC2}, and I_{CC3} are dependent upon actual output loading and cycle rates. Specified values are with outputs open.

AC TEST CONDITIONS

PARAMETER	RATING
Input Pulse Levels	V_{SS} to 3 V
Input Rise and Fall Times (10% to 90%)	5 ns
Input Timing Reference Levels	1.5 V
Output Reference Levels	1.5 V
Output Load, Timing Tests	Figure 4

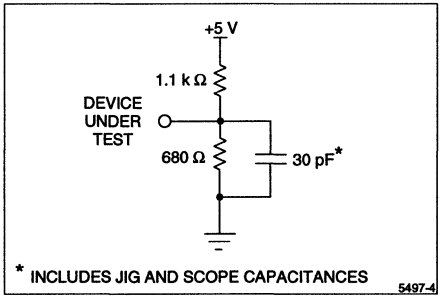


Figure 4. Output Load Circuit

CAPACITANCE [1,2]

PARAMETER	RATING
C_{IN} (Input Capacitance)	5 pF
C_{OUT} (Output Capacitance)	7 pF

NOTES:

1. Sample tested only.
2. Capacitances are maximum values at 25°C measured at 1.0 MHz with V_{IN} = 0 V.

AC ELECTRICAL CHARACTERISTICS [1] (Over Operating Range)

SYMBOL	PARAMETER	t_A = 15 ns [5]		t_A = 20 ns		t_A = 25 ns		t_A = 35 ns		t_A = 50 ns		t_A = 65 ns		t_A = 80 ns		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
READ CYCLE TIMING																
t_{RC}	Read Cycle Time	25	–	30	–	35	–	45	–	65	–	80	–	100	–	ns
t_A	Access Time	–	15	–	20	–	25	–	35	–	50	–	65	–	80	ns
t_{RR}	Read Recover Time	10	–	10	–	10	–	10	–	15	–	15	–	15	–	ns
t_{RPW}	Read Pulse Width [2]	15	–	20	–	25	–	35	–	50	–	65	–	80	–	ns
t_{RLZ}	Data Bus Active from Read LOW [3]	5	–	5	–	5	–	5	–	5	–	5	–	10	–	ns
t_{WLZ}	Data Bus Active from Write HIGH [3,4]	10	–	10	–	10	–	10	–	10	–	10	–	20	–	ns
t_{DV}	Data Valid from Read Pulse HIGH	5	–	5	–	5	–	5	–	5	–	5	–	5	–	ns
t_{RHZ}	Data Bus High-Z from Read HIGH [3]	–	15	–	15	–	15	–	15	–	20	–	30	–	30	ns
WRITE CYCLE TIMING																
t_{WC}	Write Cycle Time	25	–	30	–	35	–	45	–	65	–	80	–	100	–	ns
t_{WPW}	Write Pulse Width [2]	15	–	20	–	25	–	35	–	50	–	65	–	80	–	ns
t_{WR}	Write Recovery Time	10	–	10	–	10	–	10	–	15	–	15	–	15	–	ns
t_{DS}	Data Setup Time	10	–	10	–	10	–	15	–	20	–	20	–	20	–	ns
t_{DH}	Data Hold Time	0	–	0	–	0	–	0	–	0	–	5	–	5	–	ns
RESET TIMING																
t_{RSC}	Reset Cycle Time	25	–	30	–	35	–	45	–	65	–	80	–	100	–	ns
t_{RS}	Reset Pulse Width [2]	15	–	20	–	25	–	35	–	50	–	65	–	80	–	ns
t_{RSR}	Reset Recovery Time	10	–	10	–	10	–	10	–	15	–	15	–	15	–	ns
t_{RRSS}	Read HIGH to $\overline{RS}$ HIGH	15	–	20	–	25	–	35	–	50	–	65	–	80	–	ns
t_{WRSS}	Write HIGH to $\overline{RS}$ HIGH	15	–	20	–	25	–	35	–	50	–	65	–	80	–	ns
RETRANSMIT TIMING																
t_{RTC}	Retransmit Cycle Time	25	–	30	–	35	–	45	–	65	–	80	–	100	–	ns
t_{RT}	Retransmit Pulse Width [2]	15	–	20	–	25	–	35	–	50	–	65	–	80	–	ns
t_{RTR}	Retransmit Recovery Time	10	–	10	–	10	–	10	–	15	–	15	–	15	–	ns
FLAG TIMING																
t_{EFL}	Reset LOW to Empty Flag LOW	–	25	–	30	–	35	–	45	–	65	–	80	–	100	ns
$t_{HFH,FFH}$	Reset LOW to Half-Full and Full Flags HIGH	–	25	–	30	–	35	–	45	–	65	–	80	–	100	ns
t_{REF}	Read LOW to Empty Flag LOW	–	20	–	25	–	25	–	35	–	45	–	60	–	60	ns
t_{RFF}	Read HIGH to Full Flag HIGH	–	20	–	25	–	25	–	35	–	45	–	60	–	60	ns
t_{WEF}	Write HIGH to Empty Flag HIGH	–	20	–	25	–	25	–	35	–	45	–	60	–	60	ns
t_{WFF}	Write LOW to Full Flag LOW	–	20	–	25	–	25	–	35	–	45	–	60	–	60	ns
t_{WHF}	Write LOW to Half-Full Flag LOW	–	25	–	30	–	35	–	45	–	65	–	80	–	100	ns
t_{RHF}	Read HIGH to Half-Full Flag HIGH	–	25	–	30	–	35	–	45	–	65	–	80	–	100	ns
EXPANSION TIMING																
t_{XOL}	Expansion Out LOW	–	18	–	20	–	25	–	35	–	50	–	65	–	80	ns
t_{XOH}	Expansion Out HIGH	–	18	–	20	–	25	–	35	–	50	–	65	–	80	ns
t_{XI}	Expansion In Pulse Width	15	–	20	–	25	–	35	–	50	–	65	–	80	–	ns
t_{XIR}	Expansion In Recovery Time	10	–	10	–	10	–	10	–	10	–	10	–	10	–	ns
t_{XIS}	Expansion in Setup Time	7	–	10	–	10	–	15	–	15	–	15	–	15	–	ns

NOTES:

1. All timing measurements performed at 'AC Test Condition' levels.
2. Pulse widths less than minimum value are not allowed.
3. Values guaranteed by design not currently tested.
4. Only applies to read data flow-through mode.
5. LH5497 only.

OPERATIONAL DESCRIPTION

Reset

The device is reset whenever the Reset pin ($\overline{RS}$) is taken to a LOW state. The reset operation initializes both the read and write address pointers to the first memory location. The $\overline{XI}$ and $\overline{FL}$ pins are also sampled at this time to determine whether the device is in Single mode or Depth Expansion mode. A reset pulse is required when the device is first powered up. The Read ($\overline{R}$) and Write ($\overline{W}$) pins may be in any state when reset is initiated, but must be brought to a HIGH state t_{RPW} and t_{WPW} before the rising edge of $\overline{RS}$.

Write

A write cycle is initiated on the falling edge of the Write ($\overline{W}$) pin. Data setup and hold times must be observed on the data in ($D_0 - D_8$) pins. A write operation is only possible if the FIFO is not full, (i.e. the Full flag pin is HIGH). Writes may occur independently of any ongoing read operations.

At the falling edge of the first write after the memory is half filled, the Half-Full flag will be asserted ($\overline{HF}$ = LOW) and will remain asserted until the difference between the write pointer and read pointer indicates that the remaining data in the device is less than or equal to one half the total capacity of the FIFO. The Half-Full flag is deasserted ($\overline{HF}$ = HIGH) by the appropriate rising edge of $\overline{R}$.

The Full flag is asserted ($\overline{FF}$ = LOW) at the falling edge of the write operation which fills the last available location in the FIFO memory array. The Full flag will inhibit further writes until cleared by a valid read. The Full flag is deasserted ($\overline{FF}$ = HIGH) after the next rising edge of $\overline{R}$ releases another memory location.

Read

A read cycle is initiated on the falling edge of the Read ($\overline{R}$) pin. Read data becomes valid on the data out (Q_0–Q_8) pins after a time t_A from the falling edge of $\overline{R}$. After $\overline{R}$ goes HIGH, the data out pins return to a high-impedance state. Reads may occur independent of any ongoing write operations. A read is only possible if the FIFO is not empty ($\overline{EF}$ = HIGH).

The internal read and write address pointers are maintained by the device such that consecutive read operations will access data in the same order as it was written. The Empty flag is asserted ($\overline{EF}$ = LOW) after the falling edge of $\overline{R}$ which accesses the last available data in the FIFO memory. $\overline{EF}$ is deasserted ($\overline{EF}$ = HIGH) after the next rising edge of $\overline{W}$ loads another word of valid data.

Data Flow-Through

Read flow-through mode occurs when the Read ($\overline{R}$) pin is brought LOW while the FIFO is empty, and held LOW in anticipation of a write cycle. At the end of the next write cycle, the Empty flag will be momentarily deasserted, and the data just written will become available on the data out pins after a maximum time of $t_{WEF} + t_A$. Additional writes may occur while the $\overline{R}$ pin remains LOW, but only data from the first write flows through to the outputs. Additional data, if any, can only be accessed by toggling $\overline{R}$.

Write flow-through mode occurs when the Write ($\overline{W}$) pin is brought LOW while the FIFO is full, and held LOW in anticipation of a read cycle. At the end of the read cycle, the Full flag will be momentarily deasserted, but then immediately reasserted in response to $\overline{W}$ held LOW. Data is written into the FIFO on the rising edge of $\overline{W}$ which may occur $t_{RFF} + t_{WPW}$ after the read.

Retransmit

The FIFO can be made to reread previously read data through the retransmit function. Retransmit is initiated by pulsing $\overline{RT}$ LOW. This resets the internal read address pointer to the first physical location in the memory while leaving the internal write address pointer unchanged. Data between the read and write pointers may be reaccessed by subsequent reads. Both $\overline{R}$ and $\overline{W}$ must be inactive (HIGH) during the retransmit pulse. Retransmit is useful if no more than 1024 writes are performed between resets. Retransmit may affect the status of $\overline{EF}$, $\overline{HF}$, and $\overline{FF}$ flags, depending on the relocation of the read pointer. This function is not available in depth expansion mode.

TIMING DIAGRAMS

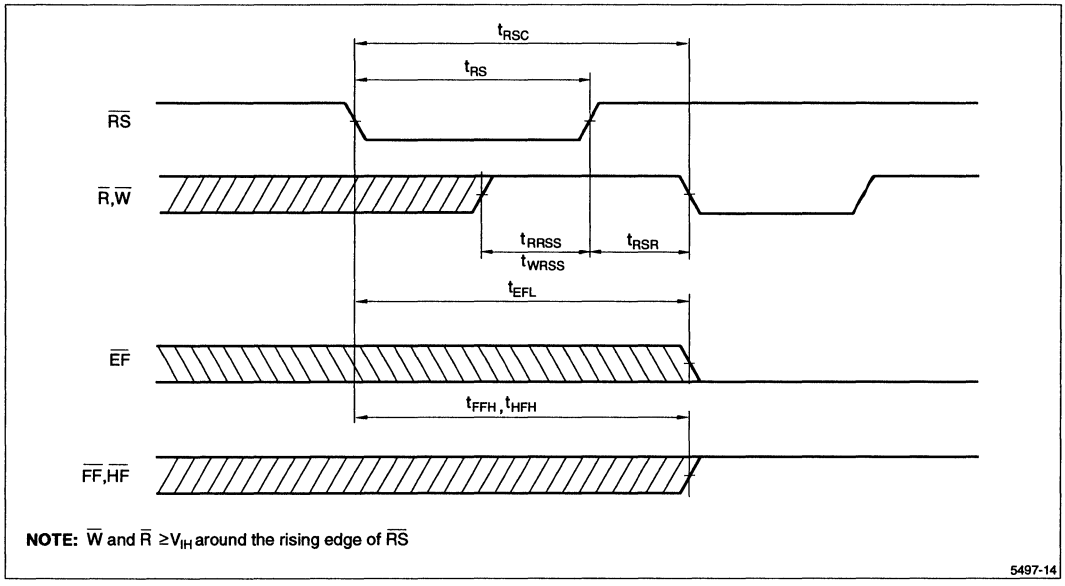


Figure 5. Reset Timing

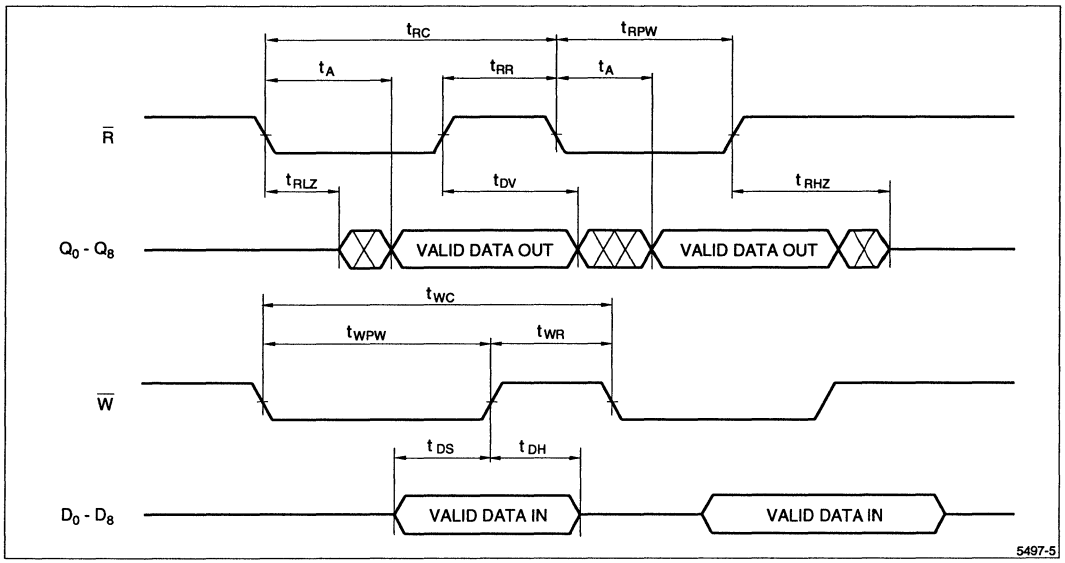


Figure 6. Asynchronous Write and Read Operation

TIMING DIAGRAMS (cont'd)

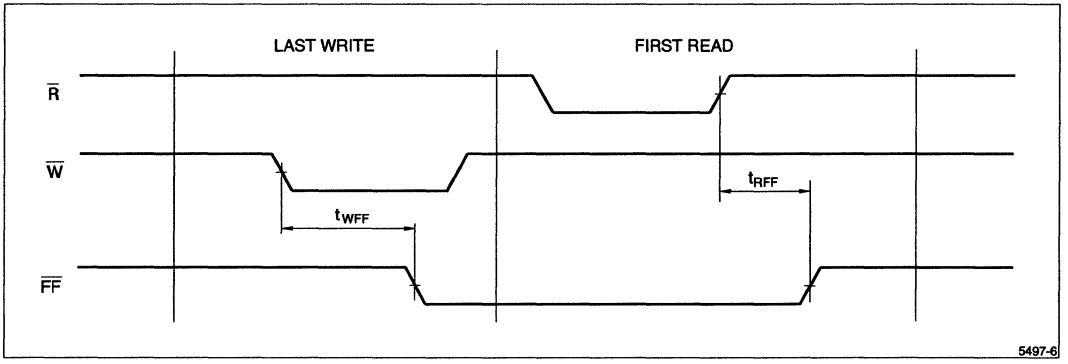


Figure 7. Full Flag from Last Write to First Read

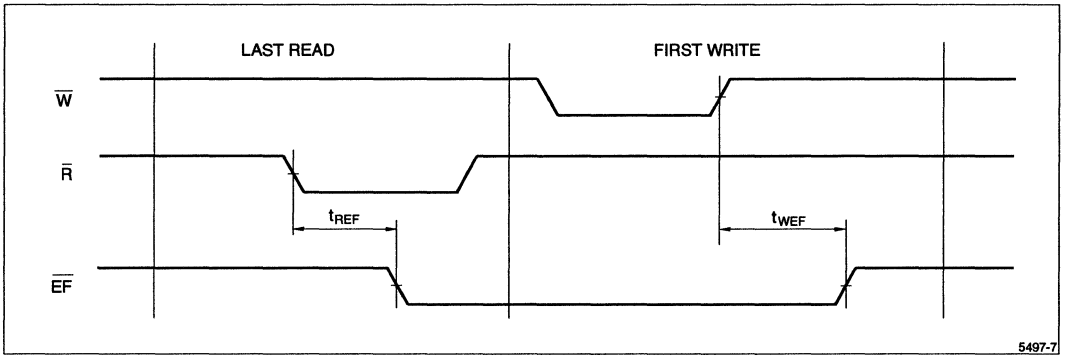


Figure 8. Empty Flag from Last Read to First Write

TIMING DIAGRAMS (cont'd)

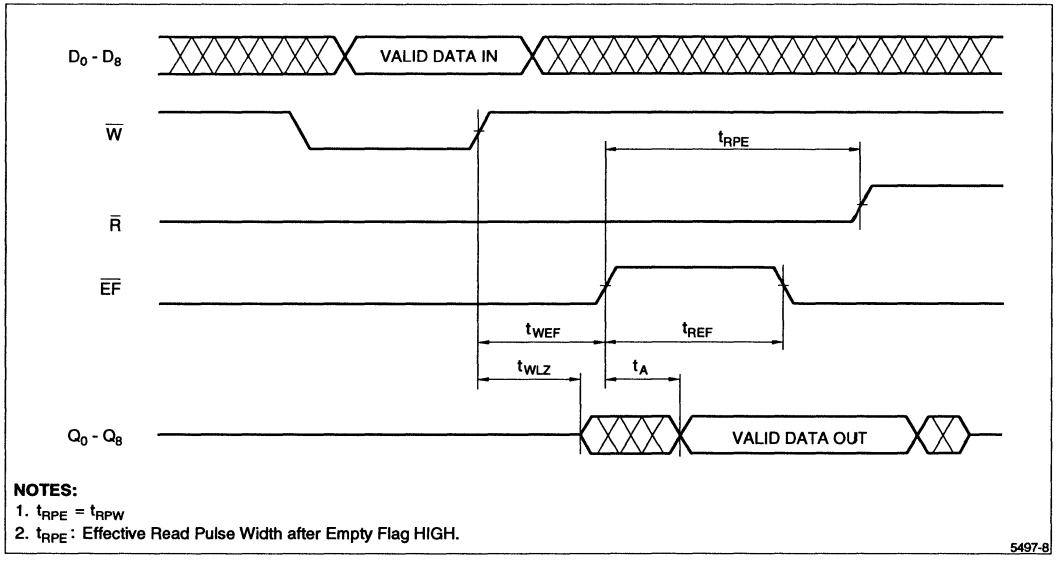


Figure 9. Read Data Flow-Through

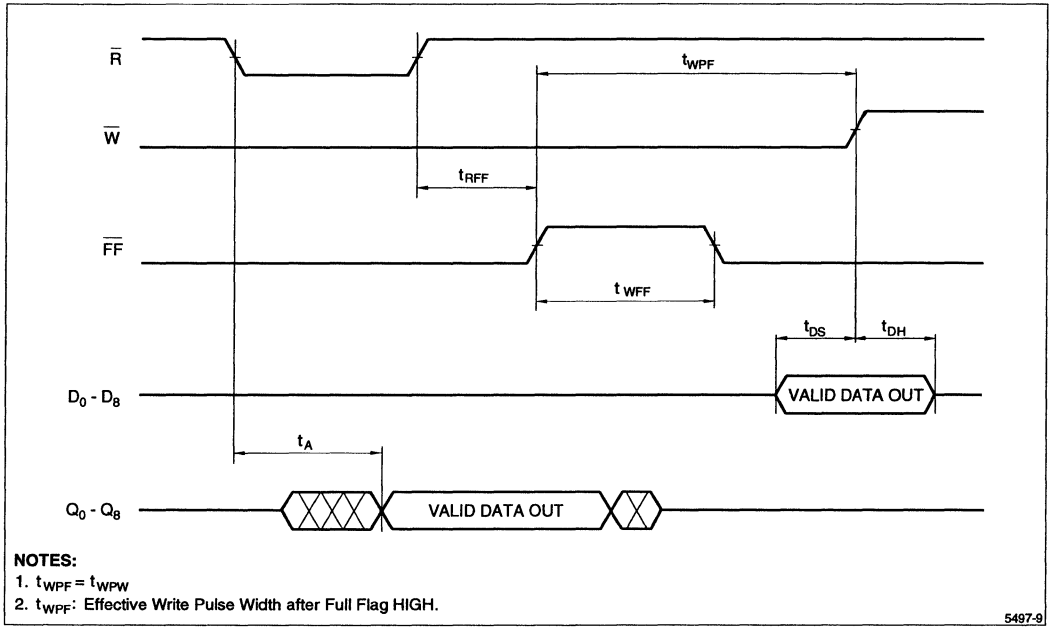


Figure 10. Write Data Flow-Through

TIMING DIAGRAMS (cont'd)

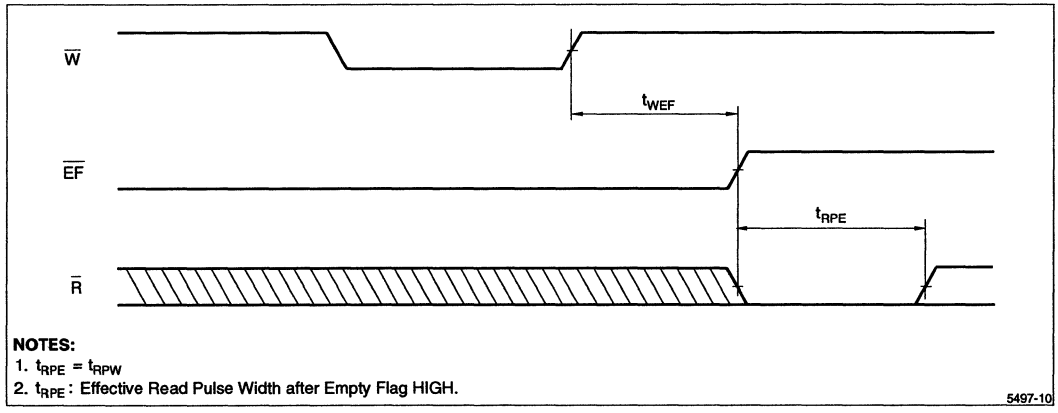


Figure 11. Empty Flag Timing

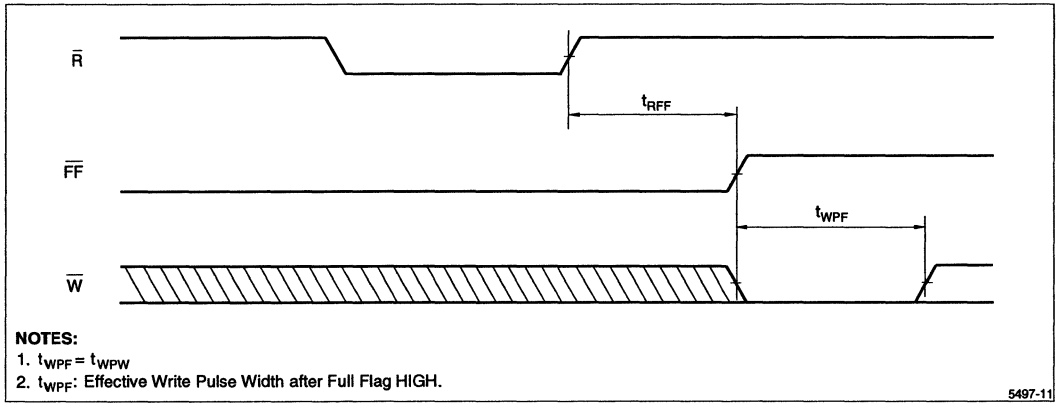


Figure 12. Full Flag Timing

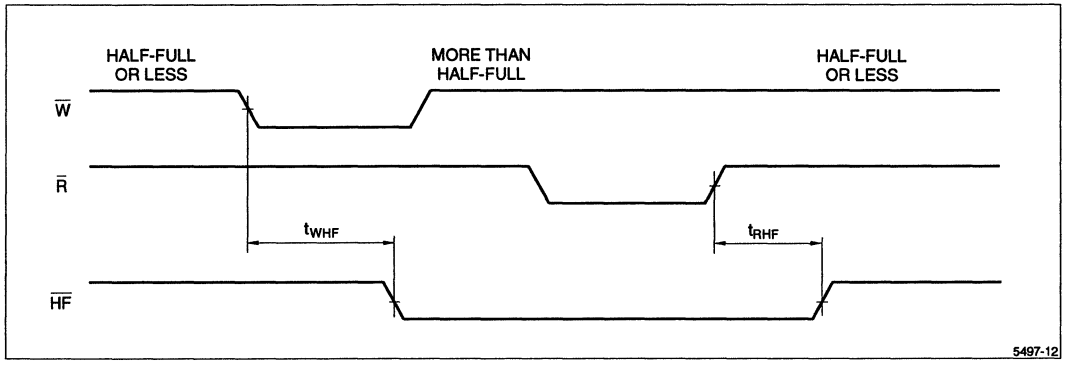


Figure 13. Half-Full Flag Timing

TIMING DIAGRAMS (cont'd)

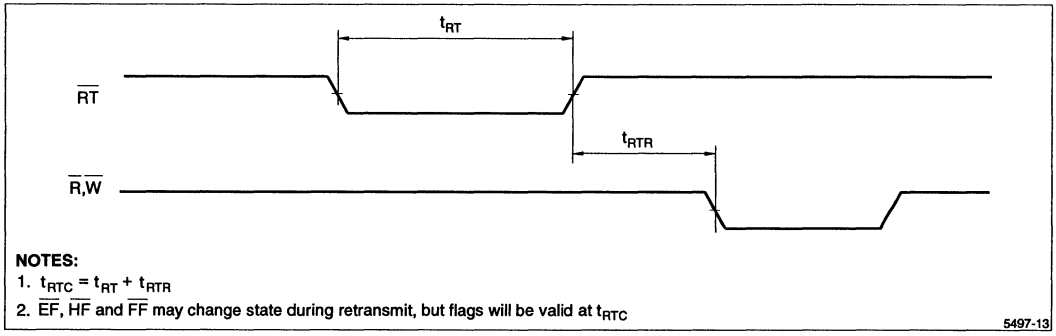


Figure 14. Retransmit Timing

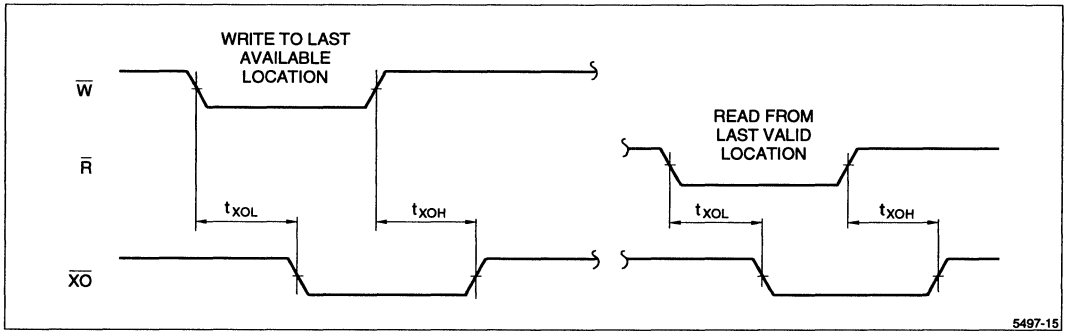


Figure 15. Expansion Out Timing

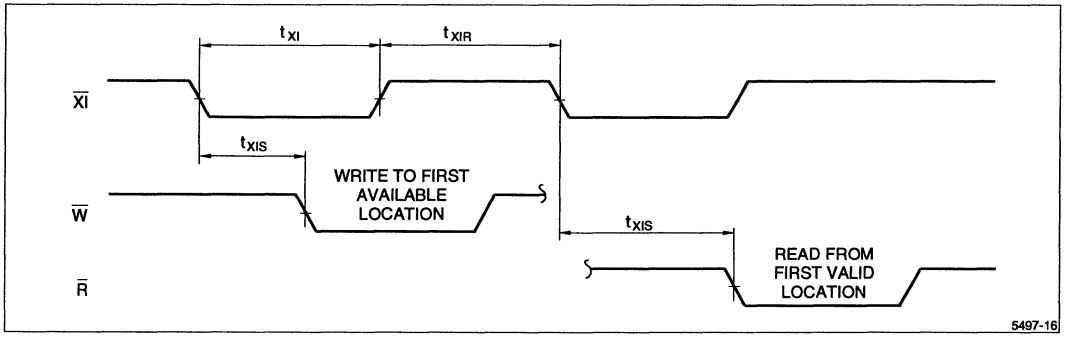


Figure 16. Expansion In Timing

OPERATIONAL MODES

Single Device Configuration

When depth expansion is not required for the given application, the device is placed in Single mode by tying the Expansion In pin ($\overline{XI}$) to ground. This pin is internally sampled during reset.

Width Expansion

Word-width expansion is implemented by placing multiple LH5497/97H devices in parallel. Each LH5497/97H should be configured for standalone mode. In this arrangement, the behavior of the status flags is identical for all devices; so, in principle, a representative value for each of these flags could be derived from any one device. In practice, it is better to derive 'composite' flag values using external logic, since there may be minor speed variations between different actual devices. (See Figures 17 and 18.)

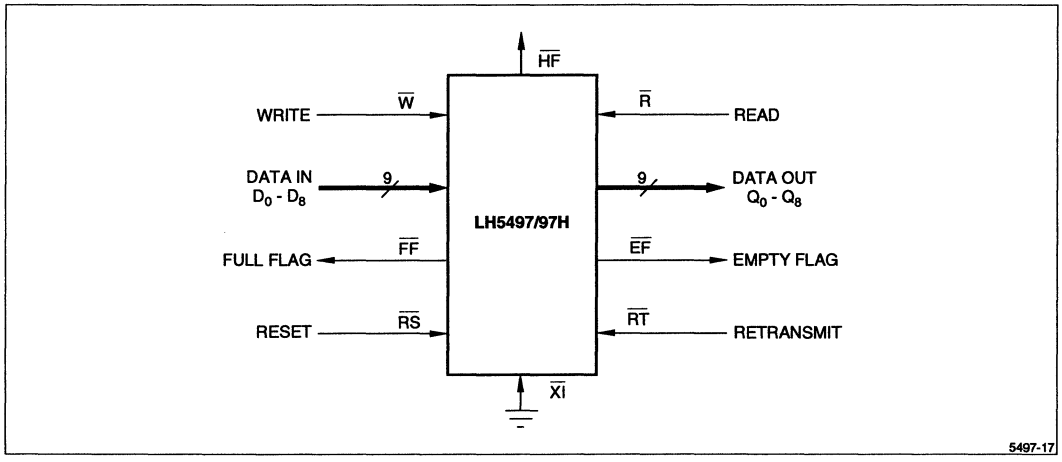


Figure 17. Single FIFO (1K × 9)

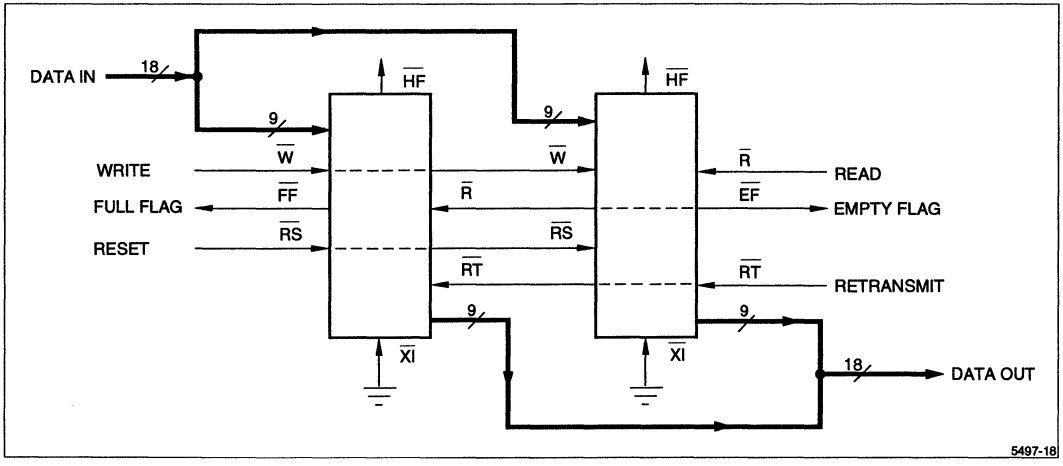


Figure 18. FIFO Width Expansion (1K × 18)

OPERATIONAL MODES (cont'd)

Depth Expansion

Depth expansion is implemented by configuring the required number of FIFOs in Expansion mode. In this arrangement, the FIFOs are connected in a circular fashion with the Expansion Out pin ($\overline{XO}$) of each device tied to the Expansion In pin ($\overline{XI}$) of the next device. One FIFO in this group must be designated as the first load device. This is accomplished by tying the First Load pin ($\overline{FL}$) of this device to ground. All other devices must have their $\overline{FL}$ pin tied to a high level. In this mode, $\overline{W}$ and $\overline{R}$ signals are shared by all devices, while internal logic controls the steering of data. Only one FIFO will be enabled for any given read cycle, so the common Data Out pins of all devices are wire-ORed together. Likewise, the common Data In pins of all devices are tied together.

In Expansion mode, external logic is required to generate a composite Full or Empty flag. This is achieved by ORing the $\overline{FF}$ pins of all devices and ORing the $\overline{EF}$ pins of all devices respectively. The Half-Full flag and Retransmit functions are not available in Depth Expansion mode.

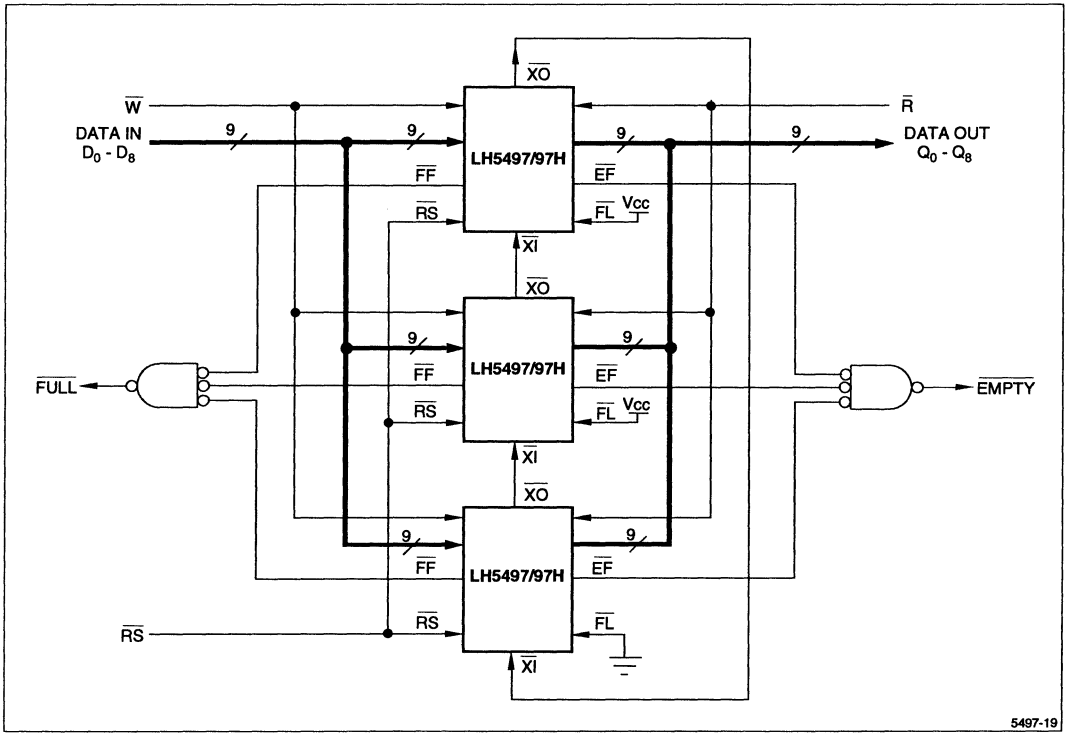


Figure 19. FIFO Depth Expansion (3072 × 9)

OPERATIONAL MODES (cont'd)

Compound Expansion

A combination of width and depth expansion can be easily implemented by operating groups of depth expanded FIFOs in parallel.

Bidirectional Operation

Applications which require bidirectional data buffering between two systems can be realized by operating LH5497/97H devices in parallel but opposite directions. The Data In pins of a device may be tied to the corresponding Data Out pins of another device operating in the opposite direction to form a single bidirectional bus interface. Care must be taken to assure that the appropriate read, write, and flag signals are routed to each system. Both depth and width expansion may be used in this configuration.

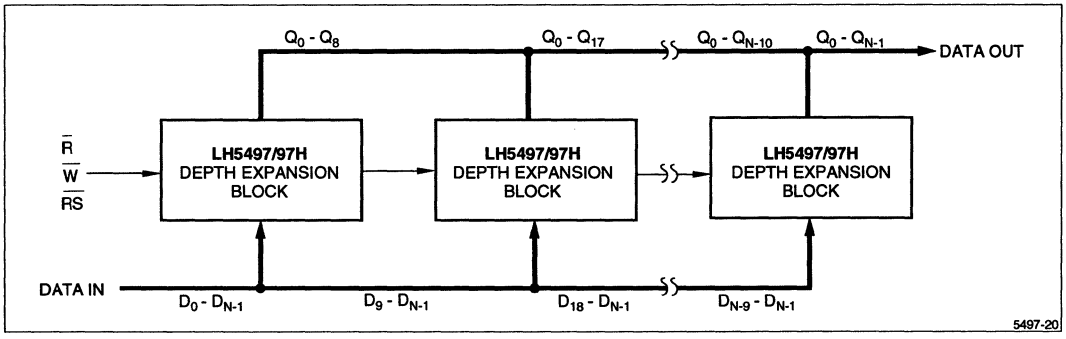


Figure 20. Compound FIFO

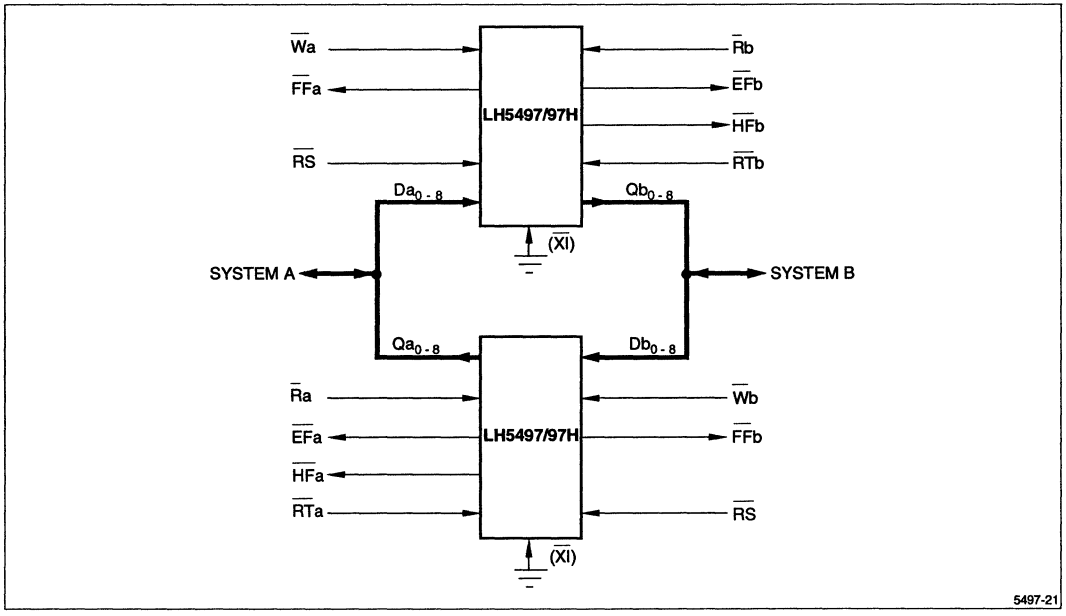
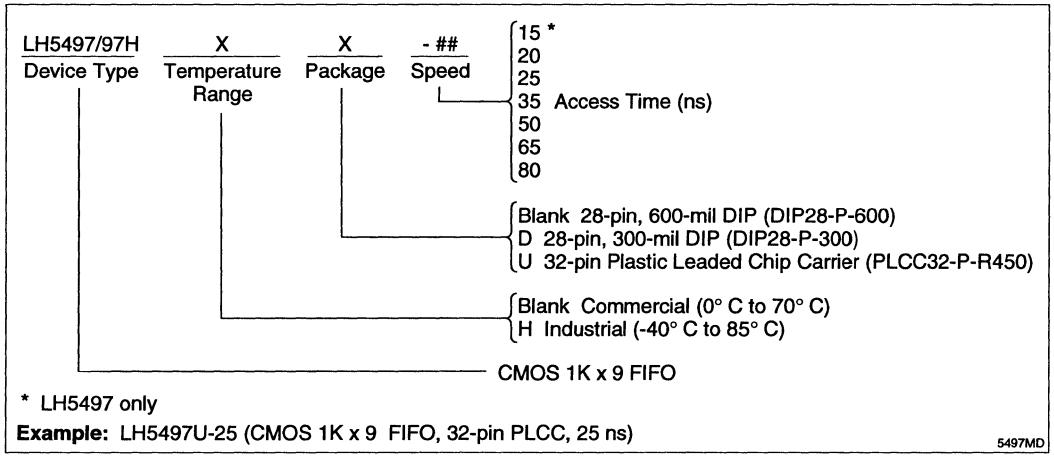


Figure 21. Bidirectional FIFO

ORDERING INFORMATION



LH5498

CMOS 2K × 9 FIFO

FEATURES

- Fast Access Times:
  15/20/25/35/50/65/80 ns
- Full CMOS Dual Port Memory Array
- Fully Asynchronous Read and Write
- Expandable in Width and Depth
- Full, Half-Full, and Empty Status Flags
- Read Retransmit Capability
- TTL Compatible I/O
- Packages:
  28-Pin, 300-mil DIP
  28-Pin, 600-mil DIP
  32-Pin PLCC
- Pin and Functionally Compatible with IDT7203

FUNCTIONAL DESCRIPTION

The LH5498 is a dual port memory with internal addressing to implement a First-In, First-Out algorithm. Through an advanced dual port architecture, it provides fully asynchronous read/write operation. Empty, Full, and Half-Full status flags are provided to prevent data overflow and underflow. In addition, internal logic is provided for unlimited expansion in both word size and depth.

Read and Write operations automatically access sequential locations in memory in such a way that data is read out in the same order that it was written, that is on a First-In, First-Out basis. Since the address sequence is internally predefined, no external address information is required for the operation of this device. A ninth data bit is provided for parity or control information often needed in communication applications.

Empty, Full, and Half-Full status flags monitor the extent to which data has been written into the FIFO, and prevent improper operations (i.e. Read if the FIFO is empty, or Write if the FIFO is full). A retransmit feature resets the Read address pointer to its initial position, thereby allowing repetitive readout of the same data. Expansion In and Expansion Out pins implement an expansion scheme that allows individual FIFOs to be cascaded to greater depth without incurring additional latency (bubblethrough) delays.

PIN CONNECTIONS

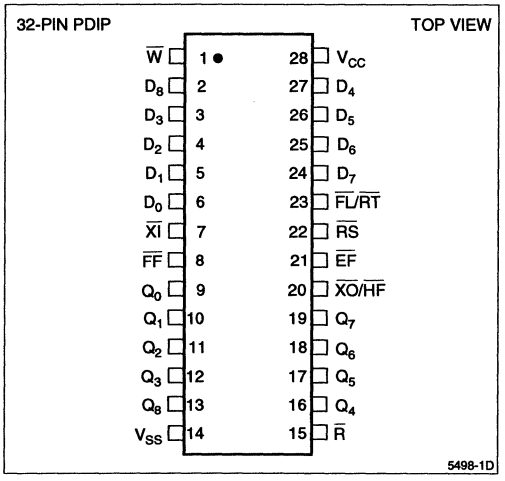


Figure 1. Pin Connections for DIP Packages

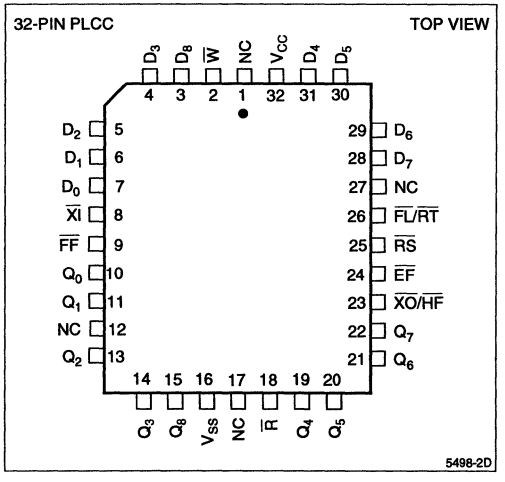


Figure 2. Pin Connections for PLCC Package

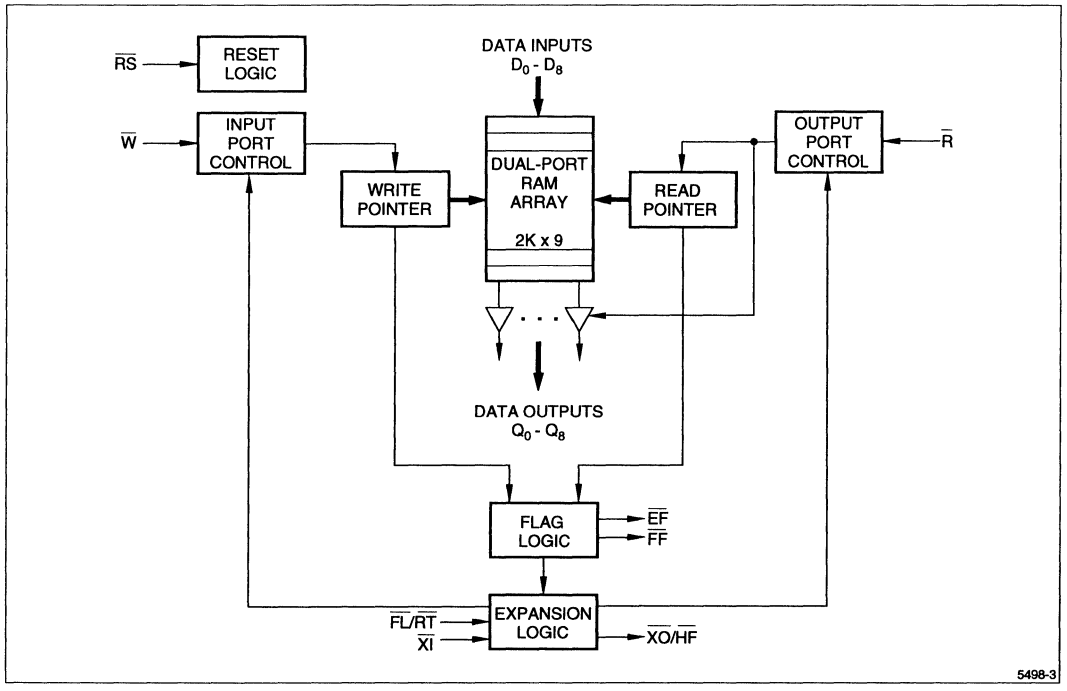


Figure 3. LH5498 Block Diagram

PIN DESCRIPTIONS

PIN	PIN TYPE *	DESCRIPTION
$D_0 - D_8$	I	Input Data Bus
$Q_0 - Q_8$	O/Z	Output Data Bus
$\overline{W}$	I	Write Request
$\overline{R}$	I	Read Request
$\overline{EF}$	O	Empty Flag
$\overline{FF}$	O	Full Flag

PIN	PIN TYPE *	DESCRIPTION
$\overline{XO}/\overline{HF}$	O	Expansion Out/Half-Full Flag
$\overline{XI}$	I	Expansion In
$\overline{FL}/\overline{RT}$	I	First Load/Retransmit
$\overline{RS}$	I	Reset
V_{CC}	V	Positive Power Supply
V_{SS}	V	Ground

* I = Input, O = Output, Z = High-Impedance, V = Power Voltage Level

ABSOLUTE MAXIMUM RATINGS [1]

PARAMETER	RATING
Supply Voltage to V_{SS} Potential	−0.5 V to 7 V
Signal Pin Voltage to V_{SS} Potential [3]	−0.5 V to V_{CC} + 0.5 V (not to exceed 7 V)
DC Output Current [2]	± 50 mA
Storage Temperature Range	−65°C to 150°C
Power Dissipation (Package Limit)	1.0 W
DC Voltage Applied to Outputs In High-Z State	−0.5 V to Vcc + 0.5 V (not to exceed 7 V)

NOTES:

1. Stresses greater than those listed under 'Absolute Maximum Ratings' may cause permanent damage to the device. This is a stress rating for transient conditions only. Functional operation of the device at these or any conditions other than those indicated in the 'Operating Range' of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Outputs should not be shorted for more than 30 seconds. No more than one output should be shorted at any time.
3. Negative undershoots of 1.5 V in amplitude are permitted for up to 10 ns once per cycle.

OPERATING RANGE

SYMBOL	PARAMETER	MIN	MAX	UNIT
T_A	Temperature, Ambient	0	70	°C
V_{CC}	Supply Voltage	4.5	5.5	V
V_{SS}	Supply Voltage	0	0	V
V_{IL}	Logic '0' Input Voltage[1]	−0.5	0.8	V
V_{IH}	Logic '1' Input Voltage	2.0	V_{CC} + 0.5	V

NOTE:

1. Negative undershoots of 1.5 V in amplitude are permitted for up to 10 ns once per cycle.

DC ELECTRICAL CHARACTERISTICS (OVER OPERATING RANGE)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
I_{LI}	Input Leakage Current	V_{CC} = 5.5 V, V_{IN} = 0 V to V_{CC}	−10	10	µA
I_{LO}	Output Leakage Current	$\overline{R} \geq V_{IH}$, 0 V ≤ V_{OUT} ≤ V_{CC}	−10	10	µA
V_{OH}	Output High Voltage	I_{OH} = −2.0 mA	2.4		V
V_{OL}	Output Low Voltage	I_{OL} = 8.0 mA		0.4	V
I_{CC}	Average Supply Current [1]	Measured at f = 40 MHz		100	mA
I_{CC2}	Average Standby Current [1]	All Inputs = V_{IH}		15	mA
I_{CC3}	Power Down Current [1]	All Inputs = V_{CC} − 0.2 V		5	mA

NOTE:

1. I_{CC}, I_{CC2}, and I_{CC3} are dependent upon actual output loading and cycle rates. Specified values are with outputs open.

AC TEST CONDITIONS

PARAMETER	RATING
Input Pulse Levels	V_{SS} to 3 V
Input Rise and Fall Times (10% to 90%)	5 ns
Input Timing Reference Levels	1.5 V
Output Reference Levels	1.5 V
Output Load, Timing Tests	Figure 4

CAPACITANCE [1,2]

PARAMETER	RATING
C_{IN} (Input Capacitance)	5 pF
C_{OUT} (Output Capacitance)	7 pF

NOTES:

1. Sample tested only.
2. Capacitances are maximum values at 25°C measured at 1.0 MHz with V_{IN} = 0 V.

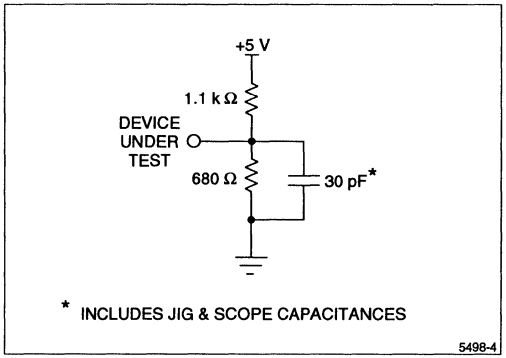


Figure 4. Output Load Circuit

AC ELECTRICAL CHARACTERISTICS [1] (Over Operating Range)

SYMBOL	PARAMETER	t_A = 15 ns		t_A = 20 ns		t_A = 25 ns		t_A = 35 ns		t_A = 50 ns		t_A = 65 ns		t_A = 80 ns		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
READ CYCLE TIMING																
t_{RC}	Read Cycle Time	25	–	30	–	35	–	45	–	65	–	80	–	100	–	ns
t_A	Access Time	–	15	–	20	–	25	–	35	–	50	–	65	–	80	ns
t_{RR}	Read Recover Time	10	–	10	–	10	–	10	–	15	–	15	–	15	–	ns
t_{RPW}	Read Pulse Width [2]	15	–	20	–	25	–	35	–	50	–	65	–	80	–	ns
t_{RLZ}	Data Bus Active from Read LOW [3]	5	–	5	–	5	–	5	–	5	–	5	–	10	–	ns
t_{WLZ}	Data Bus Active from Write HIGH [3,4]	10	–	10	–	10	–	10	–	10	–	10	–	20	–	ns
t_{DV}	Data Valid from Read Pulse HIGH	5	–	5	–	5	–	5	–	5	–	5	–	5	–	ns
t_{RHZ}	Data Bus High-Z from Read HIGH [3]	–	15	–	15	–	15	–	15	–	20	–	30	–	30	ns
WRITE CYCLE TIMING																
t_{WC}	Write Cycle Time	25	–	30	–	35	–	45	–	65	–	80	–	100	–	ns
t_{WPW}	Write Pulse Width [2]	15	–	20	–	25	–	35	–	50	–	65	–	80	–	ns
t_{WR}	Write Recovery Time	10	–	10	–	10	–	10	–	15	–	15	–	15	–	ns
t_{DS}	Data Setup Time	10	–	10	–	10	–	15	–	20	–	20	–	20	–	ns
t_{DH}	Data Hold Time	0	–	0	–	0	–	0	–	0	–	5	–	5	–	ns
RESET TIMING																
t_{RSC}	Reset Cycle Time	25	–	30	–	35	–	45	–	65	–	80	–	100	–	ns
t_{RS}	Reset Pulse Width [2]	15	–	20	–	25	–	35	–	50	–	65	–	80	–	ns
t_{RSR}	Reset Recovery Time	10	–	10	–	10	–	10	–	15	–	15	–	15	–	ns
t_{RRSS}	Read HIGH to $\overline{RS}$ HIGH	15	–	20	–	25	–	35	–	50	–	65	–	80	–	ns
t_{WRSS}	Write HIGH to $\overline{RS}$ HIGH	15	–	20	–	25	–	35	–	50	–	65	–	80	–	ns
RETRANSMIT TIMING																
t_{RTC}	Retransmit Cycle Time	25	–	30	–	35	–	45	–	65	–	80	–	100	–	ns
t_{RT}	Retransmit Pulse Width [2]	15	–	20	–	25	–	35	–	50	–	65	–	80	–	ns
t_{RTR}	Retransmit Recovery Time	10	–	10	–	10	–	10	–	15	–	15	–	15	–	ns
FLAG TIMING																
t_{EFL}	Reset LOW to Empty Flag LOW	–	25	–	30	–	35	–	45	–	65	–	80	–	100	ns
$t_{HFH,FFH}$	Reset LOW to Half-Full and Full Flags HIGH	–	25	–	30	–	35	–	45	–	65	–	80	–	100	ns
t_{REF}	Read LOW to Empty Flag LOW	–	20	–	25	–	25	–	35	–	45	–	60	–	60	ns
t_{RFF}	Read HIGH to Full Flag HIGH	–	20	–	25	–	25	–	35	–	45	–	60	–	60	ns
t_{WEF}	Write HIGH to Empty Flag HIGH	–	20	–	25	–	25	–	35	–	45	–	60	–	60	ns
t_{WFF}	Write LOW to Full Flag LOW	–	20	–	25	–	25	–	35	–	45	–	60	–	60	ns
t_{WHF}	Write LOW to Half-Full Flag LOW	–	25	–	30	–	35	–	45	–	65	–	80	–	100	ns
t_{RHF}	Read HIGH to Half-Full Flag HIGH	–	25	–	30	–	35	–	45	–	65	–	80	–	100	ns
EXPANSION TIMING																
t_{XOL}	Expansion Out LOW	–	18	–	20	–	25	–	35	–	50	–	65	–	80	ns
t_{XOH}	Expansion Out HIGH	–	18	–	20	–	25	–	35	–	50	–	65	–	80	ns
t_{XI}	Expansion In Pulse Width	15	–	20	–	25	–	35	–	50	–	65	–	80	–	ns
t_{XIR}	Expansion In Recovery Time	10	–	10	–	10	–	10	–	10	–	10	–	10	–	ns
t_{XIS}	Expansion In Setup Time	7	–	10	–	10	–	15	–	15	–	15	–	15	–	ns

NOTES:

1. All timing measurements performed at 'AC Test Condition' levels.
2. Pulse widths less than minimum value are not allowed.
3. Values guaranteed by design not currently tested.
4. Only applies to read data flow-through mode.

OPERATIONAL DESCRIPTION

Reset

The device is reset whenever the Reset pin ($\overline{RS}$) is taken to a LOW state. The reset operation initializes both the read and write address pointers to the first memory location. The $\overline{XI}$ and $\overline{FL}$ pins are also sampled at this time to determine whether the device is in Single mode or Depth Expansion mode. A reset pulse is required when the device is first powered up. The Read ($\overline{R}$) and Write ($\overline{W}$) pins may be in any state when reset is initiated, but must be brought to a HIGH state t_{RRSS} and t_{WRSS} before the rising edge of $\overline{RS}$.

Write

A write cycle is initiated on the falling edge of the Write ($\overline{W}$) pin. Data setup and hold times must be observed on the data-in ($D_0 - D_8$) pins. A write operation is only possible if the FIFO is not full, (i.e. the Full flag pin is HIGH). Writes may occur independently of any ongoing read operations.

At the falling edge of the first write after the memory is half filled, the Half-Full flag will be asserted ($\overline{HF}$ = LOW) and will remain asserted until the difference between the write pointer and read pointer indicates that the remaining data in the device is less than or equal to one-half the total capacity of the FIFO. The Half-Full flag is deasserted ($\overline{HF}$ = HIGH) by the appropriate rising edge of $\overline{R}$.

The Full flag is asserted ($\overline{FF}$ = LOW) at the falling edge of the write operation which fills the last available location in the FIFO memory array. The Full flag will inhibit further writes until cleared by a valid read. The Full flag is deasserted ($\overline{FF}$ = HIGH) after the next rising edge of $\overline{R}$ releases another memory location.

Read

A read cycle is initiated on the falling edge of the Read ($\overline{R}$) pin. Read data becomes valid on the data out (Q_0–Q_8) pins after a time t_A from the falling edge of $\overline{R}$. After $\overline{R}$ goes HIGH, the data out pins return to a high-impedance state. Reads may occur independent of any ongoing write operations. A read is only possible if the FIFO is not empty ($\overline{EF}$ = HIGH).

The internal read and write address pointers are maintained by the device such that consecutive read operations will access data in the same order as it was written. The Empty flag is asserted ($\overline{EF}$ = LOW) after the falling edge of $\overline{R}$ which accesses the last available data in the FIFO memory. $\overline{EF}$ is deasserted ($\overline{EF}$ = HIGH) after the next rising edge of $\overline{W}$ loads another word of valid data.

Data Flow-Through

Read flow-through mode occurs when the Read ($\overline{R}$) pin is brought LOW while the FIFO is empty, and held LOW in anticipation of a write cycle. At the end of the next write cycle, the Empty flag will be momentarily deasserted, and the data just written will become available on the data out pins after a maximum time of $t_{WEF} + t_A$. Additional writes may occur while the $\overline{R}$ pin remains LOW, but only data from the first write flows through to the outputs. Additional data, if any, can only be accessed by toggling $\overline{R}$.

Write flow-through mode occurs when the Write ($\overline{W}$) pin is brought LOW while the FIFO is full, and held LOW in anticipation of a read cycle. At the end of the read cycle, the Full flag will be momentarily deasserted, but then immediately reasserted in response to $\overline{W}$ held LOW. Data is written into the FIFO on the rising edge of $\overline{W}$ which may occur $t_{RFF} + t_{WPW}$ after the read.

Retransmit

The FIFO can be made to reread previously read data through the retransmit function. Retransmit is initiated by pulsing $\overline{RT}$ LOW. This resets the internal read address pointer to the first physical location in the memory while leaving the internal write address pointer unchanged. Data between the read and write pointers may be re-accessed by subsequent reads. Both $\overline{R}$ and $\overline{W}$ must be inactive (HIGH) during the retransmit pulse. Retransmit is useful if no more than 2048 writes are performed between resets. Retransmit may affect the status of $\overline{EF}$, $\overline{HF}$, and $\overline{FF}$ flags, depending on the relocation of the read pointer. This function is not available in depth expansion mode.

TIMING DIAGRAMS

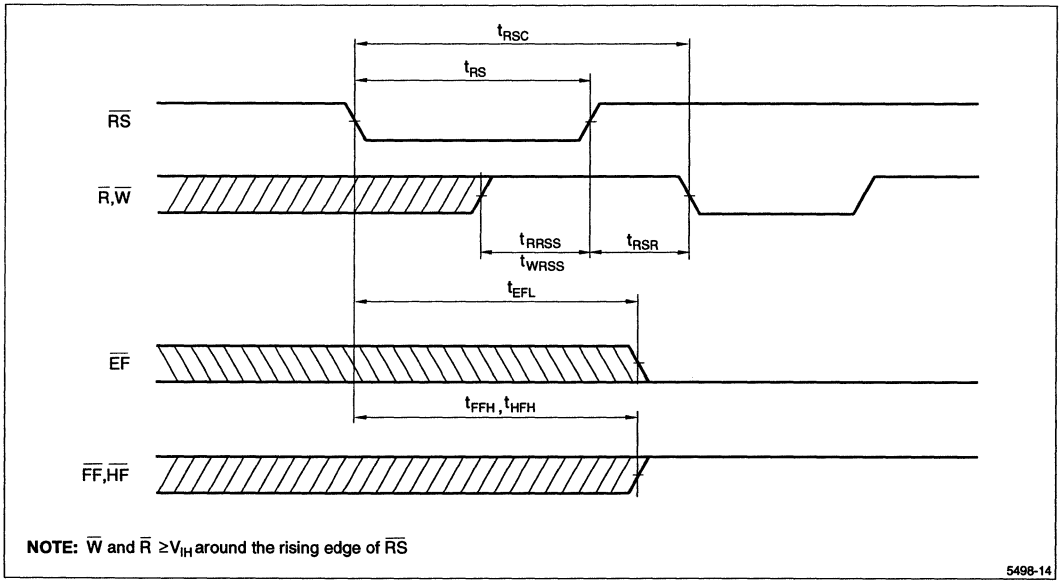


Figure 5. Reset Timing

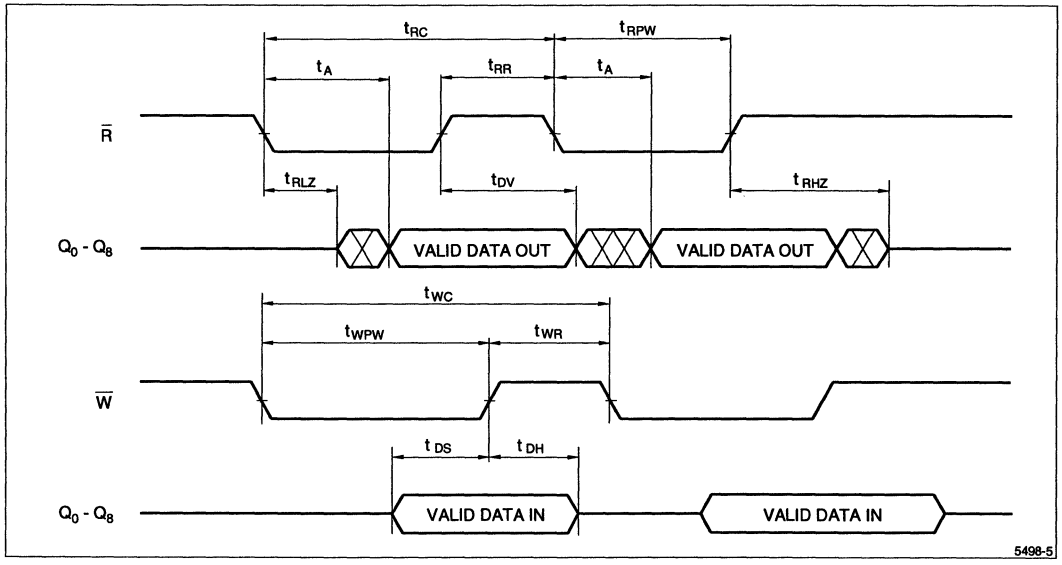


Figure 6. Asynchronous Write and Read Operation

TIMING DIAGRAMS (cont'd)

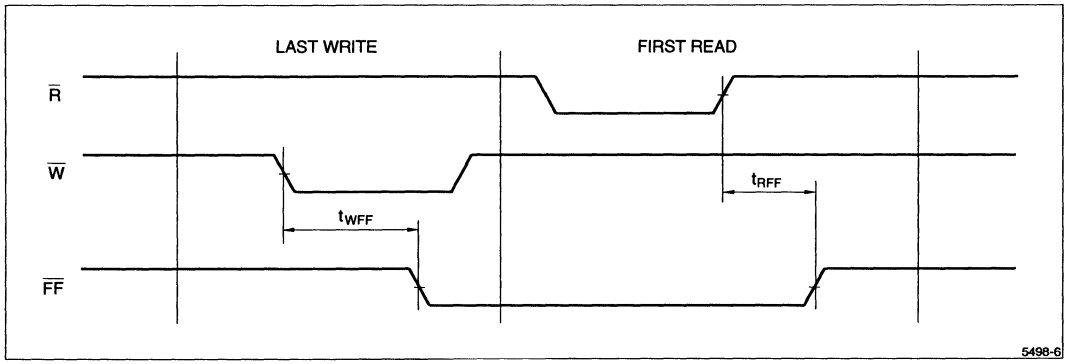


Figure 7. Full Flag from Last Write to First Read

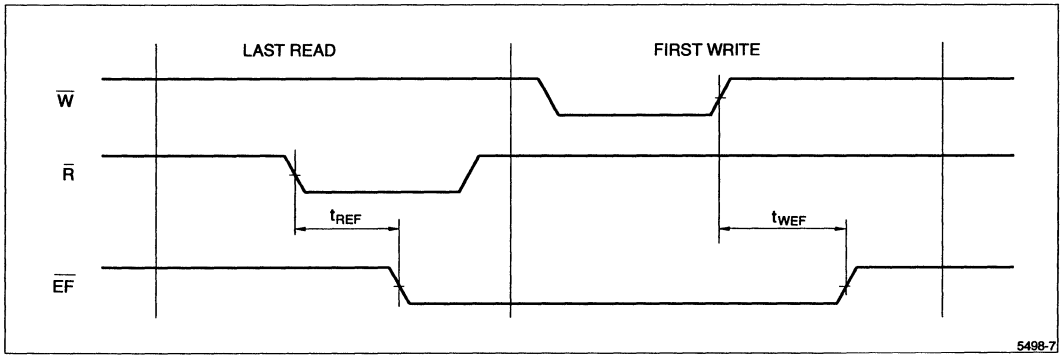


Figure 8. Empty Flag from Last Read to First Write

TIMING DIAGRAMS (cont'd)

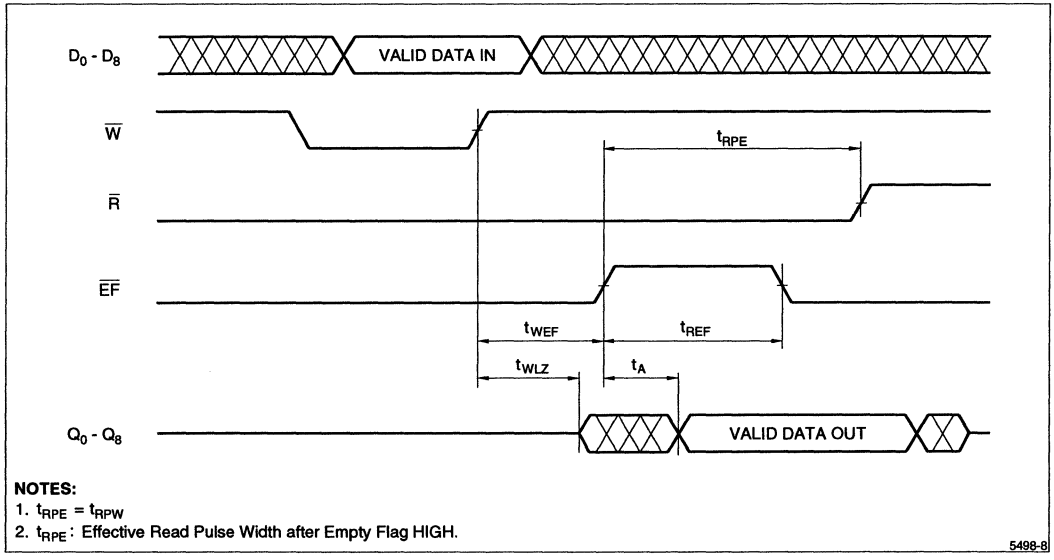


Figure 9. Read Data Flow-Through

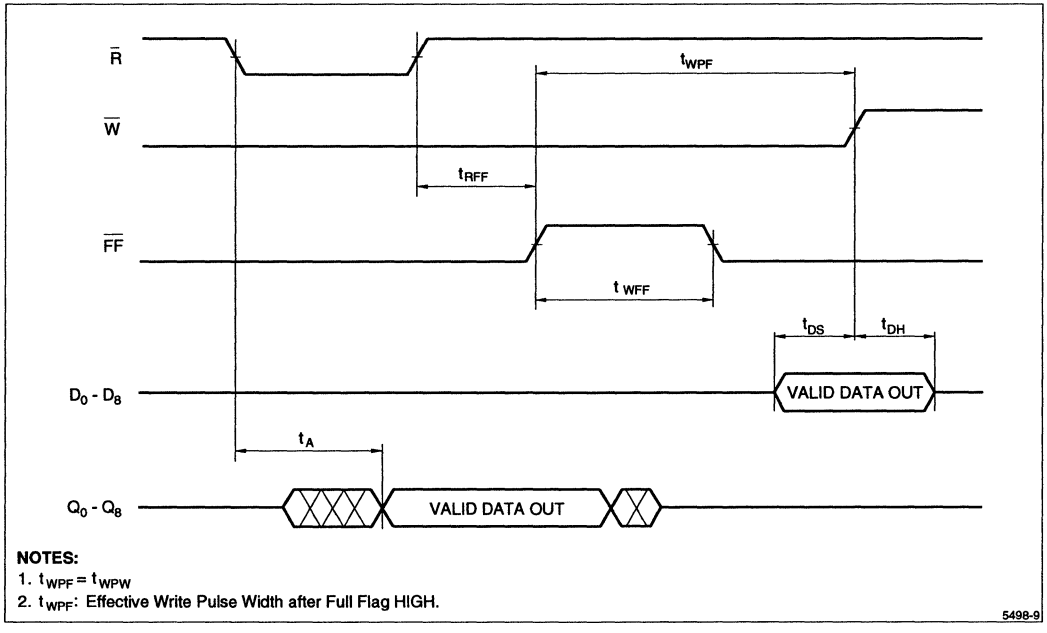


Figure 10. Write Data Flow-Through

TIMING DIAGRAMS (cont'd)

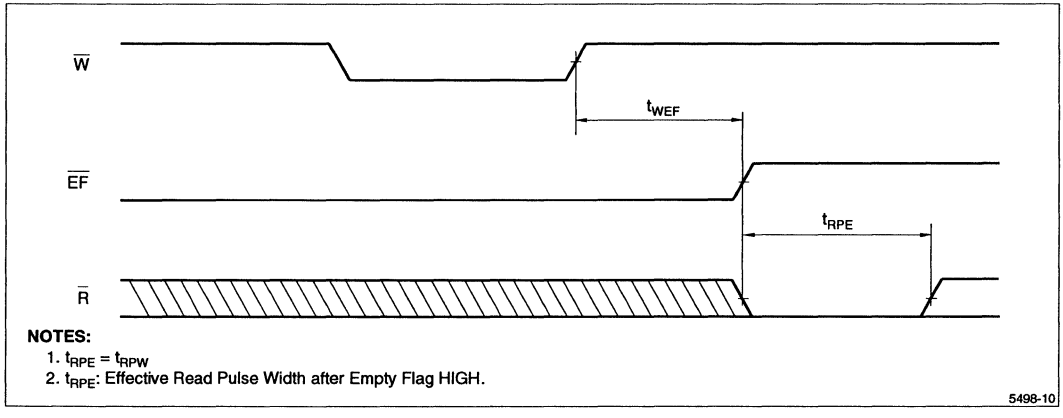


Figure 11. Empty Flag Timing

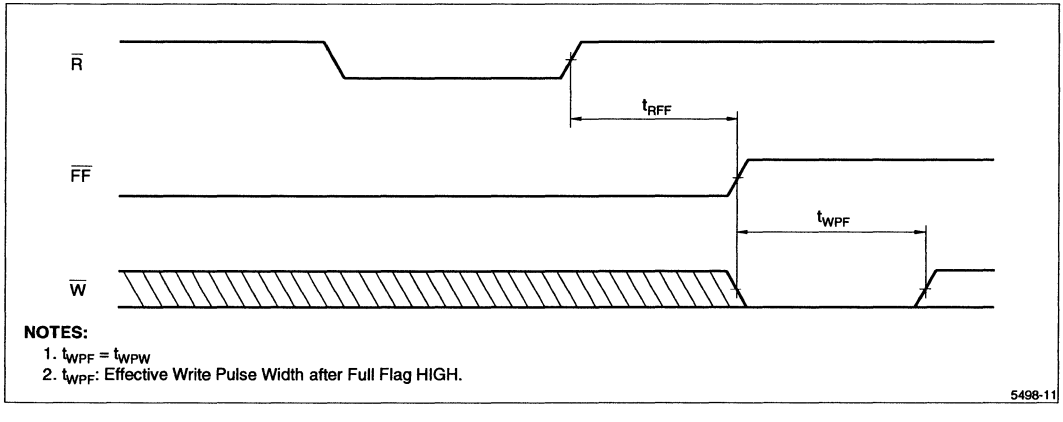


Figure 12. Full Flag Timing

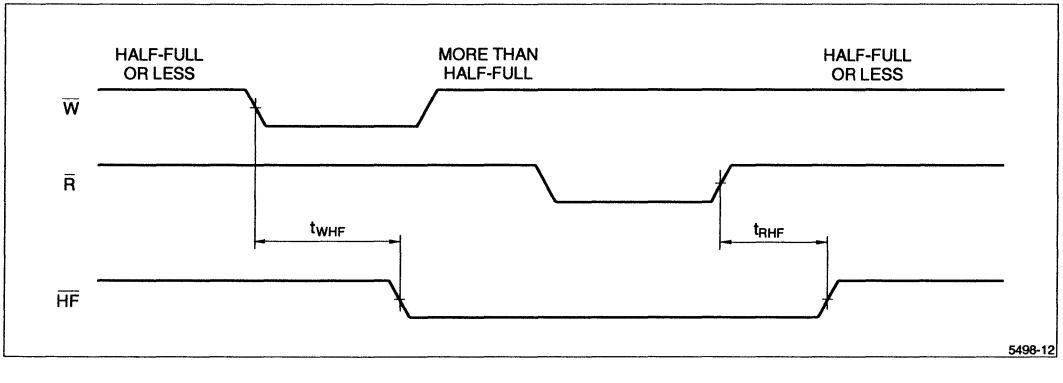


Figure 13. Half-Full Flag Timing

TIMING DIAGRAMS (cont'd)

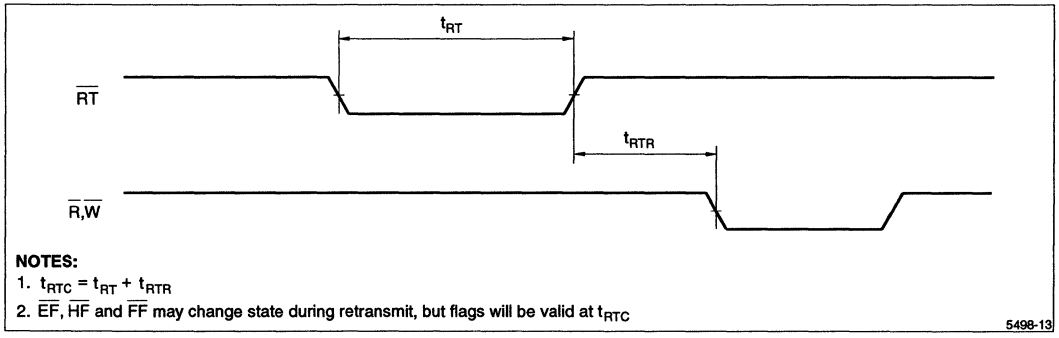


Figure 14. Retransmit Timing

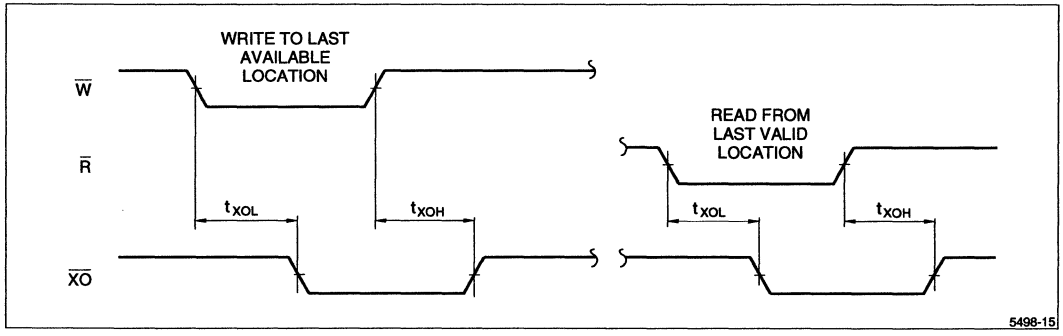


Figure 15. Expansion Out Timing

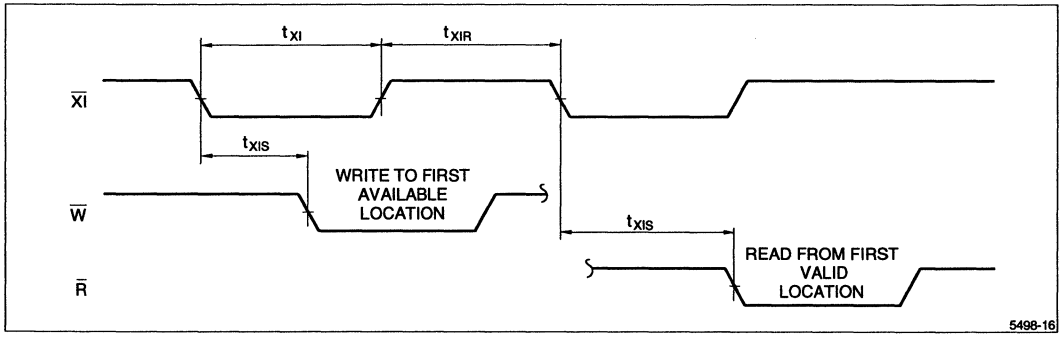


Figure 16. Expansion In Timing

OPERATIONAL MODES

Single Device Configuration

When depth expansion is not required for the given application, the device is placed in Single mode by tying the Expansion In pin ($\overline{XI}$) to ground. This pin is internally sampled during reset.

Width Expansion

Word-width expansion is implemented by placing multiple LH5498 devices in parallel. Each LH5498 should be configured for standalone mode. In this arrangement, the behavior of the status flags is identical for all devices; so, in principle, a representative value for each of these flags could be derived from any one device. In practice, it is better to derive 'composite' flag values using external logic, since there may be minor speed variations between different actual devices. (See Figures 17 and 18.)

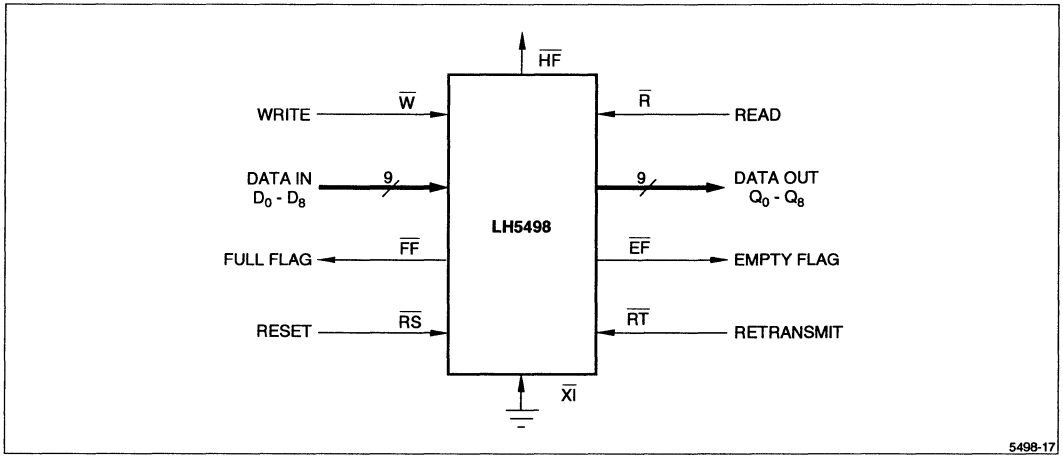


Figure 17. Single FIFO (2K × 9)

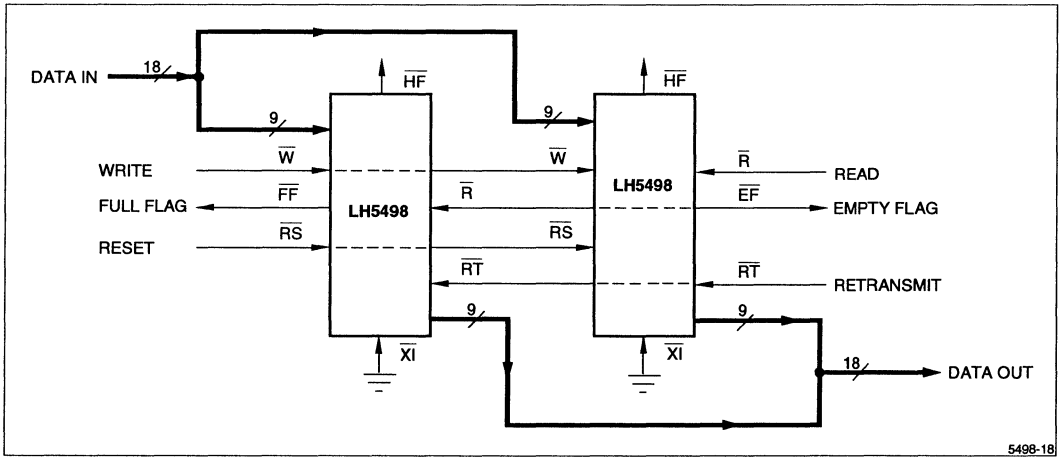


Figure 18. FIFO Width Expansion (2K × 18)

OPERATIONAL MODES (cont'd)

Depth Expansion

Depth expansion is implemented by configuring the required number of FIFOs in Expansion mode. In this arrangement, the FIFOs are connected in a circular fashion with the Expansion Out pin ($\overline{XO}$) of each device tied to the Expansion In pin ($\overline{XI}$) of the next device. One FIFO in this group must be designated as the first load device. This is accomplished by tying the First Load pin ($\overline{FL}$) of this device to ground. All other devices must have their $\overline{FL}$ pin tied to a high level. In this mode, $\overline{W}$ and $\overline{R}$ signals are shared by all devices, while internal logic controls the steering of data. Only one FIFO will be enabled for any given read cycle, so the common Data Out pins of all devices are wire-ORed together. Likewise, the common Data In pins of all devices are tied together.

In Expansion mode, external logic is required to generate a composite Full or Empty flag. This is achieved by ORing the $\overline{FF}$ pins of all devices and ORing the $\overline{EF}$ pins of all devices respectively. The Half-Full flag and Retransmit functions are not available in Depth Expansion mode.

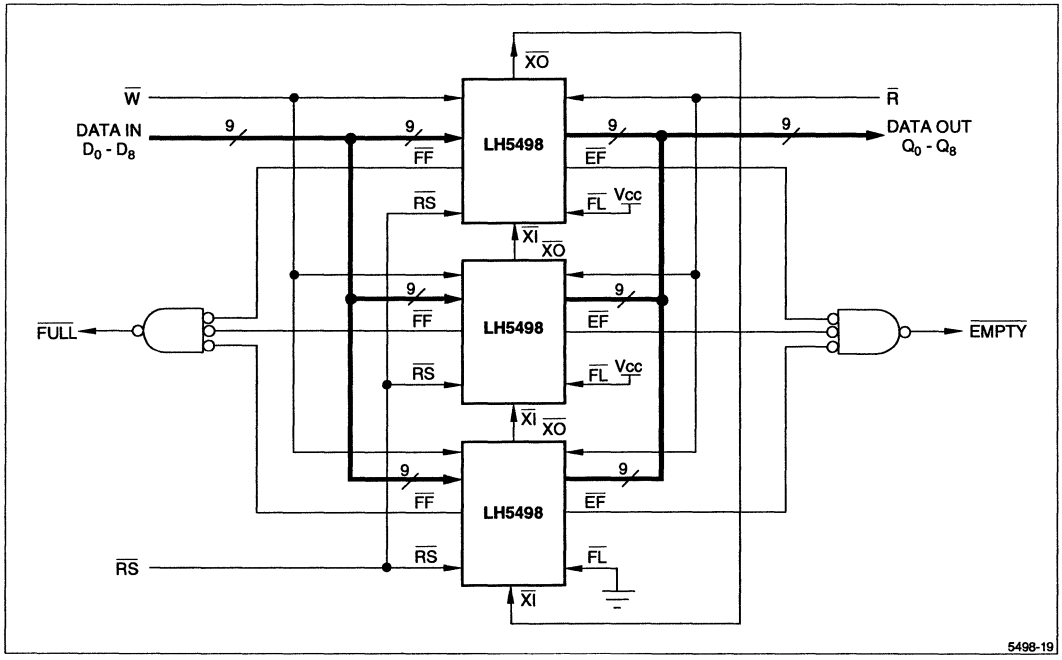


Figure 19. FIFO Depth Expansion (6144 × 9)

OPERATIONAL MODES (cont'd)

Compound Expansion

A combination of width and depth expansion can be easily implemented by operating groups of depth expanded FIFOs in parallel.

Bidirectional Operation

Applications which require bidirectional data buffering between two systems can be realized by operating LH5498 devices in parallel but opposite directions. The Data In pins of a device may be tied to the corresponding Data Out pins of another device operating in the opposite direction to form a single bidirectional bus interface. Care must be taken to assure that the appropriate read, write and flag signals are routed to each system. Both depth and width expansion may be used in this configuration.

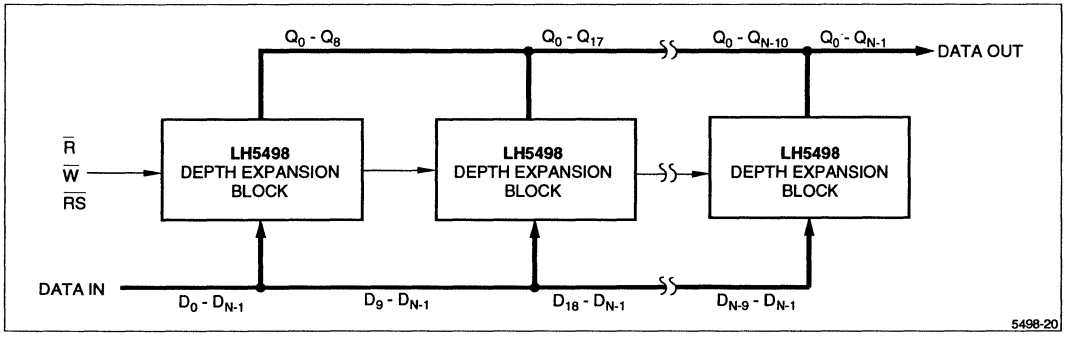


Figure 20. Compound FIFO

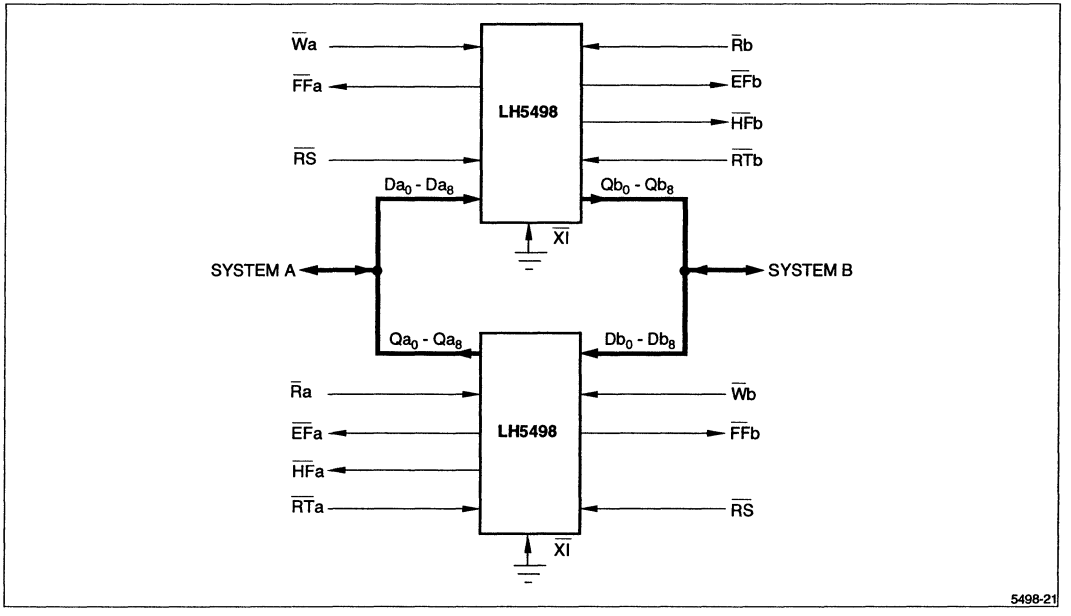
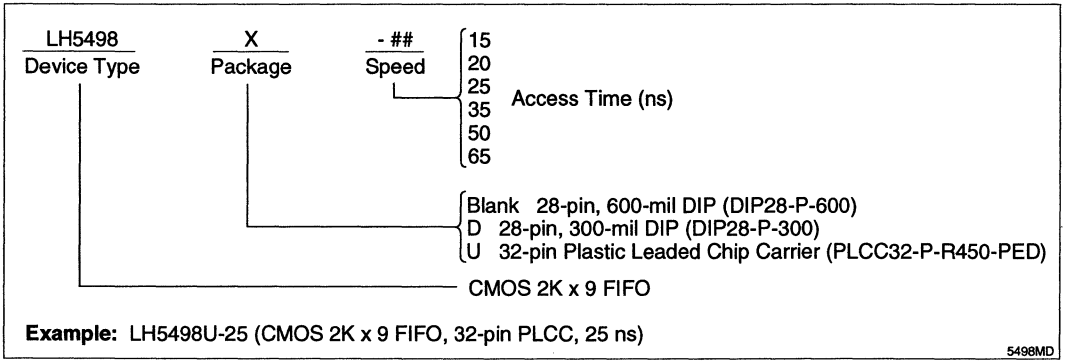


Figure 21. Bidirectional FIFO

ORDERING INFORMATION



LH5499

CMOS 4K × 9 FIFO

FEATURES

- Fast Access Times: 20/25/35/50/65/80 ns
- Full CMOS Dual Port Memory Array
- Fully Asynchronous Read and Write
- Expandable in Width and Depth
- Full, Half-Full, and Empty Status Flags
- Read Retransmit Capability
- TTL Compatible I/O
- Packages:
  28-Pin, 600-mil DIP
  32-Pin PLCC
- Pin and Functionally Compatible with IDT7204

FUNCTIONAL DESCRIPTION

The LH5499 is a dual port memory with internal addressing to implement a First-In, First-Out algorithm. Through an advanced dual port architecture, it provides fully asynchronous read/write operation. Empty, Full, and Half-Full status flags are provided to prevent data overflow and underflow. Internal logic is provided for unlimited expansion in both word size and depth.

Read and Write operations automatically access sequential locations in memory in such a way that data is read out in the same order that it was written, that is on a First-In, First-Out basis. Since the address sequence is internally predefined, no external address information is required for the operation of this device. A ninth data bit is provided for parity or control information often needed in communication applications.

Empty, Full, and Half-Full status flags monitor the extent to which data has been written into the FIFO, and prevent improper operations (i.e., Read if the FIFO is empty, or Write if the FIFO is full). A retransmit feature resets the Read address pointer to its initial position, thereby allowing repetitive readout of the same data. Expansion in and Expansion out pins implement an expansion scheme that allows individual FIFOs to be cascaded to greater depth without incurring additional latency (bubblethrough) delays.

PIN CONNECTIONS

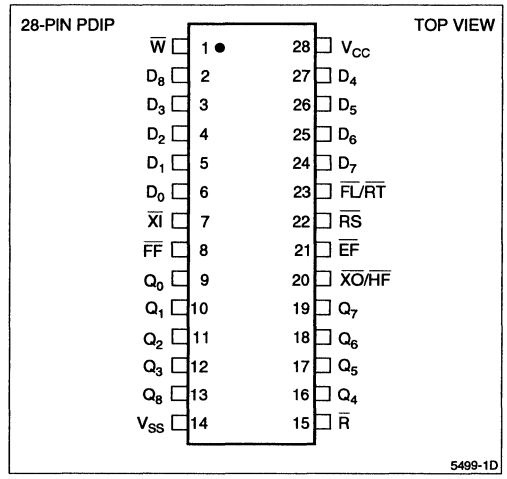


Figure 1. Pin Connections for PDIP Package

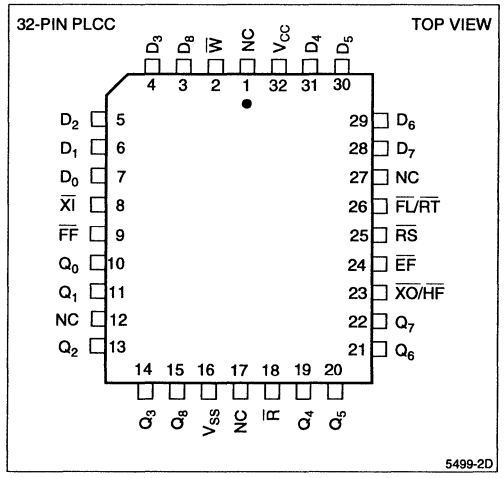


Figure 2. Pin Connections for PLCC Package

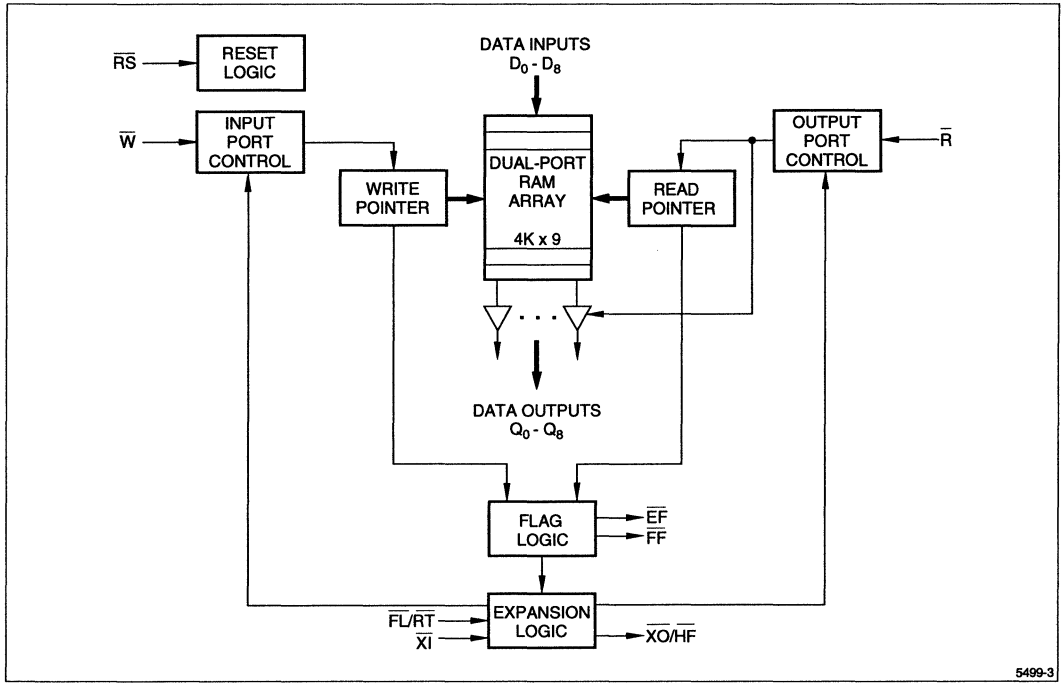


Figure 3. LH5499 Block Diagram

PIN DESCRIPTIONS

PIN	PIN TYPE *	DESCRIPTION
$D_0 - D_8$	I	Input Data Bus
$Q_0 - Q_8$	O/Z	Output Data Bus
$\overline{W}$	I	Write Request
$\overline{R}$	I	Read Request
$\overline{EF}$	O	Empty Flag
$\overline{FF}$	O	Full Flag

PIN	PIN TYPE *	DESCRIPTION
$\overline{XO}/\overline{HF}$	O	Expansion Out/Half-Full Flag
$\overline{XI}$	I	Expansion In
$\overline{FL}/\overline{RT}$	I	First Load/Retransmit
$\overline{RS}$	I	Reset
V_{CC}	V	Positive Power Supply
V_{SS}	V	Ground

* I = Input, O = Output, Z = High-Impedance, V = Power Voltage Level

ABSOLUTE MAXIMUM RATINGS [1]

PARAMETER	RATING
Supply Voltage to V_{SS} Potential	−0.5 V to 7 V
Signal Pin Voltage to V_{SS} Potential [3]	−0.5 V to V_{CC} + 0.5 V (not to exceed 7 V)
DC Output Current [2]	± 50 mA
Storage Temperature Range	−65°C to 150°C
Power Dissipation (Package Limit)	1.0 W
DC Voltage Applied to Outputs In High-Z State	−0.5 V to V_{CC} + 0.5 V (not to exceed 7 V)

NOTES:

1. Stresses greater than those listed under 'Absolute Maximum Ratings' may cause permanent damage to the device. This is a stress rating for transient conditions only. Functional operation of the device at these or any other conditions above those indicated in the 'Operating Range' of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Outputs should not be shorted for more than 30 seconds. No more than one output should be shorted at any time.
3. Negative undershoots of 1.5 V in amplitude are permitted for up to 10 ns once per cycle.

OPERATING RANGE

SYMBOL	PARAMETER	MIN	MAX	UNIT
T_A	Temperature, Ambient	0	70	°C
V_{CC}	Supply Voltage	4.5	5.5	V
V_{SS}	Supply Voltage	0	0	V
V_{IL}	Logic '0' Input Voltage [1]	−0.5	0.8	V
V_{IH}	Logic '1' Input Voltage	2.0	V_{CC} + 0.5	V

NOTE:

1. Negative undershoots of 1.5 V in amplitude are permitted for up to 10 ns once per cycle.

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
I_{LI}	Input Leakage Current	V_{CC} = 5.5 V, V_{IN} = 0 V to V_{CC}	−10	10	µA
I_{LO}	Output Leakage Current	$\overline{R} \geq V_{IH}$, 0 V ≤ V_{OUT} ≤ V_{CC}	−10	10	µA
V_{OH}	Output High Voltage	I_{OH} = −2.0 mA	2.4		V
V_{OL}	Output Low Voltage	I_{OL} = 8.0 mA		0.4	V
I_{CC}	Average Supply Current [1]	Measured at f = 33 MHz		110	mA
I_{CC2}	Average Standby Current [1]	All Inputs = V_{IH}		15	mA
I_{CC3}	Power Down Current [1]	All Inputs = V_{CC} − 0.2 V		8	mA

NOTE:

1. I_{CC}, I_{CC2}, and I_{CC3} are dependent upon actual output loading and cycle rates. Specified values are with outputs open.

AC TEST CONDITIONS

PARAMETER	RATING
Input Pulse Levels	V_{SS} to 3 V
Input Rise and Fall Times (10% to 90%)	5 ns
Input Timing Reference Levels	1.5 V
Output Reference Levels	1.5 V
Output Load, Timing Tests	Figure 4

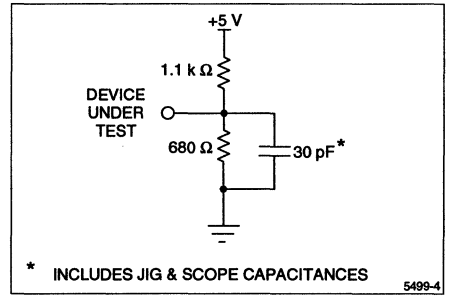


Figure 4. Output Load Circuit

CAPACITANCE [1,2]

PARAMETER	RATING
C_{IN} (Input Capacitance)	5 pF
C_{OUT} (Output Capacitance)	7 pF

NOTES:

1. Sample tested only.
2. Capacitances are maximum values at 25°C measured at 1.0 MHz with V_{IN} = 0 V.

AC ELECTRICAL CHARACTERISTICS [1] (Over Operating Range)

SYMBOL	PARAMETER	t_A = 20 ns		t_A = 25 ns		t_A = 35 ns		t_A = 50 ns		t_A = 65 ns		t_A = 80 ns		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
READ CYCLE TIMING														
t_{RC}	Read Cycle Time	30	–	35	–	45	–	65	–	80	–	100	–	ns
t_A	Access Time	–	20	–	25	–	35	–	50	–	65	–	80	ns
t_{RR}	Read Recover Time	10	–	10	–	10	–	15	–	15	–	15	–	ns
t_{RPW}	Read Pulse Width [2]	20	–	25	–	35	–	50	–	65	–	80	–	ns
t_{RLZ}	Data Bus Active from Read LOW [3]	5	–	5	–	5	–	5	–	5	–	10	–	ns
t_{WLZ}	Data Bus Active from Write HIGH [3,4]	10	–	10	–	10	–	10	–	10	–	20	–	ns
t_{DV}	Data Valid from Read Pulse HIGH	5	–	5	–	5	–	5	–	5	–	5	–	ns
t_{RHZ}	Data Bus High-Z from Read HIGH [3]	–	15	–	15	–	15	–	20	–	30	–	30	ns
WRITE CYCLE TIMING														
t_{WC}	Write Cycle Time	30	–	35	–	45	–	65	–	80	–	100	–	ns
t_{WPW}	Write Pulse Width [2]	20	–	25	–	35	–	50	–	65	–	80	–	ns
t_{WR}	Write Recovery Time	10	–	10	–	10	–	15	–	15	–	15	–	ns
t_{DS}	Data Setup Time	10	–	10	–	15	–	20	–	20	–	20	–	ns
t_{DH}	Data Hold Time	0	–	0	–	0	–	0	–	5	–	5	–	ns
RESET TIMING														
t_{RSC}	Reset Cycle Time	30	–	35	–	45	–	65	–	80	–	100	–	ns
t_{RS}	Reset Pulse Width [2]	20	–	25	–	35	–	50	–	65	–	80	–	ns
t_{RSR}	Reset Recovery Time	10	–	10	–	10	–	15	–	15	–	15	–	ns
t_{RRSS}	Read HIGH to $\overline{RS}$ HIGH	20	–	25	–	35	–	50	–	65	–	80	–	ns
t_{WRSS}	Write HIGH to $\overline{RS}$ HIGH	20	–	25	–	35	–	50	–	65	–	80	–	ns
RETRANSMIT TIMING [5]														
t_{RTC}	Retransmit Cycle Time	30	–	35	–	45	–	65	–	80	–	100	–	ns
t_{RT}	Retransmit Pulse Width [2]	20	–	25	–	35	–	50	–	65	–	80	–	ns
t_{RTR}	Retransmit Recovery Time	10	–	10	–	10	–	15	–	15	–	15	–	ns
FLAG TIMING														
t_{EFL}	Reset LOW to Empty Flag LOW	–	30	–	35	–	45	–	65	–	80	–	100	ns
$t_{HFH,FFH}$	Reset LOW to Half-Full and Full Flags HIGH	–	30	–	35	–	45	–	65	–	80	–	100	ns
t_{REF}	Read LOW to Empty Flag LOW	–	25	–	25	–	35	–	45	–	60	–	60	ns
t_{RFF}	Read HIGH to Full Flag HIGH	–	25	–	25	–	35	–	45	–	60	–	60	ns
t_{WEF}	Write HIGH to Empty Flag HIGH	–	25	–	25	–	35	–	45	–	60	–	60	ns
t_{WFF}	Write LOW to Full Flag LOW	–	25	–	25	–	35	–	45	–	60	–	60	ns
t_{WHF}	Write LOW to Half-Full Flag LOW	–	30	–	35	–	45	–	65	–	80	–	100	ns
t_{RHF}	Read HIGH to Half-Full Flag HIGH	–	30	–	35	–	45	–	65	–	80	–	100	ns
EXPANSION TIMING														
t_{XOL}	Expansion Out LOW	–	20	–	25	–	35	–	50	–	65	–	80	ns
t_{XOH}	Expansion Out HIGH	–	20	–	25	–	35	–	50	–	65	–	80	ns
t_{XI}	Expansion In Pulse Width	20	–	25	–	35	–	50	–	65	–	80	–	ns
t_{XIR}	Expansion In Recovery Time	10	–	10	–	10	–	10	–	10	–	10	–	ns
t_{XIS}	Expansion in Setup Time	10	–	10	–	15	–	15	–	15	–	15	–	ns

NOTES:

1. All timing measurements performed at 'AC Test Condition' levels.
2. Pulse widths less than minimum value are not allowed.
3. Values guaranteed by design not currently tested.
4. Only applies to read data flow-through mode.
5. See also Note 3, Figure 13.

OPERATIONAL DESCRIPTION

Reset

The device is reset whenever the Reset pin ($\overline{RS}$) is taken to a LOW state. The reset operation initializes both the read and write address pointers to the first memory location. The $\overline{XI}$ and $\overline{FL}$ pins are also sampled at this time to determine whether the device is in Single mode or Depth Expansion mode. A reset pulse is required when the device is first powered up. The Read ($\overline{R}$) and Write ($\overline{W}$) pins may be in any state when reset is initiated, but must be brought to a HIGH state t_{RPW} and t_{WPW} before the rising edge of $\overline{RS}$.

Write

A write cycle is initiated on the falling edge of the Write ($\overline{W}$) pin. Data setup and hold times must be observed on the data in ($D_0 - D_8$) pins. A write operation is only possible if the FIFO is not full, (i.e. the Full flag pin is HIGH). Writes may occur independently of any ongoing read operations.

At the falling edge of the first write after the memory is half filled, the Half-Full flag will be asserted ($\overline{HF}$ = LOW) and will remain asserted until the difference between the write pointer and read pointer indicates that the remaining data in the device is less than or equal to one half the total capacity of the FIFO. The Half-Full flag is deasserted ($\overline{HF}$ = HIGH) by the appropriate rising edge of $\overline{R}$.

The Full flag is asserted ($\overline{FF}$ = LOW) at the falling edge of the write operation which fills the last available location in the FIFO memory array. The Full flag will inhibit further writes until cleared by a valid read. The Full flag is deasserted ($\overline{FF}$ = HIGH) after the next rising edge of $\overline{R}$ releases another memory location.

Read

A read cycle is initiated on the falling edge of the Read ($\overline{R}$) pin. Read data becomes valid on the data out (Q_0–Q_8) pins after a time t_A from the falling edge of $\overline{R}$. After $\overline{R}$ goes HIGH, the data out pins return to a high-impedance state. Reads may occur independent of any ongoing write operations. A read is only possible if the FIFO is not empty ($\overline{EF}$ = HIGH).

The internal read and write address pointers are maintained by the device such that consecutive read operations will access data in the same order as it was written. The Empty flag is asserted ($\overline{EF}$ = LOW) after the falling edge of $\overline{R}$ which accesses the last available data in the FIFO memory. $\overline{EF}$ is deasserted ($\overline{EF}$ = HIGH) after the next rising edge of $\overline{W}$ loads another word of valid data.

Data Flow-Through

Read flow-through mode occurs when the Read ($\overline{R}$) pin is brought LOW while the FIFO is empty, and held LOW in anticipation of a write cycle. At the end of the next write cycle, the Empty flag will be momentarily de-asserted, and the data just written will become available on the data out pins after a maximum time of $t_{WEF} + t_A$. Additional writes may occur while the $\overline{R}$ pin remains LOW, but only data from the first write flows through to the outputs. Additional data, if any, can only be accessed by toggling $\overline{R}$.

Write flow-through mode occurs when the Write ($\overline{W}$) pin is brought LOW while the FIFO is full, and held LOW in anticipation of a read cycle. At the end of the read cycle, the Full flag will be momentarily deasserted, but then immediately reasserted in response to $\overline{W}$ held LOW. Data is written into the FIFO on the rising edge of $\overline{W}$ which may occur $t_{RFF} + t_{WPW}$ after the read.

Retransmit

The FIFO can be made to reread previously read data through the retransmit function. Retransmit is initiated by pulsing $\overline{RT}$ LOW. This resets the internal read address pointer to the first physical location in the memory while leaving the internal write address pointer unchanged. Data between the read and write pointers may be reaccessed by subsequent reads. Both $\overline{R}$ and $\overline{W}$ must be inactive (HIGH) during the retransmit pulse. Retransmit is useful if no more than 4096 writes are performed between resets. Retransmit may affect the status of $\overline{EF}$, $\overline{HF}$, and $\overline{FF}$ flags, depending on the relocation of the read pointer. This function is not available in depth expansion mode.

TIMING DIAGRAMS

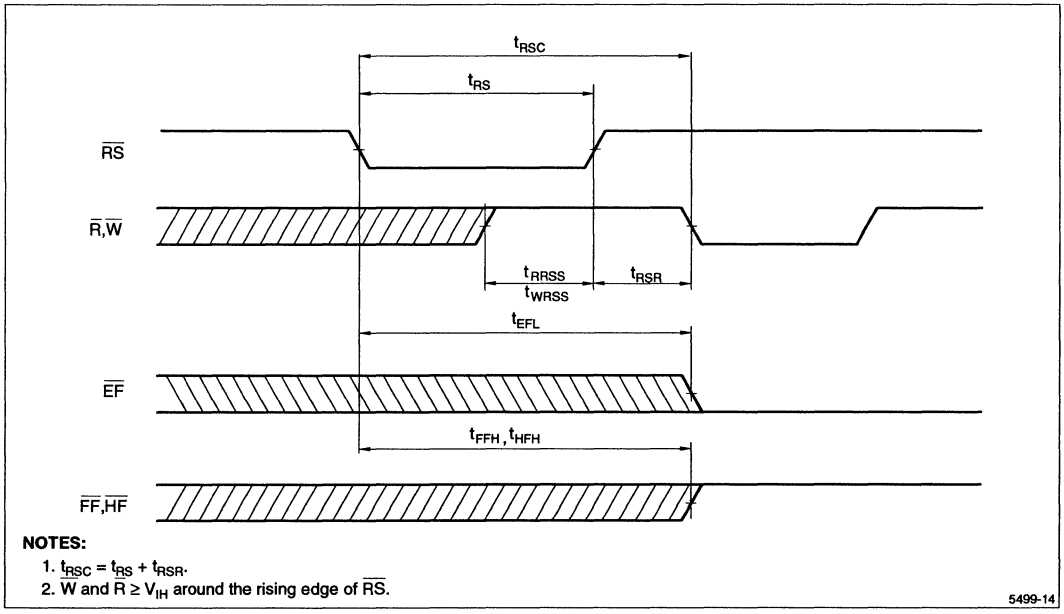


Figure 5. Reset Timing

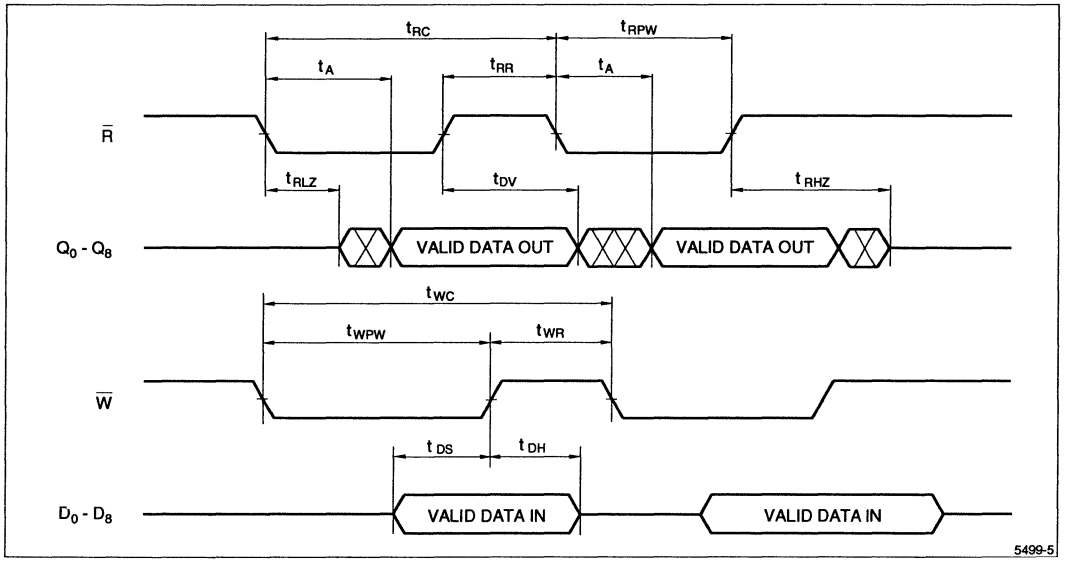


Figure 6. Asynchronous Write and Read Operation

TIMING DIAGRAMS (cont'd)

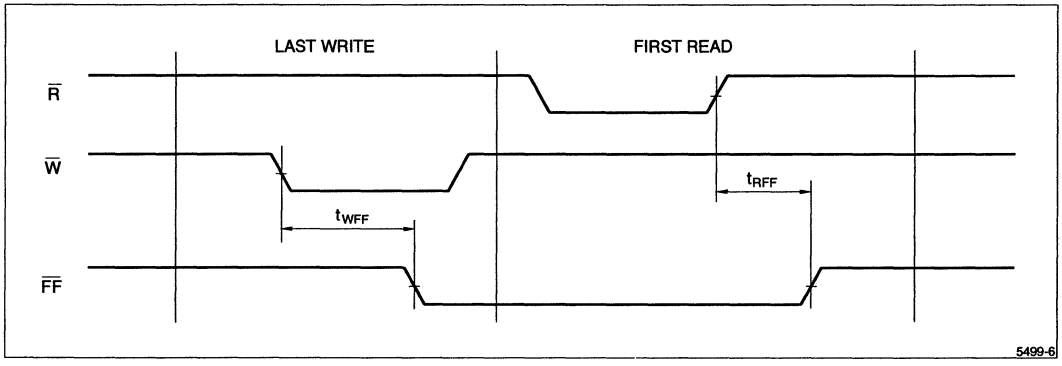


Figure 7. Full Flag from Last Write to First Read

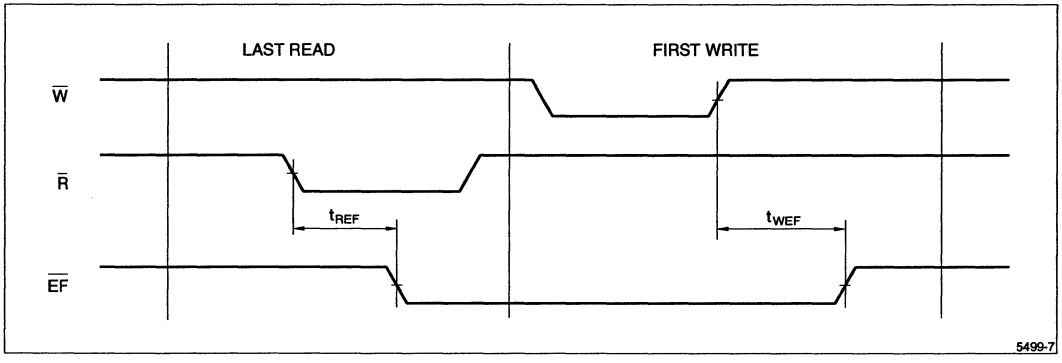


Figure 8. Empty Flag from Last Read to First Write

TIMING DIAGRAMS (cont'd)

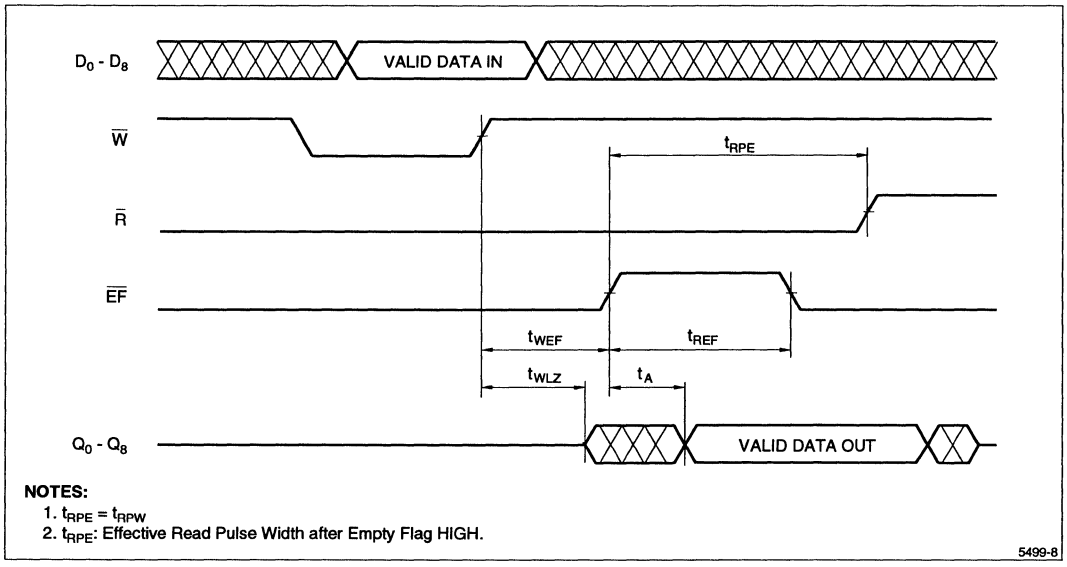


Figure 9. Read Data Flow-Through

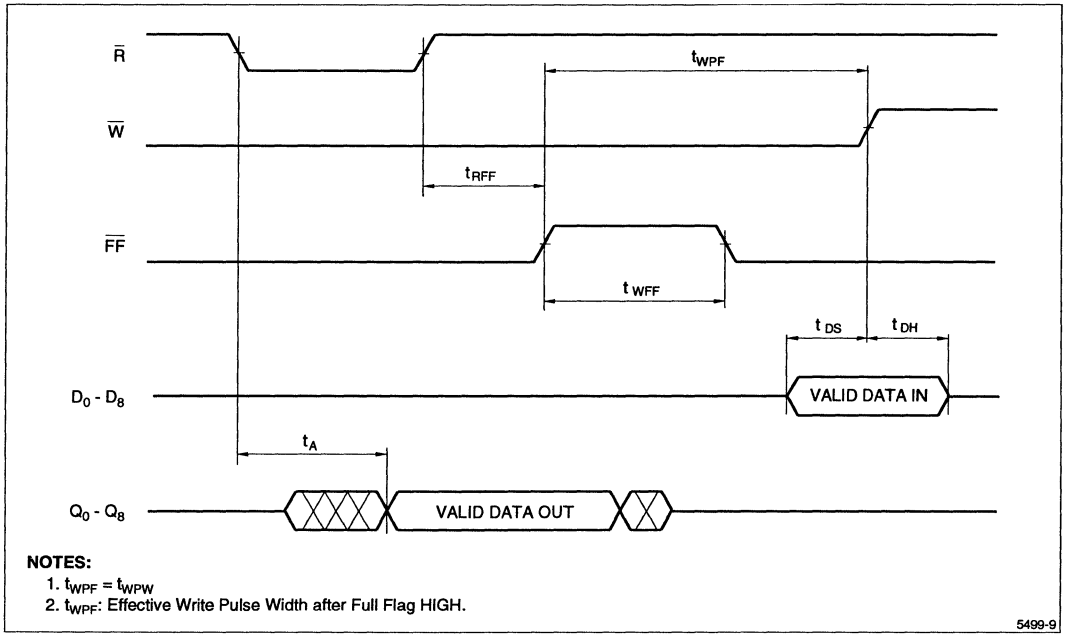


Figure 10. Write Data Flow-Through

TIMING DIAGRAMS (cont'd)

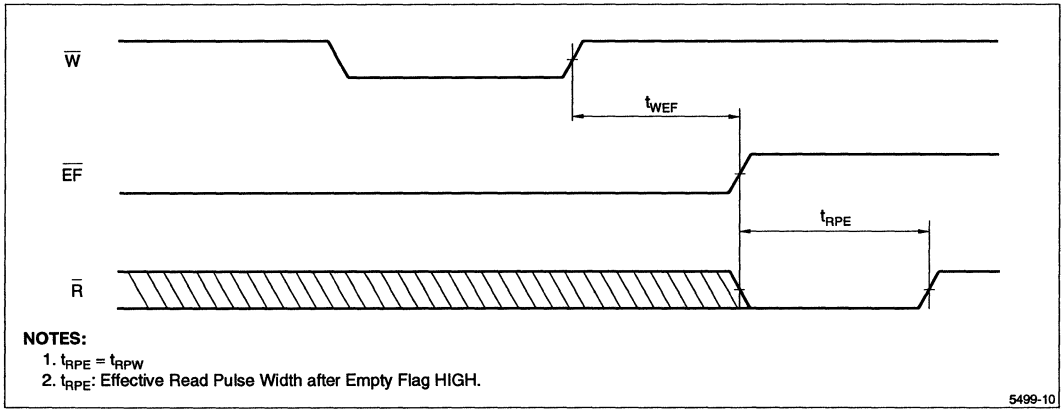


Figure 11. Empty Flag Timing

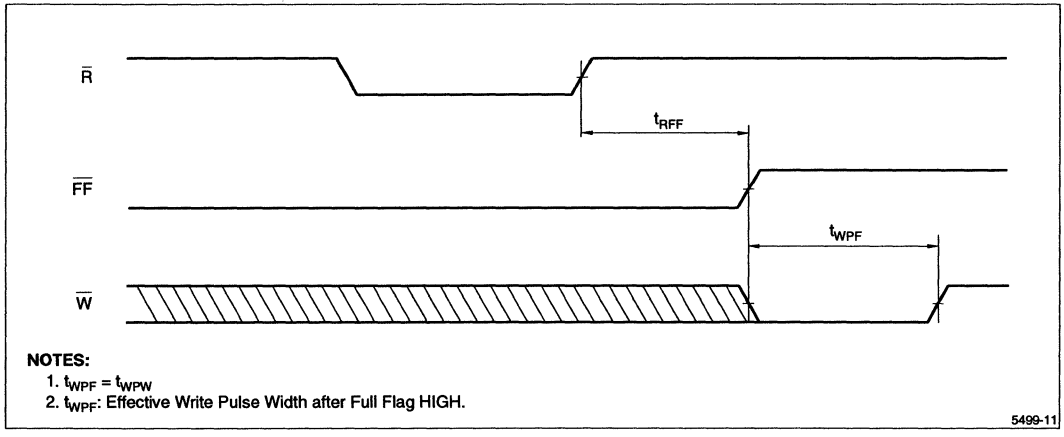


Figure 12. Full Flag Timing

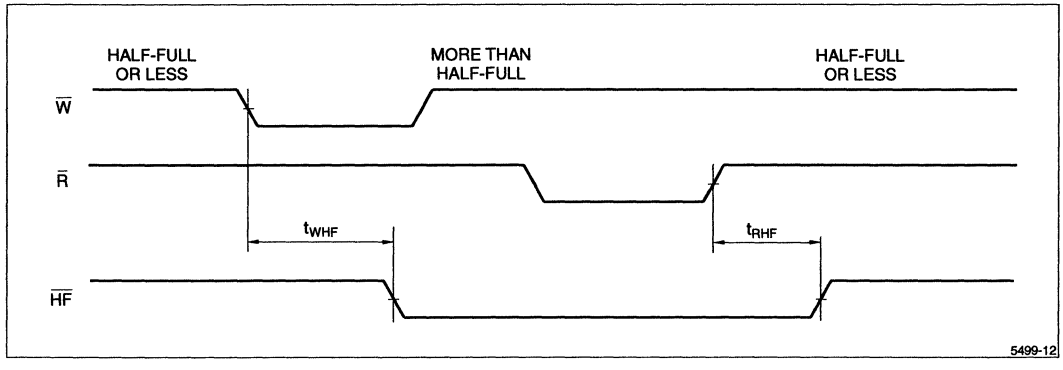


Figure 13. Half-Full Flag Timing

TIMING DIAGRAMS (cont'd)

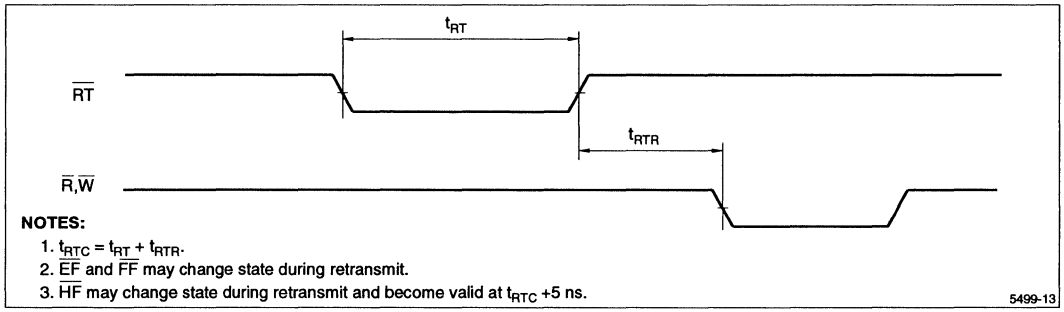


Figure 14. Retransmit Timing

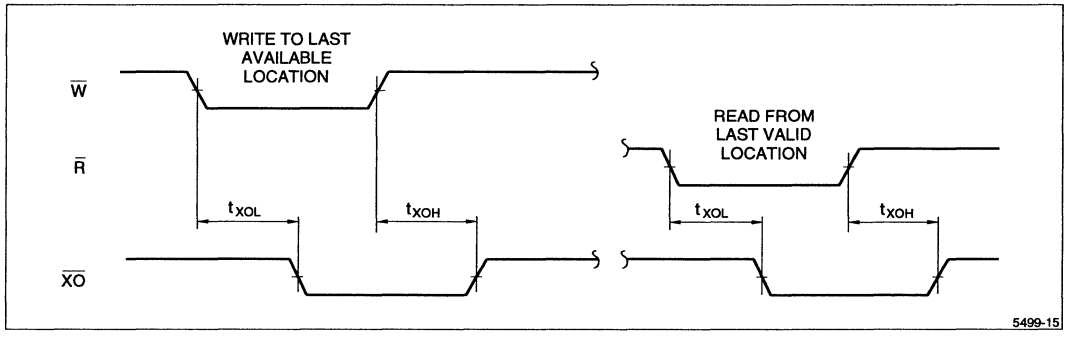


Figure 15. Expansion Out Timing

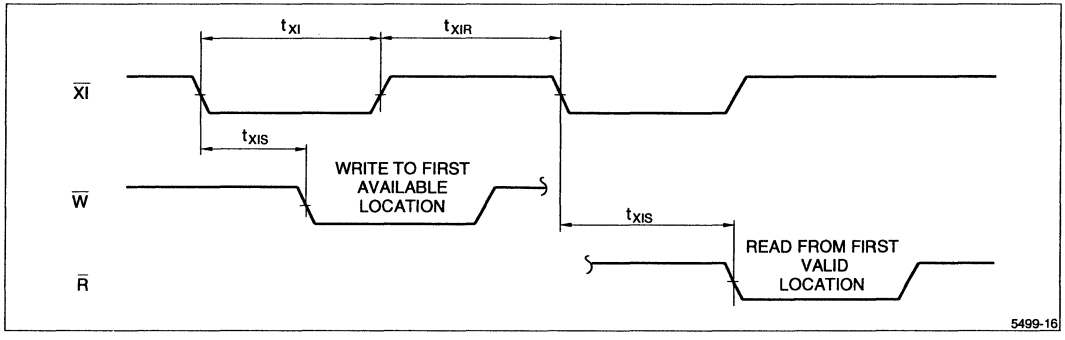


Figure 16. Expansion In Timing

OPERATIONAL MODES

Single Device Configuration

When depth expansion is not required for the given application, the device is placed in Single mode by tying the Expansion In pin ($\overline{XI}$) to ground. This pin is internally sampled during reset.

Width Expansion

Word-width expansion is implemented by placing multiple LH5499 devices in parallel. Each LH5499 should be configured for standalone mode. In this arrangement, the behavior of the status flags is identical for all devices; so, in principle, a representative value for each of these flags could be derived from any one device. In practice, it is better to derive 'composite' flag values using external logic, since there may be minor speed variations between different actual devices. (See Figures 17 and 18.)

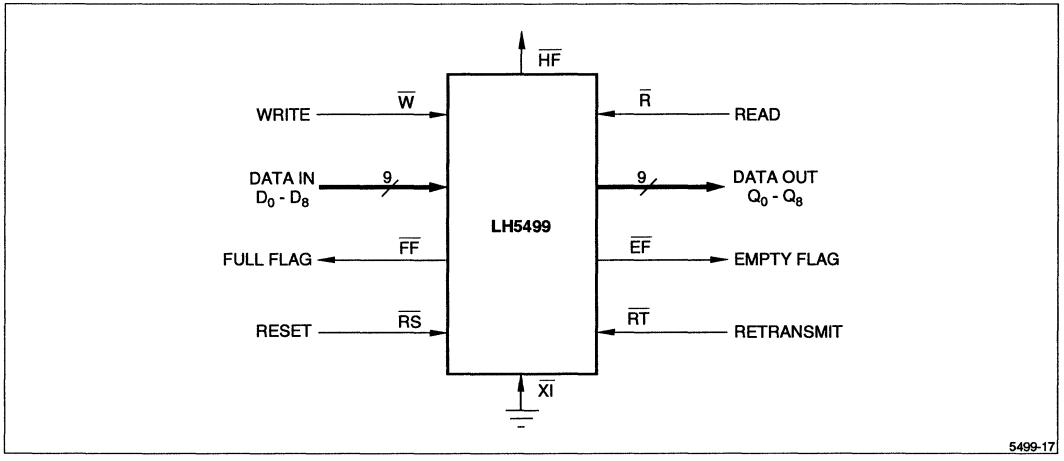


Figure 17. Single FIFO (4K × 9)

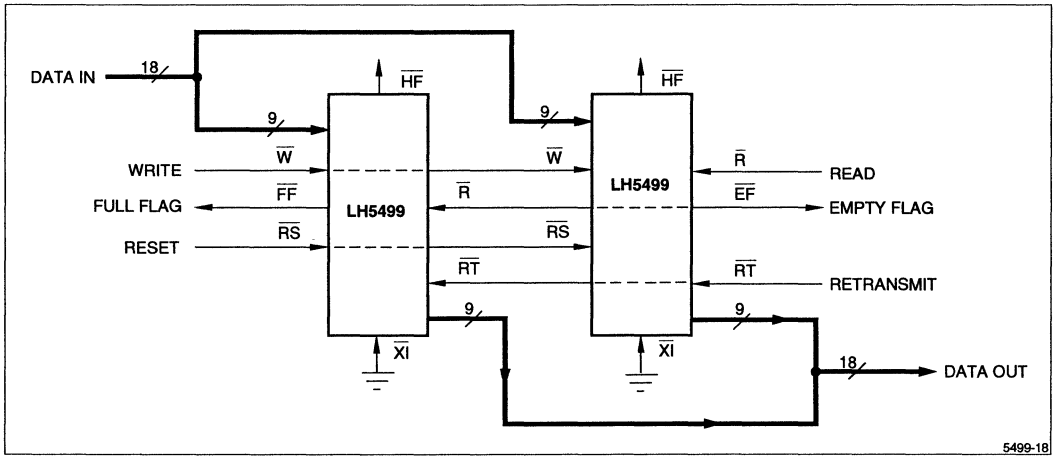


Figure 18. FIFO Width Expansion (4K × 18)

OPERATIONAL MODES (cont'd)

Depth Expansion

Depth expansion is implemented by configuring the required number of FIFOs in Expansion mode. In this arrangement, the FIFOs are connected in a circular fashion with the Expansion Out pin ($\overline{XO}$) of each device tied to the Expansion In pin ($\overline{XI}$) of the next device. One FIFO in this group must be designated as the first load device. This is accomplished by tying the First Load pin ($\overline{FL}$) of this device to ground. All other devices must have their $\overline{FL}$ pin tied to a high level. In this mode, $\overline{W}$ and $\overline{R}$ signals are shared by all devices, while internal logic controls the steering of data. Only one FIFO will be enabled for any given read cycle, so the common Data Out pins of all devices are wire-ORed together. Likewise, the common Data In pins of all devices are tied together.

In Expansion mode, external logic is required to generate a composite Full or Empty flag. This is achieved by ORing the $\overline{FF}$ pins of all devices and ORing the $\overline{EF}$ pins of all devices respectively. The Half-Full flag and Retransmit functions are not available in Depth Expansion mode.

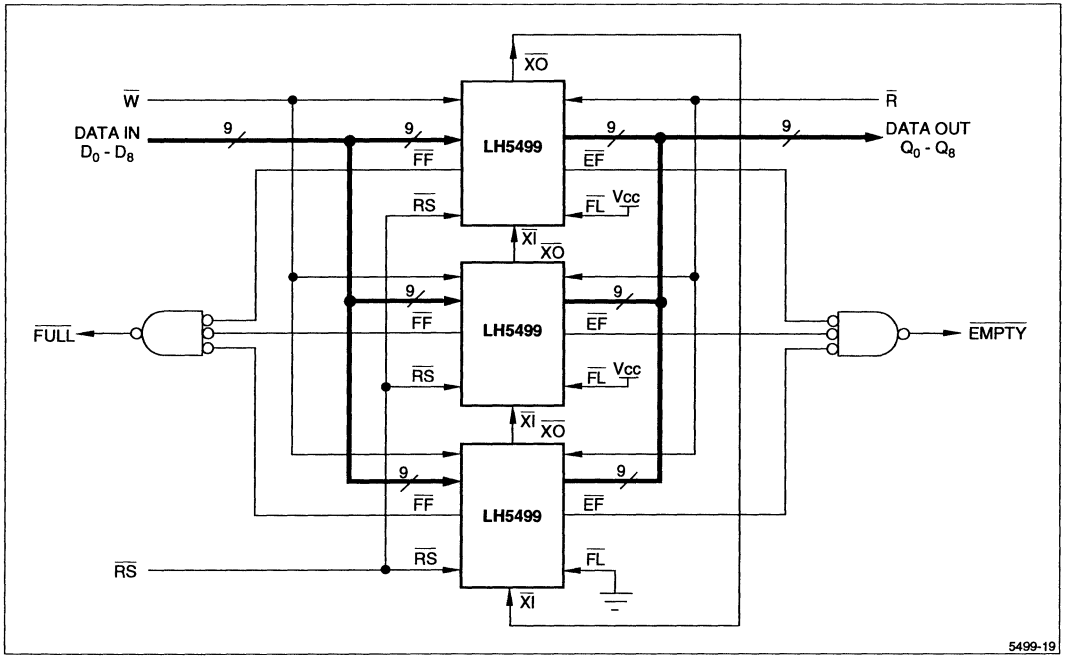


Figure 19. FIFO Depth Expansion (12288 × 9)

OPERATIONAL MODES (cont'd)

Compound Expansion

A combination of width and depth expansion can be easily implemented by operating groups of depth expanded FIFOs in parallel.

Bidirectional Operation

Applications which require bidirectional data buffering between two systems can be realized by operating LH5499 devices in parallel but opposite directions. The Data In pins of a device may be tied to the corresponding Data Out pins of another device operating in the opposite direction to form a single bidirectional bus interface. Care must be taken to assure that the appropriate read, write and flag signals are routed to each system. Both depth and width expansion may be used in this configuration.

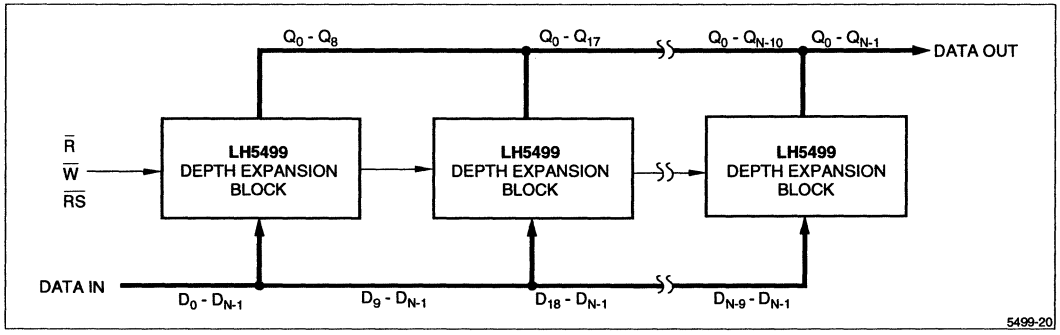


Figure 20. Compound FIFO

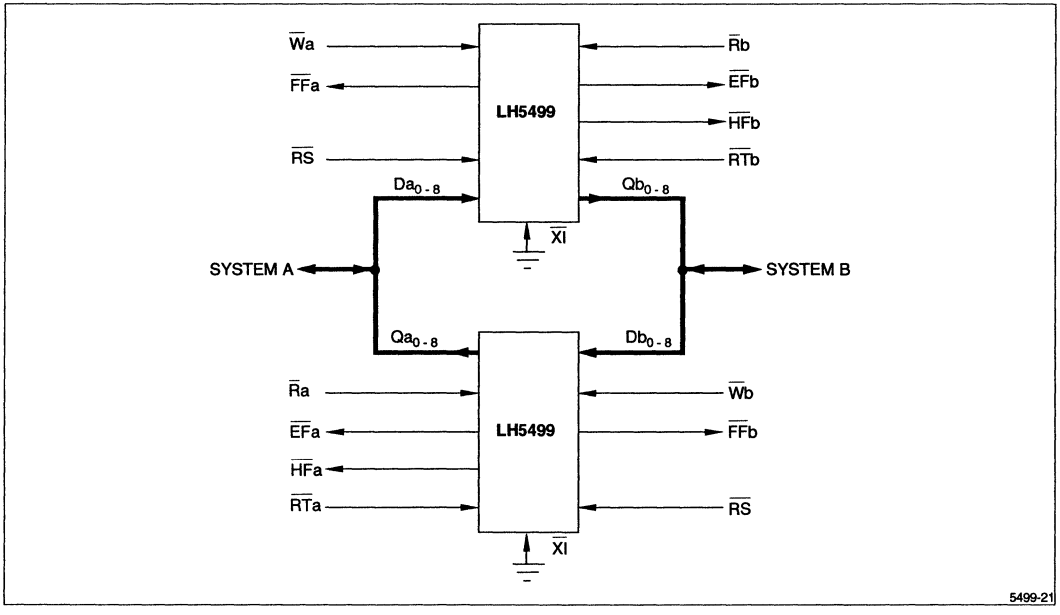
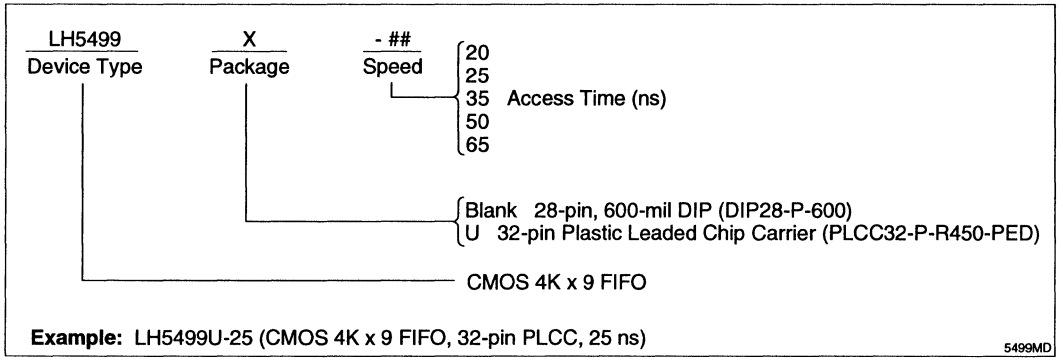


Figure 21. Bidirectional FIFO

ORDERING INFORMATION



LH5420

256 × 36 × 2 Bidirectional FIFO

FEATURES

- Fast Cycle Times: 25/30/35 ns
- Two 256 × 36-bit FIFO Buffers
- Full 36-bit Word Width
- Selectable 36/18/9-bit Word Width on Port B
- Independently-Synchronized ('Fully Asynchronous') Operation of Port A and Port B
- 'Synchronous' Enable-Plus-Clock Control at Both Ports
- R/$\overline{W}$, Enable, Request, and Address Control Inputs are Sampled on the Rising Clock Edge
- Synchronous Request/Acknowledge 'Handshake' Capability; Use is Optional
- Device Comes Up Into a Known Default State at Reset; Programming is Allowed, but is not Required
- Asynchronous Output Enables
- Five Status Flags per Port: Full, Almost-Full, Half-Full, Almost-Empty, and Empty
- Almost-Full Flag and Almost-Empty Flag are Programmable
- Mailbox Registers with Synchronized Flags
- Data-Bypass Function
- Data-Retransmit Function
- Automatic Byte Parity Checking
- TTL/CMOS-Compatible I/O
- Space-Saving PQFP and PGA Packages
- Mosel MS76542-SSFC is Pin-Compatible and Functionally Equivalent

FUNCTIONAL DESCRIPTION

The LH5420 contains two FIFO buffers, FIFO #1 and FIFO #2. These operate in parallel, but in opposite directions, for bidirectional data buffering. FIFO #1 and FIFO #2 each are organized as 256 words by 36 bits. The LH5420 is ideal either for wide unidirectional applications or for bidirectional data applications; component count and board area are reduced.

The LH5420 has two 36-bit ports, Port A and Port B. Each port has its own port-synchronous clock, but the two ports may operate asynchronously relative to each other. Data flow is initiated at a port by the rising edge of the appropriate clock; it is gated by the corresponding edge-sampled enable, request, and read/write control signals. At the maximum operating frequency, the clock duty cycle may vary from 40% to 60%. At lower frequencies, the clock waveform may be quite asymmetric, as long as the minimum pulse-width conditions for clock-HIGH and clock-LOW remain satisfied; the LH5420 is a fully-static part.

Conceptually, the port clocks CK_A and CK_B are free-running, periodic 'clock' waveforms, used to control other signals which are edge-sampled. However, there actually is not any absolute requirement that these 'clock' waveforms *must* be periodic. An 'asynchronous' mode of operation is possible, in one or both directions, independently, if the appropriate enable and request inputs are continuously asserted, and enough aperiodic 'clock' pulses of suitable duration are generated by external logic to cause all necessary actions to occur.

A synchronous request/acknowledge handshake facility is provided at each port for FIFO data access. This request/ acknowledge handshake resolves FIFO full and empty boundary conditions, when the two ports are operated asynchronously relative to each other.

FIFO status flags monitor the extent to which each FIFO buffer has been filled. Full, Almost-Full, Half-Full, Almost-Empty, and Empty flags are included for *each* FIFO. The Almost-Full and Almost-Empty flags are programmable over the entire FIFO depth, but are automatically initialized to eight locations from the respective FIFO boundaries at reset. A data block of 256 or fewer words may be retransmitted any desired number of times.

Two mailbox registers provide a separate path for passing control words or status words between ports. Each mailbox has a New-Mail-Alert Flag, which is synchronized to the reading port's clock. This mailbox function facilitates the synchronization of data transfers between asynchronous systems.

FUNCTIONAL DESCRIPTION (cont'd)

Data-bypass mode allows Port A to directly transfer data to or from Port B at reset. In this mode, the device acts as a registered transceiver under the control of Port A. For instance, a master processor on Port A can use the data bypass feature to send or receive initialization or configuration information directly, to or from a peripheral device on Port B, during system startup.

A word-width-select option is provided on Port B for 36-bit, 18-bit, or 9-bit data access. This feature allows word-width matching between Port A and Port B, with no additional logic needed. It also ensures maximum utilization of bus bandwidths.

A Byte Parity Check Flag at each port monitors data integrity. Control-Register bit 00 selects the parity mode, odd or even. This bit is initialized for odd data parity at reset; but it may be reprogrammed for even parity, or back again to odd parity, as desired.

PIN CONNECTIONS

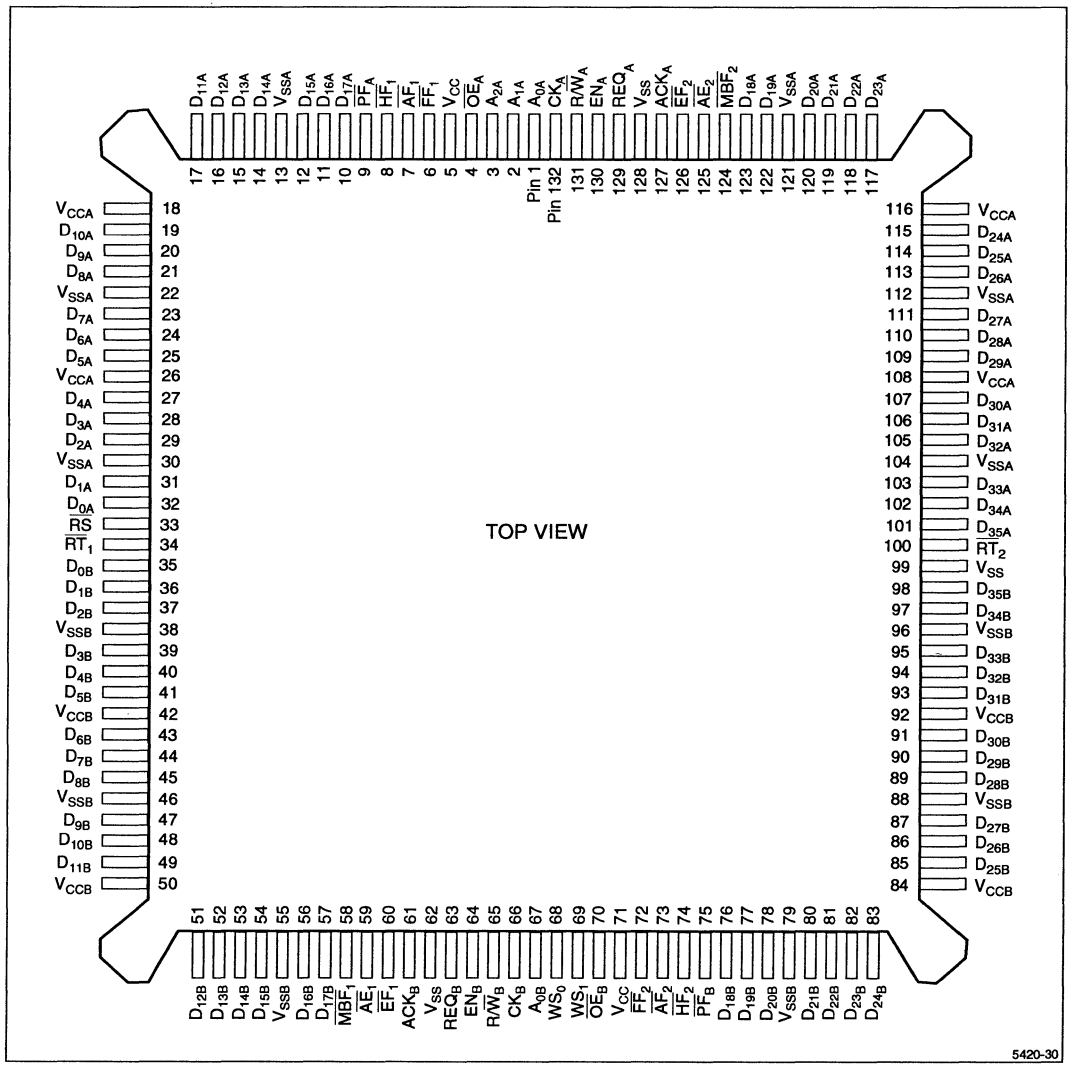
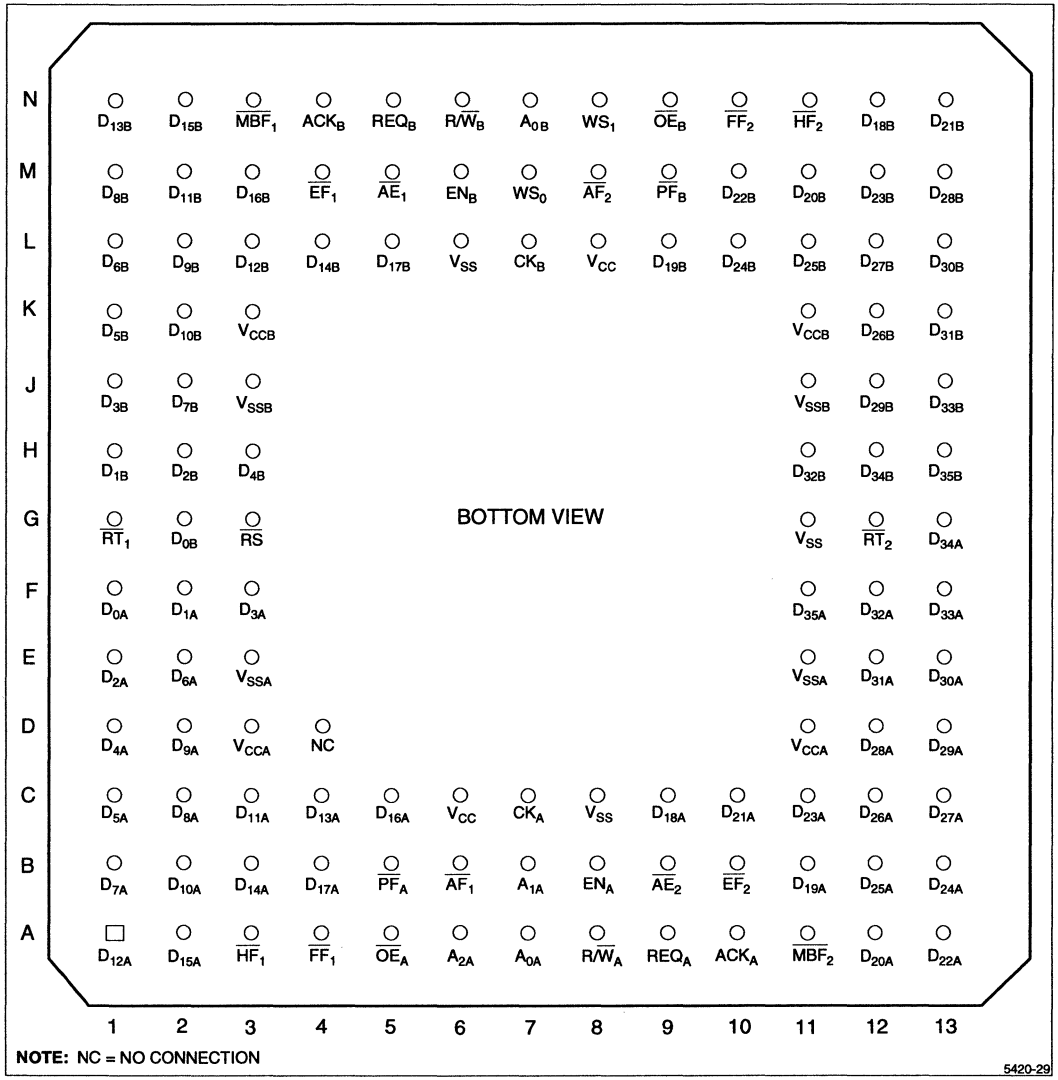


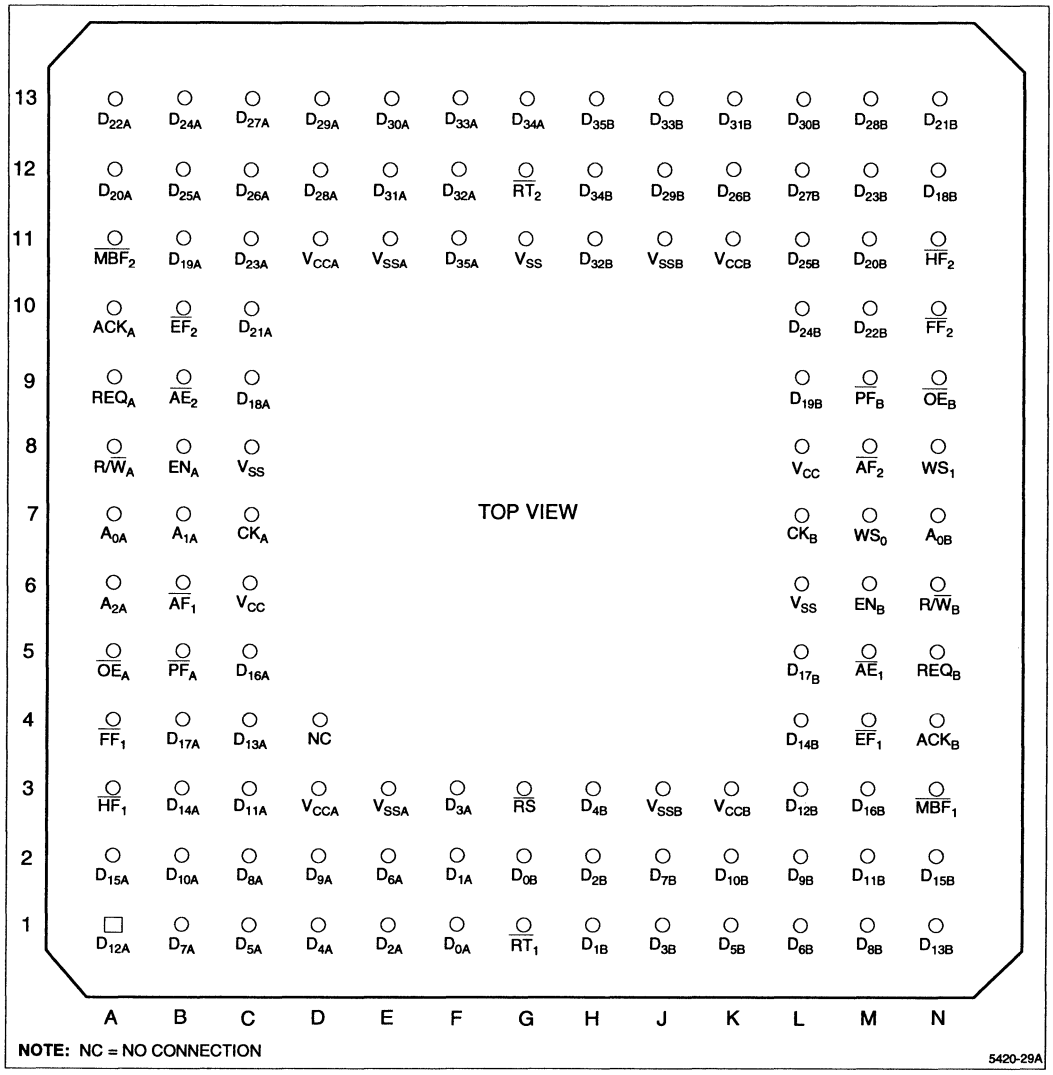
Figure 1. Pin Connections for 132-Pin Quad Flat Package (TOP VIEW)



NOTE: NC = NO CONNECTION

5420-29

Figure 2. Pin Connections for 120-Pin PGA Package (Bottom View)



NOTE: NC = NO CONNECTION

5420-29A

Figure 3. Pin Connections for 120-Pin PGA Package (Top View)

PIN LIST

SIGNAL NAME	PQFP PIN NO.	PGA PIN NO.
A_{0A}	1	A7
A_{1A}	2	B7
A_{2A}	3	A6
$\overline{OE}_A$	4	A5
$\overline{FF}_1$	6	A4
$\overline{AF}_1$	7	B6
$\overline{HF}_1$	8	A3
$\overline{PF}_A$	9	B5
D_{17A}	10	B4
D_{16A}	11	C5
D_{15A}	12	A2
D_{14A}	14	B3
D_{13A}	15	C4
D_{12A}	16	A1
D_{11A}	17	C3
D_{10A}	19	B2
D_{9A}	20	D2
D_{8A}	21	C2
D_{7A}	23	B1
D_{6A}	24	E2
D_{5A}	25	C1
D_{4A}	27	D1
D_{3A}	28	F3
D_{2A}	29	E1
D_{1A}	31	F2
D_{0A}	32	F1
$\overline{RS}$	33	G3
$\overline{RT}_1$	34	G1
D_{0B}	35	G2
D_{1B}	36	H1
D_{2B}	37	H2
D_{3B}	39	J1
D_{4B}	40	H3
D_{5B}	41	K1
D_{6B}	43	L1
D_{7B}	44	J2
D_{8B}	45	M1
D_{9B}	47	L2
D_{10B}	48	K2
D_{11B}	49	M2
D_{12B}	51	L3
D_{13B}	52	N1
D_{14B}	53	L4
D_{15B}	54	N2

SIGNAL NAME	PQFP PIN NO.	PGA PIN NO.
D_{16B}	56	M3
D_{17B}	57	L5
$\overline{MBF}_1$	58	N3
$\overline{AE}_1$	59	M5
$\overline{EF}_1$	60	M4
ACK_B	61	N4
REQ_B	63	N5
EN_B	64	M6
$R/\overline{W}_B$	65	N6
CK_B	66	L7
A_{0B}	67	N7
WS_0	68	M7
WS_1	69	N8
$\overline{OE}_B$	70	N9
$\overline{FF}_2$	72	N10
$\overline{AF}_2$	73	M8
$\overline{HF}_2$	74	N11
$\overline{PF}_B$	75	M9
D_{18B}	76	N12
D_{19B}	77	L9
D_{20B}	78	M11
D_{21B}	80	N13
D_{22B}	81	M10
D_{23B}	82	M12
D_{24B}	83	L10
D_{25B}	85	L11
D_{26B}	86	K12
D_{27B}	87	L12
D_{28B}	89	M13
D_{29B}	90	J12
D_{30B}	91	L13
D_{31B}	93	K13
D_{32B}	94	H11
D_{33B}	95	J13
D_{34B}	97	H12
D_{35B}	98	H13
$\overline{RT}_2$	100	G12
D_{35A}	101	F11
D_{34A}	102	G13
D_{33A}	103	F13
D_{32A}	105	F12
D_{31A}	106	E12
D_{30A}	107	E13
D_{29A}	109	D13

SIGNAL NAME	PQFP PIN NO.	PGA PIN NO.
D_{28A}	110	D12
D_{27A}	111	C13
D_{26A}	113	C12
D_{25A}	114	B12
D_{24A}	115	B13
D_{23A}	117	C11
D_{22A}	118	A13
D_{21A}	119	C10
D_{20A}	120	A12
D_{19A}	122	B11
D_{18A}	123	C9
$\overline{MBF}_2$	124	A11
$\overline{AE}_2$	125	B9
$\overline{EF}_2$	126	B10
ACK_A	127	A10
REQ_A	129	A9
EN_A	130	B8
$R/\overline{W}_A$	131	A8
CK_A	132	C7
V_{CC}	5	C6
V_{SSA}	13	E3
V_{CCA}	18	D3
V_{SSA}	22	E3
V_{CCA}	26	D3
V_{SSA}	30	E3
V_{SSB}	38	J3
V_{CCB}	42	K3
V_{SSB}	46	J3
V_{CCB}	50	K3
V_{SSB}	55	J3
V_{SS}	62	L6
V_{CC}	71	L8
V_{SSB}	79	J11
V_{CCB}	84	K11
V_{SSB}	88	J11
V_{CCB}	92	K11
V_{SSB}	96	J11
V_{SS}	99	G11
V_{SSA}	104	E11
V_{CCA}	108	D11
V_{SSA}	112	E11
V_{CCA}	116	D11
V_{SSA}	121	E11
V_{SS}	128	C8

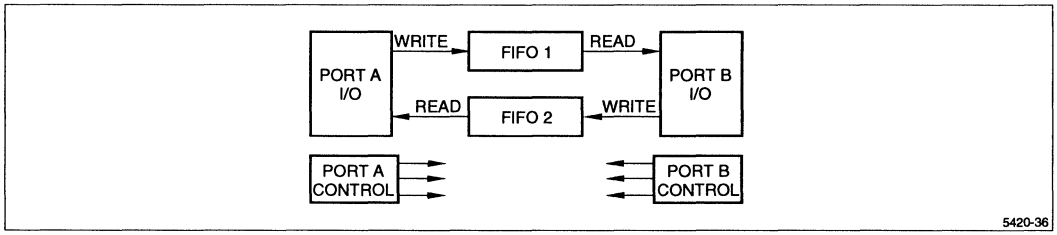


Figure 4a. Simplified LH5420 Block Diagram

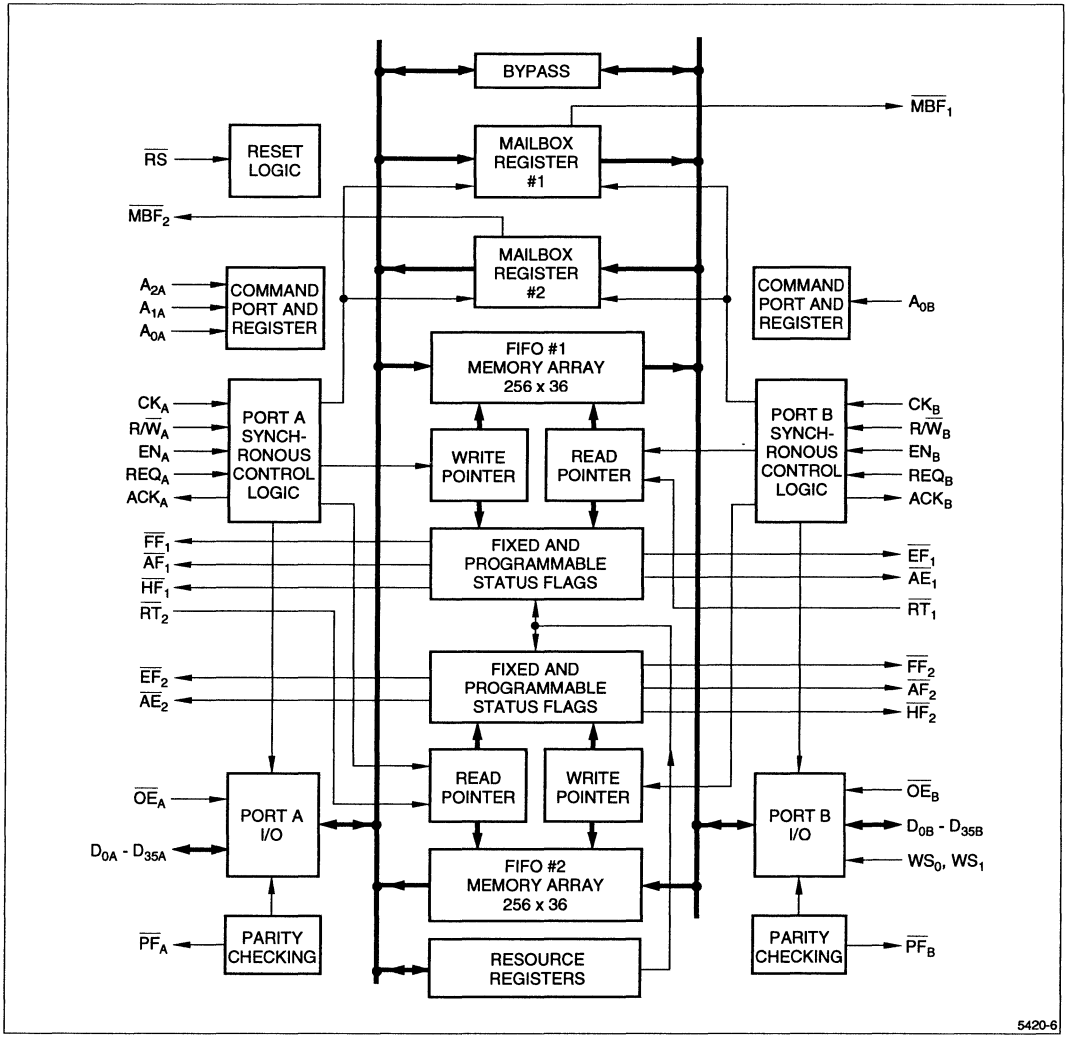


Figure 4b. Detailed LH5420 Block Diagram

PIN DESCRIPTIONS

PIN	PIN TYPE *	DESCRIPTION
		GENERAL
V_{CC}, V_{SS}	V	Power, Ground
$\overline{RS}$	I	Reset
		PORT A
CK_A	I	Port A Free-Running Clock
$R/\overline{W}_A$	I	Port A Edge-Sampled Read/Write Control
EN_A	I	Port A Edge-Sampled Enable
A_{0A}, A_{1A}, A_{2A}	I	Port A Edge-Sampled Address Pins
$\overline{OE}_A$	I	Port A Level-Sensitive Output Enable
REQ_A	I	Port A Request/Enable
$\overline{RT}_2$	I	FIFO #2 Retransmit
$D_{0A} - D_{35A}$	I/O/Z	Port A Bidirectional Data Bus
$\overline{FF}_1$	O	FIFO #1 Full Flag (Write Boundary)
$\overline{AF}_1$	O	FIFO #1 Programmable Almost-Full Flag (Write Boundary)
$\overline{HF}_1$	O	FIFO #1 Half-Full Flag
$\overline{AE}_2$	O	FIFO #2 Programmable Almost-Empty Flag (Read Boundary)
$\overline{EF}_2$	O	FIFO #2 Empty Flag (Read Boundary)
$\overline{MBF}_2$	O	New-Mail-Alert Flag for Mailbox #2
$\overline{PF}_A$	O	Port A Parity Flag
ACK_A	O	Port A Acknowledge
		PORT B
CK_B	I	Port B Free-Running Clock
$R/\overline{W}_B$	I	Port B Edge-Sampled Read/Write Control
EN_B	I	Port B Edge-Sampled Enable
A_{0B}	I	Port B Edge-Sampled Address Pin
$\overline{OE}_B$	I	Port B Level-Sensitive Output Enable
WS_0, WS_1	I	Port B Word-Width Select
REQ_B	I	Port B Request/Enable
$\overline{RT}_1$	I	FIFO #1 Retransmit
$D_{0B} - D_{35B}$	I/O/Z	Port B Bidirectional Data Bus
$\overline{FF}_2$	O	FIFO #2 Full Flag (Write Boundary)
$\overline{AF}_2$	O	FIFO #2 Programmable Almost-Full Flag (Write Boundary)
$\overline{HF}_2$	O	FIFO #2 Half-Full Flag
$\overline{AE}_1$	O	FIFO #1 Programmable Almost-Empty Flag (Read Boundary)
$\overline{EF}_1$	O	FIFO #1 Empty Flag (Read Boundary)
$\overline{MBF}_1$	O	New-Mail-Alert Flag for Mailbox #1
$\overline{PF}_B$	O	Port B Parity Flag
ACK_B	O	Port B Acknowledge

* I = Input, O = Output, Z = High-Impedance, V = Power Voltage Level

ABSOLUTE MAXIMUM RATINGS [1]

PARAMETER	RATING
Supply Voltage to V_{SS} Potential	−0.5 V to 7 V
Signal Pin Voltage to V_{SS} Potential [3]	−0.5 V to V_{CC} + 0.5 V
DC Output Current [2]	± 40 mA
Storage Temperature Range	−65°C to 150°C
Power Dissipation (Package Limit)	2 Watts (Quad Flat Pack)

NOTES:

1. Stresses greater than those listed under 'Absolute Maximum Ratings' may cause permanent damage to the device. This is a stress rating for transient conditions only. Functional operation of the device at these or any other conditions outside those indicated in the 'Operating Range' of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Outputs should not be shorted for more than 30 seconds. No more than one output should be shorted at any time.
3. Negative undershoot of 1.5 V in amplitude is permitted for up to 10 ns, once per cycle.

OPERATING RANGE

SYMBOL	PARAMETER	MIN	MAX	UNIT
T_A	Temperature, Ambient	0	70	°C
V_{CC}	Supply Voltage	4.5	5.5	V
V_{SS}	Supply Voltage	0	0	V
V_{IL}	Logic LOW Input Voltage [1]	−0.5	0.8	V
V_{IH}	Logic HIGH Input Voltage	2.2	Vcc + 0.5	V

NOTE:

1. Negative undershoot of 1.5 V in amplitude is permitted for up to 10 ns, once per cycle.

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
I_{LI}	Input Leakage Current	V_{CC} = 5.5 V, V_{IN} = 0 V To V_{CC}	−10	10	µA
I_{LO}	I/O Leakage Current	$\overline{OE} \geq V_{IH}$, 0 V ≤ $V_{OUT} \leq V_{CC}$	−10	10	µA
V_{OL}	Logic LOW Output Voltage	I_{OL} = 8.0 mA		0.4	V
V_{OH}	Logic HIGH Output Voltage	I_{OH} = −2.0 mA	2.4		V
I_{CC}	Average Supply Current [1]	Measured at f_C = max		280	mA
I_{CC2}	Average Standby Supply Current [1]	All Inputs = V_{IHMIN} (Clock idle)		30	mA
I_{CC3}	Power-Down Supply Current [1]	All Inputs = V_{CC} − 0.2 V (Clock idle)		3	mA

NOTE:

1. I_{CC}, I_{CC2}, and I_{CC3} are dependent upon actual output loading, and I_{CC} is also dependent on cycle rates. Specified values are with outputs open; and, for I_{CC}, operating at minimum cycle times.

AC TEST CONDITIONS

PARAMETER	RATING
Input Pulse Levels	V_{SS} to 3 V
Input Rise and Fall Times (10% to 90%)	5 ns
Output Reference Levels	1.5 V
Input Timing Reference Levels	1.5 V
Output Load, Timing Tests	Figure 5

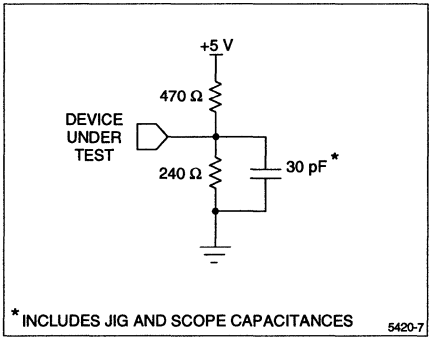


Figure 5. Output Load Circuit

CAPACITANCE [1,2]

PARAMETER	RATING
C_{IN} (Input Capacitance)	8 pF
C_{OUT} (Output Capacitance)	8 pF

NOTES:

1. Sample tested only.
2. Capacitances are maximum values at 25°C, measured at 1.0 MHz, with V_{IN} = 0 V.

AC ELECTRICAL CHARACTERISTICS [1] (V_{CC} = 5 V ± 10%, T_A = 0°C to 70°C)

SYMBOL	DECRIPTION	-25		-30		-35		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	
f_{CC}	Clock Cycle Frequency	—	40	—	33	—	28.5	MHz
t_{CC}	Clock Cycle Time	25	—	30	—	35	—	ns
t_{CH}	Clock HIGH Time	10	—	12	—	15	—	ns
t_{CL}	Clock LOW Time	10	—	12	—	15	—	ns
t_{DS}	Data Setup Time	12	—	13	—	15	—	ns
t_{DH}	Data Hold Time	0	—	0	—	0	—	ns
t_{ES}	Enable Setup Time	13	—	15	—	15	—	ns
t_{EH}	Enable Hold Time	0	—	0	—	0	—	ns
t_{RWS}	Read/Write Setup Time	13	—	15	—	18	—	ns
t_{RWH}	Read/Write Hold Time	0	—	0	—	0	—	ns
t_{RQS}	Request Setup Time	15	—	18	—	21	—	ns
t_{RQH}	Request Hold Time	0	—	0	—	0	—	ns
t_{AS}	Address Setup Time [6]	15	—	18	—	21	—	ns
t_{AH}	Address Hold Time [6]	0	—	0	—	0	—	ns
t_A	Data Output Access Time	—	16	—	20	—	25	ns
t_{ACK}	Acknowledge Access Time [8]	—	—	—	20	—	25	ns
t_{OH}	Output Hold Time	4	—	5	—	5	—	ns
t_{ZX}	Output Enable Time, $\overline{OE}$ LOW to $D_0 - D_{35}$ Low-Z [2]	5	—	5	—	5	—	ns
t_{XZ}	Output Disable Time, $\overline{OE}$ HIGH to $D_0 - D_{35}$ High-Z [2]	—	15	—	20	—	25	ns
t_{EF}	Clock to $\overline{EF}$ Flag Valid (Empty Flag)	—	22	—	25	—	30	ns
t_{FF}	Clock to $\overline{FF}$ Flag Valid (Full Flag)	—	22	—	25	—	30	ns
t_{HF}	Clock to $\overline{HF}$ Flag Valid (Half-Full)	—	22	—	25	—	30	ns
t_{AE}	Clock to $\overline{AE}$ Flag Valid (Almost-Empty)	—	20	—	25	—	30	ns
t_{AF}	Clock to $\overline{AF}$ Flag Valid (Almost-Full)	—	20	—	25	—	30	ns
t_{MBF}	Clock to $\overline{MBF}$ Flag Valid (Mailbox Flag)	—	15	—	20	—	25	ns
t_{PF}	Data to Parity Flag Valid	—	17	—	20	—	25	ns
t_{RS}	Reset/Retransmit Pulse Width [7]	40/25	—	52/30	—	65/35	—	ns
t_{RSS}	Reset/Retransmit Setup Time [3]	20	—	25	—	30	—	ns
t_{RSH}	Reset/Retransmit Hold Time [3]	10	—	15	—	20	—	ns
t_{RF}	Reset LOW to Flag Valid	—	35	—	40	—	45	ns
t_{FRL}	First Read Latency [4]	25	—	30	—	35	—	ns
t_{FWL}	First Write Latency [5]	25	—	30	—	35	—	ns
t_{BS}	Bypass Data Setup	15	—	18	—	21	—	ns
t_{BH}	Bypass Data Hold	5	—	5	—	5	—	ns
t_{BA}	Bypass Data Access	—	20	—	25	—	30	ns

NOTES:

1. Timing measurements performed at 'AC Test Condition' levels.
2. Values are guaranteed by design; not currently production tested.
3. t_{RSS} and/or t_{RSH} need not be met unless a rising edge of CK_A occurs while EN_A is being asserted, or else a rising edge of CK_B occurs while EN_B is being asserted.
4. t_{FRL} is the minimum first-write-to-first-read delay, following an empty condition, which is required to assure valid read data.
5. t_{FWL} is the minimum first-read-to-first-write delay, following a full condtion, which is required to assure successful writing of data.
6. t_{AS}, t_{AH} address setup times and hold times need only be satisfied at clock edges which occur while the corresponding enables are being asserted.
7. First number used only when CK_A or CK_B is enabled; $t_{RS} = t_{RSS} + t_{CH} + t_{RSH}$.
8. The REQ/ACK facility is not available at cycle times less than 30 ns.

OPERATIONAL DESCRIPTION

Reset

The device is reset whenever the asynchronous Reset ($\overline{RS}$) input is taken LOW. A reset operation is required after power-up, before the first write operation may occur. The LH5420 is fully ready for operation after being reset. No device programming is required if the default states described below are acceptable.

A reset operation initializes the read-address and write-address pointers for FIFO #1 and FIFO #2 to those FIFO's first physical memory locations. If the respective outputs are enabled, the initial contents of these first locations appear at the outputs. FIFO and mailbox status flags are updated to indicate an empty condition. In addition, the programmable-status-flag offset values are initialized to eight. Thus, the $\overline{AE}_1/\overline{AE}_2$ flags get asserted within eight locations of an empty condition, and the $\overline{AF}_1/\overline{AF}_2$ flags likewise get asserted within eight locations of a full condition, for FIFO #1/FIFO #2 respectively.

Bypass Operation

During reset (whenever $\overline{RS}$ is LOW) the device acts as a registered transceiver, bypassing the internal FIFO memories. Port A acts as the master port. A write or read operation on Port A during reset transfers data directly to or from Port B. Port B is considered to be the slave, and cannot perform write or read operations independently on its own during reset.

The direction of the bypass data transmission is determined by th $R/\overline{W}_A$ control input, which does not get overridden by the $\overline{RS}$ input. Here, a 'write' operation means passing data from Port A to Port B, and a 'read' operation means passing data from Port B to Port A.

The bypass capability may be used to pass initialization or configuration data directly between a master processor and a peripheral device during reset.

Address Modes

Address pins select the device resource to be accessed by each port. Port A has three resource-register-select inputs, A_{0A}, A_{1A}, and A_{2A}, which select between FIFO access, mailbox-register access, and flag-offset-value-programming operating mode. Port B has a single address input, A_{0B}, to select between FIFO access or mailbox-register access.

The status of the resource-register-select inputs is sampled at the rising edge of an enabled clock (CK_A or CK_B). Resource-register select-input address definitions are summarized in Table 1.

Table 1. Resource-Register Addresses

A_{2A}	A_{1A}	A_{0A}	RESOURCE
PORT A			
H	H	H	FIFO
H	H	L	Mailbox
H	L	H	$\overline{AF}_2$, $\overline{AE}_2$, $\overline{AF}_1$, $\overline{AE}_1$ Flag Offset Registers
H	L	L	Control Register
L	H	H	$\overline{AE}_1$ Flag Offset Register
L	H	L	$\overline{AF}_1$ Flag Offset Register
L	L	H	$\overline{AE}_2$ Flag Offset Register
L	L	L	$\overline{AF}_2$ Flag Offset Register
A_{0B}			RESOURCE
PORT B			
H			FIFO
L			Mailbox

FIFO Write

Port A writes to FIFO #1, and Port B writes to FIFO #2. A write operation is initiated on the rising edge of a clock (CK_A or CK_B) whenever: the appropriate enable (EN_A or EN_B) is held HIGH; the appropriate request (REQ_A or REQ_B) is held HIGH; the appropriate Read/Write control ($R/\overline{W}_A$ or $R/\overline{W}_B$) is held LOW; the FIFO address is selected for the address inputs ($A_{2A} - A_{0A}$ or A_{0B}); and the prescribed setup times and hold times are observed for all of these signals. Setup times and hold times must also be observed on the data-bus pins ($D_{0A} - D_{35A}$ or $D_{0B} - D_{35B}$).

Normally, the appropriate Output Enable signal ($\overline{OE}_A$ or $\overline{OE}_B$) is HIGH, to disable the outputs at that port, so that the data word present on the bus from external sources gets stored. However, a 'loopback' mode of operation also is possible, in which the data word supplied by the outputs of one internal FIFO is 'turned around' at the port and read back into the other FIFO. In this mode, the outputs at the port are not disabled. To remain within specification for all timing parameters, the Clock Cycle Frequency must be reduced slightly below the value which otherwise would be permissible for that speed grade of LH5420.

When a FIFO full condition is reached, write operations are locked out. Following the first read operation from a full FIFO, another memory location is freed up, and the corresponding Full Flag is deasserted ($\overline{FF}$ = HIGH). The first write operation should begin no earlier than a First Write Latency (t_{FWL}) after the first read operation from a full FIFO, to ensure that correct read data are retrieved.

OPERATIONAL DESCRIPTION (cont'd)

FIFO Read

Port A reads from FIFO #2, and Port B reads from FIFO #1. A read operation is initiated on the rising edge of a clock (CK_A or CK_B) whenever: the appropriate enable (EN_A or EN_B) is held HIGH; the appropriate request (REQ_A or REQ_B) is held HIGH; the appropriate Read/Write control ($R/\overline{W}_A$ or $R/\overline{W}_B$) is held HIGH; the FIFO address is selected for the address inputs ($A_{2A} - A_{0A}$ or A_{0B}); and the prescribed setup times and hold times are observed for all of these signals. Read data becomes valid on the data-bus pins ($D_{0A} - D_{35A}$ or $D_{0B} - D_{35B}$) by a time t_A after the rising clock (CK_A or CK_B) edge, provided that the data outputs are enabled.

$\overline{OE}_A$ and $\overline{OE}_B$ are assertive-LOW, asynchronous, Output Enable control input signals. Their effect is only to enable or disable the output drivers of the respective port. Disabling the outputs does *not* disable a read operation; data transmitted to the corresponding output register will remain available later, when the outputs again are enabled, unless it subsequently is overwritten.

When an empty condition is reached, read operations are locked out until a valid write operation(s) has loaded additional data into the FIFO. Following the first write to an empty FIFO, the corresponding empty flag ($\overline{EF}$) will be deasserted (HIGH). The first read operation should begin no earlier than a First Read Latency (t_{FRL}) after the first write to an empty FIFO, to ensure that correct read data is retrieved.

Dedicated FIFO Status Flags

Six dedicated FIFO status flags are included for Full ($\overline{FF}_1$ and $\overline{FF}_2$), Half-Full ($\overline{HF}_1$ and $\overline{HF}_2$), and Empty ($\overline{EF}_1$ and $\overline{EF}_2$). $\overline{FF}_1$, $\overline{HF}_1$, and $\overline{EF}_1$ indicate the status of FIFO #1; and $\overline{FF}_2$, $\overline{HF}_2$, and $\overline{EF}_2$ indicate the status of FIFO #2.

A Full Flag is asserted following the rising clock edge for a write operation that fills the FIFO. A Full Flag is deasserted following the falling clock edge for a read operation to a full FIFO. A Half-Full Flag is updated following the rising clock edge of a read or write operation to a FIFO. An Empty Flag is asserted following the rising clock edge for a read operation that empties the FIFO. An Empty Flag is deasserted following the falling clock edge for a write operation to an empty FIFO.

Programmable Status Flags

Four programmable FIFO status flags are provided, two for Almost-Full ($\overline{AF}_1$ and $\overline{AF}_2$), and two for Almost-Empty ($\overline{AE}_1$ and $\overline{AE}_2$). Thus, each port has two programmable flags to monitor the status of the two internal FIFO buffer memories. The offset values for these flags are initialized to eight locations from the respective FIFO boundaries during reset, but can be reprogrammed over the entire FIFO depth.

An Almost-Full Flag is asserted following the rising clock edge for a write operation that fills the FIFO. An Almost-Full Flag is deasserted following the falling clock edge for a read operation to a full FIFO. An Almost-Empty Flag is asserted following the rising clock edge for a read operation that empties the FIFO. An Almost-Empty Flag is deasserted following the falling clock edge for a write operation to an empty FIFO.

Flag offsets may be written or read through the Port A data bus. All four programmable FIFO status flag offsets can be set simultaneously through a single 36-bit status word; or, each programmable flag offset can be set individually, through one of four eight-bit status words. Table 3 illustrates the data format for flag-programming words, and Table 4 defines the meaning of each of the five flags.

WARNING: Control inputs which may affect the computation of flag values at a port generally should not change while the clock for that port is HIGH, since some updating of flag values takes place on the *falling* edge of the clock.

Mailbox Operation

Two mailbox registers are provided for passing system hardware or software control/status words between ports. Each port can read its own mailbox and write to the other port's mailbox. Mailbox access is performed on the rising edge of the controlling FIFO's clock, with the mailbox address selected and the enable (EN_A or EN_B) HIGH. That is, writing to Mailbox Register #1, or reading from Mailbox Register #2, is synchronized to CK_A; and writing to Mailbox Register #2, or reading from Mailbox Register #1, is synchronized to CK_B.

The $R/\overline{W}_{A/B}$ and $\overline{OE}_{A/B}$ pins control the direction and availability of mailbox-register accesses. Each mailbox register has its own New-Mail-Alert Flag ($\overline{MBF}_1$ and $\overline{MBF}_2$), which is synchronized to the reading port's clock. These New-Mail-Alert Flags are status indicators only, and cannot inhibit mailbox-register read or write operations.

Request/Acknowledge Handshake

Synchronous, request/acknowledge handshake feature is provided for each port, to perform boundary synchronization between asynchronously-operated ports. It operates only during normal FIFO operation at that port. The use of this feature is optional. When it is used, the Request input ($REQ_{A/B}$) is sampled at a rising clock edge. With $REQ_{A/B}$ HIGH, $R/\overline{W}_{A/B}$ determines whether a FIFO read operation or a FIFO write operation is being requested. The Acknowledge output ($ACK_{A/B}$) is updated during the following clock cycle(s). $ACK_{A/B}$ meets the setup and hold time requirements of the Enable input (EN_A or EN_B). Therefore, $ACK_{A/B}$ may be tied back to the enable input to directly gate FIFO accesses, at a slight decrease in maximum operating frequency.

The assertion of $ACK_{A/B}$ signifies that $REQ_{A/B}$ was asserted. However, $ACK_{A/B}$ does not depend logically on $EN_{A/B}$; and thus the assertion of $ACK_{A/B}$ does *not* prove that a FIFO write access or a FIFO read access actually took place. While $REQ_{A/B}$ and $EN_{A/B}$ are being held

OPERATIONAL DESCRIPTION (cont'd)

HIGH, $ACK_{A/B}$ may be considered as a synchronous, predictive boundary flag. That is, $ACK_{A/B}$ acts as a synchronized predictor of the Almost-Full Flag $\overline{AF}$ for write operations, or as a synchronized predictor of the Almost-Empty Flag $\overline{AE}$ for read operations.

Outside the 'almost-full' region and the 'almost-empty' region, $ACK_{A/B}$ remains continuously HIGH whenever $REQ_{A/B}$ is held continuously HIGH. Within the 'almost-full' region or the 'almost-empty' region, $ACK_{A/B}$ occurs only on every *third* cycle. Assuming that $ACK_{A/B}$ is being used to control $EN_{A/B}$, this repetition-rate decrease can help to prevent an overrun of the FIFO's actual full or empty boundaries, and to ensure that the t_{FWL} (first write latency) and t_{FRL} (first read latency) specifications are satisfied before $ACK_{A/B}$ is received.

The 'almost-full region' is defined as 'that region, where the Almost-Full Flag is being asserted'; and the 'almost-empty region' as 'that region, where the Almost-Empty Flag is being asserted.' Thus, the extent of these 'almost' regions depends on how the system has programmed the offset values for the Almost-Full Flags and the Almost-Empty Flags. If the system has *not* programmed them, then these offset values remain at their default values, eight in each case.

If a write attempt is unsuccessful because the corresponding FIFO is full, or if a read attempt is unsuccessful because the corresponding FIFO is empty, $ACK_{A/B}$ is *not* asserted in response to $REQ_{A/B}$.

If the REQ/ACK handshake is not used, then the $REQ_{A/B}$ input may be used as a second enable input, at a possible minor loss in maximum operating speed. In this case, the $ACK_{A/B}$ output may be ignored.

WARNING: Whether or not the REQ/ACK handshake is being used, the $REQ_{A/B}$ input for a port *must* be asserted for the corresponding FIFO to operate.

Data Retransmit

A retransmit operation resets the read-address pointer of the corresponding FIFO (#1 or #2) back to the first FIFO physical memory location, so that data may be reread. The write pointer is not affected. The status flags are updated; and a block of up to 256 data words, which previously had been written into and read from a FIFO, can be retrieved. The block to be retransmitted is bounded by the first FIFO memory location, and the FIFO memory location addressed by the write pointer. FIFO #1 retransmit is initiated by strobing the $\overline{RT}_1$ pin LOW. FIFO #2 retransmit is initiated by strobing the $\overline{RT}_2$ pin LOW. Read and write operations to a FIFO should be stopped while the corresponding Retransmit signal is being asserted.

Parity Check

The Parity Check Flags, $\overline{PF}_A$ and $\overline{PF}_B$, are asserted (LOW) whenever there is a parity error in the data word present on the Port A data bus or the Port B data bus respectively. The inputs to the parity-evaluation logic come directly (via isolation transistors) from the data-bus bonding *pads*, in each case.

The four bytes of a 36-bit data word are grouped as $D_0 - D_8$, $D_9 - D_{17}$, $D_{18} - D_{26}$, and $D_{27} - D_{35}$. The parity of each nine-bit byte is individually checked, and the four single-bit parity indications are logically inclusive-ORed to produce the Parity-Flag output. Parity checking is initialized for odd parity at reset, but can be reprogrammed for even parity or for odd parity during operation.

All nine bits of each byte are treated alike by the parity logic. The byte parity over the nine bits is compared with the Parity Mode bit in the Control Register, to generate a byte-parity-error indication. Then, the four byte-parity-error signals are NORed together, to compute the assertive-LOW parity-flag value.

Word-Width Selection on Port B

The word width of data access on Port B is selected by the WS_0 and WS_1 control inputs. WS_0 and WS_1 both are tied HIGH for 36-bit access; they both are tied LOW for single-byte access. For double-byte access, WS_0 is tied HIGH and WS_1 is tied LOW.

In the single-byte-access or double-byte-access modes, FIFO write operations on Port B essentially pack the data to form 36-bit words, as viewed from Port A. Similarly, single-byte or double-byte FIFO read operations on Port B essentially unpack 36-bit words through a series of shift operations. FIFO status flags are updated following the last access which forms a complete 36-bit transfer.

Since the values for each status flag are computed by logic directly associated with one of the FIFO-memory arrays, and not by logic associated with Port B, *the flag values reflect the array fullness situation in terms of complete 36-bit words*, and not in terms of bytes or double bytes.

However, there is no such restriction for switching from writing to reading, or from reading to writing, at Port B. As long as t_{RWS}, t_{DS}, and t_A are satisfied, $R/\overline{W}_B$ may change state after *any* single-byte or double-byte access, and not only after a full 36-bit-word access.

Also, the word-width-writing feature continues to operate properly in 'loopback' mode.

Note that the programmable word-width-matching feature is *only* supported for FIFO accesses. Mailbox and Data Bypass operations do *not* support word-width matching between Port A and Port B. Tables 2, 3, and 4, and Figures 6a and 6b summarize word-width selection for Port B.

Table 2. Port B Word-Width Selection

WS_1	WS_0	PORT B DATA WIDTH
H	H	36-Bit
H	L	(Reserved)
L	H	18-Bit
L	L	9-Bit

Table 3. Flag Programming Words

RESOURCE-REGISTER ADDRESS			RESOURCE-REGISTER CONTENTS
A_2	A_1	A_0	
H	H	H	**NORMAL FIFO OPERATION** X...
H	H	L	**MAILBOX** X...
H	L	H	**36-BIT MODE** D_{34A} . . . D_{27A} / D_{25A} . . . D_{18A} / D_{16A} . . . D_{9A} / D_{7A} . . . D_{0A} X $\overline{AF_2}$ Offset [1] X $\overline{AE_2}$ Offset [1] X $\overline{AF_1}$ Offset [1] X $\overline{AE_1}$ Offset [1]
H	L	L	**CONTROL REGISTER (WRITE-ONLY)** D_{0A} X... X Parity Mode [2]
L	H	H	**8-BIT $\overline{AE_1}$ FLAG** D_{7A} . . . D_{0A} X... X $\overline{AE_1}$ Offset [1]
L	H	L	**8-BIT $\overline{AF_1}$ FLAG** D_{7A} . . . D_{0A} X... X $\overline{AF_1}$ Offset [1]
L	L	H	**8-BIT $\overline{AE_2}$ FLAG** D_{7A} . . . D_{0A} X... X $\overline{AE_2}$ Offset [1]
L	L	L	**8-BIT $\overline{AF_2}$ FLAG** D_{7A} . . . D_{0A} X... X $\overline{AF_2}$ Offset [1]

NOTES:

1. All four programmable-flag-offset values are initialized to eight (8) during a reset operation.
2. Odd parity = HIGH; even parity = LOW. The parity mode is initialized to odd during a reset operation.

Table 4. Flag Definition Table [1]

FLAG	VALID FULL-WORD READ CYCLES REMAINING				VALID FULL-WORD WRITE CYCLES REMAINING			
	FLAG = LOW		FLAG = HIGH		FLAG = LOW		FLAG = HIGH	
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
$\overline{FF}$	256	256	0	255	0	0	1	256
$\overline{AF}$	256-p	256	0	255-p	0	p	p + 1	256
$\overline{HF}$	129	256	0	128	0	127	128	256
$\overline{AE}$	0	q	q + 1	256	256-q	256	0	255-q
$\overline{EF}$	0	0	1	256	256	256	0	255

NOTE:

1. p is the number in the Almost-Full-Flag-Offset-Value register for that port. q is the number in the Almost-Empty-Flag-Offset-Value register for that port.

PORT B WORD-WIDTH SELECTION

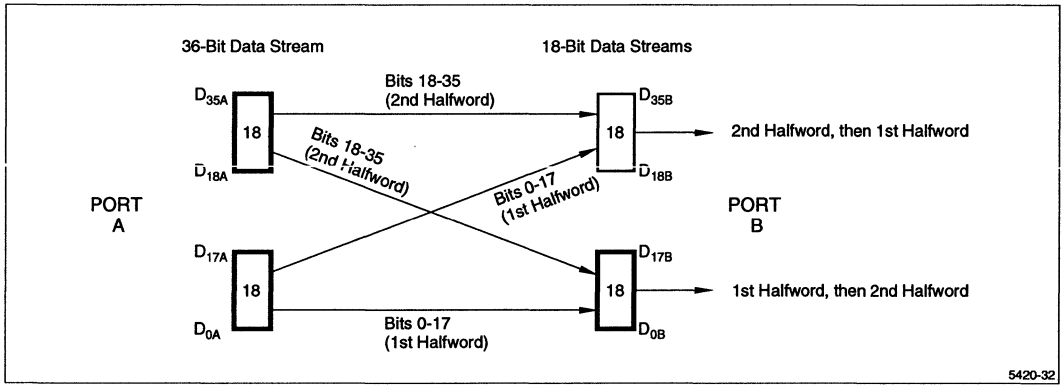


Figure 6a. 36-to-18 Funneling Through FIFO #1

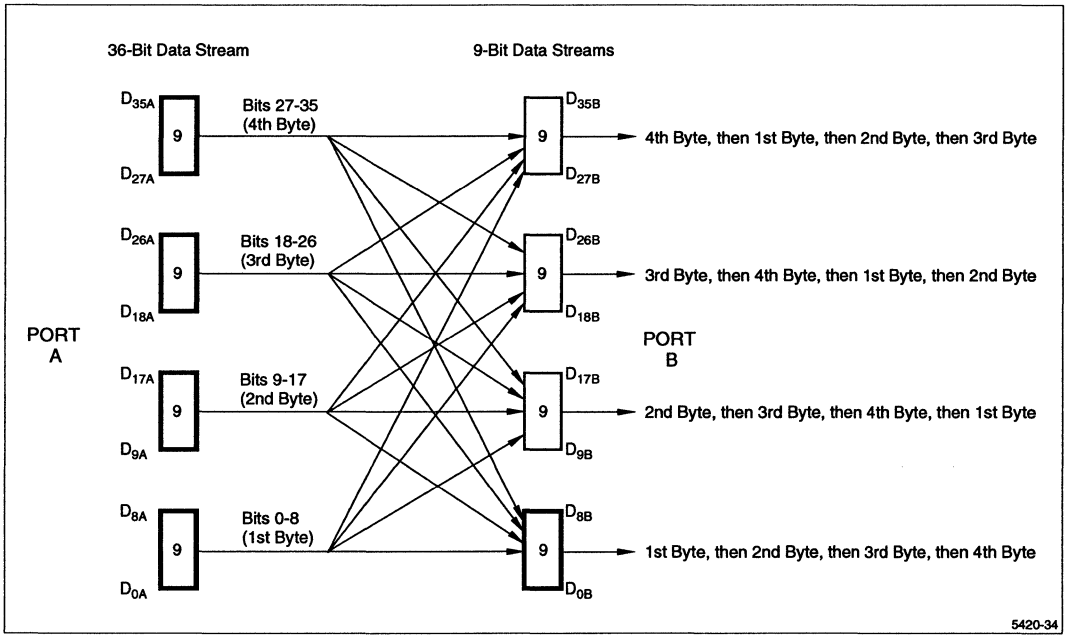


Figure 6b. 36-to-9 Funneling Through FIFO #1

NOTES:

1. The heavy black borders on register segments indicate the main data path, suitable for most applications. Alternate paths feature a different ordering of bytes within a word, at Port B.
2. The funneling process does not change the ordering of bits within a byte. Halfwords (Figure 6a) or bytes (Figure 6b) are transferred in parallel form from Port A to Port B.
3. The word-width setting may be changed during system operation; however, two clock intervals should be allowed for these signals to settle, before again attempting to read D_{0B} – D_{35B}. Also, incomplete data words may occur when the word width is changed from shorter to longer, at an inappropriate point in the data block passing through the FIFO. To avoid such incomplete data words, and to achieve proper synchronization, 'dummy' partial words should be supplied to complete the final longer word.

PORT B WORD-WIDTH SELECTION

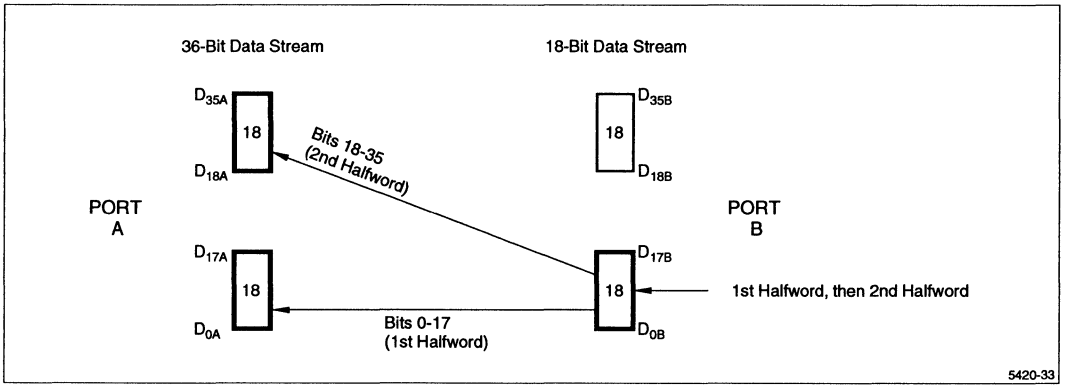


Figure 7a. 18-to-36 Defunneling Through FIFO #2

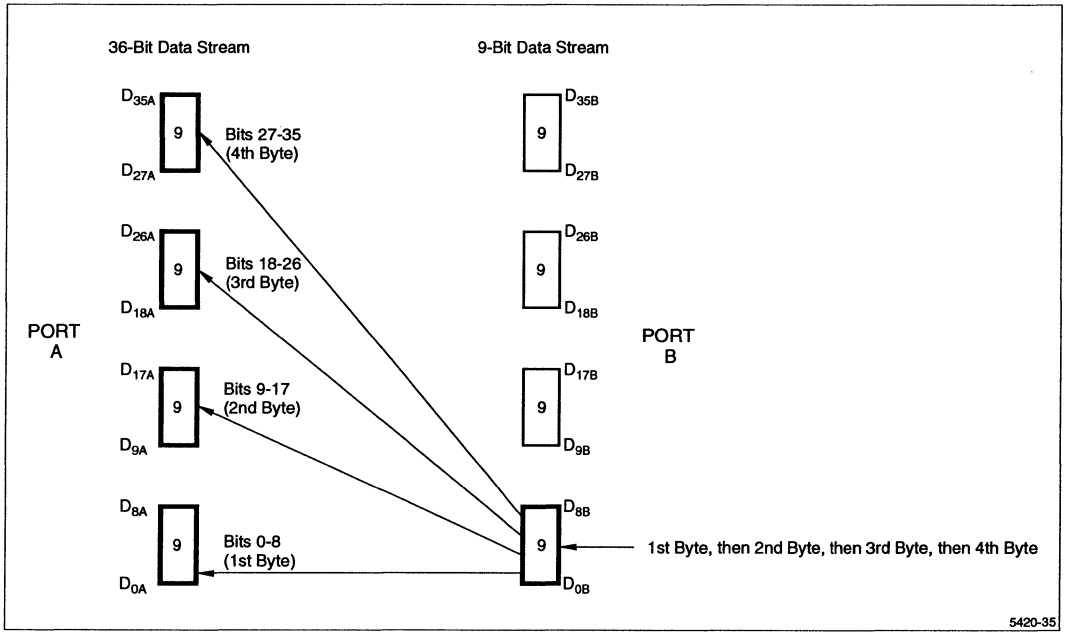
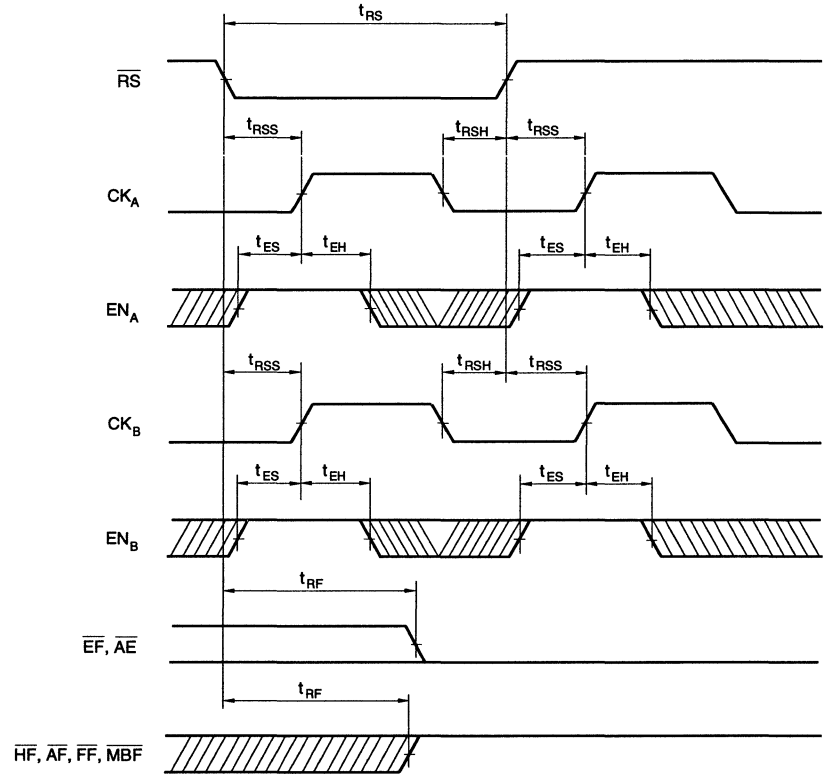


Figure 7b. 9-to-36 Defunneling Through FIFO #2

NOTES:

1. The heavy black borders on register segments indicate the only data paths used. The other byte segments of Port B do not participate in the data path during defunneling.
2. The defunneling process does not change the ordering of bits within a byte. Halfwords (Figure 7a) or bytes (Figure 7b) are transferred in parallel form from Port B to Port A.
3. The word-width setting may be changed during system operation; however, two clock intervals should be allowed for these signals to settle, before again attempting to send data. Also, incomplete data words may occur when the word width is changed from shorter to longer, at an inappropriate point in the data block passing through the FIFO. To avoid such incomplete data words, and to achieve proper synchronization, 'dummy' partial words should be supplied to complete the final longer word.

TIMING DIAGRAMS



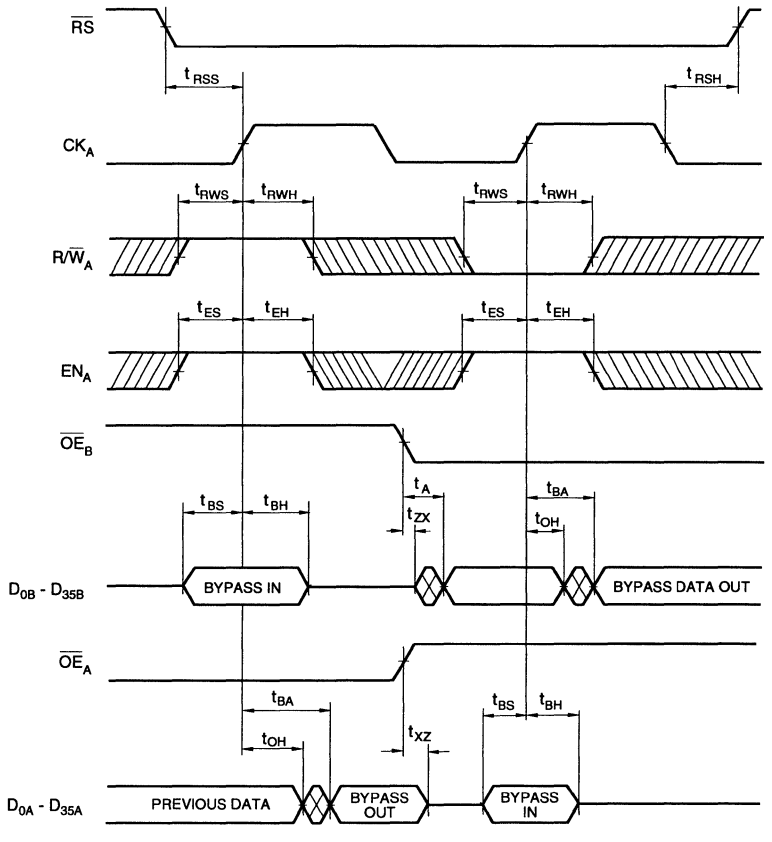
NOTES:

1. $\overline{RS}$ overrides all other input signals, except for $R/\overline{W}_A$, and operates asynchronously. $\overline{RS}$ operates whether or not EN_A and/or EN_B are asserted.
2. t_{RSS}, t_{RSH} need not be met unless the rising edge of CK_A and/or CK_B occurs while that clock is enabled.
3. The parity check is initialized to odd byte parity at reset.
4. The $\overline{AE}$ and $\overline{AF}$ flag offsets are initialized to eight locations from the boundary at reset.

5420-26

Figure 8. Reset Timing

TIMING DIAGRAMS (cont'd)



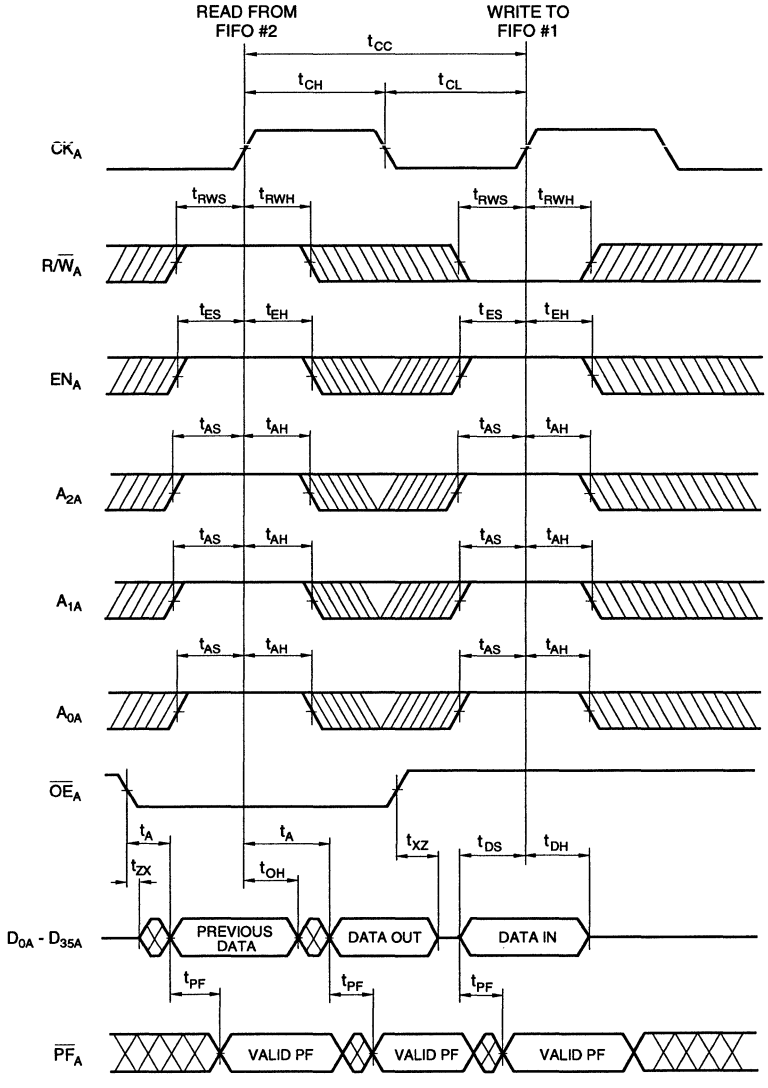
NOTES:

1. t_{RSS}, t_{RSH} need not be met unless the rising edge of CK_A or CK_B occurs while that clock is enabled.
2. Port A is considered the master port for bypass operation. Thus, CK_A, $R/\overline{W}_A$, and EN_A control the transmission of data between ports at reset.

5420-27

Figure 9. Data Bypass Timing

TIMING DIAGRAMS (cont'd)



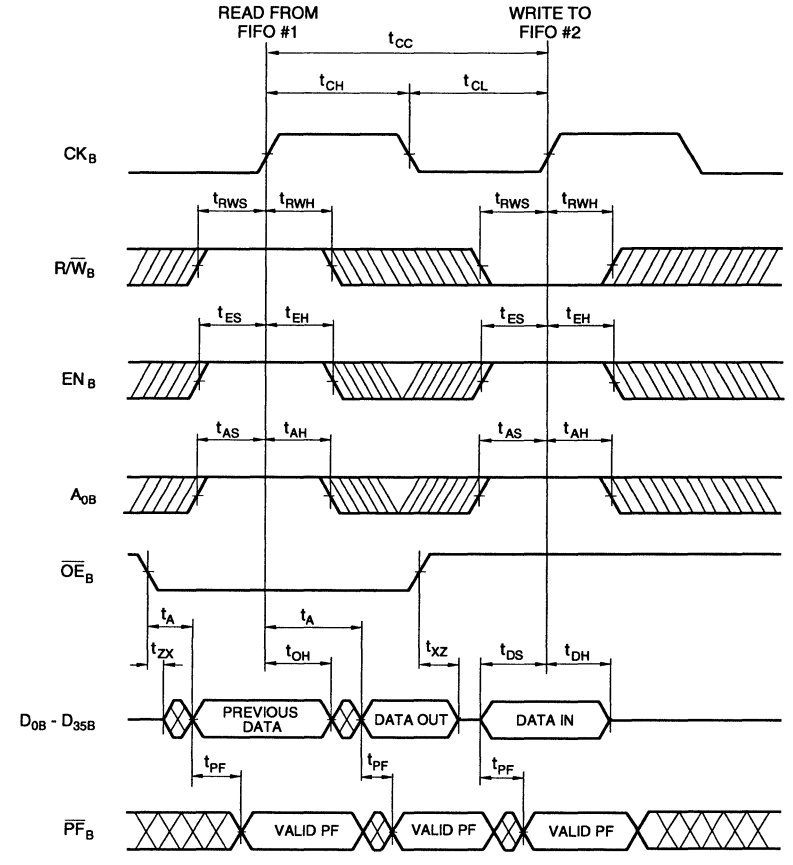
NOTES:

1. The Port A Parity Error Flag ($\overline{PF}_A$) reflects the parity status of data present on the data bus.
2. The status of $\overline{OE}_A$ does not gate read or write operations.
3. If $\overline{OE}_A$ is left LOW during a write operation, then the previous data held in the output latch is written back into FIFO #1.

5420-24

Figure 10. Port A FIFO Read/Write

TIMING DIAGRAMS (cont'd)



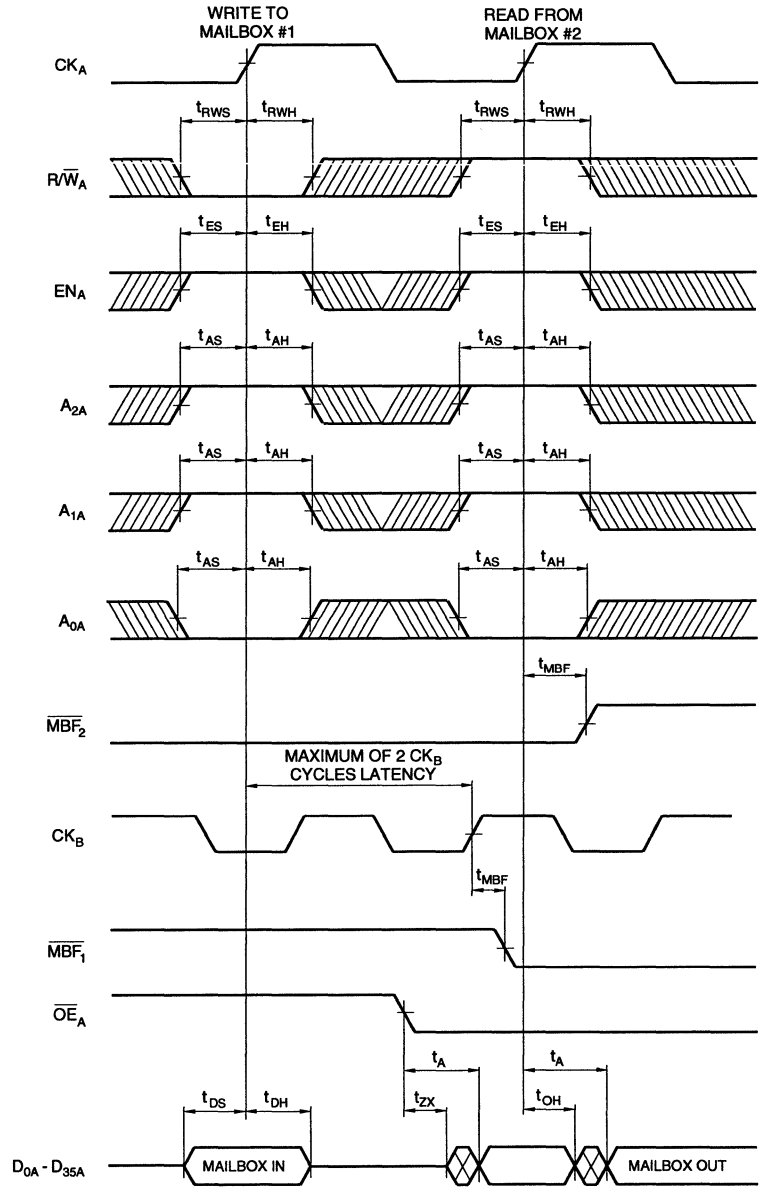
NOTES:

1. The Port B Parity Error Flag ($\overline{PF}_B$) reflects the parity status of data present on the data bus.
2. The status of $\overline{OE}_B$ does not gate read or write operations.
3. If $\overline{OE}_B$ is left LOW during a write operation, then the previous data held in the output latch is written back into FIFO #2.

5420-25

Figure 11. Port B FIFO Read/Write

TIMING DIAGRAMS (cont'd)



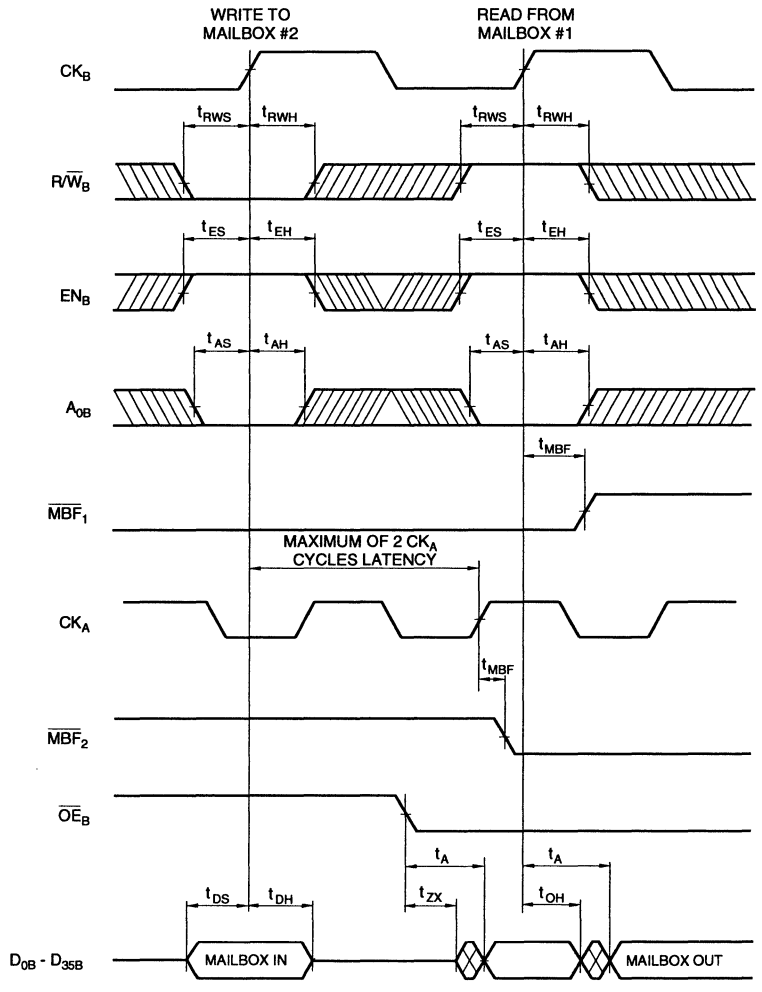
NOTES:

1. Both edges of $\overline{MBF_2}$ are synchronized to the Port A clock, CK_A.
2. Both edges of $\overline{MBF_1}$ are synchronized to the Port B clock, CK_B.
3. There is a maximum of two CK_B clock cycles of synchronization latency before $\overline{MBF_1}$ is asserted to indicate valid new mailbox data. If CK_B and CK_A are identical, there is a maximum of one clock cycle.
4. The status of mailbox flags does not prevent mailbox read or write operations.

5420-22

Figure 12. Port A Mailbox Access

TIMING DIAGRAMS (cont'd)



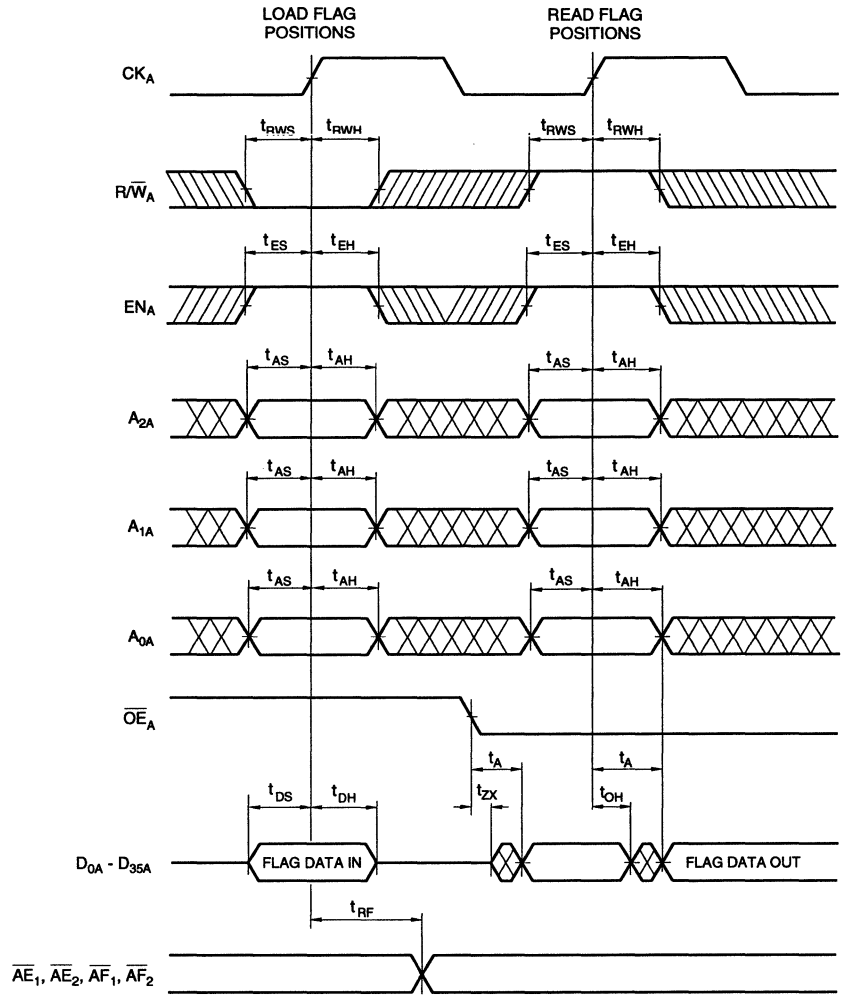
NOTES:

1. Both edges of $\overline{MBF}_2$ are synchronized to the Port A clock, CK_A.
2. Both edges of $\overline{MBF}_1$ are synchronized to the Port B clock, CK_B.
3. There is a maximum of two CK_A clock cycles of synchronization latency before $\overline{MBF}_2$ is asserted to indicate valid new mailbox data. If CK_A and CK_B are identical, there is a maximum of one clock cycle.
4. The status of mailbox flags does not prevent mailbox read or write operations.

5420-23

Figure 13. Port B Mailbox Access

TIMING DIAGRAMS (cont'd)



NOTES:

1. For valid flag address codes and data formats, see Table 3.
2. If flag status is altered by flag programming, the updated flags will be valid within a time t_{RF}.

5420-18

Figure 14. Flag Programming

TIMING DIAGRAMS (cont'd)

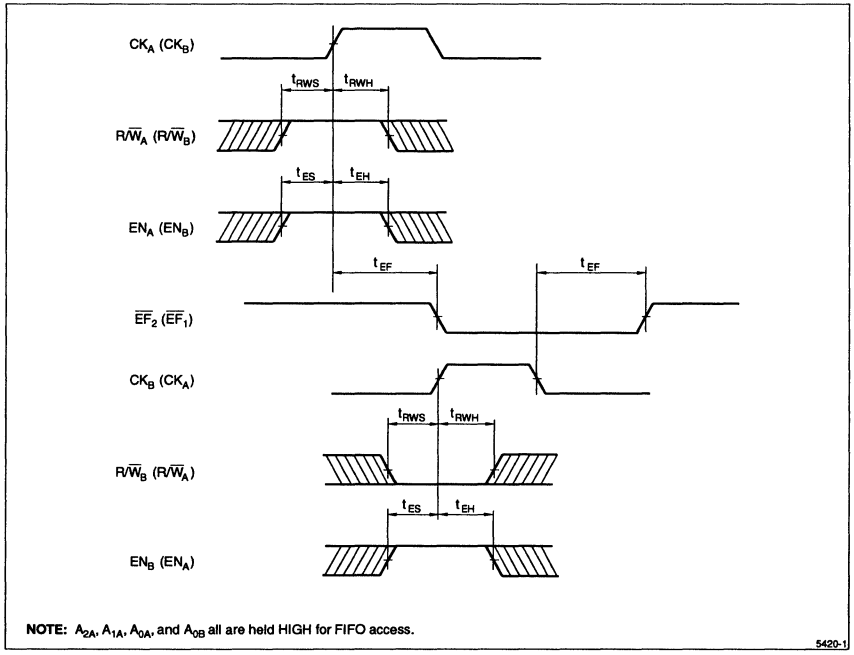


Figure 15. Empty Flag Timing

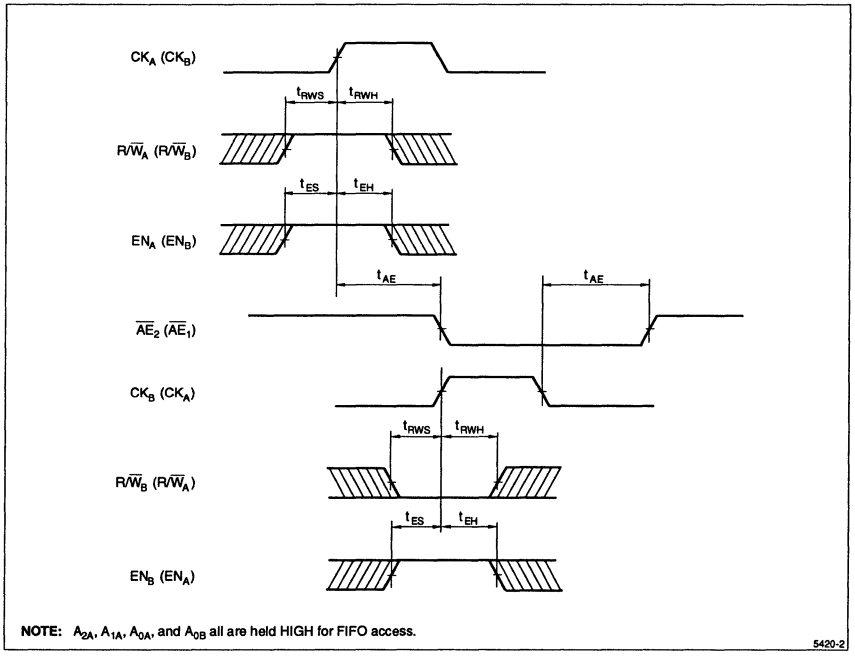


Figure 16. Almost-Empty Flag Timing

TIMING DIAGRAMS (cont'd)

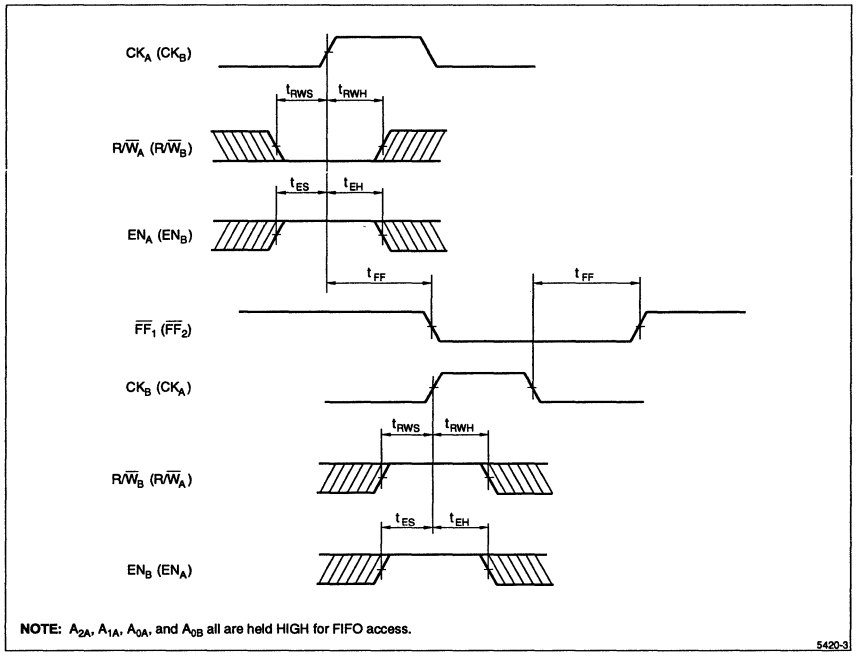


Figure 17. Full Flag Timing

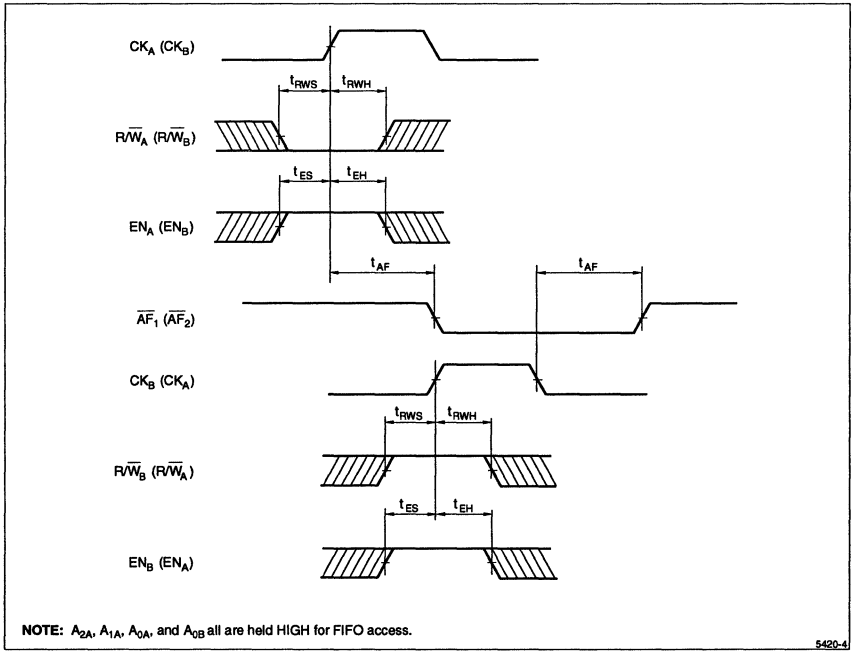
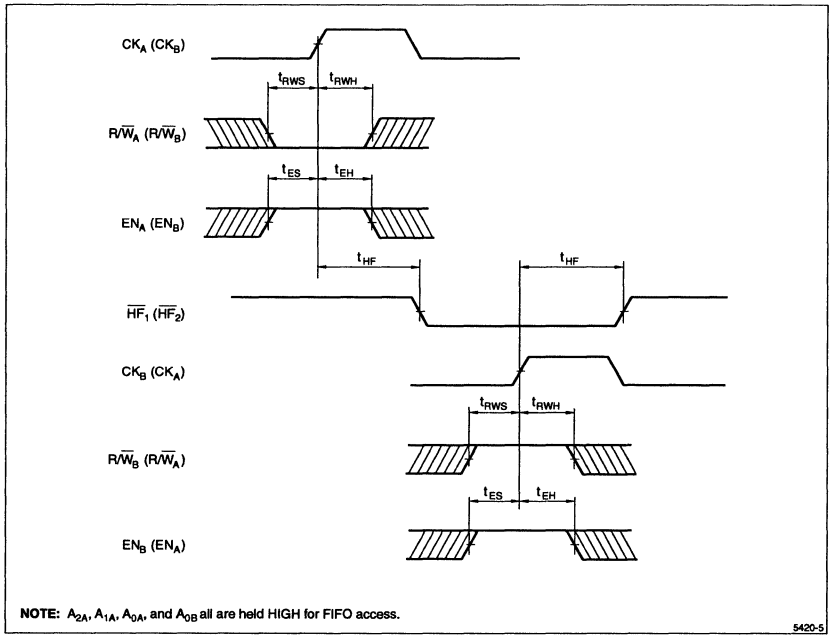


Figure 18. Almost-Full Flag Timing

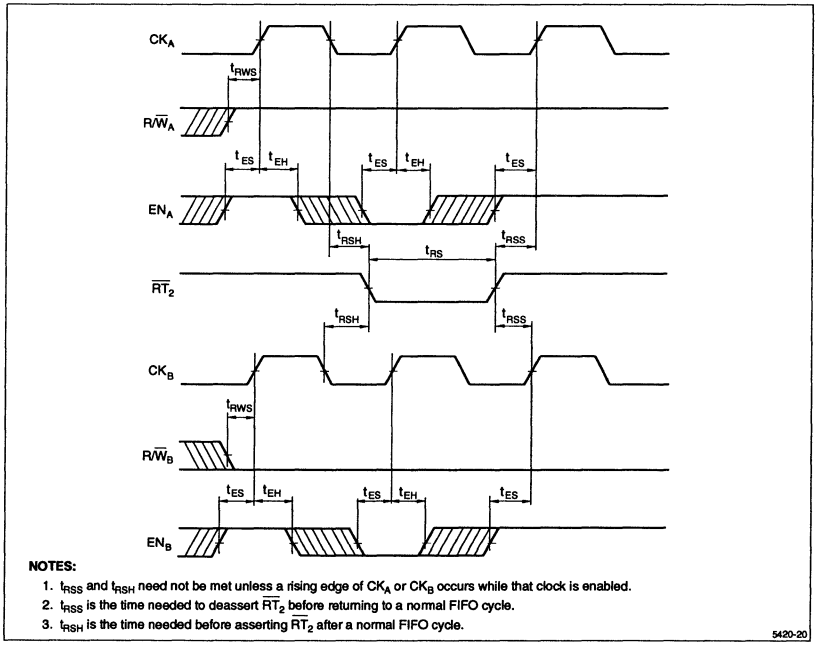
TIMING DIAGRAMS (cont'd)



NOTE: A_{2A}, A_{1A}, A_{0A}, and A_{0B} all are held HIGH for FIFO access.

5420-5

Figure 19. Half-Full Flag Timing



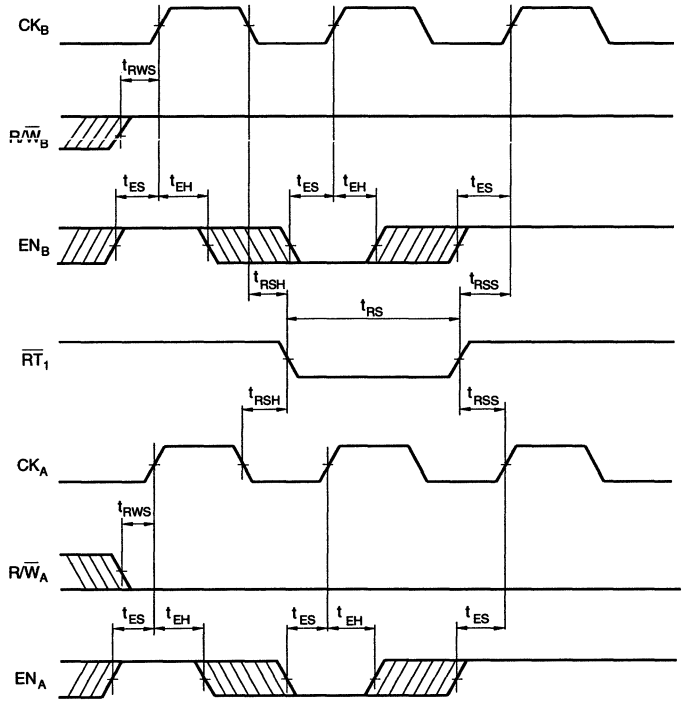
NOTES:

1. t_{RSS} and t_{RSH} need not be met unless a rising edge of CK_A or CK_B occurs while that clock is enabled.
2. t_{RSS} is the time needed to deassert $\overline{RT}_2$ before returning to a normal FIFO cycle.
3. t_{RSH} is the time needed before asserting $\overline{RT}_2$ after a normal FIFO cycle.

5420-20

Figure 20. FIFO #2 Retransmit

TIMING DIAGRAMS (cont'd)



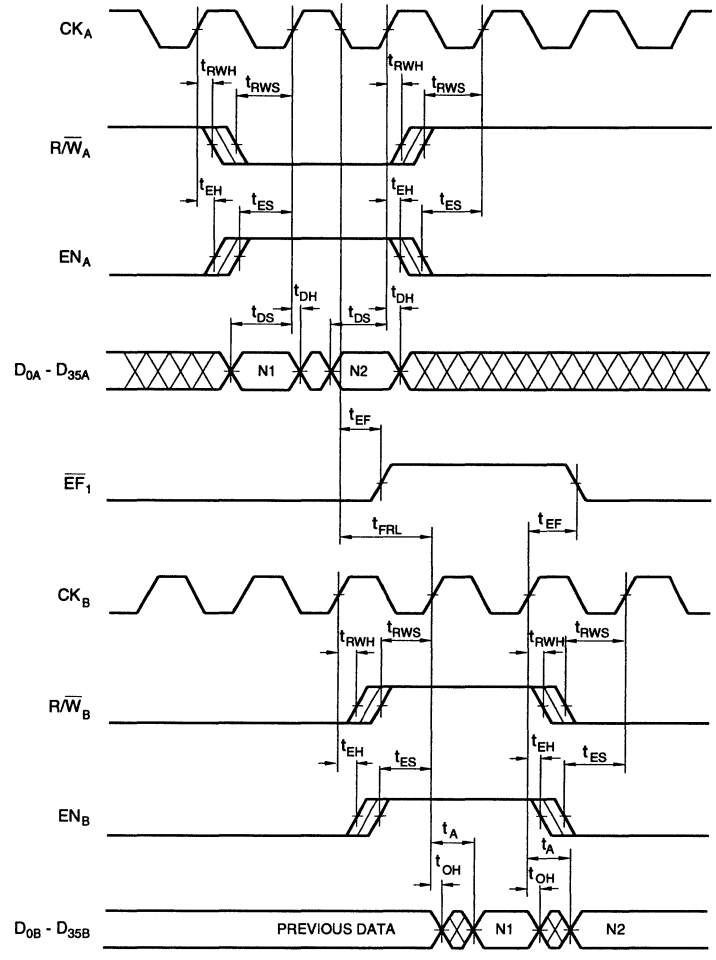
NOTES:

1. t_{RSS} and t_{RSH} need not be met unless a rising edge of CK_A or CK_B occurs while that clock is enabled.
2. t_{RSS} is the time needed to deassert $\overline{RT}_1$ before returning to a normal FIFO cycle.
3. t_{RSH} is the time needed before asserting $\overline{RT}_1$ after a normal FIFO cycle.

5420-21

Figure 21. FIFO #1 Retransmit

TIMING DIAGRAMS (cont'd)



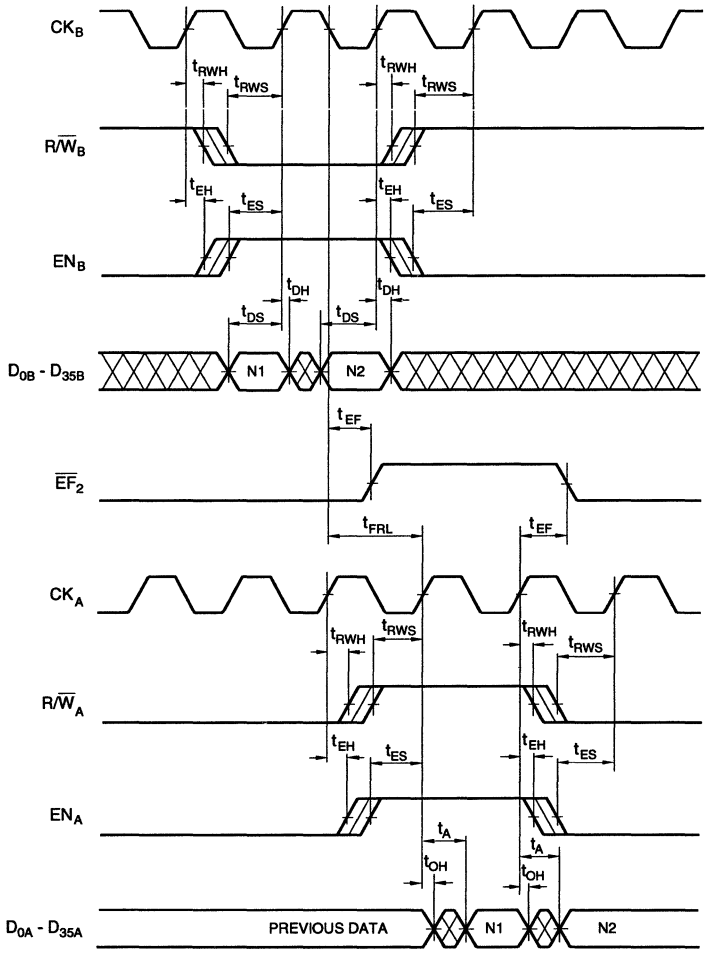
NOTES:

1. A_{2A}, A_{1A}, A_{0A}, and A_{0B} are all held HIGH for FIFO access.
2. $\overline{OE}_A$ is held HIGH.
3. $\overline{OE}_B$ is held LOW.
4. t_{FRL} (First Read Latency) - The first read following an empty condition may begin no earlier than t_{FRL} after the first write to an empty FIFO, to ensure that valid read data is retrieved.

5420-16

Figure 22. FIFO #1 Write and Read Operation in Near-Empty Region

TIMING DIAGRAMS (cont'd)



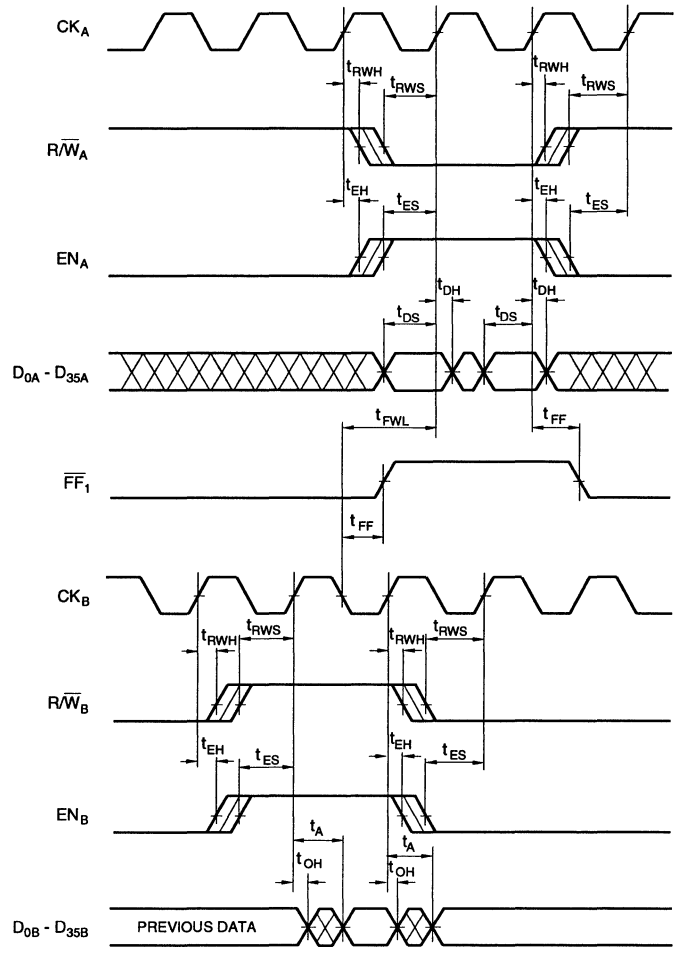
NOTES:

1. A_{2A}, A_{1A}, A_{0A}, and A_{0B} are all held HIGH for FIFO access.
2. $\overline{OE}_A$ is held HIGH.
3. $\overline{OE}_B$ is held LOW.
4. t_{FRL} (First Read Latency) - The first read following an empty condition may begin no earlier than t_{FRL} after the first write to an empty FIFO, to ensure that valid read data is retrieved.

5420-17

Figure 23. FIFO #2 Write and Read Operation in Near-Empty Region

TIMING DIAGRAMS (cont'd)



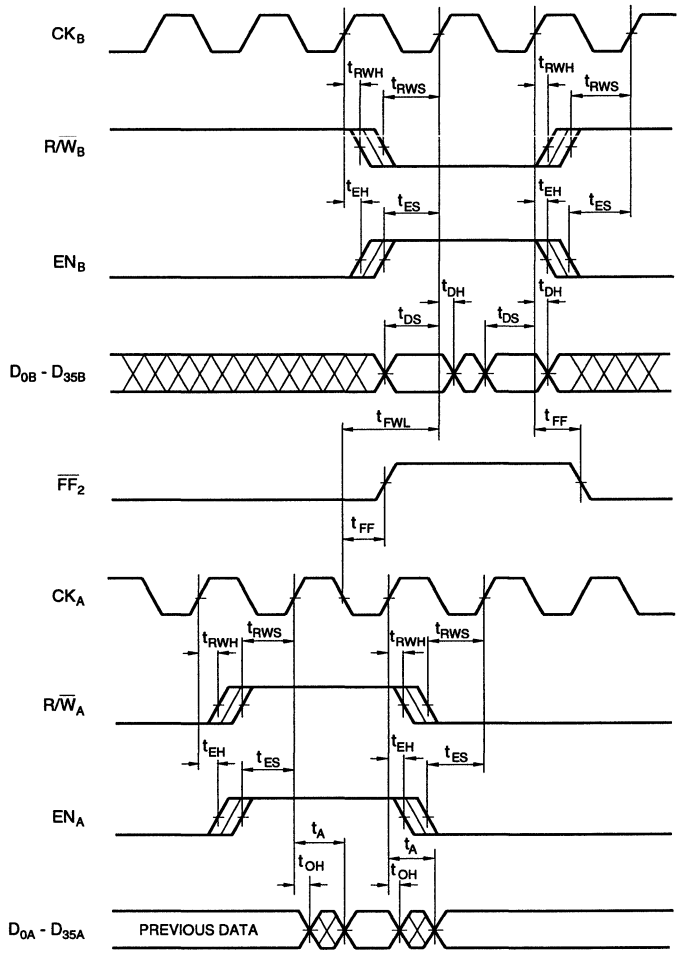
NOTES:

1. A_{2A}, A_{1A}, A_{0A}, and A_{0B} are all held HIGH for FIFO access.
2. $\overline{OE}_A$ is held HIGH.
3. $\overline{OE}_B$ is held LOW.
4. t_{FWL} (First Write Latency) - The first write following a full condition may begin no earlier than t_{FWL} after the first read from a full FIFO, to ensure that valid write data is written.

5420-14

Figure 24. FIFO #1 Read and Write Operation in Near-Full Region

TIMING DIAGRAMS (cont'd)



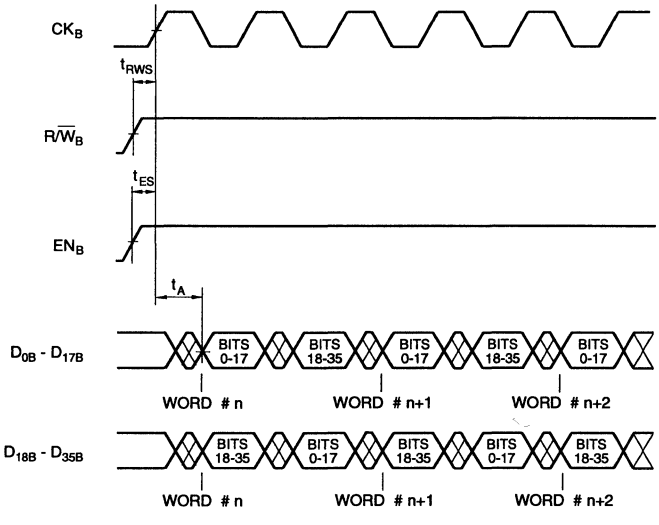
NOTES:

1. A_{2A}, A_{1A}, A_{0A}, and A_{0B} are all held HIGH for FIFO access.
2. $\overline{OE}_A$ is held LOW.
3. $\overline{OE}_B$ is held HIGH.
4. t_{FWL} (First Write Latency) - The first write following a full condition may begin no earlier than t_{FWL} after the first read from a full FIFO, to ensure that valid write data is written.

5420-15

Figure 25. FIFO #2 Read and Write Operation in Near-Full Region

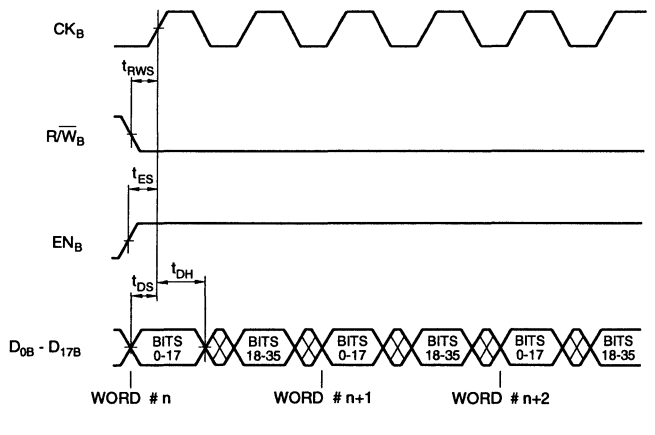
TIMING DIAGRAMS (cont'd)



NOTES:
1. $\overline{A_{0B}}$ is held HIGH for FIFO access.
2. $\overline{OE_B}$ is held LOW.
3. WS_0 is held HIGH and WS_1 is held LOW for double-byte access.

5420-13

Figure 26. Port B Double-Byte FIFO #1 Read Access for 36-to-18 Funneling

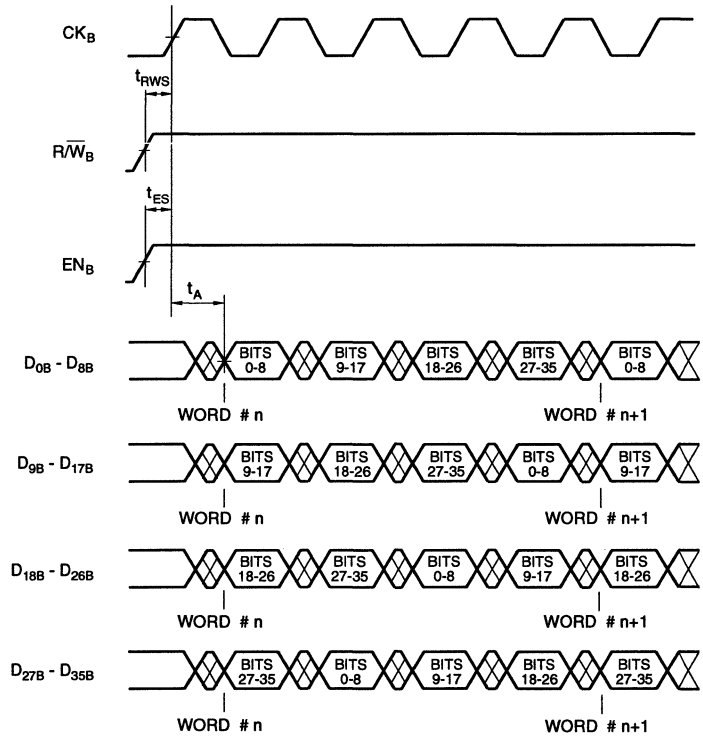


NOTES:
1. $\overline{A_{0B}}$ is held HIGH for FIFO access.
2. $\overline{OE_B}$ is held HIGH.
3. WS_0 is held HIGH and WS_1 is held LOW for double-byte access.

5420-12

Figure 27. Port B Double-Byte FIFO #2 Write Access for 18-to-36 Defunneling

TIMING DIAGRAMS (cont'd)



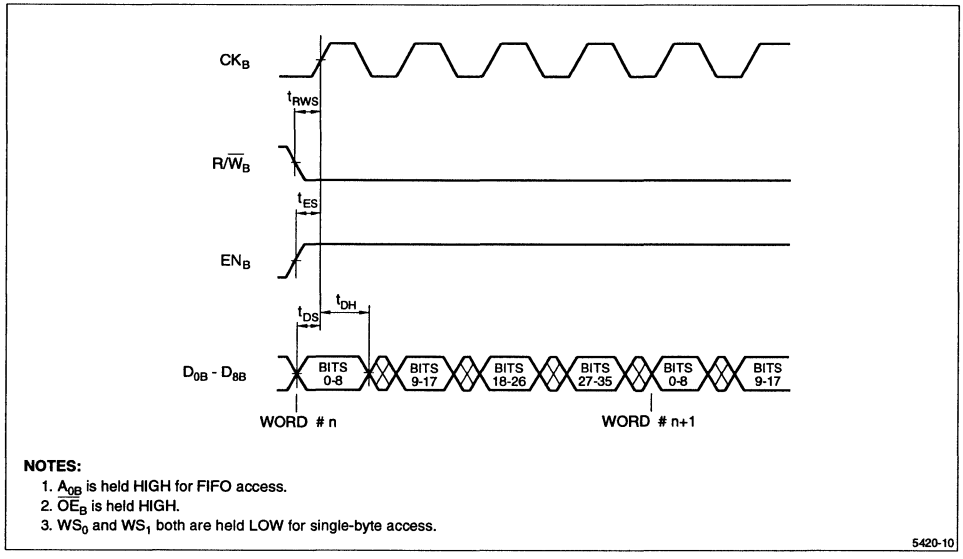
NOTES:

1. A_{0B} is held HIGH for FIFO access.
2. $\overline{OE}_B$ is held LOW.
3. WS_0 and WS_1 both are held LOW for single-byte access.

5420-11

Figure 28. Port B Single-Byte FIFO #1 Read Access for 36-to-9 Funneling

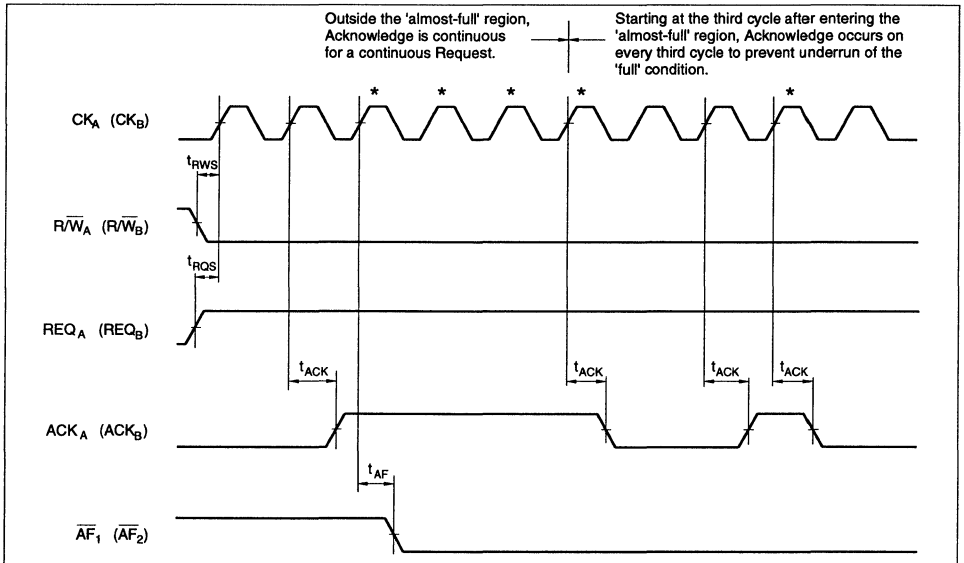
TIMING DIAGRAMS (cont'd)



NOTES:
1. A_{0B} is held HIGH for FIFO access.
2. $\overline{OE}_B$ is held HIGH.
3. WS_0 and WS_1 both are held LOW for single-byte access.

5420-10

Figure 29. Port B Single-Byte FIFO #2 Write Access for 9-to-36 Defunneling

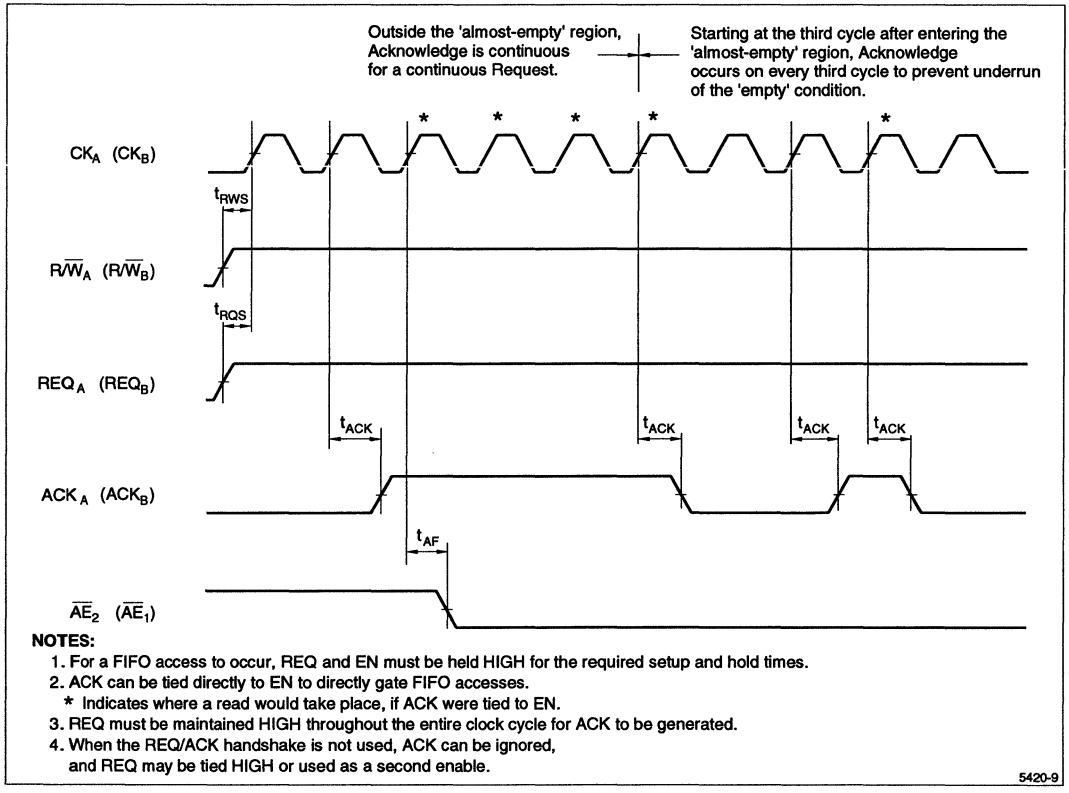


NOTES:
1. For a FIFO access to occur, REQ and EN must be held HIGH for the required setup and hold times.
2. ACK can be tied directly to EN to directly gate FIFO accesses.
   * Indicates where a write would take place, if ACK were tied to EN.
3. REQ must be maintained HIGH throughout the entire clock cycle for ACK to be generated.
4. When the REQ/ACK handshake is not used, ACK can be ignored, and REQ may be tied HIGH or used as a second enable.

5420-8

Figure 30. Write Request/Acknowledge Handshake

TIMING DIAGRAMS (cont'd)



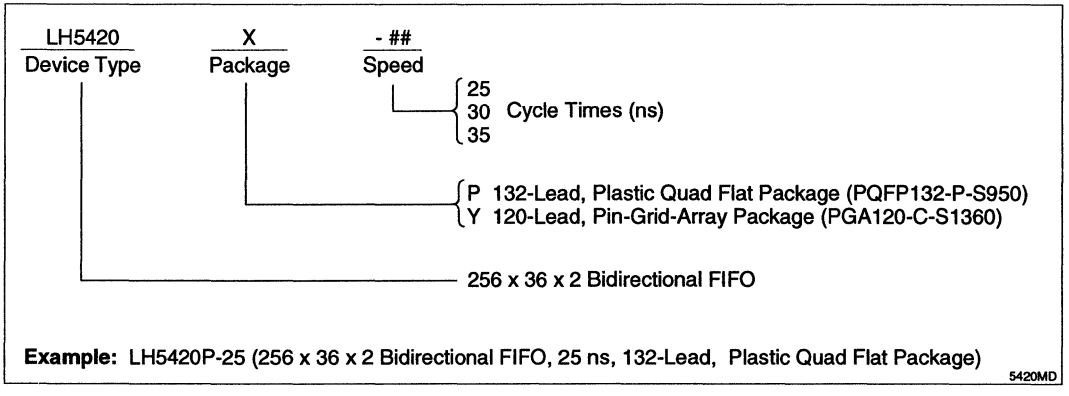
NOTES:

1. For a FIFO access to occur, REQ and EN must be held HIGH for the required setup and hold times.
2. ACK can be tied directly to EN to directly gate FIFO accesses.
   * Indicates where a read would take place, if ACK were tied to EN.
3. REQ must be maintained HIGH throughout the entire clock cycle for ACK to be generated.
4. When the REQ/ACK handshake is not used, ACK can be ignored, and REQ may be tied HIGH or used as a second enable.

5420-9

Figure 31. Read Request/Acknowledge Handshake

ORDERING INFORMATION



Example: LH5420P-25 (256 x 36 x 2 Bidirectional FIFO, 25 ns, 132-Lead, Plastic Quad Flat Package)

5420MD

LH540202

PRELIMINARY

CMOS 1024 × 9 Asynchronous FIFO

FEATURES

- Fast Access Times: 15/20/25/35/50 ns
- Fast-Fall-Through Time Architecture Based on CMOS Dual-Port SRAM Technology
- Input Port and Output Port Have Entirely Independent Timing
- Expandable in Width and Depth
- Full, Half-Full, and Empty Status Flags
- Data Retransmission Capability
- TTL-Compatible I/O
- Pin and Functionally Compatible with Sharp LH5496/97 and with Am/IDT/MS7201/02
- Control Signals Assertive-LOW for Noise Immunity
- Packages:
  - 28-Pin, 300-mil PDIP
  - 28-Pin, 600-mil PDIP *
  - 28-Pin, 300-mil SOJ *
  - 32-Pin PLCC

FUNCTIONAL DESCRIPTION

The LH540202 is a FIFO (First-In, First-Out) memory device, based on fully-static CMOS dual-port SRAM technology, capable of storing up to 1024 nine-bit words. It follows the industry-standard architecture and package pinouts for nine-bit asynchronous FIFOs. Each nine-bit LH540202 word may consist of a standard eight-bit byte, together with a parity bit or a block-marking/framing bit.

The input and output ports operate entirely independently of each other, unless the LH540202 becomes either totally full or else totally empty. Data flow at a port is initiated by asserting either of two asynchronous, assertive-LOW control inputs: Write ($\overline{W}$) for data entry at the input port, or Read ($\overline{R}$) for data retrieval at the output port.

Full, Half-Full, and Empty status flags monitor the extent to which the internal memory has been filled. The system may make use of these status outputs to avoid the risk of data loss, which otherwise might occur either by attempting to write additional words into an already-full LH540202, or by attempting to read additional words from an already-empty LH540202. When an LH540202 is operating in a depth-cascaded configuration, the Half-Full Flag is not available.

PIN CONNECTIONS

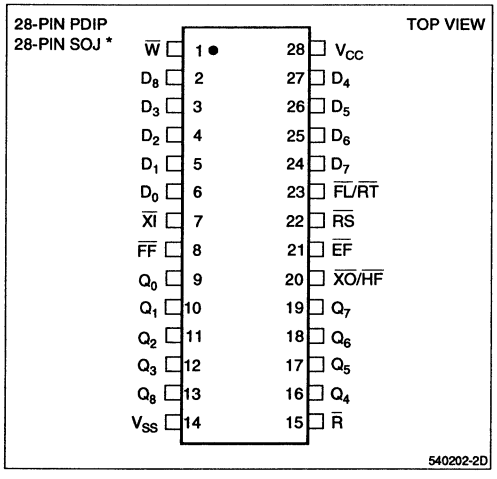


Figure 1. Pin Connections for PDIP * and SOJ * Packages

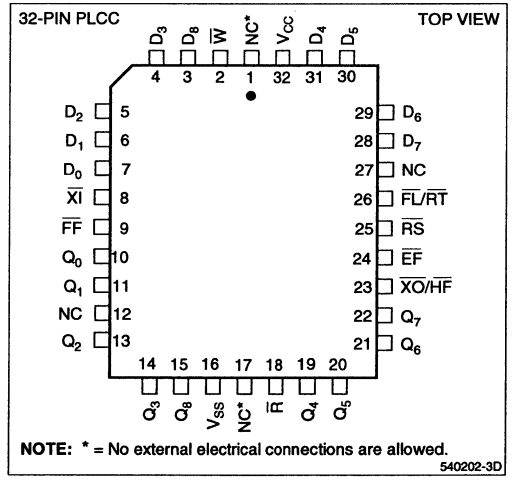


Figure 2. Pin Connections for PLCC Package

* This is a Preliminary data sheet; except that all references to the 600-mil PDIP and SOJ packages still have Advance Information status.

FUNCTIONAL DESCRIPTION (cont'd)

Data words are read out from the LH540202's output port in precisely the same order that they were written in at its input port; that is, according to a First-In, First Out (FIFO) queue discipline. Since the addressing sequence for a FIFO device's memory is internally predefined, no external addressing information is required for the operation of the LH540202 device.

Drop-in-replacement compatibility is maintained with both larger sizes and smaller sizes of industry-standard nine-bit asynchronous FIFOs. The only change is in the number of internally-stored data words implied by the states of the Full Flag and the Half-Full Flag.

The Retransmit ($\overline{RT}$) control signal causes the internal FIFO-memory-array read-address pointer to be set back to zero, to point to the LH540202's first physical memory location, without affecting the internal FIFO-memory-array write-address pointer. Thus, the Retransmit control signal provides a mechanism whereby a block of data, delimited by the zero physical address and the current write-address-pointer value, may be read out *repeatedly* an arbitrary number of times. The only restrictions are that neither the read-address pointer nor the write-address pointer may 'wrap around' during this entire process, i.e., advance past physical location zero after traversing the entire memory. The retransmit facility is not available when an LH540202 is operating in a depth-expanded configuration.

The Reset ($\overline{RS}$) control signal returns the LH540202 to an initial state, empty and ready to be filled. An LH540202 should be reset during every system power-up sequence. A reset operation causes the internal FIFO-memory-array write-address pointer, as well as the read-address pointer, to be set back to zero, to point to the LH540202's first physical memory location. Any information which previously had been stored within the LH540202 is not recoverable after a reset operation.

A cascading (depth-expansion) scheme may be implemented by using the Expansion In ($\overline{XI}$) input signal and the Expansion Out ($\overline{XO}/\overline{HF}$) output signal. This allows a deeper 'effective FIFO' to be implemented by using two or more LH540202 devices, without incurring additional latency ('fallthrough' or 'bubblethrough') delays, and without the necessity of storing and retrieving any given data word more than once. In this cascaded operating mode, one LH540202 device must be designated as the 'first-load' or 'master' device, by grounding its First-Load ($\overline{FL}/\overline{RT}$) control input; the remaining LH540202 devices are designated as 'slaves,' by tying their $\overline{FL}/\overline{RT}$ inputs HIGH. Because of the need to share control signals on pins, the Half-Full Flag and the retransmission capability are not available for either 'master' or 'slave' LH540202 devices operating in cascaded mode.

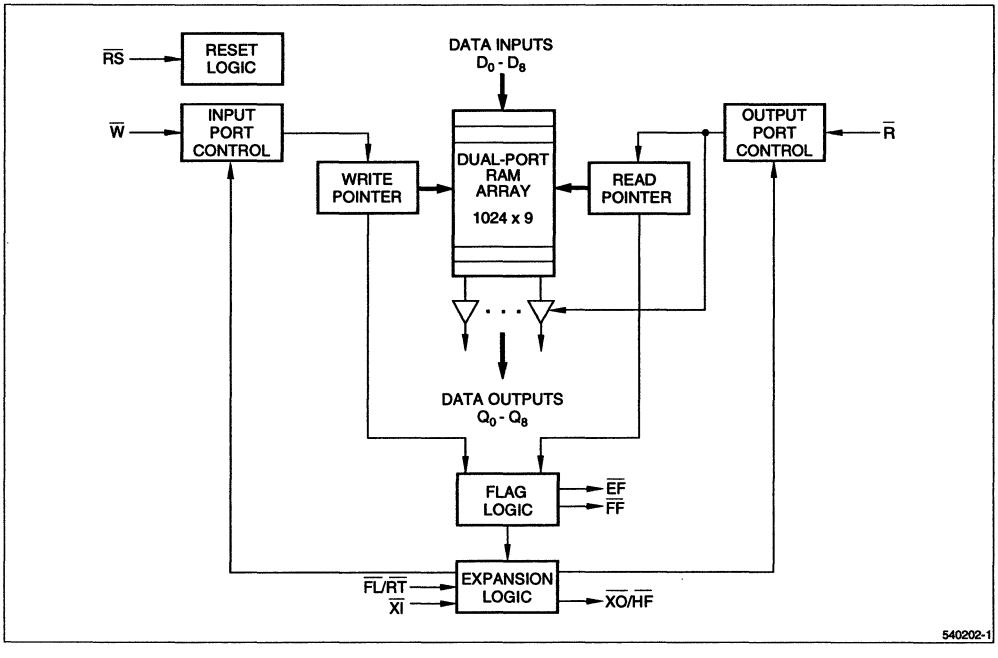


Figure 3. LH540202 Block Diagram

PIN DESCRIPTIONS

PIN	PIN TYPE *	DESCRIPTION
$D_0 - D_8$	I	Input Data Bus
$Q_0 - Q_8$	O/Z	Output Data Bus
$\overline{W}$	I	Write Request
$\overline{R}$	I	Read Request
$\overline{EF}$	O	Empty Flag
$\overline{FF}$	O	Full Flag
$\overline{XO}/\overline{HF}$	O	Expansion Out/Half-Full Flag
$\overline{XI}$	I	Expansion In
$\overline{FL}/\overline{RT}$	I	First Load/Retransmit
$\overline{RS}$	I	Reset
V_{CC}	V	Positive Power Supply
V_{SS}	V	Ground

* I = Input, O = Output, Z = High-Impedance, V = Power Voltage Level

OPERATIONAL DESCRIPTION

Reset

The LH540202 is reset whenever the Reset input ($\overline{RS}$) is taken LOW. A reset operation initializes both the read-address pointer and the write-address pointer to point to location zero, the first physical memory location. During a reset operation, the state of the $\overline{XI}$ and $\overline{FL}/\overline{RT}$ inputs determines whether the device is in standalone mode or in depth-cascaded mode. (See Tables 1 and 2.)

A reset operation is required whenever the LH540202 first is powered up. The Read ($\overline{R}$) and Write ($\overline{W}$) inputs may be in any state when the reset operation is initiated; but they must be HIGH, before the reset operation is terminated by a rising edge of $\overline{RS}$, by a time t_{RRSS} (for Read) or t_{WRSS} (for Write) respectively. (See Figure 10.)

Write

A write cycle is initiated by a falling edge of the Write ($\overline{W}$) control input. Data setup times and hold times must be observed for the data inputs ($D_0 - D_8$). Write operations may occur independently of any ongoing read operations. However, a write operation is possible only if the FIFO is not full, (i.e., if the Full Flag $\overline{FF}$ is HIGH).

At the falling edge of $\overline{W}$ for the first write operation after the memory is half filled, the Half-Full Flag is asserted ($\overline{HF}$ = LOW). It remains asserted until the difference between the write pointer and the read pointer indicates that the data words remaining in the LH540202 are filling the FIFO memory to less than or equal to one-half of its total capacity. The Half-Full Flag is deasserted ($\overline{HF}$ = HIGH) by the appropriate rising edge of $\overline{R}$. (See Table 3.)

The Full Flag is asserted ($\overline{FF}$ = LOW) at the falling edge of $\overline{W}$ for the write operation which fills the last available location in the FIFO memory array. $\overline{FF}$ = LOW inhibits further write operations until $\overline{FF}$ is cleared by a valid read operation. The Full Flag is deasserted ($\overline{FF}$ = HIGH) after the next rising edge of $\overline{R}$ releases another memory location. (See Table 3.)

Read

A read cycle is initiated by a falling edge of the Read ($\overline{R}$) control input. Read data becomes valid at the data outputs ($Q_0 - Q_8$) after a time t_A from the falling edge of $\overline{R}$. After $\overline{R}$ goes HIGH, the data outputs return to a high-impedance state. Read operations may occur independently of any ongoing write operations. However, a read operation is possible only if the FIFO is not empty (i.e., if the Empty Flag $\overline{EF}$ is HIGH).

The LH540202's internal read-address and write-address pointers operate in such a way that consecutive read operations always access data words in the same order that they were written. The Empty Flag is asserted ($\overline{EF}$ = LOW) after that falling edge of $\overline{R}$ which accesses the last available data word in the FIFO memory. $\overline{EF}$ is deasserted ($\overline{EF}$ = HIGH) after the next rising edge of $\overline{W}$ loads another valid data word. (See Table 3.)

Data Flow-Through

Read-data flow-through mode occurs when the Read ($\overline{R}$) control input is brought LOW while the FIFO is empty, and is held LOW in anticipation of a write cycle. At the end of the next write cycle, the Empty Flag $\overline{EF}$ momentarily is deasserted, and the data word just written becomes available at the data outputs ($Q_0 - Q_8$) after a maximum time of $t_{WEF} + t_A$. Additional write operations may occur while the $\overline{R}$ input remains LOW; but only data from the first write operation flows through to the data outputs. Additional data words, if any, may be accessed only by toggling $\overline{R}$.

Write-data flow-through mode occurs when the Write ($\overline{W}$) input is brought LOW while the FIFO is full, and is held LOW in anticipation of a read cycle. At the end of the read cycle, the Full Flag momentarily is deasserted, but then immediately is reasserted in response to $\overline{W}$ being held LOW. A data word is written into the FIFO on the rising edge of $\overline{W}$, which may occur no sooner than $t_{RFF} + t_{WPW}$ after the read operation.

OPERATIONAL DESCRIPTION (cont'd)

Retransmit

The FIFO can be made to reread previously-read data by means of the Retransmit function. A retransmit operation is initiated by pulsing the $\overline{RT}$ input LOW. Both $\overline{R}$ and $\overline{W}$ must be deasserted (HIGH) for the duration of the retransmit pulse. The FIFO's internal read-address pointer is reset to point to location zero, the first physical memory location, while the internal write-address pointer remains unchanged.

After a retransmit operation, those data words in the region in between the read-address pointer and the write-address pointer may be reaccessed by subsequent read operations. A retransmit operation may affect the state of the status flags $\overline{FF}$, $\overline{HF}$, and $\overline{EF}$, depending on the relocation of the read-address pointer. There is no restriction on the number of times that a block of data within an LH540202 may be read out, by repeating the retransmit operation and the subsequent read operations.

The maximum length of a data block which may be retransmitted is 1024 words. Note that if the write-address pointer ever 'wraps around' (i.e., passes location zero more than once) during a sequence of retransmit operations, some data words will be lost.

The Retransmit function is not available when the LH540202 is operating in depth-cascaded mode, because the $\overline{FL}/\overline{RT}$ control pin must be used for first-load selection rather than for retransmission control.

Table 1. Grouping-Mode Determination During a Reset Operation

$\overline{XI}$	$\overline{FL}/\overline{RT}$	MODE	$\overline{XO}/\overline{HF}$ USAGE	$\overline{XI}$ USAGE	$\overline{FL}/\overline{RT}$ USAGE
H [1]	H	Cascaded Slave [2]	$\overline{XO}$	$\overline{XI}$	$\overline{FL}$
H [1]	L	Cascaded Master [2]	$\overline{XO}$	$\overline{XI}$	$\overline{FL}$
L	X	Standalone	$\overline{HF}$	(none)	$\overline{RT}$

NOTES:
1. A reset operation forces $\overline{XO}$ HIGH for the nth FIFO, thus forcing $\overline{XI}$ HIGH for the n+1st FIFO.
2. The terms 'master' and 'slave' refer to operation in depth-cascaded grouping mode.
3. H = HIGH; L = LOW; X = Don't Care.

Table 2. Expansion-Pin Usage According to Grouping Mode

I/O	PIN	STANDALONE	CASCADED MASTER	CASCADED SLAVE
I	$\overline{XI}$	Grounded	From $\overline{XO}$ (n-1st FIFO)	From $\overline{XO}$ (n-1st FIFO)
O	$\overline{XO}/\overline{HF}$	Becomes $\overline{HF}$	To $\overline{XI}$ (n+1st FIFO)	To $\overline{XI}$ (n+1st FIFO)
I	$\overline{FL}/\overline{RT}$	Becomes $\overline{RT}$	Grounded (Logic LOW)	Logic HIGH

Table 3. Status Flags

NUMBER OF UNREAD DATA WORDS PRESENT WITHIN 1024 × 9 FIFO	$\overline{FF}$	$\overline{HF}$	$\overline{EF}$
0	H	H	L
1 to 512	H	H	H
513 to 1023	H	L	H
1024	L	L	H

OPERATIONAL MODES

Standalone Configuration

When depth cascading is not required for a given application, the LH540202 is placed in standalone mode by tying the Expansion In input ($\overline{XI}$) to ground. This input is internally sampled during a reset operation. (See Table 1.)

Width Expansion

Word-width expansion is implemented by placing multiple LH540202 devices in parallel. Each LH540202 should be configured for standalone mode. In this arrangement, the behavior of the status flags is identical for all devices; so, in principle, a representative value for each of these flags could be derived from any one device. In practice, it is better to derive 'composite' flag values using external logic, since there may be minor speed variations between different actual devices. (See Figures 4, 5, and 6.)

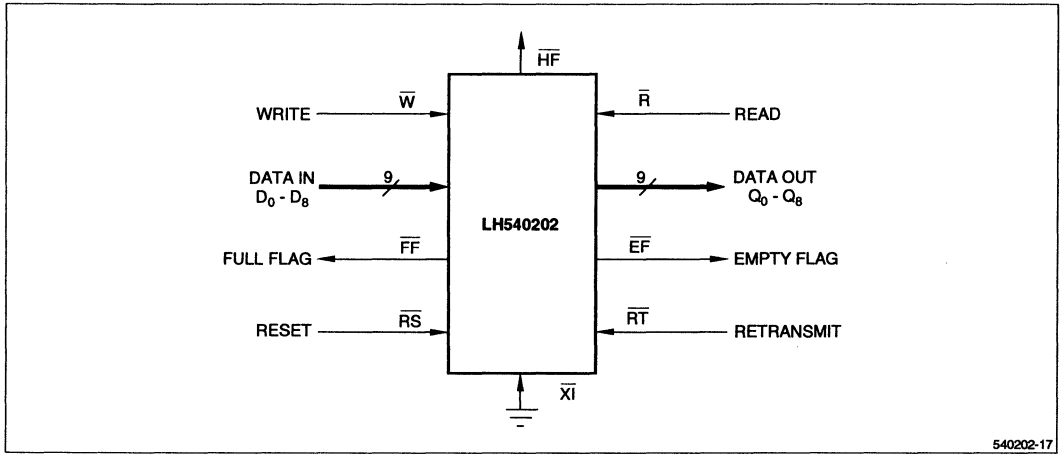


Figure 4. Standalone FIFO (1024 × 9)

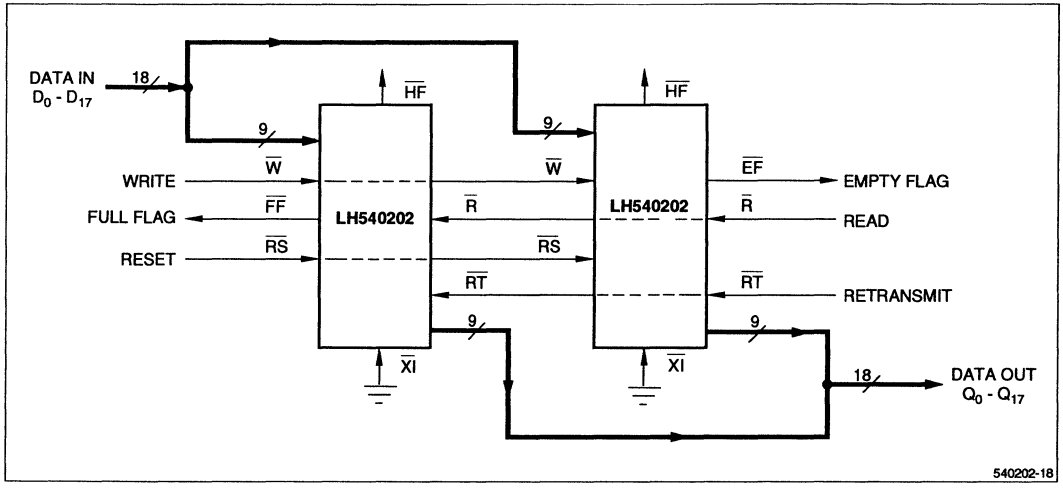


Figure 5. FIFO Word-Width Expansion (1024 × 18)

OPERATIONAL MODES (cont'd)

Depth Cascading

Depth cascading is implemented by configuring the required number of LH540202s in depth-cascaded mode. In this arrangement, the FIFOs are connected in a circular fashion, with the Expansion Out output ($\overline{XO}$) of each device tied to the Expansion In input ($\overline{XI}$) of the next device. One FIFO in the cascade must be designated as the 'first-load' device, by tying its First Load input ($\overline{FL}/\overline{RT}$) to ground. All other devices must have their $\overline{FL}/\overline{RT}$ inputs tied HIGH. In this mode, $\overline{W}$ and $\overline{R}$ signals are shared by all devices, while logic within each LH540202 controls the steering of data. Only one LH540202 is enabled during any given write cycle; thus, the common Data In inputs of all devices are tied together. Likewise, only one LH540202 is enabled during any given read cycle; thus, the common Data Out outputs of all devices are wire-ORed together

In depth-cascaded mode, external logic should be used to generate a composite Full Flag and a composite Empty Flag, by ANDing the $\overline{FF}$ outputs of all LH540202 devices together and ANDing the $\overline{EF}$ outputs of all devices together. Since $\overline{FF}$ and $\overline{EF}$ are assertive-LOW signals, this 'ANDing' actually is implemented using an assertive-HIGH physical OR gate. The Half-Full Flag and the Retransmit function are not available in depth-cascaded mode.

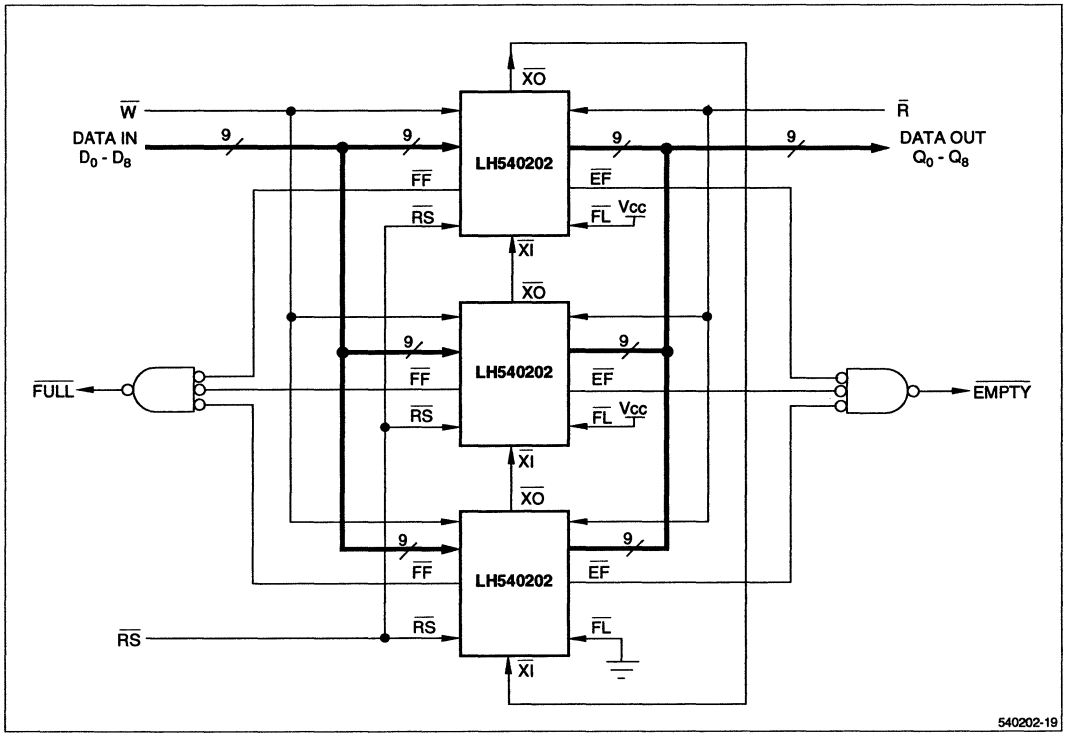


Figure 6. FIFO Depth Cascading (3072 × 9)

OPERATIONAL MODES (cont'd)

Compound FIFO Expansion

A combination of word-width expansion and depth cascading may be implemented easily by operating groups of depth-cascaded FIFOs in parallel.

Bidirectional FIFO Operation

Bidirectional data buffering between two systems may be implemented by operating LH540202 devices in parallel, but in opposite directions. The Data In inputs of each LH540202 are tied to the corresponding Data Out outputs of another LH540202, which is operating in the opposite direction, to form a single bidirectional bus interface. Care must be taken to assure that the appropriate read, write, and flag signals are routed to each system. Both word-width expansion and depth cascading may be used in bidirectional applications.

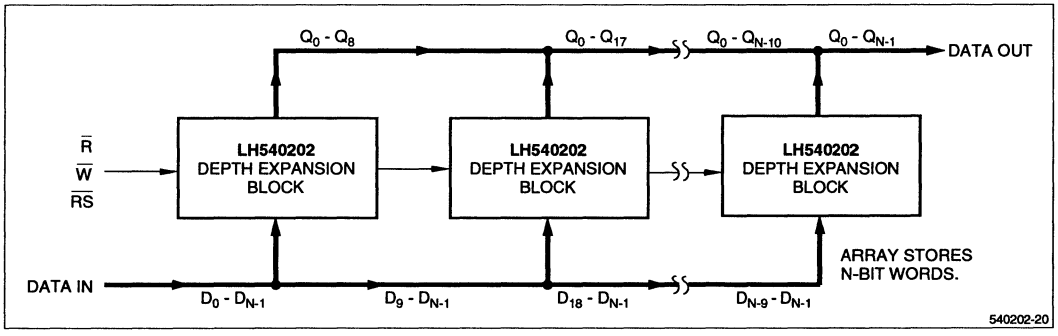


Figure 7. Compound FIFO Expansion

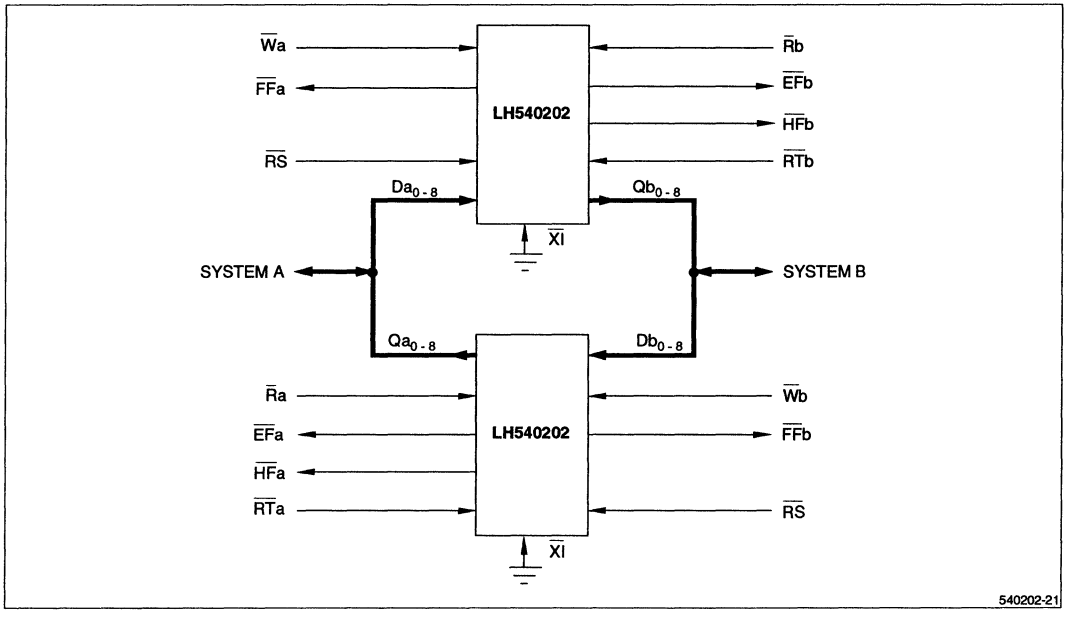


Figure 8. Bidirectional FIFO Operation (1024 × 9 × 2)

ABSOLUTE MAXIMUM RATINGS [1]

PARAMETER	RATING
Supply Voltage to V_{SS} Potential	−0.5 V to 7 V
Signal Pin Voltage to V_{SS} Potential [2]	−0.5 V to V_{CC} + 0.5 V (not to exceed 7 V)
DC Output Current [3]	± 50 mA
Storage Temperature Range	−65°C to 150°C
Power Dissipation (Package Limit)	1.0 W
DC Voltage Applied to Outputs In High-Z State	−0.5 V to V_{CC} + 0.5 V (not to exceed 7 V)

NOTES:

1. Stresses greater than those listed under 'Absolute Maximum Ratings' may cause permanent damage to the device. This is a stress rating for transient conditions only. Functional operation of the device at these or any other conditions outside of those indicated in the 'Operating Range' of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Negative undershoots of 1.5 V in amplitude are permitted for up to 10 ns once per cycle.
3. Outputs should not be shorted for more than 30 seconds. No more than one output should be shorted at any time.

OPERATING RANGE

SYMBOL	PARAMETER	MIN	MAX	UNIT
T_A	Temperature, Ambient	0	70	°C
V_{CC}	Supply Voltage	4.5	5.5	V
V_{SS}	Supply Voltage	0	0	V
V_{IL}	Logic LOW Input Voltage [1]	−0.5	0.8	V
V_{IH}	Logic HIGH Input Voltage	2.0	V_{CC} + 0.5	V

NOTE:

1. Negative undershoots of 1.5 V in amplitude are permitted for up to 10 ns once per cycle.

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
I_{LI}	Input Leakage Current	V_{CC} = 5.5 V, V_{IN} = 0 V to V_{CC}	−10	10	µA
I_{LO}	Output Leakage Current	$\overline{R} \geq V_{IH}$, 0 V ≤ V_{OUT} ≤ V_{CC}	−10	10	µA
V_{OH}	Output HIGH Voltage	I_{OH} = −2.0 mA	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 8.0 mA		0.4	V
I_{CC}	Average Supply Current [1]	Measured at f = 40 MHz		100	mA
I_{CC2}	Average Standby Current [1]	All Inputs = V_{IH}		15	mA
I_{CC3}	Power Down Current [1]	All Inputs = V_{CC} − 0.2V		5	mA

NOTE:

1. I_{CC}, I_{CC2}, and I_{CC3} are dependent upon actual output loading and cycle rates. Specified values are with outputs open.

AC TEST CONDITIONS

PARAMETER	RATING
Input Pulse Levels	Vss to 3 V
Input Rise and Fall Times (10% to 90%)	5 ns
Input Timing Reference Levels	1.5 V
Output Reference Levels	1.5 V
Output Load, Timing Tests	Figure 9

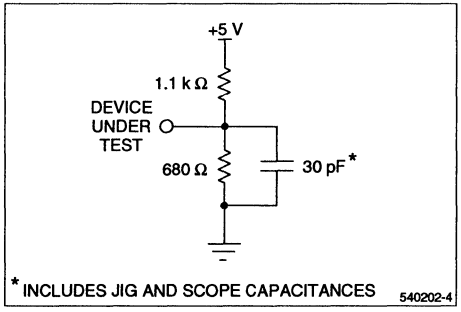


Figure 9. Output Load Circuit

CAPACITANCE [1,2]

PARAMETER	RATING
C_{IN} (Input Capacitance)	5 pF
C_{OUT} (Output Capacitance)	7 pF

NOTES:

1. Sample tested only.
2. Capacitances are maximum values at 25°C, measured at 1.0 MHz, with V_{IN} = 0 V.

AC ELECTRICAL CHARACTERISTICS [1] (Over Operating Range)

SYMBOL	PARAMETER	t_A = 15 ns		t_A = 20 ns		t_A = 25 ns		t_A = 35 ns		t_A = 50 ns		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
READ CYCLE TIMING												
t_{RC}	Read Cycle Time	25	–	30	–	35	–	45	–	65	–	ns
t_A	Access Time	–	15	–	20	–	25	–	35	–	50	ns
t_{RR}	Read Recovery Time	10	–	10	–	10	–	10	–	15	–	ns
t_{RPW}	Read Pulse Width [2]	15	–	20	–	25	–	35	–	50	–	ns
t_{RLZ}	Data Bus Active from Read LOW [3]	5	–	5	–	5	–	5	–	5	–	ns
t_{WLZ}	Data Bus Active from Write HIGH [4,5]	10	–	10	–	10	–	10	–	10	–	ns
t_{DV}	Data Valid from Read Pulse HIGH	5	–	5	–	5	–	5	–	5	–	ns
t_{RHZ}	Data Bus High-Z from Read HIGH [3]	–	15	–	15	–	15	–	15	–	20	ns
WRITE CYCLE TIMING												
t_{WC}	Write Cycle Time	25	–	30	–	35	–	45	–	65	–	ns
t_{WPW}	Write Pulse Width [2]	15	–	20	–	25	–	35	–	50	–	ns
t_{WR}	Write Recovery Time	10	–	10	–	10	–	10	–	15	–	ns
t_{DS}	Data Setup Time	10	–	10	–	10	–	15	–	20	–	ns
t_{DH}	Data Hold Time	0	–	0	–	0	–	0	–	0	–	ns
RESET TIMING												
t_{RSC}	Reset Cycle Time	25	–	30	–	35	–	45	–	65	–	ns
t_{RS}	Reset Pulse Width [2]	15	–	20	–	25	–	35	–	50	–	ns
t_{RSR}	Reset Recovery Time	10	–	10	–	10	–	10	–	15	–	ns
RETRANSMIT TIMING [5]												
t_{RTC}	Retransmit Cycle Time	25	–	30	–	35	–	45	–	65	–	ns
t_{RT}	Retransmit Pulse Width [2]	15	–	20	–	25	–	35	–	50	–	ns
t_{RTR}	Retransmit Recovery Time	10	–	10	–	10	–	10	–	15	–	ns
t_{RRSS}	Read HIGH to $\overline{RS}$ HIGH	15	–	20	–	25	–	35	–	50	–	ns
t_{WRSS}	Write HIGH to $\overline{RS}$ HIGH	15	–	20	–	25	–	35	–	50	–	ns
FLAG TIMING												
t_{EFL}	Reset LOW to Empty Flag LOW	–	25	–	30	–	35	–	45	–	65	ns
$t_{HFH,FFH}$	Reset LOW to Half-Full and Full Flags HIGH	–	25	–	30	–	35	–	45	–	65	ns
t_{REF}	Read LOW to Empty Flag LOW	–	15	–	20	–	25	–	35	–	45	ns
t_{RFF}	Read HIGH to Full Flag HIGH	–	15	–	20	–	25	–	35	–	45	ns
t_{WEF}	Write HIGH to Empty Flag HIGH	–	15	–	20	–	25	–	35	–	45	ns
t_{WFF}	Write LOW to Full Flag LOW	–	15	–	20	–	25	–	35	–	45	ns
t_{WHF}	Write LOW to Half-Full Flag LOW	–	15	–	20	–	25	–	35	–	45	ns
t_{RHF}	Read HIGH to Half-Full Flag HIGH	–	15	–	20	–	25	–	35	–	45	ns
EXPANSION TIMING												
t_{XOL}	Expansion Out LOW	–	18	–	20	–	25	–	35	–	50	ns
t_{XOH}	Expansion Out HIGH	–	18	–	20	–	25	–	35	–	50	ns
t_{XI}	Expansion In Pulse Width	15	–	20	–	25	–	35	–	50	–	ns
t_{XIR}	Expansion In Recovery Time	10	–	10	–	10	–	10	–	10	–	ns
t_{XIS}	Expansion in Setup Time	7	–	10	–	10	–	15	–	15	–	ns

NOTES:

1. All timing measurements are performed at 'AC Test Condition' levels.
2. Pulse widths less than minimum value are not allowed.
3. Values are guaranteed by design; not currently tested.
4. Only applies to read-data flow-through mode.
5. See also Note 2, Figure 19.

TIMING DIAGRAMS

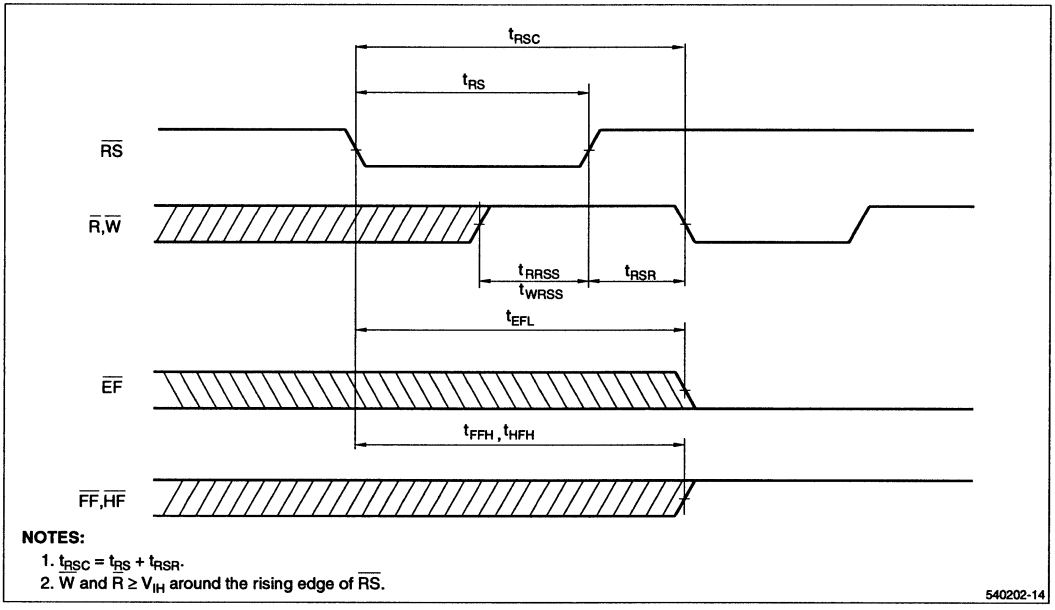


Figure 10. Reset Timing

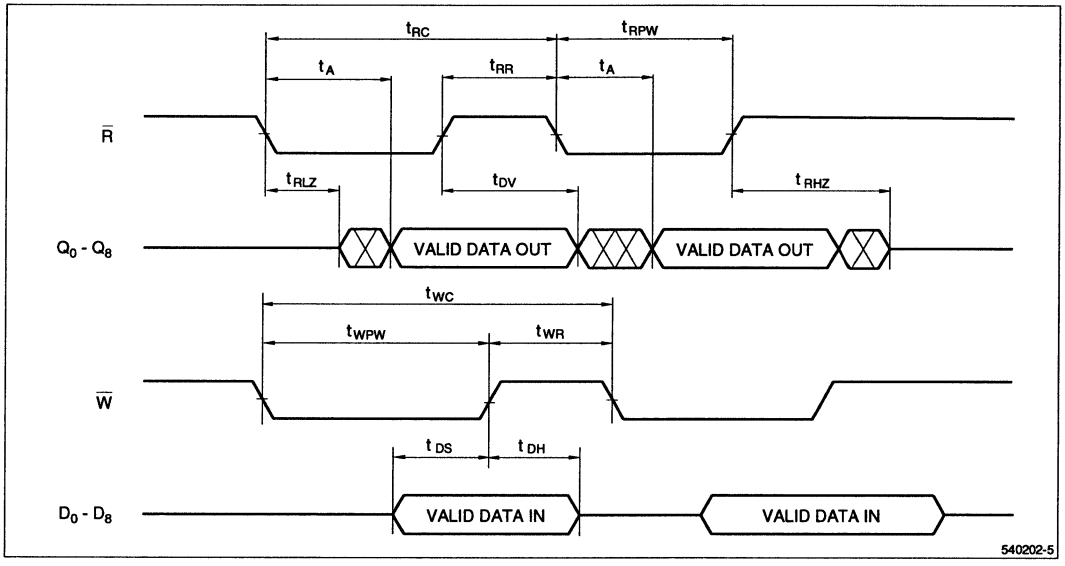


Figure 11. Asynchronous Write and Read Operation

TIMING DIAGRAMS (cont'd)

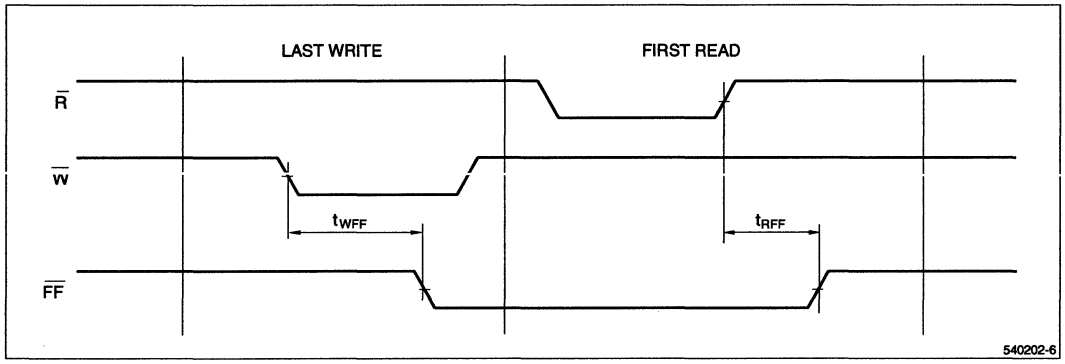


Figure 12. Full Flag From Last Write to First Read

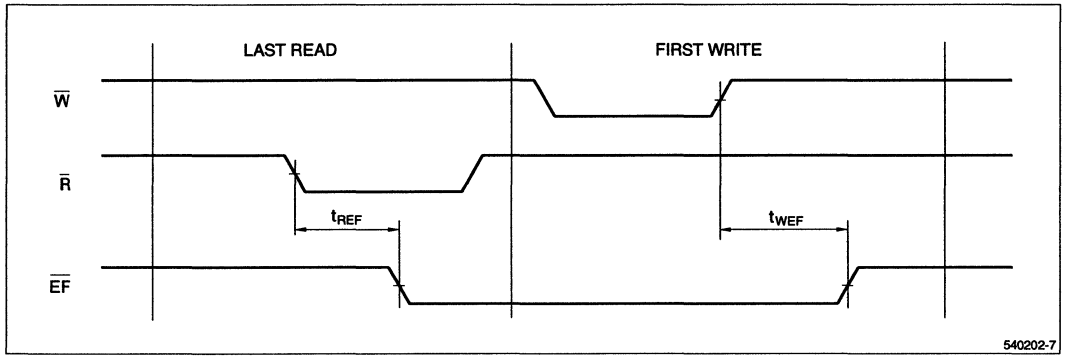
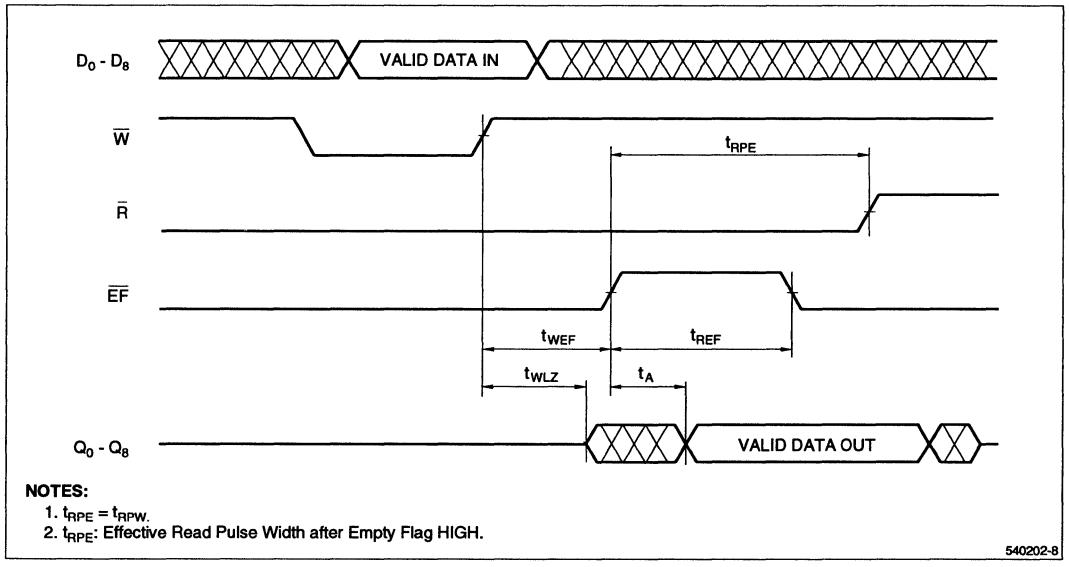


Figure 13. Empty Flag From Last Read to First Write

TIMING DIAGRAMS (cont'd)



NOTES:
1. $t_{RPE} = t_{RPW}$.
2. t_{RPE}: Effective Read Pulse Width after Empty Flag HIGH.

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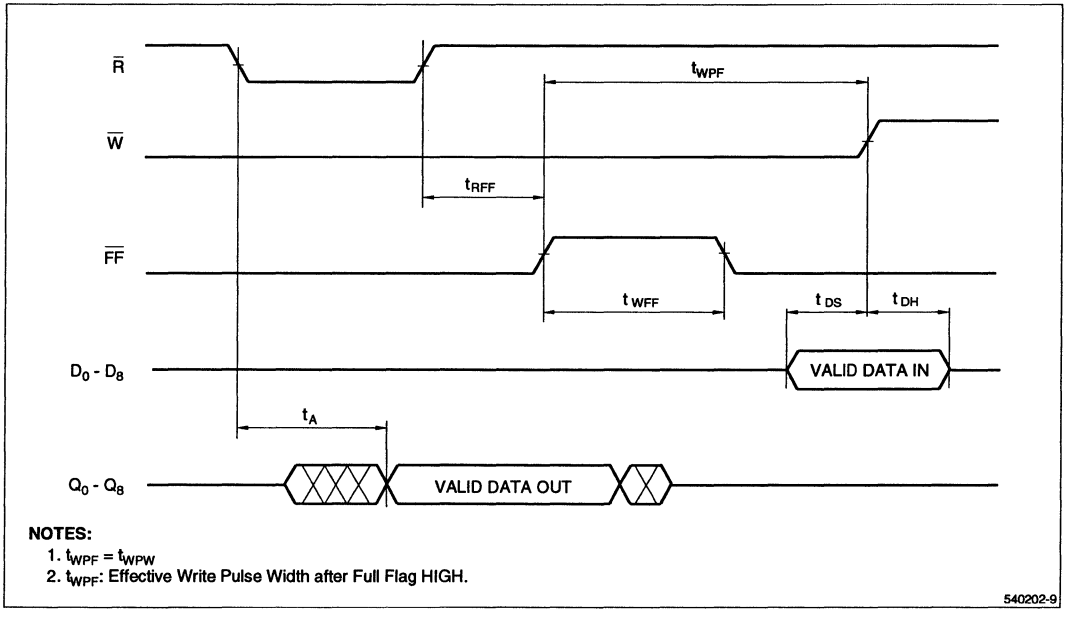
Figure 14. Read Data Flow-Through



NOTES:
1. $t_{WPF} = t_{WPW}$
2. t_{WPF}: Effective Write Pulse Width after Full Flag HIGH.

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Figure 15. Write Data Flow-Through

TIMING DIAGRAMS (cont'd)

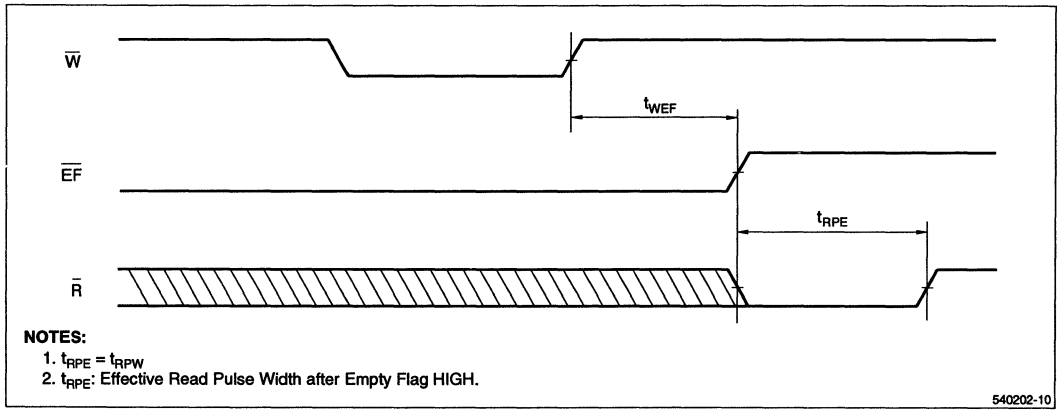


Figure 16. Empty Flag Timing

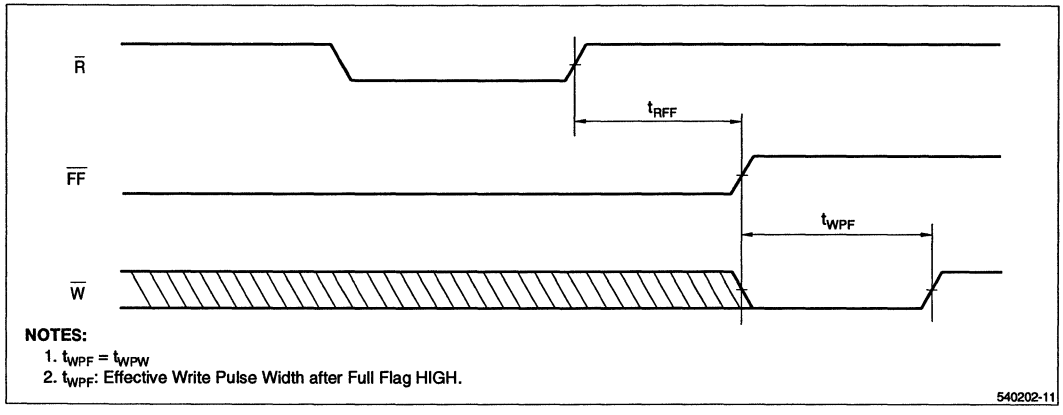


Figure 17. Full Flag Timing

TIMING DIAGRAMS (cont'd)

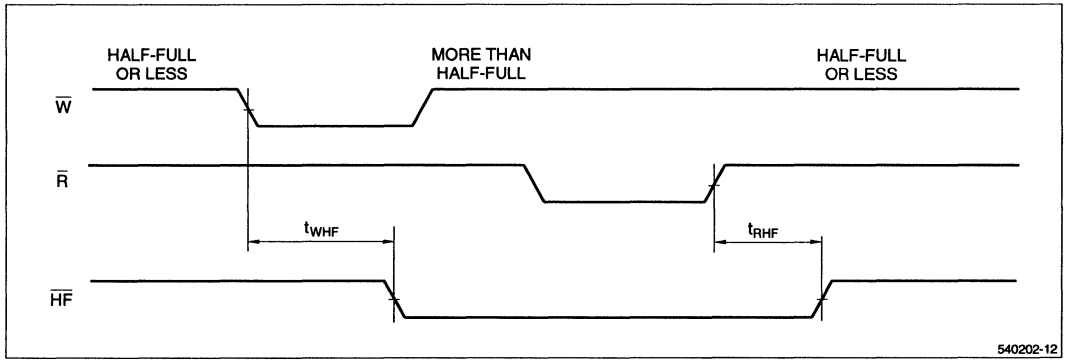


Figure 18. Half-Full Flag Timing

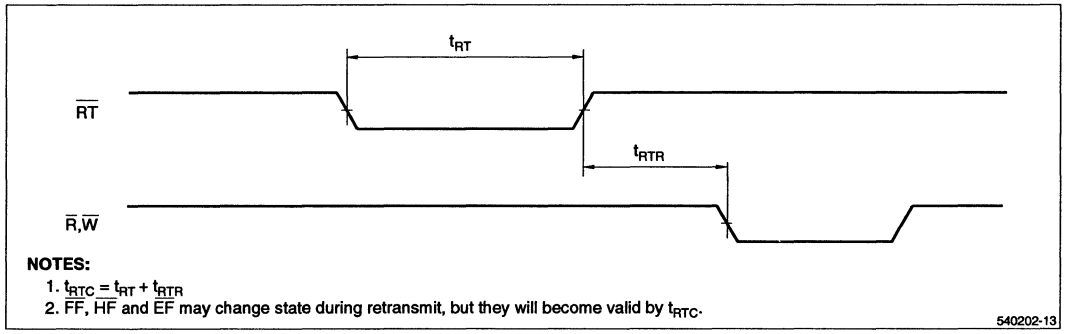


Figure 19. Retransmit Timing

TIMING DIAGRAMS (cont'd)

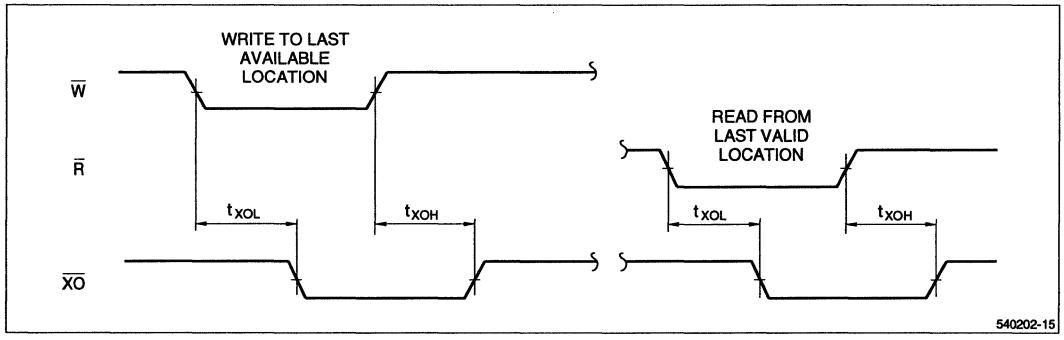


Figure 20. Expansion-Out Timing

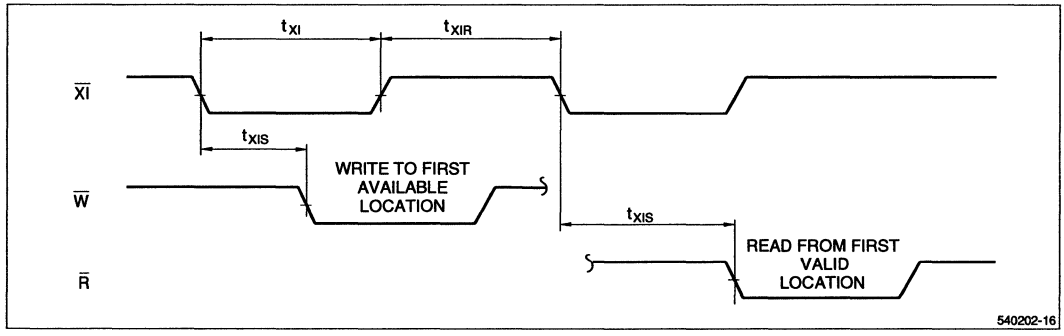
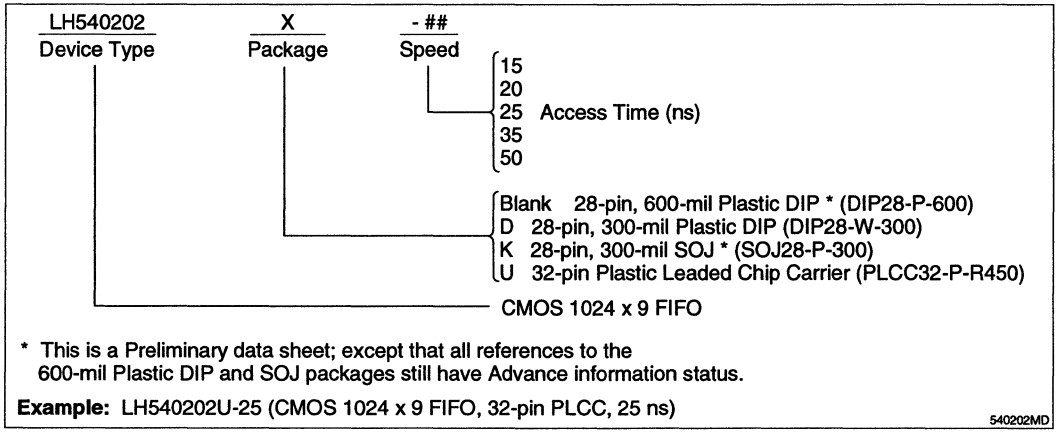


Figure 21. Expansion-In Timing

ORDERING INFORMATION



LH540203

PRELIMINARY

CMOS 2048 × 9 Asynchronous FIFO

FEATURES

- Fast Access Times: 15/20/25/35/50 ns
- Fast-Fall-Through Time Architecture Based on CMOS Dual-Port SRAM Technology
- Input Port and Output Port Have Entirely Independent Timing
- Expandable in Width and Depth
- Full, Half-Full, and Empty Status Flags
- Data Retransmission Capability
- TTL-Compatible I/O
- Pin and Functionally Compatible with Sharp LH5498 and with Am/IDT/MS7203
- Control Signals Assertive-LOW for Noise Immunity
- Packages:
  - 28-Pin, 300-mil PDIP
  - 28-Pin, 600-mil PDIP *
  - 28-Pin, 300-mil SOJ *
  - 32-Pin PLCC

FUNCTIONAL DESCRIPTION

The LH540203 is a FIFO (First-In, First-Out) memory device, based on fully-static CMOS dual-port SRAM technology, capable of storing up to 2048 nine-bit words. It follows the industry-standard architecture and package pinouts for nine-bit asynchronous FIFOs. Each nine-bit LH540203 word may consist of a standard eight-bit byte, together with a parity bit or a block-marking/framing bit.

The input and output ports operate entirely independently of each other, unless the LH540203 becomes either totally full or else totally empty. Data flow at a port is initiated by asserting either of two asynchronous, assertive-LOW control inputs: Write ($\overline{W}$) for data entry at the input port, or Read ($\overline{R}$) for data retrieval at the output port.

Full, Half-Full, and Empty status flags monitor the extent to which the internal memory has been filled. The system may make use of these status outputs to avoid the risk of data loss, which otherwise might occur either by attempting to write additional words into an already-full LH540203, or by attempting to read additional words from an already-empty LH540203. When an LH540203 is operating in a depth-cascaded configuration, the Half-Full Flag is not available.

PIN CONNECTIONS

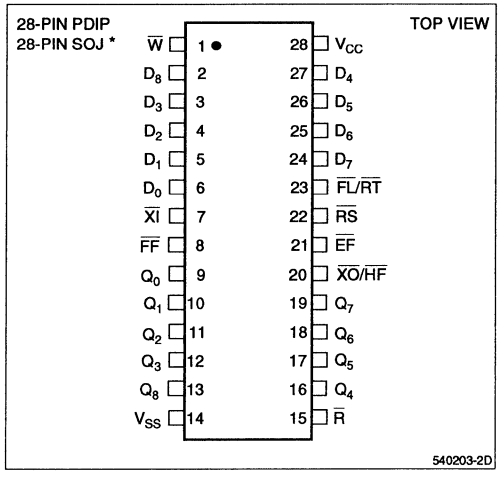


Figure 1. Pin Connections for PDIP * and SOJ * Packages

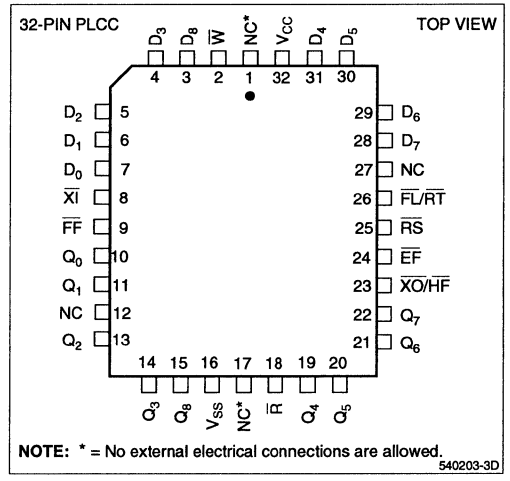


Figure 2. Pin Connections for PLCC Package

* This is a Preliminary data sheet; except that all references to the 600-mil PDIP and SOJ packages still have Advance Information status.

FUNCTIONAL DESCRIPTION (cont'd)

Data words are read out from the LH540203's output port in precisely the same order that they were written in at its input port; that is, according to a First-In, First Out (FIFO) queue discipline. Since the addressing sequence for a FIFO device's memory is internally predefined, no external addressing information is required for the operation of the LH540203 device.

Drop-in-replacement compatibility is maintained with both larger sizes and smaller sizes of industry-standard nine-bit asynchronous FIFOs. The only change is in the number of internally-stored data words implied by the states of the Full Flag and the Half-Full Flag.

The Retransmit ($\overline{RT}$) control signal causes the internal FIFO-memory-array read-address pointer to be set back to zero, to point to the LH540203's first physical memory location, without affecting the internal FIFO-memory-array write-address pointer. Thus, the Retransmit control signal provides a mechanism whereby a block of data, delimited by the zero physical address and the current write-address-pointer value, may be read out *repeatedly* an arbitrary number of times. The only restrictions are that neither the read-address pointer nor the write-address pointer may 'wrap around' during this entire process, i.e., advance past physical location zero after traversing the entire memory. The retransmit facility is not available when an LH540203 is operating in a depth-expanded configuration.

The Reset ($\overline{RS}$) control signal returns the LH540203 to an initial state, empty and ready to be filled. An LH540203 should be reset during every system power-up sequence. A reset operation causes the internal FIFO-memory-array write-address pointer, as well as the read-address pointer, to be set back to zero, to point to the LH540203's first physical memory location. Any information which previously had been stored within the LH540203 is not recoverable after a reset operation.

A cascading (depth-expansion) scheme may be implemented by using the Expansion In ($\overline{XI}$) input signal and the Expansion Out ($\overline{XO/HF}$) output signal. This allows a deeper 'effective FIFO' to be implemented by using two or more LH540203 devices, without incurring additional latency ('fallthrough' or 'bubblethrough') delays, and without the necessity of storing and retrieving any given data word more than once. In this cascaded operating mode, one LH540203 device must be designated as the 'first-load' or 'master' device, by grounding its First-Load ($\overline{FL/RT}$) control input; the remaining LH540203 devices are designated as 'slaves,' by tying their $\overline{FL/RT}$ inputs HIGH. Because of the need to share control signals on pins, the Half-Full Flag and the retransmission capability are not available for either 'master' or 'slave' LH540203 devices operating in cascaded mode.

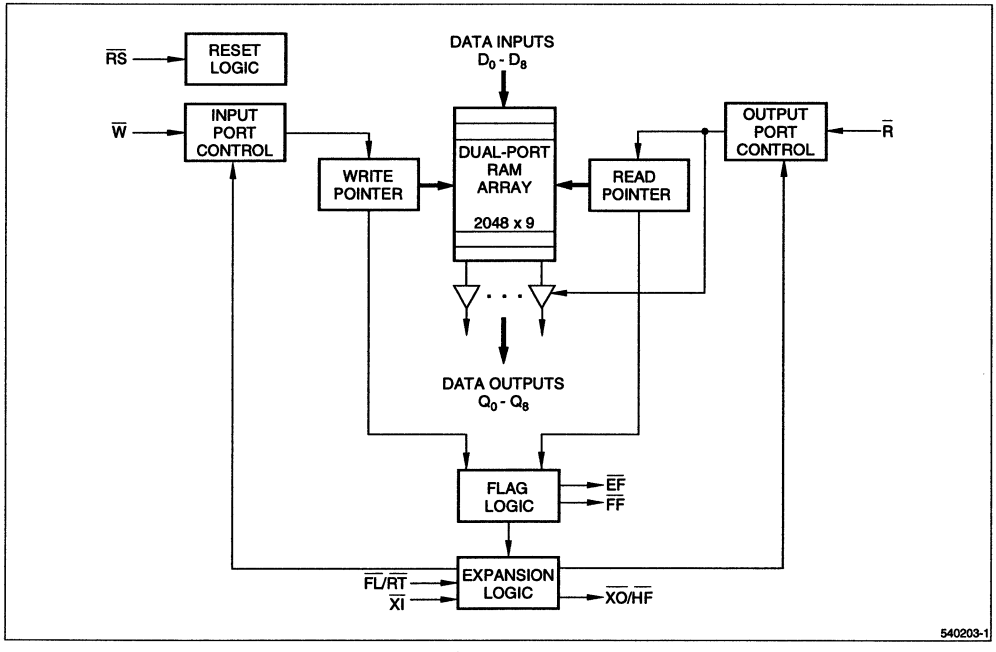


Figure 3. LH540203 Block Diagram

PIN DESCRIPTIONS

PIN	PIN TYPE *	DESCRIPTION
$D_0 - D_8$	I	Input Data Bus
$Q_0 - Q_8$	O/Z	Output Data Bus
$\overline{W}$	I	Write Request
$\overline{R}$	I	Read Request
$\overline{EF}$	O	Empty Flag
$\overline{FF}$	O	Full Flag

PIN	PIN TYPE *	DESCRIPTION
$\overline{XO/HF}$	O	Expansion Out/Half-Full Flag
$\overline{XI}$	I	Expansion In
$\overline{FL/RT}$	I	First Load/Retransmit
$\overline{RS}$	I	Reset
V_{CC}	V	Positive Power Supply
V_{SS}	V	Ground

* I = Input, O = Output, Z = High-Impedance, V = Power Voltage Level

OPERATIONAL DESCRIPTION

Reset

The LH540203 is reset whenever the Reset input ($\overline{RS}$) is taken LOW. A reset operation initializes both the read-address pointer and the write-address pointer to point to location zero, the first physical memory location. During a reset operation, the state of the $\overline{XI}$ and $\overline{FL/RT}$ inputs determines whether the device is in standalone mode or in depth-cascaded mode. (See Tables 1 and 2.)

A reset operation is required whenever the LH540203 first is powered up. The Read ($\overline{R}$) and Write ($\overline{W}$) inputs may be in any state when the reset operation is initiated; but they must be HIGH, before the reset operation is terminated by a rising edge of $\overline{RS}$, by a time t_{RRSS} (for Read) or t_{WRSS} (for Write) respectively. (See Figure 10.)

Write

A write cycle is initiated by a falling edge of the Write ($\overline{W}$) control input. Data setup times and hold times must be observed for the data inputs ($D_0 - D_8$). Write operations may occur independently of any ongoing read operations. However, a write operation is possible only if the FIFO is not full, (i.e., if the Full Flag $\overline{FF}$ is HIGH).

At the falling edge of $\overline{W}$ for the first write operation after the memory is half filled, the Half-Full Flag is asserted ($\overline{HF}$ = LOW). It remains asserted until the difference between the write pointer and the read pointer indicates that the data words remaining in the LH540203 are filling the FIFO memory to less than or equal to one-half of its total capacity. The Half-Full Flag is deasserted ($\overline{HF}$ = HIGH) by the appropriate rising edge of $\overline{R}$. (See Table 3.)

The Full Flag is asserted ($\overline{FF}$ = LOW) at the falling edge of $\overline{W}$ for the write operation which fills the last available location in the FIFO memory array. $\overline{FF}$ = LOW inhibits further write operations until $\overline{FF}$ is cleared by a valid read operation. The Full Flag is deasserted ($\overline{FF}$ = HIGH) after the next rising edge of $\overline{R}$ releases another memory location. (See Table 3.)

Read

A read cycle is initiated by a falling edge of the Read ($\overline{R}$) control input. Read data becomes valid at the data outputs ($Q_0 - Q_8$) after a time t_A from the falling edge of $\overline{R}$. After $\overline{R}$ goes HIGH, the data outputs return to a high-impedance state. Read operations may occur independently of any ongoing write operations. However, a read operation is possible only if the FIFO is not empty (i.e., if the Empty Flag $\overline{EF}$ is HIGH).

The LH540203's internal read-address and write-address pointers operate in such a way that consecutive read operations always access data words in the same order that they were written. The Empty Flag is asserted ($\overline{EF}$ = LOW) after that falling edge of $\overline{R}$ which accesses the last available data word in the FIFO memory. $\overline{EF}$ is deasserted ($\overline{EF}$ = HIGH) after the next rising edge of $\overline{W}$ loads another valid data word. (See Table 3.)

Data Flow-Through

Read-data flow-through mode occurs when the Read ($\overline{R}$) control input is brought LOW while the FIFO is empty, and is held LOW in anticipation of a write cycle. At the end of the next write cycle, the Empty Flag $\overline{EF}$ momentarily is deasserted, and the data word just written becomes available at the data outputs ($Q_0 - Q_8$) after a maximum time of $t_{WEF} + t_A$. Additional write operations may occur while the $\overline{R}$ input remains LOW; but only data from the first write operation flows through to the data outputs. Additional data words, if any, may be accessed only by toggling $\overline{R}$.

Write-data flow-through mode occurs when the Write ($\overline{W}$) input is brought LOW while the FIFO is full, and is held LOW in anticipation of a read cycle. At the end of the read cycle, the Full Flag momentarily is deasserted, but then immediately is reasserted in response to $\overline{W}$ being held LOW. A data word is written into the FIFO on the rising edge of $\overline{W}$, which may occur no sooner than $t_{RFF} + t_{WPW}$ after the read operation.

OPERATIONAL DESCRIPTION (cont'd)

Retransmit

The FIFO can be made to reread previously-read data by means of the Retransmit function. A retransmit operation is initiated by pulsing the $\overline{RT}$ input LOW. Both $\overline{R}$ and $\overline{W}$ must be deasserted (HIGH) for the duration of the retransmit pulse. The FIFO's internal read-address pointer is reset to point to location zero, the first physical memory location, while the internal write-address pointer remains unchanged.

After a retransmit operation, those data words in the region in between the read-address pointer and the write-address pointer may be reaccessed by subsequent read operations. A retransmit operation may affect the state of the status flags $\overline{FF}$, $\overline{HF}$, and $\overline{EF}$, depending on the relocation of the read-address pointer. There is no restriction on the number of times that a block of data within an LH540203 may be read out, by repeating the retransmit operation and the subsequent read operations.

The maximum length of a data block which may be retransmitted is 2048 words. Note that if the write-address pointer ever 'wraps around' (i.e., passes location zero more than once) during a sequence of retransmit operations, some data words will be lost.

The Retransmit function is not available when the LH540203 is operating in depth-cascaded mode, because the $\overline{FL}/\overline{RT}$ control pin must be used for first-load selection rather than for retransmission control.

Table 1. Grouping-Mode Determination During a Reset Operation

$\overline{XI}$	$\overline{FL}/\overline{RT}$	MODE	$\overline{XO}/\overline{HF}$ USAGE	$\overline{XI}$ USAGE	$\overline{FL}/\overline{RT}$ USAGE
H [1]	H	Cascaded Slave [2]	$\overline{XO}$	$\overline{XI}$	$\overline{FL}$
H [1]	L	Cascaded Master [2]	$\overline{XO}$	$\overline{XI}$	$\overline{FL}$
L	X	Standalone	$\overline{HF}$	(none)	$\overline{RT}$

NOTES:
1. A reset operation forces $\overline{XO}$ HIGH for the nth FIFO, thus forcing $\overline{XI}$ HIGH for the n+1st FIFO.
2. The terms 'master' and 'slave' refer to operation in depth-cascaded grouping mode.
3. H = HIGH; L = LOW; X = Don't Care.

Table 2. Expansion-Pin Usage According to Grouping Mode

I/O	PIN	STANDALONE	CASCADED MASTER	CASCADED SLAVE
I	$\overline{XI}$	Grounded	From $\overline{XO}$ (n-1st FIFO)	From $\overline{XO}$ (n-1st FIFO)
O	$\overline{XO}/\overline{HF}$	Becomes $\overline{HF}$	To $\overline{XI}$ (n+1st FIFO)	To $\overline{XI}$ (n+1st FIFO)
I	$\overline{FL}/\overline{RT}$	Becomes $\overline{RT}$	Grounded (Logic LOW)	Logic HIGH

Table 3. Status Flags

NUMBER OF UNREAD DATA WORDS PRESENT WITHIN 2048 × 9 FIFO	$\overline{FF}$	$\overline{HF}$	$\overline{EF}$
0	H	H	L
1 to 1024	H	H	H
1025 to 2047	H	L	H
2048	L	L	H

OPERATIONAL MODES

Standalone Configuration

When depth cascading is not required for a given application, the LH540203 is placed in standalone mode by tying the Expansion In input ($\overline{XI}$) to ground. This input is internally sampled during a reset operation. (See Table 1.)

Width Expansion

Word-width expansion is implemented by placing multiple LH540203 devices in parallel. Each LH540203 should be configured for standalone mode. In this arrangement, the behavior of the status flags is identical for all devices; so, in principle, a representative value for each of these flags could be derived from any one device. In practice, it is better to derive 'composite' flag values using external logic, since there may be minor speed variations between different actual devices. (See Figures 4, 5, and 6.)

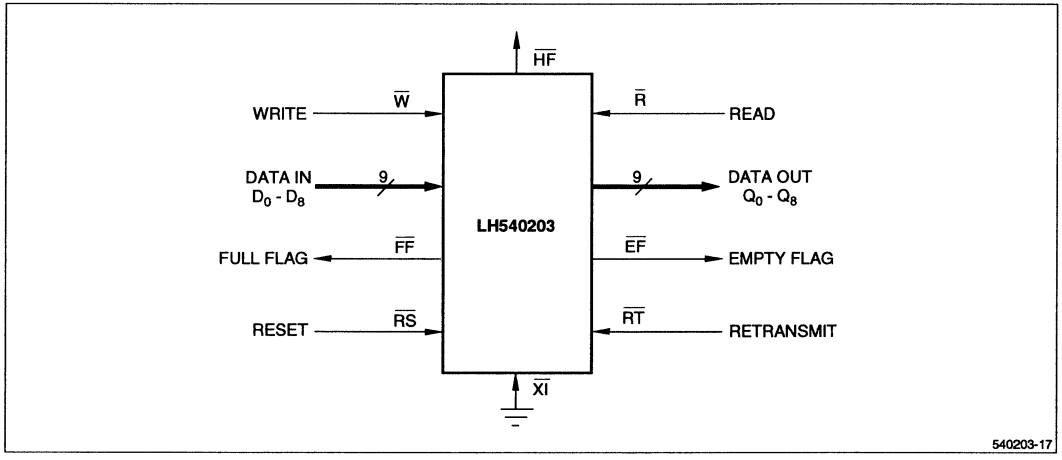


Figure 4. Standalone FIFO (2048 × 9)

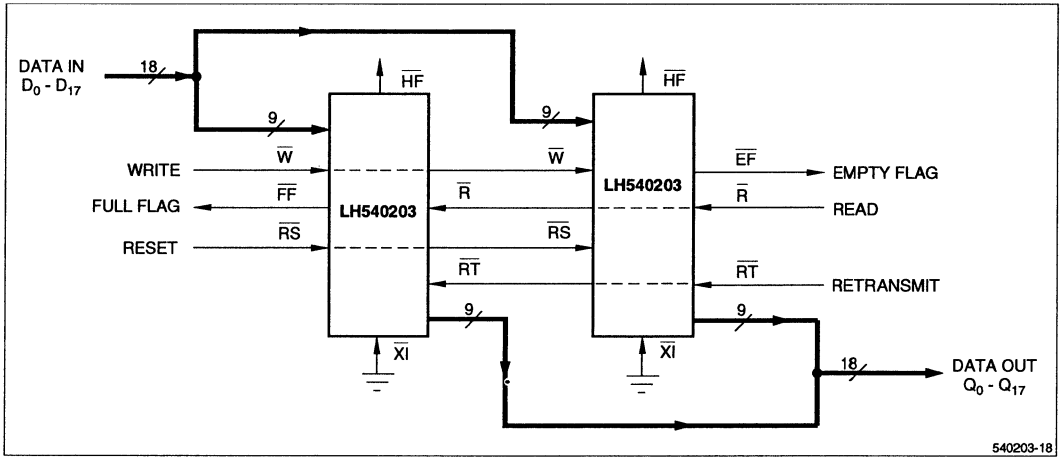


Figure 5. FIFO Word-Width Expansion (2048 × 18)

OPERATIONAL MODES (cont'd)

Depth Cascading

Depth cascading is implemented by configuring the required number of LH540203s in depth-cascaded mode. In this arrangement, the FIFOs are connected in a circular fashion, with the Expansion Out output ($\overline{XO}$) of each device tied to the Expansion In input ($\overline{XI}$) of the next device. One FIFO in the cascade must be designated as the 'first-load' device, by tying its First Load input ($\overline{FL}/\overline{RT}$) to ground. All other devices must have their $\overline{FL}/\overline{RT}$ inputs tied HIGH. In this mode, $\overline{W}$ and $\overline{R}$ signals are shared by all devices, while logic within each LH540203 controls the steering of data. Only one LH540203 is enabled during any given write cycle; thus, the common Data In inputs of all devices are tied together. Likewise, only one LH540203 is enabled during any given read cycle; thus, the common Data Out outputs of all devices are wire-ORed together.

In depth-cascaded mode, external logic should be used to generate a composite Full Flag and a composite Empty Flag, by ANDing the $\overline{FF}$ outputs of all LH540203 devices together and ANDing the $\overline{EF}$ outputs of all devices together. Since $\overline{FF}$ and $\overline{EF}$ are assertive-LOW signals, this 'ANDing' actually is implemented using an assertive-HIGH physical OR gate. The Half-Full Flag and the Retransmit function are not available in depth-cascaded mode.

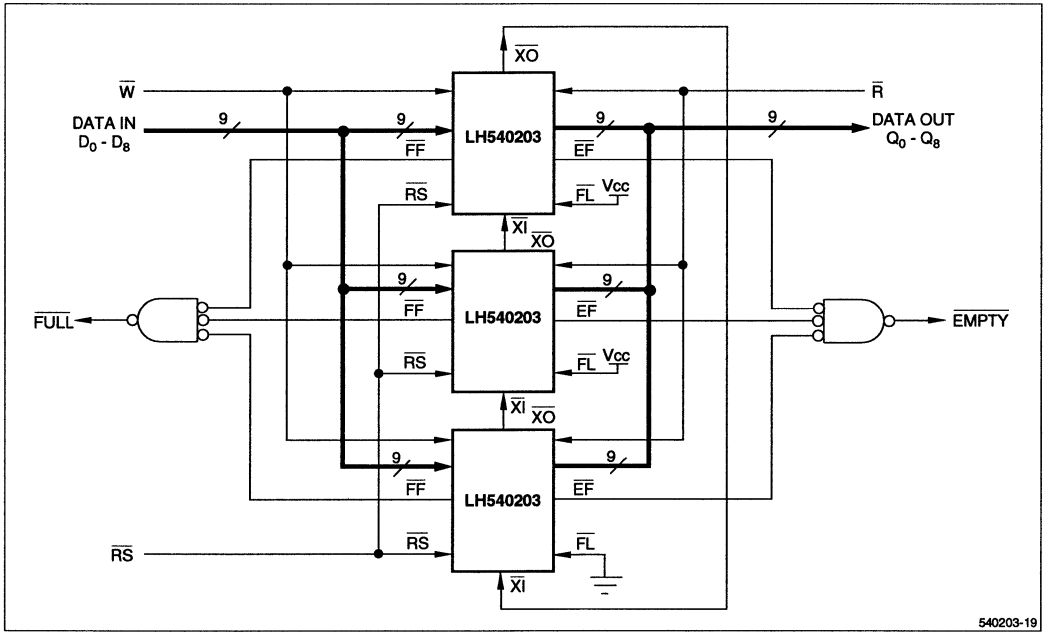


Figure 6. FIFO Depth Cascading (6144 × 9)

OPERATIONAL MODES (cont'd)

Compound FIFO Expansion

A combination of word-width expansion and depth cascading may be implemented easily by operating groups of depth-cascaded FIFOs in parallel.

Bidirectional FIFO Operation

Bidirectional data buffering between two systems may be implemented by operating LH540203 devices in parallel, but in opposite directions. The Data In inputs of each LH540203 are tied to the corresponding Data Out outputs of another LH540203, which is operating in the opposite direction, to form a single bidirectional bus interface. Care must be taken to assure that the appropriate read, write, and flag signals are routed to each system. Both word-width expansion and depth cascading may be used in bidirectional applications.

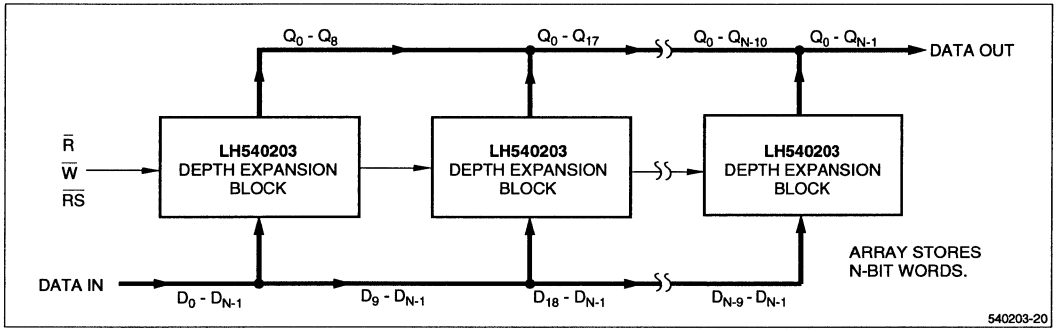


Figure 7. Compound FIFO Expansion

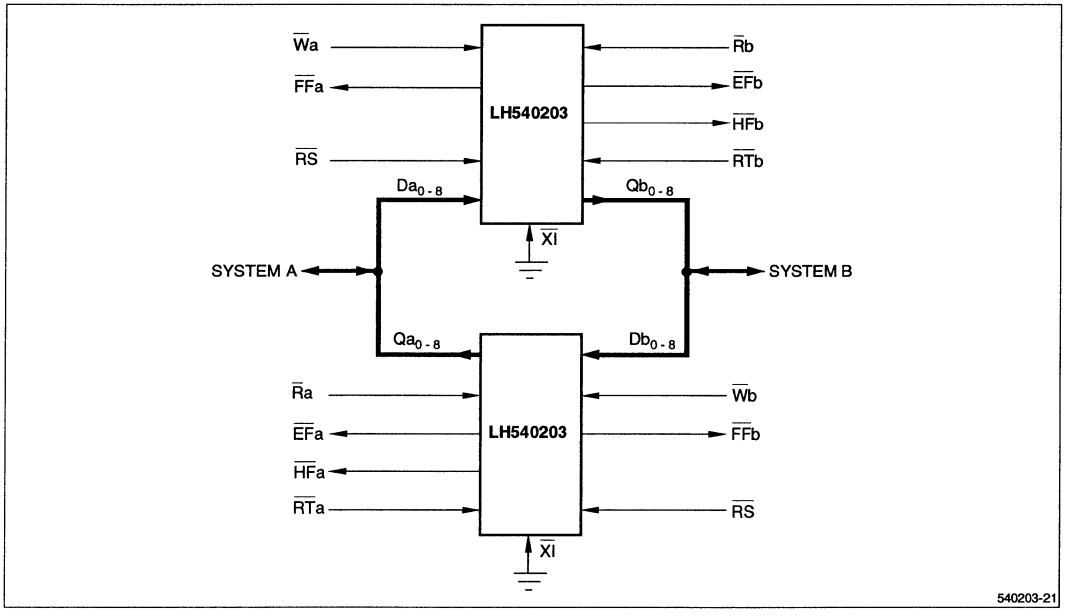


Figure 8. Bidirectional FIFO Operation (2048 × 9 × 2)

ABSOLUTE MAXIMUM RATINGS [1]

PARAMETER	RATING
Supply Voltage to V_{SS} Potential	−0.5 V to 7 V
Signal Pin Voltage to V_{SS} Potential [2]	−0.5 V to V_{CC} + 0.5 V (not to exceed 7 V)
DC Output Current [3]	± 50 mA
Storage Temperature Range	−65°C to 150°C
Power Dissipation (Package Limit)	1.0 W
DC Voltage Applied to Outputs In High-Z State	−0.5 V to V_{CC} + 0.5 V (not to exceed 7 V)

NOTES:

1. Stresses greater than those listed under 'Absolute Maximum Ratings' may cause permanent damage to the device. This is a stress rating for transient conditions only. Functional operation of the device at these or any other conditions outside of those indicated in the 'Operating Range' of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Negative undershoots of 1.5 V in amplitude are permitted for up to 10 ns once per cycle.
3. Outputs should not be shorted for more than 30 seconds. No more than one output should be shorted at any time.

OPERATING RANGE

SYMBOL	PARAMETER	MIN	MAX	UNIT
T_A	Temperature, Ambient	0	70	°C
V_{CC}	Supply Voltage	4.5	5.5	V
V_{SS}	Supply Voltage	0	0	V
V_{IL}	Logic LOW Input Voltage [1]	−0.5	0.8	V
V_{IH}	Logic HIGH Input Voltage	2.0	V_{CC} + 0.5	V

NOTE:

1. Negative undershoots of 1.5 V in amplitude are permitted for up to 10 ns once per cycle.

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
I_{LI}	Input Leakage Current	V_{CC} = 5.5 V, V_{IN} = 0 V to V_{CC}	−10	10	µA
I_{LO}	Output Leakage Current	$\overline{R} \geq V_{IH}$, 0 V ≤ V_{OUT} ≤ V_{CC}	−10	10	µA
V_{OH}	Output HIGH Voltage	I_{OH} = −2.0 mA	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 8.0 mA		0.4	V
I_{CC}	Average Supply Current [1]	Measured at f = 40 MHz		100	mA
I_{CC2}	Average Standby Current [1]	All Inputs = V_{IH}		15	mA
I_{CC3}	Power Down Current [1]	All Inputs = V_{CC} − 0.2V		5	mA

NOTE:

1. I_{CC}, I_{CC2}, and I_{CC3} are dependent upon actual output loading and cycle rates. Specified values are with outputs open.

AC TEST CONDITIONS

PARAMETER	RATING
Input Pulse Levels	V_{SS} to 3 V
Input Rise and Fall Times (10% to 90%)	5 ns
Input Timing Reference Levels	1.5 V
Output Reference Levels	1.5 V
Output Load, Timing Tests	Figure 9

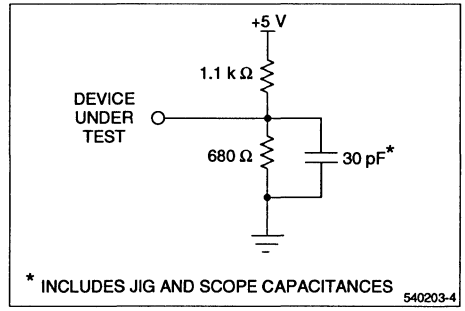


Figure 9. Output Load Circuit

CAPACITANCE [1,2]

PARAMETER	RATING
C_{IN} (Input Capacitance)	5 pF
C_{OUT} (Output Capacitance)	7 pF

NOTES:

1. Sample tested only.
2. Capacitances are maximum values at 25°C, measured at 1.0 MHz, with V_{IN} = 0 V.

AC ELECTRICAL CHARACTERISTICS [1] (Over Operating Range)

SYMBOL	PARAMETER	t_A = 15 ns		t_A = 20 ns		t_A = 25 ns		t_A = 35 ns		t_A = 50 ns		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
READ CYCLE TIMING												
t_{RC}	Read Cycle Time	25	–	30	–	35	–	45	–	65	–	ns
t_A	Access Time	–	15	–	20	–	25	–	35	–	50	ns
t_{RR}	Read Recovery Time	10	–	10	–	10	–	10	–	15	–	ns
t_{RPW}	Read Pulse Width [2]	15	–	20	–	25	–	35	–	50	–	ns
t_{RLZ}	Data Bus Active from Read LOW [3]	5	–	5	–	5	–	5	–	5	–	ns
t_{WLZ}	Data Bus Active from Write HIGH [4,5]	10	–	10	–	10	–	10	–	10	–	ns
t_{DV}	Data Valid from Read Pulse HIGH	5	–	5	–	5	–	5	–	5	–	ns
t_{RHZ}	Data Bus High-Z from Read HIGH [3]	–	15	–	15	–	15	–	15	–	20	ns
WRITE CYCLE TIMING												
t_{WC}	Write Cycle Time	25	–	30	–	35	–	45	–	65	–	ns
t_{WPW}	Write Pulse Width [2]	15	–	20	–	25	–	35	–	50	–	ns
t_{WR}	Write Recovery Time	10	–	10	–	10	–	10	–	15	–	ns
t_{DS}	Data Setup Time	10	–	10	–	10	–	15	–	20	–	ns
t_{DH}	Data Hold Time	0	–	0	–	0	–	0	–	0	–	ns
RESET TIMING												
t_{RSC}	Reset Cycle Time	25	–	30	–	35	–	45	–	65	–	ns
t_{RS}	Reset Pulse Width [2]	15	–	20	–	25	–	35	–	50	–	ns
t_{RSR}	Reset Recovery Time	10	–	10	–	10	–	10	–	15	–	ns
t_{RRSS}	Read HIGH to $\overline{RS}$ HIGH	15	–	20	–	25	–	35	–	50	–	ns
t_{WRSS}	Write HIGH to $\overline{RS}$ HIGH	15	–	20	–	25	–	35	–	50	–	ns
RETRANSMIT TIMING [5]												
t_{RTC}	Retransmit Cycle Time	25	–	30	–	35	–	45	–	65	–	ns
t_{RT}	Retransmit Pulse Width [2]	15	–	20	–	25	–	35	–	50	–	ns
t_{RTR}	Retransmit Recovery Time	10	–	10	–	10	–	10	–	15	–	ns
FLAG TIMING												
t_{EFL}	Reset LOW to Empty Flag LOW	–	25	–	30	–	35	–	45	–	65	ns
$t_{HFH,FFH}$	Reset LOW to Half-Full and Full Flags HIGH	–	25	–	30	–	35	–	45	–	65	ns
t_{REF}	Read LOW to Empty Flag LOW	–	15	–	20	–	25	–	35	–	45	ns
t_{RFF}	Read HIGH to Full Flag HIGH	–	15	–	20	–	25	–	35	–	45	ns
t_{WEF}	Write HIGH to Empty Flag HIGH	–	15	–	20	–	25	–	35	–	45	ns
t_{WFF}	Write LOW to Full Flag LOW	–	15	–	20	–	25	–	35	–	45	ns
t_{WHF}	Write LOW to Half-Full Flag LOW	–	15	–	20	–	25	–	35	–	45	ns
t_{RHF}	Read HIGH to Half-Full Flag HIGH	–	15	–	20	–	25	–	35	–	45	ns
EXPANSION TIMING												
t_{XOL}	Expansion Out LOW	–	18	–	20	–	25	–	35	–	50	ns
t_{XOH}	Expansion Out HIGH	–	18	–	20	–	25	–	35	–	50	ns
t_{XI}	Expansion In Pulse Width	15	–	20	–	25	–	35	–	50	–	ns
t_{XIR}	Expansion In Recovery Time	10	–	10	–	10	–	10	–	10	–	ns
t_{XIS}	Expansion in Setup Time	7	–	10	–	10	–	15	–	15	–	ns

NOTES:

1. All timing measurements are performed at 'AC Test Condition' levels.
2. Pulse widths less than minimum value are not allowed.
3. Values are guaranteed by design; not currently tested.
4. Only applies to read-data flow-through mode.
5. See also Note 2, Figure 19.

TIMING DIAGRAMS

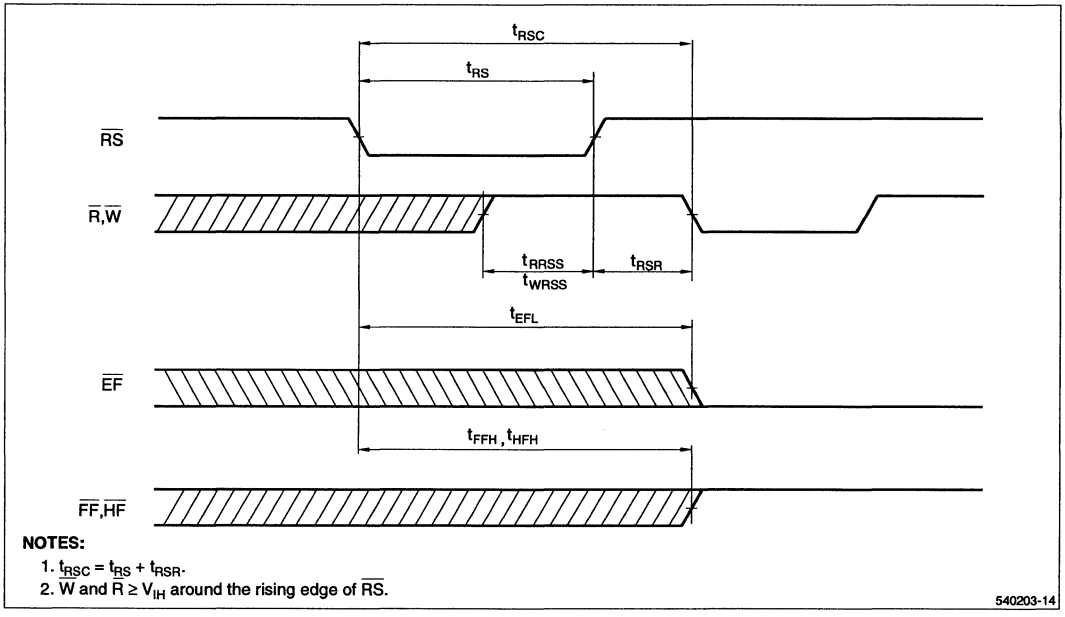


Figure 10. Reset Timing

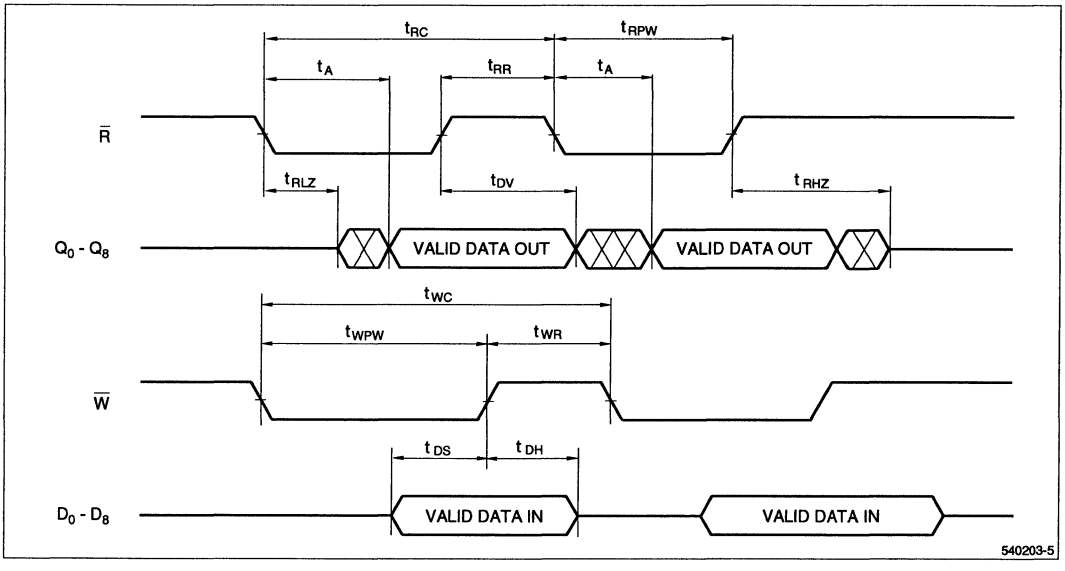


Figure 11. Asynchronous Write and Read Operation

TIMING DIAGRAMS (cont'd)

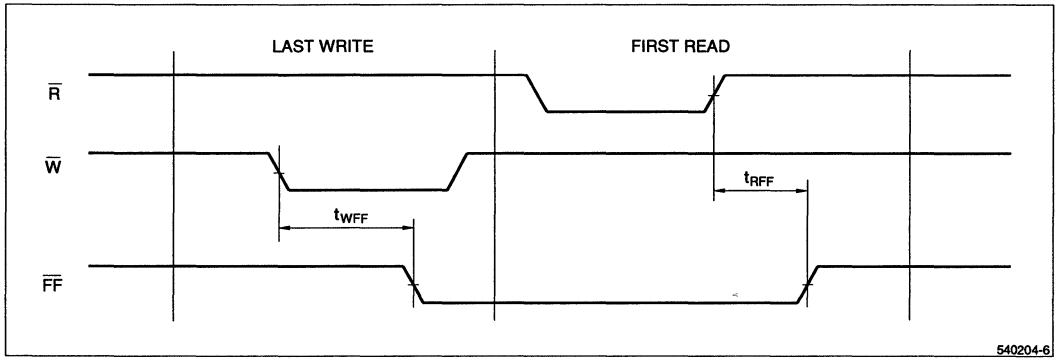


Figure 12. Full Flag From Last Write to First Read

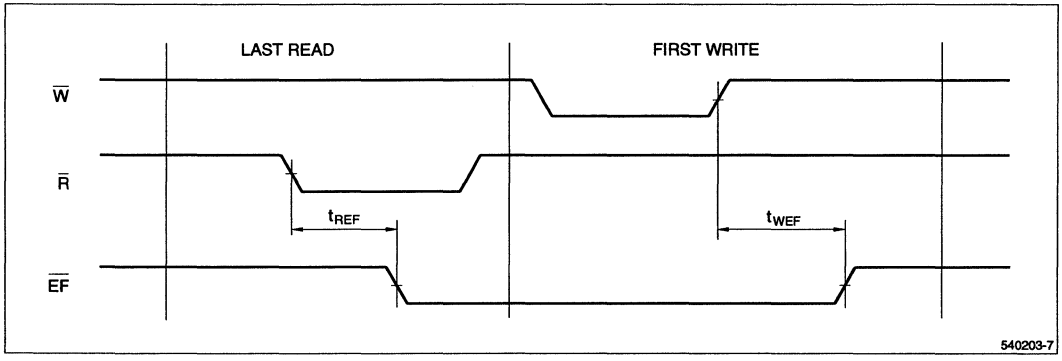
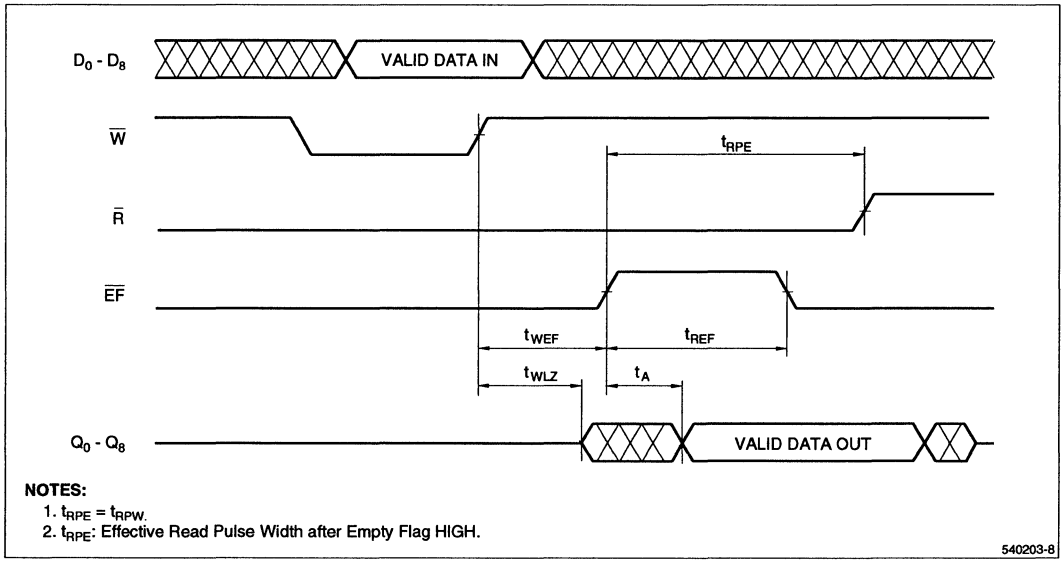


Figure 13. Empty Flag From Last Read to First Write

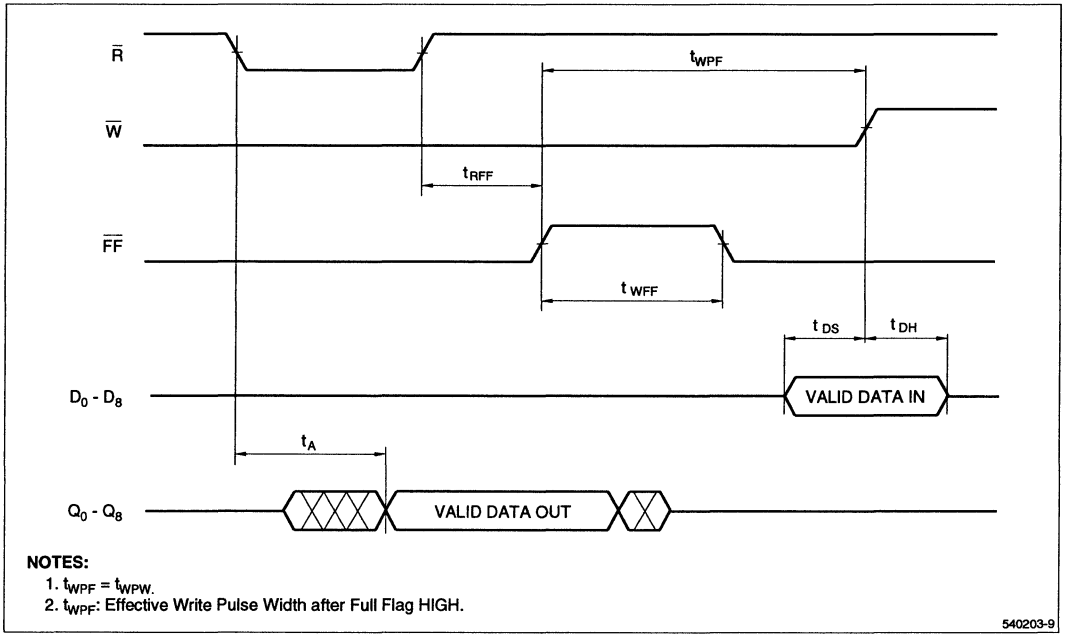
TIMING DIAGRAMS (cont'd)



NOTES:
1. $t_{RPE} = t_{RPW}$.
2. t_{RPE}: Effective Read Pulse Width after Empty Flag HIGH.

540203-8

Figure 14. Read Data Flow-Through

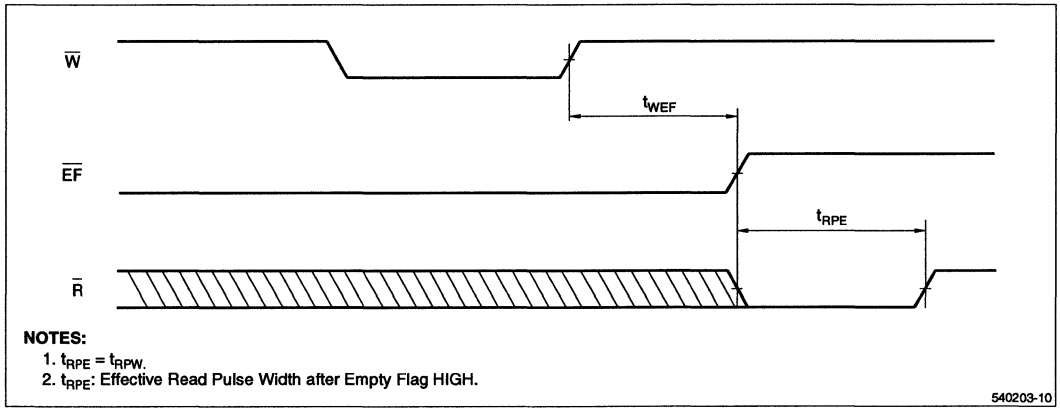


NOTES:
1. $t_{WPF} = t_{WPW}$.
2. t_{WPF}: Effective Write Pulse Width after Full Flag HIGH.

540203-9

Figure 15. Write Data Flow-Through

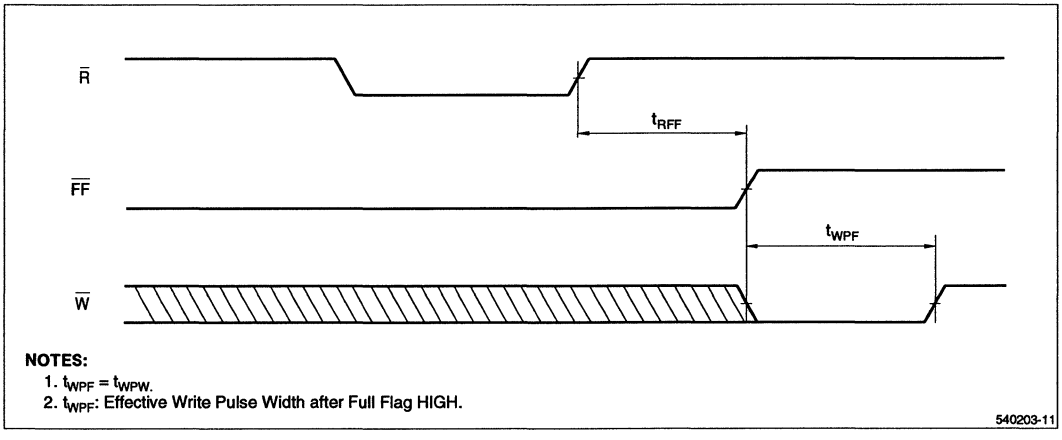
TIMING DIAGRAMS (cont'd)



NOTES:
1. $t_{RPE} = t_{RPW}$.
2. t_{RPE}: Effective Read Pulse Width after Empty Flag HIGH.

540203-10

Figure 16. Empty Flag Timing



NOTES:
1. $t_{WPF} = t_{WPW}$.
2. t_{WPF}: Effective Write Pulse Width after Full Flag HIGH.

540203-11

Figure 17. Full Flag Timing

TIMING DIAGRAMS (cont'd)

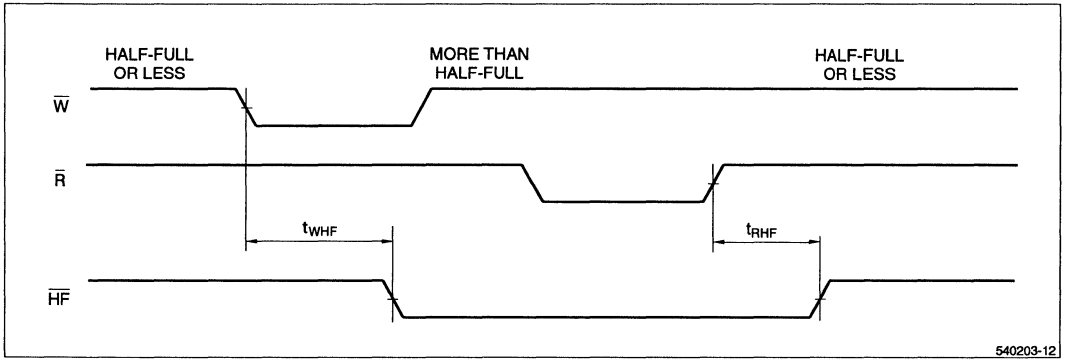


Figure 18. Half-Full Flag Timing

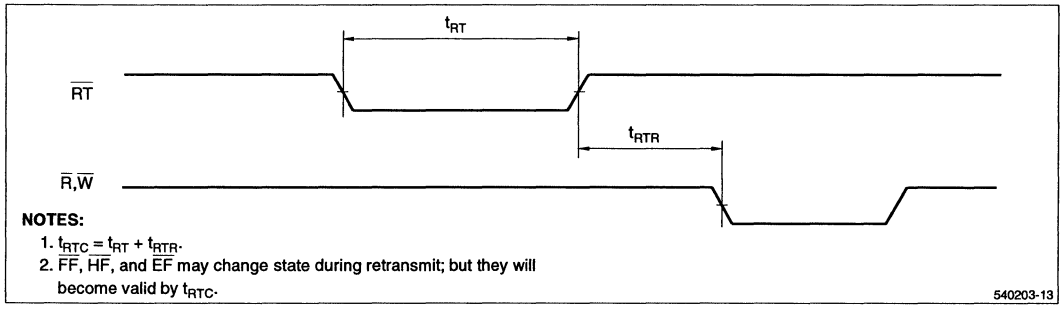


Figure 19. Retransmit Timing

TIMING DIAGRAMS (cont'd)

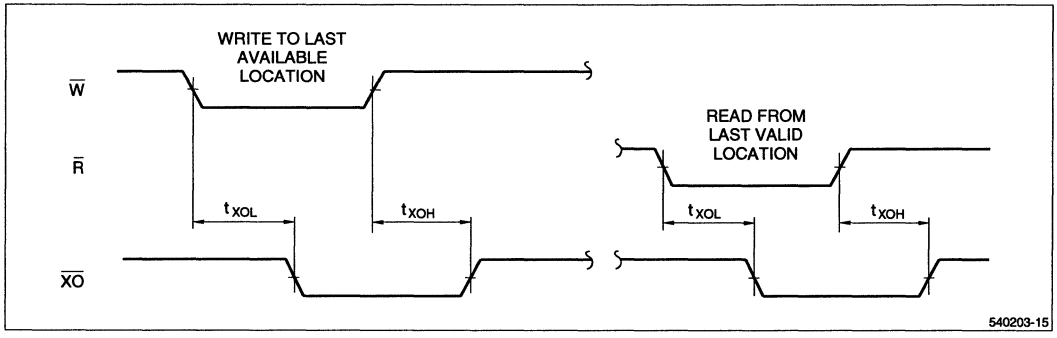


Figure 20. Expansion-Out Timing

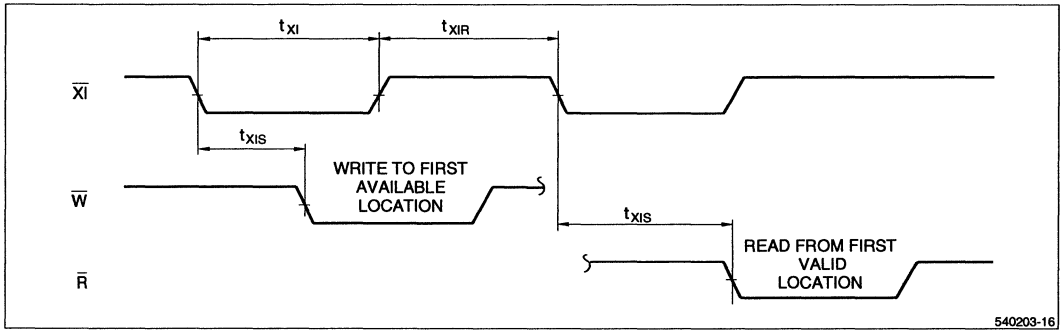


Figure 21. Expansion-In Timing

ORDERING INFORMATION

LH540203	X	- ##
Device Type	Package	Speed

Speed:
- 15
- 20
- 25 Access Time (ns)
- 35
- 50

Package:
- Blank 28-pin, 600-mil Plastic DIP * (DIP28-P-600)
- D 28-pin, 300-mil Plastic DIP (DIP28-W-300)
- K 28-pin, 300-mil SOJ * (SOJ28-P-300)
- U 32-pin Plastic Leaded Chip Carrier (PLCC32-P-R450)

Device Type:
- CMOS 2048 x 9 FIFO

* This is a Preliminary data sheet; except that all references to the 600-mil Plastic DIP and SOJ packages still have Advance information status.

Example: LH540203U-25 (CMOS 2048 x 9 FIFO, 32-pin PLCC, 25 ns)

540203MD

LH540204

ADVANCE INFORMATION

CMOS 4096 × 9 Asynchronous FIFO

FEATURES

- Fast Access Times: 20/25/35/50 ns
- Fast-Fall-Through Time Architecture Based on CMOS Dual-Port SRAM Technology
- Input Port and Output Port Have Entirely Independent Timing
- Expandable in Width and Depth
- Full, Half-Full, and Empty Status Flags
- Data Retransmission Capability
- TTL-Compatible I/O
- Pin and Functionally Compatible with Sharp LH5499 and with Am/IDT/MS7204
- Control Signals Assertive-LOW for Noise Immunity
- Packages:
  - 28-Pin, 300-mil PDIP
  - 28-Pin, 600-mil PDIP *
  - 28-Pin, 300-mil SOJ *
  - 32-Pin PLCC

FUNCTIONAL DESCRIPTION

The LH540204 is a FIFO (First-In, First-Out) memory device, based on fully-static CMOS dual-port SRAM technology, capable of storing up to 4096 nine-bit words. It follows the industry-standard architecture and package pinouts for nine-bit asynchronous FIFOs. Each nine-bit LH540204 word may consist of a standard eight-bit byte, together with a parity bit or a block-marking/framing bit.

The input and output ports operate entirely independently of each other, unless the LH540204 becomes either totally full or else totally empty. Data flow at a port is initiated by asserting either of two asynchronous, assertive-LOW control inputs: Write ($\overline{W}$) for data entry at the input port, or Read ($\overline{R}$) for data retrieval at the output port.

Full, Half-Full, and Empty status flags monitor the extent to which the internal memory has been filled. The system may make use of these status outputs to avoid the risk of data loss, which otherwise might occur either by attempting to write additional words into an already-full LH540204, or by attempting to read additional words from an already-empty LH540204. When an LH540204 is operating in a depth-cascaded configuration, the Half-Full Flag is not available.

PIN CONNECTIONS

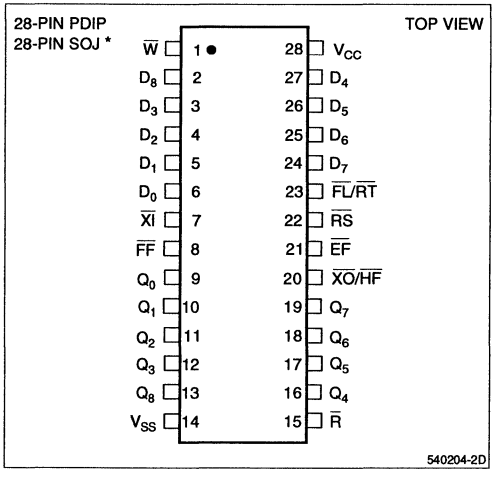


Figure 1. Pin Connections for PDIP * and SOJ * Packages

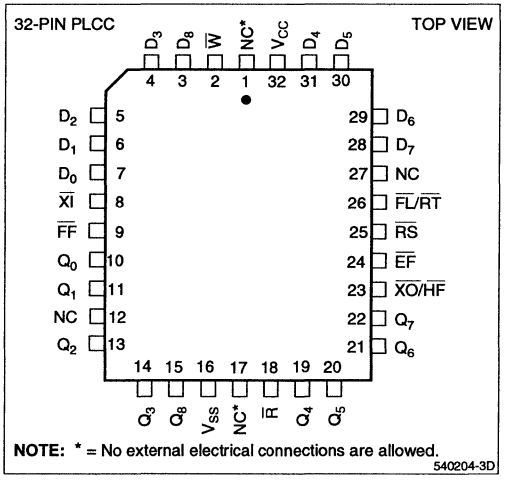


Figure 2. Pin Connections for PLCC Package

* This is an Advance Information data sheet; except that all references to the 600-mil PDIP and SOJ packages still have Product Preview status.

FUNCTIONAL DESCRIPTION (cont'd)

Data words are read out from the LH540204's output port in precisely the same order that they were written in at its input port; that is, according to a First-In, First Out (FIFO) queue discipline. Since the addressing sequence for a FIFO device's memory is internally predefined, no external addressing information is required for the operation of the LH540204 device.

Drop-in-replacement compatibility is maintained with both larger sizes and smaller sizes of industry-standard nine-bit asynchronous FIFOs. The only change is in the number of internally-stored data words implied by the states of the Full Flag and the Half-Full Flag.

The Retransmit ($\overline{RT}$) control signal causes the internal FIFO-memory-array read-address pointer to be set back to zero, to point to the LH540204's first physical memory location, without affecting the internal FIFO-memory-array write-address pointer. Thus, the Retransmit control signal provides a mechanism whereby a block of data, delimited by the zero physical address and the current write-address-pointer value, may be read out *repeatedly* an arbitrary number of times. The only restrictions are that neither the read-address pointer nor the write-address pointer may 'wrap around' during this entire process, i.e., advance past physical location zero after traversing the entire memory. The retransmit facility is not available when an LH540204 is operating in a depth-expanded configuration.

The Reset ($\overline{RS}$) control signal returns the LH540204 to an initial state, empty and ready to be filled. An LH540204 should be reset during every system power-up sequence. A reset operation causes the internal FIFO-memory-array write-address pointer, as well as the read-address pointer, to be set back to zero, to point to the LH540204's first physical memory location. Any information which previously had been stored within the LH540204 is not recoverable after a reset operation.

A cascading (depth-expansion) scheme may be implemented by using the Expansion In ($\overline{XI}$) input signal and the Expansion Out ($\overline{XO}/\overline{HF}$) output signal. This allows a deeper 'effective FIFO' to be implemented by using two or more LH540204 devices, without incurring additional latency ('fallthrough' or 'bubblethrough') delays, and without the necessity of storing and retrieving any given data word more than once. In this cascaded operating mode, one LH540204 device must be designated as the 'first-load' or 'master' device, by grounding its First-Load ($\overline{FL}/\overline{RT}$) control input; the remaining LH540204 devices are designated as 'slaves,' by tying their $\overline{FL}/\overline{RT}$ inputs HIGH. Because of the need to share control signals on pins, the Half-Full Flag and the retransmission capability are not available for either 'master' or 'slave' LH540204 devices operating in cascaded mode.

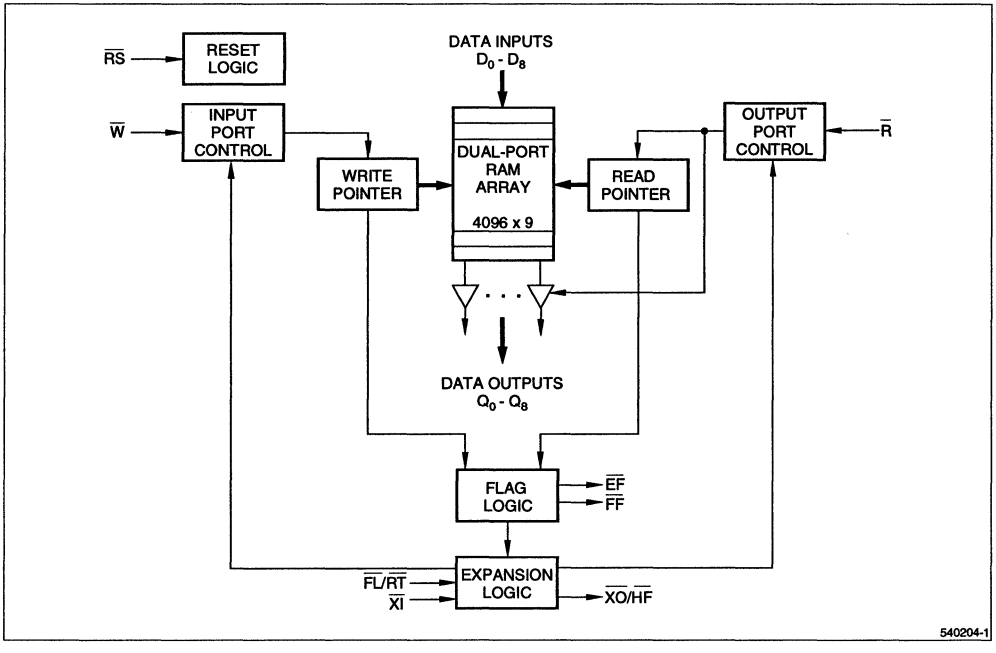


Figure 3. LH540204 Block Diagram

PIN DESCRIPTIONS

PIN	PIN TYPE *	DESCRIPTION
$D_0 - D_8$	I	Input Data Bus
$Q_0 - Q_8$	O/Z	Output Data Bus
$\overline{W}$	I	Write Request
$\overline{R}$	I	Read Request
$\overline{EF}$	O	Empty Flag
$\overline{FF}$	O	Full Flag
$\overline{XO}/\overline{HF}$	O	Expansion Out/Half-Full Flag
$\overline{XI}$	I	Expansion In
$\overline{FL}/\overline{RT}$	I	First Load/Retransmit
$\overline{RS}$	I	Reset
V_{CC}	V	Positive Power Supply
V_{SS}	V	Ground

* I = Input, O = Output, Z = High-Impedance, V = Power Voltage Level

OPERATIONAL DESCRIPTION

Reset

The LH540204 is reset whenever the Reset input ($\overline{RS}$) is taken LOW. A reset operation initializes both the read-address pointer and the write-address pointer to point to location zero, the first physical memory location. During a reset operation, the state of the $\overline{XI}$ and $\overline{FL}/\overline{RT}$ inputs determines whether the device is in standalone mode or in depth-cascaded mode. (See Tables 1 and 2.)

A reset operation is required whenever the LH540204 first is powered up. The Read ($\overline{R}$) and Write ($\overline{W}$) inputs may be in any state when the reset operation is initiated; but they must be HIGH, before the reset operation is terminated by a rising edge of $\overline{RS}$, by a time t_{RRSS} (for Read) or t_{WRSS} (for Write) respectively. (See Figure 10.)

Write

A write cycle is initiated by a falling edge of the Write ($\overline{W}$) control input. Data setup times and hold times must be observed for the data inputs ($D_0 - D_8$). Write operations may occur independently of any ongoing read operations. However, a write operation is possible only if the FIFO is not full, (i.e., if the Full Flag $\overline{FF}$ is HIGH).

At the falling edge of $\overline{W}$ for the first write operation after the memory is half filled, the Half-Full Flag is asserted ($\overline{HF}$ = LOW). It remains asserted until the difference between the write pointer and the read pointer indicates that the data words remaining in the LH540204 are filling the FIFO memory to less than or equal to one-half of its total capacity. The Half-Full Flag is deasserted ($\overline{HF}$ = HIGH) by the appropriate rising edge of $\overline{R}$. (See Table 3.)

The Full Flag is asserted ($\overline{FF}$ = LOW) at the falling edge of $\overline{W}$ for the write operation which fills the last available location in the FIFO memory array. $\overline{FF}$ = LOW inhibits further write operations until $\overline{FF}$ is cleared by a valid read operation. The Full Flag is deasserted ($\overline{FF}$ = HIGH) after the next rising edge of $\overline{R}$ releases another memory location. (See Table 3.)

Read

A read cycle is initiated by a falling edge of the Read ($\overline{R}$) control input. Read data becomes valid at the data outputs ($Q_0 - Q_8$) after a time t_A from the falling edge of $\overline{R}$. After $\overline{R}$ goes HIGH, the data outputs return to a high-impedance state. Read operations may occur independently of any ongoing write operations. However, a read operation is possible only if the FIFO is not empty (i.e., if the Empty Flag $\overline{EF}$ is HIGH).

The LH540204's internal read-address and write-address pointers operate in such a way that consecutive read operations always access data words in the same order that they were written. The Empty Flag is asserted ($\overline{EF}$ = LOW) after that falling edge of $\overline{R}$ which accesses the last available data word in the FIFO memory. $\overline{EF}$ is deasserted ($\overline{EF}$ = HIGH) after the next rising edge of $\overline{W}$ loads another valid data word. (See Table 3.)

Data Flow-Through

Read-data flow-through mode occurs when the Read ($\overline{R}$) control input is brought LOW while the FIFO is empty, and is held LOW in anticipation of a write cycle. At the end of the next write cycle, the Empty Flag $\overline{EF}$ momentarily is deasserted, and the data word just written becomes available at the data outputs ($Q_0 - Q_8$) after a maximum time of $t_{WEF} + t_A$. Additional write operations may occur while the $\overline{R}$ input remains LOW; but only data from the first write operation flows through to the data outputs. Additional data words, if any, may be accessed only by toggling $\overline{R}$.

Write-data flow-through mode occurs when the Write ($\overline{W}$) input is brought LOW while the FIFO is full, and is held LOW in anticipation of a read cycle. At the end of the read cycle, the Full Flag momentarily is deasserted, but then immediately is reasserted in response to $\overline{W}$ being held LOW. A data word is written into the FIFO on the rising edge of $\overline{W}$, which may occur no sooner than $t_{RFF} + t_{WPW}$ after the read operation.

OPERATIONAL DESCRIPTION (cont'd)

Retransmit

The FIFO can be made to reread previously-read data by means of the Retransmit function. A retransmit operation is initiated by pulsing the $\overline{RT}$ input LOW. Both $\overline{R}$ and $\overline{W}$ must be deasserted (HIGH) for the duration of the retransmit pulse. The FIFO's internal read-address pointer is reset to point to location zero, the first physical memory location, while the internal write-address pointer remains unchanged.

After a retransmit operation, those data words in the region in between the read-address pointer and the write-address pointer may be reaccessed by subsequent read operations. A retransmit operation may affect the state of the status flags $\overline{FF}$, $\overline{HF}$, and $\overline{EF}$, depending on the relocation of the read-address pointer. There is no restriction on the number of times that a block of data within an LH540204 may be read out, by repeating the retransmit operation and the subsequent read operations.

The maximum length of a data block which may be retransmitted is 4096 words. Note that if the write-address pointer ever 'wraps around' (i.e., passes location zero more than once) during a sequence of retransmit operations, some data words will be lost.

The Retransmit function is not available when the LH540204 is operating in depth-cascaded mode, because the $\overline{FL}/\overline{RT}$ control pin must be used for first-load selection rather than for retransmission control.

Table 1. Grouping-Mode Determination During a Reset Operation

$\overline{XI}$	$\overline{FL}/\overline{RT}$	MODE	$\overline{XO}/\overline{HF}$ USAGE	$\overline{XI}$ USAGE	$\overline{FL}/\overline{RT}$ USAGE
H [1]	H	Cascaded Slave [2]	$\overline{XO}$	$\overline{XI}$	$\overline{FL}$
H [1]	L	Cascaded Master [2]	$\overline{XO}$	$\overline{XI}$	$\overline{FL}$
L	X	Standalone	$\overline{HF}$	(none)	$\overline{RT}$

NOTES:
1. A reset operation forces $\overline{XO}$ HIGH for the nth FIFO, thus forcing $\overline{XI}$ HIGH for the n+1st FIFO.
2. The terms 'master' and 'slave' refer to operation in depth-cascaded grouping mode.
3. H = HIGH; L = LOW; X = Don't Care.

Table 2. Expansion-Pin Usage According to Grouping Mode

I/O	PIN	STANDALONE	CASCADED MASTER	CASCADED SLAVE
I	$\overline{XI}$	Grounded	From $\overline{XO}$ (n-1st FIFO)	From $\overline{XO}$ (n-1st FIFO)
O	$\overline{XO}/\overline{HF}$	Becomes $\overline{HF}$	To $\overline{XI}$ (n+1st FIFO)	To $\overline{XI}$ (n+1st FIFO)
I	$\overline{FL}/\overline{RT}$	Becomes $\overline{RT}$	Grounded (Logic LOW)	Logic HIGH

Table 3. Status Flags

NUMBER OF UNREAD DATA WORDS PRESENT WITHIN 4096 × 9 FIFO	$\overline{FF}$	$\overline{HF}$	$\overline{EF}$
0	H	H	L
1 to 2048	H	H	H
2049 to 4095	H	L	H
4096	L	L	H

OPERATIONAL MODES

Standalone Configuration

When depth cascading is not required for a given application, the LH540204 is placed in standalone mode by tying the Expansion In input ($\overline{XI}$) to ground. This input is internally sampled during a reset operation. (See Table 1.)

Width Expansion

Word-width expansion is implemented by placing multiple LH540204 devices in parallel. Each LH540204 should be configured for standalone mode. In this arrangement, the behavior of the status flags is identical for all devices; so, in principle, a representative value for each of these flags could be derived from any one device. In practice, it is better to derive 'composite' flag values using external logic, since there may be minor speed variations between different actual devices. (See Figures 4, 5, and 6.)

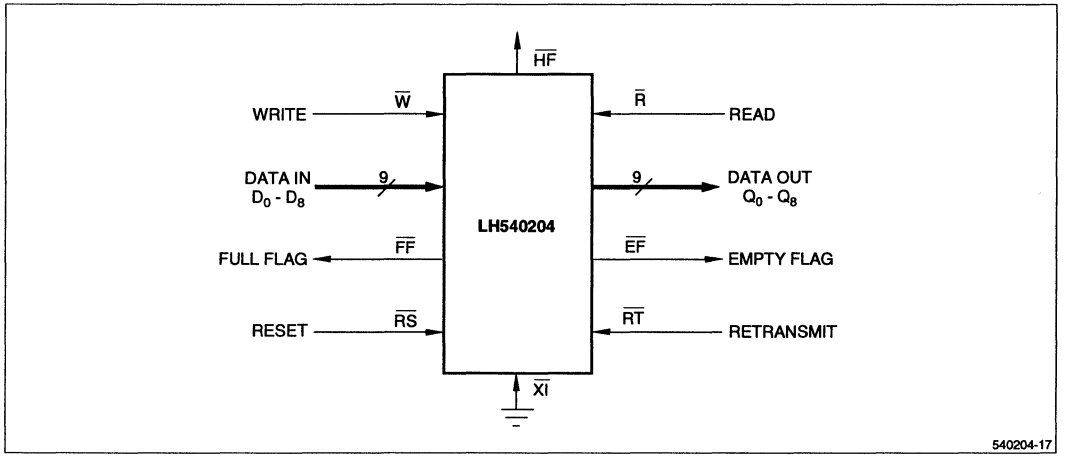


Figure 4. Standalone FIFO (4096 × 9)

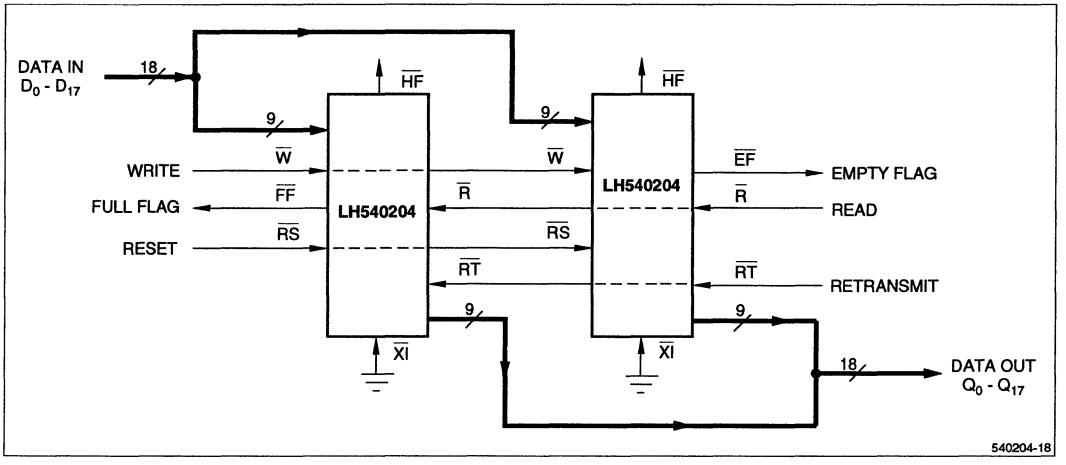


Figure 5. FIFO Word-Width Expansion (4096 × 18)

OPERATIONAL MODES (cont'd)

Depth Cascading

Depth cascading is implemented by configuring the required number of LH540204s in depth-cascaded mode. In this arrangement, the FIFOs are connected in a circular fashion, with the Expansion Out output ($\overline{XO}$) of each device tied to the Expansion In input ($\overline{XI}$) of the next device. One FIFO in the cascade must be designated as the 'first-load' device, by tying its First Load input ($\overline{FL}/\overline{RT}$) to ground. All other devices must have their $\overline{FL}/\overline{RT}$ inputs tied HIGH. In this mode, $\overline{W}$ and $\overline{R}$ signals are shared by all devices, while logic within each LH540204 controls the steering of data. Only one LH540204 is enabled during any given write cycle; thus, the common Data In inputs of all devices are tied together. Likewise, only one LH540204 is enabled during any given read cycle; thus, the common Data Out outputs of all devices are wire-ORed together.

In depth-cascaded mode, external logic should be used to generate a composite Full Flag and a composite Empty Flag, by ANDing the $\overline{FF}$ outputs of all LH540204 devices together and ANDing the $\overline{EF}$ outputs of all devices together. Since $\overline{FF}$ and $\overline{EF}$ are assertive-LOW signals, this 'ANDing' actually is implemented using an assertive-HIGH physical OR gate. The Half-Full Flag and the Retransmit function are not available in depth-cascaded mode.

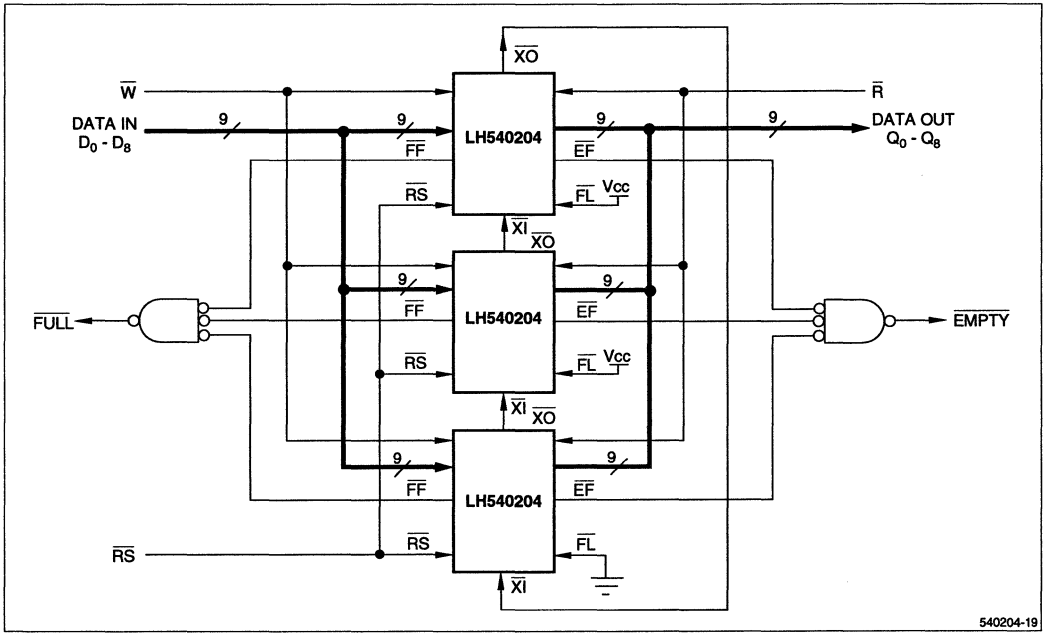


Figure 6. FIFO Depth Cascading (12288 × 9)

OPERATIONAL MODES (cont'd)

Compound FIFO Expansion

A combination of word-width expansion and depth cascading may be implemented easily by operating groups of depth-cascaded FIFOs in parallel.

Bidirectional FIFO Operation

Bidirectional data buffering between two systems may be implemented by operating LH540204 devices in parallel, but in opposite directions. The Data In inputs of each LH540204 are tied to the corresponding Data Out outputs of another LH540204, which is operating in the opposite direction, to form a single bidirectional bus interface. Care must be taken to assure that the appropriate read, write, and flag signals are routed to each system. Both word-width expansion and depth cascading may be used in bidirectional applications.

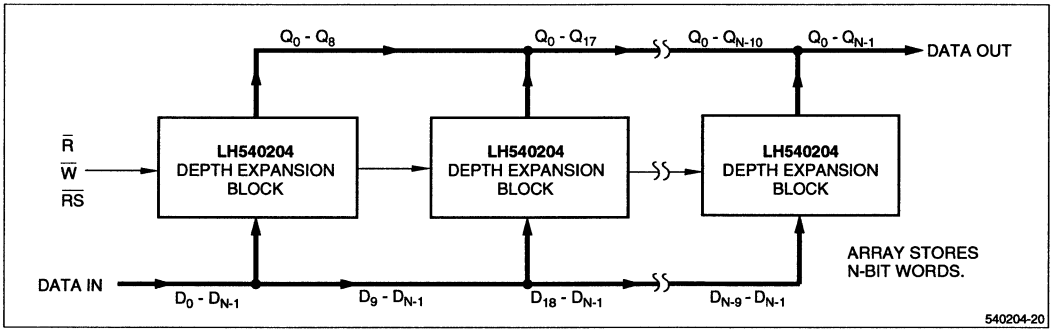


Figure 7. Compound FIFO Expansion

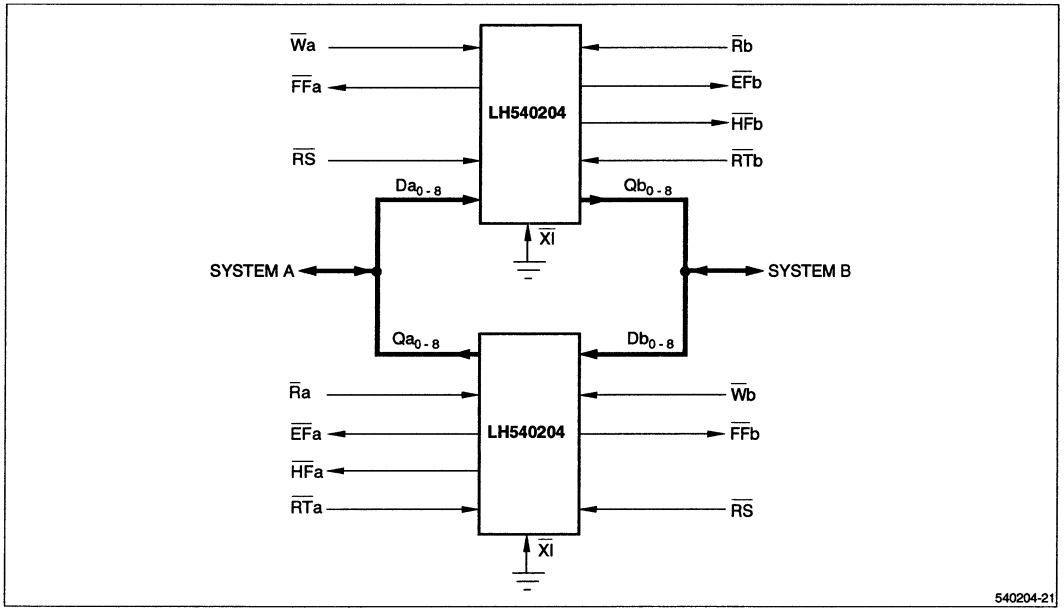


Figure 8. Bidirectional FIFO Operation (4096 × 9 × 2)

ABSOLUTE MAXIMUM RATINGS [1]

PARAMETER	RATING
Supply Voltage to V_{SS} Potential	−0.5 V to 7 V
Signal Pin Voltage to V_{SS} Potential [2]	−0.5 V to V_{CC} + 0.5 V (not to exceed 7 V)
DC Output Current [3]	± 50 mA
Storage Temperature Range	−65°C to 150°C
Power Dissipation (Package Limit)	1.0 W
DC Voltage Applied to Outputs In High-Z State	−0.5 V to V_{CC} + 0.5 V (not to exceed 7 V)

NOTES:

1. Stresses greater than those listed under 'Absolute Maximum Ratings' may cause permanent damage to the device. This is a stress rating for transient conditions only. Functional operation of the device at these or any other conditions outside of those indicated in the 'Operating Range' of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Negative undershoots of 1.5 V in amplitude are permitted for up to 10 ns once per cycle.
3. Outputs should not be shorted for more than 30 seconds. No more than one output should be shorted at any time.

OPERATING RANGE

SYMBOL	PARAMETER	MIN	MAX	UNIT
T_A	Temperature, Ambient	0	70	°C
V_{CC}	Supply Voltage	4.5	5.5	V
V_{SS}	Supply Voltage	0	0	V
V_{IL}	Logic LOW Input Voltage [1]	−0.5	0.8	V
V_{IH}	Logic HIGH Input Voltage	2.0	V_{CC} + 0.5	V

NOTE:

1. Negative undershoots of 1.5 V in amplitude are permitted for up to 10 ns once per cycle.

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
I_{LI}	Input Leakage Current	V_{CC} = 5.5 V, V_{IN} = 0 V to V_{CC}	−10	10	µA
I_{LO}	Output Leakage Current	$\overline{R} \geq V_{IH}$, 0 V ≤ V_{OUT} ≤ V_{CC}	−10	10	µA
V_{OH}	Output HIGH Voltage	I_{OH} = −2.0 mA	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 8.0 mA		0.4	V
I_{CC}	Average Supply Current [1]	Measured at f = 33 MHz		110	mA
I_{CC2}	Average Standby Current [1]	All Inputs = V_{IH}		15	mA
I_{CC3}	Power Down Current [1]	All Inputs = V_{CC} − 0.2V		8	mA

NOTE:

1. I_{CC}, I_{CC2}, and I_{CC3} are dependent upon actual output loading and cycle rates. Specified values are with outputs open.

AC TEST CONDITIONS

PARAMETER	RATING
Input Pulse Levels	Vss to 3 V
Input Rise and Fall Times (10% to 90%)	5 ns
Input Timing Reference Levels	1.5 V
Output Reference Levels	1.5 V
Output Load, Timing Tests	Figure 9

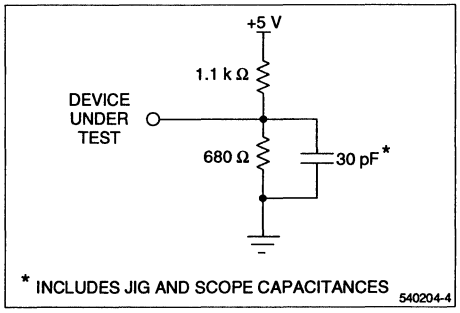


Figure 9. Output Load Circuit

CAPACITANCE [1,2]

PARAMETER	RATING
C_{IN} (Input Capacitance)	5 pF
C_{OUT} (Output Capacitance)	7 pF

NOTES:

1. Sample tested only.
2. Capacitances are maximum values at 25°C, measured at 1.0 MHz, with V_{IN} = 0 V.

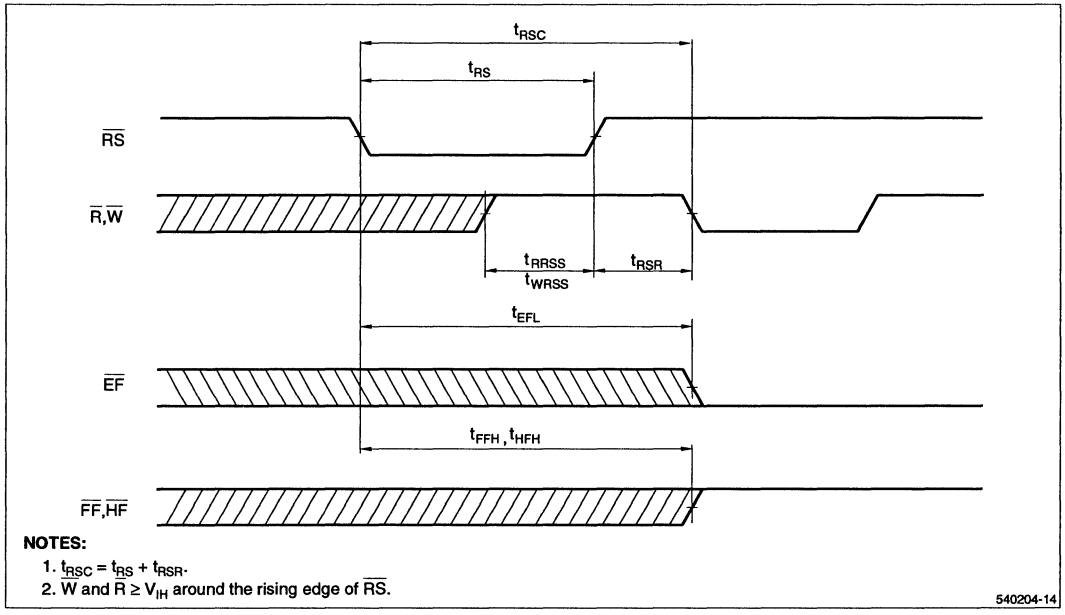
AC ELECTRICAL CHARACTERISTICS [1] (Over Operating Range)

SYMBOL	PARAMETER	t_A = 20 ns		t_A = 25 ns		t_A = 35 ns		t_A = 50 ns		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
READ CYCLE TIMING										
t_{RC}	Read Cycle Time	30	–	35	–	45	–	65	–	ns
t_A	Access Time	–	20	–	25	–	35	–	50	ns
t_{RR}	Read Recovery Time	10	–	10	–	10	–	15	–	ns
t_{RPW}	Read Pulse Width [2]	20	–	25	–	35	–	50	–	ns
t_{RLZ}	Data Bus Active from Read LOW [3]	5	–	5	–	5	–	5	–	ns
t_{WLZ}	Data Bus Active from Write HIGH [3,4]	10	–	10	–	10	–	10	–	ns
t_{DV}	Data Held Valid from Read Pulse HIGH	5	–	5	–	5	–	5	–	ns
t_{RHZ}	Data Bus High-Z from Read HIGH [3]	–	15	–	15	–	15	–	20	ns
WRITE CYCLE TIMING										
t_{WC}	Write Cycle Time	30	–	35	–	45	–	65	–	ns
t_{WPW}	Write Pulse Width [2]	20	–	25	–	35	–	50	–	ns
t_{WR}	Write Recovery Time	10	–	10	–	10	–	15	–	ns
t_{DS}	Data Setup Time	10	–	10	–	15	–	20	–	ns
t_{DH}	Data Hold Time	0	–	0	–	0	–	0	–	ns
RESET TIMING										
t_{RSC}	Reset Cycle Time	30	–	35	–	45	–	65	–	ns
t_{RS}	Reset Pulse Width [2]	20	–	25	–	35	–	50	–	ns
t_{RSR}	Reset Recovery Time	10	–	10	–	10	–	15	–	ns
t_{RRSS}	Read HIGH to $\overline{RS}$ HIGH	20	–	25	–	35	–	50	–	ns
t_{WRSS}	Write HIGH to $\overline{RS}$ HIGH	20	–	25	–	35	–	50	–	ns
RETRANSMIT TIMING [5]										
t_{RTC}	Retransmit Cycle Time	30	–	35	–	45	–	65	–	ns
t_{RT}	Retransmit Pulse Width [2]	20	–	25	–	35	–	50	–	ns
t_{RTR}	Retransmit Recovery Time	10	–	10	–	10	–	15	–	ns
FLAG TIMING										
t_{EFL}	Reset LOW to Empty Flag LOW	–	30	–	35	–	45	–	65	ns
$t_{HFH,FFH}$	Reset LOW to Half-Full and Full Flags HIGH	–	30	–	35	–	45	–	65	ns
t_{REF}	Read LOW to Empty Flag LOW	–	20	–	25	–	35	–	45	ns
t_{RFF}	Read HIGH to Full Flag HIGH	–	20	–	25	–	35	–	45	ns
t_{WEF}	Write HIGH to Empty Flag HIGH	–	20	–	25	–	35	–	45	ns
t_{WFF}	Write LOW to Full Flag LOW	–	20	–	25	–	35	–	45	ns
t_{WHF}	Write LOW to Half-Full Flag LOW	–	20	–	25	–	35	–	45	ns
t_{RHF}	Read HIGH to Half-Full Flag HIGH	–	20	–	25	–	35	–	45	ns
EXPANSION TIMING										
t_{XOL}	Expansion Out LOW	–	20	–	25	–	35	–	50	ns
t_{XOH}	Expansion Out HIGH	–	20	–	25	–	35	–	50	ns
t_{XI}	Expansion In Pulse Width	20	–	25	–	35	–	50	–	ns
t_{XIR}	Expansion In Recovery Time	10	–	10	–	10	–	10	–	ns
t_{XIS}	Expansion in Setup Time	10	–	10	–	15	–	15	–	ns

NOTES:

1. All timing measurements are performed at 'AC Test Condition' levels.
2. Pulse widths less than minimum value are not allowed.
3. Values are guaranteed by design; not currently tested.
4. Only applies to read-data flow-through mode.
5. See also Note 2, Figure 19.

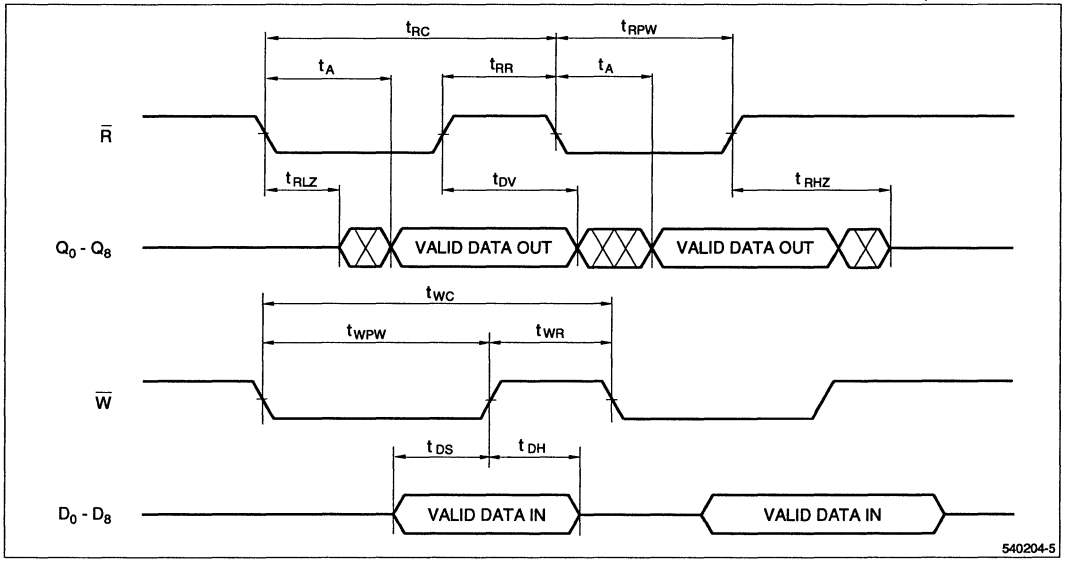
TIMING DIAGRAMS



NOTES:
1. $t_{RSC} = t_{RS} + t_{RSR}$.
2. $\overline{W}$ and $\overline{R} \geq V_{IH}$ around the rising edge of $\overline{RS}$.

540204-14

Figure 10. Reset Timing



540204-5

Figure 11. Asynchronous Write and Read Operation

TIMING DIAGRAMS (cont'd)

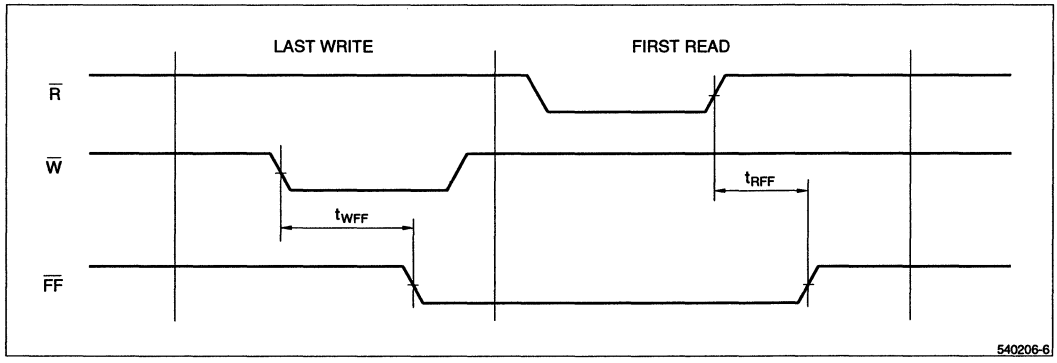


Figure 12. Full Flag From Last Write to First Read

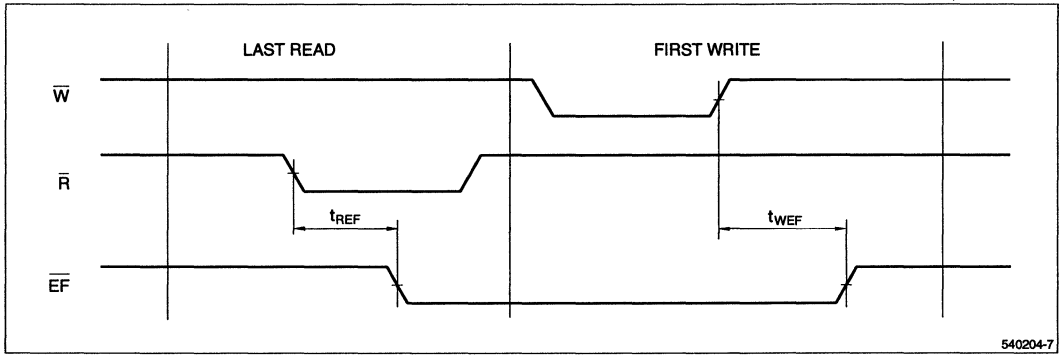
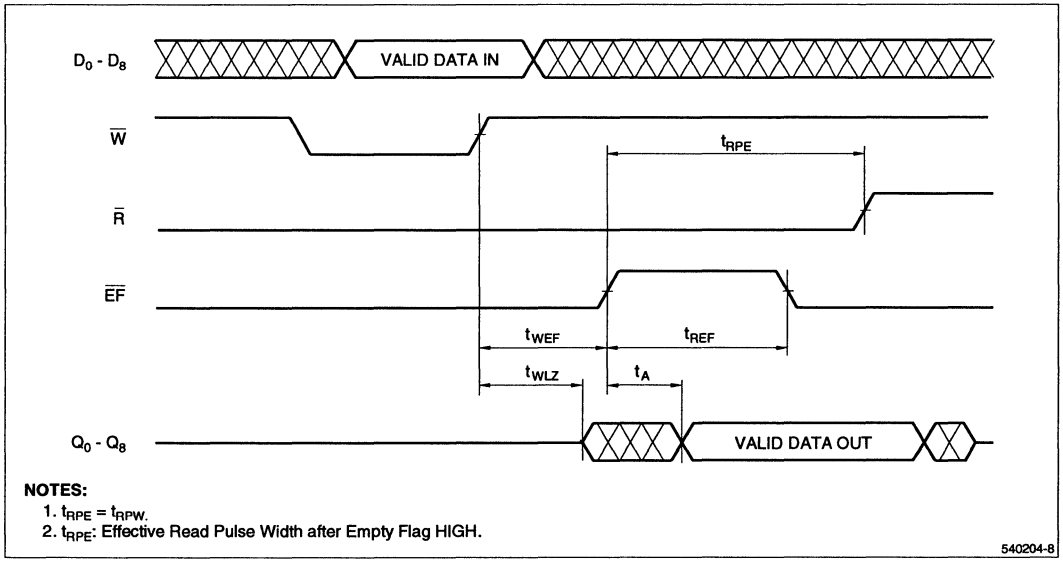


Figure 13. Empty Flag From Last Read to First Write

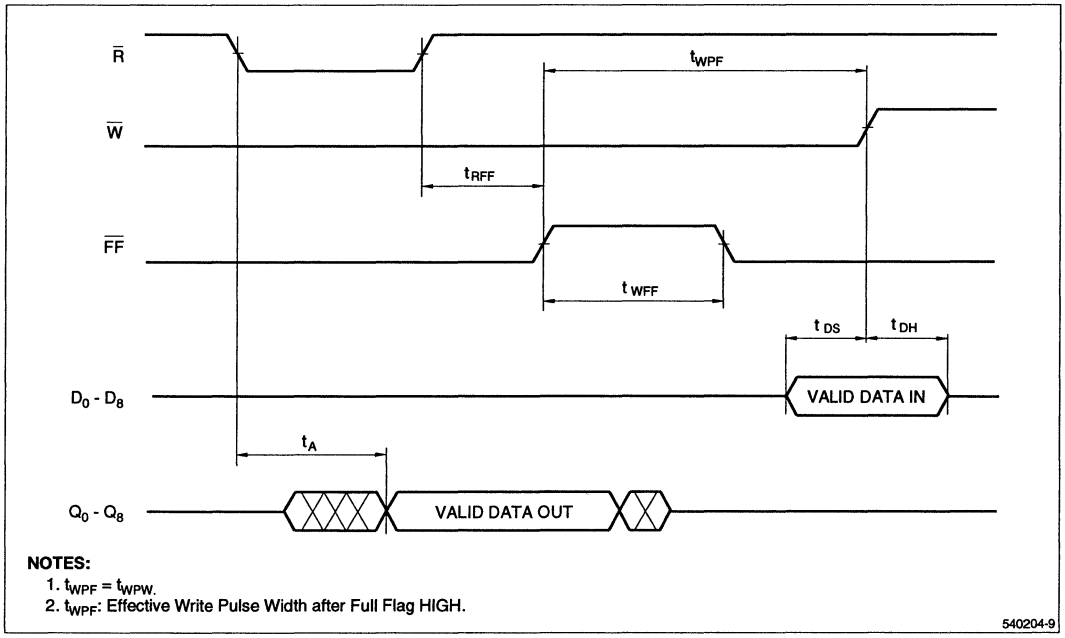
TIMING DIAGRAMS (cont'd)



NOTES:
1. $t_{RPE} = t_{RPW}$.
2. t_{RPE}: Effective Read Pulse Width after Empty Flag HIGH.

540204-8

Figure 14. Read Data Flow-Through

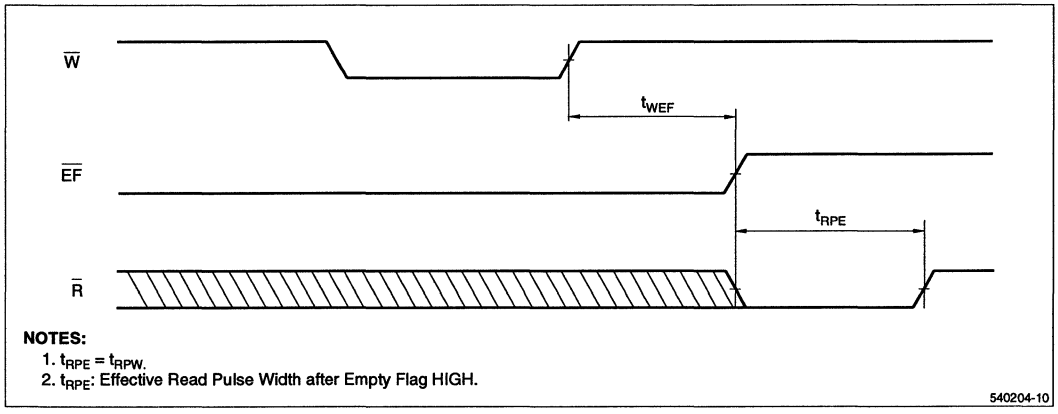


NOTES:
1. $t_{WPF} = t_{WPW}$.
2. t_{WPF}: Effective Write Pulse Width after Full Flag HIGH.

540204-9

Figure 15. Write Data Flow-Through

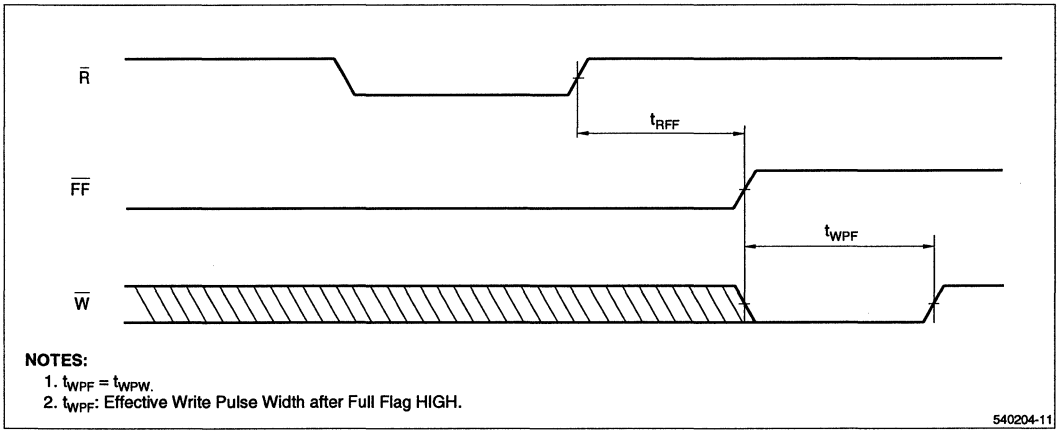
TIMING DIAGRAMS (cont'd)



NOTES:
1. $t_{RPE} = t_{RPW}$.
2. t_{RPE}: Effective Read Pulse Width after Empty Flag HIGH.

540204-10

Figure 16. Empty Flag Timing



NOTES:
1. $t_{WPF} = t_{WPW}$.
2. t_{WPF}: Effective Write Pulse Width after Full Flag HIGH.

540204-11

Figure 17. Full Flag Timing

TIMING DIAGRAMS (cont'd)

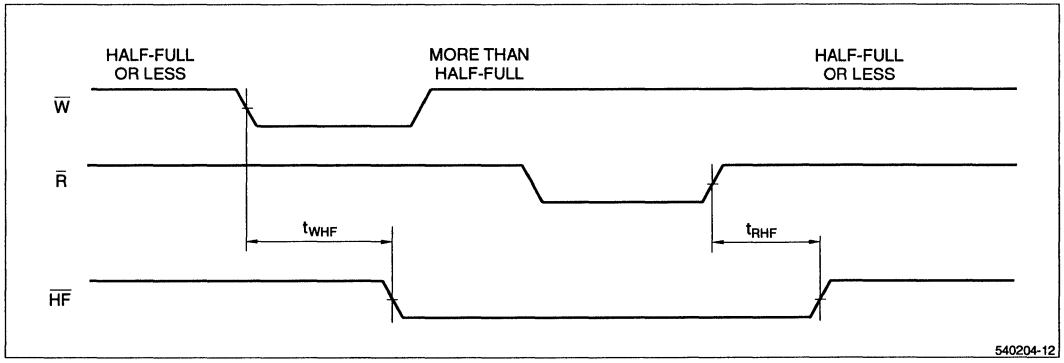


Figure 18. Half-Full Flag Timing

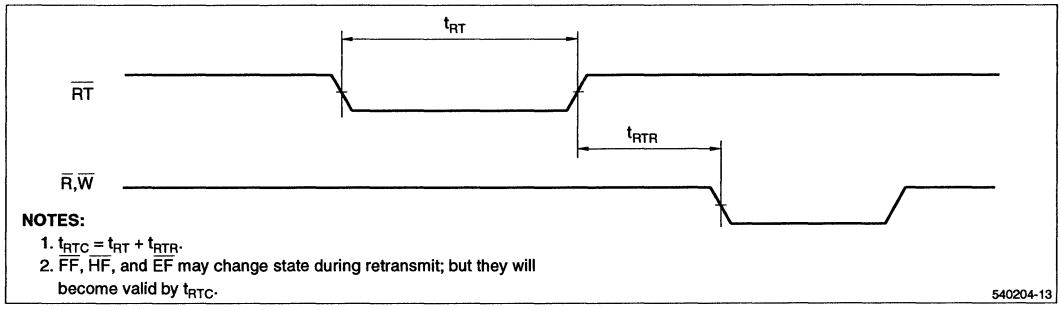


Figure 19. Retransmit Timing

TIMING DIAGRAMS (cont'd)

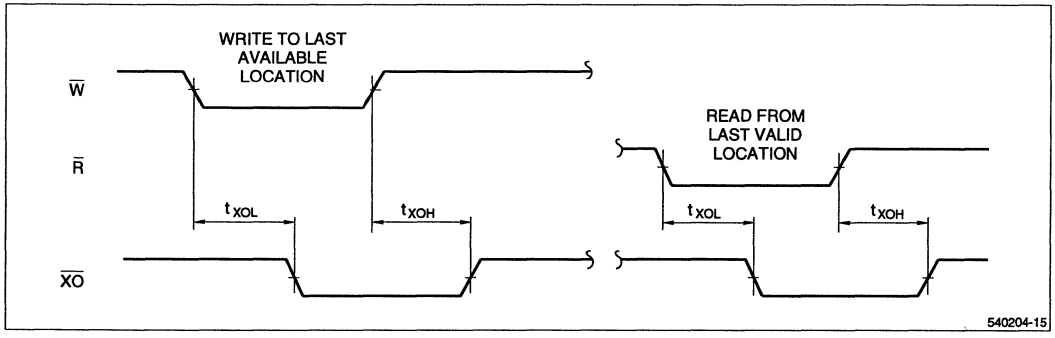


Figure 20. Expansion-Out Timing

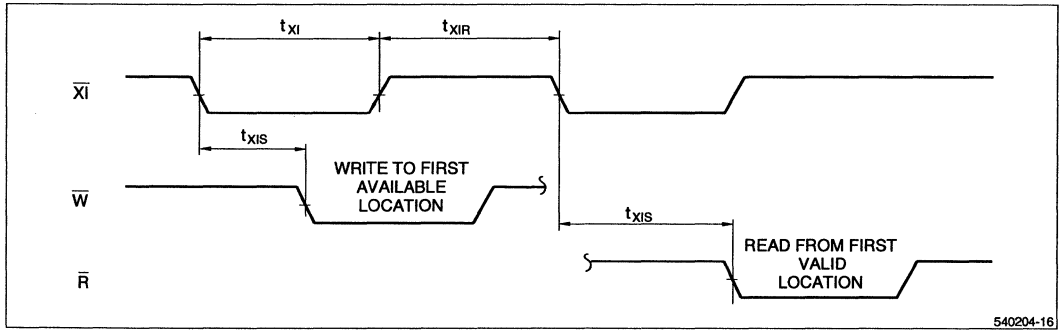
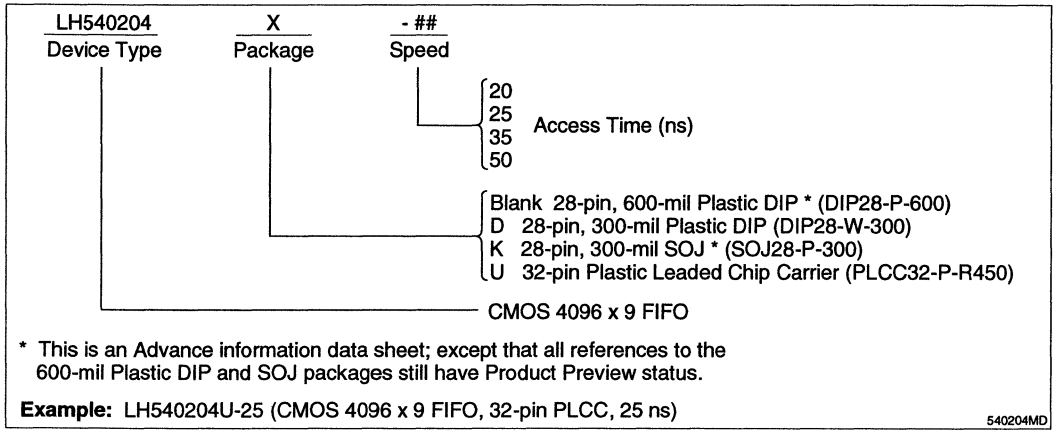


Figure 21. Expansion-In Timing

ORDERING INFORMATION



LH540205

ADVANCE INFORMATION

CMOS 8192 × 9 Asynchronous FIFO

FEATURES

- Fast Access Times: 20/25/35/50 ns
- Fast-Fall-Through Time Architecture Based on CMOS Dual-Port SRAM Technology
- Input Port and Output Port Have Entirely Independent Timing
- Expandable in Width and Depth
- Full, Half-Full, and Empty Status Flags
- Data Retransmission Capability
- TTL-Compatible I/O
- Pin and Functionally Compatible with Am/IDT7205
- Control Signals Assertive-LOW for Noise Immunity
- Packages:
  28-Pin, 300-mil PDIP
  28-Pin, 600-mil PDIP *

FUNCTIONAL DESCRIPTION

The LH540205 is a FIFO (First-In, First-Out) memory device, based on fully-static CMOS dual-port SRAM technology, capable of storing up to 8192 nine-bit words. It follows the industry-standard architecture and package pinouts for nine-bit asynchronous FIFOs. Each nine-bit LH540205 word may consist of a standard eight-bit byte, together with a parity bit or a block-marking/framing bit.

The input and output ports operate entirely independently of each other, unless the LH540205 becomes either totally full or else totally empty. Data flow at a port is initiated by asserting either of two asynchronous, assertive-LOW control inputs: Write ($\overline{W}$) for data entry at the input port, or Read ($\overline{R}$) for data retrieval at the output port.

Full, Half-Full, and Empty status flags monitor the extent to which the internal memory has been filled. The system may make use of these status outputs to avoid the risk of data loss, which otherwise might occur either by attempting to write additional words into an already-full LH540205, or by attempting to read additional words from an already-empty LH540205. When an LH540205 is operating in a depth-cascaded configuration, the Half-Full Flag is not available.

Data words are read out from the LH540205's output port in precisely the same order that they were written in at its input port; that is, according to a First-In, First Out (FIFO) queue discipline. Since the addressing sequence for a FIFO device's memory is internally predefined, no external addressing information is required for the operation of the LH540205 device.

Drop-in-replacement compatibility is maintained with both larger sizes and smaller sizes of industry-standard nine-bit asynchronous FIFOs. The only change is in the number of internally-stored data words implied by the states of the Full Flag and the Half-Full Flag.

The Retransmit ($\overline{RT}$) control signal causes the internal FIFO-memory-array read-address pointer to be set back to zero, to point to the LH540205's first physical memory location, without affecting the internal FIFO-memory-array write-address pointer. Thus, the Retransmit control signal provides a mechanism whereby a block of data, delimited by the zero physical address and the current write-address-pointer value, may be read out *repeatedly* an arbitrary number of times. The only restrictions are that neither the read-address pointer nor the write-address pointer may 'wrap around' during this entire process, i.e., advance past physical location zero after traversing the entire memory. The retransmit facility is not available when an LH540205 is operating in a depth-expanded configuration.

PIN CONNECTIONS

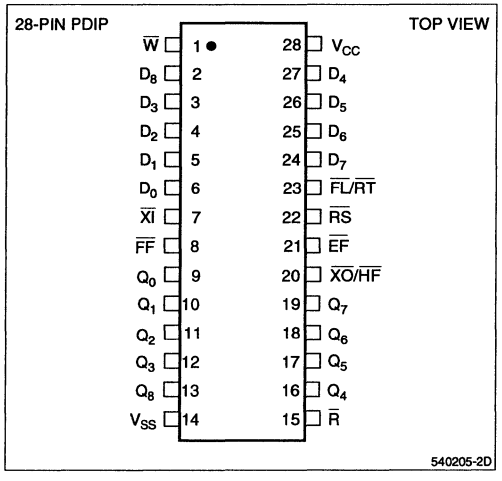


Figure 1. Pin Connections for PDIP Packages

* This is an Advance Information data sheet; except that all references to the 600-mil PDIP still have Product Preview status.

FUNCTIONAL DESCRIPTION (cont'd)

The Reset ($\overline{RS}$) control signal returns the LH540205 to an initial state, empty and ready to be filled. An LH540205 should be reset during every system power-up sequence. A reset operation causes the internal FIFO-memory-array write-address pointer, as well as the read-address pointer, to be set back to zero, to point to the LH540205's first physical memory location. Any information which previously had been stored within the LH540205 is not recoverable after a reset operation.

A cascading (depth-expansion) scheme may be implemented by using the Expansion In ($\overline{XI}$) input signal and the Expansion Out ($\overline{XO}/\overline{HF}$) output signal. This scheme allows a deeper 'effective FIFO' to be implemented by using two or more individual LH540205 devices, without incurring additional latency ('fallthrough' or 'bubblethrough') delays, and without the necessity of storing and retrieving any given data word more than once. In this cascaded operating mode, one LH540205 device must be designated as the 'first-load' or 'master' device, by grounding its First-Load ($\overline{FL}/\overline{RT}$) control input; the remaining LH540205 devices are designated as 'slaves,' by tying their $\overline{FL}/\overline{RT}$ inputs HIGH. Because of the need to share control signals on pins, the Half-Full Flag and the retransmission capability are not available for either 'master' or 'slave' LH540205 devices operating in cascaded mode.

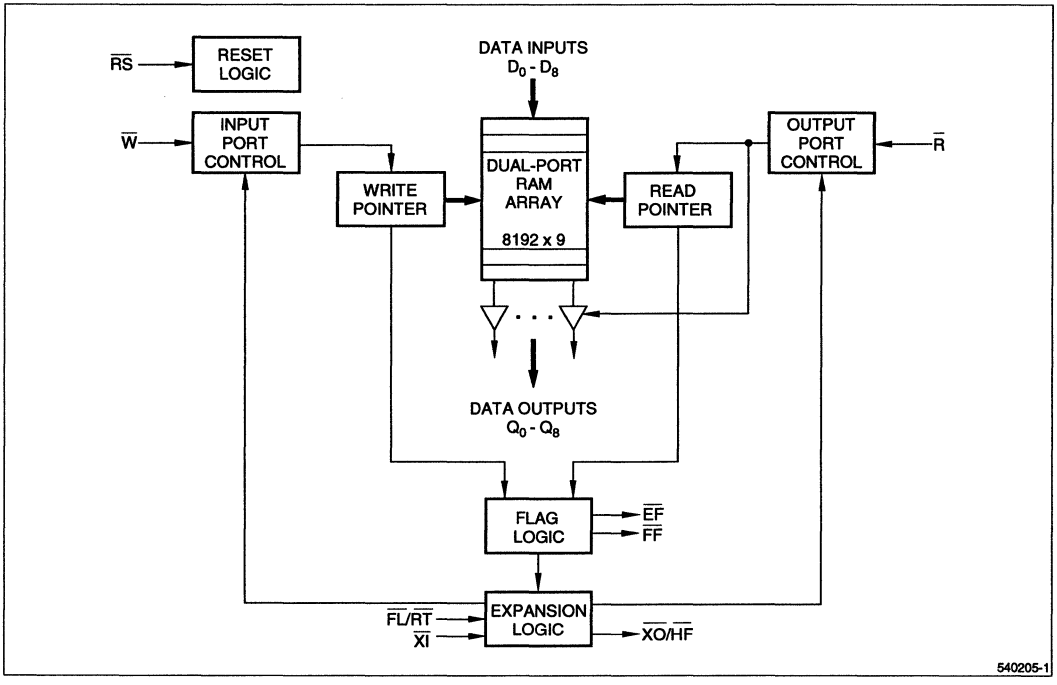


Figure 2. LH540205 Block Diagram

PIN DESCRIPTIONS

PIN	PIN TYPE *	DESCRIPTION
$D_0 - D_8$	I	Input Data Bus
$Q_0 - Q_8$	O/Z	Output Data Bus
$\overline{W}$	I	Write Request
$\overline{R}$	I	Read Request
$\overline{EF}$	O	Empty Flag
$\overline{FF}$	O	Full Flag

PIN	PIN TYPE *	DESCRIPTION
$\overline{XO}/\overline{HF}$	O	Expansion Out/Half-Full Flag
$\overline{XI}$	I	Expansion In
$\overline{FL}/\overline{RT}$	I	First Load/Retransmit
$\overline{RS}$	I	Reset
V_{CC}	V	Positive Power Supply
V_{SS}	V	Ground

* I = Input, O = Output, Z = High-Impedance, V = Power Voltage Level

OPERATIONAL DESCRIPTION

Reset

The LH540205 is reset whenever the Reset input ($\overline{RS}$) is taken LOW. A reset operation initializes both the read-address pointer and the write-address pointer to point to location zero, the first physical memory location. During a reset operation, the state of the $\overline{XI}$ and $\overline{FL}/\overline{RT}$ inputs determines whether the device is in standalone mode or in depth-cascaded mode. (See Tables 1 and 2.)

A reset operation is required whenever the LH540205 first is powered up. The Read ($\overline{R}$) and Write ($\overline{W}$) inputs may be in any state when the reset operation is initiated; but they must be HIGH, before the reset operation is terminated by a rising edge of $\overline{RS}$, by a time t_{RRSS} (for Read) or t_{WRSS} (for Write) respectively. (See Figure 9.)

Write

A write cycle is initiated by a falling edge of the Write ($\overline{W}$) control input. Data setup times and hold times must be observed for the data inputs ($D_0 - D_8$). Write operations may occur independently of any ongoing read operations. However, a write operation is possible only if the FIFO is not full, (i.e., if the Full Flag $\overline{FF}$ is HIGH).

At the falling edge of $\overline{W}$ for the first write operation after the memory is half filled, the Half-Full Flag is asserted ($\overline{HF}$ = LOW). It remains asserted until the difference between the write pointer and the read pointer indicates that the data words remaining in the LH540205 are filling the FIFO memory to less than or equal to one-half of its total capacity. The Half-Full Flag is deasserted ($\overline{HF}$ = HIGH) by the appropriate rising edge of $\overline{R}$. (See Table 3.)

The Full Flag is asserted ($\overline{FF}$ = LOW) at the falling edge of $\overline{W}$ for the write operation which fills the last available location in the FIFO memory array. $\overline{FF}$ = LOW inhibits further write operations until $\overline{FF}$ is cleared by a valid read operation. The Full Flag is deasserted ($\overline{FF}$ = HIGH) after the next rising edge of $\overline{R}$ releases another memory location. (See Table 3.)

Read

A read cycle is initiated by a falling edge of the Read ($\overline{R}$) control input. Read data becomes valid at the data outputs ($Q_0 - Q_8$) after a time t_A from the falling edge of $\overline{R}$. After $\overline{R}$ goes HIGH, the data outputs return to a high-impedance state. Read operations may occur independently of any ongoing write operations. However, a read operation is possible only if the FIFO is not empty (i.e., if the Empty Flag $\overline{EF}$ is HIGH).

The LH540205's internal read-address and write-address pointers operate in such a way that consecutive read operations always access data words in the same order that they were written. The Empty Flag is asserted ($\overline{EF}$ = LOW) after that falling edge of $\overline{R}$ which accesses the last available data word in the FIFO memory. $\overline{EF}$ is deasserted ($\overline{EF}$ = HIGH) after the next rising edge of $\overline{W}$ loads another valid data word. (See Table 3.)

Data Flow-Through

Read-data flow-through mode occurs when the Read ($\overline{R}$) control input is brought LOW while the FIFO is empty, and is held LOW in anticipation of a write cycle. At the end of the next write cycle, the Empty Flag $\overline{EF}$ momentarily is deasserted, and the data word just written becomes available at the data outputs ($Q_0 - Q_8$) after a maximum time of $t_{WEF} + t_A$. Additional write operations may occur while the $\overline{R}$ input remains LOW; but only data from the first write operation flows through to the data outputs. Additional data words, if any, may be accessed only by toggling $\overline{R}$.

Write-data flow-through mode occurs when the Write ($\overline{W}$) input is brought LOW while the FIFO is full, and is held LOW in anticipation of a read cycle. At the end of the read cycle, the Full Flag momentarily is deasserted, but then immediately is reasserted in response to $\overline{W}$ being held LOW. A data word is written into the FIFO on the rising edge of $\overline{W}$, which may occur no sooner than $t_{RFF} + t_{WPW}$ after the read operation.

OPERATIONAL DESCRIPTION (cont'd)

Retransmit

The FIFO can be made to reread previously-read data by means of the Retransmit function. A retransmit operation is initiated by pulsing the $\overline{RT}$ input LOW. Both $\overline{R}$ and $\overline{W}$ must be deasserted (HIGH) for the duration of the retransmit pulse. The FIFO's internal read-address pointer is reset to point to location zero, the first physical memory location, while the internal write-address pointer remains unchanged.

After a retransmit operation, those data words in the region in between the read-address pointer and the write-address pointer may be reaccessed by subsequent read operations. A retransmit operation may affect the state of the status flags $\overline{FF}$, $\overline{HF}$, and $\overline{EF}$, depending on the relocation of the read-address pointer. There is no restriction on the number of times that a block of data within an LH540205 may be read out, by repeating the retransmit operation and the subsequent read operations.

The maximum length of a data block which may be retransmitted is 8192 words. Note that if the write-address pointer ever 'wraps around' (i.e., passes location zero more than once) during a sequence of retransmit operations, some data words will be lost.

The Retransmit function is not available when the LH540205 is operating in depth-cascaded mode, because the $\overline{FL}/\overline{RT}$ control pin must be used for first-load selection rather than for retransmission control.

Table 1. Grouping-Mode Determination During a Reset Operation

$\overline{XI}$	$\overline{FL}/\overline{RT}$	MODE	$\overline{XO}/\overline{HF}$ USAGE	$\overline{XI}$ USAGE	$\overline{FL}/\overline{RT}$ USAGE
H [1]	H	Cascaded Slave [2]	$\overline{XO}$	$\overline{XI}$	$\overline{FL}$
H [1]	L	Cascaded Master [2]	$\overline{XO}$	$\overline{XI}$	$\overline{FL}$
L	X	Standalone	$\overline{HF}$	(none)	$\overline{RT}$

NOTES:
1. A reset operation forces $\overline{XO}$ HIGH for the nth FIFO, thus forcing $\overline{XI}$ HIGH for the n+1st FIFO.
2. The terms 'master' and 'slave' refer to operation in depth-cascaded grouping mode.
3. H = HIGH; L = LOW; X = Don't Care.

Table 2. Expansion-Pin Usage According to Grouping Mode

I/O	PIN	STANDALONE	CASCADED MASTER	CASCADED SLAVE
I	$\overline{XI}$	Grounded	From $\overline{XO}$ (n-1st FIFO)	From $\overline{XO}$ (n-1st FIFO)
O	$\overline{XO}/\overline{HF}$	Becomes $\overline{HF}$	To $\overline{XI}$ (n+1st FIFO)	To $\overline{XI}$ (n+1st FIFO)
I	$\overline{FL}/\overline{RT}$	Becomes $\overline{RT}$	Grounded (Logic LOW)	Logic HIGH

Table 3. Status Flags

NUMBER OF UNREAD DATA WORDS PRESENT WITHIN 8192 × 9 FIFO	$\overline{FF}$	$\overline{HF}$	$\overline{EF}$
0	H	H	L
1 to 4096	H	H	H
4097 to 8191	H	L	H
8192	L	L	H

OPERATIONAL MODES

Standalone Configuration

When depth cascading is not required for a given application, the LH540205 is placed in standalone mode by tying the Expansion In input ($\overline{XI}$) to ground. This input is internally sampled during a reset operation. (See Table 1.)

Width Expansion

Word-width expansion is implemented by placing multiple LH540205 devices in parallel. Each LH540205 should be configured for standalone mode. In this arrangement, the behavior of the status flags is identical for all devices; so, in principle, a representative value for each of these flags could be derived from any one device. In practice, it is better to derive 'composite' flag values using external logic, since there may be minor speed variations between different actual devices. (See Figures 3 and 4.)

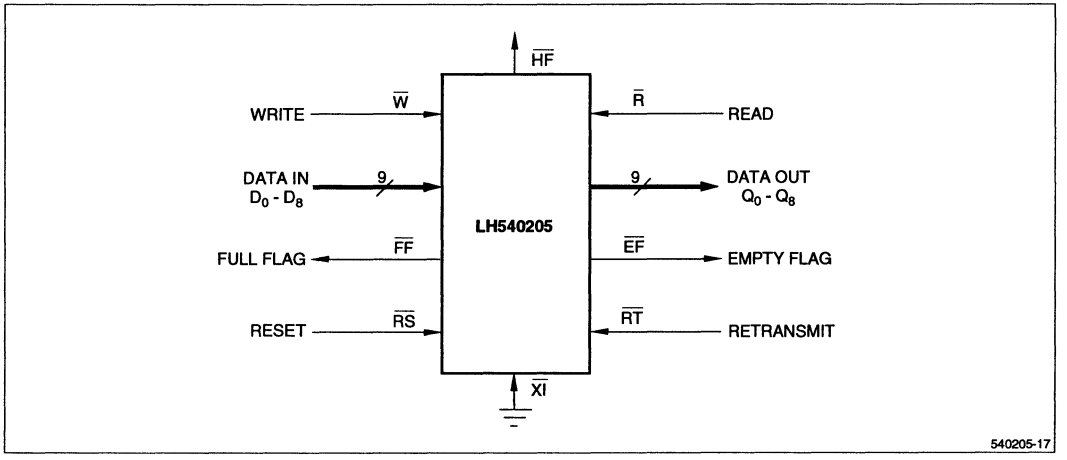


Figure 3. Standalone FIFO (8192 × 9)

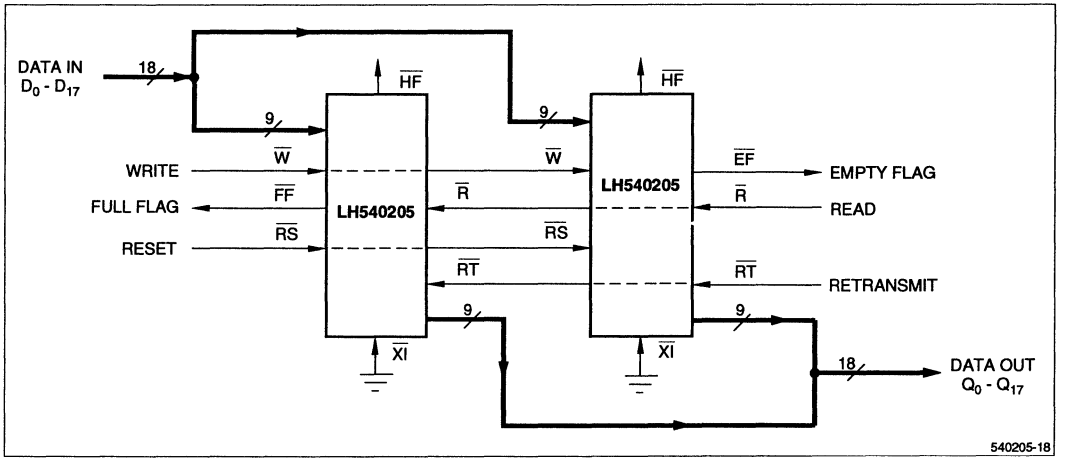


Figure 4. FIFO Word-Width Expansion (8192 × 18)

OPERATIONAL MODES (cont'd)

Depth Cascading

Depth cascading is implemented by configuring the required number of LH540205s in depth-cascaded mode. In this arrangement, the FIFOs are connected in a circular fashion, with the Expansion Out output ($\overline{XO}$) of each device tied to the Expansion In input ($\overline{XI}$) of the next device. One FIFO in the cascade must be designated as the 'first-load' device, by tying its First Load input ($\overline{FL}/\overline{RT}$) to ground. All other devices must have their $\overline{FL}/\overline{RT}$ inputs tied HIGH. In this mode, $\overline{W}$ and $\overline{R}$ signals are shared by all devices, while logic within each LH540205 controls the steering of data. Only one LH540205 is enabled during any given write cycle; thus, the common Data In inputs of all devices are tied together. Likewise, only one LH540205 is enabled during any given read cycle; thus, the common Data Out outputs of all devices are wire-ORed together

In depth-cascaded mode, external logic should be used to generate a composite Full Flag and a composite Empty Flag, by ANDing the $\overline{FF}$ outputs of all LH540205 devices together and ANDing the $\overline{EF}$ outputs of all devices together. Since $\overline{FF}$ and $\overline{EF}$ are assertive-LOW signals, this 'ANDing' actually is implemented using an assertive-HIGH physical OR gate. The Half-Full Flag and the Retransmit function are not available in depth-cascaded mode.

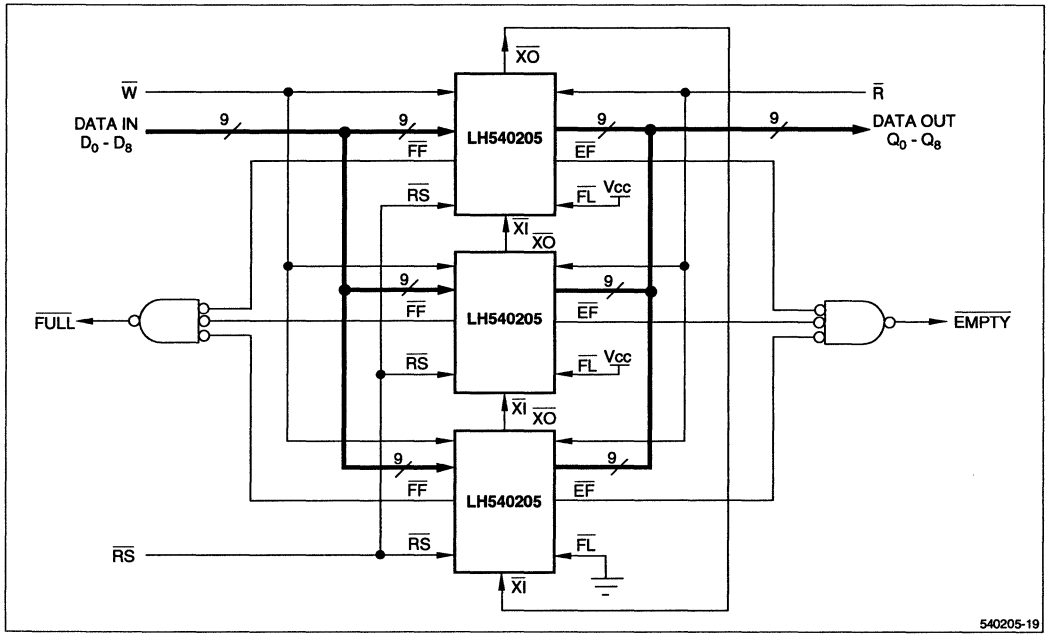


Figure 5. FIFO Depth Cascading (24576 × 9)

OPERATIONAL MODES (cont'd)

Compound FIFO Expansion

A combination of word-width expansion and depth cascading may be implemented easily by operating groups of depth-cascaded FIFOs in parallel.

Bidirectional FIFO Operation

Bidirectional data buffering between two systems may be implemented by operating LH540205 devices in parallel, but in opposite directions. The Data In inputs of each LH540205 are tied to the corresponding Data Out outputs of another LH540205, which is operating in the opposite direction, to form a single bidirectional bus interface. Care must be taken to assure that the appropriate read, write, and flag signals are routed to each system. Both word-width expansion and depth cascading may be used in bidirectional applications.

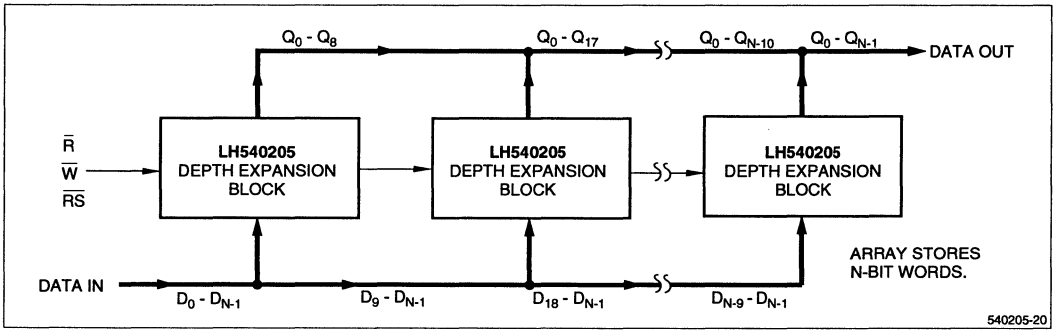


Figure 6. Compound FIFO Expansion

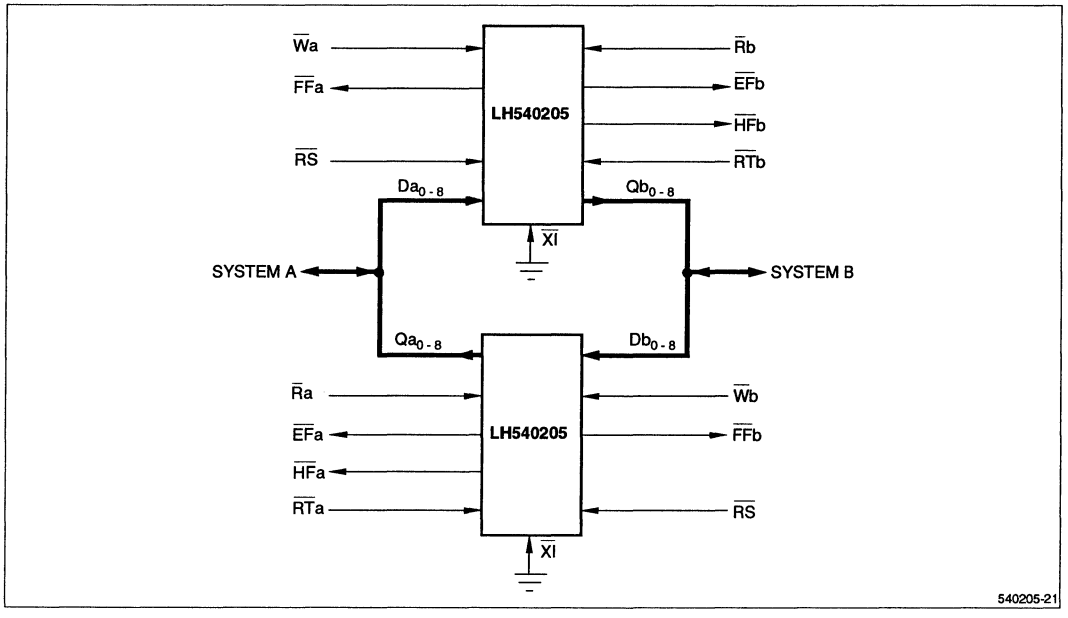


Figure 7. Bidirectional FIFO Operation (8192 × 9 × 2)

ABSOLUTE MAXIMUM RATINGS [1]

PARAMETER	RATING
Supply Voltage to V_{SS} Potential	−0.5 V to 7 V
Signal Pin Voltage to V_{SS} Potential [2]	−0.5 V to V_{CC} + 0.5 V (not to exceed 7 V)
DC Output Current [3]	± 50 mA
Storage Temperature Range	−65°C to 150°C
Power Dissipation (Package Limit)	1.0 W
DC Voltage Applied to Outputs In High-Z State	−0.5 V to V_{CC} + 0.5 V (not to exceed 7 V)

NOTES:

1. Stresses greater than those listed under 'Absolute Maximum Ratings' may cause permanent damage to the device. This is a stress rating for transient conditions only. Functional operation of the device at these or any other conditions outside of those indicated in the 'Operating Range' of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Negative undershoots of 1.5 V in amplitude are permitted for up to 10 ns once per cycle.
3. Outputs should not be shorted for more than 30 seconds. No more than one output should be shorted at any time.

OPERATING RANGE

SYMBOL	PARAMETER	MIN	MAX	UNIT
T_A	Temperature, Ambient	0	70	°C
V_{CC}	Supply Voltage	4.5	5.5	V
V_{SS}	Supply Voltage	0	0	V
V_{IL}	Logic LOW Input Voltage [1]	−0.5	0.8	V
V_{IH}	Logic HIGH Input Voltage	2.0	V_{CC} + 0.5	V

NOTE:

1. Negative undershoots of 1.5 V in amplitude are permitted for up to 10 ns once per cycle.

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
I_{LI}	Input Leakage Current	V_{CC} = 5.5 V, V_{IN} = 0 V to V_{CC}	−10	10	µA
I_{LO}	Output Leakage Current	$\overline{R} \geq V_{IH}$, 0 V ≤ V_{OUT} ≤ V_{CC}	−10	10	µA
V_{OH}	Output HIGH Voltage	I_{OH} = −2.0 mA	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 8.0 mA		0.4	V
I_{CC}	Average Supply Current [1]	Measured at f = 33 MHz		110	mA
I_{CC2}	Average Standby Current [1]	All Inputs = V_{IH}		15	mA
I_{CC3}	Power Down Current [1]	All Inputs = V_{CC} − 0.2V		8	mA

NOTE:

1. I_{CC}, I_{CC2}, and I_{CC3} are dependent upon actual output loading and cycle rates. Specified values are with outputs open.

AC TEST CONDITIONS

PARAMETER	RATING
Input Pulse Levels	V_{SS} to 3 V
Input Rise and Fall Times (10% to 90%)	5 ns
Input Timing Reference Levels	1.5 V
Output Reference Levels	1.5 V
Output Load, Timing Tests	Figure 8

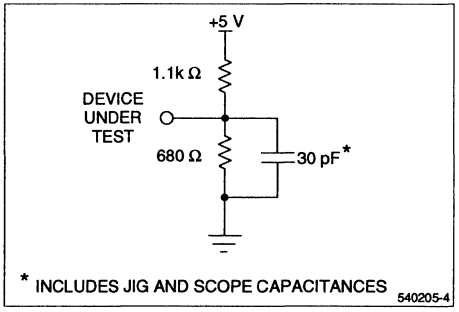


Figure 8. Output Load Circuit

CAPACITANCE [1,2]

PARAMETER	RATING
C_{IN} (Input Capacitance)	5 pF
C_{OUT} (Output Capacitance)	7 pF

NOTES:

1. Sample tested only.
2. Capacitances are maximum values at 25°C, measured at 1.0 MHz, with V_{IN} = 0 V.

AC ELECTRICAL CHARACTERISTICS [1] (Over Operating Range)

SYMBOL	PARAMETER	t_A = 20 ns		t_A = 25 ns		t_A = 35 ns		t_A = 50 ns		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
READ CYCLE TIMING										
t_{RC}	Read Cycle Time	30	–	35	–	45	–	65	–	ns
t_A	Access Time	–	20	–	25	–	35	–	50	ns
t_{RR}	Read Recovery Time	10	–	10	–	10	–	15	–	ns
t_{RPW}	Read Pulse Width [2]	20	–	25	–	35	–	50	–	ns
t_{RLZ}	Data Bus Active from Read LOW [3]	5	–	5	–	5	–	5	–	ns
t_{WLZ}	Data Bus Active from Write HIGH [3,4]	10	–	10	–	10	–	10	–	ns
t_{DV}	Data Held Valid from Read Pulse HIGH	5	–	5	–	5	–	5	–	ns
t_{RHZ}	Data Bus High-Z from Read HIGH [3]	–	15	–	15	–	15	–	20	ns
WRITE CYCLE TIMING										
t_{WC}	Write Cycle Time	30	–	35	–	45	–	65	–	ns
t_{WPW}	Write Pulse Width [2]	20	–	25	–	35	–	50	–	ns
t_{WR}	Write Recovery Time	10	–	10	–	10	–	15	–	ns
t_{DS}	Data Setup Time	10	–	10	–	15	–	20	–	ns
t_{DH}	Data Hold Time	0	–	0	–	0	–	0	–	ns
RESET TIMING										
t_{RSC}	Reset Cycle Time	30	–	35	–	45	–	65	–	ns
t_{RS}	Reset Pulse Width [2]	20	–	25	–	35	–	50	–	ns
t_{RSR}	Reset Recovery Time	10	–	10	–	10	–	15	–	ns
t_{RRSS}	Read HIGH to $\overline{RS}$ HIGH	20	–	25	–	35	–	50	–	ns
t_{WRSS}	Write HIGH to $\overline{RS}$ HIGH	20	–	25	–	35	–	50	–	ns
RETRANSMIT TIMING [5]										
t_{RTC}	Retransmit Cycle Time	30	–	35	–	45	–	65	–	ns
t_{RT}	Retransmit Pulse Width [2]	20	–	25	–	35	–	50	–	ns
t_{RTR}	Retransmit Recovery Time	10	–	10	–	10	–	15	–	ns
FLAG TIMING										
t_{EFL}	Reset LOW to Empty Flag LOW	–	30	–	35	–	45	–	65	ns
$t_{HFH,FFH}$	Reset LOW to Half-Full and Full Flags HIGH	–	30	–	35	–	45	–	65	ns
t_{REF}	Read LOW to Empty Flag LOW	–	20	–	25	–	35	–	45	ns
t_{RFF}	Read HIGH to Full Flag HIGH	–	20	–	25	–	35	–	45	ns
t_{WEF}	Write HIGH to Empty Flag HIGH	–	20	–	25	–	35	–	45	ns
t_{WFF}	Write LOW to Full Flag LOW	–	20	–	25	–	35	–	45	ns
t_{WHF}	Write LOW to Half-Full Flag LOW	–	20	–	25	–	35	–	45	ns
t_{RHF}	Read HIGH to Half-Full Flag HIGH	–	20	–	25	–	35	–	45	ns
EXPANSION TIMING										
t_{XOL}	Expansion Out LOW	–	20	–	25	–	35	–	50	ns
t_{XOH}	Expansion Out HIGH	–	20	–	25	–	35	–	50	ns
t_{XI}	Expansion In Pulse Width	20	–	25	–	35	–	50	–	ns
t_{XIR}	Expansion In Recovery Time	10	–	10	–	10	–	10	–	ns
t_{XIS}	Expansion in Setup Time	10	–	10	–	15	–	15	–	ns

NOTES:

1. All timing measurements are performed at 'AC Test Condition' levels.
2. Pulse widths less than minimum value are not allowed.
3. Values are guaranteed by design; not currently tested.
4. Only applies to read-data flow-through mode.
5. See also Note 2, Figure 18.

TIMING DIAGRAMS

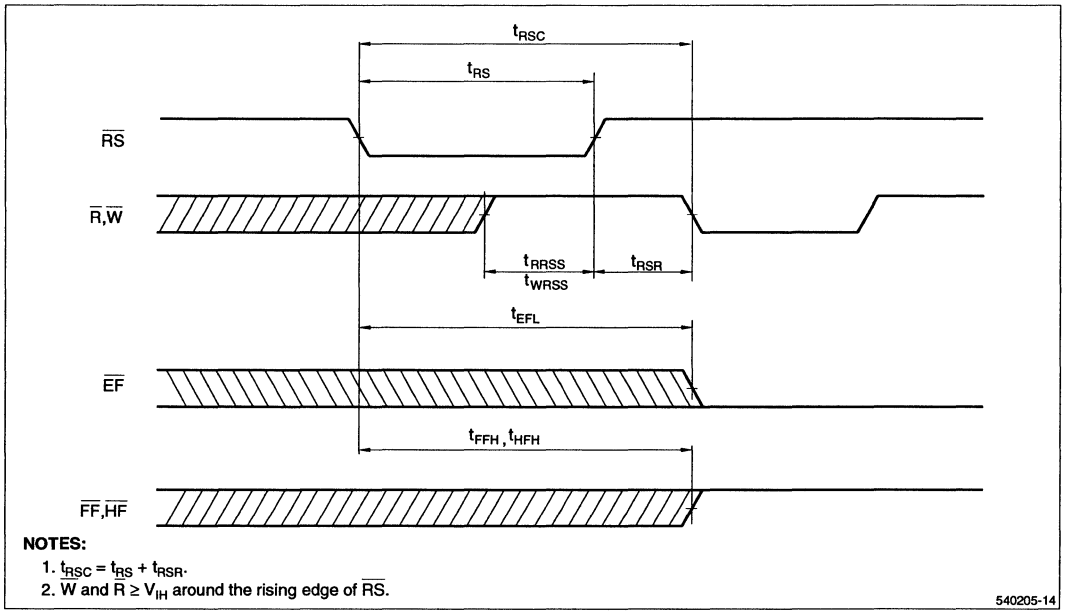


Figure 9. Reset Timing

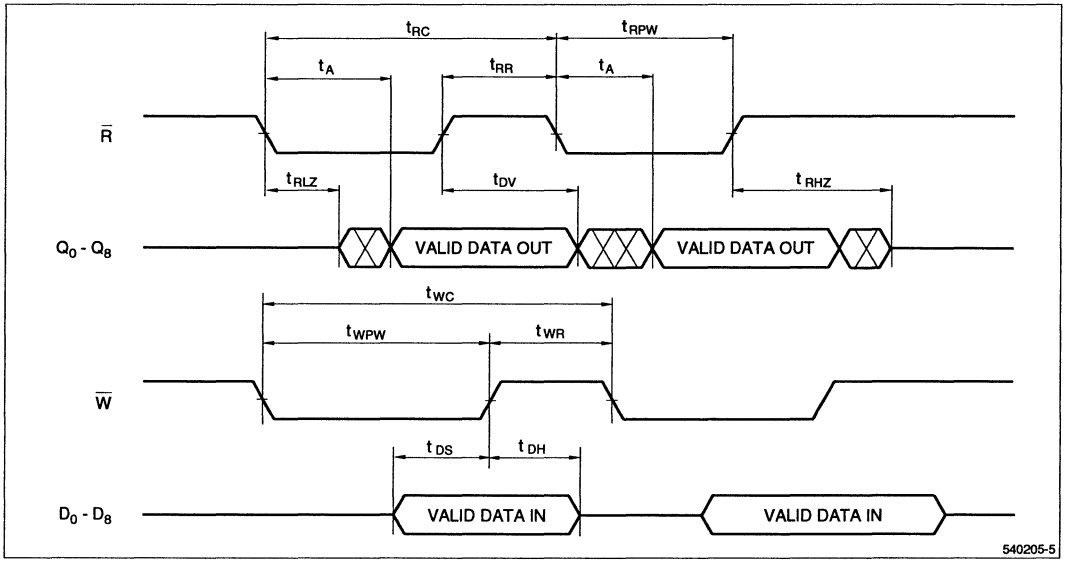


Figure 10. Asynchronous Write and Read Operation

TIMING DIAGRAMS (cont'd)

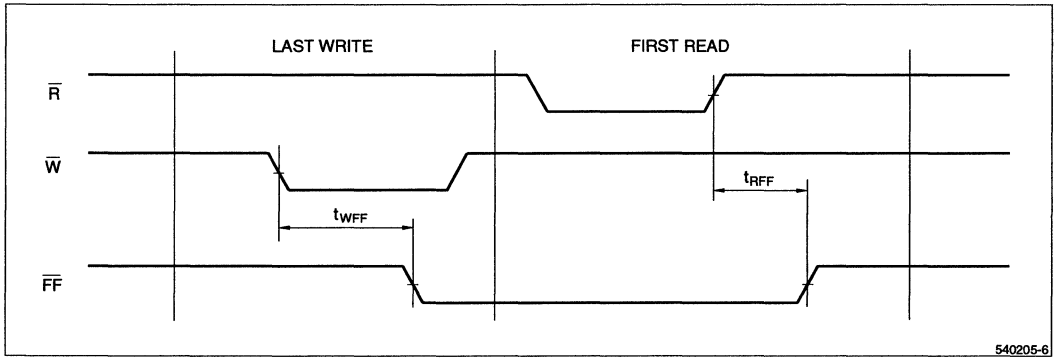


Figure 11. Full Flag From Last Write to First Read

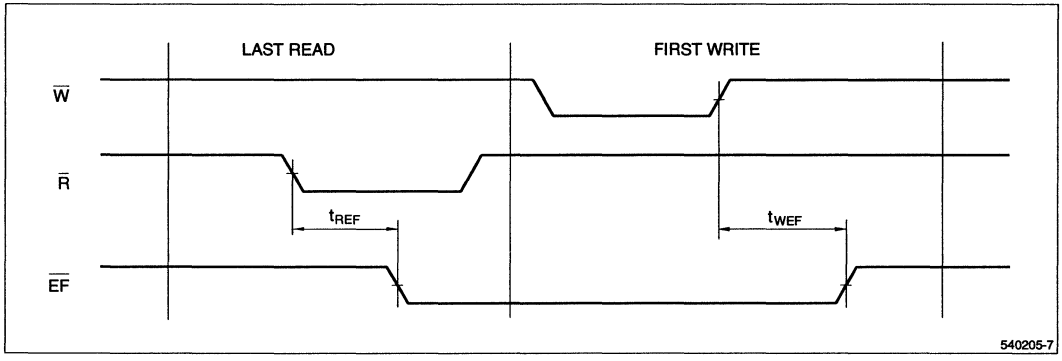
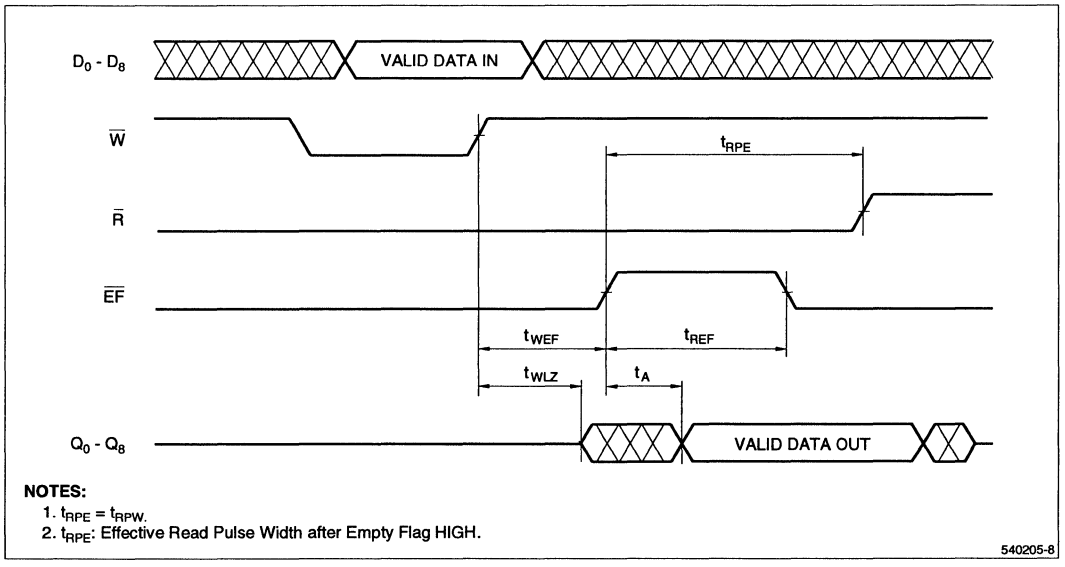


Figure 12. Empty Flag From Last Read to First Write

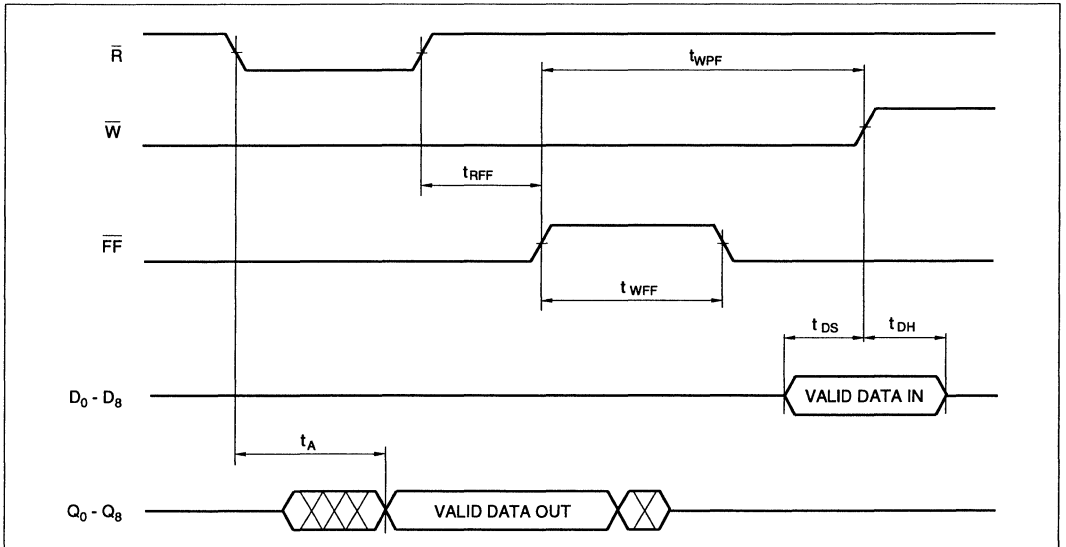
TIMING DIAGRAMS (cont'd)



NOTES:
1. $t_{RPE} = t_{RPW}$.
2. t_{RPE}: Effective Read Pulse Width after Empty Flag HIGH.

540205-8

Figure 13. Read Data Flow-Through

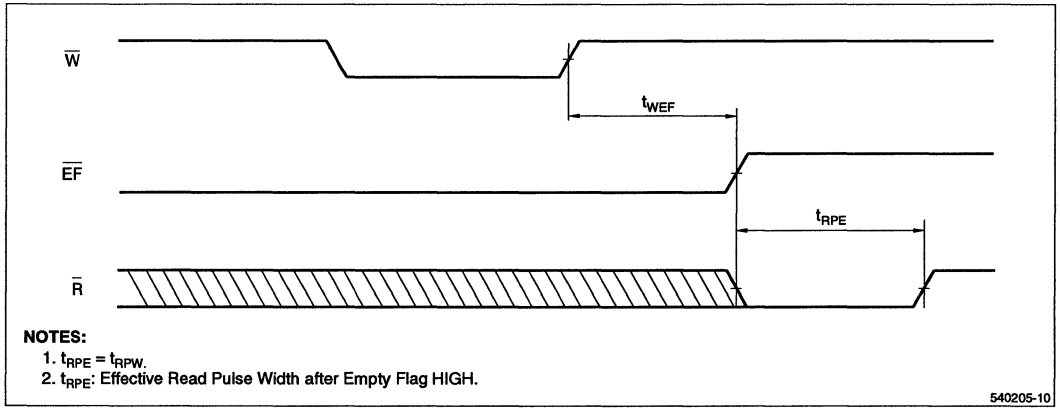


NOTES:
1. $t_{WPF} = t_{WPW}$.
2. t_{WPF}: Effective Write Pulse Width after Full Flag HIGH.

540205-9

Figure 14. Write Data Flow-Through

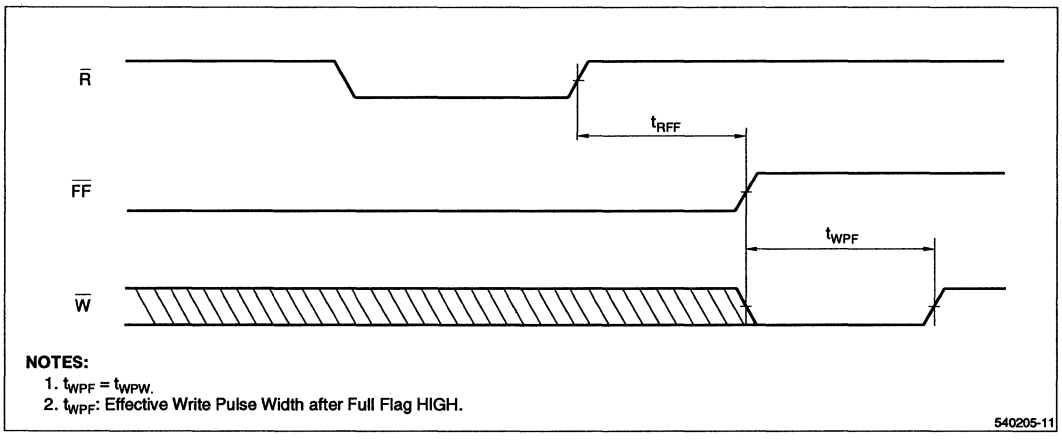
TIMING DIAGRAMS (cont'd)



NOTES:
1. $t_{RPE} = t_{RPW}$.
2. t_{RPE}: Effective Read Pulse Width after Empty Flag HIGH.

540205-10

Figure 15. Empty Flag Timing



NOTES:
1. $t_{WPF} = t_{WPW}$.
2. t_{WPF}: Effective Write Pulse Width after Full Flag HIGH.

540205-11

Figure 16. Full Flag Timing

TIMING DIAGRAMS (cont'd)

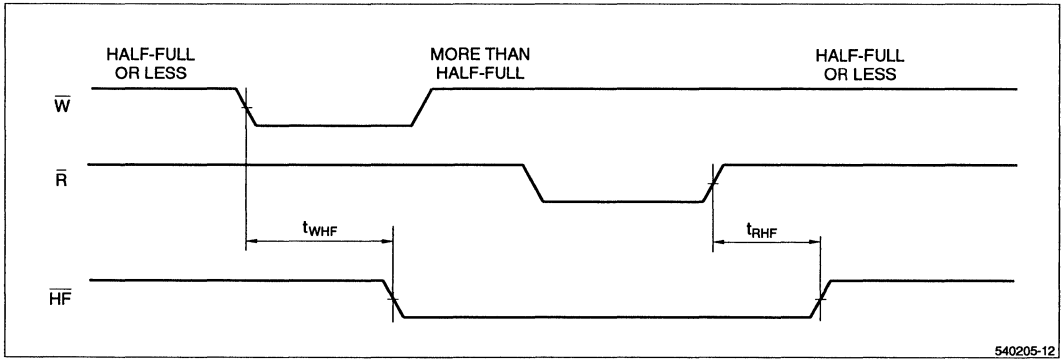


Figure 17. Half-Full Flag Timing

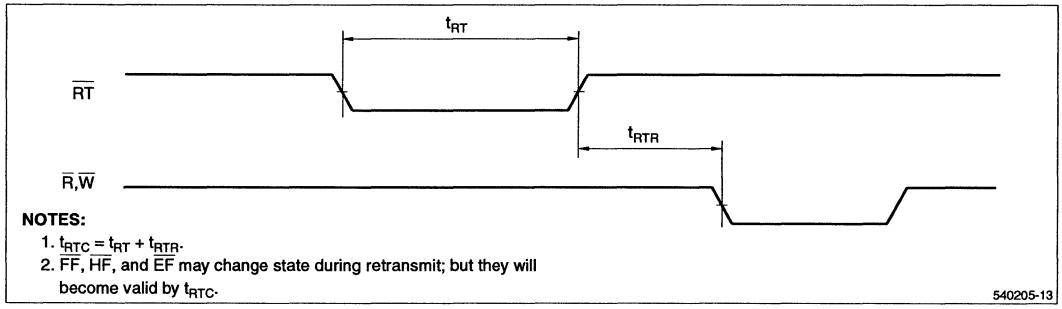


Figure 18. Retransmit Timing

TIMING DIAGRAMS (cont'd)

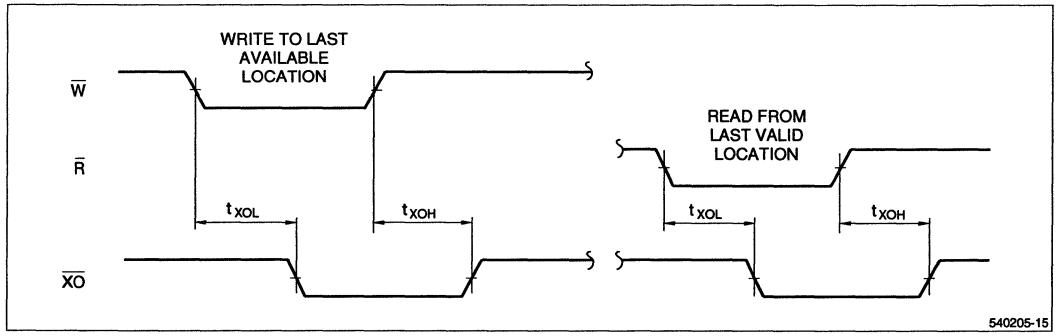


Figure 19. Expansion-Out Timing

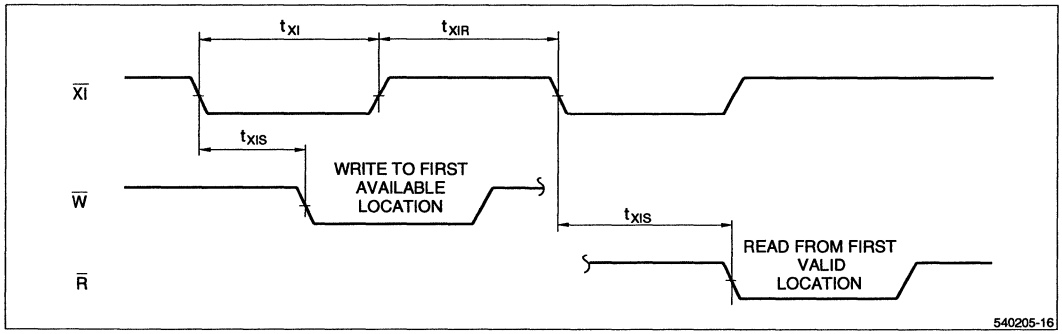
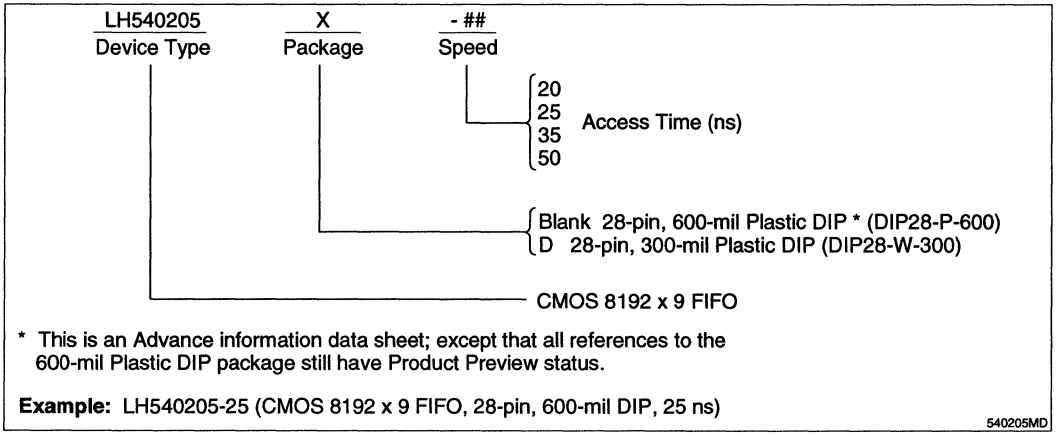


Figure 20. Expansion-In Timing

ORDERING INFORMATION



LH540215/25

PRELIMINARY

512 × 18 / 1024 × 18 Synchronous FIFO

FEATURES

- Fast Cycle Times: 20/25/35 ns
- Pin-Compatible Drop-In Replacements for IDT72215B/25B FIFOs
- Choice of IDT-Compatible or Enhanced Operating Mode; Selected by an Input Control Signal
- Device Comes Up into One of Two Known Default States at Reset Depending on the State of the EMODE Control Input: Programming is Allowed, but is not Required
- Internal Memory Array Architecture Based on CMOS Dual-Port SRAM Technology, 512 × 18 or 1024 × 18
- 'Synchronous' Enable-Plus-Clock Control at Both Input Port and Output Port
- Independently-Synchronized Operation of Input Port and Output Port
- Control Inputs Sampled on Rising Clock Edge
- Most Control Signals Assertive-LOW for Noise Immunity
- May be Cascaded for Increased Depth, or Paralleled for Increased Width
- 16-mA-I_{OL} Three-State Outputs
- Five Status Flags: Full, Almost-Full, Half-Full, Almost-Empty, and Empty; 'Almost' Flags are Programmable
- ***In Enhanced Operating Mode, Almost-Full, Half-Full, and Almost-Empty Flags can be Made Completely Synchronous***
- ***In Enhanced Operating Mode, Duplicate Enables for Interlocked Paralleled FIFO Operation, for 36-Bit Data Width, when Selected and Appropriately Connected***
- ***In Enhanced Operating Mode, Disabling Three-State Outputs May be Made to Suppress Reading***
- ***Data Retransmit Function***
- TTL/CMOS-Compatible I/O
- Space-Saving 68-Pin PLCC Package

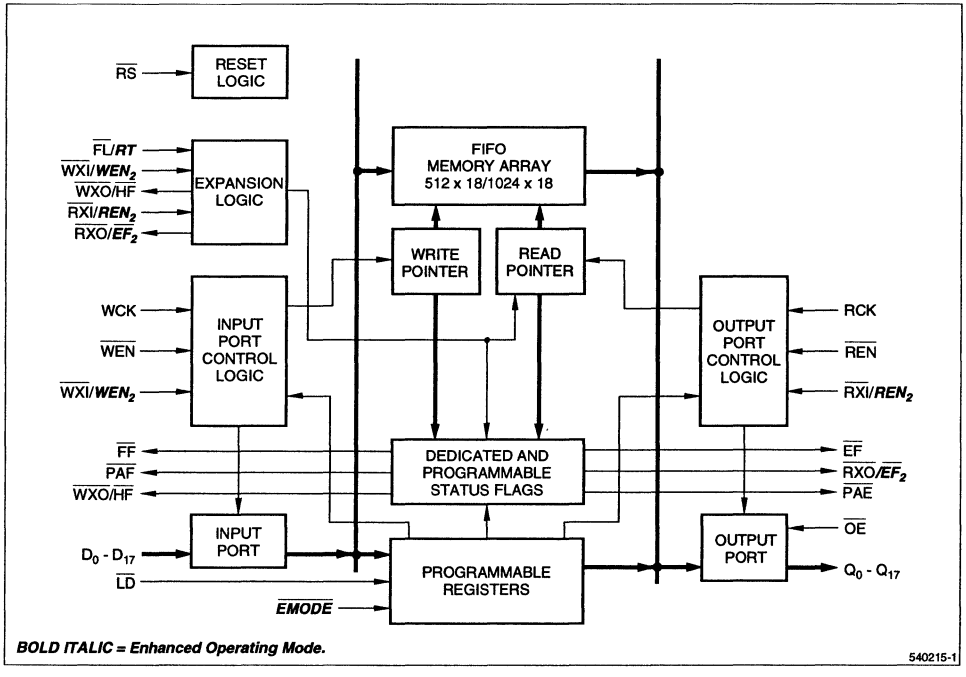


Figure 1. LH540215/25 Block Diagram

BOLD ITALIC = Enhanced Operating Mode

FUNCTIONAL DESCRIPTION

NOTE: Throughout this data sheet, a ***BOLD ITALIC*** type font is used for all references to ***Enhanced Operating Mode*** features which do not function in IDT-Compatible Operating Mode; and also for all references to the ***retransmit*** facility (which is not an IDT72215B/25B FIFO feature), even though it may be used – subject to some restrictions – in either of these two operating modes. Thus, readers interested only in using the LH540215/25 FIFOs in IDT-Compatible Operating Mode may skip over ***BOLD ITALIC*** sections, if they wish.

The LH540215/25 are FIFO (First-In, First-Out) memory devices, based on fully-static CMOS dual-port SRAM technology, capable of containing up to 512 or 1024 18-bit words respectively. They can replace two or more byte-wide FIFOs in many applications, for microprocessor-to-microprocessor or microprocessor-to-bus communication. Their architecture supports synchronous operation, tied to two independent free-running clocks at the input and output ports respectively. However, these 'clocks' also may be aperiodic, asynchronous 'demand' signals. Almost all control-input signals and status-output signals are synchronized to these clocks, to simplify system design.

The input and output ports operate altogether independently of each other, unless the FIFO becomes either totally full or else totally empty. Data flow is initiated at a port by the rising edge of its corresponding clock, and is gated by the appropriate edge-sampled enable signals.

The following FIFO status flags monitor the extent to which the internal memory has been filled: Full, Almost-Full, Half-Full, Almost-Empty, and Empty. The Almost-Full and Almost-Empty flag offsets are programmable over the entire FIFO depth; but, during a reset operation, each of these is initialized to a default offset value of 63 (LH540215) or 127 (LH540225) FIFO-memory words, from the respective FIFO boundary. If this default offset value is satisfactory, no further programming is required.

After a reset operation during which the ***$\overline{EMODE}$*** control input was not asserted (was HIGH), these FIFOs operate in the IDT-Compatible Operating Mode. In this mode, each part is pin-compatible and functionally-compatible with the IDT72215B/25B part of similar depth and speed grade; and the ***Control Register*** is not even accessible or visible to the external-system logic which is controlling the FIFO, although it still performs the same control functions.

However, assertion of the $\overline{EMODE}$ control input during a reset operation leaves Control Register bits 00-05 set, and causes the FIFO to operate in the Enhanced Operating Mode. In essense, asserting $\overline{EMODE}$ chooses a different default state for the Control Register. The system optionally then may program the Control Register in any desired manner to activate or deactivate any or all of the Enhanced-Operating-Mode features which it can control, including selectable-clock-edge flag synchronization, and read inhibition when the data outputs are disabled.

BOLD ITALIC = Enhanced Operating Mode

Whenever $\overline{EMODE}$ is being asserted, interlocked-operation paralleling also is available, by appropriate interconnection of the FIFO's expansion inputs.

The retransmit facility is available during standalone operation, in either IDT-Compatible Operating Mode or Enhanced Operating Mode. (See Tables 1 and 2.) It is inoperative if the $\overline{FL}/RT$ input signal is grounded. It is not an IDT72215B/25B feature. ***The Retransmit control signal causes the internal FIFO read-address pointer to be set back to zero, without affecting the internal FIFO write-address pointer. Thus, the Retransmit control signal also provides a mechanism whereby a block of data delimited by the zero physical address and the current write-address-pointer address may be read out repeatedly, an arbitrary number of times. The only restrictions are that neither the read-address pointer nor the write-address pointer may 'wrap around' during this entire process, and that the retransmit facility is not available during depth-cascaded operation, either in IDT-Compatible Operating Mode or in Enhanced Operating Mode. (See Tables 1 and 2.) Also, the flags behave differently for a short time after a retransmit operation. Otherwise, the retransmit facility is available during standalone operation, in either IDT-Compatible Operating Mode or Enhanced Operating Mode.***

Programming the programmable-flag offsets, ***the timing synchronization of the various status flags, the optional read-suppression functionality of $\overline{OE}$***, and the behavior of the pointers which access the offset-value registers ***and the Control Register*** may be individually controlled by asserting the signal $\overline{LD}$, without any reset operation. When $\overline{LD}$ is being asserted, and writing is being enabled by asserting $\overline{WEN}$, some portion of the input bus word $D_0 - D_{17}$ is used at the next rising edge of WCLK to program one or more of the programmable registers on successive write clocks. Likewise, the values programmed into these programmable registers may be read out for verification by asserting $\overline{LD}$ and $\overline{REN}$, with the outputs $Q_0 - Q_{17}$ enabled. Reading out these programmable registers should not be initiated while they are being written into. Table 3 defines the possible modes of operation for loading and reading out the contents of programmable registers.

In the Enhanced Operating Mode, coordinated operation of two 18-bit FIFOs as one 36-bit FIFO may be ensured by 'interlocked' crosscoupling of the status-flag outputs from each FIFO to the expansion inputs of the other one; that is, $\overline{FF}$ to $\overline{WXI}/WEN_2$, and $\overline{EF}$ to $\overline{RXI}/REN_2$, in both directions between two paralleled FIFOs. This 'interlocked' operation takes effect automatically, if two paralleled FIFOs are crossconnected in this manner, with the $\overline{EMODE}$ control input being asserted (LOW). (See Tables 1 and 2.) IDT-compatible depth cascading no longer is available when operating in this 'interlocked-paralleled' mode; however, pipelined depth cascading remains available.

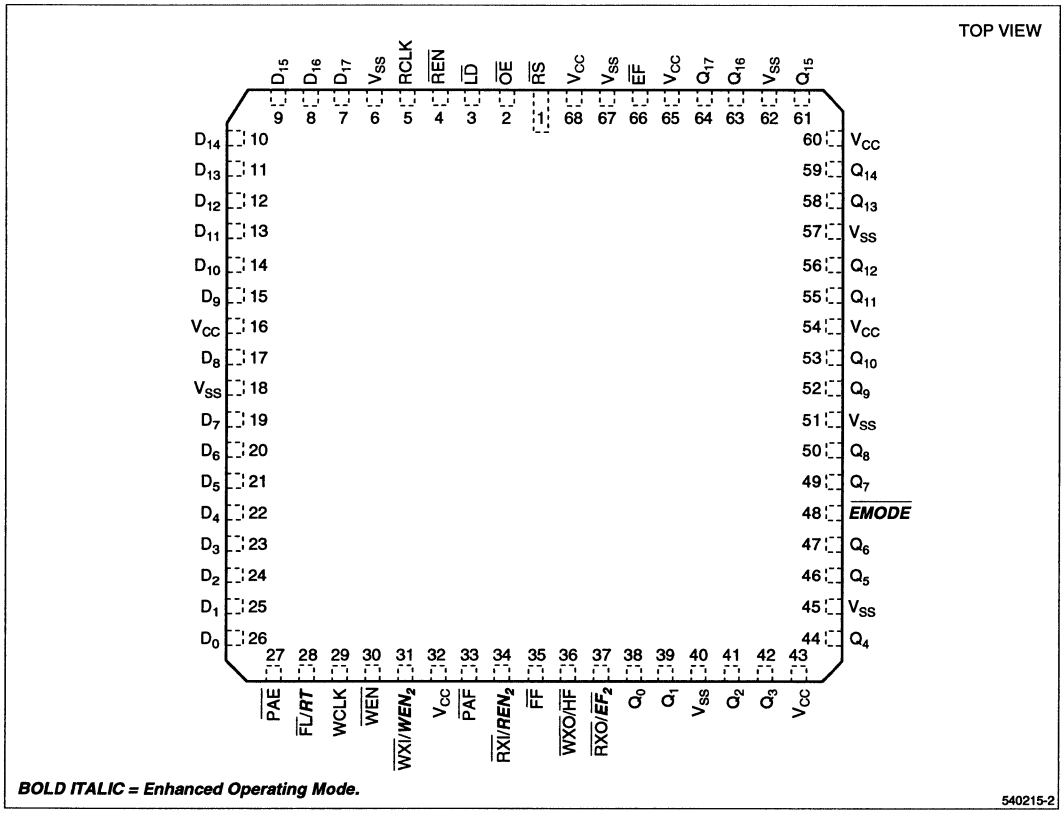


Figure 2. Pin Connections for PLCC Package

SUMMARY OF SIGNALS/PINS

PIN	NAME
$D_0 - D_{17}$	Data Inputs
$\overline{RS}$	Reset
$\overline{EMODE}$	***Enhanced Operating Mode***
WCLK	Write Clock
$\overline{WEN}$	Write Enable
RCLK	Read Clock
$\overline{REN}$	Read Enable
$\overline{OE}$	Output Enable
$\overline{LD}$	Load
$\overline{FL}$/***RT***	First Load/***Retransmit***
$\overline{WXI}$/***WEN2***	Write Expansion Input/***Write Enable 2***

PIN	NAME
$\overline{RXI}$/***REN2***	Read Expansion Input/***Read Enable 2***
$\overline{FF}$	Full Flag
$\overline{PAF}$	Programmable Almost-Full Flag
$\overline{WXO}$/$\overline{HF}$	Write Expansion Output/Half-Full Flag
$\overline{PAE}$	Programmable Almost-Empty Flag
$\overline{EF}$	Empty Flag
$\overline{RXO}$/***EF2***	Read Expansion Output/***Empty Flag 2***
$Q_0 - Q_{17}$	Data Outputs
V_{CC}	Power
V_{SS}	Ground

BOLD ITALIC = Enhanced Operating Mode

PIN DESCRIPTIONS

PIN	NAME	PIN TYPE [1]	DESCRIPTION
$D_0 - D_{17}$	Data Inputs	I	Data inputs from an 18-bit bus.
$\overline{RS}$	Reset	I	When $\overline{RS}$ is taken LOW, the FIFO's internal read and write pointers are set to address the first physical location of the RAM array; $\overline{FF}$ and $\overline{PAF}$ go HIGH; and $\overline{PAE}$ and $\overline{EF}$ go LOW. The programmable-flag-offset registers ***and the Control Register*** are set to their default values. (But see the description of ***EMODE***, below.) A reset is required before an initial read or write operation after power-up.
$\overline{EMODE}$	***Enhanced Operating Mode***	***I***	***When $\overline{EMODE}$ is held LOW, the default setting for Control Register bits 00-05 after a reset operation changes to HIGH rather than LOW, thus enabling all Control-Register-controllable Enhanced Operating Mode features, and allowing access to the Control Register for reprogramming or readback. (See Tables 1, 2 and 5.) If this behavior is desired, EMODE may be grounded; however, Control Register bits 00-05 still may be individually programmed to selectively enable or disable certain of the Enhanced Mode features, even though those features associated with interlocked-paralleled operation always are enabled whenever EMODE is being asserted. (See Table 2.) Alternatively, EMODE may be tied to V_{CC}, so that the FIFO is functionally IDT-compatible, and the Control Register is not accessible or visible. Controlling EMODE dynamically during system operation is not recommended.***
WCLK	Write Clock	I	Data is written into the FIFO on a LOW-to-HIGH transition of WCLK, whenever $\overline{WEN}$ (Write Enable) is being asserted (LOW), and $\overline{LD}$ is HIGH. If $\overline{LD}$ is LOW, a programmable register rather than the internal FIFO memory is written into.
$\overline{WEN}$	Write Enable	I	When $\overline{WEN}$ is LOW and $\overline{LD}$ is HIGH, an 18-bit data word is written into the FIFO on every LOW-to-HIGH transition of WCLK. When $\overline{WEN}$ is HIGH, the FIFO internal memory continues to hold the previous data. (See Table 3.) Data will not be written into the FIFO if $\overline{FF}$ is LOW. ***In the Enhanced Operating Mode, WEN_2 is ANDed with $\overline{WEN}$ to produce an effective internal write-enable signal.*** [2]
RCLK	Read Clock	I	Data is read from the FIFO on a LOW-to-HIGH transition of RCLK whenever $\overline{REN}$ (Read Enable) is being asserted (LOW), and $\overline{LD}$ is HIGH. If $\overline{LD}$ is LOW, a programmable register rather than the internal FIFO memory is read from.
$\overline{REN}$	Read Enable	I	When $\overline{REN}$ is LOW and $\overline{LD}$ is HIGH, an 18-bit data word is read from the FIFO on every LOW-to-HIGH transition of RCLK. When $\overline{REN}$ is HIGH, and/or also when $\overline{EF}$ is LOW, the FIFO's output register continues to hold the previous data word, whether or not $Q_0 - Q_{17}$ (the data outputs) are enabled. (See Table 3.) ***In the Enhanced Operating Mode, REN_2 is ANDed with $\overline{REN}$ (and whenever Control Register bit 05 is HIGH, also with $\overline{OE}$) to produce an effective internal read-enable signal.*** [2]
$\overline{OE}$	Output Enable	I	When $\overline{OE}$ is LOW, the FIFO's data outputs drive the bus to which they are connected. If $\overline{OE}$ is HIGH, the FIFO's outputs are in high-Z (high-impedance) state. ***In the Enhanced Operating Mode, $\overline{OE}$ not only continues to control the outputs in this same manner, but also can function as an additional $\overline{ANDing}$ input to the combined effective read-enable signal, along with $\overline{REN}$ and REN_2, whenever Control Register bit 05 is HIGH. (See Table 5.)*** [2]
$\overline{LD}$	Load	I	When $\overline{LD}$ is LOW, the data word on $D_0 - D_{17}$ (the data inputs) is written into a programmable-flag-offset register, ***or into the Control Register (when in the Enhanced Operating Mode),*** on the LOW-to-HIGH transition of WCLK, whenever $\overline{WEN}$ is LOW. (See Table 3.) Also, when $\overline{LD}$ is LOW, a word is read to $Q_0 - Q_{17}$ (the data outputs) from the offset registers ***and/or the Control Register (when in the Enhanced Operating Mode)*** on the LOW-to-HIGH transition of RCLK, whenever $\overline{REN}$ is LOW. (See again Table 3.) When $\overline{LD}$ is HIGH, normal FIFO write and read operations are enabled.

[1] I = Input, O = Output, Z = High-Impedance, V = Power Voltage Level

[2] The ostensible differences in signal assertiveness are reconciled before ANDing.

BOLD ITALIC = Enhanced Operating Mode

PIN DESCRIPTIONS (cont'd)

PIN	NAME	PIN TYPE[1]	DESCRIPTION
$\overline{FL}$/***RT***	First Load/ ***Retransmit***	I	In the standalone or paralleled configuration, $\overline{FL}$ may be grounded. ***However, in the standalone or paralleled configuration, if FL is taken HIGH, it functions instead as RT (Retransmit), and resets the FIFO's internal read pointer to the first physical location of the RAM array. Note that although Retransmit is an 'enhanced' feature, it is always available for a FIFO during standalone operation, whether the FIFO is in IDT-Compatible Operating Mode or in Enhanced Operating Mode; it is not regulated by the Control Register or by the EMODE control input.*** In IDT-compatible cascaded configuration, $\overline{FL}$ has an entirely different function; it is grounded for the first FIFO device (the 'master' device or 'first-load' device), and is set to HIGH for all other FIFO devices in the daisy chain. Thus, the ***Retransmit*** feature is not available for FIFOs operating in a cascaded configuration. The external differences in signal assertiveness are reconciled before ANDing. [2]
$\overline{WXI}$/***WEN_2***	Write Expansion Input/***Write Enable 2***	I	This signal is dual-purpose; its functionality is determined during a reset operation, according to its own state, and also according to the states of the three other control inputs RXI/***REN_2***, FL/***RT***, and ***EMODE***. (See Tables 1 and 2.) In the standalone or paralleled configuration, $\overline{WXI}$/***WEN_2*** is grounded. In the cascaded configuration, $\overline{WXI}$/***WEN_2*** is connected to $\overline{WXO}$ (Write Expansion Output) of the previous device, and functions as $\overline{WXI}$. ***In the Enhanced Operating Mode, WXI/WEN_2 functions as a second write-enable signal, WEN_2, which is ANDed with WEN to produce an effective internal write-enable signal.*** [2]
$\overline{RXI}$/***REN_2***	Read Expansion Input/***Read Enable 2***	I	This signal is dual-purpose; its functionality is determined during a reset operation, according to its own state, and also according to the states of the three other control inputs WXI/***WEN_2***, FL/***RT***, and ***EMODE. (See Tables 1 and 2.)*** In the standalone or paralleled configuration, RXI/REN_2 is grounded. In the cascaded configuration, RXI/REN_2 is connected to RXO (Read Expansion Output) of the previous device, and functions as $\overline{RXI}$. ***In the Enhanced Operating Mode, $\overline{RXI}$/$\overline{REN_2}$ functions as a second read-enable signal, REN_2, which is ANDed with REN – and perhaps also with OE, if Control-Register bit 05 is HIGH – to produce an effective internal read-enable signal.*** [2]
$\overline{FF}$	Full Flag	O	When $\overline{FF}$ is LOW, the FIFO is full; further advancement of its internal write-address pointer, and further data writes into its inputs, are inhibited. When $\overline{FF}$ is HIGH, the FIFO is not full. $\overline{FF}$ is synchronized to WCLK. $\overline{FF}$ is functionally equivalent to an assertive-HIGH 'Input Ready' status output signal.
$\overline{PAF}$	Programmable Almost-Full Flag	O	When $\overline{PAF}$ is LOW, the FIFO is 'almost full,' based on the almost-full-offset value programmed into the FIFO. The default value of this offset at reset is one-eighth of the total number of words in the FIFO-memory array, minus one, measured from 'full.' (See Table 4.) In the IDT-Compatible Operating Mode, $\overline{PAF}$ is asynchronous. ***In the Enhanced Operating Mode, PAF is synchronized to WCLK after a reset operation, according to the state of Control Register bit 04. (See Table 5.)***
$\overline{WXO}$/$\overline{HF}$	Write Expansion Output/ Half-Full Flag	O	This signal is dual-purpose; its functionality is determined during a reset operation according to the states of the two control inputs WXI/***WEN_2*** and RXI/***REN_2***. (See Tables 1 and 2.) In the standalone or paralleled configuration, whenever $\overline{HF}$ is LOW the device is more than half full. In IDT-Compatible Operating Mode, $\overline{HF}$ is asynchronous; ***in the Enhanced Operating Mode, HF may be synchronized either to WCLK or to RCLK after a reset operation, according to the state of Control Register bits 02 and 03. (See Table 5.)*** In the IDT-compatible cascaded configuration, a pulse is sent from $\overline{WXO}$ to the $\overline{WXI}$ input of the next FIFO in the daisy-chain cascade, whenever the last location in the FIFO is written.

[1] I = Input, O = Output, Z = High-Impedance, V = Power Voltage Level

[2] The ostensible differences in signal assertiveness are reconciled before ANDing.

BOLD ITALIC = Enhanced Operating Mode

PIN DESCRIPTIONS (cont'd)

PIN	NAME	PIN TYPE [1]	DESCRIPTION
$\overline{PAE}$	Programmable Almost-Empty Flag	O	When $\overline{PAE}$ is LOW, the FIFO is 'almost empty,' based on the almost-empty-offset value programmed into the FIFO. The default value of this offset at reset is one-eighth of the total number of words in the FIFO-memory array, minus one, measured from 'empty.' (See Table 4.) In IDT-Compatible Operating Mode, $\overline{PAE}$ is asynchronous. ***In the Enhanced Operating Mode, $\overline{PAE}$ is synchronized to RCLK after a reset operation, according to the state of Control Register bit 01. (See Table 5.)***
$\overline{EF}$	Empty Flag	O	When $\overline{EF}$ is LOW, the FIFO is empty; further advancement of its internal read-address pointer, and further changes in the data word present at its outputs, are inhibited. When $\overline{EF}$ is HIGH, the FIFO is not empty. $\overline{EF}$ is synchronized to RCLK. $\overline{EF}$ is functionally equivalent to an assertive-HIGH 'Output Ready' status output signal.
$\overline{RXO}/\overline{EF_2}$	Read Expansion Output	O	This signal is dual-purpose; its functionality is determined by the state of the ***EMODE*** control input during a reset operation. (See Tables 1 and 2.) In the IDT-Compatible Operating Mode, in a cascaded configuration, a pulse is sent from RXO to the RXI input of the next FIFO in the daisy-chain cascade, whenever the last location of the FIFO is read. ***In the Enhanced Operating Mode, whenever EMODE is being asserted (LOW), $\overline{EF_2}$ behaves as an exact duplicate of $\overline{EF}$, but delayed by one full cycle of RCLK with respect to $\overline{EF}$.***
$Q_0 - Q_{17}$	Data Outputs	O/Z	Data outputs to drive an 18-bit bus.
V_{CC}	Power	V	Seven +5 V power-supply pins.
V_{SS}	Ground	V	Eight 0 V ground pins.

[1] I = Input, O = Output, Z = High-Impedance, V = Power Voltage Level

BOLD ITALIC = Enhanced Operating Mode

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING
Supply Voltage to V_{SS} Potential	−0.5 V to 7 V
Signal Pin Voltage to V_{SS} Potential	−0.5 V to V_{CC} + 0.5 V
DC Output Current [1]	±75 mA
Temperature Range with Power Applied [2]	−55°C to 125°C
Storage Temperature Range	−65°C to 150°C
Power Dissipation (PLCC Package Limit)	2 W

NOTES:
1. Only one output may be shorted at a time, for a period not exceeding 30 seconds.
2. Measured with clocks idle.

OPERATING RANGE

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
T_A	Temperature, Ambient	0	70	C
V_{CC}	Supply Voltage	4.5	5.5	V
V_{SS}	Supply Voltage	0	0	V
V_{IL}	Logic LOW Input Voltage	−0.5	0.8	V
V_{IH}	Logic HIGH Input Voltage	2.0	V_{CC} + 0.5	V

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN.	MAX.	UNIT
I_{LI}	Input Leakage	V_{CC} = 5.5 V, V_{IN} = 0 V to V_{CC}	−1	1	µA
I_{LO}	I/O Leakage	$\overline{OE} \geq V_{IH}$, 0 V ≤ $V_{OUT} \leq V_{CC}$	−2	2	µA
V_{OH}	Output HIGH Voltage	I_{OH} = −8.0 mA	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 16.0 mA		0.4	V
I_{CC}	Average Operating Supply Current [1]	Measured at f_{CC} = maximum		250	mA
I_{CC2}	Average Standby Supply Current	All inputs = V_{IHMIN} (clocks idle)		60	mA
I_{CC3}	Power-Down Supply Current	All inputs = V_{CC} − 0.2 V (clocks idle)		1	mA

NOTE:
1. Output load is disconnected.

AC TEST CONDITIONS

PARAMETER		RATING
Input Pulse Levels		V_{SS} to 3 V
Input Rise and Fall Times (10% to 90%)		3 ns
Input Timing Reference Levels		1.5 V
Output Timing Reference Levels		1.5 V
Output Load, Timing Tests (Figure 3)	R_1 (Top Resistor)	1.1k Ω
	R_2 (Bottom Resistor)	680 Ω
	C_L (Load Capacitance)	30 pF

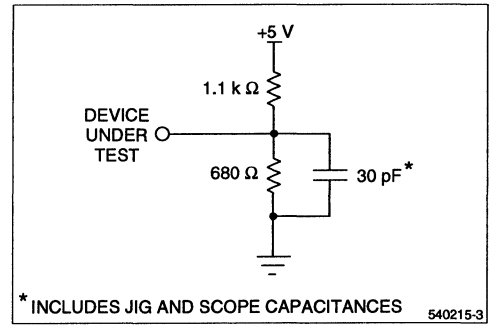


Figure 3. Output Load Circuit

CAPACITANCE

PARAMETER	RATING
C_{IN} (Input Capacitance) V_{IN} = 0 V	10 pF
C_{OUT} (Output Capacitance) V_{OUT} = 0 V	10 pF

BOLD ITALIC = Enhanced Operating Mode

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	-20		-25		-35	
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.
f_{CC}	Clock Cycle Frequency		50		40		28.6
t_A	Data Access Time	2	12	3	15	3	20
t_{CLK}	Clock Cycle Time	20		25		35	
t_{CLKH}	Clock HIGH Time	8		10		14	
t_{CLKL}	Clock LOW Time	8		10		14	
t_{DS}	Data Setup Time	5		6		7	
t_{DH}	Data Hold Time	1		1		2	
t_{ENS}	Enable Setup Time	5		6		7	
t_{ENH}	Enable Hold Time	1		1		2	
t_{RS}	Reset Pulse Width [1]	20		25		35	
t_{RSS}	Reset Setup Time [2]	12		15		20	
t_{RSR}	Reset Recovery Time [2]	12		15		20	
t_{RSF}	Reset to Flag and Output Time		30		35		40
t_{OLZ}	Output Enable to Output in Low-Z [2]	0		0		0	
t_{OE}	Output Enable to Output Valid		9		12		15
t_{OHZ}	Output Enable to Output in High-Z [2]	1	9	1	12	1	15
t_{WFF}	Write Clock to Full Flag		12		15		20
t_{REF}	Read Clock to Empty Flag		12		15		20
t_{PAF}	Clock to Programmable Almost-Full Flag (IDT-Compatible Operating Mode)		14		17		23
t_{PAE}	Clock to Programmable Almost-Empty Flag (IDT-Compatible Operating Mode)		14		17		23
t_{HF}	Clock to Half-Full Flag (IDT-Compatible Operating Mode)		14		17		23
t_{PAFS}	***Clock to Programmable Almost-Full Flag (Enhanced Operating Mode)***		***14***		***17***		***23***
t_{PAES}	***Clock to Programmable Almost-Empty Flag (Enhanced Operating Mode)***		***14***		***17***		***23***
t_{HFS}	***Clock to Half-Full Flag (Enhanced Operating Mode)***		***14***		***17***		***23***
t_{XO}	Clock to Expansion-Out		12		15		20
t_{XI}	Expansion-In Pulse Width	8		10		14	
t_{XIS}	Expansion-In Setup Time	8		10		15	
t_{SKEW1}	Skew Time Between Read Clock and Write Clock for Full Flag [3]	14		16		18	
t_{SKEW2}	Skew Time Between Write Clock and Read Clock for Empty Flag [4]	14		16		18	

NOTES:

1. Pulse widths less than the stated minimum values may cause incorrect operation.
2. Values are guaranteed by design; not currently tested.
3. These times also apply to the Programmable-Almost-Full and Half-Full flags when they are synchronized to WCLK.
4. These times also apply to the Half-Full and Programmable-Almost-Empty flags when they are synchronized to RCLK.

BOLD ITALIC = Enhanced Operating Mode

DESCRIPTION OF SIGNALS AND OPERATING SEQUENCES

Table 1. Grouping-Mode Determination During a Reset Operation [4]

$\overline{EMODE}$	$\overline{WXI}$/WEN_2	$\overline{RXI}$/REN_2	$\overline{FL}$/RT	MODE	$\overline{WXO}$/$\overline{HF}$ USAGE	$\overline{WXI}$/WEN_2 USAGE	$\overline{RXI}$/REN_2 USAGE	$\overline{FL}$/RT USAGE	$\overline{RXO}$/$\overline{EF_2}$ USAGE
H	H	H	H	Cascaded Slave [1]	$\overline{WXO}$	$\overline{WXI}$	$\overline{RXI}$	$\overline{FL}$	$\overline{RXO}$
H	H	H	L	Cascaded Master [1]	$\overline{WXO}$	$\overline{WXI}$	$\overline{RXI}$	$\overline{FL}$	$\overline{RXO}$
H	H	L	X	(Reserved)	–	–	–	–	–
H	L	H	X	(Reserved)	–	–	–	–	–
H	L	L	H [2]	(Not Allowed)	($\overline{HF}$)	(none)	(none)	***(RT)***	(none)
H	L	L	L [2]	Standalone	$\overline{HF}$	(none)	(none)	***RT***	(none)
L	***X***	***X***	***L*** [2]	***Interlocked Paralleled*** [3]	$\overline{HF}$	WEN_2	REN_2	***RT***	$\overline{EF_2}$

NOTES:

1. The terms 'master' and 'slave' refer to IDT-compatible cascading. In pipelined cascading[3], there is no such distinction.
2. ***Once grouping mode has been determined during a reset operation, $\overline{FL}$/RT then may go HIGH to activate a retransmit operation.***
3. ***$\overline{EMODE}$ must be asserted for access to the Control Register to be enabled. Also, FIFOs being used in a pipelined-cascading configuration should be in Interlocked Paralleled mode.***
4. Setup-time and recovery-time specifications apply during a reset operation.
5. H = HIGH; L = LOW; X = Don't Care.

Table 2. Expansion-Pin Usage According to Grouping Mode

I/O	PIN	IDT-COMPATIBLE OPERATING MODE			ENHANCED OPERATING MODE
		MASTER	SLAVE	STANDALONE	*INTERLOCKED PARALLELED*
I	$\overline{WXI}$/WEN_2	From $\overline{WXO}$ (n-1st FIFO)	From $\overline{WXO}$ (n-1st FIFO)	Grounded	***From $\overline{FF}$ (other FIFO)***
O	$\overline{WXO}$/$\overline{HF}$	To $\overline{WXI}$ (n+1st FIFO)	To $\overline{WXI}$ (n+1st FIFO)	Becomes $\overline{HF}$	***Becomes $\overline{HF}$***
I	$\overline{RXI}$/REN_2	From $\overline{RXO}$ (n-1st FIFO)	From $\overline{RXO}$ (n-1st FIFO)	Grounded	***From $\overline{EF}$ (other FIFO)***
O	$\overline{RXO}$/$\overline{EF_2}$	To $\overline{RXI}$ (n+1st FIFO)	To $\overline{RXI}$ (n+1st FIFO)	Unused	***Becomes $\overline{EF_2}$***
I	$\overline{FL}$/RT	Grounded (Logic LOW)	Logic HIGH	***Becomes RT*** [1]	***Becomes RT*** [1]

NOTE:

1. $\overline{FL}$/RT may be grounded if ***the Retransmit facility*** is not being used.

BOLD ITALIC = Enhanced Operating Mode

Table 3. Selection of Read and Write Operations

$\overline{LD}$	$\overline{WEN}^3$	$\overline{REN}^3$	WCLK	RCLK	ACTION
L	X	X	–	–	No operation.
L	L	H	∧	–	Write to a programmable register. [1]
L	H	H	∧	–	Hold present value of programmable-register write counter, and do not write. [2]
L	H	L	–	∧	Read from a programmable register. [1]
L	H	H	–	∧	Hold present value of programmable-register read counter, and do not read. [2]
L	X	X	∧	∧	Illegal combination, which will cause errors.
H	L	X	∧	X	Normal FIFO write operation.
H	X	L	X	∧	Normal FIFO read operation.
H	L	X	–	X	No write operation.
H	H	X	X	X	No write operation.
H	X	L	X	–	No read operation.
H	X	H	X	X	No read operation.
H	L	L	–	–	No operation.
H	H	H	X	X	No operation.

KEY:

H = Logic 'HIGH'; L = Logic 'LOW'; X = 'Don't-care' (logic 'HIGH,' logic 'LOW,' or any transition);

∧ = A 'LOW'-to-'HIGH' transition; – = Any condition EXCEPT a 'LOW'-to-'HIGH' transition.

NOTES:

1. The selection of a programmable register to be written or read is controlled by two simple state machines. One state machine controls the selection for writing; the other state machine controls the selection for reading. These two state machines operate independently of each other. Both state machines are reset to point to Word 0 by a reset operation. ***In the Enhanced Operating Mode, if Control Register bit 00 is set, both state machines are also reset to point to Word 0 by deassertion of $\overline{LD}$ after $\overline{LD}$ has been asserted (that is, by a rising edge of $\overline{LD}$), followed by a valid write cycle for the writing-control state machine and/or by a valid read cycle for the reading-control state machine.***
2. The order of the two programmable registers which are accessible in IDT-Compatible Operating Mode, as selected by either state machine, is always:
   Word 0: Almost-Empty Offset Register
   Word 1: Almost-Full Offset Register
   Word 0: Almost-Empty Offset Register
   ...
   (repeats indefinitely)
   ...

   The order of the three programmable registers which are accessible in Enhanced Operating Mode, as selected by either state machine, is always:
   Word 0: Almost-Empty Offset Register
   Word 1: Almost-Full Offset Register
   Word 2: Control Register
   Word 0: Almost-Empty Offset Register
   ...
   (repeats indefinitely)
   ...

   In IDT-Compatible Operating Mode, Word 2 is not accessed, and Word 0 and Word 1 alternate.
3. After normal FIFO operation has begun, writing new contents into either of the two offset registers is not recommended, as it may cause erroneous output values for the respective flag outputs.
4. ***WEN_2, REN_2, and $\overline{OE}$ may be ANDed terms in the enabling of read and write operations, according to the state of the $\overline{EMODE}$ control input and of Control Register bit 05.***

BOLD ITALIC = Enhanced Operating Mode

Table 4. Status Flags

NUMBER OF UNREAD DATA WORDS PRESENT WITHIN FIFO [1,2]		FULL FLAG	MIDDLE FLAGS			EMPTY FLAG
512 × 18 FIFO	1024 × 18 FIFO	$\overline{FF}$	PAF	$\overline{HF}$	PAE	$\overline{EF}$
0	0	H	H	H	L	L
1 to q	1 to q	H	H	H	L	H
(q + 1) to 256	(q + 1) to 512	H	H	H	H	H
257 to (512 – (p + 1))	513 to (1024 – (p + 1))	H	H	L	H	H
(512 – p) to 511	(1024 – p) to 1023	H	L	L	H	H
512	1024	L	L	L	H	H

NOTES:

1. q = Programmable-Almost-Empty Offset value. (Default values: 512 × 18, q = 63; 1024 × 18, q = 127.)
2. p = Programmable-Almost-Full Offset value. (Default values: 512 × 18, p = 63; 1024 × 18, p = 127.)
3. Only 9 (512 × 18) or 10 (1024 × 18) of the 12 offset-value-register bits should be programmed. The unneeded most-significant-end bits should be LOW (zero).
4. The flag output is delayed by one full clock cycle in Enhanced Operating Mode, when synchronous operation is specified for intermediate flags.

BOLD ITALIC = Enhanced Operating Mode

DESCRIPTION OF SIGNALS AND OPERATING SEQUENCES (cont'd)

Table 5. Control-Register Format

COMMAND REGISTER BITS	CODE	VALUE AFTER RESET		FLAG AFFECTED, IF ANY	DESCRIPTION	NOTES
		$\overline{EMODE}$ = H	$\overline{EMODE}$ = L			
00	L	L	H	–	Deassertion of $\overline{LD}$ does not reset the programmable-register write pointer and read pointer.	IDT-compatible addressing of programmable registers.
	H				Deassertion of $\overline{LD}$ resets the programmable-register write pointer and read pointer to address Word 0, the Programmable-Almost-Empty-Flag-Offset Register. The change takes effect after a valid write operation or a valid read operation, respectively.	Non-ambiguous addressing of programmable registers.
01	L	L	H	$\overline{PAE}$	Set by ↑RCLK, reset by ↑WCLK.	Asynchronous flag clocking.
	H				Set and reset by ↑RCLK.	Synchronous flag clocking.
03, 02	LL	LL	HH	$\overline{HF}$	Set by ↑WCLK, reset by ↑RCLK.	Asynchronous flag clocking.
	LH				Set and reset by ↑RCLK.	Synchronous flag clocking at output port.
	HL, HH				Set and reset by ↑WCLK.	Synchronous flag clocking at input port.
04	L	L	H	$\overline{PAF}$	Set by ↑WCLK, reset by ↑RCLK.	Asynchronous flag clocking.
	H				Set and reset by ↑WCLK.	Synchronous flag clocking.
05	L	L	H	–	$\overline{OE}$ has no effect on an internal read operation, apart from disabling the outputs.	Allows the read-address pointer to advance even when $Q_0 - Q_{17}$ are not driving the output bus.
	H				$\overline{OE}$ inhibits a read operation whenever the data outputs $Q_0 - Q_{17}$ are in the high-Z state.	Inhibits the read-address pointer from advancing when $Q_0 - Q_{17}$ are not driving the output bus; thus, guards against data loss.
06	L	L	L	–	Reserved.	Future use to control depth cascading and interlocked paralleling.
	H					
07, 08, 09, 10,11	LLLLL	LLLLL	LLLLL	–	Reserved.	Reserved.

NOTES:

1. When $\overline{EMODE}$ is HIGH, and ***Control Register bits 00-05 are LOW,*** the FIFO behaves in a manner functionally equivalent to the IDT72215B/25B FIFO of similar depth and speed grade. Under these conditions, the ***Control Register*** is not visible or accessible to the external system which includes the FIFO.
2. If $\overline{EMODE}$ is not asserted (is HIGH), ***Control Register bits 00-05 remain LOW*** after a reset operation. ***However, if $\overline{EMODE}$ is asserted (is LOW) during a reset operation, Control Register bits 00-05 are forced HIGH, and remain HIGH until changed. Control Register bits 06-11 are unaffected by $\overline{EMODE}$.***

BOLD ITALIC = Enhanced Operating Mode

Data Inputs

DATA IN ($D_0 - D_{17}$)

Data, programmable-flag-offset values, and Control-Register codes are input to the FIFO as 18-bit words on $D_0 - D_{17}$. Unused bit positions in offset-value and *Control-Register* words should be zero-filled.

Control Inputs

RESET ($\overline{RS}$)

The FIFO is reset whenever the asynchronous Reset ($\overline{RS}$) input is taken to a LOW state. A reset operation is required after power-up, before the first write operation may occur. The state of the FIFO is fully defined after a reset operation. If the default values which are entered into the Programmable-Flag-Offset-Value Registers and the *Control Register* by a reset operation are acceptable, then no device programming is required. A reset operation initializes the FIFO's internal read-address and write-address pointers to the FIFO's first physical memory location. The five status flags, $\overline{FF}$, $\overline{PAF}$, $\overline{HF}$, $\overline{PAE}$, and $\overline{EF}$, are updated to indicate that the FIFO is completely empty; thus, the first three of these are reset to HIGH, and the last two are reset to LOW. The flag-offset values for $\overline{PAF}$ and $\overline{PAE}$ each are initialized to one-eighth of the depth of a single FIFO, minus one; 63 for a 512-word FIFO, and 127 for a 1024-word FIFO. If ***$\overline{EMODE}$*** is not being asserted (i.e., if ***$\overline{EMODE}$*** is HIGH), the *Control Register* is initialized to configure the FIFO to operate in the IDT72215B/25B-Compatible Operating Mode. Until a write operation occurs, the data outputs $D_0 - D_{17}$ all are LOW whenever $\overline{OE}$ is LOW.

ENHANCED OPERATING MODE ($\overline{EMODE}$)

Whenever $\overline{EMODE}$ is asserted during a reset operation, Control Register bits 00-05 remain HIGH rather than LOW after the completion of the reset operation. Thus, $\overline{EMODE}$ has the effect of activating Enhanced-Operating-Mode features, without the need to configure the Control Register by the normal programming method. The behavior of these Enhanced-Operating-Mode features is described in Table 5. For permanent Enhanced-Operating-Mode operation, $\overline{EMODE}$ must be grounded; dynamic control of $\overline{EMODE}$ during system operation is not recommended.

Asserting $\overline{EMODE}$ during a reset operation also causes $\overline{WXI}/WEN_2$ to be configured as WEN_2, and $\overline{RXI}/REN_2$ to be configured as REN_2, to support interlocked-paralleled operation of two FIFOs 'side by side.'

WRITE CLOCK (WCLK)

A rising edge (LOW-to-HIGH transition) of WCLK initiates a FIFO write cycle if $\overline{LD}$ is HIGH, or a programmable-register write cycle if $\overline{LD}$ is LOW. The 18 data inputs, and all input-side synchronous control inputs, must meet setup and hold times with respect to the rising edge of WCLK. The input-side status flags are meaningful after specified time intervals, following a rising edge of WCLK.

Conceptually, the WCLK input receives a free-running, periodic 'clock' waveform, which is used to control other signals which are edge-sensitive. However, there actually is not any absolute requirement that the WCLK waveform *must* be periodic. An 'asynchronous' mode of operation is in fact possible, if $\overline{WEN}$ is continuously asserted (that is, is continuously held LOW), and WCLK receives aperiodic 'clock' pulses of suitable duration. There likewise is no requirement that WCLK must have any particular synchronization relation to the read clock RCLK. These two clock inputs may in fact receive the same 'clock' signal; or they may receive totally-different signals, which are not synchronized to each other in any way.

WRITE ENABLE ($\overline{WEN}$)

Whenever $\overline{WEN}$ is being asserted (is LOW) and ***$\overline{LD}$*** is HIGH, and the FIFO is not full, an 18-bit data word is loaded into the effective input register for the memory array at every WCLK rising edge (LOW-to-HIGH transition). Data words are stored into the two-port memory array sequentially, regardless of any ongoing read operation. Whenever $\overline{WEN}$ is not being asserted (is HIGH), the input register retains whatever data word it contained previously, and no new data word gets loaded into the memory array.

To prevent overrunning the internal FIFO boundaries, further write operations are inhibited whenever the Full Flag ($\overline{FF}$) is being asserted (is LOW). If a valid read operation then occurs, upon the completion of that read cycle $\overline{FF}$ again goes HIGH after a time t_{WFF}, and another write operation is allowed to begin whenever WCLK makes another LOW-to-HIGH transition. Effectively, $\overline{WEN}$ is overridden by $\overline{FF}$; thus, during normal FIFO operation, $\overline{WEN}$ has no effect when the FIFO is full.

In the Enhanced Operating Mode, whenever $\overline{EMODE}$ is being asserted (is LOW), $\overline{WXI}/WEN_2$ functions as WEN_2, an additional duplicate (albeit assertive-HIGH) write-enable input, in order to provide an 'interlocking' mechanism for reliable synchronization of two paralleled FIFOs. To control writing, WEN_2 is combined with $\overline{WEN}$; the logic-AND function of $\overline{WEN}$ and WEN_2 then behaves like $\overline{WEN}$ in the foregoing description.

BOLD ITALIC = Enhanced Operating Mode

DESCRIPTION OF SIGNALS AND OPERATING SEQUENCES (cont'd)

READ CLOCK (RCLK)

A rising edge (LOW-to-HIGH transition) of RCLK initiates a FIFO read cycle if $\overline{LD}$ is HIGH, or a programmable-register read cycle if $\overline{LD}$ is LOW. All output-side synchronous control inputs must meet setup and hold times with respect to the rising edge of RCLK. The 18 data outputs, and the output-side status flags, are meaningful after specified time intervals, following a rising edge of RCLK.

Conceptually, the RCLK input receives a free-running, periodic 'clock' waveform, which is used to control other signals which are edge-sensitive. However, there actually is not any absolute requirement that the RCLK waveform *must* be periodic. An 'asynchronous' mode of operation is in fact possible, if $\overline{REN}$ is continuously asserted (that is, is continuously held LOW), and RCLK receives aperiodic 'clock' pulses of suitable duration. There likewise is no requirement that RCLK must have any particular synchronization relation to the write clock WCLK. These two clock inputs may in fact receive the same 'clock' signal; or they may receive totally-different signals, which are not synchronized to each other in any way.

READ ENABLE ($\overline{REN}$)

Whenever $\overline{REN}$ is being asserted (is LOW), and the FIFO is not empty, an 18-bit data word is loaded into the output register from the memory array at every RCLK rising edge (LOW-to-HIGH transition). Data words are read from the two-port memory array sequentially, regardless of any ongoing write operation. Whenever $\overline{REN}$ is not being asserted (is HIGH), the output register retains whatever data word it contained previously, and no new data word gets loaded into it from the memory array.

To prevent underrunning the internal FIFO boundaries, further read operations are inhibited whenever the Empty Flag ($\overline{EF}$) is being asserted (is LOW). If a valid write operation then occurs, upon the completion of that write cycle $\overline{EF}$ again goes HIGH after a time t_{REF}, and another read operation is allowed to begin whenever RCLK makes another LOW-to-HIGH transition. Effectively, $\overline{REN}$ is overridden by $\overline{EF}$; thus, during normal FIFO operation, $\overline{REN}$ has no effect when the FIFO is empty.

In the Enhanced Operating Mode, one (or, sometimes two) additional read-enable inputs may be combined with $\overline{REN}$ to control reading. The additional read-enable input(s) are $\overline{RXI}/REN_2$ (and $\overline{OE}$). The logic-AND function of these two (or three) inputs then behaves like $\overline{REN}$ in the foregoing description.

Whenever $\overline{EMODE}$ is being asserted (is LOW), $\overline{RXI}/REN_2$ functions as REN_2, an additional duplicate (albeit assertive-HIGH) Read-Enable input, in order to provide an 'interlocking' mechanism for reliable synchronization of two paralleled FIFOs. Also, if Control Register bit 05 has been set, $\overline{OE}$ takes on the extra role of serving as yet another duplicate read-enable input, in addition to its usual function of controlling the FIFO's data outputs, in order to inhibit further read operations whenever the FIFO's data outputs are disabled, and thereby to prevent data loss under some circumstances.

OUTPUT ENABLE ($\overline{OE}$)

$\overline{OE}$ is an assertive-LOW, asynchronous, output enable. In the IDT-Compatible Operating Mode, $\overline{OE}$ has only the effect of enabling or disabling the data outputs $Q_0 - Q_{17}$. That is, disabling $Q_0 - Q_{17}$ does not inhibit a read operation, for data being transmitted to the output register; the same data will remain available later, when the outputs are again enabled, unless subsequently overwritten. When $Q_0 - Q_{17}$ are enabled, each of these 18 data outputs is in a normal HIGH or LOW state, according to the bit pattern of the data word in the output register. When $Q_0 - Q_{17}$ are disabled, each of these outputs is in the high-Z (high-impedance) state.

In the Enhanced Operating Mode, if Control Register bit 05 has been set, $\overline{OE}$ behaves as an additional read-enable control input, as well as enabling and disabling the data outputs $Q_0 - Q_{17}$. Under these circumstances, incrementing the read-address pointer is inhibited whenever $Q_0 - Q_{17}$ are in the high-Z state. Thus, 'reading' successive words which fail ever to reach the outputs is prevented, as a safeguard against data loss.

LOAD ($\overline{LD}$)

The Sharp LH540215/25 FIFOs contain ***three*** 18-bit programmable registers. The contents of these three registers may be loaded with data from the data inputs $D_0 - D_{17}$, or read out onto the data outputs $Q_0 - Q_{17}$. The first two registers are the Programmable-Flag-Offset-Value Registers, for the Programmable Almost-Empty Flag ($\overline{PAE}$) and the Programmable Almost-Full Flag ($\overline{PAF}$) respectively. ***The third register is the Control Register, which includes several configuration-control bits for Sharp's Enhanced-Operating-Mode features.***

BOLD ITALIC = Enhanced Operating Mode

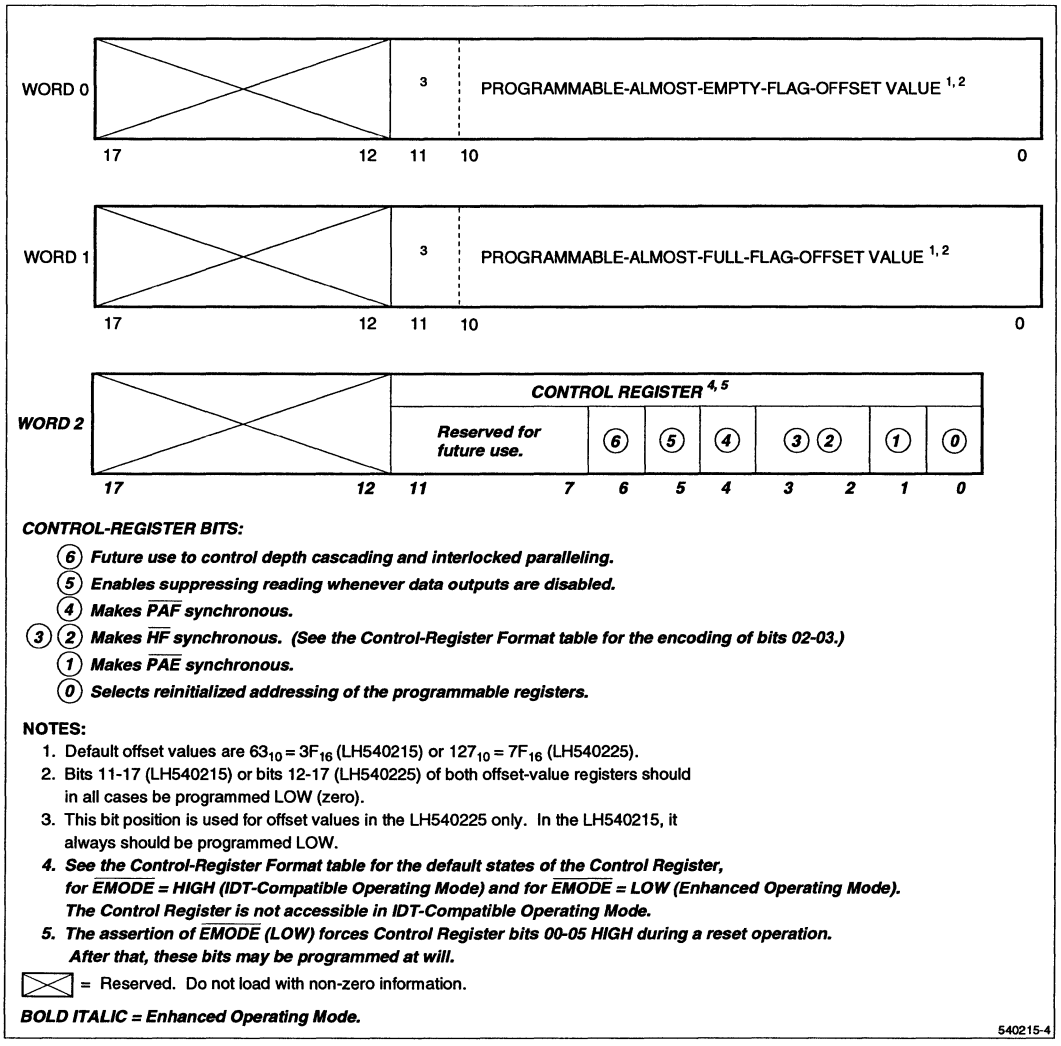


Figure 4. Programmable Registers

None of these three registers makes use of all of its available 18 bits. Figure 4 shows which bit positions of each register are operational. The two Programmable-Flag-Offset-Value Registers each contain an offset value in bits 0-10 (LH540215) or 0-11 (LH540225); bits 11-17 (LH540215) or 12-17 (LH540225) are unused. The default values for both offsets are one-eighth of the total number of words in the FIFO memory array, minus one: 63 for a 512 × 18 FIFO, and 127 for a 1024 × 18 FIFO.

The ***Control Register*** configuration is shown in Figure 4 and in Table 5. For the ***Control Register***, in the IDT-Compatible Operating mode, with ***EMODE*** deasserted (HIGH), the default value for any operational bit which has not been programmed is zero (LOW); ***in the Enhanced Operating Mode, with EMODE asserted (LOW), the default value for bits 00-05 is HIGH, and the default value for bits 06-11 is LOW.***

Whenever $\overline{LD}$ and $\overline{WEN}$ are simultaneously being asserted (are both LOW), the 18-bit data word from the data inputs $D_0 - D_{17}$ is written into the Programmable-Almost-Empty-Flag-Offset-Value Register at the first rising edge (LOW-to-HIGH transition) of the write clock (WCLK). (See Table 3.) If $\overline{LD}$ and $\overline{WEN}$ continue to be simultaneously asserted, another 18-bit data word from the data inputs $D_0 - D_{17}$ is written into the Programma-

BOLD ITALIC = Enhanced Operating Mode

DESCRIPTION OF SIGNALS AND OPERATING SEQUENCES (cont'd)

ble-Almost-Full-Flag-Offset-Value Register at the second rising edge of WCLK.

What happens next is determined by the state of the ***EMODE*** control input. If it is deasserted (HIGH), the next 18-bit word from the data inputs $D_0 - D_{17}$ is written back into the Programmable-Almost-Empty-Flag-Offset-Value Register again.

But, if EMODE is asserted (LOW), then still another 18-bit data word from the data inputs $D_0 - D_{17}$ is written into the Control Register at the third rising edge of WCLK. At the fourth rising edge of WCLK, writing again occurs to the Programmable-Almost-Empty-Flag-Offset-Value Register; and the same three-step writing sequence gets repeated on subsequent WCLK rising edges.

The lower nine bits of these offset-value words are made use of by the 512-word LH540215, and the lower ten bits by the 1024-word LH540225. *Five active bits are used for the Control Register*, by both the LH540215 and the LH540225. There is no restriction on the values which may occur in these data fields. However, ***reserved*** bit positions must be encoded LOW, in order to maintain forward compatibility.

Writing contents to these two or *three* programmable registers does not have to occur all at one time, or to be effected by one single sequence of steps. Whenever $\overline{LD}$ is being asserted (is LOW) but $\overline{WEN}$ is not being asserted (is HIGH), the FIFO's internal programmable-register-write-address pointer maintains its present value, without any writing actually taking place at each rising edge of WCLK. (See Table 3.) Thus, for instance, one or two programmable registers may be written, after which the FIFO may be returned to normal FIFO-array-read/write operation by deasserting $\overline{LD}$ (to HIGH).

Likewise, whenever $\overline{LD}$ and $\overline{REN}$ are simultaneously being asserted (are both LOW) the 18-bit data word (zero-filled as necessary) from the Programmable-Almost-Empty-Flag-Offset-Value Register is read to the data outputs $Q_0 - Q_{17}$ at the first rising edge (LOW-to-HIGH transition) of the read clock (RCLK). (See Table 3.) If $\overline{LD}$ and $\overline{REN}$ continue to be simultaneously asserted, another 18-bit data word from the Programmable-Almost-Full-Flag-Offset-Value Register is read to the data outputs $Q_0 - Q_{17}$ at the second rising edge of RCLK.

What happens next is determined by the state of the ***EMODE*** control input. If it is deasserted (HIGH), the next 18-bit word again comes from the Programmable-Almost-Empty-Flag-Offset-Value Register; it is read to the data outputs $Q_0 - Q_{17}$.

But, if EMODE is asserted (LOW), then the next 18-bit data word instead comes from the Control Register; it is read to the data outputs $Q_0 - Q_{17}$ at the third rising edge of RCLK. At the fourth rising edge of RCLK, reading again occurs from the Programmable-Almost-Empty-Flag-Offset-Value Register; and the same three-step reading sequence gets repeated on subsequent RCLK rising edges.

Reading contents from these two or ***three*** programmable registers does not have to occur all at one time, or to be effected by one single sequence of steps. Whenever $\overline{LD}$ is being asserted (is LOW) but $\overline{REN}$ is not being asserted (is HIGH), the FIFO's internal programmable-register-read-address pointer maintains its present value, without any reading actually taking place at each rising edge of RCLK. (See Table 3.) Thus, for instance, one or two programmable registers may be read, after which the FIFO may be returned to normal FIFO-array-read/write operation by deasserting $\overline{LD}$ (to HIGH).

To ensure correct operation, rising edges of WCLK and RCLK should not both be occuring at the same time while $\overline{LD}$ is being asserted.

FIRST LOAD/*RETRANSMIT* ($\overline{FL}$/*RT*)

$\overline{FL}$/RT is a dual-purpose signal. It is one of three input signals which select the grouping mode in which the FIFO operates after being reset; the other two of these input signals are ***$\overline{WXI}$/WEN2*** and ***$\overline{RXI}$/REN2***. There are ***four*** possible grouping modes: standalone, ***interlocked paralleled***, cascaded 'master' or 'first-load,' and cascaded 'slave.' The designations 'master' and 'slave' pertain to IDT-compatible depth cascading. Tables 1 and 2 show the signal encodings which select each grouping mode.

In standalone or paralleled operation, the ***$\overline{FL}$/RT*** pin should be grounded for strict IDT72215B/25B-compatible operation. ***However, if it is taken HIGH, regardless of the state of the EMODE control input, the FIFO's internal read-address pointer is reset to address the FIFO's first physical memory location, without the other usual reset actions being taken; in particular, the FIFO's internal write-address pointer is unaffected. Subsequent read operations may then again read out the same block of data, delimited by the FIFO's first physical memory location and the current value of the write pointer, as was read out previously. There is no limit on the number of times that a block of data may be retransmitted. The only restrictions are that neither the read-address pointer nor the write-address pointer may 'wrap around' and address the FIFO's first physical memory location a second time during the retransmission process, and*** that the retransmit facility is unavailable during cascaded operation.

BOLD ITALIC = Enhanced Operating Mode

In IDT-compatible cascaded operation, $\overline{FL}$/***RT*** is grounded to distinguish the 'master' or 'first-load' FIFO from the other 'slave' FIFOs in the cascade, which must all have their $\overline{FL}$/***RT*** inputs HIGH during a reset operation. (See again Tables 1 and 2.) The cascade will not operate correctly either without any 'master' FIFO, or with more than one 'master' FIFO.

WRITE EXPANSION INPUT/*WRITE ENABLE 2* ($\overline{WXI}$/***WEN2***)

$\overline{WXI}$/***WEN2*** is a dual-purpose signal. It is one of three input signals which select the grouping mode in which the FIFO operates after being reset; the other two of these input signals are $\overline{FL}$/***RT*** and $\overline{RXI}$. There are ***four*** possible grouping modes: standalone, ***interlocked paralleled***, cascaded 'master' or 'first-load,' and cascaded 'slave.' The designations 'master' and 'slave' pertain to IDT-compatible depth cascading. Tables 1 and 2 show the signal encodings which select each grouping mode.

In standalone operation, $\overline{WXI}$/***WEN2*** and $\overline{RXI}$/***REN2*** both must be grounded so that the FIFO comes up in the standalone grouping mode after a reset operation. ***In interlocked paralleled operation, $\overline{WXI}$/WEN2 is tied to $\overline{FF}$ of the other paralleled FIFO, and $\overline{RXI}$/REN2 is tied to $\overline{EF}$ of that same other FIFO. This interconnection scheme ensures that both FIFOs will operate together, and remain coordinated, regardless of timing skews.***

In cascaded operation, $\overline{WXI}$/***WEN2*** is connected to the $\overline{WXO}$ (Write Expansion Output; actually $\overline{WXO}$/$\overline{HF}$) output of the previous FIFO in the cascade. $\overline{RXI}$/***REN2*** is likewise connected to the $\overline{RXO}$ (Read Expansion Output) output of that previous FIFO. A reset operation forces $\overline{WXO}$/$\overline{HF}$ and $\overline{RXO}$ HIGH for each FIFO; consequently, all FIFOs with their $\overline{WXI}$/***WEN2*** and $\overline{RXI}$/***REN2*** inputs thus connected come up in one of the two cascaded grouping modes, according to whether their $\overline{FL}$/***RT*** inputs are grounded or tied HIGH. (See again Tables 1 and 2.)

READ EXPANSION INPUT/*READ ENABLE 2* ($\overline{RXI}$/*REN2*)

$\overline{RXI}$/***REN2*** is a dual-purpose signal. It is one of three input signals which select the grouping mode in which the FIFO operates after being reset; the other two of these input signals are $\overline{FL}$/***RT*** and $\overline{WXI}$. There are *four* possible grouping modes: standalone, *interlocked paralleled*, cascaded 'master' or 'first-load,' and cascaded 'slave.' The designations 'master' and 'slave' pertain to IDT-compatible depth cascading. Tables 1 and 2 show the signal encodings which select each grouping mode.

In standalone operation, $\overline{WXI}$/***WEN2*** and $\overline{RXI}$/***REN2*** both must be grounded so that the FIFO comes up in the standalone grouping mode after a reset operation. ***In interlocked paralleled operation, $\overline{WXI}$/WEN2 is tied to $\overline{FF}$ of the other paralleled FIFO, and $\overline{RXI}$/REN2 is tied to $\overline{EF}$ of that same other FIFO. This interconnection scheme ensures that both FIFOs will operate together, and remain coordinated, regardless of timing skews.***

In cascaded operation, $\overline{RXI}$/***REN2*** is connected to $\overline{RXO}$ (Read Expansion Output) of the previous FIFO in the cascade. $\overline{WXI}$/***WEN2*** is likewise connected to $\overline{WXO}$ (Write Expansion Output; actually $\overline{WXO}$/HF) output of that previous FIFO. A reset operation forces $\overline{RXO}$ and $\overline{WXO}$/$\overline{HF}$ HIGH for each FIFO; consequently, all FIFOs with their $\overline{RXI}$/***REN2*** and $\overline{WXI}$/***WEN2*** inputs thus connected come up in one of the two IDT-compatible cascaded grouping modes, according to whether their $\overline{FL}$/***RT*** inputs are grounded or tied HIGH. (See again Tables 1 and 2.)

Data Outputs

DATA OUT ($Q_0 - Q_{17}$)

Data, programmable-flag-offset values, and *Control-Register* codes are output from the FIFO as 18-bit words on $Q_0 - Q_{17}$. Unused bit positions in offset-value words and *Control-Register* words are zero-filled.

Control/Status Outputs

FULL FLAG ($\overline{FF}$)

$\overline{FF}$ goes LOW whenever the FIFO is completely full. That is, whenever the FIFO's internal write pointer has completely caught up with its internal read pointer; so that, if another word were to be written, it would have to overwrite the unread word which is now in position for reading out by the next requested read operation. Under these conditions, the FIFO is filled to its nominal capacity, which is 512 18-bit words for the LH540215 or 1024 18-bit words for the LH540225 respectively. Write operations are inhibited whenever $\overline{FF}$ is LOW, regardless of the assertion or deassertion of Write Enable ($\overline{WEN}$).

If the FIFO has been reset by asserting $\overline{RS}$ (LOW), $\overline{FF}$ initially is HIGH. But, whenever no read operations have been performed since the completion of the reset operation, $\overline{FF}$ goes LOW after 512 write operations for the LH540215, or after 1024 write operations for the LH540225. (See Table 4.)

$\overline{FF}$ gets updated after a LOW-to-HIGH transition of the Write Clock (WCLK).

PROGRAMMABLE ALMOST-FULL FLAG ($\overline{PAF}$)

$\overline{PAF}$ goes LOW whenever the FIFO is 'almost' full; that is, whenever subtracting the value of the FIFO's internal read pointer from the value of its internal write pointer yields a difference which is less than the value of the Programmable-Almost-Full-Flag Offset 'p.' The subtraction is performed using modular arithmetic, modulo the total nominal number of 18-bit words in the FIFO's physical memory, which is 512 for the LH540215 or 1024 for the LH540225 respectively.

DESCRIPTION OF SIGNALS AND OPERATING SEQUENCES (cont'd)

The default value of 'p' after the completion of a reset operation is one-eighth of the total number of words in the FIFO-memory array, minus one: 63 for the LH540215 or 127 for the LH540225 respectively. However, 'p' may be set to any value which does not exceed this total nominal number of words for the device, as explained in the description of Load ($\overline{LD}$).

If the FIFO has been reset by asserting $\overline{RS}$ (LOW), and no read operations have been performed since the completion of the reset operation, $\overline{PAF}$ goes LOW after (512-p) write operations for the LH540215, or after (1024-p) write operations for the LH540225. (See Table 4.)

If p is still at its default value, $\overline{PAF}$ is LOW whenever the FIFO is from 7/8 full to completely full.

In the IDT-Compatible Operating Mode, $\overline{PAF}$ changes from HIGH to LOW only after a LOW-to-HIGH transition of the Write Clock WCLK, and from LOW to HIGH only after a LOW-to-HIGH transition of the Read Clock RCLK. Thus, in this operating mode, $\overline{PAF}$ behaves as an 'asynchronous flag.'

In the Enhanced Operating Mode, on the other hand, $\overline{PAF}$ gets updated only after a LOW-to-HIGH transition of the Write Clock WCLK, and thus behaves as a 'synchronous flag.' (See Table 5.) This behavior is selected whenever Control Register bit 04 is HIGH.

WRITE EXPANSION OUT/HALF-FULL FLAG ($\overline{WXO}/\overline{HF}$)

$\overline{WXO}/\overline{HF}$ is a dual-purpose signal. In 'standalone' operation, it behaves as a Half-Full Flag ($\overline{HF}$), in accordance with Table 4. In IDT-compatible 'cascaded' operation, it behaves as a Write Expansion Output ($\overline{WXO}$) signal to coordinate writing operations with the next FIFO in the cascade. Under these same conditions, also, the dual-purpose $\overline{WXI}/WEN_2$ and $\overline{RXI}/REN_2$ inputs behave as Write Expansion Input ($\overline{WXI}$) and Read Expansion Input ($\overline{RXI}$) signals respectively.

When two or more LH540215 or LH540225 FIFOs are 'cascaded' to operate as a larger 'effective FIFO,' in an IDT-style 'daisy-chain' ring configuration, the Write Expansion Input ($\overline{WXI}$) of each FIFO is connected to $\overline{WXO}$ of the previous FIFO in the ring, with $\overline{WXI}$ of the 'first-load' or 'master' FIFO being connected to $\overline{WXO}$ of the last FIFO so as to complete the ring. Similar connections are made for each FIFO in the ring, parallel to these $\overline{WXO}$-to-$\overline{WXI}$ connections, for Read Expansion Input ($\overline{RXI}$) and Read Expansion Output ($\overline{RXO}$).

When the last physical location has been written in a FIFO operating in cascaded mode, a LOW-going pulse is emitted by that FIFO on its $\overline{WXO}$ output, and it is deactivated for writing at the next valid WCLK; and the next FIFO in the ring is simultaneously activated for writing. Otherwise, $\overline{WXO}$ remains constantly HIGH whenever the FIFO is operating in cascaded mode. This LOW-going $\overline{WXO}$ pulse serves as a 'token' in the 'token-passing' FIFO-cascading scheme; it is passed on to the next FIFO in the ring via its $\overline{WXI}$ input. When this next FIFO receives the token, it is activated for writing at the next valid WCLK.

The foregoing description applies both to the 'first-load' or 'master' FIFO in the ring, and to any and all 'slave' FIFOs in the ring. However, $\overline{WXO}$ has no necessary function for FIFOs operating in the 'standalone' mode. Consequently, in that mode, the same output pin is used for $\overline{HF}$; it follows that $\overline{HF}$ is not available as an output from any FIFO which is operating in the IDT-compatible cascaded mode. A FIFO is initialized into 'cascaded master' mode, into 'cascaded slave' mode, *into interlocked paralleled mode*, or into standalone mode according to the state of its $\overline{WXI}/$***WEN_2***, $\overline{RXI}/$***REN_2***, and $\overline{FL}/$***RT*** control inputs during a reset operation, ***and of $\overline{EMODE}$***. (See Table 1, Table 2, and Table 5.)

In standalone ***or interlocked paralleled*** operation, $\overline{HF}$ goes LOW whenever the FIFO is more than half full; that is, whenever subtracting the value of the FIFO's internal read pointer from the value of its internal write pointer yields a difference which is less than half of the total nominal number of 18-bit words in the FIFO's physical memory, which is 256 for the LH540215 or 512 for the LH540225 respectively. (See Table 4.) The subtraction is performed using modular arithmetic, modulo this total nominal number of words, which is 512 for the LH540215 or 1024 for the LH540225 respectively.

If the FIFO has been reset by asserting $\overline{RS}$ (LOW), and it is operating in standalone mode ***or in interlocked paralleled*** mode, and no read operations have been performed since the completion of the reset operation, $\overline{HF}$ goes LOW after 257 write operations for the LH540215, or after 513 write operations for the LH540225. (See again Table 4.)

In the IDT-Compatible Operating Mode, $\overline{HF}$ changes from HIGH to LOW only after a LOW-to-HIGH transition of the Write Clock WCLK, and from LOW to HIGH only after a LOW-to-HIGH transition of the Read Clock RCLK. Thus, in this operating mode, $\overline{HF}$ behaves as an 'asynchronous flag.'

BOLD ITALIC = Enhanced Operating Mode

In the Enhanced Operating Mode, on the other hand, $\overline{HF}$ gets updated only after a LOW-to-HIGH transition of the Read Clock RCLK, or else after a LOW-to-HIGH transition of the Write Clock WCLK, according to the setting of bits 03 and 02 of the Control Register. (See Table 5.) Thus, in this mode $\overline{HF}$ behaves as a 'synchronous flag,' and may be synchronized either to the input side of the FIFO (i.e., to WCLK), or to the output side of the FIFO (i.e., to RCLK).

PROGRAMMABLE ALMOST-EMPTY FLAG ($\overline{PAE}$)

$\overline{PAE}$ goes LOW whenever the FIFO is 'almost empty'; that is, whenever subtracting the value of the FIFO's internal write pointer from the value of its internal read pointer yields a difference which is less than q + 1, where 'q' is the value of the Programmable-Almost-Empty-Flag Offset. The subtraction is performed using modular arithmetic, modulo the total nominal number of 18-bit words in the FIFO's physical memory, which is 512 for the LH540215 or 1024 for the LH540225 respectively.

The default value of q after the completion of a reset operation is one-eighth of the total number of words in the FIFO-memory array, minus one; 63 for the LH540215 or 127 for the LH540225 respectively. However, q may be set to any value which does not exceed this total nominal number of words for the device, as explained in the description of Load ($\overline{LD}$).

If the FIFO has been reset by asserting $\overline{RS}$ (LOW), and no write operations have been performed since the completion of the reset operation, then $\overline{PAE}$ is LOW. (See Table 4.)

If q is still at its default value, $\overline{PAE}$ is LOW whenever the FIFO is from 1/8 full to completely empty.

In the IDT-Compatible Operating Mode, $\overline{PAE}$ changes from HIGH to LOW only after a LOW-to-HIGH transition of the Read Clock RCLK, and from LOW to HIGH only after a LOW-to-HIGH transition of the Write Clock WCLK. Thus, in this operating mode, $\overline{PAE}$ behaves as an 'asynchronous flag.'

In the Enhanced Operating Mode, on the other hand, $\overline{PAE}$ gets updated only after a LOW-to-HIGH transition of the Read Clock RCLK, and thus behaves as a 'synchronous flag.' (See Table 5.) This behavior is selected whenever Control Register bit 01 is HIGH.

EMPTY FLAG ($\overline{EF}$)

$\overline{EF}$ goes LOW whenever the FIFO is completely empty. That is, whenever the FIFO's internal read pointer has completely caught up with its internal write pointer; so that, if another word were to be read out, it would have to come from the physical memory location which is now in position to be written into by the next requested write operation. Read operations are inhibited whenever $\overline{EF}$ is LOW, regardless of the assertion or deassertion of Read Enable ($\overline{REN}$).

If the FIFO has been reset by asserting $\overline{RS}$ (LOW), and no write operations have been performed since the completion of the reset operation, then $\overline{EF}$ is LOW. (See Table 4.)

$\overline{EF}$ gets updated after a LOW-to-HIGH transition of the Read Clock RCLK.

READ EXPANSION OUT/*EMPTY FLAG 2* ($\overline{RXO}$/$\overline{EF_2}$)

When two or more LH540215 or LH540225 FIFOs are operating in IDT-compatible 'cascaded' mode as a larger 'effective FIFO,' the dual-purpose $\overline{RXI}$/***REN_2*** and $\overline{WXI}$/***WEN_2*** inputs behave as Read Expansion Input ($\overline{RXI}$) and Write Expansion Input ($\overline{WXI}$) signals respectively. An IDT-style cascade of these FIFO devices has a 'daisy-chain' ring configuration; the Read Expansion Input ($\overline{RXI}$) of each FIFO is connected to $\overline{RXO}$ of the previous FIFO in the ring, with $\overline{RXI}$ of the 'first-load' or 'master' FIFO being connected to $\overline{RXO}$ of the last FIFO so as to complete the ring. Similar connections are made for each FIFO in the ring, parallel to these $\overline{RXO}$-to-$\overline{RXI}$ connections, for Write Expansion Input ($\overline{WXI}$) and Write Expansion Output ($\overline{WXO}$).

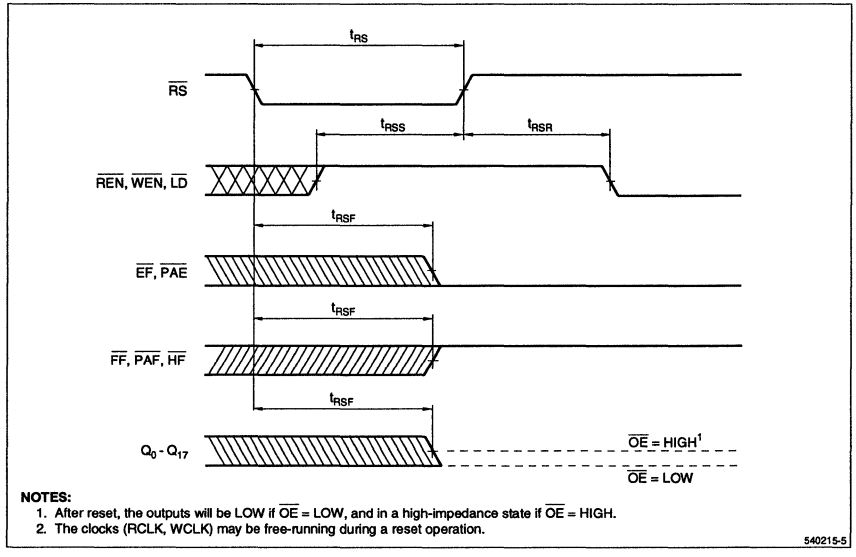
When the last physical location has been read in a FIFO operating in IDT-style cascaded mode, a LOW-going pulse is emitted by that FIFO on its $\overline{RXO}$ output; otherwise, $\overline{RXO}$ remains constantly HIGH. This LOW-going $\overline{RXO}$ pulse serves as a 'token' in the token-passing FIFO-cascading scheme; it is passed on to the next FIFO in the ring via its $\overline{RXI}$ input. When this next FIFO receives the token, it is activated for reading at the next valid RCLK.

After a FIFO emits an $\overline{RXO}$ pulse, it is deactivated for reading at the next valid RCLK; and the next FIFO in the ring is simultaneously activated for reading. Also, its data outputs go into high-Z state, regardless of the assertion or deassertion of its Output Enable ($\overline{OE}$) control input, until it again receives the token.

The foregoing description applies both to the 'first-load' or 'master' FIFO in the ring, and to any and all 'slave' FIFOs in the ring. However, $\overline{RXO}$ has no necessary function for a FIFO which is operating in 'standalone' mode. Consequently, in that mode, $\overline{RXO}$ is never asserted, and remains constantly HIGH. A FIFO is initialized into 'standalone' mode, into 'cascaded master' mode, or into 'cascaded slave' mode according to the state of its $\overline{WXI}$/***WEN_2***, $\overline{RXI}$/***REN_2***, and $\overline{FL}$/***RT*** control inputs during a reset operation. ***It also may be forced into interlocked paralleled mode by $\overline{EMODE}$. (See Table 1, Table 2, and Table 5.)***

BOLD ITALIC = Enhanced Operating Mode

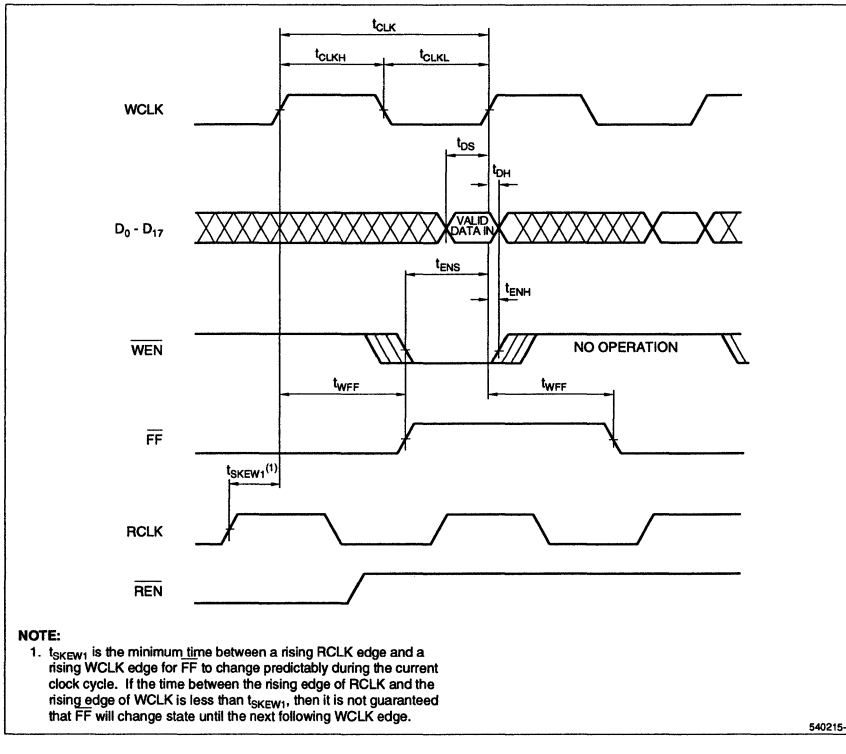
TIMING DIAGRAMS



NOTES:
1. After reset, the outputs will be LOW if $\overline{OE}$ = LOW, and in a high-impedance state if $\overline{OE}$ = HIGH.
2. The clocks (RCLK, WCLK) may be free-running during a reset operation.

540215-5

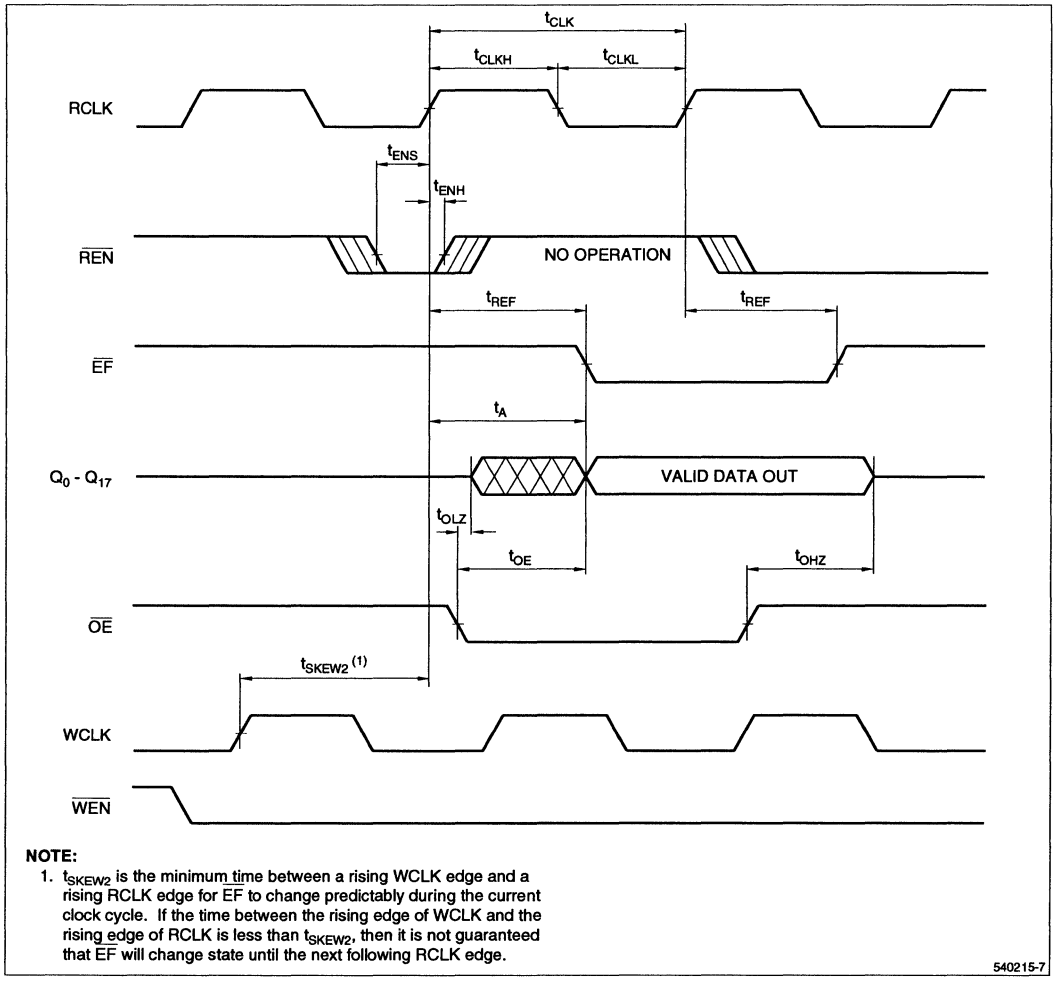
Figure 5. Reset Timing



NOTE:
1. t_{SKEW1} is the minimum time between a rising RCLK edge and a rising WCLK edge for $\overline{FF}$ to change predictably during the current clock cycle. If the time between the rising edge of RCLK and the rising edge of WCLK is less than t_{SKEW1}, then it is not guaranteed that $\overline{FF}$ will change state until the next following WCLK edge.

540215-6

Figure 6. Synchronous Write Operation



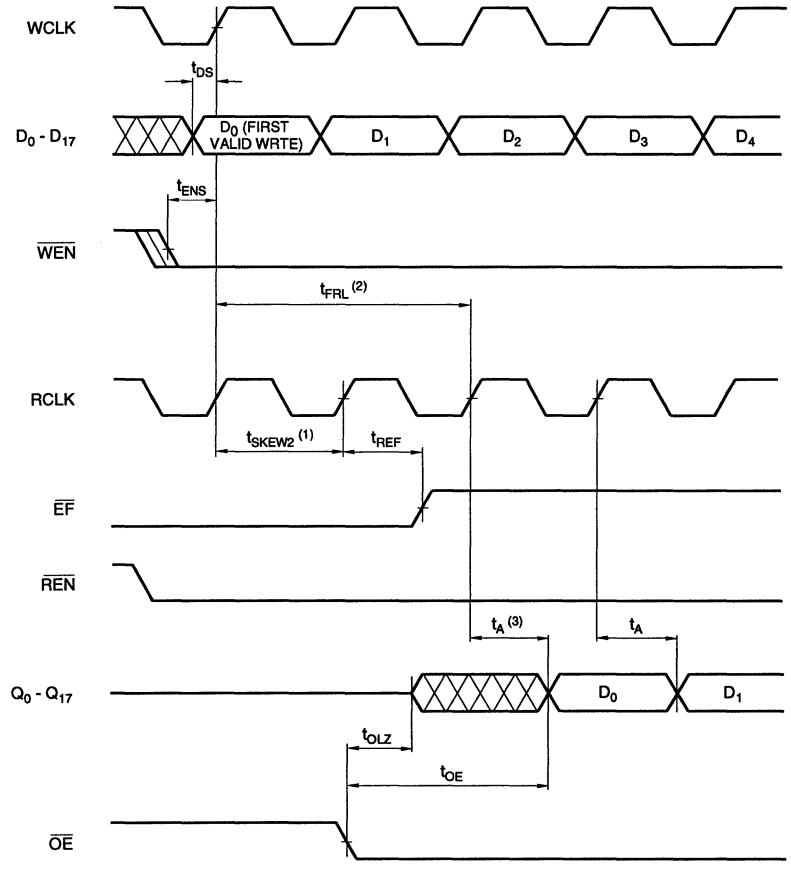
NOTE:

1. t_{SKEW2} is the minimum time between a rising WCLK edge and a rising RCLK edge for $\overline{EF}$ to change predictably during the current clock cycle. If the time between the rising edge of WCLK and the rising edge of RCLK is less than t_{SKEW2}, then it is not guaranteed that $\overline{EF}$ will change state until the next following RCLK edge.

540215-7

Figure 7. Synchronous Read Operation

TIMING DIAGRAMS (cont'd)



NOTES:

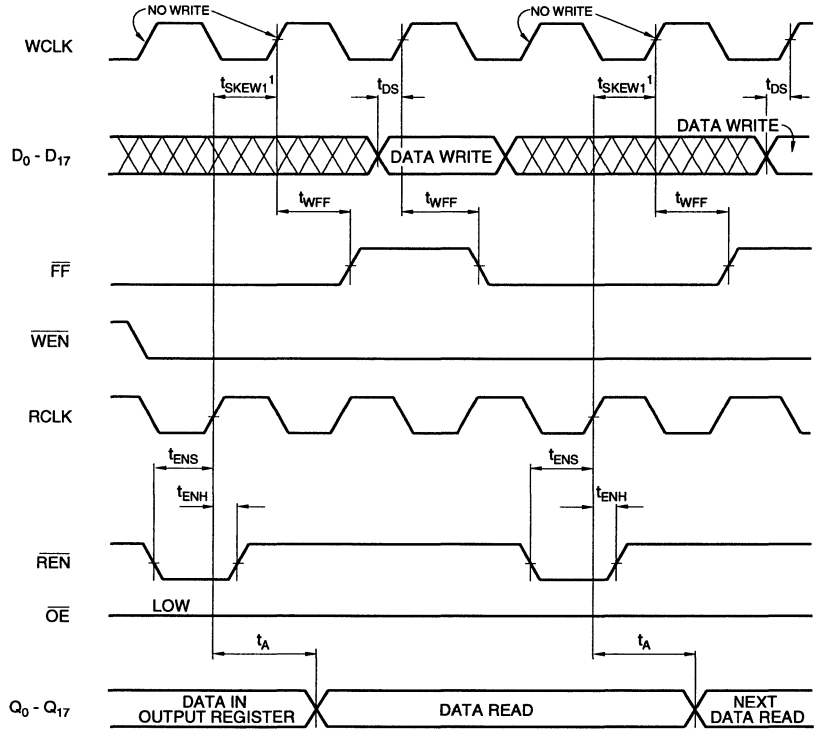
1. t_{SKEW2} is the minimum time between a rising RCLK edge and a rising WCLK edge for FF to change predictably during the current clock cycle. If the time between the rising edge of RCLK and the rising edge of WCLK is less than t_{SKEW2}, then it is not guaranteed that FF will change state until the next following WCLK edge.

2. t_{FRL} (First-Read Latency) is the minimum time between a rising WCLK edge and a rising RCLK edge to assure a correct readout of the first data word D_0 in response to the next RCLK edge. Thus, $t_{FRL} = t_{CLK} + t_{SKEW2}$. If t_{FRL} is not met, D_0 may be available either at $t_{CLK} + t_{SKEW2}$, or after one more clock cycle delay at $2\ t_{CLK} + t_{SKEW2}$. The First-Read Latency timing restrictions apply only when the FIFO has been empty ($\overline{EF}$ = LOW).

3. $\overline{EF}$ may be used to determine when the first data word D_0 may be read. D_0 always is available on the next cycle after $\overline{EF}$ has gone HIGH.

540215-8

Figure 8. Latency for the First Data Word After a Reset Operation, With Simultaneous Read and Write



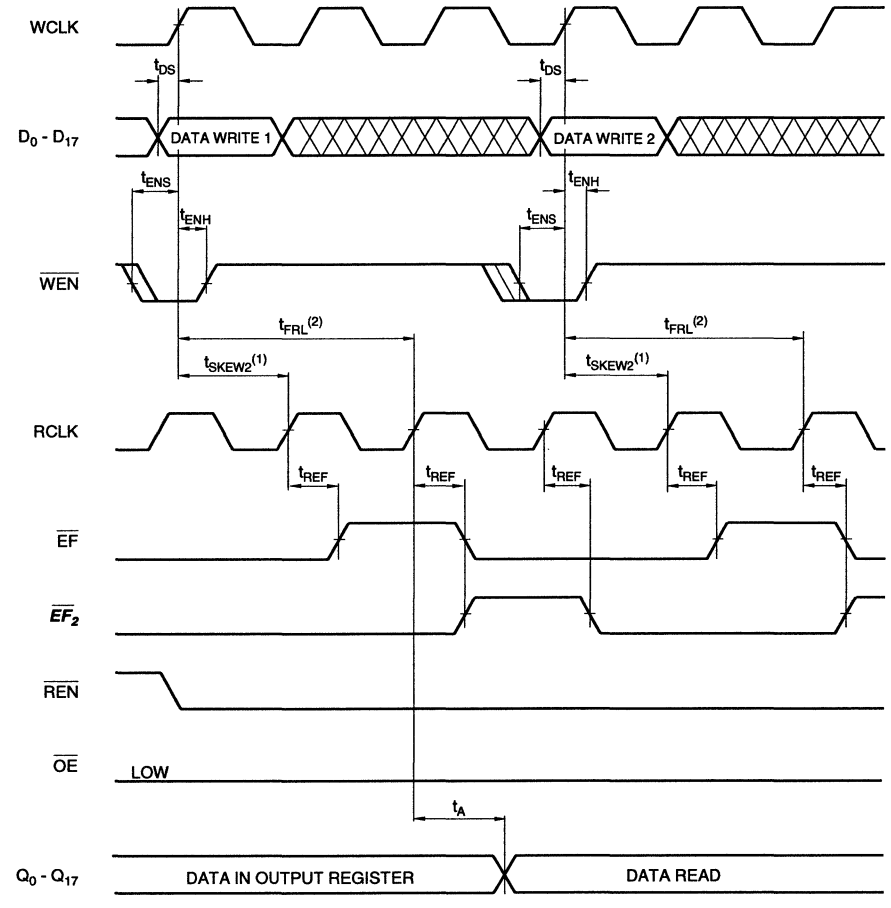
NOTE:

1. t_{SKEW1} is the minimum time between a rising RCLK edge and a rising WCLK edge for FF to change predictably during the current clock cycle. If the time between the rising edge of RCLK and the rising edge of WCLK is less than t_{SKEW1}, then it is not guaranteed that FF will change state until the next following WCLK edge.

540215-9

Figure 9. Full-Flag Timing

TIMING DIAGRAMS (cont'd)



NOTES:

1. t_{SKEW2} is the minimum time between a rising WCLK edge and a rising RCLK edge for $\overline{EF}$ to change predictably during the current clock cycle. If the time between the rising edge of WCLK and the rising edge of RCLK is less than t_{SKEW2}, then it is not guaranteed that $\overline{EF}$ will change state until the next following RCLK edge.

2. t_{FRL} (First-Read Latency) is the minimum time between a rising WCLK edge and a rising RCLK edge to assure a correct readout of the first data word D_0 in response to the next RCLK edge. Thus, $t_{FRL} = t_{CLK} + t_{SKEW2}$. If t_{FRL} is not met, D_0 may be available either at $t_{CLK} + t_{SKEW2}$, or after one more clock cycle delay at 2 $t_{CLK} + t_{SKEW2}$. The First-Read Latency timing restrictions apply only when the FIFO has been empty ($\overline{EF}$ = LOW).

3. $\overline{EF}$ may be used to determine when the first data word D_0 may be read. D_0 always is available on the next cycle after $\overline{EF}$ has gone HIGH.

BOLD ITALIC = Enhanced Operating Mode.

540215-10

Figure 10. Empty-Flag Timing

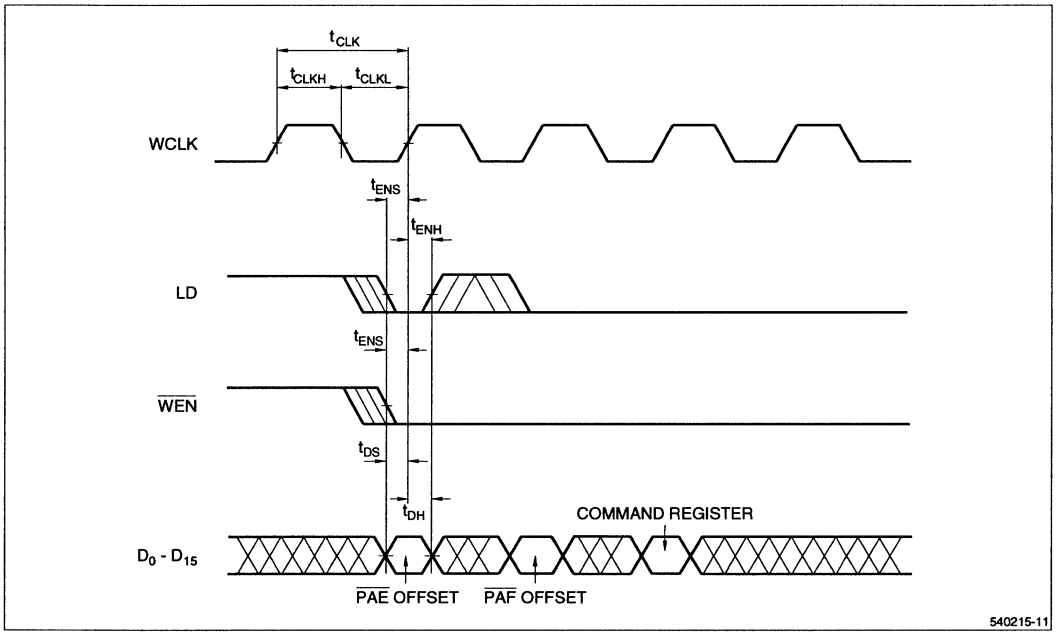


Figure 11. Programmable-Register Write Operation

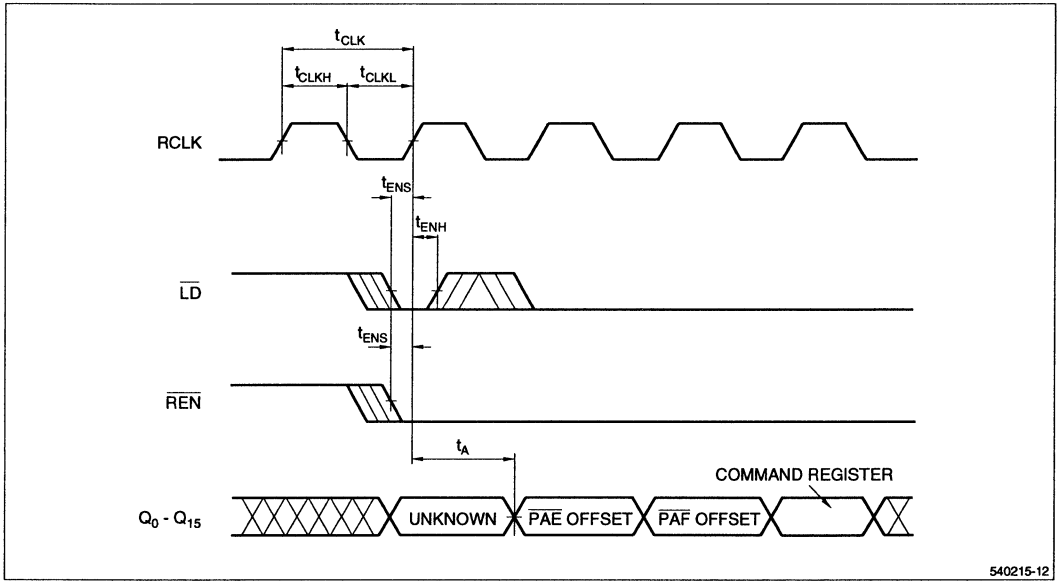


Figure 12. Programmable-Register Read Operation

TIMING DIAGRAMS (cont'd)

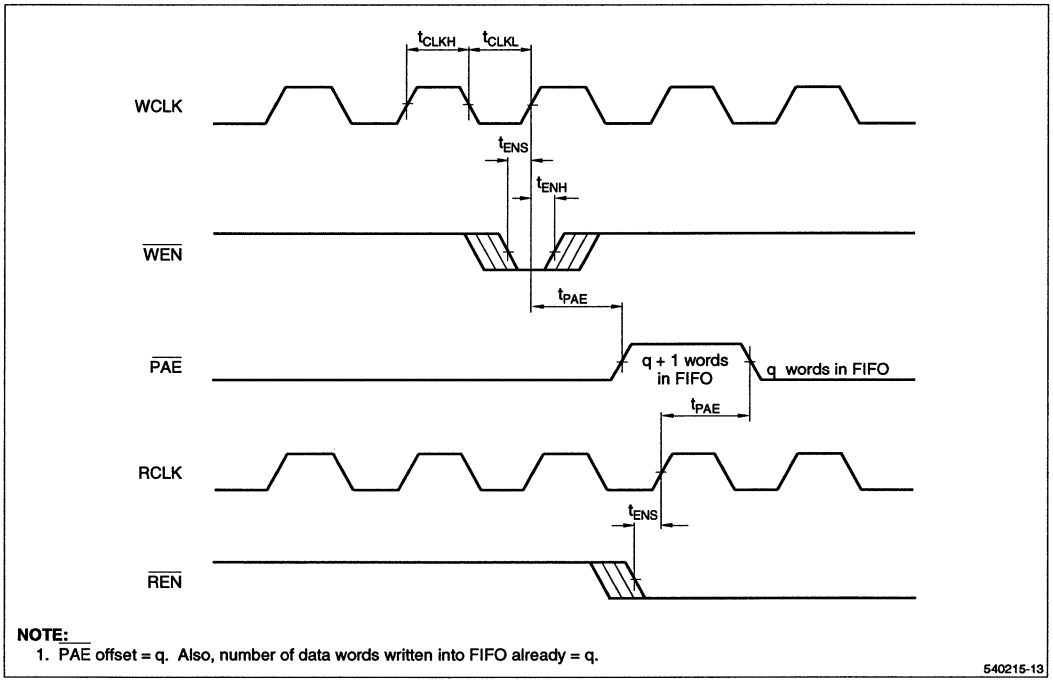
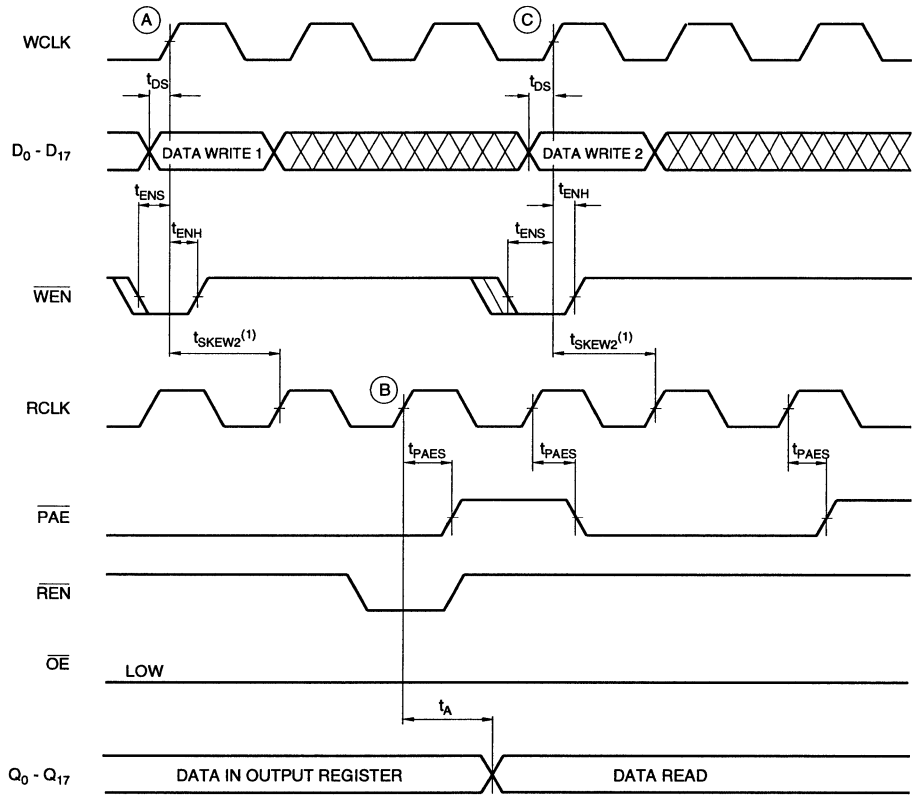


Figure 13. Programmable-Almost-Empty Flag Timing, IDT-Compatible Operating Mode

Enhanced Operating Mode Timing Diagram



NOTES:

1. t_{SKEW2} is the minimum time between a rising WCLK edge and a rising RCLK edge for PAE to change predictably during the current clock cycle. If the time between the rising edge of WCLK and the rising edge of RCLK is less than t_{SKEW2}, then it is not guaranteed that PAE will change state until the next following RCLK edge.
2. PAE offset = q. Also, number of data words written into FIFO already = q.
3. The internal state of the FIFO:

   At (A), q+1 words.

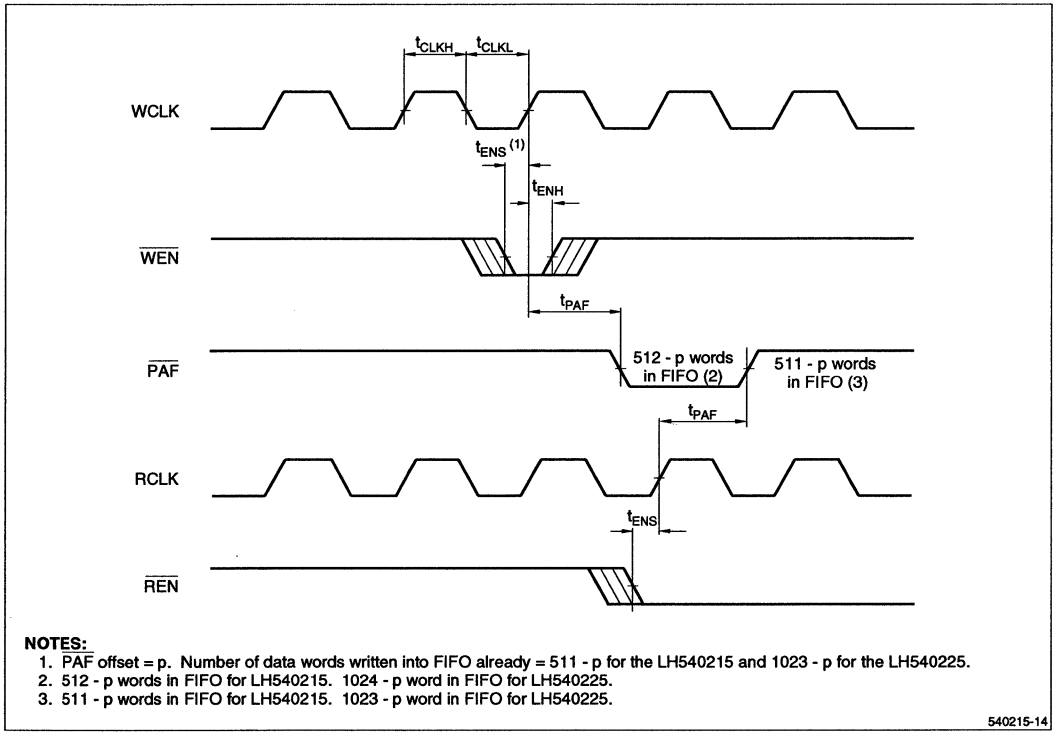
   At (B), q words.

   At (C), q+1 words again.

540215-23

Figure 14. Programmable-Almost-Empty Flag Timing, When Synchronous (Enhanced Operating Mode)

TIMING DIAGRAMS (cont'd)

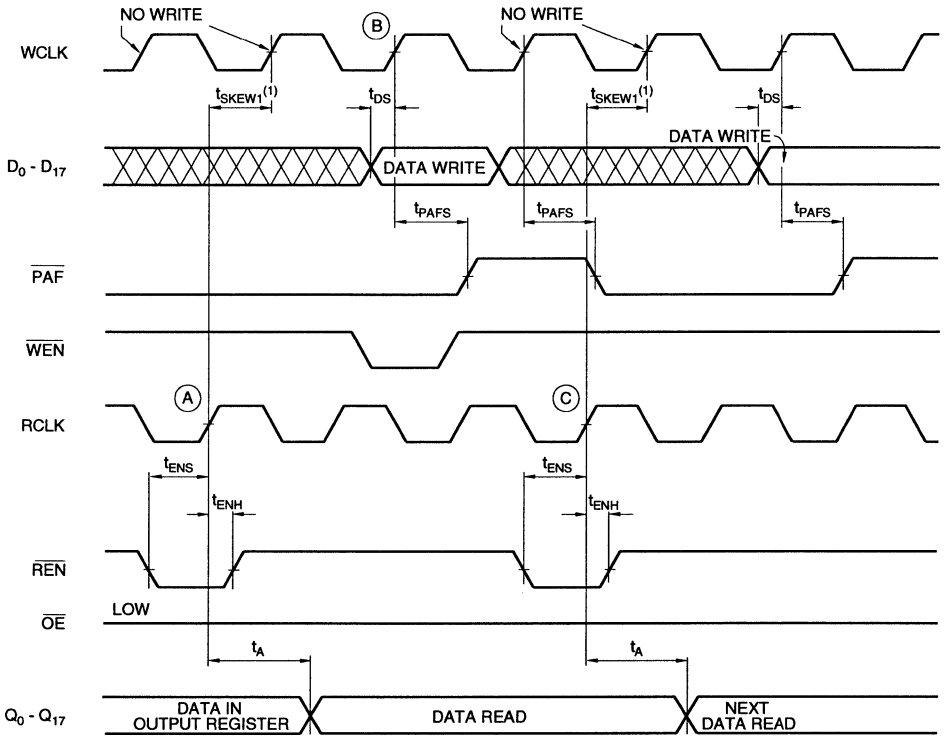


NOTES:
1. $\overline{PAF}$ offset = p. Number of data words written into FIFO already = 511 - p for the LH540215 and 1023 - p for the LH540225.
2. 512 - p words in FIFO for LH540215. 1024 - p word in FIFO for LH540225.
3. 511 - p words in FIFO for LH540215. 1023 - p word in FIFO for LH540225.

540215-14

Figure 15. Programmable Almost-Full-Flag Timing, IDT-Compatible Operating Mode

Enhanced Operating Mode Timing Diagram



NOTES:

1. t_{SKEW1} is the minimum time between a rising RCLK edge and a rising WCLK edge for PAF to change predictably during the current clock cycle. If the time between the rising edge of RCLK and the rising edge of WCLK is less than t_{SKEW1}, then it is not guaranteed that PAF will change state until the next following WCLK edge.
2. PAF offset = p. Number of data words written into FIFO already = 511 - p for the LH540215 and 1023 - p for the LH540225.
3. 512 - p words in FIFO for LH540215. 1024 - p word in FIFO for LH540225.
4. 511 - p words in FIFO for LH540215. 1023 - p word in FIFO for LH540225.
5. The internal state of the FIFO:

   At (A), 511-p words.

   At (B), 512-p words.

   At (C), 511-p words again.

540215-24

Figure 16. Programmable-Almost-Full-Flag Timing, When Synchronous (Enhanced Operating Mode)

TIMING DIAGRAMS (cont'd)

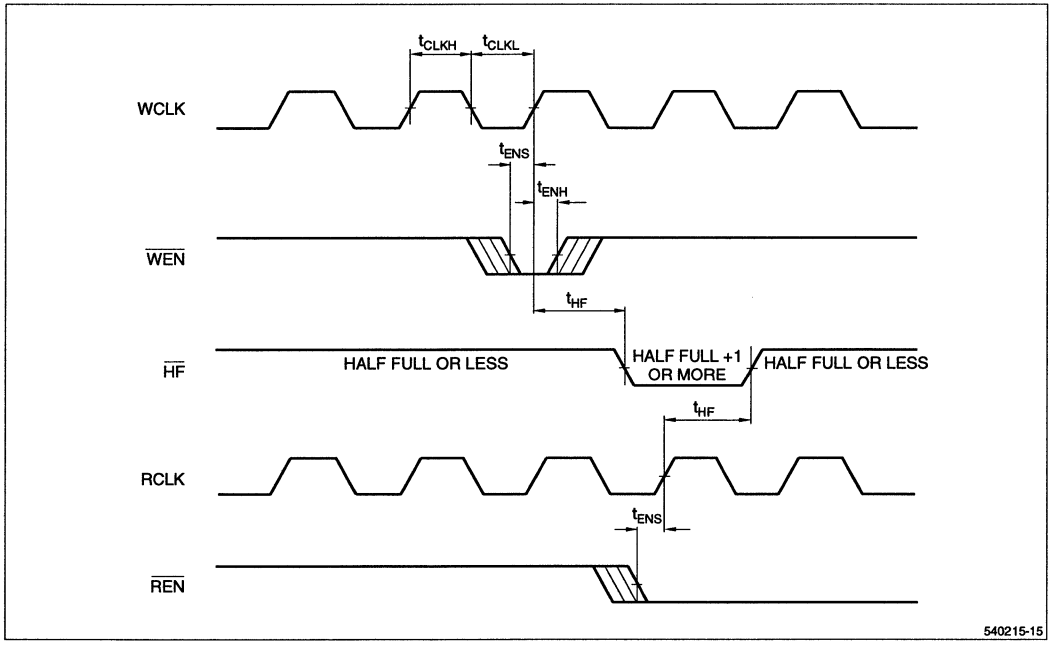
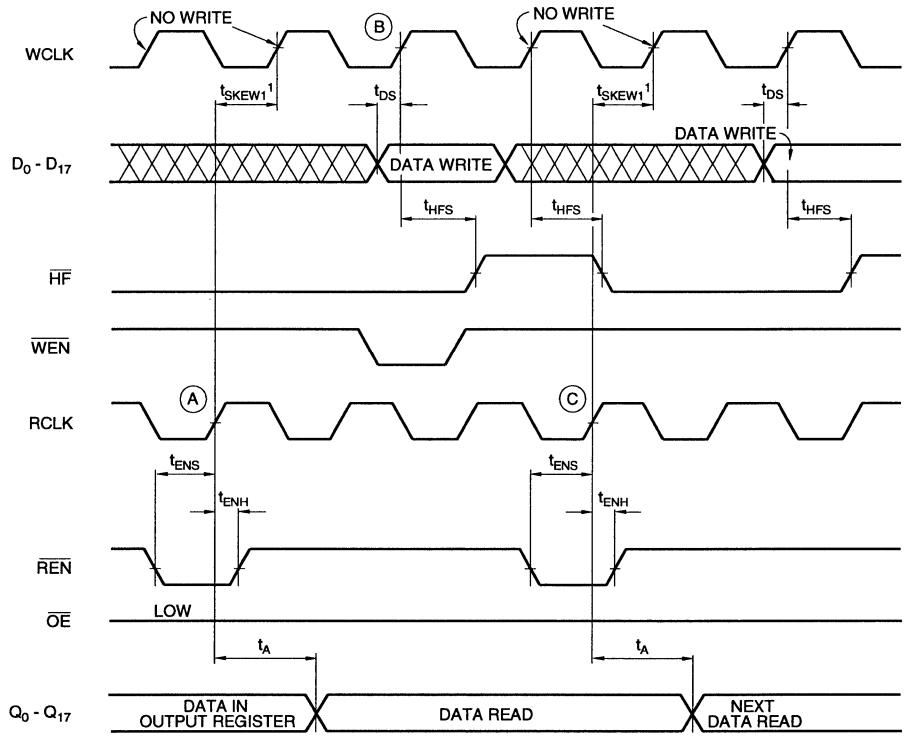


Figure 17. Half-Full-Flag Timing, IDT-Compatible Operating Mode

Enhanced Operating Mode Timing Diagram



NOTES:

1. t_{SKEW1} is the minimum time between a rising RCLK edge and a rising WCLK edge for $\overline{HF}$ to change predictably during the current clock cycle. If the time between the rising edge of RCLK and the rising edge of WCLK is less than t_{SKEW1}, then it is not guaranteed that $\overline{HF}$ will change state until the next following WCLK edge.

2. The internal state of the FIFO:

   At (A), exactly half full.

   At (B), half+1 words.

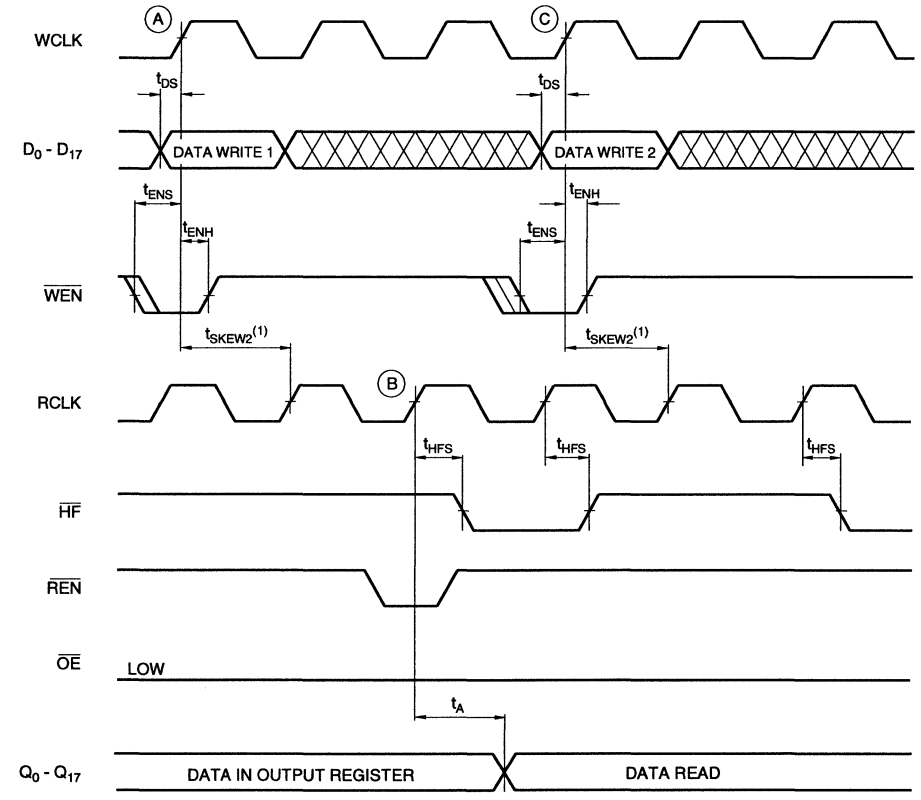
   At (C), exactly half full again.

540215-25

Figure 18. Half-Full-Flag Timing, When Synchronized to Input Port (Enhanced Operating Mode)

TIMING DIAGRAMS (cont'd)

Enhanced Operating Mode Timing Diagram



NOTE:

1. t_{SKEW2} is the minimum time between a rising WCLK edge and a rising RCLK edge for $\overline{HF}$ to change predictably during the current clock cycle. If the time between the rising edge of WCLK and the rising edge of RCLK is less than t_{SKEW2}, then it is not guaranteed that $\overline{HF}$ will change state until the next following RCLK edge.
2. The internal state of the FIFO:

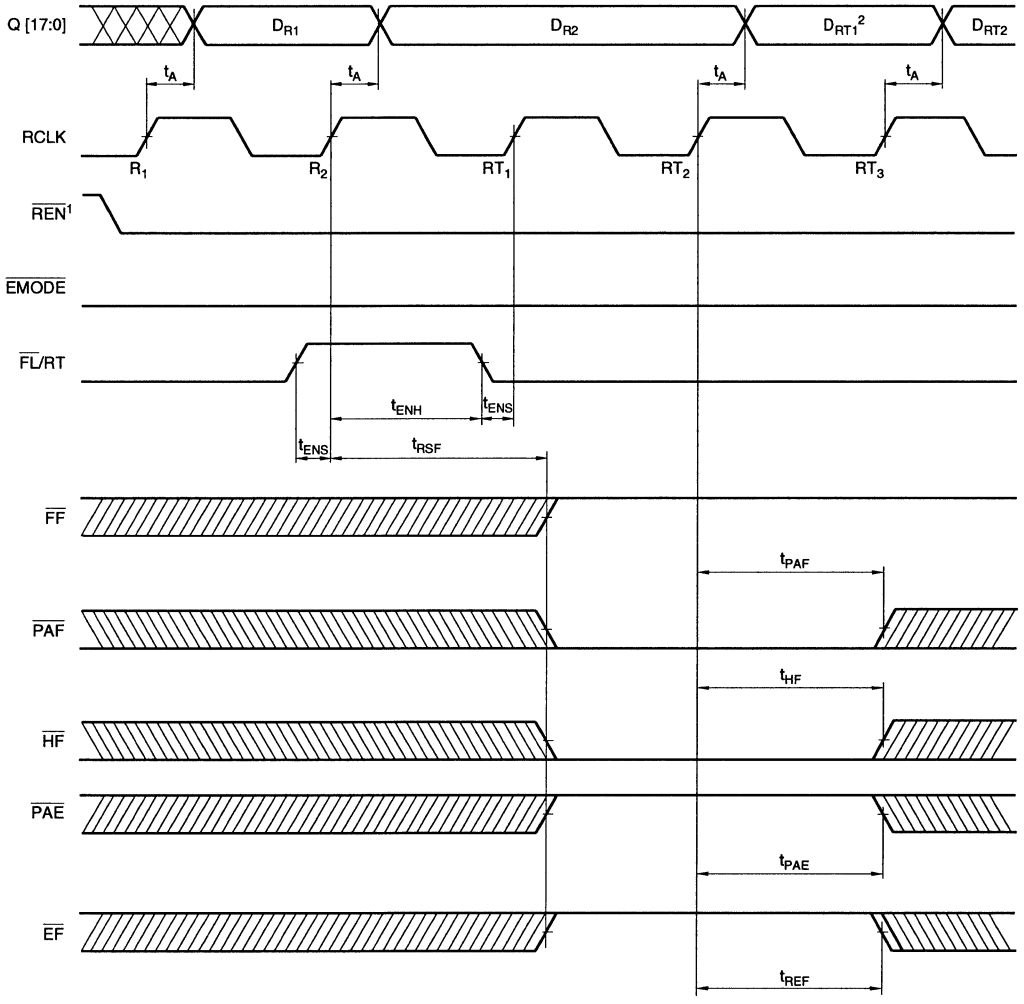
   At (A), half+1 words.

   At (B), exactly half full.

   At (C), half+1 words again.

540215-26

Figure 19. Half-Full-Flag Timing, When Synchronized to Output Port (Enhanced Operating Mode)



NOTES:

1. In IDT-compatible operating mode, $\overline{REN}$ = LOW; in Enhanced Operating Mode, also REN_2 = HIGH (and $\overline{OE}$ = LOW, if Control Register bit 05 = HIGH). In any case, $\overline{LD}$ = HIGH.
2. D_{RT1} is the data item in physical location zero of the FIFO memory array.
3. The asynchronous intermediate flags (corresponding to LOW Control-Register bits) will show correct status two or more RCLK cycles after a retransmit operation. (RT_2, in the above RCLK waveform.)
4. The synchronous intermediate flags (corresponding to HIGH Control-Register bits) will show correct status three or more RCLK cycles after a retransmit operation. (RT_3, in the above RCLK waveform.)
5. Immediately after a reset operation, before any write operations have taken place, a retransmit operation is a 'no-op', and does not change the state of any FIFO registers or flags.

540215-28

Figure 20. Retransmit Timing, IDT-Compatible Operating Mode

TIMING DIAGRAMS (cont'd)

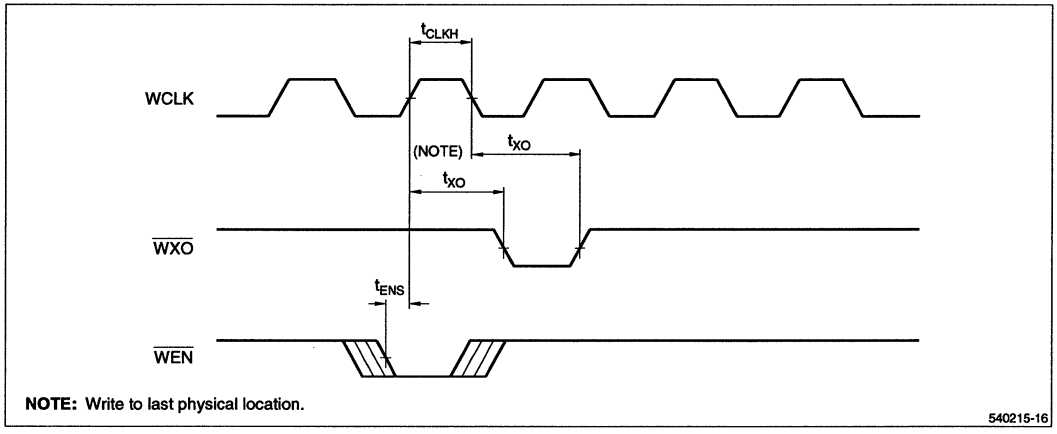


Figure 21. Write-Expansion-Out Timing, IDT-Compatible Operating Mode

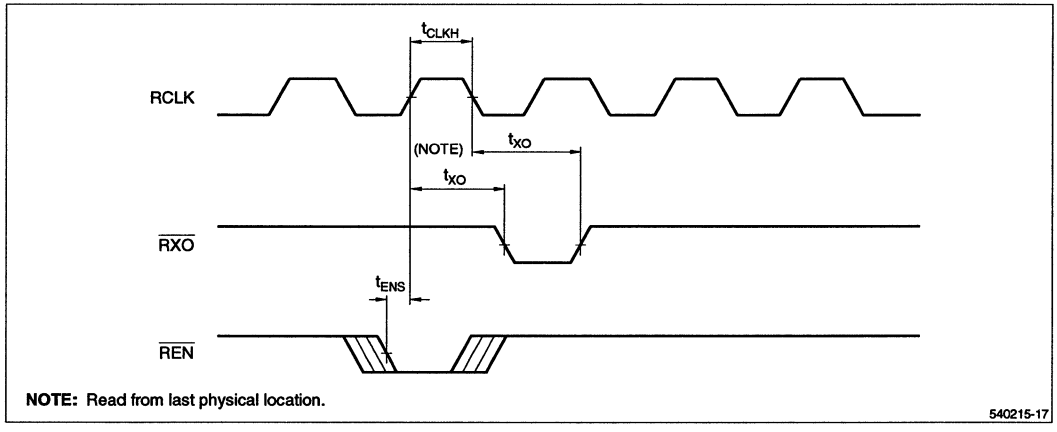


Figure 22. Read-Expansion-Out Timing, IDT-Compatible Operating Mode

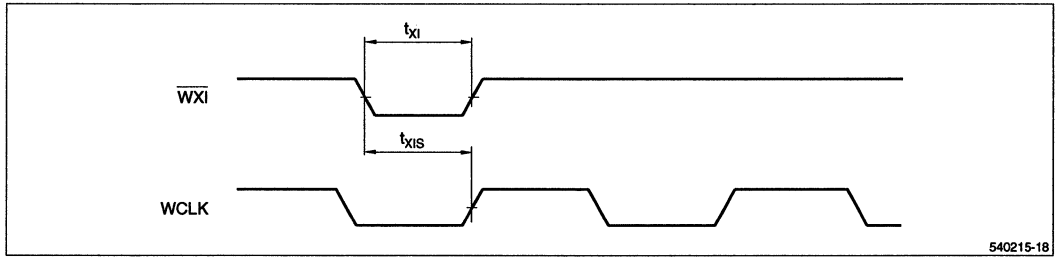


Figure 23. Write-Expansion-In Timing, IDT-Compatible Operating Mode

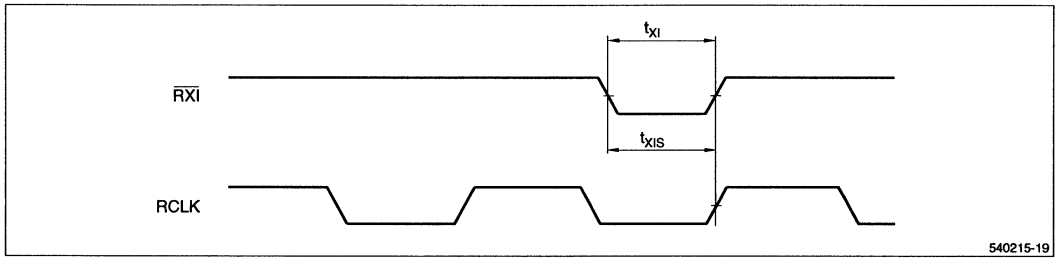


Figure 24. Read-Expansion-In Timing, IDT-Compatible Operating Mode

APPLICATIONS INFORMATION

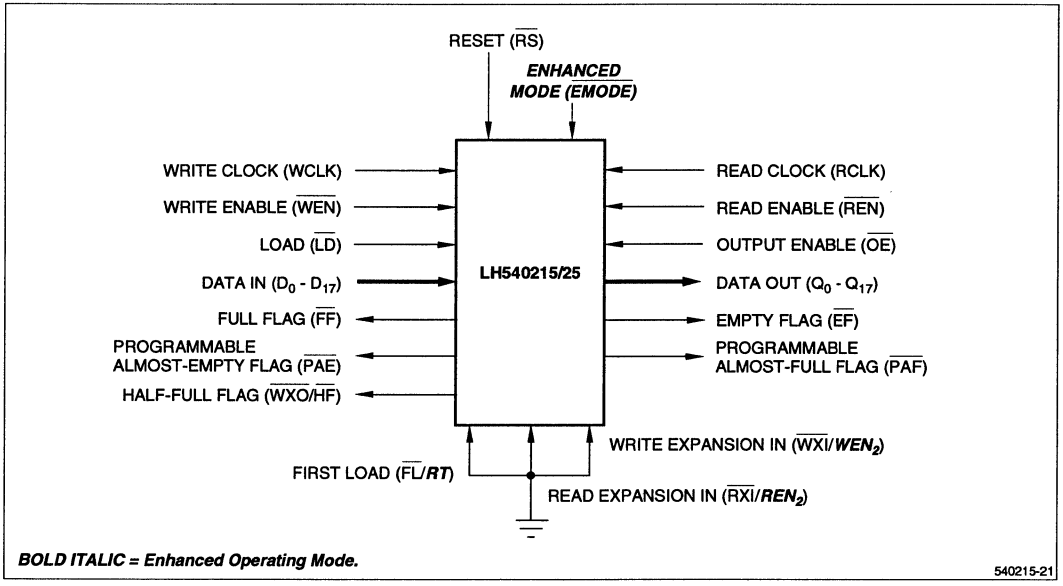


Figure 25. Standalone FIFO (512 × 18 / 1024 × 18)

APPLICATIONS INFORMATION (cont'd)

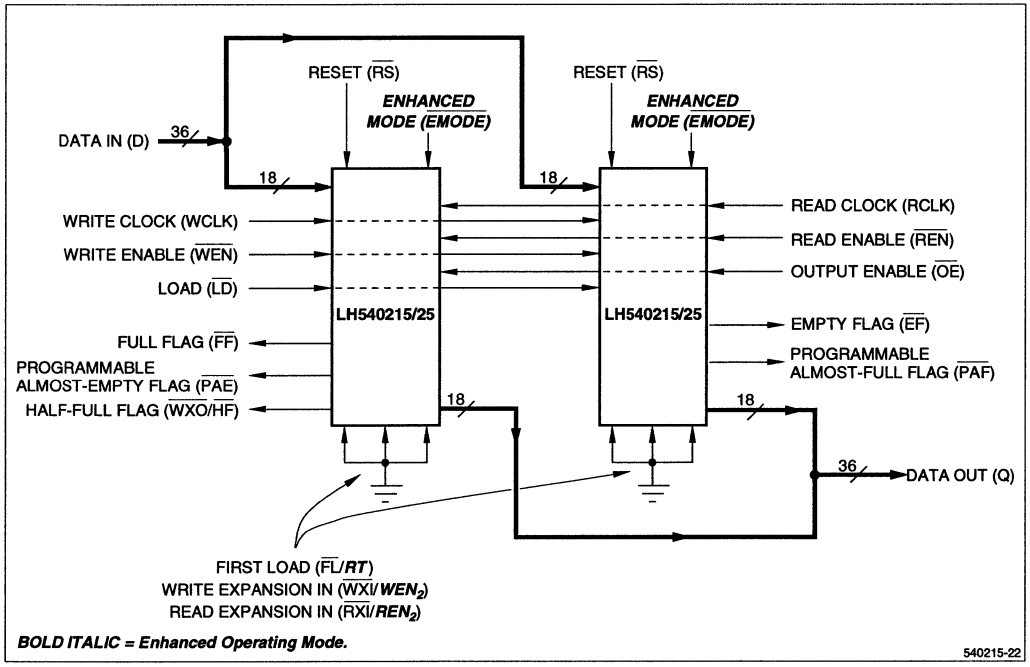


Figure 26. FIFO Word-Width Expansion, IDT-Compatible Operating Mode (512 × 36 / 1024 × 36)

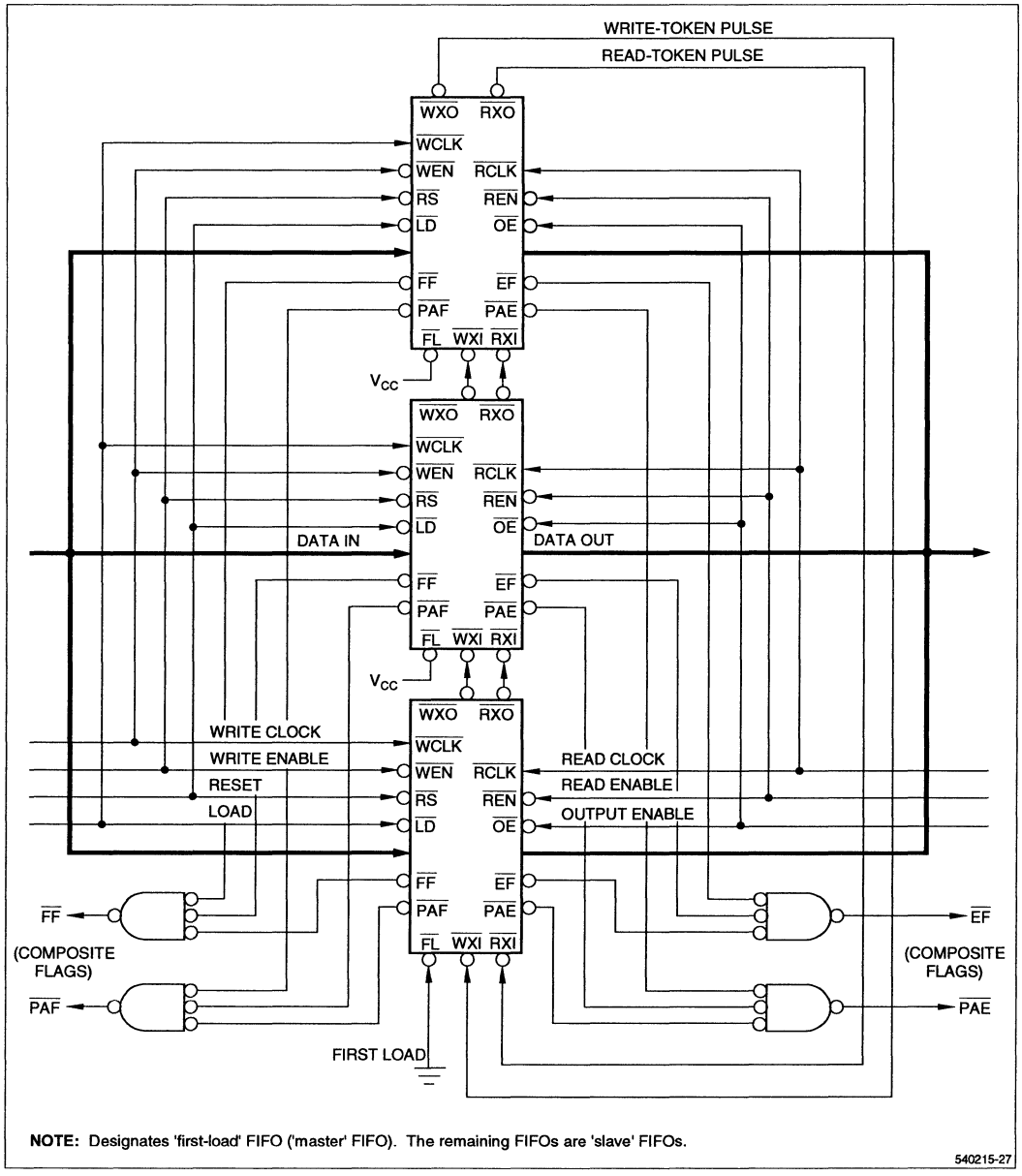
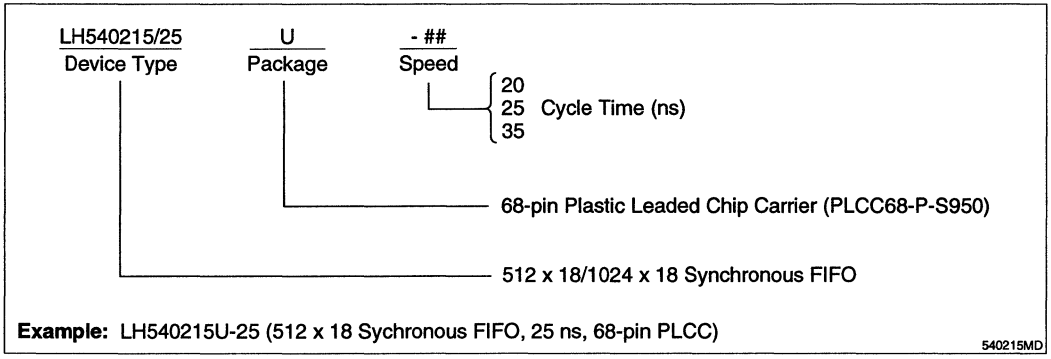


Figure 27. Synchronous FIFO Depth Cascading Using IDT-Compatible 'Token-Passing' Scheme

ORDERING INFORMATION



LH543601/11

PRODUCT PREVIEW

256 × 36 × 2 / 512 × 36 × 2 BiFIFOs

FEATURES

- Fast Cycle Times: 15/20/25/30/35 ns
- Pin-Compatible and Functionally-Compatible 0.8μ-Technology Replacements for Sharp LH5420
- Two 256 × 36-bit/512 × 36-bit FIFO Buffers
- Full 36-bit Word Width
- Selectable 36/18/9-bit Word Width on Port B
- Independently-Synchronized ('Fully-Asynchronous') Operation of Port A and Port B
- 'Synchronous' Enable-Plus-Clock Control at Both Ports
- R/$\overline{W}$, Enable, Request, and Address Control Inputs are Sampled on the Rising Clock Edge
- Synchronous Request/Acknowledge 'Handshake' Capability; Use is Optional
- Device Comes Up Into a Known Default State at Reset; Programming is Allowed, but is not Required
- Asynchronous Output Enables
- Five Status Flags per Port: Full, Almost-Full, Half-Full, Almost-Empty, and Empty
- Almost-Full Flag and Almost-Empty Flag are Programmable
- Mailbox Registers with Synchronized Flags
- Data-Bypass Function
- Data-Retransmit Function
- Automatic Byte Parity Checking
- 16 mA-I_{OL} Three-State Outputs; TTL/CMOS-Compatible I/O
- Space-Saving PQFP and PGA Packages

FUNCTIONAL DESCRIPTION

The LH543601/11 contain two FIFO buffers, FIFO #1 and FIFO #2. These operate in parallel, but in opposite directions, for bidirectional data buffering. FIFO #1 and FIFO #2 each are organized as 256 or 512 words by 36 bits. The LH543601/11 are ideal either for wide unidirectional applications or for bidirectional data applications; component count and board area are reduced.

The LH543601/11 have two 36-bit ports, Port A and Port B. Each port has its own port-synchronous clock, but the two ports may operate asynchronously relative to each other. Data flow is initiated at a port by the rising edge of the appropriate clock; it is gated by the corresponding edge-sampled enable, request, and read/write control signals. At the maximum operating frequency, the clock duty cycle may vary from 40% to 60%. At lower frequencies, the clock waveform may be quite asymmetric, as long as the minimum pulse-width conditions for clock-HIGH and clock-LOW remain satisfied; the LH543601/11 are fully-static parts.

Conceptually, the port clocks CK_A and CK_B are free-running, periodic 'clock' waveforms, used to control other signals which are edge-sensitive. However, there actually is not any absolute requirement that these 'clock' waveforms *must* be periodic. An 'asynchronous' mode of operation is possible, in one or both directions, independently, if the appropriate enable and request inputs are continuously asserted, and enough aperiodic 'clock' pulses of suitable duration are generated by external logic to cause all necessary actions to occur.

A synchronous request/acknowledge handshake facility is provided at each port for FIFO data access. This request/ acknowledge handshake resolves FIFO full and empty boundary conditions, when the two ports are operated asynchronously relative to each other.

FIFO status flags monitor the extent to which each FIFO buffer has been filled. Full, Almost-Full, Half-Full, Almost-Empty, and Empty flags are included for *each* FIFO. The Almost-Full and Almost-Empty flags are programmable over the entire FIFO depth, but are automatically initialized to eight locations from the respective FIFO boundaries at reset. A data block of 256 (LH543601) or 512 (LH543611) or fewer words may be retransmitted any desired number of times.

FUNCTIONAL DESCRIPTION (cont'd)

Two mailbox registers provide a separate path for passing control words or status words between ports. Each mailbox has a New-Mail-Alert Flag, which is synchronized to the reading port's clock. This mailbox function facilitates the synchronization of data transfers between asynchronous systems.

Data-bypass mode allows Port A to directly transfer data to or from Port B at reset. In this mode, the device acts as a registered transceiver under the control of Port A. For instance, a master processor on Port A can use the data bypass feature to send or receive initialization or configuration information directly, to or from a peripheral device on Port B, during system startup.

A word-width-select option is provided on Port B for 36-bit, 18-bit, or 9-bit data access. This feature allows word-width matching between Port A and Port B, with no additional logic needed. It also ensures maximum utilization of bus bandwidths.

A Byte Parity Check Flag at each port monitors data integrity. Control-Register bit 00 selects the parity mode, odd or even. This bit is initialized for odd data parity at reset; but it may be reprogrammed for even parity, or back again to odd parity, as desired.

PIN CONNECTIONS

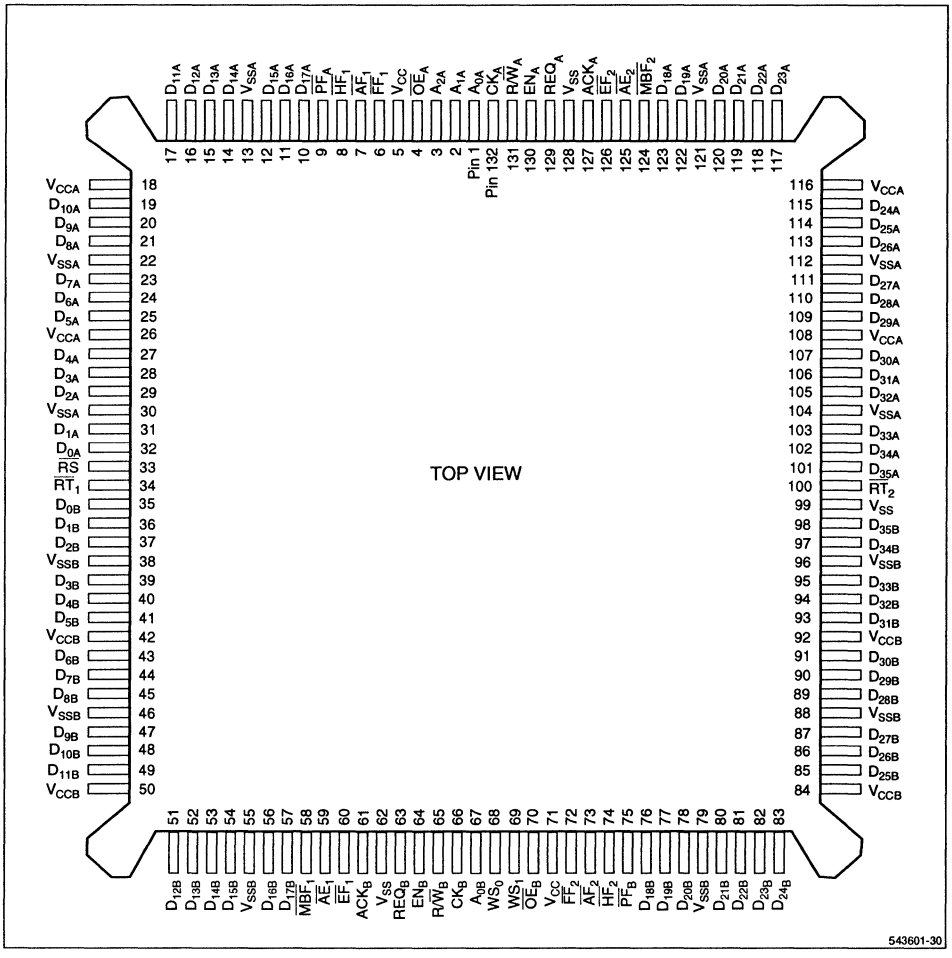


Figure 1. Pin Connections for 132-Pin Quad Flat Package (Top View)

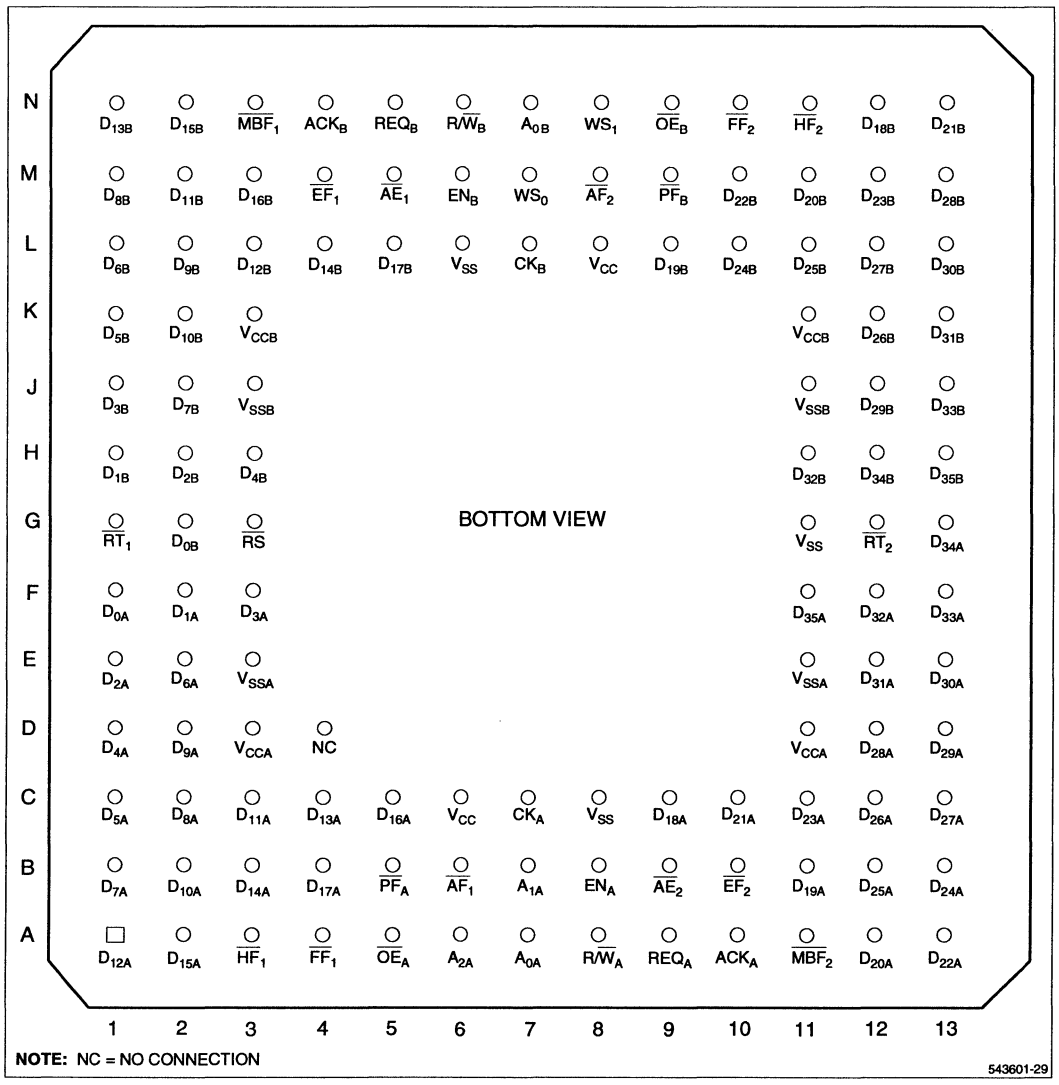
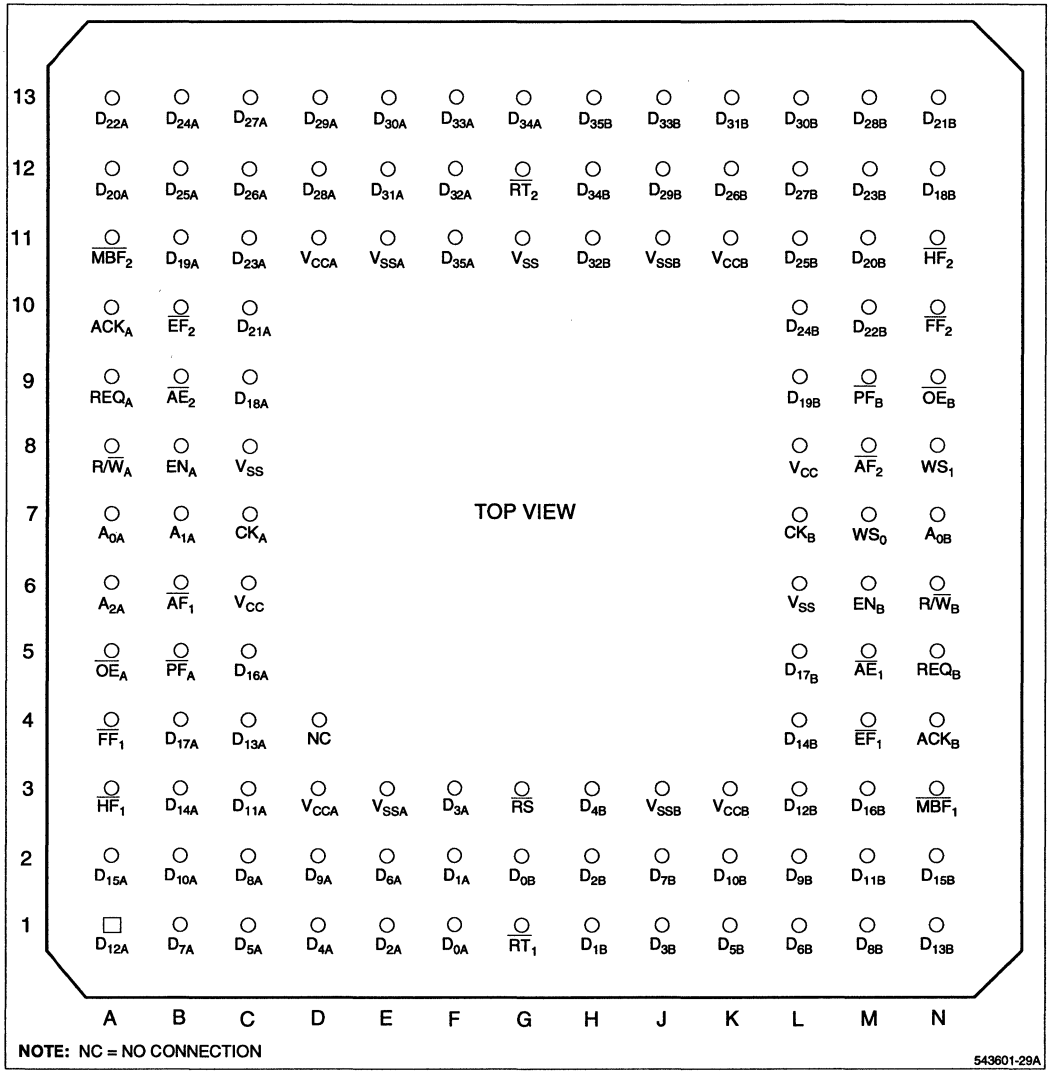


Figure 2. Pin Connections for 120-Pin PGA Package (Bottom View)



NOTE: NC = NO CONNECTION

543601-29A

Figure 3. Pin Connections for 120-Pin PGA Package (Top View)

PIN LIST

SIGNAL NAME	PQFP PIN NO.	PGA PIN NO.
A_{0A}	1	A7
A_{1A}	2	B7
A_{2A}	3	A6
$\overline{OE}_A$	4	A5
$\overline{FF}_1$	6	A4
$\overline{AF}_1$	7	B6
$\overline{HF}_1$	8	A3
$\overline{PF}_A$	9	B5
D_{17A}	10	B4
D_{16A}	11	C5
D_{15A}	12	A2
D_{14A}	14	B3
D_{13A}	15	C4
D_{12A}	16	A1
D_{11A}	17	C3
D_{10A}	19	B2
D_{9A}	20	D2
D_{8A}	21	C2
D_{7A}	23	B1
D_{6A}	24	E2
D_{5A}	25	C1
D_{4A}	27	D1
D_{3A}	28	F3
D_{2A}	29	E1
D_{1A}	31	F2
D_{0A}	32	F1
$\overline{RS}$	33	G3
$\overline{RT}_1$	34	G1
D_{0B}	35	G2
D_{1B}	36	H1
D_{2B}	37	H2
D_{3B}	39	J1
D_{4B}	40	H3
D_{5B}	41	K1
D_{6B}	43	L1
D_{7B}	44	J2
D_{8B}	45	M1
D_{9B}	47	L2
D_{10B}	48	K2
D_{11B}	49	M2
D_{12B}	51	L3
D_{13B}	52	N1
D_{14B}	53	L4
D_{15B}	54	N2

SIGNAL NAME	PQFP PIN NO.	PGA PIN NO.
D_{16B}	56	M3
D_{17B}	57	L5
$\overline{MBF}_1$	58	N3
$\overline{AE}_1$	59	M5
$\overline{EF}_1$	60	M4
ACK_B	61	N4
REQ_B	63	N5
EN_B	64	M6
$R/\overline{W}_B$	65	N6
CK_B	66	L7
A_{0B}	67	N7
WS_0	68	M7
WS_1	69	N8
$\overline{OE}_B$	70	N9
$\overline{FF}_2$	72	N10
$\overline{AF}_2$	73	M8
$\overline{HF}_2$	74	N11
$\overline{PF}_B$	75	M9
D_{18B}	76	N12
D_{19B}	77	L9
D_{20B}	78	M11
D_{21B}	80	N13
D_{22B}	81	M10
D_{23B}	82	M12
D_{24B}	83	L10
D_{25B}	85	L11
D_{26B}	86	K12
D_{27B}	87	L12
D_{28B}	89	M13
D_{29B}	90	J12
D_{30B}	91	L13
D_{31B}	93	K13
D_{32B}	94	H11
D_{33B}	95	J13
D_{34B}	97	H12
D_{35B}	98	H13
$\overline{RT}_2$	100	G12
D_{35A}	101	F11
D_{34A}	102	G13
D_{33A}	103	F13
D_{32A}	105	F12
D_{31A}	106	E12
D_{30A}	107	E13
D_{29A}	109	D13

SIGNAL NAME	PQFP PIN NO.	PGA PIN NO.
D_{28A}	110	D12
D_{27A}	111	C13
D_{26A}	113	C12
D_{25A}	114	B12
D_{24A}	115	B13
D_{23A}	117	C11
D_{22A}	118	A13
D_{21A}	119	C10
D_{20A}	120	A12
D_{19A}	122	B11
D_{18A}	123	C9
$\overline{MBF}_2$	124	A11
$\overline{AE}_2$	125	B9
$\overline{EF}_2$	126	B10
ACK_A	127	A10
REQ_A	129	A9
EN_A	130	B8
$R/\overline{W}_A$	131	A8
CK_A	132	C7
V_{CC}	5	C6
V_{SSA}	13	E3
V_{CCA}	18	D3
V_{SSA}	22	E3
V_{CCA}	26	D3
V_{SSA}	30	E3
V_{SSB}	38	J3
V_{CCB}	42	K3
V_{SSB}	46	J3
V_{CCB}	50	K3
V_{SSB}	55	J3
V_{SS}	62	L6
V_{CC}	71	L8
V_{SSB}	79	J11
V_{CCB}	84	K11
V_{SSB}	88	J11
V_{CCB}	92	K11
V_{SSB}	96	J11
V_{SS}	99	G11
V_{SSA}	104	E11
V_{CCA}	108	D11
V_{SSA}	112	E11
V_{CCA}	116	D11
V_{SSA}	121	E11
V_{SS}	128	C8

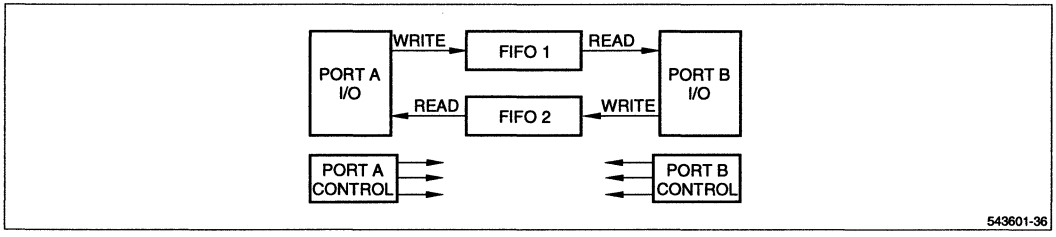


Figure 4a. Simplified LH543601/11 Block Diagram

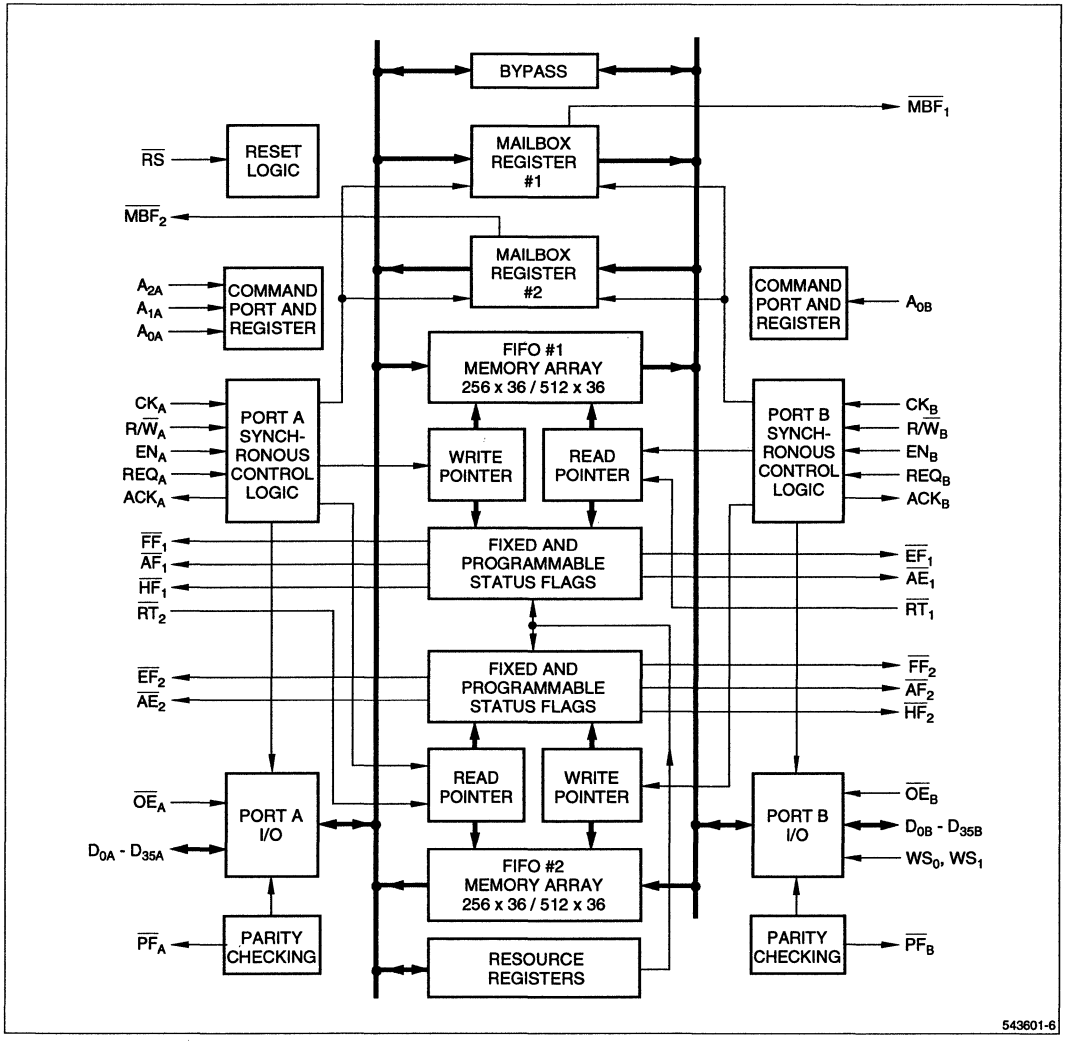


Figure 4b. Detailed LH543601/11 Block Diagram

PIN DESCRIPTIONS

PIN	PIN TYPE *	DESCRIPTION
		GENERAL
V_{CC}, V_{SS}	V	Power, Ground
$\overline{RS}$	I	Reset
		PORT A
CK_A	I	Port A Free-Running Clock
$R/\overline{W}_A$	I	Port A Edge-Sampled Read/Write Control
EN_A	I	Port A Edge-Sampled Enable
A_{0A}, A_{1A}, A_{2A}	I	Port A Edge-Sampled Address Pins
$\overline{OE}_A$	I	Port A Level-Sensitive Output Enable
REQ_A	I	Port A Request/Enable
$\overline{RT}_2$	I	FIFO #2 Retransmit
$D_{0A} - D_{35A}$	I/O/Z	Port A Bidirectional Data Bus
$\overline{FF}_1$	O	FIFO #1 Full Flag (Write Boundary)
$\overline{AF}_1$	O	FIFO #1 Programmable Almost-Full Flag (Write Boundary)
$\overline{HF}_1$	O	FIFO #1 Half-Full Flag
$\overline{AE}_2$	O	FIFO #2 Programmable Almost-Empty Flag (Read Boundary)
$\overline{EF}_2$	O	FIFO #2 Empty Flag (Read Boundary)
$\overline{MBF}_2$	O	New-Mail-Alert Flag for Mailbox #2
$\overline{PF}_A$	O	Port A Parity Flag
ACK_A	O	Port A Acknowledge
		PORT B
CK_B	I	Port B Free-Running Clock
$R/\overline{W}_B$	I	Port B Edge-Sampled Read/Write Control
EN_B	I	Port B Edge-Sampled Enable
A_{0B}	I	Port B Edge-Sampled Address Pin
$\overline{OE}_B$	I	Port B Level-Sensitive Output Enable
WS_0, WS_1	I	Port B Word-Width Select
REQ_B	I	Port B Request/Enable
$\overline{RT}_1$	I	FIFO #1 Retransmit
$D_{0B} - D_{35B}$	I/O/Z	Port B Bidirectional Data Bus
$\overline{FF}_2$	O	FIFO #2 Full Flag (Write Boundary)
$\overline{AF}_2$	O	FIFO #2 Programmable Almost-Full Flag (Write Boundary)
$\overline{HF}_2$	O	FIFO #2 Half-Full Flag
$\overline{AE}_1$	O	FIFO #1 Programmable Almost-Empty Flag (Read Boundary)
$\overline{EF}_1$	O	FIFO #1 Empty Flag (Read Boundary)
$\overline{MBF}_1$	O	New-Mail-Alert Flag for Mailbox #1
$\overline{PF}_B$	O	Port B Parity Flag
ACK_B	O	Port B Acknowledge

* I = Input, O = Output, Z = High-Impedance, V = Power Voltage Level

ABSOLUTE MAXIMUM RATINGS [1]

PARAMETER	RATING
Supply Voltage to V_{SS} Potential	−0.5 V to 7 V
Signal Pin Voltage to V_{SS} Potential [3]	−0.5 V to V_{CC} + 0.5 V
DC Output Current [2]	± 40 mA
Storage Temperature Range	−65°C to 150°C
Power Dissipation (Package Limit)	2 Watts (Quad Flat Pack)

NOTES:

1. Stresses greater than those listed under 'Absolute Maximum Ratings' may cause permanent damage to the device. This is a stress rating for transient conditions only. Functional operation of the device at these or any other conditions outside those indicated in the 'Operating Range' of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Outputs should not be shorted for more than 30 seconds. No more than one output should be shorted at any time.
3. Negative undershoot of 1.5 V in amplitude is permitted for up to 10 ns, once per cycle.

OPERATING RANGE

SYMBOL	PARAMETER	MIN	MAX	UNIT
T_A	Temperature, Ambient	0	70	°C
V_{CC}	Supply Voltage	4.5	5.5	V
V_{SS}	Supply Voltage	0	0	V
V_{IL}	Logic LOW Input Voltage [1]	−0.5	0.8	V
V_{IH}	Logic HIGH Input Voltage	2.2	Vcc + 0.5	V

NOTE:

1. Negative undershoot of 1.5 V in amplitude is permitted for up to 10 ns, once per cycle.

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
I_{LI}	Input Leakage Current	V_{CC} = 5.5 V, V_{IN} = 0 V To V_{CC}	−10	10	µA
I_{LO}	I/O Leakage Current	$\overline{OE} \geq V_{IH}$, 0 V ≤ $V_{OUT} \leq V_{CC}$	−10	10	µA
V_{OL}	Logic LOW Output Voltage	I_{OL} = 16.0 mA		0.4	V
V_{OH}	Logic HIGH Output Voltage	I_{OH} = −4.0 mA	2.4		V
I_{CC}	Average Supply Current [1]	Measured at f_C = max		280	mA
I_{CC2}	Average Standby Supply Current [1]	All Inputs = V_{IHMIN} (Clock idle)		75	mA
I_{CC3}	Power-Down Supply Current [1]	All Inputs = V_{CC} − 0.2 V (Clock idle)		0.1	mA

NOTE:

1. I_{CC}, I_{CC2}, and I_{CC3} are dependent upon actual output loading, and I_{CC} is also dependent on cycle rates. Specified values are with outputs open; and, for I_{CC}, operating at minimum cycle times.

AC TEST CONDITIONS

PARAMETER	RATING
Input Pulse Levels	Vss to 3 V
Input Rise and Fall Times (10% to 90%)	5 ns
Output Reference Levels	1.5 V
Input Timing Reference Levels	1.5 V
Output Load, Timing Tests	Figure 5

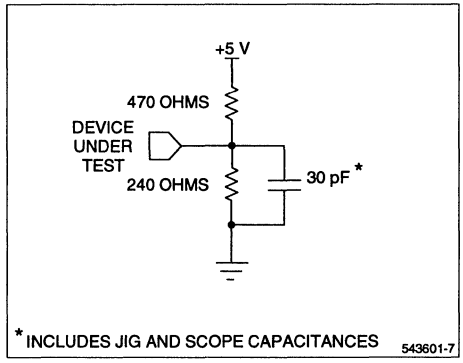


Figure 5. Output Load Circuit

CAPACITANCE [1,2]

PARAMETER	RATING
C_{IN} (Input Capacitance)	8 pF
C_{OUT} (Output Capacitance)	8 pF

NOTES:

1. Sample tested only.
2. Capacitances are maximum values at 25°C, measured at 1.0MHz, with V_{IN} = 0 V.

AC ELECTRICAL CHARACTERISTICS [1] (V_{CC} = 5 V ± 10%, T_A = 0°C to 70°C)

SYMBOL	DECRIPTION	–15		–20		–25		–30		–35		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{CC}	Clock Cycle Frequency	—	67	—	50	—	40	—	33	—	28.5	MHz
t_{CC}	Clock Cycle Time	15	—	20	—	25	—	30	—	35	—	ns
t_{CH}	Clock HIGH Time	6	—	8	—	10	—	12	—	15	—	ns
t_{CL}	Clock LOW Time	6	—	8	—	10	—	12	—	15	—	ns
t_{DS}	Data Setup Time	4	—	5	—	6	—	7	—	8	—	ns
t_{DH}	Data Hold Time	0	—	0	—	0	—	0	—	0	—	ns
t_{ES}	Enable Setup Time [6]	4	—	5	—	6	—	7	—	8	—	ns
t_{EH}	Enable Hold Time [6]	0	—	0	—	0	—	0	—	0	—	ns
t_{RWS}	Read/Write Setup Time	4	—	5	—	6	—	7	—	8	—	ns
t_{RWH}	Read/Write Hold Time	0	—	0	—	0	—	0	—	0	—	ns
t_{RQS}	Request Setup Time [6]	9	—	12	—	15	—	18	—	21	—	ns
t_{RQH}	Request Hold Time [6]	0	—	0	—	0	—	0	—	0	—	ns
t_{AS}	Address Setup Time [6]	9	—	12	—	15	—	18	—	21	—	ns
t_{AH}	Address Hold Time [6]	0	—	0	—	0	—	0	—	0	—	ns
t_A	Data Output Access Time	—	9	—	12	—	15	—	18	—	21	ns
t_{ACK}	Acknowledge Access Time	—	9	—	12	—	15	—	18	—	21	ns
t_{OH}	Output Hold Time	3	—	4	—	5	—	5	—	5	—	ns
t_{ZX}	Output Enable Time, $\overline{OE}$ LOW to $D_0 - D_{35}$ Low-Z [2]	3	—	4	—	5	—	5	—	5	—	ns
t_{XZ}	Output Disable Time, $\overline{OE}$ HIGH to $D_0 - D_{35}$ High-Z [2]	—	9	—	12	—	15	—	18	—	21	ns
t_{EF}	Clock to $\overline{EF}$ Flag Valid (Empty Flag)	—	9	—	12	—	15	—	18	—	21	ns
t_{FF}	Clock to $\overline{FF}$ Flag Valid (Full Flag)	—	9	—	12	—	15	—	18	—	21	ns
t_{HF}	Clock to $\overline{HF}$ Flag Valid (Half-Full)	—	9	—	12	—	15	—	18	—	21	ns
t_{AE}	Clock to $\overline{AE}$ Flag Valid (Almost-Empty)	—	9	—	12	—	15	—	18	—	21	ns
t_{AF}	Clock to $\overline{AF}$ Flag Valid (Almost-Full)	—	9	—	12	—	15	—	18	—	21	ns
t_{MBF}	Clock to $\overline{MBF}$ Flag Valid (Mailbox Flag)	—	9	—	12	—	15	—	18	—	21	ns
t_{PF}	Data to Parity Flag Valid	—	9	—	12	—	15	—	18	—	21	ns
t_{RS}	Reset/Retransmit Pulse Width [7]	24/15	—	32/20	—	40/25	—	52/30	—	65/35	—	ns
t_{RSS}	Reset/Retransmit Setup Time [3]	12	—	16	—	20	—	25	—	30	—	ns
t_{RSH}	Reset/Retransmit Hold Time [3]	6	—	8	—	10	—	15	—	20	—	ns
t_{RF}	Reset LOW to Flag Valid	—	25	—	30	—	35	—	40	—	45	ns
t_{FRL}	First Read Latency [4]	15	—	20	—	25	—	30	—	35	—	ns
t_{FWL}	First Write Latency [5]	15	—	20	—	25	—	30	—	35	—	ns
t_{BS}	Bypass Data Setup	9	—	12	—	15	—	18	—	21	—	ns
t_{BH}	Bypass Data Hold	3	—	4	—	5	—	5	—	5	—	ns
t_{BA}	Bypass Data Access	—	12	—	16	—	20	—	25	—	30	ns

NOTES:

1. Timing measurements performed at 'AC Test Condition' levels.
2. Values are guaranteed by design; not currently production tested.
3. t_{RSS} and/or t_{RSH} need not be met unless a rising edge of CK_A occurs while EN_A is being asserted, or else a rising edge of CK_B occurs while EN_B is being asserted.
4. t_{FRL} is the minimum first-write-to-first-read delay, following an empty condition, which is required to assure valid read data.
5. t_{FWL} is the minimum first-read-to-first-write delay, following a full condtion, which is required to assure successful writing of data.
6. t_{AS}, t_{AH} address setup times and hold times need only be satisfied at clock edges which occur while the corresponding enables are being asserted.
7. First number used only when CK_A or CK_B is enabled; $t_{RS} = t_{RSS} + t_{CH} + t_{RSH}$.

OPERATIONAL DESCRIPTION

Reset

The device is reset whenever the asynchronous Reset ($\overline{RS}$) input is taken LOW. A reset operation is required after power-up, before the first write operation may occur. The LH543601/11 are fully ready for operation after being reset. No device programming is required if the default states described below are acceptable.

A reset operation initializes the read-address and write-address pointers for FIFO #1 and FIFO #2 to those FIFO's first physical memory locations. If the respective outputs are enabled, the initial contents of these first locations appear at the outputs. FIFO and mailbox status flags are updated to indicate an empty condition. In addition, the programmable-status-flag offset values are initialized to eight. Thus, the $\overline{AE}_1/\overline{AE}_2$ flags get asserted within eight locations of an empty condition, and the $\overline{AF}_1/\overline{AF}_2$ flags likewise get asserted within eight locations of a full condition, for FIFO #1/FIFO #2 respectively.

Bypass Operation

During reset (whenever $\overline{RS}$ is LOW) the device acts as a registered transceiver, bypassing the internal FIFO memories. Port A acts as the master port. A write or read operation on Port A during reset transfers data directly to or from Port B. Port B is considered to be the slave, and cannot perform write or read operations independently on its own during reset.

The direction of the bypass data transmission is determined by th $R/\overline{W}_A$ control input, which does not get overridden by the $\overline{RS}$ input. Here, a 'write' operation means passing data from Port A to Port B, and a 'read' operation means passing data from Port B to Port A.

The bypass capability may be used to pass initialization or configuration data directly between a master processor and a peripheral device during reset.

Address Modes

Address pins select the device resource to be accessed by each port. Port A has three resource-register-select inputs, A_{0A}, A_{1A}, and A_{2A}, which select between FIFO access, mailbox-register access, and flag-offset-value-programming operating mode. Port B has a single address input, A_{0B}, to select between FIFO access or mailbox-register access.

The status of the resource-register-select inputs is sampled at the rising edge of an enabled clock (CK_A or CK_B). Resource-register select-input address definitions are summarized in Table 1.

FIFO Write

Port A writes to FIFO #1, and Port B writes to FIFO #2. A write operation is initiated on the rising edge of a clock (CK_A or CK_B) whenever: the appropriate enable (EN_A or EN_B) is held HIGH; the appropriate request (REQ_A or REQ_B) is held HIGH; the appropriate Read/Write control ($R/\overline{W}_A$ or $R/\overline{W}_B$) is held LOW; the FIFO address is selected for the address inputs ($A_{2A} - A_{0A}$ or A_{0B}); and the prescribed setup times and hold times are observed for all of these signals. Setup times and hold times must also be observed on the data-bus pins ($D_{0A} - D_{35A}$ or $D_{0B} - D_{35B}$).

Normally, the appropriate Output Enable signal ($\overline{OE}_A$ or $\overline{OE}_B$) is HIGH, to disable the outputs at that port, so that the data word present on the bus from external sources gets stored. However, a 'loopback' mode of operation also is possible, in which the data word supplied by the outputs of one internal FIFO is 'turned around' at the port and read back into the other FIFO. In this mode, the outputs at the port are not disabled. To remain within specification for all timing parameters, the Clock Cycle Frequency must be reduced slightly below the value which otherwise would be permissible for that speed grade of LH5420.

When a FIFO full condition is reached, write operations are locked out. Following the first read operation from a full FIFO, another memory location is freed up, and the corresponding Full Flag is deasserted ($\overline{FF}$ = HIGH). The first write operation should begin no earlier than a First Write Latency (t_{FWL}) after the first read operation from a full FIFO, to ensure that correct read data are retrieved.

Table 1. Resource-Register Addresses

A_{2A}	A_{1A}	A_{0A}	RESOURCE
PORT A			
H	H	H	FIFO
H	H	L	Mailbox
H	L	H	$\overline{AF}_2$, $\overline{AE}_2$, $\overline{AF}_1$, $\overline{AE}_1$ Flag Offset Registers
H	L	L	Control Register
L	H	H	$\overline{AE}_1$ Flag Offset Register
L	H	L	$\overline{AF}_1$ Flag Offset Register
L	L	H	$\overline{AE}_2$ Flag Offset Register
L	L	L	$\overline{AF}_2$ Flag Offset Register
A_{0B}			RESOURCE
PORT B			
H			FIFO
L			Mailbox

FIFO Read

Port A reads from FIFO #2, and Port B reads from FIFO #1. A read operation is initiated on the rising edge of a clock (CK_A or CK_B) whenever: the appropriate enable (EN_A or EN_B) is held HIGH; the appropriate request (REQ_A or REQ_B) is held HIGH; the appropriate Read/Write control ($R/\overline{W}_A$ or $R/\overline{W}_B$) is held HIGH; the FIFO address is selected for the address inputs

OPERATIONAL DESCRIPTION (cont'd)

($A_{2A} - A_{0A}$ or A_{0B}); and the prescribed setup times and hold times are observed for all of these signals. Read data becomes valid on the data-bus pins ($D_{0A} - D_{35A}$ or $D_{0B} - D_{35B}$) by a time t_A after the rising clock (CK_A or CK_B) edge, provided that the data outputs are enabled.

$\overline{OE}_A$ and $\overline{OE}_B$ are assertive-LOW, asynchronous, Output Enables control input signals. Their effect is only to enable or disable the output drivers of the respective port. Disabling the outputs does *not* disable a read operation; data transmitted to the corresponding output register will remain available later, when the outputs again are enabled, unless it subsequently is overwritten.

When an empty condition is reached, read operations are locked out until a valid write operation(s) has loaded additional data into the FIFO. Following the first write to an empty FIFO, the corresponding empty flag ($\overline{EF}$) will be deasserted (HIGH). The first read operation should begin no earlier than a First Read Latency (t_{FRL}) after the first write to an empty FIFO, to ensure that correct read data is retrieved.

Dedicated FIFO Status Flags

Six dedicated FIFO status flags are included for Full ($\overline{FF}_1$ and $\overline{FF}_2$), Half-Full ($\overline{HF}_1$ and $\overline{HF}_2$), and Empty ($\overline{EF}_1$ and $\overline{EF}_2$). $\overline{FF}_1$, $\overline{HF}_1$, and $\overline{EF}_1$ indicate the status of FIFO #1; and $\overline{FF}_2$, $\overline{HF}_2$, and $\overline{EF}_2$ indicate the status of FIFO #2.

A Full Flag is asserted following the rising clock edge for a write operation that fills the FIFO. A Full Flag is deasserted following the falling clock edge for a read operation to a full FIFO. A Half-Full Flag is updated following the rising clock edge of a read or write operation to a FIFO. An Empty Flag is asserted following the rising clock edge for a read operation that empties the FIFO. An Empty Flag is deasserted following the falling clock edge for a write operation to an empty FIFO.

Programmable Status Flags

Four programmable FIFO status flags are provided, two for Almost-Full ($\overline{AF}_1$ and $\overline{AF}_2$), and two for Almost-Empty ($\overline{AE}_1$ and $\overline{AE}_2$). Thus, each port has two programmable flags to monitor the status of the two internal FIFO buffer memories. The offset values for these flags are initialized to eight locations from the respective FIFO boundaries during reset, but can be reprogrammed over the entire FIFO depth.

An Almost-Full Flag is asserted following the rising clock edge for a write operation that fills the FIFO. An Almost-Full Flag is deasserted following the falling clock edge for a read operation to a full FIFO. An Almost-Empty Flag is asserted following the rising clock edge for a read operation that empties the FIFO. An Almost-Empty Flag is deasserted following the falling clock edge for a write operation to an empty FIFO.

Flag offsets may be written or read through the Port A data bus. All four programmable FIFO status flag offsets can be set simultaneously through a single 36-bit status word; or, each programmable flag offset can be set individually, through one of four eight-bit (LH543601) or nine-bit (LH543611) status words. Table 3a illustrates the data format for flag-programming words for the LH543601, and Table 3b illustrates the data format for flag-programming words for the LH543611.

Also, Table 4a defines the meaning of each of the five flags, both the dedicated flags and the programmable flags, for the LH543601. Likewise, Table 4b lists the same definitions for the LH543611.

WARNING: Control inputs which may affect the computation of flag values at a port generally should not change while the clock for that port is HIGH, since some updating of flag values takes place on the *falling* edge of the clock.

Mailbox Operation

Two mailbox registers are provided for passing system hardware or software control/status words between ports. Each port can read its own mailbox and write to the other port's mailbox. Mailbox access is performed on the rising edge of the controlling FIFO's clock, with the mailbox address selected and the enable (EN_A or EN_B) HIGH. That is, writing to Mailbox Register #1, or reading from Mailbox Register #2, is synchronized to CK_A; and writing to Mailbox Register #2, or reading from Mailbox Register #1, is synchronized to CK_B.

The $R/\overline{W}_{A/B}$ and $\overline{OE}_{A/B}$ pins control the direction and availability of mailbox-register accesses. Each mailbox register has its own New-Mail-Alert Flag ($\overline{MBF}_1$ and $\overline{MBF}_2$), which is synchronized to the reading port's clock. These New-Mail-Alert Flags are status indicators only, and cannot inhibit mailbox-register read or write operations.

Request Acknowledge Handshake

A synchronous, request-acknowledge handshake feature is provided for each port, to perform boundary synchronization between asynchronously-operated ports. The use of this feature is optional. When it is used, the Request input ($REQ_{A/B}$) is sampled at a rising clock edge. With $REQ_{A/B}$ HIGH, $R/\overline{W}_{A/B}$ determines whether a FIFO read operation or a FIFO write operation is being requested. The Acknowledge output ($ACK_{A/B}$) is updated during the following clock cycle(s). $ACK_{A/B}$ meets the setup and hold time requirements of the Enable input (EN_A or EN_B). Therefore, $ACK_{A/B}$ may be tied back to the enable input to directly gate FIFO accesses, at a slight decrease in maximum operating frequency.

The assertion of $ACK_{A/B}$ signifies that $REQ_{A/B}$ was asserted. However, $ACK_{A/B}$ does not depend logically on $EN_{A/B}$; and thus the assertion of $ACK_{A/B}$ does *not* prove that a FIFO write access or a FIFO read access actually took place. While $REQ_{A/B}$ and $EN_{A/B}$ are being held HIGH, $ACK_{A/B}$ may be considered as a synchronous, predictive boundary flag. That is, $ACK_{A/B}$ acts as a synchronized predictor of the Almost-Full Flag $\overline{AF}$ for write operations, or as a synchronized predictor of the Almost-Empty Flag $\overline{AE}$ for read operations.

OPERATIONAL DESCRIPTION (cont'd)

Outside the 'almost-full' region and the 'almost-empty' region, $ACK_{A/B}$ remains continuously HIGH whenever $REQ_{A/B}$ is held continuously HIGH. Within the 'almost-full' region or the 'almost-empty' region, $ACK_{A/B}$ occurs only on every *third* cycle, to prevent an overrun of the FIFO's actual full or empty boundaries and to ensure that the t_{FWL} (first write latency) and t_{FRL} (first read latency) specifications are satisfied before $ACK_{A/B}$ is received.

The 'almost-full region' is defined as 'that region, where the Almost-Full Flag is being asserted'; and the 'almost-empty region' as 'that region, where the Almost-Empty Flag is being asserted.' Thus, the extent of these 'almost' regions depends on how the system has programmed the offset values for the Almost-Full Flags and the Almost-Empty Flags. If the system has *not* programmed them, then these offset values remain at their default values, eight in each case.

If a write attempt is unsuccessful because the corresponding FIFO is full, or if a read attempt is unsuccessful because the corresponding FIFO is empty, $ACK_{A/B}$ is *not* asserted in response to $REQ_{A/B}$.

If the REQ/ACK handshake is not used, then the $REQ_{A/B}$ input may be used as a second enable input, at a possible minor loss in maximum operating speed. In this case, the $ACK_{A/B}$ output may be ignored.

WARNING: Whether or not the REQ/ACK handshake is being used, the $REQ_{A/B}$ input for a port *must* be asserted for the corresponding FIFO to operate.

Data Retransmit

A retransmit operation resets the read-address pointer of the corresponding FIFO (#1 or #2) back to the first FIFO physical memory location, so that data may be reread. The write pointer is not affected. The status flags are updated; and a block of up to 256 (LH543601) or 512 (LH543611) data words, which previously had been written into and read from a FIFO, can be retrieved. The block to be retransmitted is bounded by the first FIFO memory location, and the FIFO memory location addressed by the write pointer. FIFO #1 retransmit is initiated by strobing the $\overline{RT}_1$ pin LOW. FIFO #2 retransmit is initiated by strobing the $\overline{RT}_2$ pin LOW. Read and write operations to a FIFO should be stopped while the corresponding Retransmit signal is being asserted.

Parity Check

The Parity Check Flags, $\overline{PF}_A$ and $\overline{PF}_B$, are asserted (LOW) whenever there is a parity error in the data word present on the Port A data bus or the Port B data bus respectively. The inputs to the parity-evaluation logic come directly (via isolation transistors) from the data-bus bonding *pads*, in each case.

The four bytes of a 36-bit data word are grouped as $D_0 - D_8$, $D_9 - D_{17}$, $D_{18} - D_{26}$, and $D_{27} - D_{35}$. The parity of each nine-bit byte is individually checked, and the four single-bit parity indications are logically inclusive-ORed to produce the Parity-Flag output. Parity checking is initialized for odd parity at reset, but can be reprogrammed for even parity or for odd parity during operation.

All nine bits of each byte are treated alike by the parity logic. The byte parity over the nine bits is compared with the Parity Mode bit in the Control Register, to generate a byte-parity-error indication. Then, the four byte-parity-error signals are NORed together, to compute the assertive-LOW parity-flag value.

Word-Width Selection on Port B

The word width of data access on Port B is selected by the WS_0 and WS_1 control inputs. WS_0 and WS_1 both are tied HIGH for 36-bit access; they both are tied LOW for single-byte access. For double-byte access, WS_0 is tied HIGH and WS_1 is tied LOW.

In the single-byte-access or double-byte-access modes, FIFO write operations on Port B essentially pack the data to form 36-bit words, as viewed from Port A. Similarly, single-byte or double-byte FIFO read operations on Port B essentially unpack 36-bit words through a series of shift operations. FIFO status flags are updated following the last access which forms a complete 36-bit transfer.

Since the values for each status flag are computed by logic directly associated with one of the two FIFO-memory arrays, and not by logic associated with Port B, *the flag values reflect the array fullness situation in terms of complete 36-bit words*, and not in terms of bytes or double bytes.

However, there is no such restriction for switching from writing to reading, or from reading to writing, at Port B. As long as t_{RWS}, t_{DS}, and t_A are satisfied, $R/\overline{W}_B$ may change state after *any* single-byte or double-byte access, and not only after a full 36-bit-word access.

Also, the word-width-matching feature continues to operate properly in 'loopback' mode.

Note that the programmable word-width-matching feature is *only* supported for FIFO accesses. Mailbox and Data Bypass operations do *not* support word-width matching between Port A and Port B. Tables 2, 3a, 3b, 4a, and 4b, and Figures 6a, 6b, 7a, and 7b summarize word-width selection for Port B.

Table 2. Port B Word-Width Selection

WS_1	WS_0	PORT B DATA WIDTH
H	H	36-Bit
H	L	(Reserved)
L	H	18-Bit
L	L	9-Bit

Table 3a. LH543601 Resource-Register Programming

RESOURCE-REGISTER ADDRESS			RESOURCE-REGISTER CONTENTS								
A_2	A_1	A_0									
			NORMAL FIFO OPERATION								
H	H	H	X...								
			MAILBOX								
H	H	L	X...								
			36-BIT MODE								
			$D_{34A} \ldots D_{27A}$		$D_{25A} \ldots D_{18A}$		$D_{16A} \ldots D_{9A}$		$D_{7A} \ldots D_{0A}$		
H	L	H	X	$\overline{AF}_2$ Offset [1]	X	$\overline{AE}_2$ Offset [1]	X	$\overline{AF}_1$ Offset [1]	X	$\overline{AE}_1$ Offset [1]	
			CONTROL REGISTER (WRITE-ONLY)								
									D_{0A}		
H	L	L	X...						X	Parity Mode [2]	
			8-BIT $\overline{AE}_1$ FLAG								
									$D_{7A} \ldots D_{0A}$		
L	H	H	X...						X	$\overline{AE}_1$ Offset [1]	
			8-BIT $\overline{AF}_1$ FLAG								
									$D_{7A} \ldots D_{0A}$		
L	H	L	X...						X	$\overline{AF}_1$ Offset [1]	
			8-BIT $\overline{AE}_2$ FLAG								
									$D_{7A} \ldots D_{0A}$		
L	L	H	X...						X	$\overline{AE}_2$ Offset [1]	
			8-BIT $\overline{AF}_2$ FLAG								
									$D_{7A} \ldots D_{0A}$		
L	L	L	X...						X	$\overline{AF}_2$ Offset [1]	

NOTES:

1. All four programmable-flag-offset values are initialized to eight (8) during a reset operation.
2. Odd parity = HIGH; even parity = LOW. The parity mode is initialized to odd during a reset operation.

Table 3b. LH543611 Resource-Register Programming

RESOURCE-REGISTER ADDRESS			RESOURCE-REGISTER CONTENTS			
A_2	A_1	A_0				
			NORMAL FIFO OPERATION			
H	H	H	X...			
			MAILBOX			
H	H	L	X...			
			36-BIT MODE			
			D_{35A} . . . D_{27A}	D_{26A} . . . D_{18A}	D_{17A} . . . D_{9A}	D_{8A} . . . D_{0A}
H	L	H	$\overline{AF}_2$ Offset [1]	$\overline{AE}_2$ Offset [1]	$\overline{AF}_1$ Offset [1]	$\overline{AE}_1$ Offset [1]
			CONTROL REGISTER (WRITE-ONLY)			
						D_{0A}
H	L	L	X...		X	Parity Mode [2]
			8-BIT $\overline{AE}_1$ FLAG			
						D_{8A} . . . D_{0A}
L	H	H	X...		X	$\overline{AE}_1$ Offset [1]
			8-BIT $\overline{AF}_1$ FLAG			
						D_{8A} . . . D_{0A}
L	H	L	X...		X	$\overline{AF}_1$ Offset [1]
			8-BIT $\overline{AE}_2$ FLAG			
						D_{8A} . . . D_{0A}
L	L	H	X...		X	$\overline{AE}_2$ Offset [1]
			8-BIT $\overline{AF}_2$ FLAG			
						D_{8A} . . . D_{0A}
L	L	L	X...		X	$\overline{AF}_2$ Offset [1]

NOTES:

1. All four programmable-flag-offset values are initialized to eight (8) during a reset operation.
2. Odd parity = HIGH; even parity = LOW. The parity mode is initialized to odd during a reset operation.

Table 4a. LH543601 Flag Definition Table [1]

FLAG	VALID READ CYCLES REMAINING				VALID WRITE CYCLES REMAINING			
	FLAG = LOW		FLAG = HIGH		FLAG = LOW		FLAG = HIGH	
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
$\overline{FF}$	256	256	0	255	0	0	1	256
$\overline{AF}$	256-p	256	0	255-p	0	p	p + 1	256
$\overline{HF}$	129	256	0	128	0	127	128	256
$\overline{AE}$	0	q	q + 1	256	256-q	256	0	255-q
$\overline{EF}$	0	0	1	256	256	256	0	255

Table 4b. LH543611 Flag Definition Table [1]

FLAG	VALID READ CYCLES REMAINING				VALID WRITE CYCLES REMAINING			
	FLAG = LOW		FLAG = HIGH		FLAG = LOW		FLAG = HIGH	
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
$\overline{FF}$	512	512	0	511	0	0	1	512
$\overline{AF}$	512-p	512	0	511-p	0	p	p + 1	512
$\overline{HF}$	257	512	0	256	0	255	256	512
$\overline{AE}$	0	q	q + 1	512	512-q	512	0	511-q
$\overline{EF}$	0	0	1	512	512	512	0	511

NOTE:

1. p is the number in the Almost-Full-Flag-Offset-Value register for that port. q is the number in the Almost-Empty-Flag-Offset-Value register for that port.

PORT B WORD-WIDTH SELECTION

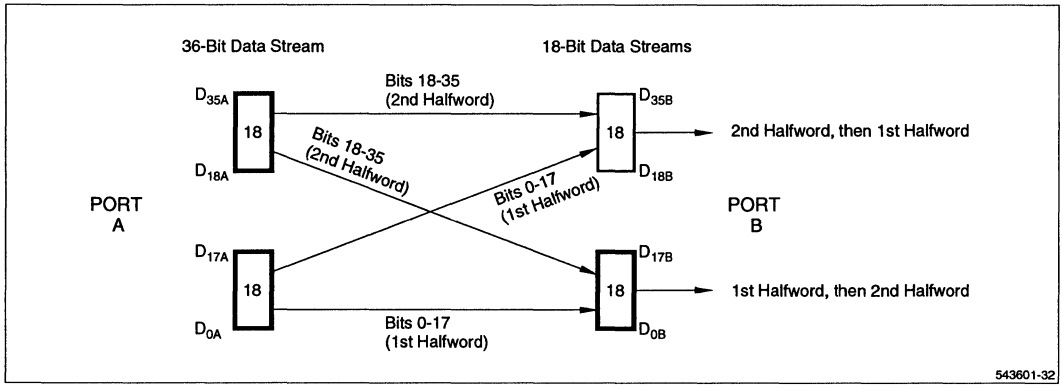


Figure 6a. 36-to-18 Funneling Through FIFO #1

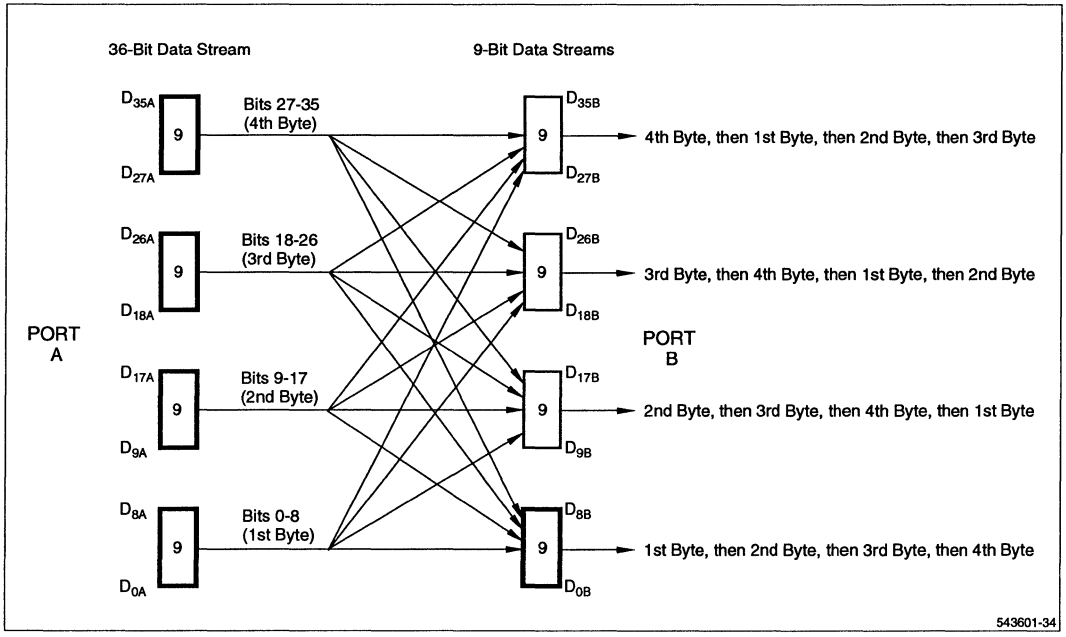


Figure 6b. 36-to-9 Funneling Through FIFO #1

NOTES:

1. The heavy black borders on register segments indicate the main data path, suitable for most applications. Alternate paths feature a different ordering of bytes within a word, at Port B.
2. The funneling process does not change the ordering of bits within a byte. Halfwords (Figure 6a) or bytes (Figure 6b) are transferred in parallel form from Port A to Port B.
3. The word-width setting may be changed during system operation; however, two clock intervals should be allowed for these signals to settle, before again attempting to read $D_{0B} - D_{35B}$. Also, incomplete data words may occur when the word width is changed from shorter to longer, at an inappropriate point in the data block passing through the FIFO.

PORT B WORD-WIDTH SELECTION

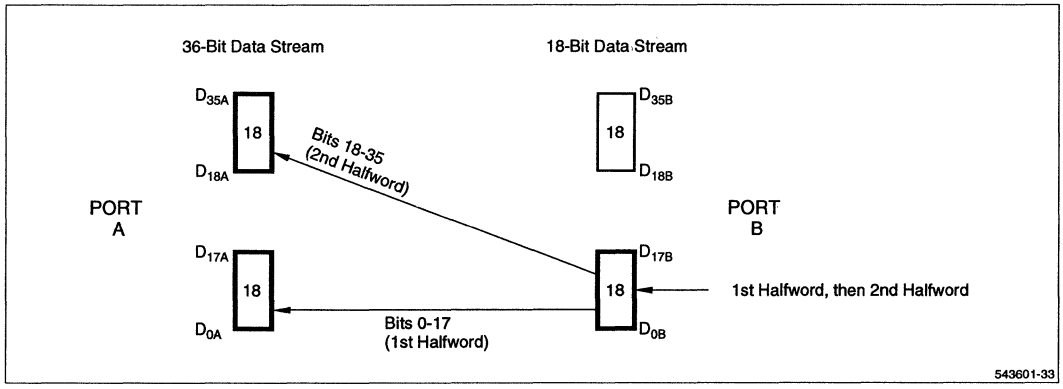


Figure 7a. 18-to-36 Defunneling Through FIFO #2

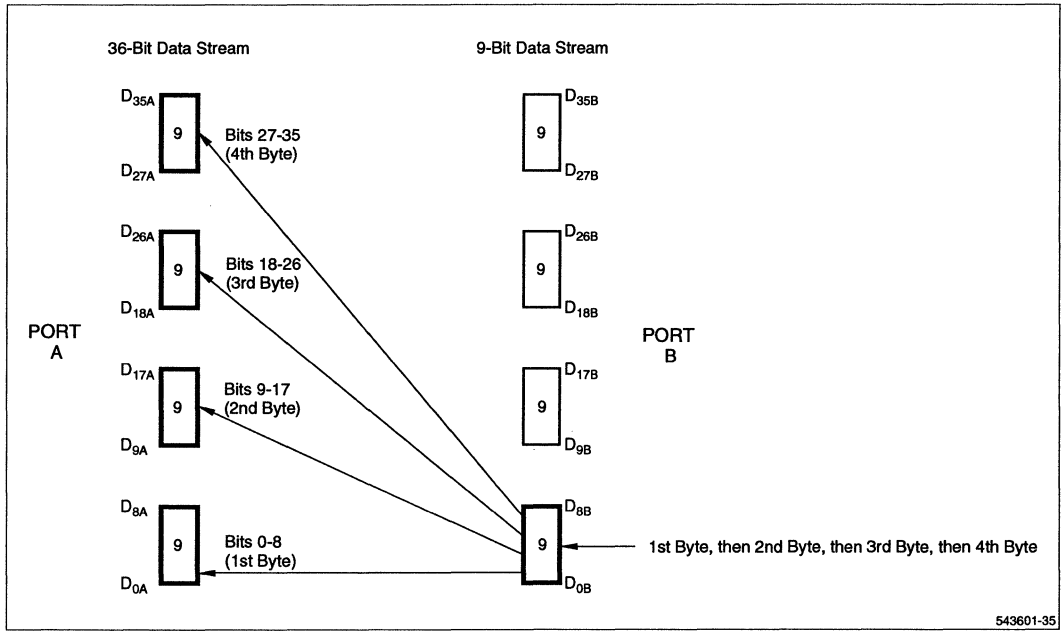
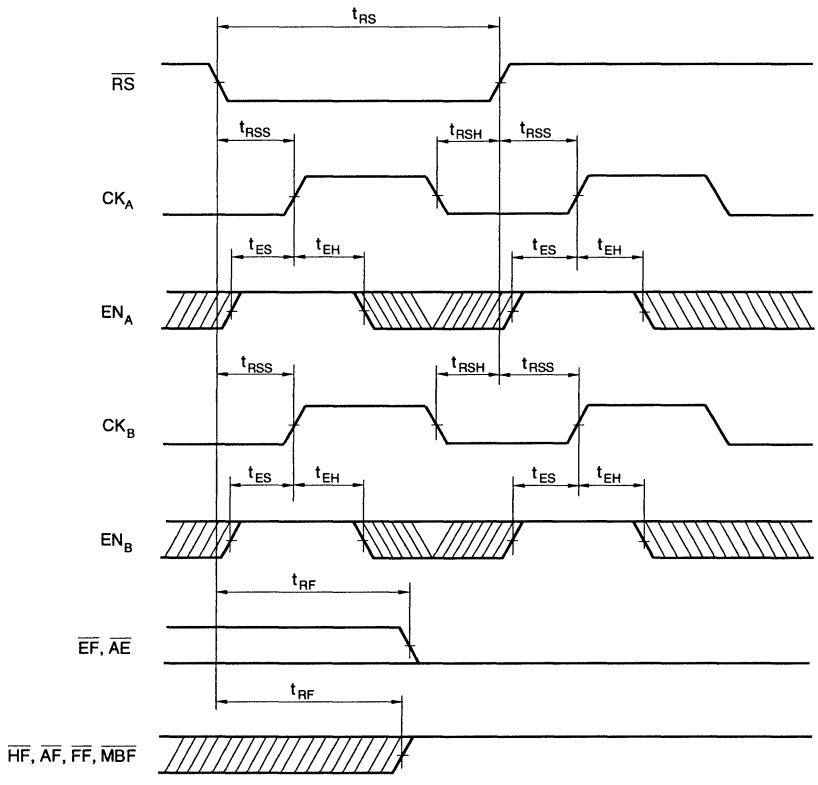


Figure 7b. 9-to-36 Defunneling Through FIFO #2

NOTES:

1. The heavy black borders on register segments indicate the only data paths used. The other byte segments of Port B do not participate in the data path during defunneling.
2. The defunneling process does not change the ordering of bits within a byte. Halfwords (Figure 7a) or bytes (Figure 7b) are transferred in parallel form from Port B to Port A.
3. The word-width setting may be changed during system operation; however, two clock intervals should be allowed for these signals to settle, before again attempting to send data. Also, incomplete data words may occur when the word width is changed from shorter to longer, at an inappropriate point in the data block passing through the FIFO.

TIMING DIAGRAMS



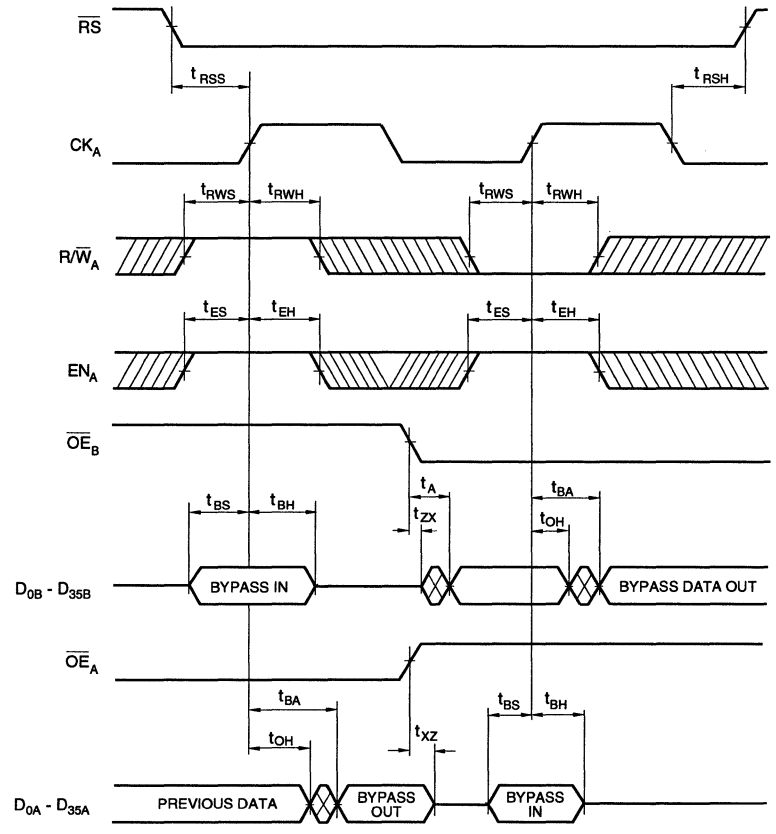
NOTES:

1. $\overline{RS}$ overrides all other input signals, except for $R/\overline{W}_A$, and operates asynchronously. $\overline{RS}$ operates whether or not EN_A and/or EN_B are asserted.
2. t_{RSS}, t_{RSH} need not be met unless the rising edge of CK_A and/or CK_B occurs while that clock is enabled.
3. The parity check is initialized to odd byte parity at reset.
4. The $\overline{AE}$ and $\overline{AF}$ flag offsets are initialized to eight locations from the boundary at reset.

543601-26

Figure 8. Reset Timing

TIMING DIAGRAMS (cont'd)



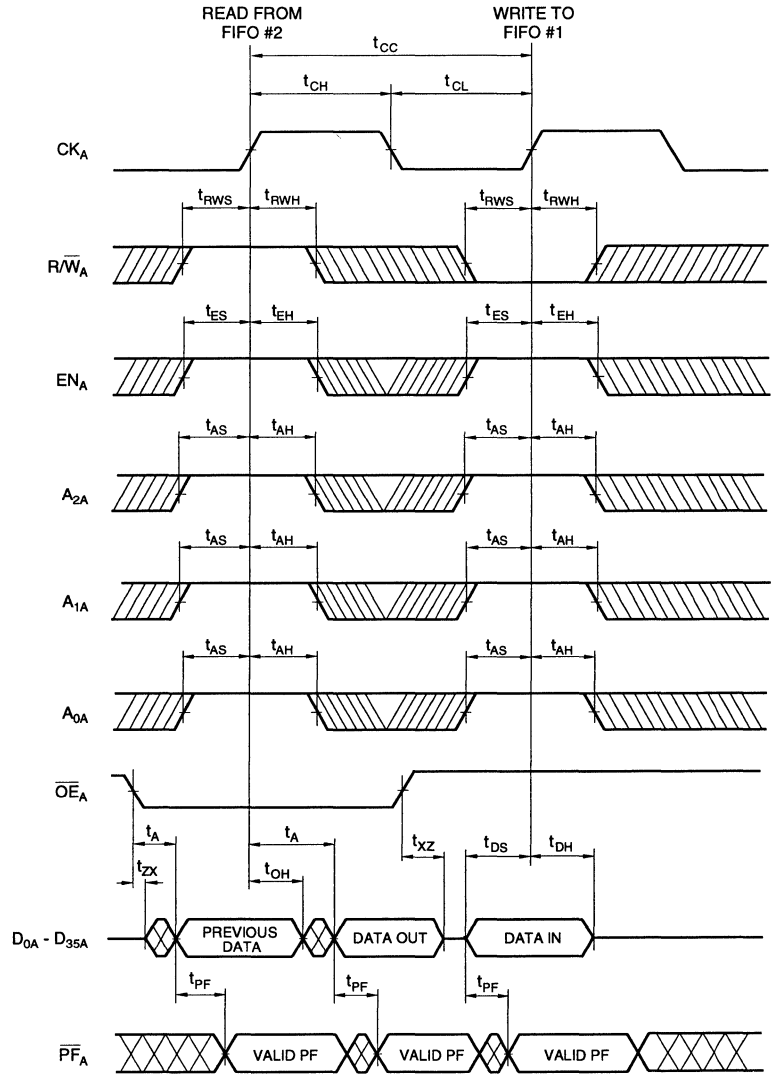
NOTES:

1. t_{RSS}, t_{RSH} need not be met unless the rising edge of CK_A or CK_B occurs while that clock is enabled.
2. Port A is considered the master port for bypass operation. Thus, CK_A, $R/\overline{W}_A$, and EN_A control the transmission of data between ports at reset.

543601-27

Figure 9. Data Bypass Timing

TIMING DIAGRAMS (cont'd)



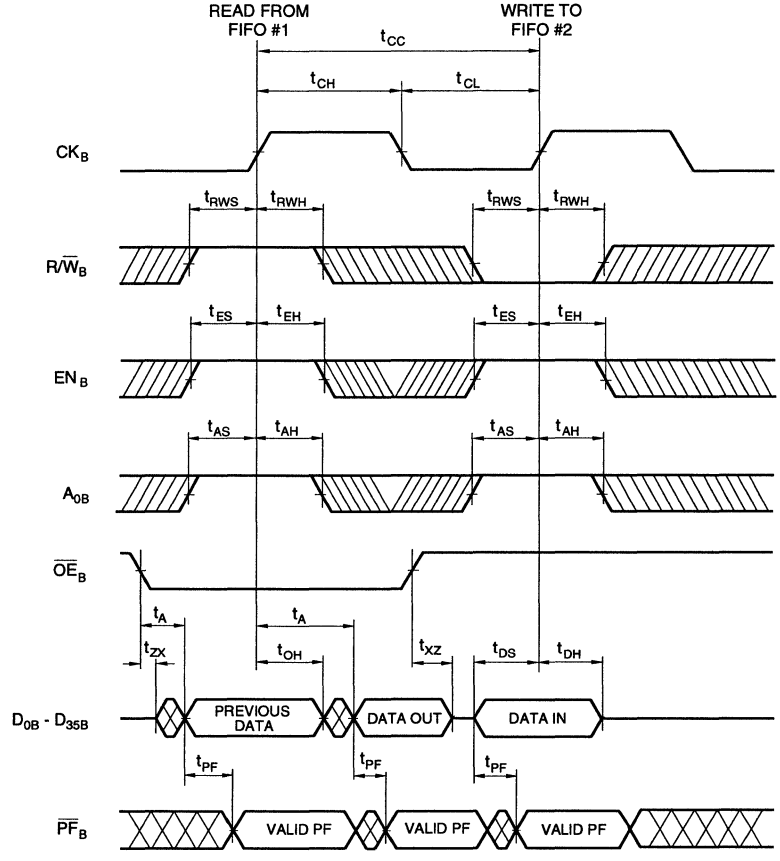
NOTES:

1. The Port A Parity Error Flag ($\overline{PF}_A$) reflects the parity status of data present on the data bus.
2. The status of $\overline{OE}_A$ does not gate read or write operations.
3. If $\overline{OE}_A$ is left LOW during a write operation, then the previous data held in the output latch is written back into FIFO #1.

543601-24

Figure 10. Port A FIFO Read/Write

TIMING DIAGRAMS (cont'd)



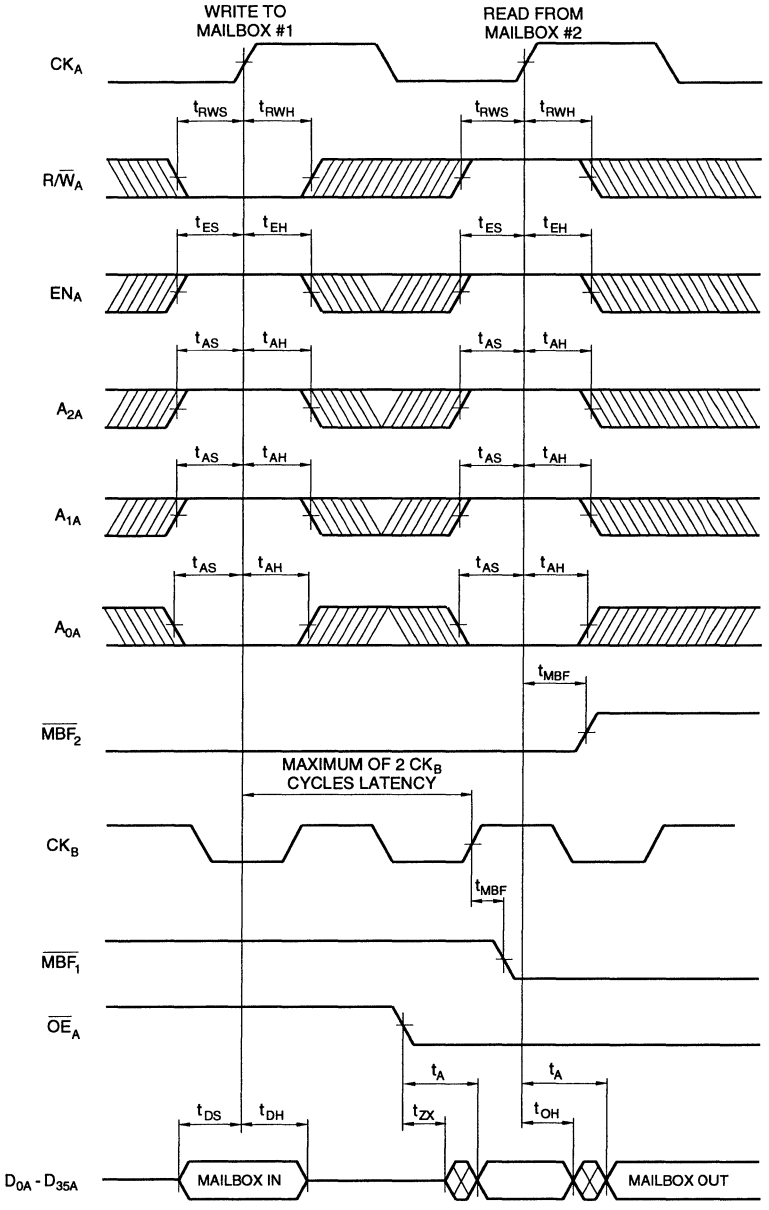
NOTES:

1. The Port B Parity Error Flag ($\overline{PF}_B$) reflects the parity status of data present on the data bus.
2. The status of $\overline{OE}_B$ does not gate read or write operations.
3. If $\overline{OE}_B$ is left LOW during a write operation, then the previous data held in the output latch is written back into FIFO #2.

543601-25

Figure 11. Port B FIFO Read/Write

TIMING DIAGRAMS (cont'd)



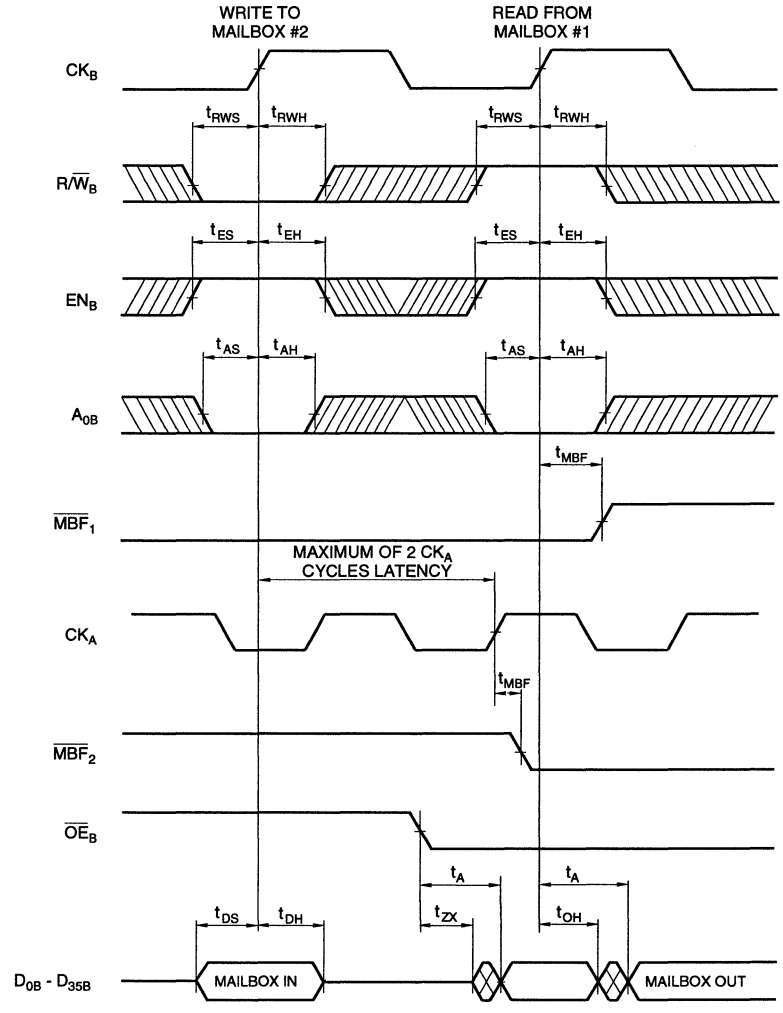
NOTES:

1. Both edges of $\overline{MBF_2}$ are synchronized to the Port A clock, CK_A.
2. Both edges of $\overline{MBF_1}$ are synchronized to the Port B clock, CK_B.
3. There is a maximum of two CK_B clock cycles of synchronization latency before $\overline{MBF_1}$ is asserted to indicate valid new mailbox data.
4. The status of mailbox flags does not prevent mailbox read or write operations.

543601-22

Figure 12. Port A Mailbox Access

TIMING DIAGRAMS (cont'd)



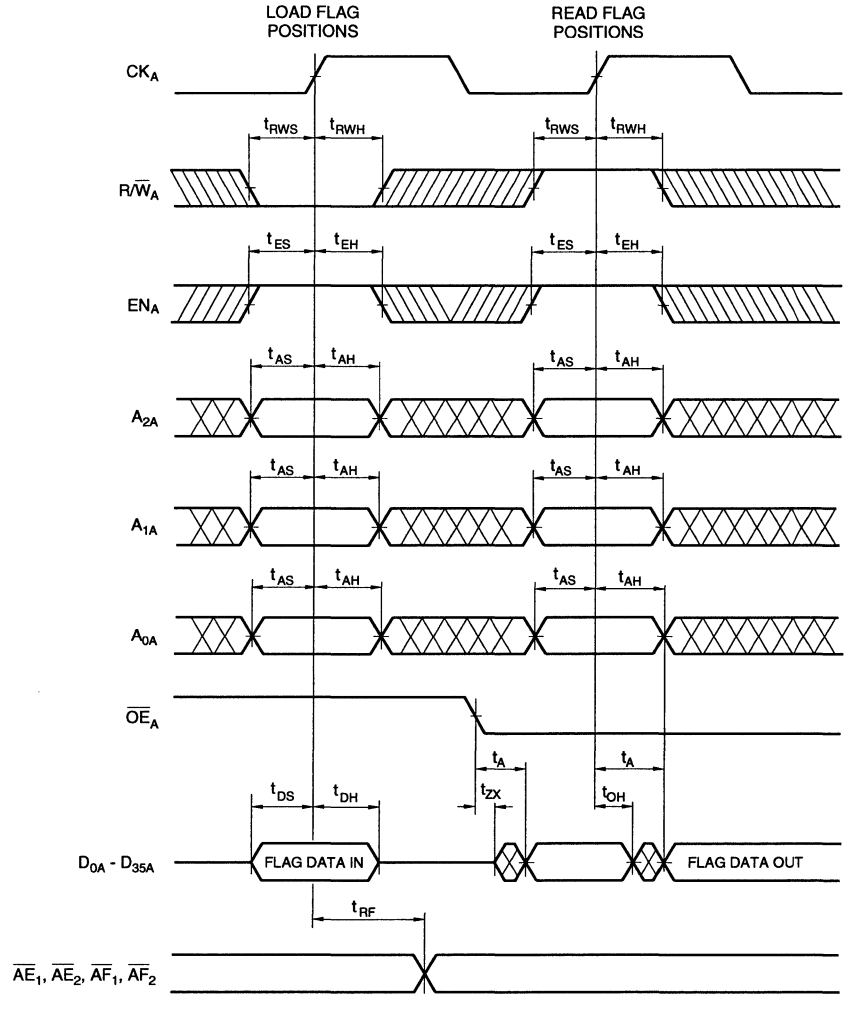
NOTES:

1. Both edges of $\overline{MBF}_2$ are synchronized to the Port A clock, CK_A.
2. Both edges of $\overline{MBF}_1$ are synchronized to the Port B clock, CK_B.
3. There is a maximum of two CK_A clock cycles of synchronization latency before $\overline{MBF}_2$ is asserted to indicate valid new mailbox data.
4. The status of mailbox flags does not prevent mailbox read or write operations.

543601-23

Figure 13. Port B Mailbox Access

TIMING DIAGRAMS (cont'd)



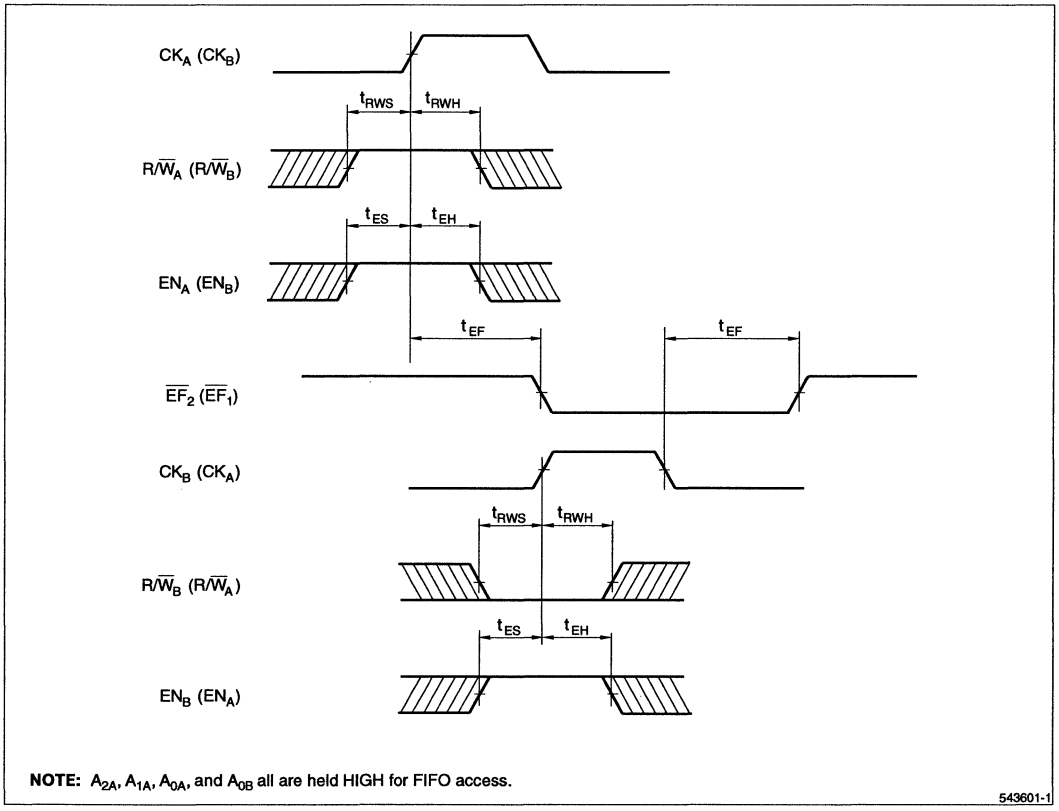
NOTES:

1. For valid flag address codes and data formats, see Table 3.
2. If flag status is altered by flag programming, the updated flags will be valid within a time t_{RF}.

543601-18

Figure 14. Flag Programming

TIMING DIAGRAMS (cont'd)

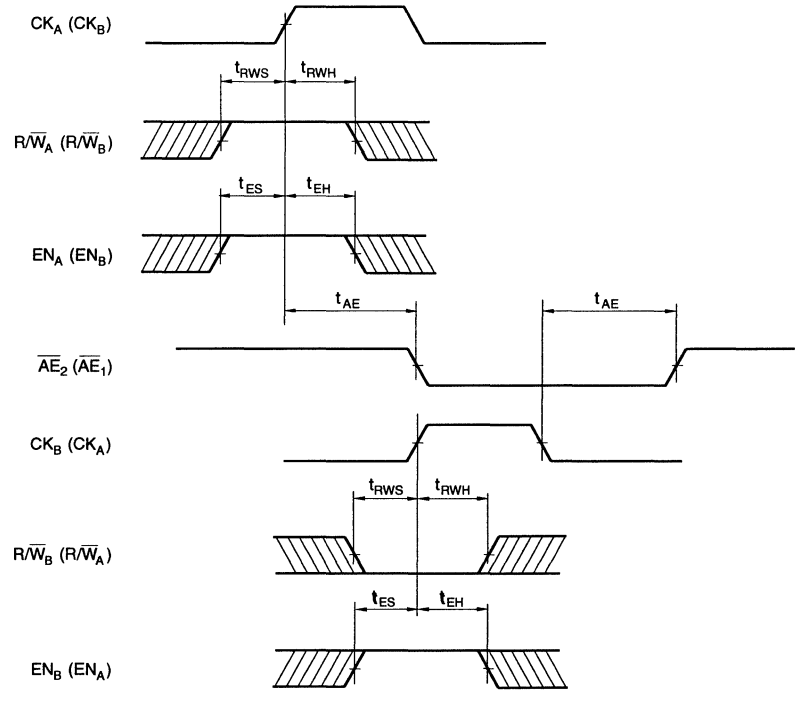


NOTE: A_{2A}, A_{1A}, A_{0A}, and A_{0B} all are held HIGH for FIFO access.

543601-1

Figure 15. Empty Flag Timing

TIMING DIAGRAMS (cont'd)

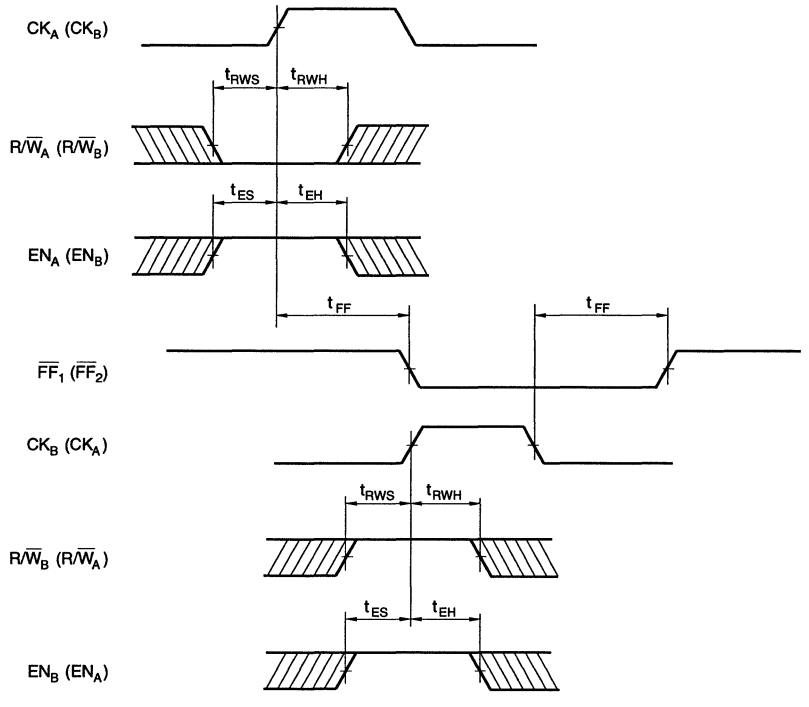


NOTE: A_{2A}, A_{1A}, A_{0A}, and A_{0B} all are held HIGH for FIFO access.

543601-2

Figure 16. Almost-Empty Flag Timing

TIMING DIAGRAMS (cont'd)

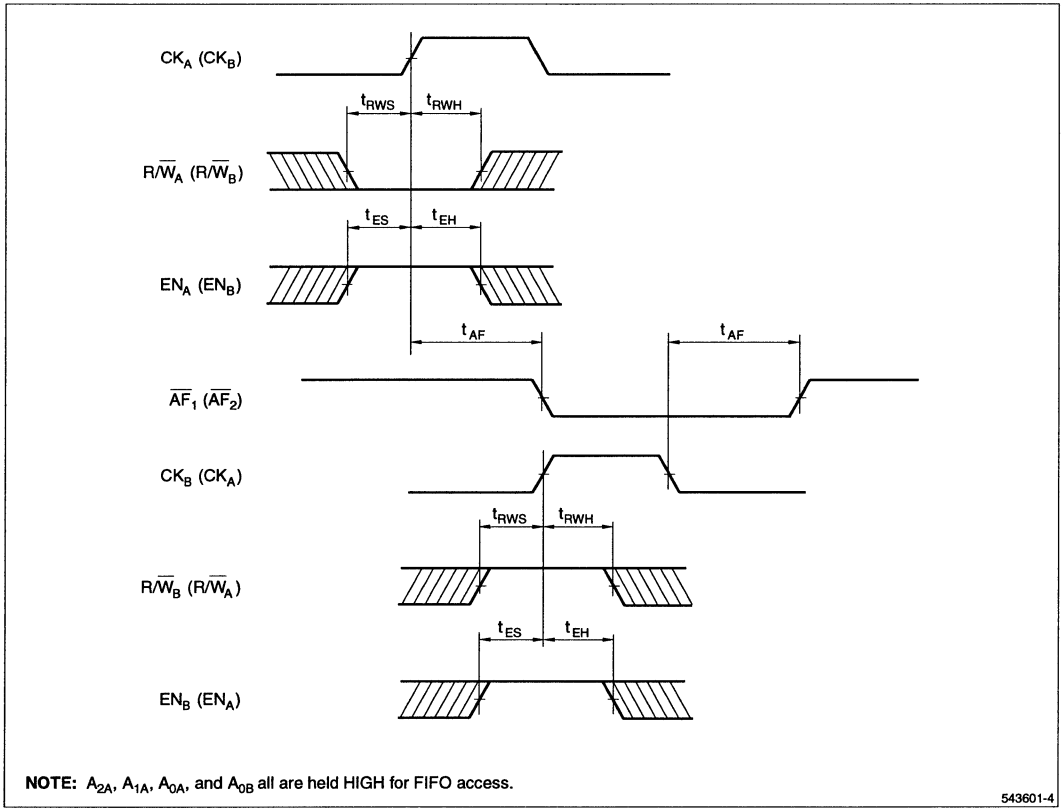


NOTE: A_{2A}, A_{1A}, A_{0A}, and A_{0B} all are held HIGH for FIFO access.

543601-3

Figure 17. Full Flag Timing

TIMING DIAGRAMS (cont'd)

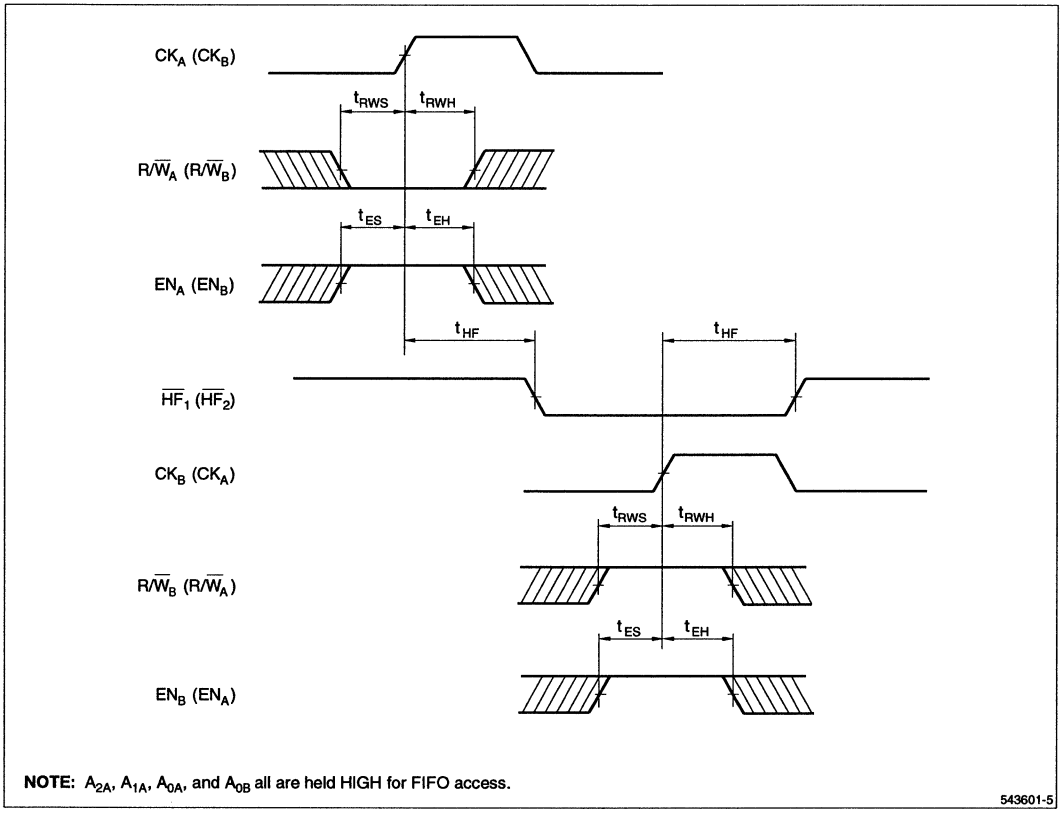


NOTE: A_{2A}, A_{1A}, A_{0A}, and A_{0B} all are held HIGH for FIFO access.

543601-4

Figure 18. Almost-Full Flag Timing

TIMING DIAGRAMS (cont'd)

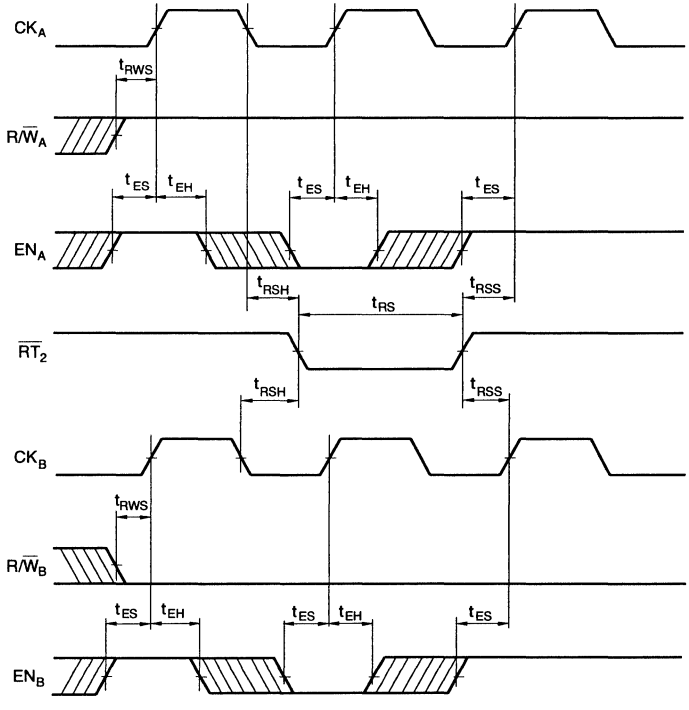


NOTE: A_{2A}, A_{1A}, A_{0A}, and A_{0B} all are held HIGH for FIFO access.

543601-5

Figure 19. Half-Full Flag Timing

TIMING DIAGRAMS (cont'd)



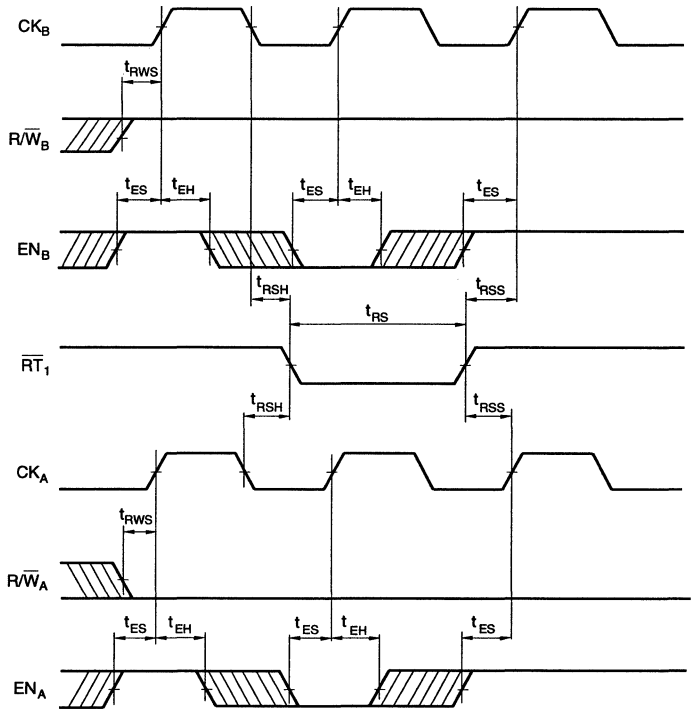
NOTES:

1. t_{RSS} and t_{RSH} need not be met unless a rising edge of CK_A or CK_B occurs while that clock is enabled.
2. t_{RSS} is the time needed to deassert $\overline{RT}_2$ before returning to a normal FIFO cycle.
3. t_{RSH} is the time needed before asserting $\overline{RT}_2$ after a normal FIFO cycle.

543601-20

Figure 20. FIFO #2 Retransmit

TIMING DIAGRAMS (cont'd)



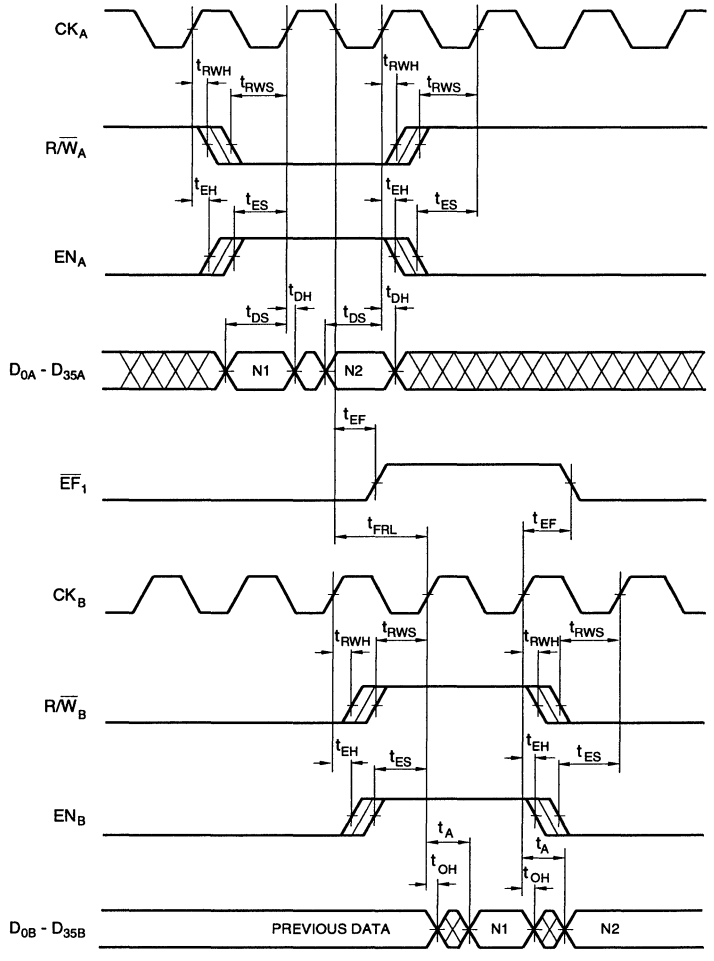
NOTES:

1. t_{RSS} and t_{RSH} need not be met unless a rising edge of CK_A or CK_B occurs while that clock is enabled.
2. t_{RSS} is the time needed to deassert $\overline{RT}_1$ before returning to a normal FIFO cycle.
3. t_{RSH} is the time needed before asserting $\overline{RT}_1$ after a normal FIFO cycle.

543601-21

Figure 21. FIFO #1 Retransmit

TIMING DIAGRAMS (cont'd)



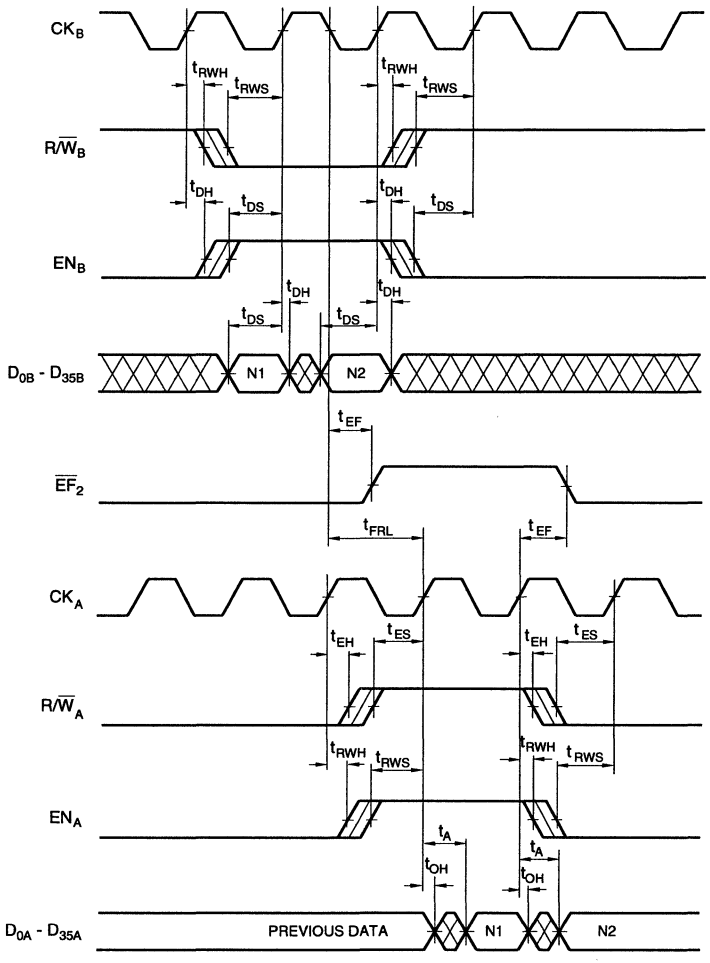
NOTES:

1. A_{2A}, A_{1A}, A_{0A}, and A_{0B} are all held HIGH for FIFO access.
2. $\overline{OE}_A$ is held HIGH.
3. $\overline{OE}_B$ is held LOW.
4. t_{FRL} (First Read Latency) - The first read following an empty condition may begin no earlier than t_{FRL} after the first write to an empty FIFO, to ensure that valid read data is retrieved.

543601-16

Figure 22. FIFO #1 Write and Read Operation in Near-Empty Region

TIMING DIAGRAMS (cont'd)



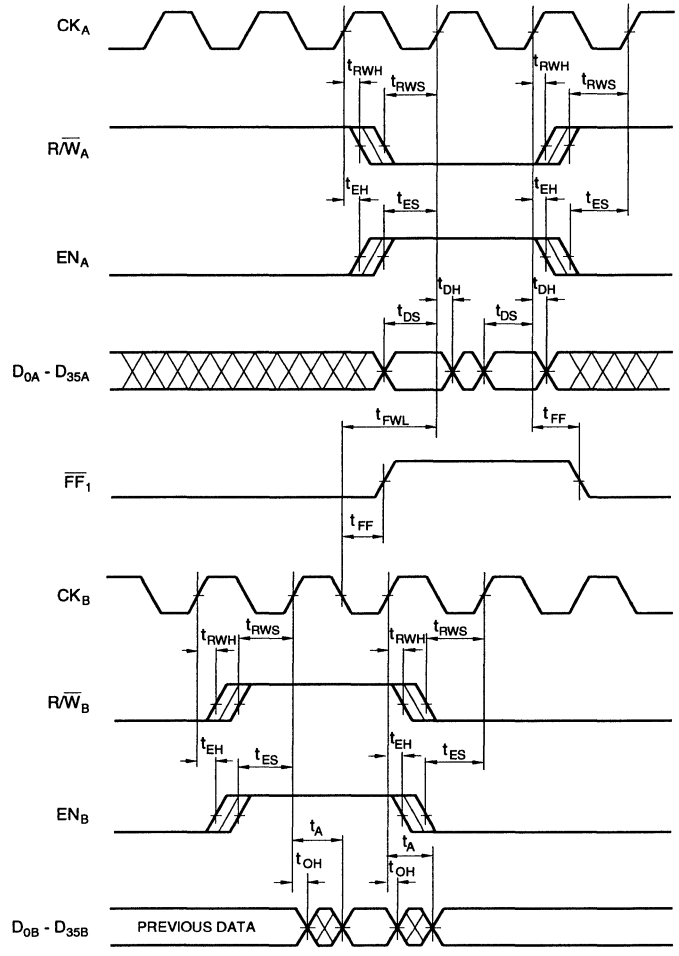
NOTES:

1. $\overline{A_{2A}}$, A_{1A}, A_{0A}, and A_{0B} are all held HIGH for FIFO access.
2. $\overline{OE}_A$ is held HIGH.
3. $\overline{OE}_B$ is held LOW.
4. t_{FRL} (First Read Latency) - The first read following an empty condition may begin no earlier than t_{FRL} after the first write to an empty FIFO, to ensure that valid read data is retrieved.

543601-17

Figure 23. FIFO #2 Write and Read Operation in Near-Empty Region

TIMING DIAGRAMS (cont'd)



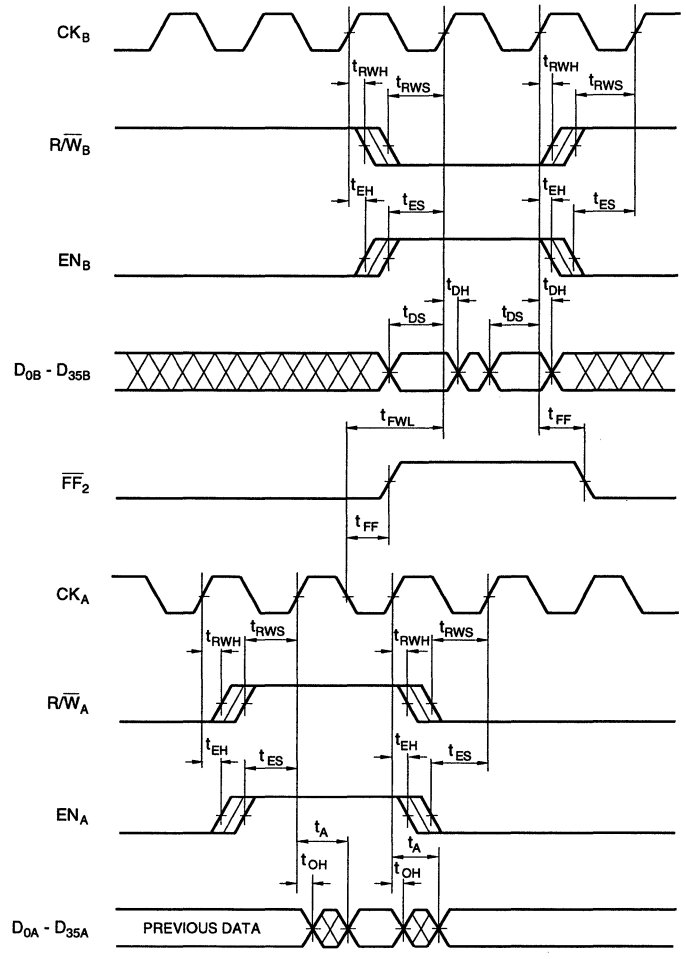
NOTES:

1. A_{2A}, A_{1A}, A_{0A}, and A_{0B} are all held HIGH for FIFO access.
2. $\overline{OE}_A$ is held HIGH.
3. $\overline{OE}_B$ is held LOW.
4. t_{FWL} (First Write Latency) - The first write following a full condition may begin no earlier than t_{FWL} after the first read from a full FIFO, to ensure that valid write data is written.

543601-14

Figure 24. FIFO #1 Read and Write Operation in Near-Full Region

TIMING DIAGRAMS (cont'd)



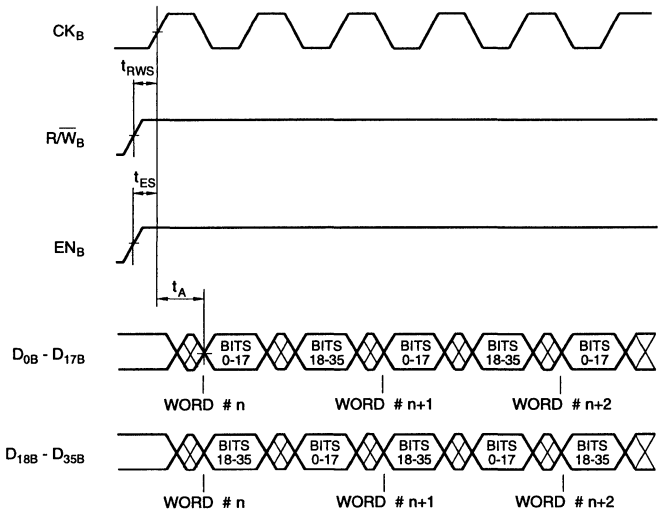
NOTES:

1. A_{2A}, A_{1A}, A_{0A}, and A_{0B} are all held HIGH for FIFO access.
2. $\overline{OE}_A$ is held LOW.
3. $\overline{OE}_B$ is held HIGH.
4. t_{FWL} (First Write Latency) - The first write following a full condition may begin no earlier than t_{FWL} after the first read from a full FIFO, to ensure that valid write data is written.

543601-15

Figure 25. FIFO #2 Read and Write Operation in Near-Full Region

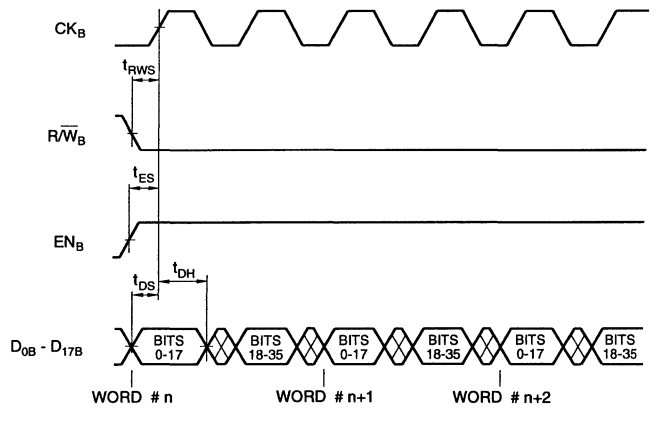
TIMING DIAGRAMS (cont'd)



NOTES:
1. $\overline{A_{0B}}$ is held HIGH for FIFO access.
2. $\overline{OE_B}$ is held LOW.
3. WS_0 is held HIGH and WS_1 is held LOW for double-byte access.

543601-13

Figure 26. Port B Double-Byte FIFO #1 Read Access for 36-to-18 Funneling

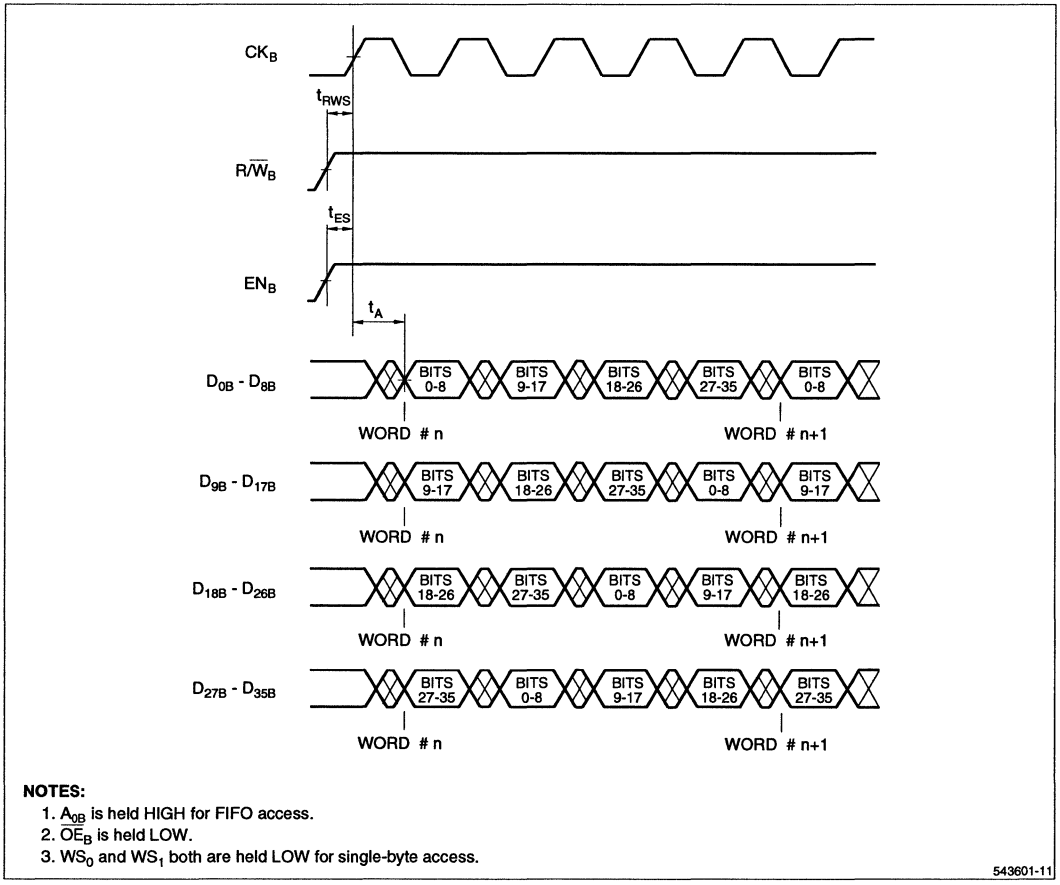


NOTES:
1. $\overline{A_{0B}}$ is held HIGH for FIFO access.
2. $\overline{OE_B}$ is held HIGH.
3. WS_0 is held HIGH and WS_1 is held LOW for double-byte access.

543601-12

Figure 27. Port B Double-Byte FIFO #2 Write Access for 18-to-36 Defunneling

TIMING DIAGRAMS (cont'd)

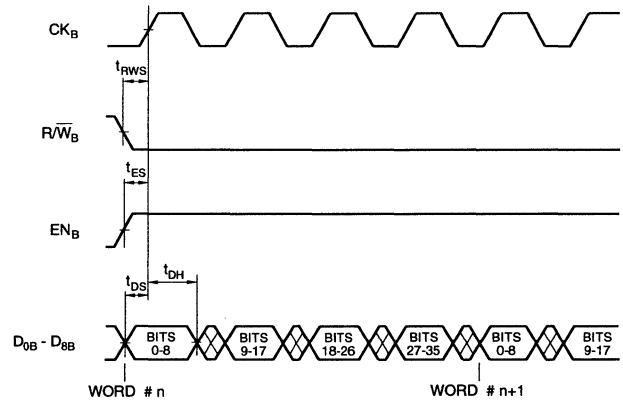


NOTES:
1. A_{0B} is held HIGH for FIFO access.
2. $\overline{OE}_B$ is held LOW.
3. WS_0 and WS_1 both are held LOW for single-byte access.

543601-11

Figure 28. Port B Single-Byte FIFO #1 Read Access for 36-to-9 Funneling

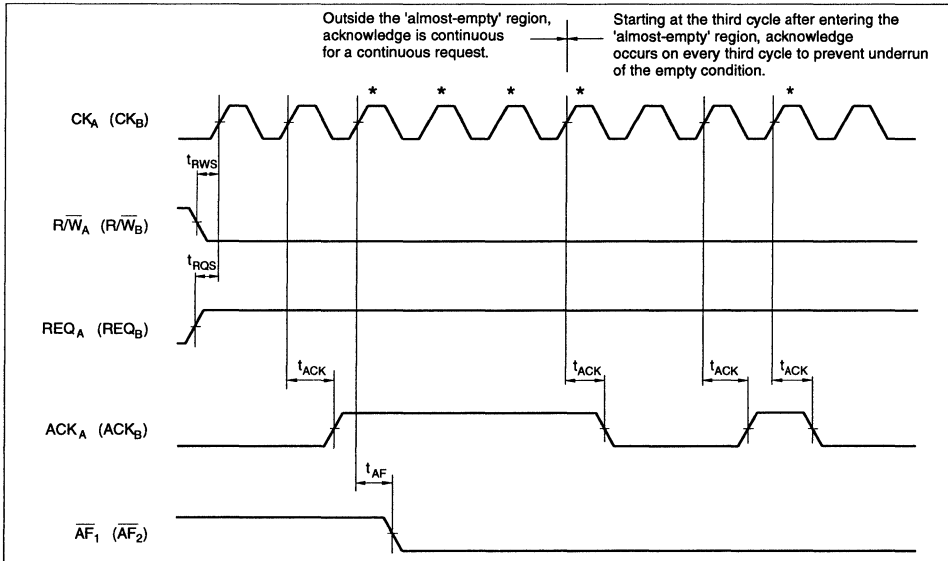
TIMING DIAGRAMS (cont'd)



NOTES:
1. A_{0B} is held HIGH for FIFO access.
2. $\overline{OE}_B$ is held HIGH.
3. WS_0 and WS_1 both are held LOW for single-byte access.

543601-10

Figure 29. Port B Single-Byte FIFO #2 Write Access for 9-to-36 Defunneling

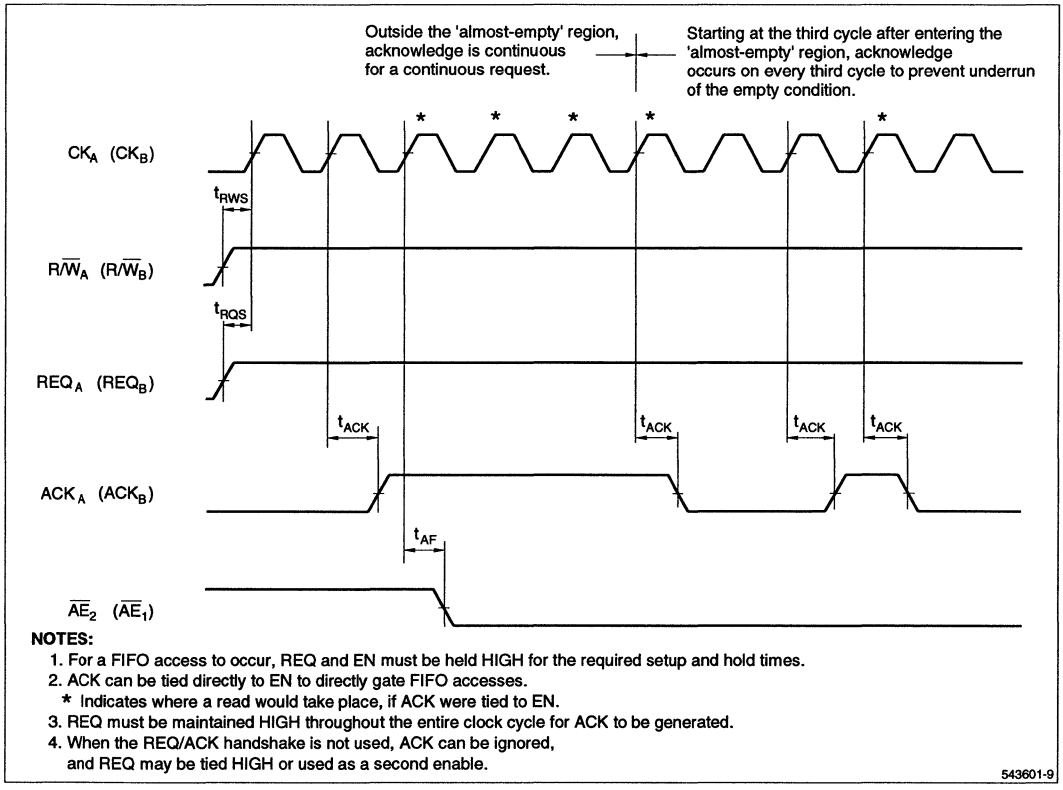


NOTES:
1. For a FIFO access to occur, REQ and EN must be held HIGH for the required setup and hold times.
2. ACK can be tied directly to EN to directly gate FIFO accesses.
   * Indicates where a write would take place, if ACK were tied to EN.
3. REQ must be maintained HIGH throughout the entire clock cycle for ACK to be generated.
4. When the REQ/ACK handshake is not used, ACK can be ignored, and REQ may be tied HIGH or used as a second enable.

543601-8

Figure 30. Write Request/Acknowledge Handshake

TIMING DIAGRAMS (cont'd)



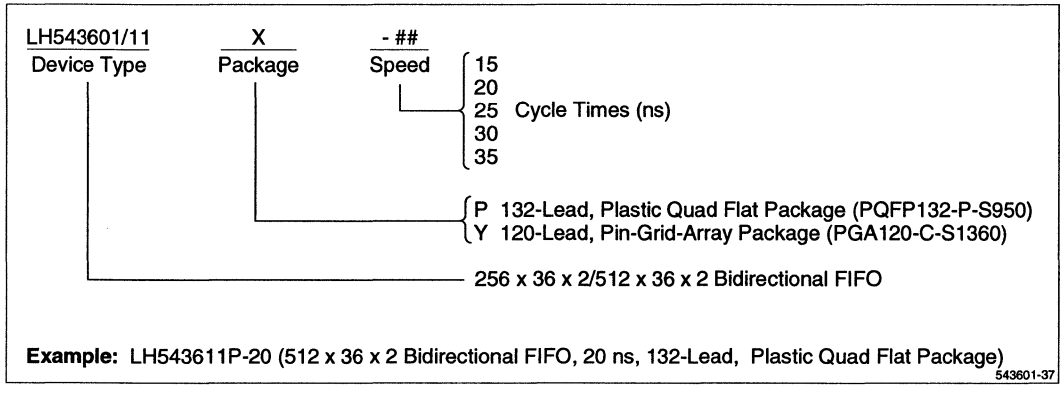
NOTES:

1. For a FIFO access to occur, REQ and EN must be held HIGH for the required setup and hold times.
2. ACK can be tied directly to EN to directly gate FIFO accesses.
   * Indicates where a read would take place, if ACK were tied to EN.
3. REQ must be maintained HIGH throughout the entire clock cycle for ACK to be generated.
4. When the REQ/ACK handshake is not used, ACK can be ignored, and REQ may be tied HIGH or used as a second enable.

543601-9

Figure 31. Read Request/Acknowledge Handshake

ORDERING INFORMATION



Example: LH543611P-20 (512 x 36 x 2 Bidirectional FIFO, 20 ns, 132-Lead, Plastic Quad Flat Package)

543601-37

LH543620

ADVANCE INFORMATION

1024 × 36 Synchronous FIFO

FEATURES

- Fast Cycle Times: 20/25/30 ns
- Selectable 36/18/9-Bit Word Width for Both Input Port and Output Port
- Byte-Order-Reversal Function (i.e., 'Big-Endian' ↔ 'Little-Endian' Conversion)
- 16-mA-I_{OL} Three-State Outputs
- Automatic Byte Parity Checking
- Selectable Byte Parity Generation
- Five Status Flags: Full, Almost-Full, Half-Full, Almost-Empty, and Empty
- Programmed Values may be entered from either Port
- Two Enable Control Signals for each Port
- Mailbox Register with Synchronized Flags
- Asynchronous Data-Bypass Function
- Data-Retransmit Function
- Configurable for Paralleled FIFO Operation (72-Bit Data Width)
- PQFP-to-PGA Package Conversion *
- Package: Space-Saving PQFP

* For PQFP-to-PGA conversion for thru-hole board designs, Sharp recommends ITT Pomona Electronics' SMT/PGA Generic Converter model #5853®. This converter maps the LH543620 132-pin PQFP to a generic 13 x 13, 132-pin PGA (100-mil pitch). For more information, contact Sharp or ITT Pomona Electronics at 1500 East Ninth Street, Pomona, CA 91766, (909) 469-2900.

FUNCTIONAL DESCRIPTION

The LH543620 is a FIFO (First-In, First-Out) memory device, based on fully-static CMOS RAM technology, capable of containing up to 1024 36-bit words. It can replace four or more nine-bit-wide FIFOs in many applications.

The input port and the output port operate independently of each other. Write operations are performed on the rising edge of the input clock CKI, and enabled by two enabled signals ENI_1, ENI_2. Read operations are performed on the rising edge of the output clock CKO and enabled by two enabled signals ENO_1, ENO_2.

Five status flags are available to monitor the memory array status: Full, Almost-Full, Half-Full, Almost-Empty, and Empty. The Almost-Full and Almost-Empty flags are initialized to a default offset of eight locations from their respective boundaries, but they are each programmable over the entire FIFO depth.

Both the input port and the output port may be set independently to operate at three data-word widths: 36 bits, 18 bits, or 9 bits. This setting may be changed during system operation. The LH543620 can perform Byte-Order-Reversal on the four nine-bit bytes of each 36-bit data word passing through it, thus accomplishing 'Big Endian' ↔ 'Little Endian' conversion.

When data is read out of the FIFO a byte-parity check is performed. The parity flag is used to indicate that a parity error was detected in one of the 9-bit bytes of the output word.

Parity generation, when selected, creates the parity bit of each 8-bit byte of the input word. The result is written into the MSB-bit of each 9-bit byte, overwriting the previous contents of the bit. The default is odd parity. However, the FIFO may be programmed to use even parity.

The LH543620 has a data-bypass mode that connects the output port to the input port asynchronously. A mailbox facility with Synchronized Flags is provided from the input port to the output port.

The LH543620's 'Smart-Retransmit' capability sets the internal-memory read pointer to any arbitrary memory location. The 'Smart-Retransmit' capability includes a Marking Function and a Programmable Offset to support data communication and digital signal processing applications.

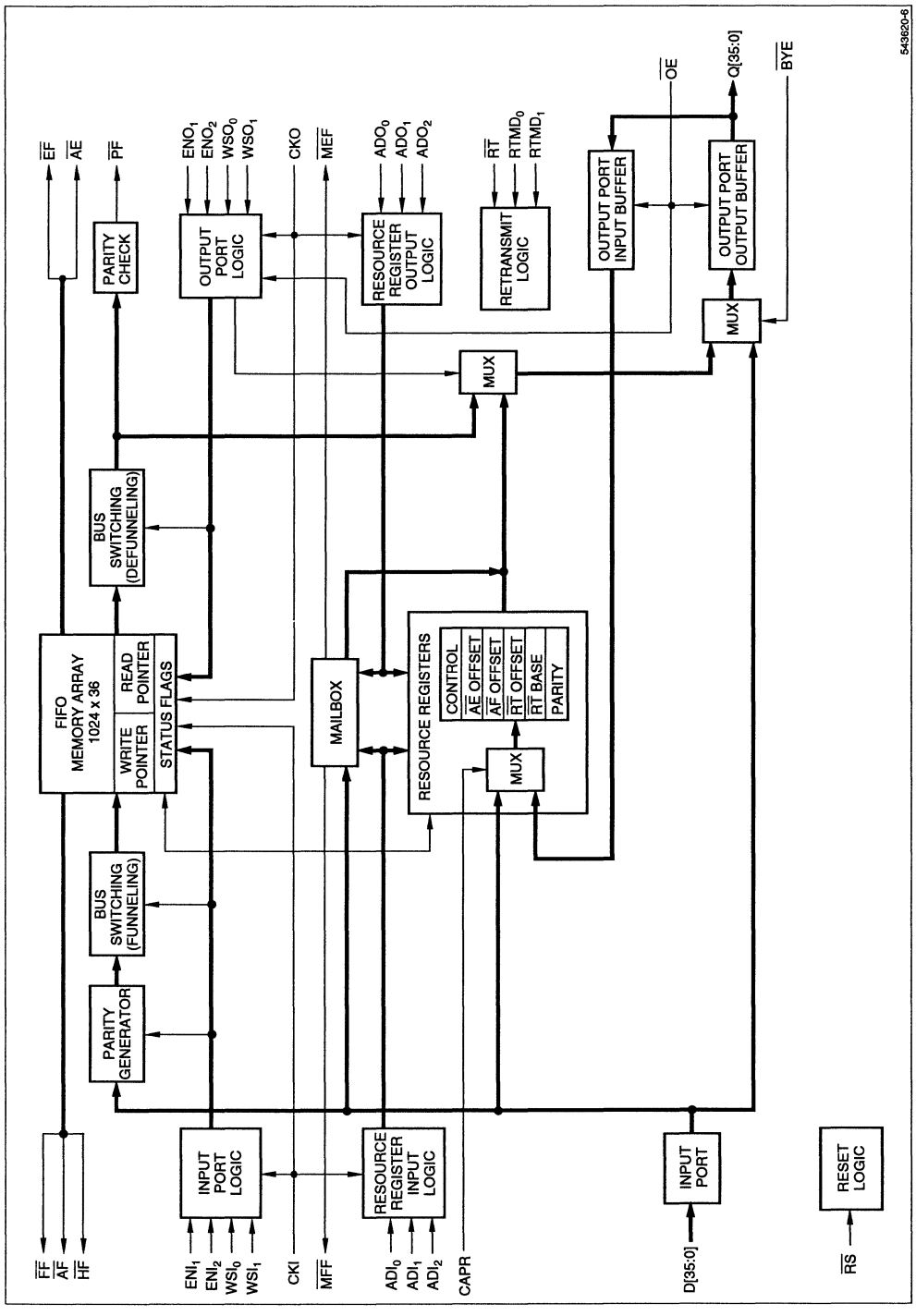


Figure 1. LH543620 Block Diagram

PIN DESCRIPTIONS (SUMMARY)

PIN NAME	PIN TYPE *	DESCRIPTION
DATABUS		
D[35:0]	I	36-Bit Input-Port Databus
Q[15:0]	I/O/Z	Three-State 36-Bit Output-Port Databus
Q[35:16]	O/Z	
CLOCKS		
CKI	I	Input-Port Clock
CKO	I	Output-Port Clock
ASYNCHRONOUS CONTROL		
$\overline{RS}$	I	Master Reset
$\overline{OE}$	I	Output Enable
$\overline{BYE}$	I	Data-Bypass Enable
CAPR	I	Command-Address Port Reference
CONTROL SIGNALS SYNCHRONOUS TO THE INPUT CLOCK		
ENI_1,ENI_2	I	Input-Port Enables
ADI[2:0]	I	Input-Port Address
WSI[1:0]	I	Input-Port Word-Width-Selection Address Field
STATUS FLAGS SYNCHRONOUS TO THE INPUT CLOCK		
$\overline{FF}$	O	Full Flag
$\overline{AF}$	O	Almost-Full Flag
$\overline{HF}$ [1]	O	Half-Full Flag
$\overline{MFF}$	O	Mailbox-Full Flag

PIN NAME	PIN TYPE *	DESCRIPTION
CONTROL SIGNALS SYNCHRONOUS TO THE OUTPUT CLOCK		
ENO_1,ENO_2	I	Output-Port Enables
ADO[2:0]	I	Output-Port Address Field
WSO[1:0]	I	Output-Port Word-Width-Selection Address Field
RTMD[1:0]	I	Retransmit Mode Control
$\overline{RT}$	I	Retransmit
STATUS FLAGS SYNCHRONOUS TO THE OUTPUT CLOCK		
$\overline{AE}$	O	Almost-Empty Flag
$\overline{EF}$	O	Empty Flag
$\overline{PF}$	O	Parity-Error Flag
$\overline{MEF}$	O	Mailbox-Empty Flag
VOLTAGES AND GROUNDS		
V_{CC}	V	Positive Power for Internal Logic
V_{CCO}	V	Positive Power for Output Drivers
V_{SS}	V	Ground for Internal Logic
V_{SSO}	V	Ground for Output Drivers

* I = Input, O = Output, V = Voltage, Z = High-Impedance

1. The half-full flag is user-selectable to be synchronized to either CKI or CKO.

PIN CONNECTIONS

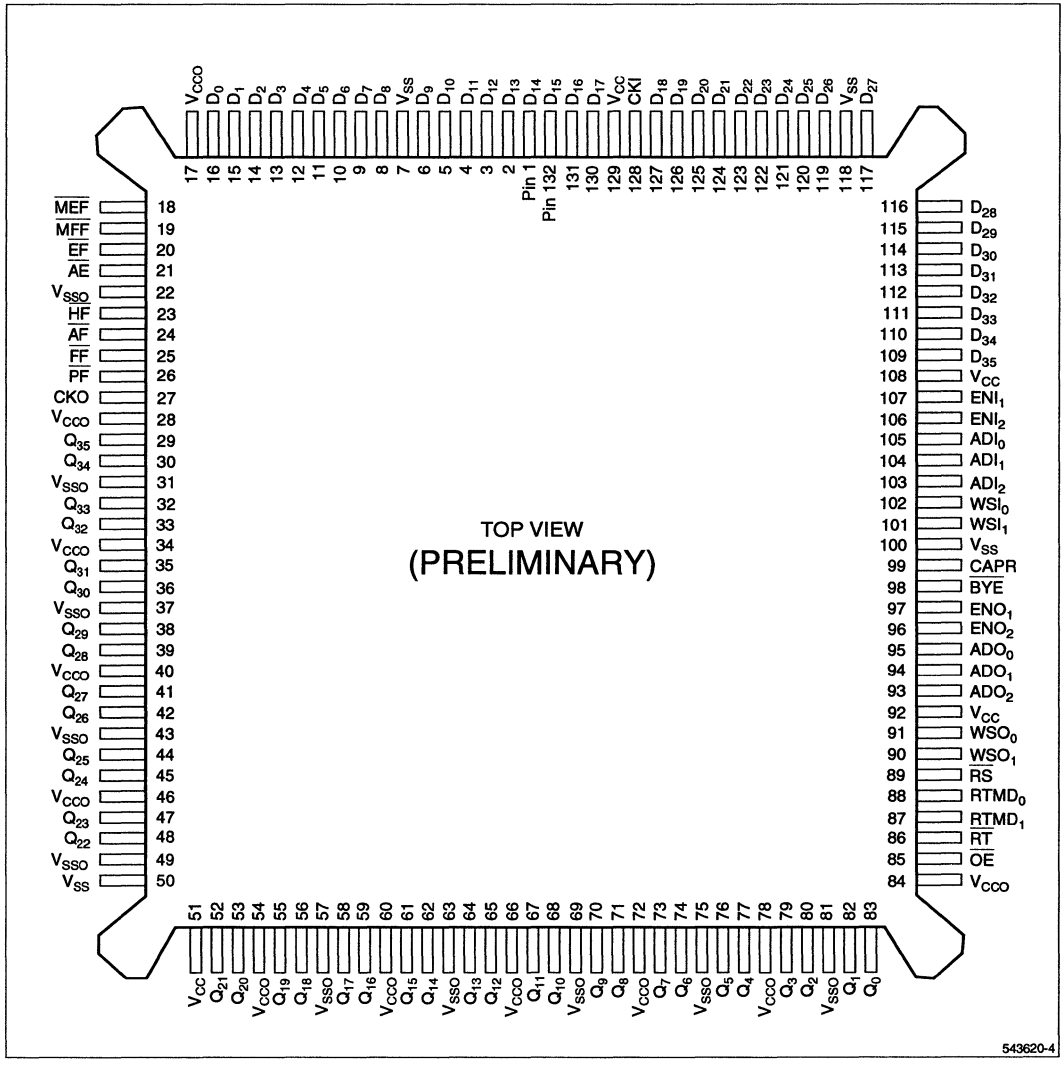


Figure 2. LH543620 1024 × 36 FIFO PQFP Package

PIN LIST

PIN NAME	PIN NO.
D_{14}	1
D_{13}	2
D_{12}	3
D_{11}	4
D_{10}	5
D_9	6
D_8	8
D_7	9
D_6	10
D_5	11
D_4	12
D_3	13
D_2	14
D_1	15
D_0	16
$\overline{MEF}$	18
$\overline{MFF}$	19
$\overline{EF}$	20
$\overline{AE}$	21
$\overline{HF}$	23
$\overline{AF}$	24
$\overline{FF}$	25
$\overline{PF}$	26
CKO	27
Q_{35}	29
Q_{34}	30
Q_{33}	32
Q_{32}	33
Q_{31}	35
Q_{30}	36
Q_{29}	38
Q_{28}	39
Q_{27}	41
Q_{26}	42
Q_{25}	44
Q_{24}	45
Q_{23}	47
Q_{22}	48
Q_{21}	52
Q_{20}	53
Q_{19}	55
Q_{18}	56
Q_{17}	58
Q_{16}	59

PIN NAME	PIN NO.
Q_{15}	61
Q_{14}	62
Q_{13}	64
Q_{12}	65
Q_{11}	67
Q_{10}	68
Q_9	70
Q_8	71
Q_7	73
Q_6	74
Q_5	76
Q_4	77
Q_3	79
Q_2	80
Q_1	82
Q_0	83
$\overline{OE}$	85
$\overline{RT}$	86
$RTMD_1$	87
$RTMD_0$	88
$\overline{RS}$	89
WSO_1	90
WSO_0	91
ADO_2	93
ADO_1	94
ADO_0	95
ENO_2	96
$EN0_1$	97
$\overline{BYE}$	98
CAPR	99
WSI_1	101
WSI_0	102
ADI_2	103
ADI_1	104
ADI_0	105
ENI_2	106
ENI_1	107
D_{35}	109
D_{34}	110
D_{33}	111
D_{32}	112
D_{31}	113
D_{30}	114
D_{29}	115

PIN NAME	PIN NO.
D_{28}	116
D_{27}	117
D_{26}	119
D_{25}	120
D_{24}	121
D_{23}	122
D_{22}	123
D_{21}	124
D_{20}	125
D_{19}	126
D_{18}	127
CKI	128
D_{17}	130
D_{16}	131
D_{15}	132
V_{SS}	7
V_{CCQ}	17
V_{SSQ}	22
V_{CCQ}	28
V_{SSQ}	31
V_{CCQ}	34
V_{SSQ}	37
V_{CCQ}	40
V_{SSQ}	43
V_{CCQ}	46
V_{SSQ}	49
V_{SS}	50
V_{CC}	51
V_{CCQ}	54
V_{SSQ}	57
V_{CCQ}	60
V_{SSQ}	63
V_{CCQ}	66
V_{SSQ}	69
V_{CCQ}	72
V_{SSQ}	75
V_{CCQ}	78
V_{SSQ}	81
V_{CCQ}	84
V_{CC}	92
V_{SS}	100
V_{CC}	108
V_{SS}	118
V_{CC}	129

ABSOLUTE MAXIMUM RATINGS [1]

PARAMETER	RATING
Supply Voltage to V_{SS} Potential	−0.5 V to 7 V
Signal Pin Voltage to V_{SS} Potential [2]	−0.5 V to V_{CC} + 0.5 V
DC Output Current [3]	±75 mA
Storage Temperature Range	−65°C to 150°C
Power Dissipation (Package Limit)	2 Watts (Quad Flat Pack)

NOTES:

1. Stresses greater than those listed under 'Absolute Maximum Ratings' may cause permanent damage to the device. This is a stress rating for transient conditions only. Functional operation of the device at these or any other conditions outside those indicated in the 'Operating Range' of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Negative undershoot of 1.5 V in amplitude is permitted for up to 10 ns, once per cycle.
3. Outputs should not be shorted for more than 30 seconds. No more than one output should be shorted at any time.

OPERATING RANGE

SYMBOL	PARAMETER	MIN	MAX	UNIT
T_A	Temperature, Ambient	0	70	°C
V_{CC}	Supply Voltage	4.5	5.5	V
V_{SS}	Supply Voltage	0	0	V
V_{IL}	Logic LOW Input Voltage [1]	−0.5	0.8	V
V_{IH}	Logic HIGH Input Voltage	2.2	Vcc + 0.5	V

NOTE:

1. Negative undershoot of 1.5 V in amplitude is permitted for up to 10 ns, once per cycle.

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
I_{LI}	Input Leakage Current	V_{CC} = 5.5 V, V_{IN} = 0 V To V_{CC}	−10	10	µA
I_{LO}	I/O Leakage Current	$\overline{OE} \geq V_{IH}$, 0 V ≤ $V_{OUT} \leq V_{CC}$	−10	10	µA
V_{OL}	Logic LOW Output Voltage	I_{OL} = 16.0 mA		0.4	V
V_{OH}	Logic HIGH Output Voltage	I_{OH} = −8.0 mA	2.4		V
I_{CC}	Average Supply Current [1]	Measured at f_C = maximum		280	mA
I_{CC2}	Average Standby Supply Current [1]	All Inputs = V_{IHMIN} (Clock idle)		75	mA
I_{CC3}	Power-Down Supply Current [1]	All Inputs = V_{CC}, Outputs – open, Control – deasserted, Clocks = V_{CC}		1.0	mA

NOTE:

1. I_{CC}, I_{CC2}, and I_{CC3} are dependent upon actual output loading, and I_{CC} is also dependent on cycle times. Specified values are with outputs open; and, for I_{CC}, operating at minimum cycle times.

AC TEST CONDITIONS

PARAMETER	RATING
Input Pulse Levels	V_{SS} to 3 V
Input Rise and Fall Times (10% to 90%)	3 ns
Output Reference Levels	1.5 V
Input Timing Reference Levels	1.5 V
Output Load, Timing Tests	Figure 3

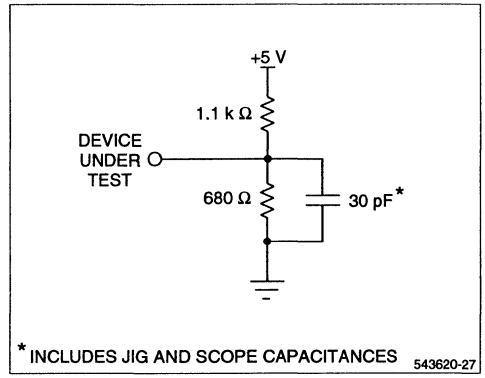


Figure 3. Output Load Circuit

CAPACITANCE [1,2]

PARAMETER	RATING
C_{IN} MAX. (Input Capacitance)	8 pF
C_{OUT} MAX. (Output Capacitance)	8 pF

NOTES:

1. Sample tested only.
2. Capacitances are maximum values at 25°C, measured at 1.0 MHz, with V_{IN} = 0 V.

AC ELECTRICAL CHARACTERISTICS [1] (See Timing Diagrams Pages 21-35)

SYMBOL	DESCRIPTION	-20		-25		-30		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_C	Clock Cycle Time	20		25		30		ns
t_{CH}	Clock HIGH Time	8		10		12		ns
t_{CL}	Clock LOW Time	9		12		14		ns
t_{DS}	Data In Setup Time	5		6		7		ns
t_{DSO}	Data Setup Time When Writing to Resource Register From Output Port	10		12		14		ns
t_{DH}	Data In Hold Time	1		1		1		ns
t_{DHO}	Data Hold Time When Writing to Resource Register From Output Port	2		2		2		ns
t_A	Data Out Access Time		14		17		21	ns
t_{OH}	Data Out Hold Time	4		5		5		ns
t_{ES}	Enable Setup Time	5		6		7		ns
t_{EH}	Enable Hold Time	1		1		1		ns
t_{OES}	Output Enable Setup Time	6		7		8		ns
t_{OEH}	Output Enable Hold Time	1		1		1		ns
t_{OL}	$\overline{OE}$ to Data Out Low-Z [2]	1		1		1		ns
t_{OZ}	$\overline{OE}$ to Data Out High-Z [2]		12		15		19	ns
t_{OE}	$\overline{OE}$ to Data Valid		14		17		21	ns
t_{EF}	Empty Flag Access Time		14		17		21	ns
t_{FF}	Full Flag Access Time		14		17		21	ns
t_{AE}	$\overline{AE}$ Flag Access Time		14		17		21	ns
t_{AF}	$\overline{AF}$ Flag Access Time		14		17		21	ns
t_{HF}	$\overline{HF}$ Flag Access Time		14		17		21	ns
t_{PF}	Parity Flag Access Time		14		17		21	ns
t_{MFF}	Mailbox $\overline{FF}$ Access Time		14		17		21	ns
t_{MEF}	Mailbox $\overline{EF}$ Access Time		14		17		21	ns
t_{AS}	Address Setup Time	9		10		11		ns
t_{AH}	Address Hold Time	1		1		1		ns
t_{WSS}	WSI and WSO Setup Time	5		6		7		ns
t_{WSH}	WSI and WSO Hold Time	1		1		1		ns
t_{RTMS}	Retransmit Mode Setup Time	5		6		7		ns
t_{RTMH}	Retransmit Mode Hold Time	1		1		1		ns
t_{RTS}	Retransmit Setup Time	5		6		7		ns
t_{RTH}	Retransmit Hold Time	1		1		1		ns
t_{RS}	Reset Pulse Width	20		25		30		ns
t_{RSR}	Reset Recovery Time [2]	10		12		15		ns
t_{RF}	Reset LOW to Flag Valid		30		35		40	ns
t_{RO}	Reset to Data Out LOW		20		25		30	ns
t_{BA}	Bypass LOW to Data Valid		14		17		21	ns
t_{BD}	Bypass Propagation Delay		14		17		21	ns
t_{SKEW1}	Skew Time Between CKO and CKI for $\overline{FF}$ [3]	14		17		21		ns
t_{SKEW2}	Skew Time Between CKI and CKO for $\overline{EF}$ [4]	14		17		21		ns
t_{SKEWM}	Skew Time Between Clock for Mailbox Flags	14		17		21		ns

NOTES:

1. Timing measurements performed at 'AC Test Condition' levels.
2. Values are guaranteed by design; not currently tested.
3. These times also apply to the Programmable-Almost-Full and Half-Full flags when they are synchronized to CKI.
4. These times also apply to the Half-Full and Programmable-Almost-Empty flags when they are synchronized to CKO.

PIN DESCRIPTIONS (FUNCTIONAL)

PIN NAME	DESCRIPTION
	DATABUS
D[35:0]	**36-bit Input-Port Databus.** The D port is the input port for the FIFO memory array, the resource registers, and the mailbox, or it may be directly connected to the output port. See Figure 4. D[35:0] is synchronous to the rising edge of CKI.
Q[35:0]	**Three-State 36-Bit Output-Port Databus.** The Q port is the output port for the FIFO memory array, the resource registers, and the mailbox, or it may be directly connected to the input port. See Figure 4. Q[35:0] is synchronous to the rising edge of CKO. The lower 16 bits of the Q port (Q[15:0]) may also be used as the input port for the resource register.
	CLOCKS
CKI	**Input-Port Clock.** CKI is a free-running waveform controlled by an oscillator. It may be irregular or asynchronous if minimum clock-HIGH times and clock-LOW times are met.
CKO	**Output-Port Clock.** CKO is a free-running waveform controlled by an oscillator. It may be irregular or asynchronous if minimum clock-HIGH times and clock-LOW times are met.

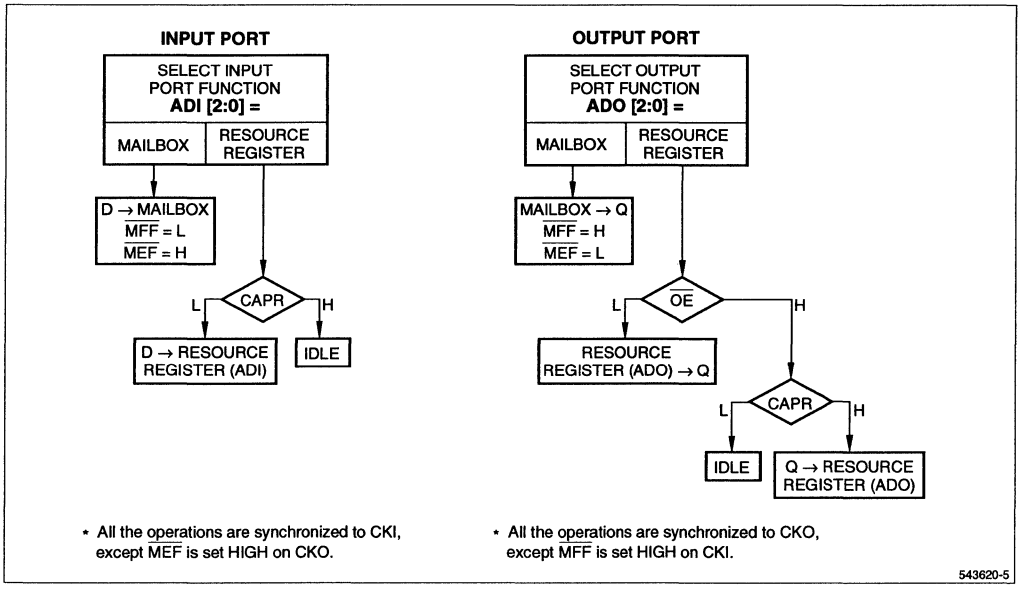


Figure 4. Resource Registers, Read and Write

PIN NAME	DESCRIPTION
	ASYNCHRONOUS CONTROL
$\overline{RS}$	**Master Reset.** When asserted LOW, the LH543620 internal resource registers are set to their default value. See Table 1. The status flags indicate Empty FIFO.
$\overline{OE}$	**Output Enable.** When asserted LOW, $\overline{OE}$ forces Q[35:0] to be active. When deasserted HIGH, $\overline{OE}$ forces Q[35:0] into a Hi-Z state. Bit 6 of the control register governs whether $\overline{OE}$ suppresses the advancement of the Read Pointer (RP). In this case, $\overline{OE}$ must obey setup time and hold time relative to CKO.
$\overline{BYE}$	**Data-Bypass Enable.** When asserted LOW, $\overline{BYE}$ connects Q[35:0] directly to D[35:0].
CAPR	**Command-Address Port Reference.** CAPR determines the source of the 16-bit word to be loaded into the resource register. Whenever CAPR is LOW, the word comes from the Input Port. Whenever CAPR is HIGH ($\overline{OE}$ is HIGH), the word comes from the Output Port. **NOTES:** 1. The destination of the resource register is always the Output Port. 2. CAPR is assumed to be a steady signal. It is not allowed to change 'on-the-fly' during operation.
	CONTROL SIGNALS SYNCHRONOUS TO THE INPUT CLOCK
ENI_1, ENI_2	**Input-Port Enables.** ENI_1 and ENI_2 are active HIGH and synchronous to the rising edge of CKI. Data is written into the FIFO memory array when both ENI_1 and ENI_2 are asserted HIGH. **NOTE:** ENI_1, ENI_2 DO NOT ENABLE writing data into the Resource Registers or the Mailbox.
ADI[2:0]	**Input-Port Address.** ADI[2:0] specifies the Input-Port destination. See Table 1. ADI[2:0] is synchronized to the rising edge of CKI.
WSI[1:0]	**Input-Port Word-Width-Selection Address Field.** WSI[1:0] selects the Input-Port Word-Width. See Table 2. WSI[1:0] is synchronous to the rising edge of CKI.

Table 1. Input-Port Address Field

ADI_2	ADI_1	ADI_0	SELECTION	DEFAULT VALUE (of the selected REGISTER)
L	L	L	RBASE register	0
L	L	H	ROFFSET register	0
L	H	L	$\overline{AF}$ offset value	8
L	H	H	Parity register	0
H	L	L	$\overline{AE}$ offset value	8
H	L	H	Control register	1
H	H	L	Mailbox	0
H	H	H	Resource registers write disabled	

Table 2. Input-Port Word-Width Selection

WSI_1	WSI_0	FUNCTION	
L	L	9-Bit Data-Path Width	Input data D[8:0]
L	H	18-Bit Data-Path Width	Input data D[17:0]
H	L	Reserved	
H	H	36-Bit Data-Path Width	Input data D[35:0]

PIN NAME	DESCRIPTION
	STATUS FLAGS SYNCHRONOUS TO THE INPUT CLOCK
$\overline{FF}$	**Full Flag.** $\overline{FF}$ is synchronous to the rising edge of CKI. When asserted LOW, 1024 36-bit words of the FIFO memory array contain meaningful data. When $\overline{FF}$ is asserted, writing data to the FIFO is disabled.
$\overline{AF}$	**Almost-Full Flag.** When asserted LOW, $\overline{AF}$ indicates that there are at most 'p' vacant 36-bit words remaining in the FIFO memory array, where 'p' is the value of the Almost-Full-Offset-Value. $\overline{AF}$ has two synchronization modes depending on Bit 5 of the control register. *Bit 5 = 0* (Default) Asynchronous Mode *Bit 5 = 1*: $\overline{AF}$ is synchronous to the rising edge of CKI.
$\overline{HF}$	**Half-Full Flag.** When asserted LOW, there are at least 513 36-bit words in the FIFO memory array. $\overline{HF}$ has three synchronization modes depending on Bits 3 and 4 of the control register. See Table 3.
$\overline{MFF}$	**Mailbox-Full Flag.** $\overline{MFF}$ is synchronized to the rising edge of CKI. When asserted LOW, it indicates that a new mail word has been placed in the mailbox.
	CONTROL SIGNALS SYNCHRONOUS TO THE OUTPUT CLOCK
ENO_1, ENO_2	**Output-Port Enables.** ENO_1 and ENO_2 are active HIGH, synchronous to the rising edge of CKO. Data is read from the FIFO memory array when both ENO_1, ENO_2 are asserted. **NOTE:** ENO_1, ENO_2 DO NOT ENABLE reading data from the Resource Register or the Mailbox.
ADO[2:0]	**Output-Port Address Field.** ADO[2:0] specifies the Output-Port source/destination. See Table 4. ADO[2:0] is synchronous to the rising edge of CKO. **NOTE:** In order to read the resource register at the output bus, $\overline{BYE}$ should be deasserted and the FIFO memory array should be disabled.

Table 3. $\overline{HF}$ Synchronization Modes

CONTROL REGISTER		FUNCTION
BIT 4	BIT 3	
L *	L *	Asynchronous Mode: $\overline{HF}$
L	H	Synchronous Mode I: $\overline{HF}$ is synchronous to the rising edge of CKO
H	L	Synchronous Mode II: $\overline{HF}$ is synchronous to the rising edge of CKI
H	H	

* Default Mode

Table 4. Output-Port Address Field

ADO_2	ADO_1	ADO_0	SELECTION	DEFAULT VALUE (of the selected REGISTER)
L	L	L	RBASE register	0
L	L	H	ROFFSET register	0
L	H	L	$\overline{AF}$ offset value	8
L	H	H	Parity register	0
H	L	L	$\overline{AE}$ offset value	8
H	L	H	Control register	1
H	H	L	Mailbox	0
H	H	H	Resource registers read disabled	Not applicable

PIN NAME	DESCRIPTION
	CONTROL SIGNALS SYNCHRONOUS TO THE OUTPUT CLOCK (cont'd)
WSO[1:0]	**Output-Port Word-Width-Selection Address Field.** WSO[1:0] is synchronous to the rising edge of CKO. WSO[1:0] selects the Output-Port Word-Width and controls byte-order-reversal according to Table 5.
RTMD[1:0]	**Retransmit Mode Control.** RTMD[1:0] is synchronized to the rising edge of CKO. RTMD[1:0] controls the placement of new contents into the Read Pointer (RP) and/or the Retransmit Base (RBASE) registers. Whenever Retransmit ($\overline{RT}$) is asserted, one of three operations is performed according to the setting of RTMD[1:0]. See Table 6. **NOTES:** 1. When RTMD[1:0] is set to 0, the FIFO is in depth cascade mode, and the Retransmit mechanism can not be used. In cascade mode, the Almost-Empty Flag is a handshake signal for cascading. The Almost-Empty Flag is used as an input to the ENI of the next FIFO in the chain. 2. In standard FIFO operation RTMD[1:0] must be set to 3 and the Retransmit signal should be HIGH.
$\overline{RT}$	**Retransmit.** $\overline{RT}$ is synchronized to the rising edge of CKO. When asserted LOW, $\overline{RT}$ causes one of the Retransmit Mode operations to be performed, according to the encoding of RTMD[1:0]. See Table 6. **NOTE:** When RTMD[1:0] = 0 (FIFO is in cascade mode) $\overline{RT}$ is ignored.

Table 5. Output-Port Word-Width Selection

WSO_1	WSO_0	FUNCTION	
L	L	9-Bit Data-Path Width	Output data Q[8:0]
L	H	18-Bit Data-Path Width	Output data Q[17:0]
H	L	36-Bit Data-Path Width With Byte-Order-Reversal	Output data Q[35:0]
H	H	36-Bit Data-Path Width	Output data Q[35:0]

Table 6. Retransmit Operation Modes

$RTMD_1$	$RTMD_0$	OPERATION	ACTION TAKEN
L	L	Depth Cascade Mode	The Almost-Empty Flag is a handshake signal for cascading
L	H	Retransmit	(RBASE) + (ROFFSET) → RP
H	L	Retransmit and Mark	(RBASE) + (ROFFSET) → RP and (RBASE) + (ROFFSET) → RBASE
H	H	Mark	(RP) → RBASE

PIN NAME	DESCRIPTION
	STATUS FLAGS SYNCHRONOUS TO THE OUTPUT CLOCK
$\overline{AE}$	**Almost-Empty Flag.** The $\overline{AE}$ flag has two modes of operation depending on the RTMD[1:0] setting. **1. RTMD[1:0] ≠ 0:** $\overline{AE}$ is a standard Almost-Empty Flag. When asserted LOW, $\overline{AE}$ implies that there are at most 'q' 36-bit words in the FIFO memory array, where 'q' is Almost-Empty-Offset-Value register value. In this mode $\overline{AE}$ has two synchronization options depending on the setting of Bit 2 of the control register. *Bit 2 = 0* (Default) Asynchronous Mode *Bit 2 = 1* Synchronous Mode: $\overline{AE}$ is synchronous to the rising edge of CKO. **2. RTMD[1:0] = 0:** $\overline{AE}$ is a handshake signal for cascading.
$\overline{EF}$	**Empty Flag.** $\overline{EF}$ is synchronous to the rising edge of CKO. When asserted LOW, all 1024 36-bit words are vacant. When asserted, $\overline{EF}$ disables the FIFO Read operation.
$\overline{PF}$	**Parity-Error Flag.** $\overline{PF}$ is synchronized to the rising edge of CKO. When asserted LOW, $\overline{PF}$ implies that a parity error has occurred in at least one 9-bit byte within a 36-bit word read from the FIFO memory array. If there are no errors, it is deasserted HIGH. When an error is detected, the parity check result of each 9-bit byte of the 36-bit output word is written to the parity register. The content of the parity register is frozen until read. The $\overline{PF}$ signal is delayed by one CKO cycle compared to the output data (i.e., if the $\overline{PF}$ is asserted, there was an error in the previous word).
$\overline{MEF}$	**Mailbox-Empty Flag.** $\overline{MEF}$ is synchronous to the rising edge of CKO. When asserted LOW, $\overline{MEF}$ indicates that there is no new mail word in the mailbox.
	VOLTAGES AND GROUNDS
V_{CC}	**Positive Power for Internal Logic.**
V_{CCO}	**Positive Power for Output Drivers.**
V_{SS}	**Ground for Internal Logic.**
V_{SSO}	**Ground for Output Drivers.**

OPERATIONAL DESCRIPTION

The LH543620 has four operating modes:

- Normal Mode
- Programmable Resource Registers
- Mailbox
- Data Bypass

NORMAL MODE

Normal FIFO operation refers to Read and Write operations to the FIFO memory array. Data Write operations into the FIFO memory array occur at the rising edge of CKI. The operation is enabled if both ENI_1 and ENI_2 are asserted HIGH. Data Read operations from the FIFO memory occur at the rising edge of CKO. The operation is enabled if both ENO_1 and ENO_2 are asserted HIGH.

The FIFO write and read operations are supported by the following mechanisms:

- Byte-Order-Reversal and Bus Funneling/Defunneling Functions
- Status Flags
- Retransmit Mechanism
- Parity Checking
- Parity Generation

Byte-Order-Reversal and Bus Funneling/ Defunneling Functions

Word width can be selected at the Input Port and/or the Output Port to be 36, 18 or 9 bits wide. When the Output Port width is selected to be 36 bits, it is possible to select Byte-Order-Reversal.

The funneling mechanism is controlled by the inputs WSI[1:0] and WSO[1:0] according to Tables 2 and 5. Data is packed and unpacked from a 36-bit word memory array. Table 7 describes all combinations of funneling/defunneling.

Changes to the funneling/defunneling settings during system operation should be made one clock before a word boundary, as shown in Example 3.

Example 1: 36-to-9 Funneling

CONDITIONS		RESULTS
WSI[1:0]	WSO[1:0]	
3	–	Input 36 bits wide.
–	0	Output 9 bits wide. Pins used are Q[8:0].

The dataflow structure is illustrated by Figure 5.

Example 2: 18-to-36 Defunneling With Byte Reversal

This example performs two functions:

1. Bus width change
2. Big Endian to Little Endian conversion

This configuration can be used for connecting the Intel 80286 to the Motorola 68040.

CONDITIONS		RESULTS
WSI[1:0]	WSO[1:0]	
1	–	Input 18 bits wide. Pins used are D[17:0].
–	2	Output 36 bits wide with byte reversal order.

The dataflow structure is illustrated by Figure 6.

Example 3: Changing Input Bus Width From 9 to 36 During Operation

CKI	WSI	ACTION
0	0	Write 1st 9-bit byte
1	0	Write 2nd 9-bit byte
2	0	Write 3rd 9-bit byte
3	3	Write 4th 9-bit byte
4	3	Write 1st 36-bit word

Table 7. Bus Funneling/Defunneling *

INPUT				OUTPUT															
CKI	WSI = 0			CKO	WSO = 3				WSO = 2				WSO = 1				WSO = 0			
cycles	D[35:9]		D[8:0]	cycles	Q[35:0]				Q[35:0]				Q[35:18]		Q[17:0]		Q[35:9]			Q[8:0]
0	xxx		B0	0	B3	B2	B1	B0	B0	B1	B2	B3	B3	B2	B1	B0	B3	B2	B1	B0
1	xxx		B1	1	B7	B6	B5	B4	B4	B5	B6	B7	B1	B0	B3	B2	B0	B3	B2	B1
2	xxx		B2	2									B7	B6	B5	B4	B1	B0	B3	B2
3	xxx		B3	3									B5	B4	B7	B6	B2	B1	B0	B3
4	xxx		B4	4													B7	B6	B5	B4
5	xxx		B5	5																
6	xxx		B6	6																
7	xxx		B7	7																
8	xxx		B8	8																
	WSI = 1				WSO = 3				WSO = 2				WSO = 1				WSO = 0			
	D[35:18]		D[17:0]		Q[35:0]				Q[35:0]				Q[35:18]		Q[17:0]		Q[35:9]			Q[8:0]
0	xx	B1	B0	0	B3	B2	B1	B0	B0	B1	B2	B3	B3	B2	B1	B0	B3	B2	B1	B0
1	xx	B3	B2	1	B7	B6	B5	B4	B4	B5	B6	B7	B1	B0	B3	B2	B0	B3	B2	B1
2	xx	B5	B4	2									B7	B6	B5	B4	B1	B0	B3	B2
3	xx	B7	B6	3									B5	B4	B7	B6	B2	B1	B0	B3
4	xx	B9	B8	4													B7	B6	B5	B4
	WSI = 3				WSO = 3				WSO = 2				WSO = 1				WSO = 0			
	D[35:0]				Q[35:0]				Q[35:0]				Q[35:18]		Q[17:0]		Q[35:9]			Q[8:0]
0	B3	B2	B1	B0	0	B3	B2	B1	B0	B0	B1	B2	B3	B3	B2	B1	B0	B3	B2	B1	B0
1	B7	B6	B5	B4	1	B7	B6	B5	B4	B4	B5	B6	B7	B1	B0	B3	B2	B0	B3	B2	B1
														B7	B6	B5	B4	B1	B0	B3	B2
														B5	B4	B7	B6	B2	B1	B0	B3
																		B7	B6	B5	B4

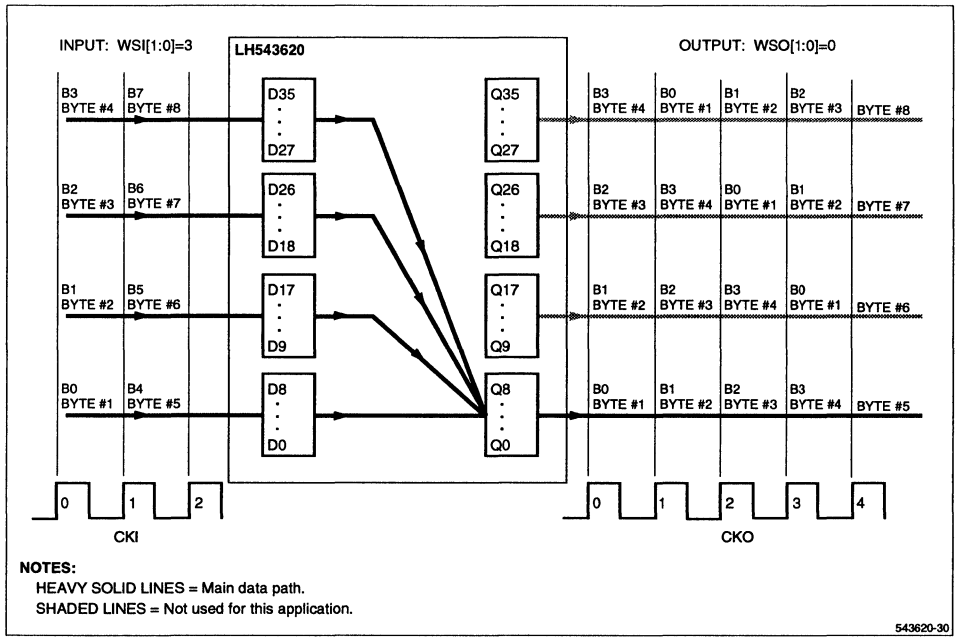


Figure 5. 36-to-9 Bus Funneling

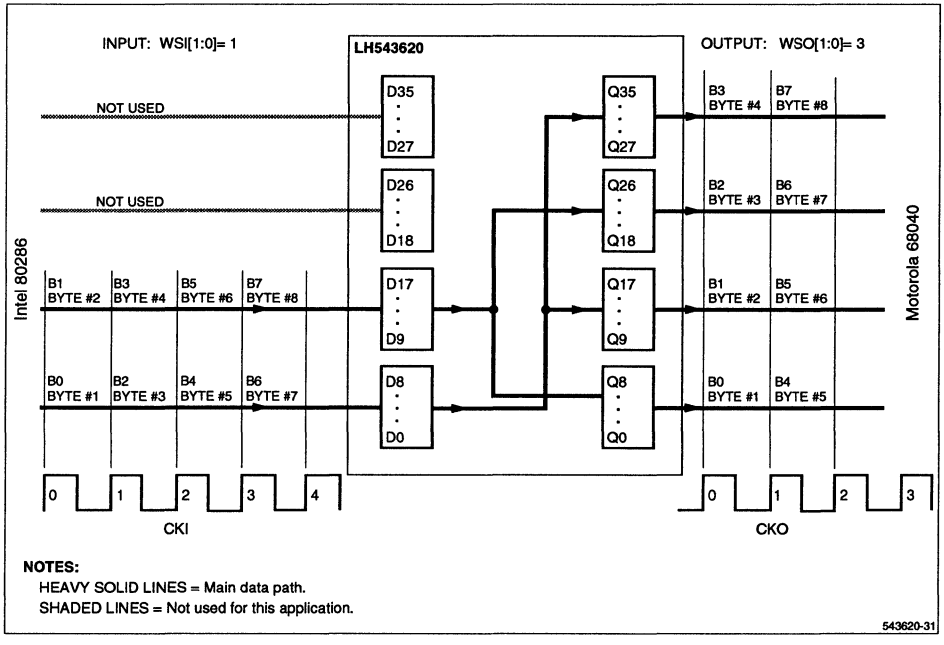


Figure 6. Example of 18-to-36 Bus Defunneling

Status Flags

There are five status flags:

$\overline{FF}$ Full Flag

$\overline{AF}$ Almost-Full Flag

$\overline{HF}$ Half-Full Flag

$\overline{EF}$ Empty Flag

$\overline{AE}$ Almost-Empty Flag

$\overline{EF}$ Empty Flag

The functionality and the synchronization of the status flags are detailed in the *Pins Descriptions (Functional)* section. All status flags are generated for 36-bit word widths, not according to selected input or output port widths.

Retransmit Mechanism

With standard FIFO operations, every data word can be read out of the FIFO once. The Retransmit mechanism allows reading the data more than once by providing flexible control of the Read Pointer.

Associated with the Retransmit mechanism are three control lines: RTMD[1:0], $\overline{RT}$, and two Resource registers: RBASE and ROFFSET.

RTMD[1:0] sets the mode of operation. See Table 6.

$\overline{RT}$ enables the operation synchronous to CKO.

Retransmit allows three modes of operation:

Mark: RTMD[1:0] = 3 and $\overline{RT}$ is asserted. The value of the Read Pointer is saved into the RBASE register.

Retransmit: RTMD[1:0] = 1 and $\overline{RT}$ is asserted. The Read Pointer is loaded by the value of RBASE plus the value of ROFFSET.

Retransmit and Mark: RTMD[1:0] = 2 and $\overline{RT}$ is asserted: The Read Pointer is loaded by the value of RBASE plus the value of ROFFSET. Then the value of the Read Pointer is saved into the RBASE register.

The timing of the retransmit is illustrated in Figures 26 and 27.

When $\overline{RT}$ is asserted and RTMD[1:0] is set to 1 or 2, the flags change their value to indicate a 'Retransmit state', i.e., $\overline{EF}$, $\overline{AE}$, $\overline{FF}$ deasserted; $\overline{AF}$, $\overline{HF}$ asserted. Three enable-read cycles are required to read the new data word. The flags reflect the new status. The retransmit is acknowledged even when the output is disabled (ENO = LOW), but enable-read cycles are needed to fill the pipeline with new information before reading the new data.

NOTES

1. The Retransmit mechanism can be used independently and parallel to the write operation.
2. When using normal read and write operations, the $\overline{FF}$ inhibits writing when the FIFO is full and the $\overline{EF}$ inhibits reading when the FIFO is empty. This behavior provides a protection from wraparound situations (i.e., the Read pointer is ahead of the Write Pointer). This protection is NOT provided when using retransmit. The user should be careful not to write more than 1024 words from the marked point.
3. When the retransmit mechanism is not used, the recommended connection is:
   RTMD[1:0] = 3
   $\overline{RT}$ = HIGH

The Retransmit mechanism can be useful in many applications. For example:

1. Computer-communications applications.

   When the receiver reads a block of data and finds no errors in the data block, it can mark the beginning of the new message by setting the FIFO in MARK mode RTMD[1:0] = 3 and assert the $\overline{RT}$ signal for one clock cycle.

   If the receiver finds an error in the data block, it can read the last message again by setting the FIFO in Retransmit mode RTMD[1:0] = 1 and asserting the $\overline{RT}$ signal for one cycle.

2. Overlap addressing for DSP applications.

   A typical DSP consists of A/D-FIFO-DSP. In many applications, the DSP needs to read a block of data where each block overlaps the previous block (like the overlap-and-save method for filtering.) The overlap addressing can be implemented by using the LH543620 with no additional hardware as follows:

   The FIFO is set to retransmit and mark mode: RTMD[1:0] = 2, the $\overline{AF}$ offset register is programmed to N = Block Size, and the ROFFSET register is programmed to (N – Overlap). The data is loaded into the FIFO each time CKin is triggered.

   The DSP can sense the $\overline{AF}$ flag of the FIFO. Whenever this flag is being asserted, a new block of data is available in the FIFO. The DSP then reads a block of data, and then asserts the FIFO's $\overline{RT}$ signal, which causes the RP and RBASE register to be set at the beginning of the new block.

Parity Checking

The Parity checking mechanism is always active. Parity checking is done separately for each of the 9-bit bytes of the 36-bit word read from the memory array. Toggling Bit 0 of the control register selects odd or even parity. When a parity error is detected in one or more bytes, the signal $\overline{PF}$ is asserted and the result of the individual parity checks are written to the parity register. See Example 3.

The parity register is frozen until read. When read, the parity register is released and ready to store the next parity error data.

Parity Generation

After Reset, parity generation is not active. Parity generation is active only when Bit 1 of the control register is HIGH. The parity mechanism, when enabled, creates a parity bit for each of the bytes of the input word. The parity bit for each byte is created based on its 8 least significant bits of each 9-bit byte of the input-data word and on Bit 0 of the control register (it specifies odd or even parity). The result of the parity generation is written back to the MSB of the data byte. See Example 4.

PROGRAMMABLE RESOURCE REGISTERS

The LH543620 has six programmable resource registers. The resource registers may be loaded from either the Input Port or the Output Port. They can be read from the Output Port. The selection and loading or reading of the resource registers is controlled by ADI, ADO and CAPR. See Tables 1 and 4 and Figure 4.

The resource registers are:

Control (Default = 1).

$\overline{AE}$ Offset – Offset value of the $\overline{AE}$ flag (Default = 8).

$\overline{AF}$ Offset – Offset value of the $\overline{AF}$ flag (Default = 8).

$\overline{RT}$ Offset – Offset value of the Retransmit mechanism (Default = 0).

$\overline{RT}$ Base – Base register of the Retransmit mechanism (Default = 0).

Parity

EXAMPLE 3

PARITY CHECK

	Q35			Q0
Output word:	100111100	000111100	100111000	000111000

Odd parity: Parity Register = 0110; PF-Asserted Low

Even parity: Parity Register = 1001; PF-Asserted Low

EXAMPLE 4

PARITY GENERATION

	D35			D0
Input word:	**1**00111100	**0**00111100	**1**00111000	**0**00111000
Output, odd parity:	**1**00111100	**1**00111100	**0**00111000	**0**00111000
Output, even parity:	**0**00111100	**0**00111100	**1**00111000	**1**00111000

Control Register (See Figure 7)

After reset, the control register's value is 1. This sets the following conditions:

Odd parity

Disabling parity generation (parity check is active).

$\overline{AF}$, $\overline{HF}$, $\overline{AE}$ flags are asynchronous.

$\overline{OE}$ signal does not control the Read pointer.

Read/Write Resource Register Mode

It is possible to write to the resource registers from either the Input Port or the Output Port. Reading from the resource register is possible only from the Output Port. The source port for the write operation is determined by the control signal CAPR.

Input Port:

Data from the Input Port is written to a resource register when:

the value of the input-address field, ADI, selects the register (see Table 1)

CAPR is LOW

The operation is enabled by ADI[2:0] and synchronized to CKI.

Output Port:

Data from the Output Port is written to a resource register when:

the value of the output-address field, ADO, selects the register (see Table 4)

CAPR is HIGH

$\overline{OE}$ is HIGH

Data is read from a resource register to the Output Port when:

the value of the output-address field, ADO, selects the register (see Table 4)

$\overline{OE}$ is LOW

Both operations are enabled by ADO[2:0] and are synchronous to CKO.

MAILBOX

The mailbox mechanism includes:

One 36-bit data register.

Two status flags:
– $\overline{MFF}$ Mailbox Full Flag
– $\overline{MEF}$ Mailbox Empty Flag

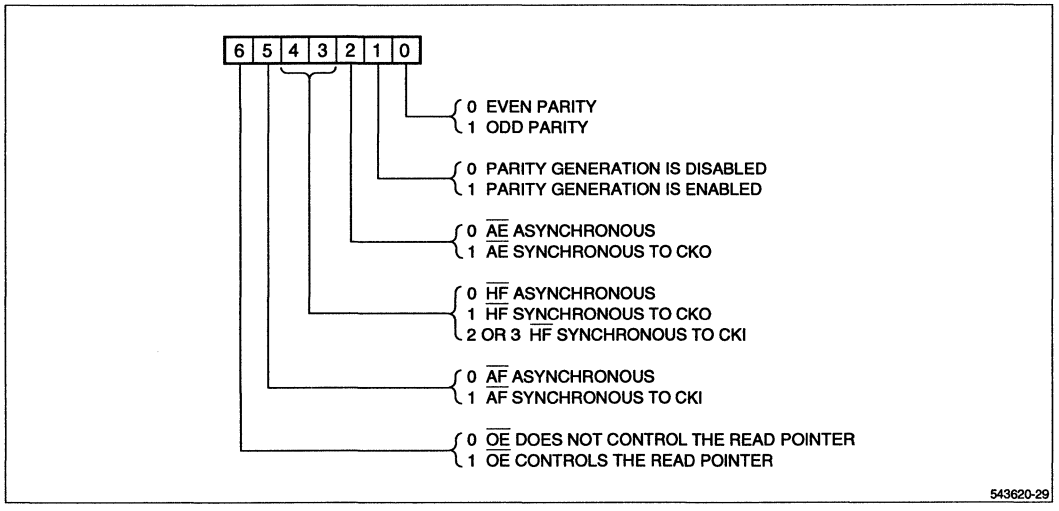


Figure 7. LH543620 Control Register

Writing to the Mailbox is enabled from the Input Port when the Input Port address field ADI[2:0] = 6. The write operation is synchronous to the rising edge of CKI.

When writing to the Mailbox, the status flags are changed as follows:

$\overline{MEF}$ is deasserted HIGH on the rising edge of CKO.

$\overline{MFF}$ is asserted LOW on the rising edge of CKI.

A Mailbox read is enabled from the Output Port, when the Output Port address field ADO[2:0] = 6. The Read operation is synchronized to CKO.

When reading the Mailbox, the status flags are changed as follows:

$\overline{MEF}$ is asserted LOW on the rising edge of CKO.

$\overline{MFF}$ is deasserted HIGH on the rising edge of CKI.

After reset the Mailbox is empty (i.e., $\overline{MFF}$ = HIGH, $\overline{MEF}$ = LOW).

When using Mailbox, the transmitter side can transfer a message to the receiver side without interrupting the data in the FIFO memory array.

DATA BYPASS MODE

Data Bypass mode is selected when $\overline{BYE}$ = LOW. In this mode, data may be transferred asynchronously from the Input Port to the Output Port. The device may be placed in Data Bypass mode without voiding the contents of the FIFO memory array, the Mailbox Register, or the Resource Register. However, if the input is enabled ($ENI_{1,2}$ = HIGH) then the input data D is also written to the FIFO memory array on the rising edge of CKI. If the Output is enabled, ($ENO_{1,2}$ = HIGH) then the input data D is transferred to the output buffer, and the Read Pointer is incremented by CKO. The control signal $\overline{OE}$ is functioning when $\overline{BYE}$ is asserted.

The recommended control setting for bypass is:

ENI = LOW, ENO = LOW, ADI[2:0] = 7,
ADO[2:0] = 7, $\overline{OE}$ = LOW, $\overline{BYE}$ = LOW

OPERATIONAL MODES AND CONFIGURATIONS

Interlocked Width Expansion (Figure 8A)

Two LH543620s may be configured to expand the width to 72 bits. This is accomplished by:

Cross-connecting the $\overline{FF}$ output of each FIFO to ENI_1 (or ENI_2) input of the other FIFO.

Cross-connecting the $\overline{EF}$ output of each FIFO to ENO_1 (or ENO_2) input of the other FIFO.

The composite status flags are the OR function of the individual flags.

Pipeline Cascading Mode and 'Two-Dimension' Pipeline Cascading Mode (Figure 8B and 8C)

Depth cascading is accomplished by:

Setting the upper FIFO into cascade mode:
RTMD[1:0] = 0

Connecting the same free-running clock to CKO of the upper FIFO and to CKI input of the lower FIFO.

Connecting the $\overline{AE}$ output of the upper FIFO to ENI_1 input (or ENI_2) of the lower FIFO.

Connecting the $\overline{FF}$ output of the lower FIFO to ENO_1 input (or ENO_2) of the upper FIFO.

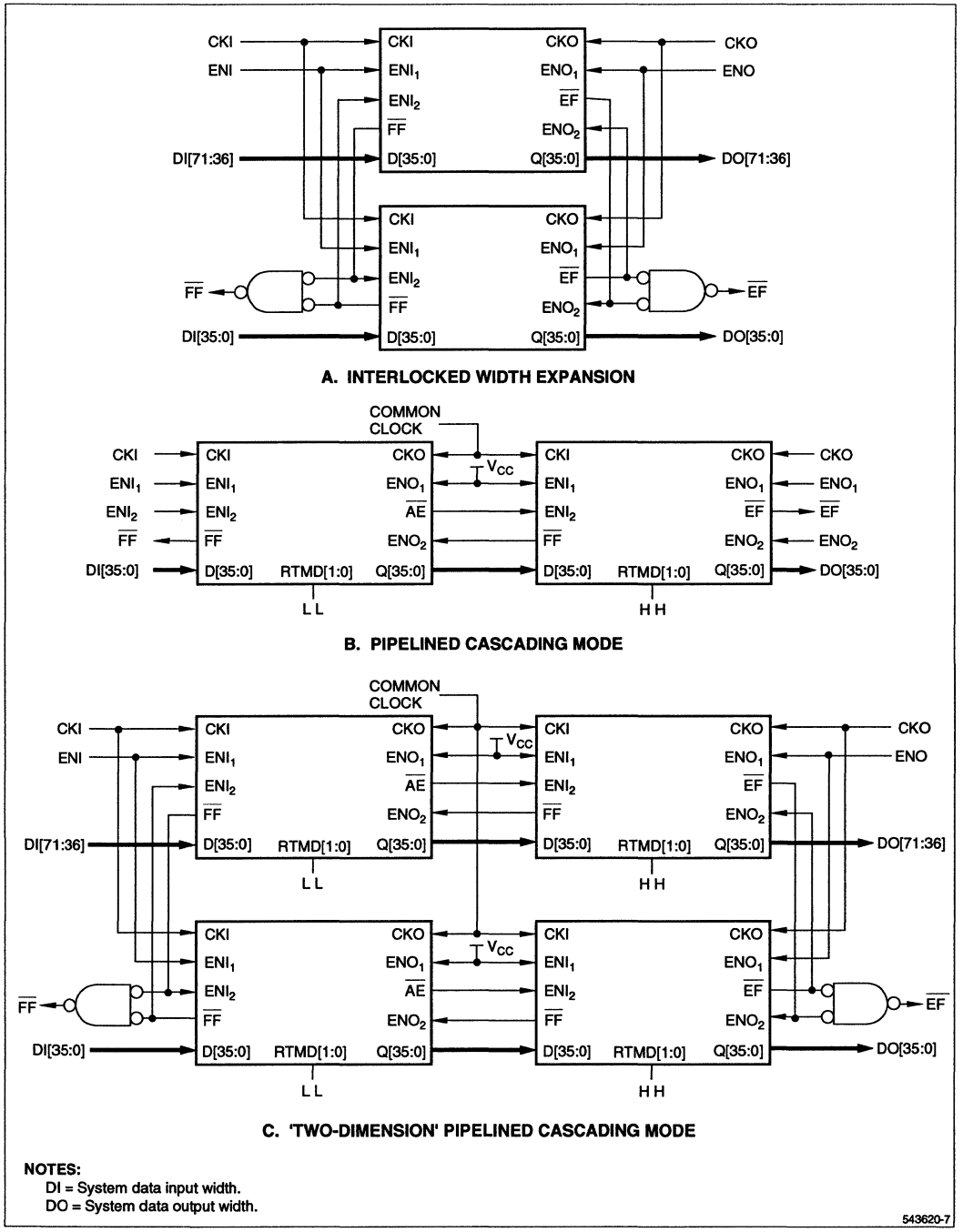
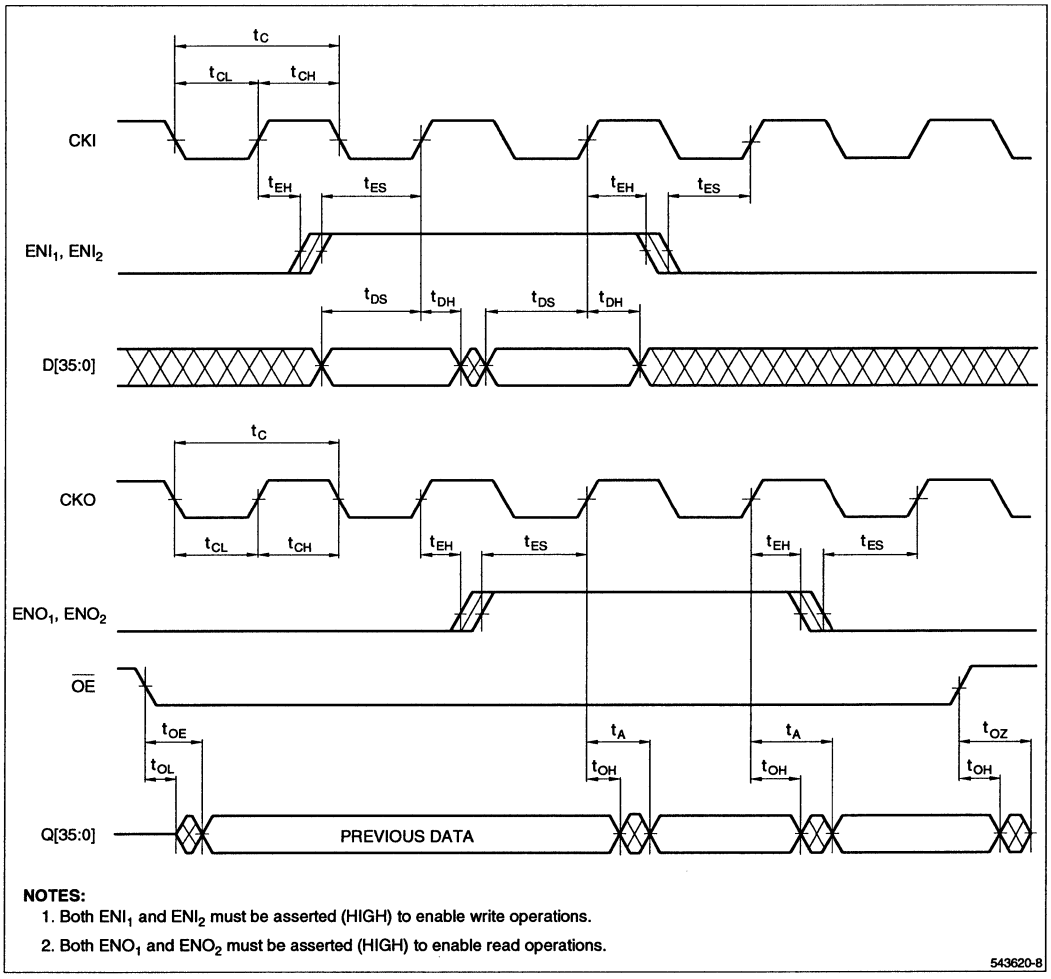


Figure 8. LH543620 Width and Depth Expansion Scheme

TIMING DIAGRAMS



NOTES:

1. Both ENI_1 and ENI_2 must be asserted (HIGH) to enable write operations.
2. Both ENO_1 and ENO_2 must be asserted (HIGH) to enable read operations.

543620-8

Figure 9. Write and Read Operation

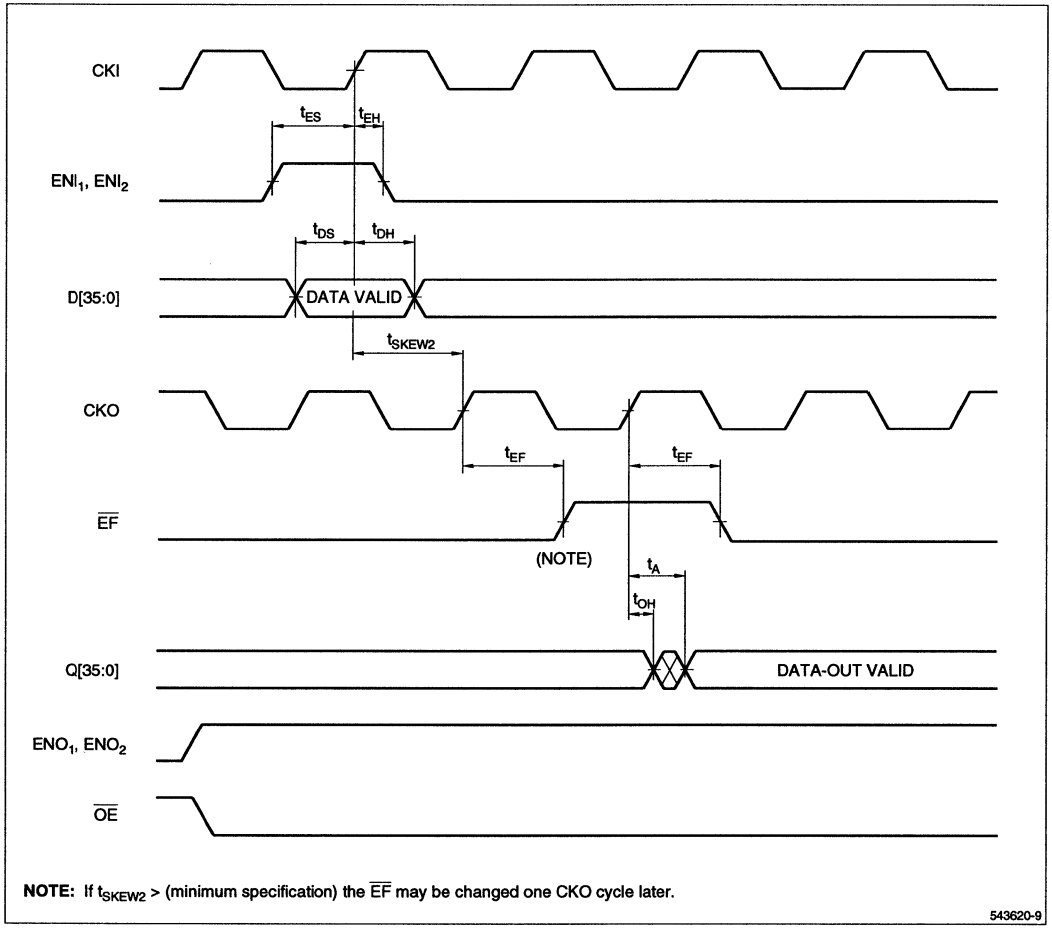


Figure 10. Empty Flag Timing

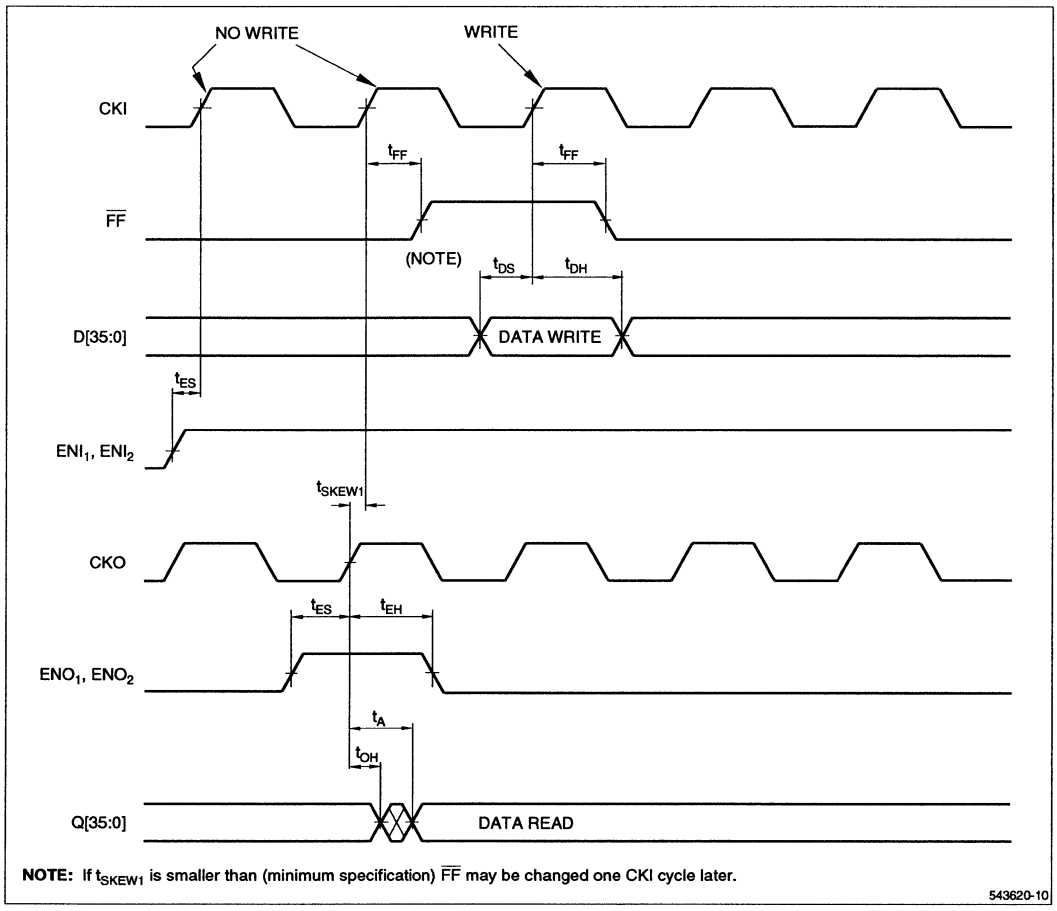
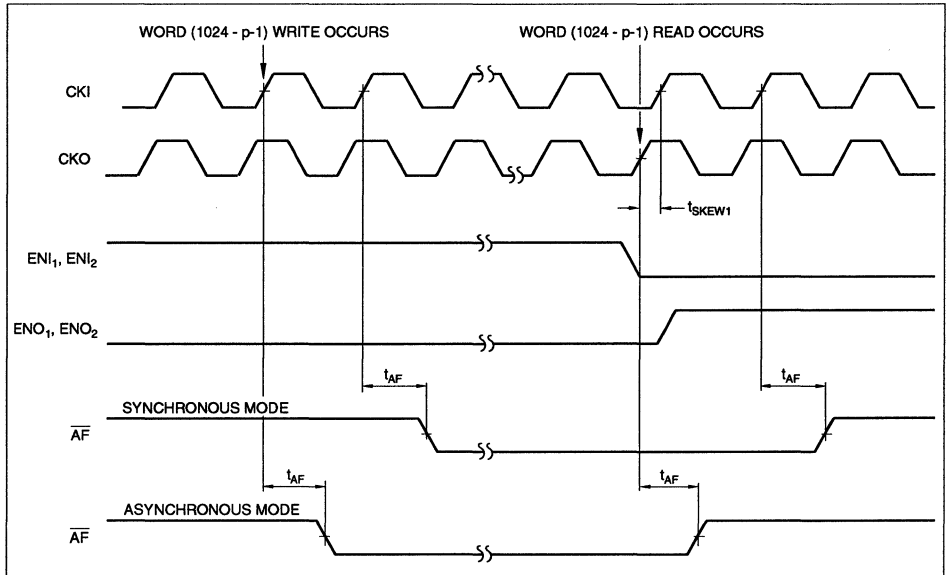


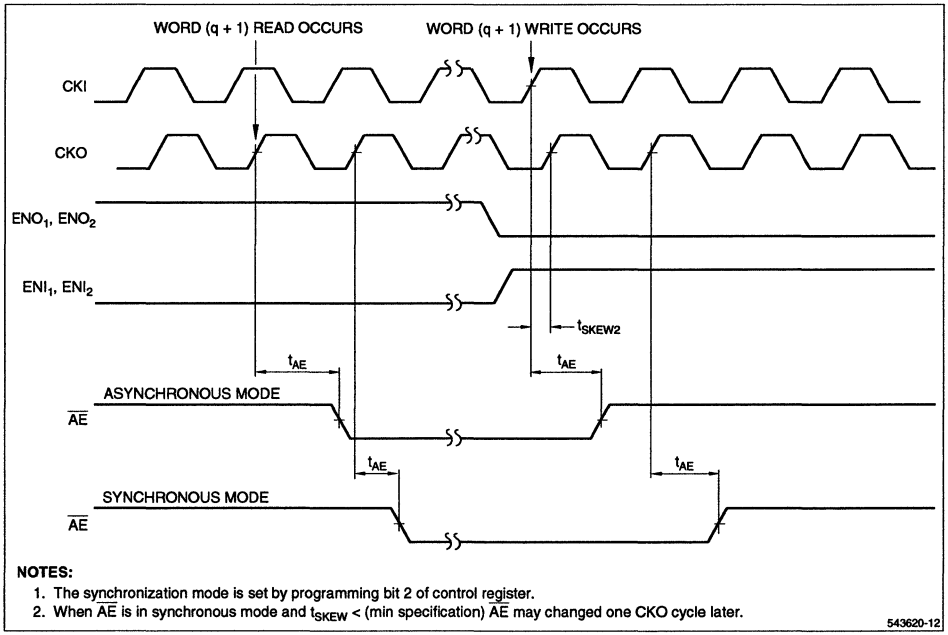
Figure 11. Full Flag Timing



NOTES:
1. The synchronization mode of $\overline{AF}$ is set by programming bit 5 of control register.
2. When in synchronization mode and t_{SKEW} < (min specification) then $\overline{AF}$ may change one CKI later.

543620-11

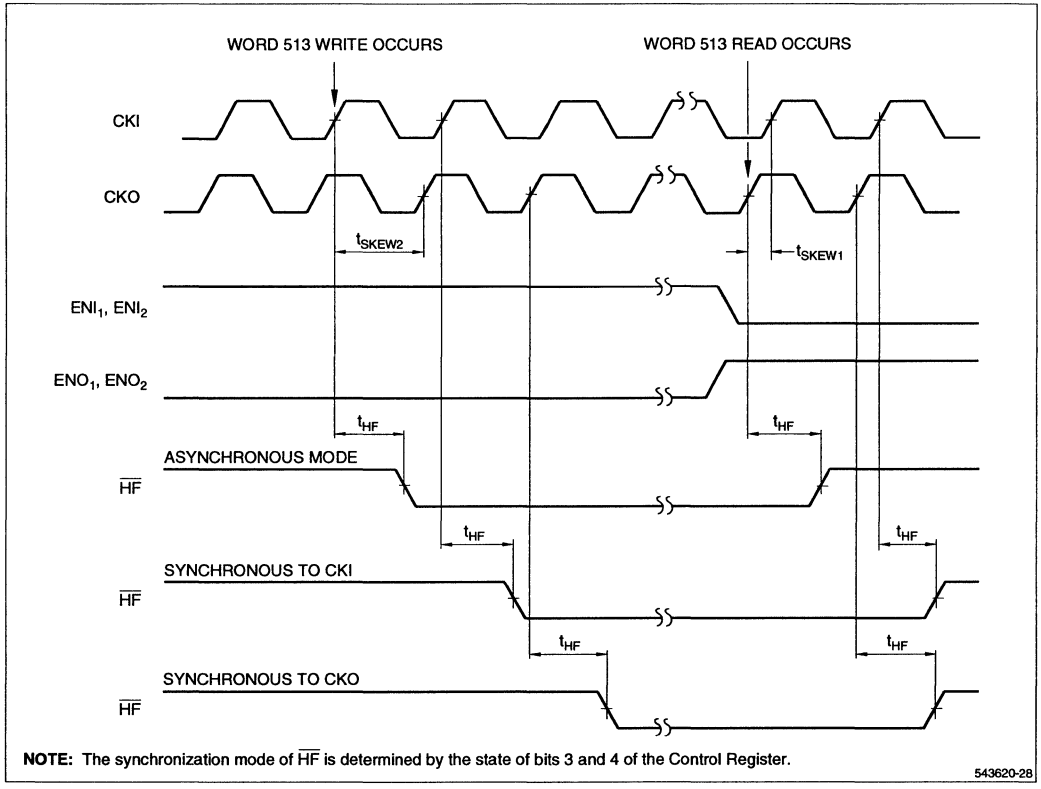
Figure 12. Almost-Full Flag - Synchronous and Asynchronous Modes



NOTES:
1. The synchronization mode is set by programming bit 2 of control register.
2. When $\overline{AE}$ is in synchronous mode and t_{SKEW} < (min specification) $\overline{AE}$ may changed one CKO cycle later.

543620-12

Figure 13. Almost-Empty Flag - Synchronous and Asynchronous Modes



NOTE: The synchronization mode of $\overline{HF}$ is determined by the state of bits 3 and 4 of the Control Register.

Figure 14. Half-Full Flag - Synchronous and Asynchronous Modes

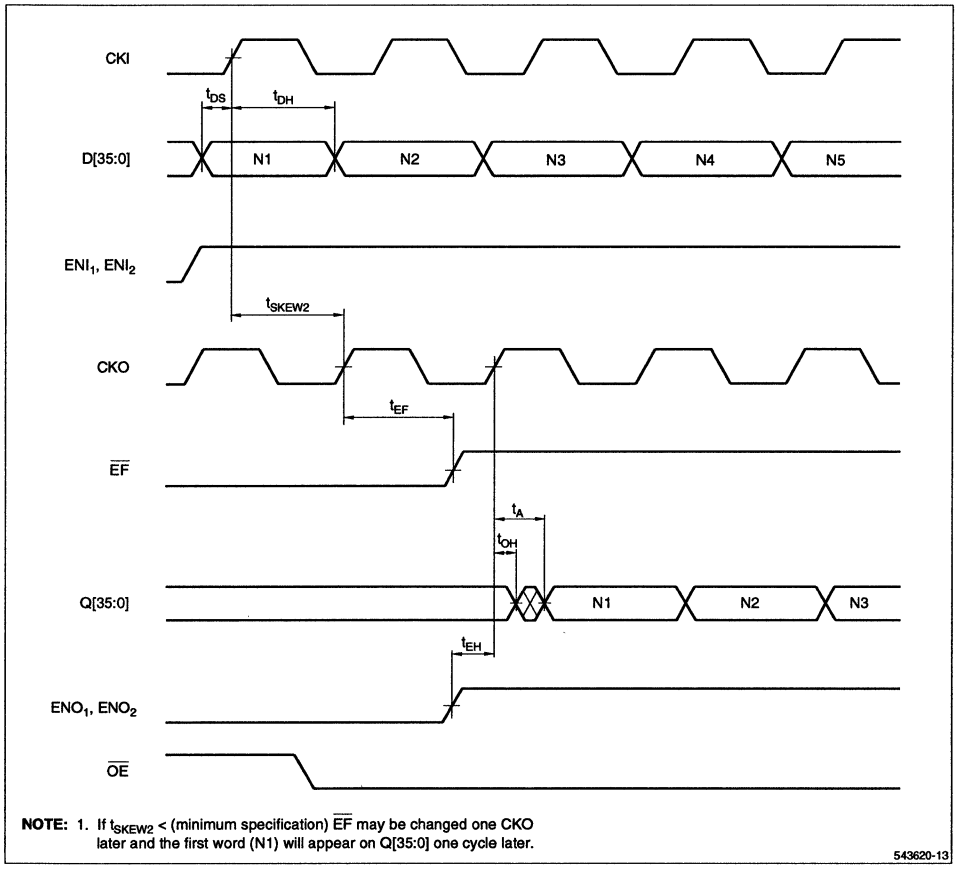


Figure 15. First Word Latency

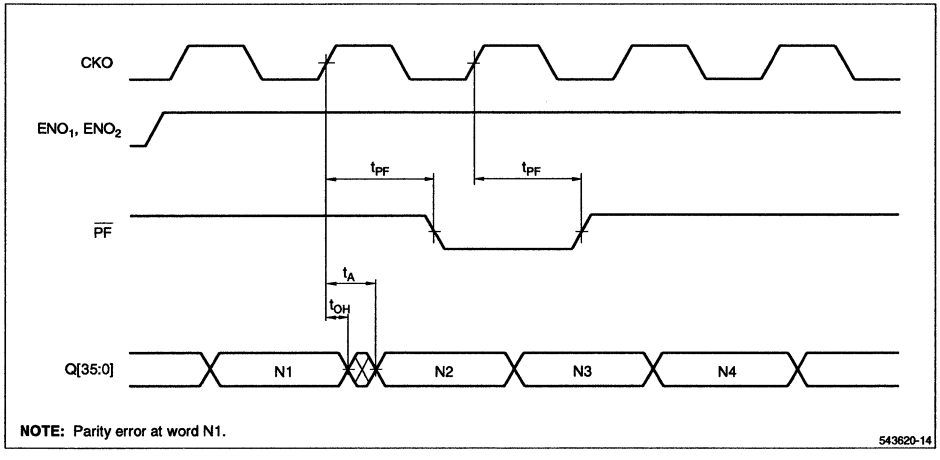
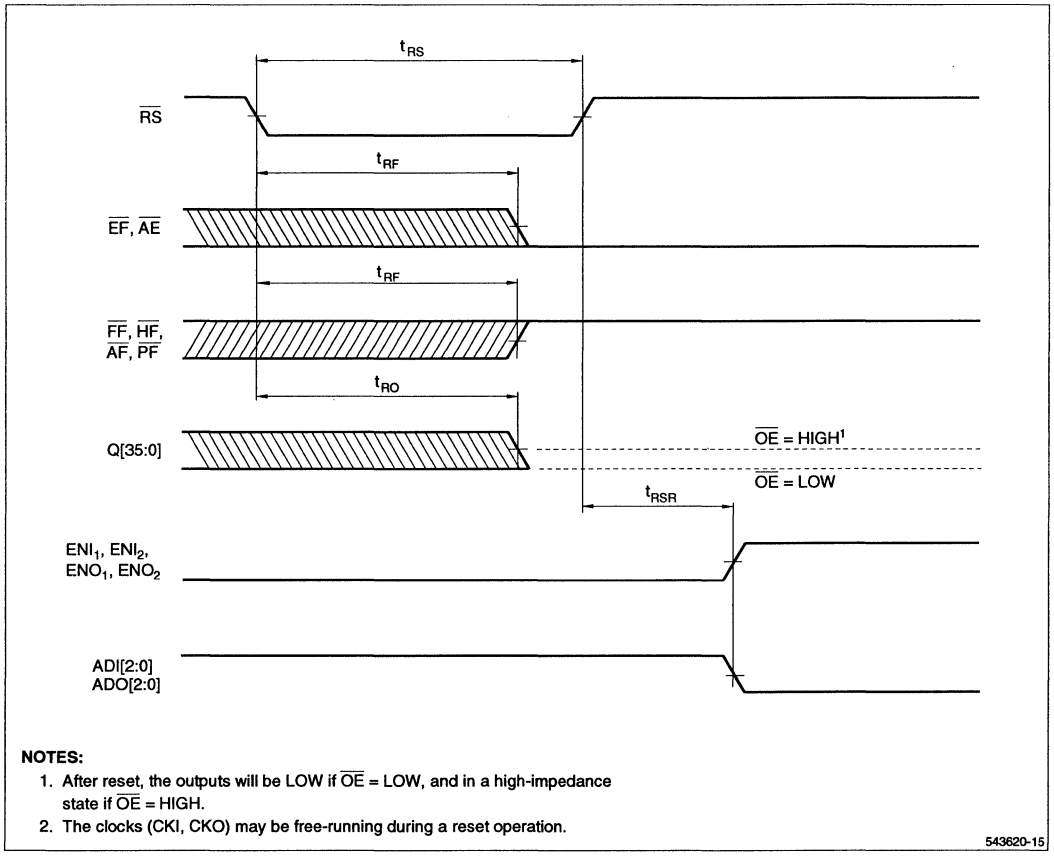


Figure 16. Parity Flag

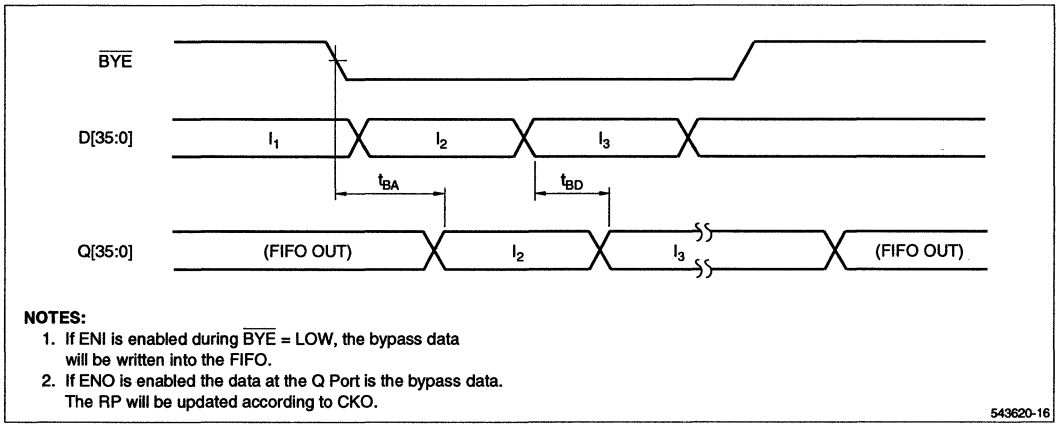


NOTES:

1. After reset, the outputs will be LOW if $\overline{OE}$ = LOW, and in a high-impedance state if $\overline{OE}$ = HIGH.
2. The clocks (CKI, CKO) may be free-running during a reset operation.

543620-15

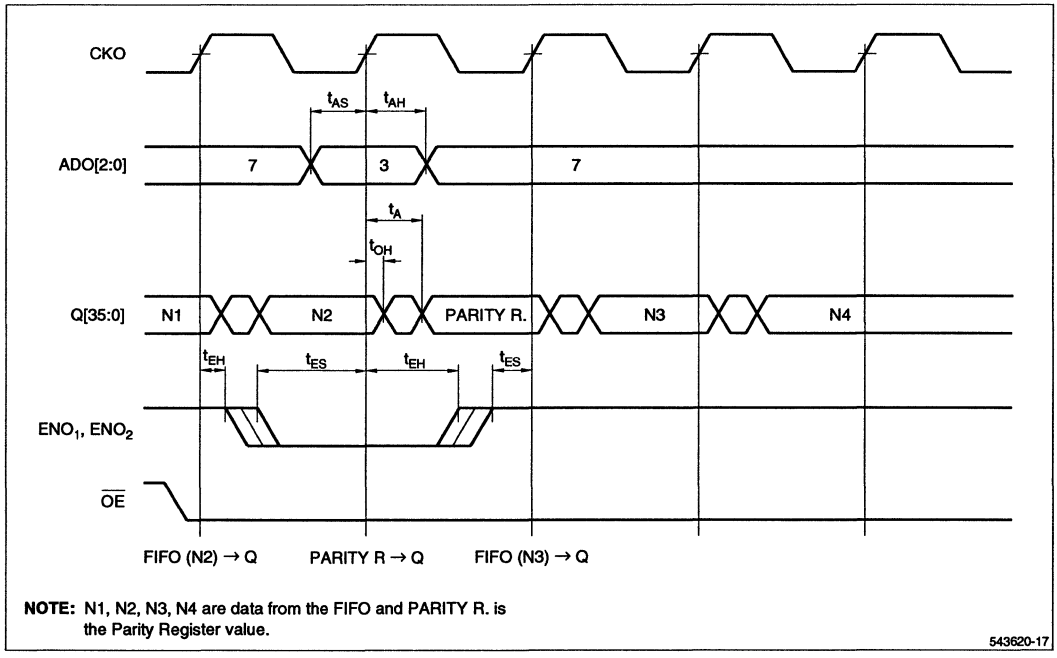
Figure 17. Reset Timing



NOTES:
1. If ENI is enabled during $\overline{BYE}$ = LOW, the bypass data will be written into the FIFO.
2. If ENO is enabled the data at the Q Port is the bypass data. The RP will be updated according to CKO.

543620-16

Figure 18. Bypass



NOTE: N1, N2, N3, N4 are data from the FIFO and PARITY R. is the Parity Register value.

543620-17

Figure 19. Read Resource Register

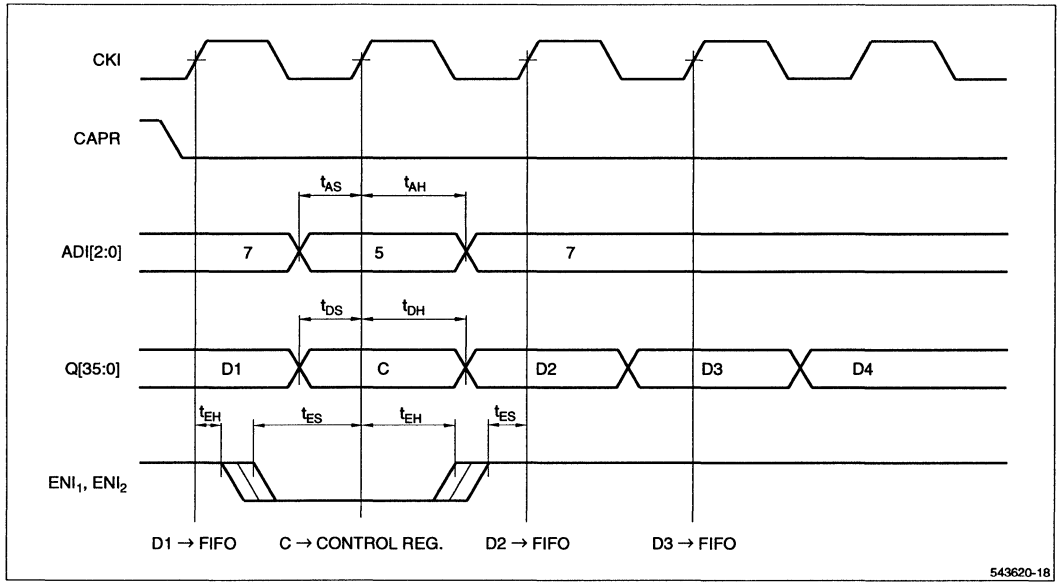


Figure 20. Write Resource Register From the Input Port

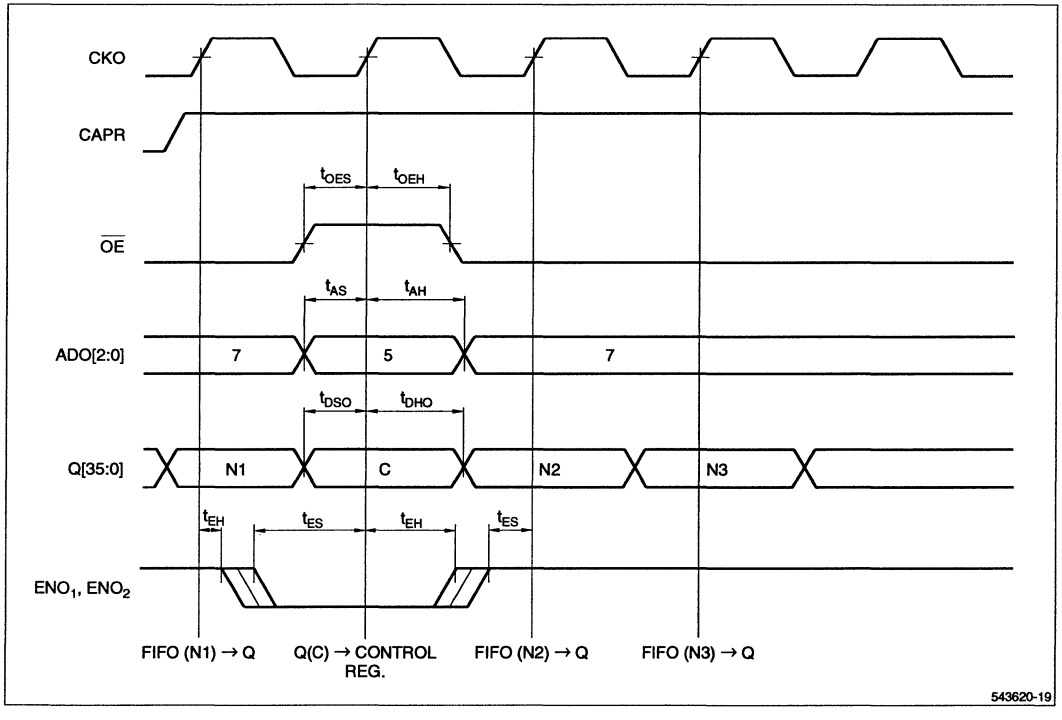


Figure 21. Write Resource Register From Output Port

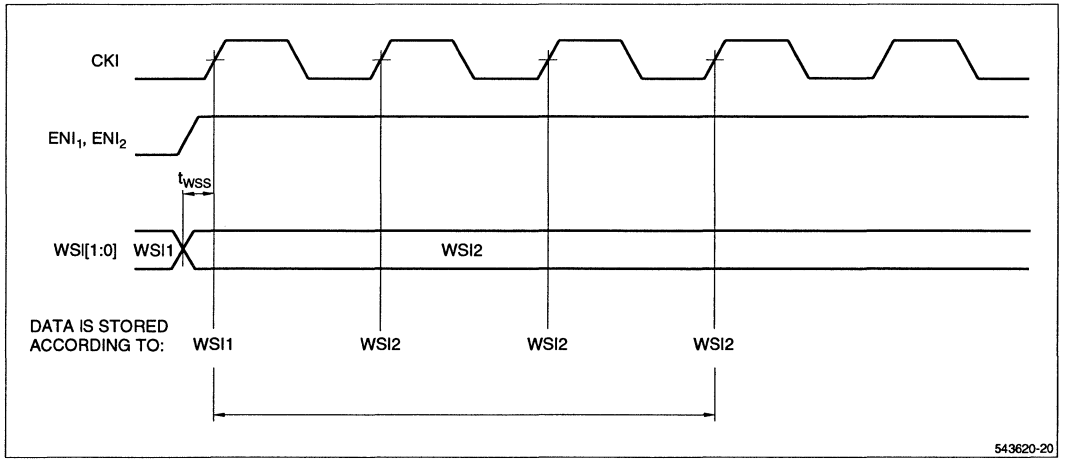


Figure 22. WSI[1:0] Timing

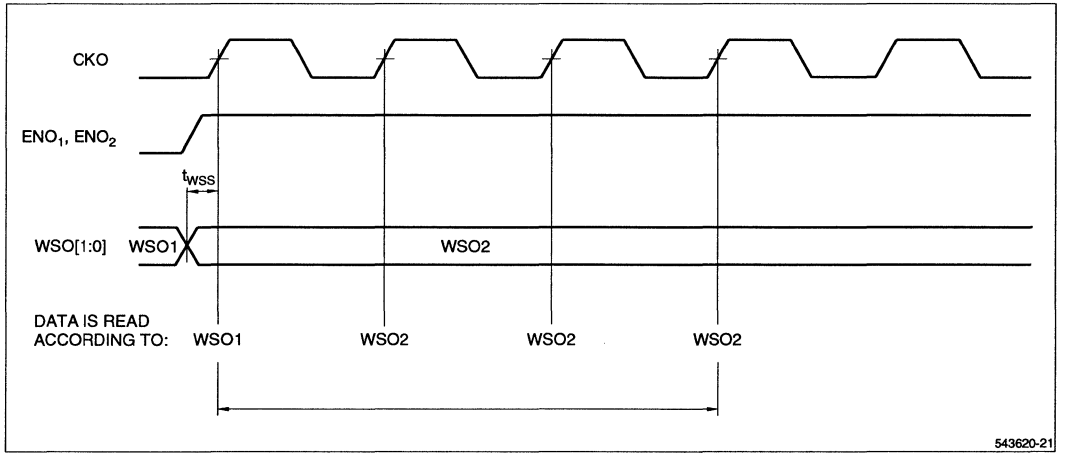


Figure 23. WSO[1:0] Timing

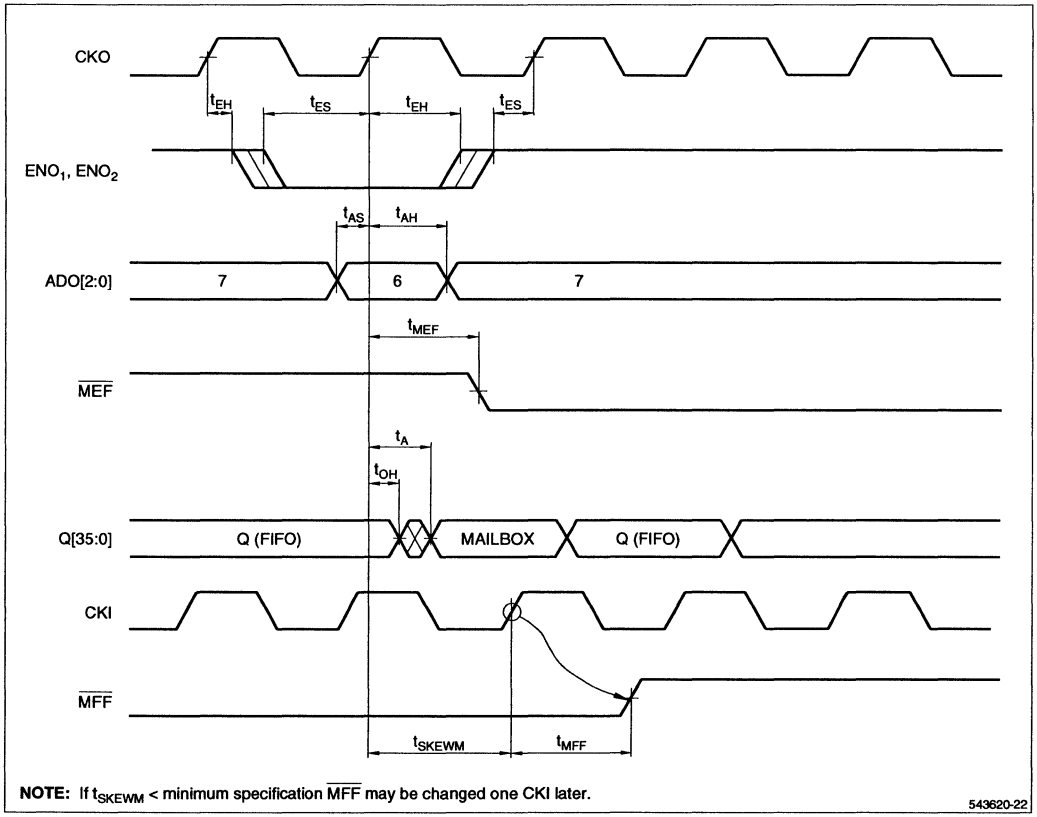


Figure 24. Mailbox Read

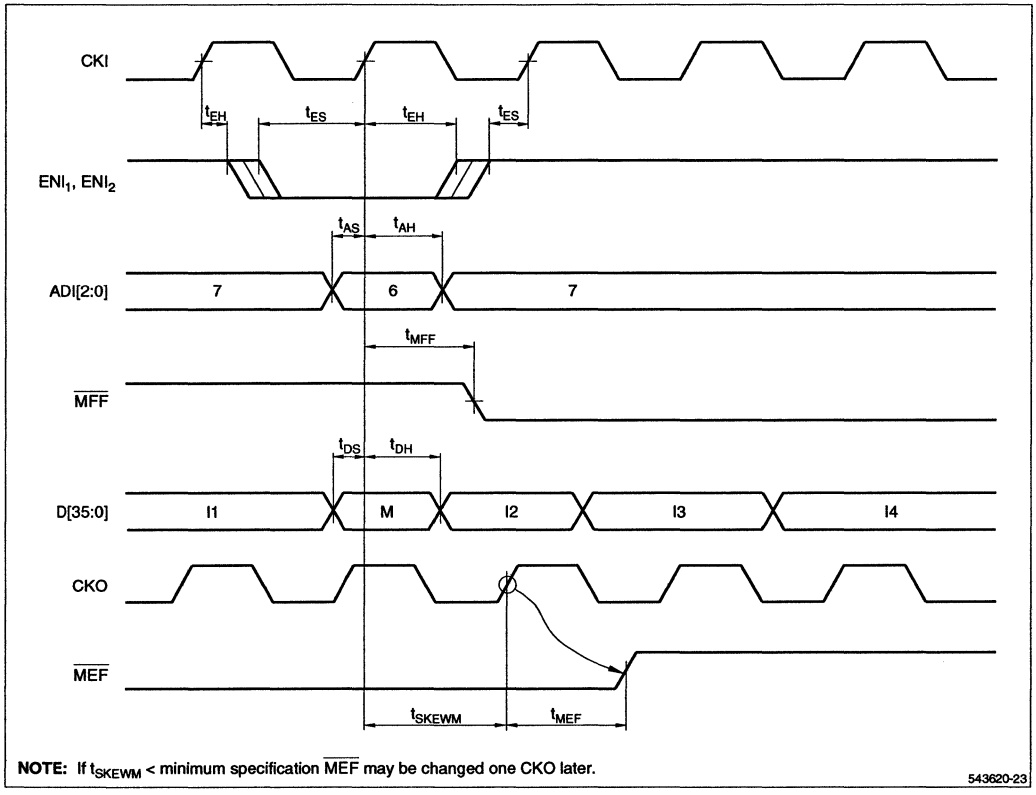
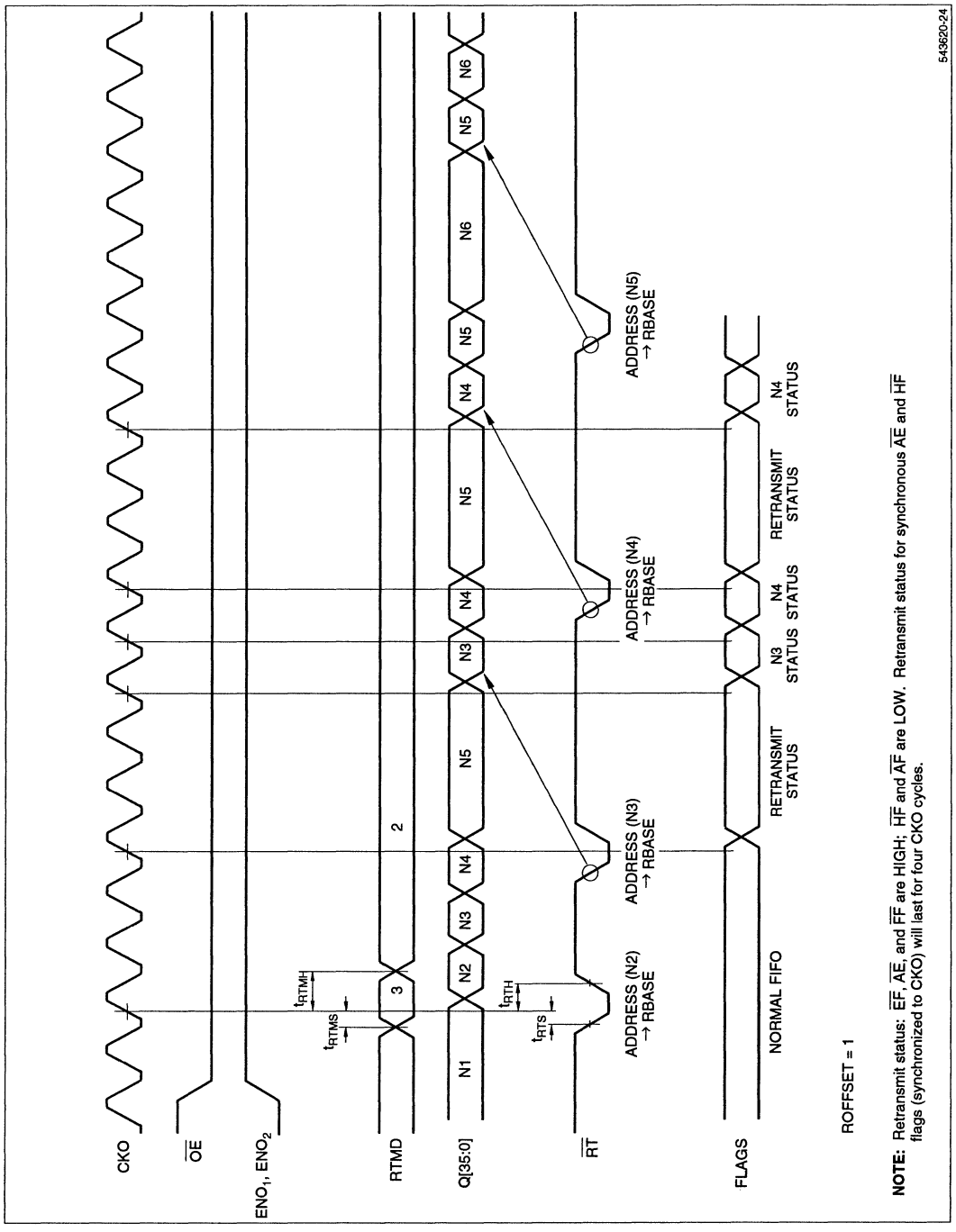
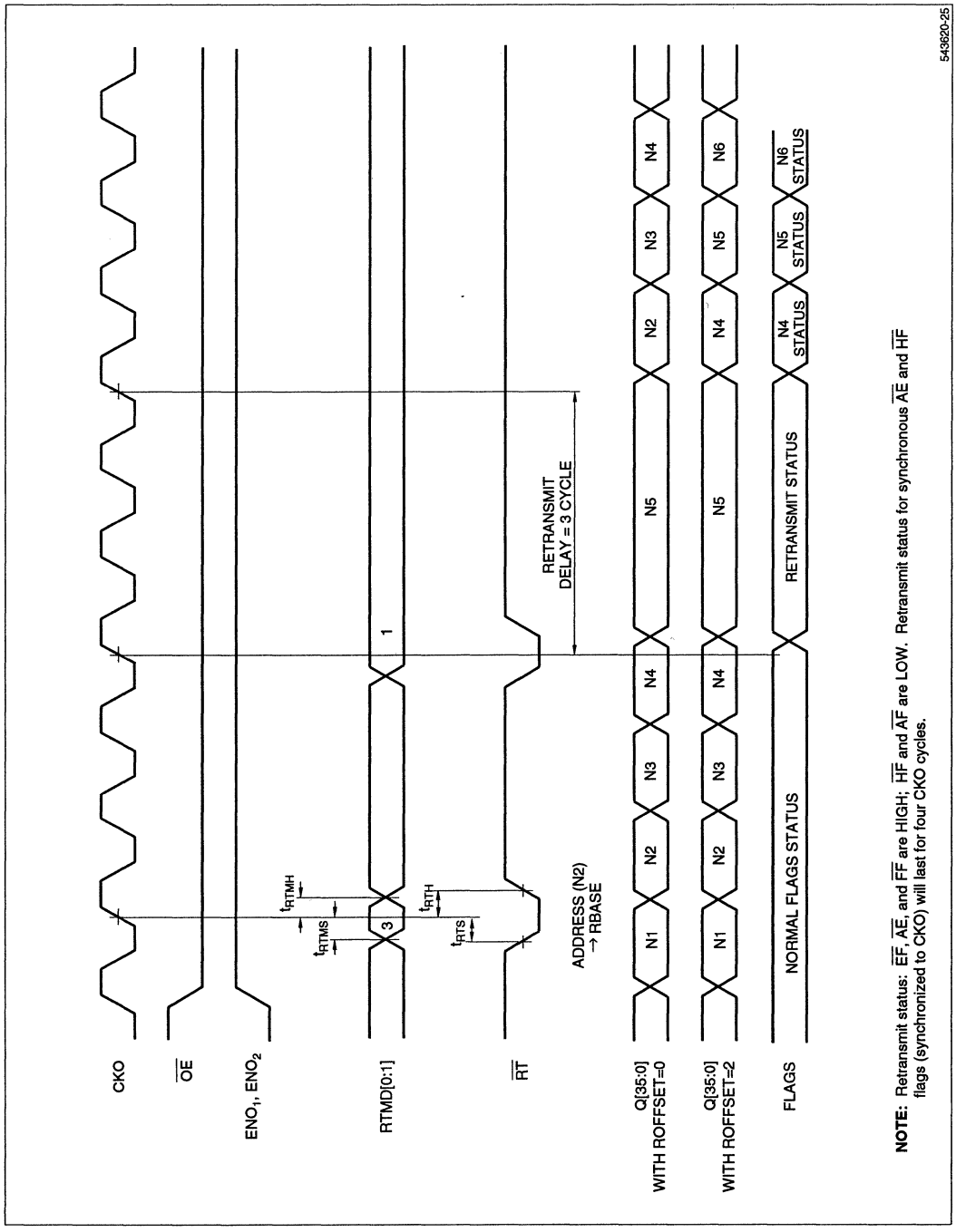


Figure 25. Mailbox Write



NOTE: Retransmit status: $\overline{EF}$, $\overline{AE}$, and $\overline{FF}$ are HIGH; $\overline{HF}$ and $\overline{AF}$ are LOW. Retransmit status for synchronous $\overline{AE}$ and $\overline{HF}$ flags (synchronized to CKO) will last for four CKO cycles.

Figure 26. Retransmit Using Retransmit and Mark Mode



NOTE: Retransmit status: $\overline{EF}$, $\overline{AE}$, and $\overline{FF}$ are HIGH; $\overline{HF}$ and $\overline{AF}$ are LOW. Retransmit status for synchronous $\overline{AE}$ and $\overline{HF}$ flags (synchronized to CKO) will last for four CKO cycles.

Figure 27. Retransmit Using Mark Mode and Retransmit Mode

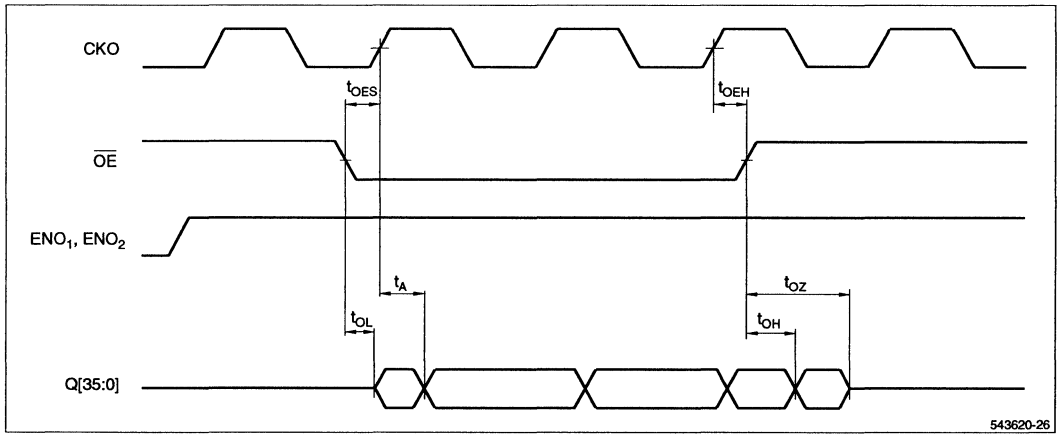
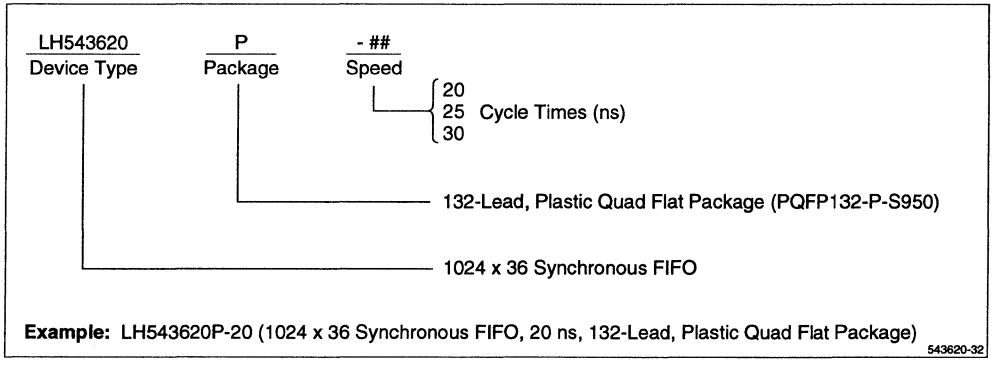


Figure 28. $\overline{OE}$ When Bit 6 of the Control Register is HIGH

ORDERING INFORMATION



FIFO CROSS REFERENCE

ORGANIZATIONAL STRUCTURE	SHARP MODEL *	COMPETITIVE VENDOR	COMPETITIVE MODEL	ACCESS TIME	PACKAGE OPTIONS
256 x 36 x 2	LH5420	Mosel/Vitelic	MS76542	25/30/35 ns	PQFP/PGA
64 x 8	LH5481	Cypress	CY7C408	35/25/15 MHz	DIP/PLCC
64 x 9	LH5491	Cypress	CY7C409	35/25/15 MHz	DIP/PLCC
4,096 x 9	LH5492	Mosel/Vitelic	MS76492	25/30/35 ns	PLCC
512 x 9	LH5496/96H	AMD	Am7201	15 to 80 ns	DIP/PLCC
		Cypress	CY7C420		DIP
			CY7C421		DIP/PLCC
		Dallas	DS2009		
		IDT	IDT7201		
		Micron	MT52C9005		
		Mosel/Vitelic	MS7201A		
		MUSIC	MU9C7201		
		Quality	QS7201/8201		
		Samsung	KM75C01		
		SGS	MK4501		
1,024 x 9	LH5497/97H	AMD	Am7202A	15 to 80 ns	DIP/PLCC
		Cypress	CY7C424		DIP
			CY7C425		DIP/PLCC
		Dallas	DS2010		
		IDT	IDT7202		
		Micron	MT52C9010		
		Mosel/Vitelic	MS7202A		
		MUSIC	MU9C7202		
		Quality	QS7202/8202		
		Samsung	KM75C02		
2,048 x 9	LH5498	AMD	Am7203	15 to 80 ns	DIP/PLCC
		Cypress	CY7C428		DIP
			CY7C429		DIP/PLCC
		Dallas	DS2011		
		Hitachi	HM63921		
		IDT	IDT7203		
		Micron	MT52C9020		
		Mosel/Vitelic	MS7203		
		MUSIC	MU9C7203		
		Quality	QS7203/8203		
		Samsung	KM75C03		
		SGS	MK4503		
4,096 x 9	LH5499	AMD	Am7204	20 to 80 ns	DIP/PLCC
		Cypress	CY7C432		DIP
			CY7C433		DIP/PLCC
		Dallas	DS2012		
		Hitachi	HM63941		
		IDT	IDT7204		
		Mosel/Vitelic	MS7204		
		MUSIC	MU9C7204		
		Quality	QS7204/8204		

* Released to production as of the date of publication of this data book.

APPLICATION NOTES

Pseudo SRAMs 256K (32K × 8), 1M (128K × 8), 4M (512K × 8)

Bob Laird, Field Applications Engineer

INTRODUCTION

The Sharp LH5P8512 is a 4M bit Pseudo-Static RAM (PSRAM) manufactured on a 0.8 µm CMOS process in one of Sharp's state-of-the-art wafer fabs. The LH5P8512 is the newest member of SHARP's family of PSRAMs that began with the 256K bit LH5P832.

Sharp is committed to expanding its presence in the PSRAM market, which has been growing rapidly over the last few years. Initially developed as a low-cost alternative to a Static RAM (SRAM), the PSRAM has also successfully replaced Dynamic RAMs (DRAM) in certain applications. This application note will discuss the advantages and disadvantages of using a PSRAM over an SRAM or DRAM.

DEFINITIONS

A **DRAM** is a volatile, dynamic memory IC. Volatile means that if it loses power, it will also lose its memory. Dynamic means that it must constantly be refreshed since the memory cell itself utilizes a small storage capacitor that must be constantly recharged. Refresh is accomplished when the memory contents of a row of cells are read by the sense amplifiers, and the logic states that were read are amplified and written back to the cells.

An **SRAM** is a volatile, static memory IC. Static means that it will maintain its memory indefinitely with no external clocking, as long as power is supplied. The memory cell is a simple latch that is either set or reset depending on the data that was written to it.

A **PSRAM** is a volatile, dynamic memory IC. It uses the same memory cell structure as a DRAM. Like a DRAM, a PSRAM must be refreshed, but it incorporates the refresh timing and control logic on-chip to simplify and minimize external logic. Having the refresh logic circuitry on-chip also provides more flexibility to the designer to reduce the power consumption of the PSRAM. The benefit of this is discussed later.

The Pseudo SRAM got its name because it was designed to be offered in the same package and have the same pinout as an SRAM. A PSRAM, while pin-for-pin compatible with an SRAM, would not be a direct drop-in replacement because it must be refreshed.

Schematic diagrams of the memory cell structures for the DRAM/PSRAM and SRAM are shown in Figure 1. For the SRAM, the cell structure shown is the most commonly used by SRAM vendors. There are SRAMs available with 6-transistor cell structures for ultra-low power applications, but they will not be discussed in this application note.

Pinout diagrams for the 4M bit versions of the PSRAM, SRAM, and DRAM are shown in Figure 2.

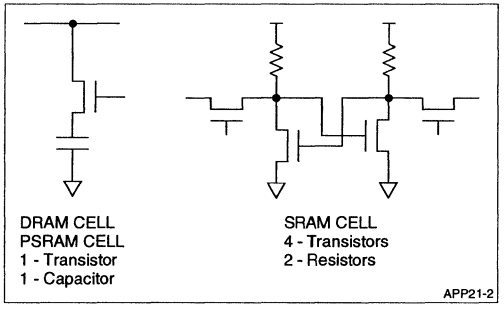


Figure 1. Memory Cell Structures for DRAM/PSRAM and SRAM

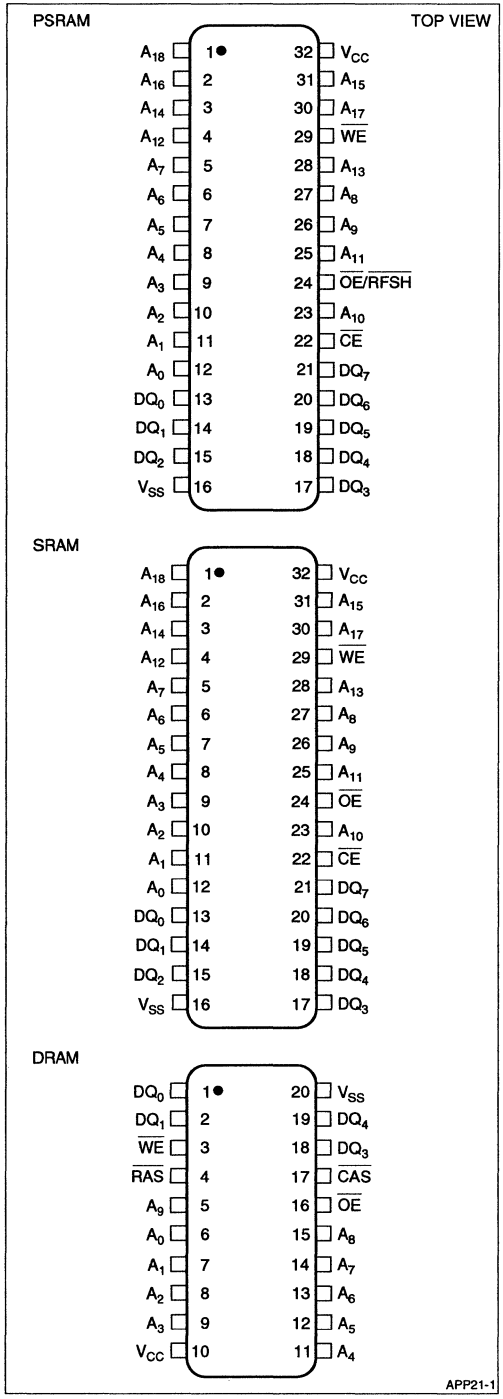


Figure 2. Pin Connections for PSRAM, SRAM and DRAM Packages

ADVANTAGES AND DISADVANTAGES

The major considerations when deciding which memory IC to use in your design are as follows:

1) Cost
2) Density and speed
3) Design ease
4) Power consumption

1) Cost

The PSRAM carries a small-cost premium over DRAM because of its added circuitry. The premium has been 1.2× to 1.4×, but it is expected to decrease as the volume usage of PSRAMs increases.

The DRAM has traditionally been the high-volume memory of choice based on its low cost per bit, high density, and small package. It is ideal for large systems that use many Megabytes of memory.

The SRAM is the most expensive of the three technologies. The memory cell area of an SRAM is much greater than that of the DRAM/PSRAM, resulting in a much larger die size. On a cost-per-bit basis, an SRAM is typically 3× to 4× that of a DRAM. The differences in cell complexity can be seen in Figure 1.

2) Density and Speed

Design engineers selecting the density of their memory ICs must consider what is currently available on the market versus next generation devices. The PSRAM utilizes a DRAM for its base design, so it tends to lag behind the DRAM design introduction by a year or more. Since the DRAM, with its small cell size, is easier to manufacture than an SRAM of the same density, DRAMs and PSRAMs lead SRAMs to market by at least one generation. Today, leading DRAM vendors are just starting small volume production of 16M bit DRAMs while the 4M bit PSRAM is readily available on the market. Leading SRAM manufacturers are just starting to sample 4M bit SRAMs. New DRAMs have historically gone to market with a very high initial cost. The PSRAM tends to go to market with a cost comparable to its corresponding DRAM, which has come down the cost curve, making it attractive for new designs. Compared to an SRAM then, the PSRAM will be one generation ahead in density, and very cost competitive from its introduction.

PSRAMs (and DRAMs) compete against SRAMs in what would be considered the slow-speed classification. The 4M bit PSRAM is offered with access times ranging from 60 ns to 80 ns and cycle times from 110 ns to 130 ns, respectively. Slow 1M bit SRAMs are available with access times of 70 ns or 100 ns. For an SRAM, the access time and cycle time are the same simplifying system timing requirements. DRAMs have speeds comparable to or slightly faster than PSRAMs. Fast SRAMs, with sub 45 ns access times, fulfill a speed requirement for high-end systems that DRAMs and PSRAMs cannot fill. There-

fore, PSRAMs and DRAMs do not compete against fast SRAMs.

3) Design Ease

A DRAM is the most complex device to design with because of its multiplexed addressing and refresh circuitry requirements. The address provided by the microprocessor while it is accessing memory does not multiplex the address. Therefore, decode logic is required between the DRAM and microprocessor to perform the multiplexing function. No such logic is required for PSRAMs or SRAMs.

The refresh specification for the DRAM and PSRAM defines the maximum time allowed between refreshes. This means that both the DRAM and PSRAM require a timer circuit to monitor the refresh time, and also control logic to provide the refresh clocking. Both the DRAM and PSRAM have internal counters that can be used to provide the refresh address. On DRAMs, it is called a $\overline{CAS}$ before $\overline{RAS}$ refresh. On PSRAMs, it is called Auto refresh. In either case, external refresh clocking is required. An example of the refresh timing is shown in Figure 3. This timing represents the refresh of one row internal to the memory. The 4M bit PSRAM requires that 2048 rows be refreshed every 32 ms.

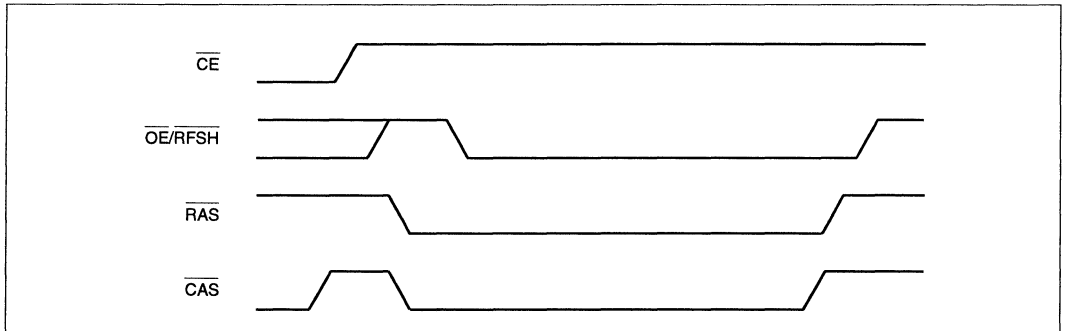
One large advantage that a PSRAM has over a DRAM is a Self Refresh mode. The PSRAM can be put into Self Refresh mode in which an internal clock provides the refresh timing, and no external timing is required. It is very useful during standby mode when memory is not being accessed. The timing for Self Refresh looks the same as that for Auto Refresh except that the OE/RFSH pin must be held LOW for longer than 8 µs. After 8 µs, the internal Self refresh clock begins to automatically refresh the memory array. It will continue to refresh the array as long as OE/RFSH is held LOW with CE held HIGH.

The standard through hole package for the 4M bit PSRAM (and SRAM) is a 32-pin, 600-mil PDIP. For the 4M bit DRAM (1M × 4), it is a 20-pin, 300-mil DIP. The DRAM package is the smaller package, which is preferred because it helps reduce board size. One reason that it has a smaller package is that the DRAM has fewer outputs than the others. The DRAM is organized as 1M x 4 while the PSRAM and SRAM are organized as 512K x 8. The wide width of the PSRAM and SRAM is advantageous for small memory systems. For example, assume that a system required no more than 512Kb of density. If this system used one of the common microprocessors on the market that has a 32-bit data bus, then you would need four 512K × 8 memories to meet the required data width. The same system would need eight 1M × 4 DRAMs to meet the same 32-bit width. Recently, some DRAM vendors announced plans to offer devices with ×8 configurations, targeting small and medium size systems.

A second reason for the smaller package is that the DRAM has almost half the number of addresses as the PSRAM or SRAM. This is because it uses multiplexed addressing. Multiplexing allows you to clock in two different 10-bit addresses on the same address pins to achieve the 20 address bits required to select one of the 1M different memory locations. On the PSRAM and SRAM, you must provide all of the required 19 address bits at the same time to select one of the 512K memory locations.

4) Power Consumption

There is not a significant difference in operating power consumption for a PSRAM, SRAM, and DRAM. The operating power is composed primarily of switching currents from the CMOS peripheral circuits surrounding the memory arrays, and those circuits are reasonably similar for all three memories. Differentiation is seen in standby power. The term standby means that no Reads or Writes



NOTES:
1. PSRAM auto refresh (cycle $\overline{RFSH}$ pin while $\overline{CE}$ inactive HIGH).
2. DRAM $\overline{CAS}$ before $\overline{RAS}$ (cycle $\overline{CAS}$ active LOW before $\overline{RAS}$).

APP21-3

Figure 3. Refresh Timing

are taking place. A sample of standby current (I_{SB}) specifications is given below. Note that a DRAM must have its supply voltage maintained within the operating range (4.5 V ~ 5.5 V) during standby, but with SRAMs and 4M bit PSRAMs the supply voltage can be dropped to a data retention voltage (typically 3 V) during standby, significantly reducing power consumption.

	4M Bit PSRAM	4M Bit DRAM	1M Bit SRAM
I_{SB} max @ V_{CC} = 5 V	100 µA	1 mA	100 µA
I_{SB} max @ V_{CC} = 3 V	50 µA	–	50 µA

The standby current given for the PSRAM at V_{CC} = 3 V is actually a self refresh current, so it includes the additional current required to perform the internal refresh. The standby current given for the DRAM does not include refresh current. The typical standby current seen with an SRAM is actually much lower than that for a PSRAM, making SRAMs the best choice for low standby power consumption.

Low-standby power consumption is a critical parameter for battery operated systems such as Notebook computers. A decrease in power consumption directly translates to an increase in battery life. PSRAMs have proven to be an ideal choice for main memory in the Notebooks where low-power consumption is required at a reasonable cost.

For systems requiring a small amount of memory to be battery backed up (usually a small 3 V lithium battery), an SRAM is still the memory of choice, due to its low I_{SB} and static operation.

SUMMARY

Pseudo-Static RAMs have advantages and disadvantages when compared to either SRAMs or DRAMs. The market has shown that the PSRAM can win designs against either, depending on the application. A summary of the advantages and disadvantages is given below.

ADVANTAGE	DISADVANTAGE
Versus SRAM	
Much lower cost	More complex design
Higher density	Higher standby power
Versus DRAM	
Lower standby power	Higher cost
Ease of design	Larger Package
	Lag in time-to-market

PARITY CHECKING IN THE LH5420 BiFIFO

Bob Laird, Field Applications Engineer

INTRODUCTION

Sharp's LH5420 256 × 36 × 2 bidirectional FIFO (BiFIFO) was the first monolithic FIFO from the semiconductor industry to offer customers a full 36-bit data word-width.

The LH5420's 36-bit wordwidth makes it the ideal choice for those 32-bit or 64-bit systems which use parity. It remains an ideal choice, even for those wide-word systems that don't use parity, because there are no available 32-bit FIFOs, and because systems frequently use an extra bit per byte for some type of 'tag' information anyway.

WHAT IS PARITY?

Many systems need to have error detection and correction (EDAC) implemented into the design, but cannot afford the added overhead – memory requirements increase dramatically. The most common compromise is to use just error detection.

By adding a single bit to each byte of data, the occurrence of single-bit errors may be monitored. This extra bit is referred to as the *parity bit.*

Parity is not a perfect means of detecting errors; but it is easy to implement. In fact, many off-the-shelf memory, microprocessor, and general-purpose-logic integrated circuits make provision for parity bits.

A system using parity requires a *parity-generation* circuit. The purpose of a parity-generation circuit is to examine each data byte, and set that byte's parity bit based on the number of ones (logic 'HIGH' levels) in the eight data bits.

Either 'odd parity' or 'even parity' may be chosen. These are defined as follows:

Odd Parity: The parity bit is set to one if there is an even number of ones; otherwise, it is cleared (not set). Thus, the total number of ones, *including* the parity bit, is odd.

Even Parity: The parity bit is set to one if there is an odd number of ones; otherwise, it is cleared (not set). Thus, the total number of ones, *including* the parity bit, is even.

In either case, a single-bit error in any bit position within a data byte, including an error in the parity bit itself, causes a parity-error indication.

The type of parity chosen may be dictated by the system design. However, neither type of parity offers any major economic or performance advantage over the other one. Some designers prefer odd parity, on the grounds that the correct parity bit is a one for an all-zero byte. Thus, a *completely*-blank byte (which presumably arose from some type of data-recording failure) shows up as having a parity error.

In any case, it is a good idea to maintain the same type of parity throughout the entire system.

LH5420 PARITY CHECKING

The LH5420 offers parity checking, which means that it examines each data byte to determine what its parity is, thereby computing an internal parity bit for that byte. This parity bit then is compared with the Parity Mode bit in the LH5420's Control Register. If they do not match, then there is the presumption of a parity error in that byte.

Since an LH5420 word is 36 bits wide, parity checking is done in parallel on the four bytes that make up a 36-bit word. If an error is detected in ANY of these four bytes, the parity flag is asserted LOW, indicating the parity error.

Figures 1 and 2 show the parity-flag logic for Port A. The ten-bit parity trees for the other three bytes are configured identically with the one shown in Figure 1, which is for the low-order byte. Also, the parity-flag logic for Port B is configured identically with that for Port A.

Since there is parity-flag circuitry associated with both LH5420 ports, data words may be checked both entering and exiting the BiFIFO. The parity-tree inputs are connected to the actual port input/output *pads*, through isolation transistors. Data words are monitored as they change on the system bus, which connects to the pads at that port.

It should be noted that the parity-flag circuitry at an LH5420 port is *not* controlled by the Output Enable ($\overline{OE}$) control signal at that port. Hence, parity checking *always* is active, regardless of whether or not the BiFIFO itself is driving the system bus. Therefore, as data constantly

changes on the bus, the parity flag may keep on changing states also. Some transitions on the data lines may make it appear that a parity error has occurred.

According to the LH5420 data sheet specification, the parity flag at a port is not guaranteed to be valid, until some given delay time *after* stable data is present at the input/output pads. For the LH5420P-25, for instance, this delay time is a maximum of 17 ns. Thus, to monitor the parity of data entering the LH5420, the sum of the data setup time and the data hold time must be sufficient to satisfy this 17 ns delay time.

Also, when monitoring the parity of data words being read from the LH5420, it is necessary to keep $\overline{OE}$ asserted long enough to satisfy this parity-flag delay time. If the LH5420 is being operated at the minimum cycle time of 25 ns, then $\overline{OE}$ would have to remain asserted 6 ns into the next cycle. In most designs, this requirement does not present a problem.

As it is, an LH5420 cannot perform a read operation and a write operation on *consecutive* cycles, when operating at the *minimum* cycle time. The reason is that the sum of the data-access time (for outbound data words) and the data-setup time (for inbound data words) already exceeds the minimum cycle time, for all three LH5420 speed grades.

The LH5420 Control Register Parity Mode bit is initialized for odd parity during a reset operation. However, it may be reprogrammed for even parity, and then back to odd parity, at will during system operation. Programming is performed by loading a full 36-bit word into the Control Register from Port A, with the code HLL at the LH5420's Address (resource-register-selection) inputs A_{2A}-A_{0A}. The least-significant bit of that 36-bit word, D_{0A}, selects the Parity Mode: HIGH for odd, and LOW for even. The Control Register is written into at the next rising edge of CK_A.

Note that the Control Register is a 'blind' or write-only register. The system cannot read it back.

The normal convention for parity-bit position is to use the most-significant bit of each byte; that is, D_{8A}, D_{17A}, D_{26A}, D_{35A}, D_{8B}, D_{17B}, D_{26B}, and D_{35B}. Now, the LH5420 is designed in such a way that *any* bit position within a data byte may be used as the parity bit. However, when programming the Almost-Full Flags and the Almost-Empty Flags, the offset values are written into the resource register using data pins D_{0A}-D_{7A}, D_{9A}-D_{16A}, D_{18A}-D_{25A}, and D_{27A}-D_{34A}. Thus, there is a presumption that the least-significant eight bits of a byte are 'the data bits.'

So, for systems using byte parity with the most-significant bit as the parity bit, which use the programmable-flag feature, the fields line up as they should. Otherwise, special consideration must be given when using the parity bit as a data bit for programming.

Figure 1 is a simple schematic for the ten-bit parity-checking logic circuit for one byte, in this case the least-significant byte at Port A. The tenth bit is the Control Register Parity Mode bit. Since this bit is HIGH for odd parity and LOW for even parity, the output of the ten-bit parity checker is LOW whenever the parity of the data byte being examined agrees with the LH5420's Parity Mode bit.

The parity-circuit outputs for the four bytes of Port A, designated in Figure 1 as PC_{0A}-PC_{3A}, are NORed together to compute the parity flag $\overline{PF_A}$. Similar logic is used at Port B, to compute $\overline{PF_B}$.

Note that the $\overline{PF_A}$ and $\overline{PF_B}$ NOR gates do not incorporate latches. The states of these two outputs depend directly on the data words present at Port A and at Port B respectively.

USING PARITY CHECKING TOGETHER WITH WORDWIDTH SELECTION

Another useful feature offered by the LH5420 BiFIFO is *wordwidth selection*, also known as *funneling/defunneling*, at Port B. Port A always assumes a wordwidth of 36 bits. But Port B may assume a 36-bit, 18-bit, or 9-bit wordwidth, according to the setting of two LH5420 control input signals, WS_0 and WS_1. In the latter two cases, there is an effect on parity checking at Port B.

For example, assume that Port B has been set for 9-bit wordwidth. As a byte is being written into D_{0B}-D_{8B}, the lowest-order Port B byte, the Port B parity checker is monitoring not only this byte, but also the three *unused* bytes D_{9B}-D_{35B}. If any of those three bytes has improper parity, according to the current Parity Mode setting, then $\overline{PF_B}$ is asserted LOW to indicate a parity error.

If the Port B 9-bit-wordwidth setting never changes during system operation, then it may be advantageous to tie pins D_{9B}-D_{35B} all HIGH for odd parity, or all LOW for even parity. Similar statements apply for pins D_{18B}-D_{35B}, given the use of 18-bit wordwidth at Port B.

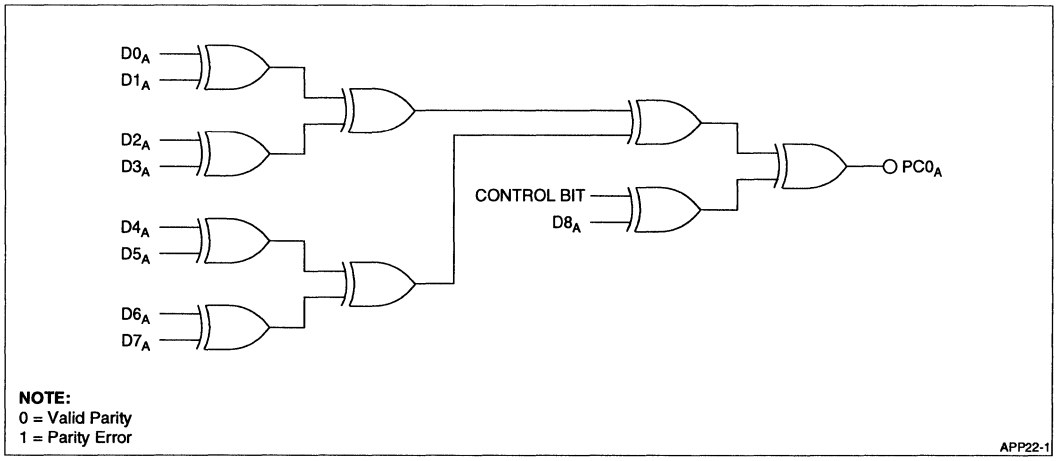


Figure 1. Example of Byte-Parity Gate: Port A, Low Order Byte

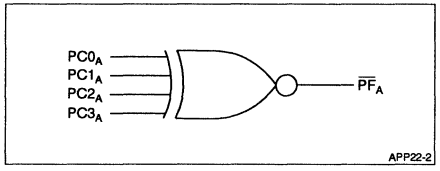


Figure 2. Example of Parity-Flag Logic: Port A

When outputting a byte from Port B with 9-bit word-width in effect, the LH5420 actually conveys a full 36-bit word to the output buffers; although, presumably, the other devices on the output bus are examining only D_{0B}-D_{8B}. Presenting the remaining bytes to the output bus is accomplished by circular-shifting operations, which are inherently available in the Port B output logic. The second byte of the word is read by shifting D_{9B}-D_{17B} down to D_{0B}-D_{8B}. Concurrently, D_{27B}-D_{35B} are shifted down to D_{18B}-D_{26B}, D_{18B}-D_{26B} are shifted down to D_{9B}-D_{17B}, and D_{0B}-D_{8B} are shifted circularly to D_{27B}-D_{35B}.

This circular-shifting procedure is repeated twice more, for the remaining two bytes of that data word. After that, another full 36-bit data word is again fetched, to output the next byte. Assuming that the fetched data bytes all have correct parity, then $\overline{PF}_B$ continues to indicate correct parity, after each successive circular shift of the data word.

SUMMARY

Sharp's LH5420 256 × 36 × 2 BiFIFO features two built-in parity checkers, one connected to each 36-bit data bus. The parity of each 9-bit data byte may be checked twice as it passes through an LH5420: once as it enters, and once as it leaves.

An LH5420 parity checker may be used to examine a data word which is present on either of the LH5420's two 36-bit data buses, even if that word never actually gets read into one of the LH5420's internal FIFO memories.

The LH5420 may be programmed to consider either odd parity or even parity as correct. A parity error in any byte, of a data word passing through an LH5420 port, is signaled by asserting the LH5420's parity flag at that port LOW, as long as that data word remains present there.

Proper use of this port parity flag can detect *any* single-bit error in *any* data byte passing through an LH5420, assuming that the parity flag gets read at the appropriate time. No additional hardware is required.

FIFO FLAG TIMING: MARCHING TO TWO DIFFERENT DRUMMERS *

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INTRODUCTION

A FIFO (First-In, First-Out memory device) can. be thought of as a 'passthrough window' between two *independently-clocked* digital subsystems – each marching to its own drummer, as it were. To adequately perform this role in practical digital systems, FIFOs are 'schizoid': they are memory devices, and they also are logic-synchronization circuits.

Increasingly, newer FIFOs have been made capable of recognizing commands from the overall digital system of which they are part, and also of providing that system with timely status information in the form of 'flag' values.

A FIFO can undergo a change in its status because of an event synchronized *either* to the subsystem at its input end, *or* to the subsystem at its output end. These two subsystems usually are independently clocked; and either of the two clock signals can affect a flag value. The external logic normally uses one or the other of these clock signals to synchronize reading the flag, which leads directly to a potential metastability hazard. The very newest FIFOs incorporate internal logic to minimize any practical metastability hazard; but, even then, their specifications have to include 'skew parameters,' which must be complied with by the external logic.

This paper includes a short review of FIFO basics, followed by a more detailed discussion of flag-synchronization and metastability issues. Finally, the flag-synchronization features of the new Sharp LH540215/25 18-bit synchronous FIFOs are described, as a case in point.

WHAT IS IT THAT FIFOs DO, IN THE FIRST PLACE?

Conceptually, using a FIFO as a 'passthrough window' accomplishes two related but different system functions:

- *Providing 'rubber-band memory'* between Subsystem A and Subsystem B.
- *Decoupling the clocking* of each subsystem from that of the other subsystem.

As long as each subsystem deals with the other subsystem through a FIFO, the two subsystems don't have to be synchronized or coordinated with each other in *any* way, at least for the purpose of passing a data stream from one to the other. This is a powerful *simplifying assumption* in digital-system design and integration. FIFOs often are used to save design effort and leadtime, and to reduce the complexity of timing logic, when interfacing two independent subsystems together.

Subsystem A, functionally upstream, stuffs data into a FIFO at whatever rate Subsystem A likes best; and Subsystem B, functionally downstream, unloads the data from the FIFO at whatever rate Subsystem B likes best. These rates may be derived from oscillator-driven clock circuits; or, they may not even be constant, if the 'clock' actually is an aperiodic 'demand' signal.

To cope with the requirements of this usage, a FIFO must include an *input register* which can be synchronized or 'clocked' by Subsystem A, and an *output register* which can be synchronized or 'clocked' by Subsystem B. In between, there needs to be the 'rubber-band memory.' (Also known as 'elastic storage,' if you prefer more formal-type technobabble.) This rubber-band memory should appear both to Subsystem A and to Subsystem B as having unlimited depth; that is, as containing enough words that neither subsystem ever bumps up against finite FIFO-memory capacity as a bothersome constraint. If you've designed with FIFOs previously, then maybe you knew all that.

Historically, FIFOs have been perceived by system-design engineers as *premium* semiconductor parts which Make Problems Go Away. That is, FIFOs are supposed to be *liberating*. It follows, of course, that these same customers can become severely annoyed with FIFOs, if they ever begin to feel that using FIFOs gets them entan-

* This paper was prepared for, and presented at, Northcon/93 and Wescon/93. It appeared in the *Northcon/93 Conference Record;* Session 12, paper 3. It also appeared in the *Wescon/93 Conference Record;* Session 26, paper 3.

gled in lots of timing hassles. But, sometimes, they fail to distinguish between those timing issues which arise from the use of a particular part, and those timing issues which arise *intrinsically* from the characteristics of their application.

REAL-WORLD MATHEMATICAL ISSUES WHEN USING FIFOs

The term 'FIFO' comes from operations research, a branch of mathematics. It stands for a *queue discipline*, that of 'First In, First Out.' The term FIFO also turns up in cost-accounting methodology, for reckoning the cost of items being withdrawn from an inventory after having been bought at varying prices.

The operations-research 'single-server' model fits FIFOs being used to buffer 'randomly-arriving' data, as well as fitting the classic example of hamburger stands serving 'randomly-arriving' customers. In this model, the arrival of a piece of data at the FIFO's input end ('a customer') and the unloading of a piece of data from the output end of the FIFO ('serving a customer') are random events. In between the input end and the output end, there is a *queue* of customers waiting to be served – here, words being temporarily stored within the FIFO's internal memory array. If you like mathematical lingo, the entire scene is a 'stochastic process,' meaning that the events which are occurring are 'probabilistic' and not 'determinate.'

Why is this operations research model of interest? In the 'single-server' model, the *queue length* is a 'random walk,' and – if it is given enough time to fluctuate – is *unbounded*, meaning that no FIFO used to queue up *truly* random data can *ever* be quite big enough, if it has to operate for an infinitely-long time. Thus, this operations-research model *in principle* contradicts the common-sense notion that there is some 'large-enough' size for every FIFO application.

So, it's *not* just that semiconductor manufacturers don't *choose* to develop FIFOs having deep-enough internal memory-array capacities. It's that there *isn't* any finite depth which can provide theoretically-*absolute* protection, in the *truly*-random case.

DESIGN STRATEGIES USING FIFOs

But, *in practical systems*, there always *is* a 'large-enough' FIFO size. The probability of any queue length growing past a certain value, before the next ice age, usually can be made *very* small without making the FIFO's queue-length capacity uneconomically large.

If a catastrophic increase in queue length starts to occur, often because of some sudden-onset system problem, the designer's line of defense is the FIFO's 'fullness flags.' If the system is monitoring these, they can provide an adequate early warning of impending trouble, so that the system can take timely and effective countermeasures.

The key point here is that *finite*-depth FIFOs – and the semiconductor industry hasn't built any other kind of FIFOs yet! – *must*, for basic *mathematical* reasons, incorporate some kind of bulletproof logic for dealing with 'full' and 'empty' queue conditions.

Of course, there are also 'block-oriented' FIFO applications, in which Subsystem A dumps another block of data into the FIFO only when the FIFO is less than half full, and the FIFO size has been chosen a priori to be large enough to hold *two* blocks of data. Here, Subsystem A is doing some of the 'elastic' adaptation to fluctuations in the data rate, and is no longer depending upon the downstream FIFO to do all of that adaptation. Consequently, not all of the pessimistic assumptions of the 'single-server' model still have to be satisfied. But limiting the queue length in this manner can exact a price, in some other system-level performance characteristic.

Prudent digital-system designers usually try to avoid *ever* allowing their FIFOs to get *either* completely 'full' *or* completely 'empty' during normal system operation. Following this rule means that many fascinating 'gotchas,' which in principle can raise their ugly heads at these boundary conditions, never get to disturb the serenity of the system's operation, or of the system designer's working day. However, the Product Engineering and Test Engineering staffs of semiconductor manufacturers often must spend major time and effort dealing with these boundary-condition 'gotchas.'

FIFO 'FULLNESS' STATUS FLAGS

Contemporary FIFOs commonly provide *several* status flags, to inform the system logic external to the FIFO as to the FIFO-memory array's relative state of fullness or emptiness. Often, there are five such flags: 'Full,' 'Almost Full,' 'Half Full,' 'Almost Empty,' and 'Empty.' These 'Almost' flags originated some years ago, as a semiconductor-piece-part adaptation of the 'Yellow Warning' interrupt-flag scheme used in DEC's PDP-11 family of minicomputers.

Sometimes, when there aren't quite enough pins to provide every FIFO feature desired by the semiconductor manufacturer and its customers, the 'Almost-Full Flag' signal and the 'Almost-Empty Flag' signal are combined as an 'inclusive-ORed' 'Almost Full/Empty Flag' signal on one pin. The external logic can distinguish these conditions one from another by examining the 'Half-Full Flag,' on the assumption that a FIFO which is 'almost full' can be presumed to be more than 'half full,' and likewise that a FIFO which is 'almost empty' can be presumed to be less than 'half full.'

This last assumption sounds obvious to the point of silliness. Still, it needs to be *rechecked* when designing with FIFOs which feature 'programmable' 'Almost-Full Flag' and 'Almost-Empty Flag' signals, whenever *large* 'offset' values are being 'programmed' into the 'offset-value registers' which are associated with each of these two flags. These 'offset' values define the 'almost-full' condition as some exact number of words away from 'full,' and the 'almost-empty' condition as some exact number of words away from 'empty.' Obviously, the rules are going to change, if ever one or both of these offset values exceeds half of the number of words in the FIFO-memory array.

THE FLAG-SYNCHRONIZATION DILEMMA

Back to Subsystem A, which is being synchronized by Clock A, and Subsystem B, which is being synchronized by Clock B. Subsystem A is 'synchronously' dumping data destined for Subsystem B into a FIFO, which is there to make everything come out OK so that Subsystem B can 'synchronously' read these same data back out.

Whenever Subsystem A stuffs in one more word, the FIFO can suddenly become 'full,' 'almost full,' or 'half full'; or it can suddenly cease to be 'almost empty' or 'empty.' Similarly, Subsystem B unloading one word can cause the FIFO now suddenly to become 'almost empty' or 'empty,' or now suddenly to cease to be 'full,' 'almost full,' or 'half full.' Thus, each flag signal can be affected for one transition by a 'write event,' and can be affected for the other transition by a 'read event.' Therefore,

> Events which can cause the state of any 'fullness flag' to change can occur at either end of the FIFO.

So, *each* of the five flags can change state *either* in synchronism with Clock A, *or* else with Clock B. So all five flags are 'synchronized to both clocks,' which is the same as saying that they aren't *really* synchronized to either clock – that is, that they are *asynchronous*. These statements, of course, apply strictly to the *internal* values of the five flags, as these values are computed by the FIFO's control circuits.

Incidentally, if this operational description seems to be stacked lopsidedly in favor of fullness, it's because the 'Half-Full Flag' customarily is called just that, rather than being called the 'Half-Empty Flag.' Probably, the term 'Half-Empty Flag' just sounded too negativistic for the tastes of positive-thinking FIFO marketeers! Anyway, the logic which controls the 'Half-Full Flag' behaves exactly in accordance with what one would expect from that name.

Now, in a 'synchronous' FIFO having 'enable' inputs as well as 'clock' inputs for both writing and reading, a 'write event' is synchronized to the 'write clock' input, and is made to occur by asserting the 'write enable' input. Likewise, a 'read event' is synchronized to the 'read clock' input, and is made to occur by asserting the 'read enable' input.

In principle, the 'write clock' and the 'read clock' both may be free-running periodic waveforms derived from crystal-oscillator frequency sources. However, most contemporary FIFOs avoid the use of any internal circuit techniques which would *require* that these 'clock' signals must be periodic.

So, now, what happens when either Subsystem A or Subsystem B wants to *read* the value of one of these flags? If Subsystem A and Subsystem B are connected by a 'synchronous' FIFO, then the logic outside the FIFO which is trying to read the FIFO's flag(s) very likely *also* is synchronized, probably either to the 'write clock' (here, Clock A) or to the 'read clock' (here, Clock B). Which is fine, as long as the flag value is stable, or as long as the most recent event which is capable of affecting this flag value was synchronized to the *same* 'clock' signal to which flag *reading* also is being synchronized.

But what, then, if the most recent event which has affected this flag value was synchronized to the *other* 'clock' signal? Then, we have a signal getting changed in synchronism with *one* 'clock' signal, but being read in synchronism with a second, *different* 'clock' signal which is not necessarily in any way synchronized or coordinated with the first 'clock' signal. Thus, the FIFO's flag output is most unlikely *always* to be meeting the setup-time and hold-time specifications for the downstream semiconductor-device input which it is driving.

METASTABILITY

This latter situation is, of course, the recipe for instant *metastability*. Metastability is a digital-system form of 'bad vibes.' It arises as the result of trying to read a digital signal while that signal is *changing*.

A potential 'metastability hazard' exists whenever the signal being read isn't a stable HIGH or a stable LOW, as of the exact instant when the clock-signal transition edge comes along to synchronize the reading process. If there are many ongoing attempts to read the signal, and the timing of the signal is unrelated to that of the clock signal, then what we have here is another example of a 'stochastic process.' And, eventually, there is bound to be an attempt to read the signal at *exactly* the wrong time.

When attempting to read such an unstable signal, three different outcomes are possible:

- The signal can be read as a HIGH.
- The signal can be read as a LOW.
- The reading circuit element itself can just get confused and 'hang up' in a 'metastable' state, outputting a signal close to its own input 'trip point' or 'transition threshold' for a while, before settling back either into a stable HIGH condition or else into a stable LOW condition.

This 'metastable' state can, in some circuit technologies, last for as long as *several* additional clock periods. Now, the probability of 'going metastable' remains very small as long as the reading circuit isn't being operated at a frequency really close to its maximum; but it increases, quite dramatically, as this maximum is approached. The potentially-ruinous impacts on system reliability are all too obvious.

Notice that we got into this metastability issue as a direct consequence of the burden which FIFOs are expected to take on in systems, of Making Synchronization Problems Go Away. Ultimately, metastability is not intrinsically just a circuit-design problem; it arises mathematically as an *operations-research* problem, when deterministic digital circuits are used – whether wittingly or not! – to try to deal with 'stochastic processes.'

RESYNCHRONIZING FLAG SIGNALS

FIFO customers, like customers for any other products, develop new Wants over time, as suppliers learn to satisfy their previous Wants. So customers *now* Want to be able to perform flag-reading operations from *whichever* end of the FIFO they wish, for *any* of the five usual 'fullness flags,' without having to spend time and circuit-board real estate protecting themselves against metastability hazards.

FIFO manufacturers first began to address this customer Want by attempting to handle the potential metastability problems internally *within* the FIFO, but for just two out of the five flags – the 'Full Flag,' and the 'Empty Flag.' The approach was to resynchronize each of these two flag signals, for *both* of its possible state transitions, to the clock signal for that end of the FIFO where there usually is the greatest interest in reading that flag: the 'Full Flag' to the 'write clock,' and the 'Empty Flag' to the 'read clock.'

The premise for these choices was, of course, that it's essential for Subsystem A to know if a FIFO which it's trying to write into is 'Full'; if it is, then the write operation can't be completed. But there's no similarly-urgent reason why Subsystem A needs to know if the FIFO which it's trying to write into is 'Empty.' Analogous reasoning also applies at the other end of the FIFO, where words are being read out.

USING PROGRAMMABLE FLAGS TO DO END-OF-BLOCK DETECTION

Certainly, this resynchronization of the external values for the 'Full Flag' and the 'Empty Flag' was a step in the right direction. It costs some on-chip resynchronizing flipflops; but it provides system designers with an easier-to-use FIFO part. But it didn't go quite far enough, since customers *also* turned out to be intensely concerned about getting absolutely dead-on-accurate readings from the 'Almost-Full Flag' and from the 'Almost-Empty Flag' – not just readings accurate to within a word or two.

A puzzling attitude, if one assumes that these latter flags are being used *only* as warnings to the system that it needs to do something soon, before the FIFO becomes either *completely* full or else *completely* empty as the case may be. But, as often happens, customers found a major use for the 'Almost-Full Flag' feature and the 'Almost Empty Flag' feature which was utterly different from the type of use planned for by the semiconductor manufacturers. In this case, the unanticipated major usage was as *cheap block-length counters.*

The semiconductor industry originally opened the door to this block-length-counter trick, while trying simultaneously to satisfy all of the different customers who could not agree on just what 'almost full' and 'almost empty' ought to mean – that is, how many words away from 'full' should be defined to mean 'almost full,' and how many words away from 'empty' should be defined to mean 'almost empty.'

The industry's response was to say, in effect, "Hey, you guys decide," by including *programmable registers* within FIFOs to hold 'offset values' which could be loaded during the operation of a system. These 'offset values' allowed the system to *specify* the 'how-many-words-away' parameters, during operation.

In older-architecture FIFOs which date back to when 'almost' flags first were introduced, these 'offset values' were *fixed*, 'wired-in,' architectural-design parameters. There are even certain newer FIFOs which have wired-in offset values, generally because they come in small packages without any extra pins to spare which could be used for controlling the necessary programmable registers, if their offset values were to be specifiable. Eight has been one very common wired-in offset value.

However, the very newest FIFOs generally have architectural provisions for reading in these 'offset values' from the external logic. If the external logic never gets around to imposing its own choice of 'offset values' on the FIFO, the FIFO's 'default values' for these parameters remain

in effect during system operation. Again, eight is a very common 'default value.' Another frequent choice is one-eighth of the FIFO depth.

As for block-length counting, to make a long story short, if the sum of the two 'offset values' and the desired block length equals the depth of the FIFO, then the system can use a state change by one of the 'almost' flags as an 'end-of-block' signal. The details are left as an Exercise For The Reader.

A CONTEMPORARY EXAMPLE OF SYNCHRONOUS-FIFO ARCHITECTURE

Consider now Sharp's new 18-bits-wide synchronous FIFOs, LH540215 (512 x 18) and LH540225 (1024 x18). These new x18 FIFOs are pin-compatible drop-in replacements for the IDT72215B and IDT72225B x18 synchronous FIFOs. But they also have some useful enhanced features, which go some ways beyond the architecture of the original IDT parts.

Naturally, they offer programmable offset-value registers for the Almost-Full Flag ($\overline{PAF}$) and the Almost-Empty Flag ($\overline{PAE}$). The default values for the contents of these registers are one-eighth of the FIFO depth, minus one.

Also, the LH540215/25's Full Flag ($\overline{FF}$) and Empty Flag ($\overline{EF}$) signals have been made to behave fully 'synchronously,' as far as the outside world is concerned. In order to avoid metastability problems, these flags have been *resynchronized*, to the clock at that end of the FIFO where the external logic is most likely to be trying to read them.

To review the rationale for this resynchronization, Subsystem A (the writing/input side) normally won't need to read $\overline{EF}$, since writing can occur at any time when the FIFO isn't actually full. Likewise, Subsystem B (the reading/output side) normally won't need to read $\overline{FF}$, since reading can occur at any time when the FIFO isn't actually empty. Therefore, $\overline{FF}$ has been resynchronized to change *only* as the result of a rising edge of WCLK (the writing-side clock); and $\overline{EF}$ has been resynchronized to change *only* as the result of a rising edge of RCLK (the reading-side clock).

This flag-signal behavior is probably optimum, from the viewpoint of a digital-system designer trying to make use of these FIFOs. However, for the resynchronization circuits within the FIFO to have time to function properly, it has proven necessary to specify two new 'skew' timing parameters, t_{SKEW1} and t_{SKEW2}; see Figure 1 and Figure 2.

t_{SKEW1} is the minimum delay for a rising edge of WCLK to occur after a rising edge of RCLK, in order to guarantee that the value of $\overline{FF}$ will be accurate as of *this* rising edge of WCLK, and won't get delayed until the *next* rising edge of WCLK. Similarly, t_{SKEW2} is the minimum delay for a rising edge of RCLK to occur after a rising edge of WCLK, in order to guarantee that the value of $\overline{EF}$ will be accurate as of *this* rising edge of RCLK, and will not get delayed until the *next* rising edge of RCLK.

Impatient digital-system designers sometimes are annoyed by having to observe the timing restrictions implied by these 'skew parameters.' However, even the fastest digital logic can't respond instantaneously. It appears that their objections really are to restrictions which are *inherent* in what FIFOs must be, if they are to solve the system timing problems which they are expected to solve. The basic flag-synchronization problem can be moved around, and changed in form, in all sorts of different ways; but it can't ever be totally *eliminated*.

Because a FIFO is inherently a pass-through window, between two logic subsystems which are synchronized *differently*, at *some* point there is always going to be a *boundary* between these two subsystems. And, at this boundary, the system designer inevitably is going to have to make allowances for some 'boundary effects.'

THE 'MIDDLE' FLAG SIGNALS

In the IDT x18 FIFOs, the three 'middle' flags – the 'Programmable Almost-Full Flag' ($\overline{PAF}$), the 'Half-Full Flag' ($\overline{HF}$), and the 'Programmable Almost-Empty Flag' ($\overline{PAE}$) – have been passed straight through to the outside world in the exact same form in which, as we have seen, the FIFO's internal logic inevitably must generate them. That is, these flags are 'synchronized to both clocks,' which is to say that they are 'asynchronous.'

But the Sharp x18 replacements for these IDT parts go one step further. They incorporate a programmable 'Control Register,' by means of which the system can specify 'synchronous' behavior for these three 'middle' flags *also*.

$\overline{PAF}$, like $\overline{FF}$, normally gets read at the writing side of the FIFO; and so there is a Control-Register bit which can be used to program $\overline{PAF}$ to be resynchronized to WCLK. $\overline{PAE}$, like $\overline{EF}$, normally gets read at the reading side of the FIFO; and so there is a Control-Register bit which can be used to program $\overline{PAE}$ to be resynchronized to RCLK.

However, a priori, $\overline{HF}$ is equally likely to be needed at *either* end of the FIFO. Therefore, *two* Control-Register bits have been allocated for $\overline{HF}$ resynchronization. The system can select either WCLK or RCLK as the resynchronizing clock for $\overline{HF}$. Or, it can leave $\overline{HF}$ 'synchronized to both ends of the FIFO' – i.e., as 'asynchronous.'

These Sharp x18 FIFOs incorporate an 'Enhanced MODE' control signal ($\overline{EMODE}$), which allows the system to select between two different sets of Control-Register 'default' conditions. If $\overline{EMODE}$ is held HIGH during a reset operation, the FIFO is initialized to function exactly like

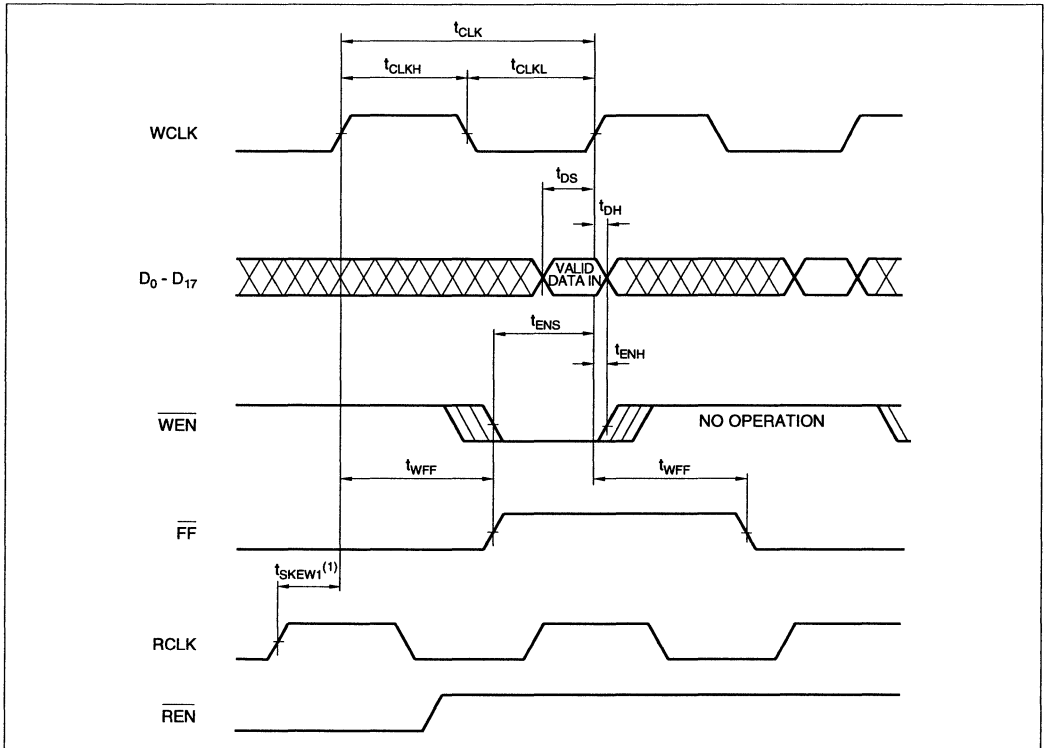
the same-depth IDT ×18 FIFO. But, if $\overline{EMODE}$ is held LOW during a reset operation, a selection is made from the Sharp ×18-FIFO menu of enhanced features; see Table 1. Also, the Control Register then becomes accessible for further modification of these selections.

The pin used for the $\overline{EMODE}$ control input is a Vcc pin in the IDT72215B and IDT72225B ×18 FIFOs. So, whenever the Sharp LH540215 and LH540225 ×18 FIFOs are used in pre-existing IDT ×18-FIFO sockets, they automatically get 'strapped' (pin-programmed) to behave exactly like the IDT FIFOs which they are replacing.

SUMMARY

A FIFO's mission is to serve as a 'pass-through window' between two conceptually-independent subsystems, which should not need to be coordinated or synchronized together in any way. To perform this mission well, the FIFO must provide *'rubber-band memory'* between the two subsystems, and also must *decouple* their clocking synchronizations one from another.

In its 'pass-through window' role, the FIFO itself has its input side and its output side 'marching to two different drummers.' The values of the FIFO's status flags, by which the FIFO informs the outside world of its state of



NOTE:

1. t_{SKEW1} is the minimum time between a rising RCLK edge and a rising WCLK edge for $\overline{FF}$ to change predictably during the current clock cycle. If the time between the rising edge of RCLK and the rising edge of WCLK is less than t_{SKEW1}, then it is not guaranteed that $\overline{FF}$ will change state until the next following WCLK edge.

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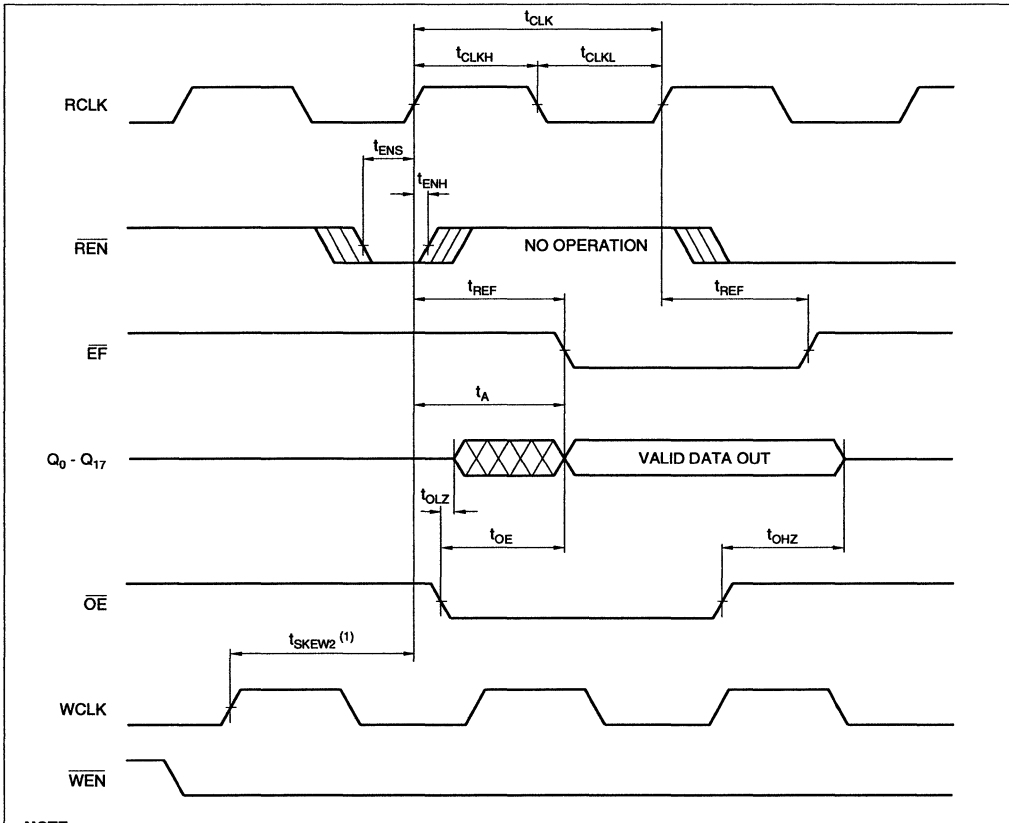
Figure 1. Synchronous Write Operation

relative fullness or emptiness, arise from computations which unavoidably are synchronized first to one subsystem, and then to the other.

These status-flag values must be *resynchronized* to one or the other of the two subsystem clocks. Otherwise, the external logic must contend with the hazards of *metastability*, which can give rise to profound system processing errors if no countermeasures are taken.

Two new Sharp ×18 synchronous FIFOs, the LH540215 (512 × 18) and LH540225 (1024 × 18), offer advanced new functionality for controlling status-flag synchronization. For practical purposes, when reading status-flag values, fully-synchronous status flags can reduce the risk of metastability to negligible levels.



NOTE:

1. t_{SKEW2} is the minimum time between a rising WCLK edge and a rising RCLK edge for $\overline{EF}$ to change predictably during the current clock cycle. If the time between the rising edge of WCLK and the rising edge of RCLK is less than t_{SKEW2}, then it is not guaranteed that $\overline{EF}$ will change state until the next following RCLK edge.

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Figure 2. Synchronous Read Operation

Table 1. Control-Register Format for Sharp LH540215/25 ×18-Bit FIFOs

CONTROL REGISTER BITS	CODE	VALUE AFTER RESET		FLAG AFFECTED, IF ANY	DESCRIPTION	NOTES
		$\overline{EMODE}$ = H	$\overline{EMODE}$ = L			
00	L	L	H	–	Deassertion of $\overline{LD}$ does not reset the programmable-register write pointer and read pointer.	IDT-compatible addressing of programmable registers.
	H				Deassertion of $\overline{LD}$ resets the programmable-register write pointer and read pointer to address Word 0, the Programmable-Almost-Empty-Flag-Offset Register. The change takes effect after a valid write operation or a valid read operation, respectively.	Non-ambiguous addressing of programmable registers.
01	L	L	H	$\overline{PAE}$	Set by ↑RCLK, reset by ↑WCLK.	Asynchronous flag clocking.
	H				Set and reset by ↑RCLK.	Synchronous flag clocking.
03, 02	LL	LL	HH	$\overline{HF}$	Set by ↑WCLK, reset by ↑RCLK.	Asynchronous flag clocking.
	LH				Set and reset by ↑RCLK.	Synchronous flag clocking at output port.
	HL, HH				Set and reset by ↑WCLK.	Synchronous flag clocking at input port.
04	L	L	H	$\overline{PAF}$	Set by ↑WCLK, reset by ↑RCLK.	Asynchronous flag clocking.
	H				Set and reset by ↑WCLK.	Synchronous flag clocking.
05	L	L	H	–	$\overline{OE}$ has no effect on an internal read operation, apart from disabling the outputs.	Allows the read-address pointer to advance even when $Q_0 - Q_{17}$ are not driving the output bus.
	H				$\overline{OE}$ inhibits a read operation whenever the data outputs $Q_0 - Q_{17}$ are in the high-Z state.	Inhibits the read-address pointer from advancing when $Q_0 - Q_{17}$ are not driving the output bus; thus, guards against data loss.
06	L	L	L	–	Reserved.	Future use to control depth cascading and interlocked paralleling.
	H					
07, 08, 09, 10,11	LLLLL	LLLLL	LLLLL	–	Reserved.	Reserved.

NOTES:

1. *When $\overline{EMODE}$ is HIGH, and Control Register bits 00-05 are LOW, the FIFO behaves in a manner functionally equivalent to the IDT72215B/25B FIFO of similar depth and speed grade. Under these conditions, the Control Register is not visible or accessible to the external system which includes the FIFO.*
2. *If $\overline{EMODE}$ is not asserted (is HIGH), Control Register bits 00-05 remain LOW after a reset operation. However, if $\overline{EMODE}$ is asserted (is LOW) during a reset operation, Control Register bits 00-05 are forced HIGH, and remain HIGH until changed. Control Register bits 06-11 are unaffected by $\overline{EMODE}$.*

BOLD ITALIC = Enhanced Operating Mode

DIFFERENT STROKES: HOW TO CASCADE AND PARALLEL FIFOs OF VARIOUS ARCHITECTURES *

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1. INTRODUCTION

In the design of digital systems, there's never quite enough memory. It's as if there's a memory corollary of 'Parkinson's Law' [1], stating that 'Information expands to fill the memory available.'

FIFOs ('First-In, First-Out memories'; pronounced 'fye-foes') are one type of VLSI semiconductor memory device. Their storage and readout properties are just what their name, 'FIFO,' implies. That is, the first data word taken in becomes the first data word read out, from the opposite end of the same FIFO. Once input, subsequent data words also emerge with no change in their sequential ordering.

In recent years, FIFOs have become large enough, and cheap enough, to prove their worth in a very wide variety of digital systems.

FIFOs too are notoriously subject to 'Parkinson's Law of Memory.' As system designers discover the operational advantages of increasing the size of their FIFOs, and as new FIFO applications emerge, system needs continually arise for larger FIFOs – typically having two to three times the capacity of any which currently are available.

One practical answer is to use several FIFOs, or even many FIFOs, together in a coordinated manner, in order to provide FIFO capabilities and behavior with expanded memory capacity. This tutorial paper presents some FIFO-memory-capacity expansion methods, and describes the built-in support for these methods which is provided by various industry-standard FIFO architectures.

2. FIFOs AS MEMORY COMPONENTS

In certain ways, FIFOs behave like memory components; in other ways, they behave like logic components. Obviously, FIFO-memory expansion techniques are aimed at increasing memory size. However, the required logic is somewhat subtle and sophisticated, as compared with the expansion logic needed with other types of memory components.

2.1 FIFOs as Compared With RAMs

Within a digital system, FIFOs mostly are used to store data words *temporarily*, while they are 'just passing through' on their way to some other part of the system. Sometimes, they are used to repetitively read out the same data block sequentially, over and over again. Random-access memories (RAMs), on the other hand, almost always are used to store data words which need to be kept available, 'on tap,' for the entire duration of some computational procedure.

The tendency of RAM devices to get larger over time is well known. According to 'Moore's Law,' as stated originally by Gordon Moore of Intel Corporation, the capacity in bits of RAM devices quadruples every two to three years, as semiconductor manufacturers continually develop larger RAM devices to keep up with the memory capacities that digital-system builders and their customers are demanding.

The majority of applications for RAMs use large arrays of them. Usually, systems need much greater RAM storage capacity than is to be found within any single physical semiconductor-RAM device.

FIFOs are more likely than RAMs to be deployed in systems individually, here and there, one by one. But, sometimes, FIFOs too are used in arrays. When there is a need for temporary-storage capacity exceeding that of any available single physical FIFO device, several individual FIFO devices may be teamed up into an expansion array, to comprise a larger 'effective FIFO.'

Some corollary of 'Moore's Law' certainly applies to FIFOs; the capacity of single-package FIFO devices has been doubling approximately every two years. Thus, at any given time, FIFO expansion arrays fill the gap between the largest single-package FIFO devices available, and the still-larger 'effective FIFOs' which system designers feel that they need for their very latest applications.

* This paper was prepared for, and presented at, Northcon/93. It appeared in *The Northcon/93 Conference Record;* Session 9, paper 1.

2.2 FIFO Family Pin-Compatibility

Unlike RAMs, FIFOs have the startling and valuable property that their pinouts do *not* depend in any way on their 'depth,' i.e., on the number of words which they can store. RAMs have to include more memory-address pins as their depth increases; but FIFOs don't *have* any memory-address pins to start with. Thus, very deep FIFOs frequently have been made pin-compatible with shallow ones.

Consequently, FIFO devices usually are marketed as members of 'families' of pin-compatible, architecturally-identical, mutually drop-in-interchangeable parts. Members of a given family differ architecturally only in the depth of their internal FIFO-memory arrays, and in whatever that implies about the behavior of the 'flag' status-output signals – for instance, how many words the FIFO must contain in order to be 'half full.' In most FIFO families, the depth difference from one family member to the next one is by a factor of *two*, rather than by a factor of four as is standard for RAMs.

It is a fairly common design practice to defer a final decision as to the depth of a FIFO, for a given system application, until the system has been built and tested under realistic operating conditions. Then, deeper FIFOs may replace shallower FIFOs, which often speeds up the system. Or, instead, shallower FIFOs may replace deeper FIFOs, to save money. In either case, there aren't any address pins to rewire; and the FIFO depth may be chosen *after* the fact, to optimize cost/performance.

Unless, of course, the system designer needs a FIFO deeper than any which is available! When that's the case, the designer suddenly starts taking an intense interest in FIFO depth-expansion methods.

Obviously, the *deepest* member of a FIFO product family is the one which is going to get used most often in applications involving depth-expansion.

3. USING FIFOs IN ARRAYS

When an array has FIFOs interconnected in a *depth*-expansion pattern, to provide *more* words than are available in any single FIFO device, such interconnection is referred to as 'cascading,' or sometimes more precisely as 'depth cascading.'

In contrast, when the array has FIFOs interconnected in a *wordwidth*-expansion pattern, to provide *wider* words than are available in any single FIFO device, such interconnection is referred to as 'paralleling' — or sometimes as 'width cascading.' For clarity's sake, in this paper 'cascading' always means *depth* cascading; and 'width cascading' always is referred to as '*paralleling*.'

Frequently, practical FIFO expansion arrays feature *both* cascading and paralleling.

3.1 Architectural Support for FIFO Expansion

Four different industry-standard FIFO-architectures to support depth-cascading have been widely implemented. These are:

(1) Handshake

(2) Handclasp

(3-1) One-Wire Token Passing

(3-2) Two-Wire Token Passing

Sharp happens to be the *only* FIFO manufacturer producing at least one FIFO having each of these four industry-standard FIFO cascading architectures. Sharp's FIFO products include various alternate-sourced competitor-defined FIFOs, and also Sharp-defined proprietary FIFOs. Included among the alternate-sourced parts are FIFOs which support three out of the four industry-standard architectures; and there is a Sharp proprietary FIFO which supports the remaining architecture.

This tutorial application note presents each of these four architectures, and shows for each of them how to hook multiple FIFO devices together for increased depth.

Increased wordwidth is a separate topic, and is covered last. In general, unless a system designer is prepared to take the chance that the system will have some inherent, hard-to-find intermittent malfunctions, 'paralleling' FIFOs is *not* just a simple matter of placing them side-by-side and hooking their control inputs up in parallel. Rather, there need to be some 'interlocking' cross-coupling interconnections, so that each paralleled FIFO is compelled always to do — or to not do — the same operation at the same time. By now, some limited architectural support also exists in newer FIFOs for interlocked paralleling.

3.2 Synchronous and Asynchronous FIFOs

In practice, both the 'handshake' architecture (1) and the 'one-wire token-passing' architecture (3-1) have been used most successfully in 'asynchronous' FIFOs. On the other hand, both the 'handclasp' architecture (2) and the 'two-wire token-passing' architecture (3-2) have been used most successfully in 'synchronous' FIFOs. There are some pragmatic reasons for this state of affairs, but nothing rigid or absolute.

Here, a 'synchronous' FIFO is defined as one which <a> uses a free-running 'write-clock' signal, which in principle is generated by an external oscillator, and is gated within the FIFO chip itself by a level-sensitive 'write-enable' signal, to synchronize write operations; and also <b> uses a free-running 'read-clock' signal, which in principle is generated by a second external oscillator, and

is gated within the FIFO chip itself by a level-sensitive 'read-enable' signal, to synchronize read operations.

These two 'enable' signals may in principle be completely independent of one another. Also, between them, they completely control the distribution within the FIFO of the two free-running clock signals. Thus, by using these enable signals to control a synchronous FIFO, a data-transfer procedure at one end of the FIFO can be started, and also can be stopped, quite independently of any data-transfer procedure which may or may not be going on concurrently at the other end of the FIFO.

'Asynchronous' FIFOs don't have any such 'write-enable' or 'read-enable' signals. They can't even make use of free-running 'clock' signals, since a data word would have to be transferred willy-nilly on *every* 'clock' rising edge.

Or, to state the matter another way: At each end of an 'asynchronous' FIFO, the functionality of the level-sensitive 'enable' signal is combined with that of the 'clock' signal, into a single edge-sensitive 'demand' signal.

Usually, asynchronous FIFOs have 'Shift In' and 'Shift Out' control inputs, which function respectively as 'write-demand' and 'read-demand' control signals. Now, these inputs are edge-sensitive, like 'clock' signals; that is, a rising edge or a falling edge of the signal waveform is what causes things to happen, and not a steady-state level. But otherwise these inputs function quite differently from 'clock' signals, in that they cause direct, immediate action in and of themselves whenever they occur.

In general, synchronous FIFOs can operate at much higher data-transfer repetition rates, with many fewer system-timing headaches, than can asynchronous FIFOs which have been produced at the same level of semiconductor process technology. It is increasingly difficult to control the timing and shaping of the 'demand' pulses for asynchronous FIFOs, in order to achieve reliable operation with them, as repetition rates become higher and higher. As a general guideline, asynchronous FIFOs no longer are the best way to go, whenever operating FIFO repetition rates exceed roughly 25 MHz.

3.3 Series and Parallel Data-Bus Connections

Another distinction, among these various cascading architectures, is whether the successive FIFOs in the cascade are deployed in series, or in parallel; see Figure 1.

In the handshake and handclasp architectures, successive FIFOs in the cascade are connected *in series* as in Figure 1a, like a string of sausages. Here, the 'read' (data-output) bus of the i^{th} FIFO is connected to the 'write' (data-input) bus of the $(i+1)^{st}$ FIFO. A data word enters the 'effective FIFO' via the data-input bus of the first FIFO in the cascade, and passes through each of the other FIFOs in the cascade, and exits via the data-output bus of the last FIFO in the cascade.

Obviously, the data word needs to get handled N times, by N different FIFOs. (The case N = 5 is illustrated in Figure 1.) All this handling of data implies greater 'latency' or 'pipeline delay,' and also gives rise to more occasions where possibly *mis*handling may occur. However, there is a compensating advantage: each FIFO output-bus driver element is required to drive just one single load. And the operating speed of a FIFO with lightly-loaded data outputs is relatively predictable.

In the two token-passing architectures, on the other hand, all FIFOs in the cascade are connected *in parallel* as in Figure 1b, somewhat like a bunch of bananas — at least, assuming that all of the banana-blossom ends were somehow to grow together, like the banana stem ends! Anyway, the data-input buses of all of the FIFOs are tied together, and the data-output buses of all of the FIFOs are tied together. A data word passes through only one FIFO in the cascade, no more, on its way through the 'effective FIFO'; and so it gets handled just once.

But now, by duality, there is an offsetting *dis*advantage: the data-input bus and the data-output bus, each of which are *common* to N (here 5) FIFOs, present a greater *capacitive load* to whatever devices are called upon to drive them. In the case of the data-output bus, the FIFO output-bus driver elements themselves must drive some number N-1 of similar data outputs from other FIFO devices, which at the moment are in a high-impedance state, in addition to whatever other system devices have their inputs or their three-state outputs on the FIFO-data-output bus. And since the FIFO data outputs now are more heavily loaded, their operating speed becomes harder to predict.

The characteristics, strengths, and weaknesses of each of these four FIFO cascading architectures are summarized in Tables 1 and 2.

Table 1. Conventional Classification of FIFO Cascading Architectures

TIMING CONTROL PRINCIPLE	DEPTH-CASCADING ARRANGEMENT	
	SERIES	PARALLEL
Asynchronous	Handshake	One-Wire Token Passing
Synchronous	Handclasp	Two-Wire Token Passing

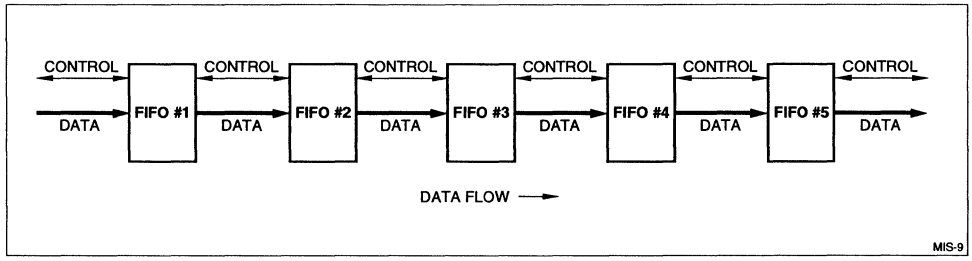


Figure 1a. Series Connection of Depth-Cascaded FIFOs

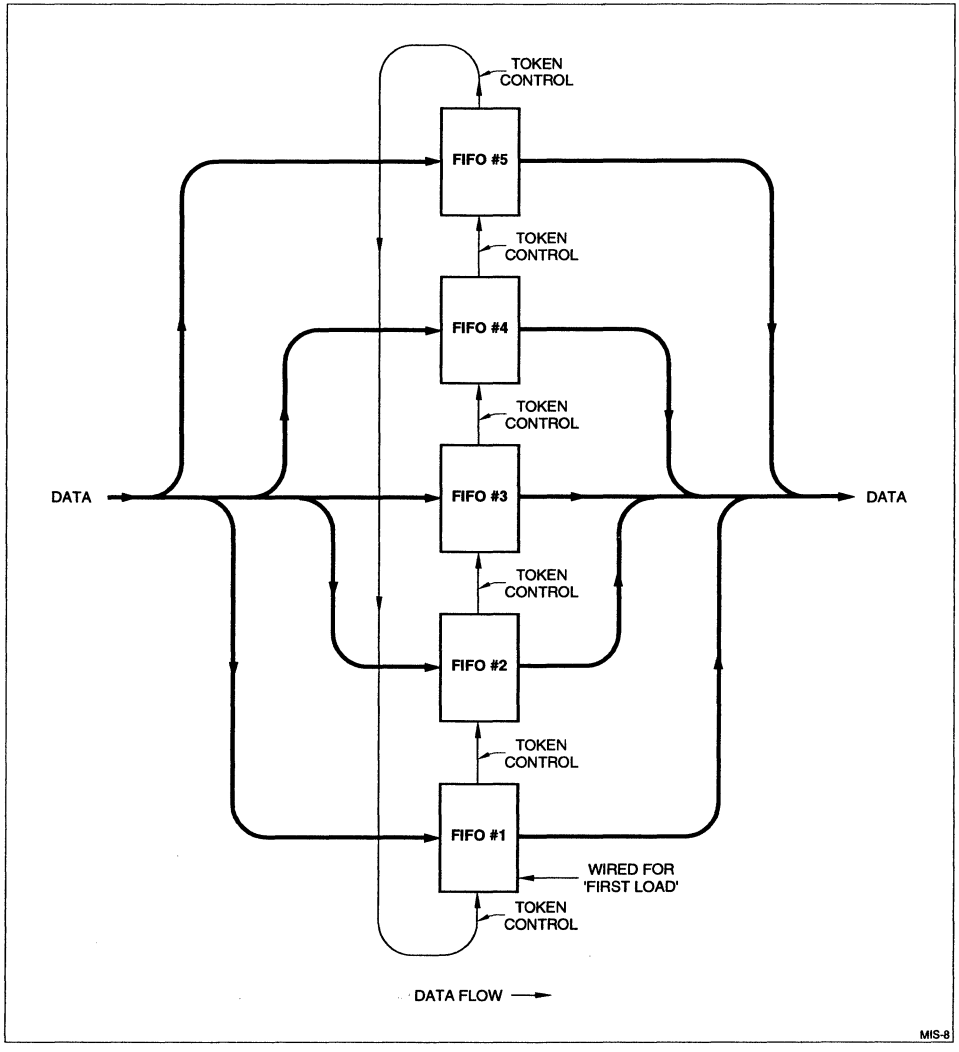


Figure 1b. Parallel Connection of Depth-Cascaded FIFOs

Table 2. Characteristics of FIFO Cascading Architecures

ARCHITECTURAL SCHEME	USUAL TIMING CONTROL PRINCIPLE	NUMBER OF TIMES A DATA WORD GETS HANDLED	NUMBER OF EXTRA LOADS ON A DATA OUTPUT	SUITABILITY FOR HIGH-SPEED OPERATION	SHARP FIFOs WHICH USE THIS SCHEME
Handshake	A	N	0	Very Poor	LH5481/91
Handclasp	S	N	0	Excellent	LH543620
One-Wire Token Passing	A	1	N-1	Poor	LH5496/97/98/99, LH540202/03/04/05
Two-Wire Token Passing	S	1	N-1	Very Good	LH540215/25

KEY:
A = Asynchronous. S = Synchronous. N = Number of FIFOs in the cascade.

4. DESIGN APPROACHES FOR FIFO CASCADING

This discussion of each cascading architecture refers to the Sharp FIFOs having that architecture. However, the same analysis applies, equally well, to other manufacturers' FIFOs having an identical or a similar architecture.

Even among FIFOs having the same basic cascading architecture, there still is some variation in the recommended interconnections. Some FIFOs are designed to 'cascade' without the need for any external 'glue logic' whatever, but some are not. Neither of these alternatives always is necessarily better than the other; there are tradeoffs both ways.

4.1 Cascading Asynchronous-Handshake FIFOs

The 'handshake' architecture for asynchronous FIFOs dates back all the way to 1969, when Fairchild introduced the 800 KHz PMOS 64×4 type 3341 FIFO. Sharp has used this architecture in the 64×8 LH5481 and in the 64×9 LH5491. Other manufacturers still make 3341-pinout 64×4 FIFOs, and also 64×5 FIFOs. Of course, these parts generally use some more-recent-vintage CMOS technology, rather than sticking with PMOS! Anyway, it's mostly the oldest-pinout, smallest-capacity FIFOs which use 'handshake' cascading.

This architecture is the oldest one of the four. It has served semiconductor users well for a quarter of a century. Nevertheless, it is by far the most difficult architecture of the four to understand, and to explain. Also, the explanations of the other three architectures do not depend strongly on this 'handshake-cascading' explanation. Consequently, this section of the paper is not a prerequisite to the other sections which follow; and so it may be skipped over, if desired.

Anyway, in the handshake architecture, each FIFO has two control inputs, Shift In and Shift Out; and two status flags, 'Input Ready' and 'Output Ready.' As previously discussed, these Shift In and Shift Out control inputs are edge-sensitive, rather than level-sensitive.

Input Ready is asserted by a FIFO whenever it is not totally full, so that it can accommodate at least one more input data word. Output Ready is asserted whenever the FIFO is not totally empty, so that it can furnish at least one more output data word.

The Input Ready and Output Ready status flags have the same system meaning respectively as $\overline{FF}$ (assertive-LOW Full Flag) and $\overline{EF}$ (assertive-LOW Empty Flag) in other FIFO architectures. And, even though the nomenclature is opposite, the polarity of the actual signal does not change; the same logic state of the flag (HIGH or LOW) still means exactly the same thing, with respect to the internal status of the FIFO. However, when cascading asynchronous-handshake FIFOs, the Input Ready and Output Ready flags normally function as *pulses*, and not as levels, as is emphasized here in the description of the procedure by which data words get transferred from one FIFO in a cascade to the next one.

Asynchronous-handshake FIFOs are cascaded in series, like sausages, as in Figure 1a. The interconnections from each FIFO, to the next one downstream from it in the cascade, are as shown in Figure 2. Output Ready of the upstream FIFO is connected to Shift In of the downstream FIFO, and Input Ready of the downstream FIFO is connected to Shift Out of the upstream FIFO. As for the data path, the data outputs of the upstream FIFO are connected to the data inputs of the downstream FIFO.

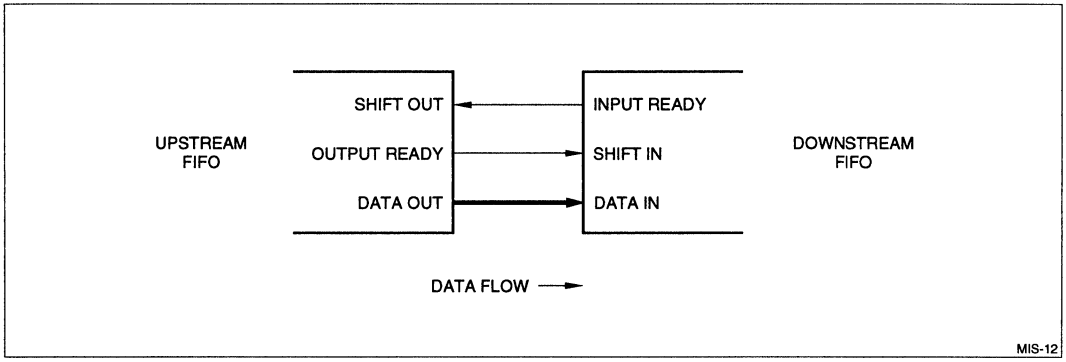


Figure 2. Cascading Interface Between Handshake-Architecture FIFOs

With these interconnections, and assuming that the FIFO cascade has been operating for a while, the procedure for transferring a data word from the upstream FIFO to the downstream FIFO may be described as follows:

(1) The downstream FIFO's Input Ready signal becomes asserted, whenever it ceases to be full. (Or, see Step (6) below.)

(2) Since this Input Ready signal is connected to the Shift Out control input of the upstream FIFO, when it is asserted it becomes a read-demand pulse for the upstream FIFO.

(3) Assuming that the upstream FIFO is not empty, so that its Output Ready signal has been asserted, it then performs a read operation – meaning that its internal read pointer gets advanced by one word position, and a new word becomes available on its data outputs. When those events have occurred, its Output Ready signal becomes deasserted. The upstream FIFO's internal logic actually forms the Output Ready signal as a delayed and inverted *copy* of the Shift Out input control pulse which was received from the downstream FIFO. So, unless the upstream FIFO was entirely emptied out by the read operation which it just performed, it then reasserts its Output Ready signal, after a time lag determined by an internal-gating delay from the deassertion of its Shift Out control input.

(4) Since this Output Ready signal is connected to the Shift In control input of the downstream FIFO, when it is asserted it becomes a write-demand pulse for the downstream FIFO.

(5) Since the downstream FIFO is not full (see Step (1) above), its Input Ready signal has been asserted. So it then performs a write operation – meaning that the new word from the upstream FIFO, which is present at its data inputs, gets written into its internal memory, and its internal write pointer then gets advanced by one word position. When those events have occurred, its Input Ready signal becomes deasserted. The downstream FIFO's internal logic actually forms the Input Ready signal as a delayed and inverted *copy* of the Shift In input control pulse which was received from the upstream FIFO.

(6) If the new word just acquired did not fill up the downstream FIFO, it then reasserts its Input Ready signal, after a time lag which is determined by an internal gating delay from the deassertion of its Shift In control input; and the entire sequence just described starts up all over again. (So, go back to Step (2), and repeat!)

The above word description may seem confusing at first, because of its inherently recursive, round-and-round, never-ending-story flavor! Figure 3 is a waveform description; it shows the pulses for one representative complete word-transfer cycle.

The length of the Shift In and Shift Out pulses must be well-controlled by internal FIFO circuits. A pulse from one FIFO always must be sufficiently long, that it will supply enough energy to cause the appropriate action to take place in another architecturally-similar FIFO – making allowances for lot-to-lot semiconductor-manufacturing variations. Also, particular care should be used, when laying out the circuit-board wiring for these signals, in order to avoid vulnerability to noise problems. Spurious

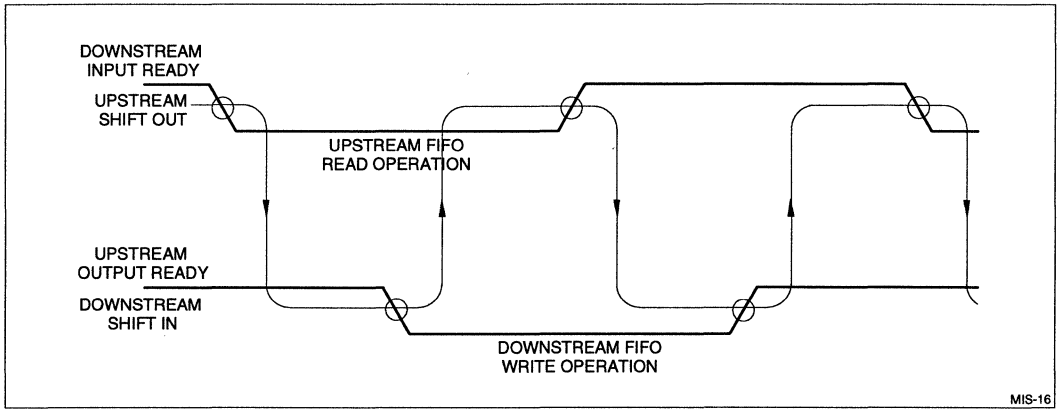


Figure 3. Control-Signal Waveforms for Handshake Cascading

control pulses between cascaded FIFOs may cause erroneous data-transfer-procedure steps to occur.

Nowhere in this entire scene is there any role for a controlled, periodic 'clock' signal. Hence, the timing of the data-transfer operations depends entirely on *gate delays* within the FIFO devices themselves. Thus, in principle, this timing is *process-dependent.*

The data-word-transfer procedure pauses after every word, because of the circuit delays. But it does not halt completely, until either the upstream FIFO has become empty, or else the downstream FIFO has become full. Subsequently, whenever it happens that the upstream FIFO is non-empty while the downstream FIFO is non-full, the procedure automatically restarts itself again.

4.2 Cascading Synchronous-Handclasp FIFOs

Superficially, the arrangement for cascading 'synchronous-handclasp' FIFOs resembles that for 'asynchronous-handshake' FIFOs. Again the FIFOs are in series, like sausages, as in Figure 1a. And again each FIFO has two control inputs, which in principle might be called 'Shift In' and 'Shift Out'; and also two status flags, which in principle might be called 'Input Ready' and 'Output Ready.'

But usually, for these synchronous FIFOs, these control inputs and status flags have different names. In the Sharp LH543620 1024×36 synchronous FIFO, 'Shift In' is called 'Write Enable'; and there actually are two such 'Write Enable' signals, which get ANDed together. Likewise, 'Shift Out' is rechristened 'Read Enable,' and again there are two such ANDed signals. 'Input Ready' and 'Output Ready' are renamed 'Full Flag' and 'Empty Flag' respectively, and now are understood as assertive-LOW signals.

And there is one enormous architectural and behavioral difference, which goes far beyond mere nomenclature or signal assertiveness, and which changes the entire character of the data-transfer procedure for the handclasp cascading architecture. Now, there is an external, free-running '*transfer clock.*' For any given two successive FIFOs in the cascade, this transfer clock is connected both to the 'read-clock' input at the output port of the upstream FIFO, and to the 'write-clock' input at the input port of the downstream FIFO.

So, this transfer clock does *all* of the necessary timing. There is no 'handshaking'; and the repetition rate of the data-transferring procedure *isn't* derived from any process-dependent internal-gating delays within FIFOs.

The transfer clock does *not* have to be the same as the write clock which is visible to the rest of the system, at the input port of the entire FIFO cascade. Nor does it have to be the same as the system-visible read clock, at the output port of the entire FIFO cascade. However, for overall smoothness of operation, it certainly is desirable that the same transfer clock get used at each FIFO-to-FIFO interface, everywhere *within* the cascade; that is, that there only be one transfer clock per 'effective FIFO.'

Apart from the use of the transfer clock, the handclasp interconnections between a FIFO and its downstream successor in the cascade look very similar to those for asynchronous-handshake FIFOs; see Figure 4. The downstream FIFO's Full Flag is connected to both of the upstream FIFO's Read Enable inputs; and the upstream FIFO's Empty Flag is connected to both of the downstream FIFO's Write Enable inputs. It is all right to connect duplicate enables together at the FIFO ports *interior* to the cascade; although the duplicate-enable functionality often is needed at the two extreme ends (input and output)

of the entire FIFO cascade, it isn't needed for FIFO-to-FIFO data transfer *within* the cascade.

Full Flag and Empty Flag are assertive-LOW signals. Thus, when Full Flag is HIGH, the downstream FIFO is not full, and may be written into; and when Empty Flag is HIGH, the upstream FIFO is not empty, and may be read from. So, the system meaning of these signals resembles that of the assertive-HIGH Input Ready and Output Ready signals, except of course that now the signals behave as levels and not as pulses. But the names, and the semantic-psychological assertiveness perceptions of designers, have changed.

And the mechanism for data transfer from an upstream FIFO to a downstream FIFO reduces to the following simple rule: *Whenever the upstream FIFO is not empty, and the downstream FIFO is not full, a data word is transferred from the upstream FIFO to the downstream FIFO after EVERY transfer-clock rising edge.*

Assuming that the transfer clock never is interrupted, this procedure obviously continues until either the upstream FIFO becomes empty, or else the downstream FIFO becomes full. Thus, the stable quiescent condition for the entire FIFO cascade, if neither any write operations nor any read operations are taking place, is that all of the data words 'fall to the bottom' of the cascade, as in a 'hopper.' As a matter of fact, 'hopper' is one synonym for 'FIFO'; in the specialized jargon used by the designers of digital telephone-switching systems, FIFOs traditionally are called 'hoppers.'

4.3 Cascading Token-Passing FIFOs

Token passing as a method of controlling cascaded FIFOs was introduced by Mostek in 1981, in the MK4501 512×9 asynchronous FIFO. Today, FIFOs which conform to the MK4501 asynchronous one-wire token-passing architecture dominate the world FIFO market. By now, architecturally-compatible descendants of the MK4501 are offered in every power-of-two depth from 256×9 to 16384×9.

Sharp has produced the LH5496/97/98/99 family of asynchronous MK5401-architecture FIFOs for several years; these are 512×9, 1024×9, 2048×9, and 4096×9 respectively. Sharp's newer LH540202/03/04/05 family directly replaces the largest three FIFOs in that older Sharp family, and adds an 8192×9 FIFO at the deeper end.

The original MK4501 was very slow; its cycle time was 235 nsec, and its data-access time was 200 nsec. But the speed of more-recent architecturally-similar FIFOs has improved dramatically. For instance, Sharp offers speed grades of the new LH540202 (1024×9) and LH540203 (2048×9) FIFOs with the cycle time at 25 nsec, and the data-access time and the flag-access times all the way down to 15 nsec.

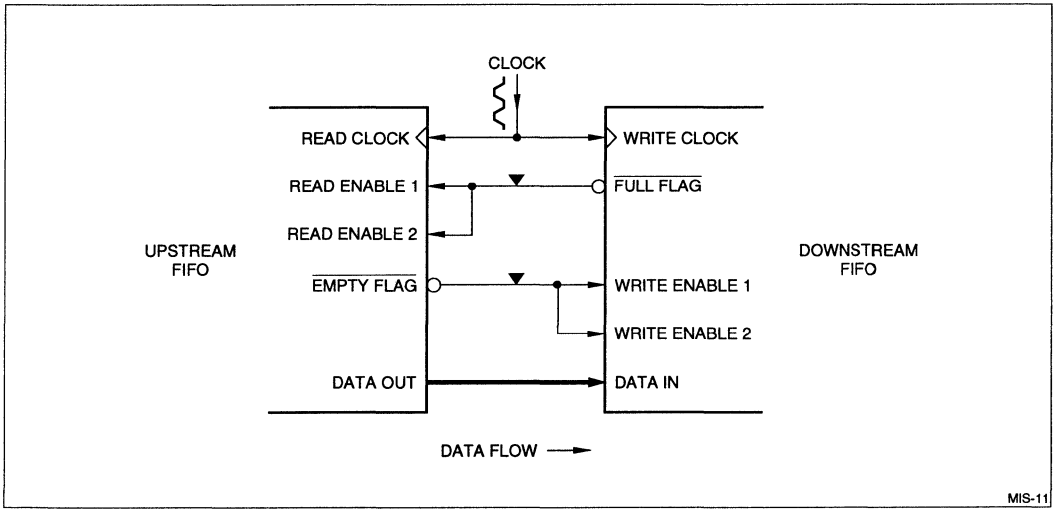


Figure 4. Cascading Interface Between Handclasp-Architecture FIFOs

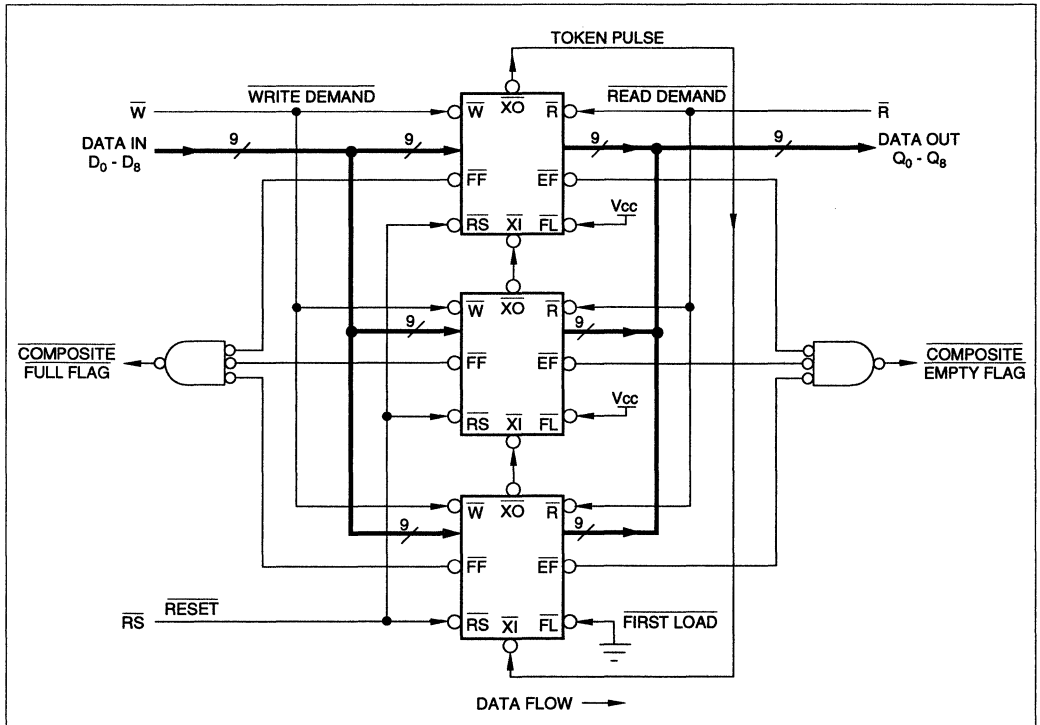
Nevertheless, operation of asynchronous FIFOs in systems at very high speeds, say above 25 MHz to 30 MHz, becomes progressively more difficult. The difficulties have led to a boom in new synchronous architectures for FIFOs. However, some of the earliest synchronous-FIFO architectures did not make any explicit provision for depth cascading.

Subsequently, Integrated Device Technology attempted to use the one-wire-token-passing architecture in a line of fast 18-bit-wide synchronous FIFOs. That attempt did not succeed; predictably, once in a very great while, the 'one wire' becomes a severe bottleneck, for reasons which are discussed below.

And so IDT, Sharp, and other manufacturers switched to the two-wire-token-passing architecture for new synchronous FIFOs. Adding the second wire eliminates a troublesome technical problem, and thereby provides very much better performance at high speeds. Sharp's new LH540215 and LH540225 synchronous FIFOs, 512×18 and 1024×18 respectively, use the two-wire-token-passing architecture.

In either token-passing architecture, FIFOs are cascaded in *parallel*, like bananas, rather than in series like sausages. (Refer to Figures 1a, 1b, 5, and 6.) The input-data buses of all FIFOs in the cascade are tied together, and likewise for their output-data buses and their Read Enable and Write Enable control inputs. One FIFO in the cascade is designated as 'first-load' or 'master,' normally by tying a certain control pin LOW which is tied HIGH for all other FIFOs in the cascade. And the token-passing signaling pins of all FIFOs in the cascade are connected together in a *ring* configuration.

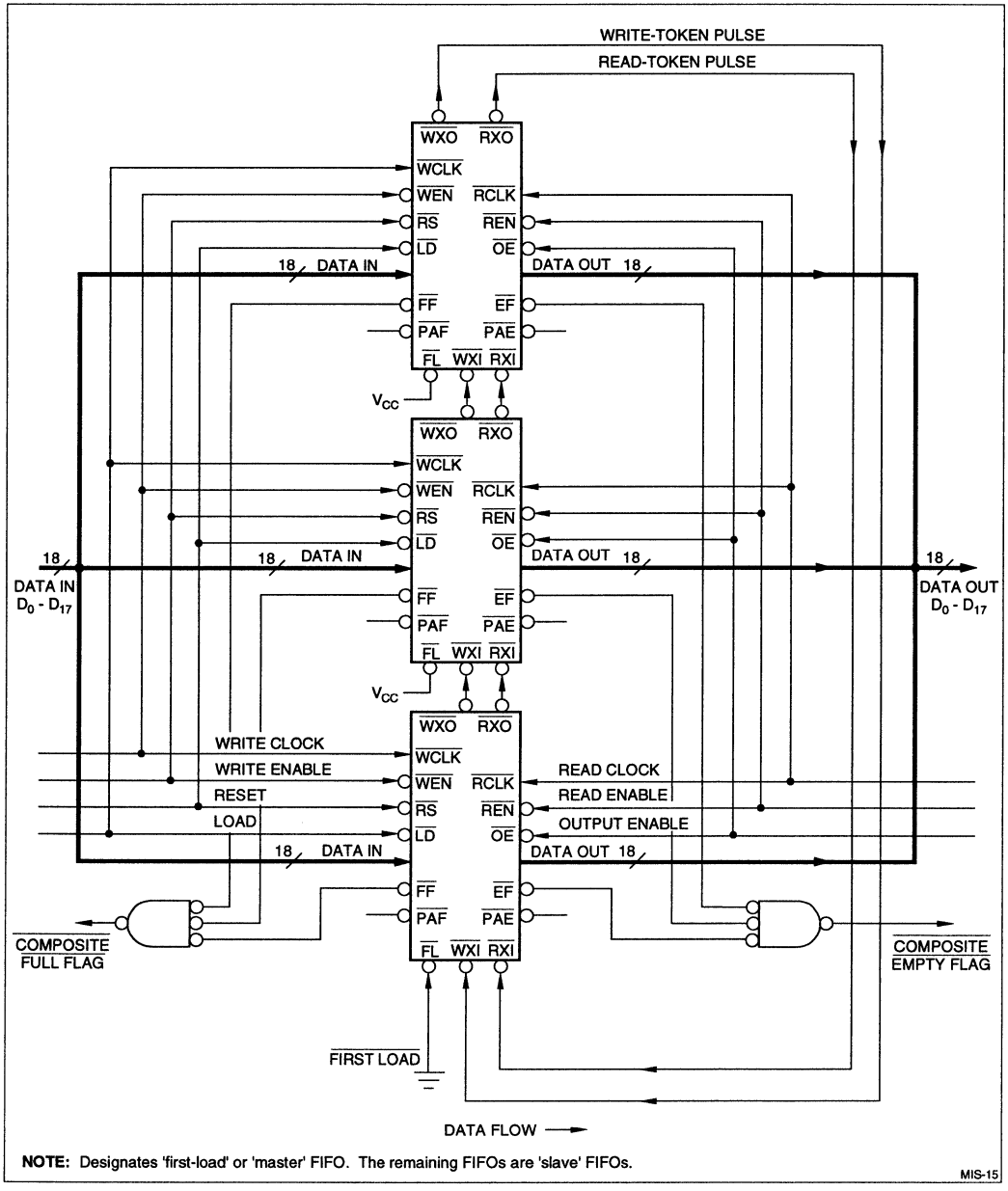
When the array of FIFOs is reset, the internal logic of the master FIFO comes up in a slightly different state than that of the other FIFOs. Actually, there are THREE possible post-reset internal-logic states; besides 'cascaded-master' and 'cascaded-non-master' (or, 'cascaded-slave'), there is a third state which applies to a 'stand-alone' FIFO, that is, to a FIFO which is not part of any cascade.



NOTE: Designates 'first-load' or 'master' FIFO. The remaining FIFOs are 'slave' FIFOs.

MIS-14

Figure 5. Depth Cascading for Three One-Wire-Token-Passing 9-Bit Asynchronous FIFOs



NOTE: Designates 'first-load' or 'master' FIFO. The remaining FIFOs are 'slave' FIFOs.

MIS-15

Figure 6. Depth Cascading for Three Two-Wire-Token-Passing 18-Bit Synchronous FIFOs

For concreteness and descriptive simplicity in what follows, the FIFO depth is assumed to be 1024 words.

According to common sense, the first FIFO operation after a reset operation always should be a write operation; if you haven't written anything into the FIFO yet, there's nothing meaningful in there which you can read back out. Thus, when the first write operation is requested of the FIFO array after a reset operation, the designated master FIFO has the 'write token' within its internal write-pointer-counting and memory-array-addressing logic. There is likewise a 'read token,' which this designated master FIFO also has within its internal read-pointer-counting and memory-array-addressing logic, which comes into play whenever the first read operation is requested of the FIFO array.

After 1024 words have been written into the master FIFO, it passes the write token on to the next FIFO in the cascade. In between FIFOs, this token takes the form of a pulse, LOW-going in all common FIFO architectures, and generally having a duration of approximately half of one clock interval.

The read token also is passed along from one FIFO to the next one by this same procedure. But one more thing must happens also: a FIFO's data outputs must be in a high-impedance state *unless* that FIFO has the read token, *even if* that FIFO's 'Output Enable' ($\overline{OE}$) control input is being asserted. In practice, $\overline{OE}$ is routed in parallel to every FIFO in the cascade, anyway. Thus, the sending FIFO's data outputs go into a high-impedance state as soon as the read token has been passed on; and the receiving FIFO's data outputs, which had been in a high-impedance state, become active as soon as the read token has been received.

In a FIFO with the one-wire-token-passing architecture, the 'one wire' carries both the write token and the read token, at different times. The output pin for the sending FIFO usually is called 'Expansion Out' ($\overline{XO}$); and the input pin for the receiving FIFO usually is called 'Expansion In' ($\overline{XI}$).

In a FIFO with the two-wire-token-passing architecture, there is a 'write-token wire,' and also a 'read-token wire.' The output pins for the sending FIFO are called 'Write Expansion Out' ($\overline{WXO}$) and 'Read Expansion Out' ($\overline{RXO}$); and the input pins for the receiving FIFO are called 'Write Expansion In' ($\overline{WXI}$) and 'Read Expansion In' ($\overline{RXI}$).

Whether an 'effective FIFO' array or an individual FIFO is being considered, the 'empty' condition may be described as the read token catching up with the write token; and the 'full' condition may be described as the write token catching up – *almost* – with the read token.

Almost, but not quite; the read token still must be one position ahead of the write token, unless a one-word 'overrun' (overwriting a data word location not yet read out) has occurred. Now, most FIFO architectures include internal 'interlock' logic to prevent such an overrun. But a few FIFOs, for instance Sharp's LH5492 4096×9 synchronous FIFO, are designed to operate with *external* interlock logic, and do not have internal logic to inhibit either overrun or the opposite condition, 'underrun' (reading out from a data word location not yet written).

Returning to the one-wire-token-passing architecture, how does a FIFO which has just received a pulse on its $\overline{XI}$ input know whether that pulse is to be interpreted as a read token, or as a write token? Simple, as long as all FIFO circuits operate reliably, and there haven't been any spurious noise pulses on the 'one wire'; the first pulse received after a reset operation is considered to be a write token, the second is a read token, the third is again a write token, the fourth is again a read token, and thereafter the interpretation alternates between write- token and read-token. Thus, the interpretation is determined by the equivalent of a *trigger flipflop* within the FIFO's internal control logic.

Now, to see why the one-wire-token-passing architecture becomes inappropriate for high-speed FIFOs, consider what happens when the read token catches up with the write token exactly at the point where an $\overline{XO}$ pulse is ready to go out, on the 'one wire,' from one FIFO to the next FIFO in a cascade.

What now? The write token is all set to move on to the next FIFO, and so is the read token. And, both of these pass through the 'one wire' between the two FIFOs in the form of half-clock-period-duration LOW-going pulses. So, should there be just one regular-length token pulse, or one double-length token pulse, or two token pulses?

The receiving FIFO's $\overline{XI}$ input circuit and read-token/write-token trigger flipflop are *edge-sensitive*. Thus, they need to see *two distinct pulses* – perhaps, even, two pulse falling *edges;* in order to start off *both* that FIFO's internal write pointer and its internal read pointer, there indeed must be two *separate* LOW-going pulses. And, there has to be a long-enough HIGH interval, in between these two LOW-going pulses, that they always get detected reliably as two pulses. Any token-pulse detection mistake by the receiving FIFO would immediately put the entire FIFO array into an erroneous operating state, from which no recovery would be possible without another reset operation. That event, in turn, would render all the data in the entire FIFO array unrecoverable.

Extra time must be allocated by the FIFO's internal logic, therefore, just in case it is necessary on any given cycle to generate and propagate *two distinct* token pulses. Consequently, to avoid losing data when this condition occurs, this occasional extra time must be

allowed for in the design and timing of the entire system, thus reducing system performance.

On an entirely-random basis, it would be a very rare event that the read token would catch up with the write token precisely at the most-inconvenient time. However, if the system has a standard block length which is some power of two, blocks may end precisely on FIFO boundaries fairly often. And, if the system usually writes a block, and then reads it before doing anything else, then a problem may occur fairly frequently.

In any case, simply adding the second token-passing wire, so that the write token and the read token each have their very own wire, completely eliminates this particular bottleneck problem.

Returning to the behavior of the entire FIFO array, the array wiring should connect $\overline{XO}$ (or, $\overline{WXO}$ and $\overline{RXO}$) of the last FIFO back to $\overline{XI}$ (or, $\overline{WXI}$ and $\overline{RXI}$) of the 'master' or 'first-load' FIFO. After both tokens have gotten started off and are circulating through the array, this master FIFO becomes activated for writing or reading by receiving the applicable token, just like any other FIFO in the array. See again Figure 5, for one-wire token passing; also Figure 6, for two-wire token passing.

In some FIFO architectures, the master FIFO takes on an additional responsibility, that of computing 'master' fullness-flag values ($\overline{FF}$ and $\overline{EF}$) for the entire FIFO array. The intent of this feature is to eliminate the need for the usual 'jellybean' logic external to the FIFO array, which otherwise is used to compute 'composite' fullness flags for the entire array. IDT first added this 'master-flag' feature to the initial version of their two-wire-token-passing FIFOs, the 512×18/1024×18 IDT72215A/IDT72225A. In these FIFOs, and in the Paradigm Technology PDM722n5 FIFOs which emulate their architecture, the master FIFO's $\overline{FF}$ and $\overline{EF}$ outputs no longer reflect the fullness situation just within the master FIFO itself, but instead reflect the fullness situation for the *entire* FIFO array.

To implement this usage, the master FIFO must know how many FIFOs there are in the entire FIFO array. And so there is a 'depth code,' which must be loaded into a master-FIFO internal register by the system. Also, the master FIFO must have redundant master counters, to keep track of where the write token and the read token are in the entire FIFO array, with enough bits to provide enough states to encompass representing the complete range of addresses for the entire FIFO array. Since any physical FIFO device must be capable of filling a master-FIFO socket, all the compatible FIFO devices manufactured must include the necessary master-counter logic.

And, during system operation, if the master read counter or write counter ever gets out of synchronization with the local read counter or write counter respectively, within whichever FIFO currently has the applicable token, this discrepancy must get resolved somehow, whenever that token again comes around the loop back into the master FIFO's $\overline{XI}$ (or $\overline{WXI}$ or $\overline{RXI}$) input.

In any case, IDT did not go into full-scale production with their IDT722n5A ×18 FIFOs, but instead has produced the IDT722n5B versions. These IDT722n5B FIFOs no longer incorporate the master-fullness-flag logic; the master FIFO's $\overline{FF}$ and $\overline{EF}$ outputs reflect just the fullness situation within the master FIFO itself. Sharp's LH540215 and LH540225 ×18 FIFOs are pin-compatible replacements for the IDT72215B and IDT72225B ×18 FIFOs respectively. However, Sharp's versions also have some additional flag-synchronization and high-impedance-read-inhibit functionality, which is outside the scope of this paper. [2], [3]

When a token-passing-architecture FIFO is being used 'standalone,' and is not part of any cascade, its $\overline{XO}$ (or $\overline{WXO}$ and $\overline{RXO}$) outputs have no cascading-related function. Thus, in several different FIFO architectures, the $\overline{XO}$ output or the $\overline{WXO}$ output has been used opportunistically, to provide a Half-Full Flag ($\overline{HF}$) status output whenever the FIFO is in 'standalone' mode; the applicable data sheets show a pin designated as '$\overline{XO}/\overline{HF}$,' or as '$\overline{WXO}/\overline{HF}$.' The FIFO's internal logic determines the FIFO's mode, 'cascaded-master' or 'cascaded-slave' or 'standalone, during a reset operation, according to the connection of the $\overline{XI}$ (or $\overline{WXI}$ or $\overline{RXI}$) and 'first-load' control inputs.

Of course, when a FIFO is included within some cascade, its $\overline{HF}$ output is not available. It would not have any useful system meaning, even if it were available.

5. PARALLELING FIFOs

Previous sections have discussed different architectural approaches to *cascading* FIFOs, that is, to *depth* expansion of a FIFO array. This final section analyzes *paralleling* FIFOs, that is, *width* expansion of a FIFO array. Of course, both types of expansion may occur within one FIFO array.

In a perfect world, two FIFOs logically and physically next to each other, each receiving exactly the same waveforms at their corresponding control inputs, always would do exactly the same thing at the same time.

In the real world, the circuit-board wires leading to the control inputs for one of these two FIFOs may be just a little bit longer, than those leading to the other FIFO. Also, the two FIFO devices may have come from different fab lots, and thus may differ in their inherent speed. Both should respond to the same control-input-signal combination in the same way; but one may respond more quickly than the other.

Apparent reliability problems may arise when control-input signals violate setup-time specifications for the two FIFOs; but one FIFO is quick enough to be able to respond, and the other one isn't. At that point, it's possible that the write pointers, and/or the read pointers, in the two side-by-side FIFOs are no longer pointing at the same relative internal FIFO-memory locations. Thereafter, the output data stream will consist of full words which are derived half from one input-data-stream word, and half from the one before it. In this situation, a reset operation is the only way to get the two FIFOs back to tracking each other properly again.

Even though a system designer may have tried very conscientiously to observe FIFO timing specifications, there are subtle ways in which timing violations may occur. Now, as a general rule, the two opposite ends of the two side-by-side FIFOs may be responding to clock signals, or demand signals, which are not synchronized with each other in any way.

So, say that both FIFOs become completely full, and that a read operation comes along at some time which isn't serendipitous with respect to the write-port timing, and creates a vacancy so that one more word now may be written. If both FIFOs contain internal interlock logic to prevent them from trying to write a word when they are full, but this internal logic *releases* the internal write-lock-out signal much more rapidly for one of the two FIFOs than for the other one when the vacancy is created, then one FIFO may allow the next write operation – and the other one may not! Or, if there also is *external* interlock logic in the surrounding system, one FIFO's Full Flag may respond more quickly than the other one's, causing a similar effect.

This particular type of problem, of paralleled FIFOs 'getting out of step' with each other, may arise either with asynchronous FIFOs or with synchronous FIFOs.

Also, by duality, there is a similar sequence of events which may occur at the other ports of the two FIFOs, as a consequence of their having become completely empty; when another word gets written in at a non-serendipitous time, one FIFO may become again ready to output data before the other one does.

A robust solution to this 'getting-out-of-step' design problem is the 'interlocked-crosscoupling' paralleling-interconnection scheme shown in Figure 7. The Full Flag output of each FIFO is connected to one of the Write Enable control inputs of the other FIFO. And, likewise, the

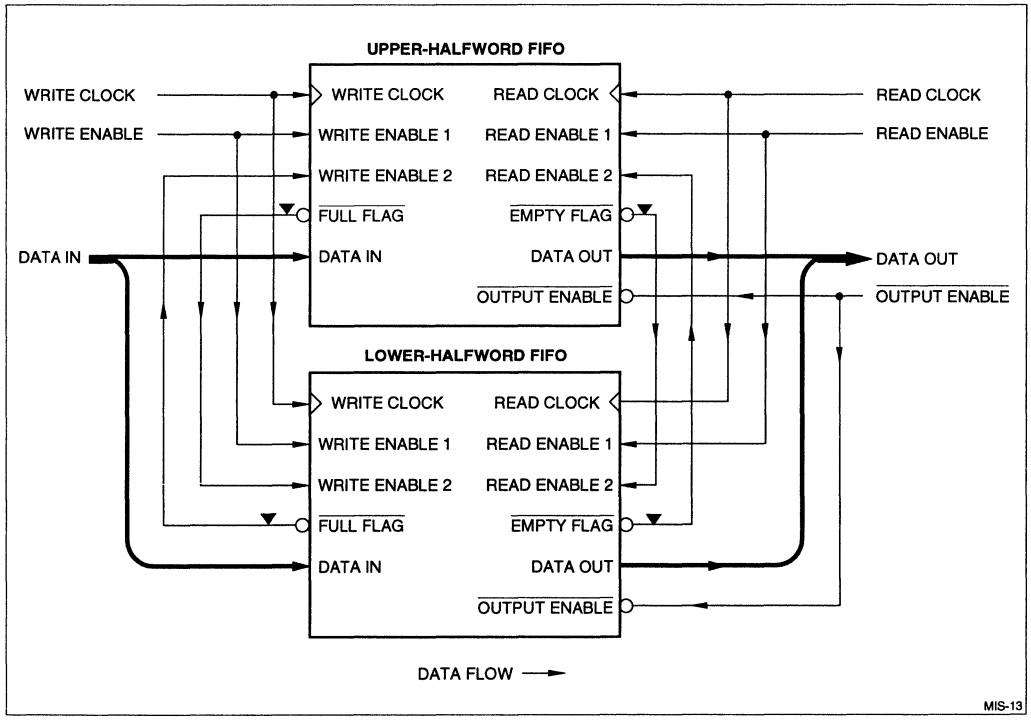


Figure 7. Crosscoupled Interlocking of Paralleled Synchronous FIFOs

Empty Flag output of each FIFO is connected to one of the Read Enable control inputs of the other FIFO.

Notice that, even though the Write Enable and Read Enable control inputs are assertive-HIGH, and the Full Flag and Empty Flag status outputs are assertive-LOW, the polarity of the actual signals still works out OK. When the Full Flag $\overline{FF}$ is deasserted, meaning that the FIFO isn't full and can accept more data words, $\overline{FF}$ is HIGH – and, if it is connected to Write Enable, writing is thereby enabled! Ditto for the Empty Flag $\overline{EF}$, when it is connected to Read Enable.

The small triangular symbol denotes a change in perceived signal assertiveness, from a driving output to driven input(s).

Now, assuming that the two FIFOs both have internal interlocking to prevent overrun and underrun, *neither* FIFO can respond to a write request or a read request, unless *both* it *and* the other one truly are ready to respond. Thus, borderline cases, where one FIFO gets out of step with the other one, get suppressed.

Many FIFOs, including Sharp's LH5492 4096×9 and LH543620 1024×36 synchronous FIFOs, feature duplicate Write Enable signals, and also duplicate Read Enable signals, specifically to support interlocked crosscoupling. Even if one enable signal of each type is used in this manner, the other one of the same type still remains available for control of the FIFO array by the system.

External logic generally is required, in order to crosscouple more than two paralleled FIFOs in this manner, since present-day FIFO pinouts don't provide more than two enables of each type. This logic computes a 'Composite Full Flag' and a 'Composite Empty Flag,' which are logic-AND functions (with appropriate use of de Morgan's Theorem) of the corresponding flags of the individual FIFO devices. These composite flags are routed respectively back to one Write Enable control input, and one Read Enable control input, of each of the individual FIFOs.

6. SUMMARY

FIFOs are *memory* components internally. But they interact with the system of which they are part, and with each other, like *logic* devices.

FIFOs often are used in arrays, to expand the memory available within the 'effective FIFO' which is required by the system. The expansion may be either in *depth* (the number of memory words), or in *width* (the number of bits within one memory word), or in both depth and width at once.

Recent FIFOs include architectural features to make depth-expansion *(cascading)* and width-expansion *(paralleling)* both more designer-friendly and more reliable. Four different cascading architectures are in widespread use today. Architectural support for paralleling comes down simply to providing extra 'enable' control inputs.

7. REFERENCES

[1] C. Northcote Parkinson, *Parkinson's Law and Other Studies in Administration*, Houghton Mifflin Company, Boston, MA, 1957; also Ballantine Books, New York, NY, 1964.

[2] Chuck Hastings, *FIFO Flag Timing: Marching to Two Different Drummers*, Northcon/93 Conference Record; Session 12, Paper 3. Also, Wescon/93 Conference Record; Session 26, Paper 3. Available from The Institute of Electrical and Electronics Engineers, Inc., 445 Hoes Lane, P. O. Box 1331, Piscataway, NJ 08855-1331. Also reprinted in the *1993 Sharp Memory Data Book*, pages 6-5 to 6-12. Refer in particular to Table 1.

[3] Preliminary Datasheet, Sharp LH540215/25 512×18/1024×18 Synchronous FIFO, *1993 Sharp Memory Data Book*, pages 5-226 to 5-262. Refer in particular to Table 5 and to Figure 4.

PACKAGING

PACKAGE SELECTIONS: STATIC RAMs

PRODUCT	PIN COUNT (NOMINAL DIMENSIONS)																				
	DIP							SDIP		SOJ				SOP			TSOP			PLCC
	18 (300)	22 (300)	24 (300)	24 (600)	28 (300)	28 (600)	32 (600)	24 (300)	28 (300)	24 (300)	28 (300)	28 (400)	32 (400)	24 (450)	28 (450)	32 (525)	28[1] (0813)	32[2] (400)	32[1] (820)	52 (750)
PSEUDO-STATIC RAMs																				
LH5P832						X			X						X					
LH5P864																X				
LH5P8128							X									X			X	
LH5P8129							X									X			X	
STATIC RAMs																				
LH5101		X																		
LH5114	X																			
LH5116/H				X				X						X						
LH5116S														X						
LH5118/H				X				X						X						
LH5168/H						X			X						X		X			
LH5168SH															X					
LH5168ST																	X			
LH5168Z8															X					
LH5168Z9															X					
LH5268A						X			X						X					
LH51256L						X									X					
LH52B256					X	X									X					
LH52252A			X							X										
LH52253					X						X									
LH52258A					X						X									
LH521002												X								
LH521007A													X							
LH521008													X							
LH521028																				X

1. TSOP(I)
2. TSOP(II) – Consult factory for availability.

PACKAGE SELECTIONS: MASK-PROGRAMMABLE ROMs

PRODUCT	PIN COUNT (NOMINAL DIMENSIONS)												
	DIP				SOP				QFP			TSOP	
	28 (600)	32 (600)	40 (600)	42 (600)	28 (450)	32 (525)	40 (525)	44 (600)	44 (1010)	44 (1414)	64 (1420)	32[1] (0820)	48[2] (1218)
MASK-PROGRAMMABLE ROMs													
LH53259	X				X				X				
LH53515	X				X	X			X				
LH53H0900		X				X							
LH530800A		X				X			X				
LH530800A-Y		X				X			X				
LH531000B	X				X					X			
LH532000B			X				X		X	X			X
LH532000B-S			X				X		X	X			X
LH532100B		X				X						X	
LH53H4100		X				X						X	
LH53H4000			X				X						X
LH534K00		X				X						X	
LH534P00			X				X			X			X
LH534R00		X				X						X	
LH534000B			X				X		X	X			X
LH534000B-S			X				X		X	X			X
LH534100B		X				X							
LH534500A			X				X			X			X
LH534600A			X				X			X			
LH538P00A				X				X					X
LH538R00A		X				X						X	
LH538000-S				X				X			X		X
LH538300B		X				X						X	
LH538500B				X				X		X	X		X
LH538600				X				X		X	X		X
LH5316500C				X				X					X
LH5316501				X				X					
LH5332500								X			X		

1. TSOP (Type II)
2. TSOP (Type I)

PACKAGE SELECTIONS: FIFO MEMORIES

PRODUCT	PIN COUNT (NOMINAL DIMENSIONS)							
	DIP		SOJ	PLCC			PQFP	PGA
	28 (300)	28 (600)	28 (300)	28 (450)	32[1] (450)	68 (950)	132 (950)	120 (1360)
FIFO MEMORIES								
LH5481/91	X			X				
LH5492					X			
LH5496/96H	X	X			X			
LH5497/97H	X	X			X			
LH5498	X	X			X			
LH5499		X			X			
LH5420							X	X
LH540202	X	X	X		X			
LH540203	X	X	X		X			
LH540204	X	X	X		X			
LH540205	X	X						
LH540215/25						X		
LH543601/11							X	X
LH543620							X	

1. Rectangular Body (450 × 550)

PACKAGING NOMENCLATURE

DIP – Dual-In-line-Package

- SKDIP – Skinny DIP (0.300 inch package width)
- SDIP – Shrink DIP (0.070 inch lead pitch)
- CERDIP – Ceramic DIP

SOP – Small Outline Package

- TSOP – Thin SOP

SOJ – Small Outline J-Leaded Package

ZIP – Zigzag In-line Package

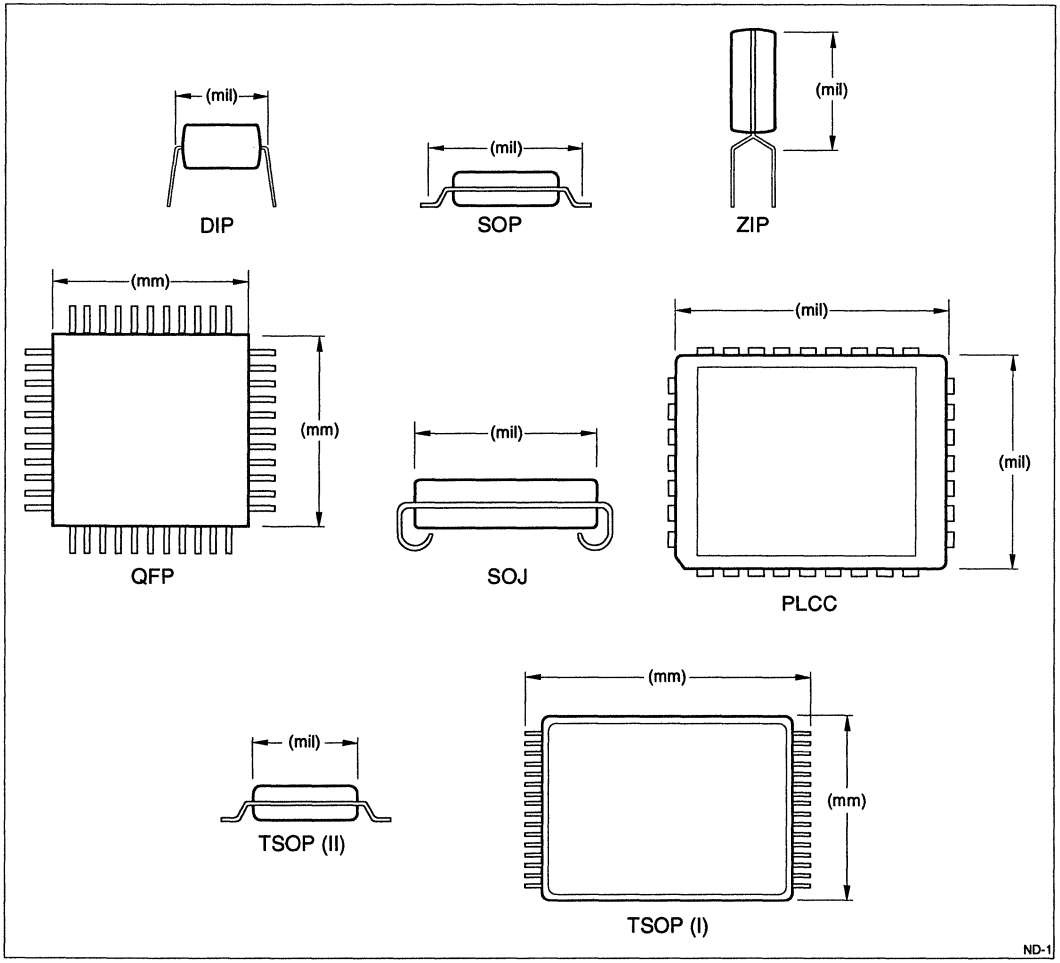
QFP – Quad Flat Package (Metric Standard)

- PQFP – Plastic QFP (JEDEC Bumpered Standard)

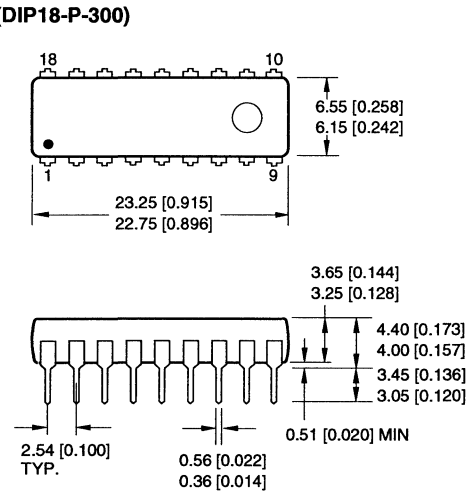
PLCC – Plastic Leaded Chip Carrier

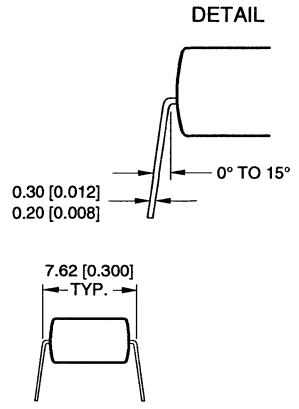
PGA – Pin Grid Array

NOMINAL DIMENSIONS



18DIP (DIP18-P-300)

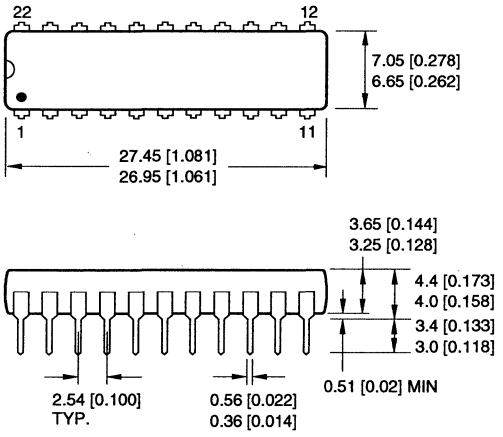


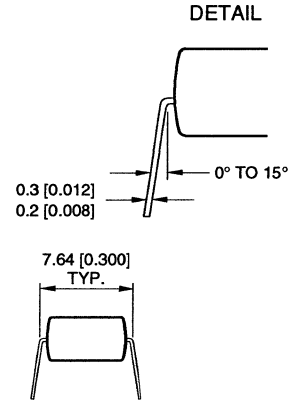


DIMENSIONS IN MM [INCHES] MAXIMUM LIMIT / MINIMUM LIMIT

18DIP

22DIP (DIP22-P-300)

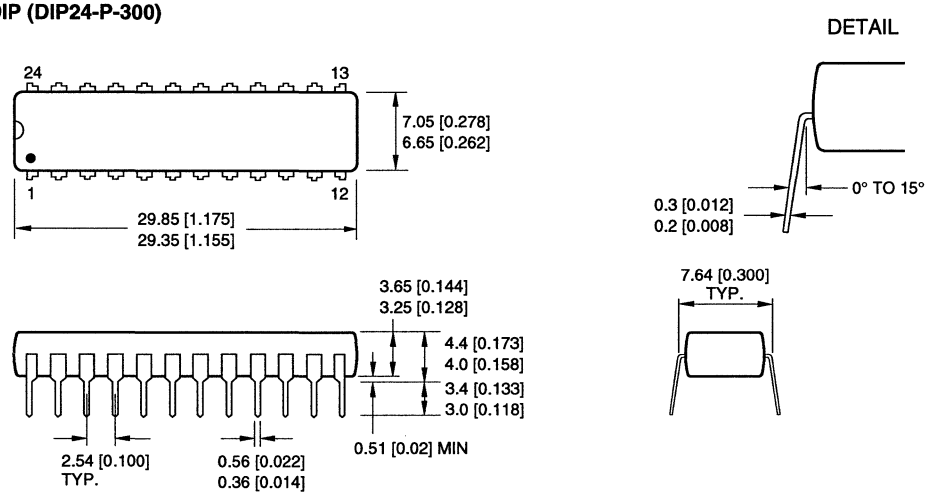




DIMENSIONS IN MM [INCHES] MAXIMUM LIMIT / MINIMUM LIMIT

22DIP-3

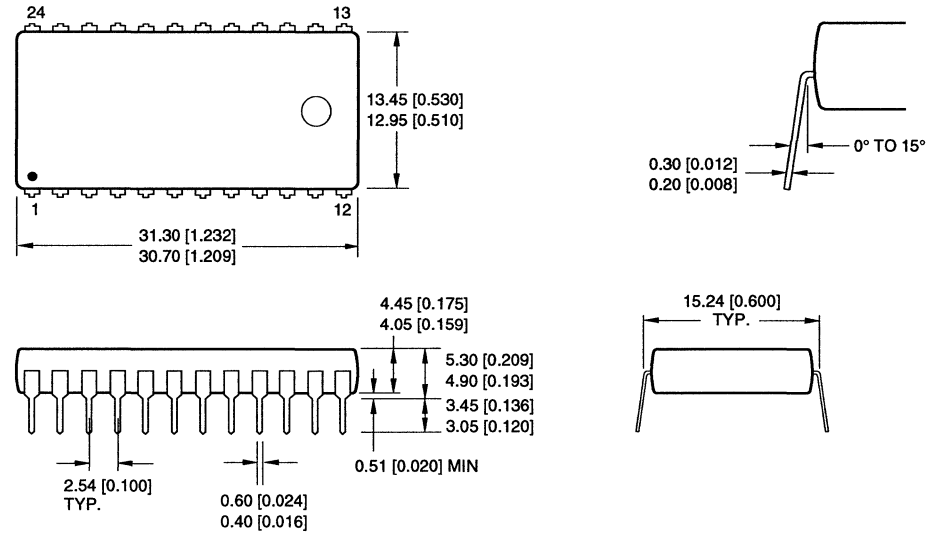
24DIP (DIP24-P-300)



DIMENSIONS IN MM [INCHES] MAXIMUM LIMIT / MINIMUM LIMIT

24DIP-1

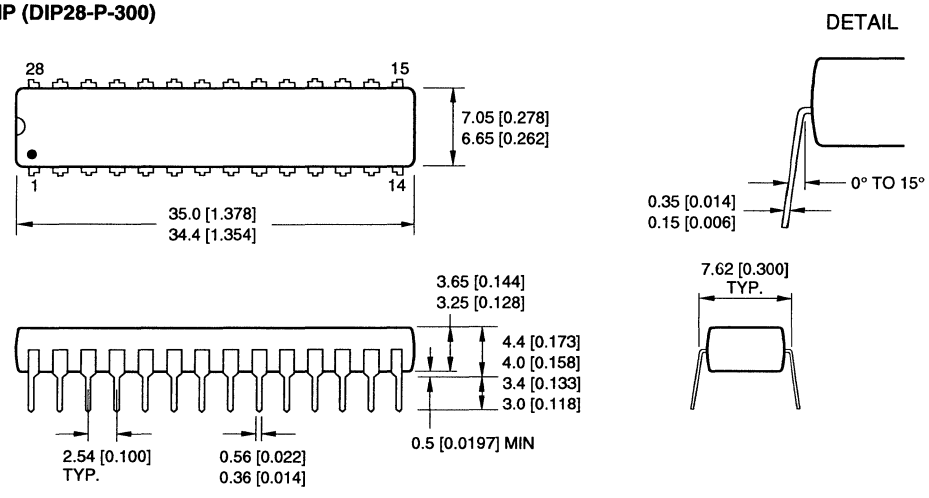
24DIP (DIP24-P-600)



DIMENSIONS IN MM [INCHES] MAXIMUM LIMIT / MINIMUM LIMIT

24DIP-2

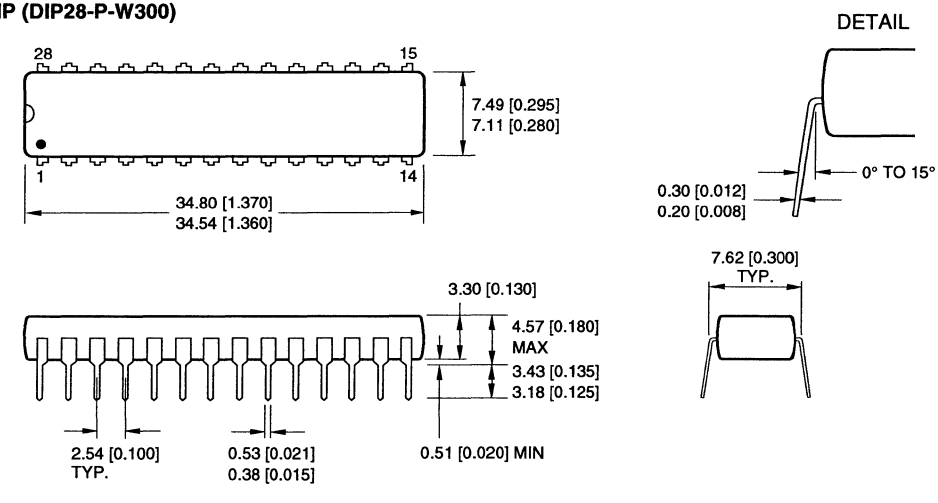
28DIP (DIP28-P-300)



DIMENSIONS IN MM [INCHES] MAXIMUM LIMIT / MINIMUM LIMIT

28DIP-1

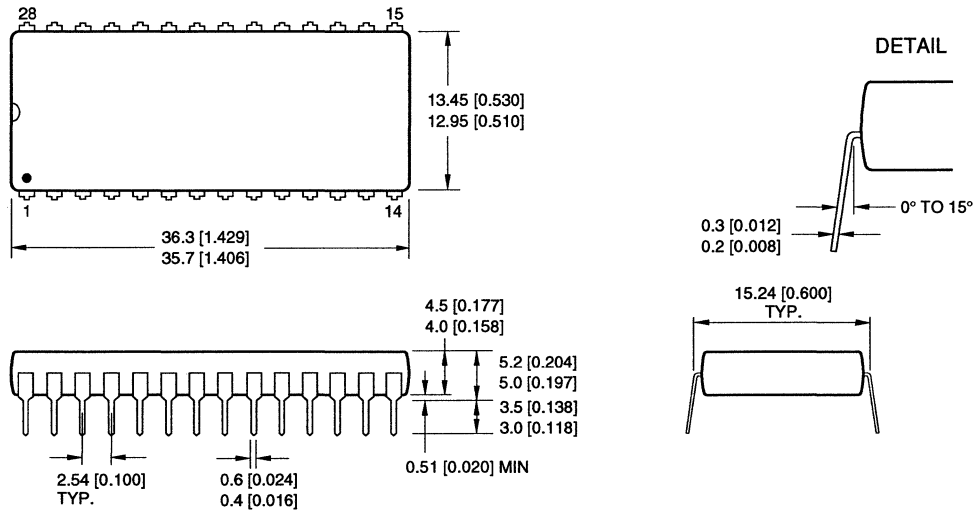
28DIP (DIP28-P-W300)



DIMENSIONS IN MM [INCHES] MAXIMUM LIMIT / MINIMUM LIMIT

28DIP-5

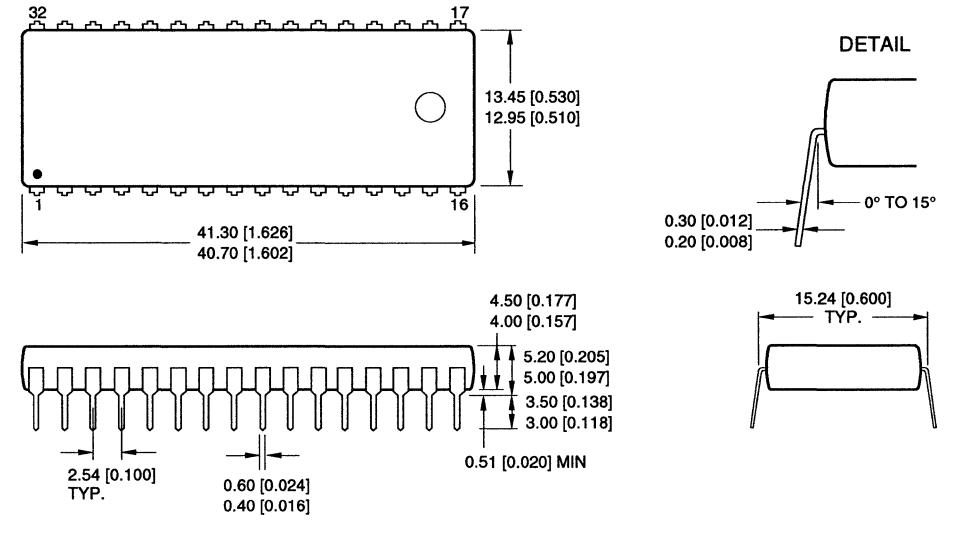
28DIP (DIP28-P-600)



DIMENSIONS IN MM [INCHES] MAXIMUM LIMIT / MINIMUM LIMIT

28DIP-2

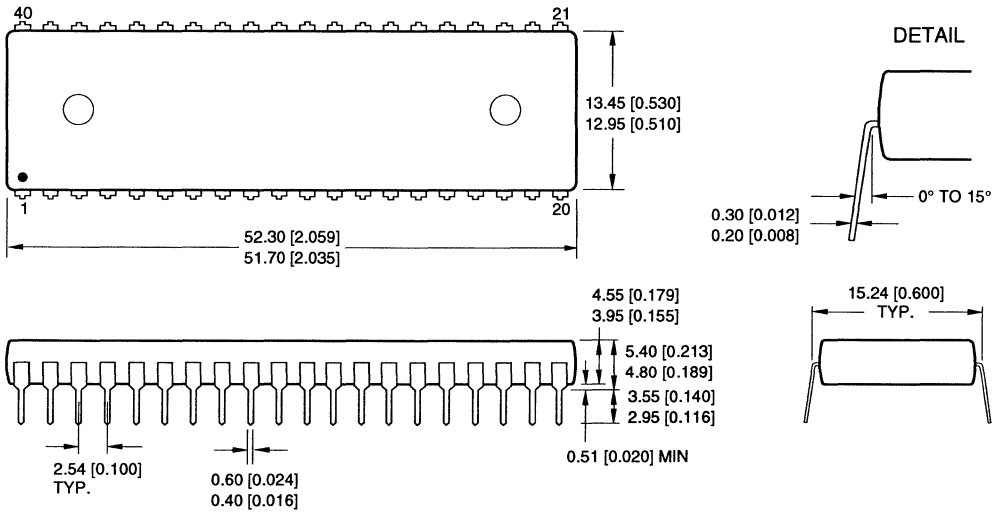
32DIP (DIP32-P-600)



DIMENSIONS IN MM [INCHES] MAXIMUM LIMIT / MINIMUM LIMIT

32DIP

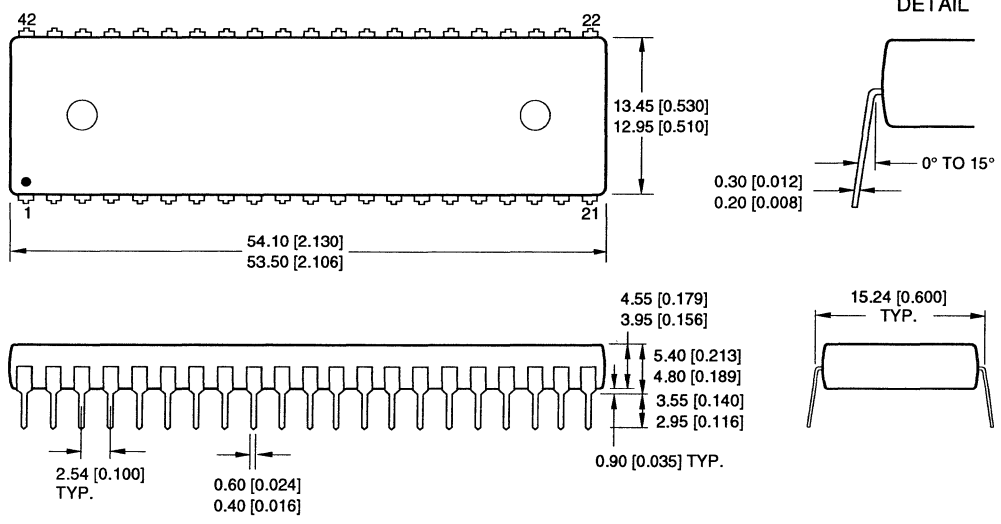
40DIP (DIP40-P-600)



DIMENSIONS IN MM [INCHES] MAXIMUM LIMIT / MINIMUM LIMIT

40DIP

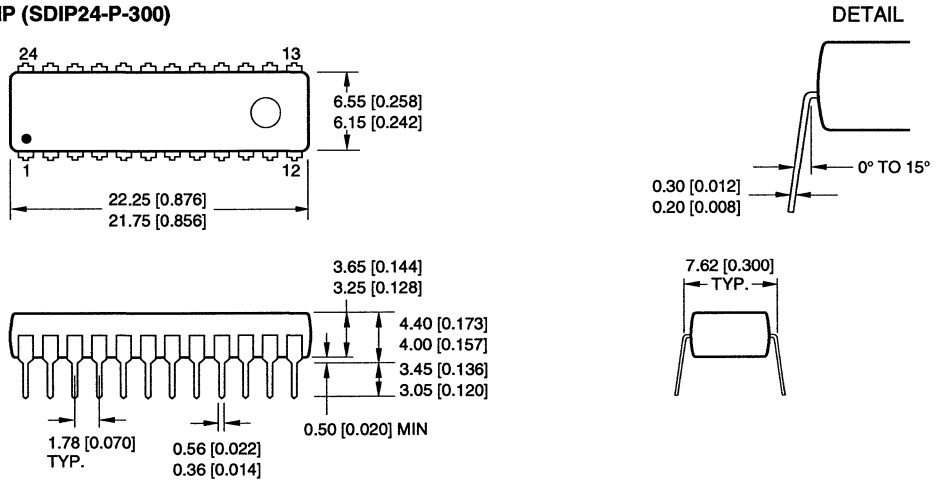
42DIP (DIP42-P-600)



DIMENSIONS IN MM [INCHES] MAXIMUM LIMIT / MINIMUM LIMIT

42DIP

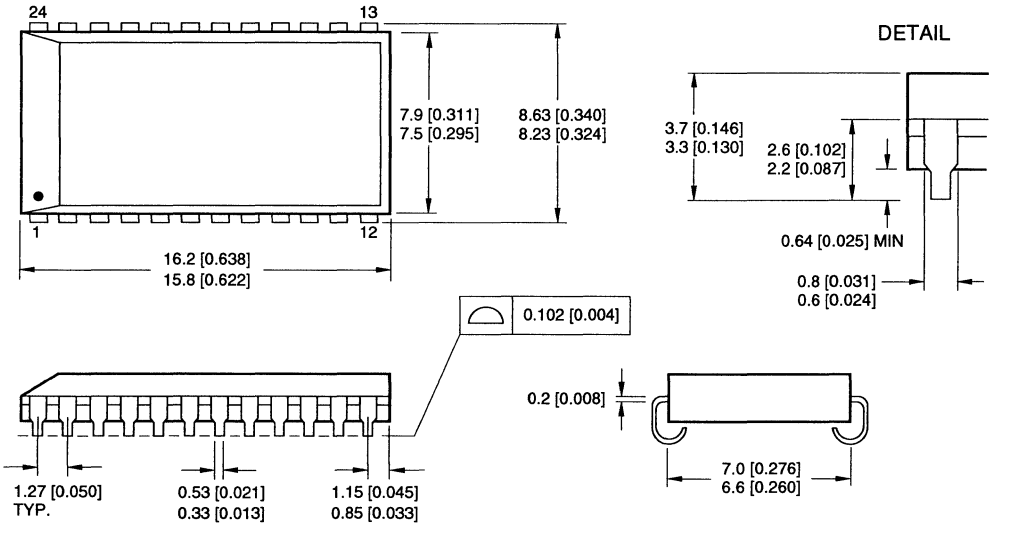
24SDIP (SDIP24-P-300)



DIMENSIONS IN MM [INCHES] MAXIMUM LIMIT / MINIMUM LIMIT

24SDIP

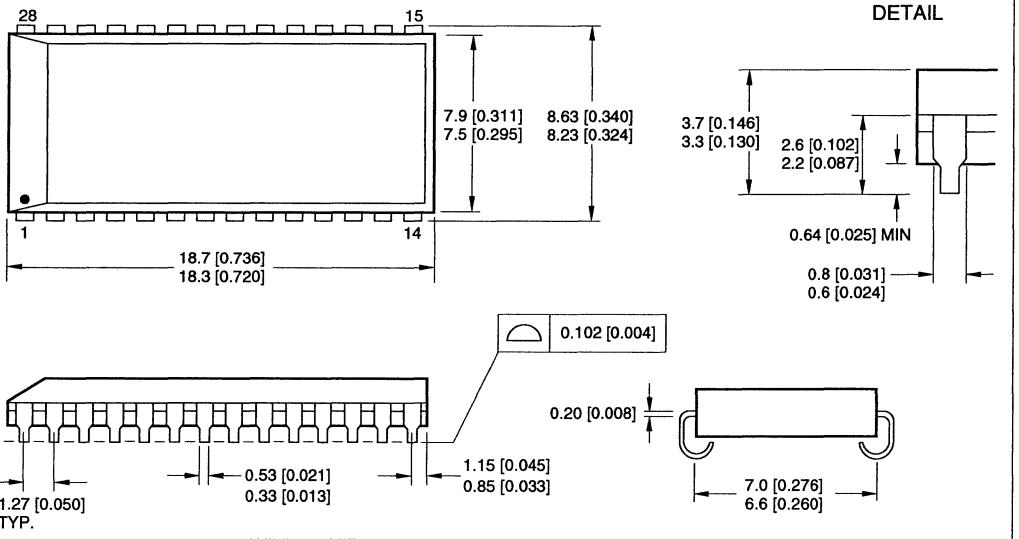
24SOJ (SOJ24-P-300)



DIMENSIONS IN MM [INCHES] MAXIMUM LIMIT / MINIMUM LIMIT

24SOJ

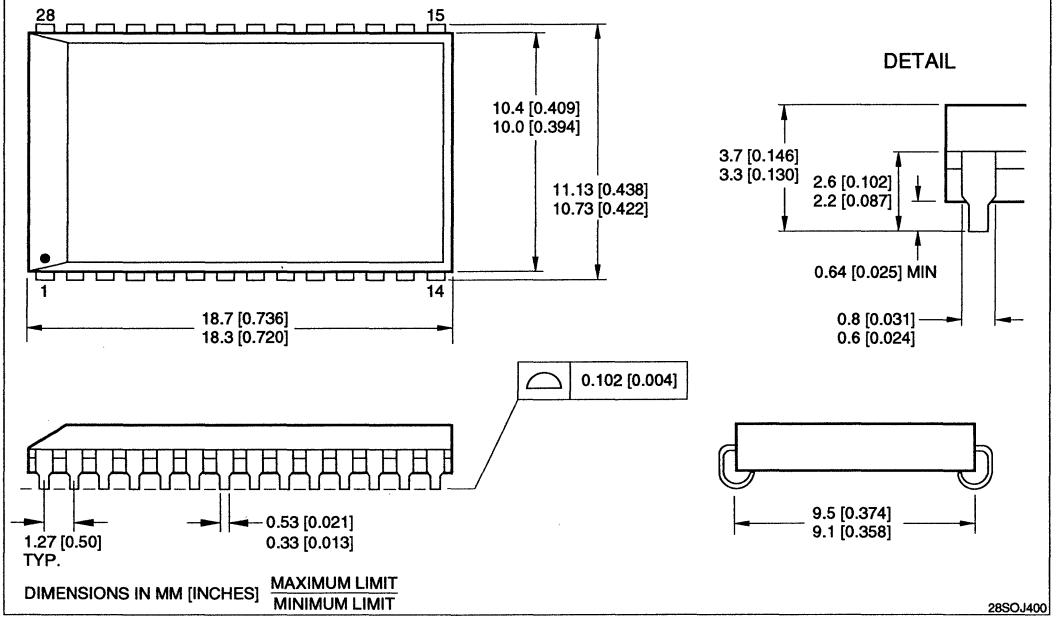
28SOJ (SOJ28-P-300)



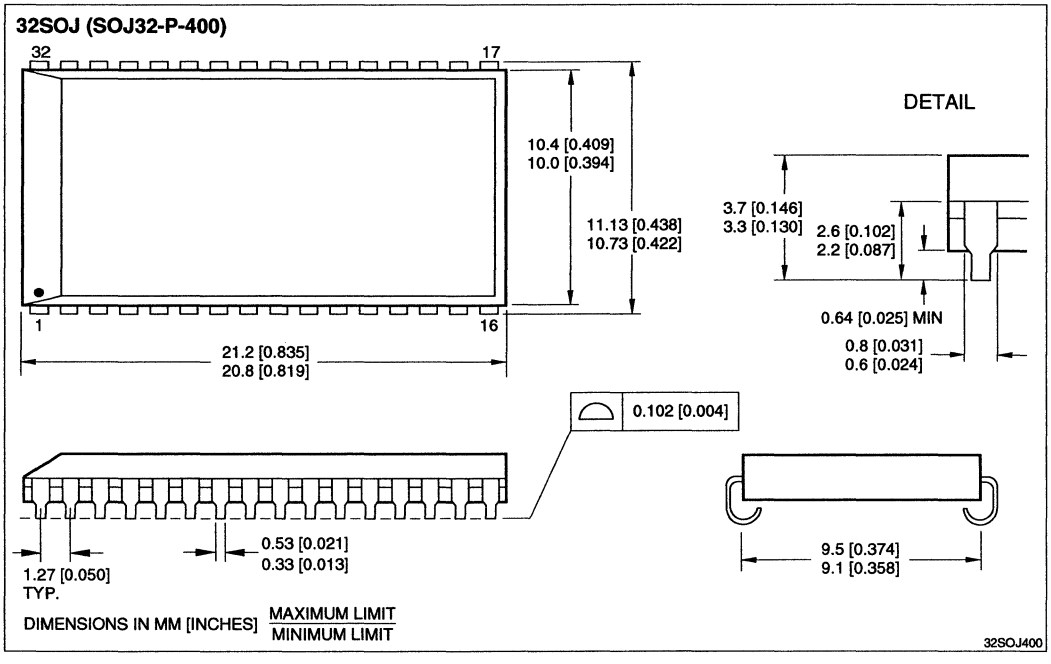
DIMENSIONS IN MM [INCHES] MAXIMUM LIMIT / MINIMUM LIMIT

28SOJ300

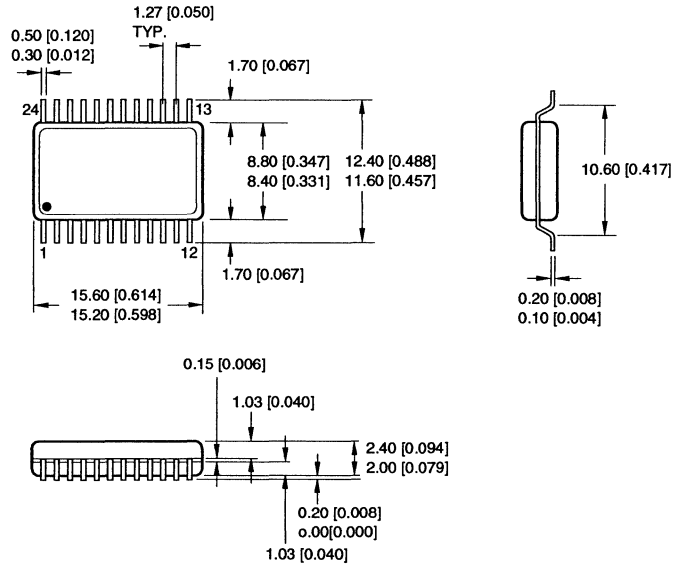
28SOJ (SOJ28-P-400)



32SOJ (SOJ32-P-400)



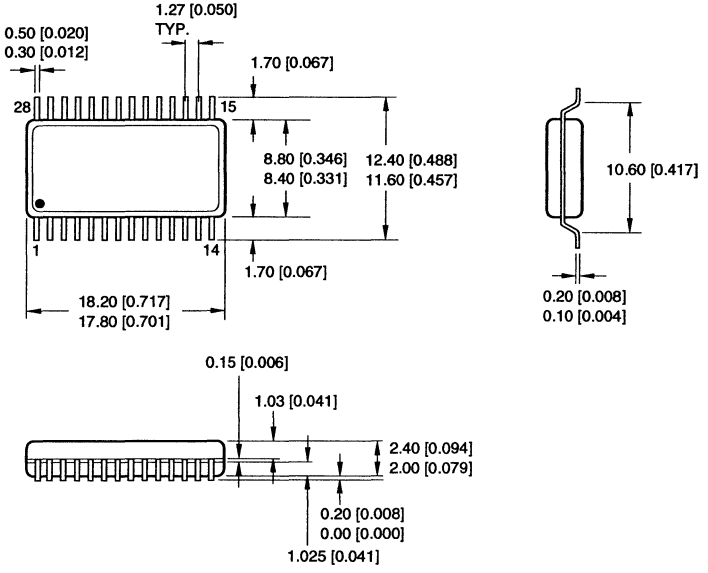
24SOP (SOP24-P-450)



DIMENSIONS IN MM [INCHES] MAXIMUM LIMIT / MINIMUM LIMIT

24SOP

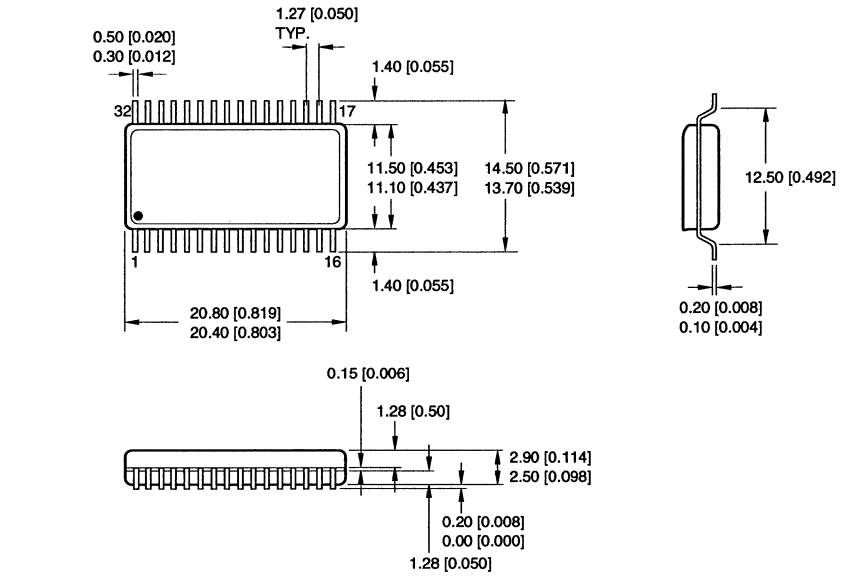
28SOP (SOP28-P-450)



DIMENSIONS IN MM [INCHES] MAXIMUM LIMIT / MINIMUM LIMIT

28SOP

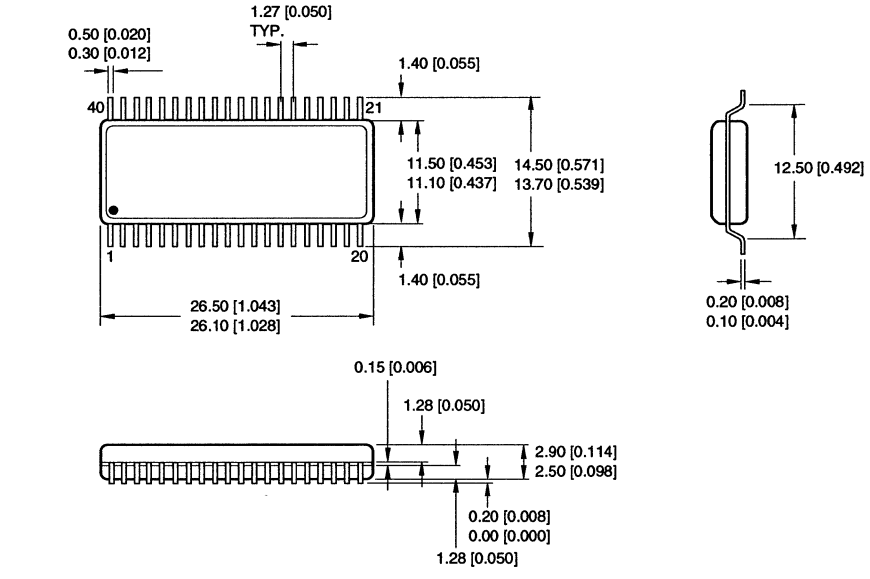
32SOP (SOP32-P-525)



DIMENSIONS IN MM [INCHES] MAXIMUM LIMIT / MINIMUM LIMIT

32SOP

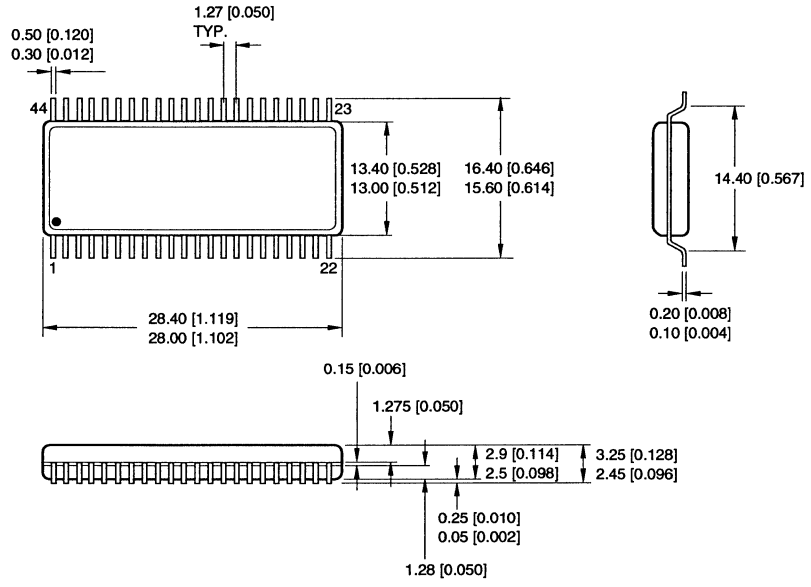
40SOP (SOP40-P-525)



DIMENSIONS IN MM [INCHES] MAXIMUM LIMIT / MINIMUM LIMIT

40SOP

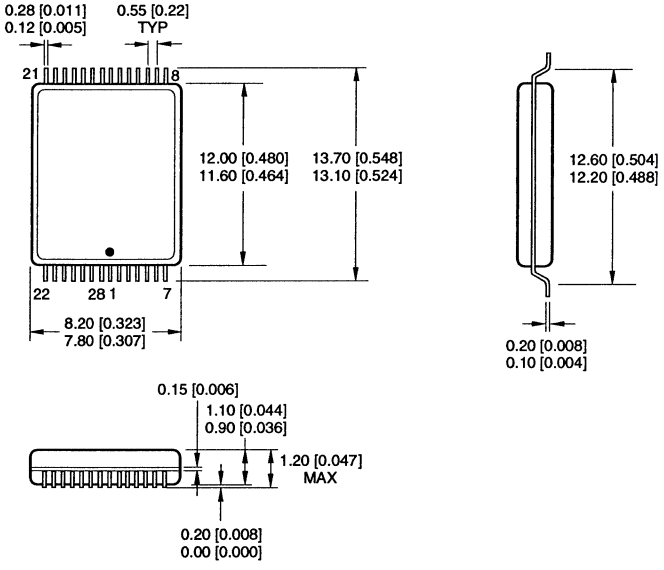
44SOP (SOP44-P-600)



DIMENSIONS IN MM [INCHES] MAXIMUM LIMIT / MINIMUM LIMIT

44SOP

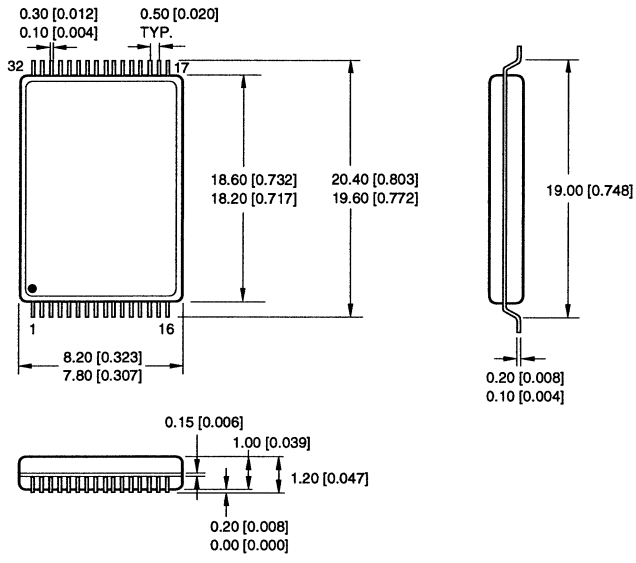
28TSOP (TSOP28-P-0813)



DIMENSIONS IN MM [INCHES] MAXIMUM LIMIT / MINIMUM LIMIT

28TSOP

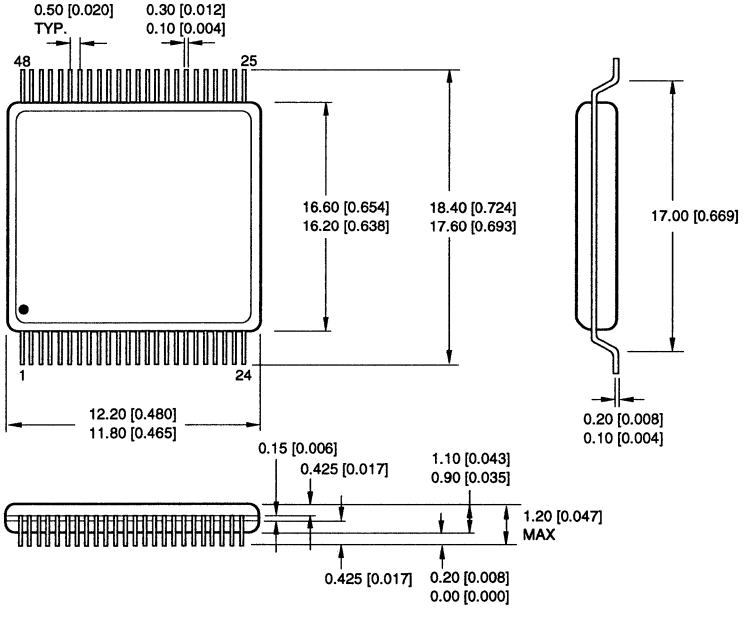
32TSOP (TSOP32-P-0820)



DIMENSIONS IN MM [INCHES] MAXIMUM LIMIT / MINIMUM LIMIT

32TSOP

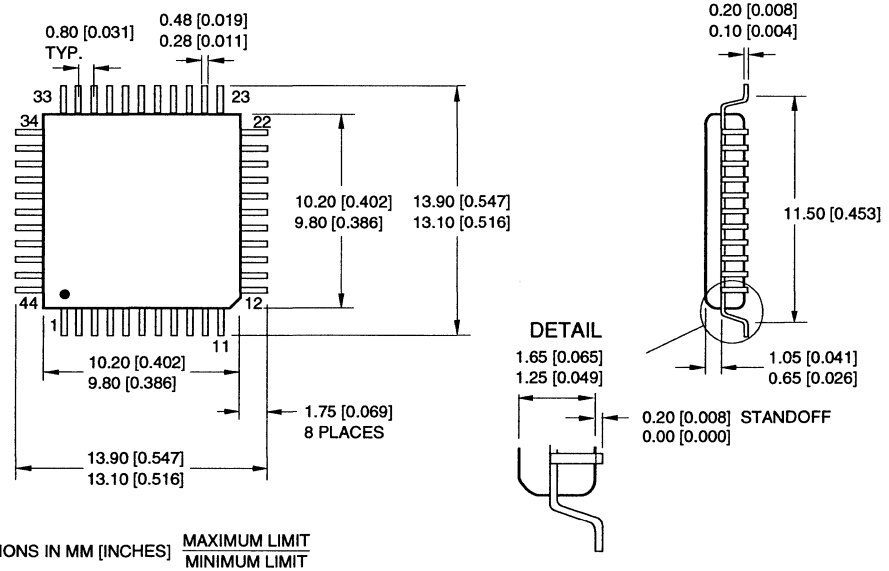
48TSOP (TSOP48-P-1218)



DIMENSIONS IN MM [INCHES] MAXIMUM LIMIT / MINIMUM LIMIT

48TSOP

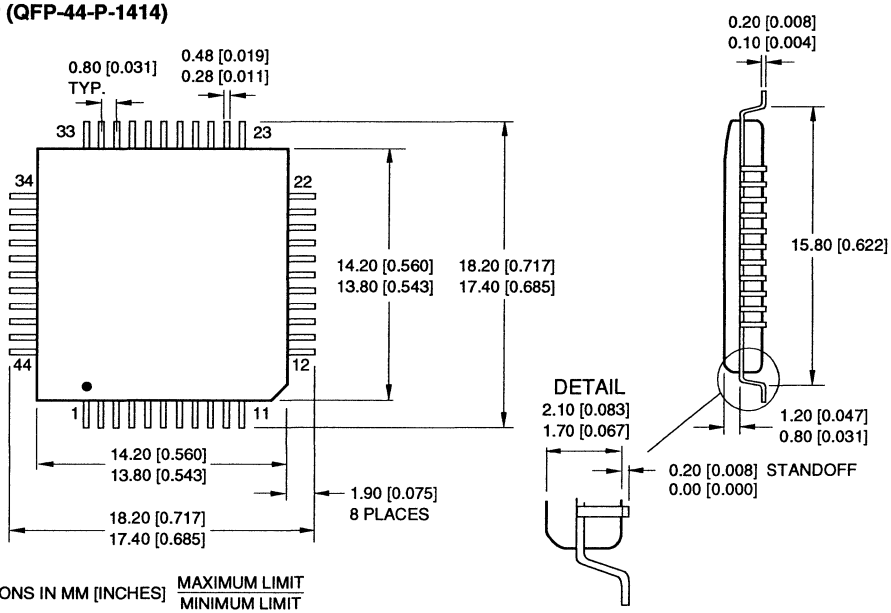
44QFP (QFP-44-P-1010)



DIMENSIONS IN MM [INCHES] MAXIMUM LIMIT / MINIMUM LIMIT

44QFP-1

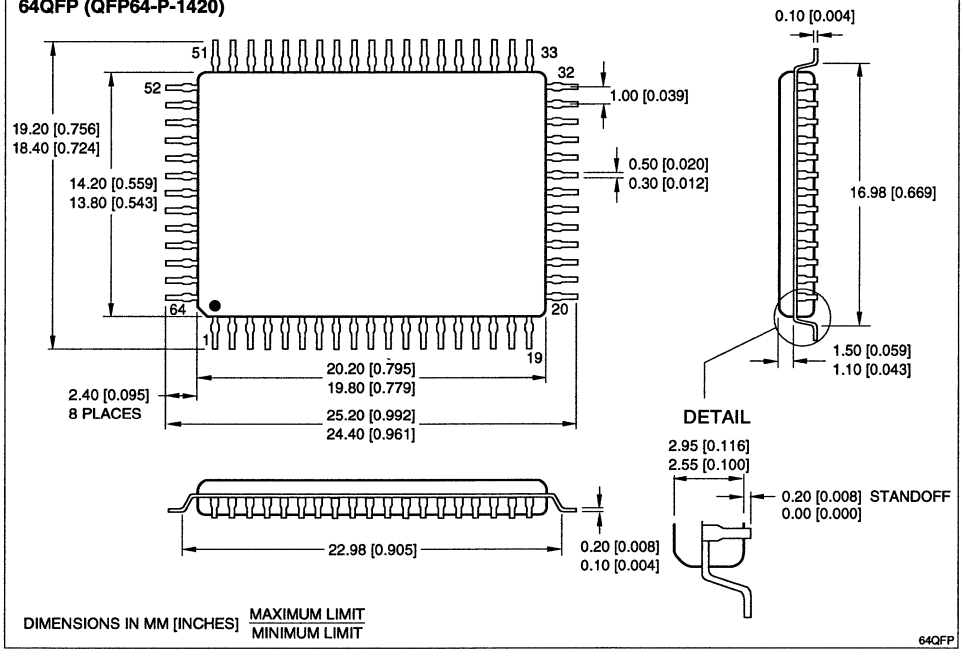
44QFP (QFP-44-P-1414)



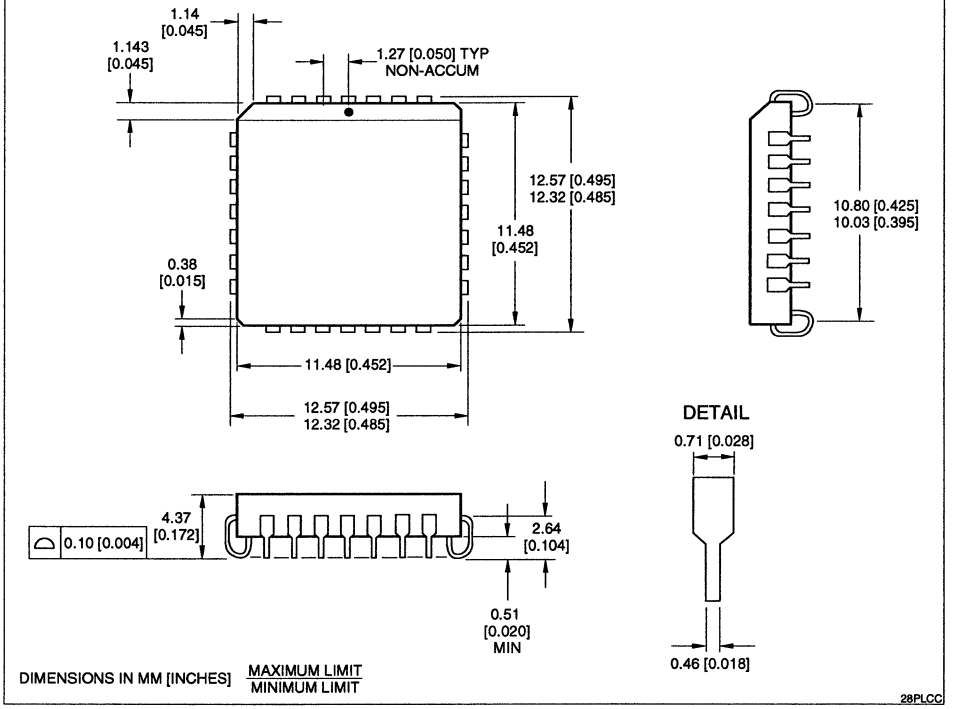
DIMENSIONS IN MM [INCHES] MAXIMUM LIMIT / MINIMUM LIMIT

44QFP-2

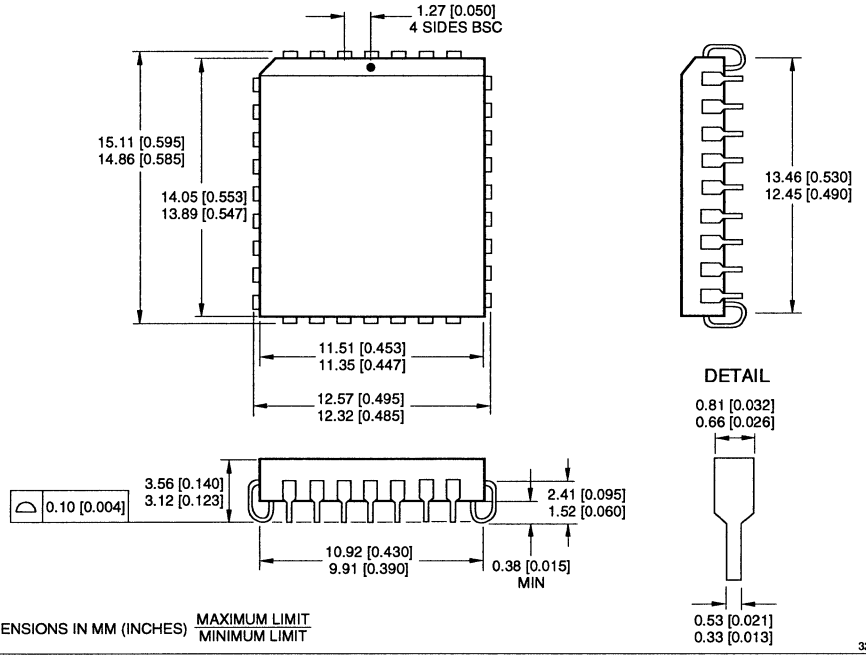
64QFP (QFP64-P-1420)



28PLCC (PLCC28-P-S450)

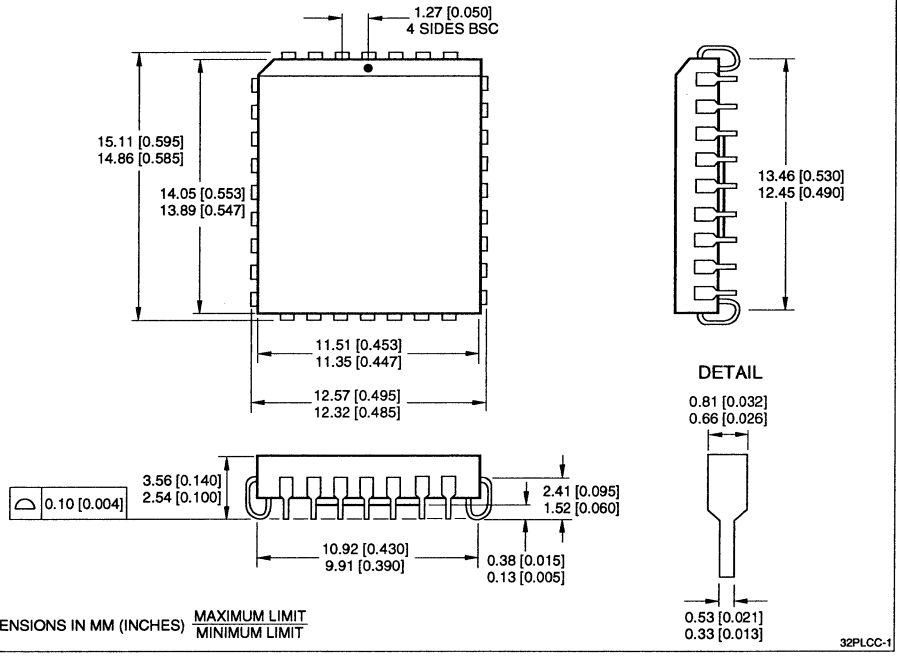


32PLCC (PLCC32-P-R450)



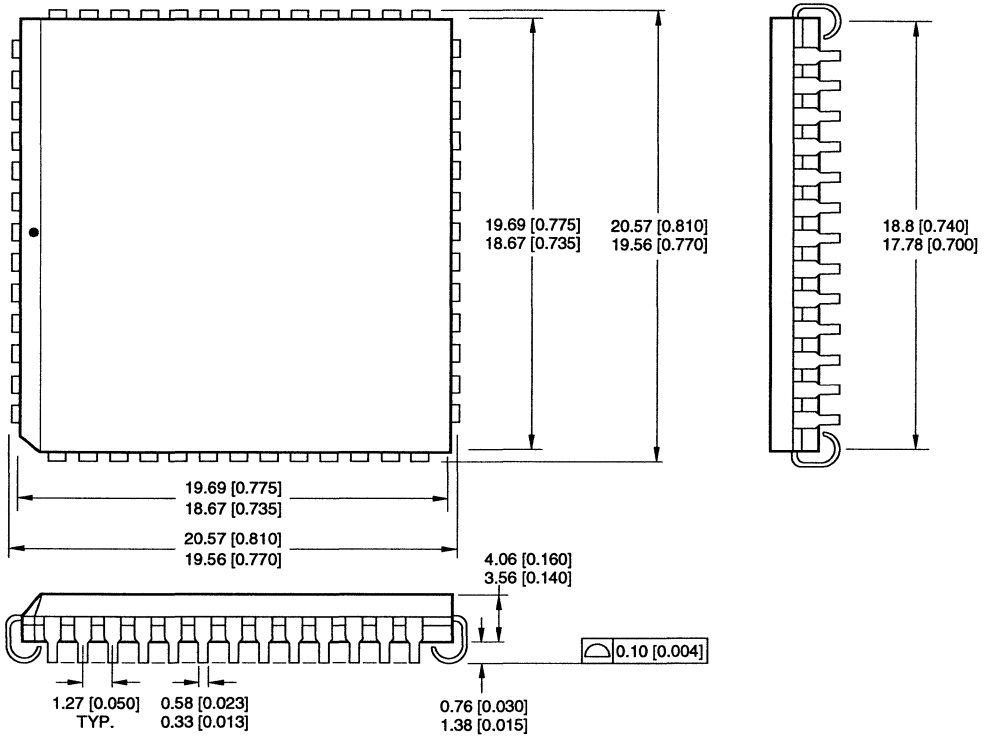
DIMENSIONS IN MM (INCHES) MAXIMUM LIMIT / MINIMUM LIMIT

32PLCC (PLCC32-P-R450-PED)



DIMENSIONS IN MM (INCHES) MAXIMUM LIMIT / MINIMUM LIMIT

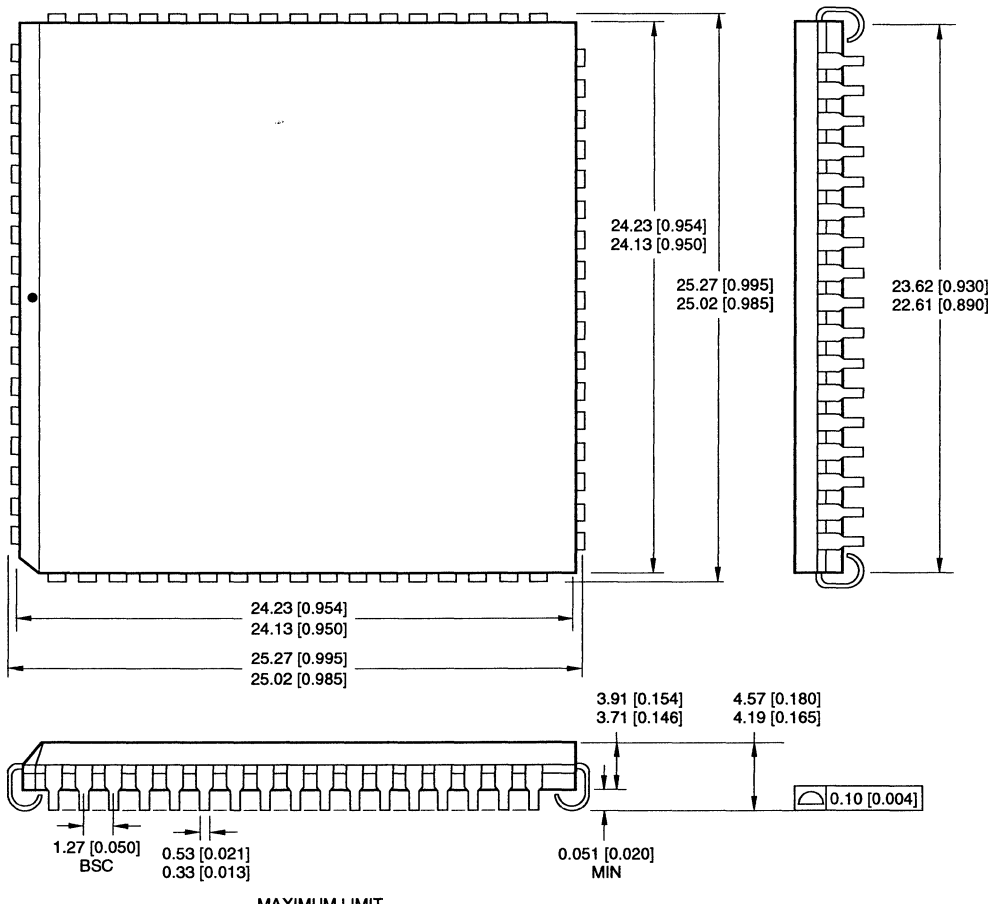
52PLCC (PLCC52-P-750)



DIMENSIONS IN MM (INCHES) MAXIMUM LIMIT / MINIMUM LIMIT

52PLCC

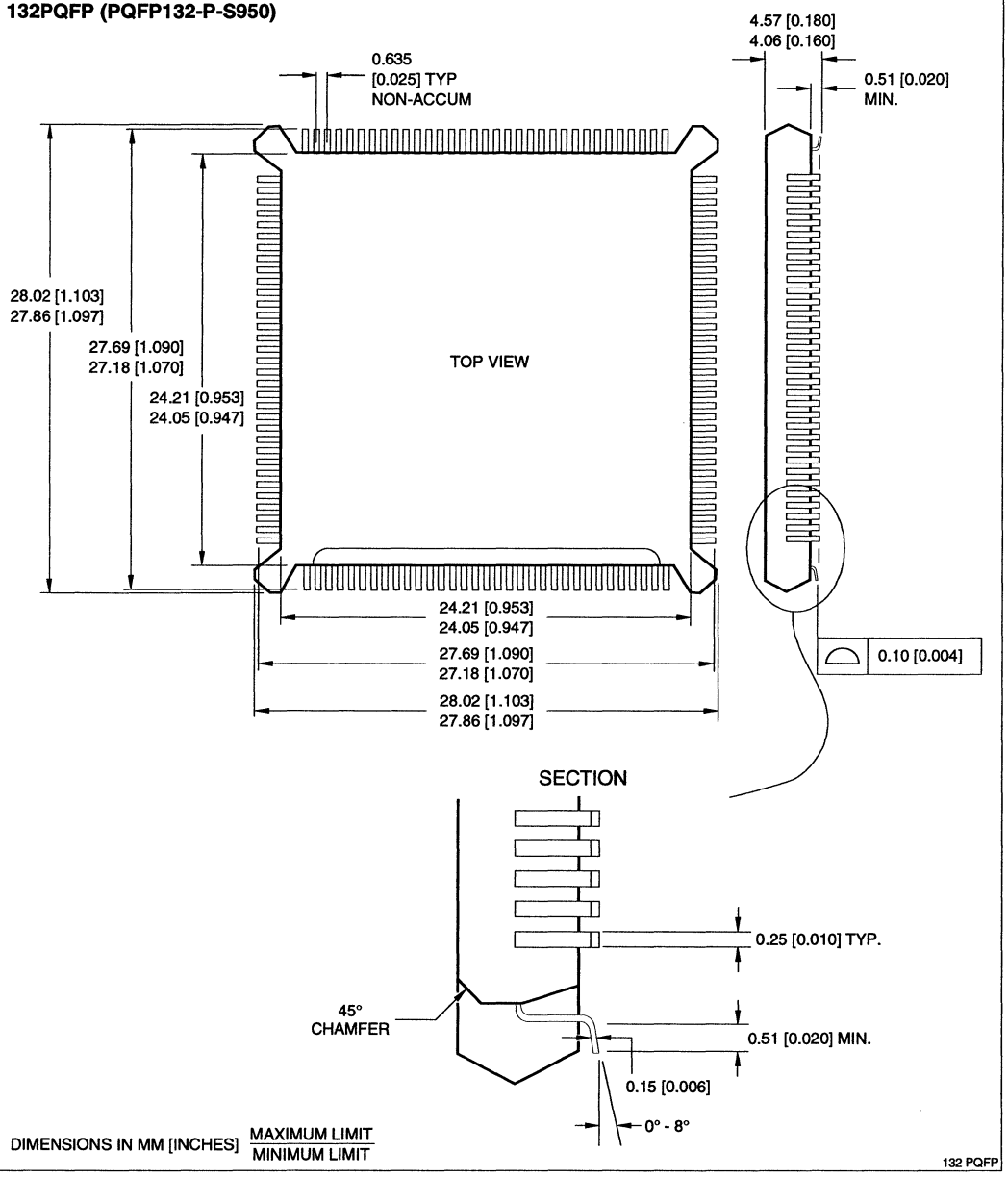
68PLCC (PLCC68-P-950)



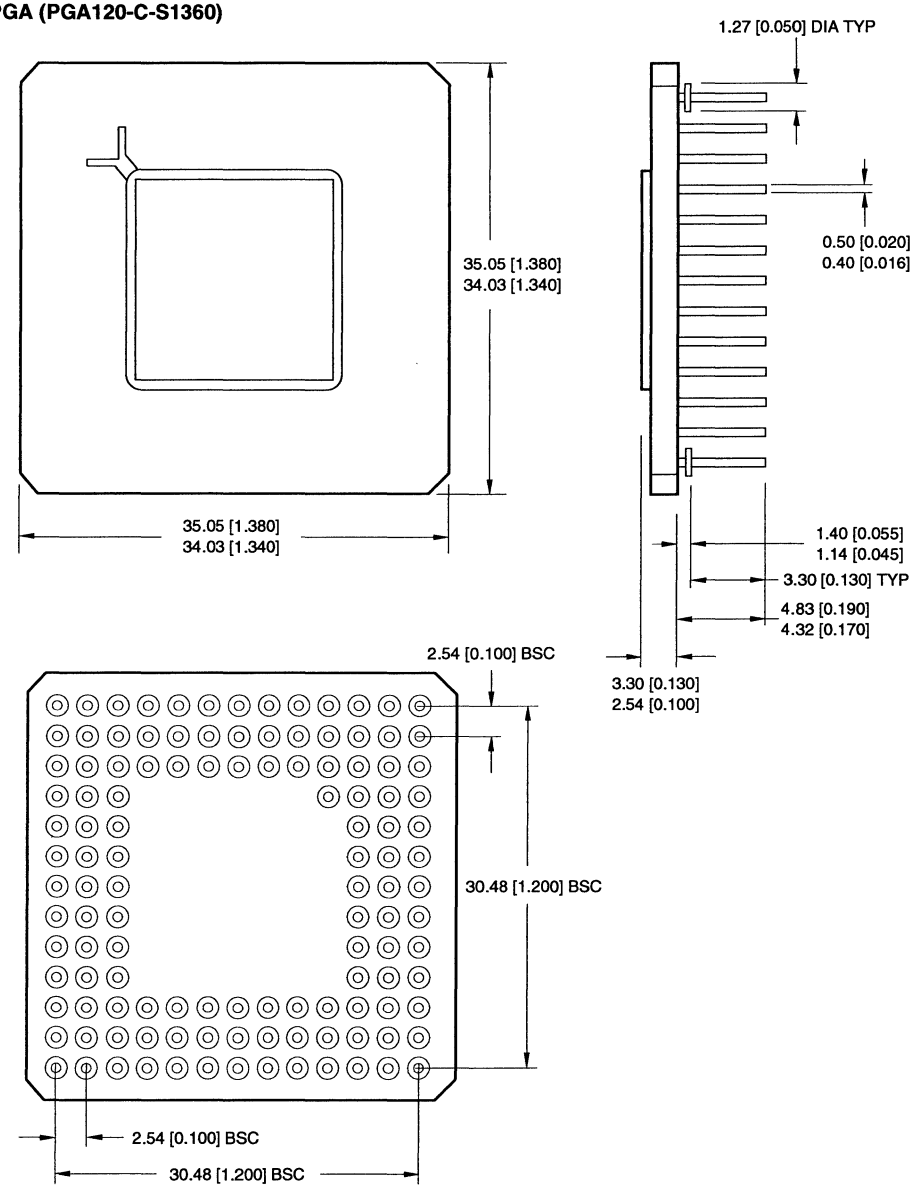
DIMENSIONS IN MM [INCHES] MAXIMUM LIMIT / MINIMUM LIMIT

68PLCC-1

132PQFP (PQFP132-P-S950)



120PGA (PGA120-C-S1360)



DIMENSIONS IN MM [INCHES] MAXIMUM LIMIT / MINIMUM LIMIT

120PGA

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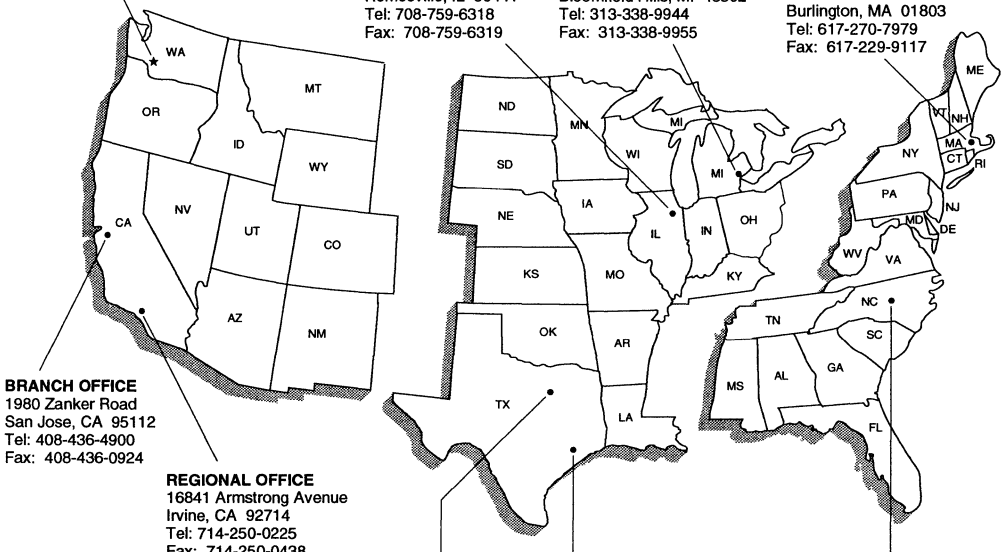

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